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The Application of Forward Error Correction Techniques in Wireless ATM

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Synopsis

The possibility of providing wireless access to an ATM network promises nomadic users a communication tool of unparalleled power and flexibility. Unfortunately, the physical realization of a wireless ATM system is fraught with technical difficulties, not the least of which is the problem of supporting a traditional ATM protocol over a non-benign wireless link. The objective of this thesis, titled "*The Application of Forward Error Correction Techniques in Wireless ATM*" is to examine the feasibility of using forward error correction techniques to improve the perceived channel characteristics to the extent that the channel becomes transparent to the higher layers and allows the use of an unmodified ATM protocol over the channel.

In the course of the investigation that this dissertation describes, three possible error control strategies were suggested for implementation in a generic wireless channel. These schemes used a combination of forward error correction coding schemes, automatic repeat request schemes and interleavers to combat the impact of bit errors on the performance of the link. The following error control strategies were considered :

1. A stand alone fixed rate Reed-Solomon encoder/decoder with automatic repeat request.
2. A concatenated Reed-Solomon, convolution encoder/decoder with automatic request and convolution interleaving for the convolution codec.
3. A dynamic rate encoder/decoder using either a concatenated Reed-Solomon, convolution scheme or a Reed-Solomon only scheme with variable length Reed-Solomon words.

The purpose of the study was to evaluate the performance of the schemes suggested in a simulated environment approximating as closely as possible that encountered by a wireless terminal unit. The principle performance criteria for the scheme was end to end efficiency, while restrictions were placed on the permissible impact on the quality of service parameters of bit error rate, latency and jitter. The simulated operating environments were an indoor pico-cell architecture operating with high carrier frequencies and thus experiencing large possible attenuation characteristics, and an outdoor mobile environment with rapid fading characteristics due to terminal movement. Traffic sources directly considered were CBR voice and real-time VBR, with conclusions for ABR performance inferred from the results obtained for the other traffic classes.

The study methodology involved an extensive simulation process on a custom developed C simulation platform. Theoretical verification of the performance of the modeling platform was also conducted.

The simulation process led to the conclusion that the inclusion of forward error control strategies permits the use of wireless links that would otherwise be useless for wireless ATM transmission. Given an effective error control strategy, the high error rate link becomes transparent to the higher layers. The study further showed that the use of a dynamic rate scheme added significant performance advantages in terms of efficiency, allowing the use of the most economical scheme for the existing channel characteristic.

Declaration

I declare that this thesis is my own work. Where collaboration with other people has taken place, or material generated by other researches is included, the parties and/or material is indicated in the acknowledgements or references as appropriate.

This work is being submitted for the Master of Science Degree at the University of Cape Town, department of Electrical Engineering. It has not been submitted to any other university for any other degree or examination.

Craig Ian McLuckie

Date

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1 Introduction

ATM has been heralded the broadband solution for future network implementations. The advantages of ATM are many – it yields a flexible bandwidth on demand system, supporting a large number of services and offering guaranteed QoS constraints. It is fairly natural to wish to offer the benefits of environment to the nomadic user. The notion of linking the two fields was first proposed in 1992 by D. Raychaudhuri [62]. Since then a considerable amount of research has been conducted in the field and the first ATM forum specifications for wireless ATM are due for release in 1999 [73].

A number of factors have contributed to the massive interest that the prospect of wireless ATM has received:

The first contributing factor to the interest in wireless ATM is the substantial increase in portable processing power that has become available. Powerful applications can now be run on lap-top computers and PDA's (personal digital assistants). Portable terminals are able to support bandwidth hungry applications that users have come to and will continue to demand.

The second major reason for interest in the field of wireless ATM is the exponential growth in demand for both mobile personal communications and high bandwidth multimedia applications since their inception in the past few years. Looking to the future, it seems likely that the merging of the two fields is likely to meet with considerable interest.

Another contributing factor for the interest in wireless ATM is the fact that ATM has been accepted in many areas as the broadband carrier of many communication systems. This includes the third generation cellular phone systems of UMTS and IMT2000 [34]. The final step of bringing ATM to the mobile user is thus a fairly natural one, moving the boundary of the ATM network out the one, final stage.

The substantial increase in demand for wireless LAN style networking in the GHz bandwidth area is another reason for the interest in wireless ATM. Wireless LAN's have grown in popularity because of the flexibility and cost effectiveness they represent (since cabling does not have to be laid). Wireless ATM may prove an invaluable means of connecting non-mobile users to a wireline backbone without the problems associated with cabling installation and maintenance.

The final reason for the interest in wireless ATM is what it may come to represent – the promise of a universal access protocol. Because ATM provides an extraordinarily flexible platform from which to operate, it is not inconceivable that in the future a wireless ATM terminal could provide universal access – that is access to any class of traffic at any realistic data rate, from any user location.

In principle, two possible strategies exist to provide the nomadic user with access to a wired ATM backbone. The first is true ATM – that is extending the ATM interface to the wireless terminal without modifying the cell format in any significant manner. The second means of providing access is to terminate the ATM network at the mobile base-station. Although there are arguments supporting the second method, it is not in truth wireless ATM as described by the ATM forum in the draft version of the wireless ATM specification [75]. It is because true wireless ATM has generally been accepted by the research community as the most likely means of transparently accessing a wired ATM network that this project has been dedicated solely to the study of this field, largely ignoring the possibility of discarding the ATM protocol at the *user network interface* (UNI).

As clear as the advantages of providing wireless/nomadic access to the ATM user may be, the physical process of supporting a wireless link in an ATM environment is not without difficulties. A number of new problems must be addressed by the design engineer if the access technology is to be successful. These problems include shared medium complications, security issues, nomadic support and difficulties relating to poor link quality.

It is the issue of poor link quality upon which this thesis is based, with specific emphasis on improving the performance of a wireless ATM link through the strategic implementation of forward error correction coding techniques.

Forward Error Correction (FEC) coding refers to the process of adding coding overhead to a transmitted data sequence, such that errors introduced into the sequence during transmission may be detected, and in some cases corrected without the requirements of retransmission. The set of forward error correcting codes may be divided into two: block codes and convolution codes. The application of both types will be considered with the Reed-Solomon codes as the suggested block code and a Viterbi decoding based system as the convolution candidate. The objective of this thesis is to explore the feasibility of using forward error correction coding to improve the perceived channel characteristics to the point that standard ATM QoS requirements may be met over a typical wireless link.

1.1 Wireless ATM Implementation Issues

1.1.1 General Implications of Wireless Access in an ATM Environment

The process of supporting wireless access to a wireline ATM environment presents a number of challenges. The wireless environment represents a far more hostile backdrop for the operation of ATM with a number of issues to be considered. These include:

- **MAC (Media Access Control)** – Unlike a fiber operating environment, a single end-user does not have a dedicated end connection. Multiple users are liable to compete for access to the wired network in the same locale. The process of coordinating the access of multiple users to a network raises a number of design issues in terms of bandwidth sharing strategies and the overall control process.
- **Bandwidth Restrictions** – Another issue that, although not unique to the wireless domain, is that of bandwidth restrictions. The problems associated with connection bandwidth are more acute in the wireless environment than in fiber links. The limiting factor with regard to the speed of access to the wireline network is the amount of free and usable bandwidth available. Unlike a wireline link, it is not possible to increase link capacity by laying more and faster pipes. All users must share the finite amount of usable electromagnetic spectrum available. These constraints introduce the necessity for efficient channel modulation schemes, the extensive use of data compression and the use of higher and higher carrier frequencies.
- **Security and User Authentication Issues** – Because a wireless link is a shared medium, the possibility of information snooping and fraudulent access become more significant than in a relatively secure dedicated fiber link. Technologies such as spread spectrum encoding and cryptography become prevalent.
- **Poor Link Quality** – The ATM protocol was intended for implementation in fiber environments where the bit errors are scarce (occur with probabilities in general of less than 10^{-10} [3]). Wireless channels are far less benign, with BER's (bit error rates) often substantially worse than 10^{-4} [21]. It is with this issue that this thesis is primarily concerned.

1.1.2 Implications of High Bit Error Rates on ATM

The nominal bit error rates for fiber environments are low, and it is for this reason that little emphasis was placed on error recovery techniques in the ATM layer. Error control elements are present in the protocol, but these are primarily for the detection of errors and in general result in the discard of the data being transmitted, with the task of error recovery delegated to the AAL or application layers. The error control features present in the unmodified ATM format are listed below:

1.1.2.1 Error Control Features Present in the Standard ATM Protocol Stack

Some error control features are included in the standard ATM format, at the *ATM Adaptation Layer* (AAL) layers and in the cell headers.

1. HEC Field

As part of the standard ATM format, an 8-bit CRC check is applied to the cell header. As part of the 5-byte header, an 8-bit header error correction (HEC) field is defined which performs a polynomial CRC (cyclic redundancy check) on the rest of the cell header. The decoder may be viewed as a two-state state machine operating either in detect only or detect and correct mode. In correct mode the decoder will automatically correct any single bit error in the header. If an error is detected, the decoder will switch over into detect only mode in which any cells with header errors are be discarded. Switch back to correct mode occurs after a cell without header errors is detected. The CRC field is also responsible for detecting synchronization.

Nakayama and Aikawa [57] argue that this standard HEC field is inadequate to ensure header integrity in noisy wireless environments. They suggest that additional error correction facilities be provided.

2. AAL 1,3/4 and 5

AAL refers to the ATM adaptation layer – the transparent interface between the ATM transport layer and the application in use. Each ATM layer is aimed at a specific type of traffic and each has error protection schemes associated with it.

AAL 1 – This adaptation layer is used with constant bit rate connection oriented services with specific timing and delay requirements. The data stream is divided into 47-octet segments, to which are added a 4-bit sequence number and a further 4-bit sequence number protection (a three bit CRC and an even parity bit) to ensure integrity of the SN field. No payload error detection facilities are present.

AAL3/4 – Supports connectionless and connection oriented VBR services. Associated with each cell is a 10-bit CRC check. Any cell failing the CRC check must be retransmitted.

AAL 5 – Supports connection oriented CBR, VBR traffic and ABR traffic. The data stream is divided into frames of no more than 65535 octets. Associated with each frame is a 32-bit CRC check. The SAR layer breaks the frame into 48 octet segments for transmission. At the receiver the frame is reconstructed and the CRC-check performed. If the frame fails the CRC check, it must be retransmitted if required.

1.1.2.2 Application Considerations With Regard to Native Error Control Measures

In a high bit error rate environment, the ATM native error control features are inadequate. To illustrate this, consider the utilisation of an ATM connection over a wireless link with a bit error rate of 10^{-4} (a fairly realistic operating level for a typical wireless link). An AAL 5 frame may consist of up to 65635 bytes of data. The probability of the correct transmission of the entire frame without a single bit error is in the region of 1 in 10^{23} . This is clearly non-feasible and additional facilities are required.

1.2 Assumed Wireless ATM System Architecture

Before the design phase of the project may commence, the envisaged operating environment for the suggested error control strategies must be defined. This definition occurs both in terms of the physical implementation architecture and in terms of the parameter settings for the associated system elements. The following section will describe as clearly as possible the context within which the suggested error control strategies will be placed. The discussion will include the adjustments made to the standard ATM protocol stack in order to support wireless/nomadic access, channel models to yield the transmission bit error rates, selected MAC strategy and traffic classes supported with their associated QoS requirements.

1.2.1 Physical Architecture

As was stated in the introduction, the ATM protocol stack will be retained to the accessing wireless terminal. In order to maintain the ATM system format and introduce new functionality, some modification must be made to the ATM protocol stack.

To support all the functionality of network access, three new elements (above the physical layer) will be added to the classic ATM model at the wireless interface: Wireless Control, Wireless Data Link Control and Wireless MAC (medium access control). The basis for this assumption is provided in [60;61].

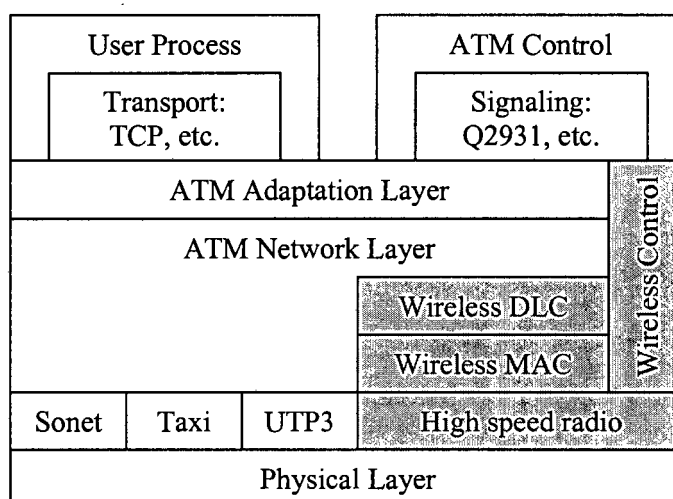


Figure 1-1 : Additions to the ATM Model to Support Wireless Access

1.2.1.1 Wireless Medium Access Control (MAC)

The MAC algorithm for a wireless ATM environment is presented with a number of problems that must be overcome. These include the wide variety of services that must be supported and their widely different constraints they place on the system. The MAC protocol must also be able to operate with the non-benign channel characteristics that represent the ATM environment.

The media access control segment will be subdivided into the *supervisory MAC (S-MAC)* and the *core MAC (C-MAC)*. The S-MAC is responsible for high level functions such as slot allocation and QoS management. The C-MAC is responsible for high speed functions such as multiplexing according to the multiple access scheme and transmission/reception.

1. Supervisory MAC

The S-MAC processes the control information received from higher levels and generates a *schedule table*. This schedule table is based on the control information received via meta-signalling from the wireless control layer. In this instance, meta-signalling refers to the process of passing control information embedded in standard ATM cells between layers via dedicated VCI/VPI pairs. Each entry in the table contains information regarding the type of service (transmission/reception), message type (information/control), VCI, position and duration of service. In the generation of the table, the S-MAC attempts to fulfil the QoS requirements for all of the services in use, by VC. The S-MAC at the network access point is also responsible for slot allocations on both the up and down links for data and control information transactions. It is also responsible for call admission control.

2. Core MAC

The C-MAC architecture is a candidate for hardware implementation as it is system specific and needs to operate at very high speeds. It functions largely as the interface between the physical DLC and the physical medium. Because all control aspects are delegated to the S-MAC, the access point and terminal C-MAC's are essentially the same. Based on the information supplied by the S-MAC in the schedule table, transmissions and receptions are multiplexed or de-multiplexed for each existing VC.

1.2.1.2 Wireless Data Link Control (DLC)

The data link control layer provides the link between the MAC layers and higher levels. The core function is error control and it is here that the error control schemes suggested in later chapters would be implemented. At this level cell sequencing would also take place. The exact action of the DLC would be service dependant (as the system constraints are generated by the needs of the service supported).

1.2.1.3 Wireless Control

The wireless control layer is responsible for overseeing all the functions that must be introduced to support wireless access, including mobile identification assignment at startup, MAC layer control, handoff, transmitter/receiver control (frequency and power management). Communication with the base station occurs via meta-signaling which is passed to the DLC and MAC layers, but at the receiving entity is not passed to the ATM layer.

1.2.2 Channel Models

It is necessary to select channel models for the simulation procedure that emulate the physical channels the error control schemes may be expected to operate under as closely as is feasible. From the communication engineer's perspective, the single most important characteristic of a wireless channel is the moment to moment bit error rate. For a wireless link, the moment to moment bit error rate is determined by the received signal to noise ratio at the terminal.

1.2.2.1 Factors Affecting Channel Characteristics

A number of factors have been identified as being responsible for the variation in channel characteristics in a wireless environment and hence are sources of error in the transmission of data over a wireless channel. These include :

- Attenuation due to dispersion. As the receiver is moved further and further from the transmitter, natural received power loss occurs proportional to the square of the distance from of the link.
- Attenuation due to objects in the transmission path. Ignoring the dispersive effects of a change of medium, some transmitted power loss must occur as an electromagnetic wave moves through a non-vacuum.
- Multipath interference. When a electromagnetic wave encounters a change in medium, inevitably reflection and refraction occur. This may cause a number of possible paths to the receiver from the transmitter, all of different lengths. Phase differences associated may lead to destructive interference and hence signal power reduction.
- Front end overloading. Front end overloading occurs when filters in a transmitter are unable to remove the effects of a powerful alternative source radiating at a frequency close to that used by the channel. This leads to interference and the introduction of errors.
- Narrowband interference. This occurs when narrowband applications have a small overlapping segment of frequency that results in interference.
- Spread-spectrum interference. In a spread-spectrum environment the signal power is dispersed over a wide bandwidth in an effort to make the best use of the frequency space available. Even in a perfectly operating system, some interference resulting from peer spread spectrum devices is inevitable.

-
- **Background noise.** Background noise is inevitable and unavoidable and may result from any of a number of factors such as spurious signals received from surrounding cells and thermal noise.
 - **Motion.** The Doppler effect results in perceived frequency shifting at the receiver.
 - **Data dependant effects.** Clock synchronisation may be lost in certain environments with the transmission of certain data sequences. This is implementation specific.

Clearly the specific operating environment of a channel determines the magnitude of the effect of each of the above listed characteristics. In a simulation environment, it is not ordinarily feasible to consider all of the above factors. The wireless environments chosen embody a few of the most significant aspects of channel degradation and the others are ignored.

1.2.2.2 Channel Models Selected for Evaluation of Error Control Architecture

To best evaluate the performance of the error control architecture that the author intends to propose, the intended operating environment for the scheme must be stipulated and modeled as accurately as possible. One approach to the process would be to select a single operating environment, for instance an indoor pico-cellular architecture with a very high data rate, and work from that position. The goal of the project is however to develop a generic, flexible error control architecture, instead of tailoring one specifically to the characteristics of the operating environment. It is for this reason that two channel models will be implemented, each highlighting specific difficulties from the developers perspective. The models that will be developed are as follows:

1. Environment 1: Indoor Pico-Cellular Architecture.

The first simulation environment will be the high data rate indoor environment such as that encountered by wireless LAN's. In this environment it will be assumed that the user is stationary and that channel characteristics variation will be relatively slow.

Distances between the user and the base station will be measured in 10's of meters (hence the pico-cellular architecture). Carrier frequencies will be in the region of 20GHz with data rates in excess of 50Mb/s.

The principle influencing factor of the scheme will be simple attenuation due to objects in the transmission path and distance to the antennae. Other factors influencing the received signal to noise ratio will not be considered. This channel model will be dominated by slow but extreme shifts in bit error rates with random, independently and non-auto-correlated bit errors.

2. Environment 2: Outdoor Cellular Architecture

This assumes an outdoor cellular architecture with a mobile user travelling in an automobile at a velocity of 60km/h away from the base station. The user will be assumed to be near the edge of the cell with distance between the base station at around 1km. This channel will be subject to Rayleigh fading.

The peak data rate will be assumed to be 400kb/s with a 1.8GHz carrier.

The variable signal degradation aspects represented by this scheme will be the effects of attenuation due to multipath effects, attenuation due to distance, attenuation due to objects in the transmission path, and effect of Doppler fading. All other signal to noise ratio influencing aspects will be ignored by the channel. This channel type will be dominated by slow fading effects due to changes in the transmission path, and also rapid fading, auto-correlated or burst errors due to Rayleigh fading.

1.2.3 MAC Strategy

It will be assumed that a *time division multiple access* (TDMA) technique will be used to provide multiple users access to the shared channel medium.

With the TDMA system, time slots are allocated to by the controller to the competing users in the cell. This system will assume the use of a dedicated control slot used to handle slot allocation and de-allocation. A schematic representation of the TDMA system is given in Figure 1-2.

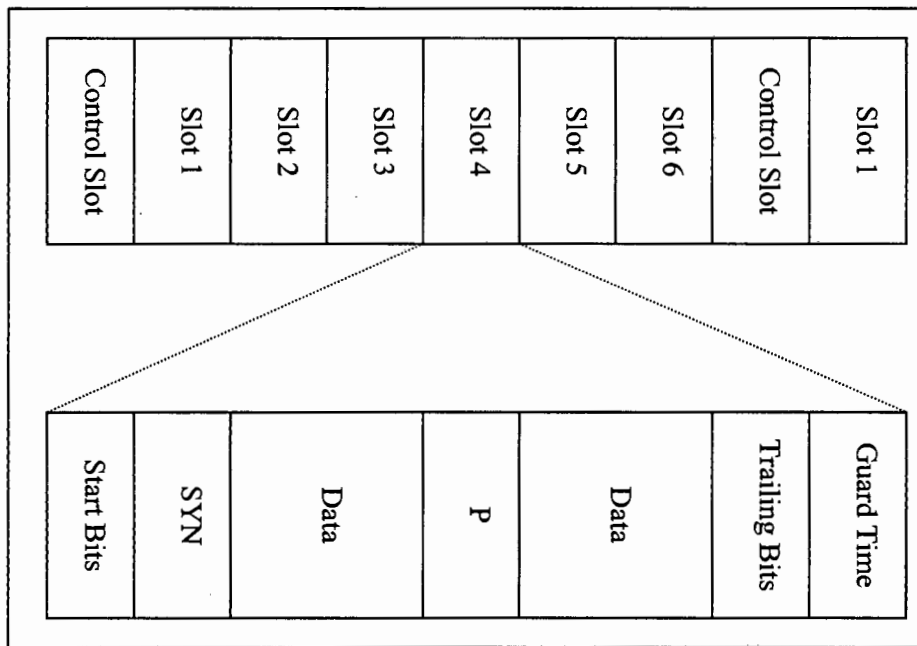


Figure 1-2 :TDMA Schematic Representation

Each slot starts with a series of start bits, followed by a SYN sequence to aid the synchronisation process. Data segments follow with the possible insertion of a known sequence P that may be used to gauge the moment to moment channel impulse response for applications such as adaptive filters. The final data segment is terminated by a series of trailing bits and a transmission NULL segment may be included to avoid collisions in transmissions.

1.2.4 Traffic Classes Supported

The evaluation process for the schemes that are to be developed will essentially involve estimating their performance in a real physical environment with real traffic. It is for this reason that a broad selection of traffic types with varying QoS requirements will be selected.

The traffic classes that will be considered include:

- Real-time CBR.
- Real-time VBR.
- ABR.

1.3 Thesis Objective and Development Methodology

The title of this thesis is “*The Application of Forward Error Correction Techniques in Wireless ATM*”.

The fundamental premise upon which the project is based is that the strategic application of forward error correction techniques, when applied with other feasible error control techniques at the physical or data link layers, may improve the perceived quality of a wireless access link from the perspective of the higher network layers to the point where the link itself becomes transparent to these higher layers.

Broadly speaking, the objective of the thesis is to propose and evaluate a generic error control strategy that may be applied to commonly encountered wireless channels. The proposed scheme should be as flexible, powerful and broadly applicable as possible, without adding any more transmission overhead than necessary. The scheme should also be feasible from an implementation perspective and not break the *quality of service* (QoS) bounds specified by the traffic classes that use it.

The development procedure for the project that this dissertation documents may be described as follows:

1. A general research segment to define as clearly as possible the issues relating to the intended undertaking.
2. With the knowledge gained relating to the research topic, to develop a series of design criteria by which the performance of the suggested error control architectures may be evaluated.
3. By referring to published material on the topic, to suggest a series of likely candidates for the final error control architecture.
4. A preliminary evaluation of the schemes suggested using a custom developed computer based simulation procedure.
5. A refining process and more extensive evaluation procedure, making use of the information gained in the preliminary study to make improvements to the suggested error control schemes and to define areas requiring further investigation.
6. Mathematical substantiation of the simulation findings.
7. A critical evaluation of the findings to suggest the most feasible means of introducing forward error correction techniques to the wireless ATM environment.

1.4 Dissertation Structure

The structure of this dissertation is intended to match as closely as possible the logical development of the project it represents.

Chapter 1, including this section, introduces the topic and attempts to specify the objective of the research project, defining the specific operating constraints of the system that is to be developed.

Chapter 2 lists the quality of service constraints that must be adhered to by any error control strategy introduced.

Chapter 3 introduces means of combating the effects of high bit error rates in wireless ATM and describes the tools that will be applied to this effect.

Chapter 4 introduces three error control schemes that may be used in a physical system. These schemes are based partially on work undertaken by other researches and referenced in turn, and partially on ideas generated during the study period before the tangible work on this project commenced. The error control mechanisms that will be considered for implementation will consist of a combination of Reed-Solomon block codes, convolution codes with Viterbi decoding, selective repeat request automatic repeat request elements, and cyclic redundancy checks. The schemes introduced in this section are as follows:

- A stand alone Reed-Solomon forward error correcting mechanism operating with a 1 cell word.
- A concatenated coding system consisting of a Reed-Solomon outer code with a convolution inner code, applied to frames of 4 complete ATM cells.
- An adjustable rate code, able to operate as either of the first two models, with adjustable length frame sizes.

All of the suggested schemes would operate with a 32 bit cyclic redundancy check triggering selective automatic repeat requests should the forward error correcting strategies fail.

Chapter 5 describes in detail various facets of the assumed operating environment of the simulation platform that was developed for the testing of the schemes introduced in Chapter 4. Detailed descriptions and derivations of the channel models and traffic models are given, along with the operating assumptions for the environment and envisaged restrictions to be placed on the simulation platform.

Chapter 6 provides insight into the design and operation of the simulation platform that was developed to test the performance and feasibility of the error control strategies presented in this thesis.

Chapter 7 details the testing of the principle components of the simulation platform.

Chapter 8 provides a detailed list of the simulations performed to evaluate the error control schemes. For each test is presented the objective of the test, test methodology including operating parameters and results in tabular and graphic format.

Chapter 9 presents an interpretation and analysis of the simulations and provides commentary of the schemes' performances, based upon the simulation results.

Chapter 10 documents a theoretical study to predict bit and header error rate performance.

Chapter 11 details the conclusions reached from the presented theoretical and simulated results.

Chapter 12 presents recommendations and details areas for future research.

The body of the dissertation is concluded with a *glossary* and the project *bibliography*.

Information relevant to the topic either as background or theoretical justification, but not directly affecting the progression of the dissertation is included in a series of appendices.

Appendix A provides insight into the operation and performance of a Reed-Solomon Codec.

Appendix B provides insight into the operation and performance of a convolution encoder and Viterbi Decoder.

Appendix C provides insight into the operation and performance of a CRC.

Appendix D details the action of the convolution interleaver employed in the project.

Appendix E lists the files used in the simulation platform project.

2 Quality of Service Constraints

The evaluation process for the schemes that are to be developed will essentially involve estimating their performance in a real physical environment with real traffic. It is for this reason that a broad selection of traffic types with varying QoS requirements will be selected.

The traffic classes that will be considered include:

- Real-time CBR.
- Real-time VBR.
- ABR.

For each of the traffic sources, the QoS requirements are described in terms of end to end latency, jitter tolerance and tolerable bit error rate. The QoS requirements by traffic class are obtained from a discussion in [6].

It should be noted that the latency described is the maximum end to end latency for any single data bit, and packetization delays are not accounted for on a per cell basis.

In the context that follows, cell jitter will be referenced by the time difference between the earliest delivery time for any cell and the latest. The latency statistics yield the largest delivery time for any data element, and it follows logically that jitter may be eliminated through the use of buffering to ensure that no cell is delivered before this time. So long as the latency introduced does not break the specified QoS constraints and buffering is physically feasible, the elimination of jitter in this manner is viable.

2.1 CBR Traffic Class

For the purposes of evaluation, the CBR traffic type used will be a 64kb/s voice connection.

2.1.1 Voice Error Rate Requirements

For identically, and independently distributed (IID) random bit errors, it is accepted that an average bit error rate of 3×10^{-5} may be tolerated without being perceptible for a 64kb/s PCM voice link.

ITU Recommendation G.821, further makes allowance for unevenly distributed error rates. It states that to fall within acceptable limits:

- Fewer than 10% of 1 minute intervals may have BER's in excess of 10^{-6} .
- Fewer than 0.2% of 1 second intervals may have a bit error rate in excess of 10^{-3} .
- Fewer than 8% of 1 second intervals may have any bit errors.

2.1.2 Voice Latency Requirements

The ITU specifies that if the delays on a line are in excess of 25ms, echo control must be applied to the link. Assuming the use of full echo cancellation, the absolute level of latency is an issue of contention. Figures ranging from 100ms to 600ms for acceptable latencies on telephonic connections have been stipulated.

For the sake of analysis, we shall assume that the maximum permissible latency for a telephonic type connection is 250ms end to end.

If both participants in a telephonic conversation use wireless access technologies, the maximum latency introduction due to the access scheme on each side would thus be 125ms without any transmission delay.

For the sake of evaluation, a 100ms latency ceiling will be applied (the maximum acceptable latency introduction by the error control scheme is 100ms). Further, from the evaluation point of view, the further inside the 100ms boundary the better.

2.1.3 Voice Jitter Requirements

With any system, jitter may be traded off for additional introduced latency through the introduction of adequate buffering. Instead of specifying jitter requirements for the traffic classes, buffering requirements to eliminate jitter will be estimated. Traffic classes that are jitter sensitive will thus be treated as jitter intolerant, no perceivable output jitter will be tolerated. Through the process of handling jitter in this manner, latency becomes the only timing criterion so long as buffering is feasible.

2.2 VBR (Real-time) Traffic Class

For the purpose of the evaluation, the real-time VBR traffic type used will be a real-time compressed MPEG-1 video stream.

2.2.1 MPEG-1 Video Stream Error Rate Requirements

The quoted acceptable bit error rate for 1.5 Mb/s inter-frame coded video traffic is 10^{-9} to 10^{-10} .

The maximum acceptable error rate will be taken as the most pessimistic of the error range, namely 10^{-10} .

2.2.2 MPEG Video Stream Latency Requirements

The voice stream associated with the MPEG1 video stream is not embedded with the video data. It occupies a separate stream. The maximum delay constraint will thus be taken as being equal to that for the voice channel and set at 100ms.

2.2.3 MPEG Video Stream Jitter Requirements

As with the voice stream, the MPEG stream will be treated as jitter intolerant.

2.3 ABR (Traffic Class)

For the purpose of the evaluation, the ABR traffic type used will be a simple data transfer such as an FTP transaction.

2.3.1 Data Transfer Error Rate Requirements

For data transactions, the acceptable error rate is ascertained by the required link efficiency and frame length, given that an errored data frame must be retransmitted.

Assuming a frame length of 64kB, and a required end to end efficiency of 95%, the acceptable BER p_b would be that such that:

$$0.95 = (1-p_b)^{8 \times 65535}$$

Solving the above equation yields an acceptable error rate of $p_b \approx 10^{-7}$

2.3.2 Data Transfer Latency Requirements

For a non-real-time application, the impact of latency is not significant as long as it is kept within finite bounds. For this application, the maximum allowable latency will be set at 1s as an arbitrary upper bound.

2.3.3 Data Transfer Jitter Requirements

Jitter plays no significant role in data transmissions. Early packet delivery will not adversely affect performance.

3 Error Control Techniques for Wireless ATM

Before addressing the problem of improving robustness of a wireless link supporting ATM traffic in the face high bit error rates, possible tools available to this end must be listed. A number of means of improving a wireless link exist from the perspective of bit error characteristics. These include physical level improvements, *forward error correction* (FEC) techniques, *automatic repeat request* (ARQ) facilities, interleaving, and hybrids of these elements.

3.1 Physical Level Improvements

A number of attempts may be made at the physical level to improve the channel for the transmission of digital information. Physical level improvements include the utilization of antennae diversity both at the base station [15], and in the case of certain modern applications, at the mobile itself [34], the utilization of dynamic filters and spectrally efficient modulation techniques.

3.2 Forward Error Correction Techniques

FEC coding refers to the process of appending additional coding overhead to the data transmitted over the channel. The decoding operation that is performed on the received word consisting of the original data plus the overhead allows for the detection and correction of certain error sequences. The forward error correcting codes may be divided into block codes and convolution codes.

3.2.1 Block codes

Block code type operations are performed on a fixed length data block. The data to be protected must be buffered, encoded, transmitted, and then buffered again before the decoding process may be initiated. When referring to block codes, the notation (n, k, t) will be used where:

n is the number of symbols in the code word. In a binary code each symbol is a bit, but non-binary codes are often also used.

k is the number of data symbols in the code word.

t is the number of random symbol errors that may be corrected by the code.

Examples of block codes are the Hamming codes, BCH codes and length specific non-binary extensions of the BCH codes, the Reed-Solomon codes. In the context of the wireless channel, Reed-Solomon codes are the most commonly used of the block codes since their performance is optimal from a distance point of view [7]. The Reed-Solomon codec will be that chosen for block codes in the work that follows.

For a complete description of the Reed-Solomon code, please refer to the Appendix A.

With slight relative performance degradation, a more versatile set of codes may be derived from any given Reed-Solomon code by shortening the code word. Shortened RS codes are generated by stuffing the non-data segment of the code-word with 0's and applying the coding technique. Since the code is systematic, the data segment may be transmitted as it stands with the appended FEC overhead appended at either the beginning or the end. At the receiver, the full length code word is once again generated by stuffing the code word with zero's and decoding. In this manner multiple length code words may be generated from a single RS codec.

3.2.2 Convolution Codes

Unlike block codes, convolution codes are applied in a stream like manner. Data for transmission retains the stream properties and there is no fixed length code word. The standard manner of referencing a convolution code is by the rate which refers to the ratio of the input stream length to the output stream length. The coding rate may vary from 1/3 to 4/5. Other parameters for the code are the *constraint length* (k) and the coding polynomials.

A number of decoding techniques for the convolution codes exist including sequential decoding, Viterbi decoding, and others. Viterbi decoding with hard decisions will be used as it is easily implemented in terms of physical hardware and is one of the most commonly encountered forms of decoders. Hard decisions will be implemented since although soft decisions may yield some performance advantages, they require direct access to the receiver

for decoding information and would prove impractical for the generic simulation platform that is to follow. Their utilisation would not however fundamentally change any findings, merely degrade the possible performance results marginally.

Complete descriptions of the convolution encoding algorithm and the Viterbi decoding algorithm are included in Appendix B.

3.3 Automatic Repeat Request

The automatic repeat request process involves a checking procedure which verifies data received and then in the event of errored data, sends a repeat-request to the transmitting entity, requesting retransmission of the errored segment.

The presence of an error is generally determined by some type of parity check - usually a CRC (cyclic redundancy check). A CRC is a polynomial code that is generated by taking the remainder when a polynomial representing the code stream is divided by a generator polynomial.

Two classes of ARQ exist, stop-and-wait and continuous. With a stop-and-wait ARQ system, the transmitter sends a data packet and will not send anything else until the recipient acknowledges its correct arrival or asks for retransmission (ACK – acknowledge or NACK – negative acknowledge). In continuous ARQ systems a continuous stream of packets is sent and retransmission only occurs when the sender receives a NACK from the recipient. The recipient may request retransmission of the errored packet and all subsequent packets (referred to as a go-back-n system) or only the errored packet (referred to as a selective-repeat-request system).

Clearly the continuous system offers better channel efficiency than the stop-and-wait system and inside the continuous system the go-back-n protocol is less efficient than the selective repeat system.

Only the selective repeat request system will be considered for implementation in the applications developed. The justification for this is that although the implementation of such a system is necessarily more complex than for other schemes, it does offer significant performance advantages in terms of throughput efficiency.

3.4 Hybrid Schemes

Hybrid schemes refer to the combination of FEC and ARQ in an attempt to optimise channel performance. Two types of hybrid scheme have been defined:

3.4.1 Type I Hybrid Scheme

A type I hybrid scheme represents the most obvious combination of FEC and ARQ. Each segment of data transmitted has a FEC appended to it. At the receiver, the FEC overhead is decoded, and if no errors or a recoverable number of errors have occurred, the data is recovered from the code word. If an uncorrectable number of errors have occurred, an ARQ NACK is triggered.

3.4.2 Type II Hybrid Scheme

A type II Hybrid scheme offers many performance advantages over a plain ARQ system without the introduction of additional FEC overhead in the data. Like a plain ARQ system however, every error received triggers an ARQ.

The type II hybrid scheme works by generating a rate $\frac{1}{2}$ block code for each data segment to be transmitted. The word that is transmitted is the first half of the code with an additional CRC appended to it. The second half of the code is buffered in case a NACK is received later. On reception of the word, the CRC code is checked to ascertain whether errors have occurred – if they have, a NACK is generated and the transmitter sends the second half of the rate $\frac{1}{2}$ code with its own CRC attached to it. Should this second word be received without errors, the first half is discarded and the data extracted directly from it. If the second half of the word is also errored, the two halves are combined and the resulting rate $\frac{1}{2}$ code decoded. If there are still too many errors for recovery, the first half of the code is resent and the process continued with the second half of the code retained.

3.5 Interleaving

Interleaving refers to the process of mixing the symbols of forward error correcting codes with one another across code-words, or inside a single code-word , depending on the nature of the coding scheme. The reason for the interleaving process is to de-emphasise the impact of burst errors on the error correcting code.

4 Proposed Error Control Schemes

In the study, three different error control schemes will be considered for implementation. Each scheme will be constructed from fixed set of error control tools suggested by [25]. These tools are as follows:

Selective repeat request ARQ element triggered by a 32 bit CRC check.

Reed-Solomon Codec (255,239,8) that may be shortened to yield different length codes.

Convolution Codec with Viterbi Decoding Algorithm (hard decoding decisions will be used in the implementation).

Using the above possible tools, 3 error control schemes were devised and will be tested against various performance criteria for efficiency in realistic wireless operating environments.

Associated with the error control schemes will be certain support mechanisms necessary for the correct operation of the systems proposed. These include:

CRC32 check – the CRC check is necessary for the operation of the ARQ schemes. The ARQ is triggered by failure of this element.

Cell sequence number – the entire contents of each ATM cell transmitted over the wireless link is liable to be protected by a CRC32 check, and any errored cell will be discarded and re-transmitted. The HEC field thus becomes redundant with regard to the wireless link segment. What is however required for the operation over the wireless link segment is a cell re-sequencing number. ATM guaranties cell order preservation, but the operation of a selective repeat request element necessarily re-orders the cells. Some means of recovering cell order is thus required and this is suggested as a simple solution. This may however prove to be non-optimal for wireless environments with mobility support. Mobility support, like the ARQ process may introduce cell re-ordering problems. If end to end cell order information is used (for instance in the cell payload), this information could also be used to re-establish cell order after wireless transmission.

Interleavers – As stated earlier, interleaving is a technique that may be used to improve the performance of error correction schemes by spreading errors across a greater code segment. In the case of convolution codes the interleaving process is performed at a bit level and distributes burst errors in the time domain, allowing the decoder a greater chance of retaining the correct decoding path. In the case of Reed-Solomon codecs, interleaving is used at the

symbol level and is used to spread burst type errors across multiple code words, increasing the probability that errors may be transparently recovered. The cost of the use of interleavers is the systematic introduction of latency.

Buffers – Since each coding element has different operation rates and data lengths, buffering between stages is necessary for the operation of the system. This is clearly also necessary for the operation of the ARQ scheme (the information to retransmit must be held at the transmitter for some time after transmission, should the receiver request re-transmission).

4.1 Scheme 1: Fixed Rate Reed-Solomon Codec with Selective Repeat Request ARQ Element

The first proposed scheme involves a fixed rate Reed-Solomon codec protecting the data transmitted. The specific Reed-Solomon code used would be determined by the nature of the channel to be used. Possible candidates for the scheme are shortened versions of the classic (255,239,8) Reed-Solomon codes:

- (232,216,8) – Four complete ATM cells plus an additional CRC32 check for ARQ purposes.
- (179,163,8) – Three complete ATM cells plus an additional CRC32 check for ARQ purposes.
- (126,110,8) – Two complete ATM cells plus an additional CRC32 check for ARQ purposes.
- (73,57,8) – One ATM cell plus an additional CRC32 check for ARQ purposes.

Considering the nature of the channels that will be used in the evaluation of the error control schemes, the most powerful of the codes (73,57,8) recommends itself as the most useful candidate and this code will hence be used in the tests that follow. For relatively benign wireless links, the less powerful schemes may be closer to the optimal coding levels.

4.2 Scheme 2: Fixed Rate Concatenated Reed-Solomon / Convolution Codec with Selective Repeat Request ARQ

The second scheme proposed is that suggested by Cain and MacGregor in [7]. This coding scheme utilises a concatenated codec with a Reed-Solomon outer code and a convolution inner code. The concatenated code uses the fact that the Reed-Solomon and convolution coding schemes naturally complement one another. The convolution code is very good at recovering from random bit errors, and when it fails it produces burst errors. The Reed-Solomon code has strong burst error correction facilities since each works on a symbol by

symbol basis (there is no additional penalty in the decoding process for the introduction of a full symbol error over that for the introduction of a single bit error). This means that Reed-Solomon codec performs relatively worse in a random bit error environment for the same nominal bit error rate as it would in a burst error environment. Applying the Reed-Solomon codec after the convolution codec thus yields significant performance advantages. The codes adapted from the Cain and MacGregor scheme are as follows:

Reed-Solomon Outer Codec: Cain and MacGregor used a (228,212,8) shortened code. This will be extended to the (232,216,8) code to allow for the introduction of the CRC32 check in the simulation process.

Convolution Inner Codec: The convolution inner code used will be a constraint length 8 code with the Viterbi decoding algorithm. The initial convolution code rate will be set at $\frac{1}{2}$, but this may be adjusted if necessary.

4.3 Scheme 3: Dynamic Rate Concatenated Reed-Solomon / Convolution Codec with Selective Repeat Request ARQ.

The motivation for the use of a dynamic rate coding scheme is that the wireless environment operates with a very wide range of channel characteristics, not all of which vary rapidly or unpredictably. Since the nominal bit error rate is not constant, it is not possible to select one coding rate that will perform at optimal levels. It seems logical that the ability to adjust the coding gain provided by the FEC elements depending on the moment to moment channel characteristics ought to prove advantageous from a coding point of view. It is with this in mind that dynamic coding rate adjustment is introduced into the third coding scheme.

The third scheme will be constructed of the same elements as scheme 2, but rate adjustments will be possible. The rate adjustment mechanism involves the use of variable length shortened RS code-words, that may be switched between. The convolution codec may also be switched in or ignored. During operation, four discrete coding states will exist, namely two stand alone RS states with words consisting of either a single ATM cell or four ATM cells, and two concatenated states where the one and four cell RS words are additionally protected by a convolution codec.

4.3.1 Dynamic code rate selection.

For each of the four possible coding schemes that may be utilized by the dynamic codec, there is an error profile section where the scheme provides the best performance in terms of channel efficiency. The coding rate controller may be viewed as a state machine with four possible states. The four states correspond to the following code rates:

Table 4-1 : State Table for Dynamic Rate Codec

State	RS code	Convolution rate
0	(232,216,8)	1
1	(73,53,8)	1
2	(232,216,8)	1/2
3	(73,57,8)	1/2

State transitions would be initiated when a low pass accumulator crossed a certain threshold. The accumulator would store an estimate of the moment to moment word error rate for the currently operating RS code-word. The formula for the accumulator would be:

$$A_t = \sigma A_{t-1} + (1-\sigma)(ARQ_t)$$

σ is the filter weight and ARQ_t holds a 1 if an ARQ was requested at time t , and a 0 otherwise.

For the initial simulation a weight of 0.2 for σ was chosen. Impact of changing the sigma value is an issue that will be addressed in the simulation section.

The efficiency zones for each of the codes may be read off the following graphs that represent the channel efficiency for the various codes under a nominal bit error rate (BER). Once the desired transition BER's are known the RS-word error (and hence ARQ rate) may be calculated using the Equation 4-1 [13]:

$$P_{RS_WE} = 1 - P_{!RS_WE} = 1 - \sum_{i=0}^t \left(\binom{n}{i} \cdot P_{RS_SE}^i \cdot P_{!RS_SE}^{(n-i)} \right)$$

Equation 4-1

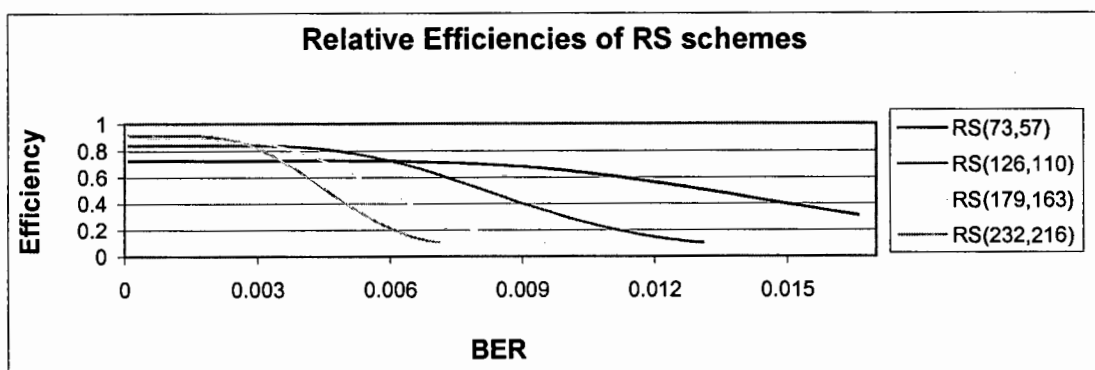
P_{RS_WE} is the observed word error rate for the RS decoder. P_{RS_SE} is the probability of an RS symbol error. The derivation of the formula results from a simple application of combinatorial mathematics.

Given the probability of an uncorrectable RS word error, one may deduce that the form of the equation for the end to end expected efficiency is as follows:

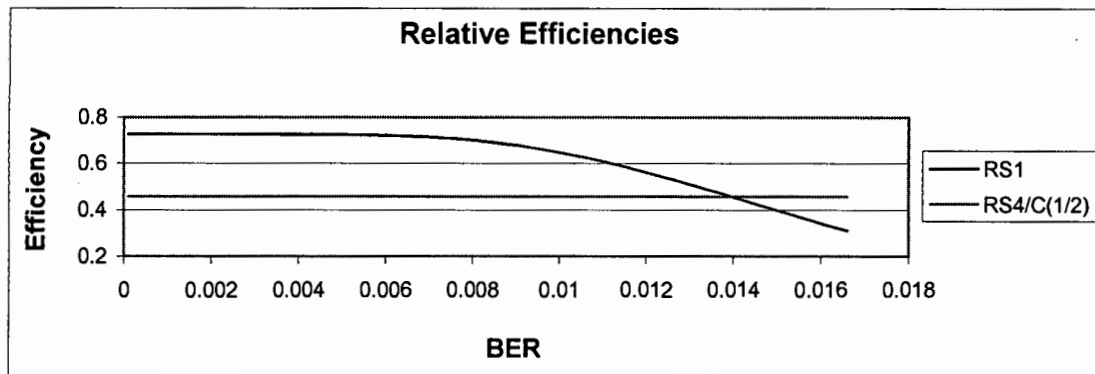
$$Eff = \frac{(Frame_Length)}{(Cell_Data_Length) \cdot \sum_{i=1}^{\infty} (i \cdot P(Frame_Error)^{i-1} \cdot (1 - P(Frame_Error)))}$$

Equation 4-2

The above equation computes efficiency as the length of information in a frame (including the ATM header) divided by the average amount of data sent in the frame transmission procedure. The formula is derived on the basis that the average amount of information sent is the sum of the lengths of the possible streams times the probability of the occurrence of a stream that length. The Cell_Data_Length is thus 1 frame length times the probability that there are no transmission errors in a single frame, plus 2 frame lengths times the probability that there is one errored frame followed by a correct frame, etc.



Graph 4-1 : Relative Efficiencies of RS Codes



Graph 4-2: Relative Efficiency of Concatenated and Short RS Only Codes

4.3.1.1 Transitions:

State 1-2 and 2-1 - On chart 1, the intersection between the (73,57,8) and (232,216,8) words occurs at a BER of 0.00355. This corresponds to a word error rate of 0.00021 (for the 73 symbol code - calculated using Equation 4-1) and 0.206 (for the 232 symbol code).

State 2-3 - The intersection on chart 2 occurs at a BER of 0.0139. This represents an RS word error rate of 0.3707.

State 3-2 - The actual cross over point would require the detection of the event of the BER crossing the 0.0139 threshold. This threshold represents an almost negligible probability of word error for the concatenated codec. An artificially high threshold must therefore be set for this transition - this will result in periodic incorrect movement back up to rate 2 for a steady state BER less than the threshold, requiring associated changes back down to state 2, but ensures that the transition does in fact happen.

State 3-4 and 4-3 - These states are analogous with states 1 and 2. The same word error thresholds will thus be used to dictate the state transitions.

When the held value of A_t crosses the calculate state thresholds, the mentioned state transition will be initiated.

5 Simulation Models: Assumptions, Limitations and Techniques

The evaluation process of the error control techniques suggested in this dissertation will involve extensive simulation. In order to simulate the error control schemes, the scope of the simulation platform in terms of operating assumptions, limitations and the models of the various aspects of operation must be described.

5.1 Assumptions

The following assumptions were made to allow the feasible implementation of a modeling platform:

- **ATM cells will be treated as blocks instead of streams.** That is, unless otherwise stated, no operation that is dependent on a previous operation will commence until such time as the previous operation has terminated. For a series of k bit oriented operations feeding one another, the total introduced latency for the stream will be $k \times (\text{mean bit processing time of the operations}) + \text{block transmission delay}$. The block transmission delay is time required to pass an entire cell at the simulation rate and indicates the time between the first bit and the last bit being received. In the model this will be emulated by introducing a single bit time for each operation in the stream and also a cell time latency for the last stream operation in the chain. It should thus be clear that a number of unbroken stream oriented segments are logically replaced by a single block operation from a timing perspective. This is a valid assumption if the start and end functions are block oriented (that is only whole ATM cells are delivered to the final output stage).
- **MAC strategy transparent to the system.** The operation of the MAC layer will not be considered by the simulation platform. It will be assumed that the application will be allocated as much bandwidth as is required up to the maximum channel capacity. The efficiency aspects of the schemes will be evaluated by the number of bits sent to transmit a fixed amount of information. The effect of multiple users competing for bandwidth will not be explored and is deemed beyond the scope of this project.
- **Perfect Control Channel.** The control channel used to negotiate MAC transactions and request information repeats for unrecoverable data is assumed to be perfect - that is it uses as much error control coding as is required to effectively remove their impact on the operation of the control channel.

5.2 Limitations

The following deviations from the real operation of the envisaged error control mechanisms will be introduced to aid the simulation procedure:

Convolution operations will be performed on independent blocks. The convolution encoder and Viterbi decoding procedure will be applied in the simulation environment on a frame by frame basis, flushing the internal buffer with zero's at the end of each frame to displace the last data bits. This may introduce a slightly optimistic impression of the operation of the convolution encoder as the bits that are used to flush the decoder will not be errored, favoring the correct decoding path for the last bits passed. With long frames this should not however greatly misrepresent the performance of the decoder.

Hard decision based Viterbi decoding. Although soft decision decoding offers some performance advantages, a hard decoding strategy was introduced to simplify the simulation procedure as the interactions between the wireless terminal and the error control elements would prove difficult to emulate and would not significantly add to the understanding gained of the error management strategy.

5.3 Channel Models

An accurate representation of the transmission channel properties is required if the performance properties of the error control architectures are to be accurately modeled. To this end two channel models were developed to emulate encountered operating environments as closely as possible. After examining possible means of emulating a wireless channel [11;13;19;21;29;36;37;40;42;45;49;52;58;59;63;65;70], the two principle channel models were chosen both for their implementation feasibility and for their comprehensiveness in emulating significant and commonly encountered channel characteristics.

A third trivial model where the BER was linearly swept was included for testing purposes.

5.3.1 Channel Model 1

The objective of channel model 1 is to emulate an indoor wireless ATM pico-cellular environment. The basis for the model that is used is described in [21].

The model in principle incorporates all the slow fading characteristics that a stationary indoor wireless terminal operating in the 20GHz range would experience since it is based on a measured indoor wireless channel. What is not considered is rapid fading and auto-correlated or burst errors due to multi-path effects and movement of the mobile.

Table 5-1 : Specifications for the Indoor Wireless System

Centre Frequency	19.37GHz
Modulation scheme	Offset QPSK
Bit Rate	70.208Mbit/s
3dB Bandwidth	35.1MHz
Transmitter Power	20dBm
MAC Protocol	TDD/TDMA

In the model that was generated to emulate the described environment, the moment to moment bit error rates were those derived from direct measurement from the wireless ATM test-bed documented in [21].

In the paper, the following route through the test office:

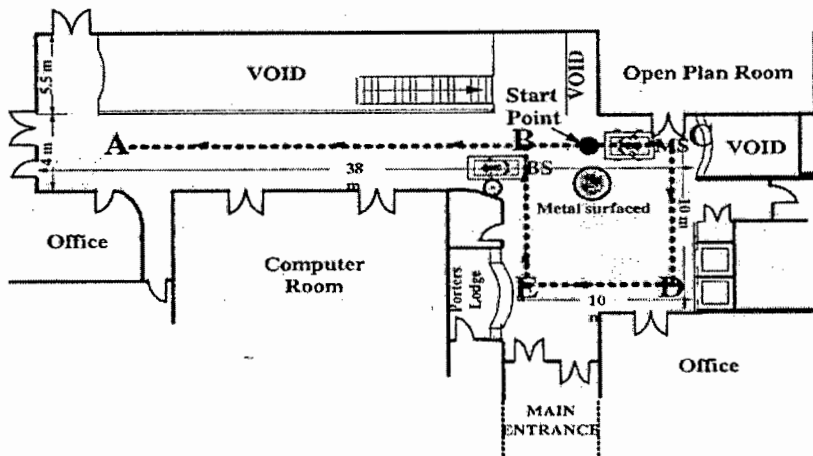
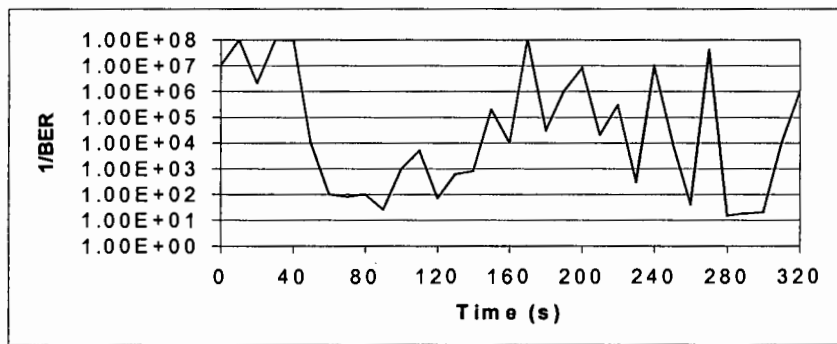


Figure 5-1 :Route Taken to Generate Error Rates Sample

Measurements of the moment to moment bit error rates were as follows:



Graph 5-1: Channel Bit Error rate

In the physical model, the bit errors were independently and randomly distributed with the moment to moment bit error rate being that represented in the graph above.

In principle this model will indicate the operating characteristics of a stationary or very slow moving wireless terminal in an indoor environment. The dominant characteristic will be the very high levels of attenuation experienced during some of the time intervals considered.

5.3.2 Channel Model 2

The objective of channel model 2 is to emulate an out-doors cellular environment. This model will show the applicability of the error control modules developed in the presence of auto-correlated/bursty fluctuations in SNR introduced through the motion of the mobile and Doppler shifting.

Table 5-2 : Summary of the Outdoor Simulated Environment.

Carrier frequency	1.8GHz
Modulation Scheme	OQPSK
Transmitted symbol rate	2×10^5 / second
Transmitter power	9W =39.5dBm
Transmitter antenna	Type: Omni-directional with 9dB gain. Elevation: 12m*
Receiver antenna gain	Type: Omni-directional with unitary gain. Elevation: 1.5m
Mobile velocity	16m/s (57.6km/h) away from receiver
Distance to base station	1km at commencement, 1.5km at termination.
Assumed background noise levels	1.25×10^{-21} W/Hz =-156dBm #
Transmission path loss model	Hato Urban Model (slightly modified).
Slow fading attenuation distribution	Type: Log-Normal μ : 0 [dB] σ : 7.4 [dB] from [13, page 163]
Doppler fading model	8 state Markov process

* Since the path-loss model is only valid for antennae heights of 30m or more, 30m will be used for the path-loss computation. This is not invalid since it is assumed that the SNR is set to effect a reasonable data error rate at the operating distance.

In a physical system, the transmitter power would be selected to yield on operable SNR. Working from this assumption, a noise power was chosen to give a realistic nominal BER at the receiver (since the receiver power for a known transmitter was given). This does not negatively impact on the validity of the model for testing of the error control mechanisms since the principle emphasis of the channel model is to validate the error control mechanisms ability to handle the introduced slow and fast fading. Large magnitude, slow fading falls within the domain of model 1.

The assumed channel model will be a Rayleigh fading model implemented in a highly built up urban area. It will be assumed that the only components of the transmitted signal that reach the mobile unit are non-direct. The modeling of the channel includes the effects of slow and fast fading. The moment to moment channel bit error rate will be ascertained by the computed

moment to moment signal to noise ratio at the mobile unit. Factors which affect this calculated signal to noise ratio will include systematic effects and random effects.

Systematic effects included in the simulation:

- Transmission path attenuation. This model will calculate the attenuation due to distance from the transmitter to the receiver, but this displacement will be held constant instead of increasing with time since the principle emphasis of this model is to highlight the effects of movement and multi-path fading on the perceived channel characteristics.
- Background noise. (White Gaussian Noise assumed to be of constant power).

Non-systematic effects:

- General Transmission Path Irregularities. Typically the received power of a channel experiences slow fading due to random variations in the nature of the transmission path. These variations are generally assumed to exhibit a log-normal pdf.
- Rayleigh Fading. In this environment, the received signal is constituted of a number of multipath components, each with independent phase and magnitude characteristics. For a mobile unit in an urban environment, it is not unreasonable to assume no direct line of sight component in the received power envelope. In this case the pdf of the received envelope is Rayleigh distributed. Time variations of the envelope are due to Doppler frequency shifts on the individual multipath components due to the relative movement of the mobile.

5.3.2.1 Simulation Technique

To model the operation of the channel, random bit errors will be introduced into the transmitted data stream. The base probability of the introduction of bit errors for any given bit will be inferred from the moment to moment channel signal to noise ratio and the coding scheme utilized (in this case OQPSK). It is therefore necessary to estimate the signal to noise ratio at any given location in an attempt to calculate the expected bit error rate for the location. The noise segment in the signal to noise ratio calculation will be the constant background noise assumed for the channel (consisting of inter-cell interference and other sources). The signal component will be the original transmitted power, reduced by the systematic and non-systematic attenuation factors.

5.3.2.2 Transmission path attenuation

An adaptation to the Hata model will be used to yield the average transmission loss for the channel with distance from the receiver. The original model is described in [13]. The original Hata model is limited for use up to 1500MHz, but the system specification for the proposed system is 1800MHz. The COST-231 working committee extension to the original Hata model will thus be used as it extends the modelling range to 2000MHz. This modified model is described in [10].

The formula for the COST-231 path-loss model in a metropolitan centre is defined as:

$$L_{Hu} = 46.3 + 33.9\log_{10}f - 13.82\log_{10}h_{BS} - a(h_{MS}) + (44.9 - 6.55\log_{10}h_{BS})\log_{10}d + 3[\text{dB}]$$

Where:

- f is the propagation frequency in MHz.
- h_{BS} is the elevation of the base station antenna in meters.
- h_{MS} is the elevation of the mobile station antenna in meters.
- d is the distance in km from the base station to the mobile station.
- $a(h_{MS})$ is a terrain dependant correction factor:

$$a(h_{MS}) = 3.2[\log_{10}(11.75h_{MS})]^2 - 4.97$$

The limitations for the model are specified as follows:

f : 1500-2000MHz

h_{BS} : 30-200m

h_{MS} : 1-10m

d : 1-20km

The value obtained will be incorporated as the mean of the log-normal function generated for the slow fading estimation.

5.3.2.3 The Rayleigh Fading Model

With this channel model, unlike the Ricean distribution, there is no assumed direct line of sight link between the transmitter and the receiver that carries a significantly higher signal

strength than that of the indirect waves received. The interfering effect of the multipath components results in a received signal envelope with a pdf that is Rayleigh distributed.

A finite-state Markov process is used to emulate the Rayleigh fading properties of the operating environment. This technique is illustrated in [70]. With this model, the state machine representing the transmission channel may move into any one of a number of states, with each state having an associated bit error probability. In essence, this is an extension of the trivial Gilbert-Elliot channel model. The Gilbert-Elliot model represents the most simplistic version of Markov implementations - the model has only two states, one representing a 0.5 error probability and the other representing a zero error probability. The Markov process used in the simulation may be represented as follows:

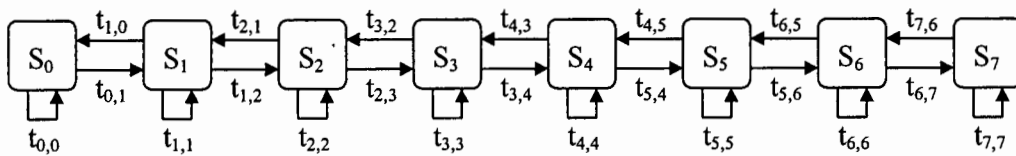


Figure 5-2 : State Transition Model of 8 State Markov Process for Rayleigh Fading Channel.

S_0 to S_7 are the *states*.

$t_{x,y}$ is the *state transition probability* from state x to state y .

Clearly:

$$\sum_{i=0}^7 t_{x,i} = 1$$

For this process: $t_{x,y} = 0 \forall x,y \in \{0,1,2,\dots,7\}$ if $|x-y| > 1$.

Define the *steady states probabilities* p_0, \dots, p_7 to be the probability of the model being in any given state at some arbitrary time without the knowledge of previous states.

Associated with each state is an attenuation a_0 to a_7 .

Let A be the *received signal to noise ratio* detected at the receiver. This represents the ratio of the received signal power to the received noise power and is proportional to the square of the amplitude of the received signal envelope.

The final received signal power $A = A' \cdot a_x$ where A' is the power received before attenuation due to the Rayleigh fading properties (i.e. due to other transmission losses and multipath effects) and a_x is the attenuation introduced into the model by the process occupying state x .

For the generation of the Markov model, assume that other channel factors are held constant. In this case we have a signal to noise ratio of A' before Rayleigh fading factors are compensated for.

Define:

$$\rho = E[A] = A'$$

Also define several signal to noise ratio thresholds A_0 to A_8 such that:

$$0 = A_0 < A_1 < A_2 < \dots < A_7 < A_8 = \infty$$

and

$$p(A \in [A_x, A_{x+1})) = p_x$$

When modeling the wireless channel, we will state that:

$$\text{State} = S_x \Rightarrow A \in [A_x, A_{x+1})$$

From this, for each state x , a nominal attenuation a_x will be defined, which when multiplied with the pre-Rayleigh fading SNR produces A .

In the generation of the model, firstly note that A is exponentially distributed:

$$p_A(a) = \frac{1}{\rho} e^{-\frac{a}{\rho}}$$

for $a \geq 0$.

The formula linking the steady state probabilities and the thresholds selected are as follows:

$$p_k = \int_{A_k}^{A_{k+1}} \frac{1}{\rho} e^{-\frac{a}{\rho}} da$$

$$p_k = e^{-\frac{A_k}{\rho}} - e^{-\frac{A_{k+1}}{\rho}}$$

For the model, the ratios of A_k/ρ will be chosen in such a way that:

$$p_0 = p_1 = \dots = p_7 = 1/8$$

Knowing that $A_0 = 0$ and $A_7 = \infty$, we are able to ascertain the other values of A_x/ρ or the net attenuation.

Table 5-3 : Calculated values of state attenuation thresholds.

x	$\exp(A_x/\rho)$	A_x/ρ
0	1.0000	0
1	0.8750	0.1335
2	0.7500	0.2877
3	0.6250	0.4700
4	0.5000	0.6931
5	0.3750	0.9808
6	0.2500	1.3863
7	0.1250	2.0794
8	0	∞

From the state attenuation thresholds, one is able to obtain the average attenuation by state – a_x .

$$a_x = \frac{\int_{A_x}^{A_{x+1}} \frac{1}{\rho} e^{-\frac{a}{\rho}} \left(\frac{a}{\rho} \right) da}{\int_{A_x}^{A_{x+1}} \frac{1}{\rho} e^{-\frac{a}{\rho}} da} = \int_{A_x}^{A_{x+1}} \frac{8}{\rho} e^{-\frac{a}{\rho}} \left(\frac{a}{\rho} \right) da$$

Solving yields:

$$a_x = 8 \left[e^{-\frac{a}{\rho}} \left(-\frac{a}{\rho} - 1 \right) \right]_{A_x}^{A_{x+1}}$$

Applying the following substitution to the above formula :

$$A_x = \rho.(A_x/\rho)$$

yields the following set of results:

Table 5-4: Calculated values of a_x , the per state attenuation factors.

x	a_x	a_k (dB)
0	0.0652	-11.8575
1	0.2087	-6.80478
2	0.3760	-4.24812
3	0.5773	-2.38598
4	0.8301	-0.8087
5	1.1700	0.681859
6	1.6930	2.28657
7	3.0795	4.884802

The final requirement for the model is the computation of the state transition factors, $t_{x,y}$. For a Rayleigh fading system, the movement rate (v) of the receiver with respect to the transmitter and the wavelength (λ) of the carrier yield the Doppler frequency (f_m):

$$f_m = \frac{v}{\lambda}$$

We also know that the expected number of times per second (N) the received SNR crosses a given threshold t per second is:

$$N = \sqrt{\frac{2\pi t}{\rho}} f_m e^{-\frac{t}{\rho}}$$

Let the number of symbols per second transmitted be R_t . On average, the number of symbols per second transmitted when the channel is in state S_i is:

$$R_t^{(k)} = R_t \times p_k$$

Let N_k be the average number of times per second that the channel crosses the threshold A_k :

$$N_k = \sqrt{\frac{2\pi A_k}{\rho}} f_m e^{-\frac{A_k}{\rho}}$$

Table 5-5 : Calculated Values of N_k for Markov Model

Velocity of Mobile	16m/s
Carrier Wavelength	0.1667m
f_m	96Hz
R_t	2×10^5
p_k	0.125
$R_t^{(k)}$	2.5×10^4
N_0	0
N_1	76.93492
N_2	96.80205
N_3	103.1078
N_4	100.1728
N_5	89.37074
N_6	70.83165
N_7	43.37687
N_8	0

From [70] the Markov transition probabilities are approximated by:

$$t_{k, k+1} \approx \frac{N_{k+1}}{R_t^{(k)}}, k \in 0, 1, 2, \dots, 6$$

and

$$t_{k, k-1} \approx \frac{N_k}{R_t^{(k)}}, k \in 1, 2, \dots, 7$$

and

$$t_{k,k} = 1 - t_{k,k+1} - t_{k,k-1}; k=1,2,\dots,6$$

$$t_{0,0} = 1 - t_{0,1}; t_{7,7} = 1 - t_{7,6}$$

Table 5-6 : State Transition Matrix for Markov Model

	0	1	2	3	4	5	6	7
0	0.9969	0.0031						
1	0.0031	0.9930	0.0039					
2		0.0039	0.9920	0.0041				
3			0.0041	0.9919	0.0040			
4				0.0040	0.9924	0.0036		
5					0.0036	0.9936	0.0028	
6						0.0028	0.9955	0.0017
7							0.0017	0.9983

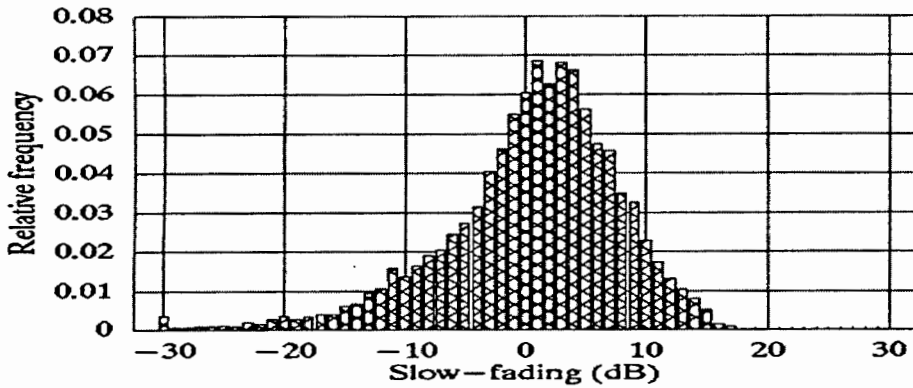
5.3.2.4 Slow fading

To generate a representation of the slow, non-systematic variability of the channel, the slow fading attenuation (in decibels) will be instances of a uniform distribution mapped to the log-normal distribution [13],[49],[52]. The reason for the acceptance of the lognormal distribution is that the resulting path attenuation for the channel is the arithmetic product of a number of independent factors. The pdf of the product of a number of independent factors is lognormally distributed. Since the attenuation is lognormally distributed, the attenuation expressed in decibels will be normally distributed.

Because the fading rate is slow, fewer realisations of the pdf will be generated and a quadratic interpolation technique will be applied to estimate the value of the attenuation between realisations of the pdf. It should be noted that the mean of this pdf would correspond to the average transmission path attenuation.

[13] documents experiments conducted in typical urban environments and give expected standard deviations in decibels for various base station antennae heights. Their model used a sampling rate of 1 sample every 6.44m. In the model generated here, this will be the observation instance generation interval and intermediate values will be interpolated using the quadratic fit technique.

The following graphic was taken from [13] and represents the measured slow fading distribution for various antennae heights. It is this distribution that will be used to generate the slow fading statistics used in this channel model.



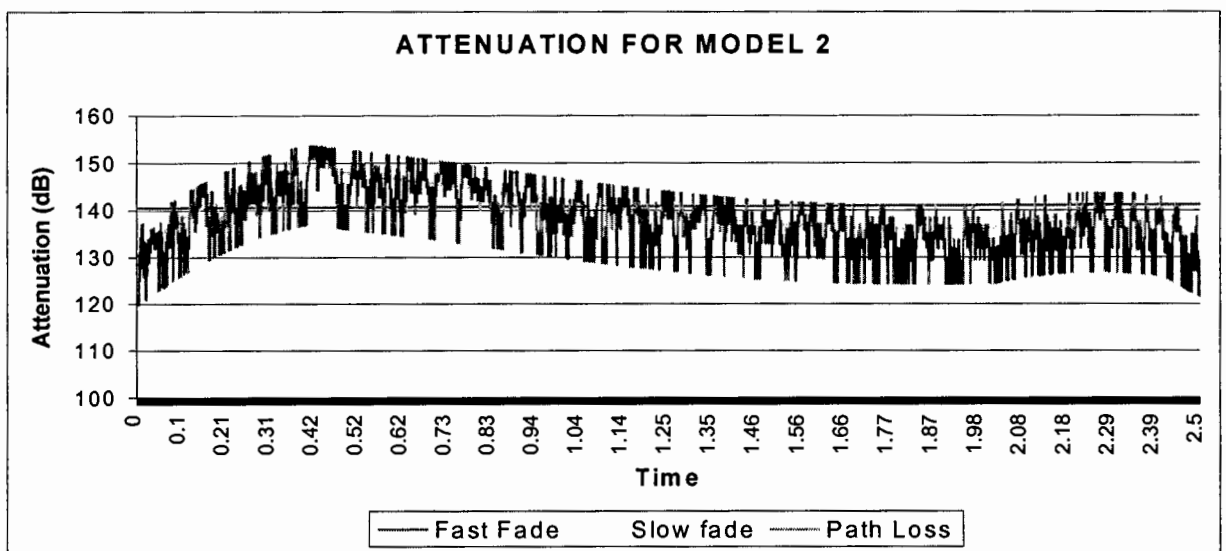
Graph 5-2 :Slow Fading Statistics for Various Antennae Elevations

5.3.2.5 Resultant BER Probability Calculation

Given the transmitted signal power in dBm, the attenuation factor for transmission over the channel (slow fading, fast fading and path loss), and the signal to noise ratio for the channel, one is able to ascertain the momentary signal to noise ratio for the channel for each bit transmitted. From this, the bit error probability for any bit transmitted may be ascertained as follows:

$$P_e = Q \left(\sqrt{\frac{E_s}{\eta}} \right) = Q \left(\sqrt{\frac{ST_s}{\eta}} \right)$$

A sample BER-time plot for the final model is given in Graph 5-3.



Graph 5-3 : Typical Fading Statistics for Model 2

5.4 Traffic Models

In order to simulate a wireless link, traffic models are necessary. Three types of traffic will be assumed: *variable bit rate* (VBR), *constant bit rate* (CBR) and *available bit rate* (ABR). Each traffic class has a different cell generation profile and different *quality of service* (QoS) constraints.

5.4.1 Modeling CBR Traffic

Of the possible traffic models, the CBR traffic model is the simplest. The inter-cell arrival times for the model will be held constant. For the simulation process the assumed CBR connection will be that of a voice link with a nominal data rate of 64kb/s. The inter-cell arrival time for the traffic source will thus be 6ms. It is assumed that the network delivering the data introduces no jitter.

5.4.2 Modeling VBR Traffic

To generate a realistic VBR traffic stream, a cell arrival time model based on an MPEG-1 encoded video stream ("The Wizard of Oz") is utilised. The model used is given in [47].

The MPEG video stream used for the model has the following characteristics:

- The frame rate is 30 frames per second.
- The frame cycle is 15 frames:
I - B - B - P - B - B - P - B - B - P - B - B - P - B - B
- The lognormal distribution is used to model the number of ATM cells required for the transmission of an entire frame. The pdf for the function is as follows:

$$p(z) = \frac{1}{z\sqrt{2\pi\sigma^2}} \exp\left[-\frac{(\ln(z)-\mu)^2}{2\sigma^2}\right] \quad \text{if } z>0$$

$$p(z) = 0 \quad \text{if } z \leq 0$$

- The *maximum likelihood estimator* (MLE) parameters for the models are as given below:

Table 5-7 : Maximum Likelihood Estimators for MPEG Model

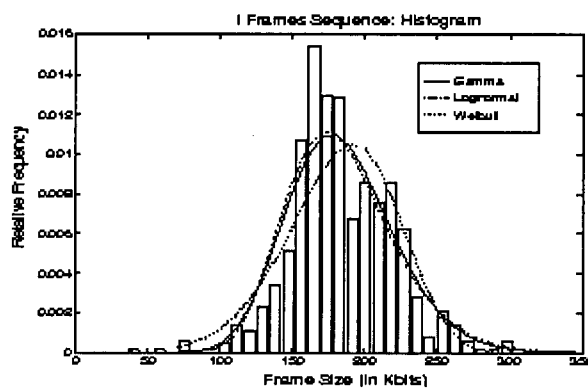
Frame Type	μ	σ
I	5.1968	0.2016
P	3.7380	0.5961
B	2.8687	0.2675

- It is assumed that the carrier network adds no latency in the delivery of the MPEG cells. Cell jitter before wireless transmission is purely a function of the nature of VBR - there is no in-frame jitter introduced. The inter-cell arrival time (ICAT) used in terms of the frame size (FS) and frame rate or number of frames per second (FR) is thus :

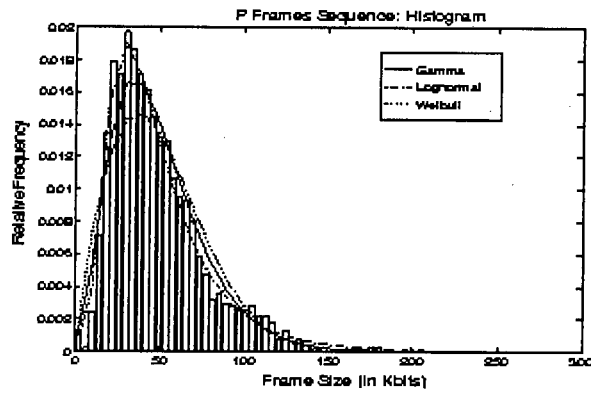
$$\text{ICAT} = 1/(\text{FS} \cdot \text{FR})$$

- There is no traffic shaping performed by the model.
- For low data rate links a modified version of the traffic source was introduced, with traffic density of $1/20^{\text{th}}$ of that for the MPEG video stream. This is not intended to emulate any specific service, but yields an impression of the operation of a VBR type traffic source in such an environment.

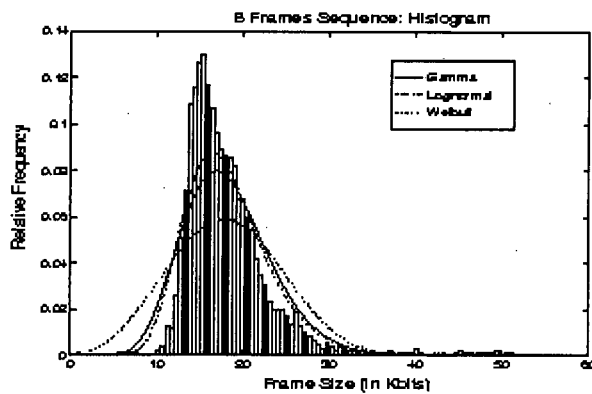
The following plots are taken from [47] and illustrate the frame size distribution in kilobits of the various frame types:



Graph 5-4 :Distribution Function for I-Type Frame Sizes



Graph 5-5 :Distribution Function for P-Type Frame Sizes



Graph 5-6 :Distribution Function for B-Type Frame Sizes

5.4.3 Modelling ABR Traffic

An explicit ABR traffic model will not be generated. Results pertaining to ABR traffic will be inferred from the results for the CBR and VBR traffic classes.

Motivation for not explicitly introducing an ABR traffic model is that the ABR congestion control measures will be assumed to operate correctly to the end terminal and sufficient buffer space will be present to handle any feed-back system lag. In this case, the performance of the scheme for an ABR traffic source will be entirely based on the throughput efficiency, and this will be adequately measured by the simulations performed using the CBR traffic class.

6 Simulation Platform

The section that follows is intended to document the simulation platform that was used in the evaluation of the error control mechanisms suggested for operation in the assumed wireless ATM operating environment.

6.1 Design Criteria

In order to evaluate the performance of the coding schemes that have been proposed, a comprehensive simulation platform was developed in C. The following were criterion for the platform under development:

- The platform should be modular and re-configurable in nature so that by re-ordering the components, any scheme could be represented.
- Each module should function as efficiently as possible due to the size of the samples that the simulator will process, and the computational complexity of the schemes used.
- Each module should be internally re-configurable in an effort to allow maximum system flexibility.
- The model should be event driven to emulate real time operation and enable transactions between modules. The operation of each module would be triggered by a scheduled event implicating the module being processed. During the module's operation, further events could be scheduled involving other modules.

6.2 Schematic Representation of the Developed Simulation Platform

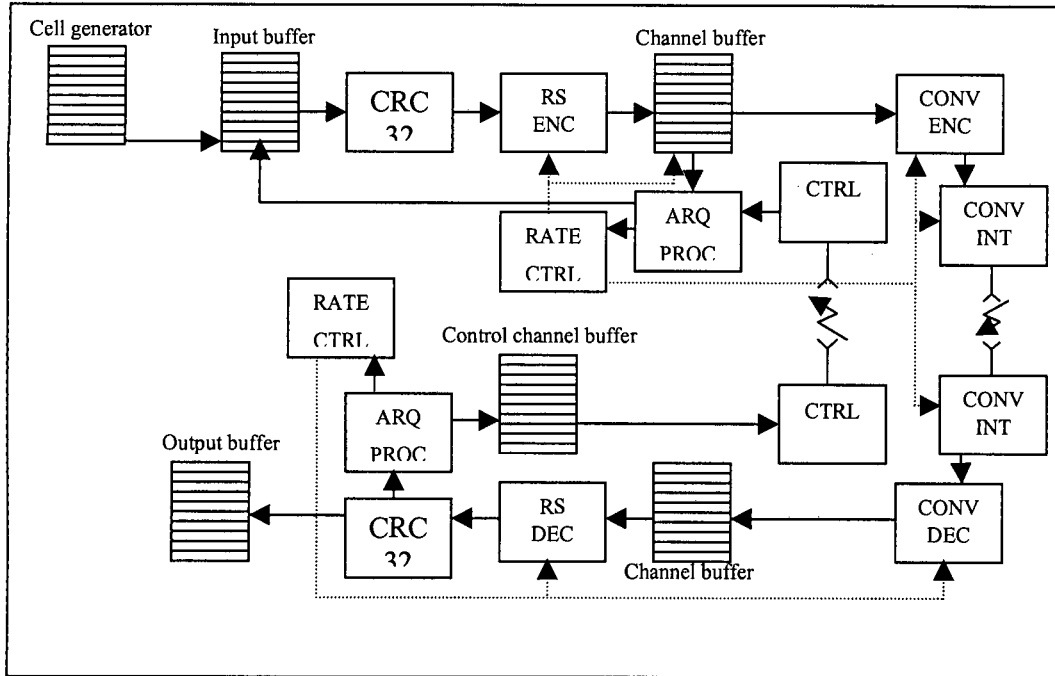


Figure 6-1: Schematic Representation of Wireless Architecture

6.3 Logical Modules of the Simulation Platform

The simulation platform may be broken down into a number of logical elements.

6.3.1 Event Processing Section

The event queue is used to store in chronological order the events that have been scheduled. These events are processed one at a time. Any module may add events to the queue of scheduled events. Once the module associated with a specific event has performed the required functions, control is returned to the event-processing element and the module associated with the next scheduled event is called.

Each functional module has an associated event processing element. This element is called and in turn calls the necessary functions attached to the module (for example, encode the using the RS algorithm and pass the encoded information to the next buffer stage). Each stage's event processing routine would also schedule events associated with the next processing element.

The first event is manually scheduled and corresponds to the arrival of the first ATM cell in the chain. Every subsequent event is introduced automatically by the event processing elements and the simulation block terminates when there are no more events to process.

On the termination of an event, the internal state register is checked to ascertain whether any other events should also be generated, the justification for this is that a full buffer may have inhibited the action of a previous module, and this condition may have changed with the most recently processed event. This feature ensures that the system never locks up if for some reason an event cannot be processed at any point.

6.3.2 Cell Generator

The cell generator is responsible for the generation of ATM cells to pass through the simulator. Each ATM cell is generated by producing random data to represent the contents of the cells and the cell headers. Inter-cell arrival time is a function of the traffic type being considered and the mean data rate of the channel. Cells are generated in blocks of either five hundred or five thousand and stored in a buffer array (Input Buffer) with associated arrival times generated from the known cell inter-arrival time distribution stored in a separate array. The cell data is generated by the C pseudo-random function, although simple zero only cells could have been used since no non-linear codes are used and the actual data transmitted should in no way affect the performance of the error control elements.

Specified in the design section is the addition of 1 byte of cell sequence number to replace the HEC field that is made redundant by the additional error control elements. This replacement is reversed (i.e. the HEC field is regenerated) before the ATM layer and it is intended to conserve bandwidth and preserve cell order. In the simulation platform, two bytes were introduced as the last two bytes of the cell to emulate this element. This deviation from the real operating method (that is, using two bytes of data instead of 1) was made to make the

statistics processing function simpler and should not significantly alter the performance of the model since the additional overhead does not enter into the efficiency calculations.

6.3.2.1 Inter-cell Arrival Times Distributions

Two basic inter-arrival time distributions were used, one for CBR traffic (64kb/s voice) and one for VBR traffic ($\pm 1.5\text{Mb/s}$ mpeg1 video stream). The actual arrival times used are described in section 5.4.2.

A modified VBR source was also generated for use in a low data rate channel with cell inter-arrival times of 20 times higher than a classic MPEG video stream.

6.3.3 Buffers

Two types of buffers are used in the model. The input and output buffers are standard arrays. The input buffer holds the data produced by the cell generator and has an associated array of projected cell arrival times. With the arrival of each cell, the arrival of the next cell is scheduled in the priority queue. Data parsed by the simulator is written into the output buffer in sequential order. Once the entire block of data has been passed through the simulated transmission channel (the input buffer pointer designates the end of the input block and all pending events have been processed), the input and output data blocks may be compared. This comparison involves checking cell by cell for bit errors and comparing the arrival times of the cell at both ends of the network. It is from this process that the simulation statistics of overall bit error rate, latency and jitter are derived.

The remaining buffers operate in a FIFO manner. Upper and lower pointers are used to designate the location of the cells in a continuous segment of memory. Non-single element buffers are necessary, as the operation speeds of various elements in the simulator are not all equal. Inevitably one element will represent the bottleneck for the operation of the system and under high traffic load it is the buffer that is used to supply this element with data that will overflow. Buffer over and under-flow conditions are ascertained by watching the pointers to the elements in memory. Over and underflow are indicated by the setting of an error flag that may be observed by control modules at any point. It is expected that underflow conditions should never occur since an event to a module is only ever generated when data is made available for that module.

6.3.4 CRC32

The CRC element appends a CRC check to frames passed through it. Because the CRC operation is very simple and fast, this element does not have a dedicated buffer. The time for the operation is added onto the time for the next stage.

The CRC decoder occurs after the last stage of FEC decoding and is used to supply information for the action of the automatic repeat request unit.

Please consult Appendix C for details of CRC generation.

6.3.5 RS ENC and DEC

The Reed-Solomon encoder and decoder elements were adapted from a segment of code written by Simon Adelaide. The encoding and decoding procedure are performed on data held in predefined variables. The only adjustment made to the original code was in the treatment of un-decodable errors. The original code passed the data unadjusted to the next stage in the process, but a minor adjustment was made enabling the detection of uncorrectable errors and making this information known to the ARQ PROCESSOR. A description of the RS encoding and decoding process is included as Appendix A.

6.3.5.1 Encoder and Decoder Implementation

The Reed-Solomon encoder and decoder elements, depending on the specific nature of the implementation introduce system latency and jitter. In terms of the decoder, it is fairly clear that a finite amount of latency will be introduced into the system - the block decoding process must take a finite amount of time. The physical amount of time to perform the decoding function is also dependant on the specific nature of the code word being processed. (From the description in Appendix A it is clear that the process of decoding in the presence of data errors is more computationally intensive than the same process where errors are not present and thus takes more time). In order to support the maximum data rate specified in the system specifications for the coding scheme, it is assumed that a VLSI implementation would be installed. In this case the expected time characteristics are as follows:

Encoder processing time: 6.45 μ s

Decoder processing time: 8.65 μ s

(See [24]).

It should be noted that the impact of decoder variance is not directly considered (this may in a real system introduce an aspect of system jitter, but the net cell delivery time difference will clearly not exceed 8.65 μ s).

6.3.6 Convolution Code Encoder

Full description of the operation of a convolution encoder is included in Appendix B.

The convolution encoder segment consists of the convolution encode event processor and the physical convolution encoder. Like the other event processors, the convolution event processor schedules the next event in the transmission chain when the decoder is complete.

The physical convolution encoder operates by shifting each bit to be sent into a shift register of length the (constraint length of the code + 1). By logically xoring the elements of the shift register indicated by the generator polynomial with one another, the encoded data sequence is generated.

The convolution encoder is a bit oriented or stream based process instead of a block process - that is the code is passed sequentially through the encoder and may be transmitted by the channel immediately after the code is generated. As stated in the design assumptions, the latency introduced by this element will be the time required to pass a single bit. The cell transmission delay in moving back to a block structure will be introduced at the end of the stream chain. It is for this reason that the code delay introduced by this element is constant and small - equal to the time required to logically XOR the contents of the shift register with one another.

The block size of the output of the code is dependent on the coding rate. For the rate 1/2 code, the block passed to the next element is clearly twice the size of the previous block.

6.3.6.1 Encoder Implementation

A VLSI implementation using 2micron technology was assumed. For a constraint length 8, rate 1/2, a pessimistic estimate for the bit-wise latency is 35ns based on a per gate estimate. This assumes a 3 stage XOR architecture, shift register and 2 stage output MUX.

It should be noted that the given 35ns delay is insignificant with respect to the general simulation. It will be far overshadowed by the latency introduced in moving back to a block methodology. Even if the actual introduced latency was an order of magnitude higher, it would still play no significant role. It is for this reason that it was not computed precisely.

6.3.7 Convolution Code Decoder

The convolution code decoding process uses the Viterbi decoding algorithm described in Appendix B.

The module consists of the convolution decode event processing element and the physical Viterbi decoder.

The decoder that was written for the simulation platform is generic and is able to operate for any code rate and constraint length. The functionality required for the operation of the decoder with shortened codes was however not included. In order to decode the data, a state transition matrix or decoding butterfly is first generated using the given code polynomials. With this matrix, the lowest hamming distance path through the memory could be calculated. The memory depth used should generally be greater or equal to 4 times the code constraint length [7]. In this case the constraint length for the code was 8 and the memory depth chosen was thus 42.

The internal mode of operation of the simulation platform was one of parsing frame by frame when the end of frame time event occurred. It was for this reason that the convolution codec was used in a block operating mode. That is, for each block the initial memory state would be empty and at the end of the block zero's would be stuffed to push out the data in the memory through the normal action of the codec. This form of operation may yield slightly optimistic performance indications since one is guaranteed not to be operating on a false path when the last segment of data is parsed. To avoid this, the bits stuffed into the decoder to move out the last of the data could be errored at the same rate as the surrounding data (since the decoder is

linear in operation, this causes no inconsistencies). With large frames, this effect should however be negligible.

The assumed introduced latency for the decoder is 3 bit times at 1.5 Mb/s or $2\mu\text{s}$. [39] provides material for an exact estimate of the latency, but because the maximum latency due to the decoder is overshadowed by at least two orders of magnitude by the transmission delay for an entire cell and the RS decoder works on a frame by frame basis, there is no reason to attempt a precise estimate of this latency. The $2\mu\text{s}$ was included for the sake of completeness, and is not intended to significantly contribute to the end results.

6.3.8 Convolution Interleaver

The convolution interleaver was included with the convolution codec to provide as high a level of robustness against random errors as possible. The memory block size chosen for the convolution interleaver was 16×16 bits. This size was selected since with a memory depth of 32 at most two bits of a short burst error would appear in a single memory trace-back operation, yet the induced latency would not be intolerable.

The action of the convolution interleaver is described in Appendix D.

6.3.9 Rate Control

For coding schemes that utilize the dynamic rate option, ARQ system events were used to derive an estimate of the moment to moment bit error rates and this information would be used to ascertain rate transitions. The rate control algorithm is described in Chapter 4.3.1. An accumulator would be used to track the perceived bit error rate by monitoring the cell retransmit requests from the ARQ processor. If a transition threshold is crossed, a code rate change is signalled to the coding elements.

Code rate synchronization is maintained in the model by the fact that the control channel is perfect and no retransmit requests are lost. In this way the transmitter and receiver would be able to maintain synchronized accumulators and by monitoring the ARQ's in transmit effect the code rate changes. In reality, the use of explicit code rate changes via the control channel is likely to be the most effective means of implementation.

6.3.10 ARQ Processor

The ARQ processing element is triggered on the reception of an ARQ event (this event would be generated if the CRC check failed at some point).

The model assumes that the perfect control channel is utilized to transmit the ARQ request and no compensation is made for the potential loss of an ARQ transmission. The event that represents the ARQ reception has a delay time of the classic time to transmit 100 bytes of data over the channel. This number was arbitrarily chosen and a comprehensive study of the MAC algorithm would be required to yield an accurate figure.

On reception of an ARQ, the data transmitting module makes use of a “virtual timestamp”. Instead of using the sequence numbers to ascertain the repeat request information, the model simply tracks how many cells have been sent since the beginning of the transmission of the ARQ request and by considering decoder data rates and channel transmission times, ascertains to which frame the ARQ is pertaining. This frame is then extracted from the channel buffer and the data contents written to the bottom of the input buffer. In this manner the data is retransmitted. The virtual time-stamp method may be augmented or totally replaced in real systems by the use of the sequence numbers associated with each cell (replacing the HEC field), but the simplicity of the method is ideal for the simulation implementation.

The ARQ transmission event information is also used in the rate control algorithm.

6.3.11 Re-sequencing Module

Because the ARQ system introduces problems with cell ordering and the ATM protocol guarantees sequential cell delivery, a re-sequencing element is necessary. In the simulation platform, an explicit re-sequencing module is not included, instead cell output times are simply adjusted such that no cell leaves the logical cell re-sequencing buffer until such time as all its predecessors have done so. This emulates the operation of a cell re-sequencing buffer, without the introduction of additional simulation complexity.

6.3.12 Statistics Generation and Output Module

To evaluate the performance of the schemes designed, a statistics collection and output module was a necessary addition. This module compared the input and output data on the completion of each simulation set (of 500 or 5000 cells) to yield timing, efficiency and error rate statistics, along with internal flag statuses to indicate error conditions such as buffer over and under-runs.

The output of this module included the following:

- Number of block.
- Time of block termination.
- Data sent to date.
- Bits transmitted to date.
- Bit errors introduced.
- ARQ requests sent and received.
- Maximum buffer sizes.
- Average, maximum and minimum cell delays.
- Variance of Cell Delays

7 Theoretical Confirmation of Performance of Codecs.

In order to confirm the validity of the test results obtained through the use of the simulation platform, two tests will be performed to confirm the action of the two principle coding elements, the Reed-Solomon codec and the convolution codec with the Viterbi decoder. These tests will match the measured performance of the coding schemes with their expected theoretical performance.

7.1 Test 1: Testing the Viterbi decoder.

7.1.1 Objective

The objective of this simulation was to test the action of the Viterbi decoder in an AGW channel and reconcile the results obtained against those described in reference material [7].

7.1.2 Methodology

In order to test the action of the coder and decoder, written in C, several sets of data were encoded and subsequently decoded by the decoder.

Table 7-1 : Constraint Lengths, Memory Depths and Coding Polynomials (in decimal) of Test Codes

K	τ	P_1	P_2
3	16	7	5
4	16	15	13
5	32	29	19
6	32	61	43
7	32	121	91
8	32	249	167

For each of the codes, 1000 samples of 5000 bits were generated and sent for each possible signal level. These samples were then encoded using the convolution schemes mentioned above. The transmission process was simulated through the introduction of random bit errors (corresponding to the action of a AWGN channel) to the encoded stream.

The bit error rates used in the test are listed in the table below.

Table 7-2 : BER's Used in Test

125
100
75
50
40
30
25
20
15
10

In the simulation a total of 4×10^8 bits were therefore encoded, modified and transmitted.

The simulator returned the total number of decoded bit errors in the decoded data set. The effective SNR was calculated for a AWGN channel using OQPSK.

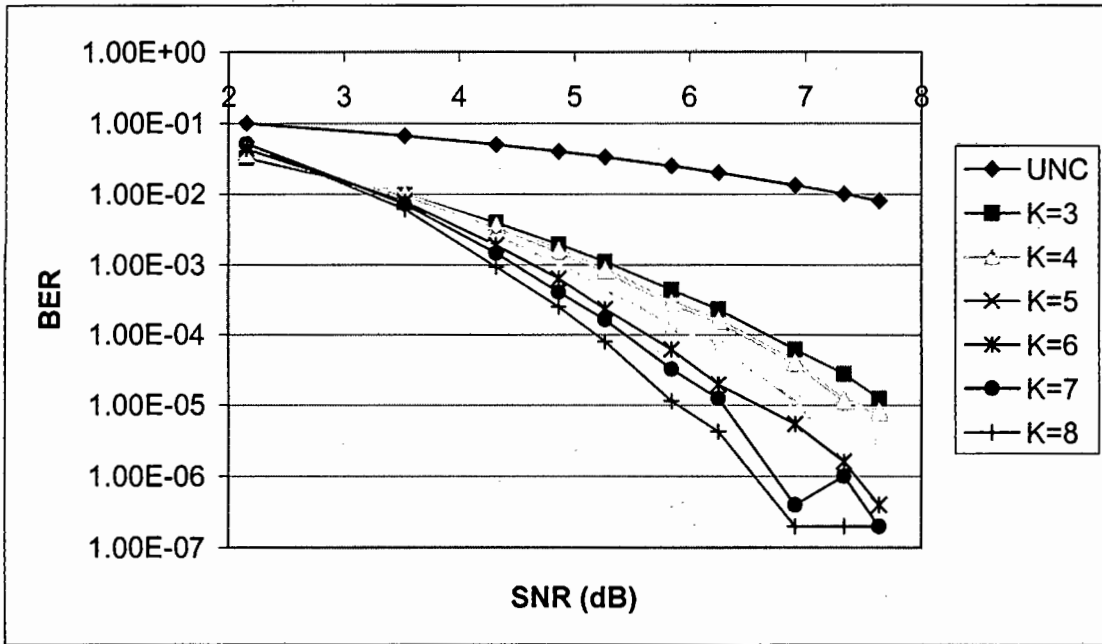
7.1.3 Results

The number of bit errors after decoding for each of the coding schemes and each of the bit error rates is included in Table 7-3.

Table 7-3 : Post Decoding Bit Errors for Convolution Test

BER:	K=3	K=4	K=5	K=6	K=7	K=8
125	62	40	15	2	0	0
100	138	58	9	8	5	0
75	306	202	57	27	2	0
50	1145	795	338	98	62	21
40	2170	1419	679	309	161	57
30	5466	4109	2323	1167	815	399
25	9766	7843	5027	3164	2024	1249
20	19586	17781	12968	9474	7204	4616
15	49041	49296	44340	39354	36560	30796
10	161677	185231	208174	217376	257962	258438

This may be graphed as follows:

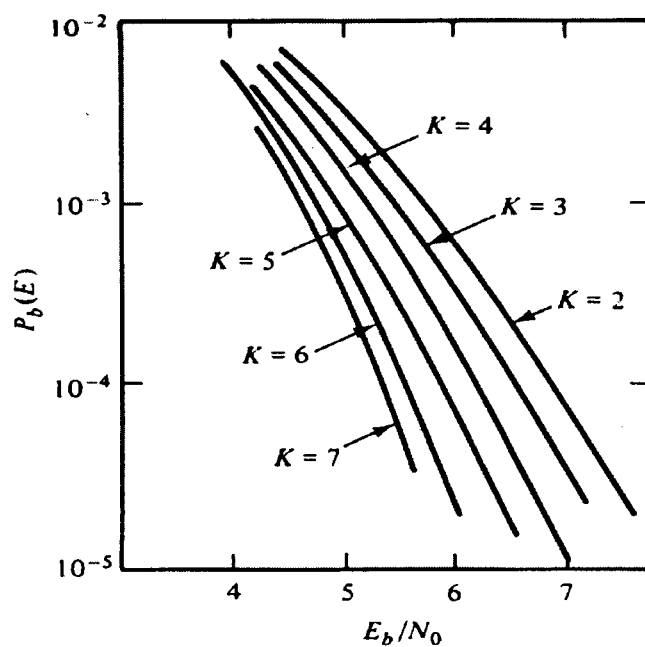


Graph 7-1 : Results of Viterbi Decoder Test

The series labeled UNC above represents the un-encoded case.

7.1.4 Observations

[7] documents a study by Heller and Jacobs where extensive computer based simulations were performed for a convolution encoder operating with a Viterbi decoder. The results of this study are summarized in the following graph:



Graph 7-2 : Theoretical BER for OQPSK Channel with Viterbi Decoding

7.1.5 Conclusions

The expected BER's match very closely those observed. From the simulations performed, one may conclude that the convolution coder and the Viterbi decoder are operating as expected.

7.2 Test 2: Theoretical Confirmation of the Performance of the Reed-Solomon Codec

7.2.1 Objective

The objective of this study is to reconcile the performance of the Reed-Solomon Codec used in the test against the theoretical performance of the codec, thereby confirming the fact that the codec operates correctly. To achieve this end, the theoretical performance of the error control mechanism utilizing only the Reed-Solomon codec will be calculated (namely the scheme with the stand alone 1 cell from RS code as the only FEC module). Tests of the scheme using the simulation platform will then be conducted to yield the performance of the scheme under a controlled bit error rate environment.

7.2.2 Theoretical Performance of Scheme 1 (RS Only)

Scheme 1 suggests the use of a RS (73,57,8) code as the principle error control element.

The empirical evaluation of this scheme is based on the following operating procedure:

- ATM cells are transmitted as they arrive at the terminal.
- To each cell is appended a 16 byte RS coding overhead.
- To each frame is appended a 4 byte CRC check.
- The frame is transmitted over a wireless channel and random bit errors generated at the nominal bit error rate are appended.
- The nominal bit error rate does not change inside a single frame.
- If the CRC check fails, a retransmit signal is generated.
- The cell is resent until such time as it is received correctly.
- Efficiency is defined as the ratio of sent information (in bits) to data length transmitted (in bits).

To calculate the efficiency of the scheme Equation 7-2, is applied to obtain for a given bit error rate the probability of a word error. From the word error rate, the efficiency of the scheme may be inferred from the following relationship:

$$Eff = \frac{(Frame_Length)}{(Cell_Data_Length) \cdot \sum_{i=1}^{\infty} (i \cdot P(Frame_Error)^{i-1} \cdot (1 - P(Frame_Error)))}$$

Equation 7-1

Where the probability of an errored frame is equal to:

$$P(Frame_Error) = 1 - \sum_{i=0}^8 \binom{n}{i} (1 - (1 - p)^8)^i (1 - (1 - (1 - p)^8))^{n-i}$$

Equation 7-2

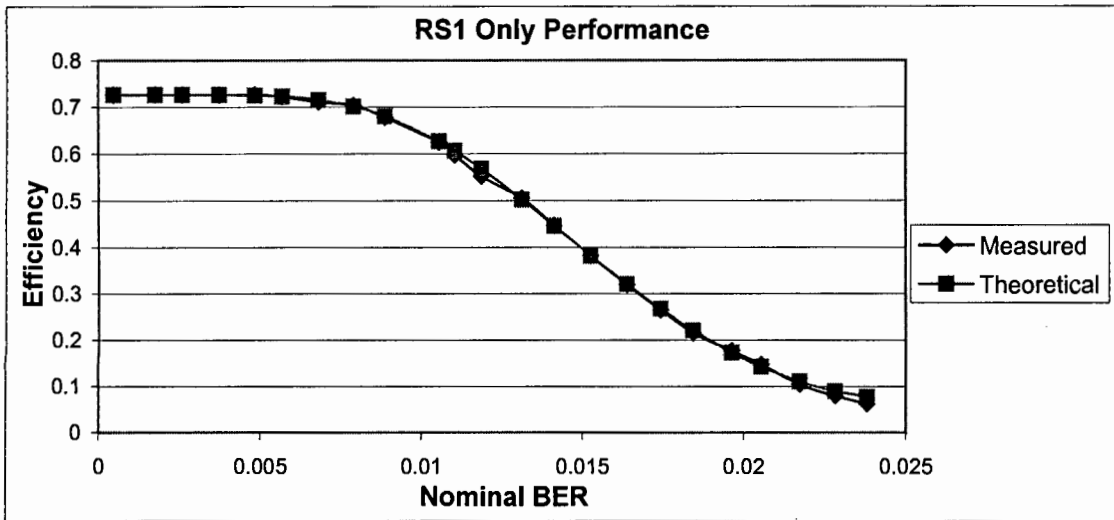
Using the above formulae, theoretical performance results for the scheme were calculated and compared to the simulated results (the results were computed using a spreadsheet and are presented with the simulation results in the section that follows).

7.2.3 Methodology

To test the performance of the scheme, the simulation platform was used to process the simulated transmission of 100 seconds of data over a channel with the bit error rate swept linearly from 0 to 0.023. The traffic source chosen for the simulation was a 64kb/s CBR traffic generator. From the resulting transmission bit and data bit counts, the operating efficiency of the scheme may be calculated and will be reconciled against the theoretical results for efficiency using the BER's indicated in the simulation platforms output segment.

7.2.4 Results

The results of the simulation and theoretical calculations are presented in the graph that follows.



Graph 7-3: RS(73,57,8) Only Performance - Measured and Theoretical

7.2.5 Observations

The performance of the platform very closely models the predicted performance in terms of end to end efficiency.

7.2.6 Conclusion

The Reed-Solomon codec is operating as expected. It may also be inferred that the other modules of the simulation platform involved in the processing of the RS only module operate correctly. These include the CRC and ARQ segment, the cell re-sequencing module, buffers and the statistic generation elements. The only two modules not verified by the test are the dynamic rate control module and the convolution codec.

8 Simulations Performed

A series of simulation runs were performed to gain an indication of the operating characteristics of the error control mechanisms in terms of their impact on the QoS parameters of the supported traffic classes.

The simulation runs were categorized into sets. Each set of simulations explored one specific facet of the operation of the schemes. The sets of tests were then further categorized into groups. The first group consisted of initial exploratory simulation sets to gain an impression of the general operating characteristics of the schemes. The second group consisted of a series of more focused sets aimed at ascertaining more clearly the impact of a specific operating parameter on the operation of the error control mechanisms.

8.1 Simulation Set 1 - Indoor CBR Preliminary Study

8.1.1 Objective

The objective of this set of simulations is to evaluate the performance of the three suggested error control schemes operating in the indoor pico-cellular wireless environment. The traffic class used for this set of simulations is the 64kb/s voice CBR model.

The performance criteria that will be investigated and measured are end to end channel efficiency for each of the schemes, introduced latency for the schemes and latency variation or jitter.

Although the traffic source is a low data rate CBR source, performance results for ABR traffic may also be inferred from the results. Because the ABR traffic class has end to end flow control and is relatively latency and jitter insensitive, the principle evaluation factor is throughput efficiency. The CBR model is able to measure this accurately and the results may thus be directly applied to the ABR traffic source.

It should also be noted that although the specified data rate is far below the channel capacity, a good indication of performance is likely to be presented. The reason for this is that it is assumed that for any realizable data rate, it is the responsibility of the MAC protocol to allocate sufficient bandwidth for the transmission. Since the MAC strategy is not simulated, we assume that the MAC mechanism will allocate as much bandwidth as is required, up to the total channel capacity. Knowing the likely requirements for a data source, it will then be the responsibility of the MAC to ensure that sufficient bandwidth is available when a connection is initiated, or the connection should be refused.

8.1.2 Methodology

Traffic source	64kb/s CBR source with intercell arrival times of 0.006s
Channel Model	Measured indoor pico-cellular model with a non-correlated error sequence [21].
Channel bit rate	70Mb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

The following table documents the details of each of the 3 trials performed:

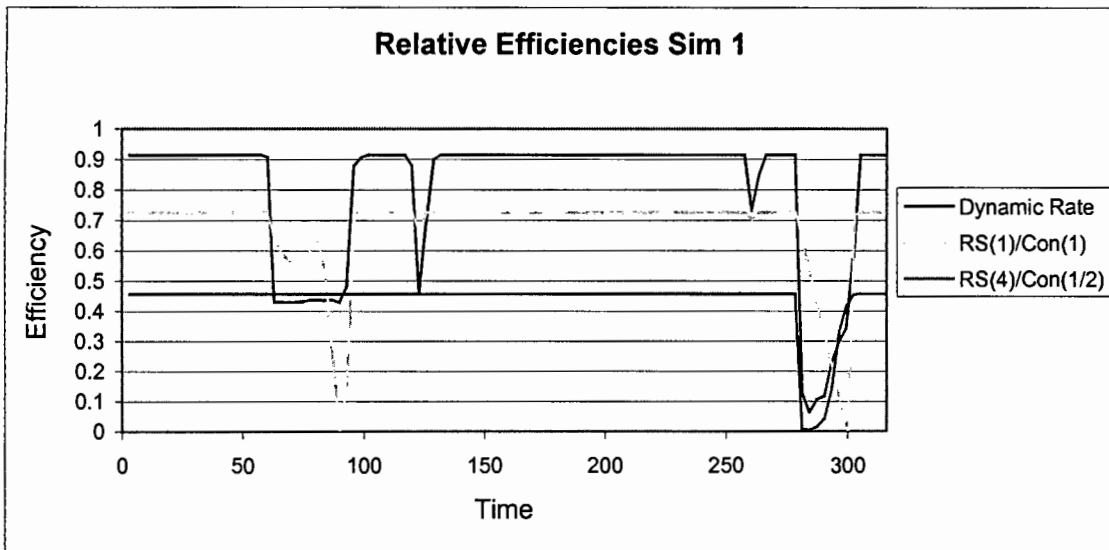
Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	4 cells/1 cell	½ / off	0.1	T1outa.txt
Trial 2	1 cell	off	0	T2outa.txt
Trial 3	4 cells	½	0	T3outa.txt

8.1.3 Results

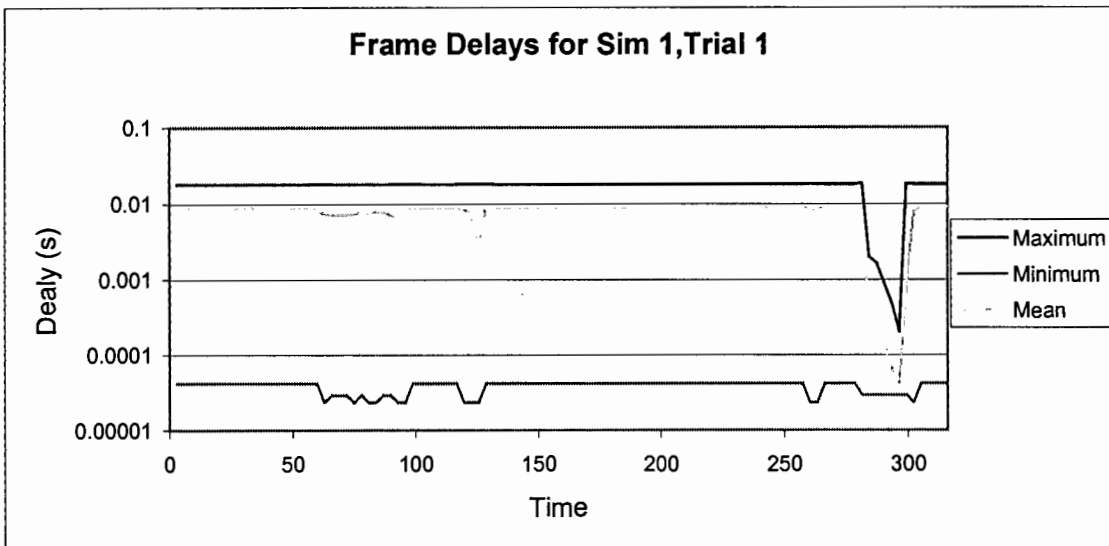
Table 8-1 : Simulation 1 Numerical Results

Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	22472000	37496120	0.599315	0.008213	0.018291	2.34E-05
2	20988000	1.43E+09	0.014696	0.107542	20.002	2.34E-05
3	22472000	1.50E+08	0.150261	0.009202	0.056394	4.72E-05

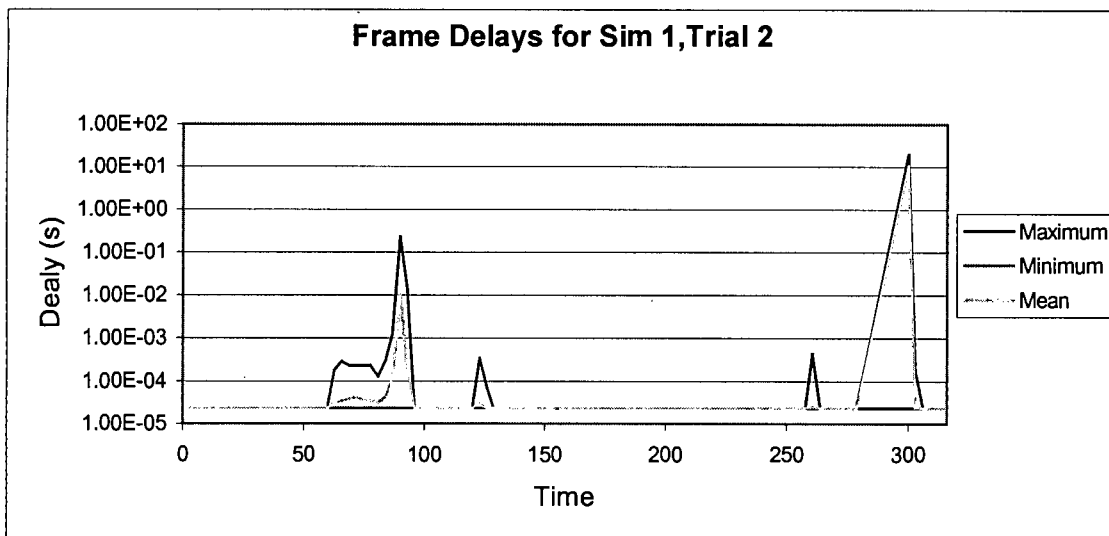
The results of the simulations may be graphically represented as follows:



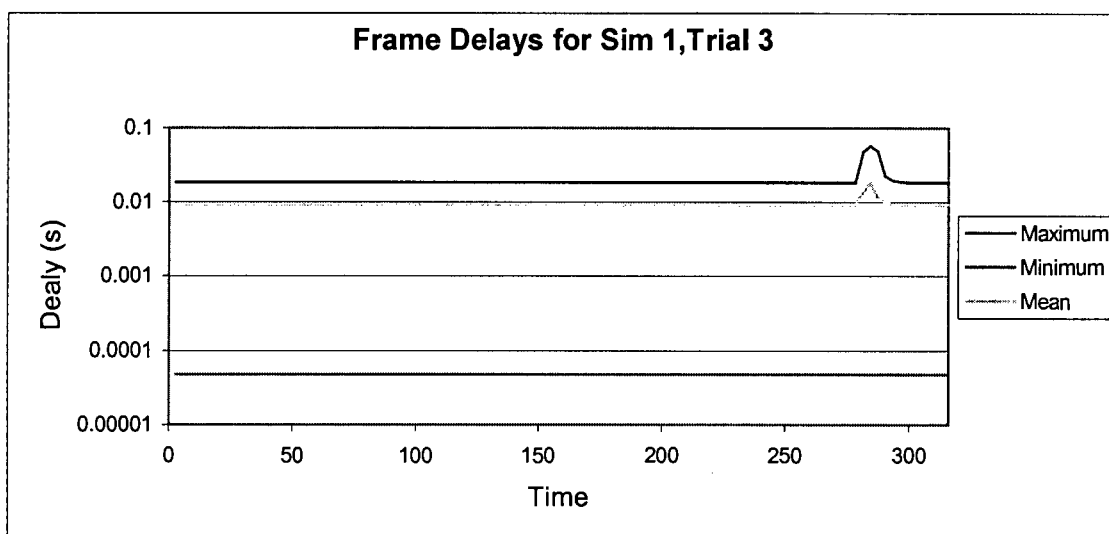
Graph 8-1: Relative Efficiencies of the Schemes Over Time for a CBR Source in an Indoor Channel



Graph 8-2: Cell Delays Plotted For Each Simulation Frame For Scheme 3 (Dynamic Code Rate)



**Graph 8-3: Cell Delays Plotted For Each Simulation Frame For Scheme 2
(RS(1)Conv(1))**



**Graph 8-4: Cell Delays Plotted For Each Simulation Frame For Scheme 1
(RS(4)Conv(1/2))**

8.2 Simulation Set 2 - Indoor VBR Preliminary Study

8.2.1 Objective

The objective of the this set is to gauge the performance of the schemes proposed (1,2 and 3) in an indoor wireless environment with a high data rate ($\pm 1.5\text{mb/s}$) VBR traffic source.

Performance criteria for the test are throughput (i.e. end to end efficiency), cell delay and jitter statistics.

8.2.2 Methodology

Traffic source	MPEG 1 video stream with lognormal frame sizes.
Channel Model	Measured indoor pico-cellular model with a non-correlated error sequence [21].
Channel bit rate	70Mb/s
Simulation Time	> 315s
Simulation Frame Size	5000 ATM cells

The following table documents the details of each of the 3 trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	4 cells/1 cell	$\frac{1}{2}$ / off	0.1	T4outa.txt
Trial 2	1 cell	off	0	T5outa.txt
Trial 3	4 cells	$\frac{1}{2}$	0	T6outa.txt

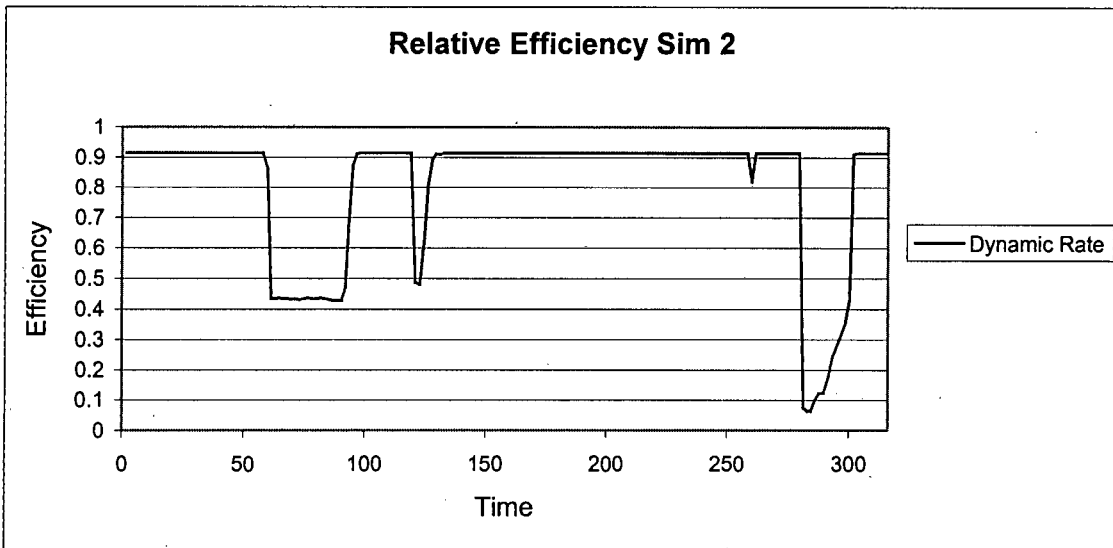
8.2.3 Results

The results from set 1 clearly indicated the inadequacies of the first two error control mechanisms in this channel type. There was little insight to be gained from running Scheme 1

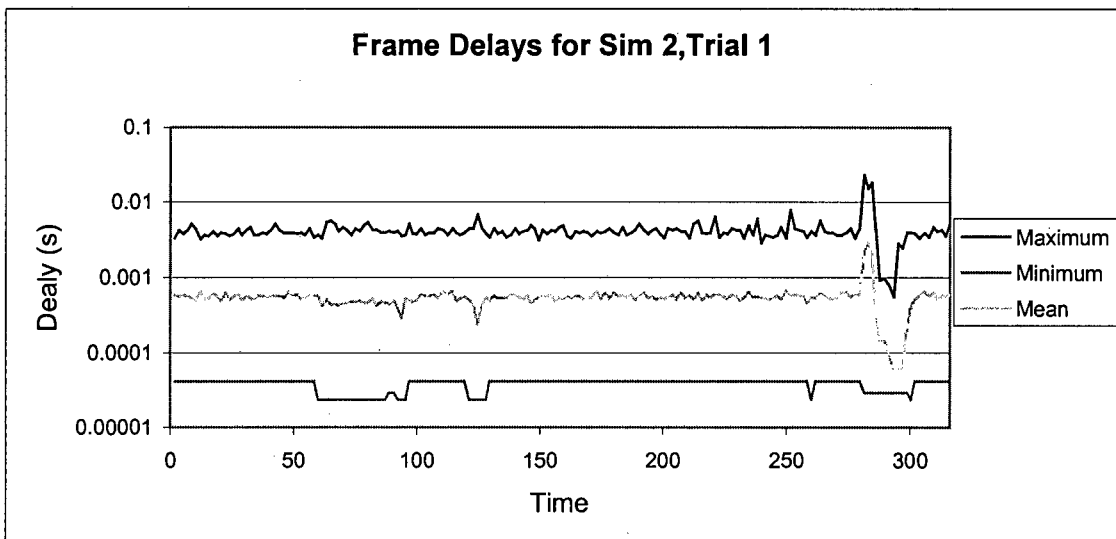
and Scheme 2 to completion and the execution time would have proved prohibitive due to the massive number of ARQ's transmitted.

Table 8-2 : Simulation Set 2 Numerical Results

Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	392200000	654235456	0.5994784	0.0005504	0.0228097	2.34E-05



Graph 8-5 : Relative Efficiency of the Dynamic Rate Scheme Over Time for a CBR Source in an Indoor Channel



Graph 8-6 : Cell Delays Plotted For Each Simulation Frame For Scheme 3 (Dynamic Code Rate)

8.3 Simulation Set 3 - Outdoor CBR Preliminary Study

8.3.1 Objective

The objective of this set of simulations is the general evaluation of the performance of the suggested error control architectures in an outdoors environment with relatively low data rates and auto-correlated error sequences (i.e. errors with a burst nature), with a constant rate CBR traffic source emulating voice with a bit rate of 64kb/s.

As with simulation sets 1 and 2, criteria for scheme performance are channel efficiency after coding, introduced latency and jitter.

8.3.2 Methodology

Traffic source	64kb/s CBR source with intercell arrival times of 0.006s
Channel Model	Simulated outdoor cellular environment with Rayleigh fading.
Channel bit rate	400kb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

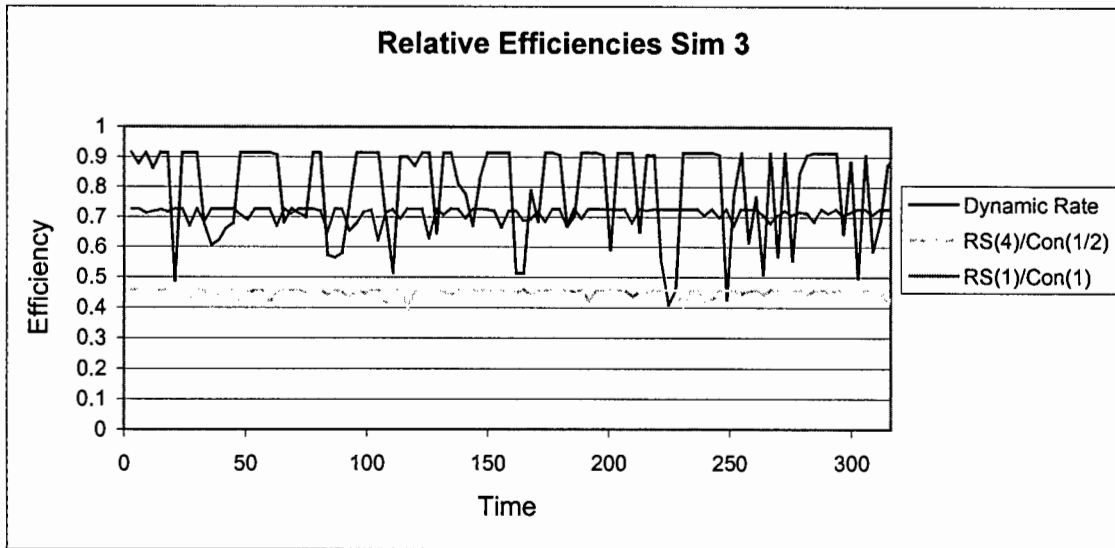
The following table documents the parameter settings of each of the 3 trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	4 cells/1 cell	½ / off	0.1	T7outa.txt
Trial 2	4 cells	½	0	T8outa.txt
Trial 3	1 cell	off	0	T9outa.txt

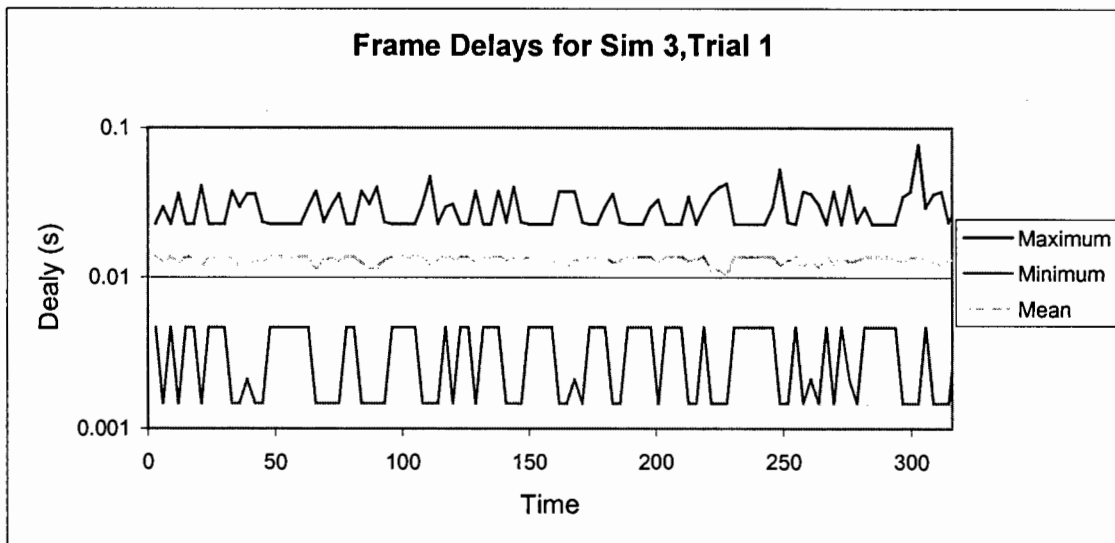
8.3.3 Results

Table 8-3 : Simulation Set 3 Numerical Results

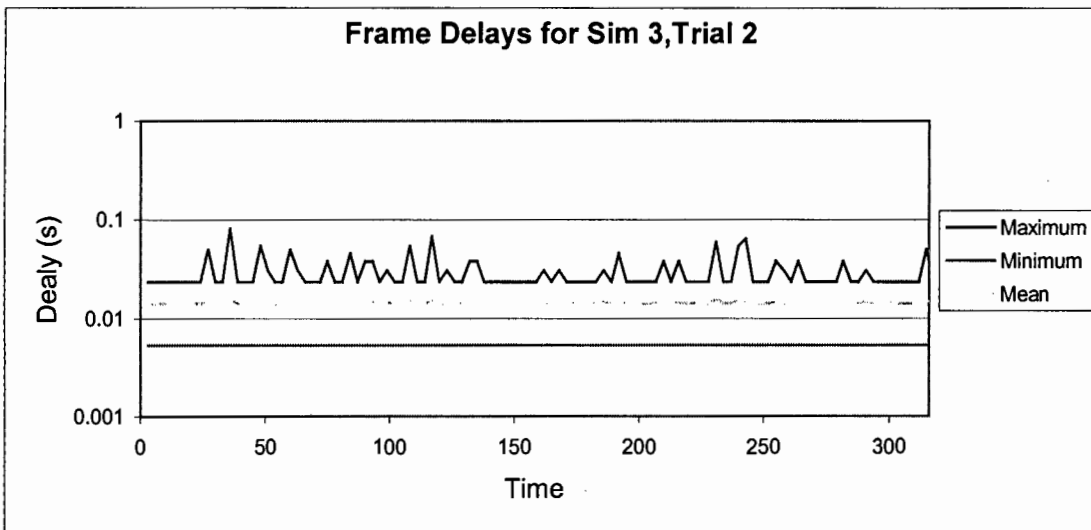
Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	22472000	29617672	0.758736	0.013077	0.077717	1.48E-03
2	22472000	50015488	0.449301	0.014436	0.08236	5.30E-03
3	22472000	31598488	0.711173	0.001566	0.050227	1.48E-03



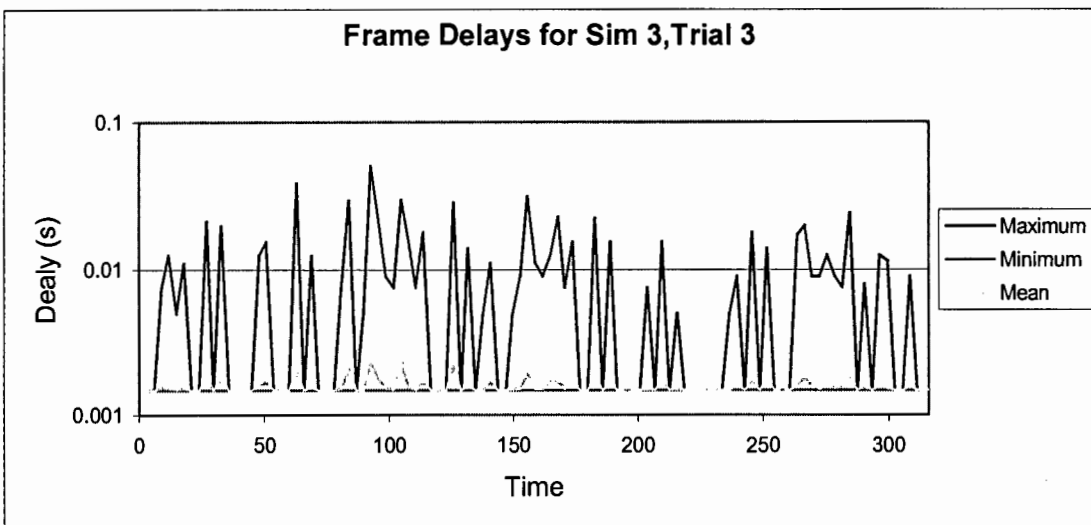
Graph 8-7 : Relative Efficiencies of the Schemes Over Time for a CBR Source in an Outdoor Rayleigh Fading Channel



Graph 8-8 : Cell Delays Plotted For Each Simulation Frame For Scheme 3 (Dynamic Rate)



Graph 8-9 : Cell Delays Plotted For Each Simulation Frame For Scheme 2 (RS(4)Conv(1/2))



Graph 8-10 : Cell Delays Plotted For Each Simulation Frame For Scheme 1 (RS(1))

8.4 Simulation Set 4 - Outdoor VBR Preliminary Study

8.4.1 Objective

Simulation set 4 is the final set in the preliminary evaluation group and the objective of the set is to gauge the performance of the error control schemes suggested in the outdoor wireless environment with a relatively low data rate VBR traffic source.

As with the previous simulation sets, the performance statistics of relevance are end-to-end efficiency, latency and jitter introduction.

The intercell delays for the traffic source are modeled on a standard MPEG-1 stream, downscaled by a factor of twenty.

8.4.2 Methodology

Traffic source	Modified VBR stream model.
Channel Model	Simulated outdoor cellular environment with Rayleigh fading.
Channel bit rate	400kb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

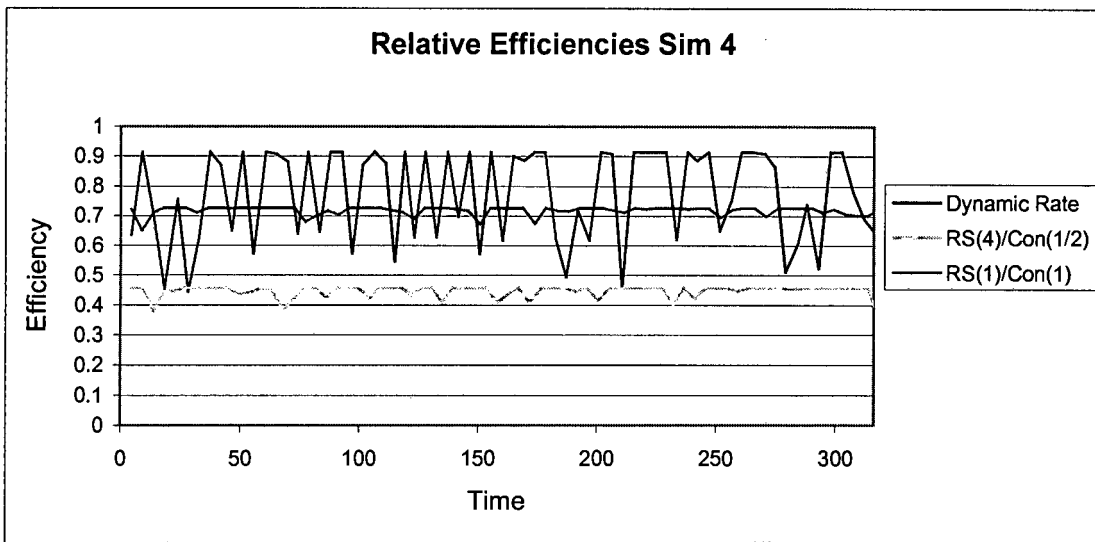
The following table documents the details of each of the 3 trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	4 cells/1 cell	1/2 / off	0.1	T10outa.txt
Trial 2	4 cells	1/2	0	T11outa.txt
Trial 3	1 cell	off	0	T12outa.txt

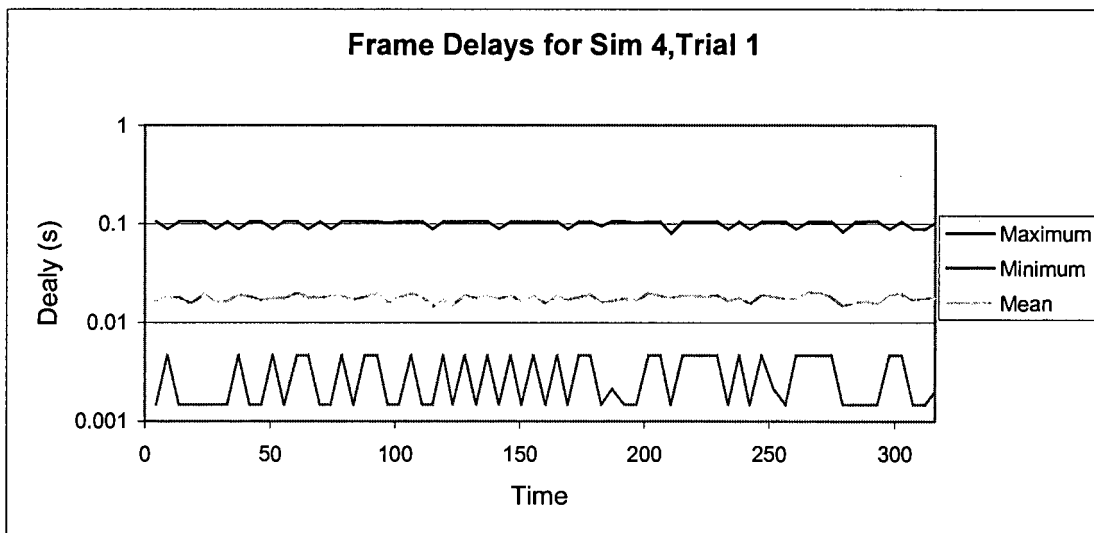
8.4.3 Results

Table 8-4 : Simulation Set 4 Numerical Results

Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	14628000	19871480	0.73613	0.017667	0.105297	1.48E-03
2	14840000	33382016	0.444551	0.019351	0.11363	5.30E-03
3	14628000	20410216	0.7167	0.002209	0.047108	1.48E-03



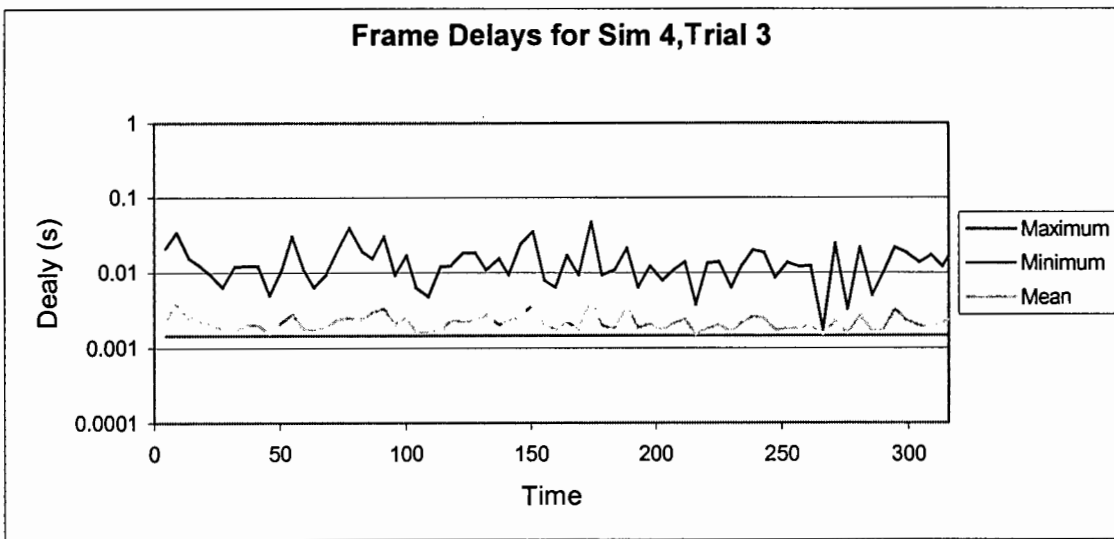
Graph 8-11 : Relative Efficiencies of Error Control Schemes Operating in an Outdoor Wireless Environment with a VBR Traffic Source



Graph 8-12 : Cell Delays Plotted For Each Simulation Frame For Scheme 3 (Dynamic Rate) .



Graph 8-13 :Cell Delays Plotted For Each Simulation Frame For Scheme 2 (RS(4)Conv(1/2)).



Graph 8-14 :Cell Delays Plotted For Each Simulation Frame For Scheme 1 (RS(1))

8.5 Simulation Set 5 - Use of Smaller Packets to Reduce Latency

8.5.1 Objective

From the preliminary simulation group, it may be observed that the use of a RS codec with a 4 ATM cell word may lead to the introduction of large latency times for cell delivery. For real time services, this may prove unacceptable. The objective of this simulation is the evaluation of a modified version of the dynamic rate codec where the RS(232,216,8) codec is removed from the scheme. In essence the modified scheme may switch in or out the convolution codec.

This set will evaluate the performance of the modified dynamic code rate scheme in the indoor pico-cellular environment with CBR/ABR and VBR traffic sources.

Introduced latency and jitter will be measured along with the scheme throughput and an effort will be made to reconcile the loss in throughput efficiency that the scheme may introduce against the potential jitter and/or latency reductions.

8.5.2 Methodology

Traffic source	Trial 1:64kb/s CBR source with intercell arrival times of 0.006s Trial 2 :MPEG 1 video stream with lognormal frame sizes
Channel Model	Measured indoor pico-cellular model with a non-correlated error sequence [21].
Channel bit rate	70Mb/s
Simulation Time	> 315s
Simulation Frame Size	Trial 1 :500 ATM cells Trial 2: 5000 ATM cells

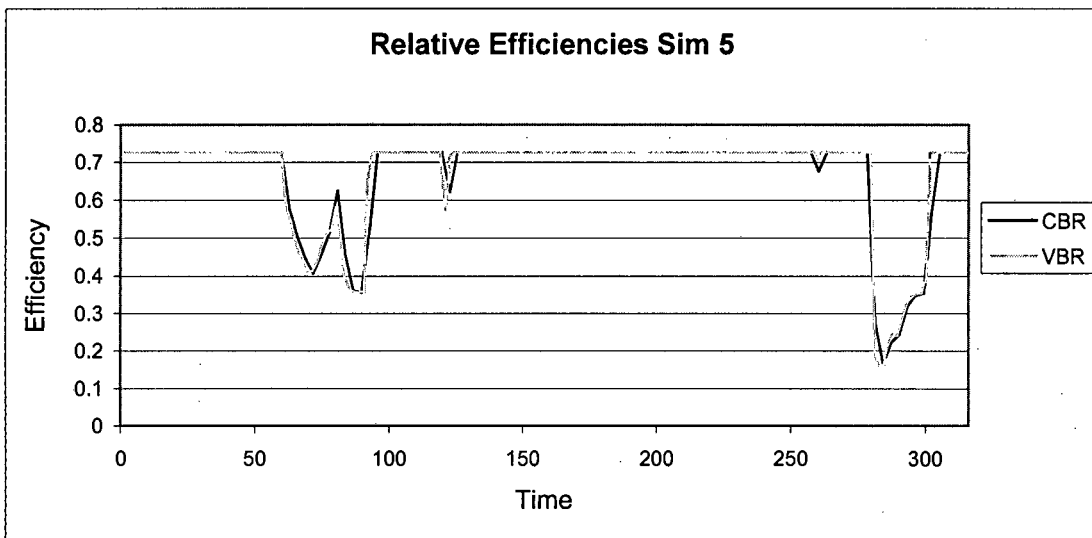
The following table documents the details of each of the trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	1 cell	1/2 / off	0.1	T13outa.txt
Trial 2	1 cell	1/2 / off	0.1	T14outa.txt

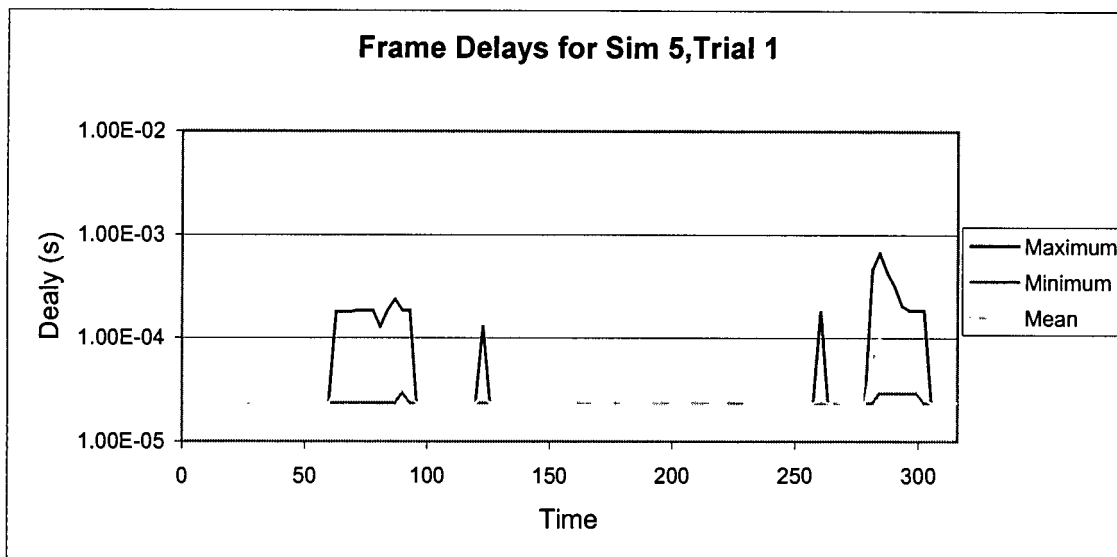
8.5.3 Results

Table 8-5 : Simulation Set 5 Numerical Results

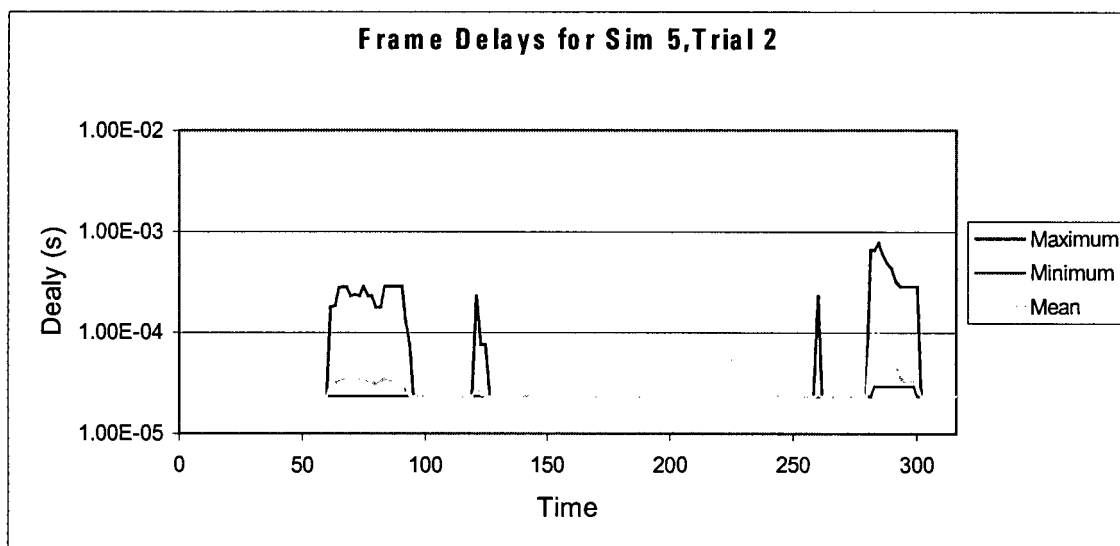
Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	22472000	36671112	0.612798	2.64E-05	0.000663	2.34E-05
2	392200000	642402920	0.6105202	2.6545E-05	0.0007208	2.34E-05



Graph 8-15 : Relative Efficiencies for Truncated Dynamic Rate Codec Operating in an Indoor Wireless Environment



Graph 8-16 :Cell Delays Plotted For Each Simulation Frame For Modified Scheme 3 (Dynamic Rate Truncated Code) with CBR Traffic.



Graph 8-17 :Cell Delays Plotted For Each Simulation Frame For Modified Scheme 3 (Dynamic Rate Truncated Code) with VBR Traffic

8.6 Simulation Set 6 - Indoor Environment with Increased Convolution Coding Gain

8.6.1 Objective

The preliminary set of simulations indicated that in the case of the indoor wireless channel presented in [21], the power of the suggested error control schemes was inadequate when the channel bit error rate became very high. This simulation set evaluates a modified version of error control schemes 2 and 3 (that is the concatenated fixed rate codec and the dynamic rate codec) where a more powerful 1/3 rate convolution codec is used.

Throughput efficiency, jitter and latency will be measured. These statistics may be used to compare the scheme to that with the higher rate convolution code.

The selected environment will be the indoor pico-cellular architecture, with the CBR traffic source.

8.6.2 Methodology

Traffic source	64kb/s CBR source with intercell arrival times of 0.006s
Channel Model	Measured indoor pico-cellular model with a non-correlated error sequence [21].
Channel bit rate	70Mb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

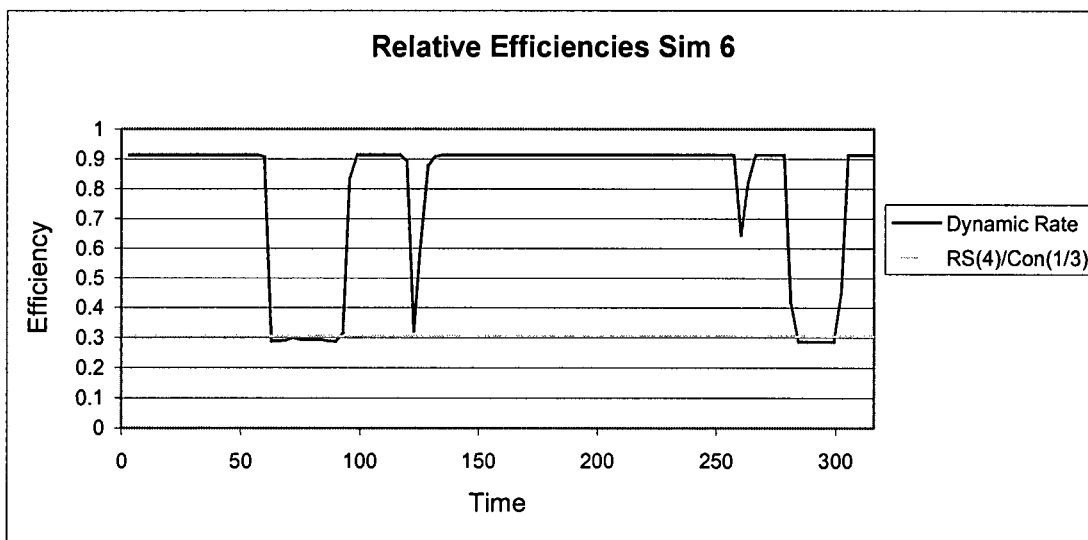
The following table documents the details of each of the trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	1 cell/4 cells	1/3 / off	0.1	T15outa.txt
Trial 2	4 cells	1/3	0	T16outa.txt

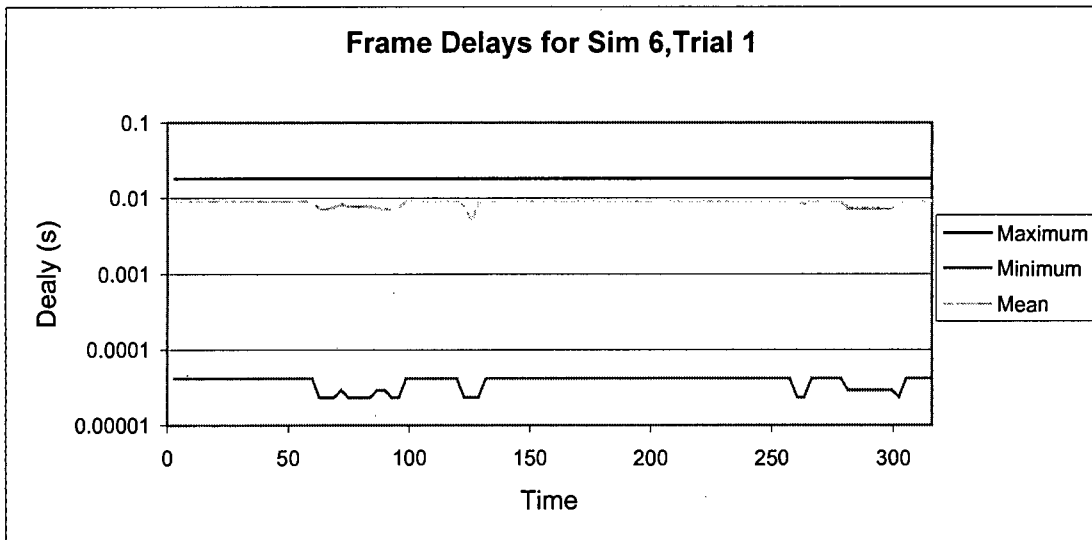
8.6.3 Results

Table 8-6 : Simulation Set 6 Numerical Results

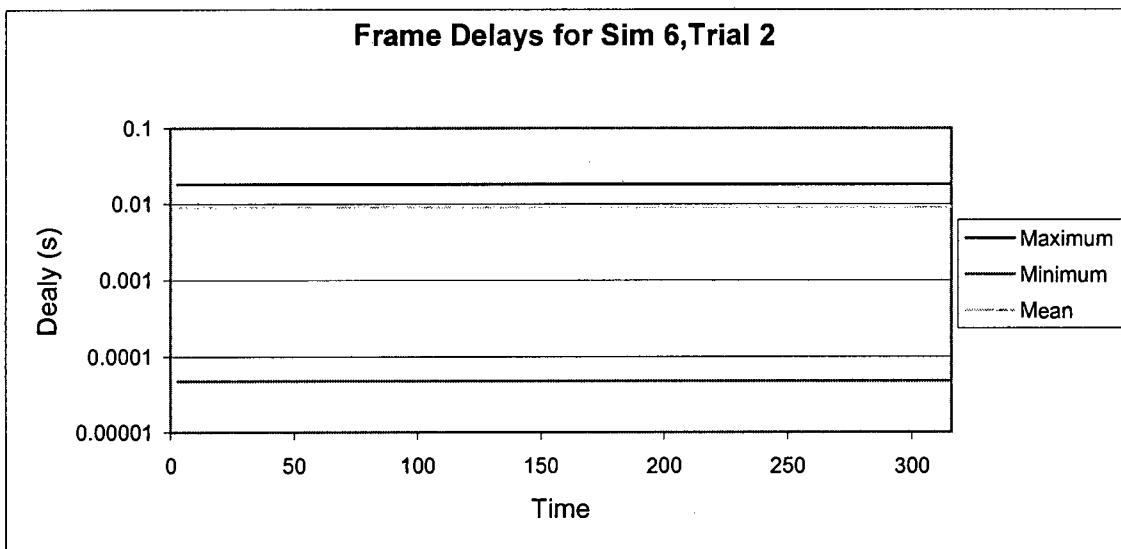
Model	Data Sent	Bits Sent	Eff. ' "	Avg Latency	Max Latency	Min Latency
1	22472000	34258128	0.655961	0.008666	0.018271	2.34E-05
2	22472000	73776000	0.304598	0.009047	0.018047	4.72E-05



Graph 8-18 :Relative Efficiency for Codes with Lower Concatenated Coding Rates Operating in an Indoor Wireless Environment with CBR Traffic



Graph 8-19 :Cell Delays Plotted For Each Simulation Frame For Dynamic Rate Scheme with Reduced 1/3 Rate Concatenated Codec



Graph 8-20 :Cell Delays Plotted For Each Simulation Frame for Scheme 2 With Rate 1/3 Concatenated Codec

8.7 Simulation Set 7 - Effect of Modifying Sigma

8.7.1 Objective

Preliminary results indicate that the dynamic scheme's performance in the outdoors channel with burst type errors may not be ideal – there were areas where the efficiency of the scheme dropped below that of scheme 1. This tends to indicate that there may be problems with the logic element's ability to track rapidly fluctuating signal levels.

This simulation set's function is to ascertain the impact of adjusted sigma levels on the performance of the dynamic rate codec in the presence of burst type errors.

The chosen simulation environment is the outdoors mobile environment with a modified VBR traffic source. The principle issue addressed is throughput efficiency, although as with all schemes latency and jitter levels are measured.

8.7.2 Methodology

Traffic source	Modified rate VBR traffic source.
Channel Model	Simulated outdoor cellular environment with Rayleigh fading
Channel bit rate	400kb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

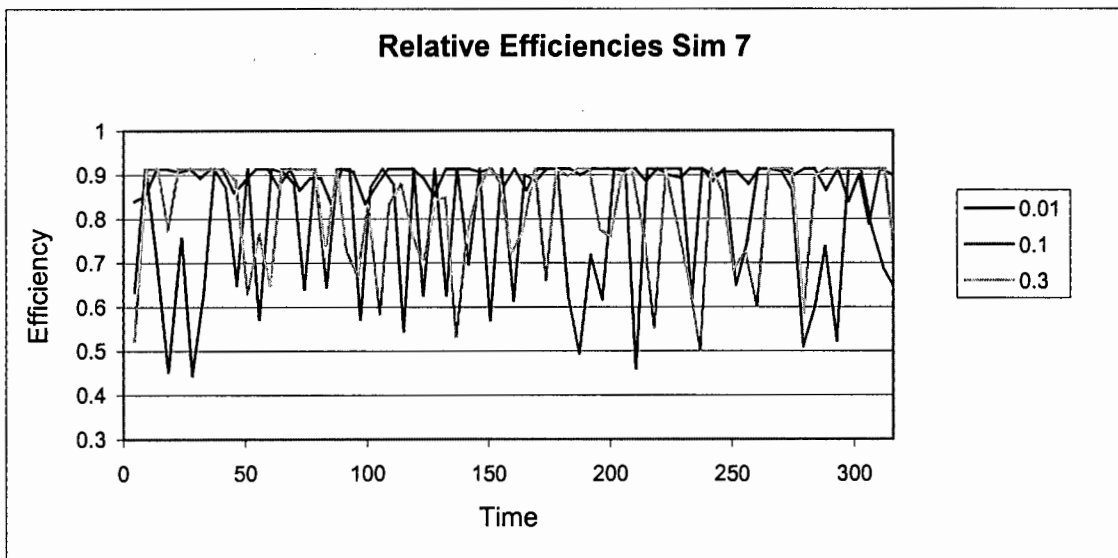
The following table documents the details of each of the 4 trials performed:

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	1 cell/4 cells	½ / off	0.01	T17outa.txt
Trial 2	1 cell/4 cells	½ / off	0.05	T18outa.txt
Trial 3	1 cell/4 cells	½ / off	0.1	T19outa.txt
Trial 4	1 cell/4 cells	½ / off	0.2	T10outa.txt
Trial 5	1 cell/4 cells	½ / off	0.3	T21outa.txt

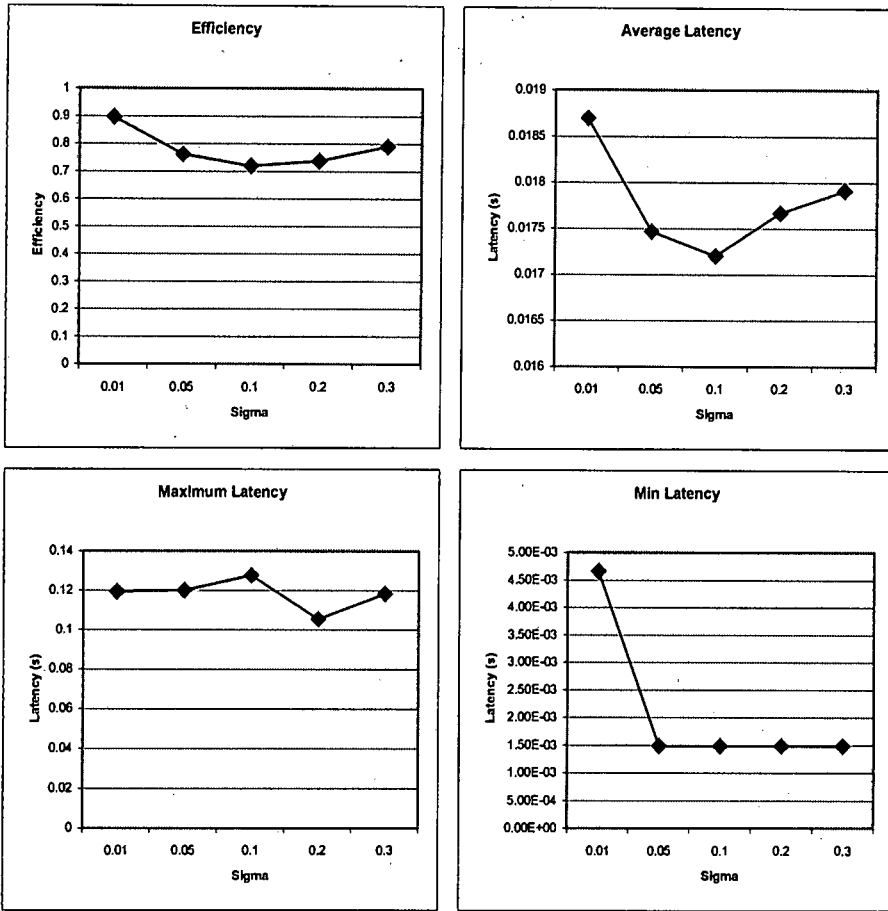
8.7.3 Results

Table 8-7 : Simulation 7 Numerical Results

Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	14628000	16334656	0.895519	0.0187	0.119295	4.66E-03
2	14628000	19229048	0.760724	0.017464	0.119926	1.48E-03
3	14840000	20648096	0.71871	0.017197	0.127607	1.48E-03
4	14628000	19871480	0.73613	0.017667	0.105297	1.48E-03
5	14628000	18545520	0.788762	0.017911	0.118382	1.48E-03



Graph 8-21 : Relative Efficiencies For Scheme 3 With 3 Sigma Values in an Outdoor Wireless Environment with VBR Traffic



Graph 8-22 : Graphs of Final Results for Various Sigma Values

8.8 Simulation Set 8 - Use of Shortened RS Codes

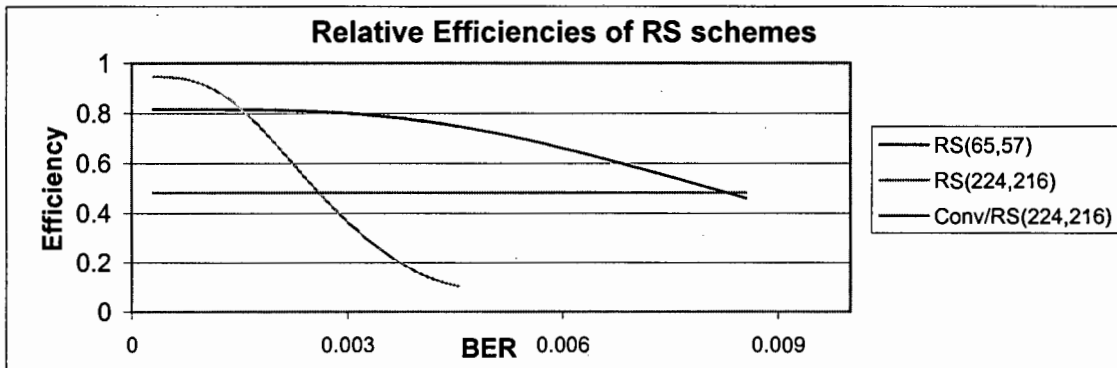
8.8.1 Objective

At the beginning of the project undertaking, the use of the (255,239,8) RS word was assumed. The objective of this set of simulations is to estimate whether there would be performance advantages in reducing the coding power for the RS code in the dynamic coding rate situation where the rate 1/2 convolution code is used. Instead of shortened codes from the (255,239,8) word, shortened codes from the (255,247,4) code will be used. This should provide an indication of whether there are performance advantages to be gained for the specific channel types used in reducing RS coding overhead.

8.8.2 Methodology

The first issue that must be resolved before the simulation may commence is the issue of the adjusted threshold values for the dynamic rate codec. These were calculated in the same manner as the initial thresholds for the 8-symbol-correcting-code.

The following graphic represents the efficiency cross over points calculated using a spreadsheet and the formulae introduced in Chapter 4.3.1.1.



Graph 8-23 : Efficiency Cross-Over Thresholds for Modified RS Scheme

Using an interpolation method, the calculated thresholds were:

	BER	WER
RS4-1	0.001579	0.1397
RS1-4	0.001579	0.0012
RS1 - Concatenated	0.0086	0.4394
Concatenated - RS1	X	0.0001

The threshold adjustments were then made to the platform, and the simulations performed with the listed parameter settings.

Traffic source	CBR 64kb/s voice source.
Channel Model	Test 1: Measured indoor pico-cellular environment. Test 2: Simulated outdoor cellular environment with Rayleigh fading.
Channel bit rate	Test 1:1.5Mb/s Test 2:400kb/s
Simulation Time	> 315s
Simulation Frame Size	500 ATM cells

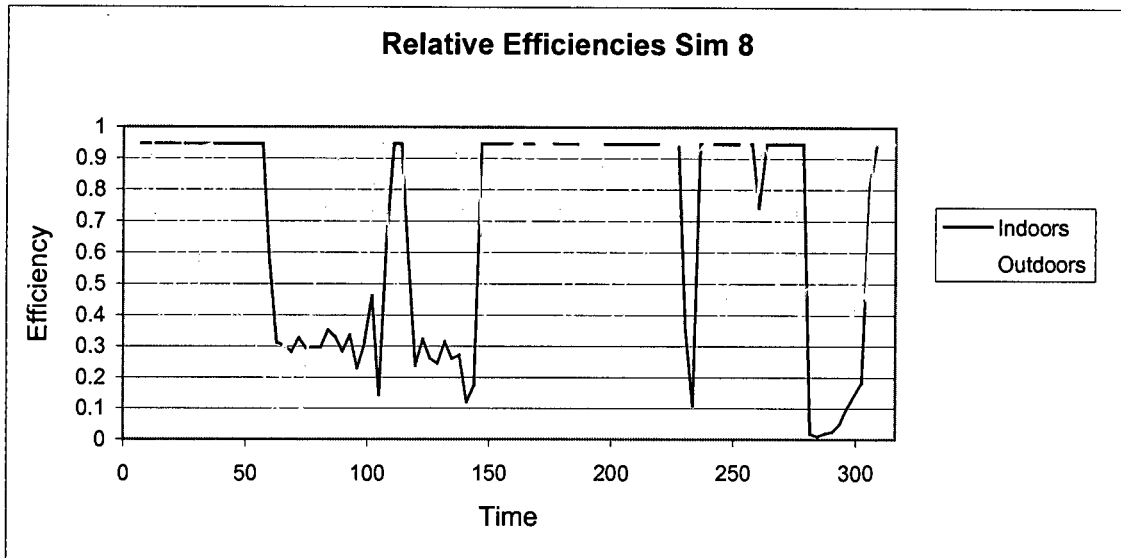
The following table documents the parameter settings of the 2 trials performed.

Trial Number	RS words lengths	Convolution rate settings	Sigma	Output file
Trial 1	1 cell/4 cells	½ / off	0.02	T22outa.txt
Trial 2	1 cell/4 cells	½ / off	0.02	T23outa.txt

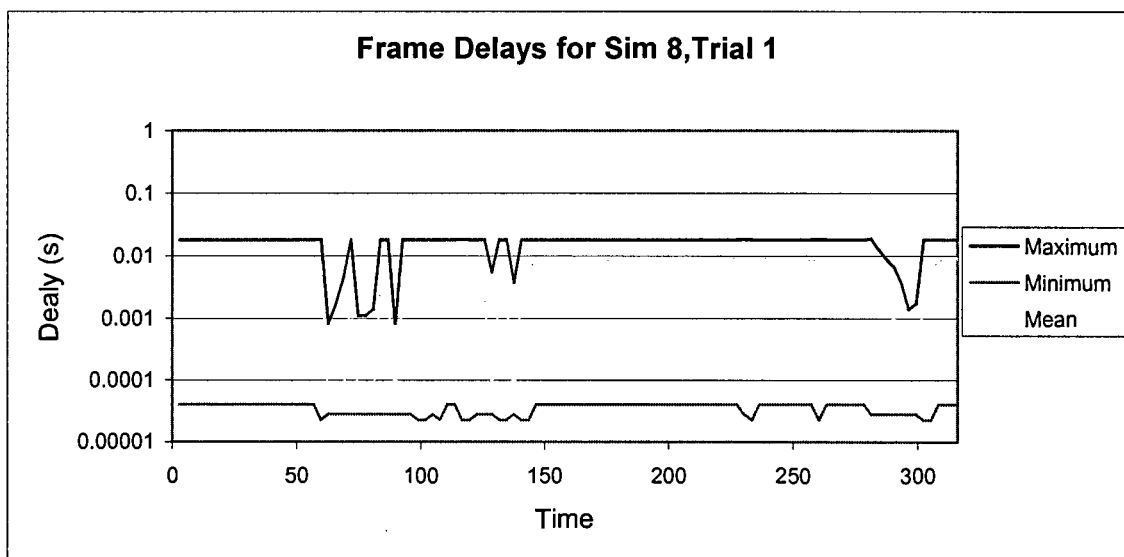
8.8.3 Results

Table 8-8 : Simulation 8 Numerical Results

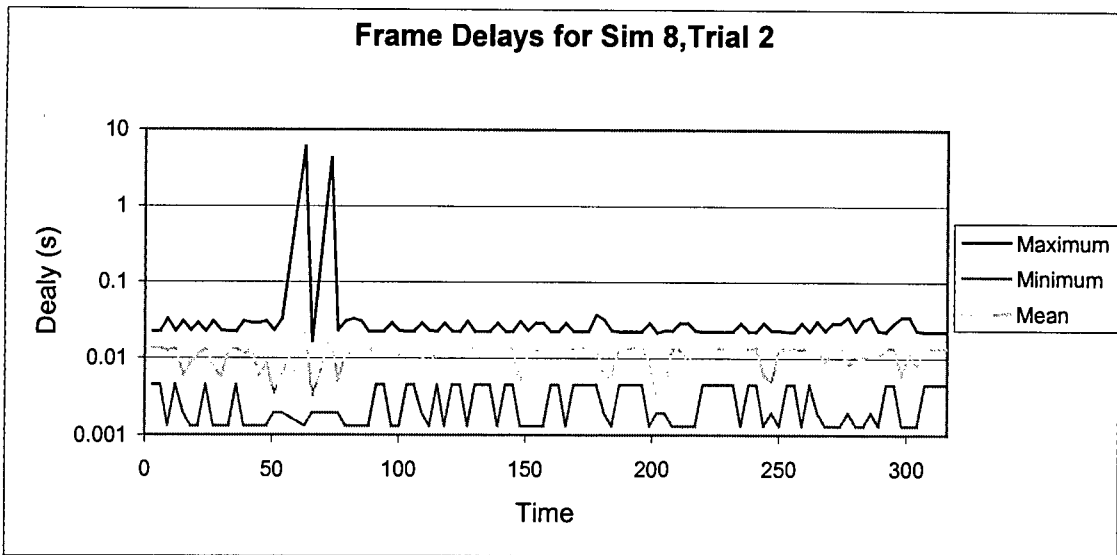
Model	Data Sent	Bits Sent	Eff.	Avg Latency	Max Latency	Min Latency
1	22472000	1.07E+08	0.210895	0.006683	0.018393	2.25E-05
2	21624000	39609632	0.545928	0.011551	6.00116	1.32E-03



Graph 8-24 : Relative Efficiencies For Scheme 3 With Reduced RS Protection in Indoor and Outdoor Environments



Graph 8-25 : Relative Efficiencies Plotted For Indoor Channel With Reduced RS Overhead and Dynamic Rate Scheme.



Graph 8-26 : Relative Efficiencies Plotted For Outdoor Channel With Reduced RS Overhead and Dynamic Rate Scheme

9 Discussion of Results

Having obtained the results of the simulations, it is necessary to perform an interpretation of the observations. From this interpretation conclusions regarding the performance of the schemes will later be drawn.

As was stated earlier, the simulations were divided into groups as the most course break-up and then further into sets. The objective of the first group was to gain a broad impression of the operation of the suggested error control schemes without *a priori* knowledge. The second group would then be composed of a series of tests to illustrate specific properties of the simulated error control schemes.

9.1 Simulation Group 1

9.1.1 Simulation Set 1 - Indoor CBR Preliminary Study

Environment:	Indoor Wireless Environment
Traffic Source:	64kb/s CBR
Coding Schemes:	i) Stand alone 1 cell RS codec.
	ii) Concatenated codec with 4 cell RS codec and rate $\frac{1}{2}$ convolution codec.
	iii) Dynamic rate code with 1 cell and 4 cell RS codes available and either rate $\frac{1}{2}$ convolution code, or no convolution code.

9.1.1.1 Bit Error Rate Issues

No bit errors were passed by any of the schemes. Clearly the end performance falls within the required bit error rate requirements for any traffic class, so long as the wireline network does not introduce additional errors.

9.1.1.2 Throughput Efficiency Issues

The indoor wireless environment model used is marked by an extraordinarily high level of BER variability, most likely due to the high levels of attenuation experienced by EM waves in the 10's of GHz region by barriers that would provide little attenuation to lower frequencies. This environment with high levels of attenuation proved very demanding on the coding schemes. Of the three schemes considered, only the dynamic rate scheme performed adequately (overall efficiency of 60%) when the channel quality deteriorated seriously since it has access to the most powerful of the possible coding schemes – the concatenated code with the RS codec operating with single cell frames and the rate $\frac{1}{2}$ convolution code. The results suggested that the other schemes were not really suitable for operation in this specific environment with efficiencies of 15% and less than 2%. If a fixed rate codec was to be used in this environment, higher coding gain would have to be utilized.

The results of this simulation indicate far superior performance of the dynamic rate code, even if the inadequacy of the other codes to handle poor channel characteristics is discounted. There was a period around the 70 second simulation period where the RS only scheme did perform better than the dynamic scheme, possibly indicating some error tracking deficiencies.

9.1.1.3 Latency Issues

As with the efficiency results, latency was adversely affected in the non-dynamic coding schemes. The latency performance of the non-concatenated codec was very poor, with a peak figure in excess of 20s – far exceeding the acceptable latency for CBR traffic. The other schemes provided latency statistics within the acceptable bounds for voice traffic (18ms for the dynamic rate scheme and 56ms for the concatenated, fixed rate scheme).

An interesting effect was the fact that in adverse channel conditions, the average latency for the dynamic scheme was lower than at other points in time where the BER was relatively better. This effect is counter-intuitive, since with the increase in ARQ activity, one would expect increased latency. The reason for the observed latency decrease is that the principle contributor to latency with the low rate voice link was packetization delay, which was reduced when the 1 cell RS frame was introduced in an attempt to increase coding gain.

9.1.1.4 Jitter Issues

As was stated earlier, jitter may be removed from the system through the use of buffering at the output stage. The required output buffer size to ensure that there is no perceived jitter introduction by the wireless link may be calculated by comparing the difference in time between the earliest and latest cell deliveries for each scheme. The buffer size required to eliminate jitter is equal to the difference in time between the latest possible cell arrival and the earliest possible cell arrival multiplied by the data rate in bits per second. When this buffer size is in operation, all cells would arrive with a latency equal to the maximum observed latency in the simulations, and no jitter.

For the dynamic scheme, the required buffer size would be 146 bytes or 3 complete ATM cells. Using this buffer, the cell delivery delay could be held at 18ms.

For the scheme utilizing the fixed rate concatenated codec, the required buffer size would be 450 bytes or 9 complete ATM cells. Using this buffer, the cell delivery delay could be held at 56ms.

The introduced latency in the RS only scheme discounts it as a serious contender for an implementation with a channel as poor as the one simulated here.

9.1.2 Simulation Set 2 - Indoor VBR Preliminary Study

Environment:	Indoor Wireless Environment
Traffic Source:	VBR MPEG Video Stream
Coding Schemes:	<ul style="list-style-type: none">i) Stand alone 1 cell RS codec.ii) Concatenated codec with 4 cell RS codec and rate $\frac{1}{2}$ convolution codec.iii) Dynamic rate code with 1 cell and 4 cell RS codes available and either rate $\frac{1}{2}$ convolution code, or no convolution code.

This simulation set was not completed since the inadequacies of the non-dynamic coding schemes to deal with the very high BER's meant inordinately long simulation times would be required to yield the same information presented by the simulation set 1, namely that higher coding gain is required when the BER deteriorates below 1 bit in 20. The results for the dynamic rate coding scheme are however relevant as they give an indication of the impact of the error control mechanism on the QoS constraints for a VBR traffic source.

9.1.2.1 Bit Error Rate Issues

No bit errors were passed to the higher layers. This clearly adheres to the QoS constraints specified for the VBR source.

9.1.2.2 Throughput Efficiency Issues

The measured throughput efficiency for the channel using the dynamic rate coding scheme was no different to that measured for the CBR traffic class, namely 60%.

9.1.2.3 Latency Issues

The maximum introduced latency for the scheme was 23ms, 5ms higher than the maximum latency introduced when the lower rate CBR traffic source was used. It is not immediately possible to deduce whether the extra latency was a result of increased packetization delay due to a traffic lull, or a result of increased ARQ activity associated with a high intensity burst

since the VBR traffic source is by definition unpredictable. We are however able to ascertain that the use of the error control scheme in the given channel allows the transmission of the data without breaking the latency requirements indicated for the VBR traffic class.

9.1.2.4 Jitter Issues

The approach to jitter that has been adopted in this project is to declare the traffic sources completely jitter intolerant and to use output buffering to smooth the traffic flow, so long as the latency requirements for the traffic classes are not broken.

An exact calculation for the buffer size required to smooth traffic for this class is not possible from the results obtained since the momentary data rate when the maximum introduced latency instance was realized is not known. It is however possible to estimate the approximate buffer size by the average traffic rate of the source.

Estimated required buffer size to completely remove system jitter is 4273 bytes, or 81 complete ATM cells. Assuming the estimate is correct, the cell delivery delay could be held at 18ms using the buffer.

9.1.3 Simulation Set 3 - Outdoor CBR Preliminary Study

Environment:	Outdoor Wireless Environment
Traffic Source:	64kb/s CBR voice.
Coding Schemes:	i) Stand alone 1 cell RS codec. ii) Concatenated codec with 4 cell RS codec and rate $\frac{1}{2}$ convolution codec. iii) Dynamic rate code with 1 cell and 4 cell RS codes available and either rate $\frac{1}{2}$ convolution code, or no convolution code.

9.1.3.1 Bit Error Rate Issues

No bit errors were passed by the system. The schemes clearly therefore operated within tolerable bit error rate specifications for the CBR traffic source.

9.1.3.2 Throughput Efficiency Issues

All of the suggested schemes were able to operate in the simulated outdoor environment without severe penalties to efficiency being incurred by the necessity of multiple ARQ's. In terms of the end to end throughput efficiency, the dynamic rate coding scheme dominated with the ability to switch to the low overhead option operating without the convolution codec and with the 4 cell RS code word. The overall channel efficiency for the dynamic code scheme was 76% with the stand alone RS code with a single word length frame exhibiting an end to end efficiency of 71%. The convolution codec exhibited a higher level of coding gain than required from an efficiency viewpoint and yielded an end to end throughput efficiency of 45%.

An issue that was observed was that there were time periods where the dynamic rate codec dropped its code rate through the introduction of the convolution code, and in doing so performed worse than the fixed rate RS codec. This effect indicates an inadequacy with the channel tracking algorithm to track the rapidly fading channel characteristics associated with the Rayleigh fading channel. This shows that in a physical implementation, a more sophisticated means of tracking the moment to moment channel characteristics would improve the performance of the scheme.

Another issue that was highlighted by the simulation set was that the convolution codec rate was too low for this particular channel environment. It overprotects the data, generating no real performance advantage for a substantial increase in overhead.

9.1.3.3 Latency Issues

All three of the schemes tested adhered to the maximum latency constraints indicated for the class of service utilized (CBR voice). The best scheme from the latency perspective was the stand alone RS scheme with maximum induced latency of 50ms. The reason for this performance was that there was no induced packetization delay with the scheme. The dynamic rate codec induced at most 78ms latency, while the concatenated codec introduced a maximum of 86ms latency.

9.1.3.4 Jitter Issues

To eliminate jitter with the schemes, the following buffer sizes would be required:

Dynamic rate concatenated codec: 609 bytes or 12 cells. Using this buffer, the cell delivery delay could be held at 78ms.

Fixed rate concatenated codec: 702 bytes or 14 cells. Using this buffer, the cell delivery delay could be held at 82ms.

Fixed RS only codec: 390 bytes or 8 cells. Using this buffer, the cell delivery delay could be held at 50ms.

9.1.4 Simulation Set 4 - Outdoor VBR Preliminary Study

Environment:	Outdoor Wireless Environment
Traffic Source:	Reduced rate VBR
Coding Schemes:	i) Stand alone 1 cell RS codec.
	ii) Concatenated codec with 4 cell RS codec and rate $\frac{1}{2}$ convolution codec.
	iii) Dynamic rate code with 1 cell and 4 cell RS codes available and either rate $\frac{1}{2}$ convolution code, or no convolution code.

9.1.4.1 Bit Error Rate Issues

No bit errors were passed by the encoders, and the performance of the schemes thus adheres to the requirements for any class of traffic so long as the wireline carrier adheres to the requirements for the service.

9.1.4.2 Throughput Efficiency Issues

There was no marked difference in the performance of the dynamic rate scheme over the fixed rate Reed-Solomon only scheme. Both schemes performed with an end to end efficiency of 72%. The fixed rate concatenated codec performed worse than either with an average end to end efficiency of 44%.

Once again the inadequacy of the channel tracking algorithm to follow rapid channel fluctuations was illustrated by the fact that the dynamic code rate performed no better than the fixed rate RS only code.

9.1.4.3 Latency Issues

The only scheme of the three simulated that adhered to the 100ms latency constraint was the codec operating with the stand alone 1 cell RS code. The maximum latency introduced by this scheme was 47ms. Latency introduced for the other two schemes was in excess of 110ms. The principle cause of the massive latency was the use of a very low data rate VBR source.

The packetization delay associated with the large frame became prohibitive. The VBR source was in some ways artificial with a very low data rate (+- 48kb/s) and this yields an unfairly pessimistic impression of the performance of the scheme when higher data rate streams are utilized.

9.1.4.4 Jitter Issues

As was stated with the MPEG encoded VBR source preliminary test, the exact size of the buffer required to completely eliminate the presence of jitter may not readily be calculated because the moment to moment data rate for the source is not known. An estimate for the required buffer size may however be obtained through the utilization of the average data rate.

Dynamic rate concatenated codec: 598 bytes or 12 complete ATM cells. Assuming the estimated buffer size is correct, the cell delivery delay could be held at 105 ms.

Fixed rate concatenated codec: 657 bytes or 13 complete ATM cells. Assuming the estimated buffer size is correct, the cell delivery delay could be held at 114 ms.

Fixed RS only codec: 365 or 7 complete ATM cells. Assuming the estimated buffer size is correct, the cell delivery delay could be held at 47ms.

9.2 Simulation Group 2

9.2.1 Simulation Set 5 - Use of Smaller Packets to Reduce Latency

Environment: Indoor Wireless Environment
Traffic Source: 64 kb/s CBR voice stream.
MPEG 1 video source.
Coding Schemes: Dynamic Rate codec with RS frame length fixed to 1 cell and either rate 1/2 or rate 1 convolution code.

9.2.1.1 Efficiency Changes

It was anticipated that the efficiency of the dynamic coding rate scheme would drop when the number of possible operating modes was reduced. This was not however the case. The actual operating efficiency increased by 1%. The only reasonable explanation for this is that the dynamic rate control element was incapable of accurately tracking the channel characteristics so that the correct rate scheme could be selected for any given SNR.

9.2.1.2 Latency Reduction Due to Elimination of Packetization Delay

The principle objective of the simulation was to explore the impact of eliminating packetization delay introduced through the use of 4 cell RS words. To achieve this end, the 4 cell length codes were removed from the dynamic rate scheme and simulations on the indoor channel were repeated. The maximum induced latency for the 64kb/s channel was 663 μ s, and the figure for the VBR source was 721 μ s.

These figures are substantially below the required 100ms latency figures for the traffic classes, indicating that packetization delay is a major contributor to delay, particularly for low data rate traffic. This indicates that low data rate or very delay sensitive traffic should not make use of the larger frame option.

9.2.2 Simulation Set 6 - Indoor Environment with Increased Convolution Coding Gain

Environment:	Indoor Wireless Environment
Traffic Source:	64 kb/s CBR voice.
Coding Schemes:	i) Dynamic rate coding scheme with 1 and 4 cell RS word and convolution rate of 1/3 or 1. ii) Concatenated code with 4 cell RS frame and 1/3 rate concatenated code.

9.2.2.1 Throughput Efficiency Changes

The motivation for this simulation set was to explore the impact of reducing the convolution code rate in the non-benign indoor environment, to ascertain whether the suggested rate 1/2 code was in fact under-powered for operation in an environment such as that measured.

The impact on the end-to-end throughput efficiency for the dynamic rate code was improved by an overall figure of 6%. The impact on the fixed rate concatenated code was far more marked, moving from an efficiency of 15% for the concatenated codec with 1/2 rate convolution code to 30% for the rate 1/3 code.

The results obtained tend to indicate that the use of the rate 1/3 code in the concatenated codes used in the test channel offers substantial performance advantages over the use of the rate 1/2 code.

9.2.2.2 Latency Changes

The maximum induced latency for the schemes, for both error control mechanisms was 18ms, well below the specified latency limit. This result was the same for the dynamic rate scheme as when the rate 1/2 concatenated codec was used. The fixed rate concatenated coding scheme performed better than when the rate 1/2 code was used since fewer successive ARQ were called, dropping the maximum induced latency to 18ms from 50ms.

9.2.2.3 Jitter Changes

With regard to the dynamic rate scheme, there was little perceived jitter improvement since the packetization delay was still the greatest contributor to latency (rather than transmission delay) and this meant the increased frame lengths associated with the rate 1/3 frame hardly affected performance.

The jitter on the fixed rate scheme was reduced since the maximum latency was decreased. This would imply that smaller buffer sizes would be required with this scheme in the given environment.

9.2.3 Simulation Set 7 - Effect of Modifying Sigma

Environment: Outdoor Wireless Channel

Traffic Source: 64kb/s CBR voice

Coding Schemes: Dynamic Rate Code with sigma values of 0.01,0.05,0.1,0.2,0.3

9.2.3.1 Effect of Adjusting Sigma on Efficiency

Observing the performance of the dynamic rate codec in the presence of rapidly changing signal characteristics indicated that the channel tracking facilities were incapable of following rapidly changing signal strengths. This experiment was conducted in an attempt to observe the impact of adjusting the sigma factor on the throughput efficiency of the scheme.

The results of this experiment indicated that the sigma of 0.1 was situated in a performance depression (with end to end efficiency of 72%). Decreasing the sigma value to 0.01 improved the channel efficiency to 90% from 74% (for the 0.2 sigma simulation) while increasing the sigma value to 0.3 improved the channel efficiency to 79%.

The most probable explanation for the local performance depression is that the performance degradation was caused by switch down to a low rate coding scheme for a short lived channel fluctuation. The recovery to the higher rate code was then lengthy. The lower sigma value thus improved performance because the switchover to lower rates was made less likely, while the higher sigma made the recovery time from the low rate operation mode smaller.

9.2.4 Simulation Set 8 - Use of Shortened RS Code Word

Environment: Outdoor Wireless Channel
Indoor Wireless Channel

Traffic Source: 64kb/s CBR voice

Coding Schemes: Dynamic Rate Code with Reduced RS Overhead (8 bytes added, capable of correcting 4 symbol errors).

9.2.4.1 Efficiency Issues

Reducing the amount of overhead did not improve the system performance in either of the simulated channel environments. In the case of the indoor test, the efficiency perceived dropped to 21% from 60%. In the indoor environment the through efficiency dropped to 55% from 76%. From an efficiency point of view, there is an apparent degradation of the performance when the RS rate is dropped.

9.2.4.2 Latency Issues

The system indicated a maximum induced latency for the outdoors channel of 6s. This far exceeds the permissible latency for the CBR traffic class. In the indoor environment the introduced latency was comparable to that introduced for the standard scheme with the 8 symbol error correcting RS word. Clearly the outdoors channel passed through a period where the induced bit error rate exceeded the error control mechanism's recovery abilities.

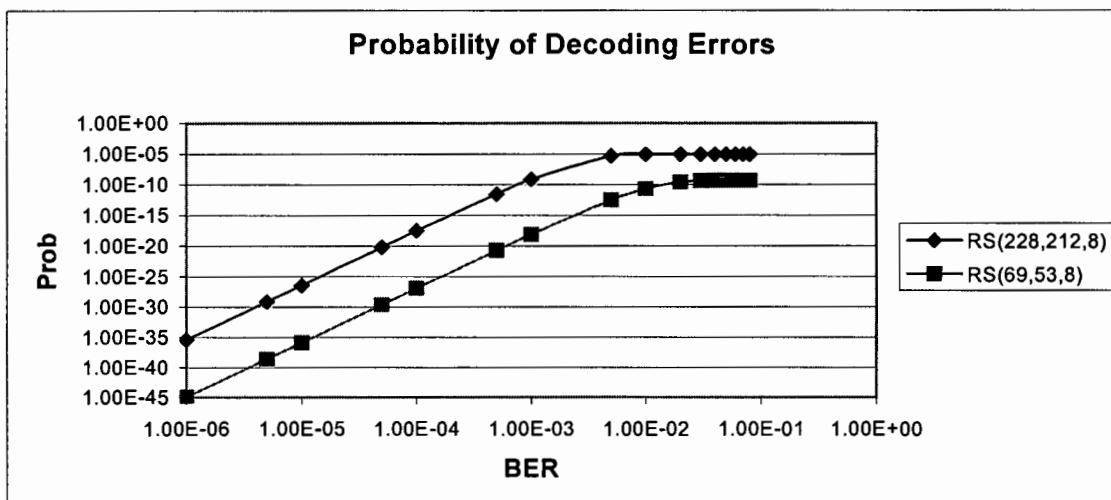
10 Theoretical Discussion of Post Decoding Error Rates and Header Error Probabilities

In the simulations performed, hundreds of millions of bits were transmitted without the reception of a single bit error. While an error free operating environment is clearly a boon from the application's point of view, it may indicate excessive protection. A CRC32 check was appended to each frame transmitted, adding an overhead of 4 bytes to each frame. While enhancing the error detection capabilities of schemes used, the additional overhead does reduce system throughput.

The objective of the section that follows is to explore the impact of using less powerful CRC checks, making partial use of the innate ability of the RS codes present in all the coding schemes to detect situations where uncorrectable errors are present. The first stage in the investigation process is to evaluate the probability of incorrectly decoding an RS word (i.e. the probability that the RS codec is not aware of the presence of errors). Once this has been calculated, the minimum power of the CRC check to be used may be ascertained.

10.1 Probability of Incorrectly Decoding an RS Codeword

Appendix A includes a section on the probability of incorrectly decoding an RS word and presents the formula for the probability of undetected errors (Equation AA-27, Appendix A). This formula was numerically evaluated using a C routine to yield the results in the chart below.



Graph 10-1 :Probability of a Decoding Error for a Code Word at a Given BER

The graph indicates that the probability of incorrectly interpreting an irreparably damaged word of a shortened RS code-word as a reparable word may be as high as 1 in 10^5 under certain error conditions.

10.2 Required Power of CRC Check to Adhere to QoS Constraints and Header Error Values

There are two considerations regarding the required power of the CRC check associated with each frame. The first is that the QoS requirements stipulate the maximum tolerable BER associated with each traffic class. The second consideration is that the native ATM format requires certain protection levels on the header, and with specific reference to the error control mechanism illustrated here, cell ordering problems may occur if errors are introduced into the re-sequencing field.

As was stated in the introductory section, each class of service has different QoS requirements in terms of the allowable perceived bit error rate. For the sake of this discussion, the maximum permissible BER's for the classes of traffic considered will be:

CBR (voice): 10^{-6}

VBR (MPEG): 10^{-10}

ABR (data): 10^{-7}

A theoretical analysis will be conducted to estimate the minimum necessary power for the CRC check. A precise study of the power of the CRC will not be undertaken owing to both the complexity of the combinatorial mathematics required to derive precise bit error characteristics of the post decoded RS words, and the complexity of precisely ascertaining the error probability of a shortened CRC check. Comprehensive empirical evaluation is also not feasible owing to time constraints. The computational complexity and sample sizes required for error rate estimations make the run-time required excessive. Instead the approximate formula for undetected errors after CRC decoding presented in Appendix C will be used in conjunction with a simplified estimate of the post RS decoding error statistics. Owing both to the imprecision of the obtained estimates, and the byte-centric orientation of the scheme to date, the resolution of the suggested CRC checks will be limited to bytes. After analysis, either the CRC8, CRC16, CRC24 or CRC32 check will be suggested for frame protection. It should be noted that owing to the number of sweeping assumptions made by the analysis that

follows, its application directly is limited. It is instead intended for the sake of completion to estimate the performance of the scheme in terms of the introduction of bit errors and header errors in a worst-case-scenario type environment, not provide concrete bounds on the expected performance. A precise analysis could be undertaken as a separate project if performance bounds are required. See [27;30] for details.

The analysis that follows will list the assumptions made in reaching an estimate on the perceived bit error rate passed to the ATM layer.

Assumption 1 - Because the CRC check to be appended to the frame's length is to be ascertained, the length of the CRC will be excluded from the frame. This will slightly modify the performance of the RS code, but the impact is likely to be small and this section is intended for estimation purposes only.

Assumption 2 - The impact of ARQ extending the effective amount of data transmitted for a fixed information segment will not be included. Failure rates will be calculated on the probability of failure for the first transmit attempt.

Assumption 3 - Assume worst case channel scenario from the graph indicating the probability of incorrect decoding. That is (228,212,16) type RS word, with channel bit error rate of 0.1. The probability of incorrect decoding of the RS code word in this case will be taken to be 10^{-5} (read from Graph 9-1).

Based on the BER given in assumption 1, with an operating frame length of 212 symbols or 1696 bits, we may expect on average 1696×0.1 bit errors in the frame or 170 bit errors.

Assumption 4 - Assume that 170 bit errors are present in the frame that is to be considered.

Given that a word is incorrectly decoded, between 0 and 8 symbols may be spuriously regenerated by the decoder.

Assumption 5 - Assume that 4 symbols are written over by the decoder (this is chosen as an average figure).

Given that 4 symbols are incorrectly decoded, additional errors will be introduced into the frame. The error estimate may be based on the notion that 4 symbols of 8 bits each are in error. This means 32 bits are regenerated. Half of these bits will be incorrect, and of these, 10% will already have been errored in the channel. This implies the introduction of another approximately $(4 \times 8 \times 0.5 \times 0.9)$ bit errors in the frame - approximately 14 additional errors.

Assumption 6 - Assume that 14 additional bit errors are appended to the frame, yielding a total of 184 bit errors in the frame.

From assumption 3 and assumption 6, one may estimate the post decoding bit error probability to be (excluding errors introduced through headers):

$$\frac{184}{1696} \cdot 10^{-5} \cdot P_{CRC_FAILURE}$$

Assumption 7 - Assume that the probability of failing to detect an error by a CRC element with m order generator polynomial is 2^{-m} . This ignores the impact of shortening CRC words.

From the estimate on the post decoding bit error rate based on the probability of CRC failure, one may estimate the required power (RP) of the CRC check on a per traffic class basis to adhere to the QoS constraints. The CRC length required to generate the required power for the CRC check based on Assumption 7 will also be listed in the table that follows:

Table 10-1 : CRC Power Calculations

Class	Required Power (i.e. min error rate probability)	Required CRC
CBR	$RP = 1$ from $RP \times (184/1696) \cdot 10^{-5} \leq 10^{-6}$	None
VBR	$RP = 9.2E-6$ from $RP \times (184/1696) \cdot 10^{-5} \leq 10^{-10}$	CRC17 since $17 \geq \log_2(10^5)$
ABR	$RP = 9.2E-2$ from $RP \times (184/1696) \cdot 10^{-5} \leq 10^{-7}$	CRC4 since $4 \geq \log_2(10)$

If one CRC check is to be applied to all the traffic classes, then the CRC24 check must be used in order to ensure that at no time does the perceived bit error rate break the QoS constraints for any traffic class. The specified resolution on the CRC is 8 bits and 24 is the smallest multiple of 8 greater than or equal to the 17 bit requirement for the VBR traffic class. Assuming the use of the CRC24, we will be able to gain an

estimate of the probability of an undetected error in the header or cell sequence number.

To estimate the post decoding probability of a header error or cell sequence error in the environment specified in assumption 3, we must first estimate the probability of incorrect decoding of the RS code-word and of failure of the CRC24 check. From assumption 3 and assumption 7 using a CRC24 check, the combined probability of RS decoder and CRC failure is :

$$10^{-5} \times 2^{-24} \text{ or } 5.96 \times 10^{-13}$$

Assumption 8 - The probability of error check failure will be 5.96×10^{-13} .

Given a bit error rate of 0.1 and the fact that incorrect decoding has occurred, we may estimate the probability that at least one bit in the header has been adjusted.

Two sources of errors exist, the first being through the channel introduced errors and the second through the introduction of errors due to incorrect decoding.

The probability that a random bit error occurred in the header is equal to:

$$1 - P(\text{NO BIT ERRORS}).$$

For the 5 symbol or 40 bit header with the 0.1 bit error rate specified in assumption 3, the probability of introducing an error in the header is:

$$1 - (0.9)^{40} \text{ or } 98.52\%.$$

From this figure it is clear that there is no need to calculate the probability of additional error introduction through the incorrect RS decoding procedure since the probability of error introduction is very nearly 1. We may therefore deduce that the post RS and CRC header error probability for the system is less than 10^{-12} . Using the original CRC32 decreases this by a factor of approximately 2^8 .

11 Conclusions

As a result of simulations and analysis performed on the generic error control architectures suggested for implementation in wireless environments, a number of conclusions may be reached.

11.1 Bit Error Rate Performance Of Suggested Schemes

Through testing it was shown that the addition of an effective error control strategy consisting of FEC, CRC activated ARQ and interleaving elements, the wireless links considered in this project may appear effectively transparent to the higher layers of the ATM protocol stack in terms of their effect on QoS parameters. Since an ARQ element was present, the effective perceived bit error rate of a link was dependant on the test element that triggered the ARQ's ability to detect errors. It was estimated that a CRC check generated by an order 24 polynomial would adequately protect the data payload for any traffic class as long as the CRC check was operating in conjunction with an RS codec operating with a 16 byte parity segment (using shortened versions of the RS(255,239,16) code).

An estimation of the likelihood of errored cell headers was estimated to be less than 1 in 10^{12} , even in the most hostile of operating conditions. Should this be considered unacceptable, use of a CRC 32 check could boost this figure to better than 1 in 2×10^{14} . Tests run with the CRC32 did not generate a single bit error for hundreds of millions of transmitted bits. Although the sample was not high enough to be certain from an empirical view point that the perceived error rate adhered to the classic QoS constraints for a VBR link, it was high enough (in excess of 10 times the number of bits required to on average receive a single bit error [3]) to infer that the assumed QoS constraints for CBR and ABR were not broken through the action of the wireless link segment.

It may thus be concluded that the addition of a FEC based error control strategy makes possible the use of a channel that would not otherwise be practically harnessed, because of the adverse impact of random bit errors on the non-error tolerant elements of the ATM protocol.

11.2 Throughput Efficiency and Dynamic Coding Rates

Observing the channel characteristics associated with the measured indoor wireless environment, it was clear that the wireless terminal may be exposed to extraordinarily variable bit error rates, particularly if high carrier frequencies are used. Committing a channel to a fixed rate code therefore implies that either sufficient coding gain is provided when the link conditions are adverse and bandwidth is wasted when conditions are good, or the terminal ceases to operate correctly in poor conditions. Although dynamic rate coding adds additional system complexity at the MAC level, the advantages are clear. Simulations indicated substantial throughput efficiency gains for the highly variable indoor channel through the use of dynamic rate adjustment, with non-dynamic schemes performing poorly by comparison.

From observations of the action of the dynamic rate scheme in conditions of rapidly changing signal strengths (the outdoor wireless channel with Rayleigh fading), it was clear that the ARQ based rate control mechanism was incapable of tracking rapidly fluctuating signal strengths and a better means of checking signal strength may lead to performance gains. A clear example illustrating the inadequacies of the tracking mechanisms was the case where a reduced set of RS coding words lead to an improvement in throughput efficiency, contrary to the theoretical expectations. In a physical implementation, it is likely that the MAC layer would have access to a hardware based estimate of the channel characteristics, and this could be used for coding rate control. While the outdoor simulation may have given a slightly pessimistic impression of the dynamic rate coding mechanism, it should be remembered that the model did not consider changing attenuation with distance from the base station in the actual simulation. The indoor model was used as a sole means of exploring the impact of slow, but large scale signal fluctuations. It is therefore likely that the existing dynamic rate coding scheme would still show large performance advantages in an outdoor environment as long as the sigma level was set low enough not to be affected by the fast Rayleigh fading.

It may be concluded that the dynamic rate scheme presents substantial efficiency advantages over non-dynamic rate schemes, as it makes possible the use of powerful error control mechanisms for use when the channel characteristics became poor, without introducing excessive overhead at other times, but a more effective means of tracking the momentary SNR should be found for a practical implementation.

11.3 Latency Issues

The greatest source of latency for the low data rate traffic sources was packetization delay for schemes with frame lengths of 4 ATM cells. In the case where the data rate was low, the induced delay was more than the assumed permissible latency introduction for the real-time traffic classes of 100ms. The other reason for the proposed schemes breaching the latency constraints was when the schemes floundered due to inoperable data rates. The dynamic rate scheme was however able to function without this effect in the modeled channel environments.

One may conclude that the dynamic rate coding scheme suggested does not break the QoS requirements set on timing for either the ABR,CBR or VBR traffic classes as long as the data rate did not drop below 64kb/s for a real-time application in the tested channels. Given a low data rate or very delay sensitive application, a modified scheme composed of a subset of the possible rates is advised. This scheme would ignore the use of the long RS words, substituting some efficiency for improved timing results.

11.4 Jitter Issues

To avoid the complexity of optimizing with two QoS constraints, it was assumed that the real-time applications would be jitter insensitive, trading off additional latency for zero jitter. Buffer sizes required to achieve this state were specified and did not exceed 5kB. Since the schemes performed well within the latency requirements, this is not an unreasonable assumption.

11.5 Specific Coding Rates and Extension of Scheme to Any Environment

With the dynamic rate coding scheme, this dissertation presents a generic error control mechanism that may easily be applied to a variety of wireless environments. Clearly, there are however parameters in the scheme that must be adjusted to suit the environment. Through the use of simulations for example, it was found that the most appropriate convolution coding scheme for an indoors environment with similar SNR properties to that simulated would be a rate 1/3 concatenated codec that could be switched in or out, operating in concatenated mode

with the 8-error-symbol-correcting RS code. In other environments, this and parameters such as the RS word length and RS overhead could be adjusted to refine the operation of the error control mechanism. What is therefore presented is a suggested error control infrastructure, with parameter values optimized for a specific environment, rather than a pre-refined mechanism for generic operation.

12 Recommendations and Future Work

During the course of the study, several areas of interest were highlighted, but fell out of the scope of this project. Further research into the topics listed below could provide further understanding of the practical implementation and operation of the suggested error control method.

Description of the MAC strategy - In the study, it is assumed that a TDMA type MAC protocol is used, with adequate free time slots to allocate additional bandwidth to the application up to the maximum data rate for the wireless channel. The statistical effect of multiple users competing for the same spectral space is not considered. A further study to ascertain the number of users that could be supported given the assumed channel conditions, for a given traffic type could be of interest.

Control Channel Implementation - The control channel that is used by the MAC layer to negotiate for system resources and request automatic repeat requests is assumed to be perfect (i.e. to have sufficient FEC overhead to make the probability of data errors insignificant). Further study into physical implementation of this channel and the implications of imperfections could be undertaken, and would be necessary if the suggested control schemes were ever to be used.

Mathematical Evaluation - A comprehensive mathematical study of the concatenated codec could be undertaken as an academic exercise. It was not included in the project as the operation of the two codecs comprising the concatenated codec were independently verified. See [71] for details.

Viterbi Soft Decoding - A hard decision decoding method was used with the Viterbi decoder as the channel model and the decoding modules were independently developed. The implementation of soft decision decoding for the convolution codec could provide an element of gain and enhance the performance of the schemes somewhat.

Dynamic Rate Control - The ARQ based rate control module was found to be inadequate in some circumstances. A study to use the moment to moment signal strength figures known by the receiver to negotiate moment to moment code rates could be undertaken as this would offer performance advantages with respect to tracking the moment to moment data error rate. Likewise, the RS algorithm is able to ascertain the average number of symbol errors per cycle and this information too could be used to make better rate control decisions, enhancing the performance of the dynamic rate error control scheme.

Hybrid Type II Scheme - A further study into the possible advantages of a hybrid type II ARQ system could be undertaken to broaden the coding possibilities offered by the error control architecture.

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14 Glossary

List of Acronyms

AAL	ATM Adaptation Layer
ABR	Automatic Repeat Request
ACK	Acknowledge
ARQ	Automatic Repeat Request
ATM	Asynchronous Transfer Mode
CBR	Constant Bit Rate
C-MAC	Core - Media Access Control
CODEC	Encoder/Decoder
CRC	Cyclic Redundancy Check
DLC	Data Link Control
FEC	Forward Error Correction
HEC	Header Error Correction
MAC	Media Access Control
N-ACK	Negative Acknowledge
OQPSK	Offset Quadrature Phase Shift Keying
pdf	Probability Density Function
PHY	Physical Layer
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RS	Reed-Solomon
SAR	Segmentation and Re-assembly
S-MAC	Supervisory - Media Access Control
SNR	Signal to Noise Ratio
UNI	User Network Interface
VBR	Variable Bit Rate
VC	Virtual Channel
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier

Appendix A – Reed-Solomon Codec

The Reed-Solomon codes represent a specific instance of the BCH codes. These codes are generated on the non-binary Galois fields $GF(2^m)$ and have a specified word length of $2^m - 1$ (n) symbols with 2^m distinct symbols existing. Each symbol may be seen as representing m bits of data. Of the n symbols transmitted in a word, some represent actual data (k) and some represent coding overhead ($n-k$). If $(n-k)$ symbols of overhead are included in the word, then the code may correct $(n-k)/2$ symbol errors (t). The code representation is thus a (n, k, t) . The encoder may also operate in erasure recovery mode where the positions of the errors are given and may correct fully $2t$ erasures.

The information presented below is taken from [7][2][13] and is intended to introduce the topic of Reed-Solomon coding and illustrate some of the properties of the codes.

Before examining the action of the Reed-Solomon code in terms of encoding and decoding, it is necessary to explore the topic of finite or Galois fields. Thereafter, the encoding and decoding procedures will be described.

Basic Field Theory

A field is defined as a set that adheres to the following properties:

- Two operations are defined on the set, addition (+) and multiplication (\cdot).

The set is closed under addition and multiplication ($\forall(a,b) \in F^2, \exists(c,d) \in F^2$ such that $(a+b)=c$ & $(a \cdot b)=d$).

- The identity element exists for both operations. We shall call the additive identity element 0 and the multiplicative identity element 1 ($\forall a \in F, (a + 0) = a$ & $(a \cdot 1) = 1$).
- Inverse elements exist for all elements of the set under both operations. We shall denote the additive inverse of an element a as $(-a)$ and we shall designate the multiplicative inverse as (a^{-1}) ($\forall a \in F, \exists((-a), a^{-1}) \in F$) such that $(a + (-a)) = 0$ & $(a \cdot a^{-1}) = 1$.
- The associative law applies. ($\forall(a,b,c) \in F^3, a + (b + c) = (a + b) + c$ & $a \cdot (b \cdot c) = (a \cdot b) \cdot c$).
- The commutative law applies. ($\forall(a,b) \in F^2, a + b = b + a$ & $a \cdot b = b \cdot a$).
- The distributive law applies. ($\forall(a,b,c) \in F^3, a \cdot (b + c) = a \cdot b + a \cdot c$).

The existence of inverse elements allows the introduction of the operations of subtraction (-) and division (/). Subtraction is defined as adding the additive inverse $(-(a) \equiv +(-a))$ and division is defined as multiplying by the multiplicative inverse

If the field has a finite set of distinct elements, it is called a finite field or Galois field. The number of distinct elements in the field is called the *order* of the field. A number of the properties of a general field F and finite field GF(q) are listed below without proof:

1. The order of a finite field must either be prime or the power of a prime.
2. $\forall a \in F, a \cdot 0 = 0 \cdot a = 0$.
3. $\forall (a,b) \in F^2, (a \neq 0) \ \& \ (b \neq 0) \Rightarrow a \cdot b \neq 0$.
4. $\forall (a,b) \in F^2, (a \cdot b = 0) \ \& \ (a \neq 0) \Rightarrow b = 0$.
5. $\forall (a,b) \in F^2, -(a \cdot b) = (-a) \cdot b = a \cdot (-b)$. $\forall (a,b,c) \in F^3, (a \neq 0) \ \& \ (a \cdot b = a \cdot c) \Rightarrow b = c$.
6. $\exists k \in Z$ such that

$$\sum_{i=1}^k 1 = 0$$

the smallest positive integer λ such that this is the case is defined as the *characteristic* of the code and is always prime.

7. $\forall a \in F; a \neq 0, \exists n \in Z$ such that $a^n = 1$. The smallest positive value of n for which this holds is termed the order of the element a.
8. $\exists k \in F$, such that $\forall a \in F, \exists n \in Z$ such that $a = k^n$. We call this element k a *primitive element*.
9. From any given field GF(p) where p is prime, it is possible to construct a field with p^m elements (this field is known as an extension field and denoted GF(p^m)).
10. $\forall a \in GF(q); a \neq 0 \Rightarrow a^{q-1} = 1$ where q is the order of the field.
11. $\forall a \in GF(q); a \neq 0 \Rightarrow (q-1) \text{MOD}(\text{order}(a)) = 0$.

Generation of the Galois Field

We know that it is possible to generate an extension field from the GF(2) of order 2^m . The process will be described here.

Before exploring the generation of the Galois field GF(2^m) from GF(2), it is necessary to formalize the use of polynomial notation in this setting and view some properties of polynomials on GF(2).

Polynomial notation

The notation used to represent polynomials with coefficients on GF(2) follows the standard polynomial naming convention.

$$f(X) = f_0 + f_1X + f_2X^2 + \dots + f_nX^n$$

All coefficients are elements of GF(2), i.e. $f_x \in \text{GF}(2)$, $\forall x \in [0,n]$.

X is the *variable* associated with the polynomial.

The degree of the polynomial is the largest power of X with a non-zero coefficient.

Some properties of polynomials on GF(2) are included below:

1. The commutative law applies:

$$a(X) + b(X) = b(X) + a(X)$$

$$a(X) \cdot b(X) = b(X) \cdot a(X)$$

2. The associative law applies:

$$a(X) + [b(X) + c(X)] = [a(X) + b(X)] + c(X)$$

$$a(X) \cdot [b(X) \cdot c(X)] = [a(X) \cdot b(X)] \cdot c(X)$$

3. The distributive law applies:

$$a(X) \cdot [b(X) + c(X)] = [a(X) \cdot b(X)] + [a(X) \cdot c(X)]$$

4. Euclid's division algorithm - when a polynomial $f(X)$ is divided by a non-zero polynomial $g(X)$, two unique polynomials are generated, $q(X)$ and $r(X)$ where $q(X)$ is the *quotient* and $r(X)$ is the *remainder*:

$$f(X) = q(X) \cdot g(X) + r(X).$$

5. Any irreducible polynomial over GF(2) of degree m divides $X^{2^m-1} + 1$ exactly.
6. An irreducible polynomial $p(X)$ is *primitive* if the smallest positive integer for which $p(X)$ is a factor of X^n+1 is $n=2^m-1$.
7. It can be shown that $[f(X)]^{2^i} = f(X^{2^i})$.

Extension of GF(2) to GF(2^m)

Begin with the two elements of GF(2), 0 and 1. Introduce a new symbol α . Introduce an operation of multiplication " \cdot " which allows the generation of the powers of α .

Therefore:

$$0 \cdot 0 = 0$$

$$0 \cdot 1 = 0$$

$$0 \cdot \alpha = 0$$

$$1 \cdot 1 = 1$$

$$1 \cdot \alpha = \alpha$$

$$\alpha \cdot \alpha = \alpha^2$$

$$\alpha \cdot \alpha \cdot \alpha = \alpha^3$$

.

.

.

$$\alpha \dots \alpha \cdot \alpha \cdot \alpha = \alpha^j$$

We may deduce from the laws of multiplication that the following hold:

$$0 \cdot \alpha^j = \alpha^j \cdot 0 = 0$$

$$1 \cdot \alpha^j = \alpha^j \cdot 1 = \alpha^j$$

$$\alpha^i \cdot \alpha^j = \alpha^j \cdot \alpha^i = \alpha^{i+j}$$

Introduce a set of elements upon which the operation of multiplication is defined:

$$F = \{0, 1, \alpha, \alpha^2, \alpha^3, \dots, \alpha^j, \dots\}$$

We now place constraints on the element α for the operation "." such that:

- i. F is closed under multiplication.
- ii. F contains only 2^m distinct elements.

Assume that α is a root of a primitive polynomial $p(X)$ of degree m over $\text{GF}(2)$, $p(\alpha) = 0$.

We know that $p(X)$ divides $X^{2^m-1} + 1$. This implies that:

$\exists q(X)$ over $\text{GF}(2)$, such that:

$$X^{2^m-1} + 1 = q(X) \cdot p(X)$$

Substituting α for X , we find:

$$\alpha^{2^m-1} + 1 = q(\alpha).p(\alpha) = q(\alpha).0 = 0$$

Hence,

$$\begin{aligned}\alpha^{2^m-1} + 1 &= 0 \\ \alpha^{2^m-1} &= 1\end{aligned}$$

This means that under the condition that $p(\alpha) = 0$, the set of F becomes finite and contains only the 2^m elements:

$$F^* = \{0, 1, \alpha, \alpha^2, \dots, \alpha^{2^m-2}\}$$

It can easily be seen that the non-zero elements of F^* form a group under multiplication.

To extend F^* to a field, the addition operation must also be introduced. We will use the standard notation “+” to reference the addition operation in this context. If the addition operation can be introduced such that it forms a commutative group over F^* then F^* will be a non-binary finite or Galois field with 2^m elements.

For $0 \leq i < 2^m-1$, we may divide X^i by $p(X)$ and obtain the following:

$$X^i = q_i(X)p(X) + a_i(X)$$

$q_i(X)$ is the quotient and $a_i(X)$ the remainder. The remainder is a polynomial over $GF(2)$ of degree $\leq m-1$ and may be expressed as follows:

$$a_i(X) = a_{i0} + a_{i1}X + a_{i2}X^2 + \dots + a_{i(m-1)}X^{m-1}$$

X and $p(X)$ are relatively prime so:

$$\forall i > 0, a_i \neq 0$$

It may also be demonstrated that::

$$0 \leq i, j \leq 2^m - 1 \text{ and } i \neq j \Rightarrow a_i(X) \neq a_j(X)$$

Since we know that $p(\alpha) = 0$, we may express α^i as follows by substituting α for X :

$$\alpha^i = q_i(\alpha) \cdot 0 + a_i(\alpha) = a_{i0} + a_{i1}\alpha + a_{i2}\alpha^2 + \dots + a_{i(m-1)}\alpha^{m-1}$$

The $2^m - 1$ non-zero elements $\alpha^0, \alpha^1, \dots, \alpha^{2^m-1}$ in F^* are represented by 2^{m-1} distinct nonzero polynomials of α over $GF(2)$ with degree $m-1$ or less. The zero element may be represented by the zero polynomial.

The addition operation “+” may be defined as follows:

$$0 + 0 = 0$$

and for $0 \leq i, j < 2^m - 1$,

$$\begin{aligned} 0 + \alpha^i &= \alpha^i + 0 = \alpha^i \\ \alpha^i + \alpha^j &= (a_{i0} + a_{i1}\alpha + a_{i2}\alpha^2 + \dots + a_{i,m-1}\alpha^{m-1}) + (a_{j0} + a_{j1}\alpha + a_{j2}\alpha^2 + \dots + a_{j,m-1}\alpha^{m-1}) \\ &= (a_{i0} + a_{j0}) + (a_{i1}\alpha + a_{j1}\alpha) + (a_{i2}\alpha^2 + a_{j2}\alpha^2) + \dots + (a_{i,m-1} + a_{j,m-1})\alpha^{m-1} \end{aligned}$$

if $i=j$, clearly, $\alpha^i + \alpha^j = 0$.

The set F^* is commutative group under the operation of addition or “+”. It may also be noted that the multiplication on F^* is distributive over addition on F^* and that the set $F^* = \{0, 1, \alpha, \dots, \alpha^{2^m-2}\}$ is a Galois field of 2^m elements or $GF(2^m)$.

Properties of the Galois Field $GF(2^m)$

The following are properties of the extended Galois field $GF(2^m)$:

- Let $f(X)$ be a polynomial with coefficients from $GF(2)$. Let β be an element of an extension field of $GF(2)$. If β is a root of $f(X)$, then for any $k \geq 0$, β^{2^k} is also a root of $f(X)$.
- The $2^m - 1$ nonzero elements of $GF(2^m)$ form all the roots of $X^{2^m-1} + 1$.

-
- A minimal polynomial $\phi(X)$ of β is defined as the polynomial with smallest degree over $\text{GF}(2)$ such that $\phi(\beta) = 0$, where $\beta \in \text{GF}(2^m)$. The minimal polynomial of a field element β is irreducible.
 - Let $f(X)$ be a polynomial over $\text{GF}(2)$. Let $\phi(X)$ be the minimal polynomial of a field element β . If β is a root of $f(X)$, then $f(X)$ is divisible by $\phi(X)$.
 - The minimal polynomial $\phi(X)$ of an element β in $\text{GF}(2^m)$ divides $X^{2^m} + X$.
 - Let β be an element in $\text{GF}(2^m)$ and let e be the smallest non-negative integer such that $\beta^{2^e} = \beta$. Then

$$\bullet \quad f(X) = \prod_{i=0}^{e-1} (X + \beta^{2^i})$$

- is an irreducible polynomial over $\text{GF}(2)$.
- Let $\phi(X)$ be the minimal polynomial of an element β in $\text{GF}(2^m)$. Let e be the smallest integer such that $\beta^{2^e} = \beta$. Then

$$\bullet \quad \phi(X) = \prod_{i=0}^{e-1} (X + \beta^{2^i})$$

- Let $\phi(X)$ be the minimal polynomial of an element β in $\text{GF}(2^m)$. Let e be the degree of $\phi(X)$. Then e is the smallest integer such that $\beta^{2^e} = \beta$. Also, $e \leq m$.
- If β is a primitive element of $\text{GF}(2^m)$, all its conjugates $\beta^2, \beta^{2^2}, \dots$ are primitive elements of $\text{GF}(2^m)$.

Reed-Solomon Encoding Procedure

We will assume a set notation for various aspects of the Reed-Solomon Codes. This notation is documented in [x].

Table AA-1 : Notation used in illustrating the Reed-Solomon Encoding Procedure.

n	Total number of symbols in RS word
k	Number of data symbols in RS word
t	Number of correctable symbols
m	Order of the Galois field (ie GF(2 ^m))
d(x)	raw information polynomial
p(x)	parity polynomial
c(x)	codeword polynomial
g(x)	generator polynomial
q(x)	quotient polynomial
r(x)	remainder polynomial

The code word polynomial (c(x)) will be broken down into parity(p(x)) and information (d(x)) segments.

$$\begin{aligned}
 c(x) &= c_{n-1}x^{n-1} + c_{n-2}x^{n-2} + \dots + c_1x^1 + c_0x^0. \\
 d(x) &= c_{n-1}x^{n-1} + c_{n-2}x^{n-2} + \dots + c_{2t+1}x^{2t+1} + c_{2t}x^{2t}. \\
 p(x) &= c_{2t-1}x^{2t-1} + c_{2t-2}x^{2t-2} + \dots + c_1x^1 + c_0x^0.
 \end{aligned}$$

Clearly,

$$c(x) = d(x) + p(x).$$

A vector of n elements is a RS codeword if and only if the polynomial it represents is a multiple of the generator polynomial g(x). This generator polynomial is of the form:

$$g(x) = (x+\alpha)(x+\alpha^2)\dots(x+\alpha^{2t}).$$

One means of deriving the parity polynomial is by dividing the codeword polynomial by the generator polynomial and then observing the value of the remainder:

$$d(x) = g(x)q(x) + r(x)$$

The codeword polynomial will then be expressed as:

$$c(x) = p(x) + g(x)q(x) + r(x).$$

By setting the parity polynomial's coefficients equal to the negatives of the coefficients of $r(x)$, we generate find that $c(x)$ becomes:

$$c(x) = g(x)q(x)$$

and is thus a multiple of $g(x)$.

As with hardware implementations on $GF(2)$, a shift register implementation may be used to perform the coding operation.. Figure AA-1 illustrates the encoding procedure using a shift registers. The X 's represent multiplication of a pair of m -bit numbers on $GF(2^m)$ and the $+$ operations are X-OR of 2 m -bit numbers.

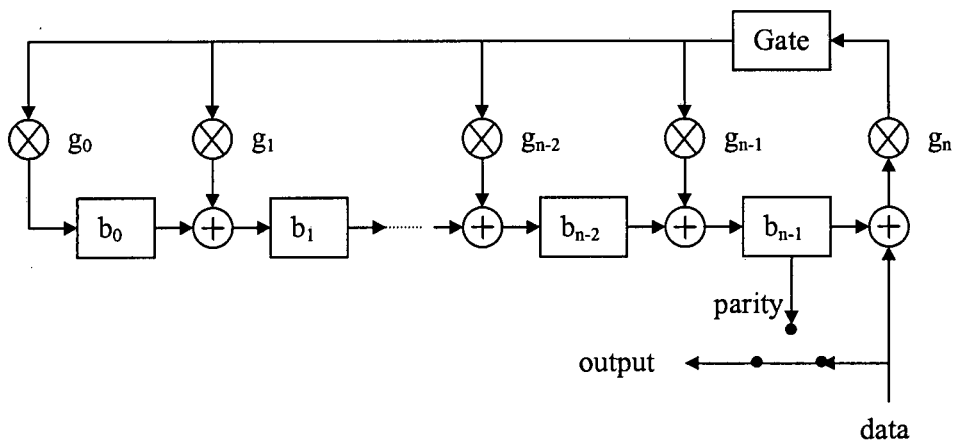


Figure AA-1 :Reed-Solomon Shift Register Based Encoder

Reed-Solomon Decoding Procedure

Principles of Operation

In addition to the polynomials defined in the previous section, the following are defined or redefined and will be used with respect to the decoding operation:

Table AA-2 : Additional Notation for Discussion

$e(x)$	Error polynomial
$r(x)$	Now refers to the received word.

In order to illustrate the process of decoding a Reed-Solomon code, assume that a transmitted word $r(x)$ is received by the decoding entity:

$$r(x) = r_{n-1}x^{n-1} + r_{n-2}x^{n-2} + \dots + r_1x^1 + r_0x^0.$$

Equation AA-1

This received code word consists of the original codeword $c(x)$:

$$c(x) = c_{n-1}x^{n-1} + c_{n-2}x^{n-2} + \dots + c_1x^1 + c_0x^0.$$

Equation AA-2

With the addition of an error sequence $e(x)$:

$$e(x) = e_{n-1}x^{n-1} + e_{n-2}x^{n-2} + \dots + e_1x^1 + e_0x^0.$$

Equation AA-3

The error sequence is defined as the difference between the received sequence and the original sequence.

$$e(x) = r(x) - c(x).$$

Equation AA-4

For the code, a set of $2t$ *partial syndromes* S_i are defined where $i \in [1, 2t]$ and:

$$S_i = r(\alpha^i)$$

Equation AA-5

Since $\alpha^1, \alpha^2, \dots, \alpha^{2t}$ are roots $c(x)$:

$$c(\alpha^1) = c(\alpha^2) = \dots = c(\alpha^{2t}) = 0.$$

Equation AA-6

We may thus deduce that:

$$r(\alpha^i) = c(\alpha^i) + e(\alpha^i) = e(\alpha^i) = S_i.$$

Equation AA-7

Clearly therefore, the partial syndrome is a function of the error sequence received purely and is independent of the original data sequence.

Assuming the transmitted word contains k errored symbols at locations $x^{j_1}, x^{j_2}, \dots, x^{j_k}$ and that ($j_1 < j_2 < \dots < j_k$).

$$e(x) = e_{j_1}x^{j_1} + e_{j_2}x^{j_2} + \dots + e_{j_k}x^{j_k}.$$

Equation AA-8

Now define a set of $2t$ error locator numbers $\beta_i = \alpha^{j_i}$, $i \in [1, k]$.

$$\begin{aligned} S_1 &= e_{j_1}\beta_1 + e_{j_2}\beta_2 + \dots + e_{j_k}\beta_k \\ S_2 &= e_{j_1}\beta_1^2 + e_{j_2}\beta_2^2 + \dots + e_{j_k}\beta_k^2 \\ &\dots\dots\dots \\ S_{2t} &= e_{j_1}\beta_1^{2t} + e_{j_2}\beta_2^{2t} + \dots + e_{j_k}\beta_k^{2t} \end{aligned}$$

Equation AA-9

The process of decoding a RS word is logically equivalent to solving the above set of equations.

The decoding process for a Reed-Solomon code word may be broken down into 5 separate procedures:

- The calculation of the $(2t)$ partial syndromes.
- The Berlekamp-Massey algorithm to generate the error location polynomial $\sigma(x)$.
- The Chien search algorithm to calculate the specific error locations from the error locator polynomial.

- Calculation of the magnitude of the error at each location indicated as errored.
- Correction of up to t errors given the error locations and magnitudes.

Partial Syndrome Calculation

Classically with cyclic codes, the syndrome is defined as the remainder when the received codeword ($r(x)$) is divided by the generator polynomial. For the case of the Reed-Solomon decoding process, *partial syndromes* are used. A partial syndrome S_i is defined as the remainder when the received codeword is divided by i^{th} factor of the generator polynomial $g(x)$, namely $(x + \alpha^i)$.

So,

$$S_i = \text{rem} \left[\frac{r(x)}{x + \alpha^i} \right], i = 1, 2, \dots, 2t$$

Equation AA-10

It can be shown that the division operation to obtain the remainder when the received word is divided by the factor relating to the factor $(x + \alpha^i)$ is analogous to evaluating $r(\alpha^i)$. The reasoning is as follows:

By the definition of the division operation, the remained term must have a lower order than the divisor. In this case, the divisor has order 1 – the i^{th} term is $(x + \alpha^i)$. This implies that the remainder must be order zero, or a single element of the field $\text{GF}(2^m)$.

We now observe that the division operation may be expressed in terms of the divisor ($r(x)$), quotient ($q(x)$), dividend $(x + \alpha^i)$ and remainder r , as:

$$r(x) = q(x) \cdot (x + \alpha^i) + r$$

Equation AA-11

When $x = \alpha^i$, $(x + \alpha^i) = 0$ and hence

$$r(\alpha^i) = r = S_i$$

Equation AA-12

It is therefore clear that the division algorithm is not required to generate the partial syndromes, single enumerations of the received polynomials are sufficient.

So,

$$r(\alpha^i) = r_0 + r_1\alpha^i + r_2\alpha^{2i} + \dots + r_{n-1}\alpha^{(n-1)i}$$

Equation AA-13

For computational purposes, this may be re-written as follows:

$$r(\alpha^i) = (\dots((r_{n-1}\alpha^i + r_{n-2})\alpha^i + r_{n-3})\alpha^i + \dots)\alpha^i + r_0$$

Equation AA-14

Error Locator Polynomial Generation

As stated earlier, the operation of the Reed-Solomon involves the solution of the $2t$ equations relating the computed syndromes to the error locations and magnitudes stated in the introduction to this section.

We now introduce a new polynomial referred to as the error locator polynomial:

$$\sigma(x) = (1 + \beta_1x)(1 + \beta_2x) \dots (1 + \beta_kx) = \sigma_0 + \sigma_1x + \dots + \sigma_kx^k$$

Equation AA-15

The roots of the error locator polynomial are the inverses of the error locator numbers. The coefficients of $\sigma(x)$ and the error location numbers (β_i where $i \in [1, k]$) are linked by the following series of equations derived by multiplying out the above formula:

$$\begin{aligned} \sigma_0 &= 1 \\ \sigma_1 &= \beta_1 + \beta_2 + \dots + \beta_k \\ \sigma_2 &= \beta_1\beta_2 + \beta_1\beta_3 + \dots + \beta_{k-1}\beta_k \\ &\dots\dots\dots \\ \sigma_k &= \beta_1\beta_2\dots\beta_k \end{aligned}$$

Equation AA-16

The unknowns of σ_i and β_i may be further related using Newton’s identities as follows:

$$\begin{aligned}
 S_1 + \sigma_1 &= 0 \\
 S_2 + S_1\sigma_1 + 2\sigma_2 &= 0 \\
 S_3 + S_2\sigma_1 + S_2\sigma_1 + 2\sigma_2 &= 0 \\
 &\dots\dots\dots \\
 S_k + S_{k-1}\sigma_1 + \dots + S_2\sigma_{k-2} + S_1\sigma_{k-1} + k\sigma_2 &= 0
 \end{aligned}$$

Equation AA-17

Berlekamp’s Iterative Algorithm to Calculate the Error Locator Polynomial $\sigma(X)$

The first step of the algorithm to compute the error locator polynomial is to find a minimum-degree polynomial $\sigma_1(X)$ to satisfy the first of the Newton’s identities listed in Equation AA-17. The coefficients must then be tested against the second identity. If the coefficients of $\sigma(X)$ satisfy the second identity, then we set $\sigma^{(2)}(X) = \sigma^{(1)}(X)$, otherwise a correction term is added to $\sigma^{(1)}(X)$ to form $\sigma^{(2)}(X)$. This correction factor must be chosen so that $\sigma^{(2)}(X)$ has minimum degree and its coefficients satisfy the second identity of Equation AA-17. The same operation is repeated until $\sigma^{(2i)}(X)$ is generated for each of $\sigma^{(i)}(X)$, for $i=3, \dots, 2t$.

$\sigma^{(2i)}(X)$ is taken to be the error-location polynomial $\sigma(X)$ and will yield an error pattern $e(X)$ of minimum weights that satisfy Equation AA-9. If the number of errors received in $r(X)$ is t or less, then the error sequence generated by $\sigma(X)$ is the true error pattern.

The physical calculation procedure for $\sigma(X)$ is as follows:

Let:

$$\sigma^{(\mu)}(X) = 1 + \sigma_1^{(\mu)}(X) + \sigma_2^{(\mu)}(X) + \dots + \sigma_{l_\mu}^{(\mu)}(X)$$

Equation AA-18

be a polynomial of minimal weight computed at the μ^{th} step of the iterative procedure that satisfies the first μ identities of Equation AA-17. To compute the next iteration in the series, $\sigma^{(\mu+1)}(X)$, we calculate the μ^{th} discrepancy or d_μ as follows:

$$d_\mu = S_{\mu+1} + \sigma_1^{(\mu)}S_\mu + \sigma_2^{(\mu)}S_{\mu-1} + \dots + \sigma_{l_\mu}^{(\mu)}S_{\mu+1-l_\mu}$$

Equation AA-19

If $d_\mu = 0$, the coefficients of $\sigma^{(\mu)}(X)$ satisfy the $(\mu+1)^{\text{th}}$ Newton's identity. If this is the case, then we may set:

$$\sigma^{(\mu+1)}(X) = \sigma^{(\mu)}(X)$$

Equation AA-20

If $d_\mu \neq 0$, then a correction factor must be added to $\sigma^{(\mu)}(X)$ to make $\sigma^{(\mu+1)}(X)$ satisfy the $(\mu+1)^{\text{th}}$ Newton's Identity. To make this correction, we must go back to the steps prior to the μ^{th} step and determine a polynomial $\sigma^{(\rho)}(X)$ such that the ρ^{th} discrepancy $d_\rho \neq 0$ and $\rho - l_\rho$ (where l_ρ is the degree of $\sigma^\rho(X)$) has the largest value. Then:

$$\sigma^{(\mu+1)}(X) = \sigma^{(\mu)}(X) + d_\mu d_\rho^{-1} X^{(\mu-\rho)} \sigma^{(\rho)}(X)$$

Equation AA-21

$\sigma^{(\mu+1)}(X)$ is the minimum degree polynomial whose coefficients satisfy the first $\mu+1$ Newton identities.

The iterative procedure is performed by filling out the following table:

Table AA-3 : Berlekamp's Iterative Method

μ	$\sigma^{(\mu)}(X)$	d_μ	l_μ	$\mu - l_\mu$
-1	1	1	0	-1
0	1	S_1	0	0
1				
...				
2t				

l_μ is the degree of $\sigma^{(\mu)}(X)$.

To compute the $\mu+1^{\text{th}}$ row from the μ^{th} row, the following steps are taken:

1. If $d_\mu = 0$, then $\sigma_{\mu+1}^{(\mu+1)}(X) = \sigma^{(\mu)}(X)$ and $l_{\mu+1} = l_\mu$.
2. If $d_\mu \neq 0$, find another row ρ prior to the μ^{th} row such that $d_\rho \neq 0$ and the number $\rho - l_\rho$ in the last column in the table has the largest value. Then $\sigma^{(\mu+1)}(X)$ is given by Equation AA-21 and

$$l_{\mu+1} = \max(l_\mu, l_\rho + \mu - \rho)$$

Equation AA-22

For both the cases of 1. and 2.,

$$d_{\mu+1} = S_{\mu+2} + \sigma_1^{(\mu+1)} S_{\mu+1} + \sigma_2^{(\mu+1)} S_\mu + \dots + \sigma_\mu^{(\mu)} S_{\mu+2-l(\mu+1)}$$

Equation AA-23

When the table is completely entered, $\sigma^{(2t)}(X)$ in the last row yields the required $\sigma(X)$. If this polynomial has degree greater than t , then there are more than t errors, and they cannot, in general, be recovered.

Finding the Error Locations and Magnitudes.

The last stage of the Reed-Solomon decoding procedure involves finding the error-location numbers that are the reciprocals of the roots of $\sigma(X)$.

The roots of $\sigma(X)$ may be found by a simple substitution procedure. The values $1, \alpha, \alpha^2, \alpha^3, \dots, \alpha^{n-1}$ are substituted into $\sigma(X)$. Clearly k is a root of $\sigma(X)$ if $\sigma(k) = 0$.

Let:

$$Z(X) = 1 + (S_1 + \sigma_1)X + (S_2 + \sigma_1 S_1 + \sigma_2)X^2 + \dots + (S_v + \sigma_1 S_{v-1} + \sigma_2 S_{v-2} + \dots + \sigma_v)X^v$$

Equation AA-24

The error value at location $\beta_i = \alpha^{ji}$ is given by:

$$e_{j_i} = \frac{Z(\beta_i^{-1})}{\prod_{i=1; i \neq j}^v (1 + \beta_i \beta_i^{-1})}$$

Equation AA-25

With the known error locations (β_i) and the known error values (e_{j_i}), the corrected code word may be recovered. The corrected code word is:

$$g(X) = r(X) - e(X)$$

Reed-Solomon Code Properties

The Reed-Solomon code used for the implementations was the (255,239,8) code. This choice was based on arguments proposed by Cain and MacGregor in [25]. The basic code was shortened to yield other codes, namely (232,216,8) and (73,57,8). As stated previously the code operates on the Galois field $GF(2^8)$ which implies 8 bit symbols. The code is able to correct 8 random symbol errors in a 255 symbol code word with the addition of 16 bytes of coding overhead.

The concept of minimum distance is used in the discussion of block codes. This is defined as the minimum number of elements by which two code words may differ. In the case of binary codes, this refers to the minimum hamming distance between two code words. In the case of non-binary codes, such as the Reed-Solomon code used here, the measure is applied to the number of symbols differing between the code words.

The Reed-Solomon codes achieve the greatest free distance for any block code, namely:

$$d_{\min} = 2e+1$$

where e is the number of symbols that may be corrected. In the case of the code chosen, this free distance is 17.

To conceptualize the block code decoding procedure, [13] presents a useful concept of coding space. In the following figure, a code word is represented by a point in the “coding space”.

The distance separating points references the symbol distance between two code words.

In the space there are $(2^m)^n$ words of which $(2^m)^k$ are valid code words. If the received code word contains no more than t errored symbols, it lies within the decoding sphere of the correct code word. If more than t errors are present in the decoded symbol, then error recovery will not be possible. Two possibilities may occur in this case, namely the decoded word does not fall within the decoding sphere of another legitimate code word, in which case the decoder is aware of its inability to correct transmitted errors, or the received word lies within the decoding sphere of another code word (in which case the decoder incorrectly interprets the received word as another legitimate code word and additional errors may be introduced).

Schematically the code space analogy may be visualised as follows:

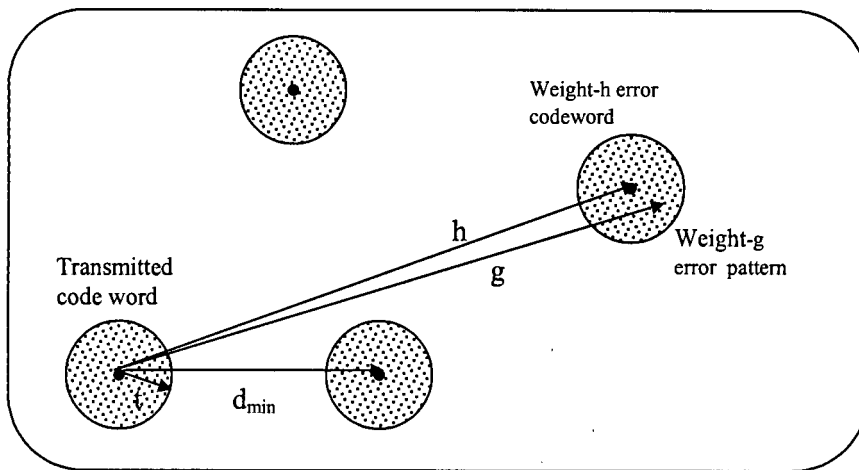


Figure AA-2: Code Space Representation of Decoding Procedure

In order to predict the behaviour of the RS codec, the decoder failure probabilities must be determined for any given nominal symbol error rate and code rates (232,216,8) and (73,57,8).

For the calculations that follow, assume the following:

p_{be} = probability of a single bit error

p_{se} = probability of a symbol error = $1 - (1 - p_{be})^8$

p_{we} = probability of a word error

p_{lwe} = probability that word is correctly decoded = $(1 - p_{we})$

The calculations that follow in 0 assume that bit errors are identically and independently distributed and that the bit error rate does not change significantly during a single code word. The case of burst errors will be considered later.

Probability of Decoder Failure

The probability that a code word is correctly decoded is equal to the probability that less than e symbols are errored in the transmission process.

This may be found to be equal to:

$$P_{we} = (1 - p_{we}) = \sum_{i=0}^e \binom{n}{i} (1 - p_{se})^{n-i} (p_{se})^i$$

Equation AA-26

Probability of Faulty Correction Procedure

The derivation of the probability of a block code with a given minimum free distance being interpreted as a code-word other than that transmitted is given in [23].

P_{ICD} , the probability of incorrectly decoding an RS code word may be shown to be the following:

$$P_{ICD} = \left[\sum_{h=d}^n \left[\binom{n}{h} (q^{m-1}) \sum_{j=0}^{h-d} (-1)^j \binom{h-1}{j} (q^m)^{h-d-j} \right] \sum_{s=0}^t \sum_{g=h-s}^{h+s} \left\{ \begin{array}{l} \sum_{z=z_{\min}}^{z_{\max}} \binom{h}{h-s+z} \binom{s-z}{g-h+s-2z} \\ \binom{n-h}{z} (2^m - 2)^{g-h+s-2z} (2^{m-1})^z \\ \frac{1}{(2^m - 1)^g} [1 - (1 - p_b)^m]^g [(1 - p_b)^m]^{n-g} \end{array} \right\} \right]$$

Equation AA-27

In the above equation:

- $z_{\min} = \max\{0, g - h\}$
- $z_{\max} = \frac{1}{2}(g - h + s)$

Appendix B: Convolution Codes

Since their inception in 1955, the convolution codes have found many applications in high noise environments, with particular emphasis on satellite and deep space communication systems. The codes are particularly robust in channels with high levels of random, uncorrelated bit errors.

Encoding

The code stream is generated by continuously shifting M bits into a shift register memory element. The depth of the shift register memory element is referred to as the constraint length (K) of the code. Output bits are generated from a set of N generator polynomials, where the contents of the SR are logically ANDed with the polynomials and the resulting bits XORed together. In this way a code of rate M/N is generated.

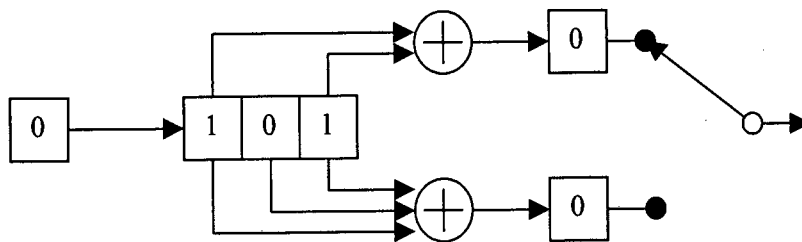


Figure AB-1 : Convolution Code Operation Procedure

Figure AB-1 illustrates the operation of a simple rate $1/2$ convolution encoder where the generator polynomials are 111 and 101 (binary). The number of bits in the shift register yields the *constraint length* k of the encoder. Often another definition of the constraint length of the decoder is used. Constraint length is also sometimes defined as the base 2 logarithm of the number of states in the decoder and designated as v .

Decoding

A number of decoding methods are available and include sequential decoding, threshold decoding and maximum likelihood decoding (as used by the Viterbi decoding algorithm). The Viterbi algorithm is the most popular of the decoding schemes and is documented below.

The key to understanding the operation of the convolution coder is to view the device as a state machine. The state to state transitions are determined not only by the M symbols shifted into the coder, but also by the previous bits shifted into the memory array. A means of observing this is by viewing the tree for the code (see figure 1.0). The figure shows the output of the device ascertained by the current state of the shift register and the data bit processed. From the diagram it is clear that there are only in essence 4 states, although 8 possible values of the shift register are present. The bit immediately shifted out of the register does not impact on the state transition. An example of this is examining the cases where the shift register holds 010 and 110. The action of the coder is identical for these cases.

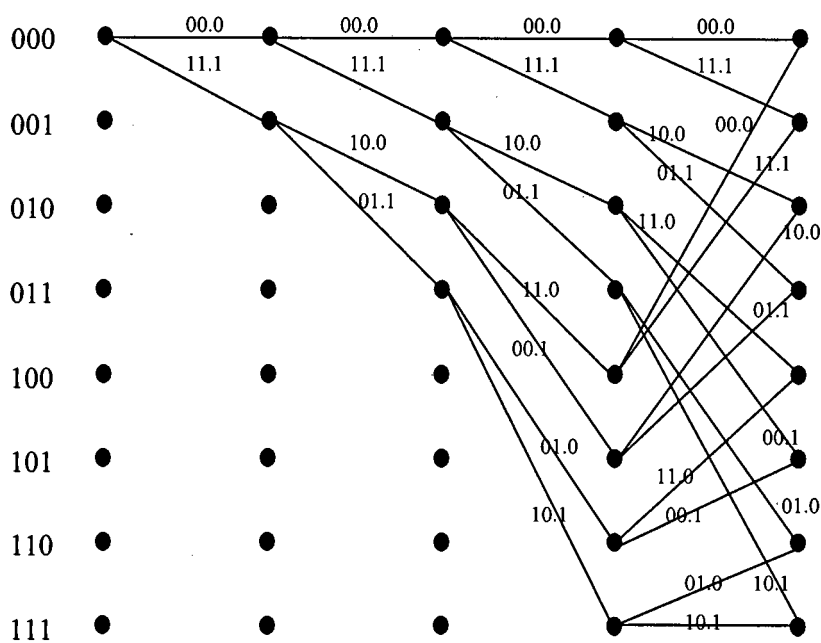


Figure AB-2: Trellis Diagram for Convolution Code

By noting the repetitive nature of the tree diagram, one may generate the state table for the coder. This is depicted in Figure AB-3.

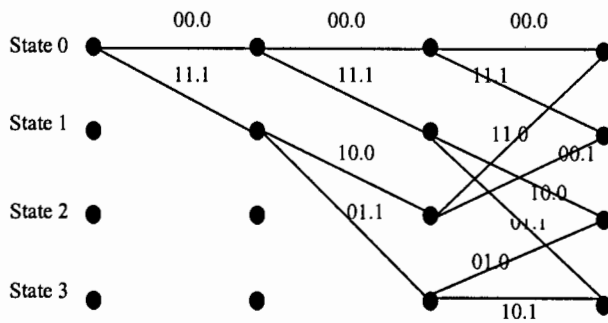


Figure AB-3 : Collapsed State Diagram

The Viterbi decoding algorithm works on a shortest path routine. The decoded data stream is the physically realizable stream through the trellis that deviates from the received code stream by the least amount. Level of deviation is determined by a hamming distance function.

Consider the following process. A column labeled PD holds the initiating state and accumulated hamming distance to that point. The point separates the indicator for previous state from the net hamming distance. A column labeled CD holds the code segment that was used in the transition from the state referred to in the PD column to the current state and the associated data bit. The first two elements of CD are the code segment while the last segment is the data bit that would have been shifted into the shift register to move into the current state from the previous state.

Table AB-1 shows the state of the decoder after the code sequence 010011 has been moved into the coder and the results sent to the decoder. This assumes that the memory block held no entries before this segment was shifted in. This means a default initiating state of 0. By observing the state diagram of the encoder, the encoded stream will be : 00 11 10 11 11 01. Accumulated distance is determined by comparing for each state the received code segment (pair of bits) with the possible leaving segments. The final path into a state will be from that state which offers the shortest total path length.

Table AB-1 : Illustrative State Table

	1		2		3		4		5		6	
State	PD	CD	PD	CD	PD	CD	PD	CD	PD	CD	PD	CD
0	0.0	00.0	0.2	00.0	2.2	11.0	2.0	11.0	0.2	00.0	0.3	00.0
1	0.2	11.1	0.0	11.1	2.2	00.1	0.2	11.1	0.0	11.1	0.3	11.1
2	/	/	1.1	01.0	1.0	10.0	1.3	10.0	1.3	10.0	1.2	10.0
3	/	/	1.1	10.1	1.2	01.1	1.3	01.1	1.3	01.1	1.0	01.1

When the memory buffer is full and a new symbol is received, the coder will use a trace back algorithm to find the initiating element that lies on the path through the trellis with the lowest terminal hamming distance. In the above case, the terminal state with the lowest accumulated distance is state 3. Tracing back one can reach the conclusion that the initiating state was state 0 and the corresponding data bit that would be written out is a 0. It can be seen that states lying on the shortest path correspond to the correct data sequence.

The polynomials used in the coding scheme are chosen so that the hamming distances out of a state have as large a hamming distance from one another as possible. The intention is that in noisy environments the coder will converge on the correct path, despite the presence of bit errors.

Distance Properties of Codes Used in Simulations

Like the block codes, convolution codes use the distance property to describe the performance of the code.

Since the convolution codes are linear, one may consider the all zero sequence and infer the performance of other transmitted sequences. Assuming the all zero sequence is transmitted, the *minimum free distance* d_{\min} is defined as the smallest weight of any non-zero transmitted sequence. Since the convolution code is linear, any results generated for the all zero data sequence are applicable to other sequences.

The minimum free distance for the rate $\frac{1}{2}$ with constraint length 7 and coding polynomials (octal: 371,247) is 10.

The minimum free distance for the rate $\frac{1}{3}$ with constraint length 7 and coding polynomials (octal: 367,331,225) is 15.

Appendix C: Description of 32 bit Cyclic Redundancy Check

Description of Action

For the discussion of the operation of the 32bit CRC, assume the following notation:

Table AC-1 : CRC Notation

$c(x)$	Codeword polynomial that is to be encoded.
$d(x)$	Data segment (n bits long)
$q(x)$	Quotient polynomial.
$r(x)$	Remainder of division operation
$p(x)$	Dividend or code polynomial

The above polynomials are on the binary field $GF(2)$ and all operations are hence defined as the binary operations on $GF(2)$.

The word that is sent with a CRC32 check consists of an arbitrary number, n bits of data with 32 bits of parity information appended. This forms a $(n+32,n)$ code. The data segment of the code is transmitted un-adjusted, and the 32bit CRC is then appended to the end. A code word is valid when the remainder when the polynomial representing the word divided by the generator polynomial is zero.

$$c(x) = q(x).p(x)$$

To generate a valid codeword from an arbitrary data segment $d(x)$, we must pick the remainder such that:

$$c(x) = d(x).h(x) + r(x) = q(x).p(x)$$

In this case, $h(x)$ is x^{32} . We can now see that by the properties of $GF(2)$:

$$d(x).h(x) = q(x).p(x) + r(x)$$

In both the CRC application and check procedures used in the simulation platform, a look up table is used to represent the change in state of a shift register given an input sequence of 1 byte. The look-up table thus holds 256 entries and there is one look-up operation per byte of data sent. The 32bit CRC polynomial used by the application is: 04c11db7 (expressed in hexadecimal).

CRC32 Code Properties

The discussion on the properties of CRC's is based in principle on information supplied in [30]. The following notation will be used in the discussion that follows:

P_{ud} - probability of an undetected error in a protected word.

R - number of parity digits associated with the code.

p - bit error probability for each bit.

N - length of the protected code word.

$g(x)$ - generator polynomial for the code.

With a CRC code, the native unshortened code word length is $2^{R-1}-1$ bits. When operating with this length code word, the probability of an undetected error in the word does not exceed 2^{-R} regardless of the p value used in the generation of the received codeword.

This result does not unfortunately extend to shortened codes. For codes of length less than N the probability of undetected error may be expressed as follows:

$$P_{ud}(N, p) = 2^{-R} \sum_{i=0}^N B_i (1-2p)^i - (1-p)^N$$

B_i in this case is the number of weight i codewords generated by the parity check polynomial $h(x)$ where:

$$h(x) = \frac{(x^{2^{R-1}-1} - 1)}{g(x)}$$

The computation of the weights B_i may be calculated in a number of ways, but is beyond the scope of this project. For the sake of calculations in this thesis, 2^{-R} will be used as an estimate

on the P_{ud} . Should the scheme be seriously considered for implementation, this issue would have to be addressed and an accurate estimate for the error probability obtained.

Appendix D: Convolutional Interleaver to Improve Convolution Code Performance

When FEC coding is used in physical implementations, interleavers are often used to improve the coding gain by de-emphasizing the impact of burst errors on the codes. Convolution codes work well with random bit errors, but are adversely affected by burst errors. The function of the interleaver is to spread the transmitted errors over time so that they appear to the Viterbi decoder to be random bit errors. Two types of interleavers are used, block interleavers and convolutional interleavers. Emphasis is placed on the action of convolution interleavers since they operate naturally with convolution codes.

The reason the convolutional interleaver performs well with the convolution code is that like the code it operates on a data stream, rather than a data block. In this manner the introduction of the unnecessary latency to fill the contents of a block interleaver is avoided and the data is written out as it is received. Clearly some overhead in terms of data sent and latency is introduced in the process of applying the interleaver – at the beginning of a stream the buffer must be filled using the normal interleaving procedure before the initial stuffed bits which occupy the memory are flushed. At the end of a stream additional flushing bits must be passed into the interleaver to move out the required data.

Convolution Interleaving Procedure

The core of the convolution interleaver is a segment of memory, $n \times m$ bits wide. Operations on the memory consist of write operations into specific locations and a shift operation where the last row of the memory is discarded and the rest of the rows are shifted up. The information written to the channel is that contained in the last memory row.

The interleaving procedure commences as follows:

For an $m \times n$ memory, conceptually break the memory into n bit blocks. The i^{th} bit of the block is written into the $\{i, (i \bmod m)\}$ bit location.

The i^{th} output bit for the conceptual output block of n output bits is obtained from the $\{i, m\}$ memory location.

After the transmission of the n^{th} bit of the conceptual block, the memory block is shifted such that row (i) becomes row (i+1), row 1 contains no pertinent data and row m is discarded.

The following table illustrates the write-in order for a 8×4 block if the data sequence is (01010011):

Table AD-1 : Write-In Order for a 8×4 Block

	1	2	3	4	5	6	7	8
1	1-0	0	0	1	5-0	1	1	0
2	0	2-1	1	1	1	6-0	1	0
3	1	1	3-0	1	0	1	7-1	0
4	1	0	0	4-1	0	1	0	8-1

In the above case, the output sequence would be (10010101).

After the shift, the memory would look as follows:

Table AD-2 : Memory State After Shift

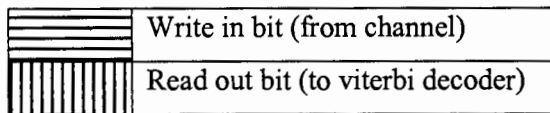
	1	2	3	4	5	6	7	8
1	X	X	X	X	X	X	X	X
2	0	0	0	1	0	1	1	0
3	0	1	1	1	1	0	1	0
4	1	1	0	1	0	1	1	0

Convolution De-Interleaving Procedure

The convolution de-interleaving procedure follows in a similar manner to the interleaving procedure, data is written into the bottom row of the interleaver memory block as it is received and is read from the memory block in the same order it was written in. To illustrate the de-interleaving procedure, consider the following data block:

Table AD-3 : Illustration of the De-Interleaving Procedure

	1	2	3	4	5	6	7	8
1	0	1	1	1	1	1	1	1
2	0	0	0	1	0	1	1	0
3	0	1	1	1	1	0	1	0
4	1	1	0	1	0	1	1	0



The data sequence that would have been read out of the memory block would be (11010011) and the data block written most recently into the codec would be (11010110).

Appendix E: Description of the Simulation Platform

The following is a description of the modules of the simulation platform:

`Bit_comp.cc` - Returns the number of bit errors introduced in the transmission process by comparing the input and output blocks.

`Cbr_gen.cc` - Generates the cell arrival times for a block of 64kb/s CBR voice traffic.

`Consts.cc` - Centralized list of the simulation parameter settings.

`Conv.cc` - Holds the functions for the convolution encode and Viterbi decoding operations.

`Conv_int.cc` - Applies the convolution interleaving and de-interleaving process.

`Crc_block.cc` - Holds the functions used to apply the CRC appending operation.

`Earqrec.cc` - Event processing segment for an ARQ arrival. Cells are copied into the input buffer from the channel buffer.

`Ecellarr.cc` - Event processing segment for the scheduled arrival of a cell. The next cell arrival is scheduled, the cell data is copied into the input buffer and if the RS encoder is not busy, the RS coding event is scheduled.

`echtrans.cc` - Event processing segment for the scheduled event of channel transmission including all the bit-centric functions including convolution interleaving and de-interleaving, convolution encoding and Viterbi decoding and error introduction.

`err_gen.cc` - Momentary bit error generation element for the indoor wireless channel.

`err_gen1.cc` - Momentary bit error generation element for the outdoor wireless channel.

`err_gen2.cc` - Momentary bit error generation element for the test channel with a swept bit error rate.

ersdec.cc - Event processing segment for the scheduled event of RS decoding. Decoded data is written to the output buffer.

ersenc.cc - Event processing segment for the scheduled event of RS encoding. The encoded data is copied into the input data stream buffer.

frst_pro.cc - Initialization segment that is operated at the beginning of the simulation process and never again.

global.cc - Holding area for global variables.

global.h - Header file included with global variables.

init_pro.cc - Initialization segment that is operated at the beginning of each simulation block.

next_ev.cc - An event triggering element called after each event schedule as a failsafe to schedule events that may have become due after the last operation. This avoids the possibility of lockup due to an event schedule being missed by full buffers or an active element.

priority.cc - Event scheduling priority queue functions.

proc_ele.cc - Processes a scheduled event (calls the correct event handling process).

reseq.cc - Re-sequences the data held in the output buffer before processing for statistics. This includes correcting the output times and in this way a real cell re-sequencer is emulated.

rs-code.cc - Holds the RS encode and decode functions written by Simon Adelaide.

rt_chng.cc - Handles the rate change process associated with the dynamic rate codec.

simpac.cc - Central element, schedules the first cell and performs the looping functions and statistics output.

stat_gen.cc - Generates the statistics associated with each simulation block.

vbr_gen.cc - Generates the cell arrival times for a MPEG-2 video traffic source.

vbr_gen2.cc - Generates a modified VBR video source with 1/20 the data rate of the main MPEG based VBR source.

The listed files are included on the CD attached to this dissertation. Readme.txt files are included at each directory level to aid navigation.