

The copyright of this thesis vests in the author. No quotation from it or information derived from it is to be published without full acknowledgement of the source. The thesis is to be used for private study or non-commercial research purposes only.

Published by the University of Cape Town (UCT) in terms of the non-exclusive license granted to UCT by the author.

**ANALYSIS AND DESIGN OF A 1KW CLASS-GD
ULTRASONIC GENERATOR**

By

Jacques Wheeler

2006

**ANALYSIS AND DESIGN OF A 1KW CLASS-GD
ULTRASONIC GENERATOR**

Submitted to:

The Department of Electrical Engineering for
fulfilment of the requirements for the Degree of
Master of Science in Electrical Engineering

by:

Jacques Wheeler

University of Cape Town, October 2006

Declaration

I declare that the contents of this thesis represent my own work except where otherwise specified. The references refer to words and ideas of other people. This work has not been previously examined at this, or any other institute.

University of Cape Town

signature removed

J. Wheeler

Cape Town, 2006

..... 22/01/2007

Date

Acknowledgements

I should like to thank my father P.W. Wheeler and mother M.M. Wheeler for years of support and patience. Without their guidance this study would not have possible.

Next but no less important, I should like to thank Prof. J. Tapson (UCT) and Prof. J Davies (CPUT) for being my M.Sc. Supervisors. I could not have completed my Higher Education if it was not for their continued support and guidance.

For the motivation and support from my under studies Brevin Claassen and Gregory Payne, I would like to give a special thanks.

Lastly, I should like to thank the staff and students at the Centre of Instrumentation Research at the Cape Peninsula University of Technology especially Dr A. Campbell, Dr I de Vries. As well as I. Robertson and G. Rose in the Heavy Current Laboratories.

Jacques Wheeler

Synopsis

Ultrasonic generators combined with ultrasonic transducers play a significant role in the industrial and medical fields. These devices are frequently used in food processing industry where bacteria are destroyed by destructive cavitation. They are also used for medical imaging, which is usually referred to as the “ultrasound”. A wide range of general-purpose ultrasonic generators is currently available on the market and recently, compact efficient modules have become available. The problem with most ultrasonic generators is that they are application specific and have only a few pre-programmed selectable control options. In the field of ultrasound and acoustics research, a need exists for an ultrasonic generator that is capable of having a new control topology applied without the need for costly and time consuming circuit design and PCB population. The need also exists for a flexible power controller stage on which designer waveforms can be specified and applied without the same need for circuit design and PCB population. The universal ultrasonic generator would also require an array of feedback loops for power and frequency control.

Linear amplifiers have been used in the past, and to this day, as ultrasonic generators as they have a wide bandwidth. The problem with these amplifiers is their poor efficiency, leading to costly and bulky systems with limited power handling capabilities. Switch mode type ultrasonic generators provide great efficiencies, leading to compact systems with almost unlimited power handling capabilities.

Key to the success of the Class-GD ultrasonic generator approach is utilization of a software layer, reprogrammable controllers, and a switch mode power stage. These features will allow the researcher to design, implement and evaluate different control topologies in a matter of hours, with negligible cost. The power control stage is programmable, allowing open loop wave shaping, thus allowing the researcher the ability to evaluate the effectiveness of designer waves. The switch mode power stage allows advanced ultrasonics to be realized with comparable efficiencies, but with much higher power densities.

This document describes the simulation, design and testing of a prototype Class-GD ultrasonic generator. Although the topology is capable of achieving high power output (approximately 1 kW), results were only obtained for moderately low transducer power levels. This was due to the lack of a large enough acoustic load and transducer horn. The generator successfully detected the optimum operating frequency of a single ultrasonic transducer by means of a peak current detection process. The generator was also successful in tracking the optimum operating frequency of a single ultrasonic transducer by means of a peak current detection process.

The success of this project lies in the user-friendliness of the control layer and the software layer. This was proven when two students Brevin Claassen and Gregory Payne successfully designed, implemented and tested their own control topologies under my guidance. Gregory Payne, with guidance from Dr Lynn Brown and myself, showed how the Class-GD ultrasonic generator could be used to perform microencapsulation. Microcapsules with a diameter of $100\mu\text{m}$ to $200\mu\text{m}$ were produced at a success rate of 61.9%, compared to previous work done at the Cape Technikon where only 10% of the microcapsules produced were smaller than $186\mu\text{m}$.

Table of contents

	<i>Page</i>
Declaration	i
Acknowledgements	ii
Synopsis	iii
Table of contents	v
List of Figures	ix
List of Tables	xi
Glossary of Terms	xii
Chapter 1 – Introduction	1
1.1 Formulating the Problems	1
1.2 The Problem in Context.....	2
1.3 Aims and Objectives	3
1.4 Thesis Structure	4
Chapter 2 – Preliminary Investigation	6
2.1 Background	6
2.2 Ultrasound	6
2.2.1 Cavitations.....	6
2.2.2 The Ultrasonic Transducer.....	8
2.4 Ultrasonic generator.....	12
2.4.1 Linear Ultrasonic Generators.....	12
2.4.2 Switch Mode Ultrasonic Generator	13
2.5 Ultrasonic Control Techniques	14
2.5.1 Phase-lock Loop	15
2.5.2 Admittance locking.....	15
2.5.3 Sweep Frequency	16
Chapter 3 – Design specifications	18
3.1 The Class-GD Specifications.....	19
3.2 Anticipated Electrical Specifications	19
3.3 Comparison of the Class-GD approach to established systems	20
3.4 Block Diagram of the Class-GD System	20
Chapter 4 – Class-GD generator sub-system design	22
4.1 Power Layer Selection and Design	22
4.1.1 Rectifier and Filter Design.....	23

4.1.2	Buck Regulator Design	23
4.1.3	H-bridge Inverter Design	24
4.1.4	Power Filter Design.....	30
4.2	Power Interface Layer Design	31
4.2.1	Buck Regulator Driver Design.....	31
4.2.2	H-Bridge Driver Design	32
4.2.3	V and I Sensor Design	32
4.3	Signal Layer Design.....	33
4.3.1	Voltage and Current Signal Conditioning	34
4.3.2	Voltage Comparator	34
4.3.3	Voltage Controlled Oscillator	35
4.4	Control Layer Design.....	35
4.5	Software Layer Design.....	38
4.5.1	DC Bus-voltage Control.....	38
4.5.2	Frequency Control.....	40
4.5.3	Digital Sinusoidal Pulse-width Modulation (SPWM) control.....	41
4.5.4	Implementing Auto Transducer Frequency Detect.....	44
4.5.5	Implementing phase-lock loop control	45
4.5.6	Implementing Admittance Locking Control	46
4.5.7	Implementing the frequency modulation technique.....	48
Chapter 5 – Experimental Evaluation		50
5.1	General System Performance	50
5.1.1	General System Efficiency.....	51
5.1.2	General Frequency Scan Results.....	52
5.1.3	General Admittance Locking Control Techniques Results	54
5.2	Single Ultrasonic Transducer Performance Tests.....	55
5.2.1	Single Transducer Scan Results	56
5.2.2	Single Transducer Admittance Locking Results.....	57
5.2.3	Single Transducer Saw-tooth Locking Results	58
5.2.4	Single Transducer Triangle Locking Results.....	58
5.2.5	Single Transducer Power Transfer Results	59
5.3	Transducer Array Performance Tests.....	60
5.3.1	Transducer Array Scan Results	61
5.3.2	Transducer Array Power Transfer Results	61

Chapter 6 - Conclusions and Recommendations	63
6.1 Conclusions	63
6.2 Recommendations	65
References	66
Appendix A - Schematic Diagrams	71
A1 Control circuit schematic diagram	72
A2 Power circuit schematic diagram	73
Appendix B - Experimental results	74
B1 System efficiency	75
B2 Scan results	76
B3 Single Transducer scan results	78
B4 Transducer Array scan results	80
B5 Admittance locking control techniques results	82
B6 Single transducer admittance locking results	83
B7 Single transducer saw-tooth locking results	84
B8 Single transducer triangle locking results	85
B9 Single Transducer power transfer results	86
B10 Transducer array Admittance locking power transfer results	87
B11 Transducer array Saw tooth locking power transfer results	88
B12 Transducer array Triangle locking power transfer results	89
B13 Transducer array power transfer results	90
Appendix C - Detailed design	91
C1 Power layer - Rectifier and filter	93
C1.1 Power switch (SW1)	93
C1.2 Input fuse (F1)	94
C1.3 Input rectifier (DB1)	94
C1.4 Filter capacitors (C1)	95
C1.5 Capacitor charging circuit	97
C1.6 Relay RL1	97
C2 Power layer - Buck regulator and filter	98
C2.1 Input filter capacitors (C1)	98
C2.2 Switching MOSFET (M1)	98
C2.3 MOSFET Heatsink selection	98
C2.4 Filter Inductor (L1)	100

C2.6	Diode D1	101
C3	Power layer - H-Bridge Inverter.....	102
C3.1	Switching component selection	102
C4	Power layer - Power filter.....	104
C5	Power interface layer - Buck regulator driver.....	105
C5.1	Selection of the bootstrap capacitor (C1).....	105
C6	Power interface layer - H-Bridge driver	106
C7	Power interface layer - V and I Sensor.....	107
C8	Signal layer - Voltage and current signal conditioning.....	108
C9	Signal layer - Voltage Comparator	109
C9.1	R2 and C1 selection	109
C10	Signal layer - Voltage controlled oscillator.....	111
C11	Control layer - Microcontroller	112
C12	Control layer - FPGA	113
C13	Software layer - Microcontroller program	114
C13.1	Transducer auto detect scan flowchart.....	114
C13.2	Admittance locking flowchart.....	115
C13.3	Saw-tooth locking flowchart	116
C13.4	Triangle locking flowchart.....	117
C13.5	Micro program	118
C14	Software layer – FPGA logic program.....	133
C14.1	Sinpwm2dec.....	134
C14.2	Sinpwm2.....	135
C14.3	Mod4a.....	135
C14.4	Lead_lag	136
C14.5	Power1.....	136

List of Figures

	<i>Page</i>
Figure 1: Block diagram of the Class-GD ultrasonic generator	3
Figure 2: The life cycle of a cavitation bubble	7
Figure 3: Construction of a typical magnetostrictive transducer	8
Figure 4: Construction of a typical piezoelectric transducer, shown in cross section	9
Figure 5: Mason's Electrical Equivalent of an Ultrasonic Transducer.....	10
Figure 6: Conductance and susceptance of a transducer	11
Figure 7: Three most common linear amplifier types	12
Figure 8: Full bridge inverter driving an ultrasonic transducer	13
Figure 9: The Class GD topology	14
Figure 10: Simplified block diagram of the phase-lock loop control topology	15
Figure 11: An illustration showing standing waves and effect	17
Figure 12: Alternative uses or the Class-GD solution	18
Figure 13: Block diagram of the Class-GD ultrasonic generator	21
Figure 14: Power layer	22
Figure 15: Input switch, rectifier and filter	23
Figure 16: Buck regulator and filter	24
Figure 17: H-bridge inverter	24
Figure 18: SIMCAD schematic of the H-bridge inverter stage	25
Figure 19: SIMCAD waveforms of MOSFET gating signals and load current	26
Figure 20: SIMCAD waveforms of MOSFET current	26
Figure 21: Positive cycle currents in an H-bridge inverter	27
Figure 22: ORCAD simulation with switch average power loss	28
Figure 23: MOSFET and IGBT H-bridge hybrid	28
Figure 24: ORCAD simulation with switch average power loss	29
Figure 25: A balanced two-pole filter was used to reduce the EMI	30
Figure 26 Filter frequency response	30
Figure 27: Power interface layer	31
Figure 28: Buck regulator driver circuit	31
Figure 29: H-Bridge driver circuit	32
Figure 30: Current transformer and voltage transformer	33
Figure 31: Signal layer	33

Figure 32: Voltage and current peak and zero crossing detection circuit	34
Figure 33: DC Bus-voltage comparator	34
Figure 34: Voltage controlled oscillator	35
Figure 35: Control Layer	36
Figure 36: The Microcontroller with human interface and FPGA	37
Figure 37: DC Bus-voltage control path	39
Figure 38: SIMCAD simulation of the Buck regulator	40
Figure 39: Frequency control path	41
Figure 40 Digital bipolar SPWM circuit with load voltage waveform	42
Figure 41: Digital unipolar SPWM circuit with load voltage waveform	43
Figure 42: FFT of a Square-wave, Unipolar and Bipolar SPWM signal	43
Figure 43: Simplified auto transducer frequency detect flowchart	44
Figure 44: Phase-lock loop control path	45
Figure 45: Admittance locking control path	46
Figure 46: Admittance locking control technique	47
Figure 47: Simplified admittance locking flowchart	47
Figure 48: Saw-tooth locking control technique	48
Figure 49: Triangle locking control technique	49
Figure 50: The setup used to measure system efficiency	51
Figure 51: Percentage efficiency versus output power at various loads	51
Figure 52: Transducer frequency versus PIC frequency set point	52
Figure 53: Admittance scan for a single and multiple transducer array	53
Figure 54: Class-GD scan versus HP impedance analyser	54
Figure 55: The signal transducer arrangement	55
Figure 56: Single transducer scan results	56
Figure 57: Single transducer admittance locking results	57
Figure 58: Single transducer saw-tooth locking results	58
Figure 59: Single transducer triangle wave locking results	59
Figure 60: Single transducer power transfer results	59
Figure 61: The multi-transducer array setup	60
Figure 62: Transducer array scan results	61
Figure 63: Aluminium foil showing destruction pattern	62
Figure 64: Transducer array power transfer results	62

List of Tables

	<i>Page</i>
Table 1: Product specifications of two commercially available linear generator.....	13
Table 2: The product specifications of the OW series from MASTERSONIC	14
Table 3: Ultrasonic applications	19
Table 4: Anticipated electrical specifications	19
Table 5: Comparison of the various generator topologies	20
Table 6: FPGA frequency ranges	41
Table 7: Test to be performed on the Class-GD ultrasonic generator.....	50
Table 8: Frequency shift with a increase in voltage set point for a single transducer	57
Table 9 Frequency shift with a increase in voltage set point for a transducer array.....	61
Table 10: Ultrasonic generator comparison.....	64

University of Cape Town

Glossary of Terms

AC	Alternating current or voltage
Acoustic	The energy of sound waves.
Acoustics	The science and application of acoustic energy.
Admittance	A measure of electrical conduction, the reciprocal of impedance.
Bubble	A spherical volume of gas or vapour in a liquid.
Cavitation	The sequential formation and collapse of vapour bubbles in a liquid subjected to acoustic energy.
CIR	Centre for Instrumentation Research
Conductance	The power of a specified material to conduct electricity.
COTS	Commercial off The Shelf systems
Efficiency	The ratio of useful work performed to the total energy expended
EMI radiation	Electromagnetic interference
Firmware	Software programmed into a device to make it perform a function according to the condition set in the software.
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
LCD	Liquid Crystal Display
LPF	Low Pass Filter
Magnetostriction	The change in dimension of a ferromagnetic body caused by a change in its state of magnetization.
Micro-encapsulation	The process of producing Microcapsules
Microcapsules	A small soluble gelatine or gum drop with a hard shell enclosing a dose of medicine. With a diameter between 100 μ m and 200 μ m.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PIC	Programmable Interrupt Controller.
PLL	Phase-Locked loop
Resonance	Resonance is defined as the frequency at which the applied voltage and the resultant are in phase.
RS232	A serial communication port normally found on a personal computer.
Sonochemistry	Driving and accelerating chemical reactions through the application of ultrasonic energy.

SPWM	Sinusoidal Pulse Width Modulation
Transducer	A device for converting a signal from one medium of transmission to another, esp. an electrical signal into a non-electrical one, e.g. voltage into pressure, or vice versa.
Transducer Array	A collection (more than one) of transducers that collectively produce a greater effect.
Ultrasonic	Sound with a frequency above 20kHz.
Ultrasound	Refer to Ultrasonic
Ultrasonics	The application of using ultrasonic energy to do work.
VCO	Voltage Controlled Oscillator

University of Cape Town

Chapter 1

Introduction

Ultrasound refers to an audio signal above 20 kHz, which is beyond a human's maximum audible frequency [1]. It is normally employed in performing duties that require such a frequency [2]. Frequencies between 20 kHz and 100 kHz are categorised as power ultrasound (destructive), and frequencies between 5 MHz and 10 MHz as diagnostic ultrasound (non-destructive) [3].

1.1 Formulating the Problems

Piezoelectric ultrasonic transducers are designed with an optimum operational frequency or resonant frequency. However, because of environmental conditions around the transducer, this frequency sometime changes [4]. This complicates the process of determining an exact starting frequency at which to drive a transducer.

A second problem with piezoelectric ultrasonic transducers is the resonant frequency varies as load conditions change. This results in the driving of the transducer at a frequency other than at optimum operational frequency, which reduces performance and lead to poor system efficiency plus possible transducer damage [4].

Another problem encountered in applications involving more than one ultrasonic transducer is that even though each transducer was designed with identical optimum operational frequencies, the resonant frequency of each transducer changed independently because of unbalanced loading. This reduced system performance, leading to poor system efficiency and a risk of transducer damage [4].

A need exists for a locally produced ultrasonic supply showing improved efficiency and higher energy density than off-the-shelf linear modules. Also required is an ultrasonic generator with a flexible control system. Many existing systems, dependent on analog control circuits, require complete system re-design to accommodate newly designed control topologies.

1.2 The Problem in Context

The system described in this document needs to facilitate easy implementation of various control techniques required to detect optimal operating frequency of an ultrasonic transducer and to ensure the system operated at peak efficiency as it delivers power to the load.

A digital controller with a software platform would permit the designer to implement and test various control topologies, without the need for costly and time-consuming PCB design, manufacturing and populating.

The digital controller used must facilitate various programming languages to allow users of different skill levels an opportunity to use the system in their study of ultrasonics and their control.

The PIC microcontroller must give users at tertiary level equipped with basic skills and some guidance an opportunity to programme the system with new control techniques by means of a language named PIC Basic. Advanced users will be able to programme the system with other software languages such as Assembler or C. High speed functions such as voltage control, wave shaping and circuit protection can, however, not be done by the PIC microcontroller and was allocated to a FPGA.

The system requires a control stage able to control the power supply to the load in a manner such that power is not wasted in the system, resulting in high efficiency, and incorporating high energy density.

A switchmode power stage offers a system with greater efficiency when compared to a linear equivalent.

These criteria led to the design of the novel Class-GD ultrasonic generator, discussed in this document. It may be seen in block format in Figure 1. The application's control system will be software based, allowing system upgrades through firmware updates. Such technology permits advanced ultrasonics to be realised with improved efficiency and higher power densities.

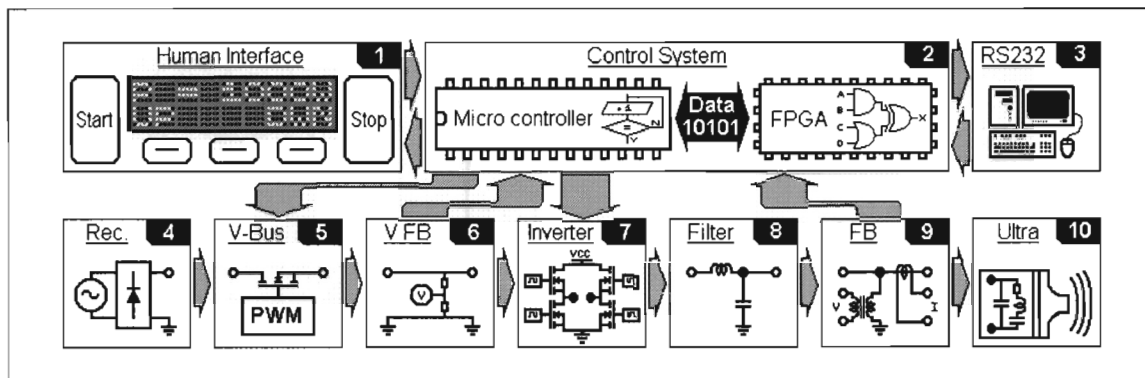


Figure 1: Block diagram of the Class-GD ultrasonic generator

The following modules are shown in Figure 1:

1. **Human interface** – permits an operator to control the mode of operation by using buttons to navigate a menu-driven display. The display is used to inform the user on system status and mode of operation.
2. **Control system** – is software driven and utilises a microcontroller and FPGA to monitor system status and operate the modules required to make the system work.
3. **RS232** – connects the system to a personal computer, where telemetry can be stored and from which commands can be accepted.
4. **Rec.** (rectifier) – rectifies and filters the AC mains into a DC waveform.
5. **V-Bus** (DC voltage bus control) – is used for power control in the system.
6. **V FB** (voltage feedback) – the voltage feedback circuit is used to monitor the V-Bus module
7. **Inverter** – changes the DC voltage from the V-Bus into a high frequency modulated sinusoidal AC waveform.
8. **Filter** – removes the modulation signal, leaving only the desired sinusoidal wave.
9. **FB** (feedback) – the controller uses the voltage and current feedback.
10. **Ultra** (ultrasonic transducer) – converts the electrical signal into mechanical work.

1.3 Aims and Objectives

The first aim was to determine the optimum operational frequency or resonant frequency of the ultrasonic transducer. The Class-GD ultrasonic generator needed to perform a frequency scan from 16 kHz to 50 kHz in steps of ± 20 Hz, while measuring current to determine the transducer resonant frequency.

Once a resonant frequency had been found, two control techniques are independently implemented and tested for effectiveness in locking and following the resonant frequency of a transducer under varying load conditions. These control techniques are phase-lock loop control and admittance locking [5], [6].

Two additional control techniques were investigated. These are monotonically swept frequency (saw-tooth wave) control and frequency-modulated control (triangle wave). These locking techniques are designed for equal power distribution in applications where more than one ultrasonic transducer is supplied by the same ultrasonic generator [7].

This project combines two existing amplifier types, namely Class-D and Class-G amplifiers to produce a system superior to either [8]. The control sub-system will utilise two reprogrammable devices, allowing reconstruction of the control topology by writing a new software code for the system. This eliminated the need for time-consuming hardware development. The technology allowed advanced ultrasonics to be realised with improved efficiencies and with higher power densities.

1.4 Thesis Structure

Chapter 1 (Introduction) formulates the problem an ultrasonic generator needed to overcome when driving ultrasonic transducers. The Class-GD ultrasonic generator is introduced. Aims and objectives for this thesis are set and the thesis structure presented.

Chapter 2 (Preliminary Investigation) gives a background to ultrasound, covering a brief history of the subject. Some effects of ultrasound are considered, including cavitation. The ultrasonic transducer is described and some applications of ultrasound investigated. Varieties of ultrasonic generators are introduced. Finally a few ultrasonic control techniques are described.

Chapter 3 (Design Specifications) describes the design specifications of the Class-GD ultrasonic generator. Applications for this ultrasonic generator are introduced and anticipated electrical parameters shown. The Class-GD generator is compared to established systems; finally the Class-GD amplifier is introduced.

Chapter 4 (Class-GD generator sub-system design) describes design procedure for the various sub-systems and modules of the Class-GD ultrasonic generator. It includes simulations of some of the modules, sub-system component value calculations, and implementation procedures for the various modules. The implementation of the various control techniques is explained.

Chapter 5 (Experimental Evaluation) contains the experimental evaluation of the Class-GD ultrasonic generator. Here the test procedures are described and results shown. Observations are made on results achieved.

Chapter 6 (Conclusions and Recommendations) discusses the results and makes recommendations for development.

References: Lists all sources of information used in the compilation of this document.

Appendix A: (Schematic Diagrams) illustrates Class-GD ultrasonic generator.

Appendix B: (Experimental Results) offers detailed experimental results.

Appendix C: (Detailed Design) shows the detailed design of the Class-GD ultrasonic generator, including hardware and software.

Chapter 2

Preliminary investigation

2.1 Background

In 1880, Pierre and Jacques Curie observed and published the piezoelectric phenomenon. They achieved this by conclusively measuring the surface charge that appeared on specially prepared crystals (tourmaline, quartz, topaz, cane sugar and Rochelle salt) when subjected to a mechanical stress and vice versa. Lord Rayleigh (John W. Stutt) became the greatest of all acousticians when he published *The Theory of sound* in the beginning of the 20th century [9].

Today, two main compounds, Barium Titanate and Lead Zirconate Titanate, are used in the manufacturing process of piezoelectric ceramic. This ceramic has the advantage of being hard, chemically inert and immune to other atmospheric conditions. It may be given almost any shape or size during manufacture [10].

2.2 Ultrasound

Ultrasound refers to an audio signal beyond a human's maximum audible frequency of about 20 kHz [1]. Ultrasound is generally used to perform work which depends on that frequency [2]. Frequencies between 20 kHz and 100 kHz are generally categorised as power ultrasound (destructive) and frequencies between 5 MHz and 10 MHz as diagnostic ultrasound (non-destructive) [3].

2.2.1 Cavitations

Cavitation occurs when the amount of ultrasonic energy applied to a liquid exceeds the energy of the forces holding the molecules together [10]. This results in the growth and the collapse through implosion of tiny micro bubbles. The implosion of these tiny bubbles produces short-lived hot spots, releasing enough energy to drive a variety of chemical and mechanical applications [11].

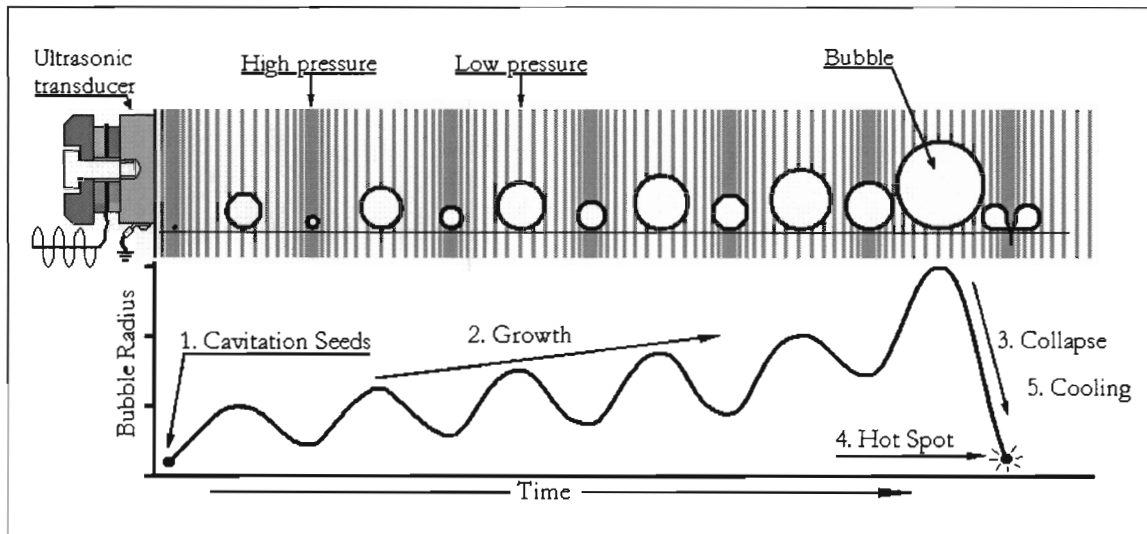


Figure 2: The life cycle of a cavitation bubble. The ultrasonic transducer converts the electrical signal into pressure waves in the liquid. These pressure waves compress and stretch a bubble making it “grow”. At the end of the life cycle the bubble collapses and releases energy [11]

There are two types of cavitations generated by ultrasound. One is stable cavitation. This type of cavitation occurs at high frequency. The bubbles formed by this type of cavitation are relatively permanent and can continue to oscillate for many cycles of acoustic pressure. These bubbles have less time to grow as the high frequency produces a small bubble size, resulting in less violent cavitation and low destructive capabilities [11].

A second type of cavitation is transient cavitation. This type occurs at lower frequencies. The bubbles formed by this type of cavitation last a shorter time (usually less than one cycle) [11].

Factors affecting the cavitation process include temperature, power, frequency and standing waves. Temperature directly influences the cavitation process by affecting liquid viscosity, solubility of gas in the liquid, and vapour pressure. The cavitation intensity is directly related to ultrasonic power [12].

At high power levels large numbers of bubbles are formed. Some may merge to form bigger bubbles, causing implosions that are more violent. At excessively high power levels large numbers of bubbles may form at the transducer surface, thus decoupling the transducer from the load and resulting in decreased power transfer [4]. The cavitation intensity is inversely related to the ultrasonic frequency.

The higher the frequency, the smaller the bubbles will be, because of a shorter growth period resulting in less violent cavitation.

2.2.2 The Ultrasonic Transducer

An ultrasonic transducer is a device that converts electrical energy into a mechanical displacement at a frequency above the human audible range of about 20 kHz [1].

The two most commonly used ultrasonic transducers are the magnetostrictive and the piezoelectric transducers. Magnetostrictive transducers are known for their robustness in industrial applications [10].

Zero-space magnetostrictive transducers are manufactured by placing nickel laminations tightly together with an electrical coil placed over the nickel stack. These transducers use the principle of magnetostriction in which certain materials expand and contract when placed in an alternating magnetic field. When an oscillating current is sent through the coil the nickel stack vibrates. This vibration frequency is equal to twice the oscillating current frequency [10].

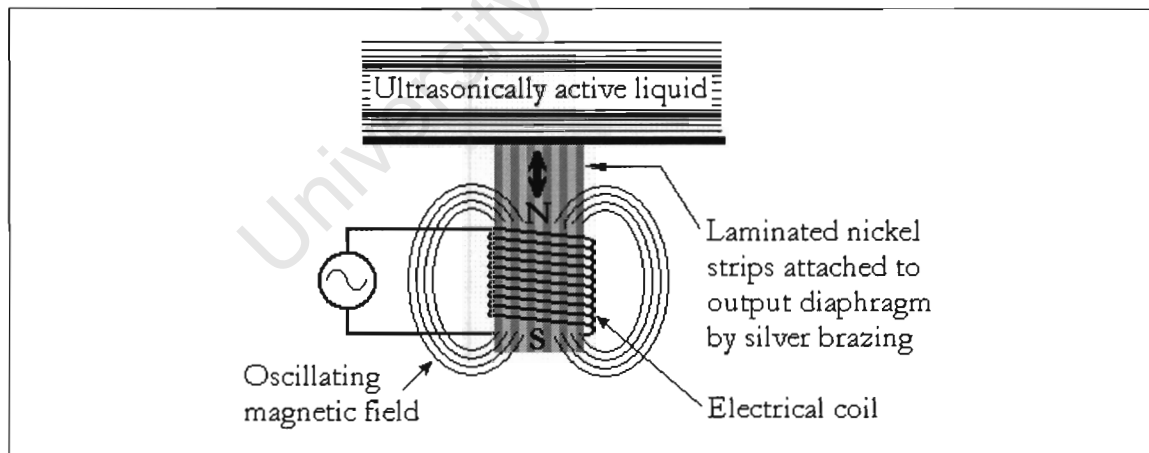


Figure 3: Construction of a typical magnetostrictive transducer [10]

Piezoelectric transducers are, however, generally preferred because of greater efficiency and operating frequency, when compared to magnetostrictive transducers [10].

A piezoelectric transducer is seen in Figure 4. The active element in this type of transducer is the piezo-polarized material (piezoelectric driving element). When an electric field is applied across the piezoelectric driving element, the molecules align [4].

This causes the piezoelectric driving element to change dimensions in a process known as electrostriction [4].

Piezoelectric transducers are optimised to resonate at a predetermined frequency to deliver power to a liquid medium [4]. This document refers to the optimised transducer frequency as its resonant frequency, or optimum operating frequency.

The Optimisation of the Piezoelectric Transducer

The resonant frequency of the piezoceramic material is determined by the thickness of the piezoceramic material (piezoelectric driving elements), where the piezoceramic material is cut to half the desired wavelength along one axis of resonance [4].

A matching layer (often an aluminium coupling mass) is used to obtain maximum energy transfer to the load. This layer is usually cut to a quarter wavelength of the transducer's frequency, so the signal at the face of the transducer is in phase [4].

The backing mass (usually stainless steel) greatly influences the damping characteristics of the ultrasonic transducer. To ensure a narrow bandwidth of the transducer a backing mass is selected with an impedance value similar to that of the active element [4].

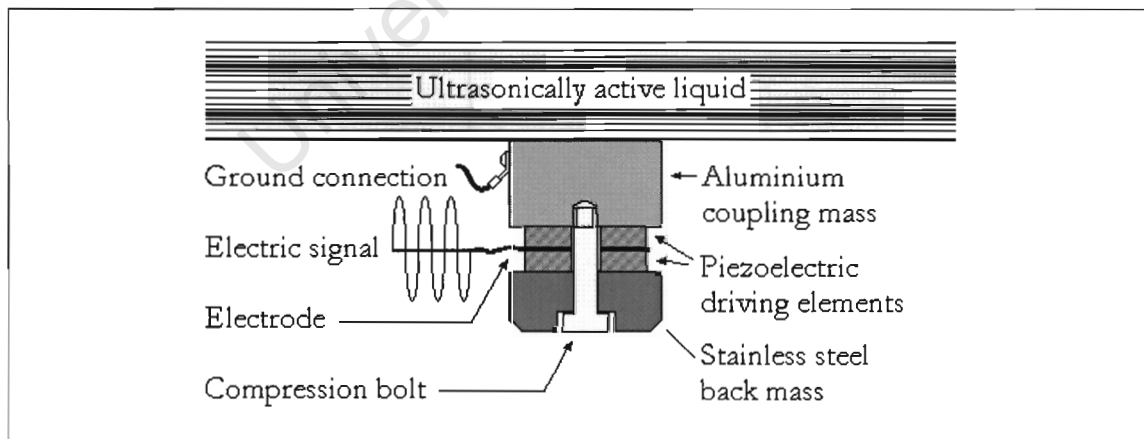


Figure 4: Construction of a typical piezoelectric transducer, shown in cross section [4]

WP Mason of Bell Telephone Laboratories electrically modelled the piezoelectric transducer in the 1930s. His simplified electric model of the piezoelectric transducer is seen in Figure 5 [13].

In Figure 5 the capacitor C_s represents the physical capacitance of the piezoelectric driving elements. This capacitance is dependant on the physical structure of the piezoelectric driving elements such as thickness, permittivity, type of piezoelectric material and area of the electrodes [13].

The electromechanical coupling ratio is represented by the transformer $T1$. The series LCR network represents the moving parts of the transducer [13].

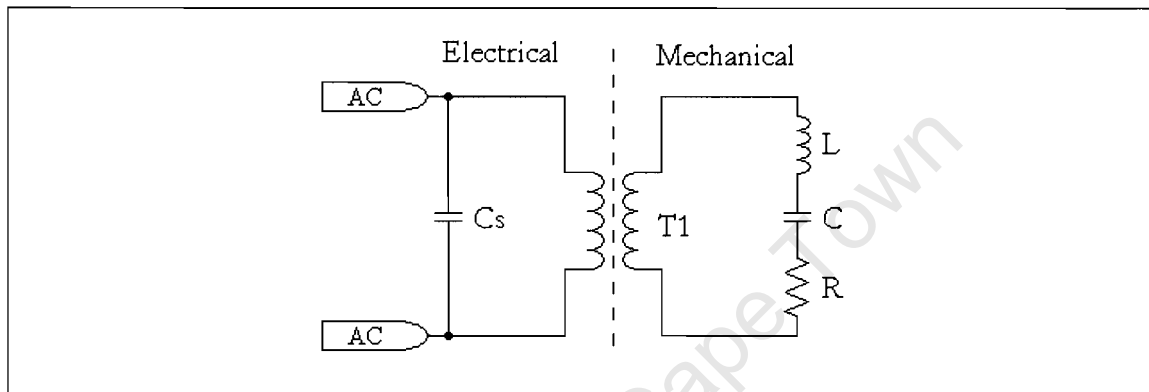


Figure 5: Mason's Electrical Equivalent of an Ultrasonic Transducer. C_s represents the physical capacitance of the piezoelectric driving elements. The electromechanical coupling ratio is represented by $T1$. The series LCR network represents the moving parts of the transducer [13]

The model piezoelectric transducer may be operated in one of two modes, series resonant mode and the parallel resonant mode. In series resonant mode, the transducer delivers a high output force at a low velocity (high pressure) to the load. In parallel resonant mode, the transducer delivers a low output force at a high velocity to the load [13]. Maximum acoustic power is delivered when the transducer is driven in series resonant mode.

Figure 6 shows the electrical conductance peaks at the frequency f_c . This is where the series resonant circuit is purely resistive and the impedance of the series resonant circuit is at a minimum. The susceptance reaches zero at the point where the impedance of the entire circuit is purely resistive. This is not at the frequency f_c , as the capacitor C_s causes the resonant frequency of the entire circuit to be higher than the resonant frequency of the series circuit. With a compensation inductor used to null the static capacitance C_s , the maximum power point occurs at the point of peak conductance and admittance [14].

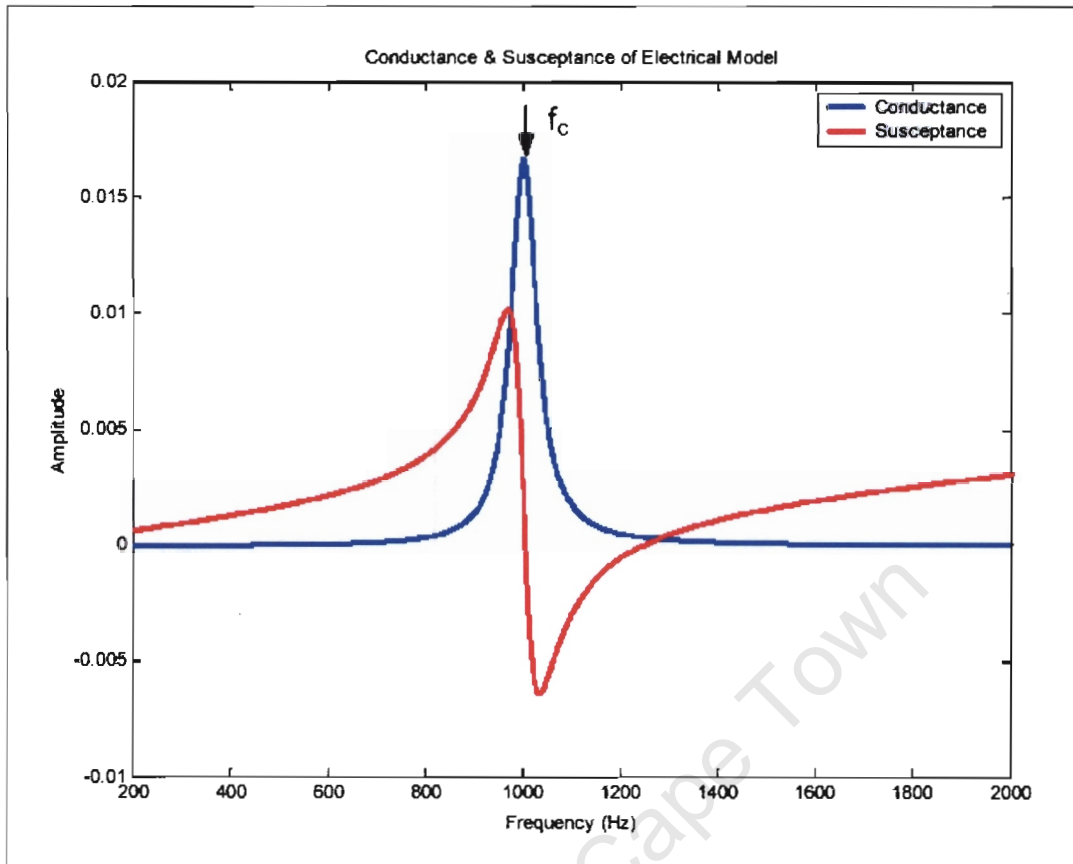


Figure 6: Conductance and susceptance of a transducer. The electrical conductance peaks at the frequency f_c . This is where the series resonant circuit is purely resistive and the impedance of the series resonant circuit is at a minimum. [14]

2.3 Applications of Ultrasound

Ultrasonics is the science of ultrasound and is grouped into two categories; power ultrasound (destructive) and diagnostic ultrasound (non-destructive) [3].

Power ultrasound describes most applications where the destructive cavitation effect of ultrasound is used to undertake work. Frequencies for this category usually range between 20 kHz and 100 kHz [3]. Applications associated with this category include the processes of sonochemistry, ultrasonic cleaning, cell disruption, plastic welding, etc [10].

Diagnostic ultrasound describes applications at frequencies where the destructive cavitation effect cannot occur. The frequency for this category begins around 5 MHz but may exceed a frequency of 10 MHz [3]. Applications associated with this category include high intensity focused ultrasound (HIFU) and wound healing [15].

2.4 Ultrasonic generator

The ultrasonic generator is a device designed to change the AC mains (50 Hz in South Africa) or battery power into a voltage and frequency (greater than 20 kHz) used to drive an ultrasonic transducer optimally.

The control technique used in such generators to drive an ultrasonic transducer optimally can be a simple phase-lock loop control technique [5], or a complicated multi-frequency, multi-mode, modulated control technique [16]. These generators are found in numerous applications from simple humidifiers to complicated ultrasonic imaging devices and surgical equipment [15]. Generators can be small enough to put in a portable device or be larger than a fridge as in industrial applications.

2.4.1 Linear Ultrasonic Generators

Linear power ultrasonic generators use one of the three linear amplifier topologies (shown in Figure 7) as their final driving stage. These amplifier topologies utilise the linear region of the active element (transistor) to form the shape of the output wave. This results in low system efficiency with low signal distortion [17].

Class A amplifiers account for a small portion of the audio market because of their low efficiency, which is typically less than 25%. This amplifier topology, however, has the least amount of distortion, consequently offering the best sound quality. Class B has the highest efficiency of the three topologies, typically around 78%. This amplifier topology, however, provides poor linearity around the crossover region. Class AB has a good efficiency (around 78%) and excellent linearity that makes this topology the most popular for audio amplifier design [17]. Class G and H amplifiers control the supply rail to a linear output thereby improving efficiency in the system [18], [21].

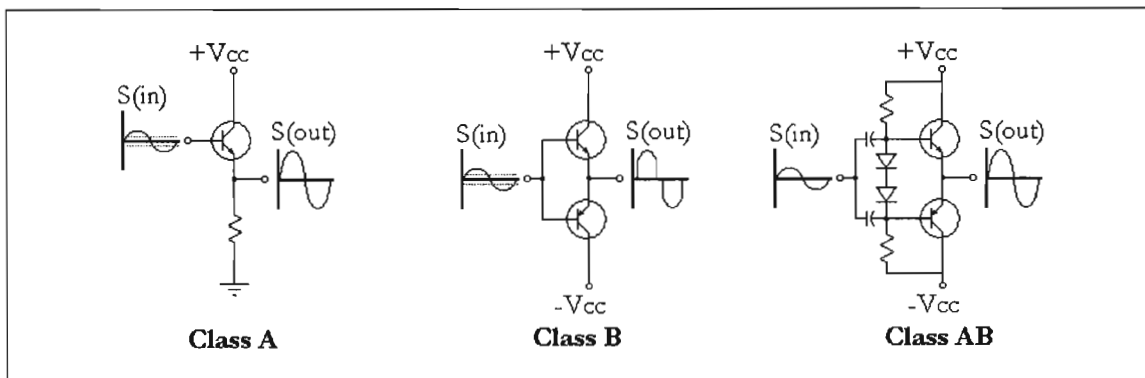


Figure 7: Three most common linear amplifier types, with their input and output signals [17].

Two commercially available linear ultrasonic generator solutions, the AG1006 LF from HOLTEK technologies and the ULTRA 2020 from T&C Power Conversion, Inc are used for comparison. The ULTRA 2020 linear amplifier design incorporates both Class A and Class AB topologies. This device uses the Class A topology in linear mode when supplying power to a maximum load of 50W, in addition, Class AB topology when supplying power to a maximum load of 175W. The Class B amplifier topology is used in the output power stage of the AG1006 LF ultrasonic generator. These devices are general-purpose air-cooled amplifiers suitable for a wide range of applications which include industrial, laboratory and medical applications [19], [20].

Specifications	ULTRA 2020 [20]	AG1006 LF [19]
Class of Operation:	Class A up to 50 W (linear) Class AB up to 175W (saturated)	Class B
Frequency range:	10 kHz to 15MHz minimum	25 kHz to 10MHz
Output power:	175W	300W
Efficiency:	NA	NA
Dimensions:	H 135 x W 254 x D 385 mm	H 135 x W 254 x D 385 mm
Weight:	~ 12 kg	~ 12 kg

Table 1: Product specifications of two commercially available linear ultrasonic generator solutions, the AG1006 LF and the ULTRA 2020 [19], [20]

2.4.2 Switch Mode Ultrasonic Generator

Switch mode ultrasonic generators use a half bridge or full bridge inverter. They predominantly utilise the cut-off and saturation regions of the active element (transistor) to form the output wave. This results in high system efficiencies, typically above 90% [21]. Output power is controlled by increasing and decreasing the duty cycle of the pulse width modulation (PWM) or “dead time” between the positive and negative cycle as shown in Figure 8 [22].

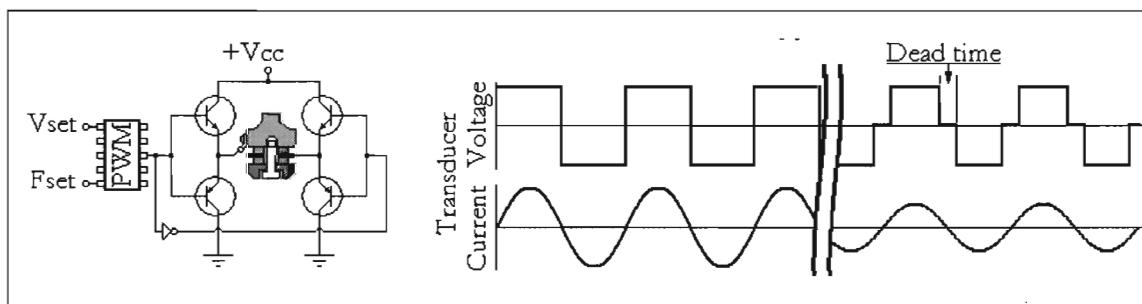


Figure 8: Full bridge inverter driving an ultrasonic transducer. The duty cycle to the full bridge inverter is set to 50% resulting in the first transducer voltage and current waves resulting in maximum power to the transducer. The duty cycle is reduced resulting in a dead time and a reduction in the power to the load [22]

A commercially available switch mode ultrasonic generator solution, the universal and wideband multi-frequency power supplies from MASTERSONIC, is used for comparison. It employs a multi-frequency, multi-mode, modulated (MMM) control technique and is capable of driving all kinds of piezoelectric transducers, submersible transducers, bench top cleaners and sonochemical reactors [23]. The switching output stage of this device makes it highly efficient and compact.

Specifications	MSG.300.OW	MSG.600.OW	MSG.1200.OW
Class of Operation:	NA	NA	NA
Frequency range:	21.435 – 40.560 kHz	21.435 – 40.560 kHz	21.435 – 40.560 kHz
Output power:	300W	600W	1200W
Efficiency:	approx. 95%	approx. 95%	approx. 95%
Dimensions:	170 x 150 x 150 mm	250 x 150 x 150 mm	230 x 160 x 370 mm
Weight:	2 kg	3.6 kg	4 kg

Table 2: The product specifications of the OW series from MASTERSONIC [23]

The Class GD is a combination of the Class G amplifier that controls the supply rail and the Class D switchmode amplifier.

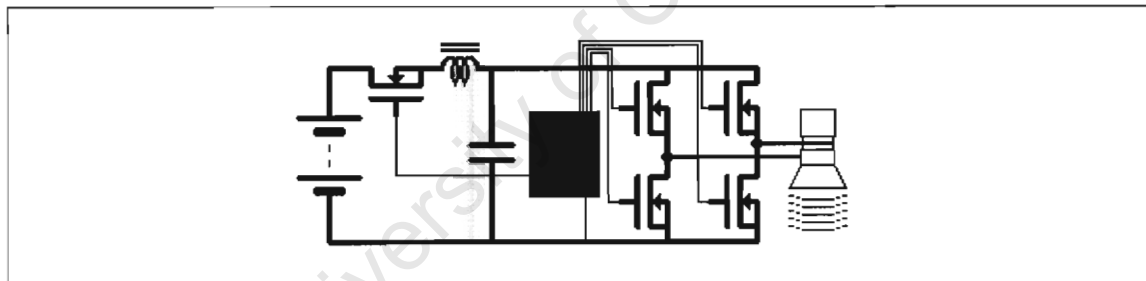


Figure 9: The Class GD topology uses the controlled supply rail of the Class G amplifier topology and replaces the linear amplifier stage with a Class D amplifier topology thereby improving the efficiency of the overall system

2.5 Ultrasonic Control Techniques

The resonant frequency of the ultrasonic transducer does not remain fixed at one frequency and will move because of change in the load and the transducer. If the resonant frequency of the ultrasonic transducer is not followed, the transducer will not operate optimally [4]. This means an automatic control system is required to maintain the ultrasonic generator's frequency at the ultrasonic transducer's optimum frequency [5], [6].

2.5.1 Phase-lock Loop

A method used to maintain an ultrasonic generator's frequency at the ultrasonic transducer optimum frequency is named a phase-locked loop (PLL) control. This control technique tracks the series resonant frequency, the frequency where voltage and current to the transducer are in phase. The PLL will monitor the phase of the voltage and current to the transducer, and will change the frequency until the voltage and current are in phase [5].

The phase-lock loop control topology consists of three main parts as seen in Figure 10. The first is the phase detector (multiplier), which determines phase difference between the transducer's voltage and current.

The low pass filter (LPF), filters the signal from the phase detector so that the filter output voltage represents the phase shift. The voltage-controlled oscillator (VCO) changes the output frequency according to the error signal obtained from the LPF [24]. A typical analog PLL device used is the 74HC4046A [25].

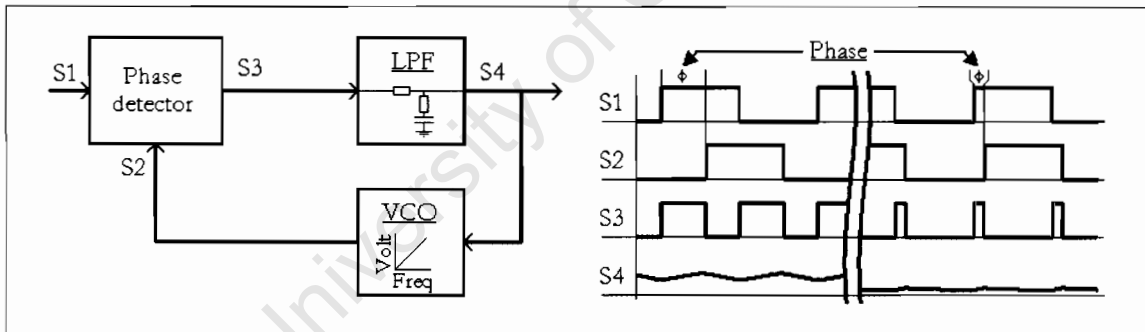


Figure 10: Simplified block diagram of the phase-lock loop control topology. The phase detector, determines phase difference between the transducer's voltage and current. The low pass filter (LPF), filters the signal from the phase detector so that the filter output voltage represents the phase shift. The voltage-controlled oscillator (VCO) changes the output frequency according to the error signal obtained from the LPF [24], [5].

2.5.2 Admittance locking

Another method employed to hold an ultrasonic generator's frequency at the ultrasonic transducer optimum frequency is called admittance-locking control. This technique is based on the principle maximum power transfer between the ultrasonic transducer and the liquid (load) occurs when the admittance of the transducer is at a maximum. The admittance locking ultrasonic generator will regulate constant voltage while monitoring

the current to the transducer and change the frequency until current is at a maximum (maximum admittance) [6].

The performance of the admittance locking control technique can, however, be improved as described in a thesis by William Robert Patterson in 2002. He shows the maximum power point is not at the point of maximum admittance, but instead at the point of maximum conductance. This error may be eliminated by a compensation inductor used to null the static capacitance in the ultrasonic transducer [14].

2.5.3 Sweep Frequency

Ultrasonic cleaning systems have long been troubled by the formation of standing waves. When sound waves (pressure waves) generated by the ultrasonic transducer interact with reflected waves, regions of increased and reduced cavitation intensity are produced, hence “standing waves”. These, as seen in Figure 11, might produce “zebra stripes” on the component being cleaned [10], [26].

At low power intensities, light regions on the foil as seen in Figure 11 would represent areas where no cleaning occurred. At high power intensities and with soft metals including aluminium, brass and copper, dark regions on the foil would represent areas where damage would appear. The basic solution to this problem is to move the component being cleaned around in the cleaning tank [10].

It was found that by varying or sweeping the frequency of the ultrasonic generator it was possible to reduce the effect of these standing waves [16]. This discovery led to the new field of frequency modulation techniques, all aimed to reduce the effect of standing waves without the loss of output power.

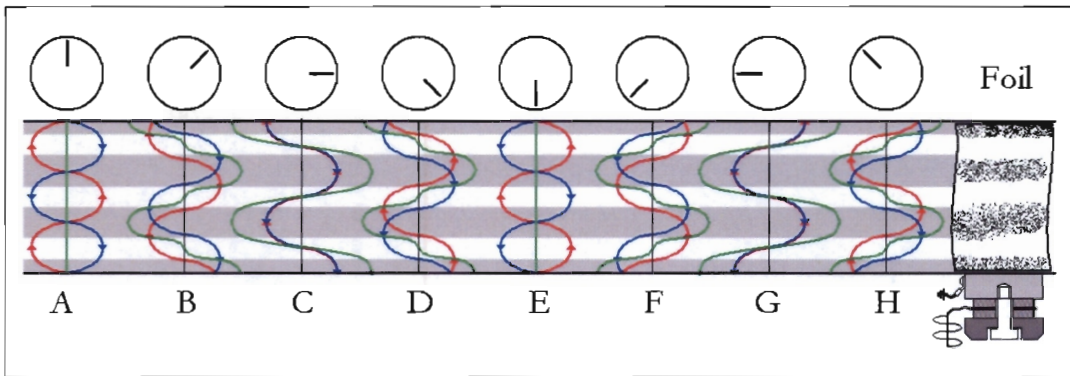


Figure 11: An illustration showing standing waves and effect. The red waves are from the ultrasonic transducer, the blue waves are the reflected waves and the green waves are resultant pressure. In A and E the transducer and reflected waves cancel. In C and G the transducer and reflected waves add. The grey lines represent areas of increased cavitation (standing waves). The foil shows the destructive pattern (zebra stripes) [10], [26]

Today's high power ultrasonic cleaning systems use an array of transducers to drive the load. This has led to a fresh problem. In spite of the careful selection of the individual transducers to ensure all have the same resonant frequency, it was found that under load conditions transducers with resonant frequencies closest to the optimal frequency draw the most current. This led to uneven power distribution in the ultrasonic cleaning bath [26].

It was found by sweeping the frequency to the transducer array, it was possible to deliver a similar amount of power to each transducer, as each would receive resonant frequency for an equal period. This sweeping also reduced the standing waves in the bath [26].

Parameters associated with sweep frequency control are the sweep bandwidth, usually 0 – 1000Hz, and sweep rate. The sweep bandwidth is usually placed symmetrically around the ultrasonic transducer's resonant frequency. The sweep rate refers to the speed at which the sweep is conducted. The sweep may also be performed at a fixed rate, or according to a pre-programmed function [16].

Chapter 3

Design Specifications

The Class-GD ultrasonic generator is a novel solution to an old problem. It shows an improved efficiency when compared to linear amplifier type ultrasonic generators. In addition it has greater flexibility as compared to existing ultrasonic generators. The success of this topology lies in its simplicity of design. It is possible to customise and alter the control topology and application of this device by changing its operating system software.

Typical applications for the Class-GD amplifier include ultrasonic cleaning, sonar and solar power motor speed drives as shown in Figure 12C (with future design). When configured as a ultrasonic generator, as seen in Figure 12A, the input to the Class-GD generator controls the output frequency. By ramping the input voltage up and down it is possible to provide a type of sweep frequency control. This control is performed automatically in the Class-GD generator, allowing the input to be used for power control or sweep bandwidth control. Figure 12B shows the Class-GD generator configured as a sonar power supply. The generator will automatically produce the carrier frequency needed to drive the sonar. The input to the Class-GD generator could be used to transmit information under water via the sonar. The output signal is typically a phase shift keyed modulation signal [27].

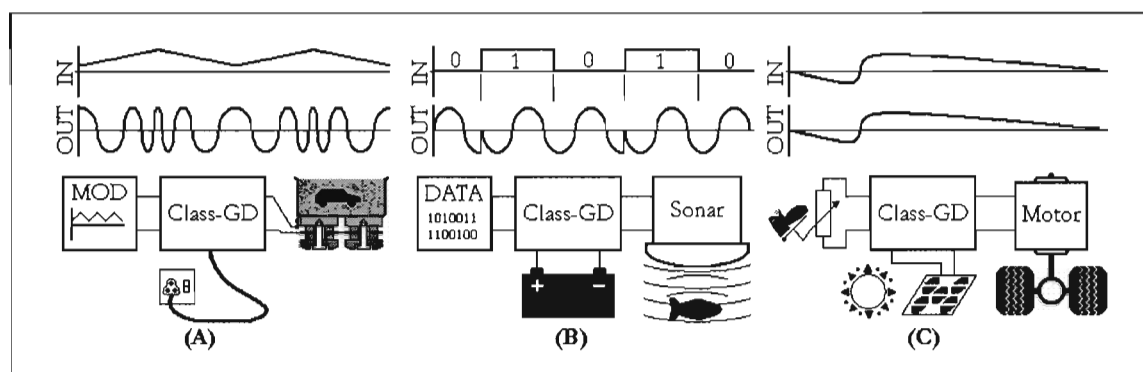


Figure 12: Alternative uses of the Class-GD solution. Option A shows the Class-GD system used as a ultrasonic bath driver with sweep frequency control. Option B shows the Class-GD system as a sonar driver with data transmitting capabilities. Option C shows the Class-GD system as a variable speed drive for a solar powered motor vehicle

3.1 The Class-GD Specifications

This project will concentrate on low frequency power ultrasonic generation, with a frequency range of 15 kHz - 50 kHz and a power range of between 1W to 1kW [23]. The device utilise a novel digital open loop sinusoidal pulse width modulation (SPWM) control technique and a open-ended control system. Possible ultrasonic applications where this technology may be advantageous include:

Low-Power applications	High-Power applications
Fault detections in materials	Soldering of aluminium
	Riveting and insertion of plastic parts
Dental drilling	Welding of metal
	Welding of plastics materials
Flow measurement	Drilling and cutting of materials
	Mixing of insoluble materials
Sonochemistry	Cleaning of metal
	Destruction of bacteria

Table 3: Ultrasonic applications [10], [23]

3.2 Anticipated Electrical Specifications

The values shown in Table 4 were selected using the following criteria:

1. Supply Voltage – Available AC mains in South Africa
2. Supply Current – Determined by output power and anticipated efficiency
3. Supply Frequency – Available AC mains in South Africa
4. Operating Bandwidth – Aimed at low frequency ultrasonic applications
5. Load Voltage (Peak) – Determined by the topology
6. Load Current (RMS) – Determined by the topology and selected components
7. Load Power (RMS) – Required output power
8. Load Impedance – Determined by the topology
9. Efficiency – Approximate

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VSUP	Supply Voltage (RMS)	Operation	180	220	250	V
ISUP	Supply Current (RMS)	Full power operation	–	–	6	A
fSUP	Supply Frequency	Operation	40	50	440	Hz
fBW	Operating Bandwidth	Full power	15	–	50	kHz
VL	Load Voltage (Peak)	Full power	–	–	300	V
IL	Load Current (RMS)	Operation	–	–	15	A
PL	Load Power (RMS)	Specified	–	1000	–	W
LZ	Load Impedance	Load at resonance	–	–	10k	Ω
η	Efficiency	Full power	–	85	–	%

Table 4: Anticipated electrical specifications

3.3 Comparison of the Class-GD approach to established systems

Many manufacturers have well established COTS (commercial off-the-shelf systems) ultrasonic generators available. Practical considerations when selecting a general-purpose ultrasonic generator are efficiency, operating bandwidth, range of applications, power rating, upgradeability, volume-to-power ratio (mm^3/Watt) and mass-to-power ratio (kg/Watt).

	Linear generator	Switch mode generator	Class-GD generator†
Efficiency	0 (less than 50%)	++ (greater than 80%)	++ (greater than 80%)
Operating bandwidth	++ (10kHz - 15MHz)	~ (19.02kHz - 46.73kHz)	~ (15kHz - 50kHz)
Range of applications	++ (destructive, non)	~ (destructive only)	+ (not only ultrasound)
Power rating	+ (linear)	++ (switch mode)	++ (switch mode)
Upgradeable	~ (analog circuits)	+ (control only)	++ (control and wave)
Volume-to-power ratio	~ (± 44000)	++ (± 11000)	++ (switch mode)
Mass-to-power ratio	~ (± 0.04)	++ (± 0.006)	++ (switch mode)

0 Below average, ~ Average, + Good, ++ Excellent

Table 5: Comparison of the various generator topologies [19], [20], [23]

When compared to linear ultrasonic generators and switch mode generators the Class-GD system performs best.

3.4 Block Diagram of the Class-GD System

The Class-GD ultrasonic generator consists of three main building blocks. The first is the power control block. Here energy is moved from the AC power outlet to the transducer. The second building block is the digital control system. Energy flowing in the power control system is monitored and controlled according to pre-programmed conditions. The final building block is the human interface. A user will be able to decide the type of control technique to be applied and the power needed at the transducer.

In order to achieve full power control, a multiple feedback path in the control loop is required to achieve maximum power transfer to the transducer. In addition, the Class-GD ultrasonic generator consisting of numerous control models, will also need controls. The complete system is, therefore, relatively complex. Thus a development path based on modules and layers was investigated.

A block diagram of the Class-GD ultrasonic generator is seen below in Figure 13.

To ensure maximum flexibility, a digital system was chosen. The system would operate according to conditions and instructions that can be programmed in a software platform. The system consists of five layers: the power layer, the power interface layer, the signal layer, the control layer and the software layer.

1. **Power layer:** Controls the energy to the ultrasonic transducer.
2. **Power interface layer:** Prevents the EMI that is generated in the power layer from affecting the signal layer. This layer insures the optimal performance of the signal and control layer.
3. **Signal layer:** Is used for signal conditioning, comparison and conversion.
4. **Control layer:** Controls the modules.
5. **Software layer:** Provides supervisory control functionality.

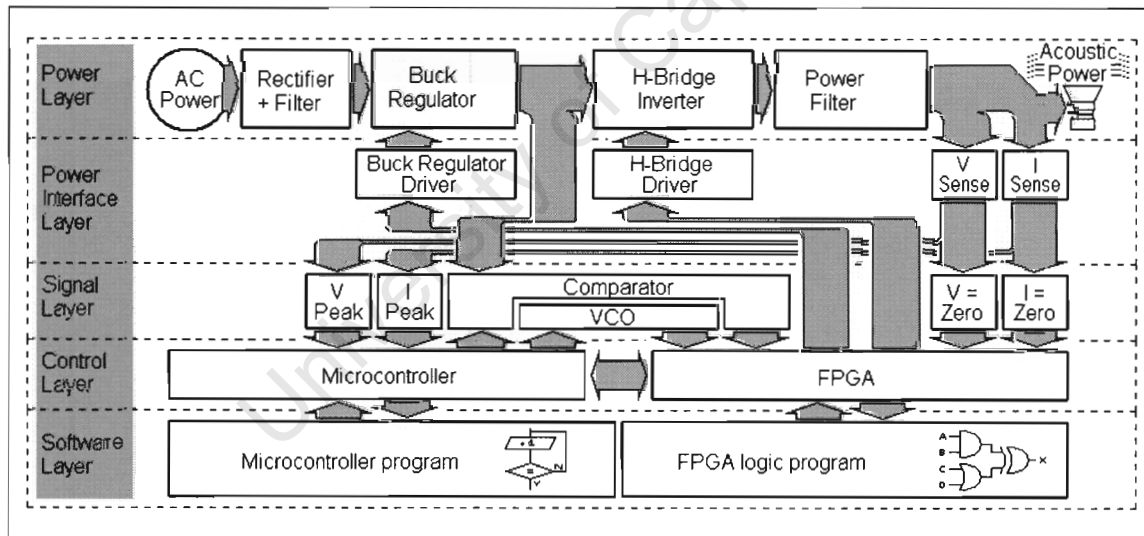


Figure 13: Block diagram of the Class-GD ultrasonic generator as described in this document

Chapter 4

Class-GD Ultrasonic Generator Sub-system Design

The Class-GD ultrasonic generator was designed as a universal digital ultrasonic generator. To achieve that goal it was necessary to include both voltage and current feedback loops with peak detection and zero-crossing detection circuits. Such circuits were required for varying types of ultrasonic control topologies. The complete system is, therefore, relatively complex. The development path was based on modules and layers.

4.1 Power Layer Selection and Design

The power layer (see Figure 14) controls the flow of energy from the AC power supply to the ultrasonic transducer; two active modules control the flow. The first is the buck regulator, the primary function of which is the control of voltage to an H-bridge inverter. A change of voltage supply to the inverter indirectly changes power delivered to the ultrasonic transducer.

The second active module is the H-bridge inverter. This module changes the DC voltage from the buck regulator to a high frequency modulated wave. The power filter then filters this modulated wave and the result supplied to the ultrasonic transducer resembles a sinusoidal waveform.

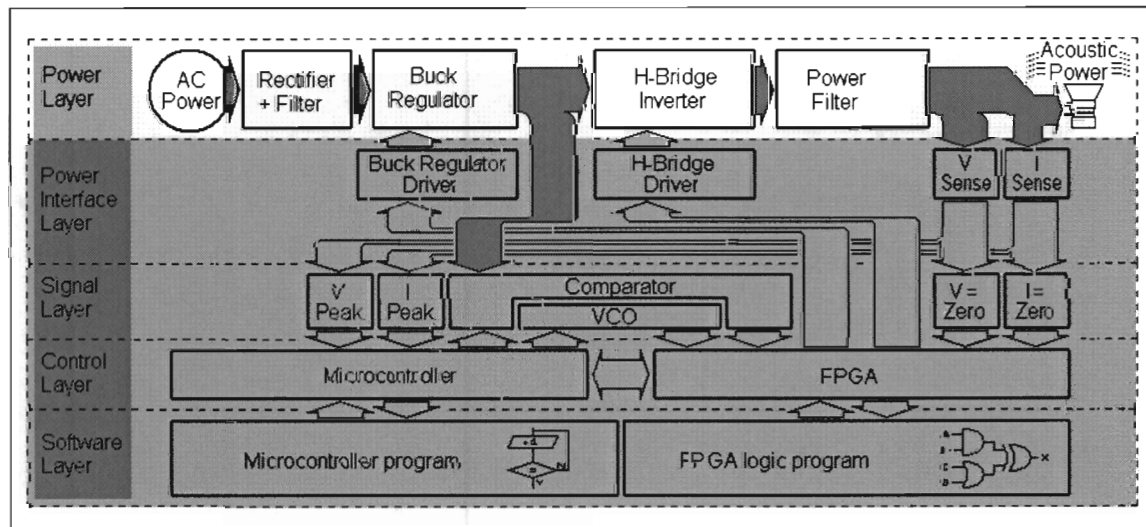


Figure 14: Power layer

4.1.1 Rectifier and Filter Design

This module converted the AC mains sourced from an AC supply into DC voltage; full bridge rectifier (DB1 in Figure 15) performed the AC to DC conversion. The pulsating DC voltage was filtered by a capacitor (C1 in Figure 15). A SPST switch (SW1 in Figure 15) supplied and interrupted power to the Class-GD ultrasonic generator. A fuse (F1 in Figure 15) provided over-current protection.

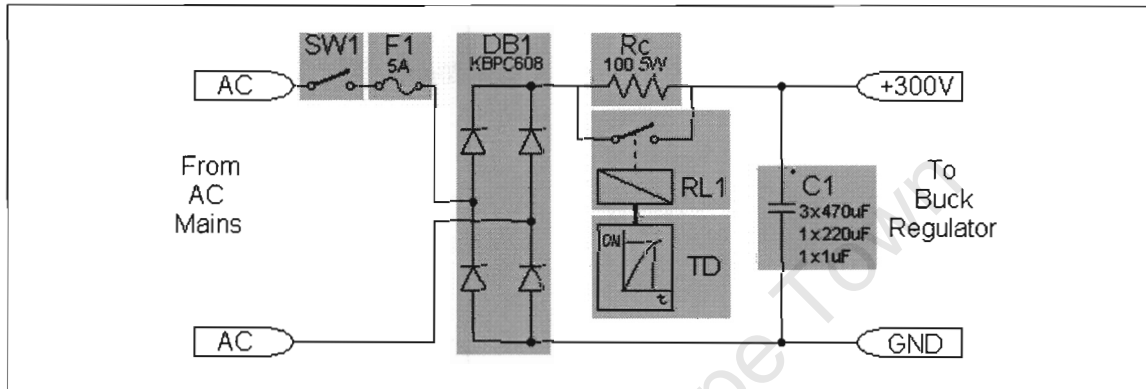


Figure 15: Input switch, rectifier and filter. The component calculation is in Appendix C1

Implementation

Capacitor C1 was unable to respond to high current transients and was replaced by two capacitors $C1_{LF}$ and $C1_{HF}$. The fuse (F1 in Figure 15) acted as a secondary protective device. An electronic circuit was added to detect over-current conditions, then shutting down both buck regulator and HI-bridge inverter modules.

4.1.2 Buck Regulator Design

The buck regulator was used to change the approximately 300V DC supplied by the rectifier and filter module, to a lower DC voltage. The output voltage varied from 0V to 250V DC and was achieved by changing the duty cycle of the MOSFET (M1 in Figure 16). The MOSFET (M1) reduces the 300V, depending on the duty cycle, to a lower average voltage. This chopped voltage wave was then filtered by the inductor (L1) and capacitor.

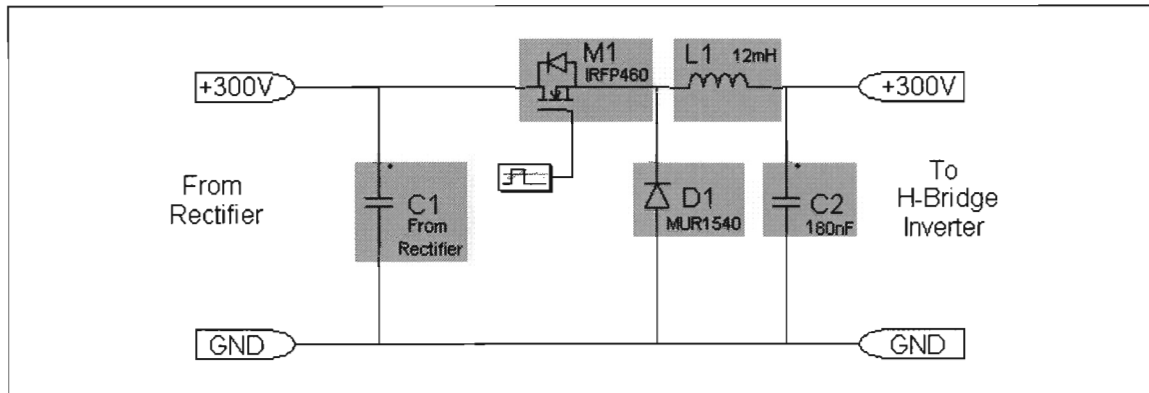


Figure 16: Buck regulator and filter. The component calculation is in Appendix C2

Implementation

Additional time was spent on the design of the buck regulator to ensure short lead lengths and to minimise EMI radiation. The high frequency capacitor (C1) was placed close to the MOSFET (M1) for that purpose. A 15V zener diode was placed from the gate to the source of the MOSFET (M1) to ensure reliable operation. Capacitor C2 was increased in size to a 2 μ F capacitor. The increase in capacitor size reduced the response time, but significantly improved system stability.

4.1.3 H-bridge Inverter Design

This module performed the function of converting the DC voltage from the buck regulator into a sinusoidal pulse width modulated AC voltage. A full bridge inverter (Figure 17) performed this DC to AC conversion. The inverter controlled the frequency and shape of the voltage to the load, but not the magnitude of the output waveform. The buck regulator module determined output magnitude.

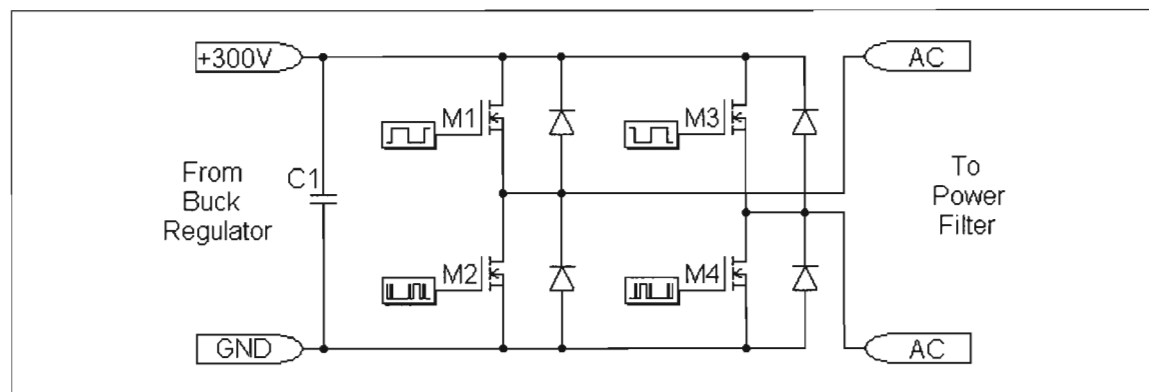


Figure 17: H-bridge inverter

A digital Sinusoidal Pulse-width modulation (SPWM) technique with unipolar voltage switching was chosen. A simulation package SIMCAD, was used for a better understanding of the operation of the circuit. In Figure 18 is the schematic as entered into SIMCAD.

The three square wave generators, and the XOR, NOT and two AND gates to the left in Figure 18 were used to generate the unipolar digital SPWM. The load was designed to resonate at about 25 kHz and to simulate the real load.

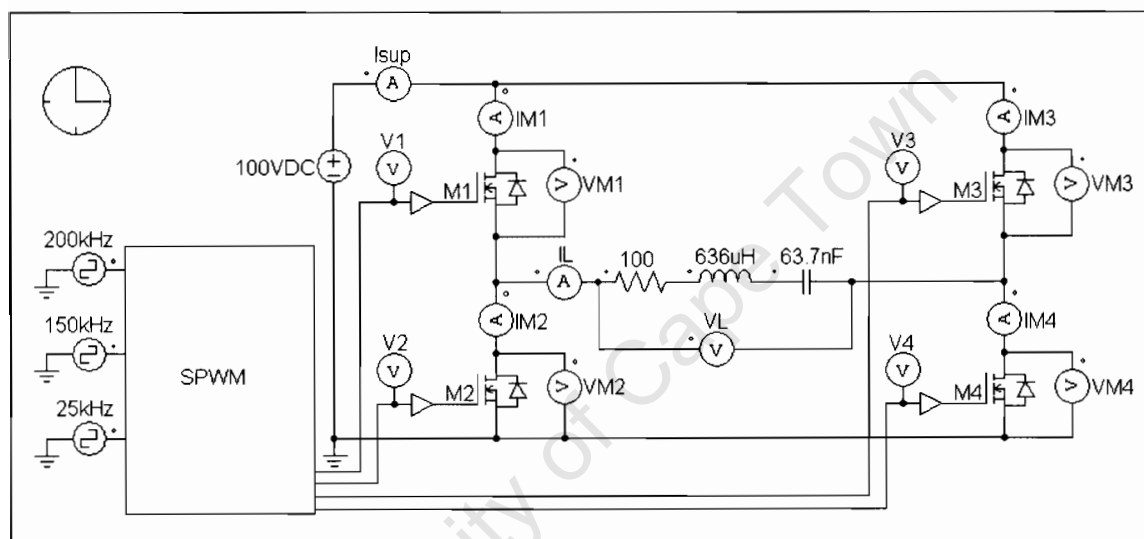


Figure 18: SIMCAD schematic of the H-bridge inverter stage

Figure 19 shows the simulated waveforms used to drive the MOSFETs in the inverter circuit. Signal V1 switched M1 on when high and signal V4 switched M4 on when high. MOSFETs 1 and 4 were used to generate a positive output voltage and MOSFETs 2 and 3 to generate a negative output voltage. As a result, signal V3 had a similar shape to signal V1, except that they were 180° out of phase, and signal V2 had a similar shape to signal V4 except, that they were 180° out of phase. Signal IL was the simulated load current.

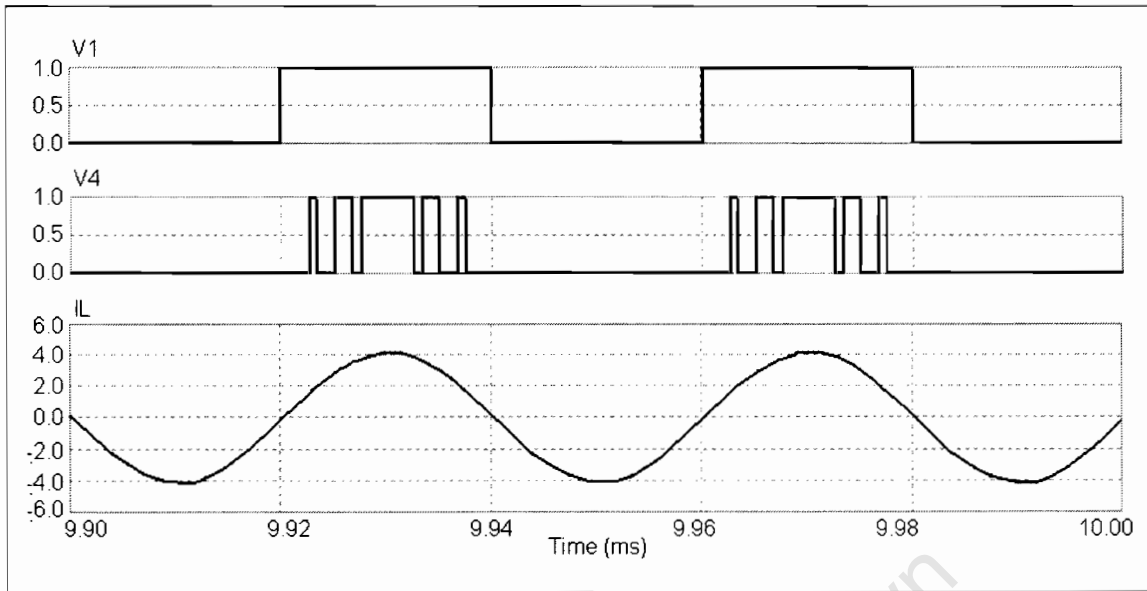


Figure 19: SIMCAD waveforms of MOSFET gating signals and load current. MOSFETs 1 and 4 are used to produce a positive voltage across the load. V1 drives MOSFET 1 and is switched at 25 kHz. The SPWM signal V4 drives the MOSFET 4 and is used for wave shaping. IL shows the load current to the resonant load.

Figure 20 shows the current signals in MOSFETs 1, 3 and 4. The waves were selected to demonstrate the commutation paths in the inverter circuit.

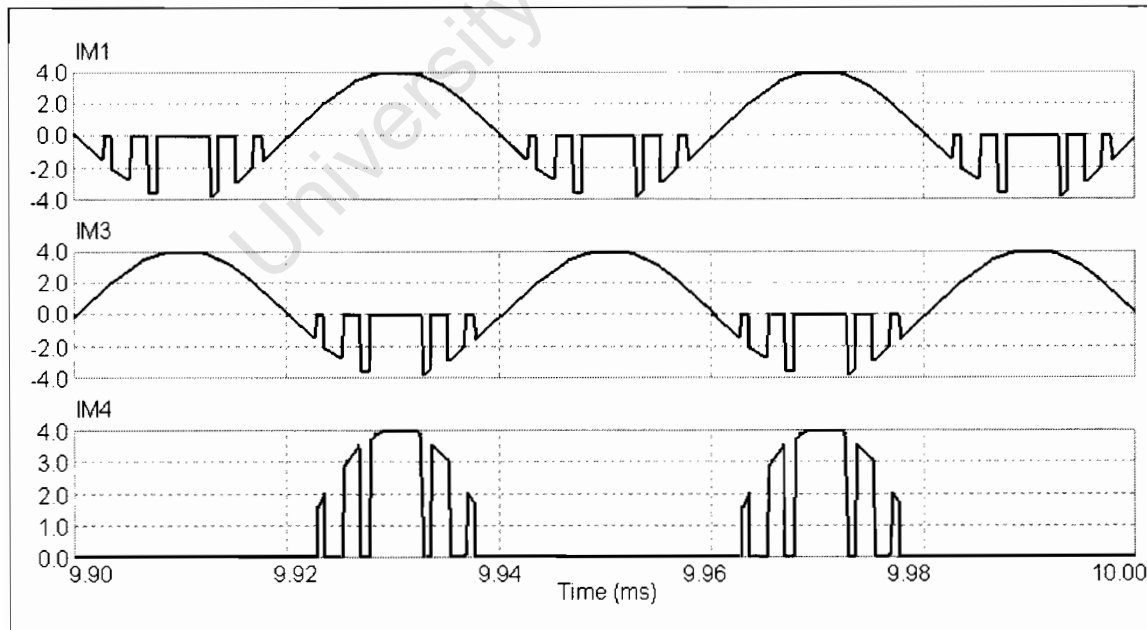


Figure 20: SIMCAD waveforms of MOSFET current. For the positive load cycle, MOSFET 1 is switched on allowing current to flow, and MOSFET 4 is switched on allowing current to flow. When MOSFET 4 is switched off, the diode in MOSFET 3 will conduct resulting in a negative current in MOSFET 3. The diode in MOSFET 3 thus provides a path during the commutation interval.

From Figure 20 we are able to make the following observations for the positive current cycle:

- When M1 and M4 were on (as seen in Figure 21A) current flowed from the 300V terminal through M1, the load and M4 to the ground terminal, while charging the resonant load.
- When M1 is on and M4 is off (as seen in Figure 21B) current flowed through M1, the resonant load and the internal diode of M3.
- When M1 and M4 were on (as seen in Figure 21C) the process was repeated.
- The switching frequency of M1 and M3 was equal to the load frequency of 25 kHz.
- The switching frequency of the internal diodes for M1 and M3 were about five times higher than the load frequency.
- The switching frequency of M2 and M4 were about five times higher than the load frequency
- The internal diodes of M2 and M4 did not conduct current.

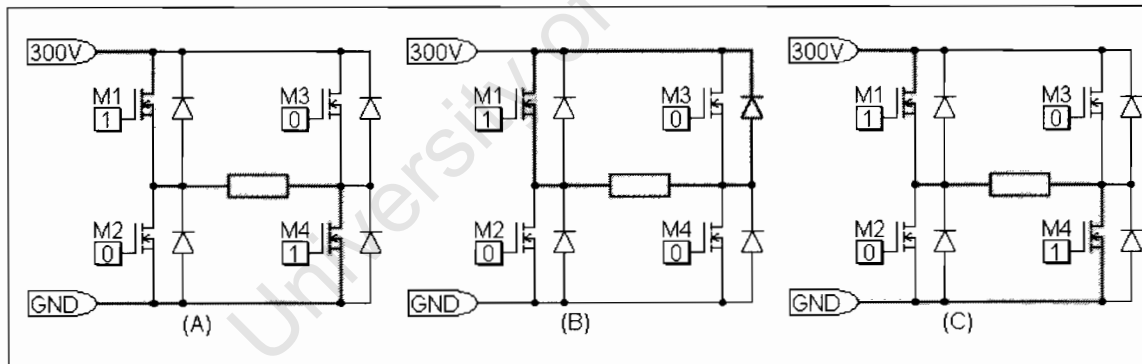


Figure 21: Positive cycle currents in an H-bridge inverter. Circuit A and C shows the current path used to charge the resonant load. Circuit B shows the current path during the commutation interval

The calculations needed to determine the power loss of the inverter circuit became reasonably complicated after considering switching, conduction, cross conduction and reverse recovery losses. Because of the complexity of switching conditions, a simulation programme ORCAD 10, determined power losses in the inverter circuit.

The simulations results are seen in Figure 22. From these results, we determined the inverter efficiency was about 75%.

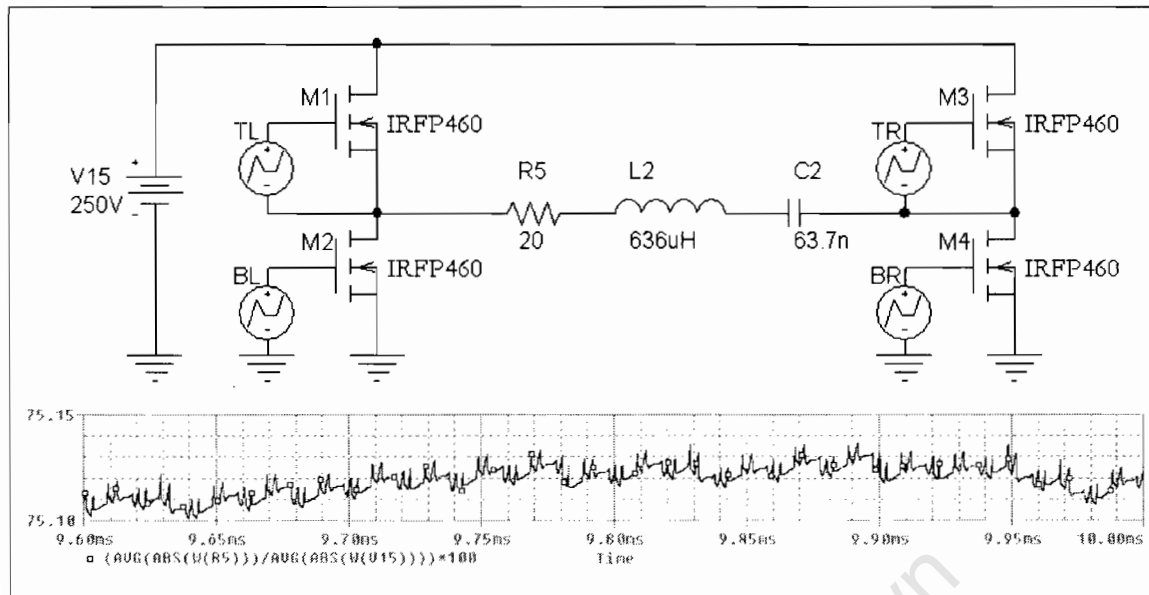


Figure 22: ORCAD simulation with switch average power loss

It was determined with further simulations that a large amount of power was wasted because of the reverse recovery time of the internal diodes of MOSFETs M1 and M3. Other configurations and switching devices were considered. Among these were FREDFETs. FREDFETs are MOSFETs with ultra-fast internal diodes. These devices would solve the reverse recovery time problem found with the previous circuit. They were, however, not selected because of the difficulty of sourcing the devices. An alternative was to use of IGBTs. The low frequency demand placed on MOSFETs M1 and M3 made IGBTs ideal candidates. The benefit of using IGBTs was that they came with higher voltage and current ratings, and ultra fast diodes built into the package. MOSFETs M2 and M4 were not replaced as IGBTs were not rated as high frequency devices, and would suffer from high switching power losses if subjected to the switching signals of MOSFETs M2 and M4.

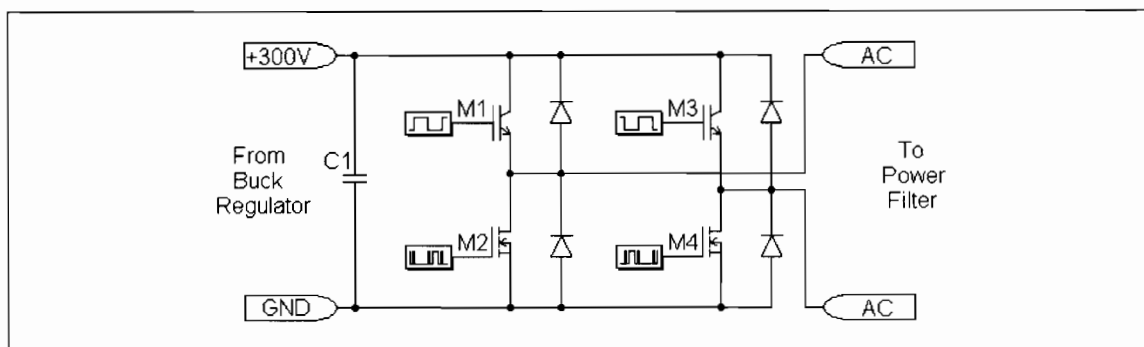


Figure 23: MOSFET and IGBT H-bridge hybrid

The new circuit shown in Figure 23 was simulated in ORCAD 10 to determine if the new circuit had lower power losses and improved efficiency.

The simulation results can be seen in Figure 24. From these results it was determined that the inverter efficiency was about 86.14%.

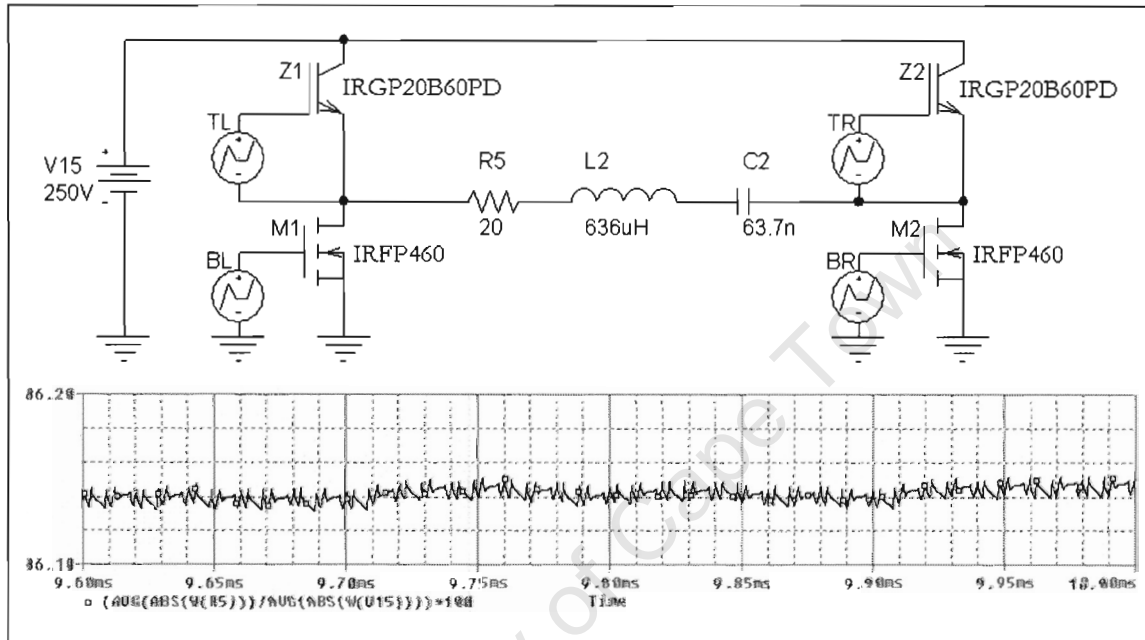


Figure 24: ORCAD simulation with switch average power loss. The component calculation is in Appendix C3

The new circuit shown in Figure 23 showed improved efficiency with regard to the circuit shown in Figure 17. The circuit shown in Figure 23 was thus used as the inverter module for the Class-GD ultrasonic generator.

Implementation

Additional time was spent on the design of the inverter circuit to ensure short lead lengths and to minimise EMI radiation. The high frequency capacitor (C1) was placed close to the switching pairs Z1 – M1 and Z2 – M2 to reduce EMI radiation. A 15V zener diode was placed from the gate to the source of the switches to ensure reliable operation.

4.1.4 Power Filter Design

A demodulation filter removed the high frequency SPWM switching component from the full bridge inverter, leaving only the desired output sine waveform across the load.

The following concept was used as a guide for the designing of the output filter.

1. The filter needed a constant amplitude and linear phase response within the required bandwidth (15 – 50 kHz). This minimised the distortion level in the load [28].
2. A passive filter was used to minimise power losses. The resistive element of the filter was the main cause of power dissipation and was minimised by careful design [28].
3. The filter was designed to attenuate the carrier frequency (modulating frequency) and its harmonics from the output waveform [28].

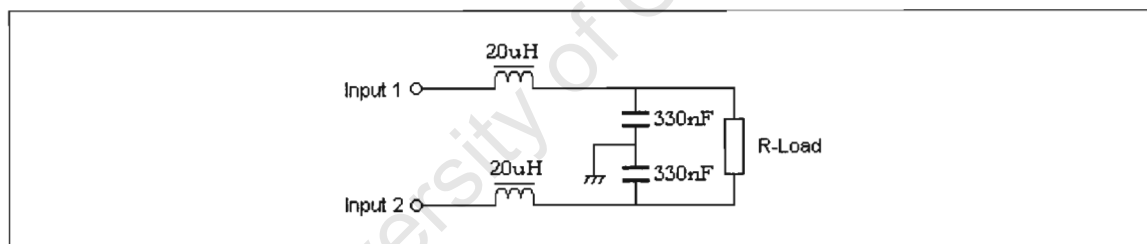


Figure 25: A balanced two-pole filter was used to reduce the EMI produced by the system [29].

The component calculation is in Appendix C4

The filter responded well to the operating bandwidth of 15 to 50 kHz and provided adequate attenuation of the switching frequency of 200 to 400 kHz.

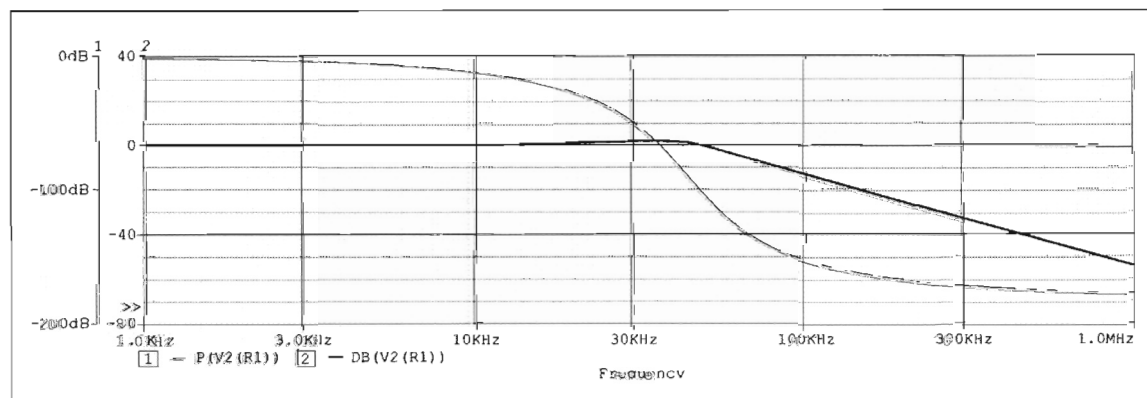


Figure 26 Filter frequency response

Implementation

The value of the capacitors were decreased from 330nF to 100nf. This value was found to give both lowest harmonic distortion and best response time.

4.2 Power Interface Layer Design

The power interface layer isolated the power layer from the signal layer. This ensured the reliable operation of the control circuit by protecting control circuit signals from the EMI generated in the power circuit (see Figure 27).

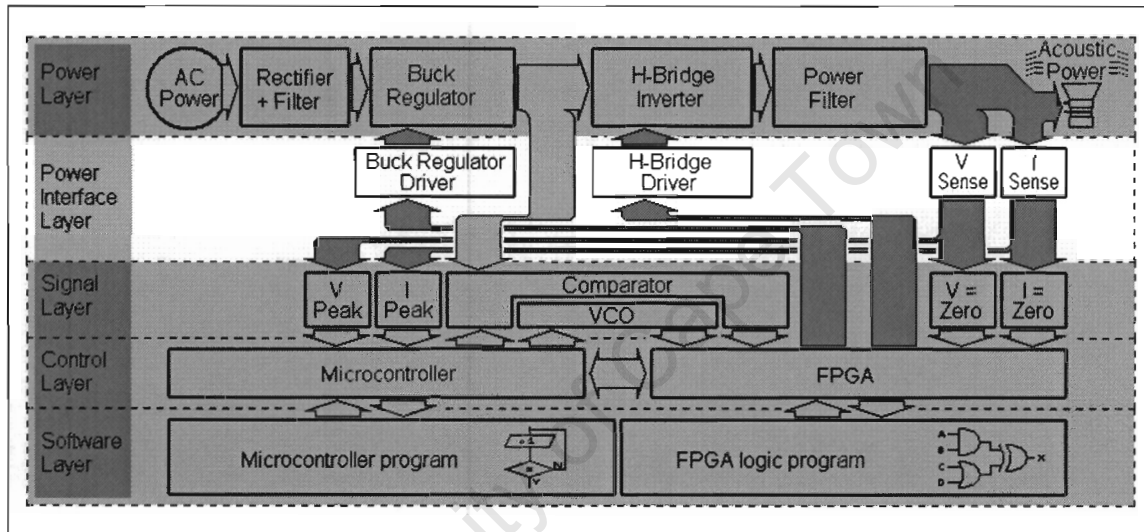


Figure 27: Power interface layer

4.2.1 Buck Regulator Driver Design

The buck regulator driver was used to change the 5V logic switching signal from the FPGA into a level shifted 15V signal to determine the switching state of the buck regulator MOSFET (see Figure 28).

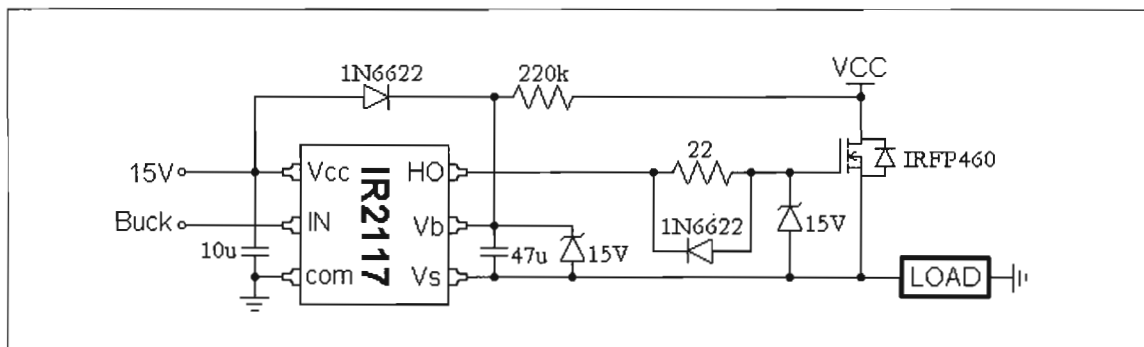


Figure 28: Buck regulator driver circuit. The component calculation is in Appendix C5

Implementation

The bootstrap capacitor was increased from 47nF to 100nF. This ensured reliable operation of the buck regulator.

4.2.2 H-Bridge Driver Design

The H-bridge inverter driver was used to change the 5V logic switching signal from the FPGA into a level shifted 15V signal to determine the switching states of the inverter MOSFETs and IGBTs (see Figure 29).

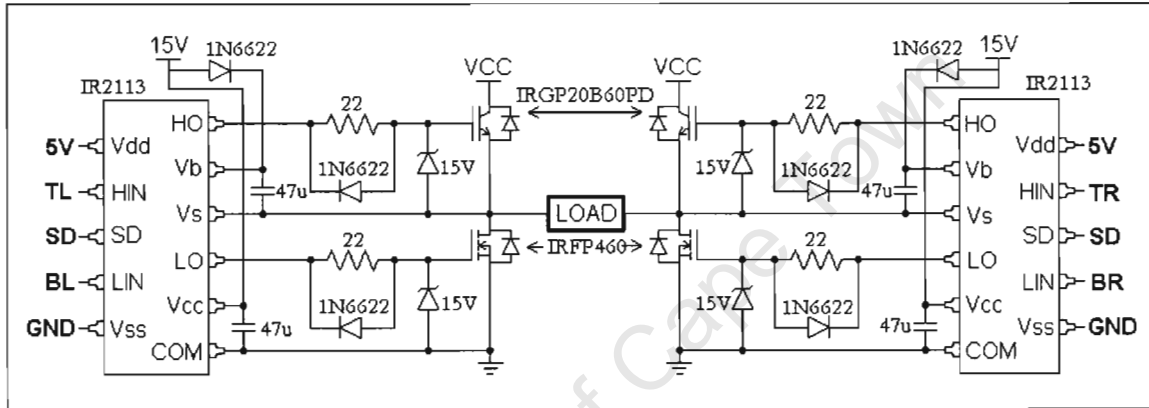


Figure 29: H-Bridge driver circuit. The component calculation is in Appendix C6

Implementation

The bootstrap capacitors were increased from 47nF to 100nF. This was done to ensure reliable operation of the inverter.

4.2.3 V and I Sensor Design

A current transformer (CT) was used to measure current flowing to the transducer. The CT changed the measured current of 0 to 10A into a voltage of 0 to 5V. The voltage was measured by the microprocessor via one of the internal analog-to-digital modules, where the 0 to 5V value is changed into an 8-bit digital value. A voltage transformer (PT) measured the voltage across the transducer. The PT changed the 0 to 220V measured across the load to 0 to 5V. This voltage was measured by a second analog-to-digital module where this voltage was converted to an 8-bit digital value (see Figure 30).

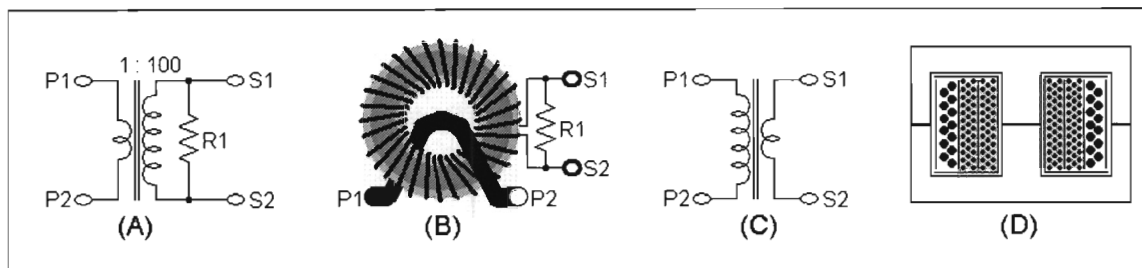


Figure 30: Current transformer and voltage transformer. The schematic of the CT is shown in *A* and the CT is shown in *B*. The schematic of the PT is shown in *C* and a cross sectional view is shown in *D*. The component calculation is in Appendix C7

Implementation

No problems were encountered with the voltage transformer, but the current transformer needed additional fine-tuning to calibrate the output voltage range.

4.3 Signal Layer Design

Signal conditioning and control were performed in the signal layer. Signal conditioning was performed by the V-Peak, I-Peak, V-Zero and I-Zero, where the voltage or current was changed to a signal type used by the microcontroller and FPGA, where the signal type to the microcontroller was 0 to 5V analog and the signal type to the FPGA was 5V digital. Control was performed by the comparator and the voltage-controlled oscillator (VCO). The comparator compared a 0 to 5V analog signal from the power layer with a 0 to 5V analog signal from the Microcontroller and drove the FPGA with a 5V digital signal. The VCO accepted an analog signal from the microcontroller and controlled the FPGA with a 5V digital signal (see Figure 31).

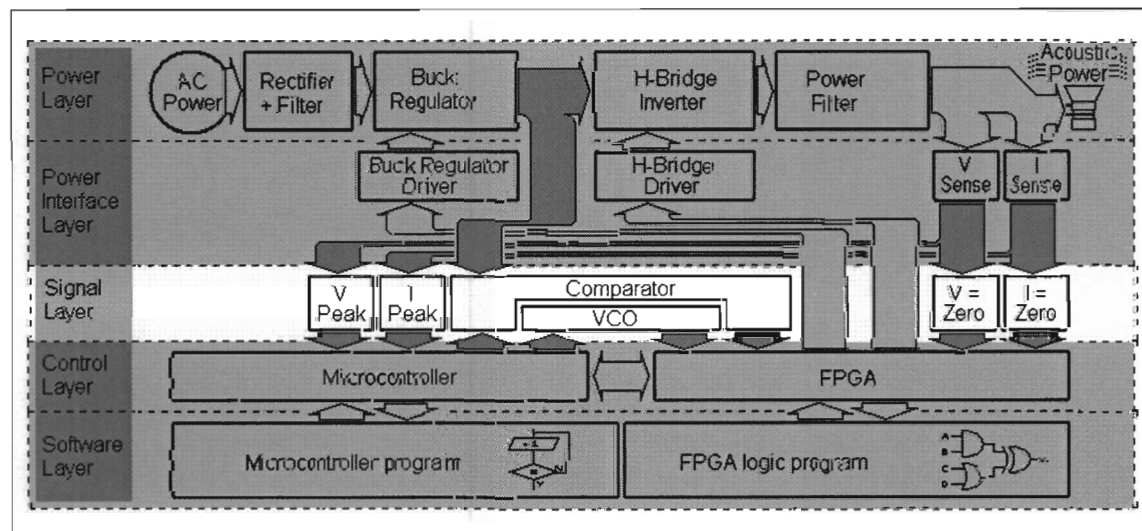


Figure 31: Signal layer

4.3.1 Voltage and Current Signal Conditioning

The voltage and current zero crossing detector was employed in the phase lock loop (PLL) control technique, as discussed in Chapter 4.5.5. The voltage and current peak detector was used in the admittance locking control technique, as discussed in Chapter 4.5.6 (see Figure 32).

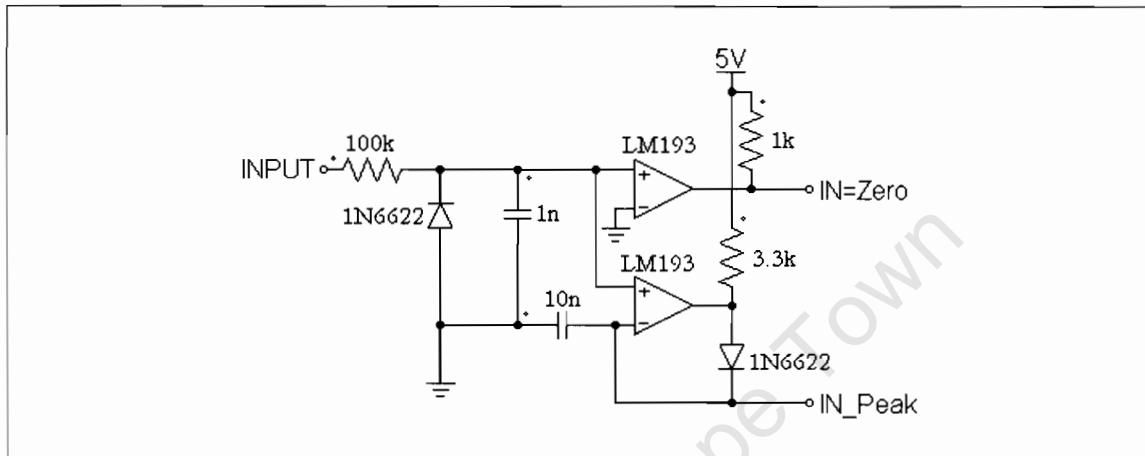


Figure 32: Voltage and current peak and zero crossing detection circuit. The transducer voltage or current is entered at the input of this circuit. The PLL uses the zero crossing detector signal at *IN=Zero* and the admittance locking control technique uses the peak detector signal at *IN_Peak*. The component calculation is in Appendix C8

4.3.2 Voltage Comparator

The voltage comparator compared the feedback signal from the power layer with the preset signal from the microcontroller, and drove the FPGA. This circuit formed an integral part of the buck regulator control circuit, as seen in Chapter 4.5.1 (see Figure 33).

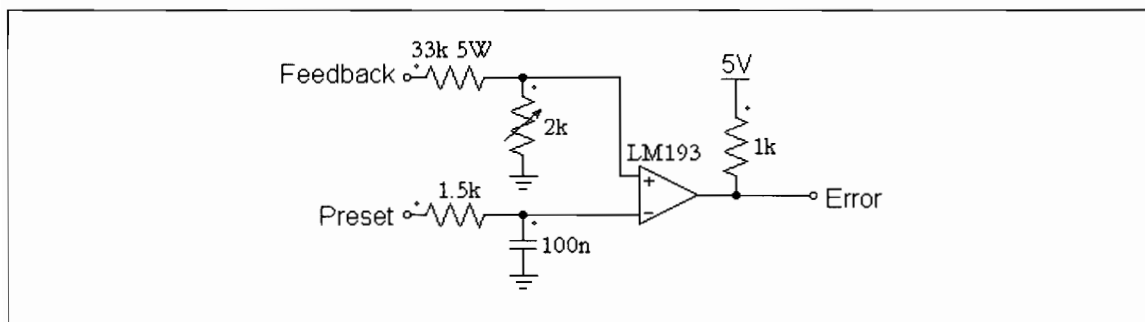


Figure 33: DC Bus-voltage comparator. The feedback signal from the buck regulator is compared with the preset signal from the microcontroller, and drives the buck regulator control program in the FPGA. The component calculation is in Appendix C9

4.3.3 Voltage Controlled Oscillator

The voltage-controlled oscillator (VCO) controlled the global clock frequency of the FPGA. A microcontroller changed the voltage at the “Freq con” input of the VCO resulting in a change in frequency at the “Freq OUT” output of the VCO. This circuit thus gave the microcontroller an ability to control the frequency of the transducer (see Figure 34).

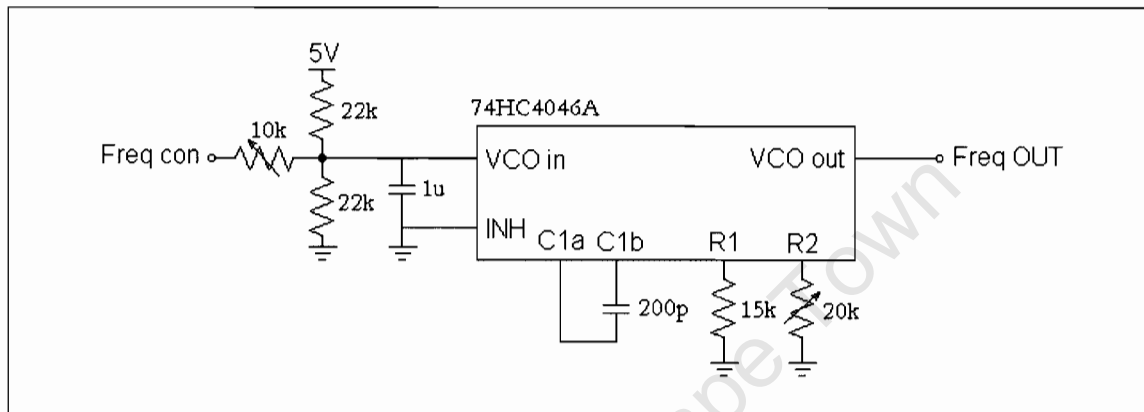


Figure 34: Voltage controlled oscillator. The component calculation is in Appendix C10

Implementation

Problems were encountered with this circuit. The VCO was unable to deliver the 4 to 6 MHz for which it was designed. The cause of the problem was bad PCB design. The PCB had long and wide tracks which added capacitance to C1, resulting in a lower VCO output frequency. There were two possible solutions: to re-design and re-populate the PCB, or to decrease the value of C1 and find the closest value of C1 to make the circuit work. The second option was selected.

4.4 Control Layer Design

The control layer consists of two reprogrammable controllers. The microcontroller determined the function of this device and method of operation. The FPGA performed most of the high-speed functions the microcontroller could not, and was used for power control and wave shaping. The controller type was selected based on the target market. The project was designed for University of Technology students, interested in ultrasonics and their control. The PIC microcontroller was the preferred microcontroller at the Cape Peninsula University of Technology in Cape Town. This resulted in the selection of the PIC16F876.

The functions of the microcontroller were to:

1. Inform the user by means of a 2x16 LCD display
2. Accept commands from the user by means of five buttons
3. Communicate with a personal computer (PC) via a RS232 port
4. Control the transducer output power by controlling the DC bus voltage
5. Control the transducer frequency by controlling the VCO
6. Setting the frequency range of the ultrasonic generator
7. Drive the ultrasonic transducer according to a pre-programmed control topology
8. Perform pre-programmed functions

The functions of the FPGA were to:

1. Generate a sinusoidal pulse width modulation signal
2. Drive the H-Bridge inverter
3. Drive the buck regulator
4. Phase detection (lead/lag)
5. Fault detection and shutdown

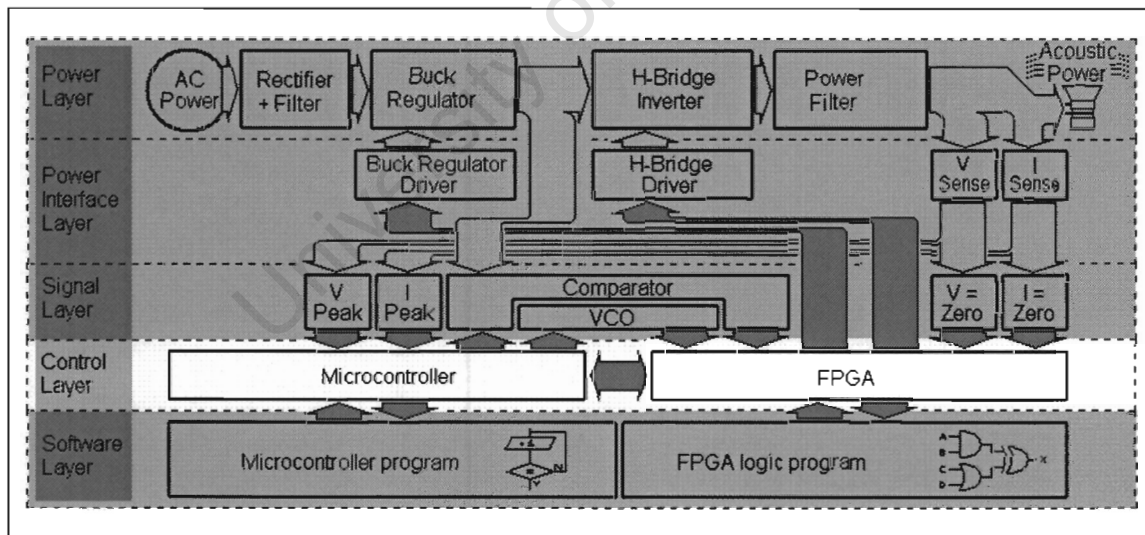


Figure 35: Control Layer

In Figure 36 it may be seen how the microcontroller and the FPGA were connected to the circuit. The microcontroller (PIC16F876) drove an LCD display used to display a menu which the user could navigate via push buttons.

Information could be logged and stored on a personal computer by means of the RS232 port. The ultrasonic generator could also be controlled by means of the RS232 port. The ultrasonic generator was improved by means of firmware updates programmed through the RS232 port.

The microcontroller sent the frequency range serially to the FPGA via the **FREQ RANGE DATA** and **FREQ RANGE CLK** lines. The microcontroller was able to measure the transducer frequency by means of the **FREQ MEASURE** line and determine if the transducer current was leading or lagging the transducer voltage, by means of the **LEAD/LAG** line.

The microcontroller could control the FPGA global clock frequency and ultimately the transducer frequency by changing the voltage to the VCO.

A sinusoidal waveform was applied to the ultrasonic transducer by the FPGA driving the H-Bridge inverter using a SPWM signal.

Power was controlled to the ultrasonic transducer by monitoring the voltage to the H-bridge inverter. The voltage was controlled by the buck regulator, which in turn was controlled by the FPGA and indirectly controlled by the microcontroller.

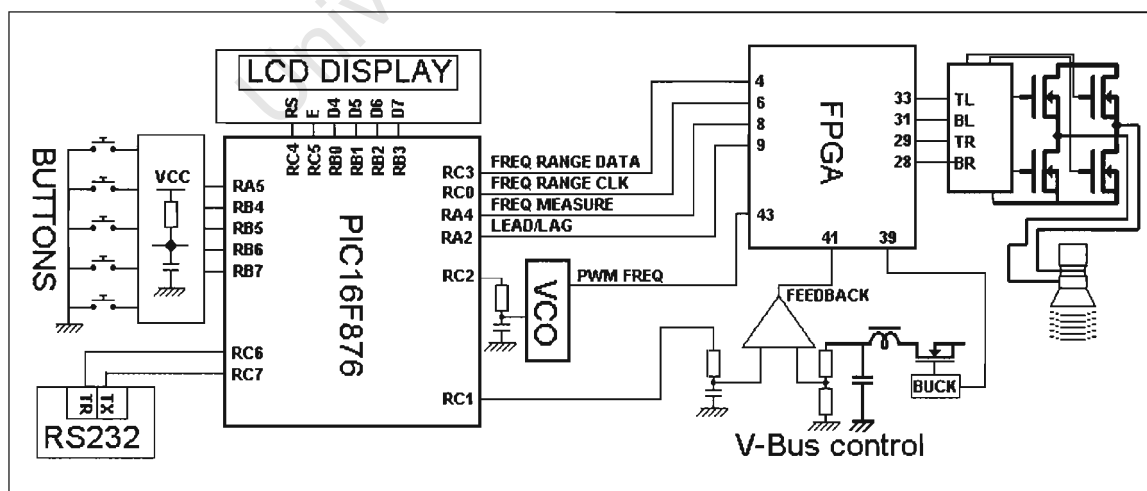


Figure 36: The Microcontroller with human interface and FPGA driving the inverter and buck regulator

4.5 Software Layer Design

The software layer determined the operation of the Class-GD ultrasonic generator. The microcontroller selected was a PIC16F876. The software code was written in the PIC Basic Pro language and designed in the MicroCode Studio Plus. This software package allowed the software designer to perform complicated functions with a single command statement as seen in Appendix C13.5. The FPGA software code was written in the Graphic mode of the ALTERA MAX +plus software. This software allowed the software designer to write his programme by using logic symbols and mega-functions as seen in Appendix C14.

The test programme designed for the Class-GD ultrasonic generator gave the generator two main modes of operation. The first was manual mode, in which the user was able to control the voltage and frequency to the transducer by means of a menu-driven display and five push buttons. In this mode, the user was able monitor the transducer peak voltage, peak current, real frequency and VA.

Auto mode was a second mode of operation. The user had the option of selecting between three control techniques: peak admittance locking, triangle sweep frequency mode, and saw-tooth sweep frequency mode. Each control mode required the user to preset the bus voltage. The device then performed a scan to determine optimal frequency and frequency range for that specific transducer and load. During the scan data was sent to a PC via the RS232 port to generate a current versus frequency plot. The resonant frequency was displayed and the user given an opportunity to begin the process. The process began and the peak admittance automatically tracked according to a selected topology. The current and frequency was displayed on the LCD, and then sent to the PC for later analysis. The user had an opportunity to stop the process at any time.

4.5.1 DC Bus-voltage Control

The DC bus voltage referred to the voltage between the buck regulator and the H-Bridge inverter. By controlling the amplitude of the voltage to the inverter, one effectively controlled the amplitude of the AC sine wave of the inverter. This change in voltage across the transducer resulted in a form of power control for the transducer. Below in Figure 37 may be seen the modules highlighted that were used for power control.

The bus voltage was controlled in two ways. In auto mode the voltage set point was automatically controlled by the microcontroller according to pre-programmed function (power control). In manual mode the user was able to set the bus voltage in one volt steps between 0 and 250V.

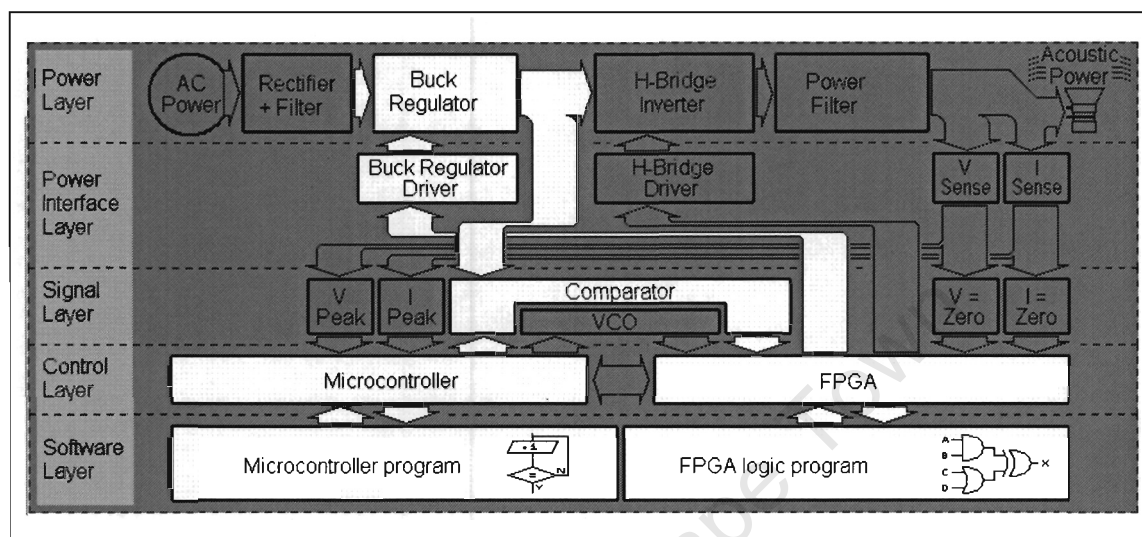


Figure 37: DC Bus-voltage control path

Figure 38 is a simplified circuit showing the operation of the buck regulator the microcontroller set the required output voltage (V_{setp}). The comparator (COMP) then compared the set point voltage from the microcontroller with the actual output voltage by means of the feedback circuit (FB). The error signal from the comparator was sent to the bang-bang controller in the FPGA. The bang-bang controller consisted of a clock signal ($\pm 75\text{kHz}$) to determine the period of the PWM signal, an AND gate and RS flip-flop. If the output voltage was too low and a clock signal received, the RS flip-flop would be set on. This in turn placed the MOSFET of the buck regulator in an “on” state. If the output voltage exceeds the set point voltage the RS flip-flop reset off and in turn placed the MOSFET in an “off” state. The MOSFET chopped the input voltage (300V), and the diode, inductor and capacitor filtered the chopped voltage waveform, leaving a near DC waveform. The output voltage was then delivered to the load.

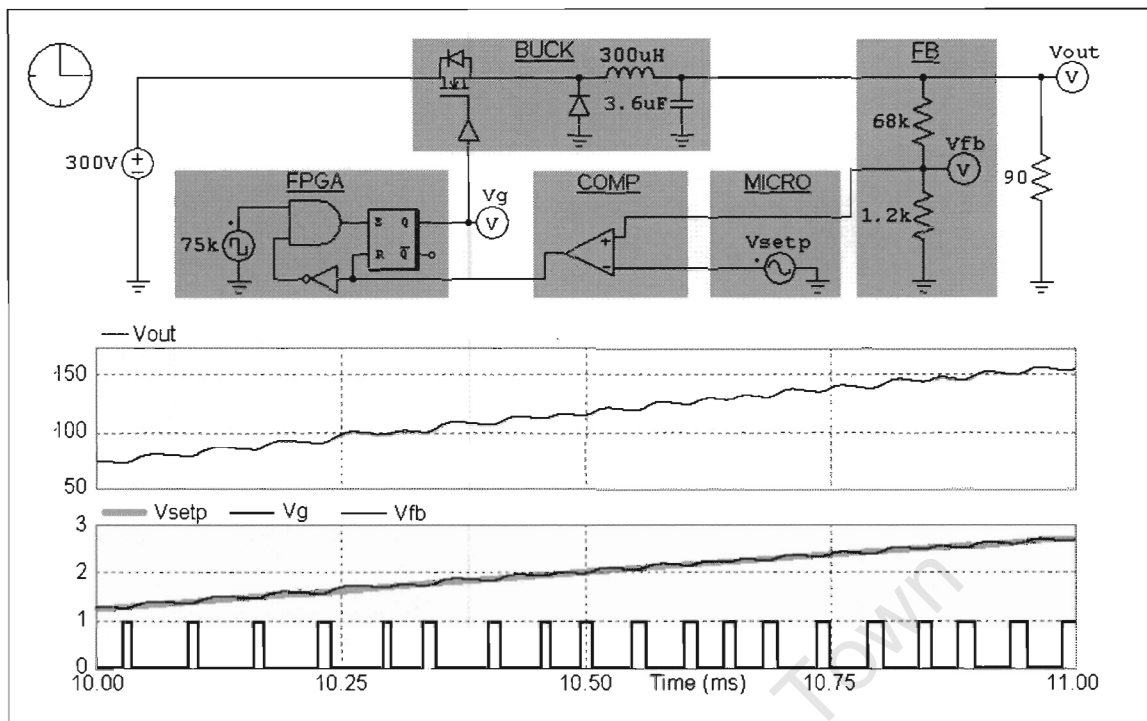


Figure 38: SIMCAD simulation of the Buck regulator. The output voltage (V_{out}) is determined by the voltage set by the microcontroller. The feedback voltage (V_{fb}) is compared to the set point voltage (V_{setp}) and the error signal from the comparator controllers the buck regulator program in the FPGA

The change in MOSFET duty cycle (V_g) can be clearly seen in Figure 38 above. One will also notice the MOSFET switched off when the feedback voltage (V_{fb}) exceeded the set point voltage (V_{setp}).

4.5.2 Frequency Control

To drive the transducer at optimal frequency a form of frequency control was required. The transducer frequency was determined by the operating frequency of the H-bridge inverter, in turn controlled by the SPWM signal generated by the FPGA.

The SPWM signal from the FPGA was controlled by two parameters set either by the microcontroller or by the user. The first is the frequency range. This parameter was set by serially shifting a 3-bit binary value from the microcontroller to the FPGA. These frequency ranges were used to improve the frequency resolution of the ultrasonic generator, resulting in small frequency steps of ± 20 Hz in the 25 kHz frequency range.

Frequency Range	Minimum frequency	Centre frequency	Maximum frequency
0 (000)	OFF	OFF	OFF
1 (001)	16 kHz	20 kHz	24 kHz
2 (010)	21 kHz	26 kHz	31 kHz
3 (011)	25 kHz	31 kHz	37 kHz
4 (100)	29 kHz	36 kHz	43 kHz
5 (101)	33 kHz	42 kHz	50 kHz

Table 6: FPGA frequency ranges

A second parameter was the frequency within the range. The microcontroller or user changed an 8-bit value in a hardware PWM port of the microcontroller. This controlled the voltage to the voltage-controlled oscillator (VCO) and in turn the frequency of the global clock of the FPGA and the SPWM signal. Below in Figure 39 can be seen the modules highlighted that were used for frequency control.

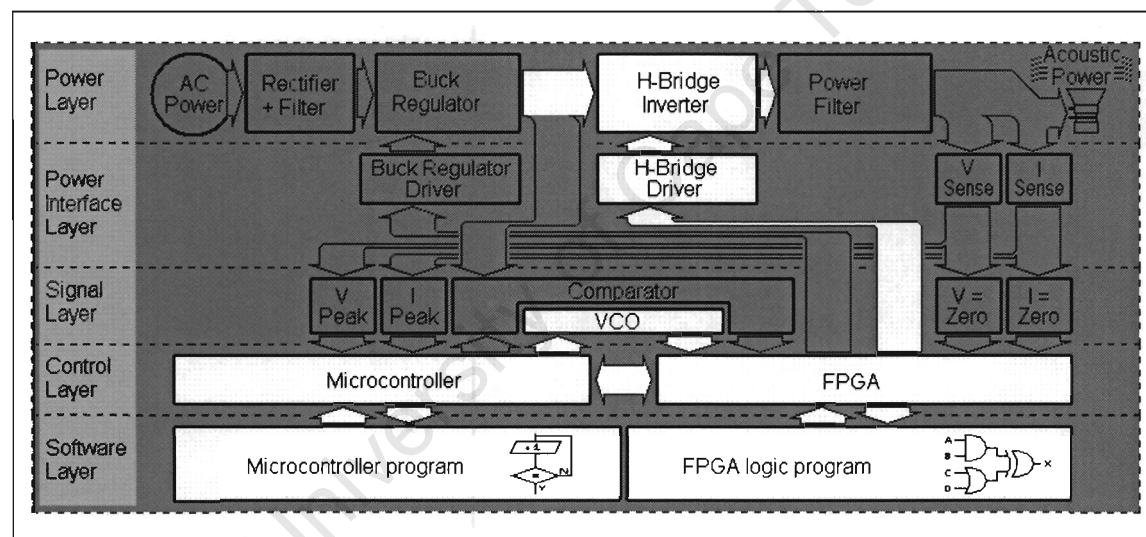


Figure 39: Frequency control path

4.5.3 Digital Sinusoidal Pulse-width Modulation (SPWM) control

Two conventional SPWM options were available. The first was an analog modulation technique where a sinusoidal control signal is compared with a repetitive switching-frequency triangle waveform in order to generate the switching signals. The second option, a digital modulation technique, utilizes a lookup table to generate the sinusoidal switching signal [22].

The main advantages of a digital approach over analog are:

- Lower sensitivity to changes in temperature, supply voltage fluctuations and aging of components [22].
- Reduced part count and increased reliability [22].

A novel digital open loop sinusoidal pulse-width modulation technique was developed for this project. This bipolar technique utilises a beat frequency technique. This was achieved by XORing two digital square waves with different frequencies. The resultant frequency was equal to the difference between the two frequencies.

In Figure 40 may be seen a SIMCAD simulation for the novel bipolar digital sinusoidal pulse width modulation technique. Two signals are used to generate the 50Hz digital SPWM signal, a 300 Hz, 50% duty cycle and a 350 Hz, 50% duty cycle. The XOR gate extracted the SPWM waveform from these signals, and with the help of a NOT gate we can generate the switching signals for the H-bridge inverter.

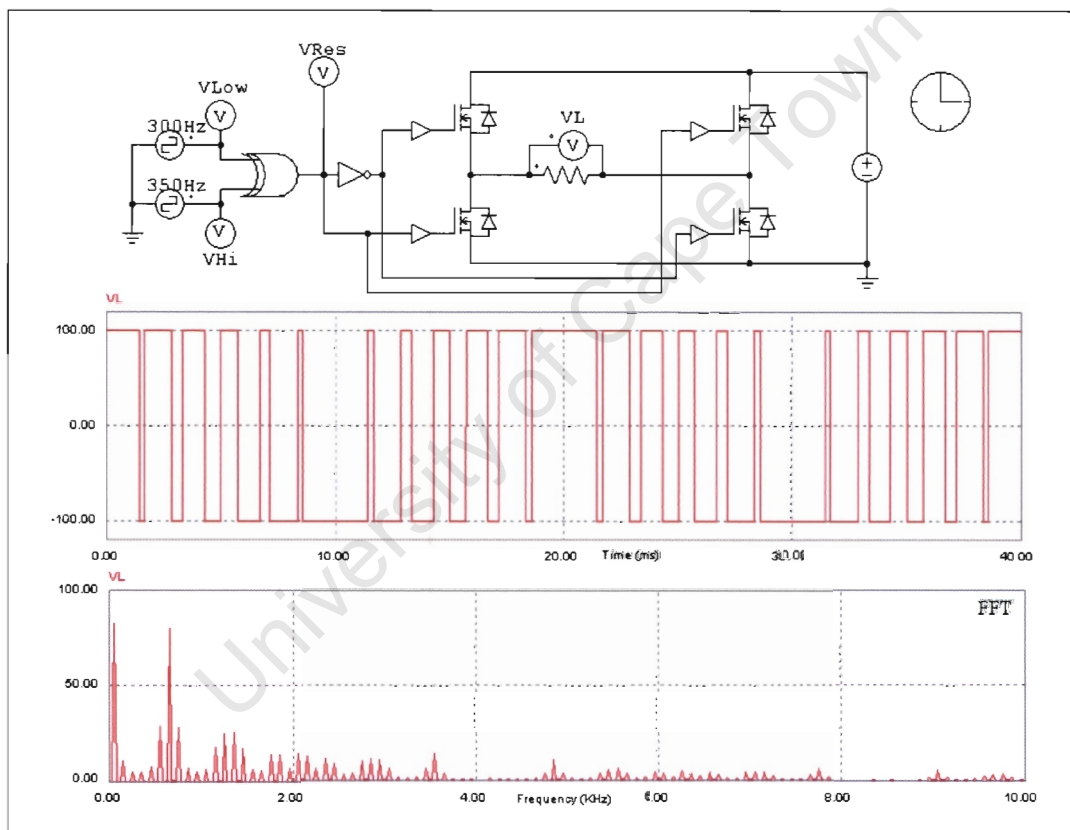


Figure 40 Digital bipolar SPWM circuit with load voltage waveform and FFT of the load voltage

In Figure 41 may be seen a SIMCAD simulation for the novel unipolar digital sinusoidal pulse width modulation technique. Three signals are used to generate the 50Hz digital SPWM signal: 300Hz, 350Hz and 400Hz. Three XOR gates extracted the SPWM waveform from these signals, and with the help of an additional 50Hz signal and two

AND gates and a NOT gate we can generate the switching signals for the H-bridge inverter.

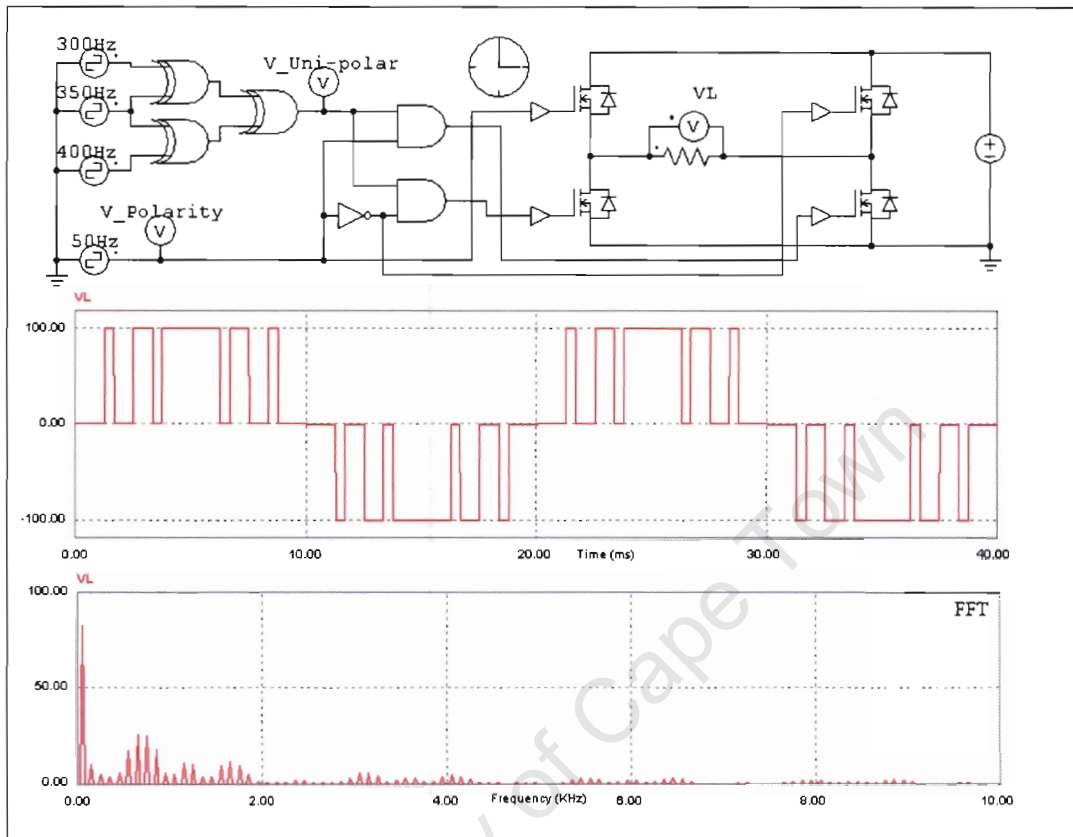


Figure 41: Digital unipolar SPWM circuit with load voltage waveform and FFT of the load voltage

The digital unipolar SPWM technique was used for this project as it generated less harmonic distortion after the output filter attenuated the switching frequency.

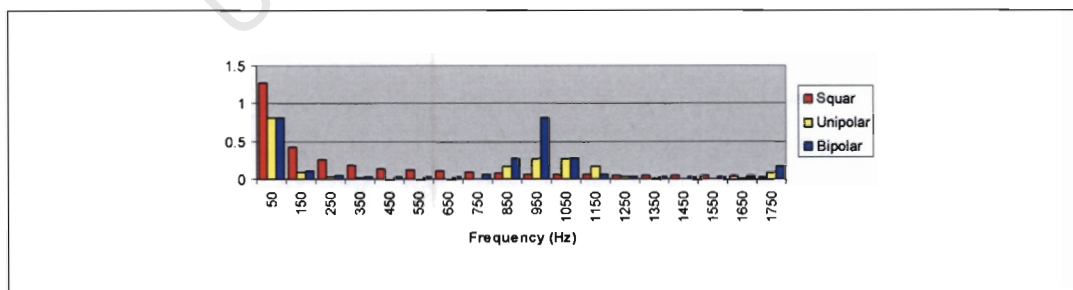


Figure 42: FFT of a Square-wave, Unipolar and Bipolar SPWM signal

4.5.4 Implementing Auto Transducer Frequency Detect

Each ultrasonic transducer has its own optimal operating frequency as seen in Appendix B1. This optimal transducer frequency showed a tendency to move when subjected to a load as seen in Appendix B2 and B3.

The Class-GD ultrasonic generator was designed with predetermined frequency ranges and required an auto-transducer frequency detection sub-routine in the ultrasonic generator programme to determine at which frequency range the transducer operated.

This subroutine was used during fault finding to determine the presence of an ultrasonic transducer, and the condition or health of the ultrasonic transducer. During that subroutine it was also possible to determine if the output leads of the transducer were shorted, leading to system shutdown and fault indication.

The complete transducer auto detect subroutine may be seen in Appendix C13.1 and C13.5 line 766.

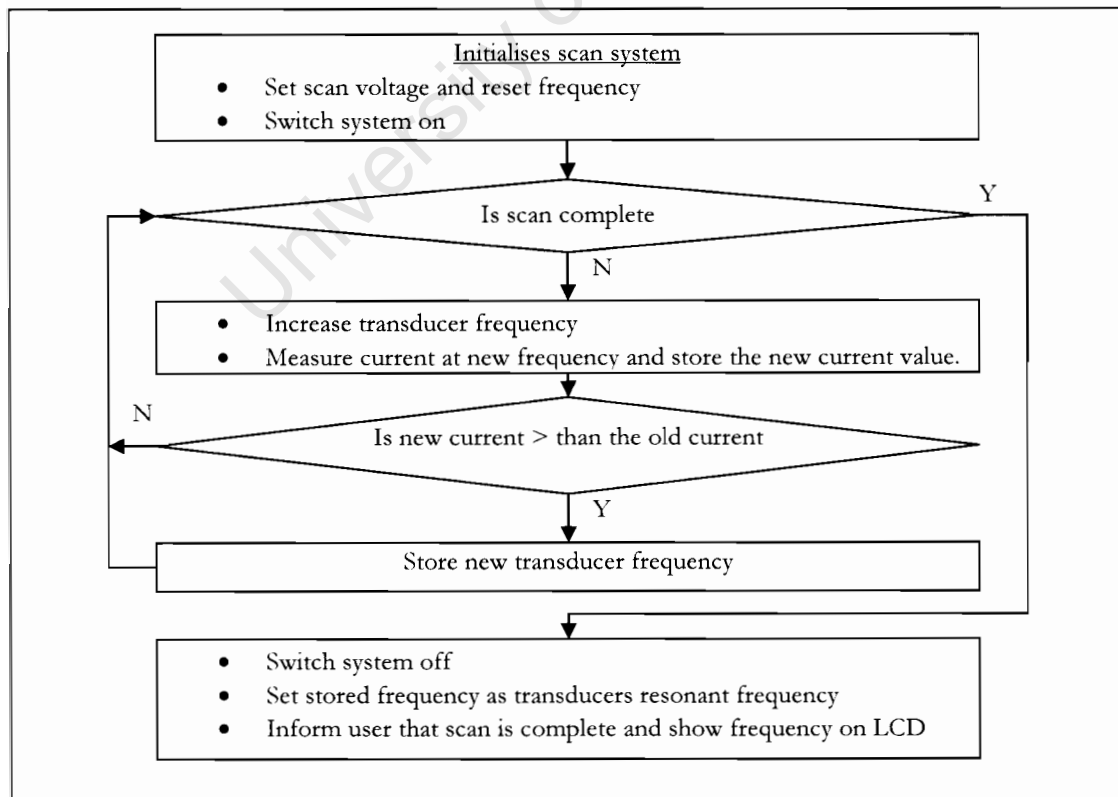


Figure 43: Simplified auto transducer frequency detect flowchart

4.5.5 Implementing phase-lock loop control

The transducer delivered the most power to the load when in series resonant mode. To determine if the transducer was at resonance, the voltage and current were monitored to check if they were in phase, and thus at resonance. The output frequency was determined by the microcontroller frequency range and set point.

In turn the FPGA generated the digital SPWM signal and drove the H-bridge inverter supplying the ultrasonic generator with a sinusoidal wave. The ultrasonic transducer then drew a current with some magnitude and phase with respect to the voltage; the V-Zero and I-Zero detected the zero crossing of the voltage and current. The FPGA determined if the current was leading or lagging the voltage before sending a high or a low to the microcontroller. The microcontroller then increased or decreased the frequency, while maintaining the phase around the lead/lag point at resonance.

The phase-lock loop control technique was abandoned after it was discovered that the current transformer added an additional phase shift in the current, making it impossible to perform phase lock loop control. This problem might have been solved with a new current transformer. A second and more serious problem encountered was that the voltage and current waveforms became less than ideal when the transducer was not at resonance. Multiple zero voltage and current transitions were detected when the transducer was off resonance. This was caused by harmonic distortion in the voltage and current waveforms. The problem might be solved with a improved power filter stage.

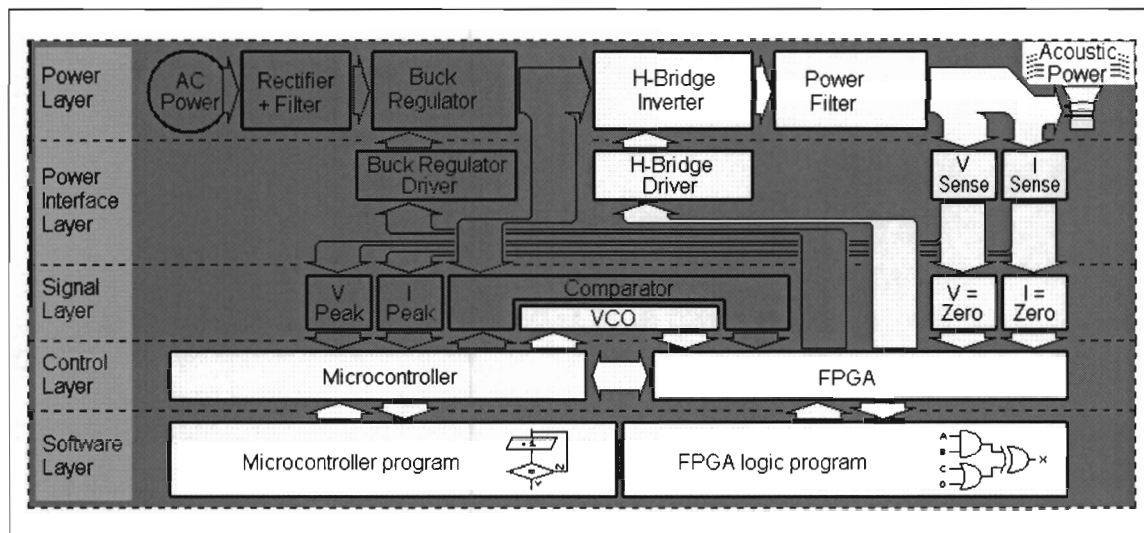


Figure 44: Phase-lock loop control path

4.5.6 Implementing Admittance Locking Control

The transducer delivered most power to the load when in series resonant mode or at the point of peak admittance. To determine if the transducer was at peak admittance, voltage was kept constant and current was monitored. The I-Peak detected the peak current value and supplied the microcontroller with peak current value. The microcontroller then increased and decreased the frequency while maintaining the voltage constant and determining if peak admittance point had moved to a different frequency value.

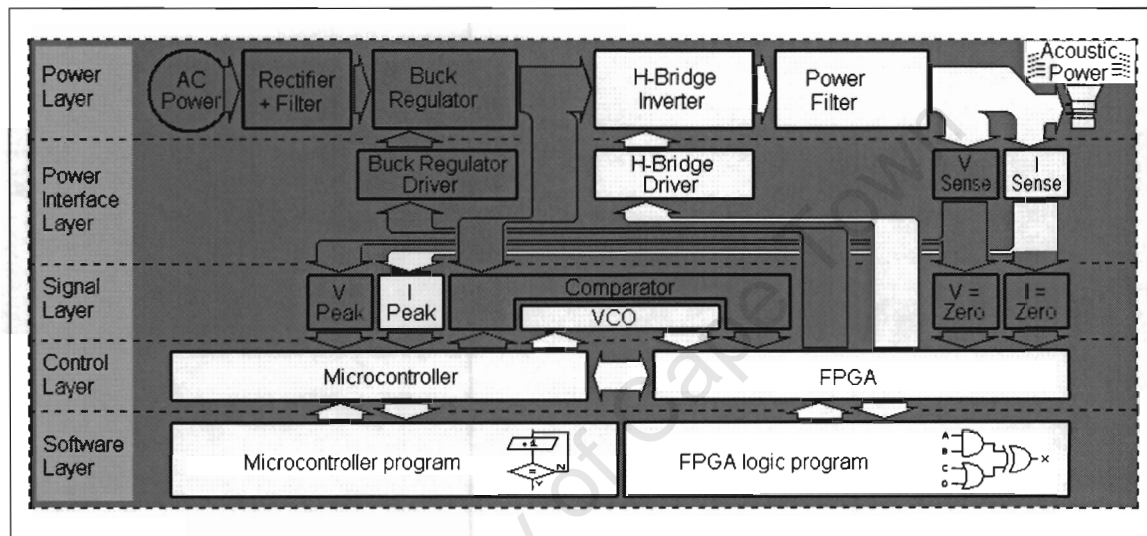


Figure 45: Admittance locking control path

Below in Figure 46 may be seen the basic operation of the admittance locking control technique.

1. The microcontroller increased the frequency and compared the new current with the current at f_c . When the new current was lower,
2. The microcontroller decreased the frequency and compared the new current with the current at f_c . If the new current was lower,
3. The frequency was increased to its original frequency.
4. The system tracked peak admittance by staying at the new current and restarting the scan from the new f_c frequency.

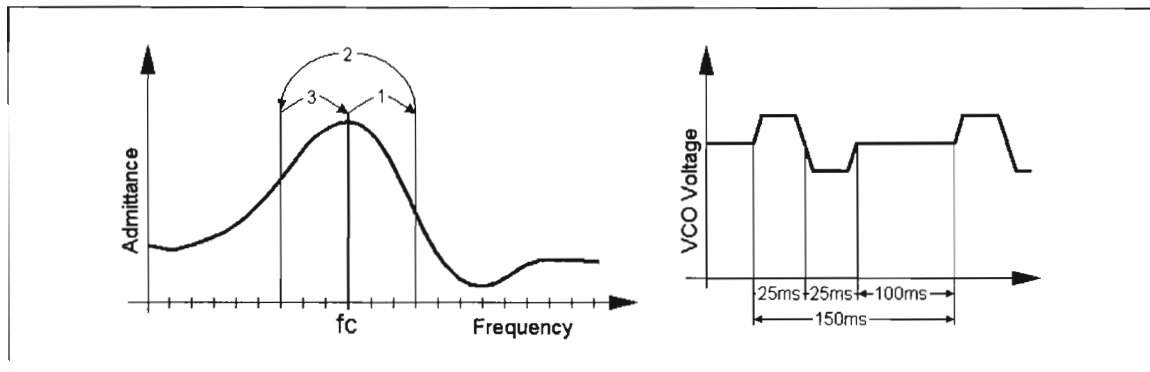


Figure 46: Admittance locking control technique will test left and right of f_c to determine if the admittance has moved. The VCO voltage controls the frequency; 50ms is used for the peak detection and 100ms is used to deliver power to the load at its optimal frequency

The complete admittance locking subroutine can be seen in Appendix C13.2 and C13.5 line 507.

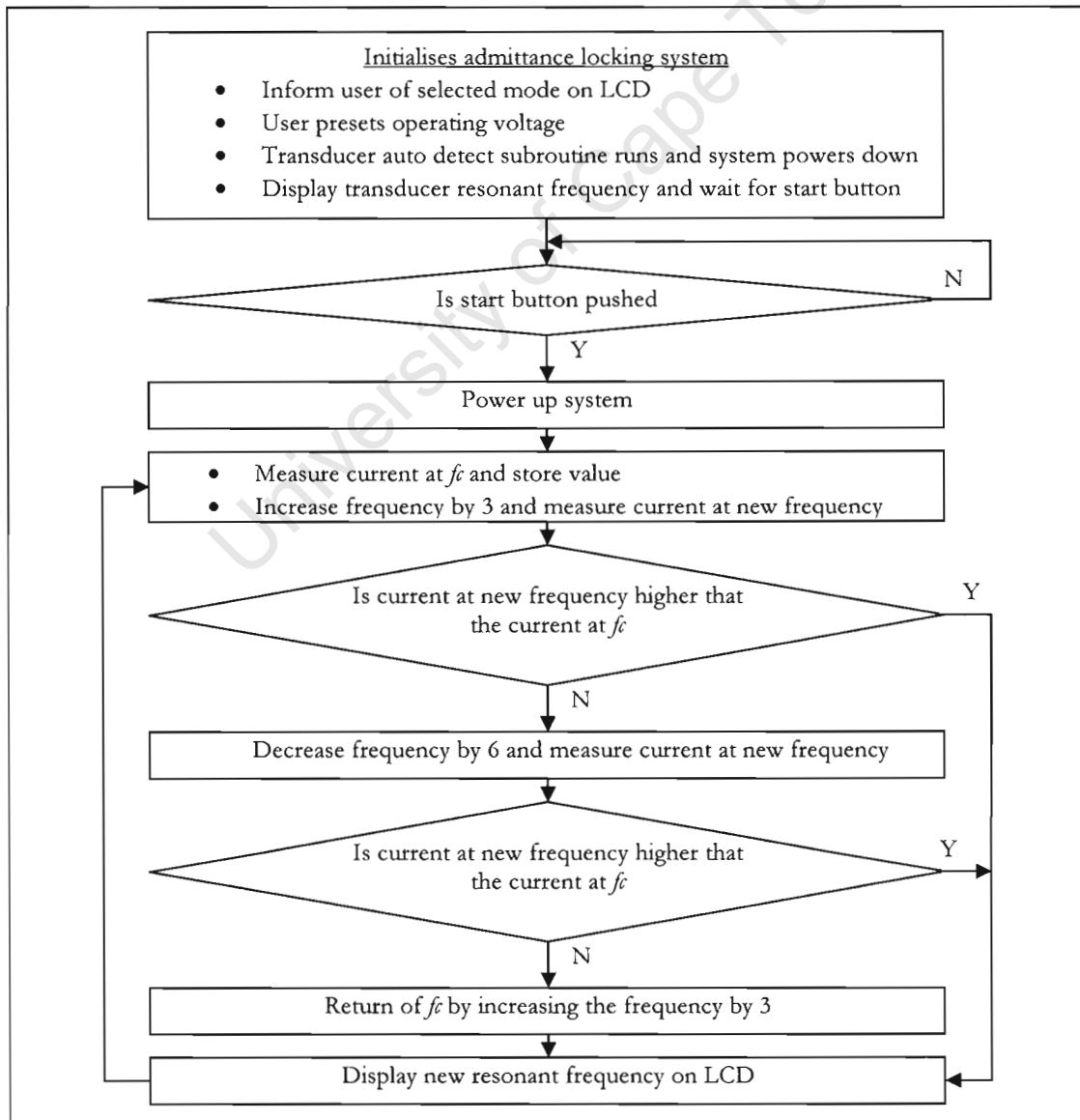


Figure 47: Simplified admittance locking flowchart

4.5.7 Implementing the frequency modulation technique

Two sweep frequency modulation techniques were investigated for this project.

In Figure 48 may be seen the basic operation of the saw-tooth locking control technique.

1. The microcontroller decreased the frequency to five frequency set points below the centre frequency f_c as detected by the transducer auto-detect scan sub-routine.
2. The microcontroller increased the frequency and compared the new current with the previous current value and stored the highest value; performed 10 times.
3. The microcontroller then decreased the frequency to five frequency set points below the new peak admittance value then went to step two.

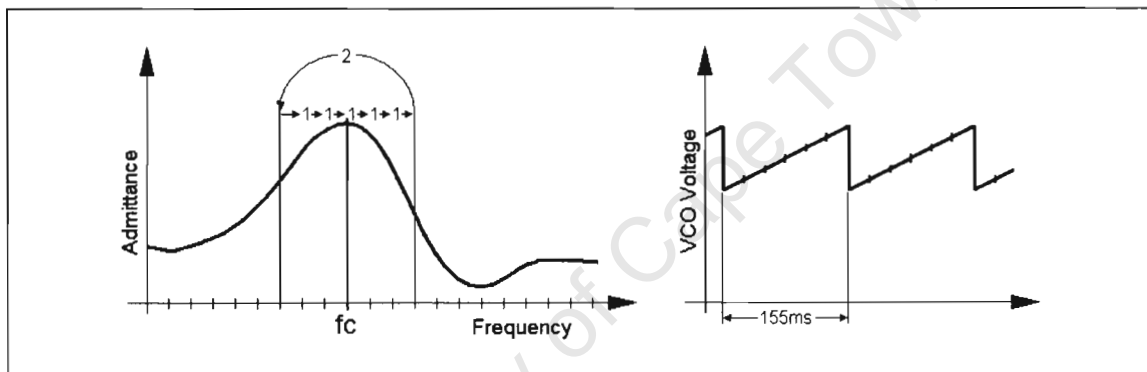


Figure 48: Saw-tooth locking control technique showing the frequency sweep and repetition period

The saw-tooth locking control sub-routine may be found in Appendix C13.3 as a flowchart and the microprocessor code examined in Appendix C13.5 line 574.

In Figure 49 is shown the basic operation of the triangle locking control technique.

1. The microcontroller decreased the frequency to five frequency set points below the centre frequency f_c as detected by the transducer auto detect scan sub-routine.
2. The microcontroller increased the frequency and compared the new current with the previous current, value before storing the highest value; performed 10 times.
3. The microcontroller then slowly decreased the frequency to five frequency set points below the new peak admittance value before going to step two.

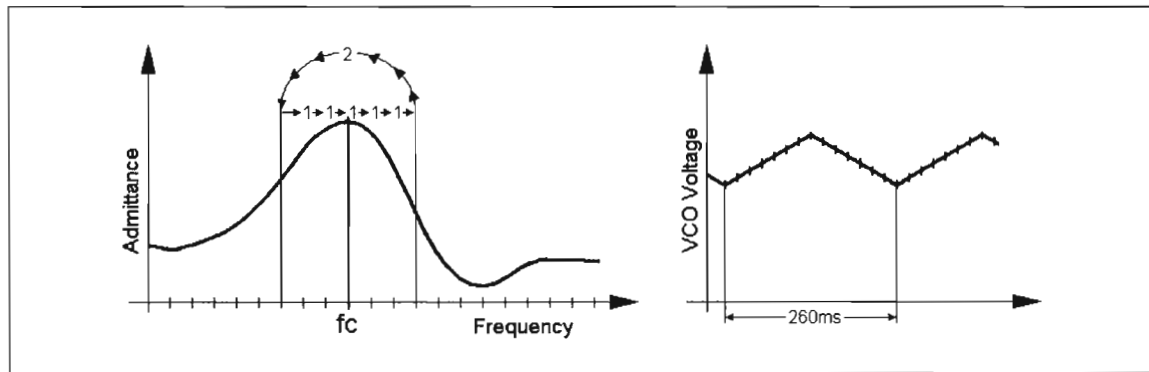


Figure 49: Triangle locking control technique showing the frequency sweep and repetition period

The triangle locking control subroutine can be found in Appendix C13.4 as a flowchart and the microprocessor code is in Appendix C13.5 line 646.

Chapter 5

Experimental Evaluation

This chapter concentrates on evaluating the performance of the Class-GD ultrasonic generator. Although the topology was simulated and is theoretically known to work, there were problems with practical implementation, such as reverse recovery time of the diodes in the IGBTs in the H-bridge inverter and the stability and effectiveness of the different control topologies. Performance characteristics looked at in detail were the system efficiency, auto detection of transducer peak admittance and the performance of the various control topologies for different load conditions.

5.1 General System Performance

Table 7 shown the various tests performed on the Class-GD ultrasonic generator. These were performed for two different load types and varying load conditions. The first load was a single transducer; a second load condition was a four transducer array with four different optimal operating frequencies.

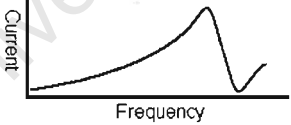
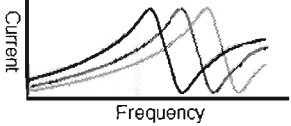

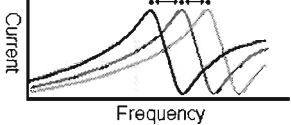
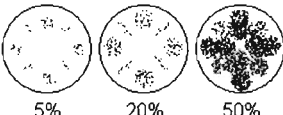
Test	Graph	Description
General admittance frequency sweep and AUTO detect		While keeping the voltage constant increase the frequency in steps. Record the current at each frequency step.
Admittance, frequency shift with a increase in power		Perform the standard admittance frequency sweep at different voltage (power) levels and monitor the admittance peak shift.
Admittance locking		Evaluate the peak admittance locking.
Admittance, SAW and Triangle locking, frequency shift with power		Monitor the admittance peak shift tracing capabilities of the three control topologies with a change in load conditions.
Admittance, SAW and Triangle locking power transfer		Evaluate the effectiveness of the three control topologies under investigation.

Table 7: Test to be performed on the Class-GD ultrasonic generator

5.1.1 General System Efficiency

The efficiency of the Class-GD generator was measured by connecting the system to a resistive load of known resistance and driving the load at varying power levels. The input power was measured as seen below in Figure 50. An analog power meter measured the AC power to the Class-GD ultrasonic generator. A power analyser and digital scope measured power to the resistive load. The computer was connected to the Class-GD ultrasonic generator communication port to monitor system status.

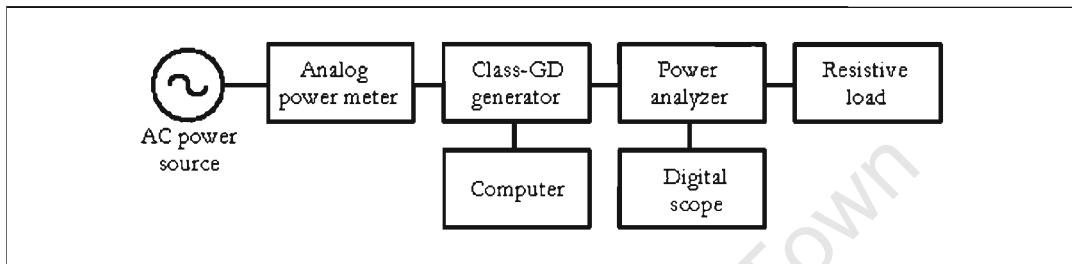


Figure 50: The setup used to measure system efficiency

The efficiency was measured by following procedure:

1. The load was selected and connected to the Class-GD generator.
2. The input and output power were measured and recorded in a table (as seen in Appendix B1) at varying voltage set points and loads.
3. The percentage efficiency was calculated by dividing the input power into output power. The result was multiplied by 100 to achieve a percentage.

The low efficiency at low power was because of the power requirements of the control circuit. Measurements may be seen in Figure 51.

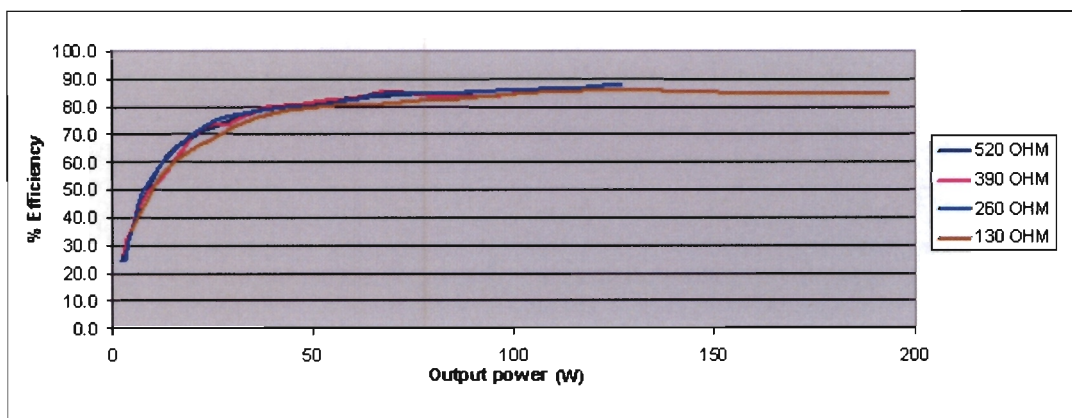


Figure 51: Percentage efficiency versus output power at various loads

5.1.2 General Frequency Scan Results

The output frequency was determined by two variables in the microcontroller. The first was the frequency range, a second the frequency set point. In Figure 52 may be seen the transducer frequency versus the PIC microcontroller frequency set point for two of the five frequency ranges.

From Figure 52 the following observations were made and changes implemented:

Observations:

1. The change in output frequency was reasonably linear between the PIC frequency set points of 100 and 200.
2. There was a adequate amount of transducer frequency overlap between both ranges with limited PIC frequency set point span of 100 and 200.

Changes implemented:

1. The PIC frequency set point range was limited to between 0 to 200 in the software.
2. If the Class-GD ultrasonic generator was run in AUTO mode, the device selected a frequency range for a particular transducer where the normal operating frequency was about in the middle of the frequency range.

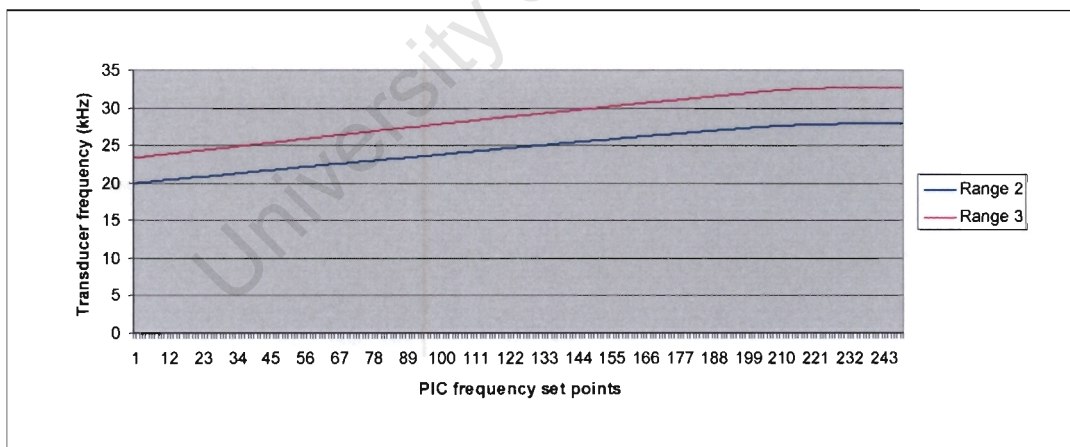


Figure 52: Transducer frequency versus PIC frequency set point

A frequency scan was performed to discover if the Class-GD ultrasonic generator would be able to determine peak admittance of a particular transducer load. The data in Figure 53 was acquired by connecting the Class-GD ultrasonic generator to the load and instructing it to perform a scan, while capturing the information on a PC via the serial port and later exporting the information to an Excel spreadsheet as seen in Appendix B2.

From the results in Figure 53 the following observations were made:

1. A peak current amplitude of 8.65A was measured at 23.71kHz for the single ultrasonic transducer as seen in Appendix B2. The peak was easy to track as it moved because of the “sharpness” of the peak. One frequency step to either side of the peak constituted a $\pm 40\text{Hz}$ change in transducer frequency and a minimum amplitude change of about 568mA.
2. For the multiple transducer array a peak current of 6.61A was measured at 26.01kHz as seen in Appendix B2. The peak tracking for the multiple transducer array was less accurate when compared to the tracking for the single transducer. For a single ultrasonic transducer there was one optimal frequency but for a ultrasonic transducer array there was myriad optimal frequency. Each ultrasonic transducer in the array had its own optimal frequency, each frequency moving independently depending on the loading of each transducer.

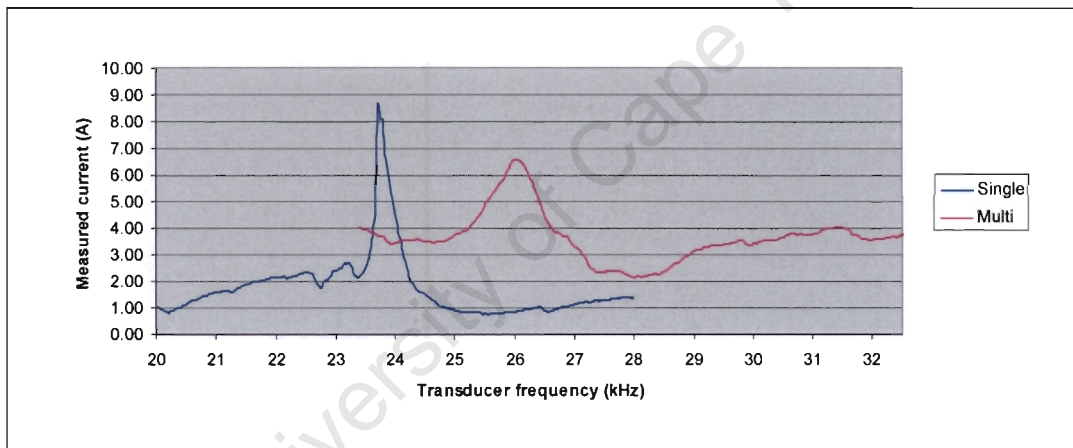


Figure 53: Admittance scan for a single and multiple transducer array

A low power Class-GD scan was compared with the real admittance plot for ultrasonic transducer and load. The Hewlett Packard 4192A LF impedance analyser was used to measure real admittance. The results may be seen in Figure 54. From the results it was seen the current scan from the Class-GD generator closely resembled the actual admittance plot of the transducer. The admittance and current peaks were at slightly different frequencies because of the optimal transducer frequency shift that occurred at different power levels. The impedance analyser used tiny signals to determine admittance of the transducer, where as the Class-GD generator used a larger signal of about 20V peak-to-peak.

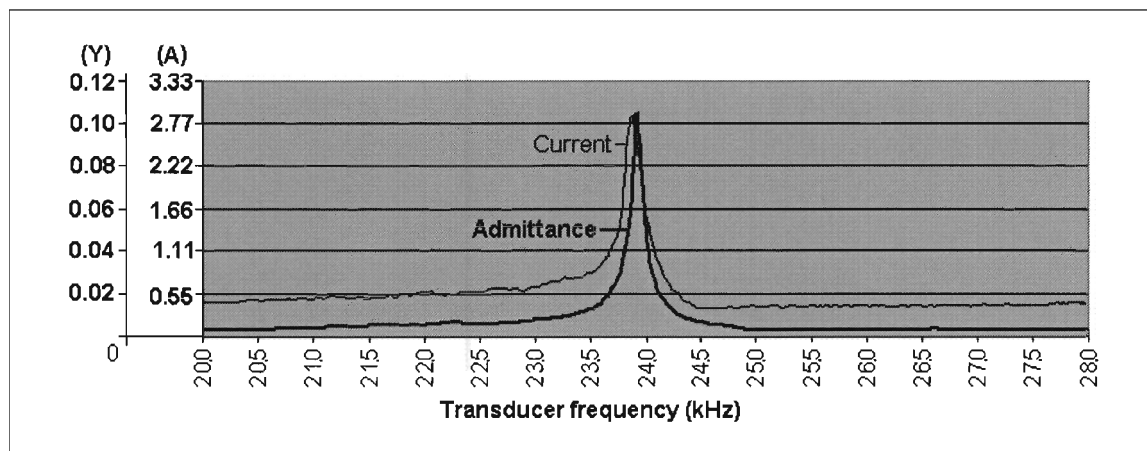


Figure 54: Class-GD scan versus HP impedance analyser

5.1.3 General Admittance Locking Control Techniques Results

Three parameters were important for admittance lock. The first was system stability: did the system lock to the peak admittance and remain locked to the peak admittance with a change in load? A second important parameter was response time: how fast did the system respond to a change in load? A third parameter was time at optimal frequency: the more time spent at optimal frequency the more effective the system.

From Figure 46 it may be observed the response time for the admittance locking control topology was 150ms and that 67% of the time was spent at peak admittance. This control technique appeared better suited for a single ultrasonic transducer system as it needed only to lock to one optimal frequency.

Figure 48 Shows that the response time for the saw-tooth locking topology was 155ms and that about 10% of the time was spent at peak admittance. This control technique was better suited for an ultrasonic transducer array system as it needed to deliver power at more than one optimal frequency.

Figure 49 Shows that the response time for the triangle locking topology was 260ms and that about 10% of the time was spent at peak admittance. This control technique was better suited for an ultrasonic transducer array system as it needed to deliver power at more than one optimal frequency.

5.2 Single Ultrasonic Transducer Performance Tests

For the single ultrasonic transducer performance test the arrangement used may be seen in Figure 55. An ultrasonic transducer was connected to a titanium horn. The tip of the horn was then submerged in Weisslers solution (iodine solution) where the discolouration of the solution would be proportional to power transfer [30].

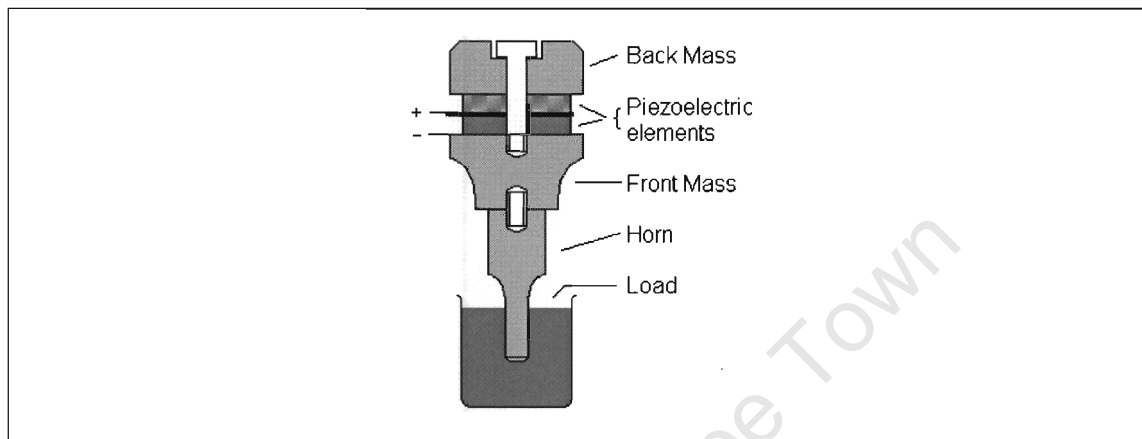


Figure 55: The signal transducer arrangement

Test procedures:

For frequency scan results - the tip of the horn was left at a fixed depth.

For admittance locking results - the tip of the horn was placed at two depths.

For power transfer results - a quantitative determination of iodine release was used.

The iodine solution [30]

1. 16.6g KI, potassium iodide
2. 0.1g $(\text{NH}_4)_6\text{MoO}_{24} \cdot 4\text{H}_2\text{O}$, ammonium heptamolybdate
3. 1L H_2O
4. The chemicals were mixed with minimum stirring and heating.
5. The solution was stored in a cool dark place and used as rapidly as possible.

The procedure of the test

1. The solution was kept at low temperature and the experiments performed rapidly.
2. Before the topology test was performed, one millilitre of solution was decanted into a cuvette to provide a same age reference.
3. The iodine solution was exposed for 5min at a fixed voltage set point.

4. After exposure, one millilitre was decanted into a cuvette and temporarily stored in a cool dark place.
5. The process of exposing the iodine solution to cavitation was repeated for each voltage set point and topology as in Appendix B9.
6. Absorbance was measured at 352nm using a JENWAY 6300 spectrophotometer.
7. This information was then tabulated in an Excel spreadsheet as in Appendix B9.

What happens to the solution?

Free radicals formed in the iodine solution during the cavitation process. The free radicals oxidized the I^- to I_2 . By using the JENWAY spectrophotometer at a wavelength of 352nm we determined the amount of I_2 present in the solution. This in turn was used to determine the quantity of free radicals present in the solution [30]. The spectrophotometer was used to measure the absorbance, later used in a comparative study as seen in Appendix B9.

5.2.1 Single Transducer Scan Results

From the information in Figure 56 and Appendix B3 it was observed with an increase in voltage set point there was an increase in transducer current. Also observed are current peak shifts in the frequency range with an increase in voltage set point. The increase in current with an increase in voltage set point was because of Ohm's Law.

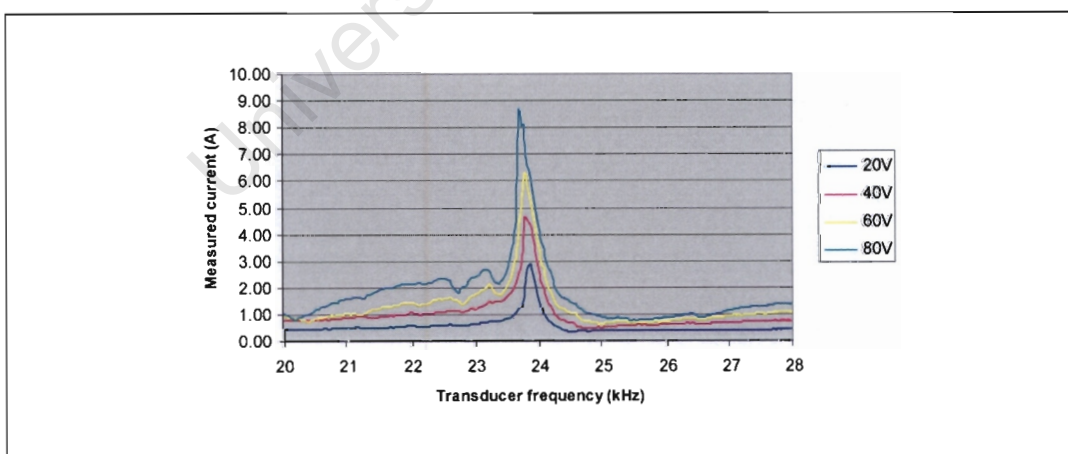


Figure 56: Single transducer scan results

The current peak shifted from 23.87kHz at voltage set point 20 to 23.71kHz at voltage set point 80 as seen in Table 8. These results coincided with the results obtained by Alex Green, a former UCT MSc student, who demonstrated the frequency shift in admittance with an increase in power [31].

Voltage set point	Frequency	Current
20V	23.87 kHz	2.86A
40V	23.82 kHz	4.67A
60V	23.82 kHz	6.32A
80V	23.71 kHz	8.65A

Table 8: Frequency shift with a increase in voltage set point for a single transducer

5.2.2 Single Transducer Admittance Locking Results

The admittance locking result is seen in Figure 57. The load was changed at time step 20. As the load changed, the admittance locking system responded to the change and locked to the new resonant frequency. At time step 55 the load was returned to this original value and the system responded by locking to the new resonant frequency. The system managed to lock to the new frequency in one time step equal to $\pm 150\text{ms}$.

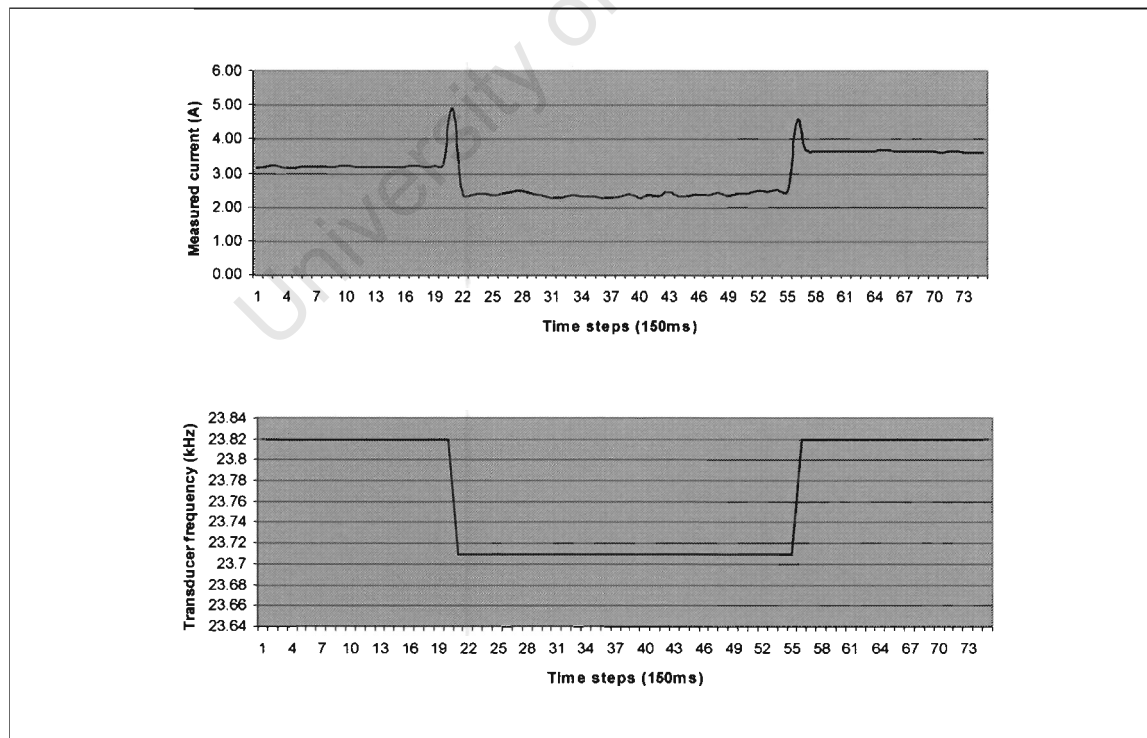


Figure 57: Single transducer admittance locking results. At time step 20 the load was changed, the system responded to the change in one time step of 150ms by reducing the frequency by 110Hz or three frequency set points. At time step 55 the load was returned to the original value

5.2.3 Single Transducer Saw-tooth Locking Results

The saw-tooth locking result is seen in Figure 58. The load was changed at time step 20. As the load changes the saw-tooth locking system responded to the change and locked to the new resonant frequency. At time step 55 the load returned to the original value and the system responded by locking to the new resonant frequency. Frequency lock was achieved in one time step equal to $\pm 155\text{ms}$.

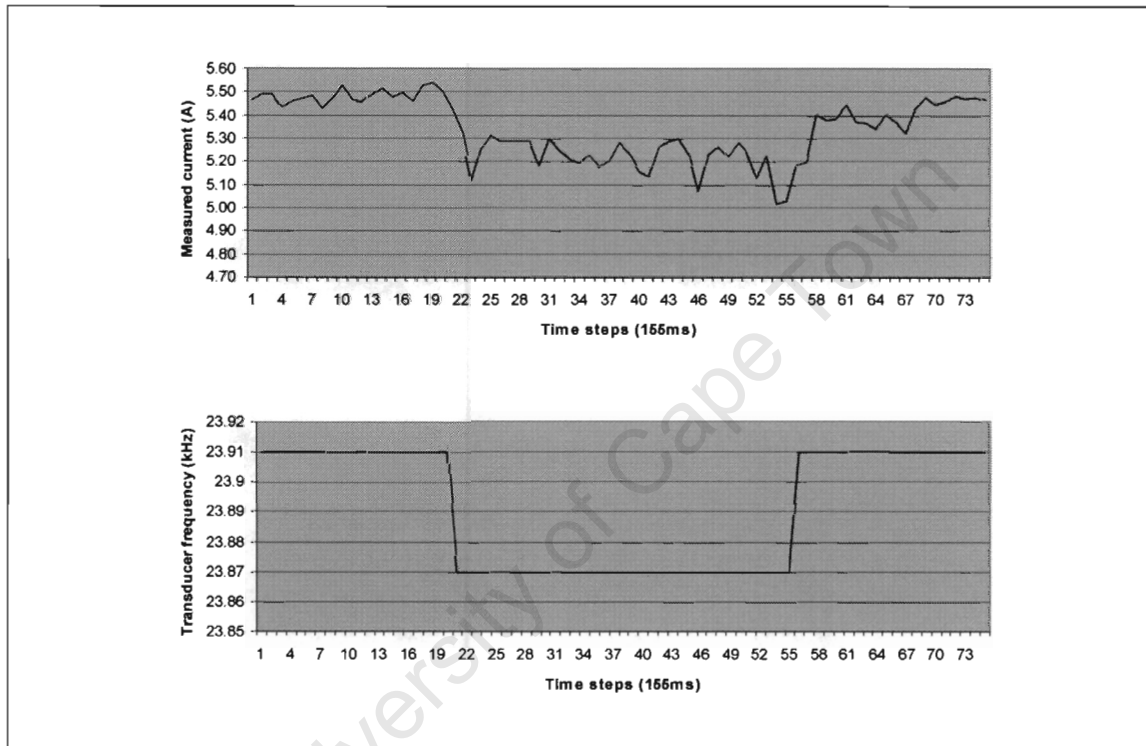


Figure 58: Single transducer saw-tooth locking results. At time step 20 the load was changed, the system responded to the change in one time step of 155ms by reducing the frequency by 40Hz or one frequency set point. At time step 55 the load was returned to the original value

5.2.4 Single Transducer Triangle Locking Results

The triangle locking result can be seen in Figure 59. The load was changed at time step 22. As the load changed the admittance locking system responded to the change and locked to the new resonant frequency. At time step 40 the load was returned to the original value and the system responded by locking to the new resonant frequency. The system managed to lock to the new frequency in one time step equal to $\pm 260\text{ms}$.

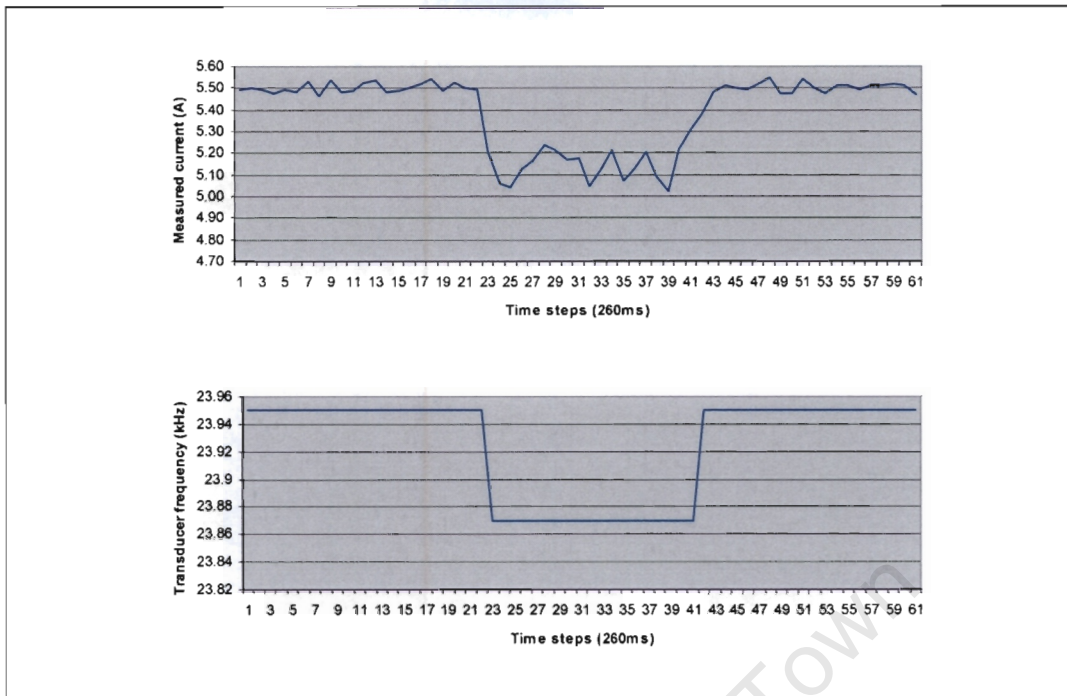


Figure 59: Single transducer triangle wave locking results. At time step 22 the load was changed, the system responded to the change in one time step of 260ms by reducing the frequency by 80Hz or two frequency set points. At time step 40 the load was returned to the original value

5.2.5 Single Transducer Power Transfer Results

From the results in Figure 60 it may be observed the manual mode (fixed frequency) performed worst. This was because of a reduction in transducer effectiveness as the transducer's resonant frequency shifted further from the set frequency with increase in power. The peak admittance locking performed best across the entire voltage range. The triangle and saw-tooth topologies performed better than the manual mode, but were unable to compete with peak admittance locking mode. Because of swept frequency only a fraction of the time was spent at the transducer resonant frequency.

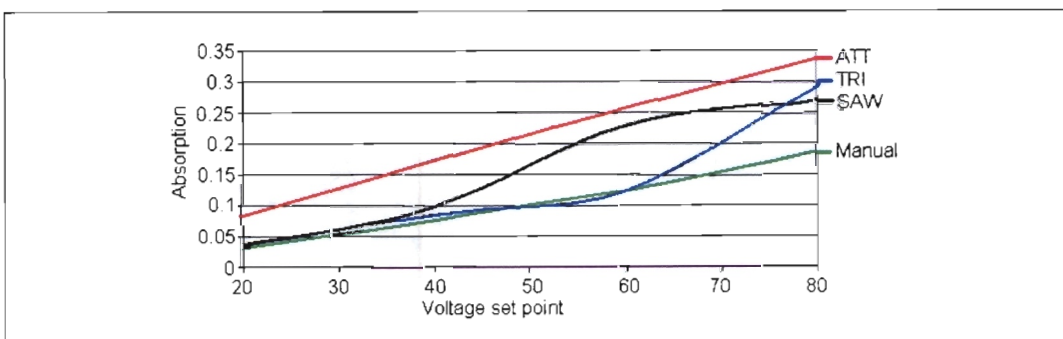


Figure 60: Single transducer power transfer results

5.3 Transducer Array Performance Tests

For the multi-ultrasonic transducer performance test, the arrangement may be seen in Figure 61. Four ultrasonic transducers were connected to a cavitation bath and the bath partially filled with water.

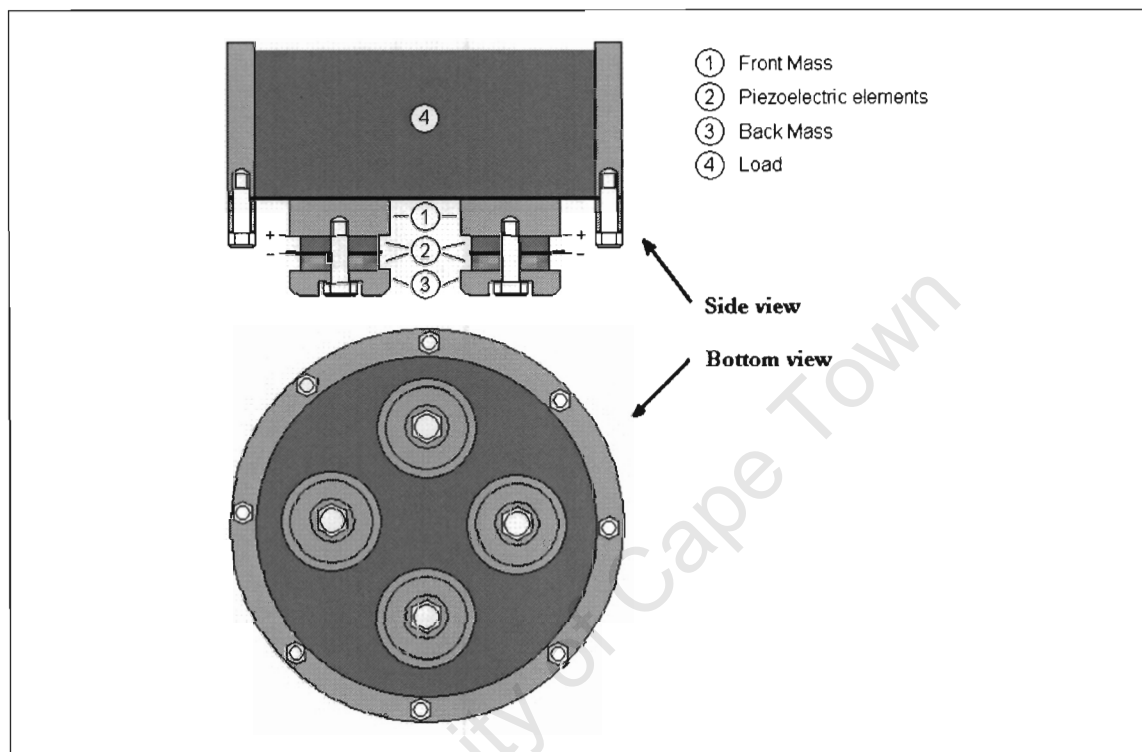


Figure 61: The multi-transducer array setup showing the four transducers arrangement (No scale)

For the frequency scan results - the water in the bath was kept at a fixed level.

For the power transfer results - two factors were considered. One to determine the amount of power delivered by each ultrasonic transducer, to establish if there was equal load sharing between the ultrasonic transducers, another a test to determine the power transfer at different power levels.

The iodine solution determined only the power transfer test, not the power distribution in the cavitation bath; the aluminium destruction test was able to determine both measurements. A sheet of heavyweight aluminium foil was placed in the bath and used to measure destructive power in the bath. All results were later used for a comparative study.

5.3.1 Transducer Array Scan Results

From the information in Appendix B4 and as seen in Figure 62, it was surmised with an increase in voltage set point there was an increase in transducer array current. It may also be observed the current peak shifts in the frequency range under an increased voltage set point.

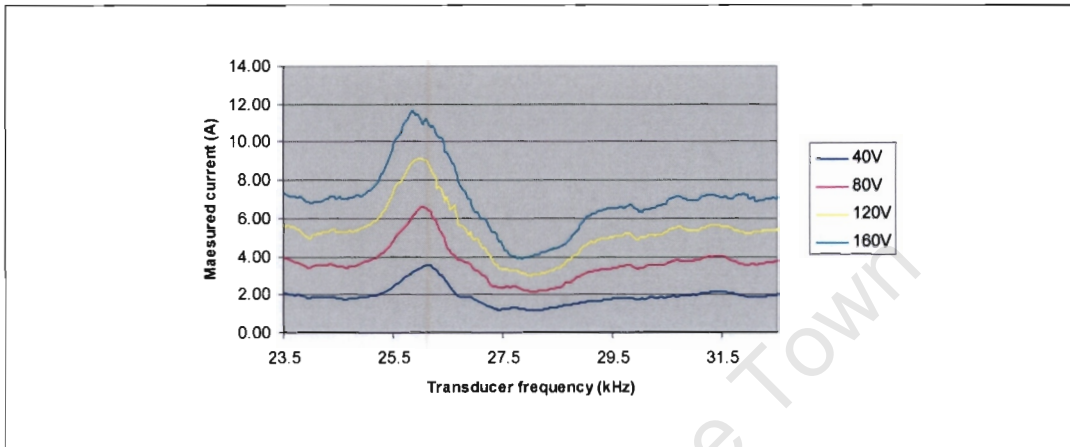


Figure 62: Transducer array scan results

The current peak shifted from 26.14kHz at voltage set point 40 to 25.87kHz at voltage set point 160 as seen in Table 9.

Voltage set point	Frequency	Current
40V	26.14 kHz	3.58A
80V	26.01 kHz	6.61A
120V	26.01 kHz	9.15A
160V	25.87 kHz	11.67A

Table 9 Frequency shift with a increase in voltage set point for a transducer array

5.3.2 Transducer Array Power Transfer Results

For this test a circular piece of heavyweight aluminium foil was placed at the bottom of the bath. The destructive cavitation eroded (black areas are eroded) the foil as seen in Figure 63.

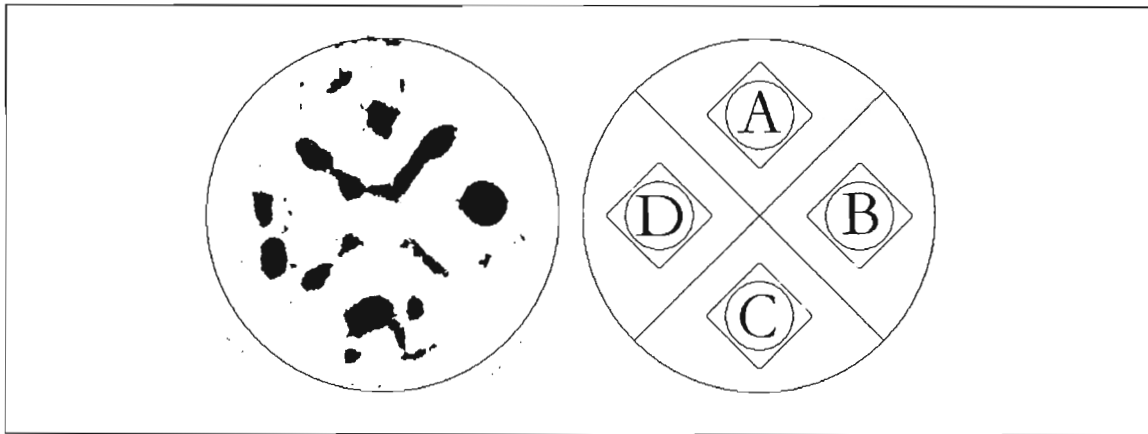


Figure 63: Aluminium foil showing destruction pattern. The dark area represents areas of destruction

The peak admittance locking control technique performed best of the three control topologies as seen in Figure 64. The reduced performance of the saw-tooth (SAW) and triangle wave (TRI) control techniques were because of the applied sweep frequency technique. Only a fraction of the time was spent at transducer resonant frequency.

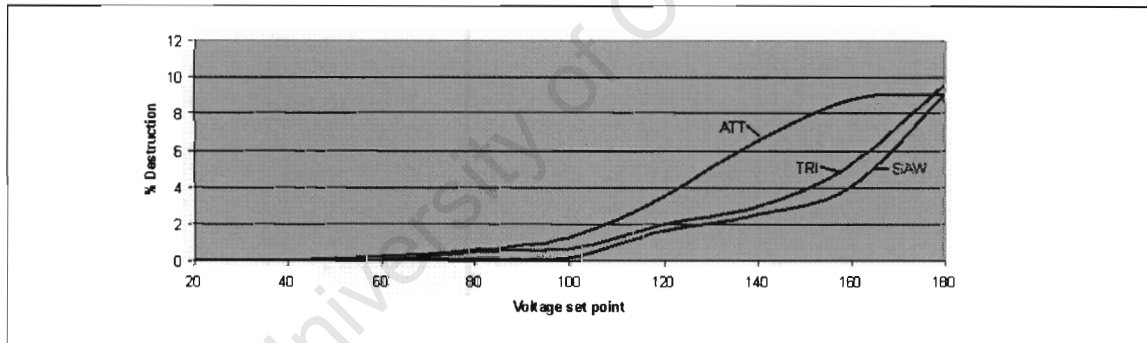


Figure 64: Transducer array power transfer results

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

A study was made in the field of ultrasound and the uses of ultrasound to prepare the reader for the research described in this document (Chapter 2). The document describes the design of the Class-GD ultrasonic generator prototype. It argued that this device provided a more efficient solution compared to linear amplifier solutions, and greater flexibility compared to existing switch mode solutions (Chapter 3). The design, implementation and testing of a working Glass-GD ultrasonic generator utilizing a software platform is shown. It explains how various software control topologies were designed, implemented and tested on the Glass-GD ultrasonic generator (Chapter 4, 5). Experimental results highlighted several practical construction problems, but never the less, demonstrated an efficient system with a highly adaptable control sub-system. Further attention to the voltage and current feedback circuit design in order to improve the performance to acceptable levels was suggested.

The use of a structured software layer approach, a microcontroller for control topology implementation and an FPGA as a power controller proved invaluable especially for testing new control topologies. The microcontroller made it possible to design, implement, test and fine-tune a new control topology in a matter of minutes with a negligible cost of implementation. The FPGA provided the opportunity to test various PWM switching techniques and power control techniques through simple software design. This software layer thus avoided many costly and time-consuming pitfalls especially in the development of new hardware.

The use of a hybrid H-bridge inverter with MOSFETs and IGBTs (with ultra-fast diodes) showed greater efficiency compared to the established H-bridge configurations with only one switch type. The open-loop digital beat-frequency SPWM technique was shown to successfully generate a sine wave.

The Class-GD ultrasonic generator successfully detected the optimum operating frequency of a single ultrasonic transducer by means of a peak current detection process and successfully pinpointed the series resonant frequency of the transducer. The implementation of the PLL control topology was unsuccessful. The cause of the failure was found to be the current transformer design as it added a phase shift in the measured current. This added phase shift in the current made accurate phase detection impossible.

The admittance locking control technique proved a great success and led to a successful design, implementation and testing of peak admittance locking, monotonically swept frequency and frequency modulation control techniques.

Table 10 compared two commercially available products with the Class-GD ultrasonic generator. The Class-GD ultrasonic generator provided better efficiency, upgradeability, energy density and mass density than the AG 1006 LF linear ultrasonic generator. The AG1006 LF, however provided a better operating bandwidth. The Class-GD ultrasonic generator provided better operating bandwidth, upgradeability, energy density and mass density than the MSG.1200.OW switch mode ultrasonic generator. The MSG.1200.OW, however, provided better efficiency. The Class-GD ultrasonic generator performed generally well as it achieved goals set out in the beginning of this document, to have better efficiency than linear ultrasonic and greater control flexibility than existing switch mode ultrasonic generators.

	AG 1006 LF [19] (Linear generator)	MSG.1200.OW [23] (Switch mode)	Class-GD (Switch mode)
Efficiency	Less than 50%	Approx. 95%	Approx. 85%
Operating bandwidth	25kHz - 10MHz	19.02kHz - 46.73kHz	15kHz – 50kHz
Power rating	300W	1200W	1000W
Upgradeable	Yes (manufacturer only)	Yes (manufacturer only)	Yes (any e.g. student)
Volume to power ratio	44006	11347	Approx. 3000
Mass to power ratio	0.04	0.003	Approx. 0.002

Table 10: Ultrasonic generator comparison

The success of this project lies in the user-friendliness of the control layer and the software layer. This was proved when two students Brevin Claassen [32] and Gregory Payne [33] successfully designed, implemented and tested their own control topologies under my guidance. Gregory Payne with guidance from Dr Lynn Brown and myself showed how the Class-GD ultrasonic generator could be used to perform microencapsulation. Microcapsules with a diameter of 100 μ m to 200 μ m were produced

at a success rate of 61.9% [33], compared to previous work where only 10% of the microcapsules produced were smaller than $186\mu\text{m}$ [34].

6.2 Recommendations

From the present research, the following recommendations are made for development:

- An improved phase detector circuit for the use in phase lock loop control.
- The PIC microcontroller is in use at the Cape Peninsula University of Technology (CPUT) as a standard. This led to the use of a PIC microcontroller in the Class-GD ultrasonic generator to make development easier for students. A more powerful microcontroller, or DSP, is recommended for this project to maximise system performance and capability.
- A larger FPGA is also recommended. This will give a designer greater freedom to be creative, without worrying about counting logic-cells.
- The voltage and current feedback circuits need redesigning to give the Class-GD ultrasonic generator a greater frequency bandwidth. The Class-GD ultrasonic generator has a potential to generate a sine wave from a fraction of 1Hz up to about 100kHz, and a square wave up to about 1MHz, with some modifications.
- An electrically isolated RS232 port is recommended; with an improved system the use of USB should be considered.
- True transducer power measurement needs to be developed for the Class-GD ultrasonic generator.
- This project has great potential as it permits a university student to develop and test a new ultrasonic transducer control topology in a fraction of the conventional time.

References

- [1] A. S. Morris, *Measurement & Instrumentation Principles*, 3rd ed. Oxford: Elsevier Butterworth-Heinemann, 2005, pp. 259.
- [2] T. F. Hueter and R. H. Bolt, *Sonics: Techniques for the use of sound and ultrasound in engineering and science*, New York: John Wiley & Sons Inc., 1955.
- [3] T. J. Mason and J. P. Lorimer, *Applied Sonochemistry: Uses of Power Ultrasound in Chemistry and Processing*, Wiley-VCH, 2002, pp. 4.
- [4] D. Stansfield, *Underwater electroacoustic transducers*, Wiltshire: Redwood Press Limited, 1991, pp.
- [5] S. Adams, *Phase Locking and Digital Power Control for Ultrasonics*, BTech Thesis, Cape Technikon, 2002.
- [6] B. Mortimer, T. du Bruyn, J. Davies, J. Tapson, *High power resonant tracking amplifier using admittance locking*, Elsevier science, Ultrasonics 39, 2001, pp. 257-259.
- [7] L. William, W. Puskas, T. Piazza, *Designer Waveforms: Ultrasonic Technologies to Improve Cleaning and Eliminate Damage*, August 2001. [Online]. Available: http://www.blackstone-ney.com/pdfs/T_Designer_waveforms.pdf. [Accessed Nov. 2005].
- [8] Wikipedia, *Electronic amplifier*, September 2006. [Online]. Available: http://en.wikipedia.org/wiki/Electronic_amplifier. [Accessed October 2006].
- [9] L. L. Beranek, *Acoustic measurement*, United States of America: John Wiley & Sons Inc, 1949, pp.3 – 15.
- [10] H. Kuttruff, *Ultrasonics: Fundamentals and applications*, England: Elsevier applied science, 1991.

- [11] D. Cheeke, C. N. Cheeke, J. D. N. Cheeke, *Fundamentals and applications of Ultrasonic waves*, New York, Washington D.C: CRC Press. 2002.
- [12] V.A. Shutilov, *Fundamental Physics of Ultrasound*, Amsterdam: Gordon and Breach Science publishers. 1988.
- [13] W.P. Mason, *An electromechanical representation of a piezoelectric crystal used as a resonator*, Proc. IRE, Vol23, no. 10, pp. 1252-1263, 1935.
- [14] W.R. Patterson, *Complex Analysis of Ultrasonic Transducers operating at High Power*, Btech Thesis Cape Technikon 2002.
- [15] N.R. Owen, M.R. Bailey, B.J.P. Mortimer, H. Kolve, J. Hossack, L.A. Crum, *Development of Power Supplies for Portable HIFU Therapy Systems*, Proc. Int. Symp. Therapeutic Ultrasound, 399-404, 2003.
- [16] MASTERSONIC, *Basic Elements of MMM Systems & How MMM Systems Operate*, [Online]. Available: <http://www.mpi-ultrasonics.com>. [Accessed November 2005].
- [17] T.L. Floyd, *Electronic Devices*, 3rd ed. New York: Merrill, 1992, pp. 388 - 421.
- [18] D. Self, *Audio Power Amplifier Design Handbook*, 3rd ed. Oxford: Newnes, 2002, pp. 36 – 38.
- [19] HOLTEK technologies, *AG1006 LF ultrasonic Generator and Power Linear Amplifier*, Datasheet, [Online]. Available: <http://www.hotektech.com/TCPoComp.htm>, [Accessed November 2005].
- [20] T&C Power Conversion, *ULTRA 2020 linear amplifier*, Operation manual, [Online]. Available: <http://tcpowerconversion.com/ultral/2020.html>, [Accessed November 2005].

- [21] G.R. Slone, *High-Power Audio Amplifier Construction Manual*, USA: McGraw-Hill Professional, 1999, pp. 53.
- [22] N. Mohan, T.M. Undeland, W.P. Robbins: *Power Electronics*, 3rd Edition, USA: John Wiley & sons, 2003, pp.162-341.
- [23] MASTERSONIC, *MMM Transducers & MMM Transducers & Systems*, [Online]. Available: http://www.mastersonic.com/documents/mmm_products_overview.pdf, [Accessed November 2005].
- [24] C. Langton, *Unlocking the Phase Lock Loop – Part 1*, [Online]. Available: <http://www.complextoreal.com/chapters/pll.pdf>, [Accessed November 2005].
- [25] Philips semiconductors, *74HC/HCT4046A Phase-locked-loop with VCO*, Datasheet, Available: <http://www.standardics.philips.com/products/hc/pdf/74hc4046a.pdf>, [Accessed November 2005].
- [26] F.J. Fuchs, *Continuing Developments in Ultrasonic Technology*, [Online]. Available: <http://www.cemag.us/articles.asp?pid=468>, [Accessed October 2006].
- [27] R. Alksne, *RDS Underwater Acoustic Telemetry trials Report*, [Online]. Available: <http://www.dsto.defence.gov.au/corporate/report/DSTO-TN-0259.pdf>, [Accessed November 2005].
- [28] C.N. Hemmings, *Improving Class D audio power amplifiers*, Bachelor of Engineering, The University of Queensland, 1999
- [29] Maxim, *Class D Audio Amplifier Output Filter Optimization*, Application notes, [Online]. Available: www.maxim-ic.com/appnotes.cfm/appnote_number/624, [Accessed November 2005].
- [30] A. Henglein, *Sonochemistry: Historical Developments and Modern Aspects*, Ultrasonics, 1987.

- [31] A.G. Green, *The Design of High Power Ultrasonic Transducers*, MSc Electrical Engineering Thesis (UCT, South Africa) April 2002, pp 110-121.
- [32] B. Claassen, *Digital control techniques for a multiple transducer array*, BTech Thesis, Cape Peninsula University of Technology 2005.
- [33] G. Payne, *Digital locking techniques for a single ultrasonic transducer*, BTech Thesis, Cape Peninsula University of Technology 2005.
- [34] S. Kokott, *Microencapsulation and supply of Bifidobacterium lactis in fermented traditional African beverages*, Cape Technikon, 2004.
- [35] International Rectifier, *IR2117 Single channel high speed power MOSFET and IGBT driver*, Datasheet, [Online]. Available: www.irf.com/product-info/datasheets/data/ir2117.pdf, [Accessed November 2005].
- [36] International Rectifier, *HV Floating MOS-Gate Driver ICs*, Application notes, [Online]. Available: www.irf.com/technical-info/an978/an-978.htm, [Accessed November 2005].
- [37] International Rectifier, *IR2113 Dual channel high speed power MOSFET and IGBT driver*, Datasheet, [Online]. Available: www.irf.com/product-info/datasheets/data/ir2113.pdf, [Accessed November 2005].
- [38] Fairchild semiconductor: *LM193 Low Power Low Offset Voltage Dual Comparators*, Datasheet, [Online]. Available: <http://www.national.com/ds/LM/LM193.pdf>, [Accessed November 2005].
- [39] P. Amar, *Using PWM to Generate Analog Output*, Application notes, [Online]. Available: <http://ww1.microchip.com/downloads/en/AppNotes/00538c.pdf>, [Accessed November 2005].
- [40] Microchip, *PIC16F87X 28/40-Pin 8-Bit CMOS FLASH Microcontrollers*, Datasheet, [Online]. Available: <http://ww1.microchip.com/downloads/en/DeviceDoc/>

30292c.pdf, [Accessed November 2005].

- [41] Altera: *MAX 7000 Programmable Logic Device Family*, Data Sheet, [Online]. Available: <http://www.altera.com/literature/ds/m7000.pdf>, [Accessed November 2005].

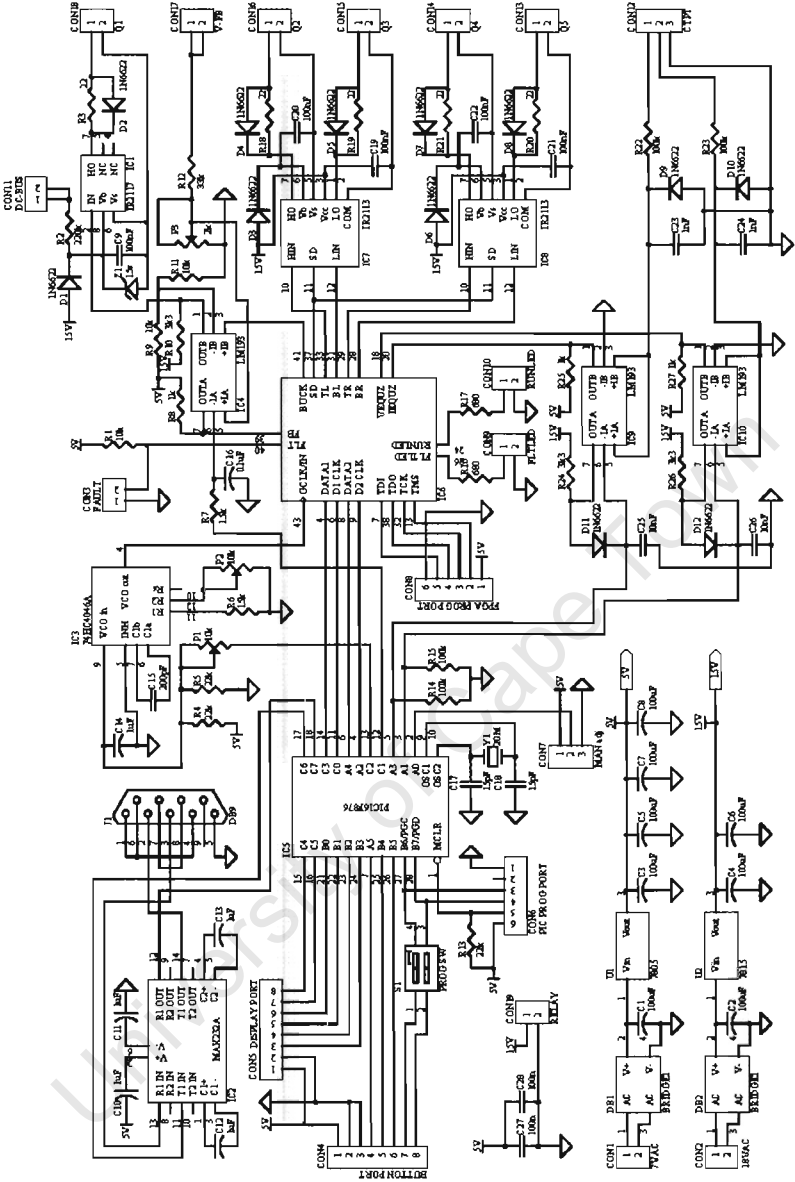
University of Cape Town

Appendix A - Schematic Diagrams

- A1 Control circuit schematic diagram
- A2 Power circuit schematic diagram

University of Cape Town

A1 Control circuit schematic diagram



Appendix B - Experimental results

- B1 System efficiency
- B2 Scan results
- B3 Single Transducer scan results
- B4 Transducer Array scan results
- B5 Admittance locking control techniques results
- B6 Single transducer admittance locking results
- B7 Single transducer saw tooth locking results
- B8 Single transducer triangle locking results
- B9 Single Transducer power transfer results
- B10 Transducer array Admittance locking power transfer results
- B11 Transducer array Saw tooth locking power transfer results
- B12 Transducer array Triangle locking power transfer results
- B13 Transducer array power transfer results

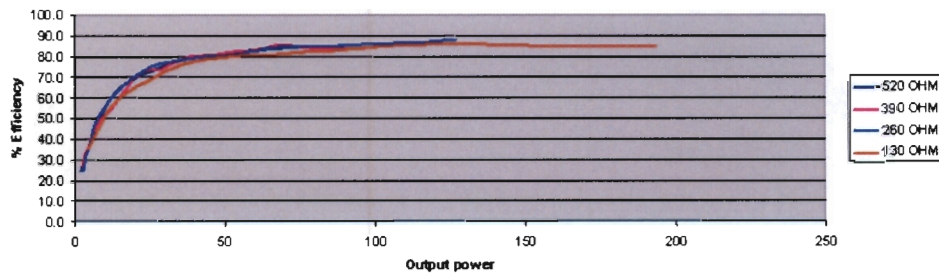
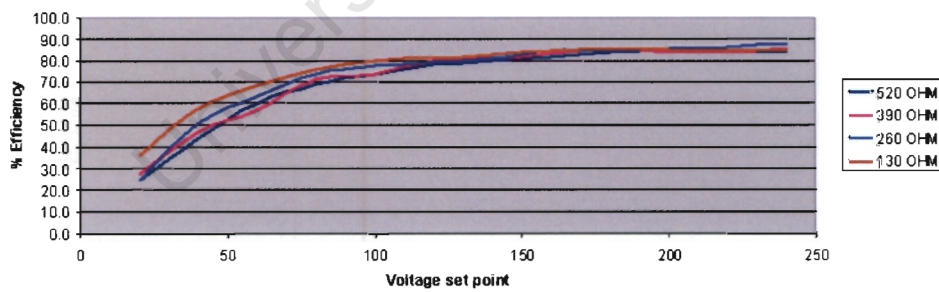
B1 System efficiency

At a load of 520Ω			
Vsetp	Pin	Pout	%Eff
20	10	2.47	24.7
40	16	7.01	43.8
60	21	12.57	59.8
80	28	19.2	68.5
100	36	26.5	73.6
120	44	34.2	77.7
140	54	43.1	79.8
160	65	53.1	81.6
180	76	63.6	83.6
200	88	74.5	84.6
220	100	84.3	84.3
240	114	95.4	83.6

At a load of 390Ω			
Vsetp	Pin	Pout	%Eff
20	10	2.72	27.2
40	16	7.46	46.6
60	24	13.7	57
80	30	21.3	71
100	39	28.7	73.5
120	48	38.2	79.5
140	59	47.7	80.8
160	71	58.9	82.9
180	82	69.7	85
200	98	81.8	83.4
220	112	93.6	83.5
240	124	106	85.4

At a load of 260Ω			
Vsetp	Pin	Pout	%Eff
20	12	2.95	24.5
40	16	8.07	50.4
60	24	15.2	63.3
80	32	23.5	73.4
100	42	32.5	77.3
120	54	42.9	79.4
140	68	55	80.8
160	80	67.6	84.5
180	95	80.3	84.5
200	112	95.7	85.4
220	128	110	85.9
240	144	127	88.1

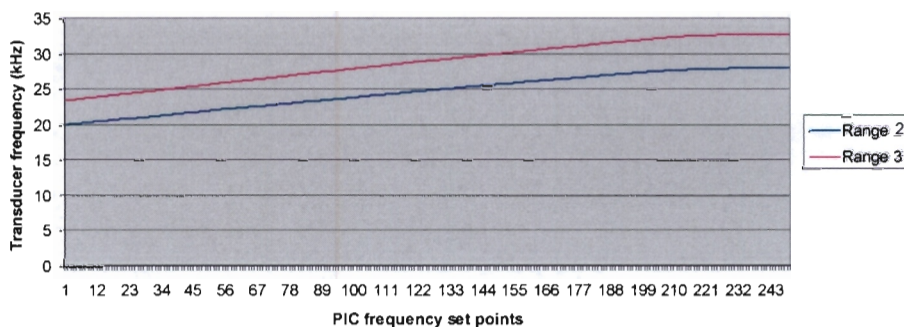
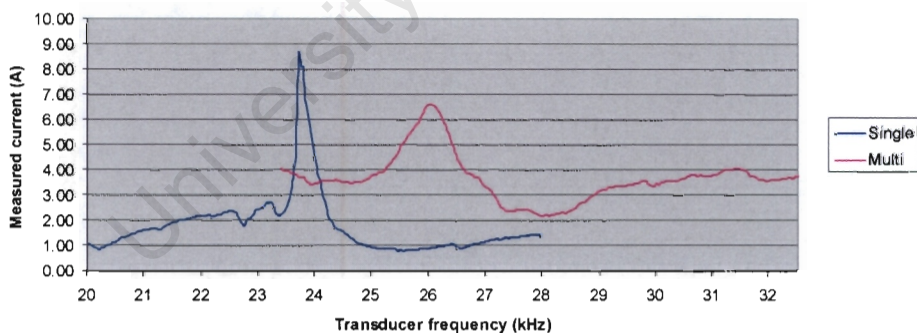
At a load of 130Ω			
Vsetp	Pin	Pout	%Eff
20	14	4.95	35.3
40	24	13.9	57.9
60	36	24.5	68
80	48	36.4	75.8
100	64	51.1	79.8
120	83	67.4	81.2
140	104	86.1	82.7
160	125	106	84.8
180	150	128	85.3
200	172	146	84.8
220	200	169	84.5
240	228	194	85.1



B2 Scan results

Single		Multi		Single		Multi		Single		Multi	
Freq	Amp	Freq	Amp	Freq	Amp	Freq	Amp	Freq	Amp	Freq	Amp
24.8	1.17	28.97	3.27	23.22	2.70	27.18	2.92	26.31	1.00	30.76	3.76
20.02	1.06	23.41	4.03	23.26	2.57	27.23	2.70	26.35	1.01	30.8	3.78
20.05	1.00	23.45	3.97	23.28	2.45	27.25	2.60	26.38	1.01	30.83	3.74
20.09	0.94	23.49	3.94	23.32	2.25	27.3	2.45	26.4	1.03	30.86	3.76
20.13	0.89	23.53	3.93	23.35	2.20	27.34	2.41	26.44	1.01	30.9	3.75
20.17	0.85	23.58	3.87	23.39	2.15	27.39	2.37	26.47	0.98	30.94	3.74
20.21	0.82	23.62	3.84	23.43	2.23	27.43	2.34	26.5	0.92	30.98	3.74
20.24	0.89	23.67	3.79	23.47	2.34	27.48	2.36	26.53	0.89	31.02	3.81
20.28	0.92	23.72	3.72	23.51	2.54	27.53	2.34	26.57	0.87	31.06	3.80
20.32	0.95	23.76	3.72	23.55	2.83	27.56	2.41	26.6	0.89	31.1	3.84
20.36	0.98	23.81	3.63	23.59	3.36	27.62	2.40	26.64	0.90	31.14	3.89
20.39	1.02	23.85	3.56	23.63	3.84	27.66	2.41	26.67	0.94	31.18	3.95
20.43	1.06	23.9	3.46	23.67	4.86	27.71	2.41	26.71	0.96	31.23	3.98
20.48	1.12	23.94	3.40	23.71	8.65	27.75	2.39	26.74	0.98	31.27	4.01
20.51	1.17	23.99	3.43	23.75	8.08	27.79	2.37	26.78	1.01	31.3	4.00
20.55	1.21	24.04	3.47	23.79	8.12	27.84	2.31	26.81	1.03	31.35	4.01
20.58	1.24	24.08	3.54	23.82	6.99	27.88	2.25	26.85	1.04	31.39	4.03
20.63	1.30	24.13	3.57	23.87	6.36	27.93	2.20	26.88	1.06	31.43	4.04
20.67	1.30	24.17	3.56	23.91	5.73	27.97	2.16	26.92	1.09	31.47	4.04
20.7	1.33	24.22	3.55	23.95	5.12	28.02	2.17	26.94	1.11	31.51	4.01
20.74	1.38	24.27	3.56	23.99	4.54	28.06	2.18	26.98	1.12	31.55	3.98
20.77	1.44	24.32	3.57	24.04	4.06	28.11	2.17	27.02	1.14	31.59	3.93
20.79	1.44	24.34	3.59	24.07	3.69	28.16	2.20	27.05	1.16	31.63	3.85
20.84	1.46	24.39	3.57	24.1	3.43	28.17	2.20	27.08	1.19	31.67	3.76
20.87	1.50	24.43	3.56	24.13	3.02	28.21	2.21	27.11	1.19	31.71	3.75
20.91	1.55	24.47	3.52	24.17	2.73	28.26	2.24	27.13	1.19	31.73	3.73
20.95	1.57	24.53	3.48	24.22	2.36	28.31	2.25	27.16	1.20	31.77	3.69
20.99	1.60	24.57	3.49	24.25	2.10	28.35	2.29	27.19	1.24	31.8	3.64
21.03	1.60	24.62	3.43	24.3	1.91	28.4	2.27	27.23	1.24	31.85	3.61
21.08	1.60	24.67	3.44	24.33	1.73	28.44	2.30	27.25	1.22	31.89	3.58
21.12	1.63	24.71	3.49	24.37	1.66	28.49	2.36	27.29	1.25	31.93	3.57
21.16	1.66	24.76	3.49	24.41	1.62	28.53	2.40	27.33	1.26	31.97	3.55
21.2	1.66	24.81	3.48	24.44	1.59	28.57	2.45	27.36	1.28	32	3.57
21.24	1.59	24.85	3.57	24.48	1.53	28.62	2.54	27.39	1.27	32.05	3.60
21.29	1.59	24.9	3.59	24.52	1.46	28.66	2.63	27.41	1.28	32.08	3.59
21.33	1.72	24.95	3.66	24.57	1.41	28.71	2.68	27.45	1.29	32.12	3.58
21.37	1.75	24.99	3.73	24.6	1.36	28.75	2.70	27.48	1.30	32.16	3.62
21.41	1.81	25.04	3.79	24.65	1.26	28.79	2.78	27.51	1.31	32.19	3.61
21.46	1.86	25.09	3.82	24.68	1.19	28.84	2.90	27.54	1.30	32.24	3.63
21.5	1.89	25.13	3.88	24.72	1.11	28.88	2.95	27.57	1.32	32.27	3.65
21.54	1.92	25.18	3.92	24.76	1.06	28.92	3.01	27.6	1.30	32.3	3.66
21.58	1.96	25.23	4.01	24.79	1.04	28.97	3.09	27.63	1.33	32.34	3.69
21.62	1.98	25.28	4.15	24.84	1.01	29.01	3.15	27.66	1.33	32.38	3.69
21.65	1.99	25.3	4.18	24.87	0.99	29.05	3.18	27.68	1.36	32.4	3.67
21.69	2.00	25.35	4.32	24.91	0.96	29.1	3.22	27.7	1.37	32.43	3.70
21.73	1.98	25.4	4.49	24.93	0.94	29.12	3.22	27.72	1.37	32.46	3.72
21.77	2.03	25.45	4.63	24.96	0.93	29.17	3.28	27.73	1.38	32.47	3.74
21.8	2.07	25.49	4.83	25	0.89	29.21	3.29	27.76	1.37	32.49	3.74
21.85	2.09	25.53	4.98	25.04	0.89	29.25	3.30	27.77	1.39	32.51	3.75
21.89	2.12	25.58	5.15	25.07	0.85	29.29	3.33	27.79	1.39	32.53	3.75
21.93	2.16	25.63	5.35	25.11	0.83	29.34	3.33	27.81	1.39	32.55	3.75
21.97	2.15	25.67	5.44	25.15	0.85	29.38	3.33	27.81	1.39	32.57	3.74

22.01	2.16	25.72	5.58	25.19	0.85	29.43	3.36	27.83	1.39	32.58	3.73
22.05	2.16	25.77	5.74	25.22	0.86	29.47	3.36	27.84	1.39	32.59	3.76
22.09	2.16	25.82	5.92	25.26	0.87	29.51	3.40	27.86	1.40	32.61	3.78
22.14	2.18	25.87	6.13	25.29	0.87	29.56	3.38	27.86	1.40	32.62	3.75
22.18	2.11	25.91	6.28	25.33	0.84	29.6	3.40	27.88	1.39	32.63	3.76
22.21	2.14	25.95	6.45	25.37	0.84	29.64	3.45	27.88	1.41	32.64	3.76
22.25	2.16	26.01	6.61	25.4	0.83	29.68	3.47	27.89	1.41	32.65	3.79
22.3	2.20	26.05	6.59	25.44	0.80	29.72	3.50	27.9	1.41	32.65	3.77
22.34	2.19	26.1	6.53	25.48	0.77	29.77	3.55	27.9	1.40	32.67	3.76
22.37	2.26	26.14	6.43	25.51	0.78	29.82	3.57	27.92	1.41	32.68	3.79
22.41	2.29	26.19	6.32	25.54	0.76	29.85	3.47	27.92	1.39	32.68	3.80
22.45	2.32	26.23	6.08	25.58	0.78	29.89	3.38	27.92	1.39	32.69	3.77
22.49	2.33	26.28	5.83	25.61	0.78	29.94	3.36	27.93	1.40	32.69	3.80
22.51	2.34	26.3	5.78	25.65	0.78	29.98	3.36	27.94	1.38	32.7	3.79
22.55	2.34	26.35	5.40	25.66	0.79	30	3.43	27.93	1.39	32.71	3.79
22.59	2.30	26.4	5.05	25.7	0.79	30.04	3.39	27.94	1.39	32.71	3.81
22.63	2.27	26.44	4.85	25.74	0.80	30.08	3.45	27.95	1.39	32.71	3.81
22.66	2.09	26.49	4.43	25.77	0.81	30.13	3.52	27.95	1.38	32.72	3.85
22.7	1.92	26.54	4.28	25.81	0.82	30.17	3.56	27.95	1.38	32.72	3.85
22.75	1.77	26.59	4.11	25.85	0.83	30.21	3.57	27.95	1.37	32.73	3.85
22.78	1.96	26.63	4.02	25.88	0.83	30.25	3.55	27.96	1.38	32.73	3.89
22.82	2.05	26.68	3.84	25.92	0.85	30.29	3.56	27.96	1.38	32.73	3.90
22.86	2.06	26.72	3.84	25.95	0.85	30.34	3.56	27.97	1.38	32.74	3.86
22.9	2.14	26.77	3.74	25.99	0.87	30.38	3.56	27.97	1.39	32.74	3.88
22.93	2.27	26.81	3.72	26.03	0.87	30.42	3.58	27.97	1.38	32.75	3.86
22.97	2.38	26.86	3.70	26.06	0.89	30.47	3.64	27.98	1.39	32.75	3.90
23.01	2.38	26.91	3.55	26.1	0.89	30.51	3.67	27.98	1.38	32.75	3.88
23.04	2.44	26.95	3.42	26.13	0.91	30.54	3.72	27.98	1.38	32.75	3.91
23.08	2.48	27	3.31	26.17	0.93	30.59	3.75	27.98	1.37	32.76	3.89
23.11	2.57	27.04	3.24	26.2	0.93	30.63	3.79	27.98	1.39	32.76	3.90
23.15	2.68	27.09	3.13	26.24	0.95	30.68	3.80				
23.19	2.67	27.14	2.98	26.28	0.96	30.72	3.76				



B3 Single Transducer scan results

Freq	Scan voltage set point			
	20V	40V	60V	80V
24.8	0.21	0.71	0.96	1.17
20.02	0.44	0.80	0.94	1.06
20.05	0.44	0.81	0.94	1.00
20.09	0.45	0.81	0.90	0.94
20.13	0.45	0.80	0.87	0.89
20.17	0.45	0.81	0.87	0.85
20.21	0.44	0.80	0.83	0.82
20.24	0.45	0.80	0.83	0.89
20.28	0.45	0.81	0.82	0.92
20.32	0.45	0.78	0.80	0.95
20.36	0.46	0.80	0.79	0.98
20.39	0.46	0.80	0.77	1.02
20.43	0.46	0.80	0.78	1.06
20.48	0.46	0.80	0.82	1.12
20.51	0.46	0.81	0.84	1.17
20.55	0.46	0.83	0.86	1.21
20.58	0.47	0.81	0.87	1.24
20.63	0.46	0.81	0.89	1.30
20.67	0.49	0.84	0.91	1.30
20.7	0.47	0.82	0.94	1.33
20.74	0.47	0.85	0.94	1.38
20.77	0.49	0.85	0.97	1.44
20.79	0.49	0.85	0.96	1.44
20.84	0.49	0.85	0.98	1.46
20.87	0.49	0.86	0.99	1.50
20.91	0.50	0.86	1.02	1.55
20.95	0.49	0.87	1.02	1.57
20.99	0.49	0.88	1.03	1.60
21.03	0.51	0.90	1.03	1.60
21.08	0.50	0.89	1.02	1.60
21.12	0.51	0.89	1.03	1.63
21.16	0.53	0.93	1.01	1.66
21.2	0.52	0.94	0.98	1.66
21.24	0.52	0.93	1.00	1.59
21.29	0.50	0.94	1.03	1.59
21.33	0.49	0.90	1.10	1.72
21.37	0.49	0.92	1.16	1.75
21.41	0.51	0.92	1.20	1.81
21.46	0.50	0.92	1.21	1.86
21.5	0.50	0.92	1.21	1.89
21.54	0.51	0.93	1.26	1.92
21.58	0.51	0.94	1.27	1.96
21.62	0.52	0.95	1.28	1.98
21.65	0.52	0.96	1.29	1.99
21.69	0.54	0.99	1.28	2.00
21.73	0.52	0.96	1.30	1.98
21.77	0.53	0.98	1.32	2.03
21.8	0.54	0.99	1.35	2.07
21.85	0.54	1.01	1.39	2.09
21.89	0.53	1.01	1.44	2.12
21.93	0.55	1.02	1.46	2.16
21.97	0.58	1.07	1.42	2.15
22.01	0.58	1.07	1.44	2.16
22.05	0.59	1.06	1.42	2.16
22.09	0.56	1.03	1.39	2.16

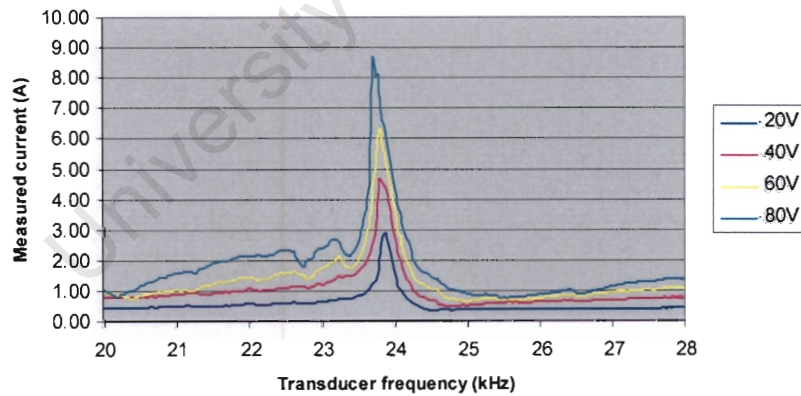
Freq	Scan voltage set point			
	20V	40V	60V	80V
23.22	0.71	1.43	2.08	2.70
23.26	0.77	1.47	2.14	2.57
23.28	0.76	1.46	2.02	2.45
23.32	0.76	1.47	1.85	2.25
23.35	0.76	1.48	1.79	2.20
23.39	0.76	1.49	1.72	2.15
23.43	0.77	1.49	1.72	2.23
23.47	0.81	1.55	1.84	2.34
23.51	0.83	1.65	1.97	2.54
23.55	0.85	1.73	2.17	2.83
23.59	0.92	1.84	2.45	3.36
23.63	1.02	2.01	2.86	3.84
23.67	1.08	2.24	3.22	4.86
23.71	1.22	2.57	4.10	8.65
23.75	1.36	3.04	5.39	8.08
23.79	1.68	4.60	6.30	8.12
23.82	2.38	4.67	6.32	6.99
23.87	2.86	4.43	5.48	6.36
23.91	2.60	4.13	4.87	5.73
23.95	2.17	3.40	4.33	5.12
23.99	1.70	2.86	3.80	4.54
24.04	1.33	2.47	3.33	4.06
24.07	1.12	2.11	2.89	3.69
24.1	1.01	1.98	2.68	3.43
24.13	0.87	1.71	2.27	3.02
24.17	0.75	1.40	2.01	2.73
24.22	0.64	1.21	1.71	2.36
24.25	0.58	1.03	1.53	2.10
24.3	0.54	0.93	1.37	1.91
24.33	0.48	0.84	1.25	1.73
24.37	0.45	0.80	1.22	1.66
24.41	0.42	0.79	1.19	1.62
24.44	0.40	0.75	1.13	1.59
24.48	0.35	0.71	1.12	1.53
24.52	0.36	0.68	1.06	1.46
24.57	0.37	0.62	1.03	1.41
24.6	0.36	0.57	0.98	1.36
24.65	0.37	0.55	0.89	1.26
24.68	0.37	0.52	0.80	1.19
24.72	0.37	0.52	0.77	1.11
24.76	0.38	0.52	0.74	1.06
24.79	0.37	0.51	0.73	1.04
24.84	0.37	0.52	0.71	1.01
24.87	0.38	0.52	0.70	0.99
24.91	0.38	0.51	0.69	0.96
24.93	0.39	0.53	0.68	0.94
24.96	0.40	0.53	0.66	0.93
25	0.38	0.52	0.64	0.89
25.04	0.39	0.53	0.67	0.89
25.07	0.38	0.53	0.67	0.85
25.11	0.38	0.55	0.69	0.83
25.15	0.40	0.56	0.69	0.85
25.19	0.40	0.55	0.72	0.85
25.22	0.37	0.57	0.74	0.86
25.26	0.38	0.58	0.76	0.87

Freq	Scan voltage set point			
	20V	40V	60V	80V
26.31	0.40	0.67	0.84	1.00
26.35	0.39	0.67	0.85	1.01
26.38	0.39	0.66	0.86	1.01
26.4	0.40	0.69	0.86	1.03
26.44	0.40	0.68	0.85	1.01
26.47	0.40	0.67	0.83	0.98
26.5	0.39	0.65	0.81	0.92
26.53	0.38	0.64	0.80	0.89
26.57	0.40	0.64	0.80	0.87
26.6	0.38	0.64	0.81	0.89
26.64	0.40	0.67	0.81	0.90
26.67	0.40	0.66	0.83	0.94
26.71	0.40	0.66	0.84	0.96
26.74	0.40	0.67	0.87	0.98
26.78	0.40	0.69	0.87	1.01
26.81	0.40	0.68	0.88	1.03
26.85	0.40	0.68	0.89	1.04
26.88	0.40	0.68	0.91	1.06
26.92	0.40	0.69	0.90	1.09
26.94	0.39	0.68	0.92	1.11
26.98	0.40	0.70	0.94	1.12
27.02	0.40	0.70	0.95	1.14
27.05	0.42	0.71	0.95	1.16
27.08	0.40	0.71	0.97	1.19
27.11	0.41	0.69	0.96	1.19
27.13	0.40	0.72	0.96	1.19
27.16	0.40	0.71	0.97	1.20
27.19	0.40	0.71	0.96	1.24
27.23	0.41	0.73	0.98	1.24
27.25	0.42	0.73	1.01	1.22
27.29	0.40	0.73	1.00	1.25
27.33	0.40	0.73	1.00	1.26
27.36	0.40	0.73	1.01	1.28
27.39	0.40	0.73	1.02	1.27
27.41	0.41	0.73	1.01	1.28
27.45	0.41	0.73	1.03	1.29
27.48	0.40	0.75	1.04	1.30
27.51	0.40	0.73	1.04	1.31
27.54	0.41	0.76	1.03	1.30
27.57	0.41	0.75	1.02	1.32
27.6	0.41	0.74	1.03	1.30
27.63	0.40	0.76	1.05	1.33
27.66	0.42	0.74	1.05	1.33
27.68	0.42	0.75	1.05	1.36
27.7	0.42	0.76	1.05	1.37
27.72	0.43	0.76	1.06	1.37
27.73	0.42	0.78	1.08	1.38
27.76	0.42	0.77	1.07	1.37
27.77	0.43	0.77	1.09	1.39
27.79	0.42	0.76	1.07	1.39
27.81	0.42	0.79	1.09	1.39
27.81	0.42	0.77	1.08	1.39
27.83	0.43	0.78	1.07	1.39
27.84	0.44	0.78	1.09	1.39
27.86	0.43	0.78	1.08	1.40

22.14	0.54	1.01	1.36	2.18
22.18	0.53	0.98	1.37	2.11
22.21	0.55	1.03	1.38	2.14
22.25	0.55	1.05	1.41	2.16
22.3	0.57	1.03	1.45	2.20
22.34	0.59	1.05	1.50	2.19
22.37	0.59	1.07	1.54	2.26
22.41	0.60	1.09	1.55	2.29
22.45	0.60	1.09	1.57	2.32
22.49	0.59	1.10	1.56	2.33
22.51	0.60	1.10	1.58	2.34
22.55	0.60	1.12	1.58	2.34
22.59	0.62	1.12	1.59	2.30
22.63	0.62	1.14	1.62	2.27
22.66	0.62	1.14	1.58	2.09
22.7	0.62	1.14	1.53	1.92
22.75	0.60	1.14	1.49	1.77
22.78	0.61	1.13	1.46	1.96
22.82	0.62	1.12	1.39	2.05
22.86	0.60	1.14	1.45	2.06
22.9	0.60	1.16	1.55	2.14
22.93	0.62	1.18	1.64	2.27
22.97	0.63	1.22	1.71	2.38
23.01	0.64	1.21	1.73	2.38
23.04	0.64	1.24	1.77	2.44
23.08	0.67	1.28	1.82	2.48
23.11	0.68	1.31	1.87	2.57
23.15	0.70	1.36	1.96	2.68
23.19	0.72	1.39	1.98	2.67

25.29	0.39	0.61	0.77	0.87
25.33	0.40	0.60	0.75	0.84
25.37	0.39	0.60	0.74	0.84
25.4	0.39	0.60	0.71	0.83
25.44	0.38	0.61	0.69	0.80
25.48	0.40	0.61	0.68	0.77
25.51	0.40	0.60	0.68	0.78
25.54	0.38	0.61	0.69	0.76
25.58	0.40	0.62	0.67	0.78
25.61	0.38	0.61	0.68	0.78
25.65	0.40	0.62	0.69	0.78
25.66	0.39	0.62	0.68	0.79
25.7	0.40	0.61	0.69	0.79
25.74	0.39	0.62	0.69	0.80
25.77	0.39	0.62	0.71	0.81
25.81	0.40	0.62	0.71	0.82
25.85	0.39	0.61	0.73	0.83
25.88	0.38	0.62	0.72	0.83
25.92	0.40	0.62	0.73	0.85
25.95	0.40	0.63	0.73	0.85
25.99	0.40	0.64	0.76	0.87
26.03	0.39	0.62	0.76	0.87
26.06	0.40	0.64	0.77	0.89
26.1	0.39	0.63	0.78	0.89
26.13	0.40	0.64	0.79	0.91
26.17	0.39	0.63	0.80	0.93
26.2	0.38	0.65	0.80	0.93
26.24	0.39	0.65	0.82	0.95
26.28	0.39	0.65	0.83	0.96

27.86	0.43	0.77	1.10	1.40
27.88	0.43	0.78	1.07	1.39
27.88	0.44	0.78	1.10	1.41
27.89	0.43	0.77	1.08	1.41
27.9	0.44	0.77	1.07	1.41
27.9	0.43	0.77	1.09	1.40
27.92	0.44	0.77	1.09	1.41
27.92	0.42	0.77	1.10	1.39
27.92	0.43	0.78	1.08	1.39
27.93	0.44	0.78	1.07	1.40
27.94	0.42	0.77	1.10	1.38
27.93	0.44	0.77	1.08	1.39
27.94	0.43	0.77	1.09	1.39
27.95	0.44	0.77	1.07	1.39
27.95	0.43	0.78	1.08	1.38
27.95	0.44	0.77	1.07	1.38
27.95	0.44	0.78	1.08	1.37
27.96	0.44	0.78	1.08	1.38
27.96	0.42	0.78	1.08	1.38
27.97	0.43	0.77	1.08	1.38
27.97	0.43	0.76	1.07	1.39
27.97	0.44	0.77	1.08	1.38
27.98	0.44	0.77	1.06	1.39
27.98	0.44	0.76	1.08	1.38
27.98	0.44	0.76	1.07	1.38
27.98	0.44	0.77	1.07	1.37
27.98	0.44	0.77	1.07	1.39



B4 Transducer Array scan results

Freq	Scan voltage set point			
	40V	80V	120V	160V
28.97	1.78	3.27	4.73	6.22
23.41	2.13	4.03	5.71	7.41
23.45	2.11	3.97	5.66	7.41
23.49	2.09	3.94	5.69	7.39
23.53	2.07	3.93	5.60	7.29
23.58	2.05	3.87	5.62	7.24
23.62	2.01	3.84	5.55	7.17
23.67	2.00	3.79	5.55	7.18
23.72	1.98	3.72	5.47	7.16
23.76	1.99	3.72	5.42	7.13
23.81	1.98	3.63	5.32	7.18
23.85	1.92	3.56	5.17	7.02
23.9	1.87	3.46	5.10	6.91
23.94	1.82	3.40	4.99	6.86
23.99	1.82	3.43	4.96	6.80
24.04	1.87	3.47	5.14	6.86
24.08	1.89	3.54	5.15	6.88
24.13	1.89	3.57	5.23	6.91
24.17	1.89	3.56	5.25	6.93
24.22	1.91	3.55	5.26	6.96
24.27	1.89	3.56	5.27	7.01
24.32	1.88	3.57	5.31	7.07
24.34	1.89	3.59	5.35	7.14
24.39	1.89	3.57	5.40	7.18
24.43	1.85	3.56	5.42	7.14
24.47	1.81	3.52	5.32	7.01
24.53	1.81	3.48	5.27	7.14
24.57	1.80	3.49	5.30	7.02
24.62	1.77	3.43	5.28	7.01
24.67	1.81	3.44	5.26	7.04
24.71	1.84	3.49	5.34	7.07
24.76	1.84	3.49	5.32	7.11
24.81	1.84	3.48	5.37	7.15
24.85	1.84	3.57	5.37	7.24
24.9	1.85	3.59	5.50	7.16
24.95	1.87	3.66	5.49	7.25
24.99	1.88	3.73	5.55	7.34
25.04	1.89	3.79	5.63	7.47
25.09	1.94	3.82	5.70	7.51
25.13	1.93	3.88	5.84	7.64
25.18	1.96	3.92	5.88	7.77
25.23	2.00	4.01	6.05	7.97
25.28	2.08	4.15	6.23	8.26
25.3	2.11	4.18	6.33	8.37
25.35	2.13	4.32	6.50	8.61
25.4	2.24	4.49	6.77	9.01
25.45	2.32	4.63	7.03	9.36
25.49	2.42	4.83	7.33	9.71
25.53	2.52	4.98	7.57	10.01
25.58	2.59	5.15	7.77	10.24
25.63	2.72	5.35	7.97	10.49
25.67	2.81	5.44	8.11	10.82
25.72	2.89	5.58	8.31	11.07
25.77	3.00	5.74	8.55	11.23
25.82	3.10	5.92	8.78	11.47

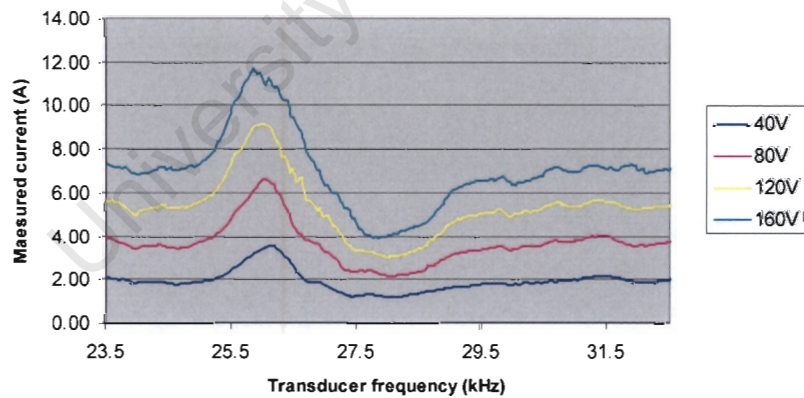
Freq	Scan voltage set point			
	40V	80V	120V	160V
27.18	1.48	2.92	4.40	5.98
27.23	1.42	2.70	4.09	5.73
27.25	1.37	2.60	4.08	5.57
27.3	1.32	2.45	3.85	5.30
27.34	1.28	2.41	3.63	5.28
27.39	1.23	2.37	3.52	5.16
27.43	1.21	2.34	3.40	4.80
27.48	1.22	2.36	3.33	4.78
27.53	1.28	2.34	3.31	4.40
27.56	1.24	2.41	3.34	4.32
27.62	1.28	2.40	3.31	4.08
27.66	1.29	2.41	3.30	4.01
27.71	1.30	2.41	3.26	4.05
27.75	1.30	2.39	3.24	3.93
27.79	1.25	2.37	3.20	3.96
27.84	1.23	2.31	3.15	3.91
27.88	1.23	2.25	3.11	3.95
27.93	1.20	2.20	3.08	3.99
27.97	1.19	2.16	3.00	3.99
28.02	1.21	2.17	3.01	4.01
28.06	1.17	2.18	3.06	4.06
28.11	1.21	2.17	3.06	4.08
28.16	1.20	2.20	3.06	4.14
28.17	1.21	2.20	3.08	4.21
28.21	1.19	2.21	3.11	4.22
28.26	1.24	2.24	3.15	4.26
28.31	1.23	2.25	3.18	4.30
28.35	1.30	2.29	3.25	4.35
28.4	1.30	2.27	3.30	4.40
28.44	1.31	2.30	3.34	4.47
28.49	1.32	2.36	3.39	4.49
28.53	1.37	2.40	3.45	4.54
28.57	1.39	2.45	3.52	4.60
28.62	1.43	2.54	3.57	4.67
28.66	1.46	2.63	3.77	4.75
28.71	1.49	2.68	3.85	4.92
28.75	1.49	2.70	3.94	5.08
28.79	1.52	2.78	4.02	5.21
28.84	1.53	2.90	4.11	5.35
28.88	1.55	2.95	4.26	5.53
28.92	1.59	3.01	4.42	5.70
28.97	1.60	3.09	4.56	5.85
29.01	1.62	3.15	4.61	6.03
29.05	1.66	3.18	4.69	6.12
29.1	1.68	3.22	4.78	6.22
29.12	1.68	3.22	4.77	6.24
29.17	1.71	3.28	4.84	6.29
29.21	1.71	3.29	4.90	6.34
29.25	1.70	3.30	4.91	6.41
29.29	1.70	3.33	4.93	6.42
29.34	1.74	3.33	4.94	6.48
29.38	1.72	3.33	4.97	6.48
29.43	1.76	3.36	4.96	6.52
29.47	1.75	3.36	5.02	6.54
29.51	1.79	3.40	5.03	6.52

Freq	Scan voltage set point			
	40V	80V	120V	160V
30.76	1.95	3.76	5.52	7.11
30.8	1.96	3.78	5.45	7.06
30.83	1.95	3.74	5.41	7.02
30.86	1.96	3.76	5.39	6.98
30.9	1.95	3.75	5.36	6.99
30.94	1.96	3.74	5.34	6.98
30.98	1.99	3.74	5.33	6.97
31.02	1.98	3.81	5.36	6.97
31.06	2.00	3.80	5.39	6.98
31.1	2.03	3.84	5.43	7.07
31.14	2.06	3.89	5.49	7.16
31.18	2.08	3.95	5.53	7.20
31.23	2.09	3.98	5.59	7.25
31.27	2.11	4.01	5.62	7.23
31.3	2.14	4.00	5.65	7.24
31.35	2.15	4.01	5.63	7.23
31.39	2.16	4.03	5.63	7.18
31.43	2.16	4.04	5.64	7.17
31.47	2.17	4.04	5.60	7.13
31.51	2.14	4.01	5.57	7.12
31.55	2.14	3.98	5.55	7.14
31.59	2.12	3.93	5.57	7.12
31.63	2.11	3.85	5.53	7.05
31.67	2.06	3.76	5.48	7.06
31.71	2.02	3.75	5.41	7.08
31.73	2.02	3.73	5.39	7.16
31.77	2.00	3.69	5.35	7.21
31.8	1.97	3.64	5.30	7.23
31.85	1.95	3.61	5.29	7.23
31.89	1.92	3.58	5.24	7.31
31.93	1.91	3.57	5.22	7.27
31.97	1.87	3.55	5.24	7.24
32	1.87	3.57	5.22	7.07
32.05	1.89	3.60	5.25	7.08
32.08	1.88	3.59	5.28	7.10
32.12	1.89	3.58	5.30	6.92
32.16	1.86	3.62	5.26	6.93
32.19	1.89	3.61	5.29	6.98
32.24	1.90	3.63	5.31	7.00
32.27	1.91	3.65	5.35	7.00
32.3	1.91	3.66	5.35	7.00
32.34	1.92	3.69	5.36	7.02
32.38	1.92	3.69	5.37	7.03
32.4	1.94	3.67	5.35	7.04
32.43	1.97	3.70	5.39	7.07
32.46	1.96	3.72	5.39	7.08
32.47	1.98	3.74	5.39	7.04
32.49	1.96	3.74	5.39	7.06
32.51	1.98	3.75	5.39	7.09
32.53	1.99	3.75	5.40	7.10
32.55	1.99	3.75	5.43	7.11
32.57	2.00	3.74	5.44	7.15
32.58	2.00	3.73	5.44	7.20
32.59	1.98	3.76	5.44	7.34
32.61	2.00	3.78	5.46	7.33

25.87	3.19	6.13	8.96	11.67
25.91	3.27	6.28	9.07	11.43
25.95	3.36	6.45	9.11	11.52
26.01	3.42	6.61	9.15	11.23
26.05	3.49	6.59	9.05	10.91
26.1	3.55	6.53	9.02	11.25
26.14	3.58	6.43	8.83	10.91
26.19	3.52	6.32	8.53	10.80
26.23	3.44	6.08	8.33	10.84
26.28	3.29	5.83	8.03	10.47
26.3	3.24	5.78	7.56	10.35
26.35	3.09	5.40	7.67	10.24
26.4	2.95	5.05	7.21	10.15
26.44	2.81	4.85	6.93	9.55
26.49	2.63	4.43	7.09	9.44
26.54	2.41	4.28	6.45	9.22
26.59	2.21	4.11	6.54	8.88
26.63	2.07	4.02	6.67	8.68
26.68	1.96	3.84	5.74	8.11
26.72	1.91	3.84	5.66	7.73
26.77	1.91	3.74	5.59	7.53
26.81	1.86	3.72	5.40	7.38
26.86	1.85	3.70	5.13	7.06
26.91	1.87	3.55	5.31	6.98
26.95	1.82	3.42	4.94	6.62
27	1.73	3.31	4.85	6.34
27.04	1.70	3.24	4.93	6.33
27.09	1.60	3.13	4.67	6.09
27.14	1.55	2.98	4.44	6.00

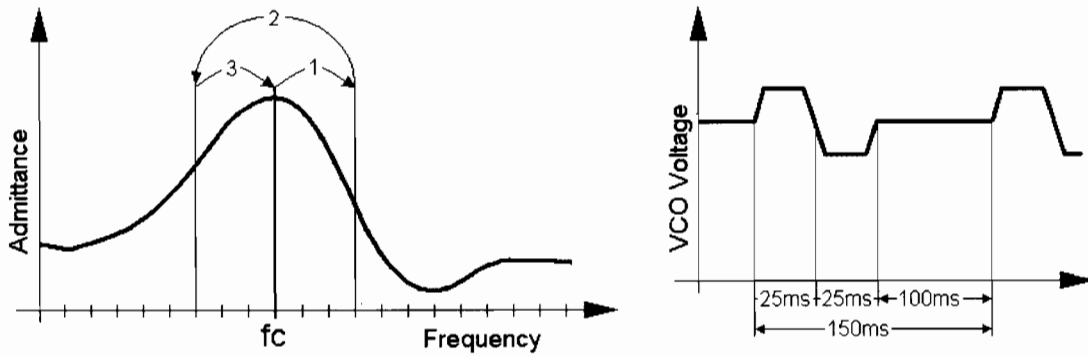
29.56	1.79	3.38	5.06	6.56
29.6	1.80	3.40	5.07	6.58
29.64	1.83	3.45	5.08	6.59
29.68	1.84	3.47	5.10	6.62
29.72	1.84	3.50	5.16	6.57
29.77	1.83	3.55	5.26	6.67
29.82	1.83	3.57	5.17	6.79
29.85	1.80	3.47	5.08	6.68
29.89	1.77	3.38	4.94	6.55
29.94	1.71	3.36	4.91	6.47
29.98	1.71	3.36	4.93	6.36
30	1.74	3.43	4.99	6.38
30.04	1.78	3.39	5.01	6.34
30.08	1.77	3.45	5.04	6.46
30.13	1.79	3.52	5.12	6.47
30.17	1.86	3.56	5.17	6.49
30.21	1.86	3.57	5.12	6.52
30.25	1.84	3.55	5.10	6.52
30.29	1.81	3.56	5.06	6.60
30.34	1.82	3.56	5.12	6.66
30.38	1.85	3.56	5.14	6.70
30.42	1.84	3.58	5.20	6.75
30.47	1.86	3.64	5.27	6.79
30.51	1.87	3.67	5.34	6.93
30.54	1.89	3.72	5.40	7.02
30.59	1.93	3.75	5.46	7.09
30.63	1.93	3.79	5.52	7.13
30.68	1.91	3.80	5.52	7.16
30.72	1.95	3.76	5.54	7.16

32.62	2.02	3.75	5.46	7.33
32.63	2.01	3.76	5.41	7.31
32.64	2.02	3.76	5.44	7.33
32.65	2.04	3.79	5.44	7.31
32.65	2.02	3.77	5.46	7.36
32.67	2.04	3.76	5.46	7.31
32.68	2.04	3.79	5.47	7.29
32.68	2.05	3.80	5.61	7.32
32.69	2.05	3.77	5.60	7.30
32.69	2.07	3.80	5.59	7.29
32.7	2.06	3.79	5.61	7.28
32.71	2.07	3.79	5.60	7.28
32.71	2.09	3.81	5.58	7.31
32.71	2.07	3.81	5.59	7.27
32.72	2.05	3.85	5.60	7.25
32.72	2.07	3.85	5.60	7.27
32.73	2.07	3.85	5.59	7.24
32.73	2.07	3.89	5.59	7.27
32.73	2.09	3.90	5.55	7.26
32.74	2.06	3.86	5.56	7.23
32.74	2.06	3.88	5.60	7.24
32.75	2.05	3.86	5.58	7.26
32.75	2.08	3.90	5.55	7.23
32.75	2.08	3.88	5.55	7.26
32.75	2.05	3.91	5.56	7.24
32.76	2.09	3.89	5.54	7.21
32.76	2.08	3.90	5.53	7.30

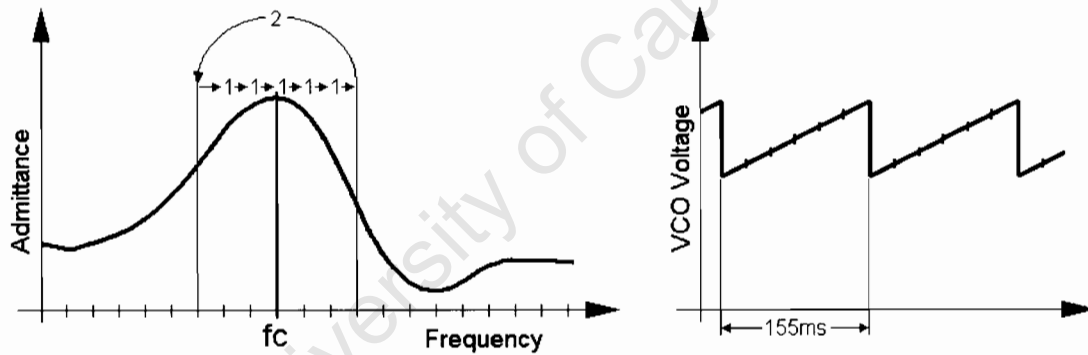


B5 Admittance locking control techniques results

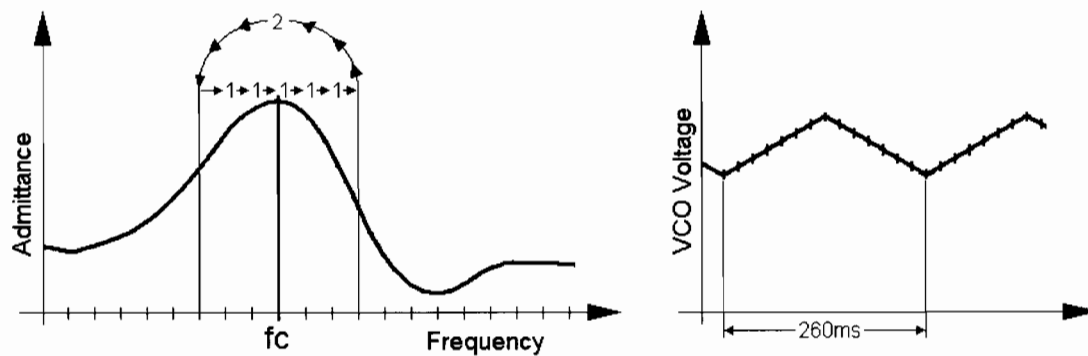
Peak Admittance locking



Saw tooth admittance locking

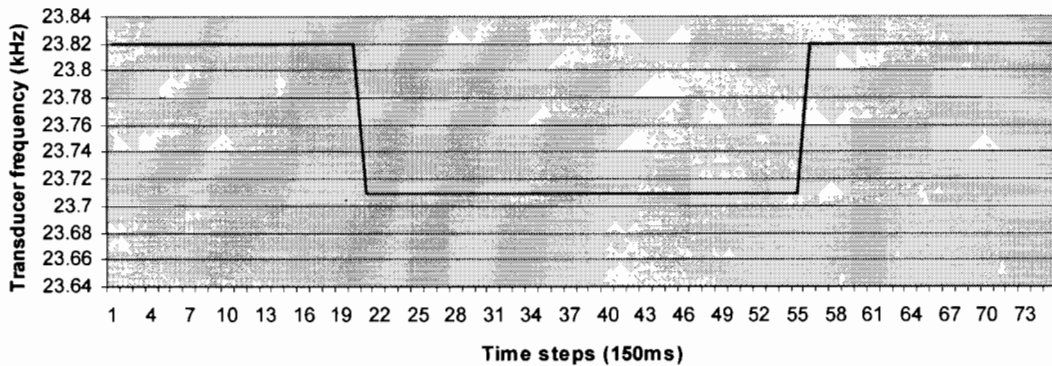
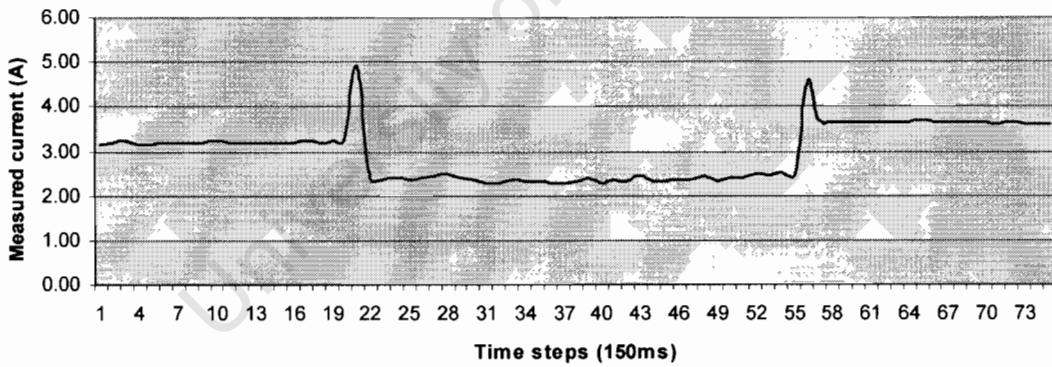


Triangle admittance locking



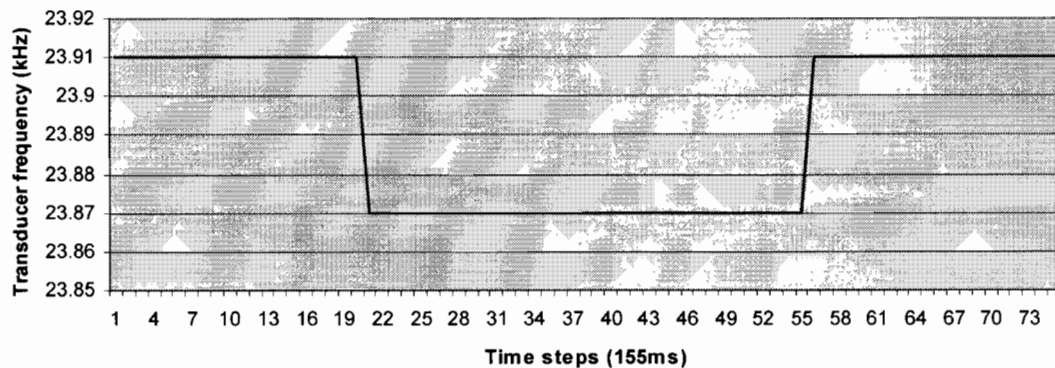
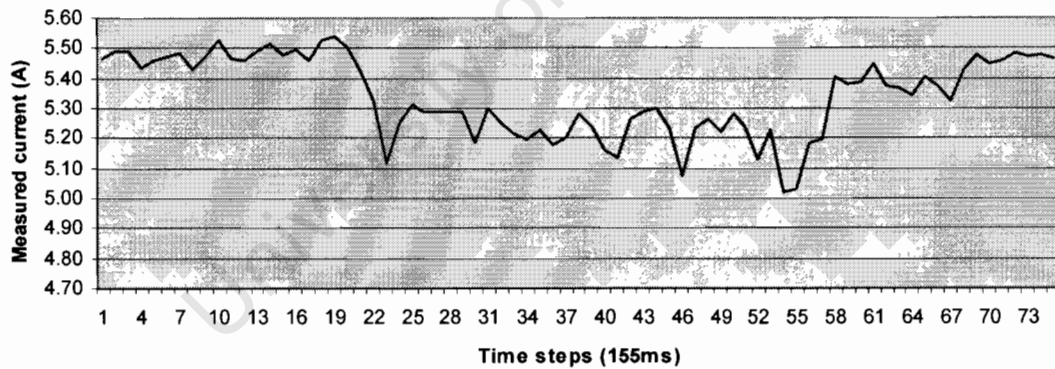
B6 Single transducer admittance locking results

Amp	Freq	Amp	Freq	Amp	Freq
3.13	23.82	2.40	23.71	2.39	23.71
3.19	23.82	2.45	23.71	2.48	23.71
3.21	23.82	2.48	23.71	2.46	23.71
3.15	23.82	2.42	23.71	2.54	23.71
3.16	23.82	2.34	23.71	2.45	23.71
3.19	23.82	2.28	23.71	4.53	23.82
3.18	23.82	2.29	23.71	3.70	23.82
3.17	23.82	2.36	23.71	3.63	23.82
3.20	23.82	2.34	23.71	3.63	23.82
3.21	23.82	2.31	23.71	3.65	23.82
3.17	23.82	2.27	23.71	3.63	23.82
3.19	23.82	2.28	23.71	3.64	23.82
3.19	23.82	2.31	23.71	3.63	23.82
3.18	23.82	2.39	23.71	3.65	23.82
3.17	23.82	2.29	23.71	3.67	23.82
3.20	23.82	2.38	23.71	3.65	23.82
3.22	23.82	2.33	23.71	3.66	23.82
3.18	23.82	2.43	23.71	3.65	23.82
3.21	23.82	2.32	23.71	3.65	23.82
3.24	23.82	2.32	23.71	3.64	23.82
4.93	23.71	2.38	23.71	3.61	23.82
2.41	23.71	2.35	23.71	3.64	23.82
2.38	23.71	2.43	23.71	3.58	23.82
2.41	23.71	2.34	23.71	3.58	23.82
2.38	23.71	2.39	23.71	3.61	23.82



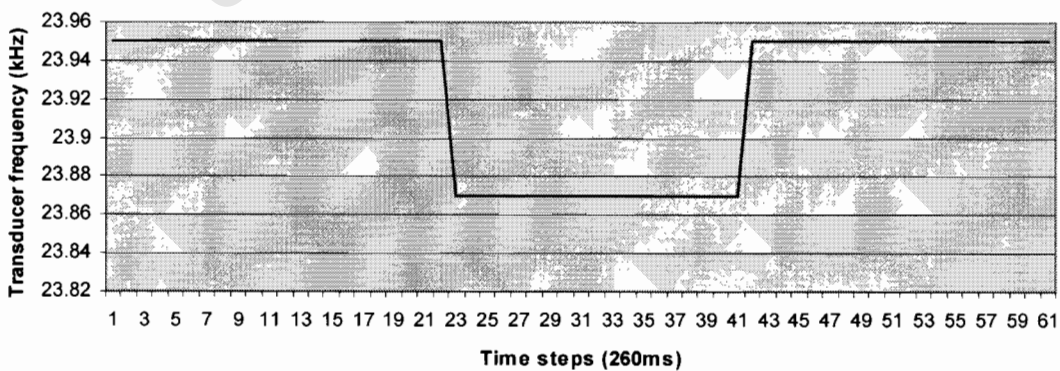
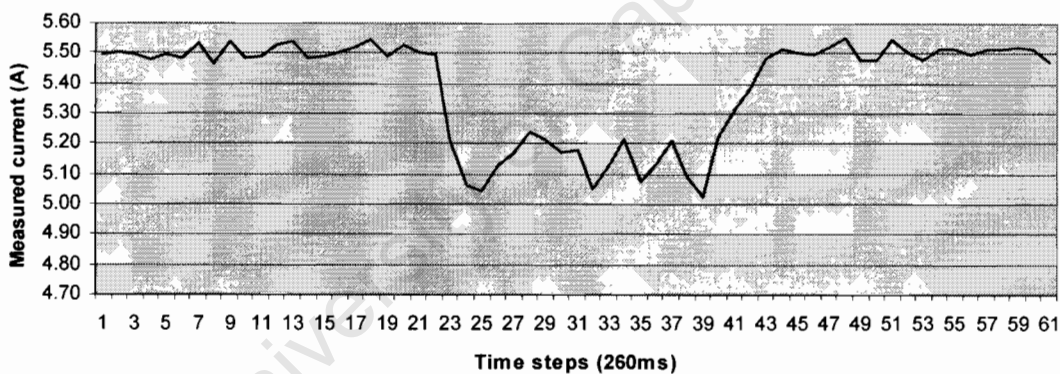
B7 Single transducer saw-tooth locking results

Amp	Freq	Amp	Freq	Amp	Freq
5.46	23.91	5.29	23.87	5.24	23.87
5.49	23.91	5.29	23.87	5.13	23.87
5.49	23.91	5.29	23.87	5.23	23.87
5.44	23.91	5.29	23.87	5.02	23.87
5.46	23.91	5.19	23.87	5.03	23.87
5.47	23.91	5.30	23.87	5.19	23.91
5.48	23.91	5.25	23.87	5.19	23.91
5.43	23.91	5.21	23.87	5.40	23.91
5.47	23.91	5.19	23.87	5.38	23.91
5.53	23.91	5.23	23.87	5.39	23.91
5.46	23.91	5.18	23.87	5.45	23.91
5.46	23.91	5.20	23.87	5.37	23.91
5.49	23.91	5.28	23.87	5.37	23.91
5.51	23.91	5.24	23.87	5.35	23.91
5.48	23.91	5.16	23.87	5.40	23.91
5.50	23.91	5.14	23.87	5.37	23.91
5.46	23.91	5.26	23.87	5.32	23.91
5.53	23.91	5.29	23.87	5.43	23.91
5.54	23.91	5.30	23.87	5.48	23.91
5.51	23.91	5.23	23.87	5.45	23.91
5.42	23.87	5.08	23.87	5.46	23.91
5.32	23.87	5.23	23.87	5.48	23.91
5.12	23.87	5.26	23.87	5.47	23.91
5.25	23.87	5.22	23.87	5.48	23.91
5.31	23.87	5.28	23.87	5.46	23.91



B8 Single transducer triangle locking results

Amp	Freq	Amp	Freq	Amp	Freq
5.50	23.95	5.50	23.95	5.38	23.95
5.51	23.95	5.21	23.87	5.48	23.95
5.50	23.95	5.06	23.87	5.51	23.95
5.48	23.95	5.04	23.87	5.51	23.95
5.50	23.95	5.13	23.87	5.50	23.95
5.48	23.95	5.17	23.87	5.52	23.95
5.53	23.95	5.24	23.87	5.55	23.95
5.46	23.95	5.21	23.87	5.48	23.95
5.54	23.95	5.17	23.87	5.48	23.95
5.48	23.95	5.18	23.87	5.55	23.95
5.49	23.95	5.05	23.87	5.51	23.95
5.53	23.95	5.13	23.87	5.48	23.95
5.54	23.95	5.21	23.87	5.51	23.95
5.48	23.95	5.08	23.87	5.51	23.95
5.49	23.95	5.13	23.87	5.50	23.95
5.51	23.95	5.21	23.87	5.51	23.95
5.52	23.95	5.09	23.87	5.51	23.95
5.55	23.95	5.03	23.87	5.52	23.95
5.49	23.95	5.22	23.87	5.51	23.95
5.53	23.95	5.31	23.87	5.47	23.95
5.51	23.95				



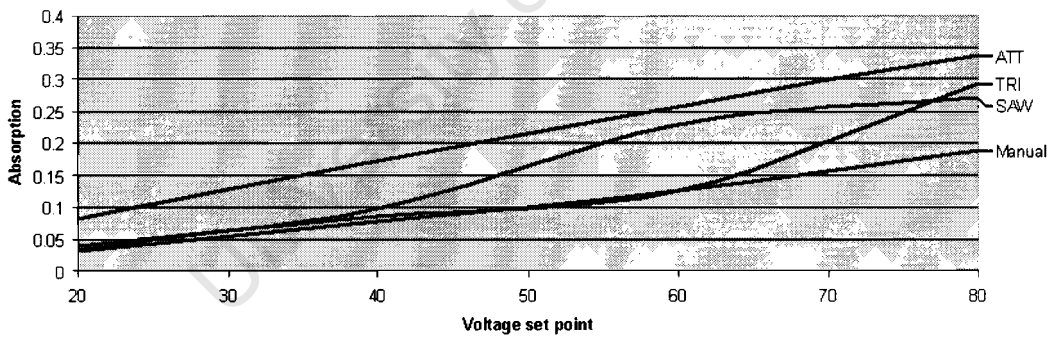
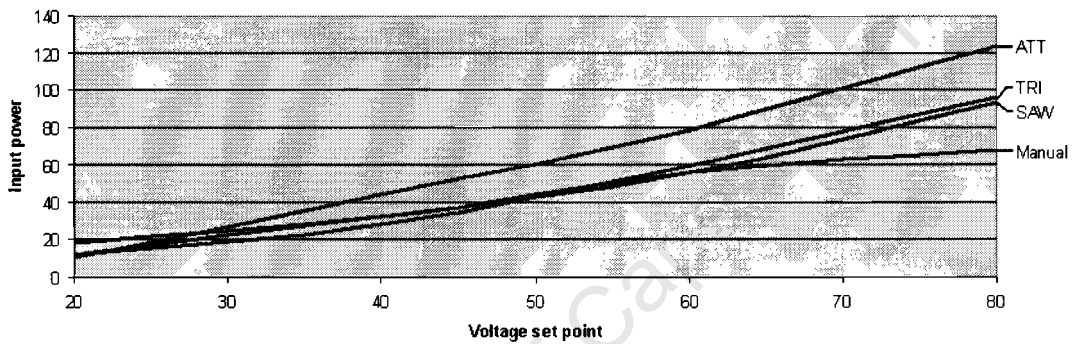
B9 Single Transducer power transfer results

Manual mode		
Volt set point	Input power	Absorption
20V	18W	0.031
40V	32W	0.078
60V	56W	0.126
80V	68W	0.188

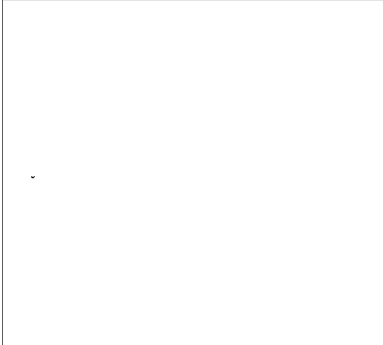
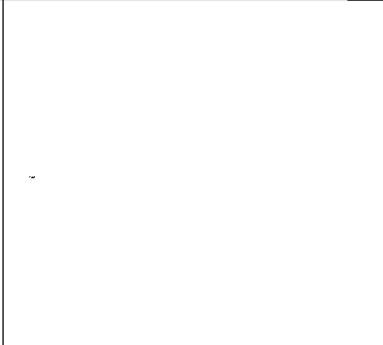
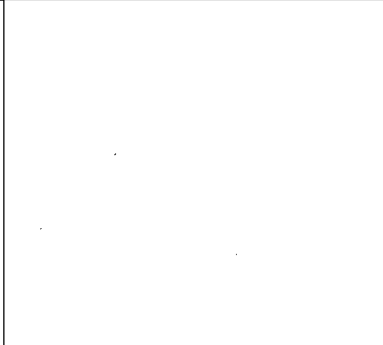
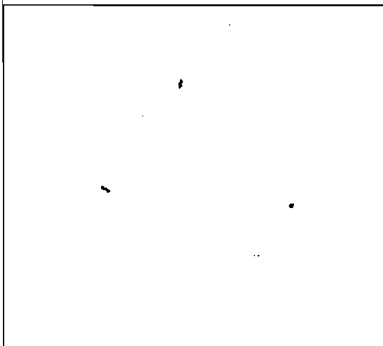



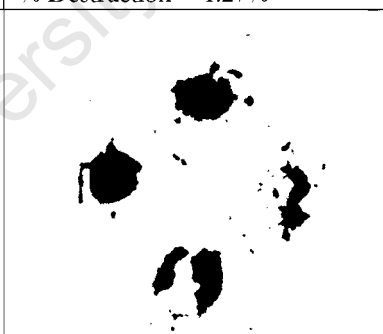
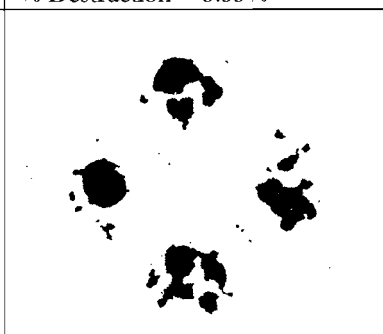
Admittance mode		
Volt set point	Input power	Absorption
20V	10W	0.081
40V	44W	0.172
60V	79W	0.258
80V	124W	0.338

Saw tooth mode		
Volt set point	Input power	Absorption
20V	12W	0.034
40V	32W	0.098
60V	56W	0.229
80V	94W	0.291

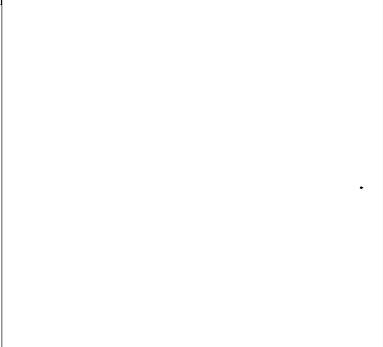

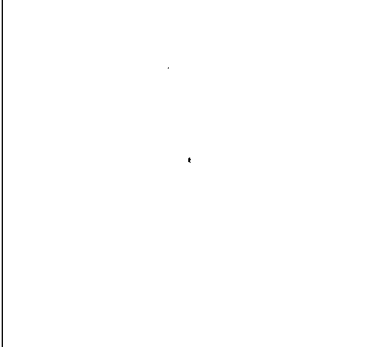
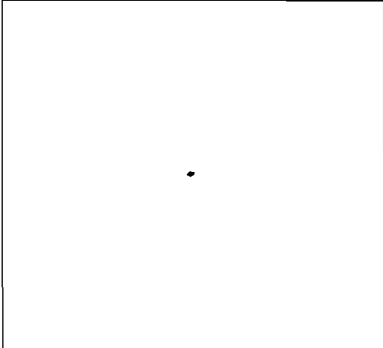
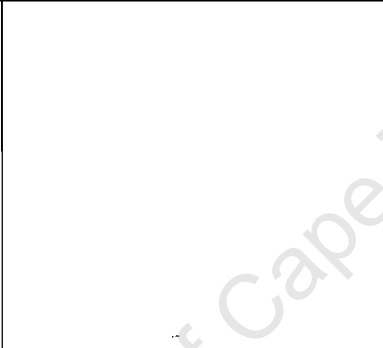
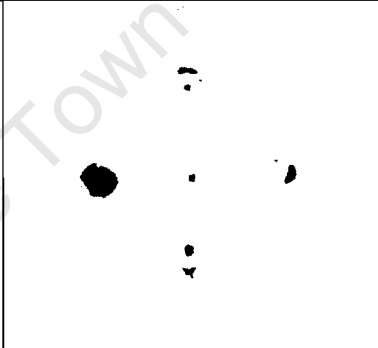


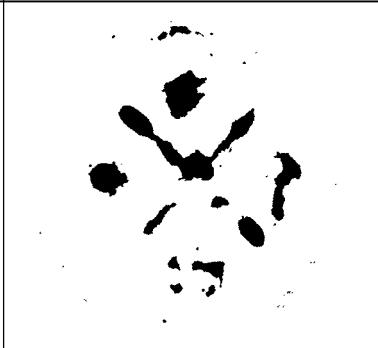
Triangle mode		
Volt set point	Input power	Absorption
20V	12W	0.039
40V	28W	0.085
60V	60W	0.200
80V	96W	0.293



B10 Transducer array Admittance locking power transfer results

 <p>Voltage set point = 20V Resonant frequency = 26.14 kHz Input Power = 6W % Destruction = 0%</p>	 <p>Voltage set point = 40V Resonant frequency = 26.00 kHz Input Power = 18W % Destruction = 0%</p>	 <p>Voltage set point = 60V Resonant frequency = 25.84 kHz Input Power = 32W % Destruction = 0.22%</p>
 <p>Voltage set point = 80V Resonant frequency = 26.15 kHz Input Power = 56W % Destruction = 0.55%</p>	 <p>Voltage set point = 100V Resonant frequency = 26.11 kHz Input Power = 80W % Destruction = 1.27%</p>	 <p>Voltage set point = 120V Resonant frequency = 25.96 kHz Input Power = 104W % Destruction = 3.53%</p>
 <p>Voltage set point = 140V Resonant frequency = 26.5 kHz Input Power = 140W % Destruction = 6.54%</p>	 <p>Voltage set point = 160V Resonant frequency = 26.29 kHz Input Power = 180W % Destruction = 8.8%</p>	 <p>Voltage set point = 180V Resonant frequency = 24.69 kHz Input Power = 220W % Destruction = 9.05%</p>

B11 Transducer array Saw tooth locking power transfer results

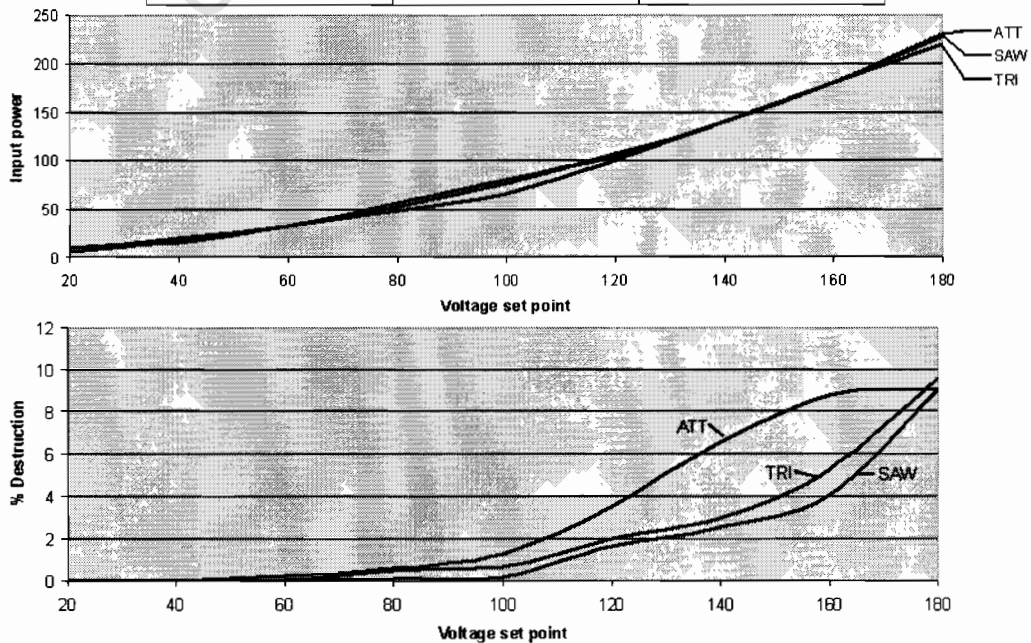
 <p>Voltage set point = 20V Resonant frequency = 25.42 kHz Input Power = 10W % Destruction = 0%</p>	 <p>Voltage set point = 40V Resonant frequency = 25.42 kHz Input Power = 16W % Destruction = 0%</p>	 <p>Voltage set point = 60V Resonant frequency = 24.31 kHz Input Power = 32W % Destruction = 0.06%</p>
 <p>Voltage set point = 80V Resonant frequency = 24.24 kHz Input Power = 48W % Destruction = 0.09%</p>	 <p>Voltage set point = 100V Resonant frequency = 24.39 kHz Input Power = 66W % Destruction = 0.13%</p>	 <p>Voltage set point = 120V Resonant frequency = 24.39 kHz Input Power = 100W % Destruction = 1.64%</p>
 <p>Voltage set point = 140V Resonant frequency = 24.52 kHz Input Power = 140W % Destruction = 2.48%</p>	 <p>Voltage set point = 160V Resonant frequency = 24.55 kHz Input Power = 180W % Destruction = 4.05%</p>	 <p>Voltage set point = 180V Resonant frequency = 24.93 kHz Input Power = 228W % Destruction = 9.01%</p>

B12 Transducer array Triangle locking power transfer results

<p>Voltage set point = 20V Resonant frequency = 25.76 kHz Input Power = 10W % Destruction = 0%</p>	<p>Voltage set point = 40V Resonant frequency = 25.6 kHz Input Power = 20W % Destruction = 0%</p>	<p>Voltage set point = 60V Resonant frequency = 24.88 kHz Input Power = 32W % Destruction = 0.02%</p>
<p>Voltage set point = 80V Resonant frequency = 24.88 kHz Input Power = 52W % Destruction = 0.47%</p>	<p>Voltage set point = 100V Resonant frequency = 24.98 kHz Input Power = 76W % Destruction = 0.65%</p>	<p>Voltage set point = 120V Resonant frequency = 25.2 kHz Input Power = 106W % Destruction = 1.99%</p>
<p>Voltage set point = 140V Resonant frequency = 25.5 kHz Input Power = 140W % Destruction = 2.96%</p>	<p>Voltage set point = 160V Resonant frequency = 25.5 kHz Input Power = 180W % Destruction = 5.28%</p>	<p>Voltage set point = 180V Resonant frequency = 25.13 kHz Input Power = 230W % Destruction = 9.56%</p>

B13 Transducer array power transfer results

Admittance mode		
Volt set point	Input power	% Destruction
20V	6W	0%
40V	18W	0%
60V	32W	0.22%
80V	56W	0.55%
100V	80W	1.27%
120V	104W	3.53%
140V	140W	6.54%
160V	180W	8.8%
180V	220W	9.05%
Saw tooth mode		
Volt set point	Input power	% Destruction
20V	10W	0%
40V	16W	0%
60V	32W	0.06%
80V	48W	0.09%
100V	66W	0.13%
120V	100W	1.64%
140V	140W	2.48%
160V	180W	4.05%
180V	228W	9.01%
Triangle mode		
Volt set point	Input power	% Destruction
20V	10W	0%
40V	20W	0%
60V	32W	0.02%
80V	52W	0.47%
100V	76W	0.65%
120V	106W	1.99%
140V	140W	2.96%
160V	180W	5.28%
180V	230W	9.56%



Appendix C - Detailed design

- C1 Power layer - Rectifier and filter
 - C1.1 Power switch (SW1)
 - C1.2 Input fuse (F1)
 - C1.3 Input rectifier (DB1)
 - C1.4 Filter capacitors (C1)
 - C1.5 Capacitor charging circuit
 - C1.6 Relay RL1
- C2 Power layer - Buck regulator and filter
 - C2.1 Input filter capacitors (C1)
 - C2.2 Switching MOSFET (M1)
 - C2.3 MOSFET Heatsink selection
 - C2.4 Filter Inductor (L1)
 - C2.6 Diode D1
- C3 Power layer - H-Bridge Inverter
 - C3.1 Switching component selection
- C4 Power layer - Power filter
- C5 Power interface layer - Buck regulator driver
 - C5.1 Selection of the bootstrap capacitor (C1)
- C6 Power interface layer - H-Bridge driver
- C7 Power interface layer - V and I Sensor
- C8 Signal layer - Voltage and current signal conditioning
- C9 Signal layer - Voltage Comparator
 - C9.1 R2 and C1 selection
- C10 Signal layer - Voltage controlled oscillator
- C11 Control layer - Microcontroller
- C12 Control layer - FPGA
- C13 Software layer - Microcontroller program
 - C13.1 Transducer auto detect scan flowchart
 - C13.2 Admittance locking flowchart

C13.3 Saw-tooth locking flowchart

C13.4 Triangle locking flowchart

C13.5 Micro program

C14 Software layer – FPGA logic program

C14.1 Sinpwm2dec

C14.2 Sinpwm2

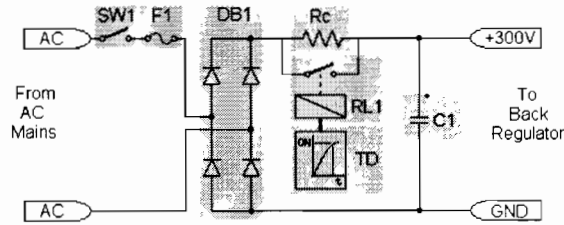
C14.3 Mod4a

C14.4 Lead_lag

C14.5 Power1

University of Cape Town

C1 Power layer - Rectifier and filter



C1.1 Power switch (SW1)

Worst-case input power is determined by dividing the maximum output power 1000W by the lowest expected efficiency of 80 %.

$$P_i = P_o / \eta$$

$$P_i = 1000 \text{ W} / 0.8$$

$$P_i = 1250 \text{ W}$$

Input Power	P_i	=	1250	W
Output Power	P_o	=	1000	W
Efficiency	η	=	80	%

The minimum input voltage is determined by the following formula:

$$V_{imin(220)} = (V_{i(220)} \times 0.85 \times \sqrt{2}) - 2V_f$$

$$V_{imin(220)} = (220 \text{ V} \times 0.85 \times \sqrt{2}) - (2 \times 1 \text{ V})$$

$$V_{imin(220)} = 262.46 \text{ V}$$

Minimum possible direct input voltage with 220 V line	$V_{imin(220)}$	=	262.46	V
Nominal direct input voltage with 220 V line	$V_{i(220)}$	=	220	V
Forward voltage drop	V_f	=	1	V

The average input current is calculated by dividing the maximum input power by the minimum input voltage.

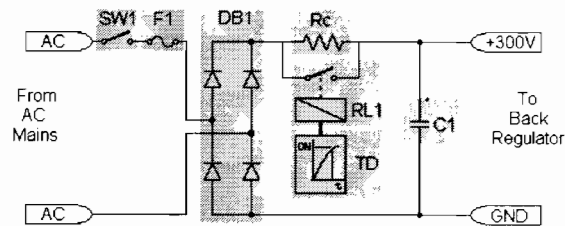
$$I_{iAV(220)} = P_i / V_{imin(220)}$$

$$I_{iAV(220)} = 1250 \text{ W} / 262.46 \text{ V}$$

$$I_{iAV(220)} = 4.76 \text{ A}$$

Mean converter input current with line 220 V	$I_{iAV(220)}$	=	4.76	A
Input Power	P_i	=	1250	W
Minimum possible direct input voltage with 220 V line	$V_{imin(220)}$	=	262.46	V

A 250V, 5A switch was selected.



C1.2 Input fuse (F1)

$$I_{iAV(220)} = 4.76 \text{ A}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

A 250V, 5A slow-blow fuse was selected.

C1.3 Input rectifier (DB1)

Selecting the input rectifier DB1 will depend on the following three factors:

1. Working peak reverse voltage
2. Average rectifier forward current
3. Operating junction temperature

The peak reverse voltage is determined by multiplying the nominal line voltage by 2.83.

$$V_{m} \geq 2.83 \times V_{i(220)}$$

$$V_{m} \geq 2.83 \times 220 \text{ V}$$

$$V_{m} \geq 622.6 \text{ V}$$

Peak repetitive reverse voltage

$$V_{m} = 622.6 \text{ V}$$

Nominal direct input voltage with 220 V line

$$V_{i(220)} = 220 \text{ V}$$

The average rectifier forward current is equal to the average input current.

$$I_{iAV(220)} = 4.76 \text{ A}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

$$P_D = I_{iAV(220)} \times V_F$$

$$P_D = 4.76 \text{ A} \times 1.1 \text{ V}$$

$$P_D = 5.236 \text{ W}$$

Power dissipated in diode

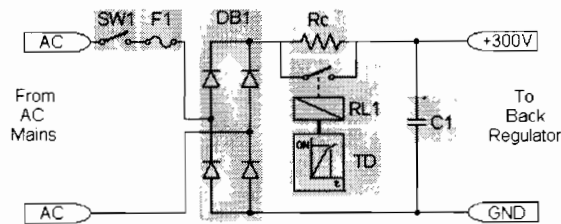
$$P_D = 5.236 \text{ W}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

Diode forward voltage drop

$$V_F = 1.1 \text{ V}$$



Operating junction temperature

$$\Delta T_j = P_D \times R_{thjc}$$

$$\Delta T_j = 5.236 \text{ W} \times 15 \text{ }^\circ\text{C/W}$$

$$\Delta T_j = 78.54 \text{ }^\circ\text{C}$$

Junction temperature rise

Power dissipated in diode

Thermal resistance of junction to case

ΔT_j	=	78.54	$^\circ\text{C}$
P_D	=	5.236	W
R_{thjc}	=	15	$^\circ\text{C/W}$

An 800 V, 6A bridge rectifier was selected.

C1.4 Filter capacitors (C1)

C1 is determined for worst-case conditions, that being low efficiency and low input voltage.

The maximum peak-to-peak ripple voltage of the output filter must not exceed 5% of the nominal input voltage.

$$V_{in(220)} = \sqrt{2} \times V_{i(220)}$$

$$V_{in(220)} = \sqrt{2} \times 220 \text{ V}$$

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage

Nominal direct input voltage with 220 V line

$V_{in(220)}$	=	311	V
$V_{i(220)}$	=	220	V

$$V_{p-p} = V_{in(220)} \times r$$

$$V_{p-p} = 311 \text{ V} \times 0.05$$

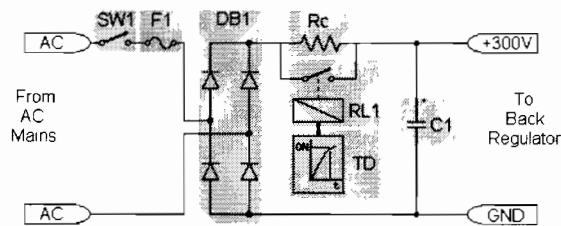
$$V_{p-p} = 15.55 \text{ V}$$

Ripple voltage, peak-to-peak value

Nominal direct input voltage

Percentage ripple

V_{p-p}	=	15.55	V
$V_{in(220)}$	=	311	V
r	=	5	$\%$



The following formula is used to calculate the filter capacitor.

$$C_e = (I_{iAV(220)} / V_{p-p}) \times (T / 2)$$

$$C_e = (4.76 \text{ A} / 15.55 \text{ V}) \times (10 \text{ ms} / 2)$$

$$C_e = 1530 \mu\text{F}$$

Effective capacitance

$$C_e = 1530 \mu\text{F}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

Ripple voltage, peak-to-peak value

$$V_{p-p} = 15.55 \text{ V}$$

Period ($T = 1/f$)

$$T = 10 \text{ ms}$$

Underestimating the RMS current in the filter capacitor can lead to the destruction of this component. This is due to the heat generated in this component due to the I^2R losses in the capacitor.

$$I_{C_{rms}} = I_{iAV(220)} \sqrt{(0.5k_{fD}^2 + k_{fi}^2 - 2)}$$

$$I_{C_{rms}} = 4.76 \text{ A} \sqrt{(0.5 \times 4.6^2 + 1.5^2 - 2)}$$

$$I_{C_{rms}} = 15.66 \text{ A}$$

Alternating current loading of capacitor

$$I_{C_{rms}} = 15.66 \text{ A}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

Diode current form factor

$$k_{fD} = 4.6$$

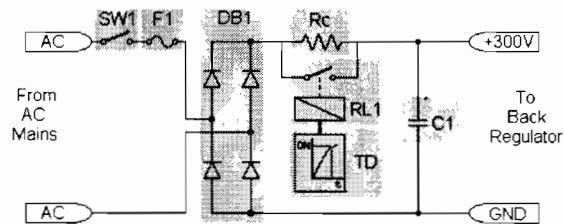
Converter input current form factor

$$k_{fi} = 1.5$$

C1 represents two capacitors C_{LF} and C_{HF} :

C_{LF} is an electrolytic capacitors (400 V, three 470 μ F and one 220 μ F)

C_{HF} is a high frequency response capacitor (400 V, 1 μ F)



C1.5 Capacitor charging circuit

R_c is determined for worst-case conditions, that being Peak supply voltage and fully discharged capacitor.

$$R_c = V_{in(220)} / I_{iAV(220)}$$

$$R_c = 311V / 4.76A$$

$$R_c = 65.34\Omega$$

Capacitor charge resistor

$$R_c = 65.34 \quad \Omega$$

Nominal direct input voltage

$$V_{in(220)} = 311 \quad V$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \quad A$$

An 100 Ω , 5W resistor was selected.

C1.6 Relay RL1

Selection of Relay RL1 depended on the following two factors:

4. Maximum possible input voltage
5. Average current

$$V_{in(220)} = \sqrt{2} \times V_{i(220)}$$

$$V_{in(220)} = \sqrt{2} \times 220 \text{ V}$$

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage

$$V_{in(220)} = 311 \quad V$$

Nominal direct input voltage with 220 V line

$$V_{i(220)} = 220 \quad V$$

The average Relay current is equal to the average input current.

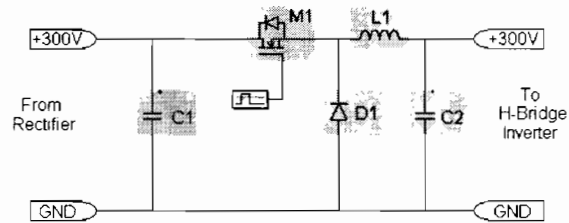
$$I_{iAV(220)} = 4.76 \text{ A}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \quad A$$

An 5A relay was selected.

C2 Power layer - Buck regulator and filter



C2.1 Input filter capacitors (C1)

The capacitor C1 was designed in Appendix C1.4

C2.2 Switching MOSFET (M1)

Selecting the input rectifier Misfit's will depend on the following three factors:

6. Maximum possible input voltage
7. Average MOSFET current

$$V_{in(220)} = \sqrt{2} \times V_{i(220)}$$

$$V_{in(220)} = \sqrt{2} \times 220 \text{ V}$$

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage with 220 V line

$$V_{i(220)} = 220 \text{ V}$$

The average MOSFET current is equal to the average rectifier forward current.

$$I_{iAV(220)} = 4.76 \text{ A}$$

Mean converter input current with line 220 V

$$I_{iAV(220)} = 4.76 \text{ A}$$

The IRFP460 was selected for this project.

C2.3 MOSFET Heatsink selection

$$I'_{Dmax} = I_{Dmax} \times 1.4$$

$$I'_{Dmax} = 4.76 \text{ A} \times 1.4$$

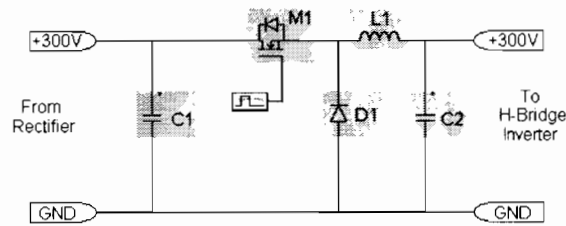
$$I'_{Dmax} = 6.664 \text{ A}$$

True maximum drain current

$$I'_{Dmax} = 6.664 \text{ A}$$

Maximum drain current

$$I_{Dmax} = 4.76 \text{ A}$$



$$P_{T_{rc}} = R_{DS(on)max} \times I_{Dmax}^2 \times \delta_{Tmax}$$

$$P_{T_{rc}} = 0.27 \Omega \times 6.664^2 \text{ A} \times 0.9$$

$$P_{T_{rc}} = 10.79 \text{ W}$$

Conduction loss

$$P_{T_{rc}} = 10.79 \text{ W}$$

On-state resistance

$$R_{DS(on)max} = 0.27 \Omega$$

True maximum drain current

$$I_{Dmax} = 6.664 \text{ A}$$

Maximum duty cycle

$$\delta_{Tmax} = 0.9$$

$$P_{T_{rs(on)}} = 1/6 \times V_{imax} \times I_{Dmax} \times t_r \times f_s$$

$$P_{T_{rs(on)}} = 1/6 \times 311 \text{ V} \times 6.664 \text{ A} \times 81 \text{ ns} \times 100 \text{ kHz}$$

$$P_{T_{rs(on)}} = 2.798 \text{ W}$$

Turn-on loss

$$P_{T_{rs(on)}} = 2.798 \text{ W}$$

Maximum possible input voltage

$$V_{imax} = 311 \text{ V}$$

True maximum drain current

$$I_{Dmax} = 6.664 \text{ A}$$

Rise time

$$t_r = 81 \text{ ns}$$

Maximum switching frequency

$$f_s = 100 \text{ kHz}$$

$$P_{T_{rs(off)}} = 1/6 \times V_{imax} \times I_{Dmax} \times t_f \times f_s$$

$$P_{T_{rs(off)}} = 1/6 \times 311 \text{ V} \times 6.664 \text{ A} \times 65 \text{ ns} \times 100 \text{ kHz}$$

$$P_{T_{rs(off)}} = 2.245 \text{ W}$$

Turn-off loss

$$P_{T_{rs(off)}} = 2.245 \text{ W}$$

Maximum possible input voltage

$$V_{imax} = 311 \text{ V}$$

True maximum drain current

$$I_{Dmax} = 6.664 \text{ A}$$

Rise time

$$t_r = 65 \text{ ns}$$

Switching frequency

$$f_s = 100 \text{ kHz}$$

$$P_{T_{r(tot)}} = P_{T_{rc}} + P_{T_{rs(on)}} + P_{T_{rs(off)}}$$

$$P_{T_{r(tot)}} = 10.79 \text{ W} + 2.798 \text{ W} + 2.245 \text{ W}$$

$$P_{T_{r(tot)}} = 15.833 \text{ W}$$

Total MOSFET loss

$$P_{T_{r(tot)}} = 15.833 \text{ W}$$

Conduction loss

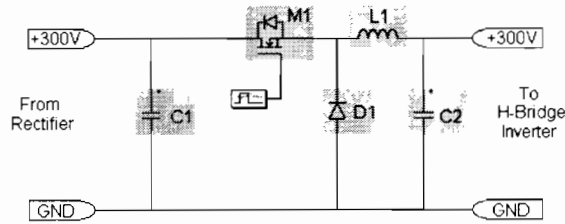
$$P_{T_{rc}} = 10.79 \text{ W}$$

Turn-on loss

$$P_{T_{rs(on)}} = 2.798 \text{ W}$$

Turn-off loss

$$P_{T_{rs(off)}} = 2.245 \text{ W}$$



$$R_{thca} \leq ((\theta_{jmax} - \theta_{amax}) / P_{Tr(tot)}) - R_{thjc}$$

$$R_{thca} \leq ((125\text{ }^{\circ}\text{C} - 55\text{ }^{\circ}\text{C}) / 15.833\text{ W}) - 0.5\text{ }^{\circ}\text{C/W}$$

$$R_{thca} \leq 3.92\text{ }^{\circ}\text{C/W}$$

Thermal resistance of heatsink

Maximum junction temperature

Maximum ambient temperature

Total MOSFET loss

Thermal resistance, junction to case

R_{thca}	=	3.92	$^{\circ}\text{C/W}$
θ_{jmax}	=	125	$^{\circ}\text{C}$
θ_{amax}	=	55	$^{\circ}\text{C}$
$P_{Tr(tot)}$	=	15.833	W
R_{thjc}	=	0.5	$^{\circ}\text{C/W}$

C2.4 Filter Inductor (L1)

$$I_{L(avg)} = P_{o(max)} / V_{o(min)}$$

$$= 1.25\text{kW} / 120\text{V}$$

$$= 10.42\text{A}$$

Average inductor current

Maximum output power

Minimum output voltage at full power

$I_{L(avg)}$	=	10.42	A
$P_{o(max)}$	=	1.25	kW
$V_{o(min)}$	=	120	V

$$I_{p-p} = I_{out} \times r$$

$$= 10.42\text{A} \times 0.01$$

$$= 104.2\text{mA}$$

Ripple current, peak-to-peak value

Average inductor current

Percentage ripple

I_{p-p}	=	104.2	mA
$I_{L(avg)}$	=	10.42	A
r	=	1	%

$$L1 = (V_{i(avg)} \times \delta_{T(min)} (1 - \delta_{T(min)})) / (f \times I_{p-p})$$

$$= (300\text{V} \times (0.4)(1 - 0.4)) / (60\text{kHz} \times 104.2\text{mA})$$

$$= 11.52\text{mH}$$

Inductor value

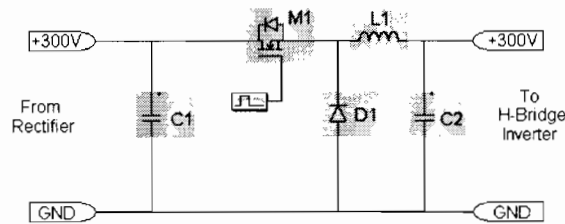
Average input voltage

Minimum duty cycle at full power

Minimum converter operating frequency

Ripple current, peak-to-peak value

L1	=	11.52	mH
$V_{i(avg)}$	=	300	V
$\delta_{T(min)}$	=	0.4	
f	=	60	kHz
I_{p-p}	=	104.2	mA



C2.5 Filter Capacitor (C2)

$$\begin{aligned} V_{p-p} &= V_{o(avg)} \times r \\ &= 120V \times 0.01 \\ &= 1.2V_{p-p} \end{aligned}$$

Ripple voltage, peak-to-peak value
Average output voltage
Percentage ripple

$$\begin{aligned} V_{p-p} &= 1.2 \text{ V} \\ V_{o(avg)} &= 120 \text{ V} \\ r &= 1 \% \end{aligned}$$

$$\begin{aligned} C2 &= (V_{i(avg)} \times \delta_{T(min)} (1 - \delta_{T(min)})) / (8 \times L1 \times f^2 \times V_{p-p}) \\ &= (300V \times (0.4)(1 - 0.4)) / (8 \times 11.52mH \times (60kHz)^2 \times 1.2V_{p-p}) \\ &= 180nF \end{aligned}$$

Capacitor value
Average input voltage
Minimum duty cycle at full power
Inductor value
Minimum converter operating frequency
Ripple voltage, peak-to-peak value

$$\begin{aligned} C1 &= 180 \text{ nF} \\ V_{i(avg)} &= 300 \text{ V} \\ \delta_{T(min)} &= 0.4 \\ L1 &= 11.52 \text{ mH} \\ f &= 60 \text{ kHz} \\ V_{p-p} &= 1.2 \text{ V} \end{aligned}$$

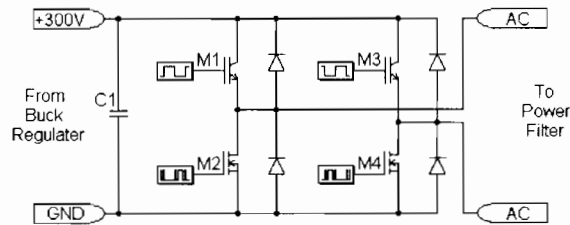
C2.6 Diode D1

$$\begin{aligned} I_{D1(avg)} &= (T_{off} / T) \times I_{o(avg)} \\ &= 0.6 \times 10.42A \\ &= 6.252A \end{aligned}$$

Average diode current
Off duty cycle
Average output current

$$\begin{aligned} I_{D1(avg)} &= 6.252 \text{ A} \\ (T_{off}/T) &= 0.6 \\ I_{o(avg)} &= 10.42 \text{ A} \end{aligned}$$

C3 Power layer - H-Bridge Inverter



C3.1 Switching component selection

Pre-selection of MOSFETs and IGBTs depended on the following three factors:

8. Maximum possible input voltage
9. Average MOSFET current
10. Availability of components

$$V_{in(220)} = \sqrt{2} \times V_{i(220)}$$

$$V_{in(220)} = \sqrt{2} \times 220 \text{ V}$$

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage

$$V_{in(220)} = 311 \text{ V}$$

Nominal direct input voltage with 220 V line

$$V_{i(220)} = 220 \text{ V}$$

$$I_{Dmax} = P_i / V_{imin(120)}$$

$$I_{Dmax} = 1100 \text{ W} / 120 \text{ V}$$

$$I_{Dmax} = 9.17 \text{ A}$$

Maximum drain current

$$I_{Dmax} = 9.17 \text{ A}$$

Input power

$$P_{imax} = 1100 \text{ W}$$

Minimum possible direct input voltage with 120 V line

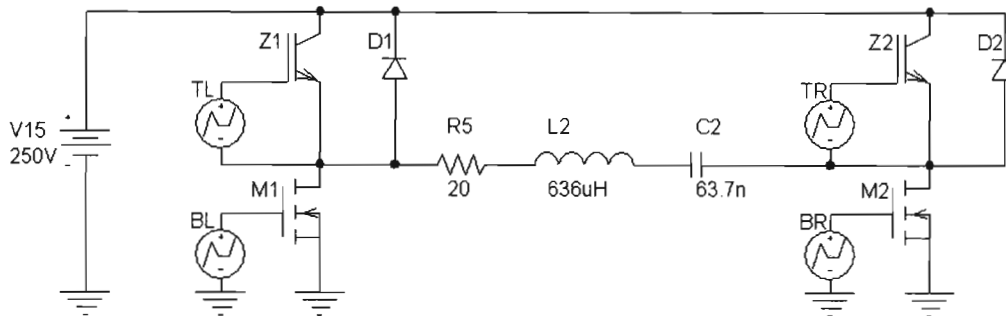
$$V_{imin(220)} = 120 \text{ V}$$

Selected MOSFETs IRFP460, 500V, 20A

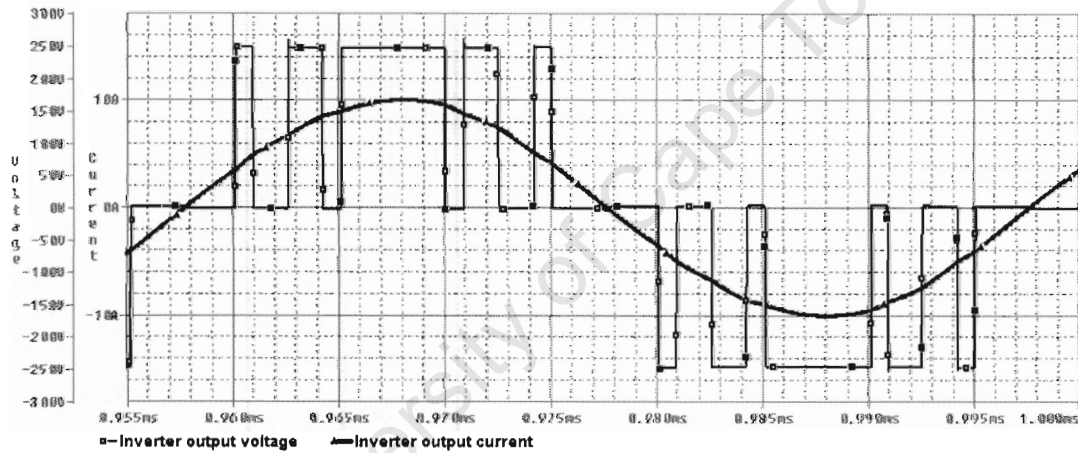
Selected IGBTs IRGP20B60PD, 600V, 20A with ultrafast soft recovery diode

C3.2 Switching component simulations

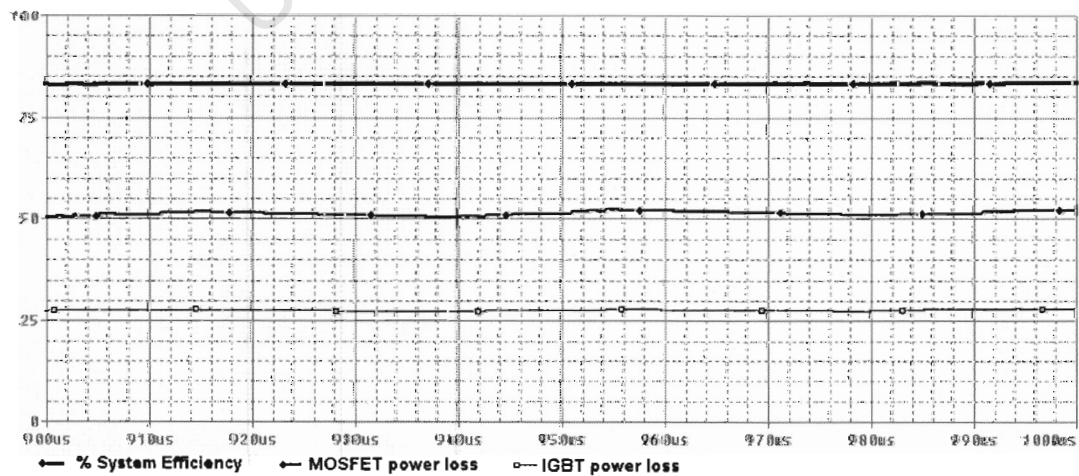
ORCAD schematic



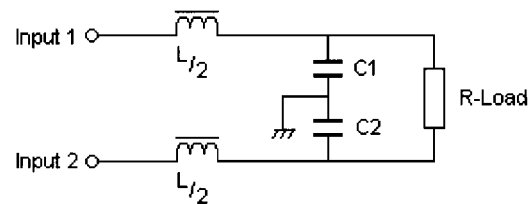
ORCAD results of output voltage and current waveforms



ORCAD results showing individual switch losses and system efficiency



C4 Power layer - Power filter



First, we need to determine the size of output resistance. Where:

$$R_{out} = (V_{RMS})^2 / P_{OUT}$$

$$R_{out} = 110V^2 / 1kW$$

$$R_{out} = 12.1\Omega$$

Next we determine the minimum inductor (L) value assuming that the roll-off frequency (f_c) is at 50kHz. Where:

$$L = R_{Load} / (2 \times \pi \times f_c)$$

$$L = 12.1 / (2 \times 3.14 \times 50000)$$

$$L = 38.52\mu H$$

Now to determine the impedance at the switching frequency of 250 kHz. Where:

$$X_L = 2 \times \pi \times f_{sw} \times L$$

$$X_L = 2 \times 3.14 \times 250 \text{ kHz} \times 38.52\mu H$$

$$X_L = 60.51\Omega$$

From this we can see that the switching frequency impedance is 5 times the load impedance, meaning that no significant power is lost at the switching frequency.

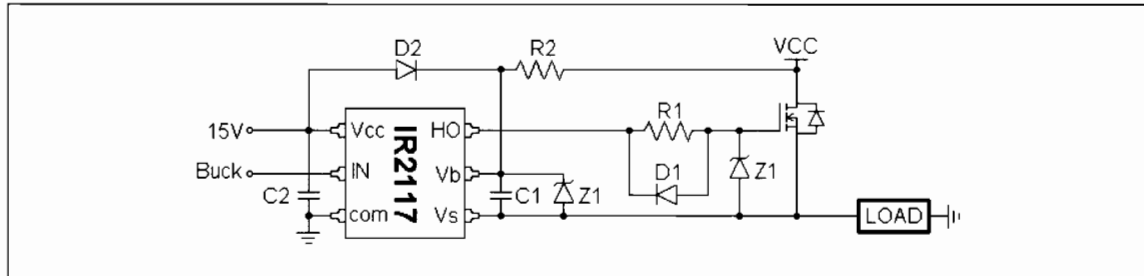
Lastly we need to determine values for C1 and C2 Where:

$$C1 = C2 = (L/2) / (4 \times (R/2)^2 \times \xi^2)$$

$$C1 = C2 = 19.26\mu H / (4 \times (6.05)^2 \times (0.707)^2)$$

$$C1 = C2 = 263.18nF$$

C5 Power interface layer - Buck regulator driver



The design is partially based on the information obtained in the data sheet of the MOSFET driver in use, the IR2117 [35]. Optimization of the design was achieved by the additional information obtained in the International Rectifier application note AN978a [36].

C5.1 Selection of the bootstrap capacitor (C1)

$$C \geq (2(2Q_g + ((I_{qbs(max)})/f) + Q_{ls} + ((I_{C,bs(leak)})/f))) / (V_{cc} - V_f - V_{1,S} - V_{Min})$$

$$C \geq (2(2 \times 120\text{nC} + ((240\mu\text{A})/90\text{kHz}) + 5\text{nC} + ((0)/90\text{kHz}))) / (15\text{V} - 0.5\text{V} - 3\text{V} - 0\text{V})$$

$$C \geq (2(240\text{nC} + 2.67\text{nC} + 5\text{nC} + 0\text{nC})) / (11.5\text{V})$$

$$C \geq 495.34\text{nC} / 11.5\text{V}$$

$$C \geq 43.07\text{nF}$$

Gate charge of high side FET

$$Q_g = 120 \text{ nC}$$

Quiescent current for the high side driver circuitry

$$I_{qbs(max)} = 240 \text{ uA}$$

Frequency of operation

$$f = 90 \text{ kHz}$$

Level shift charge required per cycle

$$Q_{ls} = 5 \text{ nC}$$

Supply voltage

$$V_{cc} = 15 \text{ V}$$

Forward voltage drop across the bootstrap diode

$$V_f = 0.5 \text{ V}$$

Voltage drop across the low side FET or load

$$V_{1,S} = 3 \text{ V}$$

Selected a 100nF, 35V capacitor

Selected C2 as a 10uF, 35V electrolytic capacitor

Selected D1 and D2 as 1N6622

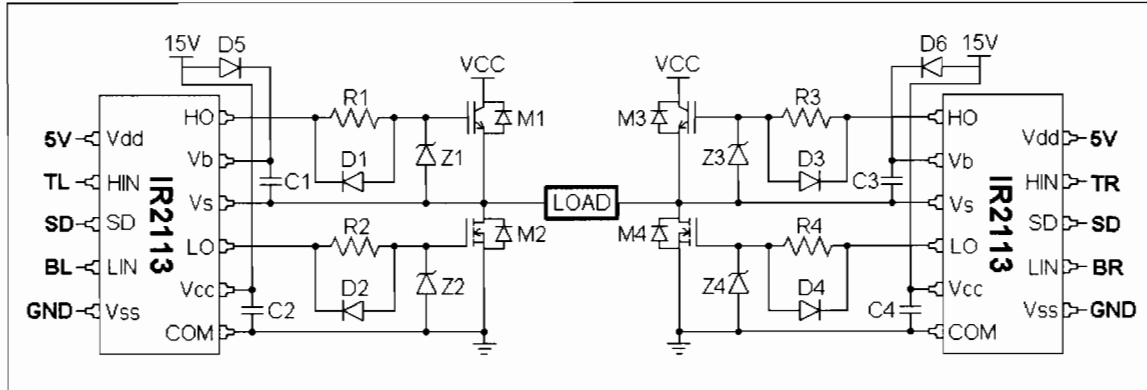
Selected Z1 and Z2 as a 15V, 250mW

R1 was selected at 22Ω, 250mW

The function of R2 is to keep the bootstrap capacitor charged at high switch duty cycle values.

R2 was selected at 220kΩ, 250mW

C6 Power interface layer - H-Bridge driver



The design is based on the information obtained in the data sheet of the MOSFET driver in use, the IR2113 [37].

A 100nF capacitor was selected as bootstrap capacitors: C1, C2, C3 and C4

The 1N6622 diode was selected as discharge diodes D1, D2, D3 and D4

The 1N6622 diode was selected for D5 and D6

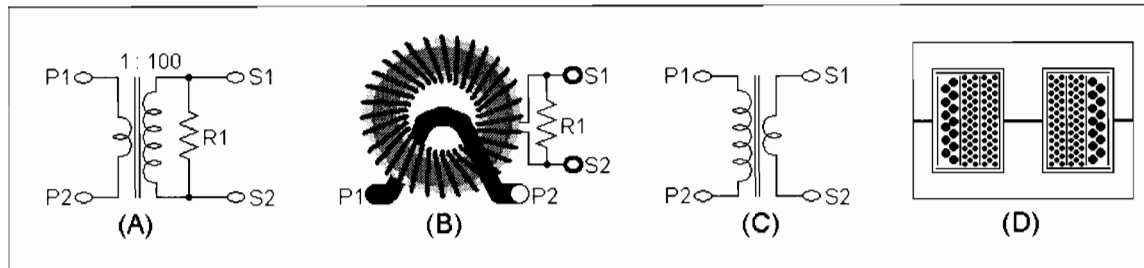
The IRGP20B60PD was selected as IGBTs for M1 and M3

The IRFP460 was selected as MOSFETs for M2 and M4

A 22Ω, 250mW resistor was selected for R1 and R2

A 15V zener was selected for Z1, Z2, Z3 and Z4 to protect the gate of the MOSFETs and IGBTs

C7 Power interface layer - V and I Sensor



C7.1 Current Transformer

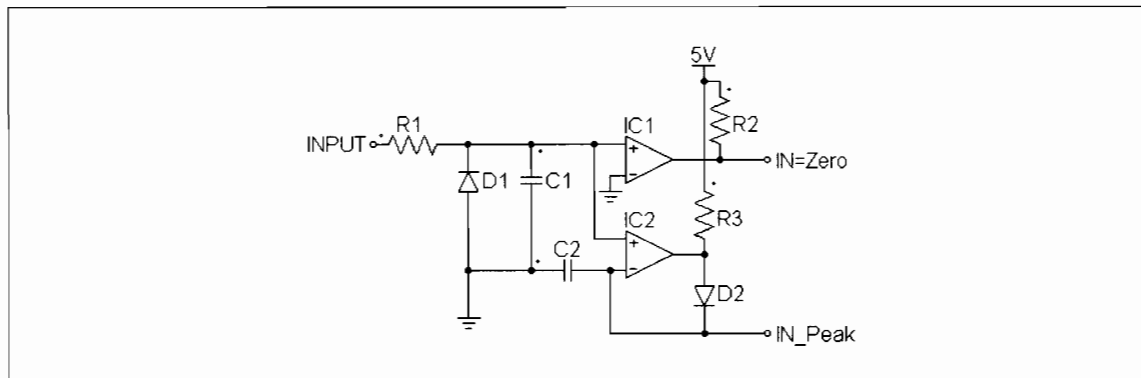
<u>Parameter</u>	<u>Current transformer (CT)</u>
Core type	- TN 20/10/7
Core material	- 3E5
Number of primary turns	- 1 Turns
Parallel primary conductors	- 1
Primary conductor gage	- AWG #25
Number of secondary turns	- 100 Turns
Parallel secondary conductors	- 1
Secondary conductor gage	- AWG #25
Burden resistor	- 100Ω

C7.2 Voltage Transformer

The voltage transformer needs to step 300V peak to 5V peak. The burden on the transformer was selected at 1W. This transformer is used for voltage measurements only and the voltage measurement device has a high input impedance.

<u>Parameter</u>	<u>Voltage transformer (PT)</u>
Core type	- RM8
Core material	- 3C85
Number of primary turns	- 396 Turns
Parallel primary conductors	- 1
Primary conductor gage	- AWG #40
Number of secondary turns	- 9 Turns
Parallel secondary conductors	- 2
Secondary conductor gage	- AWG #36

C8 Signal layer - Voltage and current signal conditioning



C8.1 Zero crossing detector

The comparator used for the zero crossing detector was the LM193 and the design of the zero crossing detector is based of the design found in the datasheet of this device [38].

The capacitor C1 was selected at 1nF

The 1N6622 diode was selected for D1

The input resistor R1 was a 100k Ω , 250mW resistor.

A 1k Ω resistor was selected as a pull-up resistor for R2

C8.2 Peak detector

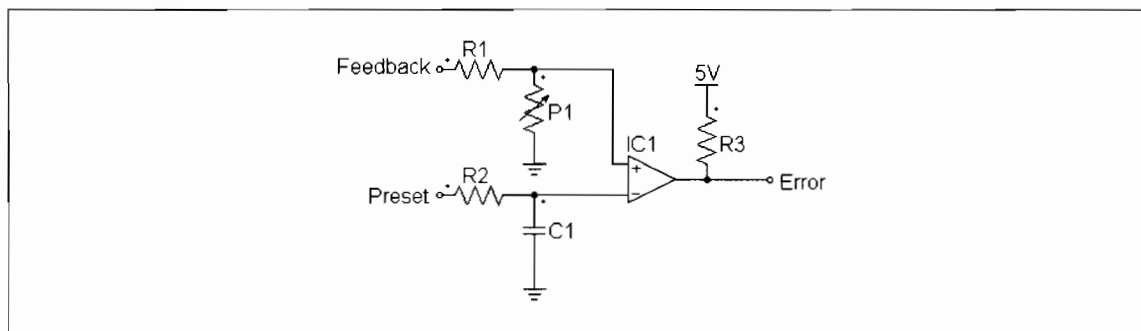
The comparator used for the peak detector was the LM193.

Capacitor C2 was selected at 10nF

The 1N6622 diode was selected for D2

A 3.3k Ω resistor was selected for R3

C9 Signal layer - Voltage Comparator



The design is partially based on the information obtained in the data sheet of the comparator in use, the LM193 [38]. The filter design used to change the PWM signal (at the Preset) from the microcontroller to an analog signal was obtained from Microchip application note AN538 [39].

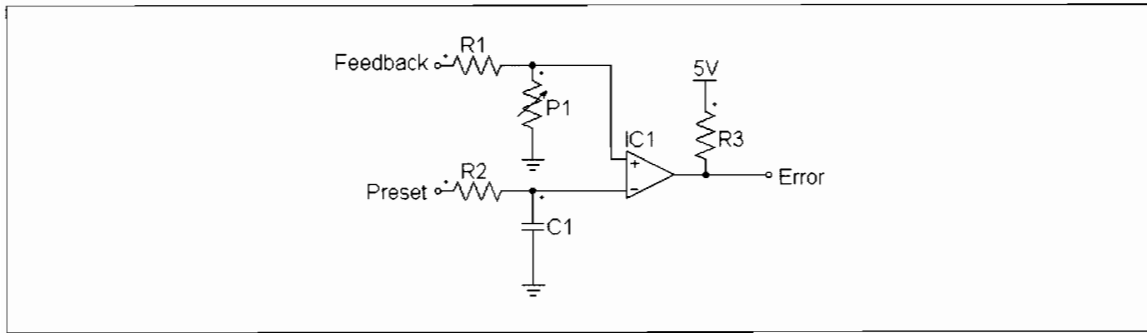
C9.1 R2 and C1 selection

The PWM port of the PIC operates at 10 kHz, this frequency was selected in the microcontroller program.

The -3 dB point was chosen at 1 kHz. From the application note the following formula was obtained: $RC = 1/(2 \times \pi \times f)$. A value for C1 was selected at 0.1 μ F and this resulted in R2 being equal to 1591 Ω , a 1.5 k Ω resistor was selected.

$$R2 = 1.5 \text{ k}\Omega$$

$$C1 = 0.1 \text{ }\mu\text{F}$$



C9.2 R1, R3 and P1 selection

The maximum feedback voltage is equal to the maximum voltage from the Buck regulator.

$$V_{inom(220)} = \sqrt{2} \times V_{i(220)}$$

$$V_{inom(220)} = \sqrt{2} \times 220 \text{ V}$$

$$V_{inom(220)} = 311 \text{ V}$$

Nominal direct input voltage

$$V_{inom(220)} = 311 \text{ V}$$

Nominal direct input voltage with 220 V line

$$V_{i(220)} = 220 \text{ V}$$

The maximum voltage across P1 is equal to the maximum voltage from the Preset, which is equal to 5 V. The remainder of the voltage will be across R1. This results in a maximum voltage across R1 being equal to 306 V. The maximum power dissipated in potentiometer P1 must not exceed 50 mW. The current thru R1 and P1 is determined by the formula: Current = (Power dissipated in P1)/(Voltage across P1). The current is calculated at 10 mA. From this we can determine the values of R1 and P1 by simply dividing the voltage across the resistor by the current thru the resistor. The following components were selected:

$$R1 = 33 \text{ k}\Omega$$

$$P1 = 2 \text{ k}\Omega$$

$$R3 = 1 \text{ k}\Omega$$

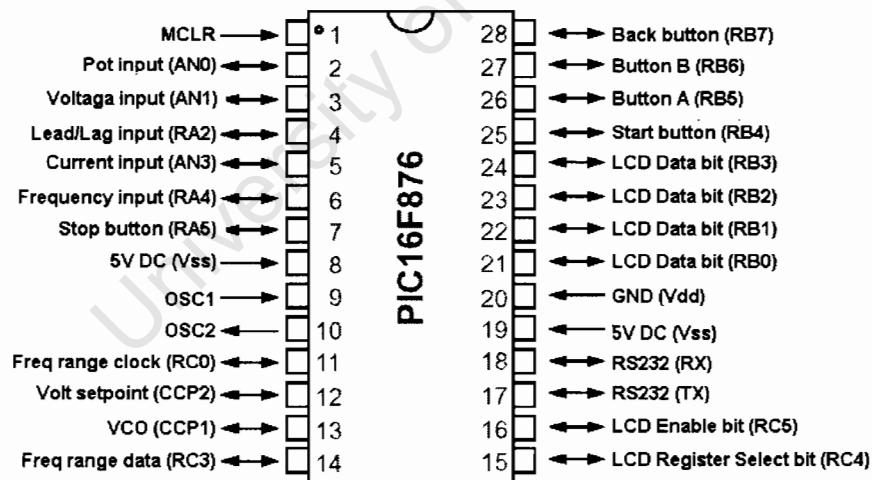
C11 Control layer - Microcontroller

The Microcontroller used in the project was the PIC16F876 [40]. This device was selected on the following criteria:

1. Availability
2. Flash programmable
3. 28 pins required for this project
4. 2 Hardware Pulse width modulation ports
5. Analog ports
6. RS232 capabilities

The pin out of the PIC16F876 can be seen below. The pin functions allocation was based on the following parameters:

1. Manufacturers specifications with regards to pre-assigned pins,
2. PCB layout and
3. PIC Basic requirements



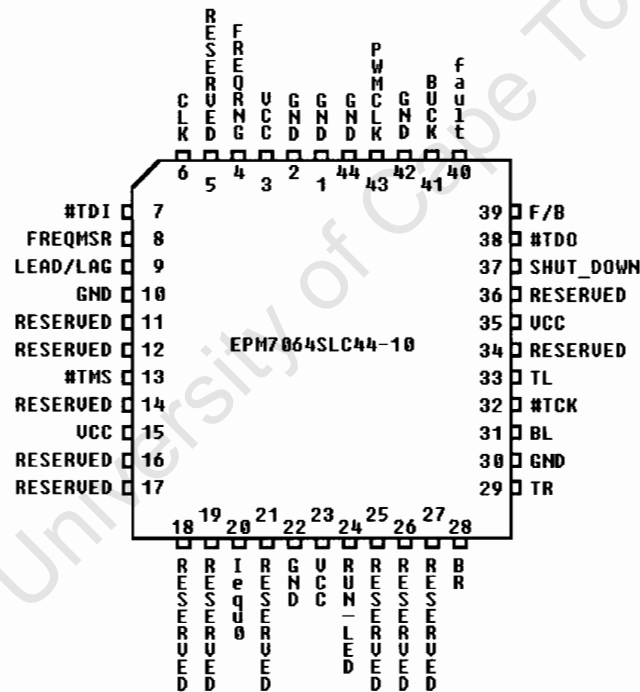
C12 Control layer - FPGA

The FPGA used in the project was the EPM7064SLC44-10 [41]. The criteria for selecting this device were as follows:

4. The project required 51 Logic cells
5. The operation speed is 6 MHz
6. The system voltage is 5 V
7. And availability

Program requirements:

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	LCs	Shareable Expanders	% Utilized
temp6	EPM7064SLC44-10	6	9	0	51	36	79 %



N.C. = No Connect. This pin has no internal connection to the device.

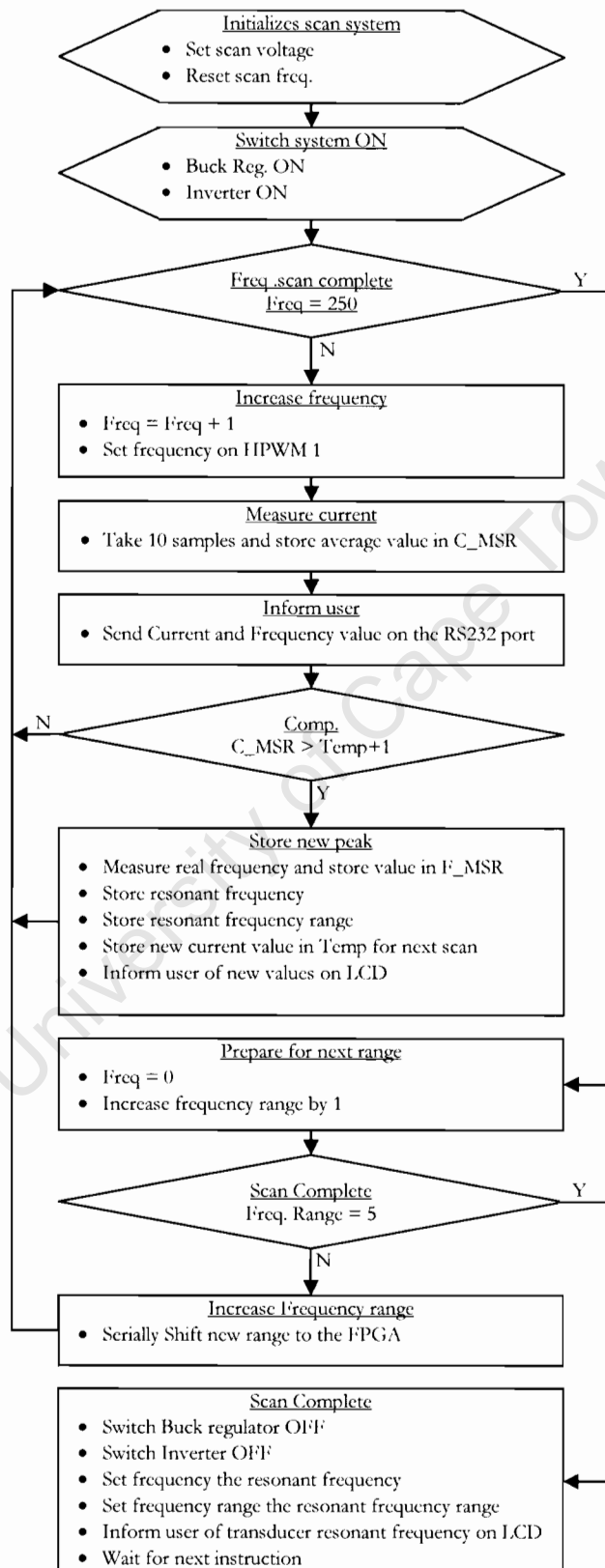
VCC = Dedicated power pin, which MUST be connected to VCC.

GND = Dedicated ground pin or unused dedicated input, which MUST be GND.

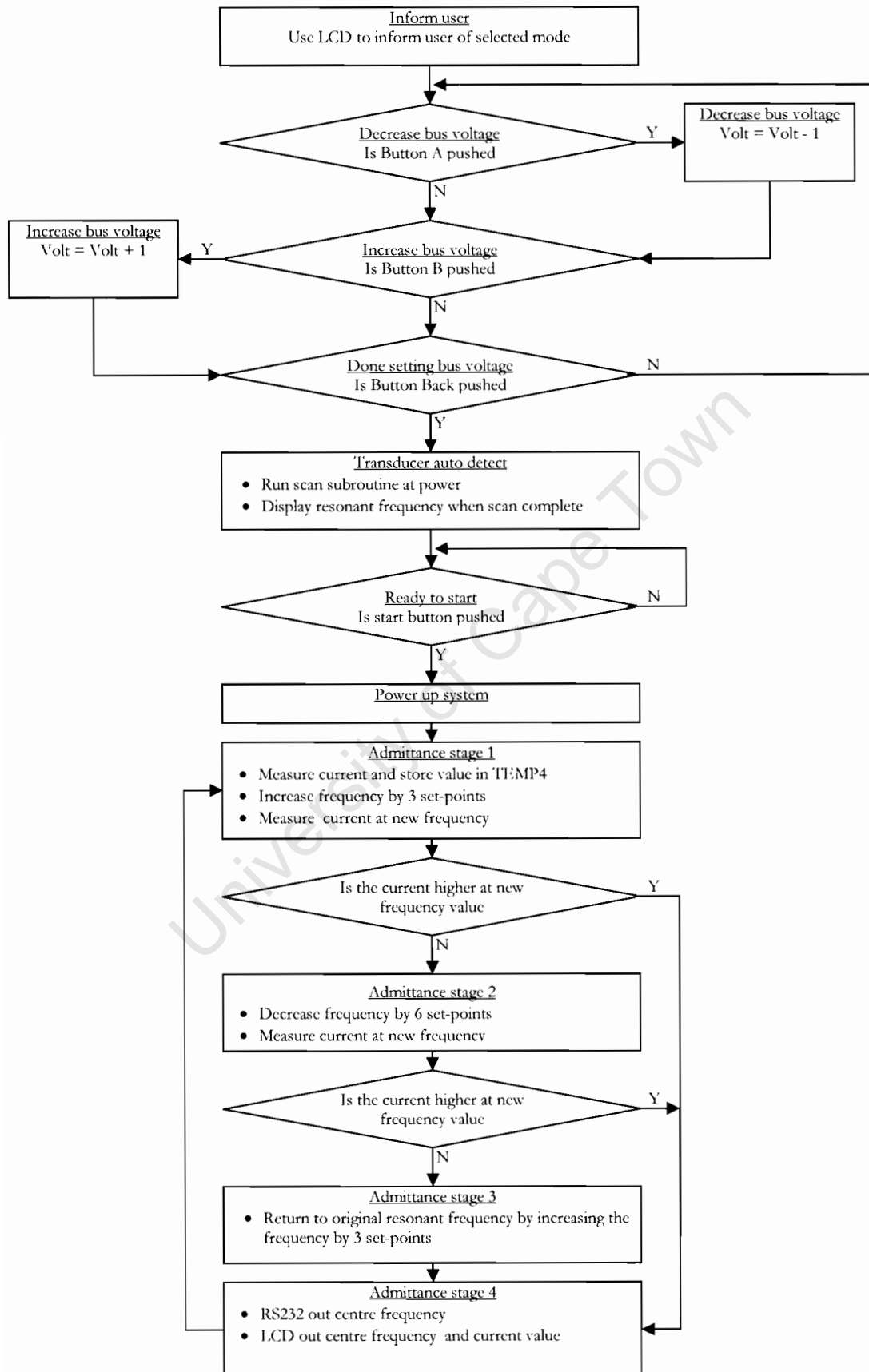
RESERVED = Unused I/O pin, which MUST be left unconnected.

C13 Software layer - Microcontroller program

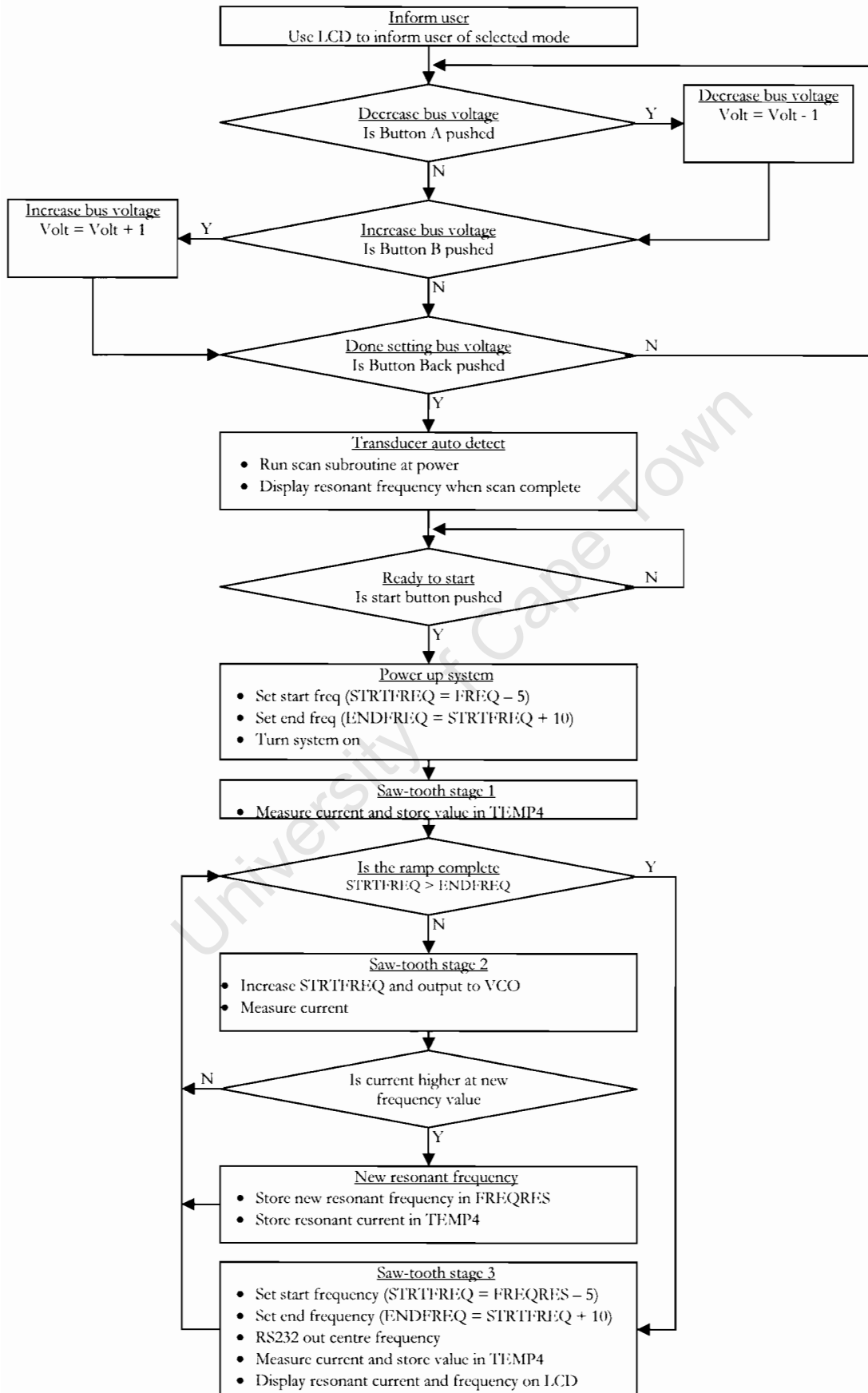
C13.1 Transducer auto detect scan flowchart



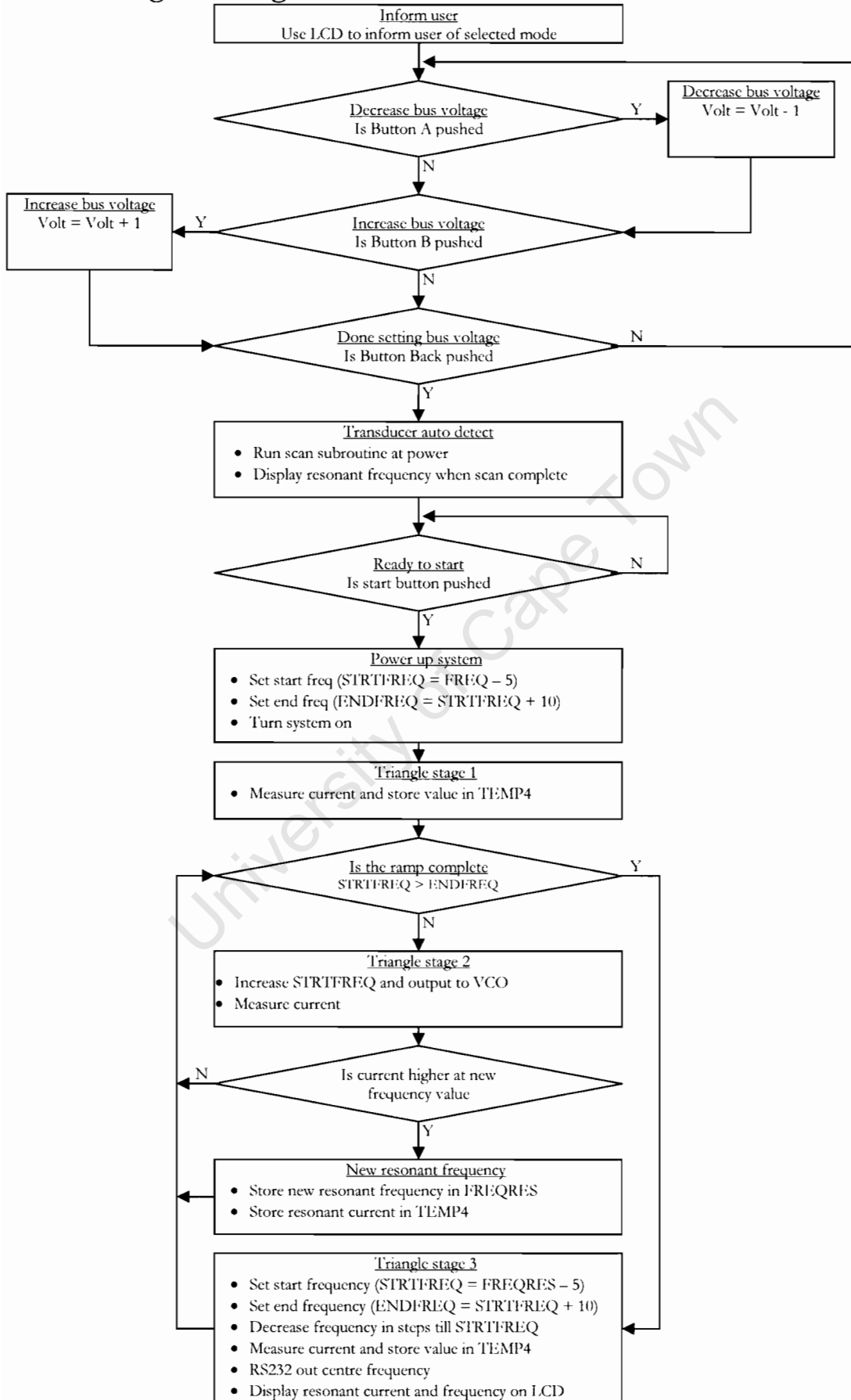
C13.2 Admittance locking flowchart



C13.3 Saw-tooth locking flowchart



C13.4 Triangle locking flowchart



C13.5 Micro program

```

*****
* Name : ClassGD.BAS Author : Jacques Wheeler Date : 9/11/05 *
*****
1. INCLUDE "modedefs.bas"
2. DEFINE LOADER_USED 1 'Bootloader
3. DEFINE ADC_BITS 8 'Set number of bits in result
4. DEFINE ADC_CLOCK 3 'Set clock source (rc = 3)
5. DEFINE ADC_SAMPLEUS 50 'Set sampling time in microseconds
6. DEFINE CCP1_REG PORTC 'HPWM 1 pin port
7. DEFINE CCP1_BIT 2 'HPWM 1 pin bit
8. DEFINE CCP2_REG PORTC 'HPWM 2 pin port
9. DEFINE CCP2_BIT 1 'HPWM 2 pin bit
10. DEFINE LCD_DREG PORTB 'Set LCD Data port
11. DEFINE LCD_DBIT 0 'Set starting Data bit (0 or 4) if 4-bit bus
12. DEFINE LCD_RSREG PORTC 'Set LCD Register Select port
13. DEFINE LCD_RSBIT 4 'Set LCD Register Select bit
14. DEFINE LCD_EREG PORTC 'Set LCD Enable port
15. DEFINE LCD_EBIT 5 'Set LCD Enable bit
16. DEFINE LCD_BITS 4 'Set LCD bus size (4 or 8 bits)
17. DEFINE LCD_LINES 2 'Set number of lines on LCD
18. DEFINE LCD_COMMANDUS 2000 'Set command delay time in us
19. DEFINE LCD_DATAUS 50 'Set data delay time in us
20. DEFINE OSC 20 'Oscillator speed in MHz; 20
21. DEFINE SHIFT_PAUSEUS 100 'Slow the clock by an additional 1s
22. DEFINE HSER_RCSTA 90h 'Set receive register to receiver enabled
23. DEFINE HSER_TXSTA 20h 'Set transmit register to transmitter enabled
24. DEFINE HSER_BAUD 2400 'Set baud rate
25. RNSTP VAR BIT 'Run / stop bit for safety
26. VOLT VAR BYTE 'Voltage set variable (0-250)(1V = 1)
27. FREQ VAR BYTE 'Frequency set variable (0-250)
28. FREQRNG VAR BYTE 'Frequency range set variable (0-3)
29. FREQRES VAR BYTE 'Frequency with highest current (Resonant frequency)
30. FRGRES VAR BYTE 'Frequency range with highest current (Resonant frequency)
31. STRTFREQ VAR BYTE 'Start frequency value
32. ENDFREQ VAR BYTE 'End frequency value
33. FRACT VAR WORD 'Actual measured resonant frequency
34. POWER VAR WORD 'Power set variable (0-1000)
35. MAXPWR VAR WORD 'Maximum Power set variable (0-100)
36. V_MSR VAR WORD 'Voltage read value
37. C_MSR VAR WORD 'Current read value
38. F_MSR VAR WORD 'Frequency read value
39. P_MSR VAR WORD 'Power calculated value
40. TEMP1 VAR WORD 'Temporarily storage space
41. TEMP2 VAR WORD 'Temporarily storage space
42. TEMP3 VAR WORD 'Temporarily storage space
43. TEMP4 VAR WORD 'Temporarily storage space
44. TEMP5 VAR WORD 'Temporarily storage space
45. TEMP6 VAR WORD 'Temporarily storage space
46. LEADLAG VAR PORTA.2 'Phase Lead/Lag bit
47. FREQM VAR PORTA.4 'Frequency measure bit
48. BUTSTOP VAR PORTA.5 'Stop button
49. BUTSTRT VAR PORTB.4 'Start button
50. BUTA VAR PORTB.5 'Button A
51. BUTB VAR PORTB.6 'Button B
52. BUTBACK VAR PORTB.7 'Back button
53. FREQCLK VAR PORTC.0 'Frequency range clock bit
54. FREQDAT VAR PORTC.3 'Frequency range data bit
55. VOLTM CON 1 'Voltage measure bit
56. CURTM CON 3 'Current measure bit
57. HPWMF CON 10000 'HPWM frequency at 10kHz

```

```

58. '===== INITIALISE SYSTEM =====
59. INIT:   'Set port direction
60.         TRISA = %111111 'A5-Stop but;A4-F meas;A3-V meas;A2-L/L meas;A1-I meas,
61.         TRISB = %11110000 'IIIIOOOO
62.         TRISC = %10000000 'TOOOOOOO
63.         ADCON1 = 4 'PortA.0, PortA.1, PortA.3 is analogy, PortA.2 PortA.5 is digital
64.         CLEAR 'Clear all variables and ports
65.         'Initialise FPGA
66.         FREQRNG = 0 'Set frequency range to zero = pwm OFF
67.         HPWM 2,0,HPWMF 'Set zero bus voltage at 2kHz pwm
68.         HPWM 1,125,HPWMF 'Set VCO to centre frequency at 2kHz pwm
69.         SHIFTOUT FREQDAT, FREQCLK, 1,[FREQRNG\3] 'Stop pwm in FPGA
70.         'Inform user of restart
71.         PAUSE 1000 'Delay for 1 second
72.         LCDOUT $FE, 1, "Initializing" 'Clear ,show "Initializing"
73.         PAUSE 200 'Delay for 0.2 second
74.         LCDOUT $FE, $C0, "****"
75.         PAUSE 200 'Delay for 0.2 second
76.         LCDOUT $FE, $C0, "*****"
77.         PAUSE 200 'Delay for 0.2 second
78.         LCDOUT $FE, $C0, "*****"
79.         PAUSE 200 'Delay for 0.2 second
80.         LCDOUT $FE, $C0, "*****"
81.         PAUSE 400 'Delay for 0.4 seconds
82.
83. '===== START-UP MENU =====
84. STARTUP: 'Start-up menu
85.         LCDOUT $FE, 1, " SELECT MODE " 'Clear ,show "SELECT MODE"
86.         LCDOUT $FE, $C0, "MANUAL  AUTO" 'Move cursor to beginning of second line ,show
87. STUP1:   'Button no auto repeat
88.         PAUSE 300 'Delay for 0.3 seconds as de-bounce
89.         IF BUTA = 0 THEN STUP1 'If button A not reset, wait
90.         IF BUTB = 0 THEN STUP1 'If button B not reset, wait
91.         IF BUTBACK = 0 THEN STUP1 'If button BACK not reset, wait
92. STUP2:   'Test buttons
93.         IF BUTA = 0 THEN MANUAL 'If button A is pushed, jump to MANUAL MODE
94.         IF BUTBACK = 0 THEN AUTO 'If BACK button is pushed, jump to AUTO MODE
95.         GOTO STUP2 'Test buttons again
96.
97. '===== MAIN PROGRAM =====
98.
99. '----- MANUAL MODE -----
100. '----- SELECT OPTION - SET CENTER FREQUENCY -----
101. MANUAL: LCDOUT $FE, 1, " SELECT OPTION " 'Clear ,show " SELECT OPTION "
102.         LCDOUT $FE, $C0, " SET CF >>" 'Move cursor to beginning of second line ,show
103. SMAN1:  'Button no auto repeat
104.         PAUSE 300 'Delay for 0.3 seconds as de-bounce
105.         IF BUTA = 0 THEN SMAN1 'If button A not reset, wait
106.         IF BUTB = 0 THEN SMAN1 'If button B not reset, wait
107.         IF BUTBACK = 0 THEN SMAN1 'If button BACK not reset, wait
108. SSMAN1: 'Test buttons
109.         IF BUTB = 0 THEN 'If select button pushed, go to set centre frequency
110.             GOSUB POFF 'Stop power when setting centre frequency
111.             GOSUB SETCF 'Go to set centre frequency
112.             ENDIF
113.         IF BUTBACK = 0 THEN MAN2 'If Forward button is pushed, jump to menu 2
114.         IF BUTSTOP = 0 THEN 'If stop button pushed, then
115.             GOSUB POFF 'Stop power
116.             GOTO MANUAL 'If stopped, redisplay original
117.             ENDIF
118.         GOTO SSMAN1 'Test buttons again

```

```

119.
120. '----- SELECT OPTION - SET VOLTAGE -----
121. MAN2:  LCDOUT $FE, 1, " SELECT OPTION " 'Clear ,show " SELECT OPTION "
122.        LCDOUT $FE, $C0, "<< SET VOLT >>" 'Move cursor to beginning of second line ,show
123. SMAN2:  'Button no auto repeat
124.        PAUSE 300 'Delay for 0.3 seconds as de-bounce
125.        IF BUTA = 0 THEN SMAN2 'If button A not reset, wait
126.        IF BUTB = 0 THEN SMAN2 'If button B not reset, wait
127.        IF BUTBACK = 0 THEN SMAN2 'If button BACK not reset, wait
128. SSMAN2: 'Test buttons
129.        IF BUTA = 0 THEN MANUAL 'If Back button is pushed, jump to menu 1
130.        IF BUTB = 0 THEN 'If select button pushed, go to set voltage
131.            GOSUB SETV 'Go to set SETV
132.            ENDF
133.        IF BUTBACK = 0 THEN MAN3 'If Forward button is pushed, jump to menu 3
134.        IF BUTSTOP = 0 THEN 'If stop button pushed,
135.            GOSUB POFF 'Stop power
136.            GOTO MAN2 'If stopped, redisplay original
137.            ENDF
138.        GOTO SSMAN2 'Test buttons again
139.
140.
141. '----- SELECT OPTION - SET FREQUENCY -----
142. MAN3:  LCDOUT $FE, 1, " SELECT OPTION " 'Clear ,show " SELECT OPTION "
143.        LCDOUT $FE, $C0, "<< SET FREQ >>" 'Move cursor to beginning of second line ,show
144. SMAN3:  'Button no auto repeat
145.        PAUSE 300 'Delay for 0.3 seconds as de-bounce
146.        IF BUTA = 0 THEN SMAN3 'If button A not reset, wait
147.        IF BUTB = 0 THEN SMAN3 'If button B not reset, wait
148.        IF BUTBACK = 0 THEN SMAN3 'If button BACK not reset, wait
149. SSMAN3: 'Test buttons
150.        IF BUTA = 0 THEN MAN2 'If Back button is pushed, jump to menu 2
151.        IF BUTB = 0 THEN 'If select button pushed, go to set frequency
152.            GOSUB SETF 'Go to set SETF
153.            ENDF
154.        IF BUTBACK = 0 THEN MAN4 'If Forward button is pushed, jump to menu 4
155.        IF BUTSTOP = 0 THEN 'If stop button pushed, then
156.            GOSUB POFF 'Stop power
157.            GOTO MAN3 'If stopped, redisplay original
158.            ENDF
159.        GOTO SSMAN3 'Test buttons again
160.
161.
162. '----- SELECT OPTION - SHOW REAL VALUES -----
163. MAN4:  LCDOUT $FE, 1, " SELECT OPTION " 'Clear ,show " SELECT OPTION "
164.        LCDOUT $FE, $C0, "<< SHOW REAL >>" 'Move cursor to beginning of second line ,show
165. SMAN4:  'Button no auto repeat
166.        PAUSE 300 'Delay for 0.3 seconds as de-bounce
167.        IF BUTA = 0 THEN SMAN4 'If button A not reset, wait
168.        IF BUTB = 0 THEN SMAN4 'If button B not reset, wait
169.        IF BUTBACK = 0 THEN SMAN4 'If button BACK not reset, wait
170. SSMAN4: 'Test buttons
171.        IF BUTA = 0 THEN MAN3 'If Back button is pushed, jump to menu 3
172.        IF BUTB = 0 THEN 'If select button pushed, go to show real values
173.            GOSUB SHOWR 'Go to set SHOWR
174.            ENDF
175.        IF BUTBACK = 0 THEN MAN5 'If Forward button is pushed, jump to menu 5
176.        IF BUTSTOP = 0 THEN 'If stop button pushed,
177.            GOSUB POFF 'Stop power
178.            GOTO MAN4 'If stopped, redisplay original
179.            ENDF

```

```

180.          GOTO SSMAN4 "Test buttons again
181.
182. '----- SELECT OPTION - EXIT MANUAL MODE -----
183. MAN5:    LCDOUT $FE, 1, " SELECT OPTION " 'Clear ,show " SELECT OPTION "
184.          LCDOUT $FE, $C0, "<< EXIT MANUAL " 'Move cursor to beginning of second line ,show
185. SMAN5:   'Button no auto repeat
186.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
187.          IF BUTA = 0 THEN SMAN5 'If button A not reset, wait
188.          IF BUTB = 0 THEN SMAN5 'If button B not reset, wait
189.          IF BUTBACK = 0 THEN SMAN5 'If button BACK not reset, wait
190. SSMAN5:  'Test buttons
191.          IF BUTA = 0 THEN MAN4 'If Back button is pushed, jump to menu 4
192.          IF BUTB = 0 THEN 'If select button pushed, exit manual mode
193.          GOSUB POFF 'Stop power when not in preset mode
194.          GOTO STARTUP 'Exit manual mode
195.          ENDIF
196.          IF BUTSTOP = 0 THEN 'If stop button pushed,
197.          GOSUB POFF 'Stop power
198.          GOTO MAN5 'If stopped, redisplay original
199.          ENDIF
200.          GOTO SSMAN5 "Test buttons again
201.
202. '----- SELECT CENTRE FREQUENCY - OFF -----
203. SETCF:   'Set centre frequency
204. CF1:     LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
205.          LCDOUT $FE, $C0, " OFF >>" 'Move cursor to beginning of second line ,show
206. SCF1:    'Button no auto repeat
207.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
208.          IF BUTA = 0 THEN SCF1 'If button A not reset, wait
209.          IF BUTB = 0 THEN SCF1 'If button B not reset, wait
210.          IF BUTBACK = 0 THEN SCF1 'If button BACK not reset, wait
211. SSCF1:   'Test buttons
212.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency OFF
213.          FREQRNG = 0 'Set frequency range to zero
214.          GOTO MANUAL
215.          ENDIF
216.          IF BUTBACK = 0 THEN CF2 'If Forward button is pushed, jump to menu 2
217.          GOTO SSCF1 "Test buttons again
218.
219. '----- SELECT CENTER FREQUENCY - 20kHz -----
220. CF2:     LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
221.          LCDOUT $FE, $C0, "<< 20kHz >>" 'Move cursor to beginning of second line ,show
222. SCF2:    'Button no auto repeat
223.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
224.          IF BUTA = 0 THEN SCF2 'If button A not reset, wait
225.          IF BUTB = 0 THEN SCF2 'If button B not reset, wait
226.          IF BUTBACK = 0 THEN SCF2 'If button BACK not reset, wait
227. SSCF2:   'Test buttons
228.          IF BUTA = 0 THEN CF1 'If Back button is pushed, jump to menu 1
229.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency 20kHz
230.          FREQRNG = 1 'Set frequency range to 20kHz
231.          GOTO MANUAL
232.          ENDIF
233.          IF BUTBACK = 0 THEN CF3 'If Forward button is pushed, jump to menu 3
234.          GOTO SSCF2 "Test buttons again
235.
236. '----- SELECT CENTER FREQUENCY - 25kHz -----
237. CF3:     LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
238.          LCDOUT $FE, $C0, "<< 25kHz >>" 'Move cursor to beginning of second line ,show
239. SCF3:    'Button no auto repeat
240.          PAUSE 300 'Delay for 0.3 seconds as de-bounce

```

```

241.          IF BUTA = 0 THEN SCF3 'If button A not reset, wait
242.          IF BUTB = 0 THEN SCF3 'If button B not reset, wait
243.          IF BUTBACK = 0 THEN SCF3 'If button BACK not reset, wait
244. SSCF3:    'Test buttons
245.          IF BUTA = 0 THEN CF2 'If Back button is pushed, jump to menu 2
246.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency 25kHz
247.             FREQRNG = 2 'Set frequency range to 25kHz
248.             GOTO MANUAL
249.             ENDIF
250.          IF BUTBACK = 0 THEN CF4 'If Forward button is pushed, jump to menu 4
251.          GOTO SSCF3 'Test buttons again
252.
253.
254. '----- SELECT CENTER FREQUENCY - 30kHz -----
255. CF4:      LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
256.          LCDOUT $FE, $C0, "<< 30kHz >>" 'Move cursor to beginning of second line ,show
257. SCF4:    'Button no auto repeat
258.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
259.          IF BUTA = 0 THEN SCF4 'If button A not reset, wait
260.          IF BUTB = 0 THEN SCF4 'If button B not reset, wait
261.          IF BUTBACK = 0 THEN SCF4 'If button BACK not reset, wait
262. SSCF4:    'Test buttons
263.          IF BUTA = 0 THEN CF3 'If Back button is pushed, jump to menu 3
264.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency 30kHz
265.             FREQRNG = 3 'Set frequency range to 30kHz
266.             GOTO MANUAL
267.             ENDIF
268.          IF BUTBACK = 0 THEN CF5 'If Forward button is pushed, jump to menu 5
269.          GOTO SSCF4 'Test buttons again
270.
271.
272. '----- SELECT CENTER FREQUENCY - 35kHz -----
273. CF5:      LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
274.          LCDOUT $FE, $C0, "<< 35kHz >>" 'Move cursor to beginning of second line ,show
275. SCF5:    'Button no auto repeat
276.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
277.          IF BUTA = 0 THEN SCF5 'If button A not reset, wait
278.          IF BUTB = 0 THEN SCF5 'If button B not reset, wait
279.          IF BUTBACK = 0 THEN SCF5 'If button BACK not reset, wait
280. SSCF5:    'Test buttons
281.          IF BUTA = 0 THEN CF4 'If Back button is pushed, jump to menu 4
282.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency 35kHz
283.             FREQRNG = 4 'Set frequency range to 35kHz
284.             GOTO MANUAL
285.             ENDIF
286.          IF BUTBACK = 0 THEN CF6 'If Forward button is pushed, jump to menu 6
287.          GOTO SSCF5 'Test buttons again
288.
289.
290. '----- SELECT CENTER FREQUENCY - 40kHz -----
291. CF6:      LCDOUT $FE, 1, "SELECT CENT FREQ" 'Clear ,show "SELECT CENT FREQ"
292.          LCDOUT $FE, $C0, "<< 40kHz " 'Move cursor to beginning of second line ,show
293. SCF6:    'Button no auto repeat
294.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
295.          IF BUTA = 0 THEN SCF6 'If button A not reset, wait
296.          IF BUTB = 0 THEN SCF6 'If button B not reset, wait
297.          IF BUTBACK = 0 THEN SCF6 'If button BACK not reset, wait
298. SSCF6:    'Test buttons
299.          IF BUTA = 0 THEN CF5 'If Back button is pushed, jump to menu 5
300.          IF BUTB = 0 THEN 'If select button pushed, go to centre frequency 40kHz
301.             FREQRNG = 5 'Set frequency range to 40kHz

```

```

302.          GOTO MANUAL
303.          ENDIF
304.          GOTO SSCF6 'Test buttons again
305.
306. '----- SET VOLTAGE -----
307. SETV:      'Set voltage
308.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
309.          IF BUTB = 0 THEN SETV 'If button B not reset, wait
310.
311. SETV1:     GOSUB CALC_P 'Go to subroutine power measure
312.          PAUSE 100
313.
314.          LCDOUT $FE, 1, "REAL P = ", #P_MSR, "W" 'Clear ,show real power value as measured
315.          LCDOUT $FE, $C0, "DN]", #VOLT, "V]UP BACK" 'Move cursor to second line ,show
316.
317.          IF (BUTA = 0) AND (VOLT > 0) AND (RNSTP = 1) THEN
318.              'If button A is pushed and VOLT is more then 0 and the power is ON then
319.              VOLT = VOLT - 1 'Decrease VOLT by 1
320.              HPWM 2,VOLT,HPWMF 'Set new bus voltage at 2kHz pwm
321.              ENDIF
322.          IF (BUTB = 0) AND (VOLT < 250) AND (RNSTP = 1) THEN
323.              'If button B is pushed and VOLT is less then 250 and the power is ON
324.              VOLT = VOLT + 1 'Increase VOLT by 1
325.              HPWM 2,VOLT,HPWMF 'Set new bus voltage at 2kHz pwm
326.              ENDIF
327.          IF BUTBACK = 0 THEN MAN2
328.          IF BUTSTRT = 0 THEN
329.              GOSUB ONN
330.              ENDIF
331.          IF BUTSTOP = 0 THEN
332.              GOSUB POFF
333.              ENDIF
334.
335.          GOTO SETV1
336.
337. '----- SET FREQUENCY -----
338. SETF:      'Set frequency
339.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
340.          IF BUTB = 0 THEN SETF 'If button B not reset, wait
341.
342. SETF1:     GOSUB MEAS_F 'Go to subroutine frequency measure
343.          PAUSE 100
344.
345.          LCDOUT $FE, 1, "REAL F = ", #F_MSR, "HZ" 'Clear ,show real frequency value
346.          LCDOUT $FE, $C0, "DN[F", #FREQ, "]UP BACK" 'Move cursor to second line ,show
347.
348.          IF (BUTA = 0) AND (FREQ > 0) AND (RNSTP = 1) THEN
349.              'If button A is pushed and FREQ is more then 0 and the power is ON then
350.              FREQ = FREQ - 1 'Decrease frequency by 1
351.              HPWM 1,FREQ,HPWMF 'Set new bus frequency at 2kHz pwm
352.              ENDIF
353.          IF (BUTB = 0) AND (FREQ < 250) AND (RNSTP = 1) THEN
354.              'If button B is pushed and FREQ is less then 250 and the power is ON
355.              FREQ = FREQ + 1 'Increase frequency by 1
356.              HPWM 1,FREQ,HPWMF 'Set new bus frequency at 2kHz pwm
357.              ENDIF
358.          IF BUTBACK = 0 THEN MAN3
359.          IF BUTSTRT = 0 THEN
360.              GOSUB ONN
361.              ENDIF
362.          IF BUTSTOP = 0 THEN

```

```

363.          GOSUB POFF
364.          ENDIF
365.
366.          GOTO SETF1
367.
368. '----- SHOW REAL VALUES - VOLTAGE -----
369. SHOWR:    'Show real values
370.
371. SR1:      'Button no auto repeat
372.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
373.          IF BUTA = 0 THEN SR1 'If button A not reset, wait
374.          IF BUTB = 0 THEN SR1 'If button B not reset, wait
375.
376. SSR1:     V_MSR = TEMP4 / 50 'Average of repetitions
377.          LCDOUT $FE, 1, "V = ", #V_MSR, "V" 'Clear ,show measured voltage
378.          LCDOUT $FE, $C0, ">> BACK" 'Move cursor to beginning of second line ,show
379.
380.          TEMP3 = 50 'Total repetitions
381.          TEMP4 = 0 'Temporary voltage value
382.
383. SSSR1:    GOSUB MEAS_V 'Go to subroutine measure voltage
384.          TEMP4 = TEMP4 + V_MSR
385.
386.          IF BUTB = 0 THEN SR2 'If button pushed, jump to menu 2
387.          IF BUTBACK = 0 THEN MAN4 'If return button is pushed, leave show real
388.          IF BUTSTRT = 0 THEN
389.              GOSUB ONN
390.              ENDIF
391.          IF BUTSTOP = 0 THEN
392.              GOSUB POFF
393.              ENDIF
394.
395.          TEMP3 = TEMP3 - 1
396.          IF TEMP3 = 0 THEN SSR1
397.
398.          GOTO SSSR1 'Test buttons again
399.
400. '----- SHOW REAL VALUES - CURRENT -----
401. SR2:      'Button no auto repeat
402.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
403.          IF BUTA = 0 THEN SR2 'If button A not reset, wait
404.          IF BUTB = 0 THEN SR2 'If button B not reset, wait
405.
406. SSR2:     C_MSR = TEMP4 / 50 'Average of repetitions
407.          LCDOUT $FE, 1, "I = ", #C_MSR, "A" 'Clear ,show measured current
408.          LCDOUT $FE, $C0, "<< >> BACK" 'Move cursor to beginning of second line ,show
409.
410.          TEMP3 = 50 'Total repetitions
411.          TEMP4 = 0 'Temporary current value
412.
413. SSSR2:    GOSUB MEAS_C 'Go to subroutine measure current
414.          TEMP4 = TEMP4 + C_MSR
415.
416.          IF BUTA = 0 THEN SR1 'If button pushed, jump to menu 1
417.          IF BUTB = 0 THEN SR3 'If button pushed, jump to menu 3
418.          IF BUTBACK = 0 THEN MAN4 'If return button is pushed, leave show real
419.          IF BUTSTRT = 0 THEN
420.              GOSUB ONN
421.              ENDIF
422.          IF BUTSTOP = 0 THEN
423.              GOSUB POFF

```

```

424.          ENDIF
425.
426.          TEMP3 = TEMP3 - 1
427.          IF TEMP3 = 0 THEN SSR2
428.
429.          GOTO SSSR2 "Test buttons again"

430. '----- SHOW REAL VALUES - FREQUENCY -----
431. SR3:      'Button no auto repeat
432.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
433.          IF BUTA = 0 THEN SR3 'If button A not reset, wait
434.          IF BUTB = 0 THEN SR3 'If button B not reset, wait
435.
436. SSR3:      GOSUB MEAS_F 'Go to subroutine measure frequency
437.          TEMP3 = F_MSR / 100 'Frequency calculation HPWMF / 100 = 20
438.          TEMP4 = F_MSR // 100 'Frequency calculation HPWMF / 100 = 00
439.          LCDOUT $FE, 1, "f = ", #TEMP3, ".", #TEMP4, "kHz" 'Clear ,show measured frequency
440.          LCDOUT $FE, $C0, "<< >> BACK" 'Move cursor to beginning of second line ,show
441.          IF BUTA = 0 THEN SR2 'If button pushed, jump to menu 2
442.          IF BUTB = 0 THEN SR4 'If button pushed, jump to menu 4
443.          IF BUTBACK = 0 THEN MAN4 'If return button is pushed, leave show real
444.          IF BUTSTRT = 0 THEN
445.              GOSUB ONN
446.              ENDIF
447.          IF BUTSTOP = 0 THEN
448.              GOSUB POFF
449.              ENDIF
450.          GOTO SSR3 "Test buttons again"
451.
452. '----- SHOW REAL VALUES - POWER -----
453. SR4:      'Button no auto repeat
454.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
455.          IF BUTA = 0 THEN SR4 'If button A not reset, wait
456.          IF BUTB = 0 THEN SR4 'If button B not reset, wait
457.
458. SSR4:      P_MSR = TEMP4 / 50 'Average of repetition
459.          LCDOUT $FE, 1, "P = ", #P_MSR, "W" 'Clear ,show measured power
460.          LCDOUT $FE, $C0, "<< BACK" 'Move cursor to beginning of second line ,show
461.          TEMP3 = 50 'Total repetitions
462.          TEMP4 = 0 'Temporary current value
463.
464. SSSR4:     GOSUB CALC_P 'Go to subroutine calculate power
465.          TEMP4 = TEMP4 + P_MSR
466.
467.          IF BUTA = 0 THEN SR3 'If button pushed, jump to menu 3
468.          IF BUTBACK = 0 THEN MAN4 'If return button is pushed, leave show real
469.          IF BUTSTRT = 0 THEN
470.              GOSUB ONN
471.              ENDIF
472.          IF BUTSTOP = 0 THEN
473.              GOSUB POFF
474.              ENDIF
475.          TEMP3 = TEMP3 - 1
476.          IF TEMP3 = 0 THEN SSR4
477.          GOTO SSSR4 "Test buttons again"
478.
479. '----- AUTO MODE -----
480. AUTO:     'inform user of auto mode
481.          LCDOUT $FE, 1, "INT. AUTO MODE" 'Clear ,show
482.          PAUSE 100 'Delay for 0.1 second
483.          LCDOUT $FE, $C0, "****"

```

```

484.          PAUSE 100 'Delay for 0.1 second
485.          LCDOUT $FE, $C0, "*****"
486.          PAUSE 100 'Delay for 0.1 second
487.          LCDOUT $FE, $C0, "*****"
488.          PAUSE 100 'Delay for 0.1 second
489.          LCDOUT $FE, $C0, "*****"
490.          PAUSE 200 'Delay for 0.2 seconds
491. '----- SELECT CONTROL TECHNIQUE -----
492. AUTO1:   'Button no auto repeat
493.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
494.          IF BUTA = 0 THEN AUTO1 'If button A not reset, wait
495.          IF BUTB = 0 THEN AUTO1 'If button B not reset, wait
496.          IF BUTBACK = 0 THEN AUTO1 'If button BACK not reset, wait
497.          LCDOUT $FE, 1, " SELECT CONTROL " 'Clear ,show
498.          LCDOUT $FE, $C0, "ATT TRI SAW"
499.
500. AUTO2:   PAUSE 100 'Delay for 0.1 seconds
501.          IF BUTA = 0 THEN ATT 'If button A go to admittance locking
502.          IF BUTB = 0 THEN TRI 'If button B go to triangle locking
503.          IF BUTBACK = 0 THEN SAW 'If button BACK go to saw-tooth locking
504.          IF BUTSTOP = 0 THEN STARTUP
505.          GOTO AUTO2
506.
507. '----- ADMITTANCE LOCKING MODE -----
508. ATT:     'Button no auto repeat
509.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
510.          IF BUTA = 0 THEN ATT 'If button A not reset, wait
511.          IF BUTB = 0 THEN ATT 'If button B not reset, wait
512.          IF BUTBACK = 0 THEN ATT 'If button BACK not reset, wait
513.          'Inform user of ATT mode
514.          LCDOUT $FE, 1, "INT. ATT MODE" 'Clear ,show
515.          PAUSE 100 'Delay for 0.1 second
516.          LCDOUT $FE, $C0, "****"
517.          PAUSE 100 'Delay for 0.1 second
518.          LCDOUT $FE, $C0, "*****"
519.          PAUSE 100 'Delay for 0.1 second
520.          LCDOUT $FE, $C0, "*****"
521.          PAUSE 100 'Delay for 0.1 second
522.          LCDOUT $FE, $C0, "*****"
523.          PAUSE 200 'Delay for 0.2 seconds
524.
525. ATT1:    LCDOUT $FE, 1, "SET VOLT = ", #VOLT, "V" 'Clear ,show
526.          LCDOUT $FE, $C0, " DN UP NEXT" 'Move cursor to beginning of second line ,show
527.          IF (BUTA = 0) AND (VOLT > 0) THEN 'If button A pushed and VOLT more then 0 then
528.              VOLT = VOLT - 1 'Decrease VOLT by 1
529.          ENDIF
530.          IF (BUTB = 0) AND (VOLT < 250) THEN 'If button B pushed and VOLT less then 250
531.              VOLT = VOLT + 1 'Increase VOLT by 1
532.          ENDIF
533.          IF BUTBACK = 0 THEN ATT2
534.          IF BUTSTOP = 0 THEN AUTO1
535.          PAUSE 200 'Delay for 0.2 second
536.          GOTO ATT1 'Return to loop
537.
538. ATT2:    GOSUB SCAN 'Start scan
539.          TEMP3 = FRACT / 100 'Frequency calculation 2000 / 100 = 20
540.          TEMP4 = FRACT // 100 'Frequency calculation 2000 / 100 = 00
541.          LCDOUT $FE, 1, "Rs f = ", #TEMP3, ".", #TEMP4, "kHz" 'Clear ,show meas frequency
542.          LCDOUT $FE, $C0, "Push start" 'Move cursor to beginning of second line ,show
543.
544. ATT3:    PAUSE 100 'Wait for start

```

```

545.          IF BUTSTRT = 0 THEN ATT4
546.          GOTO ATT3
547.
548. ATT4:    GOSUB ONN 'Turn power on
549.
550. ATT5:    GOSUB MEAS_C 'Measure real current
551.          TEMP4 = C_MSR 'Store current value of current
552.          FREQ = FREQ + 3 'Increase frequency
553.          HPWM 1,FREQ,HPWMF 'Set next frequency
554.          PAUSE 20
555.          GOSUB MEAS_C 'Measure real current
556.          IF C_MSR > (TEMP4 + 5) THEN ATT6 'Test if new frequency is better
557.          FREQ = FREQ - 6 'Decrease frequency
558.          HPWM 1,FREQ,HPWMF 'Set next frequency
559.          PAUSE 20
560.          GOSUB MEAS_C 'Measure real current
561.          IF C_MSR > (TEMP4 + 5) THEN ATT6 'Test if new frequency is better
562.          FREQ = FREQ + 3 'Return to old value
563.          HPWM 1,FREQ,HPWMF 'Set next frequency
564.
565. ATT6:    HSEROUT [DEC C_MSR, 32, DEC FREQ, 13,10]
566.          LCDOUT $FE,1,"I = ",#C_MSR," F = ",#FREQ 'Clear ,show real current
567.          IF BUTSTOP = 0 THEN
568.              GOSUB POFF
569.              GOTO ATT1
570.          ENDIF
571.          PAUSE 50
572.          GOTO ATT5
573.
574. '----- SAWTOOTH LOCKING MODE -----
575. SAW:    'Button no auto repeat
576.          PAUSE 300 'Delay for 0.3 seconds as de-bounce
577.          IF BUTA = 0 THEN SAW 'If button A not reset, wait
578.          IF BUTB = 0 THEN SAW 'If button B not reset, wait
579.          IF BUTBACK = 0 THEN SAW 'If button BACK not reset, wait
580.          'Inform user of SAW mode
581.          LCDOUT $FE, 1, "INT. SAW MODE" 'Clear ,show
582.          PAUSE 100 'Delay for 0.1 second
583.          LCDOUT $FE, $C0, "****"
584.          PAUSE 100 'Delay for 0.1 second
585.          LCDOUT $FE, $C0, "*****"
586.          PAUSE 100 'Delay for 0.1 second
587.          LCDOUT $FE, $C0, "*****"
588.          PAUSE 100 'Delay for 0.1 second
589.          LCDOUT $FE, $C0, "*****"
590.          PAUSE 200 'Delay for 0.1 seconds
591.
592. SAW1:    LCDOUT $FE, 1, "SET VOLT = ", #VOLT, "V" 'Clear ,show
593.          LCDOUT $FE, $C0, " DN UP NEXT" 'Move cursor to beginning of second line ,show
594.          IF (BUTA = 0) AND (VOLT > 0) THEN 'If button A pushed and VOLT more then 0 then
595.              VOLT = VOLT - 1 'Decrease VOLT by 1
596.          ENDIF
597.          IF (BUTB = 0) AND (VOLT < 250) THEN 'If button B pushed and VOLT less then 250
598.              VOLT = VOLT + 1 'Increase VOLT by 1
599.          ENDIF
600.          IF BUTBACK = 0 THEN SAW2
601.          IF BUTSTOP = 0 THEN AUTO1
602.          PAUSE 200 'Delay for 0.2 second
603.          GOTO SAW1 'Return to loop
604.
605. SAW2:    GOSUB SCAN 'Start scan

```

```

606.      TEMP3 = FRACT / 100 'Frequency calculation 2000 / 100 = 20
607.      TEMP4 = FRACT // 100 'Frequency calculation 2000 / 100 = 00
608.      LCDOUT $FE, 1, "Rs f = ", #TEMP3, ".", #TEMP4, "kHz" 'Clear ,show meas frequency
609.      LCDOUT $FE, $C0, "Push start" 'Move cursor to beginning of second line ,show
610.
611.SAW3:  PAUSE 100 'Wait for start
612.      IF BUTSTRT = 0 THEN SAW4
613.      GOTO SAW3
614.
615.SAW4:  STRTFREQ = FREQ - 5 'Set SAW start frequency
616.      ENDFREQ = STRTFREQ + 10 'Set SAW end frequency
617.      HPWM 1,STRTFREQ,HPWMF 'Set start frequency
618.      GOSUB ONN 'Turn power on
619.      PAUSE 100
620.      GOSUB MEAS_C 'Measure real current
621.      TEMP4 = C_MSR 'Store current value of current
622.
623.SAW5:  IF STRTFREQ > ENDFREQ THEN SAW6
624.      STRTFREQ = STRTFREQ + 1
625.      HPWM 1,STRTFREQ,HPWMF 'Set start frequency
626.      GOSUB MEAS_C 'Measure real current
627.      IF C_MSR > (TEMP4 + 5) THEN
628.          FREQRES = STRTFREQ
629.          TEMP4 = C_MSR
630.      ENDIF
631.      GOTO SAW5
632.
633.SAW6:  STRTFREQ = FREQRES - 5 'Set SAW start frequency
634.      ENDFREQ = STRTFREQ + 10 'Set SAW end frequency
635.      HPWM 1,STRTFREQ,HPWMF 'Set start frequency
636.      GOSUB MEAS_C
637.      TEMP4 = C_MSR
638.      HSEROUT [DEC TEMP4, 32, DEC FREQRES, 13,10]
639.      LCDOUT $FE,1,"I = ",#TEMP4," F = ",#FREQRES 'Clear ,show real current
640.      IF BUTSTOP = 0 THEN
641.          GOSUB POFF
642.          GOTO SAW1
643.      ENDIF
644.      GOTO SAW5
645.
646. '----- TRIANGULAR WAVE LOCKING MODE -----
647. TRI:   'Buton no auto repeat
648.      PAUSE 300 'Delay for 0.3 seconds as de-bounce
649.      IF BUTA = 0 THEN TRI 'If button A not reset, wait
650.      IF BUTB = 0 THEN TRI 'If button B not reset, wait
651.      IF BUTBACK = 0 THEN TRI 'If button BACK not reset, wait
652.      'Inform user of TRI mode
653.      LCDOUT $FE, 1, "INT. TRI MODE" 'Clear ,show
654.      PAUSE 100 'Delay for 0.1 second
655.      LCDOUT $FE, $C0, "*****"
656.      PAUSE 100 'Delay for 0.1 second
657.      LCDOUT $FE, $C0, "*****"
658.      PAUSE 100 'Delay for 0.1 second
659.      LCDOUT $FE, $C0, "*****"
660.      PAUSE 100 'Delay for 0.1 second
661.      LCDOUT $FE, $C0, "*****"
662.      PAUSE 200 'Delay for 0.2 seconds
663.
664. TRI1:  LCDOUT $FE, 1, "SET VOLT = ", #VOLT, "V" 'Clear ,show
665.      LCDOUT $FE, $C0, " DN UP NEXT" 'Move cursor to beginning of second line ,show
666.      IF (BUTA = 0) AND (VOLT > 0) THEN 'If button A pushed and VOLT more then 0 then

```

```

667.          VOLT = VOLT - 1 'Decrease VOLT by 1
668.          ENDIF
669.          IF (BUTB = 0) AND (VOLT < 250) THEN 'If button B pushed and VOLT less than 250
670.              VOLT = VOLT + 1 'Increase VOLT by 1
671.          ENDIF
672.          IF BUTBACK = 0 THEN TRI2
673.          IF BUTSTOP = 0 THEN AUTO1
674.          PAUSE 200 'Delay for 0.2 second
675.          GOTO TRI1 'Return to loop
676.
677. TRI2:      GOSUB SCAN 'Start scan
678.              TEMP3 = FRACT / 100 'Frequency calculation 2000 / 100 = 20
679.              TEMP4 = FRACT // 100 'Frequency calculation 2000 / 100 = 00
680.              LCDOUT $FE, 1, "Rs f = ", #TEMP3, ".", #TEMP4, "kHz" 'Clear ,show meas frequency
681.              LCDOUT $FE, $C0, "PUSH START" 'Move cursor to beginning of second line ,show
682.
683. TRI3:      PAUSE 100 'Wait for start
684.              IF BUTSTRT = 0 THEN TRI4
685.              GOTO TRI3
686.
687. TRI4:      STRTFREQ = FREQ - 5 'Set TRI start frequency
688.              ENDFREQ = STRTFREQ + 10 'Set TRI end frequency
689.              HPWM 1,STRTFREQ,HPWMF 'Set start frequency
690.              GOSUB ONN 'Turn power on
691.              PAUSE 100
692.              GOSUB MEAS_C 'Measure real current
693.              TEMP4 = C_MSR 'Store current value of current
694.
695. TRI5:      IF STRTFREQ > ENDFREQ THEN TRI6
696.              STRTFREQ = STRTFREQ + 1
697.              HPWM 1,STRTFREQ,HPWMF 'Set start frequency
698.              GOSUB MEAS_C 'Measure real current
699.              IF C_MSR > (TEMP4 + 5) THEN
700.                  FREQRES = STRTFREQ
701.                  TEMP4 = C_MSR
702.              ENDIF
703.              GOTO TRI5
704.
705. TRI6:      STRTFREQ = FREQ - 5 'Set TRI start frequency
706.              ENDFREQ = STRTFREQ + 10 'Set TRI end frequency
707.
708. TRI7:      IF STRTFREQ > ENDFREQ THEN TRI8
709.              ENDFREQ = ENDFREQ - 1
710.              HPWM 1,ENDFREQ,HPWMF 'Set end frequency
711.              PAUSE 10
712.              GOTO TRI7
713. TRI8:      STRTFREQ = FREQRES - 5 'Set TRI start frequency
714.              ENDFREQ = STRTFREQ + 10 'Set TRI end frequency
715.              HPWM 1,STRTFREQ,HPWMF 'Set start frequency
716.              GOSUB MEAS_C
717.              TEMP4 = C_MSR
718.              HSEROUT [DEC TEMP4, 32, DEC FREQRES, 13,10]
719.              LCDOUT $FE,1,"I = ", #TEMP4," F = ", #FREQRES 'Clear ,show real current
720.              IF BUTSTOP = 0 THEN
721.                  GOSUB POFF
722.                  GOTO TRI1
723.              ENDIF
724.              GOTO TRI5
725.
726. '=====MEASUREMENTS AND CALCULATIONS=====
727. '-----MEASURE VOLTAGE-----

```

```

728. MEAS_V:  'MEAS_V will average the voltage over number of samples defined in TEMP1
729.          TEMP1 = 20 'Number of samples
730.          V_MSR = 0 'Reset measured voltage value
731.
732. MV:      ADCIN VOLTM, TEMP2 'Measure voltage and store in TEMP2
733.          V_MSR = V_MSR + TEMP2 'Add values to be averaged
734.          TEMP1 = TEMP1 - 1
735.          IF TEMP1 > 0 THEN MV 'If not fin resample else complete average
736.          V_MSR = V_MSR / 20 'Average voltage
737.          RETURN
738.
739. '----- MEASURE CURRENT -----
740. MEAS_C:  'MEAS_C will average the current over number of samples defined in TEMP1
741.          TEMP1 = 100 'Number of samples
742.          C_MSR = 0 'Reset measured current value
743.
744. MC:      ADCIN CURTM, TEMP2 'Measure current and store in TEMP2
745.          C_MSR = C_MSR + TEMP2 'Add values to be averaged
746.          TEMP1 = TEMP1 - 1
747.          PAUSEUS 10
748.          IF TEMP1 > 0 THEN MC 'If not fin resample else complete average
749.          C_MSR = C_MSR / 10 'Average voltage
750.          RETURN
751.
752. '----- MEASURE FREQUENCY -----
753. MEAS_F:  'MEAS_F will average the frequency over number of samples defined in TEMP1
754.          COUNT FREQM, 100, F_MSR 'Count pulses on freq bit for 100ms, store in F_MSR
755.          'eg. if pulses is 5000 then frequency is 50.00kHz
756.          RETURN
757.
758. '----- MEASURE POWER -----
759. CALC_P:  GOSUB MEAS_V 'Measure real voltage
760.          GOSUB MEAS_C 'Measure real current
761.          C_MSR = C_MSR / 10
762.          P_MSR = V_MSR * C_MSR 'Calculate power
763.          P_MSR = P_MSR / 20
764.          RETURN
765.
766. '===== OPTIMAL FREQUENCY RANGE DETECT =====
767. SCAN:    'Start scan
768.          LCDOUT $FE, 1, "STARTING SCAN" 'Clear ,show "STARTING SCAN"
769.          'Set initial values
770.          FREQ = 0 'Set low frequency
771.          FREQRNG = 3 'Set first frequency range
772.          GOSUB ONN
773.          TEMP3 = 0
774.
775. SCAN1:   IF FREQ = 250 THEN 'If scan complete then
776.           FREQ = 0 'Reset low frequency
777.           GOTO SCAN2 'Go to set next frequency range
778.           ENDIF
779.           FREQ = FREQ + 1 'If scan not complete increment frequency
780.           HPWM 1,FREQ,HPWMF 'Set next frequency
781.           GOSUB MEAS_C 'Measure new current
782.           HSEROUT [DEC C_MSR,44 , #FREQ, 13,10]
783.           TEMP6 = FREQ * 10
784.           TEMP6 = TEMP6 / 25
785.           LCDOUT $FE,2,"SCANNING ",#TEMP6,"%"
786.           IF C_MSR > (TEMP3 + 1) THEN 'If new high current then
787.           GOSUB MEAS_F 'Measure frequency
788.           FREQRES = FREQ 'Store resonant frequency

```

```

789.          FRGRES = FREQRNG 'Store resonant frequency range
790.          TEMP3 = C_MSR 'Store new high current value for next scan
791.          FRACT = F_MSR 'Store measured resonant frequency
792.          LCDOUT $FE, 1, "SCANNING ",#TEMP6,"% " 'Clear ,show "SCANNING"
793.          LCDOUT $FE, $C0, "RNG", #FRGRES, " fc", #FREQRNG, " I", #TEMP3
794.          ENDIF
795.          GOTO SCAN1 'Start next frequency value
796.
797. SCAN2:    FREQRNG = FREQRNG + 1 'Increment frequency range
798.          IF FREQRNG = 4 THEN 'If scan complete then
799.              FREQ = FREQRNG 'Set frequency the resonant frequency
800.              FRGRES = FREQRNG 'Set frequency range the resonant frequency range
801.              GOSUB POFF 'Stop power
802.              RETURN 'Scan complete
803.          ENDIF
804.          SHIFTOUT FREQDAT, FREQCLK, 1,[FREQRNG\3] 'Set new range in FPGA
805.          GOTO SCAN1 'Start frequency scan in new frequency range
806.
807. '===== SYSTEM POWER =====
808. '----- SWITCH POWER OFF -----
809. POFF:      IF RNSTP = 0 THEN 'If off, no need to switch off
810.              RETURN
811.          ENDIF
812.          HPWM 2,0,HPWMF 'Set zero bus voltage at 2kHz pwm
813.          SHIFTOUT FREQDAT, FREQCLK, 1,[0\3] 'Stop pwm in FPGA
814.          RNSTP = 0
815.          'Inform user of stopping
816.          LCDOUT $FE, 1, "POWER DOWN" 'Clear ,show
817.          PAUSE 100 'Delay for 0.1 second
818.          LCDOUT $FE, $C0, "****"
819.          PAUSE 100 'Delay for 0.1 second
820.          LCDOUT $FE, $C0, "*****"
821.          PAUSE 100 'Delay for 0.1 second
822.          LCDOUT $FE, $C0, "*****"
823.          PAUSE 100 'Delay for 0.1 second
824.          LCDOUT $FE, $C0, "*****"
825.          PAUSE 200 'Delay for 0.1 seconds
826.          RETURN
827.
828. '----- SWITCH POWER ON -----
829. ONN:      IF RNSTP = 1 THEN 'If on, no need to switch on
830.              RETURN
831.          ENDIF
832.          'Inform user of starting
833.          LCDOUT $FE, 1, "POWER UP" ' Clear ,show
834.          PAUSE 100 'Delay for 0.1 second
835.          LCDOUT $FE, $C0, "****"
836.          PAUSE 100 'Delay for 0.1 second
837.          LCDOUT $FE, $C0, "*****"
838.          PAUSE 100 'Delay for 0.1 second
839.          LCDOUT $FE, $C0, "*****"
840.          PAUSE 100 'Delay for 0.1 second
841.          LCDOUT $FE, $C0, "*****"
842.          SHIFTOUT FREQDAT, FREQCLK, 1,[FREQRNG\3] 'Starting pwm in FPGA
843.          RNSTP = 1
844.          TEMP1 = 0
845. ONN1:    IF TEMP1 > VOLT THEN 'Test if set point reached
846.              RETURN
847.          ENDIF
848.          HPWM 2,TEMP1,HPWMF 'Set new bus voltage at 2kHz pwm
849.          TEMP1 = TEMP1 + 1 'Increment TEMP1

```

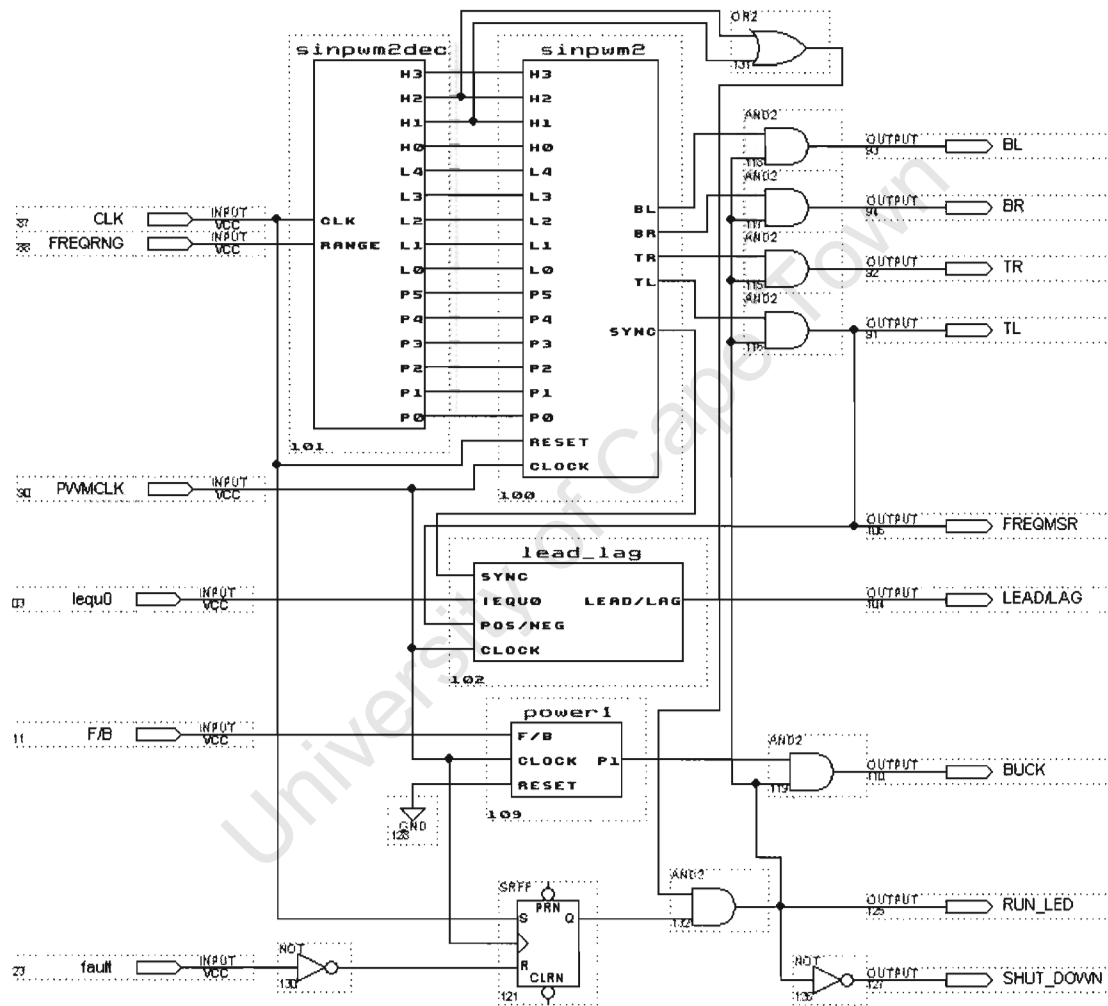
```
850.          GOTO ONN1 'Repeat till voltage resorted'
851.
852. '=====
853. END
```

University of Cape Town

C14 Software layer – FPGA logic program

The main FPGA program has the following control functions:

1. Sinusoidal pulse width modulation with frequency range selection
2. Phase Lead/lag detection
3. Buck regulator control
4. Fault, shutdown mode



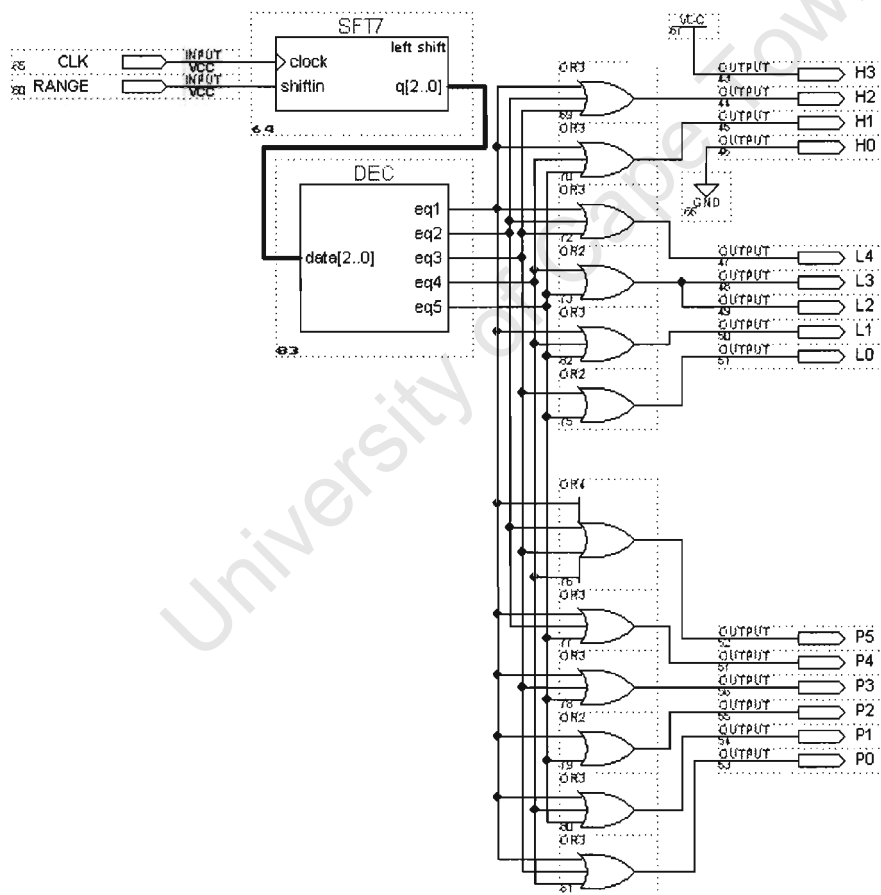
C14.1 Sinpwm2dec

This module decodes a three bit serial value into three parallel values

The three bit serial value will determine the SPWM centre frequency and bandwidth.

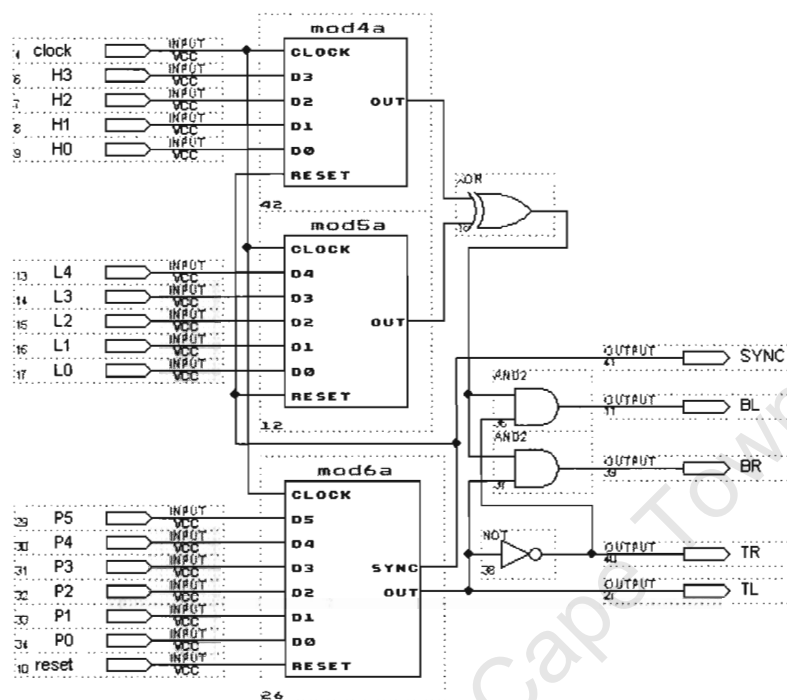
Frequency range			Serial value	Parallel value H	Parallel value L	Parallel value P
Min	Cent.	Max				
OFF	OFF	OFF	000 (0)	1000 (8)	00000 (0)	000000 (0)
16kHz	20kHz	24kHz	001 (1)	1110 (14)	10010 (18)	111111 (63)
21kHz.	26kHz	31kHz	010 (2)	1100 (12)	10000 (16)	110000 (48)
25kHz	31kHz	37kHz	011 (3)	1100 (12)	10001 (17)	101001 (41)
29kHz	36kHz	43kHz	100 (4)	1010 (10)	01110 (14)	100011 (35)
33kHz	42kHz	50kHz	101 (5)	1010 (10)	01111 (15)	011110 (30)

.Below is the circuit as programmed into the FPGA



C14.2 Sinpwm2

This module generates the sinusoidal pulse width modulation signals needed to drive the full bridge inverter.



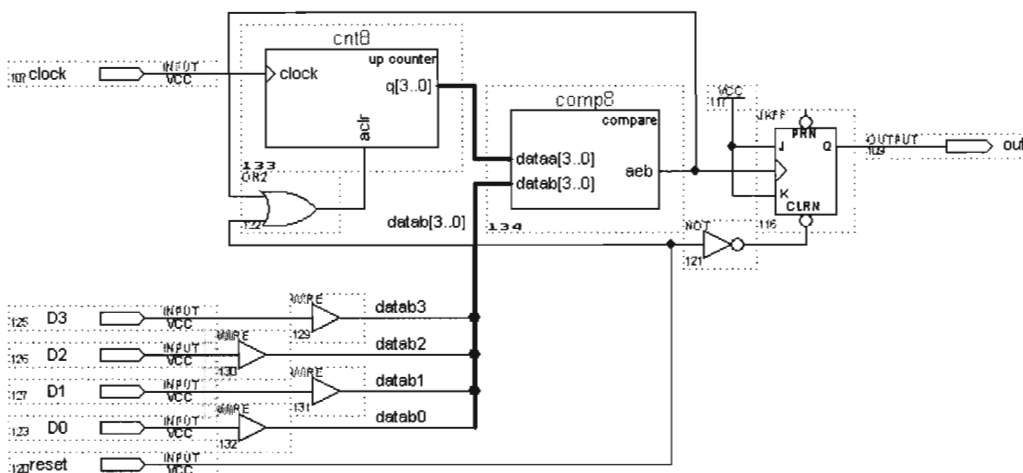
C14.3 Mod4a

The mod4a module is a frequency generator that is controlled by a 4 bit value. The mod5a and mod6a modules are similar to the mod4a module. The only difference is the amount of control bits. The amount of control bits is given by the number after “mod”..

The equation controlling the output frequency is given as:

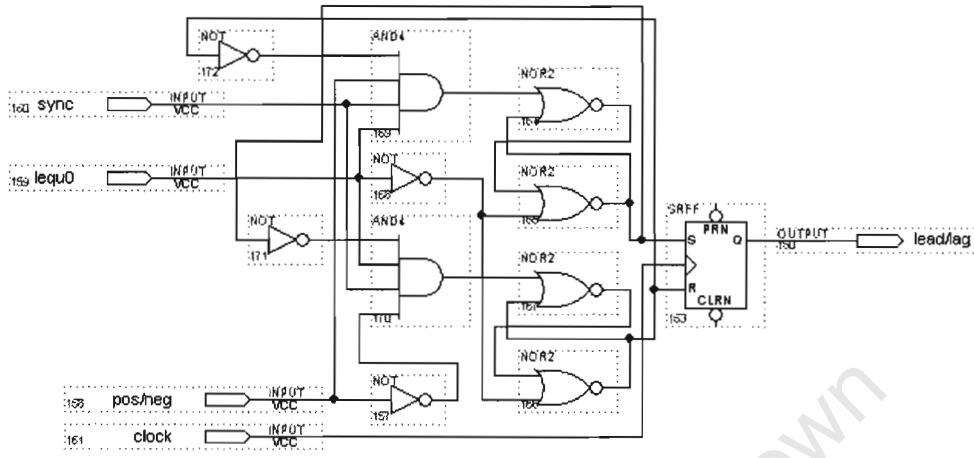
$$\text{Frequency out} = (\text{clock frequency} / (4\text{bit value multiplied by two}))$$

Eg. 250kHz = (5Mhz / (10 x 2))



C14.4 Lead_lag

This module will determine if the transducer current is leading or lagging transducer voltage.



C14.5 Power1

This module is used to drive the Buck regulator. This control technique is a form of Pulse width modulation known as a Bang-bang control. The operation frequency is between 62.5kHz and 93.75kHz.

