A Series-connected VSC for Voltage Regulation, Balancing and Harmonics Mitigation

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DECLARATION

I declare that this thesis, "A Series-connected VSC for Voltage Regulation, Balancing and Harmonics Mitigation" is my own work and has not been submitted to any other university. I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own.

---------- 31st March 2006

Gregory Bathfield

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Professor Timothy Dunne for proof reading the thesis

TERMS OF REFERENCE

This project was proposed by M. Michel Malengret, lecturer at the University of Cape on the 10th February 2005. The project is aimed at designing a device for the detection and mitigation of power quality problems.

The requirements for this thesis project were set by M. Michel Malengret, who also supervised the progress on the project.

The specific instructions were:

1. To review the relevant literature on available mitigation devices with particular emphasis on series-connected devices

2. To review the literature on controllers used to detect and mitigate power quality problems

3. To design a device for mitigation of these power quality problems

4. To develop a control algorithm for the device

5. To test these algorithms in Matlab-Simulink

6. To implement the control algorithm experimentally using the DS1104 Controller card and to test the efficiency of the mitigation device

SYNOPSIS

Introduction

Voltage sensitive electronic equipment, such as computers, process controllers, programmable logic controllers, adjustable speed drives and robotic devices is increasingly used in modern industrial processes. Industrial loads thus require a supply free of voltage disturbances such as voltage dips, swells, unbalances and harmonics. The effect of these disturbances may be as bad as a complete shut down of a production line, hence giving rise to the growing interest and need, for mitigation of such power quality problems. The objective of this thesis is to design and build a mitigation device to shield loads from these problems.

System Description

The schematic of the proposed system is illustrated below.

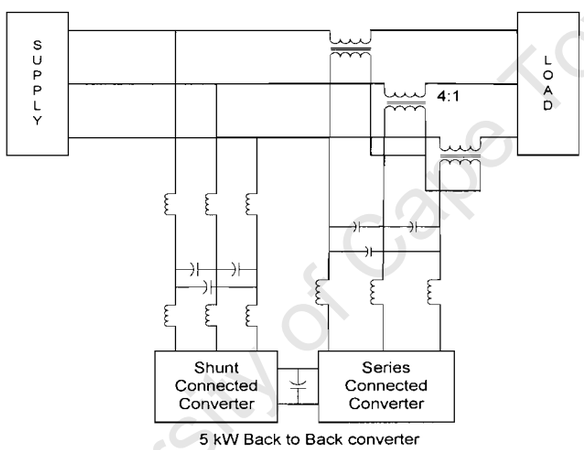

Figure 0-1: Configuration of the system used in this thesis

A back to back converter is to be used. One converter is connected in parallel with the supply and called the shunt converter. The other converter is connected in series with the supply via series transformers and is known as the series connected converter. The shunt converter is controlled to regulate the DC bus voltage shared by both converters. The series connected converter mitigates disturbances by injecting voltages through the series transformers.

Control techniques for both converters

The shunt converter uses a Hysteresis current control technique (HCC) instead of the more efficient Space Vector Pulse Width Modulation (SVPWM) to regulate the DC bus voltage. This choice is due to the limitation of the DS1104 controller board to perform SVPWM switching for exclusively one converter, and is used for the control of the series connected converter. The inputs to the SVPWM algorithm are the stationary frame components U_α and U_β which are the ouputs of the controllers designed to detect and mitigate disturbances. Individual controllers are first developed to detect and mitigate various disturbances separately and then combined to obtain the final algorithm.

The first controller is designed for mitigation of balanced dips and swells. Three phase balanced voltages (consisting solely of a positive sequence) are measured and transformed to a synchronous reference frame where the magnitude of these voltages is obtained as a dc component. This dc component is then used to detect balanced dips or swells. A PI controller is used to track the reference rated voltage. However, in the presence of an unbalance, the negative sequence present causes 100Hz oscillations to appear superimposed on the dc component and the control fails. To deal with unbalanced dips, a second controller is designed to remove the negative sequence from the supply. The supply voltage is decomposed into its positive and negative sequence components. The unbalance is removed using a negative sequence controller and the dip regulated using the positive sequence controller previously designed.

The third controller is used to detect and mitigate low order harmonics. Low order harmonics are detected and isolated from each other in different synchronous frames. Once their phase and magnitude have been measured, the negative of these harmonics can be injected back into the supply to mitigate them.

Finally, the various controllers are combined to obtain the final algorithm, capable of mitigating swells, unbalanced dips and harmonics. The combined effect of the filter and transformers at the output of the series inverter is compensated by adding different gains and phase shifts to the positive and negative sequences as well as to the different harmonics. The schematic of the final algorithm is shown in figure 0.2.

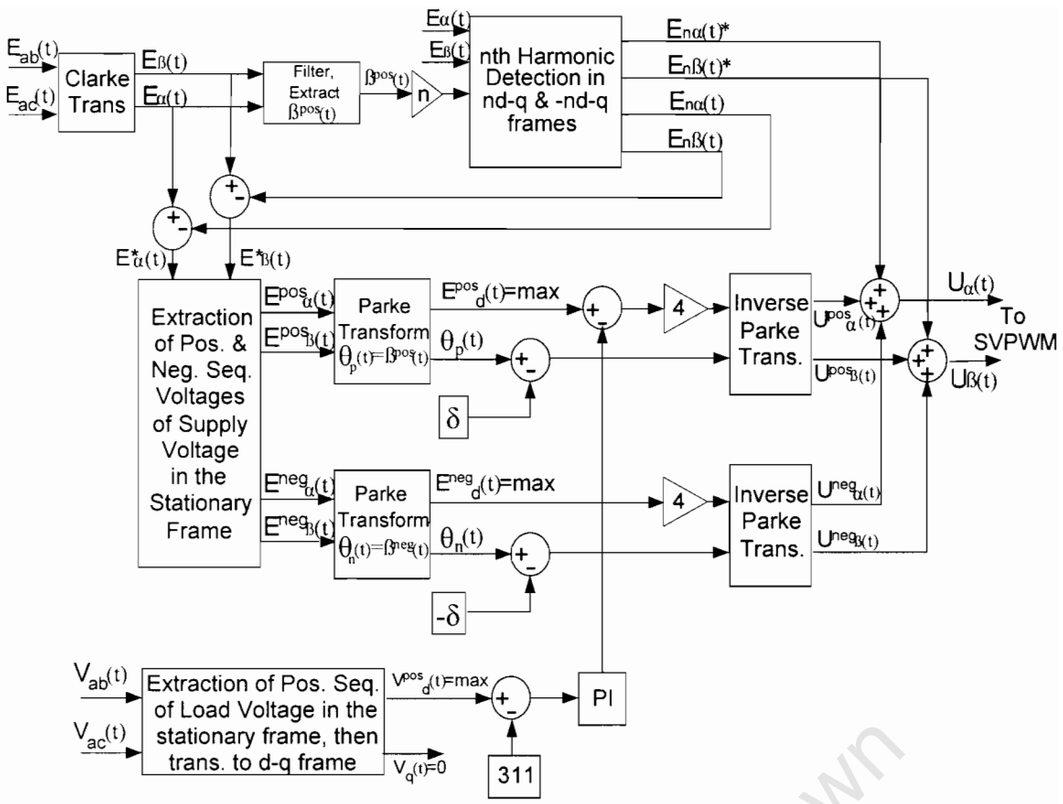

Figure 0-2: Schematic of the final algorithm for mitigation of power quality problems

Testing of the system

All the controllers designed are tested both in simulation and experimentally. The Matlab-Simulink package is used for simulations while the dSPACE ACE Kit is used for real time implementation. Faults are created by placing three variable resistors in line with the supply and switching them on and off using a three phase contractor. Harmonics already present in the UCT supply are used to test the ability of the device to mitigate harmonics.

Conclusions

The prototype successfully mitigates voltage swells, unbalanced dips as well as low order harmonics. The response of the device is slowed down by the presence of filters in the algorithm. The HCC technique is not appropriate when limited to low switching frequencies. The current overshoot generates harmonics in the supply.

Recommendations

Two embedded DSP systems could be used to control the two converters separately. In doing so, the SVPWM control for the DC bus regulation could be implemented to avoid the drawbacks of the HCC method. Furthermore, with a DSP allocated exclusively to the series converter, the DVC algorithm could be implemented for both the positive and negative sequences as well as for the various harmonics to avoid the delays of filters and achieve a completely automated system.

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1. INTRODUCTION

1.1 Overview

The thesis describes the design, modeling and implementation of a back to back converter for voltage regulation and balancing as well as mitigation of low order voltage harmonics in the supply. The system designed in this project supports rather than completely shields the load voltage and thus only needs to be a fraction of the power rating of the load. Both converters share a common DC bus. The first converter is connected in parallel with the supply side and uses a Hysteresis Current Control algorithm (HCC) to regulate the DC bus. The second converter is connected via series injection transformers to the load side. It uses power from the common DC bus and Space Vector Pulse Width Modulation technique (SVPWM) to inject three phase AC voltages of controllable amplitude and phase through the series transformers. Thus, by injecting the correct voltage in each phase, the system can shield critical loads by mitigating disturbances present at the supply side.

1.2 Background and Motivation

Voltage sensitive electronic equipment such as computers, process controllers, programmable logic controllers, adjustable speed drives and robotic devices is increasingly being used in modern industrial processes [1, 2, 3]. As a result, industrial loads need a supply that is free of voltage disturbances while industrial clients are becoming more aware of the losses that results from low power quality [4]. In fact, even voltage dips lasting a few milliseconds can cause production stops with substantial associated costs. These costs include production losses, equipment restarting, damaged or low quality product and reduced customer satisfaction. These costs explain the growing interest and need, for mitigation of power quality problems such as voltage dips, swells and harmonics [4, 5]. The most common disturbances are

voltage dips, voltage unbalance, voltage swells and voltage harmonics. These disturbances are described in the following sections.

1.2.1 Voltage Dips and Voltage Unbalance

Voltage dips are the most serious power quality problem [3, 6]. In [4], a voltage dip is described as a decrease in the rms voltage from 0.1 to 0.9 pu at the power frequency for duration from 0.5 cycles to 1 minute. However, the majority of voltage reductions are typically to about 0.7 pu of a nominal 1.0 pu supply voltage [7]. If all phases decrease by the same magnitude, the dip is said to be a balanced one. If the phases have unequal magnitude during the dip, then the dip is said to be an unbalanced one.

Voltage dips may be caused by faults in power systems or when large induction motors are started, when large loads are switched on [3, 4]. However, the most common cause of voltage dips in industrial plants is a short-circuit fault [5]. Voltage unbalance is a result of the increased number of nonlinear loads [8]. Voltage dips and unbalances have undesirable effects on industrial equipment. For example, ac electric machines supplied with unbalanced voltages produce large negative sequence current components due to low negative sequence impedance. These currents increase machine losses, reduce torque and cause extra temperature rise which is likely to shorten the machine's life [8, 9 ,10].

Figure 1.1 shows the Information Technology Industry Council (ITIC) power acceptability curve. This curve is a modification of the Computer Business Equipment Manufacturers Association (CBEMA) curve and is used to assess whether loss of load is expected during a particular disturbance. The CBEMA curve was initially designed to assess computer vulnerability to power supply disturbances. However, the curve has been applied to adjustable speed drives, fluorescent lighting, general loads, and modern computer and microprocessor loads [11]. The curve illustrates that dips and swells of large magnitude occurring for a very short period are usually tolerable. However, only disturbances of +/- 10% are tolerable for a period exceeding 10s.

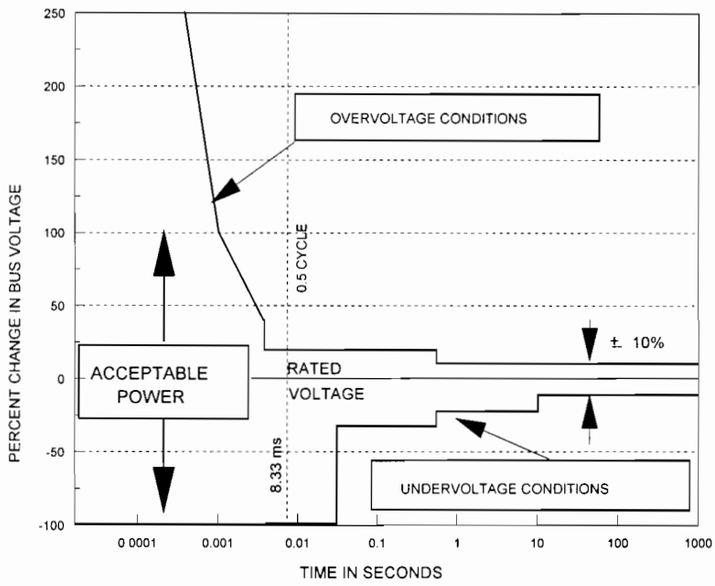

Figure 1-1: The ITIC power acceptability curve [11]

1.2.2 Voltage swells

In [4], a voltage swell is described as an increase in the rms voltage above 1.1 pu at the power frequency for duration from 0.5 cycle to 1 minute. Voltage swells can happen for different reasons. For example, capacitors are often used for power factor correction. If all three phases are over-compensated a three phase over-voltage will occur where all three voltages will be higher than the rated value. This situation usually happens when a plant is shut down but the capacitors are still connected to the system [10]. Voltage swells can cause over-heating, tripping or even damage of industrial equipment such as drives and control relays [4].

1.2.3 Voltage harmonics

Harmonics are caused by power electronic equipment and nonlinear and large single phase loads [8]. Harmonic waveform distortion has become a problem to sensitive loads such as electronic devices as their control often relies either on peak value or

zero crossing of the supplied voltage, both of which are affected by harmonic distortion [4, 12].

1.3 Objectives

The objectives of the thesis are to:

- conduct a thorough literature review of mitigation devices and ways of controlling them to detect and mitigate power quality problems
- design a topology for the mitigation device
- develop a control algorithm that detects disturbances and calculates a three-phase voltage that needs to be injected to correct the supply voltage
- test the control algorithm in Matlab/Simulink
- test the device experimentally on a 10kW resistive load using the DS1104 Controller card

1.5 Plan of Development

The thesis consists of 7 chapters and is outlined as follows:

Chapter 2 focuses on the design of the proposed system for mitigation of disturbances described in chapter1. Switching techniques are suggested for the switching of both series and shunt connected converters.

In chapter 3, different algorithms are discussed for the detection and mitigation of different disturbances. A simple positive sequence controller is first designed to sense and mitigate balanced dips and swells. A second controller is then designed for detection and elimination of negative sequence voltages which are responsible for unbalanced supplies. Together, the two controllers achieve mitigation of balanced and unbalanced dips or swells. A third controller is designed to isolate low order harmonics from each other. Once isolated, the harmonics are measured and mitigated.

Finally, all three controllers are combined to achieve mitigation of swells, balanced and unbalanced dips as well as mitigation of low order harmonics.

Chapter 4 describes the hardware and software. The hardware includes the two converters, driver modules for the IGBTs of the converters, LEM modules for current and voltage measurements and the DS1104 R&D Controller Card and board. The software comprises the Real Time Interface (RTI) and the Control Desk programs from the dSPACE package as well as Matlab-Simulink.

In chapter 5, both simulation and experimental results are presented and compared for the regulation of the DC bus by the shunt converter as well as the mitigation of different disturbances by the series inverter. Conclusions are then drawn in chapter 6 and recommendations made in chapter 7.

1.6 Background Research

1.6.1 Mitigation Devices

The number of devices for mitigation of different power quality problems is immense ranging from traditional equipment to modern power electronic based devices. Some of these devices are presented in the following sections.

1.6.1.1 Motor-Generator Sets [5, 13]

A traditional device used to mitigate voltage dips is the Motor-generator set illustrated in figure 1.2. It consists of a motor, a synchronous generator and a flywheel all connected together. The motor is fed by the supply and the generator feeds the load. In this device, the rotational energy stored in a flywheel provides power to the load during the dip. This device is very efficient but has drawbacks such as its size, noise and maintenance requirements.

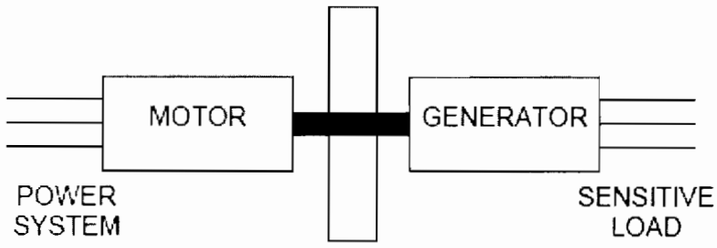

Figure 1-2: Motor-generator set [5]

1.6.1.2 Constant Voltage Transformer (CVT) [5]

A constant voltage or ferro-resonant transformer (CVT) illustrated in figure 1.3, is similar to a 1:1 transformer that has been excited at a high point on its saturation curve and produces an output voltage that is unaffected by variations in the input voltage. The CVT is however only appropriate for low power constant loads.

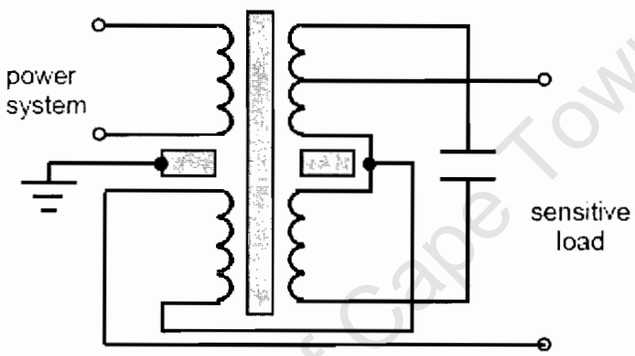

Figure 1-3: Typical circuit for a ferro resonant-transformer [5]

1.6.1.3 Static Voltage Regulator (SVR) [5, 13]

Electronic tap changes mounted on a transformer change the turn ratio to allow regulation of the secondary voltage in steps when dips occur at the primary side. This device is called the static voltage restorer and is illustrated in figure 1.4. The disadvantage of this method is that the thyristor switches it uses can only be switched on once per cycle resulting in time delays of at least half a cycle.

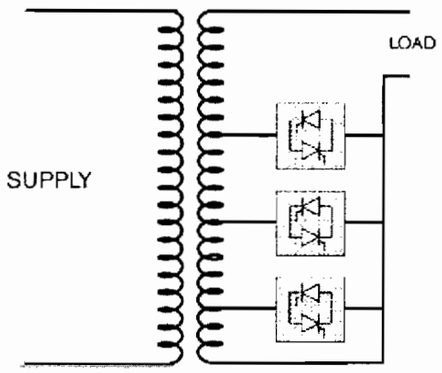

Figure 1-4: SVR [13]

1.6.1.4 Static Transfer Switch (STS) [5, 13, 14]

The STS (figure 1.5) consists of two three phase static switches that allow a fast transfer (less than a quarter of a cycle) of sensitive loads from a primary source that experiences the disturbance, to a secondary source independent of the primary one. The drawback of this device is that load will not be protected if the disturbance affects both sources. Furthermore this solution can not be used if a secondary source is unavailable.

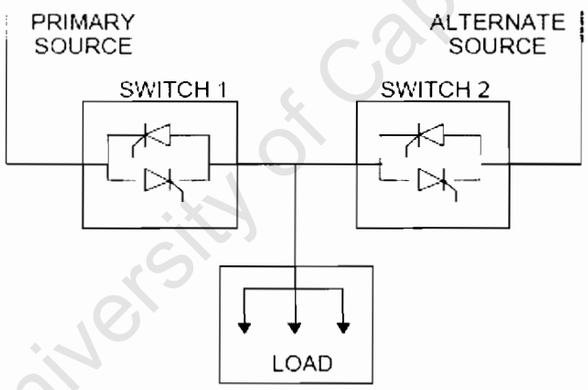

Figure 1-5: Static Transfer Switch [5]

1.6.1.5 Uninterruptible Power Supply (UPS) [5, 13]

The UPS consists of a diode rectifier followed by an inverter as indicated by figure 1.6. Energy is stored in batteries and is used to maintain the DC bus that supplies the inverter during a dip or an interruption. This solution is suitable for low power

equipment. However, for bigger loads, the costs associated with conversion losses and maintenance of batteries renders the UPS not such a viable solution.

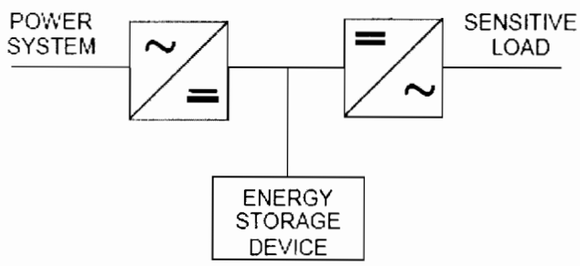

Figure 1-6: Uninterruptible power supply [5]

1.6.1.6 Static Series Compensator (SSC) [5, 13]

The SSC (figure 1.7), commercially known as the Dynamic Voltage Restorer (DVR) is a voltage source controller (VSC) connected in series with the supply voltage by means of a series connected injection transformer. The device injects a voltage of controllable magnitude and phase to obtain the desired load voltage and can thus be used to mitigate voltage swells, dips and harmonics. The real power transferred by the VSC is obtained from an energy storage device. The size and cost of that energy storage device has a large impact of the compensation ability of the SSC and represents the greatest limitation of that device. The inverter consisting of IGBTs can perform perfect compensation in less than half a cycle.

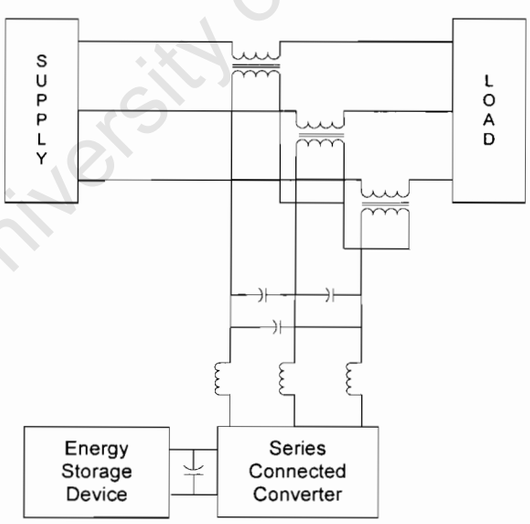

Figure 1-7: Scheme of series compensator for voltage dip mitigation

1.6.1.7 Static Synchronous Compensator (STATCOM) [15, 16]

The STATCOM (figure 1.8) is a VSC connected to the supply via a shunt connected converter as compared to the VSC which is connected in series to the supply. By varying the amplitude of the voltage produced by the VSC, flow of reactive power between the supply and the converter is achieved. Flow of real power is achieved by changing the phase angle between the converter voltage and the output voltage. The STATCOM can thus be used for power factor correction. It can also be used for unbalance compensation as presented in [34].

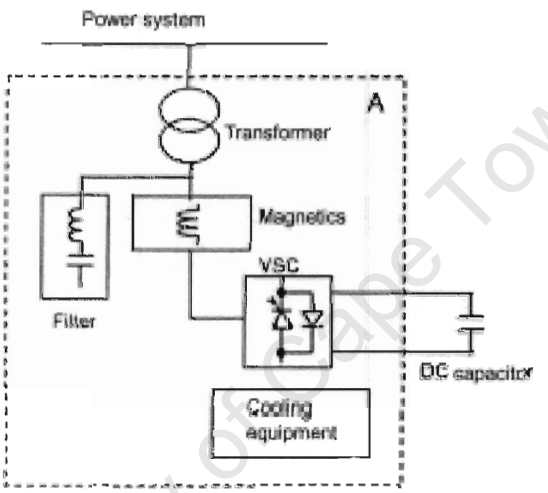

Figure 1-8: STATCOM Configuration [15]

1.6.1.8 The UPFC and the UPQC

The UPQC (Unified Power Qualitty Controller) is a modification of the Unified Power Flow Controller (UPFC) [18] and is considered to be one of the most powerful solutions to large sensitive loads [21]. Both the UPFC and the UPQC consist of two converters, one connected in parallel with the line and one in series, and can be regarded as a combination of a STATCOM and a VSC as illustrated in figure 1.9. This configuration provides an alternative to the limitation of an energy storage device of the SSC as the parallel converter provides the active power required by the series converter. The UPFC instantaneously controls active and reactive power flow in the transmission line while maintaining a fixed voltage at the point of compensation [19, 20, 22]. The UPQC benefits from the capabilities of both the STATCOM and the SSC and can thus mitigate sags, swells, voltage imbalance, flicker, harmonics, and reactive currents [18]. It can also perform power factor

correction [19]. Its main disadvantage is the complexity of the control required due to the number of solid-state devices used [17].

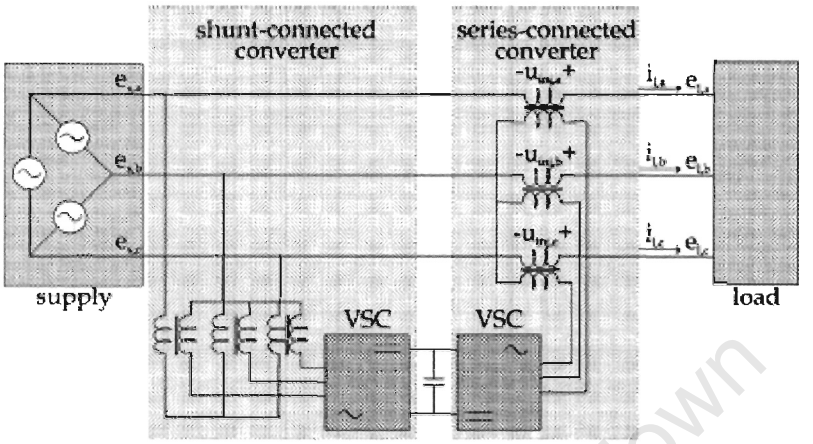

Figure 1-9: Scheme of the unified power quality conditioner (UPQC) [13]

1.6.2 Control Strategies for Mitigation Devices

It is evident that the configuration scheme of both the UPFC and UPQC makes them the most versatile and complex power electronic equipment that have been developed for power quality improvement [20]. In this section, control strategies proposed in the literature for both the shunt and the series converter are discussed

1.6.2.1 DC Bus Voltage Regulation

The shunt converter can perform power factor correction as described in 1.6.1.8. However, when used for that purpose, DC bus voltage oscillations occur. These oscillations affect the performance of the series converter and as a result, a complex control technique is now required for that converter [18]. Thus, the shunt controller implemented in this thesis is solely designed for DC bus regulation to provide active power to the series converter, thus simplifying the control.

In [23] different control strategies are studied for the regulation of a DC bus in a grid connected converter. All these strategies achieve bi-directional power flow at unity power factor to control the DC bus. The three control techniques are Hysteresis Current Control (HCC), Voltage Oriented Control (VOC) and Direct Power Control – Space Vector Modulation (DPC-SVM). The HCC algorithm is the simplest one to

implement [hysteresis] and involves only one PI controller compared to the three that both other techniques require. The results of this thesis indicate that VOC and DPC-SVM, which use the more efficient Space Vector Pulse Width Modulation (SVPWM), are preferred to HCC although the latter offers a slightly faster response. HCC has the disadvantage of a varying frequency which generates continuous harmonics spectrum [13]. It also requires fast sampling frequencies to avoid current overshoots in the hysteresis currents [24]. However, only one converter can be controlled using SVPWM by the DS1104 Controller card and this switching technique is implemented for the series converter. Thus, the Hysteresis Current Control is used for the shunt converter.

1.6.2.2 Detection and Mitigation of Dips

The series inverter is the most important component of the device and mitigates power quality problems. In this thesis, mitigation of voltage swells, unbalanced dips and voltage harmonics is performed. Different control techniques have been reported in literature for the detection and mitigation of these disturbances and are discussed in this section.

The detection of a power quality problem can only be detected by measurements of the supply voltage and/or currents. Conventional methods related to phasors proposed in [25] involve calculation of rms values of voltages which degrades the performance during transients. In this thesis, a technique based on the synchronous d-q frame is used. Line to line voltages are measured and transformed to the stationary frame. Then, the stationary frame components are transformed to the d-q synchronous frame using an angle θ. By carefully choosing that angle, the supply voltage can be represented as dc components which are easier to control. However, if the supply voltage is unbalanced, the supply voltage will not be represented as pure dc components any longer, due to the presence of a negative sequence [26].

To tackle this difficulty, [26-30] propose the concept of two rotating coordinate frames to extract the positive and negative sequence components of the supply voltage using angle θ. The author uses a phase lock loop which is slow and degrades the response during transients [30]. In this thesis, the grid voltages are sampled continuously and θ is calculated instantaneously from these voltages. Thus, the delays

associated with the phase lock loop are eliminated resulting in a superior dynamic response. The instantaneous positive and negative sequence components are extracted using a set of equations derived in [31]. The same equations are used in [26-30]. The unbalanced system can be balanced by removing the negative sequence, and regulated by controlling the amplitude of the positive sequence voltage [9, 26-30]. This technique is implemented in section 3.2 of this thesis.

The presence of a low pass filter and of three single phase transformers affects the performance of the device by causing a voltage drop as well as a phase shift to the voltage supplied by the converter [26-28, 30]. In [26-28, 30] the author uses a filter compensation matrix which performs a back calculation of the filter input voltage to compensate for the filter effect. This method necessitates three additional current measurements. However, the author assumes that the transformer is ideal and thus does not compensate for its effect. Furthermore, this method has been found to offer poor transient performance and is sensitive to variations in filter parameters [6, 32, 33].

To overcome the drawbacks of this algorithm, a Double Vector Algorithm (DVC) is presented in [32]. This algorithm is executed in the d-q synchronous frame where the supply voltage is represented by dc components. Thus, a PI controller is used to track the reference voltage. The algorithm uses two vector-control loops to track the reference of the injected voltage which includes compensation for the voltage drop across the filter. The outer voltage loop controls the capacitor voltage by calculating a reference for the inductor current. This current reference is used by the inner current loop to estimate the converter voltage. This algorithm shows an improved transient response compared to the one presented in [26-28, 30] but is also based on the assumption of an ideal injection transformer. In [12], the DVC algorithm is altered to accommodate the presence of a real transformer. The leakage inductance of the transformers adds up to the filter present between the converter and the grid, creating an L-C-L filter and not just an L-C filter as assumed up to now. [12] proposes the addition of a third control loop and the calculation of the voltage drop on the windings of the transformer that must be added to the reference voltage before it is injected.

The two DVC methods discussed above are designed for purely balanced systems. In the case of an unbalanced system, the presence of oscillations in the dc components obtained in the d-q synchronous frame causes the method to fail [6, 33]. Thus, [6, 33] propose a Modified Double Vector Control (MDVC) where the positive and negative sequence are extracted from the supply voltage as in [26-30] using the equations derived in [31]. They are then transformed into two synchronous frames rotating in opposite directions. In their respective frames, both sequences appear as dc components and two DVC algorithms are used to control the two sequences separately.

Both the DVC [32] and MDVC [6, 33] have a few drawbacks. They both require 12 measurements:

- The three supply voltages
- The voltages across the three capacitors
- The three supply currents
- The three inductor currents

The MDVC algorithm is not implemented in this thesis due to the number of measurements required. The DS1104 Controller card is limited to 8 ADC channels only. A simpler approach to filter compensation is presented in chapter three of this thesis.

Furthermore, both the DVC and the MDVC are designed for supplies free of harmonics. In the presence of harmonics, oscillations of higher frequencies than in the case of an unbalance appear in the dc components of the d-q synchronous frame, causing both algorithms to fail. Thus, the PI controller used in the DVC fails to track its reference. A possible solution to that problem is proposed in [4, 12] where a moving average filter is used to remove the oscillations due to harmonics. The drawback of this method is a delay of half a cycle due to the filter. Thus, the response of the device will lag by 0.01s.

In [28, 30] a better solution is suggested to achieve a faster response of the device to a dip. The oscillations present in the d-q frame due to the presence of harmonics can be removed by measuring the harmonics and subtracting them from the measured signals to obtain their fundamental component. This subtraction is performed in the α-β stationary frame and avoids the need for the moving average filter. However, this method depends on accurate measurements of the harmonics which will be discussed shortly. This technique is used to extract the fundamental of the supply voltage in this project.

1.6.2.3 Detection and Mitigation of Harmonics

Techniques for harmonic mitigation have been researched and developed for a long time. Passive filters were traditionally used to mitigate harmonics. However, these filters have some disadvantages such as a slow response, dependence on the system impedance and inability to adjust to load variations [12, 13]. Hence, active filters have been proposed instead [2, 12, 28, 30].

Different algorithms have been developed for detecting and measuring harmonics. In [34], three different techniques are compared. The first one is a direct active filtering method (D-Method) performed in the d-q synchronous frame. The oscillations due to the harmonics in the d-q frame are removed by using low pass filters and the filtered signal is subtracted from the unfiltered one. The result is the d-q components of all the harmonics present in the supply. The drawback of this method is a delay of 25ms as well as a phase shift caused by the filters. The second method described as the F-Method in [34] uses a moving Fourier series to detect the harmonics. This method has a better response time 10ms but is complex. The last method called the T-method uses low pass filters to extract the magnitude of various harmonics in separate rotating frames. It has the same drawbacks as the D-Method but achieves the detection of the harmonics separately.

In [4, 12], resonant filters are used to isolate different harmonics. The filter is designed to have a low gain for all frequencies except for the one being isolated. The filter is also designed to introduce no phase shift to the measured harmonic. In [28, 30], a more accurate algorithm is developed to isolate the harmonics in different synchronous frames, where the harmonic appears as dc and all other harmonics

appear as oscillations. It is similar to the T-method presented in [34] but is a much faster and more accurate algorithm. By averaging over half a cycle of the system frequency, the harmonics appearing as oscillations are cancelled and the dc component isolated. Thus, the exact magnitude and phase of that harmonic is obtained. This method involves a delay of 10ms and is implemented in section 3.3 of this project.

Once the harmonics have been detected and measured, they can be subtracted from the supply by using the injection transformers as in [4, 12]. However, the filter at the output of the converter will affect the injected voltages in a similar way to that with the fundamental components. [4, 12] do not offer compensation for the effect of the filter. In [28, 30], a filter compensation matrix for harmonics similar to the one developed for the fundamental component [26-28, 30] is proposed. Although this algorithm has been found to present a poor transient performance when applied to the positive and negative sequence components [6, 32 ,33], it is suitable for mitigation of harmonics that usually happens in steady state [28]. A better method would be to use the DVC algorithm applied to the positive and negative sequences to each harmonic in the different d-q synchronous frames where each harmonic is detected as dc components. None of the papers studied have applied this concept.

1.6.3 Summary and Conclusions of the Research

The relevant literature survey can be summarized as follows:

- The use of a system combining both a shunt and a series converter is a powerful solution for mitigation of power quality problems. However, the control of this system as a UPQC is very complex.

- The VOC-SVPWM method for DC bus regulation is the preferred method and uses the efficient SVPWM. However, due to the limitation of the DS1104 Controller card, only the HCC technique can be implemented.

- The transformation of the positive and negative sequences in two synchronous frames where each sequence appears as dc components simplifies the design of the respective controllers. This technique is implemented in this thesis.

- The low pass filter at the output of the converter affects the voltages injected by the converter. Several algorithms have been discussed for compensation of the filter effects. The first technique performs a back calculation of the filter input voltage to compensate for the filter effect but is based on the assumption that the injection transformers are ideal. Furthermore, this method has been found to offer poor transient performance and is sensitive to variations in filter parameters. The MDVC provides a much better solution but also assumes ideal transformers. It also requires the measurements of 12 signals and thus can not be implemented using the DS1104 Controller card which includes only 8 ADC channels.

- Finally, techniques for detection and mitigation of harmonics have been discussed. The most accurate technique uses half cycle averaging of the d-q components of the supply in different synchronous frames to isolate and measure the magnitude and phase of each harmonic separately. This algorithm is implemented in this project.

2 DESIGN OF THE PROPOSED SYSTEM

This chapter begins with a description of the configuration chosen for the compensator. Then, all the different elements of the system are discussed. Special attention is given to the choice made for the turns ratio of transformers. This ratio determines the overall rating of the system in comparison to the load. Finally, the function of each converter, and as the corresponding switching method for each of them, is also described.

2.1 Connection scheme of the compensator

One of the converters is connected in parallel with the line and will be referred to as the shunt converter. An LC filter is placed between the converter and the supply to remove high frequency harmonics. Line inductors are also used to limit the amount of ripple current [24]. The other converter is connected in series with the line through series injection transformers. Again, an LC filter is used to cancel the high frequency harmonics of the inverter. Both converters share a common DC bus that is supported by a capacitor bank. The shunt converter can be placed upstream of the series compensator or on the load side. In this thesis, the shunt converter is placed upstream of the compensator to maintain the power rating of the converter as low as possible. Indeed, if the shunt converter were placed on the load side, the series inverter would have to supply power both to the load and to the shunt converter. Three resistors and contractors are placed in series with the supply to create disturbances. This arrangement is discussed in section 2.6. The system is tested with a 10kW resistive load made up of nine 48.5Ω resistors rated at 220V. However, the prototype built is rated for a larger load due to the availability of equipment in the machine's laboratory. Figure 2.1 illustrates the configuration used in this project.

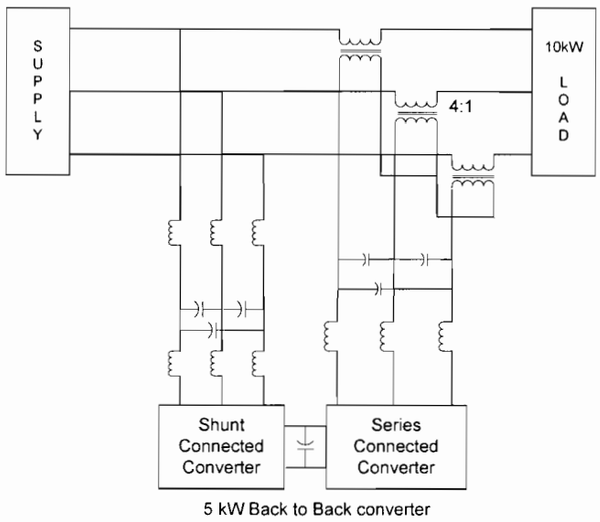

Figure 2-1: Configuration of compensating device

The device can be off and operated in standby mode when there is no disturbance, and switched on by the occurrence of a disturbance. In standby mode, the compensator side of the transformer is short circuited to reduce its leakage impedance. Alternatively, the compensator can be continually on, providing compensation during normal operation (no disturbance) to compensate the voltage drop due to the load current flowing in the series transformer [35]. In this project, the compensator is operated continually.

2.2 The Series Injection Transformers

Three identical single phase transformers are used to inject voltage in series with the line. Each transformer is rated to a third of the size of the mitigation device. However, in this project, three 5000 KVA transformers as showed in figure 2.2, are used as they are the only available transformers in the machine's laboratory.

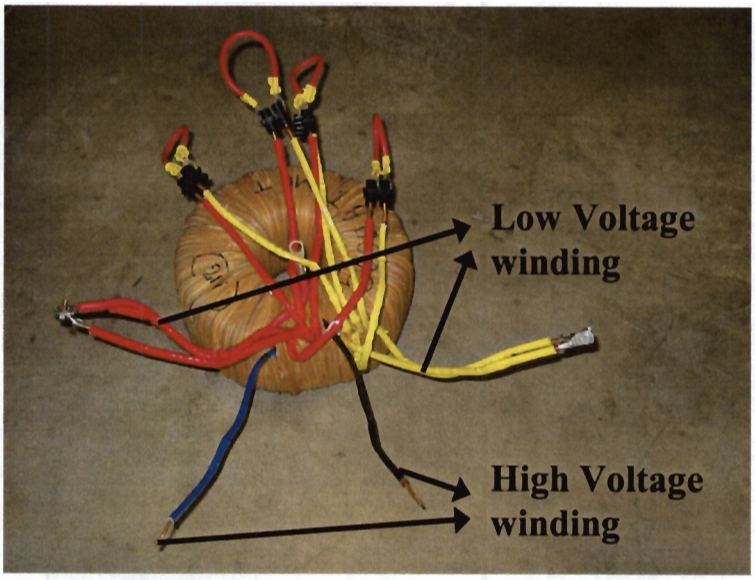

Figure 2-2: Series injection transformer

The primary side of the transformer is connected in star to the series inverter via an LC filter. The secondary side is connected in series with the line on the load side. The transformers should have low impedances so that the voltage drop across them is negligible. The transformer's turns ratio must be carefully chosen as it determines:

- The ratio between the load rated power and that of the mitigation device
- The mitigation range possible
- The cost of the system

Three identical single phase 4:1 turns ratio transformers are preferred in the prototype built in this project. With that ratio, the mitigation device only needs to be rated at a quarter of the maximum load rated power. Thus, all the components that make up the device are rated for a quarter of the rated load power. Consequently the price for each of these components is reduced resulting in a much cheaper system than if it was rated for the full load rating. The drawback of this saving is that the device can only mitigate for disturbances of 25% of the supply voltage. However, as mentioned in section 1.2.1, most of the dips are typically to about 0.7 pu of a nominal 1.0 pu supply voltage. Thus, if a dip of that magnitude should occur, the mitigation device would bring the voltage on the load side up to 0.95 pu (0.7 + 0.25), which is acceptable

according to the ITIC curve illustrated in figure 1.1. However, if greater dips were to occur, the device would only be able to bring the system back by 25%.

The equivalent circuit of the transformer referred to the high voltage side is illustrated in figure 2.2 [38]. The circuit parameters were determined by performing an open-circuit test and a short circuit test. Results from these two tests as well as the calculations of the circuit parameters are shown in appendix A.

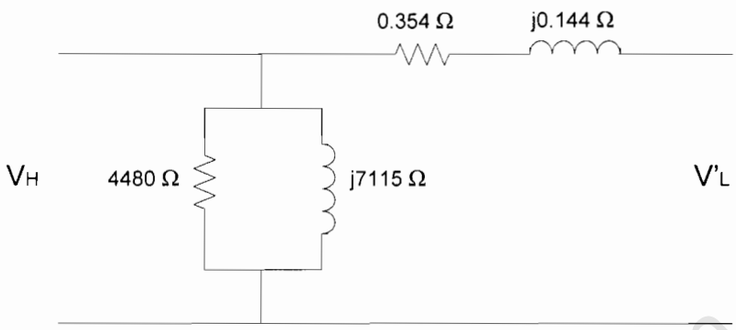

Figure 2-3: Transformer equivalent circuit referred to high voltage side

2.3 The LC filters

The LC filters reduce the dv/dt effect on windings of the injection transformer and remove the high frequency harmonics produced by the high frequency switching of the IGBTs to obtain a sinusoidal voltage waveform [12]. The range of capacitors and inductors available in the Machines Laboratory at UCT is limited and the best combination is chosen to achieve the finest filtering possible. The cut-off frequency of each filter is also calculated using the following formula:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (2.1)$$

A large inductor was used for the shunt converter to reduce the current overshoot of the hysteresis currents. This is discussed in section 2.5.2.The parameters of the filter are indicated in table 2.1. They have been calculated as follows:

Table 2-1: Parameters of the LC filter

	Shunt Converter	Series Converter
L, Inductance	40mH	2.5mH
C, Capacitance	9uF	9uF
Cut-off Frequency	265Hz	1060Hz

2.4 The Series Inverter

The series inverter is the main component of the system. It controls the magnitude and phase of the voltage to be injected through the series transformers to keep the load voltage balanced. The switching technique used for the series inverter is Space Vector Pulse Width Modulation (SVPWM) technique. This switching technique is described in the following section. A control algorithm (discussed in detail in chapter 3) detects disturbances in the supply voltage and evaluates the corresponding voltage that must be injected by the series inverter to shield the load side voltage from the disturbance. The outputs of this control algorithm are the two stationary frame components, U_α and U_β. These components are used as inputs to the SVPWM technique that produces the switching signals for the IGBTs of the inverter.

2.4.1 Advantages of Space Vector Pulse Width Modulation Technique

SVPWM is chosen because it offers many advantages over other Pulse Width Modulation (PWM) methods [36, 37]:

- It generates lower harmonic content in the output current, especially at high modulation indexes.

- It uses the dc-bus more efficiently than sinusoidal PWM. A 15% increase in DC link voltage utilization is obtained compared to the sinusoidal PWM.

- It minimizes switching losses by performing the minimum amount of switching required to change states. This performance is achieved by changing the state of only one switch when going from one switch combination to the other.

- SVM allows its user to place the voltage or current space vector exactly where desired in the d-q plane.

2.4.2 Analysis of SVPWM

Only the top 3 switches of the converter need to be controlled. The 3 bottom switches require the opposite states of the corresponding top switches. As a result, 8 combinations are possible. These combinations range from (000) to (111), where the first number represents the state of switch S1, the second number that of switch S3 and the last one that of switch S5 as shown in the figure 2.4. A '0' indicates an open switch and a '1' indicates a closed one.

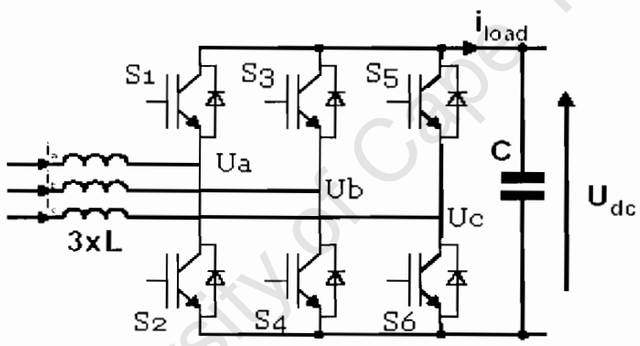

Figure 2-4 : Typical schematic of a converter

For each state, the phase voltages U_a, U_b and U_c can be summed vectorially to obtain the resultant space vector in the α-β plane. Each combination thus represents a vector in the α-β plane called a basic vector. The eight combinations form a hexagon. Two combinations, (000) and (111) lie at the centre of the hexagon. They are called the zero vectors. The other six combinations form six sectors inside the hexagon and are called the non-zero basic vectors [36]. This hexagonal structure is showed in figure 2.5.

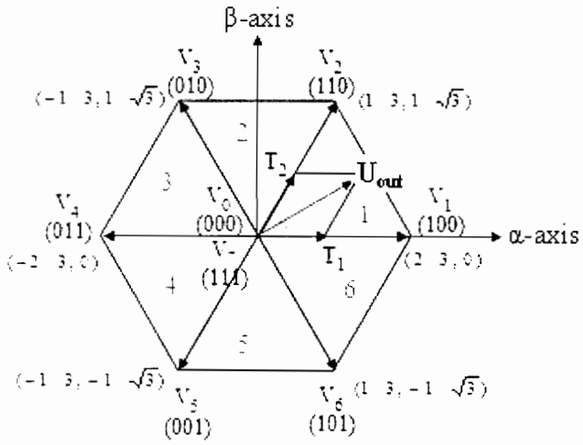

Figure 2-5: The Basic Space Vectors (Normalized w.r.t. Vdc) and Switching States

The average output voltage vector, $\mathbf{U_{out}}$ (corresponding to the maximum fundamental phase voltage), can be created by time weighted averaging of the two neighboring basic non-zero vectors that form the sector in which $\mathbf{U_{out}}$ lies, as well as the two zero vectors for equal time duration [36]. In figure 2.5, $\mathbf{U_{out}}$ is obtained by applying the non-zero basic vectors (100) and (110) for times t_1 and t_2 and applying the zero basic vectors (000) and (111) for the rest of the period time i.e. $t_0 = T_s - t_1 - t_2$ [36]. The use of the two zero basic vectors ensures that only one converter phase is commutated at time.

2.4.3 Avoiding Over Modulation

The inputs to the SVPWM technique used in this thesis are $U_\alpha(t)$, $U_\beta(t)$ and $V_{dc}(t)$, the magnitude of the DC bus. $U_\alpha(t)$ and $U_\beta(t)$ are the two components of $U_{out}(t)$, and are obtained from two peak line-to-line voltage measurements using the modified Clarke transform (refer to equ.3.2 in section 3.1.1). In this project, the control loop may produce values of U_α, and U_β which causes $U_{out}=\sqrt{((U_\alpha)^2+ (U_\beta)^2)}$ to be greater than the maximum achievable value represented by the hexagonal envelope which corresponds to the linear modulation range. If $\mathbf{U_{out}}$ exceeds the hexagon, $(t_1+ t_2) > T_s$, and over modulation occurs. If this condition arises, then $t_1$and t_2 must be rescaled by dividing each of them by $(t_1+ t_2)$. However, for sinusoidal line to line voltages, the locus of vector $\mathbf{U_{out}}$ should be circular. Thus, the largest possible voltage magnitude that can be achieved using this switching strategy is equal to the radius of the largest circle

that can be fitted inside the hexagon of figure 2.5 [36] rather than equal to the magnitude of the vector that can be fitted inside the hexagonal envelope. Hence, it is essential to limit the two stationary frame components so that $U_{out} \leq V_{dc}/\sqrt{3}$. A limiting method is used to constrain U_{out} to the maximum circular locus described above. If U_{out} exceeds $V_{dc}/\sqrt{3}$, the limiting method will shrink U_{out} to $U_{out}^* = \sqrt{((U_\alpha^*)^2 + (U_\beta^*)^2)}$ so that it does not exceed $V_{dc}/\sqrt{3}$. The new vector will be oriented in the same direction as U_{out} but will be shorter. This shrinkage is achieved by readjusting U_α and U_β to U_α^* and U_β^* as shown by equ.2.2 and equ.2.3.

$$U_\alpha^* = \frac{V_{dc}}{\sqrt{3}.\sqrt{U_\alpha^2 + U_\beta^2}} \times U_\alpha \qquad (2.2)$$

$$U_\beta^* = \frac{V_{dc}}{\sqrt{3}.\sqrt{U_\alpha^2 + U_\beta^2}} \times U_\beta \qquad (2.3)$$

2.4.4 Determining Sector and State Times

Knowing the sign and magnitude of U_α and U_β, the sector in which U_{out} lies is easily found as illustrated by the flow diagram shown in figure 2.6 [37].

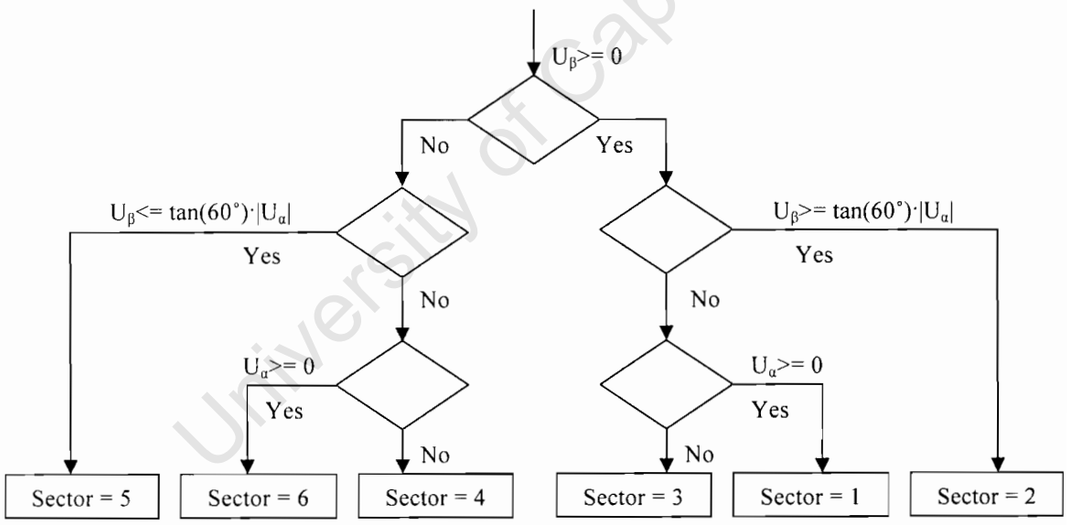

Figure 2-6: Flow diagram to find sector [37]

Once the sector is known, times t_1 and t_2 are calculated using the table 2.2 below:

Table 2-2: Formula to calculate duty cycle once sector number is known [37]

Sector Number	Duty Cycle $t_x = \frac{T_s}{V_{DC}}\{A.U_\alpha + B.U_\beta\}$	A	B
Sector 1	$t_{1(Sector1)}$	1	$-\frac{1}{\sqrt{3}}$
	$t_{2(Sector1)}$	0	$\frac{2}{\sqrt{3}}$
Sector 2	$t_{1(Sector2)}$	1	$\frac{1}{\sqrt{3}}$
	$t_{2(Sector2)}$	-1	$\frac{1}{\sqrt{3}}$
Sector 3	$t_{1(Sector3)}$	0	$\frac{2}{\sqrt{3}}$
	$t_{2(Sector3)}$	-1	$-\frac{1}{\sqrt{3}}$
Sector 4	$t_{1(Sector4)}$	-1	$\frac{1}{\sqrt{3}}$
	$t_{2(Sector4)}$	0	$-\frac{2}{\sqrt{3}}$
Sector 5	$t_{1(Sector5)}$	-1	$-\frac{1}{\sqrt{3}}$
	$t_{2(Sector5)}$	1	$-\frac{1}{\sqrt{3}}$
Sector 6	$t_{1(Sector6)}$	0	$-\frac{2}{\sqrt{3}}$
	$t_{2(Sector6)}$	1	$\frac{1}{\sqrt{3}}$

Once t_1 and t_2 have been found, t_0 is calculated as $t_0 = (T_s - t_1 - t_2)$.

2.4.5 Obtaining the switching signals

The next step is to create three reference voltage signals representing the three phases to compare to a carrier signal of frequency, $1/T_s$, to obtain the PWM signals required [37].

$$A_{ref} = t_1 + t_2 + \frac{t_0}{2} \qquad (2.4)$$

$$B_{ref} = t_2 + \frac{t_0}{2} \qquad (2.5)$$

$$C_{ref} = \frac{t_0}{2} \qquad (2.6)$$

The comparison with the high frequency carrier signal is done using 3 comparators, CMP1, CMP2 and CMP3. Note that the frequency of the carrier determines the switching frequency ($f_s=1/T_s$).

To ensure that only one switch changes state when going from one combination to the other, the reference voltages, A_{ref}, B_{ref} and C_{ref}, must be compared to the carrier signal using the correct comparators depending on the sector in which U_{out} is lying in. Table 2.3 indicates which comparator must be used for each voltage reference in a particular sector [37].

Table 2-3: Reference voltage and Comparator combinations for minimum switching [37]

Sector	CMPR1	CMPR2	CMPR3
1	A_{ref}	B_{ref}	C_{ref}
2	B_{ref}	A_{ref}	C_{ref}
3	C_{ref}	A_{ref}	B_{ref}
4	C_{ref}	B_{ref}	A_{ref}
5	B_{ref}	C_{ref}	A_{ref}
6	A_{ref}	C_{ref}	B_{ref}

Figure 2.7 illustrates the three voltage references A_{ref}, B_{ref} and C_{ref} as well as the carrier signal. The PWM signal is created by comparing the voltage reference signals to the carrier. If the voltage reference signal is larger than the carrier, the output signal is "1". Similarly, if the reference voltage lies below the carrier, the output signal is "0".

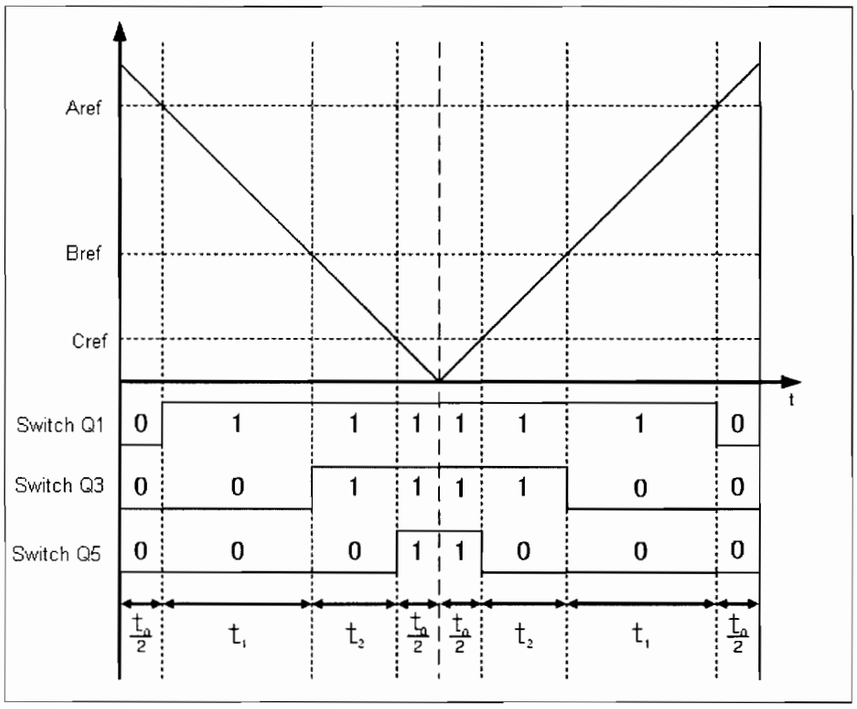

Figure 2-7: Comparison of reference voltages to obtain switching pattern [37]

Once the 3 voltage references have been compared to the carrier signal, 3 PWM signals are obtained for the top 3 switches. These signals are then inverted and fed to the bottom switches. This SVPWM algorithm is used for the simulations in Matlab-Simulink. However, when the system is implemented in real time using the DS1104 controller card, there is a limit on the minimum step size achievable. Thus, the generation of a high frequency carrier signal as well as the comparison of the three reference signals with that carrier is difficult to implement. However, the DS1104 controller card provides a SVPWM block available from the DS1104 RTI library which is able to produce high frequency switching signals independent of the step size. This block uses the times t_1 and t_2 as inputs and does the remaining processing to obtain the switching signals. However, only one SVPWM block is available so that only one converter can be controlled using that switching technique.

2.5 The Shunt Converter

The shunt converter is connected to the supply and shares a common DC bus with the series converter. Its function is to transfer active power to maintain a stiff DC bus that supplies the series converter. In the case of a voltage dip, the series inverter needs to add voltage to maintain a constant voltage on the load side and absorbs power from the DC bus to do so. In addition, during a voltage dip, more power is absorb from the supply by the shunt converter to maintain a constant DC bus. On the other hand, in the case of a voltage swell, the series inverter must remove the extra voltage and thus dumps all the extra power on the DC bus. This extra power is then transferred to the supply by the shunt converter (which now acts as an inverter). The shunt converter thus has to achieve bi-directional power flow in order to maintain the DC bus constant. The theory behind bidirectional power flow is discussed in section 2.5.1. Different control algorithms are presented in [23] with the Voltage Oriented Control being the preferred one. However, the HCC technique is used because only one converter can be controlled by the DS1104 Controller card using SVPWM switching as mentioned in section 2.4.5. The HCC technique is studied in the sections 2.5.2 and 2.5.3.

2.5.1 Bidirectional Power Flow

A typical configuration used for a grid connected converter for bidirectional power flow and DC bus voltage regulation is shown in figure 2.8. The converter is connected to the grid through line inductors. The inductors limit the amount of ripple current [24]. This configuration can be simplified as illustrated in figure 2.9. 'E' represents the supply (grid) voltage and 'U' represents the voltage supplied by the converter while 'i' is the current flowing through the line inductor. The resistance 'R' of the inductor is neglected since the voltage drop on resistance is much lower than the voltage drop on the inductance.

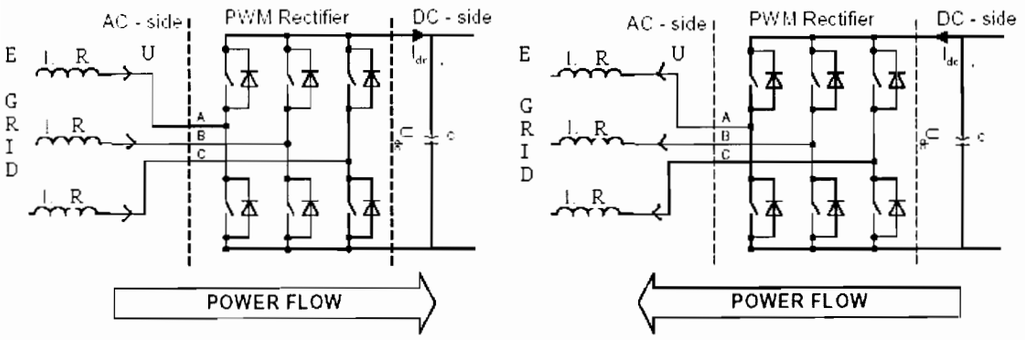

Figure 2-8: Bi-directional power flow in converter

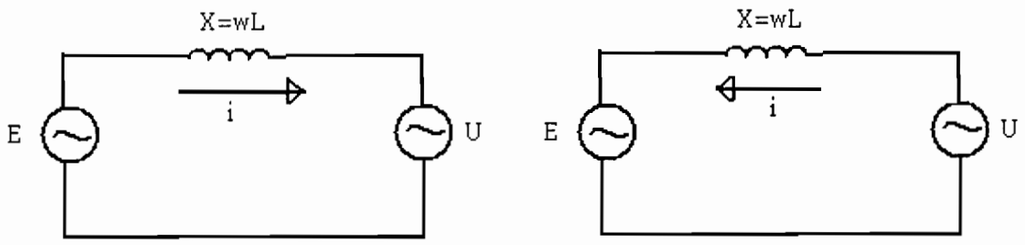

Figure 2-9: Simplified schematic of converter set up

Using figure 2.9, respective vector diagrams in the d-q plane can be drawn to illustrate bidirectional power flow at unity power factor. This is shown in figure 2.10. The supply voltage's vector **E** is locked to the d-axis. This is explained in section 3.1.1.

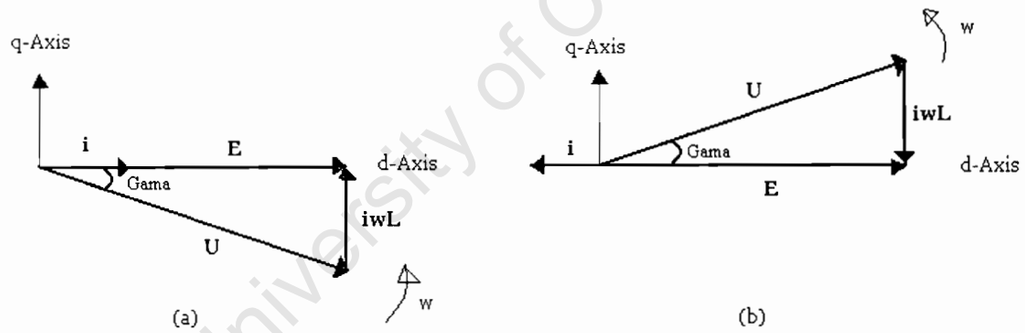

Figure 2-10: (a) Power flow to DC bus, (b) Power flow to grid

In Figure 2.10(a), the current is in phase with the supply voltage and **U** lags **E**. Thus, real power flows from the supply to the DC bus. On the other hand, in figure 2.10(b), the current is 180 degrees out of phase with the supply voltage and **U** leads **E** showing that real power flows out of the DC bus to the supply.

Table 2-4: Parameters for the PI current controller

Proportional Gain (Kp)	1
Integral Gain (Ki)	100
Upper Limit	30
Lower Limit	-30
Output Initial Value	0
Sample Time	Ts

Then, using the inverse Park transform (equ.2.9) [40], and the supply voltage angle θ, $i_{\alpha\ ref}$ and $i_{\beta\ ref}$ are obtained from $i_{d\ ref}$ and $i_{q\ ref}$. Then, using the inverse Clarke [40] transform, the reference three phase currents, $i_{abc\ ref}$, are found (equ.2.10).

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix} \qquad (2.9)$$

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \qquad (2.10)$$

Once the reference currents have been processed, they are compared to the real line currents by a hysteresis controller which then determines the switching states of the converter. The converter valves are switched to keep track of the reference currents. When the current exceeds its reference value by a certain margin x, the top switch is turned off and on again when the current falls below the reference value by the same margin x [41]. (The bottom switches are fed with complementary signals of the top switches.)

TA+ on (=> TA- off) when $i_a = (i_{a\ ref} - x)$

TA+ off (=> TA- on) when $i_a = (i_{a\ ref} + x)$, where x = current hysteresis band.

As a result, the phase currents are confined within a sinusoidal band: $(i_{a\ ref} - x)$ and $(i_{a\ ref} + x)$ as illustrated in figure 2.12.

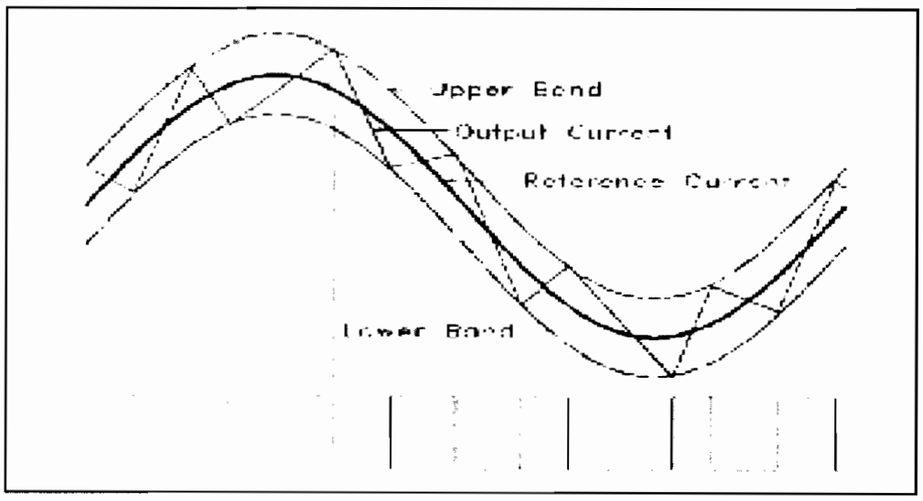

Figure 2-12: Principle of Hysteresis Current Control [41]

However, the sampling frequency dictates whether or not the currents remain confined to the hysteresis band. In fact, with a digital controller, events happen at discrete intervals. The measured currents are digitised and compared to their reference digitally at the sampling frequency of the analogue to digital converter (ADC) that samples the measured currents. If this sampling frequency is too low it is feasible that the current will have exceeded the hysteresis band by the time the comparison is made. [24] Figure 2.13 shows the how the current regularly exceeds the hysteresis band if the sampling frequency is too low.

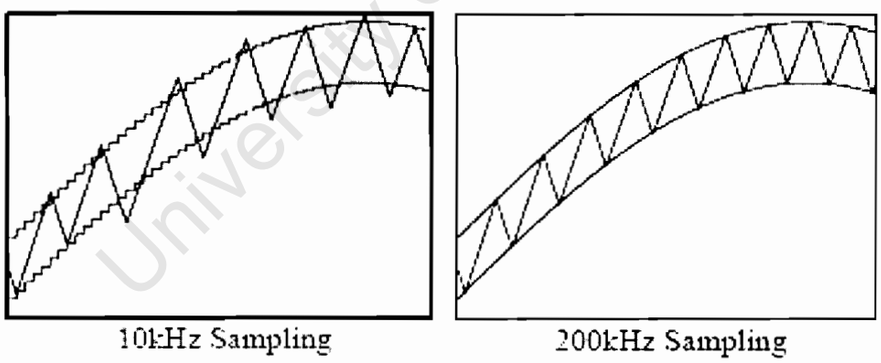

Figure 2-13 : Current overshoot at different sampling frequencies [24]

The current overshoot is related to the size of the line inductors, the sampling frequency and the DC bus voltage. In fact, with a large inductor, di/dt is smaller and thus current overshoot decreases. The inductor limits the amount of ripple current. Similarly, the lower the sampling f_{sample} the smaller the overshoot will be for the same inductor size [24].

Equ.(2.11) gives the maximum current overshoot Δi_{Over} for an inverter using a DC bus voltage V_{DC} with line inductance L while sampling at f_{Sample} assuming that $v_{Supply} = 0$. [24]

$$\Delta i_{Over} = \frac{1}{2 f_{Sample}} \frac{V_{DC}}{L} \qquad (2.11)$$

2.6 Creating faults

Faults can also be simulated using a fault generator [21] or a programmable power supply [12]. However, neither a fault generator nor a programmable supply voltage is available in the laboratory. Thus, to simulate faults, a combination of three single phase resistors and contractors is used as shown in figure 2.14.

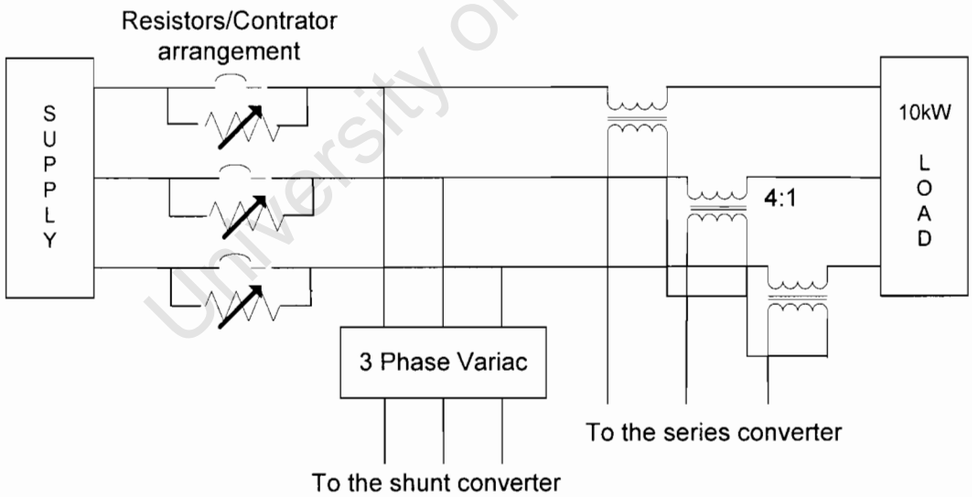

Figure 2-14: Schematic of the resistors/contractor arrangement for creating faults

This configuration gives faults types that are comparable to those created by a fault generator [7]. Current flowing to the load flows through the resistors causing a voltage drop. As a result, by varying the size of these resistors, balanced and unbalanced dips are generated. Swells are generated by stepping up the supply voltage using a three phase variac and dropping voltage across the resistors to obtain 380V at the output of the variac. By disconnecting the resistors, a sudden increase in voltage occurs simulating a swell. Harmonics already present in the UCT supply are used to test the final algorithm including harmonic mitigation. The two main harmonics present are the 5th and the 7th as illustrated in figure 2.15.

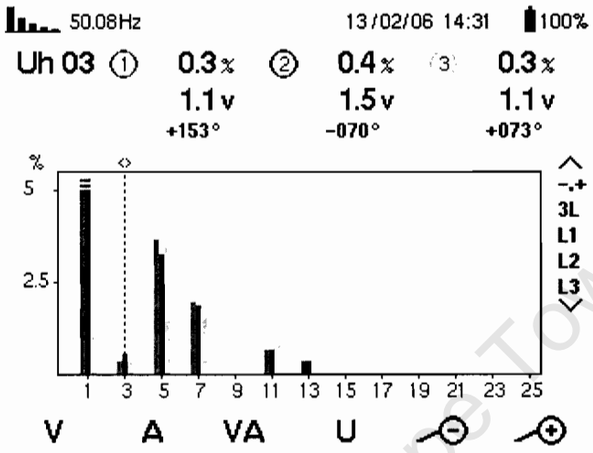

Figure 2-15: Harmonic spectrum of the UCT supply

3 DETECTION & MITIGATION OF THE DISTURBANCE

3.1 Balanced Voltage Dips or Swells

This section describes how three phase balanced voltages are measured and transformed to a synchronous reference frame where the magnitude of these voltages is obtained as a dc component. This dc component is then used to detect balanced dips or swells. A control algorithm is then developed to compensate for these disturbances.

3.1.1 Transformation of Balanced Voltages into Synchronous Frame

Any balanced three phase voltage system free from harmonics consists solely of a positive sequence voltage. The supply voltage can be represented as a vector which in this case is equal to the positive sequence voltage vector, whose locus is a circle [42], rotating counterclockwise with speed, ω, in a stationary reference frame called the α-β reference frame. This circular locus is illustrated in figure 3.1 below:

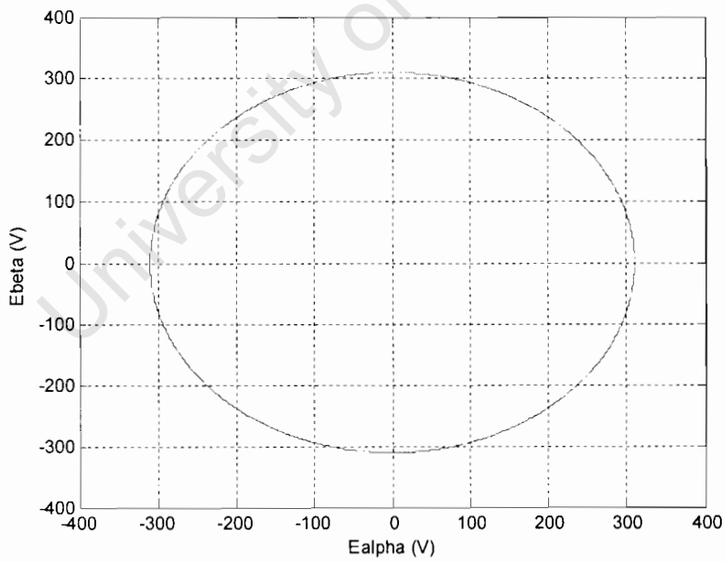

Figure 3-1: Locus of the 3 phase balanced voltages in stationary frame

The α-β stationary frame components can be obtained from three phase voltage measurements by using the Clarke transform [40]:

(1 1)

The real power transferred in a circuit such as figure 2.7 is given by [38]:

$$P = \frac{(E * U)}{\omega L} * \sin(\delta) \qquad (2.7)$$

where 'δ' is 'Gama' in figure 2.8 and is known as the 'power angle' [38].

Thus, by varying 'δ', the amount of real power flowing can be altered. Whenever the real power demand is changed, 'δ' is changed accordingly to meet that demand.

The reactive power transferred is given by [38]:

$$Q = \frac{E}{\omega L} * (U \cos(\delta) - E) \qquad (2.8)$$

Power flow at unity power factor is achieved when no reactive power flows, i.e., when cos (δ) = E / U. That happens when the current is in phase or 180 degrees out of phase with the supply voltage as illustrated in figure 2.8. Because the supply voltage's vector **E** is locked to the d-axis, the current vector **i** must also be locked to the d or –d axis to achieve unity power factor. This is achieved by setting the q-component of the current, i_q, to zero.

2.5.2 Overview of HCC

In this section the use of hysteresis current controllers to control the switches of the shunt converter is discussed. The DC link voltage is kept constant at all times using a PI controller which forces the DC voltage across the capacitor bank to track its reference value. In addition, a vector controlled approach is used to achieve independent control of the reactive power. The schematic is shown in the figure 2.11.

$$\begin{pmatrix} E_\alpha(t) \\ E_\beta(t) \end{pmatrix} = \begin{pmatrix} \frac{1}{3} & \frac{1}{3} \\ \frac{\sqrt{3}}{3} & \frac{-\sqrt{3}}{3} \end{pmatrix} \begin{pmatrix} E_{ab}(t) \\ E_{ac}(t) \end{pmatrix} \qquad (3.2)$$

Once transformed to the stationary frame, the positive sequence voltage can then be represented in a synchronous reference frame called the d-q reference frame using the Park transform [40]:

$$\begin{pmatrix} E_d(t) \\ E_q(t) \end{pmatrix} = \begin{pmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{pmatrix} \begin{pmatrix} E_\alpha(t) \\ E_\beta(t) \end{pmatrix} \qquad (3.3)$$

$\theta(t) = \omega t$ is a rotating angle between the d axis and the α axis. By choosing $\theta(t)$ properly, it is possible to obtain dc values of the voltage components, which is very advantageous in the control of the inverter. This technique is described below.

Let $\beta(t)$ be the supply voltage angle, i.e. the angle between the supply voltage vector, **E** (equal to the positive sequence voltage), and the α-axis as shown in figure 3-3(a). Angle $\beta(t)$ rotates between π and $-\pi$. Figure 3.2 obtained through simulation in Matlab-Simulink illustrates angle $\beta(t)$.

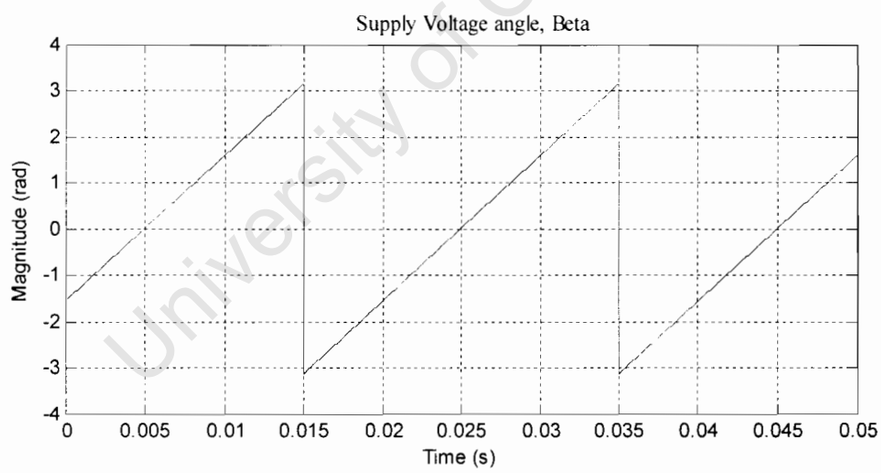

Figure 3-2: Supply Voltage angle, β

The supply voltage vector, **E,** is locked to the d axis by simply letting θ(t) equal to β(t) (equ.3.3). The 'atan2' function provided by Matlab-Simulink is used in this thesis and takes into account the quadrant in which the two vectors lie. This concept is shown in figure 3-3(b).

$$\theta(t) = \beta(t) = \arctan\left(\frac{E_\beta(t)}{E_\alpha(t)}\right) \qquad (3.4)$$

The d-axis is the real axis and the q axis is the imaginary one. In contrast to the α-β frame which is stationary, the d-q frame rotates anticlockwise at a speed ω. Thus the supply voltage vector, **E,** which also rotates at speed ω now becomes stationary in this new rotating frame.

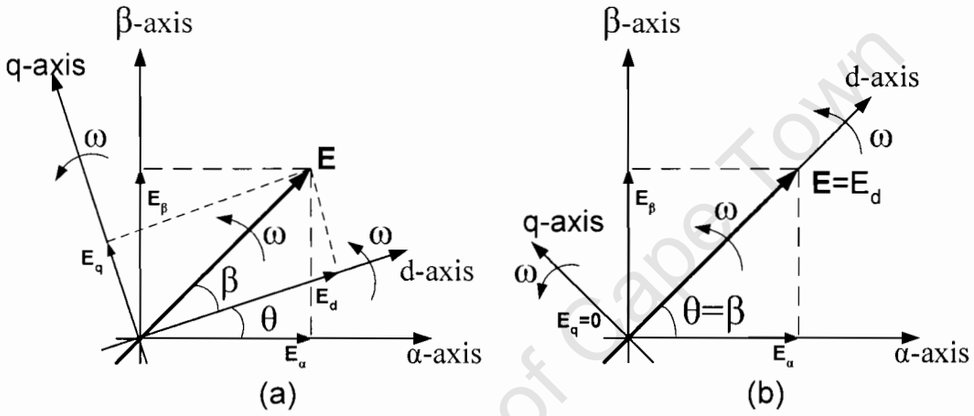

Figure 3-3: (a) α-β Reference frame, (b) d axis locked to vector E

By locking the voltage space vector to the d axis, the q-component, $E_q(t)$, of the voltage vector is forced to zero while the d-component, $E_d(t)$, becomes dc. Figure 3.4 obtained from a Matlab-Simulink simulation illustrates this concept. Using the modified Park (equ.3.2) transform and the Park transform (equ.3.3), $E_d(t)$ becomes equal to 311V for a 380V line to line system as shown in figure 3.4.

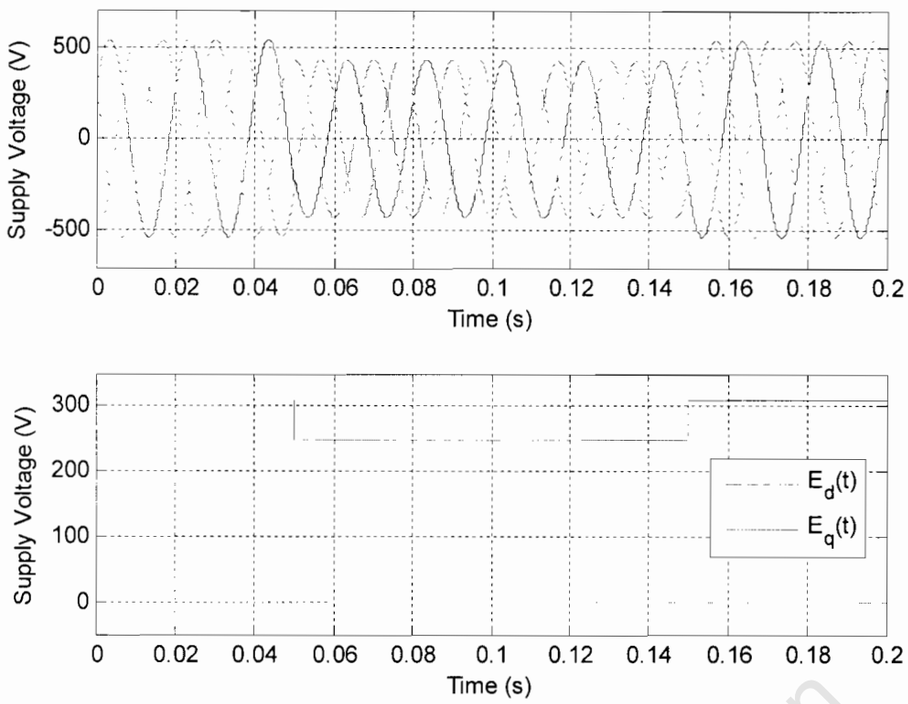

Figure 3-4: DC representation of a balanced voltage dip

3.1.2 Positive Sequence Voltage Controller

$E_d(t)$, the dc representation of the supply voltage is fed to a controller that is designed to keep the voltage on the load side steady. To mitigate a dip, the series inverter needs to inject the missing voltages via the series transformers. For example, in the event of a dip of 60V, the inverter must add 60V with the series connected transformers. Knowing that $E_d(t)$ is 311V for 380V rms line to line voltages, the reference voltage $E_{dref}(t)$ is set to 311V. Thus, $E_d(t)$ is simply compared to its reference and the error transformed back to the stationary α-β frame using angle $\theta(t)$. The real and imaginary components are used as inputs to the SVPWM technique for the switching of the inverter. A schematic of the control is shown in figure 3-5. Because 4:1 step down series transformers are used, a gain of 4 is introduced in the algorithm.

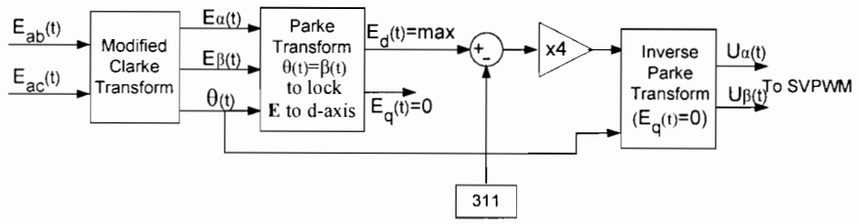

Figure 3-5: Control Schematic for mitigation of balanced faults

It must be noted that perfect compensation can not be achieved using this method because of the effect of the LC low pass filter and transformers combination present at the output of the inverter (figure 2.1). Together, they cause a volt drop as well as a phase shift which has not been taken into account.

3.1.3 Improved Positive Sequence Voltage Controller

A PI controller is proposed to ensure zero steady state error and compensate for the voltage drop across the filter and transformer combination. Two line to line voltages are measured on the load side to calculate the d-component $V_d(t)$ of the load voltage. This value is compared to the reference load voltage d-component $V_{dref}(t)$ and the error fed to the PI controller. The parameters of the PI controller are illustrated in Table 3-1. The appropriate parameters are obtained experimentally by trial and error.

Table 3-1: Parameters of the PI controller for voltage regulation

Proportional Gain (K_p)	1
Integral Gain (K_i)	10
Upper Limit	350
Lower Limit	220
Output Initial Value	310
Sample Time (T_s)	2e-5

The output of the PI controller is subtracted from E_d and the error is transformed back to the α-β stationary frame, again using the angle θ(t). Note that a constant angle, δ, equal to the phase shift caused by the LC filter and transformer combination, is subtracted from the angle θ(t) before transforming back to the α-β stationary frame. Angle, δ, is constant at all times for practical purposes. This step of the algorithm serves to cancel the phase shift effect of the combination of the filter and transformers. Thus, when setting up the device, one must adjust δ until the correct value for full compensation of the phase shift is determined. The α-β components are then used as inputs to the SVPWM technique. The new algorithm including compensation for the filter is shown in figure 3.6.

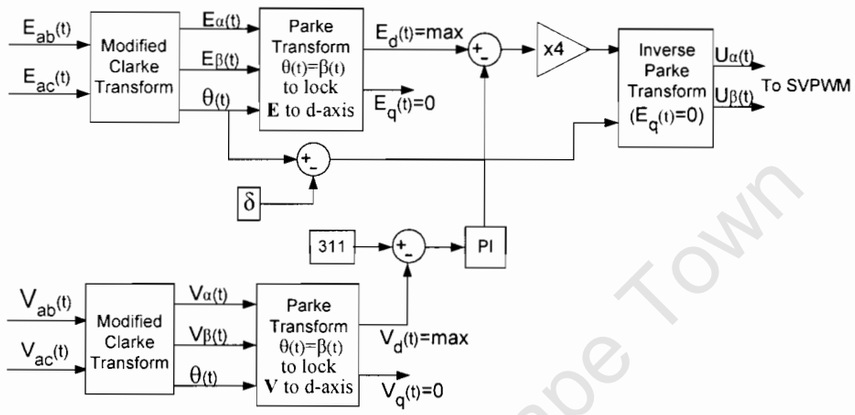

Figure 3-6: Schematic of improved control algorithm for positive sequence voltage

This compensation algorithm only works provided no unbalance is present in the supply voltage. In the presence of an unbalance, the q-component, $E_q(t)$, of the supply voltage will still be zero. However, the d-component, $E_d(t)$, will no longer exist as dc and the supply voltage angle becomes distorted. In fact, in the presence of a negative sequence in unbalanced systems, $E_d(t)$ will appear as a dc component superimposed with oscillations at twice the system frequency. This effect is demonstrated by figure 3.7 obtained from simulation in Matlab-Simulink. The oscillations are due to the presence of a negative sequence vector that rotates in opposite direction to the d-q synchronous frame. As a result, the vector appears to be rotating at double the speed [6, 26, 28, 43].

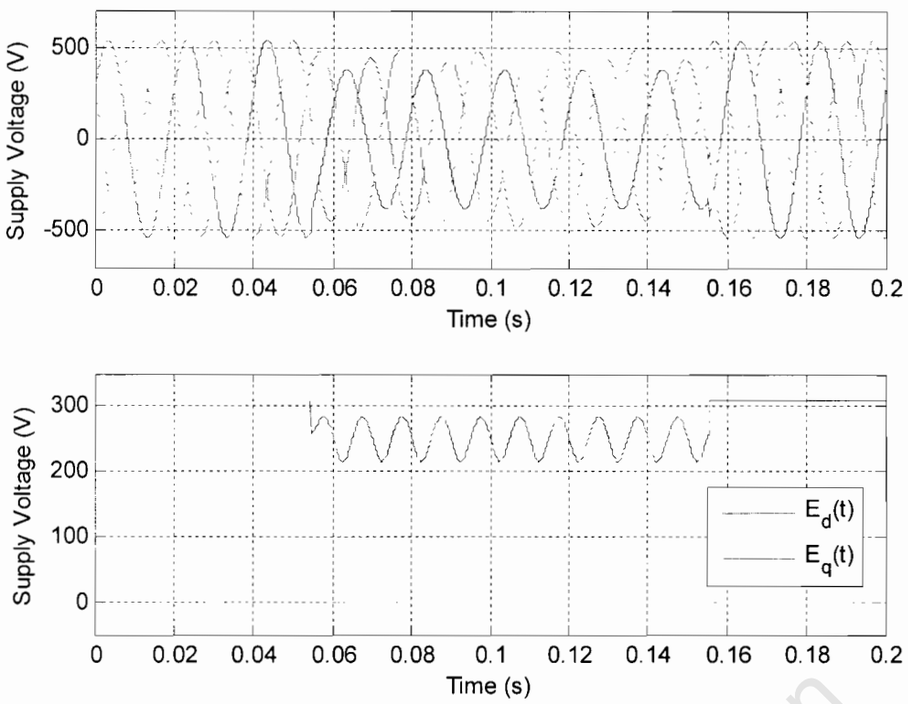

Figure 3-7: 100 Hz oscillations superimposed during an unbalanced dip

Likewise, harmonics will have a similar effect on $E_d(t)$ and on the supply voltage angle except that the superimposed oscillations will have different frequencies depending on the harmonic order [43]. For example, a 5^{th} harmonic rotating in a clockwise direction (opposite direction to the d-q synchronous frame) will appear as 300Hz ((5+1) x 50Hz) oscillations. Figure 3.8 shows the simulation results obtained when transforming a 5^{th} harmonic contaminated three phase voltage to the synchronous frame. A 7^{th} harmonic rotating in the same direction as the d-q synchronous frame will also appear as 300Hz ((7-1) x 50Hz) oscillations. On the other hand, an 11^{th} harmonic rotating in a clockwise direction will appear as 600Hz ((11+1) x 50Hz) oscillations.

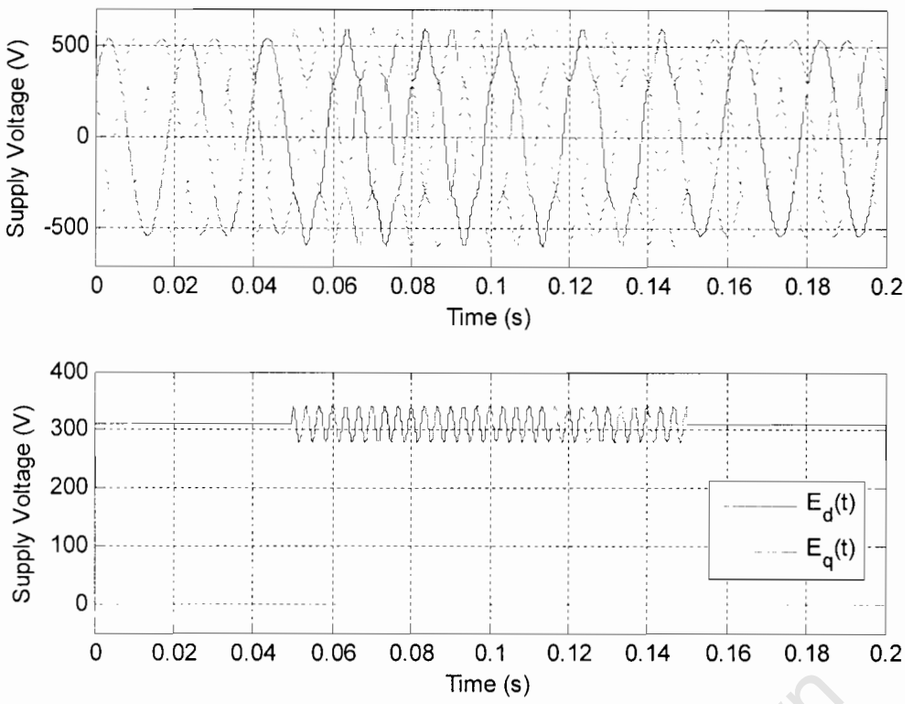

Figure 3-8: 300Hz oscillations superimposed due to a 0.05pu of 5th harmonic

In this project, both the positive sequence controller and its improved version are tested in simulations and experimentally. However, as mentioned in section 2.6, the UCT supply does not have a pure sinusoidal waveform. Thus, oscillations will appear superimposed on $E_d(t)$ as well as on $V_d(t)$ resulting in failure of the controller. However, unlike unbalance, harmonics can be filtered. Thus, the supply α-β voltage components are filtered to obtain improved sinusoidal signals. Band pass filters work better than low pass filters as they do not introduce a phase shift in the signals filtered. The oscillations caused by harmonics on $E_d(t)$ and $V_d(t)$ can be greatly reduced by the filters so that both algorithms can be tested experimentally. However, the use of the filters delays the response of the two controllers. In this project, discrete second order band pass filters from the SimPowerSystem Toolbox in Matlab-Simulink are used to filter the harmonics on both the supply and the load voltage. Figures 3.9 and 3.10 describe the characteristic of the filter used while figure 3.11 illustrates how the harmonic oscillations in figure 3.8 are filtered by the discrete band pass filters.

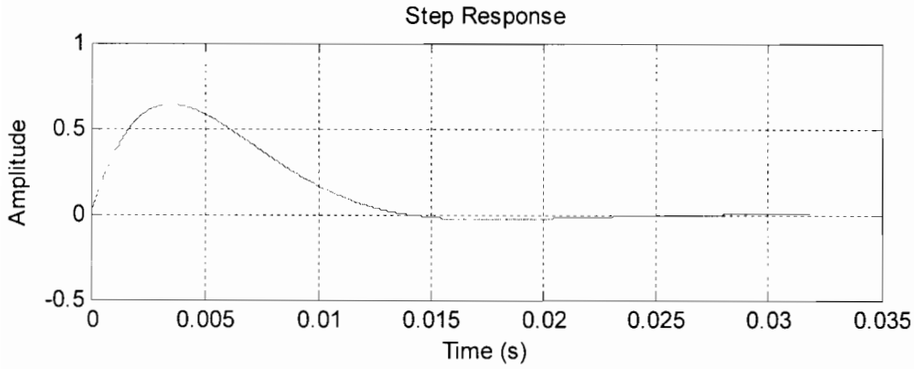

Figure 3-9: Step response of second order discrete filter

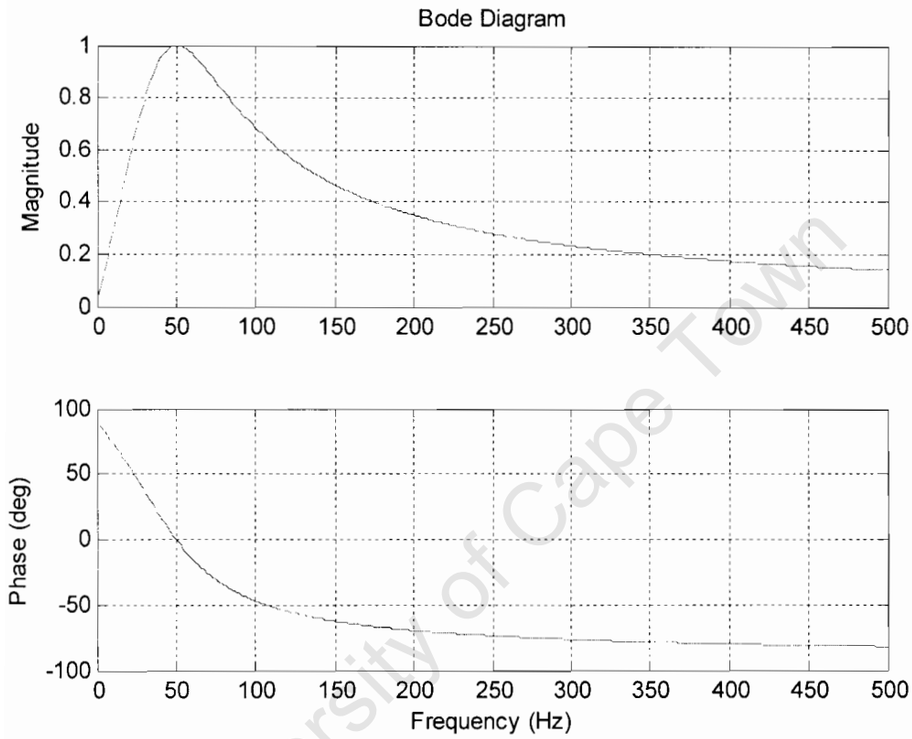

Figure 3-10: Bode diagram for second order discrete filter

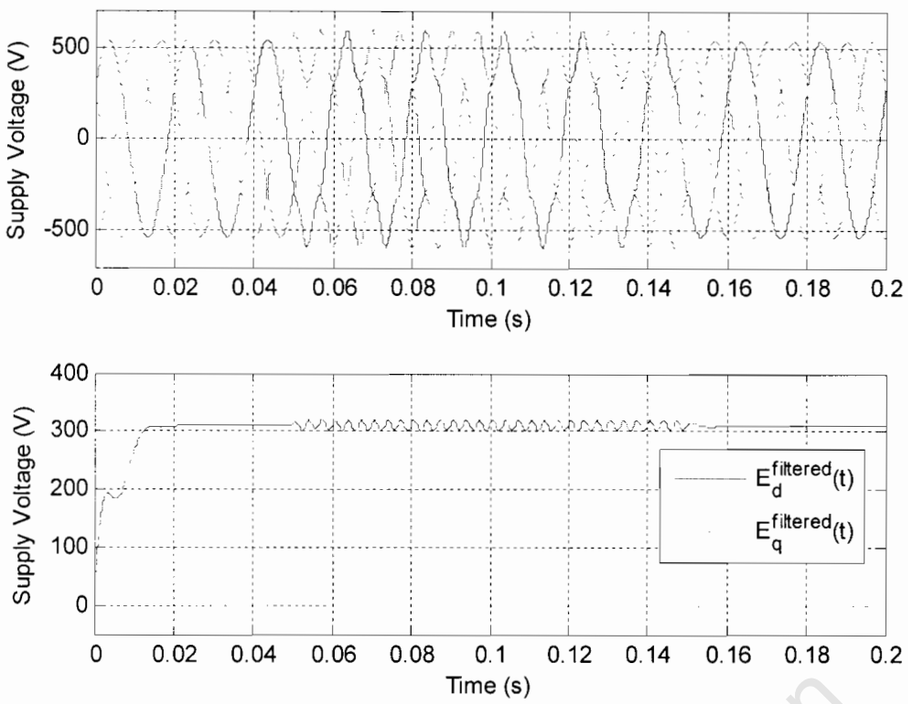

Figure 3-11: Filtering of harmonics illustrated in d-q voltage components

3.2 Unbalanced Voltage Dip or Swell

This section describes how the compensation algorithm from section 3.1.3 can be modified to include mitigation of unbalanced disturbances as well. Unbalanced three phase voltages can be represented as two rotating vectors in the α-β stationary frame called the positive and the negative sequence voltages. These two sequences can be extracted in the stationary frame and controlled separately to accomplish compensation of unbalanced disturbances [26-30].

3.2.1 Transformation of Unbalanced Voltages into Synchronous Frame

When the three voltage phases are unequal, the system is said to be unbalanced. In that situation, the locus drawn by the space vector in the α-β stationary frame becomes an ellipse and the supply vector describing that locus is no longer equal to the positive

sequence voltage vector [42]. This outcome is due to the presence of a negative sequence voltage. The negative sequence voltage vector rotates at the same speed ω as the positive sequence voltage but in opposite direction, i.e. in a clockwise direction. The two sequences describe two balanced line to line voltages. The existence of both sequences at the same time is the result of the unbalance in the system. The positive component is the useful one while the negative component is undesirable [9]. They both add up to form an ellipse as shown in figure 3.12.

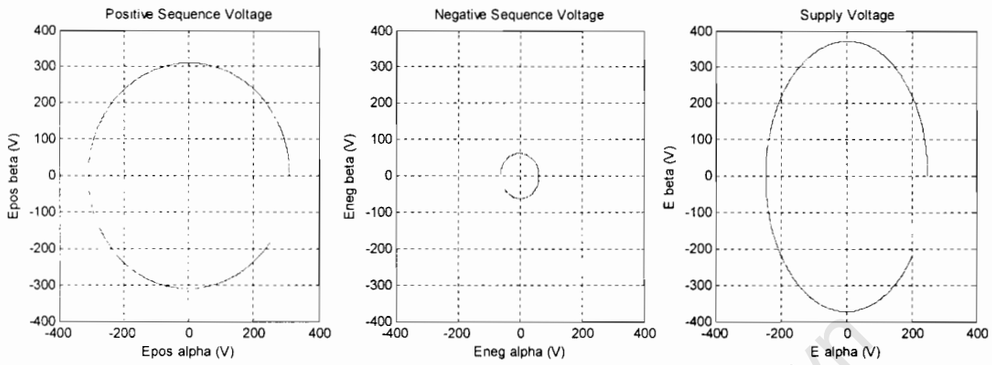

Figure 3-12: Positive and Negative sequence voltages and the Supply voltage

If the supply space vector is transformed to the synchronous d-q frame using the supply angle θ(t), the q component is still zero but the d component is no longer dc. As mentioned in section 3.1.3, the d-component has a sine wave constituent at twice the line frequency superimposed on the dc component. The dc component is the magnitude of the positive sequence voltage while the magnitude of the sine waveform is equal to the magnitude negative sequence component.

As already mentioned, the negative sequence voltage is undesirable. To balance an unbalanced system, the negative system component must be removed. The magnitude and phase of the negative sequence voltage must therefore be extracted from the supply voltage. Similarly, the positive sequence component must be extracted so as to obtain a clean dc signal in the d-q synchronous frame.

The decomposition of the supply voltage into positive and negative sequence components is performed in the α-β stationary frame. By using instantaneous values and stored values taken at a quarter cycles earlier, the two sequences are extracted

using equ.3.6 [31]. The extraction of both sequences from an unbalanced supply voltage in the stationary frame is simulated and illustrated in figure 3.13.

$$
\begin{aligned}
\underline{E}^{pos}_{\alpha}(t) &= \frac{\underline{E}_{\alpha}(t) - \underline{E}_{\beta}(t-\frac{T}{4})}{2} \\
\underline{E}^{pos}_{\beta}(t) &= \frac{\underline{E}_{\alpha}(t-\frac{T}{4}) + \underline{E}_{\beta}(t)}{2} \\
\underline{E}^{neg}_{\alpha}(t) &= \frac{\underline{E}_{\alpha}(t) + \underline{E}_{\beta}(t-\frac{T}{4})}{2} \\
\underline{E}^{neg}_{\beta}(t) &= \frac{\underline{E}_{\beta}(t) - \underline{E}_{\alpha}(t-\frac{T}{4})}{2}
\end{aligned}
\qquad (3.5)
$$

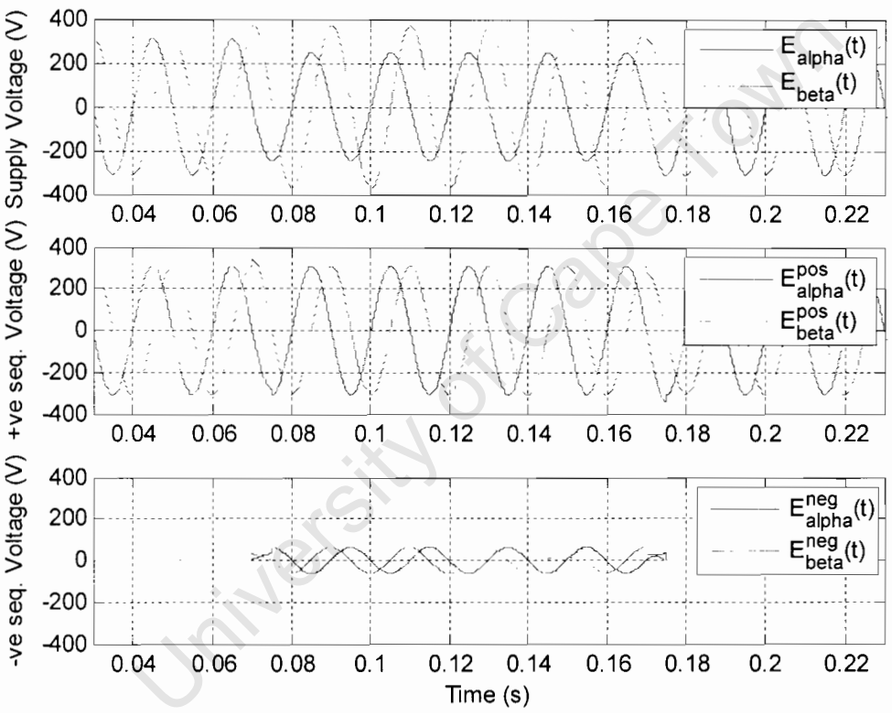

Figure 3-13: Stationary frame components of supply and +ve and -ve seq. voltages

3.2.2 Positive and Negative Sequence Voltage Controller

Once the two sequence voltages have been separated, two controllers are designed to balance and regulate voltages on the load side. The first controller ensures that the negative sequence component of the supply voltage is removed while the second controller forces the positive sequence voltage to track its reference set point at 311V. To summarize, the control algorithm must achieve two goals:

1. Remove the negative sequence voltage from the unbalanced supply
2. Ensure that the positive sequence voltage tracks its reference at 311V

The same positive sequence controller developed in 3.1.2 is used. The only difference here is that the positive sequence voltage must first be extracted from the voltage supply in the stationary frame before being transformed to the d-q synchronous frame so that a clean dc measurement of the phase supply voltage is obtained. Angle $\theta(t) = \beta(t)$ cannot be used for the transformation because $\beta(t)$ is affected by the negative sequence voltage. In fact, the supply voltage, $\beta(t)$, is no longer equal to the positive sequence voltage as it includes a negative sequence voltage. It will be affected by the phase and magnitude of the negative sequence voltage. Figure 3.14 and 3.15 demonstrates how $\beta(t)$ is affected in the presence of a negative sequence voltage. In both figures, a negative sequence voltage is added to a balanced system of voltages at time t=0.02s. In figure 3.14, the phase of $\beta(t)$ is not affected since the negative sequence voltage present is in phase with the positive sequence voltage. However, a clear distortion is visible. Both graphs are results of simulations performed in Matlab-Simulink.

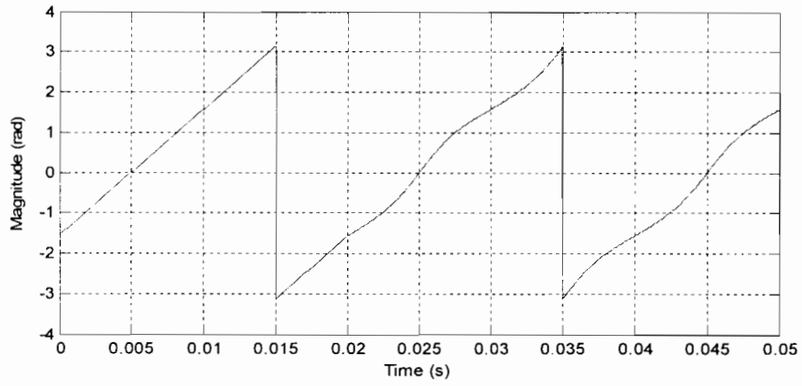

Figure 3-14: Distortion in supply angle due to negative sequence voltage

On the other hand, in figure 3.15, both a distortion and a phase shift are observed at 0.02s since the negative sequence voltage is not in phase with the positive sequence voltage.

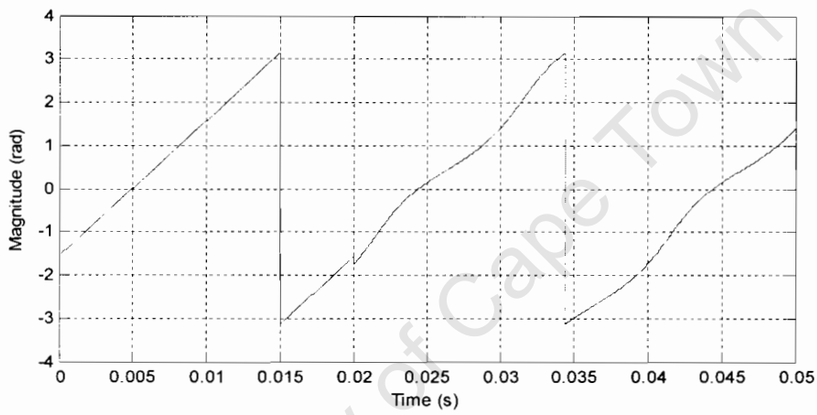

Figure 3-15: Distortion and phase shift in supply angle due to neg. sequence voltage

As a result, the positive sequence voltage angle, $\beta^{pos}(t)$, is now used instead of angle $\beta(t)$. $\beta^{pos}(t)$ is calculated using equ.3.6. A new angle angle, $\theta_p(t)$, is now used for the Park Transformation (equ.3.2) and set equal to $\beta^{pos}(t)$ to lock the positive sequence supply voltage vector, $\mathbf{E}^{pos}$ to the d-axis as described in section 3.1.1.

$$\theta_p(t) = B^{pos}(t) = arc\tan\left(\frac{E^{pos}{}_{\beta}(t)}{E^{pos}{}_{\alpha}(t)}\right) \qquad (3.6)$$

The supply and positive sequence angles are illustrated in figure 3.16 attained from simulations in Matlab-Simulink.

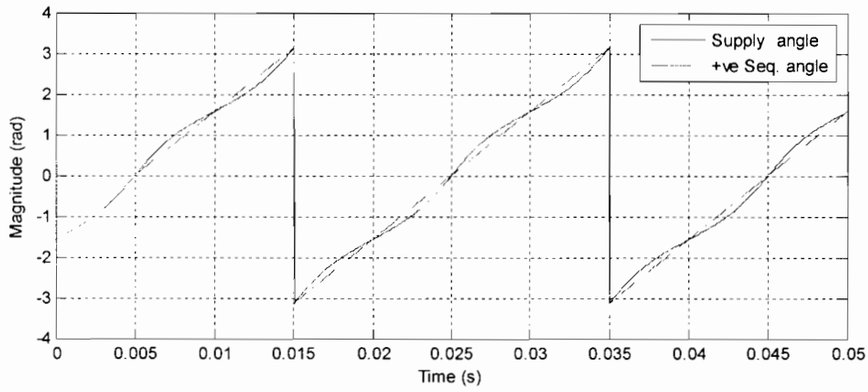

Figure 3-16: Supply and Positive sequence voltage angles

Once $\beta^{pos}(t)$ has been processed, the d-q components of the positive sequence voltage are found. As the d-axis is locked to the positive sequence voltage, the q-component, $E^{pos}{}_q(t)$, is zero and the d-component, $E^{pos}{}_d(t)$, is a maximum equal to the magnitude of the positive sequence voltage. A delay of a quarter cycles (5ms) occurs when extracting the positive sequence voltage components. This concept is shown in figure 3.17 which is obtained from a Matlab-Simulink simulation.

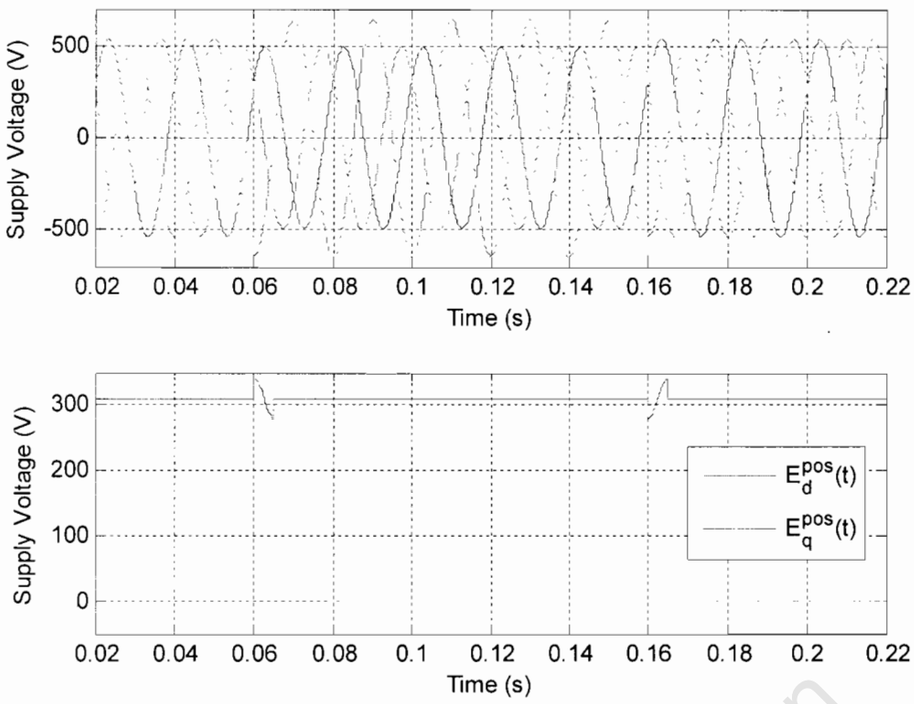

Figure 3-17: DC representation of unbalanced supply

Similarly, the positive sequence voltage of the load voltage is extracted and $V^{pos}{}_d(t)$ calculated in the same way that $E^{pos}{}_d(t)$ is found. This step is necessary as any unbalance present in the supply voltage will also be present on the load side before the mitigation device is switched on.

To obtain a balance system, the negative sequence of the supply voltage must be removed. This removal is achieved by injecting the negative of the negative sequence through the series transformers. Thus, the α-β components of the negative sequence extracted from the supply voltage (equ.3.6) are added to the α-β components of the positive sequence and fed to the SVPWM algorithm. Similarly to the positive sequence voltage correction, a constant angle, $-\delta$, is added to $\theta_n(t)$ which is equal to the negative sequence angle $\beta^{neg}(t)$ (refer equ.3.7), to cancel the effect of the filter and transformer combination on the negative sequence.

$$\theta_n(t) = B^{neg}(t) = arc\tan\left(\frac{E^{neg}{}_{\beta}(t)}{E^{neg}{}_{\alpha}(t)}\right) \qquad (3.7)$$

The new algorithm for compensation of unbalanced disturbances is shown in figure 3.18.

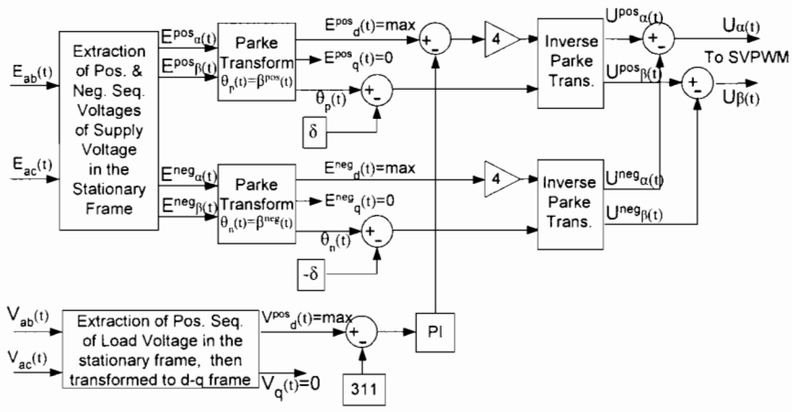

Figure 3-18: Schematic of Pos. & Neg. Sequence voltages controllers

This algorithm is designed for a purely sinusoidal supply. As discussed in section 3.1.3, in the presence of harmonics, the d-component, $E_d(t)$, includes oscillations at frequencies dependent on the harmonic order. These harmonics also affect the positive and negative sequence voltage as well as the positive and negative sequence angles. These harmonics are also present in the voltage at the load side before the mitigation device is switched on and will affect $V^{pos}{}_d(t)$. As in section 3.1.3, the calculated α-β voltage components of the supply and load voltages can be filtered using appropriate band pass filters to test the efficiency of the controller. Again, the response of the system will be delayed due to the presence of the filters.

3.3 Low order Harmonics

In this section, a separate algorithm is designed to measure balanced and unbalanced low order harmonics in the supply and mitigate them. Low order harmonics in a three

phase system can be detected and isolated from each other in different synchronous frames [28, 30]. This new algorithm is then combined to the algorithm from section 3.2 to obtain a system that mitigates balanced and unbalanced voltage dips and swells as well as low order voltage harmonics.

3.3.1 Detection and Mitigation of Low Order Harmonics

The low order harmonics usually present in three phase systems are the 5^{th}, 7^{th}, 11^{th} and 13^{th} [28]. Harmonics of the order n = 3k, k=1, 2, 3… will not exist in a three wire system. Thus only harmonics of the order n=6k+1 and n=6k-1 will exist [43]. Harmonics in a three phase system will rotate differently when transformed to the α-β stationary frame depending on the harmonic number. As already mentioned, the fundamental positive sequence voltage will rotate at speed ω anticlockwise. On the other hand, the 5^{th} harmonic will rotate clockwise at a speed $5.\omega$ while the 7^{th} harmonic will rotate anticlockwise at a speed $7.\omega$ [43]. These phenomena are illustrated by figure 3.19.

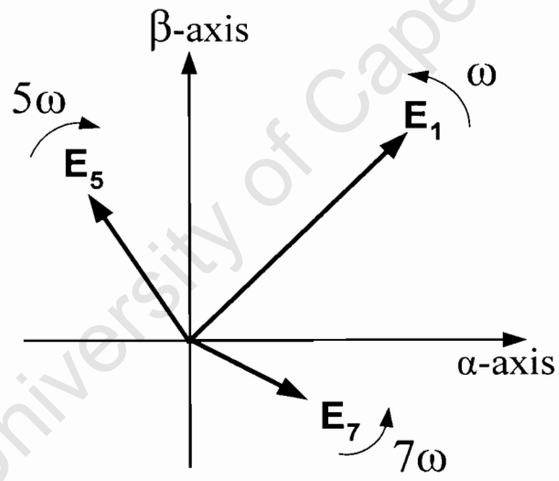

Figure 3-19: Direction of different harmonics in stationary frame

Harmonics of the order n=6k+1 will rotate in the positive anticlockwise direction while harmonics of the order n=6k-1 will rotate in the negative clockwise direction [43]. This pattern holds in the case of balanced harmonics. For unbalanced harmonics,

there will be two vectors rotating in opposite direction for each harmonic order (figure 3.20) as it is the case when the fundamental is unbalanced (giving rise to two vectors, the positive and the negative sequence voltages) [28].

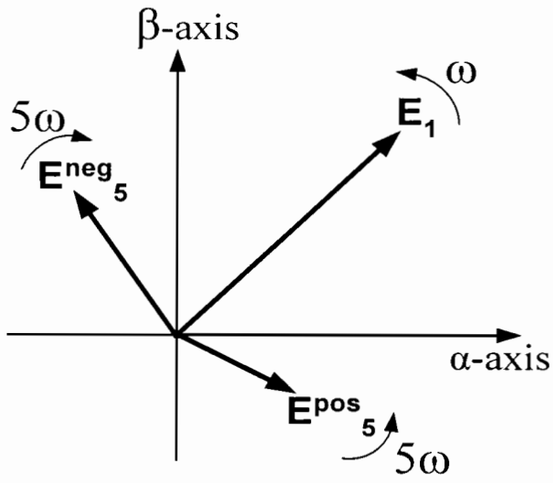

Figure 3-20: Unbalanced 5th harmonic vectors rotating in opposite direction

Consider a harmonic n=6k+1 that rotates at speed nω in the positive direction. If it is transformed to a synchronous frame, called the nd-q, which rotates at speed nω in the positive direction, the vector will appear as a dc component [28]. The positive sequence voltage angle, $\beta^{pos}(t) = \omega t$, is amplified by the factor 'n' and used for the transformation. However, before processing the angle, the two α-β stationary frame components of the positive sequence components are first filtered using band pass filters. This filtering is needed to remove the distortion caused by the harmonics. This process is illustrated in figure 3.21 where the supply contains 10% of 11th order harmonic.

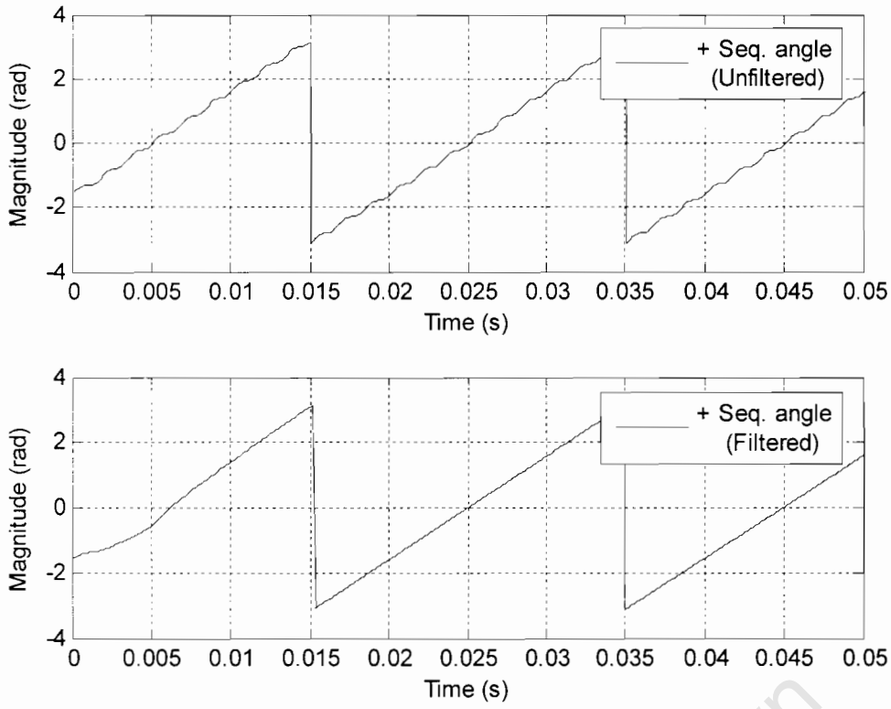

Figure 3-21: Pos. seq. angle obtained from unfiltered & filtered α-β pos. seq. components

If that harmonic is unbalanced, the second vector, rotating at the same speed nω in the negative direction will appear as rotating at double the frequency (hence even) when transformed to the nd-q synchronous frame [28]. All other harmonics including the fundamental will also appear as vectors rotating at different speeds. Because n is always odd (n = 1, 6k+1 or 6k-1), the fundamental and all the other harmonics will rotate at multiples of double the speed of the frame when transformed to the nd-q synchronous frame, i.e. with an even angular frequency [28]. They will thus appear as oscillations of various frequencies (even) superimposed on the dc representation of the $(6k+1)^{th}$ harmonic in the nd-q reference frame. Therefore, by averaging over one half of the fundamental component frequency, i.e. 50Hz, the $(6k+1)^{th}$ harmonic will be isolated as all the other harmonics will be cancelled [28]. The d and q components give the magnitude and phase of that harmonic with respect to the fundamental positive sequence voltage. Similarly, the negative sequence voltage of that harmonic can be isolated in the -nd-q synchronous frame which rotates in opposite direction to the nd-q frame [28]. The procedure is illustrated in figure 3.22.

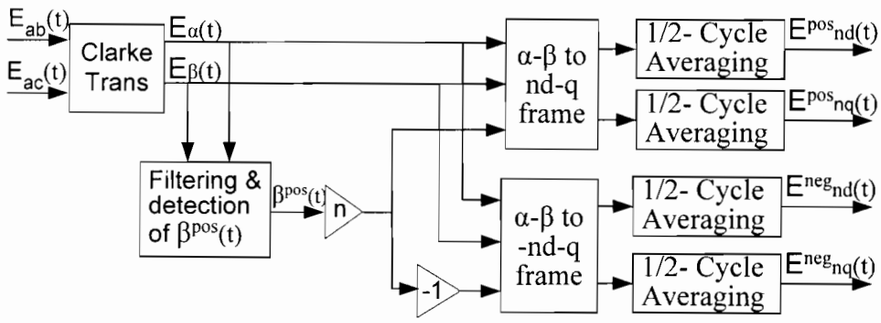

Figure 3-22: Algorithm used to isolate the nth order harmonic

The signals before and after the half-cycle averaging block are illustrated in Figure 3.23. This diagram shows the results obtained with a simulated supply voltage including a 10% unbalanced 5th harmonic (10% of positive and negative 5th harmonic voltage) in phase with the fundamental.

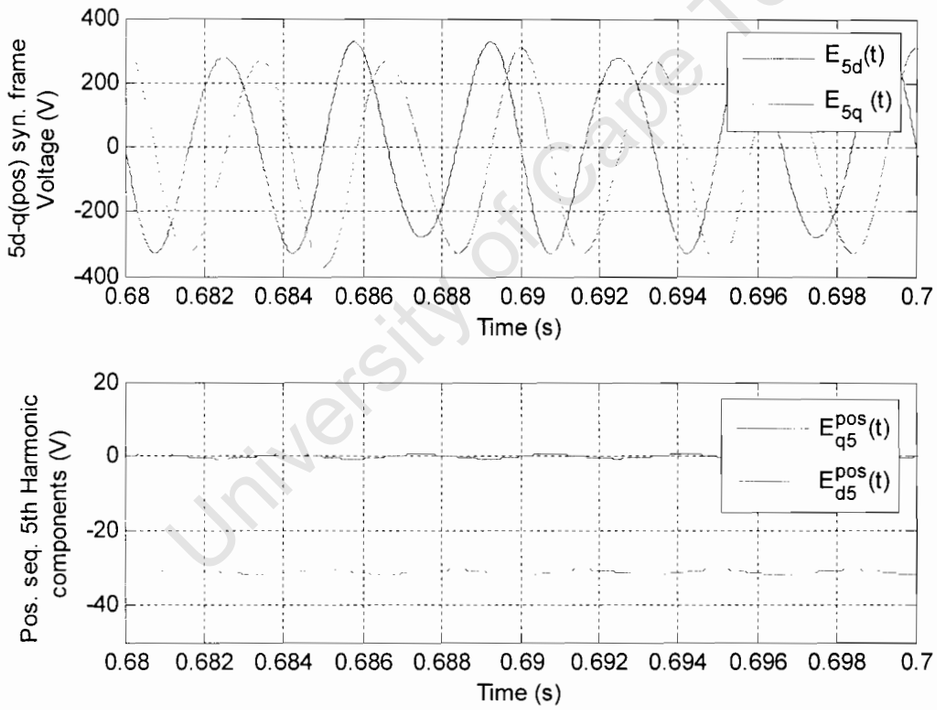

Figure 3-23: Detection of the Pos. seq. 5th harmonic in the 5d-q (pos) syn. frame

Once the d-q components of the n^{th} order harmonic have been found, they are transformed back to the α-β stationary frame using the angles $n\beta^{pos}(t)$ or $-n\beta^{pos}(t)$ which were initially used to detect them in the d-q synchronous frame. The complete process is shown in figure 3.24.

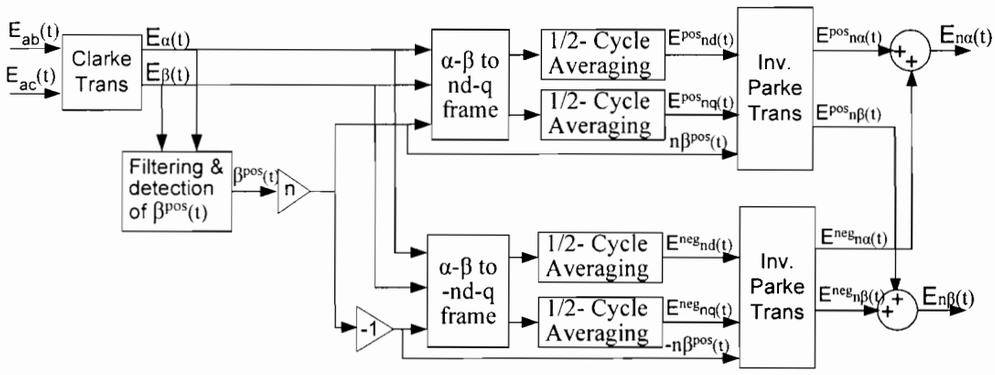

Figure 3-24: Extraction of the α-β components of the n^{th} harmonic

However, $E_{n\alpha}(t)$ and $E_{n\beta}(t)$ can not be fed to the SVPWM block to be injected by the inverter for mitigation. This constraint arises because the effect of the filter and transformers at the output of the inverter has not been taken into account yet. In fact, the d-q components must first be amplified by a factor G(n), which will differ for each harmonic order 'n'. This factor takes into account the stepping down ratio of the transformers as well as the effect of the combination of the filter and transformer on the harmonic. Similarly, an angle, λ(n), is inserted to cancel the phase shift caused by the LPF and transformers on the harmonic. The d-q components are then transformed back to the α-β stationary frame using the angles $(n\beta^{pos}(t) - \lambda(n))$ and $(-n\beta^{pos}(t) - -\lambda(n))$ to obtain $E_{n\alpha}(t)^*$ and $E_{n\beta}(t)^*$, the modified α-β components necessary to achieve proper mitigation of the harmonics. The two factors G(n) and λ(n) are estimated by producing the different harmonics using the inverter and measuring the effect of the filter on them. Accurate values for G(n) and λ(n) can then be established when the mitigation device is in operation by adjusting these two factors until maximum mitigation of the detected harmonics is achieved. The detected harmonics can now be removed from the system using the series transformers. This mitigation is achieved by feeding the α-β stationary frame harmonics components to the SVPWM technique block.

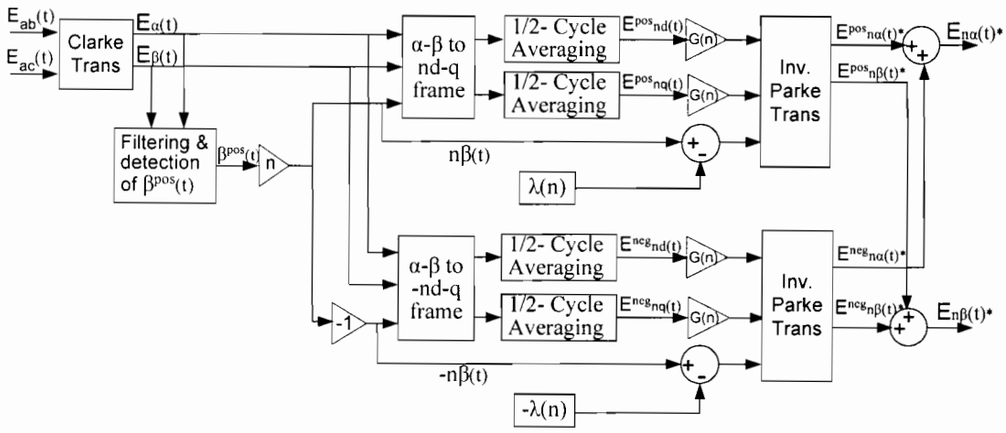

Figure 3-25: Extraction of the modified α-β components of the n^{th} order harmonic

Figure 3.25 shows a general schematic for the detection and mitigation of the n^{th} order harmonic. Indeed, this method can be used to detect all harmonic orders. Note that this algorithm involves a delay of one half-period at the system frequency and is thus subject to twice the time lag of the procedure to extract the positive and negative sequence voltage components. However, the speed of response is not a major concern as harmonics mitigation happens in steady state [28].

3.3.2 Combining the two algorithms

In this section, the harmonic mitigation algorithm is combined with the positive and negative sequences controllers to obtain a final system that is capable of mitigating balanced and unbalanced dips, swells and voltage harmonics. As discussed in section 3.3.1, harmonics present in the supply can be isolated and detected in different synchronous frames. Once $E_{n\alpha}(t)$ and $E_{n\beta}(t)$ have been calculated, they can be subtracted from the supply voltage α-β components $E_\alpha(t)$ and $E_\beta(t)$ to obtain the fundamental voltage free of all the harmonics. This subtraction is simulated in Matlab-Simulink and the result is illustrated in figure 3.26. The fundamental of the supply voltage is then fed to the positive and negative sequences controllers. This step solves all the problems caused by harmonics described in sections 3.1.3 and 3.2.2

making the algorithms described in these sections operational in the presence of harmonics without the need to filter voltages.

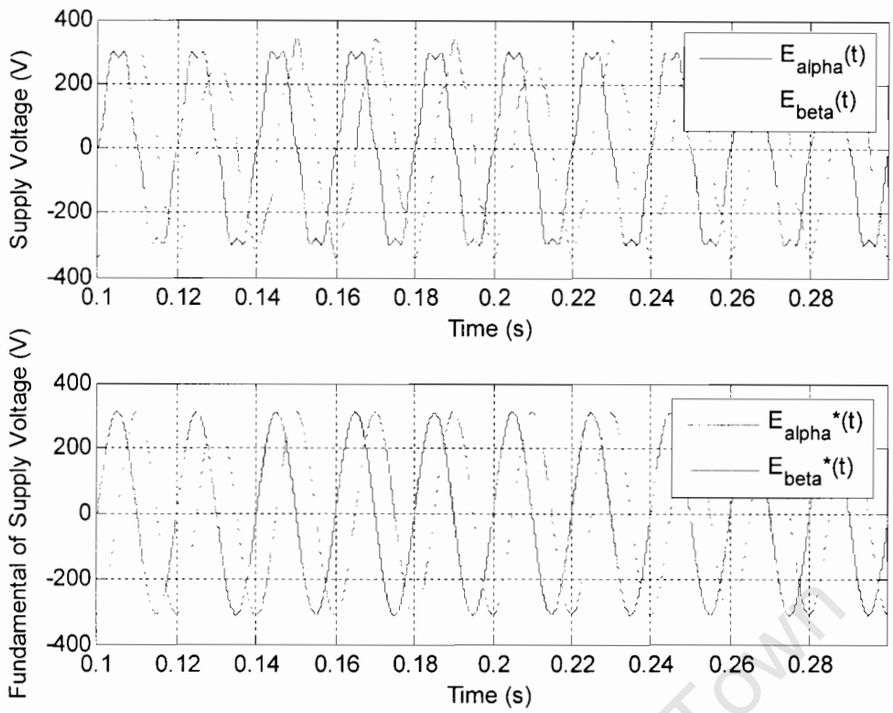

Figure 3-26: Subtraction of harmonics from supply voltage in α-β stationary frame

The modified $E_{n\alpha}(t)^*$ and $E_{n\beta}(t)^*$ α-β harmonic components are also required to mitigate the harmonics detected. Thus, the algorithms of figure 3.24 and figure 3.25 are combined to obtain both the exact α-β components and the modified α-β components of the detected harmonics, $E_{n\alpha}(t)$ and $E_{n\beta}(t)$, and $E_{n\alpha}(t)^*$ and $E_{n\beta}(t)^*$ respectively. The modified algorithm is illustrated in figure 3.27.

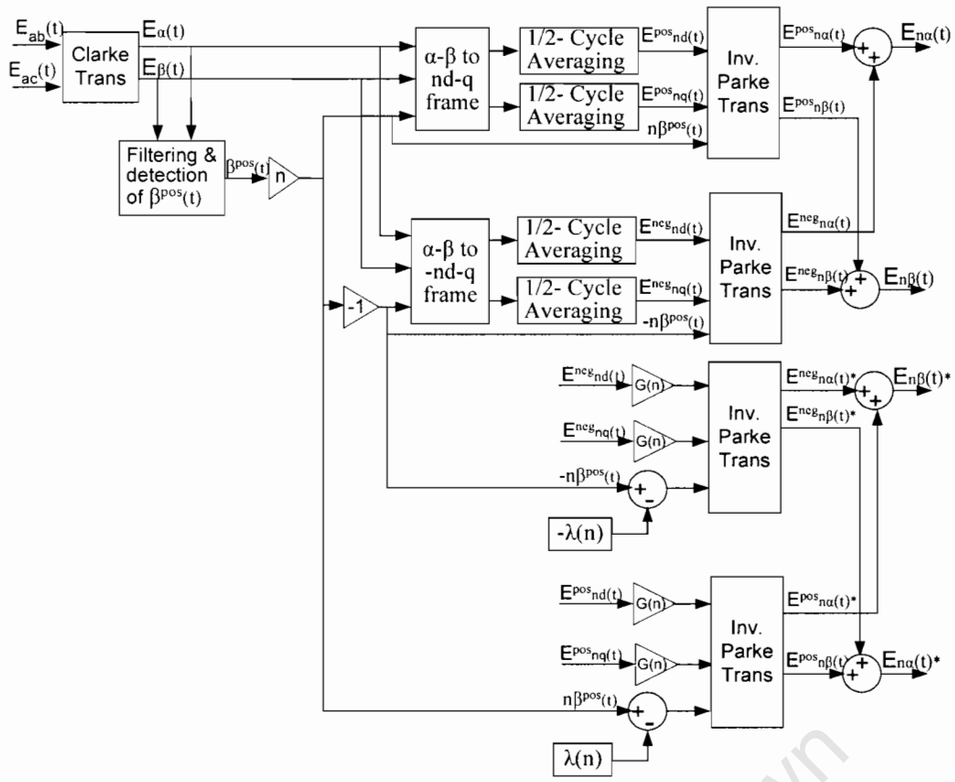

Figure 3-27: Modified algorithm to obtain Enα*, Enβ*, Enα and Enβ

The exact α-β components of the different harmonics are used to obtain the fundamental of the supply voltage while the modified α-β components of these harmonics are added to the positive and negative sequence voltage α-β components, which must be injected on the load side to mitigate any disturbance present. Together they are fed to the SVPWM algorithm to be subtracted from the supply voltage using the series inverter and the three single phase transformers.

The final control schematic is shown in figure 3-28. Note that the blocks called n^{th} Harmonic Detection represent the algorithm illustrated in figure 3-27. This block can be used to mitigate any n^{th} harmonic.

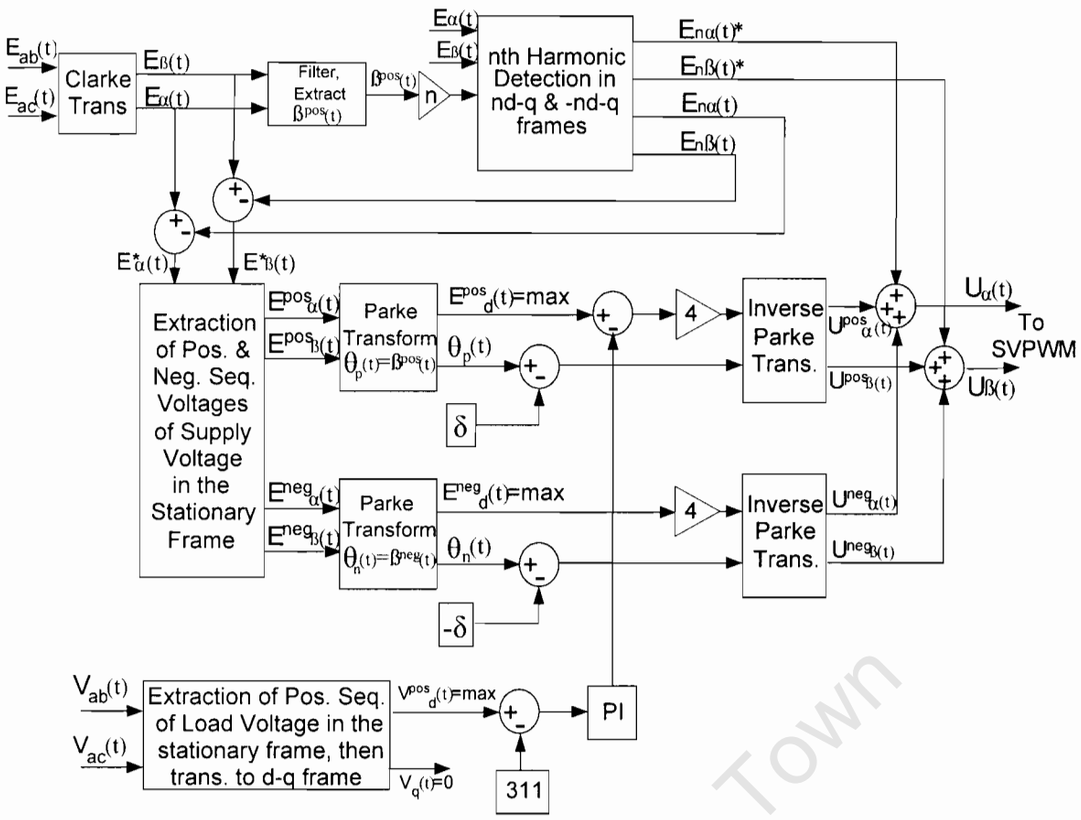

Figure 3-28: Schematic of the final algorithm including mitigation of harmonics

4 EXPERIMENTAL SETUP – HARDWARE & SOFTWARE

4.1 Description of the experimental setup

Fig 4.1 shows the overall schematic of the experimental setup. The picture on the left of the figure illustrates the load, the transformers, the low pass filter and the line inductors at the output of the shunt converter. The picture on the right hand side shows the back to back converter, level shifter circuits and their power supplies, the dSPACE CLP1104 combined Connector/LED Panel and the PC used to control the mitigation device. The control strategies employed are described in Chapter 3. Measured signals from the voltage and current transducers are fed to the dSPACE CLP1104 Combined Connector/LED Panel that act as an interface between the I/O signals and the controller card. All computational tasks are processed by the DS1104 R&D Controller Card which is connected to a PC where all the control is handled.

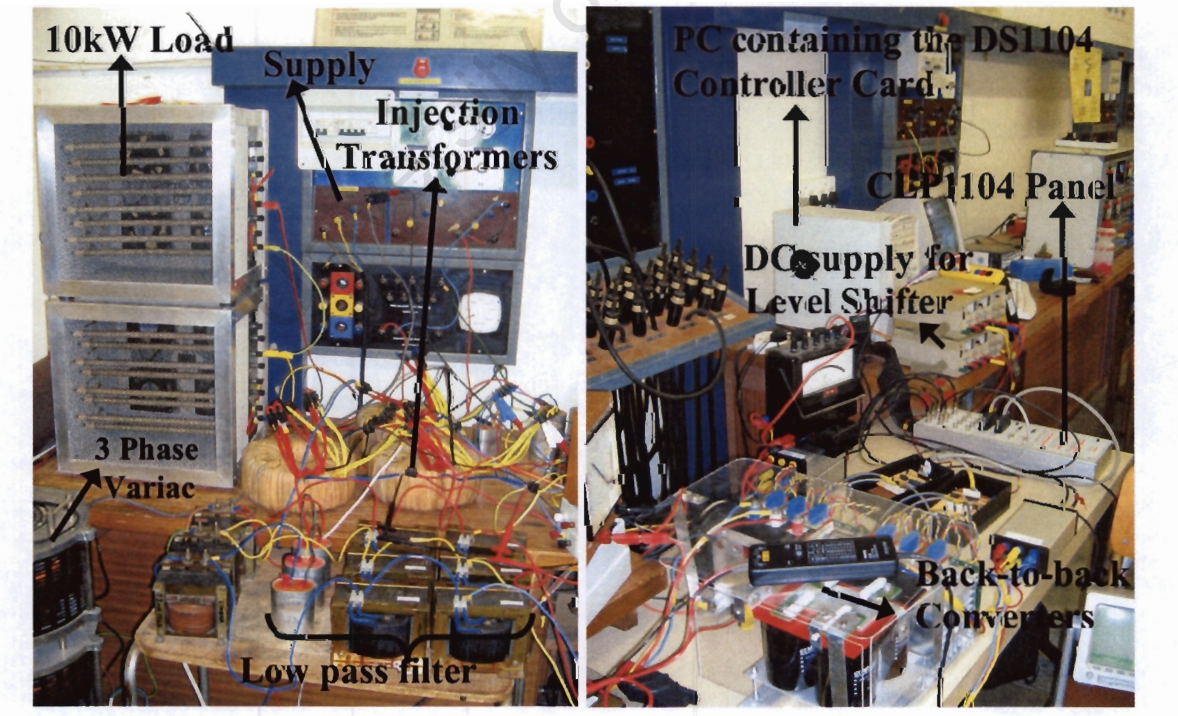

Figure 4-1: Experimental Set up in the Machines Laboratory at UCT

4.2 Hardware Design

In this section, the design of the components that make up the inverter is discussed. The inverter used consists of Semikron insulated gate bipolar transistors (IGBTs). These IGBTs are driven by Semikron drivers, which get their switching signals from the CLP1104 panel via a level shifter and buffer circuit. Finally, the design of LEM modules used for voltage and current measurements is outlined.

4.2.1 Insulated Gate Bipolar Transistors (IGBTs)

The IGBTs used are obtained in pairs in a package called SKM 50GB 123D from Semikron (Appendix B). These semiconductor switches are voltage controlled. They are able to handle larger collector currents than other semiconductor devices such as MOSFETs and therefore have higher power ratings. The ratings of the IGBTs far surpass the rating of the system due to the availability of equipment in the machine's laboratory.

4.2.2 Driver Modules

The driver modules used are the SKHI 22A (Appendix C) from Semikron. Each module drives a pair of IGBT. These devices have a large number of protection schemes to protect both the IGBTs and the controller card. One of the most important features is short circuit protection by monitoring the voltage across the collector and the emitter.

Six driver circuits are built for each module. These driver modules accept -15V (off) and +15V (on) signals and output the turn-off, -6.5V, and turn-on, +14.9V threshold voltages of the IGBTs. However, the output signals from the dSPACE board are 0V (off) and +5V (on). Thus, a level shifter circuit is used to convert the switching signals accordingly. The level shifter circuit outputs pwm signals to the three driver modules of the converter. Thus, two of these circuits are built for the two converters.

Figure 4.2 illustrates the six driver modules and the two level shifter circuits, one for each converter. This circuit is shown in Appendix D.

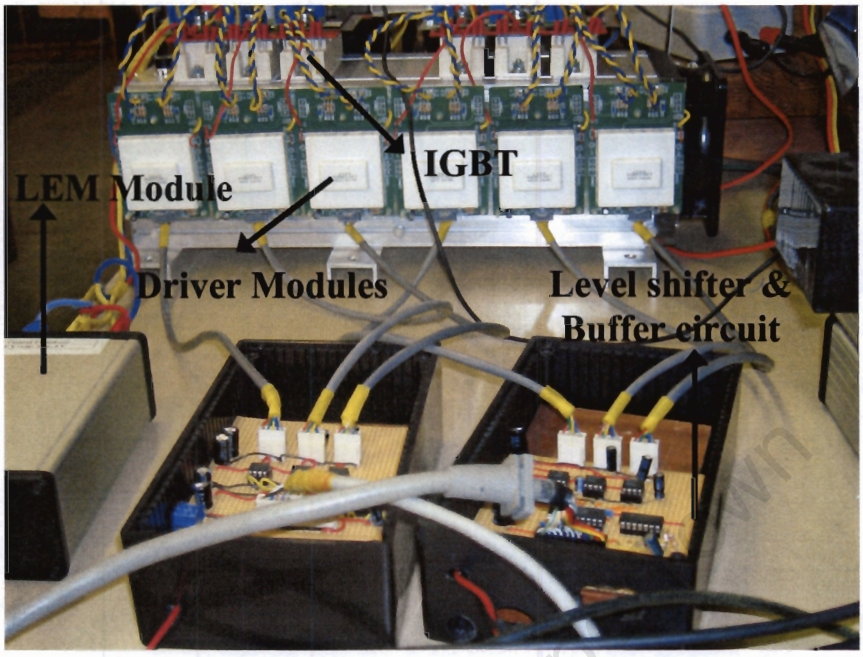

Figure 4-2: Driver modules and Level shifter circuits

The values of the resistors and capacitors needed are calculated from equations given in the SKHI 22A datasheet (Appendix C). These calculations are shown below:

R_{CE}:

This resistor sets the reference for V_{CE} monitoring. The data sheet recommends a value of 5V for the IGBT used in this thesis project. However, the closest value which can be obtained using the available resistors is 5.6V. Thus, if this threshold is exceeded, the driver will trigger and error and stop the IGBT.

From equation (4.1) obtained from the datasheet, R_{CE} is calculated to be 27kΩ.

$$V_{CEstat}(V) = \frac{10.R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1.4 \qquad (4.1)$$

Note also that no resistance is used for R_{VCE} when driving 1200V IGBT.

C_{CE}:

This capacitor is calculated using equations (4.2) and (4.3) below extracted from the datasheet. According to the datasheet, this capacitor needs to be smaller than 2.7nF.

$$t_{min} = \tau_{CE}.\ln[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)}] \qquad (4.2)$$

$$\tau_{CE}(\mu s) = C_{CE}(nF).\frac{10.R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} \qquad (4.3)$$

Using the above equations, and the recommended value of 1.45us for t_{min} as well as the calculated value of 27kΩ for R_{CE}, the value calculated for C_{CE} is 0.33nF.

R_{ON} & R_{OFF}:

These resistors increase the turn-on time and turn-off time and power dissipation. The datasheet recommends a value > 3 Ω. Higher resistance increases both turn-on time and turn-off time, and power dissipation. R_{ON} and R_{OFF} are both chosen to be 3.3Ω.

4.2.3 The LEM Modules

LEM modules are special transducers that measure high currents and voltages and output a low voltage signal. These transducers offer many advantages. Some of these are:

- Very good linearity
- Low temperature drift
- Excellent accuracy

In this thesis, the line-to-line rms voltage is rated at 380V but can vary between 300V and 420V in the case of a dip or swell. The current is dependent on the load connected to the supply. In this project, a star-connected 10kW load is used. Thus, the line currents are 15A rms for rated voltage but will vary between 14 and 20A in the case of voltage dips or swells. However, because the current measurements are made on the shunt converter side, only a quarter of the load current flows because of the

transformer turns ratio. Thus, only up to 5A flows. Moreover, the common dc bus voltage of the converters must be measured and is fixed at 600V. With knowledge of the magnitude of the currents and voltages to be measured, LEM modules are selected. Thus, the LV 25-P and the LA 25-NP are used as voltage and current transducers respectively. Their respective datasheets are attached in Appendix E.

Both transducers require a +/- 15V supply voltage as well as external resistors to determine the ratio between the input signal and the output signal. This ratio is determined by the magnitude of the maximum current or voltage that must be measured on the primary side of the LEM module as well as by the magnitude of the desired output voltages on the secondary side. The output signals must be restricted to +/- 10V, which is the maximum allowable voltage of the ADC of the DS 1104 Controller card.

LV 25-P:

In this project, six voltage measurements are made. Five of them are ac line-to-line voltage measurements while the sixth one is a dc voltage measurement. For all of them, the LV 25-P is used. However, different resistor values are used for the ac and dc measurements. Figure 4.3 illustrates a schematic of the LV 25-P device as well as the external connections to the voltage supply and necessary resistances.

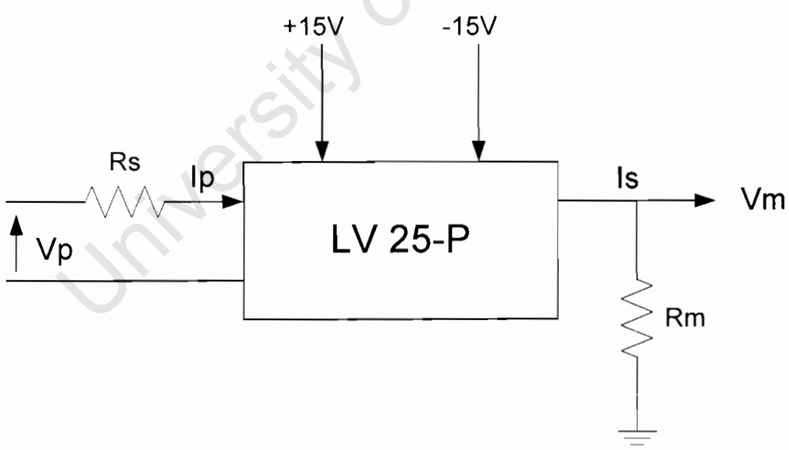

Figure 4-3: Schematic of the LV 25-P with all the external connections

The calculation of R_s and R_m are as follows:

1. The minimum value of R_s required is calculated using equ.4.4 and equ.4.5 and then a value for R_s is chosen accordingly.

$$R_s = \frac{V_p}{I_p} \qquad (4.4)$$

$$I_{p\,\max} = \pm 14mA \qquad (4.5)$$

2. Using equ.4.4, I_p is calculated and is used to calculate I_s using equ.4.7. Finally, R_m is found using equ.4.6.

$$R_m = \frac{V_m}{I_s} \qquad (4.6)$$

$$I_s = \frac{2500}{1000} \times I_p \qquad (4.7)$$

Table 4.1 illustrates the different component values calculated and chosen for the LV25-P module. Note that R_s and V_m are chosen to be well inside the allowable range so that the ADC of the DS1104 Controller card remains protected in the unlikely event of a fault.

Table 4-1: Values of external resistors chosen for LV 25-P voltage transducer

Measurements	Vp max (V)	Ip max (mA)	Rs min (Kohms)	Rp chosen (Kohms)	Ip (mA)	Is (mA)	Vm (V)	Rm (ohms)	RATIO
DC Voltage	700	14	50	81	8.64	21.6	7.6	352	94
AC Voltage	420	14	30	94	4.47	11.2	4.42	390	95

LA 25-NP:

In this project, two line currents measurements are made using the LA 25-NP. The transducer induces a current, I_s, in its secondary coil, which is a scaled-down replica of the actual line, I_p, current that flows through its primary coil. The scaling factor is adjusted by connecting the input and output pins of the module in different

combinations as indicated in the datasheet supplied as Appendix E. Figure 4.4 illustrates a schematic of the LV 25-P device as well as the external connections to the voltage supply and necessary resistances.

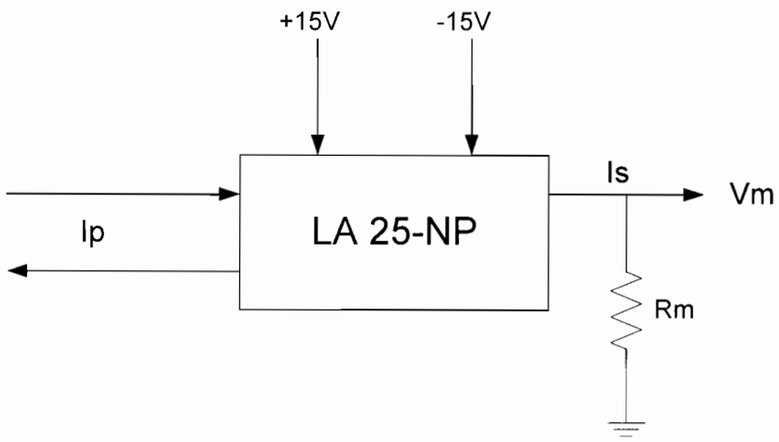

Figure 4-4: Schematic of the LA 25-NP with all the external connections

The calculation of R_m is as follows:

1. A scaling factor, K, is first chosen to make proper use of the ADC input range for good precision. Then, I_s is calculated using equ.4.8

$$I_s = \frac{I_p}{K} \qquad (4.8)$$

2. Using equ.4.9, R_m is chosen so as to obtain a value of V_m that is inside the +/- 10V range of the ADC. According to the datasheet, R_m must lie between 150Ω and 325 Ω.

$$R_m = \frac{V_m}{I_s} \qquad (4.9)$$

Table 4.2 illustrates the values chosen for K and R_m as well as the calculated values of I_p and I_s. V_m is chosen well inside the allowable range to protect the ADC in the unlikely event of a fault.

Table 4-2: Values chosen for K, and Rs for the LA 25-NP current transducer

Measurements	Ip max (A)	K	Is (mA)	Rm chosen (ohms)	Vm (V)	RATIO
Current (A)	10	0.002	20	270	5.4	1.85

4.2.4 The DS1104 R&D Controller Card

The DS1104 R&D Controller Card forms part of the Advanced Control Educational Kit (ACE kit) manufactured by dSPACE. The kit upgrades the PC to a powerful development system for rapid control prototyping [44].

The DS1104 R&D Controller Card, shown in figure 4.5, is slotted into the PC's motherboard. It executes all computational and control tasks for both the series connected inverter and the shunt connected converter.

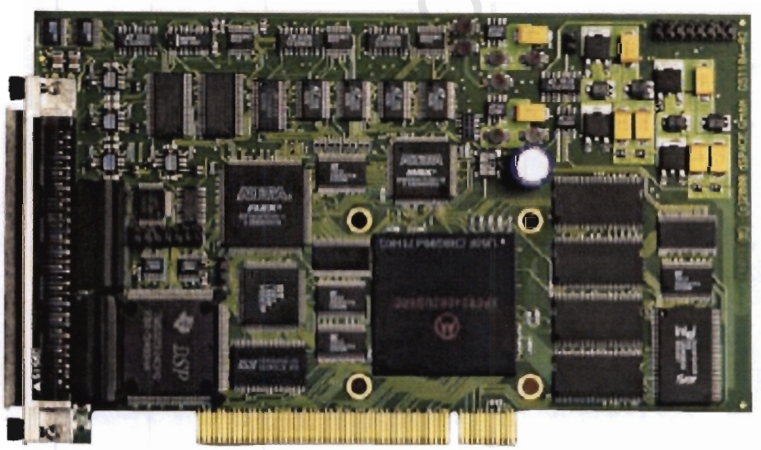

Figure 4-5: The DS1104 R&D Controller Card [44]

Some of the main features of the card include the main processor, a PowerPC603e with a 250MHz CPU clock frequency and a slave DSP from Texas instruments (DSP TMS 320F240) [card]. The card also consists of Digital I/O ports, Slave I/O PWM ports, ADC and DAC channels, an incremental encoder interface and a UART interface. In this thesis, the Slave I/O ports as well as the ADC channels were used. A schematic description of the features input and output ports of the card is given in figure 4.6.

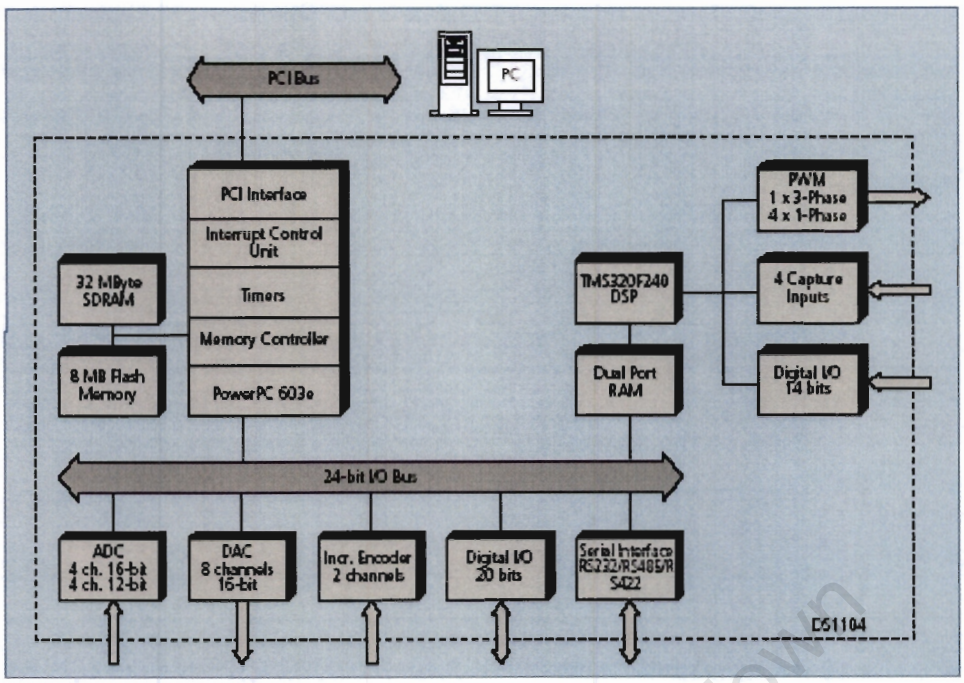

Figure 4-6: Features of the DS1104 R&D Controller Card [44]

The card is programmed in Matlab-Simulink. The Real-Time Interface (RTI) software, which is included in the ACE Kit is the link between the dSPACE Card and the Matlab-Simulink software.

4.2.5 The CLP1104 Combined Connector/LED Panel

The dSPACE CLP1104 combined Connector/LED Panel completes the hardware package of the ACE Kit. Figure 4.7 shows the dSPACE CLP1104 Panel.

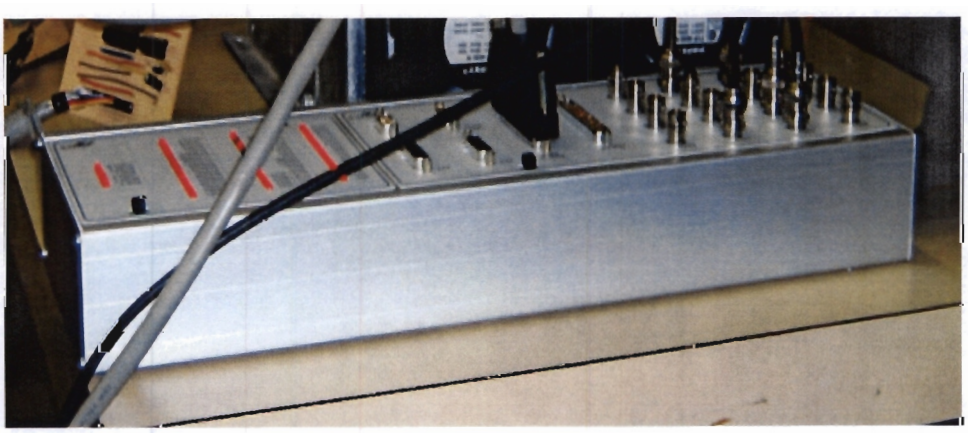

Figure 4-7: CLP1104 Connector/LED Panel

The LED panel on the left of the board indicates the state of the ports and is very useful for debugging. The panel provides different connectors for easy access of each specific port. For example, it allows access to analog signals via BNC connectors and access to digital signals via Sub-D connectors [45].

4.3 Software Design

Three software packages are used in the development and control of the project. These packages are:

(1) Matlab-Simulink
(2) Real-Time Interface (RTI)
(3) ControlDesk

The Real-Time Interface and the Control Desk are the two software packages provided in the ACE Kit.

4.3.1 Matlab-Simulink

Matlab-Simulink is a simulation based software package. All the simulations were performed in Simulink. Simulations are an important part of the whole design process. Different models are built in Simulink to validate the control algorithms derived from theory. As the system consists of two converters controlled independently, the algorithms for the two converters were tested separately. First, the DC bus voltage control for the shunt converter was tested. Then, the DC voltage source used by the series inverter and regulated by the shunt active rectifier was simulated as a pure dc source to simulate the different algorithms for the series converter. The simulated results are shown in Chapter 6. Appendix F show two Simulink models used to simulate the system. The first model is for the DC bus voltage regulation of the shunt converter using the HCC technique. The second one illustrates the complete algorithm of the series converter for regulation, balancing and harmonic mitigation.

Before running simulations in Simulink, careful attention must be given to the choice of the solver as well as the step size because these parameters can affect the simulation results considerably. A fixed Step solver with a step size of 0.00002s was used. Because a frequency of 5 kHz is chosen for the SVPWM switching, a 5 kHz saw tooth carrier signal is needed to obtain the switching signals. Thus, according to the Nyquist theorem, a maximum sample time of 0.0001s (1/2*5kHz) must be used. However, even a step size of 0.0001s is not good enough for acceptable results of the SVPWM algorithm. Thus, the step size was decreased to 0.00002s. Note that such a small step size is not achievable in the real time simulations using the DS1104 controller card. However, the DS1104SL_DSP_PWMSV block available from the DS1104 RTI Library is used to produce 5 kHz-switching signals independent of the step size.

4.3.2 Real–Time Interface

"Real-Time Interface (RTI) is the link between dSPACE hardware and the development software MATLAB/Simulink/Stateflow from The MathWorks. It extends Real-Time Workshop® and Stateflow Coder® (C code generators) for the seamless, automatic implementation of your Simulink and Stateflow models on the systems' real-time hardware" [46].

This software basically translates the Simulink model into equivalent C-code for processing by the main processor allowing for rapid testing of models. The Real-Time Interface also provides I/O modules from the RTI I/O library that connect the Simulink model to the DS1104 Controller Card.

Once the Simulink model has been tested, it has to be prepared for implementation on the real-time hardware. This preparation is done by replacing some of the Simulink blocks with I/O modules from the RTI I/O library. These modules form the interface to the real controlled system and allow real time simulations. All the input and output signals are read using the I/O modules while all the control is performed using the original Simulink blocks. For example, the three-phase voltage source block in the simulations is replaced by ADC RTI blocks, which output actual currents and voltages signals measured by the LEM modules and read by the controller card.

However, the control blocks are left unchanged and are the same as those used in simulations.

Once all the necessary Simulink blocks have been replaced by their corresponding I/O modules, the model is run in Simulink to check for errors. Thereafter, the Simulink model is converted to equivalent C-code by the Real-Time Workshop and downloaded onto the controller card. Appendix G shows the final Simulink RTI model for the final algorithm. The model includes HCC control of the shunt converter as well as the complete control algorithm for the series converter for regulation, balancing and harmonic mitigation.

4.3.3 ControlDesk

"ControlDesk is experiment software for seamless controller development with just one tool. Right from the start of experimentation, ControlDesk performs all the necessary tasks. With ControlDesk installed, you will benefit from using the same experiment environment throughout the various stages" [47].

CopntrolDesk is used to manage real-time experiments. It keeps track of all the data generated during the experiment. In fact, data can be stored and send to Matlab for further computation. Control panels are built in ControlDesk by dragging and dropping components such as displays and sliders included in the Control Desk library. The control panel serves as an interface to the experiment. Using the control panel, measured signals read by the DS1104 Controller Card can be observed and parameters of the controllers can be changed in real time.

Figure 4.8 illustrates the control panel built to manage the experiment. The red buttons are used to switch the two converters. Each converter has an "on" and "off" state. During the "off" state, no IGBTs are activated and no switching takes place. During the "on" state, the IGBTs switch according to the switching signals outputted by the DS1104 Controller Card. The supply and load voltages as well as their d-component, the DC bus voltage and the hysteresis currents are all monitored in the control panel.

Some of the sliders shown are used to insert different gains and phase shifts to the negative sequence voltage component and to the various harmonics to compensate for the effect of the low pass filter and transformers arrangement. These gains and phase shifts are adjusted by visualizing the harmonic spectrum of the load voltage on the 'Qualistar' three phase power quality analyzer.

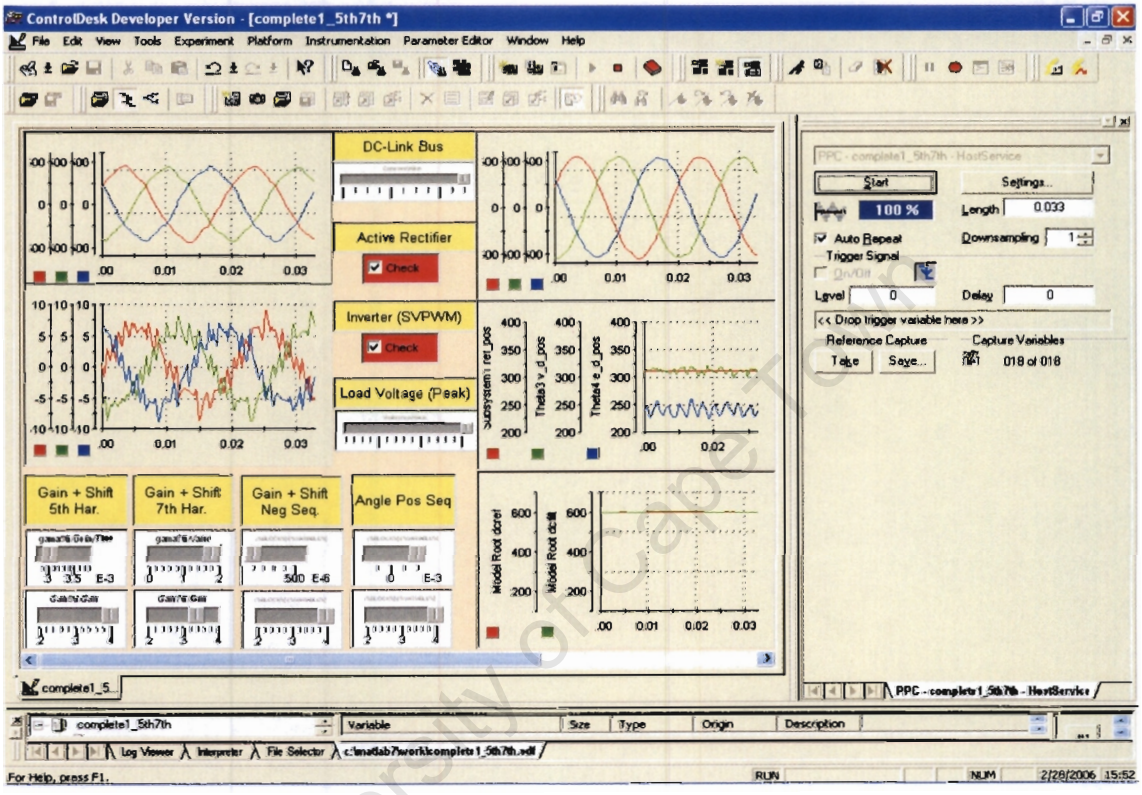

Figure 4-8: Control panel designed to control the mitigation device

5 SIMULATED AND EXPERIMENTAL RESULTS

This chapter discusses the results achieved from the tests carried out on the compensating device. Simulations are first performed to validate the control algorithms derived from theory before being implemented experimentally. The simulations were performed in Matlab-Simulink as described in Chapter 4. All simulation parameters are based on the actual parameters of the components used in the laboratory setup. The experimental results obtained arise from the experimental setup described in section 4.1. For all simulation and experimental results, a load of 10kW is used. Different experiments were performed to test both the HCC technique for DC bus regulation as well as the various controllers presented in chapter 3.

5.1 Positive Sequence Controller

The first experiment is carried out to test the ability of the controller shown in figure 3.5 of section 3.1.2 to regulate a three phase supply voltage. The efficacy of that controller is then compared to its improved version as described in section 3.1.3 and illustrated in figure 3.6. The HCC algorithm for the DC bus voltage regulation of the shunt converter is tested simultaneously. Both controllers as well as the HCC algorithm are tested for balanced dips. The improved controller and the HCC algorithm are also tested for swells as well. A slight modification is made to the two controllers due to the presence of harmonics in the supply. As discussed in section 3.1.3, band pass filters are added to both controllers to filter the supply and load stationary frame α-β components. This modification is essential to test the algorithm because no pure three phase supply is available in the Machines laboratory.

5.1.1 Initial Positive Sequence Controller

This section describes the results obtained when using the initial positive sequence controller shown in figure 3.5 of section 3.1.2 in the event of a balanced dip. The ability of the HCC technique to regulate the DC bus voltage while transferring power

at unity factor is also tested. Both simulated and experimental results are shown for comparison.

As shown by figures 5.1 and 5.2, the shunt converter absorbs more current from the supply when the dip occurs in order to maintain the DC bus voltage at 600V. Power transfer occurs at unity power factor since i_q is 0. Figures 5.3 and 5.4 show that the DC bus is correctly regulated at 600V.

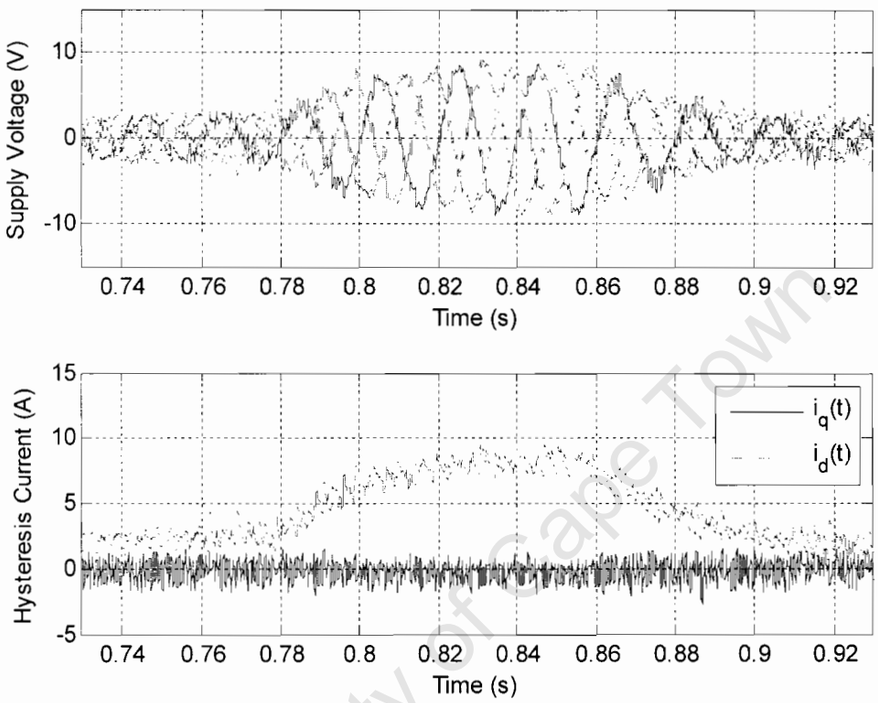

Figure 5-1: Simulated hysteresis currents during a balanced dip

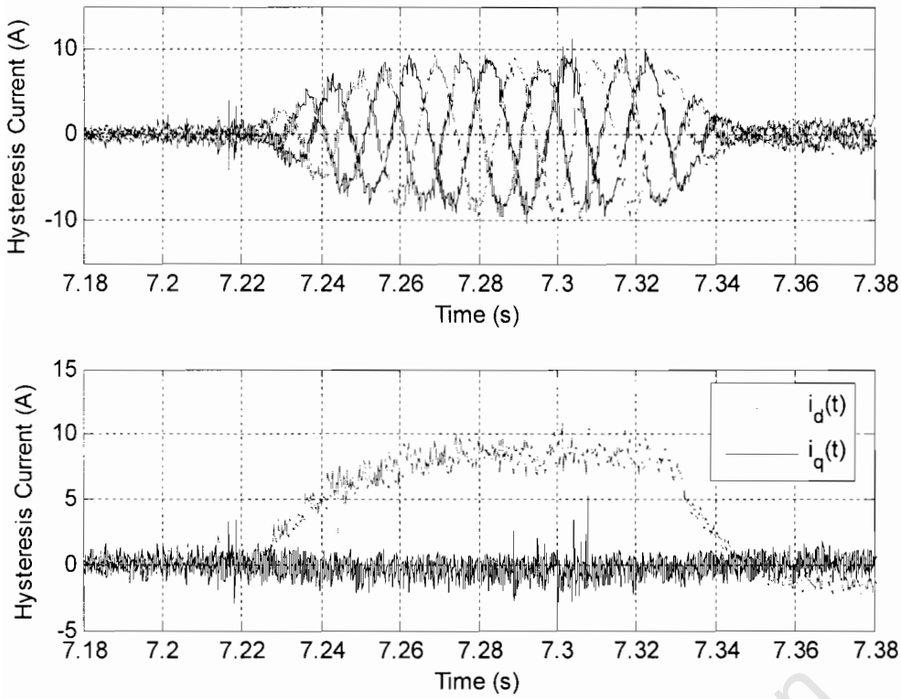

Figure 5-2: Experimental hysteresis currents during a balanced dip

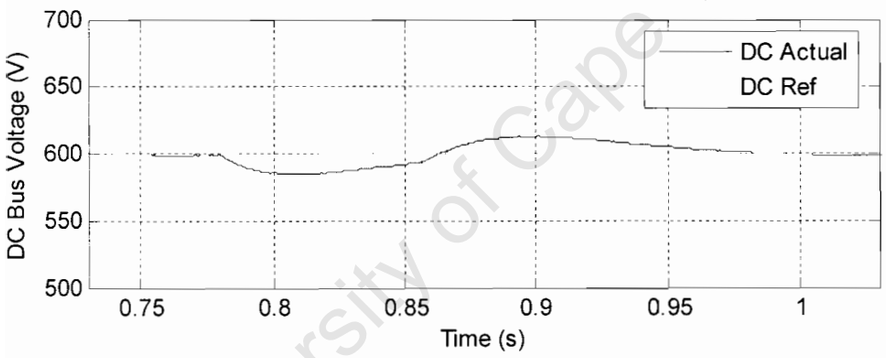

Figure 5-3: Simulated DC Bus voltage during a balanced dip

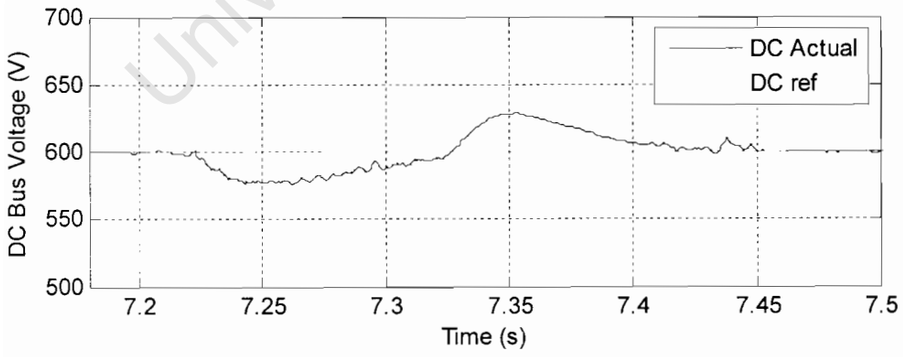

Figure 5-4: Experimental DC Bus voltage during a balanced dip

The supply and load three phase voltages are illustrated in figures 5.5 and 5.6 while their filtered d-component is displayed in figures 5.7 and 5.8. These graphs demonstrate that the controller does not achieve perfect compensation. This phenomenon is due to the voltage drop across the filter and transformers combination as discussed in section 3.1.2. Some oscillations due to harmonics are still present in the filtered signals of $E_d(t)$ and $V_d(t)$ but are of no consequence to the control.

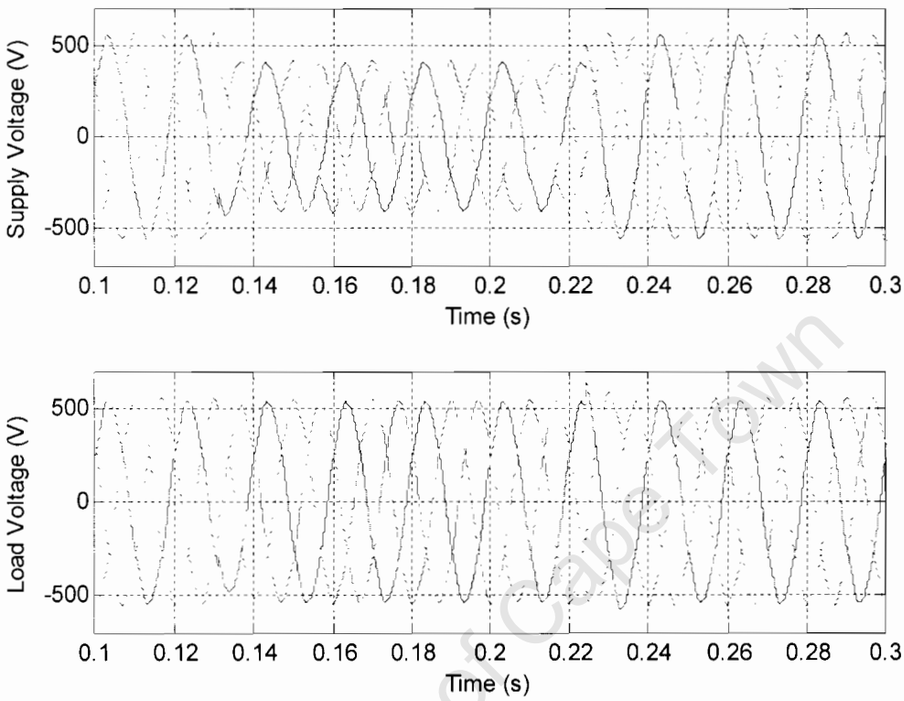

Figure 5-5: Simulated 3 phase voltages during a balanced dip

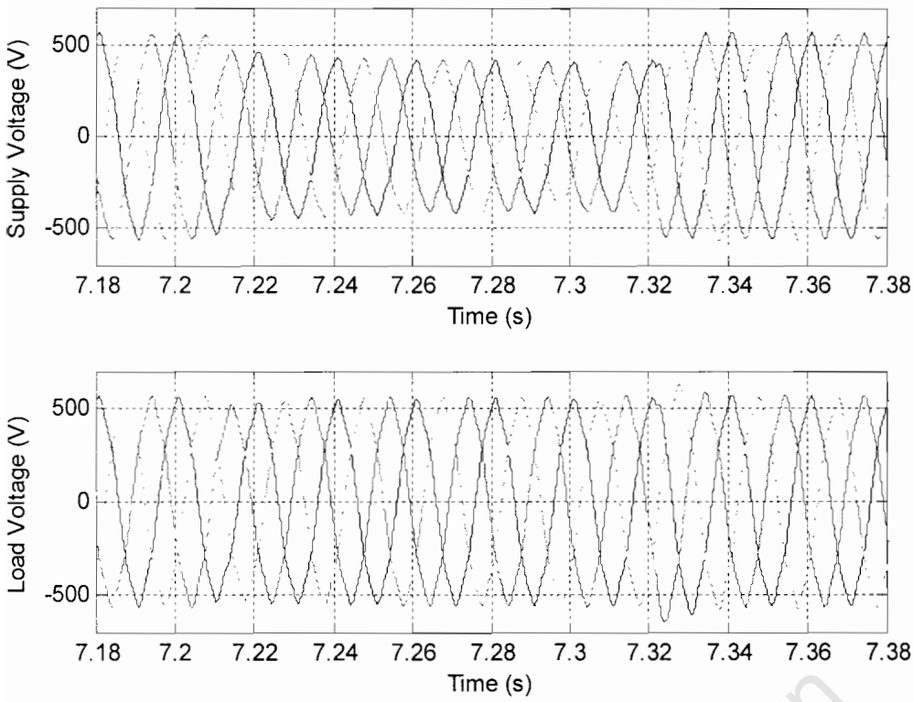

Figure 5-6: Experimented 3 phase voltages during a balanced dip

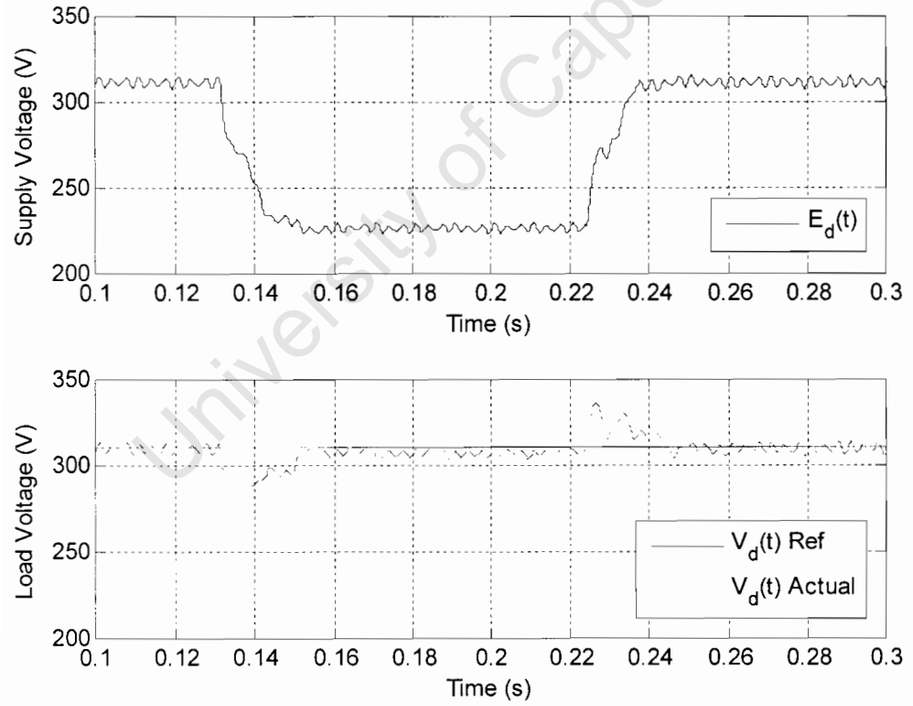

Figure 5-7 : Simulated d-components during a balanced dip

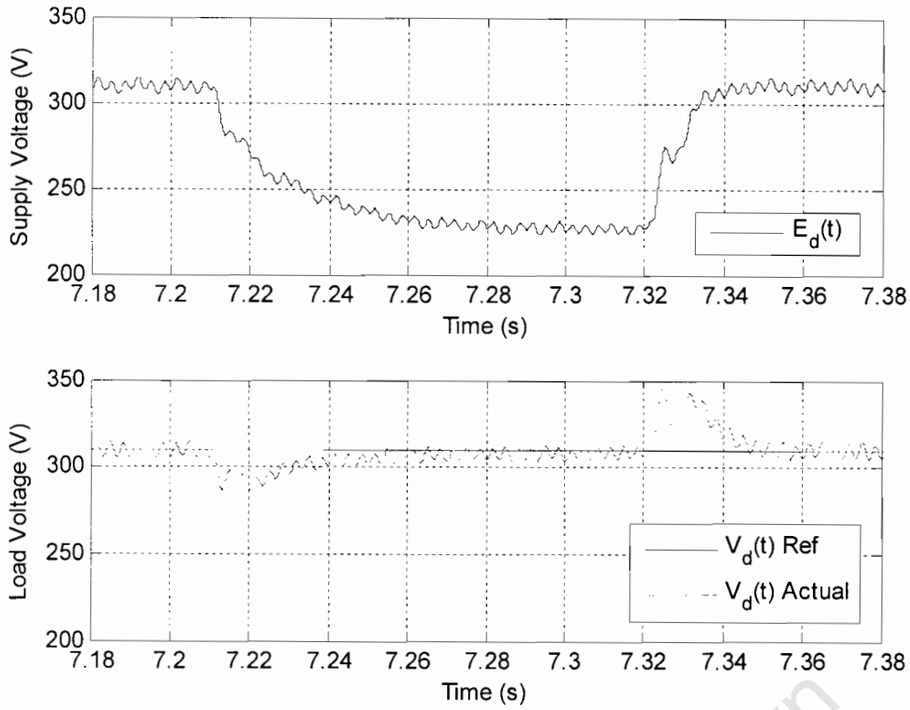

Figure 5-8: Experimental d-components during a balanced dip

5.1.2 Improved Positive Sequence Controller

This section describes the results obtained when using the improved positive sequence controller shown in figure 3.6 of section 3.1.3. The controller is tested with a similar dip as in section 5.1.1 for proper comparison of the two positive sequence controllers. The response of the controller and the HCC algorithm to a swell is also tested.

5.1.2.1 Regulation of balanced Dips

The same graphs as in section 5.1.1 are plotted for comparison. These contrasting plots indicate that the improved controller fully regulates the load voltage side. In fact, no steady state error occurs due to the presence of the PI controller. Full compensation should be achieved instantaneously but occurs within 1 cycle. This delay is due to the filters added to the algorithm because of the effect of harmonics. Some overshoot occurs due to the delay in the response of the controller (due to the filters) when the fault disappears. This overshoot is not harmful to the load as it lasts less than half a cycle, in compliance with the ITIC curve shown in figure 1.1.

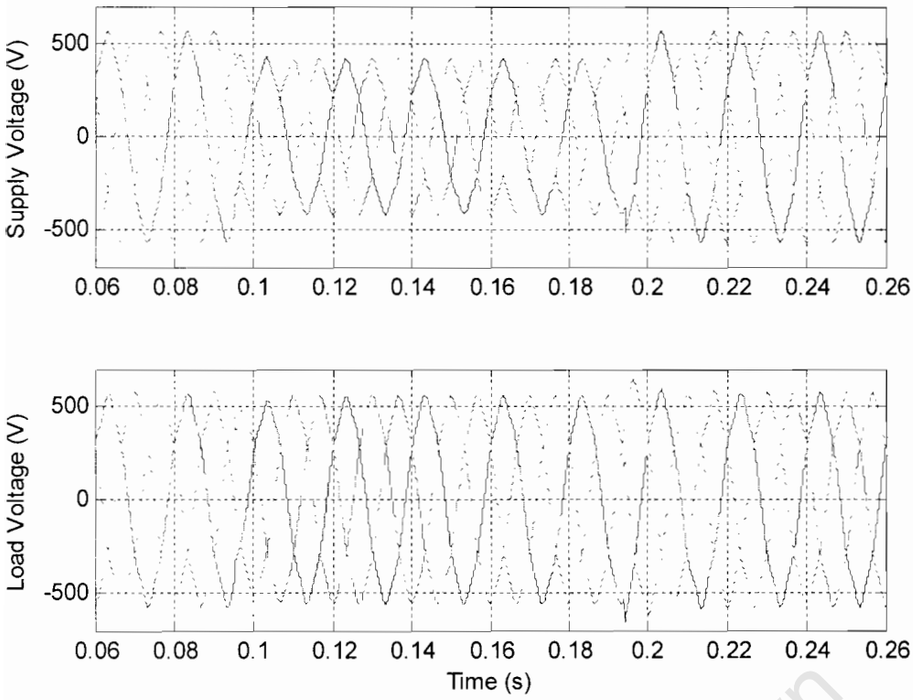

Figure 5-9: Simulated 3 phase voltages during a balanced dip

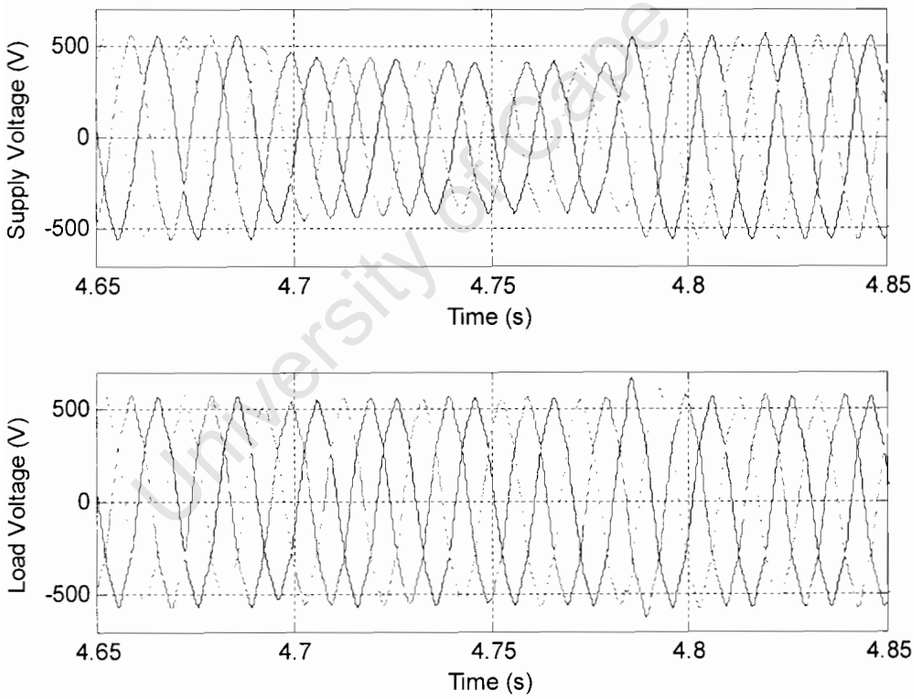

Figure 5-10: Experimental 3 phase voltages during a balanced dip

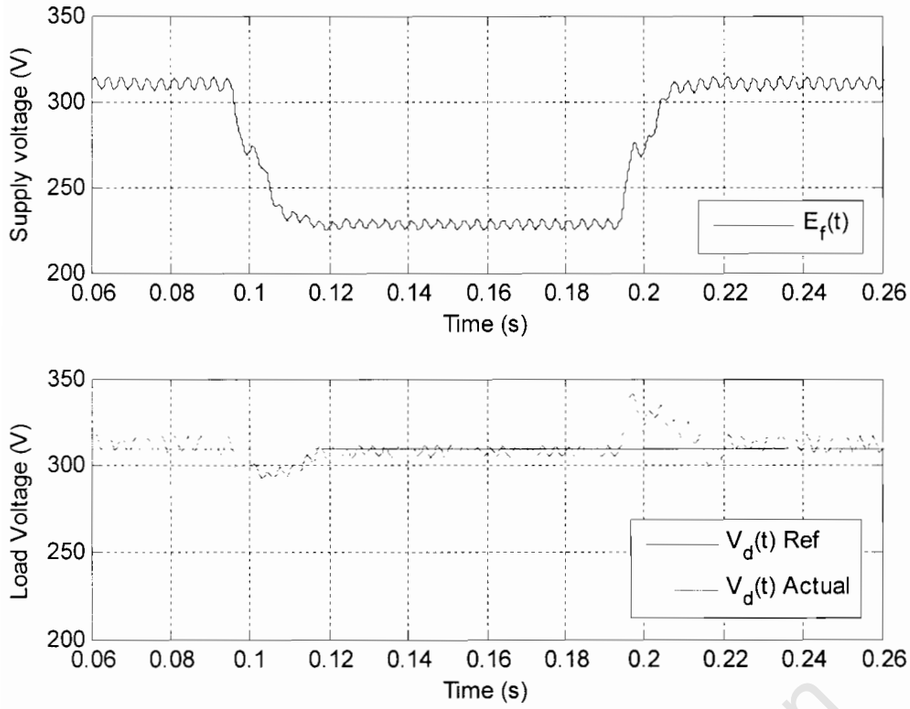

Figure 5-11: Simulated d-components during a balanced dip

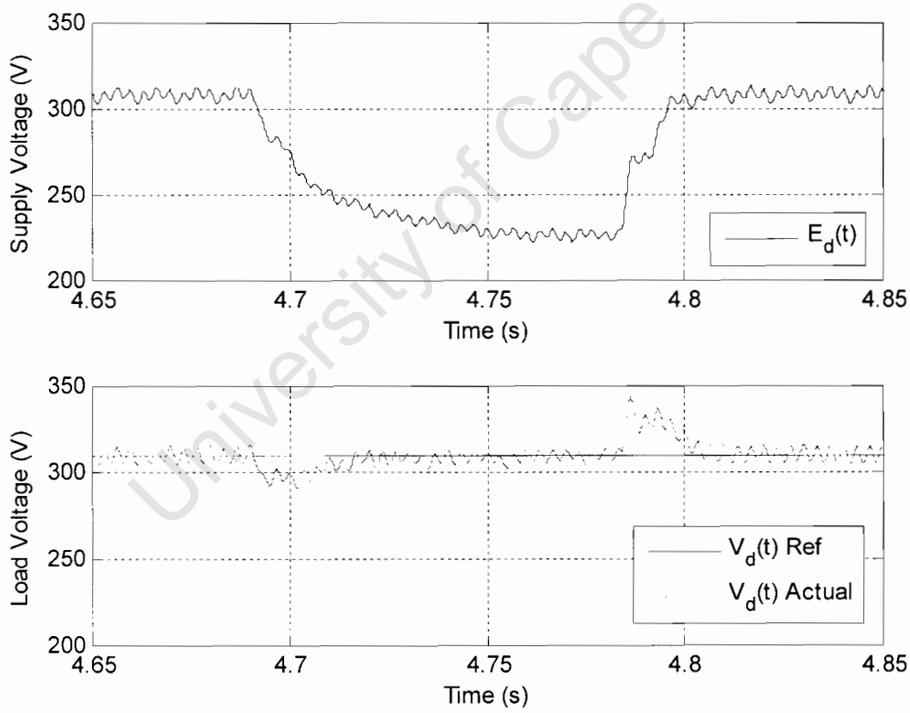

Figure 5-12: Experimental d-components during a balanced dip

3.6.1.1 Regulation of Swells

In this section, the improved positive sequence controller and the HCC technique are tested in the event of a 0.15pu swell. The swell is created as described in section 2.6.

As shown by figures 5.13 and 5.14, the shunt converter now pushes current to the supply when the swell occurs, in order to maintain the DC bus voltage at 600V. This response is indicated by the magnitude of i_d which is now negative. Power transfer occurs at unity power factor since i_q is 0. Figures 5.15 and 5.16 confirm that the DC bus is again successfully regulated at 600V.

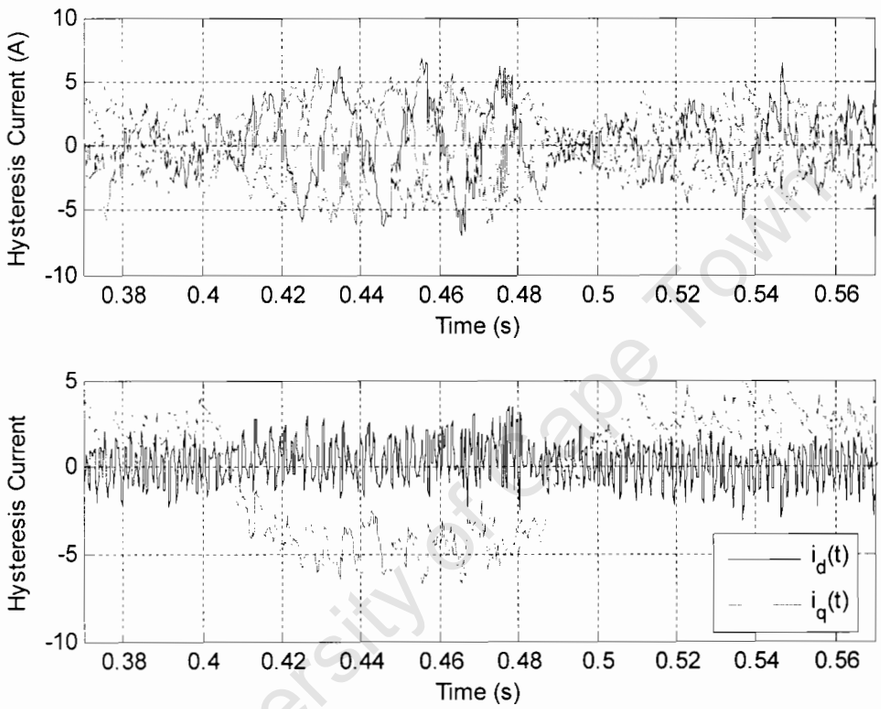

Figure 5-13: Simulated hysteresis currents during a swell

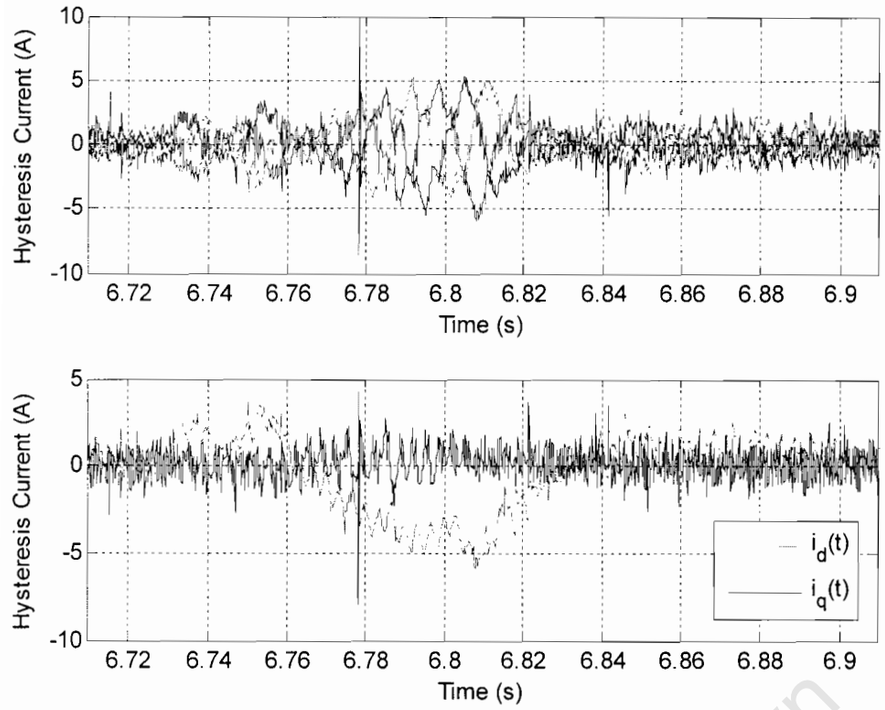

Figure 5-14: Experimental hysteresis currents during a swell

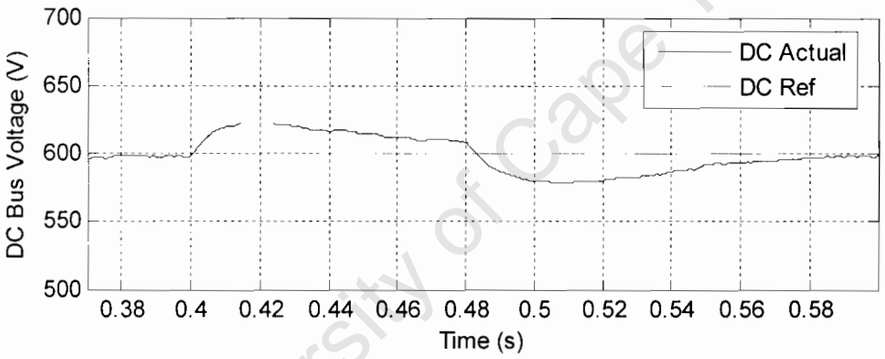

Figure 5-15: Simulated DC Bus voltage during a swell

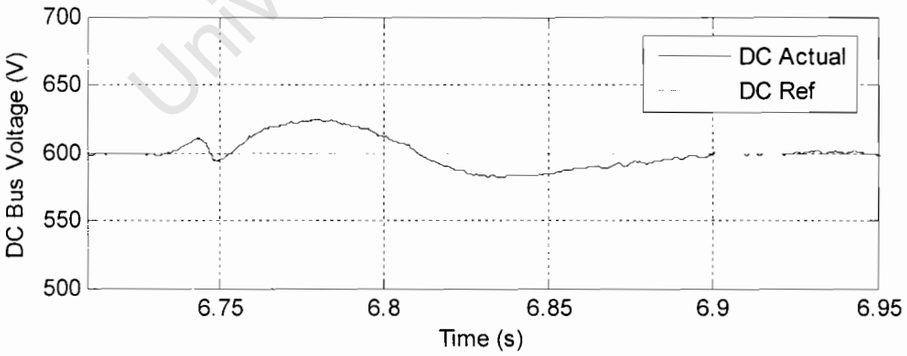

Figure 5-16: Experimental DC Bus voltage during a swell

The supply and load three phase voltages are illustrated in figures 5.17 and 5.18 while their filtered d-components are displayed in figures 5.19 and 5.20. These graphs demonstrate that the controller shields the load successfully from the voltage swell. Once more, the effect of the filters used is visible as a delay in the response of the device. The oscillations due to harmonics are again visible in the filtered signals of $E_d(t)$ and $V_d(t)$ but are small enough to be of no consequence to the control.

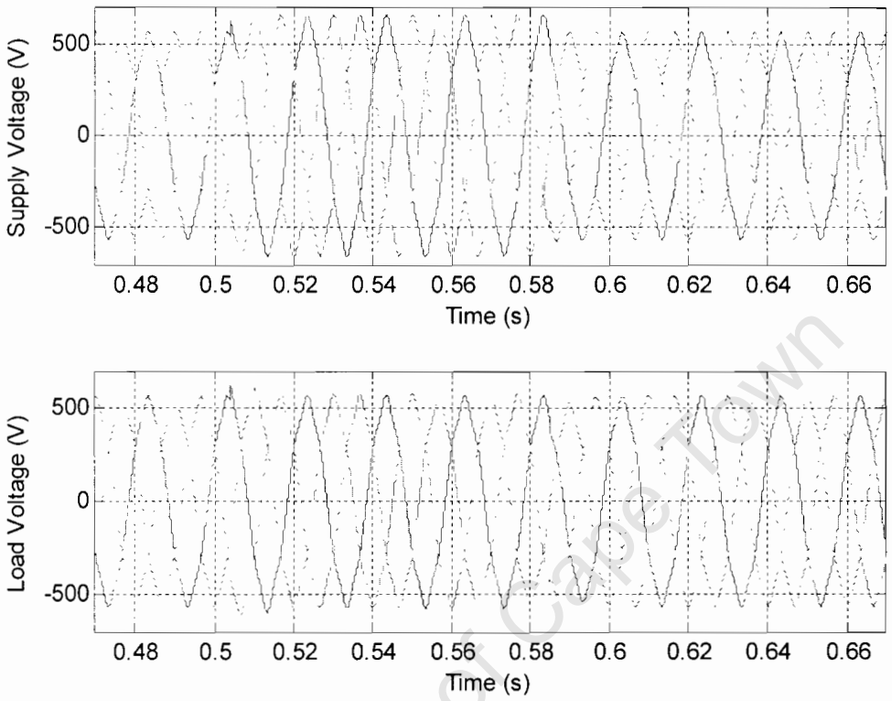

Figure 5-17: Simulated 3 phase voltages during a swell

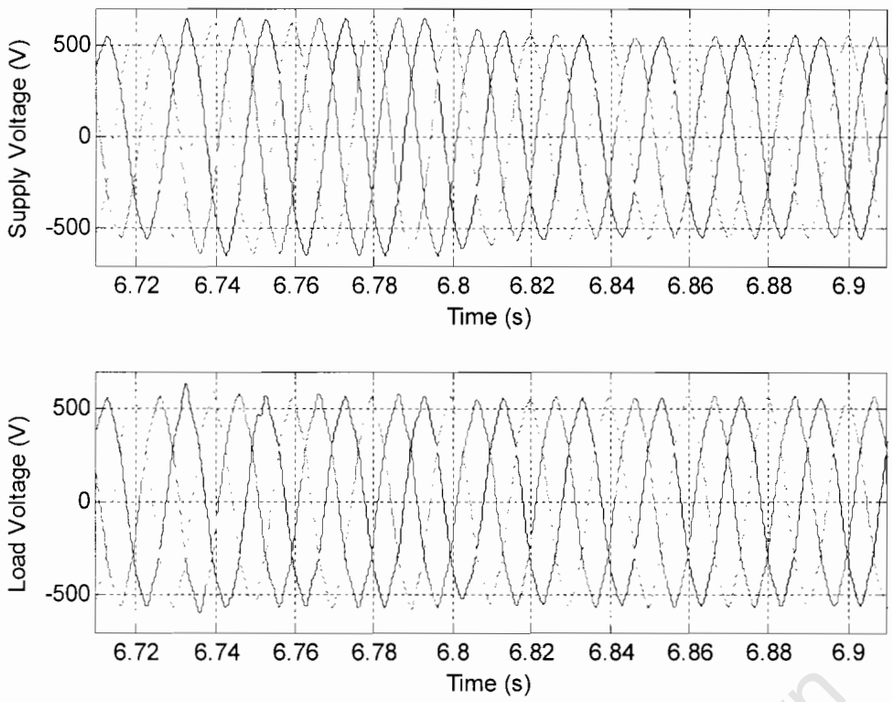

Figure 5-18: Experimental 3 phase voltages during a swell

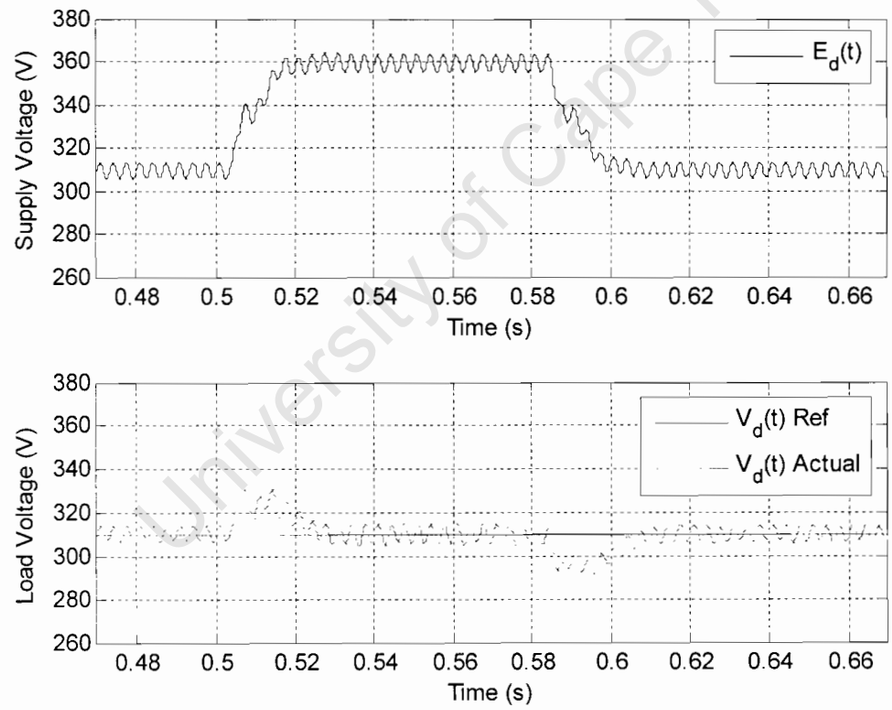

Figure 5-19: Simulated d-components during a swell

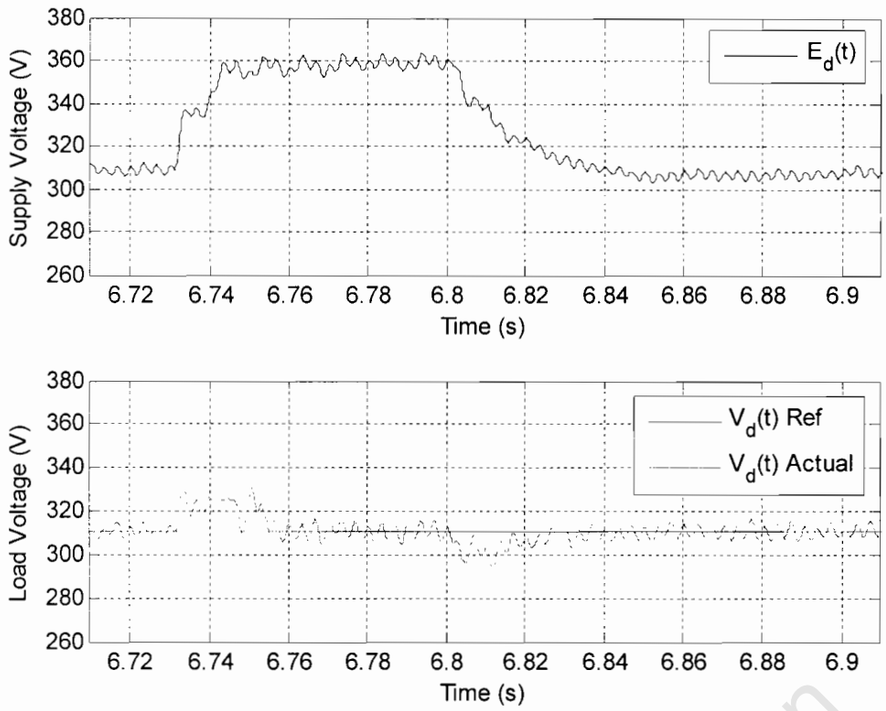

Figure 5-20: Experimental d-components during a swell

5.2 Positive and Negative Sequences Controllers

In this section, the algorithm illustrated in figure 3.18 of section 3.2.2 including both positive and negative sequences controllers, is tested for an unbalanced dip. The ability of the HCC technique to regulate the DC bus voltage in the presence of an unbalanced dip is also tested. The algorithm is again modified by adding band pass filters to handle the harmonics present in the supply and load voltages.

As shown by figures 5.21 and 5.22, the shunt converter absorbs current from the supply when a unbalanced dip occurs to regulate the DC bus voltage at 600V. i_q is again forced to 0 indicating that only real power flows. Figures 5.23 and 5.24 show the regulated DC bus at 600V. It is worth noting that the hysteresis currents include more ripple than in section 5.1.1. This outcome arises because the sampling frequency is lower here due to the more complex algorithm. As discussed in section 2.5.2, the current overshoot increases with decrease in the sampling frequency.

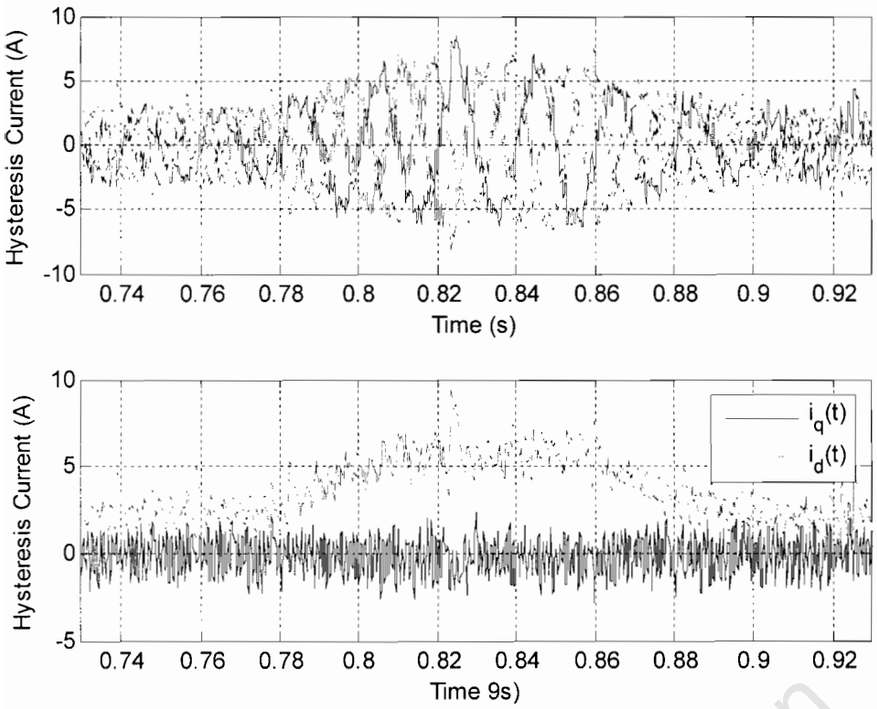

Figure 5-21: Simulated hysteresis currents during an unbalanced dip

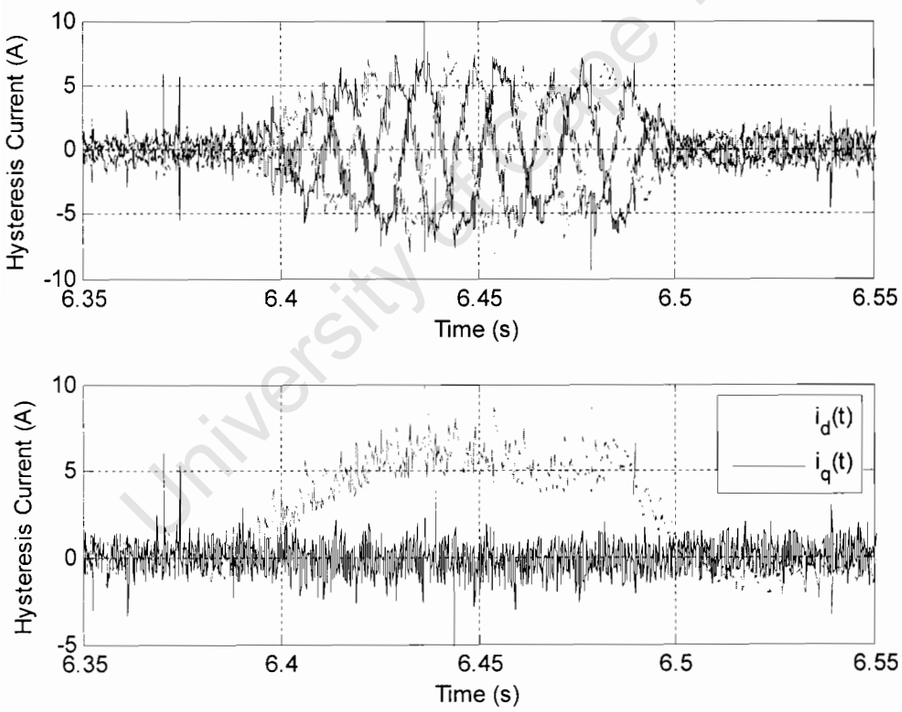

Figure 5-22: Experimental hysteresis currents during an unbalanced dip

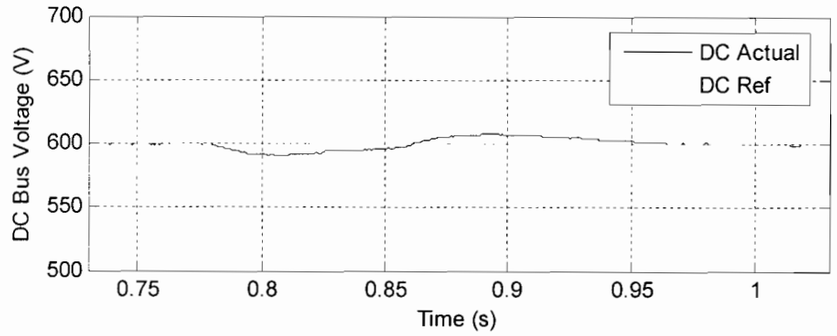

Figure 5-23: Simulated DC Bus voltage during an unbalanced dip

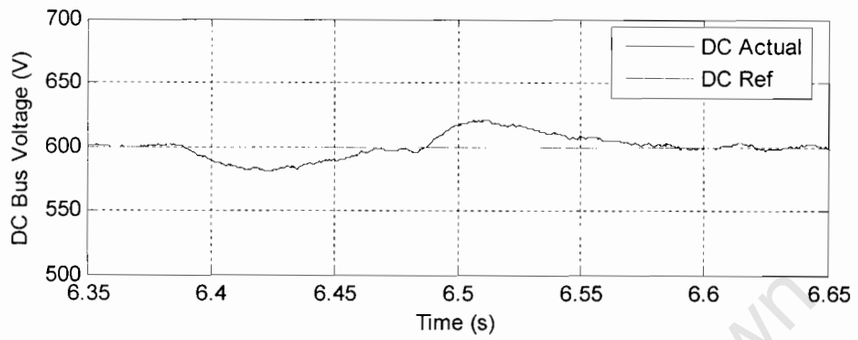

Figure 5-24: Experimental DC Bus voltage during an unbalanced dip

Figures 5.25 and 5.26 illustrate the supply and load three phase voltages while figure 5.27 and 5.28 show the filtered positive sequence d-components. The inverter injects a combination of positive and negative sequence to ensure that the unbalance is removed and full compensation is achieved. The response of this controller should be a quarter of a cycle but is longer due to the presence of filters to suppress the harmonics. Figures 5.29 and 5.30 demonstrate how the negative sequence present in the supply voltage is mitigated by the device.

When the positive and negative sequence voltages are extracted from the supply and load voltages, the main harmonics, i.e. the 5^{th} and 7^{th} harmonics, appear only in the negative sequence. For this reason the d-components of the supply and load positive sequence voltages, $E_d^{pos}(t)$ and $V_d^{pos}(t)$ (figures 5.27 and 5.28), do not include the oscillations that appear in the d-components of the supply and load voltage, $E_d(t)$ and $V_d(t)$ (figures 5.7, 5.8, 5.11 and 5.12), respectively. However, these oscillations can be observed in the supply and load negative sequence d-components, $E_d^{neg}(t)$ and $V_d^{neg}(t)$.

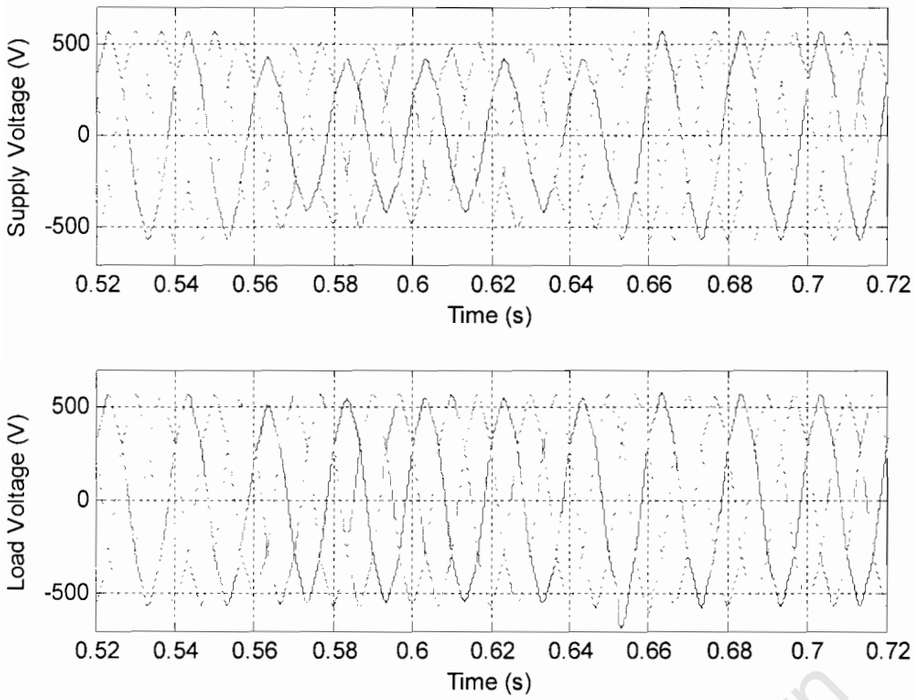

Figure 5-25: Simulations 3 phase voltages during an unbalanced dip

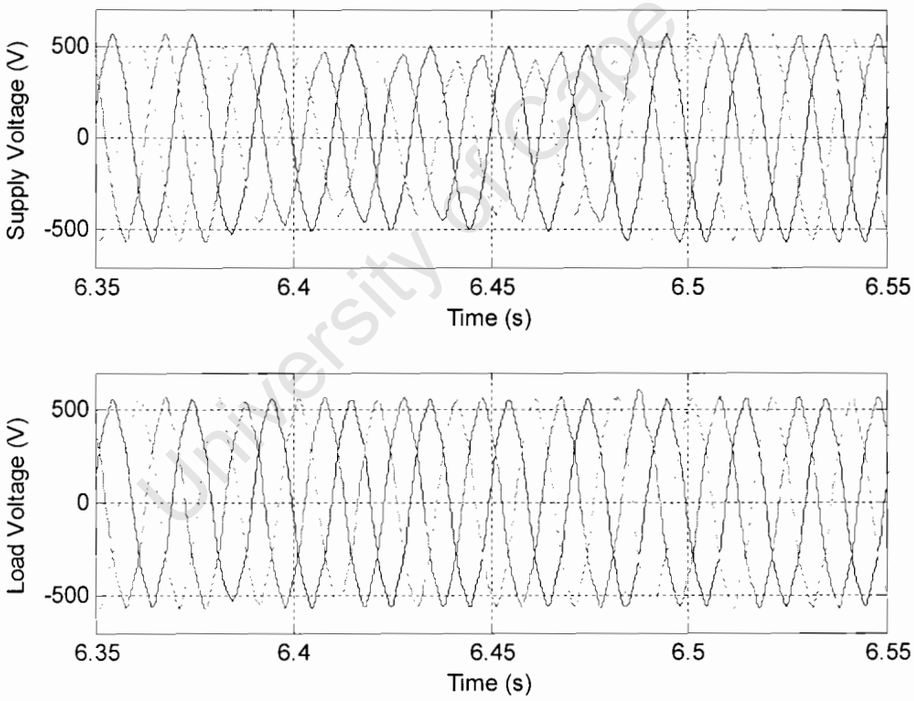

Figure 5-26: Experimental 3 phase voltages during an unbalanced dip

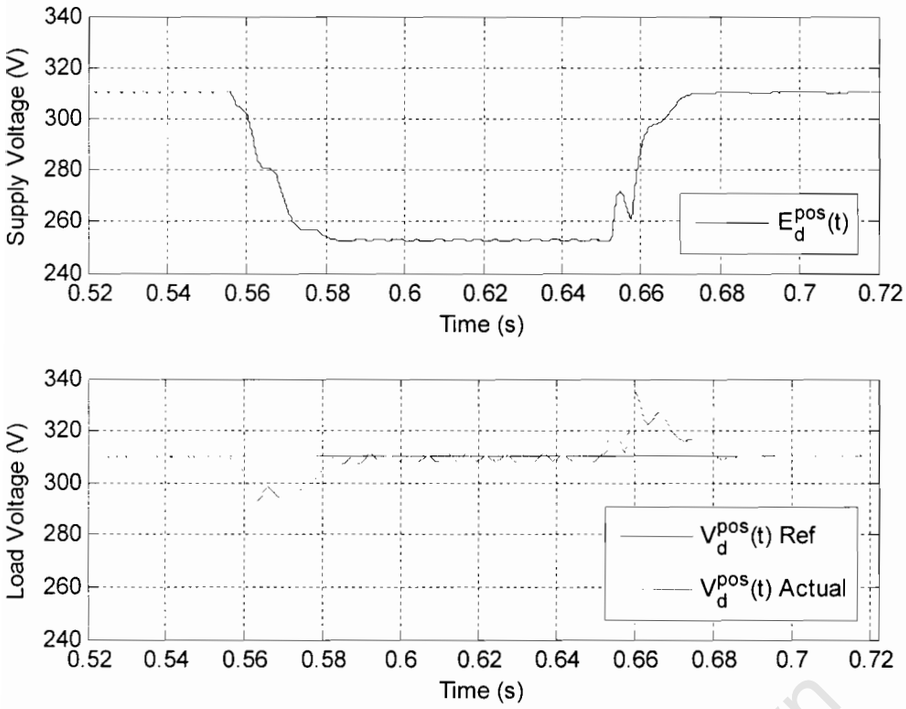

Figure 5-27: Simulated Pos. Seq. voltage d-components during an unbalanced dip

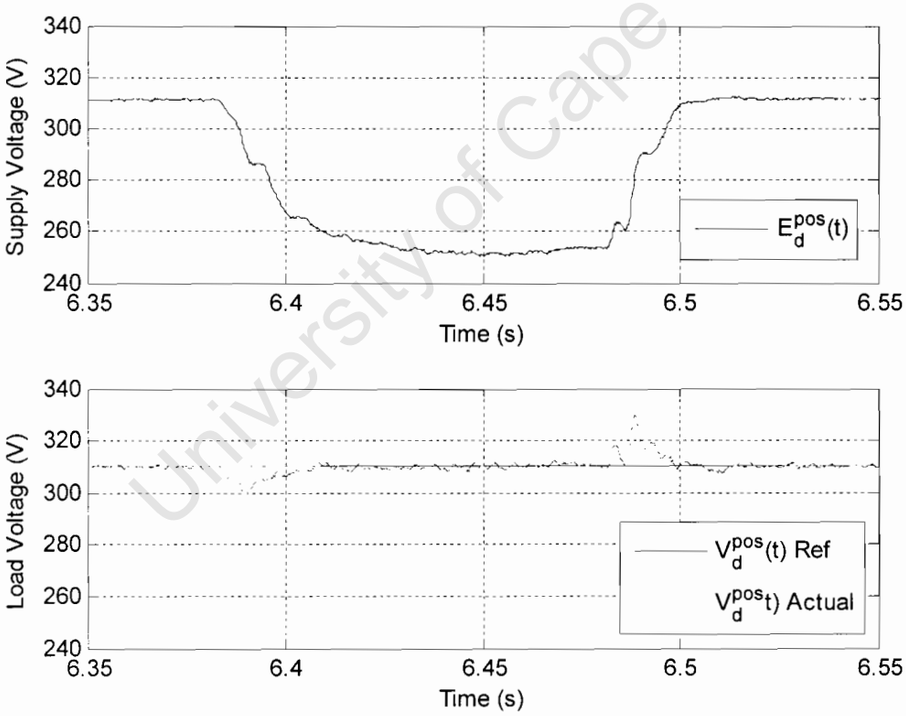

Figure 5-28: Experimental Pos. Seq. voltage d-components during an unbalanced dip

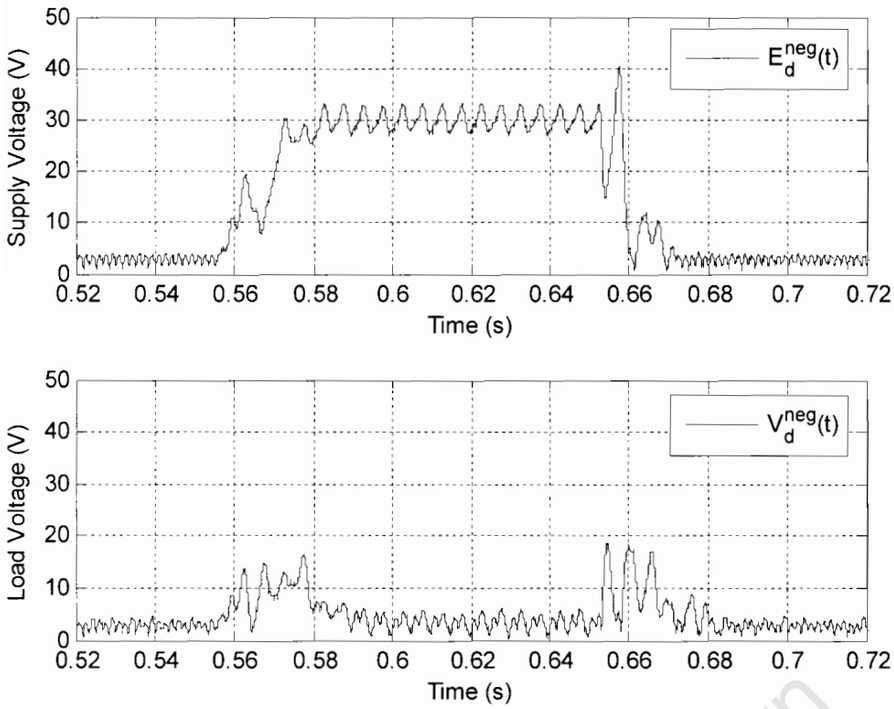

Figure 5-29: Simulated Neg. Seq. voltage d-components during an unbalanced dip

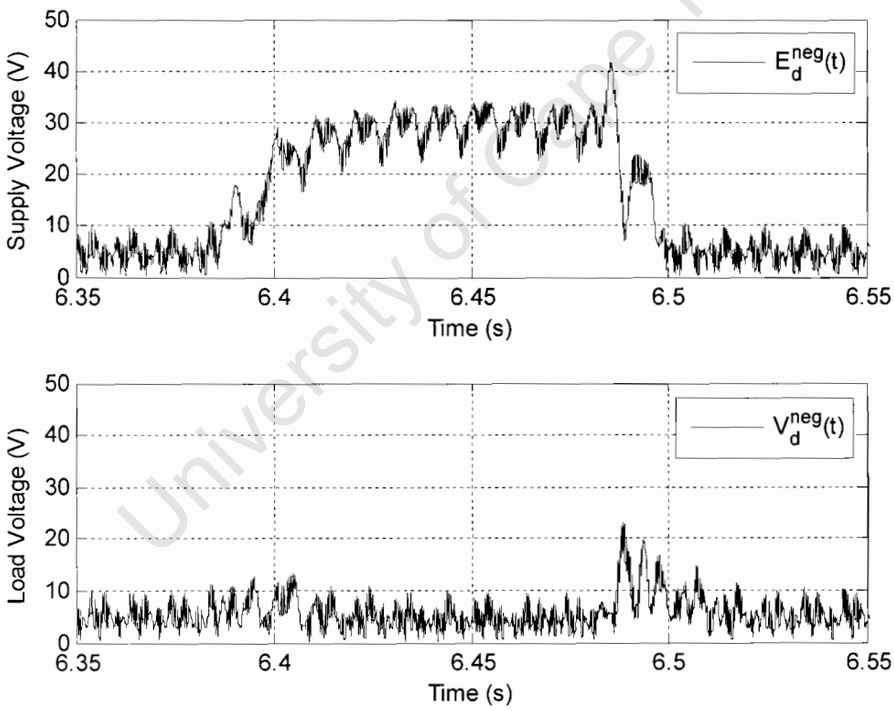

Figure 5-30: Experimental Neg. Seq. voltage d-components during an unbalanced dip

5.3 Low Order Harmonics Detection and Mitigation

In this section, the technique described in section 3.3.1 (figure 3.25) for the detection and mitigation of low order harmonics is tested. The two main harmonics present in the UCT supply, namely the 5^{th} and the 7^{th} are detected and mitigated. No filtering is needed in this case as no PI controller is used in the algorithm. The d-components illustrated in figures 3.33 and 5.34 are thus the actual signals unlike the d-components plotted in the previous sections which are filtered signals. The mitigation device is initially off and turned on at time t=2.32s in real time experimentation and at t=0.20s in simulation. Figures 3.31 and 5.32 clearly indicate that the 5^{th} and 7^{th} harmonics have been mitigated within a cycle, as pure sinusoidal waveforms are obtained.

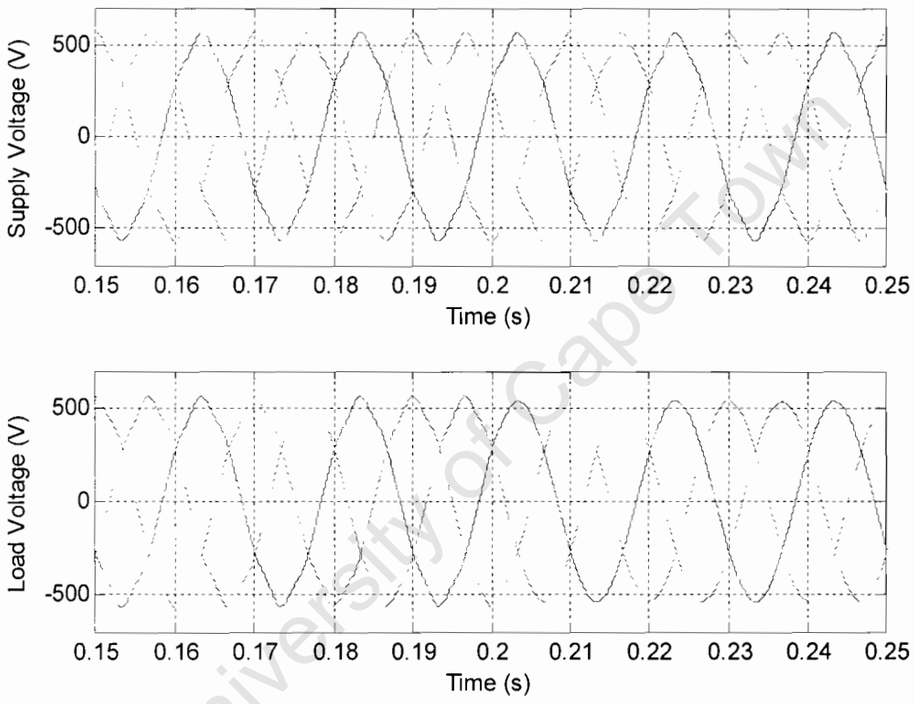

Figure 5-31: Simulated 3 phase voltages with 5^{th} & 7^{th} harmonics mitigation

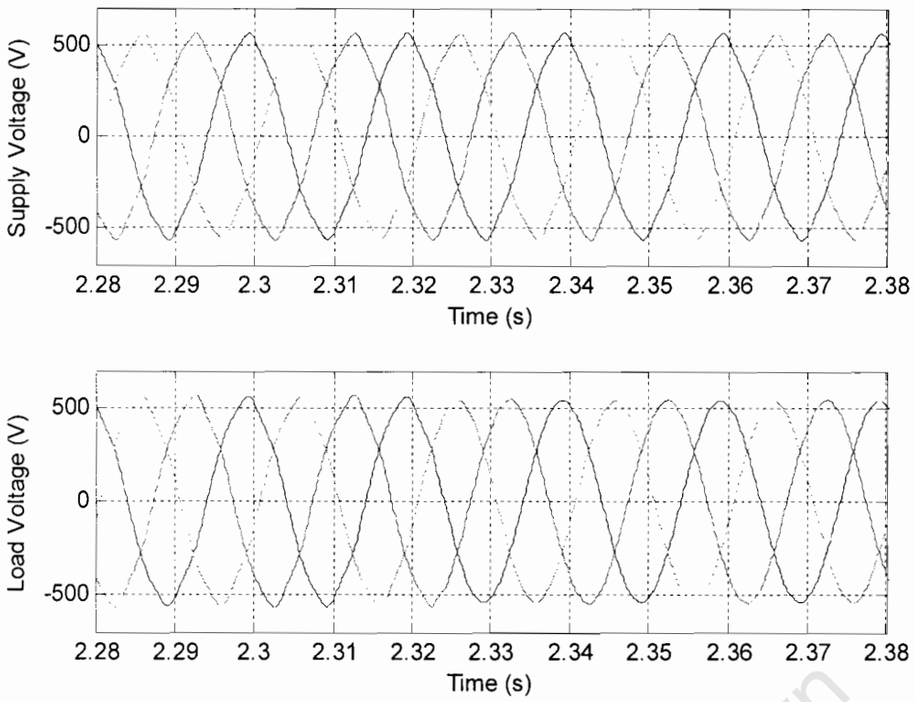

Figure 5-32: Experimental 3 phase voltages with 5th & 7th harmonics mitigation

Figures 5.33 and 5.34 show the actual supply voltage d-component, $E_d(t)$. The 5th and 7th harmonics are visible as superimposed 300Hz oscillations as discussed in section 3.1.3. As the device is switched on, these oscillations almost disappear completely on the load side d-component, $V_d(t)$, confirming that the two harmonics have indeed been mitgated. The high frequency oscillations left on the experimented load voltage d-component are due to the 11th and 13th harmonics which have not been detected. The simulated load voltage d-component does not include these higher oscillations because the three phase programmable voltage source from the SimPowerSystems Toolbox in Matlab-Simulink can not be programmed with more than two harmonics. Thus, only the 5th and the 7th harmonics were present in the simulated supply voltage.

Finally, the captured harmonics measurements from the Qualistar three phase power quality analyzer shown in figure 5.35 confirm that the magnitudes of both these harmonics have been reduced greatly.

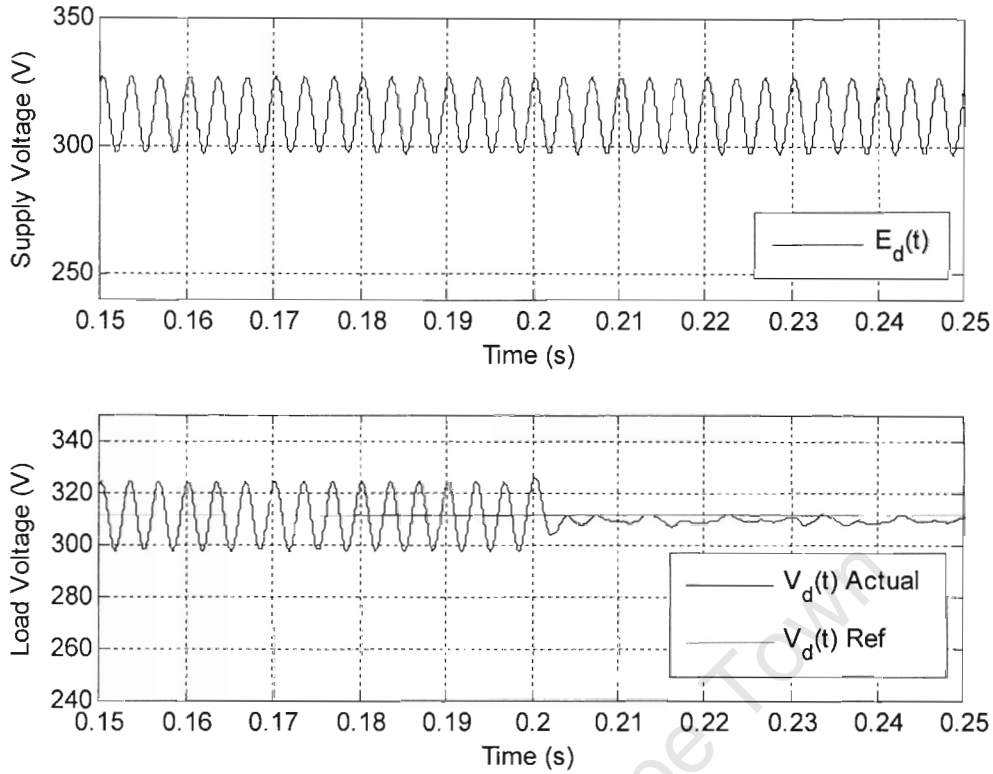

Figure 5-33: Simulated d-components with 5th & 7th harmonics mitigation

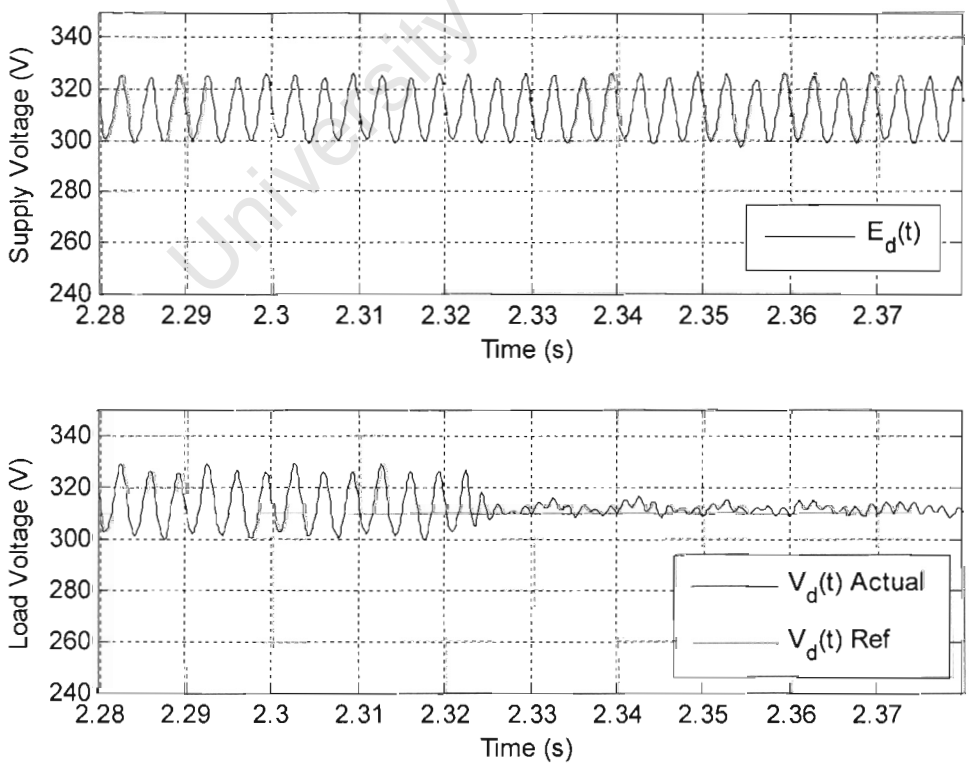

Figure 5-34: Experimental d-components with 5th & 7th harmonics mitigation

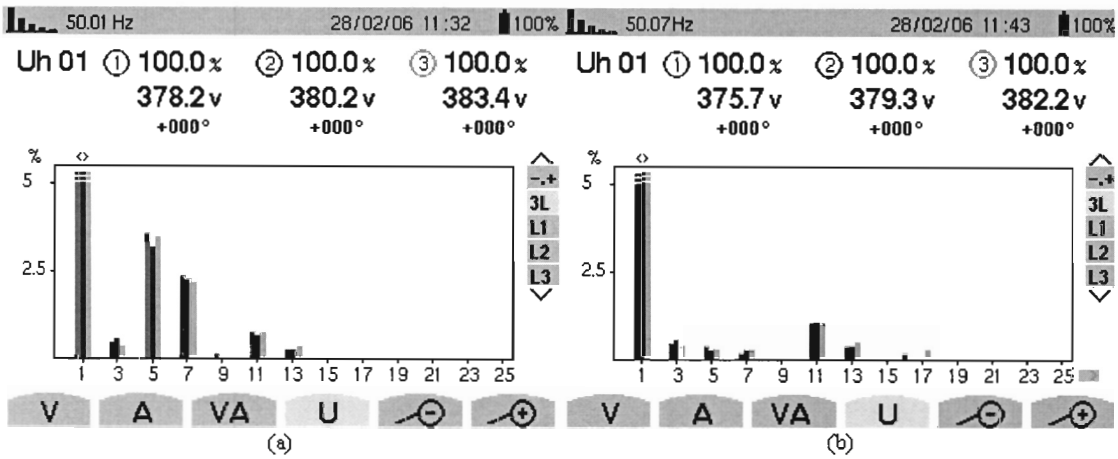

Figure 5-35: Harmonic spectrum for (a) Supply voltage and (b) Load voltage

5.4 The Complete System

In this section, the complete algorithm, with the positive and negative sequences controllers as well as harmonics detection and mitigation, is tested. This algorithm is shown in figure 3.28 in section 3.3.2. The α-β voltage components, $E_\alpha(t)^*$ and $E_\beta(t)^*$, obtained from subtracting the 5^{th} and 7^{th} harmonics supply α-β voltage components from the supply α-β voltage components, contain higher harmonics. Indeed, as illustrated in figure 5.35, the supply voltage also includes some 11^{th} and 13^{th} order harmonics. These harmonics are not detected to simplify the algorithm and maintain an acceptable sampling frequency. Hence, $E_\alpha(t)^*$ and $E_\beta(t)^*$ are filtered to remove these two harmonics. The same band pass filters as described in section 5.1 are used for that purpose. Similarly, $V_\alpha(t)$ and $V_\beta(t)$ must also be filtered to remove these two harmonics which are not mitigated by the device. Thus, the response of the device is slowed down by these filters. However, if all harmonics were detected, none of these filters would be used and a much faster response would be achieved.

As in section 5.3, the d-components illustrated in this section are the actual supply and load d-components. They are unfiltered signals unlike those plotted as in section 5.2 and 5.3. The two signals $E_d(t)$ and $V_d(t)$ include information that describe the supply and load voltages. As described in chapter 3, an unbalance is depicted by 100Hz oscillations superimposed on that d-component. On the other hand, the 5^{th} and 7^{th}

harmonic will appear as 300 Hz oscillations while higher harmonics will appear as oscillations of even higher frequencies.

5.4.1 Balanced Dip and Harmonic Mitigation

In this section, the complete algorithm is tested for mitigation of the 5^{th} and 7^{th} harmonics as well as mitigation of a balanced dip. Both simulated and experimental results are presented.

Figures 5.36 and 5.37 show the three phase supply and load voltages. It is quite clear from these waveforms that the load is shielded from the dip. It is also observed that better sinusoidal waveforms are achieved on the load side indicating mitigation of harmonics. Once again, the delay due to the filters is visible as the disturbance is mitigated after about a cycle (instead of a quarter of a cycle).

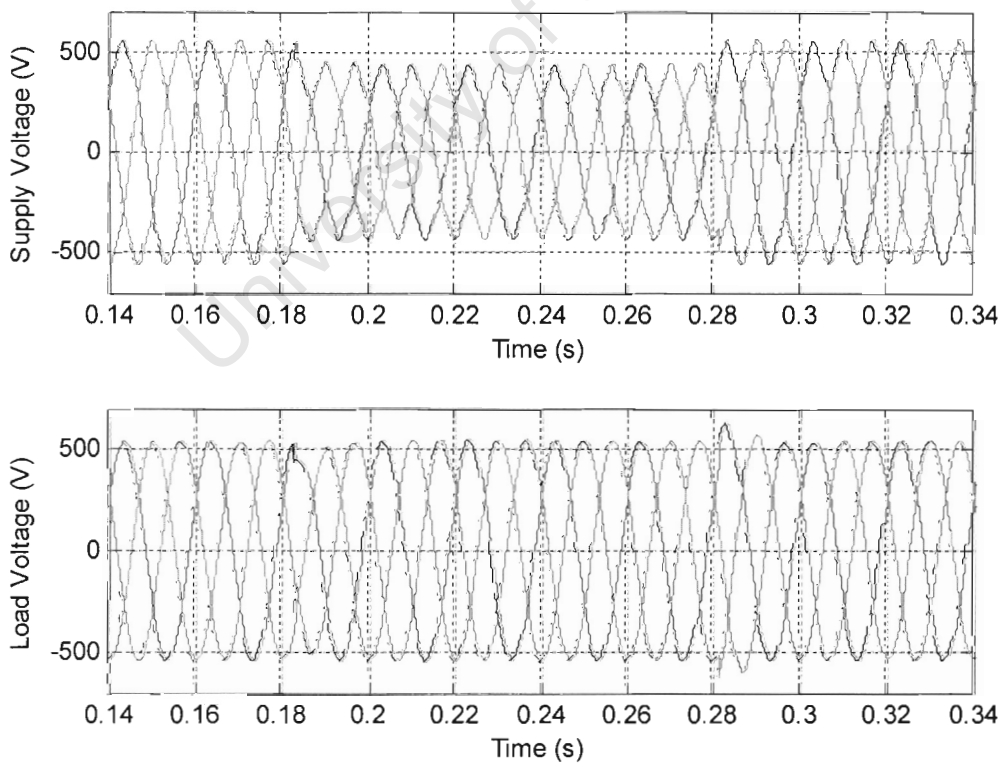

Figure 5-36: Simulated 3 phase voltages during the dip with harmonics mitigation

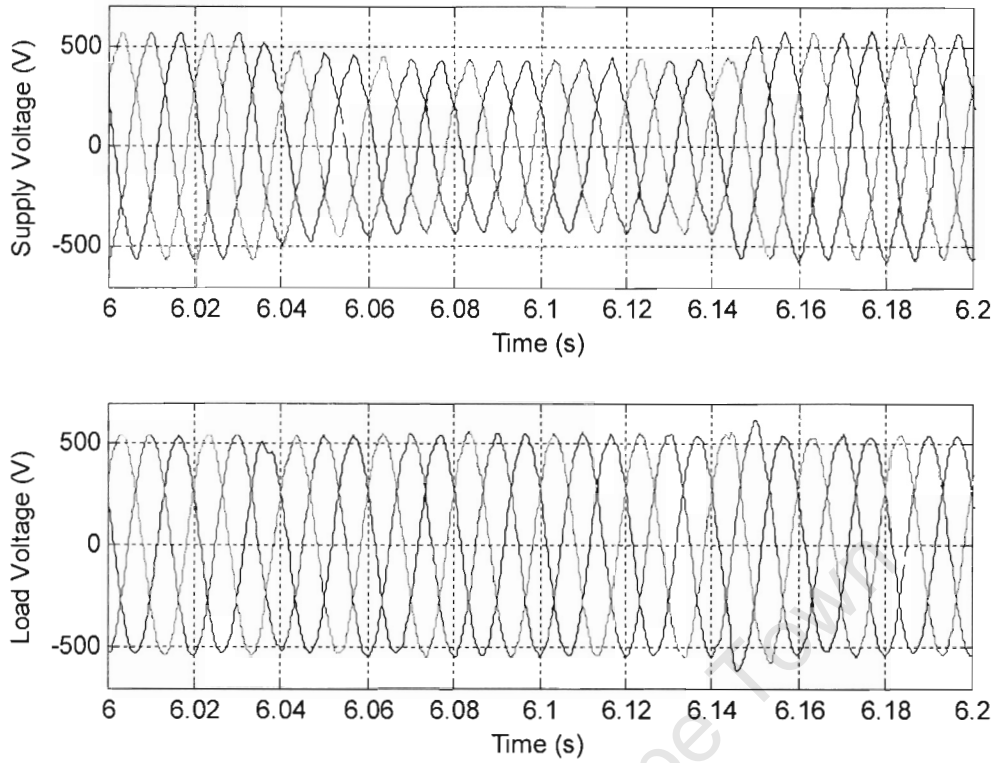

Figure 5-37: Experimental 3 phase voltages during the dip with harmonics mitigation

Figures 5.38 and 5.39 illustrate the supply and load voltages d-components. The 300Hz oscillations present in $E_d(t)$ are less visible in $V_d(t)$ indicating that the 5^{th} and 7^{th} harmonics have been mitigated. However, the load voltage d-component from experiment results includes some higher frequency oscillations that are not present in the simulated signal. This phenomenon arises because:

a) As mentioned in the previous section, the simulated three phase source does not include the 11^{th} and 13^{th} harmonic present in the actual three phase source. Thus, the oscillations due to these harmonics that appear on the experimental $V_d(t)$ does not appear on the simulated one.

b) Furthermore, the processor controls both the shunt and the series converter performing DC bus regulation as well as mitigation of dips, swells and harmonics. Thus, the cycle time of the processor is rather large. As a result, the sampling frequency, hence the switching frequency of the shunt converter

is low. This low frequency causes large current overshoots in the three phase hysteresis currents as discussed in section 2.5.2, and when the currents are large as during a dip, they generate additional harmonics in the supply. However, as described in section 4.3.1, a pure DC source was used to supply the series converter in simulations. Thus, the harmonics generated by the hysteresis currents were not encountered and did not appear on the simulated d-component.

Figures 5.39 and 5.40 confirm that as the hysteresis currents become more significant during the dip, the harmonics generated by the current overshoot increases and more oscillations appear on $V_d(t)$.

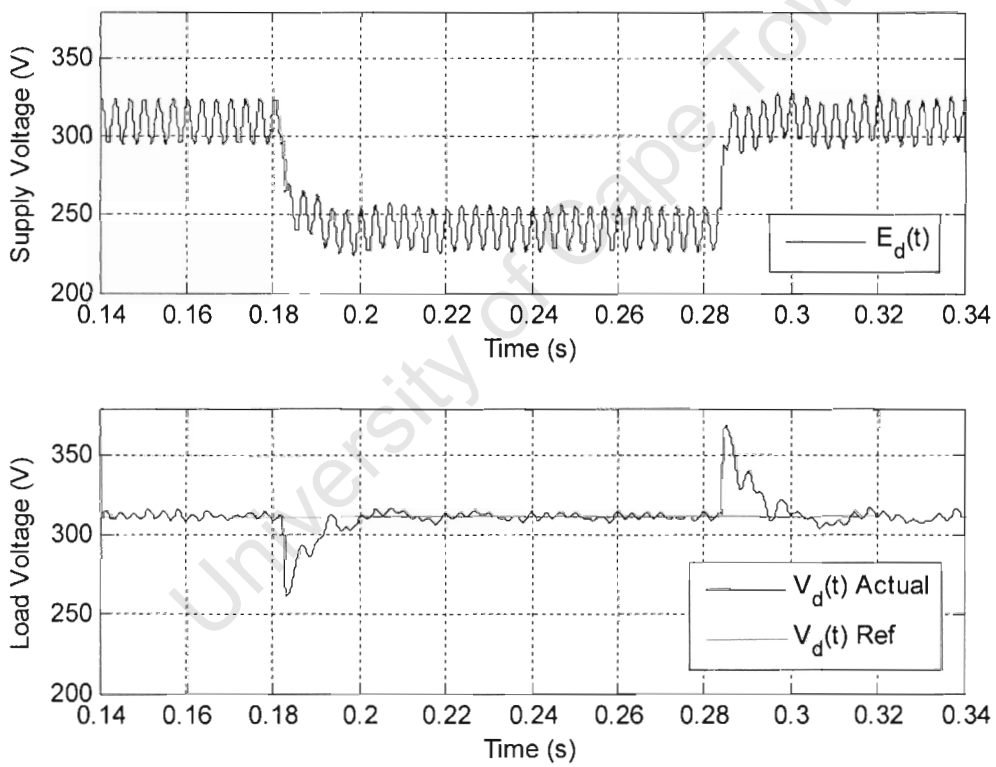

Figure 5-38: Simulated d-components during the dip with harmonics mitigation

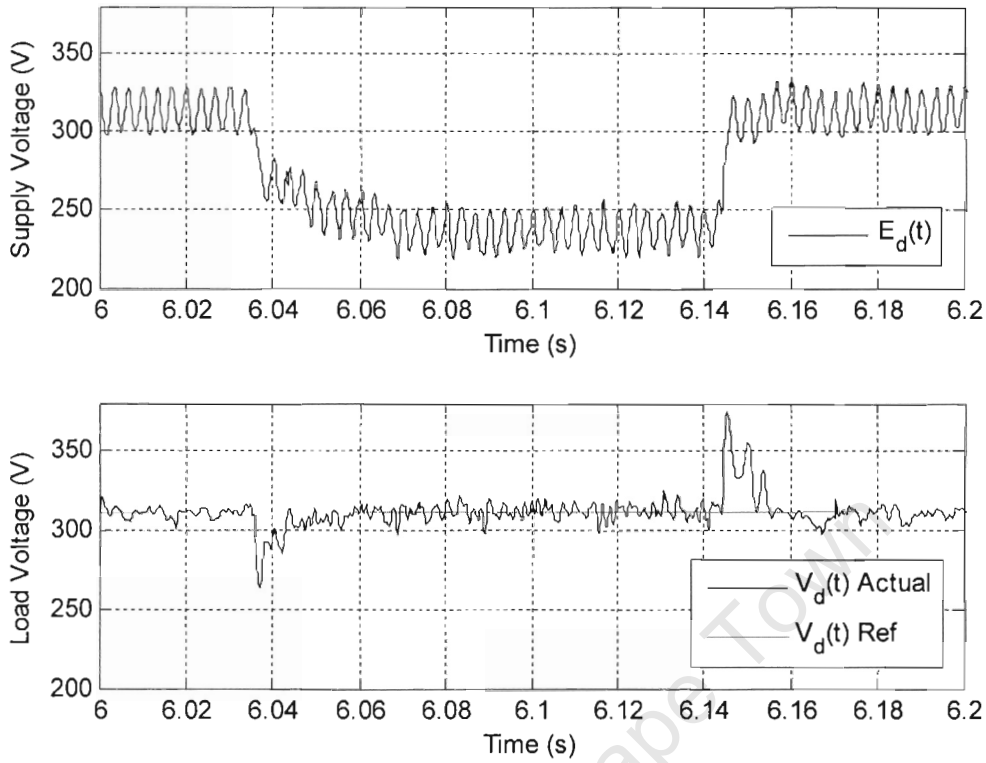

Figure 5-39: Experimental d-components during the dip with harmonics mitigation

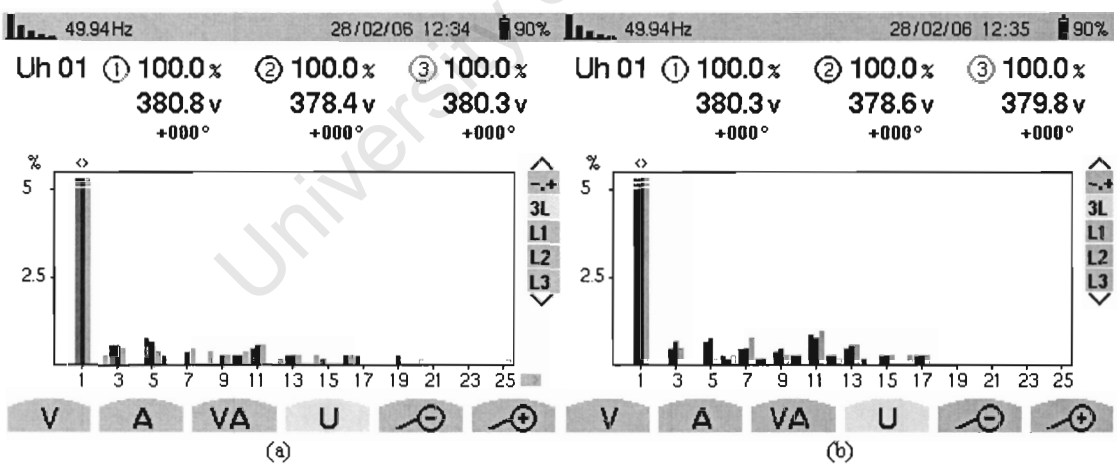

Figure 5-40: Harmonic spectrum of load volt. during (a) normal operation and (b) dip

Figure 5.41 demonstrate the results obtained from an experiment carried out to confirm the explanation given in part (b) concerning the harmonics generated by hysteresis currents. The dc bus of the shunt converter was connected to a 3kW dc load to simulate the power absorbed by the series converter during a 0.25pu dip. A 0.25 dip was then created and the DC bus was regulated by the HCC technique at 600V. Two

tests were performed, one using a sampling frequency of 0.0001s and the other 0.000165s which is the sampling frequency used in the previous experiment for both balanced dip and harmonic mitigation. The harmonic spectrum of the supply for the higher sampling frequency is shown in picture (b) while the spectrum of the supply for the lower one is shown in picture (a) of figure 5.41. The two harmonic spectrum confirm that at a low sampling frequency (thus switching frequency), the hysteresis currents do indeed add extra harmonics (5^{th}, 11^{th}, 13^{th}, 15^{th}, 17^{th}, 19^{th} and 21^{st}) to the ones that were already present in the supply (3^{rd}, 5^{th}, 7^{th}, 11^{th} and 13^{th}).

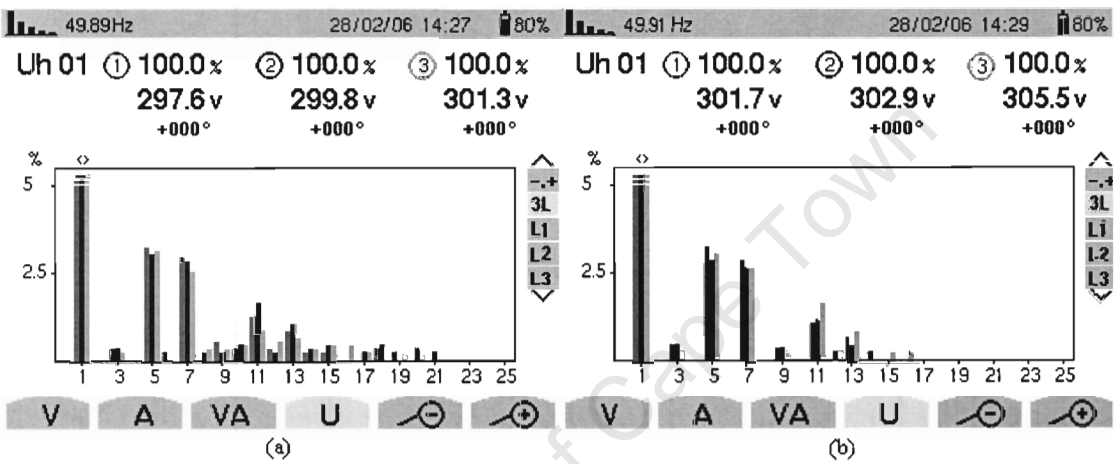

Figure 5-41: Harmonic spectrum of supply voltage for different sampling frequencies

5.4.2 Swell and Harmonic Mitigation

In this section, the complete algorithm is tested for mitigation of the 5^{th} and 7^{th} harmonics as well as mitigation of a swell. Again, both simulated and experimental results are presented.

Figures 5.42 and 5.43 show the three phase supply and load voltages. The three phase voltage on the load side is well regulated and barely affected by the swell. Furthermore, as in section 5.4.1, the mitigation of harmonics is visible on the load side. The delay caused by the filter is yet again observed.

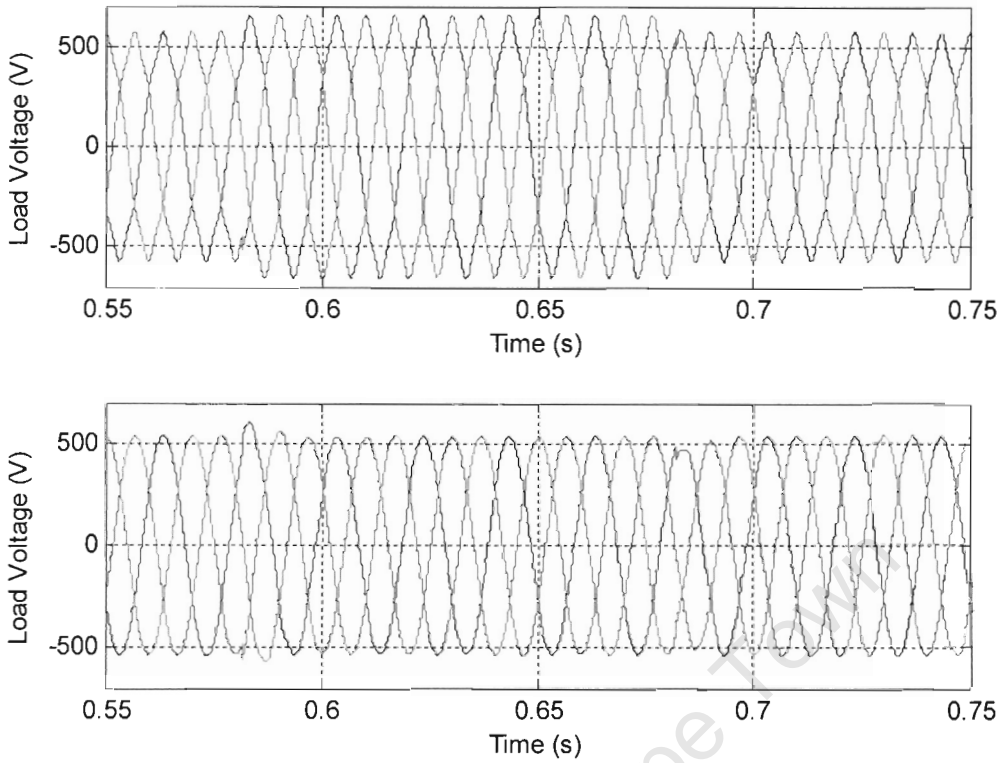

Figure 5-42: Simulated 3 phase voltages during the swell with harmonics mitigation

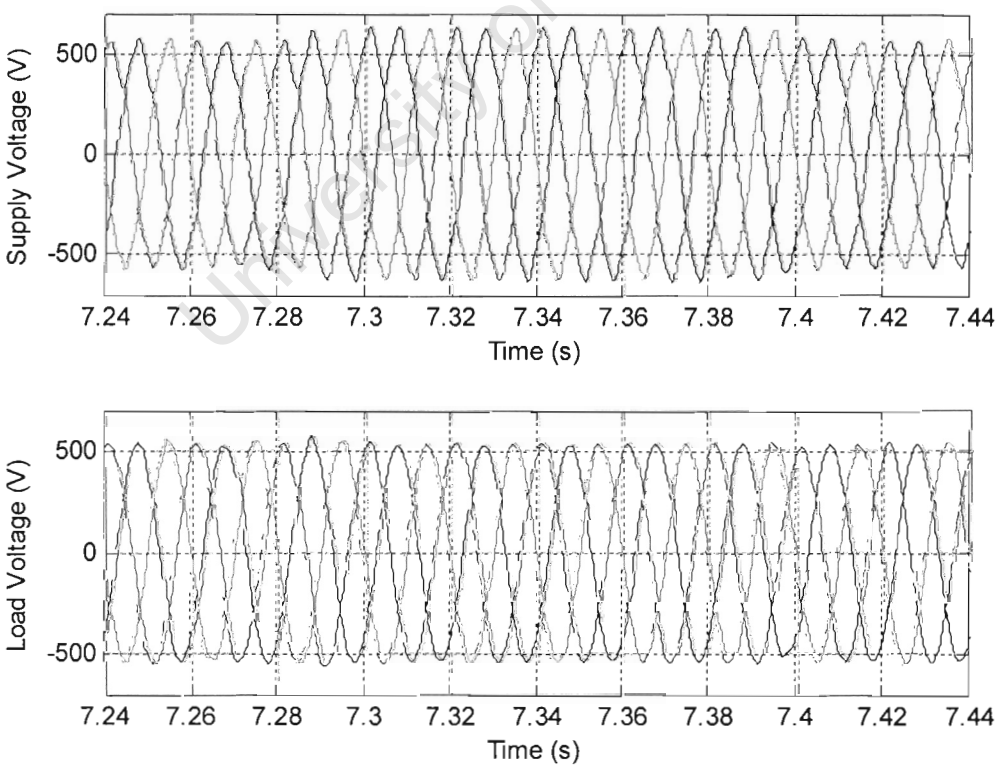

Figure 5-43: Experimental 3 phase voltages during the swell with harmonics mitigation

Figures 5.44 and 5.45 show the supply and load voltages d-components. The same observations as in section 5.4.1 are made concerning the mitigation of oscillations in $V_d(t)$ and the difference between the simulated and experimental $V_d(t)$. The overshoot in the $V_d(t)$ is due to the slow response of the device due to the filters added.

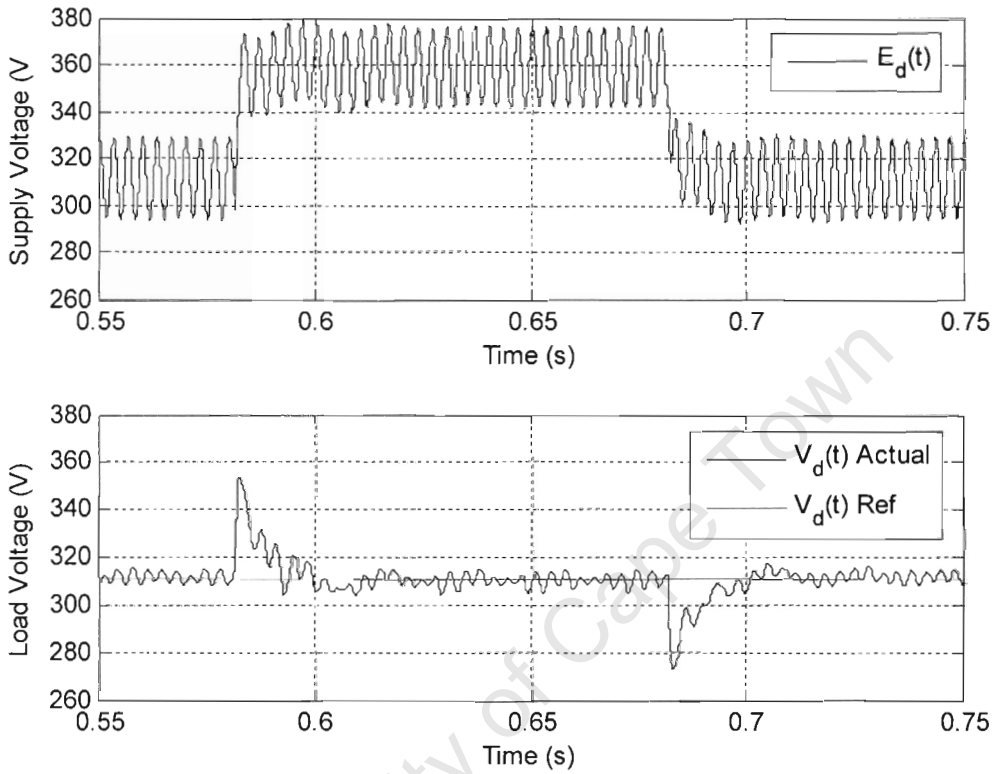

Figure 5-44: Simulated d-components during the swell with harmonics mitigation

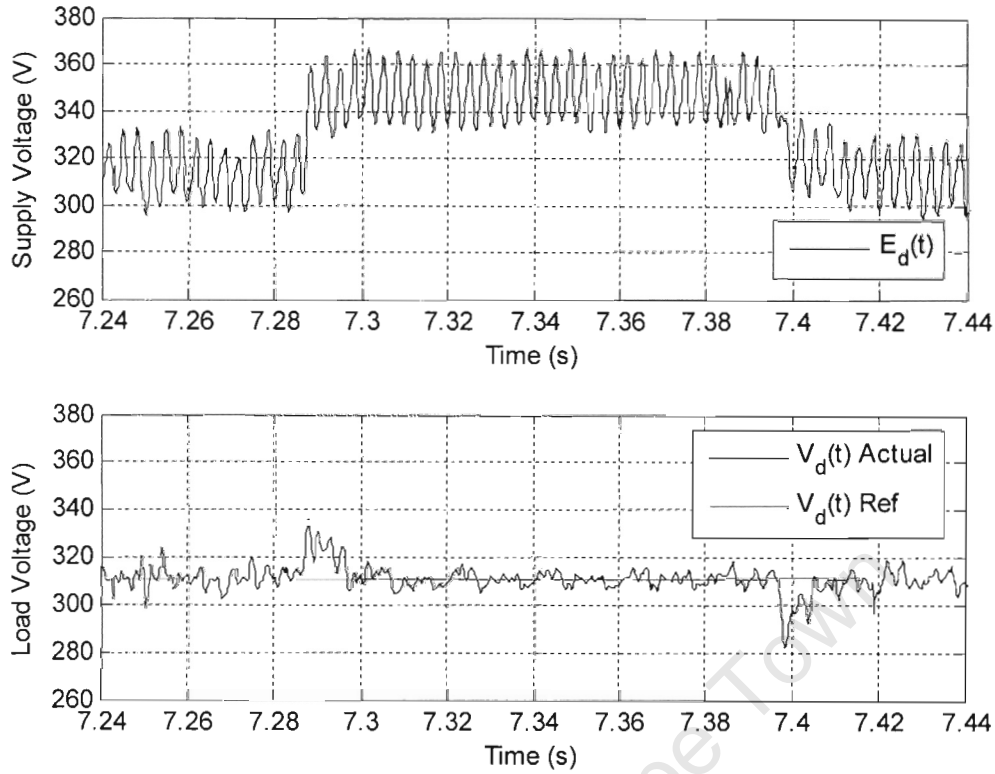

Figure 5-45: Experimental d-components during the swell with harmonics mitigation

5.4.3 Unbalanced Dip and Harmonic Mitigation

This section presents the results obtained for the final experiment – mitigation of both an unbalanced dip as well as of the 5^{th} and the 7^{th} harmonics. The same graphs as in the previous two sections are plotted. Figures 5.46 and 5.47 illustrate how the load is shielded from the dip and how the two harmonics are mitigated. A slight overshoot occurs at the end of the dip due to the delay caused by the filters but last only half a cycle and thus is not harmful to the load as indicated by the ITIC curve in figure 1.1.

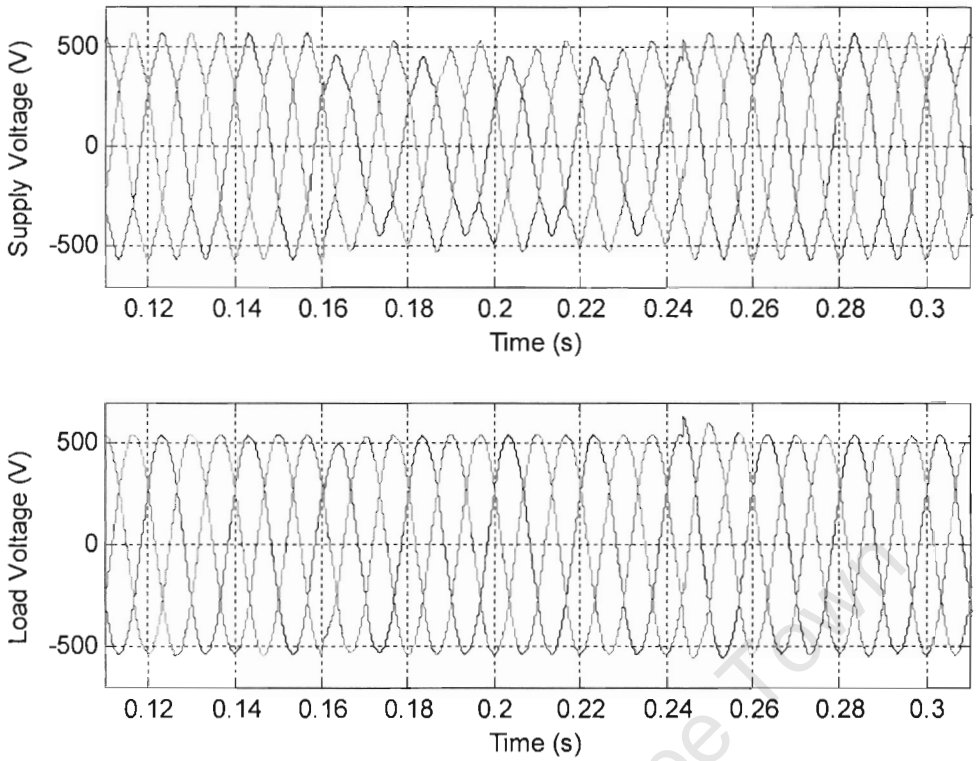

Figure 5-46: Simulated 3 phase voltages during unbalanced dip with harm. mitigation

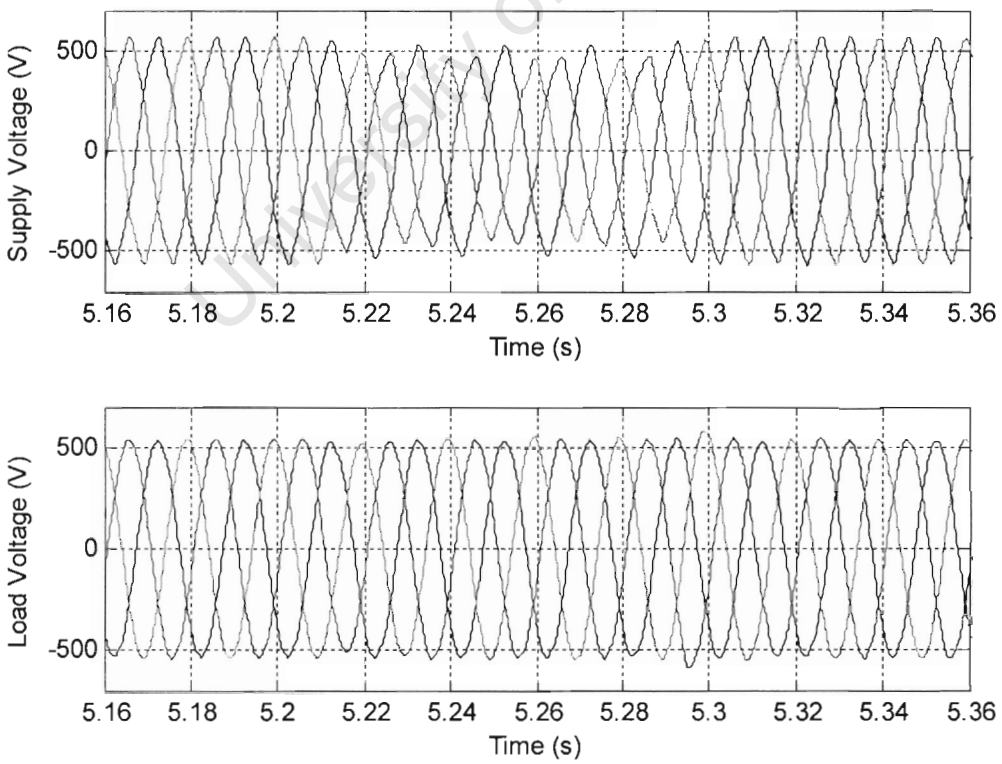

Figure 5-47: Experimental 3 phase volt. during unbalanced dip with harm. mitigation

The presence of the 5th and 7th harmonics is illustrated by the 300Hz superimposed oscillations on $E_d(t)$. The drop in the magnitude of $E_d(t)$ and presence on the 100Hz and 300Hz oscillations indicate that an unbalanced dip occurs at that time and that the 5th and 7th harmonics are still present. The efficiency of the mitigation device is demonstrated by the load voltage d-component $V_d(t)$ which is shielded from the dip, showing that it is correctly regulated. Moreover, both the 100Hz and 300Hz oscillations are reduced indicating that both the unbalance and the harmonics have been mitigated.

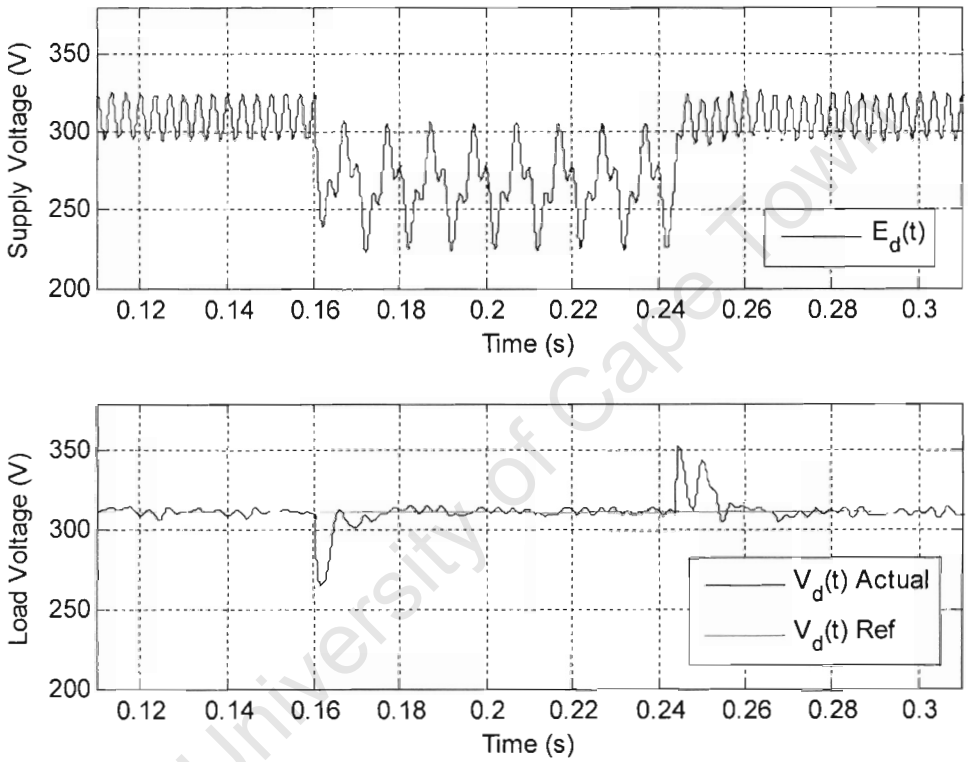

Figure 5-48: Simulated d-components during unbalanced dip with harm. mitigation

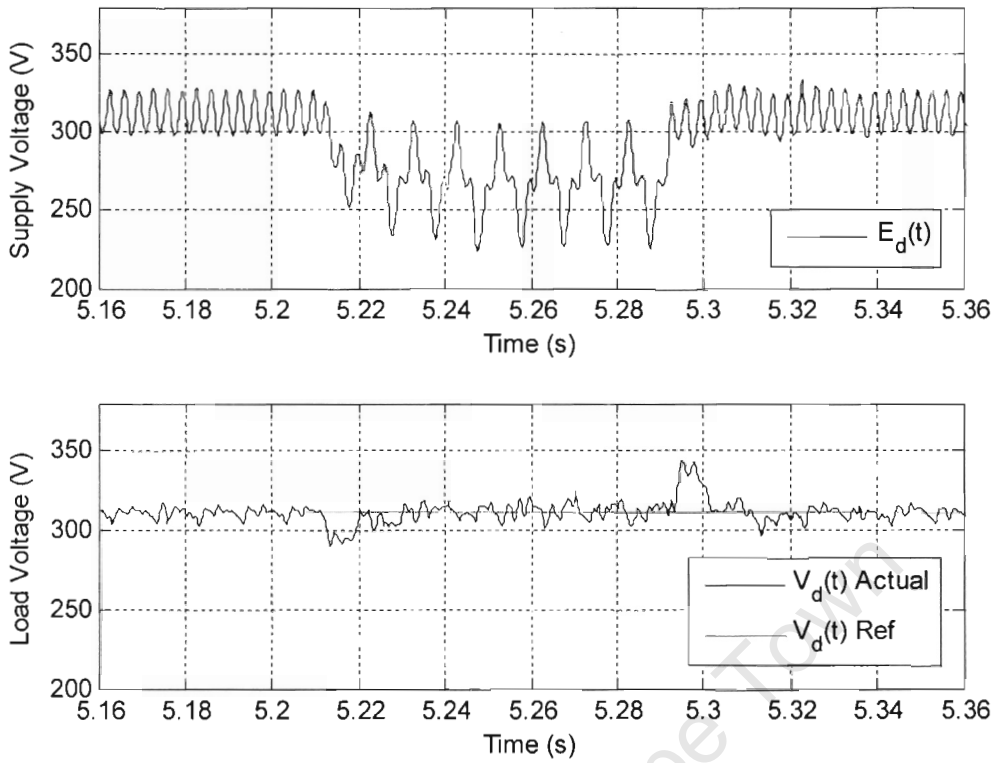

Figure 5-49: Experimental d-components during unbalanced dip with harm. mitigation

6. CONCLUSIONS

Based on the experimental results of this research, the following conclusions are drawn:

1. A mitigation device based on the UPQC configuration is designed. The need for an energy storage device is thus eliminated by using the shunt converter as an energy supply.

2. The control of the shunt converter is performed by a HCC technique instead of the preferred VOC technique due to the limitation of the DS1104 controller card. The HCC method was tested for balanced and unbalanced voltage as well as for voltage swells both in simulations and experimentally. Both DC bus regulation and bidirectional power flow at unity power factor were successfully achieved. However, the current overshoot in the hysteresis currents become large when limited to low switching frequencies generating harmonics in the supply.

3. The DVC algorithm which includes compensation for the output filter could not be implemented as it requires the measurements of 12 signals and only 8 ADC channels are available on the DS1104 Controller Card. The controllers presented in this thesis were tested both in simulations and experimentally. Mitigation of the different power quality problems was successfully achieved. However, the response of the device was slowed down by the presence of filters used to handle some undetected harmonics. These harmonics were disregarded to simplify the algorithm to maintain an acceptable sampling frequency.

4. A simple method for the compensation of the effects of the output filter is designed whereby the magnitude of some gains and phase shifts are adjusted manually. The technique works well for constant loads as shown in this thesis. However, it is not suitable if the device is used to shield a variable load.

7. RECOMMENDATIONS

Based on the experimental results and conclusions of this report, the mitigation device has met its specifications. However, it is possible to improve the control of the system to eliminate the drawbacks mentioned in the conclusions.

The drawbacks of the prototype are due to the limitation of the DS1104 Controller Card when used to control two converters simultaneously. Thus, by using two low cost embedded DSP systems, the control and response of the mitigation device can be improved greatly. With a DSP allocated to the shunt converter only, high sampling frequencies could be achieved resulting in smooth sinusoidal hysteresis currents. Alternatively, the VOC-SVPWM technique could be implemented for the shunt converter. Similarly, with the other DSP allocated exclusively to the series converter, the DVC algorithm could be applied to the positive sequence, the negative sequence as well as to all the detected harmonics, as sufficient ADC channels would be available. This modification would improve the device making it suitable for non-constant loads as well. Furthermore, the algorithm for harmonic detection could include all harmonics so as to eliminate the delay caused by the filters used to handle undetected harmonics not measured initially.

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APPENDICES

APPENDIX A :

OPEN CIRCUIT AND SHORT CIRCUIT TESTS FOR THE TRANSFORMERS

TRANSFORMER LABORATORY

Aim: To experimentally determine the parameters of the equivalent circuit of a given transformer.

1) ESTABLISHING THE TURNS RATIO OF THE TRANSFORMER

The high voltage winding of the transformer is connected to the rated 220V supply. The voltage on the secondary winding is then measured and the turns ration is calculated as follows:

$$a = \frac{N1}{N2} = \frac{V1}{V2} = \frac{220}{55} = 4$$

The operation of a transformer can be modelled by using an equivalent circuit. The equivalent circuit can be drawn as follows. (Fig. 1)

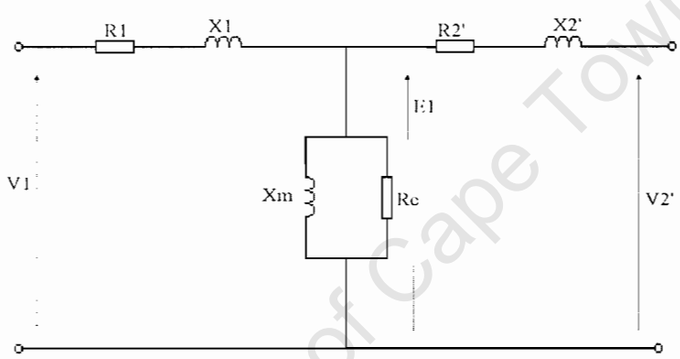


Figure 1: Transformer equivalent circuit

Since the volt drop across R1 and X1 is normally small, $|E_1| \approx |V_1|$. Based on this assumption the shunt branch can be moved to the primary side (Fig. 2). This simplifies the computation of currents, because both the exciting branch impedance and the load branch impedance are directly connected across the supply voltage. Moreover, by means of a short-circuit test and a no-load (open circuit), the parameters of the approximate equivalent circuit can be calculated.

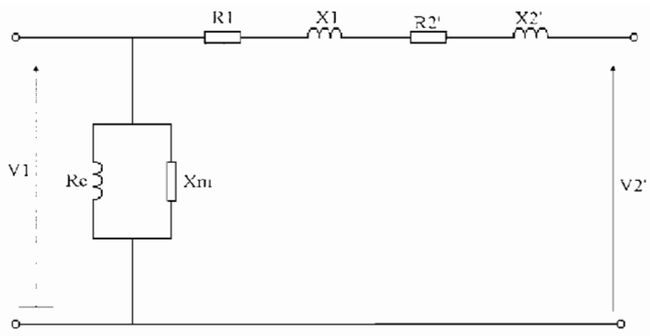


Figure 2: Transformer approximate equivalent circuit

2) SHORT CIRCUIT TEST

The approximate equivalent circuit of the transformer when its output is short circuited is shown in figure 3.

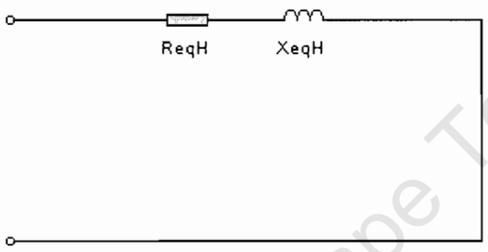


Figure 3: Equivalent circuit for short circuited low-voltage side

The rated current on the high voltage side when operating at full load is:

$$I_{Hrated} = \frac{5000}{220} = 22.72A$$

Figure 4 shows the connection of the transformer for the short circuit test. A single phase variac is used to increase the voltage on the high voltage side of the transformer until rated current flows in that winding.

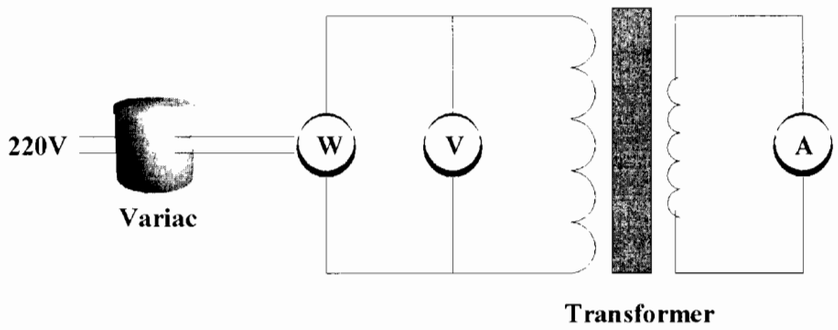


Figure 4: Connection of the transformer for short circuit test

The real power, voltage and current on the high voltage side are measured:

$I_H = 22.5A$

$V_H = 8.6V$

$P_H = 179W$

From these three measurements, the series impedance, the series resistance and the series reactance are calculated:

$P_{cu} = I_H^2 \times R_{eq H}$

$\Rightarrow R_{eq H} = \frac{179}{22.5^2} = 0.354\Omega \leftarrow$

$Z_{eq H} = \frac{V_H}{I_H} = \frac{8.6}{22.5} = 0.382\Omega$

$X_{eq H} = \sqrt{(Z_{eq H}^2 - R_{eq H}^2)} = 0.144\Omega \leftarrow$

3) OPEN CIRCUIT TEST

The approximate equivalent circuit of the transformer when its output is open circuited is shown in figure 4.

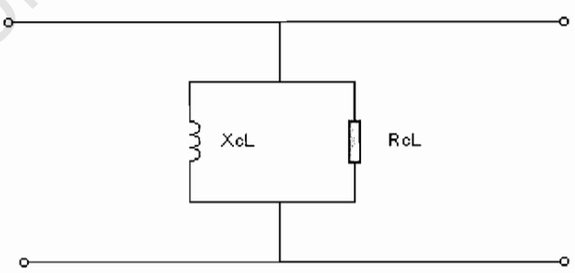


Figure 4: Equivalent circuit with high voltage side open

Figure 5 shows the connection of the transformer for the open circuit test. A single phase variac is used to apply rated voltage on the low voltage side of the transformer.

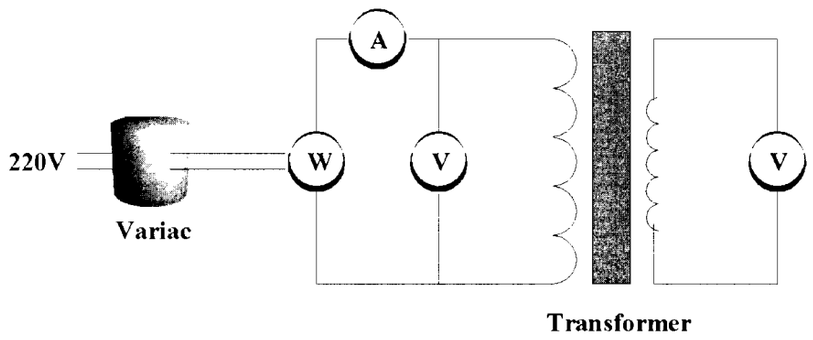


Figure 5: Connection of the transformer for open circuit test

The real power, voltage and current on the low voltage side are measured:

$I_L = 22mA$

$V_L = 55V$

$P_L = 10W$

From these three measurements, the series impedance, the magnetizing reactance and the resistance representing the core loss can be calculated:

$$P_{oc} = \frac{V_L^2}{R_{cL}}$$

$$\Rightarrow R_{cL} = \frac{55^2}{10} = 302.5\Omega \leftarrow$$

$$I_{cL} = \frac{V_L}{R_{cL}} = \frac{55}{302.5} = 0.182A$$

$$I_{mL} = \sqrt{(I_L^2 - I_{cL}^2)} = 0.124A$$

$$X_{mL} = \frac{V_L}{I_{mL}} = \frac{55}{0.123} = 444.7\Omega \leftarrow$$

The corresponding parameters for the high-voltage side are obtained as follows:

The turns ratio, $a = 4$

$R_{cH} = a^2 R_{cL} = 4840\Omega \leftarrow$

$X_{mH} = a^2 X_{mL} = 7115\Omega \leftarrow$

The equivalent circuit of the transformer referred to the high-voltage side is illustrated in figure 6.

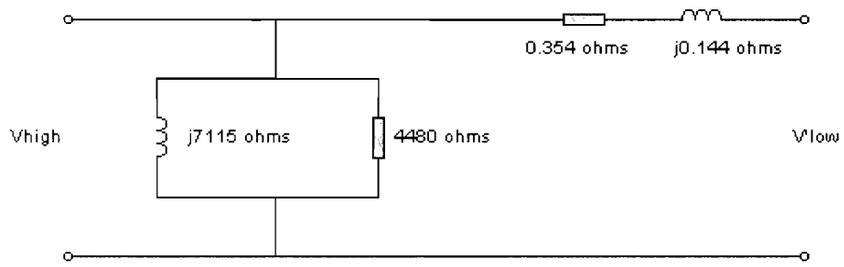


Figure 6: Equivalent circuit of the transformer referred to the high-voltage side

APPENDIX B :

IGBT MODULES

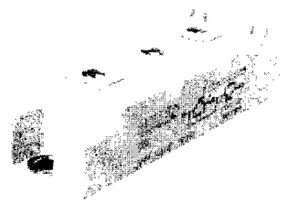
SEMIKRON

Absolute Maximum Ratings Symbol	Conditions [1]	Values ... 123 D	Units
V_{CES}		1200	V
V_{CGR}	R_{GE} = 20 kΩ	1200	V
I_C	T_{case} = 25/80 °C	50 / 40	A
I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	100 / 80	A
V_{GES}		± 20	V
P_{tot}	per IGBT, T_{case} = 25 °C	310	W
T_j, (T_{stg})		– 40 . . .+150 (125)	°C
V_{isol}	AC, 1 min.	2 500	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	40/125/56	
Diodes			
I_F= – I_C	T_{case} = 25/80 °C	50 / 40	A
I_{FM}= – I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	100 / 80	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	550	
I^2t	t_p = 10 ms; T_j = 150 °C	1500	A^2s

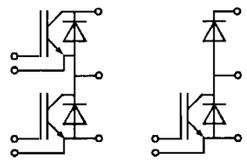
Characteristics Symbol	Conditions [1]	min.	typ.	max.	Units
$V_{(BR)CES}$	V_{GE} = 0, I_C = 1 mA	≥ V_{CES}	–	–	V
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 2 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, T_j = 25 °C	–	0,3	1	mA
	V_{CE} = V_{CES}, T_j = 125 °C	–	3	–	mA
I_{GES}	V_{GE} = 20 V, V_{CE} = 0	–	–	200	nA
V_{CEsat}	I_C = 40 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,5(3,1)	3(3,7)	V
V_{CEsat}	I_C = 50 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,7(3,5)	–	V
g_{fs}	V_{CE} = 20 V, I_C = 40 A		30	–	S
C_{CHC}	per IGBT	–	–	350	pF
C_{ies}	V_{GE} = 0	–	3300	4000	pF
C_{oes}	V_{CE} = 25 V	–	500	600	pF
C_{res}	f = 1 MHz	–	220	300	pF
L_{CE}		–	–	30	nH
$t_{d(on)}$	V_{CC} = 600 V	–	70	–	ns
t_r	V_{GE} = + 15 V / - 15 V [3]	–	60	–	ns
$t_{d(off)}$	I_C = 40 A, ind. load	–	400	–	ns
t_f	R_{Gon} = R_{Goff} = 27 Ω	–	45	–	ns
E_{on} [5]	T_j = 125 °C	–	7	–	mWs
E_{off} [5]		–	4,5	–	mWs
Diodes [8]					
V_F = V_{EC}	I_F = 40 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	1,85(1,6)	2,2	V
V_F = V_{EC}	I_F = 50 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,0(1,8)	–	V
V_{TO}	T_j = 125 °C	–	–	1,2	V
r_T	T_j = 125 °C	–	–	22	mΩ
I_{RRM}	I_F = 40 A; Tj = 25 (125) °C [2]	–	23(35)	–	A
Q_{rr}	I_F = 40 A; T_j = 25 (125) °C [2]	–	2,3(7)	–	µC
Thermal Characteristics					
R_{thjc}	per IGBT	–	–	0,4	°C/W
R_{thjc}	per diode	–	–	0,7	°C/W
R_{thch}	per module	–	–	0,05	°C/W

SEMITRANS® M IGBT Modules

SKM 50 GB 123 D
SKM 50 GAL 123 D



SEMITRANS 2



GB GAL

Features

- MOS input (voltage controlled)
- N channel, Homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 * I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes [8]
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (10 mm) and creepage distances (20 mm).

Typical Applications: → **B 6 - 85**

- Three phase inverter drives
- Switching (not for linear use)

1) T_{case} = 25 °C, unless otherwise specified
2) I_F = – I_C, V_R = 600 V, – di_F/dt = 800 A/µs, V_{GE} = 0 V
3) Use V_{GEoff} = -5 ... -15 V
5) See fig. 2 + 3; R_{Goff} = 27 Ω
8) CAL = Controlled Axial Lifetime Technology.

Case and mech. data → **B 6 - 86**
SEMITRANS 2

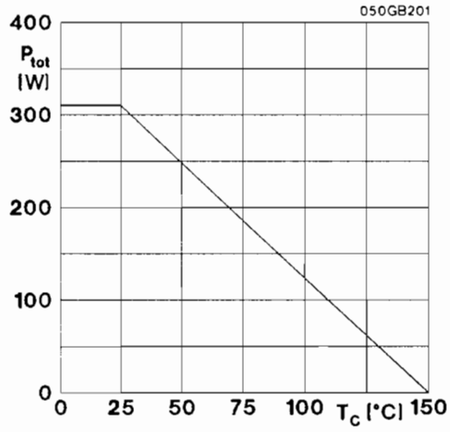
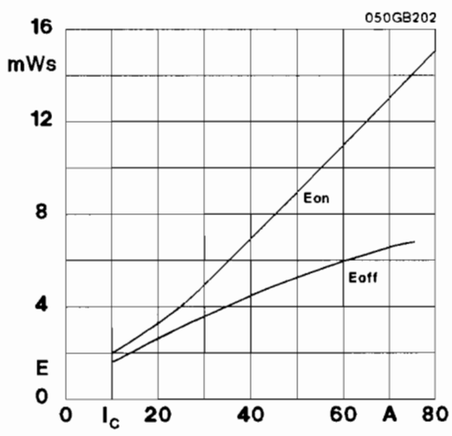
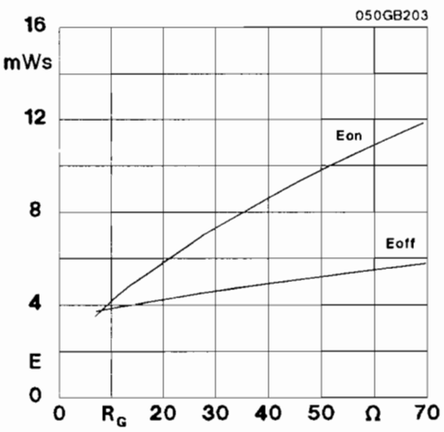


Fig. 1 Rated power dissipation P_{tot} = f (T_C)



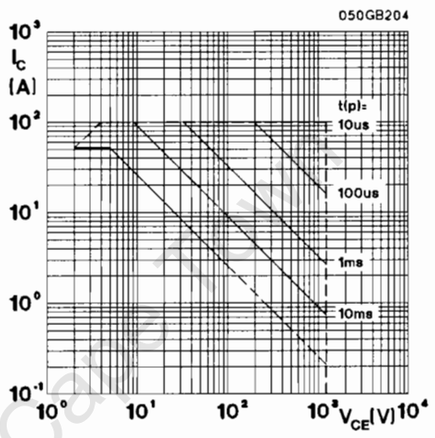
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_G = 27 Ω

Fig. 2 Turn-on /-off energy = f (I_C)



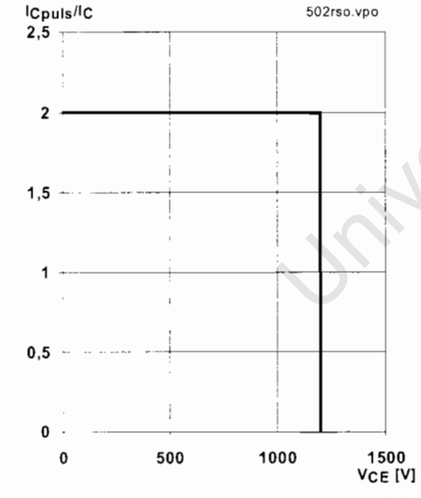
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 40 A

Fig. 3 Turn-on /-off energy = f (R_G)



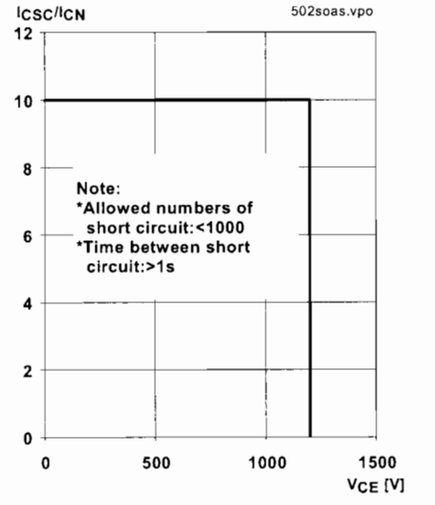
1 pulse
T_C = 25 °C
$T_j \leq$ 150 °C

Fig. 4 Maximum safe operating area (SOA) I_C = f (V_{CE})



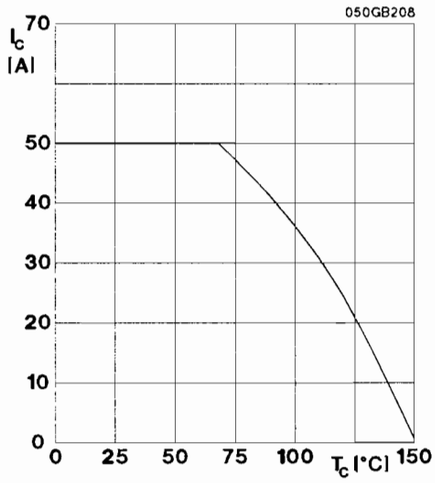
$T_j \leq$ 150 °C
V_{GE} = ± 15 V
R_{Goff} = 27 Ω
I_C = 40 A

Fig. 5 Turn-off safe operating area (RBSOA)



$T_j \leq$ 150 °C
V_{GE} = ± 15 V
$t_{sc} \leq$ 10 µs
L < 25 nH
I_{CN} = 40 A

Fig. 6 Safe operating area at short circuit I_C = f (V_{CE})



T_j = 150 °C
$V_{GE} \geq$ 15 V

Fig. 8 Rated current vs. temperature $I_C = f(T_C)$

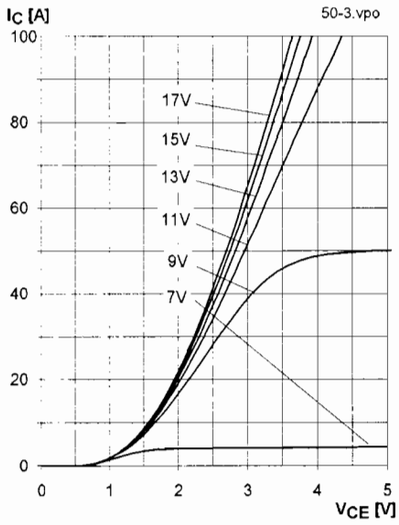


Fig. 9 Typ. output characteristic, t_p = 80 µs; 25 °C

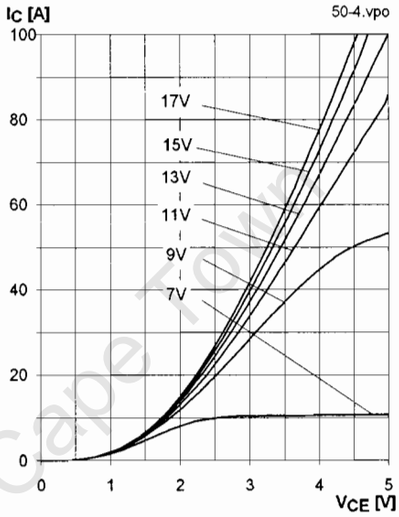


Fig. 10 Typ. output characteristic, t_p = 80 µs; 125 °C

$P_{cond(t)} = V_{CEsat(t)} \cdot I_{C(t)}$

$V_{CEsat(t)} = V_{CE(TO)(Tj)} + r_{CE(Tj)} \cdot I_{C(t)}$

$V_{CE(TO)(Tj)} \leq 1{,}5 + 0{,}002\ (T_j - 25)$ [V]

typ.: $r_{CE(Tj)} = 0{,}02 + 0{,}00008\ (T_j - 25)$ [Ω]

max.: $r_{CE(Tj)} = 0{,}03 + 0{,}00010\ (T_j - 25)$ [Ω]

valid for $V_{GE} = +15\ ^{+2}_{-1}$ [V]; $I_C > 0{,}3\ I_{Cnom}$

Fig. 11 Saturation characteristic (IGBT)
Calculation elements and equations

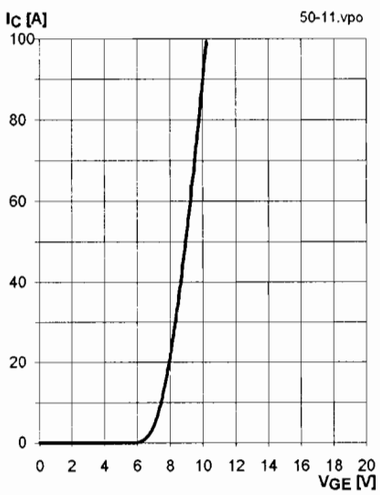
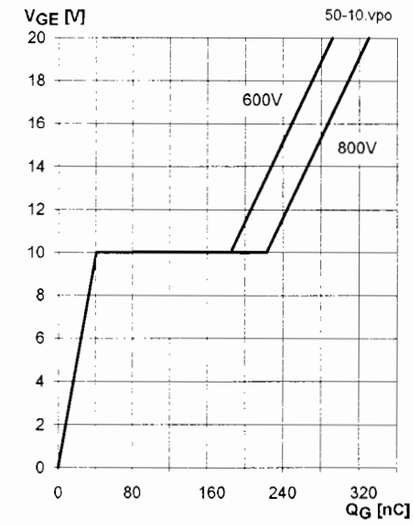
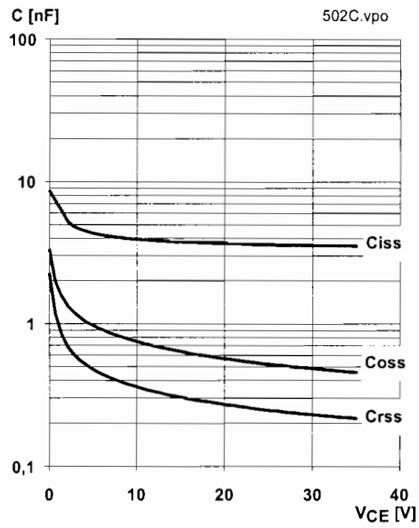


Fig. 12 Typ. transfer characteristic, t_p = 80 µs; V_{CE} = 20 V



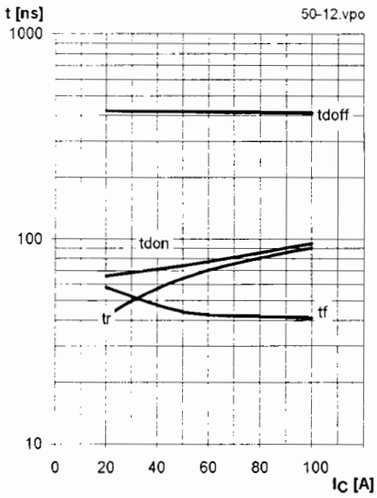
I_{Cpuls} = 50 A

Fig. 13 Typ. gate charge characteristic



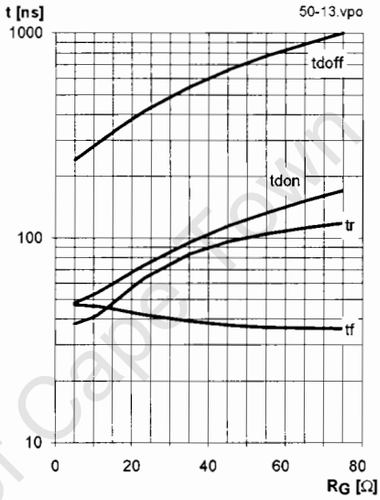
V_{GE} = 0 V
f = 1 MHZ

Fig. 14 Typ. capacitances vs.V_{CE}



T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_{Gon} = 27 Ω
R_{Goff} = 27 Ω
induct. load

Fig. 15 Typ. switching times vs. I_C



T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 40 A
induct. load

Fig. 16 Typ. switching times vs. gate resistor R_G

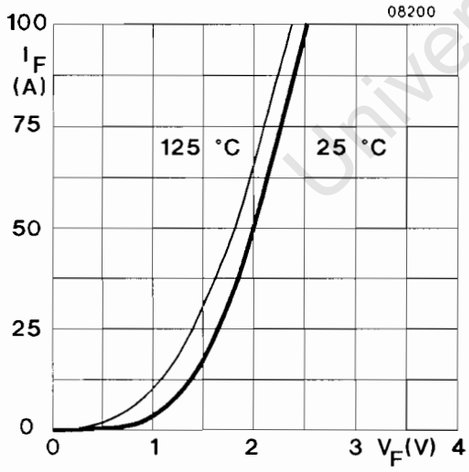


Fig. 17 Typ. CAL diode forward characteristic

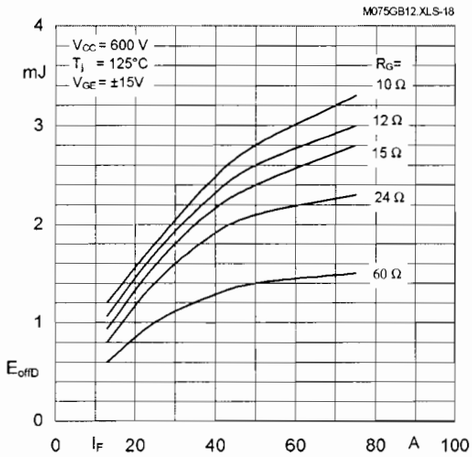


Fig. 18 Diode turn-off energy dissipation per pulse

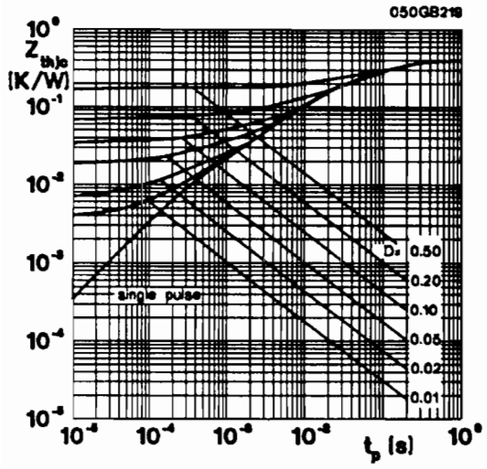


Fig. 19 Transient thermal impedance of IGBT
$Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

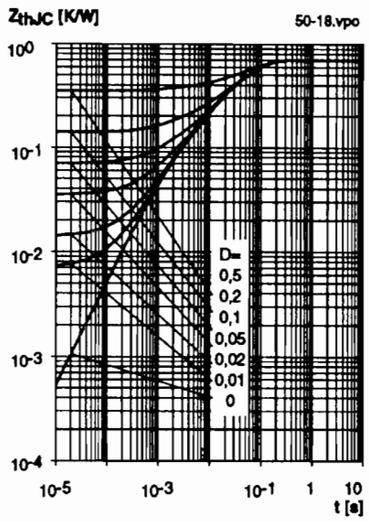


Fig. 20 Transient thermal impedance of inverse CAL diodes $Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

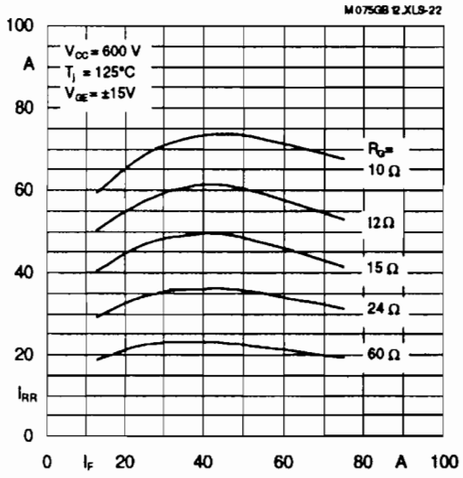


Fig. 22 Typ. CAL diode peak reverse recovery current
$I_{RR} = f(I_F, R_G)$

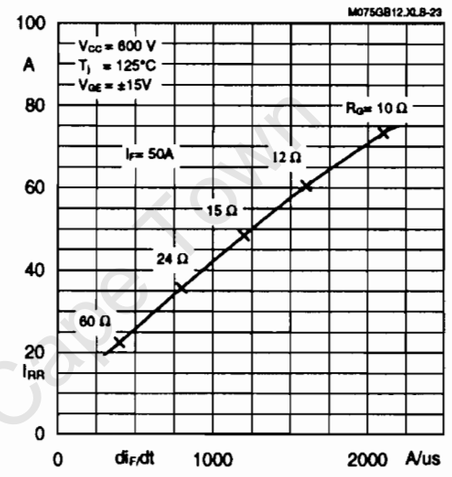


Fig. 23 Typ CAL diode peak reverse recovery current
$I_{RR} = f(di/dt)$

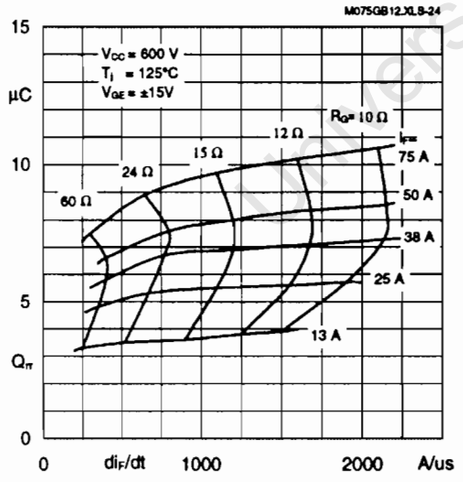


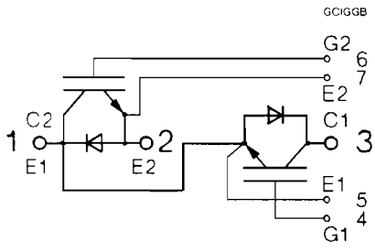
Fig. 24 Typ. CAL diode recovery charge

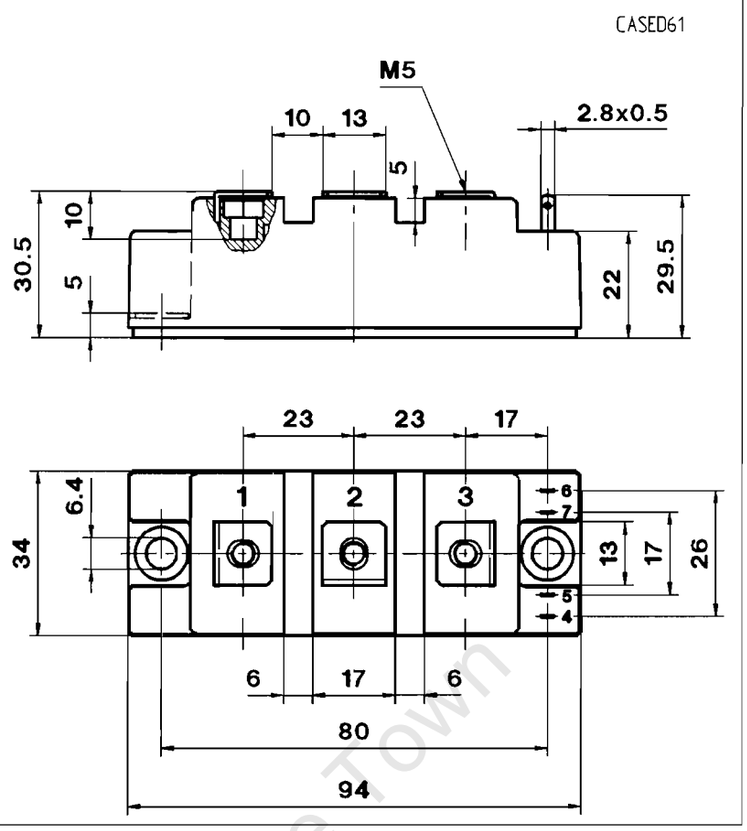
Typical Applications

Include

Switched mode power supplies
DC servo and robot drives
Inverters
DC choppers
AC motor speed control
Inductive heating
UPS Uninterruptable power supplies
General power switching applications
Electronic (also portable) welders
Pulse frequencies also above 15 kHz

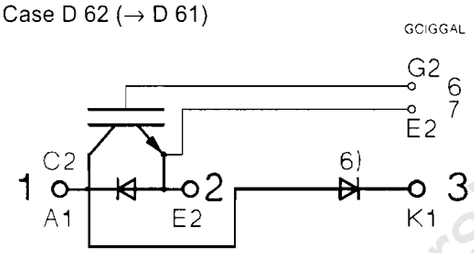
SEMITRANS 2
Case D 61
UL Recognized
File no. E 63 532
SKM 50 GB 123 D





Dimensions in mm

SKM 50 GAL 123 D
Case D 62 (→ D 61)



Case outline and circuit diagrams

Mechanical Data

Symbol	Conditions		Values min.	typ.	max.	Units
M_1	to heatsink, SI Units	(M6)	3	–	5	Nm
	to heatsink, US Units		27	–	44	lb.in.
M_2	for terminals, SI Units	(M5)	2,5	–	5	Nm
	for terminals US Units		22	–	44	lb.in.
a			–	–	5x9,81	m/s^2
w			–	–	160	g

This is an electrostatic discharge sensitive device (ESDS). Please observe the international standard IEC 747-1, Chapter IX.

Eight devices are supplied in one SEMIBOX A without mounting hardware, which can be ordered separately under Ident No. 33321100 (for 10 SEMITRANS 2)
Larger packaging units of 20 or 42 pieces are used if suitable
Accessories → B 6 – 4.
SEMIBOX → C – 1.

APPENDIX C :

SKHI22A DRIVER MODULES

SEMIKRON

Absolute Maximum Ratings

Symbol	Term		Values	Units
V_S	Supply voltage prim.		18	V
V_{iH}	Input signal volt. (High)	SKHIxxA	V_S + 0,3	V
		SKHI22B	5 + 0,3	V
$Iout_{PEAK}$	Output peak current		8	A
$Iout_{AVmax}$	Output average current		40	mA
f_{max}	max. switching frequency		50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT		1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side		50	kV/µs
V_{isolIO}	Isolation test voltage	Standard	2500	Vac
	input-output (2 sec.AC)	Version „H4"	4000	Vac
V_{isol12}	Isolation test voltage ouput 1 - output 2 (2 sec.AC)		1500	V
R_{Gonmin}	Minimum rating for R_{Gon}		3	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}		3	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse		4 [1]	µC
T_{op}	Operating temperature		- 40... + 85	°C
T_{stg}	Storage temperature		- 40... + 85	°C

Electrical Characteristics (T_a = 25 °C)

Symbol	Term		Values min.	typ.	max.	Units
V_S	Supply voltage primary side		14,4	15	15,6	V
I_{SO}	Supply current primary side (no load)		–	80	–	mA
	Supply current primary side (max.)		–	–	290	mA
V_i	Input signal voltage	SKHIxxA on/off	–	15 / 0	–	V
		SKHI22B on/off	–	5 / 0	–	V
V_{iT+}	Input threshold voltage (High)	SKHIxxA	10,9	11,7	12,5	V
		SKHI22B	3,5	3,7	3,9	V
V_{iT-}	Input threshold voltage (Low)	SKHIxxA	4,7	5,5	6,5	V
		SKHI22B	1,5	1,75	2,0	V
R_{in}	Input resistance	SKHIxxA	–	10	–	kΩ
		SKHI22B	–	3,3	–	kΩ
$V_{G(on)}$	Turn on gate voltage output		–	+15	–	V
$V_{G(off)}$	Turn off gate voltage output	SKHI22x	–	-7	–	V
		SKHI21A	–	0	–	V
R_{GE}	Internal gate-emitter resistance		–	22	–	kΩ
f_{ASIC}	Asic system switching frequency		–	8	–	MHz
$t_{d(on)IO}$	Input-output turn-on propagation time		0,85	1	1,15	µs
$t_{d(off)IO}$	Input-output turn-off propagation time		0,85	1	1,15	µs
$t_{d(err)}$	Error input-output propagation time		–	0,6	–	µs
$t_{pERRRESET}$	Error reset time		–	9	–	µs
t_{TD}	Top-Bot Interlock Dead Time	SKHIxxA	3,3	–	4,3	µs
		SKHI22B	0	–	4,3	µs
V_{CEstat}	Reference voltage for V_{CE}-monitoring		–	5 [2]	10	V
			–	6 [3]	10	V
C_{ps}	Coupling capacitance primary secondary		–	12	–	pF
MTBF	Mean Time Between Failure T_a = 40° C		–	2,0	–	10^6 h
m	weight		–	45	–	g

SEMIDRIVER®
Hybrid Dual IGBT Driver
SKHI 22 A / B

- Double driver for halfbridge IGBT modules
- SKHI 22 A/B H4 is for 1700 V-IGBT
- SKHI 22 A is compatible to old SKHI 22
- SKHI 22 B has additional functionality

Hybrid Dual MOSFET Driver
SKHI 21 A

- drives MOSFETs with $V_{DS(on)}$ < 10 V
- is compatible to old SKHI 21

Preliminary Data

Features

- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and switch off
- Drive interlock top/bottom
- Isolation by transformers
- Supply undervoltage protection (13 V)
- Error latch/output

Typical Applications

- Driver for IGBT and MOSFET modules in bridge circuits in choppers, inverter drives, UPS and welding inverters
- DC bus voltage up to 1200V

[1] see fig. 6
[2] At R_{CE} = 18 kΩ, C_{CE} = 330pF
[3] At R_{CE} = 36 kΩ, C_{CE} = 470pF, R_{VCE} = 1kΩ

External Components

Component	Function	Recommended Value
R_{CE}	Reference voltage for V_{CE}-monitoring $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}4$ (1) with R_{VCE} = 1kΩ (1700V IGBT): $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}8$ (1.1)	10kΩ < R_{CE} < 100kΩ 18kΩ for SKM XX 123 (1200V) 36kΩ for SKM XX 173 (1700V)
C_{CE}	Inhibit time for V_{CE} - monitoring $t_{min} = \tau_{CE} \cdot \ln\left[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)}\right]$ (2) $\tau_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$ (3)	C_{CE} < 2,7nF 0,33nF for SKM XX 123 (1200V) 0,47nF for SKM XX 173 (1700V) 0,5µs < t_{min} < 10µs
R_{VCE}	Collector series resistance for 1700V IGBT-operation	1kΩ / 0,4W
R_{ERROR}	Pull-up resistance at error output $\frac{U_{Pull-Up}}{R_{ERROR}} < 15mA$	1kΩ < R_{ERROR} < 10kΩ
R_{GON}	Turn-on speed of the IGBT [4]	R_{GON} > 3Ω
R_{GOFF}	Turn-off speed of the IGBT [5]	R_{GOFF} > 3Ω

[4] Higher resistance reduces free-wheeling diode peak recovery current, increases IGBT turn-on time.
[5] Higher resistance reduces turn-off peak voltage, increases turn-off time and turn-off power dissipation

PIN array

Fig. 2 shows the pin arrays. The input side (primary side) comprises 10 inputs (SKHI 22A / 21A 8 inputs), forming the interface to the control circuit (see fig.1).

The output side (secondary side) of the hybrid driver shows two symmetrical groups of pins with 4 outputs, each forming the interface to the power module. All pins are designed for a grid of 2,54 mm.

Primary side PIN array

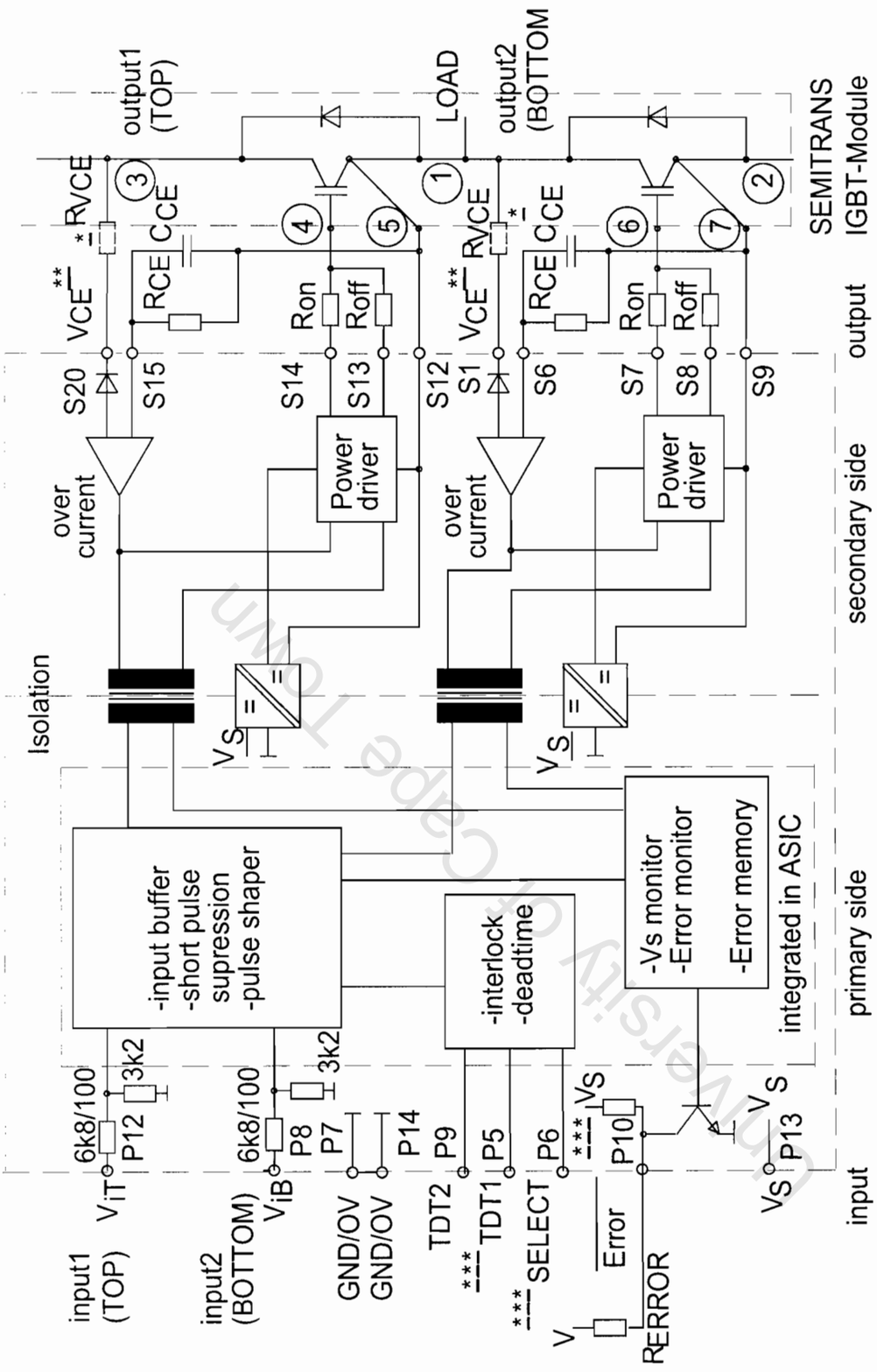
PIN No.	Designation	Explanation
P14	GND / 0V	related earth connection for input signals
P13	V_S	+ 15V ± 4% voltage supply
P12	V_{IN1}	switching signal input 1 (TOP switch) positive 5V logic (for SKHI22A /21A, 15V logic)
P11	free	not wired
P10	/ERROR	error output, low = error; open collector output; max 30V / 15mA (for SKHI22A /21A, internal 10kΩ pull-up resistor versus V_S)
P9	TDT2	signal input for digital adjustment of interlocking time; **SKHI22B: to be switched by bridge to GND (see fig. 3)** **SKHI22A /21A: to be switched by bridge to V_S**
P8	V_{IN2}	switching signal input 2 (BOTTOM switch); positive 5V logic (for SKHI22A /21A, 15V logic)
P7	GND / 0V	related earth connection for input signals
P6	SELECT	signal input for neutralizing locking function; to be switched by bridge to GND
P5	TDT1	signal input for digital adjustment of locking time; to be switched by bridge to GND

ATTENTION: Inputs P6 and P5 are not existing for SKHI 22A/ 21A. The contactor tracks of the digital input signals P5/ P6/ P9 must not be longer than 20 mm to avoid interferences, if no bridges are connected.

Secondary side PIN array

PIN No.	Designation	Explanation
S20	V_{CE1}	collector output IGBT 1 (TOP switch)
S15	C_{CE1}	reference voltage adjustment with R_{CE} and C_{CE}
S14	G_{ON1}	gate 1 R_{ON} output
S13	G_{OFF1}	gate 1 R_{OFF} output
S12	E1	emitter output IGBT 1 (TOP switch)
S1	V_{CE2}	collector output IGBT 2 (BOTTOM switch)
S6	C_{CE2}	reference voltage adjustment with R_{CE} and C_{CE}
S7	G_{ON2}	gate 2 R_{ON} output
S8	G_{OFF2}	gate 2 R_{OFF} output
S9	E2	emitter output IGBT 2 (BOTTOM switch)

ATTENTION: The connector leads to the power module should be as short as possible.



* When SKHI22B is driving 1700V IGBTs, a 1kΩ / 0,4W R_{VCE}-resistor must be connected in series to the V_{CE} input.
** The VCE-terminal is to be connected to the IGBT collector C. If the V_{CE}-monitoring is not used, connect S1 to S9 or S20 to S12 respectively.
*** Terminals P5 and P6 are not existing for SKHI22A/21A; internal pull-up resistor exists in SKHI22A/21A only.
1-7 Connections to SEMITRANS GB-module

Fig. 1 Block diagram of SKHI 22 A / B / 21 A

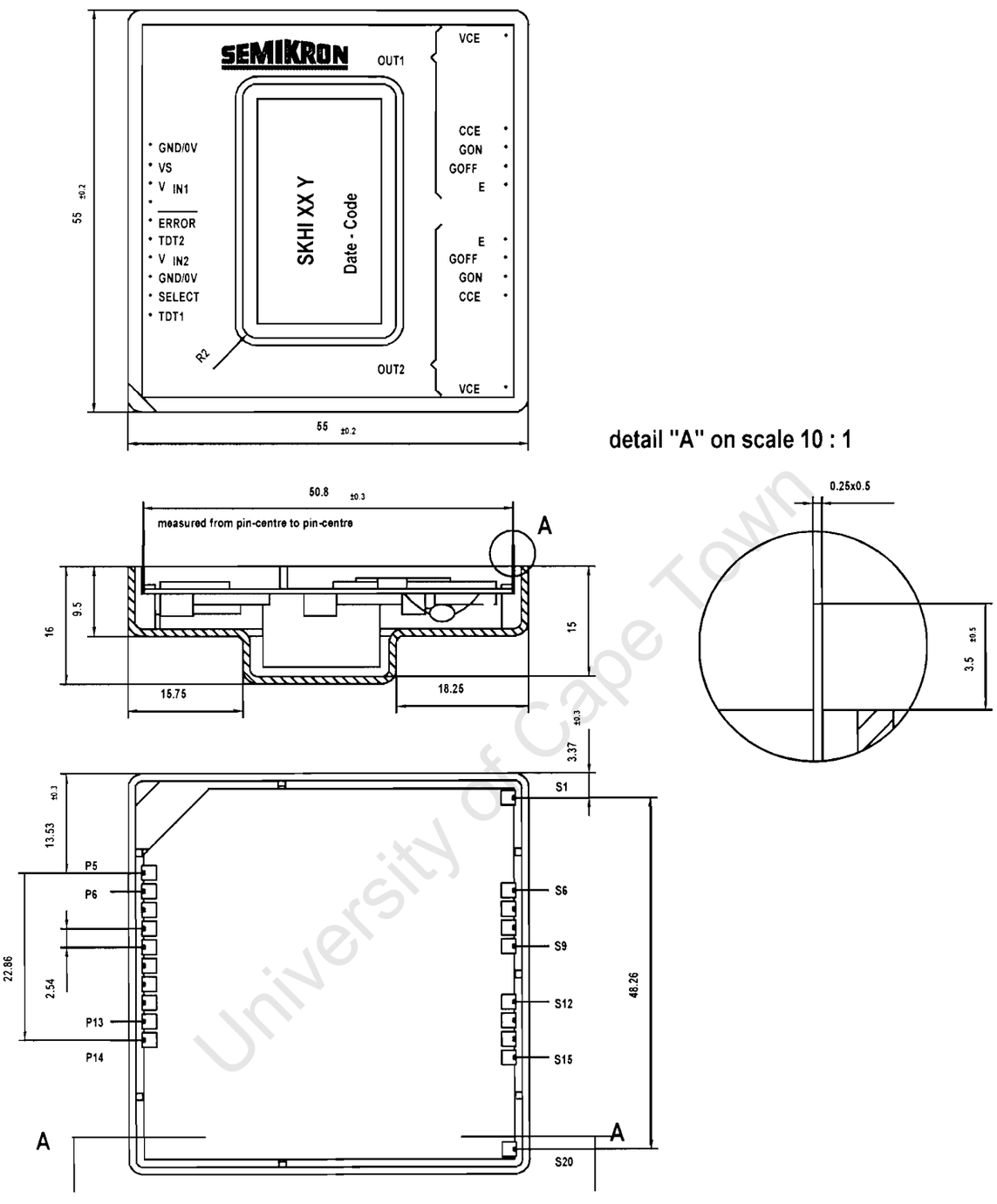


Fig. 2 Dimension drawing and PIN array (P5 and P6 are not existing for SKHI22A/21A)

SEMIDRIVER®

SKHI 22A / 22B und SKHI 21A

Hybrid dual drivers

The driver generation SKHI 22A/B and SKHI 21A will replace the hybrid drivers SKHI 21/22 and is suitable for all available low and medium power range IGBT and MOSFETs.

The SKHI 22A (SKHI 21A) is a form-, fit- and mostly function-compatible replacement to its predecessor, the SKHI 22 (SKHI 21).

The SKHI 22B is recommended for any new development. It has two additional signal pins on the primary side with which further functions may be utilized.

The SKHI 22A and SKHI 22B are available with standard isolation (isolation testing voltage 2500 VAC, 1min) as well as with an increased isolation voltage (type "H4") (isolation testing voltage 4000 VAC, 1min). The SKHI 21A is only offered with standard isolation features.

Differences SKHI 22-22A (SKHI 21-21A)

Compared to the old SKHI 22/21 the new driver SKHI 22A / 21A is absolutely compatible with regards to pins and mostly with regards to functions. It may be equivalently used in existing PCBs.

The following points have to be considered when exchanging the drivers:

- **Leave out the two resistors RTD for interlocking dead time adjustment at pin 11 and pin 9.**
- **The interlocking time of the driver stages in halfbridge applications is adjusted to 3,25 µs. It may be increased up to 4,25 µs by applying a 15 V (VS) supply voltage at Pin 9 (TDT2) (wire bridge)**
- **The error reset time is typically 9µs.**
- **The input resistance is 10 kΩ.**

As far as the SKHI 22A is concerned, the negative gate voltage required for turn-off of the IGBT is no longer -15V, but -7V.

General description

The new driver generation SKHI 22A/B, SKHI 21A consists of a hybrid component which may directly be mounted to the PCB.

All devices necessary for driving, voltage supply, error monitoring and potential separation are integrated in the driver. In order to adapt the driver to the used power module, only very few additional wiring may be necessary.

The forward voltage of the IGBT is detected by an integrated short-circuit protection, which will turn off the module when a certain threshold is exceeded.

In case of short-circuit or too low supply voltage the integrated error memory is set and an error signal is generated.

The driver is connected to a controlled + 15 V-supply voltage. The input signal level is 0/15 V for the SKHI 22A/ 21A and 0/5 V for the SKHI 22B.

In the following explanations the whole driver family will be designated as SKHI 22B. If a special type is referred to, the concerned driver version will explicitly be named.

Technical explanations[1]

Description of the circuit block diagram and the functions of the driver

The block diagram (fig.1) shows the inputs of the driver (primary side) on the left side and the outputs (secondary side) on the right.

The following functions are allocated to the primary side:

Input-Schmitt-trigger, CMOS compatible, positive logic (input high = IGBT on)

Interlock circuit and deadtime generation of the IGBT

If one IGBT is turned on, the other IGBT of a halfbridge cannot be switched. Additionally, a digitally adjustable interlocking time is generated by the driver (see fig. 3), which has to be longer than the turn-off delay time of the IGBT. This is to avoid that one IGBT is turned on before the other one is not completely discharged. This protection-function may be neutralized by switching the select input (pin6) (see fig. 3). fig. 3 documents possible interlock-times. "High" value can be achieved with no connection and connection to 5 V as well.

P6 ; SELECT	P5 ; TDT1	P9 ; TDT2	interlock time t_{TD}/µs
open / 5V	GND	GND	1,3
open / 5V	GND	open / 5V	2,3
open / 5V	open / 5V	GND	3,3
open / 5V	open / 5V	open / 5V	4,3
GND	X	X	no interlock

Fig. 3 SKHI 22B - Selection of interlock-times: „High"-level can be achieved by no connection or connecting to 5 V

Short pulse suppression

The integrated short pulse suppression avoids very short switching pulses at the power semiconductor caused by high-frequency interference pulses at the driver input signals. Switching pulses shorter than 500 ns are suppressed and not transmitted to the IGBT.

Power supply monitoring (V_S)

A controlled 15 V-supply voltage is applied to the driver. If it falls below 13 V, an error is monitored and the error output signal switches to low level.

1. The following descriptions apply to the use of the hybrid driver for IGBTs as well as for power MOSFETs. For the reason of shortness, only IGBTs will be mentioned in the following. The designations "collector" and "emitter" will refer to IGBTs, whereas for the MOSFETs "drain" and "source" are to be read instead.

Error monitoring and error memory

The error memory is set in case of under-voltage or short-circuit of the IGBTs. In case of short-circuit, an error signal is transmitted by the V_{CE}-input via the pulse transformers to the error memory. The error memory will lock all switching pulses to the IGBTs and trigger the error output (P10) of the driver. The error output consists of an open collector transistor, which directs the signal to earth in case of error. SEMIKRON recommends the user to provide for a pull-up resistor directly connected to the error evaluation board and to adapt the error level to the desired signal voltage this way. The open collector transistor may be connected to max. 30 V / 15 mA. If several SKHI 22Bs are used in one device, the error terminals may also be paralleled.

ATTENTION: Only the SKHI 22A / 21A is equipped with an internal pull-up resistor of 10 kΩ versus V_S. The SKHI 22B does not contain an internal pull-up resistor.

The error memory may only be reset, if no error is pending and both cycle signal inputs are set to low for > 9 µs at the same time.

Pulse transformer set

The transformer set consists of two pulse transformers one is used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between primary and secondary side, the other one for the DC/DC-converter. The DC/DC-converter serves as potential-separation and power supply for the two secondary sides of the driver. The isolation voltage for the "H4"-type is 4000 V_{AC} and 2500 V_{AC} for all other types.

The secondary side consists of two symmetrical driver switches integrating the following components:

Supply voltage

The voltage supply consists of a rectifier, a capacitor, a voltage controller for - 7 V and + 15 V and a + 10 V reference voltage.

Gate driver

The output transistors of the power drivers are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed by the external resistors R_{ON} and R_{OFF}. Do not connect the terminals S7 with S8 and S13 with S14, respectively. The IGBT is turned on by the driver at + 15 V by R_{ON} and turned off at - 7 V by R_{OFF}. R_{ON} and R_{OFF} may not chosen below 3 Ω. In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a 22 kΩ-resistor versus the emitter output (E) has been integrated at output G_{OFF}.

V_{CE}-monitoring

The V_{CE}-monitoring controls the collector-emitter voltage V_{CE} of the IGBT during its on-state. V_{CE} is internally limited to 10 V. If the reference voltage V_{CEref} is exceeded, the IGBT will be switched off and an error is indicated. The reference voltage V_{CEref} may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in the steady state. This value will, however, be reset, when the IGBT is turned off. V_{CEstat} is the steady-state value of V_{CEref} and is adjusted to the required maximum value for each IGBT by an external resistor R_{CE} to be connected between the terminals C_{CE} (S6/S15) and E (S9/S12). It may not exceed 10 V. The time constant for the delay of V_{CEref} may be increased by an external capacitor C_{CE}, which is connected in parallel to R_{CE}. It controls the time tmin which passes after turn-on of the IGBT before the V_{CE}-monitoring is activated. This makes possible any adaptation to the switching behavior of any of the IGBTs. After t_{min} has passed, the V_{CE}-monitoring will be triggered as soon as $V_{CE} > V_{CEref}$ and will turn off the IGBT.

External components and possible adjustments of the hybrid driver

Fig. 1 shows the required external components for adjustment and adaptation to the power module.

VCE - monitoring adjustment

The external components R_{CE} and C_{CE} are applied for adjusting the steady-state threshold and the short-circuit monitoring dynamic. R_{CE} and C_{CE} are connected in parallel to the terminals C_{CE} (S15/ S6) and E (S12/ S9) .

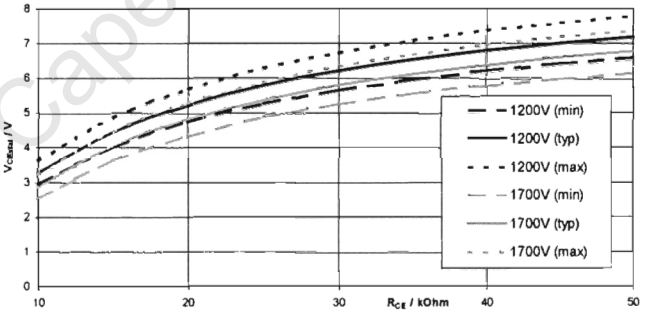


Fig. 4 V_{CEstat} in dependence of R_{CE} (T_{amb} = 25°C)

Dimensioning of R_{CE} and C_{CE} can be done in three steps:

1. Calculate the maximum forward voltage from the datasheet of the used IGBT and determine V_{CEstat}
2. Calculate approximate value of R_{CE} according to equation (1) or (1.1) from V_{CEstat} or determine R_{CE} by using fig.4.
3. Determine t_{min} and calculate C_{CE} according to equations (2) and (3).

Typical values are

for 1200 V IGBT: V_{CEstat} = 5 V; t_{min} = 1,45 µs,
R_{CE} = 18 kΩ, C_{CE} = 330 pF

for 1700 V IGBT: V_{CEstat} = 6 V; t_{min} = 3 µs,
R_{CE} = 36 kΩ, C_{CE} = 470 pF

Adaptation to 1700 V IGBT

When using 1700 V IGBTs it is necessary to connect a 1 kΩ / 0,4 W adaptation resistor between the V_{CE}-terminal (S20/ S1) and the respective collector.

Adaptation to error signal level

An open collector transistor is used as error terminal, which, in case of error, leads the signal to earth. The signal has to be adapted to the evaluation circuit's voltage level by means of an externally connected pull-up resistor. The maximum load applied to the transistor shall be 30 V / 15 mA.

As for the SKHI 22A / 21A a 10 kΩ pull-up resistor versus V_S (P13) has already been integrated in the driver.

IGBT switching speed adjustment

The IGBT switching speed may be adjusted by the resistors R_{ON} and R_{OFF}. By increasing R_{ON} the turn-on speed will decrease. The reverse peak current of the free-wheeling diode will diminish. SEMIKRON recommends to adjust R_{ON} to a level that will keep the turn-on delay time $t_{d(on)}$ of the IGBT < 1 µs.

By increasing R_{OFF} the turn-off speed of the IGBT will decrease. The inductive peak overvoltage during turn-off will diminish.

The minimum gate resistor value for R_{OFF} and R_{ON} is 3 Ω. Typical values for R_{ON} and R_{OFF} recommended by SEMIKRON are given in fig. 5

SK-IGBT-Modul	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kΩ	R_{VCE} kΩ
SKM 50GB123D	22	22	330	18	0
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0
SKM 400GA123D	6,8	6,8	330	18	0
SKM 75GB173D	15	15	470	36	1
SKM 100GB173D	12	12	470	36	1
SKM 150GB173D	10	10	470	36	1
SKM 200GB173D	8,2	8,2	470	36	1

Fig. 5 Typical values for external components

Interlocking time adjustment

Fig. 3 shows the possible interlocking times between output1 and output2. Interlocking times are adjusted by connecting the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) either to earth/ GND (P7 and P14) according to the required function or by leaving them open.

A typical interlocking time value is 3,25 µs (P9 = GND; P5 and P6 open). For SKHI 22A / 21A the terminals TDT1 (P5) and SELECT (P6) are not existing. The interlocking time has been fixed to 3,25 µs and may only be increased to 4,25 µs by connecting TDT2 (P9) to V_S (P13).

ATTENTION: If the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) are not connected, eventually connected track on PC-board may not be longer than 20 mm in order to avoid interferences.

SEMIKRON recommends to start-up operation using the values recommended by SEMIKRON and to optimize the values gradually according to the IGBT switching behaviour and overvoltage peaks within the specific circuitry.

Driver performance and application limits

The drivers are designed for application with halfbridges and single modules with a maximum gate charge Q_{GE} < 4 µC (see fig. 6).

The charge necessary to switch the IGBT is mainly depending on the IGBT's chip size, the DC-link voltage and the gate voltage.

This correlation is also shown in the corresponding module datasheet curves.

It should, however, be considered that the SKHI 22B is turned on at + 15 V and turned off at - 7 V. Therefore, the gate voltage will change by 22 V during every switching procedure.

Unfortunately, most datasheets do not indicate negative gate voltages. In order to determine the required charge, the upper leg of the charge curve may be prolonged to + 22 V for determination of approximate charge per switch.

The medium output current of the driver is determined by the switching frequency and the gate charge. For the SKHI 22B the maximum medium output current is $Iout_{AVmax}$ < ± 40 mA.

The maximum switching frequency f_{MAX} may be calculated with the following formula, the maximum value however being 50 kHz due to switching reasons:

$$f_{MAX}(kHz) = \frac{4 \cdot 10^4}{Q_{GE}(nC)}$$

Fig. 6 shows the maximum rating for the output charge per pulse for different gate resistors.

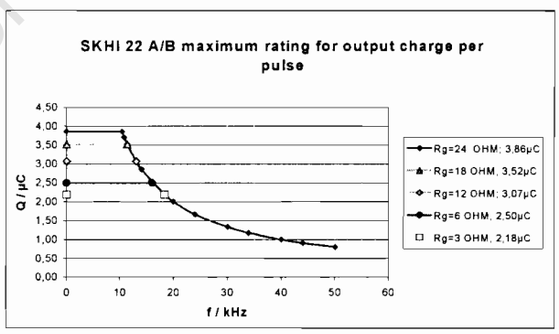


Fig. 6 Maximum rating for output charge per pulse

Further application notes

The CMOS-inputs of the hybrid driver are extremely sensitive to over-voltage. Voltages higher than V_S + 0,3 V or below – 0,3 V may destroy these inputs. Therefore, control signal over-voltages exceeding the above values have to be avoided.

Please provide for static discharge protection during handling. As long as the hybrid driver is not completely

assembled, the input terminals have to be short-circuited. Persons working with CMOS-devices have to wear a grounded bracelet. Any synthetic floor coverings must not be statically chargeable. Even during transportation the input terminals have to be short-circuited using, for example, conductive rubber. Worktables have to be grounded. The same safety requirements apply to MOSFET- and IGBT-modules!

The connecting leads between hybrid driver and the power module should be as short as possible, the driver leads should be twisted.

Any parasitic inductances within the DC-link have to be minimized. Over-voltages may be absorbed by C- or RCD-snubbers between the main terminals for PLUS and MINUS of the power module.

When first operating a newly developed circuit, SEMIKRON recommends to apply low collector voltage and load current in the beginning and to increase these values gradually, observing the turn-off behaviour of the free-wheeling diode and the turn-off voltage spikes generated accross the IGBT. An oscillographic control will be necessary. In addition to that the case temperature of the module has to be monitored. When the circuit works correctly under rated operation conditions, short-circuit testing may be done, starting again with low collector voltage.

It is important to feed any errors back to the control circuit and to switch off the device immediately in such events. Repeated turn-on of the IGBT into a short circuit with a high frequency may destroy the device.

Mechanical fixing on PCB:

In applications with mechanical vibrations (vehicles)[2] do not use a ty-rap for fixing the driver, but - after soldering and testing - apply special glue. Recommended types: CIBA GEIGY XP 5090 + 5091; PACTAN 5011; WACKER A33 (ivory) or N199 (transparent), applied around the case edge (forms a concave mould). The housing may not be pressed on the PCB; do not twist the PCB with the driver soldered on, otherwise the internal ceramics may crack. The driver is not suitable for big PCBs.

SEMIKRON offers a printed circuit board (PCB) type SKPC2006 compatible for mounting a SKHI 21A or SKHI 22A. This PCB contains the necessary tracks to connect the external capacitors C_{CE} and resistors R_{CE}, R_{on}, R_{off} (see fig. 1).

The PCB may directly be plugged to SEMITRANS 3-IGBT modules and be fixed to the heatsink by 3 thread bolts.

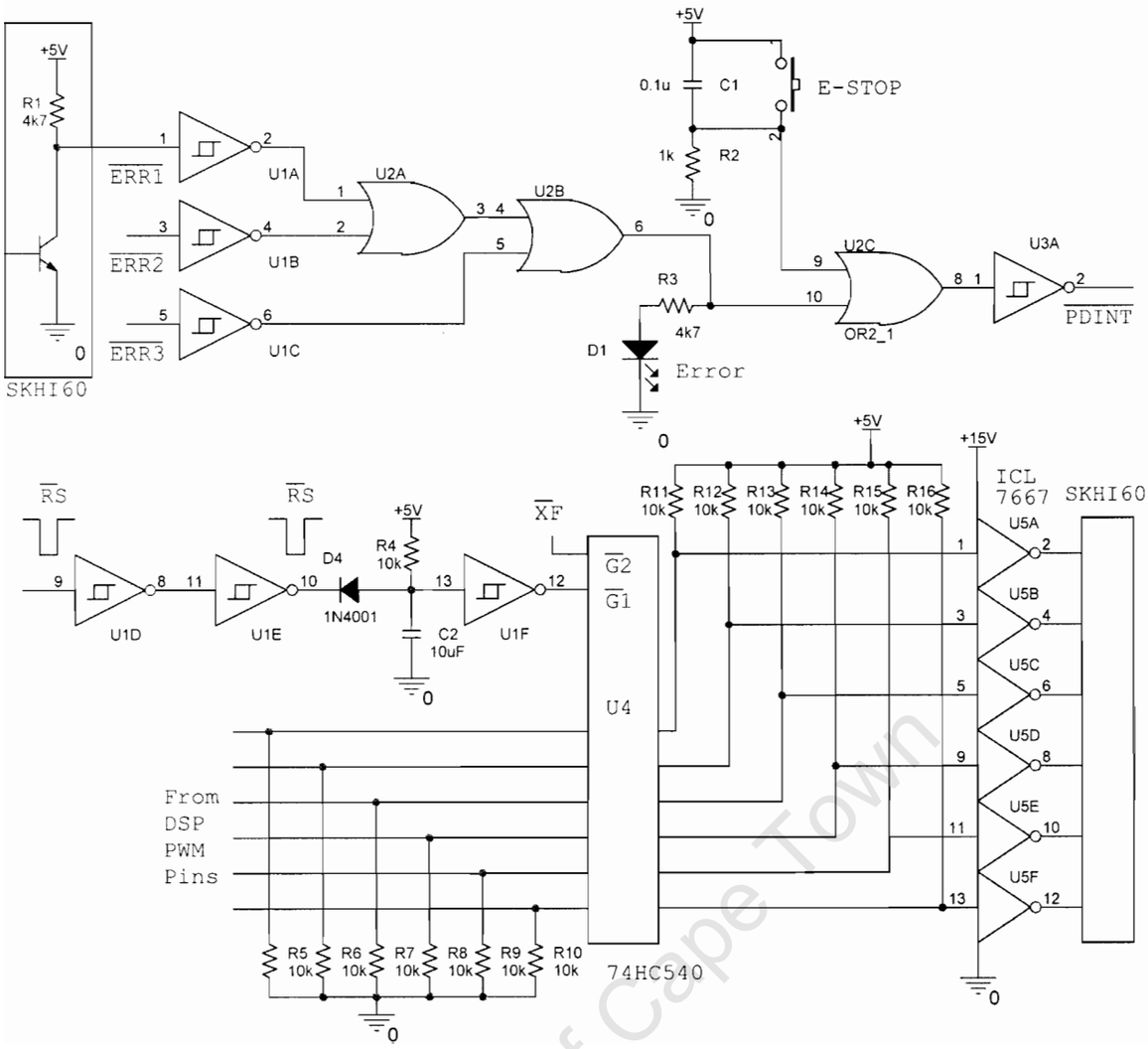
Dimensions: L x W x H = 96 x 67 x 1,5 mm.

For further details please contact SEMIKRON.

2. tested acceleration (x; y; z-axis):10-100 Hz: 1,5 g; shock: 5 g (TÜV according to LES-DB-BN 411002)

APPENDIX D :

LEVEL SHIFTER CIRCUIT



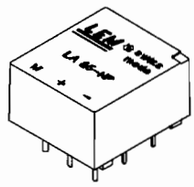
APPENDIX E :

LEM MODULES

Current Transducer LA 25-NP/SP25

I_{PN} = 5-6-8-12-25 A

For the electronic measurement of currents : DC, AC, pulsed, mixed, with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		25		At
I_P	Primary current, measuring range		0 .. ± 36		At
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 15 V	@ ± 25 At_{max}	150	325	Ω
		@ ± 36 At_{max}	150	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		1-2-3-4-5 : 1000		
V_C	Supply voltage (± 5 %)		± 15		V
I_C	Current consumption		10 + I_S		mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn		2.5 (4 kV DC/5 mn)		kV
V_b	R.m.s. rated voltage [1],	safe separation	600		V
		basic isolation	1700		V

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN} , T_A = 25°C		± 0.6		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current [2] @ I_P = 0, T_A = 25°C		± 0.05	± 0.15	mA
I_{OM}	Residual current [3] @ I_P = 0, after an overload of 3 x I_{PN}		± 0.05	± 0.15	mA
I_{OT}	Thermal drift of I_O	- 40°C .. + 85°C	± 0.25	± 0.70	mA
t_r	Response time [4] @ 90 % of I_{PN}		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
f	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature		- 40 .. + 85	°C
T_S	Ambient storage temperature		- 50 .. + 100	°C
R_P	Primary coil resistance (per turn) @ T_A = 25°C		< 1.25	mΩ
R_S	Secondary coil resistance @ T_A = 85°C		115	Ω
R_{IS}	Isolation resistance @ 500 V, T_A = 25°C		> 1500	MΩ
m	Mass		22	g
	Standards [5]		EN 50155	

Notes : [1] Pollution class 2
[2] Measurement carried out after 15 mn functionning
[3] The result of the coercive field of the magnetic circuit
[4] With a di/dt of 100 A/µs
[5] A list of corresponding tests is available

Features

- Closed loop (compensated) multi-range current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Special features

- V_d = 2.5 kV (4 kV DC/5 mn)
- T_A = - 40°C .. + 85°C.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

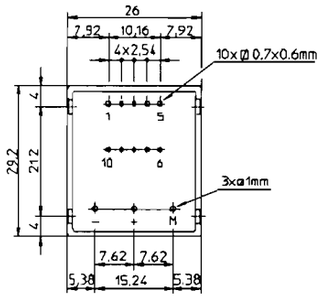
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

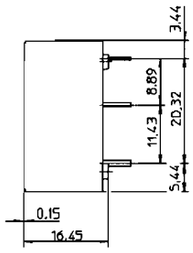
000425/4

Dimensions LA 25-NP/SP25 (in mm. 1 mm = 0.0394 inch)

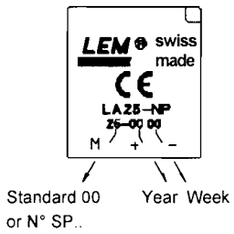
Bottom view

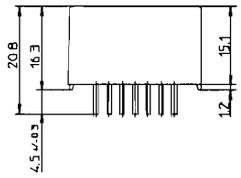


Right view



Top view



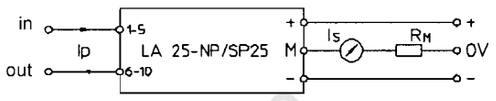


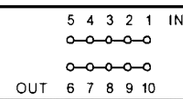
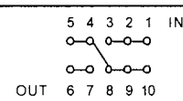
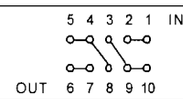
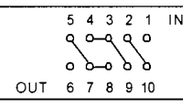
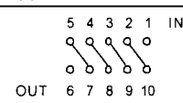
Back view

Secondary terminals

Terminal + : supply voltage +15 V
Terminal M : measure
Terminal - : supply voltage - 15 V

Connection



Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended connections
1	25	36	25	1 / 1000	0.3	0.023	
2	12	18	24	2 / 1000	1.1	0.09	
3	8	12	24	3 / 1000	2.5	0.21	
4	6	9	24	4 / 1000	4.4	0.37	
5	5	7	25	5 / 1000	6.3	0.58	

Mechanical characteristics

General tolerance	± 0.2 mm
Fastening & connection of primary	10 pins 0.7 x 0.6 mm
Fastening & connection of secondary	3 pins ⌀ 1 mm
Recommended PCB hole	1.2 mm

Remark

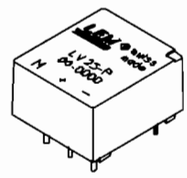
- I_S is positive when I_P flows from terminals 1, 2, 3, 4, 5 to terminals 10, 9, 8, 7, 6.

Voltage Transducer LV 25-P

I_{PN} = 10 mA

V_{PN} = 10 .. 500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		10		mA
I_P	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA_{max}	30	190	Ω
		@ ± 14 mA_{max}	30	100	Ω
	with ± 15 V	@ ± 10 mA_{max}	100	350	Ω
		@ ± 14 mA_{max}	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@±15 V) + I_S		mA
V_d	R.m.s. voltage for AC isolation test[1], 50 Hz, 1 mn		2.5		kV

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time[2] @ 90 % of V_{PN}		40		µs

General data

T_A	Ambient operating temperature	0 .. + 70		°C
T_S	Ambient storage temperature	- 25 .. + 85		°C
R_P	Primary coil resistance @ T_A = 70°C	250		Ω
R_S	Secondary coil resistance @ T_A = 70°C	110		Ω
m	Mass	22		g
	Standards	EN 50178 (97.10.01)		

Notes : [1] Between primary and secondary

[2] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit).

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

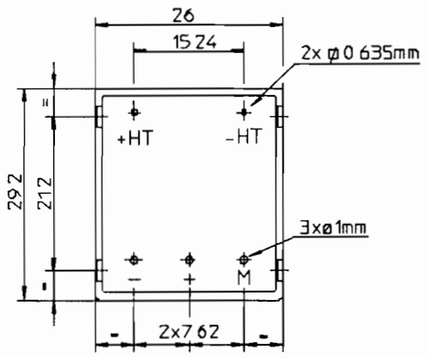
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

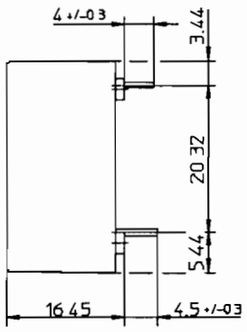
981009/14

Dimensions LV 25-P (in mm. 1 mm = 0.0394 inch)

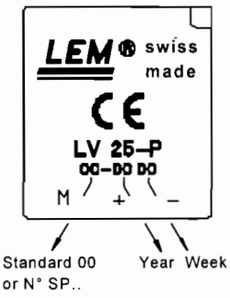
Bottom view

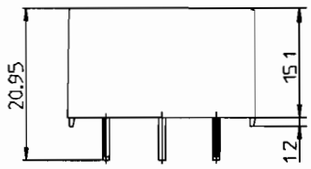


Right view



Top view



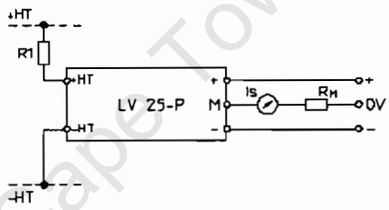


Back view

Secondary terminals

Terminal + : supply voltage + 12 .. 15 V
Terminal M : measure
Terminal - : supply voltage - 12 .. 15 V

Connection



Mechanical characteristics

General tolerance	± 0.2 mm
Fastening & connection of primary	2 pins 0.635 x 0.635 mm
Fastening & connection of secondary	3 pins ø 1 mm
Recommended PCB hole	1.2 mm

Remarks

- I_S is positive when V_P is applied on terminal +HT.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Instructions for use of the voltage transducer model LV 25-P

Primary resistor R_1 : the transducer's optimum accuracy is obtained at the nominal primary current. As far as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

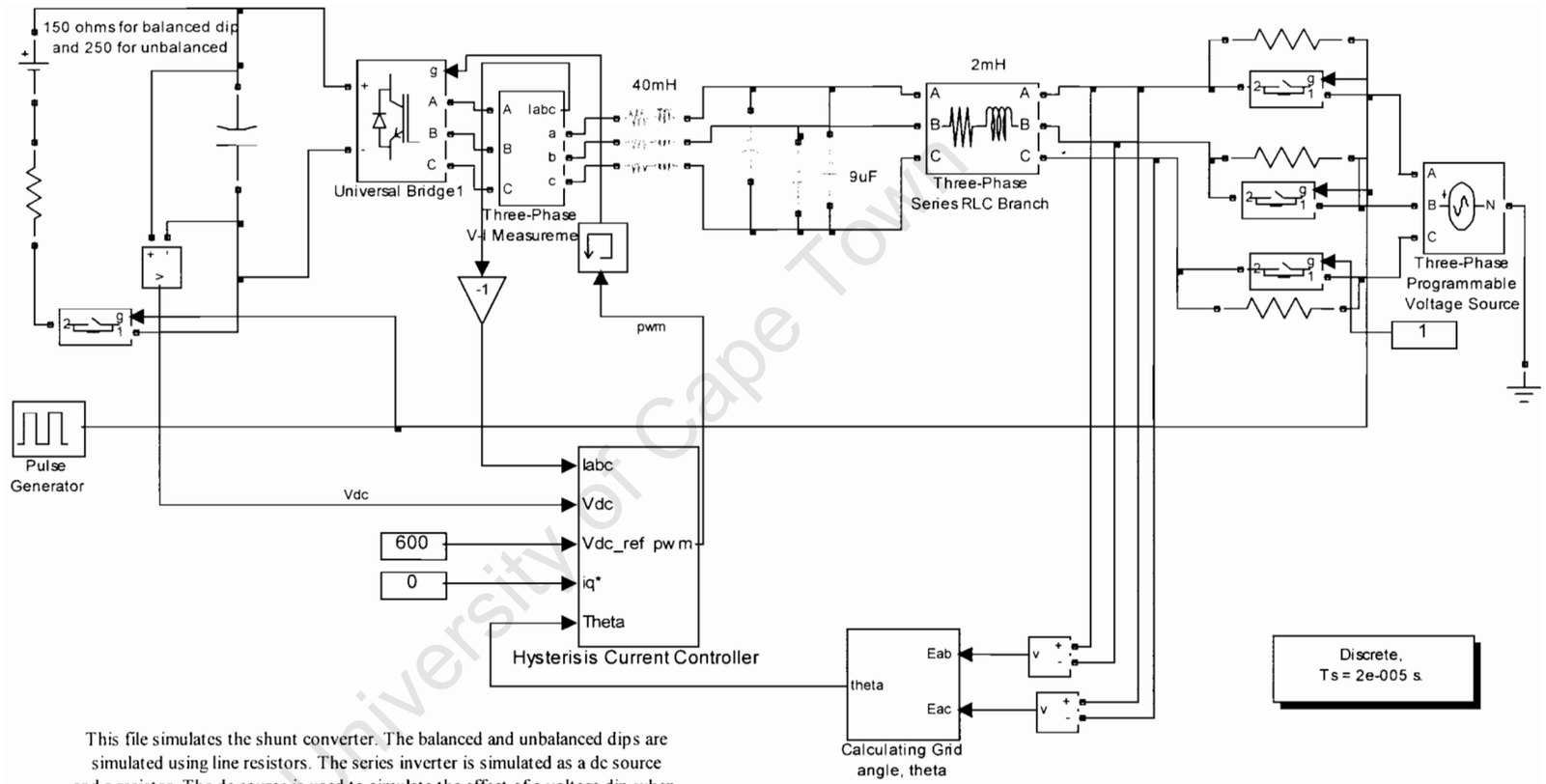
Example: Voltage to be measured V_{PN} = 250 V

a) R_1 = 25 kΩ / 2.5 W, I_P = 10 mA Accuracy = ± 0.8 % of V_{PN} (@ T_A = +25°C)
b) R_1 = 50 kΩ / 1.25 W, I_P = 5 mA Accuracy = ± 1.6 % of V_{PN} (@ T_A = +25°C)

Operating range (recommended) : taking into account the resistance of the primary windings (which must remain low compared to R_1 in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

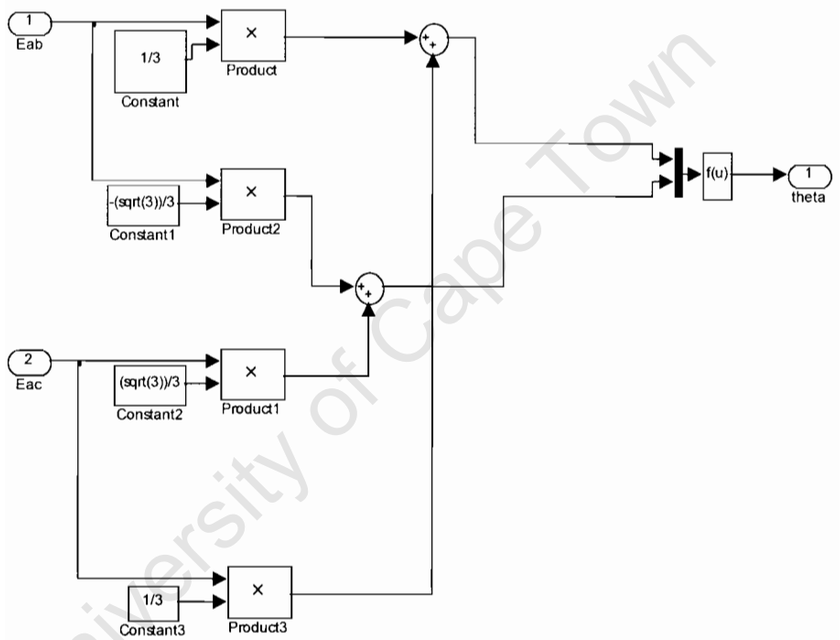
APPENDIX F :

MATLAB SIMULINK MODELS

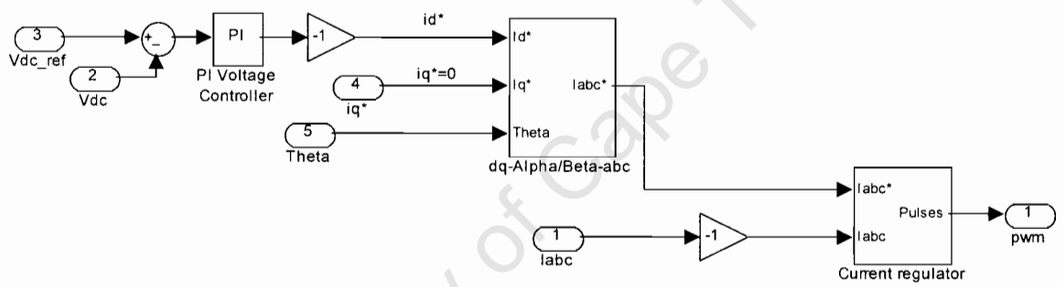


This file simulates the shunt converter. The balanced and unbalanced dips are simulated using line resistors. The series inverter is simulated as a dc source and a resistor. The dc source is used to simulate the effect of a voltage dip when power flows from the series inverter to the shunt converter. The resistor represent the power absorb by the series inverter when a dip occurs. The pulse generator is used to switch on/off line resistors as well as the dc source + resistor.

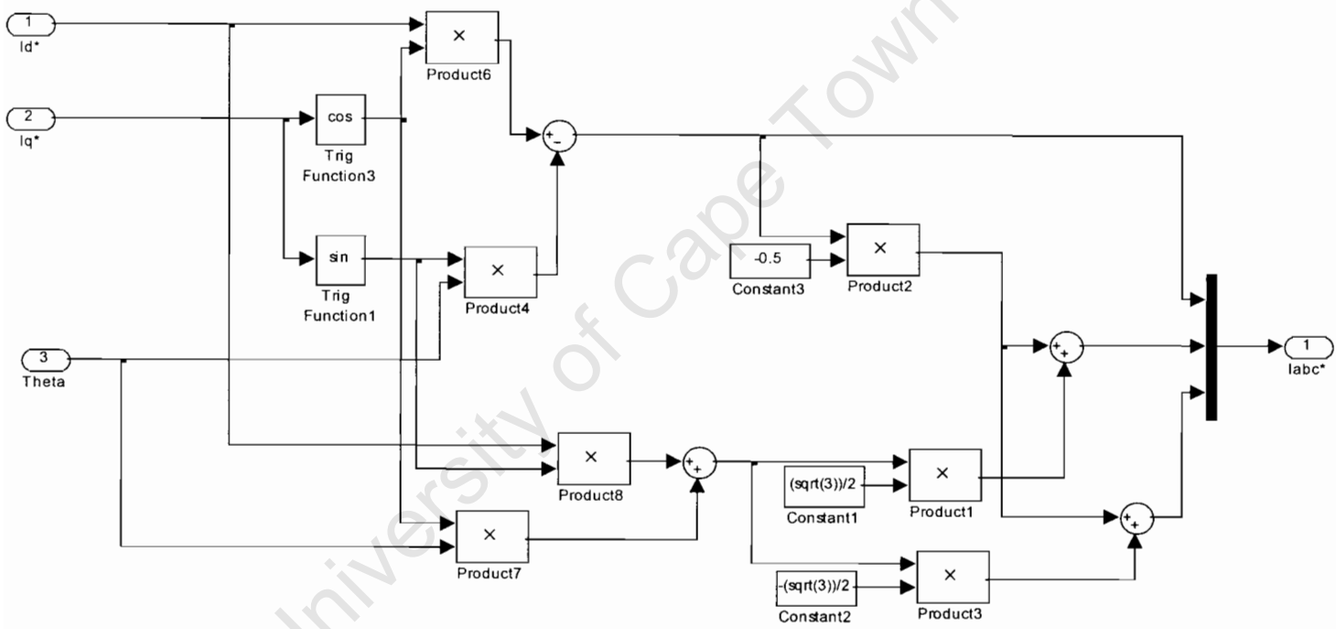
This is the "Calculating Grid angle, theta" block. The alpha and beta components of the supply voltage is obtained form the modified clarke transform and theta calculated as arctan of Ubeta/Ualpha



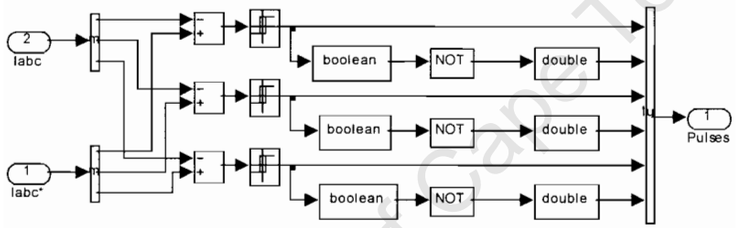
This is the "Hysteresis Current Controller" block. It consist of a PI controller and a current regulator. The output of the PI is the reference d-component of the current while the q-component is set to zero for unity power factor. These two components are then transformed to the abc reference currents which are compared tot he actual currents to obtain the swithcing signals for the shunt converter

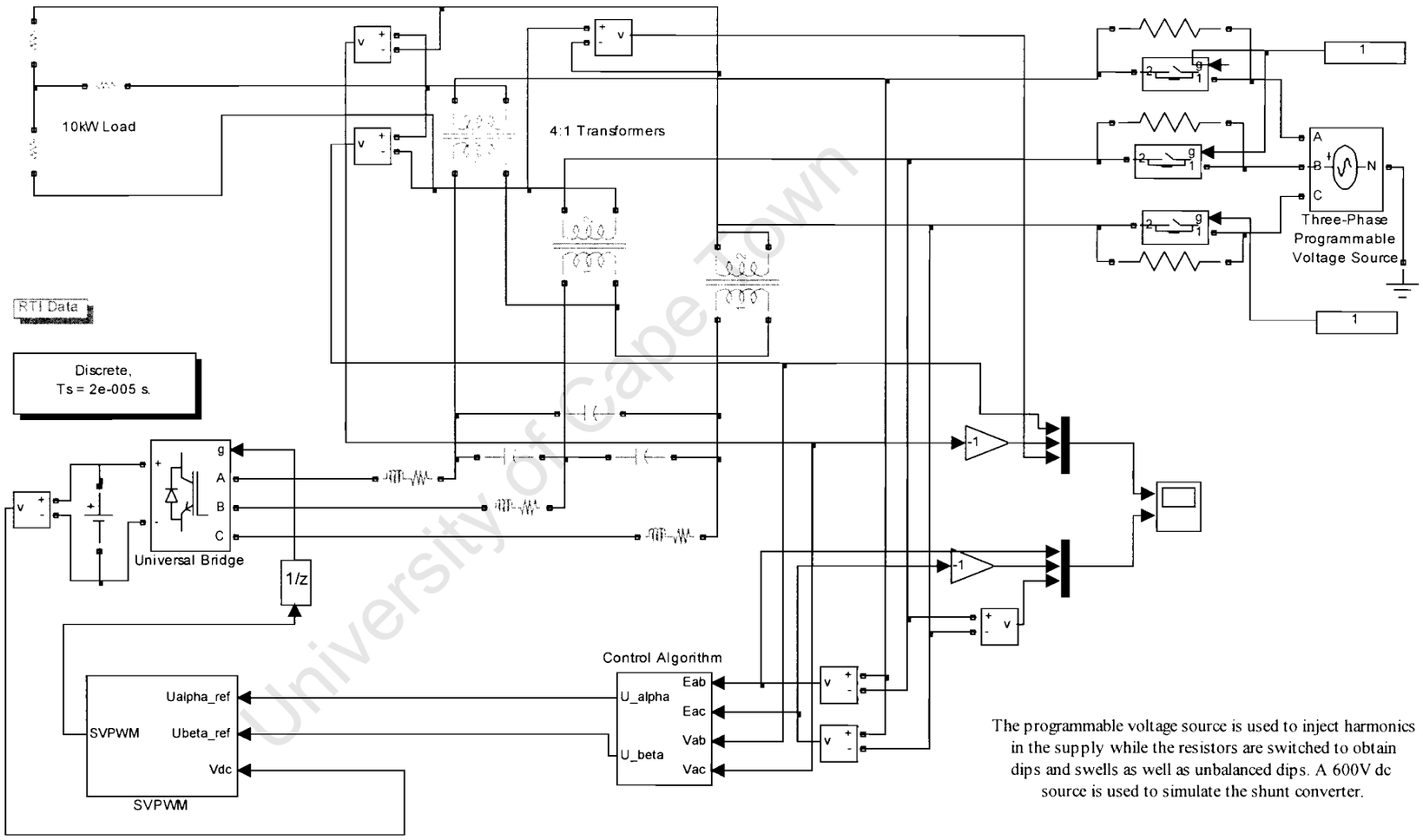


This is the "dq-Alpha/Beta-abc" block. This is where the reference 3 phase currents are obtained form the d-q reference currents.

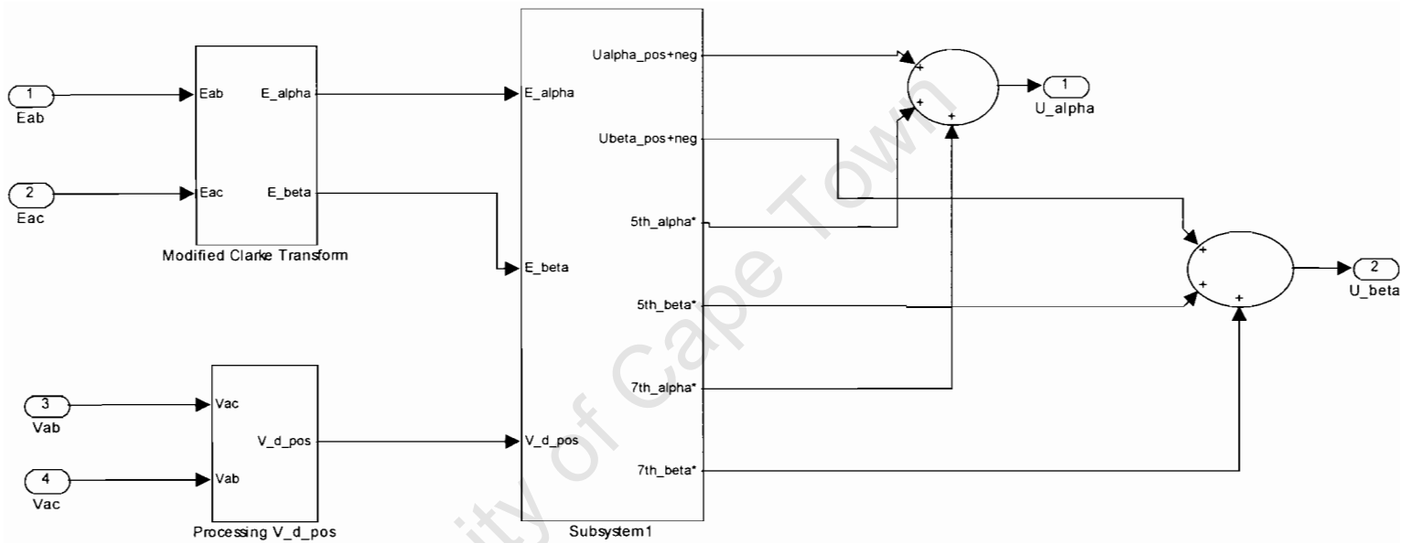


This is the "Hysteresis Current controller" block. This is where the actual currents are compared to the reference currents to obtain the switching signals for the shunt converter.



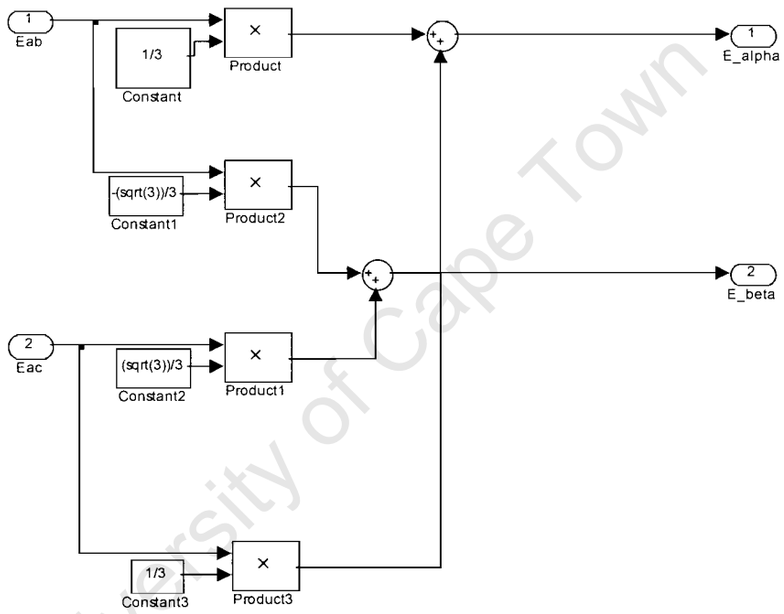


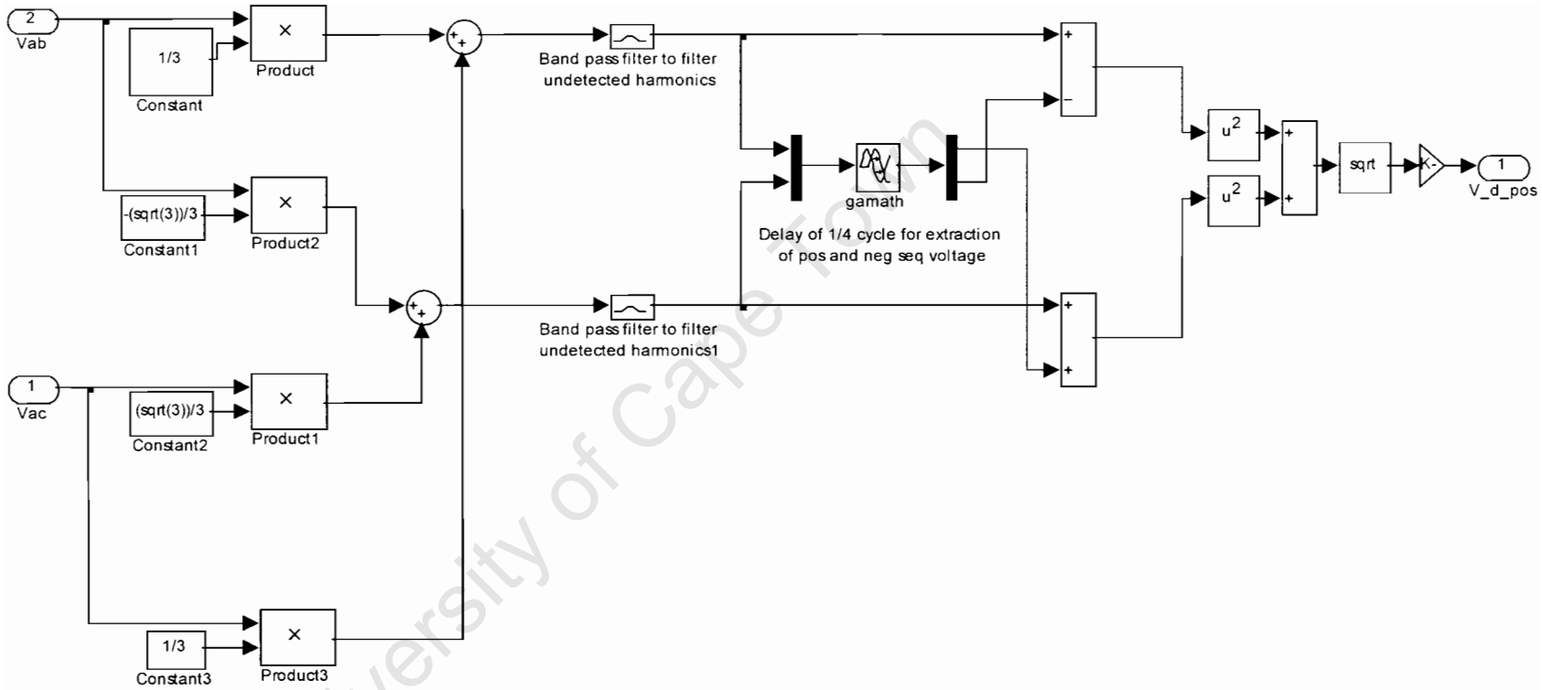
The programmable voltage source is used to inject harmonics in the supply while the resistors are switched to obtain dips and swells as well as unbalanced dips. A 600V dc source is used to simulate the shunt converter.



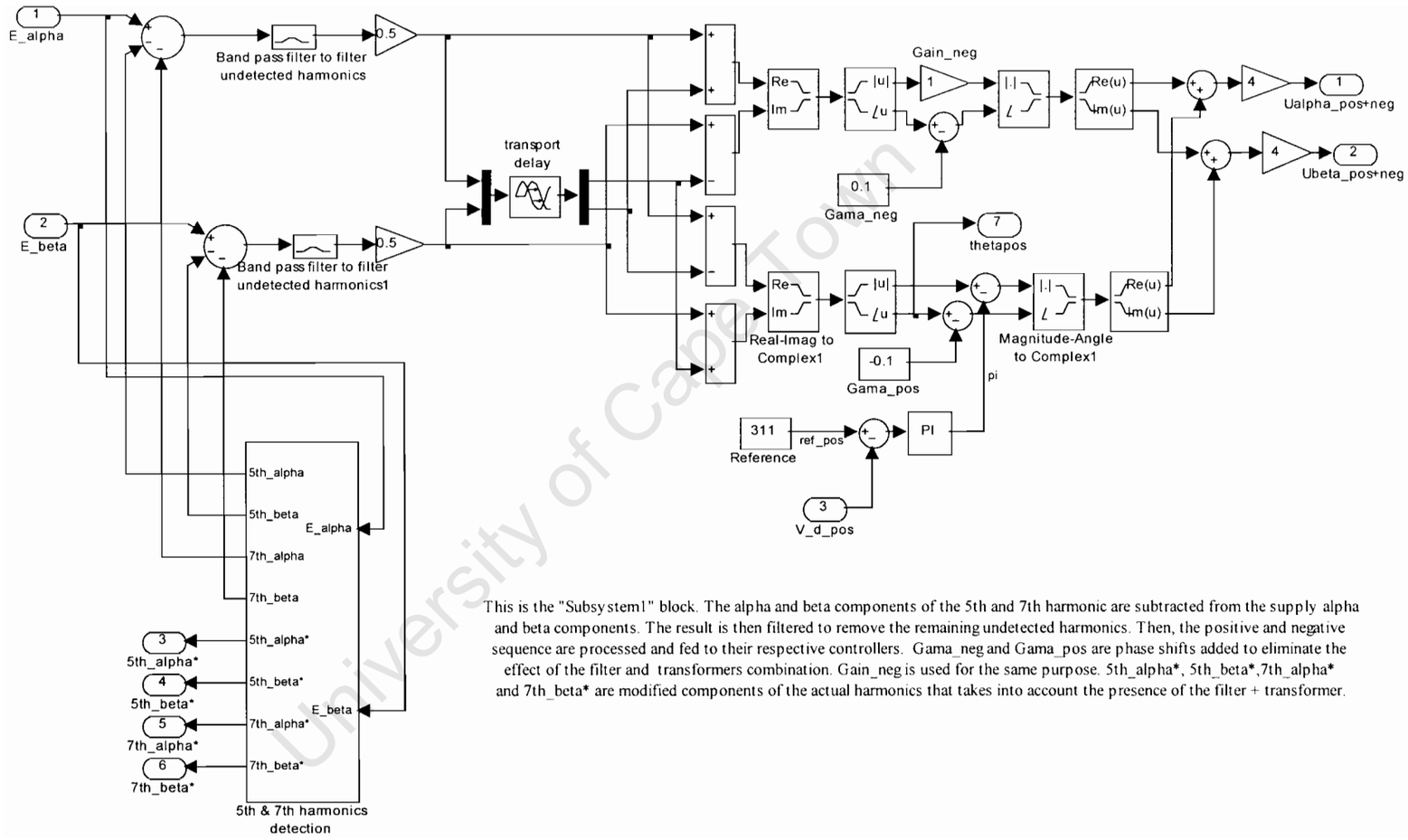
This is the "Control Algorithm" block. Two line-to-line voltages from the supply and load are used to obtain the alpha and beta components of supply voltgae as well as V_d_pos of the load voltage.the suThe 5th and 7th harmonics as well as the positive and negative sequence components that need to be injected into the system are added to obtain U_alpha and U_beta which are the inputs to the Space Vector pwm algorithm

This is the "Modified Clarke Transform" block

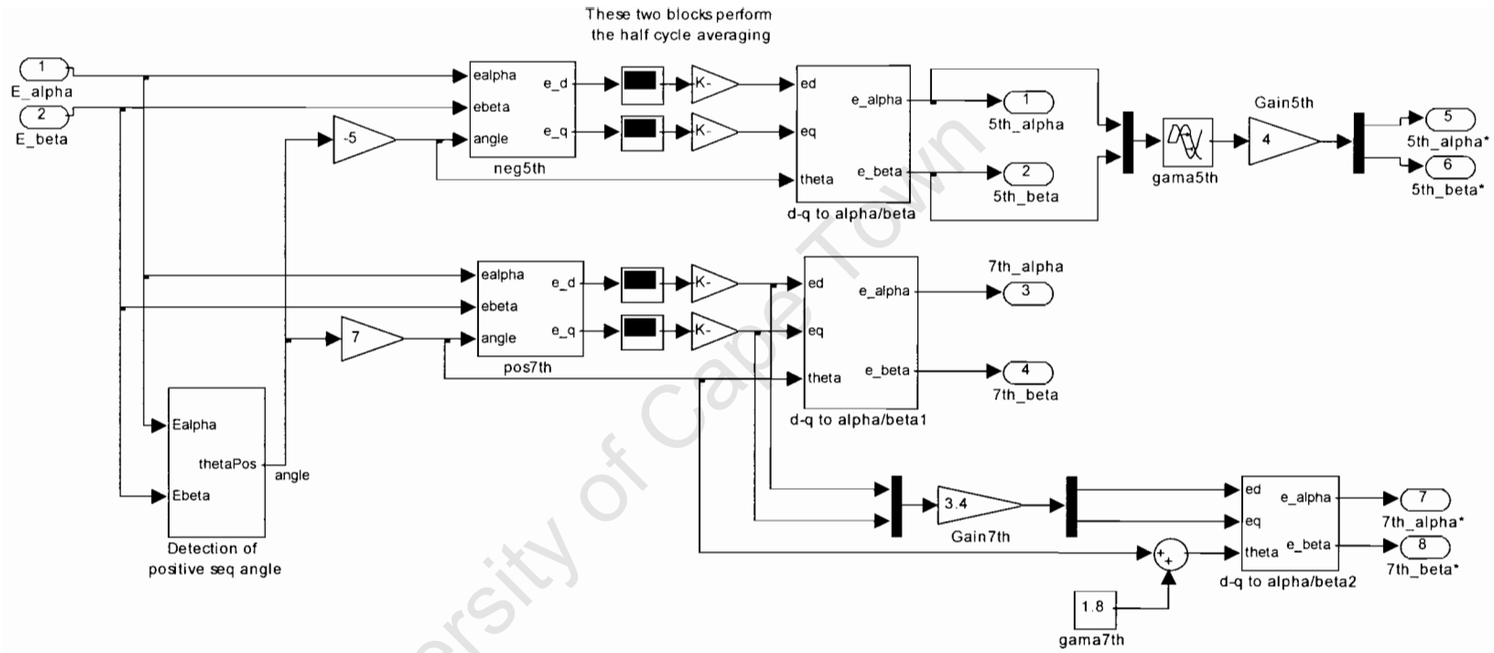




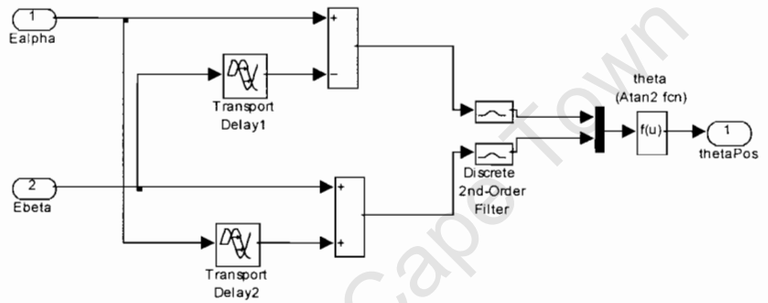
This is the "Processing V_d_pos " block. The alpha and beta components of the load voltage are calculated form two line-to-line voltage using the modified clarke transform. These components are filtered to remove the undetected harmonics and then the positive sequence voltage components are extracted. Finally, V_d_pos is calculated.



This is the "Subsystem1" block. The alpha and beta components of the 5th and 7th harmonic are subtracted from the supply alpha and beta components. The result is then filtered to remove the remaining undetected harmonics. Then, the positive and negative sequence are processed and fed to their respective controllers. Gama_neg and Gama_pos are phase shifts added to eliminate the effect of the filter and transformers combination. Gain_neg is used for the same purpose. 5th_alpha*, 5th_beta*,7th_alpha* and 7th_beta* are modified components of the actual harmonics that takes into account the presence of the filter + transformer.

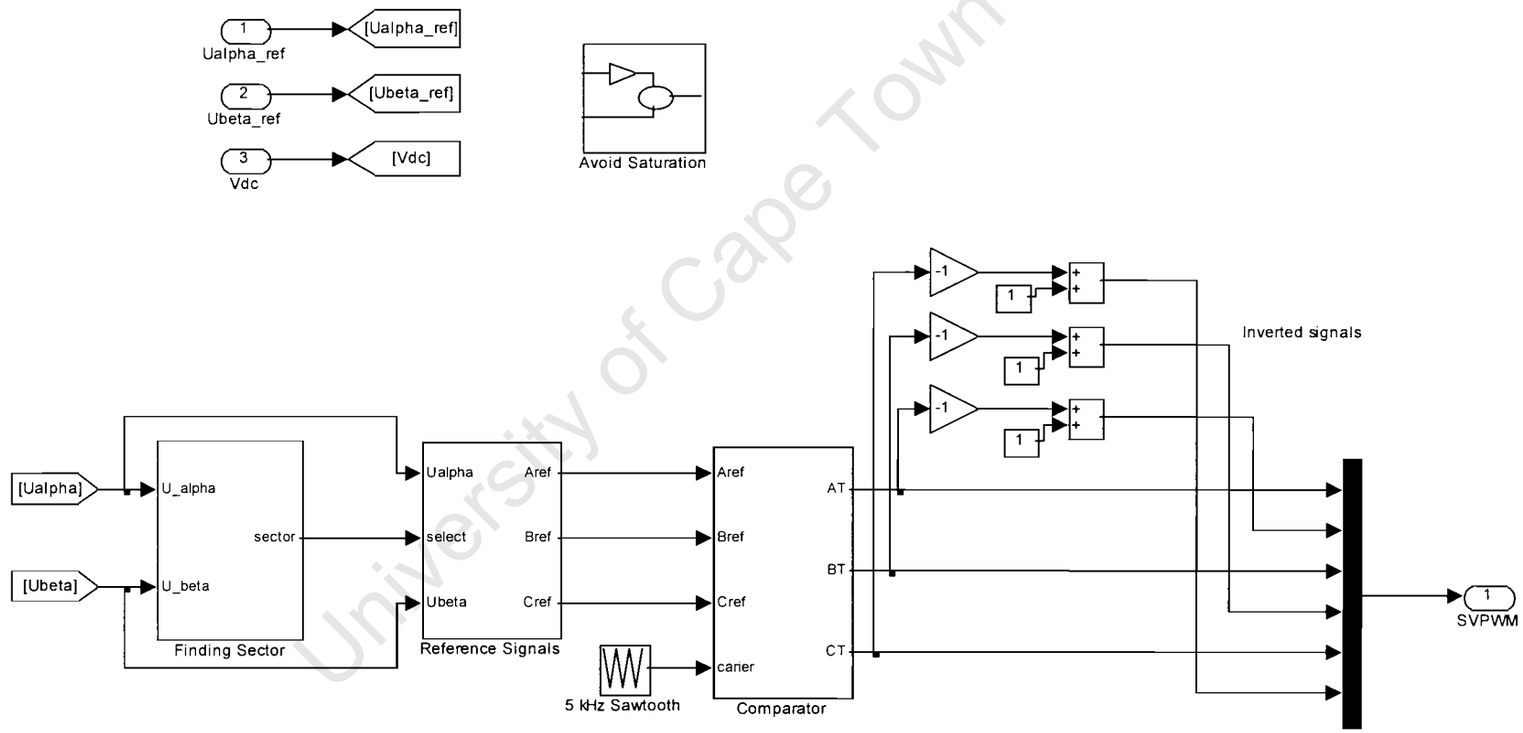


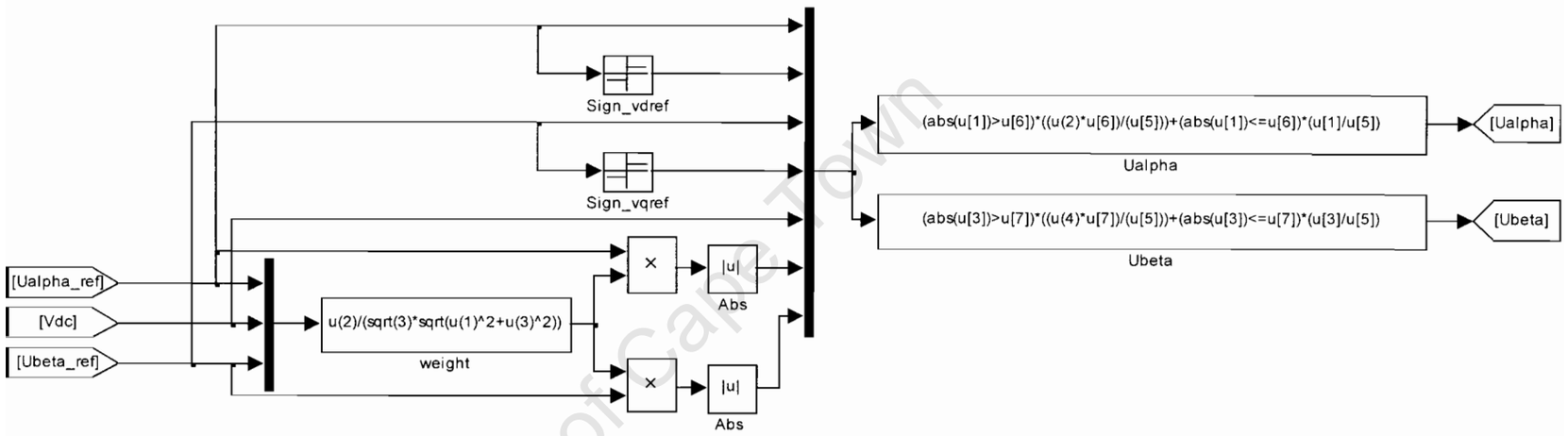
This is the "5th & 7th harmonics detection" block. Only the negative sequence 5th harmonic and positive sequence 7th harmonic are detected to reduce the amount of compututation in order to achieve a resonable large sampling frequency. The supply alpha and beta components are transformed to different synchronous frames where the 5th and 7th harmonics are isolated. Then, using the half cycle averaging technique, they are measured. Thereafter, they are transformed back to the stationary frame. Gain7th, Gain5th, gama7th and gama5th are introduced to eliminate the effects of the combination of the low pass filter and of the transformers on the injected harmonics. The modified harmonic components are injected by the series inverter while the true components of these harmonics are used to obtain the fundamental components of the supply voltage.



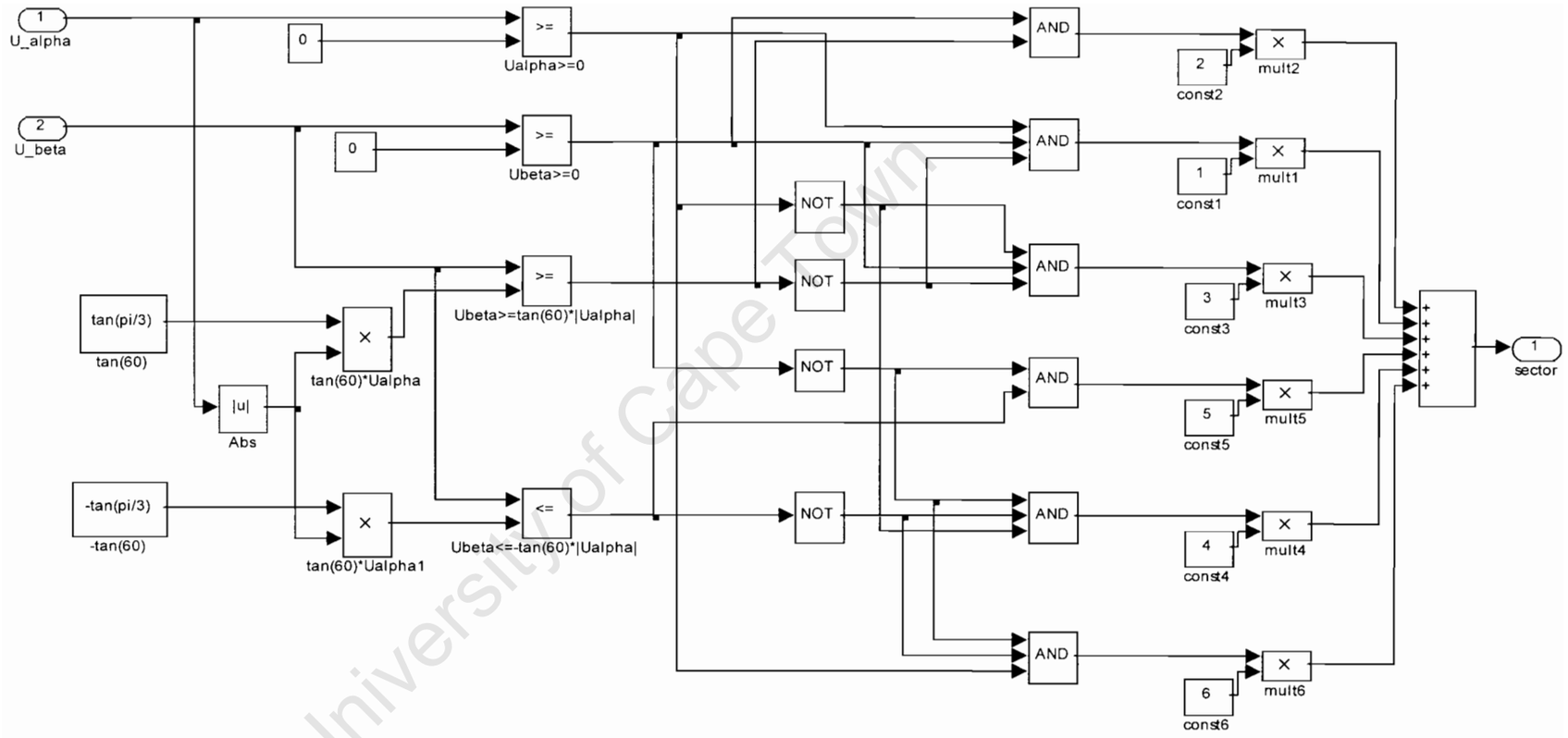
This is the "Detection of positive seq angle" block. The positive sequence voltage of the supply is first extrated. Bandpass filters are then used for filtering all the harmonics present before the the supply positive sequence angle is computed

This is the "SVPWM" block. The SVPWM algorithm is processed here. First, the alpha and beta components are scaled down by the "Avoid Saturation" block if they exceed the maximum limit.The sectors in which the vector lies are computed and three reference signals Aref, Bref and Cref are computed. These signals are then compared to a high frequency carrier to obtain the switching signals. These signals are then inverted for the other IGBTs.



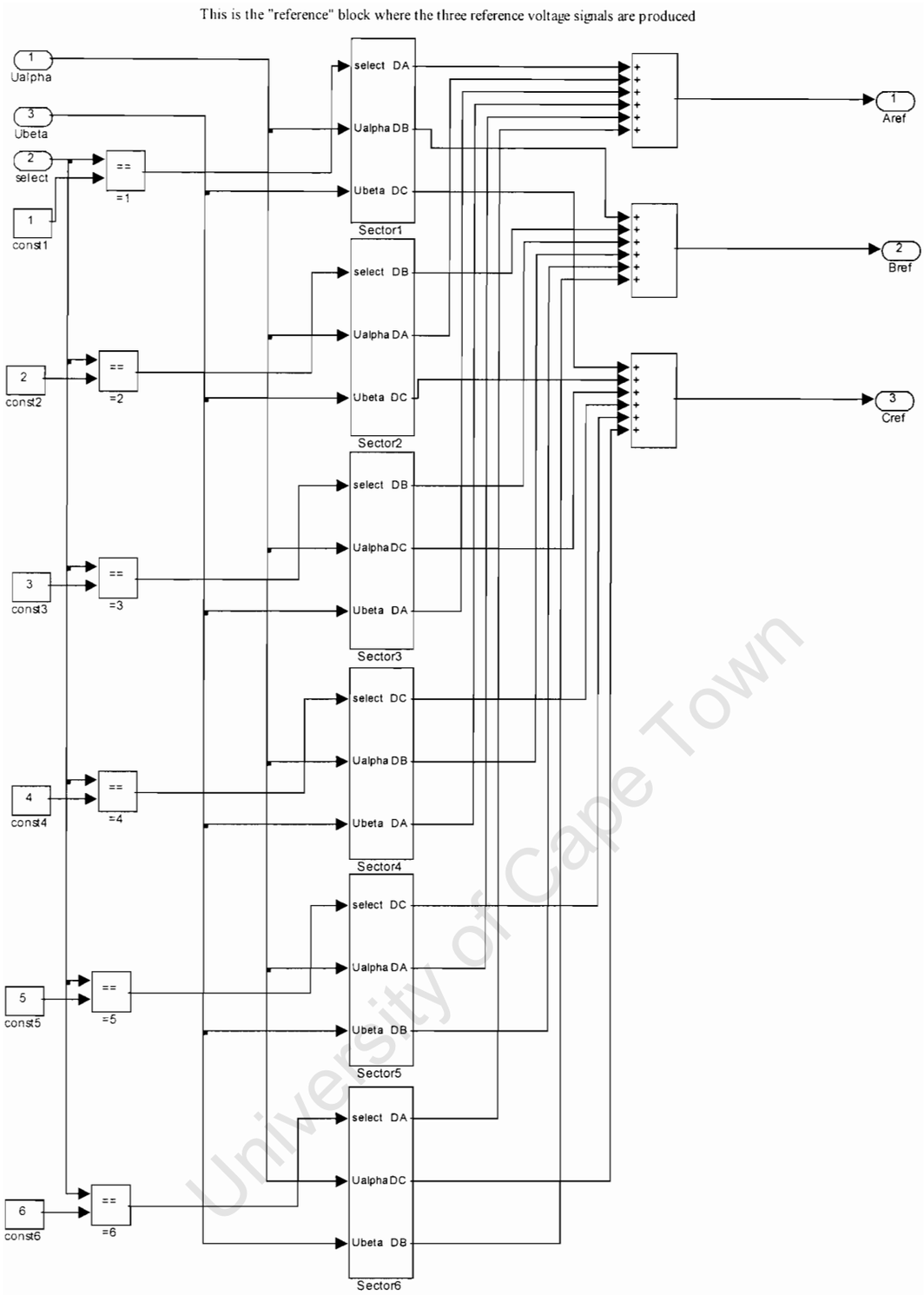


This is the "Avoid Saturation" block. The alpha and beta components from the control algorithm are limited to a maximum value so that the vector Uout does not exceed Vdc/sqrt(3). First, the maximum allowable value of Ualpha and Ubeta is processed. Then, the actual values of Ualpha and Ubeta are compared to that maximum. If they are smaller, they are unchanged. However, if they exceed that maximum value, they are shrunk to the maximum value allowable.

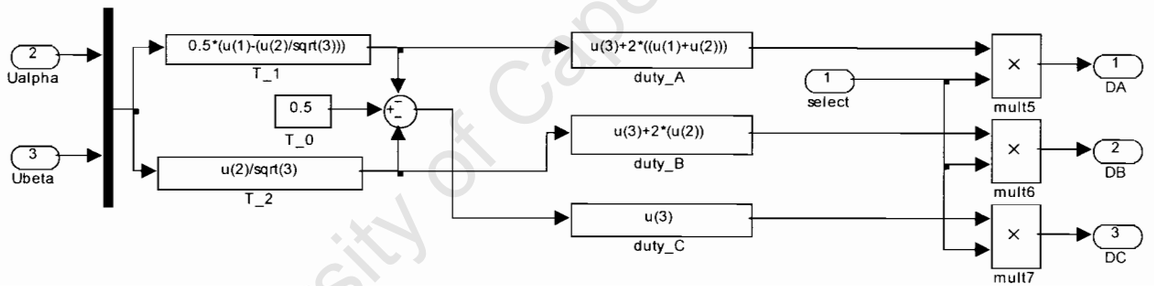


This is the "Finding Sector" block. The sector in which Uout lies is determined according to the flow chart given in chapter two of the thesis.

This is the "reference" block where the three reference voltage signals are produced

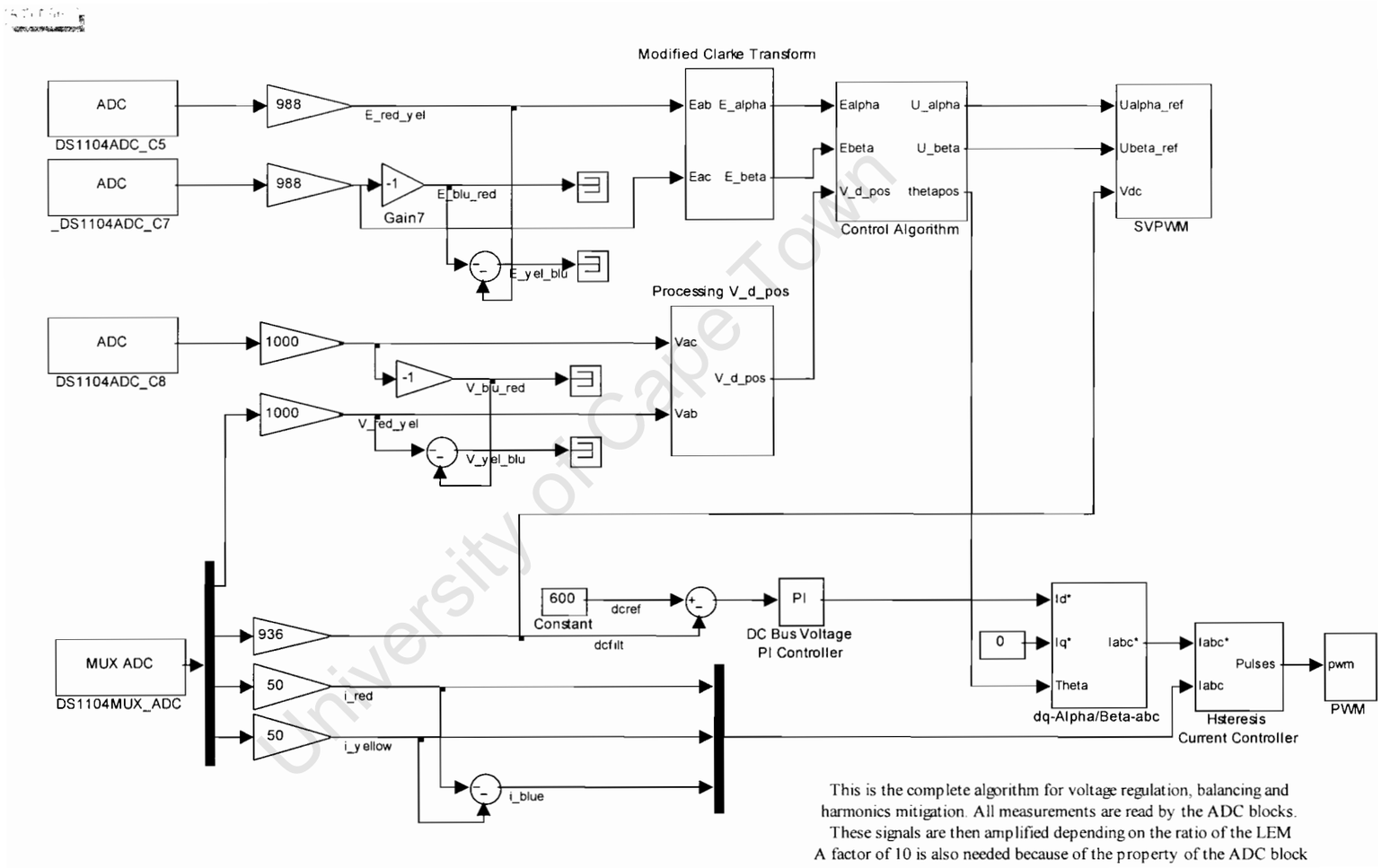


This is the "Sector 1" block. Knowing the sector number, the reference signals can be calculated as described in chapter 2 of the thesis. Only the code for sector 1 is shown in this appendix. The code is very similar for other sectors. The only diference is in the maths function used to calculate the reference signals which is sector dependent as described in the thesis



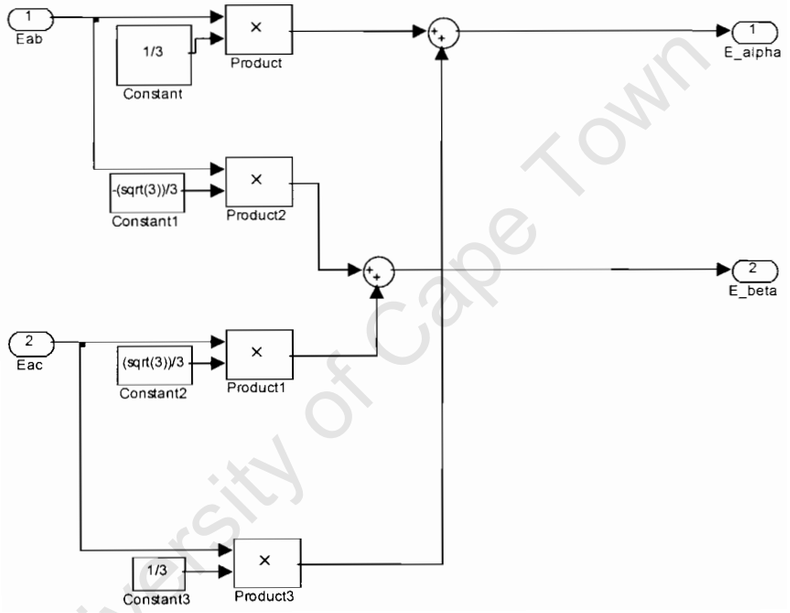
APPENDIX G:

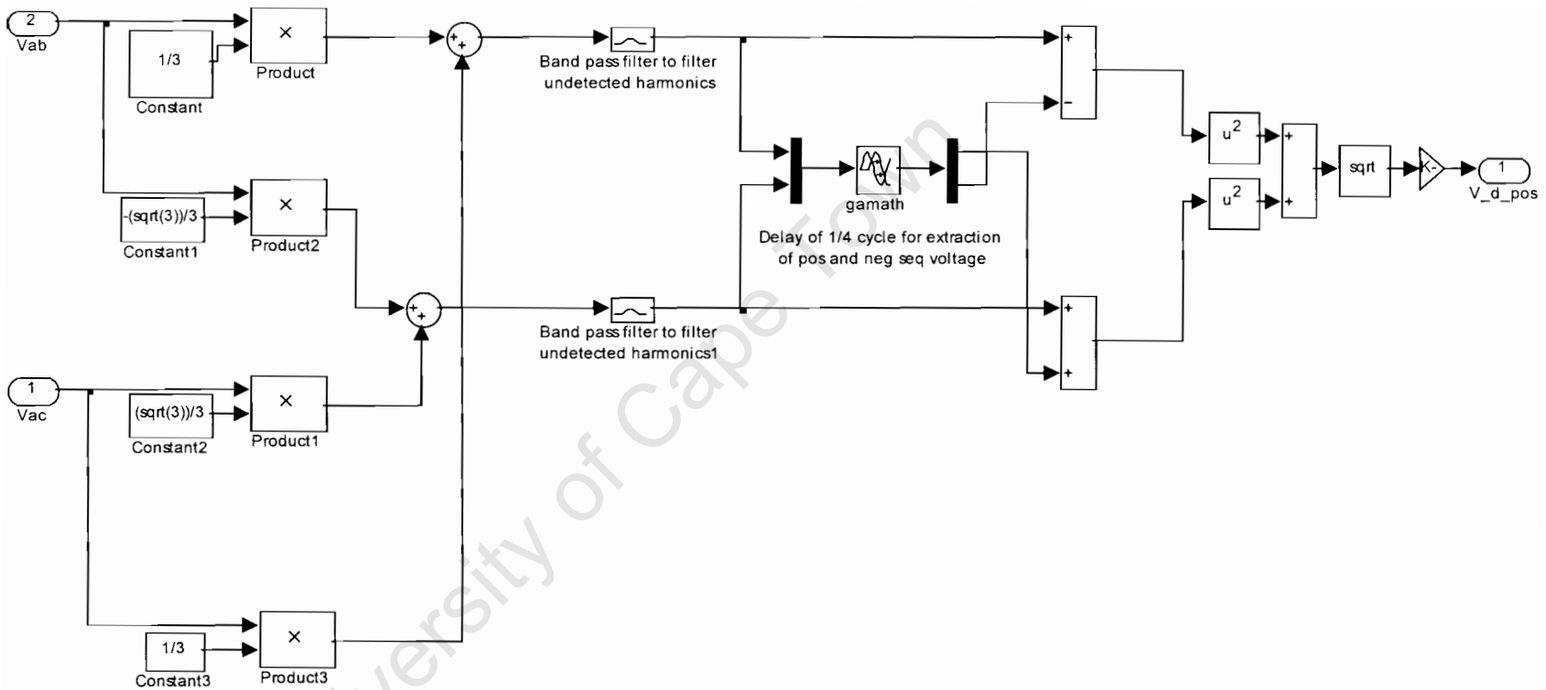
MATLAB SIMULINK MODELS WITH REAL TIME INTERFACE



This is the complete algorithm for voltage regulation, balancing and harmonics mitigation. All measurements are read by the ADC blocks. These signals are then amplified depending on the ratio of the LEM A factor of 10 is also needed because of the property of the ADC block

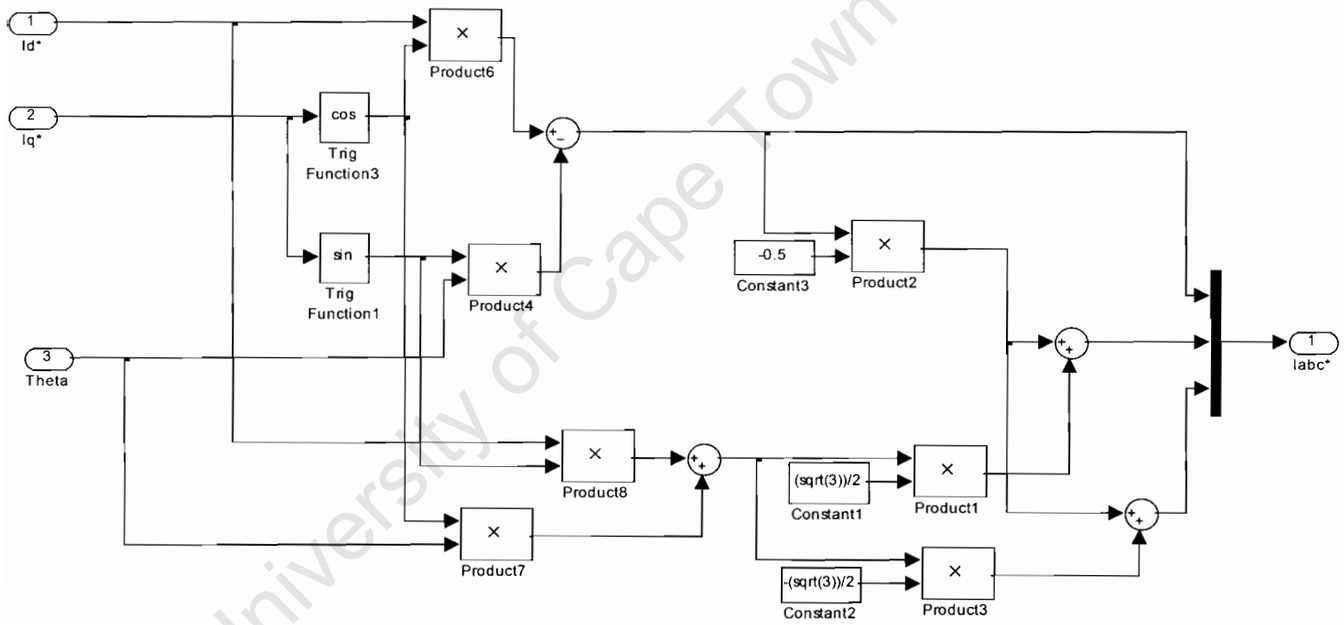
This is the "Modified Clarke Transform" block



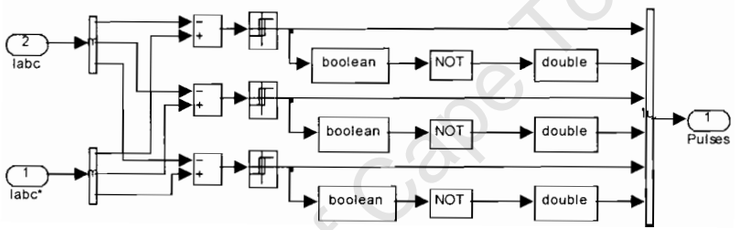


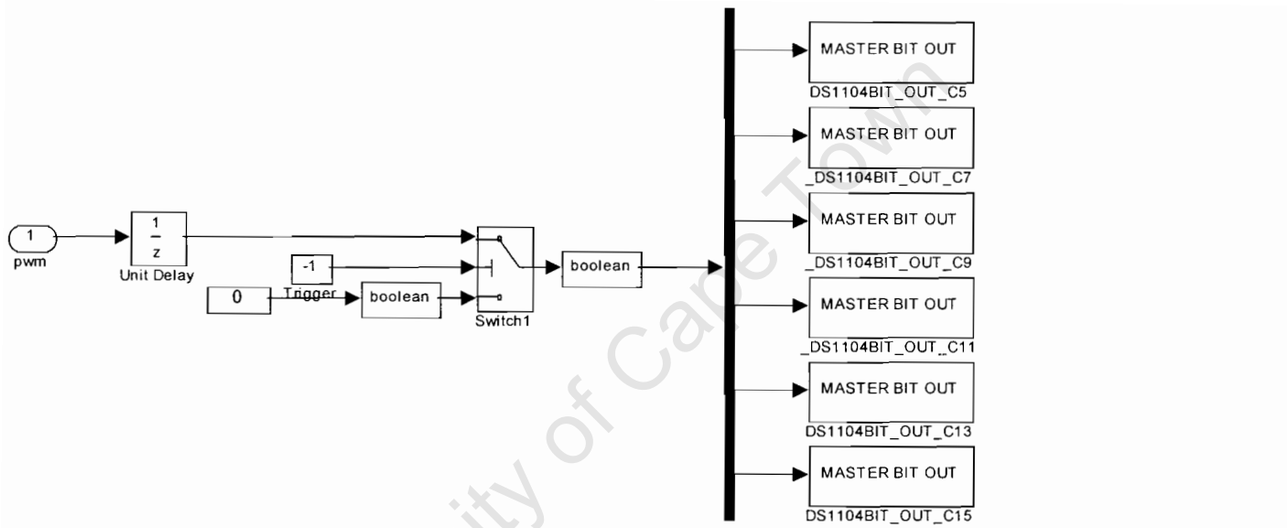
This is the "Processing V_d_pos " block. The alpha and beta components of the load voltage are calculated form two line-to-line voltage using the modified clarke transform. These components are filtered to remove the undetected harmonics and then the positive sequence voltage components are extracted. Finally, V_d_pos is calculated.

This is the "dq-Alpha/Beta-abc" block. This is where the reference 3 phase currents are obtained form the d-q reference currents.

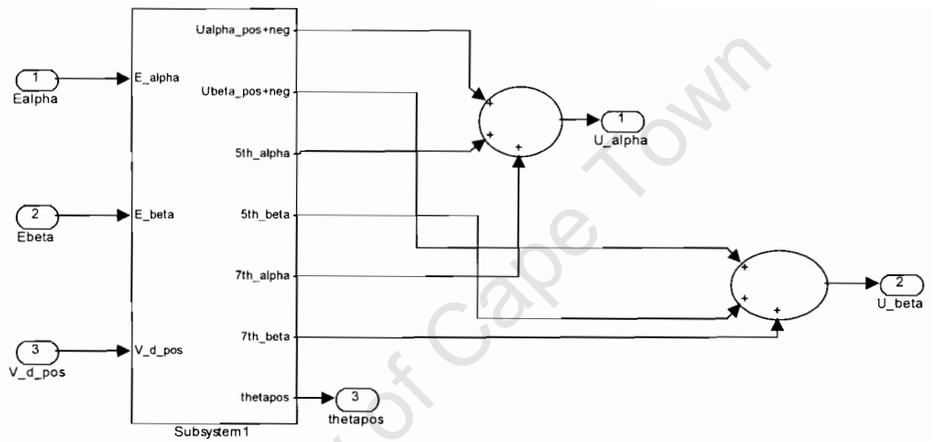


This is the "Hysteresis Current controller" block. This is where the actual currents are compared to the reference currents to obtain the switching signals for the shunt converter.

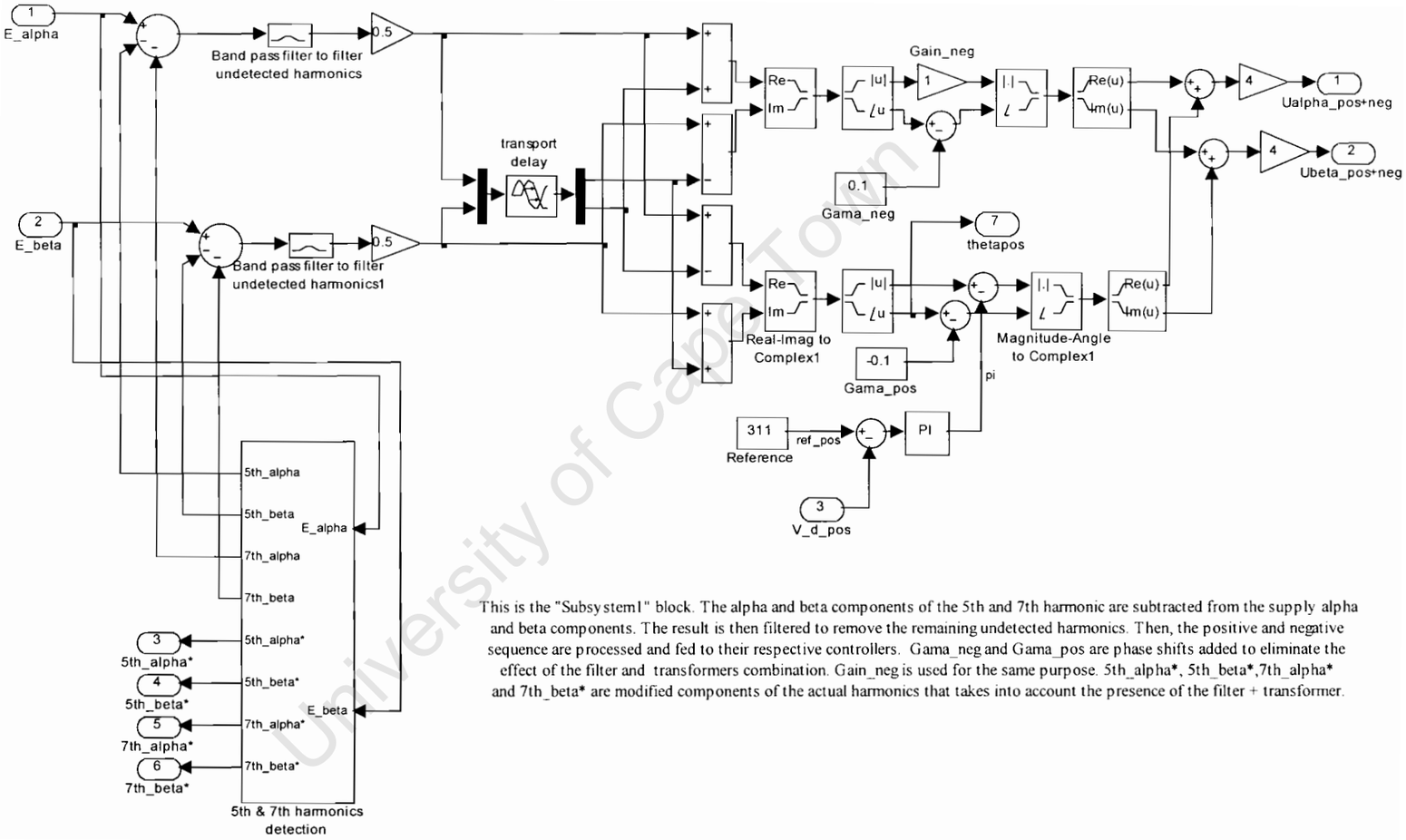




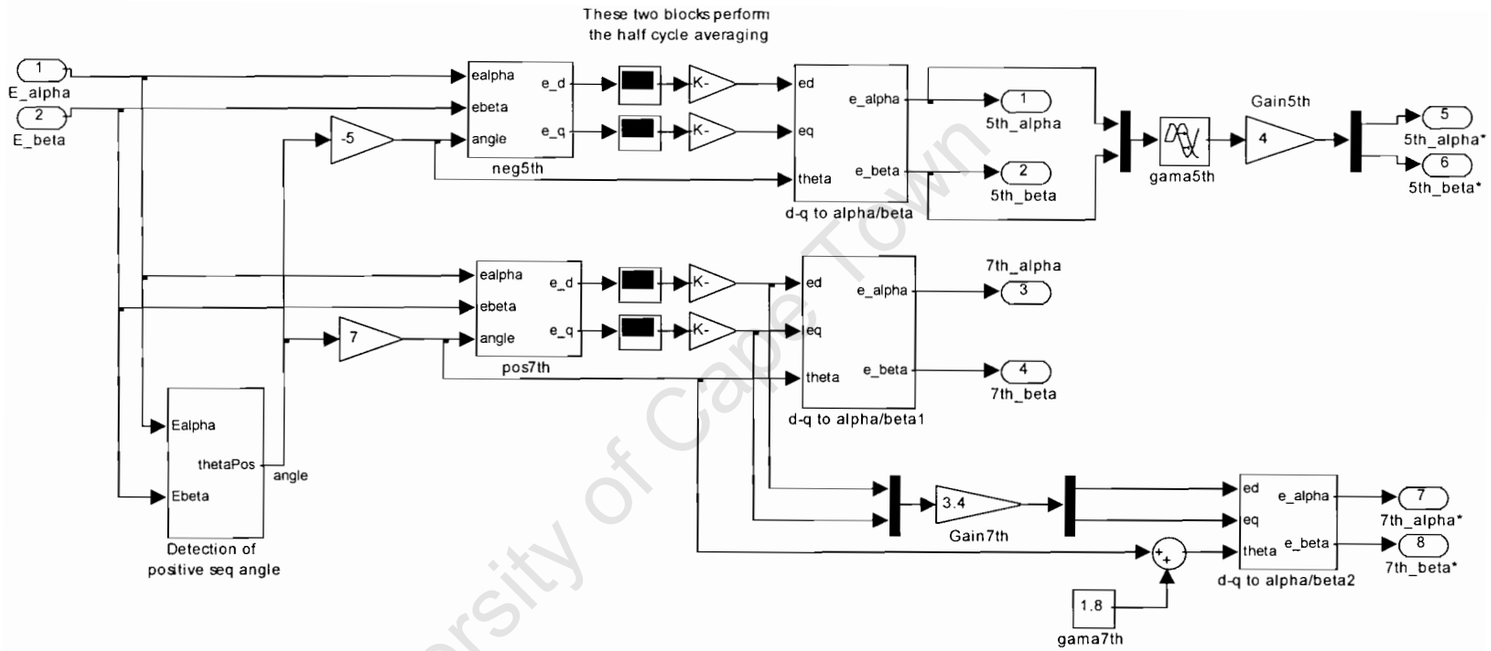
This is the "PWM" block. The hysteresis switching signals are sent to the i/o ports using the "master bit out" blocks. The switch is used to start and stop switching.



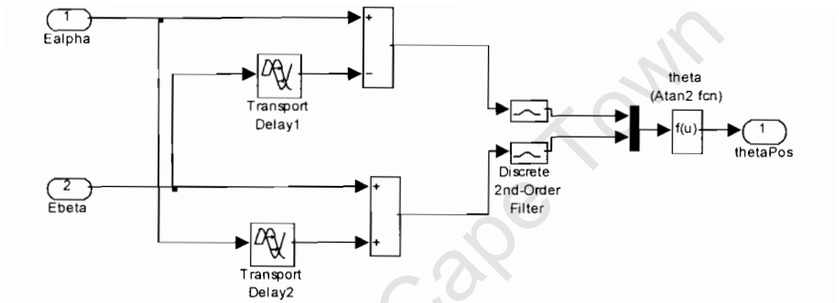
This is the "Control Algorithm" block. The 5th and 7th harmonics as well as the positive and negative sequence components that need to be injected into the system are added to obtain U_alpha and U_beta which are the inputs to the Space Vector pwm algorithm



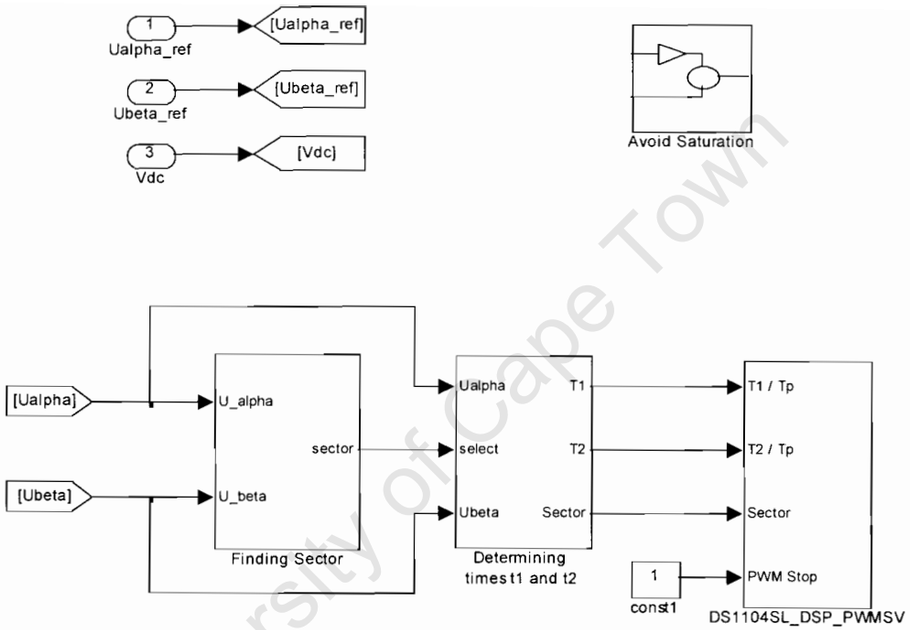
This is the "Subsystem1" block. The alpha and beta components of the 5th and 7th harmonic are subtracted from the supply alpha and beta components. The result is then filtered to remove the remaining undetected harmonics. Then, the positive and negative sequence are processed and fed to their respective controllers. Gama_neg and Gama_pos are phase shifts added to eliminate the effect of the filter and transformers combination. Gain_neg is used for the same purpose. 5th_alpha*, 5th_beta*,7th_alpha* and 7th_beta* are modified components of the actual harmonics that takes into account the presence of the filter + transformer.



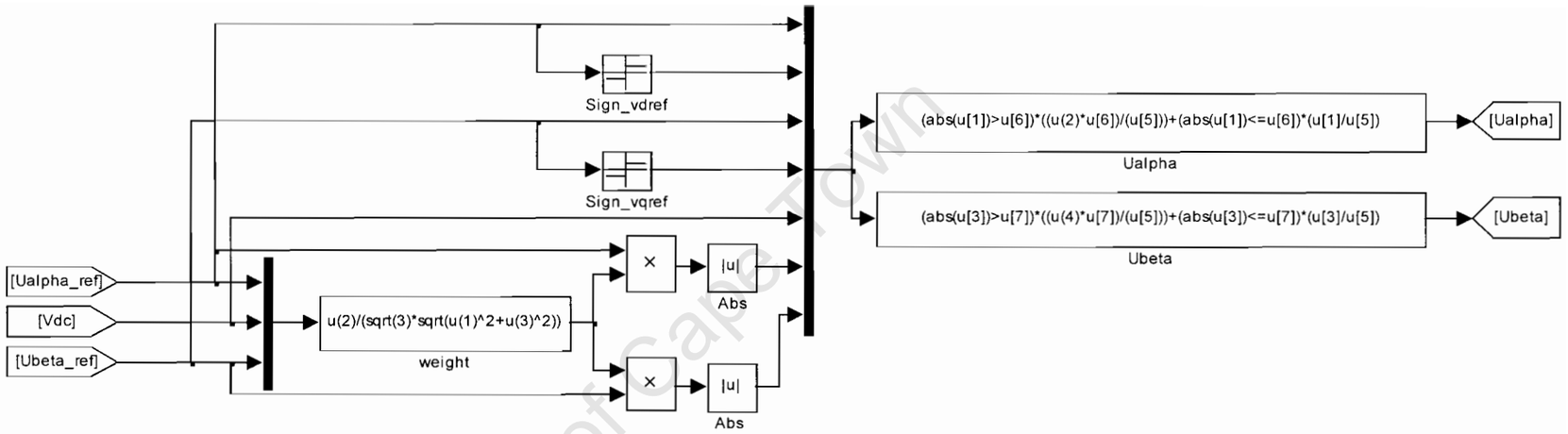
This is the "5th & 7th harmonics detection" block. Only the negative sequence 5th harmonic and positive sequence 7th harmonic are detected to reduce the amount of compututation in order to achieve a resonable large sampling frequency. The supply alpha and beta components are transformed to different synchronous frames where the 5th and 7th harmonics are isolated. Then, using the half cycle averaging technique, they are measured. Thereafter, they are transformed back to the stationary frame. Gain7th, Gain5th, gama7th and gama5th are introduced to eliminate the effects of the combination of the low pass filter and of the transformers on the injected harmonics. The modified harmonic components are injected by the series inverter while the true components of these harmonics are used to obtain the fundamental components of the supply voltage.



This is the "Detection of positive seq angle" block. The positive sequence voltage of the supply is first extrated. Bandpass filters are then used for filtering all the harmonics present before the the supply positive sequence angle is computed

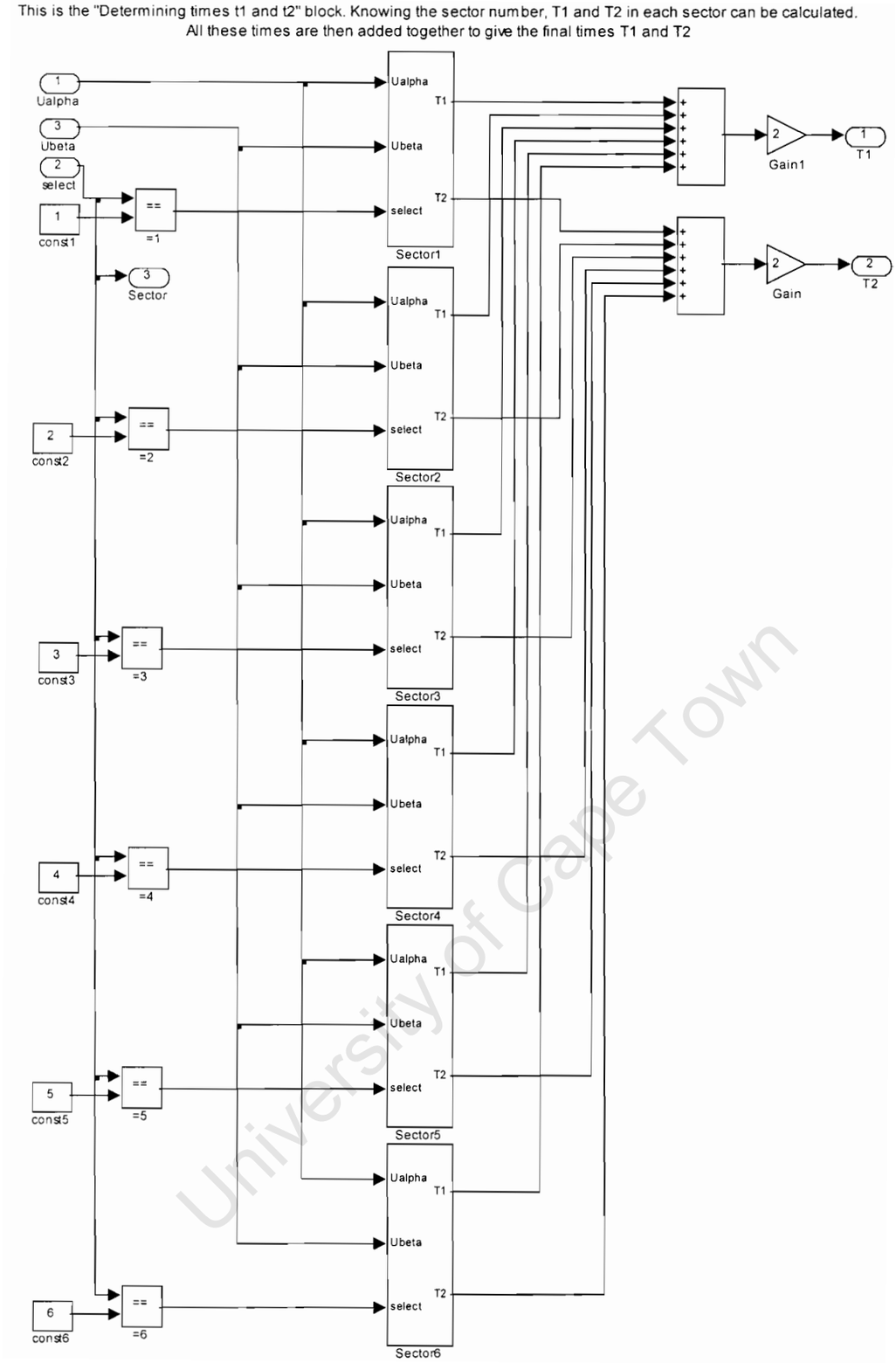


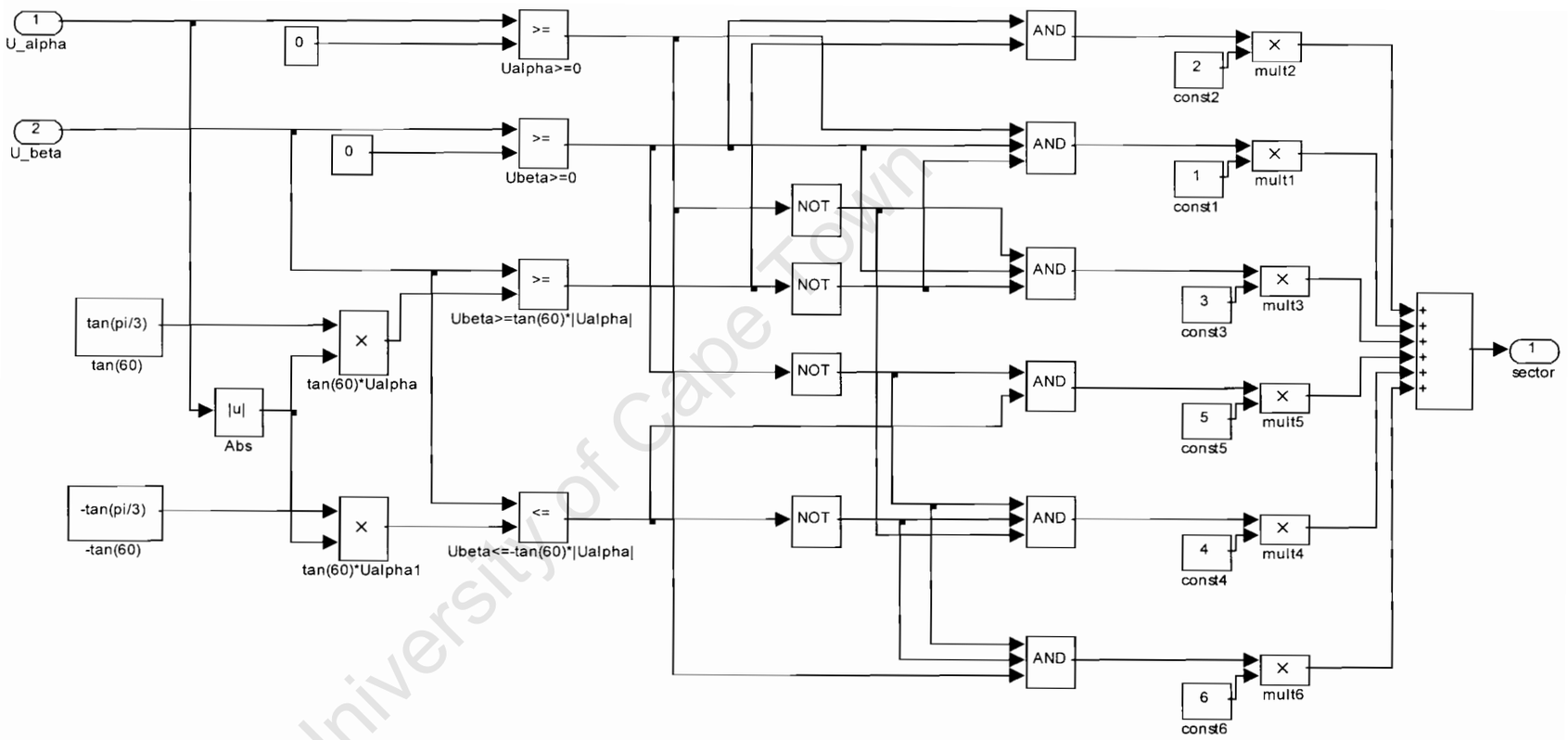
This is the "SVPWM" block. The SVPWM algorithm is processed here. First, the alpha and beta components are scaled down by the "Avoid Saturation" block if they exceed the maximum limit.The sectors in which the vector lies are computed and times T1 and T2 are found. The sector number and the two times are then fed to the DS1104SL_DSP_PWMSV block which produces the switching signals on the CPL1104 panel



This is the "Avoid Saturation" block. The alpha and beta components from the control algorithm are limited to a maximum value so that the vector Uout does not exceed Vdc/sqrt(3). First, the maximum allowable value of Ualpha and Ubeta is processed. Then, the actual values of Ualpha and Ubeta are compared to that maximum. If they are smaller, they are unchanged. However, if they exceed that maximum value, they are shrunk to the maximum value allowable.

This is the "Determining times t1 and t2" block. Knowing the sector number, T1 and T2 in each sector can be calculated.
All these times are then added together to give the final times T1 and T2





This is the "Finding Sector" block. The sector in which Uout lies is determined according to the flow chart given in chapter two of the thesis.

Thus is the block "Sector 1". Note that blocks for the remaining sectors are not shown in this appendix but they are similar to this one. Only the mathematical formulae, T_1 and T_2, changes according to the code describe in chapter 2 of this thesis.