Load Compensation

Design of a Real Time Analysis

and

Control Device

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in

Electrical Engineering

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To

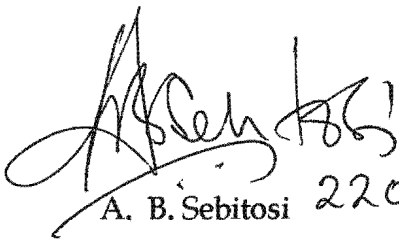
the glory of God

and

Peace on earth

Declaration

The thesis is submitted as a requirement for the award of the degree of Master of Science in Electrical Engineering at the University of Cape Town. It has not been submitted before at this or any other university. The author hereby confirms that it is based on his own work.



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Finally to my family, Esther, Sandra, Gideon and Benja who have had to fend for themselves.

Abstract

The aim of this thesis is to produce a load compensator for a three-phase system. It should be simple, accurate and affordable.

The three-phase load compensator design is based on a more recent definition of power factor. Attempts to establish a universally acceptable definition can be traced as early as 1920 at the 36th Annual convention of the American Institution of Electrical Engineers. Subsequently, a number of definitions have been adopted by different scholars. Each definition can lead to a different compensator solution. This problem for, example, is illustrated by Emanuel [25].

A highly respected approach was recently presented by L. S. Czarnecki [11]. He defined a three-phase system current vector, I, consisting of the line currents, i_r, i_s and i_t as the elements. $I = [i_r\ i_s\ i_t]^t$. He decomposed the system current vector into a set of orthogonal current components namely, active current, reactive current, harmonic current and scattered current.

The load balancing technique used in this thesis was based on Czarnecki's definition of orthogonal currents. The presentation is however limited to a symmetrical and sinusoidal supply fed to a linear load where, the scattered and harmonic currents are assumed to be negligible.

A major contribution of this thesis is the derivation of the compensator values. A model using two line currents and two line voltages measured in real time was designed. It was successfully simulated and tested on a real load. The design's versatility was demonstrated further by successfully controlling a single-to-three-phase compensator for a complex three-phase load.

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1. Introduction

1.1 Background and objectives

The author researched load compensation through an extensive study of a range of proposals and load compensating methods used over the years. One method, in particular, "a balancing compensator," as proposed by L.S. Czarnecki [11], is studied in greater detail. In brief, this proposal suggests that by measuring only two line currents and two line-to-line voltages of an unbalanced linear complex load, supplied with a symmetrical and sinusoidal three-phase voltage, it is possible to design a load compensator to correct both power factor and load unbalance.

The goal of this thesis was to establish the viability of this proposal by:

- Studying and compiling a literature review on load compensation.
- Designing a compensator model, using analogue circuit techniques.
- Performing computer simulations of the design and using the space vector for analysis.
- Physically constructing the design with ordinary off-the-shelf components.
- Finally testing, in the laboratory, the constructed compensator system.

The author is not aware of any prototype or commercial product designed along this proposal.

As time and opportunity may permit, if the above equipment should succeed in achieving the initial goal, a brief investigation may be carried out into its versatility, on another application.

1.2 The need for load compensation in power systems

T. J. E. Miller [9] has defined load compensation as the management of system reactive power to improve the quality of ac power supply.

It is estimated that over thirty percent of all primary energy resources worldwide are converted to electrical energy and inefficient use of electricity has profound impact on the environment. Between 6-10% of this generated power is lost, while being delivered to the consumer [8]. Rising costs of construction materials and labor mean that older networks have to continue for longer than perhaps initially planned and cable wear and tear through heating must be minimized.

Transmission of vars and negative sequence currents all the way from generation to consumers is a major contributor of power delivery losses and generator inefficiency. Because cable warming is proportional to the square of the current, (I^2R), small current imbalances result in noticeable increases in cable heating. Analysis has shown [3], that copper loss during load unbalance is the sum of the loss due to positive sequence and negative sequence currents considered separately, while that due to power factor as a result of reactive loading (typically lagging) increases as the inverse square of the power factor, $1/\lambda^2$, (where, λ, the power factor is defined as the ratio of the real power, P, to the total apparent power, S, generated by a voltage source).

The demand for higher power quality is increasing daily as the use of more sophisticated but power-vulnerable microelectronics control based equipment increases. It has been verified that in addition to losses incurred by the utility, as a result of the above problems, the quality of power is compromised.

In his paper, "Reactive power and unbalanced circuits", Waldo Lyon [3], (a professor at the Massachusetts Institute of Technology), says of load unbalance and power factor, ".... the capacities of all generating, transforming and

distributing devices are reduced and an additional burden is thrust upon the producer. If the line voltages are unbalanced, as a result of the unbalanced currents, all symmetrical poly-phase motors will take additional reverse-phase-order currents, the effect of which is two fold. The capacities of the motors are reduced and their losses are increased".

In some countries like Uganda, with unplanned suburban housing estates, a single-phase can be extended (from a local substation transformer) for kilometers on a string at the expense of the other two phases. This often causes transformer under utilization and premature failure. Moreover, the resulting negative sequence currents that get dumped on the system are unlikely to be canceled as they are not planned for. In planned housing the power utility attempts to match the number of single-phase consumers per phase. But even in such cases equating of line currents on a given substation, in the author's experience, rarely exceeds 70%.

This is especially highlighted for private generator sets where a trip circuit rated for a full capacity of 100 amperes may go off when one of the lines is only delivering 60 amperes, as tripping only requires one line current to exceed the threshold. In a typical case the interpretation will be that the generator is undersize; either forcing some functions to be abandoned or purchasing a new and much bigger than necessary generator set. This also does not guarantee that the existing installed cabling will be adequate.

This scenario is very common is East Africa, where cash strapped public power utilities are often generating 30% below their consumer capacities, forcing consumers to look for their own alternative means. The Government of Kenya, for example, has sought to address the problem in one way by waiving fuel duty for industrial consumers with generator sets of 100kva and over, to encourage them to be more self reliant and ease demand on the public utilities.

Furthermore, such circumstances also imply that only the existing urban and industrial consumers, that constitute some 8% or so, will be maintained, leaving the hapless but otherwise viable upcoming rural enterprises to fend for themselves.

Loads that consume vars tend to depress voltages at their points of connection. One might perhaps argue that pre-empting this by installation of permanent capacitance would solve the problem. However since the load demand for the vars continuously varies a practically similar problem due to excess rise in the terminal voltage, at times of low var demand, would have different but equally undesirable consequences. Hence the need to compute the appropriate compensator parameters at a particular moment.

Utilities in East Africa erroneously assume the effects of load unbalance to be always subtractive on a macro level and only act to remedy reactive loading. As a deterrent to the consumer a surcharge for reactive power consumption is incorporated in the bill.

In countries like the USA public power utilities require that consumers take responsibility for both their power factor and balancing of their load currents. As international laws and norms get standardized it will be a matter of time before our local regulations take cue. When one considers such heavy single-phase consumers like the railways, arc furnaces, arc welders and induction welders it would be wrong to assume that some system load distribution matching would take care of such large amounts of negative sequence currents, or for the power supply utility to provide the compensation at no extra cost.

So concludes Lyon [3], "Both unbalancing current and low power factor increase loss in the circuit and the necessary capacity of infrastructure and should be penalized".

1.3 Structure

The thesis is divided in four chapters excluding this one.

Chapter 2 begins by restating the basic objectives of the thesis. It explains, with illustrations, the following terms: space vector, power factor (both in single and three-phase), unbalance and compensation.
It then continues by reviewing theories of various models of compensators proposed by different designers for similar or different applications and discusses their merits and limitations. A special example of single-phase load compensation is shown for the arc furnace.

Chapter 3 covers computer simulations. It begins by defining and then analyzing an ideal load, with illustrations, using the space vector. These results are later used to judge the performance of a load compensator. More illustrations are used to explain the terms, load current, source current and compensator current.
A complete model for measuring the admittance of a complex three-phase linear load is designed. The details of its conception from basic principles are covered.
Finally a fully automated compensation of a random complex load is successfully simulated. The results are displayed as a series of oscilloscope waveforms and space vector loci.

Chapter 4 covers the practical implementation of the model designed earlier. It compares and contrasts the problems of physical component circuitry with those of computer toolboxes. The techniques used to overcome the practical problems

are discussed. The climax of this chapter is when the compensator achieves load balance and power factor correction.

Chapter 5 explores the versatility of the admittance meter with a different type of problem; the operation of a three-phase load with a single-phase supply. A series of formulae to be used are derived. The various problems encountered as well as their solutions are discussed. Computer simulations are successfully carried out. Finally the physical design and construction of additional circuitry is illustrated and also carried out. Due to lack of time the laboratory tests were not done.

2 A Review of a variety of load compensation methods

2.1 Introduction

This review covers definitions, concepts, designs and practices in the field of load compensation. Key words are, total apparent power, reactive, unbalance, compensator, symmetrical and sinusoidal.

2.1.1 Objectives

As has been stated earlier, unbalanced and reactive loads result in additional power delivery losses and reduce the general performance of all power system functions.

In this thesis the basic objectives are:

- Reduction of the system reactive power requirement.
- Restoration of supply current balance.

By achieving the above two objectives one can improve on generator efficiency, transmission line power quality and efficiency and voltage balance. It is also worth noting that load currents and load power factor cannot be changed. It is the source currents and power factor that are changed by a load compensator.

An ideal compensator is one that will correct the power factor to unity and reduce current unbalance to zero. It will provide "stepless" responses to load changes by instantaneously injecting the correct compensator currents and in addition will be unaffected by voltage supply fluctuations.

In practice there are a variety of factors one weighs against, for an optimum compensator in a specific context, not least of which is economics. For example, achieving a power factor of 0.95 is regarded as optimum by some industrial consumers. As for the smoothness of the steps, it's normally practical to switch in

predetermined sizes of reactive components, from a bank. Load patterns also vary from types that have long term predictability and only require routine checks (for semi-automated switching) to those that are continuously varying and require continuous monitoring and automated compensation.
This thesis will only consider the effects of power factor and load unbalance as undesirable. It will be assumed that, harmonic and scattered currents are negligible. The supply voltages will be sinusoidal and symmetrical and loads will be linear.

2.2 The Space vector

This is an approach to the real time analysis of asymmetry in three-phase steady state systems. It will be used extensively in this thesis. The following is a review of this concept, initially developed by K P Covacs and I Razc [13]. It involves the transformation of the values of a three-phase system into a two-dimensional vector system. This was initially conceived for the two dimensional control of rotating machines that have three-phase balanced windings.

Let figure 2.1 represent a motor. Its windings are balanced and are along axes OA, OB, and OC. Their magnetic field forces are along OA', OB' and OC'. Let the direction of field force OA' be taken as the reference. Then the other two field forces can be resolved both in phase as well as in quadrature with OA', by the following expressions.

Let F be the system magnetic field force.

$F = A' + B'(\cos 120° + j\sin 120°) + C'(\cos(-120°) + j\sin(-120°))$

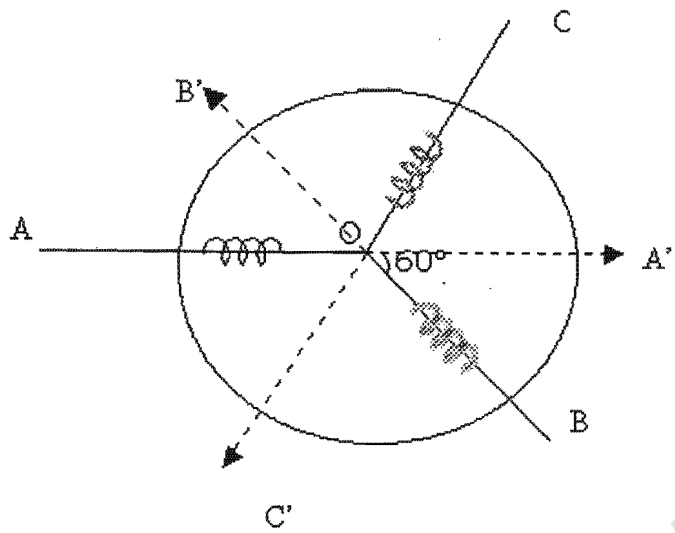

Figure 2.1

$F = A' + B'(-1 + j\sqrt{3})/2 + C' (-1 - j\sqrt{3})/2$ (where F is the resultant (real time) two dimensional force vector)

$a^2 = -(1 + j\sqrt{3})/2$ and $a = (-1 + j\sqrt{3})/2$

Therefore the field magnetic space vector, F, can be defined as

$$F = A' + aB' + a^2C' \qquad (2.1)$$

This is a mathematical coordinate transformation. The orientation of unit vectors 1, a and a^2 is independent of the spatial orientation of the three-phase equipment. This useful transformation and can also be applied to transformers, transmission lines and three-phase loads, with, flux, current and/or voltage as the parameters to be analyzed for asymmetry. This analysis is valid for periodic functions as well as dc conditions.

Let us consider a special case represented by the phasor diagram in figure 2.2.

Three balanced line current phasors, I_a, I_b and I_c, are in positive sequence.

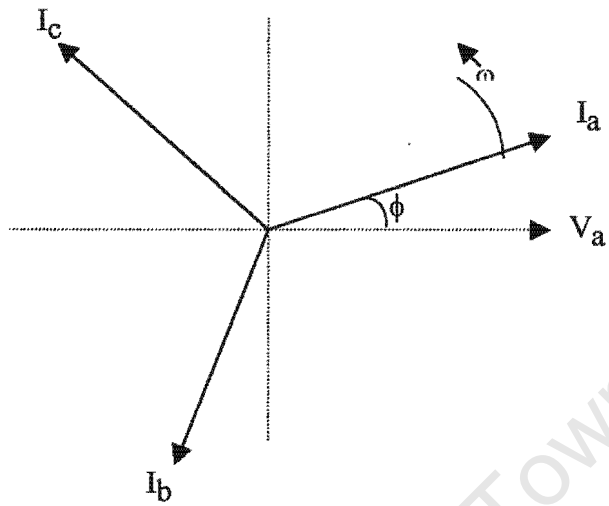

Figure 2.2 (Three-phase currents leading)

V_a is the reference voltage of a three-phase supply. Current I_a is sinusoidal and has a maximum amplitude, I_1. The angular frequency of I_a is (equal to that of V_a) ω radians per second and leading the reference voltage, V_a, by ϕ radians. The three-phase voltage supply is sinusoidal, symmetrical (relative phase differences are $2\pi/3$ radians) and in positive sequence. The instantaneous values of the line currents above are therefore given by

$$i_a = I_1\cos(\omega t + \phi)$$

$$i_b = I_1\cos(\omega t + \phi - 2\pi/3)$$

$$i_c = I_1\cos(\omega t + \phi + 2\pi/3) \qquad (2.2)$$

Using Euler's identity:

$$e^{j\theta} = \cos\theta + j\sin\theta \quad \Rightarrow \quad \cos\theta = \mathrm{Re}(e^{j\theta})$$

From Euler's identity and the definition of space vector in the example in figure 2.1 it can be shown that the system current vector is given by

$$i_1 = I_1 e^{j\phi} e^{j\omega t}$$

$$= I_1 e^{j\omega t} \text{ (since } I_1 e^{j\phi} \text{ is a constant, } I_1 \text{ is a complex number)} \quad (2.3)$$

This is the same usual expression for a complex alternating current phasor whose locus is a circle at a constant angular velocity, ω. This set up constitutes a symmetrical positive sequence and the direction is anticlockwise.

On the other hand if the currents in figure 2.2 were to rotate in the clockwise direction then they would be said to be in negative sequence and their expressions would be

$$i_a = I_1 \cos(\omega t + \phi)$$

$$i_b = I_1 \cos(\omega t + \phi + 2\pi/3)$$

$$i_c = I_1 \cos(\omega t + \phi - 2\pi/3) \quad (2.4)$$

Likewise the expression for the system negative sequence current, I_2, can be shown to be $i_2 = I_2 e^{-j\phi_2} e^{-j\omega t}$. This rotates in the negative (clockwise) direction at the same angular velocity but a different maximum amplitude, I_2.

In a load unbalance situation both sequences are present. The total system current vector is the sum of an anti-clockwise circular locus and a circular clockwise locus. The result is an ellipse, as shown in figure 2.3.

As will be illustrated later a compensator to redress the system current unbalance exploits Kirchhoff's current law (KCL). A node on a load current supply line, is injected with a component of current equal to the negative sequence of the load current for that line. Since the load current cannot change, the source is relieved from supplying that component.

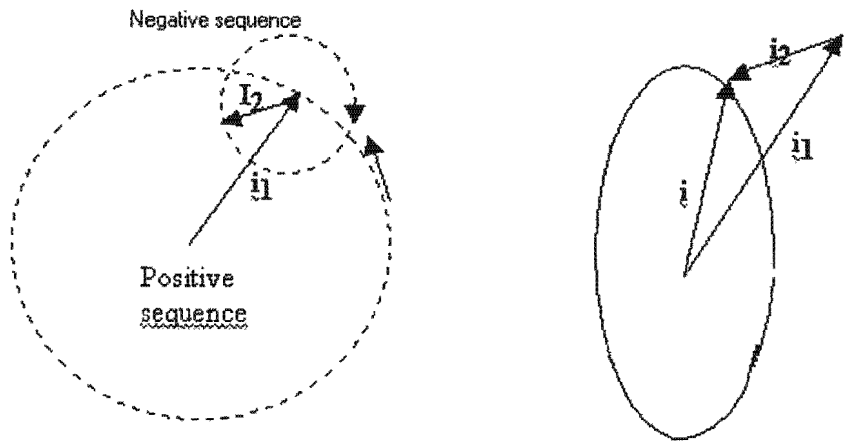

Figure 2.3

Summation of positive and negative sequence space vector currents

$i = i_1 + i_2 = I_1 e^{j\phi} e^{j\omega t} + I_2 e^{-j\phi_2} e^{-j\omega t}$ (the sum of the positive and negative sequence)

2.3 Compensator concepts

The purpose of this is to explain the relationship between the power source, the load and the compensator.

2.3.1 Reactive current and Power factor in single-phase

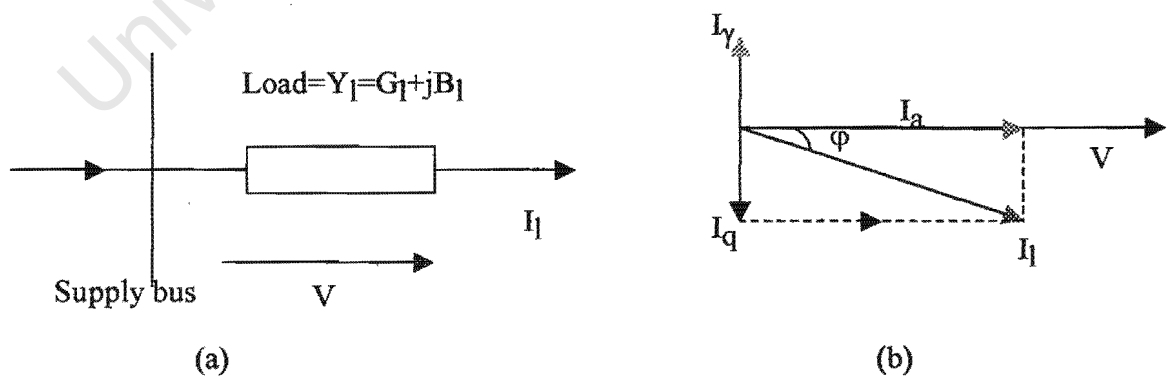

Figure 2.4

Complex single-phase load and its current and voltage phasors

Figure 2.4a is a Thevenin model. A single-phase load with admittance, Y_l, is comprised of a conductance G_l and a susceptance, B_l.

$Y_l = G_l + jB_l$ is supplied with a voltage V, resulting in I_l, the load current. Therefore,

$$I_l = V(G_l + jB_l) = VG_l + jVB_l = I_a + I_q \quad (2.5)$$

Figure 2.4b is a phasor representation of 2.4a. Positive rotation is anticlockwise. Voltage V is the reference. Current I_l is said to lag the voltage. Such a load has an inductive susceptance and a resistive conductance. The load current can be decomposed into two components. I_a is the active current, which is due to the conductance and is in phase with the supply voltage. I_q is the reactive current, and is due to the susceptance. It is in quadrature with the supply voltage.

Let φ be the phase angle between the supply voltage, V, and the load current I_l.

If S_l is the total apparent power supplied by the voltage source, then

$$S_l = VI^*_l = V^2 G_l - jV^2 B_l = P_l + jQ_l \quad (2.6)$$

Note that

- Phasors are valid for steady state system conditions.
- Power quantities are scalar (not vector or phasor entities).
- I^*_l is the complex conjugate of I_l.
- P_l is called the real power component (or physically useful part) of S.
- Q_l is called the reactive power component. It has no tangible use but the peculiar nature of the load is such that it inherently requires it. It also contributes to system inefficiency.

The power factor, λ, is defined as the ratio of the real power, P_l to the total apparent power, S. It is equal to the cosine of the phase angle between V and I_l.

$$\lambda = \text{Cos}\varphi = P_l / S_l \qquad (2.7)$$

The concept of power factor correction is to find a substitute source for the reactive power. Then the voltage supply source is left to generate only the useful active power, P_l. This is the task of the compensator. If the reactive part of the load is jB_l, then power factor compensation is done by connecting, in parallel to the load, a pure susceptance of an equal but opposite value, $-jB_l$. The total supply source current, I_s, will then be given by the sum of the original load current, I_l and that of the compensator element, I_γ.

$$I_s = I_l + I_\gamma = V(G_l + jB_l) + V(-jB_l) = VG_l = I_a \qquad (2.8)$$

The above scenario can be viewed from a trigonometric point of view.
Let a load, Z, comprising of constant values of resistance, R, and inductance, L, be fed with a purely sinusoidal voltage, *E*.
The resulting current ***i*** is given by

$$i = \sqrt{2}I \sin \omega t \quad \text{(where } I \text{ is the rms value of the current)} \qquad (2.9)$$

The voltage drop across the load is given by

$$e = Ri + L\,(di/dt) \qquad (2.10)$$

Substituting in ***i*** we get

$$e = R\sqrt{2}I \sin \omega t + L\omega\sqrt{2}I \cos \omega t$$

The instantaneous power delivered to the load is

$$s = ei = RI^2(1 - \cos 2\omega t) + \omega L I^2 \sin 2\omega t \qquad (2.11)$$

The average active power to the load is

$$P_a = RI^2 \tag{2.12}$$

The maximum power to the magnetic field of the inductor is

$Q_r = \omega LI^2$ (is the reactive power and is delivered to the magnetic field in one half of the cycle and then back to the source in the other half.)

The total apparent power is *EI* and is given by

$$(EI)^2 = (RI^2)^2 + (\omega LI^2)^2 \tag{2.13}$$

Power factor is the ratio of the active power to the total apparent power

$$\lambda = Cos\theta = \frac{RI^2}{\sqrt{(RI^2)^2 + (\omega LI^2)^2}} \tag{2.14}$$

2.3.2 The unbalance current, I_u

- ***Unbalance defined in the symmetrical components context***

When the currents in a three-phase system are not equal they are said to be unbalanced. In this context the supply voltages are symmetrical and sinusoidal and the load is linear. Therefore the system current unbalance is directly proportional to the extent of the unbalance of the three-phase load.

One way of evaluating the extent of load unbalance is the method of symmetrical components as introduced by Fortescue [1]. This is covered later, in detail, in

section 2.4.3. In brief, it states that any three-phase system of unbalanced currents can be presented by three sets of, equal positive sequence, equal negative and equal zero sequence currents.

In a balanced situation the negative sequence currents are zero. Making this observation, J. Slepian [5], defined the extent of unbalance as the unbalance factor and is equal to the, "…. the ratio of the magnitude of counter-rotational and direct-rotational components."

The following expression gives the value of the reference phasors for the symmetrical current components. They are, the zero sequence, I_{a0}, the positive sequence, I_{a1} and the negative sequence, I_{a2}. The line currents are I_a, I_b and I_c.

$$\begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.15}$$

Zero sequence currents are often zero. The magnitudes of the other phasors in each sequence are equal. Therefore the unbalance factor is equal to the ratio of the magnitude of the negative reference phasor to the positive one.

$$\text{Unbalance factor, u.f.} = \frac{I_{a2}}{I_{a1}} = \left[\frac{| I_a + a^2 I_b + a I_c |}{| I_a + a I_b + a^2 I_c |} \right] \tag{2.16}$$

Then two extremes can be defined, namely, for a balanced three-phase system, when I_{a2} is equal to zero giving an unbalance factor of zero and the case of a single-phase, when I_{a1} is equal I_{a2} yielding a 100% unbalance factor as shown below.

From (2.15)

$$\begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} I_a \\ I_a \\ I_a \end{bmatrix}$$ for single-phase

Therefore

$I_{a1} = I_{a2}$. The same can be shown to be true if the single phase current is I_b or I_c since $\|a\| = \|a^2\|$.

The unbalance factor found much practical use mainly in analyzing unbalance in induction motors, like the effect of voltage unbalance on torque. For example the starting torque is given by

s.t = [1 – (u.f.)^2] x (positive sequence rotational torque.)

- ***Unbalance as defined by Czarnecki [11]***

Czarnecki [11] has defined the three-phase source current, i, due to a linear and time-invariant load as a vector whose elements are the line currents, i_R, i_S, i_T such that

$$i = [\, i_R, i_S, i_T \,]^T \qquad (2.17)$$

He has further decomposed this current vector into, the active current vector, i_a, the reactive current vector, i_q, the harmonic current vector, i_h, the unbalance current (due load unbalance), i_u and the scattered current, i_s (due to load conductance dependency on frequency). They are mutually orthogonal. In this thesis the voltages considered are symmetrical and sinusoidal, the loads are linear and the harmonic and scattered currents will be considered as nil.

Therefore the rms values of the load current vector components satisfy

$$\|i\|^2 = \|i_a\|^2 + \|i_q\|^2 + \|i_u\|^2 \tag{2.18}$$

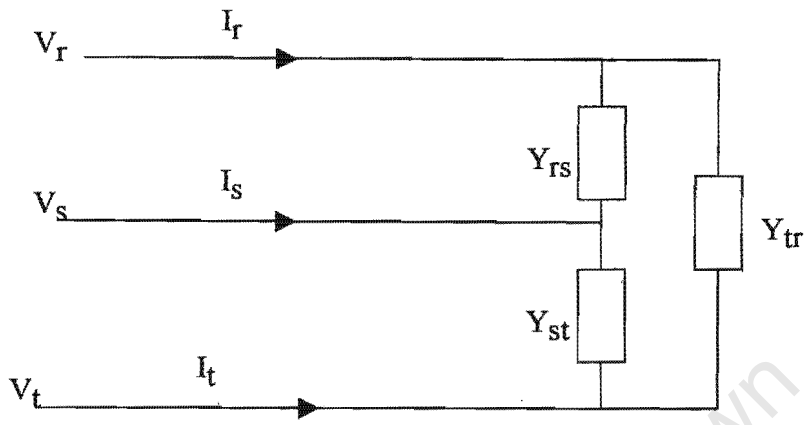

Figure 2.5

Figure 2.5 is a symmetrical and sinusoidal three-phase voltage supply, in positive sequence. The line-to-neutral voltages, V_r, V_s and V_t, are feeding an unbalanced but linear delta load Y_{rs}, Y_{st}, Y_{tr}. The line currents are, I_r, I_s, I_t.

The total complex power supplied by the source is

$$S = P + jQ = Y_{rs}V^2_{rs} + Y_{st}V^2_{st} + Y_{tr}V^2_{tr} \tag{2.19}$$

(where P is real power and Q represents the rest of the components of S)

In magnitude, $V_{rs} = V_{st} = V_{tr} = \|V\| = \sqrt{V_r^2 + V_s^2 + V_t^2}$ (2.20)

The system equivalent admittance, Y_e, as defined by Czarnecki is

$$Y_e = G_e + jB_e = Y_{rs} + Y_{st} + Y_{tr} \tag{2.21}$$

The total apparent power = $S = Y_e\|V\|^2$ (2.22)

$$S/\|V\|^2 = Y_e = G_e + jB_e \tag{2.23}$$

$$G_e = \mathrm{Re}(S/\|V\|^2) = \text{ (the equivalent conductance)} \tag{2.24}$$

$$B_e = -\mathrm{Im}(S/\|V\|^2) = \text{(the equivalent susceptance)} \tag{2.25}$$

The conductance is responsible for the active current i_a.

$$i_a = \begin{bmatrix} i_{ra} \\ i_{sa} \\ i_{ta} \end{bmatrix} = \sqrt{2}\mathrm{Re}\begin{bmatrix} I_{ra} \\ I_{sa} \\ I_{ta} \end{bmatrix} e^{j\omega t} = G_e V \tag{2.26}$$

The reactance is responsible for the reactive current, i_q.

$$i_q = \begin{bmatrix} i_{rr} \\ i_{sr} \\ i_{tr} \end{bmatrix} = B_e \frac{d}{d(\omega t)} V = \sqrt{2}\mathrm{Re}\begin{bmatrix} jB_e V_r \\ jB_e V_s \\ jB_e V_t \end{bmatrix} e^{j\omega t} \tag{2.27}$$

From which Czarnecki defines the unbalance current, i_u, as the remainder

$$i_u = i - (i_a + i_q) \tag{2.28}$$

Thus is the concept of the unbalance current, i_u. (In the three-phase dimension it constitutes the negative sequence currents)

Looking at each phase separately

For the red line, the complex rms value of the unbalance current, I_{ru}, is given by

$I_{ru} = I_r - (I_{ra} + I_{rq})$ (I_r is the total line current, I_{ra} is the active component and I_{rq} the reactive component in rms values) (2.29)

Line currents are related to the branch load currents as follows

$$I_r = I_{rs} - I_{tr} = Y_{rs}V_{rs} - Y_{tr}V_{tr} = Y_{rs}(Vr - Vs) - Y_{tr}(V_t - V_r) \quad (2.30)$$

(where I_r is the red line current and I_{rs} is the load branch current between lines r and s.)

And by Czarnecki's definition the total equivalent admittance

$$Y_e = G_e + jB_e = (Y_{rs} + Y_{st} + Y_{tr}) \quad (2.31)$$

And the sum of the active and reactive currents in line r is

$$I_{ra} + I_{rq} = V_rY_e = V_r(G_e + jB_e) = V_r(Y_{rs} + Y_{st} + Y_{tr}) \quad (2.32)$$

Therefore the unbalance current in line r is given by

$$I_{ru} = Y_{rs}(Vr - Vs) - Y_{tr}(V_t - V_r) - (G_e + jB_e)V_r$$

$$= -(Y_{st}V_r + Y_{rs}V_s + Y_{tr}V_t) \quad (2.33)$$

The supply is in positive sequence and so, $V_s = a^2V_r$, and $V_t = aV_r$

$$I_{ru} = -(Y_{st} + a^2Y_{rs} + aY_{tr})V_r \quad (2.34)$$

$$I_{ru} = AV_r \quad (2.35)$$

(A is defined by Czarnecki as the unbalance admittance; a fictitious component of the load admittance responsible for the unbalance current)

The other two line unbalance currents can be derived since they are in negative sequence and of equal magnitude ($I_{su} = aI_{ru}$ and $I_{tu} = a^2I_{ru}$).

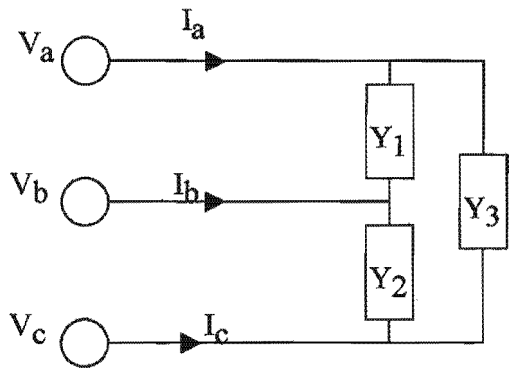

Figure 2.6

In section 2.3.2 the concept of symmetrical components was briefly introduced. A more detailed elaboration is in section 2.4.3.

In his approach to defining power factor in three-phase Emanuel [25] makes use of symmetrical components as is reviewed here. Zero sequence currents are assumed to be zero.

Figure 2.6 is a symmetrical positive sequence supply feeding an unbalanced linear three-phase load.

The supply voltages are

$V_a = V_1$; $V_b = a^2V_1$; $V_c = aV_1$ (V_1 is the reference phasor, $a = \exp(j120°)$ and $a^2 = \exp(-j120°)$)

The line voltages squared are determined by multiplying each phasor with its conjugate

$(V_a)^2 = \underline{V}a\underline{V}a^* = (V_1)^2$

$(V_b)^2 = (a^2 V_1)^2$

$(V_c)^2 = (a V_1)^2$

Summing up

$$(V_a)^2 + (V_b)^2 + (V_c)^2 = (V_1)^2 + (a^2V_1)^2 + (aV_1)^2 = 3E^2 \qquad (2.40)$$

(where E is the norm of each voltage phasor)

The line currents are

Therefore

$$I_{su} = -(a^2Y_{st} + aY_{rs} + Y_{tr})V_s = a^2AV_s \quad (2.36)$$

$$I_{tu} = - (aY_{st} + Y_{rs} + a^2Y_{tr})V_t = aAV_t \quad (2.37)$$

Now the total system unbalance admittance, A can be given by

$$A\|V\| = \|I_u\| \quad (2.38)$$

And

$$\|I\| = \sqrt{G_e^2 + B_e^2 + A^2}\ \|V\| \quad (2.39)$$

(where $\|I\|$ is the norm of the load current vector)

2.3.3 Power factor defined in three-phase

In section 2.3.1 power factor is illustrated in the context of a single-phase network. Its physical meaning is clear. A. E. Emanuel [25] has defined single-phase apparent power as the maximum active power that can be delivered to a load by a voltage source while the line rms current is maintained constant.

In the aforementioned section power factor was defined as the ratio of active power, P, to the total apparent power, S. The same definition still holds in three-phase. Problems arise with fine details. For example, is $S = S_a + S_b + S_c$ or $S = \|(P_a + P_b + P_c) + j(Q_a + Q_b + Q_c)\|$? Where a, b, c are the supply lines. P is active power and Q is the rest. It has been shown [25] that under certain multi-frequency conditions the answers will differ.

Total apparent power will be defined here in the already confined context of a sinusoidal, symmetrical voltage supply source and a linear load.

$I_a = I_1 + I_2$ (where I_1 and I_2 are the reference line positive and negative sequence currents respectively. Zero sequence currents are zero)

$I_b = a^2 I_1 + aI_2$

$I_c = aI_1 + a^2 I_2$ (2.41)

Squaring

$(I_a)^2 = (I_1 + I_2)^2$

$(I_b)^2 = (a^2 I_1 + aI_2)^2$

$(I_c)^2 = (aI_1 + a^2 I_2)^2$ (2.42)

Finally it can be shown that

$3I_1^2 + 3I_2^2 = (I_a)^2 + (I_b)^2 + (I_c)^2$ (2.43)

The apparent power is the product of the load current vector and the voltage vector.

Therefore

$S^2 = 3E^2 (3I_1^2 + 3I_2^2)$

$= (3EI_1)^2 + (3E I_2)^2$ (2.44)

The negative sequence component is undesirable. The positive sequence component of power comprises active and reactive parts of which only the active is desirable.

The active power component is the dot product of the system voltage vector and the system positive sequence current vector, I_1.

$3E \cdot I_1 = \text{Re}\,(3EI^*_1)$ (where Re stands for the real part) (2.45)

Finally power factor λ can be defined as

$\lambda = \text{Re}\,(3EI^*_1)/S$ (2.46)

2.4 Methods of compensation

2.4.1

In section 2.3 the function and purpose of a load compensator is illustrated. The depictions are of an ideal compensator. This section will cover the practical considerations for the choices of compensators, their designs, attributes and shortcomings.

2.4.2 Compensation using load admittances

A load compensator can be modeled by considering the actual load admittances. Gyugyi and others [7] presented a paper on this approach, as the following review reveals.

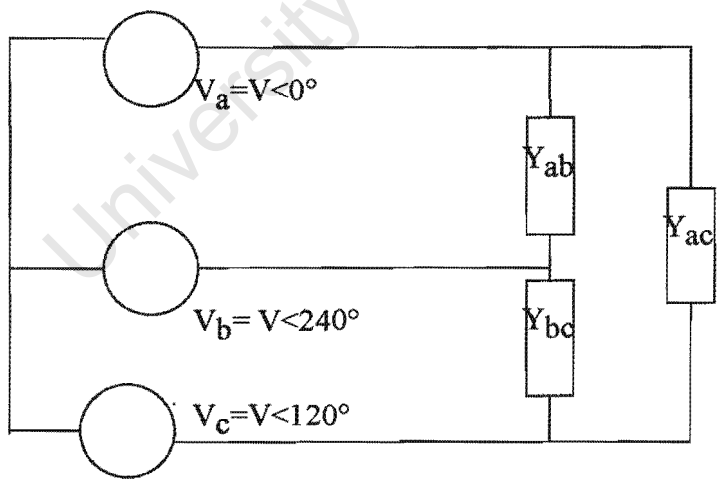

Figure 2.7

Figure 2.7 is a delta network with admittances, Y_{ab}, Y_{bc} and Y_{ca} fed with a symmetrical and sinusoidal three-phase supply in positive sequence. Let the three admittances be linear but unequal.

In section 2.3.1 a power factor correction concept was illustrated as the addition of an equal but opposite susceptance (in parallel) to a load branch admittance.

$$Y_{ab} = G_{ab} + jB_{ab} \tag{2.52}$$

In order to compensate Y_{ab} we must add, in parallel to it, a susceptance jB^*_{ab} where $B^*_{ab} = -B_{ab}$. So a full three-phase power factor compensator for this delta load will similarly add, in parallel to each of the other two branches, an equal but opposite susceptance value. Thereafter the voltage source will "see" the load as purely resistive (with conductances, G_{ab}, G_{bc} and G_{ac}) and won't generate any reactive currents. However the load will still remain unbalanced and the source will continue to generate negative sequence current components.

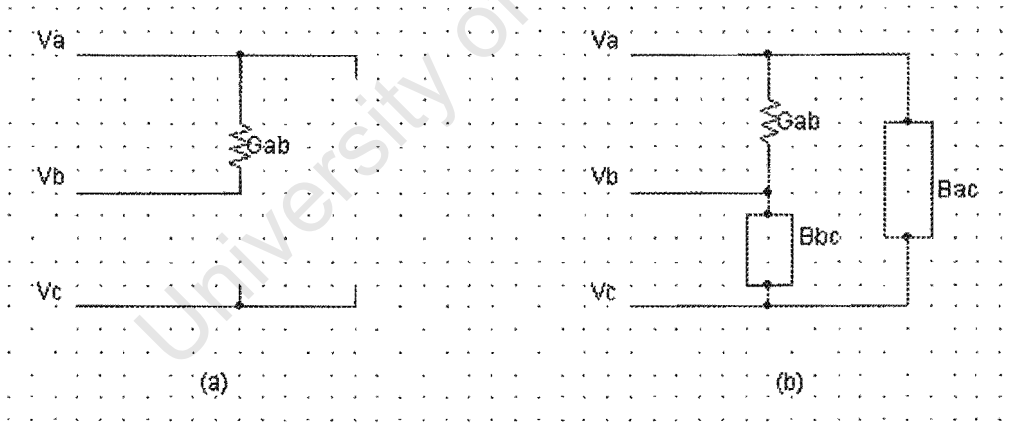

Figure 2.8

A single branch load with a three-phase supply

Consider figure 2.8(a), a single branch. The admittance Y_{ab} has become a conductance, G_{ab}, after it has been compensated for power factor, standing alone

on a three-phase supply. There will be negative sequence currents in the system due to this. To balance the system one requires to connect pure susceptances between phases, b and c and between a and c.

The superposition method is one convenient way to work out the line currents due to the individual phase voltages. Figure 2.9 illustrates the first two stages using superposition

$V_a = V$

$V_b = a^2V$

$V_c = aV$ (where a and a^2 are the 120° and 240° operators, $a = (-1/2+j\sqrt{3}/2)$, $a^2 = (-1/2-j\sqrt{3}/2)$, and are conjugates of one another.) (2.53, 2.54, 2.55)

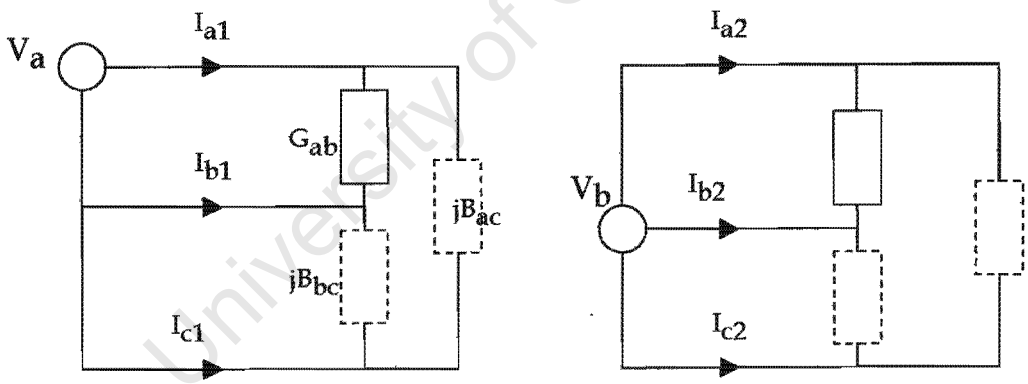

Figure 2.9

Illustrating the superposition method

Currents due to V_a are

$I_{a1} = V(G_{ab} + jB_{ac})$

$$I_{b1} = -VG_{ab}$$

$$I_{c1} = -jVB_{ac} \qquad (2.56)$$

Currents due to V_b:

$$I_{a2} = -a^2VG_{ab}$$

$$I_{b2} = a^2V(G_{ab} + jB_{bc})$$

$$I_{c2} = -ja^2VB_{bc} \qquad (2.57)$$

Currents due to V_c:

$$I_{a3} = -jaVB_{ac}$$

$$I_{b3} = -jaVB_{bc}$$

$$I_{c3} = jaV(B_{bc} + B_{ac}) \qquad (2.58)$$

The total line currents are the sum of the individual alphabetic subscripts like

$$I_a = I_{a1} + I_{a2} + I_{a3} \qquad (2.59)$$

At balance the source currents will be in positive sequence,

$$I_b = a^2I_a$$

$$I_c = aI_a \qquad (2.60)$$

Gyugyi et al finally got the following result (originally attributed to C.P. Steinmetz [2], at the beginning of the 20th century).

$$B_{bc} = (G_{ab})/\sqrt{3}$$

$$B_{ac} = (-G_{ab})/\sqrt{3} \qquad (2.61)$$

Since G_{ab} is a conductance it cannot be negative. Therefore B_{bc} is capacitive and B_{ac} is inductive.

Now having balanced the currents for G_{ab}, the same formula is used to balance the currents for each of the other two branches, G_{bc} and G_{ac}; handling each separately at a time. They are then added together with the susceptances for the reactive compensation, worked out using equation 2.6. The final product is a compensator for both load unbalance and power factor correction. The following expressions will be the values for each branch of the final compensator.

$$B^*_{ab} = -B_{ab} + (G_{ca} - G_{bc})/\sqrt{3}$$

$$B^*_{bc} = -B_{bc} + (G_{ab} - G_{ca})/\sqrt{3}$$

$$B^*_{ca} = -B_{ca} + (G_{bc} - G_{ab})/\sqrt{3} \qquad (2.62)$$

Where B^*_{ab}, is the total branch compensating susceptance for both load unbalance and power factor across phases a and b. It is important that to note that this compensator network will only be valid for the positive sequence since all the working data is derived from a positive sequence as illustrated in figure 2.7.

2.4.3 Load compensation by using symmetrical components

2.4.3.1 Method of computation

Equations 2.62 make good illustrations of what goes on in the process of load compensation. Unfortunately they assume that the load admittances are either known or can be measured; neither of which is possible in practice. A more practical approach is a formula that will yield compensating values in terms of line currents and voltages. Both of these can be easily measured.

One such approach is the principle of symmetrical components.

C. L. Fortescue [1], (in continuation of the works of A. Blondel and L. G. Stokvis), presented, "A method of symmetrical co-ordinates applied to the solution of polyphase networks".

In the context of a three-phase network the principle states that, any three-phase system of unbalanced currents can be presented as three sets of, equal positive, I_1, equal negative, I_2 and equal zero sequence currents, I_0.

Looking at figure 2.7, again, an unbalanced load is supplied by a set of symmetrical three-phase voltages, in positive sequence. Using V_a as the reference, we have

$$V_a = V;\ V_b = a^2V;\ \text{and}\ V_c = aV \qquad (2.63)$$

Where a and a^2 are the same 120° and 240° operators respectively, as previously described.

The above are line-to-neutral voltages. Line-to-line voltages are worked out by subtraction of pairs of the concerned branches as follows.

$$V_{ab} = V_a - V_b = (1 - a^2)V$$

$$V_{bc} = V_b - V_c = (a^2 - a)V$$

$$V_{ca} = V_c - V_a = (a - 1)V \qquad (2.64)$$

The load currents in figure 2.7can be worked out as follows

$$I_{ab} = Y_{ab}V_{ab} = Y_{ab}(1 - a^2)V$$

$$I_{bc} = Y_{bc}V_{bc} = Y_{bc}(a^2 - a)V$$

$$I_{ca} = Y_{ca}V_{ca} = Y_{ca}(a - 1)V \qquad (2.65)$$

The line currents are

$$I_a = I_{ab} - I_{ca}$$

$$I_b = I_{bc} - I_{ab}$$

$$I_c = I_{ca} - I_{bc} \qquad (2.66)$$

The symmetrical components referred to in [1] are given by

$$I_a = I_{a1} + I_{a2} + I_{a0}$$

$$I_b = I_{b1} + I_{b2} + I_{b0} = a^2I_{a1} + aI_{a2} + I_{a0}$$

$$I_c = I_{c1} + I_{c2} + I_{c0} = aI_{a1} + a^2I_{a2} + I_{a0} \qquad (2.67)$$

Which in matrix form

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} \tag{2.68}$$

Inverting

$$\begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.69}$$

I_{a0}, I_{a1} and I_{a2} are the reference (or line a) phasors for the zero-, positive and negative sequence.

Zero sequence currents are often zero and most certainly will be when the load balances. From equations 2.65 for I_a, I_b and I_c and substituted in equations, 2.66, we get

$I_{a0} = 0$

$I_{a1} = 1/3\,(I_a + aI_b + a^2I_c) = 1/3(I_{ab} - I_{ac}) + a(I_{bc} - I_{ab}) + a^2(I_{ca} - I_{bc})$

$=1/3(Y_{ab} + Y_{bc} + Y_{ca})V$

$I_{a2} = -1/3(a^2Y_{ab} + Y_{bc} + aY_{ca})V$ (2.70)

When the load is balanced, all admittances will appear equal ($Y_{ab} = Y_{bc} = Y_{ca}$) viewed from the source and equation 2.70 becomes

$I_{a2} = -1/3YV(a^2 + 1 + a)$

where Y is the admittance per branch

$(a^2 + 1 + a) = 0$ and therefore $I_{a2} = 0$ (under balanced conditions).

Imagine a delta compensator network with pure susceptances, B^*_{ab}, B^*_{bc} and B^*_{ca} connected on supply lines a, b and c. It will be seen by the supply, in one sense, like any other delta load. Therefore it will also have its symmetrical component currents given by

$I_{1c} = j/3(B^*_{ab} + B^*_{bc} + B^*_{ca})V$ (positive compensator current)

$I_{2c} = -j/3(a^2B^*_{ab} + B^*_{bc} + aB_{ca})V$ (negative compensator current) (2.71)

At balance therefore the sum of the load and compensator negative sequence currents must be zero. At unity power factor the sum of the positive sequence reactive components (imaginary parts) will be zero.

$I_2 + I_{2c} = 0$ (the subscript c is for the compensator) (2.72)

$Im\ (I_1 + I_{1c}) = 0$ (2.73)

- We get the load balancing values by solving equation 2.72

- We correct the power factor by canceling the imaginary parts of the positive sequence currents; solving 2.73.

$Y_{ab} = G_{ab} + jB_{ab}$

Therefore, if

$Im(I_1 + I_{c1}) = 0$ (where, ImI_1 is the reactive component of I_1)

then

$$V[(B_{ab} + B_{bc} + B_{ca}) + (B^*_{ab} + B^*_{bc} + B^*_{ca})] = 0 \quad (2.74)$$

The overall compensator values are

$$B_{\gamma ab} = -(ImI_{1l} + ImI_{2l} - \sqrt{3}ReI_2)/(3\sqrt{3}V)$$

$$B_{\gamma bc} = -(ImI_{1l} - 2ImI_{2l})/(3\sqrt{3}V)$$

$$B_{\gamma ca} = -(ImI_{1l} + ImI_{2l} + \sqrt{3}ReI_2)/(3\sqrt{3}V) \quad (2.75)$$

Note that the above equations are still in symmetrical current components. We must finally use the transformation matrix to convert the values in terms of normal line currents, I_a, I_b and I_c that can be measured as follows

$$B_{\gamma ab} = -(Im\ I_a + Im\ aI_b - Im\ a^2I_c)/3V$$

$$B_{\gamma bc} = -(Im\ aI_b + Im\ a^2I_c - Im\ I_a)/3V$$

$$B_{\gamma ca} = -(\text{Im } a^2 I_c + \text{Im } I_a - \text{Im } I_b)/3V \quad (2.76)$$

2.4.3.2 Compensator implementation using average real and imaginary power quantities

From equation 2.6 the reactive power supplied by a voltage source is equal to the imaginary part of the total apparent power S_l

$$\text{Im}S_l = \text{Im } VI^*_l = -jV^2 B_l$$

$$B_l = j(\text{Im } VI^*_l)/V^2 \quad (2.77)$$

Therefore equations 2.76 for the total compensator susceptances can be re-written as

$$B_{\gamma ab} = [\text{Im } V_a I^*_a + \text{Im } V_b I^*_b - \text{Im } V_c I^*_c]/3V^2$$

$$B_{\gamma bc} = [\text{Im } V_b I^*_b + \text{Im } V_c I^*_c - \text{Im } V_a I^*_a]/ 3V^2$$

$$B_{\gamma ca} = [\text{Im } V_c I^*_c + \text{Im } V_a I^*_a - \text{Im } V_b I^*_b]/ 3V^2 \quad (2.78)$$

Using instantaneous currents and voltages, real (or active) power is given as

$$\text{Re}[VI^*] = \frac{1}{T} \int_0^T vidt \quad (2.79)$$

In order to extract ImVI* using the same method we must integrate the current, I, multiplied by V(-π/2), the voltage delayed by 90°.

$$\text{Im } VI^* = \frac{1}{T}\int_0^T v(-\pi/2)i\,dt \qquad (2.80)$$

In practice it is possible to get a value, $v(-\pi/2)$, of one voltage that is perpendicular to another one as illustrated in figure 2.10.

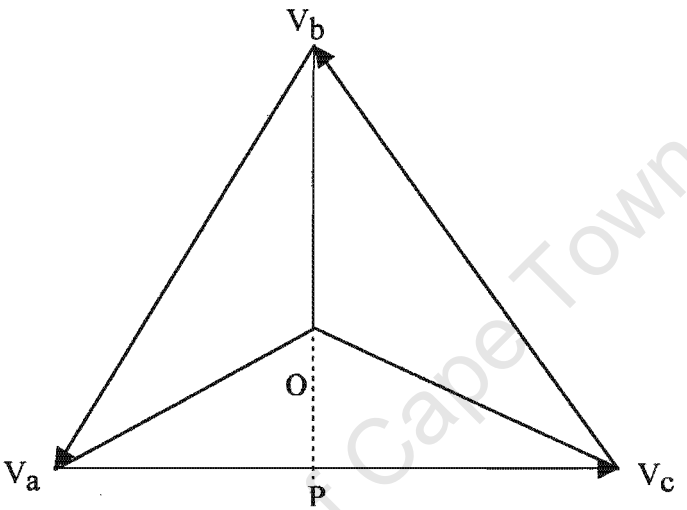

Figure 2.10

Figure 2.10 is a phasor representation of a symmetrical three-phase supply in positive sequence. V_{ao}, V_{bo} and V_{co} are the line-to-neutral voltage phasors. The figure demonstrates that if the line to neutral voltage V_{bo} is extended to point P it will intercept line-to-line voltage V_{ac} at 90°.

$$V_{ac} = -j\sqrt{3}V_{bo} \qquad (2.81)$$

So equations 2.78 can be re-written as

$$B_{\gamma ab} = 1/(3\sqrt{3}V^2)\ \frac{1}{T}\int\ (v_{bc}\,i_a + v_{ca}\,i_b - v_{ab}\,i_c)\,dt$$

$$B_{\gamma bc} = 1/(3\sqrt{3}V^2)\ \frac{1}{T}\int\ (v_{ca}\,i_b + v_{ab}\,i_c - v_{bc}\,i_a)\,dt$$

$$B_{\gamma ca} = 1/(3\sqrt{3}V^2)\ \frac{1}{T}\int\ v_{ab}\,i_c + v_{bc}\,i_a - v_{ca}\,i_b)\,dt \qquad (2.82)$$

Equations 2.82 are usable in a practical compensator control situation since they are in mathematical forms that can be converted into electronic circuitry.

2.4.3.3 Compensator implementation using instantaneous currents and voltages (By sampling method)

The instantaneous value of the line current in phase A can be represented by the following equation

$$i_a = \sqrt{2}\,Re\,[(I_{aR} + I_{ax})e^{j\omega t}$$

$$= \sqrt{2}(I_{aR}\cos\omega t - I_{ax}\sin\omega t) \qquad (2.83)$$

I_{ax} is the imaginary component of the line A current also expressed as Im I_a.
If one follows the function over a period of time, one realizes that I_{ax} will be equal to i_a at the instant when $\sin\omega t = -1$ and $\cos\omega t = 0$.

The instant can be defined using a phasor and a reference will also have to be defined.
Let phase A line-to-neutral voltage V_a be the reference. Using the same domain as the current, one gets

$$v_a = \sqrt{2}\, Re\,[V e^{j\omega t}] = \sqrt{2}\, V\cos\omega t \qquad (2.84)$$

The required instant is therefore defined by

$v_a = 0$ and must be rising or $\frac{dv_a}{dt} > 0$ because this the only instant when $\sin\omega t = -1$ as opposed to a similar moment but when $\sin\omega t = +1$.

Therefore

$$\text{Im } I_a = I_{ax} = \frac{i_a}{\sqrt{2}} \text{ (at the instant } v_a \text{ is zero and rising)}$$

The other line components can be similarly derived

$$\text{Im } I_b = I_{bx} = \frac{i_b}{\sqrt{2}} \text{ (at the instant } v_b \text{ is zero and rising)}$$

$$\text{Im } I_c = I_{cx} = \frac{i_c}{\sqrt{2}} \text{ (at the instant } v_c \text{ is zero and rising)} \qquad (2.85)$$

The expressions giving compensator susceptances in terms of imaginary line currents have already been given in equations 2.76.

This method can be suitable for a compensator system designed with a digital signal microprocessor (DSP).

2.4.3.4 Implementation using a separate positive- and a separate negative sequence network

The compensator can be designed in a split manner, with two delta networks; one dealing with the reactive component of the positive sequence and the other the total negative sequence component.

Equations 2.70 express the symmetrical components of the line currents in terms of line-to-line admittances. When these are substituted into equations 2.75 one gets

$$B_{\gamma ab} = B_{\gamma ab1} + B_{\gamma ab2}$$

$$B_{\gamma bc} = B_{\gamma bc1} + B_{\gamma bc2}$$

$$B_{\gamma ca} = B_{\gamma ca1} + B_{\gamma ca2} \quad (2.86)$$

Susceptances with the "1" subscript form the positive sequence, and the "2" form the negative sequence. But the components of each sequence are equal, therefore the positive sequence network is comprised of

$$B_{\gamma ab1} = B_{\gamma bc1} = B_{\gamma ca1} = -1/3[B_{ab} + B_{bc} + B_{ca}] \quad (2.87)$$

And the negative sequence network

$$B_{\gamma ab2} = 1/\sqrt{3}(G_{ca} - G_{bc}] + 1/3[B_{bc} + B_{ca} - 2B_{ab}]$$

$$B_{\gamma bc2} = 1/\sqrt{3}(G_{ab} - G_{ca}] + 1/3[B_{ca} + B_{ab} - 2B_{bc}]$$

$$B_{\gamma ca2} = 1/\sqrt{3}(G_{bc} - G_{ab}] + 1/3[B_{ab} + B_{bc} - 2B_{ca}] \quad (2.88)$$

2.4.4 A balancing compensator

The concept of this type of compensator as proposed by L. S. Czarnecki [11] is based on measurements and computation of the equivalent susceptance, Be and unbalanced admittance A, as defined earlier in section 2.3.2.

It is based on the assumption that only the fundamental frequency exists, which is the sinusoidal and symmetrical supply fed to a linear load.

The decomposition of the earlier mentioned load current vector, ***i***, therefore gives the active, reactive and unbalance currents whose rms values satisfy

$$\|i\|^2 = \|i_a\|^2 + \|i_q\|^2 + \|i_u\|^2 \quad (2.89)$$

The objective of this compensator is to eliminate the reactive and unbalance current components.

As earlier mentioned Czarnecki has defined the equivalent admittance, Y_e.

$Y_e = G_e + j\,B_e = Y_{rs} + Y_{st} + Y_{tr}$ (Y's are the line-to-line admittances of the load)

In appendix 2 (by M. Malengret) it is shown that

$\underline{A} = -(Y_{st} + aY_{tr} + a^*Y_{rs})$ where $a = \exp(j2\pi/3)$ and a^* is its conjugate) (2.90)

Figure 2.11 next is the proposed structure of the final compensator.

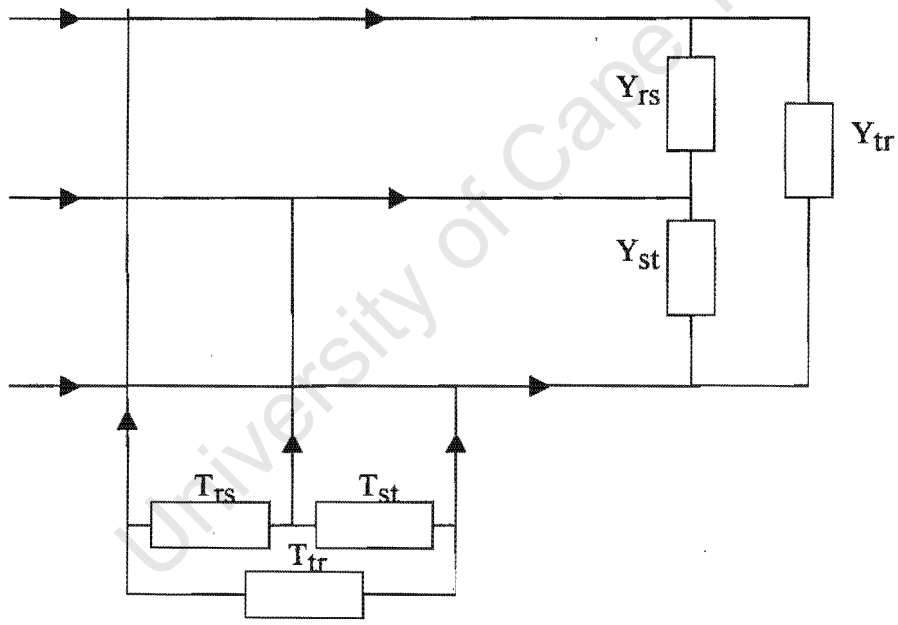

Figure 2.11

Three-phase load with a compensator in place

The values of the compensator branch susceptances given by the following expressions are also derived in Appendix 2.

$$T_{rs} = (\sqrt{3}\,\mathrm{Re}\,A - \mathrm{Im}\,A - B_e)/3$$

$$Tst = (2\,\mathrm{Im}\,A + Be)/3$$

$$T_{tr} = -(\sqrt{3}\,\mathrm{Re}\,A + \mathrm{Im}\,A + B_e)/3 \qquad (2.91)$$

The given definition for the equivalent admittance assumes that the loads are accessible, which is not possible in practice.

Let the line currents be I_r, I_s and I_t. It follows that the line-to-line load currents satisfy the following expressions

$$I_r = I_{rs} - I_{tr} = Y_{rs}V_{rs} - Y_{tr}V_{tr}$$

$$I_s = I_{st} - I_{rs} = Y_{st}V_{st} - Y_{rs}V_{rs}$$

$$I_t = I_{tr} - I_{st} = Y_{tr}V_{tr} - Y_{st}V_{st} \qquad (2.92)$$

(Where V_{rs}, V_{st} and Vtr are the load lie-to-line voltages.)
If a delta load is assumed then the sum of the line currents is zero. This makes the above equations interdependent.
Therefore one could choose any value for one of the load admittances.

If for example Y_{rs} is let to be zero, then it can be shown [10] that

$$Y_{rt} = I_r/V_{rt} \quad \text{and} \quad Y_{st} = I_s/V_{st} \qquad (2.93)$$

Load admittance values obtained this way are referred to by Czarnecki as fictitious values. Using these the expressions for the unbalance admittance and equivalent susceptance simplify to

$$Be = Im(Y_{st} + Y_{rt}) \tag{2.94}$$

$$A = -(Y_{st} + aY_{rt}) \tag{2.95}$$

From these it follows that with only two line currents and two line-to-line voltages Czarnecki's proposed compensator should correct both load unbalance and power factor.

A complete design procedure and simulations are covered in Chapter 3.

2.4.5 The p-q theory of Instantaneous power compensation

Hirofumi Akagi and others [17] proposed a totally novel technique in reactive power compensation, in their paper, "Instantaneous reactive power compensators comprising switching devices without energy storage components". They based their approach on a principle of instantaneous values of power in three-phase systems and generalized their solution for both transient and steady state conditions as well as for arbitrary voltage and current

waveforms. Moreover, the instantaneous active filter that is involved is said to require practically no energy storage components.

Akagi et al, used the p-q theory, a Clarke transformation. It involves an algebraic transformation of the three-phase voltages and currents in the a-b-c coordinates to α and β coordinates. This is followed by the computation of the instantaneous p and q (real and imaginary) power components.

Initially the procedure follows the basic norms of space vector conversion of three-phase parameters, using instantaneous values of line currents and line-to-neutral voltages. The resultant space vector is expressed in its imaginary and real components but in magnitude only; the j's get discarded until the "imaginary" reactive component is finally defined.

$$I = i_\alpha + i_\beta = i_a + a i_b + a^2 i_c \tag{2.96}$$

$$E = e_\alpha + e_\beta = e_a + a e_b + a^2 e_c \tag{2.97}$$

The subscripts α and β denote what should have ordinarily been the real and imaginary components of the instantaneous current and voltage space vectors, while a, b, c are the three-phase instantaneous parameters of current and voltage.

In matrix form

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & 1/2 & -1/2 \\ 0 & \sqrt{3/4} & -\sqrt{3/4} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.98}$$

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \begin{bmatrix} 1 & 1/2 & -1/2 \\ 0 & \sqrt{3/4} & -\sqrt{3/4} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2.99}$$

Using the current and voltage space vector magnitudes, Akagi et al defined the instantaneous real power, *p*, as,

$$p = e_\alpha . i_\alpha + e_\beta . i_\beta \quad (2.100)$$

which, in original three-phase convention, is,

$$p = i_a . e_a + i_b . e_b + i_c . e_c \quad (2.101)$$

Power is known to be is a scalar, but for the case of instantaneous reactive power, q, Akagi et al defined it as a vector and only left the real power as a scalar. q is the sum of the cross products of the instantaneous imaginary and real components of the current and voltage space vector magnitudes obtained above.

$$q = (e_\beta \times i_\alpha) + (e_\alpha \times i_\beta) \quad (2.102)$$

Being a cross product the resultant vectors are on an axis perpendicular to the α and β plane in the direction of the right hand screw rule. They called this axis the "imaginary" axis. The α and β plane is referred to as the "real plane".

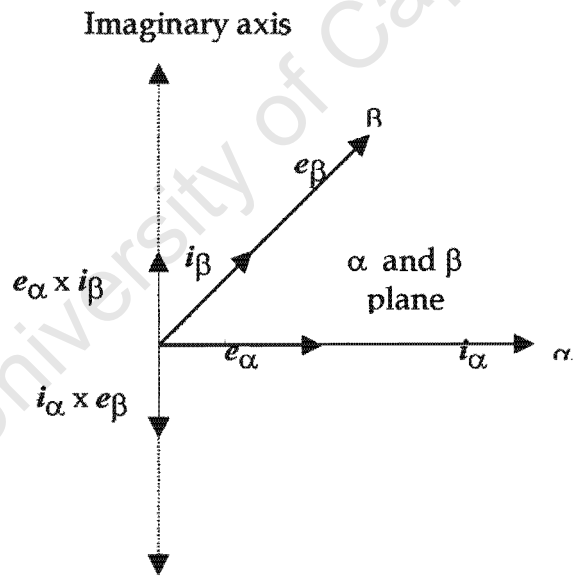

Figure 2.12

p is the value of the instantaneous real power comprising p_1 the mean value of the instantaneous real power (which is the only desirable component) and p_2 the alternative value of the instantaneous real component. The other undesirable

component is q, the instantaneous imaginary power, $(=3 \cdot V \cdot I_1 \sin\theta)$ where θ is the power factor angle.

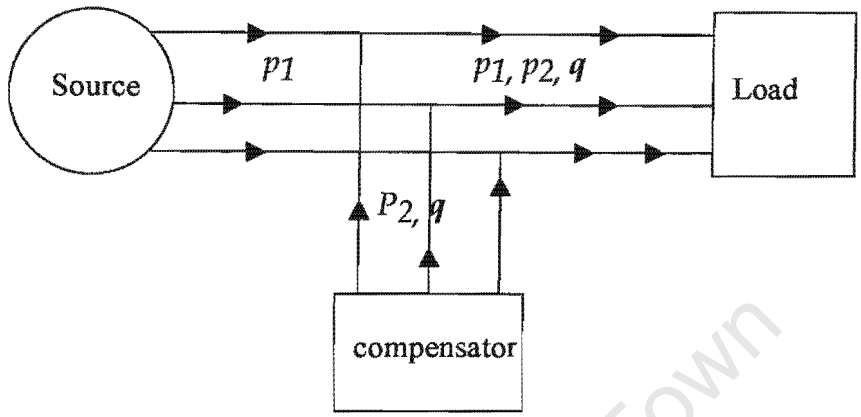

Figure 2.13

Once the components of the system have been identified an active filter is designed to take care of the undesirable components, q and p_2. Meanwhile the power source is left to supply only the mean value of the instantaneous real power.

This is a promising futuristic technique in load compensation. It is said to have the following attributes

- It is applicable to any three-phase system, whether three or four wire. In the case of a four-wire configuration, however, the conversion from three-to-two coordinates must include the zero sequence component, in which case it will be a four-to-three coordinate transformation.
- Being based on instantaneous values the dynamic response is excellent.
- Like most vector operations the signal calculations are brief and easy to translate into standard digital signal processor functions.

It permits two control strategies namely instantaneous power and sinusoidal current. Perhaps more will be discovered as its use increases.

Figure 2.13 represents what happens in principle. However in practice the load must receive the compensating signals translated back into the three-coordinate system.

Further improvements on the approach have been published by Fang Zheng Peng and others [15]. Recently, Joao Afonso and others [23] of Minho University in Portugal published a report with results of successful simulations using a model with additional improvements.

2.4.6 Compensation by phase transformation

2.4.6.1 Background

Problems associated with very heavy single-phase loads are well documented. Such loads are arc furnaces and traction drives for trains. There are instances in the past when supply utilities are reported to have resorted to expensive dedicated single-phase generators away from the grid.

Engineers have therefore had reason to try and design a transformer that could receive a three-phase input and give a single-phase output, while maintaining primary current balance.

Many configurations have been designed with varying degrees of success as will be reviewed ahead.

2.4.6.2 Open Delta for three-to-single-phase conversion

Figure 2.14 is the open delta transformer configuration. Two identical transformers have their primaries connected to a three-phase supply and their secondary windings are connected in series.

In a simulation of this configuration, with a single-phase load connected across a and c, there was no current flow in line B. Since the aim of the exercise was to attain load balance, the design failed. A single transformer connected between phases A and C would achieve the same results at 50% the cost.

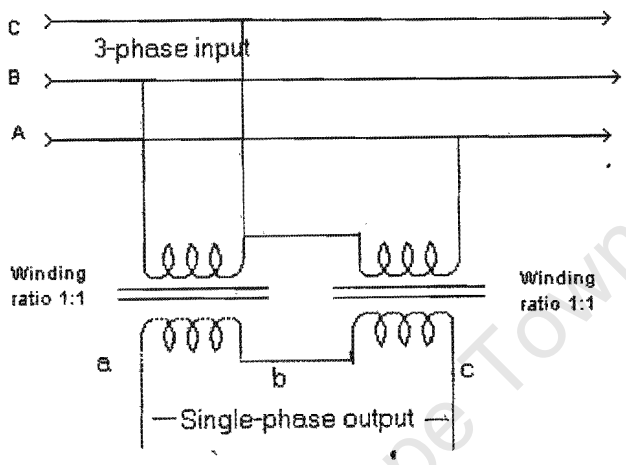

Figure 2.14

Open delta connection

2.4.6.3 The Scott-connection

This is a more ingenuous concept.

A phasor diagram is drawn in figure 2.15 to illustrate the function. In the figure is a symmetrical incoming three-phase supply, with lines, A, B and C, represented by an equilateral triangle. There are two identical transformers. Transformer A has its primary connected between lines B and C and this winding is called the main.

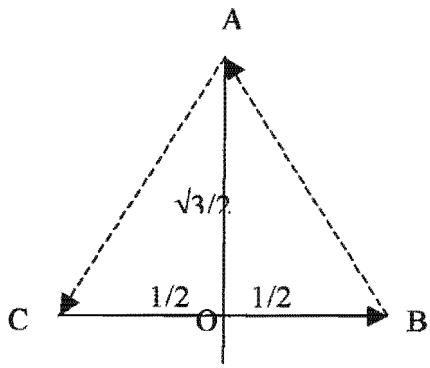

Figure 2.15
A Scott-connection phasor diagram. Phasor CB is called the main and AO is the teaser

The primary winding of transformer B is called the teaser. It has one end connected to phasor A and a length equal to $\sqrt{3}/2$ of its winding is connected in the middle of the primary winding of transformer A. This way the teaser is set up to be 90° from phasor CB, just as shown in figure 2.15. Figure 2.16 is a schematic illustration.

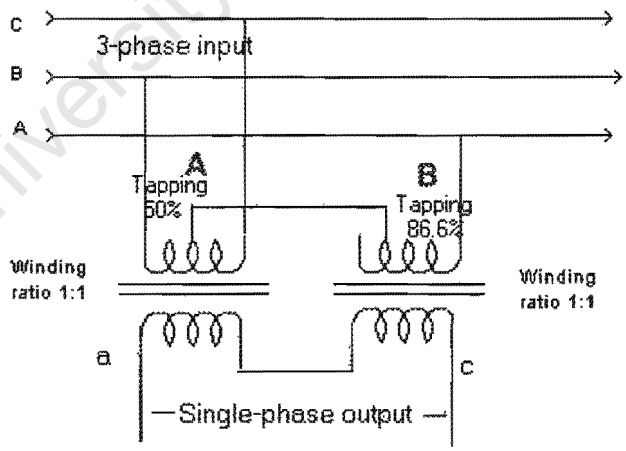

Figure 2.16
Scott-connected transformer

Once the primary input of transformer B is at right angles to that of A, the respective outputs on the secondary side will be similarly at 90° from each other.

So if the secondary outputs are connected in series the resulting phasor will be at 45° from either of them as illustrated in figure 2.17.

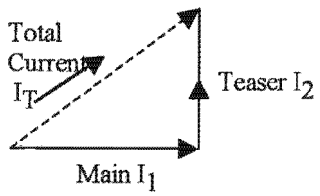

Figure 2.17

This time all the three primary lines will have currents.
However, the question is whether they are balanced or not.

Let the transformer turns ratio be 1:1 and if the supply line-to-line voltages are 100volts then the magnitude of each of the secondary outputs will be 100volts. However since they are 90° apart, their sum is going to be $\sqrt{2}$ times one of them. In this case, the single-phase output will be 141.4 volts. Let the single-phase load be 10 amps.

It should be recalled that the teaser is connected at $\sqrt{3}/2$ of the winding length. This means that being shorter it carries more amps to make the same ampere-turns as the secondary. So the primary teaser current, I_3 is

$I_3 = 10 / (\sqrt{3}/2) = 11.5$ amps.

This is equal to the difference between the currents in the two halves of the main transformer A. But the total ampere-turns in both primary and secondary windings of A have to be equal. Let the current in one half of the main be I_1 and the current in the other half be I_2, then all the above statements can be put into equations

$\frac{1}{2} I_1 + \frac{1}{2} I_2 = 10$ amp

$I_1 - I_2 = I_3 = 11.5$ amps

Solving the two simultaneous equations

$I_1 = 15.75$ amps and $I_2 = 4.25$ amps

The transformer ratings will be 10amp x 100 volt = 1000 volt amperes each, giving a total of 2kva. The power delivered to the load is 10amps x 141.4 = 1414 va.

Therefore this configuration will not only be costly but have serious line current imbalances as well.

On the other hand, if the two outputs are separated and fed to two separate single-phase loads of 10 amps each, the secondary will a capacity of

2 x 10 amp x 100volts = 2kva.

But

The secondary ampere-turns for transformer A (the main) are not equal to the ampere-turns in its primary. This because the primary has two halves each carrying currents that differ in phase from the other as well as from the secondary.

So in the primary of A there are two current components; those that are in phase with its secondary currents (which will just balance the secondary ampere-turns) and those that are at right angles to the secondary current in one half balancing out similar ones in the second half.

Despite the above anomalies, it has been shown [21, 22] that the supply line currents can balance and that the required transformer can be as low as 108% of the required full load.

A few other designs of three-to-two-phase transformation like, the Taylor, the Le Blanc and the Fortescue have been proposed but the Scott-connected three-to-two output transformer has found more wide spread commercial use, even when

it's known, for example, that the Le Blanc is more compact and cheaper to produce.

Consumers include arc furnaces and traction loads like the railways.

Obviously there is, still, room for improvement as 100% balance can never be guaranteed for two separately operated loads even under the most carefully designed distribution matching. In addition the primary current relativephase angles are not 120°.

2.4.6.4 Scalene Scott-connected transformer with SFC, (single-phase feeding power conditioner)

The set backs related to the Scott—connection have been discussed in section 2.4.6.3. Despite all that has been said it offers the best hope to-date of the ultimate three-to-single-phase conversion transformer.

Tetsuo Uzuka and others [20], of the Railway Research Institute, Kokubunji city in Japan, recently published a paper with a more promising proposal in an attempt to solve the three-to-single-phase transformer problem, using the scott transformer.

They proposed the "SFC: single phase power conditioner." The basic configuration is comprised of a Scalene Scott-connected transformer and two self commutated inverters.

Figure 2.18a and 2.18b illustrates the schematic difference between a train system running on the regular two separate single–phase Scott circuits and the new scalene Scott single-phase circuit.

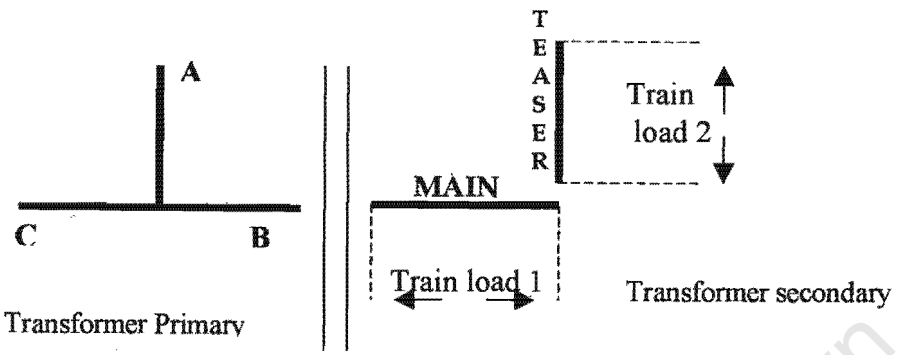

Figure 2.18a- A normal Scott-connection with two separate output circuits

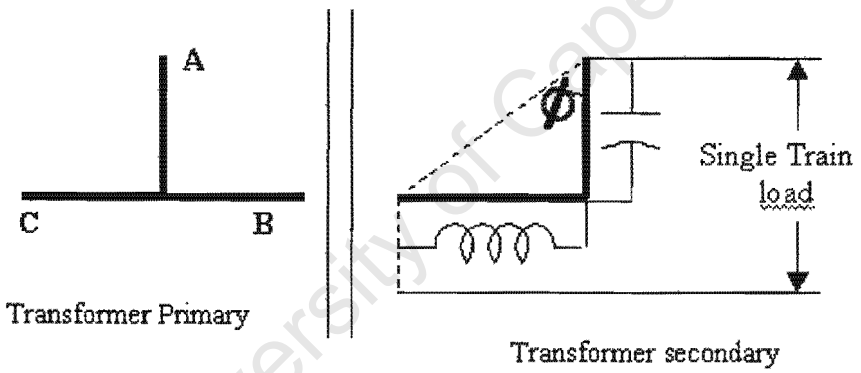

Figure 2.18b

The new Scalene Scott-configuration for three-phase-to-single-phase (with a single output circuit)

The secondary windings are connected in series and so the single-phase is supplied at 45°, lagging the teaser as explained earlier. (This was for a prototype load with unity power factor).

The two inverters are controlled by a PWM (pulse width modulation) method that enables them handle active power while at the same time compensating for the reactive power for each secondary and in the process maintaining primary

voltage symmetry and current balance. In addition, according to the report, the rated capacity of the SFC was close to that of the load itself, making it very efficient. So far this design has performed successfully under laboratory conditions.

2.4.7 Cycloconvertor-controlled synchronous machines for load compensation

P. T. Finlayson and D. C. Washburn [19], point out that loads with massive current fluctuations often cause fluctuations in supply voltages, upsetting system dynamic balance. In certain cases where the current swing is a sizable percentage of the load it may become impossible to accommodate the load unless appropriate compensation is installed.

These authors point out the most frequent cause of voltage fluctuations is the varying reactance drops in the supply impedance. However the load swings referred to in this context are real power and as such require real energy storage for stability to be restored. They suggest a cycloconvertor as the solution.

A cycloconverter is a controlled wound rotor machine. The machine is coupled to a large flywheel whose inertia can be used to provide the necessary compensation power. This method is different from the method of using synchronous machines for reactive power compensation and is the only method in this review that requires real power for load compensation.

In order to design the right capacity of the compensator one must have a good idea of the extent of the expected load swings. This is both in terms of peaks and troughs. While designing for the worst scenario is the goal, it is recommended that the control equipment should not to respond to load changes that are

deemed small enough for the mains supply utility to absorb. This is important for optimizing design costs.

A good design is one where the average energy supplied and/or absorbed by the compensator is almost nil. This is especially difficult for loads with virtually no periodicity or the so-called "almost periodic loads."

First the system behavior to pre-selected loads without any compensation in place is observed. This permits load demand curves to be plotted. An appropriate operating control point is located such that the total areas below and above the operating point are almost equal. The areas represent energy.

The equipment is comprised of a wound rotor machine with a massive flywheel (typically 100 ton). The rotor is in star configuration with a neutral (connected to a fourth slip ring). The stator has heavy electrical surge protection connected right at the machine terminals.

The cycloconverter is a static frequency changer, converting power system voltages to voltages at a lower frequency. Its frequency is variable and is a function of the control inputs. The complete circuit is a star-connection of three individual circuits, each forming a single-phase cycloconvertor.

Figure 2.19 illustrates the basic principle of the compensator. The control system, including current sensor, monitors the state of the load (whether peak or trough)

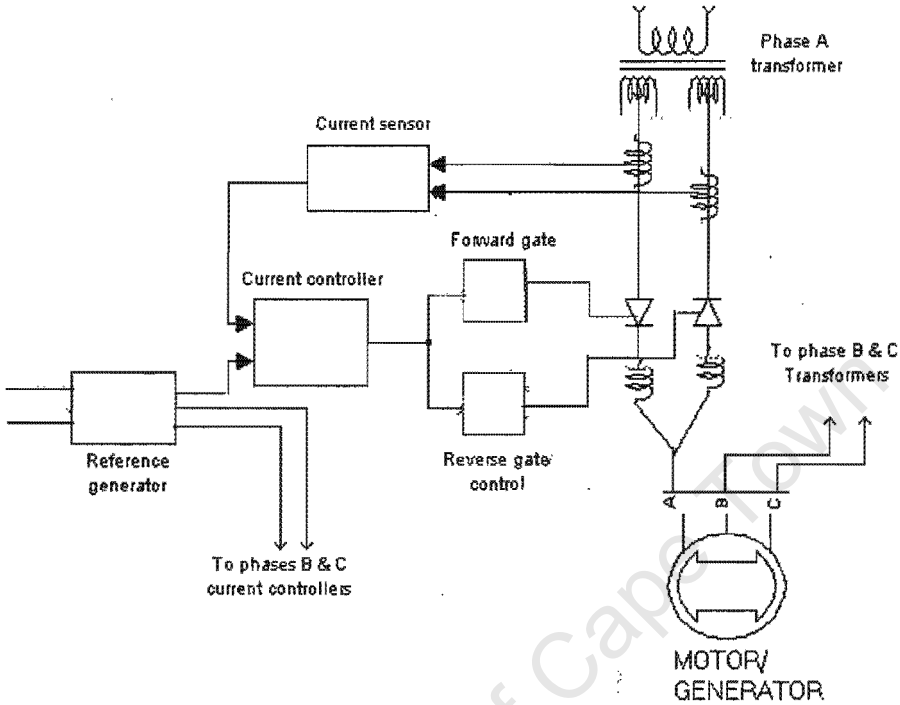

Figure 2.19
Cycloconvertor functional schematic

and enables the appropriate response from the motor. When no response is required both forward and reverse are enabled.

2.4.8 Compensation of the Arc Furnace

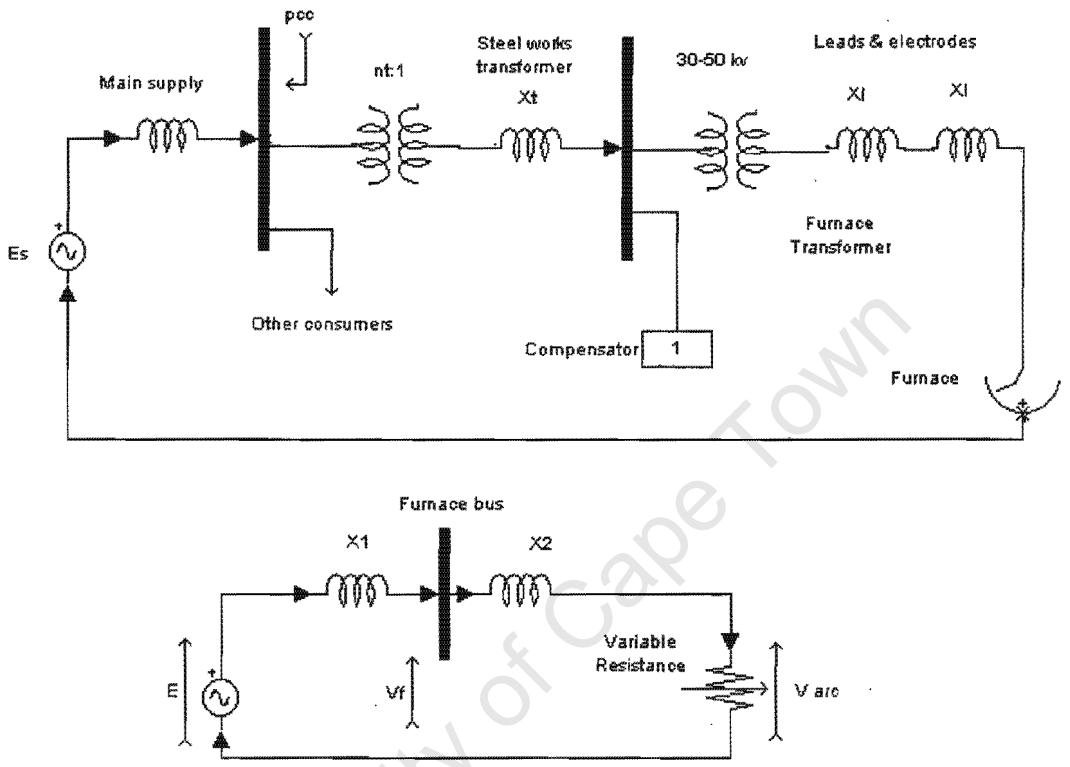

Figure 2.20

This is about the largest type single-phase load (often exceeding 50 Mva) and with some of the least predictable load parameters. Nonetheless a model must be formed before any load can be compensated. Compensation as usual is two fold; the load unbalance and reactive power compensation.

In section 2.4.6 various methods of phase transformation as a means of load balancing were discussed at length. This is the mode of load balancing that is most frequently used in single-phase arc furnaces. So at this point nothing further will be discussed on the issue of load balancing.

The issue that at this stage is power factor correction. Harmonic filtering will not be discussed.

In order to develop a model that has close semblance to reality the reader is referred to figure 2.20. It comprises two parts. The top part describes the physical items that constitute the plant network. This is followed by an equivalent circuit that approximates the dynamic operating characteristics of the furnace network.

As has earlier been mentioned, consumption of vars creates voltage dips. Voltage has up till now not been used, by this author, as an index for load compensator performance. However the nature of this load is such that its effect on voltage cannot be ignored. So the quality of reactive power management on the consumer side is best monitored by keeping the spotlight on the voltage.

Looking at figure 2.20, the arc is represented as a variable resistance. This is the dominant part of the total load resistance. All the others are comparatively negligible. The transformers, the cabling and electrodes constitute the reactive component, X, of the circuit. All reactances are referred to the secondary side of the furnace transformer.

The power delivered to the arc will vary but have a maximum value, P, given by

$$P = E^2/2X \text{ per phase} \qquad (2.103)$$

X is the total circuit reactance and the primary line currents will be assumed balanced for convenience.

The value of R_{pmax} at the maximum power condition will be equal to the equivalent source impedance, X (according to the law of maximum power transfer).

The current at the same time will be, I_{pmax} and given by

$$I_{pmax} = E/\sqrt{2}X \quad (2.104)$$

(because the total circuit impedance is $R_{pmax} + jX$, and $\| R_{pmax} \| = \|X\|$)

The voltage drop across the arc (which will also be equal to that across X), will be

$$X\, I_{pmax} = E/\sqrt{2} \quad (2.105)$$

It is a known fact that maximum arc stability is achieved at the maximum power point. Lower currents are known to give a higher power factor but at the expense of stability and melting capacity. Higher currents simply worsen the power factor and hence efficiency.

This makes it appear as though the best choice is to close in on the maximum power point. Unfortunately the refractory sidewall seems to wear very rapidly at this same point. So this becomes another issue to consider.

Refractory wear is approximately proportional to the arc length for a given power level. The arc length, in turn, is almost exclusively proportional to the voltage as opposed to current.

From above

V_{arc}(at maximum power) = $E/\sqrt{2}$ and $P = (E^2)/2X$

So

$$V_{arc} = \sqrt{(P_{max}X)} \quad (2.106)$$

Therefore for a given maximum arc length, (indicating maximum voltage), and a desired maximum arc power, the circuit reactance, X, must not exceed $V^2_{arc(max)}/P_{max}$, otherwise the operating current will have to be increased if the arc length is to be kept in check to avoid increased refractory wall corrosion.

It can be concluded from above that the most viable solution to ensuring that the desired power input is equal to the maximum power with an acceptably short arc is by **minimizing the system reactance, X.**

This is a job for a compensator.

A key factor of this compensator is rapid response time. This includes, saturated reactors, and a variety of thyristor switched static compensator types. The synchronous condenser also used to be popular before high-speed thyristor-controlled systems were fully developed.

Finally it should be pointed out that in addition to power factor correction there still exists the problem of flicker, but this will be categorized as harmonics and therefore out of scope.

2.4.9 The tapped reactor /saturated reactor compensator

The class of saturated reactor compensators is almost exclusively designed for voltage stabilization for transmission systems and therefore out of the scope of this thesis. However, the tapped reactor, being essentially a single-phase compensator is categorized as a load compensator and often finds use in small arc furnaces. For this reason the principles of operation of a saturated reactor will be briefly reviewed here.

Figure 2.21 (a) represents the controlling coil of a saturable magnetic coil with its ideal magnetization characteristic of flux versus current.

If the current in the winding is sinusoidal then

$V = N\frac{d\phi}{dt}$ ($V$is the voltage across the coil and N is the number of turns)

This relationship is depicted by figures 2.21(b) and 2.21(d). The flux level is

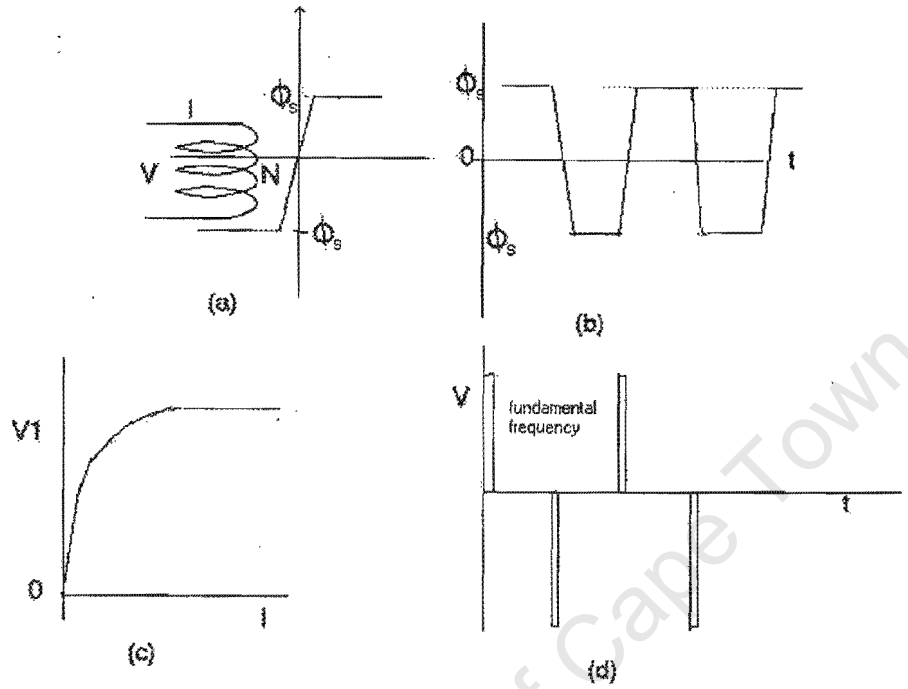

Figure 2.21

almost square and is alternating between $\pm\phi_S$. The voltage is almost a series of pulses but because the flux is virtually independent of the current the fundamental component of the voltage remains constant.

A practical magnetization curve will not be flat but quite linear above the ϕ_S level with a slope that approximates the permeability of free space. The result is similar to the voltage/current characteristic shown in 2.21c with a small positive slope. The constant fundamental voltage property follows directly from the saturation transitions of the core. Each transition induces a fixed voltage impulse independent of the rate of the transition. The fundamental voltage lags the current and vars are generated.

The structure of a tapped reactor is comprised of two of such elements, one a series and the other a shunt.

2.4.10 Synchronous condensers as load compensators

Synchronous condensers played a vital role in the history of compensation, both as transmission and load compensators. The emergency of thryristors largely contributed to their relegation and near demise. A few facts about them will nonetheless be appended here.

If a synchronous motor is properly synchronized to the supply, and carrying no load and has negligible loss, it will have a very small stator current. Its minimum armature current corresponds to near unity power factor. By increasing the field current the synchronous motor is made to supply leading vars and thus used to compensate inductive loads. By the same token, it is capable of absorbing the same vars when the field current is decreased. These two actions are referred to as over-excitation and under-excitation respectively. This motor is also capable of handling a wide range of loads. It has the ability to respond to rapid load changes. These attributes give it flexibility and an edge over other traditional alternatives.

Its shortcomings include the considerable high losses as compared to static var compensators, thus the power factor is never zero. It also has a tendency to run automatically over excited at times of high loads and under excited when the system being compensated gets under loaded. This latter problem, however, is more evident in cases of transmission line voltage stabilization.

2.5 Summary

A wide range of compensator designs and methods has been reviewed. It can be concluded that to design a load compensator one requires an accurate description of the load. More importantly, the model should use practically accessible measurements.

In this regard a method like that of symmetrical components is quite explicit. First, one eliminates the negative sequence components and then tackles the reactive content of the positive sequence. This is done by simply connecting in parallel to the load, a reactive network whose positive and negative sequence current components are equal but opposite to the undesirable ones of the load.

Gyugyi et al [7] work from the basis that the ideal negative sequence current generator is the single-phase load. So each individual load branch is handled separately. This is equally explicit.

That is why this author finds the approach by Czanecki [11] quite intriguing. He seems to ignore such established norm.

3. Computer simulations

This chapter covers computer simulations. Toolbox symbols and their functions are described in appendix 1.

3.1 Indices of compliance

An ideal load is purely resistive and balanced. It has unity power factor and zero unbalance current. Its parameters are the benchmark. To begin with a simulation of such a load, fed with a symmetrical and sinusoidal three-phase supply voltage, is done and currents are analysed for record. Then when compensating another random load, the performance of the compensator is judged against this benchmark.

In section 2.2 as well as in [13], the space vector was introduced as a real time (instant by instant) three-phase analysis tool for asymmetry. Specifically for this context, the system current space vector, **I**, is used to analyse system currents for unbalance. Additionally the system voltage space vector, **V**, can be used as a reference, for **I**, to analyse the system power factor as will be shown.

Let I_a, I_b, I_c be the line currents of a three-phase system in positive sequence.

Then the current space vector is given by

$\mathbf{I} = I_a + \mathbf{a}I_b + \mathbf{a}^2I_c$ (from equation (2.1))

$= I_a + 1/2(-1+j\sqrt{3})I_b - 1/2(1+j\sqrt{3})I_c$

$$\text{Re } \mathbf{I} = I_a - 1/2(I_b + I_c) \tag{3.1}$$

$$\text{Im } \mathbf{I} = \sqrt{3}/2(I_b - I_c) \tag{3.2}$$

For analysis, Re **I** is plotted against Im **I** using the following process.

As the line current measurements are taken, in real time, the Re I component is extracted as follows. See figure 3.1. A measurement of line A current, I_a, is

fed to an amplifier with unity gain. Meanwhile measurements of currents I_b and I_c are also separately taken and fed to amplifiers with gains of -1/2. When the three output components are summed up they constitute the real component of the system current space vector. Likewise, from equation 3.2, the imaginary component, Im I, is derived when a measurement of line B current, I_b, is amplified by a factor of $\sqrt{3}/2$ while that of line C, I_c, is amplified by $-\sqrt{3}/2$. Then the two are summed up together.

In figure 3.1 a symmetrical and sinusoidal three-phase voltage supply is connected to a balanced resistive delta load.

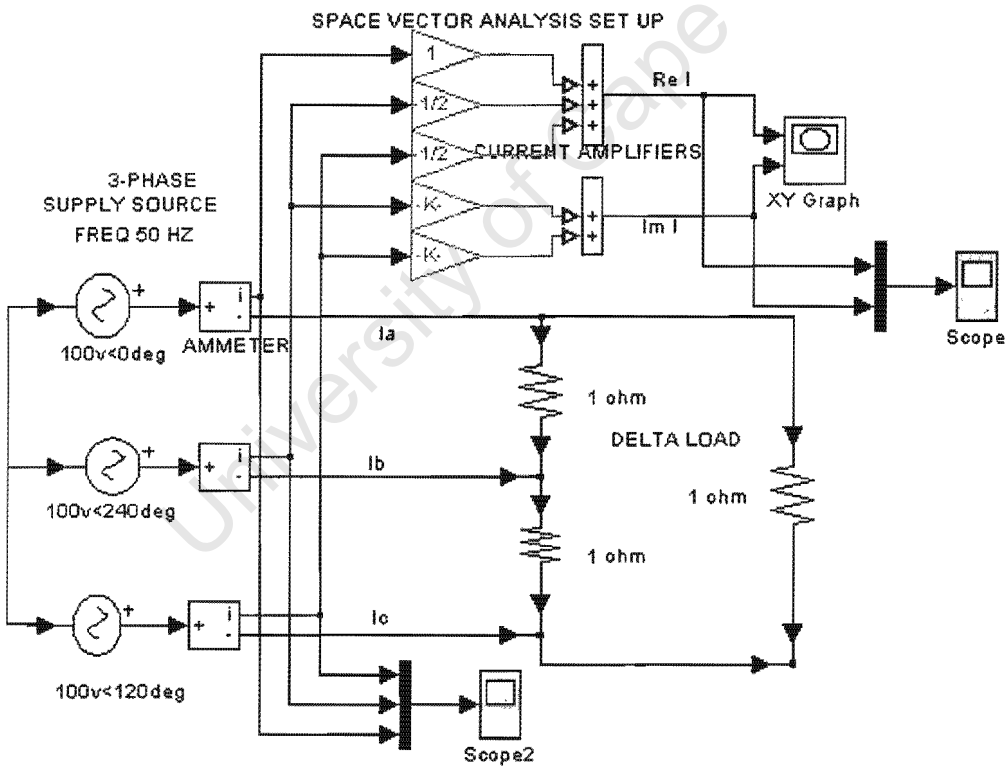

Figure 3.1
An ideal load

The following is the system analysis, in the form of illustrations, for the ideal load in figure 3.1.

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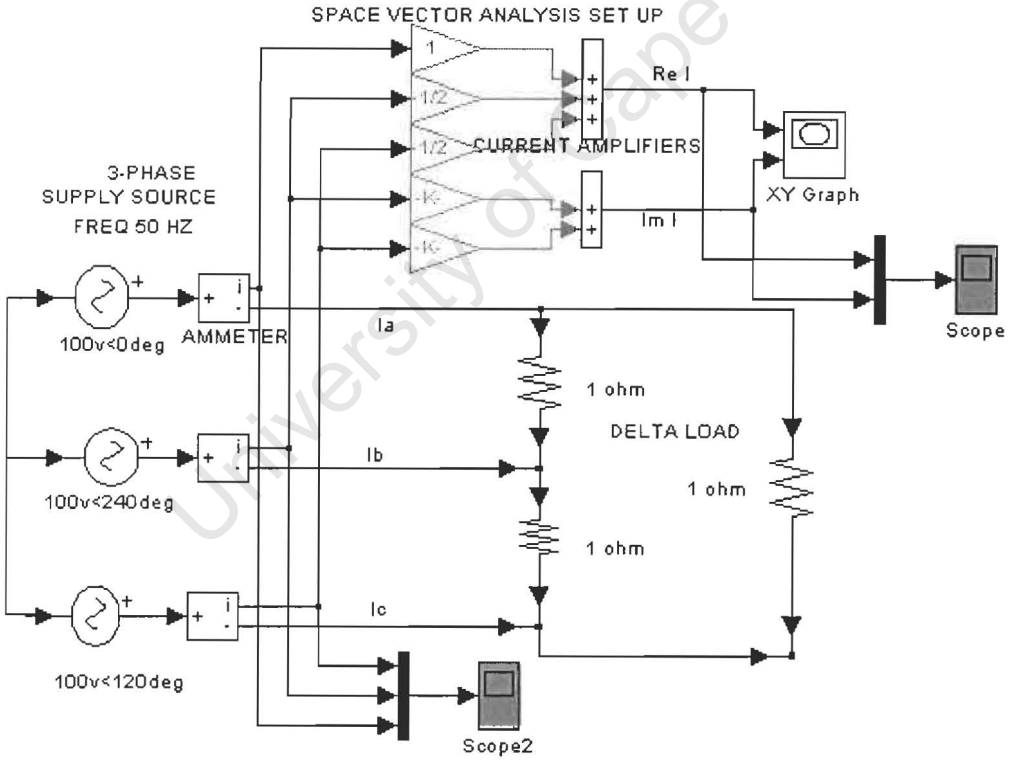

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An ideal load

The following is the system analysis, in the form of illustrations, for the ideal load in figure 3.1.

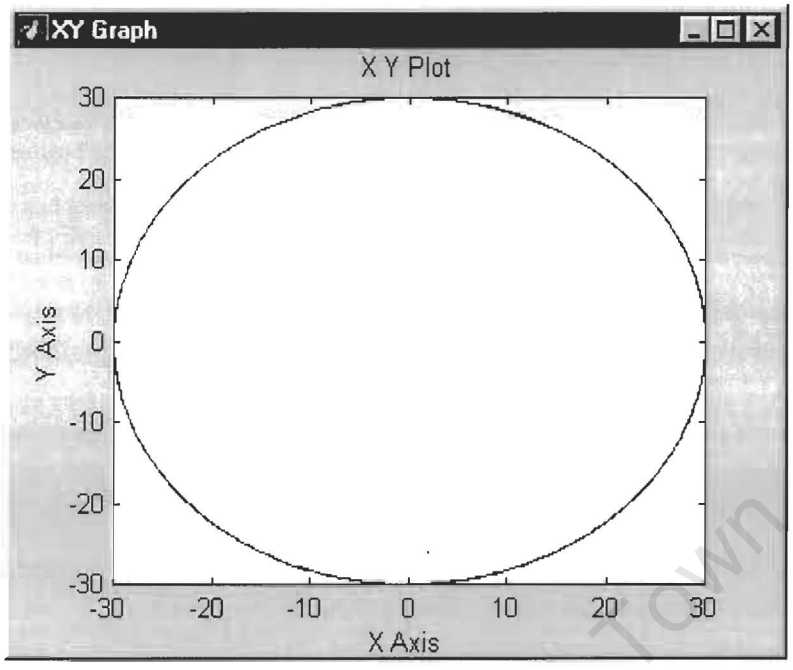


Figure 3.2
This is typically the XY plot of Re I against Im I for a perfectly balanced load

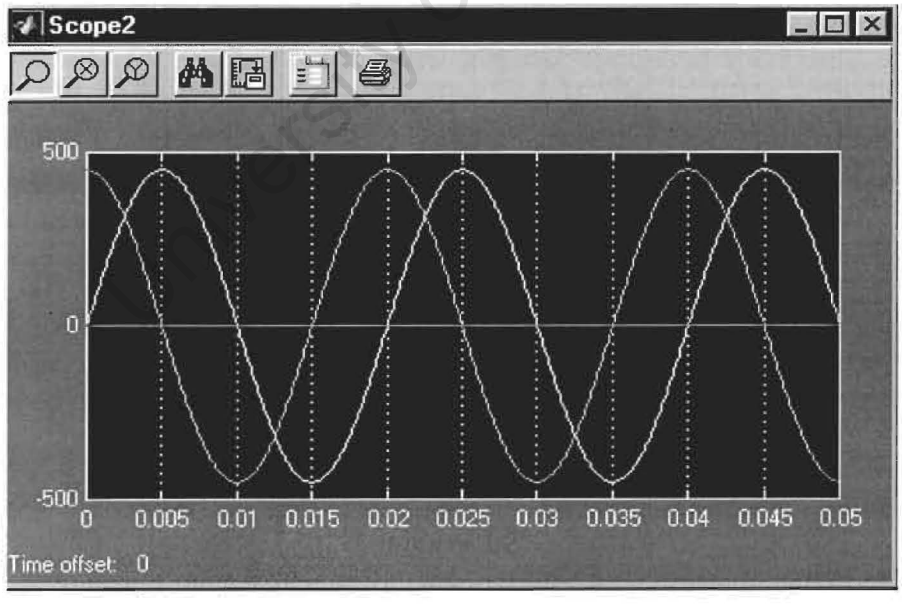


Figure 3.3
The scope output of Re I and Im I, is two sinusoidal waveforms of equal amplitude and 90° apart

The choice of a balanced resistive load was to ensure both load balance and unity power factor at the onset. It is worth pointing out at this stage (as was observed) that the XY graph will be a perfect circle even for a balanced inductive load, (when the power factor is not unity). In this case a distinction can be made using a reference voltage.

Three line currents together with the reference voltage are displayed on the scope. See figure 3.4. In the displays line A current waveform is in phase with the reference voltage in the case of a resistive load and lags by 90° in the case of an inductive load.

Figures 3.5 and 3.6 illustrate a solution the same problem by superposition of the system current and voltage space vector loci.

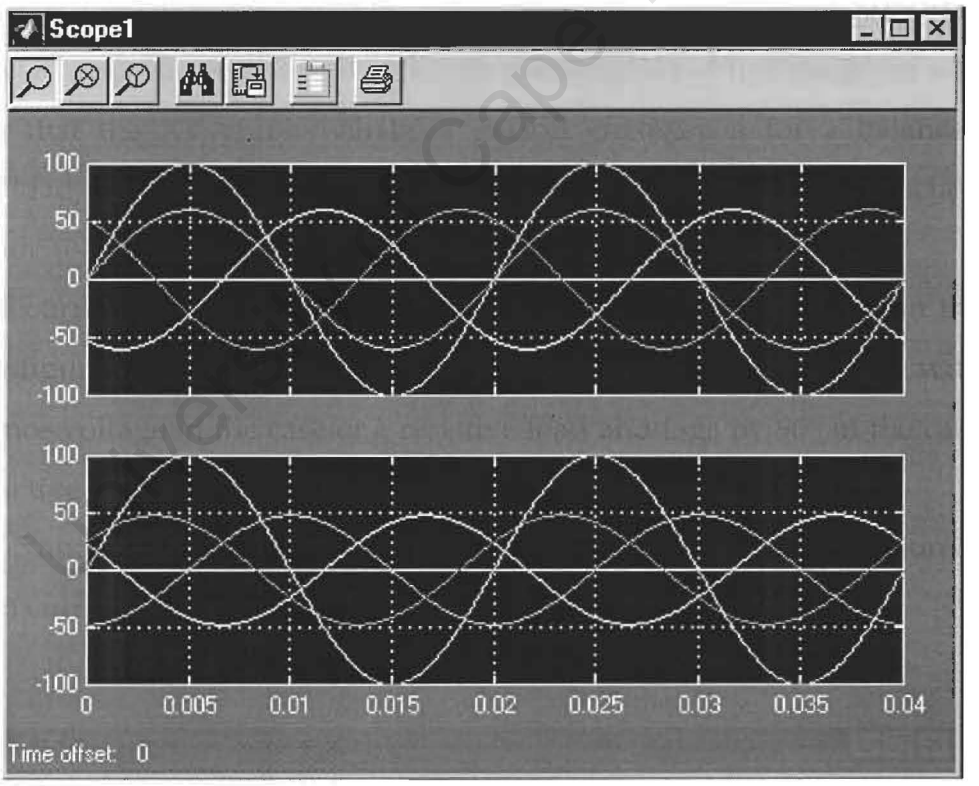


Figure 3.4

Figure 3.4 is a display of two sets of line currents. The top set is to a purely resistive delta load, while the bottom one is to a purely inductive load. Both displays have a reference line-to-neutral 100 volt.

In space vector format

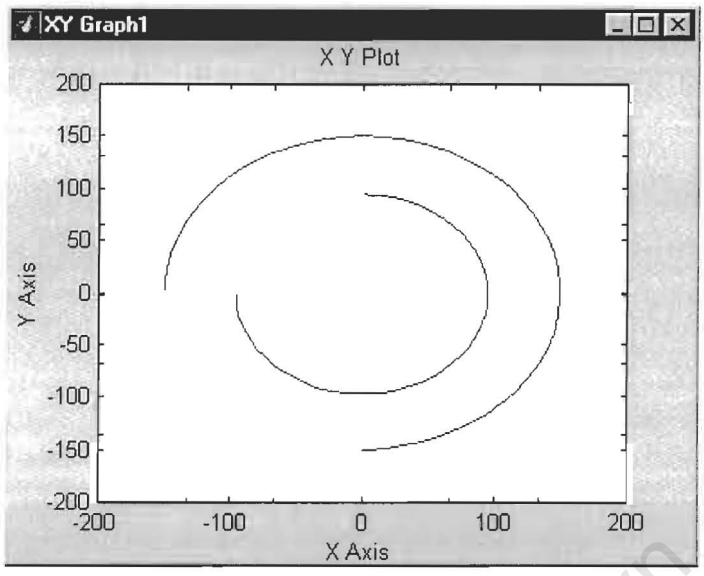


Figure 3.5
These loci represent the system voltage space vector (outer) superposed over the system current space vector for a ***purely inductive*** *balanced load. They are anticlockwise bound and the current is lagging by 90 °.*

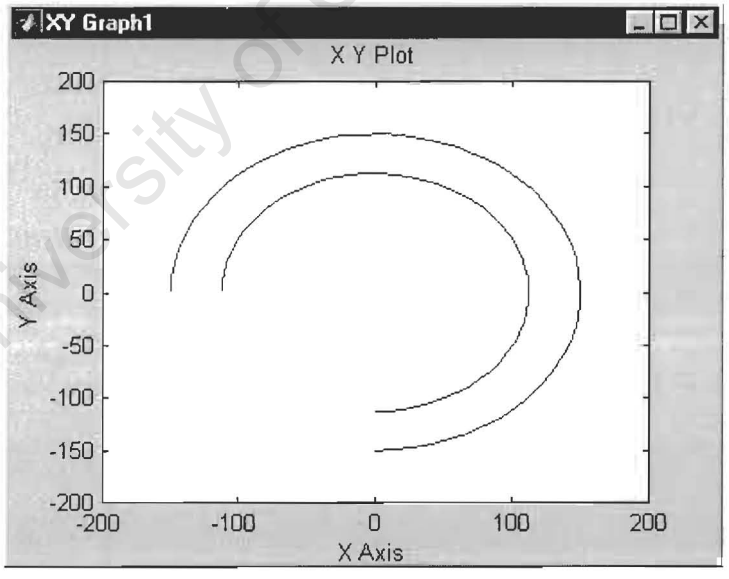


Figure 3.6
This a representation of the system voltage space vector (outer) superposed over system current space vector for a balanced ***purely resistive*** *load. They are in phase.*
Figure 3.5 and 3.6 are 15 millisecond simulations at a supply frequency of 50Hz. One cycle is 20 milliseconds.

3.2 Parameters of an unbalanced load

3.2.1 A purely resistive unbalanced load

An unbalanced resistive load is set up. Line current measurements are taken and observations are made. In figure 3.7 the XY plot (of the system current space vector locus) is ovoid as a result of the load unbalance and the amplitudes of Re I and Im I as well as the phase angle between them also change (see figure 3.8).

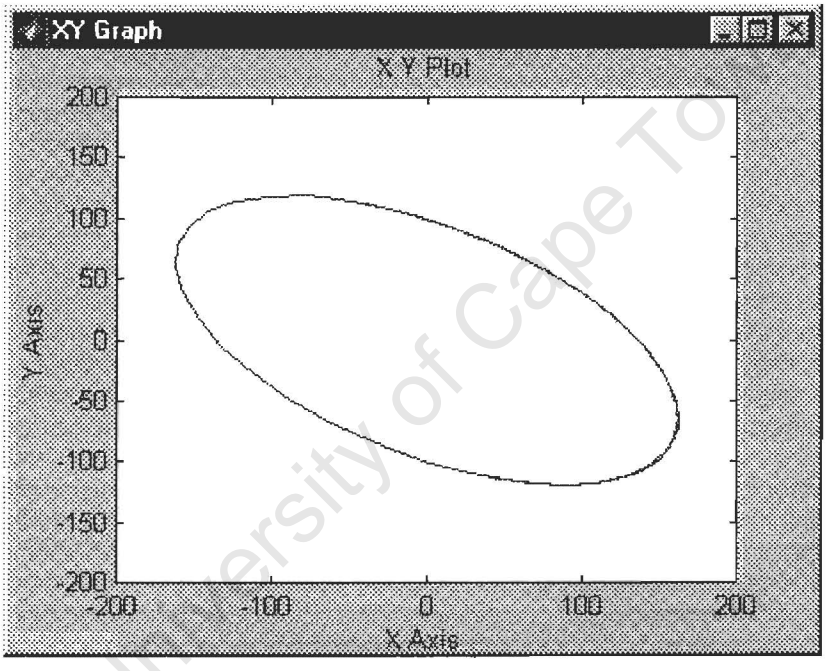


Figure 3.7

This is the output when the load is 5ohm, 5 ohm and 2 ohm.

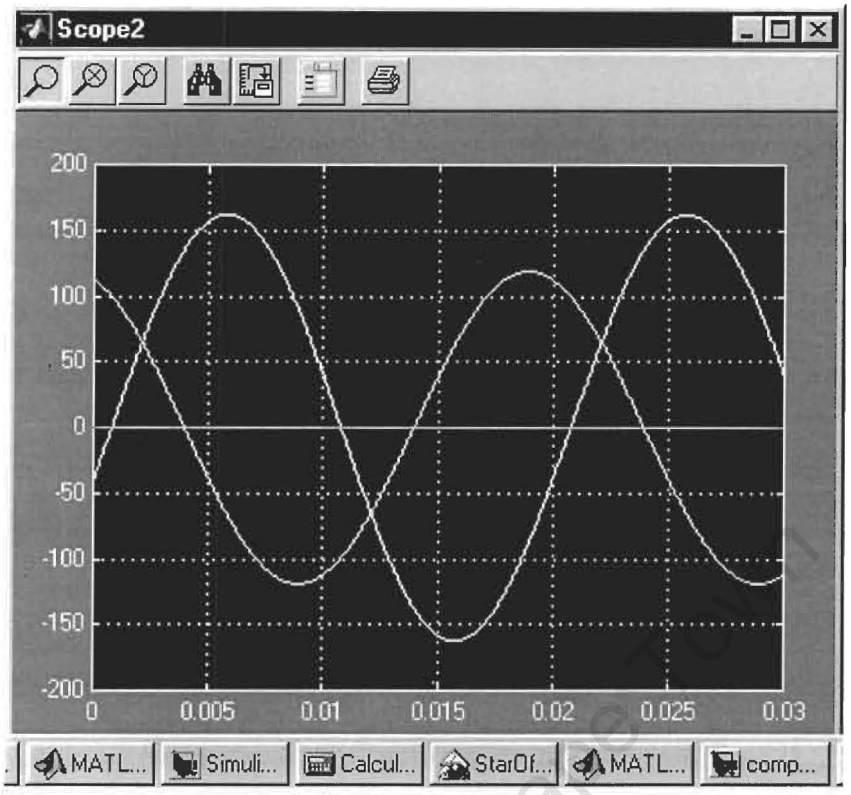


Figure 3.8

This is a scope display of the Re I and Im I waveforms for an unbalanced load

3.2.2 A purely inductive unbalanced load

System analysis of a purely inductive (or purely capacitive) unbalanced load using the current space vector alone will still yield an ellipse. However determination of the reactive content of the load requires comparison with a reference voltage as demonstrated earlier.

3.3 Balancing the load

The next task is to rebalance the system.

3.3.1 Using symmetrical components

The concept of symmetrical components as was presented by C. L. Fortescue [1] was reviewed in section 2.4.3. The action of a compensator when correcting load unbalance is introduced here as the injection of compensator

currents into the system.

As was stated in 2.4.3, any three-phase system of unbalanced currents can be presented as three separate sets of, balanced positive sequence, balanced negative sequence currents and three zero sequence currents of equal magnitude. Let I_a, I_b, I_c be the line currents.

$I_a = I_{a1} + I_{a2} + I_{a0}$ (I_a is phase **a** line current and I_{a1}, I_{a2} and I_{a0} are its positive, negative and zero sequence components)

$I_b = I_{b1} + I_{b2} + I_{b0} = \mathbf{a}^2 I_{a1} + \mathbf{a} I_{a2} + I_{a0}$ (since $I_b = \mathbf{a}^2 I_a$, for positive sequence and $I_b = \mathbf{a} I_a$, for negative sequence. **a** and $\mathbf{a}^2$ are the 120° and 240° operators respectively)

Likewise

$I_c = I_{c1} + I_{c2} + I_{0B} = \mathbf{a} I_{a1} + \mathbf{a}^2 I_{a2} + I_{a0}$

It was shown in section 2.4.3 that

$$\begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \qquad (2.69)$$

Equation 2.69 only works out the reference phasor of each sequence. In a balanced system the zero sequence components are equal to zero, and since the purpose of the exercise is to balance the system currents, only the positive and negative sequence currents are considered.

To balance the system, the compensator injects the negative sequence components into the supply lines. See figure 3.9.

Measurements of the line currents are taken. Then the reference phasor of the

negative sequence is given by

$$I_{a2} = (I_a + a^2 I_b + a I_c)/3 \qquad (3.3)$$

$I_{b2} = aI_{a2}$ and $I_{c2} = a^2 I_{a2}$ (where I_{b2} and I_{c2} are the second and third negative sequence phasors respectively). When these are injected into the respective lines by a compensator, the voltage source will be left to generate only the positive sequence currents and the system will be balanced.

Figure 3.9 illustrates compensating current sources connected to the respective lines. Then the source currents are measured to check for balance.

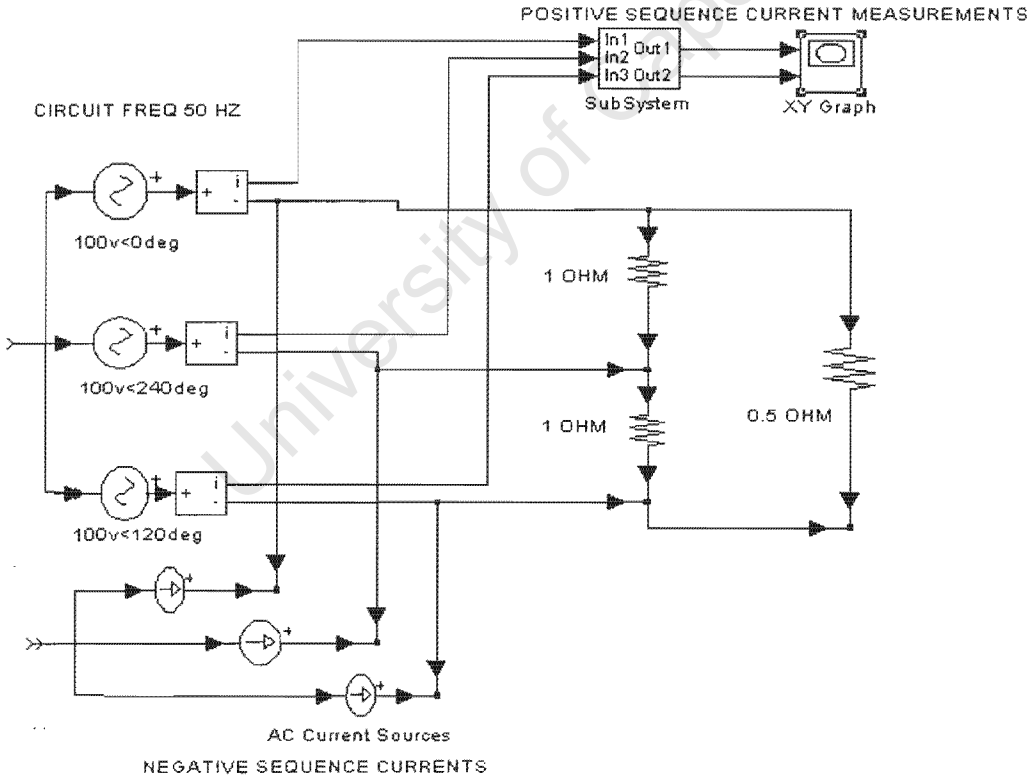


Figure 3.9

Compensation using current sources

Figure 3.9 is a purely resistive load and the negative sequence components are the only undesirable currents present.

In the case of an unbalanced complex load after eliminating of the negative sequence, the power factor problem remains.

3.3.2 Using a balancing compensator

In chapter 2 the concept of a balancing compensator as proposed by Czarnecki [11] was explained. This type of compensator realizes both load balance and power factor correction simultaneously.

From appendix 2 by M. Malengret the required line-to-line compensator susceptances are given by

$$T_{rs} = (\sqrt{3}\ \mathrm{Re}\ A - \mathrm{Im}\ A - B_e)/3 \tag{3.4}$$

$$T_{st} = (2\ \mathrm{Im}\ A - B_e)/3 \tag{3.5}$$

$$T_{tr} = -(\sqrt{3}\ \mathrm{Re}\ A + \mathrm{Im}\ A + B_e)/3 \tag{3.6}$$

T's are the compensating susceptances for the respective branches as indicated by the subscripts, (for example T_{rs} is connected between lines r and s). A, is the unbalance admittance and B_e, the equivalent susceptance.
Section 3.5 of this chapter covers from basics the design of this compensator and simulation techniques.
In this section only a brief reference is made for the purpose of illustrating the concept of load compensation itself.

A complete network, including an admittance measuring instrument is set up. Initially the compensator values are manually calculated, but later an automated computing system is designed. In figure 3.10 the computed compensator susceptances are converted to real component values. The negative values are inductive and the positive ones are capacitive.

Inductance L = $\frac{1}{T100\pi}$ henrys at 50 Hz supply frequency and T is the worked out branch compensator susceptance.

Capacitance = T100π farads at 50 Hz.

These components are then connected across the respective branches and the source currents are analyzed for both balance and power factor.

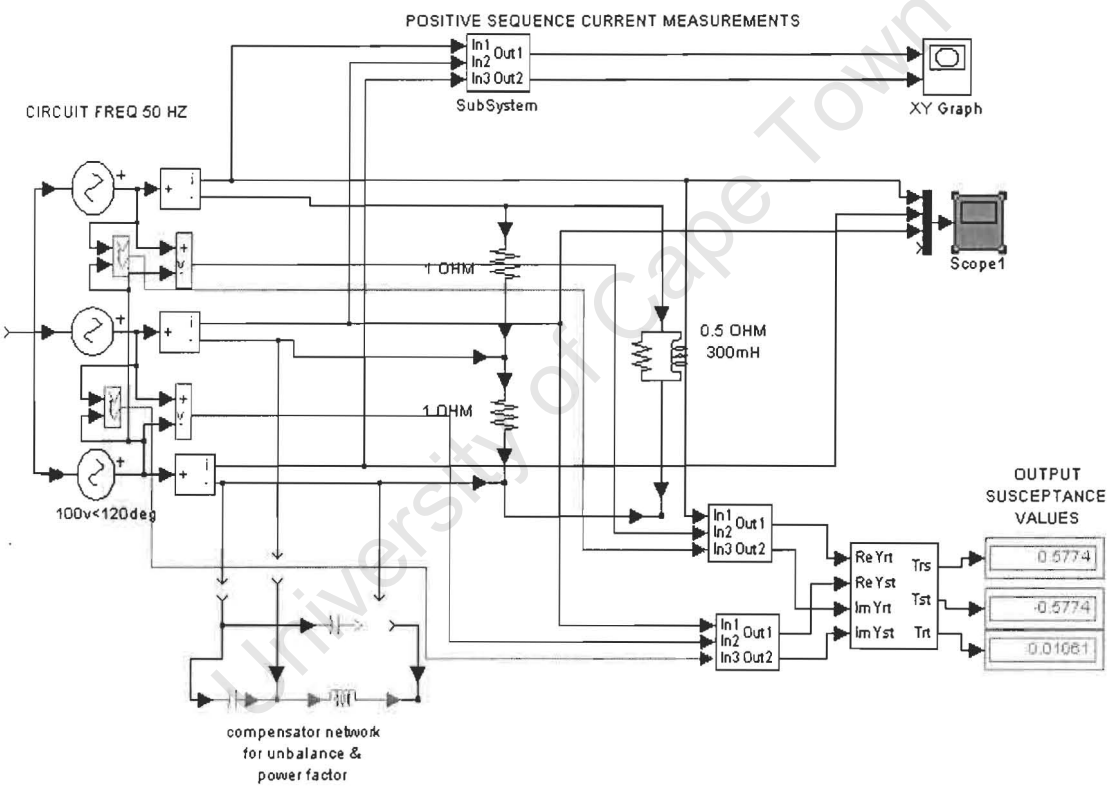


Figure 3.10

Calculation and substitution of compensator elements

3.4 What happens around the circuit during balancing?

In this section a series of illustrations are used to explain how source currents, load currents and compensator currents relate to each other, before, during and after load balancing. In figure 3.11, a resistive delta load is comprised of, two, 1 ohm resistors and a 0.5 ohm.

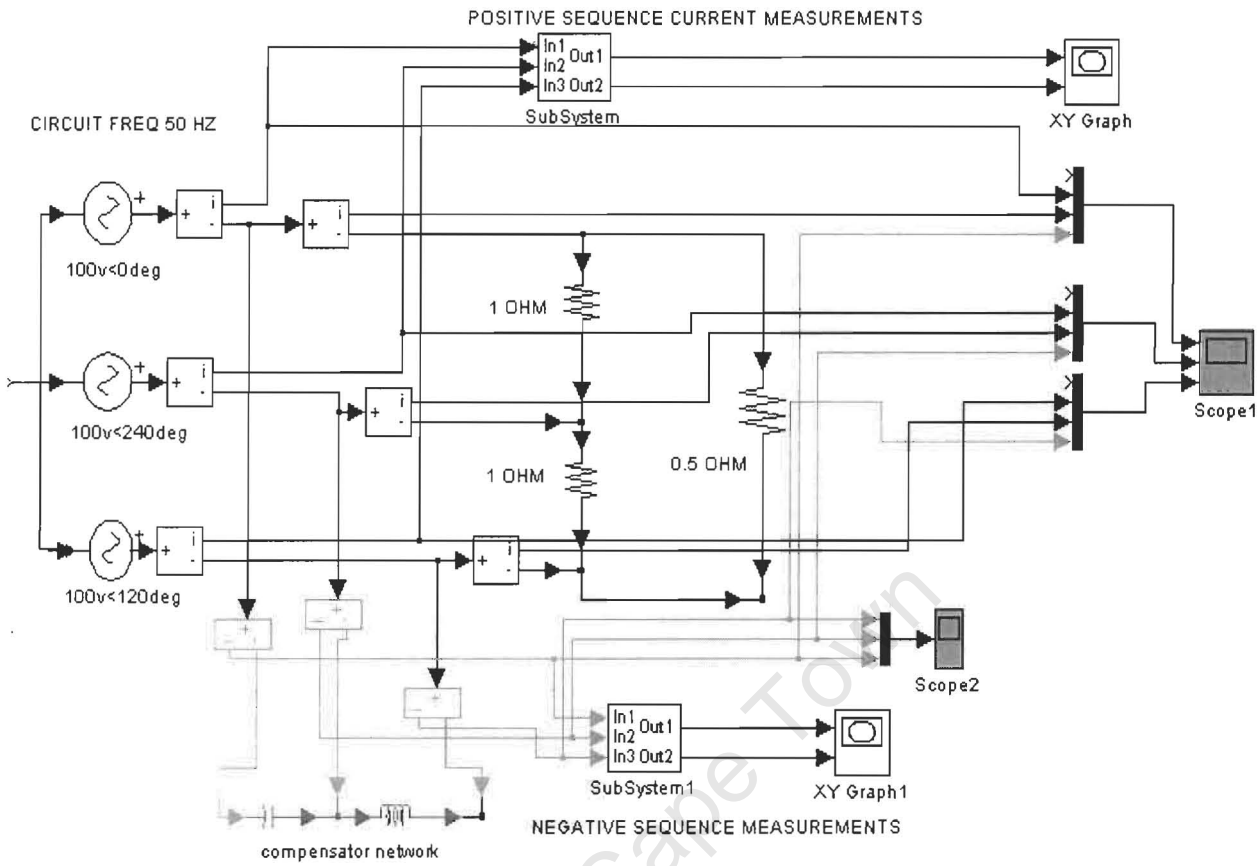


Figure 3.11

In figure 3.11, probes have been placed to monitor the source currents, the load currents and the compensator currents.

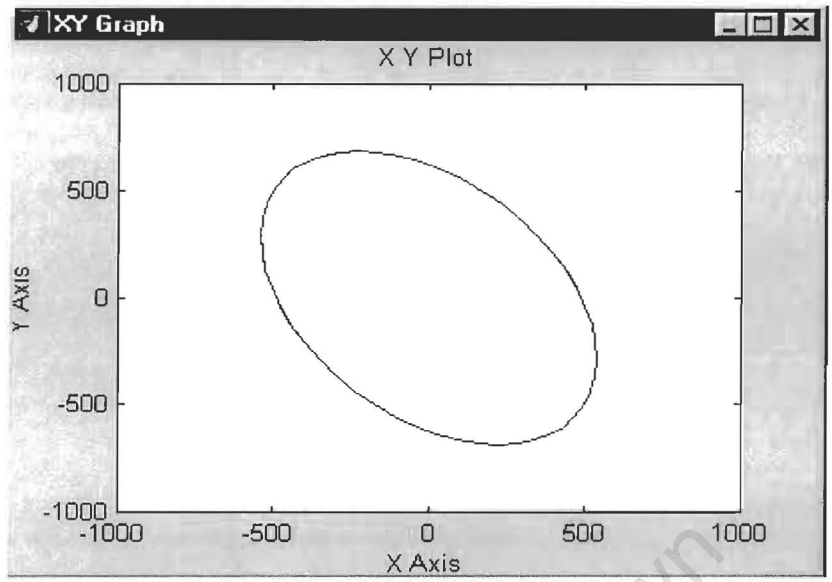


Figure 3.12

This is the space vector locus for the load current waveforms

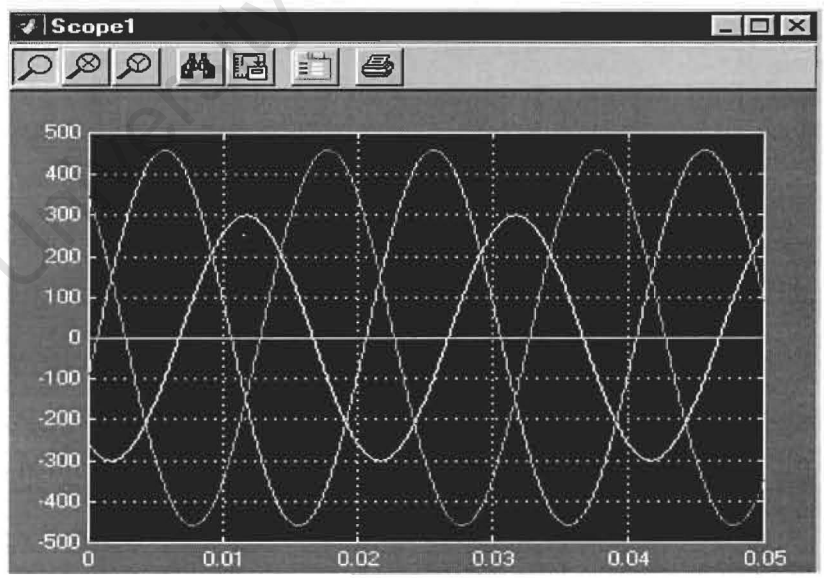


Figure 3.13

This is a scope display of load currents. They are equal to the source currents before compensation.

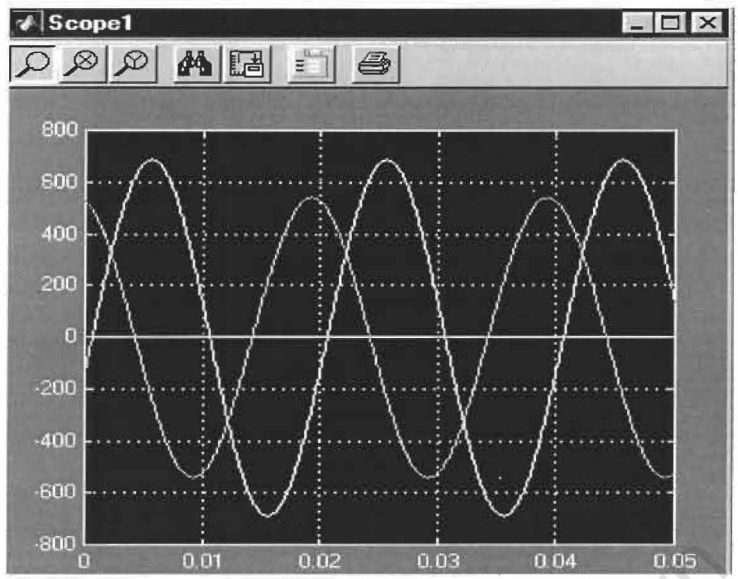


Figure 3.14

Figure 3.14 is the load current components Re I and Im I waveforms plotted against time

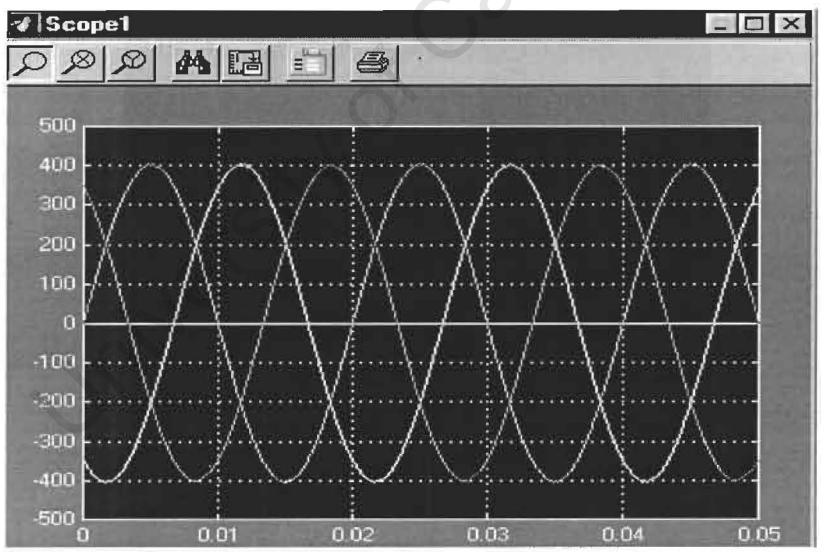


Figure 3.15

Figure 3.15 is a display of the compensated source currents

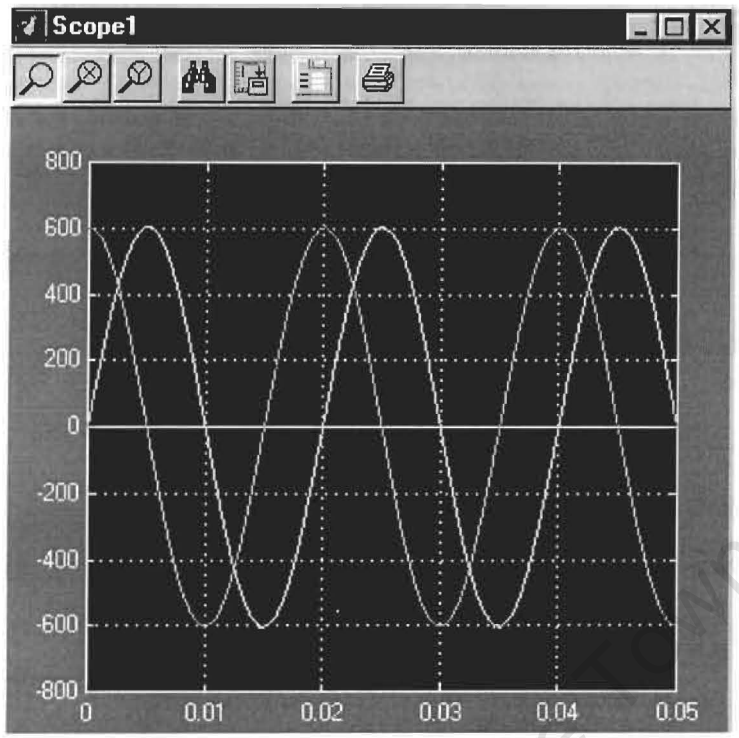


Figure 3.16

Waveforms of Re I and Im I of the compensated source currents

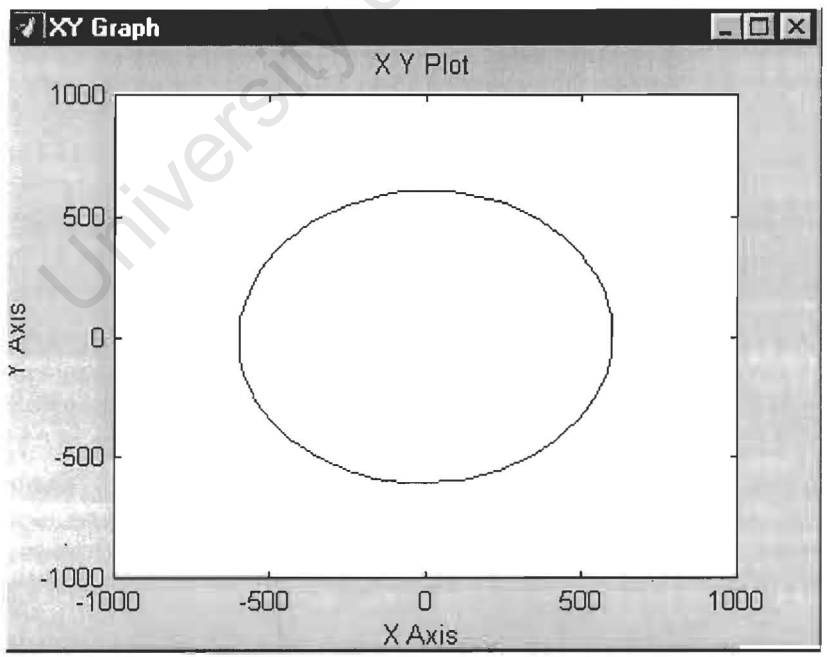
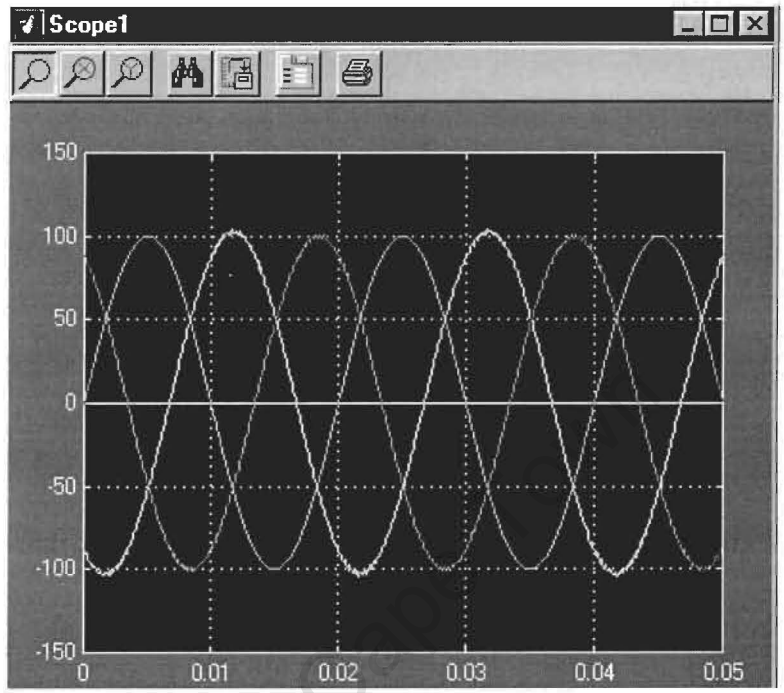


Figure 3.17

This is the XY plot of the balanced ***source*** *currents after compensation*

In figure 3.18 below are the scope waveforms of the compensator currents

Figure 3.18



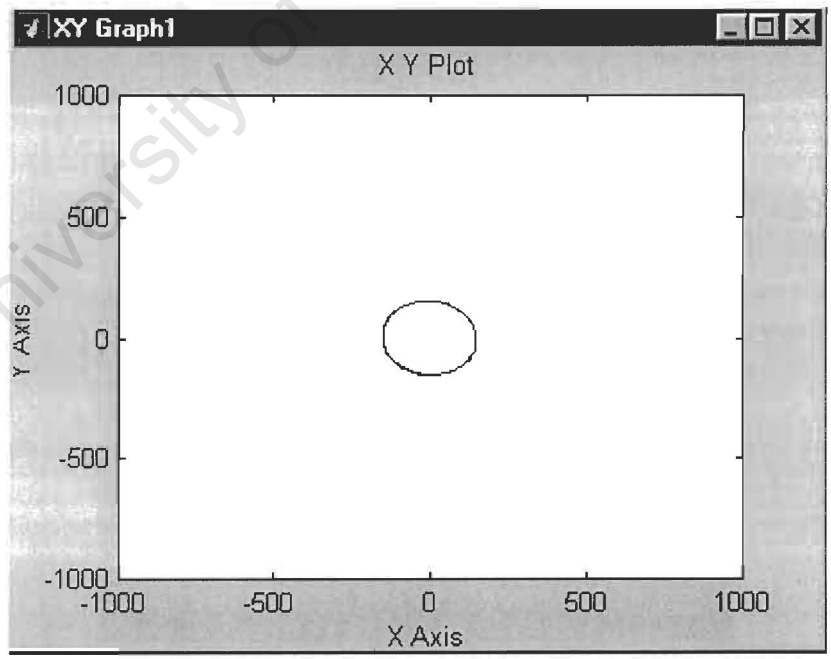
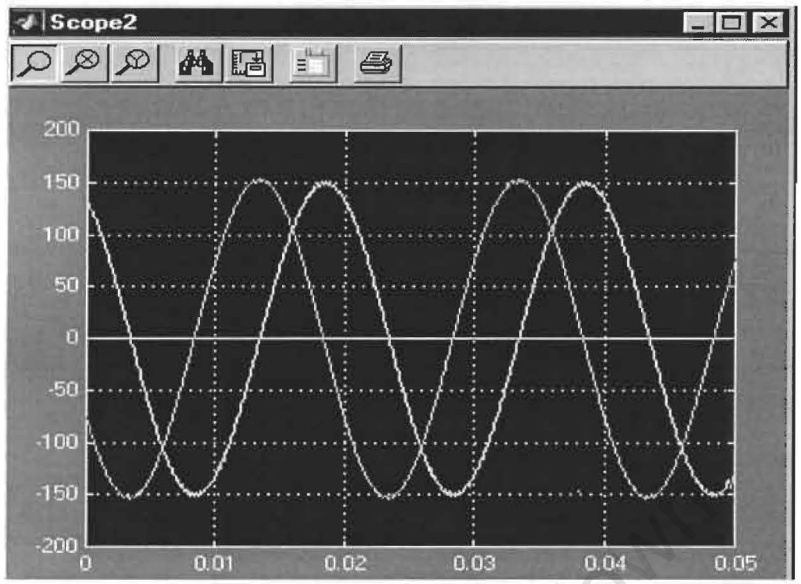


Figure 3.19

XY plot of the space vector locus for compensator currents and below in figure 3.20 is the Re I and Im I for the system compensator current.

Figure 3.20



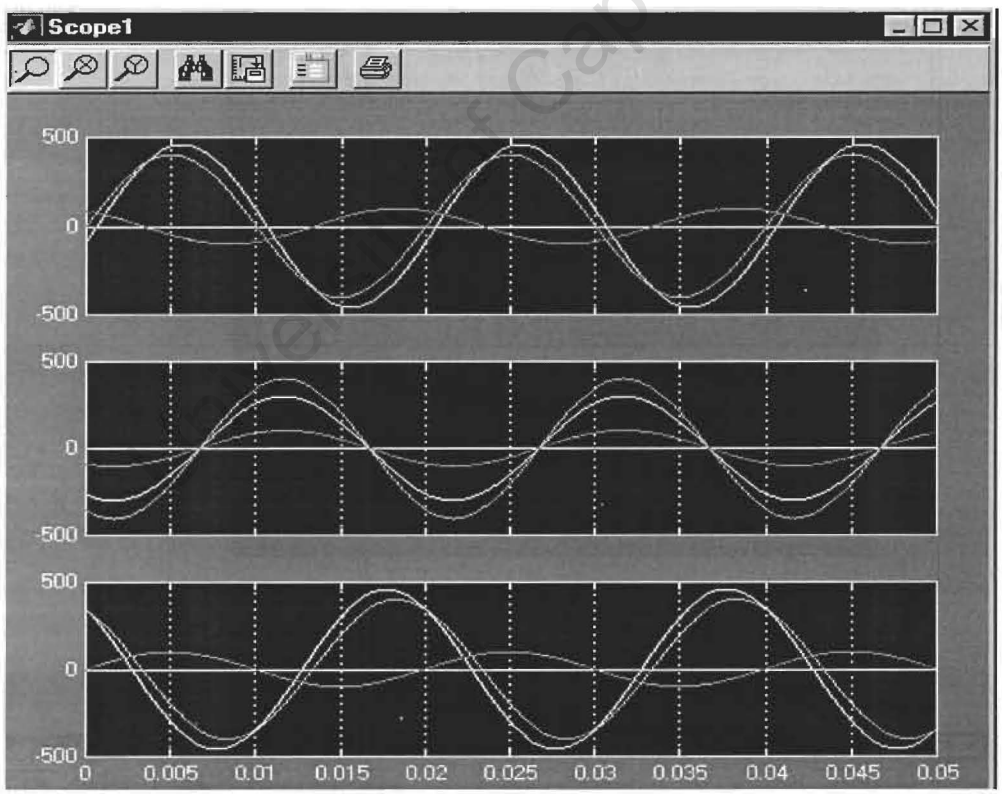


Figure 3.21

An illustration of the source, load, and compensator current and their relative amplitudes and phases for each line (note the effect of unbalance on power factor for a purely resistive load)

The above graphs in figure 3.21 show the load current, the source current and the compensator current for each line.

The biggest amplitudes are the load currents, the smallest amplitudes are the compensator currents and the medium ones are the source currents after compensation. Line 1 positive sequence current is the system reference, since it's in phase with its line to neutral voltage. Note that the load is a purely resistive but line 1 and 3 load currents are not in phase with their line to neutral voltages due to the unbalance. However the overall system power factor is still unity since line 1 load current lags the reference by exactly the same amount as line three leads.

It is evident that the compensator only corrects the source currents and not the load currents.

3.5 Designing of the complete automated compensator

This section covers the conception of the equipment from basic principles, to the final testing of the compensator system that was used in figure 3.9.

3.5.1 Decomposition of a complex signal into real and imaginary components

In section 2.3.2 and in [11] the concept of decomposing a complex current signal into constituent components was demonstrated by mathematical analysis. This author wished at this stage to devise an instrument that could decompose a complex signal. This is explained in the following illustrations.

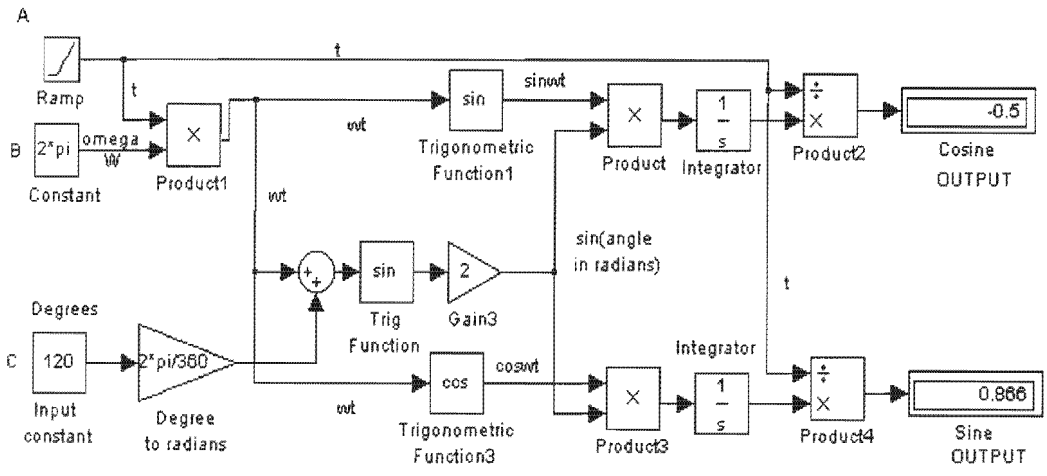


Figure 3.22

Conversion of degrees to corresponding cosine and sine

Figure 3.22 is a decomposition model; one of a large number of initial attempts. Unlike most of the others this one produced some tangible results and will be briefly described.

The aim was to feed a machine with an input in degrees and realise an output in cosine and sine. This would be similar to decomposition into real and imaginary components.

At A the ramp simulates time, t. At B is a constant, 2π, which is ω for a frequency of 1 Hz. The multiplier function, next, creates ωt. With the help of trigonometric functions, next, $\sin\omega t$ and $\cos\omega t$ are born as illustrated.

At C an input in degrees is converted to θ radians. This constant is added to ωt before a trigonometric function and an amplifier give $2\sin(\omega t + \theta)$.

Using the identities

$\text{SinASinB} = \frac{1}{2}(\text{Cos}(\text{A-B}) - \text{Cos}(\text{A+B}))$ and $\text{SinACosB} = \frac{1}{2}(\text{Sin}(\text{A+B}) + \text{Sin}(\text{A-B}))$

The following two functions can be executed

$$\frac{1}{T}\int 2\sin(\omega t + \theta)\sin\omega t dt = Cos\,\theta \quad (\text{f} = 1 \text{ and } \text{T} = 1)$$

And $$\frac{1}{T}\int 2\sin(\omega t + \theta)\cos\omega t dt = Sin\,\theta$$

The results were very exciting. The model was capable of processing any value of angle whether negative, positive, or greater than 360°. In figure 3.22 the cosine and sine of 120° are computed and correctly displayed as -0.5 and 0.866 respectively.

The following period was spent trying to get some results from a periodic complex signal using the model. There was no positive result. In the nutshell, it was a total disaster!

So, sadly, the design could not be developed beyond its initial success and the author had to go back to the "drawing board."

Figure 3.23 was proposed next, from the following concept.

The dot product of the instantaneous current and instantaneous voltage is real power and is given by.

$$\mathbf{i}\cdot\mathbf{v} = \|\mathbf{i}\|\,\|\mathbf{v}\|\cos\theta = p_{average} \tag{3.7}$$

Assuming the functions are periodic, *iv* can be integrated over a period to give average power.

$$\frac{1}{T}\int ivdt = P \tag{3.8}$$

If P is divided by the square of the voltage one should get the conductance, G, of the load.

$$\frac{\frac{1}{T}\int ivdt}{\frac{1}{T}\int vvdt} = \frac{\int ivdt}{\int v^2 dt} = G \tag{3.9}$$

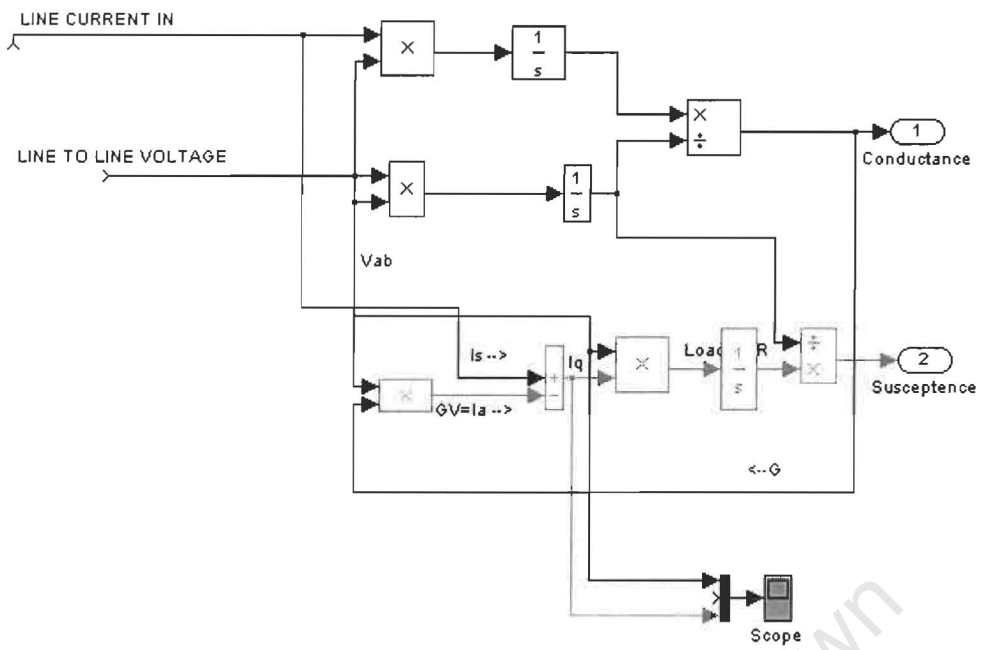


Figure 3.23

In figure 3.23 current and voltage signals are fed to a multiplier. The output is fed to an integrator. At the same time the voltage signal is fed to two inputs of a similar multiplier where it is squared and also integrated. The two integrals are fed to a divider, which executes the function in equation 3.9. This successfully extracted the conductance, G, in the first instance.

The next stage was to extract the susceptance B from the same signal. This was a failure!

Refer to figure 3.23. The conductance from the top operation is fed back and multiplied by the voltage yielding the real part, I_a, of the complex line current, I.

$$G \times V = I_a \qquad (3.10)$$

With sinusoidal conditions and a linear load it follows therefore that the remainder of the current is the reactive component, I_q.

$$I - I_a = I_q \qquad (3.11)$$

It was then assumed that the product of the reactive current, and the voltage, (VI_q) when divided by the square of the voltage, V^2, would yield the susceptance, B, in the same way a similar operation yielded the conductance, G in equation 3.9.

The following scope outputs in figure 3.24 illustrate what happens when one integrates the product between the voltage and the reactive line current, ($\mathbf{i}_q \cdot \mathbf{v}$) over a period.

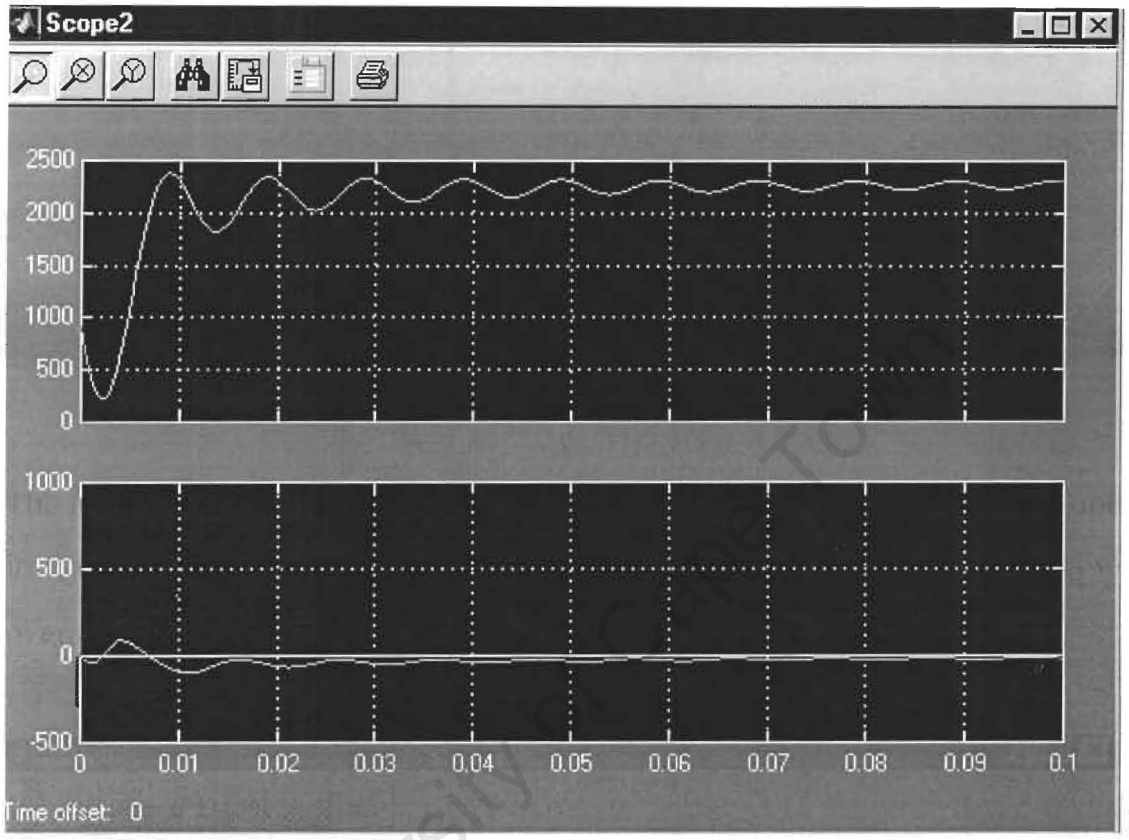


Figure 3.24

The top display is the integration of the original line current, I and the voltage, v. The final value is about 2200.The bottom display is the integral of the product of the reactive current, Iq, and the voltage, v. The result is a nil!

In section 2.4.3 it is, in fact, suggested that to get tangible results, Iq must be multiplied by V(-π/2). This is the same voltage but delayed by 90°. In figure 2.10 it is illustrated how a line-to-neutral voltage is perpendicular to one of the line-to-line voltages in a symmetrical three-phase voltage supply.

So what does one do in the absence of a three-phase supply (let alone a symmetrical one)?

The following period was spent trying to get the 90° phase delay from V. Several models were proposed as will be subsequently explained.

3.5.2 Delaying the voltage by 90°

The first method that was tried was the one suggested in section 2.4.3. In order to get a delayed equivalent of line-to-line voltage V_{ab}, the third line-to-neutral voltage V_{co} is amplified by a gain of $\sqrt{3}$ before being multiplied by the reactive current I_q. Figure 3.25 is a model to simulate the set up. This one worked, but after some hitches with the feedback loop. The conductance signal creates a surge that must be suppressed.

Later the feedback loop was removed when it was realized that

$$\int i_q v(-\pi/2)dt = \int iv(-\pi/2)dt \qquad (3.12)$$

(*i is the instantaneous total complex current and iq is the reactive current*)

The reactive current could be extracted automatically from the total complex current by the phase-shifted voltage. This is the same way the real current component is extracted using the original voltage.

The result was a compact and yet more accurate model, in figure 3.25, below.

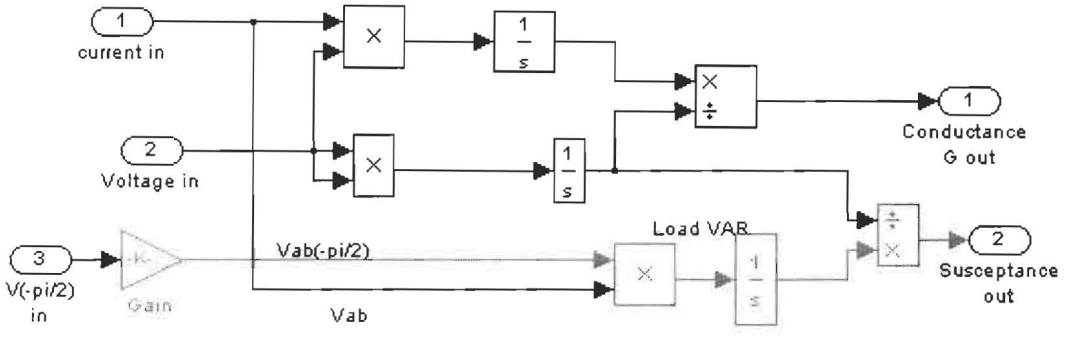


Figure 3.25

Improved admittance meter

(b) The next proposal for getting V(-π/2) was an RC network figure 3.26.

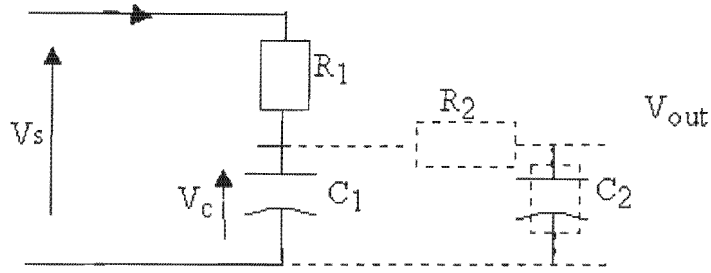


Figure 3.26

In figure 3.26, if Vs is an ac voltage source across the RC series network, then the voltage drop, V_c, across C_1 the capacitor, is given by

$$V_c = V_s \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega RC} V_s$$

$$V_c (1 + j\omega RC) = Vs \qquad (3.13)$$

If $\omega RC = 1$,

$$V_c (1 + j) = Vs \qquad (3.14)$$

Then V_c will lag V_s by 45°.

So if the same operation is repeated with a similar RC network (like in figure 3.26) in cascade the required 90° delay will be realized.

This design was criticized for being frequency dependent. The value of C is worked out by assuming a stable frequency. If there should be a big frequency drift then it could become vulnerable. So it was shelved!

(c) Another option that was considered was an operational amplifier (op-amp) integrator, with unity gain in figure 3.27.

The gain is given by equation 3.15.

$$Vout = Vin(\frac{1}{j\omega RC}) \qquad (3.15)$$

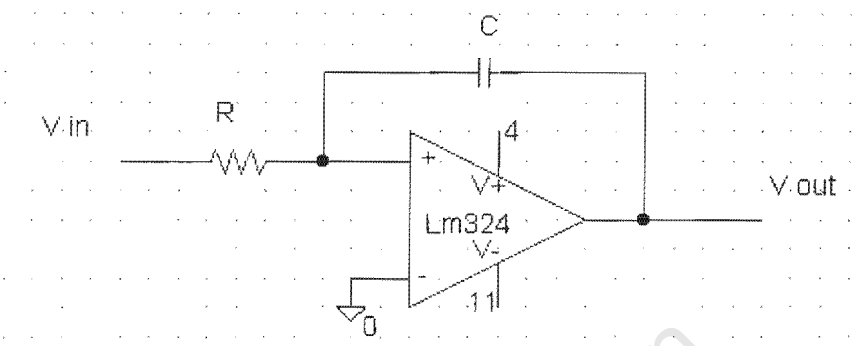


Figure 3.27

Schematic of an integrator using an operational amplifier for 90° phase shifting

This would technically guarantee an output delayed by 90° under all conditions of frequency and gain.

Saturation problems, however, made this option cumbersome, so it was also shelved.

If one re-examines the equation 3.13

$V_C (1 + j\omega RC) = V_S$

When ωRC is made very large compared to 1, then

$V_C (j\omega RC) \cong V_S$ (approximately) (3.16)

V_C and V_S will for all practical purposes be 90° apart for all frequencies and a single RC branch is all that will be required. It is simple to design.

This was adopted and worked perfectly on the computer simulation. Later with real electronics components amplifying the phase-shifted voltage back to 100% without interfering with the signal polarity proved a challenge. The

function of signal polarity is to ensure that the instrument output values for inductors are not mistaken to be capacitors. In order for a given susceptance measurement to be ascertained as capacitive and not inductive the phase shifted voltage must lag the original voltage. For a signal that must go through amplifiers, care must be taken so that amplifier inversions do not subvert this order.

3.5.3 Testing the completed admittance meter

Having sorted out that last hitch, the next stage was to test the instrument. A complex load with known parameters and connected to a single-phase supply was set up.

In figures 3.28 and 3.29 loads are set up for measurement. One has a resistive/ capacitive load and the other has an inductive/resistive one. The displayed results show that the admittance meter readings are correct for both magnitude and susceptance polarity. The inductive reading is negative and the capacitive reading is positive as should be.

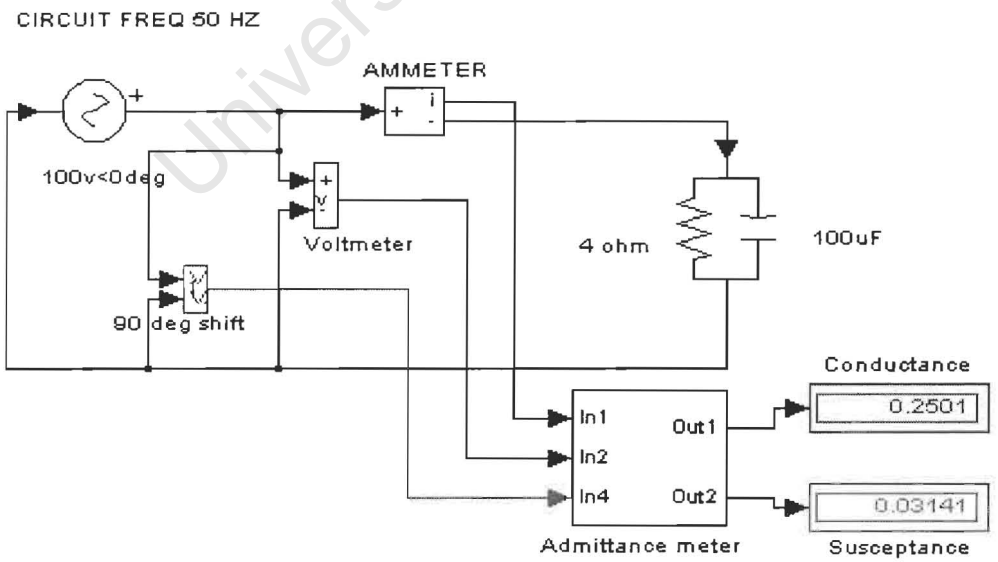


Figure 3.28

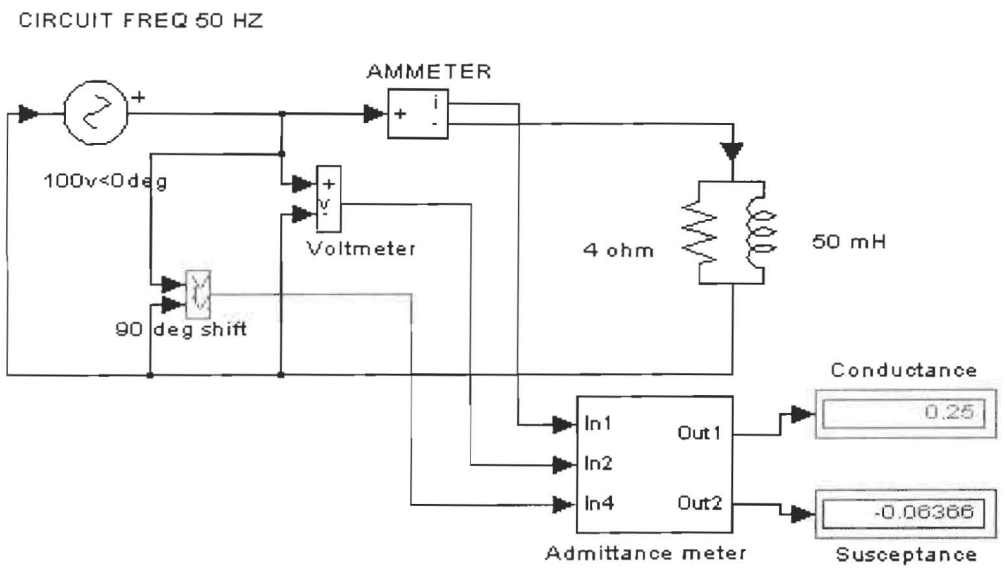


Figure 3.29

Admittance meter measuring a resistive/capacitive load in 3.28 and resistive/ inductive load in 3.29

3.5.4 Designing and testing of the compensator susceptance computer

The expressions for working out the compensating susceptances from the admittance readings were derived in appendix 2. From these expressions the computer model in figure 3.30 was designed.

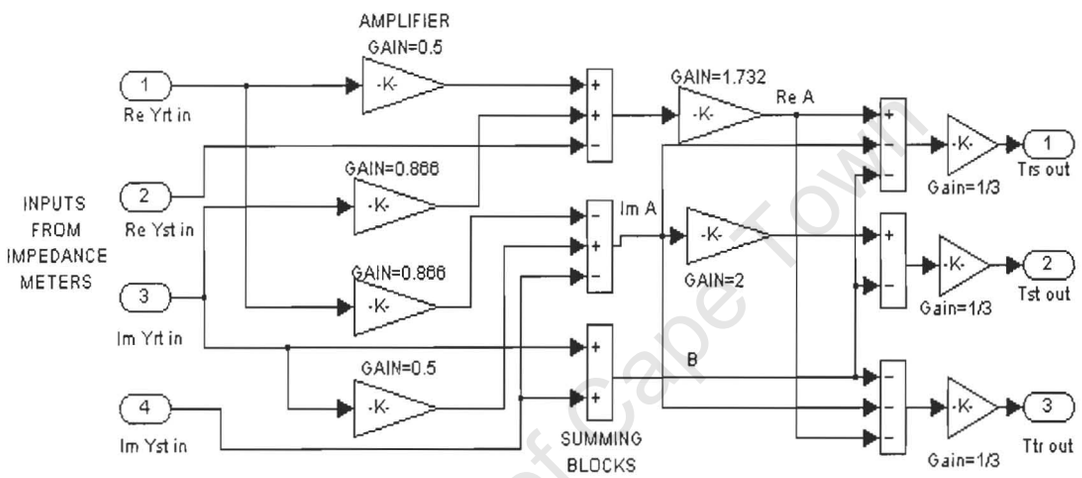


Figure 3.30

The expressions for the outputs are

$$A = -(Y_{st} + \mathbf{a}Y_{rt}) = -(Y_{st} + (-1/2 + j\sqrt{3}/2)Y_{rt}) \quad (3.14)$$

(From where Re A and Im A are derived)

And

$$Be = Im\,(Y_{st} + Y_{rt}) \quad (3.15)$$

Then finally the compensator branch elements

$T_{rs} = (\sqrt{3}\ Re\ A - Im\ A - Be)/3$

$T_{st} = (2Im\ A - Be)/3$

$T_{tr} = -(\sqrt{3}\ Re\ A + Im\ A + Be)/3$

The next stage was the setting up of a complete three-phase supply/load system together with the measurement equipment and put it to test.

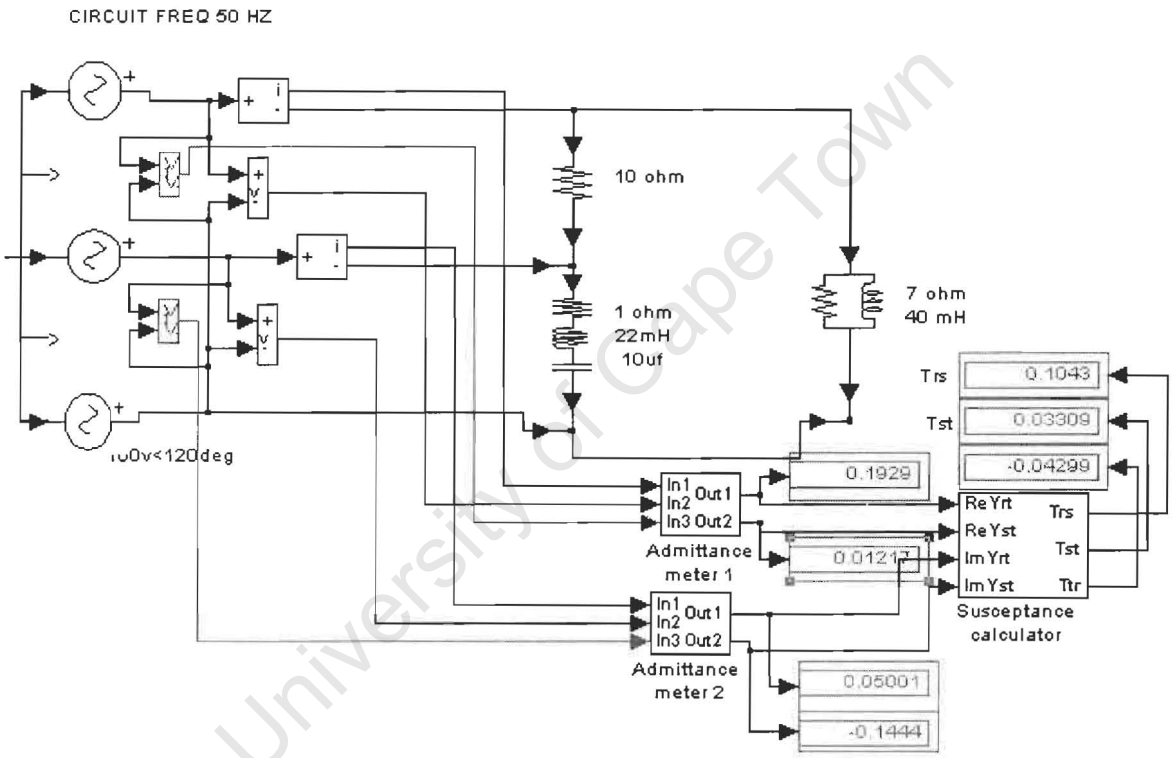


Figure 3.31

Figure 3.31 is comprised of a delta load with complex admittances as indicated. Admittance meter 1 has a fictitious conductance measurement of 0.1929 and susceptance 0.01217, while meter 2 reads a conductance of 0.05001 and a susceptance of -0.1444. The data is fed to the susceptance computer described in figure 3.30. This gives the following compensator susceptances.

Trs = 0.1043

This is positive and therefore a capacitance whose value (at a supply frequency of 50 Hz) is given by

$\omega C_{rs} = T_{rs} = 0.1043$

C = 332 μfarads (This is the compensator value between lines r and s.)

$T_{st} = \omega C_{st} = 0.03309$

C_{st} = 105.3 μfarads to compensate across lines s and t.

Finally

Ttr= -0.04299 = -1/(ωL)

$L_{tr} = 1\ \Phi\ (0.04299 \times 100\pi) = 74$ mHenrys.

These three components were installed and both load balance and power factor correction, were achieved.

3.5.5 Designing automation for the compensator feedback

Having confirmed that the computed values work the next stage was to try and create an automated feedback system.

A controllable current source is available in the simulation toolbox list. See appendix 1. Its characteristics were investigated before it could be used.

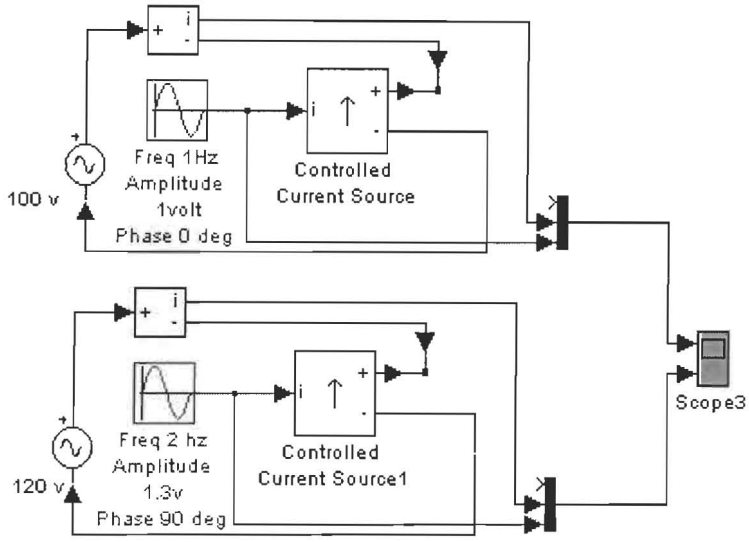


Figure 3.32

Investigating the characteristics of a controllable current source by comparing its behavior under different circuit conditions

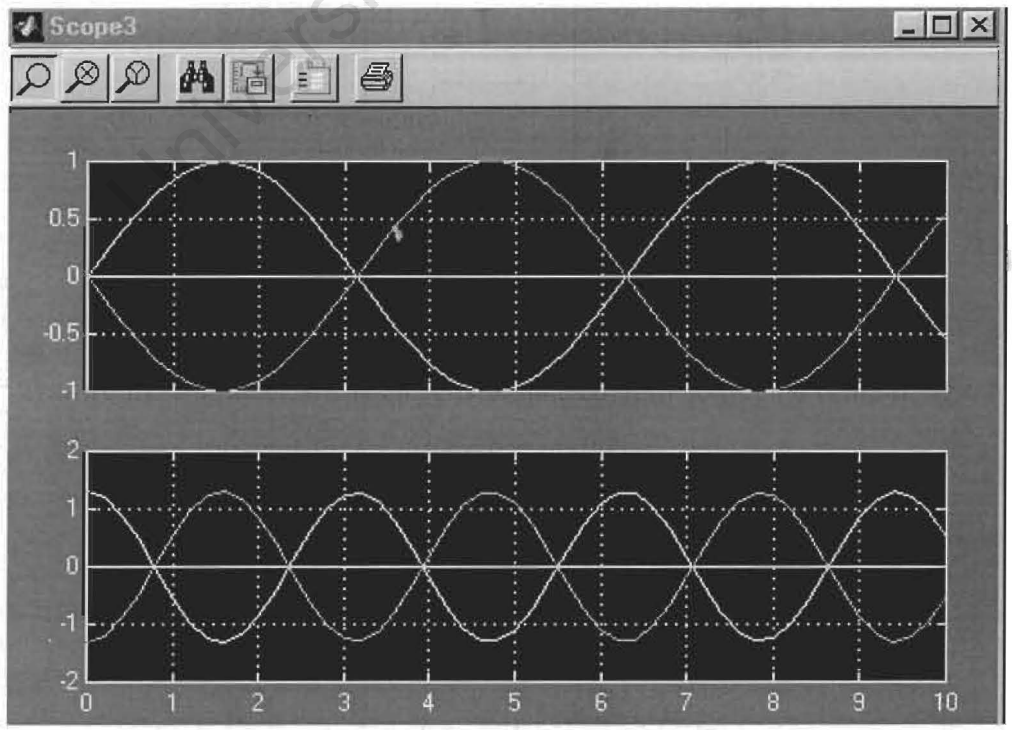


Figure 3.33

Comparison of two identical current sources under different circuit conditions

Figure 3.32 is comprised of two circuits where in each case a voltage source feeds a current controlled source. Each current source is controlled by a signal generator. The conditions of the two circuits are totally different. In each case the line current and the control signal are measured and displayed by the oscilloscope. The individual circuit conditions and measurement results are as follows.

	Top circuit	**Bottom circuit**
Supply voltage		
• Amplitude	100 volts	120volts
• Frequency	60 Hz	60 Hz
• Phase	0°	0°
Control signal		
• Frequency	1 Hz	2 Hz
• Amplitude	1 volt	1.3 volts
• Phase	0°	90°
Resulting line current		
• Frequency	1Hz	2 Hz
• Amplitude	1 volt	1.3 volt
• Phase	180°	270°

The above data strongly suggests that the current flowing through the current source (under test) is a replica of the control signal and 180° out of phase. (The author carried out further tests and confirmed this.)

This is good news.

The compensator current, Ic_{rs}, due to a susceptance, T_{rs}, across lines r and s

(with a voltage V_{rs} between them) is given by

$Ic_{rs} = T_{rs} \times V_{rs}$

Therefore a multiplier function fed with the voltage signal (from a meter across V_{rs}) and the computed dc susceptance signal (T_{rs},) should yield the right current for compensation.

If then a current controlled source should be connected across the same lines, as a compensator element, the right amount of compensator current will be injected into the system.

Precaution must be taken!!

Compensator currents are reactive and must therefore be at right angles to the line-to-line voltages. Since the susceptance values are dc signals the their effects on phase can only be either 0°(when they are positive) or 180° (when they are negative; distinguishing between capacitance and inductance). In order to effect a 90° phase change the voltage fed to the multiplier must be $V_{rs}(-\pi/2)$, the aforementioned delayed voltage. This is in the case of the compensator element between supply lines R and S. In addition, the polarity of the dc compensator susceptance must be reversed (to compensate for 180° shift inherent in the controllable current source), prior to being multiplied by the $V_{rs}(-\pi/2)$.

The next step was a set up of a simulation to verify the assertions above.

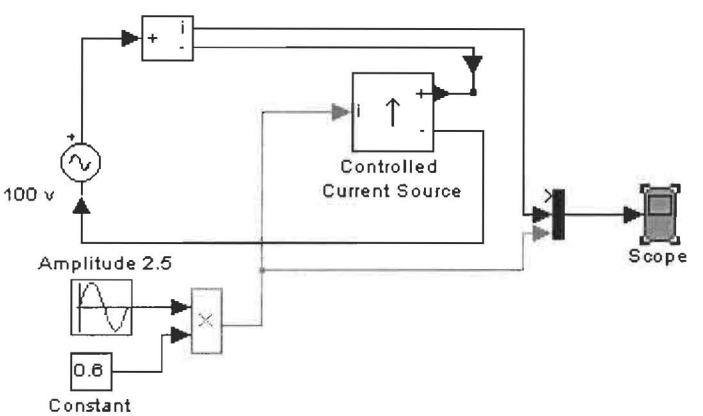


Figure 3.34

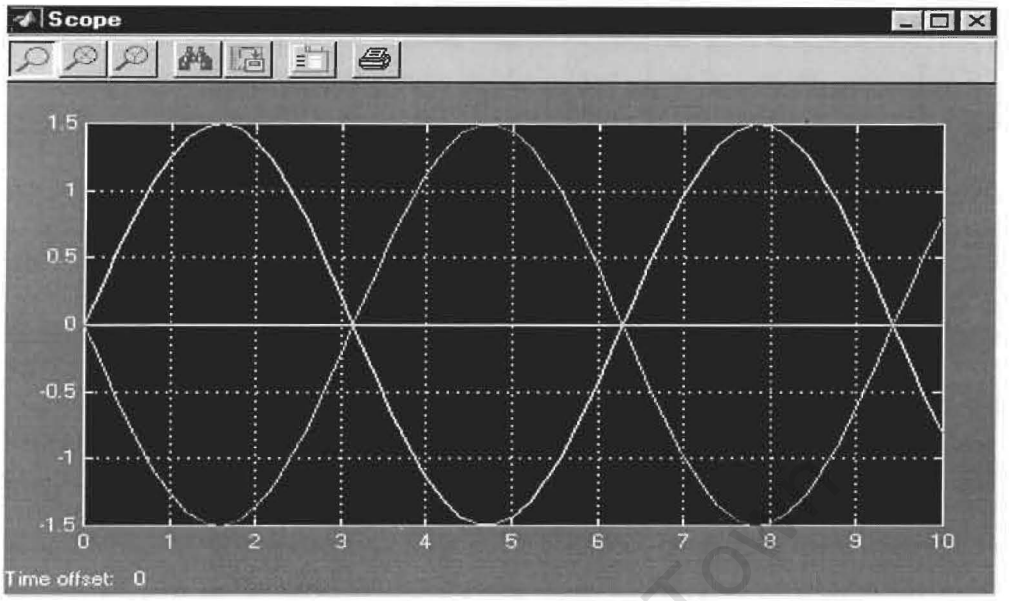


Figure 3.35

The results of the test in figure 3.34

In figure 3.34 a sine wave signal with an amplitude of 2.5 volts is multiplied by a dc signal (a constant) of amplitude 0.6volts. The result is a signal of the same frequency and phase (plus 180°) as the sine wave, but an amplitude of 1.5 volts; which is the product of (0.6 x 2.5). This is verified by the scope display in figure 3.35.

At this juncture a complete three-phase semi automated model was set up.

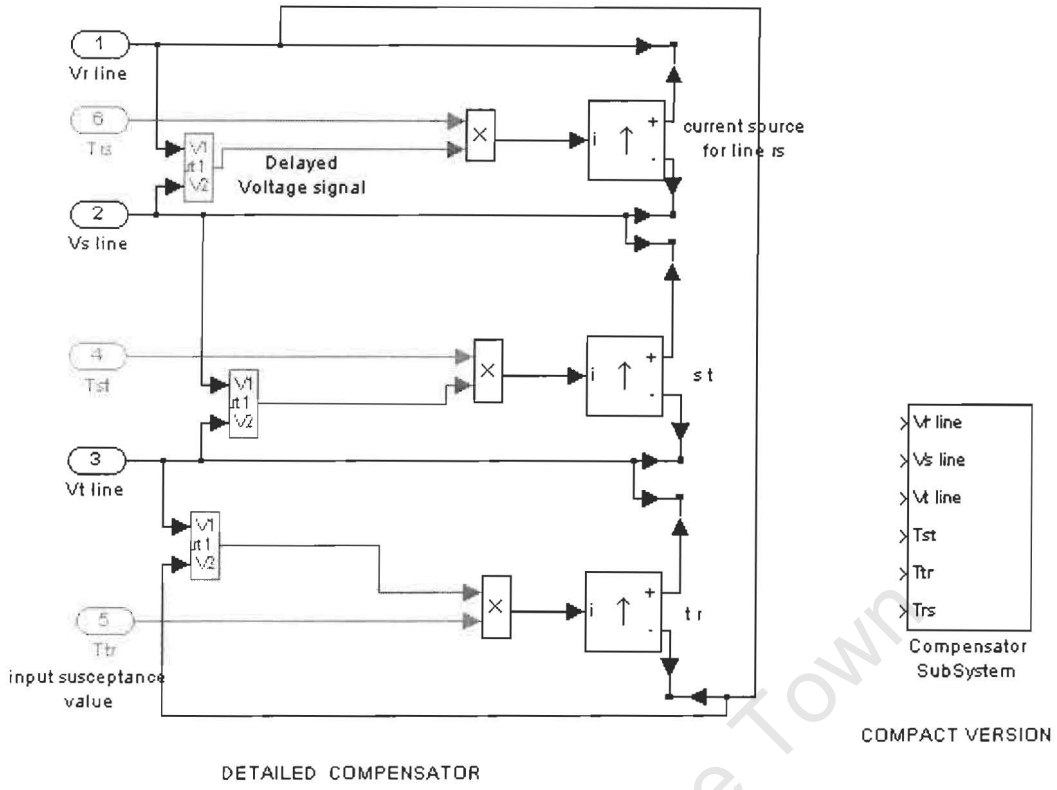


Figure 3.36

Connecting all three compensator current sources in delta configuration

In figure 3.36 a complete detailed model and its boxed compact version are shown. Between each pair of supply lines a controllable current source is connected as a compensator element. The respective control signals come from multipliers, which are fed from two sources; the delayed line-to-line voltages and the computed dc compensator signals. When a simulation of an unbalanced load was ran the susceptance computers displayed the required compensator susceptances, T_{rs}, T_{st} and T_{tr}. These values were in turn set into dc storage buffers called "constants" feeding the multipliers in figure 3.36. The load was compensated during the next simulation.

In figure 3.37 the whole system loop is connected. The constants are replaced

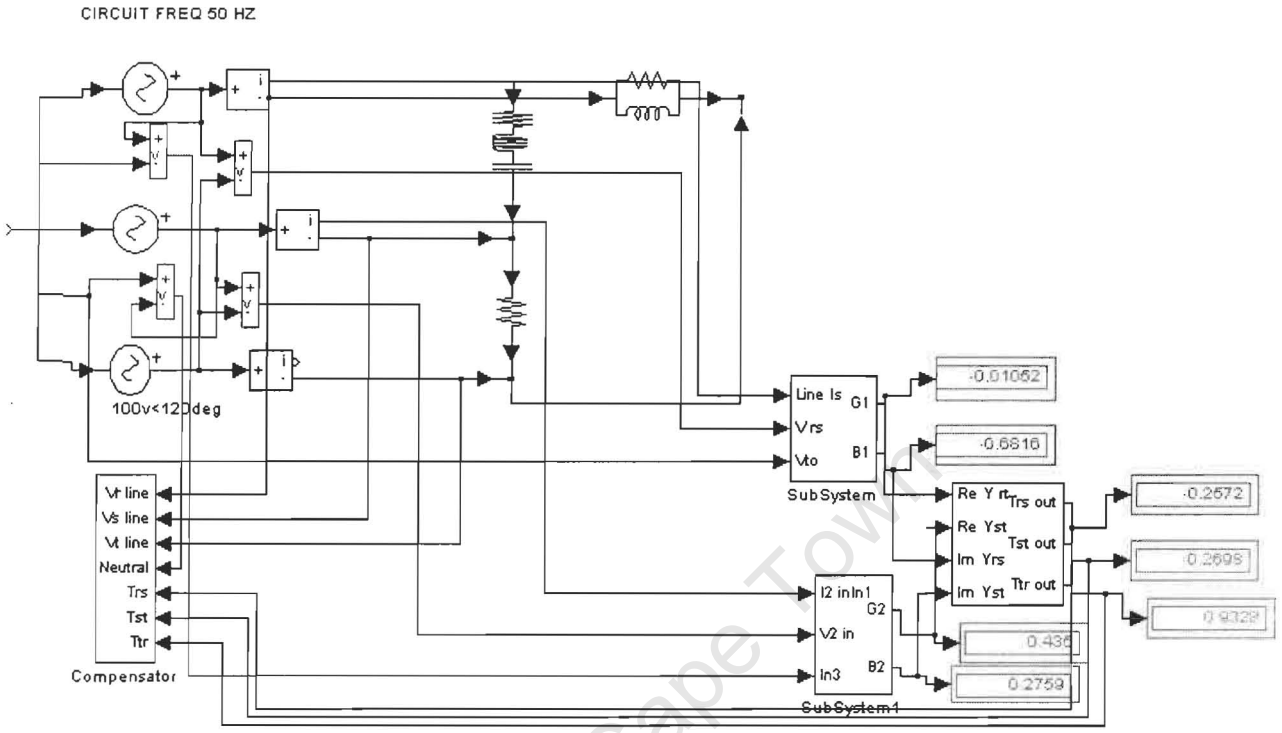


Figure 3.37

with direct connections from the susceptance computer outputs.

Closing of system control feedback loop was quite problematic. The compensator signals feeding into the multipliers that ultimately control the current sources presented surges at time, t=0, that appeared to have infinite amplitudes and shutting down the simulation. The system finally worked when these pulses or spikes were connected through appropriate buffers that did not compromise on the true rms values of the compensator signals. To improve control quality PID's (proportional integrator differentiator controllers) were added in each feedback control loop.

The following illustrations demonstrate the performance of the set up in figure 3.37, operating with a random complex load.

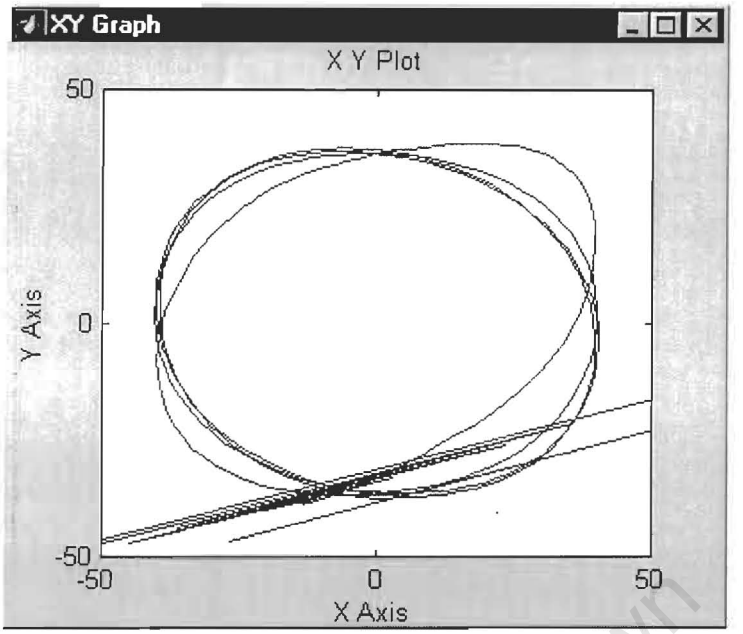


Figure 3.38

XY plot of the source current space vector.

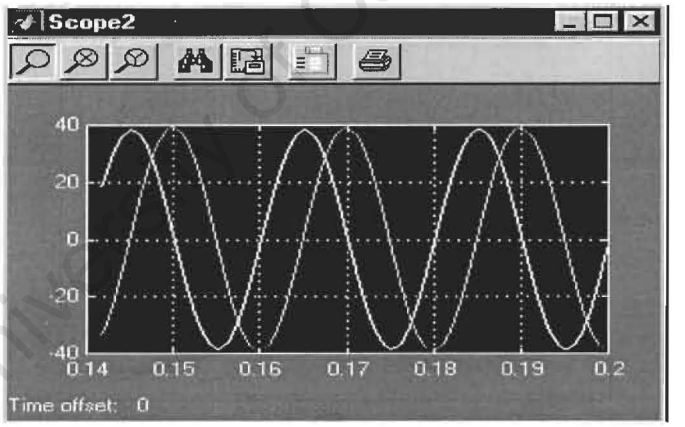


Figure 3.39

A scope display for the source current space vector. The amplitudes are equal and 90° apart. It is the clearest index of balance this time.

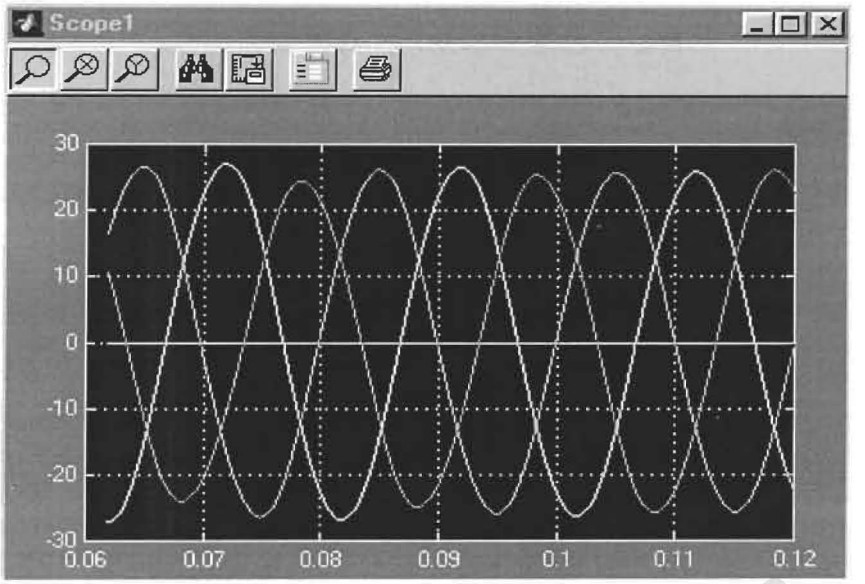


Figure 3.40

The source currents getting into balance in just under 0.1 seconds

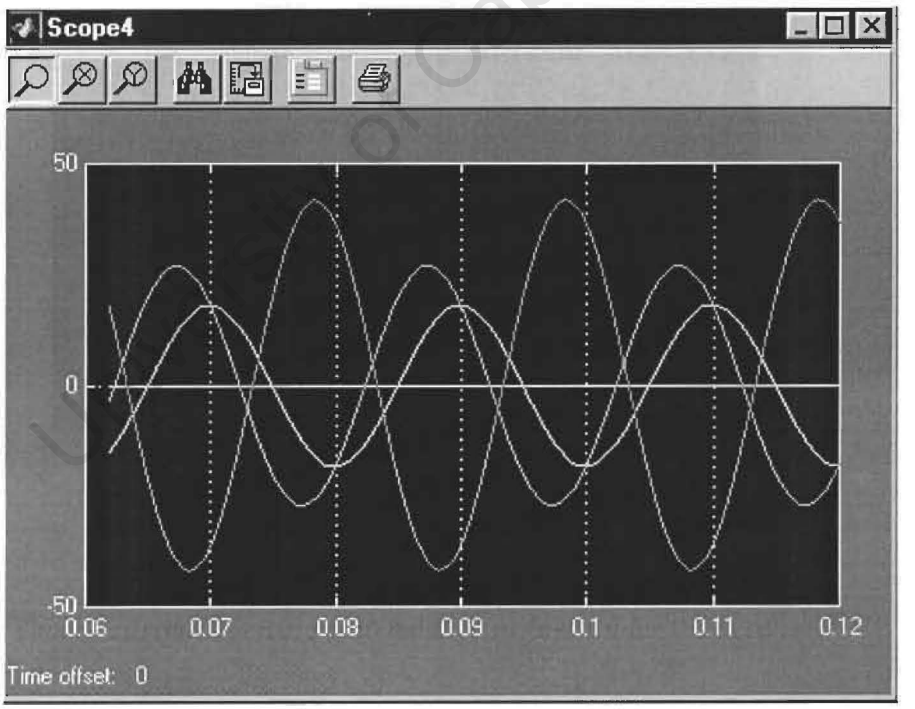


Figure 3.41

These are the load currents

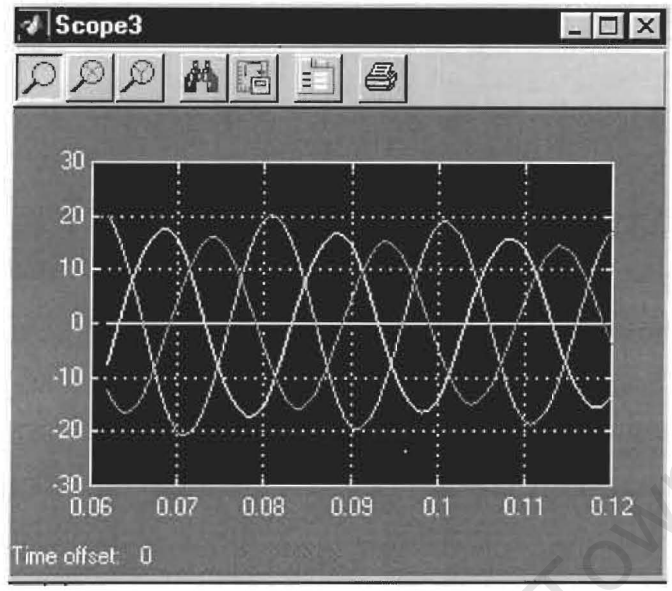


Figure 3.42

The compensator currents, which are a mixture of the negative sequence and the reactive positive sequence currents

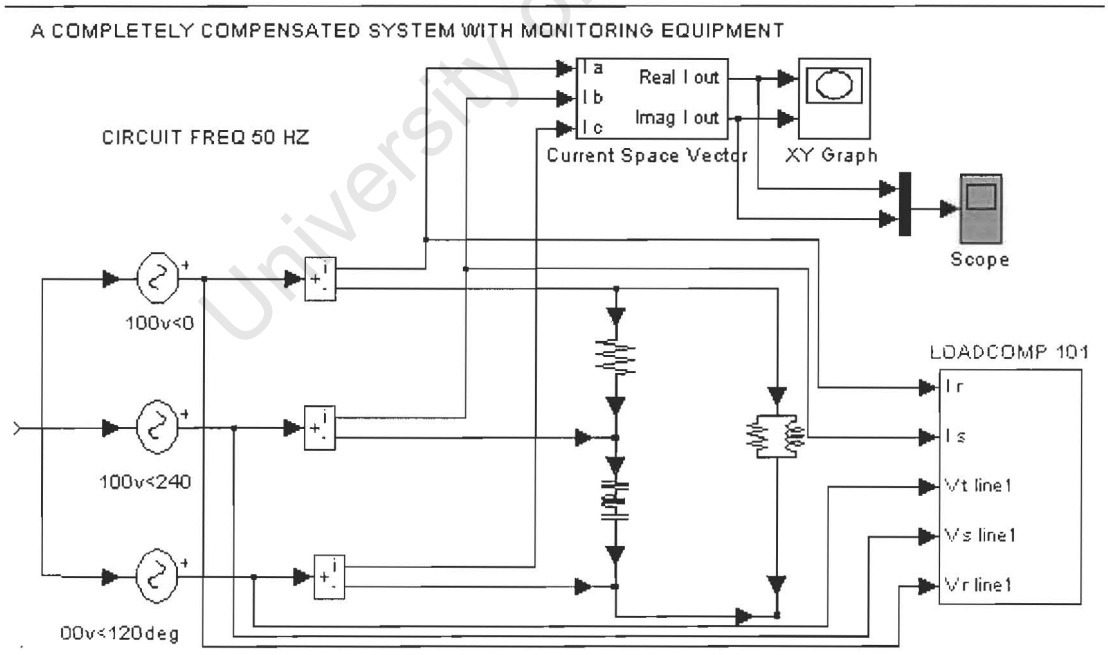


Figure 3.43

Finally all the modules are tidied up into a neat installed product "LOAD COMP 101"

3.6 Conclusion

A design and simulation based on the proposal by Czarnecki [11] has been successfully carried out. Analysis of the source currents after simulation has confirmed both load balance and power factor correction. This is a verification that the proposal by Czarnecki is realizable. It is adequate preparation for a physical design, construction and testing to be covered in chapter 4.

4 Design and construction of measurement networks

This chapter covers the physical design, construction, calibration and testing of the compensator system simulated in chapter 3. Measurements of two line currents and two line-to-line voltages will be taken in real time. The compensating susceptances will be computed and a three-phase load will subsequently be compensated for both power factor and unbalance.

4.1 Production of the admittance meters

The block diagram in figure 4.1, which was encountered in chapter 3, is a functional guide. Please also refer to the schematic diagram in figure 4.2.

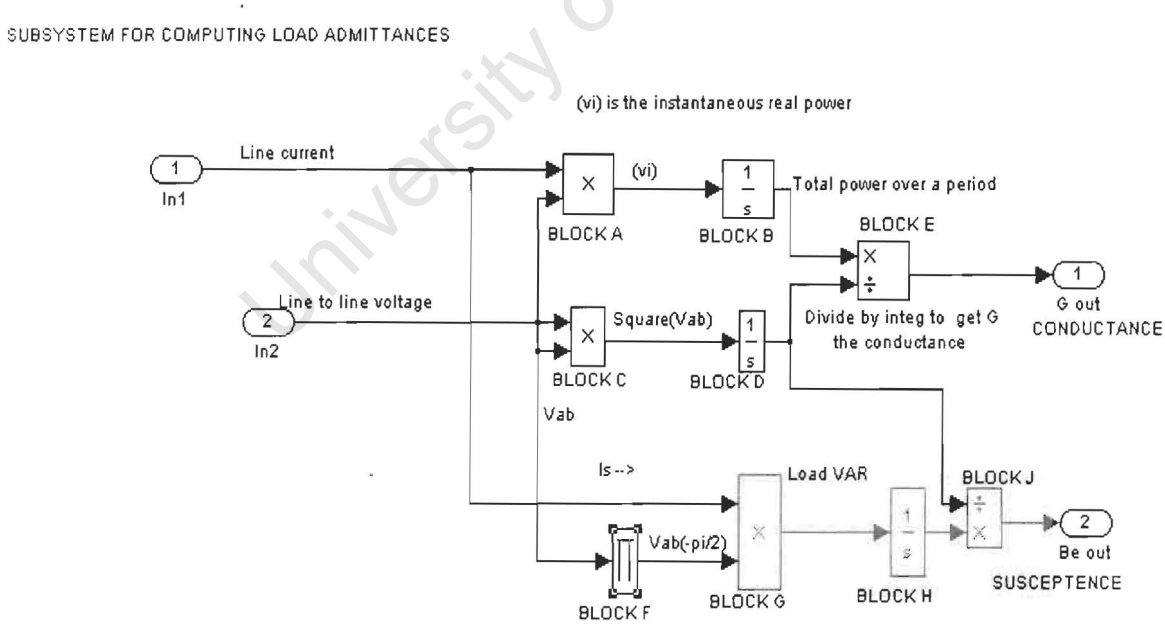


Figure 4.1
The model for extraction of conductance and susceptance

In figure 4.1, blocks A, C and G are multiplication functions, integrated circuit (IC) AD633, from Analogue Devices. A line current and the corresponding line-to-line voltage are fed into block A, which is marked as U_1 on the schematic (figure 4.2) and on the component lay out of the printed circuit board (PCB) (figure 4.8). The output is a product yielding active power at pin number 7.

From pin 7 it is integrated over an RC (resistor/capacitor) circuit with a time constant of 20msec. A variety of other combinations had been tried. It was translated into a component combination of 56k ohm and 0.33μF giving 18.4 milliseconds and worked fine.

Continuing with figure 4.1, a line-to-line voltage is fed to block C, which is marked as U_2 on the PCB. The output is the square of the voltage, V^2, which is integrated by a similar RC network, (block D). The V I (voltage x current) integral from block B is divided by the integral of V^2, from block D using block E. On the PCB it is the combination of operational amplifier (op-amp) U_{5A} and multiplier function U_6. (See appendix 3). The result is the equivalent conductance G_1 for this branch of the network.

A similar process is carried out for the measurement of the branch equivalent susceptance. This time, the line to line voltage is delayed by 90°, using block F.
As explained in section 3.5.2(b) an RC circuit was used for this function.

$$V_{out} = V_{in}/(j\omega RC + 1) \qquad (4.1)$$

When the value of ωRC is large enough V_{out} will be practically delayed by 90°.
Initially the value chosen was, ωRC = 30, but this worked out to very large values of R and/or C and had to be reduced.
What is essential is the multiplication factor between I, the line current, and V(-π/2), the delayed voltage. This is given by

$\text{Cos } \psi = \cos(\arctan(1/\omega RC))$ (4.2)

(ψ is the angle between the ideal $V(-\pi/2)$ and the real one.

Even when ωRC is only 10, $\cos \psi = 0.995$.

This is adequately accurate (technically an error of 0.5% which is far better than the tolerances of most of the other PCB components).

A combination of 100k ohm and 0.33μF achieves this result.

The above network results in an attenuation of $V(-\pi/2)$ of about 10.

$V(-\pi/2)_{out} = V_{in}/(j\omega RC+1)$

When we substitute in the values of 100k and 0.33μF

$\|V_{out}\| = 0.096 \|V_{in}\|$

$\|V_{out}\|$ must be amplified back to the value of $\|V_{in}\|$. A **non-inverting** amplifier, U7B, was chosen, specifically to avoid mixing up the phasor relationship between V_{out} and V_{in}. As has been explained, V_{out} must remain lagging V_{in}. This is vital for the distinction between capacitive and inductive susceptances at the output of the instrument.

LM324, was the op-amp type that was used as U7B. The data sheet recommends that the feedback resistor for a non-inverting configuration should be matched with the input resistance. So the same 100k was used in the gain loop. A divider resistor of 10k giving (approximately) the required gain of 10 was selected. The actual resulting gain of the stage is ((100k + 10k)/10k = 11) because of the non-inverting mode. This unwanted extra gain is left unchanged. It is scaled down at a convenient stage later on with trimmer pots (along with other circuit gain constants).

A second set of results is obtained from the second twin circuit in exactly the same stages as described above, (see figure 4.2). Once the two sets of admittance measurements are obtained the required compensator values can be worked out either manually, using the formulae (see appendix 2) or automatically by a computing network.

Note that conductance $G = (I/V)\,\mathrm{Cos}\phi$ (4.3)

Where, ϕ is the phase angle between the line current and the line-to-line voltage.

After constructing the above circuitry the twin circuits were fed with identical input sets of currents and voltages to test them. A single-phase feeding a parallel resistive/inductive load in series with a power factor meter, an ammeter and a wattmeter with a parallel voltmeter was set up.

Single-phase measurements on this equipment give the true conductance and suceptance values (and not fictitious ones as obtained for the three-phase case.) This is the best way to calibrate this equipment; using known load parameters. Trimmer pots are then set so that the instrument outputs match the load. It also ensures that both units are matched against each other.

The admittance readings in this case were compared with those calculated using the measured rms currents and voltages while taking the power factor into account.

Refer to the results in table 4.1. The calculated and the measured admittance readings initially appeared unrelated. But because both modules produced similar results, the possibility of a construction error was discounted. It was then suspected that perhaps a dc offset in the circuitry was responsible. So a subtraction column ($G_1 - G^*_1$) was created but this did not yield the desired results. (G^*_1 is the calculated conductance and G_1 the measured dc output from the PCB). However when G^*_1 was divided by G_1 a common scalar of approximately 0.667 was observed. The results strongly suggested that the PCB

circuitry was accurate. This is also confirmed by the consistent closeness displayed by the two independent twin modules as earlier pointed out.
Note that the subscripts, 1 and 2 on the conductances and susceptances denote results from the first and second PCB respectively.

Current	Watts	Power factor	G1	B1	G2	B2	PCB VOLT	G1*	G-G*	G1*/G1	Im Pf	B1*	B1/B1*
4.76	225.0	0.985	0.843	0.235	0.854	0.233	8.18	0.573	0.270	0.680	0.173	0.100	2.340
4.50	212.5	0.980	0.794	0.233	0.804	0.230	8.20	0.538	0.256	0.677	0.199	0.109	2.134
4.25	202.5	0.980	0.750	0.230	0.758	0.230	8.27	0.504	0.246	0.672	0.199	0.102	2.249
4.00	190.0	0.980	0.700	0.225	0.708	0.225	8.30	0.472	0.228	0.675	0.199	0.096	2.346
3.75	180.0	0.975	0.655	0.222	0.665	0.220	8.34	0.438	0.217	0.669	0.222	0.100	2.222
3.50	167.5	0.970	0.609	0.222	0.618	0.218	8.38	0.405	0.204	0.665	0.243	0.102	2.186
3.25	152.5	0.965	0.560	0.218	0.565	0.215	8.44	0.372	0.188	0.664	0.262	0.101	2.159
3.00	145.0	0.960	0.510	0.215	0.515	0.212	8.47	0.340	0.170	0.667	0.280	0.099	2.168
2.75	130.1	0.950	0.468	0.212	0.472	0.210	8.50	0.307	0.161	0.657	0.312	0.101	2.099
2.50	117.5	0.940	0.420	0.210	0.425	0.207	8.55	0.275	0.145	0.654	0.341	0.100	2.105
2.25	105.0	0.925	0.372	0.204	0.375	0.200	8.59	0.242	0.130	0.651	0.380	0.100	2.050
2.00	90.0	0.900	0.323	0.202	0.326	0.199	8.62	0.209	0.114	0.647	0.436	0.101	1.997
1.75	75.0	0.880	0.264	0.198	0.266	0.195	8.65	0.178	0.086	0.674	0.475	0.096	2.061

Table 4.1

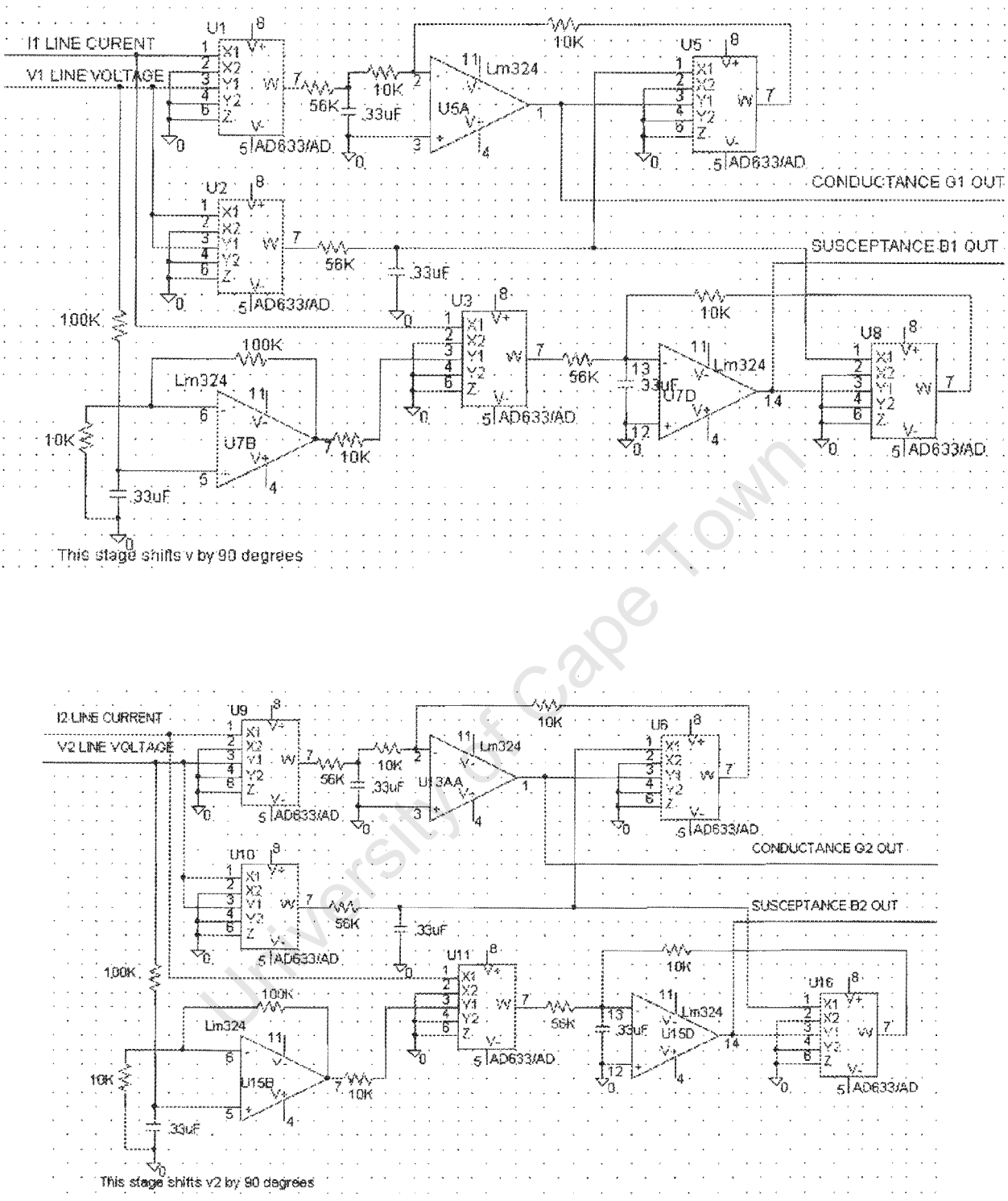


Figure 4.2
Full schematic for the twin admittance measurement meters

4.2 Production of the compensator susceptance computer

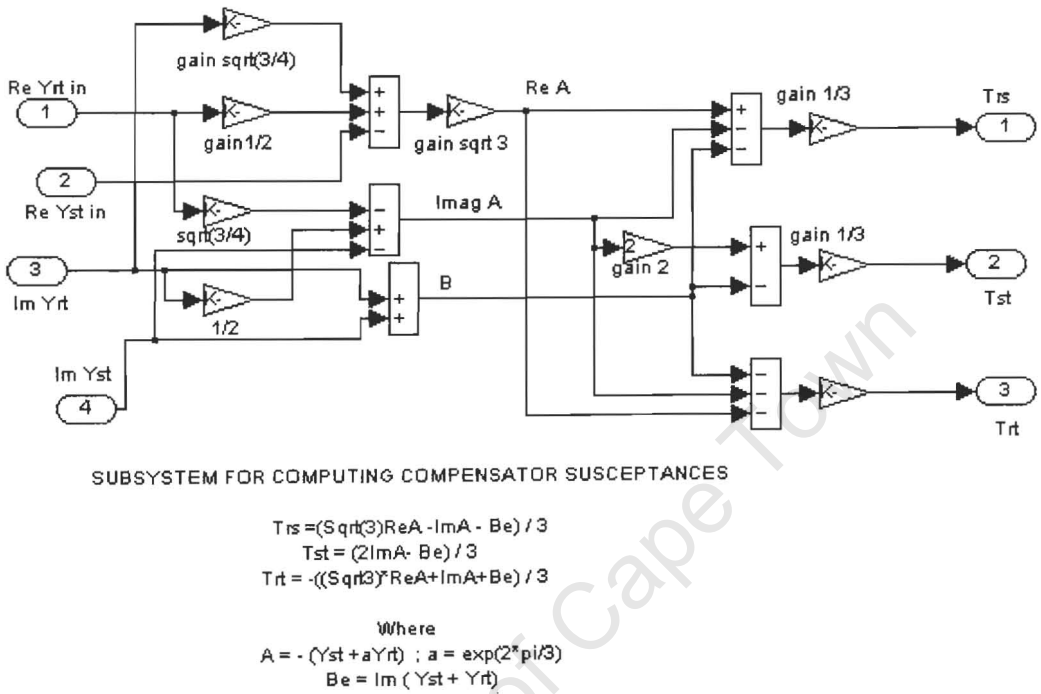


Figure 4.3

The following formulae have previously been derived (see appendix 2)

$$T_{rs} = (\sqrt{3}\ \text{Re A} - \text{Im A} - \text{Be})/3$$

$$T_{st} = (2\ \text{Im A} - \text{Be})/3$$

$$T_{rt} = -(\sqrt{3}\text{Re A} + \text{Im A} + \text{Be})/3$$

Where T_{rs}, T_{st} and T_{tr} are the required compensating susceptances and

$$Y_{st} = G_1 + jB_1$$

$Y_{tr} = G_2 + jB_2$

$A = -(Y_{st} - aY_{rt})$ is the unbalance admittance and $a = \exp(2\pi/3)$;

$B_e = \text{Im}\,(Y_{st} + Y_{rt})$, the equivalent susceptance

The above schematic (figure 4.3) previously used for computer simulation was re-interpreted into block diagrams, 4.4 and 4.6 to make it easier to translate the functions into practical electronic circuitry. Practical functional details somewhat differ from those of computer toolboxes. For example, inverting amplifiers are more convenient to work with in practice while in computer simulations this inversion problem does not exist.

Refer to the schematic in figure 4.5. The block diagram in figure 4.4, is the functional guide. The numbers in the boxes represent gains or multiplication factors of the incoming signal.

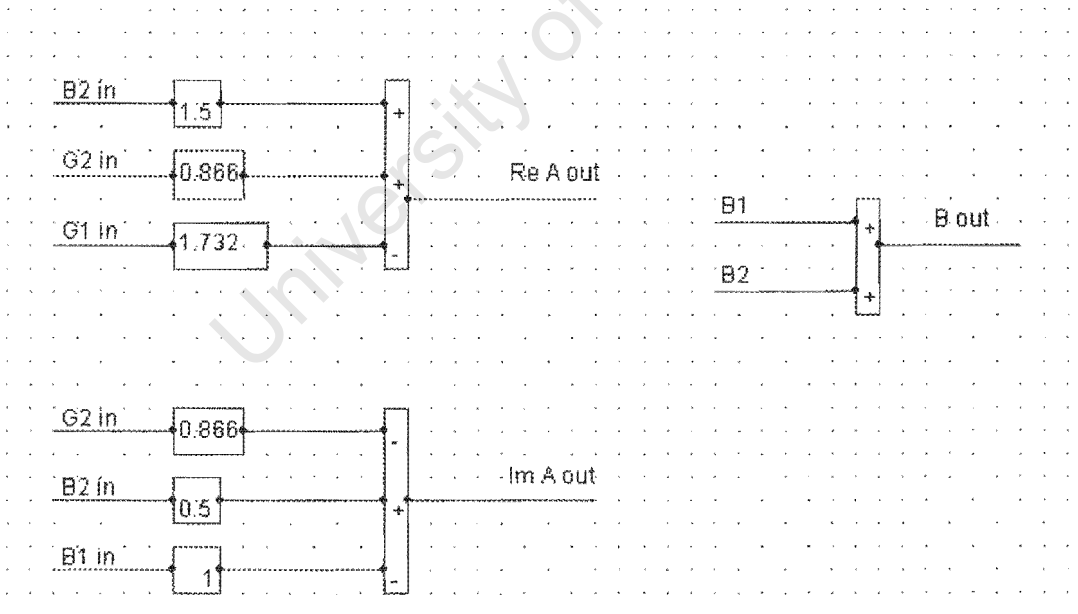


Figure 4.4

Functional block diagram for figure 4.5

As mentioned earlier the values of the metered conductances and susceptances required scaling. This was done using a quad op-amp, U2, with trimmer pots. The calibration was achieved by equating the PCB outputs with answers obtained from calculations using measured line rms currents and voltages together with the power factors. By swapping the suceptances from inductance to capacitance it also verified that the boards were both accurate and able to distinguish between capacitors and inductors.

After calibration the measurements are fed to the respective stages as indicated in the block diagrams (4.4 and 4.6) and schematics (4.5 and 4.7).

In order to produce a competitively priced product no special selection of components was done. All were regular grades generally available off the shelf. In order to minimize errors only one resistor type and size namely 10k ohm, ±5%, was consistently used throughout the networks (except for scaling and a few stages with irrational gains like √3).

The required multiplication factors were achieved by creating parallel and series combinations of the same 10k (±5%) resistor. For example the resistor configuration (of two resistors by three) of amplifier U1A (figure 4.5), gives a gain of 1.5, while that of one by two for U3B gives a gain of 0.5. It was hoped that this strategy would optimize the accuracy of the circuit.
Comparisons of the performance of this circuitry with computer simulations, were very close; strongly suggesting that the optimizing technique worked.

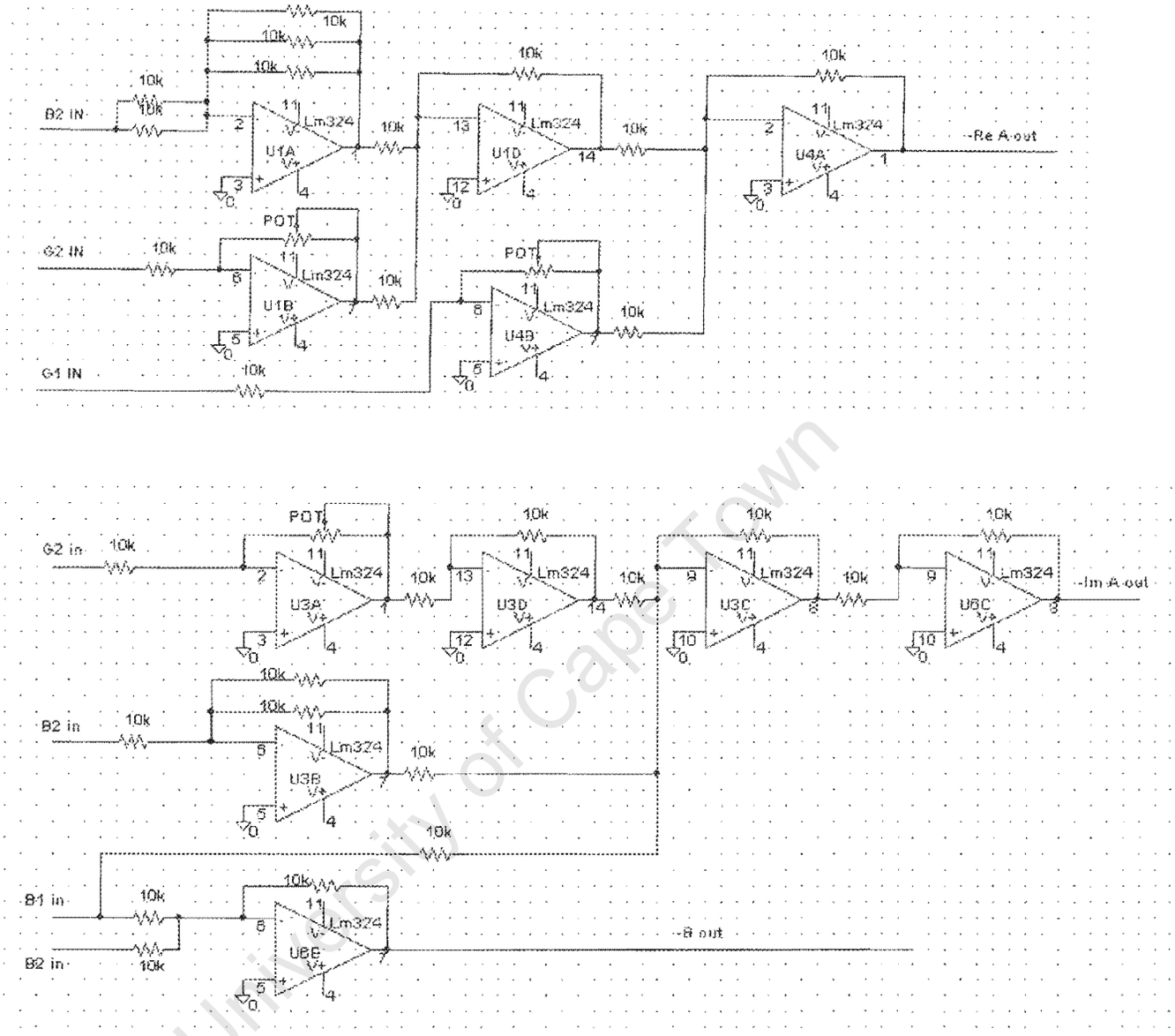


Figure 4.5

Schematic of compensator susceptance computer

The circuit configuration outputs are negative values of ReA, ImA and B. This was done deliberately in anticipation of inverting stages ahead.

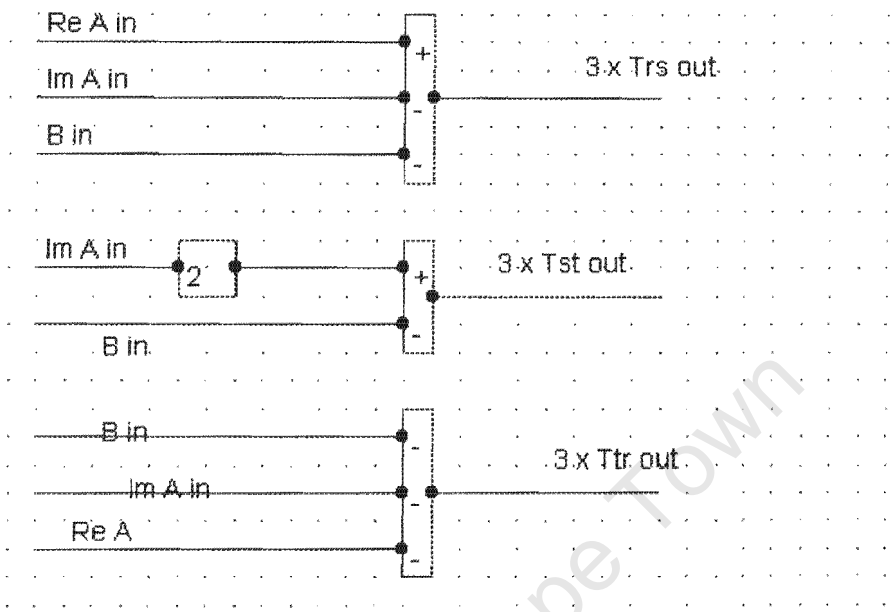


Figure 4.6

The final susceptance values came out as three times the required values and were normalized by three parallel 10k resistors in the output loops against one 10k for the input for the respective stages, giving a gains of 1/3.

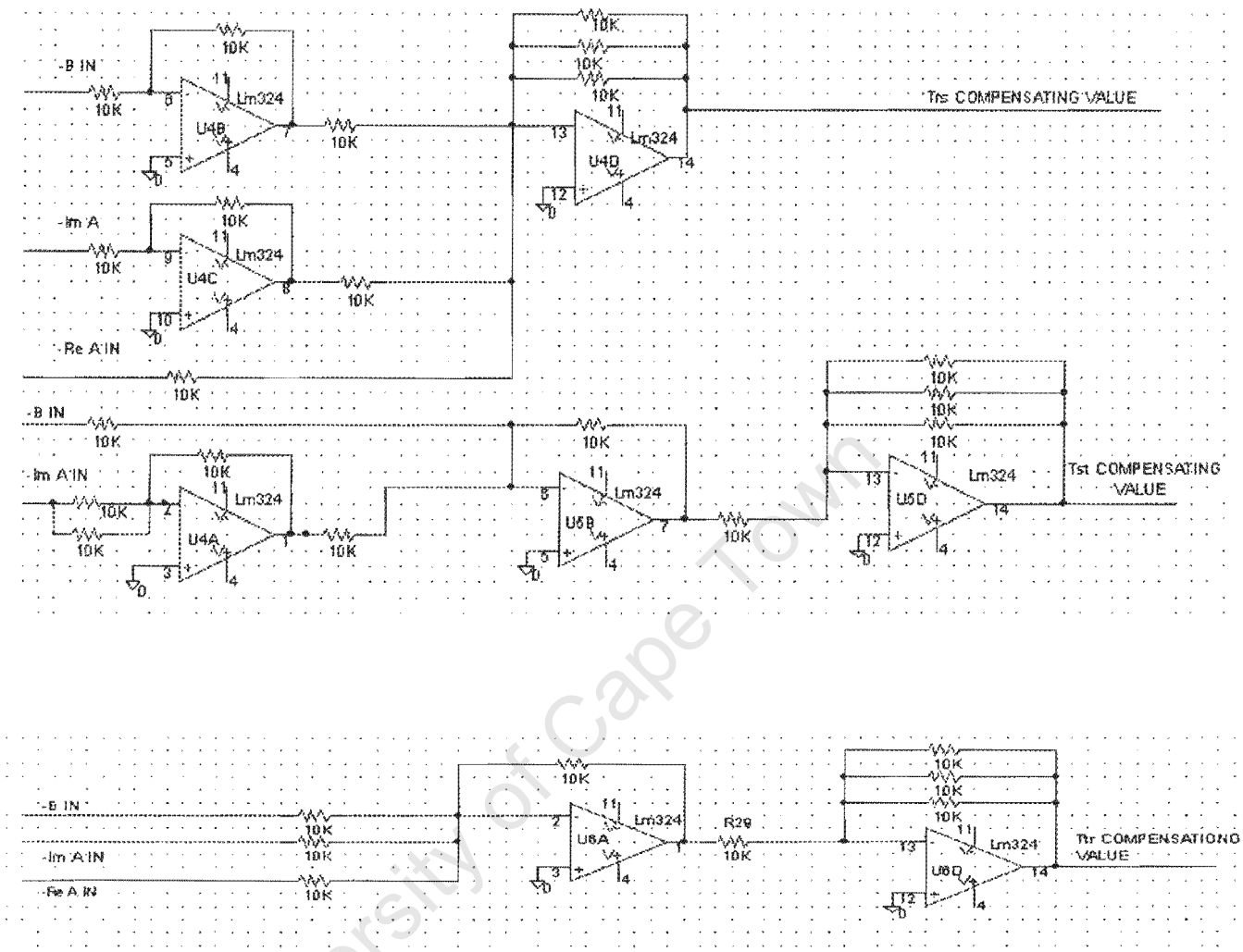


Figure 4.7

Schematic details for the dual admittance meters in figure 4.7.

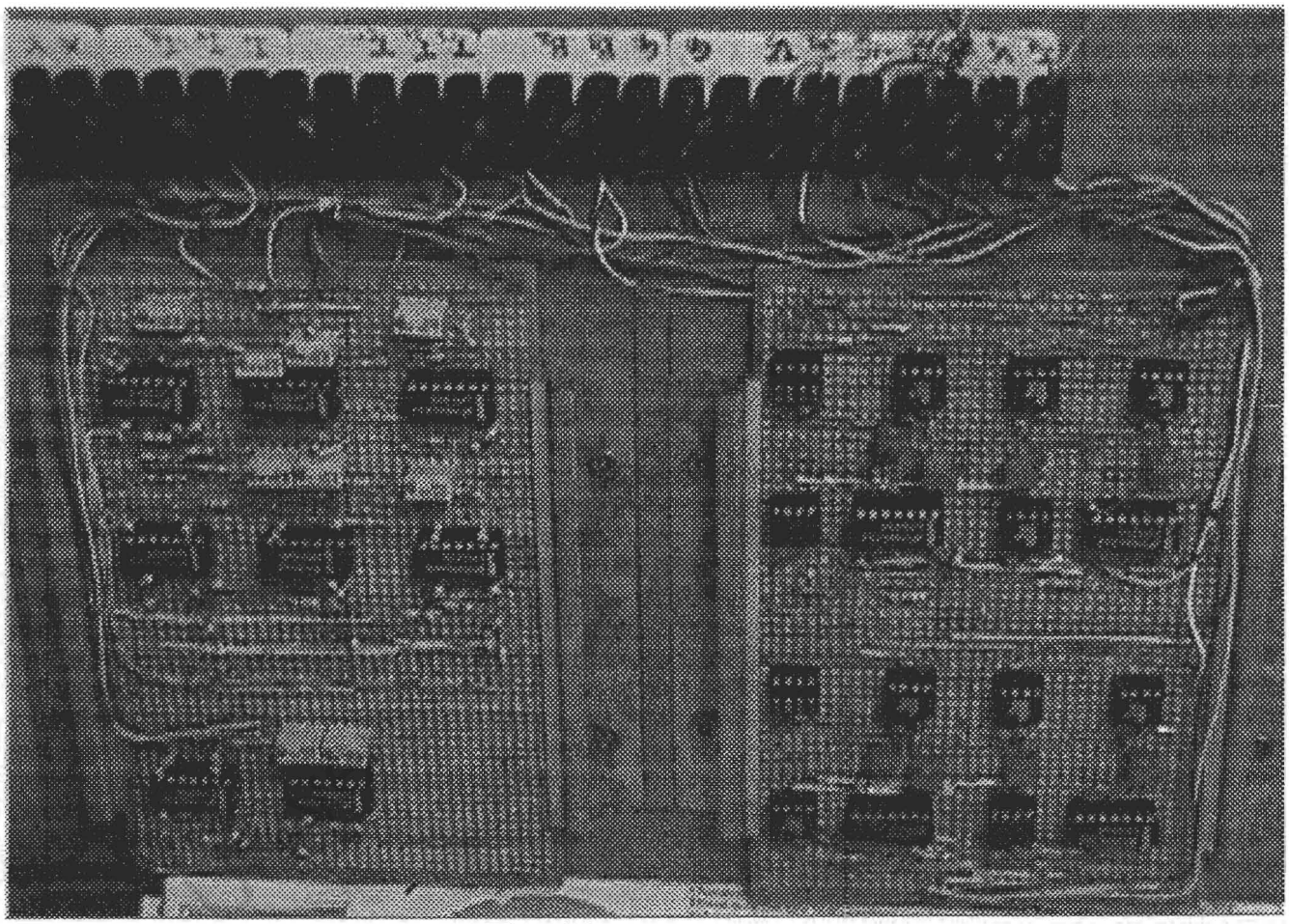


Plate 4.1

Plate 4.1 is the

Construction as was done on ordinary veroboard

4.3 Laboratory set-up and tests of compensator on loads

Once the admittance meters had been calibrated, the feeling was that moving to the laboratory for testing was just a formality; *fait acompli*. Not quite so. A series of problems, that had not been anticipated were encountered.

First of all the available inductors and capacitors had to be re-tested. The actual values of many capacitors were different from those indicated on the labels. One had to measure and label them again. The variable inductors had been labeled for maximum current rating without any indication of the voltages they operated comfortably with. While testing the inductors it was realized that increasing the operating currents in excess of 60% of the label ratings resulted in extreme humming. Without adequate experience with them it was felt safer to minimize the noise. So it was decided to operate at lower system voltages of 100 volts line-to-line. This meant that new voltage transducers had to be constructed. Currents could still be measured using the existing transducers.

A second problem with the supply voltages was that several of the available three-phase variacs were asymmetrical by more than 10%. They were to reduce the line-to-line voltages to the required 100 volts. It should be recalled that one of the requirements for this compensator system is the supply voltage symmetry. It also had to be sinusoidal. However, the latter attribute had to be dispensed with as experience has shown that UCT supply can never be sinusoidal. Besides, earlier tests with single-phase had yielded very good results with the same voltage waveform.

The issue of the voltage asymmetry was resolved by using two three-phase variacs. With six outputs available, the three of these that provided the best symmetry were selected.

Next a pure resistive unbalanced load was to be set up first. The meters would display the required compensator values. Since this was a semi-automated operation one would then compute the equivalent inductor or capacitor from the susceptance readings (at 50 Hz) and make a substitution in the appropriate branch. See section 3.5.4.

While this worked out easily in computer simulations in practice it posed a problem. The variable inductors had no indicators to show their values as one drew the plunger. On the other hand the capacitors that were clearly labeled could not be varied continuously. These problems were handled as follows.

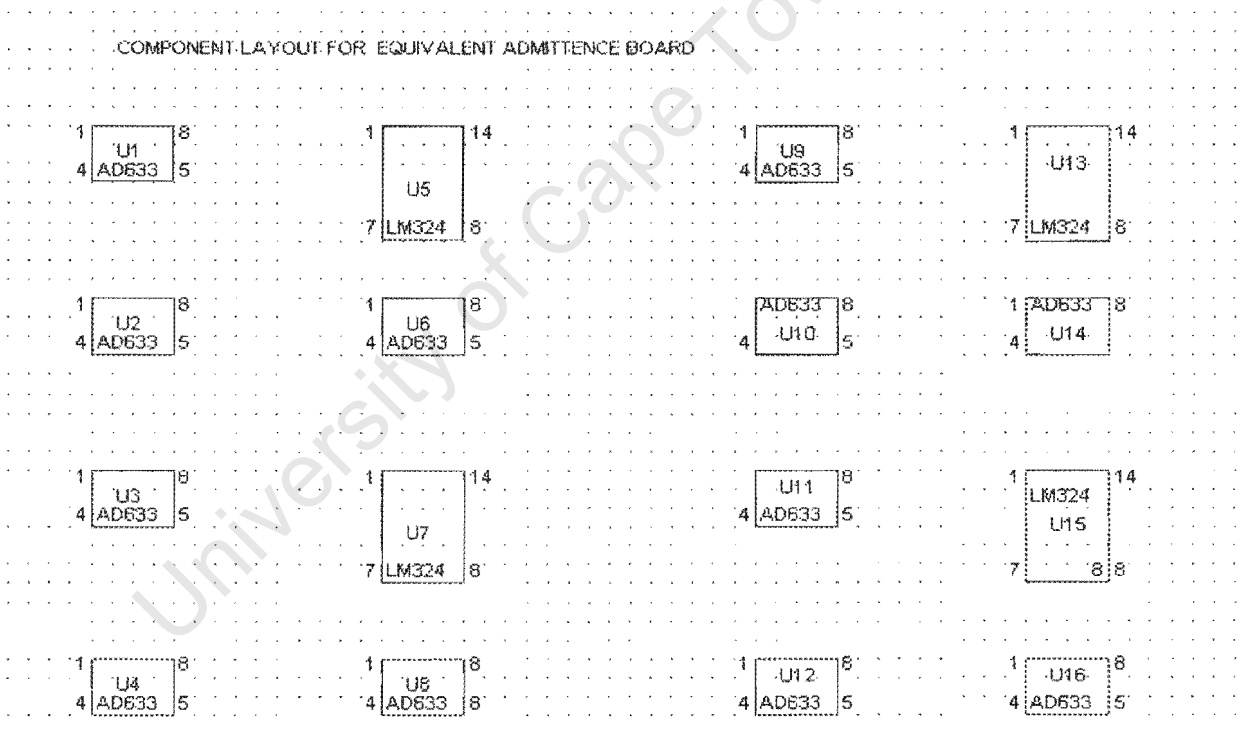


Figure 4.8

The component layout as was done on the veroboard

First, for the branches that required capacitive compensators, higher than the required values of capacitance were installed. Then a variable inductor would be

placed in parallel with the capacitor. The inductor would be varied to provide the necessary subtraction from the high capacitance. (See figure 4.8 for this illustration). A branch that required inductive compensation would be fitted with a variable inductor with a known range of operating currents and therefore a known range of inductive loading. Once these inductors were in place they would be varied systematically (almost simultaneously) until the meter compensator readings were close to nil. Capacitor switching complications were avoided by installing the capacitors while the mains supply was switched off.

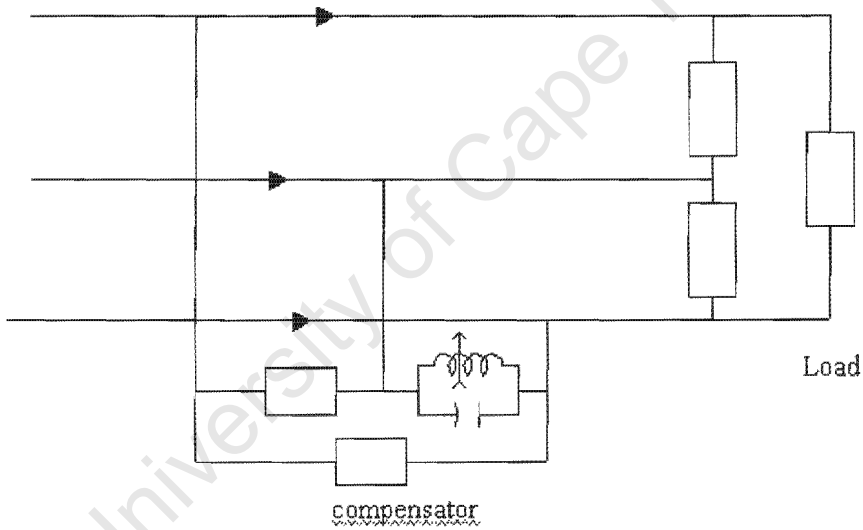


Figure 4.9

An illustration of how a compensator branch capacitance can be smoothly varied using a variable inductor connected in parallel

Prior to setting up the PCB installation, a fresh calibration problem was realized. To begin with, according to the data sheet for the division function of the AD633, the output picks up a multiplier factor of 10 from the function (see appendix 3). The dc supply was, 15, 0, -15volts for all the electronics. In order to avoid saturating the amplifiers all output peak values had to be kept below the ±15

volts. This meant that a restriction on the range of load parameters had to be imposed. Adjustment of transducer ratios within the same test may have solved the problem but could have introduced errors. So it was avoided.

Once the set up was finally rid of the hitches, balancing commenced as explained earlier. As expected the nil readings on the susceptance meters matched the moment of current balance and when the power factor was practically unity.

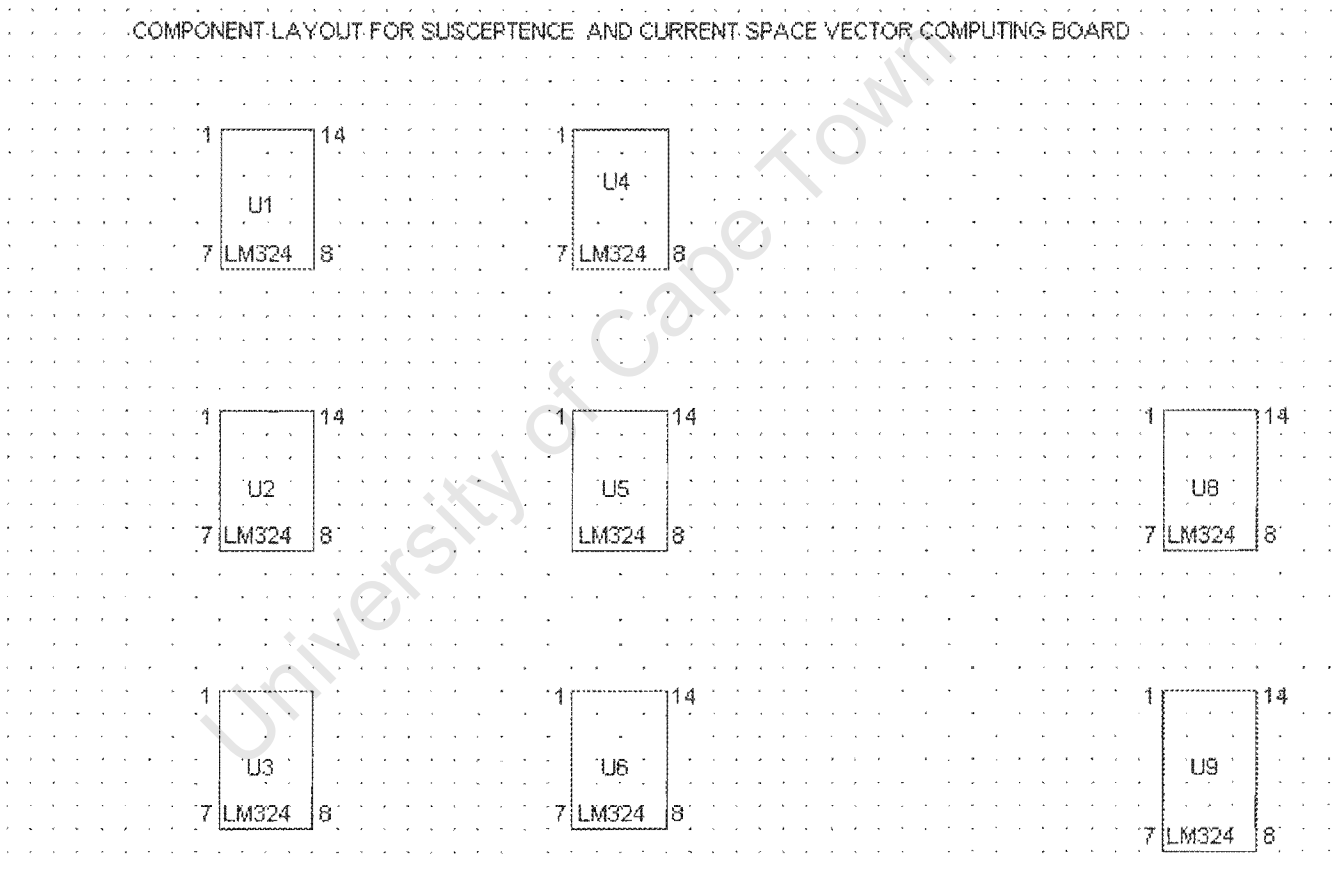


Figure 4.10

4.4 Production of the current space vector analysis circuitry

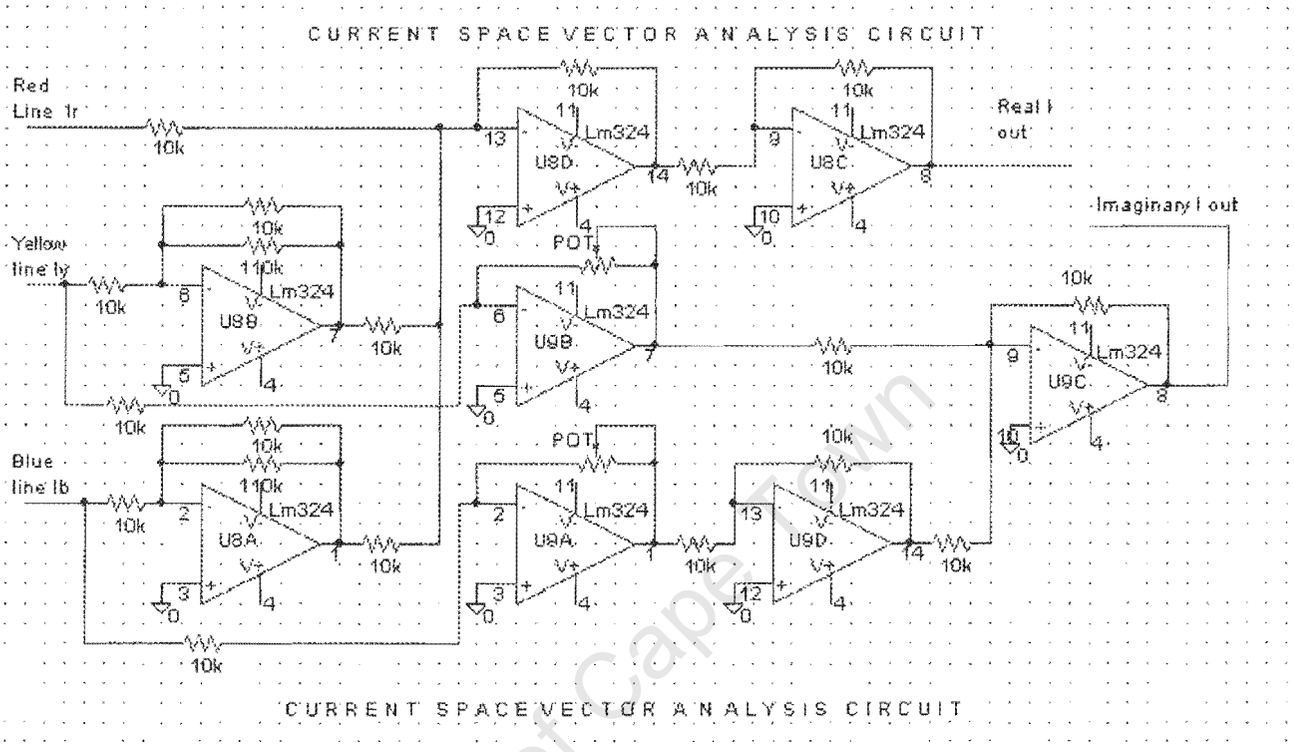


Figure 4.11

The three source currents, I_r, I_y and I_b are picked up by transducers. The transducers must be calibrated against each other.. Currents I_y and I_b are fed to U8B and U8A, respectively, whose gains are -1/2, each. They are then summed up together with I_r, at U8D. After an inversion through U8C the output is Re I, the real component vector of the three-phase current space vector.

The imaginary I is worked out by the I_y transducer output to U9B with a gain of -1.732 set by a trimmer, while I_b is fed to U9A. I_b undergoes one extra inversion through U9D, before they are both summed up by U9C.

Imaginary I, is plotted against real I using a scope in XY mode. The display is a circle when the line currents are balanced. This option was constructed and tested but was not actually deployed in the trials in section 4.3 as rms digital meter readings were used instead.

Conclusion

A practical demonstration has been carried out. Despite the few hitches, basically associated with the choice of analogue components, the results are consistent with those obtained in chapter 3.

5. The case of a single-phase supply for a three-phase load

5.1 Background

In Chapter 1 reference was been made to unplanned single-phase power distribution networks that the author has encountered in sub-Saharan Africa. With most of these economies currently in recession and having more urgently pressing needs such situations are not likely to be corrected soon. Under the circumstances there is bound to be a consumer wishing to operate some three-phase equipment from the only available single-phase supply.

A combination of purely reactive components is capable of converting a single-phase supply to three-phase. The values of the required compensator components are dependent on the parameters of a particular three-phase load. Therefore to be able to maintain a symmetrical three-phase supply, for a random or varying load, an instrument must be in place to monitor the parameters of the load.

The author therefore wished to briefly investigate if the newly designed admittance meter could make a contribution in solving this problem.

(**Equations 5.7 and 5.8 were derived by M. Malengret. The rest is the original work of the author except where it may be indicated otherwise*).

5.2 Evaluation of single-to-three-phase susceptance parameters

In figure 5.1 two admittances, Y_1 and Y_2 are in series. The current, I, flowing through them is given by

$$I = V_1 Y_1 = V_2 Y_2 \qquad (5.1)$$

Where, V_1 and V_2 are the potential drops across the respective admittances.
If one wishes to have a phase shift of 120° between V_1 and V_2 then one can use the operator **a** to denote the phase shift and solve the following equations.

$\mathbf{a}V_2 = V_1$ (where **a** = Exp(j120°) = -1/2(1 -j$\sqrt{3}$))

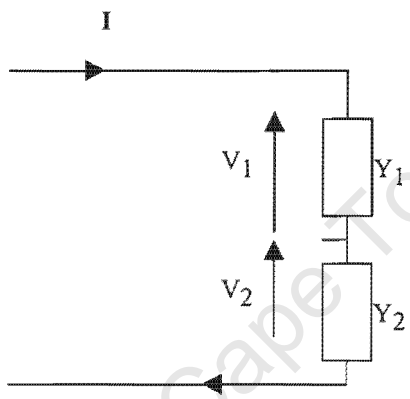


Figure 5.1
Two admittances in series

Therefore equation 5.1 becomes

$$\mathbf{I = V_1Y_1 = a\,V_1Y_2} \qquad (5.2)$$

Canceling the V_1's

$\mathbf{Y_1 = aY_2}$.

$\mathbf{Y = G + jB}$ (where G is the conductance and B is the susceptance)

So,

$G_1 + jB_1 = \mathbf{a}(G_2 + jB_2) = (-1/2+j\sqrt{3}/2)(G_2 + jB_2)$

$$= \tfrac{1}{2}(-G_2 - jB_2 + j\sqrt{3}G_2 - \sqrt{3}B_2) \quad (5.3)$$

Equating real and imaginary values

$$G_1 = 1/2(-G_2 - \sqrt{3}B_2) \quad (5.4)$$

$$B_2 = -(2G_1 + G_2)/\sqrt{3} \quad (5.5)$$

$$B_1 = 1/2(\sqrt{3}G_2 - B_2) \quad (5.6)$$

And substituting B_2

$$B_1 = 1/2(\sqrt{3}G_2 - (-2G_1 - G_2)/\sqrt{3}) = 1/2(3G_2 + 2G_1 + G_2)/\sqrt{3})$$

$$\mathbf{B_1 = (2G_2 + G_1)/\sqrt{3}} \quad (5.7)$$

$$\mathbf{B_2 = -(2G_1 + G_2)/\sqrt{3}} \quad (5.8)$$

From equations (5.7) and (5.8), it follows that the susceptances required for V_1 and V_2 to be 120° apart are exclusively dependent on the respective load conductances. The above expressions for B_1 and B_2 are the necessary and sufficient conditions.

In the next assignment tests are made using an admittance-measuring module (designed and constructed earlier) to measure the admittance of a load.

An initial demo uses the modules in figure 5.2.

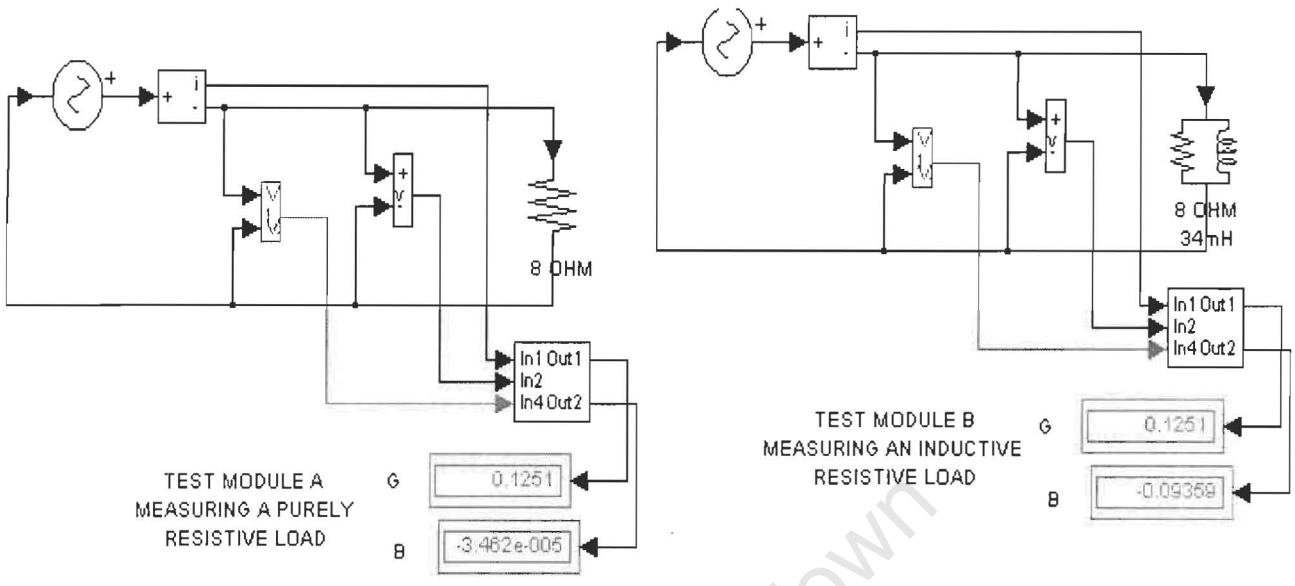


Figure 5.2

Two susceptance measurement modules

Test module A gives an output conductance, G, of 0.125 and a negligible (or spurious) value for B, the susceptance. Module B, gives a conductance of 0.125 and a susceptance of -0.09359. These are both in agreement with the given load values.

A simple series branch and an admittance meter, (similar to figure 5.1), are set up to measure the two branch admittances and compute the compensator susceptances to give the 120° shift between V_1 and V_2. When compensation is accomplished, the original single-phase voltage source will also be mutually shifted by 120° from each of V_1 and V_2 and a symmetrical three-phase voltage source will be created. See figures 5.3 and 5.4. Figures 5.5 and 5.6 show the voltage waveforms before and after compensation respectively.

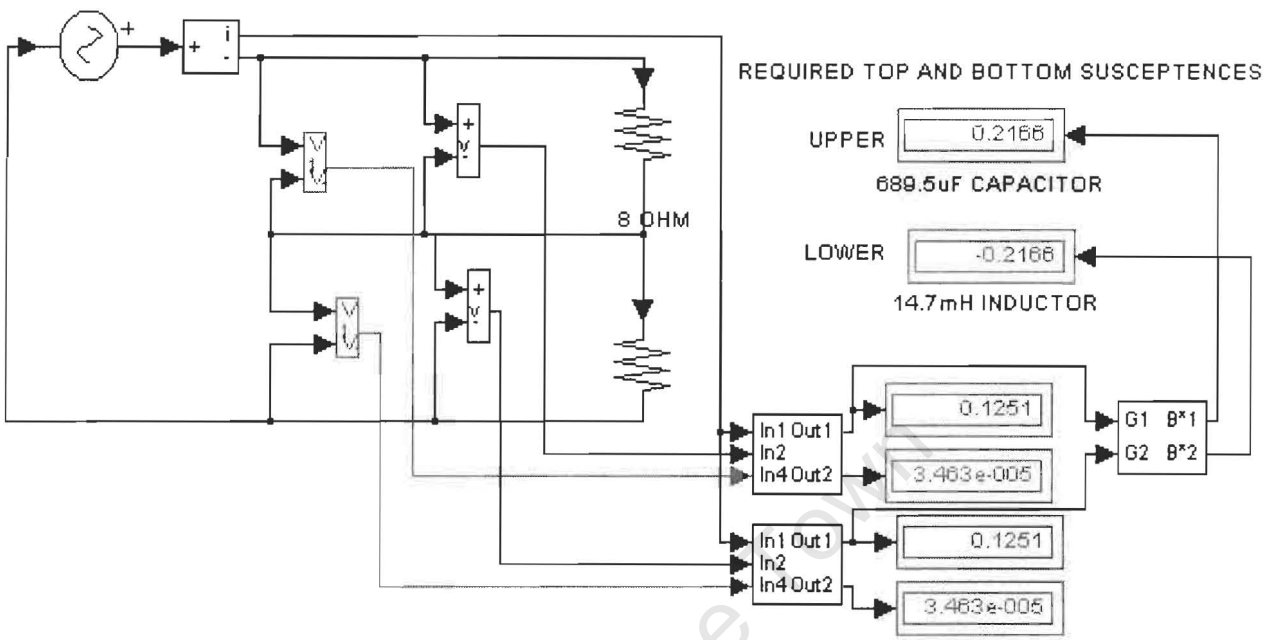


Figure 5.3

Computing susceptances for a resistive load.

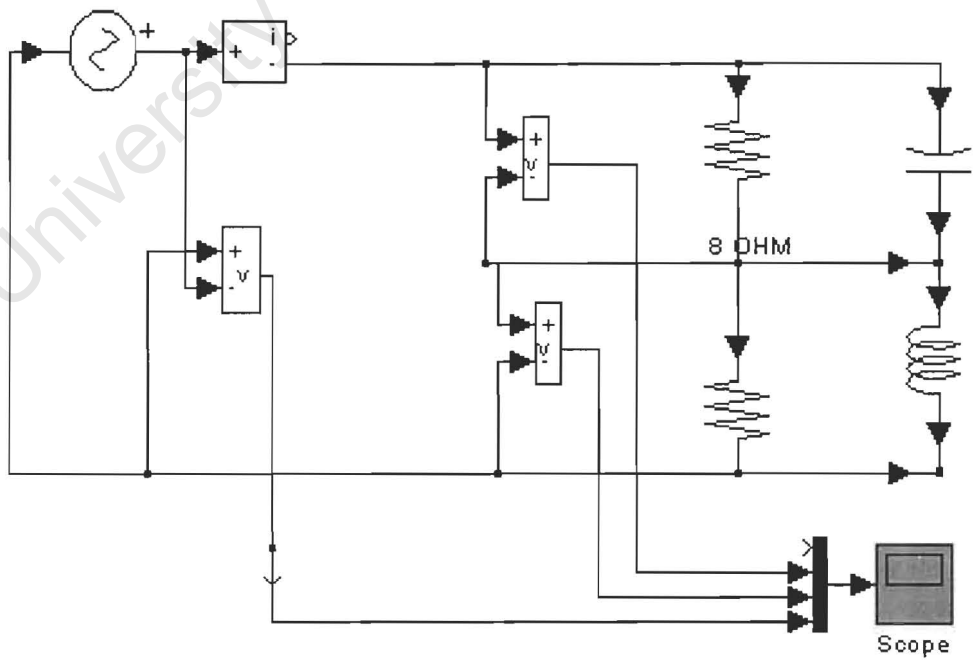


Figure 5.4

After the installation of a compensator

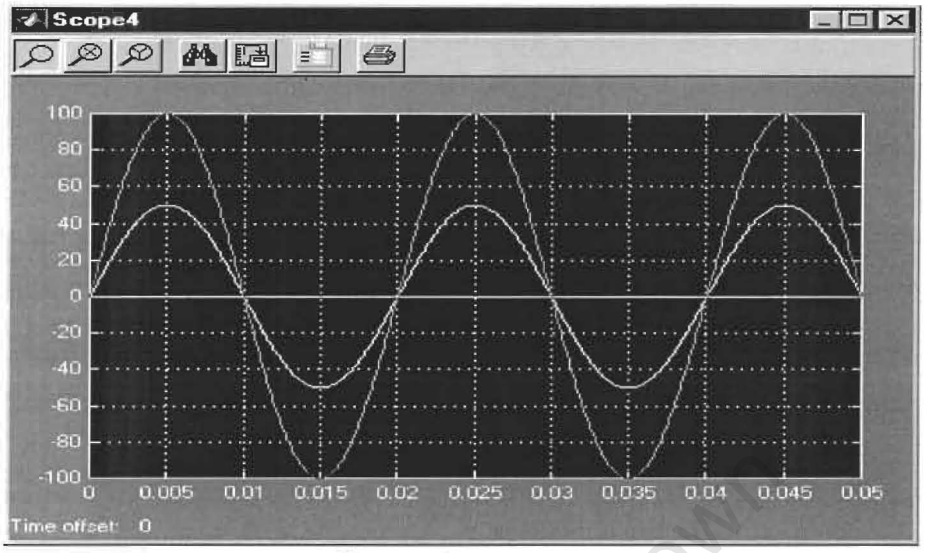


Figure 5.5

Voltage waveforms before compensation; all are in phase (V1 and V2 are overlapping)

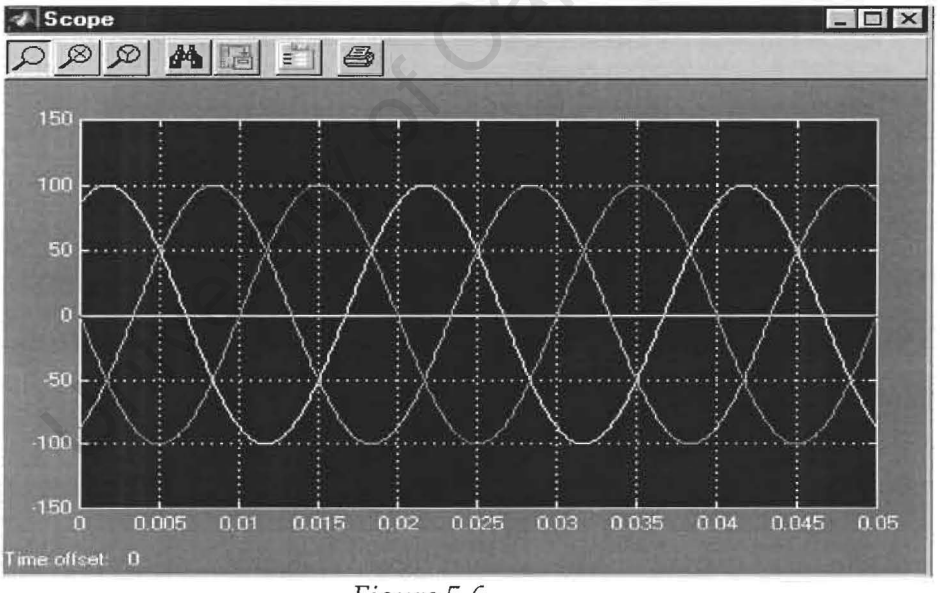


Figure 5.6

The voltage waveforms after installation of the compensator

In the first instance G_1 and G_2 were computed using the supply single-phase line current. After introducing the compensator components, the new admittance meter reading for G_2 was wrong!!

This was due to an oversight. A new current I_2 from the compensator junction flowing through R_2 was overlooked (see figure 5.7). So the actual current flowing through R_2 is the sum of I_1, from the top resistor R_1 and I_2 from the compensator junction. As illustrated in figure 5.7 this correction gives the right conductance value of resistor R_2.

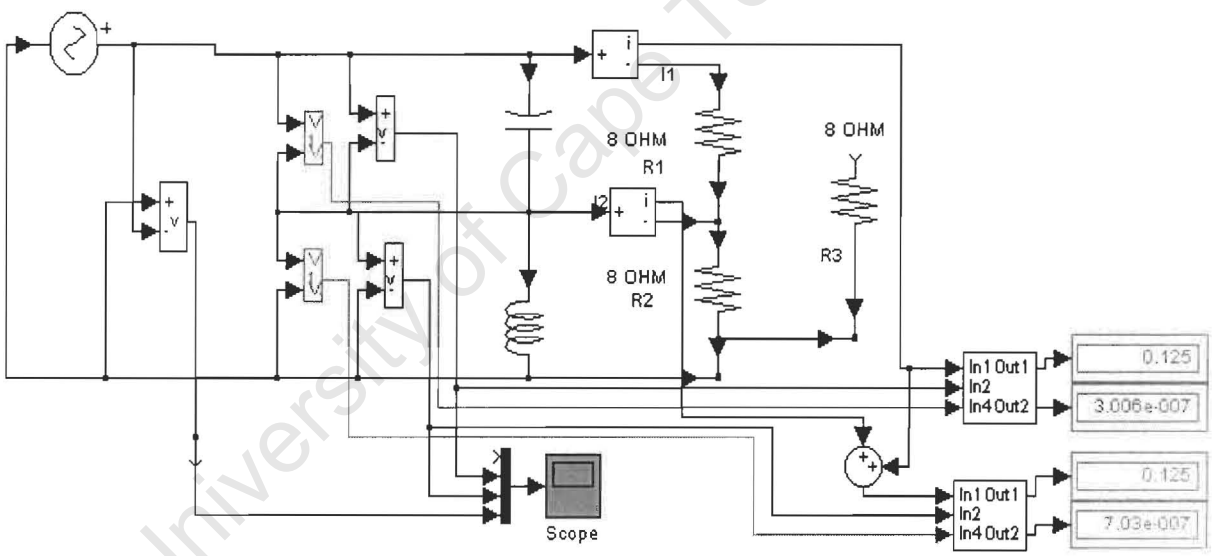


Figure 5.7.

Computing susceptances by incorporating a new current I_2 from the compensator junction.

Having sorted out the computation of R_2, a back resistor, R_3, is added to simulate a delta load. Note that to simulate a normal random delta one must ultimately consider the combination of R_1, R_2, and R3 as unknown (a black-box),

with the three wires into the box as the only access. For simplicity a balanced resistive load will be considered first.

5.3 A balanced resistive delta load

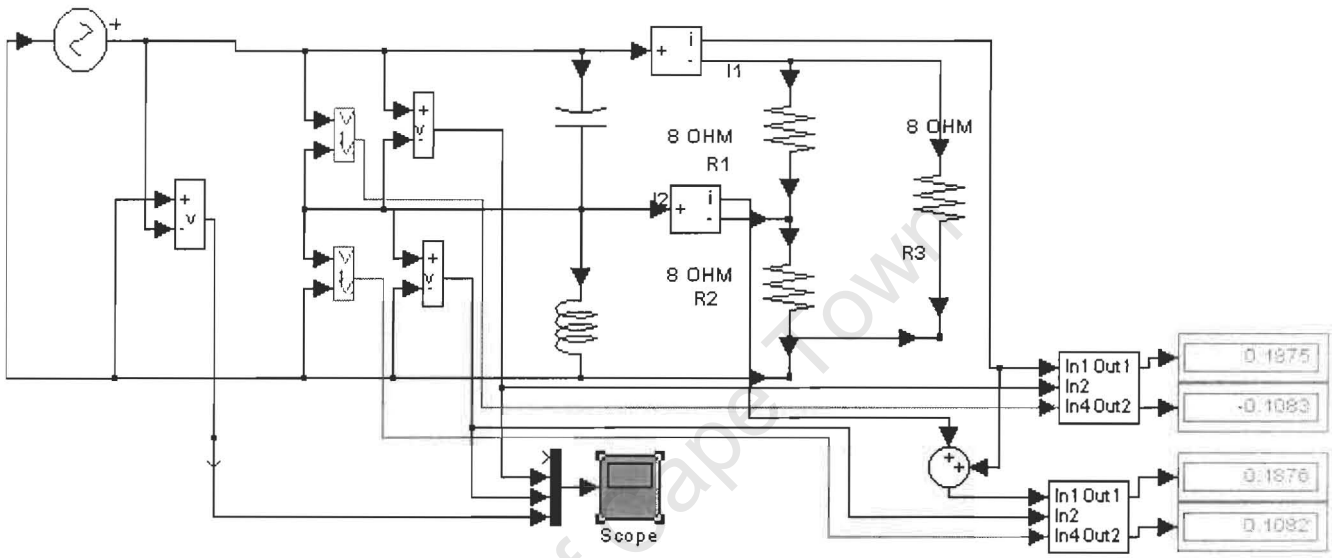


Figure 5.8

Admittance measurement of a balanced resistive load

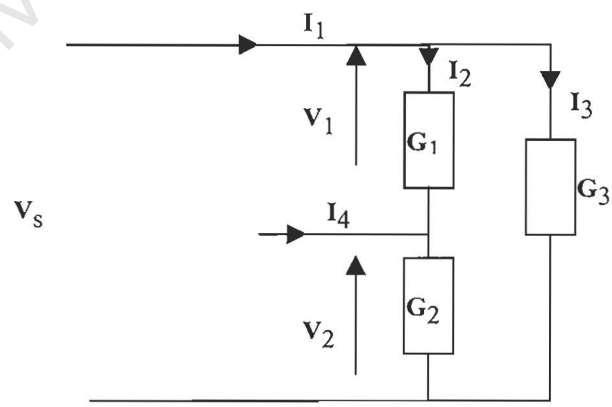


Figure 5.9

Figure 5.9 is a balanced resistive load. V_s is the single-phase supply, and V_1 and V_2 are the compensator-derived voltages.

$$I_1 = I_2 + I_3 \tag{5.9}$$

$$I_2 = V_1 G_1 = V_1 G \text{ (since all three conductances are equal)} \tag{5.10}$$

$$I_3 = V_s G = (V_1 + V_2)G \tag{5.11}$$

Dividing I_3 by I_2

$$I_3/I_2 = (V_1 + V_2)/V_1 \tag{5.12}$$

$$I_3 = I_2 (V_1 + V_2)/V_1$$

$$I_1 = I_2 + I_3 = I_2 + I_2 (V_1 + V_2)/V_1 = I_2 (2V_1 + V_2) / V_1$$

$$\mathbf{I_2 = I_1 V_1/(2V_1 + V_2)} \tag{5.13}$$

Equation 5.13 is important because in a practical situation, I_1 will be accessible but I_2 and I_3 will not. With this equation the values of I_2 and I_3 can be determined by measuring I_1 alone, and the two voltages, $V_1$and V_2.
So by measuring two currents, (I_1 and I_4) and two voltages, (V_1 and V_2) the required compensator susceptances can be computed. This is familiar ground.

It has been observed that once a compensator achieves voltage symmetry with the "front conductances," G_1 and G_2, any changes in the value of the "back" conductance G_3 will not alter this symmetry.

5.4 Achieving voltage symmetry for a balanced complex load

Refer to equation 5.13. It was derived using a purely resistive load. However there are no resistance parameters in the final equation. It should therefore be reasonable to assume that the same expression would hold for a complex balanced load.

In order to verify the above assumption a balanced complex load was set up. A simulation was run. Then the compensator readings from the admittance meter were substituted in. Surprisingly, voltage symmetry was no achieved on the next run!

What had previously been dealt were purely resistive loads. Although the expressions, in equations 5.7 and 5.8, for computing the necessary compensating susceptances require only G's, (the load conductance values), the final compensator values are inclusive of all previously existing susceptances. These must be subtracted before the correct compensator values can be realized. So one must take into account the existing load and compensator susceptances. These are the values of the B's as read on the admittance measurement instruments.

5.5 Voltage symmetry for a general unbalanced load

This is the situation of a "black box" where one's only access is the three input wires and the most convenient model to use is the delta, with none of the three branches known. It is a complicated case and several ideas were considered to determine uniquely the relationships of the three individual branch admittances.

First, consider a random delta network in figure 5.10. There are three different pairs of inputs. The admittance of the network as measured from each one of the pairs is unique. It should then be possible to generate three simultaneous equations to solve the equivalent individual branch admittances, Y_1, Y_2 and Y_3.

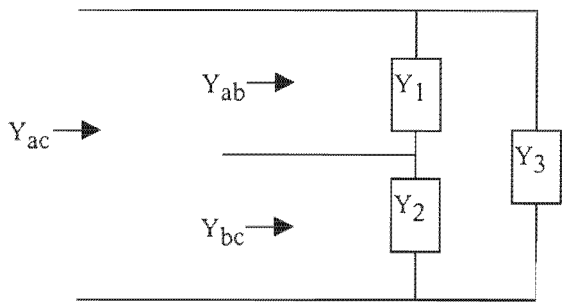


Figure 5.10

A black box delta load

Y_{ab} = (Y_1 in parallel with a series combination of Y_2 and Y_3)

$$= Y_1 + (Y_2\, Y_3) / (Y_2 + Y_3) \tag{5.14}$$

$$Y_{bc} = Y_2 + (Y_1\, Y_3) / (Y_1 + Y_3) \tag{5.15}$$

$$Y_{ac} = Y_3 + (Y_1\, Y_2) / (Y_1 + Y_2) \tag{5.16}$$

Y_{ab}, Y_{bc} and Y_{ac} can be measured. So the above equations were fed into a computer for the solutions of Y_1, Y_2, Y_3 in terms of Y_{ab}, Y_{bc} and Y_{ac}. Each value of Y_1, Y_2 and Y_3 yielded six solutions, on twenty-six A4 size pages! The solution was difficult to interpret into practical circuitry and so it was shelved. Despite

that apparent setback, it was an important landmark. This was proof that a real solution does exist. The way out then was perhaps a change of tactics.

A table of measurements for the impedances with and without the back admittance, Y_3, was drawn up. The first observation was that the readings of both susceptance and conductance were different when Y_3 was connected and when it was not. Even for purely resistive loads susceptance measurements were observed. It had been hoped that observing a good amount of data would reveal some useful patterns. See table 5.1 in appendix 3.
Examination of this data did not reveal anything useful; at least not immediately. Nonetheless it was not discarded, especially in the absence of much else.

Next, a purely resistive delta was revisited.

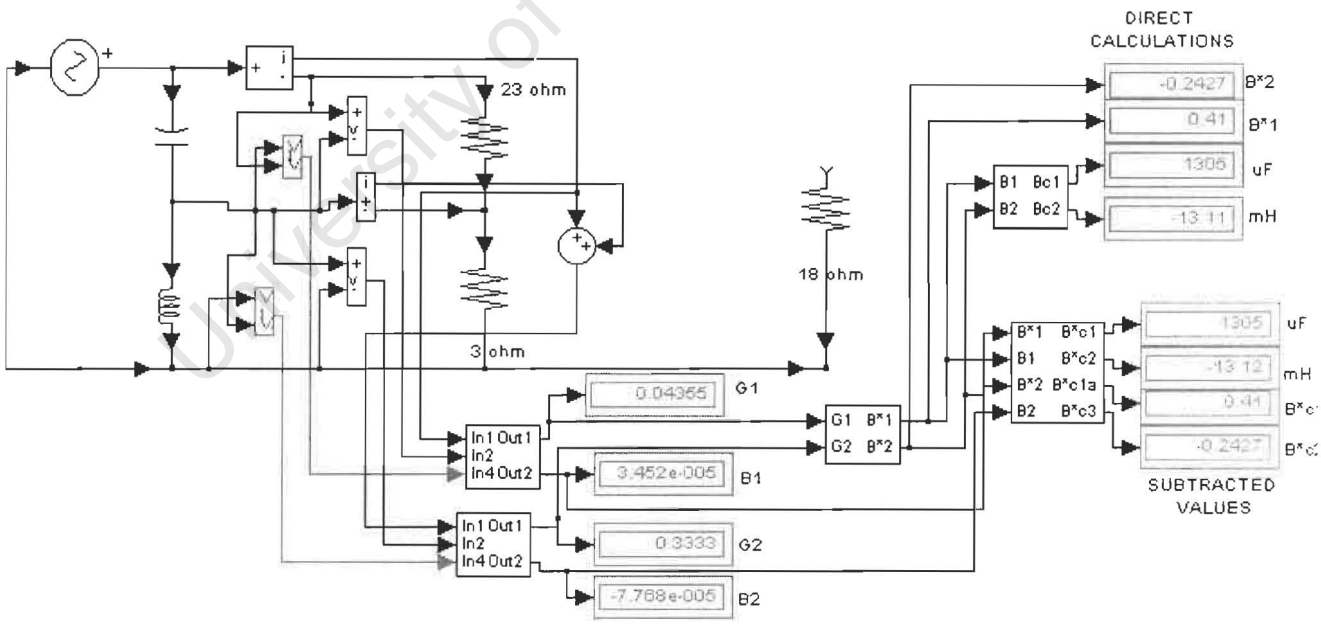


Figure 5.11

In the figure 5.11 the back resistor, R_3, is disconnected and the meter readings for G_1, B_1, G_2 and B_2 are the exact values of the load branch admittances.

The "direct calculations" are those compensating susceptances that are worked out from G_1 and G_2 (using equations 5.7 and 5.8) without considering the values of any previously existing capacitance or inductance in the system as opposed to the "subtracted susceptances".

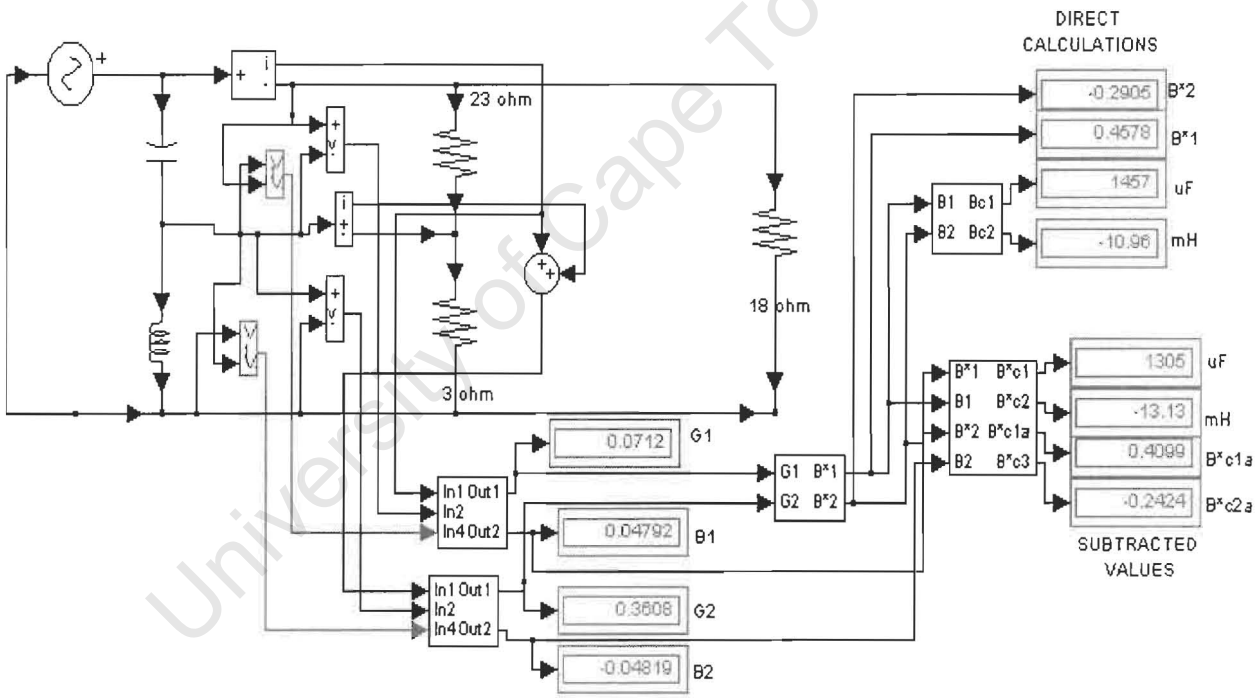


Figure 5.12

In figure 5.12 the back resistor has been reconnected. The values of G_1, G_2, are suddenly different and so are the "directly worked out " susceptances. It has been pointed out that the introduction or change of back admittances does not affect the existing voltage symmetry and the required compensating values. So

the "worked out values" couldn't be right since the network had attained voltage symmetry with the previous values. Besides, further simulation had verified voltage symmetry after the reconnection of the back resistor without any compensator changes.

Next observation was that although the load branches were pure resistances, the connection of the back resistor introduced imaginary readings (B_1 and B_2) and also changed the values for G_1 and G_2. The purpose of using pure resistances in this example was particularly to highlight this point.

Finally when one looks at the output of the "subtracted values" meters, one notices that they do not change. These figures are worked out using the new values of G_1, G_2, B_1 and B_2. When the value of R_3 was changed it was observed that the G's and B's changed but the compensating values as displayed by the "subtracted values" meters still remained the same and the voltages remained symmetrical without any compensator changes.

$B^*c_1 = B^*_1 - B_1$ (where B^*c_1 is the final value suitable for compensation. B^*_1 is the value calculated from G_1 and G_2 (using equations 5.7 and 5.8). B_1 is the susceptance value read on the admittance meter).
Likewise $B^*c_2 = B^*_2 - B_2$

From the above observations there is strong suggestion that the technique of deriving fictitious network admittances by measuring two currents and two voltages fully describes the unique behavior of any individual random three-wire 'black box', provided that the three-phase voltages are symmetrical.

5.6 Starting with random compensator values

In a normal situation one expects that the status of the compensator will be at some random point when a new load is connected. The three-phase voltage will also be asymmetrical. This means that the values of the relative phase angles and amplitudes of V_1 and V_2 will be random.

Czarnecki's [11] concept of fictitious load admittance measurement assumes that the supply voltages are symmetrical. Since the purpose of this exercise is to achieve symmetry for the same voltages, one is faced with a dilemma.
The proverbial *chicken-and-egg* scenario. So the next step was just a hunch!

A simulation was setup, with random values of load admittances and compensating susceptances, similar to the situation described above.

The first run was made and meter readings for compensator susceptances were taken. These susceptance values were then substituted back to replace the previously existing compensator values. A fresh simulation was run and the same process repeated. After several rounds it was observed that the meter susceptance readings were converging and the waveforms of the voltages were progressively getting symmetrical.

This was a solution!!
A feedback system could be installed from the output of the compensator susceptance computer to control variable compensator elements. This would systematically lead to more accurate admittances readings until the voltages would be finally symmetrical.
Further semi-automated simulations using the technique were successfully carried out. It was observed that with practice one gets very skilled.

When voltage symmetry is achieved the conductance and susceptance readings on the admittance meters will be the true fictitious values of the unknown delta network. **This is analogous to Czarnecki's [11] but not quite the same.** So this author now defines a new term, **two-branch electrical equivalent of a delta network.**

Figure 5.31 illustrates the concept of a two-branch equivalent of a delta load.

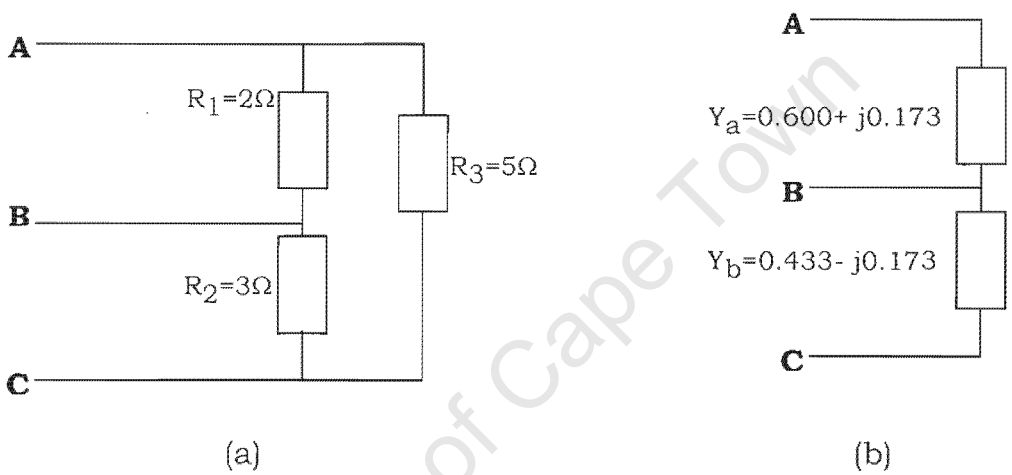


Figure 5.13

A *two-branch network equivalent to a delta*

The above two networks are a purely resistive delta and a two-branch complex pair. They should draw exactly the same line currents from a symmetrical three-phase voltage source, according to earlier observations. Note that the Y's are complex admittances and their currents are dependent on supply frequency. They are linear and as long as a sinusoidal supply is assumed there should be no problem.

So it would appear sufficient to describe a three-wire "black box" network by specifying its electrical characteristics in terms of a two-branch equivalent

network. This is fundamentally important because in order to derive equations 5.7 and 5.8, for the compensator for single-to-three-phase voltage conversion, a two-branch series model (figure 5.1) was used. If these same equations are to be the basis for attaining voltage symmetry with any random network, that network must be interpretable as a two-branch series network.

To verify the above assertions, simulations were set up, and current measurements were taken for each of the above loads (figure 5.13(a) and (b)).

First, a test was done using a three-phase voltage supply derived from a single-phase source. The waveforms obtained, in figure 5.14, show that the line currents in each case were identical.

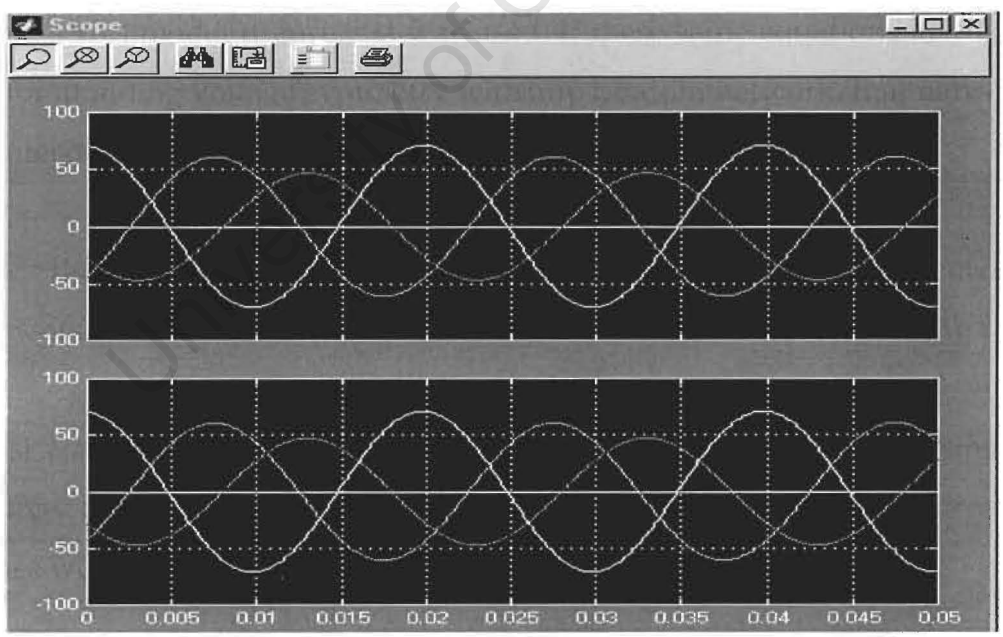


Figure 5.14

Scope comparisons of line currents obtained when the networks in figure 5.13 were fed with a three-phase supply derived from a single-phase source

Then the same networks were connected to a normal symmetrical three-phase mains supply and the following results in figure 5.15 were obtained.

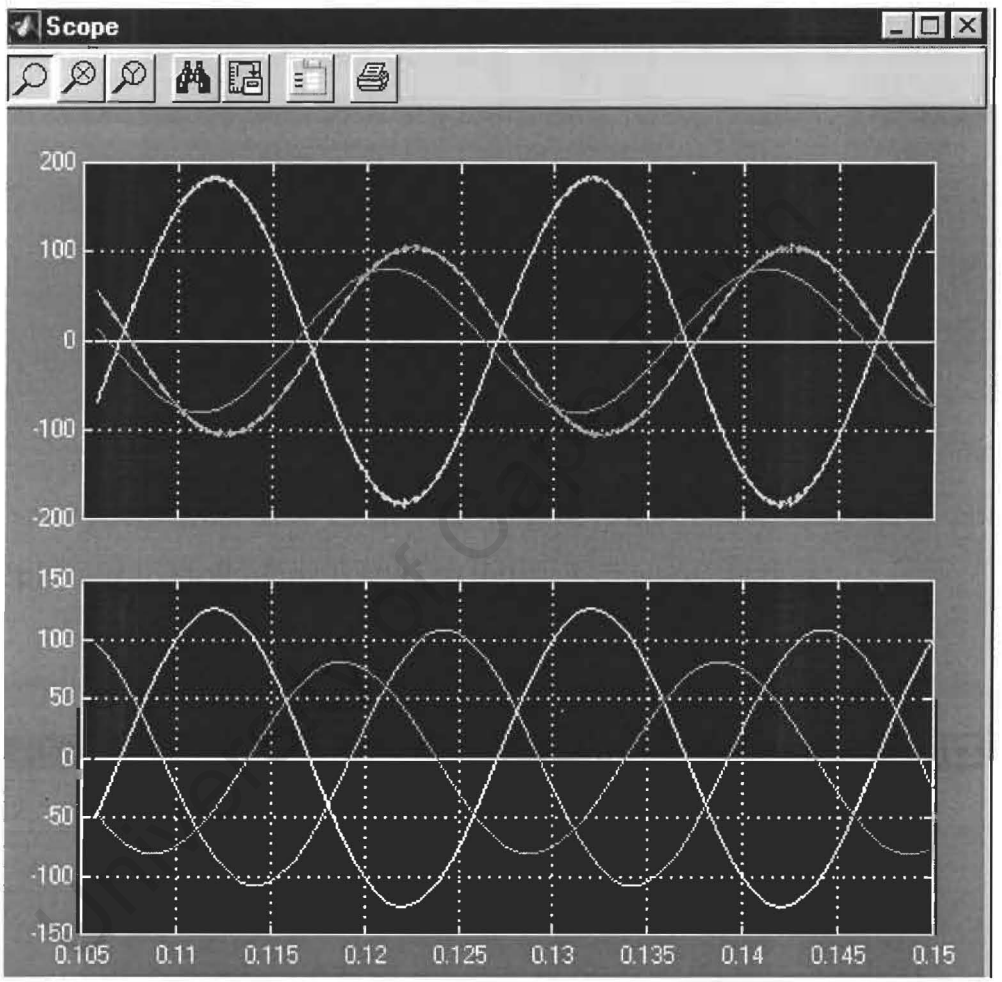


Figure 5.15

The above waveforms were line currents obtained from the networks in figure 5.13 fed with normal three-phase mains supply.

This was a disappointing result!

Looking at figure 5.15, not only are the relative phase angles different, the amplitudes in either case don't seem to have any remote bearing to those in the adjacent network.

It looked like a dead end and abandoning the whole concept of equivalent admittance was contemplated. However, out of some irrational hunch, the mains supply phase sequence was swapped (from positive to negative sequence) and the results as can be seen in figure 5.16 below were amazing! The delta load, operated from a normal positive sequence, produced exactly identical currents, (in opposing sequence notwithstanding) as the two-branch network on negative sequence supply.

A close examination of the three-phase supply derived from the single-phase source showed that the phase sequence was indeed negative.

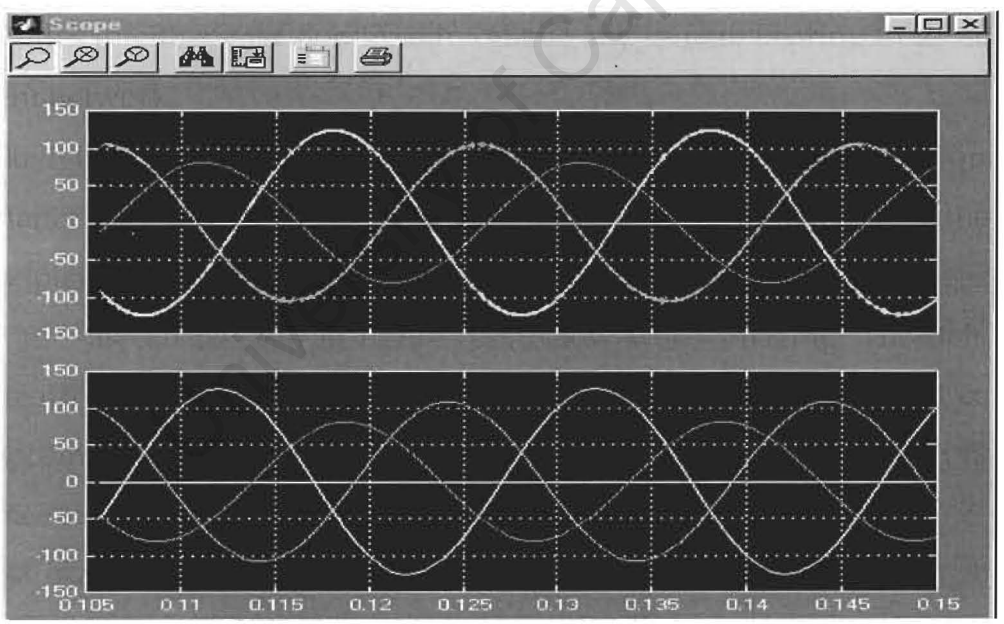


Figure 5.16

These were the waveforms when the two-branch network was run with negative sequence three-phase supply while the resistive delta remained on the positive sequence supply.

It would appear from the above observations that the equivalent two-branch of a delta network is valid for a specific, supply voltage phase sequence.

Using the results above, the relationships of the admittances of the two networks can be derived, by equating the currents in the respective phases using a symmetrical and sinusoidal supply.

5.7 Derivation of a two-branch network equivalent to a delta network

Equations 5.7 and 5.8 were derived using a series two-branch network. So in order for us to apply them to a general three-phase load we must be able to interpret a delta network as a two-branch series one.

Let a delta network connected to a symmetrical and sinusoidal three wire three-phase voltage supply draw line currents, I_R, I_Y and I_B. If a two-branch network connected to the same supply and draws equal line currents it should be said to have an impedance equivalent to the delta network (at least under those circumstances.)

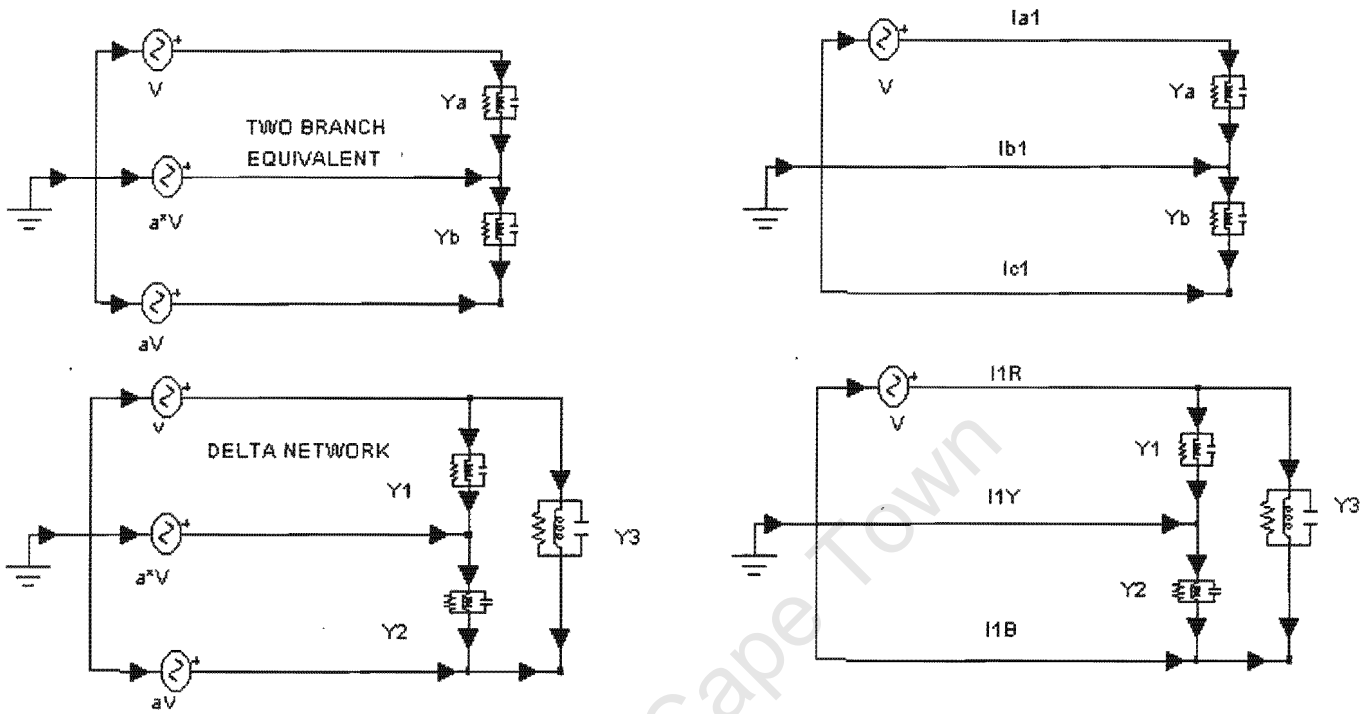


Figure 5.17

Using superposition method

Consider the schematics above, the delta and its two-branch equivalent. Y_1, Y_2 and Y_3 are the delta branch admittances and Y_a and Y_b are their equivalent two-branch admittances. The adjacent single voltage schematics assist to illustrate the superposition method to be used ahead to work out the line currents.

I_{a1}, I_{b1}, and I_{c1} denote the line currents in the two-branch network due to the reference line-to-neutral voltage, V, (acting alone). I_{1R}, I_{1Y} and I_{1B}, are the delta network line currents as a result of V. Likewise the currents that are due to the second line-to-neutral voltage, a^2V, are, I_{a2}, I_{b2}, I_{c2} and I_{2R}, I_{2Y}, I_{2B} for the two

branch and delta respectively. Finally, I_{a3}, I_{b3}, I_{c3} and I_{3R}, I_{3Y}, I_{3B} are due to the third line-to-neutral voltage, **a**V, in their respective networks.

So the actual line currents are the sums of the individually computed currents.

For the two-branch

$I_{a1} = VY_a$, $I_{b1} = -VY_a$ and $I_{c1} = 0$

$I_{a2} = -\mathbf{a}^2VY_a$, $I_{b2} = \mathbf{a}^2V(Y_a + Y_b)$ $Ic_2 = -\mathbf{a}^2VY_b$ (where **a**, and $\mathbf{a}^2$ are the usual 120° and 240° operators respectively)

$I_{a3} = 0$ $I_{b3} = -\mathbf{a}VY_b$ $I_{c3} = \mathbf{a}VY_b$

The total line currents for the two-branch network are:

$$I_a = I_{a1} + I_{a2} + I_{a3} = V(Y_a - \mathbf{a}^2Y_a) \quad (5.17)$$

$$I_b = I_{b1} + I_{b2} + I_{b3} = V(-Y_a + \mathbf{a}^2Y_a + \mathbf{a}^2Y_b - \mathbf{a}Y_b) \quad (5.18)$$

$$I_c = I_{c1} + I_{c2} + I_{c3} = V(\mathbf{a}Y_b - \mathbf{a}^2Y_b) \quad (5.19)$$

For the delta

$I_{1R} = V(Y_3 + Y_1)$; $I_{1Y} = -VY_1$; $I_{1B} = -VY_3$

$I_{2R} = -a^2Y_1$; $I2Y = a^2V(Y_1 + Y_2)$; $I_{2B} = -a^2VY_2$

$I_{3R} = -aVY_3$; $I3Y = -aVY_2$; $I_{3B} = aV(Y_2 + Y_3)$

The total line currents for the delta are

$$I_R = V(Y_3 + Y_1) - aVY_1 - a^2VY_3 \tag{5.20}$$

$$I_Y = -VY_1 + a^2V(Y_1 + Y_2) - aVY_2 \tag{5.21}$$

$$I_B = -VY_3 - a^2VY_2 + aV(Y_2 + Y_3) \tag{5.22}$$

Equating the line currents for both networks

$I_R = I_a$

$$V(Ya - a^2Y_a) = V(Y_1 + Y_3) - a^2VY_1 - aVY_3 \tag{5.23}$$

Canceling the V's

$Y_a = (Y_3 + Y_1 - a^2Y_1 - aY_3)/(1 - a^2)$

$$\mathbf{Y_a = 1/2((2Y_1 + Y_3) - j\sqrt{3}Y_3)} \tag{5.24}$$

$I_B = I_C$

$$VY_b(a - a^2) = -VY_3 - a^2VY_2 + aV(Y_2 + Y_3)$$

$$Y_b = (-Y_3 - a^2Y_2 + a(Y_2 + Y_3))/(a - a^2)$$

$$\mathbf{Y_b = 1/2((2Y_2 + Y_3) + j\sqrt{3}Y_3)} \qquad (5.25)$$

Equations, 5.24 and 5.25 for Y_a and Y_b, clearly indicate the relationship between the delta network and its equivalent two-branch for a symmetrical and sinusoidal three-phase supply. Computer simulations give exactly the same results when numerical values are substituted in.

When the back admittance, Y_3, is complex, its conductance and susceptance will contribute to both the equivalent conductance and susceptance (due the action of the j in the equation), as indicated in the following expressions.

$$Y_3 = G_3 + jB_3$$

$$\mathbf{Y_a} = Y_1 + 1/2(Y_3 - j\sqrt{3}Y_3) = Y_1 + 1/2(G_3 + jB_3 - j\sqrt{3}(G_3 + jB_3)$$

$$\mathbf{Y_a = 1/2(2G_1 + G_3 + \sqrt{3}B_3 + j(2B_1 + B_3 - \sqrt{3}G_3))} \qquad (5.26)$$

Likewise,

$$\mathbf{Y_b = 1/2(2G_2 + G_3 - \sqrt{3}B_3 + j(2B_2 + B_3 + \sqrt{3}G_3))} \qquad (5.27)$$

$ReY_a = 1/2(2G_1 + G_3 + \sqrt{3}B_3)$ and $ReY_b = 1/2(2G_2 + G_3 - \sqrt{3}B_3)$ will be the equivalent conductances, while $ImY_a = 1/2(2B_1 + B_3 - \sqrt{3}G_3)$ and

$ImY_b = (2B_2 + B_3 + \sqrt{3}G_3)$ will be the equivalent susceptences.

Note: It is important to remember that the equations for Y_a and Y_b were derived using a symmetrical three-phase supply, in positive sequence. Presently, the sequence for the 3-phase voltage derived from the single-phase supply is negative. The polarities for ImY_a and $Im\ Y_b$ must therefore be swapped to get the correct results for such a case.

The problem of the phase sequence mix-up came about when V_2 was let to be equal to aV_1, in equation (5.2), instead of $a^2 V_1$. So equations 5.7 and 5.8 were derived in conformity with this order. Normal positive sequence is 0°, 240°, 120°. If this oversight had been noted initially then the polarities for the equations for generating B_1 and B_2 would have been reversed. This was however a fortunate mistake as it has accidentally led to the discovery that for **each random delta load there are two sets of compensator susceptance values capable of achieving voltage symmetry from a single-phase supply.**

Let $a^2 V_1 = V_2$

and B_{11} and B_{22} represent the new compensator susceptances in the positions of B_1 and B_2. Using the method for deriving equations 5.7 and 5.8, it can be shown that

$$B_{11} = -(2G_2 + G_1)/\sqrt{3} \qquad (5.28)$$

$$B_{22} = (2G_1 + G_2)/\sqrt{3} \qquad (5.29)$$

Equations (5.28) and (5.29) give the compensator susceptance values for positive sequence single-to-three-phase conversion.

The magnitudes of B_{11} and B_{22} remain the same as B_1 and B_2 respectively but the polarities change. In terms of capacitor and inductor values, however, a big difference will be noticed. Moreover, since the actual final compensating values must take into account the existing load susceptances then the final result becomes significantly different.

For example, if the same resistive delta network of R_1=2ohm, R_2=3ohm and R_3 = 5ohm, is used then the following compensating figures will be displayed on the compensator meter.

For negative sequence

B_{c1} = 0.6737, or 2144uF

B_{c2} = -0.77, or 4.1mH at 50Hz.

For positive sequence

B_{c11} = -0.6737, or 4.7mH

B_{c22} = 0.77, or 2450uF at 50Hz.

Simulations have verified that both these sets of parameters will give voltage symmetry for the same load but with opposing phase rotation.

5.8 A geometric solution to the general case with unbalanced complex loads

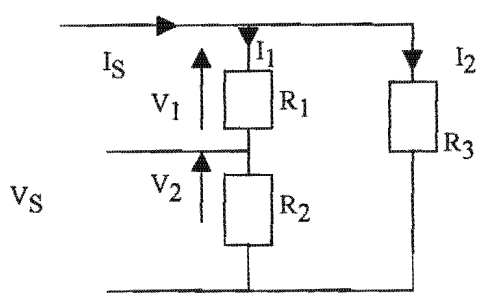


Figure 5.18

The problem up to this moment is that the method of double-voltage-double-current is designed for symmetrical three-phase voltage systems. The admittance meters give outputs by assuming that the (unmeasured) third voltage is equal to the other two in amplitude and mutually at 120°.

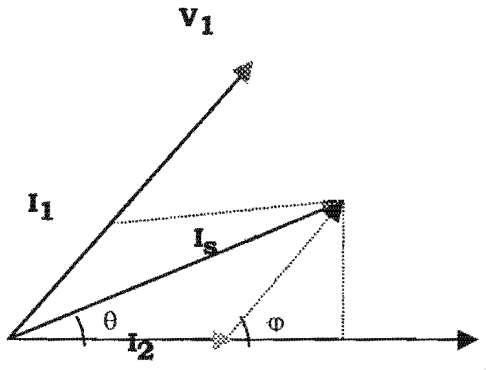


Figure 5.19

In practice, for the case of single-to-three-phase conversion, none of the voltages is predictable. Before attaining voltage symmetry, one has no choice but to measure all three voltages, if the answer must be obtained in one operation. The only consideration that saves one from absolutely requiring this condition is the fact that, ultimately, V_1 and V_2 originate from the single-phase source, Vs, and their sum must always be equal to V_s. In this case one has a choice of either measuring V_s or improvising an extra summing function for V_1 and V_2.

In the case of a purely resistive delta load, in figure 5.18, the line current, I_s, is the sum of two currents, I_1, which is now assumed to be in phase with V_1, and I_2, in phase with the source voltage (the single-phase voltage supply). If we take the single-phase supply, V_s, as the reference then construction of a phasor

parallelogram should show the magnitudes of the respective current components.

From figure 5.19

Let θ be the phase angle between the supply voltage, V_S, and the source current, I_S, and φ be the phase angle between Vs and the front branch current I_1.

Then

$$I_S \sin\theta = I_1 \sin\varphi \qquad (5.30)$$

With instruments, cosineθ and cosineφ can be measured from the ratio of apparent power and real power.

$$\text{Cos}\theta = (I_S \bullet V_S)/(\|V_S\| \|I_S\|) \qquad (5.31)$$

$$\text{Cos}\varphi = (I_1 \bullet V_S)/(\|I_1\| \|V_S\|) = (V_1 \bullet V_S)/(\|V_1\| \|V_S\|) \qquad (5.32)$$

Using the identity

$$\text{Cos}^2\theta + \sin^2\theta = 1$$

Therefore

$$I_1 = I_S \sqrt{(1 - \text{Cos}^2\theta)} / \sqrt{(1 - \cos^2\varphi)} \qquad (5.33)$$

This should solve any random purely resistive network. It should also give a practical solution to a predominantly resistive load.

Testing equation 5.33 by simulation

Equation 5.33 was put to test by simulation and problems were encountered. To begin with the model for working out the cosine of the phase angle between I_S and V_S gave an answer greater than 1! The sequence of functions had to be changed around before a sensible answer could be yielded as is illustrated in figure 5.20.

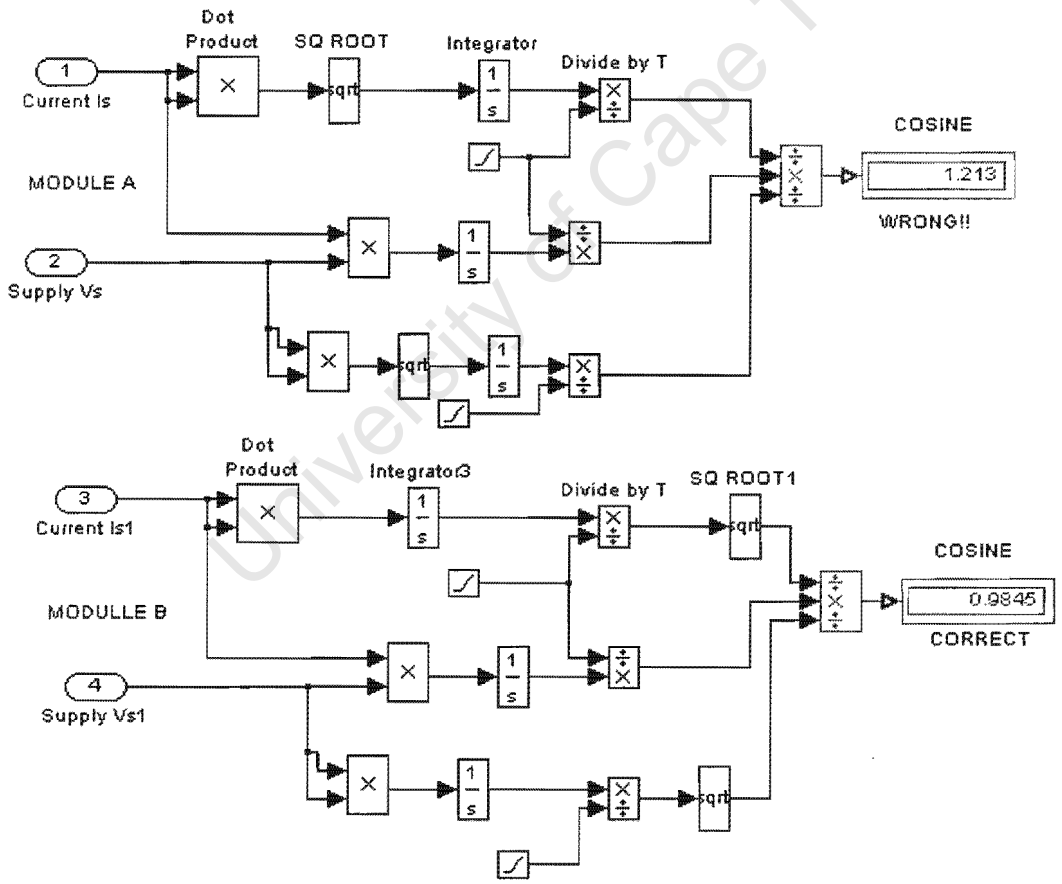


Figure 5.20

Power factor computing module

The dot product of a number with itself is equal to the square of its modulus (the norm) [12].

$\mathbf{a} \cdot \mathbf{a} = \|a\|^2$ and $\mathbf{a} \cdot \mathbf{b} = \|a\|\|b\|\cos\theta$. The modules in figure 5.20 were configured to execute these functions but the sequence of the functions surprisingly made a big difference. It took a while to figure out the working combination.

Secondly, the assumption that the load currents were a sum of the current in phase with the supply voltage, V_s and that in phase with V_1 was verified to be only partially correct. The back branch current was in phase with Vs, but the balance of the current was not wholly in phase with V_1. Closer analysis of these currents will be necessary before one can confidently split the load current.

5.9 Design and construction of an analog single-to-three-phase susceptance computer

The function of the susceptance computer is to take the admittance meter readings, G_1, B_1, G_2 and B_2 and compute the required compensator values.

$B_{c1} = ((2G_2 + G_1)/\sqrt{3}) - B_1)$

$B_{c2} = (-(2G_1 + G_2)/\sqrt{3}) - B_2)$ (where B_{c1} and B_{c2} are the top and bottom compensator elements respectively)

The block diagram in figure 5.21 illustrates the above expressions.

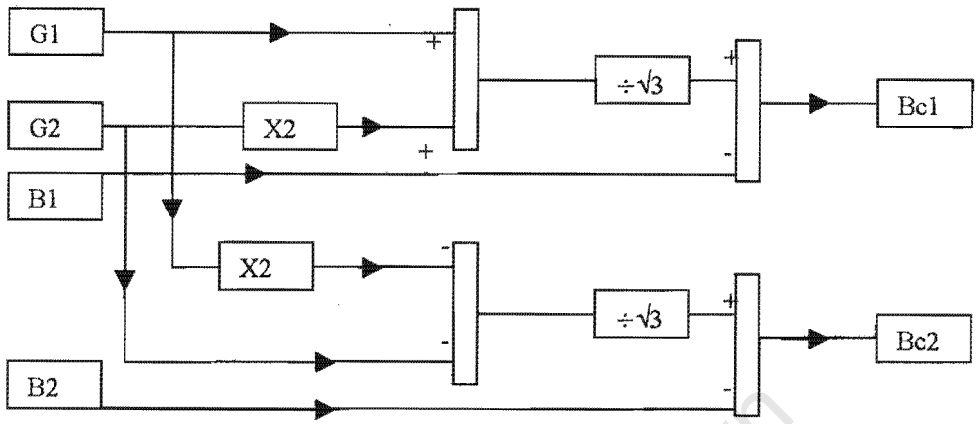


Figure 5. 21

Susceptance computer block diagram

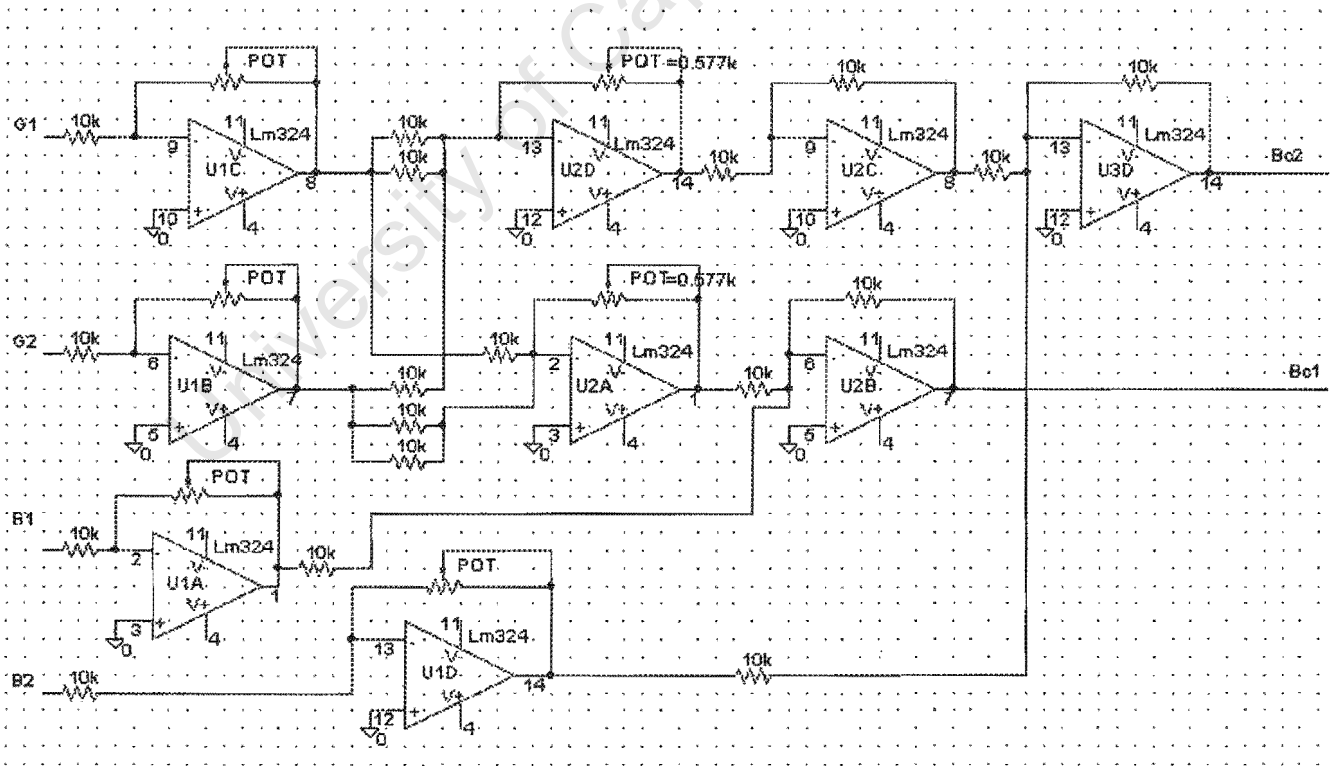


Figure 5.22

Schematic for susceptance computer

The same LM324 quad amplifiers used in chapter 4 in were used in this exercise. The author also continued with the same technique of using one resistor type, 10k, except, of course, where trimmers were required for calibration.
Four measured values of conductances and susceptances, G_1, G_2, B_1 and B_2 from the admittance meters are received by U_1. Using trimmer pots, they are calibrated and set to the correct polarities. Please refer to figures, 5.21 and 5.22.

G_1 goes through two parallel 10k resistors (for the gain of 2) to the input of U2D where it is summed up together with G_2 through a 10k resistor and U2D is set to a gain of 0.577, which is $1/\sqrt{3}$. So U2D executes the function $(2G_1+G_2)/\sqrt{3})$. This function then goes through inversion by U2C when it is joined by B_2 at the summing input of U3D, which executes a subtraction and outputs $B_{c2} = (-(2G_1+G_2)/\sqrt{3})-B_2$. This is the lower arm of the compensator.
G_2 goes through two parallel 10k resistors to the summing input of U2A, which, together with G_1 and a gain of 0.577, U2A executes $-(2G_2 + G_1)/\sqrt{3}$.
This is joined by B_1 at the summing input of U2B giving, $B_{c1} = ((2G_2 + G_1)/\sqrt{3}) - B_1$ as the output.

Note that the polarities for the values of B_{c1} and B_{c2} may be interchanged to reverse the voltage sequences, if required. This can also be achieved the traditional way by swapping the leads.

5.10 Calibration procedure of the overall susceptance measurement System

Refer to figure 5.9 and equations 5.24 and 5.25. Measurement of a purely resistive delta network in the configuration of figure 3.8 will give two sets of admittances,

$Y_a = (Y_1 + ½Y_3) + j3⁄2(Y_3)$

$Y_b = (Y_2 + ½Y_3) + j3⁄2(Y_3)$.

Using these facts a purely resistive delta load is set up, connected on a symmetrical 3-phase supply at any desirable or convenient voltage. The currents through each of the three resistive load branches are measured as well as the voltages across them. Their conductances are computed as accurately as possible. Using equations 5.24 and 5.25, the real and imaginary values for Y_a and Y_b are worked out. Once these are obtained then the constructed board can be calibrated to match these results.

5.11 Conclusion

Miller [9] has suggested that it is practically useful **if one can attach some predictability to the type of load for which compensation is required.** If the load has negligible reactance then it might be practical to consider it resistive. Should one expect the load to be balanced then, equation 5.13, will definitely be the correct choice.

A large majority of loads that require a three-phase supply in a single-phase situation are bound to be motors and therefore inherently balanced. It is quite

easy to construct a dedicated three-phase wiring and leave the single-phase loads on separate sockets.

Bearing the above in mind the author strongly recommends the new admittance meter in conjunction with equation 5.13 as a reliable practical solution for a fully automated control of a symmetrical three-phase supply from a single-phase source.

Epilogue

This thesis discusses the subject of load compensation, ranging from historical to contemporary angles. From a practical perspective the method proposed by Czarnecki [11] has been extensively explored, first through computer simulations and finally physically realized by designing, constructing and testing an analogue module on a variety of linear loads. The results were positive and strongly support the conclusions arrived at by Czarnecki.

This compensator has inherent flexibility enabling a low budget installation. The admittance measuring and susceptance computer could be constructed as one portable unit, able to supervise several compensator banks. A semi-automated switching mode for a bank of reactive compensator components would be most viable in a large number of unsophisticated load distribution situations that this author has frequently encountered in various African countries. In this case a chart for converting susceptances to capacitances or inductances would be posted next to the installation or even included as a function on the instrument display, to assist the maintenance engineer looking after the installation. This would both cut down on installation costs necessary for fully automated options and also avoid the inevitable harmonic pollution that accompanies thyristor-controlled systems which are currently the most viable.

In chapter 3 (computer simulations), the author devised a technique for the control of a current source as a compensator element, in section 3.5.5. This is worth revisiting. A phase and amplitude controlled signal drives a current source. This results in a compensator current at right angles to the line-to-line voltage. The rms value of the current is equal to the product of the computed dc

compensator susceptance value and the line-to-line voltage. The load is compensated without any reactive components! Because of the orthogonality of the compensator current to the line-to-line voltage, a real switching device should (in principle) dissipate a negligible amount of power. It is the submission of the author that a pulse width modulation control design (or other appropriate technique) using similar logic should physically realize the same result as obtained in the simulation. This could result in a tremendous response time.

The space vector method of analysis proved to be a very handy and reliable index for both unbalance and power factor.

The analogue multiplier functions, AD633, have major design limitations. For example, the divider function comes with a factor of 10, (see appendix 3). This means that one has to make sure that for each set of current and voltage measurements, the current does not exceed the voltage, in order to avoid amplifier saturation. At the same time the current and voltage transducers must have the same reduction ratios so that the computed compensator susceptances don't require extra scaling. The available voltage transducers could only be constructed for specific voltages, with very small tolerances. This made them unversatile and uneconomical.

The author suggests that instead of searching for better performing analogue functions, further work should abandon analogue circuitry altogether and proceed with programmable digital signal processor (DSP) functions. Even then, note should be taken of the above issues.

Despite the shortcomings, the results of the analogue networks were amazingly accurate, especially, considering the extent of distortion one encounters on the UCT mains supply.

In his proposal, Czarnecki [11] commits a couple of pages on specifications for the compensator reactor bank. This author opted to disregard that emphasis, during the laboratory trials, as it is geared towards full automation; a notion, as already explained, not considered of priority to the targeted consumers. The range of required susceptances should instead be worked out imperically by simulating the extent of expected load conditions and reading the results from an admittance meter.

In the case of single-to-three-phase compensation, equation 5.13, ($I_2 = I_1 V_1/(2V_1 + V_2)$), has been derived by the author. In conjunction with the newly designed admittance meter, it should provide a basis for the reliable control and maintenance of a symmetrical three-phase supply from a single-phase source, for any complex balanced load.
It is also the belief of the author that the line of argument advanced in section 5.4 for the solution of a single-to-three-phase voltage control for a general complex and unbalanced load could yield an answer if re-examined more critically.

The literature review points to the extent that the subject of load compensation has been explored over the years. The coverage is by no means exhaustive. The author is therefore conscious of the possibility that some discoveries made here, that may have appeared new, could have been made before. The effort made here was to follow standard investigative procedure, make observations, draw some conclusions and then recommendations.

For the author it has been a great learning experience. Facing the issues first hand was challenging. Having had a spell of twenty years in the industrial environment around Africa, this topic proved thoroughly relevant to contemporary industrial issues. It has certainly been a great eye opener.
It is hoped that someone may find this thesis equally enriching.

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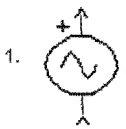
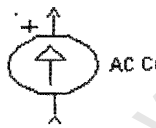
Appendix 1

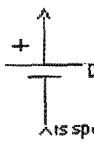
Computer simulation tools

1. 

Is specified in amplitude, frequency and phase .

2. 

Is specified in amplitude, phase, and frequency

3 

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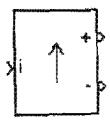
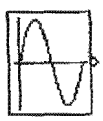
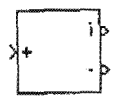
4. 

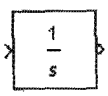
Controlled current source
Initial current specified

5. 

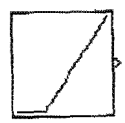
Sine Wave
Generator

6. 

Current Measurement

7. 

Integrator

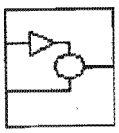
8. 

Simulates time

Ramp

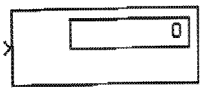
Appendix 1

Computer simulation tools

9. 

SubSystem

Helps combine sets of functions in a block

10 

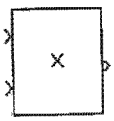
Numerical Display

11 

MUX or multiplexer

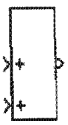
12. 

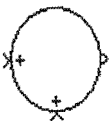
Gain -boosts a signal by a specified amount

13 

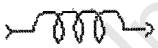
Provides for multiplication and/ or divisio of signals

Product

14. 

Sum 

summation of several signals

15 

Inductor

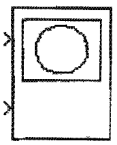
16 

Resistor

Appendix 1

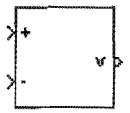
Computer simulation tools

16.



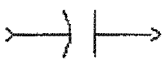
XY Graph

17



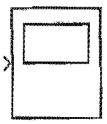
Voltage Measurement

18



Capacitor

19



Scope

Appendix 2

M. Malengret

Compensation of single-phase load connected to three-phase supply

4.1 Introduction

In the previous Chapter it was shown how various methods for balancing poly-phased systems could be achieved in practice. The author finds Czarnecky method of particular interest and is applied to single phase loads.

In this section the author provides the derivation from first principle and applies the theory to single phase loads sullied from three phase systems

Necessary condition for balancing a three phase load

A three phase three wire system can be represented as three admittances as shown in Fig 4.1. Should the loads be in a star configuration then it would be converted to a delta connected equivalent load. The three admittances are assumed to consist of linear elements such as resistors, capacitors and inductances.
If it is required for the supply current to be of equal magnitude and at 120 degree from each other then::

$I_1 = \underline{a}\, I_2 = \underline{a}^* I_3$

And In the case of a three wire three phase supply

$\underline{I}_1 + \underline{I}_2 + \underline{I}_3 = \underline{0}$

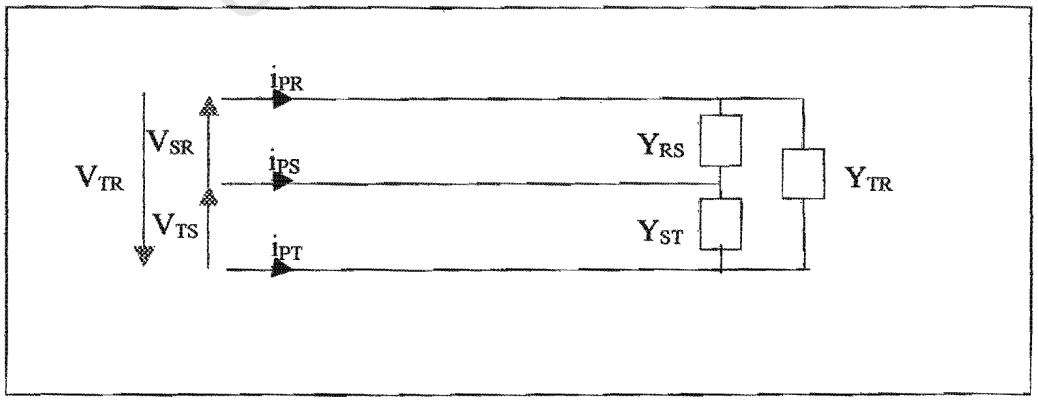


Fig 4.1 Delta connected admittances representing a three-phase load

Therefore:

$\underline{V}_1Y_1 + \underline{V}_2Y_2 + \underline{V}_3Y_3 = 0$

And since the three phase voltages supply are balanced:

$\underline{V}_2 = \underline{a}\,\underline{V}_1$ and $V_3 = \underline{a}^*\,\underline{V}_1$

Substituting the above

$\underline{V}_1Y_1 + \underline{a}\,\underline{V}_1 Y_2 + \underline{a}^*\,\underline{V}_1Y_3 = 0$

Dividing by $\underline{V}_1$

$$\mathbf{Y_1 + \underline{a}\ Y_2 + \underline{a}^*\ Y_3 = 0}$$

Eq 4.1

Therefore the condition for a three phase balanced supply voltages to supply equal currents is that the sum of the space vector sums of the three phase admittances be equal to zero.

Note that the above imply that the three admittance don't necessary have to be equal. **The only necessary condition is that the space vector sum of the three impedances be zero.** This is illustrated in Fig 2.1. ,where the admittances are shown as vectors with their respective real and imaginary components . The real part is the conductance and the imaginary part the susceptance of each load.

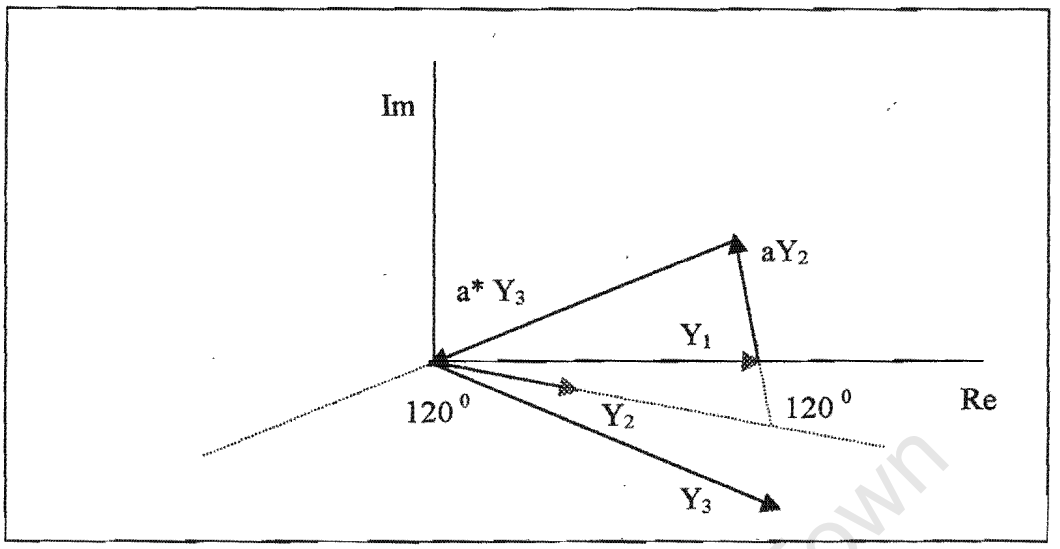
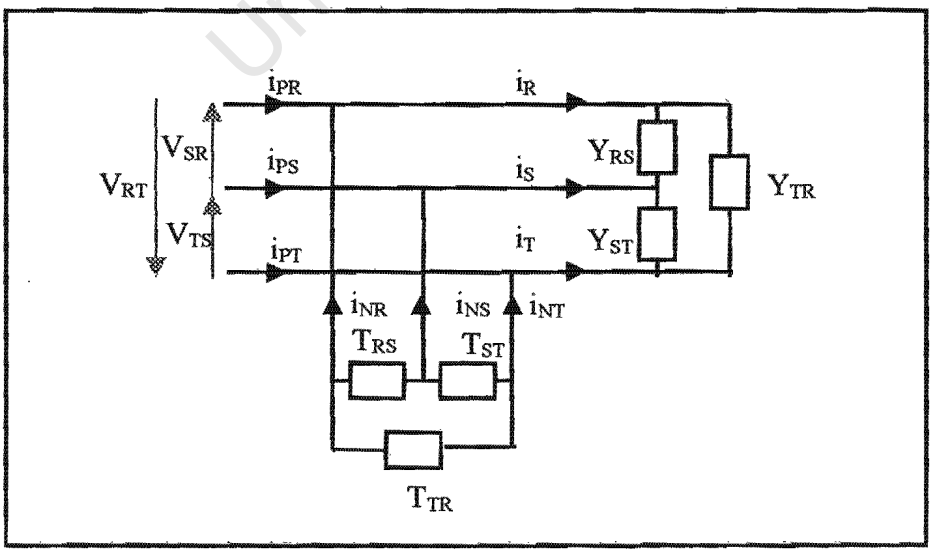


Fig 4.2 Example of unequal admittances with zero space vector sum

Load balancing compensating susceptances

Should the space phasor sum $Y_1 + \underline{a}\, Y_2 + \underline{a}^* Y_3 = \underline{A}$ and not zero. Then the load will be an unbalanced one. In order to restore the balance three susceptances T_{RS}, T_{ST}, T_{TR} can be added in parallel with each of the load admittances as seen in Fig 4.3



If the load is to be balanced by adding three susceptances T_{RS}, T_{ST}, T_{TR} in parallel with each of the load admittances then the total admittance per branch must be considered and using Eq 4.1 to obtain supply current balance:

$(Y_{RS}+ j\, T_{RS}) + a\,(Y_{ST} + j\, T_{ST})\, T_{RS} + a^{*}\,(Y_{TR} + j\, T_{TR}) = 0$

Let us now solve the above equations:

$Y_1 + \underline{a}\, Y_2 + \underline{a}^{*}\, Y_3 + j\, T_{RS} + a\, j\, T_{ST} + a^{*}\, j\, T_{TR} = 0$

$\underline{A} + j\, T_{RS} + (-\tfrac{1}{2} + j\,\sqrt{3}/2)\, j\, T_{ST} + (-\tfrac{1}{2} - j\,\sqrt{3}/2)\, j\, T_{TR} = 0$

$\mathrm{Re}\,\underline{A} + \mathrm{Im}\,\underline{A} + j\, T_{RS} - \tfrac{1}{2}\, j\, T_{ST} - \tfrac{1}{2}\, j\, T_{TR} - \sqrt{3}/2\; T_{ST} + \sqrt{3}/2\; T_{TR} = 0$

Equating real part to zero:

$\mathrm{Re}\,\underline{A} - \sqrt{3}/2\; T_{ST} + \sqrt{3}/2\; T_{TR} = 0$

$$\mathbf{T_{TR} - T_{ST} = (2/\sqrt{3})\, Re\, \underline{A}} \qquad \textbf{Eq 4.2}$$

Equating the imaginary part: to zero :

$\mathrm{Im}\,\underline{A} + j\, T_{RS} - \tfrac{1}{2}\, j\, T_{ST} - \tfrac{1}{2}\, j\, T_{TR} = 0$

$$\mathbf{T_{ST} + T_{TR} + 2\, T_{RS} = -\, Im\, \underline{A}} \qquad \textbf{Eq 4.3}$$

There are only two equations but three unknown. Therefore if one of the compensating susceptance is given any value the other two will be determined.

Load compensating with two reactances only

If one of the susceptances is zero then the two others can be determined

If T_{ST} is zero then

$$\mathbf{T_{TR} = (2/\sqrt{3})\, Re\, \underline{A}}$$

$$\mathbf{T_{RS} = -\, Im\; 1/2\, \underline{A} - (1/\sqrt{3})\, Re\, \underline{A}}$$

Load balancing and reactive compensating susceptances

A third condition such as unity power factor can also be imposed.
For unity power factor the sum of all the susceptance must be zero in the case of a balanced voltage supply. Therefore

$\text{Im } A + T_{RS} + T_{ST} + T_{TR} = 0$` Eq 4.4

Therefore combining Eq 4.2. , Eq 4.2. and Eq 4.2. gives:

$$T_{RS} = j\{\sqrt{3}\, R_e \underline{A} - \text{Im } \underline{A} - B_e\} / 3$$

$$T_{ST} = j\{2\, \text{Im } \underline{A} - B_e\} / 3$$

$$T_{TR} = -j\{\sqrt{3}\, R_e \underline{A} + \text{Im } \underline{A} + B_e\} / 3$$

Eq 4.1

As given in the previous chapter. What is of particular interest is that the three compensating elements are purely reactive.

No real power is therefore required in order to balance any unequal loads. The three load admittances Y_{RS}, Y_{ST}, Y_{TR} can be of any complex value.
A single phase load can therefore be considered as an extreme case of an unbalanced load ,where two of the load admittance are nil.

4.2 Compensator for a single phase load

The above theory is now applied by the author to an unbalanced three-phase load consisting of only one load admittance with the other two equal to zero as shown in Fig 4.2.

The load is a single-phase load. Admittances Y_{RS} and Y_{TR} are considered as open circuit, hence, $Y_{RS}=0$ and $Y_{TR}=0$. Substituting in Eq 4.1.

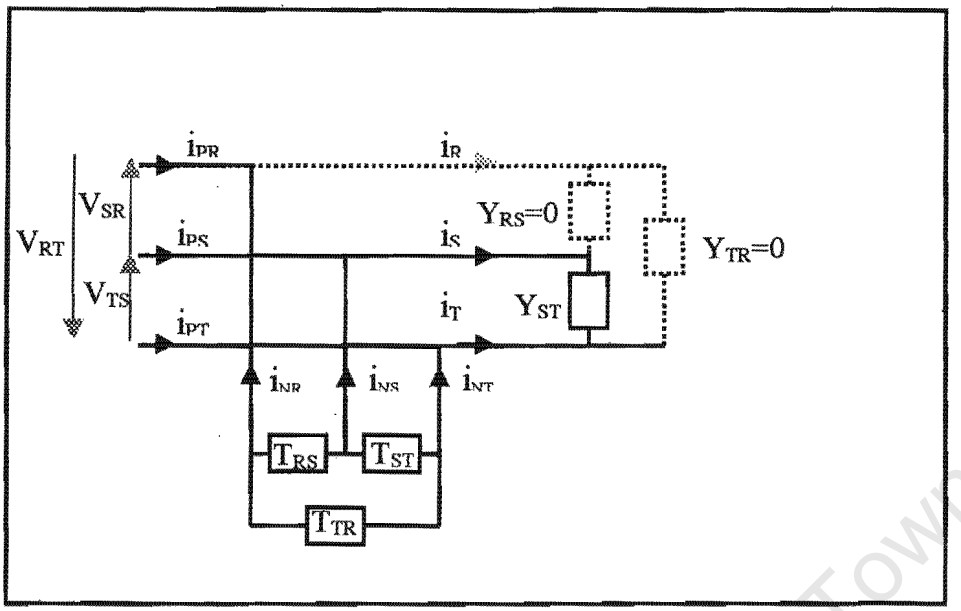


Figure 4.2 Single-phase load

$$\underline{Y}_e = Y_{ST} = G_1 + jB_1$$
$$\underline{A} = -Y_{ST} = -G_1 - jB_1$$
$$B_E = B_1$$

Eq 4.2.

G_1 is the conductance and B_1 the susceptance of the single-phase load. Substituting $\underline{B}_e$ and $\underline{A}$ in Eq 4.1.

$$T_{RS} = j\{\sqrt{3}\,\mathrm{Re}\,(-G_1-jB_1) - \mathrm{Im}\,(-G_1-jB_1) - B_1\}/3$$

$$T_{ST} = j\{2\,\mathrm{Im}\,(-G_1-jB_1) - B1\}/3$$

$$T_{TR} = -j\{\sqrt{3}\,\mathrm{Re}\,+(-G_1-jB_1)+\mathrm{Im}\,(-G_1-jB_1)+B_1\}/3$$

Hence

$$T_{RS} = -j(1/\sqrt{3})\,G_1$$

$$T_{ST} = -jB_1$$

$$T_{TR} = j(1/\sqrt{3})\,G_1$$

Eq 4.4

Therefore the three susceptances above would correct unbalance and reactive power seen by the three-phase supply.

If one adds an equal susceptance j B_1 to T_{RS}, T_{ST}, and T_{TR} respectively one would still have a balanced load from the supply point of view. The following results are obtained

$$T_{RS} = -j(1/\sqrt{3})\, G_1 + jB_1$$

$$T_{ST} = -jB_1 + jB_1 = 0$$

$$T_{TR} = j(1/\sqrt{3})\, G_1 + jB_1$$

Eq 4.5.

The compensator reduces to two elements only as seen in Fig 4.3.

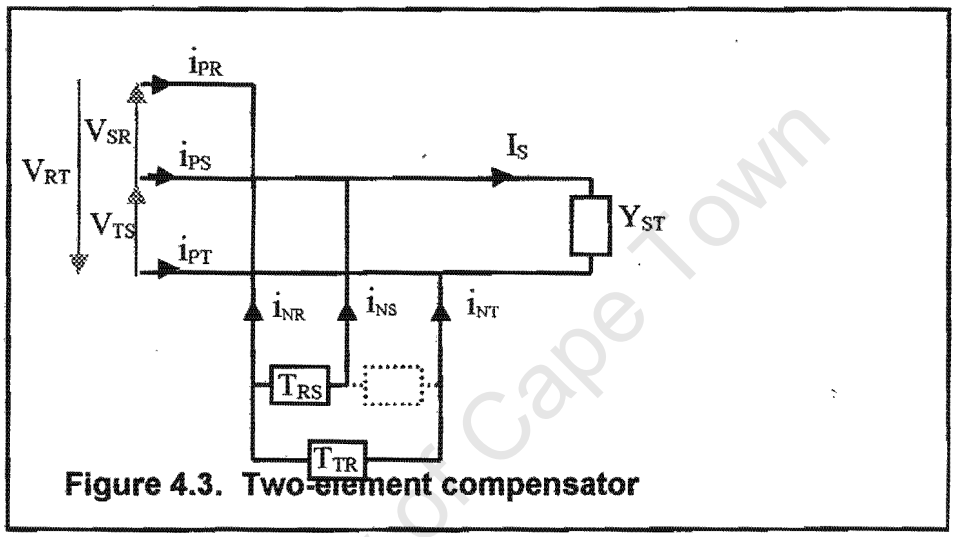


Figure 4.3. Two-element compensator

If now the two susceptances are expressed as reactances X_{RS} and X_{TS} then:

$X_{RS} = 1/T_{RS} = 1/ (-j(1/\sqrt{3})\, G_1 + jB_1) = j\sqrt{3} / (G_1 + \sqrt{3}\ B_1)$

Substituting for $G_1 = R_1 / (R_1^2 + X_1^2)$ **and** $B_1 = -X_1 / (R_1^2 + X_1^2)$

Then

$X_{RS} = j\sqrt{3}\,(R_1^2 + X_1^2) / (R_1 + \sqrt{3}\, X_1)$

$XT_R = j\sqrt{3}\,(R_1^2 + X_1^2) / (R_1 - \sqrt{3}\, X_1)$

Two susceptances are therefore sufficient to balance a single phase load. The supply will however have to supply the reactive power required by the three impedance B_1 that have been added. The three phase supply would have to deliver the active power $P=V^2G_1$ Watt of the single-phase load and the reactive power $Q= 3V^2B_1$VAr. The power factor would be cos (arctan($3B_1/G_1$)).

4.3 Compensator for resistive single-phase load.

If the load is purely resistive, then $B_1=0$ and Eq 4.5. becomes .

$$T_{RS} = -(1/\sqrt{3})\, G_1$$

$$T_{ST} = 0$$

$$T_{TR} = (1/\sqrt{3})\, G_1$$

Eq 4.6

Referring to Fig 4.3, the compensator currents $\underline{i}_{NS}$, $\underline{i}_{NT}$, $\underline{i}_{NR}$ can be calculated as follows:
Assuming that the three-phase supply voltages V_{TS}, V_{SR}, V_{RT} are balanced sinusoids and of positive sequence direction.

$\underline{V}_{TS} = V\angle 0$, $\underline{V}_{SR} = V\angle 120$, $\underline{V}_{RT} = V\angle 240$,
if $I = VG_1$
and using Eq 4.6 (see figure 4.3)

$\underline{i}_{NS} = \underline{V}_{SR}\, j\,(T_{RS}) = V\angle 120 \times (-j\, G1/\sqrt{3}) = I/\sqrt{3}\angle 120 - 90$ **$\underline{i}_{NS} = I/\sqrt{3}\angle 30$**

$\underline{i}_{NT} = -\underline{V}_{RT}\, j\,(T_{TR}) = -V\angle 240 \times (j\, G1/\sqrt{3}) = I/\sqrt{3}\angle 240 - 90$ **$\underline{i}_{NT} = I/\sqrt{3}\angle 150$**

$\underline{i}_{NR} = -\underline{i}_{NS} - \underline{i}_{NT} = -I/\sqrt{3}\angle 30 - I/\sqrt{3}\angle 150$ **$\underline{i}_{NR} = I/\sqrt{3}\angle 270$**

The magnitude of the negative sequence current is $1/\sqrt{3}$ of the single-phase load current I_S.

It is observed that this is a balanced negative sequence current
it follows that the 3 phase supply currents can be determined as :

$\underline{i}_{PR} = -\underline{i}_{NR} = -I/\sqrt{3}\angle 270$ **$\underline{i}_{PR} = I/\sqrt{3}\angle 90$**

$\underline{i}_{PS} = \underline{I}_s - \underline{i}_{NS} = I\angle 0 - I/\sqrt{3}\angle 30$ **$\underline{i}_{PS} = I/\sqrt{3}\angle -30$**

$\underline{i}_{PT} = -\underline{I}_s - \underline{i}_{NT} = I\angle 0 - I/\sqrt{3}\angle 330$ **$\underline{i}_{PT} = I/\sqrt{3}\angle 210$**

The three phase supply current magnitude are $1/\sqrt{3}$ that of the single phase load current and it is a balanced positive sequence current. The negative and positive sequence current add up to make $\underline{I}_s$, 0,$-\underline{I}_s$ .These currents can be seen that in Fig 4.4. The compensating susceptances , $T_{RS} = -(1/\sqrt{3})\, G_1$ and $T_{TR} = (1/\sqrt{3})\, G_1$ **"inject" the negative sequence current necessary** so as to balance the unbalance load consisting of a single resistive element. The supply delivers a balance three phase current.

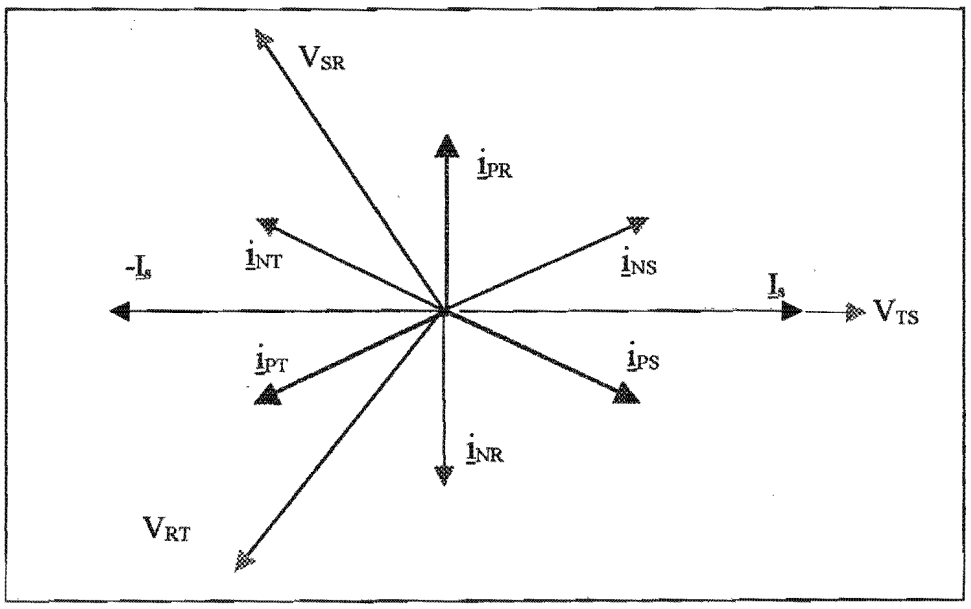


Figure 4.4. Balanced supply positive sequence current: $\underline{i}_{PS}$, $\underline{i}_{PT}$, $\underline{i}_{PR}$, compensator negative sequence current: $\underline{i}_{NS}$, $\underline{i}_{NT}$, $\underline{i}_{NR}$ and single phase load current $\underline{I}_s$.

A relevant observation is that $\underline{i}_{NS} = -\underline{i}_{PT}$ and $\underline{i}_{NT} = -\underline{i}_{PS}$. The negative sequence components are the conjugates of the positive sequence. This implies that $\underline{i}_{PS}$ can be measured directly and used as such as the commanded value for the compensator injected current $\underline{i}_{NT}$. Likewise $\underline{i}_{PT}$ can also be measured and used to control the compensator injected current $\underline{i}_{NS}$. This suggests a simple control strategy for a purely active load. See Fig 4.5.

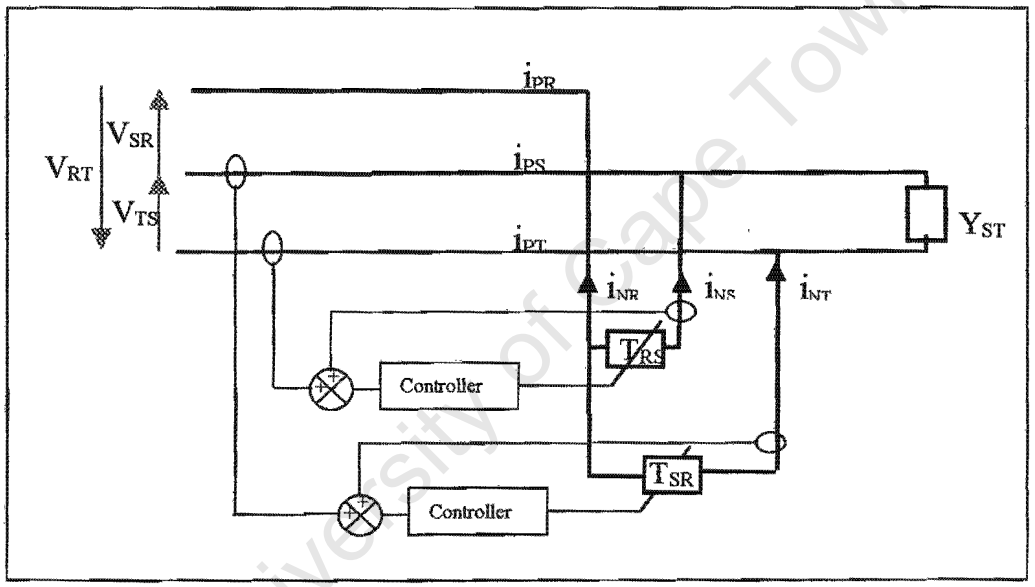


Figure 4.6. Load balancing control method

A simulated system is shown in Appendix 4

4.4 Compensator for resistive and reactive load.

In the more general case of a resistive and reactive single phase load one would like to know if above observations are still true.

Assuming that the three-phase supply voltages V_{TS}, V_{SR}, V_{RT} as the previous case balanced sinusoids and of positive sequence direction.

$\underline{V}_{TS} = V\angle 0$, $\underline{V}_{SR} = V\angle +120$, $\underline{V}_{RT} = V\angle +240$,
if now $\underline{I}_s = \underline{V}_{TS}(G_1 + j\,B_1) = \underline{V}_{TS}\,G_1 + \underline{V}_{TS}\,j\,B_1 = I + j\,I_{B1}$

where $I = V_{TS} G_1$ and $I_{B1} = V_{TS} B_1$
and using Eq 4.5

where

$T_{RS} = -j(1/\sqrt{3}) G_1 + jB_1$

$T_{ST} = 0$

$T_{TR} = j(1/\sqrt{3}) G_1 + jB_1$

Then,

$\underline{i}_{NS} = \underline{V}_{SR} (T_{RS}) = V\angle 120 \times (-j G1/\sqrt{3} + j B_1) = V (G_1/\sqrt{3} - B_1) \angle 120 - 90$
$= (G_1/\sqrt{3}) V\angle 30 - B_1 V\angle 30$ and

$\mathbf{\underline{I}_{NS} = I/\sqrt{3} \angle 30 + I_{B1} \angle 210}$

$\underline{i}_{NT} = - \underline{V}_{RT} j (T_{RT}) = - V\angle 240 \times (j G1/\sqrt{3} + j B_1) = V (G_1/\sqrt{3} + B_1) \angle 240 - 90$
$= V\angle 150 (G_1/\sqrt{3} + B_1)$ and
$= (G_1/\sqrt{3}) V\angle 150 + B_1 V\angle 150$ and

$\mathbf{\underline{I}_{NT} = I/\sqrt{3} \angle 150 + I_{B1} \angle 150}$

$\underline{i}_{NR} = -\underline{i}_{NS} - \underline{i}_{NT}$

$\mathbf{\underline{I}_{NR} = I/\sqrt{3} \angle 270 + \sqrt{3} I_{B1} \angle 0}$

It must be noted that the compensating reactances currents are not balanced
Let us now derive the supply side currents.

$\underline{i}_{PR} = -\underline{i}_{NR}$

$\mathbf{\underline{I}_{PR} = I/\sqrt{3} \angle 90 + \sqrt{3} I_{B1} \angle 180}$

$\underline{i}_{PS} = \underline{I}_s - \underline{i}_{NS} = I + j I_{B1} - I/\sqrt{3} \angle 30 + I_{B1} \angle 30 = I - I/\sqrt{3} \angle 30 + j I_{B1} + I_{B1} \angle 30$

$\mathbf{\underline{I}_{PS} = I/\sqrt{3} \angle -30 + \sqrt{3} I_{B1} \angle 60}$

$\underline{i}_{PT} = -\underline{I}_s - \underline{i}_{NT} = -I - j I_{B1} - I/\sqrt{3} \angle 150 - I_{B1} \angle 150 = -I - I/\sqrt{3} \angle 150 - j I_{B1} + I_{B1} \angle 150$

$\mathbf{\underline{I}_{PT} = I/\sqrt{3} \angle 210 + \sqrt{3} I_{B1} \angle -60}$

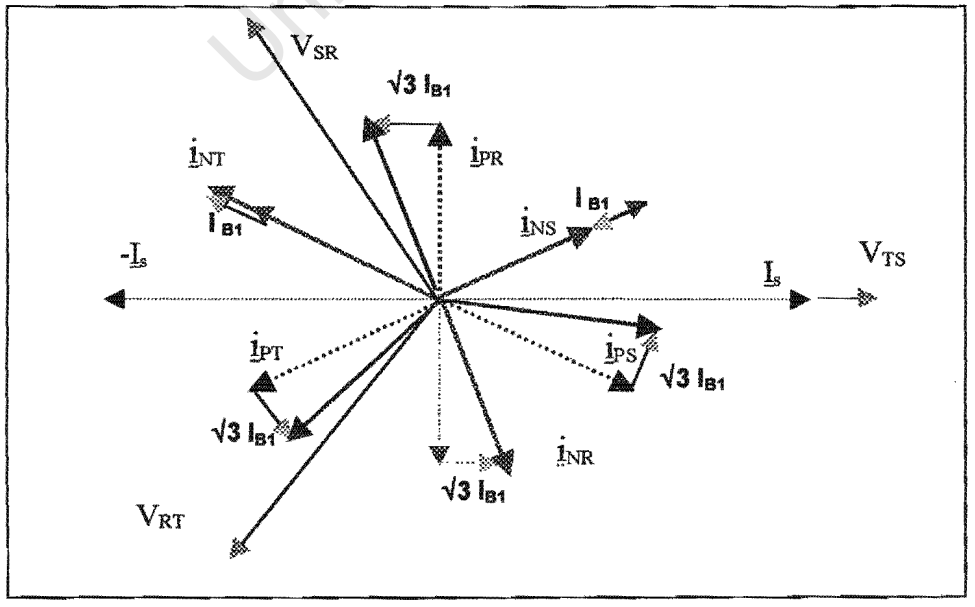


Figure 4.5. Reactive and resistive load phasor diagram. Notice that the supply positive sequence current $\underline{i}_{PS}$, $\underline{i}_{PT}$, $\underline{i}_{PR}$ are balanced and compensator current: $\underline{i}_{NS}$, $\underline{i}_{NT}$, $\underline{i}_{NR}$ are now unbalanced . The supply power factor is not unity.

In conclusion in the case of a two element compensator equation 4.4 the supply current is indeed balanced. However the power factor is not unity and the compensating current are not balanced and therefore not simply the negative sequence current.

4.5 Calculation of Compensator current for resistive and reactive single phase load

If the single phase load admittance $Y1= G_1 + j\, B_1$ is known then according to equation 4.5 only two components are necessary so as to balance the load.

$$T_{RS} = -j(1/\sqrt{3})\, G_1 + jB_1$$

$$T_{TR} = j(1/\sqrt{3})\, G_1 + jB_1$$

The conductance value G_1 and susceptance B_1 are needed. These can be obtained from the real time value of the single phase load current I_{TS} and voltage V_{TS} as seen on Fig 4.3
The conductance value G_1 and susceptance B_1 can be obtained with analogue or digital mean.

$$G1 = P / \| v \|^2$$
$$B1 = Q / \| v \|^2$$

P and Q are the average power and reactive power respectively.and $\|v\|$ the norm or RMS value of the sinusoidal voltage.
These value can be calculated with a digital or analoque method.
An practical analogue circuit is shown in appendix 5 with a Mathlab/Simulink simulation using the Power system toolbox. Experimental verification was also implemented .

4.6 Conclusion

The approach of Czarnesky for 3 phase load balancing has been adapted to the extreme case which is a single phase load. The unbalanced single phase load can be compensated with two elements only .The two elements calculated are the similar to the one derived by Holmes for single phase to three phase supply conversion and therefore suggests that the load balancing theory developed in this chapter could also be applied to single phase conversion. In the case of a unity power factor load the current flowing in these compensating reactance are shown to be balanced negative sequence current. This brings Alexander's method reviewed in Chapter 3 and Fontescue classic analysis of unbalance systems into focus. The negative sequence currents are the conjugates of the positive sequence current. This suggest a simple method of control for the variable compensating reactances.

This is however only true for unity power factor (or corrected) single-phase loads. In the case of reactive single phase load the compensating reactance or current can be calculated from the single phase conductance and susceptance. A real time method of obtaining these values has been described, simulated and tested. The single phase load was assumed to be linear and the three phase supply voltages balanced and sinusoidal.

Appendix 3

1. **Table 5.1** Admittance measurements

2. **Analogue devices** AD633 analogue multiplier

3. **National semiconductors** Lm324 Quad operational amplifier

ADMITTANCE MEASUREMENT RESULTS FOR SECTION 5.5

TARGET SUSCEPTENCES		MEAS URED SUSCE PTANCES						COMPUTED B's	
Bc1	Bc2	B1	G1	B2	G2	G(total)	B(total)	B*1	B*2
0.5197	-0.6929	0.305	0.974	0.122	0.3751	0.268	0.08717	0.9748	-1.299
0.2438	-0.2951	0.2169	0.6665	0.1206	0.3705	0.2386	0.07749	0.8126	-0.935
0.1433	-0.1954	0.1394	0.4283	0.05138	0.158	0.1155	0.03756	0.4297	-0.5858
0.2448	0.2012	0.05144	0.1581	0.09428	0.2897	0.1025	0.0333	0.4258	-0.3499
0.1086	-0.1209	0.03565	0.1096	0.02575	0.07918	0.04611	0.01498	0.1547	-0.1722
0.04955	-0.05464	0.09596	0.2949	0.07139	0.1295	0.126	0.04096	0.4237	-0.4672
0.08339	-0.0651	0.01793	0.0551	0.03898	0.1197	0.0379	0.01231	0.1701	-0.1328
1.155	-1.443	0.6507	2	0.3253	1	0.6668	0.2169	2.309	-2.887
0.5774	-0.07217	0.3253	0.999	0.1627	0.5001	0.3335	0.1085	1.155	-1.443
0.5774	-0.07217	0.3579	1.1	0.1789	0.5505	0.3668	0.1193	1.27	-1.588

Table 5.1

Low Cost Analog Multiplier

AD633

FEATURES

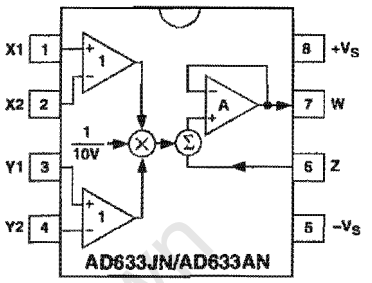
Four-Quadrant Multiplication
Low Cost 8-Lead Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS

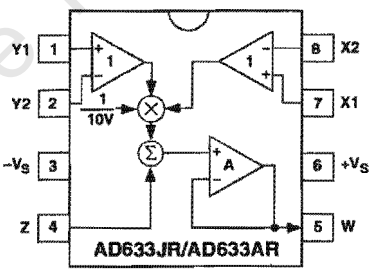
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

CONNECTION DIAGRAMS

8-Lead Plastic DIP (N) Package



8-Lead Plastic SOIC (SO-8) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

The AD633 is available in an 8-lead plastic DIP package (N) and 8-lead SOIC (R). It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the –40°C to +85°C industrial temperature range (A Grade).

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-lead plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

REV. D

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD633—SPECIFICATIONS (T_A = 25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J, AD633A			
TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	–10 V ≤ X, Y ≤ +10 V		±1	±2	% Full Scale
T_{MIN} to T_{MAX}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	±1	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	±0.4	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	±1	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	±0.4	% Full Scale
Output Offset Voltage			±5	±50	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		μV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		±11			V
Short Circuit Current	R_L = 0 Ω		30	40	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	±10			V
	Common Mode	±10			V
Offset Voltage X, Y			±5	±30	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	60	80		dB
Bias Current X, Y, Z			0.8	2.0	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		±8		±18	V
Supply Current	Quiescent		4	6	mA

NOTES

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	500 mW
Input Voltages[3]	±18 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
AD633J	0°C to 70°C
AD633A	–40°C to +85°C
Lead Temperature Range (Soldering 60 sec)	300°C
ESD Rating	1000 V

NOTES

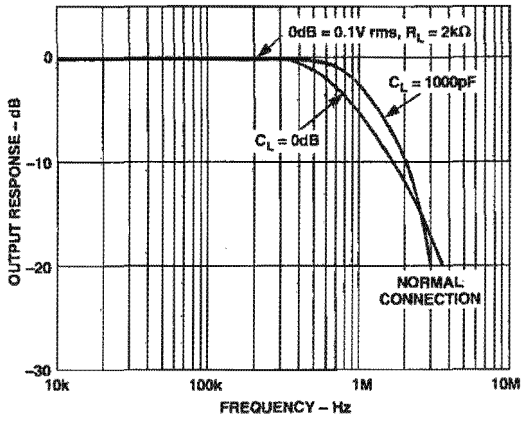
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/W; 8-Lead Small Outline Package: θ_{JA} = 155°C/W.

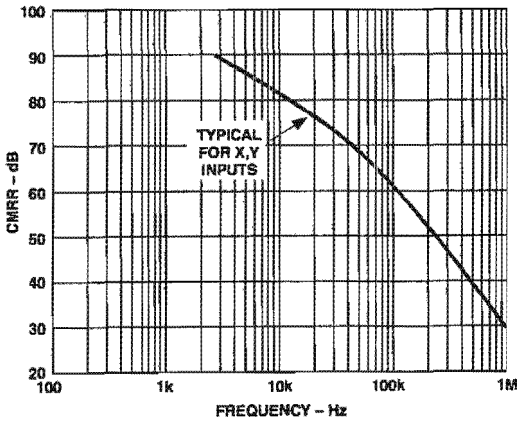
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

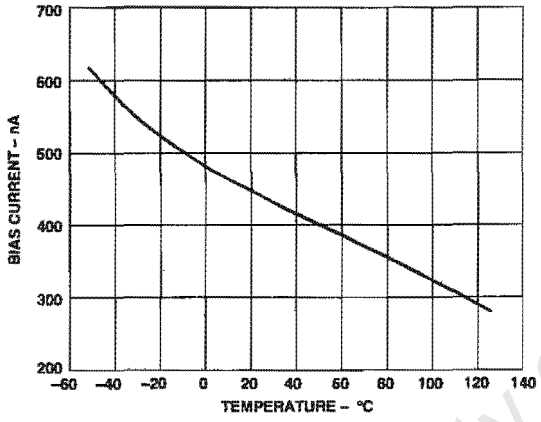
Model	Temperature Range	Package Description	Package Option
AD633AN	–40°C to +85°C	Plastic DIP	N-8
AD633AR	–40°C to +85°C	Plastic SOIC	SO-8
AD633AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD633AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
AD633JN	0°C to 70°C	Plastic DIP	N-8
AD633JR	0°C to 70°C	Plastic SOIC	SO-8
AD633JR-REEL	0°C to 70°C	13" Tape and Reel	SO-8
AD633JR-REEL7	0°C to 70°C	7" Tape and Reel	SO-8



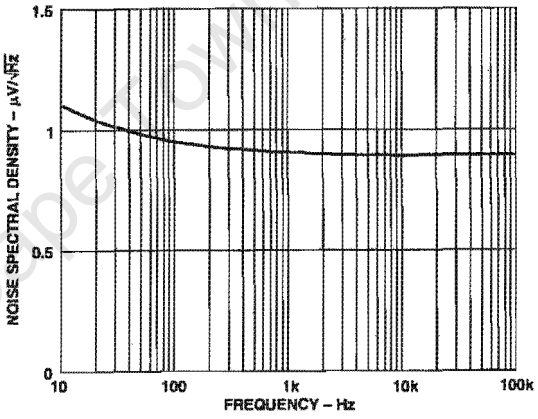
TPC 1. Frequency Response



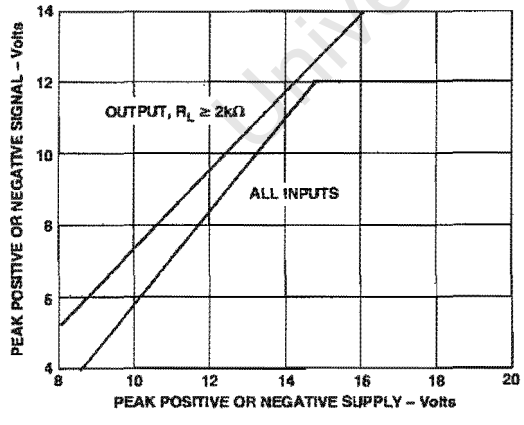
TPC 4. CMRR vs. Frequency



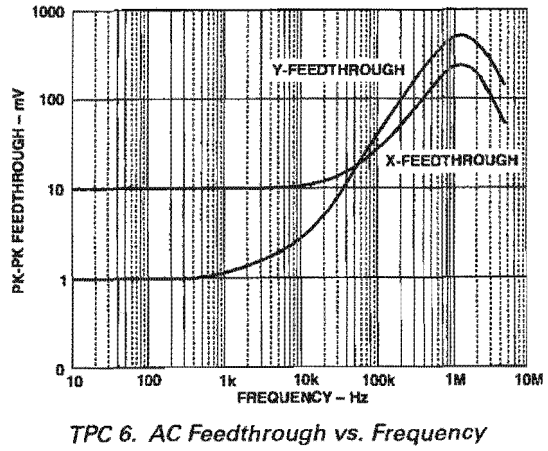
TPC 2. Input Bias Current vs. Temperature (X, Y, or Z Inputs)



TPC 5. Noise Spectral Density vs. Frequency



TPC 3. Input and Output Signal Ranges vs. Supply Voltages



TPC 6. AC Feedthrough vs. Frequency

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of $(X \times Y)/10 + Z$ is then applied to the output amplifier. The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

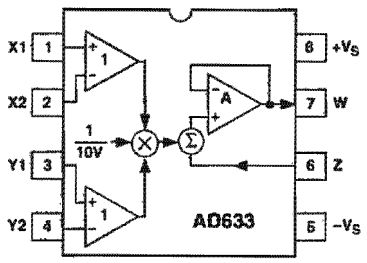


Figure 1. Functional Block Diagram (AD633JN Pinout Shown)

Inspection of the block diagram shows the overall transfer function to be:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z \qquad \text{(Equation 1)}$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 2. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

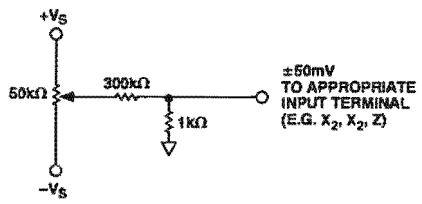


Figure 2. Optional Offset Trim Configuration

APPLICATIONS

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Note that these applications show the pin connections for the AD633JN pinout (8-lead DIP), which differs from the AD633JR pinout (8-lead SOIC).

Multiplier Connections

Figure 3 shows the basic connections for multiplication. The X and Y inputs will normally have their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

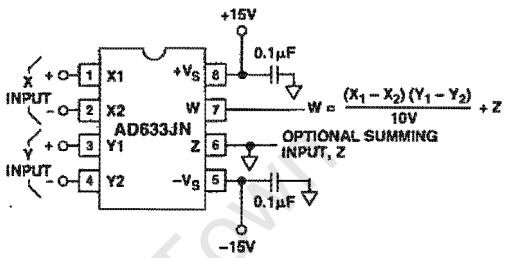


Figure 3. Basic Multiplier Connections

Squaring and Frequency Doubling

As Figure 4 shows, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input may have either polarity, but the output will be positive. However, the output polarity may be reversed by interchanging the X or Y inputs. The Z input may be used to add a further signal to the output.

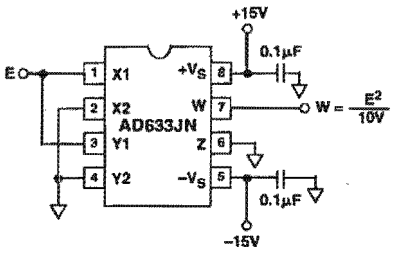


Figure 4. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, since

$$\frac{(E \sin \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - \cos 2\omega t) \qquad \text{(Equation 2)}$$

Equation 2 shows a dc term at the output which will vary strongly with the amplitude of the input, E. This can be avoided using the connections shown in Figure 5, where an RC network is used to generate two signals whose product has no dc term. It uses the identity:

$$\cos\theta \sin\theta = \frac{1}{2}(\sin 2\theta) \qquad \text{(Equation 3)}$$

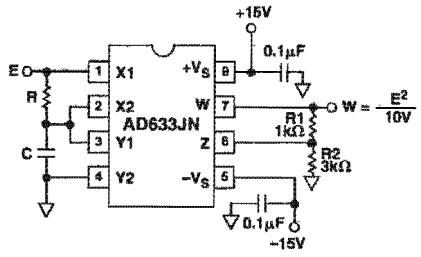


Figure 5. "Bounceless" Frequency Doubler

At $\omega_o = 1/CR$, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$), and the Y input lags the X input by 45° (and is also attenuated by $\sqrt{2}$). Since the X and Y inputs are 90° out of phase, the response of the circuit will be (satisfying Equation 3):

$$W = \frac{1}{(10\,V)}\frac{E}{\sqrt{2}}\left(\sin \omega_o t + 45°\right)\frac{E}{\sqrt{2}}\left(\sin \omega_o t - 45°\right)$$

$$= \frac{E^2}{(40\,V)}\left(\sin 2\ \omega_o t\right) \qquad \text{(Equation 4)}$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at $\omega = 0.9\ \omega_o$, and $\omega_o = 1.1\ \omega_o$.

Generating Inverse Functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 6 shows how to implement a square rooter with the transfer function

$$W = \sqrt{(10\,E)\,V} \qquad \text{(Equation 5)}$$

for the condition E<0.

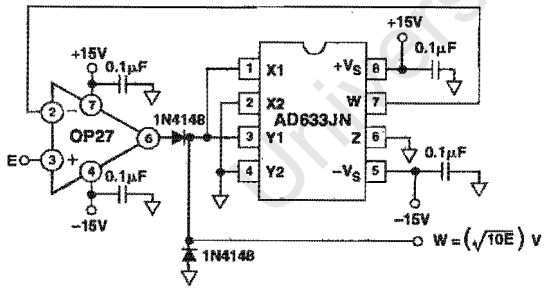


Figure 6. Connections for Square Rooting

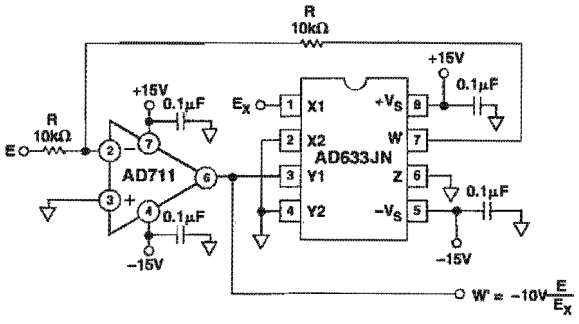


Figure 7. Connections for Division

Likewise, Figure 7 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10V)\frac{E}{E_X} \qquad \text{(Equation 6)}$$

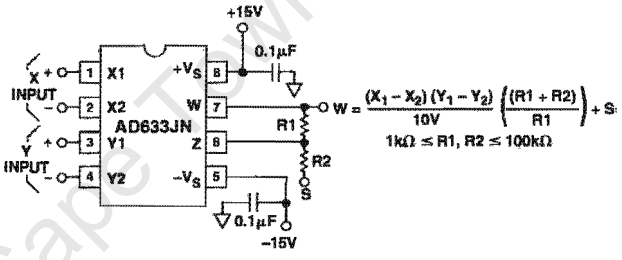


Figure 8. Connections for Variable Scale Factor

Variable Scale Factor

In some instances, it may be desirable to use a scaling voltage other than 10 V. The connections shown in Figure 8 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, may be used to add an additional signal to the output or it may be grounded.

Current Output

The AD633's voltage output can be converted to a current output by the addition of a resistor R between the AD633's W and Z pins as shown in Figure 9 below. This arrangement forms

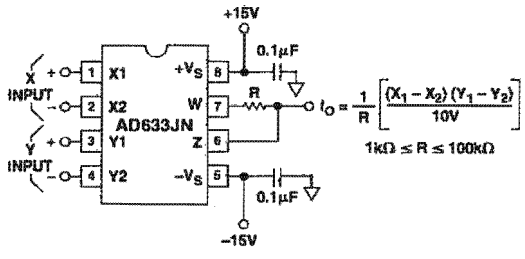


Figure 9. Current Output Connections

the basis of voltage controlled integrators and oscillators as will be shown later in this Applications section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} \qquad \text{(Equation 7)}$$

Linear Amplitude Modulator

The AD633 can be used as a linear amplitude modulator with no external components. Figure 10 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double-sideband signal. The carrier signal is fed forward to the AD633's Z input where it is summed with the double-sideband signal to produce a double-sideband with carrier output.

Voltage Controlled Low-Pass and High-Pass Filters

Figure 11 shows a single multiplier used to build a voltage controlled low-pass filter. The voltage at output A is a result of filtering, E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{(20\,V)\pi RC} \qquad \text{(Equation 8)}$$

and the rolloff is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

The voltage at output B, the direct output of the AD633, has same response up to frequency f_1, the natural breakpoint of RC filter,

$$f_1 = \frac{1}{2\pi RC} \qquad \text{(Equation 9)}$$

then levels off to a constant attenuation of $f_1/f_2 = E_C/10$.

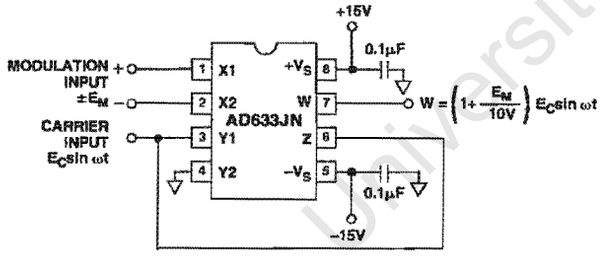


Figure 10. Linear Amplitude Modulator

For example, if R = 8 kΩ and C = 0.002 μF, then output A has a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional zero at 10 kHz (and can be loaded because it is the multiplier's low impedance output). The circuit can be changed to a high-pass filter Z interchanging the resistor and capacitor as shown in Figure 12.

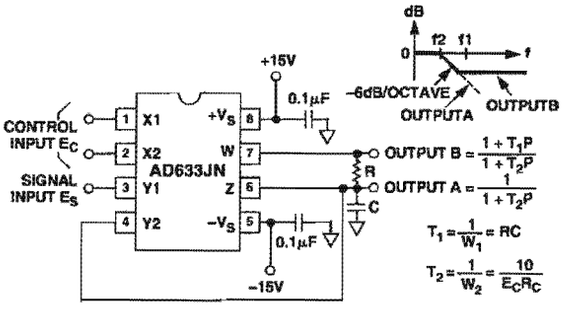


Figure 11. Voltage Controlled Low-Pass Filter

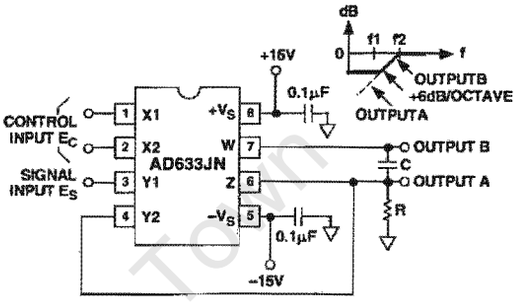


Figure 12. Voltage Controlled High-Pass Filter

Voltage Controlled Quadrature Oscillator

Figure 13 shows two multipliers being used to form integrators with controllable time constants in a 2nd order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the "next" AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y-input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AGC AMPLIFIERS

Figure 14 shows an AGC circuit that uses an rms-dc converter to measure the amplitude of the output waveform. The AD633 and A1, 1/2 of an AD712 dual op amp, form a voltage controlled amplifier. The rms dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator, whose output controls the gain of the voltage controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the circuit's output level. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

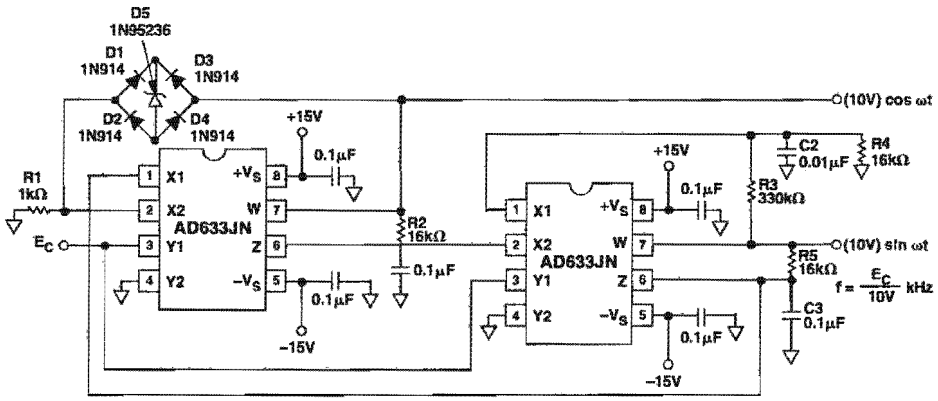


Figure 13. Voltage Controlled Quadrature Oscillator

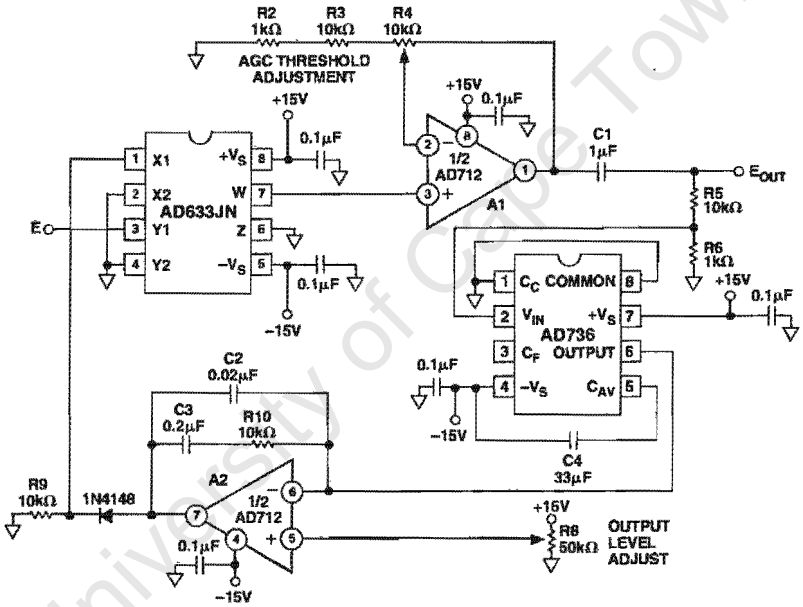
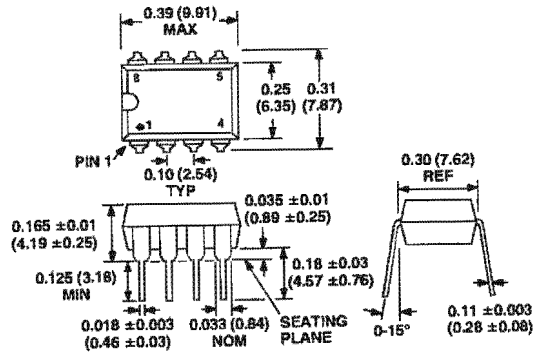


Figure 14. Connections for Use in Automatic Gain Control Circuit

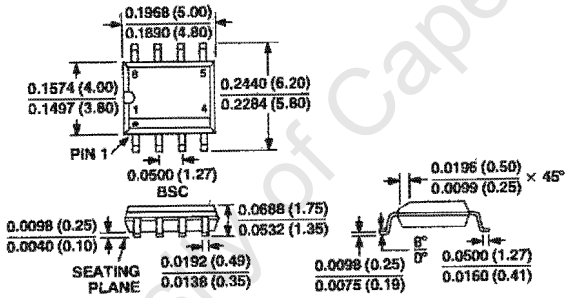
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead Plastic SOIC
(SO-8)



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National Semiconductor

August 2000

LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

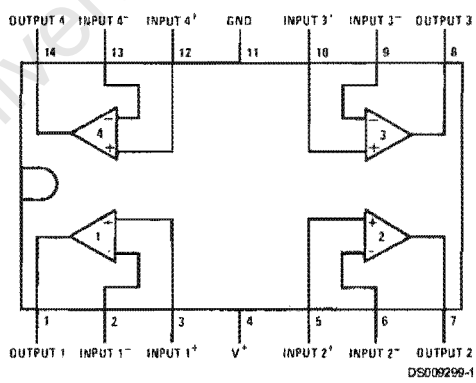
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 µA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagram

Dual-In-Line Package



Top View

Order Number LM124J, LM124AJ, LM124J/883 (Note 2), **LM124AJ/883** (Note 1), **LM224J, LM224AJ, LM324J, LM324M, LM324MX, LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT, LM324MTX or LM2902N LM124AJRQML and LM124AJRQMLV**(Note 3)

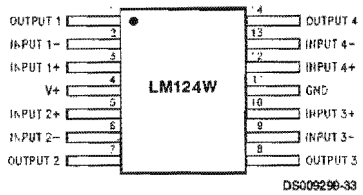
See NS Package Number J14A, M14A or N14A

Note 1: LM124A available per JM38510/11006

Note 2: LM124 available per JM38510/11005

Connection Diagram (Continued)

Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device



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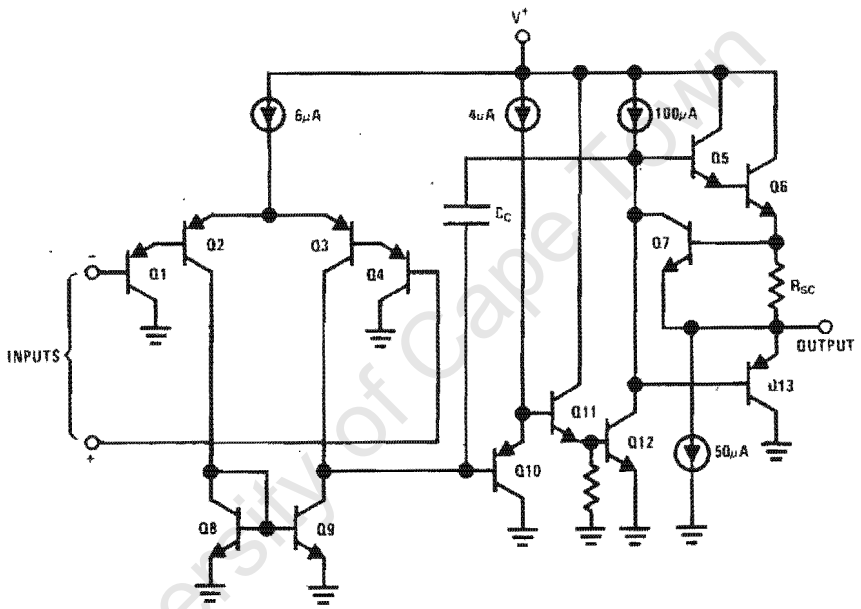
Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Schematic Diagram (Each Amplifier)



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Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current		
(V_{IN} < −0.3V) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 13)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25°C$		1	2		1	3		2	3	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps $V^+ = 30V$ (LM2902 $V^+ = 26V$) $V^+ = 5V$		 1.5 0.7	 3 1.2		 1.5 0.7	 3 1.2		 1.5 0.7	 3 1.2	mA
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25°C$	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25°C$	70	85		70	85		65	85		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124A			LM224A			LM324A			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V), T_A = 25°C		65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				4			4			5	mV
V_{OS} Drift		R_S = 0Ω			7	20		7	20		7	30	µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				30			30			75	nA
I_{OS} Drift		R_S = 0Ω			10	200		10	200		10	300	pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			25			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			26			V
			R_L = 10 kΩ	27	28		27	28		27	28		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	10	15		5	8		5	8		

Electrical Characteristics

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter	Conditions	LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) T_A = 25°C		2	5		2	7		2	7	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 10)	V^+ = 30V, (LM2902, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ On All Op Amps										mA
	V^+ = 30V (LM2902 V^+ = 26V)		1.5	3		1.5	3		1.5	3	
	V^+ = 5V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	V^+ = 15V, $R_L \geq$ 2kΩ, (V_O = 1V to 11V), T_A = 25°C	50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, V_{CM} = 0V to V^+ − 1.5V, T_A = 25°C	70	85		65	85		50	70		dB
Power Supply Rejection Ratio	V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V),	65	100		65	100		50	100		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		T_A = 25°C											
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				7			9			10	mV
V_{OS} Drift		R_S = 0Ω			7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				100			150		45	200	nA
I_{OS} Drift		R_S = 0Ω			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			22			V
			R_L = 10 kΩ	27	28		27	28		23	24		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	100	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	5	8		5	8		5	8		

Note 4: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 5: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 7: These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 8: V_O = 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V) for LM2902, V^+ from 5V to 26V.

Note 9: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 10: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of V^+.

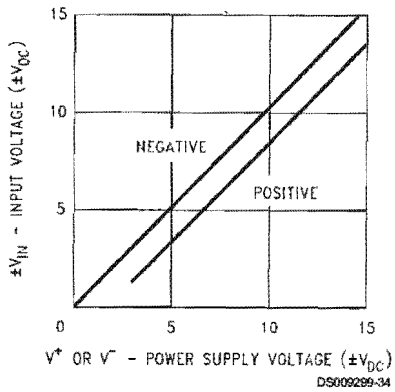
Note 11: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 12: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 13: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Input Voltage Range



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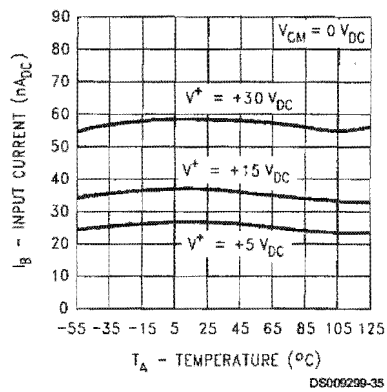
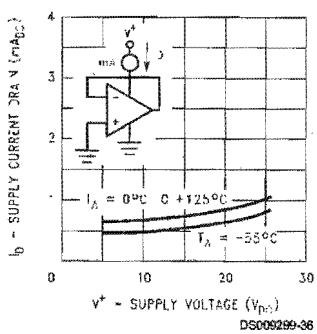
Input Current



DS009299-35

Supply Current



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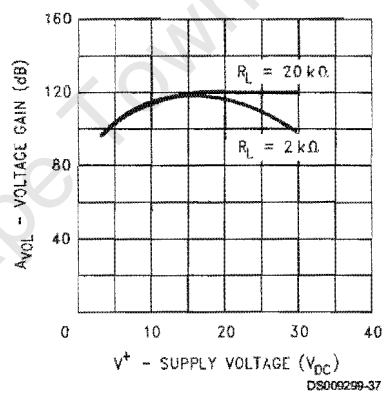
Voltage Gain



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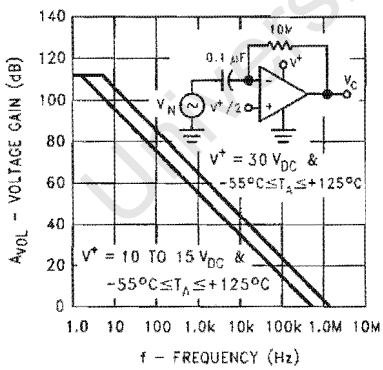
Open Loop Frequency Response



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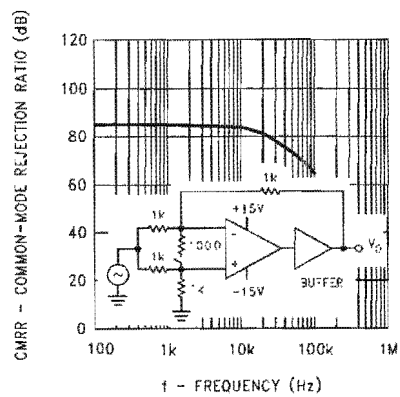
Common Mode Rejection Ratio



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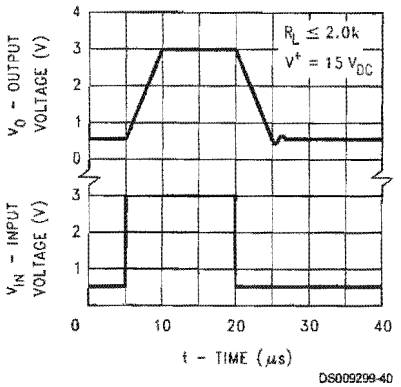
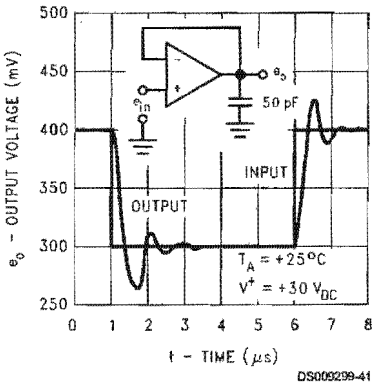
Typical Performance Characteristics (Continued)

Voltage Follower Pulse Response



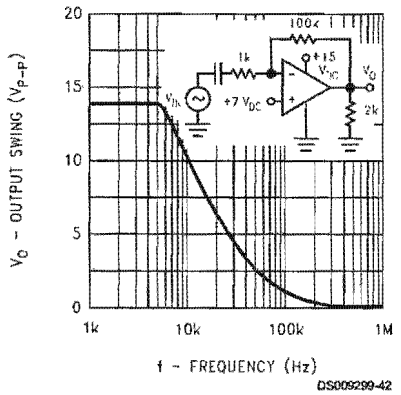
DS009299-40

Voltage Follower Pulse Response (Small Signal)



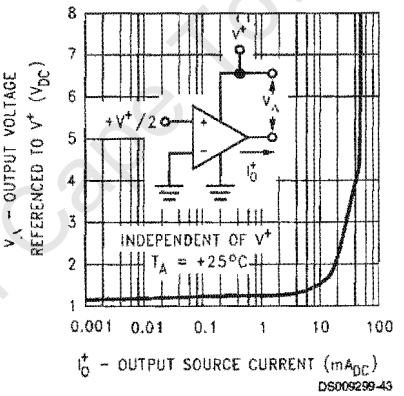
DS009299-41

Large Signal Frequency Response



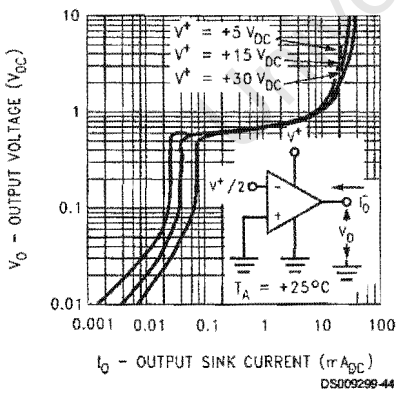
DS009299-42

Output Characteristics Current Sourcing



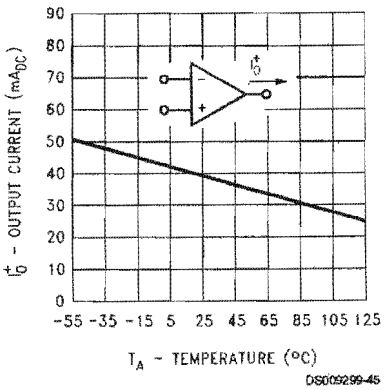
DS009299-43

Output Characteristics Current Sinking



DS009299-44

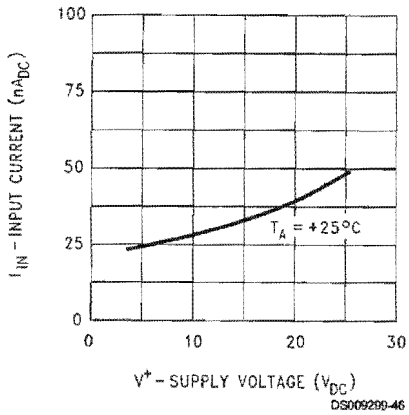
Current Limiting



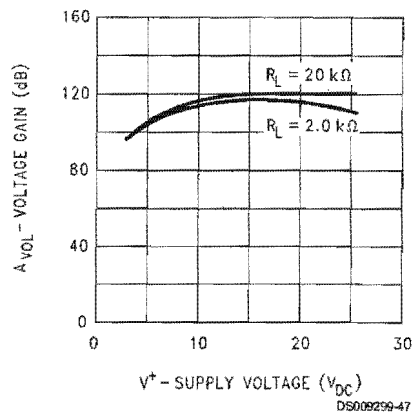
DS009299-45

Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



Voltage Gain (LM2902 only)



Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

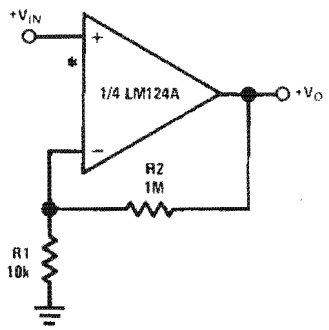
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

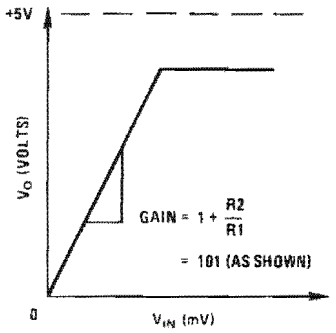
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications (V^+ = 5.0 V_{DC})

Non-Inverting DC Gain (0V Input = 0V Output)

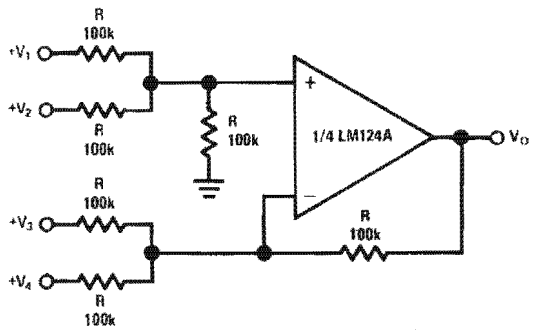




DS009299-5

*R not needed due to temperature independent I_{IN}

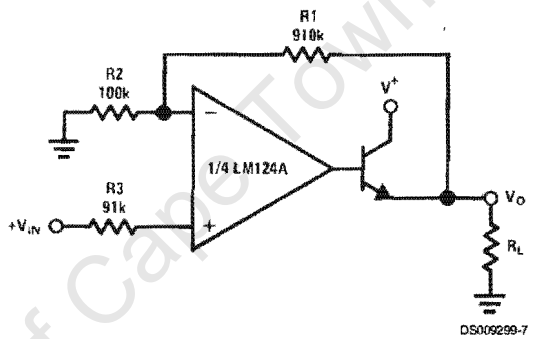
DC Summing Amplifier
(V_{IN}'s ≥ 0 V_{DC} and V_O ≥ V_{DC})



DS009299-6

Where: $V_0 = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

Power Amplifier

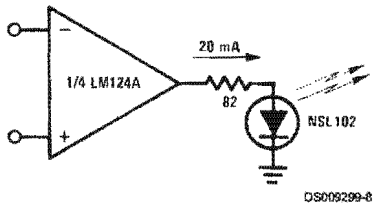


DS009299-7

V_0 = 0 V_{DC} for V_{IN} = 0 V_{DC}
A_V = 10

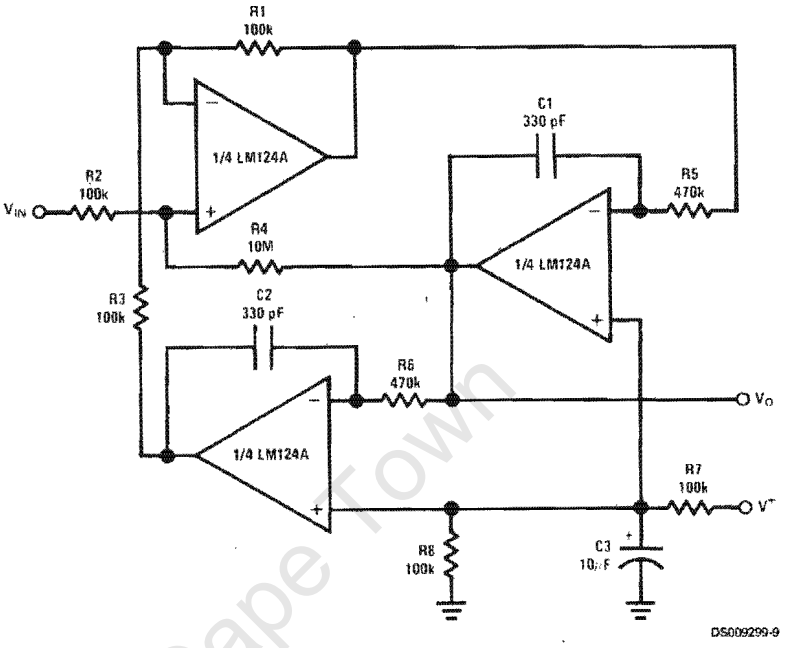
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

LED Driver



DS009299-8

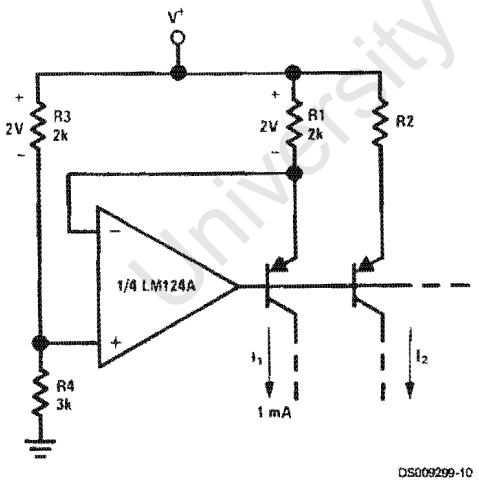
"Bi-QUAD" RC Active Bandpass Filter



DS009299-9

f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

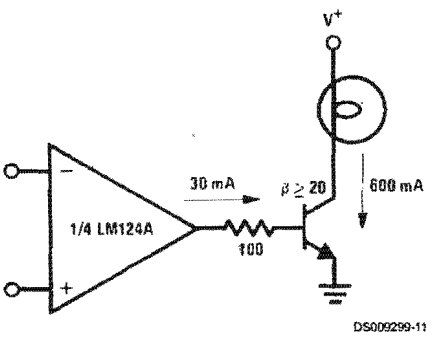
Fixed Current Sources



DS009299-10

$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

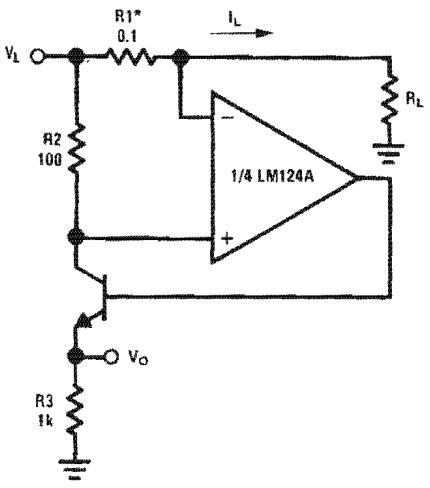
Lamp Driver



DS009299-11

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Current Monitor



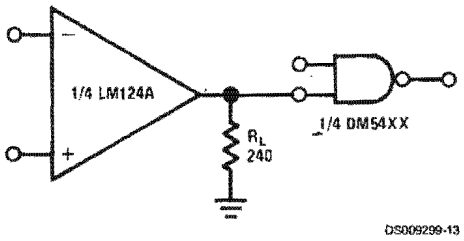
DS009299-12

$$V_O = \frac{1V(I_L)}{1A}$$

$V_L \geq V^+ - 2V$

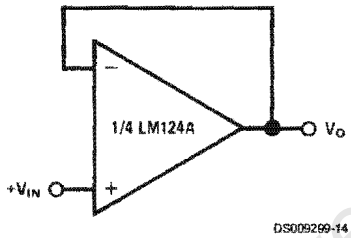
*(Increase R1 for I_L small)

Driving TTL



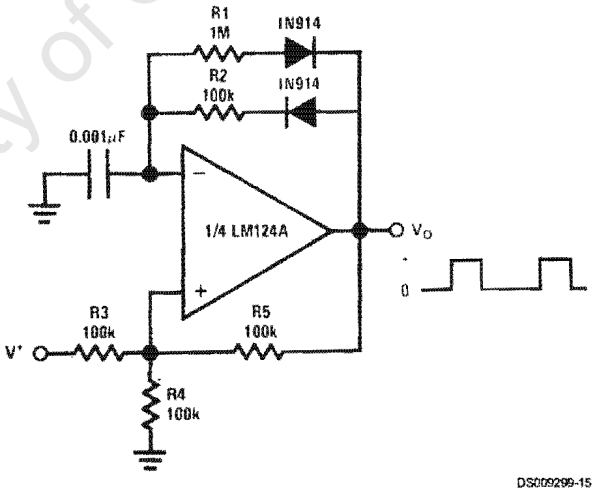
DS009299-13

Voltage Follower



DS009299-14

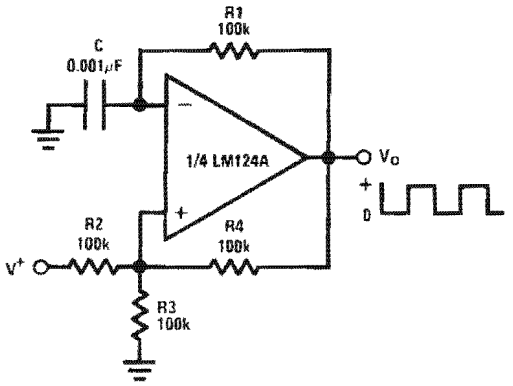
Pulse Generator



DS009299-15

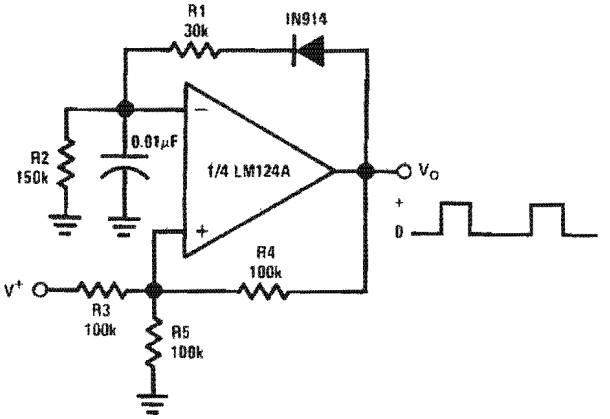
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



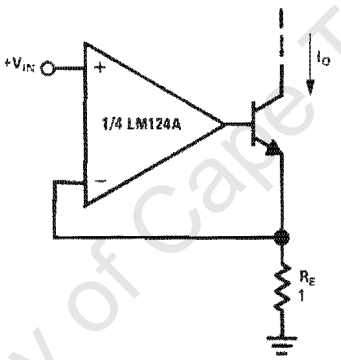
DS009299-16

Pulse Generator



DS009299-17

High Compliance Current Sink

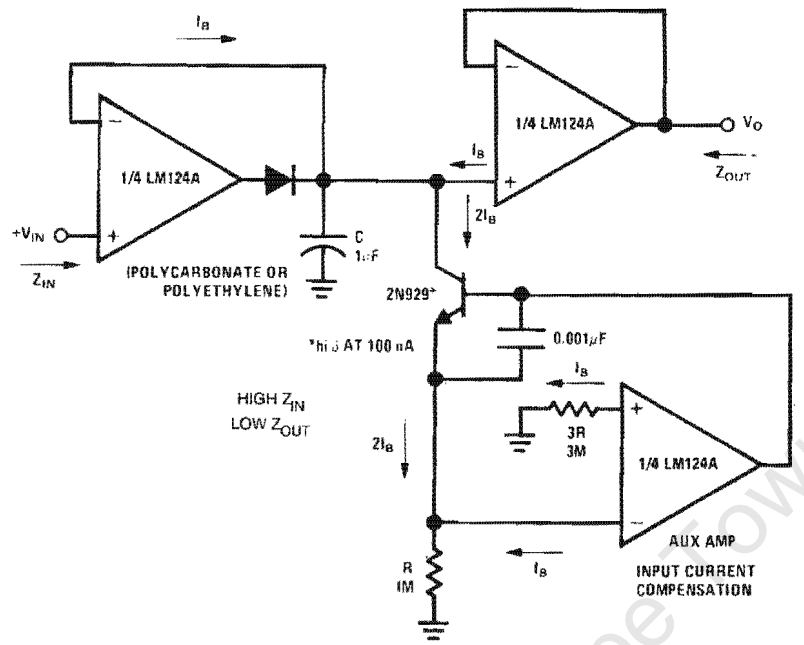


DS009299-18

I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

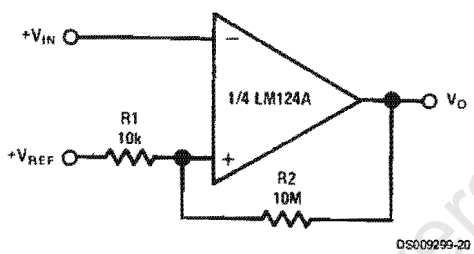
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Low Drift Peak Detector



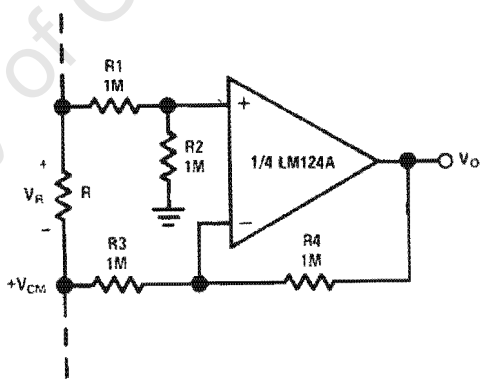
DS009299-19

Comparator with Hysteresis



DS009299-20

Ground Referencing a Differential Input Signal

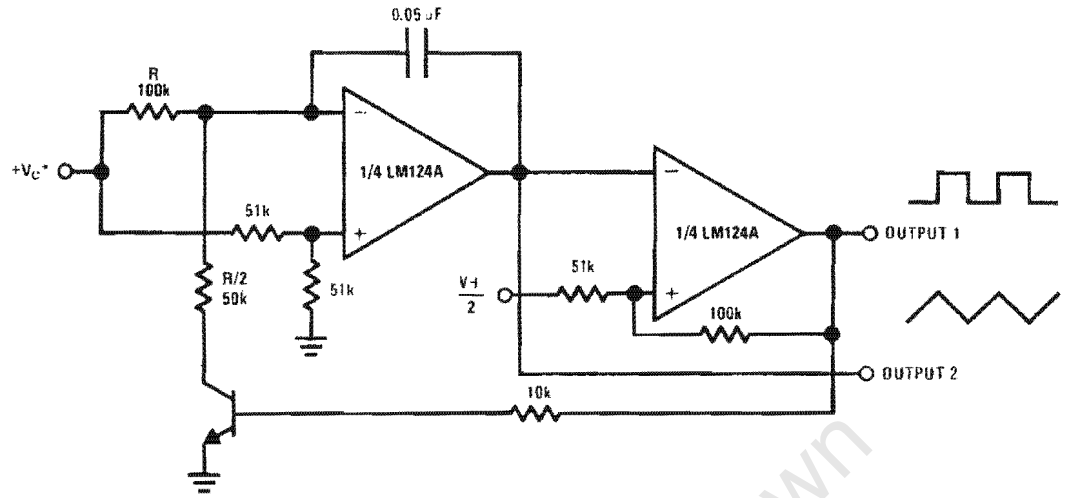


DS009299-21

$V_O = V_R$

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

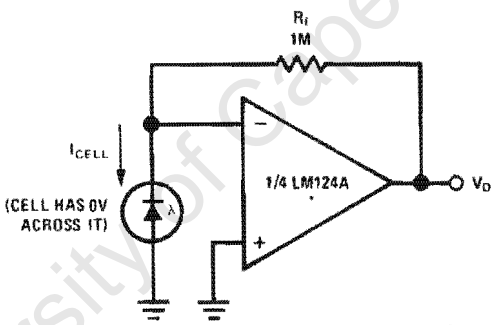
Voltage Controlled Oscillator Circuit



DS009299-22

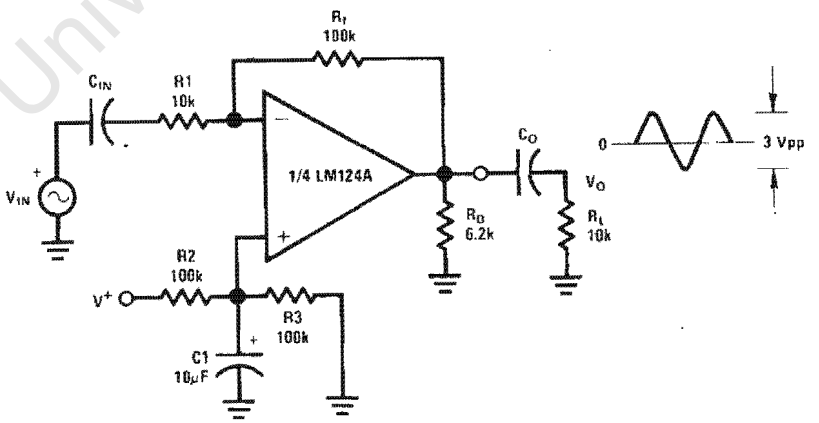
*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5$ V_{DC})

Photo Voltaic-Cell Amplifier



DS009299-23

AC Coupled Inverting Amplifier

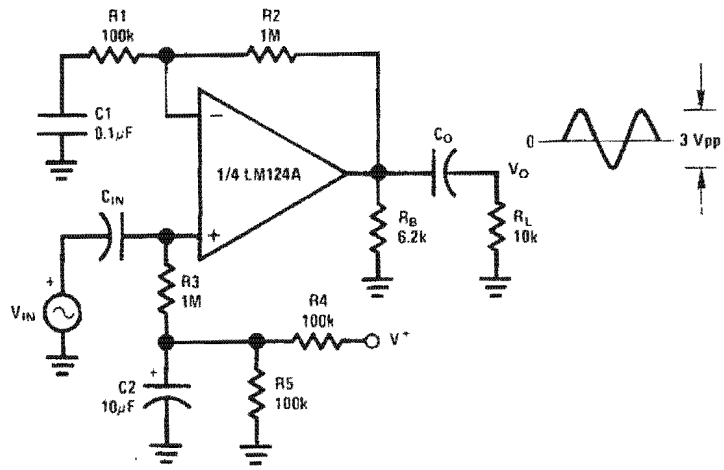


DS009299-24

$A_V = \frac{R_f}{R1}$ (As shown, A_V = 10)

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

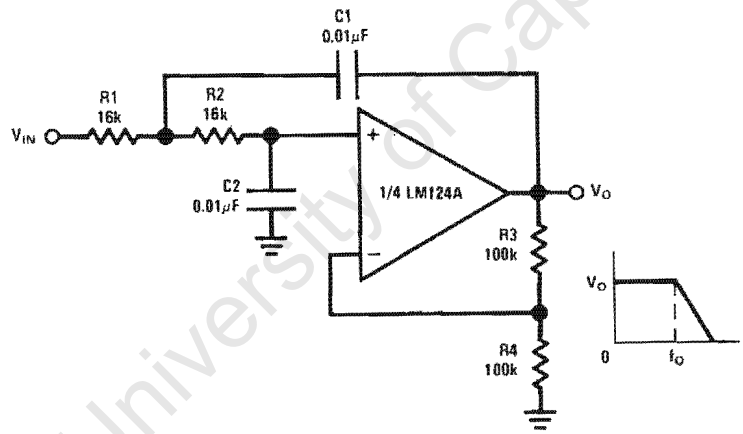


DS009299-25

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As shown)

DC Coupled Low-Pass RC Active Filter

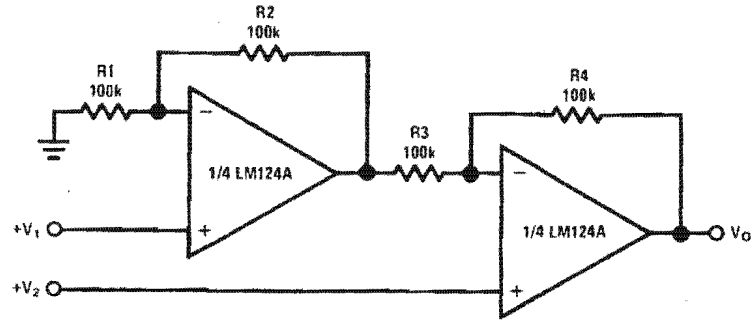


DS009299-26

f_O = 1 kHz
Q = 1
A_V = 2

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z, DC Differential Amplifier



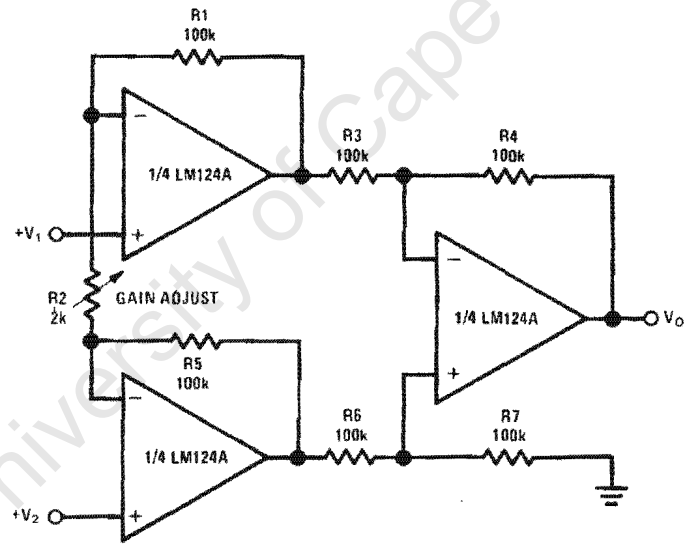
DS009299-27

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



DS009299-28

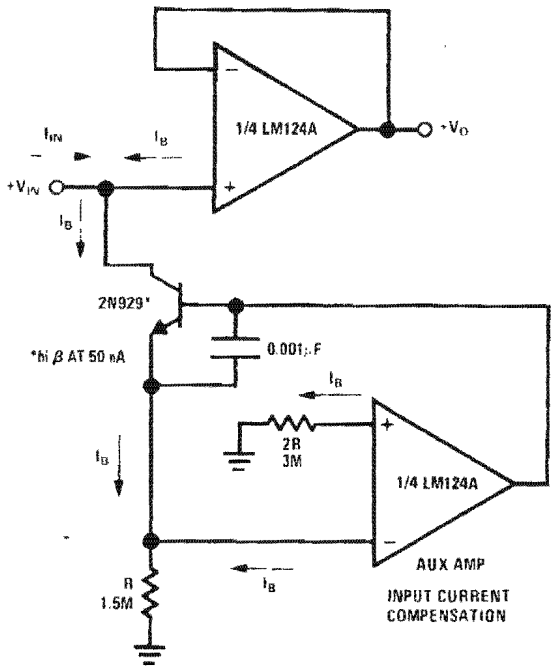
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101 (V_2 - V_1)$

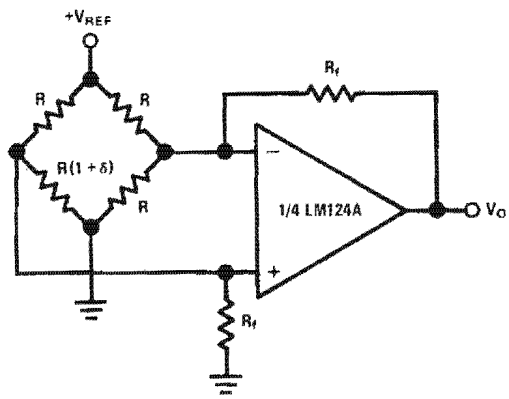
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



DS009299-29

Bridge Current Amplifier

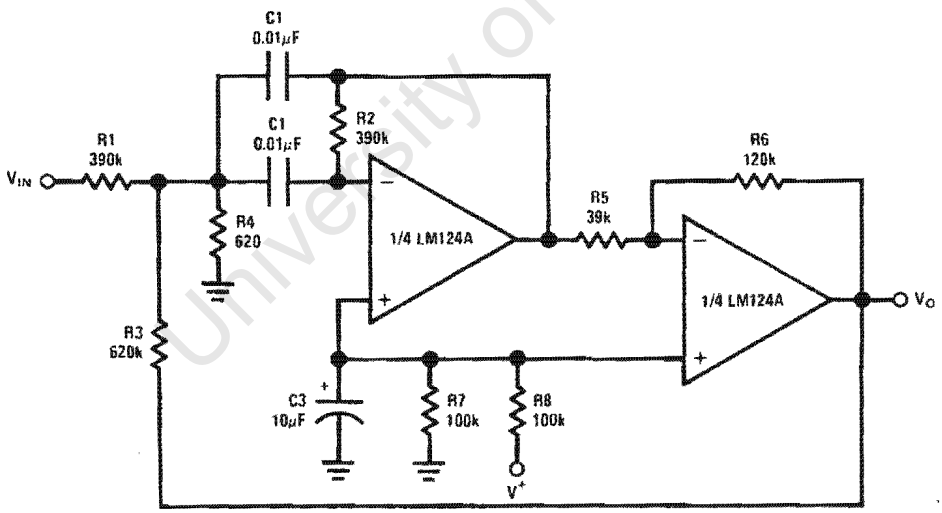


DS009299-30

For $\delta << 1$ and $R_f >> R$

$$V_O \sim V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

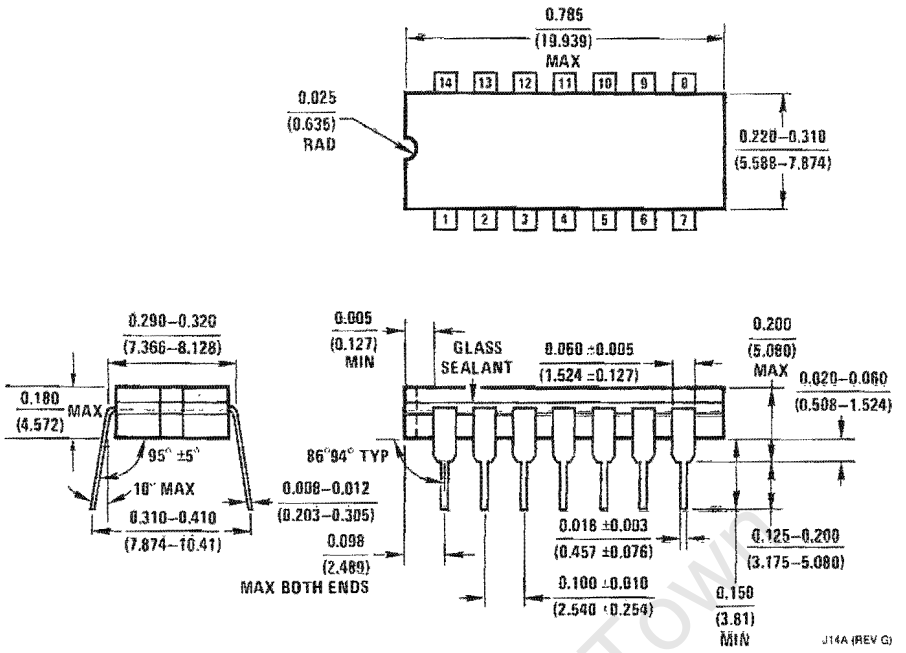
Bandpass Active Filter



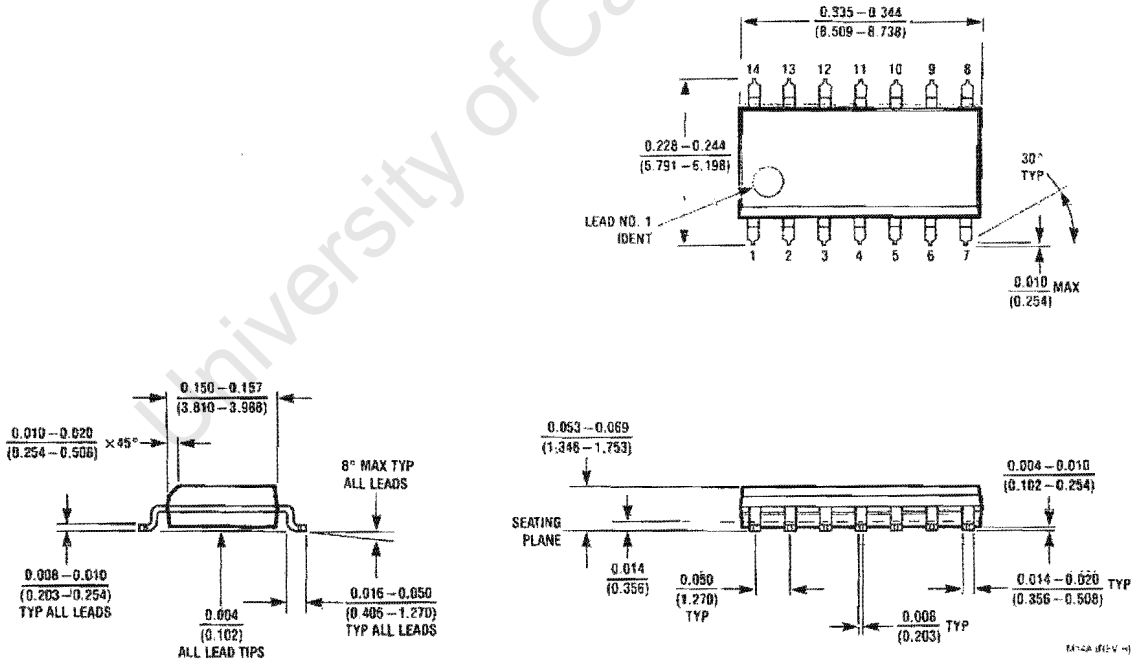
DS009299-31

f_O = 1 kHz
Q = 25

Physical Dimensions inches (millimeters) unless otherwise noted

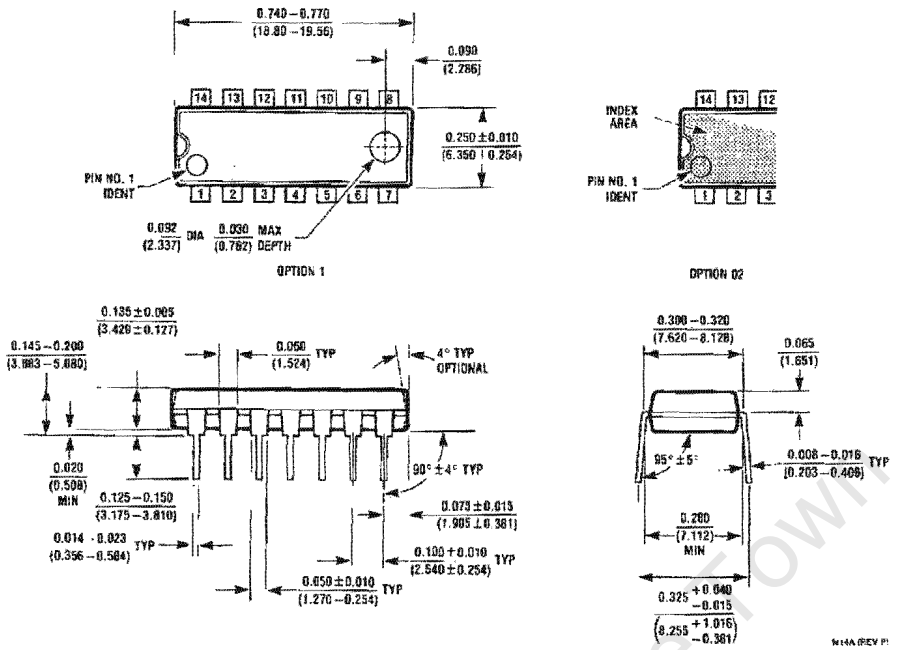


Ceramic Dual-In-Line Package (J)
Order Number JL124ABCA, JL124BCA, JL124ASCA, JL124SCA, LM124J, LM124AJ, LM124AJ/883, LM124J/883, LM224J, LM224AJ or LM324J
NS Package Number J14A

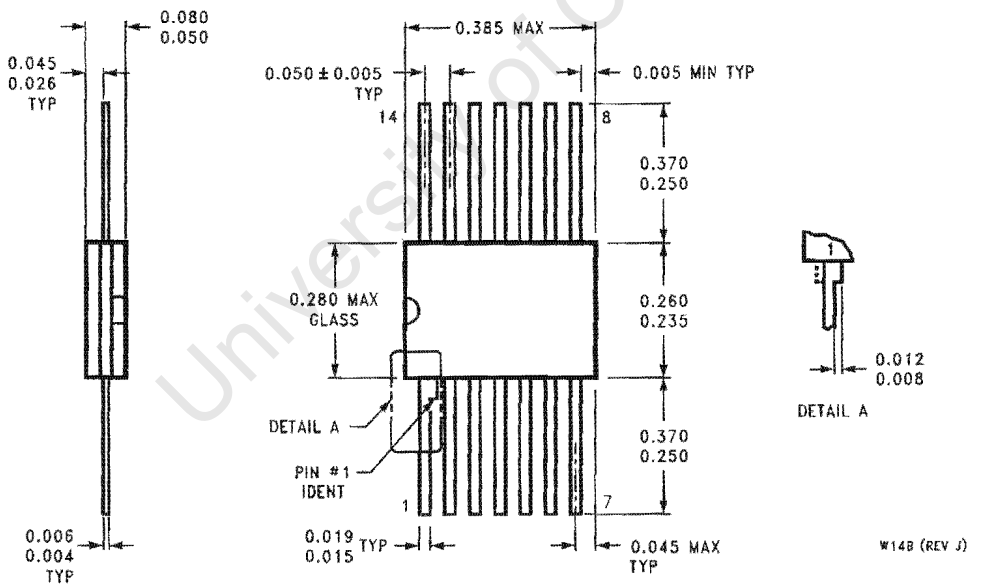


MX S.O. Package (M)
Order Number LM324M, LM324MX, LM324AM, LM324AMX, LM2902M or LM2902MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

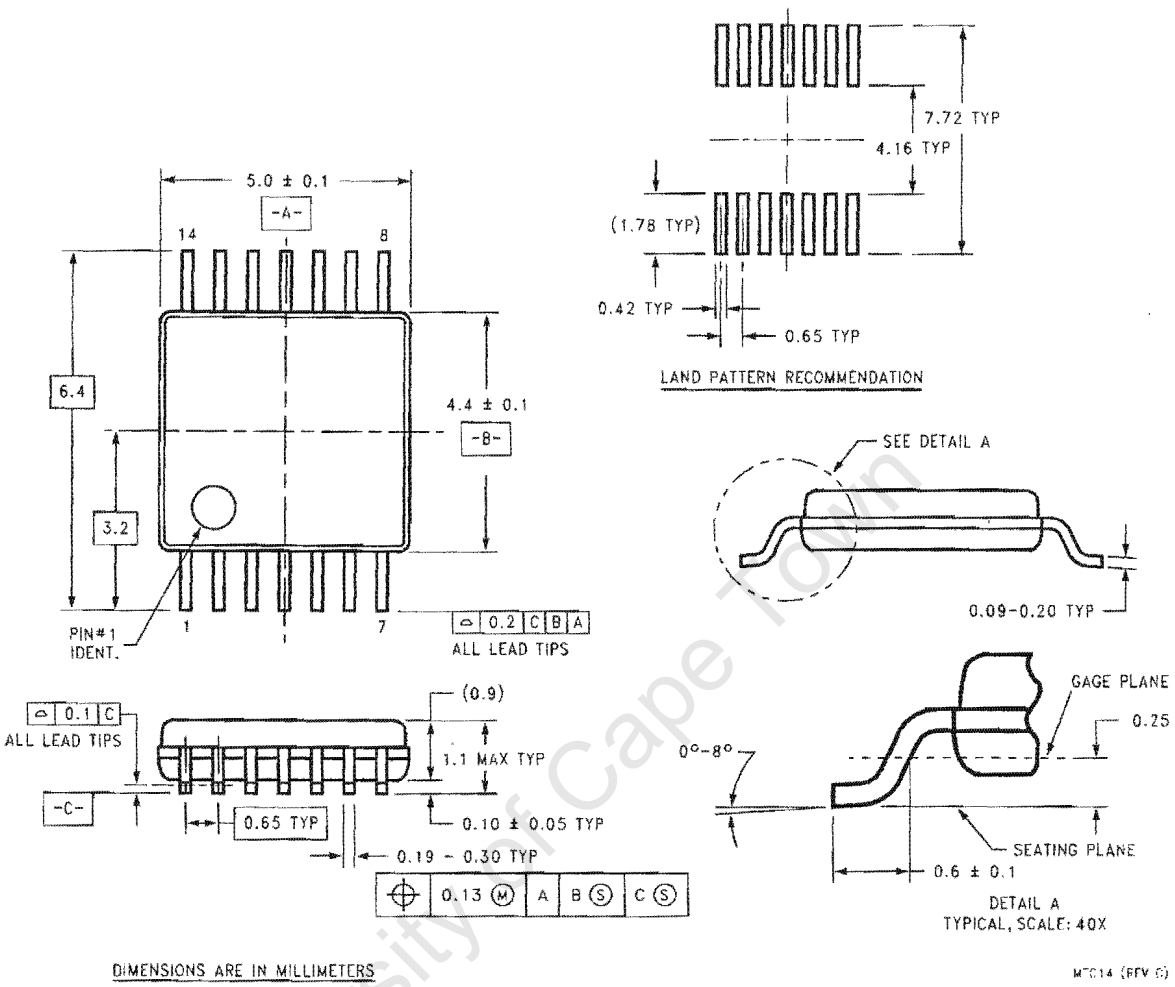


Molded Dual-In-Line Package (N)
Order Number LM324N, LM324AN or LM2902N
NS Package Number N14A



Ceramic Flatpak Package
Order Number JL124ABDA, JL124ABZA, JL124ASDA, JL124BDA, JL124BZA, JL124SDA, LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
NS Package Number W14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin TSSOP
Order NumberLM324MT or LM324MTX
NS Package Number MTC14

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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