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INDUCTION MOTOR DRIVE FOR BATTERY VEHICLE.

BY

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University of Cape Town

## ABSTRACT

- **A 9** phase transistor inverter fed induction motor for a battery vehicle with direct wheel drive is discussed. A **new** method of motor voltage control by pulse width modulation, where the phases are interlaced in a manner **to** conserve continuity of the supply current, is described. In addition to this, a novel construction, **where** the motor and the inverter are built into one compact and economical unit, is presented.

## CHAPTER I

### INTRODUCTION

Despite the numerous advantages of the electrical vehicle, it has not reached any significant percentage of modern day transportation. The lack of suitable means of storing electrical energy has been claimed to be the major drawback. Nevertheless, even with today's technology its wider application could have enormous repercussions towards solving some pertinent questions, such as the energy crisis and environmental pollution caused by the combustion engine.

The momentum of battery research and development is gaining unprecedented proportions and evidence of an imminent major breakthrough is becoming too significant to overlook. <sup>1, 2, 3</sup>

Due to the time lag involved between development of a prototype and mass production it is of utmost importance that areas other than energy storage should be thoroughly investigated now. <sup>4</sup> One area which requires particular attention is the propulsion system. Measurements indicate that vehicle range can double through propulsion systems improvement alone. <sup>5</sup>

This project is particularly concerned in producing a flexible, efficient and cheap drive. The drive is a 9 phase transistor fed squirrel cage induction motor with sufficient torque and flexibility for a direct drive without a gear box or differential. The motor voltage control is achieved by the popular method of pulse width modulation, but with the novel approach of interlacing between the phases. The advantages of interlacing are numerous and solve problems associated with the application of power transistors to inverter fed induction motors. The production of high voltage peaks **and** switching losses are drastically reduced by interlacing, thus enabling the use of cheaper transistors and increase in overall efficiency.

### 1.1 The Importance of Overall Cost

**An** analysis done by the G.E.S. Group in West Germany, which compares electrical vehicles to petrol driven counterparts, has found that series production cost of electric cars is about 11 to 12 times that of its petrol driven equivalent, with operation costs about the same, probably with a slight advantage for the electrical vehicle if a long life version is developed. The above economics might be acceptable to a fleet owner, but surely would not be so tempting for the private motorist.

It is therefore important that more effort should be made to cut down expenses on certain critical areas.

The traction motor accounts for a big share of the cost of electrical vehicles. The D.C. motor used normally is far more expensive than the internal combustion engine, probably because of its limited production.<sup>6</sup> The transmission is another costly item as it normally contains many moveable parts.<sup>7</sup> The possibility of eliminating it should strongly be considered for this reason alone.

If the electrical vehicle could improve its cost by say 25% a major shift away from internal combustion engine would be imminent. In any case as petroleum products increase, the cross over point will soon be reached.

## 1.2 The Importance of Overall Efficiency

The conversion efficiency considered is effectively a system efficiency (i.e. the fraction of power supplied by the battery which is actually available at the wheels). This overall efficiency is comprised of the individual efficiency of several vehicle components, but predominantly by the controller, motor and transmission. While each of these three components may be designed to be highly

efficient, the resulting efficiency is the product of the efficiencies of all three and is not nearly so impressive. Under present day developments it appears that the best overall efficiency is in the region of 70%.<sup>5</sup> Although the battery efficiency is not included in the above defined conversion efficiency, it must be stated that the method of power extraction of the system will have profound influence on the battery efficiency. Any system which takes power from the battery under steady conditions **as** opposed to under pulsed conditions, will increase the battery efficiency. The battery internal resistance **and** supply leads will experience losses in accord with the current square as opposed, to the output based on the average current. The capacitive property of the battery will offset the effect to some extent.

The proposed drive in this project could be optimised **and** overall efficiency as high as 90% should theoretically be possible. The efficiency of a transistor inverter could reach over 97%, especially in the light of reduced effect **of** stored magnetic energy of the inverter and supply on switching losses. The efficiency of the squirrel cage induction motor could be as high as 94%, with special attention paid to low rotor resistance.<sup>9</sup> The transmissions having been eliminated would leave bearings and universal joints only. Maximum mechanical efficiency is

secured if the traction motor or motors are fixed at the wheels and rotate at wheel speed. But as the heavy motor will need to be sprung, the need of a flexible connection such as a universal joint is required. The next option would be to use a high efficient chain drive with little **or** no gear ratio.

The effect of increased efficiency on range is more than simply linearly related to **efficiency as it's improvement** implies less battery weight compoundel with lighter vehicles.. For lead acid battery a formulae is given for range <sup>5</sup> • Range is proportional to efficiency to the power **of 1.325. Thus an increase from 70% to 90% in overall efficiency results in a range of (90/70)<sup>1.325</sup> times as much . That is 40% increase in range.**

### 1.3 The Importance of Regenerative Braking

The basic concept of regenerating is to change the motor into a generator that pumps kinetic energy back into the battery when braking. The major benefit of regenerative braking is, of course, the extended range provided by battery recharge. Theoretical estimates of the amount of recoverable energy range from 10 to 40%, but the maximum obtained in service seems to be about 12%.

Figures like **3** or 4% are more common.<sup>10</sup> **A** secondary

benefit of regenerative braking is the saving on brake wear, a substantial problem with a heavy vehicle such as a battery car. Another advantage is that regenerative braking keeps the electrolyte from forming layers of different acidity within the battery. As a result more of the acid is effectively used in both charging and discharging and battery life and efficiency are increased. Finally, an important psychological effect is to give the car a driving feel like that of an internal combustion engine vehicle, by regenerating slightly as soon as the acceleration pedal is released. Unfortunately, regenerative braking requires a certain amount of complexity of the controller to limit the current and obtain the desired deceleration. The complexity might be a stumbling block in the development of the controller for a prototype vehicle with an induction motor. But in a series production a single integrated circuit (IX) could be sufficient to provide this function in an induction motor which does not require additional power semiconductors or contactors to regenerate.

## CHAPTER II

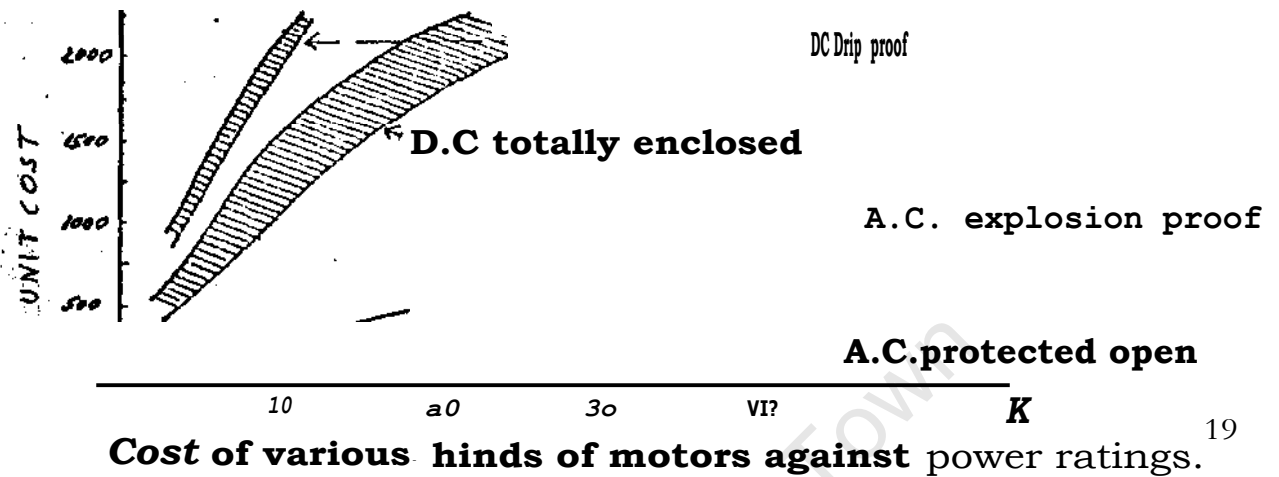
### VARIABLE SPEED INDUCTION MOTOR AND IT'S APPLICATION TO BATTERY VEHICLES

#### 2.1 The Induction Motor as opposed to D.C. Motors

Both the D.C. motor and the squirrel cage induction motor have been proclaimed as suitable for battery vehicles, but because the induction motor requires a variable voltage and variable frequency supply, the cost and complexity of the controller has discouraged a wider application. Nevertheless with the decreasing cost and increasing power handling capability of semiconductors, the inverter driven-induction motor has become cheaper and more powerful. The ability of integrated circuits (I.C.) to replace complex networks has made the controller cheaper and more reliable.

The induction motor is more robust, cheaper, (see Fig.2.1) maintenance free and has a higher power to weight ratio (kw/kg) than the D.C. motor<sup>7,3</sup> - these points should justify the use of the inverter fed squirrel cage induction motor rather than the D.C. system for propulsion of on-the-road vehicles.

FIGURE 2.1



## 2.2 Reasons for a 9 Phase Induction Motor

An induction motor with a large number of phases is the most appropriate kind of motor to provide high torque and smoothness of operation.<sup>12</sup> However the cost, weight and size of the inverter must not be increased substantially.

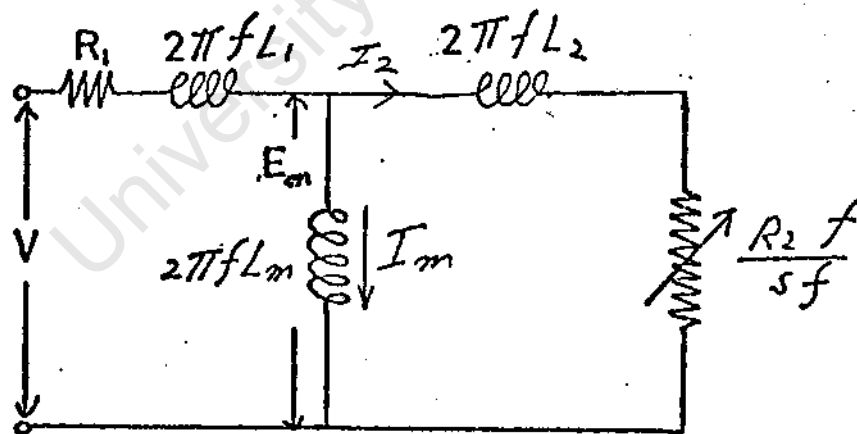
Increasing the number of phases can readily be achieved with a conventional machine winding, having sufficient number of slots, by regrouping the stator coils to provide the necessary number of supply connections.<sup>13</sup> The division of the total inverter rating into a greater number of phases reduces the required current rating of individual semiconductors, so that greater output ratings could be achieved with existing device without parallel operation. The inverter was constructed on the end plate carrying the bearings of the rotor (see constructionChapter 74therefore individual leads are short, off-setting, the cost of the increased number of leads required.

MacLean after investigating the performance of 3 phase and higher number of phase induction motors concludes that inverter circuits producing 3 phase square-wave voltages will produce a low **efficiency** drive, while a example gave almost identical performance figures to a similar sinusoidal fed 3 phase machine.

### 2.3 The Induction Motor Analysis

A per-phase equivalent circuit commonly used to analyse an induction motor is shown in Figure 2.2.

FIGURE 2.2



Equivalent circuit of an induction motor.

The synchronous speed of rotating field,  $N_s = 120 f/P$  is directly proportional to  $f$ , the applied frequency. The frequency of current, in the rotor is ( $sf$ ) the slip frequency. (This can be negative when regenerating).  
 The torque developed can be expressed as <sup>9</sup>

$$T = K_1 I_2 \phi \cos \theta_2 \quad \phi = \text{flux per pole}$$

$$K_1, K_2 = \text{constants}$$

$$\text{where } \phi = K_2 \frac{E_m}{s}$$

$\cos \theta_2$  is the rotor power factor

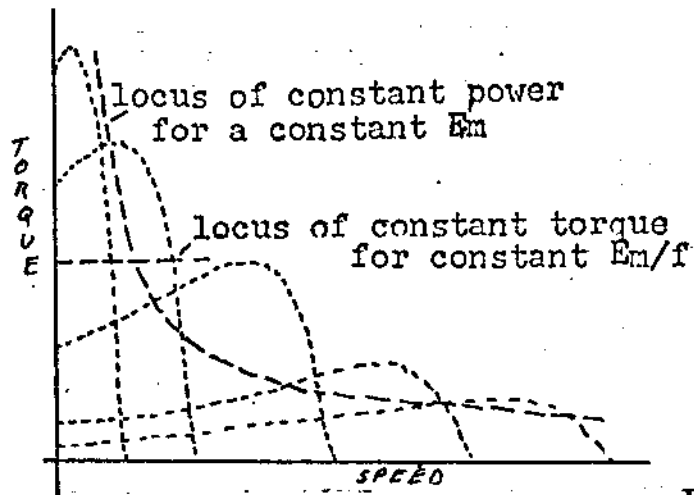
$$\theta_2 = \tan^{-1} \frac{2L_2 \pi (sf)}{R_2}$$

$L_2$  and  $R_2$  are the rotor leakage inductance and resistance

$$I_2 = \frac{E_m}{\sqrt{(2\pi f L_2)^2 + \left(\frac{R_2}{s}\right)^2}}$$

If the back emf  $E_m$  is kept constant for different frequencies the flux is inversely proportional to the frequency. The torque speed curve obtained in this way is sketched in Figure 2.3

Fig. 2.3.



Torque speed characteristic for constant  $E_m$  and  $E_m/f$  <sup>I2</sup>

At higher speeds where  $R_2/s \gg 2/f l_2$  and where the motor is running at small slip (which is normally the case) then the average mechanical power output of the motor is <sup>I2</sup>

$$P_{out} \approx \frac{m E_m^2 s (1-s)}{R_2} \quad E_m = \text{back e.m.f.}$$

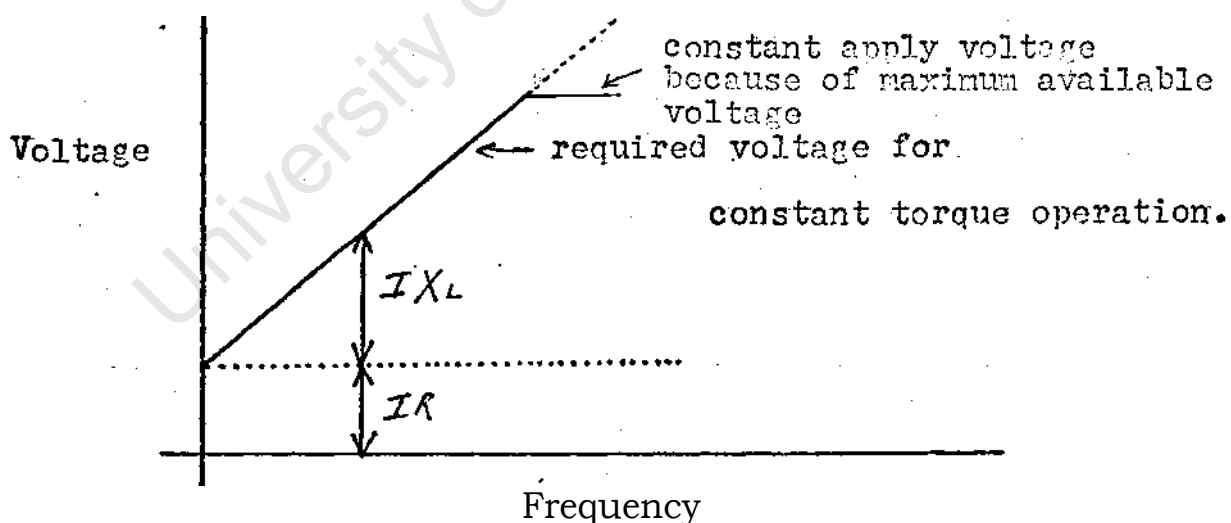
when  $m$  is the number of phases. It is seen that if the slip and  $E_m$  is kept constant the motor will run essentially at constant horse power. Although it is desirable that the average mechanical power output of the motor be approximately constant over a wide range for a given <sup>I2</sup> accelerator displacement, such a characteristic cannot be maintained at very low speeds because of consequent rapidly increasing current. By making  $E_m$  proportional to the speed of the motor at low speeds the current would remain within it's limit and the torque would be constant for a given accelerator displacement. The maximum pull out torque would be obtained when the applied frequency will render the rotor leakage reactance equal to  $R_2/s$ .

A locus of steady state operating points obtained in this way is shown in Figure 2.3 for a particular acceleration pedal displacement.

As  $E_m$  is not an accessible variable, the applied voltage is controlled. If the applied voltage, instead of  $E_m$  is made directly proportional to frequency at low frequencies, the torque is not constant because of the volt drop in the

resistance of the stator. \*winding's which starts to dominate the stator leakage reactance in magnitude. Compensation can effectively be made with a voltage to frequency linear relationship which is offset from the origin as shown in

Figure 2.4-



Required voltage for constant torque.

As an induction motor operates as a slipping clutch the slip frequency must be kept as small as possible by a high flux (high  $E_m/f$ ). Nevertheless, the motor must be kept from over-saturation which results in increase magnetizing current and losses.

## 2.4 Direct to Wheel Drive

The induction motor contemplated is to produce sufficient torque at low speeds so that no gear reduction is required. A, direct drive would therefore imply a relatively low speed motor. Because the squirrel cage induction motor is robust and has no commutator it can run at very high speeds.

Hence a higher power to weight ratio can be obtained (kw/kg) than a D.C. motor. However, with a low speed induction motor this advantage would be lost in favour of the benefits of no transmission at all. It is, therefore, debatable whether the weight of the transmission and mechanical inefficiency is more unfavourable than a heavy and more expensive low speed motor. In the case of a D.C. motor the argument brought forward by pro-transmission people is that the motor draws heavy current to produce high torques at low speeds, and therefore reduces the range. The described interlaced induction motor with **it's** ability to produce high torques with drastic reduction in supply current compared to conventional motors destroys this convincing argument. (see chapter 1! ). The heat losses dissipation within the motor will however be favoured less than with low speed motors. Forced cooling **will** be required, especially when driving up steep grades **for** extended periods. In any case, this is normally needed in transmission type electrical vehicles.

The mechanical transmission losses account for as much as 10% of the power produced in conventional drives (see appendix 11), **and** substantially reduces the benefit of regenerative braking. The **range** reduction would therefore be over 10%, especially **in town driving. This could be** translated in at least 10% increase in battery weight and electrical cost.

**A** further point is the differential action required between the traction wheels. A separate induction motor **on** each traction wheel, which all run at the same air gap frequency has this inherent characteristic. The traction force is only applied to the wheel which has grip to the road surface as the torque drops very quickly- with little increase in speed. A single stator construction with two rotors which can freely rotate could be another solution which would reduce the overall ratio of overhang copper to active copper. It must be noted that when cornering the faster wheel must not go into negative slip as the braking action would affect steering.

Reversing with an induction motor is simple and does not require a heavy contactor or gear, as in the case of the **D.C.** motor. Reversal is obtained by reversing the phase sequence to the inverter, which is obtained at the lowest power level.

## CHAPTER III

### THE 9 PHASE INTERLACED INVERTER

#### INTRODUCTION

In this Chapter the method of power conversion from D.C. to A.C. power for the proposed motor is presented. The 9 phase inverter consists of 9 conventional single phase full bridge inverters. The single phase bridge is first dealt with, to describe the basic switching action. The principle of interlacing between the 9 phases is then discussed and finally the logic control for the transistor switches. The transistor was chosen as the switching device.

#### The Single Phase Full Bridge Inverter 17

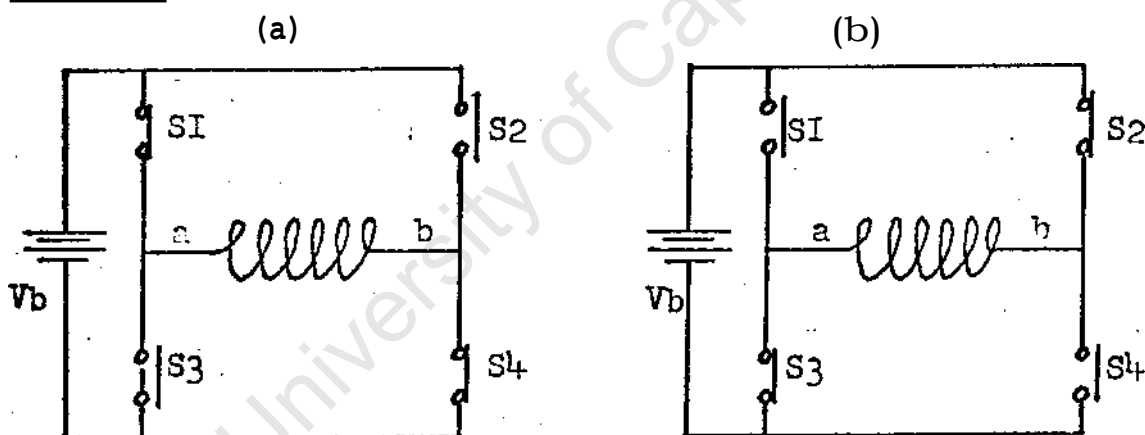
##### 3,1,1. The Basic Switching Action

To convert the D.C. voltage supply to an A.C. voltage, a modulation or switching device must be contemplated. A modulation of the voltage can be obtained by switching a phase progressively, however the difference of the supply and phase voltage results in excessive power losses in the device. Although a sinusoidal voltage waveform is ideal for an efficient operation of an induction motors

the production of sinusoidal voltage waveform by modulation of the supply would be intolerably inefficient and impractical. An A.C. voltage waveform of a square or quasi-square waveform nature is therefore produced by "fast" switching. The ideal switching action would be an instantaneous one which would result in no loss.

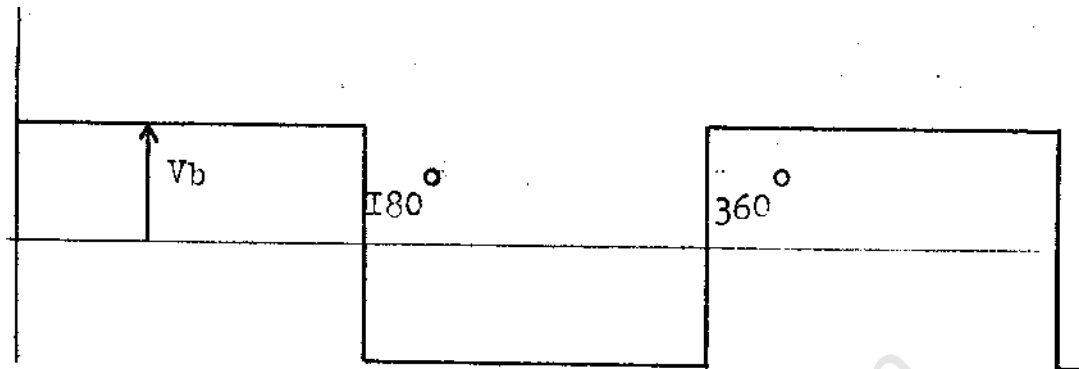
The basic switching action for a square voltage waveform is illustrated in Figure 31a and 31b :

FIGURE 1.1.



Single phase bridge inverter switching sequence to produce a square voltage waveform.

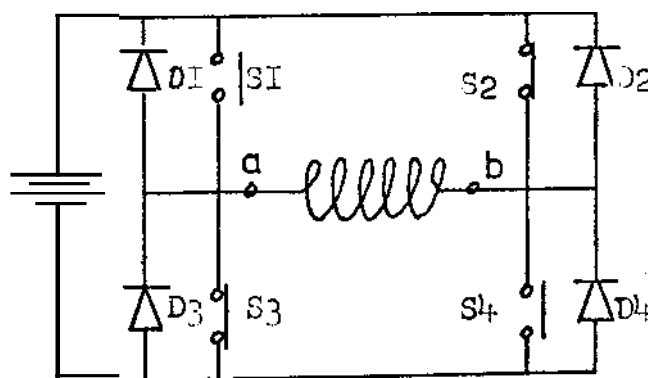
The switches S1 and S4 are controlled to connect a to the positive line and b to the negative line for half the positive cycle. The negative cycle being produced in a similar manner by S3 and S2 the resulting waveform is shown in Figure 2.

FIGURE 3.2'

Single phase square voltage waveform

An induction motor always runs with a lagging power factor. An alternate path for the current, which must still flow when the voltage is removed must be provided. Hence the need of diode D1, D2, D3, and D4, see

Figure 3.3 The freewheeling diodes are arranged to enable reactive load energy to be circulated and regeneration into the D.C. links to take place.

FIGURE 3.3

Single phase full bridge inverter with freewheeling diode

For example at the end of the positive cycle S1 and S2 are switched off, current which has been flowing through the load from a to b will continue to flow through D2 via the supply and back through D3, Although S3. and S2 will then be ready to conduct they will remain idle until current in the a to b direction has ceased. Only then will the negative current cycle start. It must be noted that there is a time during each half cycle when the inductive load feeds back power to the D.C. supply source.

A quasi-square waveform is obtained in a similar way, but one of the conducting switches of the above is turned on for a shorter interval. S2 and S3 were chosen to be switched for a shorter interval. S1 and S2 could have just as well been chosen. The switching sequence for a conduction angle of  $160^\circ$  is given in Figure 14. The conduction angle being the time during which both switches of a particular half cycle are on.

The resulting voltage waveform is shown in figure 3.5. With an inductive load, current will again lag the voltage but the lagging current will not necessarily need to flow via the supply as with the square wave inverter (e.g. when S4 is switched off, current will flow through D3, the positive rail and back through S1, only when S1 is also disconnected will the current return via the supply

FIGURE 3.4

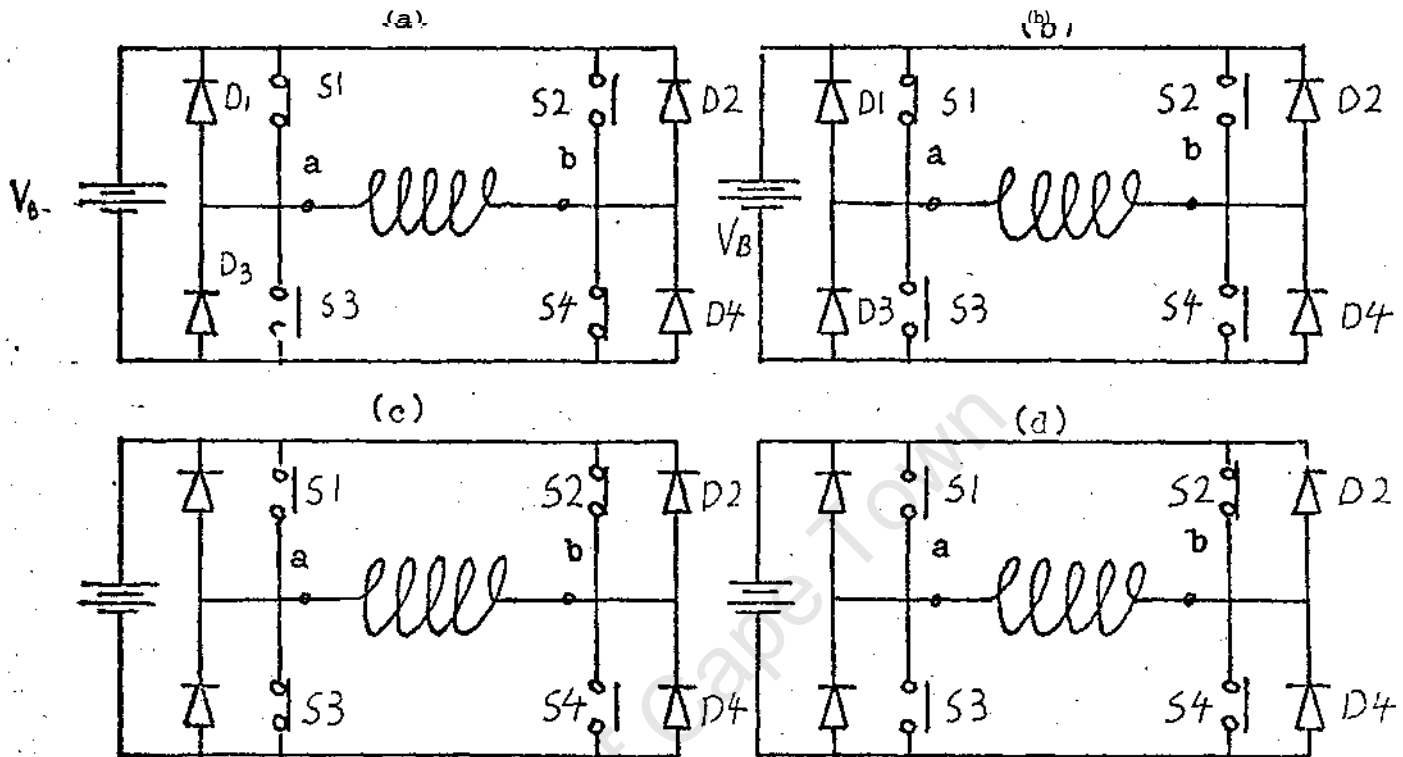
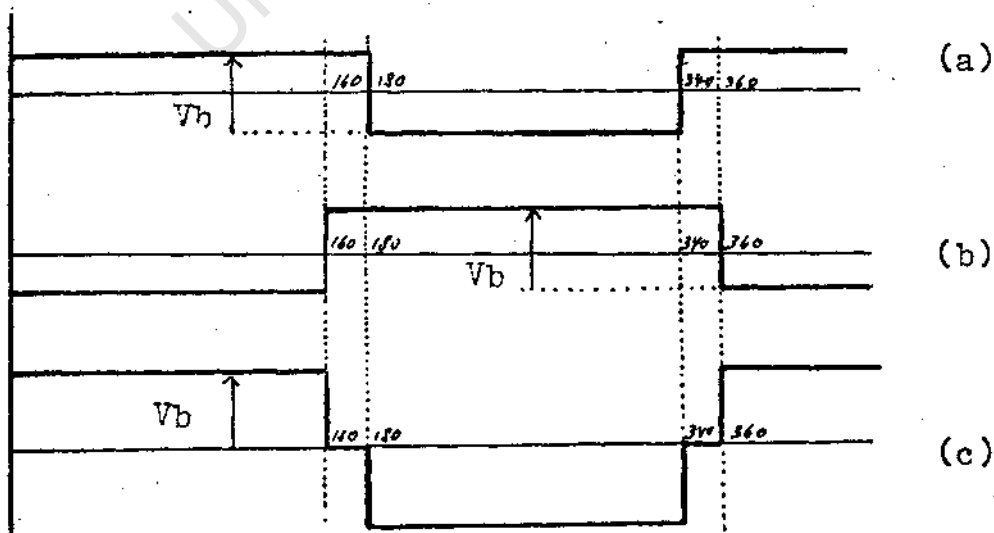


Figure 3.4 (a)  $0^\circ - 160^\circ$  (b)  $160^\circ - 180^\circ$  (c)  $180^\circ - 320^\circ$  (d)  $320^\circ - 360^\circ$   
 -Single phase. full wave inverter-bridge-for-a quasi-square voltage waveform with  $160^\circ$  conduction angle.

FIGURE 3.5.



(a) potential of terminal a of figure 3.4. (b) potential of terminal b. (c) potential difference between terminal a and terminal b

### 3.1.2. The Voltage Control

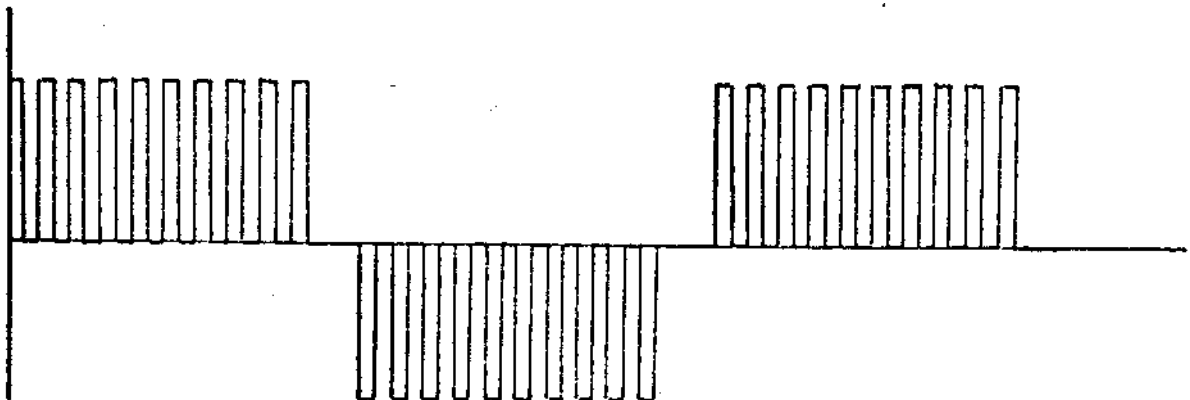
Most inverters require a means of voltage control because of variation in the inverter source voltage, regulation within the inverter and most of all because a variable speed induction motor requires a variable frequency as well as a variable voltage. This is necessary to obtain control of the air gap flux so as to operate the induction motor in an efficient and flexible manner.

The quasi-square voltage waveform described, has a fixed fundamental voltage amplitude for a particular conduction angle. The harmonic content of the inverter phase voltage is given in Appendix B. It can be seen that the fundamental voltage amplitude can be reduced by narrowing the conduction angle. But this is not a practical voltage control as the amplitude of the harmonic voltages can approach the magnitude of the fundamental voltage. Therefore this mode of voltage control must be discarded.

A very popular method of controlling the voltage in inverter is pulse width modulation, where many pulses occur during each half cycle of the fundamental frequency. This is obtained by switching on and off S3 or S4 during the positive or negative cycle respectively.

When S3 or S4 are switched off current will cease from or to the supply (depending whether motoring or regenerating) and the existing current in the load will circulate by means of diode D1 or D2 (see Figure 3.3). This current will decay or rise depending on the time constant of the phase, the combined volt drop across the transistor and diode concerned, and the voltage which may be induced within the motor phase itself. When S3 and S4 are again switched on current will again flow from or to the supply and will rise or decay depending on the supply inductance, resistance, the supply voltage, the transistor voltage drop concerned, the phase time constant, and the induced voltage. The intermediate time is the commutation time. It will depend on the speed of the semiconductors as well as the inductance and capacitance within the semiconductors and the connecting limb concerned. The voltage waveform obtained by the above pulse width voltage control is shown in Figure 3.6

FIGURE 3,6



Chopper modulated voltage waveform

The ratio of the on time to the off time is known as the mark-to-space ratio. The effective voltage is controlled **by** varying the mark-to-space ratio, as the motor phase integrates the applied voltage over a half cycle.

### 3.2 The Principle of Interlacing

The principle behind interlacing between the phases is to **keep** the supply current from the D.C. source as continuous **as** possible. The rule which applies is that a transistor **is** always switched on when another is switched off.

Supply current will transfer from say coil 1 to coil 2, without supply disruption, if and only if the current is equal in magnitude and in the same direction.

Aquasi-square waveform with 160° conduction angle,, enables one whenfleteDping", the provision of 9 phases and 40 displacement, so that a phase is always switched on when another is switched off (see Figure3.8). However, when "stepping", that is at the beginning of the half period of a phase, current which is still flowing in the opposite direction to the applied voltage (since lagging power factor) cannot assume an immediate reverse direction or magnitude. Hence the off going phase will have to regenerate the whole or part of it's current to the supply. Therefore there will be a certain amount of discontinuity

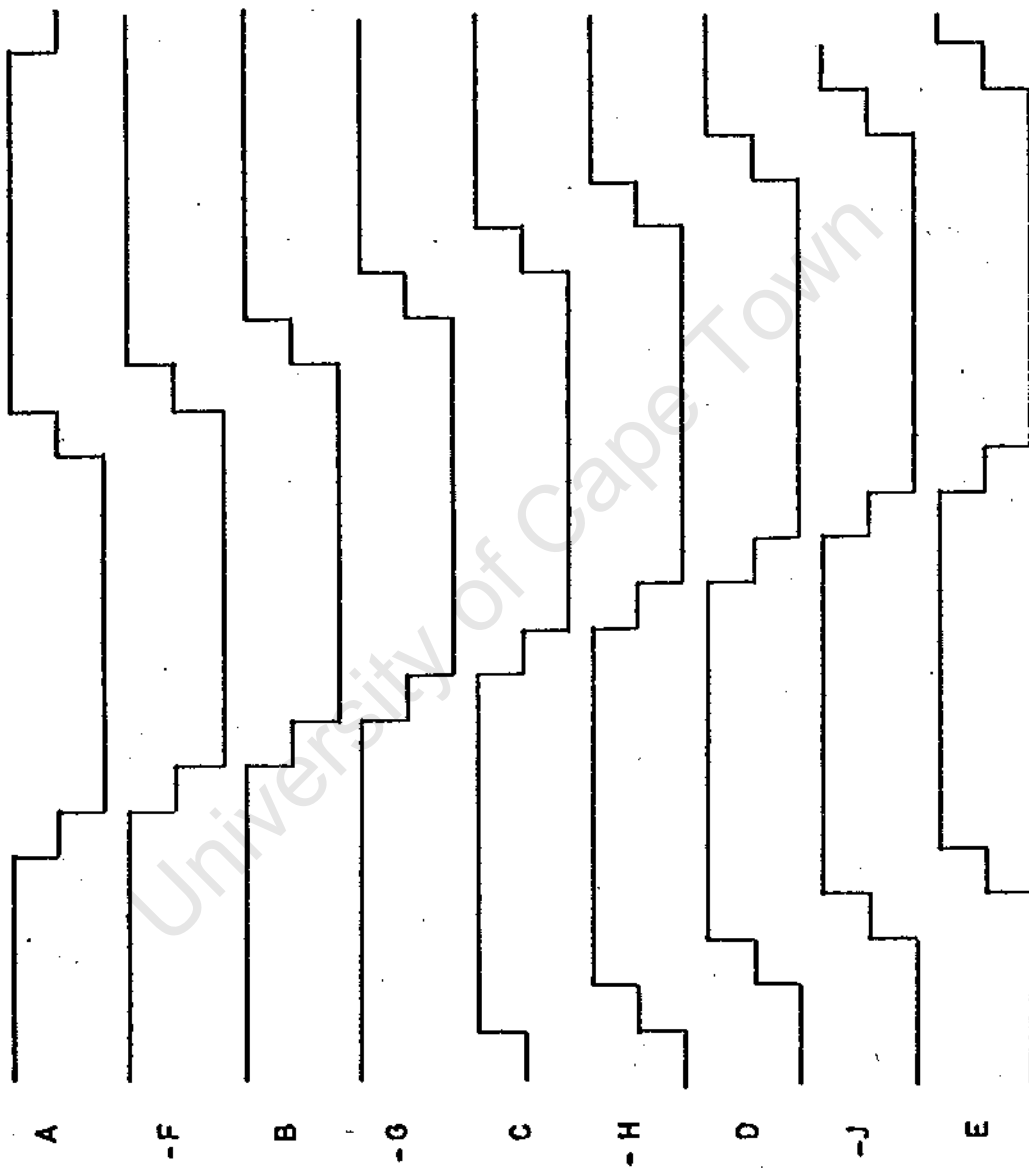


Figure 3.8 Voltage waveform of the 9 phase with  $160^\circ$  conduction angle at full M/S.

in the supply current at the beginning of each phase voltage period. It will fortunately only consist of one eighth of the total supply current (see Figure 3.5). In the case of chopper modulation it is different. Virtually complete continuity of the supply is achieved, apart from the abovementioned current disruption, which exists at the beginning of each phase voltage waveform. Pulse width modulation is normally applied by loughing on and off all the phases simultaneously. This would defeat the idea of switching on a phase when another is disconnected. Hence the phases are not simultaneously chopper modulated. But the chopper modulation is phase displaced, so that a phase is always connected to the supply when another is disconnected. The supply current will be virtually continuous between pulses, provided the 'chopping' frequency is high enough, not to permit the current to decay appreciably during the off period. When a phase is disconnected, the current simply comutates to another as long as the existing current in the latter is virtually the same as the first. Interlacing as described, can be obtained for 8 discrete mark-to-space combinations. Figure 3.9 demonstrates the above principle for a four-eighth mark-to-space ratio. Notice how for any particular time a switching off operation always corresponds to a switching on somewhere else. For, e.g.  $t_1$  time  $t_1$ ; phase F is switched on while phase H is switched off, the same at time  $t_2$  for phase E

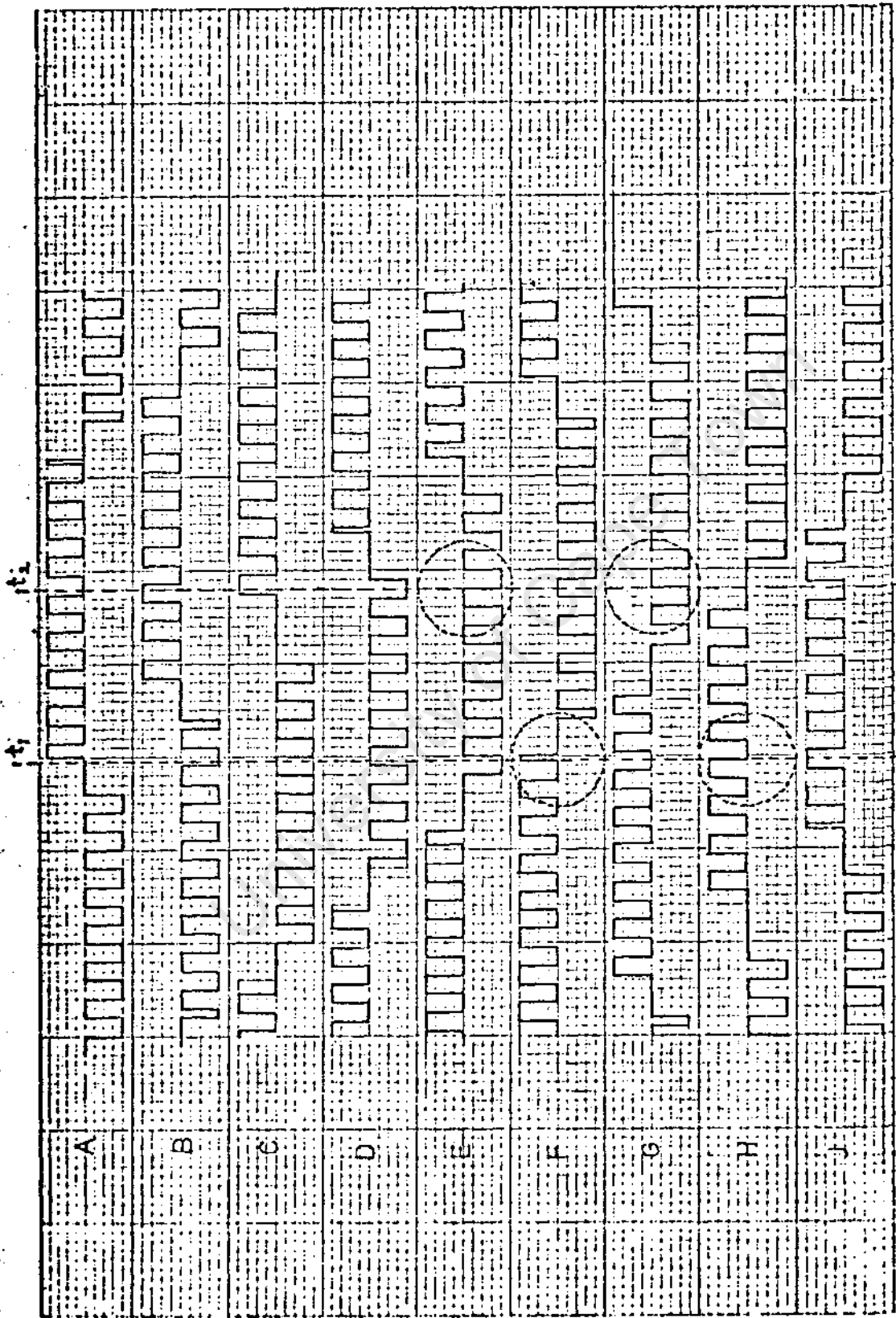
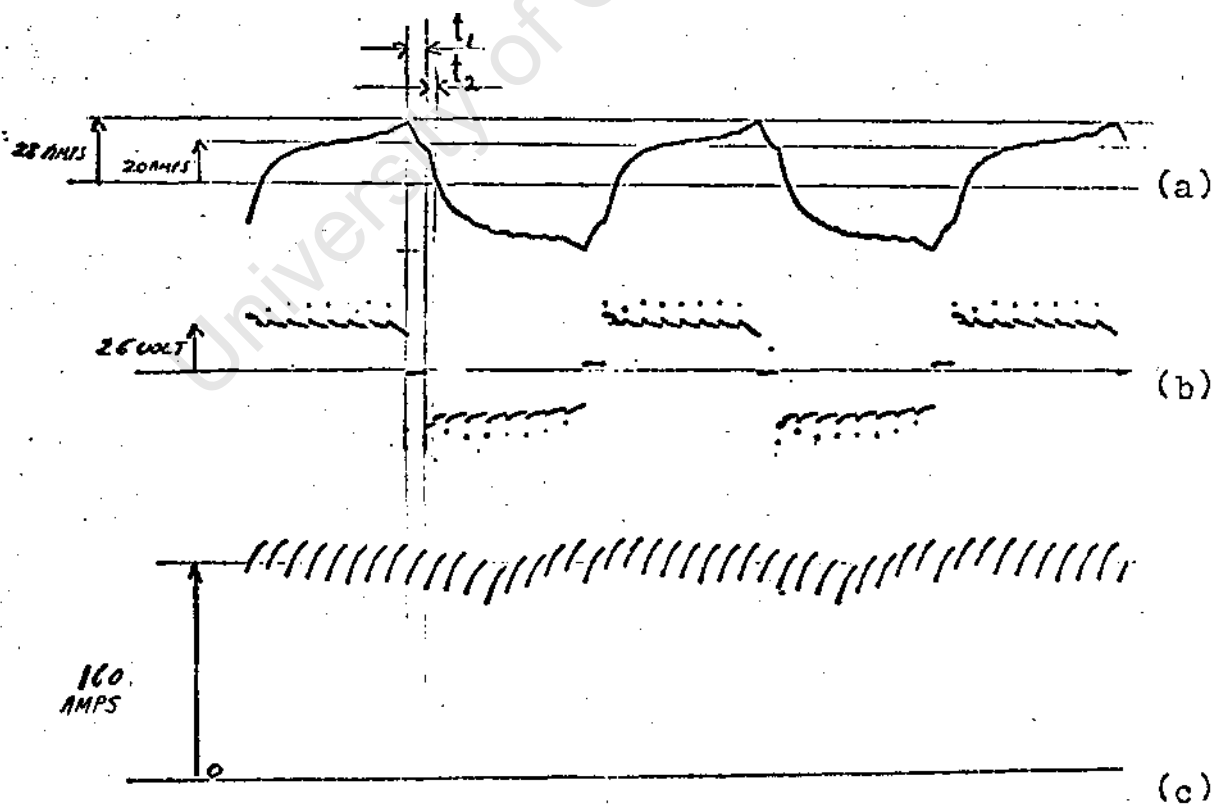


Figure 3.9 Voltage waveform of the 9 phases at 4/8 M/S.

The quasi-square waveform provides a means of circulating part or all of the lagging current, depending on the power factor of the load. It is obvious that less losses will result if this current is to be allowed to circulate within the inverter rather than the supply, especially with a battery where the charge discharge cycle is at the best 80% efficient.

Figure 3.7 illustrates how the current lags the voltage. Two distinct lagging periods are observable. One where the current circulates within the inverter ( $t_{in}$ ) one where it regenerates to the supply ( $t_a$ ). The oscillations in the motor were obtained with the motor described in appendix G

**FIGURE 3.7**



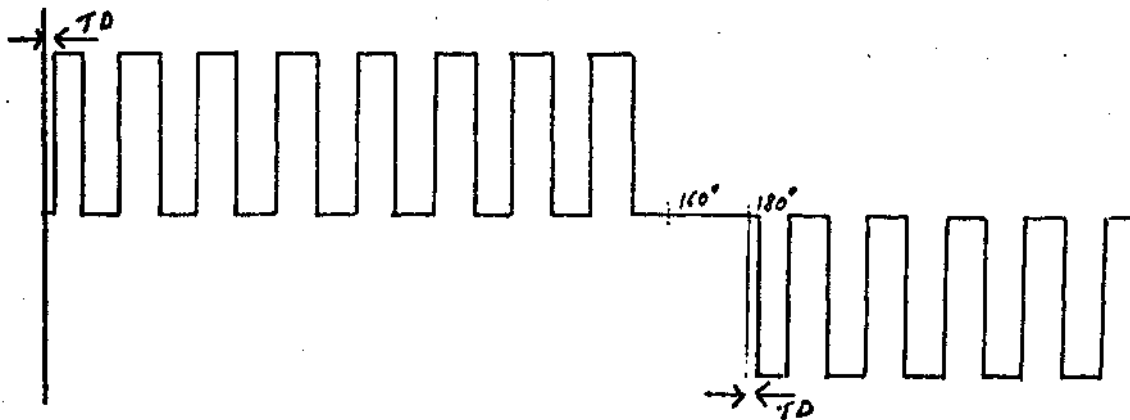
Oscilloscope photograph of a) phase current in the 9 phase inverter  
 b) phase voltage c) supply current from battery.

### 3.3 Time Delays Prevent Problems

Unless special preventative techniques are used in the bridge inverter, it is possible that all legs of the bridge will conduct simultaneously during the finite switching duration. When this occurs, a potentially destructive current is drawn which is limited only by the transistor beta. This condition can be prevented if a time delay is introduced at the first positive going edge of the signal controlling S3 and S4 switches.

**The** voltage waveform, for a particular phase full bridge inverter is shown in Figure 3.3. The output of the inverter is a quasi-square waveform with  $n \times 8$  chopping pulses per cycle. Notice how the beginning of pulse S3 and S4 are delayed by a finite amount. The logic will therefore require to incorporate this delay for smooth operation of **the** inverter.

**FIGURE 3.8**



**Quasi** square voltage waveform with 4/3 Y/S ratio and front edge delay

## CHAPTER IV

### THE TRANSISTOR AS A SWITCHING DEVICE IN THE PROPOSED INVERTER

Some very important areas of application and circuit adaptation of the transistor are discussed in the following subsections. Reasons are given for the choice made in the design of the inverter.

#### 4.1 The Power Transistor As A Switch

High power transistor were used to perform the switching function of Section 3.1 and 3.2. Figure 4.1 shows the transistor Darlington configuration to provide switches S1, S2, S3 and S4 mentioned in **the** single phase full bridge inverter of Section 3.1 and 3.2. Figure 4.2 shows how all the transistors are arranged to provide **the** 9 phase inverter which essentially consists of 9 single phase **full** bridge inverter. The freewheeling and regenerative diodes **are** also shown. The diodes are Motorola diodes M.R. 702. **The** positive rail transistors are PNP (S1, S2) types and **the** negative rail NPN (S3, S4). The power transistors **used** are the Motorola MJ802 and MJ4502. The driver transistors are the 2N3055 and 2N5530 – the design criteria **are** given in Appendix C: The interface between the Darlington and the logic is given in Appendix D.

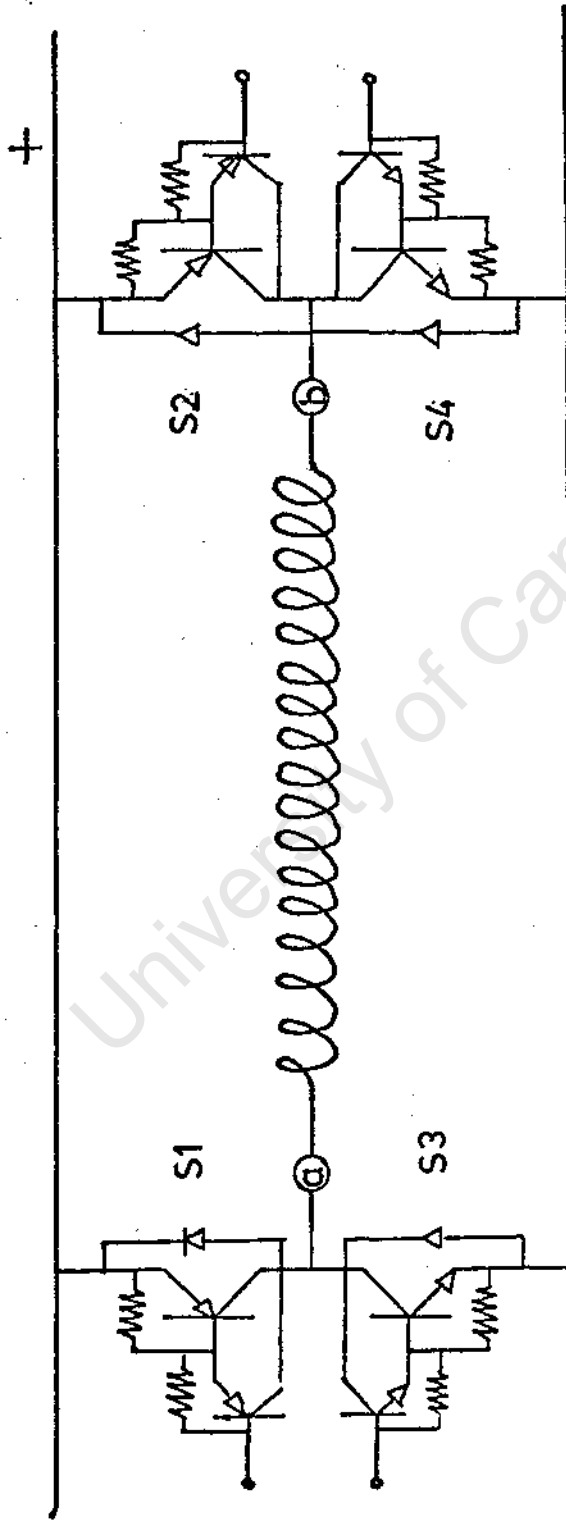


Figure 4. Transistor Darlington pairs which implement the switching function of a single phase full bridge inverter.

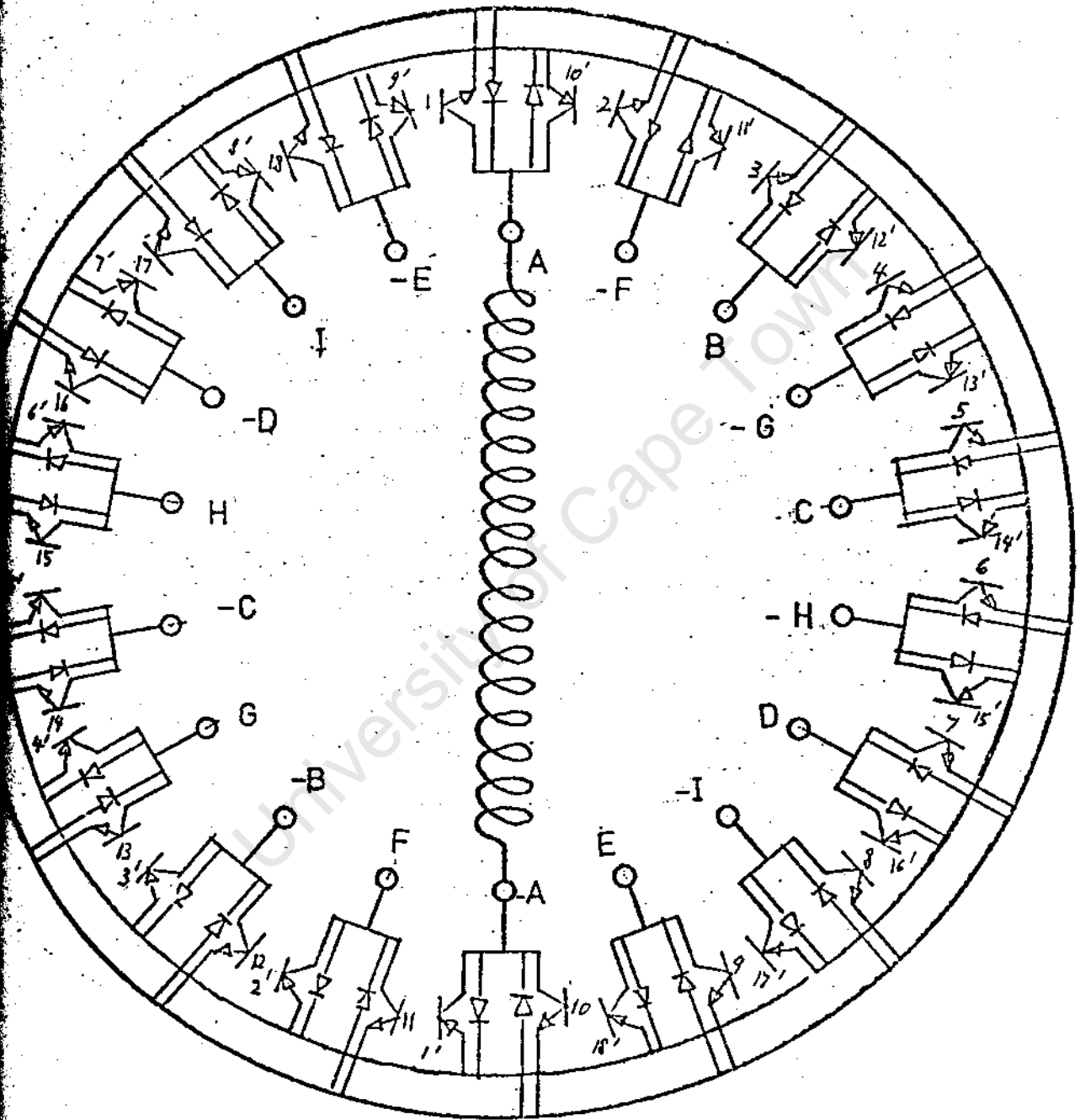


FIGURE 4.2 The power transistor arrangement to provide a 9 phase inverter. Only one phase winding is shown for the sake of simplicity

### The Transistor or the Thyristor

In this particular application where it is required to have 36 switches it is obvious that the transistor with its absence of a forced switching circuit is more economical, although the cost of the transistor exceeds that of a thyristor..

Other advantages to be credited to the transistor are low conduction forward drop,<sup>18</sup> low switching loss,<sup>8</sup> low reaction time (short circuit protection possible),<sup>19</sup> high chopper frequency possible<sup>20</sup> (reduction of current ripple through motor), and less parasitic phenomena (e.g.  $dv/dt$ ), automated mass production is possible, and more compact and lighter weight of the drive is possible.<sup>8</sup> SPCA construction Chapter 7

\*However, on the debit side, the transistor has very little overload capacity, as there is only a small difference between a transistor overload rating and steady state rating, due to the thermal capacity shortfalls. A thyristor can easily be protected with a fast H.R.C. fuse,<sup>17</sup> **but** this is not the case for a transistor. The voltage **rating** of a transistor is not yet comparable to a thyristor,<sup>20</sup> and the transistor requires a constant gating current.

Thus, if the principle disadvantages can be eliminated, or the circuit adapted, the power transistor becomes the ideal component for the 9 phase interlaced inverter drive.

#### 4. .3 Paralleling Transistors

If a three phase inverter is to be used, it is necessary to parallel transistors as existing high current transistors are at present still expensive. On the other hand, with the 9 phase inverter sufficient power is obtained with single transistor in each limb of the inverter. The 30 amp transistors used are comparatively cheap, for their 30 amp peak collector current.

Several aspects must be taken into consideration before attributing more merit to either type of inverter. When paralleling provision must be made for proper power sharing as a current hogging transistor could carry more current than it can handle and fail, . therefore leaving the full load on the remaining paralleled transistors, which in turn all fail, One way to compensate for this unequal power dissipation is to select components for their  $V_{be}-I_c$  characteristics, but this causes transistor stocking and replacement problems. Another solution, emitter

sharing resistors reduces collector current differences between transistors by making the drop across the transistors large compared to the  $V_{be}$  differences for their respective transistors. This however introduces more loss, in the switches and is therefore inefficient. Reverse biasing of the base of the transistor during turn off reduces mismatch in turn off times and storage times, and at the same time there is a decrease in the switching power loss. However, reverse biasing also introduces the problem of reverse biasing secondary breakdown, which may in turn, reduce the sustaining voltage of the transistor. Current sharing within 5% without selection or additional **circuit** is obtained if the transistors are mounted on a **common** heat sink and a current not exceeding typically 15 amp, and at the most 20 amp for a 30 amp transistor. Such inverters with power rating up to 50kw can be designed and leaving a margin of over-current possibility. However, the single transistor per leg would offer a better specific overload possibility per transistor, as peak current could approach maximum **permissible** collector current, as there is equal current **division** between the transistors.

The multiplicity of phases requires more end connections to be brought out, therefore increasing the cost.

However, this was alleviated by placing the transistors on the end plate of the motor, which carry the bearing.

See fig. 7,5 of Chapter 7

Assuming that the above advantages and disadvantages do not favour either systems, the balance tips in favour of the nine phase interlaced inverter system. When considering the avenues which open with a 9 phase system as opposed to a 3 phase. Some of these are

- (1) reduced harmonics in the air gap flux hence losses and torque pulsation reduction) 13
- (2) intermodulation

#### 4.4 Transistor Breakdown Mechanism

Apart from the maximum current rating  $I_{c\ max}$ , the maximum peak current rating  $I_{cm\ max}$ , the breakdown voltage with base open circuit  $V_{ceo}$ , the breakdown voltage with base shorted to emitter  $V_{ces}$ , the dissipation rating  $P_{tot}$ , another important limitation is secondary breakdown .22  
Secondary breakdown occurs as a device is being turned

off to block high voltages, when imperfections in the device structure cause the current flow across the collector base junction to be unequally distributed. This leads to current crowding, resulting in hot spots that present an even lower than average resistance and hence enhance the problem.<sup>23</sup> Damage is caused by the subsequent high, dissipation, and as the damage area grows, a complete collector short results.

The constraint upon the operating region of a transistor defines the safe operating area (abbreviated to SOAR) for a device. The SOAR of the MJ802 and the MJ4502 used in the inverter is shown in **Figure c..2 of Appendix C**. Note that at 60V and 25 amps the device must be switched off within 10/ $\mu$ s to survive. It should be noted that Maximum ratings are not normal practical operating values. Especially considering that 25 C is an almost universal standard, which is a completely unrealistic temperature for power semiconductors.<sup>22</sup> Ambient temperature in the typical power assembly can easily run to 80 °C. Because most specified operating areas are unrealistic and almost never fit ones particular needs it is recommended that transistors never be operated any where near the primary breakdown voltage, also repeated primary breakdown voltage shortens a transistor life.<sup>22</sup>

• 4,5 The Darlington Configuration

With high power transistors current gain (hfe) is usually sacrificed. To obtain high capability from power transistors, requires high resistivity silicon material. But then the current capability and power efficiency are reduced drastically. One solution to the high gain problem is a power darlington, but high switching speed, **and** low saturation level are somewhat disfavoured. The darlington configuration will provide at least double the saturation level voltage level, and consequently double **the** conduction loss. A separate supply for the driver **will** lead to less dissipation but this will require two separate supplies in the case of an inverter bridge. Although that this could lead to a substantial improvement in efficiency this was not adopted in the circuit **as it** increased complexity.

**The** darlington with its simplicity and easiness to operate from logic level signals makes it popular. Darlington package with snubber diodes have been available **for** several years, and considerable evidence already indicates that multi-transistor darlington (switching enhancement) devices will emerge. It is believed by **many** that the darlington is the switching device-of the future.

#### 4:6 Requirement Of The Transistor Bridge Diodes

**For** an induction load, the power factor is always lagging, **and** therefore when the voltage is removed by switching off **a** transistor an alternate path for the current must be found. This is provided by the diodes. To prevent a high kickback voltage when the current commutates from the transistor to the diode, it is essential that the transfer occurs smoothly. When a step function of forward current **is** applied, the voltage waveform appears differentiated, **as** if the diode is inductive. Therefore, the forward recovery time should be at least as fast as the transistor switch off time. This is fortunately normally the case as diodes are much faster than transistor darlington pairs.<sup>25</sup>

Although the forward characteristics are important, reverse-recovery time is of utmost importance. When a diode is conducting current in the forward direction and the transistor in the same limb, but opposite side is switched **on**, short circuit current will flow through the transistor **Art:** the reverse direction of the diode, until the latter has gone in<sub>A</sub> the blocking state. Reverse-recovery time is a measure of the commutation capability of a device to switch **from** an on state to an off state. Charge stored in the **forward** biased diode 'must be depleted, when the diode is suddenly reverse biased. Therefore, it is essential that

the structure and supply inductance limits this peak reverse current within the transistor current limit.

The diode also provides a current path when operating in the regenerative mode and therefore must be able to handle current requirement and the resulting power loss.

The diode used in the design of the inverter is the Motorola MR702

University of Cape Town

The Loss Mechanism In Transistors

The power losses involved during the forward conduction state of a transistor are simply equal to  $2V_{ce}I_m$  (neglecting switching times) where  $I_m$  is the motor phase current. During switching the losses involved are not so obvious. The energy dissipation in a switch operation is  $E_r = \frac{V_b I_m T_r}{2}$  where  $V_b$  is the battery voltage and  $T_r$  is the rise time of the collector current. The diode losses are small compared with other losses. When the transistor is cut off, a high  $dI/dt$  is produced due to the supply and structural inductance ( $L_s$ ). The following approximation can be done  $dI_m/dt = I_m/T_f$  the energy expended  $E_f = \frac{(V_b + L_s dI_m/dt) I_m T_f}{2}$  where  $T_f$  is the fall time of the collector current. Hence

$$E_f = \frac{V_b I_m T_c}{2} + \frac{L_s I_m^2}{2}$$

Therefore for  $f$  cycles the power loss is equal to  $2V_b I_m + 4(V_b I_m \frac{T_r + T_f}{2} + \frac{L_s I_m^2}{2})f$ , since two transistors per path and two switch on and switch off for one cycle.

The losses consist of three groups  $W_f = 2V_b I_m$ ,  $W_b = 4(V_b I_m \frac{T_c + T_f}{2})f$ ,  $W_s = 4V_b I_m \frac{L_s I_m^2}{2}$

$W_f$  is the forward conduction losses and is frequency independent. These are minimised with a low  $V_{ce}$  (sat).

$W_s$  is the dissipation of the magnetic energy of the structure and the supply. This term is independent of the switching speed and is minimised by keeping the structure inductance small by designing a compact structure. The shape is also important and a circular one should theoretically be best. <sup>8</sup> It is also frequency dependent and the same as the above is applied. As this term is proportional to the current square it is vital to limit the current switched on or off at any one time. The advantage of the interlacing is therefore of great importance since only 1/8 of the total current is switched at any one time.  $W_b$  is the dissipation from the source to the switch when switching, and is minimised by a fast switching time. This term is frequency dependent, and therefore the frequency must be limited so as to optimise overall efficiency of inverter and motor. The above losses were  $W_s, W_b, W_{sw}$  (separated (see Appendix E)).

## THE LOGIC WHICH IMPLEMENTS THE SWITCHING OF THE 9 PHASE INTERLACED INVERTER

### 5.1 The Logic Controller

A brief summary of the logic which produces the switching action of the interlaced 9 phase inverter is given. Each section is given in block diagram form (see FIG. 5.1) and is subsequently dealt with separately.

#### 5.1.1 Summary of Logic

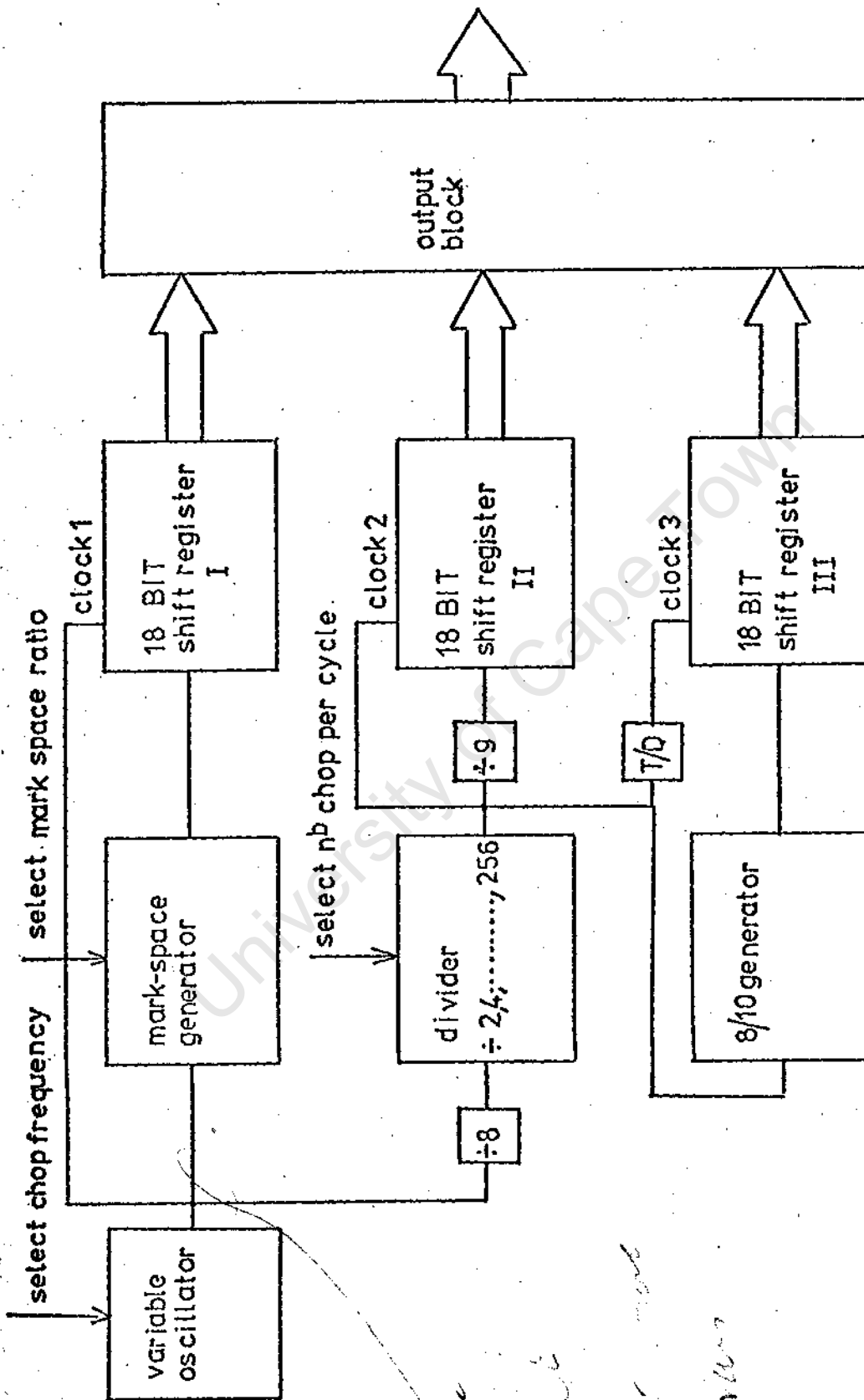
The circuit basically consists of five blocks, an oscillator, a M/S generator, a divider, an 8/10 generator, three shift registers and an output block

#### 5.1.2 The Oscillator ( FIG 5.2 )

Close loop development of the inverter drive in the present investigation was not contemplated. An ordinary bistable was sufficient. An NE 555 I.C. was found sufficiently stable and adequate for the purpose. The frequency is simply controlled by a variable resistance.

#### 5.1.3. The M/S Generator ( FIG 5.2 )

The oscillator output is fed to a binary up counter (SN7493) which resets at the count of every 8 pulses. The output of the counter is compared (SN7485) with a preset (part in 8) mark-to-space ratio on switches. The counter sets a flip flop at "0" and stays high until the



*Handwritten notes:*  
 There is a  
 4-bit  
 counter  
 counter

FIGURE 5.1 : BLOCK DIAGRAM OF TTL LOGIC CONTROLLER

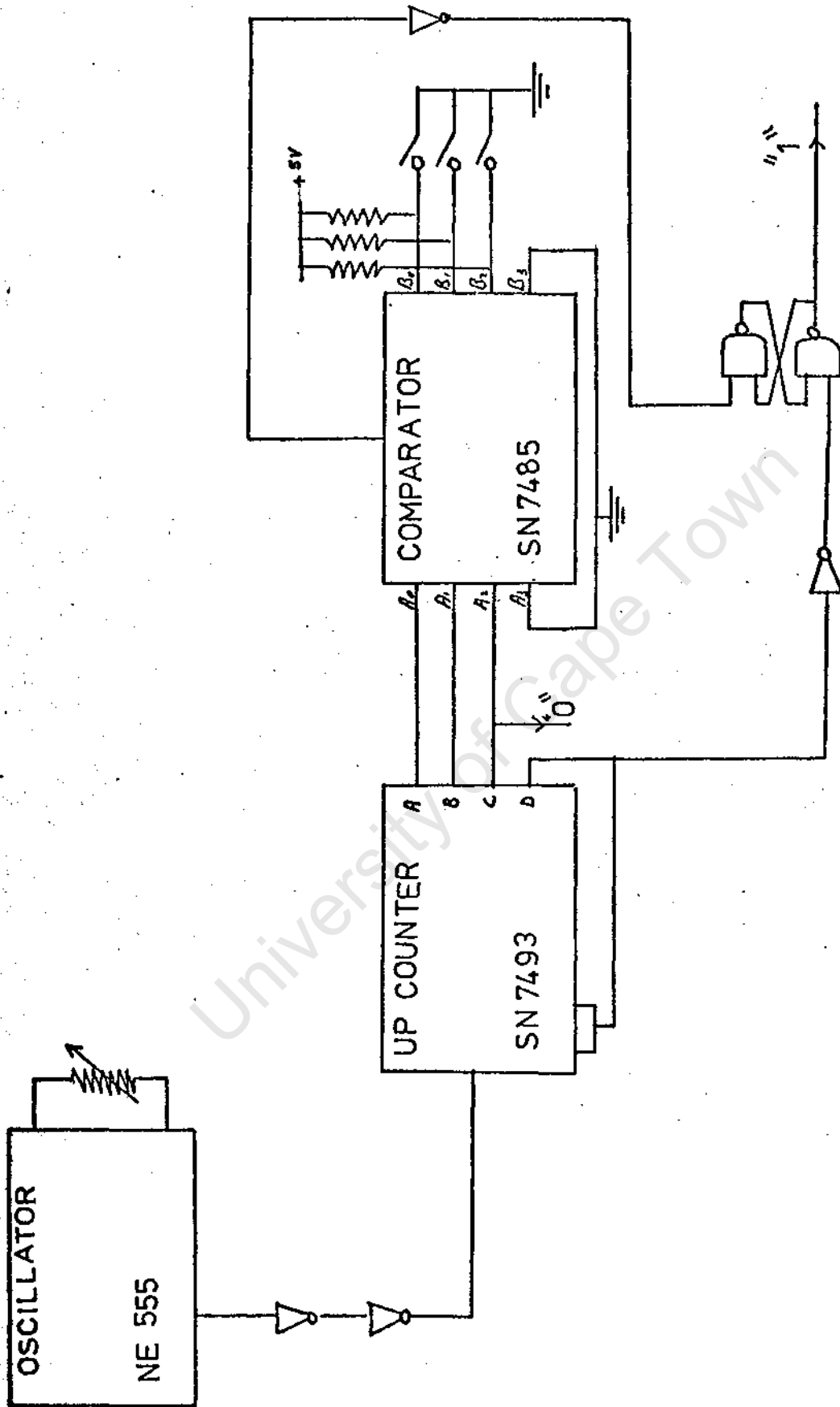


FIGURE 5.2 THE OSCILLATOR AND THE M/S GENERATOR

desired mark-to-space is counted. When A B, the flip flop is reset until the counter sets it again at the count of 8 (or "0").

#### 5.1.4 The Divider ( Fig 5.3 )

A pulse at  $1/8$  of the frequency of the oscillator is taken from the counter of the M/S generator (SN7493) and divided by 1, 2, 4, 8 ... 256, depending where the output is taken from the two 7493 I.C. The output of the latter goes to a counter (SN7490) which resets at the count of 9 pulses (i.e. when A and D are high). The C output is divided by two, by a flip flop.

#### The 8/10 Generator ( F/6 5.4 )

The same pulse from the M/S generator counter C output is used. This goes through an up counter (SN7493) which resets at the count of 18. The reset pulse is derived from the above divider, through a monostable (SN74121) to produce a short trigger pulse. The C output of the counter which is only high for 8 pulses is in turn used to produce a short trigger pulse (SN74121) to reset the flip flop (SN7400). The flip flop is set by the trigger pulse obtained from the divider, which occurs every 18 pulses. The result is a pulse with a high for 8 pulses and a low for 10, which is in step with the 9 high 9 low output of the above divider.

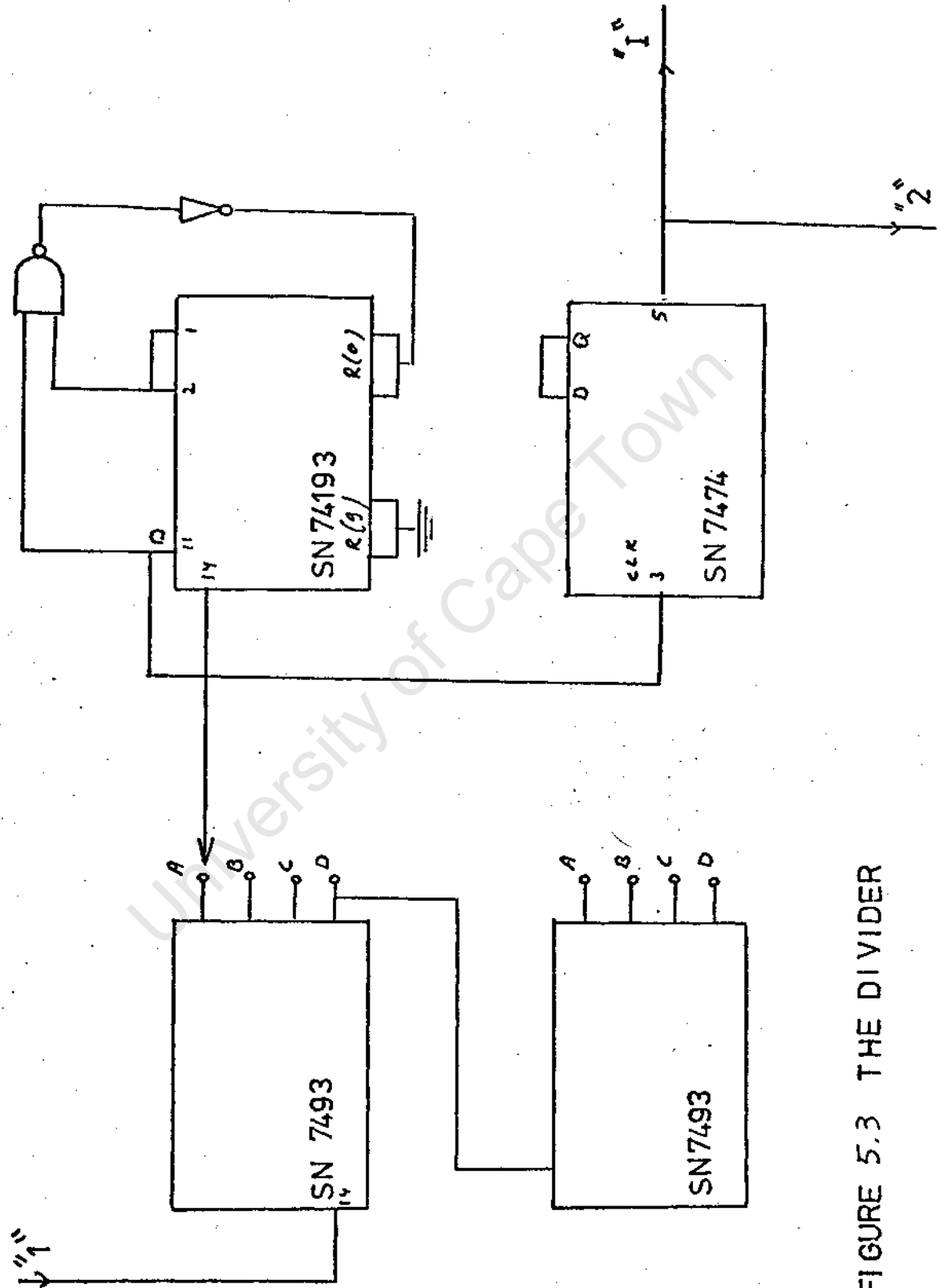


FIGURE 5.3 THE DIVIDER

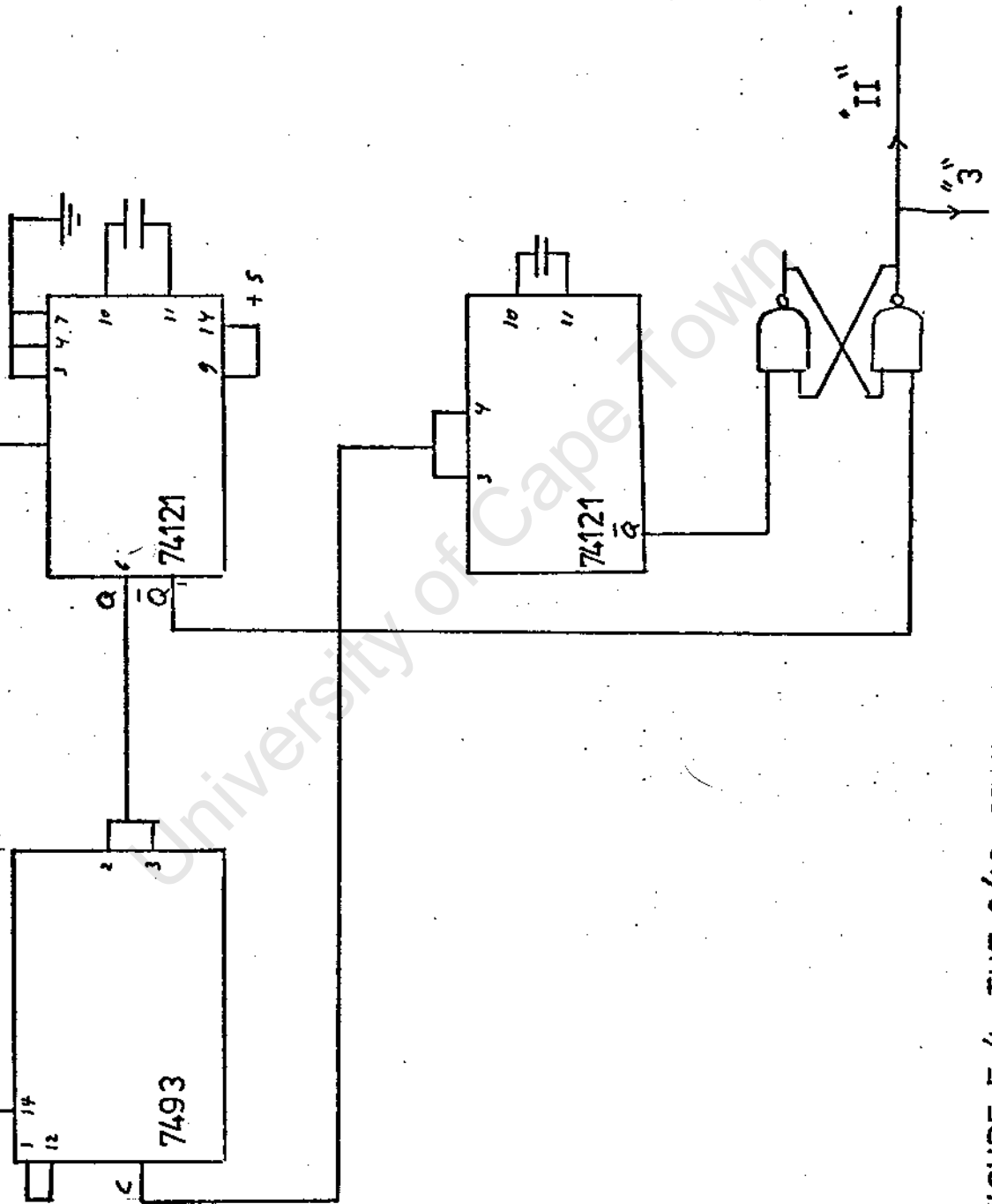


FIGURE 5.4 THE 8/10 GENERATOR

### 5.1.6. The Shift Register ( FIG 5.5 )

The shift registers are 18 bit shift registers which consist of 5 SN7495 IX. each. They can be selected to shift from left to right or right to left depending on the state of the mode control. This determines the direction of the motor. It must be noted that in the third shift register the clock pulse is delayed by a monostable (74121), This provides the required delay mentioned in Section 2.3.

### 5.1.7. The Output Block ( FIG 5.6 )

The output of the three shift registers are combined to form the control for the 36 power transistors .of the interlaced inverter. The 9/9 output of the shift register 2 is straight forward and control as such the PNP transistors. Outputs of the shift register 1 and 3 are combined to form the control of the NPN transistors. Basically it consists of taking one of the 18 output of the shift register 1 and ONE OF SHIFT REGISTER II AND COMBINING THEM At first sight it would seem sufficient to obtain the required control pulses for interlacing by simply <sup>“</sup>adding<sup>”</sup> output 1, 2, 3 ... 18 of shift register 1 with output 1, 2, .3 ... 18 ... of shift register 3 respectively. This however does not produce a complete interlacing logic as extra pulses occur when the sequence goes from

the last output to the first output of the shift register. This occurs because 18 is not divisible by 8 - therefore some of the phases would experience a higher average M/S than others. The problem was overcome by using a data selector which consists of two 7485 I.C. (see Diagram 5). The idea is to detect when a discrepancy occurs and phase shift the output for a period of time. In this manner each phase experiences the same total amount of pulse widths. The shift register and the output block are shown in figure 5.6.

A variable frequency oscillator determines the clock frequency of the first stage (clock 1) - In Section 2 the mark-space generator can produce eight discrete pulse widths whose mark-to-space ratios are selected by binary-coded switches as desired ( $1/8, 2/8 \dots 8/8$ ). The output of the mark-to-space generator is then fed to an 18 bit shift register with 18 outputs. The clock is set by the oscillator.

In Section 2 the oscillator frequency is divided by 8 and subsequently by 2, 4, 8, 16, 32, 64, 128 or 256 as selected. This output determines the clock frequency of the second stage. The clock frequency is divided by 9 to produce a pulse which is on for 9 clock pulses and off for 9 - this determines the fundamental frequency of the inverter and is fed into an 18 bit shift register.

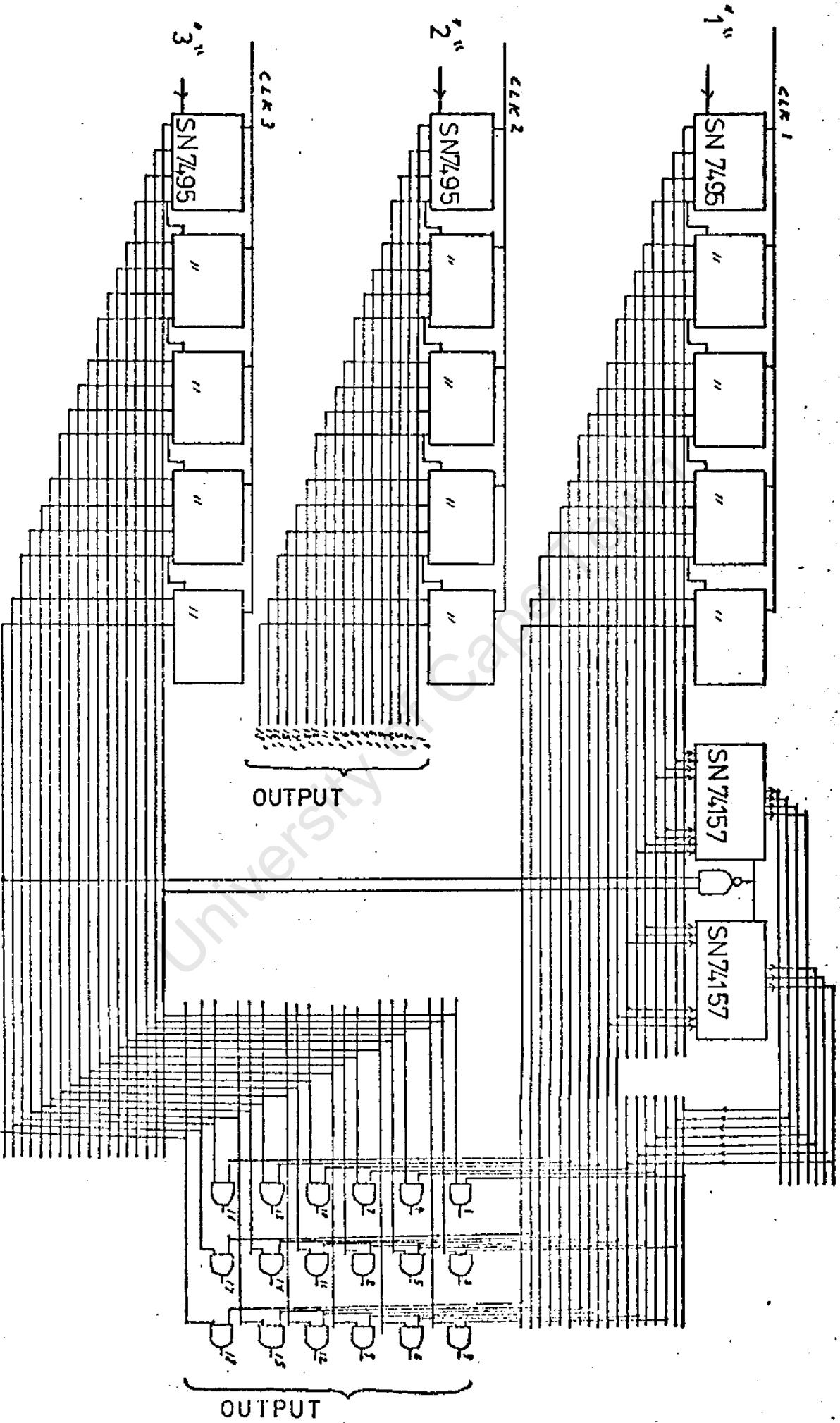


FIGURE 5.6 THE SHIFT REGISTERS AND OUTPUT BLOCK

Section 3 produces a similar pulse as above (same frequency) but on for 8 clock pulse and off for 10. This is again fed to an 18 bit shift register — the clock pulse is shortened by a variable amount between 5-30 micro seconds to produce the delay necessary when "stepping". This is the required delay mentioned in section 3,3.

## CHAPTER VI

### DESIGN OF THE 9 PHASE MOTOR (B)

#### 6.1 TORQUE REQUIREMENT

The main criteria of design was torque requirements, especially stalling torque, as the project mainly concerned itself in investigating a possible direct to wheel motor. Results obtained from the 9 phase motor (A), which is described in Appendix <sub>F)</sub> justified the design and the construction of one of the two motors which is to be directly coupled to the road wheel.

#### 6.2 DESIGN OF STATOR CORE

**A.** large diameter at the air gap is essential to achieve high torque, as the torque increases with the square of the diameter for the same core stack length and linearly with diameter for a same volume (i.e. approximately the same iron weight). As the maximum electrical loading and magnetic loading are restricted by losses, thermal dissipation and material properties, a large diameter is the most obvious answer to increase torque. Nevertheless a large diameter increases the overhang to active copper ratio as it implies a relatively small stack length. Effort must therefore be made in the

winding design so as to keep this ratio at an acceptable level (ie. many poles). Readily available laminations, with suitably large diameter of 6.245m at the air gap were chosen.

Assuming similar loading, as the motor described in appendix F which gave us a force per unit area of  $15800\text{Nm/m}^2$ , the stator core length (l) required to produce the desired torque of  $125\text{Nm}$  per motor (see Appendix H) is :

$$l = \frac{\text{required area}}{\text{radius} \times \pi \times 2} \quad \text{area} = \frac{\text{torque}}{15300}$$

$$l = \frac{125}{0.245 \times 0.1223 \times \pi \times 15300}$$

$$= 0.083 \text{ m}$$

A 0.05m stack core was decided on as the weight of the motor would become excessive. To retain the torque of  $125\text{Nm}$  on start the electrical loading will have to be increased to

$$65300 \times \frac{0.083}{0.05} = 108400 \text{ ampere conductor/m}$$

Such an electrical loading is rather high for an induction motor. But considering that the maximum torque on stalling is seldom required, it would be acceptable provided the temperature of the winding is kept within its thermal limits by the driver M with the control.

### 6.3 Winding Design

The total ampere conductor to Produce the required electrical loading of 65300 amp conductor on starting is ;-

$$108400 \times 0.24 \times \pi = 81730 \text{ ampere conductors}$$

$$\text{that is : } \frac{81730}{9} = 9081 \text{ ampere conductor/phase.}$$

Assuming all coils of each phase connected in series and a maximum current of 25 amp. The number of conductors per phase is 363. A large number of pole decreases the overhang to active copper ratio as it reduces the length of a coil pitch. However, since many poles requires many separate windings and, therefore increase the cost, a practical number must be decided upon. An 8 pole motor was chosen as it lent itself best to the available laminations

The number of turns per pole per phase (per winding) is

$$\frac{363}{8 \times 2} = 22.7$$

22 turns was chosen in accord with <sup>area of</sup> S.W.G.14 wire and the available area of the tooth gap.

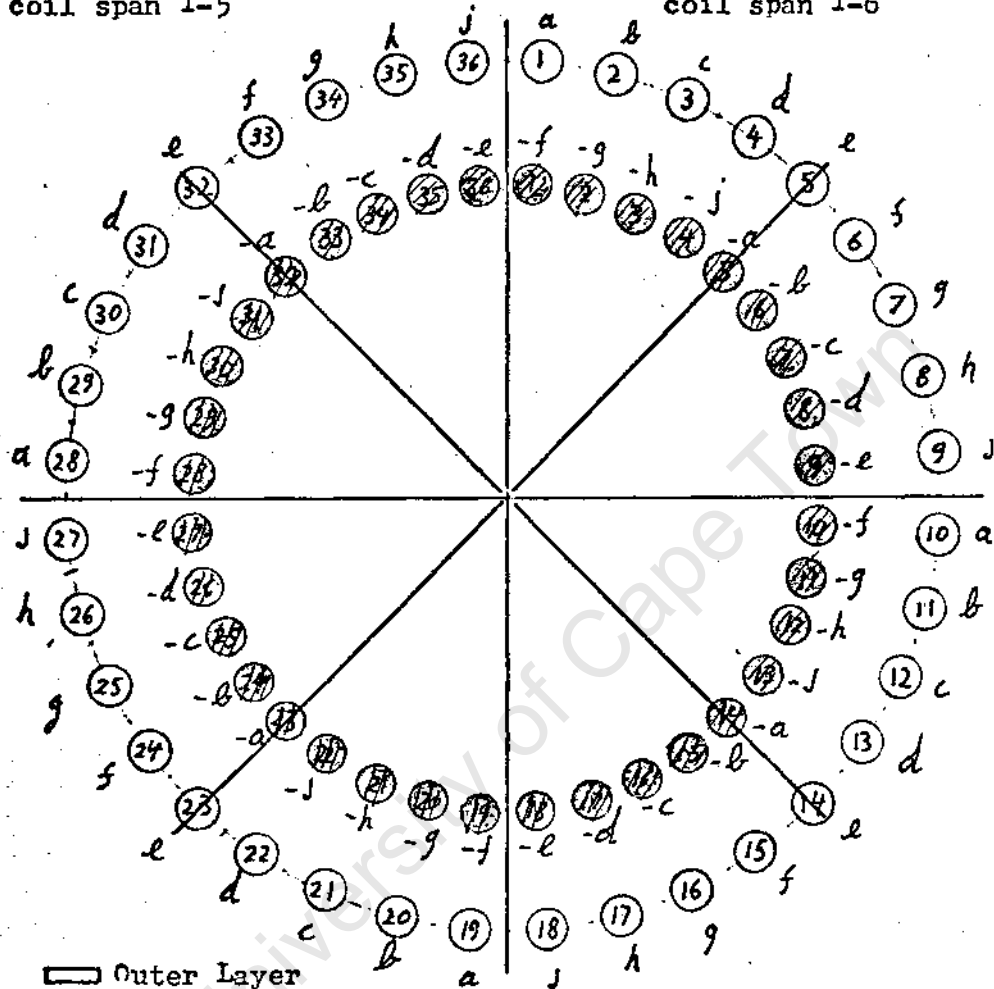
The practical realization of an 8 pole, 9 phase winding is shown in Figure 6.1. The limitation to 36 slots by the laminations which are readily available meant that with a conventional arrangement there would be 4i coils per pole for a double layer winding. These coils would have to be equally distributed between the 9 phases which were desired.

FIGURE 6.1

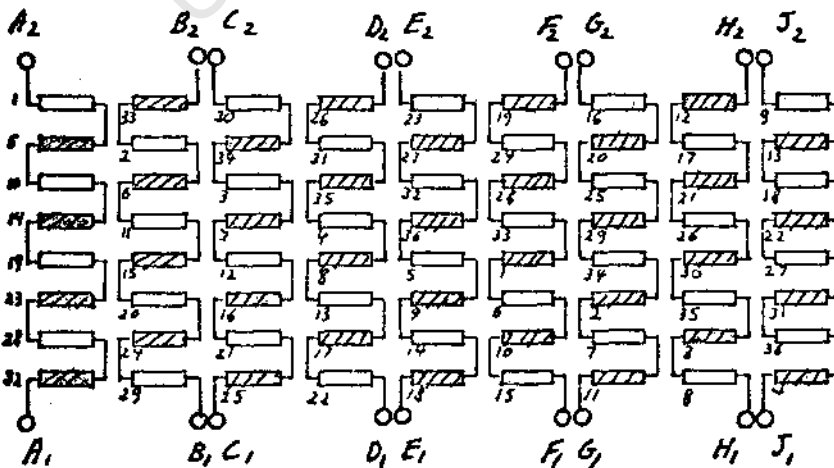
AN 8-POLE, 9-PHASE, FRACTIONAL SLOT WINDING IN 36 SLOTS

Outer double layer  
coil span 1-5

Inner double layer  
coil span 1-6



□ Outer Layer  
▨ Inner Layer



All start on  
on l.h.s  
Phase connec-  
tions ACEGJ  
on l.h.s.

All finishes  
on r.h.s.  
Phase connec-  
tions BDFH on  
r.h.s.

The average pitch is 42 slots per pole and the winding is therefore essentially fractional. The number of coils was increased to 72 by arranging for two double layer windings, one with a pitch of 4 slots and the other with 5 slots. Each phase has 8 coils with an average pitch of 42 slots.

All the starts are brought out on the left hand side of the motor and the finishes on the right hand side to facilitate the interconnections. This results in the termination of 5 phases on one side and **4** on the other and allows the convenient connection to the transistors mounted on the aluminium end shields.  
**see construction chapter 7**

#### **6.4 Maximum Speed at Full Flux**

Assuming an average flux density of  $0,6 \text{ w/m}^2$ . The average voltage per phase is

$$V_{ph} = n \times 0,6 \times v \times L$$

$n$  = number of conductors in series per phase

$v$  = velocity of air gap phase

$L$  = core stack length

With a maximum battery voltage  $V_b$

$$V_{\text{phase}} = V_b \times 8/9 \text{ (160}^\circ \text{ conduction angle)}$$

$$v = \frac{8/9 V_b}{22 \times 2 \times 8 \times 0,6 \times 0,05}$$

$$v = \frac{V_b}{11,8} \text{ m/sec}$$

or  $0,11 V_b$  revolution/sec

Velocity at road surface with a 0.32m wheel diameter

$$= \frac{V_b}{11,8} \times \frac{.240}{.1125} \times 3,6 \text{ km/h}$$

$$= 0,64 V_b \text{ km/h}$$

with a maximum battery voltage of 60v the speed of the motor is 397r.p.m., and the speed of the vehicle is 33.4km/h.

The inverter fundamental frequency is

$$0,118 \times 60 \times 4 = 26,5 \text{ Hz}$$

It must be noted that the above calculations are based on an average flux density of  $0,6 \text{ W/m}^2$  this is a value normally used for sinusoidally distributed flux and could be more as the flux has a square wave distribution and the iron is used more evenly resulting in a higher average flux density.

### Thickness of Yoke

- . Flux per pole on the basis of an average flux density of  $0,6 \text{ W/m}^2$ .

$$\text{Pole arc at air gap} = \frac{\pi \times .245}{8} \text{ m}$$

If  $B_y$  = flux density in yoke,  $dy$  = yoke radial dimension

$$\frac{0.6}{2} \times \frac{\pi \times .245}{8} \times \frac{1}{dy}$$

For a yoke flux density of  $1.3 \text{ W/m}^2$

$$\begin{aligned} dy &= \frac{0.6 \times \pi \times .245}{1.3 \times 16} \\ &= 0.022 \text{ m} \end{aligned}$$

The laminations used were 4 pole laminations with a 0.052m yoke thickness. The yoke thickness can therefore be reduced to 0.022m for an 8 pole machine. The laminations were cut to an hectoganol shape as it lent itself best to the desired type of construction (see Chapter VII Figure 7.1, 7.2, 7.3).

### ROTOR

Squirrel cage type, unskewed rotor with 32 slots.

Dinemsions :-

Copper Bars :  $0.006 \times 0.04 \times 0.05\text{m}$

Copper Rings : outside diameter ;  $0.0240\text{m}$

inside diameter ;  $0.0160\text{m}$

thickness ;  $0.006\text{m}$

## CHAPTER VII

### CONSTRUCTION OF THE MOTOR-INVERTOR ASSEMBLY

#### 7.1 STATOR

The laminations are held together by bolts which run through near the corners of the heptagonal shaped lamination. They are also sandwiched between two steel rings of 0.6mm thickness. See Figure 7.1, 7.2, 7.3. Standard 4 pole laminations were used and cut to an heptagonal shape with the yoke thickness required for an 8 pole machine. The holes for the bolts were drilled with great care. A special jig was made to assure good alignment of all the stator laminations of the core stack.

#### 7.2 WINDING

The winding as described in Section 6.3 can be seen in Figure 7.4 The interconnections between separate windings were soldered together and insulated with sleeves. Ten ends of five phases are brought out on the one side and 8 ends of the remaining 4 phases are brought out on the other side.

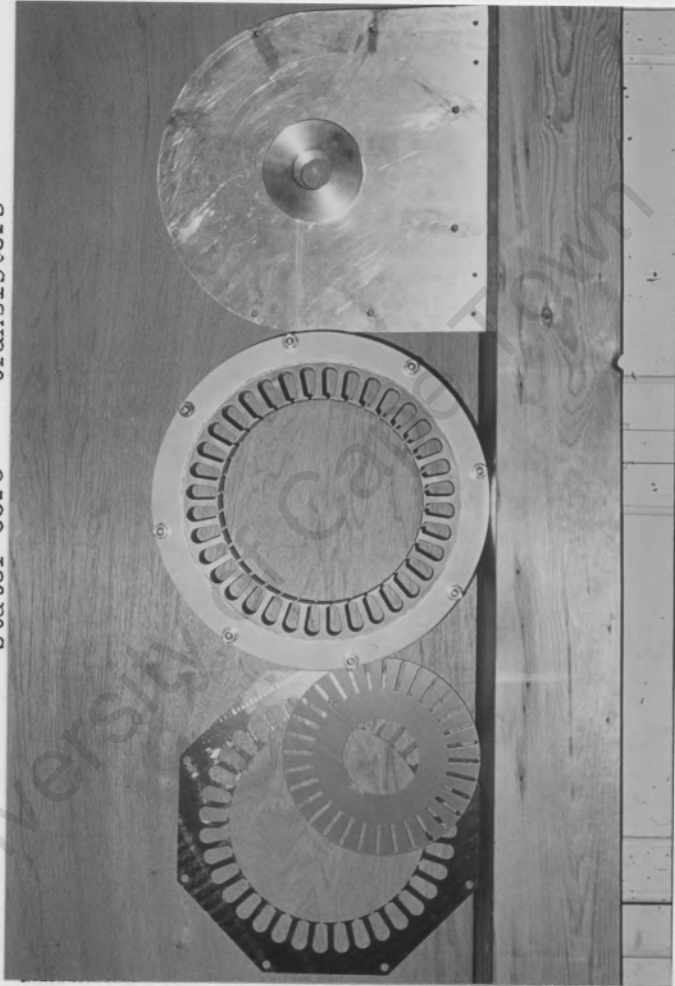
Figure 7.I

end plate without  
transistors

stator core

stator lamination

rotor lamination



Stator and rotor laminations, stator core, motor end plate

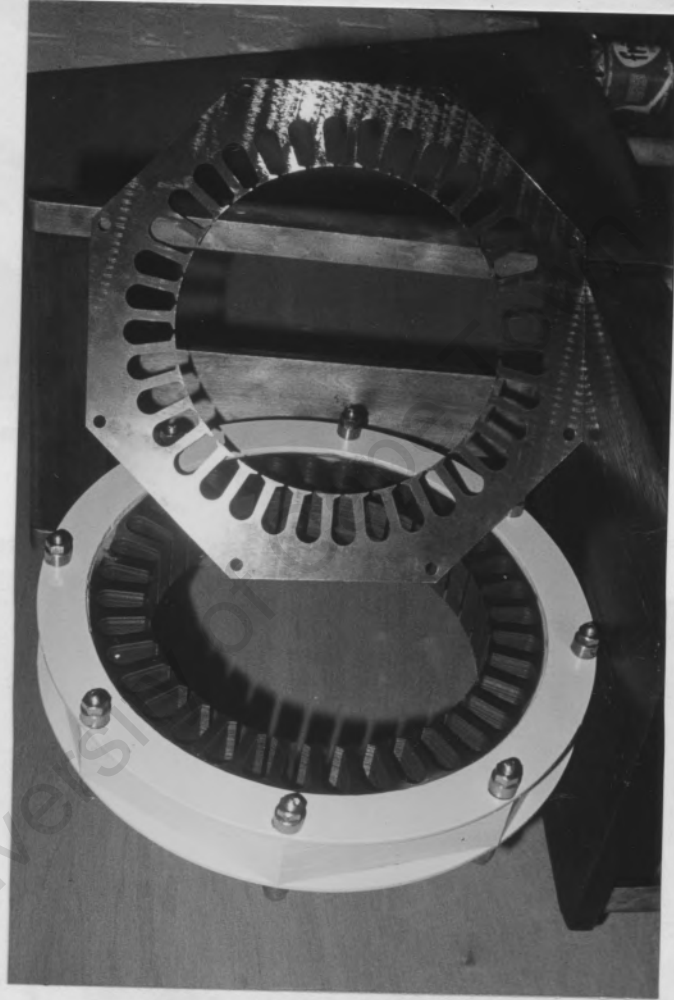


Figure 7.2

stator core

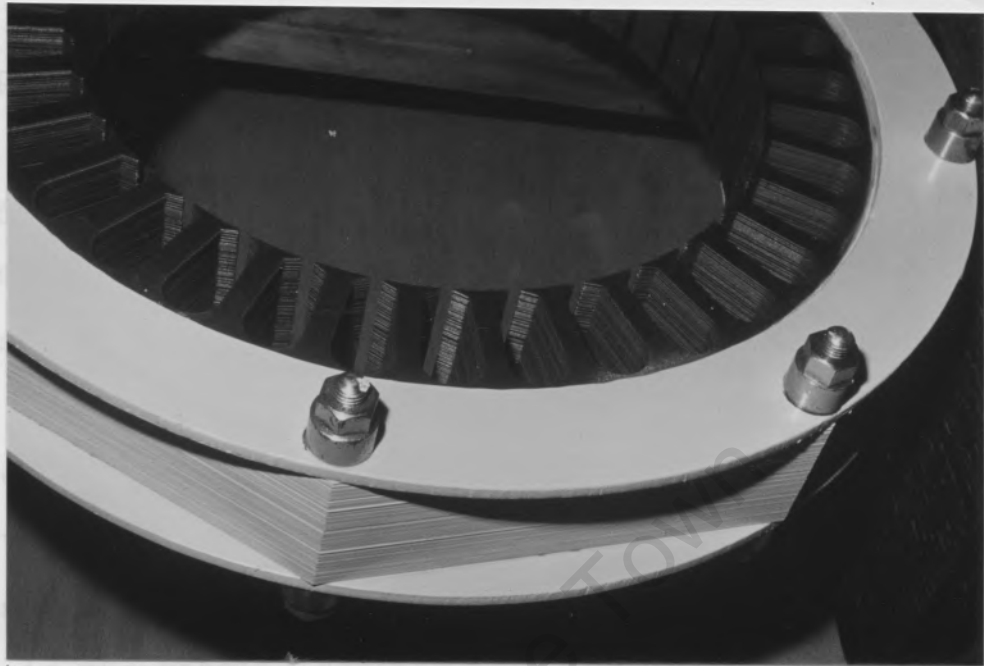
bolts

steel ring

Stator core stack with one lamination shown

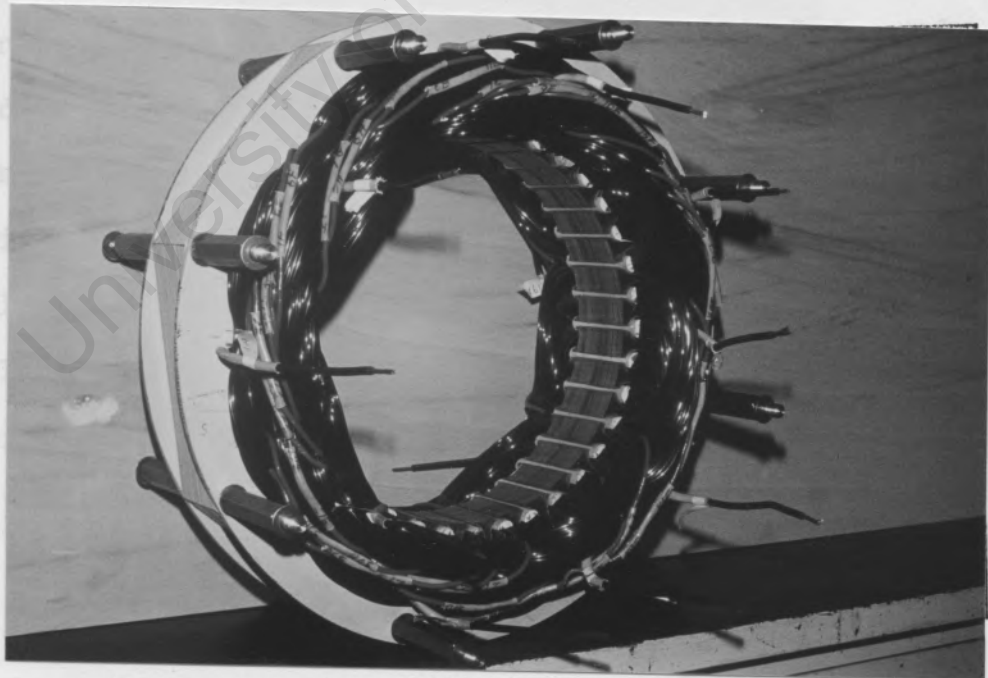
7.3 INVERTER

Figure 7.3



Close up view of stator core stack

Figure 7.4



Stator core stack with winding

The final stator core stack with winding. The multicore ribbon type leads which connect the terminal of the

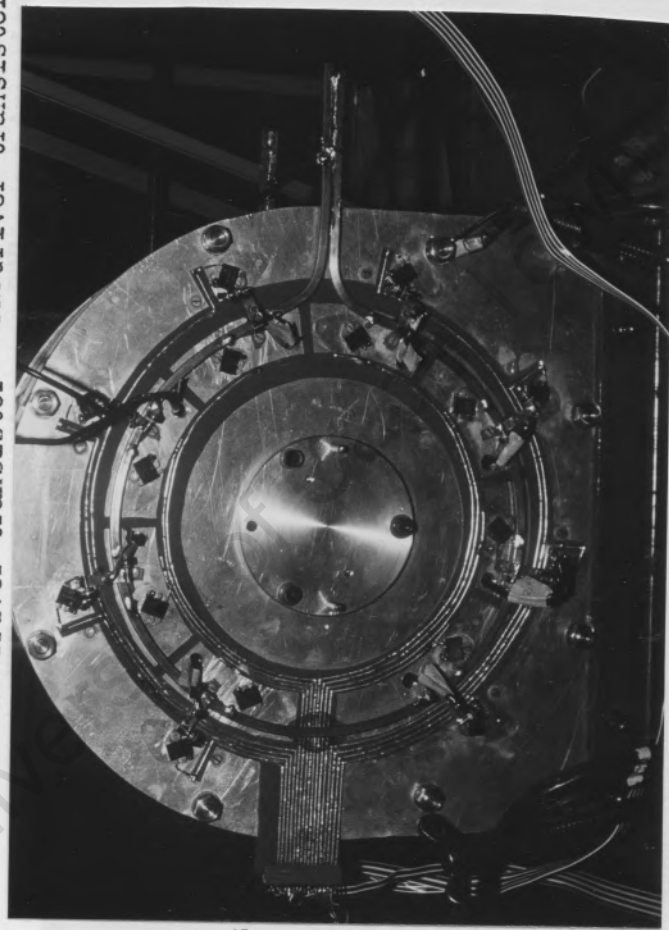
### 7.3 INVERTER

The 9 phase induction motor and its inverter are part of the same assembly. The inverter transistors are mounted on the end plates of the motor which carries the bearings. Figure 7.5 shows the outside of the transistor carrying end plates. The 2N3055 and 2N2955 transistors can be seen. The positive rail is a copper bar of 20mm<sup>2</sup> and the end plate itself is the negative supply rail. A printed circuit board links the base of the driver transistor with a terminal which brings in the biasing signals from the interface stage. On Figure 7.6, the inside of the end plates can be seen, the MJ802 and MJ4502 power transistors are shown. The power transistors leads run through the end plate and are directly connected to their respective transistors which are mounted directly on the other side as seen in Figure 7.5. The power transistors are electrically insulated from the end plate with low thermal resistance beryllium washers. Figure 7.7 shows the half assembled motor-inverter. The end plates are connected to the end plates by pillars which are threaded directly into the stator bolts, see Figure 7.9

The final assembly is seen in Figure 7.8. The multicore ribbon type leads which connect the terminal of the

Figure 7.5

NPNdriver transistor PNPdriver transistor



positive supply  
copper bar

printed  
circuit  
board

terminal

External side of end plate

Figure 7.6

NPN power transistor      PNP power transistor



Half assembled motor and inside view of one of the end plates

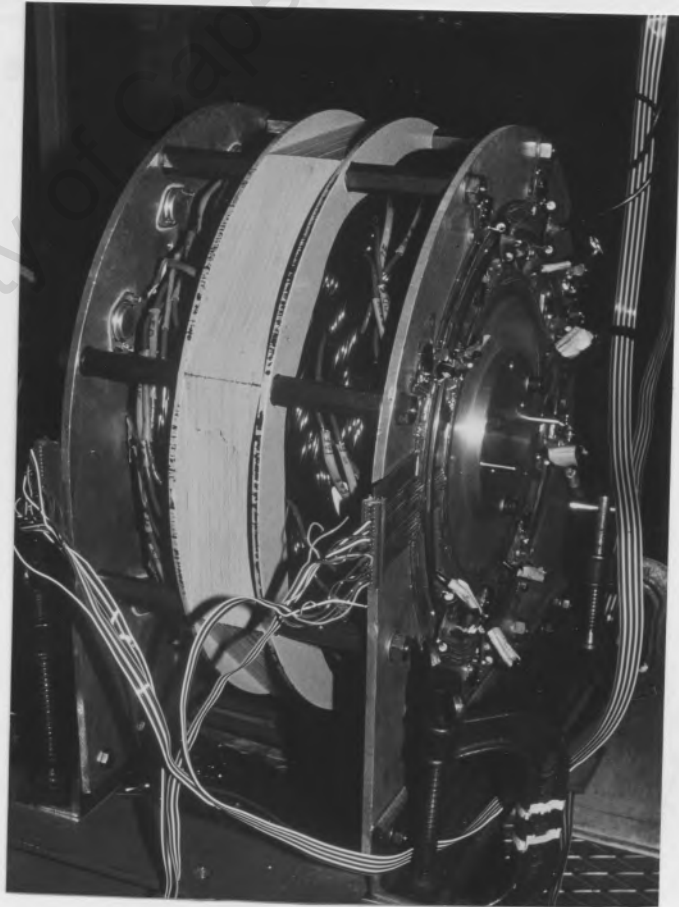
Completed motor-inverter assembly

Figure 7.7



Half assembled motor-inverter

Figure 7.8



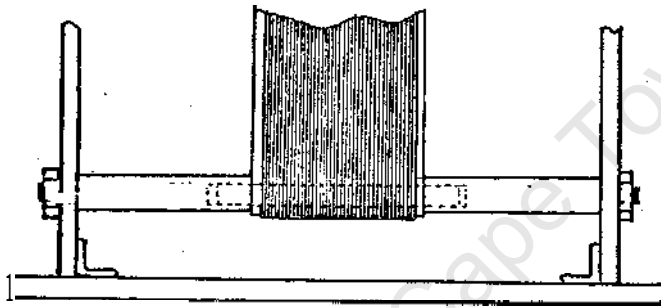
Completed motor-inverter assembly

printed circuit boards to the interface stage

(Appendix *E*) can be seen.

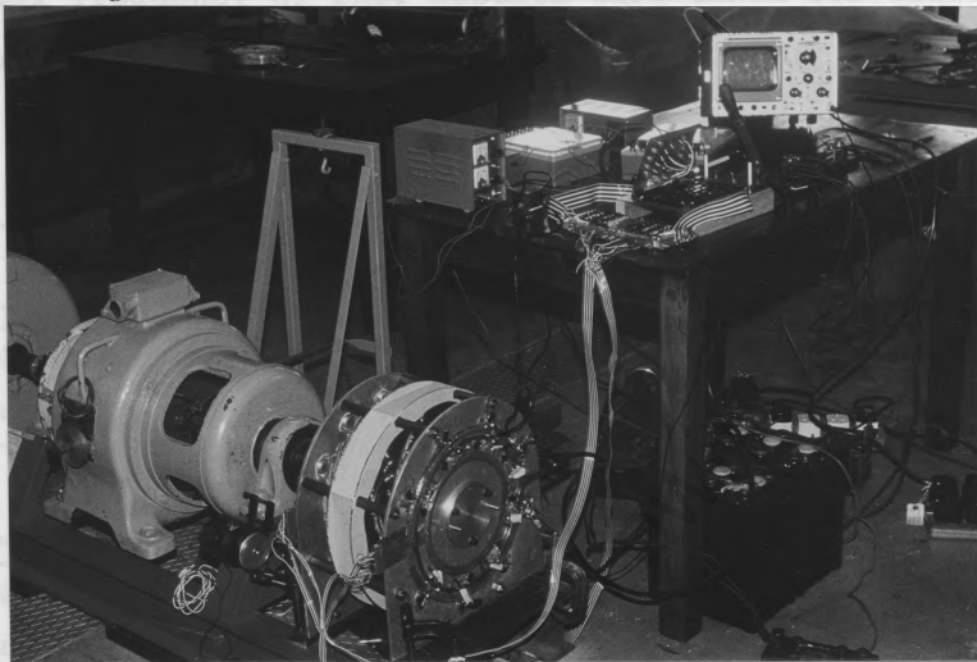
The motor was mounted to a dynamometer for testing and evaluation purpose see figure 7.10

Figure 7.9



Connection between stator core and and plate

Figure 7.10



Motor and dynamometer

V/S	1	2	3	4	5	6	7	8
torque Nm	25	54	70	91	107	-	-	-
apply amp	5	17	-	60	80	-	-	-

V/S	1	3	4	5	6	7	8
torque Nm	-	70	81	-	-	-	-
apply amp	-	22	48	-	-	-	-

The torque per amp per phase was found to be 3.9 Nm/amp/phase on average. In the design the desired torque of 125 Nm was to be obtained at 25 amp per phase, this is  $\frac{125}{25} = 5 \text{ Nm/amp/phase}$ . The torque obtained is higher than this which suggests that the flux density is above the assumed density of  $0.6 \text{ T/a}^2$ .

## CHAPTER VIII

RESULTS OF THE 9 PHASE INTERLACED INVERTER FED INDUCTION MOTOR8.1 Stalling Torque

The maximum stalling torque was recorded for an approximate fundamental frequency of 1Hz. Results were taken for different battery voltages and M/S ratios and are tabulated in table I.

TABLE 1

16V \ M/S	1	2	3	4	5	6	7	8
torque Nm	0	8	27	37	42	57	65	70
supply amp	0	6	16	32	44	56	70	105
30V \ M/S	1	2	3	4	5	6	7	8
torque Nm	0	30	57	70	84	91	100	110
supply amp	2	12	28	44	70	90	110	170
46V \ M/S	1	2	3	4	5	6	7	8
torque Nm	23	54	70	91	107	-	-	-
supply amp	5	17	36	60	80	-	-	-
60V \ M/S	1	2	3	4	5	6	7	8
torque Nm	50	70	91	-	-	-	-	-
supply amp	6	22	48	-	-	-	-	-

The torque per amp per phase was found to be 5.9 Nm/amp/phase on average. In the design the desired torque of 125 Nm was to be obtained at 25 amps per phase this is  $\frac{125}{25} = 5\text{Nm/amp/phase}$ . The torque obtained is higher than this which suggests that the flux density is above the assumed density of 0.6 Wb/m<sup>2</sup>.

The same torque can be obtained by either a low battery voltage at a high supply current with an high M/S ratio, or a high voltage and a low supply current with a low M/S. For example see Table I, 70 Nm can be obtained at 16v with full M/S with the resulting current of 105amps, 30v with M/S with 44amps, 46v with 3/8 M/S with 44amps, or 60v with with 22amps only. Hence

full torque can be obtained with a reduced M/S with a relatively small supply current. The battery supply current was found to have a maximum ripple of 15%. Therefore the R.M.S. current of such a drive is virtually the average current. It can be said that the interlaced inverter acts like a direct current transformer.

## 8.2 Magnetizing Curves

The Magnetizing characteristics for different frequencies were obtained by driving the motor so as to obtain a zero slip frequency. See figure 8.1. Saturation is seen to occur in the region of a battery voltage to frequency ratio of 2.4 (except for very low frequencies). At the maximum battery voltage of 60 volts, the saturation frequency is about 20Hz. This is less than the predicted frequency of 26Hz. (see section 6.4). This suggests that the flux density is higher than the assumed  $0.6\text{Wb/m}^2$

## 8.3 Load test at full flux.

To operate an induction machine at a good efficiency, the machine must be properly fluxed. If insufficiently fluxed it will suffer slip and if excessively fluxed it will have high iron losses and high magnetizing currents. Tests were conducted at 12.5Hz for 3 different voltages in the region of saturation, namely at 24, 30 and 36 battery volts. The torque efficiency and supply current

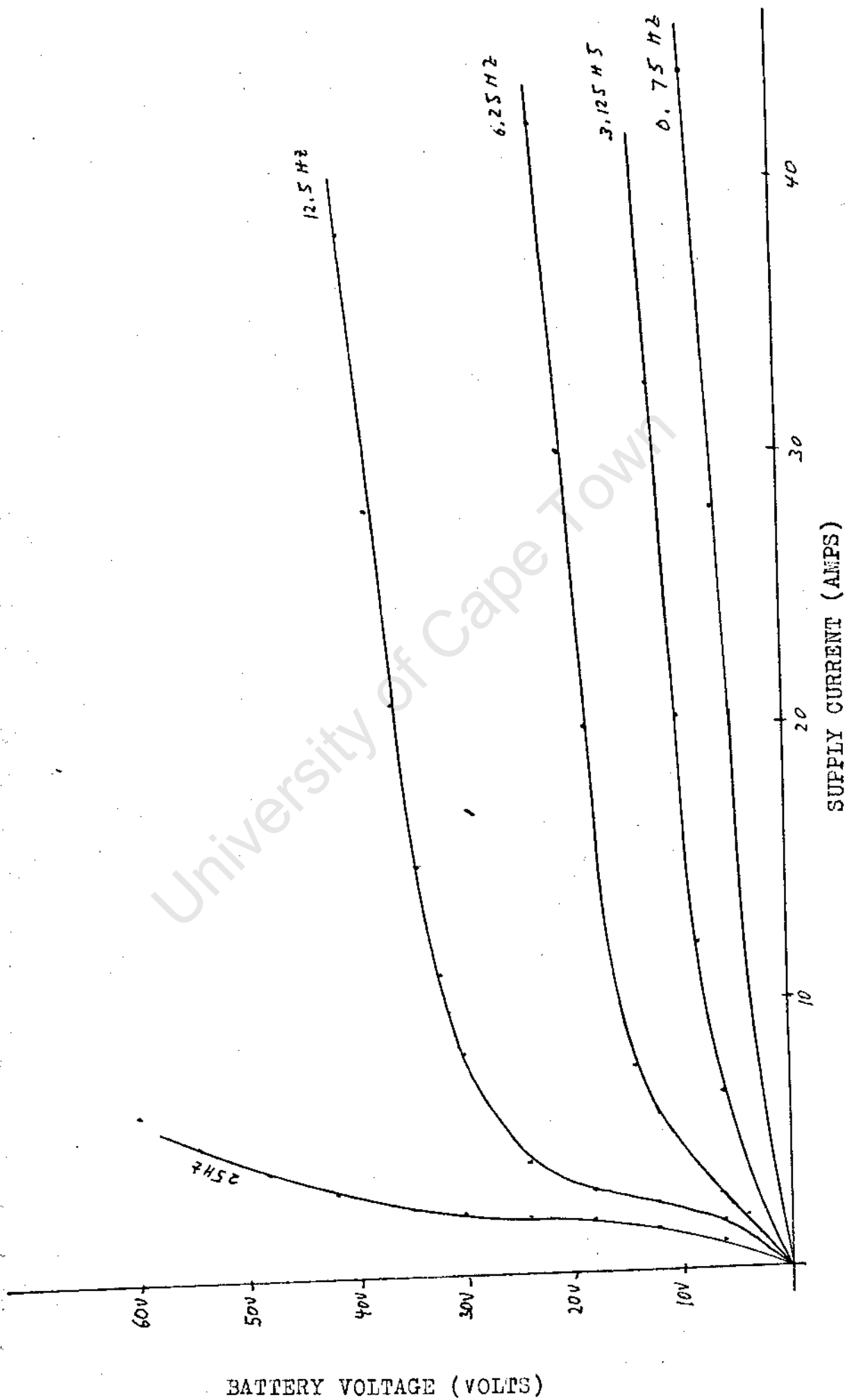


Figure 3.1 Magnetizing Curves for 9 Phase Inverter Fed Motor

obtained is shown in figures 8.2, 8.3 and 3.4. The maximum efficiency recorded for the 3 tests was 62.5% at 30 volt battery voltage with a slip of 8%. At 36 volts the maximum efficiency decreases slightly to 57.5% at 3% slip. It can also be seen that to obtain 30 Nm the efficiency is 62.3% for a slip of 8% at 30 volts and only 52% for a slip of 4% at 36 volts. On the other hand 38Nm is obtained at a slip of 16% for 30 volts and 57% at a slip of 12% for 36 volts. A large value of slip produces high currents resulting in high copper losses, while too large a value of flux will cause saturation, with the resulting increase in iron losses and magnetizing current. To obtain maximum efficiency for a desired torque at a certain speed, the inverter frequency must be set to provide the right slip frequency and the inverter voltage for the right flux density. A point to point adjustment of frequency and voltage would provide optimum efficiency throughout the speed range. The information could be obtained from experimental tests; and stored in an appropriate memory. A calculation method would be difficult as battery and inverter regulation would introduce another variable in the classical method of induction motor theory. A more simple method is to operate at constant slip frequency corresponding to maximum efficiency at rated load. Little efficiency and performance would be sacrificed.

#### .4 Load tests for variable frequency

torque versus speed characteristics were recorded on an x y recorder for 6, 12.5, 25, 37.5 and 50 Hz inverter fundamental frequencies. The voltage was varied in steps of 6 volts up to 48 volts. The results are given in figure 8.5. As torques above

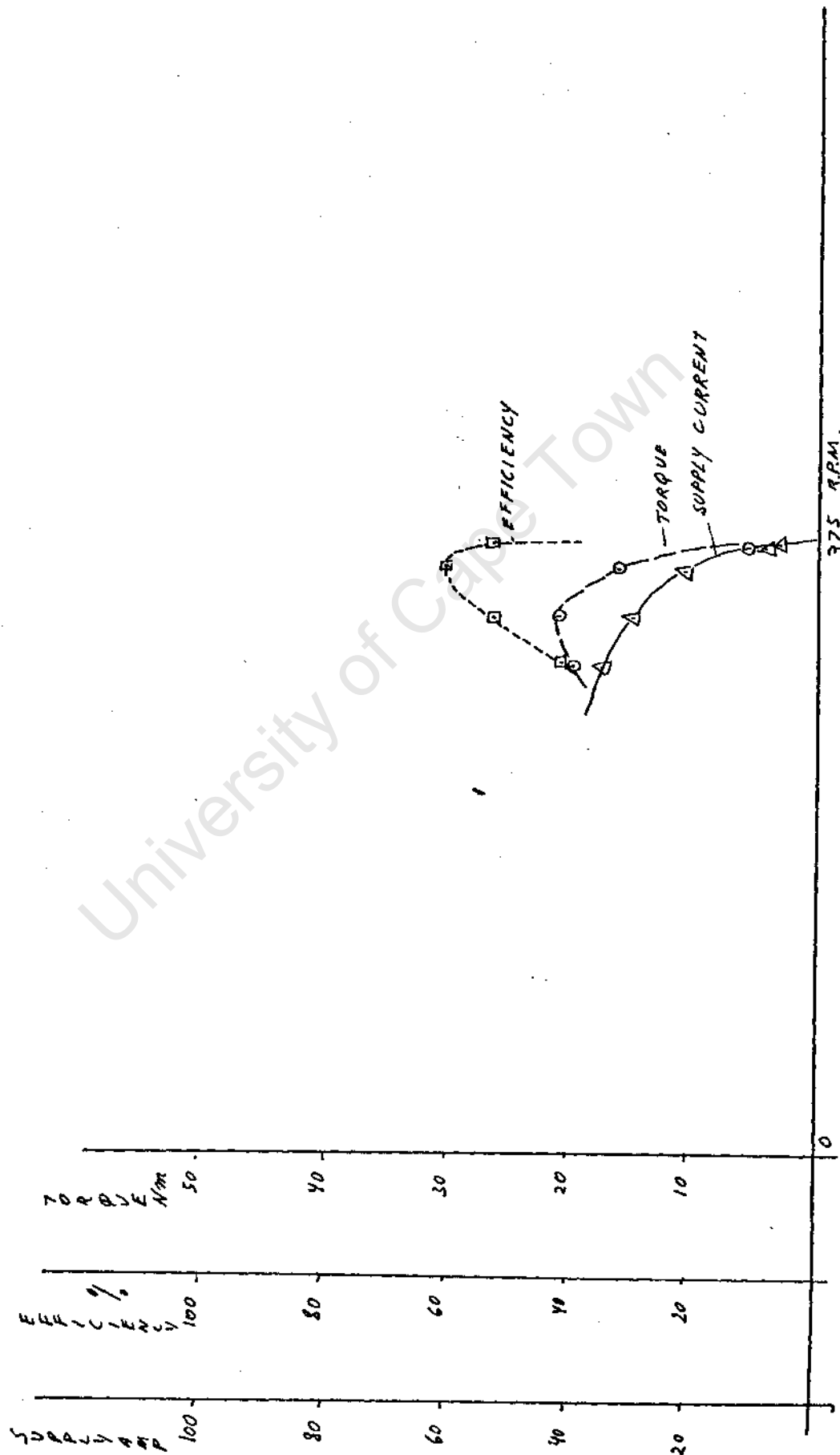


Figure 8.2 Torque, Efficiency, Supply Current VERSES Speed for 24 Volt, Full M/S at 12.5Hz.

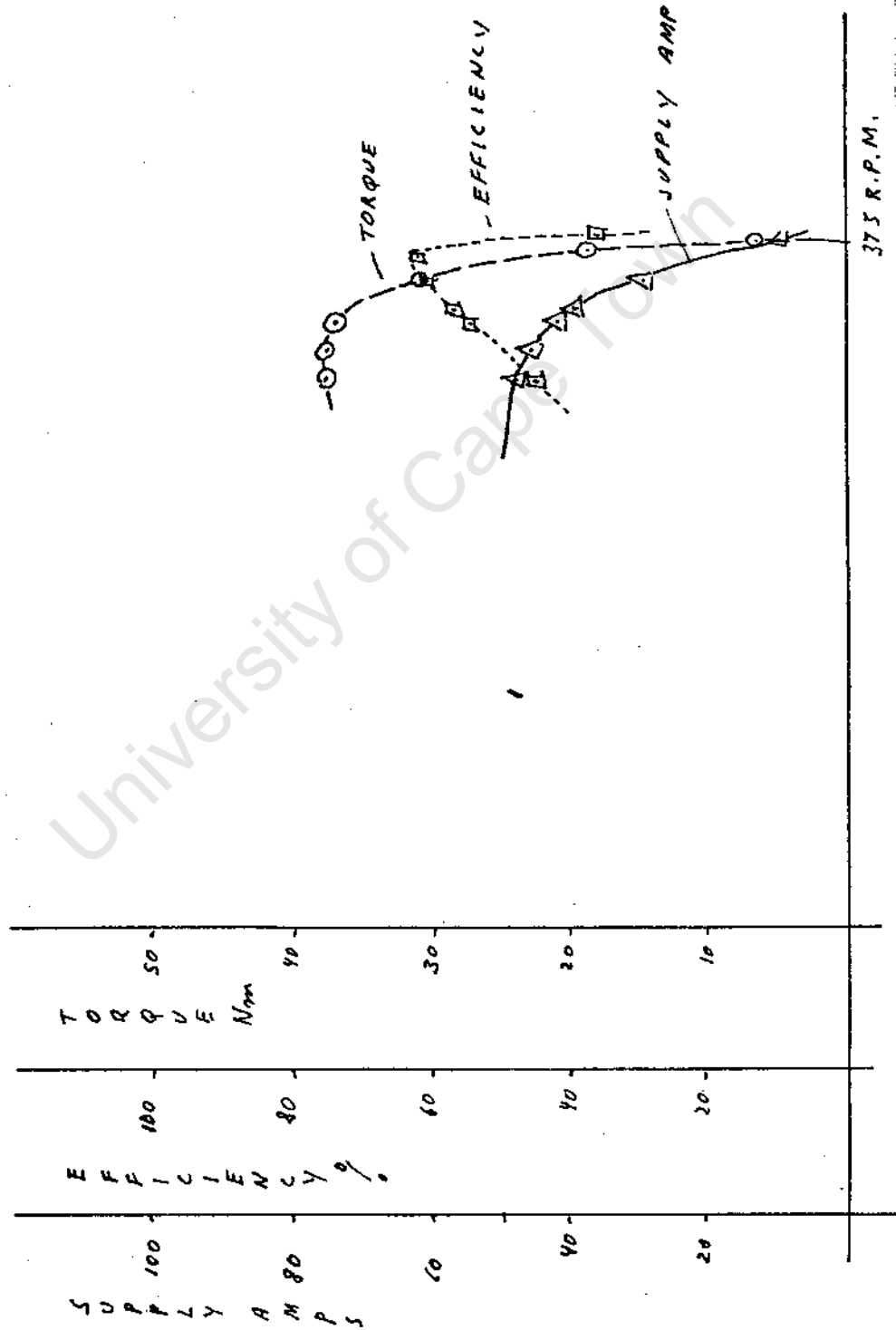


Figure 8.3 Torque, Efficiency, Supply Current VERSES Speed for

30 Volt, Full M/S at 12.5Hz.

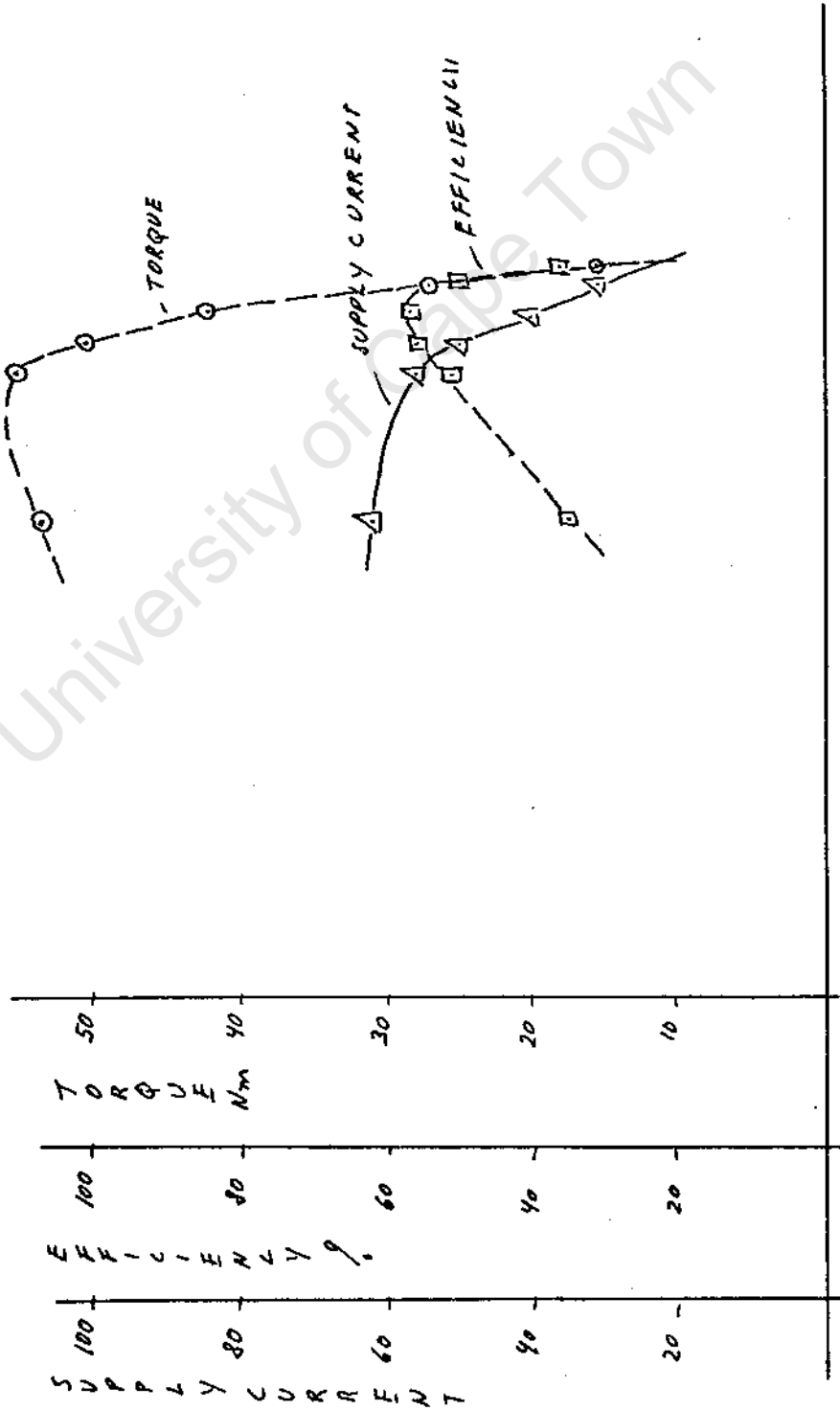


Figure 8.4 Torque, Efficiency, Supply Current VERSES Speed for 36 Volt, Full M/S at 12.5Hz.

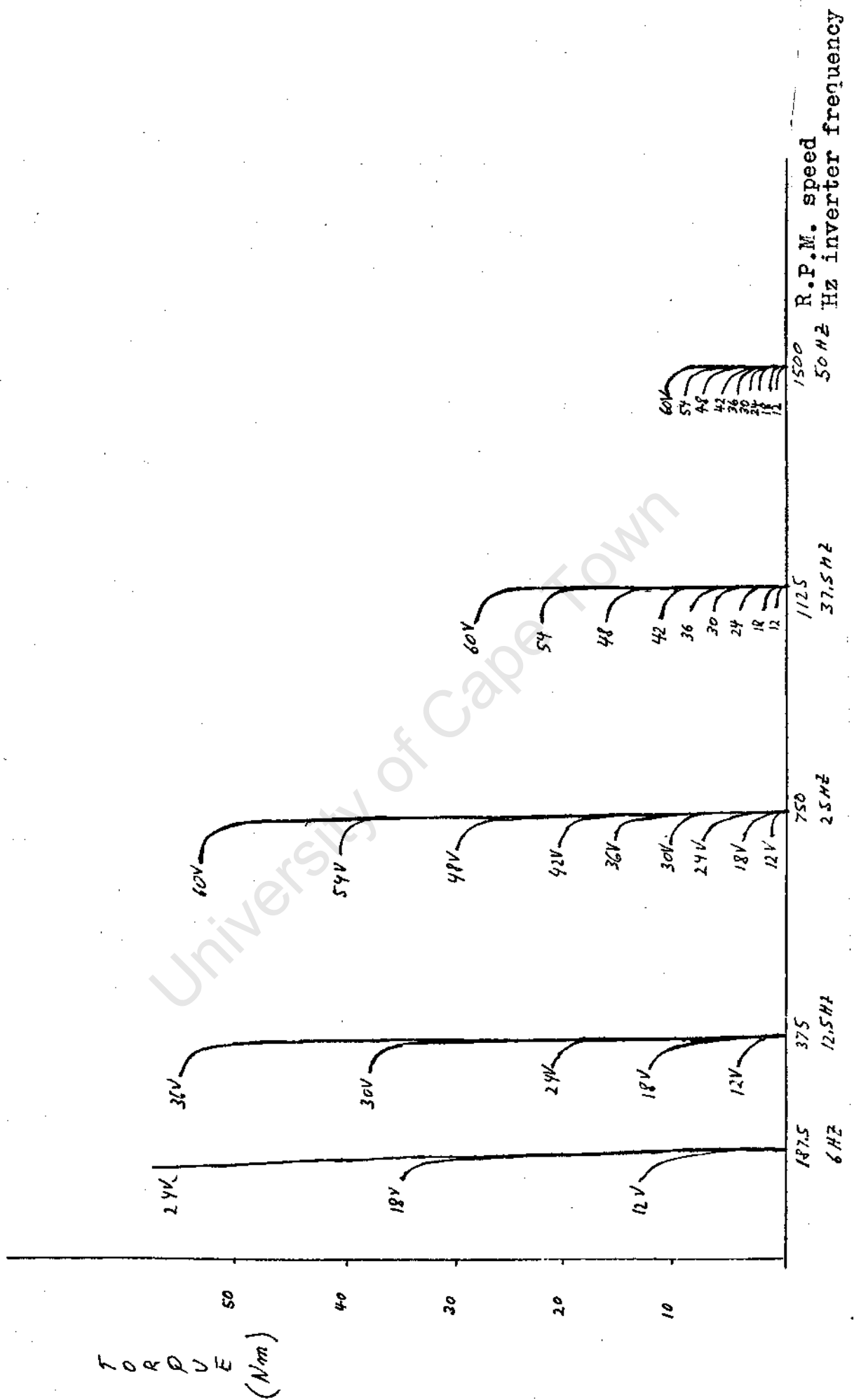


Figure 8.5 Torque, Speed Characteristics for various Frequencies and Voltages at Full M/S.

55Nm could not be recorded with the available dynamometer, the voltage test for higher voltage at low frequency could not be obtained. Full stalling torques were however obtained with a spring balance. From the magnetizing curve it was established that the saturation frequency for 60 volts is about 20Hz. As the frequency is increased above 20Hz the machine became under-fluxed as the voltage cannot be raised any more. The flux decreases linearly with the frequency and the current. The maximum torque also decreases. The flux and the current decrease linearly with frequency. Hence the maximum torque is inversely proportional to the frequency<sup>2</sup>

The corresponding road speed for a 0.32m wheel diameter at 20Hz is **18,3 km/h**. This also corresponds to peak power.

#### 8.5 Load Tests when Chopping

The chopping frequency must be a multiple of 16 times the inverter fundamental frequency, by virtue of the constraints of the logic of the interlaced inverter. The chopping frequencies which are available at 12.5Hz fundamental frequency are :- 200, 400, 800, 1600, The chopping frequency of 800 was used as it was found to give the most favourable performances. Load tests at 48 battery voltage, 5/3M/S ratio were performed (see fig 8.6) so as to compare them with the equivalent of 30 volt at full M/S results obtained in figure 8.3. The obtained torque is somewhat higher than that at 30 volt full M/S and lies between the result obtained for 30 volt and 36 volt full M/S. This is due to the fact that the volt drop due to regulation of the supply and inverter, is more pronounced for 30 volts, full M/S than 43 volts 5/3 M/S as it's supply current is higher. The

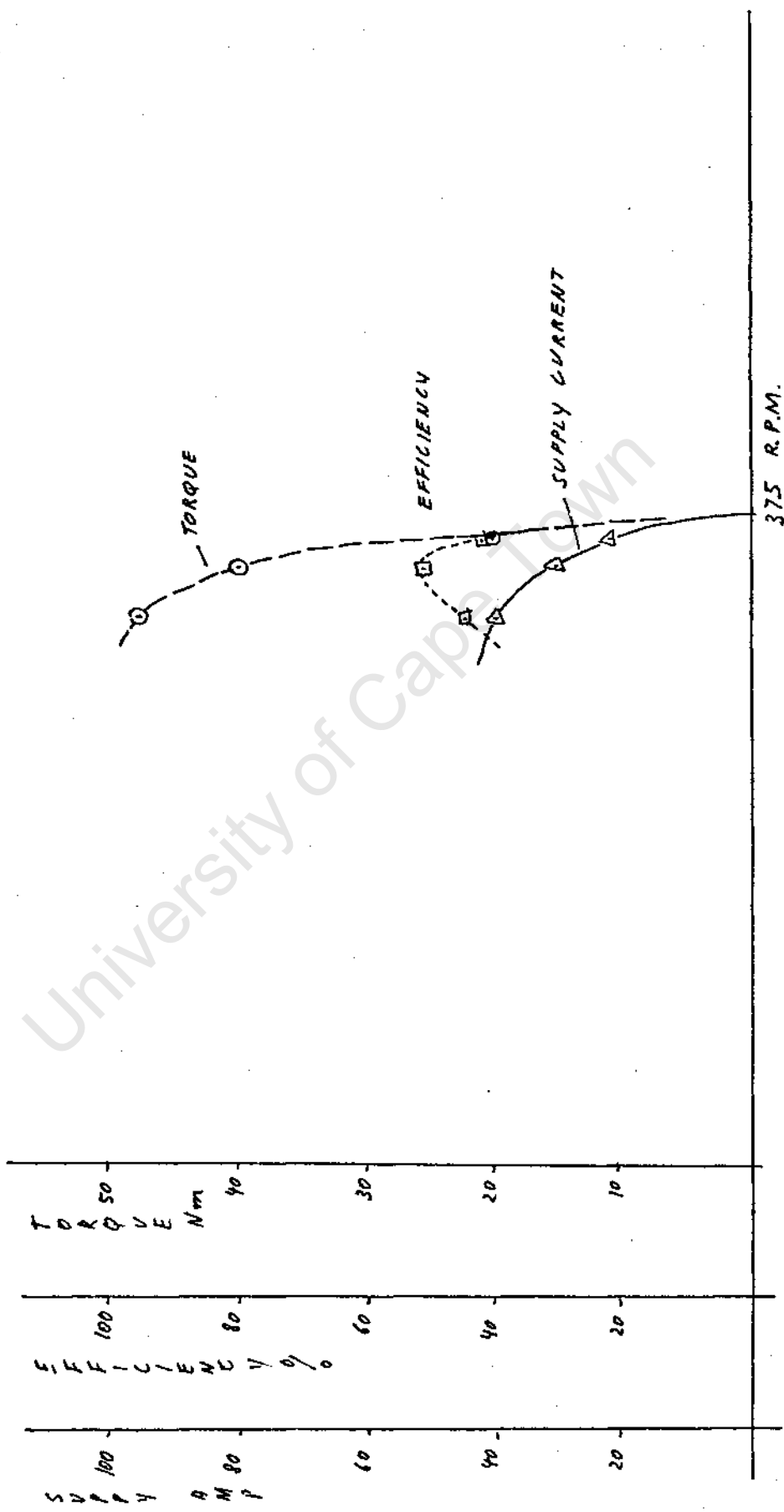


Figure 8.6 Torque, Efficiency, Supply Current VERSES Speed  
 for 43 Volt Battery Voltage, 5/8M/S, I2.5Hz, 800Hz  
 Chopping.

same can be observed for 36 volts at 5/3 M/S (see fig 8.7) and 24 volts at full M/S (see fig 8.2). The difference in efficiency between the two modes is about 25. This is accounted for by the switching losses and the effect of ripple phase current due to the chopping frequency.

### 8.6 3 Phase sinusoidal. Test

**The** 9 phases were combined so as to produce **a** 3 phase motor. Three of the phases were connected in series to obtain one phase. Tests were carried out to enable some comparisons between the efficiency of the motor when 3 phase connected, sinusoidally fed, and the efficiency of the 9 phase induction motor. The tests --, were superficial and approximate as the motor and inverter will need further alterations. A brief attempt was made at comparing the efficiency at 30 volts full M/S, 12.5 Hz and the equivalent average voltage per conductor when supplied at 75 volts and 12.5 Hz for the 3 phase motor. The characteristics of the 3 phase motor were obtained at 50 Hz and the characteristics calculated for 12.5 Hz operation (see appendix H). A maximum efficiency **of** 75% was calculated in the case of the 3 phase motor when running at 12.5 Hz and 75 volts. When compare with the overall maximum efficiency of 62.5% obtained from the 9 phase inverter **fed** motor the efficiency is appreciably less. If the inverter losses are subtracted then the efficiency of the 9 phase inverter fed motor is 67%. The difference of **8%** could be attributed to increased copper losses due to the substantial phase current ripple experienced with the present 9 phase inverter fed motor. The low efficiencies at 12.5Hz are to be expected as the copper losses **are** of importance at low frequencies, It was unfortunate that the motor could not be properly fluxed for frequencies over 20Hz

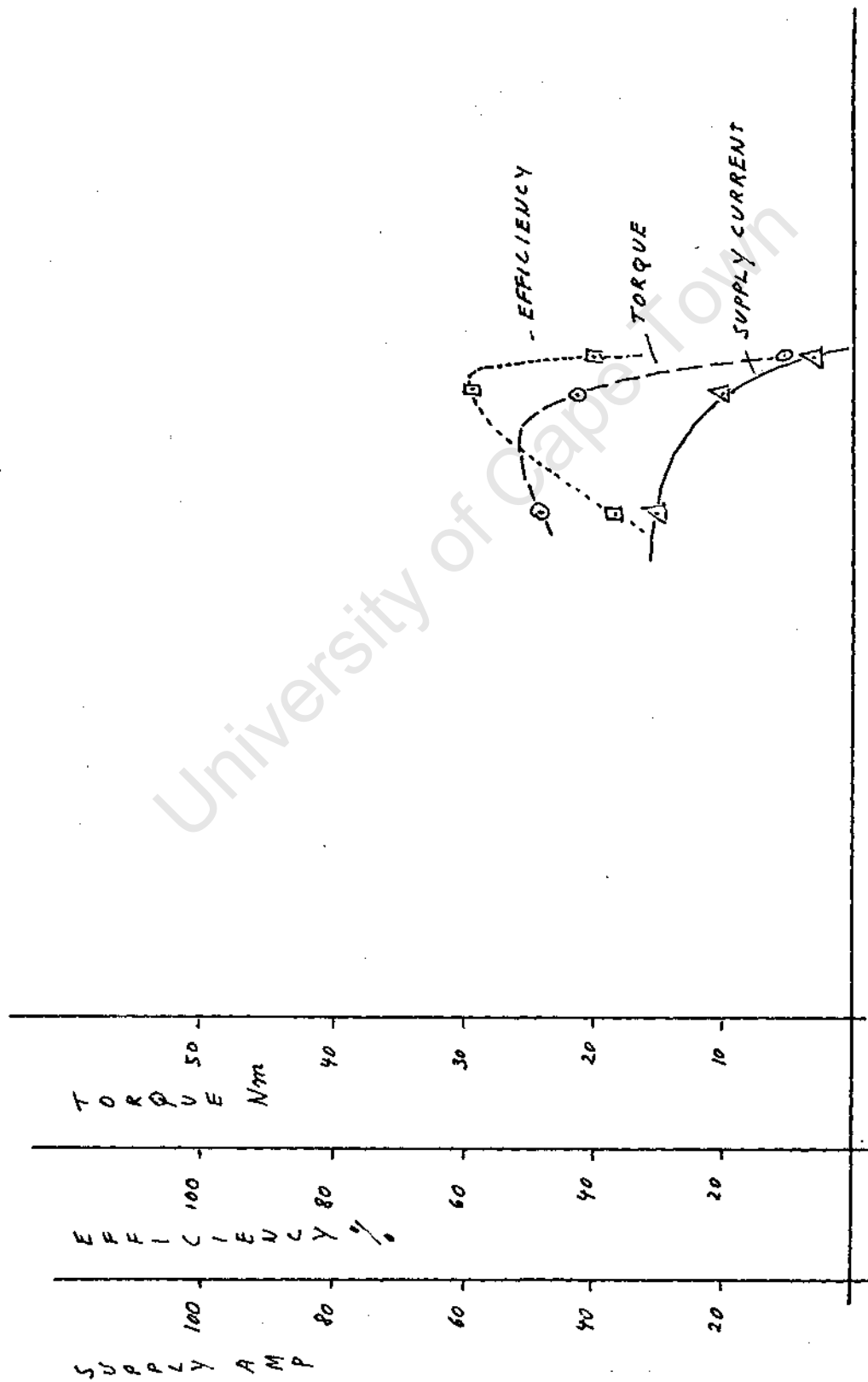


Figure 8.7 Torque, Efficiency, Supply Current of 9 Phase Interlaced Motor for 36 Volt Battery Voltage and 5/8 M/S, 12.5Hz, 800Hz Chopping.

especially when considering that the maximum efficiency of 89% was measured when running the motor on 3 phase at 250 volts and 50 Hz.

### 8.7 Oscillograms.

Oscillograms of phase voltage, phase current and supply current for different operations are shown in figures :- 8.8, 8.9, 8.10 and 8.11. The phase current and supply currents were monitored with hall effect transducers. From these oscillograms it is noticed that the voltage wave form has virtually no voltage peaks over and above the battery voltage. Therefore the transistors can be effectively used at relatively high voltage compared with normal types of choppers (ie 60 volts for a VCEO max of 90 volts). The phase current unfortunately has pronounced ripples. When comparing with the smooth phase current obtained with the 9 phase motor (A) of appendix H the difference is disturbing. Further investigation will be carried out so as to obtain a smoother phase current. A probable answer is that the present motor is unskewed while the motor of appendix H is skewed. Fractional winding, and the fact that the number of slots per pole (4) is not an integral number should have reduced the effect of slot harmonics but is not sufficient.

### 8.8 Proposed Modification to Motor

The torques measured with the present motor at different frequencies for maximum voltage (shown in figure 3.5) are replotted verses vehicle speed when using a 32cm wheel diameter. These are shown in figure 3.12 and compared with the desired torque of figure 7.3 of appendix G. The maximum desired stalling torques were achieved but unfortunately the torque drops quickly with speed as the motor becomes underfluxed. The motor will be

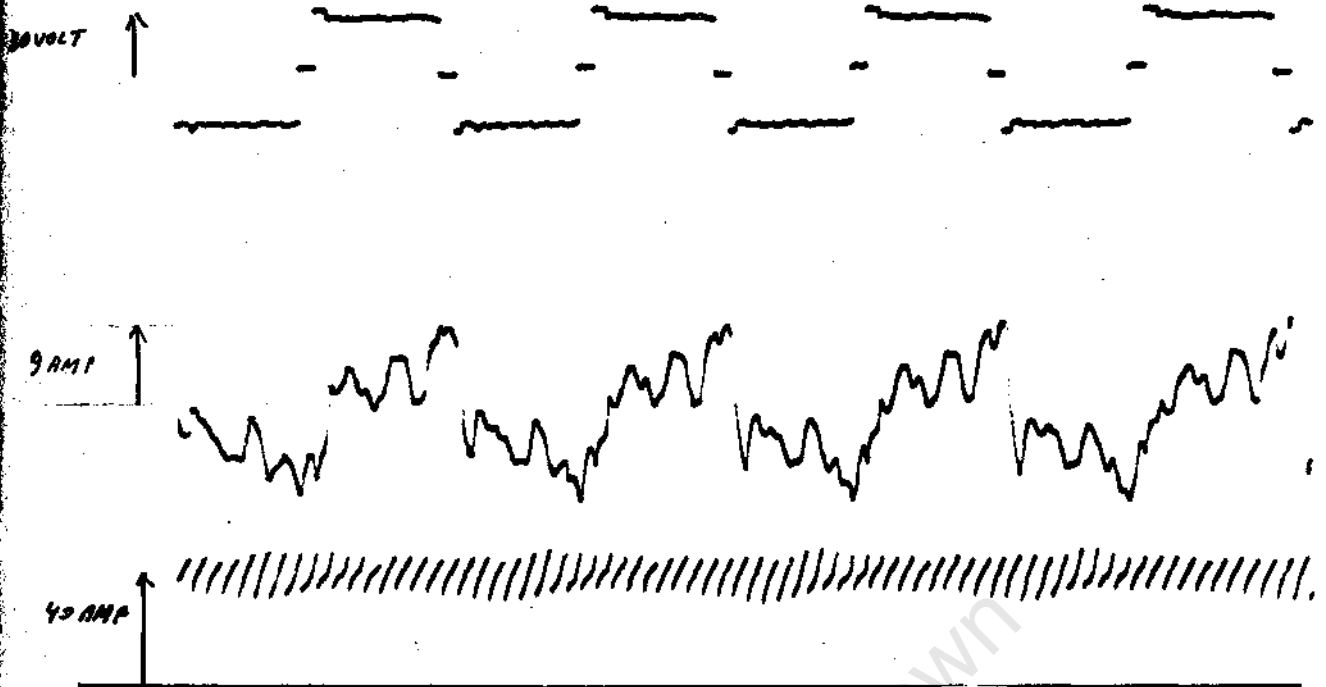


Fig 8.3 Oscilloscope for Battery Voltage of 36 volts, full M/S, 12.5Hz, 40 amp supply, 35.5 Nm torque.

a) Phase voltage. b) Phase current. c) supply current

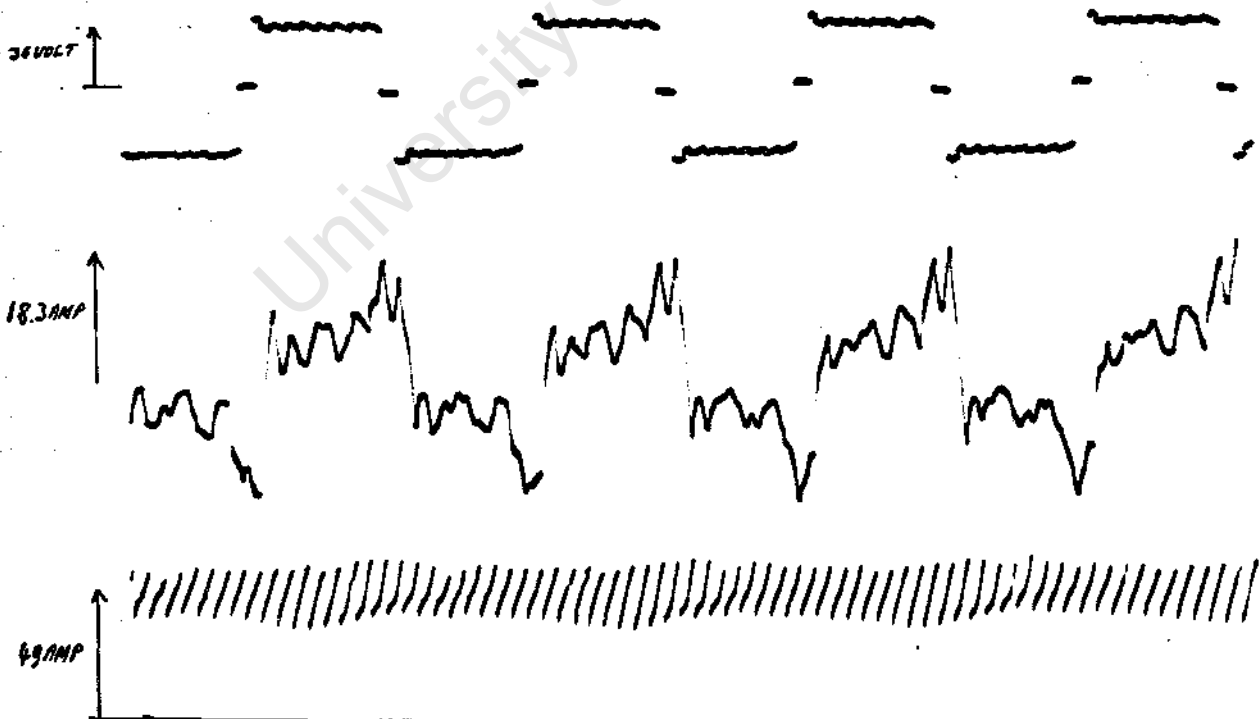


Fig 3.9 Oscilloscope for Battery Voltage of 36 volts, full M/S, 12.5Hz, 49 amp supply, 50Nm torque.

a) Phase voltage. b) Phase current c) Supply current

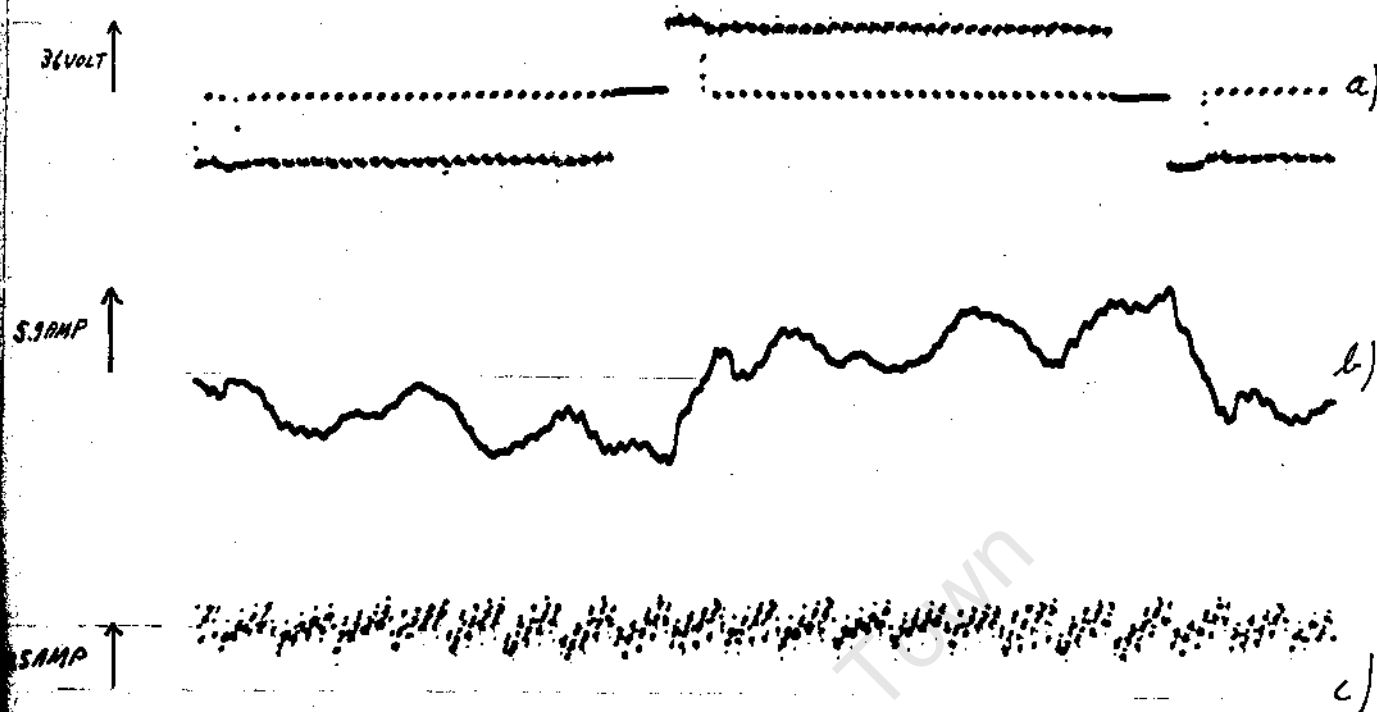


Fig 8.I0 oscillogram for Battery Voltage of 36 volt, 6/8 M/S, 12.5 Hz, 30 amp supply, 25 Nm torque.  
 a) Phase voltage. b) Phase current c) Supply current

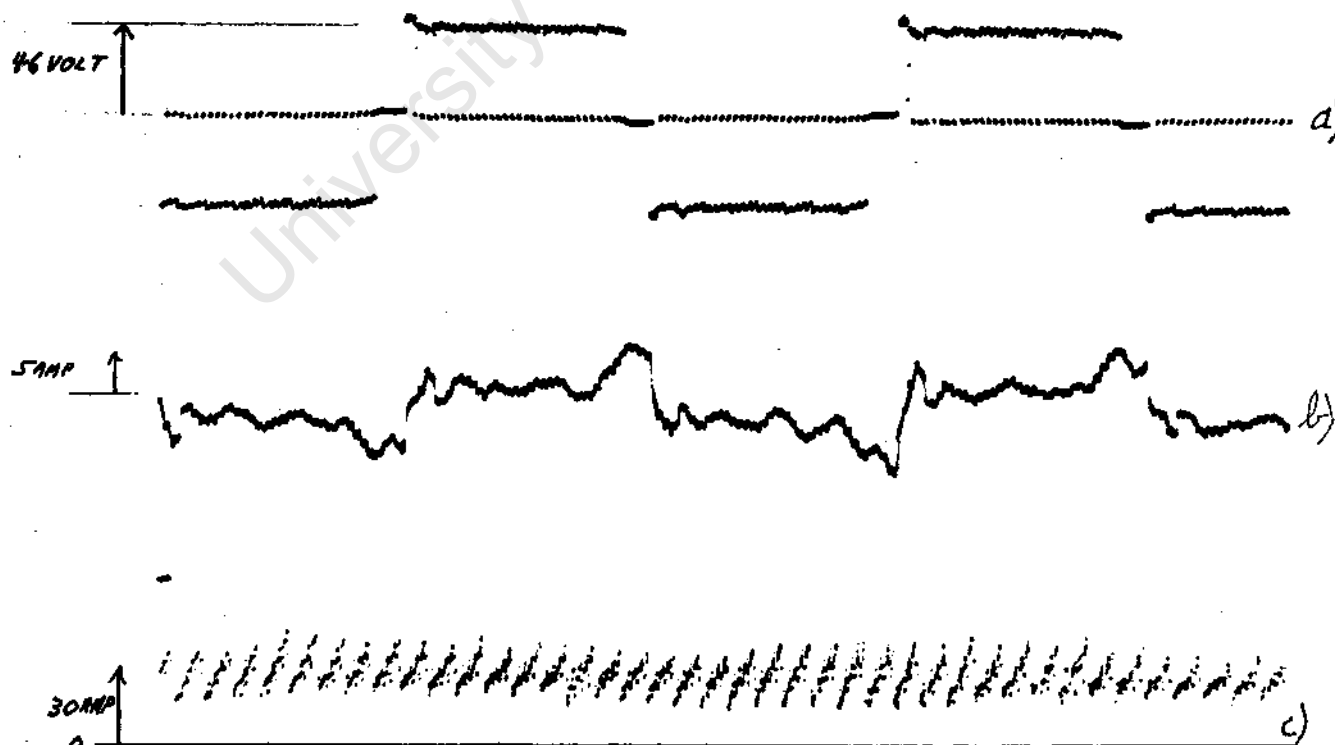


Fig 8.II Oscillogram for Battery Voltage of 43 volts, 5/3 M/S, 12.5Hz, 300Hz chopping, 30 amp supply, 40Nm torque.  
 a) Phase voltage b) Phase current c) Supply current

modified by reconnecting the winding so that there will be 2 parallel paths per phase (ie half the conductors in series per phase Newly available and cheap Darlington transistor packages MJ1015 and MJ1016 (30 amp rating 120 volt VCEO) will replace the present power transistor, driver and freewheeling diode. The battery supply voltage will be raised from 60 to 90volts. The result will be that the torque obtained will be 2.25 (ie $(90/60)^2$ ) times as much and at twice the speed. The expected torque is shown in figure 8.12. To maintain 125Nmon stalling the numbers of transistors will be doubled up. Each of the 9 phases will, consist of two parallel windings each connected to a single phase inverter. The two single phase inverters will be controlled simultaneously by the Present logic. Although the numbers of transistors will be doubled up the Darlington single package transistor, which replaces the power transistor, driver and freewheeling diode, will\*ender the construction less complicated. Also it is hoped that more powerful, cheap transistors will enable reduction in the numbers of required transistors.

More investigation of the motor design will be carried out to improve the efficiency, simplicity and reduce costs.

The logic will have to be developed to control the motor in a closed loop so as to obtain efficient and flexible operation from the accelerator and brake pedals.

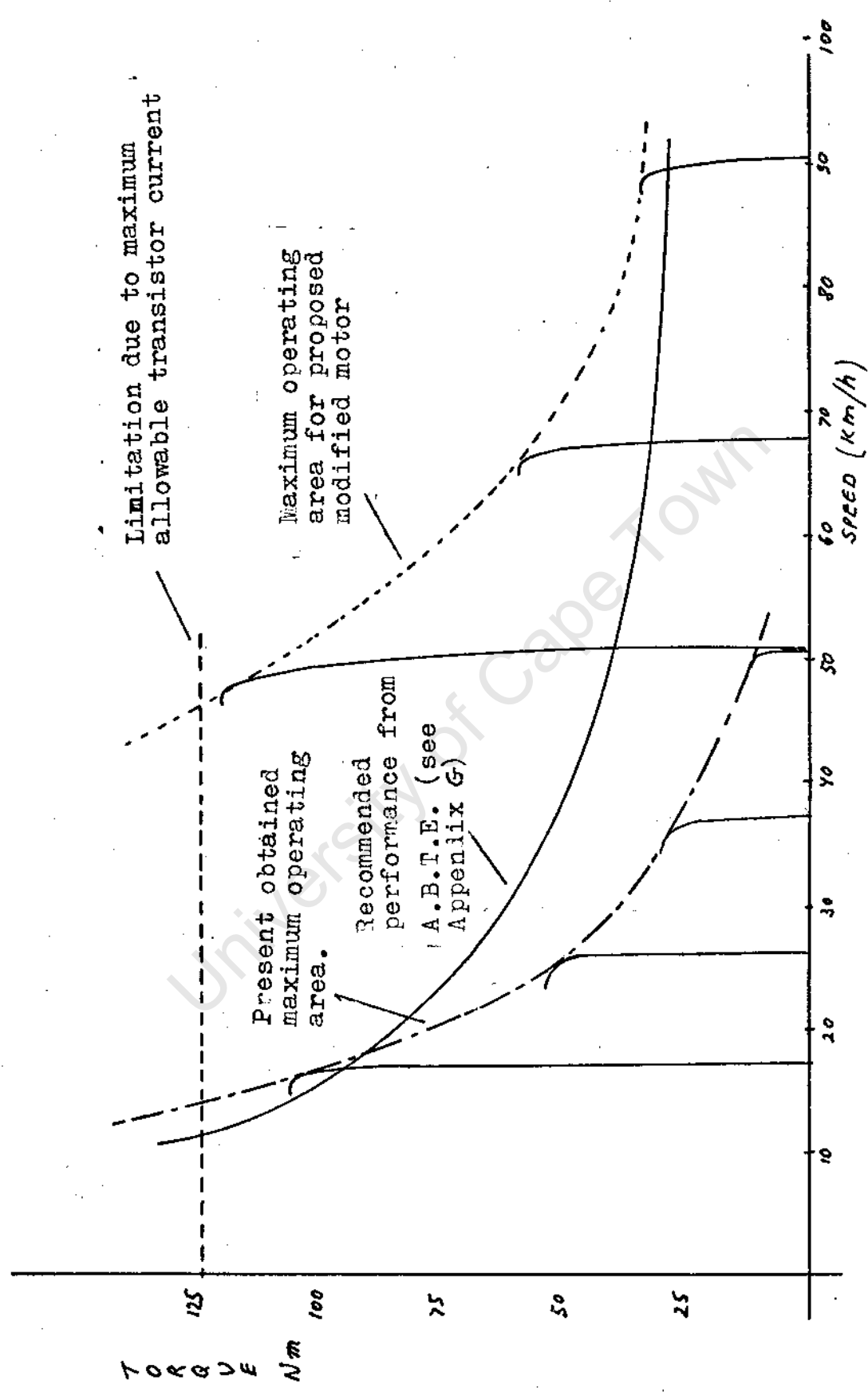


Fig 3.12 Maximum torques Per motor limits for :- Present, Proposed modified motor and recommended performance from Australian Bureau of Transport Economics (see appendix G)

## Conclusion

The project has succeeded in producing a viable drive with very high stalling torques enabling direct coupling to the wheel. The novel construction adopted has proved to be a success and has set the foundation for further improvements towards an economical battery operated motor.

The method of interlacing between the phases has produced numerous advantages, namely :-

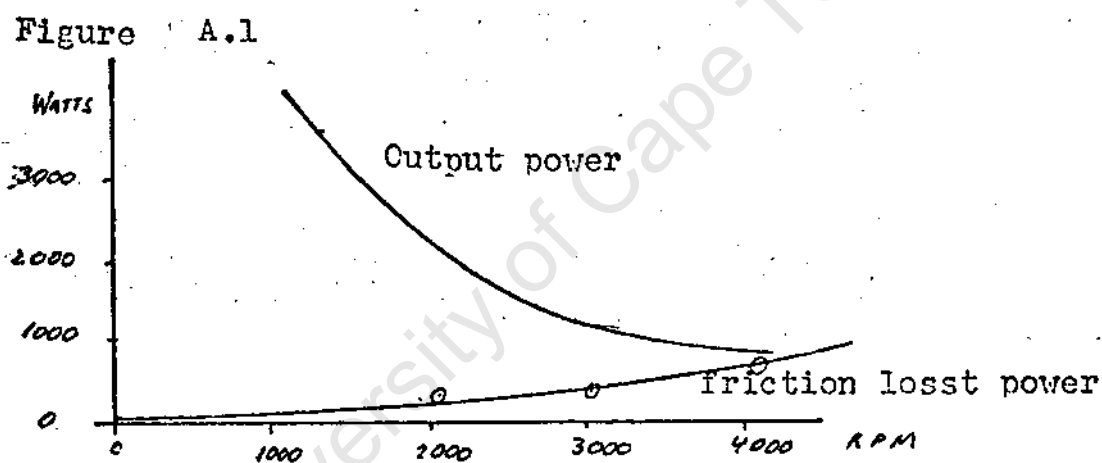
- 1) Continuity of the supply current.
- 2) Suppression of induced voltages due to supply inductance when chopper modulating,
- 3) D.C. transformer action of inverter enabling high torques with little current demand on the supply battery.
- 4) Reduction of switching losses due to stored magnetic energy when chopper modulating.

The multiplicity of phases has enabled high utilisation of the transistors.

It was unfortunate that the motor could not be properly fluxed at higher speeds, therefore no impressive efficiencies were recorded. However with future modifications and investigations there are no reasons to believe that overall efficiencies up to 90% should not be achieved with a direct to wheel drive for a battery vehicle.

## APPENDIX A

Tests to measure the frictional losses of the differential on the melex battery car were made. The series D.C. motor is coupled to the differential with a worm type gear. The motor is rated at 36V, 57 amp, 2.1 h.p. at 2 800 r.p.m. The motor and differential assembly were driven from the wheel side by an auxiliary drive through a system of pulleys. The frictional torque of the differential and bearings was measured and is shown on Figure A.1.



Output power and friction loss of melex motor and differential assembly

At Nominal output of 1 580w the losses amount to as much as 20%. The differential is no doubt a very -- inefficient part of an electric vehicle. However, this type of transmission (worm gear) is very inefficient and would not normally be used in an electrical passenger car. 10% loss would be a more realistic figure.

HARMONIC CONTENT OF VOLTAGE WAVEFORM

The harmonic content of the voltage waveform of the single phase full bridge inverter can be expressed as a function of the conduction angle

$$\begin{aligned}
 V_{(a-b)} &= \sum A_n \cos n\omega t \quad n = 1, 3, 5 \\
 A_n &= \frac{2}{\pi} \int_0^{\pi} V_{(a-b)} \cos n\omega t \, d\omega t \\
 V_{(a-b)} &= V_B \quad \text{for } 0 < \omega t < \gamma \\
 V_{(a-b)} &= 0 \quad \text{for } \gamma < \omega t < \pi/2 \\
 A_n &= \frac{4}{\pi} \int_0^{\gamma} V_B \cos n\omega t \, d\omega t \\
 &= \frac{4}{\pi} V_B \left[ \frac{\sin n\omega t}{n} \right]_0^{\gamma} \\
 &= \frac{4 V_B}{n \pi} \sin n \gamma \\
 V_{(a-b)} &= \sum_n \left( \frac{4 V_B}{n \pi} \sin n \gamma \right) \cos n\omega t \\
 n &= 1, 3, 5, \dots \\
 V_{(a-b)}(n, m) &= \frac{4 V_B}{n \pi} \sin n \gamma
 \end{aligned}$$

The maximum value of the fundamental component occurs when  $\gamma = \pi/2$  or  $V_{a-b}$  is a square wave, and is

$$V_{(a-b)}(1, m) \Big|_{\gamma = \pi/2} = \frac{4 V_B}{\pi}$$

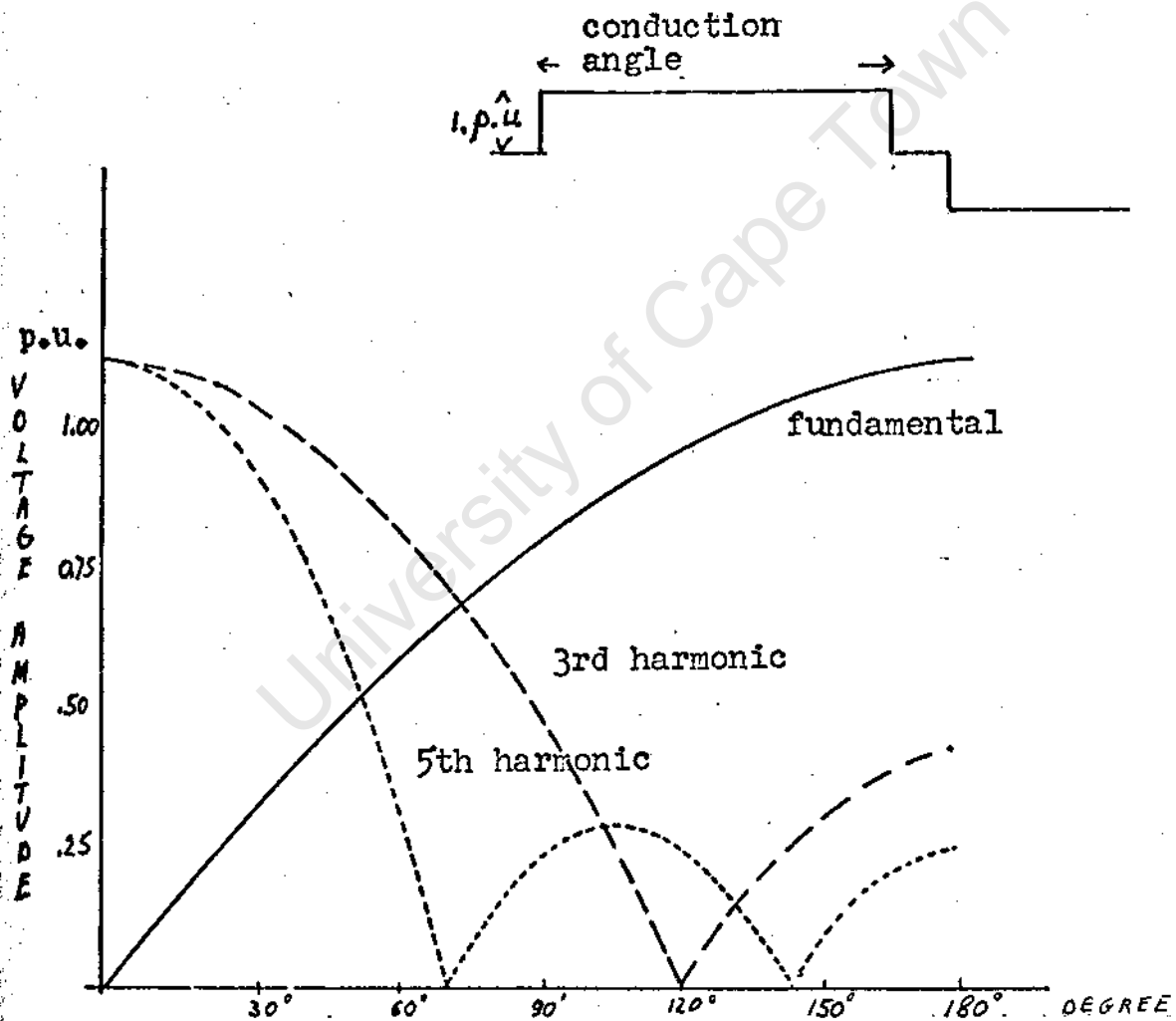
In the particular application used

$$\gamma = 160^\circ$$

$$V_a - b(1, m) \Big|_{\gamma=160^\circ/\pi} = \frac{4 V_b}{\pi} \sin 80^\circ = 1,253 V_b$$

the variation of the fundamental and harmonic content with conduction angle is given in Figure 7.1.

Figure B.1



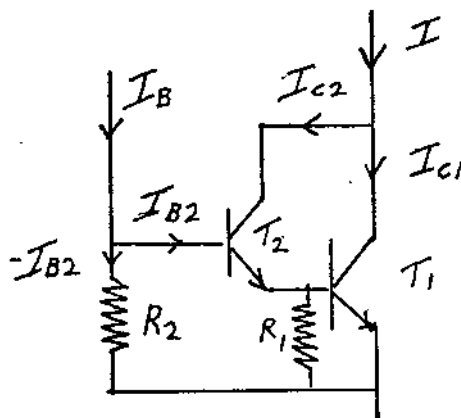
Characteristic showing the voltage output harmonic content for a quasi-square voltage waveform for different conduction angle

## APPENDIX C

### DARLINGTON CONFIGURATION DESIGN

The NPN and PNP transistors are complementary transistors with identical specifications. The design calculation of the one applies to the other as well. Considering the NPN transistors in a darlington pair configuration see Figure C.1 The values of  $R_1$ ,  $R_2$  and  $I_B$  are calculated by a method which assumes that it is very unlikely that both transistors of the darlington pair will have minimum gain. To compensate for this assumption, the contribution of  $I_{c2}$  to the load current is ignored. The manufacturers specifications for the transistors used are given at the end of this Appendix. (See Fig C.2)

Fig C.1



Power Darlington stage circuit.

$T_1$  : Assume  $h_{fe}$  = typical value

$h_{fe}$  at 25A =  $80 \times 1.2 = 9.6$  say 10

$I_{B1} = \frac{25}{10} = 2.5A$

$R_1$  and  $R_2$  are to enable quick removal of charges stored in the depletion layer, when the transistor is switched off. The value of  $I_{B1-}/I_B$  depends on design requirement. It was found that  $I_{B1-} \approx 0.12 I_{B1}$  gave adequate switch off time ( $\approx 10 \mu s$ )

$$R_1 = \frac{V_{BE1}(\text{sat})}{0.15 I_{B1-}} = \frac{1.6}{.12 \times 2.5} = 5.3 \Omega$$

$$I_{B1-} = 0.12 \times 2.5 = 0.3 \text{ A}$$

$$I_{C2} = 2.5 + 0.3 = 2.8 \text{ A}$$

$$T_2 \quad h_{fe} \text{ at } 2.8 \text{ amp} = \frac{1}{2} 40 = 20$$

$$I_{B2} = \frac{2.8}{20} = 140 \text{ mA}$$

$$R_2 = \frac{V_{BE2}(\text{sat}) + V_{BE1}(\text{sat})}{0.12 \times .140} = \frac{1.6 + 1.1}{0.12 \times .140} = 166 \Omega$$

$$I_B = .140 + 0.016 = .156 \text{ A} = 156 \text{ mA}$$



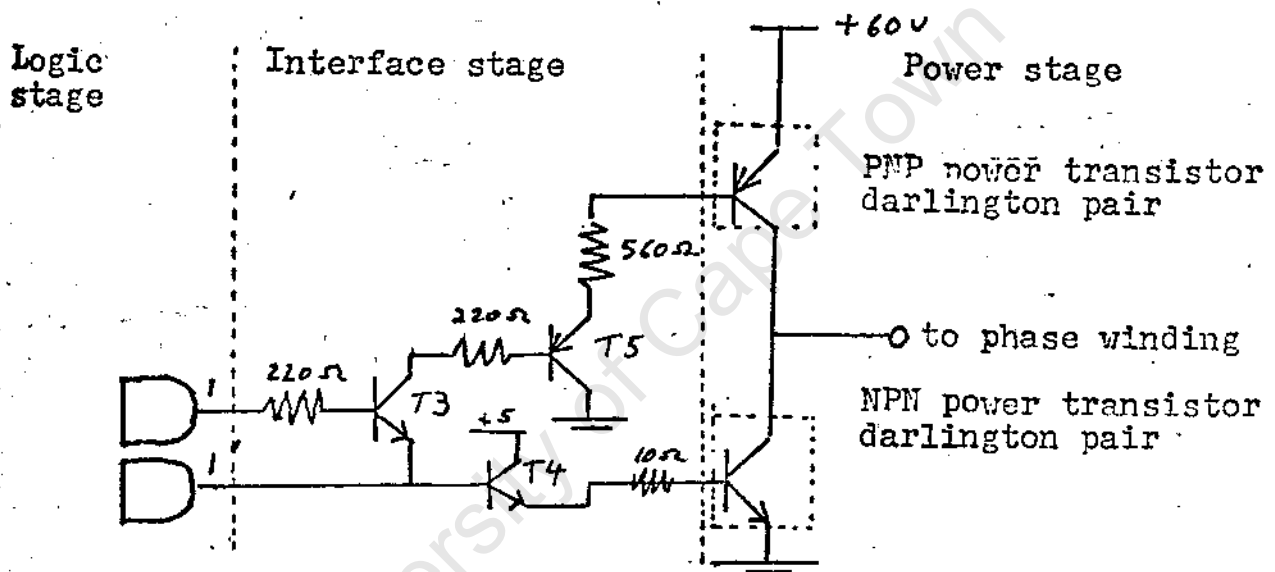
## APPENDIX

### INTERFACE BETWEEN DARLINGTON PAIRS AND TTL LOGIC CONTROLLER.

The interface circuits provide the tie between the TTL logic and the power Darlington transistors-

The NPN and PNP darlington pairs are controlled from the logic level as shown in Figure 7.3.

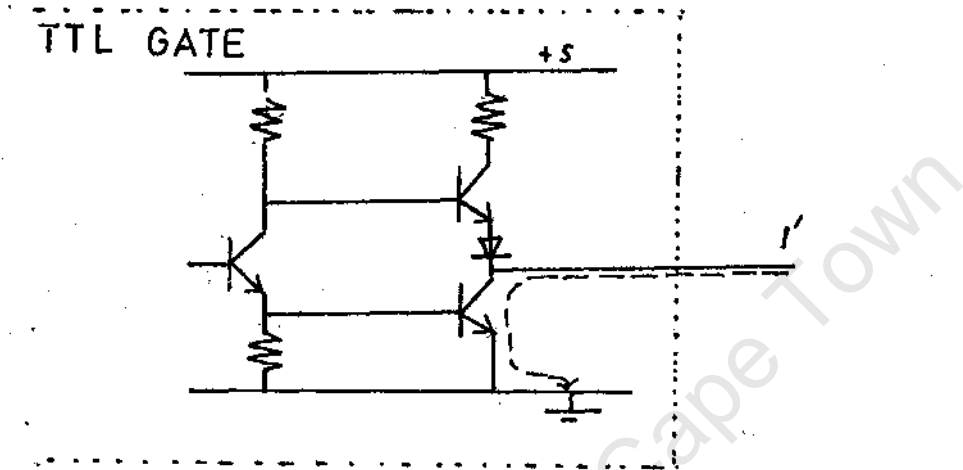
Figure D.1



Cheap transistors  $T_3$ ,  $T_4$ ,  $T_5$  are used to interface.  $T_3$ ,  $T_4$  are MPS A06 a NPN transistor and  $T_5$  a MPS 56 a PNP transistor. With this circuit both positive and negative rails are controlled from the same voltage level.  $T_3$  emitter is not connected to ground but to the logic gate of the opposite leg. This provides effective interlocking to prevent both legs coming on simultaneously, in the case of both logic gates switching on due to noise or malfunction of the controller.  $T_3$  can only be biased if , and only if, gate

is "off". The applied logic signal of gate can only return to ground through gate 1. See Figure D.2.

FIGURE D.2



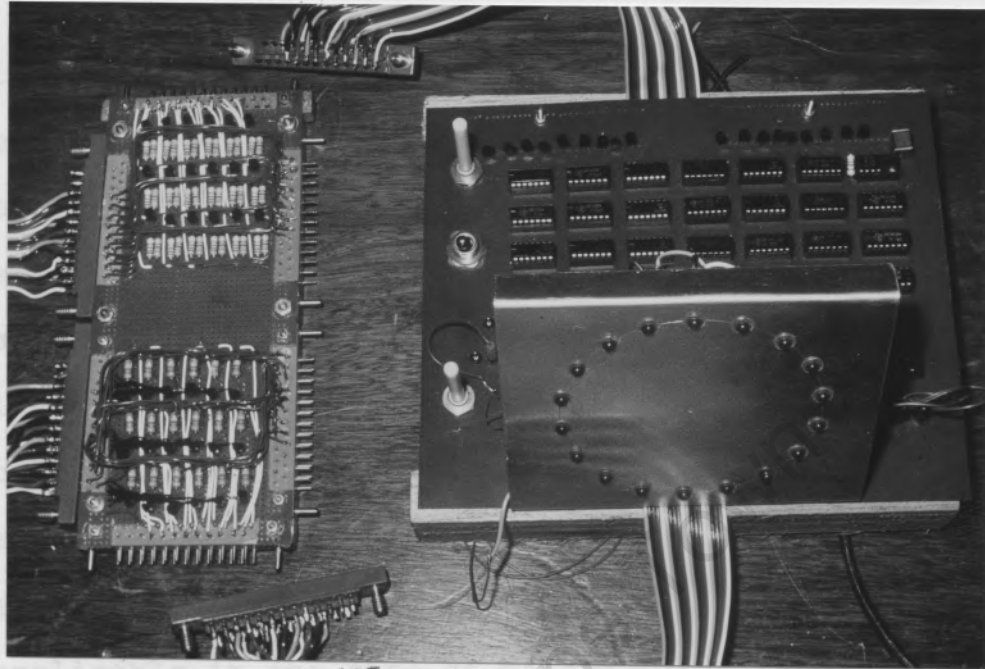
Internal circuit of TTL gate

The interface stage between the logic stage and the power stage can be seen on the left hand side of figure D.3

This interface stage has also the necessary terminals to operate a second identical motor.

## APPENDIX E

Fig D.3



Left: Interference <sup>ACE</sup> stage

Right: Logic

Graph I illustrates how the dynamic losses increase linearly with frequency for a constant voltage and current. One can attempt to separate the last two terms (see Chapter 1.6) by studying the graphs. Graph I indicates that at low voltages the increase in loss is minimal with frequency increase. Therefore, the term which is voltage independent can only be very small. It can be ignored provided the current is low, as it obeys the square law. This is indeed the case in the 9 phase inverter where only 1/9 of the total amount of current is ever switched at any particular time. The  $V_{in}(I_r + I_t)f$  term becomes significant

## APPENDIX E

The losses involved in the switches for a particular phase where measured with two wattmeters of an accuracy of 5% up to 400 Hz. Although higher frequency components are present in the quasi-square voltage waveforms and the non-sinusoidal current, it was found to give adequate results to be able to observe how different parameters affect the losses. Results were obtained driving a resistive and inductive load, and found to differ little. Hence Graph I and II which were taken for resistive load are applicable in the case of motors. The losses were measured for different frequencies, voltages and currents and are summarised in Figures E.1 and E.2.

Graph I illustrates how the dynamic losses increase linearly with frequency for a constant voltage and current. One can attempt to separate the last two terms (see Chapter 3.6) by studying the graphs. Graph **I** indicates that at **low** voltages the increase in loss is minimal with frequency increase. Therefore, the term which is voltage independent can only be very small. It can be ignored provided the current is low, as it obeys the square law. This is indeed the case in the **9** phase interlaces inverter where only 1/9 **of** the total amount of current is ever switched at any particular time. The  $\frac{V_b I_m (I_r + I_t) f}{2}$  term becomes significant

at high frequency as it is linearly proportional to frequency. Since motor losses due to ripple current decrease with frequency an optimum chopping frequency exists.

Fig E.1 Variation of switching losses with frequency and voltage with an average current of 5 amps and a quasi-square voltage waveform of 160° conduction angle in a transistor inverter

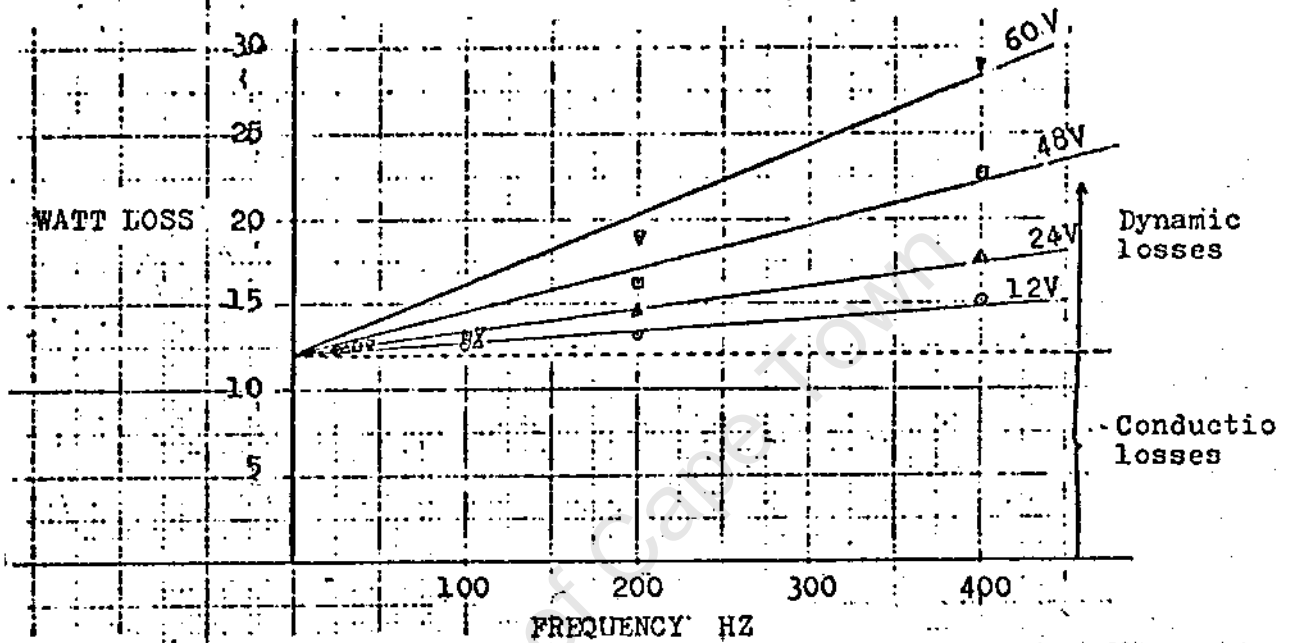
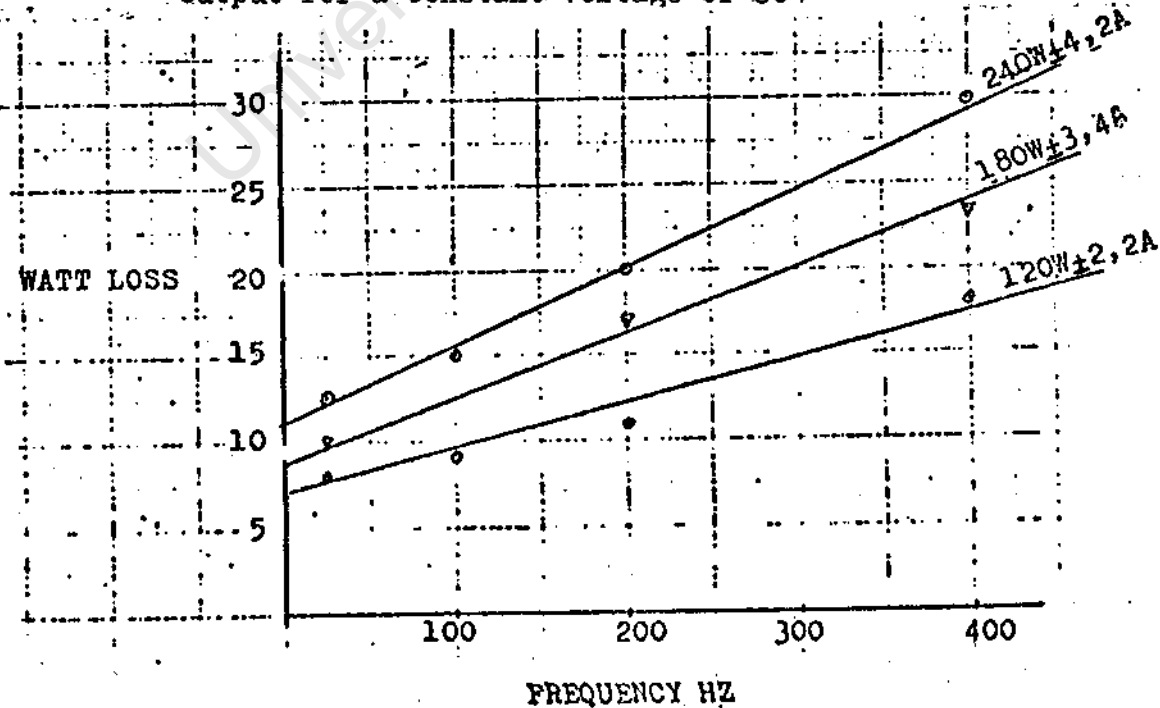


Fig E.2 Variation of switching losses with frequency and power output for a constant voltage of 60.



## APPENDIX F

### CONSTRUCTION, DESIGN AND PERFORMANCE OF TWO INTERLACED DRIVEN INDUCTION MOTOR PROTOTYPES

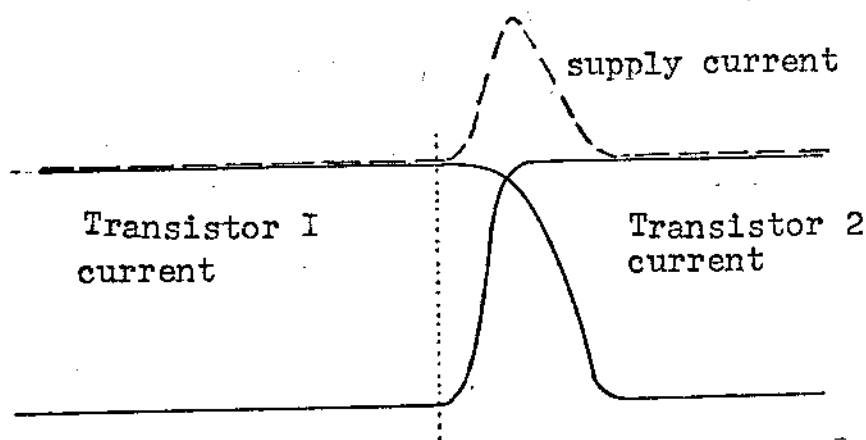
Two inverter fed induction motors were previously investigated, their success led to the described motor in Chapter VI and VII.

#### 7.1 The 6 Phase Interlace Inverter with Feedback

The first interlaced inverter attempt was a six phase inverter with controlled transistor switching rates. The rate of switching on of a transistor cannot be exactly the same as the rate of switching off.

Fence' when commutating from One coil to another the supply current to the two coils wlll vary see figure ,F.2

FIGURE F.1

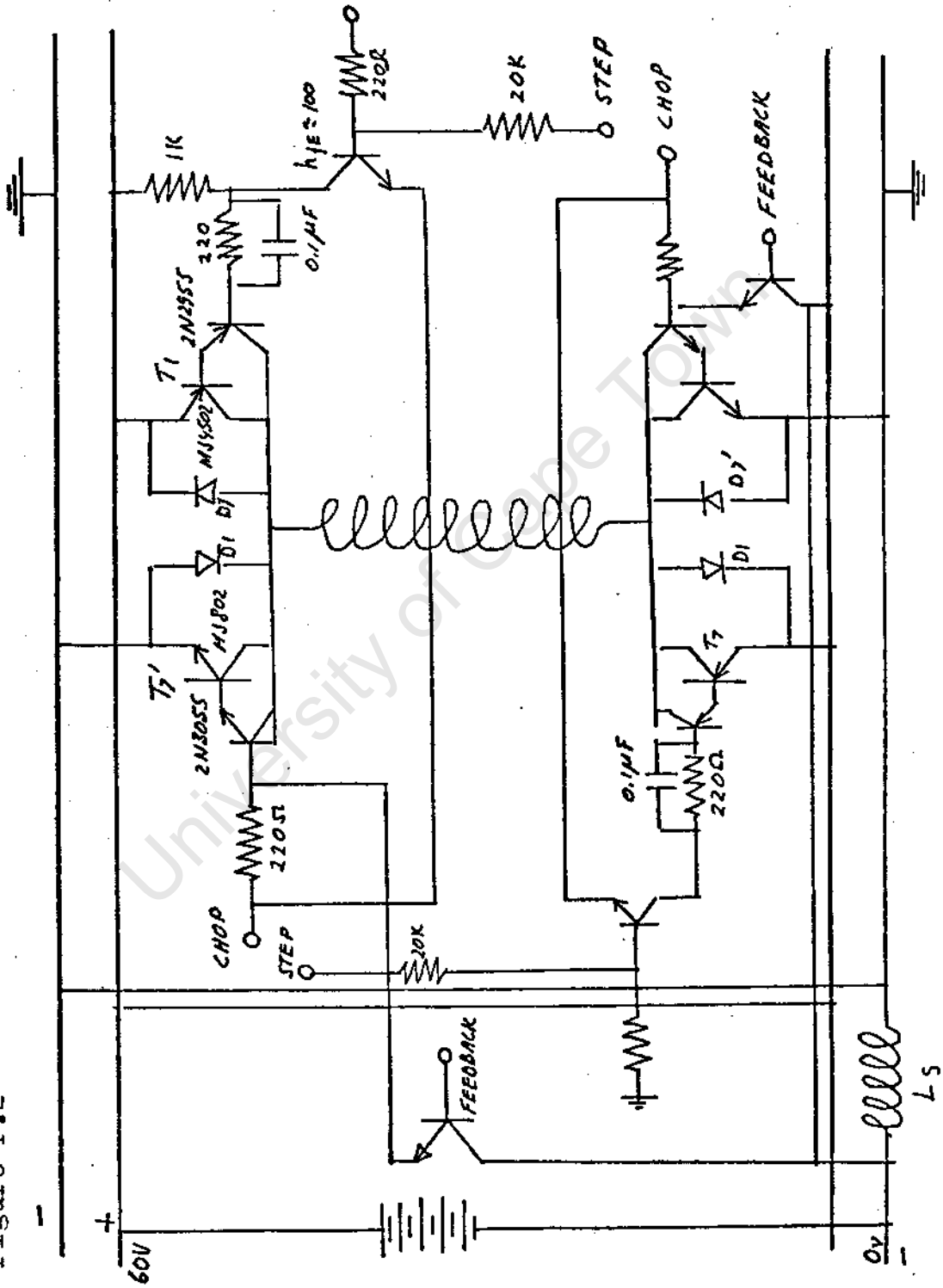


Supply current and transistor current undertaking commutation

Discontinuity of the supply current would produce an induced voltage which could not be tolerated by the transistors. ( $L \frac{di}{dt}$  due to the supply inductance). Hence the transistors were driven in a feedback manner so that the current rate of change of the off-going transistors would control the current rate of change of the switching on transistor.

This was achieved with some degree of success by delaying the signal to the oncoming transistor and controlling the on-coming transistor (during this delay) by a feedback signal from the inductance included in the supply path. When a transistor is switched off a voltage appears across the supply inductance/ ( $L_s$  included between the battery and the negative bus) due to the change of the supply current. This voltage is gated through transistors to the appropriate power transistor which is to come on. Figure F.2 gives the circuit diagram of one phase of the inverter with the transistors which implement the feedback.

Figure F.2



Phase network for controlling the rate of switching when commutating from one phase to another.

The logic which controls the inverter interlacing and modulation is shown diagrammatically in Figure F.3. Pulse generator 1 controls the chopping frequency whilst pulse generator 2 controls the stepping frequency. The logic is similar to the one explained in Chapter V, except for the additional logic control of the feedback signals. The phase voltage waveform obtained is a quasi-square waveform of 150° conduction angle, which can be pulse width modulated for five different M/S ratios (1/5, 2/5, 3/5, 4/5 and 5/5). An available 3/4 h.p., 3 phase motor of 240 volts 50 Hz, whose windings were connected to produce 6 phase, 60 volts, 50 Hz. motor was fed from the 6 phase interlaced inverter. Oscillograms of phase voltage and phase current are shown in Figure F.4, F.5, F.6, and F.7. Torque, supply current and efficiency against speed for a battery voltage of 15 and 30 volts at 25 and 50 Hz respectively is shown in graph F.3 and F.9.

## F.2 A 9 Phase Interlaced Inverter Fed Induction Motor

The motor here described is the first prototype attempt in the design and construction of a 9 phase inverter fed induction motor. Although the torque and power performances were insufficient for a battery vehicle, they established the base for the design and construction

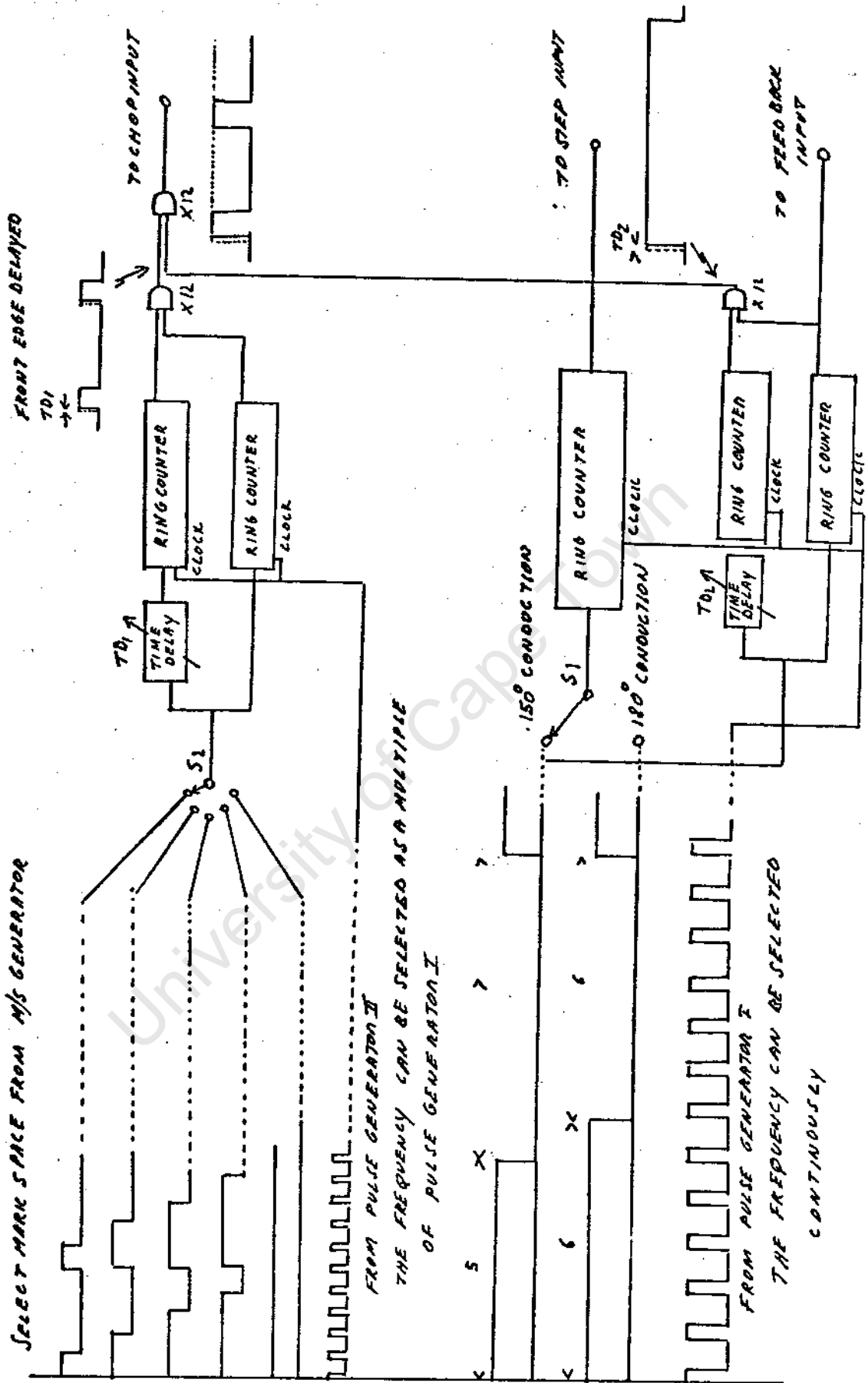


Figure F.6

VOLTAGE AND CURRENT WAVE FORM

FIG. F.4

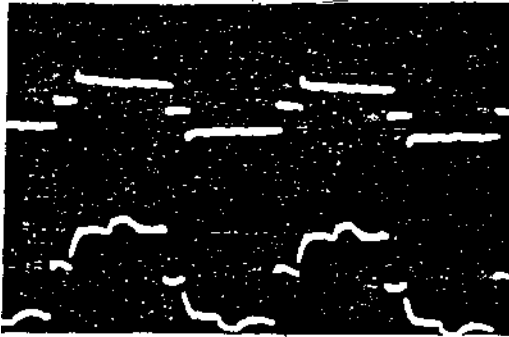


FIG. F.5

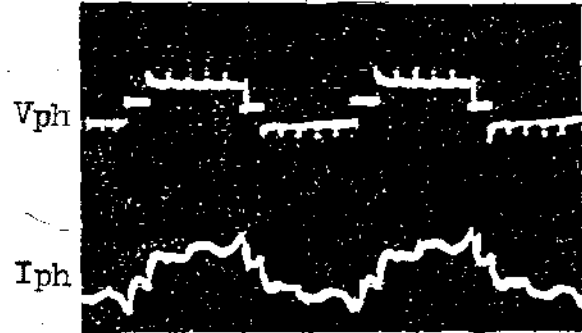


FIG. F.6

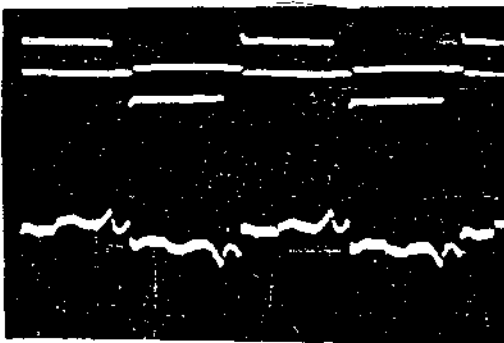


FIG. F.7

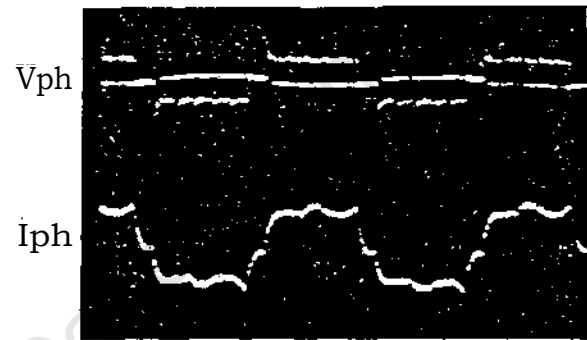


Fig F.4 Small load (+/-150 watts out). 5/5 mark space ratio

Fig F.5 No load 5/5 mark space ratio

Fig F.6 No load 3/5 mark space ratio

Fig F.7 Small load ( $\pm$  150 watts out) 3/5 mark space

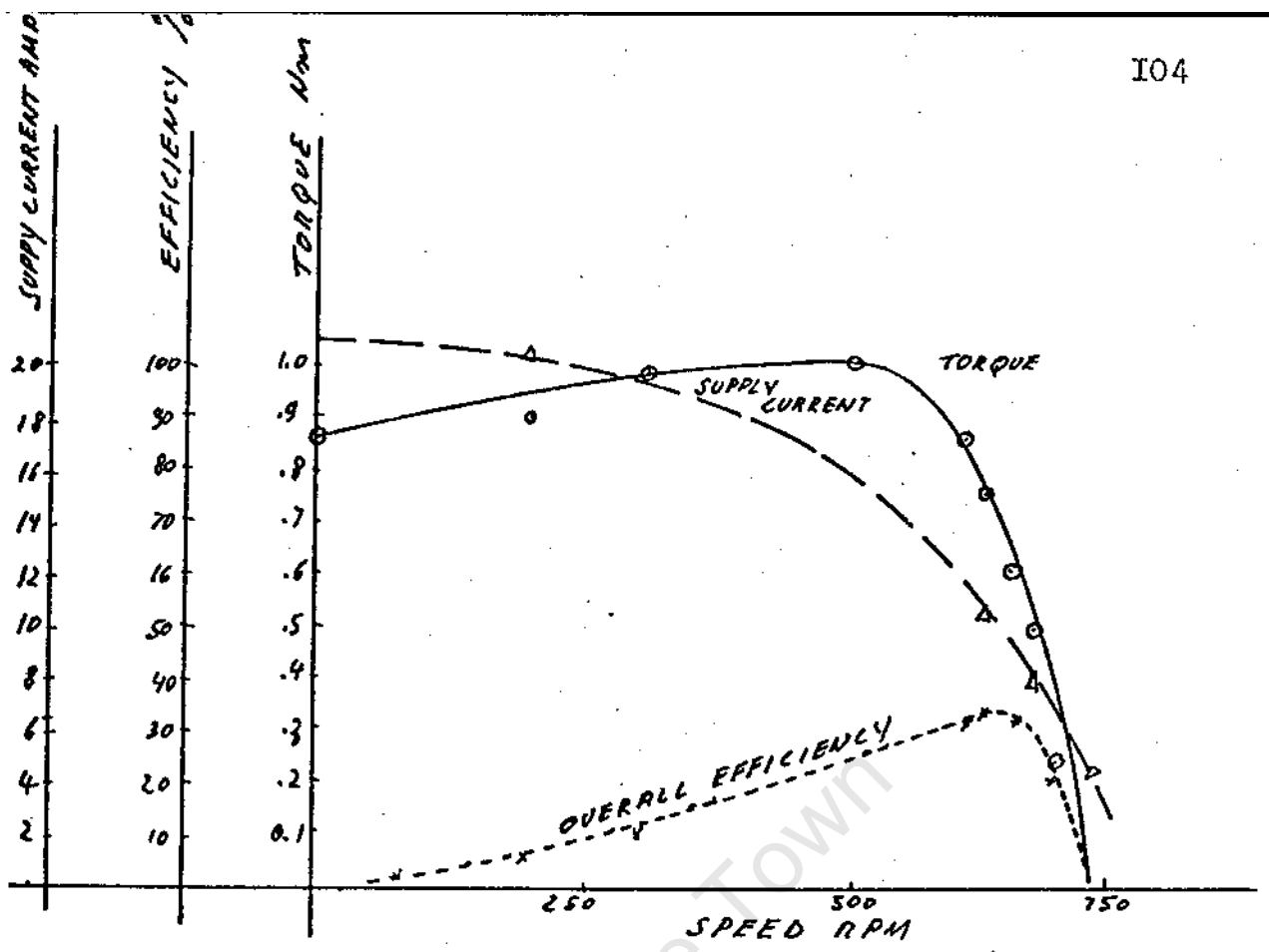


Fig F.8 Torque, Efficiency Versus Speed for 15 volt battery voltage and 25Hz inverter frequency.

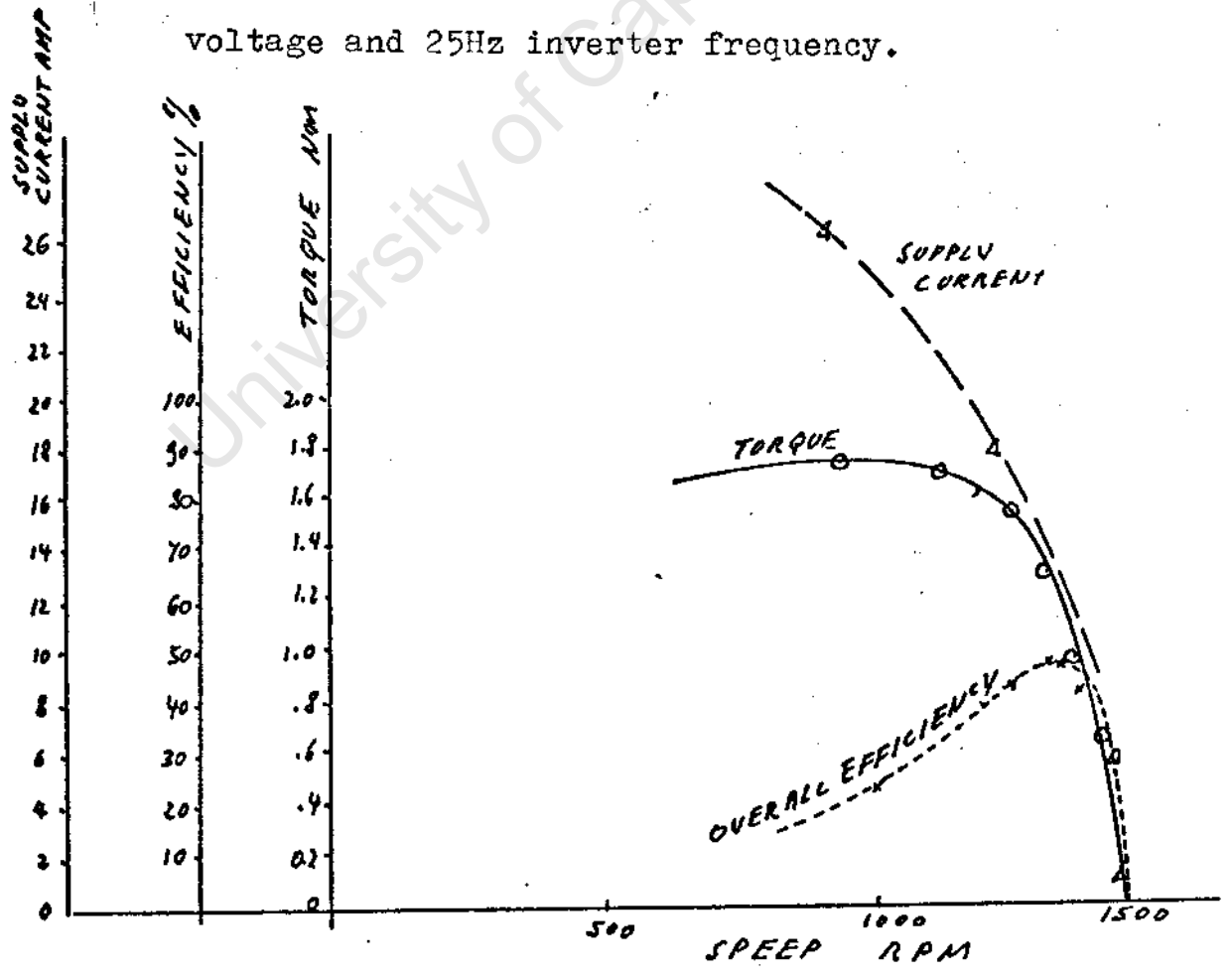


Fig F.9 Torque, Efficiency Versus Speed for 30 volt battery voltage and 50Hz inverter frequency.

of the 9 phase motor described in the project.

### F.2.1 Design of the Induction Motor

A standard type squirrel cage induction motor of rating 3.7kw, 380v, 8.3A, 50 H 980 r.p.m., 6 poles was stripped of it's winding and rewired as a 9 phase 4 pole machine, with a double layer winding and full pitch. The stator comprises of 36 slots, each winding has 9 turns of 2 x swg 14 gauge annealed copper wire. The total number of conductors is  $36 \times 18 = 648$  conductors, each phase comprises of  $648/9 = 72$  conductors in series.

### F.2.2 Dimensions

The motor has a standard frame size C, whose dimensions are :

Outside diameter of stator stamping	:	.25m
Core length	∴	0.12m
Stator bore	:	0.20m
Pole arc of air gap	:	0.157m
Total air gap area	:	0.0754m

NOTE: Skewed rotor

### F.2.3 Expected Torque on Stalling

The estimated torque was calculated using parameters of a standard 3 phase Mawdsley induction motor which produces a maximum force of  $15\ 800\text{NM/M}^2$  for a current loading of  $65\ 300$  amper conductor/m for a  $0.10\text{m}$  long stator. Assuming similar loading and performance, the estimated torque is  $15\ 800 \times 0.0754 \times 0.1 = 119\ \text{N}$ .

The machine total amper conductor to produce  $119\ \text{Nm}$  is therefore  $65\ 300 \times \pi \times 0.20 = 41\ 000$  ampereconductors.

The current per coil =  $\frac{41\ 000}{31 \times 18} = 63$  amperes. The torque per amper is  $\frac{119}{63} = 1.9\ \text{Nm/amp}$

### F.2.4 Maximum Speed at Full Flux

Assuming a square wave flux distribution the average voltage per phase ( $V_{ph}$ ) may be written as :

$$V_{ph} = nBv l$$

where  $n$  is the number of conductors per phase

$B$  is the flux density

$v$  is the velocity of the air gap flux

$l$  is the core length

$$v = \frac{V_{ph}}{nBl}$$

V<sub>ph</sub> for a 60 volt battery and a total transistor volt drop of 2 volt is

$$v_{ph} = (60 - 2) \times \frac{8}{9} = 51.6 \text{ volts}$$

$$v = \frac{51.6}{18 \times 4 \times 0.12} = 5.97 \text{ m/sec}$$

Assuming a wheel diameter of 32 cm, the speed at road surface is  $5.97 \times \frac{16}{10} \times 3.6 \text{ km/h} = 34.3 \text{ km/h}$

#### F.2.5 Laboratory Results

##### (a) Stalling Torque

Maximum stalling torque obtained was measured to be 32 Nm at 1.4 Hz, 15 volts and supply current of 128 amps that is 16 amp average current per phase. The torque per amp per phase is  $32/16 = 2 \text{ Nm/amp/phase}$ . This corresponds well with the predicted torque of 1.9 Nm/amp/phase.

##### (b) Magnetizing Current

Magnetizing curves were obtained by driving the motor with a' coupled dynamometer, so as to obtain no slip. The battery applied voltage was plotted against the supply current (See fig F.11 and F.12).

From these curves it can be seen that saturation occurs for a battery voltage to frequency ratio of approximately 1.28. This is more for lower frequencies as the stator resistance drop becomes of importance.

(c) Load Test

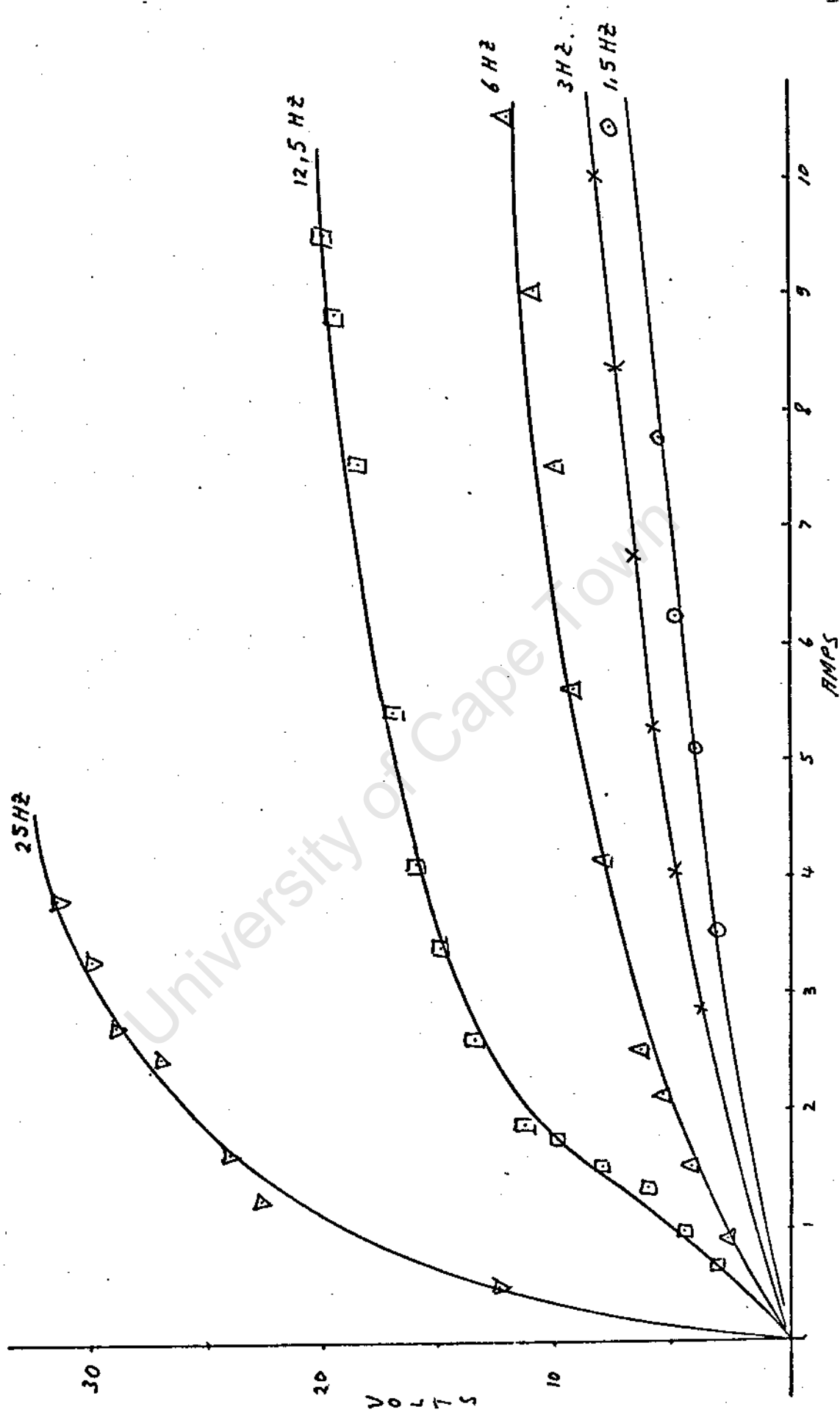
Load tests were performed for different battery voltages at full mark space (i.e.  $160^\circ$  conduction angle with no chopper modulation) and for different frequencies (see Figures F.11, F.12). Fig F.11 shows how the torque remains approximately the same for equal slip frequency if the voltage to frequency ratio ( $v/T$ ) is kept constant.

Fig F.12 shows that at lower frequencies the voltage must be augmented to compensate for the stator resistance and transistor collector to emitter volt drops in the inverter. Fig F. 13 gives torque speed characteristics for a 30-volt battery supply and an inverter frequency of 50 Hz for different mark to space ratios.

(d) Sinusoidally Fed 3 Phase Tests

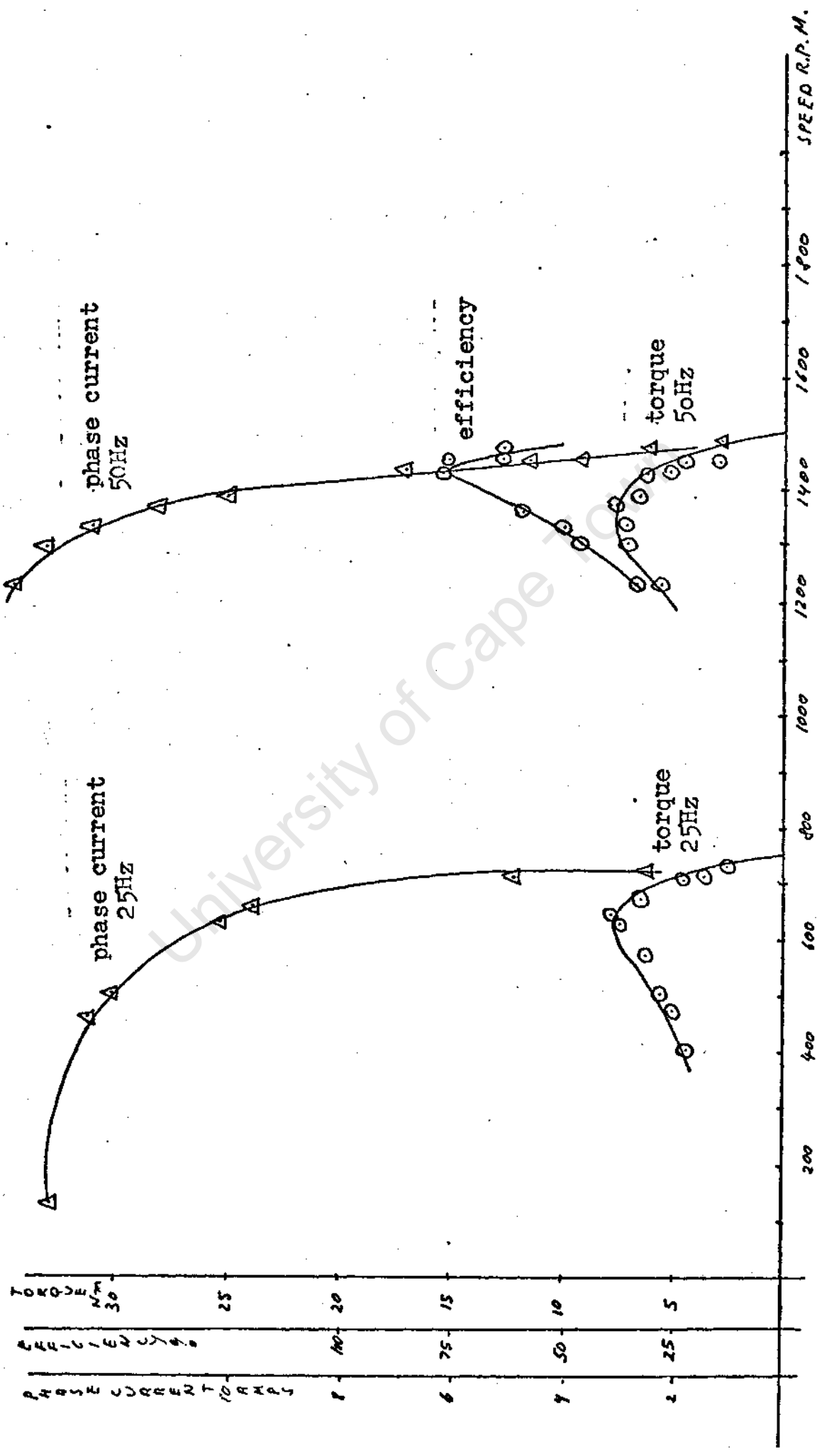
The same motor was connected as a 3 phase motor by connecting 3 windings of the 9 phase motor in series to form each phase.

Fig F.10



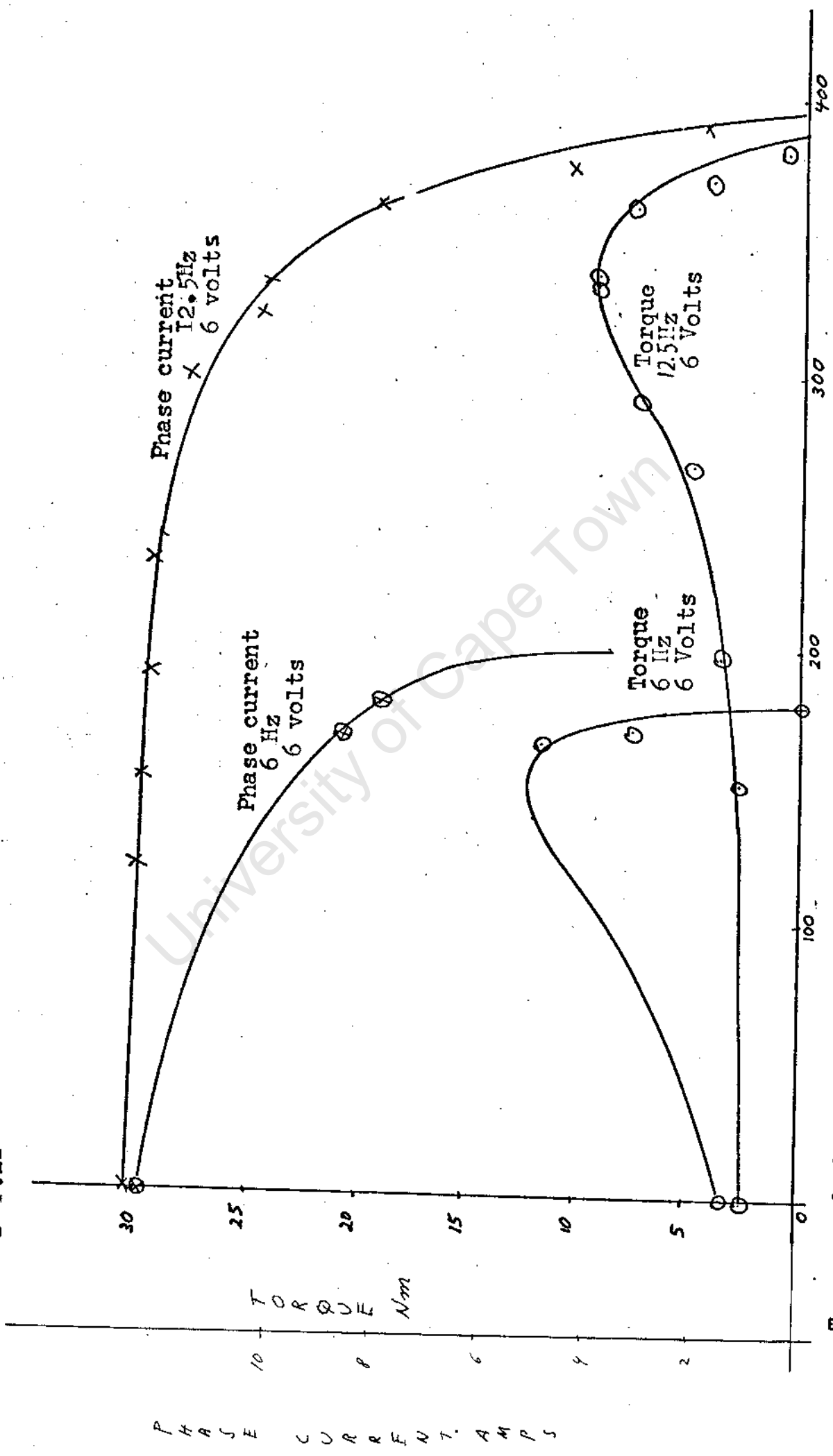
Magnetizing curves of the 9 phase inverter. Battery voltage against  $I/9$  th of battery supply current.

FIG F.11



Torque, phase current, efficiency against speed for 10 volt and 18 volt at 25 and 50 Hz respectively

FIG F.12



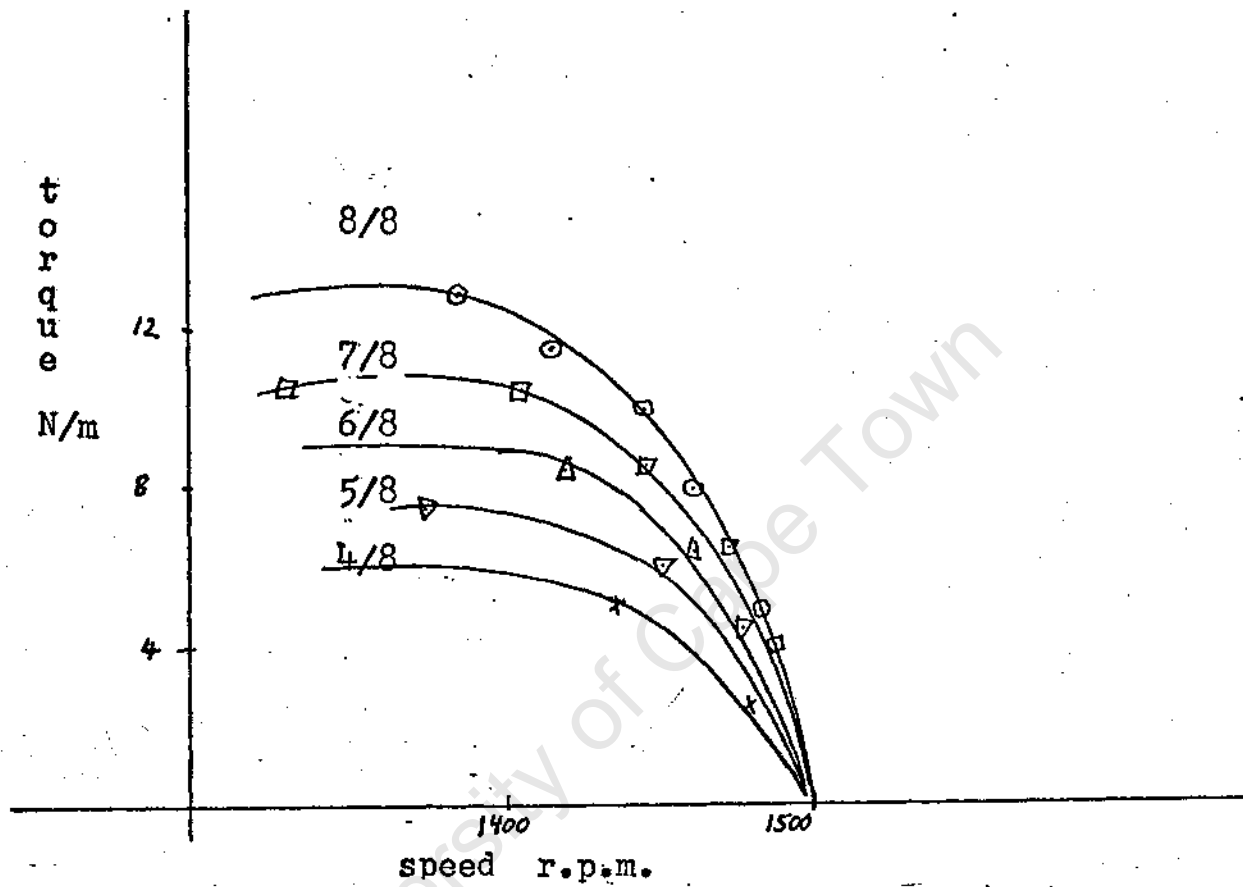
Torque and phase current against speed for 6 volt battery supply at 6 and 12.5 Hz

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PHASE CURRENT, AMPS

TORQUE Nm

Fig. F.13



Torque speed characteristic at 30 volt battery supply and 50 Hz inverter frequency for different mark to space ratios

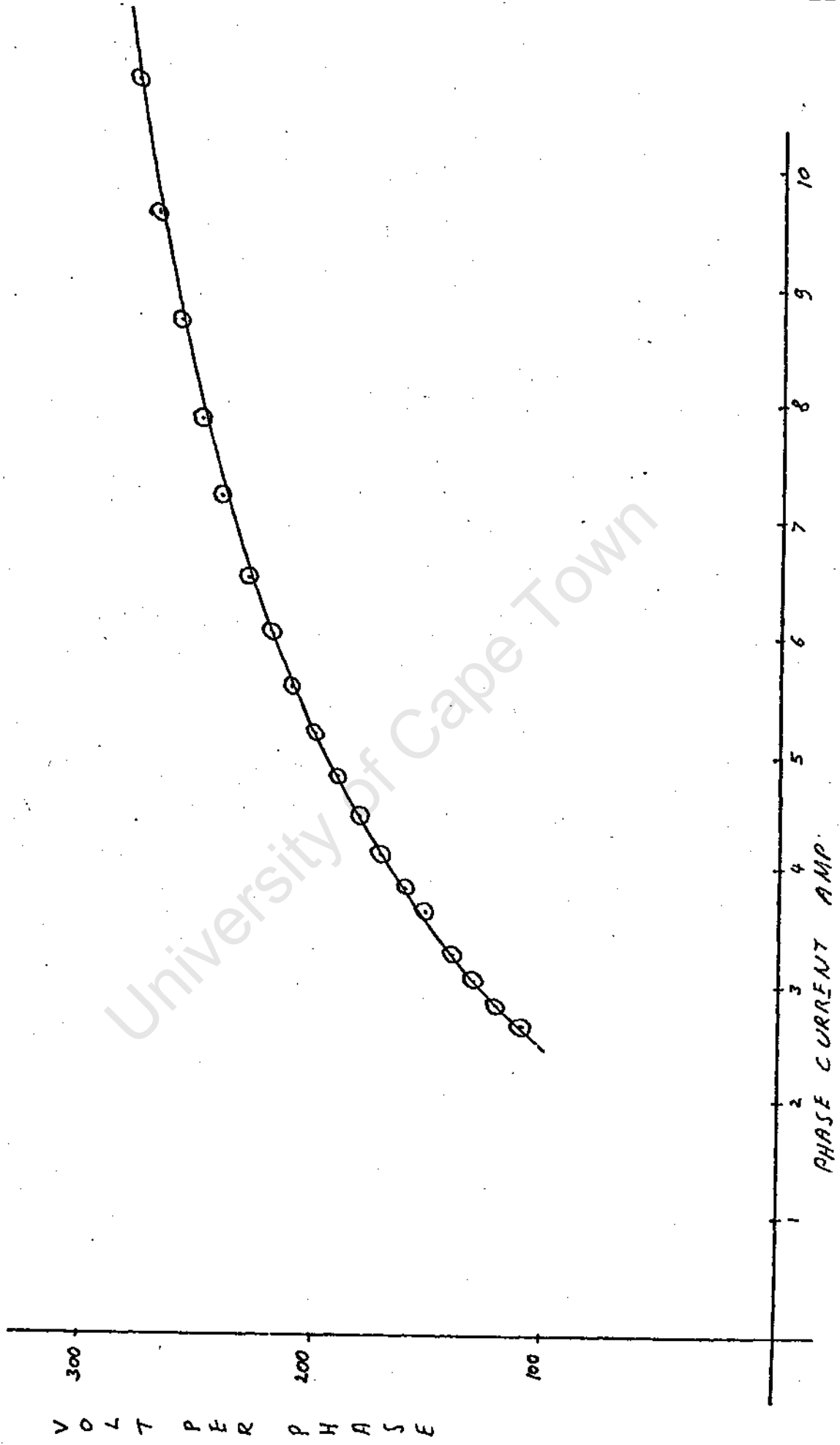
Magnetizing curves for 50 **HZ** are shown in Fig F.14  
 Torque speed characteristics at 50 H **and** 75 volts per phase is shown in Figure P.15 The reason for choosing 75 volts is that the average voltage corresponds to 30 volts for the 9 phase inverter fed induction motor.

$$v_{ph} = \frac{30 \times 8/9 \times 3}{1.11 \times .955} = 75 \text{ volts}$$

(e) Comparison of 9 Phase Inverter Fed Motor with 3 Phase Sinusoidally Fed

The comparison between the 9 phase interlaced inverter fed induction motor with the 3 phase connected sinusoidally fed induction motor was made at 50 Hz and at the same equivalent average voltage per conductor. The power output of each phase of the 9 phase inverter was measured and the total was taken as the input power to the induction motor. The shaft output torque and speed were recorded and the mechanical power output calculated. The test was made at 30 volts battery voltage and 50 **HZ** fundamental frequency of the inverter. The mechanical output power was plotted against input power of the motor when varying the load with a swinging type dynamometer. A similar test for 3 phase sinusoidally fed at 75 volt perphase and 50 **Hz**- was made, and compared on the same graph (see Fig F.16).

Fig F.14



Magnetizing curves for motor connected as 3 phase and sinusoidally fed

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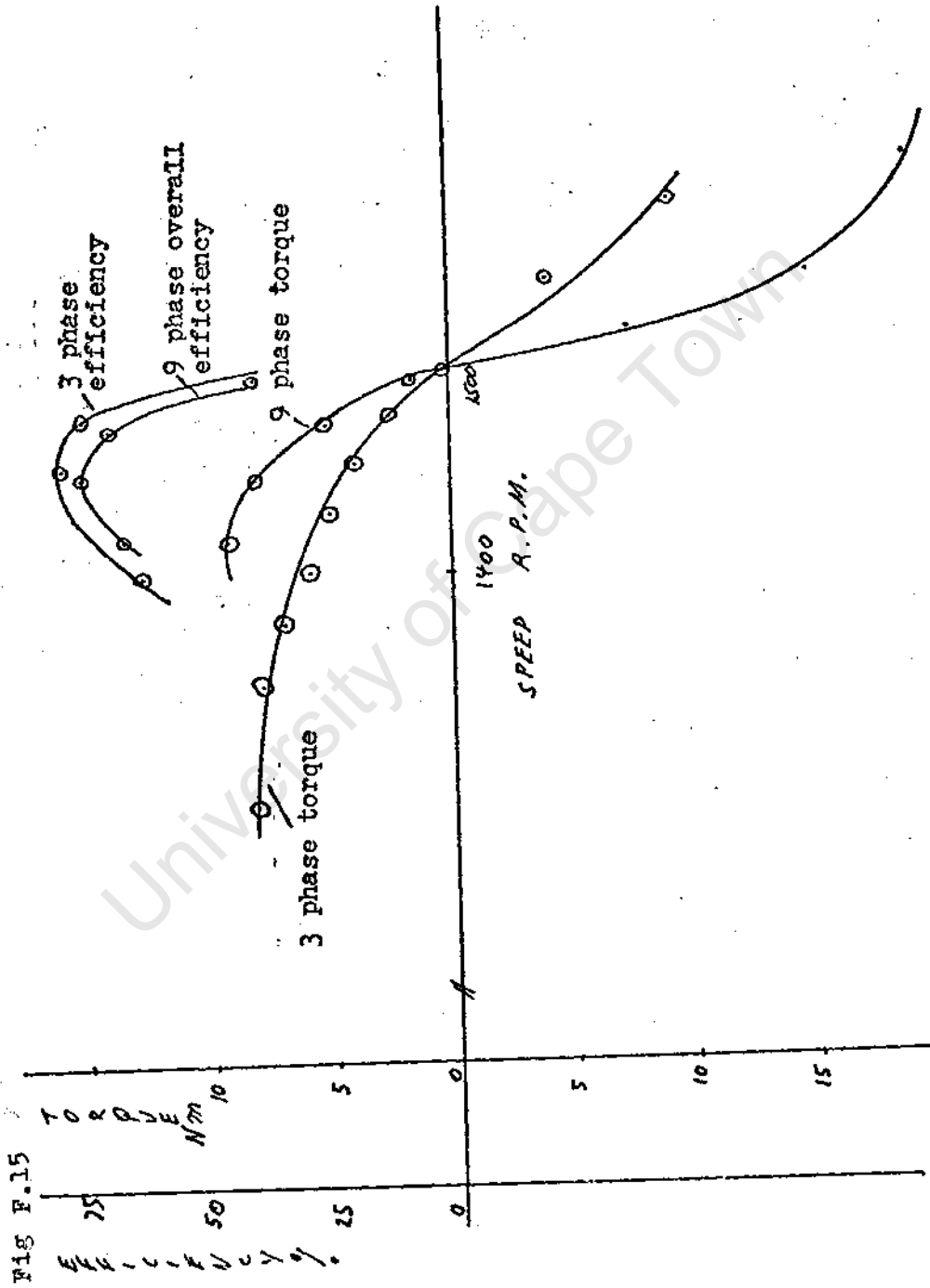
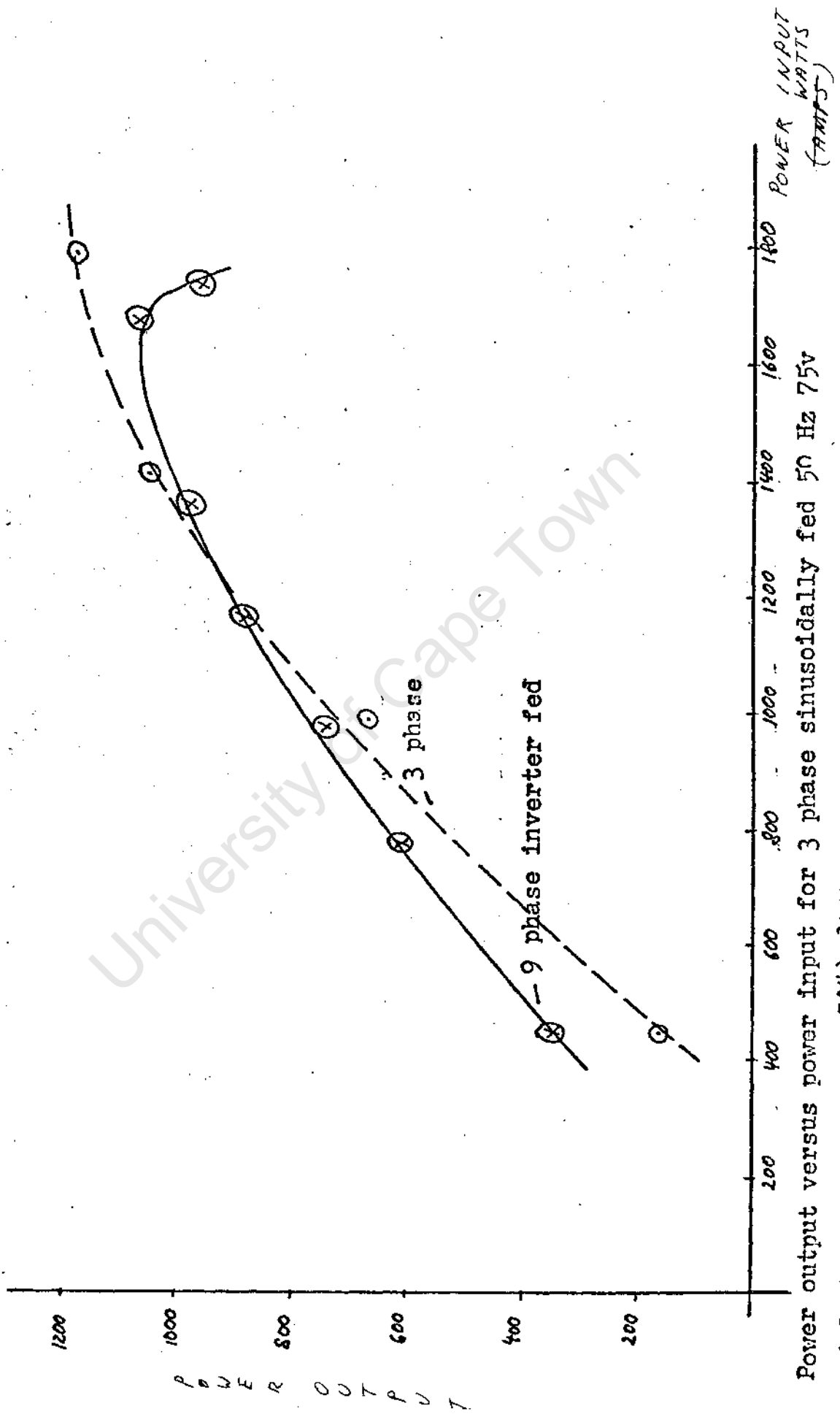


FIG F.15

Torque and efficiency versus speed for 3 phase sinusoidally fed 9 phase invert fed induction motor at 50 Hz and 75 and 30 volt respectively.

Fig F.17



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The comparison shows that the 3 phase sinusoidal motor is more efficient for output over 980 watts and less for output below. The comparison is difficult to evaluate as the 9 phase inverter fed motor has a complete different flux distribution than the sinusoidally fed motor. It is obvious that the less fluxed machine would suffer the highest slip and therefore rotor losses. Nevertheless Fig F.16 illustrates that the efficiency of a 9 phase inverter fed motor could be as good as that of a sinusoidally fed 3 phase induction motor.

The success of the Above described motor lead to the design of a motor with higher torque and power performances, for the possible application of a direct to wheel drive for a battery vehicle.

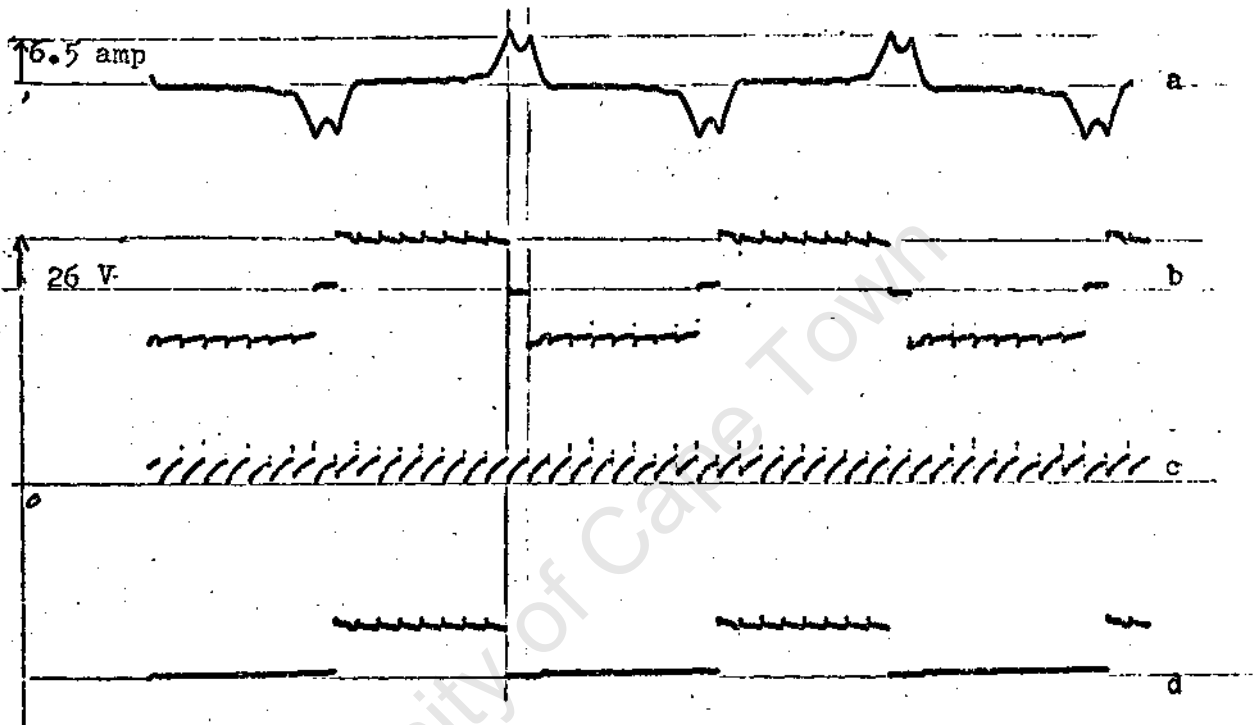
#### (f) Oscillograms

*(Oscillograms of phase current, phase voltage and supply*

current for the 9 phase interlaced inverter are shown in Figure F.17,F.13,F.19,F.20 and F.21 for no load, low, medium and high load at full mark space and a light load at 4/8 M/S ratio.

Fig F.17

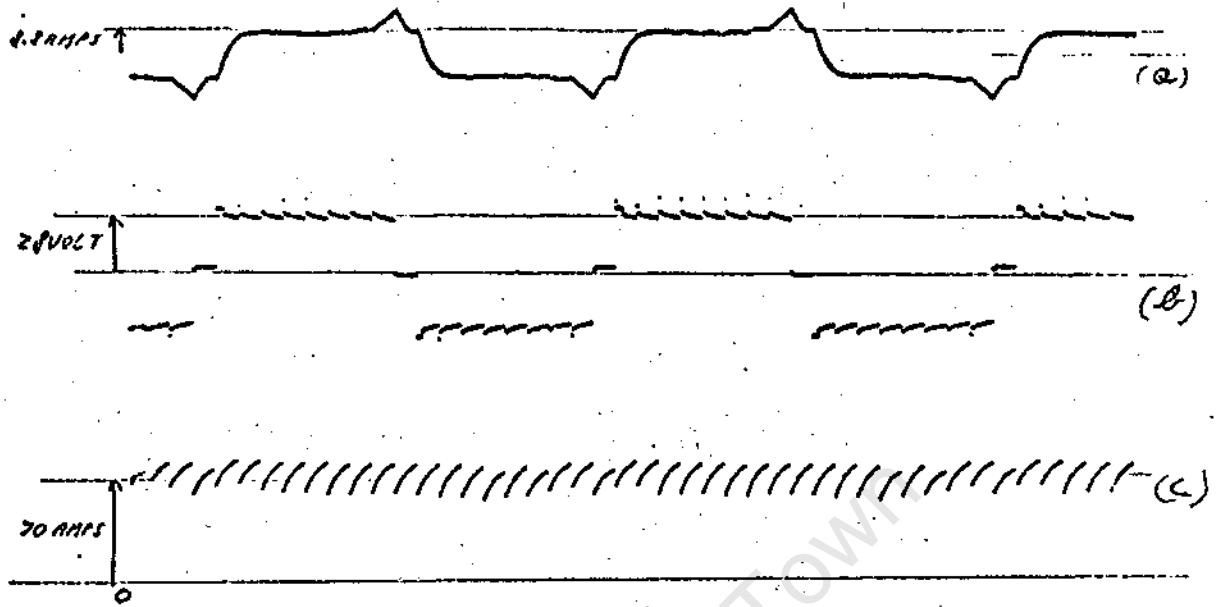
Oscillogram at no load



- a) Oscillogram of phase current on no load
- b) phase voltage at full mark space ratio
- c) supply current
- d) transistor Vce voltage

Fig F.18

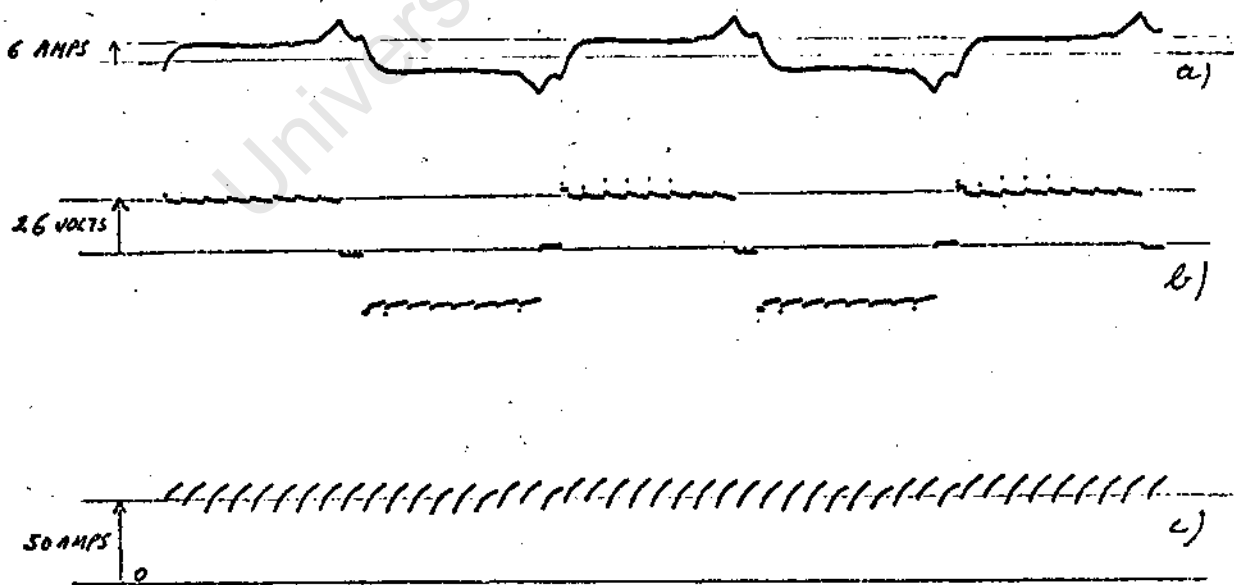
119



Oscillogram for medium load Torque: 10Nm, speed 1400 r.p.m.  
Output : 1.52 Kw, overall efficiency 71%, motor alone 76%

- a) phase current
- b) phase voltage
- c) supply current

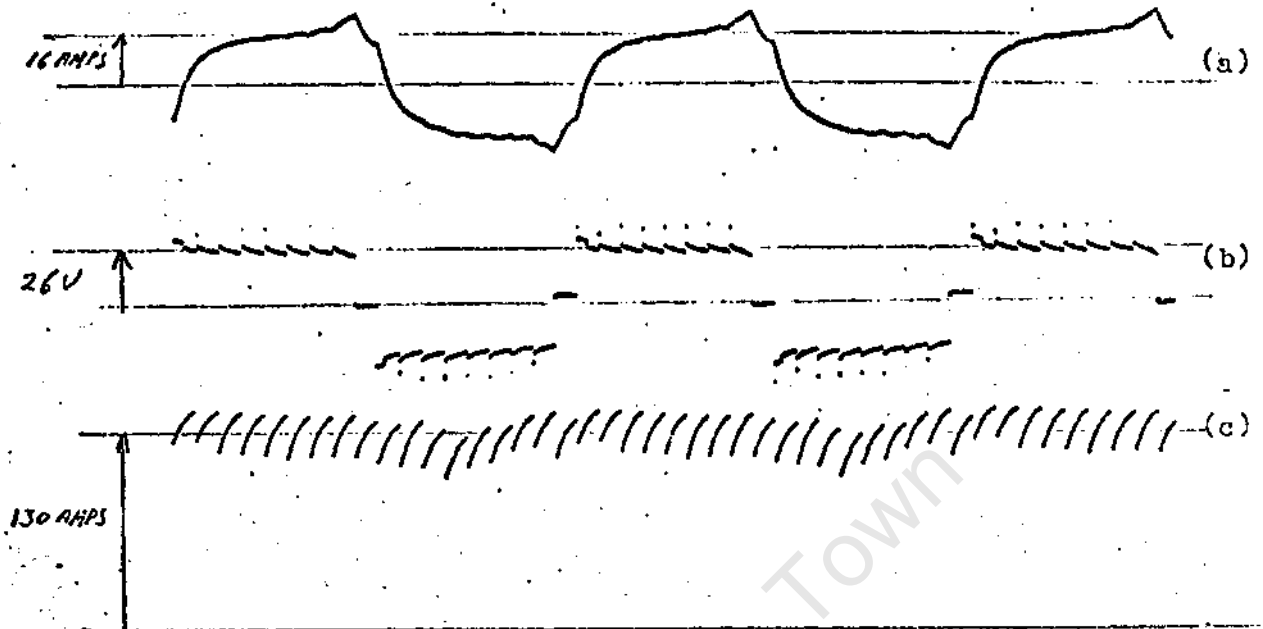
Fig F.19



Oscillogram for  
a) Phase current  
b) phase voltage  
c) supply current

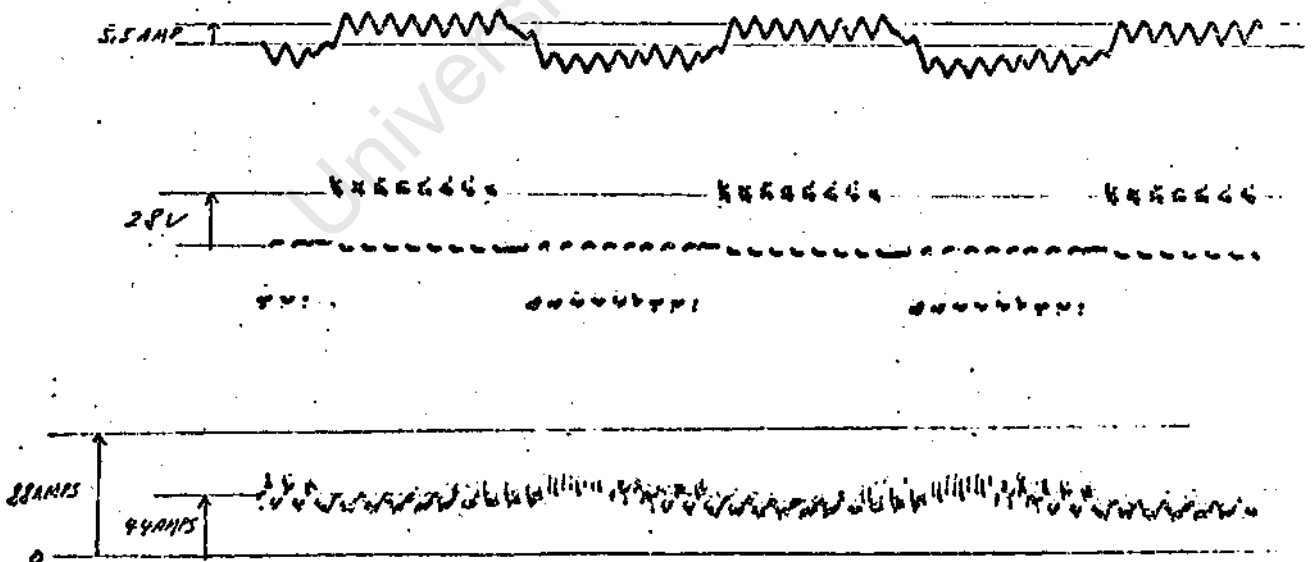
Fig F.20

I20



Oscillogram for heavy load Torque: 16Nm, speed 1330 r.p.m.  
Output : 2.25 Kw, overall efficiency 57%, motor alone 67%  
a) phase current  
b) phase voltage  
c) supply current

Fig F.21



Oscillogram for small load when chopping at 4/8 M/S  
a) phase current  
b) phase voltage  
c) supply current

## APPENDIX G

### Torque Requirement for a Battery Car

As considerations in establishing the acceptable performance for an electric vehicle is complex and relative to diverse requirements, the torque required for a suitable small passenger electrical car was based on an analytical model developed by the Australian Bureau of Transport Economics in 1974. The performances are those shown in figure G.; the aerodynamic drag coefficient and rolling resistance coefficient are those shown in figure G.2. The computed drive force, air drag and total drag for a 3m car of 600kg total running weight which provide the performances of figure 7.1 are shown in figure G.3. The maximum stalling torque of 1560N is required.

Choosing a wheel diameter of 32cm, the torque requirement is

$$\frac{1560 \times 0.16}{2} = 125 \text{Nm per motor.}$$

Fig G.1 Air Drag and Rolling Resistance coefficients.

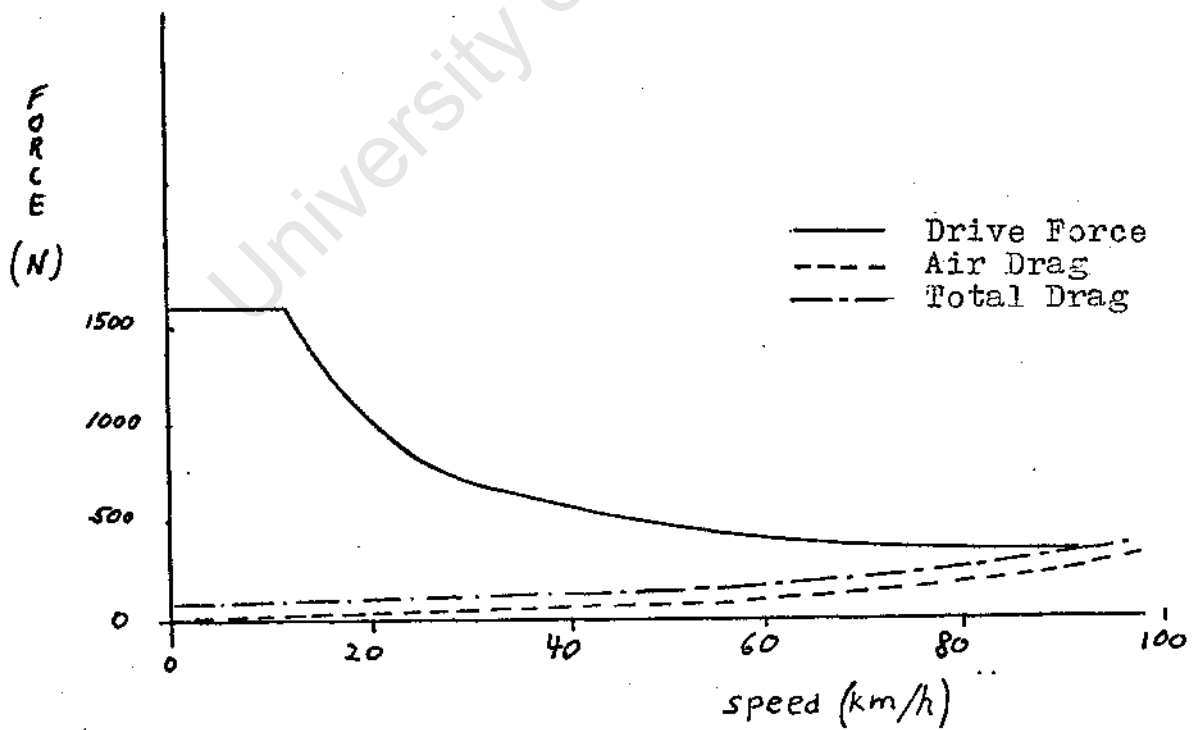
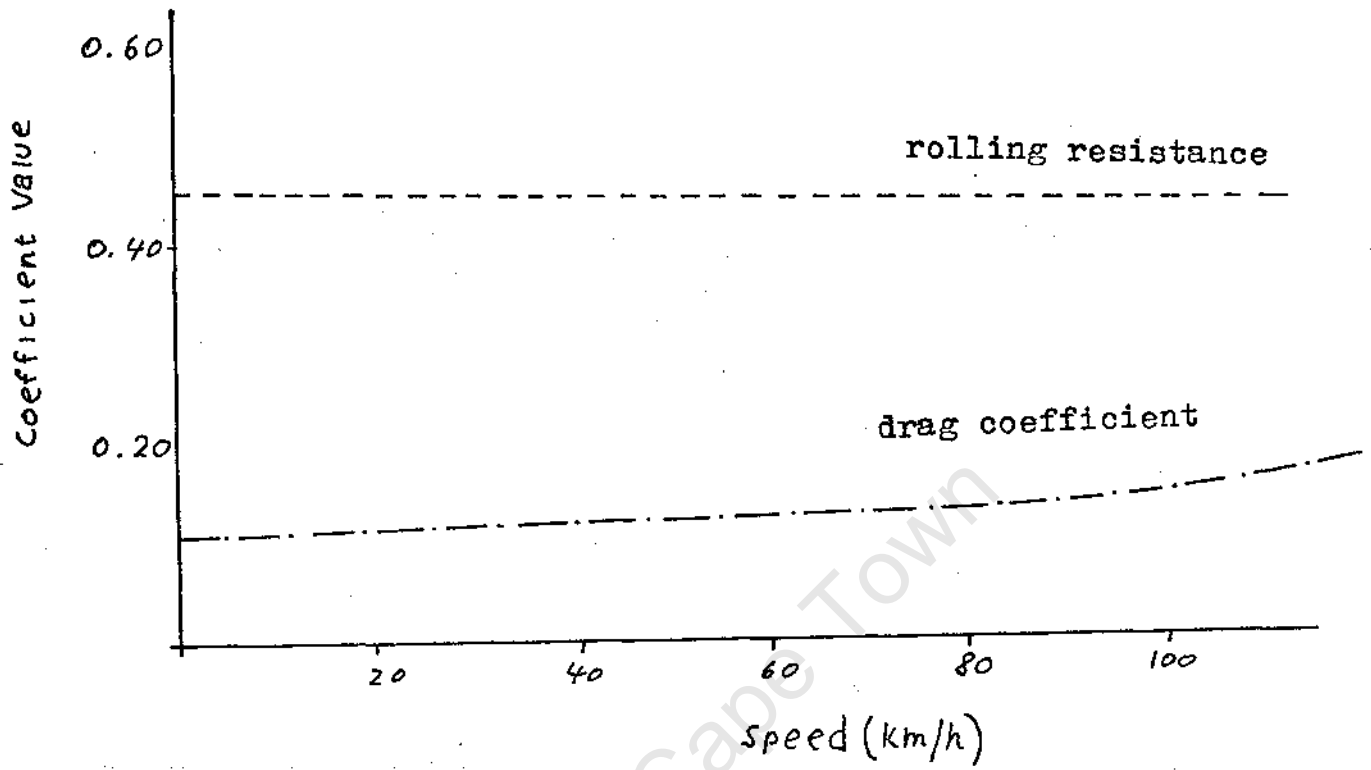


Fig G.2 Force variation 3m car, 600kg.

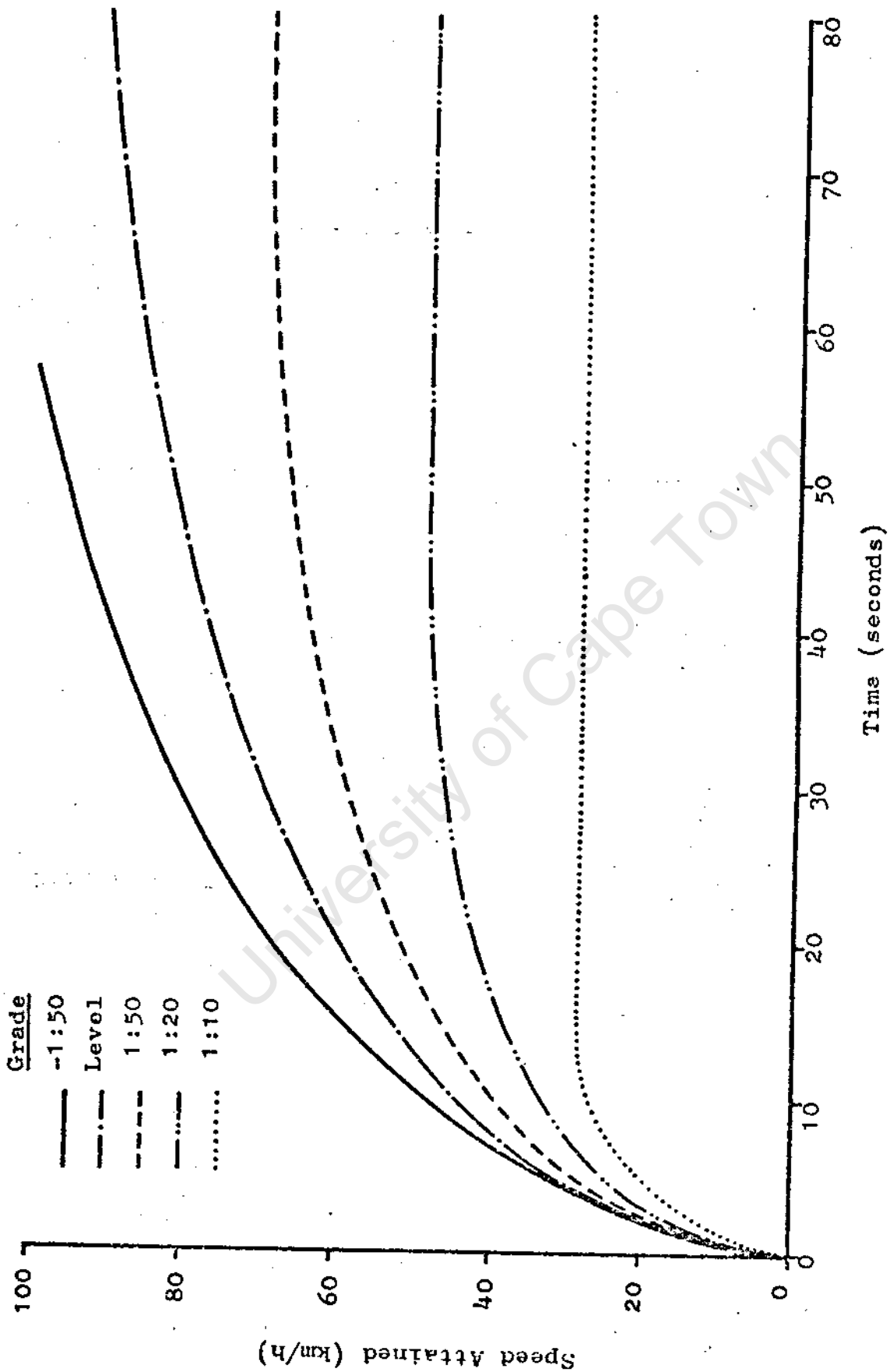


FIGURE G.3 - ACCELERATION CAPABILITIES, 3-METRE CAR

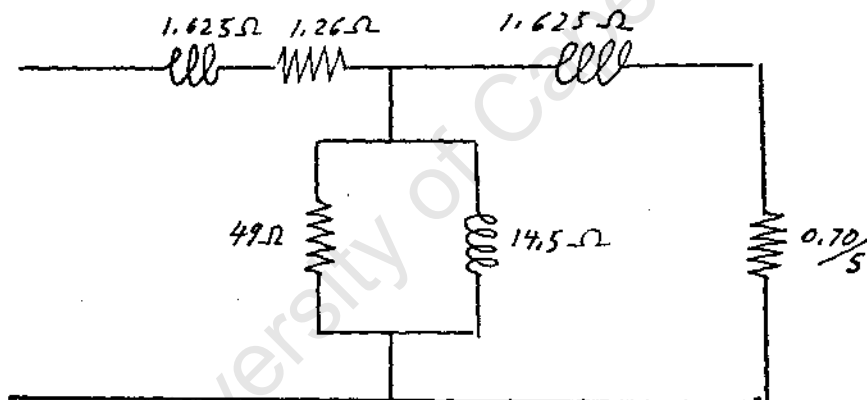
## APPENDIX H

### Characteristics and equivalent circuit of the 3 phase connected motor.

Figures H.1, H.2, H.3, give magnetizing, no-load, and short circuit tests for 50Hz. Assuming the same flux density at 300 volts 50Hz as 75 volts 12.5Hz, the magnetizing and friction losses are 370 WATTS at 50Hz. Assuming these losses to be proportional to frequency, then the constant losses at 12.5Hz would be 97.6 WATTS

The equivalent circuit for 12.5Hz is derived from the above and is given in figure H.4.

Figure H.4



Equivalent Circuit For 3 Phase Motor At 12.5Hz.

The maximum efficiency at 12.5Hz is calculated assuming constant losses equal to copper losses. The maximum efficiency is found to be 75.1% when delivering 553 WATTS.

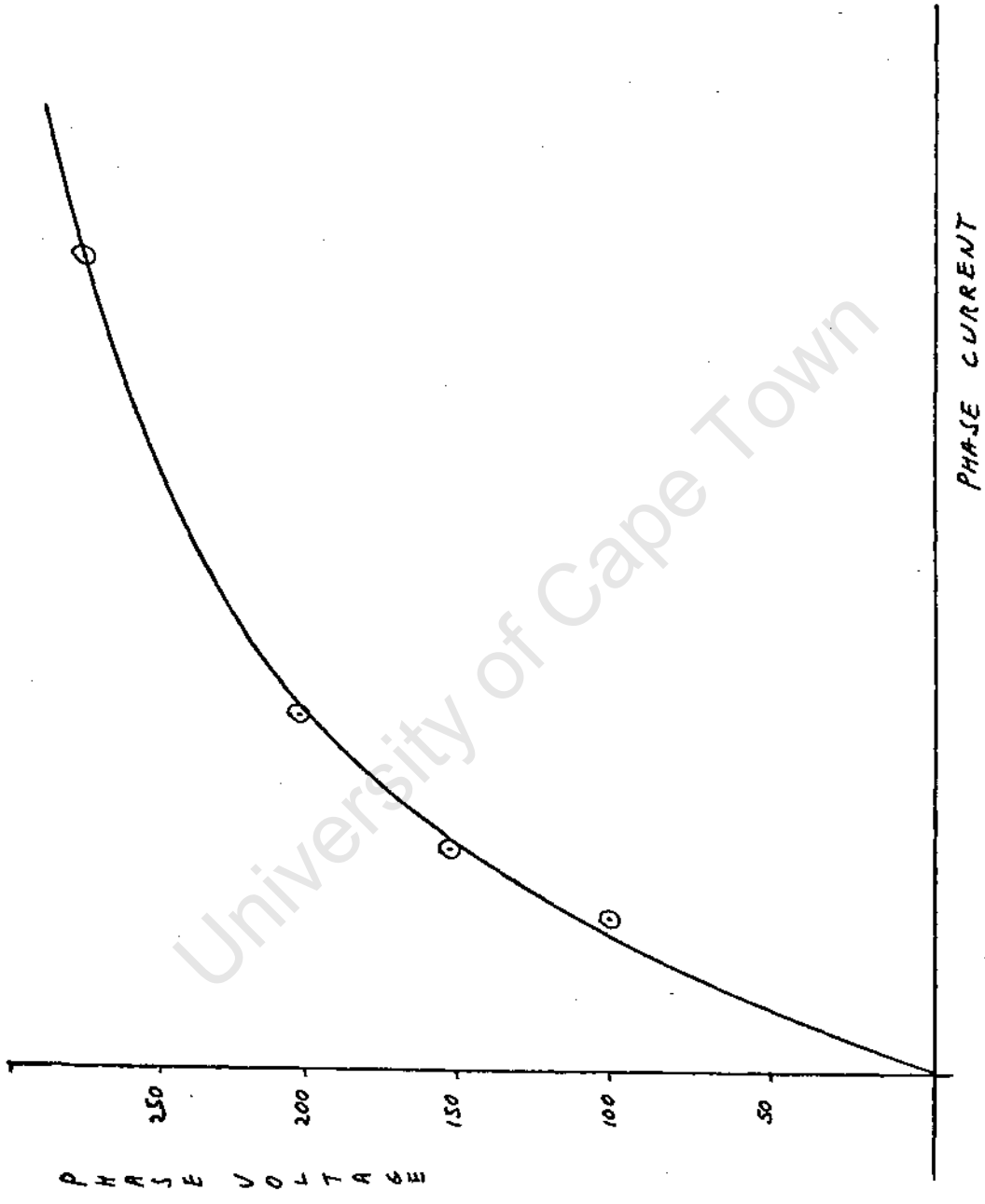
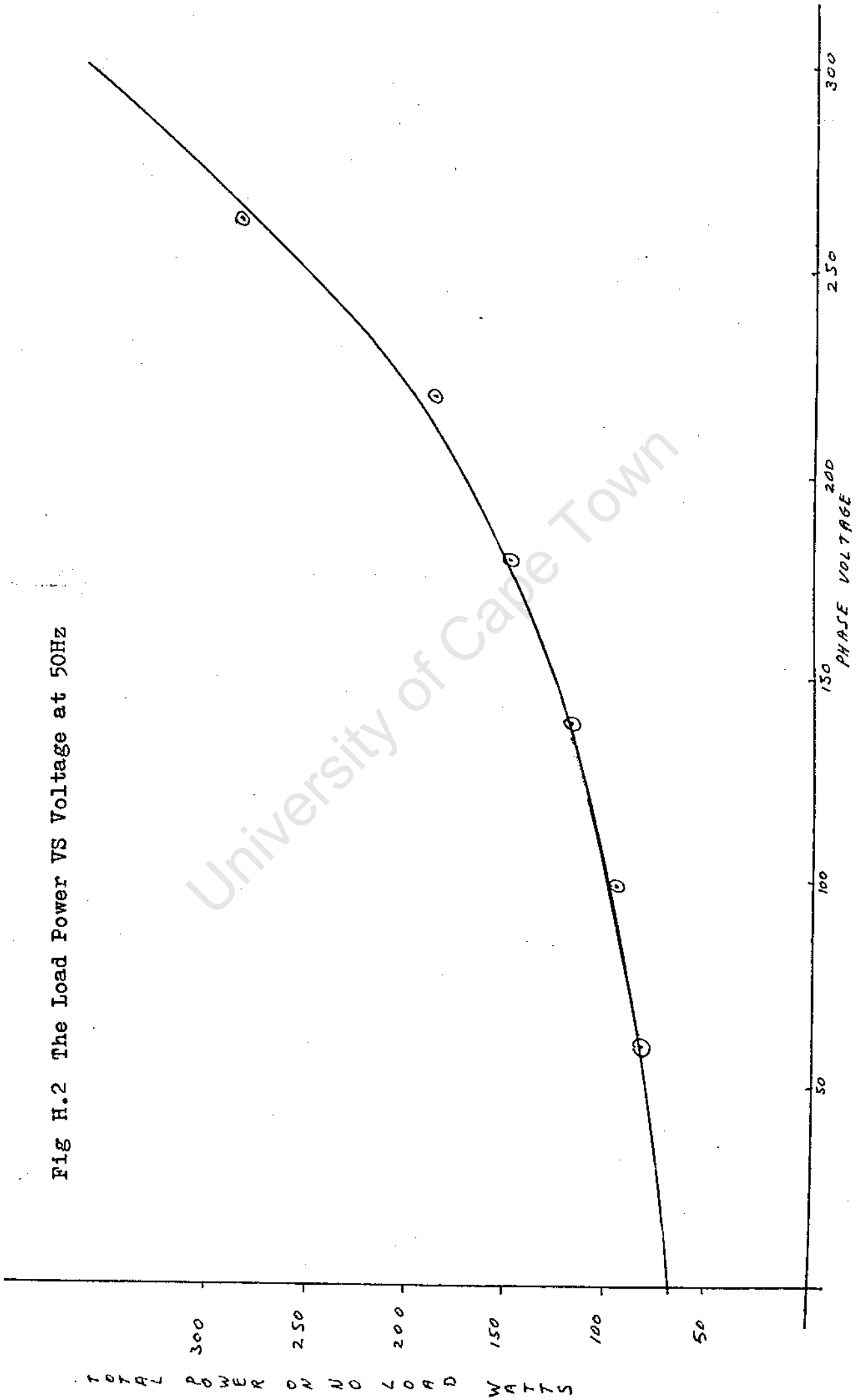


Fig H.1 Magnetizing Curve for 3 Phase Connected motor at 50Hz

15

Fig H.2 The Load Power VS Voltage at 50Hz



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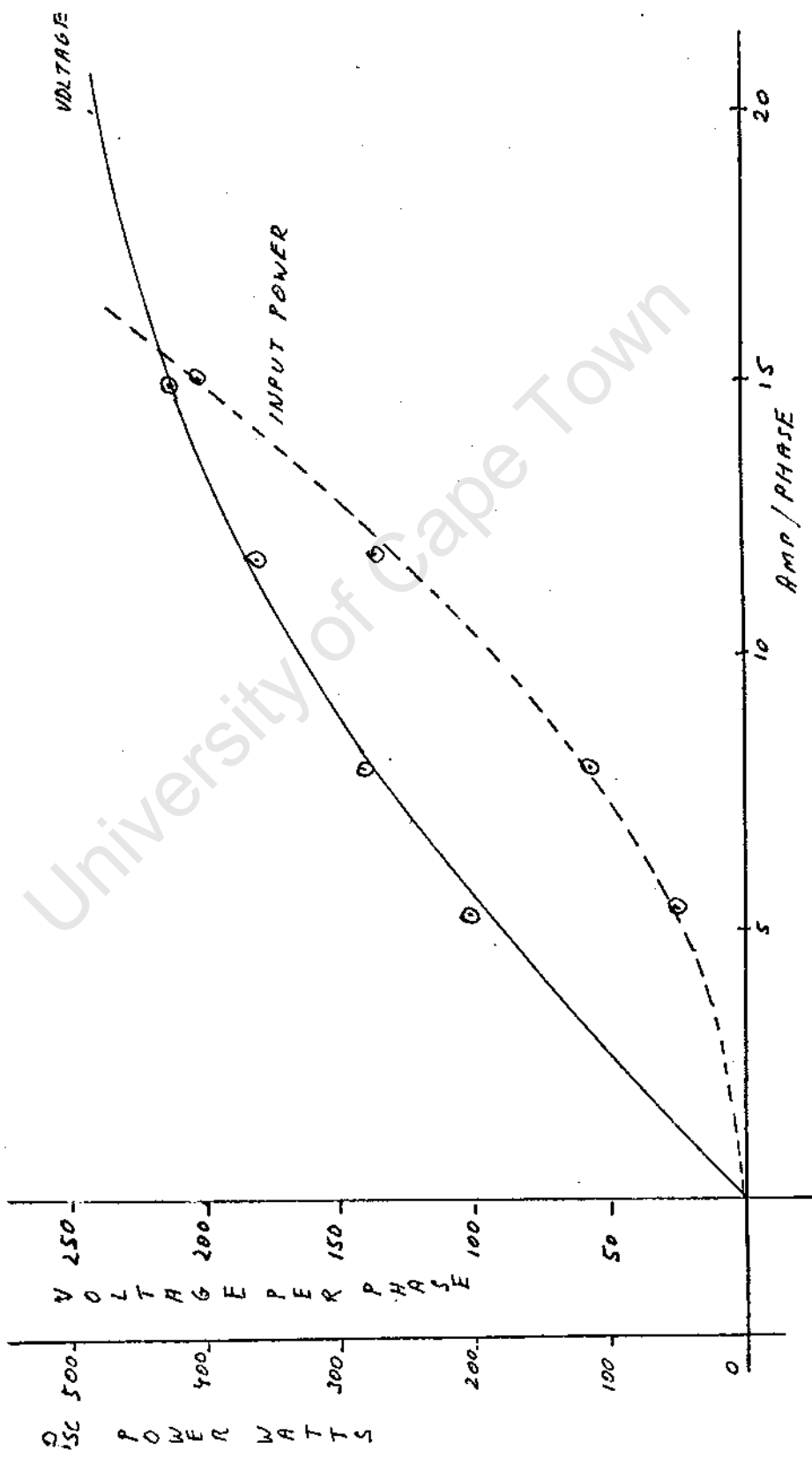


Fig H.3 Short Circuit Tests . Voltage VS Current and Input Power VS Current

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