THE MISSING BUCKET SYSTEM

a fast switch and modulator to be applied to the CERN Intersecting Storage Rings

by

A. M. Farson

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Summary

An electronic system is described, the object of which is to suppress an integral number (normally 10) of the 30 cycles of RF accelerating signal which correspond to one turn of a proton beam around the ISR.

1. Introduction

The circumference of the CERN Intersecting Storage Rings (ISR) is 1½ times that of the existing proton synchrotron (PS). Thus a proton beam ejected from the CPS into the ISR after one turn in the former, fills only two-thirds of the ISR circumference.

The r.f. accelerating field of the PS bunches the protons : the bunched beam is transferred to the ISR , picked up by an r.f. field synchronized to the bunches from the PS and accelerated into an orbit near the outside wall of the ISR vacuum chamber, where it is parked by switching off the r.f. Successive beams ("pulses") from the PS are likewise accelerated and parked in order to build up the intensity of the circulating beam. This process is called "stacking".

The r.f. accelerating voltage creates regions of stable field, referred to as "buckets", in which the bunches of protons are considered to be trapped or enclosed. Each bucket corresponds to one complete cycle of the r.f signal.

The r.f. harmonic numbers of the PS and ISR are 20 and 30, respectively; this means that if the r.f. accelerating voltage in the ISR is uninterrupted, only 20 of the 30 buckets generated in the ISR will be filled. During each cycle of stacking, the empty buckets entering the previously stacked beam cause additional perturbation and scattering of the particles already there, without adding new ones, thus diluting the beam intensity. Viewed another way, if a number of cycles of r.f. field are applied to the circulating stored beam without the addition of new particles, the beam will be scattered and thinned out. Thus the number of protons which can

be stored in one revolution in the ISR is reduced by a factor equal to the ratio of empty buckets to harmonic number. For example, if there are 10 empty buckets, then the beam intensity is reduced by one-third. These considerations apply only in the latter part of the accelerating cycle, when the buckets (and the bunches undergoing stacking) approach the previously stored beam. Here the r.f. voltage is low.

To eliminate this loss, the empty buckets must be suppressed. This is accomplished by switching off the r.f. accelerating voltage once every turn during the time when none of the newly injected proton bunches traverse the accelerating gap. Hence the designation "missing-bucket system". For a harmonic number of 30 and n bunches circulating in the ISR, the system must generate a keyed sinusoidal r.f. signal consisting of a burst of n complete cycles followed by (30-n) r.f. periods of zero voltage.

This report will describe a missing-bucket system capable of operating in two modes :

1) n cycles on followed by (30-n) cycles off, as described above.
2) n cycles at full amplitude followed by (30-n) cycles at an amplitude decaying exponentially from full to zero over a period of about 1 second. This mode will be used in experiments with imperfectly suppressed empty buckets.

2. Design criteria

2.1. Maximum voltage level at which system must operate

Towards the end of the stacking cycle, the r.f. voltage is at a low value which corresponds to buckets fitting closely around the proton bunches. It is at this voltage level [1] ideally about 13V peak (per cavity), that the missing-bucket system must be capable of producing a clean keyed sinewave at the accelerating gap.

In practice, the minimum r.f. voltage level is always higher, as beam dispersion increases the bunch area. For this and other reasons a system capable of operating at up to 250V peak would be most interesting.[2] The design target of 75V set here is a compromise between the above considerations and the limit imposed by the existing r.f. power amplifiers and cavities.

2.2. The r.f. power system from the missing bucket viewpoint

The basic parameters here are :

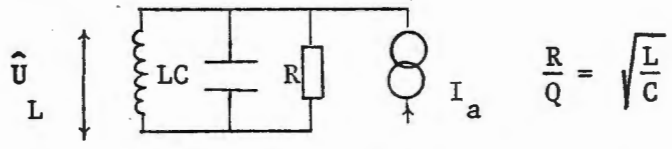
1. The electromagnetic energy W_o stored in the cavity
2. The peak anode current $\hat{I}_a$ of the tube
3. The characteristic impedance R/Q of the cavity.

The stored energy W_o can conveniently be expressed in terms of $\frac{R}{Q}$.

$$\frac{R}{Q} = \frac{\hat{U}_L^2}{2\omega W_o} \tag{2.1}$$

where $\hat{U}_L$ = peak r.f. voltage at cavity gap.

The cavity with the P.A. tube, may be represented thus :



If a current step $\hat{I}_a = \frac{\hat{U}_L Q}{R}$ is applied to the cavity in (2.2) which an amount of energy

$$W_o = \frac{\hat{U}_L^2 Q}{2\omega R} \tag{2.3}$$

is stored,

it can be shown that this energy will be removed in ¼ cycle. All these considerations apply in reverse, of course, at switch-on when energy must be transferred to the cavity.

At any instant while the current $\hat{I}_a$ is on, the instantaneous power flow from cavity to current sink (PA tube) is given by

$$p = \hat{U}_L \hat{I}_a \cos \omega t \sin \omega t \tag{2.4}$$

where $\hat{I}_a$ = peak P.A. anode current.

Average power over ¼ cycle $= \bar{P} = \frac{2}{\pi} \int_0^{\pi/2} \hat{U}_L \hat{I}_a \cos \omega t \sin \omega t \, d(\omega t)$ (2.5)

$$= \frac{2\hat{U}_L \hat{I}_a}{\pi} \left[\sin^2 \omega t \right]_0^{\pi/2} = \frac{\hat{U}_L \hat{I}_a}{\pi} \quad (2.6)$$

Energy removed from cavity in ¼ cycle $= W_a = \bar{P}.t$

where $t = \frac{1}{4f} = \frac{\pi}{2\omega}$

i.e. $W_a = \frac{\hat{U}_L \hat{I}_a}{2\omega} = \frac{\hat{I}_a^2 R}{2\omega Q}$ from 2.2 ... (2.7)

Also : initial stored energy W_o in cavity $= \frac{\hat{U}_L^2 Q}{2\omega R}$

$$= \frac{\hat{I}_a^2 R}{2\omega Q} = W_a \text{ from 2.2} \quad \ldots (2.8)$$

For the specific example of our cavity

$$f = 9.5 \text{ MHz.} \qquad \hat{I}_a = 1.6\text{A} \qquad \frac{R}{Q} = 16\Omega$$

These parameters are imposed by the existing r.f. system.
Thus for removal of all stored energy from cavity in ¼ period,

$$\hat{U}_L = \frac{I_a R}{Q} \quad \text{from 2.2}$$

$$= 1.6 \times 16 = 25.6\text{V/cavity} \simeq 150\text{V/turn}$$

For $\hat{U}_L > 25{,}6$V, the stored energy would have to be removed in several successive quarter-periods, $\hat{I}_a$ being fixed. (The same applies to the build-up of energy in the cavity after switch-on).

In general, for $\hat{U}_L = \frac{k \hat{I}_a R}{Q}$ (2.9)

$$W_o = \frac{\hat{U}_L^2 Q}{2\omega R} \qquad (2.3)$$

$$= \frac{k^2 I_a^2 R^2}{Q^2} \cdot \frac{Q}{2\omega R} \quad \text{from 2.9}$$

$$= \frac{k^2 \hat{I}_a^2 R}{2\omega Q} \qquad (2.10)$$

Energy removed per ¼ period $W_a = \frac{\hat{I}_a^2 R}{2\omega Q}$ (2. 8)

$$\therefore W_o = k^2 W_a \qquad (2.11)$$

i.e. $\hat{I}_a$ must flow for k^2 successive quarter-cycles to reduce the energy stored in the cavity to zero. For the specific case of $\hat{U}_L$ = 75V/cavity

$$k = \frac{75}{25,6} \approx 3$$

$\therefore$ $k^2 = 9$, i.e. the P.A. tube must conduct for 9 quarter-cycles at $\hat{I}_a$ = 1,6A to "empty" the cavity of stored energy - the phase relationship being such that the tube removes energy from the cavity.

If the amount of energy transferred from the cavity to the P.A. tube per quarter-cycle is constant, the peak r.f. voltage any <u>odd</u>* number N of quarter-cycles after switch-off is given by

$$|\hat{U}_{L(n)}| = |\hat{U}_L|(1 - \frac{N}{k})^{\frac{1}{2}} \qquad \ldots(2.12)$$

assuming switching at the voltage zero crossing. The instantaneous value

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* or any even number of quarter-cycles after switch-off if switching takes place at a voltage peak. Then $U_L = \hat{U}_L(1 - \frac{N}{k^2})^{\frac{1}{2}} \cos \omega t$.

U_L is given by $U_L = \hat{U}_L(1 - \frac{N}{k^2})^{\frac{1}{2}} \sin \omega t$ (2.12A).

The fact that the r.f. voltage takes several quarter-cycles to decay for $\hat{U}_L$ > 25V means that a number of empty buckets will be formed at the beginning of the train of missing buckets.

It is felt that if the peak amplitude of the r.f. cycle corresponding to one of these buckets is nearly equal to the peak steady state voltage, then this bucket could perhaps be filled with particles by timing it to coincide with a bunch from the PS, without serious perturbation of the stacked beam. This would have to be checked by computation and experiment.

On the other hand,it is believed that a bucket corresponding to an r.f. cycle having 25% (or less) of the peak amplitude can be disregarded as it will not dilute the beam significantly.

Buckets falling between these two limits could, however, be troublesome. Too many of these in the empty-bucket train would obviously vitiate the entire purpose of this project. They cannot be filled without grave perturbation of the bunches involved, so their number and amplitude must be kept to a minimum. This obviously limits the maximum switchable gap voltage.

The following curves give a rough indication of the number of buckets generated during switch-off of the r.f. cycle for the range $\hat{U}_L$ = 25V ...100V, as well as the relative amplitude of these buckets.

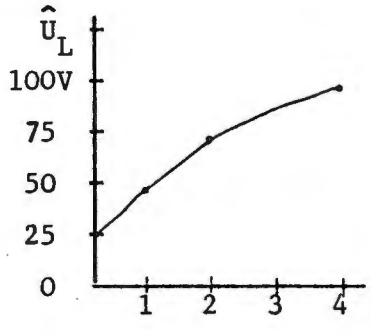

Fig. 2.1.

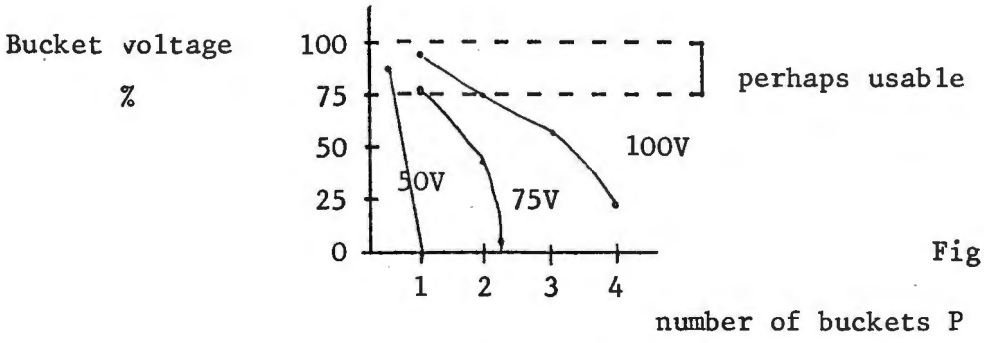

Fig.2.2

The total number of buckets of less than full amplitude generated during the missing-bucket cycle is given by 2P, as this process is repeated at switch-on. In fact, the number of empty buckets generated is doubled, as just as many residual buckets are established at switch-on as at switch-off.

The "fading-bucket" technique (progressive reduction of the amplitude of the empty buckets in accordance with a fixed law as the accelerated beam approaches the stack) may be a useful method of minimizing the effect of the useless buckets. (One residual bucket may be usable as the beam phase-lock reference.)

We will examine the behaviour of the existing cavity, with associated power amplifier and feedback circuits, and show that its response to fast switch-off of the r.f. drive is a fair approximation to (2.12) above.

3. The ISR Cavity and P.A.

3.1. The System

A block diagram of the r.f. cavity system is given in Fig. 3.1 and an outline circuit diagram in Fig. 3.2. There are seven cavities in each ring, six active and one spare.

The cavity is a capacitively loaded coaxial resonator and is driven by a 10 kW water-cooled tetrode mounted very close to it. The maximum gap voltage obtainable is 3,3kV peak (per cavity).

The cavity has a loaded Q of 200. Its bandwidth is thus sufficient to allow about $\pm$ 1% frequency shift without retuning.

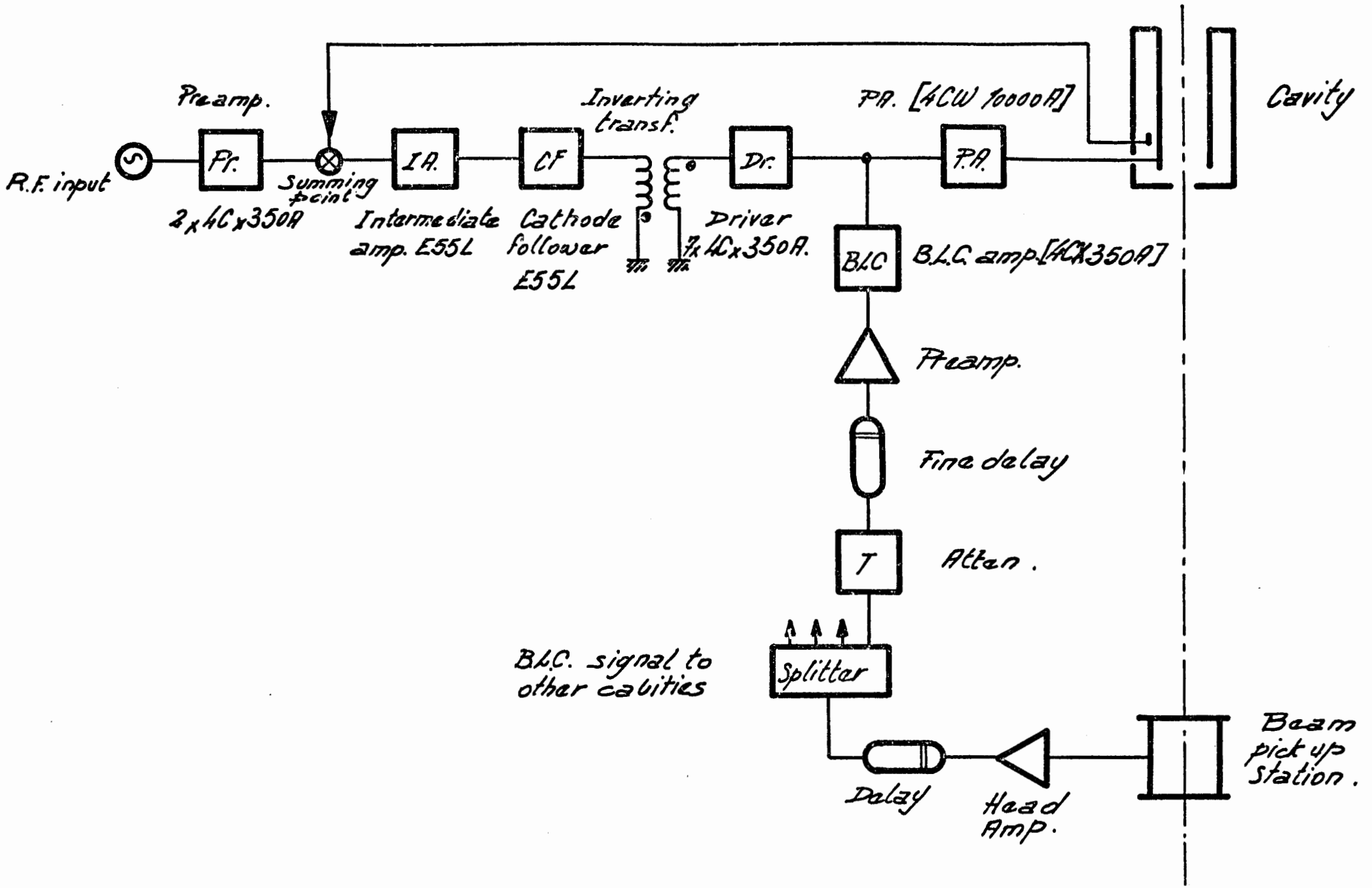

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Fig. 3.1 : Block diagram of RF cavity and amplifier chain, showing beam loading compensation (B.L.C.).

The stacking takes the r.f. voltage from 3300V peak to less than 100V peak; therefore the amplifier chain is operated in Class A to ensure linearity over a very large program voltage range. This means that the P.A. efficiency is low - of the order of 30%.

This is acceptable here if the total power input is not very large - less than 10 kW.

3.2. Beam loading

A serious problem for the r.f. power system is that of the voltage induced across the cavity gap by the beam. The peak r.f. component of the beam current at 9.5 MHz is 150 mA; it is desirable that the voltage induced in each cavity by this current be less than 1.5% of the minimum r.f. voltage, i.e. 1,5 V or less.

Beam loading is minimized in two ways: firstly, negative feedback reduces the source impedance of the cavity (as seen by the beam) to about 60Ω. Secondly, a beam-loading compensation signal derived from a wide-band induction pick-up electrode further down the ring is fed into the P.A. driver stage in the correct phase and amplitude relationship to cancel out the beam-induced voltage.

For a peak beam current of 150mA, the beam-induced voltage in 60Ω would be 9V : the beam-loading compensation circuit reduces this to 0,9 V which is acceptable. (See Fig. 3.1)

3.3. The Feedback Circuit

The feedback voltage is picked-up by a capacitive probe in proximity to the "hot" side of the cavity gap.

The current flowing out of this probe at full r.f. voltage is in the region of 400 mA; hence the two power tetrodes in the preamplifier.

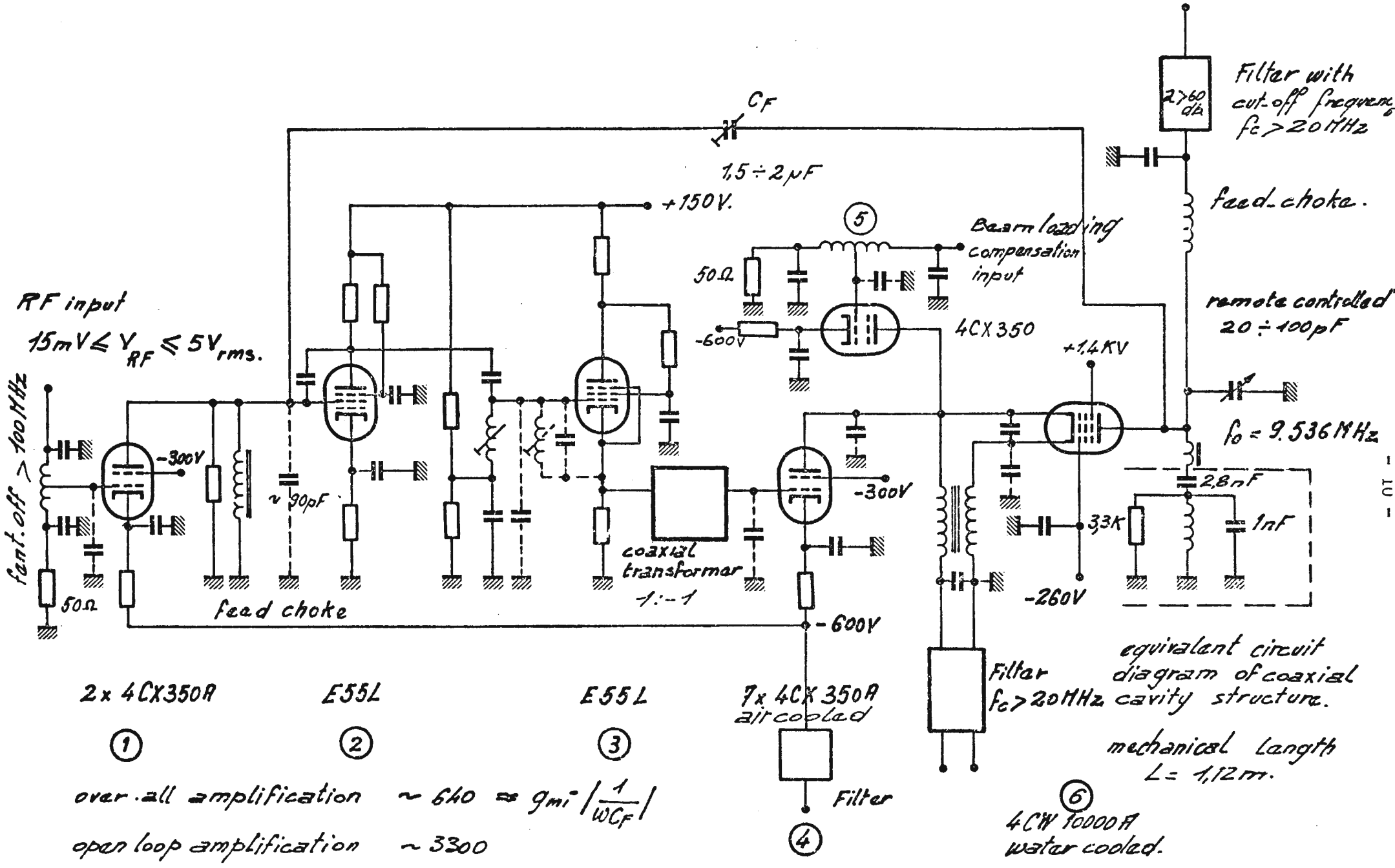

Fig. 3.2 : R.F. power amplifier including beam compensation.

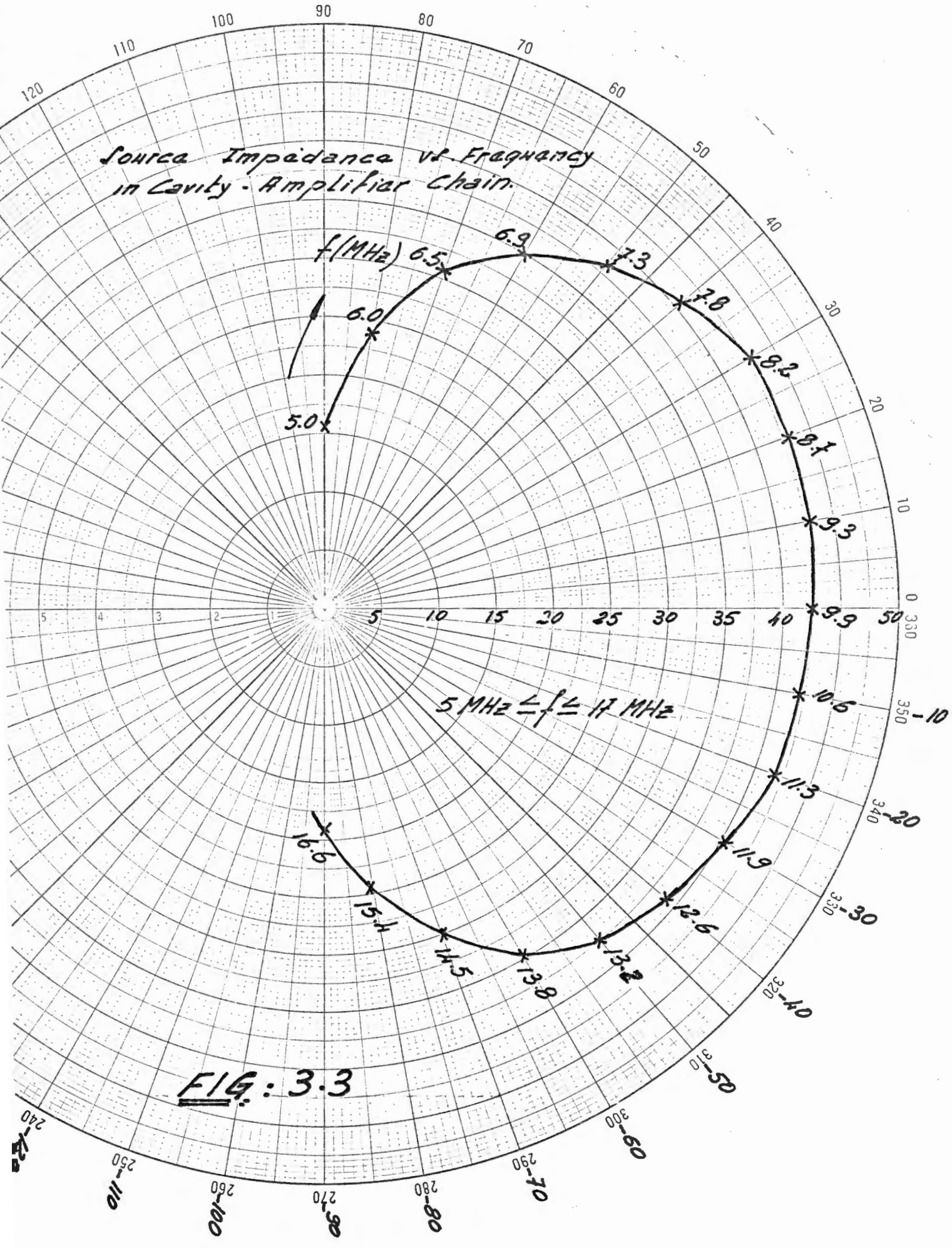
Source Impedance vs. Frequency
in Cavity - Amplifier Chain.
f(MHz) 6.5
6.9
7.3
7.8
8.2
8.1
9.3
9.9
10.6
11.3
11.9
12.6
13.2
13.8
14.5
15.4
16.6
6.0
5.0
5 MHz ≤ f ≤ 17 MHz

FIG: 3.3

During setting-up of the amplifier, the capacitive probe is adjusted such that the source impedance seen at the cavity gap is 60Ω resistive at 9.5 MHz.

A typical curve of impedance response is given in Fig. 3.3.

We are interested in what happens in the feedback amplifier when a sinusoidal input is switched off at an arbitrary point.

3.4. Response of Cavity and Amplifier to a keyed sine-wave

In the most general terms, the r.f. amplifier may be represented thus for transient response analysis:

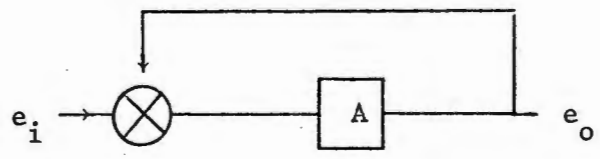

Fig. 3.4

A is of the form $A = A_e^{-j\beta\omega}$ where A = loop gain and β = forward group delay of amplifier. Assume that the feedfack path has zero group delay.

The system transfer function is given by

$$T(t) = \frac{e_o}{e_i} = \frac{A_e^{-j\beta\omega}}{1 - A_e^{-j\beta\omega}} \qquad \ldots\ldots 3.1$$

We apply to the system a sinusoidal input which is keyed off at the voltage peak.

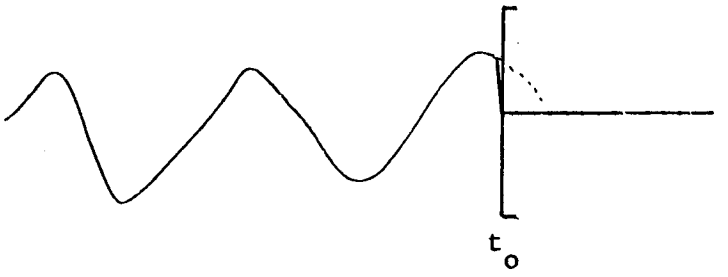

Fig. 3.5.

From Eq. 3.1,

$$T(s) = \frac{Ae^{-\beta s}}{1 - Ae^{-\beta s}} \quad \text{where } \beta > 0 \qquad \ldots 3.2$$

Input $I(t) = e_i \cos \omega t \quad 0 \leq t < t_o \qquad$ where $t_o = \frac{(2m-1)\pi}{\omega}$

$$t_o \leq t \leq \infty$$

$$I(s) = -e_i \frac{1}{s^2 + \omega^2} (1 - e^{-t_o s}) \qquad \ldots 3.3$$

Output $O(s) = T(s)\ I(s)$

$$= - e_i . A \left[\frac{1}{s^2 + \omega^2} \cdot \frac{(1 - e^{-t_o s}) e^{-\beta s}}{(1 - Ae^{-\beta s})} \right]$$

$$= -e_i . A . \left[\frac{1}{s^2 + \omega^2} \cdot \frac{1}{e^{\beta s} - A} \right] - e_i\ A . \left[\frac{1}{s^2 + \omega^2} \cdot \frac{-e^{t_o s}}{e^{\beta s} - A} \right] \qquad \ldots 3.4$$

From this, $O(t) = -e_i . A . \left[\bar{O}(t) - \bar{O}(t - t_o) \right] \qquad \ldots 3.5$

We define $\tilde{O}(s) = \frac{1}{s^2 + \omega^2} \cdot \frac{1}{e^{\beta s} - A}$

$$= \frac{s}{s^2 + \omega^2} \cdot \frac{1}{s(e^{\beta s} - A)} \qquad \ldots 3.6$$

Now $O(t) = 0$ for $0 \leq t < \beta$ ...3.7a

$$= -\frac{1 - A^n}{1 - A} \cos \omega t \text{ for } n\beta < t < (n+1)\beta \quad ...3.7b$$

For $t_o = \frac{2m\pi}{\omega}$, $\bar{O}(t) = \bar{O}(t-t_o)$ ie $O(t) = 0$

For $t_o = \frac{(2m-1)\pi}{\omega}$ $\bar{O}(t) = -\bar{O}(t - t_o)$

$$\text{i e } O(t) = 2\bar{O}(t) = -2A\, e_1 \frac{1 - A^n}{1 - A} \cos \omega t \quad ...3.8$$

The condition for validity is that $\beta > 0$ ...3.9

Initial conditions If we set $O(t) = 4Ae_i$ for $t = 0$

then, for $0 \leq t < \beta$ $O(t) = 4Ae_i \cos \omega t$ ...3.10

For $n\beta < t < (n+1)\beta$,

$$O(t) = 2A(1 - A - A^2 - \ldots - A^{n-1})\, e_i \cos \omega t \quad ...3.11$$

For $A \geq 1$ $O(t) \to -\infty$

For $A < 1$ $O(t) \to 0$.

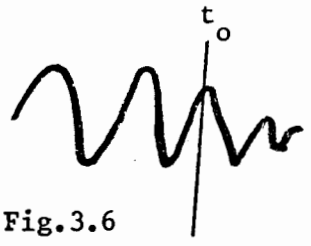

Fig.3.6

Initially $t = t_o$

$O(t) = 4Ae_i$

Here $|O(t)| = |U_L|$.

Thus, if the input is keyed off at time t_o such that the instantaneous value of output voltage is

$$O(t) = U_L = 4Ae_i \ ,$$

the output signal decays to zero at a rate determined by the system loop gain and forward group delay.

In practice the above analysis only approximately describes the system as the P.A. saturates at $\hat{I}_a = 1{,}6A$. The driver stage saturates just after the P.A. In addition, the concept of loop gain A used in the foregoing analysis refers to effective amplifier gain averaged over the group delay time.

The system loop gain is determined by the source impedance desired. By altering the point t_o with respect to the r.f. cycle, it is possible to optimize the shape of the decay envelope, as discussed in 2 above.

The following curves in Fig. 3.7 will serve to compare r.f. gap voltage U_L as a function of number of quarter-cycles after switch-off as derived from Eq. 2.12 (r.f. voltage for constant energy removal per ¼-cycle), Eq. 3.11 (approximate transient analysis) and from experimental results from tests on the system.

Consider the case for $\hat{U}_L = 75V$.
Here $k = \frac{75}{25.6} \approx 3$ for our system

$$N \doteq k^2 = 9$$

i.e. 9 quarter-cycles are required to remove all the stored energy from the cavity according to Eq. 2.11.

In our system $\beta \simeq 40$ ns. Let us take $\beta = \frac{\pi}{\omega}$ here .

i.e. $= \frac{1}{2}$ cycle. In Eq. 3.12, assume A = 0.9

We thus have the following picture.

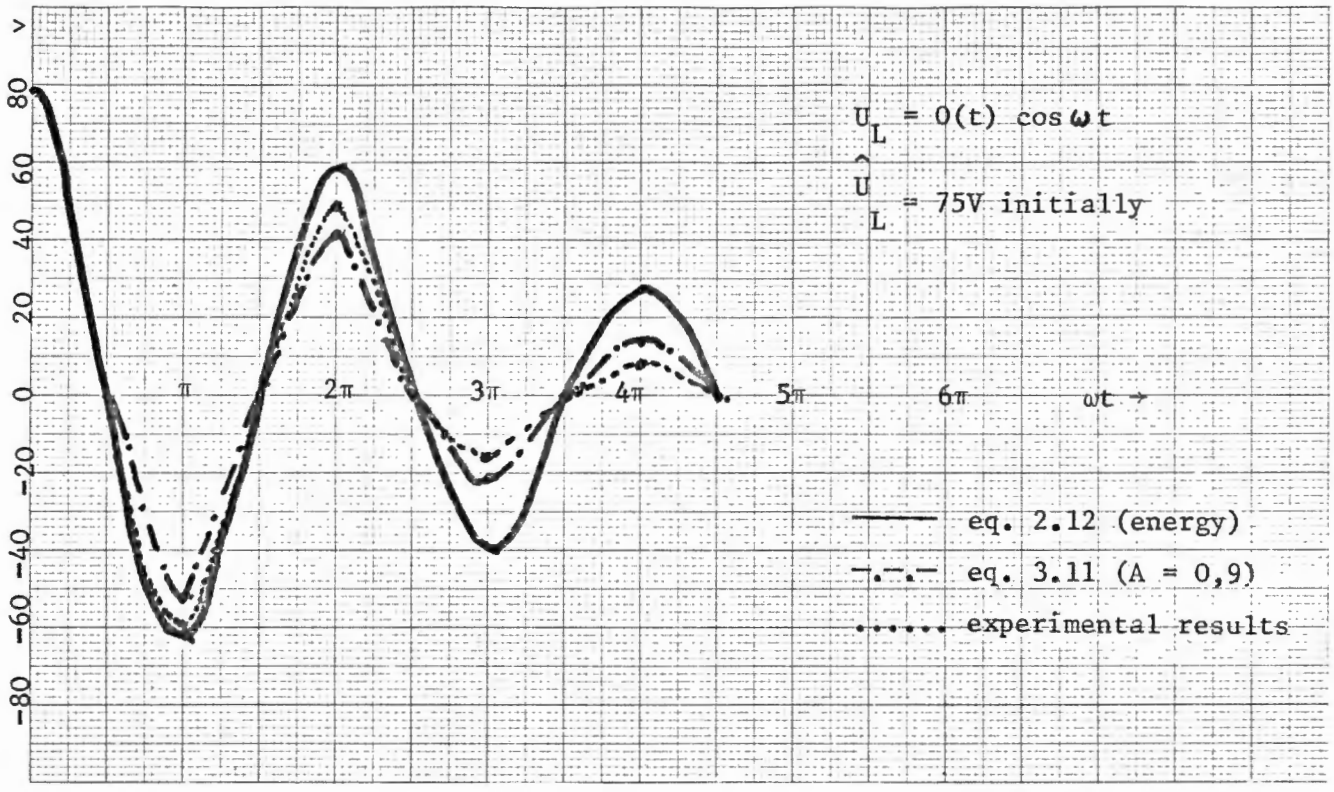

Fig. 3.7

Thus, for $\hat{U}_L$ = 75V, 2 buckets are generated at switch-off and 2 at switch-on. Of these the first, and the second, respectively may be usable. (See Fig. 3.8).

It can be seen that by correct setting of the switch point on the r.f. cycle, a fair approximation to the idealized energy removal process discussed in Section 2 can be obtained.

In the practical system, the switching transient excites parasitic damped resonances in various low-Q tuned circuits. These superimpose spurious signals on the output waveform. (See Fig. 4.2).

A fast r.f. switch incorporating circuitry for eliminating these signals will now be described.

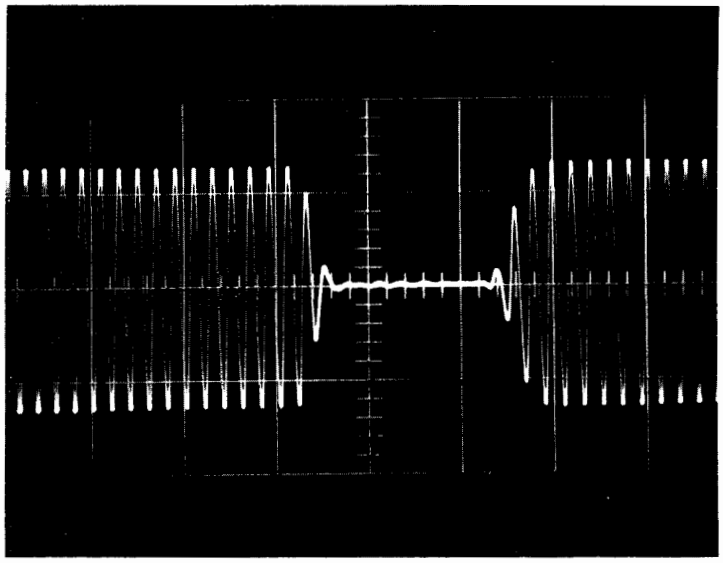

Fig. 3.8. Missing-bucket system performance: r.f. voltage waveform at cavity gap ($\hat{U}_{gap}$ = 75 V).

4. The fast r.f. switch and ringing compensation circuits

4.1. The basic r.f. switch is a commercially available solid-state device using fast diodes. It is driven by logic circuitry controlled by a counter synchronized to the bunch frequency. This counter is set to the number of missing buckets required.

The switch is a bistable changeover type ; its commutation time is of the order of 2 ns. It can switch up to 1.4 V peak in 50Ω; its insertion loss is about 1 dB and its isolation when "off" is 30 dB or better. By suitably delaying the control pulses it is possible to move the switching point anywhere on the r.f. cycle; the switching time is so short that a 9.5 MHz sinewave is hardly perturbed.

4.2. The ringing phenomenon

As mentioned above, the switching process excites a heavily-damped resonance (ringing)in the amplifier chain. There are four low-Q tuned circuits in the system; two coils which serve to tune out interelectrode and stray capacitances in the intermediate amplifier (L2 and L3 in Fig.3.2) the broadband inverting transformer and the filament choke of the P.A. tube. All these are broadly tuned to 9.5 MHz.

It has been established from measurements on the already existing amplifier system that the spurious signal is of the form of a damped sinewave having an initial peak amplitude approximately 13 db below peak r.f. gap voltage, and decaying at a rate given by a Q of about 1.

This signal appears across the gap after switch-off, and is superimposed on the gap voltage after switch-on. (See Fig. 4.2).

Although the relative amplitude of this ringing is quite low, it is felt that its suppression is justified in order to minimize beam perturbation.

4.3. The compensating circuit

Investigations carried out on the existing r.f. amplifier system have shown that it is possible to neutralize the spurious ringing signal by injecting a damped sinewave at the input*.

This compensating signal must bear the same amplitude relationship to the input as what the spurious does to the output, and must have the same damping. The compensating signal must as nearly as possible be in anti-phase with the spurious.

The simplest method for generating the compensating signal is to drive with the chopped sinusoidal r.f. a tuned circuit of low but variable Q. For this purpose the drive signal is split off from the main input and fed via a variable attenuator to an amplifier which drives the tuned circuit ("ringing circuit"). The tuning and working Q of the ringing circuit are variable by means of preset controls.

The output of the ringing circuit is added algebraically via a delay line to the main drive signal to the cavity. (Fig. 4.1). This delay line is variable and serves to set up the correct phase relationship between the ringing and drive signals.

The ringing signal is heavily damped by a variable shunt resistance. It is provided with trimmers for fine tuning and Q adjustment; these, and the delay, are adjusted for optimum suppression of the spurious ringing signal.

The ringing circuit is operated at a Q close to unity; its bandwidth is thus sufficient to obviate any need for retuning in the band 9487 .... 9534 kHz corresponding to the energy range 9 .... 28 GeV. This is the largest frequency shift which will be encountered in the ISR r.f. system.

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* See appendix II

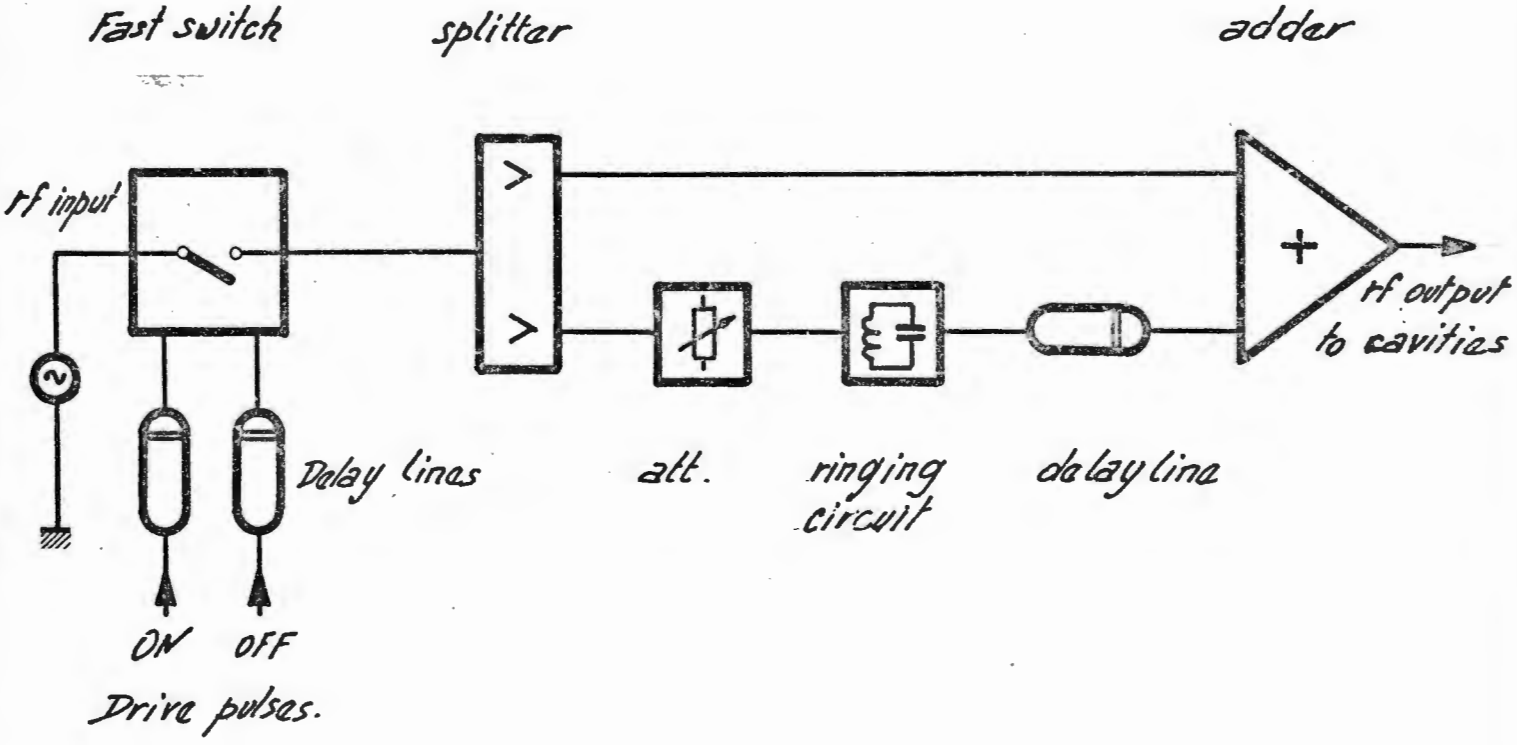

Fig. 4.1 : Block diagram of rf. switch and compensation circuit.

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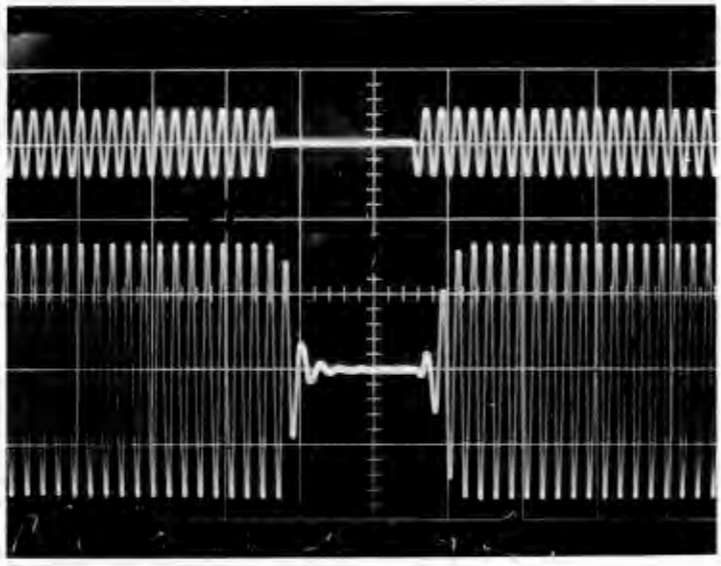

Fig. 4.2. R.F. Voltage waveform at cavity gap

<u>without</u> ringing compensation.

($\hat{U}_{gap}$ = 75 V).

Upper trace : drive

Lower trace : gap voltage

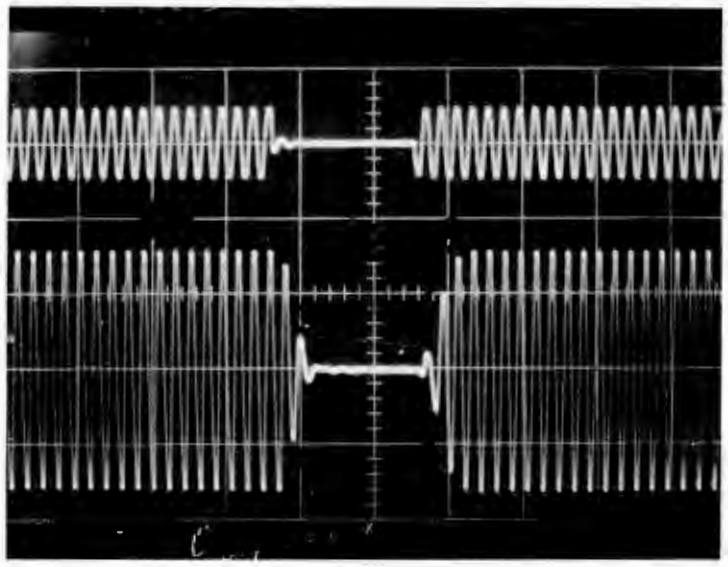

Fig. 4.3. R.F. Voltage at cavity gap with ringing compensation. ($\hat{U}_{gap}$ = 75 V).

The ringing circuit is enclosed in a plug-in chassis module which also contains drive and output amplifiers. In keeping with a standard adopted throughout the system, input and output impedances are 50Ω.

The summing network via which the ringing signal is added into the main signal line consists of a pair of broadband grounded-base amplifiers with a common collector load and output isolator. This device has a bandwidth of 100 MHz and thus passes the keyed sinewave almost undistorted. The same is true for the active signal splitters, which consist of groups of emitter followers with a common input.

Figures 4.2 and 4.3 show the r.f. voltage waveform at the cavity gap with and without compensation. It will be seen that the improvement due to the compensation circuit is worthwhile.

4.4. The control circuitry.

By this is meant the electronics associated with the fast switch. As outlined in 4.1, the r.f. switch is a commercial "black box". The switch, with its associated driver and control counter, is of a type used extensively in other parts of the ISR r.f. system.[4] It was adopted here in the interest of standardization.

The switch is controlled by a preset counter clock (CN2 in Fig. 4.4), built into the switch chassis module, which is synchronized to the 9.5 MHz master frequency and has a counting cycle of 30 pulses, corresponding to 30 bunches. The counter generates a pulse which can be preset to any count from 1 to 30.

The switch driver has two logic pulse inputs corresponding to the states of the switch. The counter is so arranged in conjunction with the switch that a "start" pulse sets the switch and starts the counter. After a preset number of pulses, the counter resets itself and the switch, and stops. The system is now ready for the next "start" pulse.

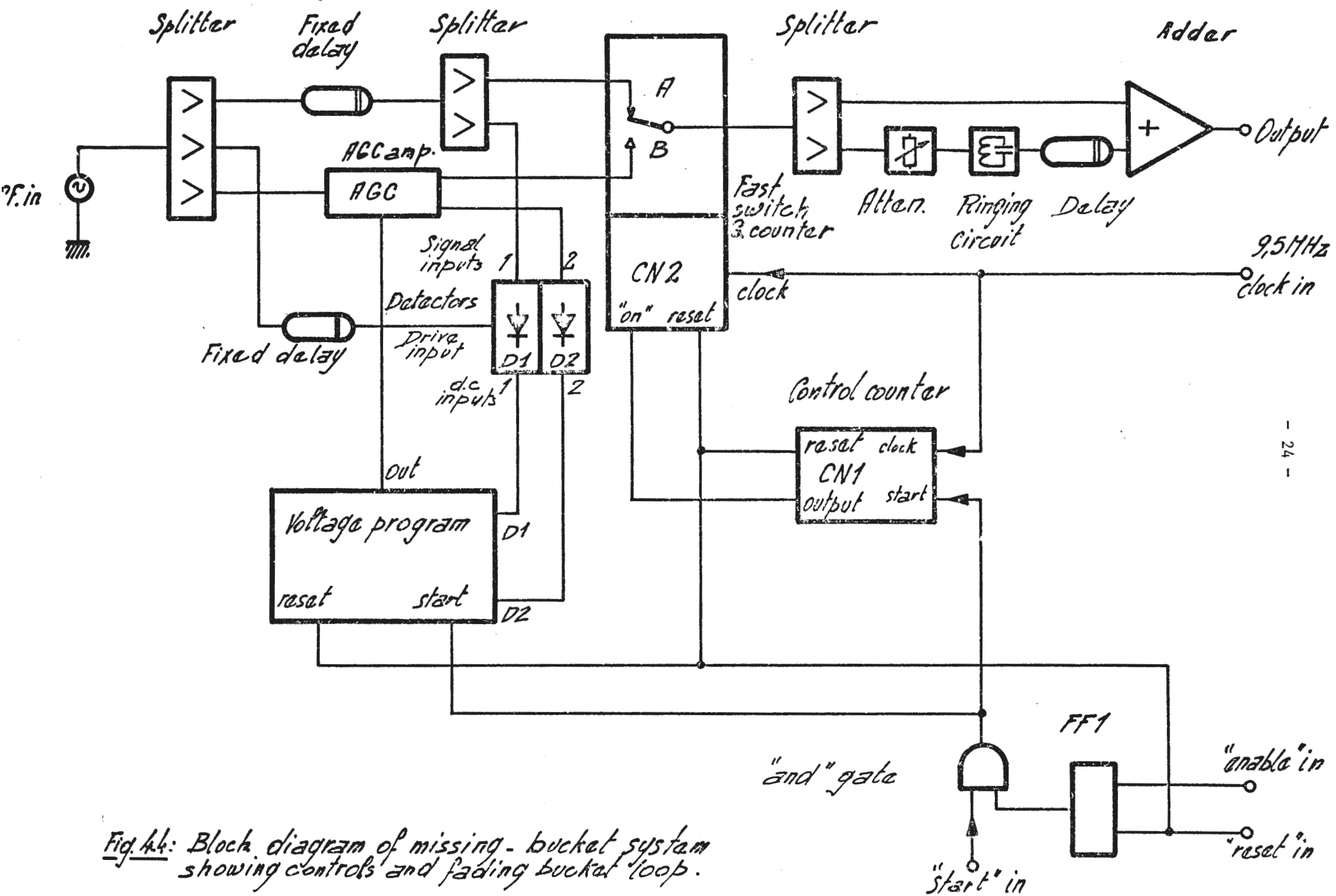

Fig. 44: Block diagram of missing-bucket system showing controls and fading bucket loop.

The switch is connected so that it cuts off the r.f. drive to the cavity when in the "set" state*. Thus the number of buckets to be suppressed may be selected by a front panel control on the switch module.

The switch is started by a second preset counter (CN1 in Fig. 4.4) which is similar to the unit described above. Counter CN1 is, however, in a chassis on its own and delivers two output pulses, one corresponding to count 30 and the other preset by a front panel control to any count from 1 to 30. CN1 runs off the same clock as CN2.

CN1 is started by a pulse derived from the beam phase lock system and synchronized to the master clock. This "start" pulse passes through a gate which opens only when the r.f. accelerating voltage falls to the preset level at which missing bucket operation is desired (75 to 100V peak).

The start pulse starts CN1; this counter starts CN2 and sets the switch after a preset number of counts. CN1 is preset so that the switch is set just after the last bunch has passed the accelerating gap. CN1 runs on and restarts the switching cycle until both counters are stopped and reset by a general reset pulse which coincides with the end of the stacking cycle.

Counter CN1 is also of a type used extensively elsewhere in the ISR r.f. system; both counters, as well as the switch control logic, use Texas 74-series TTL.

A block diagram showing the control system is given in Fig. 4.4. Figure 4.5. us a time chart showing pulse and r.f. timing relationships in the system.

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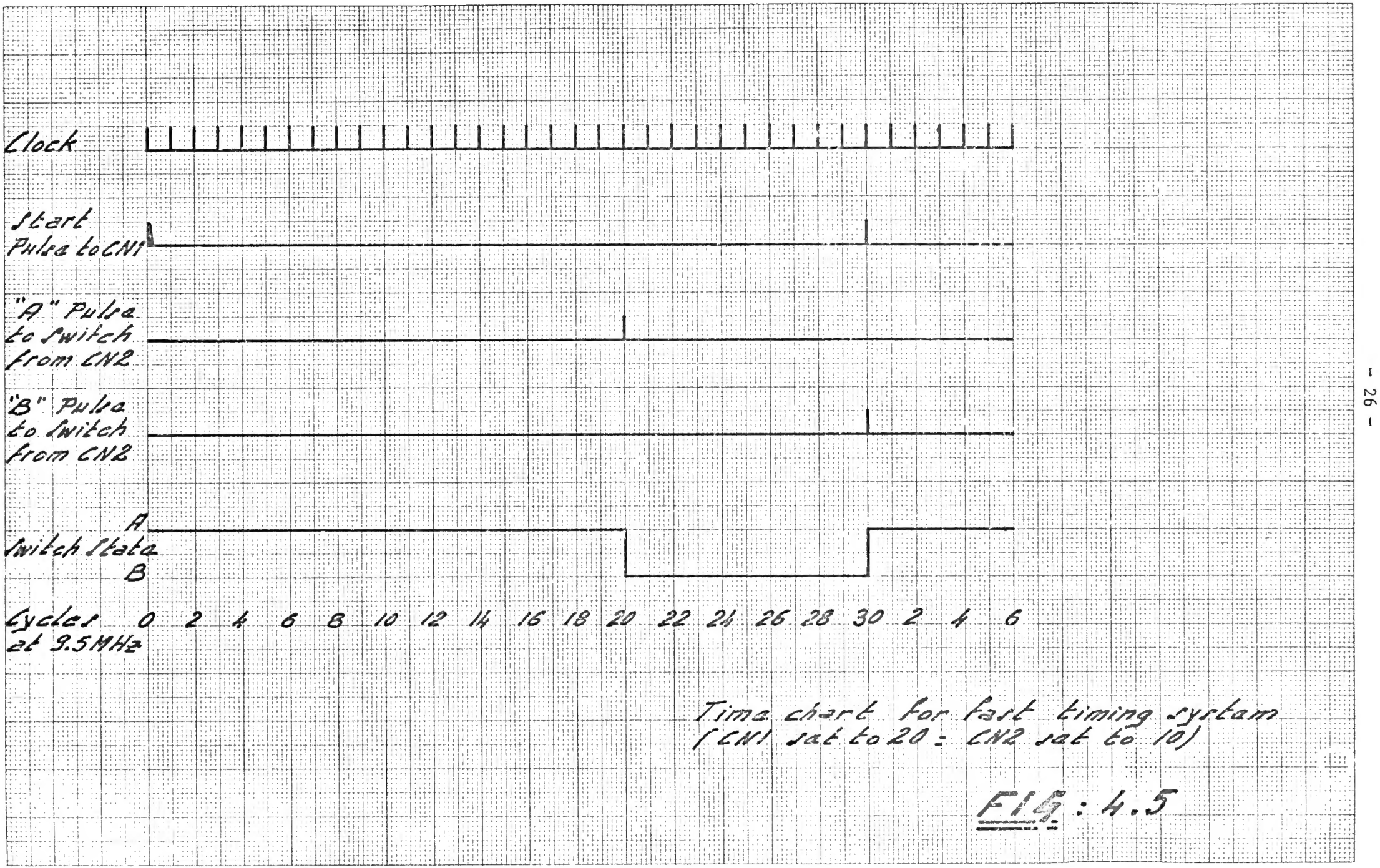
* In the "fading buckets" mode, the "set" state corresponds to the variable-gain channel. See section 5.



Time chart for fast timing system
(CN1 set to 20 : CN2 set to 10)

FIG : 4.5

By delaying the "clock" and "start" pulses going to CN1, it is possible to set the switch-on and switch-off points independently on the r.f. waveform.

One minor but nonetheless important feature of the fast r.f. switch is that it is bi-directional; it will accept drive from either side. This is significant, as we shall see, in "fading-bucket" operation.

5. "Fading buckets"

5.1. General

This term describes a technique of progressively turning down the amplitude of the empty buckets to zero as the accelerated beam approaches the stack. It is hoped that this method will minimize the phase perturbation and dilution induced in the stacked beam by the residual empty buckets generated by the switching process.

It is desirable to have the facility of reducing the amplitude of the empty buckets to zero, independently of the main ISR r.f. voltage program, during a period of time which is a compromise between the beam phase oscillation period (0.5s) and the turn-round time (0.3s) of the machine. The turndown follows an exponential law in the present system, although this may be changed later.

The simplest way of controlling the amplitude of the empty buckets is to arrange the fast r.f. switch so that instead of simply interrupting the signal path it commutates between two sources, A and B, A being of fixed amplitude and B being of variable amplitude but remaining exactly in phase with A at all voltage levels. This is essential in order to avoid phase jumps when switching.

In practice the incoming signal path is split into two branches A and B. (See Fig. 4.4) B is the variable-gain channel corresponding to "empty buckets" and is connected to the "set" terminal of the fast switch via the gain-control device. "A" is the fixed-gain channel corresponding

to "full buckets" and feeds the "reset" terminal of the switch via a phase inverting transformer (the gain control device has 180° phase shift) and a delay line whose delay is equal to that of the gain-control device. Incidentally, it is here that the symmetry of the fast switch comes in useful ..... the "in" terminal becomes the output.

The compensating circuit described in 4.3 remains unchanged, as the spurious ringing signal generated by switching channels has an initial amplitude proportional to the difference between the levels of channels A and B. This will be seen from Fig. 5.1.

5.2. The gain-control device consists of a four-stage amplifier employing variable -μ pentodes. This was chosen in preference to a semiconductor amplifier as the phase-shift between input and output over the gain-control range is far smaller than that which could be attained using solid-state devices. Over a control range of 60 dB, the phase shift is less than 2° at 9.5 MHz.

The automatic gain-control (AGC) amplifier unit, like the fast switch, is a "building block" used in other parts of the r.f. system for the ISR.[5] The amplifier is in a closed loop in which the r.f. voltage at channel B is compared with the turndown voltage program. This ensures that the envelope of the empty-bucket gap voltage is an exact replica of the program law chosen.

5.3. The fading-bucket voltage program

The voltage program unit contains the d.c. amplifiers for the control loop, the voltage program and cut-off timing capacitor groups with their selector circuitry, and control logic. The unit is enclosed in a plug-in NIM chassis.

5.3.1. Operational features

As will be seen from Fig. 5.2 the loop compares the r.f. voltage at Channel B with a reference. When the missing bucket system is in the rest state (during the earlier part of the stacking cycle) this reference is provided by Channel A, which charges the voltage program capacitor to its peak voltage. This also sets the initial value for the empty-bucket voltage.

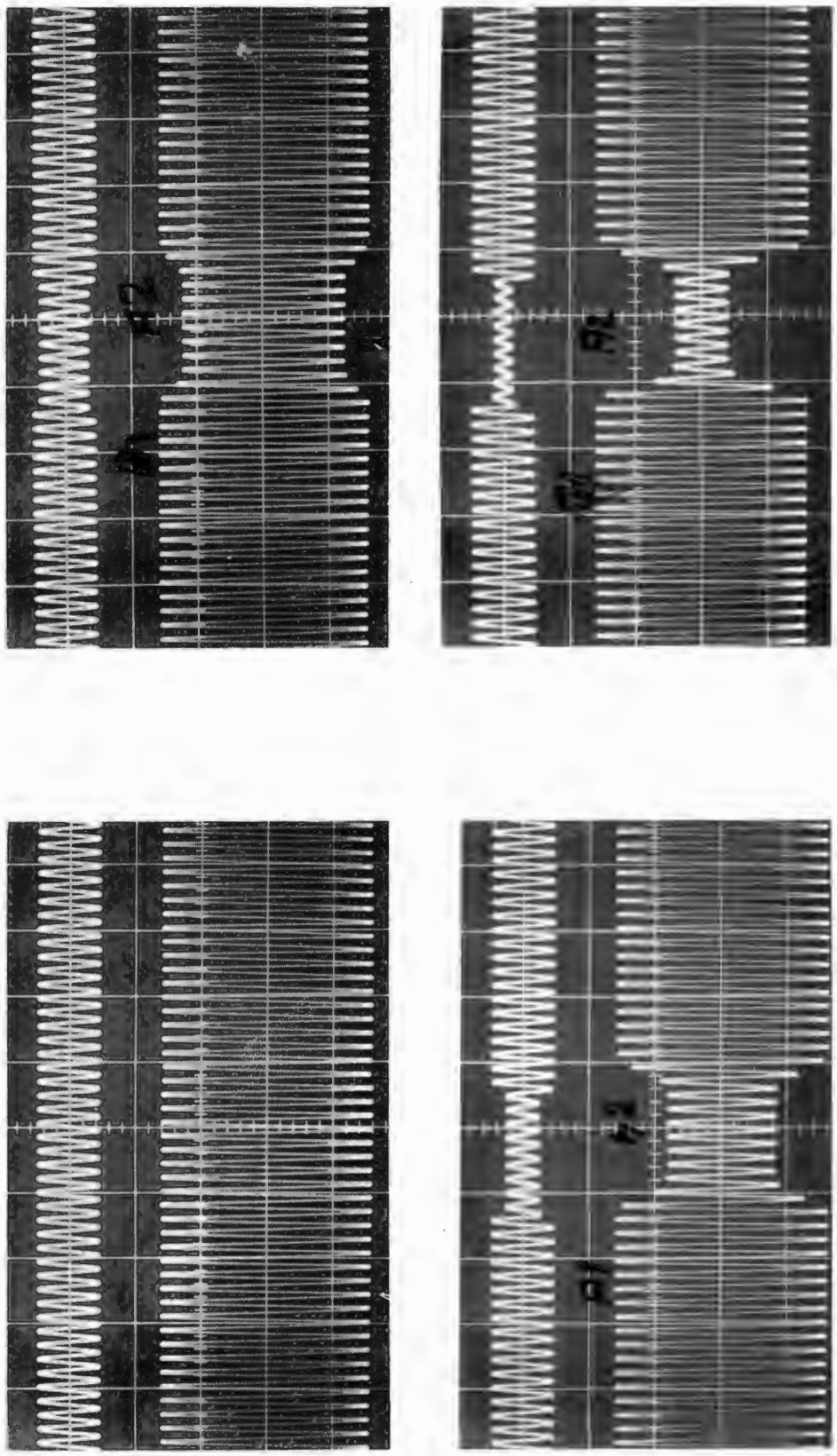


Fig. 5.1. Fading buckets. $\hat{U}_{gap}$ = 75 V.

The "start" pulse, as well as starting the counters, operates a relay in the voltage program unit which disconnects this capacitor from its charging source. The capacitor now discharges into a fixed resistance, and the Channel B voltage follows it exactly.

At the end of the stacking cycle, the general "reset" pulse restores the reference to Channel A and readies the loop for the next cycle.

The time constant of the voltage program is variable from 10 ms to 10s with 10 ms resolution. Selection is accomplished by switching capacitors arranged in 1-2-2-4-coded groups. Local and remote control facilities are provided for this, as also for the "cut-off" feature.

At a preset time after the "start" pulse the voltage program may be abruptly cut off. Experiments in stacking with this mode of operation may be interesting.

The cut-off circuit consists of a monostable which is triggered by the "start" pulse and short-circuits the voltage program capacitor via an FET switch after a preset time interval. This time may be varied from 10ms to 10 s as described for the voltage program.

It is possible to disable the cut-off circuit by means of a front-panel (or remote) switch. In addition, the system can be switched over to normal missing-bucket operation (empty buckets suppressed entirely) by setting the time constant selector to zero.

5.3.2. Control loop considerations

The grid control characteristic of the AGC amplifier is extremely non-linear; a sensitivity variation of 1000 to 1 between the high - and low - gain extremities of the gain-variation range is typical.

In order to achieve good tracking without the complexity of compensating circuits containing non-linear elements, the d.c. loop gain can be made very high while limiting the bandwidth to ensure system stability. To this end, an integrator employing an operational amplifier whose open-loop gain is 10^5 or more, forms the forward-gain-determining element of the loop. The integrator time constant is 100μS, which ensures a response time comparable to the shortest voltage-program time constant, together with a reasonable margin of stability.

The disadvantage of this type of brute-force linearisation is that the frequency response of the loop is poor at low signal amplitude; however, this is not a great problem here, as the voltage program decays relatively slowly.

The slewing rate of the loop is 1 V/s at an r.f. voltage level of 10 mV, (cf. 2kV/s at a level of 1 V). By comparison, the rate of change of voltage at the low end of the voltage-program curve is of the order of 0.1 V/s for a time constant of 10 mS.

Linearity and stability behaviour of the loop are discussed in greater detail in Appendix II.

5.3.3. Loop circuit details (Fig. 5.2)

The d.c. voltage level derived from channel A charges the voltage-program capacitor via an active isolator A1 and the control relay. An operational amplifier A2 with FET input stages, connected for unity gain, ensures that the capacitor is loaded only by the discharge resistor. The output of A1 is summed with the d.c. level from Channel B at the input of integrator A3. A further unity-gain operational amplifier A4 provides the possibility of "offset" adjustment. This is set so that the AGC amplifier is biased off when the reference voltage is zero. It is set up by disconnecting the Channel A input and adjusting the bias on A4 for zero r.f. output voltage.

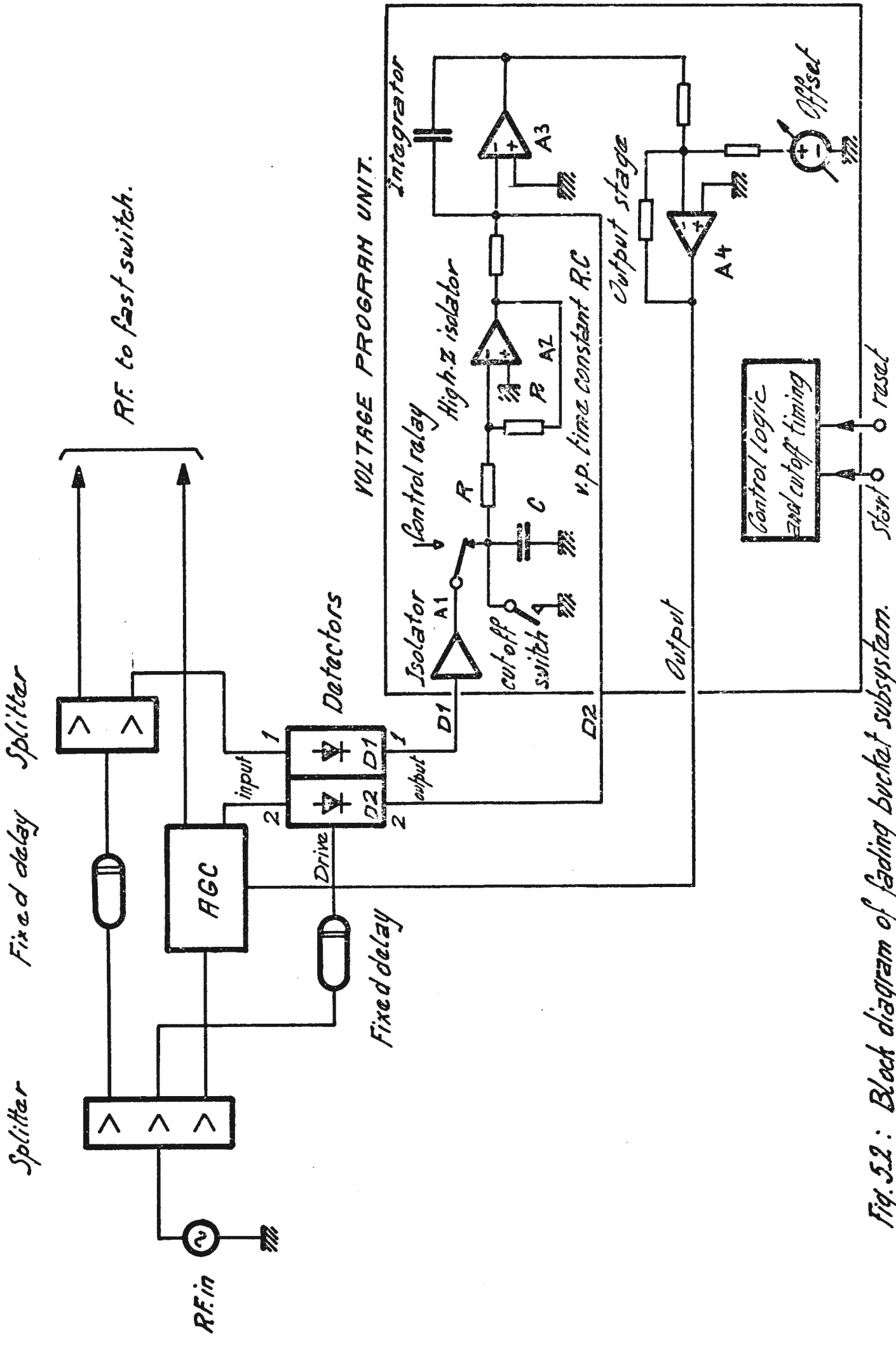


Fig. 5.2 : Block diagram of fading bucket subsystem.

The high loop gain, combined with the good linearity and large dynamic range of the detectors, ensure a control range of 50 db or better (IV ... 3m V peak r.f on Channel B). Overall loop tracking error is 0.3%. Noise is 1 mV peak-to-peak at the gain control amplifier output.

5.4. The detectors are identical synchronous sampling rectifiers employing hot-carrier diodes. Despite their complexity and their need for a drive signal, they offer very good linearity (less than 1% distortion) over a large dynamic range (5μV to 1,4V peak), together with good long-term stability.

The drive signal is taken from the signal splitter at the input to the system. The sinewave is converted to a pulse which opens the sampling gate at the negative peak of the signal to be rectified. The sampling period is 20nS.

Both detectors with their drive pulse generator are built into one NIM plug-in chassis.

5.5. Overall specifications of the fading-bucket subsystem at 9.5 MHz

1. Maximum r.f. output voltage: 1,4 peak into 50Ω
2. Control range : Better than 50 dB
3. Decay time constant range of voltage program: 10ms to 10s , with 10ms resolution.
4. Cutt-off delay range (time between "start" pulse and abrupt cut-off of output voltage) 10ms to 10s, with 10ms resolution.
5. Loop control bandwidth : 1.6 KHz at full voltage.

6. Tests on the Missing-Bucket System

Various performance tests have been carried out on the system. In most cases the system was run in conjunction with a complete cavity and r.f. amplifier chain. A test has also been performed with the whole ISR r.f. system including the missing-bucket equipment, driving all seven cavities installed in the machine tunnel. (See Fig. 6.5A).

6.1. An overall system test was first set up, in which the cavity was tuned to 9500 KHz and driven via the missing-bucket system. A block diagram of the test setup is given in Fig. 6.1.

The system was optimized with the fading-bucket circuitry disabled: the waveform appearing at the cavity gap was then recorded both in normal missing-bucket mode and in fading-bucket mode.

The results of this test are given in Figs. 6.3 - 6.5. Figure 6.3 shows the r.f. signal in missing bucket mode for a peak gap voltage of 75V, while Fig. 6.4 is the fading-bucket modulation envelope for a time constant of 0.5s with cut-off 0.6s after start. Figure 6.5 shows the r.f. signal again with conditions as for Fig.6.4. Here the progressive decay and final abrupt disappearance of the empty buckets can be seen.

6.2. A phase coherence test was next carried out. Here the phase deviation of the last three cycles after switch-off and of the first three cycles after switch-on was measured with respect to a reference signal derived from the system input. Fig. 6.6 illustrates the test setup used here. The test was performed only in missing-bucket mode.

The x-y recorder was swept externally, via the oscilloscope, from a sawtooth generator. For each set of recordings (one for switch-off and one for switch-on) two passes were taken, one with the cavity output signal and one with the reference signal. The offset controls were adjusted so that the two signals would be recorded in precisely the same phase at the starting point. This facilitated phase measurement off the graphs.

The recordings are reproduced in Figs. 6.7 and 6.8. Figure 6.9 is a record of normal missing-bucket operation. All measurements were made at an r.f. gap voltage of 75V peak.

It will be seen that phase deviation of significant half cycles is less than 2^{o}. Whether this will have any meaningful influence on the beam

remains to be investigated, although it is believed that this error will not be harmful.

6.3. The fading-bucket loop was subsequently tested. The parameters measured were :

1A DC control range (dynamic range of loop).
1B r.f. phase shift over control range.
2 Frequency response of loop
3 Step response of loop
4 Noise

Here the fading-bucket sub-system was isolated, as will be seen in Fig. 6.10.

6.3.1. The dynamic range of the loop and the phase shift of the AGC amplifier over this range were measured at the same time. The loop was set up for 1V peak output and the phasemeter zeroed. The input to signal to detector D1 (Channel A) was attenuated until the loop just opened, as indicated by saturation of the output stage of the voltage program generator. The attenuation and phase shift were noted. The phase shift was less than 2^{o} over a dynamic range of 53dB.

6.3.2. Referring again to Fig. 6.10, a modulating signal was superimposed on the loop via a series resistor at the main summing point in order to measure the system frequency response. The sinusoidal modulating voltage e_m was set for 10% A.M. at a chosen r.f. carrier level e_c and modulation frequency f_m. f_m was then increased until the recovered modulation signal voltage e_m (derived from a detector at the output of the AGC amplifier) dropped by 3dB. This gave the 3dB bandwidth for a given carrier level. This measurement was repeated over the carrier voltage range 0.9V...90mV peak, and a curve drawn up. (Figure 6.11).

6.3.3. A pulsed signal was then applied to the summing point at two carrier voltage levels, 1V peak and 10 mV peak. Slewing rates of 2kV/s at 1V and 1V s at 10 mV were obtained. (Figs. 6.12A/B). As mentioned before, this performance is acceptable.

6.4. Noise was measured at the output of the AGC amplifier. The noise output in the band DC to 150 MHz was 1 mV peak-to-peak - i.e. a signal-to-noise ratio better than 66 dB at a nominal signal level of 1V peak in 50Ω.

7. Conclusion

A missing-bucket system, based on parameters imposed by the existing RF accelerating cavities of the ISR, has been designed, constructed and tested. The performance of the system is felt to be a reasonable compromise between clean suppression of all empty buckets and voltage-handling capability. How good a compromise this is from the viewpoint of beam-density gain, will be known only when the ISR is operational - especially as regards the usefulness of the "fading buckets" mode.

Acknowledgments

The author wishes to express his profound gratitude to Dr. W. Schnell, under whose leadership and guidance the missing-bucket system was developed.

Thanks are due also to Dr. F. Ferger, who kindly made available a working prototype of the ISR cavity and amplifier chain together with complete technical information on this equipment, and with whom many enjoyable and stimulating discussions assisted progress; to Messrs. S. Hansen and M. de Jonge, who contributed to the project standard units which they had designed for use elsewhere in the ISR-RF system, as well as many useful suggestions; to Mr. P. Strolin for his kind assistance in connection with certain theoretical problems; and to those colleagues who assisted in the construction of the equipment.

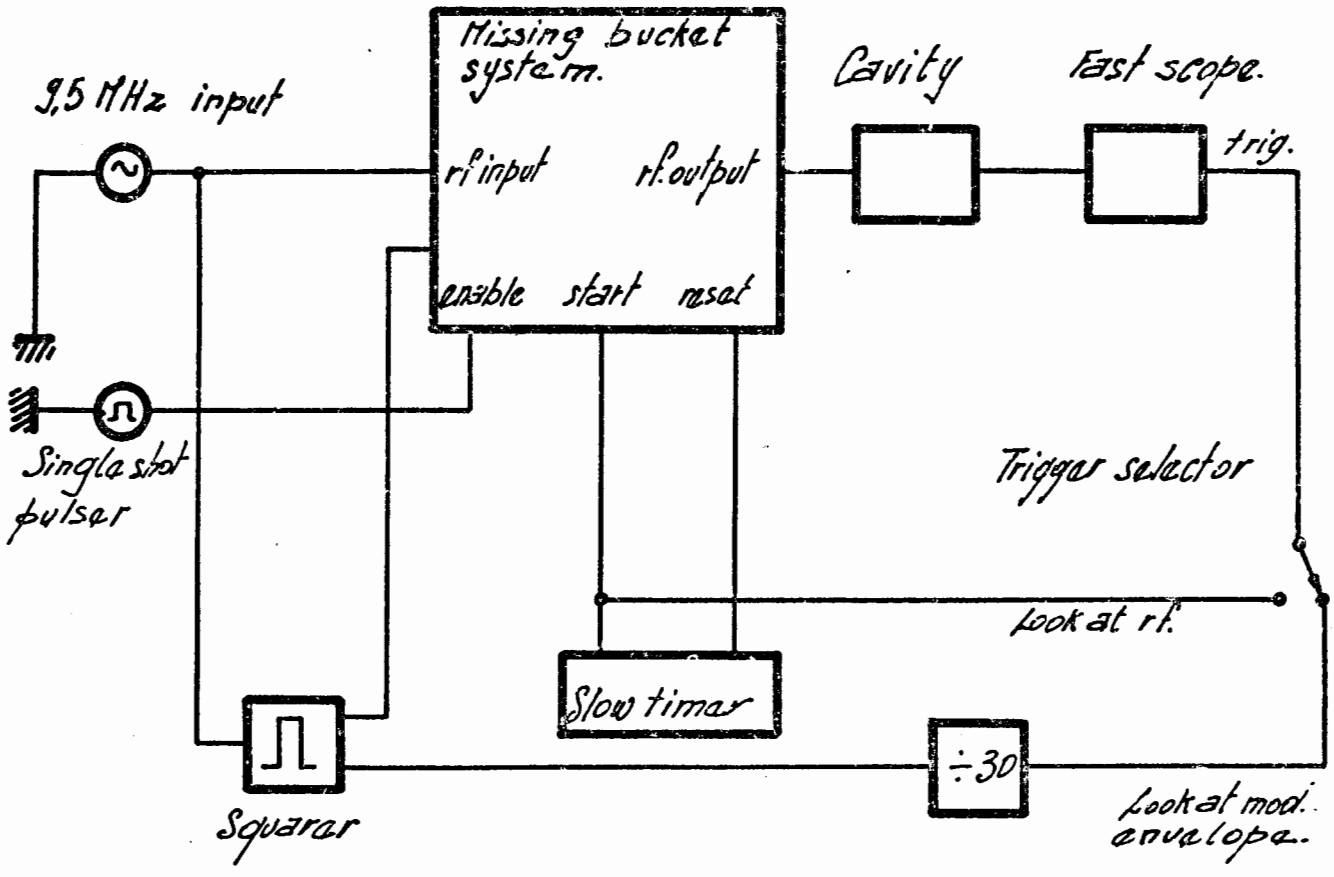


Fig. 6.1: Test set up.

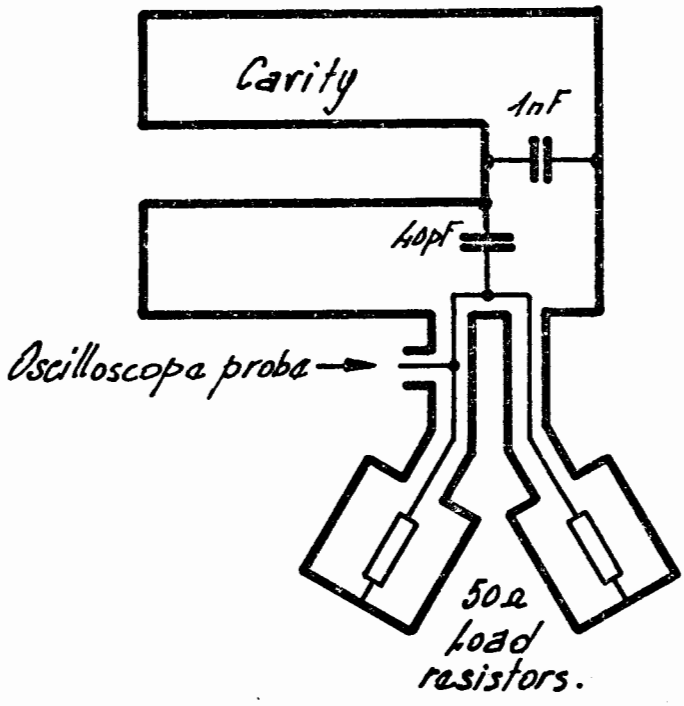


Fig. 6.2: Oscilloscope pick-off on cavity.

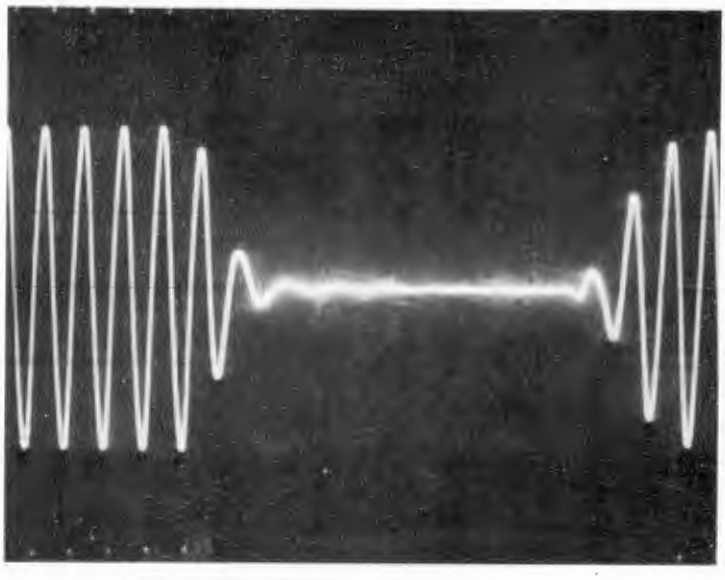


Fig. 6.3. R.F. output in missing bucket mode
$\hat{U}_{gap}$ = 75V

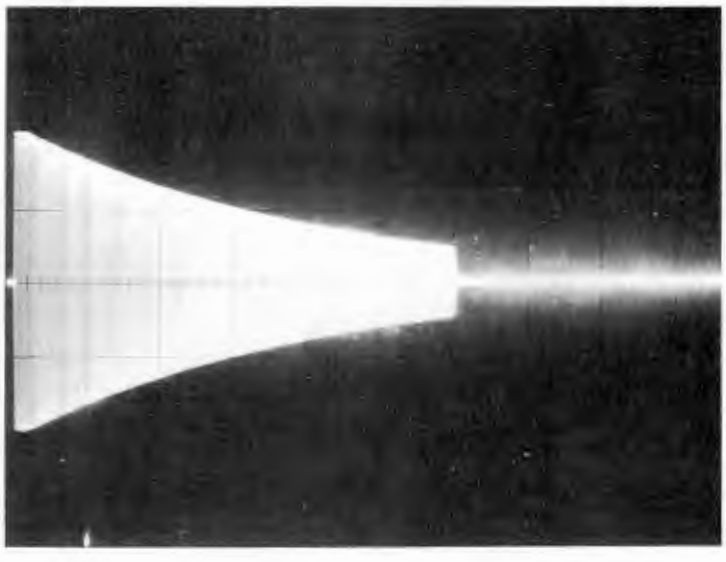


Fig. 6.4. Fading-bucket modulation envelope
Time const. _ 0.6 sec.
Cut-off after 0.6 sec.

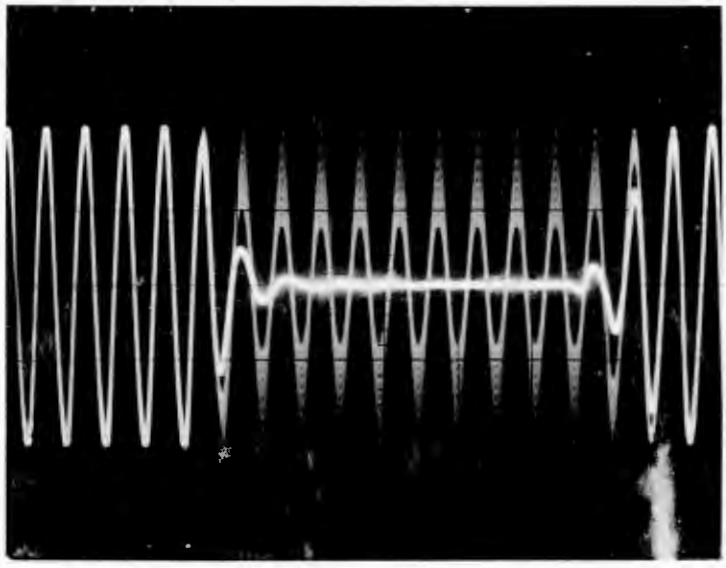


Fig. 6.5. R.F. output in fading-bucket mode with cut-off as in Fig. 6.4.

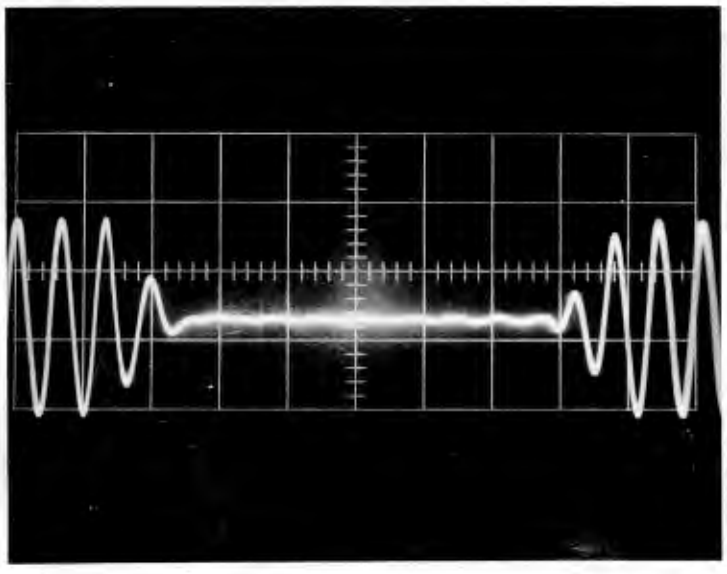


Fig. 6.5A. Missing-bucket mode:
$\hat{U}_{gap}$ = 86 V at cavity No. 6.
(Test run on complete ISR RF system)

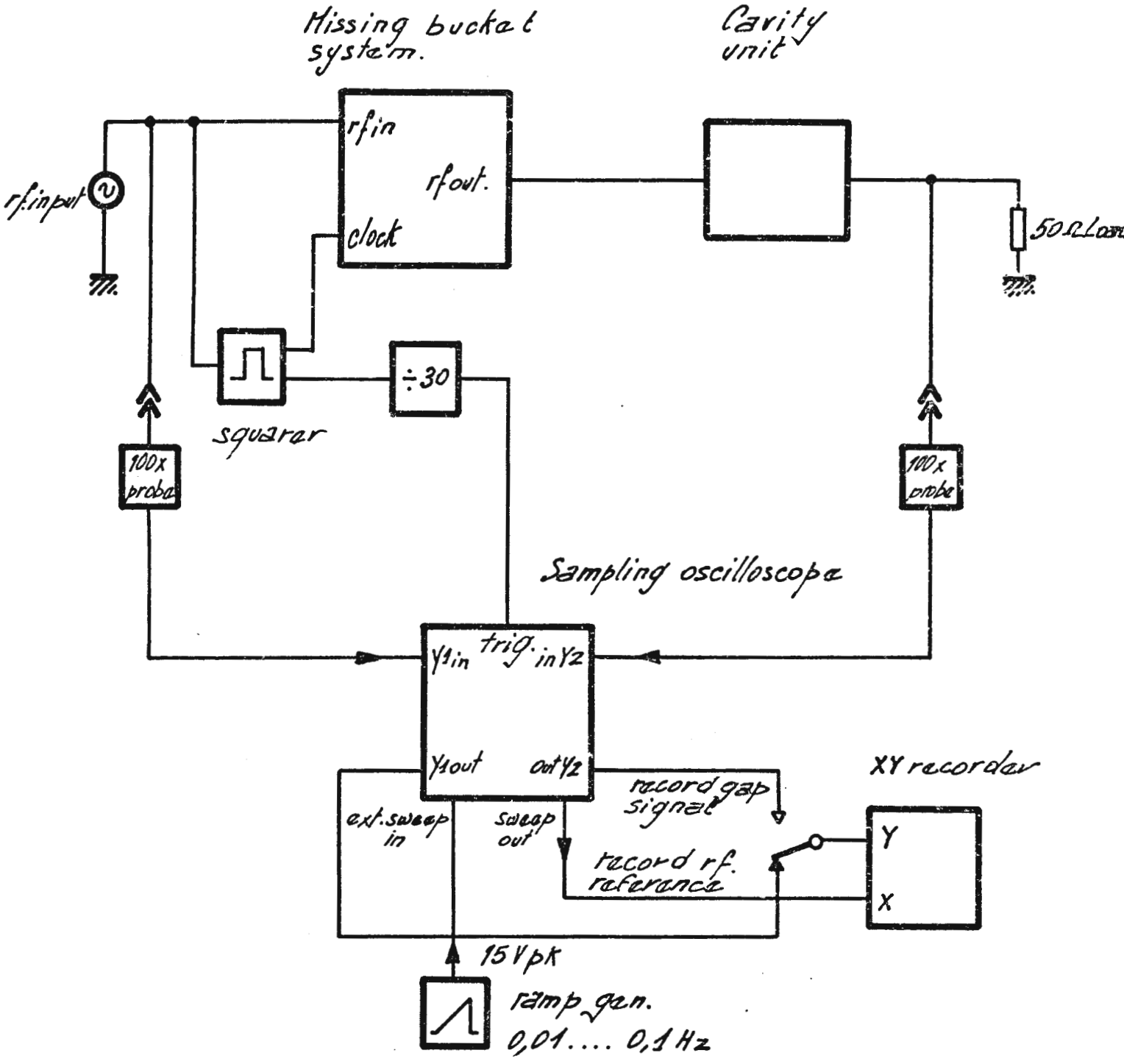


Fig. 6.6: Test set up for phase deviation.

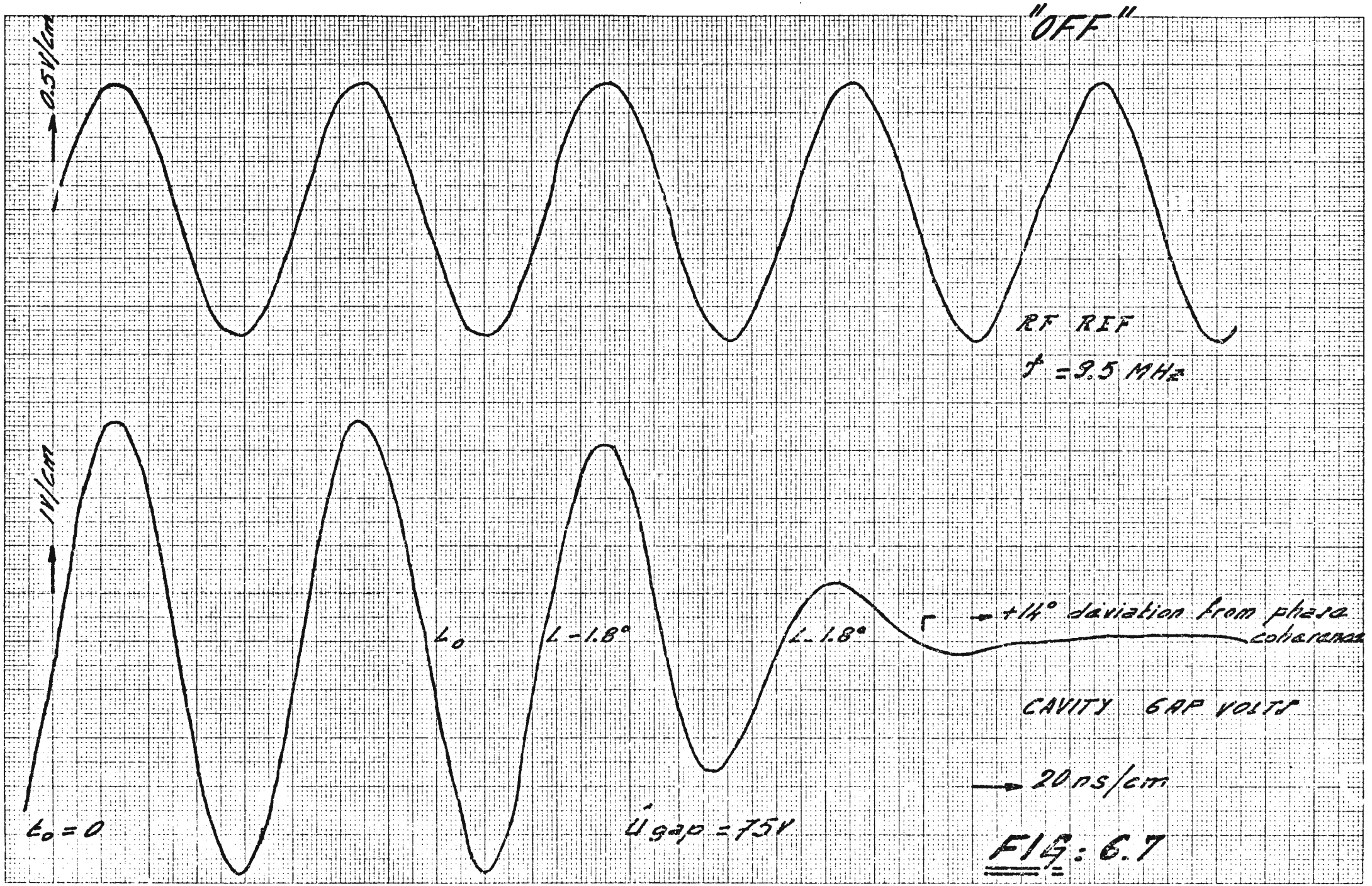
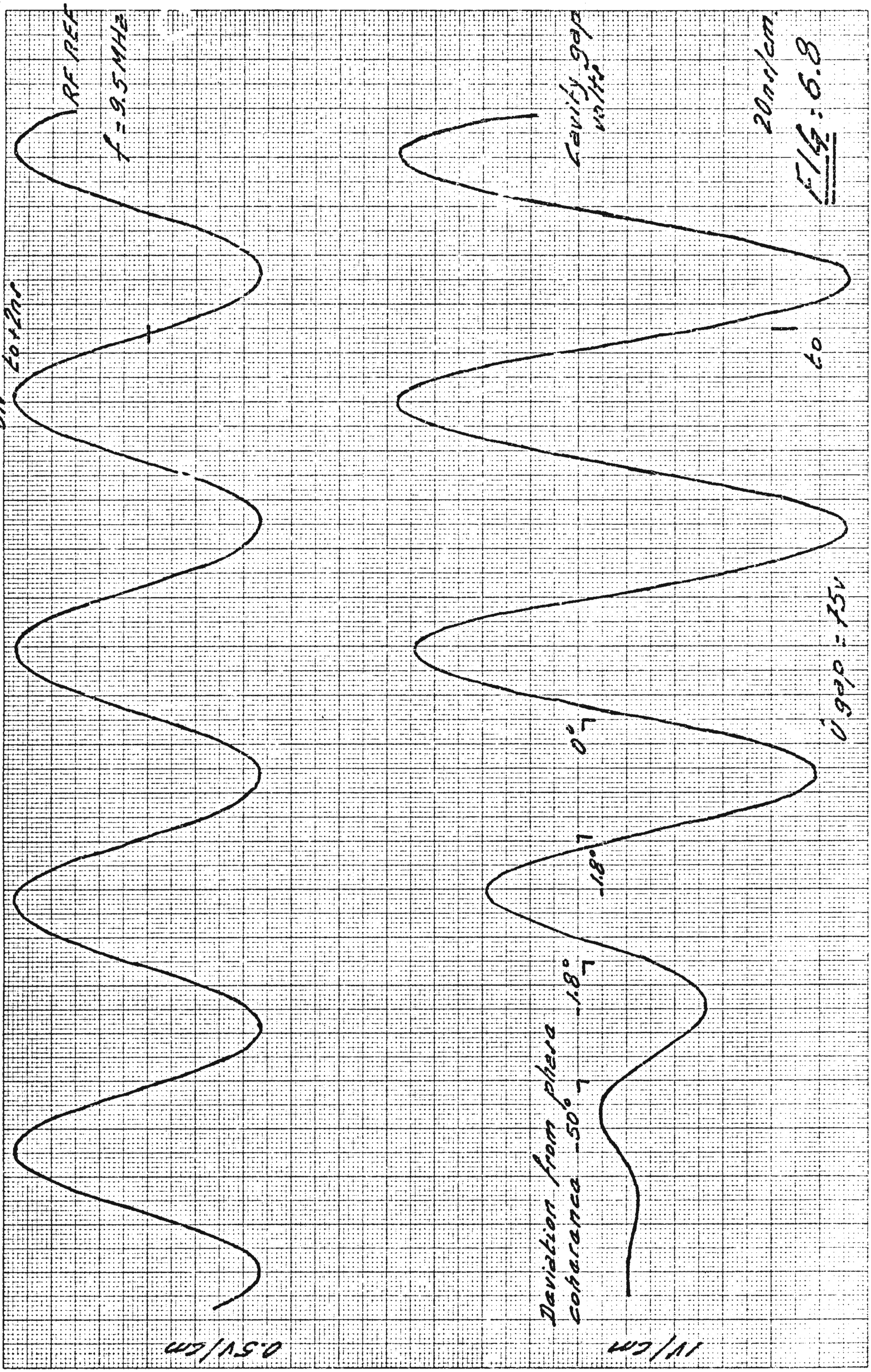

"OFF"
0.5V/cm
RF REF
f = 9.5 MHz
1V/cm
L0
L -1.8°
L -1.8°
+14° deviation from phase coherence
CAVITY GAP VOLTS
20 ns/cm
L0 = 0
Vgap = 75V

FIG: 6.7


RF REF
f = 9.5 MHz
Cavity gap volts
20ns/cm
FIG: 6.8
"ON" for 2ns
Ûgap = 75V
0°
-1.8°
Deviation from phase coherence -50°
-1.8°
0.5V/cm
1V/cm

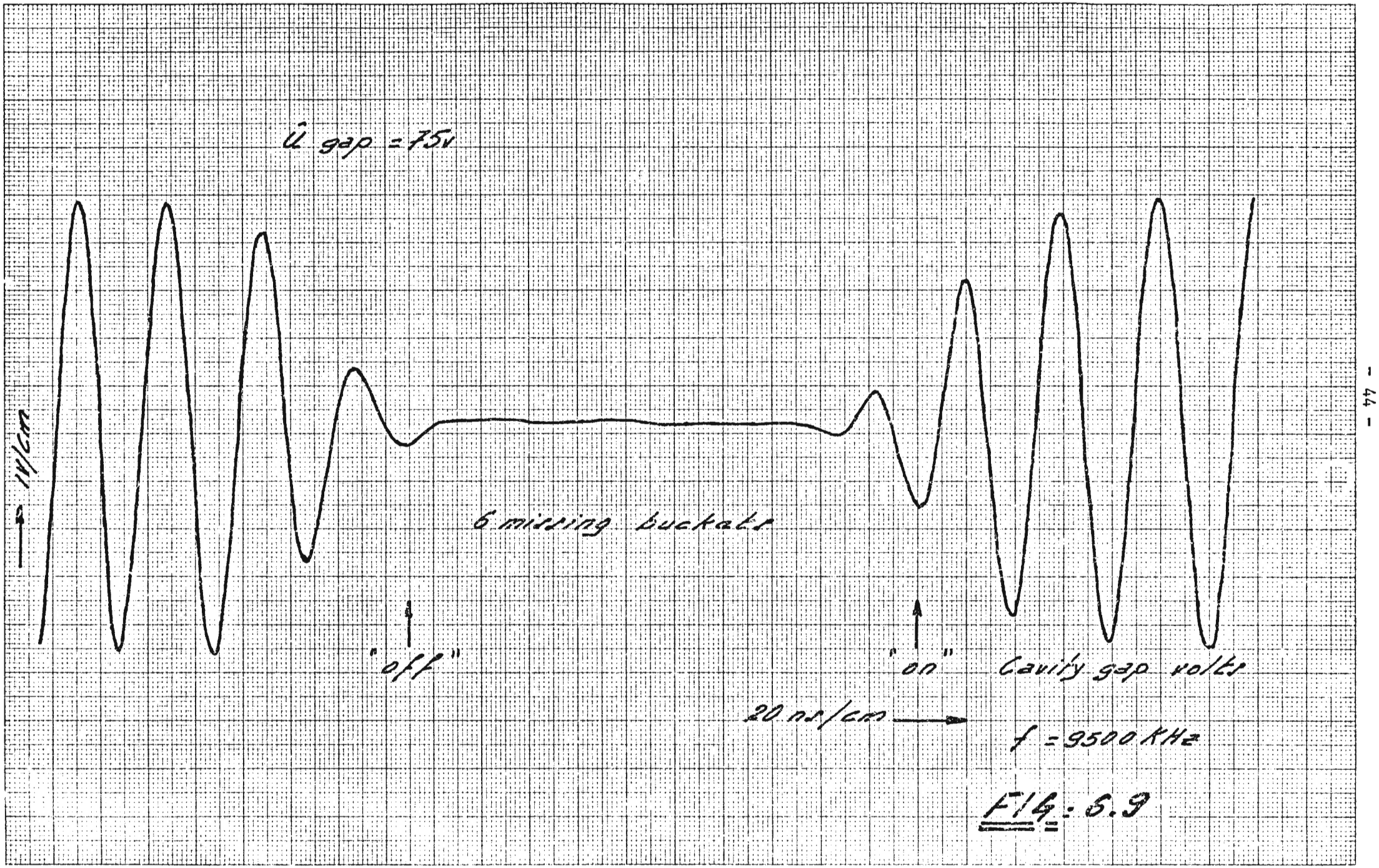


FIG: 5.9

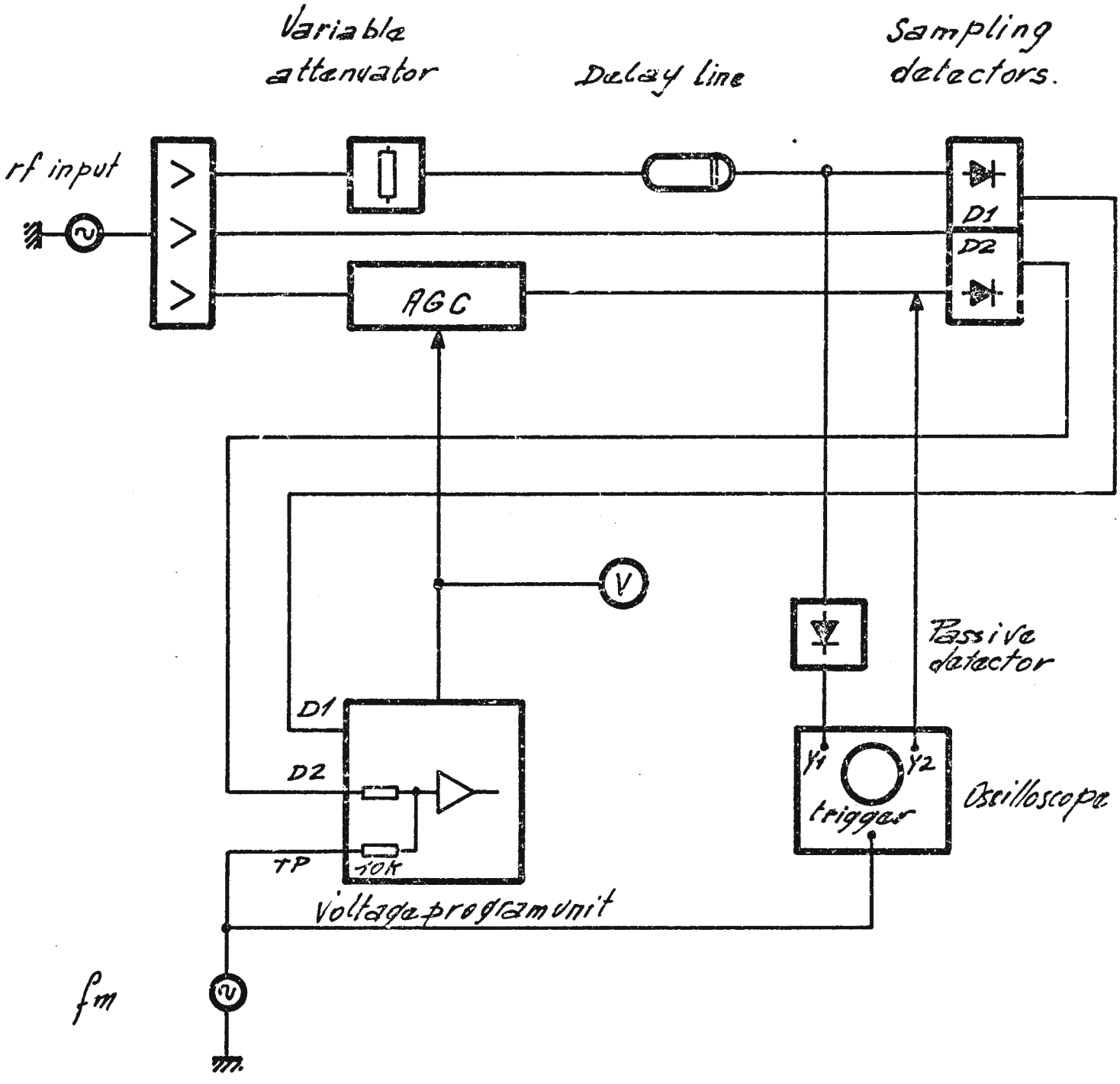


Fig. 6.10 : Test set up for frequency response and dynamic range of voltage program loop.

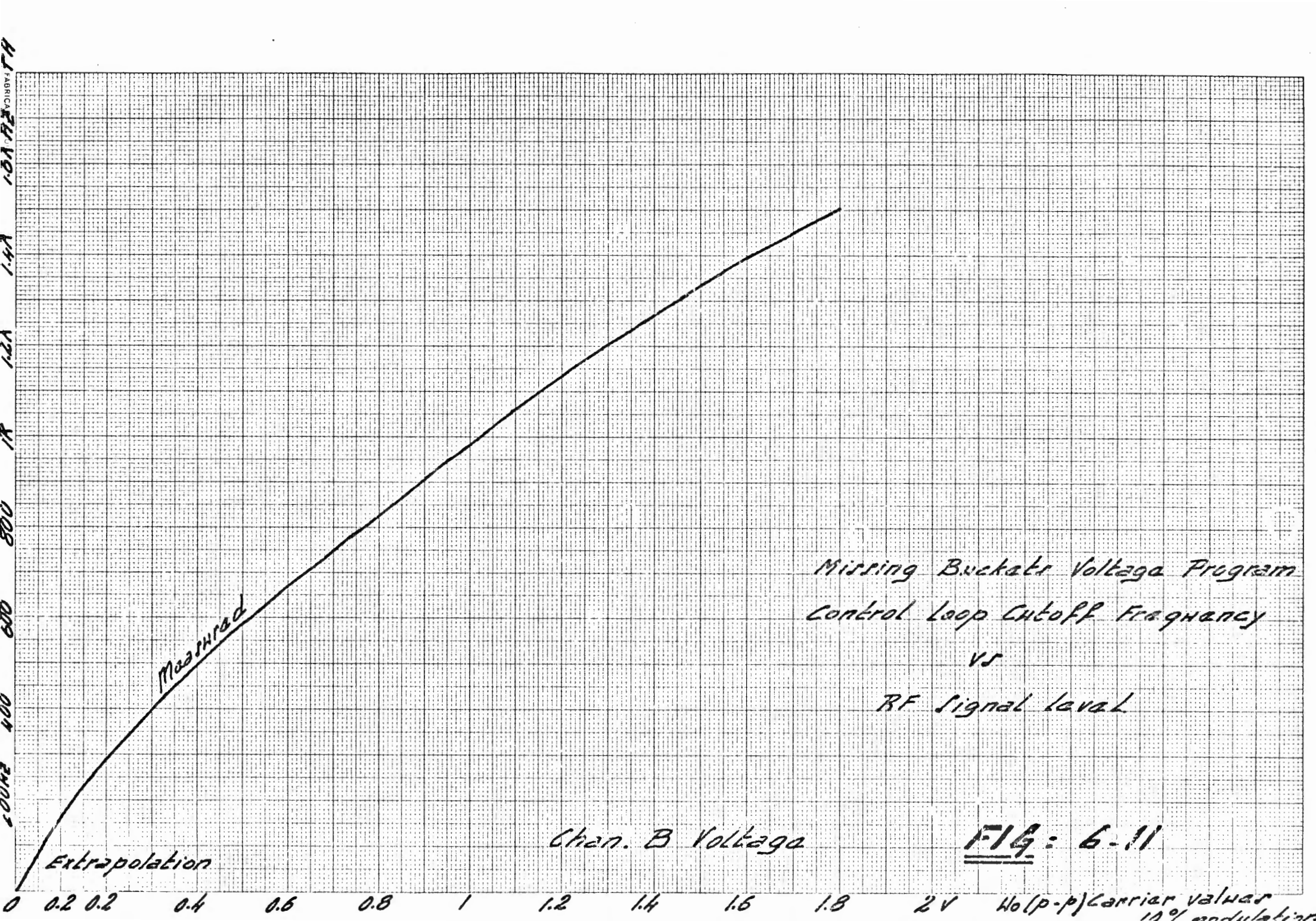
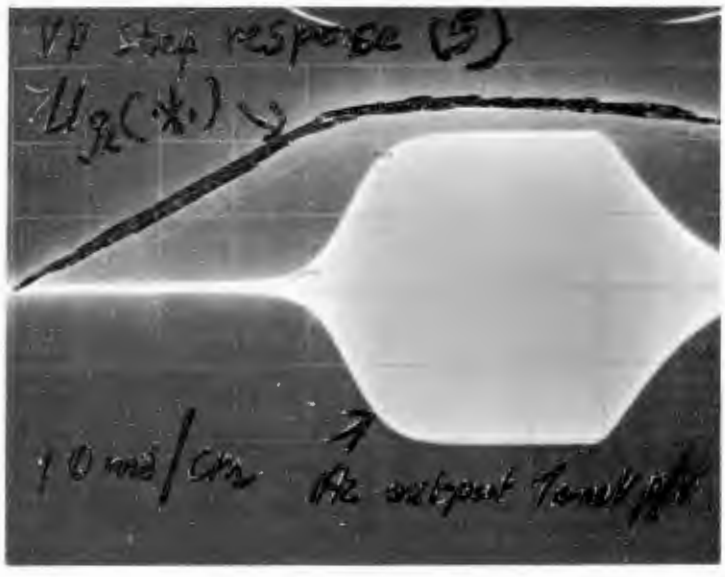
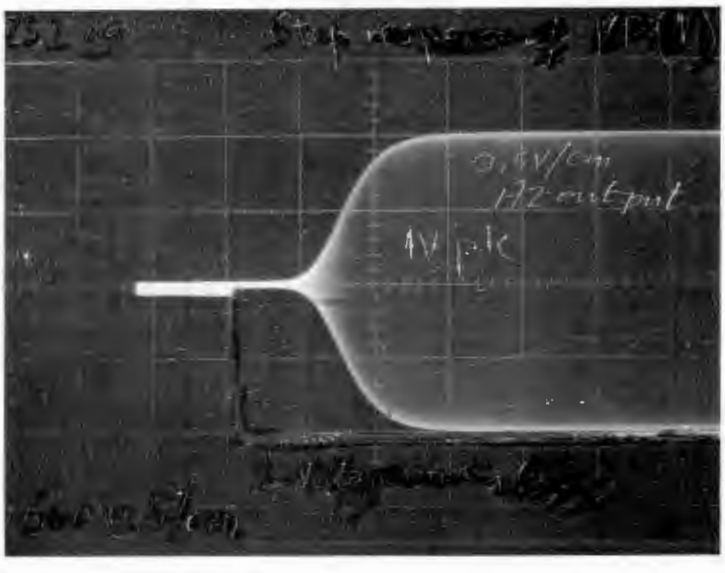

Missing Bucket Voltage Program
Control Loop Cutoff Frequency
vs
RF Signal Level
Measured
Extrapolation
Chan. B Voltage
0 0.2 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2V
No (p-p) Carrier values
10% modulation
200Hz 400 600 800 1K 1.2K 1.4K 1.6K

FIG: 6-11



↑ 5m V/cm
→ 10 mS/cm
low end



↑ 0.5 V/cm
→ 0.5 mS/cm
high end

Fig. 6.12 Slewing rate of loop

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2. Schnell,W.: "Stacking in Proton Storage Rings with Missing Buckets". ISR-RF/67-38, 2nd November, 1967.

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4. Hansen, S.: private communication.

5. De Jonge, M.: private communication.

APPENDIX I

Interfacing of the missing-bucket equipment to the ISR RF system

I.1

For this purpose the missing-bucket system may be thought of as a "box"with the following terminals, as indicated in Fig. I.1:

1. RF input ($1V_{pk}$ in 50Ω) } nominal level throughout missing bucket system
2. RF output ($1V_{pk}$ in 50Ω) }
3. Clock input (1V in 50Ω)
4. "Enable" pulse input (20V in 50Ω).
5. "Start" pulse input (2V in 50Ω : TTL compatible)
6. "Reset" pulse input (20V in 50Ω).

The signal from the ISR-RF master drive unit, frequency-modulated in accordance with the accelerating program enters the missing-bucket system at 1.[3] The processed signal from 2 drives the ISR-RF master voltage program generator, which amplitude-modulates the signal according to the accelerating voltage program. Thence the drive signal is fed to the RF cavities via a line amplifier.

The missing-bucket system must be in its rest state until the main voltage program has turned the r.f. voltage at the cavity gaps down to the level (75 to 100V peak) at which suppression of empty buckets is to commence.

When the preset level is reached, an amplitude comparator in the main voltage program unit generates an "enable" pulse which opens a gate in the "Missing Buckets Control" unit, which forms part of our system.

A "start" pulse derived from the beam phase-lock system and synchronized with the circulating bunches, now starts counters CN1 and CN2, as well as the fading-buckets voltage program, via 5. At this moment the main voltage program has stopped and the fading-bucket subsystem (if it is

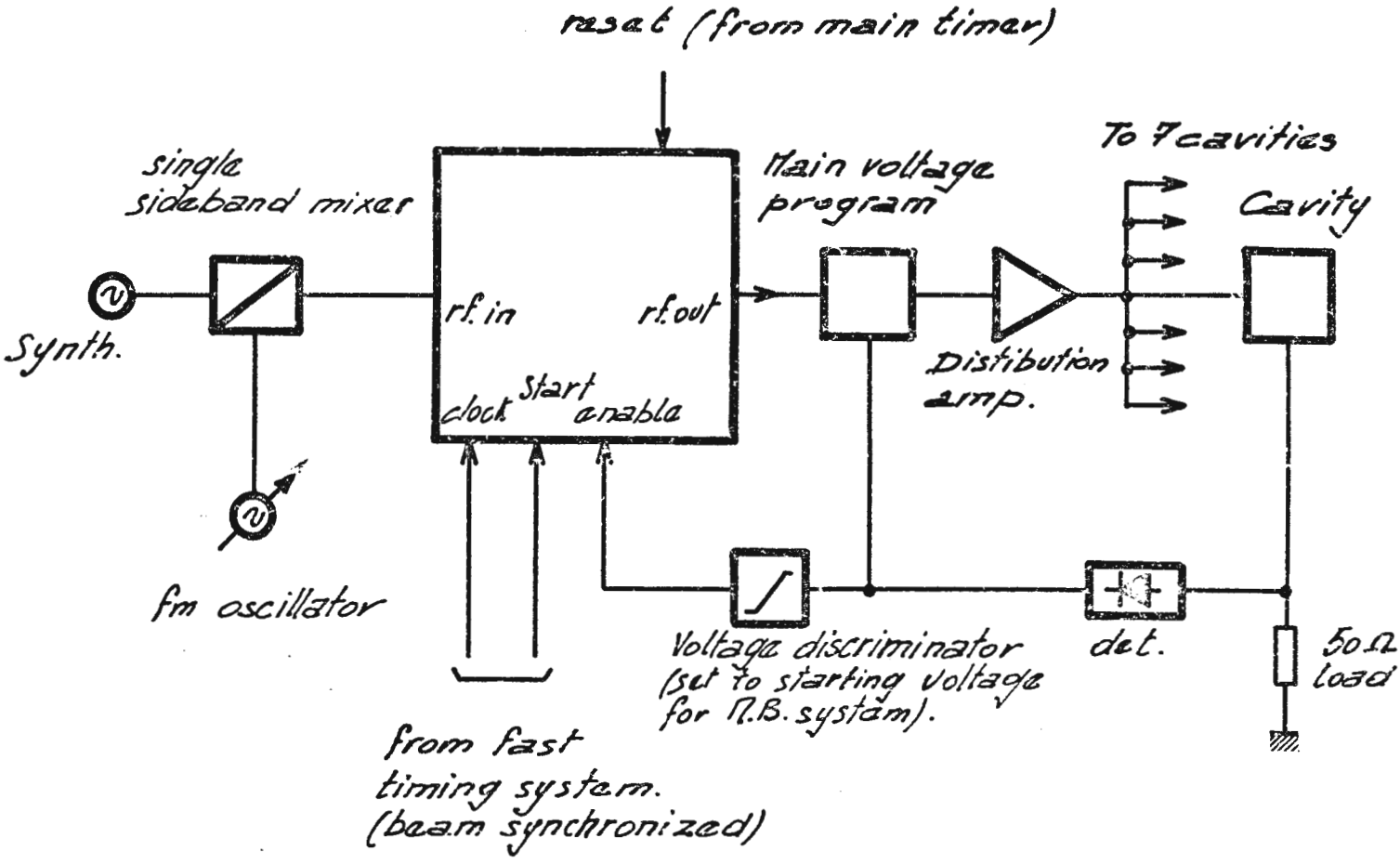


Fig. I.1: Interfacing of missing bucket system to ISR/RF system.

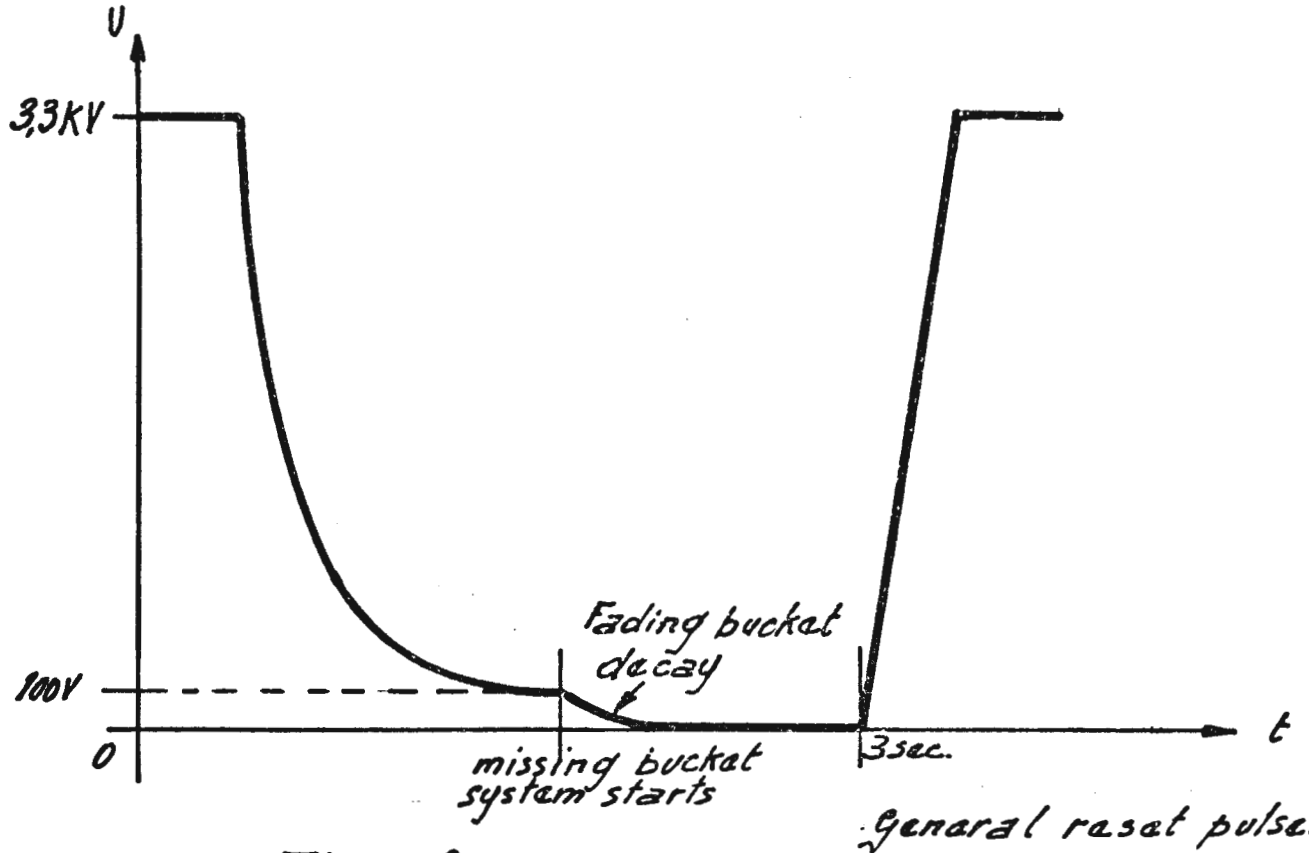


Fig. I.2: The rf accelerating voltage cycle.

switched in) takes over the amplitude modulation of the r.f. accelerating signal.

The counters are driven via 2 by a clock signal derived also from the beam phase-lock equipment. This clock drives all the other bunch-synchronized counters in the RF system.

At the end of the accelerating cycle, the "general reset" pulse generated by the ISR-RF master timer (not synchronized to the beam) stops and resets the counters and the fading-bucket circuitry, resets the enabling gate referred to above and sets the fast r.f. switch to Channel A. The system is now in the rest state and ready for the next accelerating cycle.

Provision has also been made for by-passing the r.f. portion of the missing-bucket system by means of two r.f. relays.

I.2 Construction and location of equipment and remote-control facilities

As mentioned earlier in the test, the missing-bucket system is built up out of NIM plug-in chassis modules.

The modules are fitted into three NIM 19" rack-style bins, with power supply units mounted on the back of the bin. (See Fig. I.3).

The two systems are located in the auxiliary buildings A1 and A8, close to the ISR tunnel. Remote control heads installed in the main ISR control room provide thumbwheel switch control of fading-bucket time constant, and cut-off time and cut-off disabling.

These controls are repeated on the front panel of the voltage program module.

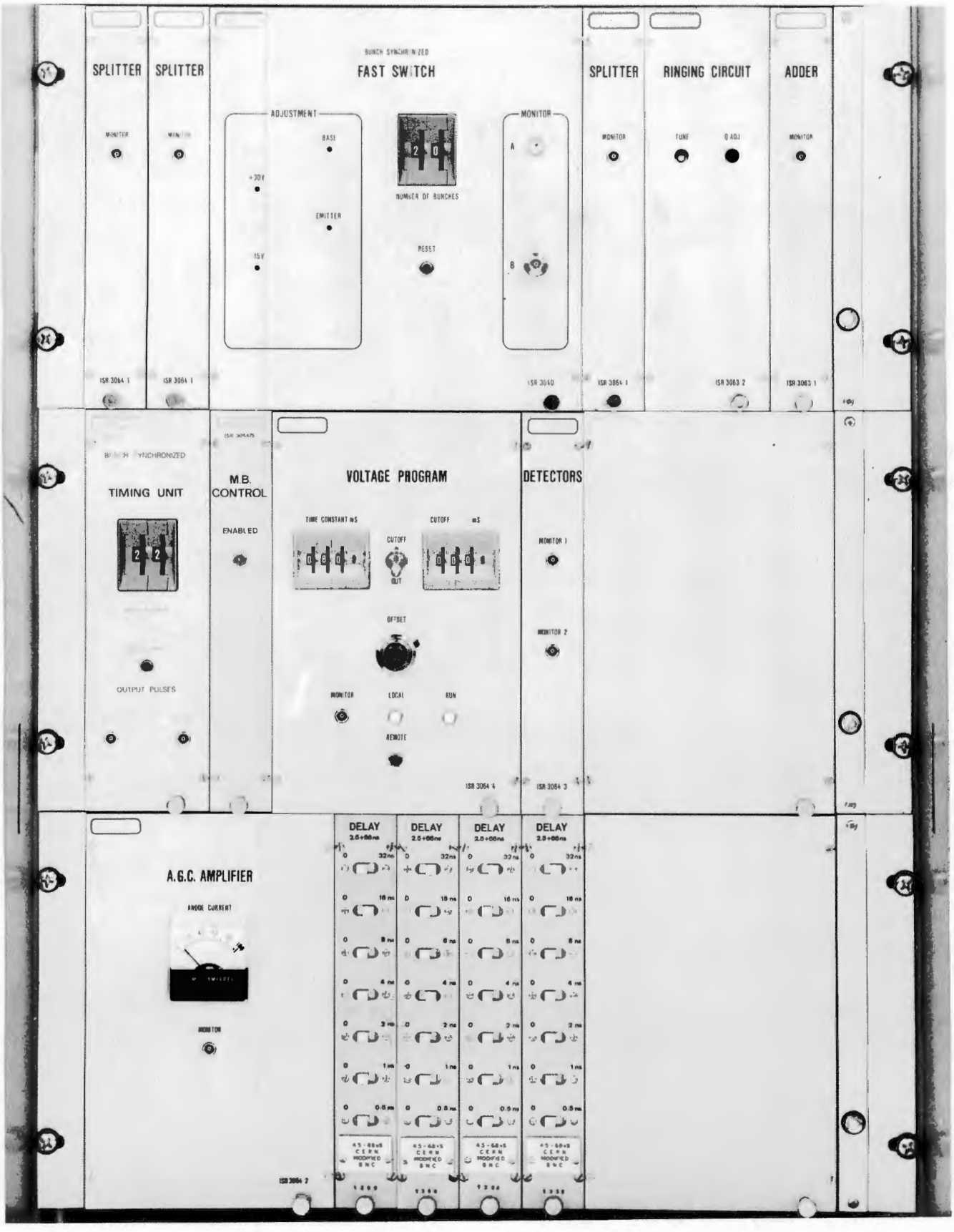


Fig. I.3 Front view of missing-bucket system

Local control only is provided for the settings of counters CN1 and CN2. It is thought most unlikely that anyone might wish to change the number of buckets suppressed in the course of an experiment with the machine.

Circuit diagrams of all system components are given in Appendix IV.

APPENDIX II

The relationship between r.f. gap voltage, input voltage and a spurious voltage source inside the feedback loop in the cavity amplifier chain.

The amplifier chain may conveniently be represented by the following equivalent circuit :

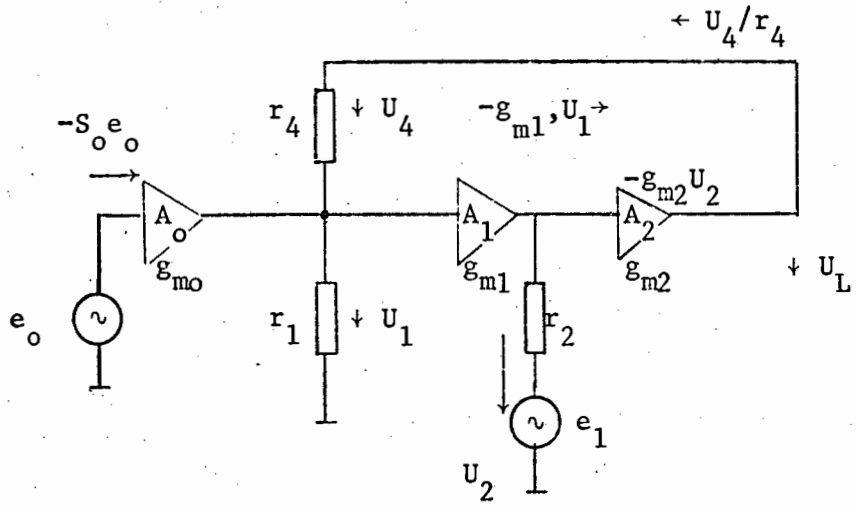


Fig. II.1

where e_o = input voltage to pre-amp.

e_1 = spurious voltage

U_L = gap voltage

$\frac{r_4}{r_1}$ = feedback ratio B

A_o ... preamplifier gain

A_1 ... intermediate amplifier (gain $g_{m1}\ r_2$)

A_3 ... P.A. driver

We wish to establish: 1. The ratio e_o/e_1 for $U_L = 0$

2. The ratio U_L/e_1 for $e_o = 0$

We have

$$-g_{mo}\, e_o + \frac{U_4}{r_4} = \frac{U_1}{r_1} \qquad \ldots \text{II.1}$$

$$U_L = U_4 + U_1 \qquad \ldots \text{II.2}$$

$$-g_{m2}\, U_2 = \frac{U_4}{R_4} \qquad \ldots \text{II.3}$$

$$U_2 = (-g_{m1} U_1) r_2 + e_1 \qquad \ldots \text{II.4}$$

1. To obtain e_o as function of e_1 when $U_L = 0$

We have from $$U_4 = - g_{m2}\, U_2\, r_4 \qquad \ldots \text{II5A}$$

$$U_L = - g_{m2}\, U_2\, r_4 + U_1 \qquad \ldots \text{II.5B}$$

$$-g_{mo}\, e_o - g_{m2}\, U_2 = \frac{U_1}{r_1} \qquad \ldots \text{II.6}$$

from which $$U_L = - g_{m2}\, r_4 \left[-g_{m1}\, U_1\, r_2 + e_1\right] + U_1 \qquad \ldots \text{II.7}$$

and $$- g_{mo}\, e_o\, r_1 - g_{m2}\, r_1 \left[-g_{m1}\, U_1\, r_2 + e_1\right] = V_1$$

$$\ldots \text{II.8}$$

i.e. $$U_1 = \frac{g_{mo} e_o r_1 + g_{m2} e_1 r_1}{g_{m2} r_1\, g_{m1} r_2 - 1} \qquad \ldots \text{II.9}$$

By equating U_L to 0 we obtain, from Eq. II.7

$$U_L = 0 = g_{m2} r_4 g_{m2} r_2 \left[\frac{g_{mo} r_1 e_o + g_{m2} r_1 e_1}{g_{m2} r_1 g_{m1} r_2 - 1}\right] - g_{m2} r_4 e_1 + \left[\frac{g_{mo} e_o r_1 + g_{m2} r_1 e_1}{g_{m2} r_1\, g_{m1} r_2 - 1}\right]$$

i.e. $$g_{mo} e_o r_1\, (g_{m2} r_4 g_{m1} r_2 + 1) - g_{m2} r_4 e_1\, (1 + \frac{r_1}{r_4}) = 0$$

$$\ldots \text{II.10}$$

Now $$g_{m2} r_4 >> 1 \quad \text{and} \quad \frac{r_1}{r_4} << 1$$

so $$g_{m2} r_4 \; g_{mo} e_o r_1 \; g_{m2} r_2 \simeq -e_1 g_{m2} r_4$$

i.e. $$\left.\frac{e_1}{e_o}\right]_{U_L = 0} \simeq -g_{mo} \, r_1 \, g_{m1} \, r_2 \qquad \text{...II.11}$$

This gives the ratio of the internally generated spurious e_1 to a known measurable e_o for $U_L = 0$.

The value of e_1 established by Eq. II.11 enables us to find the output voltage U_L for a known value of e_1 by assuming $e_o = 0$.

To obtain U_L as function of e_1, for $e_o = 0$, place $-g_{mo} e_o = 0$ in II.1

So $$\frac{U_4}{r_4} = \frac{U_1}{r_1} \qquad \text{II.12}$$

From II.12 and II.2, we obtain $U_L = U_1 \left(1 + \frac{r_4}{r_1}\right)$ II.13

also $$-g_{m2} U_2 = \frac{U_1}{r_1} \qquad \text{II.14}$$

So $$U_1 = -g_{m2} r_1 \left(-g_{m1} U_1 r_2 + e_1\right)$$

$$= \frac{g_{m2} \, r_1 \, e_1}{g_{m2} \, r_1 \, g_{m1} \, r_2 - 1} \qquad \text{II.15}$$

Now, from II.15 and II.13

$$U_L = \frac{g_{m2} \, r_1 \, e_1}{g_{m2} \, r_1 \, g_{m1} \, r_2 - 1} \left(1 + \frac{r_4}{r_1}\right) \qquad \text{...II.16}$$

For $\frac{r_4}{r_1} >> 1 \qquad g_{m2}\, r_1\, g_{m1}\, r_2 >> 1$

$$\frac{U_L}{e_1} \cong \frac{r_4}{r_1} \cdot \frac{1}{g_m r_2}$$

i.e.

$$\left[\frac{U_L}{e_1}\right]_{e_o} = \frac{B}{A_1} \qquad \text{... II.17}$$

where B = feedback ratio

A1 = gain of intermediate amplifier.

Both II.11 and II.17 are linear, time-independent relations.

In the example of our system

g_{mo} = 60mA/V $\qquad$ g_{m1} = 55mA/V $\qquad$ r_1 = 160Ω $\qquad$ r_2 = 330Ω

so

$$\frac{e_1}{e_o} = -174 \qquad \text{for } U_L = 0$$

$$\frac{U_L}{e_1} = 3{,}9 \qquad \text{for } e_o = 0$$

Steady-state gain

$$\frac{U_L}{e_o} = 70 \qquad \text{for } e_1 = 0$$

So the ratio n = $\frac{\text{peak initial compensating voltage}}{\text{peak steady-state input voltage}}$

is given by

$$n = \frac{\left[\frac{e_1}{e_o}\right]_{U_L = 0} \times \left[\frac{U_L}{e_1}\right]_{e_o = 0}}{\left[\frac{U_L}{e_o}\right]_{e_1 = 0}} \qquad \text{... II.18}$$

$$= - \frac{174 \times 3,9}{70} = - 9,7$$

In practice the compensating voltage is adjusted by means of an attenuator at the ringing-circuit input, for correct compensation.

If the ringing voltage is of the form

$$e_1 = E_1 \cdot \varepsilon^{- \omega_o t/Q_o}$$

where ω_o and Q_o refer to the spurious ringing source, then a compensating voltage of the form

$$e_o = E_o \quad \varepsilon^{-\omega_o t/Q_o} = \frac{-E'_o}{n} \quad ^{-\omega_o t/Q_o} \qquad \text{...II.18}$$

will cancel out the spurious ringing voltage exactly.

Here E'_o = initial peak (steady-state) drive voltage.

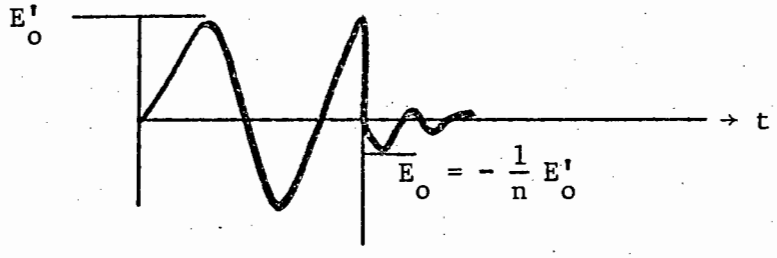


Fig. II.2

$t = t_o$.

Q_o = Q of ringing circuit = Q of spurious ringing source e_1.

As there are several low-Q resonant circuits in the cavity amplifier chain, it is rather difficult to isolate one single source e_1 of known Q. The equivalent Q was therefore determined by measurement, using a keyed sinusoidal drive signal.

From Fig. 4.2 we see that the amplitude of e_1 decays to $\frac{1}{\varepsilon} \cdot E_1$ in approximately ½ cycle. This gives

$$Q_o = \tfrac{1}{2}\pi \simeq 1,5$$

Thus the ringing circuit parameters are :

$$f_o = 9,5\text{MHz}$$

$$Q_o = 1,5$$

Attenuation $n = 9.7$

This provided a starting point for design of the compensating circuit.

APPENDIX III

Linearity and stability considerations in the control loop of the fading-bucket voltage program

III. 1 : The loop may be represented thus

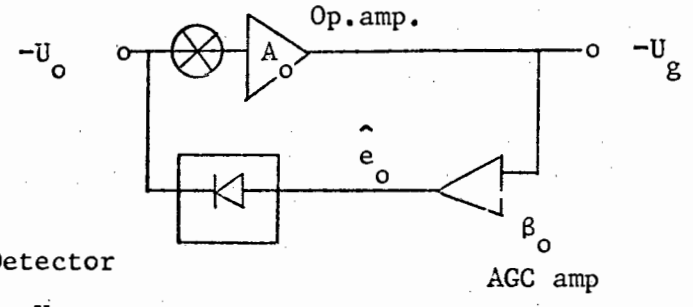


Fig. III.1

$$\frac{U_o}{\hat{e}_o} = 1$$

or more simply, by this :

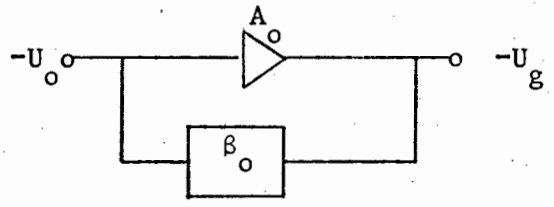


Fig. III.2

$$\beta_o = \frac{\Delta u_o}{\Delta u_g}$$

The incremental control transfer function of the AGC amplifier and detector is of the form

$$\beta_o = \frac{\Delta \hat{e}_o}{\Delta u_g} = \frac{\Delta u_o}{\Delta u_g}$$

From the slope of the transfer curve, we find that for r.f. gain A = 10 initially.

$\beta_{o1} = 1,3$ (high sensitivity end)
$\beta_{o2} = 0,00134$ (low sensitivity end)

The initial DC open-loop gain A_o is

$$A_o = 5 \times 10^5 \qquad \text{(breaking loop at } \otimes\text{)}$$

DC loop gain $A_L = \beta_o A_o$

$$A_{L1} = 5 \times 10^5 \times 1{,}3 = 6.5 \times 10^5 \qquad \text{(high-sensitivity end)}$$

$$A_{L2} = 5 \times 10^5 \times 0{,}00135 = 6{,}7 \times 10^2 \qquad \text{(low- sensitivity end)}$$

III.2 Linearity: An outside voltage is impressed on the loop via a resistive summing network.

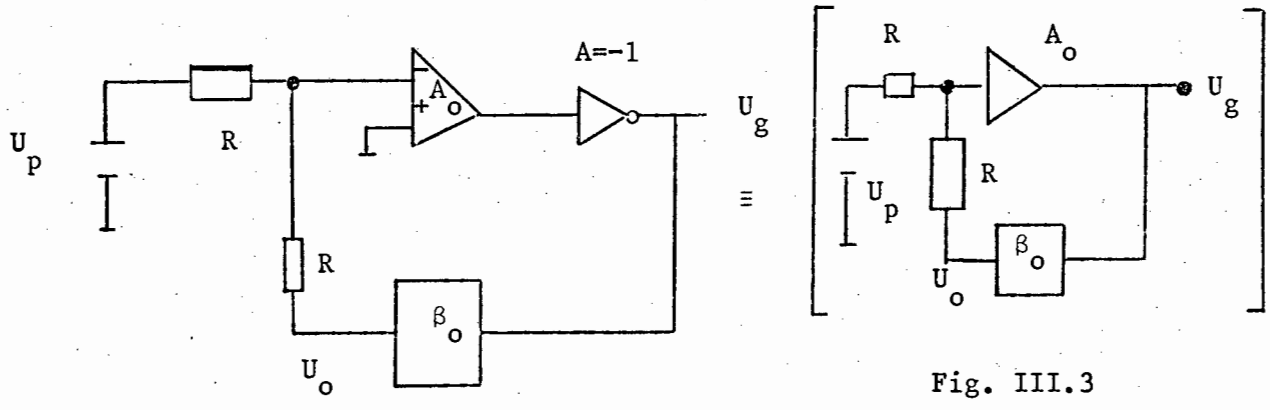


Fig. III.3

AGC amp. & det.

$$\frac{\Delta U_o}{\Delta U_p} = A_p = \frac{\beta_o A_o}{2 - \beta_o A_o} = \frac{A_L}{2 - A_L}$$

$$A_{p1} = \frac{6{,}5 \times 10^5}{2\text{-}6{,}5 \times 10^5} = -1. \qquad \text{(High sensitivity end)}$$

$$A_{p2} = \frac{670}{2 - 670} = -1{,}003 \qquad \text{(Low sensitivity end)}$$

Thus deviation from linearity is + 0,3% over whole control range.

III. 3 : Stability of loop

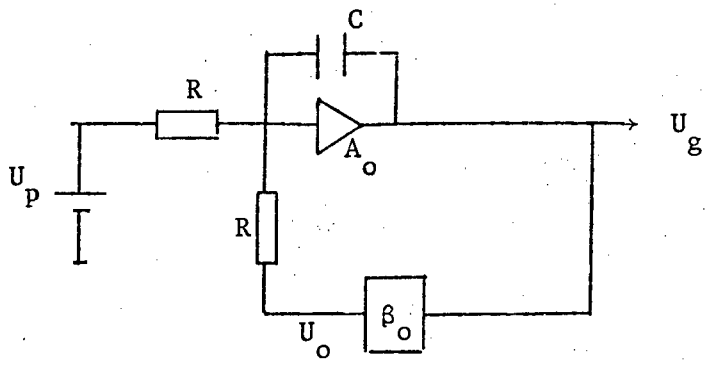


Fig. III.4

Introduce frequency dependent feed-back across opamp. such that

$$A_f = \frac{jA_o}{\omega CR}$$

Assume β_o wide band. $\tau = CR$

Condition : $\tau \geq 0.1\ \tau_{pmin}$, where τ_p = program time constant.

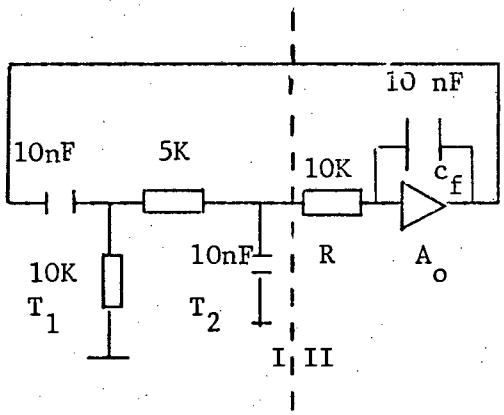


Fig. III.5

For C_f = 10 nF R = 10K

f_H = roll-off frequency for $R = 1/\omega C$ = 1,6 kHz

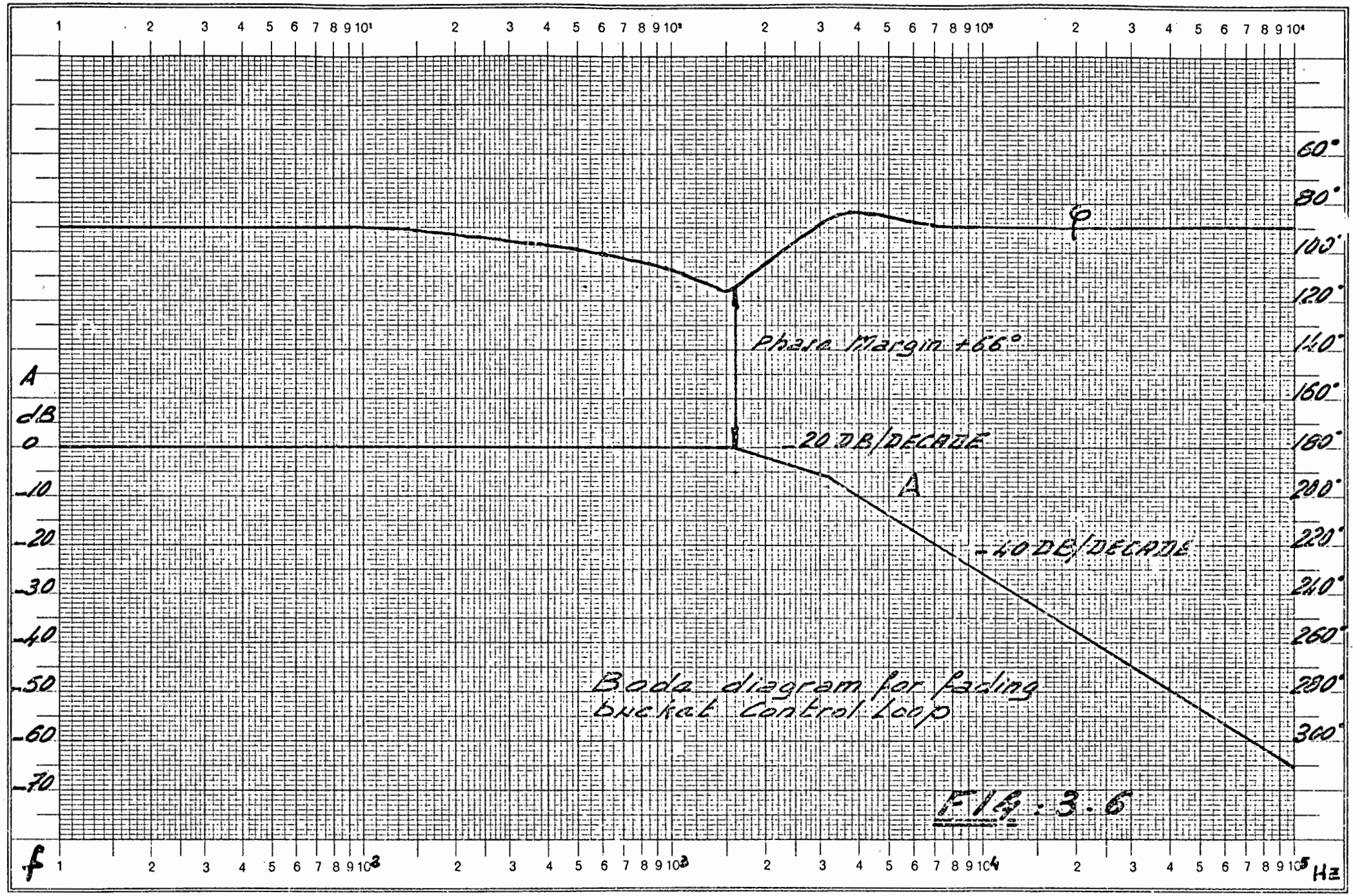
$\phi_H = -45^o$ for integrator gain $A_o = 1$ at f_H = 1,6 kHz

The effect of the R - C decoupling networks in the AGC amplifier control line may be neglected in the frequency range of interest.

The detector may be represented by I in Fig. III.5.

Here T_1 = 100 µs : f_{H1} = 1,6 kHz. T_2 = 50µs f_{H2} = 3,2 kHz.

A Bode diagram (Fig. III.6) shows that the loop is unconditionally stable. This is the case in practice.



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APPENDIX IV

Circuit Schematics of Units

Fig.	IV	1.	Splitter (signal distributor)
	IV	2.	Adder (summing amplifier)
	IV	3.	Bunch synchronized timing unit (CN1)
	IV	4A/B	Synchronized fast switch (CN2)
	IV	5	Ringing circuit
	IV	6	AGC amplifier
	IV	7/8	Detector and driver
	IV	9/10	Voltage programme unit
	IV	11	"MB Control" unit

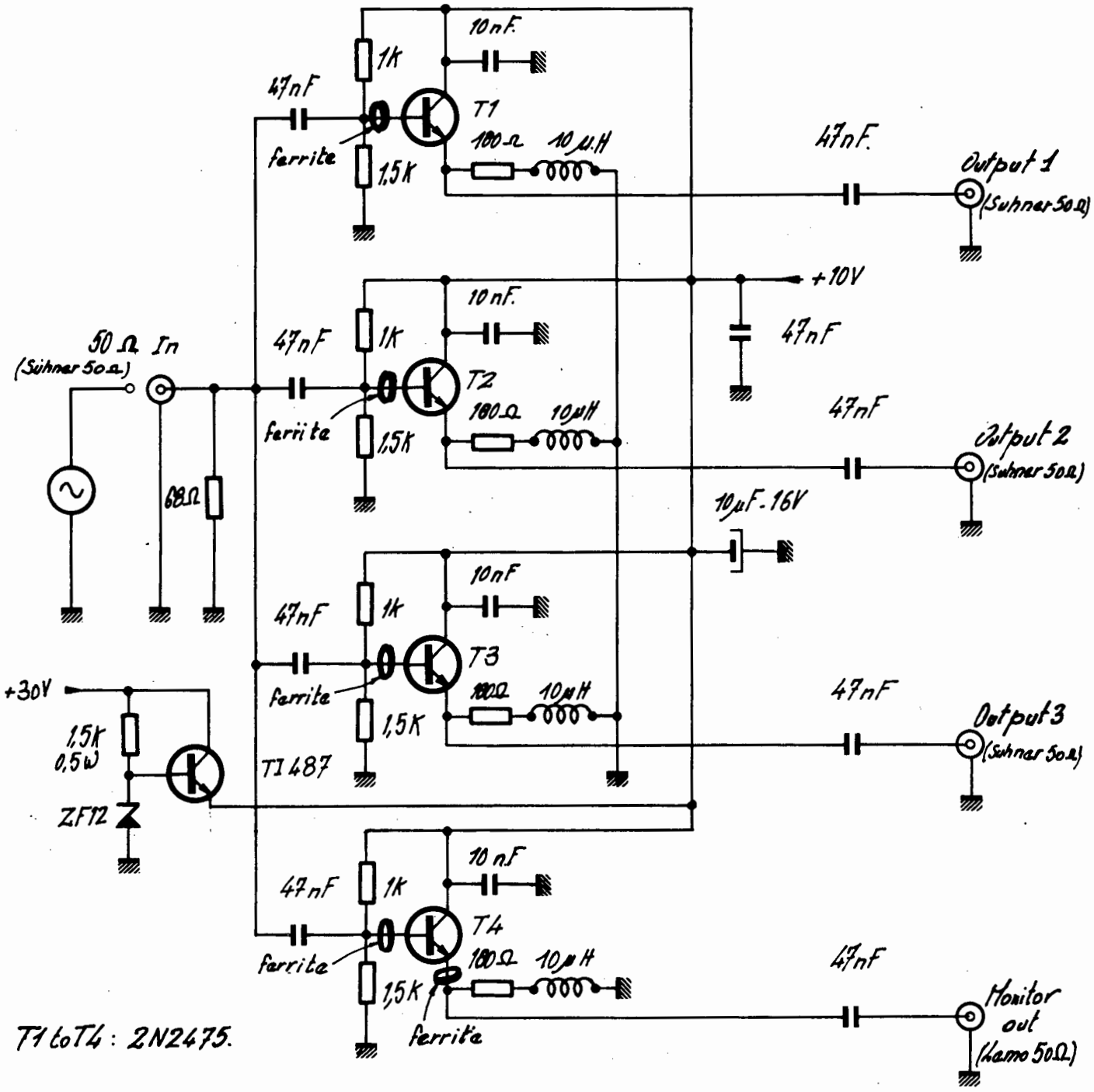


Fig.III : Splitter (ISR 3064-1)

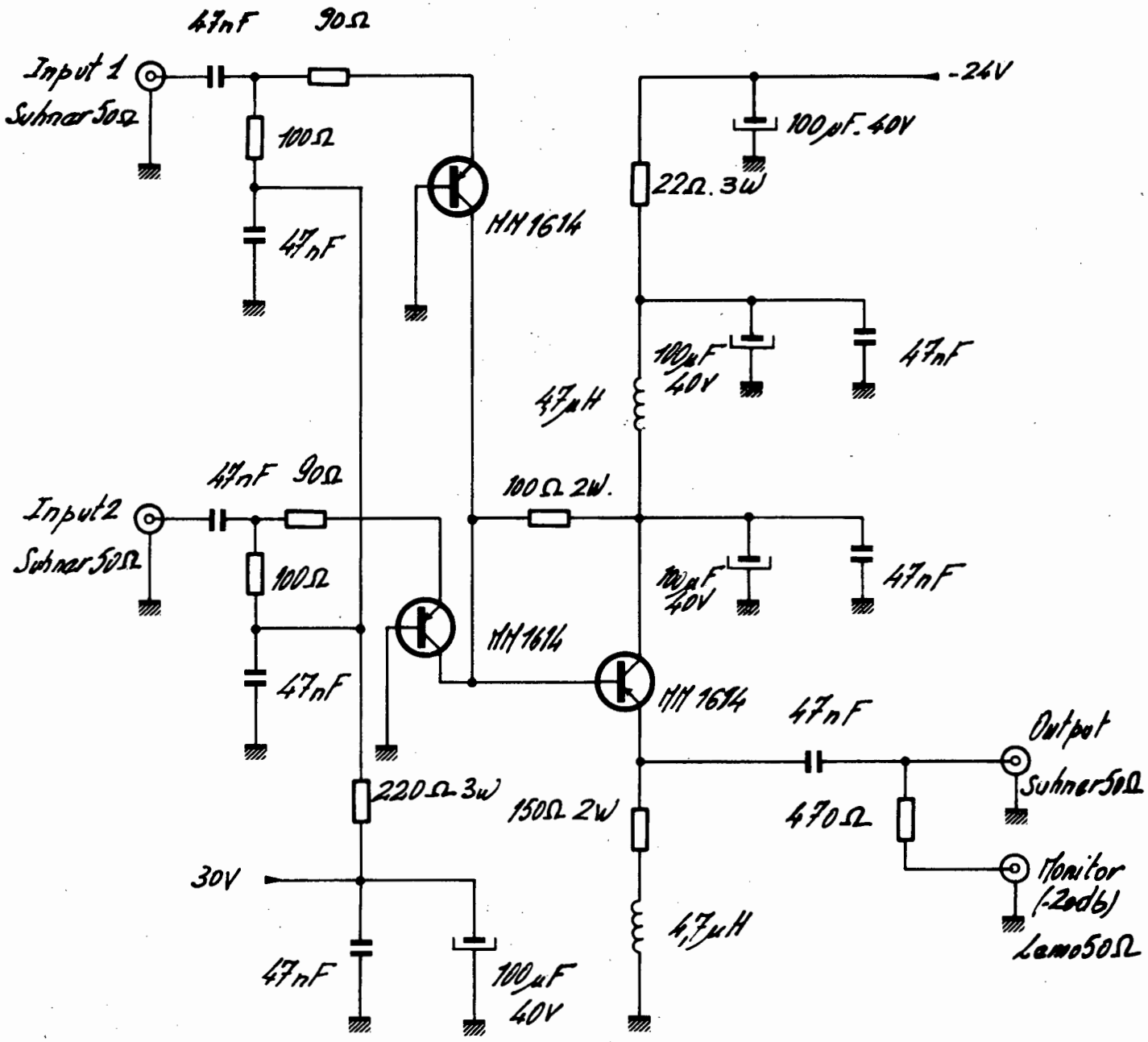
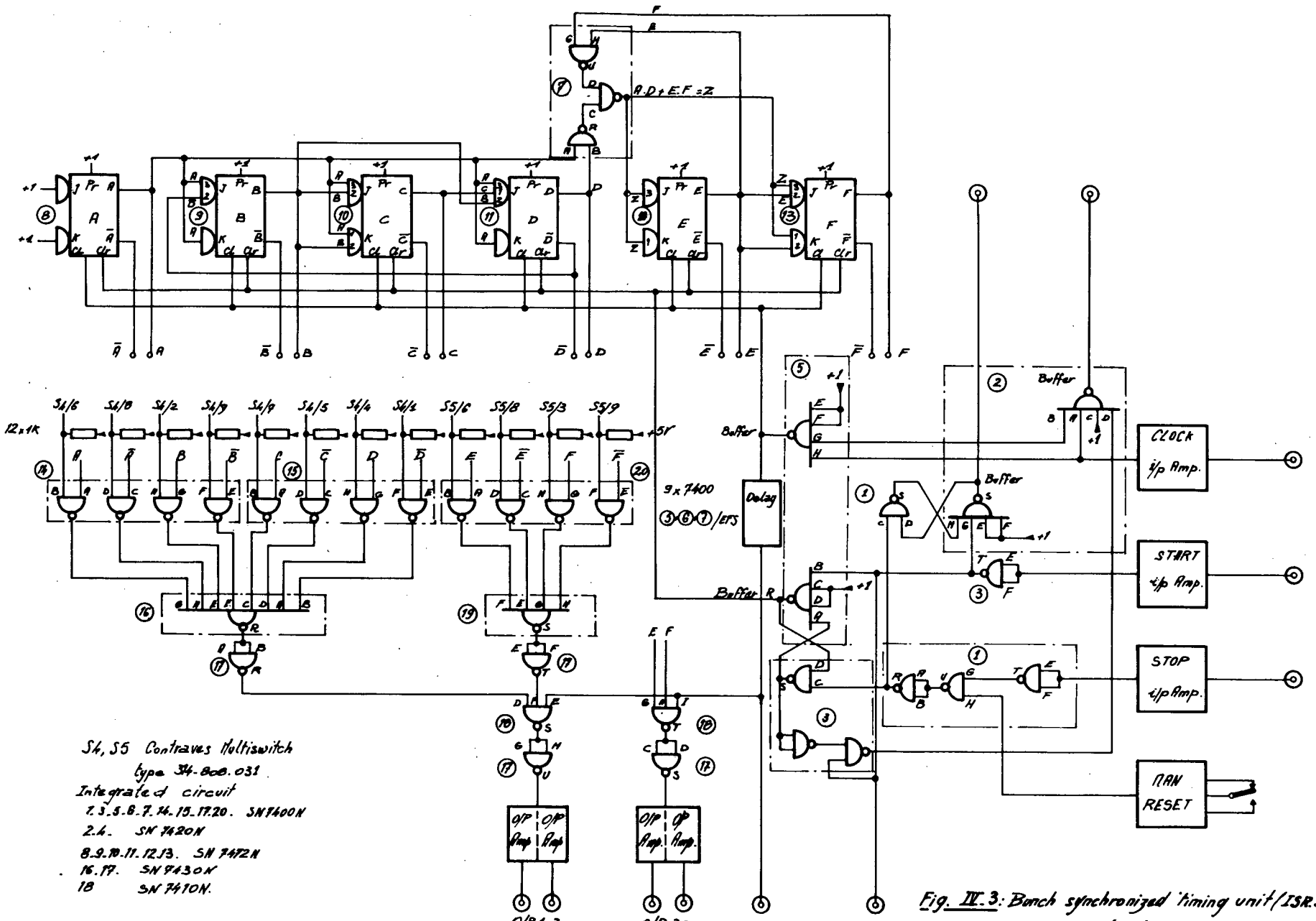


Fig IV.2: Adder (ISR.3063.1)



S4, S5 Contraves Multiswitch
type 34-808.031
Integrated circuit
1.3.5.8.7.14.15.17.20. SN7400N
2.4. SN 7420N
8.9.10.11.12.13. SN 7472N
16.17. SN 7430N
18 SN 7410N.

Fig. IV.3: Bench synchronized timing unit/ISR 3023/ (CNI)

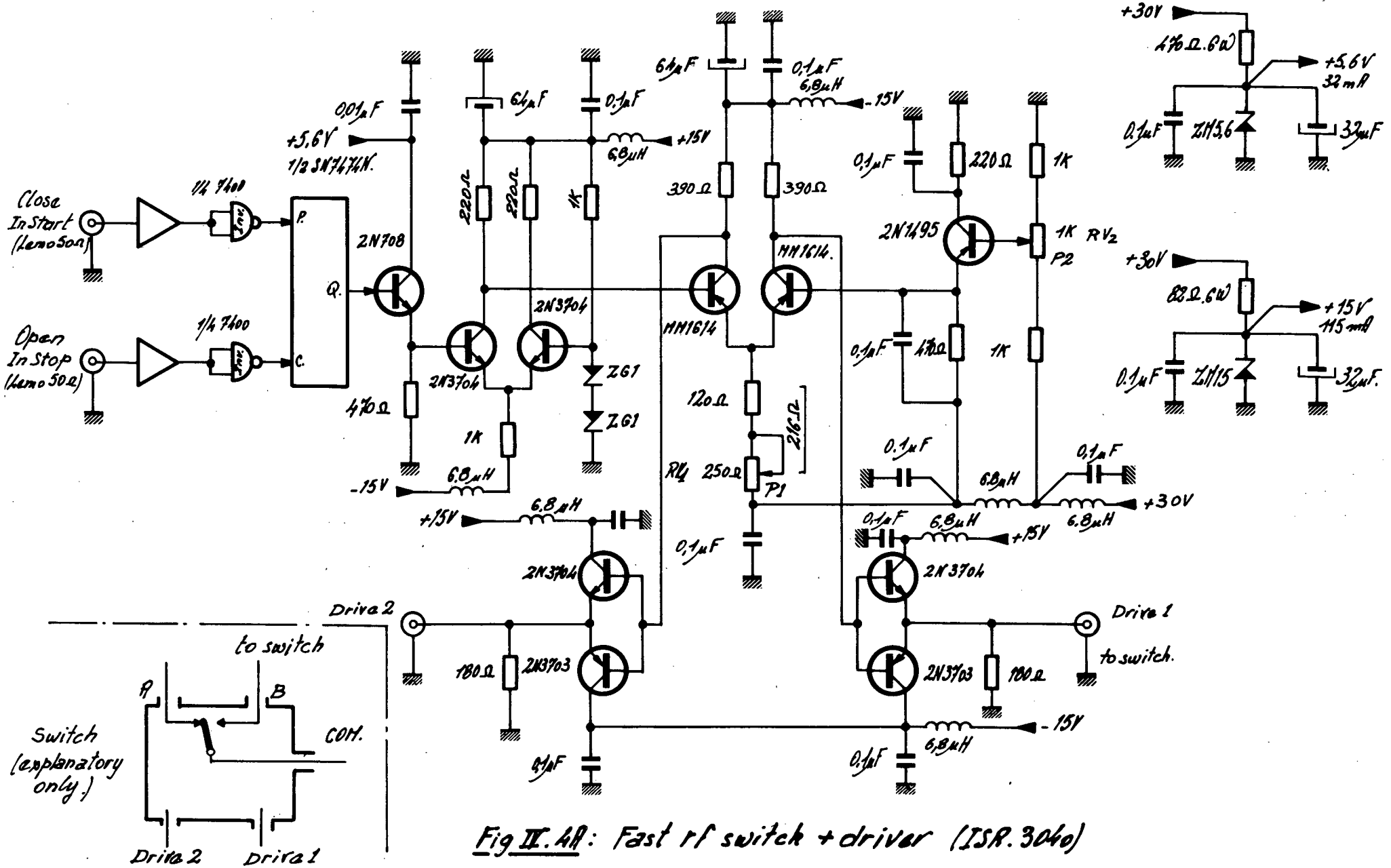


Fig II.4A: Fast rf switch + driver (ISR.30/40)

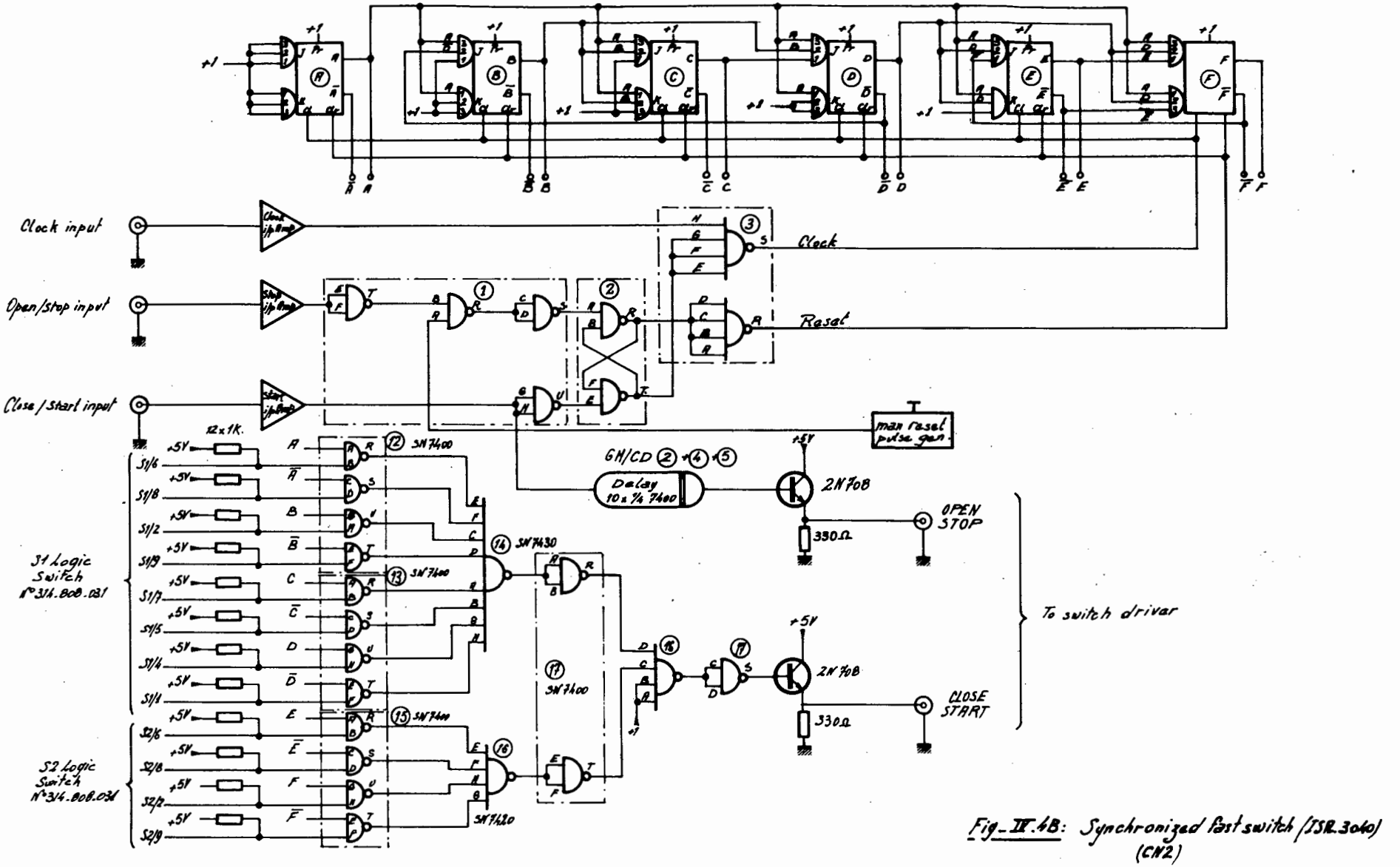


Fig. IV.4B: Synchronized fast switch (ISR.3040) (CN2)

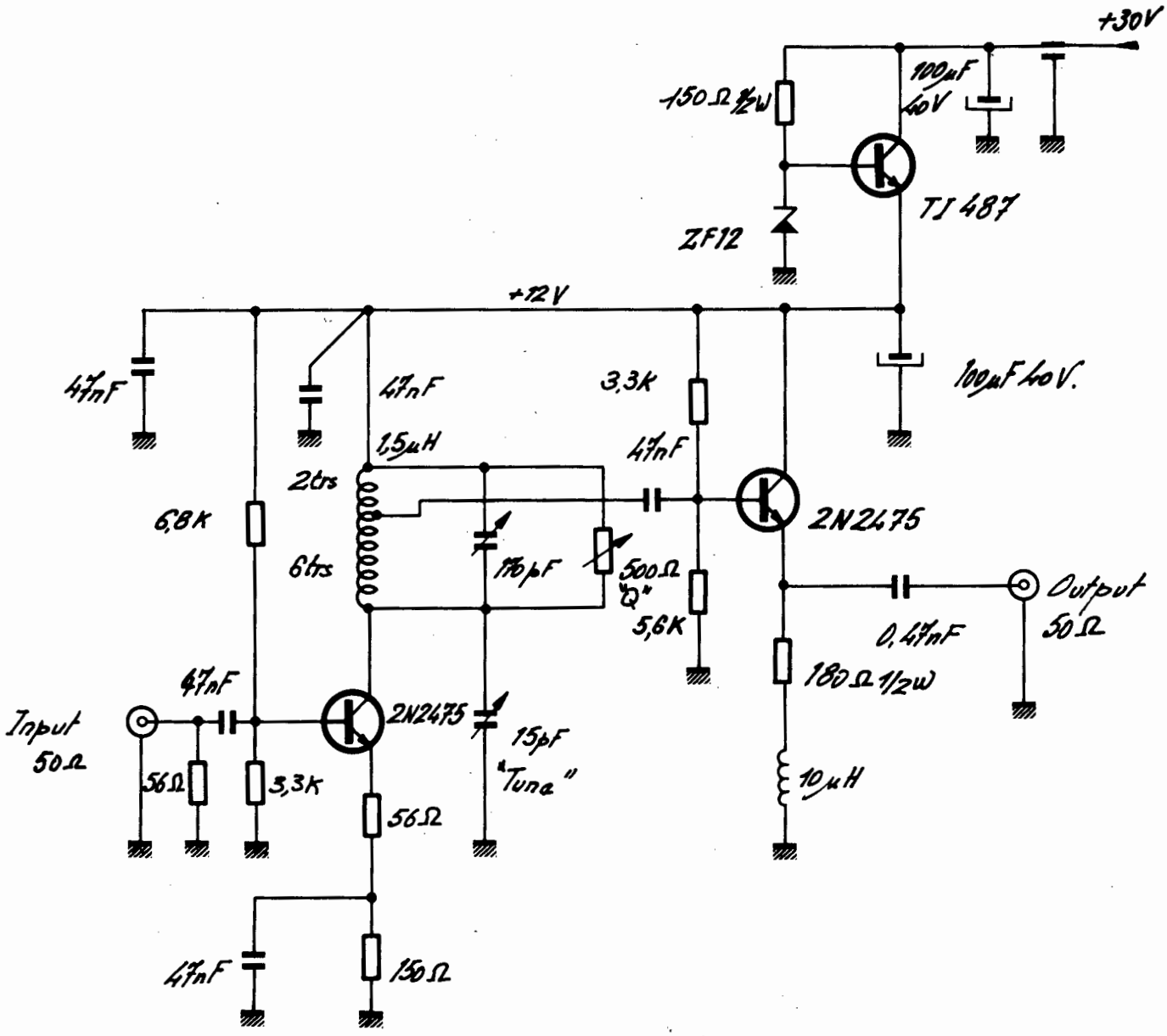


Fig. IV.5: Ringing circuit. (ISR 3063.2)

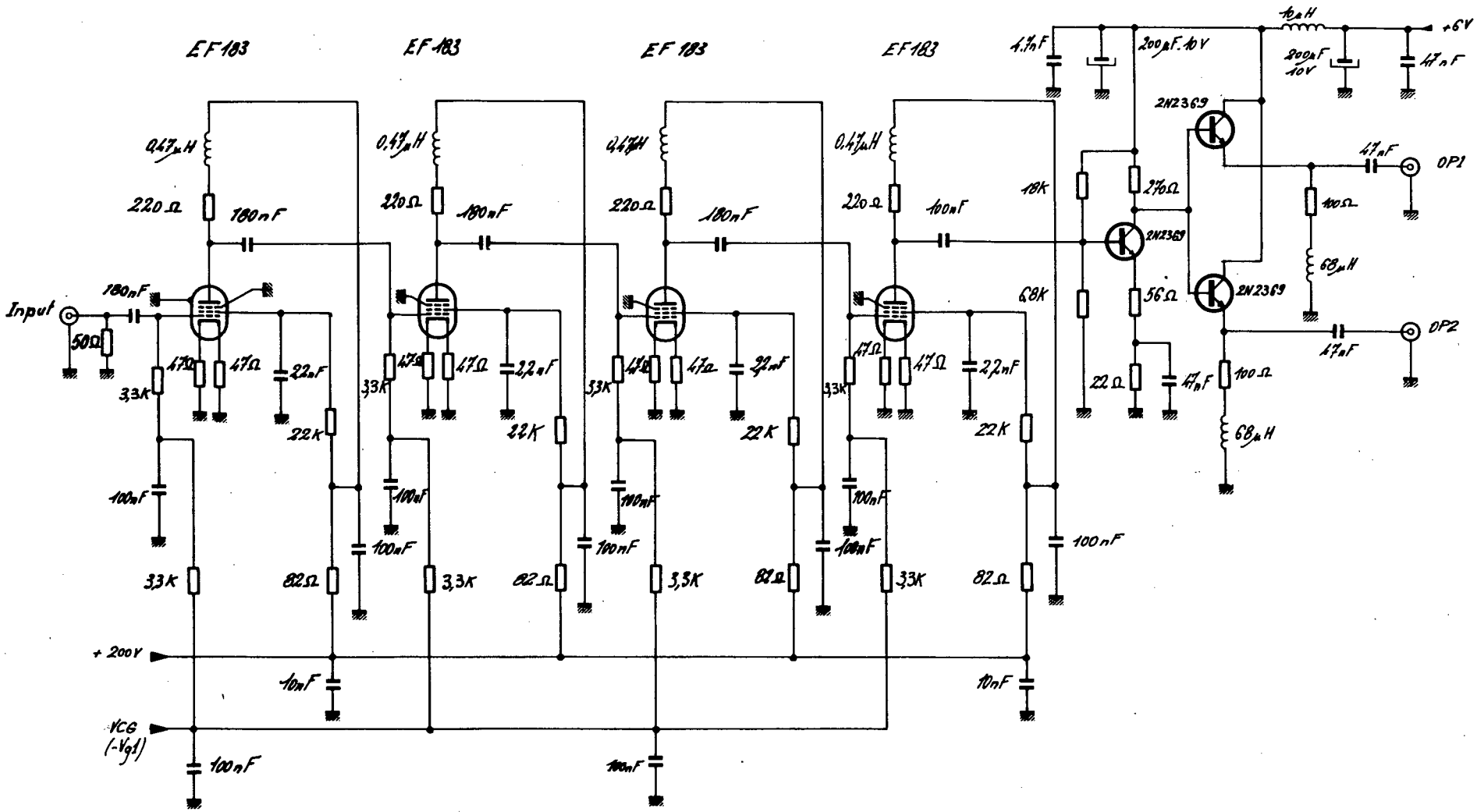


Fig. II.8: AGC Amplifier (JSR-3064-2)

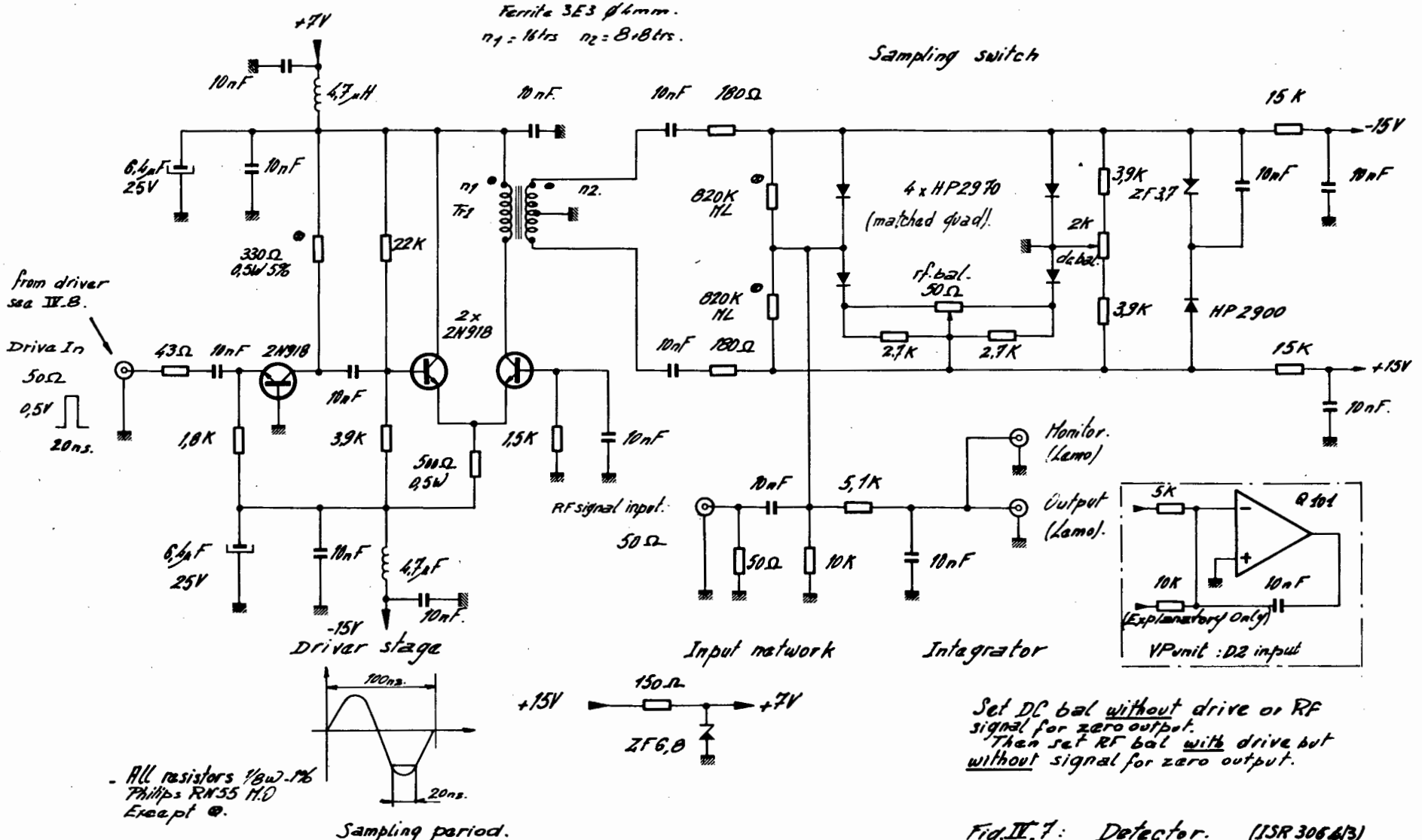
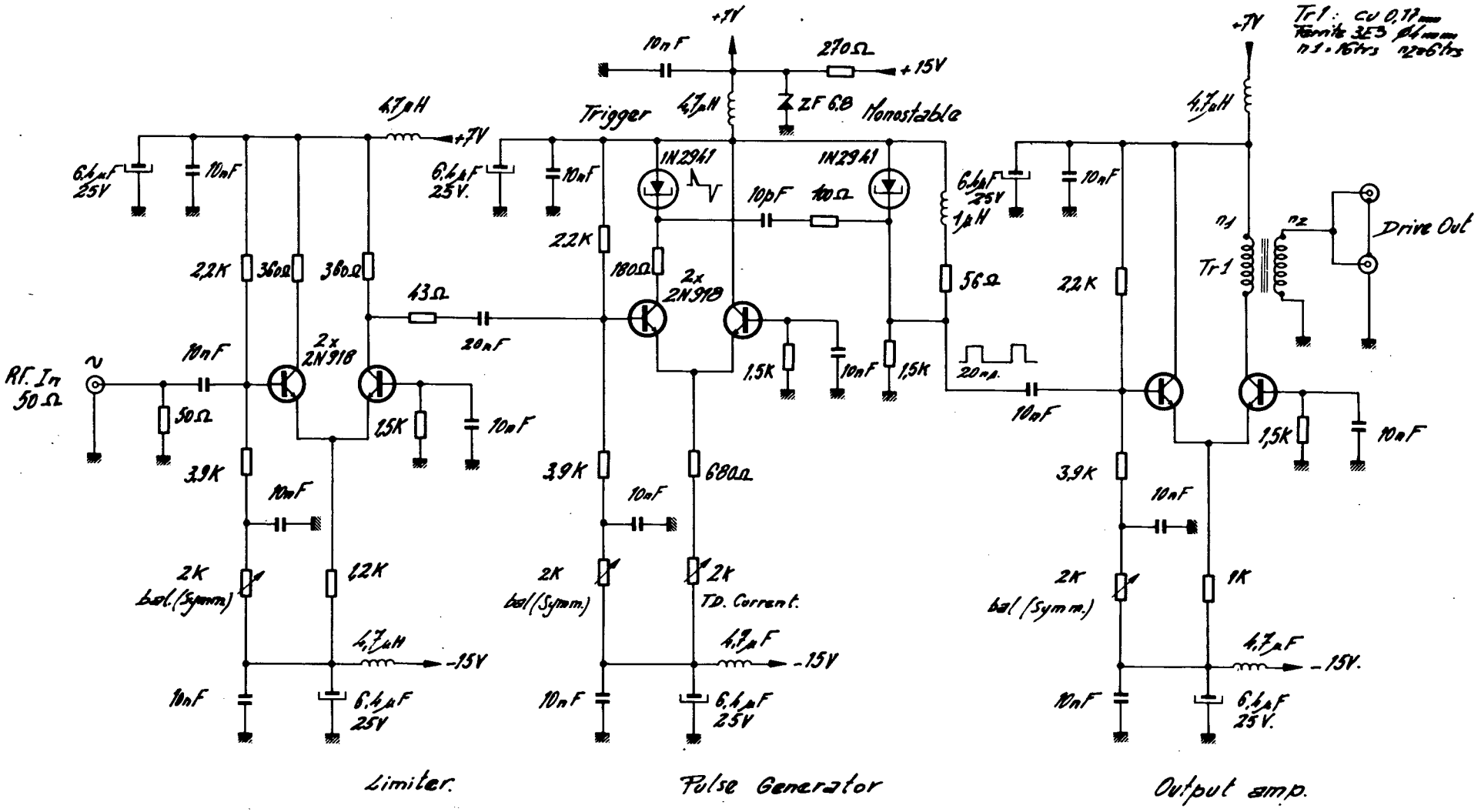


Fig.IV.7: Detector. (ISR 3064/3)



Note : Detector and detector drivers are in the same box (Detectors).

Fig. IV. 8 : Detector drivers. (ISR 3064-3)

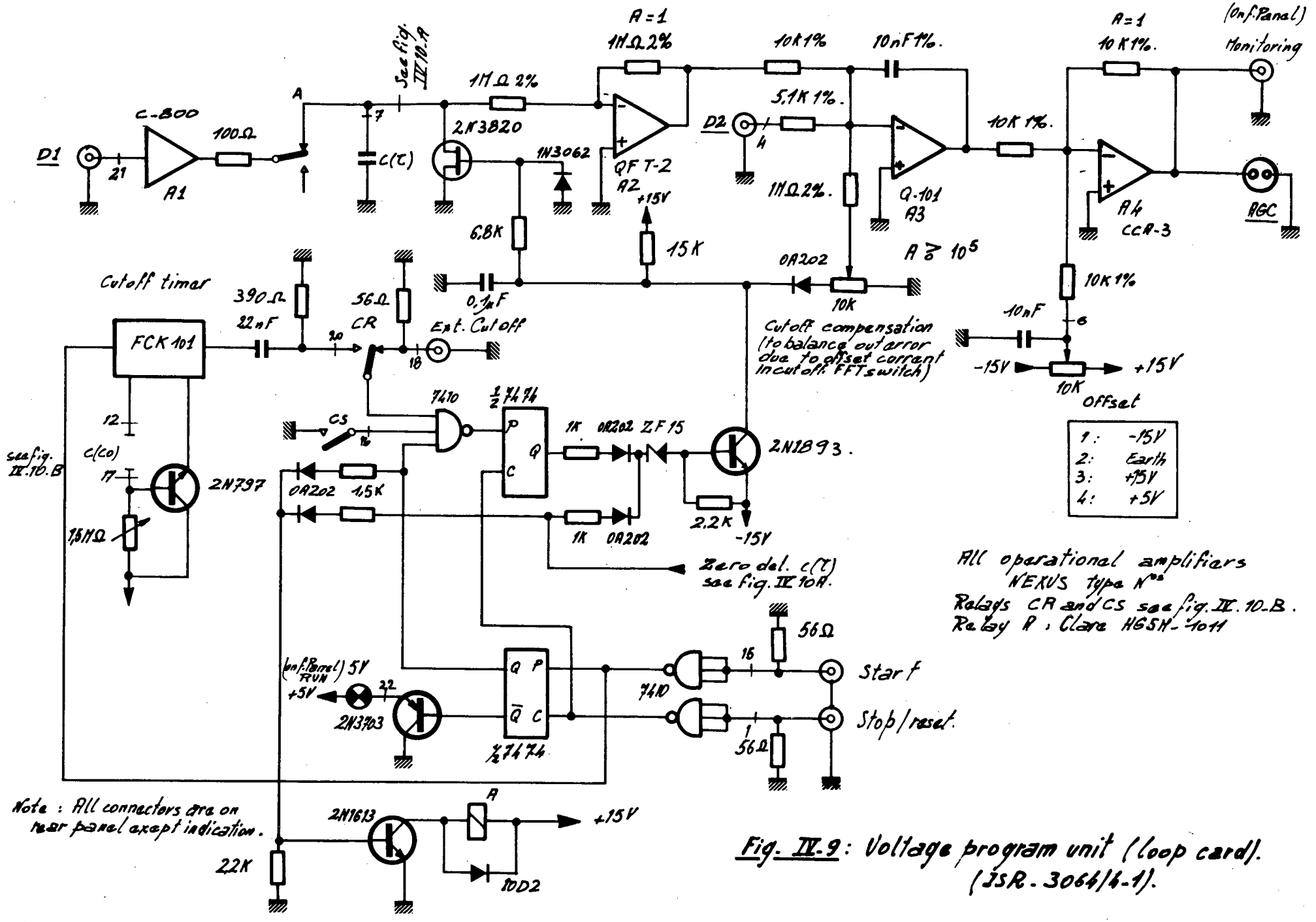


Fig. IV.9: Voltage program unit (loop card).
(JSR. 3064/4-1).

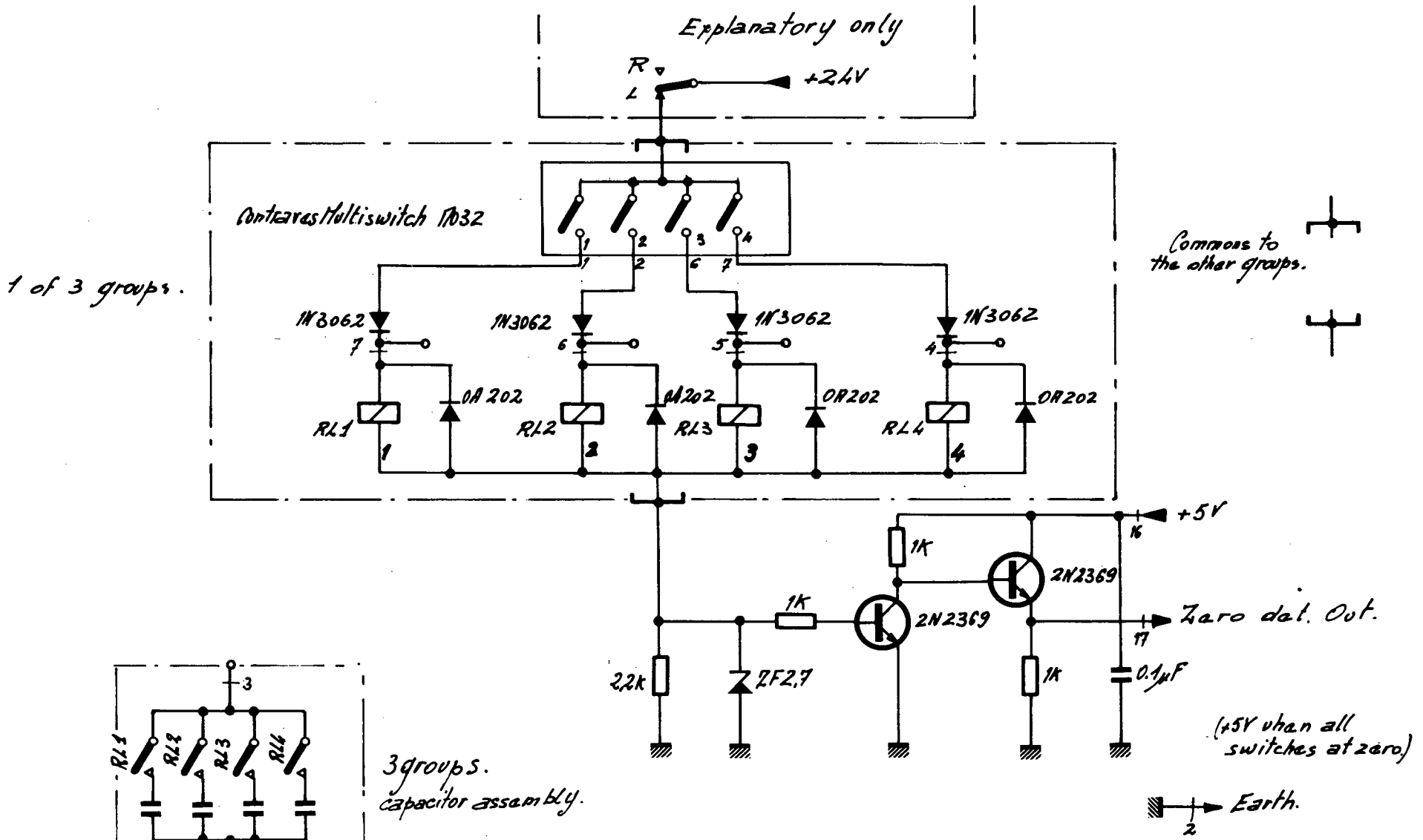


Fig. IV.10R: Voltage program unit: capacitor selector c(t) card. (ISR. 3064/4.2).

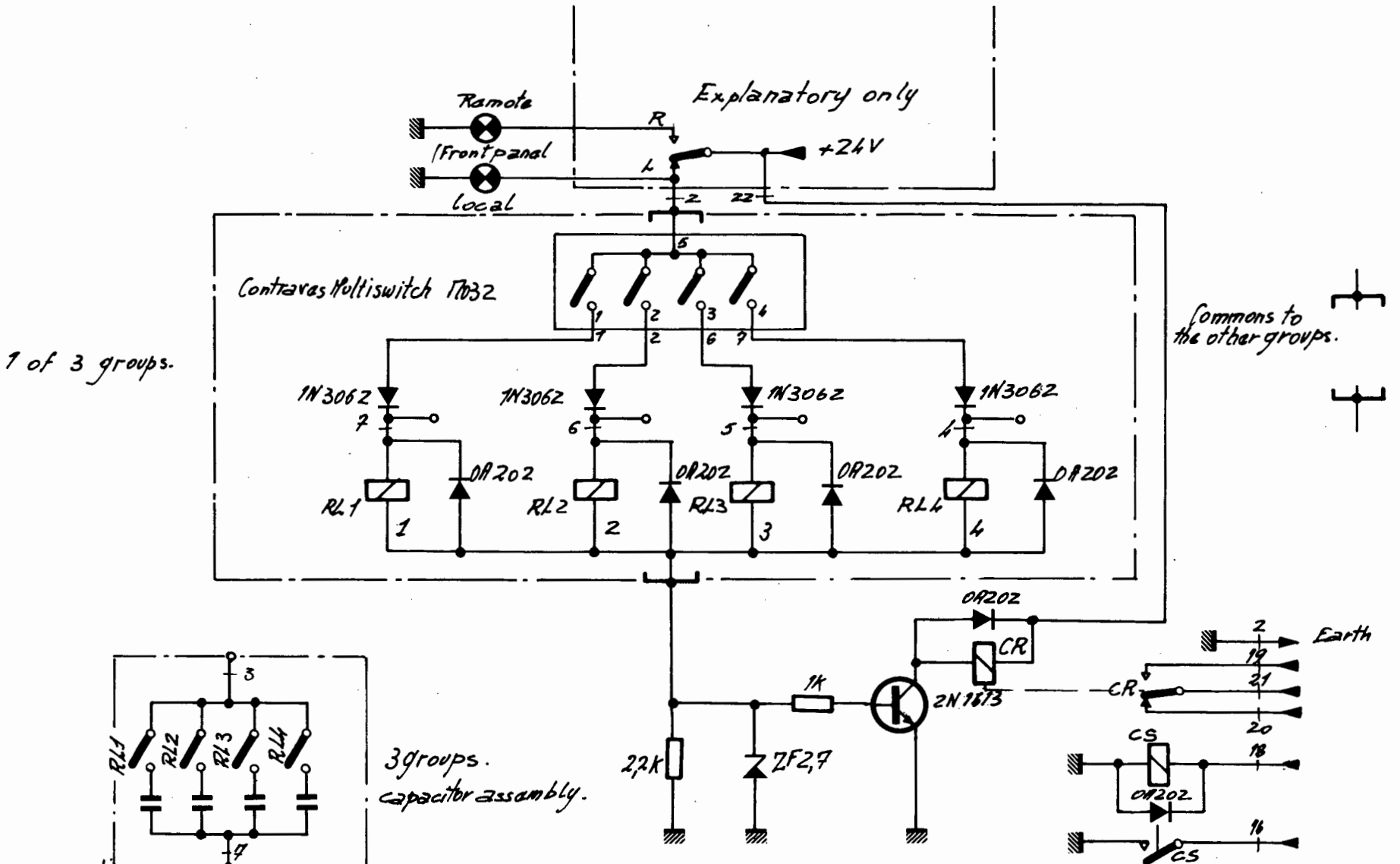
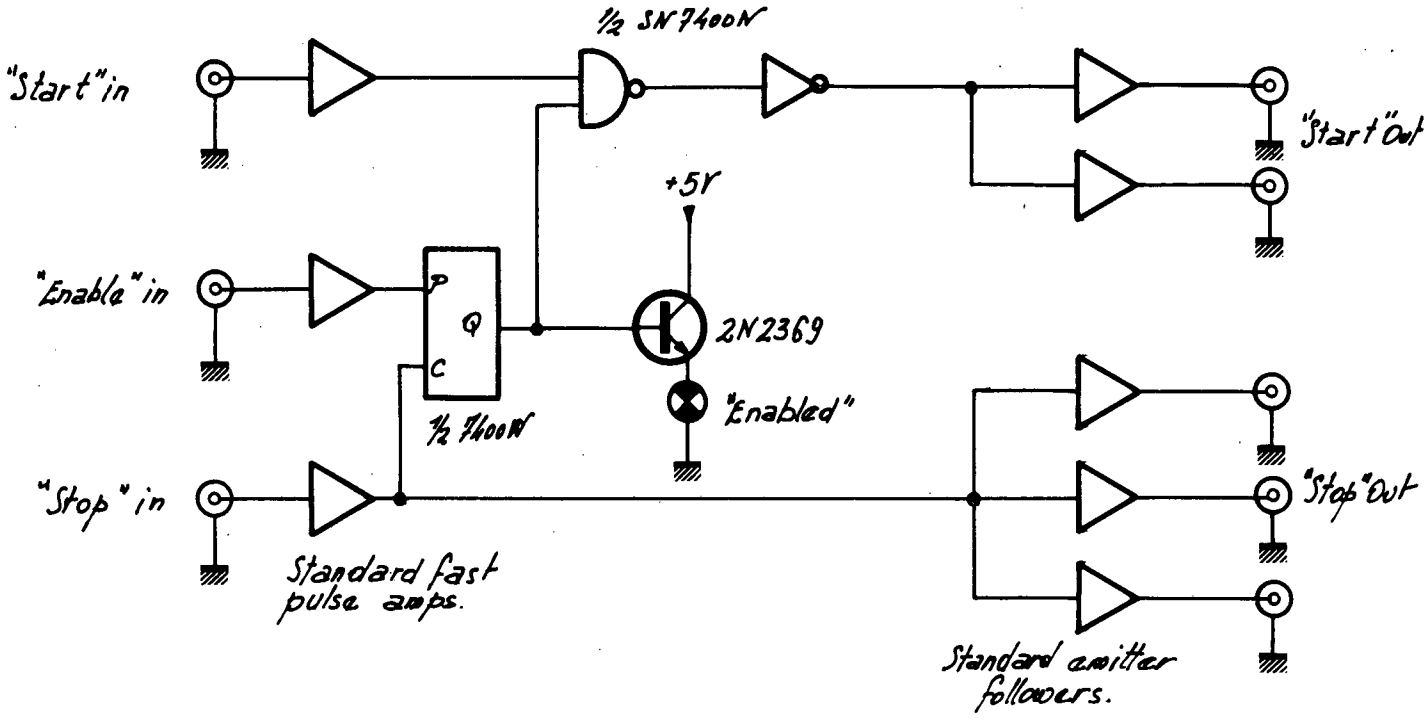
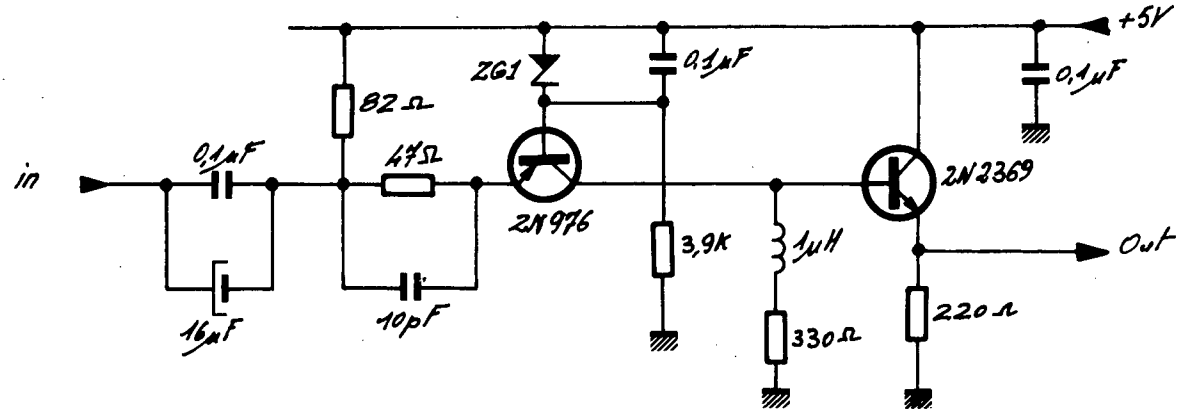
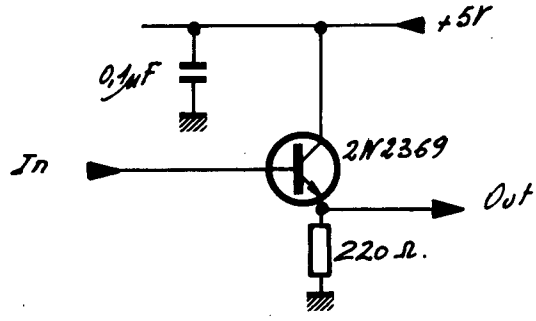


Fig. IV. 10B: Voltage program unit: capacitor selector c(co) card. (See fig. IV. 10B) (I SR. 3064/14.3)





Standard amplifier



Standard emitter follower.

Fig. IV.11: "MB Control" unit (ISR. 306615)