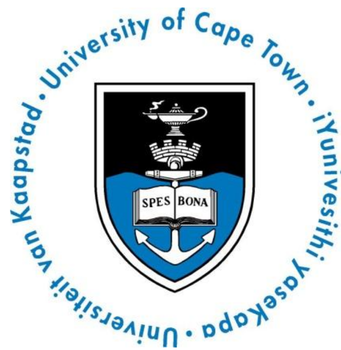
Investigating the Optical Link Performance of the End-of-Substructure Card and Susceptibility to SEUs



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Abstract

Particle physics experiments carried out by CERN attempt to investigate the fundamental forces of matter. One of these experiments is the ATLAS experiment, which studies the proton-proton collisions in the LHC. A series of upgrades are planned to increase the luminosity by a factor of five, leading to the high-luminosity LHC (HL-LHC). This upgrade will increase the potential for new discoveries but brings with it design challenges in relation to the harsh radiation environment and significant data throughput required. The ATLAS experiment is building a new detector to cope with these challenges, titled the Inner Tracker (ITk). A crucial part of this new detector is the End-of-Substructure (EoS) card, which constitutes the interface between the on-detector electronics and the off-detector systems. In addition to the operational challenges, the HL-LHC does not allow for repairs or replacing of EoS cards once operation commences, emphasizing the need for thorough testing and qualification of this component.

This thesis focuses on characterizing the performance of the EoS card in the presence of radiation, under non-ideal operating conditions and the impact of optical link parameters. The first set of tests is centered on qualifying the radiation tolerance of the EoS card. The radiation environment within the ITk poses a threat to the stable operation of electronics as energetic particles have the potential to cause erroneous changes in device logic, known as Single Event Upsets (SEU). The SEU susceptibility of the EoS card, with a focus on the Versatile Link Plus Transceiver (VTRx+) component, is studied by irradiating the EoS card with a neutron source with a distributed energy spectrum and a peak energy of 11MeV while performing a bit error rate (BER) test to monitor for radiation induced errors. The second set of tests deals with characterizing the impact of an irregular power supply on the EoS card's performance through simulating noise on the supply lines and monitoring the response in BER. The final set of tests investigates the impact the VTRx+ configuration parameters have on the quality of the optical signal.

These tests were carried out at the University of Cape Town (UCT) with the support of DESY, a national research institute in Germany, responsible for the production of the EoS cards. A number of new firmware, software and hardware modules were developed as part of this work in order to carry out the tests required. The most significant of which comprised a novel firmware addition allowing for the evaluation of the optical signal quality with an FPGA. This contribution is now being integrated into the quality control proceedings at DESY, to be used in assessing optical signal quality of the entire set of approximately 1552 EoS cards being produced.

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Chapter 1

Introduction

The thesis presents work qualifying the performance of a custom high-speed transceiver card under representative operational radiation conditions. The End-of-Substructure (EoS) card has been designed around specialized radiation-tolerant low power gigabit transceivers (lpGBT) and optical transceiver (VTRx+) components. The following thesis presents the work done on characterizing the operation of the EoS card in the presence of radiation, under non–ideal input power conditions and adjusted optical link configurations.

This project has been carried out in support of the engineering work going into the upcoming upgrade to CERN's LHC ATLAS experiment. This chapter begins with an overview of the work being done at the Large Hadron Collider (LHC), with a focus on the ATLAS experiment and the relevant aspects pertaining to this project. Following the exposition, the problem being investigated and the objectives of this dissertation are outlined. Leading into a summary of the methodology used, the hypothesis tested and establishing the scope and limitations.

1.1 Large Hadron Collider

There are four main experiments leading the research done at the LHC. They are the ATLAS [1], ALICE (A Large Ion Collider Experiment) [2], CMS (Compact Muon Spectrometer) [3], and LHCb (LHC beauty) [4] experiments. An illustration of the LHC and the locations of the various experiments can be found in Figure 1.1.

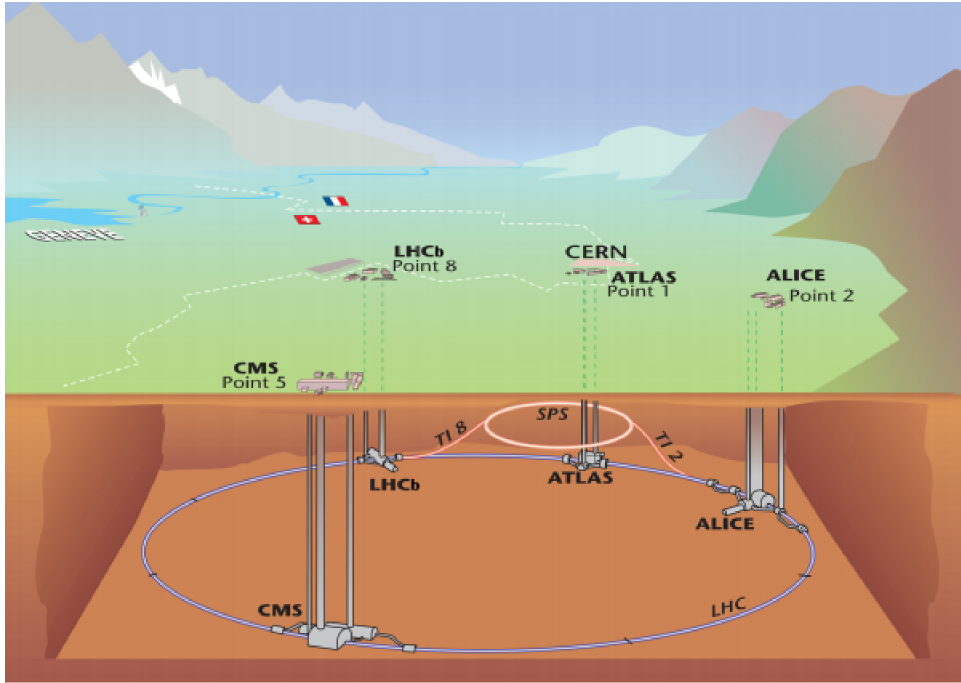


Figure 1.1: Illustration of the LHC and the four main experiments [5]

The LHC started operating in 2009 and since then a number of new discoveries have been made. One of the most notable was the discovery of the Higgs boson [6], which has helped further develop theories beyond the standard model. In the pursuit of further breakthroughs the High-Luminosity LHC (HL-LHC) is being developed as an upgrade to the LHC. Luminosity relates to the ability for a particle accelerator to produce useful interactions (events) when colliding particle beams. The beams are characterized by their intensity (number of particles) and their time dependent beam density distribution functions. The luminosity is calculated as the overlap integral of these two beams and the number of events per second is equal to the luminosity multiplied by the cross section (probability that a specific process will take place) of a particle event [7]. This upgrade intends to increase the luminosity by a factor of between 5 and 7 [8]. By increasing the number of collisions, it will be possible to study these events in more detail and increase the availability of statistics on rare events.

1.1.1 LHC Upgrade

The technology used in the LHC represented the vanguard of innovation across various disciplines at the time of its construction. As the current LHC has been operating for several years by now, numerous improvements over the original technology have been made and promote the need for an upgrade with the latest developments. This project

focuses on one of these latest technological developments, the End-of-Substructure (EoS) card and its constituent components. The EoS card acts as an interface between the on-detector electronics and off-detector systems. The development of this card and its features face unique design challenges in operating at high speeds within the harsh radioactive environment of the upcoming LHC upgrade.

The increased luminosity brings with it several design challenges. The original LHC operates at a peak luminosity of $1 \times 10^{34} cm^{-2} s^{-1}$ while the HL-LHC is planned to run at $7.5 \times 10^{34} cm^{-2} s^{-1}$. This increase corresponds to an increase in the number of events (particle collisions) from 50 per 25ns to 200 per 25ns [9]. These changes on the front-end electronics imply that they will need to withstand much higher radiation levels and accommodate significant increases in data throughput. This has led to the ATLAS collaboration deciding that an upgraded Inner Tracker (ITk) be developed to replace the current inner detector.

The ITk, depicted in Figure 1.2, consists of two detector sub-systems, the first, being closest to the beam, is the pixel detector, and the second is the strip detector. The detectors house pixel and strip sensors that are used to track the various particle collisions. The pixel sensors provide a greater resolution for detection leading to their placement being closest to the beam. However, the EoS card is only relevant to the strip detector, examined further in the next paragraph.

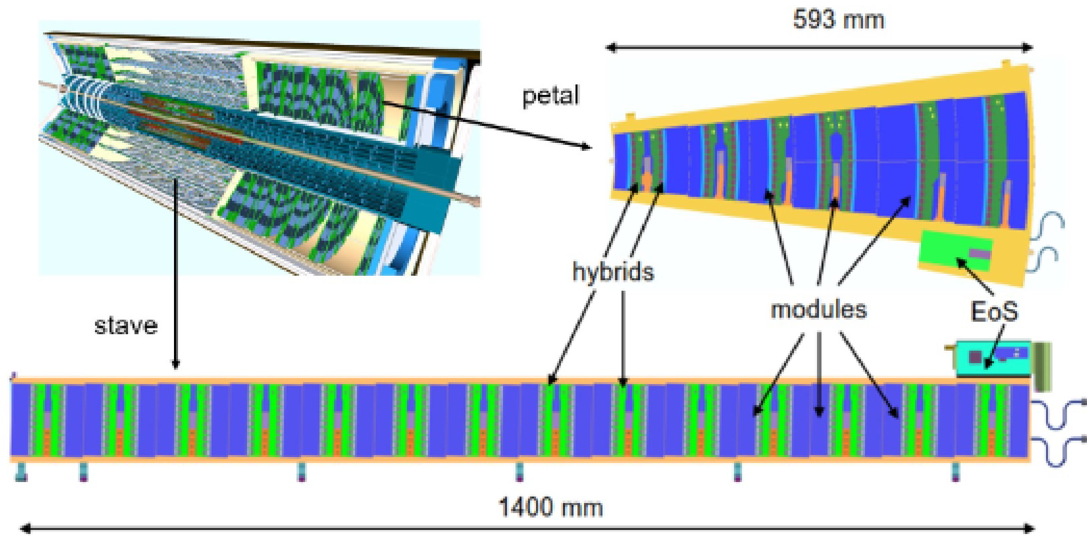


Figure 1.2: Overview over the main ATLAS ITk Strip Detector (upper left) components for the end-cap petals (upper right) and barrel staves (lower) [10]

The strip detector is divided into a barrel and two end-cap regions. Altogether, this detector will span $165m^2$ and facilitate 59.9 million readout channels. The basic building

blocks of these regions are staves for the barrel and petals for the end-caps. Each stave/petal hosts up to 14 silicon-strip modules on each side. These modules consist of a strip sensor and one or two hybrids containing the read-out ASICs and a power board hosting DC-DC converters along with the Autonomous Monitor and Control (AMAC) ASIC. The final piece to the stave/petal is the End-of-Substructure (EoS) card which acts as the interface between these components and the off-detector electronics.

1.1.2 The EoS Card

The EoS card is responsible for the transfer of data, power and control signals between various modules of the stave/petal and off-detector systems. The upstream (on-detector to off-detector) data flow consists of the EoS card receiving data from the front-end modules by up to 28 differential lines, referred to as E-links, operating at a maximum speed of 640 Mbit/s. These data lines are then multiplexed by up to two low power Gigabit Transceiver (lpGBT) ASICs and serialised before being transmitted via the Versatile Link Plus Transceiver (VTRx+) over a fibre optic link at 10 Gbit/s to the off-detector systems. The downstream data follows a similar path in the reverse direction but operates at a lower rate of 2.56 Gbit/s received over the optical link and then distributed to the front-end devices at 160 Mbit/s over the E-links. A block diagram of the EoS card is illustrated in Figure 1.3.

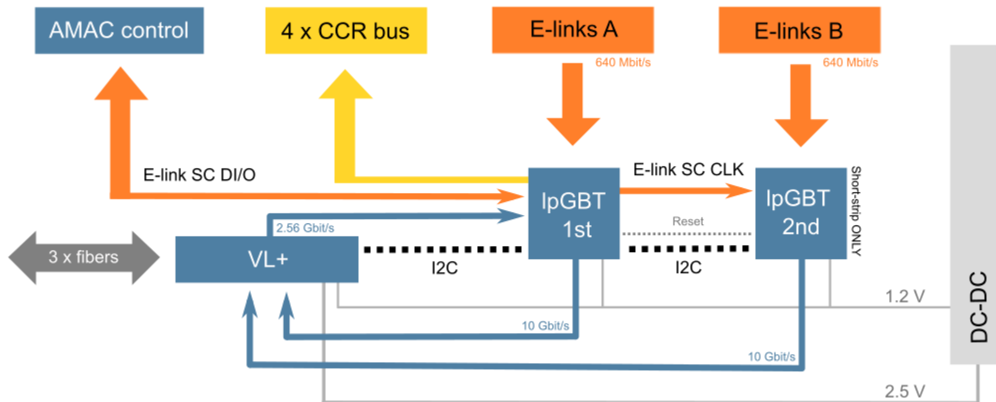


Figure 1.3: Block diagram of the EoS card, depicting the primary components and interfaces, as seen in DESY article [11]

The lpGBT operates off of a 1.2V supply while the VTRx+ requires both 1.2V and 2.5V inputs. The DC-DC converter component is responsible for providing these power

lines. A total of 10 EoS card variations have been designed to accommodate the different requirements of their associated substructures. Depending on the variant, the EoS card will house one or two lpGBTs and have minor layout differences to meet the differing mounting dimensions.

1.1.3 ITk Radiation Environment

The increased luminosity within the ITk is estimated to increase the radiation levels by an order of magnitude over the current ATLAS Inner Detector. The primary sources of radiation at the LHC are [12]:

- Particle collisions and the resulting particle debris;
- Beam-machine interactions;
- Interactions between the beam and residual gas inside the beam pipe.

Due to several factors influencing the radioactive environment, complex simulation programs are used to predict the resulting radiation levels. When quantifying radiation levels, a number of different metrics are used:

Integrated luminosity is the integral of the luminosity with respect to time. This metric is typically expressed in inverse femtobarns (fb^{-1}), which is a unit proportional to the number of proton-proton interactions in the accelerator. This value is important as it directly relates to the amount of data that can be collected and analyzed from the accelerator.

Rad is the unit used when describing the absorbed dose of ionizing radiation. A new unit of measurement, the Gray (Gy), has been proposed but has yet to see widespread adoption. To convert between the two units: 1 Gy = 100 rad. This metric is used when qualifying Total Ionizing Dose (TID) effects, which relates to the energy deposited in semiconductor devices and the impact this has on their performance.

Fluence is used to quantify the number of particles that intersect a unit area, typically expressed in particles/cm^2. This measurement is often used in conjunction with the Non-Ionizing Energy Loss (NIEL) parameter, which attempts to correlate the effects of different radiation environments (different particles, energy spectrum's and fluences), in an

effort to express complex radiation environments in a simpler mono-energetic equivalent, that is the 1 MeV neutron equivalent.

In relation to this thesis, having a focus on SEUs, fluence is the primary measurement this work is concerned with as it directly influences the probability of SEUs. As such, details on the other metrics are not analysed in-depth. The significance of these quantities is examined in the next chapter when discussing the effects radiation can have on electronics. In terms of the levels expected in the ITk, simulations of the expected fluence distributions within the ITk are depicted in Figure 1.4. These simulations are based on detailed modelling of the entire ATLAS ITk geometry and are created by the Radiation Simulation Working Group [13].

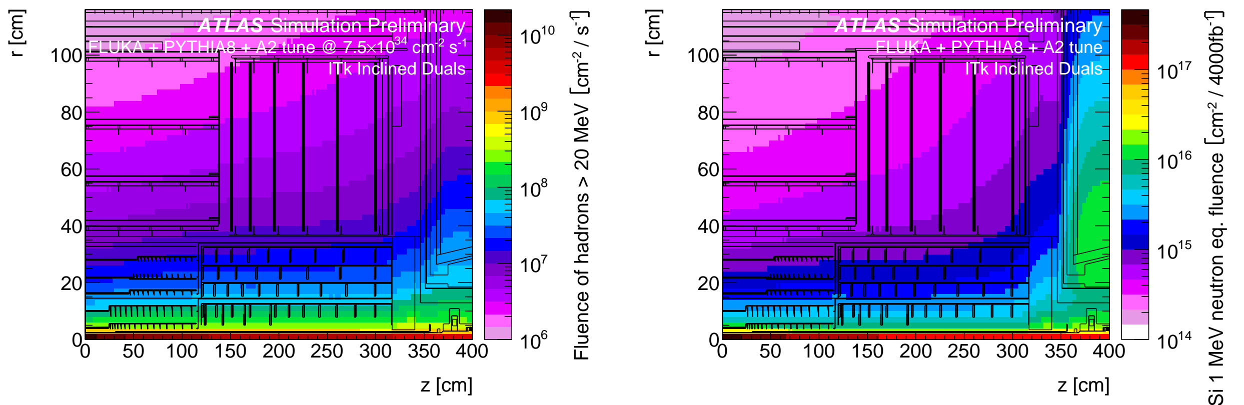


Figure 1.4: The fluence distributions for the ITk layout. **Left**: The fluence of hadrons with E>20 MeV per cm^2 per second, assuming an instantaneous luminosity of 7.5x10 $^{34}cm^{-2}s^{-1}$. **Right**: The 1 MeV neutron equivalent fluence per 4000 fb^{-1}

.

The proton collisions within the LHC will expose the electronics to significant fluxes of various particles. Close to the collision point, pions will be the dominant component of such fluxes, whereas, in the regions occupied by the majority of the electronics, neutrons will be the primary contributor [14]. Due to the presence of multiple particles with different fluxes, it is simpler to describe the fluence of hadrons with an energy greater than 20 MeV when characterising the radiation levels of the LHC, as depicted in the left plot of Figure 1.4. The same reasoning applies for describing the 1 MeV neutron equivalent fluence, as seen in the right plot of Figure 1.4.

The estimated radiation levels are used to define the radiation resistance requirements of various components depending on their location within the ITk. In order to offset the uncertainty associated with the simulations, a safety factor of 1.5 is commonly used when setting the required tolerance level. A summary of the maximum expected fluences for

the substructures carrying EoS cards are tabulated in Table 1.1.

Substructure	**Radius** [mm]	**Maximal Fluence** [n_{eq}/cm^2]	**Fluence of Hadrons** [cm^{-1}/s^{-1}]
Long Strips	762	3.8×10^{14}	4.6×10^{6}
Short Strips	405	7.2×10^{14}	1.5×10^{7}
End-cap	385	1.2×10^{15}	2.3×10^{7}

Table 1.1: Overview on the maximum fluences of relevant substructures in the ATLAS Strip Detector. The values include a safety factor of 1.5.

In summary, the LHC is undergoing a significant upgrade in order to study and increase the probability of rare events. This upgrade will result in the radiation levels increasing by an order of magnitude. As the current ATLAS detector already experiences electronic upsets caused by radiation [15, 16, 17], the new detector will require new hardware with increased resistance to radiation-induced effects. The need to test the radiation tolerance of this new hardware has led to the undertaking of this project.

1.2 Problem Description

The EoS card represents a single-point-of-failure for an entire side of each stave and petal, depicted in Figure 1.2. There is no opportunity to repair or perform maintenance on the EoS card after the HL-LHC begins operation. These factors emphasize the importance of ensuring the reliable operation of the EoS card. To this end, an extensive quality assurance and control process has been set out at DESY. This project aims to contribute towards this qualification process by exploring the susceptibility of the EoS card, with a focus on the VTRx+, to radiation-induced errors, and further characterizing the performance of this component under non-ideal configuration settings and its response to an irregular power supply.

The anticipated radiation levels within the ITk will surpass previous levels by a factor of 5. This presents a risk to the electronics within the system as radiation has the potential of interfering with the normal operation of electronic devices. The effects of radiation on electronics will be explored in-depth in the next chapter.

Radiation qualification of various components involved has already begun. The lpGBT has been put through rigorous radiation testing and was found to be susceptible to heavy

ions which resulted in short bursts of data errors [18]. The same process was followed with the VTRx+, various radiation tests were performed to qualify the device and the results revealed a vulnerability where data was corrupted in the presence of neutron radiation [19]. Both of these discoveries have been used in designing updated versions of the components with greater resilience to radiation. The vulnerabilities exposed during radiation qualification present a clear need for components to be tested thoroughly. These factors have influenced the design of the EoS card and the necessity to validate its performance in the presence of radiation.

In addition to radiation qualification, this project will also investigate the influence of noise on the power supply and the resulting impact on performance. A preliminary investigation [20] was conducted at DESY into the operation of an early prototype EoS card (using the predecessor of the lpGBT, the GBTx ASIC) when powered by a noisy input power supply. This study examined the output clock signal, EoS state machine, DAC and ADC outputs in response to a sinusoidal signal being superimposed on the 1.5 V DC power input. The clock and DAC outputs were shown to deviate from the expected values at low frequencies while the GBTx state machine was observed to switch between states erratically, making the operation unstable. These results are further supported by similar investigations [21] which demonstrate that power supply noise introduces gate delays with the potential of causing logic errors, instability in storage elements as well as timing signal jitter. This project will build upon this work to help characterise the EoS performance in terms of acceptable power margins.

Finally, this project will also contribute towards optimizing the optical link between the EoS card and the off-detector electronics. A bit error rate of 10^{-12} is one of the requirements set out for this component to ensure reliable operation. One of the primary influences over the bit error rate is the optical link quality. The VTRx+ has a number of configuration parameters (bias current, modulation current, etc.) that have been shown to influence the jitter in the optical signal [22] and impact the optical link quality. By adjusting these parameters, it is hypothesised that the optical quality link can be improved and help achieve a superior bit error rate.

1.3 Objectives

The objectives of this project are threefold:

1. Investigate the susceptibility of the VTRx+ to radiation-induced errors and the

impact this will have on the overall EoS card's performance.

2. Characterize the performance of the EoS card in response to an irregular power supply.

3. Explore the impact VTRx+ configuration parameters have over the optical signal quality.

To qualify the EoS card's, specifically the VTRx+ (seen on the right in Figure 1.5), performance in the presence of radiation, an Americium-Beryllium (AmBe) source will be used to investigate the susceptibility of the component to radiation-induced errors. Bit error rate tests will be carried out in order to determine the effect of the radiation on the performance of the device. Constraints in terms of radiation source accessibility will limit these tests to radiation levels less than that of the LHC, however, this will still prove an important step in ensuring proper operation of the device in a radiation environment. Similar studies [23, 24, 25] have shown that radiation sources (such as an AmBe source) producing relatively low energy neutrons (<10 MeV) are still capable of inducing errors and can provide meaningful results in qualifying a devices radiation tolerance. Based on the test results, it will be possible to extrapolate if the performance and tolerance requirements are being met under the experimental conditions.

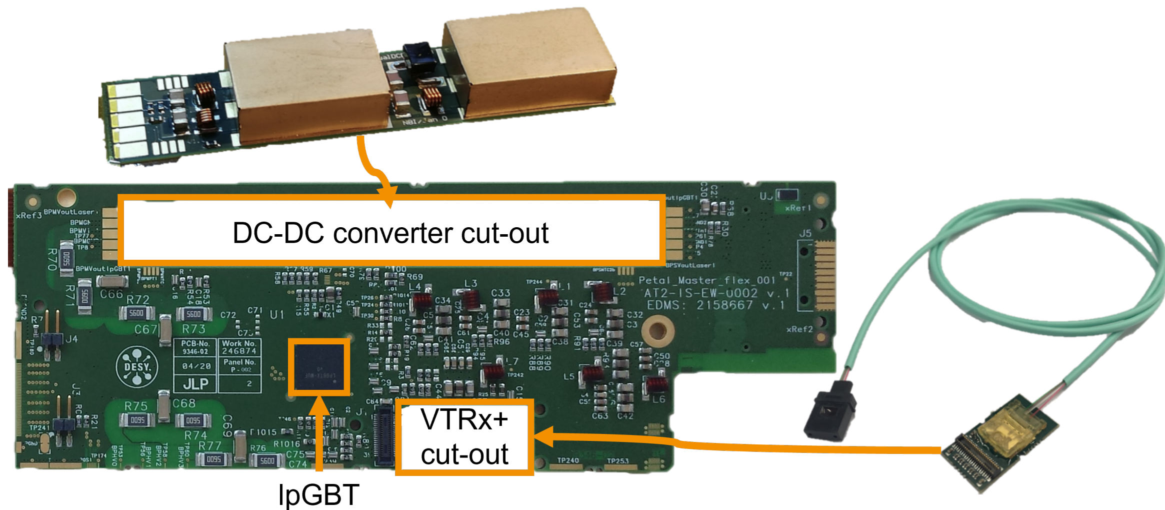


Figure 1.5: Image of a petal master EoS card and prominent components.

The EoS card will be powered by a custom component referred to as the DC-DC converter (depicted in the top of Figure 1.5), which will be elaborated on in the coming chapters. Based on the results shown in [20], the EoS card's operation can be influenced by power supply fluctuations, prompting the need for further investigation. Tests will be designed to

characterize the performance of the card when exposed to non-ideal input power conditions and these results will be compared to the DC-DC converter specifications and tolerances to ensure reliable operation.

The quality control tests being run at DESY have shown the EoS card surpassing the bit error rate requirement without any modification beyond the default operating parameters under laboratory conditions. These are promising results but the extent of impact from non-ideal operating conditions (radiation-induced effects, etc.) on the optical link remains to be seen. By optimizing the optical link through custom configurations and analysing the influence of the various parameters, it will be possible to maintain consistent performance in the presence of other extenuating factors.

1.4 Methodology Overview

The test setup at DESY was recreated using a FPGA (Xilinx KC705), a level converter card (interfacing between the FPGA 3.3 V and the EoS 1.2 V voltage levels), and a computer to run the LabView control software. The FPGA firmware and LabView software was developed at DESY and supported the majority of the test functionality required for this project, only requiring minor adaptations. The test setup is elaborated on further in the Methodology chapter.

After identifying the objectives for the project, described in the previous section, and implementing an operational test setup, the next step involved capturing a baseline for the EoS card's performance. This baseline will be used to validate the results from further experiments. Following that, the performance of the EoS card will then be monitored under various conditions (exposure to radiation, non-ideal input power, and customized optical link configurations) to evaluate the impact of these factors on performance. While conducting the experiments, software and firmware improvements will be evaluated and implemented in an effort to improve the accuracy of the results.

Research into relevant literature and related studies will provide further validation of the methodology involved in this project. Starting in the next chapter, the effect of radiation on electronics is explored, with a focus on circumstances relevant to CERN and the LHC.

1.5 Scope and Limitations

The EoS card has is a complex component having several different interfaces and the ability to facilitate the distribution of power, control and data signals between many different devices. As such, the qualification and testing of the EoS card is carried out by a team at DESY. This work has been performed in collaboration with the ATLAS-DESY group and focuses only on specific aspects of the EoS card and its components, which are outlined in the following paragraphs.

This investigation is only interested in the performance of the EoS card as determined by the bit error rate of the system and the optical link quality. Therefore, the bus tape (E-Links, power connections not directly powering the EoS card) and other features of the EoS card (ADC, NTC, etc.) are not included in this investigation. Additionally, the EoS card used in this study is a prototype of the Petal Master Flex variation and is not representative of all EoS cards.

Following on from the EoS card specifications, lpGBT ASIC used is a prototype, version 0, and is operated in a transceiver configuration. The VTRx+ is version 10, however, this is still not the final version intended for use in the ITk. The test setup makes use of I2C signals and power supply connections for the EoS card via a dedicated testing interface.

Due to the asymmetric nature of the optical link, a full loop back configuration was not possible. The lpGBT recovers a clock signal on the downlink from the testbench FPGA but carries no test data. The lpGBT is programmed to output a constant pattern on the uplink at a data rate of 10.24 Gbps using the Forward Error Correction encoding designated FEC5.

This experiment assumes the laboratory environment has a stable room temperature, there is no significant EMI interference and previous experiments run on the EoS card have left no lasting effects that would impact the results of this project. These assumptions are supported by baseline functionality tests carried out before the outset of this project, in which the EoS card operated as expected.

At the outset of this project, a significant amount of work was planned to be carried out at the research labs at DESY, making use of the high-end research equipment. However, due to the COVID pandemic, travelling to Germany was no longer an option and alternative solutions had to be made. The reduced access to specialized equipment (optical oscilloscope, optical splitter, optical attenuator, power supply Weiner crates, etc.)

led to a number of interesting developments in order to still achieve this project's goals.

1.6 Plan of Development

This thesis constitutes the work done in contributing towards the quality assurance and qualification process of the EoS card for operation within the ATLAS ITk. This report documents the steps taken in carrying out the objectives listed above and is divided into the following chapters:

- Chapter 2: This chapter introduces several concepts that are dealt with in this work. The theory and practical implications behind optical communication is explored. Followed by a discussion on how radiation and power supply fluctuations pose a threat to the reliable operation of electronic devices. A survey of relevant literature is presented, detailing the methodologies and results of similar investigations;
- Chapter 3: In this chapter, the tools used in order to carry out the necessary experiments in fulfilling the project's goals are examined. The testing infrastructure developed in this work is presented. Building on top of an initial test framework created by DESY, a number of contributions were made in extending the capabilities of this framework to suit the purpose of this thesis, in addition to expanding the testing proficiency at DESY. Moreover, the hardware developed and implemented in lieu of cost prohibitive testing equipment is reported on.
- Chapter 4: The experiment methodology followed in this work is discussed in this chapter. For each experiment carried out, the test setup and the testing procedure is explained, along with the data being collected.
- Chapter 5: This chapter reports on the results from each experiment. An analysis of the results is presented and the implications of the findings are discussed.
- Chapter 6: This chapter closes out the report with a review of the tests performed and the subsequent conclusions that are drawn. The relevance of this work and it's findings is reviewed, leading to recommendations for future work.

Chapter 2

Literature Review

This chapter begins with an exploration into communication theory. The data processing and transmission mechanisms implemented by the EoS card are reviewed. Following this, the effects of radiation on electronics are discussed with an in-depth look at the processes involved. A survey of recent literature and investigations, focusing on the susceptibility of relevant components to SEUs, is presented. Next, the effects of power supply noise are examined as well as the related testing methodologies used in similar projects. This chapter ends with a summary of the concepts covered and important implications taken from the studies reviewed.

2.1 Communication Theory

This section provides a background to data transmission theory in the context of the EoS card. Taking a top-down approach, the flow of data within the system will be outlined, followed by an analysis of the primary modules and an overview of how they function.

2.1.1 Data Flow

The EoS card is the interface between the on-detector and off-detector systems. This entails managing all communication and both the LV/HV supplies to the mounted substructure. The EoS handles this through a combination of high-speed optical links and differential lines. The following figure depicts an interface diagram of the EoS card where the various

signals and their respective interfaces are illustrated.

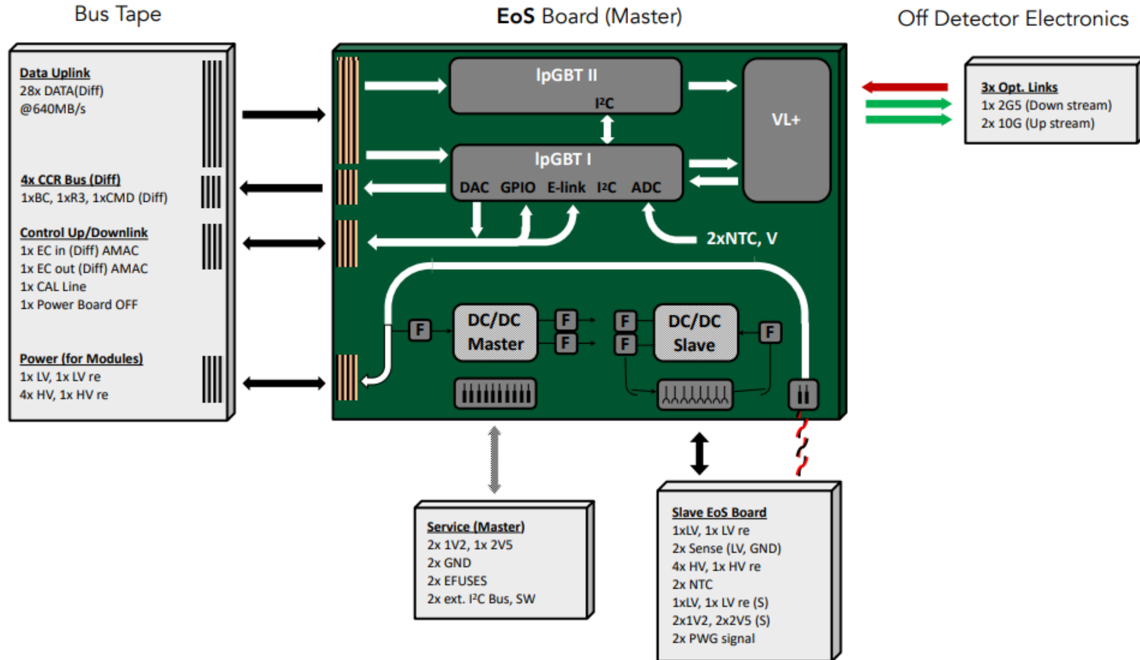


Figure 2.1: Illustration of the EoS card, the primary components and the data flow between the various interfaces, as seen in DESY presentation [26]

Starting on the right of Figure 2.1, the EoS card is connected to the off-detector systems through the power and optical links. The optical links allow for bidirectional communication and provide data paths for the Clock Control and Reject (CCR), Data Acquisition (DAQ) and Slow Control (SC) information. The data paths are functionally distinct but are merged together, allowing the optical link to be used simultaneously for data readout, trigger data, timing, experiment control and monitoring. This architecture has the advantage of operating with a constant latency that can function with high reliability within the environmental conditions expected from the LHC [8].

The optical data is received and transmitted by the Versatile Link Plus Transceiver (VTRx+) module on the EoS card. This component represents the front-end side of the optical link architecture, which will be expected to operate in the presence of high levels of radiation, where as the back-end will be operated by an FPGA and other Commercial Off-The-Shelf (COTS) components, as part of the off-detector systems. The VTRx+ is responsible for converting serial data, in the form of electrical signals into optical signals be sent over the optical fibres, and vice versa.

The on-detector modules (comprised of silicon sensors, read-out ASICs, AMAC control chips and power distribution boards), are connected to a bus-tape, which is bonded

to the EoS card, for power and signal distribution. The data and control connections between the EoS card and the front-end devices are referred to as E-links and communicate using CERN Low Power Signalling (CLPS), an NRZ transmission standard that supports multiple listening devices and a maximum data rate of 1.28Gbps [27]. Each EoS card is connected to a maximum of 28 front-end devices with the E-links operating at 640 Mb/s in the uplink direction and 320 Mb/s in the downlink direction.

In order to support the various data paths being merged, all optical data has to be transmitted serially. Data sent downstream is received by the VTRx+, then de-serialized by the Low Power Gigabit Transceiver (lpGBT) and converted to parallel form before being processed further. Additionally, to avoid having a dedicated clock line, the lpGBT, operating in transceiver configuration, is able to recover the clock signal from the downlink data stream. The front-end devices communicate with the EoS card via the bi-directional E-link connection. This allows for downstream data to be de-multiplexed and sent to the appropriate device. While in the upstream direction, data sent from the front-end devices, over the E-links, is serialized in the lpGBT before being transmitted over the optical link by the VTRx+.

2.1.2 The GBT Protocol

The HL-LHC requires a high data rate transmission system that can operate reliably within a harsh radioactive environment. In order to accommodate the high bandwidth needs without increasing the material budget (adding more optical links), the Gigabit Transceiver architecture was developed [28]. This transmission protocol supports high data rates (up to 10.24 Gb/s) and a robust error correction scheme, providing high reliability. To meet these requirements, a number of processes are performed on the transmitted data and are illustrated in Figure 2.2.

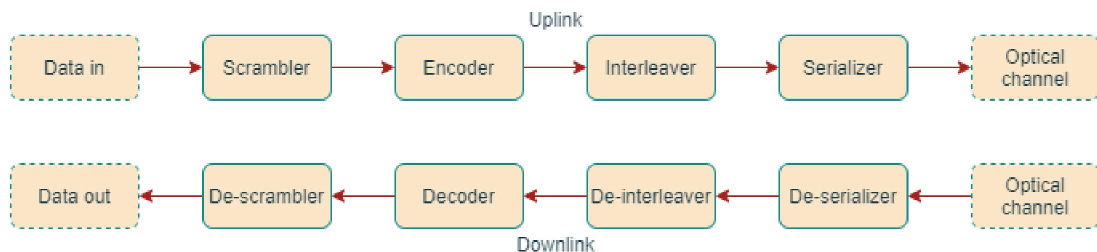


Figure 2.2: Block diagram of the GBT line coding scheme. **Top**: Uplink diagram. **Bottom**: Downlink diagram.

Scrambler On the receiver side of the lpGBT, a Clock and Data Recovery (CDR) circuit

is responsible for recovering and generating a high-speed clock signal. This recovered clock is used to correctly sample the incoming data stream. For the CDR circuit to operate reliably, the data being received needs to satisfy a few guidelines [29]:

1. A high number of 1-0 and 0-1 transitions to extract the needed frequency and phase information;
2. DC-balanced, an equivalent number of 1's and 0's to allow for AC-coupling;
3. Data must be non-periodic to reduce pattern dependent jitter.

The scrambler is responsible for ensuring the data meets the above guidelines. This is achieved by randomizing the data pattern to ensure the proper distribution of 0's and 1's. The scrambler circuit is based on linear feedback shift-registers and provides a DC-balanced output for the downlink and uplink. The de-scrambler circuit on the receiver side is responsible for recovering the original data.

Encoder The encoder implements the Forward Error Correction (mentioned previously in the mitigations against SEUs section) scheme. The FEC used in the lpGBT is a form of Reed-Solomon (RS) encoding. RS coding is classified as a systematic linear cyclic block code, and operate on "non-binary" symbols of m bits. The data to be sent, composed of k symbols, is encoded into an n symbol word, where $n = 2^m - 1$. This results in $n - k$ parity symbols, which can correct up to $t = (n - k)/2$ symbols. The code used is designated as RS(n,k). For the downlink RS(7,5) is used, where $m = 3$, resulting in a 7 symbol word (2 parity symbols and 5 data symbols) with the ability to correct 1 symbol per word (or 3 bits per 15 bits of data). In order to encode the 40 bits in the downlink frame, 4 encoders are used and generate 24 bits of parity codes. The uplink side of the lpGBT has the option of two different RS implementations, offering trade-offs between error correction strength and user bandwidth. For this investigation, the uplink FEC uses an RS(31,29) configuration, allowing for 5 errors to be corrected for every 145 data bits. 2 encoders are used in this configuration in order to protect 232 bits. Irradiation tests conducted on the VTRx [30] demonstrated that, in the presence of a mono-energetic proton beam, SEU induced burst errors were at most 3 bits long, implying that the selected FEC configuration should be capable of correcting all errors.

Interleaver After the data has been encoded, it is then interleaved. This process involves breaking up the encoded data frame into several blocks and rearranging the order of these blocks. Rearranging the data frame this way provides additional protection against burst errors (where several consecutive bits are corrupted). For example, the uplink FEC

uses symbols with a width of 5 bits, forming a word of 31 symbols, where 1 symbol per word can be corrected. If a burst error of 6 bits were to occur, this would result in the whole word (145 bits) being unrecoverable. However, when the data is rearranged through interleaving, the output from the 2 encoders are shuffled together such that adjacent symbols do not originate from the same encoder. This process can be seen in Figure 2.3. This means when a burst error of 6 bits occurs, each symbol will only have a portion of the 6 corrupted bits, allowing for the decoder to recover the original data. This effectively enhances the FEC scheme to protect against consecutive bit errors of up to 10 bits.

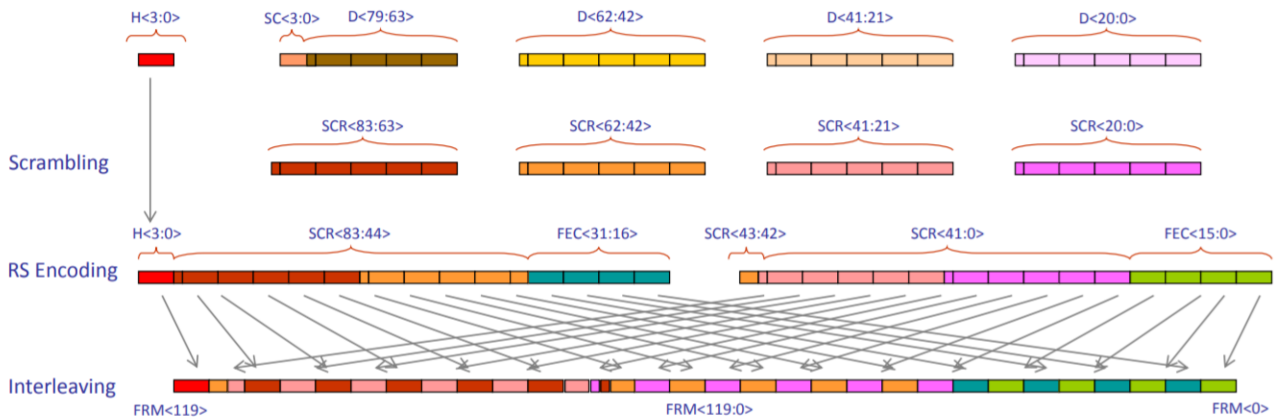


Figure 2.3: Illustration of the scrambling, encoding and interleaving process on the data frame, as seen in [31]. Note, this illustration is from the predecessor to the lpGBT, and while the processes are the same, the frame size is now 256-bits instead of 120-bits.

On the receiver side, as shown in Figure 2.2, the same processes discussed above, as applied to the transmitted data, is reversed on the receiver side in order to recover the original data. Overall, this communication architecture provides for robust error protection and high efficiency (the ratio of data bits of total bits in the frame). The Tx is determined to be 91% efficient while the Rx is 56% efficient due to the increased error protection.

2.1.3 Optical Communication

Optical data transmission is widely used in HEP applications, having several advantages over copper-based transmission. Optical fibres provide high bandwidth, low attenuation over long distances, immunity to Electromagnetic Interference (EMI), and electrical isolation between receiver and transmitter (avoiding ground-loops between the front-end and back-end electronics). These characteristics, in addition to the low cost and small-form-factor, lead to optical fibres being the chosen transmission medium over standard electrical links.

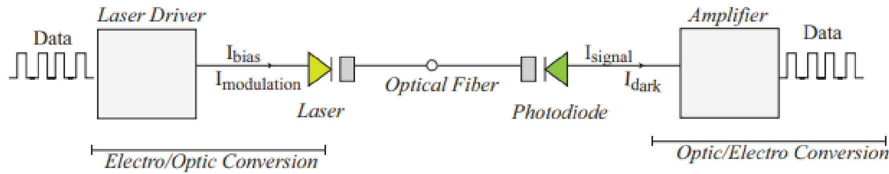


Figure 2.4: Illustration of an optical link and the components involved, [32]

An illustration of an optical link can be seen in Figure 2.4, depicting a number of the primary components involved. On the transmitter side, the laser driver and laser diode convert the electrical inputs into an optical signal to be propagated along the optical fibre. The receiver side consists of a photodiode and an amplifier which converts the optical signal back into an electrical one.

The VTRx+ used in this project makes use of the LDQ10 quad laser driver [22], which controls the operation of the laser. This component generates the bias and modulation currents necessary to drive the laser and are configured via an I2C block in the ASIC. During the pre-production qualification of this component, it was discovered that the I2C block is susceptible to SEUs when exposed to neutron irradiation [19].

The laser diode used is a commercial vertical cavity surface emitting laser (VCSEL) [33]. This type of laser diode has been shown to operate efficiently with low power consumption and demonstrated immunity towards SEUs [30]. However, this component has been shown to experience performance degradation due to cumulative radiation effects [19, 32]. This manifests in increased threshold currents and forward voltage, resulting in diminished optical output power. To compensate for these changes the driving currents, set by the LDQ10, will need to be adjusted depending on the amount of exposure to particle radiation.

The receiver side of the VTRx+ is composed of a Gigabit Transimpedance Amplifier (GBTIA) [34], and a commercial InGaAs photodiode. Photodiodes are known to be susceptible to SEUs and this is attributed to the large sensitive volume of the component [35]. The GBTIA has also been shown to be susceptible to SEUs, specifically in the component's power supply circuit [36]. The investigations carried out found SEUs in the photodiode to be responsible for single and short (at most 5 bits) burst errors, which formed the majority of errors observed. SEUs in the GBTIA were found to cause burst errors of up to 3 bits. The studies concluded that the error correction scheme employed by the GBT protocol would be sufficient in mitigating these effects.

2.1.4 Link Performance

The quality of a digital transmission system is most commonly described by its bit error rate (BER). This measurement is typically performed by a known data stream being sent through the transmission medium and counting the number of bits and bit errors that appear at the receiver. During the test, each received bit increments the total bit count (N_{bits}) and is compared to the expected bit, incrementing the bit error counter (N_{err}) for each failed compare. The BER measurement is expressed in Equation 2.1 below.

$$BER = \frac{N_{err}}{N_{bits}} \tag{2.1}$$

Another important quantity used to characterize the performance of a link is jitter. In digital communication systems, jitter is defined as the time deviation between the ideal timing of a signal transition through a decision threshold, or in simpler terms, how early or late a signal transitions with respect to the expected transition [37]. The amount of jitter in a communication channel limits the maximum frequency and quality of transmission. This is due to the impact jitter has on the sampling of the received signal, and results in errors when sampled incorrectly. There are a number of methods used when quantifying jitter, a few of the most common are listed below:

1. Absolute jitter, which is the Root Means Squared (RMS) evaluation of several edge measurements from an expected location or absolute time reference;
2. Period jitter, which is an RMS calculation of the deviation of each period from a waveform average;
3. Cycle to Cycle jitter, which is the measure of the variation of a signal between successive signals;
4. Time Interval Error, which is the time deviation between the actual threshold crossing and the expected transition point (or derived clock edge) of the signal.

When identifying the source of jitter it is useful to narrow down the possible sources by categorizing the type of jitter. There are two conventional categories used: deterministic jitter and random jitter. Deterministic jitter is typically non-Gaussian, periodic and bounded. This type of jitter can be further classified as data-dependent or periodic. Periodic jitter exhibits bounded effects but is not correlated to the pattern of data bits, and can often be caused by crosstalk from other signals or power-supply switching.

Random jitter is Gaussian, unbounded, and is often attributed to sources such as thermal noise.

Measurements of jitter are commonly made using an oscilloscope capable of producing an eye diagram of the signal. The eye diagram is a composite view of all the bit periods of a captured signal superimposed upon one another. A representative eye diagram is depicted in Figure 2.5, and illustrates a number of typical measurements that can be made.

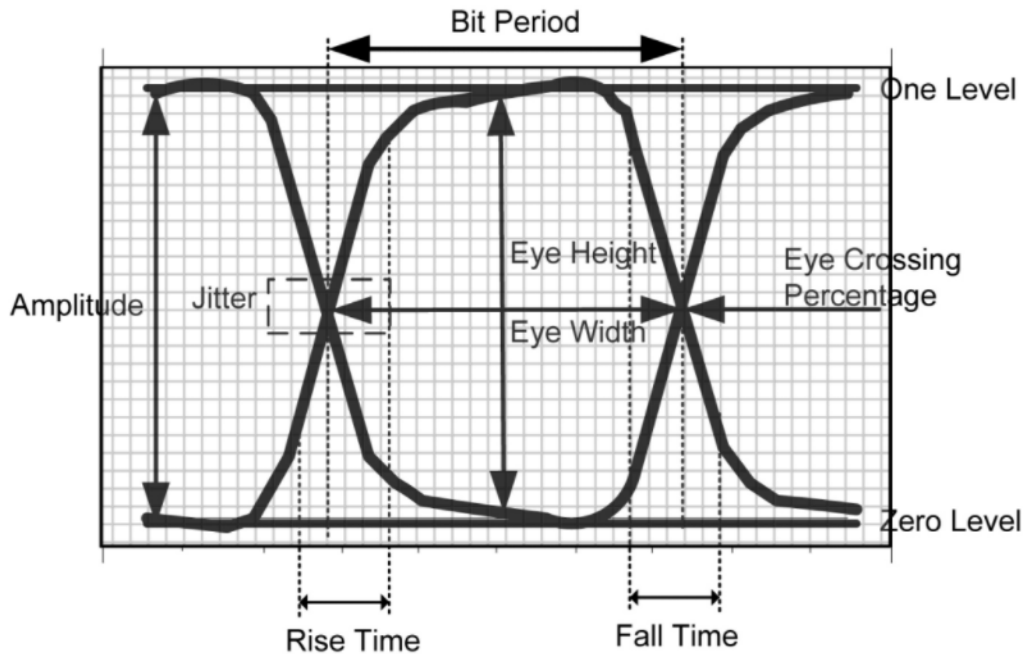


Figure 2.5: Illustration of a simple eye diagram and common measurements, [38].

Eye height is a measure of the vertical opening of the eye diagram. This provides insight into the signal-to-noise ratio at the sampling point, where a signal with an excessive amount of noise will be observed having a narrow eye-opening.

Eye width is a measure of the horizontal opening of the eye diagram. This measurement is made between the crossing points of the eye and is influenced by jitter, which is the deviation of transitions from their ideal crossing point. This provides a means for determining the impact of jitter on signal quality.

Eye crossing percentage is a measurement of the one and zero level relative to the crossing points and is calculated as $Eye\ crossing\ \% = 100 \times \frac{crossing\ level - zero\ level}{one\ level - zero\ level}$, where the crossing level is the intersection point of the signal transitions. This measurement gives an indication of duty-cycle distortion or pulse symmetry problems in the signal.

Rise and fall time are a measure of the transition time on the upward and downward slopes of the eye diagram. These measurements directly influence the eye-opening and determine the sensitivity of the system to timing errors.

2.2 Effect of Radiation on Electronics

This section introduces how radiation affects electronics. In radiation environments, such as space and high energy physics experiments, radiation is known to impact the performance of electronics and poses a design challenge in ensuring the reliability of a system. Radiation damage in electronics results from the energy loss of incident particles. These effects are often categorized between cumulative and transient effects. Cumulative effects build up over time, during exposure to radiation, and affect the electrical characteristics of a device. This will gradually degrade the efficiency of the device and after an extended period of exposure, renders the device inoperable.

Transient effects, also referred to as Single Event Effects (SEE), generally do not lead to the failure of a device but temporarily upsets the functioning, often resulting in data loss or corruption. The impact of these radiation effects can be differentiated between soft and hard errors, where the former refers to non-permanent damage as opposed to permanent damage indicated by the latter. As previously mentioned, this study has a focus on SEE and therefore will explore the related phenomena of transient effects in-depth, while only providing a brief explanation of cumulative radiation effects.

This section starts with an overview of how soft errors were first discovered and quickly became a popular topic of discussion in the development of high-reliability digital systems. Following this, the mechanism of how radiation interacts with electronics is explored and possible risks and mitigations are detailed. Finally, the last section puts all this information into context within the ITk.

2.2.1 Introduction to Soft Errors

The study of soft errors in electronics is a relatively new field, with the first formal report being published in 1975 by Binder et al. [39], investigating "anomalies" that had occurred in satellite electronics. Since then the study of soft errors has seen an exponential rise in interest. This is a natural trend as the number of electronic systems having severe

reliability requirements becomes more prevalent thus necessitating the need to account for radiation induced-errors.

With the study of Single Event Effects (SEE) gaining an increasing amount of interest over the years, there has been a lack of consistency in the terms used throughout the industry. In order to avoid confusion, a few of the most common terms are defined in this section. The image depicted in Figure 2.6 illustrates the relationship between several of the different acronyms.

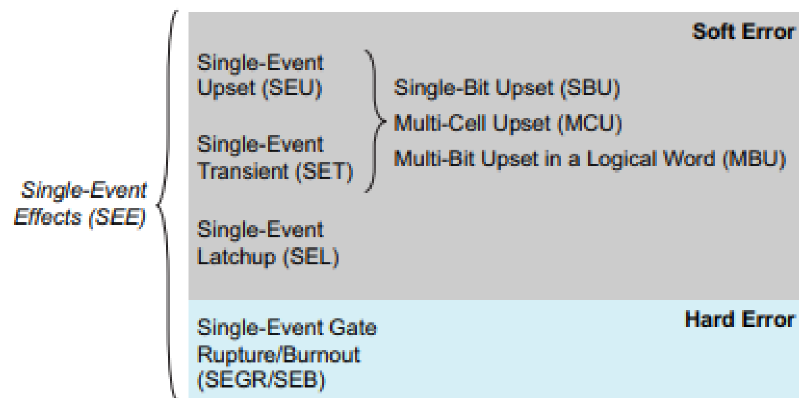


Figure 2.6: SEU acronyms, as seen in a white paper published by Altera on SEUs in FPGAs [40].

The diagram above was taken from a whitepaper published by Altera (now part of Intel) which provides an overview of SEUs for FPGA designers. This paper provides an apt source of information on SEUs, drawing from textbooks and JEDEC, an international organisation responsible for setting standards in the microelectronics industry. The following table defines the terms seen above, according to the JEDEC standard.

SEE	Single Event Effect. Any measurable or observable change in state or performance of a microelectronic device, component, sub-system, or system (digital or analog) resulting from a single energetic particle strike.
Soft Error	Storage element (memory cell, latch, or register) state change. No hardware damage and is correctable
Hard Error	An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit.
SEU	Single Event Upset. Storage element state change – may affect a single bit or multiple bits.
SBU	Single Bit Upset. A single storage location upset from a single strike.
MCU	Multiple Cell Upset. Multiple storage locations upset from a single strike.
MBU	Multiple Bit Upset. Multiple upsets in a logical word from a single strike.
SEL	Single Event Latchup. The event creates an abnormal high-current state by triggering a parasitic dual bipolar circuit, which requires a power reset. It can possibly cause permanent damage to the device, in which case the result is a hard error.

Table 2.1: Definitions for the terms used in Figure 2.6, as specified by the JEDEC standard [41]. The JEDEC association is an authority in the semiconductor engineer trade and develops standards for use in the industry.

2.2.2 Single Event Effects (SEE)

Given the above definition, the following section outlines how SEUs manifest, with an emphasis on those induced by neutrons, as is relevant to the EoS qualification procedure to be used in this work. The potential consequences of these events will be discussed. Followed by an overview of a few mitigation strategies used in the industry today.

The authors of [40] detail the mechanisms by which a charge-neutral particle (neutron) and a charged particle (alpha) can trigger an SEU. The following Figure 2.7, as seen in the paper, provides a depiction of how a neutron strike can trigger a soft error. It should be noted that neutrons have the potential to produce other charged particles, such as protons which also have the potential to induce an SEU, due to their nuclear reactions with silicon [24].

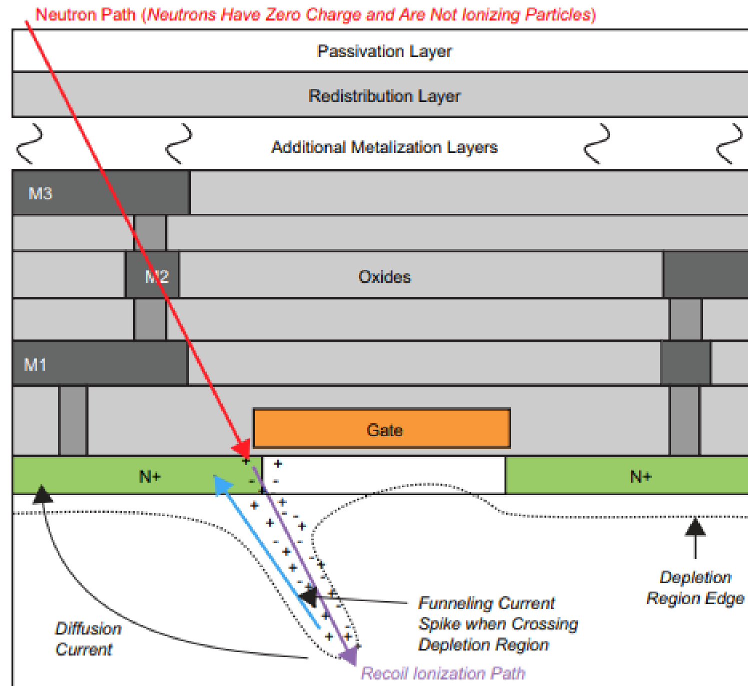


Figure 2.7: Neutron strike through a semiconductor device, as seen in [40]

In this image, the path of the neutron through the various material layers in a semiconductor device is shown (red arrow). As the neutron travels through the material, collisions with other molecules can create ions or charged particles with enough speed to produce the ionization path illustrated in 2.7 (purple arrow) and the associated electron-hole pairs. When the ion path crosses the depletion region beneath a drain-gate-source region, or near a p-n junction, the electrons created can be attracted to a higher voltage NMOS drain diffusion. If the amount of collected charge exceeds a critical value, a soft error occurs (changing the state of a storage element). In the case of PMOS transistors, holes can be attracted to a lower voltage which also can trigger a change of state in the storage element.

This thesis is focused on neutron-induced SEUs, but it is worth noting that other particles within the LHC can also cause these events. Heavy ions and other charged particles follow a similar process when striking a semiconductor device, they can produce an ionization path and depending on the energy deposited, cause a soft error.

The severity of a SEE is often location dependent. If the event occurs in an unused section of a device (e.g. an empty memory cell), it is unlikely this upset would have any measurable impact on the operation. However, should the upset occur in a critical section of the device, this could cause data loss, temporary malfunctioning or misinterpretation of erroneous data as being correct.

2.2.3 Total Ionizing Dose (TID) and Displacement Damage

The two forms of cumulative radiation effects are differentiated between TID and displacement damage. When a particle of sufficient energy interacts with a silicon chip, lattice displacements and electron-hole pairs can be generated. Displacement damage is a non-ionizing effect, where a particle transfers enough energy to an atom in a crystalline lattice, via an elastic or inelastic collision, to knock the atom free from the lattice. The atom then moves into an interstitial site and leaves behind a vacancy, this is known as a Frankel pair. An illustration of this process is depicted in Figure 2.8.

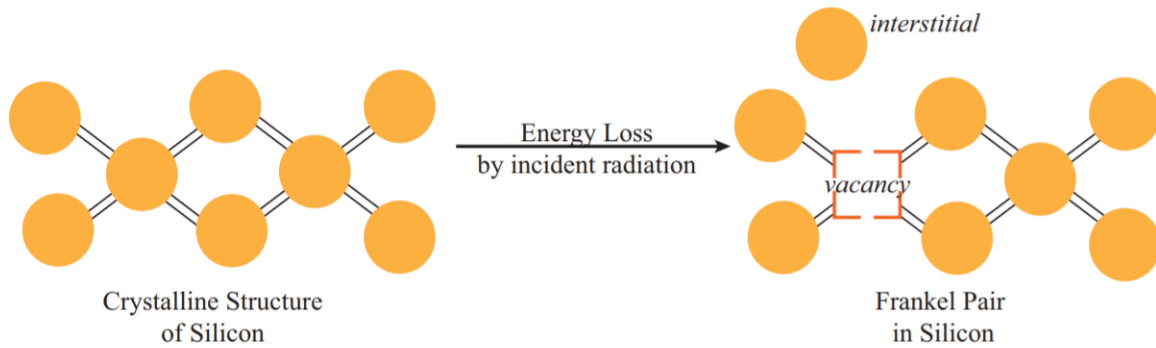


Figure 2.8: Illustrating the creation of a Frankel pair in silicon in silicon by non-ionizing energy loss. As seen in [32].

At room temperature, 90% of Frankel pairs will recombine [42] and leave the semiconductor material unaffected. The remaining Frankel pairs will form stable defects in the material, which then introduces additional energy states in the band gap of the semiconductor [43]. This has the effect of reducing minority carrier lifetime, charge carrier mobility and changing the majority carrier charge density. The practical implications of these effects manifest in shifts in the electrical performance of the device (e.g. increased base current, reduced collector current, etc) which can eventually lead to device failure as the electrical characteristics of the device degrade beyond the operating specifications.

TID effects are a consequence of the electron-hole pairs generated by incident particles interacting with the semiconductor material. The majority of these pairs will undergo recombination immediately and have no observable effect on the device. The recombination process is dependent on the type of radiation creating the pairs and the electric field in the dielectric [32]. The electrons, from the remaining electron-hole pairs, will drift through the oxide and be swept out one of the terminals of the device. This electron drift is the same mechanism, mentioned previously, that will generate SEEs when sufficient charge is produced. The holes that are left behind can become trapped in the oxide and

create a buildup of charge. An example of this occurring in an n-type metal oxide silicon transistor is illustrated in Figure 2.9.

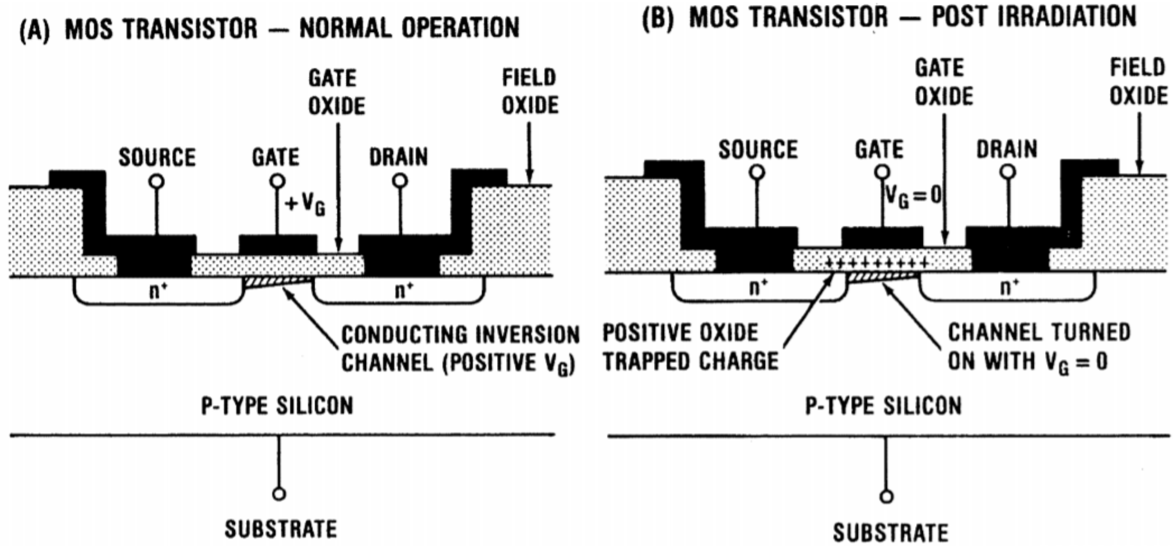


Figure 2.9: Cross section of an n-type channel metal oxide silicon transistor, illustrating positive-charge buildup in the gate oxide, where V_G is the gate voltage. As seen in [44]

The illustration in Figure 2.9, depicts the positive charge buildup post-irradiation. The holes being trapped in the gate oxide can offset the inherent conduction properties (i.e. the voltage thresholds) of the device, causing leakage current to flow when the device is in the off condition (V_G = 0V). Charge buildup in the gate oxide or field oxides will often result in large increases in static power-supply consumption (due to the leakage current) and can eventually render the device unusable.

2.2.4 Measuring SEUs

The sensitivity of a device to SEUs is characterized by its SEU cross section (σ). In the case of neutron irradiation, the cross section is defined by the ratio of bit errors ($N_{biterrors}$) over the neutron fluence (ϕ), as expressed in Equation 2.2.

$$\sigma = \frac{N_{biterrors}}{\phi} \tag{2.2}$$

There are several factors that influence a device's susceptibility to SEUs. The first two are directly related to the design of the device and are referred to as the sensitive volume (SV) and critical energy (E_{crit}). The SV is the volume within the device where ionization has to take place for the charge to be collected. The E_{crit} is the threshold amount of

energy deposited (E_{dep}) in the SV required to cause an upset. Both of these quantities have been changing over the years as technology trends are inclined towards smaller sizes and reduced power consumption. As semiconductor devices are fabricated in smaller and smaller packages each year, the SV is also reduced. However, the trend towards lower power consumption and the reduced operating voltage of these devices has also seen a reduction in the E_{crit}. In modern technology, these shifts have essentially cancelled each other out in terms of increasing or decreasing a devices susceptibility to SEUs [45].

The next influential elements are related to the radiation environment the device will be exposed to. The E_{dep} associated with a particle as it traverses a device's SV is dependent, not only on the kind of particle but also its energy distribution and its fluence. As a result of this, it is impossible to estimate the SEU upset rate of an environment based on the TID levels or 1 MeV neutron equivalent fluences. In the relevant literature, related quantities can often be seen when discussing the energy deposited by a particle, such as the energy loss $\frac{dE}{dx}$ or the linear energy transfer (LET). The dependence of E_{dep} on various factors contributes to the difficulty in effectively predicting the SEU rate of a device in a complex radiation environment.

When testing for SEU susceptibility with directly ionizing particles, the incident angle of the irradiated particles on the DUT has been shown to have a strong influence on the upset rate. This is primarily due to the orientation of the SV and the incoming particle, whereby at certain angles, the path travelled through the SV will be at a maximum, increasing the SEU rate. However, for neutrons, which are not directly ionizing, the incident angle has been demonstrated to have a negligible influence on the SEU rate and further confirms the dominant cause of neutron-induced SEUs being due to the nuclear reactions and resulting particles [35].

Lastly, the material composition of the device and the technology used also play a role in determining the SEU sensitivity. Certain materials being present within a device have been shown to increase the rate of SEUs. For example, low energy (thermal) neutrons have been shown to have an insignificant contribution towards SEU rates, unless the device contains Boron-10, in which case these neutrons can become the dominant source of SEUs [46]. Therefore, when selecting components for operation within harsh radioactive environments with the potential for SEUs, comprehensive testing across the various irradiation sources foreseen is the best method of ensuring reliable operation.

2.2.5 Mitigations Against SEUs

SEUs present a significant threat to the data integrity of digital transmission systems within the LHC. A number of techniques have been developed to counteract these effects. The suitability of the mitigation technique is often circumstance dependent as each has various pros and cons. This section will provide an overview of the techniques employed by the components populating the EoS card.

Circuit logic protection A popular mitigation technique in use today is Triple Module Redundancy (TMR) [47]. This technique has been around for a number of years now and can be implemented in a number of different forms. The main idea behind TMR involves triplicating the circuit to be protected. A simple illustration of this is provided in Figure 2.10.

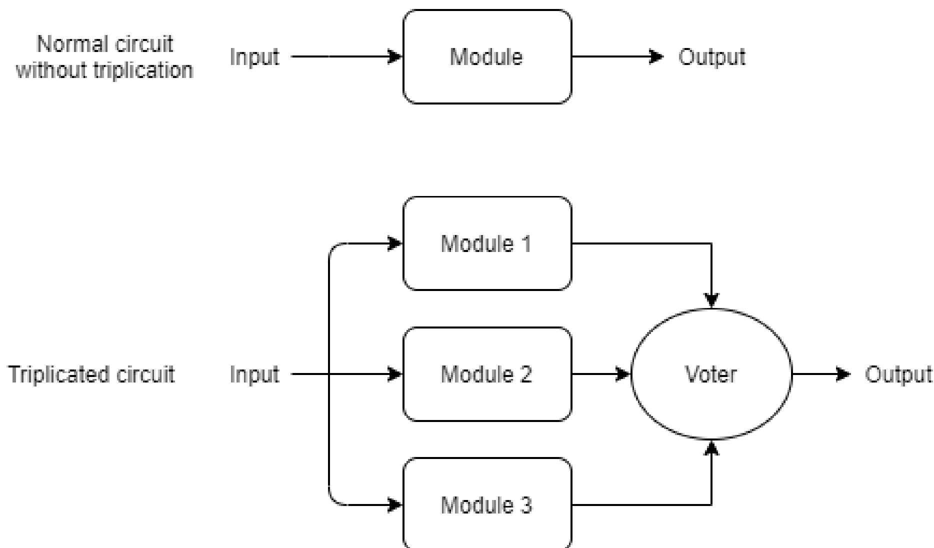


Figure 2.10: Block diagram of how TMR is applied to a simple circuit

The diagram depicts a simplified circuit, without triplication, at the top and the triplicated version below. If an SEU were to occur in the non-triplicated module, the resulting output would be rendered invalid. In the triplicated version, the voter only outputs the majority result from the modules. This design allows for an SEU to occur in one of the modules without it impacting the output, effectively protecting against single bit upsets (SBU) and multiple bit upsets (MBU). However, should more than one module experience an SEU, the output would be made invalid. For this reason, the triplicated modules are usually spread out within the device to reduce the chance of a multiple cell upset (MCU). This technique comes at the cost of power consumption and resource usage.

Cell storage protection The next mitigation technique which is gaining popularity,

is the Dual Interlocked Cell (DICE). A good explanation of this technique is provided in the textbook, Soft Errors In Modern Electronic Systems [45], where M. Nicolaidis describes a storage cell (illustrated in Figure 2.11) that has two states: the 0 state $(X_1 = 0, X_2 = 1, X_3 = 0, X_4 = 1)$ and the 1 state $(X_1 = 1, X_2 = 0, X_3 = 1, X_4 = 0)$.

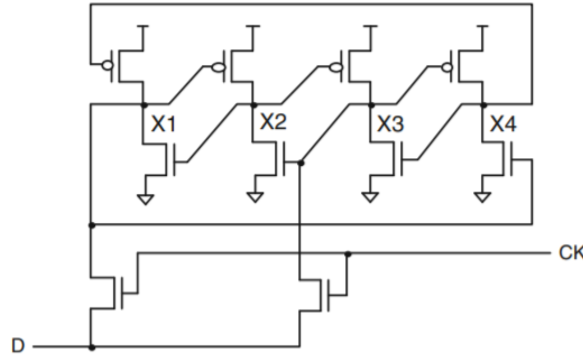


Figure 2.11: A transistor diagram of a DICE cell, as seen in [45].

In either of the two states, should any node experience an upset and a change of state, the remaining three nodes will consist of two consecutive nodes having the values of 1 and 0. These two nodes are referred to as the hold nodes the other two are the affected nodes. For example, if node X3 is struck by a particle, node X2 could also be affected but the hold nodes, X4 and X1, would remain unaffected. The hold nodes preserve their correct values and due to the arrangement of transistor gates and inverters, the current flowing through this cell quickly restores the correct values to the affected nodes. This technique comes at the cost of minor but non-negligible area, power and time-delay penalties.

Data transmission protection Forward error correction (FEC) is a well-known method of protecting data from corruption in communication systems. This technique is applied to the physical layer of a network, which describes how the raw bits are transmitted through a system. In [48] the authors demonstrate how error correction coding can also be used to mitigate the effects of SEUs in optical links. This method is employed by encoding the data at one end of a communication channel using a specific error correction algorithm before transmission. Once the data is received at the other end, it is decoded and errors are identified and corrected. The encoding process will add redundant bits to the data that allows the decoder to detect and correct a limited number of errors in the transmitted data. Different error correction codes will often have a trade-off between efficiency and the number of errors they are able to correct. Being able to predict the SEU error rate of a communication system could help determine which error correction protocol would provide the necessary protection while sacrificing as little efficiency as possible. The particular FEC scheme employed by the lpGBT is elaborated on in section

2.1.2.

2.3 SEU Testing

Several prior studies have been conducted on the impact of SEUs on the VTRx and lpGBT. Five of these studies are presented in this section, with a summary of their experimental methods and results. A sixth study is included as well and details the relationship between SEU susceptibility and supply voltage.

In [30], the authors investigate the SEU susceptibility of the VTRx (the predecessor to the VTRx+). A 70 MeV mono-energetic proton beam with a particle flux of 1x$10^8 p/cm^2/s$ is used to irradiate 3 different versions of the VTRx, as well as a similar commercially available transceiver. The test set-up used was based on an FPGA-based BER testing system [49], where an FPGA generates the test data, transmits it to the DUT where it is then sent back to the FPGA and checked for errors. This set-up is widely used as it implements the GBT protocol, supports the high-data rates required and allows direct measurement of the BER before and after FEC is applied. An illustration of the set-up used in this experiment can be seen in Figure 2.12. Each of the optical links were tested, one consisting of the transmitter of the DUT and a shielded reference receiver, and the other having a shielded reference transmitter connected to the receiver of the DUT. Optical attenuaters were used to introduce attenuation on the link and an optical oscilloscope was used to measure the optical signal amplitude.

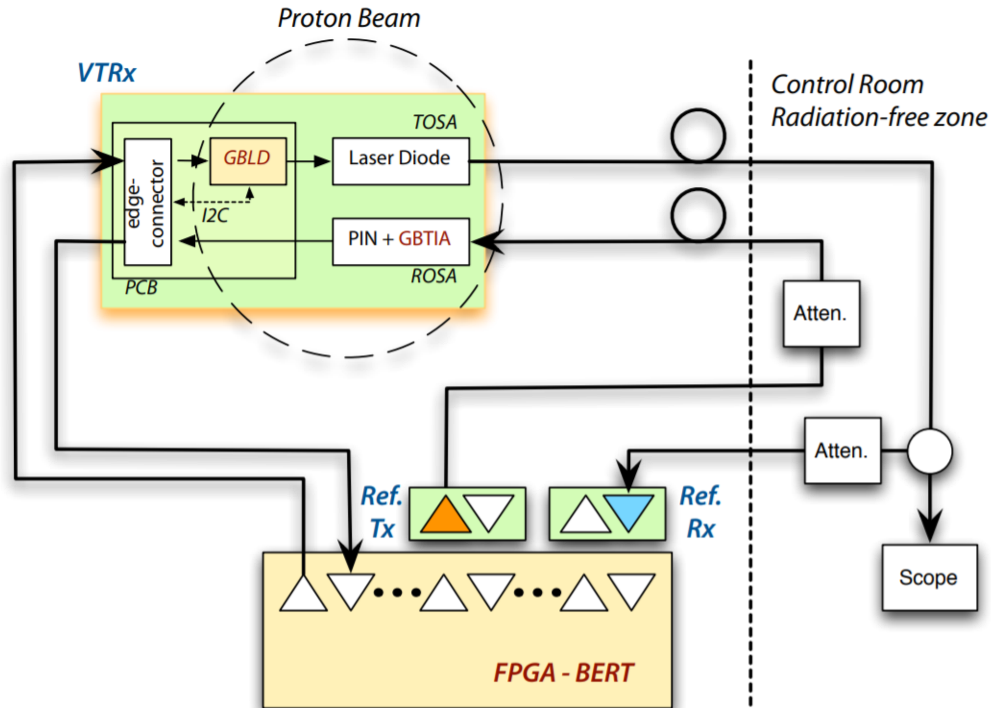


Figure 2.12: Experiment set-up used for the proton irradiation BER test, [30].

In order to quantify the susceptibility to SEUs, the cross section was measured through BER tests over a range of Optical Modulation Amplitudes (OMA), which is the optical signal amplitude at the input of the device. Additionally, the control registers of the laser driver were continuously read over I2C to monitor for upsets in the configuration memory. The results from this study showed no SEUs occurring on the transmitter side of the VTRx, nor in the control registers. SEUs were observed in the receiver components, however, all error bursts encountered were short enough to be correctable by the FEC. The effect of these SEUs on the BER of the different devices can be seen in the left plot of Figure 2.14. This method of analysis divides the measured BER into two regions: one where the primary source of errors is electrical and environmental noise; the second having the dominant source of errors being SEUs.

An in-depth study, titled "Radiation-hard Optoelectronics for LHC detector upgrades" [32] carried out a series of tests aimed at qualifying the radiation tolerance of the VTRx. A neutron beam with a distributed energy spectrum, having an average energy of 20 MeV and a maximum of 50 MeV, and a flux of 4x$10^{10} n/cm^2/s$ was used to irradiate the device while monitoring its performance through BER tests and eye diagrams. The test set-up used is depicted in Figure A.1, following a similar setup to that used in [30]; with one key difference being optical, data sent to the VTRx receiver is looped back to the VTRx transmitter and sent back to the FPGA. This setup does not test both links separately but

instead assumes that all SEUs encountered can be attributed to the receiver components.

Figure 2.13: Experiment set-up used for the neutron irradiation BER test, [32].

The results from this study have been plotted in a similar fashion to the previous study, as seen in the right plot of Figure 2.14 (the "SEU dominated" and "Noise dominated" labels are believed to have been swapped accidentally). Comparing the two plots, it can be seen that the proton-induced SEUs start having a noticeable impact on the system at a BER of 10^{-7} and -17 dBm OMA, while the results from the neutron beam show SEUs becoming the dominant source of errors at a BER of 10^{-8} and -18 dBm OMA. These results demonstrate the SEU cross section dependence on the irradiated particle energy levels and how SEUs caused by direct ionization (protons) are comparable to SEUs from nuclear reactions (neutrons).

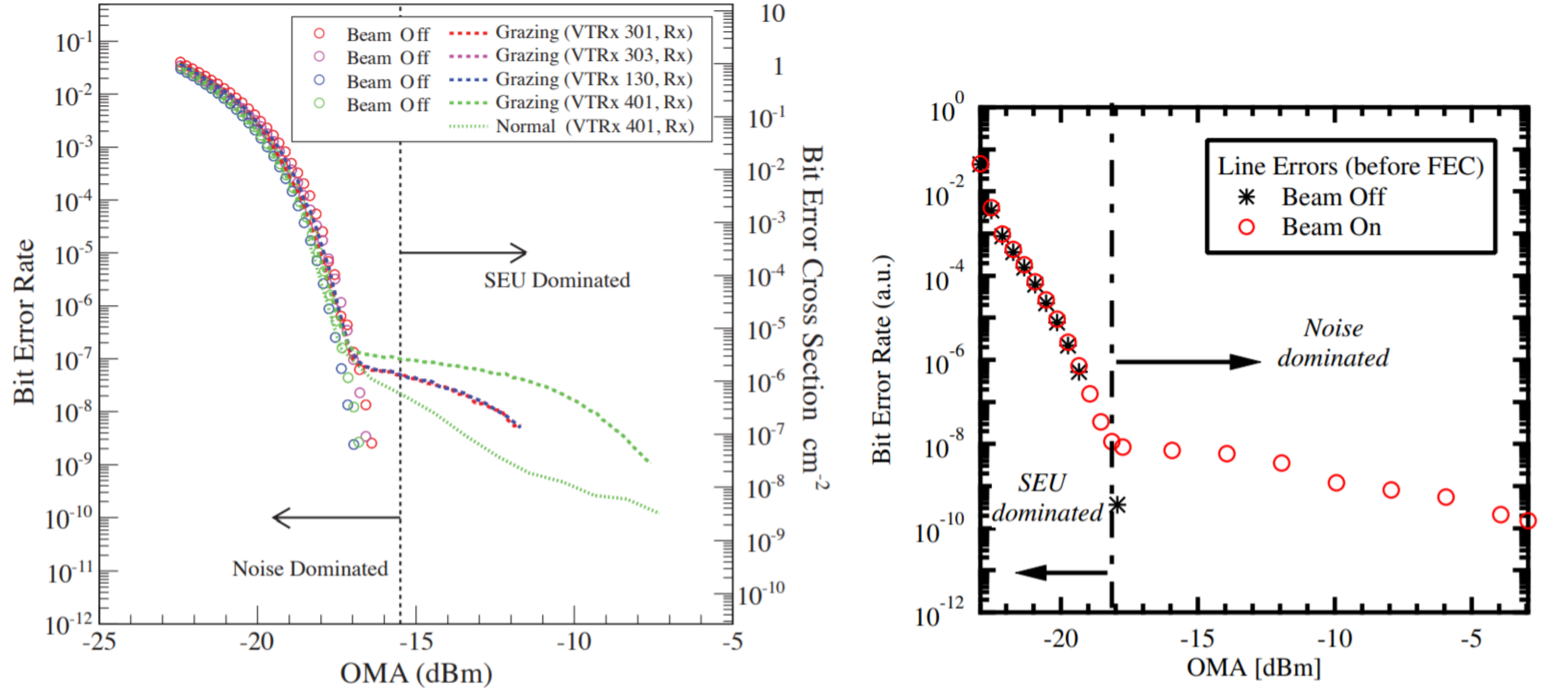


Figure 2.14: BER performance of the VTRx during irradiation and without FEC. **Left**: BER curve from [30] using a proton beam. **Right**: BER curve from [32] using a neutron beam.

.

In a similar study introduced earlier, [19] describes the development status of the VTRx+ and presents the results of various tests used to qualify the component. The irradiation tests performed revealed that the I2C block of the LDQ10 laser driver was vulnerable to SEUs. There is a lack of information provided on the radiation source used in this test, only that SEUs were discovered using a neutron source and then later reproduced in additional tests with a dual photon absorption laser and heavy ions. The SEU findings in this report are of particular interest because the LDQ10 laser driver is based on the laser driver used in [30], which showed no evidence of SEU vulnerability when irradiated with a proton beam. This discrepancy further emphasizes the need to test devices with a representative species of particles they will be exposed to.

The SEU susceptibility of the lpGBT has been thoroughly investigated in [27] and [18]. The tests carried out made use of heavy ions with LETs between 9.9 (Ar) and 62 (Xe) MeV cm^{2}mg^{-1} had a maximum flux of 15x10^3 s^{-1}cm^{-2}. Additional tests were performed with a dual photon absorption laser, reproducing results from the heavy-ion test and identifying the sensitive areas in the circuit design. The following areas were found to be vulnerable to SEUs:

- The frame aligner circuit, which would take an excessive amount of time to lock onto a frame after an SEU-induced-loss-of-lock event;
- The CDR circuit, which resulted in a short burst of data errors when an SEU would introduce an erroneous pulse in the clock divider;
- The configuration memory, which uses an asynchronous reset/set signal that could be activated by an SEU and overwriting the original contents.

As mentioned previously, the SEU susceptibility of a device is influenced by the E_{crit} of its internal nodes. As the E_{crit} is proportional to the supply voltage, a number of authors have made use of this fact when carrying out SEU tests. In [50] an investigation into the SEU sensitivity of DICE flip-flops was carried out using four different heavy ions and four different supply voltages. The results from this experiment demonstrated that a reduction in the supply voltage from 1 V to 0.5 V can increase the SEU cross section by a factor of 8.3. Another investigation on the SEU susceptibility of DICE flip-flops [51] demonstrated the same supply voltage dependence with alpha particles. This study found that a decrease in supply voltage from 1.1 V to 0.9 V resulted in the SEU cross section increasing by a factor of 3.

2.4 Power Supply Noise

Noise immunity has always been an important aspect of circuit design. Beginning with analog circuits, where fluctuations in the supply voltage could significantly impact the device's operation and performance. The increasing popularity of digital circuits can be partly attributed to their inherent noise immunity, where high-gain logic gates are capable of restoring the signal amplitude in the face of minor voltage level degradation or fluctuation. While digital circuits are less sensitive to supply variations than their analog counterparts, they are still vulnerable should their noise margins be exceeded.

In the context of this work, noise is defined as anything that causes the supply voltage to deviate from the nominal value. Based on the time-domain behaviour, noise is commonly categorized between DC noise and pulse noise. DC noise manifests as a change in the steady-state voltage level of a supply, while pulse noise is an intermittent deviation in the nominal supply level. Figure 2.15 provides a visual example of the two categories.

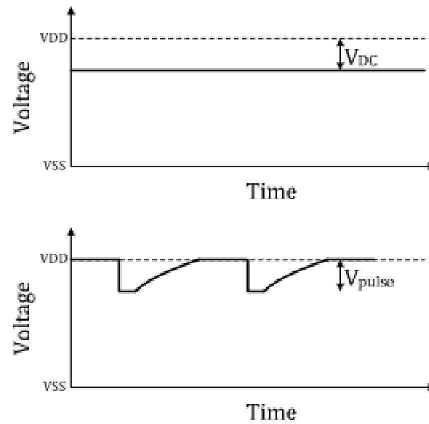


Figure 2.15: Illustration of the two categories of noise based on the time domain behaviour, as seen in [21].

The most prominent sources of noise in digital design are power supply noise, leakage noise, charge-sharing noise and crosstalk noise [52]. Leakage noise is generally associated with the off current of field-effect transistors and is a DC noise source due to the resulting change in the steady-state voltage levels (slow variation with respect to the system clock). Charge-sharing noise is commonly attributed to the redistribution of charge between various capacitive nodes within a circuit. Crosstalk noise occurs when adjacent signal lines experience inductive and/or capacitive coupling. This results in changes on one signal line, influencing the integrity of a neighboring signal. Both crosstalk and charge-sharing are sources of pulse noise.

While the sources described thus far cause fluctuations on the power supply lines in a circuit, it is important to differentiate power supply noise (PSN) as a separate source of noise explicitly appearing on the supply and ground nets of a chip. Power supply noise has both a DC and a pulse component. The DC component arises from the voltage drop through the power and ground nets due to the current demands of the chip. While the pulse component is attributed to the RLC response of the chip to current consumption. The work presented here will focus on the impact of power supply noise on the EoS cards performance. While other noise sources are acknowledged, they are considered out of scope for this work.

2.4.1 Effects of PSN

Increased Gate Delay Logic blocks within digital circuits are characterized by a propagation delay. This delay defines the time it takes from a change on the input to

produce a change on the output. Studies [53, 54] have demonstrated that the propagation delay is increased as the supply voltage decreases. If the delay exceeds the timing margins for the circuit, logic errors are likely to occur. For example, in a sequential circuit where a logic block has its output stored in a flip-flop, triggered by a periodic clock signal. If the logic block's propagation delay exceeds the clock period, an erroneous value could be stored in the flip-flop.

Storage Instability Storage elements such as flip-flops, registers and static random-access memories (SRAMs) are carefully rated for the maximum and minimum supply voltages they can operate between without error. However, experiments [55, 56] have shown that read and write errors can still occur when operating within these voltage margins due to power supply noise. The voltage fluctuations were capable of disrupting the normal charging and discharging of the transistors within the cell, such that erroneous data would be written or read.

Timing Signal Jitter Modern chips composed of various digital circuits often require multiple clock domains, where the clock signal in each domain operates at a different frequency. Phase locked-loops (PLLs) and voltage-controlled oscillators (VCOs) are commonly used to generate the different clock signals. These circuits are comprised of logic gates and suffer from the same increased delay issues mentioned previously. The result of this increased delay, in a clock generation circuit, is the introduction of jitter to the clock signal. The magnitude of the jitter has been shown to follow a linear relationship with the standard deviation of the power supply noise [57]. If the jitter exceeds the timing margins of the circuit, this can lead to synchronization errors between the various clock domains and disrupt the normal operation of the device.

2.4.2 PSN Testing

The most common approach taken, when investigating the impact of PSN on a system, is simulation. This requires building models of the device being investigated, accurately modelling not only the logic behaviour but also the power distribution network in the chip. This can be a lengthy process and often only covers static voltage drop analysis due to the complexity involved in modelling dynamic responses [58].

An investigation into the E-link clock output (eclk) on the lpGBT revealed an increase in gate delay due to decreasing supply voltages (VDD) [59]. These results were obtained by simulating the lpGBT using a reference clock (not CDR mode) at different supply voltages

and measuring the response time of various branches of the clock tree. A clock divider is connected to the reference clock and generates the eclk signal. This signal passes through two logic blocks before being output. The delay experienced by the eclk signal is measured at each stage and plotted in Figure 2.16. The blue line represents the signal coming from the clock divider, while the yellow and red lines represent the delays encountered after the first and second logic block, respectively, and the green line corresponds to the delay experienced at the signal output. The dashed green line represents the delay when the output block operates with the nominal 1.2 V supply.

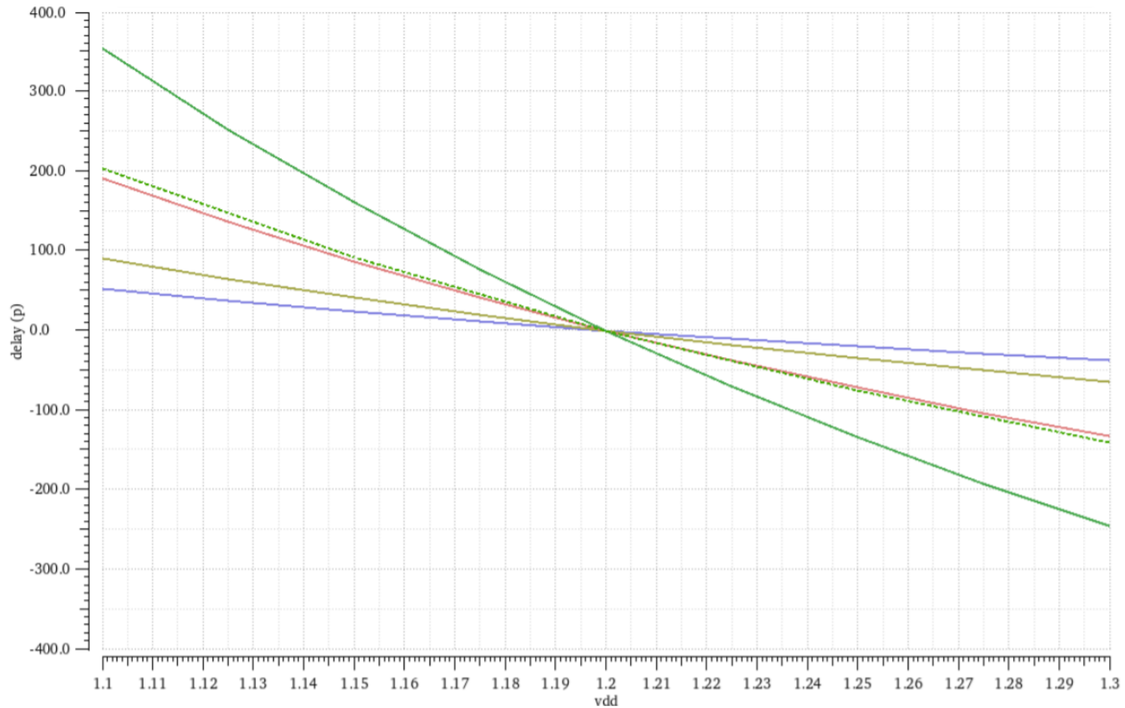


Figure 2.16: A graph of the propagation delay at various stages of the eclk signal over a range of supply votlages, [59].

The eclk signal has a period of 781.25 ps (1.28 GHz) and the delay experienced by the output signal at 1.1 V is roughly half the clock period. The study identified this as a potential issue and proposed a number of design improvements to mitigate the delay in future lpGBT iterations.

In another investigation on the lpGBT, a study was performed on the amount of jitter introduced on the lpGBT clock due to PSN [60]. This study took an experimental approach in evaluating the impact by injecting noise on the power supply in the form of sine waves over a range of frequencies. Two devices were used to inject the noise, a Line Injector J2120A to cover frequencies up to 10 MHz and a Bias-T ZX85-12G-S+ amplifier to reach frequencies up to 100 MHz. The results from this investigation can be seen depicted in Figure 2.17.

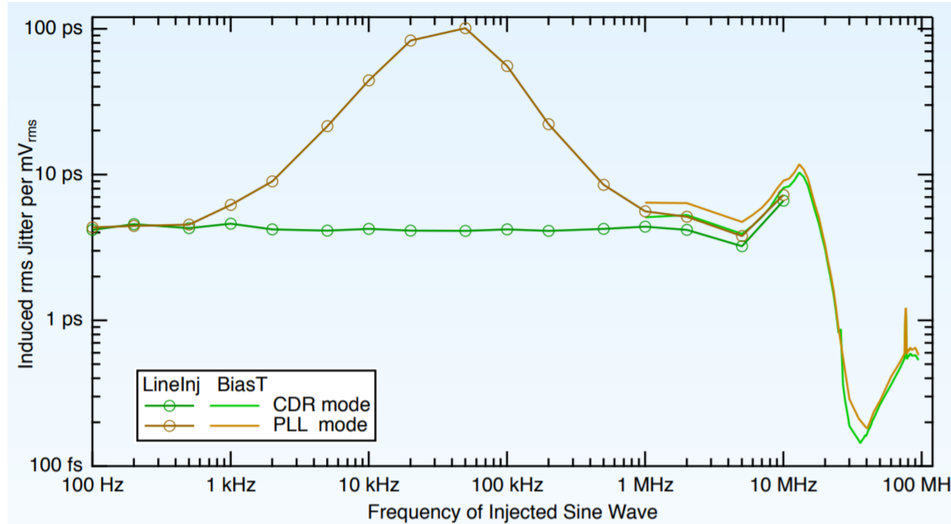


Figure 2.17: A graph of the jitter induced on the lpGBT clock as a function of frequency of the injected sinusoidal noise, [60].

The induced jitter in the lpGBT was studied in two modes of operation, CDR mode and PLL mode (using a reference clock). The results demonstrate a significant amount of jitter being induced in PLL mode, peaking around 50 kHz. While during CDR mode, the induced jitter remains constant at 4-5 ps/mV rms up to about 10 MHz. Recommendations were made on improving the PSN sensitivity by optimizing the implementation of decoupling capacitors.

2.5 Summary of Literture Review

From the discussions made in this chapter, a number of observations can be made. Firstly, it is clear that radiation poses a threat to digital communication systems in the form of SEUs. The investigations [19, 27, 18] have demonstrated that core components, the VTRx+ and lpGBT, of the EoS card are susceptible to SEUs in the presence of neutron and heavy ion irradiation. Secondly, SEU sensitivity can be influenced by the power supply voltage level, as seen in [50, 51]. Furthermore, power supply noise has been shown [59, 60] to impact the performance of the lpGBT and poses a risk to reliable operation. This project will investigate these findings with respect to the EoS card as a whole system, building upon the results from the individual components. The SEU susceptibility of the VTRx+ will be further characterized in the presence of a relatively low energy neutron source. Moreover, these tests will also incorporate an analysis of the SEU sensitivity when operating at lower supply voltages. Lastly, the performance of the EoS card will be investigated in response to power supply noise

Chapter 3

Development of Research

This chapter introduces a number of key components used to implement the experiments. Starting with an overview of how a baseline BER test is carried out and the equipment involved. This is followed by descriptions of the hardware and software implementations used to facilitate these tests.

3.1 The BER Test Setup

The BER test set-up used in this project leverages the FPGA-EoS testing framework developed at DESY. In this framework, a Xilinx KC705 evaluation board (hosting a Kintex-7 FPGA) is used to interface with the EoS card via an optical link and I2C connection. This set-up supports one TX and one RX channel for the uplink and downlink optical transmissions, respectively. The EoS card is configured using commands sent from the FPGA over I2C. Due to the lpGBT I2C signals operating at 1.2 V and the FPGA at 3.3 V, a level converter card is used to translate between the two different voltage levels. A control PC connected to the FPGA via UART is responsible for controlling the FPGA, directing the various interactions with the EoS card, monitoring the EoS card's status and reporting test results. A bench-top power supply unit (PSU) provides the 1.2 V and 2.5 V supply lines to power the EoS card. The following images illustrate this test set-up, with Figure 3.1 depicting a simplified diagram of the equipment involved, and Figure 3.2 displaying a picture of the test set-up in the lab.

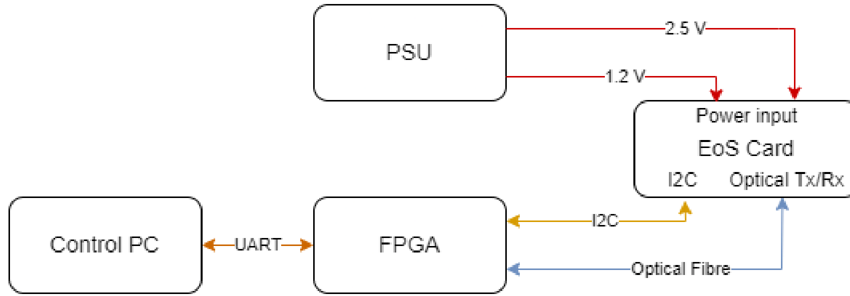


Figure 3.1: Simplified diagram of the BER test setup.

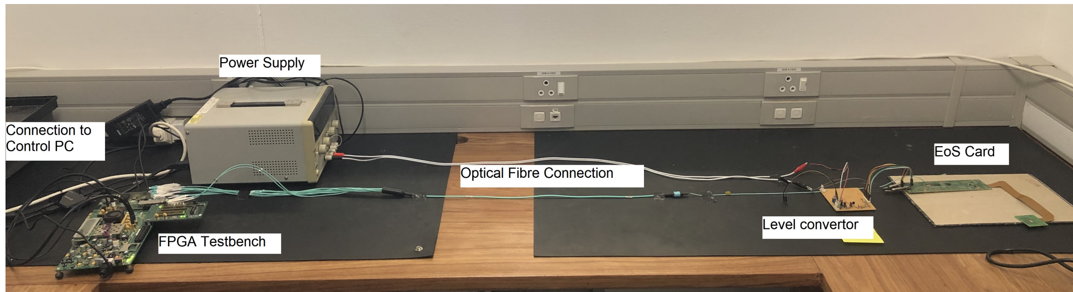


Figure 3.2: BER test set-up at UCT.

The BER tests being run at DESY make use of the E-link connections on the EoS card in order to implement a full loop-back test. The uplink BER test involves the FPGA writing data to the E-links on the EoS card, which is then processed by the lpGBT and sent on the uplink optical channel back to the FPGA. The downlink BER test is performed in the reverse direction, with the FPGA sending data on the downlink and reading it back on the E-links. Due to equipment constraints, it was not possible to implement the E-link connections at UCT and an alternative BER test set-up was implemented.

The alternative setup makes use of the constant pattern generator within the lpGBT to provide the uplink test data, instead of using the data received by the E-links. A full loop-back implementation using the TX and RX optical links was investigated but due to the asymmetric data rates (10.24 Gbps uplink, 2.56 Gbps downlink), this proved to be unsuitable. A BER test is carried out by the lpGBT transmitting a constant pattern to the FPGA over the uplink channel. The FPGA decodes and compares the received data to the expected bit pattern, recording any discrepancies in the compared patterns as bit errors. The final BER calculation, as shown in Equation 2.1, is made by dividing the total number of bit errors by the total number of bits transmitted. While the FPGA is receiving data on the uplink channel, it is also transmitting a repeated alternating sequence of '1's and '0's, using a pattern generator, on the downlink which the lpGBT uses to recover the clock.

The alternative setup built at UCT also included a number of new features that were developed for the purpose of this MSc. The first new addition was the ability to extract eye diagrams of the uplink optical signal using the FPGA testbench. This functionality allowed for evaluating the optical signal quality without the need of a high-end optical oscilloscope. This feature made it possible to measure the impact of the VTRx+ configuration settings. In conjunction with the eye diagram firmware I developed, elaborated on in section 3.3, further contributions were made to in establishing communication with the VTRx+. As this component has no direct communication with the testbench, the lpGBT is used as an I2C proxy in programming the VTRx+. The I2C commands destined for the VTRx+ have to be loaded into the appropriate "I2C master" [61] registers on the lpGBT, before initiating an I2C transaction between the lpGBT and VTRx+. This process was implemented as a custom module in Labview at UCT before being integrated into the DESY setup to streamline the VTRx+ interaction, more on this in section 3.4. In order to carry out the BER tests in the presence of power supply noise, additional test equipment was required in order to simulate the power supply noise. Without access to the appropriate commercial test equipment, I built a substitute with the components available to me capable of injecting an AC waveform onto a DC supply line, effectively simulating a noisy DC power supply. This contribution is reported on in section 3.6.

3.2 FPGA Firmware

The EoS design team at DESY have developed extensive FPGA firmware to carry out functional tests on the EoS card. A control PC is used to interact with the firmware over UART and manage the communication with the EoS. A schematic of the primary modules involved in the BER test are depicted in Figure 3.3 and their functions are described in the following paragraphs.

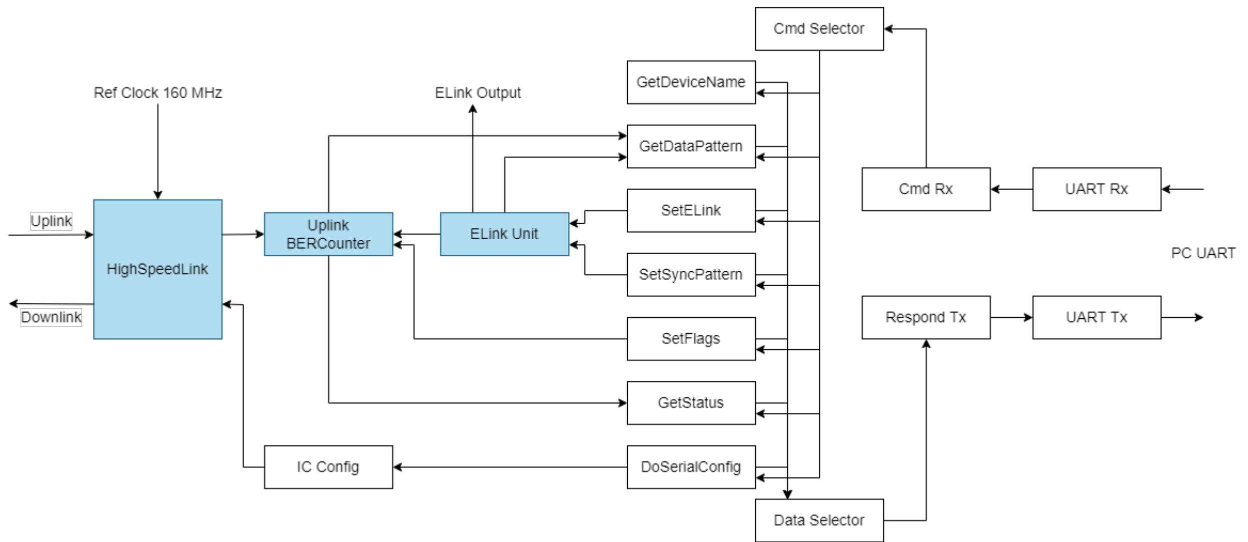


Figure 3.3: A simplified schematic of the firmware and modules used to run the BER test. The key modules used in running the tests are highlighted and the full schematic can be seen in Appendix A.1.

High-Speed Link This module implements the GBT line coding scheme, integrating IP blocks from the lpGBT design team [62] to handle of the scrambler, interleaver, and encoder processes in the downlink direction, and their counter parts performing the reverse operations on the uplink path. These modules can be seen in the block diagram in Figure 3.4.

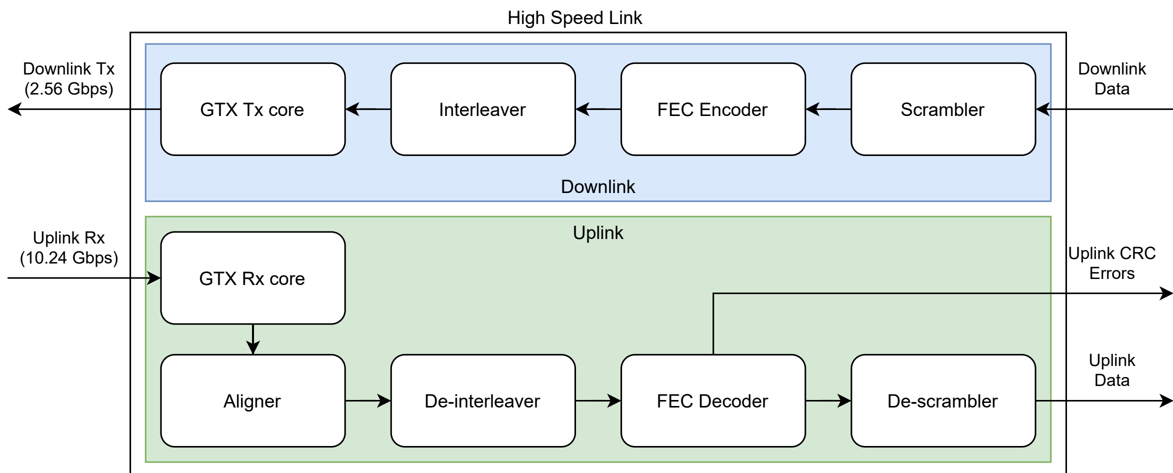


Figure 3.4: Block diagram of the high-speed link module implementation.

The GTX Tx and Rx core modules are built using a custom HDL wrapper generated by the Xilinx 7 series FPGA Transceiver Wizard. The wrapper is used to instantiate the transceiver interface with a configuration compatible with the GBT protocol. The aligner

module originates from the lpGBT design team IP blocks, as well, but is only present on the uplink data path as it is responsible for locking onto the received data frames and distinguishing one data frame from the next. The FEC decoder block can be seen to have two outputs, one passing on the decoded data to the de-scrambler, while the other (labelled Uplink CRC Errors) is used to track how many bit errors were corrected by the decoding process.

Uplink BER Counter This module is responsible for comparing the uplink data with the expected data and recording any errors encountered. The expected data pattern is received from the Elink Unit and a bit-wise XOR comparison is made with the received data to determine how many errors occurred. When a bit error is encountered, this module stores the first 32 bytes of the erroneous data, which can be read out via the GetDataPattern. This is an important feature as the expected data pattern and the received data are often received out-of-sync, requiring the expected pattern to be bit shifted or "delayed" to match the received data. Additionally, the number of misaligned frames and errors corrected by the decoder are also tracked by this module.

Elink Unit This module is in charge of generating the data pattern to be sent out over the E-links, which is also the data pattern used to perform the bit error comparison. The data pattern generated is controlled via the SetSyncPattern module. In addition, the Elink Unit also takes care of delaying the expected data pattern sent to the BER counter. The delay is implemented through a programmable bit shift, as seen in Figure 3.5, which is set via the SetElink module.

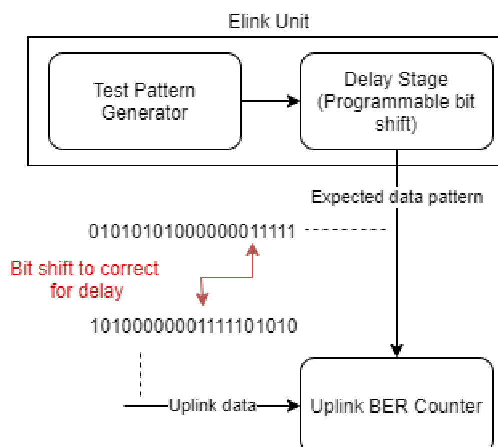


Figure 3.5: Illustration of the delay between the expected data and received data.

DoSerialConfig This module handles the configuration commands sent to the lpGBT. In the schematic shown in Figure 3.3, this module connects to the IC Config block, which embeds the configuration commands into the internal control (IC) field of the uplink data

frame. However, the lpGBT requires a minimal configuration to be programmed before it can use the optical link and IC channel. Therefore, this module also supports I2C communication with the lpGBT and the user can select which communication means to use.

3.3 Eye Diagram Firmware

In order to evaluate the quality of the optical signal beyond BER tests and without an optical oscilloscope, I created a novel piece of firmware to extract eye diagrams using an FPGA. The code designed and implemented to achieve this functionality, as well as documentation detailing the operation of and interaction with the firmware, can be found at the following link: online repository. The rest of this section describes the operation of this firmware and how it was implemented.

This firmware is based on the "RX Margin Analysis" feature covered in the FPGA's GTX transceiver documentation [63], which describes an RX eye scan mechanism for measuring and visualizing the received optical signal after equalization. This eye scan functionality allows for an eye diagram to be captured on a live system without affecting the link integrity or requiring predetermined knowledge of the data pattern being transmitted. The resulting eye diagram often appears smaller than traditional oscilloscope eye diagrams as very low probability jitter and noise is more prominent due to the greater number of samples used in the FPGA. As seen in Figure 3.6, where the left image is representative of an oscilloscope view while the right depicts the eye diagram produced by an FPGA.

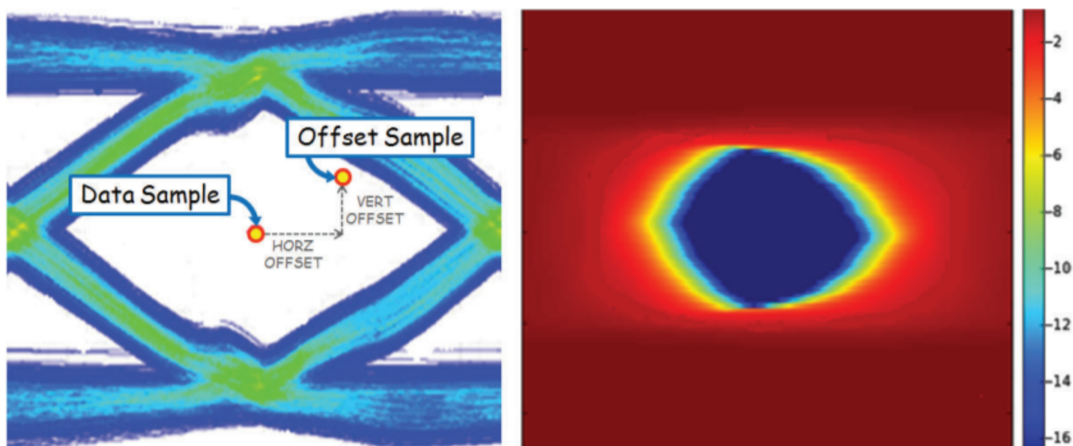


Figure 3.6: **Left**: Illustration of an Offset Sample and Data Sample used to calculate a BER. **Right**: Example eye diagram produced from multiple BER measurements, where the colour corresponds to the logarithmic BER measured. [63]

The optical signal is converted into a differential waveform and undergoes equalization in the FPGA's receiver. Following this, the received data is recovered from the waveform by sampling at a horizontal position determined by the CDR mechanism and a vertical position equal to differential zero. This is referred to as the data sample and can be seen in Figure 3.6. An additional sampler is used to capture an offset sample at a programmable horizontal and vertical offset from the data sample point.

A single eye scan involves accumulating numerous data samples (sample count) and the number of times that the offset sample disagreed with the data sample (error count). The BER at the programmed offset is then calculated as the ratio of the error count to the sample count. These BER measurements are repeated for the full array of horizontal and vertical offsets to produce the BER map as shown in Figure 3.6, where a colour map is produced from the BER measurements in logarithmic scale. A block diagram of this process is depicted in Figure 3.7. The following subsections elaborate on this methodology.

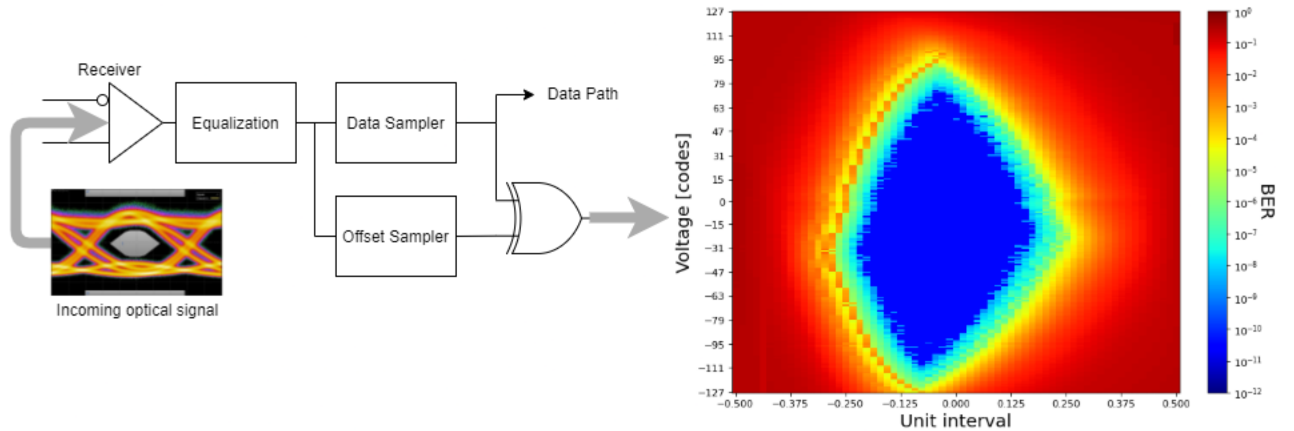


Figure 3.7: Block diagram depicting the process used to generate an eye diagram using an FPGA.

3.3.1 Equalization

The equalization processes mentioned here play an important role in supporting high-speed communication by overcoming channel attenuation. At high line rates, the eye diagram of a received signal can appear completely closed even through the eye measured after the receiver equalization is open. Capturing eye diagrams post-equalization provides additional insight into the signal quality and can aid in identifying sources of noise beyond the correction ability of the equalizer.

The received optical signal is converted into a differential waveform by a PIN diode in the

receiver. This waveform then undergoes the equalization process, which in this project consists of a Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE). As the optical signal propagates through the optical fibre, it experiences attenuation which results in a distorted version of the input signal appearing at the output. The CTLE is responsible for counteracting the attenuation caused by the channel's transfer function, which typically resembles a low-pass filter. This is accomplished through amplification, often taking the form of a high-pass filter to compensate for the attenuated frequencies.

The DFE is used to reduce inter-symbol interference (ISI). When pulses are transmitted along the optical fibre, they do not instantly transition between '1' and '0' values and have to build up or fall down to reach these magnitudes, as indicated by the rise and fall times. This intermediate phase results in pulses of magnitudes between the '1' and '0' signal amplitudes being sent along the channel and are referred to as postcursors (artefacts occurring after the main pulse) and precursors (artefacts building up to the main pulse). These cursors have the potential of interfering with the sampling of adjacent pulses and contributing to ISI. DFE attempts to combat this problem through feedback FIR filters. By determining the magnitude of the post-cursors at different intervals between samples, corresponding filter coefficients can be set to minimize the effect of the post-cursors on subsequent pulses.

3.3.2 Sampling

To construct the statistical eye diagram, a BER needs to be calculated for each horizontal and vertical offset. The horizontal axis corresponds to the unit interval (UI) of the uplink channel, which for a 10.24 Gbps channel is 1 UI = 97.7 ps. There are 65 intervals, between -0.5 UI and 0.5 UI, on the horizontal axis each corresponding to a 1.5 ps delay or advance in the sampling time of the offset samples relative to the data samples. The vertical axis represents the differential voltage level and is expressed in voltage codes ranging from -127 (minimum) to 127 (maximum). An illustration of the relationship between the Data Sample and Offset Sample can be seen in Figure 3.8.

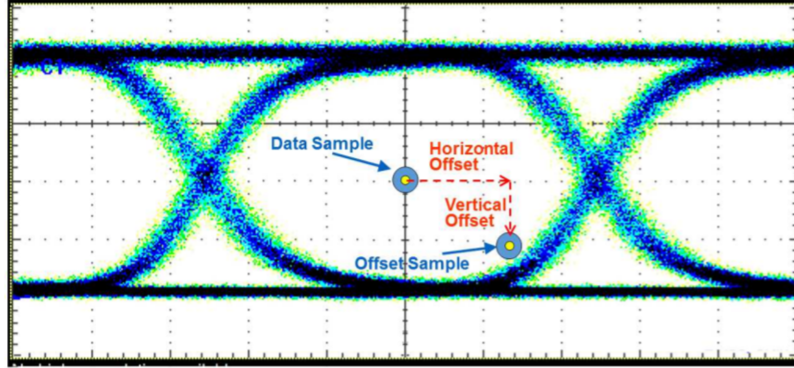


Figure 3.8: Illustration of a Data and Offset Sample used to calculate a BER, as seen in [37].

Each time an eye scan is performed, data samples and offset samples are accumulated for the programmed offset. The number of samples, and errors found from a disagreement between offset and data sample, are tracked by a sample and error counter, respectively. These counters are 16 bits wide (maximum value of 65535) and trigger the end of the eye scan when either counter is saturated. The number of bits sampled in one scan is equal to the sample counter times the bus width (32 bits), which corresponds to a maximum BER measurement of 4.8x10^{-7}. This measurement is improved more than twofold with the addition of a prescaler, where the number of bits sampled now corresponds to:

$$bits\,sampled = sample\,counter \times bus\,width \times 2^{(1+prescale)} \tag{3.1}$$

The prescale register is 5 bits wide, corresponding to a maximum value of 31, and this equates to a maximum of 9.0x10^{15} bits that can be sampled, allowing for BER measurements down to 10^{-15}.

However, with a high prescale value, when determining the BER for the edge regions of the eye (BER $>10^{-5}$), the error counter is likely to saturate before sample counter increments past 0, resulting in a divide by zero error. To overcome this, the prescale value needs to be adjusted dynamically. This was implemented in the firmware by updating the prescale value based on the error count from the previous scan. To facilitate this dynamic shifting, a number of parameters are required before starting the scan:

- Max Prescale - sets the maximum prescale value for the eye scan. This limits the maximum BER that can be measured and influences the execution time.
- Step Prescale - sets the step size used to increment or decrement the prescale value. Determines the BER gradient between successive measurements in the final eye diagram and also influences execution time.

- Error Threshold - Defines the upper and lower limits of an acceptable error count. Determines whether the error count is too large or small, and updates the prescale value accordingly.

After a scan has been run, the error count is compared against the error threshold. If too many errors were encountered, the prescale is decreased, in proportion to the number of errors, for the next scan. This optimizes the scan time as only a few errors are needed to provide an accurate BER measurement (accumulating 65535 errors at 10 Gbps with a BER of 10^{-9} takes 109 minutes for one horizontal and vertical offset, while 10 errors take 1 second).

If too few errors were encountered, the prescale value is increased and the scan is repeated at the same offset location. If the prescale value is already at the maximum, the offsets are incremented and the next scan is carried out.

3.3.3 Eye Scan Algorithm and Readout

To carry out the operations described in the previous section (incrementing the offsets, adjusting the prescale value, storing the scan data, etc.) an algorithm was designed to interact with the eye scan hardware and support reading out the data over the UART interface. The eye scan hardware is controlled by writing to and reading from various attributes made available through the dynamic reconfiguration port (DRP) of the GTX Rx core. This module is shown in Figure 3.4 and the eye scan algorithm is integrated as a sub-module running in parallel to the normal Rx operations. To facilitate reading out the data over UART, without blocking other UART commands during the scan, all relevant scan data is stored in BRAM and only read out once the full eye has been scanned. The algorithm is implemented as a state machine, as depicted in Figure 3.9, with the states described in the following paragraphs.

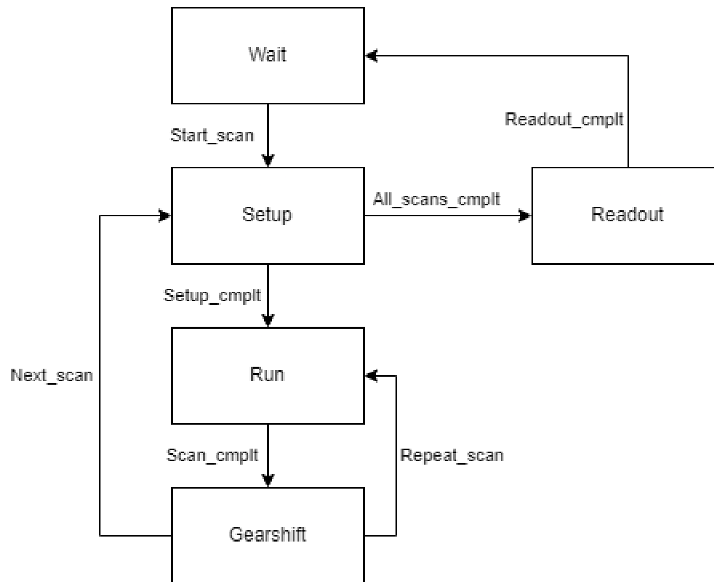


Figure 3.9: Eye scan state machine.

- **Wait** - The default state of the algorithm, initializes all parameters in preparation to start a scan. Returns to this state after the full eye has been scanned. Moves to the Setup state when a scan is started.

- **Setup** - This state sets the horizontal and vertical offsets for the current scan, as well as updates the prescale value, by writing to the corresponding attributes. Simultaneously, these settings are also stored in BRAM. Signals the end of the eye scan when all offsets have been captured and return to the Wait state. Moves to the Run state when all attributes have been set.

- **Run** - This state starts the scan at the programmed offsets. Polls the DRP status attribute to monitor for scan completion, at which point it begins reading out the sample and error count. These readings are stored in BRAM before moving into the Gearshift state.

- **Gearshift** - This state manages the dynamic prescale adjustment. The error count is compared against the threshold parameters and the prescale is adjusted if necessary. Should a scan need to be repeated, the new prescale value is written to the appropriate attribute and the algorithm returns to the Run state, overwriting the previous scan's data in BRAM. Returns to the Setup state to move on to the next scan.

- **Readout** - Once the scan has completed, a UART command triggers this state which starts the data readout process from BRAM. Due to the UART frame size being a maximum of 508 bytes and the eye scan data taking up 265,200 bytes, a series of interactions is used to perform this readout.

The readout process was developed to be compatible with the Labview control application. This meant that the readout module had to operate as an asynchronous process, allowing the Labview program to issue commands when necessary and otherwise continue its usual process execution without waiting for a response from the readout. To achieve this, a number of status bits are used to indicate the start/end of various steps in the readout. This process is illustrated in the sequence diagram seen in Figure 3.10

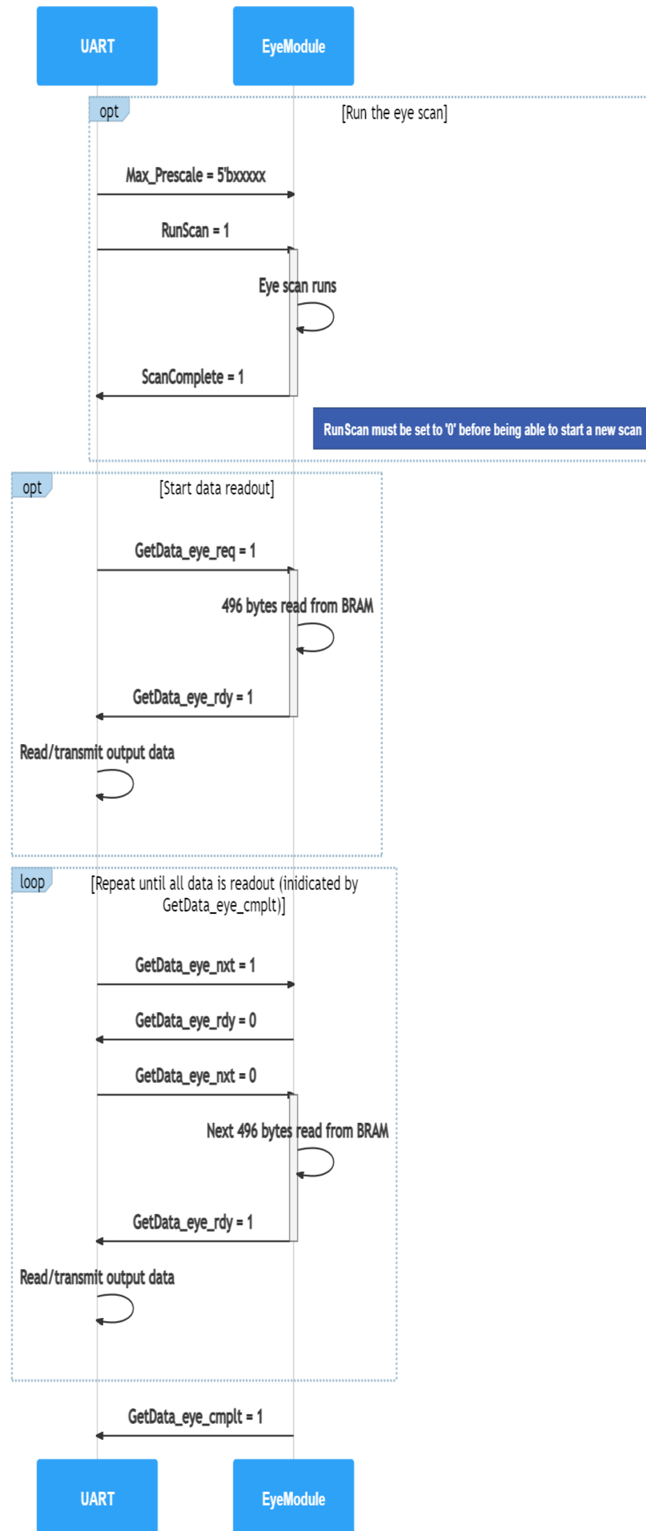


Figure 3.10: Sequence diagram illustrating the UART and eye scan module interactions in reading out the data.

Once the data has been read out, a final processing step is required before the eye diagram can be plotted. This involves iterating through the offsets and calculating the BER, which

is the error count divided by the total number of bits sampled (Equation 3.1), for each point in the diagram. Finally, the BER data corresponding to different locations in the eye diagram can be plotted as a heatmap, producing the eye diagram shown in Figure 3.11. This firmware was verified as working correctly in a controlled lab environment at DESY where the engineers had access to an optical oscilloscope capable of producing commercial eye diagrams. A pseudo-random signal was generated on the FPGA board at 10.24 Gbps and used in a loop-back test where both the optical oscilloscope and FPGA firmware were used to generate eye diagrams. These tests were run several times and while the oscilloscope produced higher resolution eye diagrams, it was reported that the both eye diagrams showed a distinct correlation as the signal quality was attenuated, thus verifying the eye diagrams produced by the FPGA firmware.

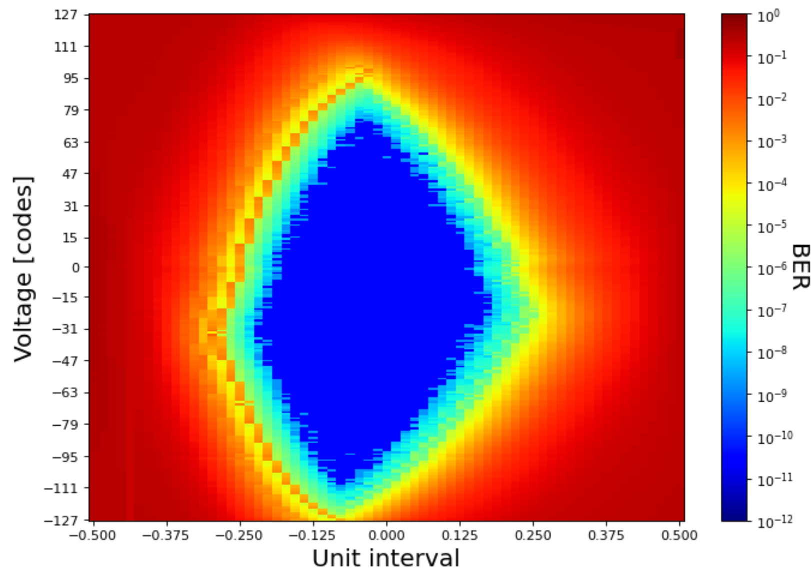


Figure 3.11: Example eye diagram after readout and post-processing.

3.4 Labview Software

The test framework developed by DESY uses a Labview application to manage the test equipment (FPGA, power supply, temperature chamber, etc.) and carry out various tests. The application allows for configuration text files to be imported, detailing what tests to be run and how to set up the hardware, enabling an automated testing workflow. A data logging feature records and saves the results from the tests into text files on the control PC. A robust GUI, displayed in Figure 3.12, provides a simple method of monitoring the tests and manually interacting with the equipment.

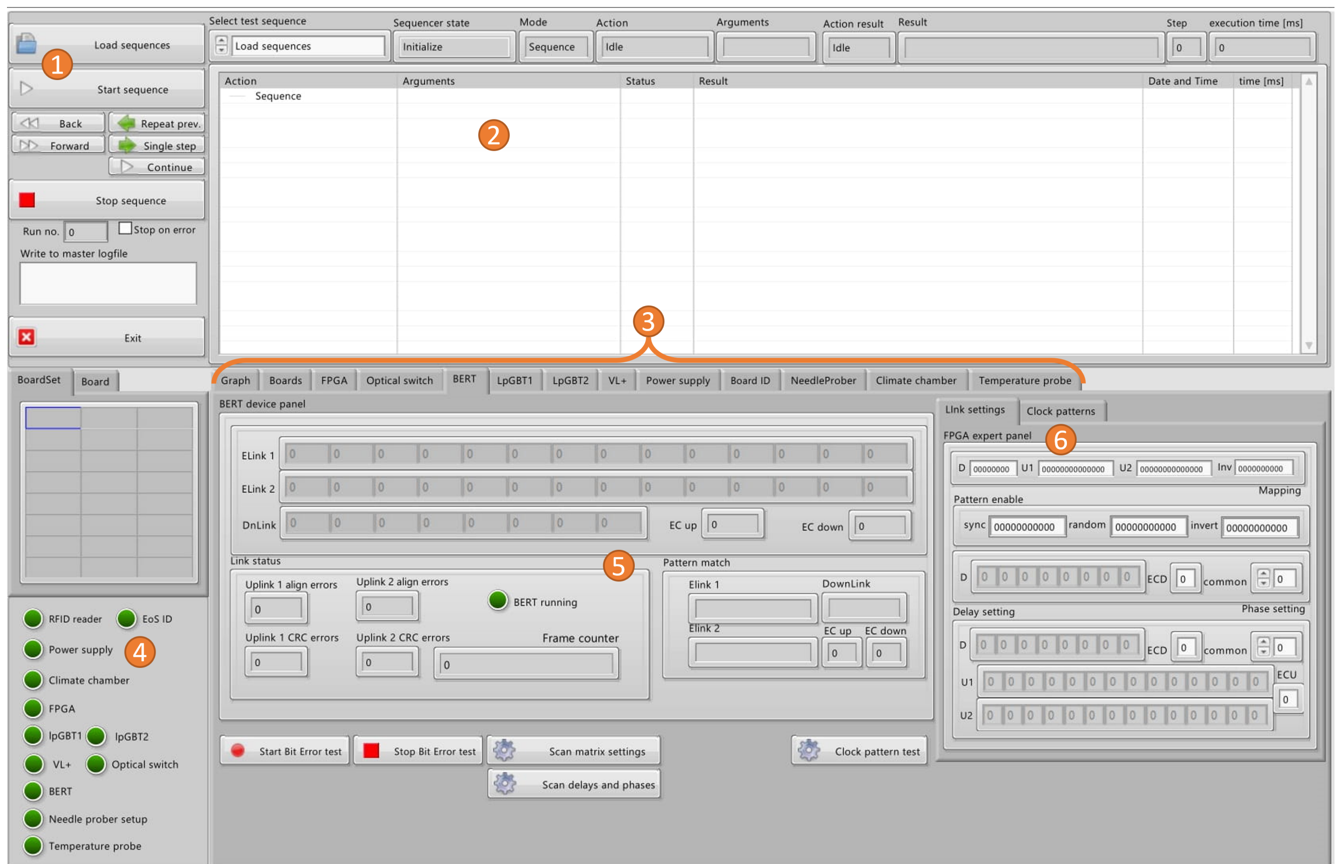


Figure 3.12: Screenshot of the BER testing control panel from the Labview application.

The annotated features in Figure 3.12 are described here:

1. The "Load sequences" and "Start sequence" buttons are used to import and execute a series of commands from a text file. The Labview application supports a variety of commands, from low-level hardware interaction specifying the device, communication protocol and command to send, all the way to high-level commands that will execute a pre-programmed series of steps and carry out specified tests.

2. This panel lists the commands that have been loaded, the arguments of the commands, current execution status and the results from the executed command.

3. The tabs seen here are used to navigate between different device control panels. The control panels most used were she lpGBT1 and VL+ (referring to the VTRx+) tabs which provide register lists used for writing to and reading from the configuration registers of the two components. Further contributions to the DESY setup included work on the I2C interaction between the lpGBT and the VTRx+. As there is no direct communication between the testbench and the VTRx+, the lpGBT had to be used as a proxy in relaying I2C commands. This communication process is

explained in [61], and after a successful implementation at UCT, the same process was integrated into the DESY setup, providing streamlined interactions with the VTRx+ registers. In this screenshot, the "BERT" tab is selected and the bit error rate test (BERT) device panel is displayed.

4. The LEDs displayed here indicate the status of the associated devices. The LED will light up if Labview is able to communicate with the device.

5. The BERT device panel contains all the information associated with running a BER test. Starting at the top of the panel, the number arrays detail the bit error count for individual E-links as well as counters for the EC up and EC down fields. Below the top panels are the link status and pattern match panels. The link status panel provides counters for the align and CRC errors for each uplink channel as well as a frame counter and LED to indicate if a BERT is running. The pattern match panel displays the results from comparing the last 15 data frames for each E-link with the expected data. This is useful for troubleshooting the connection and determining if the link settings are correct.

6. The link settings panel allows for configuring the expected data pattern and the programmed delay on the bit error counter for each E-link.

3.5 Level Converter Card

Due to the I2C interface on the lpGBT operating at 1.2 V and the FPGA's operating at 3.3 V, a level converter card was used to translate between the two voltage levels. An initial converter circuit, shown in Appendix A.2, was used to interface with the EoS card in the beginning. However, the circuit suffered from slow signal transition (rise and fall) times which resulted in an unstable I2C connection. The engineers at DESY ended up designing an improved converter circuit, depicted in Figure 3.13. This circuit proved invaluable as 1.2 V to 3.3 V level converters were not readily available in South Africa at the time of the experiment.

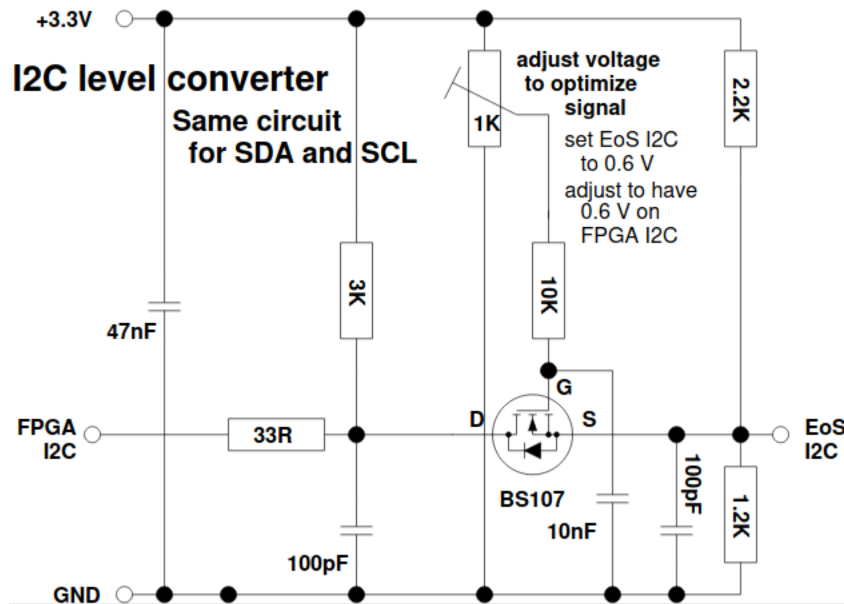


Figure 3.13: Circuit schematic of the level converter.

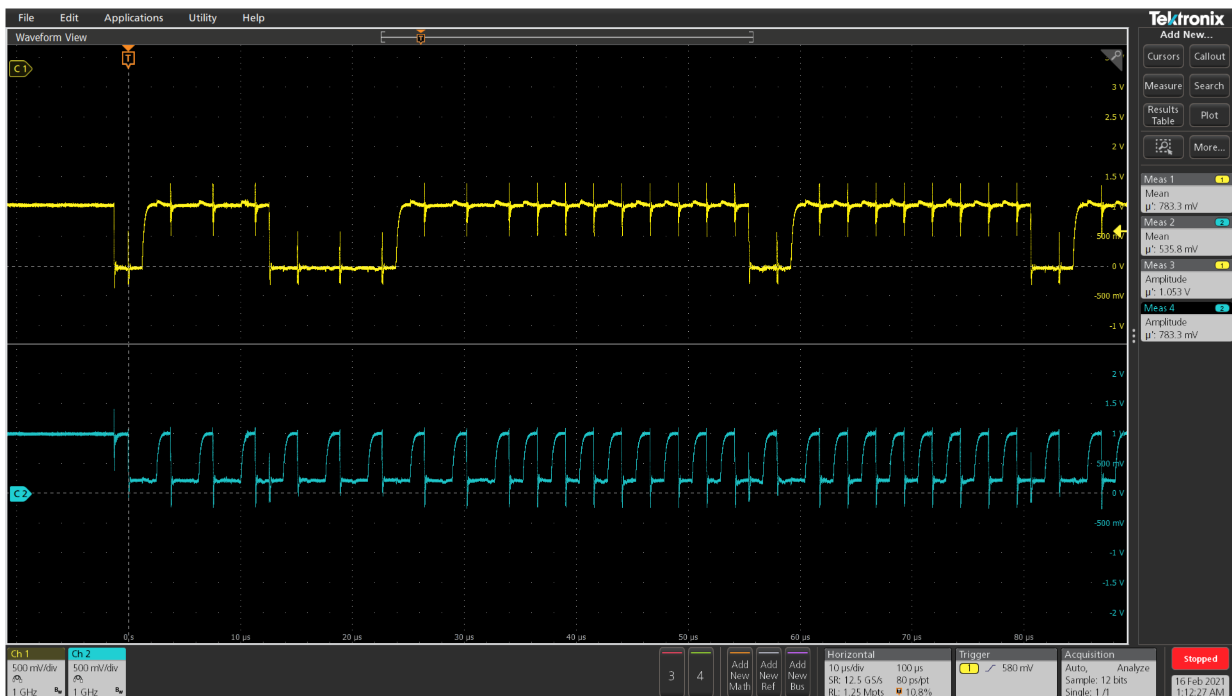


Figure 3.14: Oscilloscope screenshot of the un-optimized I2C signal at the output of the level converter card.

The new level converter circuit required fine-tuning as the capacitance load from the lpGBT, FPGA, cables and traces degraded the signal shape, as can be seen in Figure 3.14. This was carried out by observing the I2C signal output on each side of the circuit and adjusting the potentiometer until an optimal signal shape was achieved. The optimised I2C signal can be seen in Figure 3.15, where the logic analyser feature on the oscilloscope

is being used to ensure the commands are readable. The top two traces are monitoring the power supply lines, while the following two traces display the I2C data and clock lines, respectively. Below this is the logic analyser bus which can be seen decoding the I2C signal into hexadecimal data.

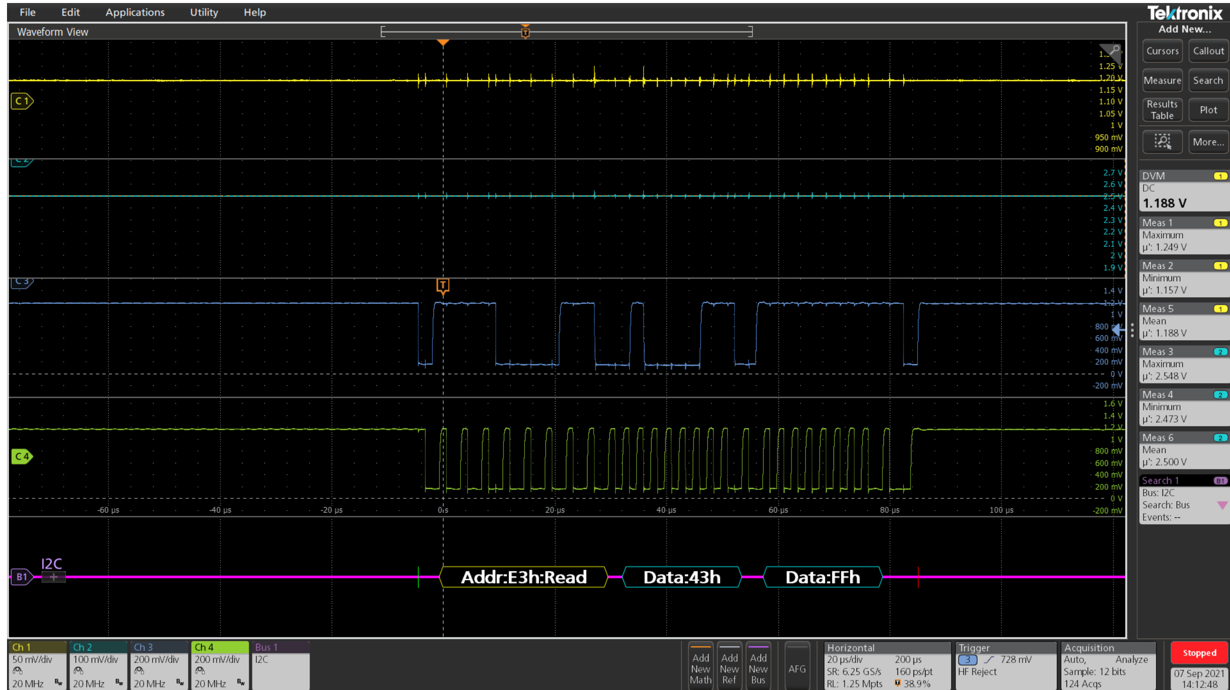


Figure 3.15: A screenshot from an oscilloscope of the optimized I2C signal.

3.6 Simulating Power Supply Noise

In order to investigate the influence of power-supply fluctuations on the EoS card's performance, a method for simulating electrical noise on the DC power supply was required. The initial supply noise investigation was carried out at DESY [20] made use of a Keysight N6705C power supply which supported outputting voltages with magnitudes following a sinusoidal waveform pattern up to 10 kHz. The power supplies available for this experiment did not support a waveform generation feature beyond 1 Hz, therefore an alternative solution was devised using a function generator, op-amp and a n-type power MOSFET to create the circuit seen in Figure 3.16.

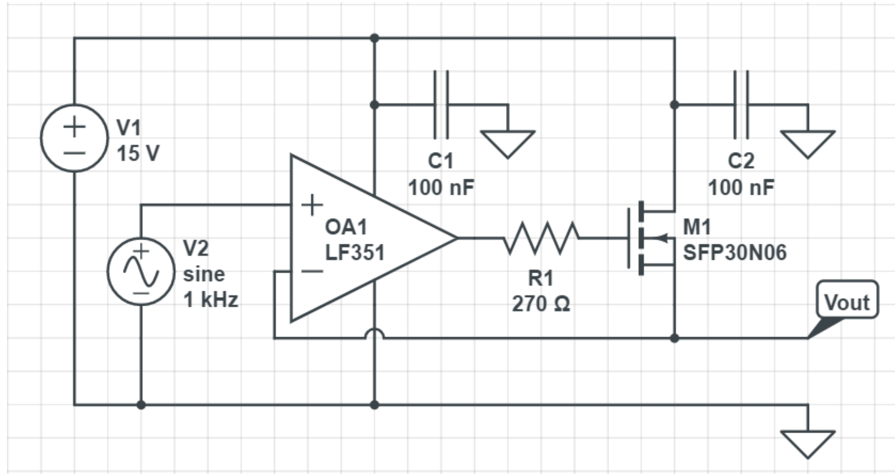


Figure 3.16: Circuit used to superimpose AC "noise" signals onto a DC supply.

The circuit uses the power MOSFET (M1) as a variable resistor between the DC supply (V1) and the load (Vout). The MOSFET's drain to source resistance is varied to modulate the DC level at the output with the noise signal from V2 (function generator on the MSO64B Tektronix Oscilloscope). The MOSFET output being fed back to the inverting input of the op-amp causes the op-amp to drive the MOSFET's gate such that the amplitude level at its output is the same as the amplitude on the non-inverting input (the AC-noise signal). The DC power supply is set to 15 V in order to keep the MOSFET biased and provide suitable input power to the op-amp. The DC component of the output is controlled by the DC offset of the function generator, allowing the circuit to be used in testing the 1.2 V and 2.5 V inputs separately.

As mentioned in section 2.4, power supply noise comes in many forms and often resembles a random sequence of fluctuations on the voltage line. To provide as much variation in the simulated noise as possible, 4 AC signals supported by the function generator were used in this test. These are the sine, ramp, sinc (sine(x)/x) and square waveforms. These waveforms were observed on the circuit's output, with no load connected, reaching bandwidths of 1 MHz. Beyond 1 MHz the output waveform is constrained by the slew rate, rise time and fall time parameters of the SFP30N06 MOSFET and LF351 op-amp, which resulted in clipping of the peak to peak voltage of the output waveform.

Before connecting this circuit to the EoS card, a preliminary test was carried out using the load feature on the PSU. This allowed the PSU to act as the DUT, where the current draw could be set to the maximum current consumption of the EoS card (300 mA) and the output voltage could be observed on the oscilloscope. The output waveforms maintained the peak to peak voltage levels up to a frequency of 100 kHz. Beyond this, the waveforms started exhibiting erratic behaviour, with random fluctuations in the voltage

level. It was noted that at frequencies greater than 100 kHz, while sourcing 300mA, the MOSFET's heatsink was reaching significantly high temperatures (enough to melt the plastic on nearby wires). This extreme increase in temperature and erratic output waveform is believed to be due to the MOSFET being unable to keep up with the output waveforms rise and fall times required at these high frequencies. Therefore, the decision was made to limit the upper frequency of the noise tests to 99 kHz, to prevent any chance of permanently damaging the EoS card.

Chapter 4

Methodology

This chapter describes the tests carried out in pursuance of this project's objectives. In order to investigate the sensitivity of the VTRx+ to SEUs, BER tests were run with the EoS card exposed to irradiation where erroneous bits are brought about by SEUs. In addition to the irradiation tests, baseline BER tests are also carried out to verify the stability of the test setup and to be able to distinguish between errors caused by SEUs and those due to ambient noise.

To characterize the performance of the EoS card in response to an irregular power supply, the BER was observed over a series of tests where the power supply was manipulated. The first set of tests involved lowering the nominal supply voltage on the 1.2 V and 2.5 V supply rails to determine the supply voltage operating margin before errors were encountered. The second set of tests consisted of generating ”noise” on the 1.2 V and 2.5 V supply lines by superimposing AC waveforms onto the DC lines. The AC waveforms were of a fixed amplitude and the BER was measured over various frequencies to cover a range of possible noise sources.

The optical signal quality was studied across a range of VTRx+ configuration parameters in order to determine the impact and optimal values of the bias and modulation current. As the optical signal quality can only be coarsely inferred from a BER test, several eye diagrams were generated over a range of configuration settings. The eye diagrams allow for a visual evaluation of the signal quality and can be used to extract eye height and width measurements to quantify the change in signal quality. The following sections elaborate on the tests described here.

When making BER measurements, there is a trade-off between test time and accuracy.

This is often addressed in literature by reporting BER test results with respect to a specific confidence level (CL). The relationship between the CL and the measurement time (T) required for a given BER is expressed in the following equation [64]:

$$T = -\frac{ln(1 - CL)}{BER * R} + \frac{ln(\sum_{k=0}^{N} \frac{(n*BER)^k}{k!})}{BER * R} \tag{4.1}$$

where R is the line rate, n is the total number of bits transmitted and N is the number of errors encountered. Table 4.1lists test times for given BER at different confidence levels. The entries are calculated using a data rate of 10.24 Gbps and assume no errors are encountered.

CL (%)	**10^{-11}** (s)	**10^{-12}** (m:s)	**10^{-13}** (m:s)	**10^{-14}** (h:m:s)	**10^{-15}** (h:m:s)
80	7.81	1:18	13:01	2:10:13	21:42:05
85	8.30	1:23	13:50	2:18:21	23:03:28
90	8.79	1:28	14:39	2:26:29	24:24:51
95	9.28	1:33	15:28	2:34:37	25:46:13
96	9.38	1:34	15:38	2:36:15	26:02:30
97	9.47	1:35	15:47	2:37:53	26:18:47
98	9.57	1:36	15:57	2:39:30	26:35:03
99	9.67	1:37	16:07	2:41:08	26:51:20

Table 4.1: Minimum measurement time required per testing interval for the given confidence level at a data rate of 10.24 Gbps.

It should be noted that this relationship between time and confidence level only holds under the assumption that errors are caused due to random noise. Therefore, the data tabulated in Table 4.1is only applicable to baseline tests where the EoS card is not exposed to additional stimuli that could influence the error rate. However, it should be noted that the test time is reduced when the system has additional stress applied [65]. This follows the assumption of errors being caused by Gaussian noise, and that by reducing the signal level while keeping the noise constant, the SNR will be reduced, resulting in a higher error rate and leading to a shorter test.

4.1 BER Test Design

The baseline BER test follows the extended test setup described in section 3.1, where the FPGA-EoS testing framework developed at DESY is discussed along with the modifications made to extend the testing capabilities, forms the foundation for the proceeding tests. To run the baseline test, the first step involved programming the lpGBT with the minimal register configuration required to operate. Following the initial configuration, the lpGBT is programmed to output the constant pattern $550F550F_{16}$, providing an equal number of 1 and 0 bits. The lpGBT pattern generator allows for a 32-bit pattern to be set, however, only 16 bits are transmitted per clock cycle (due to the lpGBT operating with a 40 MHz clock and processing 640 bits per second). Therefore, a 2 x 16-bit pattern was selected in order for the FPGA firmware to reliably lock onto the transmitted frames. The data path within the lpGBT is depicted in Figure 4.1, along with the uplink pattern generator highlighted.

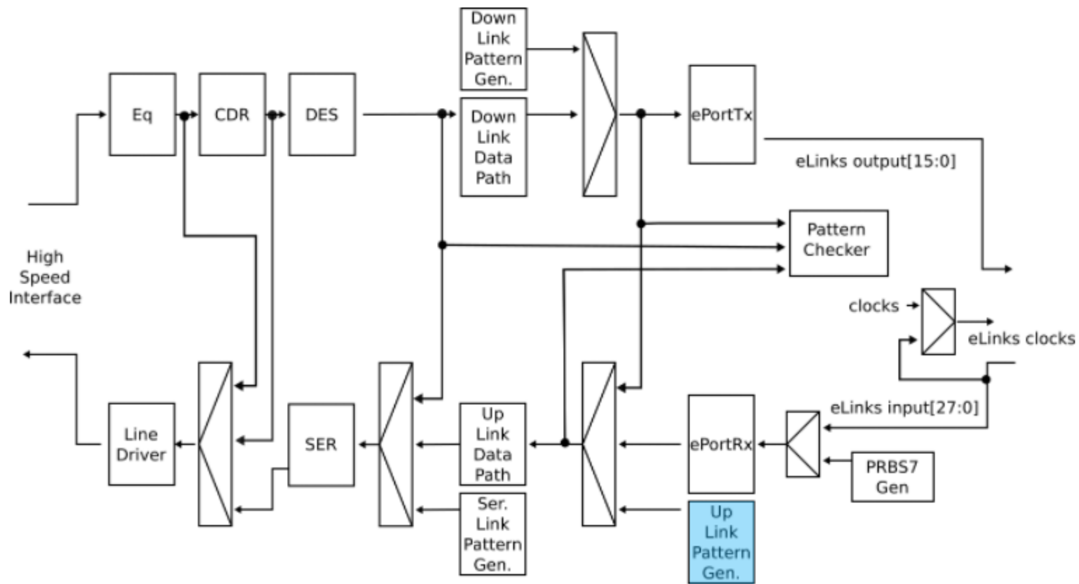


Figure 4.1: lpGBT data path, highlighting the uplink pattern generator used to generate the uplink data and bypass the E-links. Adapted from [61]

The uplink pattern generator allowed the BER tests to bypass the E-links while still making use of the majority of the processing blocks within the lpGBT. It is noted that a pseudo-random binary sequence would have been the better choice of data to use in conducting BER tests to cover a range of possible data patterns. However, this proved to be an unavoidable component limitation but not significant enough to invalidate the test results.

Following the configuration of the lpGBT, the FPGA is configured next. This involved setting the expected data pattern in the Elink unit via the SetSyncPattern command, mentioned in section 3.2. After the fixed pattern is set, the Elink unit is set to operate in a synchronous mode where the data received on the uplink is deserialized and assigned to the corresponding E-link. The uplink BER counter then compares the expected data pattern on each E-link to the received data. An illustration of the uplink BER test is shown in Figure 4.2, focusing on the steps described.

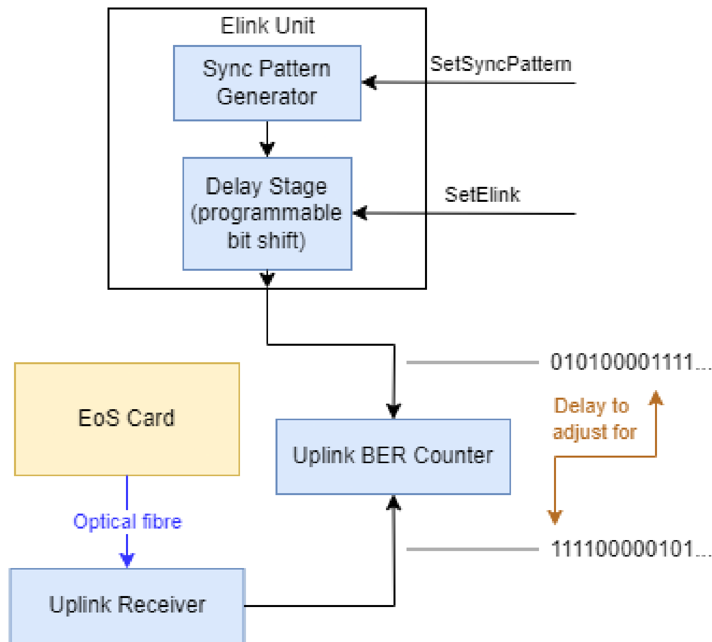


Figure 4.2: Configuring the Elink unit for an uplink bit error test without E-links and adjusting for the delay.

If the expected data pattern and received data do not align, as shown in Figure 4.2, the received data is reported as being erroneous. The Elink unit and uplink BER counter store the first 32 bits of the expected data pattern and received data when an error is encountered. The bits can then be read out using the GetDataPattern command in order to determine the extent of the delay. Following this, a bit shift can be set on the expected data pattern, using the SetElink command, to account for the misalignment.

4.1.1 Preparation for Irradiation

The above paragraphs describe the process followed in composing a baseline BER test, however in preparation for the irradiation tests, a few more adjustments were made. First, the TMR feature within the lpGBT and the VTRx+ was disabled. As discussed in section

2.2.5, TMR triplicates the processing blocks and selects the majority output, effectively masking any errors induced by SEUs in one of the processing blocks. To disable the TMR feature, the lpGBT and VTRx+ provide access to configuration registers where the clock for each triplicated branch can be enabled/disabled. When one branch is disabled, it is assumed that the output of this branch maintains the output state it held before being disabled. This means there is a 50% chance that one of the enabled branches experiences an SEU, matches with the disabled branch, and becomes the majority output. This effect can be compensated for by multiplying the number of errors encountered by 2.

The second modification made in preparation for the irradiation tests involved disabling the watchdog feature in the lpGBT. This feature monitors the state of the processing blocks within the lpGBT and should one of these blocks malfunction, the watchdog will reset force a reset on that block. It was noted in the lpGBT documentation [61] that with the watchdog disabled, should an SEU occur, the chip is always able to recover to a functional state. While the chip is recovering a certain number of bit and frame errors are expected. However, with the watchdog enabled, the recovery time after an SEU is extended and results in a greater number of bit and frame errors being reported. This feature is disabled by asserting the appropriate disable bits in the powerup register of lpGBT.

The third and final modification consisted of enabling the SEU counter within the lpGBT's process monitoring block. This is a built-in test feature provided by the lpGBT and monitors for bit-flips within the chip's memory cells. If an upset is detected, the 16-bit SEU counter is incremented and can be read out from the corresponding counter registers. This feature should not be confused with the configuration error counter, which is enabled within the lpGBT by default and monitors for upsets within the configuration memory. Any config errors detected are recorded on separate counter registers. Similarly, the VTRx+ also provides an SEU counter, enabled by default, which monitors for memory cell upsets and can be read out over I2C.

4.1.2 Labview Data Collection

The BER tests are managed by the Labview program developed at DESY, introduced in section 3.4. In addition to handling the configuration process described above in setting up a BER test, the program is also responsible for recording a plethora of data related to the tests. Starting with the bit error test results, the program was configured to record the bit error counters at 10 ms intervals upon starting a test. This consisted of recording

the CRC (correctable), Align and E-link (non-correctable) error counters, as well as the frame counter and a timestamp for each measurement. An explanation for the different error counters is provided in section 5.1.

In addition to the test results, the program also logs the configuration parameters set for the lpGBT and VTRx+. This information is important for ensuring the EoS card has been correctly configured and is used to compare the optical signal quality of the card for different VTRx+ settings. Adding to this, the eye diagram data generated by the FPGA is saved by Labview to a CSV file on the control PC.

4.2 Irradiation Environment

The irradiation tests were designed and carried out in collaboration with the Physics Department at the University of Cape Town. The nuclear research lab in the department provided two options for neutron sources: a 14 MeV mono-energetic neutron beam and a broad spectrum Americium-Beryllium (AmBe) radioisotopic source, reaching maximum energies of approximately 11 MeV. The neutron beam source presented physical challenges due to the beam tunnel diameter being only slightly larger than the width of the EoS card, requiring the card to be positioned on its side with respect to the beamline. This would have limited the fluence experienced by the card as opposed to being positioned with the face of the EoS card (top side) being perpendicular to the beamline. In addition to this, the broad energy spectrum provided by the AmBe made it the better choice for carrying out the irradiation tests. This decision was also supported by previously mentioned literature [23, 24, 32], where a Beryllium target was used to produce broad energy spectrum neutrons in the investigation of SEUs.

Neutrons are generated by the beryllium after absorbing an alpha particle emitted from the americium. The source is contained within a cylindrical capsule housing the two elements and can be seen in Figure 4.5. The neutrons are produced at a rate of 10^5 neutrons per second into 4π steradians (spherically) with an energy distribution following the spectrum depicted in Figure 4.3. From the energy spectrum plot, it can be seen that a majority of the emitted neutrons will be approximately 4 MeV, with a maximum energy of about 11 MeV.

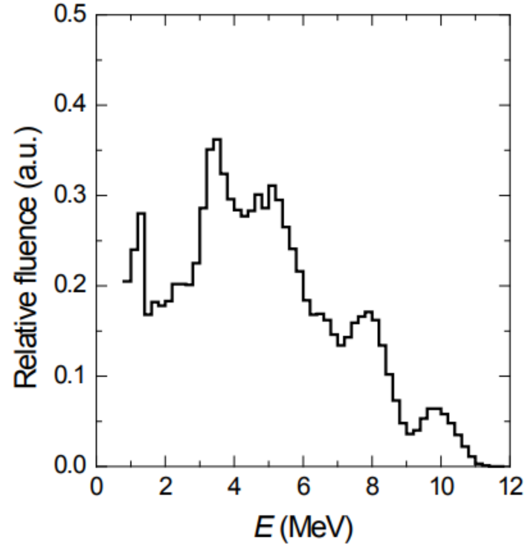


Figure 4.3: Energy spectrum of neutrons emitted by the AmBe source at UCT [66].

In order to compare the results of the irradiation tests and calculate the SEU cross section, the fluence experienced by each DUT was determined. With the source being positioned on top of each component being tested, the distance between the source and DUT is taken to be 1cm. This distance is assumed for simplicity's sake as detailed information on the internal layout of the components' was not available.

The fluence is derived from the flux of neutrons passing through the DUT multiplied by time. The flux of the DUT is calculated following Equation 4.2.

$$Flux_{DUT} = \frac{A_{DUT}}{A_{1cm}} \times Neutrons\ per\ steradian\ per\ second \tag{4.2}$$

Where A_{DUT} is the surface area of the component being irradiated and is divided by A_{1cm} is the surface area of a steradian at 1cm, which results in the steradians subtended by the DUT. It should be noted that only the surface area of the FPGA DIE was available, while the surface area of the VTRx+ and FPGA transceiver was taken from their PCB footprint dimensions as the exact DIE sizes were not publicly available. The AmBe source produces 7958 neutrons per steradian per second, as derived from the neutrons emitted per second into 4π steradians mentioned above. The flux and fluence experienced by each device is tabulated in Table 4.2.

Device	**Dimensions (mm)**	**Flux (neutrons per second)**	**Fluence (neutrons per cm^2)**
FPGA chip	31 x 31	7.65 x 10^4	1.32 x 10^{10}
FPGA transceiver	41.8 x 13.5	4.51 x 10^4	7.79 x 10^9
VTRx+	20 x 10	1.59 x 10^4	2.01 x 10^{10}

Table 4.2: Summary of irradiation experienced by each device

4.3 FPGA Testbench Stability

Before carrying out the SEU susceptibility tests on the EoS card, a preliminary test was conducted on the Xilinx KC705 FPGA board to demonstrate that the FPGA, and subsequent test results, would not be affected by the irradiation. This was a necessary step in ensuring the validity of the proceeding SEU test results as the KC705 board has been shown to experience SEUs in the presence of a 180 MeV proton beam [67]. It should be noted that this study reported radiation-induced errors with this FPGA in the presence of proton irradiation, but did not test the influence of neutron irradiation and used a source with an energy level beyond a factor of 10 greater than used in this work.

This test made use of two KC705 FPGAs connected via a 5m LC/LC optical fibre cable. The first FPGA was programmed to emulate the uplink data path of the EoS card, from generating and preparing the data to transmitting it over the fibre optic link to the second FPGA. This test setup allowed the second FPGA to run the standard testbench firmware with minor modifications. An image of this test setup with the two FPGAs can be seen in Figure 4.4.

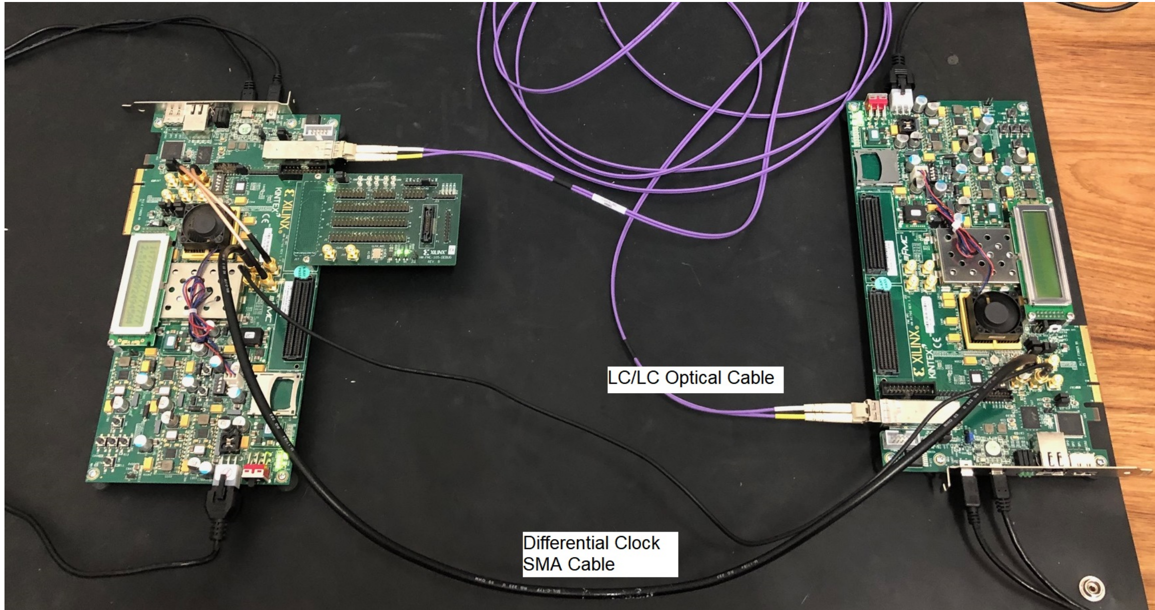


Figure 4.4: FPGA to FPGA BER test setup, with one FPGA emulating the lpGBT.

The firmware for the emulation FPGA was constructed from a mix of the testbench firmware and IP cores provided by CERN. The E-link module from the testbench firmware was re-purposed for data generation in the transmitting FPGA. This was accomplished by adjusting the existing data generation features for the downlink optical channel (2.56 Gbps) to support the uplink channel configuration (10.24 Gbps). Additional changes were made to increase the randomness of the generated data, where the lpGBT was limited to a fixed 64-bit pattern, the emulation FPGA was hard-coded to use 4 x 64-bit patterns. By iterating through the bit patterns, the testbench FPGA was able to receive and process these patterns as normal, with minor adjustments.

Following the data generation, the CERN IP cores were used to implement the scrambling, encoding and interleaving stages of the uplink data path. These stages processed data in an identical manner to the EoS card, but one final modification was required before the test setup was operational. The available IP cores did not provide a mechanism for recovering the clock on the downlink optical signal. To overcome this, a workaround was implemented where the testbench firmware, in addition to generating its own 160 MHz differential clock signal, was programmed to output an identical clock signal on the SMA connectors. This differential signal was then connected to the emulating FPGA over a pair of male/male SMA cables, as seen in Figure 4.4.

Using the FPGA-FPGA test setup described above, BER tests were carried out to ensure the FPGA correctly emulated the lpGBT. These initial tests verified the stability of the test setup, after which the irradiation tests were started. The AmBe source was first

positioned adjacent to the FPGA fan, as shown in Figure 4.5, and BER tests were carried out monitoring for SEUs. The source was positioned here as balancing it on top of the fan proved to be unstable, and due to the source emitting radiation spherically it was determined that the FPGA would still be irradiated during this test, however it should be noted that as a result the fluence calculations shown in Table 4.2 are a maximal estimate. Removing the fan to have better access to the FPGA chip was considered but was decided against due to the risk of damaging the FPGA which could not be replaced in time for future experiments should it fail. A second BER test was conducted with the source positioned above the optical transceiver of the FPGA board. This was done to concentrate the irradiation on the transceiver as the neutron energy decays rapidly over distance and would determine if the transceiver, as opposed to the FPGA chip, was more susceptible to SEUs. The results from these tests are presented in the next chapter, section 5.2.

Figure 4.5: AmBe source positioned on the FPGA board.

To further increase the probability of observing an SEU, additional irradiation tests were carried out with the FPGA operating at the minimum supply voltage. The FPGA is typically supplied by a 12 V power input. As part of the stability tests, the minimum voltage was found to be 5.25 V as lowering the voltage beyond this value resulted in the FPGA becoming unresponsive. This minimum voltage is in line with other studies [68] where several FPGAs were found to operate as normal when powered with close to half the nominal supply voltage. Every FPGA, even of the same family, was found to have a different minimum voltage threshold, at which point the FPGA would encounter faults when operating below this threshold. This experiment was limited to only lowering the

supply voltage to the whole FPGA development board and not directly adjusting the supply rails to the FPGA chip itself. Controlling the individual supply rails for each component on the board would have provided for a more robust and targeted test, however the equipment required to interface with the board's power distribution system was not accessible at the time of this experiment.

4.4 VTRx+ SEU Susceptibility

The SEU susceptibility tests of the VTRx+ followed a similar testing process to the FPGA testbench. First, BER tests were run under standard lab conditions to ensure the stability of the test setup without irradiation. Following this, undvervoltage tests were carried out on both the 1.2 V and 2.5 V supply lines. This consisted of running a BER test for a period of 2 minutes before lowering the supply voltage by 5 mV and repeating this measurement process until the optical link ceased functioning. Next, the AmBe source was positioned over the VTRx+, as seen in Figure 4.6 and the tests were repeated in the presence of irradiation.

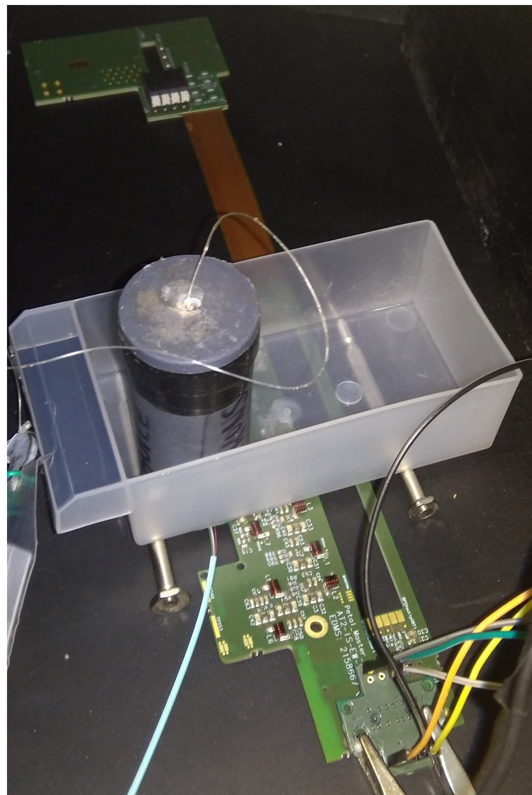


Figure 4.6: AmBe source suspended above the VTRx+ on the EoS card. A makeshift scaffold was used to support the weight of the source and prevent damage to the VTRx+.

4.5 Noisy Power Supply Tests

These tests characterized the influence of power supply noise on the performance of the EoS card as a function of BER. Therefore, these tests built upon the BER test setup previously described and introduce the noise injector circuit discussed in section 3.6 in order to simulate a noisy DC power supply. The updated test setup can be seen in Figure 4.7.

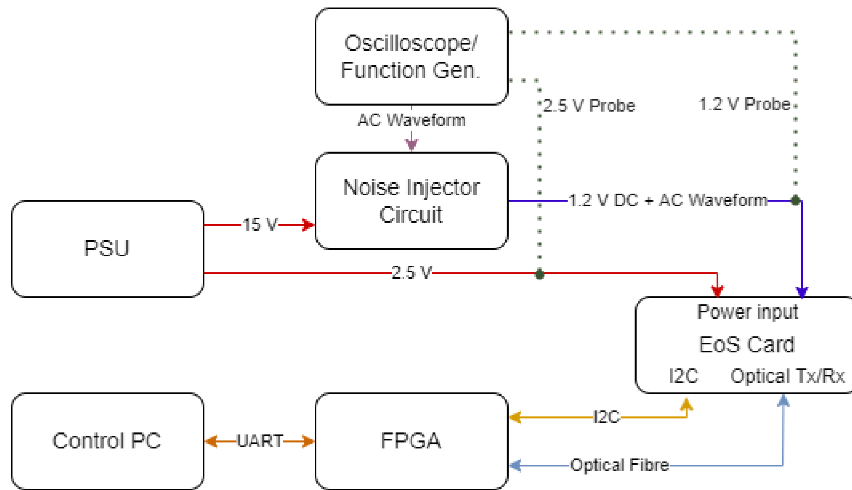


Figure 4.7: Diagram of the BER test set-up where the 1.2 V supply line is being injected with noise.

The oscilloscope is used to monitor the supply rails at the input to the EoS card, in addition to generating the AC waveform used to simulate a noisy DC supply. Only one supply line was injected with noise at a time due to the function generator being limited to one output. As previously mentioned in section 3.6, 4 AC waveforms were used in simulating the noise. The peak to peak voltage was set to 150 mV with a 1.2 V DC offset for the 1.2 V line, and 450 mV with a 2.5 V DC offset for the 2.5 V line. These values were chosen to stay within the minimum and maximum operating ratings (where the minimum was determined by the undervoltage tests and the maximum is 1.32 V and 2.75 V for each line, respectively), and limit the risk of damaging the EoS card as procuring a new one was not an option. Oscilloscope screenshots taken of the different noise waveforms can be seen in Figure 4.8.

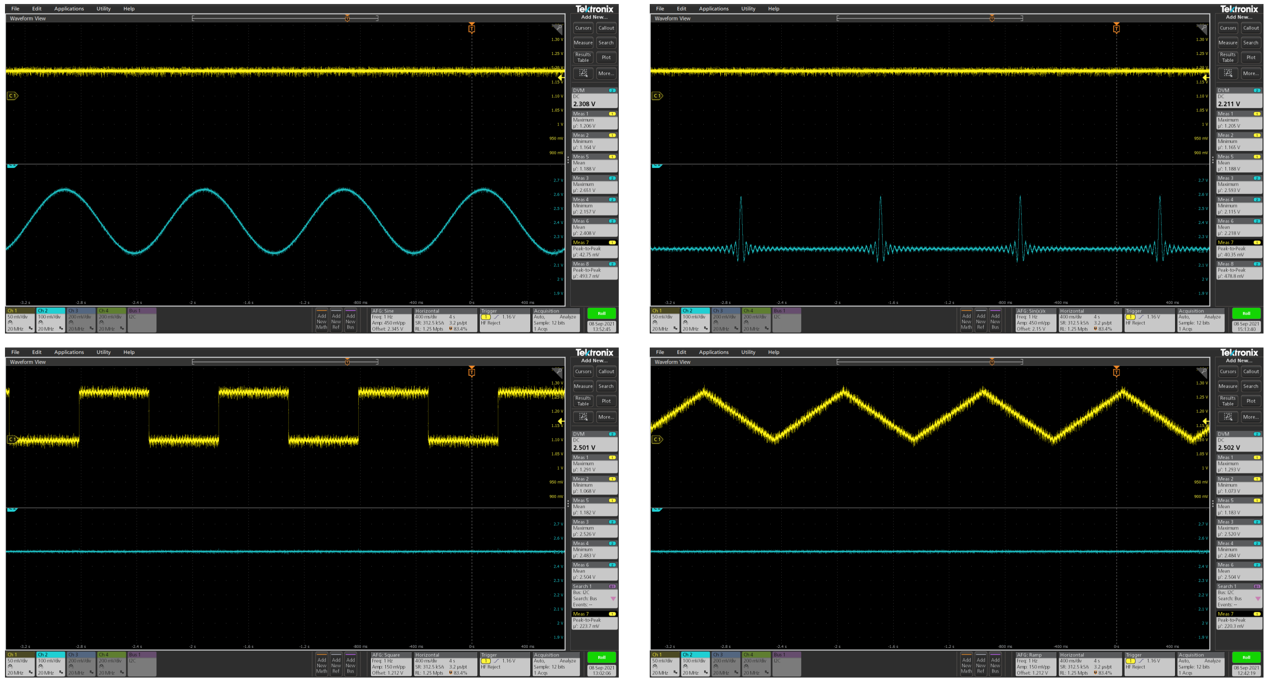


Figure 4.8: Oscilloscope screenshots of noise waveforms superimposed onto DC supply. **Top** Sine and sinc waveforms on the 2.5 V supply. **Bottom** Square and ramp waveforms on the 1.2 V supply.

Python scripts were used to automate the testing procedure by controlling the function generator on the oscilloscope as well as recording readings from the oscilloscope probes at 1s intervals (the fastest sampling rate supported by the Python interface). A BER test would be started in Labview while the Python scripts would follow the steps depicted in Figure 4.9.

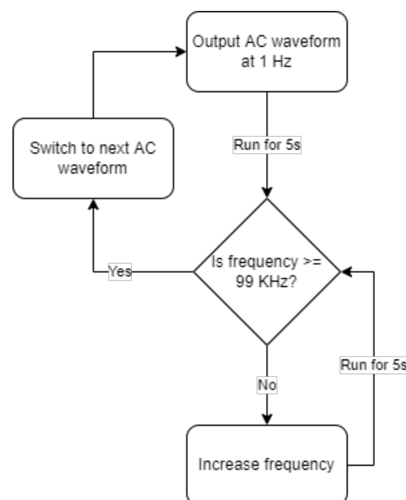


Figure 4.9: Steps followed by the Python scripts in automating the power supply noise tests.

The increase in frequency was a fixed step size for different frequency ranges, as shown below:

- 1 Hz to 1 kHz - step size of 10 Hz
- 1 kHz to 10 kHz - step size of 100 Hz
- 10 kHz to 100 kHz - step size of 1 kHz

These step sizes were based on reducing the test time and findings from initial experimenting where the lower frequencies were observed to have a greater impact on the BER than higher frequencies. BER data was collected for 5 seconds at each frequency, allowing for a minimum BER measurement of $2.23 * 10^{-11}$.

4.6 Optimising the Optical Link

This series of tests focused on characterizing the influence of different VTRx+ configuration settings on the optical signal quality. The configuration settings tested were the bias and modulation current used to operate the laser. The bias current is defined as the logical 1 level, with a maximum of 15 mA, while the modulation current is the difference between the logical 1 and 0 levels, with a maximum of 10 mA. Figure 4.10 provides an illustration of these definitions from which it can be inferred that the signal quality will decline rapidly should the modulation current exceed the bias current as the receiver would have difficulty interpreting the 1 and 0 levels of the signal. Each current setting has a step size of 100 μA and a 7-bit register used to set the desired current level [69].

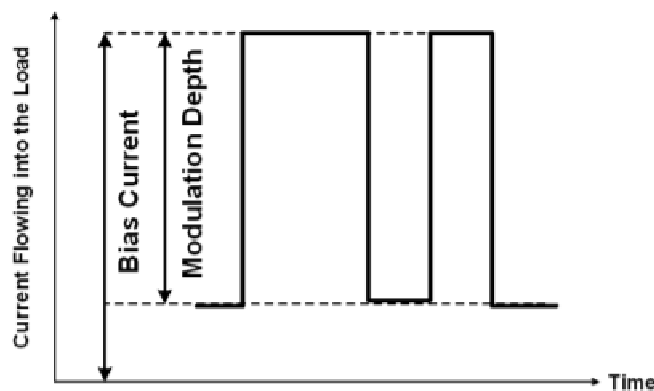


Figure 4.10: Illustration of bias and modulation current definitions. As seen in [22].

To evaluate the signal quality, eye diagrams were taken at different bias and current value pairs. This was done instead of BER tests as the BER measured for different bias and modulation current values does not change without large variations in the current settings. The eye diagrams all used a prescale of 7, allowing for a minimum BER measurement of 10^{-9}. This prescale value was primarily chosen due to time constraints as eye diagrams would take roughly 15 minutes with a prescale of 7, and each higher setting would take twice as long as the previous.

To cover the range of current values (0 to 127), increments of 10 were used, starting at 5 and going up to 125. First, the bias current was set to 5, followed by the modulation current. A BER test was then started, ensuring the link was operating correctly, after which the eye diagram was started. After the eye diagram was captured, the modulation current was increased by 10 and the process was repeated until all the modulation current intervals had been covered. The bias current was then increased by 10 and this process was repeated until all the bias current intervals were captured as well.

The eye diagrams provide a visual representation of the signal quality but were not suitable for quantitatively comparing the signal quality across the range of settings. To aid in this effort, the eye width and height pertaining to a specified BER was calculated for each eye diagram. The eye width and height are directly related to the amount of jitter and noise in the signal, as discussed in section 2.1.4, and provide a useful metric in assessing the signal quality. As the eye diagram data was constructed from a table of BER measurements, a simple algorithm was used to calculate the width as the longest consecutive row of BER measurements greater than or equal to 10^{-9}. The same process was used in calculating the height as the longest column with consecutive BER measurements greater than or equal to 10^{-9}. These height and width measurements can be seen displayed in a heatmap in section 5.6, over the range of bias and modulation current value pairs.

Chapter 5

Results and Discussion

This chapter presents the results of the various tests described in the previous chapter.

5.1 Interpreting BER results

The BERs reported in this chapter are a combination of the various error counters recorded by Labview and described below:

Correctable errors (recorded as CRC errors) indicate the number of correctable errors encountered in a received frame. These errors are identified during the FEC decoding process and are automatically corrected before the data is sent to the BER counter. The presence of CRC errors during the irradiation tests is indicative of an SEU occurring within the laser diode of the VTRx+. During the undervoltage and power supply noise tests, CRC errors are attributed to noise on the optical link.

Non-correctable errors (recorded as E-link errors) indicate the number of errors counted per E-link. These errors are reported by the BER counter and only occur when the number of corrupted bits are beyond the correction capabilities of the FEC decoder. E-link errors encountered during irradiation tests are indicative of an SEU occurring within the laser diode and affecting several bits. During the undervoltage and power supply noise tests, E-link errors are attributed to excessive noise on the optical link inducing more errors than can be corrected.

Alignment errors are caused by frames where the header bits cannot be recovered by

the Aligner module in the FPGA's receiver. When an alignment error is encountered the whole frame is discarded as its data cannot be recovered (but does not impact the non-correctable error counter). An alignment error occurring during the irradiation tests indicates the header bits being corrupted due to an SEU in the laser diode or configuration registers of the laser driver. During the undervoltage and power supply noise tests, these errors are attributed to the header bits being corrupted by noise or as a result of the clock divider within the lpGBT losing synchronization between the different processing blocks due to the increased propagation delay (as discussed in section 2.4.1).

To accommodate the different error counters, the BER is calculated as:

$$BER = \frac{CRCErrors + E - linkErrors + (AlignErrors * 14 * 16)}{TotalFrames * 14 * 16} \tag{5.1}$$

Labview only keeps track of the total frames received, however, it is a simple matter of multiplying the frame count by the number of active E-links (14) and the number of bits per E-link (16) to find the total number of bits transmitted. The same process is applied to the align errors in calculating how many bits were lost from the discarded frames. Should no errors be encountered during a test, the BER is quoted as an upper limit as opposed to an exact figure.

5.2 FPGA Test Results

The results from the FPGA-FPGA tests are tabulated in Table 5.1. No errors were encountered during the baseline, irradiated or undervoltage tests. These findings are in line with other irradiation tests done on FPGAs with neutrons at similar energy levels [70]. Therefore, it was concluded that the subsequent test results were not influenced by any SEUs occurring within the testbench.

Measurement	**FPGA Stability Test**	**FPGA SEU Test**	**FPGA SEU Undervoltage Test**
Duration	48 h	48 h	48 h
Correctable Errors	0	0	0
Non-correctable Errors	0	0	0
Alignment Errors	0	0	0
Bit Error Rate	<6.38 x 10^{-16}	<6.38 x 10^{-16}	<6.38 x 10^{-16}

Table 5.1: Summary of the FPGA stability and SEU test results.

5.3 Stability and VTRx+ SEU Tests

To verify the stability of the test setup, multiple BER tests were run, with the longest being carried out over a 96 hour period with the EoS card operating in nominal conditions. The stability tests encountered no errors, indicating that standard environmental factors and general noise do not contribute to the error rate. It is assumed that the error rate as a result of noise and other ambient effects is negligible for tests of similar duration.

The results from the stability test are presented in Table 5.2, along with the results from the longest-running irradiation test on the VTRx+. Several tests aimed at characterizing the SEU susceptibility of the VTRx+ were conducted. The test duration was increased after each test as no errors were observed and with a greater fluence, it was believed there would be a greater probability of an SEU occurring. In addition, the configuration memory error counter and SEU counter on the lpGBT, as well as the SEU counter on the VTRx+, were read out after each test. None of the counters reported any errors having occurred during the tests. Based on these results, it is concluded that the VTRx+ is not susceptible to SEUs from neutron sources with energy levels comparable to that used in this experiment. These results also indicate that the design changes implemented since [19], where SEU vulnerabilities were discovered in the laser driver of the VTRx+, have rectified the irradiation sensitivity of the component. However, further testing with a range of higher energy neutron sources would be necessary to confirm this. Additionally, these results agree with [30] where no SEUs occurred in the VTRx transmitter when irradiated with a 70 MeV proton beam.

Measurement	**Stability Test**	**VTRx+ SEU Test**
Duration	96 h	351 h
Correctable Errors	0	0
Non-correctable Errors	0	0
Alignment Errors	0	0
Bit Error Rate	$<3.22 \times 10^{-16}$	$<8.83 \times 10^{-17}$

Table 5.2: Summary of the stability and VTRx+ SEU test results.

5.4 Undervoltage Test Results

The results from the BER-undervoltage tests can be seen depicted in Figure 5.2 for the 1.2 V supply line and in Figure 5.1 for the 2.5 V supply line. The results have been

categorized by the type of errors (or lack thereof) encountered in each test. An analysis of the results and problems encountered with the experiments are presented in the following paragraphs. It should be noted that the SEU counters on both the lpGBT and VTRx+ were monitored during the irradiation tests and reported no SEUs being encountered. By considering the nature of the errors encountered, a better understanding of the EoS card's performance in response to the undervoltage power supply can be gained.

Alignment errors can be seen occurring at the lower limits of the 1.2 V undervoltage tests, indicating that the signal noise is overwhelming the aligner module in the receiver, making it impossible to distinguish a majority of the header bits (but not all as CRC errors were also present, indicating that the link was still semi-functional and not completely out of order) and subsequently the individual frames. After increasing the voltage by 5 mV, no further alignment errors are encountered and instead E-link and CRC errors are expected. At this point, the SNR has improved enough for the aligner module to operate but the noise level is still capable of overwhelming the FEC capabilities of the decoder resulting in E-link errors. Further increases to the voltage can be seen to improve the BER as the SNR continues to improve, and eventually, only CRC errors remain before no errors are encountered. An additional perspective on the SNR improving with the increasing supply voltage can be seen depicted in Figure 5.3, which displays eye diagrams captured at different supply voltages.

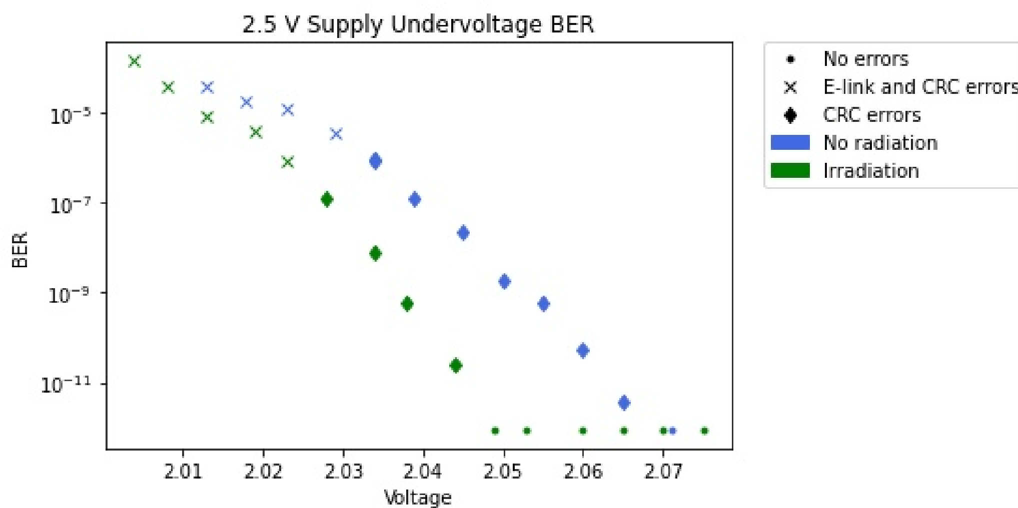


Figure 5.1: Plot of the BER as a function of the voltage read from the 2.5 V input

The relationship between the BER and supply voltage is better depicted in the 2.5 V supply results. Additionally, the transition from E-link errors to just CRC errors is clearly observable. While the BER curves do not perfectly overlap between the irradiation and non-radiation tests, this is believed to be caused by variations in coupling efficiency

between measurements and not as a result of the irradiation. This discrepancy has been encountered in similar studies [30] and was attributed to variations in the test setup between measurements.

These setup variations are also believed to be the primary cause for the spread in the 1.2 V BER results. Especially in the case of the irradiation tests, where the time in the lab is limited to a few minutes in order to minimise one's exposure to irradiation. One of the primary causes for this variability is believed to stem from the power connector used with the EoS card. This power connector is only used during testing and is adequate for the majority of tests. However, the connector is secured to the EoS card using paper clips, in lieu of a dedicated fastening, which could not guarantee the same coupling efficiency between tests. This presented problems in ensuring the setup's stability and reproducibility.

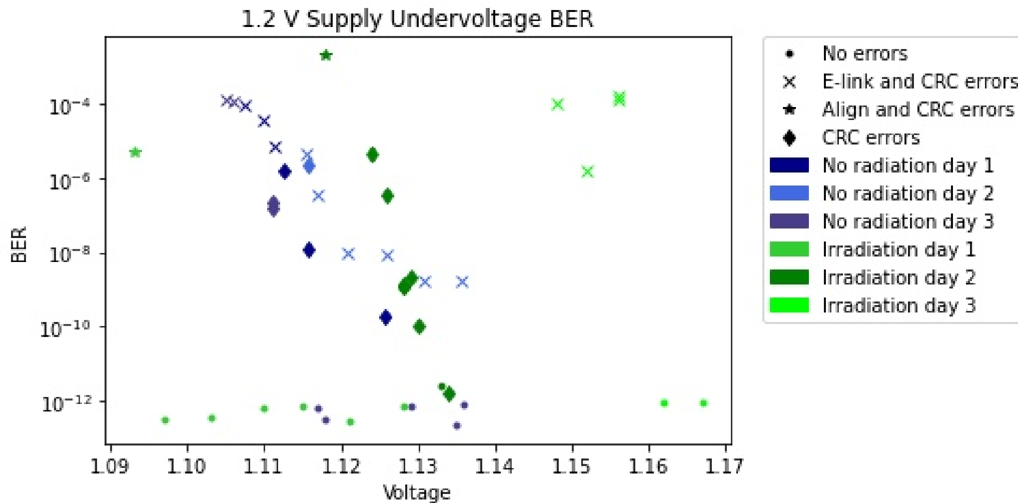


Figure 5.2: Plot of the BER as a function of the voltage read from the 1.2 V input.

Further challenges were encountered with these undervoltage tests in producing all error types during a single test. The BER measurements were expected to encounter alignment and CRC errors at the lower voltage limits, bordering the point where the EoS card shuts down. As the voltage was increased, E-link and CRC errors were expected next, followed by just CRC errors before errors are no longer encountered. While the trend of a decreasing BER as the voltage is increased is apparent, identifying the transition point between the different types of errors would have provided a broader understanding of the BER and supply voltage relationship. However, the voltage margin between the different error types and completely disconnecting the optical link proved to be smaller than expected and beyond the level of accuracy of the test equipment used.

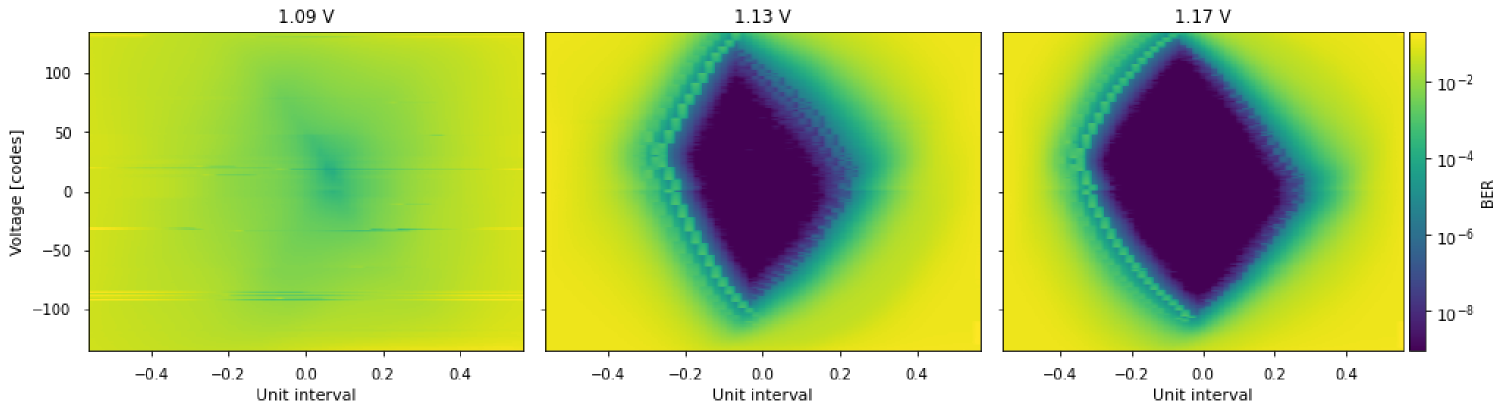


Figure 5.3: Eye diagrams at different supply voltages. **Left** taken at 1.09V, the signal is barely discernible. **Middle** taken at 1.13 V, this eye diagram corresponds with a BER of 10^-10 where CRC errors are present. **Right** taken at 1.17 V, this eye diagram represents a signal with no errors and a BER of 10^-12.

5.5 Power Supply Noise Test Results

The results from the power supply noise tests are plotted below. Each figure corresponds to a different AC noise waveform and illustrates the BER measured across a range of frequencies. The BER measurements are categorized by the types of errors observed. Following the test results, a discussion is made on some of the pitfalls of the test and how this might have influenced the results.

The tests performed on the 1.2 V supply showed a majority of the errors encountered occurring in the lower frequency range (<1 kHz) of the applied noise. This is believed to be caused by the minimum voltage level of the noise waveforms being applied for a long enough duration for undervoltage errors to be induced. With a peak to peak voltage of 150 mV for the 1.2 V noise waveforms, the minimum voltage was approximately 1.125 V. This voltage level can be seen in Figure 5.2 to cause CRC errors. This is not the case for the sinc noise waveform, which given the shape, as seen in Figure 4.8, does not reach as low a voltage level (minimum of 1.14 V) for the same peak to peak voltage as the other waveforms and therefore no errors are observed.

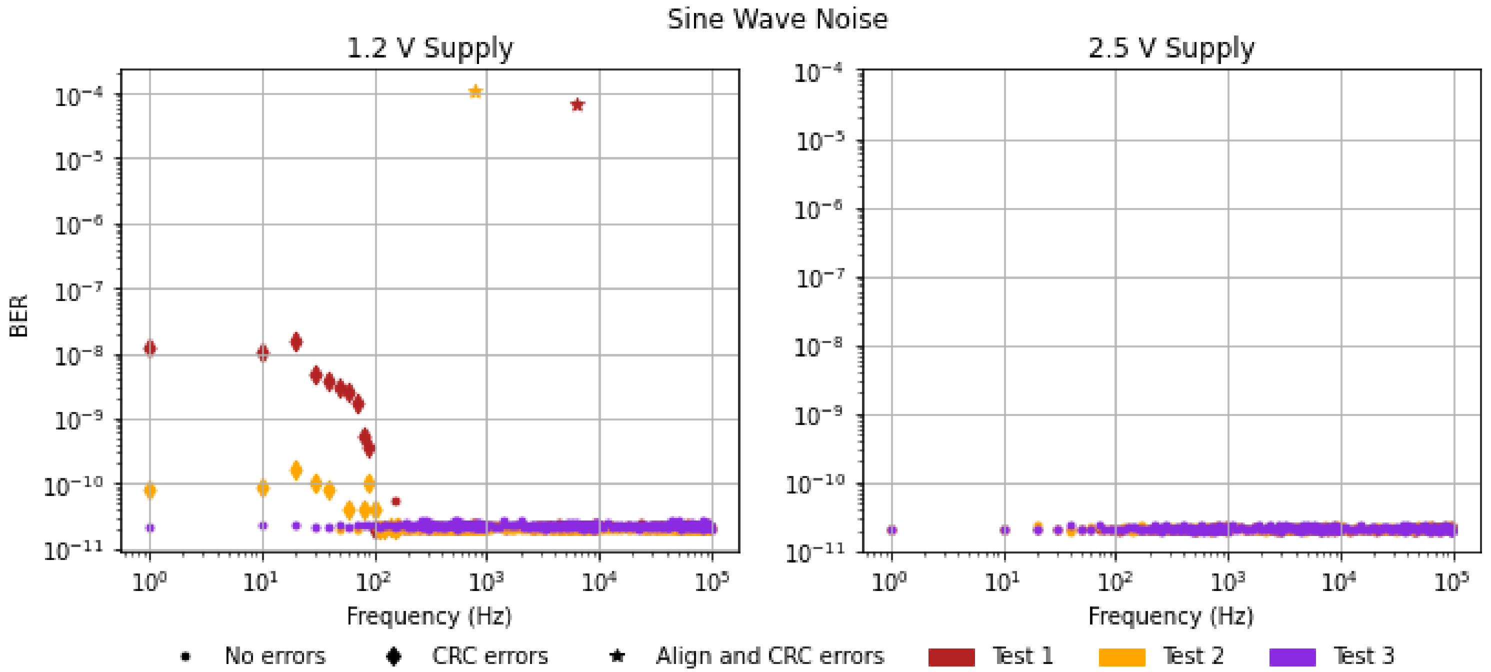


Figure 5.4: Plots of the BER measured over a range of frequencies for the power supply noise simulated using a sine waveform.

An anomaly can be seen in Figure 5.4 in the 1.2 V supply results, where alignment and CRC errors occur near the 1 kHz and 10 kHz sine wave frequencies. Based on the studies discussed in section 2.4, it is possible that at these frequencies jitter can be induced on the lpBGT clock to an extent that causes the frame aligner to lose alignment, thus causing alignment errors. However, more tests would need to be conducted in order to confirm this and given the BER at the surrounding frequencies do not exhibit similar errors, these are most likely outliers caused by equipment variations between the tests.

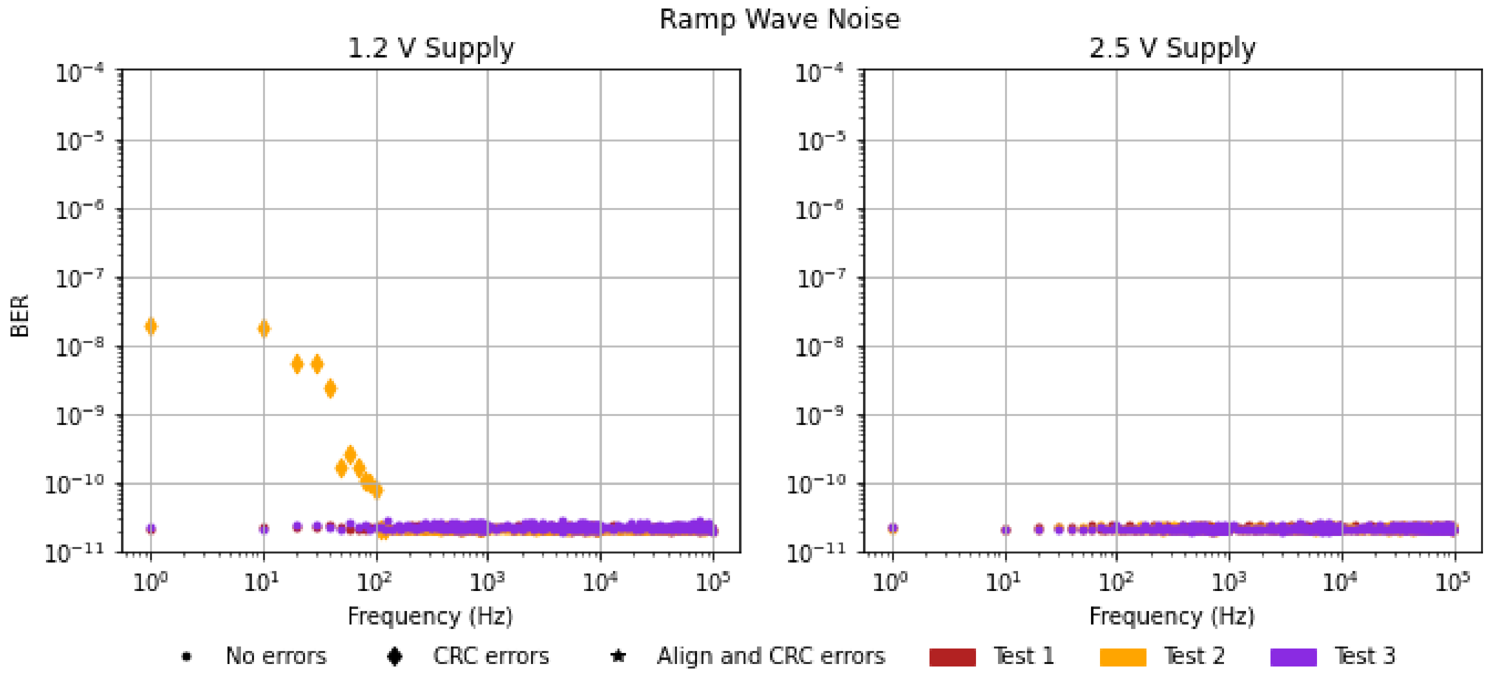


Figure 5.5: Plots of the BER measured over a range of frequencies for the power supply noise simulated using a ramp waveform.

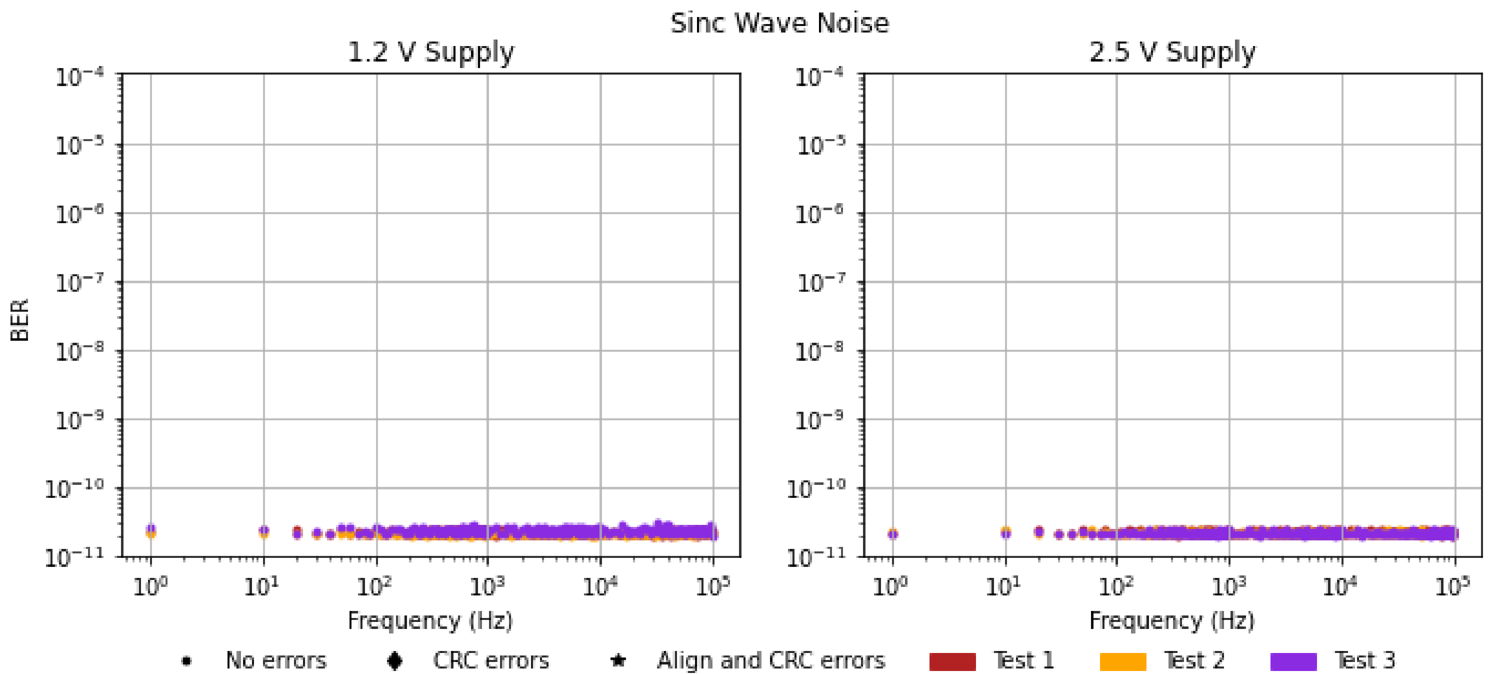


Figure 5.6: Plots of the BER measured over a range of frequencies for the power supply noise simulated using a sinc (sin(x)/x) waveform.

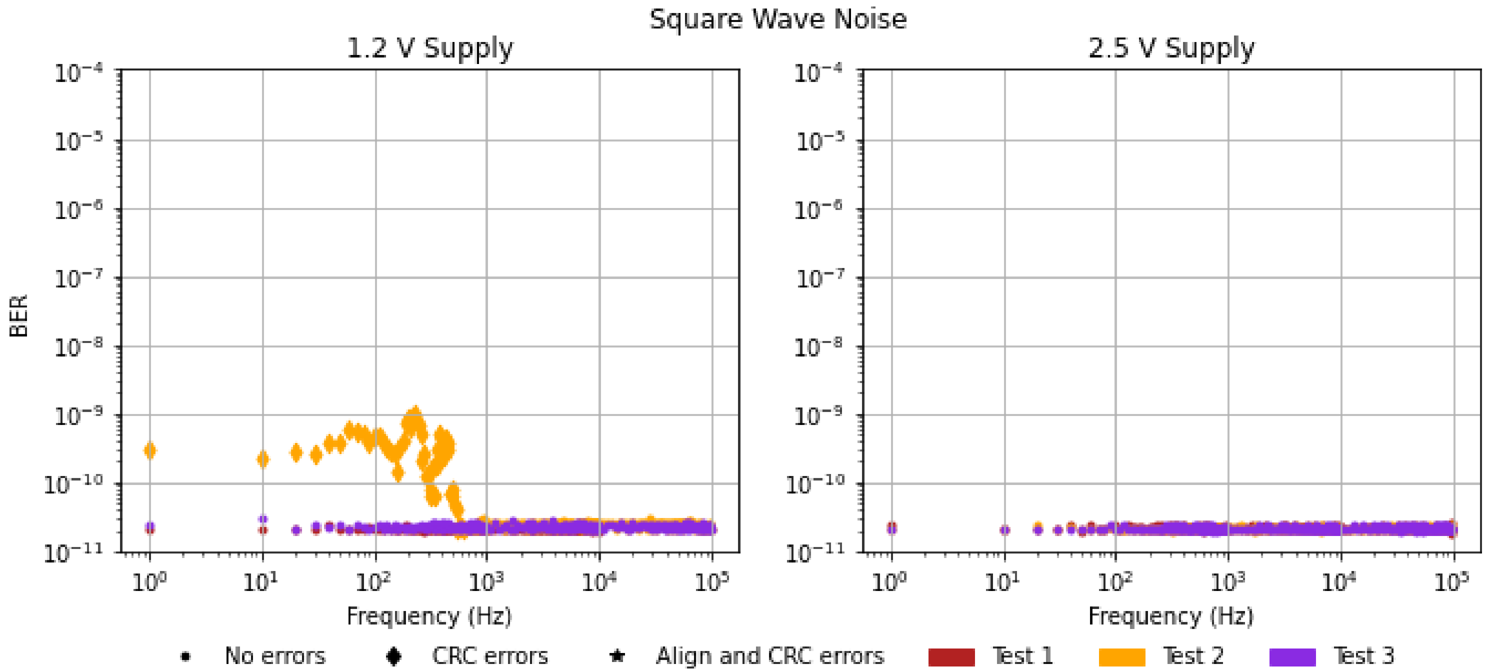


Figure 5.7: Plots of the BER measured over a range of frequencies for the power supply noise simulated using a square waveform.

The 2.5 V supply line did not experience any errors during the supply noise tests. This supply line is only used in the output stage of the VTRx+ (involved in driving the laser) which appears to be less susceptible to errors induced by voltage fluctuations. As this supply line is not used for any data processing blocks, it makes sense that the safe operating voltage margin would be greater than that of the 1.2 V supply line.

In Figure 5.8, the mean peak to peak voltage of the noise waveforms used in the above tests is plotted across the operating frequency. The peak to peak voltage was recorded by the oscilloscope during each test, however, the measurements proved to be extra sensitive to external noise appearing on the oscilloscope probes. This is important to note as the maximum peak to peak voltage was 150 mV for the 1.2 V waveforms and 450 mV for the 2.5 V waveforms. The primary takeaway from these plots is the decline in peak to peak voltage at frequencies above 1 kHz. This is a pitfall of the improvised noise injector setup where the peak to peak voltage of the output waveform is diminished due to the impedance mismatch between the EoS card power supply input and the noise injector's output. As the frequency increases, the impedance mismatch deteriorates further, resulting in the output of a less noisy signal. This problem is a serious drawback for testing higher frequencies with this circuit and would likely require a commercial line injector to be carried out accurately.

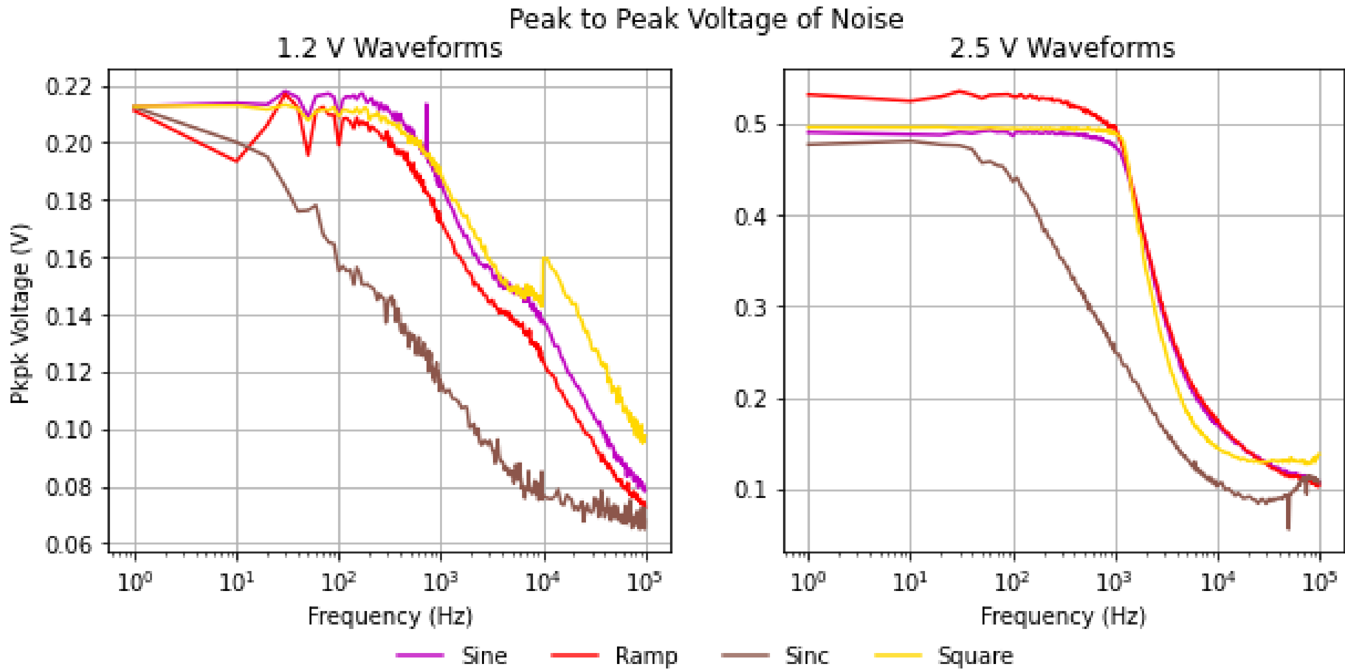
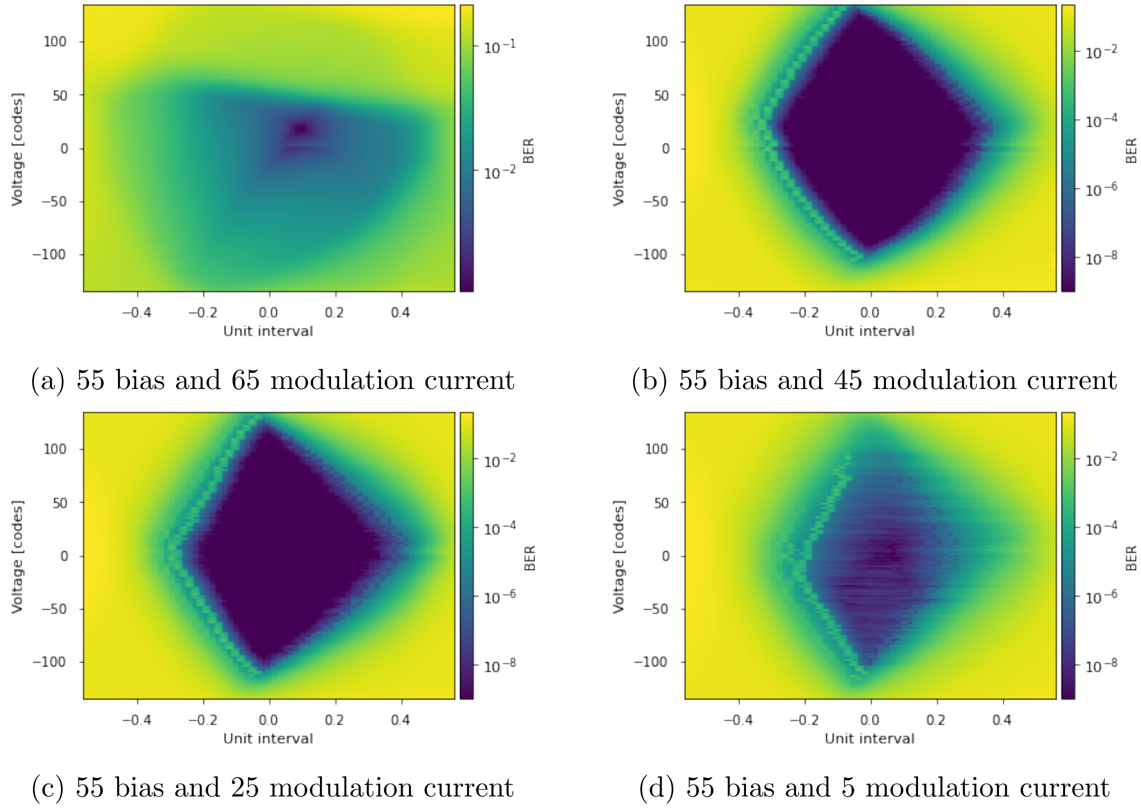


Figure 5.8: Mean peak to peak voltage of noise waveforms.

5.6 Optical Link Results

In Figure 5.9, several eye diagrams are displayed, illustrating how the signal quality changes as the modulation current is varied while the bias current remains constant. Figure 5.10 illustrates the same trend in signal quality but with the modulation current remaining constant while the bias current is varied. From these diagrams, it can be seen that the signal quality is generally better when the bias current is greater than the modulation current but the difference is not too significant. To gain a better understanding of the relationship between the current settings and the signal quality, Figures 5.11 and 5.12 depict the change in eye height and width across the different bias and modulation current levels.



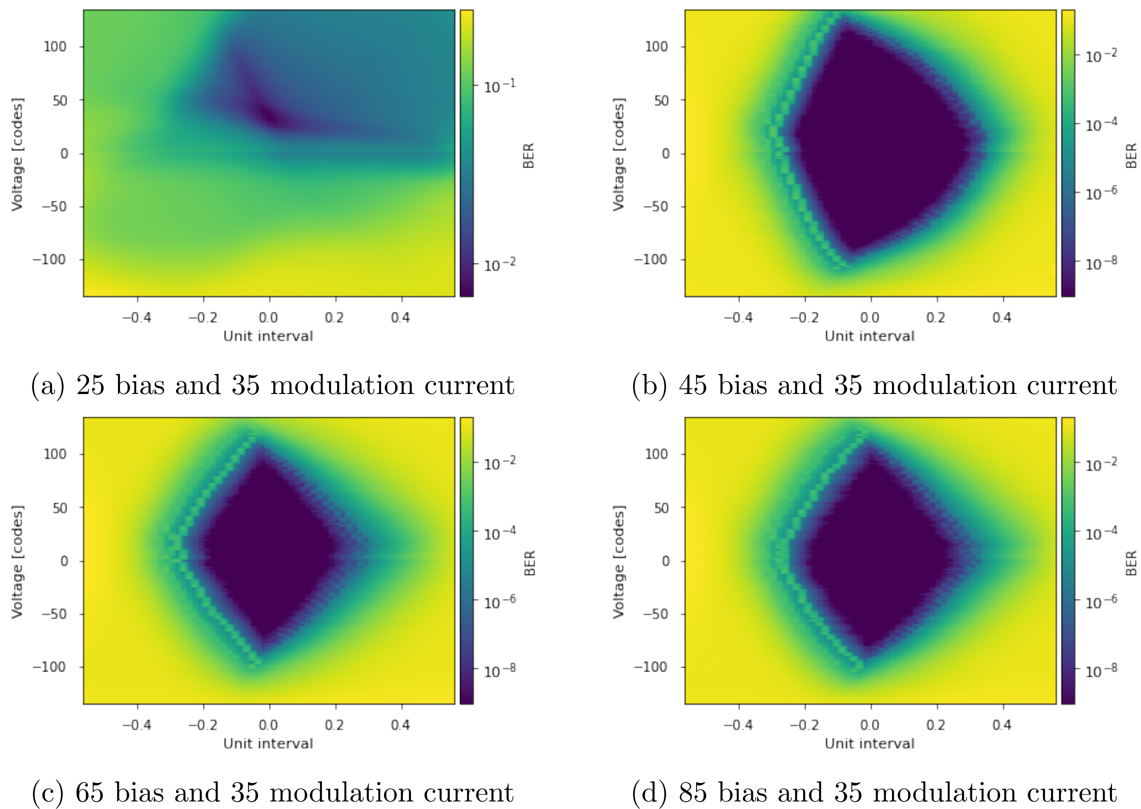
(a) 55 bias and 65 modulation current

(b) 55 bias and 45 modulation current

(c) 55 bias and 25 modulation current

(d) 55 bias and 5 modulation current

Figure 5.9: Eye diagrams depicting the change in signal quality as the modulation current is varied while the bias current remains constant.



(a) 25 bias and 35 modulation current

(b) 45 bias and 35 modulation current

(c) 65 bias and 35 modulation current

(d) 85 bias and 35 modulation current

Figure 5.10: Eye diagrams depicting the change in signal quality as the modulation current is varied while the bias current remains constant.

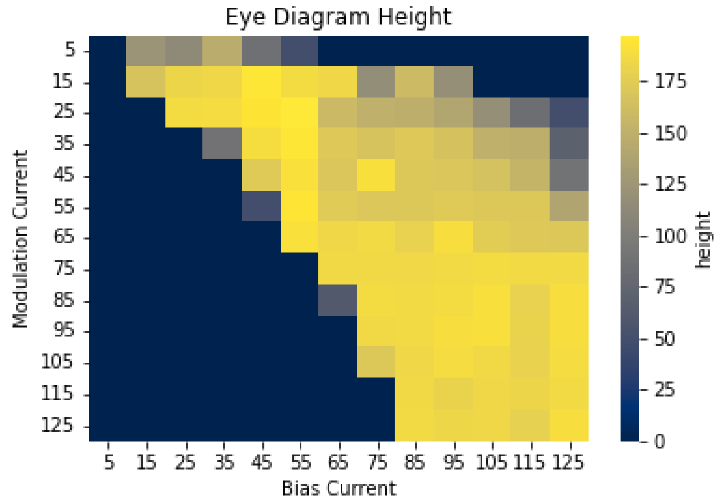


Figure 5.11: Eye diagram height measurements taken across the range of bias and modulation current settings.

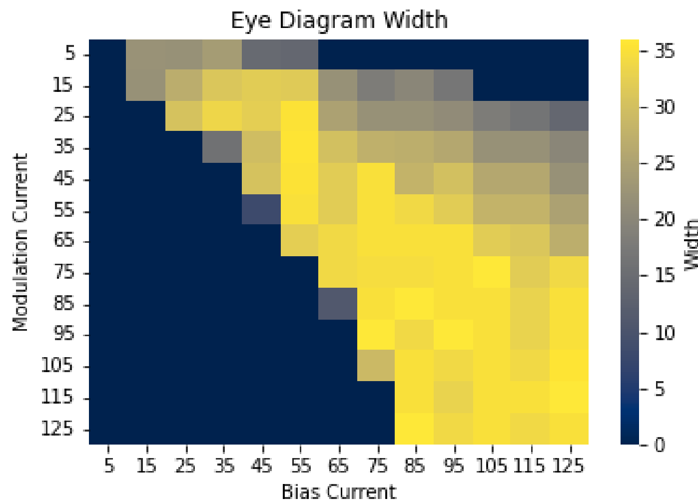


Figure 5.12: Eye diagram width measurements taken across the range of bias and modulation current settings.

From the results presented here, a few guidelines can be set out for deciding on the appropriate bias and modulation current values. It was noticed during the tests that CRC errors had a tendency of occurring when the eye diagram width was approximately 25 or less and when the height was near 150 or less. To keep above these limits, the following recommendations are made regarding the bias and modulation current settings:

$$\frac{bias}{2} \leq mod \leq bias - 10 \tag{5.2}$$

Where the bias current minimum is 35. These are rough guidelines that could be refined

with repeated tests using smaller increments for the current settings and a greater prescale setting for the eye diagrams. However, following this relationship between the bias and modulation current configuration will ensure no errors up to a BER of 10^{-12} based on the findings above.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

This research sought to qualify the performance of the EoS card in preparation for operation within the HL-LHC. This encompassed investigating the susceptibility of the VTRx+ to SEUs, characterizing the BER performance of the EoS card under non-ideal power supply conditions, and evaluating the impact of the VTRx+ configuration settings on the optical signal quality.

This work built upon the test framework developed at DESY. A number of significant additions were made to extend the testing capabilities of this test setup in pursuance of this project's objectives. New firmware modules were developed to provide eye scan functionality to the FPGA testbench (as previously stated, the firmware code can be found at this link: online repository). The Labview software was expanded by establishing communication with the VTRx+, allowing for the programming and evaluation of different configuration settings. Power supply noise injection hardware was built in order to evaluate the EoS card's BER performance in response to power supply fluctuations.

The results from the irradiation tests demonstrated that both the testbench FPGA and VTRx+ are not susceptible to SEUs in the presence of neutron radiation with an energy spectrum ranging up to 11 MeV. The effect from this species and energy level of irradiation was previously unexplored in studies focused on the VTRx+ and had been demonstrated to be useful in SEU investigations [23]. However, the lack of SEUs encountered is in agreement with similar investigations [30, 19] and demonstrates the component's SEU resilience. Undervoltage tests in the presence of radiation were also carried out with the

understanding that the device's SEU sensitivity would be increased under such conditions. The results from these tests did not indicate any SEUs had occurred but still proved useful in defining the BER performance of the EoS card under non-ideal power supply conditions. The 2.5 V power supply was found to continue operating correctly well below the specified minimum supply voltage of 2.25 V, with correctable errors appearing around 2.06 V and un-correctable errors only occurring around 2.03 V. The 1.2 V power supply experiments suffered from variations in the test setup between measurements, making it difficult to discern any useful correlations in the results.

The test results from the power supply noise tests demonstrated the effectiveness of the error correction capabilities of the GBT protocol. All errors induced by the injected noise were correctable, excluding 2 outliers attributed to the non-ideal operation of the ad-hoc noise injection equipment. Further investigation into the custom-designed noise injection equipment revealed flaws in the impedance matching capabilities and consequently, the noise waveforms above 1 kHz suffered from peak to peak voltage clipping. While still simulating noise, the magnitude of the noise was less than desired at higher frequencies. The test results demonstrate that any errors caused by power supply fluctuations are correctable and that the BER performance of the EoS card was unaffected by power supply noise.

The investigation into the optical signal quality and impact from the bias and modulation current settings revealed a trend between the width and height of the eye diagram and the associated BER. From this trend, recommendations have been made on the optimal settings configuration and how these parameters can be refined further. When used within the collider, however, the optimal settings are likely to change considering the cumulative degradation experienced by laser diodes in the presence of radiation. The wide range of operating settings allows the VTRx+ to compensate for this degradation, as discussed in [32] relation to the VTRx, and higher bias and modulation values can be used to overcome the deteriorating output efficiency of the laser.

The research presented here demonstrates the EoS card and its components to be expertly designed, exhibiting notable SEU resilience despite the SEU mitigation features being disabled. Additionally, the BER performance of the EoS card has proven to be impervious to power supply fluctuations, only faltering at levels beyond the specified operating range. The VTRx+ configuration settings have been characterized by their impact on the optical signal quality, from which guidelines on the optimal setting values have been put forth. This project has also made a significant contribution to the work being carried out at DESY with the development of the eye scan firmware being integrated into their quality control procedure. This eye scan functionality will now be used in the production phase

of the EoS card, where the entire set of approximately 2000 EoS cards will have their optical signal quality assessed with this firmware. This will lead to a better functioning ITk as subtle defects will be detected, thus avoiding future malfunctions.

6.2 Recommendations for Future Investigations

Based on the contributions covered above, the following future recommendations are made for future work:

Upscaled Neutron Tests The AmBe neutron source used in this project had an energy spectrum with a maximum energy of 11 MeV. This was a previously untested energy level of neutron irradiation for the EoS card components, however, there still remain further neutron energy levels that are expected within the HL-LHC which have yet to be tested. From the literature surveyed, the highest energy level of neutrons used in testing the VTRx was 50 MeV [32]. At iThemba LABS, a neutron beam facility is able to generate quasi-monoenergetic neutron beams in the range of 30 - 200 MeV. This is one of the few research laboratories in the world capable of sourcing neutrons with energies above 30 MeV. Performing irradiation tests in this facility would provide unique and valuable information on the radiation resilience of the EoS card and its components.

Undervoltage Test Improvements Further iterations of the supply undervoltage tests with mitigations made towards correcting equipment variation between measurements would be beneficial. These results would help define the safe operating margin for the supply voltage which were found to be above the specified minimum voltage (1.09 V), however, this is believed to be due to the variation between measurements and should be confirmed. The latest results from the DC-DC converter testing [71] indicate that the 2.5 V output remains well within the specified supply voltages while the 1.2 V output shows a much greater variation (nearly reaching 1.09V). Repeating the undervoltage tests to a greater level of accuracy would provide a better understanding on the impact of the DC-DC converter output variation could have on the EoS card's performance.

Testing with the DC-DC Converter This recommendation is made following the problems encountered with the power supply noise injection equipment. While representative power consumption/supply conditions can be set during the testing of individual components, integration and in-system tests are required to ensure reliable operation to greater certainty. This suggestion is not limited to just power supply tests and also includes performing irradiation tests with the DC-DC converter on the EoS card to ensure no unexpected

behaviour in an environment representative of the ITk.

TID Radiation Effects In [32], the author studies the laser efficiency degradation of the VTRx as a result of TID effects from irradiation. The degradation is measured and compromises are suggested in adjusting the VTRx configuration settings to compensate for these effects over time. A similar study on the EoS as a whole could provide valuable information towards extending the operational lifetime of the card. The lpGBT and VTRx+ offer a myriad of configuration options that could address the deterioration in various aspects. It is recommended that the impact of TID on the EoS card be investigated in order to understand what areas might become faulty first and how these could be mitigated.

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Appendix A

Additional Files and Schematics

A.1 Schematic of FPGA Firmware

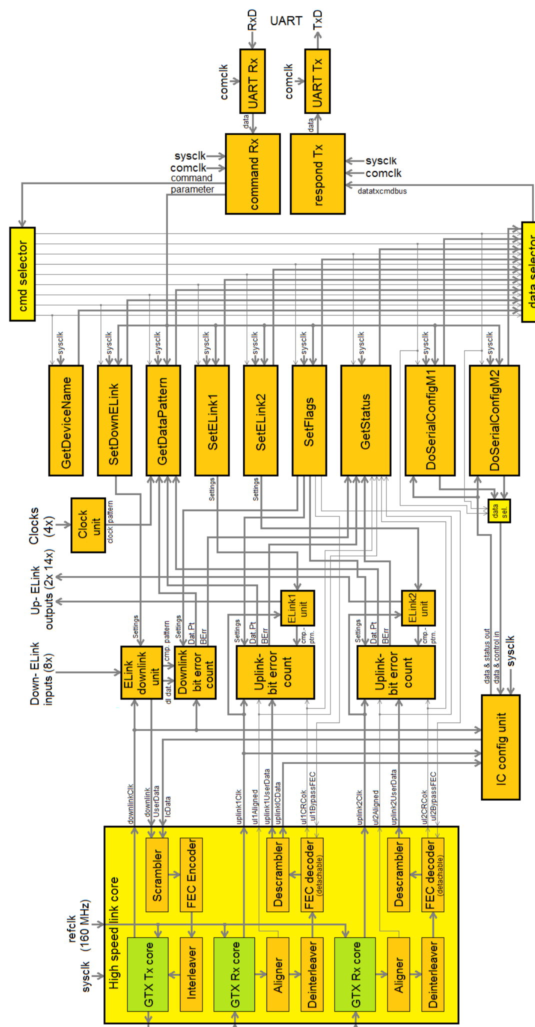

Figure A.1: Block diagram of modules in the DESY FPGA firmware. As found in the firmware documentation [72].

A.2 Initial Level Converter

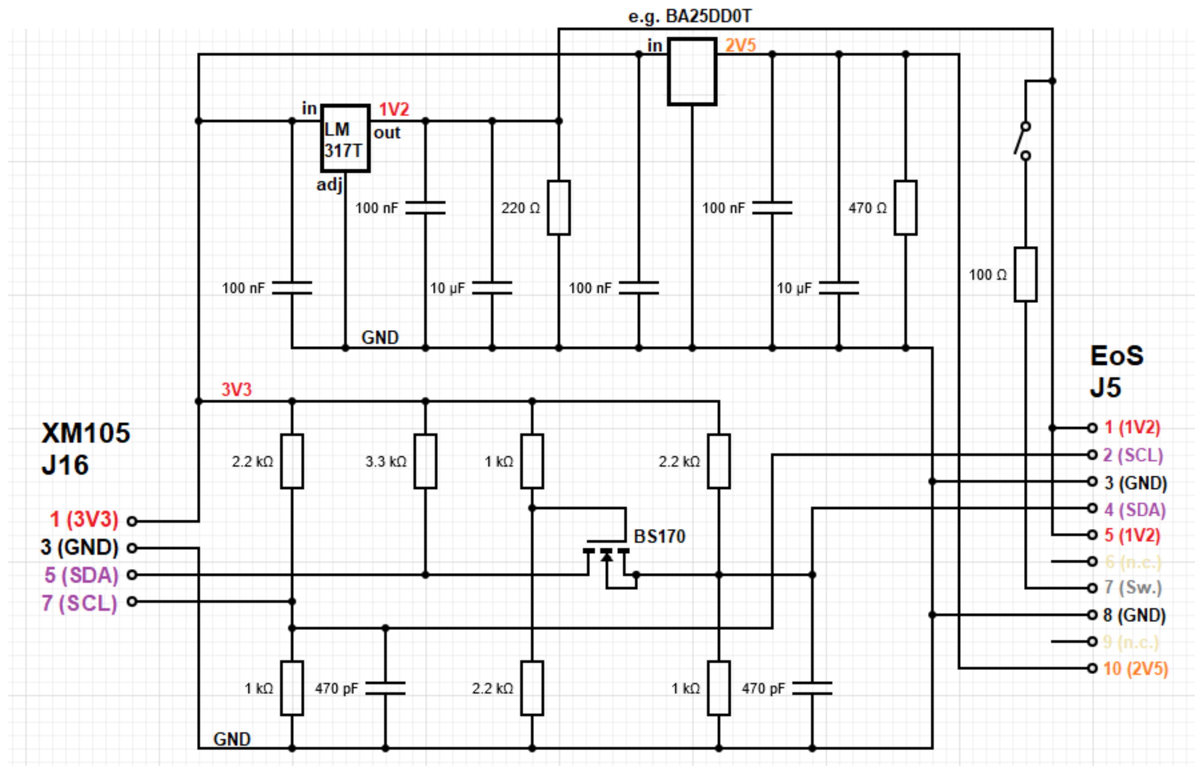

Figure A.2: Circuit schematic of the original level converter.