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A DEVELOPMENT STUDY FOR A SHORT RANGE, LOW CAPACITY
DIGITAL MICROWAVE LINK

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for the degree M.Sc(Eng).

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ABSTRACT

A specific request for development of a short-range, low capacity digital microwave transmission system has been received from the South African Dept. Posts and Telecommunications. The aim of this project is to initiate development work by determining the optimum system configuration and modulation technique to meet the design specifications. In addition, it is proposed to develop and construct an I.F. modulator/demodulator module using which simulation tests may be performed in order to assess the chosen modulation scheme's feasibility in this specific application.

First, a review of existing digital modulation techniques is made, followed by a comparative evaluation of the various schemes with regard to certain important operating parameters. This is followed by a detailed look at the specifications of the data-link we have been requested to develop. Next, a selection of the system configuration and modulation technique is made, taking into account advantages of various schemes, as well as problems envisaged. The rest of the project involves the practical realisation of various I.F. and modulator/demodulator elements required for performing tests in which R.F. data transmission employing the selected modulation scheme is simulated. Finally, a detailed description of the simulation tests which can be performed is presented.

DEDICATION

To Freda for her love and encouragement. Also to my parents whose courage provided me with opportunity.

DECLARATION

I declare that this thesis is my own unaided work. It is being submitted in part fulfilment of the requirements of a Masters degree in Engineering to the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

signature removed

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(Name of candidate)

14TH day of APRIL, 1987

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REVIEW OF MODULATION TECHNIQUES FOR DIGITAL RADIO

1.0 Introduction

The search for methods of transmitting information at higher speeds across a bandlimited channel has a long history. In 1898 Gulstad [1.1] developed a means of detecting telegraph signals which had been transmitted at twice the normal dotting rate... a procedure known as "double dotting". In 1928 Nyquist produced his paper "Certain Topics In Telegraph Transmission Theory" [1.2] in which he developed the theoretical foundation for transmission of telegraph signals over a bandlimited cable with zero intersymbol interference.

In later years, computer communication requirements led to renewed interest in bandwidth efficient digital transmission techniques. In 1962 and 1963 Lender [1.3,1.4] discovered the concept of correlative transmission techniques and presented the analytical basis for "doubinary" transmission. The doubinary concept, also dubbed "partial response", was generalised by Kretzmer [1.5,1.6] in 1966. During this era most research focussed on optimising data transmission through existing analog voice channel facilities.

Today the trend is toward digital communication systems capable of efficient simultaneous transmission of digital source information, digitized voice channels, digitized television and other analog sources which have been converted into the digital transmission format. Consequently much attention has been paid in recent times to developing new and improved modulation techniques for bandwidth efficient digital transmission.

The work of Nyquist, Lender, Kretzmer and many others form the theoretical basis for the design of bandlimited digital radio systems. However, in applying these concepts to the radio channel, several additional factors must be considered. Co-channel and adjacent channel interference, pulse-shaping filters, and contending with non-linear power amplification are some of these.

It is intended in this chapter to provide a broad description of the various modulation schemes applied in modern digital radio systems, as well as a performance comparison of these schemes subject to factors such as co-channel and adjacent channel interference, pulse-shaping, non-linear amplification etc.

The general form of a digital radio system is shown in Fig.1.0 where the position of modulator and demodulator/detector can be seen in relation to the rest of the system.

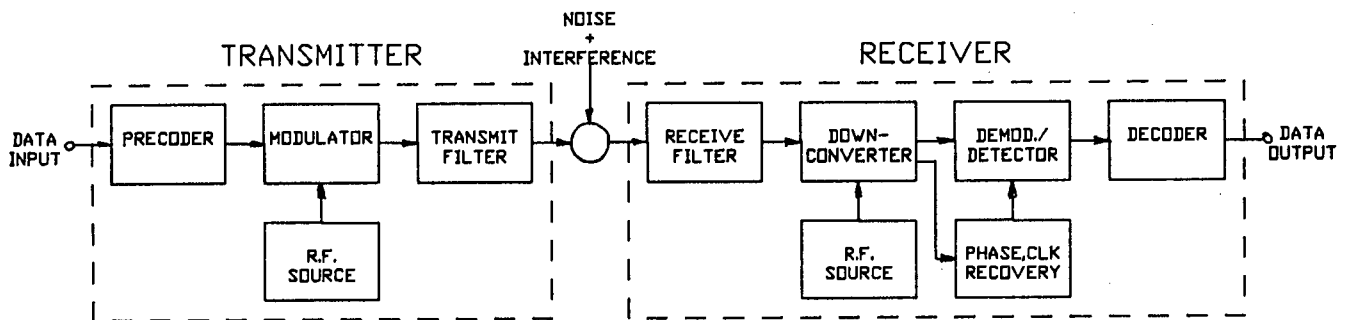


Fig.1.0 SIMPLIFIED SCHEMATIC OF A DIGITAL RADIO SYSTEM

1.1 Modulation Schemes

Amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM) are the three fundamental modulation techniques. All other modulation schemes are either variants of one of the above or hybrid schemes.

1.1.1 Amplitude modulation

In Amplitude-Shift-Keying (ASK) the signal information is conveyed via amplitude variation of the modulated signal. The technique is therefore inherently susceptible to noise and has the disadvantage of a fluctuating signal level which can cause poor performance in the presence of fading. Non-linear amplification of any signal exhibiting AM has the effect of generating additional sidebands, thereby causing spectral spreading of a band-limited AM signal.

(a) Double Sideband (DSB) is the simplest form of AM;

$$f_{DSB}(t) = \frac{A[1+m(t)]\cos(\omega_c t)}{2} \dots (1.0)$$

Where: $m(t)$ = modulating signal
 ω_c = carrier frequency [rad/s]

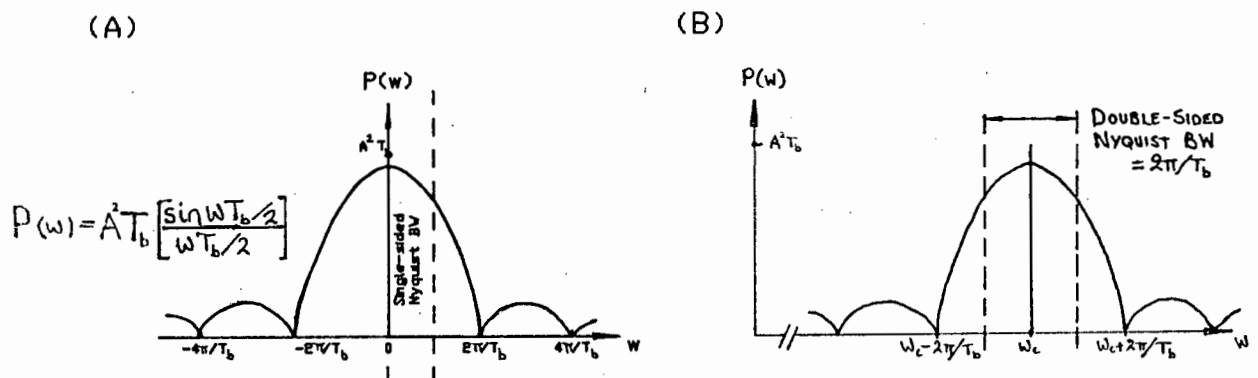


Fig. 1.1 POWER SPECTRAL DENSITY FUNCTION OF:

(A) NRZ DATA PATTERN $m(t)$

(B) DSB-MODULATED NRZ DATA SIGNAL

SPECIAL CASES: 1. For 100% modulation of an NRZ data-stream, $m(t) = \pm 1$ which yields On-Off-Keying (OOK) modulation.

2. $m(t)$ = m-level PAM (Pulse-amplitude modulation) signal yields Multiple-Amplitude-Shift-Keying (MASK)

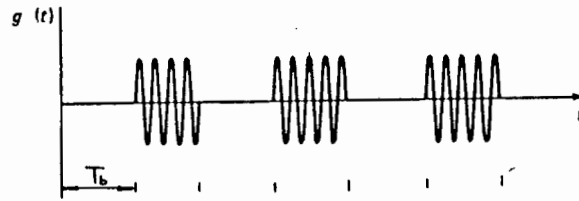


Fig. 1.2 OOK SIGNAL WAVEFORM

DETECTION: Coherent or incoherent. Advantage gained by coherent detection of DSB signal is small in relation to the increase in complexity over incoherent detection.

(b) Double Sideband - Supressed Carrier (DSB-SC) AM has improved power efficiency due to supression of the carrier which conveys no information.

$$f_{DSB-SC}(t) = Am(t)\cos(\omega_c t) \dots (1.1)$$

- SPECIAL CASES:
1. $m(t) = 0$ or 1 yields OOK once again
 2. $m(t) = \pm 1$, i.e. NRZ datastream, produces Binary Phase-Shift Keying (BPSK) - see section 1.1.3
 3. $m(t) = m$ -level PAM signal again yields a form of MASK.

DETECTION: Coherent.

(c) Single Sideband (SSB) AM has improved bandwidth efficiency over DSB-SC by supression of one redundant sideband (usually by means of a sharp cut-off bandpass filter). The SSB signal can be represented as:

$$f_{SSB}(t) = A[m(t)\cos(\omega_c t) + M(t)\sin(\omega_c t)] \dots (1.2)$$

Where: $M(t)$ = Hilbert transform of message signal $m(t)$, i.e. to produce $M(t)$ every frequency component in $m(t)$ is retarded by 90 degrees. [1.7]

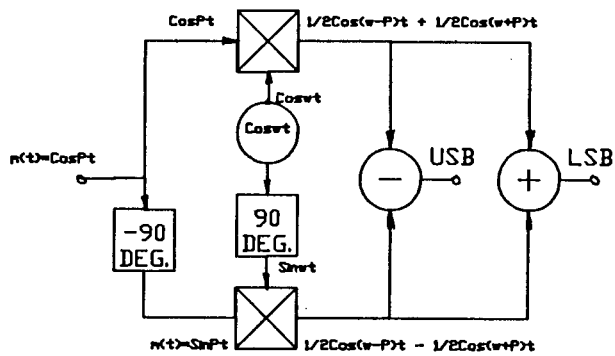


Fig. 1.3 SCHEMATIC OF AN SSB MODULATOR

Note: Since retarding every frequency component in $m(t)$ by 90 degrees is not the same as a constant time delay, clearly this realisation of an SSB modulator is only feasible for $m(t)$ sinusoidal.

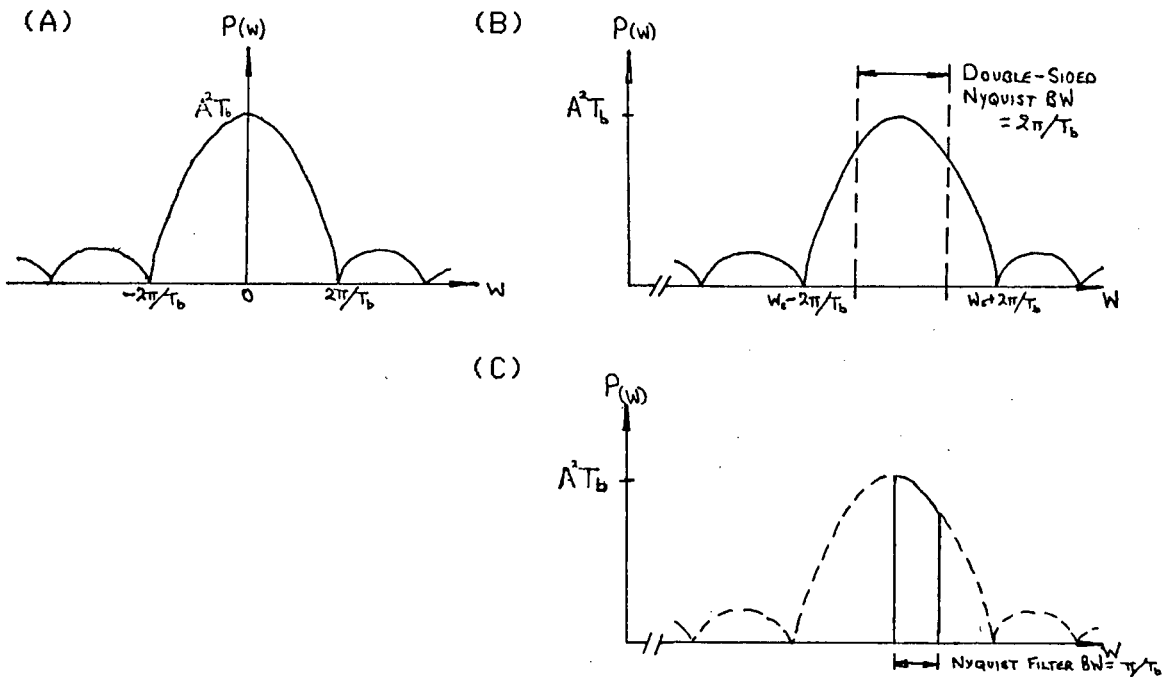


Fig. 1.4 POWER SPECTRAL DENSITY FUNCTIONS OF :

- (A) BASEBAND NRZ DATASTREAM $m(t)$
- (B) DSB-SC SIGNAL
- (C) SSB SIGNAL PRODUCED BY PASSING THE DSB-SC SIGNAL THROUGH AN IDEAL BPF

A Nyquist filter bandwidth of $f_b/2$ ($f_b=1/T_b$) for SSB signals implies a spectral efficiency (for ideal filtering) of 2 bits/s/Hz.

DETECTION: Coherent.

(d) Vestigial Sideband (VSB) AM is a compromise in bandwidth efficiency and detection simplicity between SSB and DSB. VSB is generated in the same way as SSB, but instead of using a sharp cut-off bandpass filter, a filter with a smooth roll-off is used in order to retain a vestige of the second sideband and carrier. Incoherent detection is thereby facilitated. Bandwidth efficiency is of course sacrificed in this way.

DETECTION: Coherent or incoherent.

(e) Quadrature Amplitude Modulation (QAM) is produced by adding two DSB-SC signals which have been modulated by carriers which are in phase-quadrature with one another.

$$f_{QAM}(t) = A[m_I(t)\cos(\omega_c t) + m_Q(t)\sin(\omega_c t)] \dots (1.3)$$

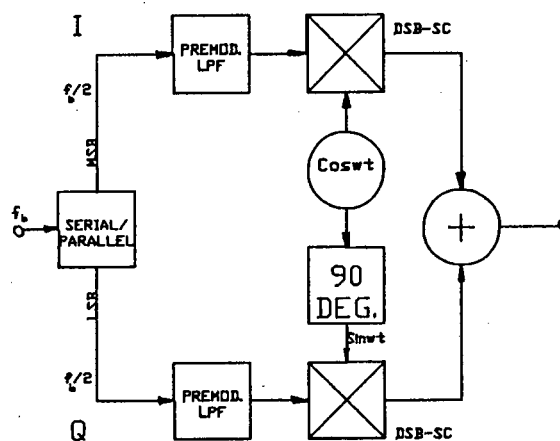


Fig. 1.5 SCHEMATIC OF A QAM MODULATOR

For 4-ary QAM there are 4 possible states for every transmitted symbol. Each symbol therefore conveys $\log_2 4 = 2$ bits of information. Symbol rate = $f_b/2$. This

means a Nyquist bandwidth of $f_b/2$ Hz, implying a theoretical spectral efficiency of 2 bits/s/Hz.

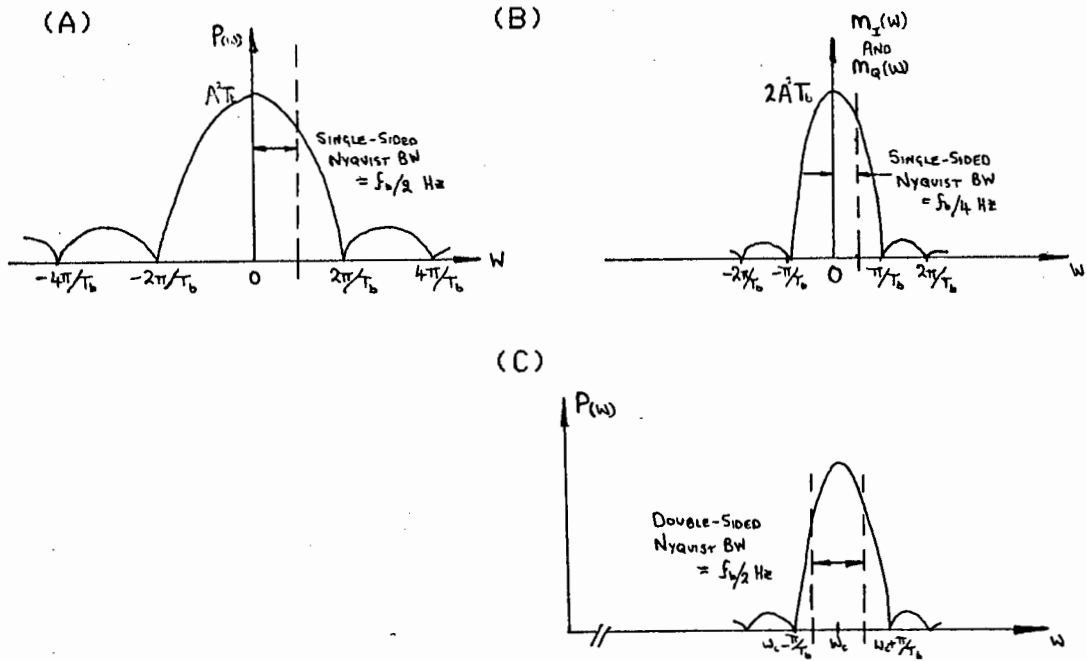


Fig. 1.6 POWER SPECTRAL DENSITY OF;

- (A) BASEBAND RANDOM BINARY DATASTREAM
- (B) I- OR Q-CHANNEL SIGNALS OUTPUT FROM THE SERIAL/PARALLEL CONVERTER
- (C) TOTAL QAM SIGNAL

SPECIAL CASES: 1. $m_i(t)$ and $m_e(t)$ are independent binary data signals (i.e. 4-ary QAM). If this is true, QAM attains the bandwidth- and power-efficiency of SSB without the stringent filtering requirements.

2. $m_e(t)$ = Hilbert transform of $m_i(t)$. For this case QAM reduces to SSB.

3. $m_i(t)$ and $m_e(t)$ are three-level duobinary signals (+1,-1,0) encoded to minimise intersymbol interference (ISI) caused by filtering. This results in Quadrature Partial Response (QPR) modulation. [1.8 - pp. 168,176]

4. $m_I(t)$ and $m_Q(t)$ take values ± 1 (i.e. NRZ datastream) yields Quadrature Phase-Shift Keying (QPSK) modulation - see section 1.1.3. However, these two techniques are only identical when $m_I(t)$ and $m_Q(t)$ are rectangular pulses.

DETECTION: Coherent detection. any errors in phase-tracking at the detector result in interference between the I- and Q-channels.

1.1.2 Frequency Modulation (FM)

In FM schemes, signal information is conveyed via frequency variation of the modulated signal. In analog communication FM is preferred to AM due to resulting noise advantages. There are additional reasons for using FM for data communication. Among these are the simple implementations of modulators and detectors.

(a) Frequency Shift Keying (FSK) modulation of a binary signal is the simplest form of FM. The modulated signal shifts abruptly between two distinct, fixed frequencies to convey the bit-pattern of the input datastream.

$$f_{FSK}(t) = A \cos(\omega_c \pm dw)t \dots (1.3)$$

Where: + or - applies if bit is 0 or 1 respectively
and: dw is the constant angular frequency offset from carrier frequency ω_c .

Let $\omega_c + dw = \omega_0$ and $\omega_c - dw = \omega_1$
then $df = (\omega_0 - \omega_1) / 2\pi$ is the frequency deviation.
(Note: $df \ll \omega_c / 2\pi$)

The "frequency deviation ratio" or "modulation index" is defined as:

$$h = df \cdot T_b \dots (1.4)$$

Where: T_b is the symbol duration (= 1/bit-rate for binary schemes).

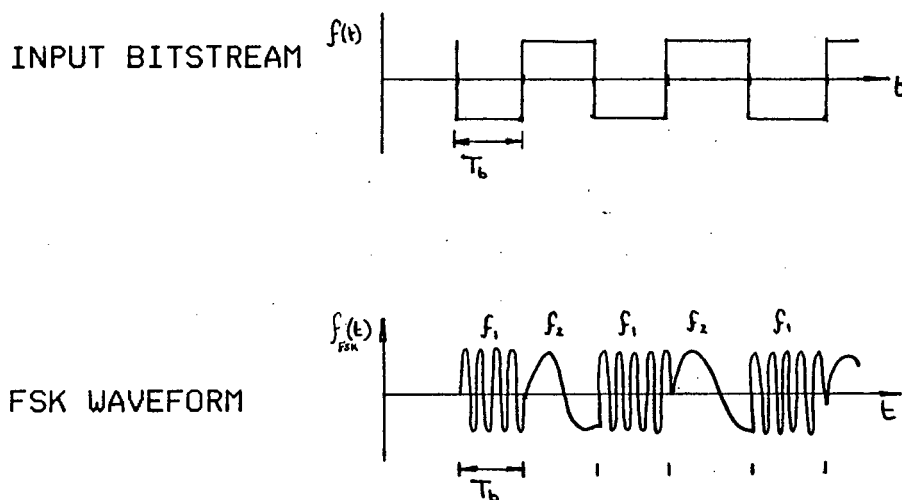


Fig. 1.7 FSK SIGNAL CORRESPONDING TO A BINARY DATA SIGNAL

The relationship between the spectrum of an FM signal and that of its corresponding baseband signal is not as simple as was the case for AM. However, an FSK signal spectrum may be derived by means of the following simple approach:

The binary FSK signal can be represented as the sum of two OOK signals; one at f_0 (the "spaces" in the input bitstream) and the other at f_1 (the "marks" in the input bitstream). Since each OOK signal has a spectrum with a $(\sin x)/x$ shape shifted to the respective carrier frequency (see Fig. 1.4), the FSK spectrum would be the sum of the two OOK spectrums.

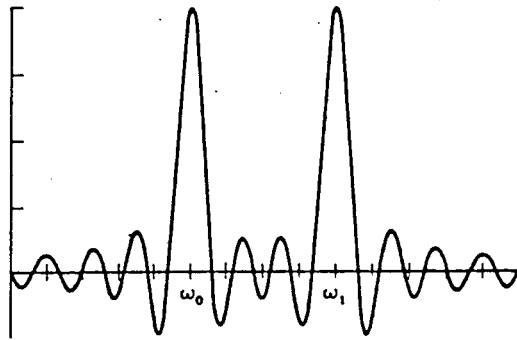


Fig. 1.8 BINARY FSK SPECTRUM

The bandwidth between the first zeros of the FSK spectrum (as shown in Fig. 1.8) is:

$$\begin{aligned} BW &= f_0 - f_1 + 2/T_b \\ &= f_0 - f_1 + 2f_b \text{ for binary FSK.} \end{aligned}$$

M-ary FSK or MFSK systems are an extension of the above principles where the binary input datastream is first converted to an m-level PAM signal.

DETECTION: Coherent or incoherent.

(b) Continuous phase FSK (CP-FSK) is a modified version of FSK in which abrupt phase-changes at the bit transition instants are avoided. Amplitude Modulation (which can cause spectral-spreading in systems exhibiting AM→PM) generated at these phase discontinuities is thereby avoided. Since the phase $\theta(t)$ is a continuous function of time, the signal itself is continuous and has thus lower spectral sidelobes than a pulsed signal. Rapid spectral roll-off and improved efficiency result.

If the phase-coherent binary CP-FSK signal is narrow-band e.g. at I.F. or R.F. then we may describe it by it's pre-envelope $u(t)$ [1.9-pp 40-42].

$$u(t) = \exp. j\{\pi(f_0 + f_1)t + \theta(t)\} \dots (1.6)$$

where the phase function $\phi(t)$ is continuous if the FSK is phase coherent.

Comparing (1.6) with the pre-envelope of a space:

$$u_{space}(t) = \exp. j\{2\pi f_0 t + \phi(0)\} \quad (0 \leq t \leq T) \dots (1.7)$$

gives:

$$\phi(T) - \phi(0) = \pi(f_1 - f_0)T = \pi h$$

where $h = dfT$ is the frequency deviation ratio and T is the symbol duration ($= 1/(\text{bit-rate})$ for binary schemes).

A space therefore increments the phase by πh and conversely a mark decrements it by πh . After S spaces and M marks, i.e. at time $(S+M)T$, we have a total phase-shift:

$$\phi\{(S+M)T\} - \phi\{0\} = (S-M)\pi h \dots (1.8)$$

[1.10]

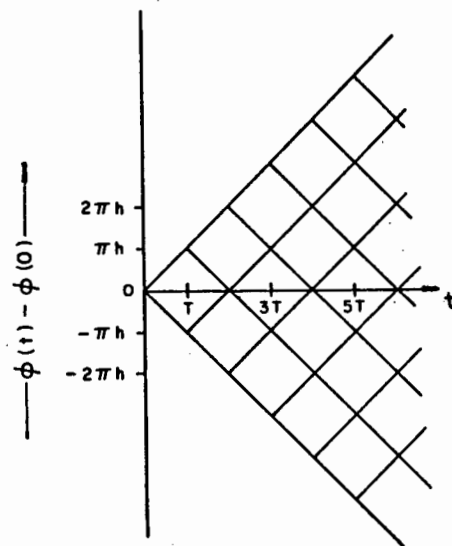


Fig. 1.9 POSSIBLE VALUES $\phi(T) - \phi(0)$

[1.10]

The phase is an even (odd) multiple of πh when $(S+M)$ is even (odd). The phase at all other times is obtained by linear interpolation.

SPECIAL CASES: Three cases of coherent FSK with small frequency deviation ratio h have received particular attention.

- (1) FSK with $h=1,0$, described in detail by Sunde [1.11] has the disadvantage of using signal power inefficiently by transmitting carrier power at frequencies f_0 and f_1 .
- (2) FSK with $h=0,71$, studied extensively by Tjhung [1.12] is claimed to be optimum under certain conditions.
- (3) FSK with $h=0,5$ (also called Minimum Shift Keying (MSK) or Fast FSK) has been singled-out as a good example for band conservation [1.13]. It is claimed to have an optimal decision structure, relatively simple receiver synchronisation requirements and an error performance about 3dB better than conventional FSK [1.10]. The optimal decision structure arises from the following: As mentioned already, the phase at times that are odd (even) multiples of T will be odd (even) multiples of πh . For the case $h=0,5$ this means that, since all phases are modulo 2π , the phase can take only the two values $\pm \pi/2$ at odd times and only the two values 0 or π at even times.

"Since each new bit is offset either $+90$ or -90 degrees from the previous bit, adjacent bits are phase-orthogonal and can be detected without ISI even though adjacent symbols overlap 50% of the time. This permits the use of symbols lasting twice the bit period, reducing occupied bandwidth. Note that in MSK the symbols are cosine-weighted so that adjacent orthogonal symbols always add to

form a constant amplitude signal. Although MSK is a special case of two-frequency FSK, the overall result is the same as that for a double binary system using the alternate transmission of two overlapped phase-quadrature channels. Such a system could theoretically operate in the same Nyquist bandwidth as QPSK. However, due to the constant-amplitude constraint on MSK requiring cosine-weighted symbols, bandwidth is slightly more than twice the Nyquist bandwidth for 4-level systems. Thus MSK may be regarded as either a less-than-ideal (but typical) 4-level system, or a nearly-ideal 2-level system." [1.14]

"Because phase-shifts are precisely controlled in MSK, coherent phase detection can be employed in MSK systems to provide the same error-rate as for PSK instead of the relatively poor performance usually associated with FSK systems." [1.14]

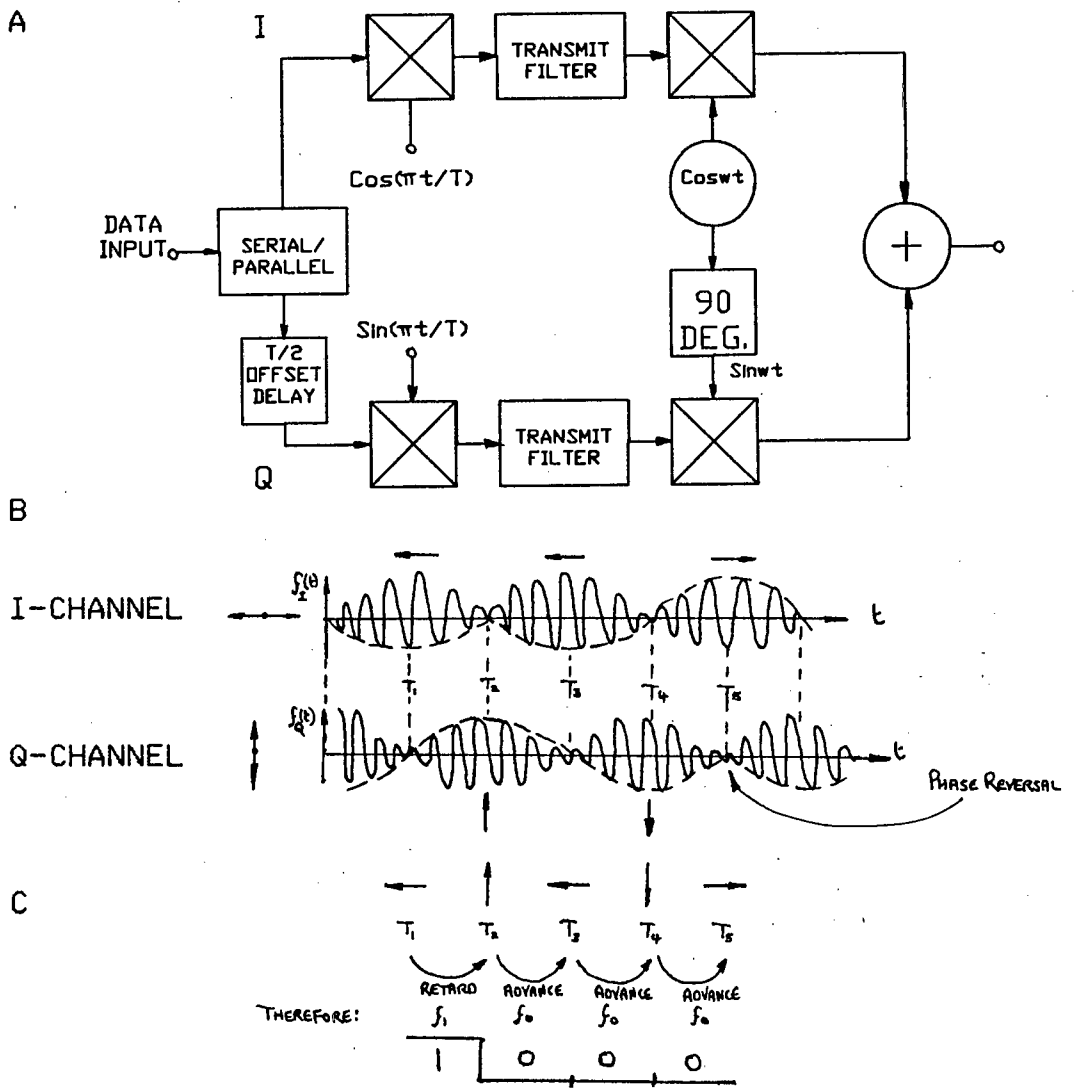


Fig. 1.10 MSK MODULATOR MODEL: (A) SCHEMATIC
 (B) SIGNALS
 (C) PHASOR SEQUENCE

As described by deBuda [1.10], the case of FSK with $h=0,71$ is only optimum for a detector decision interval equal to the bit duration interval T_b . Low modulation index FSK retains useful phase information beyond the time of bit transmission. By extending the detector decision interval to $2T_b$, MSK takes maximum advantage of this and achieves improved performance.

MSK is more power-efficient than CP-FSK ($h=1,0$) since for MSK no power is transmitted at frequencies f_0 or f_1 , leaving more power available for signalling. A relatively simple self-synchronising implementation is, however, possible.

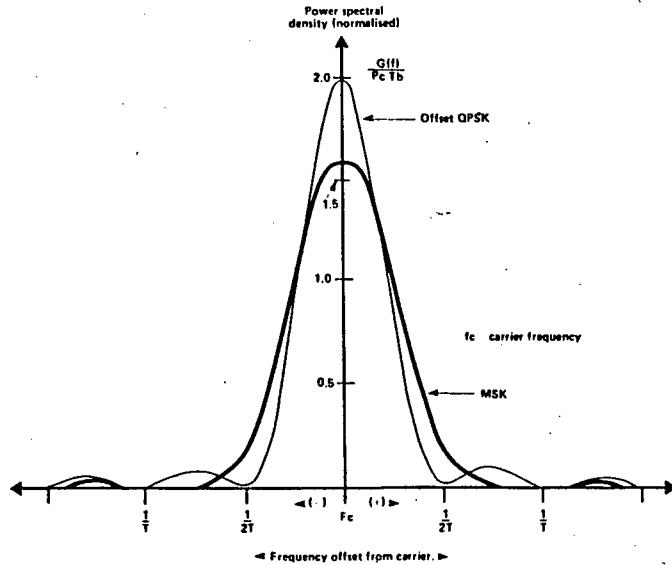


Fig. 1.11 POWER SPECTRAL DENSITY OF MSK AND OFFSET-QPSK [1.18]

1.1.3 Phase Modulation

(a) Binary Phase-Shift Keying (BPSK) is the simplest form:

$$f_{\text{BPSK}}(t) = A \cos[\omega_c t + \theta(t)] \dots (1.9)$$

Where: $\theta(t) = 0$ (I/P bit = "1")

$\theta(t) = \pi$ (I/P bit = "0")

As mentioned in section 1.1.1(b) the above expression is equivalent to:

$$f_{\text{BPSK}}(t) = A m(t) \cos \omega_c t$$

for $m(t) = \pm 1$

(b) Quadrature Phase-Shift Keying (QPSK) conveys information by encoding two bits at a time into one of four possible carrier phases spaced $\pi/2$ radians apart.

$$f_{\text{QPSK}}(t) = A \cos[\omega_c t + \theta(t)] \dots (1.10)$$

Where:

1 st I/P Bit	2 nd I/P Bit	$\theta(t)$
0	0	0
0	1	$\pi/2$
1	1	π
1	0	$3\pi/2$

[Rad.]

TABLE 1.0

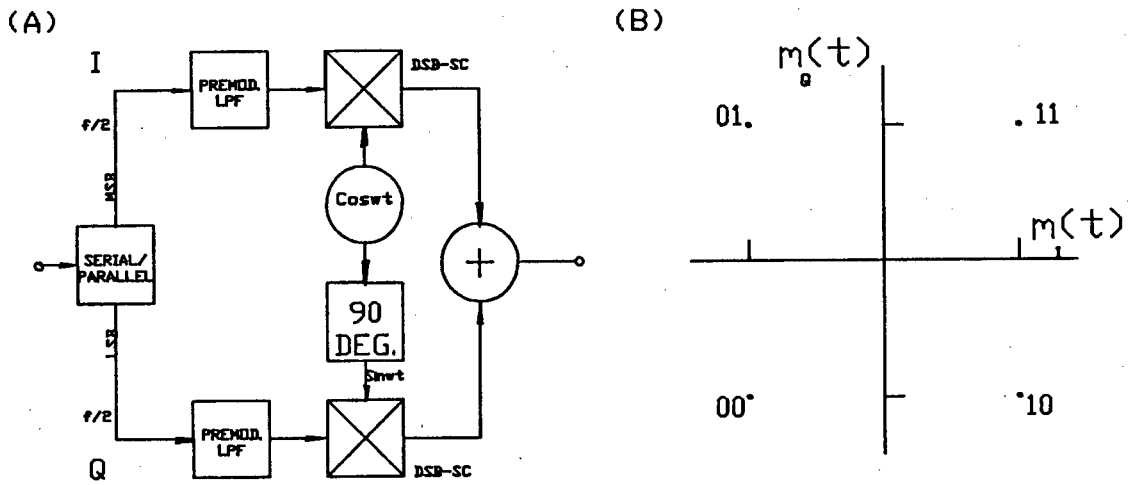


Fig. 1.12 (A) QPSK MODULATOR SCHEMATIC
(B) CORRESPONDING SIGNAL-STATE SPACE DIAGRAM

As shown in Fig. 1.12, the QPSK modulator is implemented by BPSK modulating two phase-quadrature carriers with the MSB and LSB respectively of each input bit pair.

$$f_{\text{QPSK}}(t) = A[m_{\text{MSB}}(t)\cos\omega_c t + m_{\text{LSB}}(t)\sin\omega_c t] \dots (1.11)$$

(For $m(t) = \pm 1$)

The form of the QPSK power spectral density function is identical to that of the individual orthogonal BPSK signals (symbol rate= $f_b/2$) of which it is comprised.

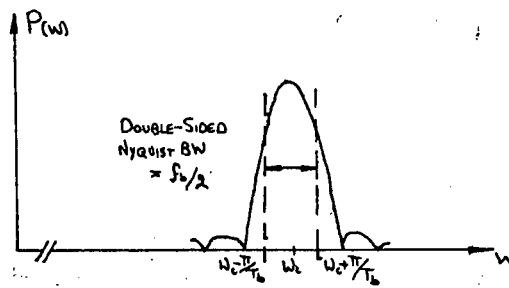


Fig. 1.13 QPSK SPECTRUM

Hence a spectral efficiency of 2 bits/s/Hz is theoretically possible for QPSK for ideal Nyquist filtering. However, using the FCC definition of bandwidth as that containing 99% of total signal power, the channel bandwidth must be extended to approx. the -13dB point. i.e. $BW_{-13dB} = 1.92 \cdot \text{Min. BW}$

That is, a practically obtainable spectral efficiency is approx. 1.04 Bits/sec./Hz.

Note however, that the phase of the QPSK (and BPSK) signal can shift abruptly by π radians. This is equivalent to 100% AM and causes sideband regeneration when the signal is passed through non-linear circuit elements.

(c) Offset-Keyed QPSK (OK-QPSK) is a modified version of QPSK where the Q-channel is shifted by $T_b/2$ seconds relative to the I-channel. Consequently, when the I- and Q-channels are added together, the resulting signal can shift abruptly by $\pi/2$ radians at most. (But shifts can occur every $T_b/2$ seconds, compared to every T_b seconds for QPSK). This scheme offers advantages over QPSK with regard to spectral efficiency, sideband regeneration and

synchronisation.

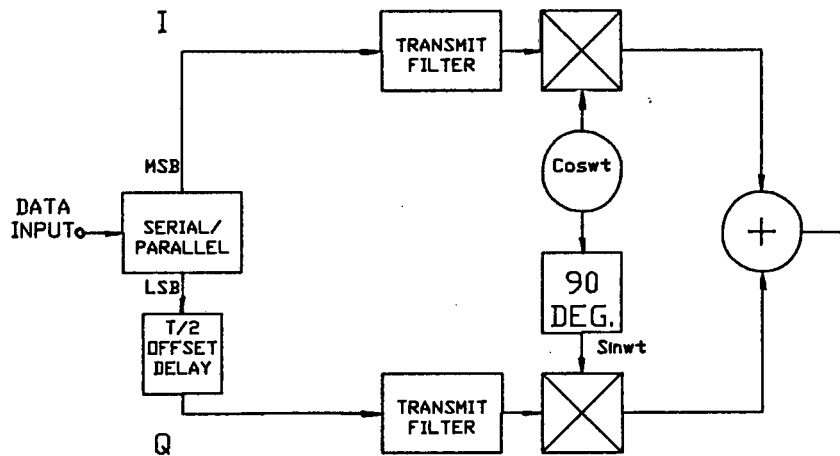


Fig. 1.14 OK-QPSK SCHEMATIC

See Fig. 1.11 for power spectral density of OK-QPSK.

Coherent detection is by definition essential for any phase modulation scheme. Most techniques for derivation of the phase-coherent carrier at the receiver result in π radian phase ambiguities. In order to solve this problem, two special forms of PSK have been developed:

- (1) Differentially-Encoded PSK (DE-PSK) conveys information via transitions in carrier phase (e.g. no transition = "1", transition = "0"). This solves the problem of π radian phase ambiguity. However, since a decision error on the current bit induces another error on the subsequent bit, performance of DE-PSK is slightly inferior to that of PSK.
- (2) Differential PSK (DPSK) is another scheme in which information is differentially encoded. However, unlike DE-PSK, no coherent phase-reference is extracted at the detector. Here the signal from the previous bit-interval is used as a phase-reference for the current interval. Since the phase-reference signal is not smoothed over many bit-intervals, performance of DPSK is worse than that of DE-PSK.

1.1.4 Hybrid modulation Schemes

(a) Amplitude and Phase-Shift Keying (APK) is an AM/PM hybrid scheme.

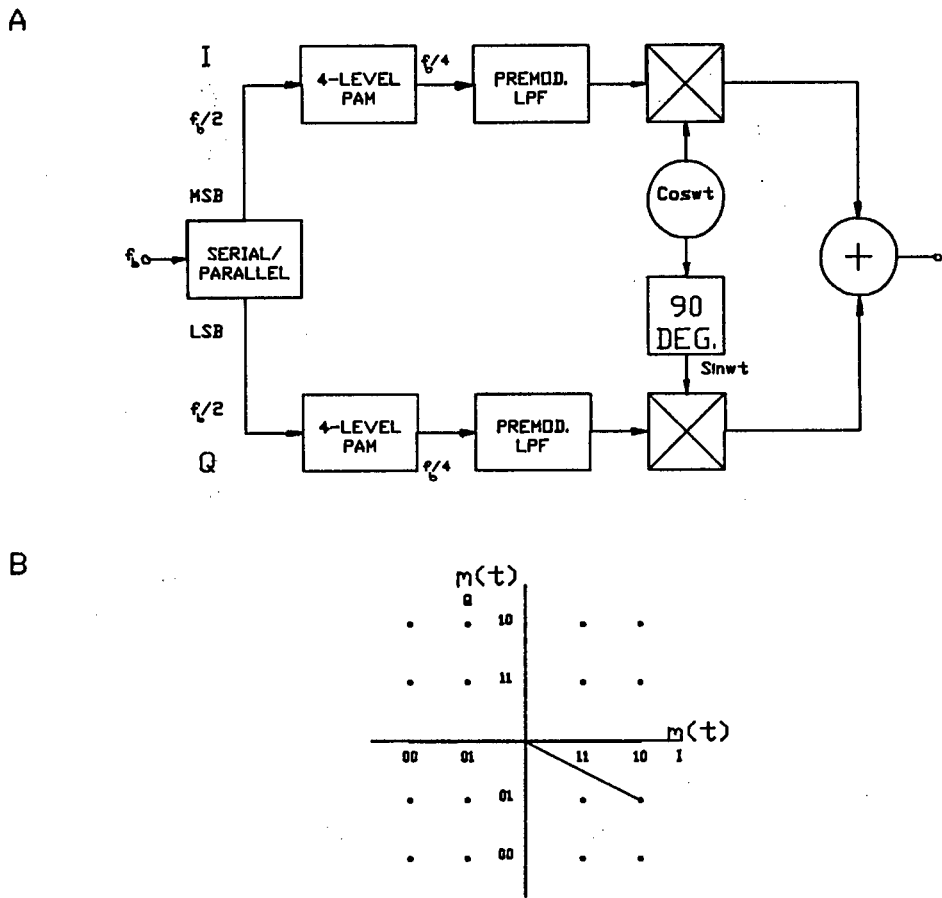


Fig. 1.15 (A) 16-ARY APK MODULATOR SCHEMATIC WITH ASSOCIATED WAVEFORMS
(B) CORRESPONDING SIGNAL-STATE SPACE DIAGRAM

As can be observed from Fig.1.15(B), for 16-ary APK there are 16 possible states for every transmitted symbol. Each symbol therefore conveys $\log_2 16 = 4$ bits of information. These symbols are transmitted at a rate equal to $1/4$ times the bit-rate. For ideal Nyquist filtering this implies a spectral efficiency of 4 bits/s/Hz.

As the name APK suggests, symbols are identified by phase- as well as amplitude-values. Note that a symbol may take one of 3 different phase values per quadrant, as well as 3 different amplitude values. This causes difficulties in detection of m-ary APK.

1.2 A Comparative Evaluation Of Modulation Scheme Performance

1.2.1 Bandwidth Efficiency

According to Oetting [1.15], for frequencies far from the centre frequency (i.e. large $(f-f_c)T$), the spectrum of AM and PM signals falls-off as f^{-2} , while that of CP-FM signals falls-off as f^{-4} . This can be confirmed by considering that all AM signal spectra are similar in shape to the baseband spectra, merely having the centre frequency shifted from $f=0$. These spectra will consequently have power spectral density functions of the form $(\sin x/x)^2$, similar to that of the baseband random binary data signal. This is also true for BPSK which is merely a special form of DSB-SC. Since addition of two similar signals in phase-quadrature does not affect the shape of the power spectral density function, we can conclude that a $(\sin x/x)^2$ form of power spectral density function is true for all AM and PM signals. Determining the spectral density of FM signals is more difficult. We can however observe the f^{-4} spectral fall-off by examining the power spectral density function of MSK:

$$G_{\text{MSK}}(f) = \frac{8P_c T_b (1 + \cos 4\pi f T_b)}{\pi^2 (1 - 16T_b^2 f^2)^2} \dots (1.12)$$

while that for OQPSK is:

$$G_{\text{OQPSK}}(f) = 2P_c T_b \left[\frac{(\sin 2\pi f T_b)}{2\pi f T_b} \right]^2 \dots (1.13)$$

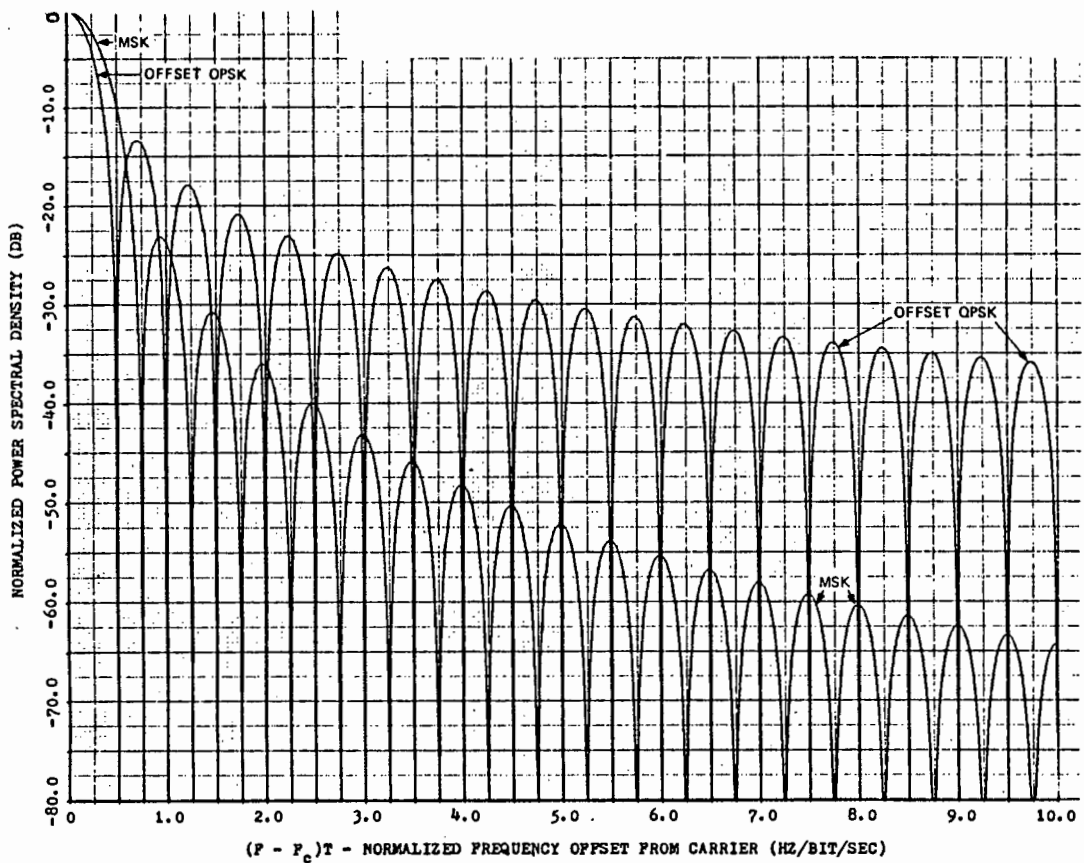


Fig. 1.16 POWER SPECTRAL DENSITIES OF MSK AND OK-QPSK
[1.16]

One may note the width of the main lobe of the MSK spectrum is 1,5 times greater than that of the OK-QPSK spectrum. A good measure of the "compactness" of the spectrum of a particular modulation scheme is the "fractional out-of-band power" P_{OB} defined as:

$$P_{OB} = 1 - \frac{\int_{-B}^B G(f) df}{\int_{-\infty}^{\infty} G(f) df} \dots (1.14)$$

P_{OB} is plotted as a function of bandwidth B:

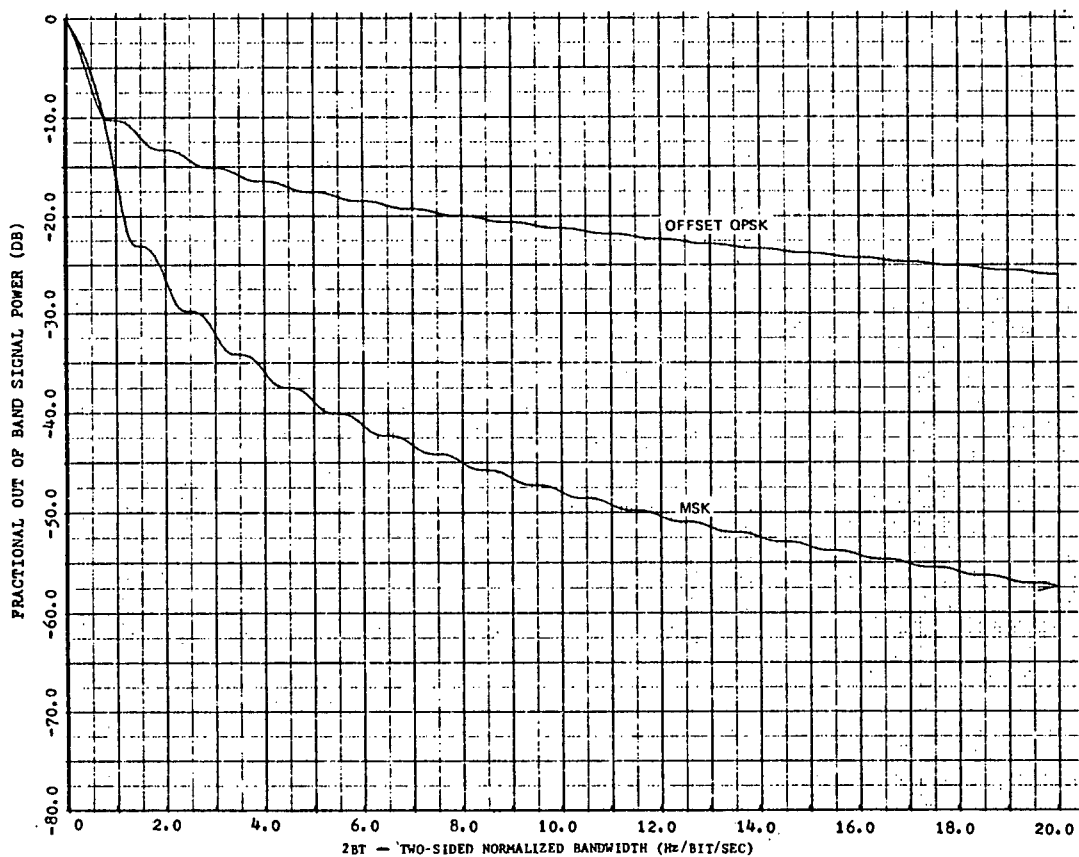


Fig. 1.17 FRACTIONAL OUT-OF-BAND POWER [1.16]

One should note that the f^{-2} fall-off of PM signal spectra assumes that these PM systems permit abrupt phase-transitions to occur. If phase-transitions can be made to occur more smoothly, improved spectral characteristics may be achieved. Modifications can also be made to AM schemes, where a type of continuous-phase AM also exhibits a spectrum that falls-off as f^{-4} [1.17]. Post-modulation filtering can always be used to reduce sidelobes, but with a consequent degradation of performance.

1.2.2 BER vs. E_b/N_0 Performance In An AWGN Environment

Table 1.1 [1.15] provides a comparison of bandwidth efficiency or "signalling speed" (equal to f_b/W , where f_b is the data rate and W is the I.F. bandwidth.) Also listed in Table 1.1 is the corresponding E_b/N_0 required to achieve the indicated bandwidth efficiency and a Bit Error

Ratio (BER) $< 10^{-4}$ for the particular modulation scheme
(i.e. degrading effects of finite bandwidth are included.)

Note:

$$E_b/N_0 = (C/N) \cdot B_n/f_b \quad . . . \quad (1.15)$$

Where: E_b = Average energy per bit = CT_b
 f_b = Bit rate = $1/T_b$
 T_b = Unit bit duration
 C = Average carrier power
 N = Total noise power
 N_0 = Noise power spectral density
 B_n = Receiver noise bandwidth

E_b/N_0 is preferred to C/N for comparison of different systems since it is independent of receiver noise bandwidth.

TYPE	MODULATION SCHEME	SPEED (b/s/Hz)	E_b/N_0 (dB)	REF.
AM	OOK-Coherent Detection	0,8	12,5	1.12
	OOK-Envelope Detection			
	QAM	1,7	9,5	1.18
	QPR	2,25	11,7	1.19
FM	FSK-Noncoherent Detection ($h=1,0$)	0,8	11,8	1.20
	CP-FSK-Coherent Detection ($h=0,71$)			
	CP-FSK-Non-Coherent Det. ($h=0,71$)	1,0	11,2	1.12
	MSK (i.e. $h=0,5$)	1,9	9,4	1.21
	MSK-Differential Encoding	1,9	10,4	1.21
	PM	BPSK-Coherent Detection	0,8	9,4
DE-BPSK		0,8	9,9	1.12
DPSK		0,8	10,6	1.22
QPSK		1,9	9,9	1.23
DQPSK		1,8	11,8	1.24
OK-QPSK				
8-ary PSK-Coherent Det.		2,6	12,8	1.23
16-ary PSK-Coherent Det.		2,9	17,2	1.25
AM/PM	16-ary APK	3,1	13,4	1.25

TABLE 1.1 RELATIVE SIGNALLING SPEEDS OF REPRESENTATIVE MODULATION SCHEMES

At this point it is obvious that the schemes displaying superior speed vs. E_b/N_0 performance for a given BER are:

1. QAM

2. QPR
3. MSK
4. QPSK
5. OK-QPSK
6. M-ary PSK ($M > 8$)
7. APK

Although M-ary PSK and APK performance is exceptionally good, these techniques require demodulator/detectors which are an order of complexity higher than those for the other modulation techniques listed above. Consequently, we shall limit our attention at this stage to techniques 1-5.

Remembering that QPSK and QPR can be regarded as special forms of QAM (as noted in section 1.1.1(e)), it is important to notice the similarity also between OK-QPSK and MSK. Examining figures 1.10 and 1.14 it becomes apparent that MSK can be regarded as a special case of OK-QPSK with sinusoidal symbol weighting.

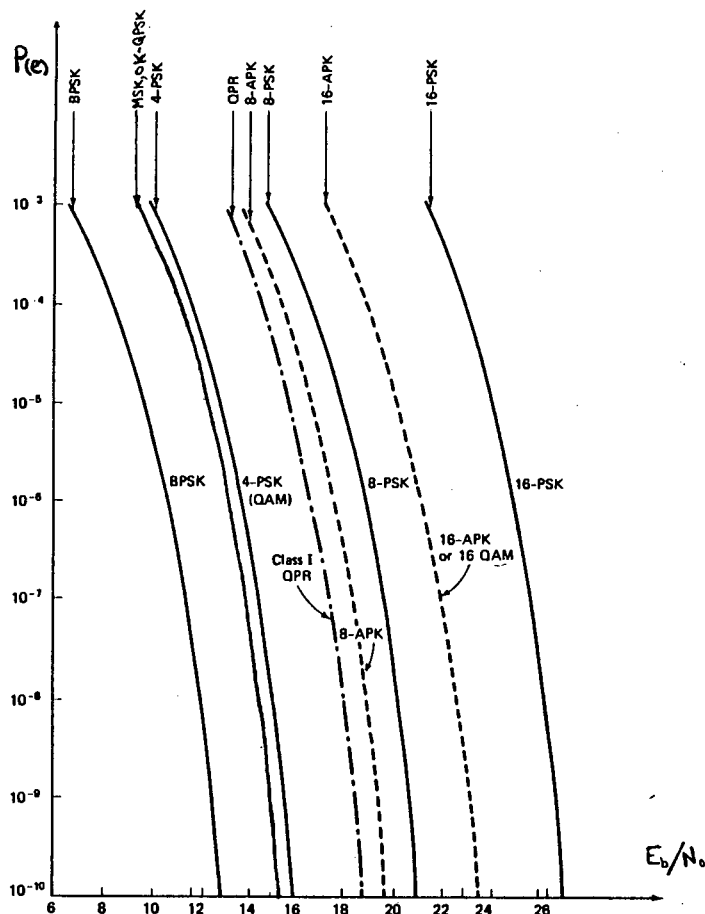


Fig.1.18 BER vs. E_b/N_0 FOR QPSK (QAM), QPR, MSK, OK-QPSK
 [1.8 p.71, 1.18 Fig. 15]

Both MSK and OK-QPSK achieve the matched-filter coherent detection BER performance of antipodal PSK on linear, infinite bandwidth, White Gaussian Noise (WGN), perfect reference channels. However, if either an MSK or OK-QPSK waveform is band-limited and then hard-limited, the degree of regeneration of filtered sidelobes is less than is the case for conventional QPSK. [1.19]

Another observation which has been made for a channel containing a hard-limiter is the following: Both MSK and OK-QPSK require a certain critical bandwidth. For narrower channels, performance rapidly degrades due to intersymbol interference and pulse distortion. BER performance of MSK is found to be superior to that of OK-QPSK only when the channel bandwidth exceeds approx. 1.1 times the binary

data-rate. [1.16] This is due to the broader main lobe of the power spectral density of MSK as compared to OK-QPSK. (See Fig. 1.16).

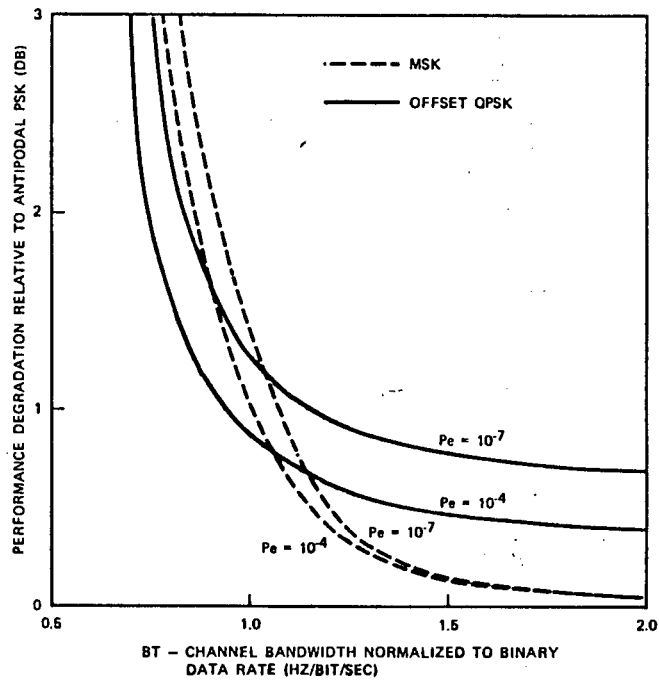


Fig. 1.19 MSK AND OK-QPSK E_b/N_0 PERFORMANCE DEGRADATION W.R.T. IDEAL ANTIPODAL PSK AS A FUNCTION OF CASCADED FILTER NOISE BANDWIDTH WITH ERROR PROBABILITY AS A PARAMETER [1.16]

For a channel containing an AM/PM system element rather than a hard-limiter, Poza and Berger [1.20] report that the E_b/N_0 advantage of MSK over OK-QPSK extends to slightly narrower bandwidths than the $1,1 \cdot f_b$ crossover bandwidth for the hard-limiter case.

1.2.3 Effects of Adjacent Channel Interference

Performance degradation due to the presence of an in-band interferer is another feature for comparison of the different modulation schemes. A measure of this is the "system gain degradation", i.e. the additional E_b/N_0 required to maintain a specified BER for a given carrier-to-interference ratio C/I [dB]. This is also dependent on

the nature of the interfering signal in terms of it's "Peak Factor" PF where:

$$PF = \frac{\text{Peak value of interfering envelope}}{\text{Mean-square value of interfering envelope}}$$

Once a suitable modulation scheme has been chosen, the receive filter is specified to ensure that within the preassigned channeling plan, adjacent channels are sufficiently suppressed. A frequently used figure for the permissible gain degradation resulting from adjacent channel interference is about 1dB.

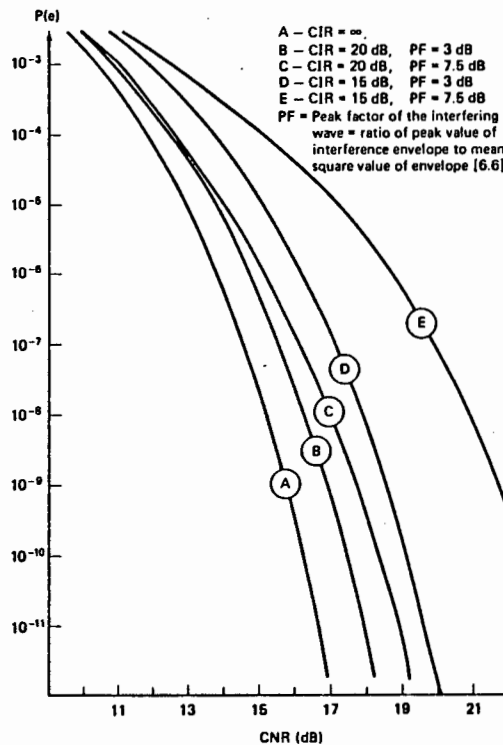


Fig. 1.20 QPSK PERFORMANCE IN THE ADJACENT-CHANNEL INTERFERENCE ENVIRONMENT OF TWO INTERFERERS

[1.8 p.131]

1.2.4 Effects of Delay Distortion

Most delay distortion observed on line-of-sight radio links is introduced by the radios and not the channel. If the distortion observed on the received signal can be

modelled by passage of the transmitted signal through a linear filter, then:

$$\begin{aligned} \text{GROUP DELAY} &= -d\theta/d\omega \\ &= \text{-derivative of filter} \\ &\quad \text{phase-freq. characteristic} \end{aligned}$$

For no distortion of the modulated signal, we require:

$$\text{Group Delay} = \text{Constant (i.e. } -d\theta/d\omega = \text{const.)}$$

$$\text{i.e. } \theta = \omega t_{\text{GROUP}} + C$$

For linear distortion: Group delay = $A\omega + B$ (A,B const.)

For quadratic distortion: Group delay = $a\omega^2 + b\omega + c$ (a,b,c const.)

Some modulation schemes are severely affected by one type of distortion and not the other. This is clearly shown in Table 1.2 which lists performance of different schemes, taking the case for which maximum differential delay (relative to mid-band delay) is equal to the symbol duration. Performance of four of the five modulation techniques on which we have focussed our attention are shown to be identical, with QPR displaying severe performance degradation in the presence of linear distortion.

MODULATION SCHEME	E_b/N_0^*	
	LINEAR	QUAD.
QAM	15,8	9,8
QPR	>25	
MSK	15,8	9,8
QPSK	15,8	9,8
OK-QPSK	15,8	9,8

(dB)

(dB)

* For bit error ratio of 10^{-4}

[1.15,1.20]

TABLE 1.2

1.2.5 Effects of Fading

- Fading may be caused by:
- (a) Two resolvable multi-path components.
 - (b) A large number of equal amplitude multi-path components.

For case (a), the signal from the secondary path may be regarded as an in-band interferer and relative performance of the different modulation techniques can be obtained from section 1.2.3.

For case (b), it has been found that the "cumulative amplitude distribution" of deep fades:

$$P(v < L) \propto L^2 \quad \text{where:}$$

v = envelope voltage of the randomly fading signal normalised to it's unfaded level

L = any specified reference level

This square-law is known as "Rayleigh fading"

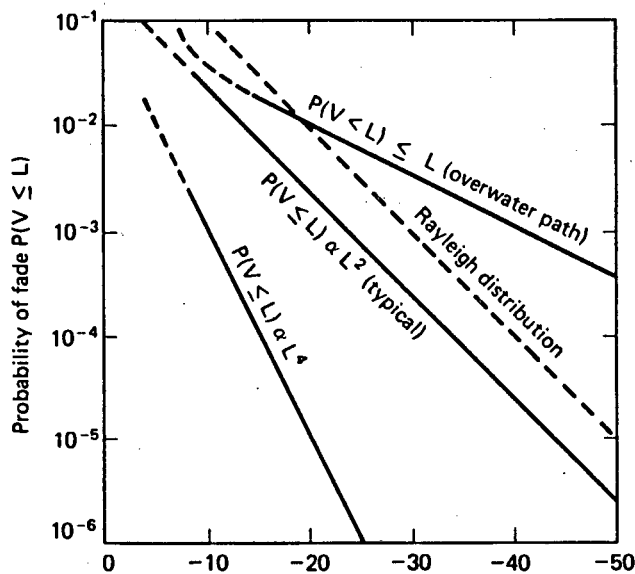


Fig. 1.21 CUMULATIVE AMPLITUDE DISTRIBUTIONS OF FADING SIGNALS [1.8]

Performance of the various modulation techniques for a Rayleigh fading channel is summarised in Table 1.3.

MODULATION SCHEME	AVERAGE E_b / N_0 *
MSK	14
MSK-Differential Encoding	17
QPSK	13,5
DQPSK	20
OK-QPSK	13,5

[dB]

* For BER of 10^{-2}

Assumes optimum variable threshold

Assumes 3-bit observation interval

TABLE 1.3

[1.15]

1.2.6 Sensitivity to Errors in Local Reference

Error-rate performance sensitivity to noisy phase-references for various modulation schemes has been investigated by Matyas [1.21]. A comparison is made of performance loss L , representing E_b/N_0 required to overcome the noisy phase-reference effect on error-rate.

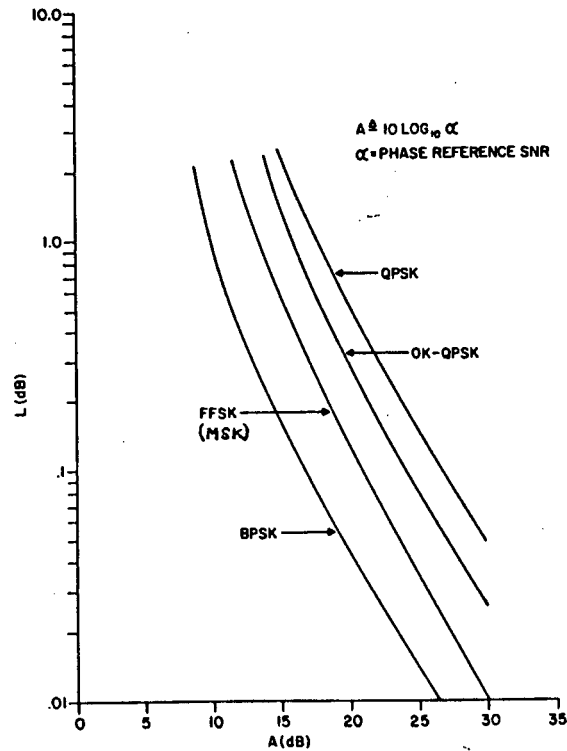


Fig. 1.22 DETECTION LOSSES AS FUNCTION OF PHASE REFERENCE SNR [1.21]

The results demonstrate how both MSK and OK-QPSK benefit from the alignment offset between channels. This offset results in a decrease in average inter-channel interference detected by the receiver.

"Because the decision on the received signal is based on integration over two bit periods during which the interchannel component may change by 180 degrees thereby effectively cancelling its interference, error-rate performance is improved relative to QPSK. Cosine weighting

further improves MSK relative to OK-QPSK by reducing the inter-channel interference component." [1.21]

1.2.7 Effects of Non-linear Amplification

As mentioned in section 1.1.2(b) carrier phase-reversals produced in some modulation schemes such as FSK, BPSK and QPSK cause envelope modulation nulls when the signal passes through a bandpass filter. This envelope fluctuation (or AM) is undesirable (as mentioned in section 1.1.1) since subsequent non-linear amplification enhances sideband energy, increases adjacent channel interference and causes AM/PM distortion effects. Both MSK and OK-QPSK avoid phase-discontinuities by staggering the I- and Q-channels, producing a constant-amplitude phasor.

1.2.8 Cost and Complexity

Cost and complexity of implementing any modulation scheme is very dependent on how the system as a whole is to be realised. Once an evaluation can be made, the result may point so favourably in the direction of a certain technique, that the advantage in cost could outweigh any deficiencies associated with the particular scheme. The overall evaluation approach then alters to one of assessing the extent to which system performance is being sacrificed by opting for the cheaper scheme.

1.3 Conclusions

The choice of modulation technique has been narrowed-down to a short-list of 5 schemes. At this stage it is impossible to say which of these will best meet our requirements, as a final assessment can only be made when details regarding the rest of the system are known.

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CHAPTER 2

DATA LINK SPECIFICATIONS

2.0 Introduction

From the start it has been clear that a system acceptable to both local and overseas telecommunications authorities will need to meet the respective specifications of both, as well as international regulations such as those of the Federal Communications Commission (FCC) and International Radio Consultative Committee (CCIR). This has resulted in the final specification comprising the most stringent elements extracted from all of the above. In addition, a limited flexibility on the part of the user in terms of channel capacity, as well as the practical problem of obtaining licences overseas for operation in congested 15GHz and 18GHz bands has led to modifications of the original specification.

2.1 Specifications

Frequency range:	21,8 to 23,0 GHz. (23 GHz band)
R.F. Channel Bandwidth:	5,0 MHz.
Transmission Capacity:	2,048 MBit/s FULL DUPLEX.
Transmit. Freq. Stability:	*-20 ppm.
Transmitted Spectrum:	To meet mask (FCC/CCIR) (See Fig. 2.0).
Transmitter Power:	21,7 dBm. (150mW)
BER:	<10 ⁻⁷ .
AGC Range:	50 dB.
Antenna Size:	60 cm.
Range:	100 m to 20 Km.
Power Supply:	240V a.c., 24-48V d.c.

Operating Temperatures: -10°C to +55°C
 Humidity: 95%
 Interface: HDB3 120Ω balanced, all other aspects as per CCITT (International Telephony and Telegraphy Committee) recommendation G703.
 System Diversity: No diversity; no protection switching.

POWER DENSITY REFERRED TO THE NOMINAL CENTRE FREQUENCY (f₀)
 FOR 14 MHz OR LOWER SPACING

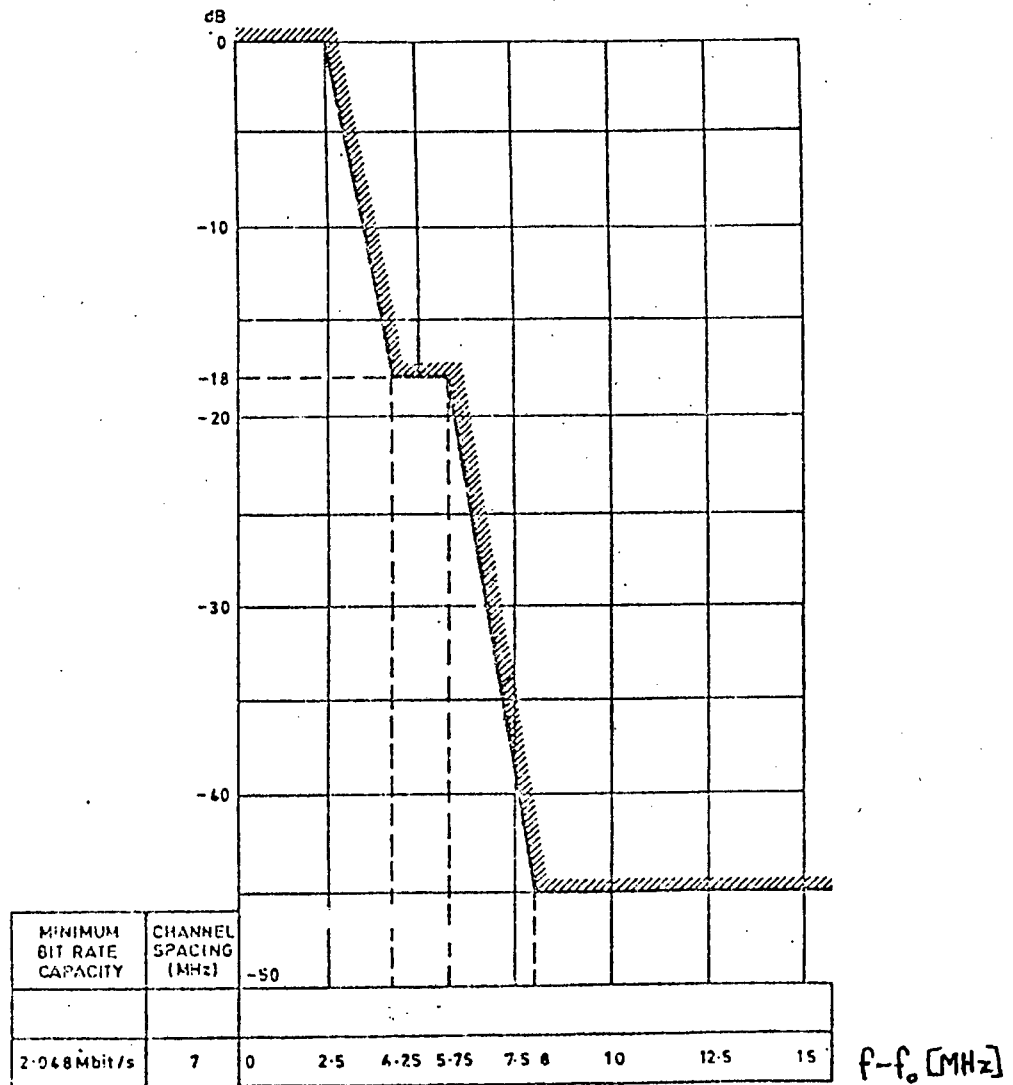


Fig. 2.0 FCC/CCIR MASK

2.2 Applications

Foreseen applications for the proposed data link include the following:

1. Providing communication links for the Local Area Network (LAN).
2. As back-up systems for PCM cable routes.
3. As a permanent installation for communication between telephone exchanges and concentrators.
4. For emergency operation during working repairs of PCM routes.

2.3 Design Priorities

Of primary importance in development of this data link is the minimization of final product cost. Meeting all of the specification requirements mentioned in section 2.2 becomes trivial if the system complexity and hence cost are without restriction.

Another fundamental requirement is reliability and robustness. The equipment produced will be expected to operate continuously for long periods of time in outdoor extreme conditions, with maximum mean time between system failures.

Future requirements of higher channel capacities cannot be excluded. The system configuration chosen must therefore be conducive to future expansion to higher data rates.

The equipment must in addition be lightweight, portable and quick and simple to install.

CHAPTER 3

SYSTEM DESIGN CONSIDERATIONS

3.0 Introduction

Decisions regarding three inter-related aspects are of fundamental importance in developing the system to meet the given specifications. These are: modulation technique, system configuration and R.F. transmission (i.e. noise budget, system gain etc.).

3.1 Modulation Technique

3.1.0 Selection

The decision regarding choice of modulation technique has been largely dominated by consideration of implementation cost. Any modulation scheme involving AM or PM requires the use of expensive microwave components such as those employing PIN diodes. The fact that the spectrum of a continuous-phase FM signal falls-off as f^{-4} as compared to f^{-2} for AM and PM (as described in section 1.2.1) is another point in favour of some form of CP-FM. In addition, the ± 20 ppm transmitter frequency stability required by the design specification makes it virtually obligatory to use an electronically-tuned R.F. source locked onto a crystal oscillator harmonic. This makes an FM technique even more attractive, since the circuitry required for frequency-modulating the R.F. carrier already exists.

Of the CP-FSK schemes considered in Chapter 1, MSK stands-out as the one whose performance in terms of parameters such as BER vs. SNR, bandwidth efficiency etc. is comparable to that of expensive schemes such as OK-QPSK. In addition, the fact that a relatively simple self-

synchronising implementation of MSK exists makes MSK an obvious choice.

3.1.1 Implementation Problems Foreseen

- (a) Arranging for full-duplex operation can be a problem in a system employing baseband modulation of the R.F. carrier. This is because no reference carrier signal exists at the receiver, since it is baseband modulated for transmission in the reverse direction. (This reasoning assumes only one R.F. source at each end of the link.) Some means must therefore be devised to obtain a carrier signal at each end suitable for down-converting the received information signal.
- (b) A fundamental requirement for MSK modulation is precise control of modulation index or "frequency deviation ratio" h (see Eqn.1.4). Variation in h will produce phase-shifts $\theta \neq \pi/2$. A theoretical analysis of this problem is performed in Appendix A. It concludes that control of the modulation index to within 3,6% of its nominal value will ensure a negligible contribution to the total bit errors, for a system $BER \leq 10^{-7}$.

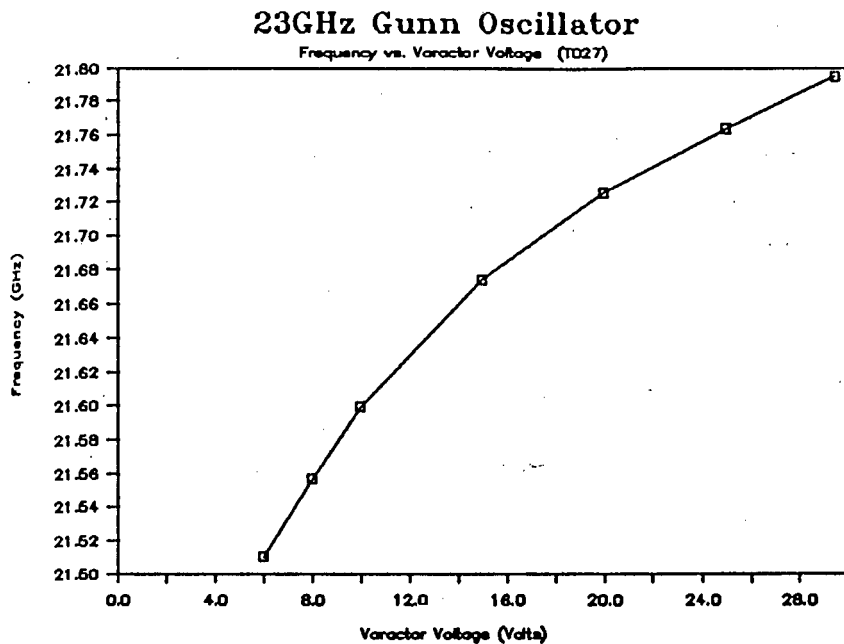


Fig. 3.0 VARACTOR DIODE FREQ. vs. VOLTAGE CHARACTERISTIC

The required precision in control of modulation index may be difficult to achieve due to the frequency/voltage characteristic of the varactor diode to be used in the R.F. source. Variations in temperature which would drift oscillator frequency cause the locked-source control-loop to adjust the voltage applied to the varactor. In this way the operating-point shifts along the varactor freq. vs. voltage characteristic. As can be seen in Fig. 3.0, the value f/v can vary by as much as a ratio of 5:1. Some form of compensation or feedback will therefore be essential to ensure that the correct signal voltage v is applied at any given temperature to produce the precise frequency-shift required.

3.2 System Configuration

Basic requirements of the system configuration are to:

- (1) Permit full-duplex operation,

- (2) Ensure image suppression,
- (3) Limit spurious transmissions.

3.2.1 Suggested Configurations

(a)

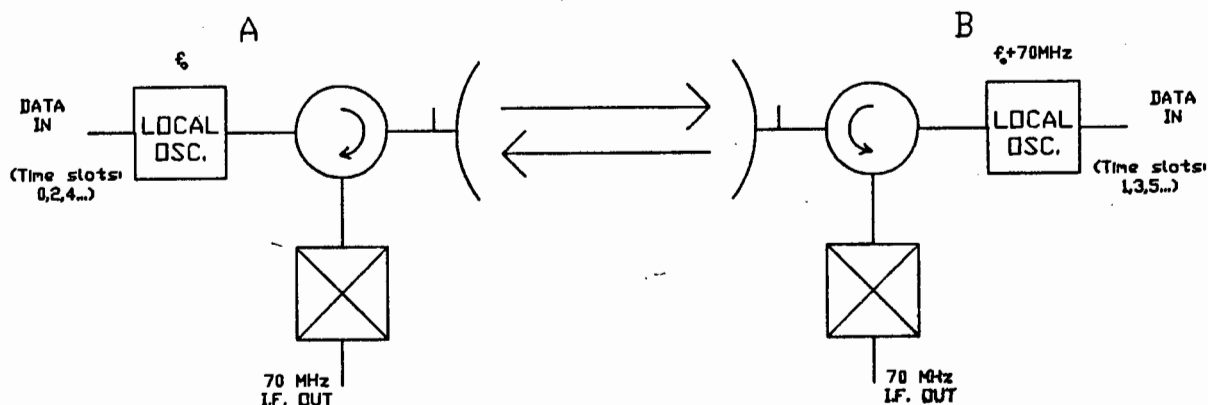


Fig. 3.1 DUPLEX BY LOOP-TURNAROUND

In this configuration, transmission only occurs in one direction at a time. Each transceiver transmits in bursts, alternating with bursts from the opposite side. In this way an unmodulated carrier signal for down-conversion purposes is made available at the end which is receiving the particular transmission burst. To achieve the required continuous duplex capacity of 2,048 MBit/s therefore, actual transmission bursts occur at data-rates in excess of 4,096 MBit/s.

Problems:

1. No image suppression. When A transmits, the I.F. filter at B will admit all the difference-frequency spectral components output by the mixer. These include not only the $(f_0 + 70) - f_0$ components, but also the $(f_0 + 140) - (f_0 + 70)$ components (which may include the frequency band of the neighbouring channel.)

2. Duplex operation is achieved by complicated and wasteful means. Extensive digital control is required to hold the incoming 2 MBit/s datastreams in buffer stores at both ends, "packetise" the data and convert it into 4 MBit/s datastreams transmitted alternately in opposite directions for half the time. It is wasteful since transmission time and hence bandwidth is wasted during loop-turnaround. The minimum time period required to achieve loop-turnaround is determined by the acquisition times of the phase-locked-loops (PLL) used in the coherent carrier extraction circuitry. The minimum PLL acquisition times, in turn, are fixed by the minimum PLL capture-range required for the specified transmitter R.F. frequency stability.
3. Emissions from the receiver mixer at frequency $f_0 + (f_0 + 70\text{MHz.})$ as well as harmonics and intermodulation products thereof may "leak" back through the circulator (undergoing an approx. 30dB attenuation) to the antenna. The power-level of these spurious out-of-band emissions is required by FCC/CCIR regulations to be at least 45dB below the transmission reference level at channel centre-frequency. (See FCC/CCIR mask in Fig. 2.0)

(b)

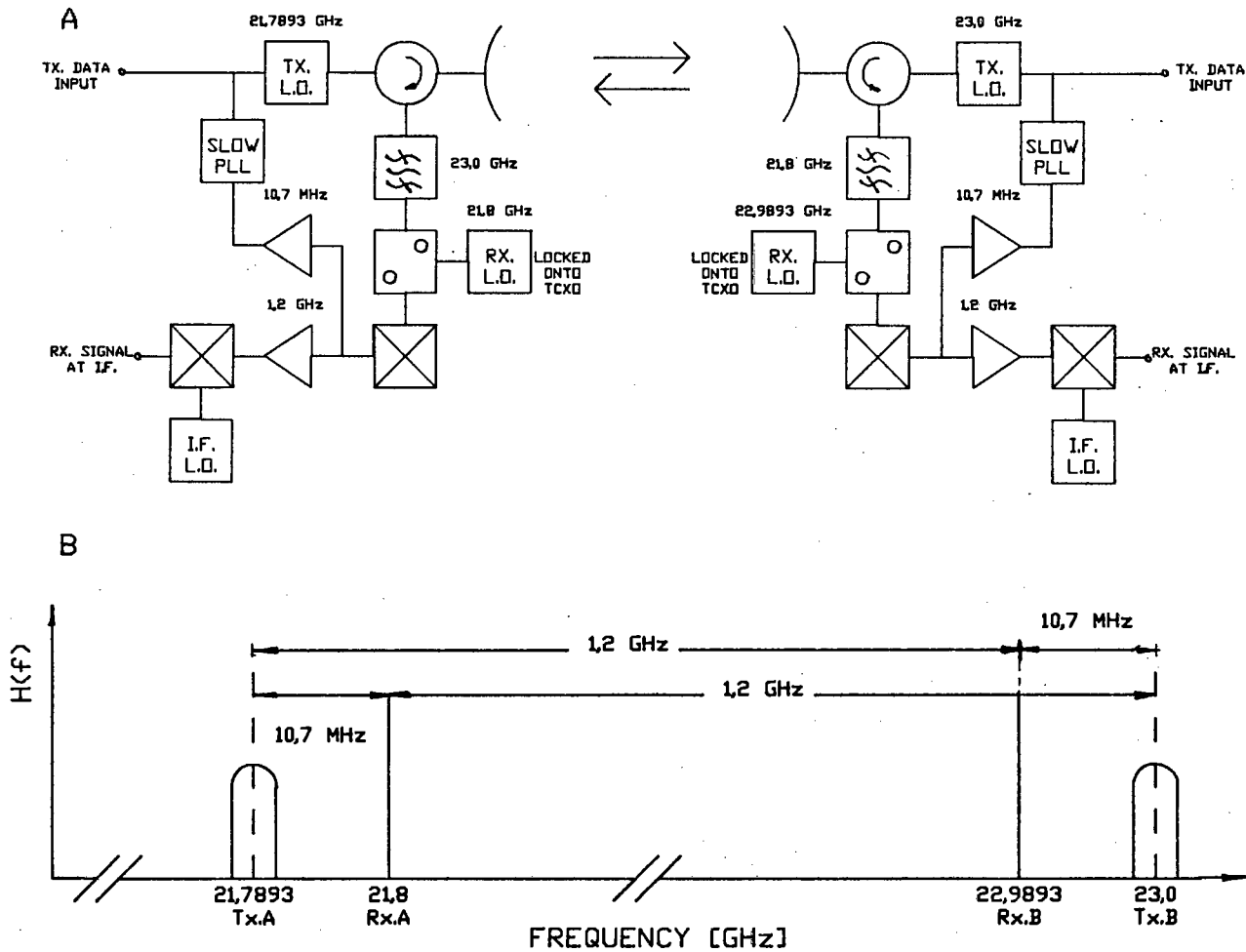


Fig. 3.2 DUPLEX BY CONTINUOUS TRANSMISSION USING DUAL R.F. SOURCES AT EACH END
(A) SCHEMATIC
(B) SPECTRUM

Duplex operation occurs here by simultaneous transmission in both directions. To achieve this, an additional R.F. local oscillator (L.O.) is required at each end purely for down-converting the received signal.

Note that inclusion of the bandpass filter at each end effectively suppresses the image spectrum. The filters

also serve to increase to approx. 60 dB. the attenuation encountered by spurious emissions in the path between the main down-conversion mixer and the antenna.

An additional advantage of this configuration is it's ability to save power if only simplex operation is required. This is done by placing the receiving-end in a "listening-only" mode where the transmit L.O. is turned-off. This is possible since it is the receive L.O. and not the transmit L.O. which is locked to a TCXO harmonic.

3.3 R.F. Transmission

3.3.0 Assumptions

Transmitter power $P_{TX} = 21,7\text{dBm}$ (150 mW)
R.F. frequency $f = 23$ GHz
Range $R = 20$ Km
Minimum SNR $(S/N)_{MIN} = 12,5$ dB (MSK for $BER < 10^{-7}$)
[2.1]
Rec. Noise Fig. $F_{REC} = 12$ dB
Noise Bandwidth $B_n = 2,5$ MHz (SAW filter)

3.3.1 Degradation Budget

For a $BER < 10^{-7}$ the theoretical SNR required for MSK is approx. 12,5 dB. For an unprotected, non-diversity practical channel however, a higher SNR is required due to various channel imperfections. A listing of the degradation budget is shown in Table 3.0. Total degradation amounts to 3,8 dB. This is added to the theoretical 12,5 dB SNR requirement, bringing the practical required SNR to 16,3 dB.

SYSTEM IMPAIRMENT	DEGRADATION
<u>1. Modem Imperfections</u>	
(a) Phase (mod. index) errors at the modulator.	0,5
(b) Intersymbol interference	0,6
(c) Carrier recovery phase noise [1.21]	0,1
(d) Jitter (incorrect sampling instants)	0,1
(e) Excess noise bandwidth of receiver	0,5
(f) Other hardware impairments (temp. variations, ageing etc.)	0,4
MODEM TOTAL	2,2
<u>2. R.F. Channel Imperfections</u>	
(a) AM/PM conversion (minimal for MSK)	0,1
(b) Band limitation, channel group delay [1.16]	0,3
(c) Adjacent R.F. channel interference	1,0
(d) Feeder and echo distortion	0,2
CHANNEL TOTAL	1,6
TOTAL DEGRADATION	3,8

[1.8]

Table 3.0 SYSTEM DEGRADATION BUDGET

3.3.2 Minimum Received Signal Level Required S_{MIN}

$$\begin{aligned}
 \text{SNR required at the receiver input} &= (S/N)_{IN} \\
 &= F_{REC} + 16,3 \text{ dB} \\
 &= 28,3 \text{ dB}
 \end{aligned}$$

$$\begin{aligned}
 \text{Receiver input noise: } N_{IN} &= kT_0 B_n \quad \dots \quad (3.1) \\
 &= -109,9 \text{ dBm.}
 \end{aligned}$$

Hence minimum input signal level at the receiver:

$$\begin{aligned} S_{MIN} &= N_{IN} + 28,3 \text{ dB} \\ &= \underline{-81,6 \text{ dBm}}. \end{aligned}$$

3.3.3 System Gain

If the transmitter and receiver are placed next to one another with no antennas attached (i.e. power received = power transmitted), then the amount by which the received power exceeds S_{MIN} is termed "System Gain G_s ".

$$\text{i.e.} \quad G_s = P_T - S_{MIN} \quad . . . (3.2)$$

$$= 21,7 \text{ dBm} - (-81,6 \text{ dBm})$$

$$G_s = \underline{103,3 \text{ dBm}}$$

3.3.4 Propagation Losses

(a) Free space propagation loss:

$$L_{FS} = 92,4 + 20 \text{ Log } d + 20 \text{ Log } f \quad [\text{dB}] \quad . . . (3.3)$$

Where: d = path length in Km

f = R.F. frequency in GHz.

Hence:

$$\begin{aligned} L_{FS} &= 92,4 + 20 \text{ Log } 20 + 20 \text{ Log } 23 \\ &= 145,7 \text{ dB} \end{aligned}$$

(b) Atmospheric attenuation due to water vapour:

$$L_{H2O} \approx 0,25 \text{ dB/Km at } 23 \text{ GHz} \quad (\text{see Fig. 3.3})$$

then $L_{H2O} \approx 5,0 \text{ dB}$ over a path of 20 Km.

Total propagation loss $L_{TOT} = L_{FS} + L_{H2O}$

$$L_{TOT} = \underline{150,7 \text{ dB}}$$

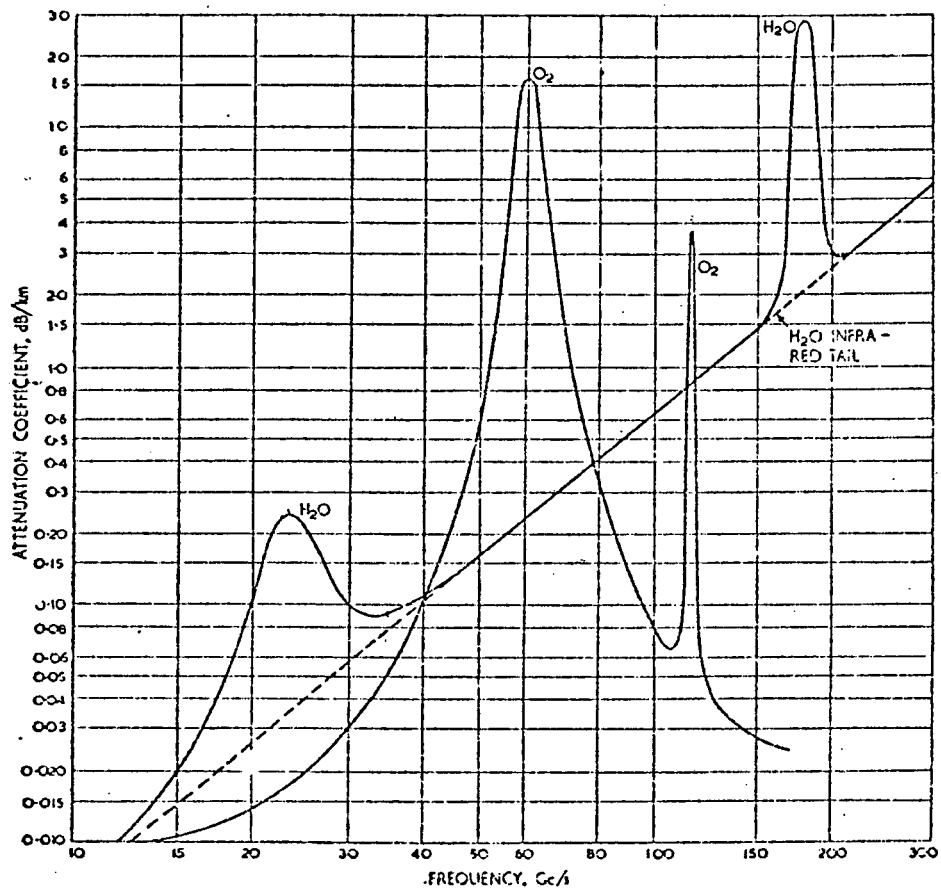


Fig. 3.3 ATMOSPHERIC ATTENUATION AT MICROWAVE FREQUENCIES

3.3.5 Fade Margin

$$FM = 30 \log d + 10 \log(6ABf) - 10 \log(1-R) - 70 \quad [\text{dB}] \quad (3.4)$$

[1.8]

Where:

(1-R) = Reliability Objective (= -40 dB for 0.01% outage)

A = Roughness factor = 4 for very smooth terrain
 = 1 for average terrain
 = 1/4 for very rough, mountainous terrain.

B = Factor to convert worst-month probability to annual probability = 1/2 for hot, humid areas
 = 1/4 for average, inland areas

= 1/8 for mountainous, very dry areas.

Taking the worst case: $AB = 2$

Then: $FM = 33,4 \text{ dB}$ (includes rainfading)

3.3.6 Antennae Gains

For the system to operate within the required specifications under worst-case conditions, it is necessary that:

$$G_B + (G_{TX} + G_{RX}) - L_{TOT} - FM \geq 0 \quad \dots (3.5)$$

Where: G_{TX} and G_{RX} are transmitter and receiver gains respectively.

$$\begin{aligned} \text{Hence: } G_{TX} + G_{RX} &\geq L_{TOT} + FM - G_B \\ &\geq 80,50 \text{ dB} \end{aligned}$$

Assuming $G_{TX} = G_{RX} = G$, then $G = 40,25 \text{ dB}$.

$$\text{Antenna gain: } G = 4\pi\eta A/\lambda^2 \quad \dots (3.6)$$

Where: A = cross-sectional antenna intercept area
 η = antenna efficiency

Assuming $\eta \approx 55\%$ then:

$$A = \lambda^2 G / (4\pi\eta) = 0,2607 \text{ m}^2$$

$$\begin{aligned} \text{Hence antenna diameter } d &= \sqrt{4A/\pi} \quad \dots (3.7) \\ &= \underline{57,6 \text{ cm}} \end{aligned}$$

The antenna size required is therefore within the 60 cm limit given in the design spec. Note that this size antenna would be necessary only for those applications where a range of approximately 20 Km is required. A quick-release mechanism for changing antennas would allow smaller antennas to be used in urban, short-range applications.

REFERENCES

- [3.1] M.C.AUSTIN, M.U.CHANG, D.F. HORWOOD, R.A. MASLOV,
"QPSK, Staggered QPSK, and MSK - A Comparative
Evaluation", IEEE Trans. on Comm., Vol.COM-31,
February 1983.

CHAPTER 4

TRANSMISSION SIMULATION

4.0 Introduction

A fairly comprehensive evaluation of the performance of various modulation schemes has been made in the literature (and summarised in Chapter 1). Why then, the need to simulate? The answer is that this specific application poses some problems to which no reference has been found in any of the past publications on the subject. It also has a unique combination of system parameters which make it unlike many systems described in these publications, making it difficult to draw relevant conclusions from the results presented.

By means of simulating the proposed MSK transmission link, information such as the following may be extracted:

- (a) The effect on BER of errors in modulation index. This problem was outlined in section 3.1.1 and a theoretical analysis was performed in Appendix A. However, the results obtained are less than adequate because:
 - (i) Only the case where the f/v varactor characteristic may be assumed locally linear was considered.
 - (ii) The analysis makes the simple assumption that once the cumulative phase error θ_c has exceeded $\pi/2$ radians, its value is reset to zero. While intuitively it seems feasible that cumulative phase error may be eroded by phase adjustments of the coherently extracted carrier, no convincing proof could be given.
- (b) MSK performance in the presence of adjacent-channel and co-channel interference represented by a CW in-band interferer 10 dB or 15 dB down in power from the desired

signal. This factor is of major importance in the urban application where many radio links may be operated within a small geographical area. Although a similar investigation has been performed by Fang [4.1], the type of system for which his results were recorded is vastly different to that proposed here. He used a system employing non-linear amplification, hard-limiting and pulse-shaping filters.

In addition, developing a working MSK modulator/demodulator for simulating data transmission gives invaluable insight into unforeseen problems in implementing an MSK scheme. It also provides a useful test-bed facility for assessing the effects of any system modifications which may later be proposed.

4.1 Simulation Strategy

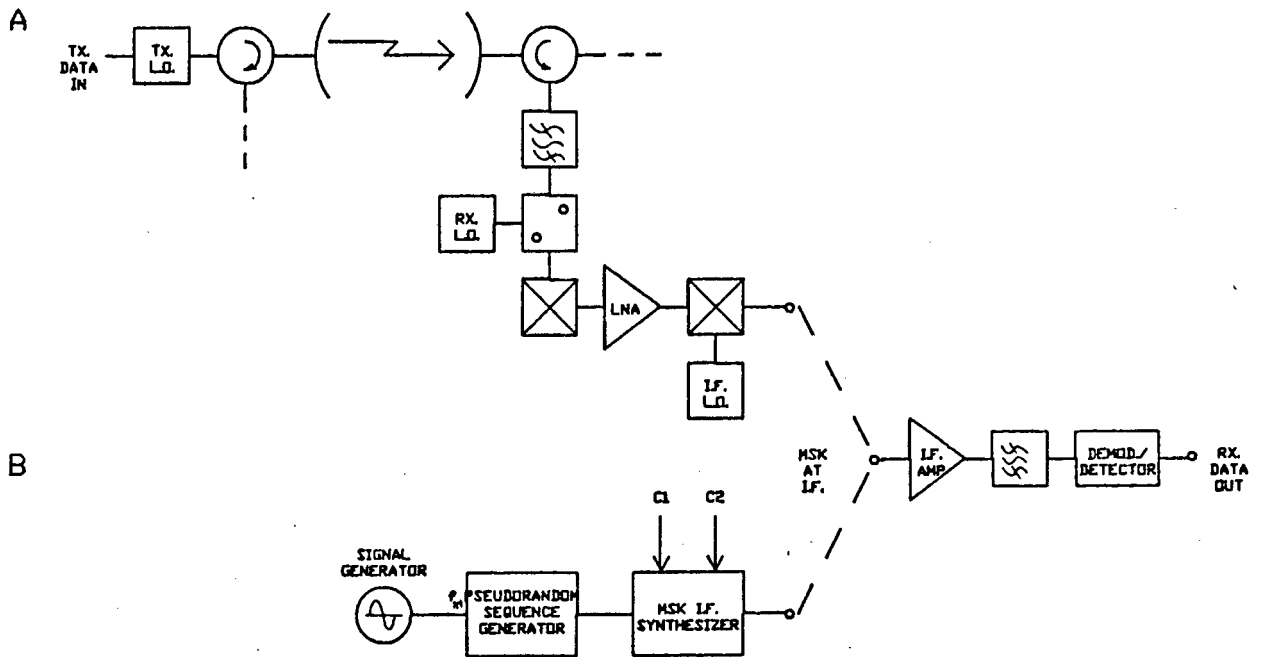


Fig. 4.0 (A) ACTUAL R.F. DATA TRANSMISSION BY MSK
 (B) SIMULATED MSK TRANSMISSION

The MSK transmitter and receiver front-end up to the main down-conversion mixer can be seen as a "black box". The data signal is applied at the input, and the corresponding MSK signal at intermediate frequency (I.F.) appears at the output. The black box can therefore be simulated simply by a module which produces the identical I.F. MSK signal at the output for a given data input. This module shall be called the "MSK I.F. Synthesizer". Demodulation and detection of the I.F. signal is performed exactly as proposed for the digital radio system.

Useful simulation tests which could be performed using the above configuration are described in detail in Chapter 7.

4.2 Modules Required

4.2.0 Pseudo-random Sequence Generator

The function of this module is to simulate the actual data to be transmitted. Although this is in fact also performed by the Data Transmission analyser (see Chapter 7), this equipment will only be available for limited periods for testing purposes. An alternative data source is therefore required. In order to produce a reasonably authentic data-signal, a bit-sequence of considerable length is required. Control of the actual bit-rate would also be an advantage for two reasons:

- (a) Experimentation with BER vs. BT_c (B =channel bandwidth) can easily be performed by using a fixed bandpass filter and simply adjusting the bit-rate (while maintaining the correct mod. index for MSK and all other operating parameters constant.)
- (b) The module could also be used for testing the feasibility of expanding to higher bit-rates, e.g. 8 MBit/s.

4.2.1 MSK I.F. Synthesizer

As will be explained later, due to a π radian phase ambiguity in the coherent carriers extracted at the receiver, differential encoding must be performed on the data signal before transmission. The MSK I.F. synthesizer serves to differentially-encode the input data and to then convert this bitstream into an MSK signal centred at the 70 MHz. I.F. The facility for independent, external control of keyed frequencies f_1 and f_2 is also required. If sufficient range of frequency variation is possible, the module may be made flexible enough to permit use at higher data-rates, e.g. 8 MBit/s.

4.2.2 I.F. Amplifier and Filter

If meaningful BER vs. E_b/N_0 measurements are to be performed during simulation tests, the amplifier used in the simulation must have a Noise Figure F whose value is precisely known.

It must also be realised that the noise figure of the I.F. amplifier and insertion loss of the I.F. filter will have little effect on the overall noise figure of the receiver in the R.F. transmission system. This is due to the gain of the Low Noise Amplifier (LNA) situated in front of the I.F. stage (see Fig. 3.2A), since total noise figure is calculated as:

$$F_{TOT} = F_1 + (F_2 - 1)/G_1 + (F_3 - 1)/G_1 \cdot G_2 + \dots \quad (4.1)$$

Where: F_i ($i=1,2,3..$) is the noise figure of the i^{th} receiver stage.

and: G_i is the gain of the i^{th} receiver stage.

During simulation tests, compensation must therefore be made for the discrepancy between actual I.F. stage noise figure and the total receiver noise figure in the real system. This may be done by making a suitable adjustment

to the noise-level added to the MSK I.F. Synthesizer signal (as described in Chapter 7).

The most important requirements of the filter are:

- (a) Minimal deviation from linear phase to avoid delay distortion. [3.1]
- (b) Lowest possible Shape Factor SF in order to ensure minimum noise bandwidth for a given channel bandwidth, where:

$$SF = \frac{40\text{dB Bandwidth}}{3\text{dB Bandwidth}} \quad . . . (4.2)$$

The system spec. requires 50 dB AGC (see Chapter 2). Since it is proposed to use logarithmic amplifiers in the actual system, they will also be used in the simulation. Information regarding MSK performance in the presence of the limiting introduced by logarithmic amplifiers can thereby be obtained.

4.2.3 Demodulator-Detector

Extraction of coherent carriers and their subsequent processing to produce a quadrature-channel matched-filter receiver structure is performed exactly as proposed for the MSK radio transmission system. (See Appendix A for a description of the principles of MSK demodulation).

The chosen scheme (shown in Fig. 4.1) for generating I- and Q-channel carrier signals avoids $n\pi/2$ radian ($n=1,2..$) phase-ambiguity. Although a phase ambiguity of $n\pi$ radians remains due to the frequency/2 operation performed, this can be satisfactorily dealt with by differentially-encoding the input data signal. The corresponding decoding process is then performed at the receiver.

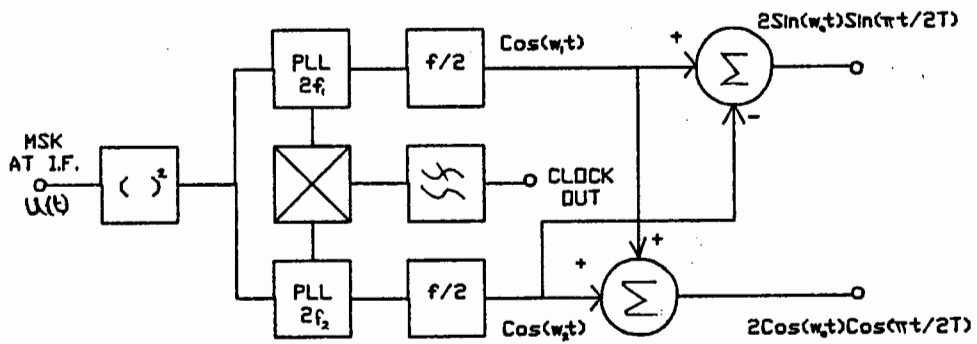


Fig. 4.1 GENERATION OF I- AND Q-CHANNEL PHASE REFERENCES

Detection filters perform the convolution integrals, then decisions on symbol-states are made by clocked threshold detectors. Finally, channel differential decoders and a bit-interleaving network reconstruct the differentially encoded 2 Mbit/s bitstream. A final differential decoder produces the original input bitstream.

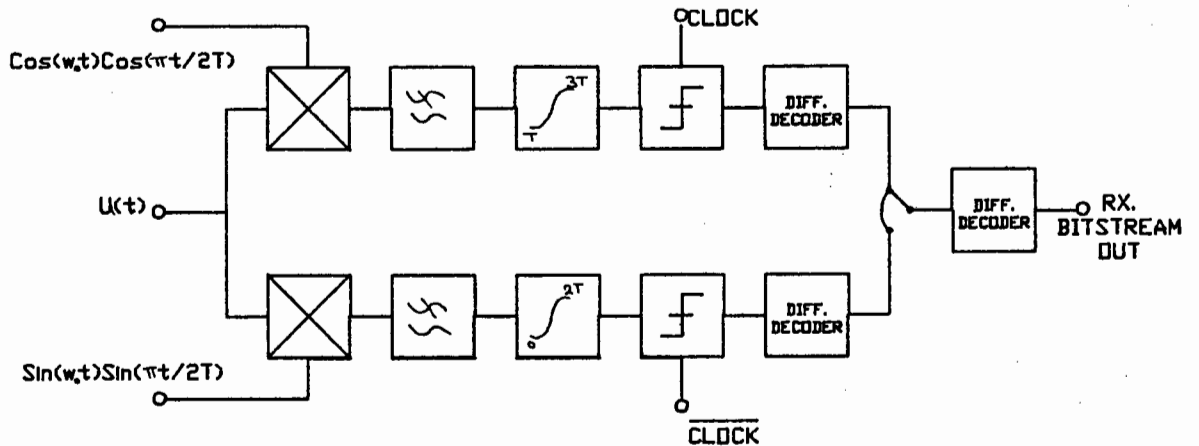


Fig. 4.2 MSK DEMODULATION-DETECTION

REFERENCES

- [4.1] R.J.FANG, "Quaternary Transmission Over Satellite Channels with Cascaded Nonlinear Elements and Adjacent Channel Interference", IEEE Trans. on Comm. Vol.COM-29, May 1981.

CHAPTER 5

DEVELOPING TRANSMITTER SIMULATION MODULES

5.1 Pseudo-random Sequence Generator



Fig. 5.0 P.R.S. GENERATOR SCHEMATIC

The data-rate of the NRZ bitstream produced is controlled by the frequency of the sinusoid applied at the input. Allowance for a weak input signal - say, $P_{i,} \geq -30$ dBm should be made. Module input and data output are terminated into 50Ω .

5.1.1 Line Receiver

FUNCTIONS: Convert the input signal ($P_{i,} \geq -30$ dBm) into a TTL clock signal.

Use hysteresis to avoid multiple switching at zero-crossing instants.

CIRCUIT:

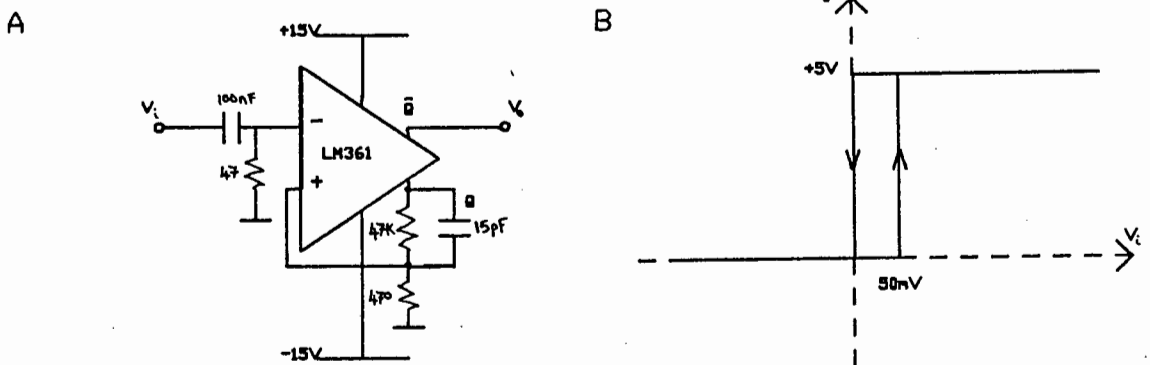


Fig. 5.1 (A) LINE RECEIVER CIRCUIT
(B) TRANSFER CHARACTERISTIC

NOTES: The LM361 high-speed differential comparator used has a response time of 14 ns (see Appendix B for device data-sheets), permitting good performance at frequencies in excess of 8 MHz. The 15 pF capacitor in the feedback circuit assists in speeding-up the response.

5.1.2 Feedback Shift Register (F.S.R.)

With limited amounts of hardware feedback shift registers may be constructed which yield long sequences of 1's and 0's before the sequences repeat in a deterministic manner.

Sequences which are of maximum length, ($2^n - 1$ bits long for an n -stage f.s.r.) are called m -sequences. The choice of pick-off points for the feedback connection determines whether or not a sequence will be of maximal length. One pick-off point must be at the final stage of the register. A position short of the final stage would result in no contribution to the feedback process from the content of stages after the pick-off.

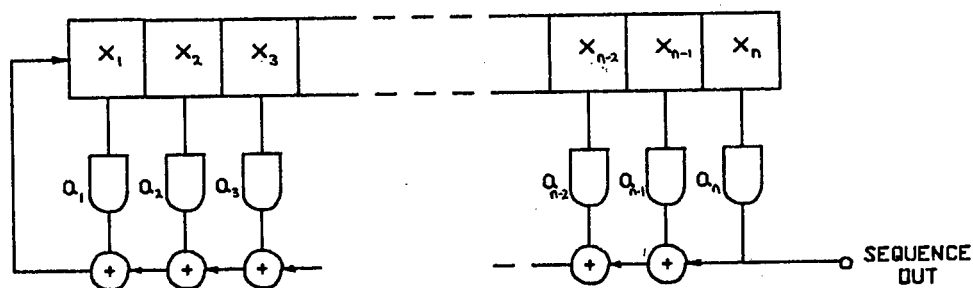


Fig. 5.2 A GENERALISED F.S.R.

Fig. 5.2 shows the general form of an f.s.r. with linear feedback comprising modulo-two additions. Each stage x_i is connected through a scalar multiplier a_i to the summing network. If $a_i = 1$ this represents a closed connection and x_i is included in the feedback path. If $a_i = 0$, then x_i is

omitted. Thus if x^1 represents the new contents of a stage, then:

$$\begin{aligned}
 x_1^1 &= a_1 x_1 + a_2 x_2 + a_3 x_3 + \dots + a_n x_n \\
 x_2^1 &= x_1 \\
 x_3^1 &= x_2 \\
 &\cdot \\
 &\cdot \\
 &\cdot \\
 x_{n-1}^1 &= x_{n-2} \\
 x_n^1 &= x_{n-1}
 \end{aligned}$$

(Where + represents modulo-2 addition.)

Reversing the order used previously, these simultaneous equations may be written in matrix form as:

$$\begin{bmatrix} x_n^1 \\ x_{n-1}^1 \\ \cdot \\ \cdot \\ x_3^1 \\ x_2^1 \\ x_1^1 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & \cdot & \cdot & \cdot & 0 \\ 0 & 0 & 1 & 0 & \cdot & \cdot & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & \cdot & \cdot & \cdot & 0 & 1 & 0 \\ 0 & 0 & \cdot & \cdot & \cdot & 0 & 0 & 1 \\ a_n & a_{n-1} & \cdot & a_3 & a_2 & a_1 & \cdot & \cdot \end{bmatrix} \cdot \begin{bmatrix} x_n \\ x_{n-1} \\ \cdot \\ \cdot \\ x_3 \\ x_2 \\ x_1 \end{bmatrix}$$

or

$$x^1 = T \cdot X \quad \dots \quad (5.1)$$

[5.1]

Where T is a transition matrix which changes a current state X of the register into the next state X^1 . Application of the transition matrix T repeatedly will take the register through a succession of states, namely:

$$X, TX, T(TX) \dots$$

i.e. $X, TX, T^2 X, T^3 X \dots$ etc.

For a register with n stages there is a maximum possible set of states, namely 2^n . The sequence of states must therefore be periodic, implying that some integer K exists, with $1 \leq K \leq 2^n$ for which:

$$T^K X = X \quad \dots \quad (5.2)$$

[5.1]

The smallest value of K to satisfy the relation is then the period of the sequence.

The state $X=0$ cannot proceed to any other non-zero state. A sequence of period one follows a starting state of $X=0$. The remaining 2^n-1 states may form one (m-sequence) or more sequence with periods between 1 and 2^n-1 (m-sequence).

A square matrix has a characteristic polynomial $Q(s)$ defined as:

$$Q(s) = |T-sI| \quad \dots \quad (5.3)$$

where I is the unit matrix. In general, an n -stage f.s.r. is described by an $n \times n$ transition matrix which yields a characteristic polynomial of degree n . Polynomials which relate to f.s.r.'s yielding m-sequences are of particular interest. Such polynomials are always irreducible, however not all irreducible polynomials provide m-sequences. [5.1]

An irreducible polynomial providing an m-sequence for a 24-stage f.s.r. is:

$$Q(s) = s^{24} + s^7 + s^2 + s + 1 \quad \dots \quad (5.4)$$

[5.2]

To establish the feedback connections for an n -stage register corresponding to a given polynomial, take each term s^k and write a term x_{n-k} in the feedback equation. Repeat for all $k < n$, interpreting 1 as s^0 . The feedback equation for a 24-stage register is then:

$$x_1' = x_{17} + x_{22} + x_{23} + x_{24} \quad \dots \quad (5.5)$$

(Where + represents mod-2 addition)

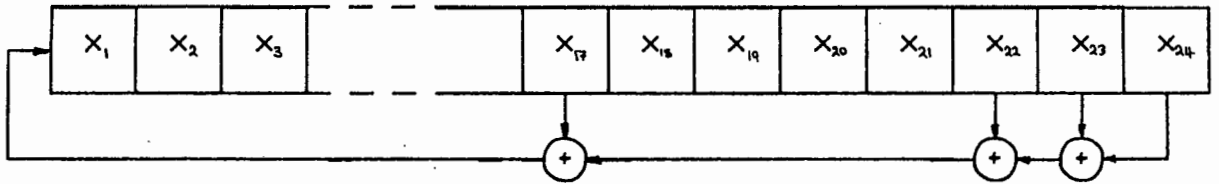


Fig. 5.3 24-STAGE F.S.R. FEEDBACK CONNECTIONS

This f.s.r. exhibits a bit-sequence of length:

$$2^{24} - 1 = 16\,777\,215$$

When clocked to produce a bit-rate of 2,048 MBit/s, the sequence repeats after 8,19 seconds.

Note that it is essential to ensure that the f.s.r. never enters the all-0's state on power-up, since the state $X=0$ cannot proceed to any other non-zero state. To avoid this, a HI pulse of duration approx. 1ms is modulo-2 added to the feedback signal immediately after power-up.

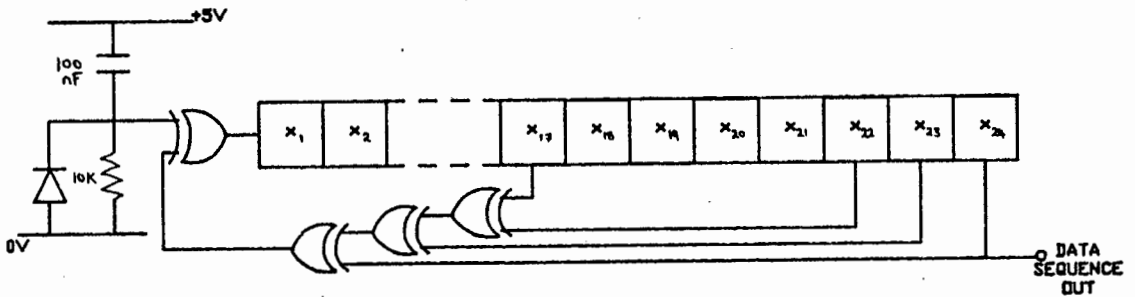


Fig. 5.4 COMPLETE F.S.R.

The function of the diode in the monostable circuit is to ensure rapid capacitor discharge and hence monostable operation even for momentary power rail intermittances.

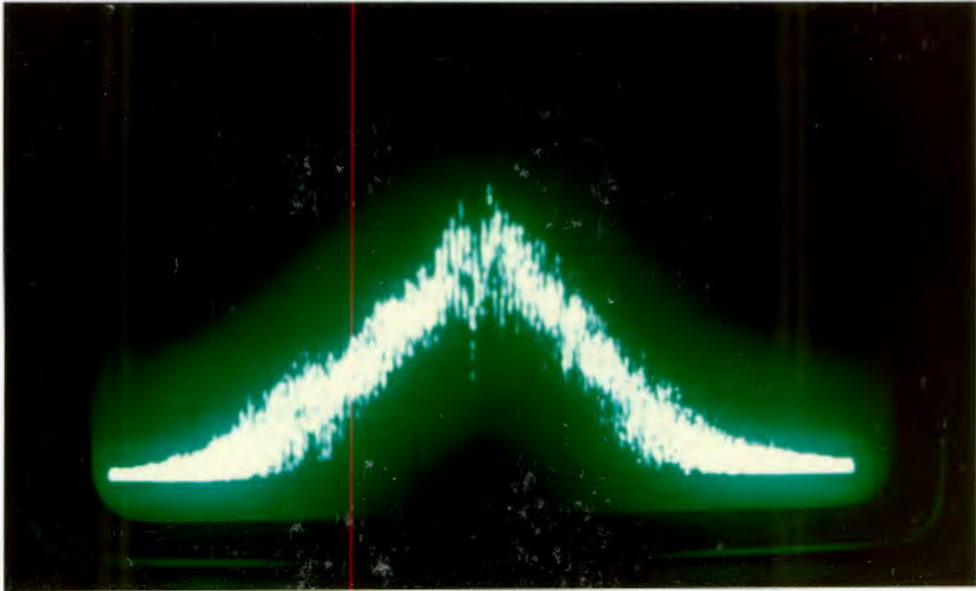


Fig. 5.5 SPECTRUM ANALYSER DISPLAY OF PSEUDORANDOM DATA SIGNAL (20 MHz/Division setting).

Note that the reduced level of the first spectral lobe is due to the low-frequency response of the spectrum analyser.

5.2 MSK I.F. Synthesizer

As shown in Fig. 5.6, the functions performed within this module permit it's subdivision into 5 sub-modules:

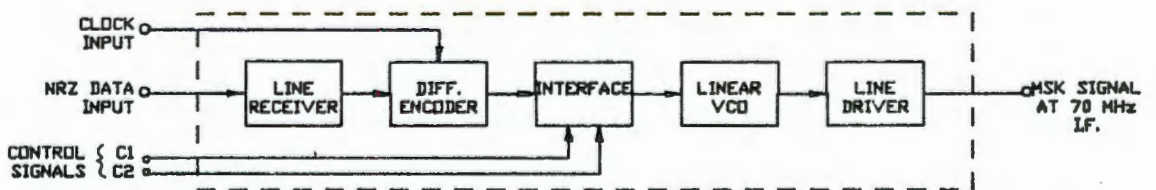


Fig. 5.6 MSK I.F. SYNTHESIZER SCHEMATIC

A brief description of each sub-module will be given, followed by a look at the unit as a whole and an appraisal of its performance.

5.2.1 Line Receiver

This is identical to that described in Section 5.1.1.

5.2.2 Differential Encoder

FUNCTION: This can best be described by means of a truth table and schematic:

$b_i((n-1)T)$	$b_i(nT)$	$b_o(nT)$
0	0	0
0	1	1
1	0	1
1	1	0

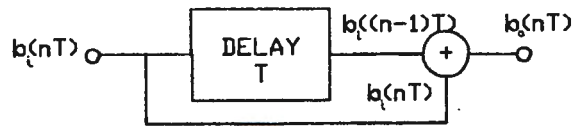


Fig. 5.7 DEFINING THE DIFFERENTIAL-ENCODER FUNCTION

CIRCUIT: Since flexibility is required in terms of the data transmission rate, control of the delay duration is necessary to ensure that it is always equal to the bit-duration T . This is most easily achieved by means of a clocked shift-register:

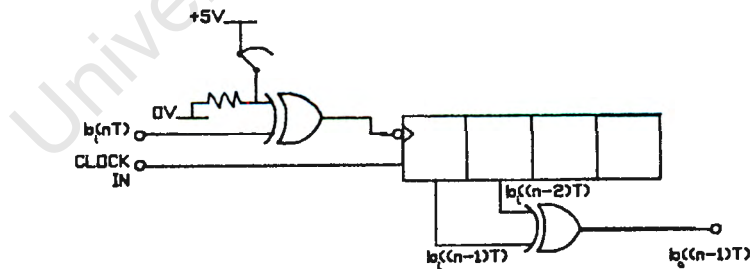


Fig. 5.8 DIFFERENTIAL-ENCODER CIRCUIT

To avoid the possibility of a "race" condition where the shift-register is clocked at the same instant as a bit transition occurs at the input,

5.2.3 Voltage Controlled Oscillator (VCO)

FUNCTION: Produce a 0 dBm sinusoidal output whose frequency varies linearly from 68 MHz to 72 MHz on variation of a control voltage input in the range 0 to +15V. Data signals of rates up to 8Mbit/s on the control input should also not result in > 10% amplitude modulation of the output signal.

CIRCUIT:

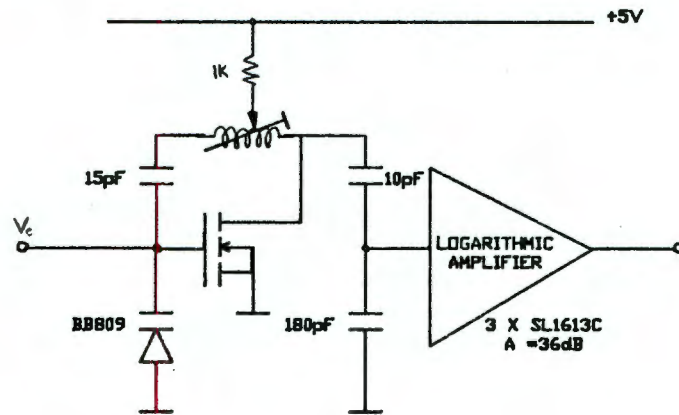


Fig. 5.9 VCO CIRCUIT

As shown in Fig. 5.10, the VCO frequency/voltage characteristic is extremely linear over the range 68-72 MHz. In that range, linear correlation coefficient $r = 0,9997$. Where r is defined as:

$$r = \frac{\{N\sum xy - \sum x \sum y\}}{\sqrt{(D_x D_y)}} \dots (5.6)$$

$$\text{Where: } D_x = N\sum x^2 - (\sum x)^2$$

$$D_y = N\sum y^2 - (\sum y)^2$$

x, y are co-ordinates of points

N is the number of points used .

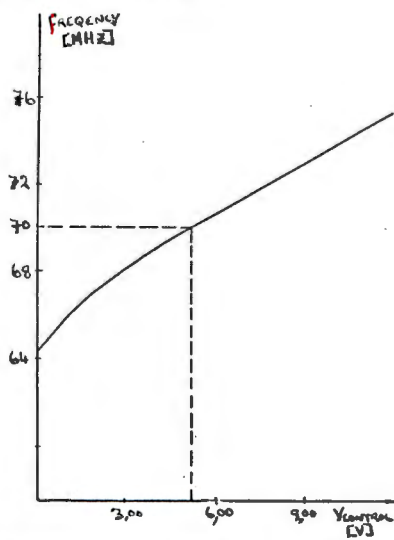


Fig. 5.10 VCO TRANSFER CHARACTERISTIC

5.2.4 Differential Encoder-VCO Interface

FUNCTIONS: To convert the TTL data signal (Fig. 5.11 A) from the differential-encoder into a signal suitable for driving the VCO (Fig. 5.11 B). V_{c1} and V_{c2} should be externally, independently variable.

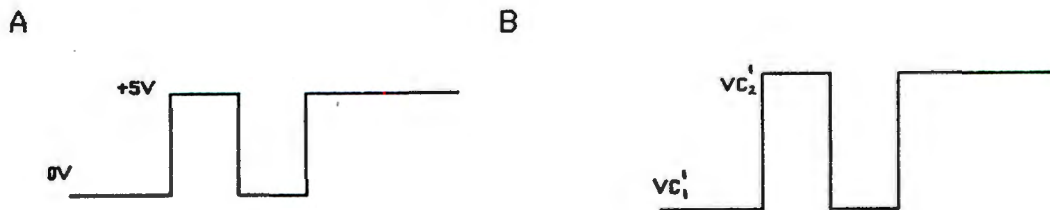


Fig. 5.11 DATA SIGNALS

CIRCUIT: Applying a high frequency (up to 8 MBit/s) signal to the control input of the VCO is difficult due to the low-pass filter effect of Z_{source} and C_{tot} .

Also, the varactor reactance at resonance:

$$X_{c2} |_{f=70\text{MHz}} \approx 56\Omega$$

Solution: make Z_{source} mostly inductive to take advantage of the decade (approx.) frequency difference between the control signal and the oscillator signal. A small amount of series resistance is also included for damping the series resonant circuit produced.

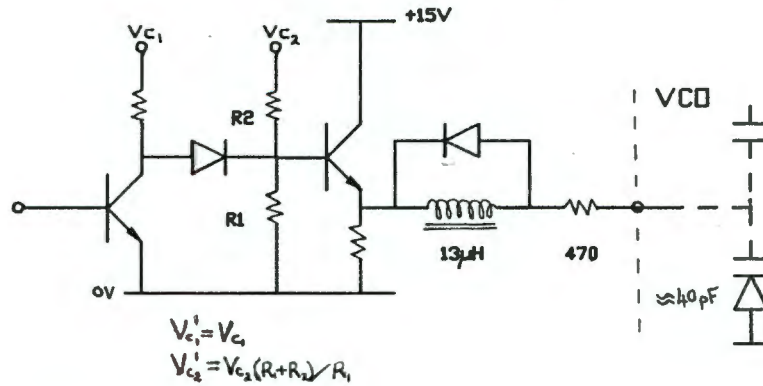


Fig. 5.12 INTERFACE CIRCUIT

Figure 5.13 shows an oscilloscope display for the signal applied to the VCO varactor diode (2MBit/s).

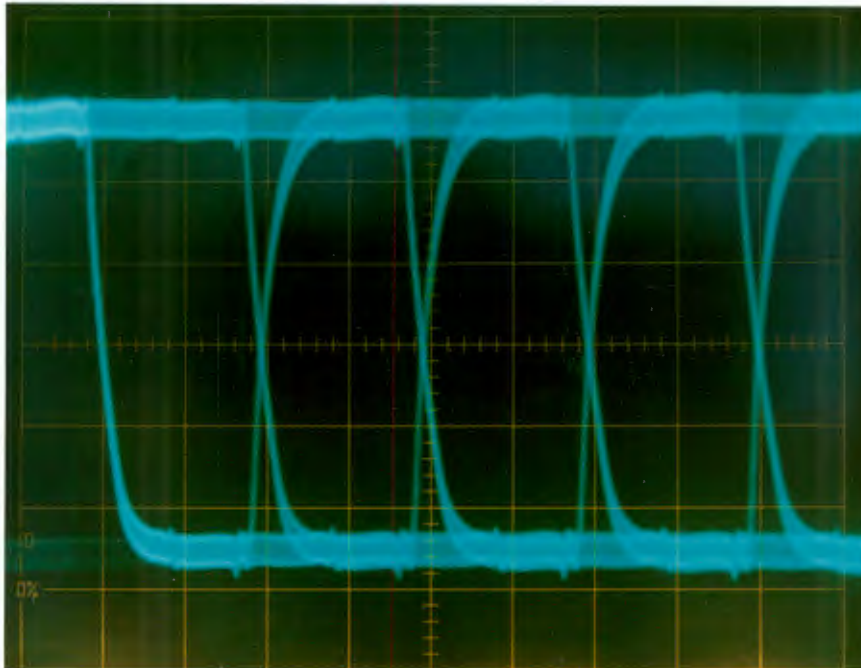


Fig. 5.13 VCO CONTROL SIGNAL

The MSK I.F. spectrum produced for a 2MBit/s datastream as seen on a spectrum analyser display is shown in Fig. 5.14.

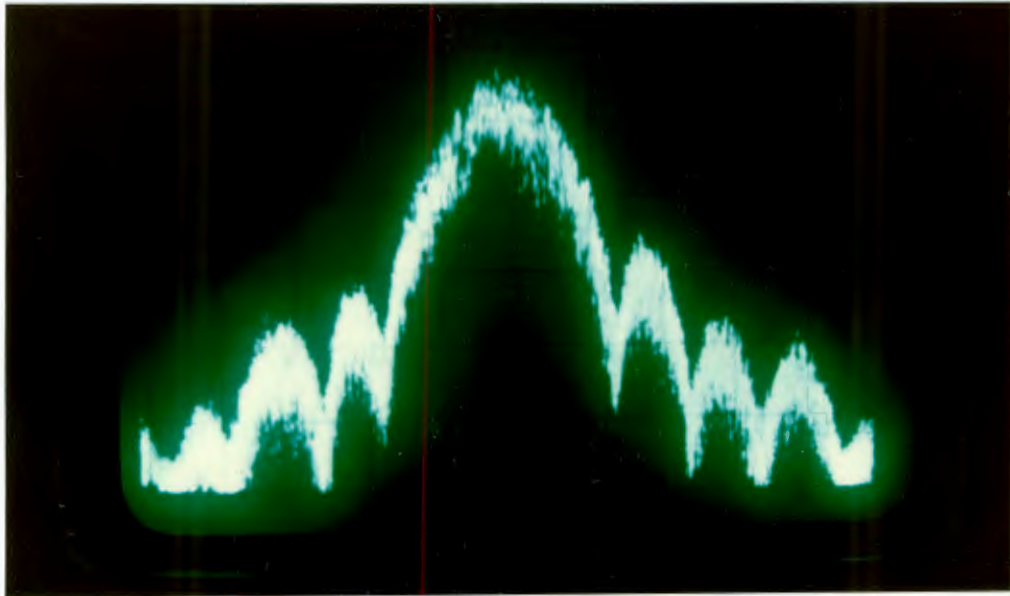


Fig. 5.14 MSK I.F. SPECTRUM

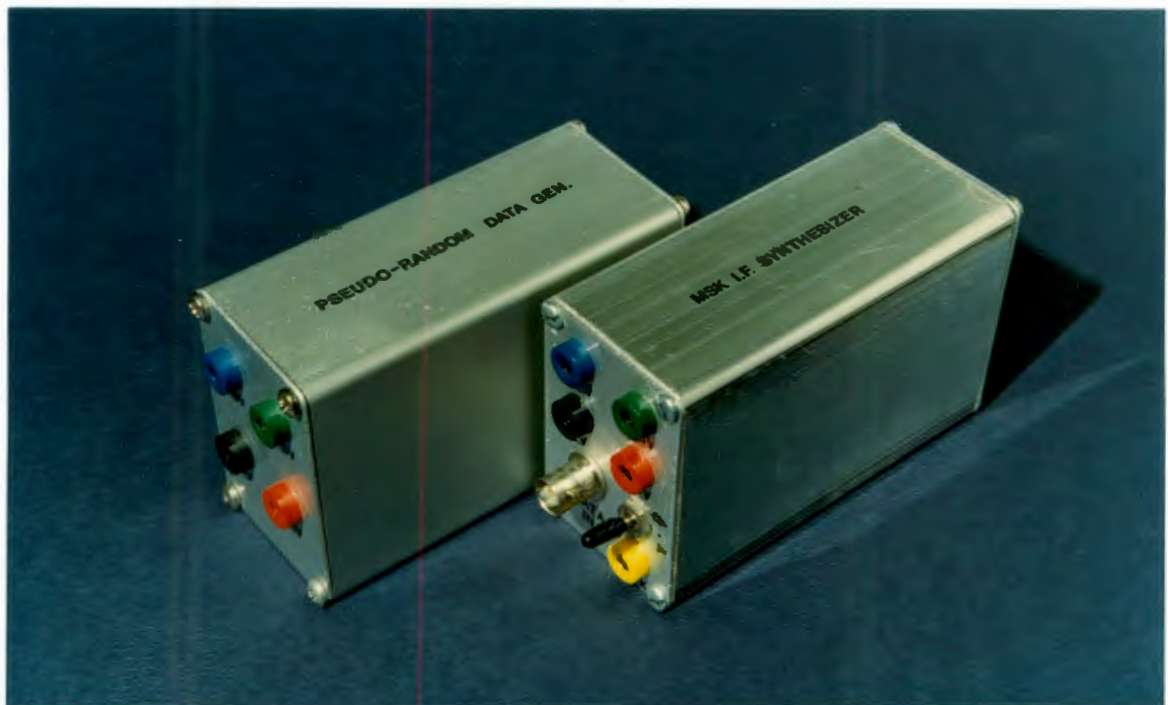


Fig. 5.15 TRANSMITTER SIMULATION MODULES

REFERENCES

- [5.1] M.G.HARTLEY, "Digital Simulation Methods",
Institution of Electrical Engineers, 1975.
- [5.2] R.CHURCH, "Tables of Irreducible Polynomials for the
First Four Prime Moduli", 'Ann. Math.,36.

DEVELOPING RECEIVER MODULES

6.0 Introduction

At the receiver, the I.F. MSK signal is first amplified to a level which is constant and suitable for signal processing. It is also passed through a band-pass filter to exclude excess noise and interference. The band-pass filtered information signal is fed to a synchronisation structure where the carrier and clock references are reconstructed, as well as to a two-channel Bayes detector (see Fig. 6.0). Cruz and Simpson [6.1] have found that probability of error is greatly affected by the characteristics of the synchronisation structure. Attention will therefore be given to optimising this structure before dealing with the detector module.

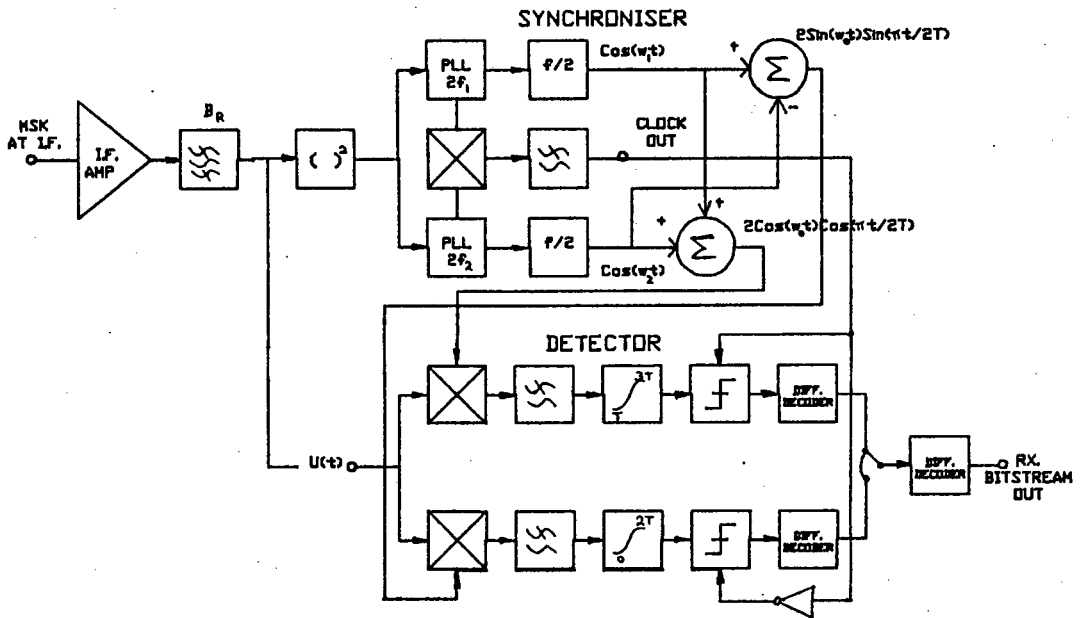


Fig. 6.0 MSK RECEIVER SCHEMATIC

6.1 I.F. Amplifier and Filter

6.1.1 Amplifier Requirements

Input Sensitivity:	$S_{i_n}(\text{min}) \approx -85 \text{ dBm}$.
Dynamic Range:	50 dB (i.e. $S_{i_n}(\text{max}) \approx -35 \text{ dBm}$.)
Output Signal-level:	0 dBm.
Noise Figure:	Constant and precisely known.
Delay Distortion:	Deviation from linear phase $< 2^\circ$ over the range 68 MHz to 72 MHz.

Total Noise Figure F of a multi-stage amplifier is given by Equation 4.1. Considering that logarithmic amplifiers are to be used (gain of these stages varies with varying signal-level), it is clear that total noise figure will not be constant but be a function of the input signal-level. If however, a high-gain linear amplifier is placed at the front-end, the contributions of later stages to overall noise figure are proportionally reduced. The variations in noise figure described could therefore be reduced to an insignificant level, provided the front-end stage has sufficient gain.

6.1.2 Filter Requirements

Bandwidth:	2,5 MHz centred at 70 MHz.
Delay Distortion:	Deviation from linear phase $< 2^\circ$ (Group delay $< 15 \text{ nS}$.)
Max. Pass-band atten.: (Insertion Loss)	As small as possible, but can be compensated-for by extra amp. gain
Min. Stop-band atten.:	40 dB
Shape-Factor (Eqn. 4.2):	$\leq 2,0$

The stringent delay distortion requirement makes a discrete-element LC-filter realisation extremely difficult. The bandwidth is too wide to use a ceramic modular filter. Helical filters at 70 MHz are physically large, although the filter could perhaps be included at the 1,2 GHz stage. Helical filters in general also have a shape-factor $\gg 2$. The most suitable option appears to be a

Surface Acoustic Wave (SAW) filter, a typical response of which is illustrated in Fig. 6.1.

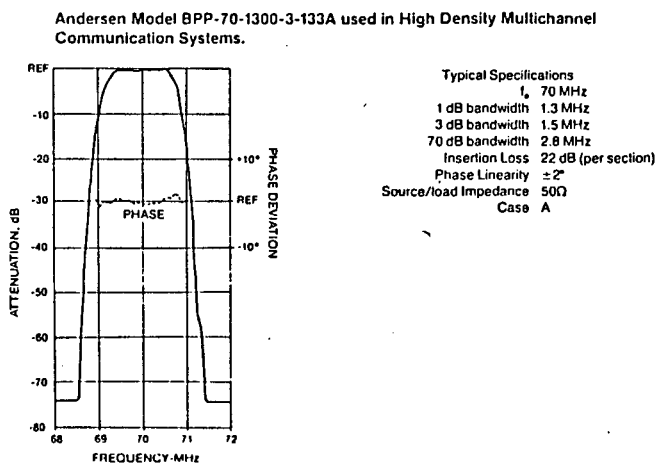


Fig. 6.1 TYPICAL SAW FILTER FREQUENCY RESPONSE

The major disadvantage of SAW filters is the large insertion loss $L_{ins} \approx 25$ dB. This can however be compensated-for by increasing amplifier gain.

6.1.3 Amplifier/Filter Stage Configuration

Selecting the best amplifier/filter stage configuration can be accomplished most easily by means of a signal-level vs. stage chart:

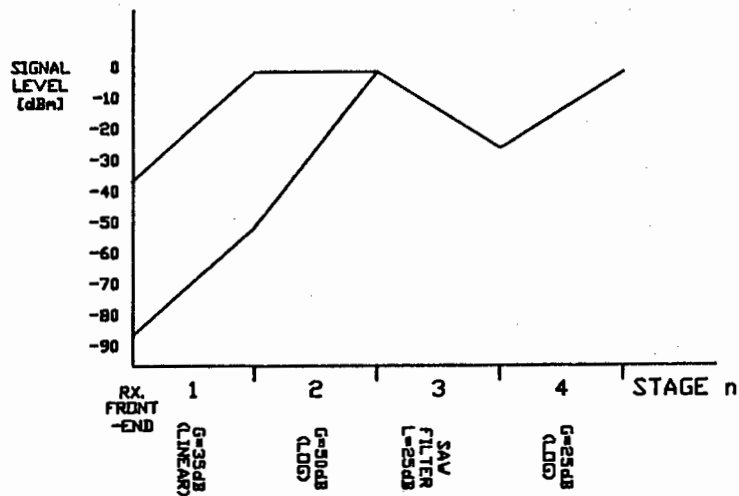


Fig. 6.2 AMP./FILTER SIGNAL-LEVEL vs. STAGE CHART

Note that the chart traces-out the signal levels at stage outputs for the two cases: $S_{i,n} = S_{i,n}(\min)$
and: $S_{i,n} = S_{i,n}(\max)$

How are the most important configuration design criteria identified on the above chart?

- Curves must meet at or before the final stage output to ensure a constant level output for maximum variation of the input signal level.
- Neither curve may exceed +10dBm at the output of stage 2, since this would exceed the SAW filter input limitations.
- An essential characteristic is the steep positive slope at the first stage- i.e. high gain at the front-end to limit the contribution of later stages to the total noise figure.

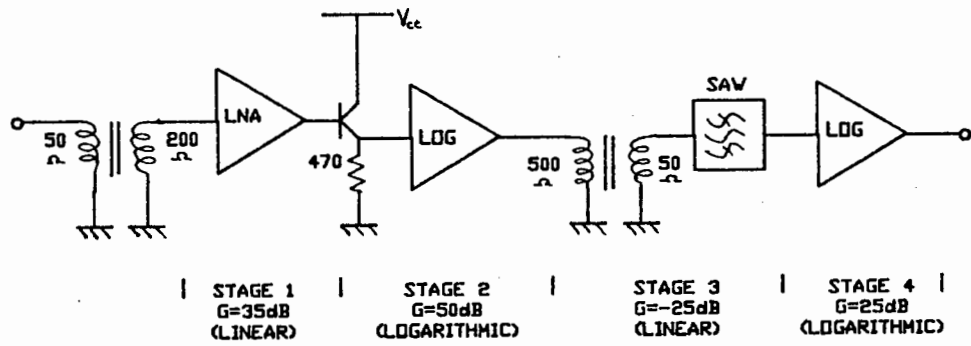


Fig. 6.3 AMPLIFIER/FILTER CONFIGURATION

Fig. 6.3 illustrates the amplifier stage configuration corresponding to the chart in Fig. 6.2.

6.1.4 Amplifier Stage Modules

6.1.4.1 Low Noise Amplifier (LNA)

The circuit (illustrated in Fig. 6.4) exhibits a wide dynamic range capability (>50 dB), a noise figure $F \approx 2,0\text{dB}$ (for $R_{\text{source}} \approx 200\Omega$) and bandwidth $\approx 150\text{ MHz}$. It consists of 2 stages of SL560C R.F. Amplifier (see Appendix B for device data-sheets), the first stage giving 20 dB gain and the second 15 dB.

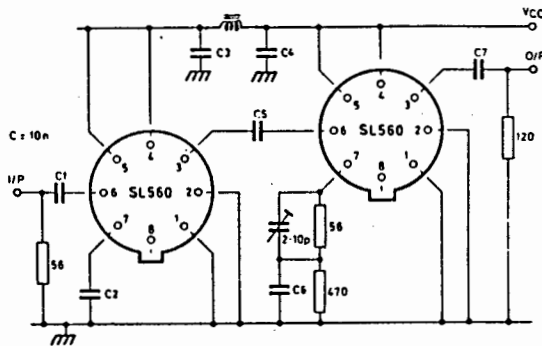


Fig. 6.4 LNA CIRCUIT

6.1.4.2 Logarithmic Amplifiers

The SL1613C Wideband Log I.F. Strip Amplifier (see Appendix B for device data-sheets) provides a suitable

building-block for meeting our log. amp. requirements. The devices are suitable for direct-coupling which minimises the total component-count, since they can be simply cascaded. Each log-stage exhibits 12,5 dB gain at 70 MHz and a noise figure of 4,5 dB.

Amplifier stage no. 2 (see Fig. 6.3) then consists of four SL1613C cascaded log stages, While amp. stage no. 4 comprises 2 cascaded log stages

6.1.5 Amplifier Performance

The noise figure of the complete I.F. amplifier and filter configuration can now be calculated (using Equation 4.1) for the full variation of input signal level.

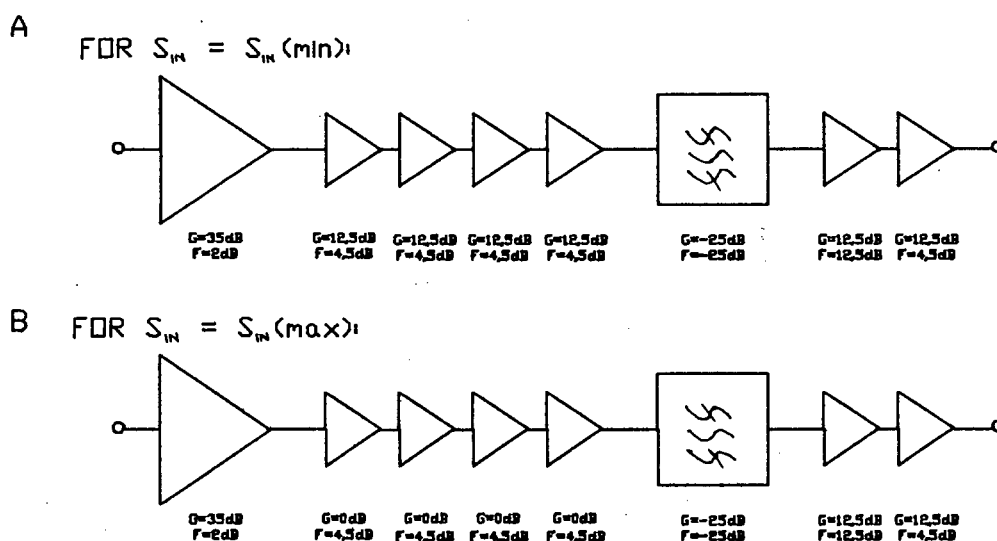


Fig. 6.5 CALCULATING TOTAL NOISE FIGURE: (A) $S_{in} = S_{in}(min)$
 (B) $S_{in} = S_{in}(max)$

For $S_{in} = S_{in}(min)$: $F_{TOT} = 2,0017$ dB.
 while for $S_{in} = S_{in}(max)$: $F_{TOT} = 2,7391$ dB.

It will therefore be necessary to make an adjustment of $\approx 0,7$ dB to the noise added to the information signal for BER vs. E_b/N_0 tests when the signal level is attenuated to

-85 dBm. This will ensure a constant E_b/N_0 at the demodulator input.

The following amplifier performance results were obtained using the H.P. 8410C Network Analyser. The tests were performed under control of an H.P. 85 microcomputer using an accuracy enhancement package. The filter and final log. amp. stage were omitted for this test. Total gain is shown as $G_v \approx 66$ dB since the sweep oscillator output signal level was set at -66 dBm. The last 2 SL1613C's in the logarithmic amplifier were therefore limiting.

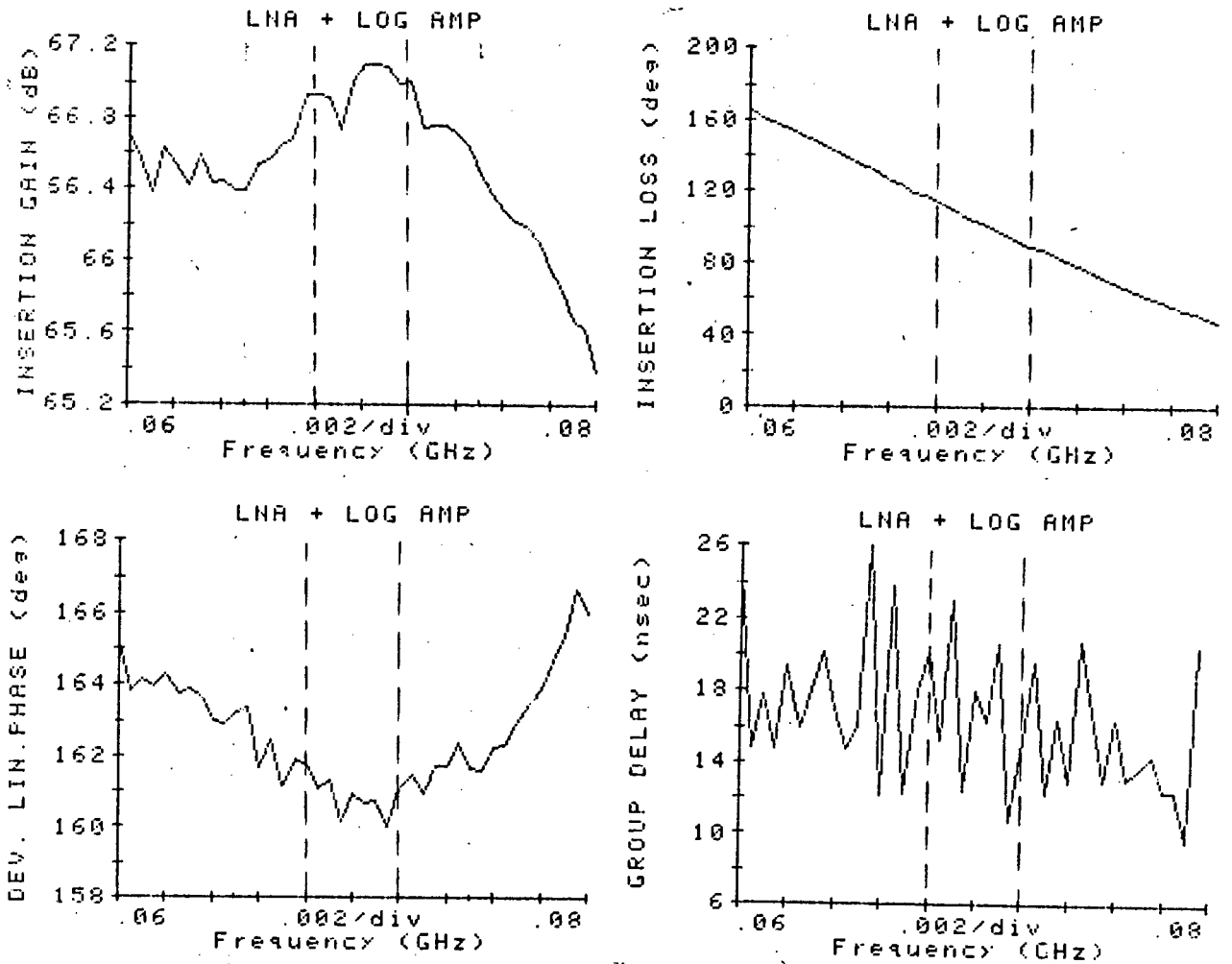


Fig. 6.6 AMPLIFIER PERFORMANCE TESTS RESULTS

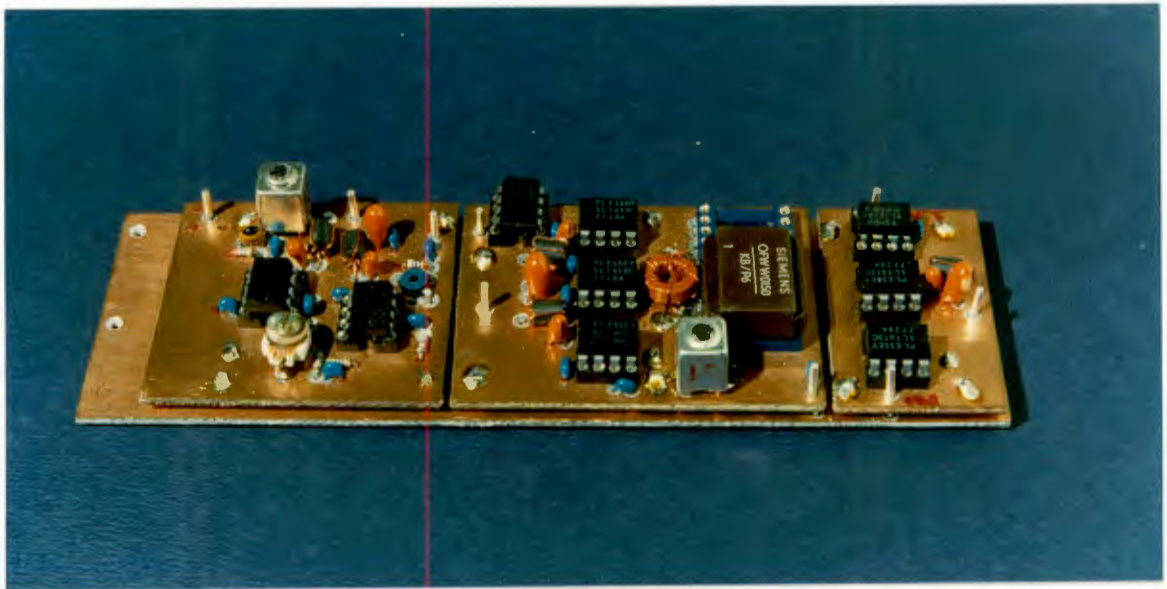


Fig. 6.7 I.F. AMPLIFIER AND FILTER

6.2 Carrier and Clock Synchronisation

As is apparent from the MSK spectrum illustrated in Fig.'s 1.18 and 5.14, the direct extraction of coherent carriers from an MSK signal is virtually impossible. This is due to the power-efficient nature of MSK in transmitting only negligible carrier power, unlike FSK with large deviation-ratio (see Fig. 1.8). This problem is solved by passing the MSK signal through a frequency-doubler, purely for the purpose of extracting phase-coherent carriers. This results in a change in modulation format from MSK to FSK ($h=1,0$), since carrier frequency-spacing has doubled while data-rate has remained the same. These double-frequency carriers may now be extracted by means of phase-lock-loops, and the frequency subsequently halved.

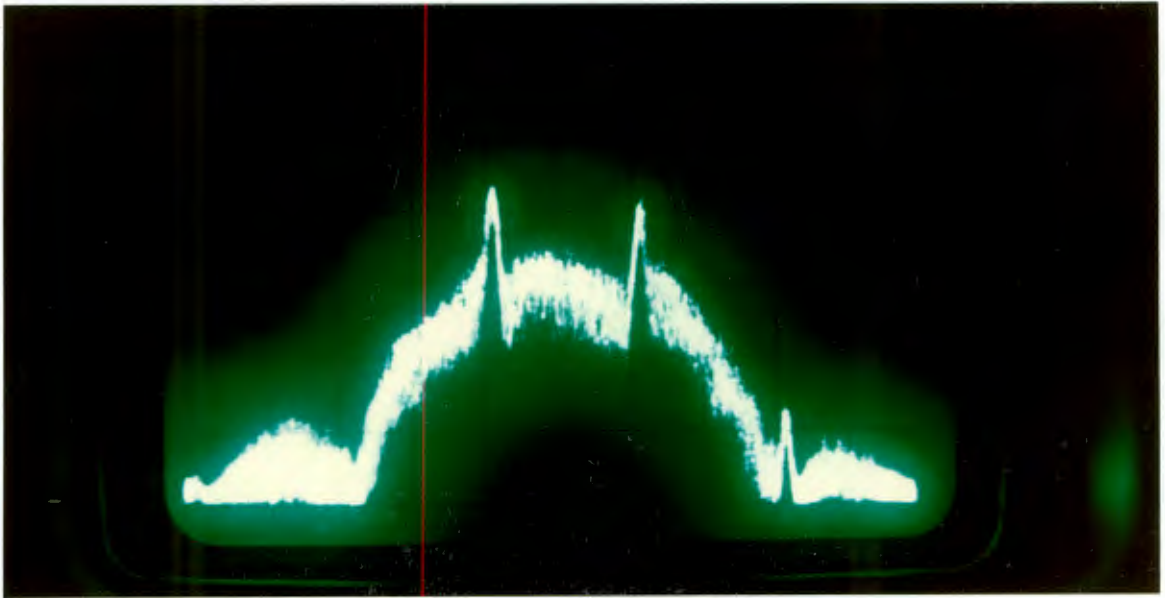


Fig. 6.8 FREQUENCY SPECTRUM OF FSK(h=1,0) SIGNAL PRODUCED BY PASSING THE MSK SIGNAL THROUGH A FREQUENCY-DOUBLER

6.2.1 Phase-Lock-Loop Design Criteria

The synchronisation performance parameter δ is defined as:

$$\delta = 1/B_L T(1+N_0 B_R T/2E_b) \quad \dots \quad (6.1)$$

[6.1]

where: $B_L \equiv$ Two-sided Phase-lock-loop (PLL) bandwidth

$B_R \equiv$ Band-pass filter bandwidth (assumed large enough to pass the signal component without distortion).

$T \equiv$ Bit period

Using Equation 1.15 this can be simplified to:

$$\delta = 1/B_L T(1+N/2S) \quad \dots \quad (6.2)$$

where: $S/N \equiv$ Signal-to-Noise ratio (SNR) at the bandpass filter output.

and: assuming noise bandwidth $B_n \approx B_R$

In Fig. 6.9 the average probability of error vs. SNR is plotted for different values of δ with $BT=\infty$. ($B \equiv$ Channel bandwidth).

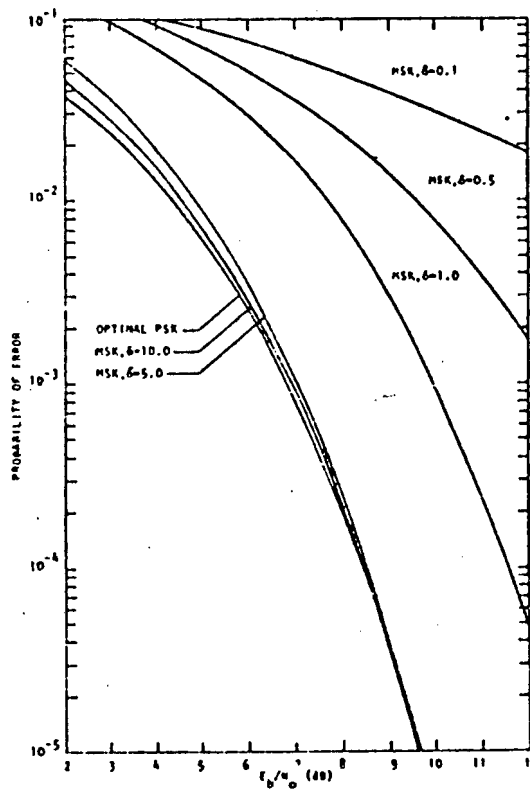


Fig. 6.9 PROBABILITY OF ERROR FOR MSK

[6.1]

It can be seen that for $\delta > 5$, the references are virtually perfect. However, for values of $\delta < 5$, the performance of the MSK system is severely degraded. (Note that the above curves are the results of an analysis where a first order loop was assumed. However, they are a good approximation for the case of a second order loop where loop SNR is sufficiently large. [6.1])

Design of the synchronisation structure should therefore aim at ensuring that δ is large. This would imply minimising loop bandwidth B_L and channel bandwidth B_R . But it has been assumed that B_R is large enough to pass the MSK signal without distortion. Our strategy should therefore be to consider Equation 6.2 instead of 6.1,

substituting $S/N = 12,5$ dB which is the minimum required for a $BER \leq 10^{-7}$ for MSK. This effectively leaves only B_L under our control in designing the synchronisation structure to maximise the parameter δ .

The question that now arises is whether a minimum limit exists for loop bandwidth due to carrier drift. For this case where variations occur in carrier frequency, two loop performance parameters are of importance, namely: "pull-in frequency" $f_{p,i}$ and "pull-out frequency" $f_{p,o}$.

Pull-in Frequency

If the loop contains a perfect integrator, pull-in will be accomplished no matter how large the initial frequency error. (Assuming no unwanted d.c. offsets in the loop and neglecting clipping limits of the integrator.) In a real loop filter, the largest frequency difference for which the loop can still pull into lock is called the "pull-in limit" $f_{p,i}$. This may be calculated by:

$$f_{p,i} \approx (2K_v K)^{1/2} / 2\pi \quad \dots \quad (6.3)$$

[6.2]

Where: $K_v = K_o K_d F(0)$

and: $K = K_o K_d F(\infty)$

and $F(0) =$ d.c. gain of entire loop filter

while $F(\infty) =$ d.c. gain of high-frequency path.

(see Fig. 6.11 and Equation 6.5)

The pull-in range may therefore be made as large as required simply by using a large d.c. gain K_v . This means that large pull-in can be achieved with as narrow a loop- (and therefore noise-) bandwidth as necessary; the two parameters are independent.

Pull-out Frequency

If the received carrier undergoes a large frequency step, the loop may unlock, skip a number of cycles and lock-up once again. There is a frequency-step limit

below which the loop does not skip cycles but remains "in-lock"; this is known as the "pull-out frequency" $f_{p.o.}$. According to Gardner [6.2] $f_{p.o.}$ is related to the loop natural frequency ω_n and damping-factor ξ as follows:

$$\omega_{p.o.} = 1,8 \cdot \omega_n (\xi + 1) \quad . . . \quad (6.4)$$

Where: $\omega_{p.o.} = 2\pi f_{p.o.}$

Pull-out frequency $f_{p.o.}$ is therefore related to loop bandwidth. The limit for the required $f_{p.o.}$ of the loop is determined by the frequency stability of the received carriers.

Drift in I.F. carrier frequencies is as a result of transmitter and receiver R.F. local oscillators drifting relative to one another.

The R.F. local oscillators are to be locked onto temperature-compensated-crystal-oscillators (TCXO's), which means a stability of $\leq 2\text{ppm}$ can be expected. Allowance must be made for the case where one oscillator drifts up and the other oscillator drifts down (they are at different locations), and vice-versa.

Total maximum relative drift is then: $df = 2 \cdot 2 \cdot 10^{-6} \cdot 23\text{GHz}$
 $= 184 \text{ KHz.}$

But the I.F. signal is passed through a frequency doubler before entering the synchronisation structure, which means maximum relative drift $df = 2 \cdot 184 = \underline{368 \text{ KHz.}}$

It is difficult to estimate the maximum instantaneous step in carrier frequency which can be expected to result from crystal instability etc. But a safe value should be approx. 50% Total expected carrier drift; i.e. approx. 184KHz.

Summarising:

We therefore require $f_{p1} \geq 368$ KHz and $f_{p0} \geq 184$ KHz in order to follow variations in I.F. carrier frequencies due to R.F. locked-source crystal instability. We also, however, require the double-sided loop bandwidth B_L small enough to ensure $\delta \geq 5$, assuming SNR at the output of the bandpass filter is 12,5 dB. Design of the PLL can now proceed on the basis of these criteria.

6.2.2 Phase-Lock-loop (PLL) Characteristics

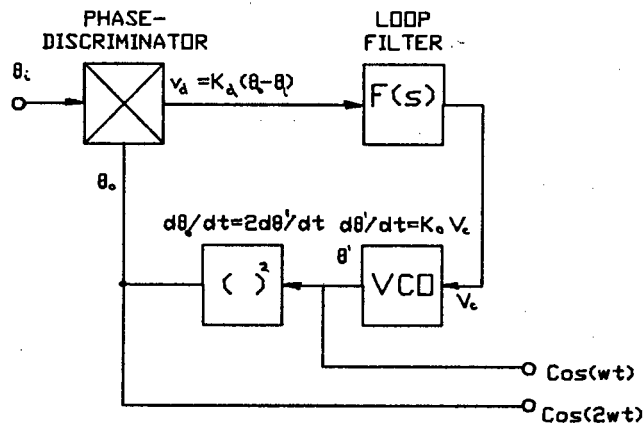


Fig. 6.10 SQUARE-LAW TRACKING LOOP SCHEMATIC

The closed-loop transfer function $H(s)$ is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = H(s) = \frac{2K_o K_d F(s)}{s + 2K_o K_d F(s)} \dots (6.5)$$

Where: K_o is the VCO gain factor,
 K_d is the Phase-detector gain factor,
 $F(s)$ is the filter transfer function.

The Type of a loop is a number equal to the number of perfect integrators within the loop. Any PLL is at least a Type I loop because of the perfect integrator in the VCO. This can be seen from the VCO transfer function:

$$\theta_o(s) = K_o V_c(s)/s \quad . . . \quad (6.6)$$

If the loop filter contains one perfect integrator, then the loop is Type II. From control theory it is known that a Type II feedback system is required to achieve zero displacement error for a step constant velocity input. This analogy to a PLL implies that a Type II loop is required to achieve zero phase error for a step frequency input. On power-up the loop VCO frequency will rarely be precisely the same as that of the carrier signal received at the loop input. This effectively represents a step constant frequency input (assuming frequency drift rate is negligible). For phase-coherent demodulation, zero phase error between extracted carriers and the information signal is required. One can therefore conclude that a Type II loop is necessary.

A second-order PLL with a high gain active filter approximates a Type II loop, whereas a PLL with a passive filter is Type I.

The type of active filter used is shown in Fig. 6.11(A), while a pole-zero plot is given in Fig. 6.11(B). A pole positioned at the s-plane origin produces the "perfect integrator" operation (and lagging phase-response), while a zero is situated on the negative real axis at $\sigma = -1/\tau_2$ (with associated leading phase response). Hence the name "lag-lead filter". Fig. 6.12(A) shows the loop Bode plot, illustrating the way in which the filter zero is positioned to ensure a reasonable phase-margin (i.e. the amount by which the open-loop phase-shift θ differs from π radians for open-loop gain = 0dB).

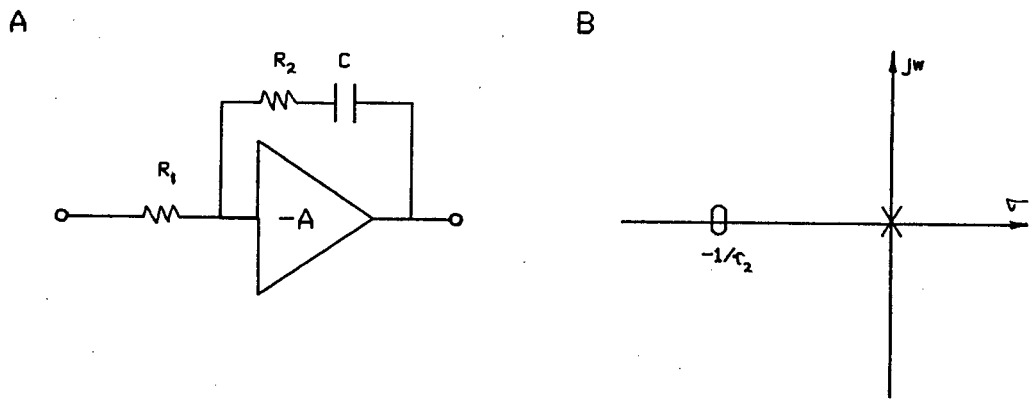


Fig. 6.11 PLL ACTIVE FILTER: (A) CIRCUIT
(B) POLE-ZERO PLOT

The transfer function for this filter:

$$F(s) = \frac{-A(sCR_2 + 1)}{sCR_2 + 1 + (1+A)(sCR_1)} \quad \dots \quad (6.7)$$

Which, for large A is approximately:

$$F(s) \approx -(s\tau_2 + 1)/s\tau_1 \quad \dots \quad (6.8)$$

$$\text{Where: } \tau_1 = R_1 C$$

$$\tau_2 = R_2 C$$

Substituting into Equation 6.5 and simplifying yields a closed-loop transfer-function of the form:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \dots \quad (6.9)$$

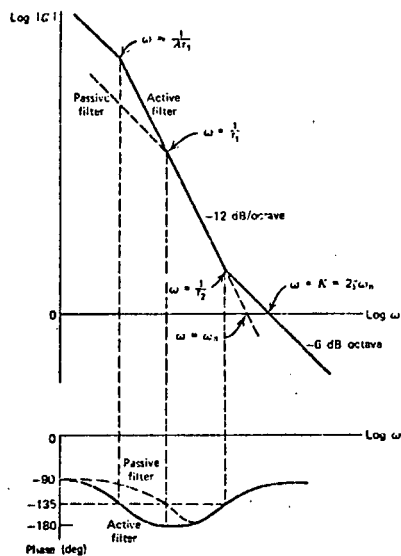
Where: $\omega_n \equiv$ natural frequency of the loop

$$= (2K_o K_d / \tau_1)^{1/2}$$

and: $\zeta \equiv$ damping factor

$$= (\tau_2 / 2) (2K_o K_d / \tau_1)^{1/2} = \tau_2 \omega_n / 2$$

A



B

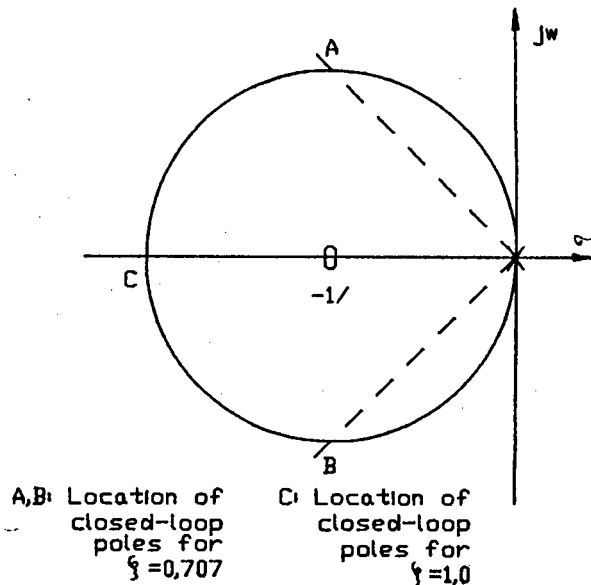


Fig. 6.12 (A) BODE-PLOTS: OPEN LOOP GAIN AND PHASE [6.2]
(B) ROOT-LOCUS PLOT

The frequency response for a high-gain second-order loop for various values of damping-factor is illustrated in Fig. 6.13. It can be seen that the loop performs a low-pass filtering operation on phase inputs. It is common practice to design second-order loops with a damping factor:

$$\zeta = 1/\sqrt{2} = 0,707$$

For this case the closed-loop poles lie on the same vertical line as the filter zero (see Fig. 6.12(B)). From Fig. 6.12(A) it can also be seen that $\zeta = 0,707$ ensures that the phase-lead breakpoint occurs above the unity gain point as required for loop stability.

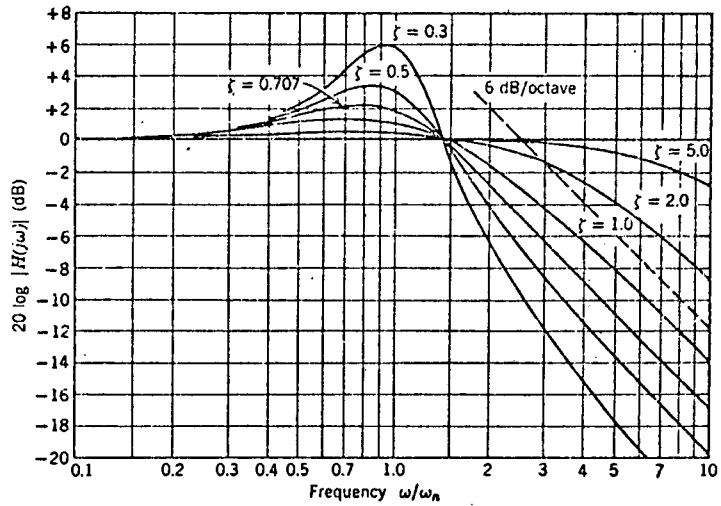


Fig. 6.13 FREQUENCY RESPONSE OF A HIGH-GAIN SECOND ORDER LOOP [6.2]

As given in Equation (6.4), the pull-out frequency $f_{p.o}$ is related to the loop natural frequency ω_n and damping-factor ζ as follows:

$$\omega_{p.o} = 1,8 \cdot \omega_n (\zeta + 1)$$

$$\text{Where: } \omega_{p.o} = 2\pi f_{p.o}$$

The required pull-out frequency $f_{p.o} = 184$ KHz and selecting a damping-factor $\zeta = 0,707$, we solve for ω_n :

$$\omega_n = \omega_{p.o} / [1,8(\zeta + 1)] = 376\,263 \text{ rad/s.}$$

$$\text{i.e. } f_n = 59,884 \text{ KHz}$$

The 3dB loop bandwidth B_L can now be calculated according to Equation 6.9:

$$B_{3dB} = (\omega_n / 2\pi) [2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{1/2}] \dots \quad (6.10)$$

Substituting for ζ and ω_n yields:

$$B_{3dB} = \omega_n / 2\pi (2,058) = 123,2 \text{ KHz.}$$

The double-sided bandwidth is then: $B_L = 2 \cdot B_{3dB}$

$$= 246,5 \text{ KHz.}$$

The parameter δ for the loop (as defined in Equation 6.2) can now be calculated. Assuming a SNR at the filter output of 12,5 dB (the minimum required for $\text{BER} \leq 10^{-7}$ for MSK):

$$\delta = 7,88 \text{ for a 2 MBit/s data-rate}$$

6.2.3 PLL Sub-Modules - Circuitry and Performance

6.2.3.1 The Phase-Discriminator

The SL6440 high-level mixer is used (see Appendix B for device data-sheets). D.C. coupling is required at the output to pass-on phase error information when frequency error = 0. Fig. 6.14(B) illustrates the transfer characteristic measured for the circuit shown in Fig. 6.14(A).

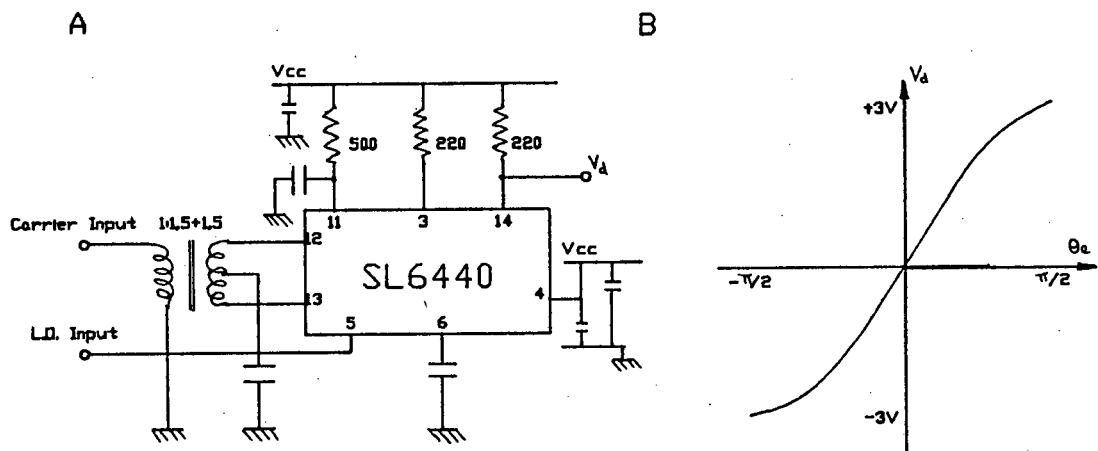


Fig. 6.14 PHASE-DISCRIMINATOR:(A) CIRCUIT

(B) TRANSFER CHARACTERISTIC

The phase-comparator output $v_o \approx 3 \sin \theta_e$ [V]

$$\approx 3\theta_e \text{ for } |\theta_e| \ll \pi/2 \text{ rad.}$$

$$\text{where: } \theta_e = (\theta_{i,n} - \theta_{o,u,t})$$

Now, $K_d(\theta) = dv_o/d\theta = d(3 \sin \theta)/d\theta = 3 \cos \theta$

i.e. $K_d(0) = 3 \text{ V/rad.}$

Better to take an average over $-\pi/2 \leq \theta \leq \pi/2$

Then $K_d \approx 6V/\pi\text{rad.} = \underline{1.9 V/\text{rad.}}$ ($-\pi/2 \leq \theta_e \leq \pi/2$)

For mixer-type phase discriminators, a phase-shift between the received carrier and the local oscillator signal of approx. $\pi/2$ radians is always present when the loop is phase-locked. To compensate for this, a $\pi/2$ radian phase-shifter is included in the loop as shown in Fig. 6.15. This modification has no effect on the closed-loop transfer function as it only serves to cancel an inherent error in the phase-discriminator.

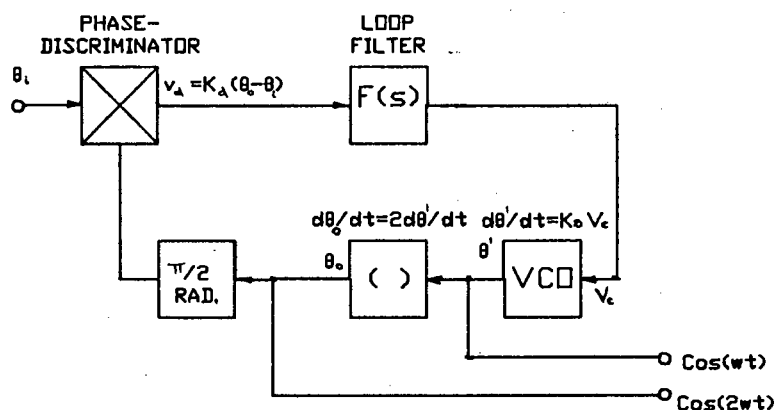


Fig. 6.15 PLL WITH $\approx \pi/2$ RADIAN PHASE-ERROR CANCELLATION

6.2.3.2 The VCO

The same VCO design as used in the MSK I.F. synthesizer is employed here. The VCO gain constant K_o can be measured from Fig. 5.10.

This gives $K_o \approx \underline{13.10^6 \text{ rad.s}^{-1}/\text{volt.}}$

6.2.3.3 The Active Filter

Time constants $\tau_1 = R_1 C$ and $\tau_2 = R_2 C$ (see Fig. 6.11) can now be calculated as follows:

Equation 6.9 gives:

$$\omega_n = (2K_o K_d / T_1)^{1/2}$$

Substituting values for ω_n , K_o and K_d and solving for τ_1 yields:

$$\tau_1 = 87.7 \cdot 10^{-6} \text{ sec.}$$

Also from Equation 6.9:

$$\xi = \tau_2 \omega_n / 2$$

Substituting $\xi = 0,707$ and ω_n gives:

$$\tau_2 = 2\xi / \omega_n = 1,88 \cdot 10^{-6} \text{ sec.}$$

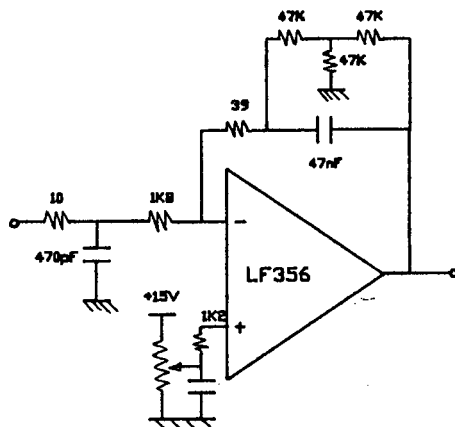


Fig. 6.16 ACTIVE FILTER CIRCUIT

An LF356 high-speed operational amplifier was used (see Appendix B for device data-sheets) to ensure good filter attenuation at high frequencies. Preventing carrier frequencies and multiples thereof (i.e. $f \geq 70$ MHz) from arriving at the active filter input is necessary since these reduce amplifier gain due to slew-rate limitation. A first order low-pass filter is included between phase-discriminator and active filter for this purpose. The breakpoint of this filter is placed sufficiently high above the difference-frequency signals of interest at the phase-discriminator output so that loop gain is not affected in terms of magnitude or phase.

An adjustable bias voltage on the non-inverting input on the op-amp is required to zero-out the d.c. offset on the signal from the phase-discriminator. The resistive network (effective resistance ≈ 140 K Ω) across the

feedback capacitor is to prevent saturation.

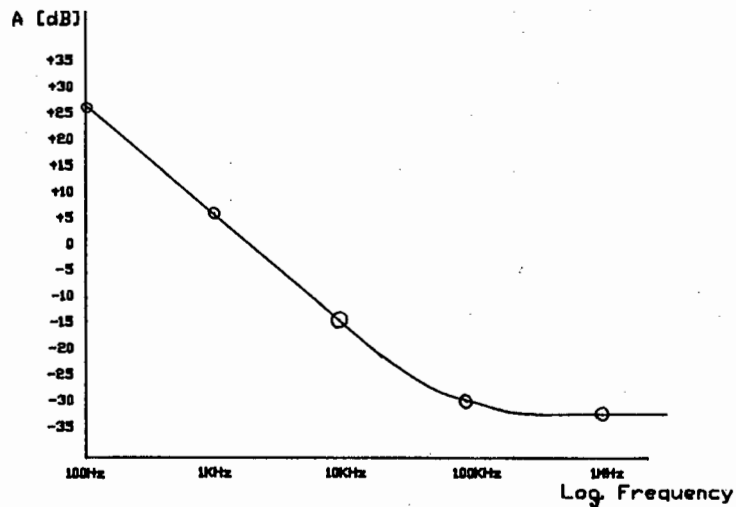


Fig. 6.17 FREQUENCY CHARACTERISTIC OF THE ACTIVE FILTER

6.2.3.4 Frequency-Doubler + $\pi/2$ Radian Phase-Shifter

Once again the SL6440 high-level mixer is used (see Appendix B for device data-sheets). However, the usual application of this device is the down-conversion of an R.F. or I.F. signal by mixing with a L.O. signal of similar frequency to yield a baseband signal. The device has therefore been designed to maximise the level of difference-frequency components, while sum-frequency components have been suppressed as much as possible.

In the frequency-doubler application, the identical signal $\cos A$ is fed into both input ports of the device, yielding an output:

$$\cos^2 A = \frac{1}{2}(1 + \cos 2A)$$

i.e. a d.c. term + a sum-frequency term.

Obtaining maximum sum-frequency output levels involves using a common-mode output stage and coupling the 2 positive power rail inputs.

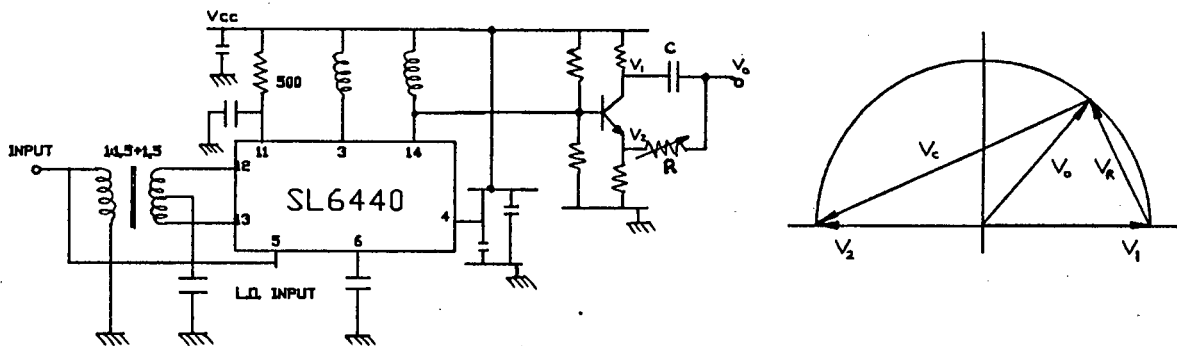


Fig. 6.18 (A) FREQUENCY-DOUBLER + $\pi/2$ RADIAN PHASE-SHIFTER

(B) PHASE-SHIFTER PHASOR DIAGRAM

6.2.4 Lock Indicator

The method of lock detection to be employed is known as the "quadrature phase detector". This phase detector has the received carrier signal applied as one input and a $\pi/2$ radian phase-shifted version of the local oscillator signal as the other. As shown in Fig. 6.14(B), the loop phase discriminator has an output voltage proportional to $\sin\theta$, (i.e. zero for $\theta_s=0$). The filtered output of the quadrature phase-detector must therefore be proportional to $\cos\theta$, (i.e. a maximum for $\theta_s=0$). "The magnitude of this output voltage, relative to that obtained from a noise-free stable input, provides a measure of the quality of lock. (If θ_s jitters, the average of $\cos\theta_s < 1$)". [6.2]

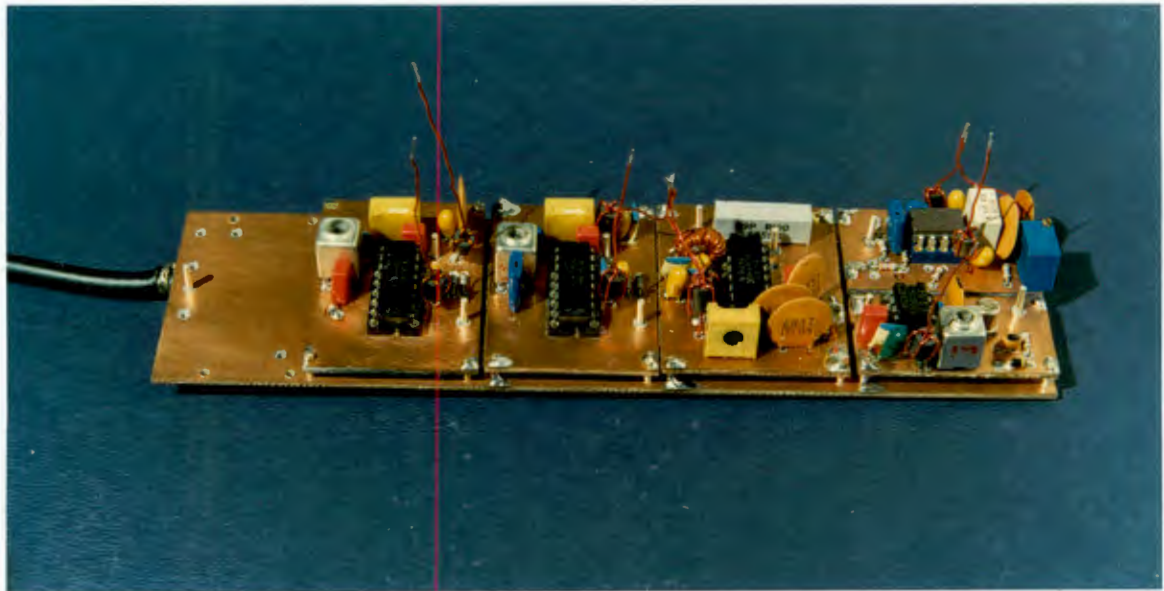


Fig. 6.21 SQUARE-LAW TRACKING LOOP

6.2.5 Producing a Clock-Signal at the Receiver

The PLL's described in preceding sections (and shown in receiver schematic Fig. 6.0) serve only to faithfully reproduce phase-coherent versions of signals $\cos(2\pi f_1 t)$ and $\cos(2\pi f_2 t)$. These are simply the two sinusoids which are "keyed" at the transmitter. Processing of these signals is still required (as shown in Fig. 6.0) in order to produce a clock signal as well as weighted quadrature carriers as required for "matched-filter" phase quadrature demodulation.

By definition, for MSK: $(f_1 - f_2)T = h = 0,5$
 i.e. $f_1 - f_2 = 1/2T$
 hence: $2f_1 - 2f_2 = 1/T$ i.e. the bit-rate
 clock signal.

6.2.5.1 Mixer Realisation

For this mixer, as well as those used for demodulation, the SL6440 device may be used in it's standard configuration as shown in Fig. 6.22.

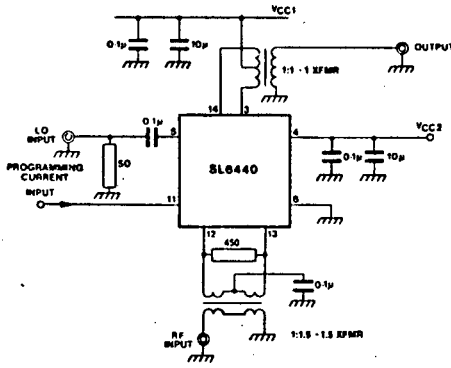


Fig. 6.22 MIXER CIRCUIT

6.2.5.2 Filter Design

Fig. 6.23(A) shows the required filter attenuation response. Although frequency components to be suppressed occur only at 140 MHz (carrier feedthrough) and 280 MHz (sum frequencies), the filter bandwidth should be made as small as possible to minimise noise on the clock signal. The attenuation response shown can be achieved by a 3rd order elliptic filter (as shown in Fig. 6.23(B)).

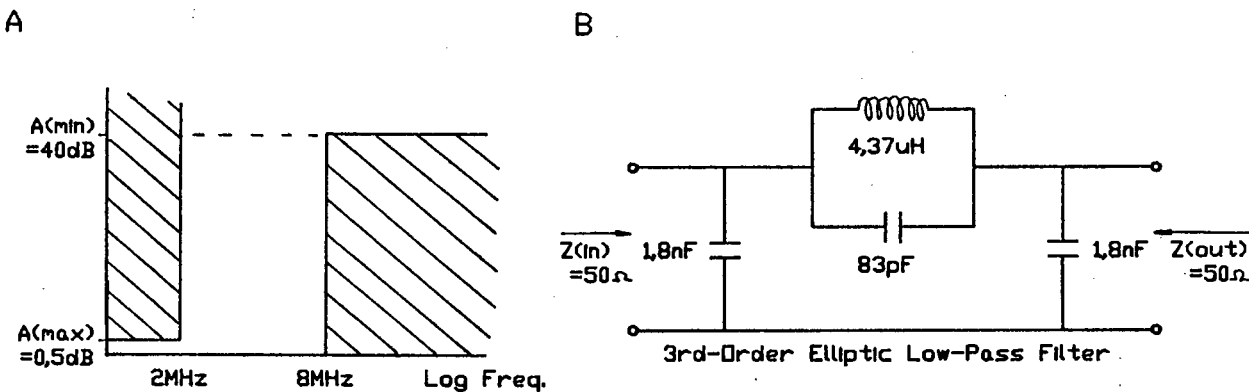


Fig. 6.23 FILTER (A) ATTENUATION RESPONSE
(B) CIRCUIT

6.2.6 Producing Weighted Quadrature Carriers

As described in Appendix A, the convolution integrals:

$$J(O) = -\int^T \text{Cos}(\pi t/2T) \text{Re}\{u(t) \cdot \exp.-j\omega_0 t\} dt \quad . . . \quad (A3)$$

$$J(T) = \int^T \text{Sin}(\pi t/2T) \text{Im}\{u(t) \cdot \exp.-j\omega_0 t\} dt \quad . . . \quad (A4)$$

where: $u(t) \equiv$ Received signal

$$\omega_0 \equiv \pi(f_1 + f_2)$$

must be performed alternately in order to make decisions on the state of bits received. These integrals can also be written:

$$J(O) = -\int^T u(t) \cdot \text{Cos}(\pi t/2T) \text{Cos}\omega_0 t \, dt \quad . . . \quad (6.11)$$

and:

$$J(T) = \int^T u(t) \cdot \text{Sin}(\pi t/2T) \text{Sin}\omega_0 t \, dt \quad . . . \quad (6.12)$$

In order to implement this, the received signal must be multiplied by the weighted quadrature carriers:

$$C_1(t) = \text{Cos}(\pi t/2T) \text{Cos}\omega_0 t$$

and $C_0(t) = \text{Sin}(\pi t/2T) \text{Sin}\omega_0 t$ before integration.

The method by which these are produced from the PLL signals (refer to Fig. 6.0) can be understood from the trigonometric identities:

$$\text{Cos}A + \text{Cos}B = 2\text{Cos}\frac{1}{2}(A-B) \cdot \text{Cos}\frac{1}{2}(A+B)$$

and:

$$\text{Cos}A - \text{Cos}B = -2\text{Sin}\frac{1}{2}(A-B) \cdot \text{Sin}\frac{1}{2}(A+B)$$

hence:

$$\text{Cos}(2\pi f_1 t) + \text{Cos}(2\pi f_2 t) = 2\text{Cos}\pi(f_1 - f_2)t \cdot \text{Cos}\pi(f_1 + f_2)t \quad . . . \quad (6.13)$$

and:

$$\text{Cos}(2\pi f_1 t) - \text{Cos}(2\pi f_2 t) = 2\text{Sin}\pi(f_2 - f_1)t \cdot \text{Sin}\pi(f_1 + f_2)t \quad . . . \quad (6.14)$$

Since by definition, for MSK: $(f_1 - f_2)T = h = 0,5$

and: $\pi(f_1 + f_2) = \omega_0$, Equations 6.13 and

6.14 can be simplified:

$$2\text{Cos}\pi(f_1 - f_2)t \cdot \text{Cos}\pi(f_1 + f_2)t = 2\text{Cos}\pi t/2T \cdot \text{Cos}\omega_0 t$$

and:

$$2\sin\pi(f_2-f_1)t \cdot \sin\pi(f_1+f_2)t = -2\sin\pi t/2T \cdot \sin\omega_0 t$$

These are the required carriers.

6.2.6.1 Summing-Point Realisation

Since signals of frequency close to I.F. (70 MHz) are to be added, the conventional operational-amplifier summing junction is impossible.

A summing junction which is capable of operating at I.F. frequencies is shown in Fig. 6.24.

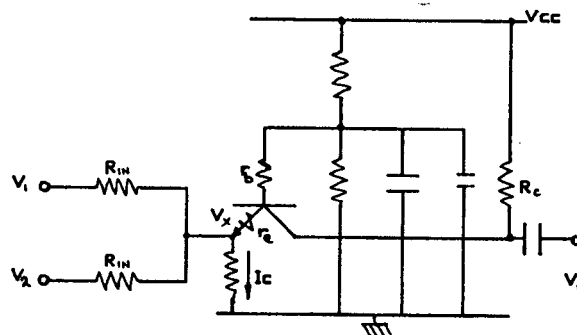


Fig. 6.24 SUMMING-JUNCTION CIRCUIT

A common-base transistor stage is employed where the small-signal impedance looking into the emitter = $r_e + r_b$, where:

$$r_e = V_T / I_c \quad [\Omega] \quad \dots \quad (6.15)$$

$$V_T = kT/q \quad (k \equiv \text{Boltzmann's const.})$$

($T \equiv$ Absolute temp.)

($q \equiv$ Electron charge)

≈ 25 mV at room temp.

$I_c =$ Quiescent collector current
[mA]

and:

$r_b =$ "Bulk" or "spreading resistance"

Then the voltage variation at the summing-point:

$$v_x = \frac{(r_e + r_b) \Sigma v_{i_n}}{(R_{i_n} + r_e + r_b)} \dots (6.16)$$

and output voltage:

$$v_o = (R_c / R_i) \Sigma v_i \quad \text{Provided } v_x \approx 0 \dots (6.17)$$

A trade-off situation clearly exists, since if R_i is made large (i.e. $R_i \gg r_e + r_b$) then it is certain that $v_x \approx 0$ and there will be therefore minimal interaction between channels. But stage gain $G_v = v_o / \Sigma v_i = R_c / R_i$ will be poor. (R_c cannot be made too large since this would force the transistor into cut-off.)

A simple implementation of the above configuration uses the SL560C R.F. Amplifier (see Appendix B for device data-sheets). The manufacturer quotes $r_b = 17\Omega$ for the transistors within the device. I_c should be set as large as feasibly possible to minimise r_e and hence v_x .

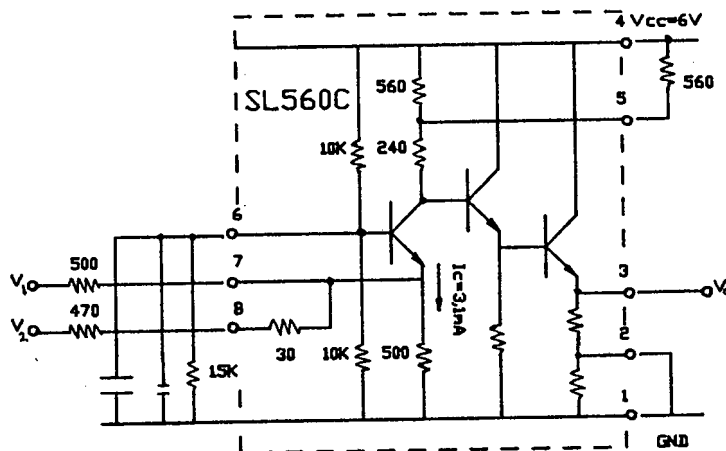


Fig. 6.26 SUMMING-JUNCTION USING THE SL560C

The circuit shown in Fig. 6.27 has:

$$r_e \approx 8\Omega$$

$$v_x / \Sigma v_{i_n} = 0,048 \text{ (i.e. <5\%)}$$

$$\text{Stage gain } v_o / \Sigma v_{i_n} \approx 0 \text{ dB.}$$

No clipping will occur due to transistor cut-off provided input signal-levels are kept below $\approx +3$ dBm.

6.3 Demodulator-Detector

As shown in the MSK receiver schematic (Fig. 6.0), the demodulation-detection process involves down-conversion by mixing the I.F. MSK signal with weighted quadrature carriers $C_i(t)$ and $C_q(t)$. Channel signals are then passed through detection filters which perform:

$$\int_{-\tau}^{\tau} dt \text{ on the I-Channel}$$

and: $\int_{-\tau}^{\tau} dt \text{ on the Q-Channel.}$

Bit-decisions for the respective channels are performed by threshold detectors, after which the bitstream of each channel must be differentially-decoded to compensate for the inherent differential encoding process associated with each channel in MSK. A bit-interleaving module then reconstructs the transmitted bitstream from the two channel bitstreams. A final differential decoder reverses the differential-encoding process which was performed at the transmitter to solve the problem of π radian carrier phase ambiguity. Timing for threshold detectors, differential decoders and bit-interleaving structure is derived from the clock signal extracted as described in Section 6.2.5.

6.3.1 Down-Conversion Mixers

These consist of SL6440 configurations precisely the same as that described in Section 6.2.5.1.

6.3.2 Detection Filters

Correlation of the received signal with it's stored replica, followed by an integration operation results in optimum detection performance. After multiplying the received signal with weighted quadrature carriers, deBuda [1.10] recommends the use of "Integrate-and-Dump" (I & D)

detection filters integrating over two bit-periods. Austin et al [3.1] show that I & D filters are only optimum for an ideal, distortionless channel. In the presence of bandlimiting, simple passive detection filters generally yield the best performance. Austin et al also show that MSK detection without receiver carrier weighting i.e. MSK(NW) may outperform a weighted-carrier demodulator-detector (MSK(W)). However, this occurs only under conditions of severe bandlimiting (see Fig. 6.26). In addition, the optimum value of detection-filter bandwidth is highly dependent on channel bandwidth in the case of MSK(NW), making this an unfavourable detection scheme for performing simulation tests in which E_b/N_0 vs. channel bandwidth performance is measured. Fig. 6.27 (A) and (B) show performance sensitivity to detection-filter bandwidth for MSK(NW) and MSK(W) respectively.

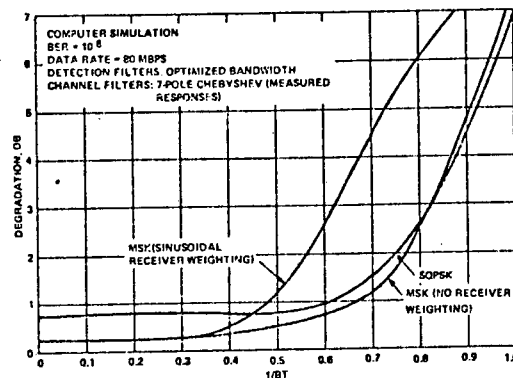
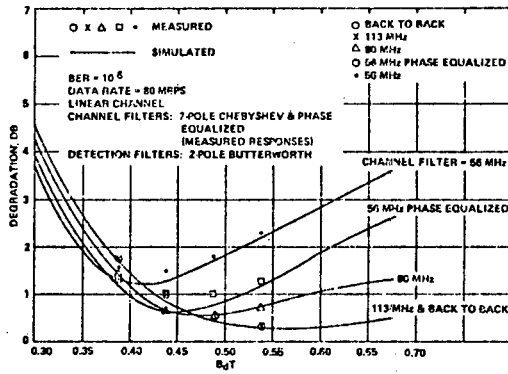


Fig. 6.26 E_b/N_0 DEGRADATION FOR LINEAR CHANNEL AND TWO
 -POLE BUTTERWORTH DETECTION FILTERS [3.1]

A



B

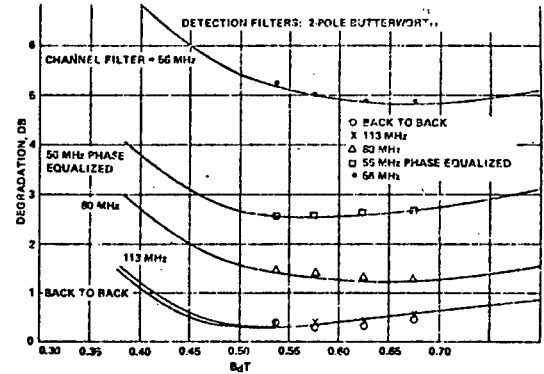


Fig. 6.27 PERFORMANCE SENSITIVITY TO DETECTION FILTER BANDWIDTH: (A) MSK(NW) (B) MSK(W) [3.1]

From Fig. 6.27(B) it can be seen that for a detection-filter bandwidth:

$$B_d = 0,65/T,$$

(where $T_s \equiv$ Symbol period = 2.bit-period T_b), MSK(W) shows a degradation from ideal performance of approx. 1,3 dB. This value also only varies by approx. 0,2dB for:

$$0,50 \leq B_d T_s \leq 0,80.$$

For a fixed detection-filter bandwidth B_d , this corresponds to a variation in channel-bandwidth/bit-rate:

$$0,8 \leq B T_s \leq 1,3$$

i.e. for a 2,048 MBit/s bit-rate, variation in channel-bandwidth: 1,64 MHz $\leq B \leq$ 2,66 MHz.

This is exactly the range of channel bandwidths in which we are interested for performing simulation tests.

The detection-filter to be used is therefore a 2-pole Butterworth passive filter with 3dB bandwidth:

$$B_d = 0,65/T_s = 0,65/2T_b = 665,6 \text{ KHz.}$$

Normalised element values for 2nd order Butterworth low-pass filter (from tables [6.3]) are:

$$L_n = 1,4142$$

$$C_n = 1,4142$$

$$(Z_{i,n} = Z_{o,n} = 1\Omega, \omega_0 = 1 \text{ rad/s.})$$

Denormalising for $Z_{in} = Z_{out} = 100\Omega$ and $\omega_0 = 2\pi \cdot 665,6 \cdot 10^3$ gives:

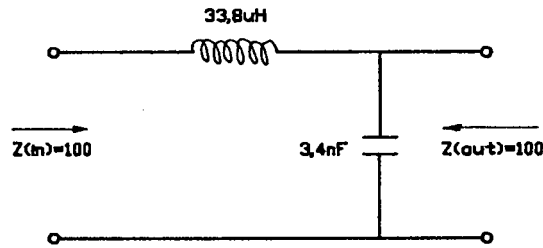


Fig. 6.28 2nd ORDER BUTTERWORTH DETECTION FILTER

6.3.3 Threshold Detector

The SL541B High slew-rate operational amplifier (see Appendix B for device data-sheets) is used as shown in Fig. 6.29. A small amount of hysteresis is included to ensure "clean" switching. The threshold detector is "clocked" by latching the output signal at rising-edge instants of the symbol-rate clock (i.e. $1/T_s = 1/2T_b$). The latch function is performed by $\frac{1}{2}$ 74LS74 D flip-flop.

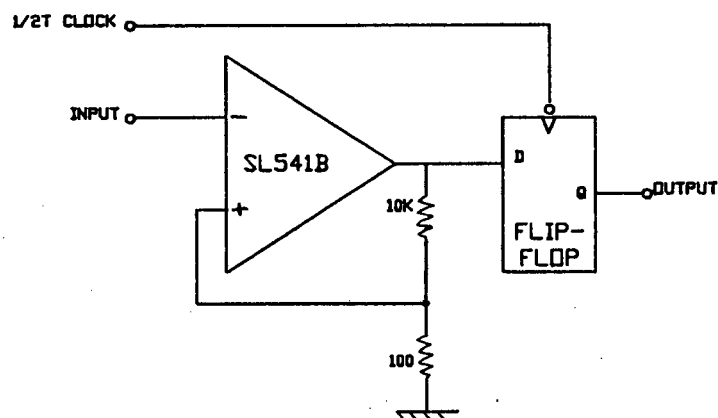


Fig. 6.29 CLOCKED THRESHOLD DETECTOR USING THE SL541B

6.3.4 Channel Differential Decoders

These perform the identical function to a differential encoder (as described in Section 5.2.2) and are constructed in the same way. These decoders, however, operate on the I- and Q-Channel bitstreams as detected by the respective threshold detectors. The symbol-rate is hence $1,024 \cdot 10^6$ symbols/s (i.e. half the transmission bit-

rate). Timing for these decoders is therefore also at half the normal clock-frequency and is derived from the clock signal described in Section 6.2.5.

6.3.5 Bit-Interleaving Network

This function can be performed simply by the use of a 74LS157 multiplexer with the SELECT input driven by a clock-signal at half the normal clock-frequency. The +5V half-cycle of the clock-signal then selects the I-Channel output, while the 0V half-cycle selects the Q-Channel output. (See Fig. 6.30)

6.3.6 Output Differential Decoder

This module is precisely the same as that described in Section 5.2.2 and is clocked at the same rate (i.e. transmission bit-rate). Fig. 6.30 illustrates the circuit configuration for the channel differential decoders, bit-interleaving network and output differential decoder.

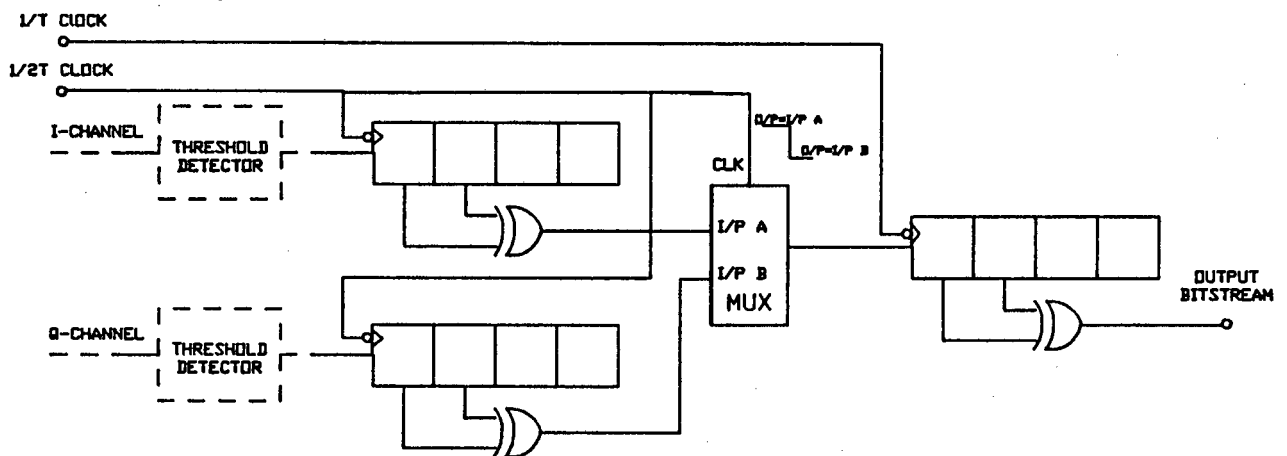


Fig. 6.30 CHANNEL DIFFERENTIAL DECODERS, BIT-INTERLEAVING NETWORK AND OUTPUT DIFFERENTIAL DECODER

REFERENCES

- [6.1] J.R.CRUIZ, R.S.SIMPSON, "Minimum-Shift-Keying Signal Detection with Noisy Reference Signals", IEEE Trans. on Comm., Vol. COM-26, June 1978.
- [6.2] F.M.GARDNER, "Phaselock Techniques", New York, John Wiley, 1979.
- [6.3] G.C.TEMES, J.W.LAPATRA, "Circuit Synthesis and Design", New York, McGraw-Hill 1977.

CHAPTER 7

SIMULATION TESTS

7.0 Introduction

The MSK transmission system described in Chapters 4,5 and 6 does actually convey digital information using the MSK format. All that is missing is the R.F. radio-link between transmitter and receiver. Information relating to the performance of an MSK digital microwave transmission system can be obtained by simulating the restrictions (e.g. bandwidth) and imperfections (e.g. noise and interference added) of the radio-link. The degrading effects of modem imperfections such as incorrect modulation index at the transmitter can be obtained, as well as MSK performance under conditions of non-linear amplification (log. amplifier).

7.1 Test Equipment

Specialised test equipment for measuring the performance of digital radio transmission systems is required for performing the simulation tests. A short description of the function of each piece of equipment is given here. Detailed specifications can be found in Appendix B.

7.1.1 Noise and Interference Test Set

The HP Model 3708A Noise and Interference Test Set is designed for operation in the I.F. section of a digital radio system where it adds calibrated levels of white noise and/or interference signals to the radio I.F. carrier. Built-in power meter and microprocessor control enable continuous adjustment of noise and interference

levels added to ensure that constant carrier-to-noise and carrier-to-interference ratios are maintained, regardless of radio carrier power variations. This "tracking-mode" hence enables the 3708A to maintain selected C/N and C/I ratios with a varying carrier.

The 3708A can, in addition, measure and display received I.F. power as well as I.F. filter noise bandwidth.

7.1.2 Digital Transmission Analyser

The HP Model 3764A Digital Transmission Analyser emits a pseudorandom data sequence to be applied to the transmitter input of a digital radio transmission system. The data sequence extracted at the receiver is then fed back into the HP 3764A input port (the same 3764A, or another one if the receiver is not situated locally). Since the pseudorandom sequence is deterministic and repetitive, a comparison can be made between the sequence as received after passing through the transmission system and the true sequence generated by the 3764A. The instrument performs this comparison and displays information regarding errors in the received data, including error ratio, error count error-free seconds etc. (see Appendix B). The HP 3764A also provides information about the timing jitter measured on the received data signal.

7.1.3 Constellation Display

The HP3709A Constellation Display is designed to provide an indication of the overall performance of a digital radio, by operation in two modes:

(a) Eye Monitor Mode

The received data signal, immediately before clocked symbol detection, is displayed in the form of an "eye-diagram" [1.8]. An indication of jitter tolerance and

inter-symbol interference (ISI) is obtained from the size of the eye-opening, both horizontally and vertically.

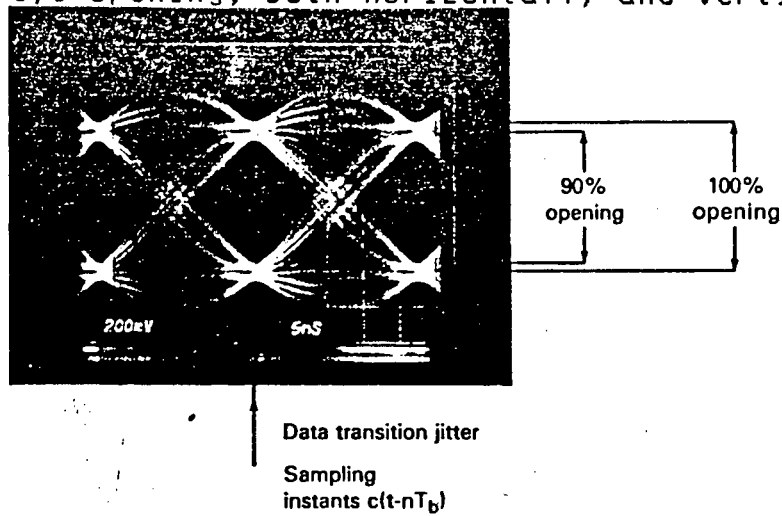


Fig. 7.0 A TYPICAL EYE DIAGRAM [1.8]

(b) Constellation Mode

The "signal state space" at the instant of symbol detection is displayed in the form of discrete points.

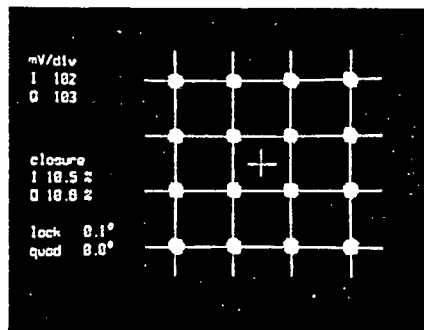


Fig. 7.1 CONSTELLATION DISPLAY OF 16-QAM

Observations which can be made from the display relating to system imperfections include:

- "Smearing" of points indicating ISI and noise
- Displacement of outermost points indicates system nonlinearities such as AM-PM conversion.

7.2 Test Descriptions

7.2.1 BER vs. Modulation Index Error Test

The "MSK I.F. Synthesizer" module (see Fig. 4.0) has two control inputs C_1 and C_2 which can be used to independently adjust keyed frequencies f_1 and f_2 respectively. This:

- (a) Facilitates unrestricted control of modulation index for the purpose of measuring BER for various errors in mod. index. These results can then be compared with analytical predictions made in Appendix A.
- (b) Provides a possible input point for feedback control of modulation index.

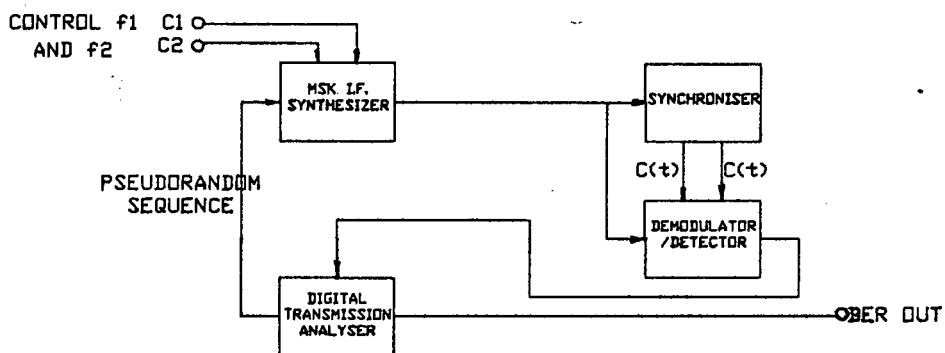


Fig. 7.2 TEST CONFIGURATION FOR MEASURING BER vs. MOD. INDEX ERRORS

For the above test mod. indexes of interest are:

- (i) For a linear varactor curve: $0,4 \leq h \leq 0,6$. Simulating erroneous mod. indexes due to a shallower or steeper varactor characteristic is achieved by reducing and increasing dV respectively. (See Fig. 7.3(A)).

- (ii) For the case where the varactor curve may not be assumed locally linear. This is simulated by reducing dV_1 and increasing dV_2 (or vice-versa) i.e.

from: $dV_1 = 0,6/2T$ and $dV_2 = 0,4/2T$

to: $dV_1 = 0,4/2T$ and $dV_2 = 0,6/2T$

(See Fig. 7.3(B)).

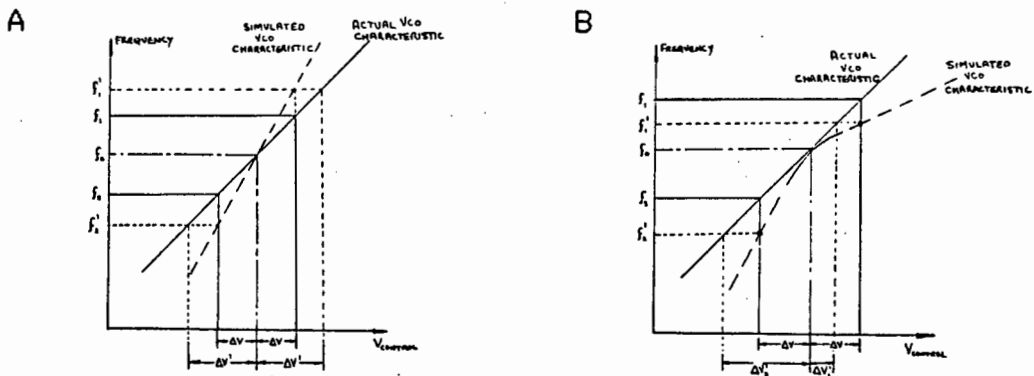


Fig. 7.3 VARIATIONS IN MOD. INDEX OF INTEREST

7.2.2 BER vs. E_b/N_0 and BER vs. C/I Tests

The HP 3708A which can control C/N and C/I by adding noise and interference respectively to the I.F. signal can be used as shown in Fig. 7.4 to measure BER vs. E_b/N_0 and BER vs. C/I for the simulated MSK system.

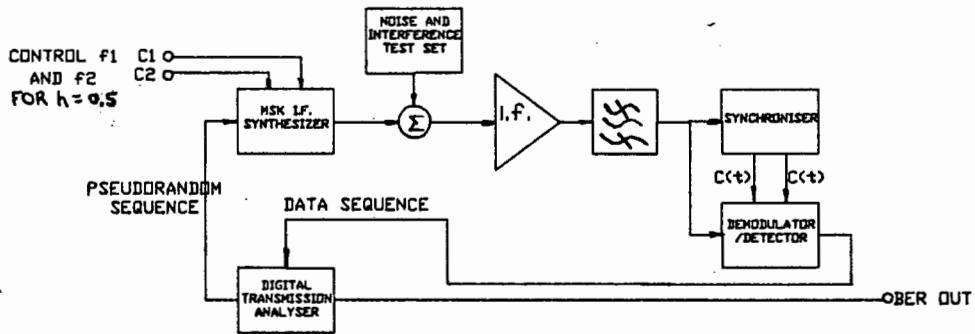


Fig. 7.4 BER vs. E_b/N_0 MSK SIMULATION TEST

7.2.3 Measuring BER Performance under Fading Conditions

Here the same test configuration as shown in Fig. 7.4 is used while including a low noise amplifier (LNA) and logarithmic amplifier in front of the demodulator. This enables tests to be performed on system performance under simulated conditions of multi-path propagation, rainfading etc. It also permits the effects of limiting of the log. amp. (to be used in the actual system) to be assessed.

7.2.4 BER vs. Bandwidth Limitation Performance Test

MSK BER vs. bandwidth limitation performance can be measured by passing the MSK I.F. signal through a bandpass filter before entering the demodulator.

In addition, combinations of all of the above tests can be carried-out simultaneously e.g. MSK noise performance measurement under conditions of various band-limitations, or BER vs. mod. index errors for various channel bandwidths etc.

INVESTIGATING THE EFFECTS ON MSK PERFORMANCE OF VARIATIONS
IN MODULATION INDEX

A.0 MSK Demodulation

In order to investigate the degradation effects caused by incorrect modulation index in an MSK system, it is necessary to first understand the theoretical operation of an MSK demodulator.

If the MSK signal at the receiver is narrow-band, e.g. at I.F. or R.F., then we may describe it by it's pre-envelope $u(t)$:

$$u(t) = \exp. j\{\pi(f_1+f_2)t+\theta(t)\} \dots (1.6)$$

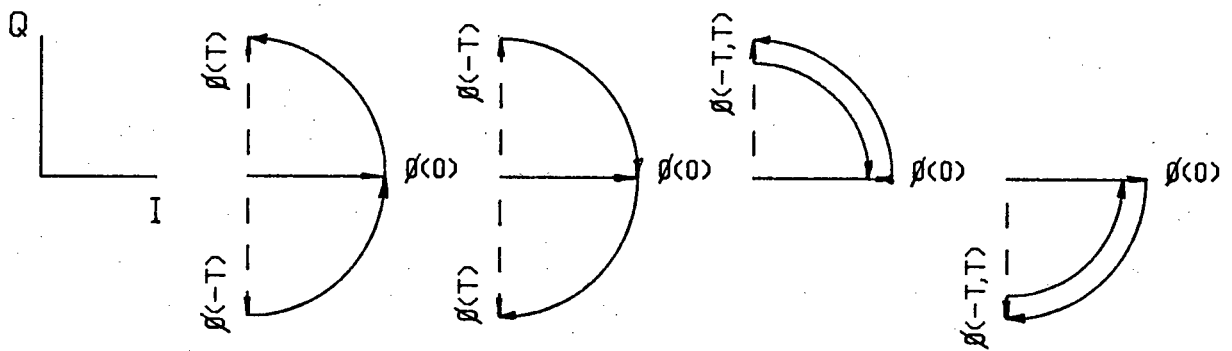
Let $\omega_0 = \pi(f_1+f_2)$ and let $\theta(0) = 0$ or π be the phase at time $t=0$, then:

$$u(t) = \begin{cases} + \exp. j(\omega_0 t - \pi t/2T) & \theta(0) = \begin{cases} 0 & \dots (A.1) \\ \pi \end{cases} \\ - \exp. j(\omega_0 t - \pi t/2T) & \end{cases}$$

$(0 \leq t \leq T)$

Where the sign within the exponent is: positive for a space
negative for a mark

Equation A.1 also holds for the interval $-T \leq t \leq 0$, even if the sign within the exponent (i.e. bit transmitted) changes from one interval to the next.



For all of the above cases $I(t) = \cos \pi t/2T$

Fig. A.0 I-CHANNEL COMPONENT FOR ALL PERMUTATIONS OF BITS TRANSMITTED DURING 2 CONSECUTIVE INTERVALS (FOR $\emptyset(0)=0$)

From Fig. A.0 it is evident that Real-part:

$$\text{Re}\{u(t)\exp.-j\omega_0 t\} = \text{Re}\{\exp.j(\cdot-\pi t/2T)\} = \cos(\pi t/2T)$$

for $\emptyset(0)=0$, and similarly for $\emptyset(0)=\pi$:

$$\text{Re}\{u(t)\exp.-j\omega_0 t\} = \text{Re}\{-\exp.j(\cdot-\pi t/2T)\} = -\cos(\pi t/2T)$$

. . . (A.2)

NOTE that the function $\text{Re}\{u(t)\exp.-j\omega_0 t\}$ depends only on $\emptyset(0)$ and not on any other $\emptyset(nT)$. ($n=\pm 1, \pm 2, \dots$). The decision can therefore be made between $\emptyset(0)=0$ or π based on the information received during both bit intervals: $-T \leq t \leq T$.

ALSO: The function $\text{Re}\{u(t)\exp.-j\omega_0 t\}$ may be produced by multiplying the incoming MSK signal at I.F. ($u(t)$) by the real-part of a phase-coherent carrier ($\cos \omega_0 t$).

A matched-filter type receiver structure can be implemented by a clocked integrate-and-dump filter in baseband which performs:

$$J(0) = -\tau \int^{-\tau}^{\tau} \cos(\pi t/2T) \text{Re}\{u(t)\exp.-j\omega_0 t\} dt \quad . . . (A.3)$$

deciding: $\emptyset(0)=0$ for $J(0) > 0$

and: $\theta(0) = \pi$ for $J(0) < 0$

This decision is made every alternate interval pair to yield phases $\theta(2nT)$ and hence the corresponding bits.

The other half of the transmitted bits i.e. every alternate interval $T, 3T, 5T \dots$ are yielded from the Q-channel (imaginary-part) of the pre-envelope:

$$J(T) = \int_0^{2T} \sin(\pi t/2T) \text{Im}\{u(t) \exp.-j\omega t\} dt \dots (A.4)$$

deciding: $\theta(T) = \pi/2$ for $J(T) > 0$

and: $\theta(T) = -\pi/2$ for $J(T) < 0$

As can be seen, this decision is taken over the interval $0 \leq t \leq 2T$. This yields phases $\theta[(2n-1)T]$.

With all $\theta(nT)$ recovered, the transmitted bitstream can be reconstructed.

A.1 The Effect of Incorrect Modulation Index on MSK Demodulation

Let the frequency deviation ratio $h = (\omega_1 - \omega_2)T_b / 2\pi = 0,5 + dh$. Then transmission of a "space", i.e. ω_1 for duration T_b will result in a linear phase-advance of the "carrier" at frequency ω_0 by: $(\omega_1 - \omega_0)T_b = \pi(0,5 + dh)$ radians.
(Where $\omega_0 = (\omega_1 + \omega_2) / 2$)

Similarly, transmission of a "mark", i.e. ω_2 for duration T_b results in a linear phase-retard = $\pi(0,5 + dh)$ radians.

Intuitively it is clear then, that a bit-pattern of alternate marks and spaces causes phase errors to cancel. However, strings of marks or spaces produce a compounding phase error.

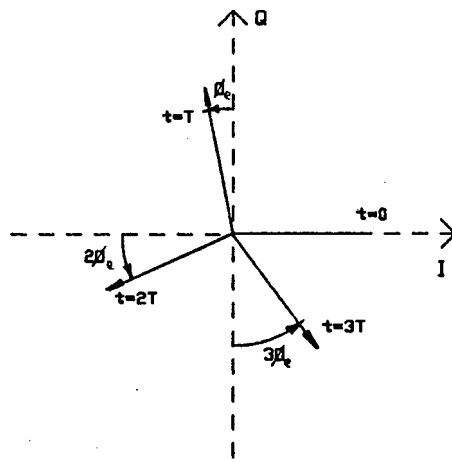


Fig. A.1 COMPOUNDING PHASE ERROR FOR 3 CONSECUTIVE "MARKS"

A.1.0 Manifestation of Phase Errors in Producing Bit Errors

Detection of the received signal phase occurs by individual multiplication of the received signal with two phase-quadrature carrier signals at frequency ω_0 , separating the I- and Q-channel components.

Note, since variations in modulation index produce frequency errors symmetrical about the carrier frequency $\omega_0 = (\omega_1 + \omega_2) / 2 = [(\omega_1 - d\omega) + (\omega_2 + d\omega)] / 2$, errors in extracted carrier frequency may be assumed negligible. (This assumes local linearity in the varactor v vs. f characteristic.)

To simplify the calculation of the effects of cumulative phase errors, two cases are considered:

(a) Assuming zero phase error at time $t=0$

Modulation index error dh changes pre-envelope $u(t)$:

$$u(t) = \begin{cases} +\exp.j[\omega t - (0,5+dh)\pi t/T] & \theta(0) = \begin{cases} 0 & \dots & (A.5) \\ \pi \end{cases} \\ -\exp.j[\omega t - (0,5+dh)\pi t/T] \end{cases}$$

(See Eqn. A.1)

Equation A.2 therefore becomes:

$$\begin{aligned} \operatorname{Re}\{u(t) \exp.-j\omega t\} &= \operatorname{Re}\{\exp.+ -j[(0,5+dh)\pi t/T]\} \\ &= \cos[(0,5+dh)\pi t/T] \end{aligned}$$

for $\varnothing(0) = 0$, and:

$$\begin{aligned} \operatorname{Re}\{u(t) \exp.-j\omega t\} &= \operatorname{Re}\{-\exp.+ -j[(0,5+dh)\pi t/T]\} \\ &= -\cos[(0,5+dh)\pi t/T] \end{aligned}$$

for $\varnothing(0) = \pi$.

. . . (A.6)

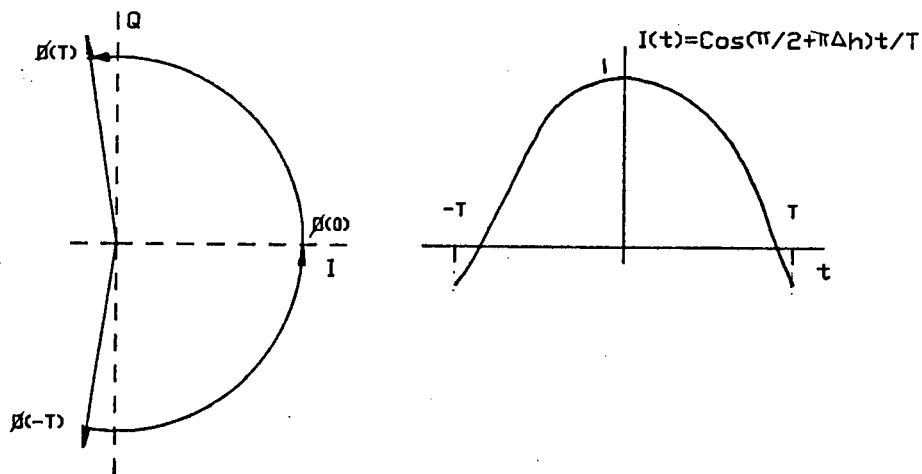


Fig. A.2 PHASOR $\varnothing(t)$ LOCUS ($-T \leq t \leq T$)

The matched-filter correlation performed in Eqn. A3 then becomes:

$$J(0) = -\int_{-T}^T \cos(\pi t/2T) \cdot [+ \cos(\pi/2 + \pi dh)t/T] dt \quad . . . (A.7)$$

(+ indicating $\varnothing(0)=0$, - indicating $\varnothing(0)=\pi$)

Considering the case $\varnothing(0)=0$, we find:

$$\begin{aligned} J(0) &= +1/2 \int_{-T}^T \{ \cos[(1+dh)\pi t/T] + \cos[(-dh)\pi t/T] \} dt \\ &= [T/(1+dh)\pi] \cdot [\sin(1+dh)\pi] + [T/dh\pi] \cdot [\sin(dh\pi)] \end{aligned}$$

Now, since $\sin(1+dh)\pi = -\sin(dh)\pi$:

$$J(0) = [T/dh\pi - T/(1+dh)\pi]\sin(dh\pi) \dots (A.8)$$

For $dh = 0$ this gives: $J(0) = T$

Now, a decision on whether $\emptyset(0) = 0$ or π is made on the basis of whether $J(0) > 0$ or $J(0) < 0$ respectively.

The value of dh for which a bit error will occur after only a single bit is therefore that for which:

$$J(0) = [T/(dh\pi) - T/(1+dh)\pi]\sin(dh\pi) = 0$$

which is true for: $[\sin(dh\pi)]/(dh\pi) = \sin(dh\pi)/(1+dh)\pi$
 $dh = \pm 1, \pm 2 \dots$

(b) The case of non-zero phase error at time $t = 0$

More interesting may be to examine the result of applying the matched-filter correlation integral to a phase-shifted input signal. That is, the case where $dh = 0$ has caused a compounding phase-shift during the time $t < 0$, causing $\emptyset(0) \neq 0$, but shifted by phase error \emptyset_0 to $\emptyset(0) = \emptyset_0$. Then:

$$\begin{aligned} J(0) &= -\int_{-T}^T \cos\pi t/2T \cdot \cos(\pi t/2T + \emptyset_0) dt \\ &= 1/2\{T/\pi[\sin(\pi + \emptyset_0) - \sin(-\pi + \emptyset_0)] + 2T\cos\emptyset_0\} \\ &= T\cos\emptyset_0 \dots (A.9) \end{aligned}$$

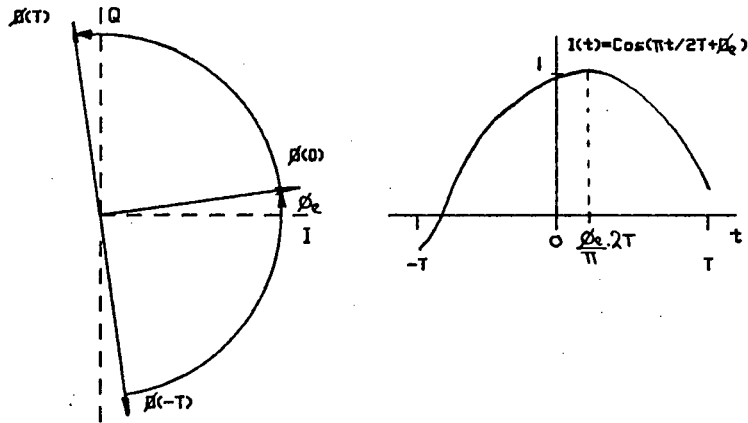


Fig. A.3 PHASOR $\phi(t)$ LOCUS ($-T \leq t \leq T$)

(Check: $\phi_e = 0$ gives $J(0) = T$, as before.)

Therefore, since the decision threshold for $J(0) = 0$, the required phase error to cause a bit decision error is:

$$\phi_e \geq \pm \pi/2$$

Since a modulation index error dh produces a phase error:

$$\phi_e = +\pi dh \text{ for a "space", and}$$

$$\phi_e = -\pi dh \text{ for a "mark",}$$

it can be deduced that in general, a bit error is produced after M marks and S spaces where:

$$|M-S|dh \geq 1/2 \quad . . . \text{ (A.10)}$$

Provided long strings of marks or spaces are avoided, and as long as purely random data is transmitted (i.e. probability $P(1)=P(0)=1/2$), the value $|M-S|$ can never exceed a certain value $|M-S|_{MAX}$. Now, provided dh is controlled to a level below $1/(2|M-S|_{MAX})$, no bit errors will occur as a result of incorrect modulation index.

A.1.1 Reducing the probability of long strings of "marks" or "spaces" in the transmitted bitstream

A simple mechanism for achieving this is to introduce identical modules at the transmitter and receiver which

perform the following function: The number of consecutive bits of equal state (i.e. mark or space) in the bitstream is counted. As soon as the count reaches some threshold e.g. 4 bits, the module inverts the bitstream, converting marks to spaces and vice versa. Since the identical function is performed twice, the net effect on the transmitted data is nil. However, it reduces (but doesn't exclude) the number of strings of marks or spaces of length > 4 passing between modulator and demodulator. Fig. A.4 illustrates how a string of length > 4 bits could still occur between modulator and demodulator.

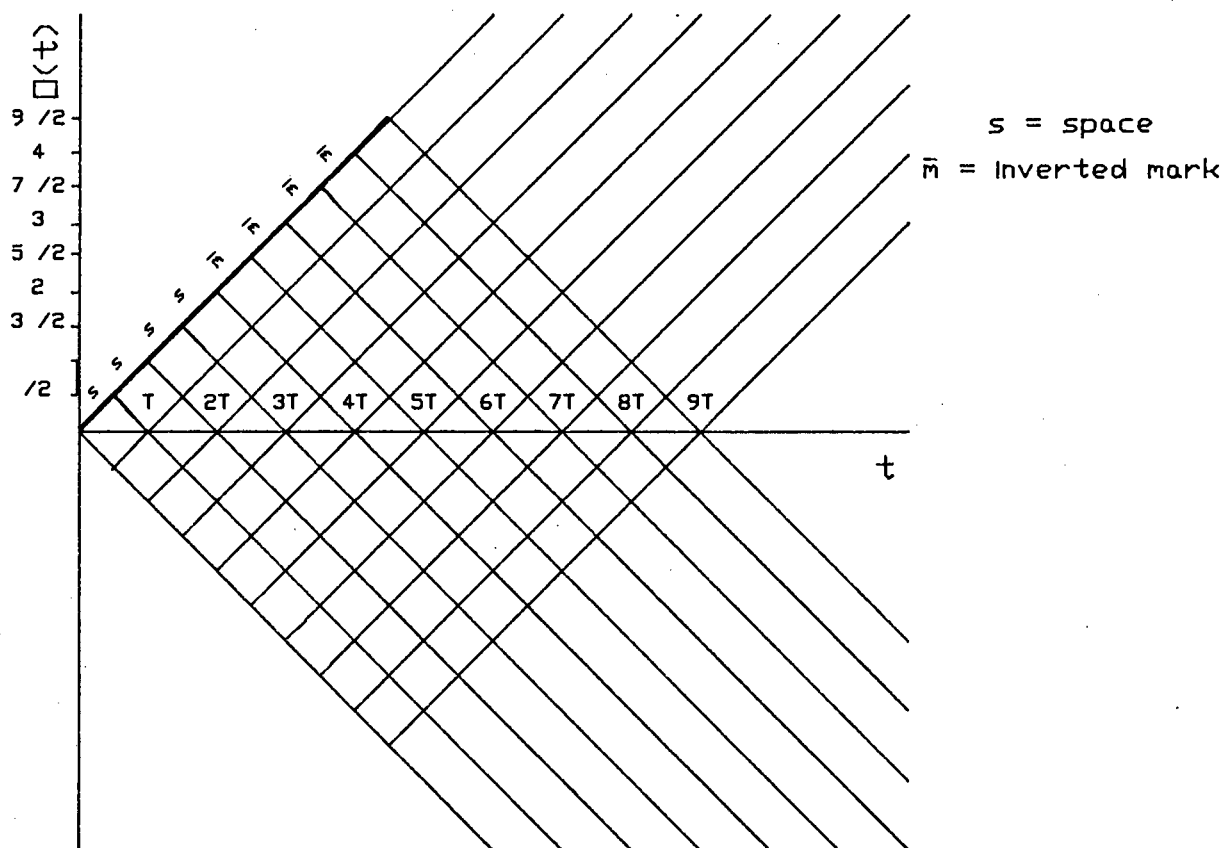


Fig. A.4 BIT SEQUENCE PRODUCING A STRING OF LENGTH > 4

Intuitively it is obvious that the operation has the important effect of reducing $|M-S|_{MAX}$. However, in order to calculate a limit for the permissible error in

modulation index dh to avoid bit errors, an indication of the actual value of $|M-S|_{MAX}$ is required.

Examining the probability distribution function (PDF) of the value of a given 4-bit "packet": (4 bits means 16 possible values)

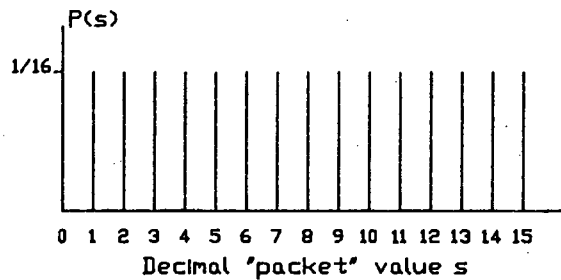


Fig. A.5 PDF OF THE DECIMAL VALUE OF A 4-BIT "PACKET"

$$P(0) = P(1) = P(2) = P(3) = \dots = 1/16$$

Considering the worst case (as shown in Fig. A.4):

$$P(8\text{-bit string}) = P(0 \text{ then } 15) + P(15, 0) = 2 \cdot 1/16 \cdot 1/16 = 2/256$$

$$P(12 \text{ " " }) = P(0, 15, 0) + P(15, 0, 15) = 2 \cdot 1/16^3$$

$$P(24 \text{ " " }) = 1,1 \cdot 10^{-7}$$

$$P(28 \text{ " " }) = 7,5 \cdot 10^{-9}$$

Clearly there is no $|M-S|_{MAX}$, however the probability of a 28-bit string (i.e. $|M-S|=28$) is \ll the required BER.

It is therefore necessary to ensure that $dh \leq 1/2 \cdot 28$ (see eqn. A.10). That is, $dh_{MAX} = 0,018$

h must therefore be controlled to within $0,018/0,5 = 3,6\%$ of it's nominal value, or:

$$0,482 \leq h \leq 0,518$$

NOTE

This analysis assumes that once \emptyset has exceeded $\pi/2$ radians and produced a bit error, it's value is reset to zero. Although this obviously doesn't happen in practice, it is a simple way of representing the possible reduction

of phase error caused by the compensating effect of shifts in the extracted carrier's phase. That is, shifts in the I-Q channel axis system orientation to align with the signal phase, effectively eliminating θ_e . It will later be shown how such shifts may occur, as well as how they can be dependent on both modulation index and bit-pattern.

A.1.2 Investigating the system's ability to recover once accumulative phase error has exceeded $\pi/2$ radians

The only conceivable ways in which the system may recover (i.e. reduce θ_e below the $\pi/2$ threshold level) are the following:

- (a) The polarity of (M-S) reverses for sufficiently long to diminish $|\theta_e| < \pi/2$.
- (b) The variation in the phase of the coherent carrier extracted at the receiver may have a compensating or "zeroing" effect on phase error. If this in fact occurs, since it is a continuous process it would erode θ_e constantly.

The influence of bit-pattern and modulation index on extracted carrier phase

Discontinuous FSK, as shown in Fig. A.6, is generated by switching to the output the signal from one of two free-running oscillators, under control of the input bit-pattern. If frequencies f_1 and f_2 are subsequently extracted from the FSK signal, the phase of these extracted carriers is totally independent of the bit-pattern used to produce the FSK signal.

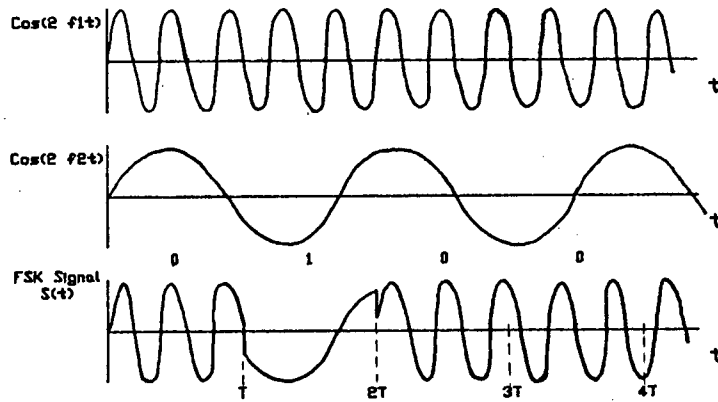


Fig. A.6 DISCONTINUOUS FSK

Continuous phase FSK, as shown in Fig. A.7 is generated by applying the input bit-pattern to the control-input of a VCO. Since the output waveform is continuous, the phase is continuous and the signal bandwidth is thus narrower than for the discontinuous case (as described in Chapter 1).

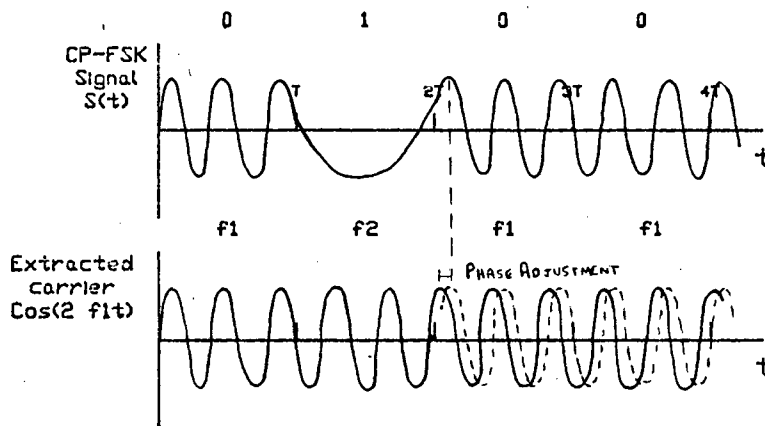


Fig. A.7 CONTINUOUS PHASE FSK (MOD. INDEX h_1)

Note that relative phase-shifts occur between one "burst" of the f_1 carrier and the next in the CP-FSK waveform (see Fig A.7). The same is also true for the f_2 carrier. This results from not permitting phase-discontinuities at bit-transition instants. Adjustments in the phase of the f_1 and f_2 components

are necessary to maintain continuous phase in the FSK signal. This inevitably causes phase changes in the f_1 and f_2 carriers extracted at the receiver. The phases of the extracted carriers are therefore modified in accordance with the bit pattern.

Now consider the above case for a different value of modulation index:

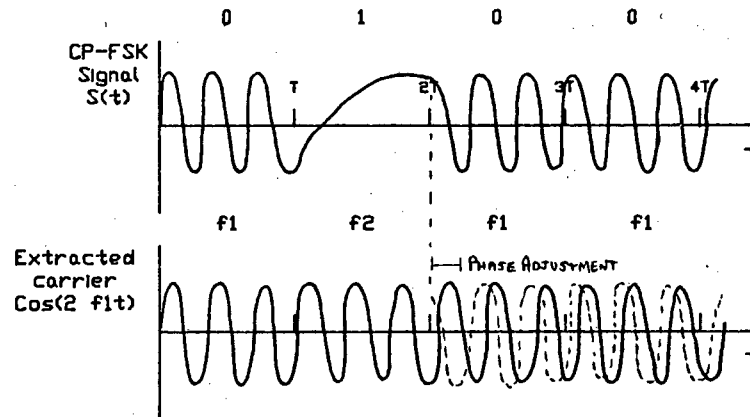


Fig. A.8 CP-FSK WITH MOD. INDEX $h_2 > h_1$

Note that the phase-shifts encountered by carriers f_1 and f_2 are different for a different value of modulation index.

It is important to note that the type of carrier phase-adjustment described above occurs at bit-transitions only. Cumulative phase-errors, on the other hand have been shown to occur for long strings of 1's or 0's. This diminishes the likelihood that this mechanism of phase adjustment would tend to diminish cumulative phase-errors. However, the possible existence of other compensating phase-shift phenomena in such a phase-coherent modulation scheme cannot be excluded. These may involve phase-shifts occurring during changes in mod. index etc.

APPENDIX B

DEVICE DATA SHEETS



**National
Semiconductor**

Voltage Comparators

LM161/LM261/LM361 High Speed Differential Comparators

General Description

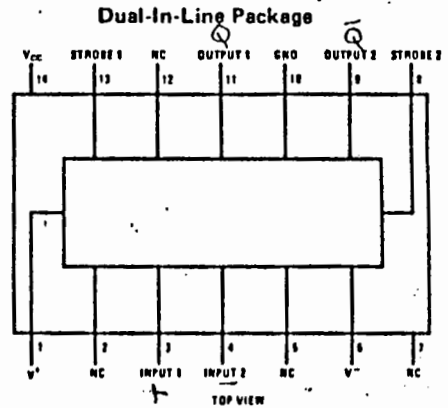
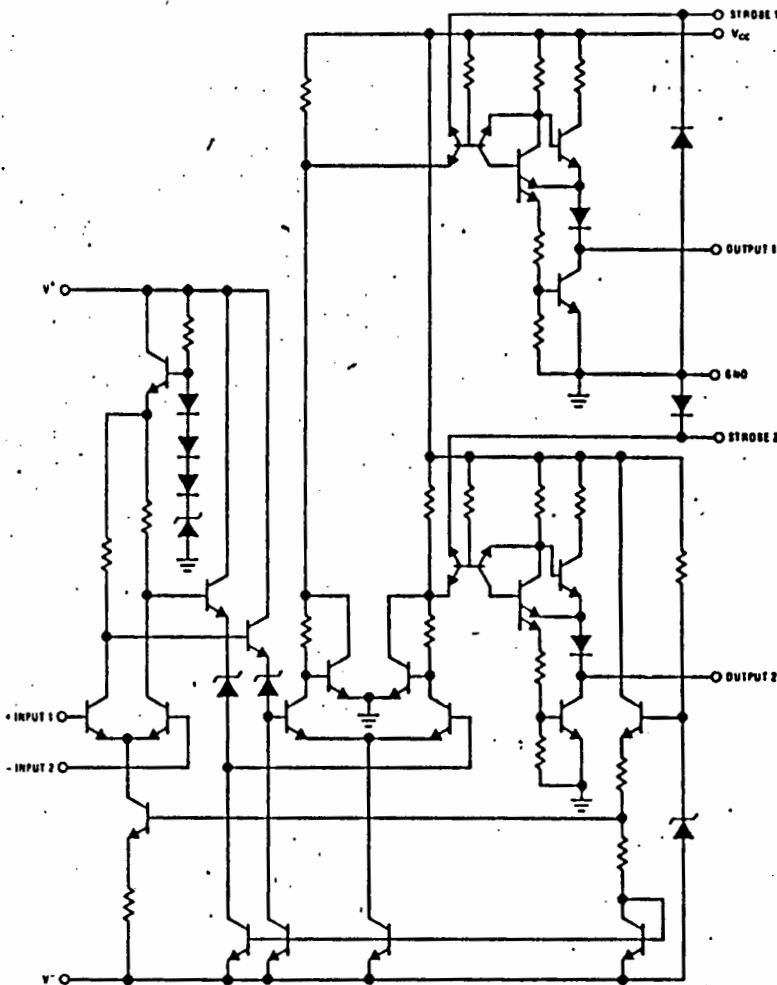
The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies ($\pm 15V$).

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disc file systems.

Features

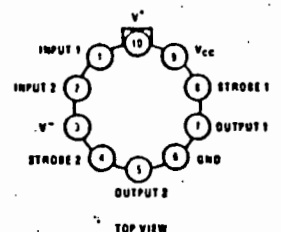
- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies $\pm 15V$
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Schematic and Connection Diagrams



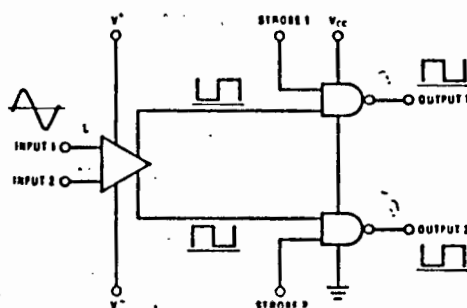
Order Number LM161J, LM261J
or LM361J
See NS Package J14A
Order Number LM361N
See NS Package N14A

Metal Can Package



Order Number LM161H, LM261H
or LM361H
See NS Package H10C

Logic Diagram



Absolute Maximum Ratings

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	-16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	-55°C to +125°C
LM261	-25°C to +85°C
LM361	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C
For Any Device Lead Below V^-	0.3V

Operating Conditions

	MIN	TYP	MAX
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	-6V		-15V
LM361	-6V		-15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM161/LM261			LM361			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25^\circ\text{C}$		5	20		10	30	μA
Input Offset Current	$T_A = 25^\circ\text{C}$		2	3		2	5	μA
Voltage Gain	$T_A = 25^\circ\text{C}$		3			3		V/mV
Input Resistance	$T_A = 25^\circ\text{C}$, $f = 1\text{ kHz}$		20			20		k Ω
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -5\text{ mA}$	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4\text{ mA}$.4			.4	V
Strobe Input "1" Current	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	μA
Strobe Input "0" Current	$V_{CC} = 5.25V$, $V_{STROBE} = .4V$			1.6			-1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$.8			.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	18		55	18		55	mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-65^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $55^\circ\text{C} < T_A < 125^\circ\text{C}$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0^\circ\text{C} < T_A \leq 70^\circ\text{C}$						20	mA
TRANSIENT RESPONSE		$V_{IN} = 50\text{ mV}$ Overdrive						
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25^\circ\text{C}$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25^\circ\text{C}$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25^\circ\text{C}$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25^\circ\text{C}$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25^\circ\text{C}$		8			8		ns

SL560C

300 MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300 MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL 560C is a general-purpose low noise, high frequency gain block.

FEATURES (Non-simultaneous)

- Gain up to 40 dB
- Noise Figure Less Than 2 dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range RF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

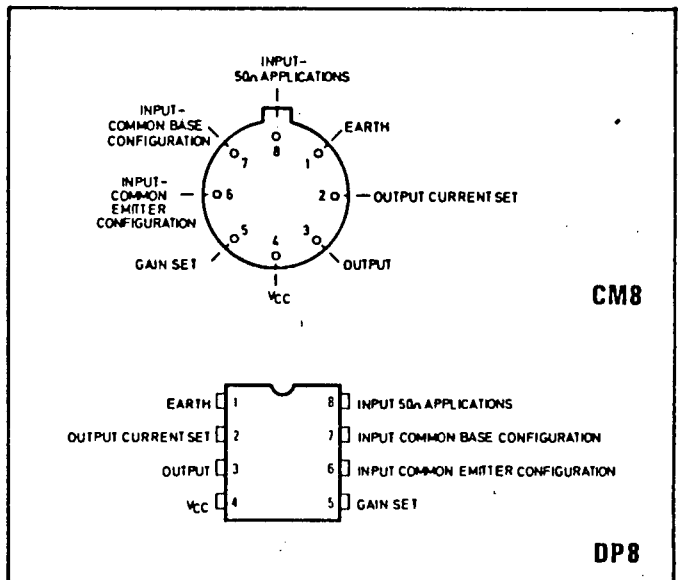


Fig. 1 Pin connections (viewed from beneath)

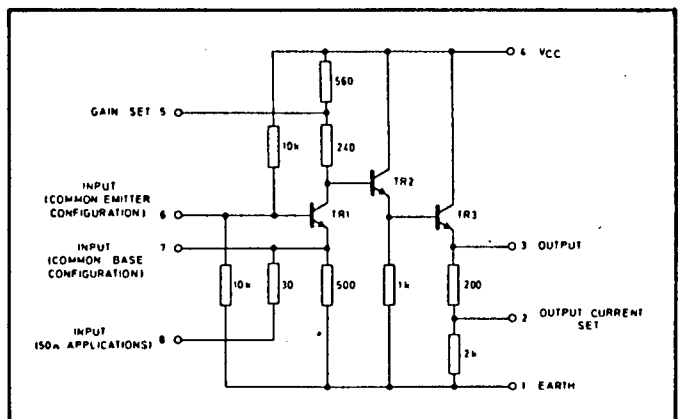


Fig. 2 SL560C circuit diagram

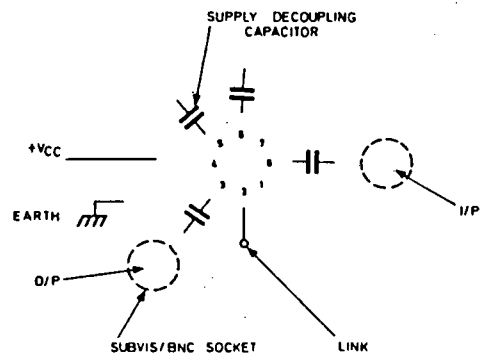
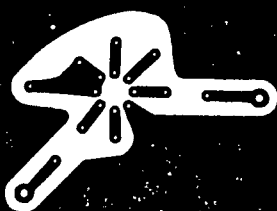


Fig. 3 PC layout for 50- Ω line driver (see Fig. 6)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

- Frequency 30 MHz
- Vcc 6V
- Rs = RL = 50Ω
- TA = 25°C
- Test Circuit: Fig. 6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	10 MHz — 220 MHz Vcc = 6V } See Fig. 5 Vcc = 9V } Rs = 200Ω Rs = 50Ω
Gain flatness		±1.5		dB	
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	
		+11		dBm	
Noise figure (common emitter)		1.8		dB	
		3.5		dB	
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance (Rbb') of 17 ohms (for low noise operation) with a small physical size — giving a transition frequency, fr, in excess of 1 GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2 dB noise figure (Rs = 200 Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75 MHz (see Figs. 8 and 9) or, using feedback, 14 dB with a bandwidth of 300 MHz (see Figs. 10 and 11).

Because the transistors used in the SL 560C exhibit a high value of fr, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is available in the Broadband Amplifier Applications' booklet.

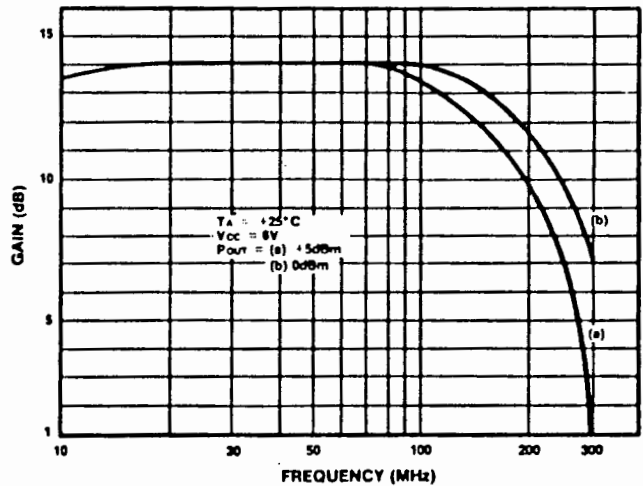


Fig. 4 Frequency response, small signal gain

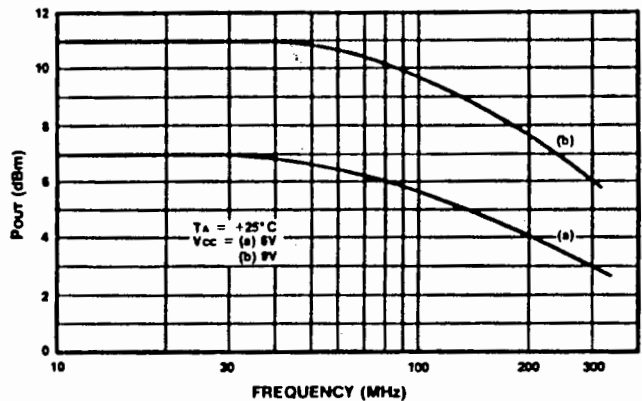


Fig. 5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression)

SL1613C

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613C is a bipolar monolithic integrated circuit wideband amplifier intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL1613C is typically 12dB.

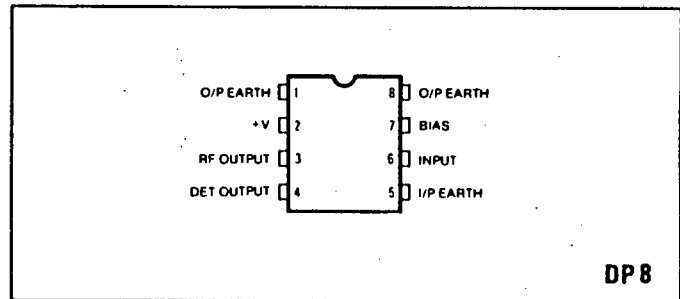


Fig. 1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	- 55°C to +125°C
Operating temperature range	- 30°C to +85°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB

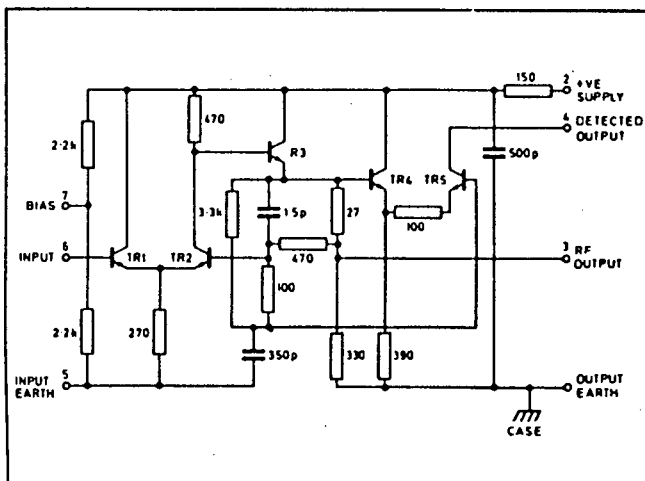


Fig. 2 Circuit diagram

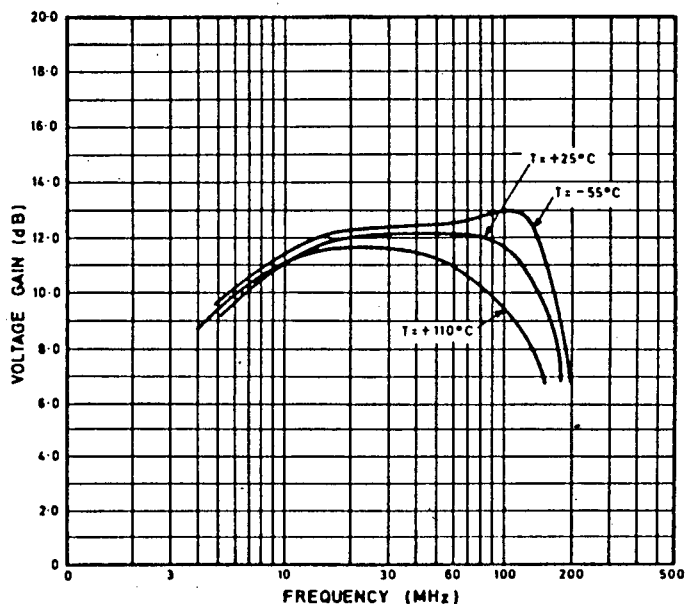


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
 $T_A = +22^\circ\text{C} \pm 2^\circ\text{C}$
 Supply voltage = +6V
 DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	$f=30\text{MHz}, R_s=10\Omega, C_L=8\text{pF}$ $R_s=10\Omega, C_L=8\text{pF}$ $R_s=10\Omega, C_L=8\text{pF}$
Upper cut-off frequency (Fig. 3)		150		MHz	
Lower cut-off frequency (Fig. 3)		5		MHz	
Propagation delay		2		ns	$f=60\text{MHz}, V_{in}=500\text{mV rms}$
Max. rectified video output current (Figs. 4 and 5)	0.8	1	1.3	mA	
Variation of gain with supply voltage		0.7		dB/V	See Note 1. $f=60\text{MHz}, R_s=450\Omega$
Variation of maximum rectified output current with supply voltage		25		%V	
Maximum input signal before overload		1.9		V rms	
Noise figure (Fig. 6)		4.5		dB	
Maximum RF output voltage		1.2		Vp-p	
Supply current		15	20	mA	

Note 1. Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction of TR1 on peak.

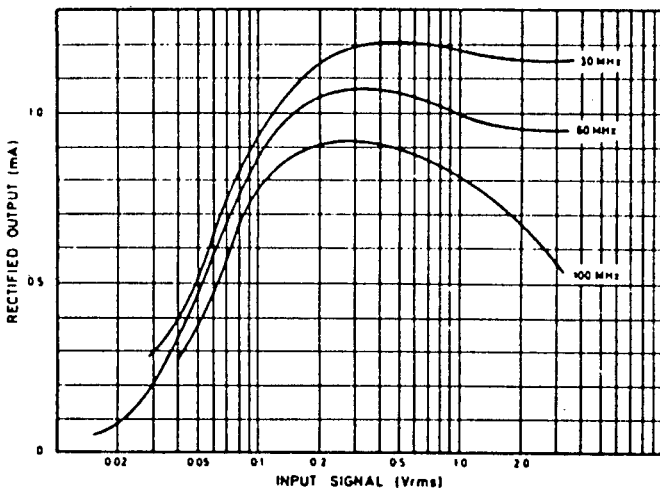


Fig. 4 Rectified output current v. input signal

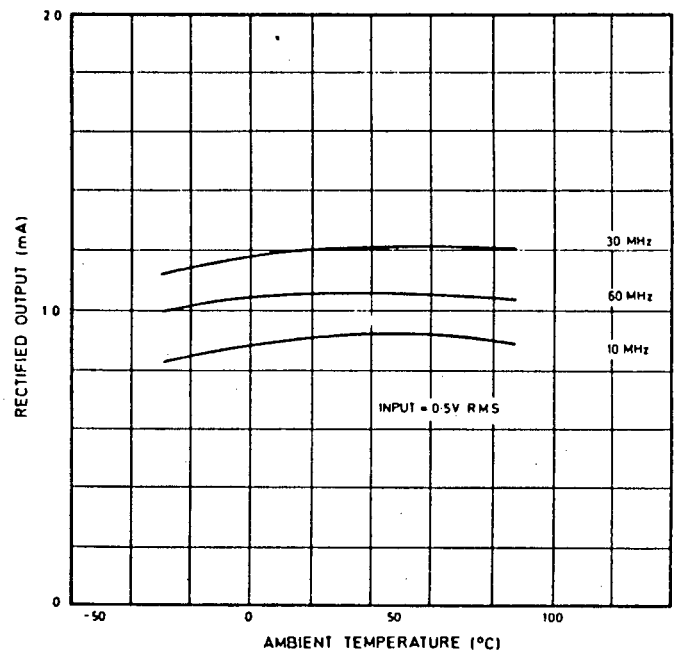


Fig. 5 Maximum rectified output current v. temperature

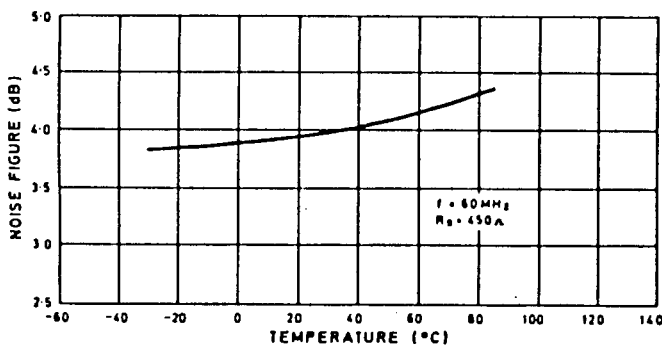


Fig. 6 Typical noise figure v. temperature

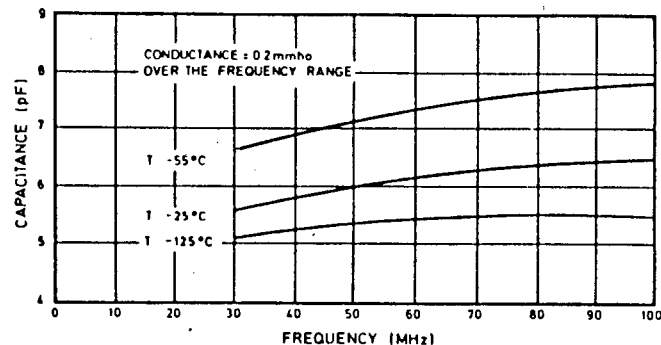


Fig. 7 Input admittance with open circuit output

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_p pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply V_{cc1} through a load.

The choice of V_{cc1} is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than V_{cc2} the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

- Minimum $V_{cc1} = (I_p \times R_L) + V_s + V_{cc2}$
- where I_p = programmed current
- R_L = DC load resistance
- V_s = max signal swing at output
- if the signal swing is not known:
- minimum $V_{cc1} = 2 (I_p \times R_L) + V_{cc2}$

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply (V_{cc2}) for the oscillator buffer (pin 4).

The current (I_p) programmed into pin 11 can be supplied via a resistor from V_{cc1} or from a current source.

The conversion gain is equal to

$$G_{dB} = 20 \text{ Log } \frac{R_L I_p}{56.6 I_p + 0.0785}$$
 for single-ended output

$$G_{dB} = 20 \text{ Log } \frac{2 R_L I_p}{55.6 I_p + 0.0785}$$
 for differential output

Device dissipation is calculated using the formula

- mW diss = $2 I_p V_O + V_p I_p + V_{cc2} \text{ Diss}$
- where V_O = voltage on pin 3 or pin 14
- V_p = voltage on pin 11
- I_p = programming current (mA)
- $V_{cc2} \text{ Diss}$ = dissipation obtained from graph (Fig.5)

As an example Fig. 7 shows typical dissipations assuming V_{cc1} and V_O are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig. 4 shows the intermodulation performance against I_p . The curves are independent of V_{cc1} and V_{cc2} but if V_{cc1} becomes too low the output signal swing cannot be accommodated, and if V_{cc2} becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

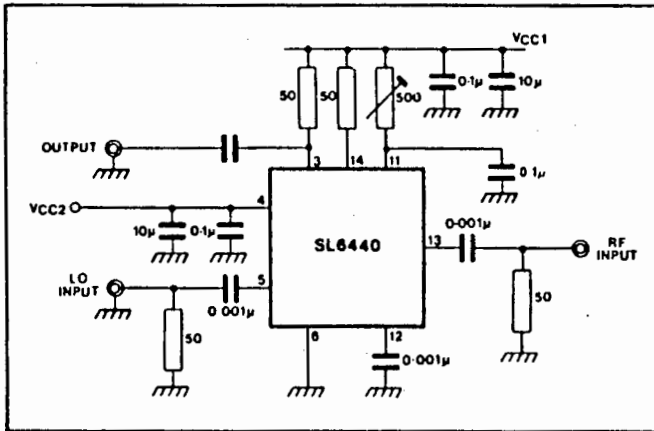


Fig.2 Typical application and test circuit

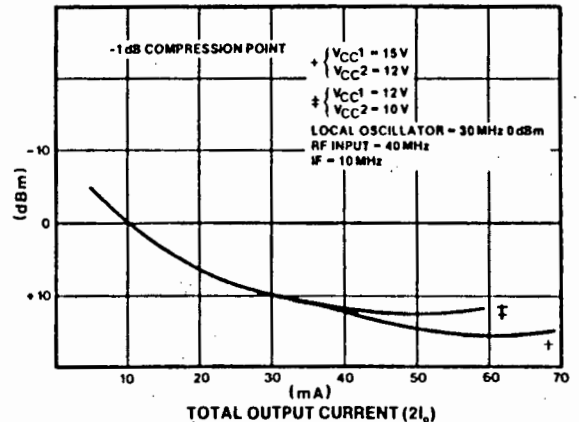


Fig.3 Compression point v. total output current

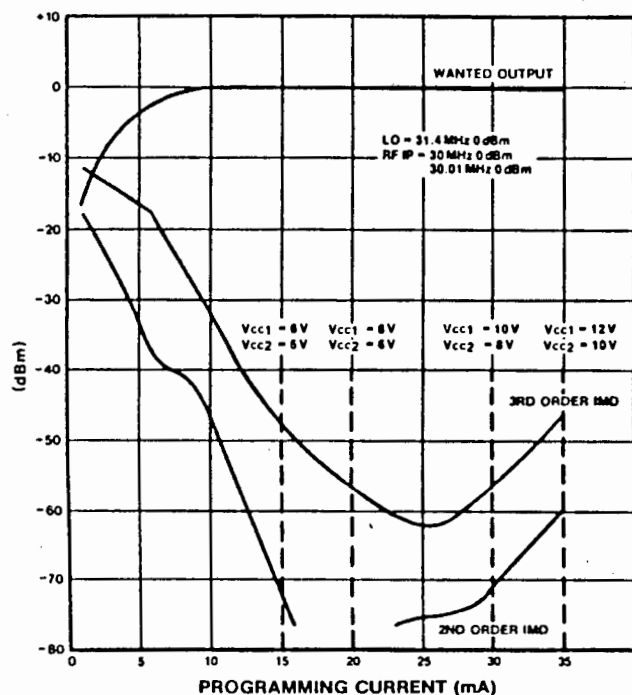


Fig.4 Intermodulation v. programming current

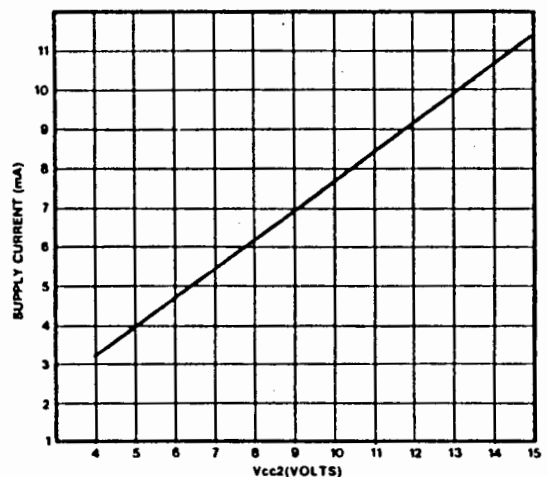
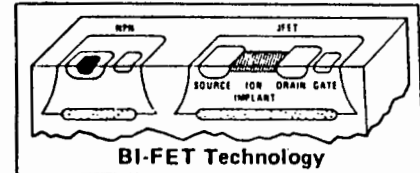


Fig.5 Supply current v. V_{cc2} ($I_p = 0$)

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11.



LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B Low Supply Current

LF156, LF156A, LF256, LF356, LF356A, LF356B Wide Band

LF157, LF157A, LF257, LF357, LF357A, LF357B Wide Band Decompensated ($A_{V_{MIN}} = 5$)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slow rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low $1/f$ noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low $1/f$ corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

- Photocell amplifiers
- Sample and Hold circuits

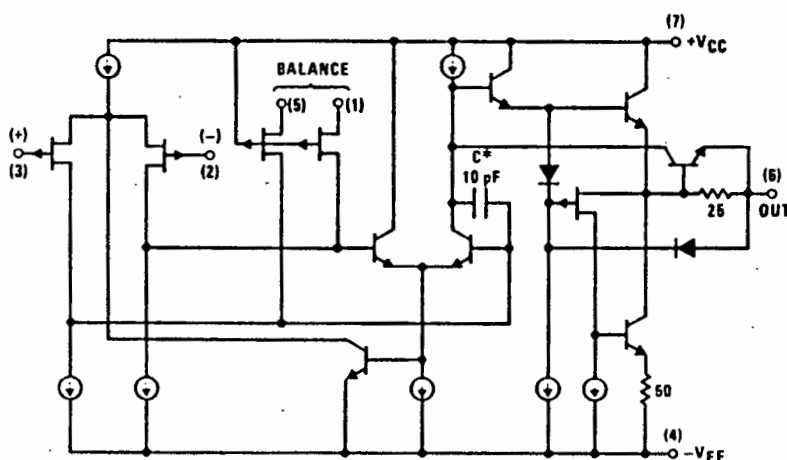
Common Features (LF155A, LF156A, LF157A)

- Low input bias current 30 pA
- Low Input Offset Current 3 pA
- High input impedance $10^{12}\Omega$
- Low input offset voltage 1 mV
- Low input offset voltage temperature drift $3\mu V/^\circ C$
- Low input noise current 0.01 pA/ \sqrt{Hz}
- High common-mode rejection ratio 100 dB
- Large dc voltage gain 106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	UNITS
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/ μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/ \sqrt{Hz}

Simplified Schematic



*C = 2 pF on LF157

Absolute Maximum Ratings

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B	LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (P _D at 25°C)				
Lead Thermal Resistance (θ _{J-A}) (Note 1)				
T _J MAX				
(H Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P _D	670 mW	670 mW	670 mW	670 mW
θ _{J-A}	150°C/W	150°C/W	150°C/W	150°C/W
(N Package) P _D			500 mW	500 mW
θ _{J-A}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	R _S = 50Ω, T _A = 25°C		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
ΔV _{OS} /ΔT	Average TC of Input Offset Voltage	R _S = 50Ω		3	5		3	5	μV/°C
ΔTC/ΔV _{OS}	Change in Average TC with V _{OS} Adjust	R _S = 50Ω, (Note 4)		0.5			0.5		μV/°C per mV
I _{OS}	Input Offset Current	T _J = 25°C, (Notes 3, 5)		3	10		3	10	pA
		T _J ≤ T _{HIGH}			10		1		nA
I _B	Input Bias Current	T _J = 25°C, (Notes 3, 5)		30	50		30	50	pA
		T _J ≤ T _{HIGH}			25		5		nA
R _{IN}	Input Resistance	T _J = 25°C		10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S = ±15V, T _A = 25°C	50	200		50	200		V/mV
		V _O = ±10V, R _L = 2k							
		Over Temperature	25			25			V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10k	±12	±13		±12	±13		V
		V _S = ±15V, R _L = 2k	±10	±12		±10	±12		V
V _{CM}	Input Common-Mode Voltage Range	V _S = ±15V	±11	+15.1		±11	+15.1		V
				-12			-12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics T_A = 25°C, V_S = ±15V

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A; A _V = 1, LF157A; A _V = 5	3	5		10	12		40	50		V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t _s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e _n	Equivalent Input Noise Voltage	R _S = 100Ω										nV/√Hz
		f = 100 Hz		25			15			15		nV/√Hz
		f = 1000 Hz		25			12			12		nV/√Hz
i _n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		pA/√Hz
		f = 1000 Hz		0.01			0.01			0.01		pA/√Hz

SL541B

HIGH SLEW RATE OPERATIONAL AMPLIFIERS

The SL541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of $\pm 5\text{mV}$ maximum and replaces the SL541C.

The SL541B is tested in two circuit applications (A and B).

FEATURES

- High Slew Rate: $175\text{V}/\mu\text{s}$
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B)
- Wide Bandwidth: DC to 100MHz at 10dB Gain
- Very Low Thermal Drift: $0.02\text{dB}/^\circ\text{C}$ Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum
- Full Military Temperature Range (DIL Only)
- Package: 10 Lead TO-5
14 Lead DIL Ceramic

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V+$ to $V-$)	24V
Input voltage (Inv. I/P to non inv. I/P)	$\pm 9\text{V}$
Storage temperature	-55°C to $+175^\circ\text{C}$
Chip operating temperature	$+175^\circ\text{C}$
Operating temperature:	TO-5: -55°C to $+85^\circ\text{C}$ DIL: -55°C to $+125^\circ\text{C}$

Thermal resistances

Chip-to-ambient: TO-5	220 $^\circ\text{C}/\text{W}$
DIL	125 $^\circ\text{C}/\text{W}$
Chip-to-case: TO-5	60 $^\circ\text{C}/\text{W}$
DIL	40 $^\circ\text{C}/\text{W}$

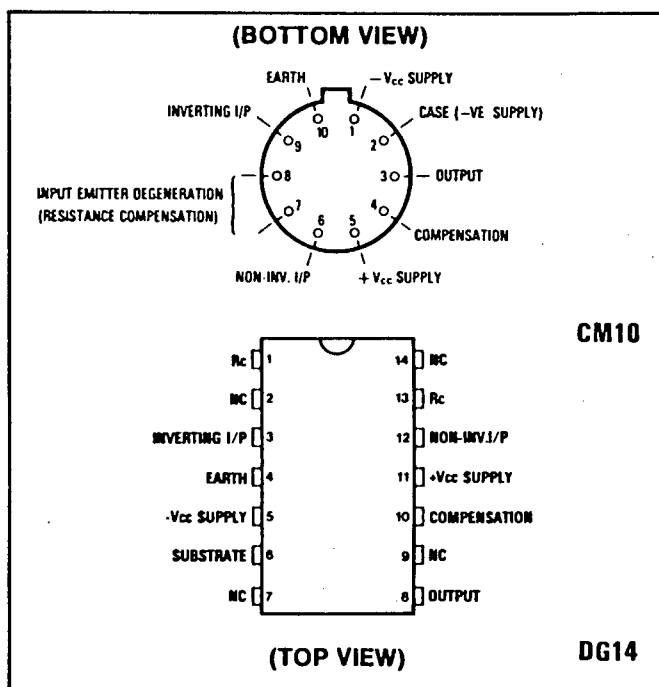


Fig. 1 Pin connections

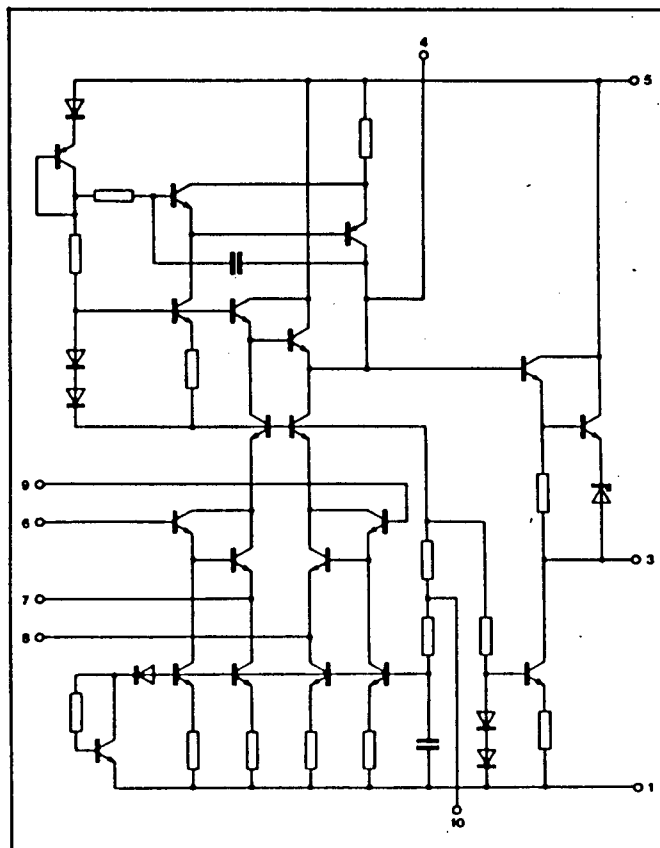


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = 25^{\circ}C$

$R_c = 0\Omega$

Test circuits: see Fig.8

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	μA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600 Ω load
	B	60	71		dB	
Open loop temperature coefficient	A,B		-0.02		dB/ $^{\circ}C$	
Closed loop bandwidth (-3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/ μs	X10 gain
Settling time to 1 %	A,B		50	100	ns	
Maximum output voltage	A	5.5	5.7		V	
			-1.9	-1.5	V	
	B	2.5	3.0	V		
		-3.0	-2.5	V		
Maximum output current	A,B	4	6.5		mA	
	Maximum input voltage	A		5	V	Non-inverting modes
-1				V		
B		3	V			
		-3	V			
Supply line rejection	A,B	54	66		dB	
			46	54	dB	
			9.85	μA		
Input offset current	A,B				dB	
Common mode rejection	A,B	60.7			dB	
Input offset voltage drift	A		25		$\mu V/^{\circ}C$	

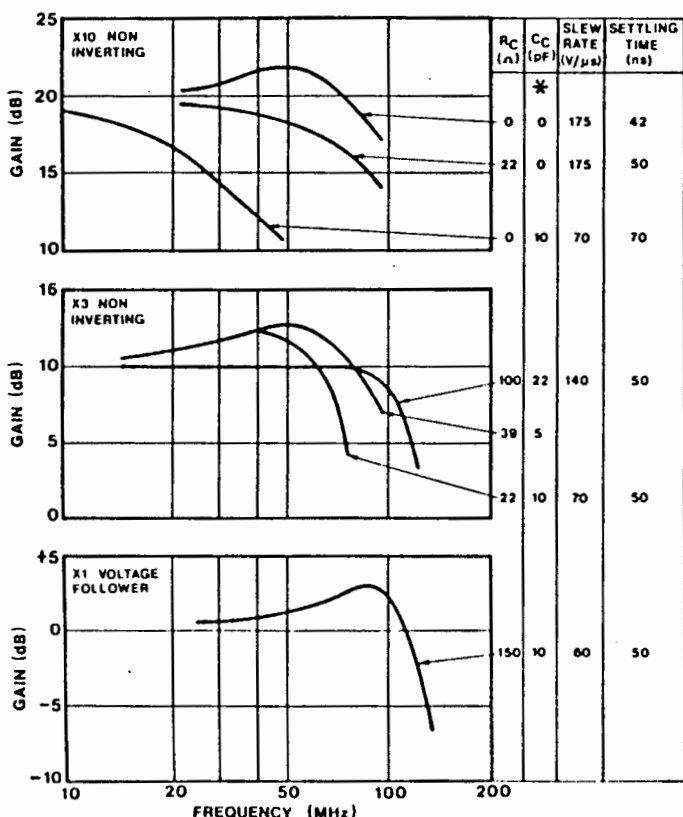


Fig. 3 Performance graphs – gain v. frequency (load = 2k Ω /10pF) * See operating note 2

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (<1k Ω), as seen from pins 6 and 9 – 100 Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ± 0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit (circuit B only).

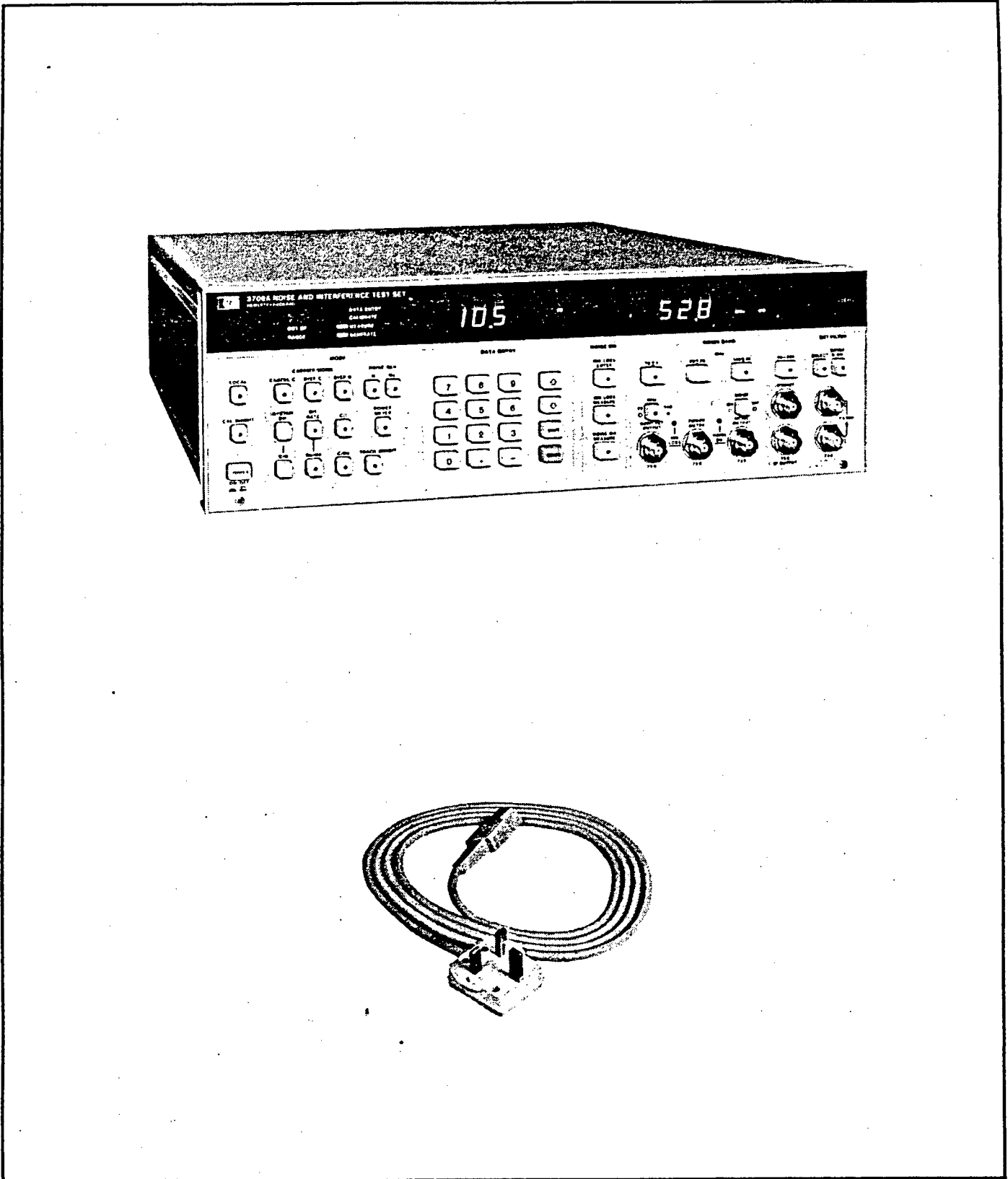


Figure 1-1 HP Model 3708A Noise and Interference Test Set

Table 1-1 Specifications

Except where otherwise indicated, the following parameters are warranted performance specifications. Parameters described as "typical" or "nominal" are supplemental characteristics which provide a useful indication of typical, but non-warranted performance characteristics. All specifications are guaranteed over an ambient temperature of 0° to 55°C, except where otherwise stated.

NOISE GENERATION

Band-limited white noise, available as "noise only" (Noise Output connector) or as "noise + carrier" (IF Output connector).

Level range of noise

At Noise Output connector (max output 6 dB lower at IF Output).

+6 to -80 dBm (filter-dependent, see table below);
-70 dBm/Hz (filter-dependent, see table below) to -154 dBm/Hz.

Absolute accuracy of noise power

(Noise Output connector)

After calibration of power meter with the 0 dBm reference tone (70 or 140 MHz).

± 0.25 dB in range +6 to -10 dBm output power at 23 ± 3°C;

± 0.5 dB in range +6 to -55 dBm output power.

Band-limiting filters

The noise bandwidth of each instrument filter set is individually measured and stored in non-volatile memory.

Values given below are typical and individual instruments will show different values on the front panel display.

Noise bandwidth accuracy: ± 0.15 dB ± 2.5%.

Frequency Bands (MHz)	Flatness (wrt centre frequency) (dB)	Noise Bandwidth* (MHz)	Typical Temperature Stability (dB/°C)	Max No* (dBm/Hz)	Min N* (dBm)
70 ± 5	± 0.3	18	0.001	-67	-81
70 ± 20	± 0.4	60	0.001	-72	-75
140 ± 40	± 0.5	125	0.001	-75	-73
10 to 200	± 0.8	215	0.0015	-78	-70

*Nominal values, will vary for individual instruments.

Crest factor

Typically ≥ 15 dB.

C/N power ratio (IF Output connector)

Range: -10 to 60 dB.

Accuracy:

Over range C = +1 to -5 dBm, C/N = 10 to 30 dB, 23 ± 3°C.

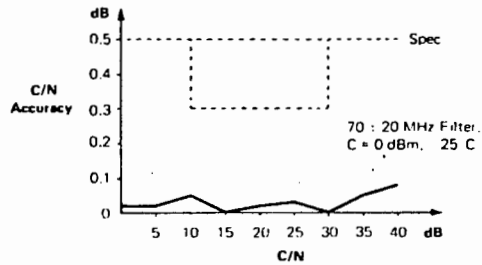
± 0.3 dB for 70 ± 20 MHz filter;

± 0.35 dB for 140 ± 40 MHz filter.

Over range C = +5 to -40 dBm, N = 0 to -45 dBm, C/N = 0 to 40 dB.

± 0.5 dB for all filters.

Typical results as shown in graph below.



Response time (tracking speed)

Typically 10 ms for a carrier power change ≤ ± 5 dB.

INTERFERENCE SIGNAL INPUTS

The HP 3708A offers two distinct facilities for interference tests. Both are broadband inputs, with a frequency range of 10 to 200 MHz.

AUXILIARY INTERFERER INPUT (rear panel)

Provides a fixed-loss path to the IF Output (but not to the Noise Output).

Flatness

70 ± 20 MHz: ± 0.2 dB with respect to 70 MHz.

140 ± 40 MHz: ± 0.6 dB with respect to 140 MHz.

Loss to IF Output

Typically 15 dB.

INTERFERER (I) INPUT (front panel, common to Ext Filter Input)

Valid interferer input power

-30 dBm typical (indicated by 1 Level lamps on front panel).

Table 1-1 Specifications (continued)

C/I power ratio

Range: -10 to 60 dB.

Accuracy:

Over range C = +1 to -5 dBm, C/I = 10 to 30 dB, $23 \pm 3^\circ\text{C}$.

± 0.3 dB for 70 \pm 10 MHz interferer;

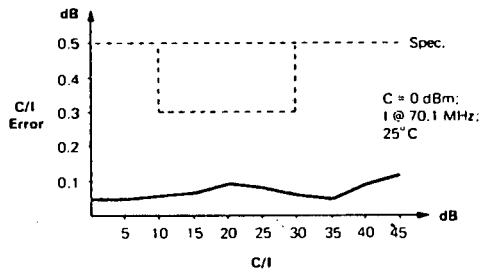
± 0.35 dB for 140 \pm 10 MHz interferer.

Over range C = +5 to -40 dBm, I = 0 to -45 dBm, C/I = 0 to 40 dB.

± 0.5 dB for interferer tone 70 \pm 20 MHz;

± 0.6 dB for interferer tone 140 \pm 40 MHz.

Typical results as shown in graph below

**Flatness of interference path**

70 \pm 5 MHz: ± 0.1 dB with respect to 70 MHz.

70 \pm 20 MHz: ± 0.4 dB with respect to 70 MHz.

140 \pm 40 MHz: ± 0.4 dB with respect to 140 MHz

10 to 200 MHz: 1 dB pk-pk

Response time

Typically 10 ms for a carrier power change ± 5 dB.

CARRIER PATH

The carrier path is specified from IF Input to IF Output.

Gain (at 70 MHz)

0 ± 0.4 dB (typically 0 ± 0.1 dB).

Flatness

70 \pm 20 MHz: ± 0.2 dB with respect to 70 MHz (typically ± 0.1 dB).

140 \pm 40 MHz: ± 0.3 dB with respect to 140 MHz (typically ± 0.1 dB).

Group delay

0.2 ns for ranges 70 \pm 20 MHz, 140 \pm 40 MHz.

3rd order intercept point

Typically +29 dBm.

POWER MEASUREMENT

Specifications apply to Power Meter input only.

Measurement range

+6 to -55 dBm.

Absolute Accuracy

± 0.3 dB at 0 dBm, 70 MHz;

(± 0.15 dB at 0 dBm, $23 \pm 3^\circ\text{C}$, 70/140 MHz after calibration using reference tone - see below).

Flatness

10 to 180 MHz: ± 0.3 dB with respect to 70 MHz.

Resolution

0.01 dB.

Linearity

Measured at 70 MHz.

+5 to -35 dBm: ± 0.1 dB (typically ± 0.05 dB).

-35 to -45 dBm: ± 0.3 dB.

REFERENCE TONE OUTPUT**Frequency**

70/140 MHz crystal-controlled oscillator, front-panel selectable. Other frequencies available on special order.

Level

0 dBm ± 0.15 dB.

Factory-set to 0 dBm ± 0.05 dB at $23 \pm 3^\circ\text{C}$.

Harmonic content

< -25 dBc.

INSERTION LOSS MEASUREMENT**Accuracy**

± 0.2 dB at 70 or 140 MHz.

Range

-5 to 35 dB.

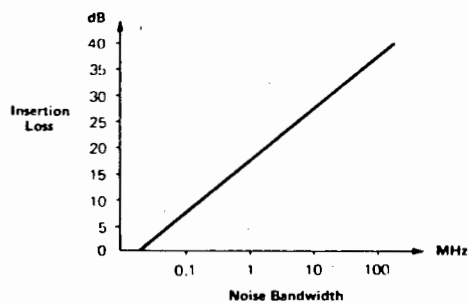
Table 1-1 Specifications (continued)

NOISE BANDWIDTH MEASUREMENT**Accuracy**

$\pm 0.4 \text{ dB} \pm 10\%$ (includes insertion loss measurement accuracy of $\pm 0.2 \text{ dB}$).

Range

Function of insertion loss and filter bandwidth, see graph below.

**HP-IB FACILITIES****Mode**

Addressable; factory-preset address 8, selected by rear-panel switch.

Load

One bus load.

Local switch

Allows switching from remote to local control, except when controller has issued a local lockout command.

Interface functions subset

SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT1, C0.

GENERAL**Connectors**

All signal connectors in the HP 3708A are BNC type and

have a return loss $> 26 \text{ dB}$ (except the rear-panel Aux Interferer input, with a return loss of 18 dB , typically).

Power supply

Input voltages: 100/120/220/240V ac.

Tolerance: $+5$ to -10% .

Frequency: 48 to 66 Hz.

Power consumption: 150VA max.

Dimensions (including connectors and feet)

145mm (5.75 in) high; 425 mm (16.75 in) wide; 540 mm (21.2 in) deep.

Weight

16 kg (35 lb), net; 29 kg (63 lb), shipping.

Environment

0° to 55°C operating; -40° to 75°C , storage.

Options

In the HP 3708A standard instrument, all signal connectors impedances are 75Ω nominal, unbal to gnd. Reference tone oscillator frequency is 70/140 MHz, selectable from the front panel. Reference tone oscillator frequencies other than the standard values are available on a special order basis.

001: CONNECTORS: all signal connectors impedances

are 50Ω nominal, unbal to gnd.

801: PROTECTIVE FRONT COVER.

907: FRONT HANDLE KIT: adds front handles to the HP 3708A. Options 801 and 907 cannot be fitted at the same time.

908: RACK FLANGE KIT: enables the HP 3708A to be secured in a 483 mm (19 in) rack.

909: RACK AND HANDLE KIT: combination of Options 907 and 908.

910: EXTRA SET OF MANUALS.

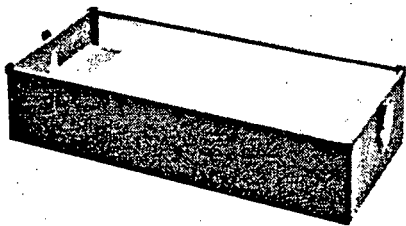
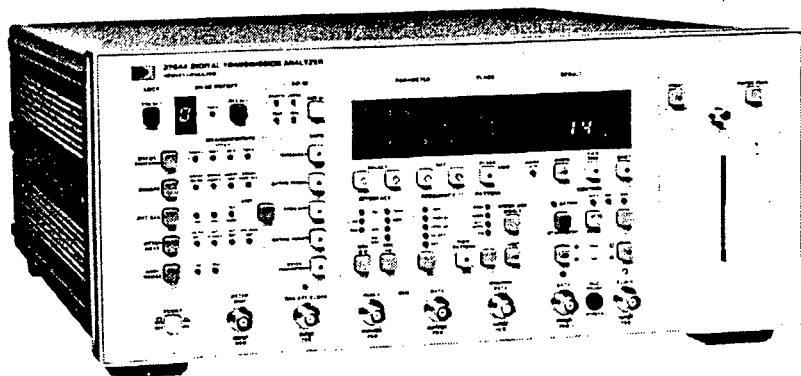


Figure 1-1 Model 3764A and Accessories supplied

Table 1-1 SPECIFICATIONS

Except where otherwise indicated the following parameters are warranted performance specifications. Parameters described as 'typical' or 'nominal' are supplemental characteristics which provide a useful indication of typical, but non-warranted, performance characteristics.

GENERATOR SECTION

Data Outputs

CODED

Format: Coded Mark Inversion (CMI).

Rate: 139.264 Mbit/s.

Impedance: nominal 75Ω unbalanced to GND.

Levels: + and $-0.5V \pm 10\%$.

Transition Times: < 2 ns into 75Ω .

Transition Tolerance (139.264 MHz internal clock):

negative transitions ± 100 ps;

coincident positive transitions ± 500 ps;

mid-period positive transitions ± 350 ps.

Overshoot/Preshoot: $< 5\%$ of pulse amplitude.

Protection: open/short circuit protected, maximum voltage $\pm 6V$ short term.

BINARY

Format: binary RZ or NRZ.

Rate: 1 kbit/s to 170 Mbit/s.

Impedance: nominal 75Ω unbalanced to $-2V$.

Amplitude: nominal ECL levels.

RZ duty cycle: nominally 50% on internal clock.

NRZ Width: $100\% \pm 5\%$.

Transition times: < 1.8 ns.

Transition timing tolerance: 0.5% of period + 350 ps.

Overshoot/Preshoot: $< 10\%$ pulse amplitude.

Clock Source

INTERNAL

Frequency: 139.264 MHz.

Accuracy: setting tolerance at ambient temperature is better than ± 3 ppm.

Temperature Stability: typically $< \pm 12$ ppm ($0^\circ C$ to $+55^\circ C$).

Ageing: typically $< \pm 5$ ppm per year.

OFFSET

Frequency: 139.264 MHz + 15 ppm and 139.264 MHz -15 ppm.

Other parameters: as for Internal Clock Source.

EXTERNAL

Frequency: 1 kHz to 170 MHz.

Impedance: nominal 75Ω to GND (selectable by internal link to $-2V$).

Triggering: nominal GND, nominal ECL or TTL thresholds selectable by internal link.

Amplitude: maximum 3V pk-pk.

Sensitivity: better than 300 mV at 170 MHz.

Clock Output

Format: squarewave, $50\% \pm 10\%$ duty cycle on internal clock.

Impedance: low, unbalanced.

Amplitude: nominal ECL levels.

Jitter (Jitter Generator off): $< 0.5\%$ period +50 ps pk-pk (e.g. < 0.005 UI pk-pk at 1 kHz; < 0.0135 UI pk-pk at 170 MHz).

External Load: 75Ω to $-2V$, dc coupled; 75Ω to GND, ac coupled.

Generator Clock Monitor Output (Rear Panel)

Source: internal or external clock.

Format: when the jitter generator is used this clock output will not be jittered by it.

Impedance: low, unbalanced to GND.

Amplitude: nominal ECL levels.

External Load: 75Ω to $-2V$, dc coupled; 75Ω to GND, ac coupled.

Patterns

PRBS: $2^{23}-1$. Polynomial is $D(23) + D(18) + 1 = 0$. Inverted sequence 23 zeros.

Word: variable length from 1 to 16 bits.

Alternating Word: external signal controls output of two half length words, changeover is synchronous with the end of a word. The half length word can be varied in length from 1 bit to 8 bits.

AIS: continuous "all ones" pattern.

Error Add (Binary Errors)

Fixed: average error ratio of 1 error in 1000 clock periods ($1 \cdot 10^{-3}$).

Flexible: one error introduced for each press of the SINGLE ERROR ADD key.

Pattern Trigger Output (Rear Panel)

Format: one pulse per PRBS or Word pattern.

Position: fixed.

Width: two clock periods.

Impedance: nominal 50Ω unbalanced.

Amplitude: 1V pk minimum.

Protection: open/short circuit protected, maximum voltage $\pm 5V$ short term.

Alternating Word Control Input (Rear Panel)

Function: the frequency of the applied signal controls the changeover rate of the half length words in alternating word mode.

Impedance: nominal 1K Ω unbalanced.

Maximum Input: 5V rms.

Sensitivity: 250 mV pk-pk squarewave dc to 100 kHz; 500 mV pk-pk sine or triangular wave 200 Hz to 100 kHz.

RECEIVER SECTION

Data Inputs

CODED (TERMINATED MODE)

Format: Coded Mark Inversion (CMI).

Impedance: nominal 75 Ω unbalanced to GND.

Rate: 139.264 Mbit/s \pm 3 Mbit/s.

Amplitude: nominal maximum pk-pk voltage into 75 Ω is 1V.

Jitter Tolerance: better than 10 UI pk-pk up to 100 kHz;
better than 0.5 UI pk-pk at 2 MHz.

Equalization: automatic equalization for cable loss of up to 12 dB at half bit-rate.

Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.

CODED (MONITOR MODE)

Additional Gain: an additional gain of 26 dB is available to allow for flat loss at equipment monitor points.

Other Parameters: as for Terminated Mode.

BINARY

Rate: 1 kbit/s to 170 Mbit/s.

Format: binary RZ or NRZ.

Impedance: nominal 75 Ω unbalanced to -2V.

Amplitude: nominal ECL levels.

Data Polarity: Data or $\overline{\text{Data}}$ switched at the binary level.

EXTERNAL ERROR

Parameters: as for Binary Data Input.

Clock Format: an external clock must be supplied, parameters as for Binary Clock Input.

Format: minimum pulse width 3 ns.

Clock Source

RECOVERED

Rate: 139.264 Mbit/s \pm 3 Mbit/s.

BINARY

Rate: 1 kHz to 170 MHz.

Impedance: nominal 75 Ω unbalanced to -2V.

Amplitude: nominal ECL levels.

Polarity: Clock or $\overline{\text{Clock}}$.

Receiver Clock Output (Rear Panel)

Impedance: low, unbalanced.

Amplitude: nominal ECL levels.

External load: 50 Ω to -2V dc coupled, or 50 Ω to GND ac coupled.

Synchronisation

Modes: automatic, manual or external.

AUTOMATIC (for bit-rates > 500 kbit/s)

Sync. Loss: greater than 10,000 errors in 90,000 clock periods.

Sync. Gain: less than 10 errors in 90 clock periods.

MANUAL

Operation: pressing the MANUAL SYNC. key will initiate a resync.

EXTERNAL SYNC. INPUT (REAR PANEL)

Operation: a "high" level on the input signal initiates a resync.

Format: nominal ECL levels.

Impedance: nominal 50 Ω unbalanced to -2V.

Pulse Width: minimum 20 ns.

Receiver Pattern Trigger Output (Rear Panel)

Format: one pulse per PRBS or Word pattern.

Position: Fixed.

Width: two clock periods.

Impedance: nominal 50 Ω unbalanced to GND.

Amplitude: 1V pk minimum.

Protection: open/short circuit protected, maximum voltage \pm 5V short term.

Error Output (Rear Panel)

Format: one edge per error. When a data loss is detected the error output port will give a continuous stream of errors. When a sync.loss is detected the output port will give an output equivalent to every other bit in error.

Impedance: nominal 50 Ω to GND, unbalanced.

Amplitude: minimum 1V pk-pk about GND.

Protection: open/short circuit protected, maximum voltage \pm 5V short term.

Auxiliary Inputs

ANALOG (1 OFF)

Format: voltage range 0 to +14.0V.

Resolution: 100 mV.

Impedance: nominal 1 M Ω .

DIGITAL (7 OFF)

Format: 3 are nominal ECL levels. Impedance 50 Ω to -2V.
4 are nominal TTL levels.

ERROR ANALYZER SECTION

Measurement Mode: the instrument will measure errors from two sources. These will be either binary errors, resulting from a bit-by-bit comparison of the received data with the internal reference pattern, or errors detected by external equipment, and input to the 3764A in the form of one pulse per error.

GATING PERIOD

Timed: a repetitive timed interval can be set in steps of 1s. (Minimum interval 1s, maximum interval approximately 100 days.) The intervals are contiguous with no 'dead-time' between them.

Manual: START/STOP key is used to control the length of the gating period.

Single: the range of the single shot gating period is in 1s increments from 1s to approximately 100 days.

Measurements

ERROR RATIO

Method: calculates the ratio of counted errors to the number of clocks in the selected gating period.

Display: of the form $X.Y \times 10^{-N}$ where N is in the range 1 to 15. If the result is based on < 100 errors the display is truncated to $X \times 10^{-N}$.

ERROR COUNT

Method: totalizes errors over the selected gating period.

Display: individual counts displayed to 99,999 then display changes to $X.Y \times 10^N$. N is ≥ 1 (Integers).

ERROR SECONDS

Method: counts the number of seconds in the gating period which contain at least one error.

Display: as for Error Count.

ERROR FREE SECONDS

Method: counts the number of seconds in the gating period which contain no errors.

Display: as for Error Count.

% AVAILABILITY

Method: repetitively calculates the system error ratio over 1s timed intervals during the overall gating period. The system is deemed to be 'unavailable' when the error ratio is greater than a preset threshold (Th) for at least 10 consecutive 1s timed intervals. The system becomes 'available' when the error ratio is less than this threshold for at least 10 consecutive 1s timed intervals.

Threshold (Th): selected over the range 10^{-1} to 10^{-6} .

%ER < N

Method: measures the error ratio over repetitive timed intervals (t), then calculates the % of the total gating period time (T) when the error ratio was less than the threshold value (N). Results are only accumulated when the system under test is deemed 'available'. During periods of system 'unavailability' the measurement counters freeze.

Measurement Period: the repetitive timed interval (t) may be selected for 1s or 60s.

Error Ratio Threshold (N): variable over the range 10^{-3} to 10^{-9} . The value of the threshold may be changed during or after a gating period without affecting the basic measurement. This allows a first approximation of the distribution of the error ratio results.

%EFS

Method: calculates the ratio of error free seconds to the total number of 'available' seconds in the gating period. During periods of system 'unavailability' the measurement counters freeze.

REAL TIME, PERPETUAL CLOCK

Function: gives the ability to display and record the following modes.

- (a) Local time : shows hours, minutes and seconds;
- (b) Date : shows day, month, year;
- (c) Elapsed time : shows time since the start of a gating period in days, hours, minutes and seconds.

Source: internal crystal oscillator with battery back-up.

Note: the clock allows for leap years and all monthly day variances.

FLAGS

Mode: certain flags in addition to being displayed when they occur, are latched in the 3764A and may be viewed subsequently on the display. These are Pattern Sync Loss (SL); AIS (AI); Data Loss (DL); Clock Loss (CL); Out of Lock - option 002 only (OL); Unavailability (UA); Power Loss. The flags are displayed in order of occurrence.

HP-IB

Modes: addressable or talk only.

Flags: Remote; Listen; Talk and SRQ are indicated by LED.

Implementation: IEEE Std 488 - 1978 implementation is as follows SH1; AH1; T5; TE0; L4; LE0; SR1; RL1; PP0; DC1; DT0; C0; E1.

The HP-IB capability also conforms to IEEE Std 728-1982 for Codes and Formats.

PRINTER

Type: 20 column impact printer.

Printing Speed: typically 0.7 lines per second.

Buffer Store: approximately 100 lines.

GENERAL

Power Supply: switched 230V + 10% -18% or 115V +10% -22% ac, 48 Hz to 66 Hz.

Probe Power: HP active probes may be powered from the 3764A's connector. Supplies available; +15V; -12.6V and GND.

Connectors: all connectors are BNC. Other types may be available to special order.

Dimensions: 178 mm high; 425 mm wide, 440 mm long (7 in x 16.75 in x 17.3 in).

Weight: net wt 15 kg (33 lb) approximately, depending on option;

shipping wt (inc front panel cover) 27 kg (59 lb).

Environment: operating temperature 0°C to 55°C;
printer 0°C to 50°C;
storage temperature range -40°C to +75°C.

OPTIONS

001 FOUR FREQUENCY OPERATION

Internal Clock Source

Frequency: four crystal-controlled frequencies of 2.048 MHz; 8.448 MHz; 34.368 MHz and 139.264 MHz.

Parameters: other parameters as for the Generator Internal Clock Source of the Standard Instrument.

OFFSET

No internal frequency offsets are available. Frequency offsets may be achieved utilizing an external clock source.

External Clock Source

Parameters: As for the External Clock Source of the Standard Instrument.

Data Outputs

CODED

Bit-rate: 2M 2.048 Mbit/s, 8M 8.448 Mbit/s, 34M 34.368 Mbit/s and 139M 139.264 Mbit/s.

Format: 2M, 8M & 34M HDB3/RZ; 139M CMI.

Nominal Maximum pk Volts: 2M & 8M 2.37V; 34M 1.0V 139M 0.5V.

PRBS: 2M & 8M $2^{15}-1$; 34M & 139M $2^{23}-1$.

Nominal Impedance to GND: 75Ω.

Transition Times (75Ω): 2M, 8M & 34M < 5 ns; 139M < 2 ns.

Patterns: as for Standard Instrument.

Protection: open/short circuit protected, maximum voltage ± 5V short term.

BINARY

Format (Nominal): 2M, 8M & 34M TTL RZ/NRZ; 139M ECL RZ/NRZ.

Rate: 2M, 8M & 34M 1 kbit/s to 50 Mbit/s; 139M 1 kbit/s to 170 Mbit/s.

Nominal Impedance: 2M, 8M & 34M 75Ω to GND; 139M 75Ω to -2V.

Clock Outputs

Format: 2M, 8M & 34M nominal TTL levels; 139M nominal ECL levels.

Rate: 2M, 8M & 34M 1 kHz to 50 MHz; 139M 1kHz to 170 MHz.

External Load: 2M, 8M & 34M 75Ω to GND; 139M 75Ω to -2V, dc; 139M 75Ω to GND, ac.

Receiver Clock Source

RECOVERED

Rate: 2.048 MHz, 8.448 MHz, 34.368 MHz and 139.264 MHz.

BINARY

Frequency: 2M, 8M & 34M 1 kHz to 50 MHz; 139M 1 kHz to 170 MHz.

Format: 2M, 8M & 34M nominal TTL levels; 139M nominal ECL levels.

Impedance: 2M, 8M & 34M nominal 75Ω to GND; 139M nominal 75Ω to -2V.

Data Inputs

CODED-TERMINATED MODE

Bit-rate: 2M 2.048 Mbit/s; 8M 8.448 Mbit/s; 34M 34.368 Mbit/s; 139M 139.264 Mbit/s.

Format: 2M, 8M & 34M HDB3/RZ; 139M CMI.

Nominal Maximum pk Volts: 2M & 8M 2.37V; 34M 1.0V; 139M 0.5V.

PRBS: 2M & 8M $2^{15}-1$; 34M & 139M $2^{23}-1$.

Nominal Impedance: 2M, 8M & 34M 75Ω to GND; 139M 75Ω to -2V.

Compensation for Maximum Loss: 2M & 8M 6 dB; 34M & 139M 12 dB.

Polarity: Data or $\overline{\text{Data}}$, switched at the binary level.

Equalization: automatic equalization for cable loss. See above for maximum loss compensation.

Other Patterns: as for Standard Instrument.

CODED-MONITOR MODE

Additional Gain: 2M & 8M 30 dB; 34M & 139M 26 dB.

Other Parameters: as for Terminated Mode.

BINARY

Bit-rate: 2M, 8M & 34M 1 kbit/s to 50 Mbit/s; 139M 1 kbit/s to 170 Mbit/s.

Nominal Amplitude: 2M, 8M & 34M TTL levels; 139M ECL levels.

Nominal Impedance: 2M, 8M & 34M 75Ω to GND; 139M 75Ω to -2V.

Patterns: as for Coded Data Inputs.

EXTERNAL ERRORS

Bit-rate: 2M, 8M & 34M 1 kbit/s to 50 Mbit/s; 139M 1 kbit/s to 170 Mbit/s.

Nominal Amplitude: 2M, 8M & 34M TTL levels; 139M ECL levels.

Nominal Impedance: 2M, 8M & 34M 75Ω unbalanced to GND; 139M 75Ω unbalanced to -2V.

002 JITTER GENERATION AND MEASUREMENT

Jitter Generator Section

INTERNAL JITTER MODULATION

Fixed Frequency Points:

100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
200 Hz	2 kHz	20 kHz	200 kHz	2 MHz
500 Hz	5 kHz	50 kHz	500 kHz	3.5 MHz
				4 MHz

Amplitude/Frequency:

Amplitude (UI pk-pk)	Frequency Range
0 to 10.0	100 Hz to 5 kHz
0 to 1.00	10 kHz to 2 MHz
0 to 0.75	at 3.5 MHz
0 to 0.50	at 4 MHz

Amplitude Steps: 0.1 UI pk-pk in the range 100 Hz to 5 kHz;
0.01 UI pk-pk in the range 10 kHz to 4 MHz.

Frequency Accuracy: crystal controlled, better than 0.1%.

Absolute Accuracy: (referred to generator clock monitor output and measured on the 0 to 1 transition of the clock output.)

Frequency Range	Amplitude Accuracy
100 Hz to 5 kHz	As for Ext Jitter Mod, range 10
10 kHz to 4 MHz	As for Ext Jitter Mod, range 1

Intrinsic Jitter: < 0.02 UI pk-pk 5 kHz and below;
< 0.01 UI pk-pk 10 kHz and above.

EXTERNAL JITTER MODULATION

Input Impedance: nominal 50Ω unbalanced to GND.

Range:

	Amplitude (UI pk-pk)	Frequency Range
Range 1	0 to 1.15	2 Hz to 2 MHz
	0 to 0.75	2 MHz to 3.5 MHz
	0 to 0.5	3.5 MHz to 5 MHz
Range 10	0 to 11.5	2 Hz to 100 kHz

Maximum Input Voltage: 10V pk-pk.

Nominal Sensitivity: Range 1 — 5V/UI pk-pk at 1 kHz;
Range 10 — 0.5V/UI pk-pk at 1 kHz.

Absolute Accuracy: (Referred to generator clock monitor output and measured on the 0 to 1 transition of the clock output)

Range 1 — better than ± 3% ± 0.01 UI pk-pk to 1 MHz
additional degradation > 1 MHz less than ± 5%.

Range 10 — better than ± 3% ± 0.1 UI pk-pk.

Intrinsic Jitter: < 0.02 UI pk-pk on range 10;
< 0.01 UI pk-pk on range 1.

Jitter Receiver Section

Mode: jitter can be measured either on a clock recovered from the CMI coded input data or on the binary input clock.

Jitter Reference: the jitter reference signal may be either derived internally from the input data/clock or provided externally.

Frequency Range: external jitter reference and jittered data/clock must be within ± 20 ppm of 139.264 MHz.

Jitter Reference Clock Input (Rear Panel)

Impedance: nominal 75Ω to GND, unbalanced.

Amplitude: nominal ECL levels.

Demodulated Jitter Output (Rear Panel)

Impedance: nominal voltage source, minimum load nominally 50Ω to GND.

Amplitude: range 1 — 5.0V/UI pk-pk;

range 10 — 0.5V/UI pk-pk.

Accuracy: as per measurement circuit (when terminated 50Ω to GND).

Bandwidth: nominally 2 Hz to 3.5 MHz.

Jitter Measurement Input (Rear Panel)

Impedance: nominal 50Ω to GND.

Sensitivity: range 1 — 0.2 UI/V pk-pk;

range 10 — 2.0 UI/V pk-pk.

Jitter Measurement Section

All jitter measurements are made over a selected gating period, as per the error measurements.

JITTER AMPLITUDE

Method: measures maximum value of pk-pk timing jitter over the selected gating period.

	Jitter Amplitude Range	
	1 UI	10 UI
Max jitter amplitude (UI pk-pk)	1.15	11.5
Lowest specified frequency (Internal Reference) (External Reference)	200 Hz nominally 2 Hz	200 Hz nominally 2 Hz
Highest specified frequency	3.5 MHz	10 kHz

RANGE 1

Accuracy (at 1 kHz):

(Internal Reference) $\pm 3\% \pm 0.01$ UI pk-pk;

(External Reference) $\pm 3\% \pm 0.02$ UI pk-pk.

Intrinsic Jitter: ≤ 0.01 UI with a 99.8% confidence level (as measured on binary clock with HP1 filter and Internal Reference).

RANGE 10

Accuracy (at 1 kHz):

(Internal Reference) $\pm 3\% \pm 0.1$ UI pk-pk;

(External Reference) $\pm 3\% \pm 0.2$ UI pk-pk.

Intrinsic Jitter: ≤ 0.1 UI with a 99.8% confidence level (as measured on binary clock with HP1 filter and Internal Reference).

Additional Degradation Factors: applicable to ranges 1 and 10.

Frequency Response: < 200 Hz and > 1 MHz — less than $\pm 5\%$.

Pattern Dependency: ≤ 0.05 UI with a 99.8% confidence level (CMI; 2^{2^3-1} PRBS; LP + HP1).

JITTER HIT COUNT

Method: counts the number of times the received jitter amplitude exceeds a user-set threshold.

Threshold Range: Range 1 — 0 to 1.00 UI pk-pk in steps of 0.01 UI;
Range 10 — 0 to 10.0 UI pk-pk in steps of 0.1 UI.

Display: as for Error Count.

Sensitivity: typically > 40 ns width to count.

JITTER HIT SECONDS

Method: counts the number of seconds in which at least one jitter hit has occurred.

Display: as for Error Count.

JITTER HIT FREE SECONDS

Method: counts the number of seconds in which no jitter hits have occurred.

Display: as for Error Count.

JITTER HITS OUTPUT (REAR PANEL)

Format: one edge per jitter hit. This is a dual purpose port. The output indicates the receipt of either an error or a jitter hit depending on the selected measurement.

INTERNAL FILTERS

The three internal filters are as specified in CCITT Recommendation 0.171.

Filter	Type	Nominal 3 dB Corner Freq	Nominal Slope Asymptote
HP1	High Pass	200 Hz	20 dB/decade
HP2	High Pass	10 kHz	20 dB/decade
LP	Low Pass	3.5 MHz	60 dB/decade

It is possible to configure these filters in the following ways:

- OFF (measurement circuit is connected directly to the jitter demodulator),
- LP; HP1; HP2; LP + HP1; LP + HP2;
- EXT (to allow connection of external filters between the demodulated jitter output port and the jitter measurement input port).

003 DELAYED DATA OUTPUTS

This option provides three data outputs on the rear panel in addition to the main data output on the front panel.

Format: CMI or binary. RZ/NRZ as selected for the main data output.

Delays: Main data O/P to delayed O/P 1 — exactly half a sequence length (on PRBS only.)

Delayed O/P 1 to delayed O/P 2 — > 1 bit;

Delayed O/P 2 to delayed O/P 3 — > 1 bit.

Other Parameters: as for the Main Data Output.

010 TAPE CARTRIDGE UNIT

Storage Capacity of Tape: approximately 210 K characters.

Format: 20 data characters per "line".

Buffer Store: approximately 100 lines.

Environment: operating temperature 0°C to 35°C.

MODES

Results Store: measurement results, system messages, time and date information may be recorded on tape.

Results Recall: the data stored on the tape may be read by two methods:

- (a) directly in a personal computer. The tape format is compatible with the HP 85 and the cartridge may be read in this machine using a suitable programme.
- (b) indirectly via a data transfer through the HP-IB port. HP-IB compatible devices will be able to input this data.

Settings Store: The contents of the measurement pre-set non-volatile memory may be stored on the tape via this control.

Setting Recall: the contents of the measurement pre-set non-volatile memory may be programmed from the tape via this control.

**SPECIAL OPTION:
ADDITIONAL CRYSTAL FREQUENCY F2**

Frequency: any crystal frequency in the range 1 MHz to 170 MHz.

Availability: available on all versions of the 3764A EXCEPT option 001 (four frequency). To special order only.

Format: available at the binary interface only.

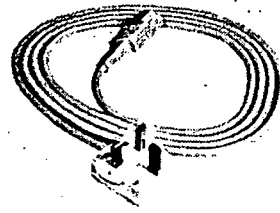
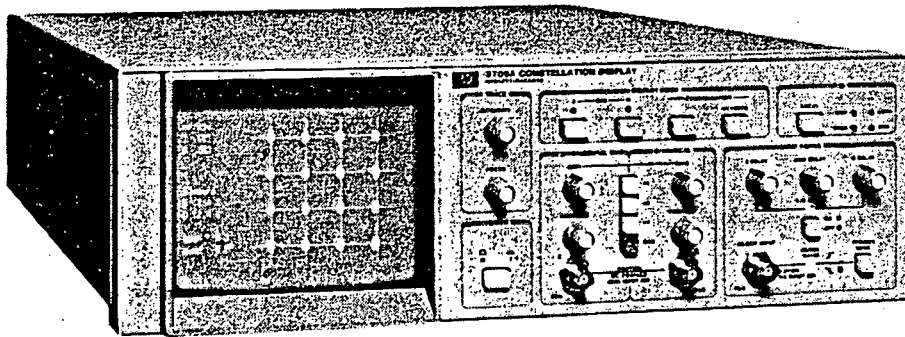


Figure 1-1 3709A Constellation Display and Accessory

General Information

Table 1-1 Specifications

Except where otherwise stated the following parameters are warranted performance specifications. Parameters described as "typical" or "nominal" are supplemental characteristics which provide a useful indication of typical, but non-warranted performance characteristics.

1. RADIO PARAMETERS

Modulation Scheme: The HP 3709A has graticules and measurement routines to cover: QPSK, 9PRS (3LPR), 16QAM, 49PRS (7LPR) and 64QAM radios.

MONITOR POINTS:

Impedance Level: All HP 3709A inputs are 75Ω terminated.

(1) **I and Q Signals:** Any of the above schemes with signal levels in the range 100 mV to 1 V p-p across the constellation. (dc offset must be no more than 0.5 × signal amplitude p-p.)

(2) **Clock:** 1 MHz to 80 MHz
100 mV to 1 V p-p.

Symbol Clock Rate	Bit Rate (Mbit/s)		
	QPSK/ 9PRS	16QAM/ 49PRS	64QAM
Min 1 MHz	2	4	6
Max 80 MHz	160	320	480

2. HP 3709A PARAMETERS

Timebase: All timebase controls autorange to match the timing clock.

Eye pattern width is two clock cycles. I Delay, Q Delay and I&Q Delay controls are adjustable over a range of one clock cycle.

Measurements:

When the MEASURE button is pressed the HP 3709A captures 600 data points and makes a single-shot measurement of the following parameters:

% Closure

The ratio of "cluster size" to "cluster separation". (For both I and Q directions.)

$$\left(\frac{2 \times \text{rms "cluster size"}}{\text{"cluster separation"}} \right) \times 100\%$$

Lock Angle Error

The overall rotation of the constellation. (Positive angle = anti-clockwise rotation.)

Quadrature Angle Error

The I and Q signals should be in Quadrature (90°). The Quadrature Angle error is the deviation from 90°. (Positive error = angle between I and Q > 90°.)

Statistical Uncertainty of Measurement Algorithms.

(Assumes additive gaussian noise is the only impairment and closure is less than 10% for lock and quad error limits.)

99% Confidence limits of statistical measurements.

Lock Angle/Quad Angle:

- < 0.9° with QPSK, 9PRS
- < 0.5° with 16QAM, 49PRS
- < 0.2° with 64QAM

3. INSTRUMENT ACCURACY

Signal Input Return Loss: ≥ 26 dB
(100 kHz to 100 MHz)

Clock Input Return Loss: ≥ 18 dB
(500 kHz to 100 MHz)

Signal Input Frequency Response:

- 0.4 dB nominal (dc to 1 MHz)
- 0.5 dB (1 MHz to 12 MHz)
- 1 dB (1 MHz to 80 MHz)

Accuracy of Displayed Sensitivity at 1 MHz after autocal: ≤ ± 4%.

"Ground Button" Offset: ≤ ± 4 mV.

Timebase Linearity: ≤ 2%.

Timing Jitter (rms):

- ≤ 10ps + 0.2% of clock period
- (= 2 ns at 1 MHz; = 35ps at 80 MHz).

Eye Pattern Width: 2.0 symbols ± 5%.

I to Q Delay: ≤ 2 ns (with I/Q Delay "off").

Residual Noise: ≤ 2 mV (rms) with

- (a) No data input
- (b) I and Q inputs terminated in 75Ω load.

GENERAL

HP-IB (IEEE 488) Capabilities: SH1, AH1, T6, L4, SR1, RL1, DC1.

Connectors: All signal connectors are BNC, 75Ω nominal, unbalanced to ground.

Power supply: 100/120/220/240 V AC;
+5 to -10%; 48 to 66 Hz; <240 VA.

Dimensions (including connectors and feet):
145 mm (5.75 in) high; 425 mm (16.75 in) wide;
540 mm (21.2 in) deep.

OPTIONS

907: Front Handle Kit; adds front handles to the HP 3709A.

908: Rack Flange Kit; enables the HP 3709A to be secured in 483 mm (19 in) rack.

910: Extra set of Manuals.

ACCESSORIES AND RELATED PRODUCTS

TRANSIT CASE

Part No. 9211-2661. Contains custom-moulded inserts which fit snugly around the instrument for maximum protection during transit.

HP 3708A NOISE AND INTERFERENCE TEST SET

The Noise and Interference Test Set can stress an analog or digital radio to simulate a wide range of operating conditions. Noise and interference can be added to the radio IF stages to establish accurate C/N and C/I conditions. Suitable for 70 and 140 MHz IFs or any band in the 10 to 200 MHz range.

APPENDIX C

CONSTRUCTION TECHNIQUES FOR VHF CIRCUITRY

The circuitry developed as described in Chapters 4, 5 and 6 operates mainly in the VHF band, i.e. at or near I.F. (70 MHz.). These signals are of wavelength too long for use of stripline constructions, with lumped-element realisations and discrete devices (even R.F. integrated circuits) being the order of the day. Special construction techniques, broadly known as "ground-plane techniques" are, however, required to avoid stray capacitance and inductance inducing parasitic oscillations and other unwanted effects.

Briefly, the techniques used include:

1. Etching circuit connections on one side of double-sided printed-circuit board (PCB), leaving the other side an unbroken copper plane. This plane is fixed at ground potential (ground plane). All components are mounted on the ground-plane side of the board.
2. Constructing circuit modules on individual boards, these being mounted-on and interconnected-via a "mother-board". (See Fig. C.1). Module-board ground planes are connected to the mother-board ground plane (and thereby to system ground) in a "star" configuration.

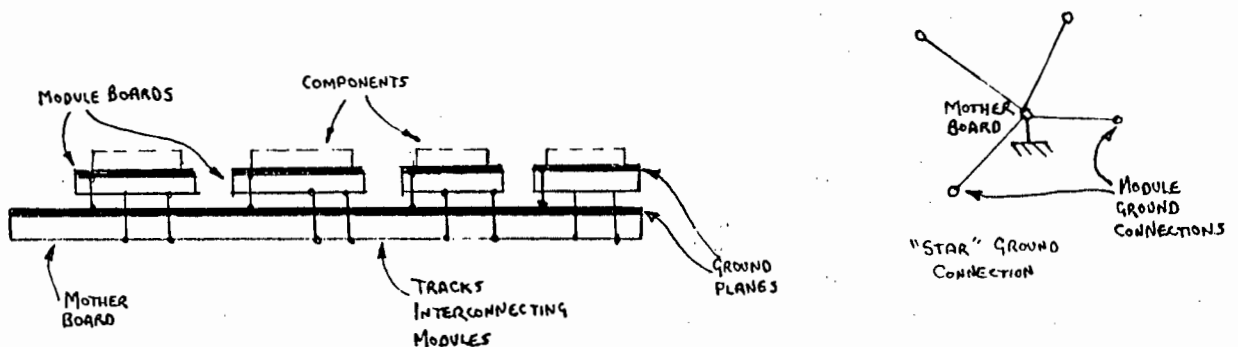


Fig. C.1 PCB CONSTRUCTION AND INTERCONNECTION

3. Ensuring that PCB lay-out avoids placing sections of circuitry operating at vastly differing signal-levels in close proximity to one another. In problem cases, grounded "screening" (copper-plate) can be introduced.
4. Making device-leads as short as possible. (A straight piece of wire exhibits an inductance $L \approx 1\text{nH}$ per mm. length.)
5. Properly decoupling power-rails by using series coils wound on lossy ferrite beads, and shunt capacitors to ground. In the case of supplying power to active devices, capacitors should be situated as near to the device pin as possible.
6. Taking care in selecting components which perform reliably at high frequencies. These include metal-film resistors, ceramic-disc capacitors, R.F. coil formers (including toroids), and of course high-frequency active devices.
7. The use of a resistor network such as in the feedback circuit of the active filter (see Fig. 6.16). The advantage of such a network over a single resistor is it has an effective resistance far larger than any of the individual resistors of which it is comprised. This avoids the problems of stray capacitance which occur with very large resistor values.