Design of *LCL*-filters for Grid-Connected Voltage Source Inverters

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Abstract

LCL-filters are preferred over conventional *L*-filters for grid-connected voltage source inverters (VSI) due to their superior harmonic attenuation, smaller filter size and weight. The *LCL*-filter design process is complex and takes an iterative approach due to the coherence between the filter parameters and design requirements.

The main aim of this thesis is to analyse different design variables that contribute to an efficient *LCL*-filter. The study carried out, falls under two sections. The first study was to understand the importance of ratio between the grid-side and inverter-side inductors, resonance frequency, reactive power production and attenuation of higher order harmonics in an *LCL*-filter. Based on the analysis, this thesis proposes a generalised *LCL*-filter design algorithm which avoids uncertainty in determining resonance frequency as the exact position of the resonance frequency is determined based on the design requirements. The proposed design method considers the *LCL*-filter as a single filtering unit rather than individual filtering contributions from passive components.

The second study is extended to understand the limits of passive components based on the reactive power production limits (based on control structure), IEEE-519 harmonic limitations and the allowable switching losses or voltage drop across the entire filter. Based on the analysis, the thesis proposes an optimum operating point for an *LCL*-filter where the minimum inductance is realised to meet IEEE-519 harmonic current limitations for a given reactive power production while ensuring reasonable switching losses.

Simulations and experimental results are presented to demonstrate the efficacy of the proposed two methods in terms of total harmonic distortion, harmonic attenuation and reactive power compensated.

In addition to the two proposed *LCL*-filter design methodologies, the thesis also presents an analysis on the suitability of the state of the art magnetic materials for inductors in VSI. Initially, properties of magnetic materials were evaluated to select a suitable material for inductor design. Simulations were carried out in ANSYS Maxwell and Simplorer to understand the magnetic behaviour of inductors designed using Sendust, operating under pulse width modulation (PWM) in a three-phase

inverter. Finally, experiments were carried out to evaluate the effectiveness of Sendust for inductors in grid-connected VSI for the proposed *LCL*-filter design.

The results obtained were used to draw conclusions and highlighted the importance of optimising these passive filters in terms of losses and size while ensuring the IEEE-519 harmonic attenuation limits and reactive power production limits of an *LCL*-filter.

Declaration

I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own.

I certify that this dissertation reports original work by me during my University research and each quotation from other people's work used in this report has been cited and listed under references.

Signature.....Signed by candidate. **Date**.....25/03/2016.....

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1 Introduction

1.1 Background and Context

Design of filters for grid-connected voltage source inverters have changed over the last decade with the increase of harmonic constraints set by IEEE-519 standard and limitations in size, weight, switching frequency etc. Initially, first order *L*-filter was used which suffered from poor harmonic attenuation, dynamic performance, higher voltage drop across the filter and bulky design [1]. As a result higher order filters were introduced to get rid of the disadvantages introduced by *L*-filter. The most popular among them is the third-order *LCL*-filter which is capable of meeting the harmonic attenuation requirements even at lower switching frequencies [1] and requires lesser total inductance when compared with the ordinary *L*-filter [1].

Despite the advantages, they introduce resonance in the grid current that should be mitigated for the proper operation of the inverter. To suppress the resonance effect of filter components, active and passive damping techniques are employed. Active damping schemes avoid the use of passive components which results in lower losses compared to passive damping techniques, but at the expense of controller complexity. Furthermore, effect of active damping on *LCL*-filter design should be taken in to consideration to achieve an efficient filter design as shown in [2][3].

As literature suggests, a properly designed filter should have the following characteristics [4];

1. Minimum voltage drop across the filter [1][2]
2. Minimum stored energy in the filter [1][2]
3. Minimum reactive power produced by *LCL*-filter capacitor [2][5][6]
4. High power factor operation [2]
5. Robust to external parameter variations such as grid impedance [2][3]
6. Improved damping performances [7]
7. Minimum damping losses in the damping scheme [7]
8. Low electromagnetic interference [8]
9. Robust to parameter variations due to aging [9]

It is a challenge to satisfy all the above mentioned criteria for an *LCL*-filter due to the interrelationship between filter parameters and different design requirements.

Therefore, it is important to understand the interrelationships between these parameters that will lead to a filter with the above mentioned characteristics. The interrelationships can also enforce limits on the passive components of an *LCL*-filter which the designer needs to be aware of to ensure the proper operation demanded by grid connecting regulations such as IEEE-519 harmonic limitations.

1.2 Scope and Objectives

The aim of this research is to design an optimum *LCL*-filter for grid-connected VSI to meet the harmonic current limitations of IEEE-519 standard, reactive power compensation limits, a robust and low loss *LCL*-filter.

Firstly, it aims to identify the significance of the ratio between the grid-side and the inverter-side inductance then the resonance frequency in realising an efficient *LCL*-filter. Furthermore, it tries to identify the significance of resonance frequency in attenuation of harmonics within an *LCL*-filter. Based on this analysis, it also aims to propose an *LCL*-filter design method which will be tested and verified using an experimental prototype. This method will avoid some difficulties faced by *LCL*-filter designers in past in estimating the resonance frequency of the filter.

Secondly, it aims to identify the relationship between the reactive power production in an *LCL*-filter with the power factor operation of the inverter and the limits of passive components of an *LCL*-filter based on IEEE-519 harmonic limitations, reactive power production and maximum allowable voltage drop across the filter to limit switching losses. Based on the relationships, it also aims to propose an optimum operating point for the *LCL*-filter where minimum inductance is realised. The design will be tested and verified using an experimental prototype controlled via the TMS320F28335 DSP.

Finally, it also aims to evaluate the suitability of other magnetic materials for inductor design in VSI as an alternative to commonly used ferrite material. It also aims to propose a magnetic material that belongs to the powder material category that can replace ferrite materials.

The following was done in order to achieve the above stated objectives:

- Literature review on design of *LCL*-filter for grid-connected VSI and active power filters.

- A review of Matlab simulation software to appreciate how it is used in modelling power electronic systems with the aid of Simscape Power System tool box available from Simulink.
- A review of ANSYS Maxwell magnetic simulation software to appreciate how it is used in modelling the behaviour of passive components (mainly inductors) in an *LCL*-filter.
- Mathematical modelling of the *LCL*-filter based on the analysis of various design criteria.
- Carry out simulations of the proposed designs to validate the theoretical derivations, assumptions etc.
- Carry out experiments in a 3-kVA hardware prototype to validate the efficacy of the proposed designs.

1.3 Achievements and Research contribution

We have been able to propose two unique *LCL*-filter designs. Design 1 considers all the variables in a grid-connected VSI in designing an *LCL*-filter while design 2 proposes an optimum operating point of an *LCL*-filter. The results demonstrate the efficacy of the two proposed methods in terms of the total harmonic distortion (THD), harmonic attenuation and reactive power compensated.

We have also proposed Sendust (KoolMu) magnetic material for inductors used in VSI as a good replacement to ferrite materials. The inductors were implemented using KoolMu material. Inductors were simulated in ANSYS Maxwell software and Simplorer to understand the variation of magnetic properties of an inductor used in an *LCL*-filter. Variation of effective inductance as the biasing current increases due to the soft saturation nature of the KoolMu magnetic material is also shown under simulation results and verified by experimental results.

1.4 Overview of Dissertation

Chapter 2 of this dissertation presents one of the proposed methods to design an *LCL*-filter for a grid-connected voltage source inverter. It includes a thorough literature review on the *LCL*-filter designs proposed in the past and provides an introduction to the basic system modelling of an *LCL*-filter. It analyses the importance of ratio

between grid-side and inverter-side inductors, resonance frequency and the role of resonance frequency in attenuation of higher order harmonics for an *LCL*-filter design.

Chapter 3 presents the second proposed method to design an *LCL*-filter for a grid-connected VSI. It includes the relationship between the reactive power produced and the power factor of the inverter as a device. It also presents the limits of passive components in an *LCL*-filter which can guarantee the IEEE-519 harmonics limitations for a given reactive power production limits while ensuring reasonable switching losses.

Chapter 4 presents inductor modelling for a grid-connected three phase VSI using Sendust powder cores. It includes a comparative analysis for selecting a magnetic material for an inductor in an *LCL*-filter. Selected material is simulated in ANSYS Maxwell and Simplorer to understand magnetic behaviour under pulse width modulation (PWM) in a three-phase inverter. Variation of the effective inductance due to soft saturation nature of the powder cores is utilized to achieve an optimized inductor.

Individual conclusions and evaluation of the research is outlined at the end of each chapter but Chapter 5 aims to provide an overall conclusion regarding an *LCL*-filter design for grid-connected VSI.

1.5 List of Publications

The following articles were written based on the work presented in this thesis and they are currently under review:

1. S. Jayalath and M. Hanif, “Generalised *LCL*-filter Design Algorithm for Grid-connected Voltage Source Inverter”, 2016, IEEE Transaction on Industrial Electronics.
2. S. Jayalath and M. Hanif, “Limits of *LCL*-filter Parameters for a Grid-connected Inverter”, 2016, IEEE Transaction on Industrial Electronics.
3. S. Jayalath and M. Hanif, “Inductor Modelling for a Grid-connected Three-phase Inverter Using Sendust Powder Cores”, 2016, IEEE Transaction on Magnetics.

In addition to the above publications, the following were published in IEEE peer-reviewed conferences. The work related to these publications were carried out during the first year of this research Msc and it covers the controller design and *CL*-filter design for a current source inverter.

[1]. S. Jayalath and M. Hanif, "Controller tuning for a single phase grid-connected current source inverter," Future Energy Electronics Conference (IFEEC), 2015 IEEE 2nd International, Taipei, 2015, pp. 1-6.

[2]. S. Jayalath and M. Hanif, "*CL*-filter design for grid-connected CSI," 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil, 2015, pp. 1-6.

2 Chapter 2

Literature Review and the Proposed Design of *LCL*-filter (Design one)

Higher order filters for VSI have been a popular topic for investigation among the power electronic researchers due to the following advantages associated with them when compared to ordinary *L*-filters:

1. Smaller passive component size
2. Improved dynamic performance
3. Capable of meeting harmonic requirements at lower switching frequencies
4. Reduction in voltage drop across the filter

Among these higher order filters, the *LCL*-filter is an attractive solution due to the simplicity of the filter modelling, implementation and controller design when compared to other higher order filters such as *LCL-LC,LLCL etc*.

The material in this chapter is presented as follows. Initially, a system description of an *LCL*-filter is briefly explained to understand why it is important to analyse certain design parameters such as ratio between the grid-side and inverter-side inductors and the resonance frequency in realising an efficient *LCL*-filter. Section 2.1, explains the importance of ratio between the grid-side and inverter-side inductor while the section 2.2 explains the importance of resonance frequency and its variation under different design requirements (Type of damping and control structure employed *etc*). At the end of the analysis, these key variables of the previously proposed filter designs in literature are compared to understand their impact on the *LCL*-filter operation. Section 2.2.3, extends the analysis to understand the relationship between the resonance frequency and the attenuation provided by an *LCL*-filter to meet the IEEE-519 harmonic limitation standards and reactive power production limits. Based on the analysis presented in section 2.2, section 2.3 presents a step by step guideline to design an *LCL*-filter for a grid-connected VSI with a design example. The design is verified by simulations in Matlab/Simulink and validated experimentally via a 3-kVA hardware prototype. Appendix A provides the derivations of key equations used in this chapter.

2.1 System Description

Figure 2.1 shows the general structure of the grid-connected three-phase VSI with *LCL*-filter, where L_i and L_g are the inverter-side and grid-side inductor, C is the capacitor with series damping resistor, R_d. Resistors R_i and R_g, are the inverter and grid-side resistances, respectively.

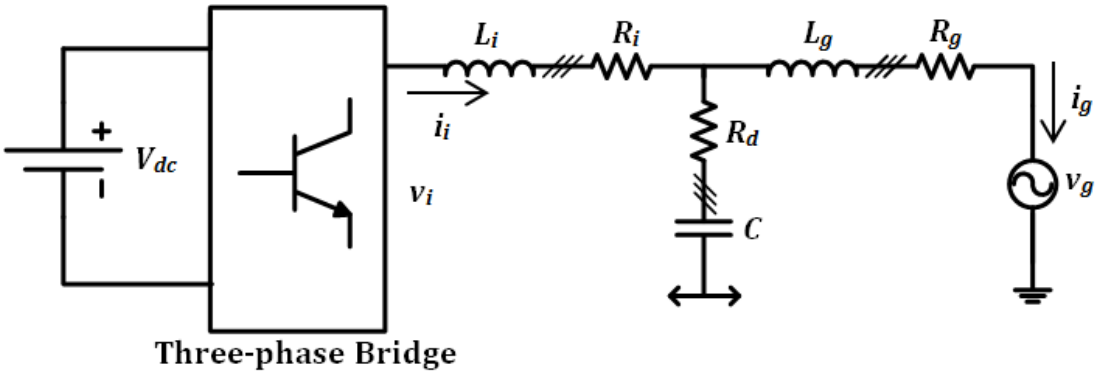


Figure 2.1 General structure of three-phase VSI with *LCL*-filter

Frequency response of the *LCL*-filter

Grid voltage is assumed to behave as an ideal voltage source which is capable of sinking all harmonics when deriving the *LCL* transfer function that is responsible for closed loop system bandwidth in grid-connected operation of the inverter [11]. All the parasitic resistors (R_d, R_i and R_g) are neglected to represent the worst damping performance of the system. For grid-side control [12];

$$\frac{i_g(s)}{v_i(s)} = \frac{1}{s^3 L_i L_g C + s(L_i + L_g)} \tag{2.1}$$

Transfer function for the inverter-side current to inverter-side voltage is;

$$\frac{i_i(s)}{v_i(s)} = \frac{s^2 L_g C + 1}{s^3 L_i L_g C + s(L_i + L_g)} \tag{2.2}$$

Transfer function for the grid-side current to inverter-side current is;

$$\frac{i_g(s)}{i_i(s)} = \frac{1}{s^2 L_g C + 1} \tag{2.3}$$

Where i_g and i_i are grid-side current and inverter-side current and v_i and v_g are the inverter-side and grid-side voltages respectively. Figure 2.2, shows the Y-connected and delta Δ-connected capacitor branch for *LCL*-filter. The resonance frequency of the *LCL*-filter with Y-connected capacitor is given by;

$$\omega_{res}^2 = \left(\frac{L_i+L_g}{L_iL_gC}\right) \tag{2.4}$$

Resonance frequency of the *LCL*-filter with Δ-connected capacitor is given by [13];

$$\omega_{res}^2 = \frac{1}{3}\left(\frac{L_i+L_g}{L_iL_gC}\right) \tag{2.5}$$

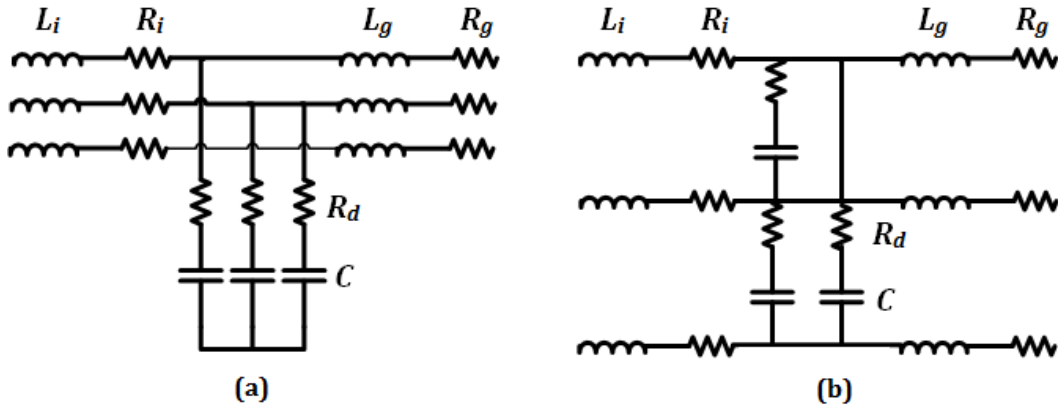


Figure 2.2 Y-connected and delta-connected capacitor branches.

Δ-connected capacitor offers higher attenuation when compared with the Y-connected capacitor. Furthermore, there are reduced harmonics in the current flowing into the Δ-connected capacitor compared to Y-connected [10]. In the case of lower switching frequencies, harmonics become significant and inverter control signal is distorted by these capacitor harmonics. However, the Δ-connected configuration can distort the grid-injected current, if the phase lock loop (PLL) is sensitive to grid line-to-line voltage harmonics [13]. The analysis in this chapter will be based on Y-connected capacitor branch. Therefore, (2.4) can be further expanded as;

$$L_TC = \frac{k^2}{4\pi^2 f_{sw}^2}\frac{(1+\mu)^2}{\mu} \tag{2.6}$$

Where total inductance, $L_T = L_i + L_g$, ratio $k = f_{sw}/f_{res}$, f_{sw} is the switching frequency of the PWM and f_{res} is the *LCL* resonance frequency and ratio $\mu = L_g/L_i$. General observation based on (2.6) is that lower resonance frequency (higher k) requires larger inductance and capacitance values in the filter, hence, higher resonance frequencies (lower k) for the filter are preferred due to lower size and cost of filter components [1]. It is important to analyze the behaviour of resonance frequency (ratio k is considered in this thesis) under various design requirements for a grid-connected VSI. Furthermore, according to (2.6), ratio μ also plays a vital role in determining the values of L_T and C. Therefore, the section below will analyze the impact of ratio μ and ratio k, on the performance of grid-connected VSI with *LCL*-filter. At the end of the analysis, the effects of these two variables in previously proposed *LCL*-filters are compared.

2.2 Interrelationship between Parameters

2.2.1 Ratio μ (L_g/L_i)

One of the main goals in *LCL*-filter design is to minimize the passive component size while ensuring that adequate attenuation and reactive power are compensated by the filter and therefore it is important to identify from (2.6) the value of μ which results in the lowest product of L_TC as it contributes the minimum passive component size.

The minimum product of L_TC for a given resonance frequency can be evaluated by differentiating (2.6) with respect to the variable μ. When $\mu=1$, the minimum product of L_TC is realized. This means for a given capacitance value, the resulting L_T is the minimum [2], hence the minimum voltage drop (V_d) across the inductors as $V_d = I_g(2\pi f_g L_T)$, where I_g is the grid injected current and f_g is the grid operating frequency. Furthermore, for a given L_T, the resulting C is minimum. Minimum C corresponds to the minimum reactive power production [2][11]. A detailed analysis on determination of reactive power compensation limits is elaborated in Section 2.2.3 of this chapter.

Pena-Alzola et.al has shown that $\mu=1$ results in an improved robust filter to grid inductance variation and minimum stored energy in the *LCL*-filter [2]. Derivation of the minimum energy storage of an *LCL*-filter at $\mu=1$ is also shown in section 2.2.2

'Ratio *k*' of this chapter. Therefore, it is evident that by selecting $\mu=1$, satisfies the points 1-5 of the characteristics for a desired filter as mentioned above in the introduction. It can be concluded that $\mu=1$ can contribute to an improved and efficient filter.

Next sub-section will evaluate the other variable parameter *k* in (2.6). Unlike μ, determining an optimum value for *k* is not straight forward due to different design considerations. Therefore, a detailed analysis based on control aspects of VSI, damping regions and damping schemes are used to understand its significance.

2.2.2 Ratio *k* (f_{sw}/f_{res})

Resonance frequency is determined by the designed filter components as shown by (2.4) and (2.5) but an estimation of the resonance frequency is crucial in *LCL*-filter design process [15],[2],[3]. It is partially guided by the stability of the inverter, controller bandwidth, damping method employed etc.

The Bode plot of transfer function (2.1) as shown in Figure 2.3, shows that *LCL*-filter has higher attenuation for the frequencies around the switching frequency of a VSI at the rate of 60dB/decade, when compared to the rate of 20dB/decade in the case of *L*-filter. Therefore, switching frequency is selected above the resonance frequency.

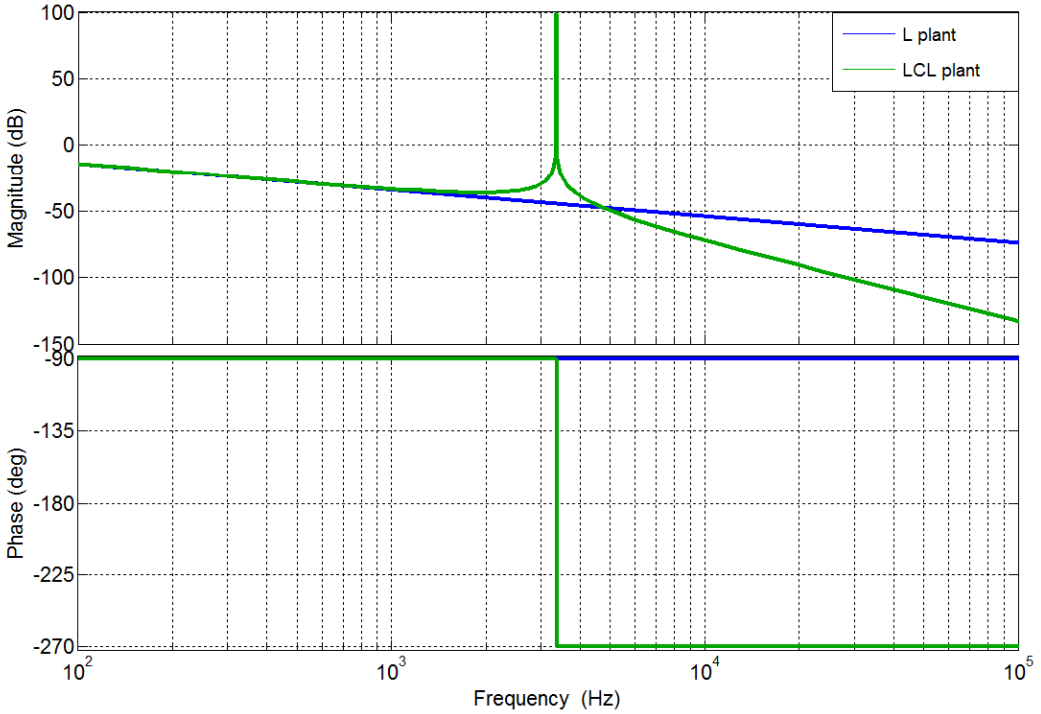


Figure 2.3 Bode plot of *L*-filter and *LCL*-filter

Furthermore, in digital controllers sampling frequency, f_s is related to switching frequency in two ways. There are two update modes used in digital implementation of the controller. In single update mode, sampling of all the measurements is carried out at the beginning of each PWM period and updating all the PWM registers at the end with the output. Therefore $f_s=f_{sw}$, while in double update PWM, reference is updated at the start of half-carrier cycle. Therefore, sampling frequency is twice the switching frequency in this case. But irrespective of the PWM method employed, sampling frequency should be at least twice the resonance frequency to ensure that resonance is visible to the digital signal processor (DSP) according to Nyquist sampling criteria.

Now, the relationship between the bandwidth frequency of the controller (f_b), resonance frequency, switching frequency and the sampling frequency can be evaluated. In order to avoid resonance inside the control bandwidth and for the resonance to be visible to the digital controller, f_{res} needs to vary between the bandwidth frequency and half of the sampling frequency, f_s of the inverter system [5][15]. Therefore, f_{res} need to satisfy the following inequality;

$$\boldsymbol{f_b < f_{res} < \frac{1}{2} f_s} \tag{2.7}$$

Bandwidth of the VSI can be evaluated by analyzing the closed loop bandwidth of the VSI in digitally controlled system as shown in [16].

$$\boldsymbol{f_b \approx \frac{f_s}{6\pi}} \tag{2.8}$$

(2.7) is modified to represent ratio k (i.e. $=f_{sw}/f_{res}$) to obtain the following inequality for double update PWM, in which f_s in (2.7) and (2.8) becomes $2f_{sw}$.

$$\boldsymbol{1 < k < 9.5} \tag{2.9}$$

The maximum and minimum limit for the single update PWM will be 2 and 19. Alternatively, a mean value for k can be derived by evaluating the geometrical mean of f_b and f_{sw} according to [2]. The mean value, k_{mean} of k provides an approximate idea of the location of resonance frequency with reference to the bandwidth of the inverter and switching frequency [2].

$$f_{res} = \sqrt{f_b * f_{sw}} \quad (2.10)$$

For Single update PWM, $f_s=f_{sw}$

$$k_{mean} \approx 4.34 \quad (2.11)$$

For Double update PWM, $f_s=2f_{sw}$

$$k_{mean} \approx 3.07 \quad (2.12)$$

According to (2.9) for double update PWM the minimum and maximum limit of k is 1 and 9 and there are infinite resonance frequencies within this range that can satisfy the basic control aspect of grid-connected VSI. However, the controller implemented in a VSI with *LCL*-filter will not function properly unless the resonance is damped.

2.2.2.1 Importance of ratio *k* on different damping regions

This section analyzes the impact of k on the damping performances. Damping regions are identified by evaluating the transfer function of the grid-injected current control. Open loop transfer function of the forward path of the grid connected inverter current control system can be derived from the control diagram shown in Figure 2.4.

$$\frac{I_g(s)}{I_e(s)} = G_c(s)V_{dc}e^{-sT_d}G_p(s) \quad (2.13)$$

Where $G_c(s)$ and $G_p(s)$ are the controller and plant transfer function. V_{dc} is the inverter gain and e^{-sT_d} is the computation delay. Detailed analysis of these transfer functions can be found in [14]. The angle of the forward path at a given frequency can be derived as shown in [14];

$$\measuredangle \frac{I_g}{I_e}(e^{j\omega T_s}) = \measuredangle \left(\frac{K_p V_{dc} T_s}{(L_i+L_g)} \frac{1}{e^{j\omega T_s}(e^{j\omega T_s}-1)} \right) \quad (2.14)$$

Where K_p is the proportional gain of the controller while the T_s is the sampling time. It is observed from the bode plot shown in Figure 2.3, that the resonance frequency is well below the unity gain cross over frequency (0dB), hence , phase contribution at crossover frequency can be neglected. Furthermore, the effect of *LCL*-filter resonance frequency on the phase response becomes dominant only around the resonance frequency as seen from Figure 2.3. Therefore, phase contribution of the *LCL*-filter at low frequencies can be approximated to $\measuredangle h\left(1/\left(e^{j\omega T}-1\right)\right)$ [14].
Consequently, (2.14) can be simplified to;

$$\measuredangle \frac{I_g}{I_e}(e^{j\omega T}) = -\omega T - \frac{\pi}{2} - \frac{\omega T}{2} \qquad 2.15$$

Critical frequency (ω_c) that separates the two stable regions of operation with and without damping can be identified by equating (2.15) to -180^0 [14]

$$\omega_c \approx \frac{\pi}{3T_s} \qquad 2.16$$

(2.16) simplifies to $f_c = f_s/6$, where f_c is the critical frequency, $\omega_c = 2\pi f_c$. If the resonant frequency is placed at f_c, the ratio k becomes 6 [14] for single update PWM, and $k=3$ for double update PWM. The system becomes unstable at f_c (at k=3 for double update PWM) due to the pair of open loop unstable poles created [17]. The designer can assign the resonant frequency above f_c to avoid the use of damping while below f_c, damping is compulsory for stable operation. In the latter case, resonant frequency should be placed reasonably above the critical resonant frequency value to ensure reasonable gain margin for a given phase margin [14]. However, the

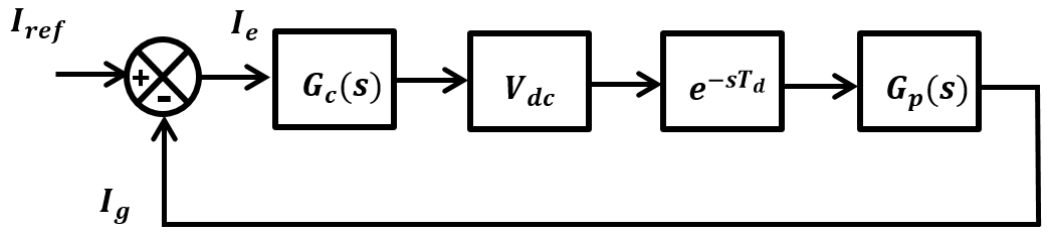


Figure 2.4 Control diagram for grid-connected VSI

performance of the *LCL*-filter varies with different damping schemes.

2.2.2.2 Importance of ratio *k* under different damping schemes

This section looks into the significance of *k* under different damping methods.

- **Active Damping**

Pan et. al[18] highlights the importance of computation and PWM delay on the effectiveness of the capacitor current feedback active damping for the *LCL* type grid-connected inverter. Similar analysis can be found in [2] and for the Lead lag method in [3]. According to analysis, selecting k=3.12 results in maximum damping at that particular damping frequency for capacitor current feedback active damping method. In the case of Lead-Lag method, ratio k=3.2 to 3.4 results in the optimum damping. Both uses single PWM update method where $f_{sw}=f_s$.

- **Passive Damping**

Passive damping schemes are preferred over active damping in the case of stiff grid operating conditions. They are relatively simple to implement at a lower cost [19]. When passive damping schemes are considered, for grid-side current control, *k* should be set to as low as possible to achieve the maximum damping of resonant harmonics [20]. But in inverter-side current feedback system, *k* should be closer to 6 (critical frequency) to achieve maximum harmonics attenuation [20].

Nevertheless, the most important aspect in passive damping schemes are the losses in the damping branch which is absent in the active damping schemes. Therefore, the impact of ratio *k* on the passive damping losses is an important factor in minimizing losses of an *LCL*-filter under passive damping. The minimum damping required in an *LCL*-filter is analyzed in [7]. The damping resistor (R_d) is proportional to:

$$\boldsymbol{R_d \; \alpha \; \frac{f_s L_g^2}{L_i + L_g}} \tag{2.17}$$

Damping power losses (P_d) will be based on the lower and upper limits of harmonic capacitor current. The lower power loss limit (P_{DL}^L) is given by [7],

$$\boldsymbol{P_{DL}^L = 3\,(I_c^L)^2 R_d} \tag{2.18}$$

Where I_c^L lower bound of *LCL*-filter capacitor current harmonics, while the upper loss limit (P_{DL}^U) is given by,

$$\boldsymbol{P_{DL}^U = 3\,(I_c^U)^2 R_d} \qquad 2.19$$

Where I_c^U upper bound of *LCL*-filter capacitor current harmonics. An average value of (2.18) and (2.19) can be used to estimate the damping power loss [7]. As shown in [2], power loss is a function of ratio *k* and higher values of *k* are preferred to reduce losses but higher values will increase the amount of stored energy in an *LCL*-filter as shown next.

The amount of stored energy in an *LCL*-filter due to the variation of *k* and μ are evaluated. Stored energy in an *LCL*-filter can be defined according to [1];

$$\boldsymbol{E_T = \frac{3}{2}(L_i I_r^2 + L_g I_r^2 + C V_r^2)} \qquad 2.20$$

Where I_r and V_r are rated grid current and voltage. (2.20) can be rearranged to give an insight into the effect of other design parameters on the filter design by substituting L_T from (2.6) into (2.20).

$$\boldsymbol{E_T = \frac{3}{2}\left(\left(\frac{k^2}{C\omega_{sw}^2}\left(\frac{(1+\mu)^2}{\mu}\right)\right) I_r^2 + C V_r^2\right)} \qquad 2.21$$

Higher values of *k* will increase the stored energy in the filter. It means that lower resonance frequencies will have higher passive component sizes according to (2.6) and understandably the stored energy will be relatively high. Furthermore, the ratio μ =1 also corresponds to the minimum stored energy, by setting the derivative of (2.21) with respect to μ equal to zero.

Finally the impact of *k* on the THD of the inverter is discussed. THD of the grid-injected current should be less than 5% according to IEEE-519[21]. The effect of various parameters on the THD is studied in [2]. According to the study, increasing ratio *k* will lower the THD as switching frequencies will have a higher attenuation level on 60 dB/decade slope as seen from Figure 2.3. It can be concluded that a mean

(midway) value of k can preferably bring about an optimum LCL-filter in terms of stored energy, THD evaluation, losses in passive damping and passive component size.

Table 2.1 summarizes the value of k under different scenarios described so far. It proves that the value of k and the performance of an LCL-filter design is highly subjective upon the design requirements. Furthermore, Table 2.2 compares the designs proposed in literature. It is evident from the comparison that there is a considerable variation in the ratio k while ratio $\mu=1$ is common in the most of the designs proposed in literature. Nevertheless, in this thesis the analysis on ratio k is extended to exploit the relationship between the degree of attenuation of harmonics at switching frequency and reactive power produced by the LCL-filter for a given ratio μ between grid-side and inverter-side inductor.

Table 2.1 Comparison of Value k Under Various Design Requirements

Scenario	$k(f_{sw}/f_{res})$
Minimum k based on single update PWM	2
Mean value of k in Double update PWM	3.07
Mean value of k in Single update PWM	4.34
Capacitor active damping(Maximum damping)	3.12
Lead Lag Network(Maximum damping)	3.2-3.4
Critical resonance frequency Single update PWM	6
Critical resonance frequency Double update PWM	3
Grid-side current control(Passive damping) (To achieve maximum resonant damping)	Small as possible
Inverter-side control(Passive damping) (To achieve maximum harmonic attenuation)	Close to 6
To minimize losses in the case passive damping	Higher values
Stored energy in the filter	Small as possible
Total Harmonic Distortion of the filter	High as possible
Small passive component size (L_T and C)	Small as possible

Table 2.2 Comparison between different filter designs proposed

Reference	$k(f_{sw}/f_{res})$	$\mu(L_g/L_i)$	PWM	Damping	Control
[6]	2.01/3.228	1.67	S	Passive	Grid-side
[11]	10	1	N/A	Passive	N/A
[10]	2.32	0.019	N/A	Passive	Grid-side
[1]	4.08	1	D	Active	N/A
	2.88	1	D		
[2]	3.27	1	S	Active	Inv-side
[15]	4.16	1	D	Passive	Inv-side
[3]	3.35	1.11	S	Active	N/A
[22]	3.39	2.7	N/A	Passive	N/A

Inv-side – Inverter side, S-Single update , D- Double update

2.2.3 Relationship between the attenuation factor

Attenuation of switching harmonics by an *LCL*-filter can be further evaluated by considering the ratios between the grid-side current harmonics ($i_g(h)$) to inverter-side voltage harmonics($v_i(h)$) and inverter-side current harmonics($i_i(h)$) to inverter-side voltage harmonics at switching frequency. To derive these transfer functions, the inverter is considered as a harmonic generator while the grid as a short circuit at high and medium frequencies [5]. The ratio of grid-side current to the inverter-side voltage at switching frequency $s=h=j\omega_{sw}=j2\pi f_{sw}$ deduced through (2.1)

$$\left|\frac{i_g(h)}{v_i(h)}\right| = \frac{1}{2\pi L_T f_{sw}|1-k^2|} = a_g \tag{2.22}$$

Where a_g is the grid-side current magnitude attenuation coefficient. The magnitude ratio of inverter-side current to the inverter-side voltage at switching frequency is given by [23],

$$\left|\frac{i_i(h)}{v_i(h)}\right| = \frac{|(1-k^2(1+\mu)|}{2\pi L_T f_{sw}|1-k^2|} = a_i \tag{2.23}$$

(2.22) shows the level of attenuation of switching frequency provided by an *LCL*-filter in which increasing L_T and k improves the attenuation for a given switching frequency. However for a given μ, L_T and f_{sw}, increasing ratio k means that the capacitance of the filter increases according to (2.6). This increase will negatively affects the reactive power production limits of an *LCL*-filter as low values of capacitances are preferred. Therefore, it is important to identify the behaviour of ratio k in an *LCL*-filter to realize an efficient filter design.

According to the analysis given in section 2.2.1, the minimum product of (L_TC) for a given k occurs when $\mu=1$. This is also shown in Figure 2.5. Alternatively (2.6) can be analyzed to understand the behaviour of ratio k for a given (L_TC) and f_{sw} with ratio μ. (2.6) becomes;

$$k^2 = \left(4\pi^2 f_{sw}^2\right)\left(L_T C\right)\frac{\mu}{\left(1+\mu\right)^2} \qquad 2.24$$

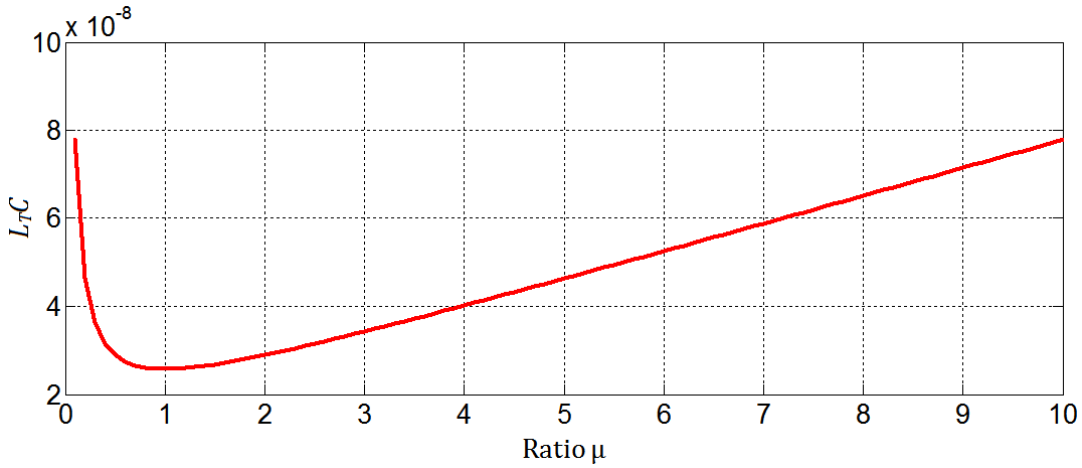


Figure 2.5 Variation of (L_TC) vs Ratio μ for a given $k\approx5$

Maximum k for a given f_{sw} and product of L_TC can be evaluated by differentiating (2.24) with respect to variable μ. When $\mu=1$, maximum k is realized (minimum resonance frequency for a given f_{sw} and product of L_TC). Ratio k of (2.24) plotted against the ratio μ is shown in Figure 2.6. The variation of k with μ has a direct impact on the attenuation of the *LCL*-filter given by (2.1), as seen by the bode plot of (2.1) shown in Figure 2.7, for a given f_{sw} and product of L_TC with varying μ. As μ increases from 0.1 to 1, the attenuation of harmonics above resonance frequency improves at a

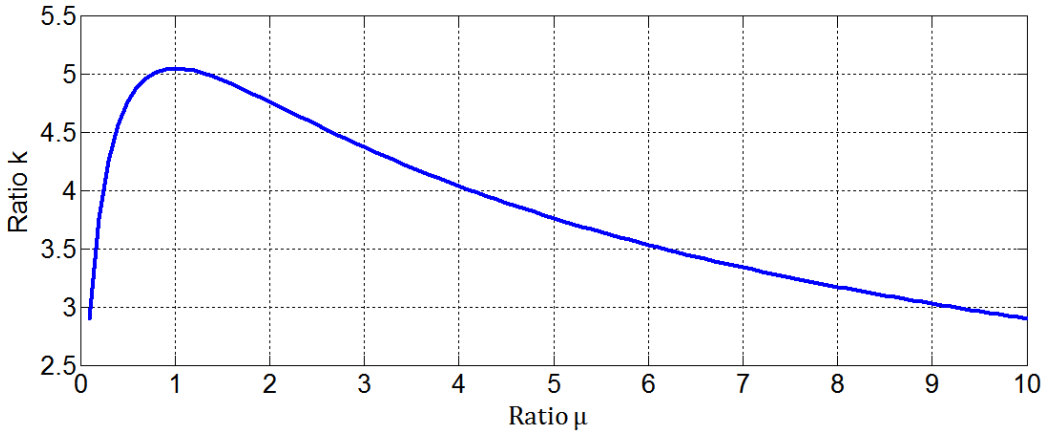


Figure 2.6 Variation of Ratio k with Ratio μ for a given L_TC=2.53x10^{-8}, f_{sw}

higher rate and reaches a maximum at μ =1 and reduces at a slower rate as μ increases. However, the attenuation of low frequencies up to resonance frequency remains constant irrespective of the μ value. Therefore impact of μ on attenuation provided by an *LCL*-filter occurs after the resonance frequency for a given L_T and C, in which μ =1 corresponds to the maximum attenuation.

However, for a given resonance frequency, there are infinite combinations of individual L_T and C as seen from the bode plot of (2.1) shown in Figure 2.8. Figure 2.8 shows the combinations listed in Table 2.3, where $\mu=1$ is considered for all the

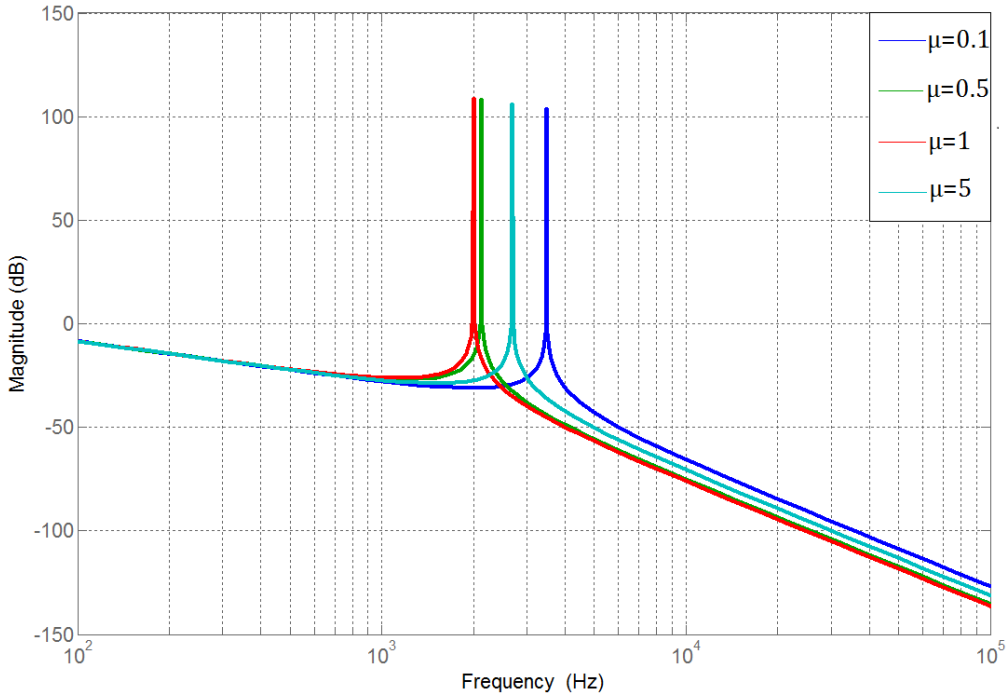


Figure 2.7 Bode plot of $i_g(s)/v_i(s)$ for different μ values

combinations and the resonance frequency is 2000 Hz (k≈5). This behavior is mathematically supported by (2.6) and (2.22). (2.6) simplifies to (2.25) when $\mu=1$,

$$\boldsymbol{L_T = \frac{4k^2}{C\omega_{sw}^2}} \qquad 2.25$$

As L_T increases, C reduces to maintain the same ratio k. The attenuation of both the low frequency up to resonance frequency and above resonance frequency increases at the same rate as seen from Figure 2.8. Unlike the previous case where change in ratio μ only impacted the attenuation after resonance frequency, here it affects the frequencies up to resonance frequency as well. Reduction in C will minimize the reactive power of the inverter or inverter operating power factor will improve (almost unity). Therefore, the capacitor C in (2.6) is selected to limit the overrating of the inverter or reduction in power factor of the inverter and to minimize the reactive power production [5][24][25]. Base impedance of an LCL-filter is given by

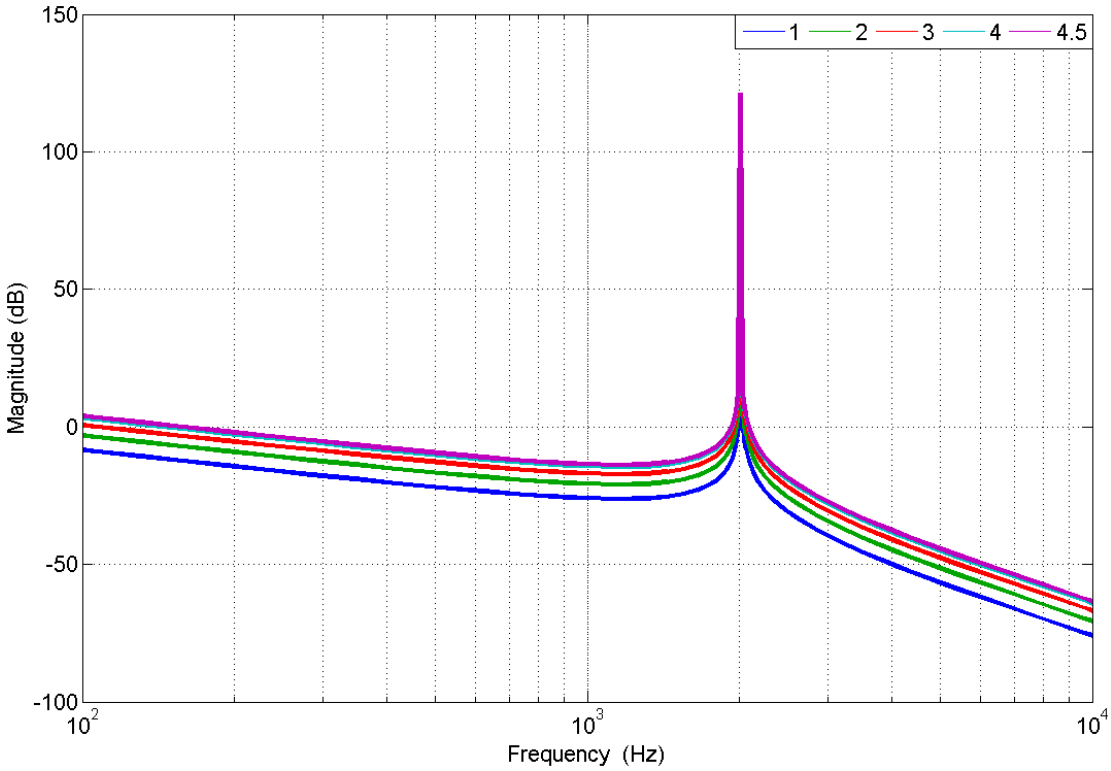


Figure 2.8 Bode plot of i_g(s)/v_i (s) for different L_TC products given in Table 2.3, where 4.5-1 refer to % of power factor variation.

Table 2.3 Power Factor Variations and *LCL*-filter Parameters

Power factor %	*C(μF)*	L_T*(mH)*	R_d*(Ω)*	*THD(%)*
1	6	4.21	4.5	0.56
2	11	2.30	2.41	0.72
3	17	1.49	1.6	1.14
4	23	1.10	1.15	1.5
4.5	25	1.01	0.96	2

$$\boldsymbol{Z_b = \frac{V_{gl-l}^2}{P_r}} \quad 2.26$$

Where $V_{gl\text{-}l}$ and P_r are line to line grid voltage and rated active power. Base capacitance

$$\boldsymbol{C_b = \frac{1}{\omega_g Z_b}} \quad 2.27$$

Filter capacitance is estimated by considering the limit of maximum power factor variation, α seen by the grid. Usually maximum value of α =5% as reported for grid-connected inverters in [10]. Filter capacitor becomes [5][6];

$$\boldsymbol{C = \alpha C_b} \quad 2.28$$

This defines the limit of capacitance variation expected around a given resonance frequency and it should always be equal or less than the maximum defined by (2.28)

$$\boldsymbol{0 < C \leq \alpha C_b} \quad 2.29$$

Similarly, the limit on total inductance, L_T needs to be identified for an *LCL*-filter. It is guided by the *IEEE*-519 harmonic limitations as shown in Table 2.4. It defines allowable percentages for limitations of grid harmonics with respect to rated grid injected current. These limitations are related to the attenuation at the switching

Table 2.4 Current Harmonic Limits according to IEEE-519 [21]

Limits as a Percentage of Rated Current Amplitude						
I_{sc}/I_L	3≤h≤11	11≤h≤17	17≤h≤23	23≤h≤35	35≤h≤50	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0

frequency given by (2.22). The minimum inductance requirement for a given k and switching frequency that satisfies the harmonic limitations listed in Table 2.4 is calculated using (2.22). In which L_T becomes;

$$\boldsymbol{L_{Tmin} = \frac{1}{2\pi f_{sw}.\left|\frac{i_g(h)}{v_i(h)}\right|.|1-k^2|}} \qquad 2.30$$

The ratio $i_g(h)/v_i(h)$ in (2.30) does not directly represents the ratios listed in Table 2.4 as it corresponds to $i_g(h)/ i_g$, where i_g is the rated grid injected current. Hence per unit representation of (2.30) is derived as it relates to the harmonic limitation ratios listed. Therefore, for a p.u system (2.30) becomes [11];

$$\boldsymbol{l_T = \frac{1}{h_{sw}\left|\frac{i_{pu}(h)}{v_{pu}(h)}\right|.|1-k^2|}} \qquad 2.31$$

Where $l_T=L_T/L_b$ is the pu inductance in which (L_b is the base inductance, $L_b=Z_b/(2*pi*f_{base})$, base impedance(Z_b) is given by (2.26) , f_{base} is base frequency of the filter, which is the frequency of the grid voltage. $h_{sw}=f_{sw}/f_{base}$ is the switching harmonic number. $i_{pu}(h) = i_g(h)/ i_g$, where i_g is the rated grid injected current. $i_{pu}(h)$ corresponds to the limits imposed by IEEE-519. It defines allowable percentages for limitations of grid harmonics with respect to rated grid injected current as shown in Table 2.4. $v_{pu}(h)=v_i(h)/v_g$, $v_i(h)$ is the voltage ripple at the switching frequency, which can be approximated to $V_{dc}/4$ as shown in [11]or can be determined based on Fourier analysis of the inverter voltage, software simulations depending on the modulation strategy used [1][23]. Where v_g is the rated inverter voltage which is approximately equal to the grid voltage. (2.31) can be solved to obtain the per unit minimum inductance requirement in the *LCL*-filter to satisfy the harmonic limitations imposed

by IEEE-519. Nominal value of L_T can be recalculated from (2.31) as $L_T=l_TZ_b/2\pi f_{base.}$ Therefore, the total inductance (L_T) needs to satisfy the following inequality.

$$\boldsymbol{L_T \geq L_{Tmin}} \qquad 2.32$$

The maximum value of L_T will be limited by the dc bus availability [5] and the anticipated switching losses as the losses increases with higher dc bus values [5]. Hence, when optimizing the entire inverter system with an *LCL*-filter, these limitations need to be considered.

It can be concluded that $\mu=1$ is a special operating region in an *LCL*-filter in which minimum product of (L_TC) is realized (small passive components) and also for a given product of (L_TC) minimum resonance frequency (maximum k) and maximum attenuation is realized.

Based on the above analysis the next section will provide a step by step guideline to design an *LCL*-filter for a grid-connected VSI.

2.3 Determining the filter parameters

In this chapter, the filter design is based on the ratio μ, k, reactive power production limit and attenuation limits of switching harmonics (a_g). Initially, the following design parameters are listed irrespective of the damping and control method used. P_r - rated active power of the system under study, ω_{sw}/f_{sw} switching frequency, ω_g/f_g - Grid operating frequency, V_{DC} – dc-link voltage, $V_{l\text{-}l}$ converter output line-to-line RMS voltage and V_g – Rated grid voltage. Then the following steps are followed;

- Determine the control method(grid-side current or inverter-side current control)
- Determining the damping method based on the application.
- Determine the ratio μ based on design method used as discussed in section 2.2.1 and 2.2.3.
- Determine the range of k depending on the PWM update used.
- Determine k that corresponds to the critical resonance frequency so that it is avoided.
- Estimate the ratio k based on the design requirements listed in Table 2.1. An average value of k is preferred.

- Determine the product L_TC that meets the ratio k.
- Determine the minimum per unit l_T (l_{Tmin}) using (2.31) to meet IEEE-519 harmonic limitations and determine nominal L (L_{Tmin}).
- Determine the maximum capacitance (C_{max}) corresponding to the L_{Tmin} using (2.6).
- Determine the maximum limit on the power factor variation seen by grid for the calculated $L_{Tmin.}$
- Determine the final values of C and L based on the required limitations on reactive power production if strict limits are required as shown later in the design example.
- Analyse the filter performance in terms of harmonic attenuation, THD and reactive power production.
- Physical design of inductors such that losses are minimised using appropriate cores, wires etc according to the guidelines provided by magnetic designers [26].

A design example is presented to evaluate the effectiveness of the proposed method.

Design Example:

System parameters are listed in the Table 2.5. Grid current is controlled in which passive damping is preferred due to the simplicity in controller implementation. Ratio $\mu = 1$, is considered as it results in the small and efficient *LCL*-filter according to the analysis presented above. Double update PWM method is selected. Therefore, k needs to satisfy the following inequality; $1<k<9.5$. Critical frequency of the system will occur at $k=3$, therefore, it is avoided. A mean value of k is selected as it brings out the best performance in the filter according to the information listed in Table 2.1. The estimated value should bring about a balance in losses in passive damping scheme, higher attenuation, minimum stored energy and small passive component size. Ideally value of k between 4.5 and 5.5 is preferred. Therefore $k\approx5$ is estimated. Value of k is substituted in (2.6) to obtain the product of $CL_T=2.53\text{x}10^{-8}$. L_{Tmin} required to meet IEEE-519 harmonics limitations calculated using (2.31) is 1.018 mH. From the product of CL_T, given by (2.6), maximum C for the harmonic limitations will be 25 μF or the maximum power factor variation seen by the grid at this particular resonance frequency will be 4.5% according to (2.28). Anyhow, the maximum power factor variation seen by the grid is set to be 1%, which results in the maximum capacitance of 6.11 μF according to (2.26)-(2.28). The corresponding L_T for the capacitance $C \approx 6$ μF will be 4.21 mH. Therefore, L_i=2.10mH, L_g=2.10mH. A similar evaluation is

carried out for different power factor variations seen by the grid and the corresponding L_T and C are given in Table 2.3. As the power factor variation seen by the grid increases, inductance required in the system can be minimized at the expense of higher reactive power production and high THD. But as seen from the Table 2.3, the selected resonance frequency is only capable of facilitating a maximum power factor variation of 4.5%. However, it is always preferable to minimize the power factor variation to ensure that inverter operates closer to unity power factor.

The advantage of this design procedure compared to the previously proposed designs [5][6][10] is that it considers the significance of ratio μ, k, attenuation of harmonics and reactive power production of an *LCL*-filter and filter operates as a single filtering unit rather than considering individual filtering contributions from L_i and L_g components. Furthermore, the presented design satisfies most of the characteristics for a desired filter as mentioned above in the introduction.

Table 2.5 System Parameters

Parameters	*Value*
Rated power(3ϕ)	3000
Rated grid voltage(rms)	75
DC voltage bus	250
Rated current(rms)	13.85
Grid operating frequency	50 Hz
Switching frequency	10 kHz
Sampling frequency	20 kHz
Z_b	5.6250
Capacitor	6 μF
Grid side inductor	2.10 mH
Inverter side inductor	2.10 mH
$a.f$	18.85
K_{P_pu}	1.20
K_{I_pu}	450
Inductor Loss	30 W
Total Power Loss	190 W

2.4 Simulation and Experimental Results

The proposed *LCL*-filter design example for a three-phase grid-connected VSI is verified using *Matlab* simulink and experimentally. The block diagram of the Matlab Simulink file is shown in Appendix D. In simulation, the controller is sampled at f_s=20 kHz (50μs) to mimic the operation inside a digital signal processor, while the rest of the system, including inverter, filter etc are sampled at a higher rate to mimic the behavior of a VSI in real time (at least >100f_s). The controller is implemented based on the per unit measurements of grid voltage and current, where grid injected current is controlled based on the reference current value given to the controller and controller gains calculated using the guidance provided in [12]. These calculated gains are multiplied by the p.u attenuation factor (*a.f*) to comply with the p.u controlling of the measured p.u currents and voltages. It is given by, $a.f = (P_r/3V_g)\sqrt{2}$, where P_r is the rated grid injected current while V_g is the rms grid voltage. Calculated *a.f* and the p.u gain values used for both simulations and experimental setup are given in Table 2.5 .

In the experimental setup, the controller is implemented in TMS320F28335 Texas instruments DSP [27]. The block diagram of the Matlab Simulink file of the controller implemented in TMS320F28335 is shown in Appendix E. Sampling is carried out at 20 kHz while the inverter is switched at 10 kHz (Double update PWM). A detailed explanation of the experimental setup is given in Appendix F.

Simulations are carried out to show the effectiveness of the proposed *LCL*-filter design. All the power factor variation scenarios described by Table 2.3 were simulated and the THD of each design is noted. It is clear for a given resonance frequency that higher power factor variations can accommodate smaller inductances in the case of *LCL*-filter and still inject currents to the grid with the THD<5%(based on *IEEE* limitations).Figure 2.9, shows a half a cycle of grid-injected current of all the five scenarios described. It confirms poor attenuation of high frequency switching harmonics with smaller inductances but it is still capable of maintaining the required THD level demanded by *IEEE* harmonics limitation standards. For higher power factor operation, the need to increase the inductance is a must.

It is a time consuming activity to experimentally implement all the cases presented in Table 2.3 as it requires 30 inductors (6 inductors per 3-phase system). Therefore, only case 1 is considered in which least reactive power is produced. The designed inductors are implemented based on the guidelines provided by magnetic inc[26]. *KoolMu* magnetic powder material is used for the implementation due to the low cost and core losses compared to the other magnetic materials available in the market [26]. Magnetic manufacturers identify cores based on the energy handing capability (E) of the core for a given dimension. It is given by $E=LI_pI_{rms}$, where L is the required inductance and I_p , I_{rms} are the peak and rms values of grid-injected current.

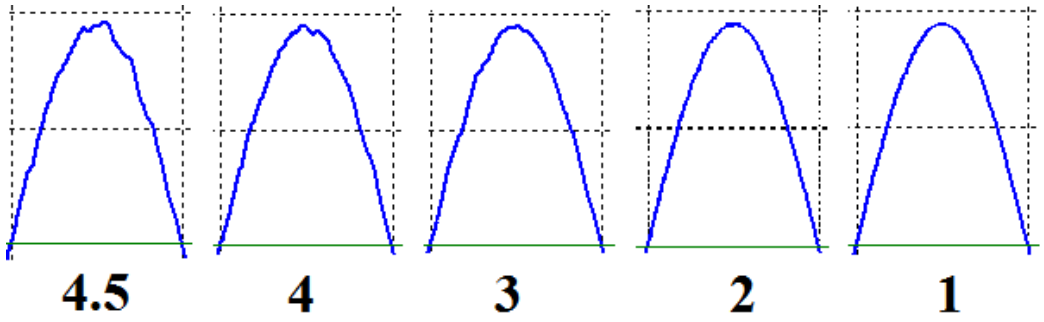


Figure 2.9 Half cycle of grid-injected current (Switching components diminishes with increase in L_T), where 4.5-1 refer to % of power factor variation.

A detailed information of inductor design can be found in [26]. Chapter 4 of this thesis provides a guidance in selecting a magnetic material for an inductor and the inductor behaviour when excited with pulse width modulation VSI is also demonstrated. E-core type *K8020E* is used for the implementation while the wire size *AWG* 13 is selected to handle the maximum rated grid injected current 13.85 A. All the

Figure 2.10 Implemented inductors using KoolMu-E cores

six inductors are wound carefully to realize equal inductance. Figure 2.10 shows one of the implemented inductors. Each inductor occupies a space of 360 cm^3 reducing the overall space requirement by almost 1/3 compared to ferrite based cores [26]. The entire experimental setup is shown in Figure 2.11.

Figure 2.12(a) and Figure 2.12(b) shows the inverter-side current from simulations and real time implementation captured using Yokogawa DL850EV ScopeCoder. High frequency switching ripple is visible in both. An amplified view of the switching component of the grid injected current is shown in Figure 2.13. These high frequency switching components contribute to the instantaneous core losses in the inductor and detailed analysis of determining these losses is given in [28]. Figure 2.14(a) and Figure 2.14(b) shows the grid injected current with a THD of 0.56% in simulations and 2% experimentally. THD plots of simulation and experimental setup (captured using PX8000) are shown in Figure 2.15(a) and Figure 2.15(b). Both simulation and experimental results confirms that the filter meets the harmonic attenuation limits defined by IEEE and the overall THD is less than the 5%.

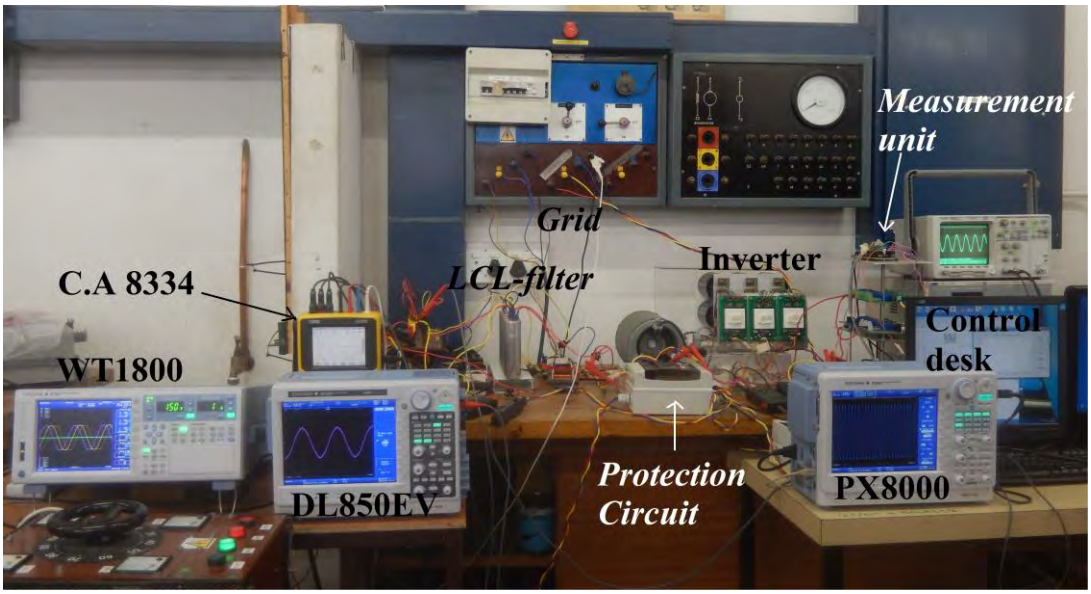
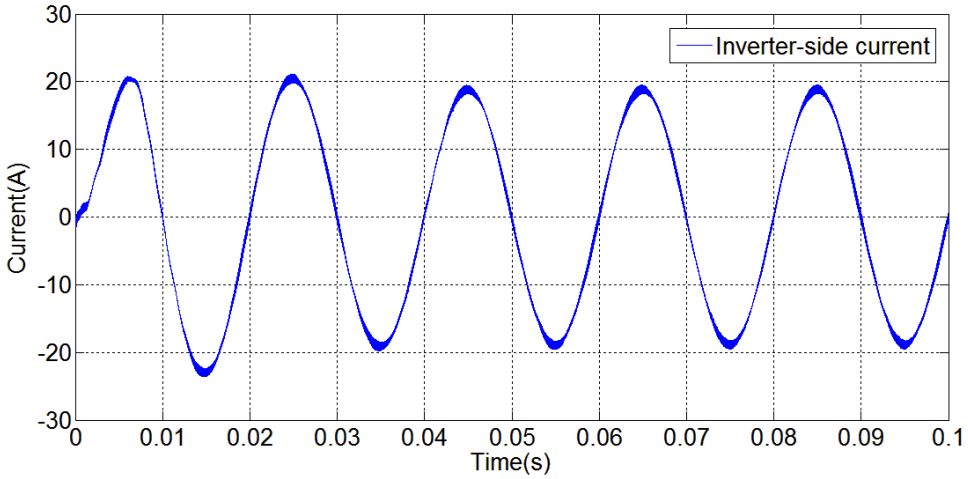
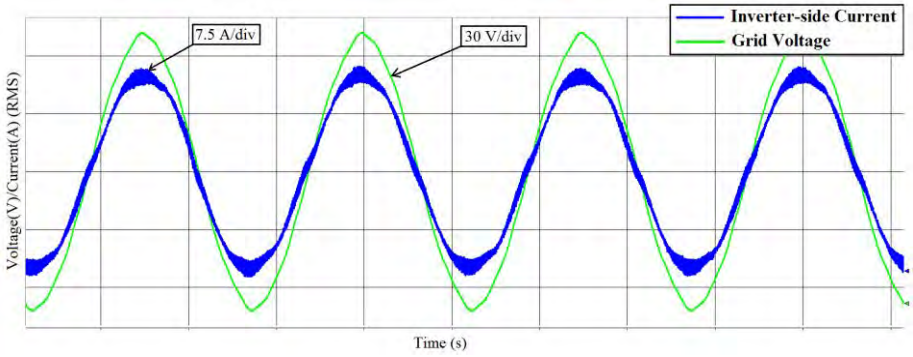


Figure 2.11 Experimental prototype



(a)



(b)

Figure 2.12 Inverter-side current, (a) simulations, (b) experimental

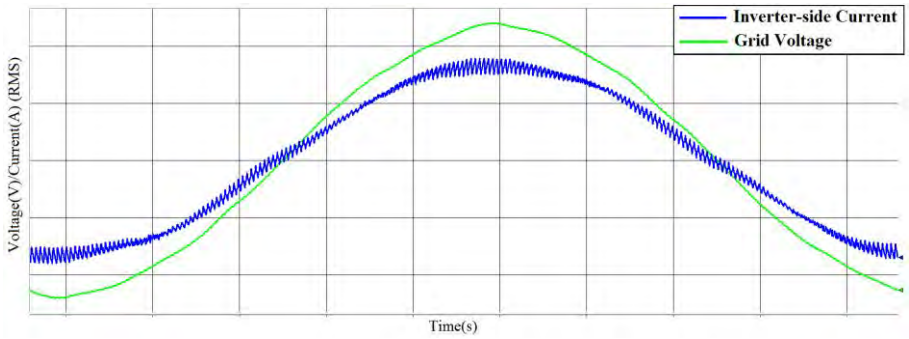
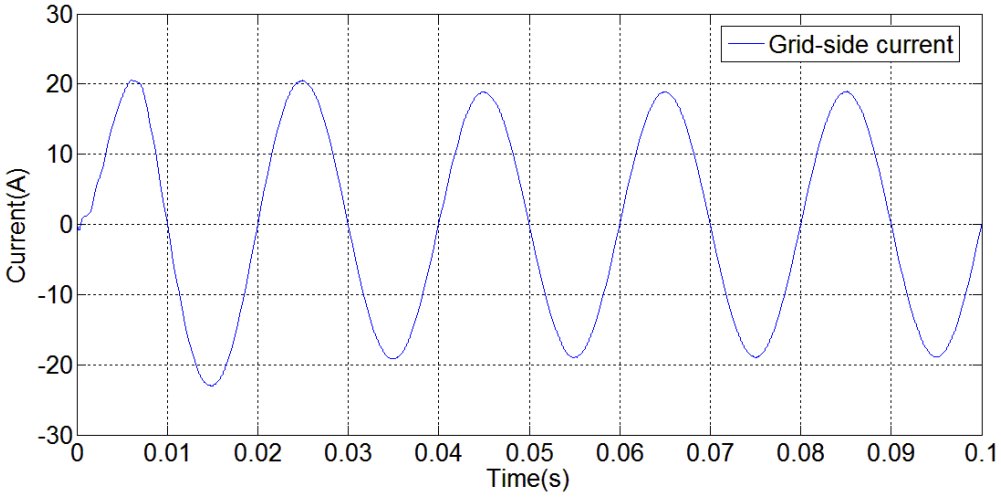
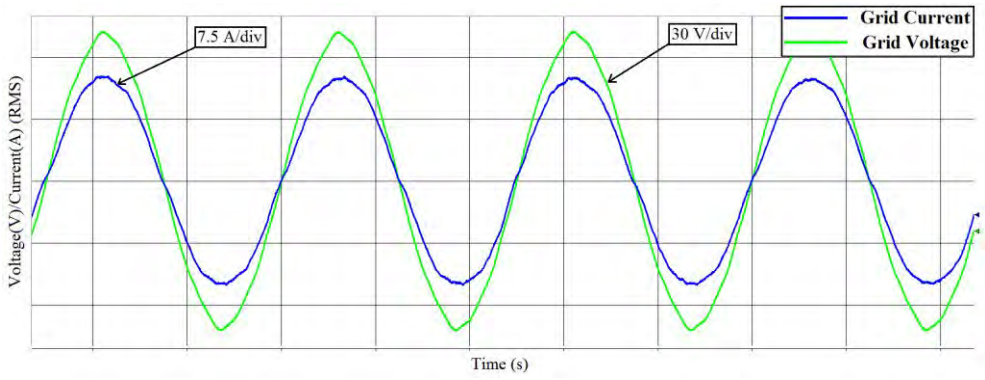


Figure 2.13 Amplified view of the inverter-side current (experimental)

Furthermore, Yokogawa PX8000 was used to measure the power loss across each inductor and the total loss across entire *LCL*-filter including losses in the damping branch is measured using Yokogawa WT1800. Measured losses are listed in Table 2.5 . Furthermore, the inverter operates with a power factor of 0.99, measured using C.A



(a)

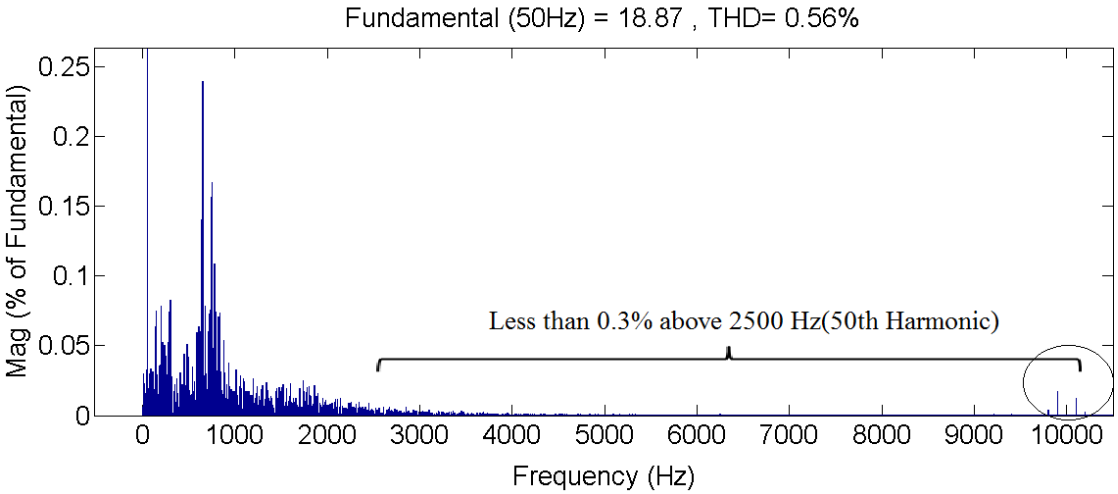


(b)

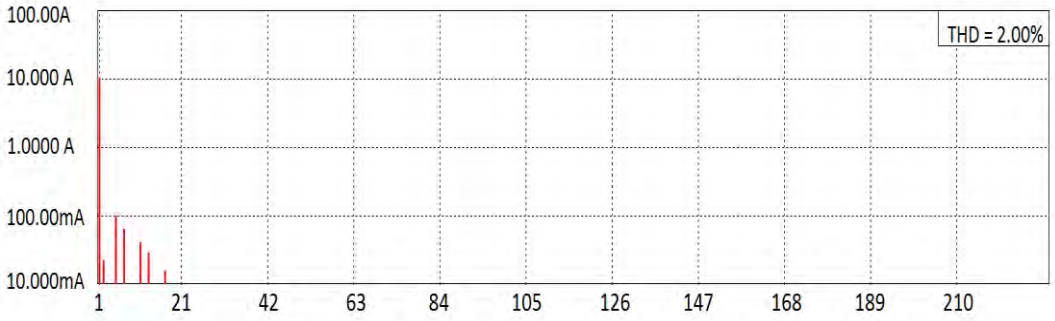
Figure 2.14 Grid-side current and grid-side voltage

8334 Power & Quality Analyzer which agrees with the initially estimated value of 1% or the limit on the reactive power produced by the *LCL*-filter capacitor.

Figure 2.16 shows the thermal image of the one of the design inductor captured using Testo 882 thermal imager. Figure 2.17 shows the temperature distribution along the x-axis, y-axis as seen from Figure 2.16. Temperature analysis performed using testo IRSoft confirms the uniform heat distribution in the designed inductor and the maximum reported temperature is 42.5 ^{0}C and on average around 39.8 ^{0}C. Temperature stability of an inductor is very important as it can reduce the cooling requirements of the inverter system and improve the reliability of the *LCL*-filter.



(a)



(b)

Figure 2.15 THD plot of grid injected current. (a)-Matlab Simulations, (b)- Captured using PX8000 up to 210 harmonic

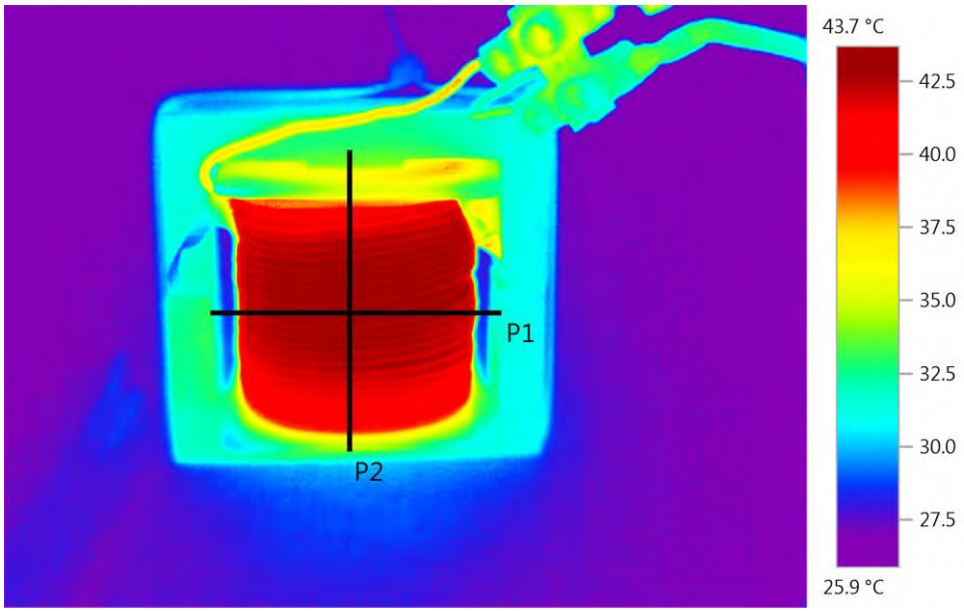


Figure 2.16 Thermal Image of the designed inductor

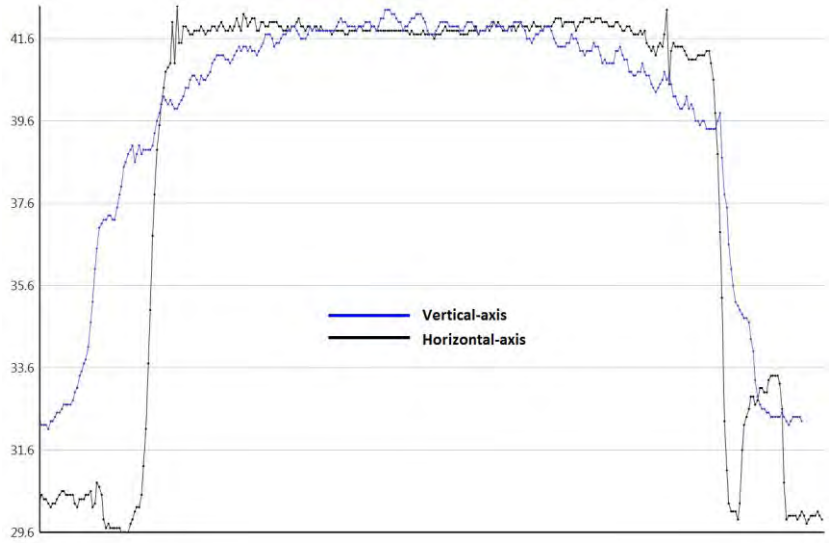


Figure 2.17 Temperature distribution across the x-axis and y-axis of the inductor shown in Figure 2.16

2.5 Conclusion

This chapter highlighted the importance of various design parameters and interrelationships in realizing an efficient *LCL*-filter. Selection of appropriate ratio μ between the grid-side and inverter-side inductors and the resonance frequency selection are deciding factors in realizing an optimized filter. μ=1 is a key variable value that can contribute to an improved *LCL*-filter when compared with other values of μ. The average value k (f_{sw}/f_{res}) should be selected to result in an optimum *LCL*-filter in terms of passive damping losses, attenuation of higher order harmonics, minimum stored energy and small passive component size. Furthermore, the design complies with the limitations on reactive power production by the filter and also harmonic attenuation limits imposed by IEEE-519. The proposed design method is simple and systematic. It considers all the variable factors in determining the performance of an *LCL*-filter and results in an efficient and optimum *LCL*-filter as validated by both simulations and experimental results.

3 Chapter 3

Optimum operating point of an *LCL*-filter (Design-Two)

Chapter 2 presented a method to design an *LCL*-filter by considering the importance of the ratio between the grid-side and inverter-side inductors, resonance frequency, reactive power production and attenuation of higher order harmonics. This chapter presents another *LCL*-filter design or an optimum operating point of an *LCL*-filter by considering the limits of passive components in an *LCL*-filter. Passive component limits are derived based on:

- Reactive power production limits based on the controller operation.
- Based on the IEEE-519 harmonic limitations
- Based on the anticipated switching losses

It is shown that there are infinite solutions to an *LCL*-filter design which satisfy the above mentioned benchmarks. Analysis identifies one of the optimum *LCL*-filter design which results in minimum inductance for a given reactive power production limit that satisfies the IEEE-519 harmonic limitations.

Section 3.1 presents per unit *LCL*-filter parameter derivation to generalise the design for different power ratings. Section 3.2 discusses the limit on reactive power production while section 3.3 defines the limits of total inductance and capacitance based on reactive power production limit. Section 3.4 identifies the maximum limit of inductance irrespective of the type of filter employed while section 3.5 presents the derivation of optimum operating point of an *LCL*-filter. This particular operating point which results in minimum inductance is verified by simulations in Matlab/Simulink and validated experimentally via a 3-kVA hardware prototype under section 3.6 and 3.7. Appendix B and C provides details of derivations of key equations used in this chapter.

3.1 Per unit derivation of *LCL*-filter parameters

Per unit derivation of filter passive components are considered in this chapter to generalize the design for wide range of power levels and to make sure that the design procedure complies with the ratings of the grid power system where most impedances are expressed in per unit basis. For a unity system (2.6) becomes (3.1) [2]:

$$l_T c = \left(\frac{f_b}{f_{res}}\right)^2 \frac{(1+\mu)^2}{\mu} \tag{3.1}$$

Where l_T is the per unit total inductance, $l_T = 2\pi f_b L_T / Z_b$, c is per unit capacitance, $c = 2\pi f_b C Z_b$, the base impedance of the system, $Z_b = V_{l\_l}^2 / P_b$, f_b=f_g, where f_g is the grid operating frequency, V_{l_l} line to line RMS grid voltage, P_b , base power and P_b=P_r, where P_r is the rated active power.

Chapter 2 showed the importance of selecting μ=1. Therefore μ=1 is used in this analysis to further evaluate the limit on reactive power, maximum and minimum inductance requirements.

3.2 Limit on reactive power (q)

If the active power of the inverter is given by p and the reactive power by q, the power factor (P_f) of the inverter output will be:

$$P_f = \frac{real\ power}{apparent\ power} = \frac{p}{\sqrt{p^2+q^2}} \tag{3.2}$$

The inverter overrating is given by the apparent power of the inverter and increase in apparent power will reduce the power factor and overrate the inverter according to (3.2). For an inverter operating at unity power factor, per unit maximum active power will be one (p=*1)*. Minimum limit on the reactive power production will determine the maximum power factor operation of the inverter.

$$P_{f\_max} = \frac{1}{\sqrt{1+q_{min}^2}} \tag{3.3}$$

It is recommended that the operating power factor should be closer to unity in most grid-connected applications [2],[6]. Hence, the filter is designed such that it doesn't exceed a specified limit of reactive power chosen by the designer (q_{min}).

3.3 Limits of total inductance and capacitance requirement

The choice of total inductance is dependent on:

- Reactive power compensation limit (power factor of the device as a whole)
- Harmonic attenuation demanded by IEEE standards
- Voltage drop across the filter

Initially it will show how setting a limit on reactive power will define the limits on capacitance and inductance of the designed filter.

Inclusion of a capacitor in the *LCL*-filter will alter the control system depending on the position of voltage and current sensing. In other words, the inverter needs to compensate the reactive power produced by the capacitor to operate with unity power factor at PCC [6]. In literature, many designs consider the amount of reactive power compensated as a percentage of base capacitance as explained in Chapter 2 of this thesis (maximum of 5%)[6][10]. In this thesis, a mathematical equation is derived based on the control structure to determine the inductance and capacitance limits. Since most of the inverters operate by sensing grid voltage and controlling grid current, here derivation of reactive power is based on it. A similar approach can be used for other control scenarios as proved in [6]. The output power of the inverter (p) expressed in per unit with active power injected by the converter is 1 p.u is given by (3.4):

$$p \approx 1 - j\left[l_T - c\right] \tag{3.4}$$

Derivation of (3.4) is given in Appendix C. Where l_T is the per unit total inductance. The per unit reactive power of the inverter can be deduced from (3.4) as

$$q \approx \left[l_T - c\right] \tag{3.5}$$

In order to avoid the increase in the rating of the inverter, given by (3.2) or drop in power factor, given by (3.3) due to reactive power production, reactive component of the filter should be theoretically zero. This is practically impossible as it will result in higher values of inductances which will take away the primary advantage offered by the low inductance of *LCL*-filters when compared with *L*-filters. This issue is addressed in this research by selecting the parameter *c* as small as possible (*c* limits the reactive power production) and parameter *l* as high as possible to preserve the minimum limitation on reactive power compensated without over rating the inverter too much. This design methodology will determine the first limit on inductance based on reactive power produced. Minimum limitation on *q* can be set by selecting minimum $c(c_{min})$ and maximum $l_T(l_{Tmax1})$ to ensure desired reactive power compensation.

$$q_{\min} \approx \left[l_{T\max 1} - c_{\min} \right] \tag{3.6}$$

Substituting (3.6) in (3.1) results in

$$\left(l_{T\max 1} - q_{\min} \right) l_{T\max 1} = \left(\frac{f_b}{f_{res}} \right)^2 \frac{(1+\mu)^2}{\mu} = 0 \tag{3.7}$$

(3.7) simplifies to

$$l_{T\max 1}^2 - q_{\min} l_{T\max 1} - k^2 \left(\frac{f_b}{f_{sw}} \right)^2 \frac{(1+\mu)^2}{\mu} = 0 \tag{3.8}$$

(3.8) takes the form of a first order quadratic equation. Solving for l_{Tmax1} will result in two values for total maximum inductance, where the negative value can be ignored as the resulting value is very small and inductance is a positive parameter. Positive l_{Tmax1} defines the first limitation on the total filter inductance requirement. The value of l_{Tmax1} may not necessarily satisfy the harmonic attenuations criterion defined in IEEE-519 standard. Therefore, the role of total inductance in harmonic attenuation needs to be further evaluated.

The second limitation criterion on total inductance requirement is based on the IEEE 519 standard for harmonic limitation [21]. (2.31) is used here:

$$l_{Tmin} = \frac{1}{h_{sw}\left|\frac{i_{pu}(h)}{v_{pu}(h)}\right|\cdot|1-k^2|} \qquad 3.9$$

It is important to notice that the l_{Tmin} will decrease with increase of k or with the drop of resonance frequency ($k=f_{sw}/f_{res}$) according to (3.9). Therefore, l_{Tmin} defines a minimum limit on total inductance based on IEEE-519 harmonic standards; the other limits depend on the reactive power compensation at the point of common coupling (PCC) as shown above and the dc bus availability as shown in section 3.4.

The variation of the l_{Tmin} and l_{Tmax1} against the variation of k for the system parameters listed in Table 3.1 is shown in Figure 3.1, assuming the minimum reactive power compensated ($q_{min}=0.05$) by the filter remains constant and $\mu=1$ is considered. Total inductance (l_T) should be either l_{Tmin} and l_{Tmax1}, whichever is highest depending on the resonance frequency (ratio k).

$$l_T = max\{l_{Tmin}, l_{Tmax1}\} \qquad 3.10$$

It can be concluded from the Figure 3.1. When $\mu=1$ the variation of l_{Tmax1} is more dominant than l_{Tmin} as the k increase (resonance frequency decrease).

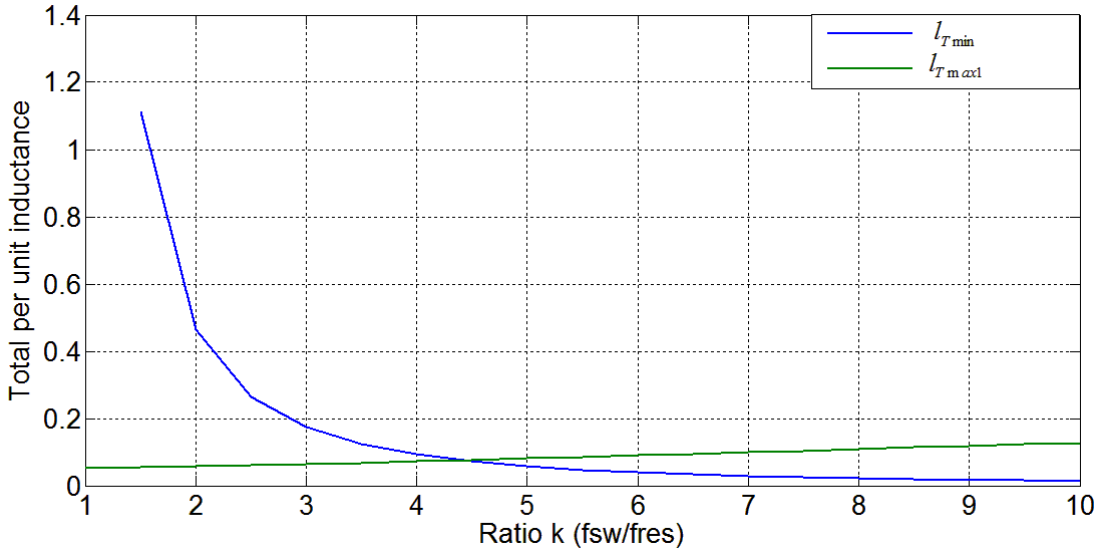


Figure 3.1 Total inductance (mH) Vs Ratio k

Table 3.1 Parameters for Evaluation of the *LCL*-filter Design

Parameter	Value
Rated Power (P_r)	3 kW
Grid Voltage RMS (V_{l_l})	75V
DC link voltage	250 V
Grid frequency (f_g)	50 Hz
Switching frequency (f_{sw})	10 kHz
Sampling frequency (f_s)	20 kHz
Base impedance (Z_b)	5.6250 Ω
Resonance frequency (f_{res})	2.272 KHz
Minimum reactive power q_{min}	0.05
Ratio $\mu(L_i/L_g)$	1
Ratio k	4.40
Inductance, l_T / L_T	0.0756/1.3539 mH
Capacitance, c/ C	0.0256/14.5μF
v_{pu}	0.8333
i_{pu}	0.003
R_d	1.7 Ω
af	18.856
K_{p_pu}	0.584
K_{I_pu}	250
l_{Tmax}(0.1pu) or L_{Tmax}	1.790 mH
Copper wire size(diameter)	1.80 mm
Number of Turns	56
Core Geometry	00K130LE026

Generally, designers want to minimize the inductance due to the bulky nature and space requirements. However, it is important to understand what determines the maximum amount of inductance allowed in a filter connected to an inverter irrespective of the type of the filter utilized. It is guided by the dc bus availability in the inverter system.

3.4 Maximum limit of total inductance requirement

The maximum limit of L_T (l_{Tmax2}) irrespective of the filter type will be based on the ac voltage drop across the total inductance during the inverter operation and anticipated switching losses. Figure 3.2 shows the vector representation of voltage drop in an inverter system. Where I_g and V_g are grid injected current and grid voltage, respectively while V_d is the voltage drop across the total inductance of the filter and V_i is the apparent voltage of the inverter. It is always advisable to minimize V_d ($\approx 2\pi f_g L_T I_g$) by reducing L_T to minimize the dc bus requirement, because for an ideal

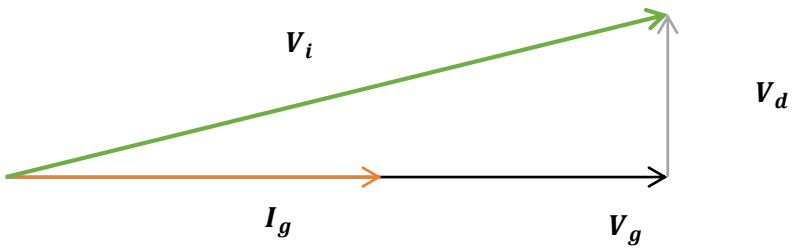


Figure 3.2 Vector representation of voltage drop in an inverter system

system the dc bus should be at least equal to $2V_{gpk}$(for bipolar PWM), where V_{gpk} is the peak grid voltage. However due to V_d, it should be large enough to compensate for the voltage drop [6] to ensure the current controllability of the inverter and to improve the robustness [6][29]. For example an inverter with 0.2 p.u total inductance (l_T) and the grid current (I_g) is in phase with the grid voltage (V_g) and both are 1 p.u. The voltage drop (V_d) of $V_d = j2\pi f l_T I_g$= 0.2 per unit (p.u) is expected. This will result in 1.02 p.u voltage across the inverter (V_i). Therefore, it is a must to increase the dc bus value to maintain proper operation of the inverter. However, higher dc bus values give rise to higher switching losses. In order to minimize switching losses, l_T is limited to 0.1 pu in grid connected VSI [5]. But these requirements may vary with STATCOM and inverters that operate with different power factors. The variation of the l_T of an *LCL*-filter of a grid-connected inverter should be within the range.

$$\boldsymbol{max}\{\boldsymbol{l_{Tmin}}, \boldsymbol{l_{Tmax1}}\} \leq \boldsymbol{l_T} < \boldsymbol{l_{Tmax2}} \qquad 3.11$$

According to the above inequality, there will be a large number of solutions for l_T of an *LCL*-filter for a given μ (=*1)* and q_{min} limit as shown by the shaded area of Figure 3.3. The selected l_T will always comply with the initially anticipated reactive power compensation limit, IEEE-519 harmonic attenuation limit and moderate switching losses. It is also important to notice that there is a range of ratio k (resonance frequencies) that can occupy the solution range. Any increase in l_T within the solution region will favourably reduce the initially anticipated reactive power and improve the harmonic attenuation level. Optimizing l_T within this range will depend on the significance of copper and core (eddy current and hysteresis) losses in the practically designed inductor [11]and the losses in the damping scheme implemented [2],[3].

Therefore, the optimization based on losses will be a multi-objective optimization problem which needs the attention of researchers. The section below will detail out the step by step procedure in realizing one of the optimum operating points of an *LCL*-filter.

3.5 *LCL*-filter design

The parameter limitations derived above can be used to realize an optimum operating point of an *LCL*-filter for grid-connected VSI. Initially, the ratio, $\mu=1$ is selected due to the advantages mentioned above. Reactive power compensated by the filter (in (3.8)) is limited to, $q_{min}=0.05$ and harmonic limits on (3.9) are based on IEEE-519 [21]. For these three requirements, there are infinite total inductance values and resonance frequencies that can satisfy the design requirements as seen from Figure 3.3. It is always preferable to minimize inductance due to the advantages mentioned above in section 3.4. Therefore, in this chapter as seen from Figure 3.3 (for optimum operating point), there is a specific resonance frequency that meets the minimum total inductance requirements while maintaining the given (q_{min}) reactive power production limit.

Once the minimum inductance is identified, minimum value of capacitance can be calculated using (3.5). Per unit and the nominal values of the total inductance and the capacitance are given in Table 3.1 for the given system parameters. Furthermore, the calculated capacitance value of the filter is 2.56% of the base capacitance

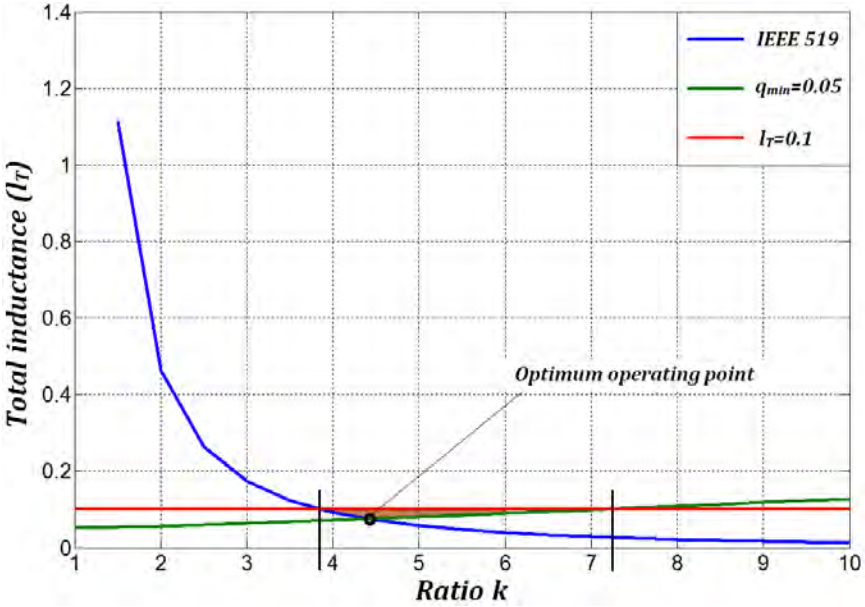


Figure 3.3 Variation of total inductance requirement Vs Ratio *k* for a given μ (μ =1)

($C_b=1/2\pi f_g Z_b=0.565mF$), which is an acceptable design criteria. Therefore, the above design identifies one of the important operating points ($k=4.40$, when $\mu=1$) of the *LCL*-filter which results in minimum inductance. In addition to the minimum inductance, an average value of k is realised. As shown in chapter 2 an average value of k results in an optimum filter in terms of THD, passive damping losses, stored energy and passive component size. This particular operating point is validated using Matlab simulations and experimental prototype.

3.6 Simulation Results

Three-phase VSI with *LCL*-filter is simulated in Matlab simulink environment where the proportional integral (PI) controller is used to regulate the grid injected current [12]. The controller implementation is similar to previous design where the calculated *p.u* gains for the given system parameters are given in Table 3.1. Figure 3.4 shows the grid injected current of a single phase of a 3ϕ VSI where the THD is 1.2% and the magnitude of the switching component is 0.2% of the fundamental current. It is below the THD requirements defined by IEEE-519 harmonic limitations as the switching component should be less than 0.3% for harmonics above 50 [21].

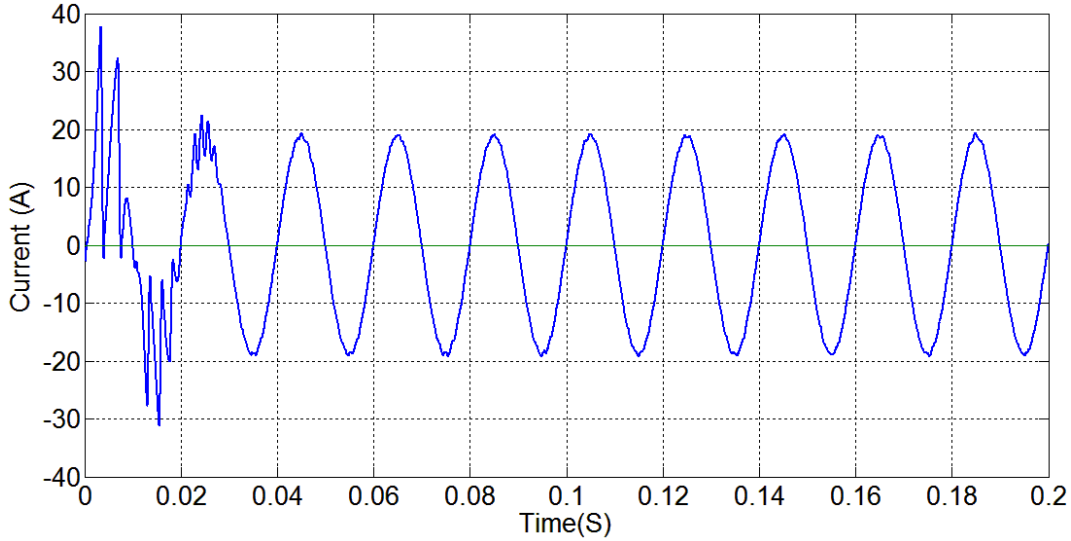


Figure 3.4 Grid-injected current for the inverter with parameters listed in Table 3.1

3.7 Experimental Verification

The proposed filter design is verified by a 3-kVA grid interface VSI hardware prototype which has been used for the previous design presented in Chapter 2 of this thesis. The inverter ratings are listed in Table 3.1. Passive damping is preferred due to the ease of implementation of the control structure. Inverter-side and grid-side

inductors are implemented using KoolMu powder material which has a saturation flux density of 1 Tesla [26]. E-core geometry is preferred due to the ease of winding over other core geometries like toroids. Inductors are designed according to the guidelines provided by the magnetic manufacturers [26]. The parameters of the implemented inductor are also listed in Table 3.1. *LCL*-filter is shown in Figure 3.5. KoolMu core "00K130LE026" is used for the implementation [26]. Larger core structures are used to minimize the core and the copper losses of the entire filter at the expense of large volume. As mentioned earlier, optimization strategies can be used to reduce the volume, losses of the entire filter [11], which is out of the scope of this research.

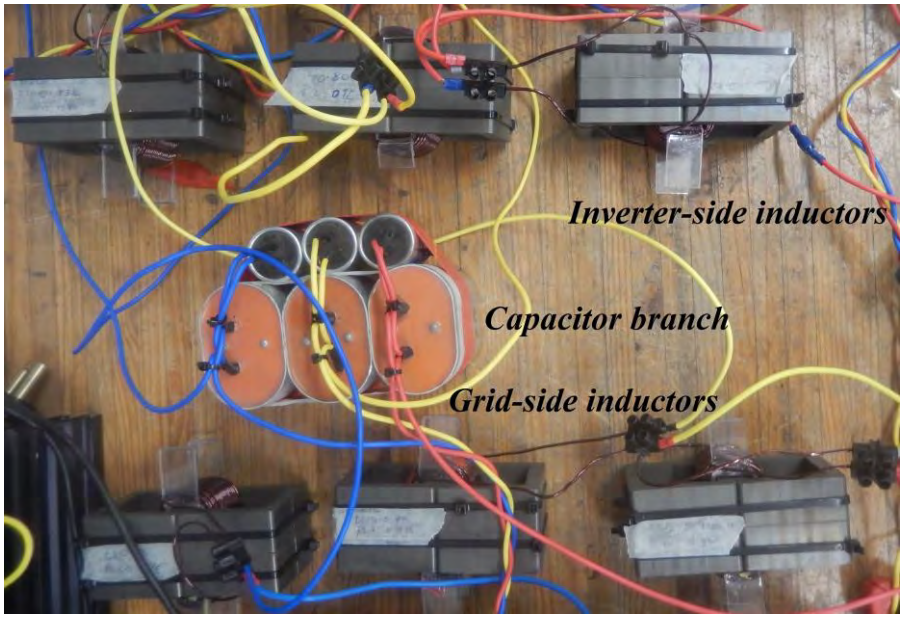


Figure 3.5 Implemented *LCL*-filter

The inverter-side and grid-side currents at rated operating conditions are captured using Yokogawa DL850EV ScopeCoder and shown in Figure 3.6 (a) and (b), respectively. The grid voltage is also shown in both waveforms as well. The large current ripple is visible from the inverter-side current waveform which consists of the high frequency switching components as observed from the THD plot of inverter-side current shown in Figure 3.7 (a) captured using Yokogawa PX8000. In addition to switching ripple frequency, higher order harmonic components are also present which need filtering to meet IEEE-519 harmonic limitations [21]. These harmonic components are successfully attenuated by the *LCL*-filter with the proposed minimum inductance to meet IEEE-519 harmonic limitations as shown by the THD (=4.00%) plot of the grid-side current shown in Figure 3.7 (b).

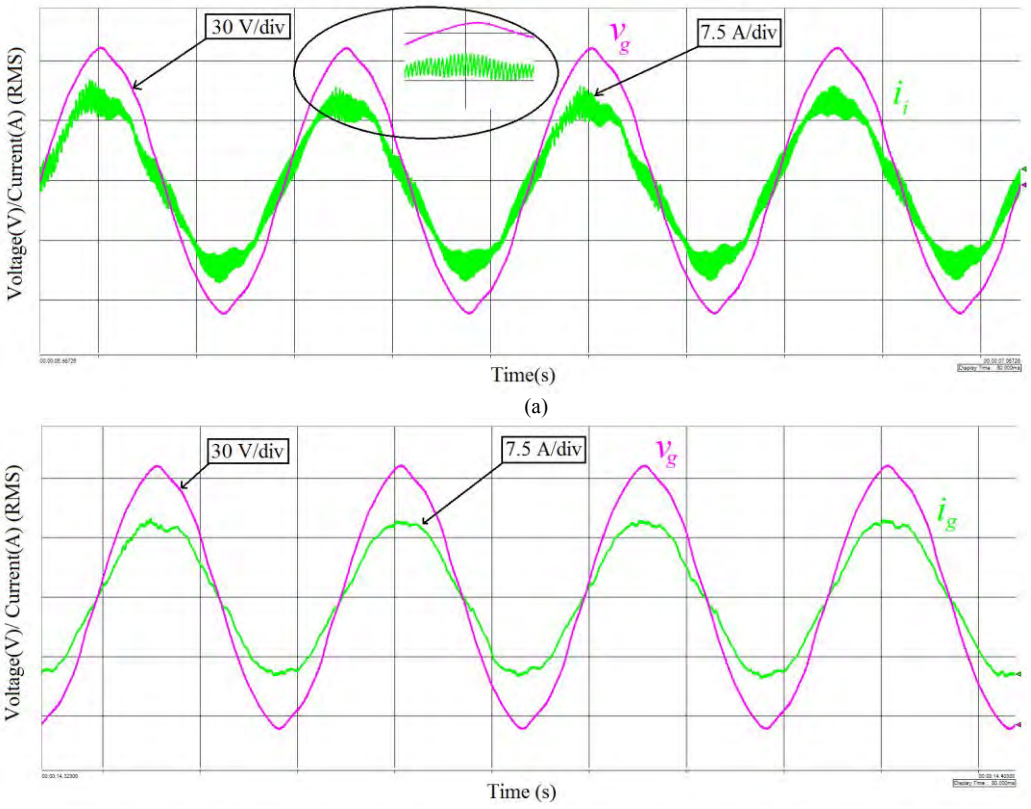


Figure 3.6 (a) inverter-side (i_i) and (b) grid-side current (i_g) waveforms

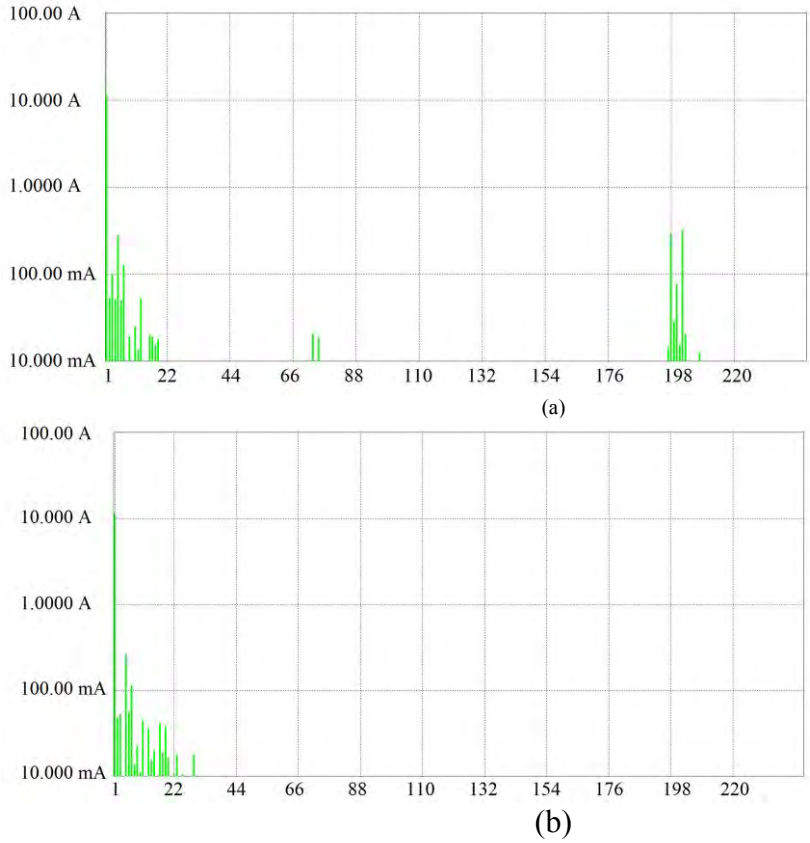


Figure 3.7 (a) THD spectrum of inverter-side and (b) grid-side current

3.8 Conclusion

LCL-filter parameter limits and their ranges that are critical for the proper operation of a grid-connected three-phase inverter are analyzed in this chapter. Analysis identifies the reactive compensation limit, the level of required attenuation of harmonics defined by IEEE-519 standard, maximum allowable voltage drop across the filter to limit switching losses of the inverter and the proper ratio between the grid-side and inverter-side inductance as the critical design requirements that can lay the foundation to an optimum *LCL*-filter design algorithm. An optimum operating point based on minimum inductance requirements is presented and it corresponds to a specific resonance frequency. Analysis can also be used as a guidance to minimize the iterations in *LCL*-filter design algorithms and to optimize the filter design process based on the application.

4 Chapter 4

Inductor Modelling for a Grid-Connected Three-Phase Inverter Using Sendust Powder Cores

Inductor design for grid-connected voltage source inverter (VSI) is an important step in realizing an efficient and optimized filter. Even though, ferrite material based inductor designing and issues related to it are deeply addressed in literatures, there is hardly any research on utilization of other magnetic materials for inductor design for filters connected to VSI. This chapter compares the suitability of the state of the art magnetic materials for inductors in VSI.

Section 4.2 justifies the selection of Sendust with a comparative analysis on the other magnetic materials available in the market. Section 4.3 analyzes the designed inductors in ANSYS Maxwell/Simplorer simulation to better understand the saturation behavior, the effect of ac biasing when excited with a sinusoidal PWM. Section 4.4 provides the experimental results of the implemented inductor's behavior when biased at the rated operating conditions.

4.1 Introduction

Recent advancements in material science have facilitated the magnetic core manufacturers to develop different core materials that offer competitive advantages depending on the application under consideration [26][30]. Higher level of saturation flux density, stable operation at higher temperatures and reduced core losses have definitely added a new dimension to the inductor design for power electronic applications.

Grid-connected VSI requires harmonic filters to meet the IEEE-519 standard in harmonic mitigation. These limitations can be addressed by use of filters such as *L*, *LC*, *LCL* and trap filters. Theoretical designs of these filters are well addressed in literatures and also in section 2 and 3 of this thesis with the assumption that the designed value of components perform ideally in hardware applications and there is hardly any consideration about the behavior of these passive components under PWM voltage excitation and the subsequent power losses [11].

Inductors are one of the essential integrated components in harmonic filters. Their performance level directly affects the quality of the power produced and the efficiency of the system. Ferrite material based inductor design and issues related to it are well addressed in the literature [11],[31] but there is hardly any information about the suitability of other magnetic materials for the inductor design for grid-connected VSI. Therefore, this chapter focuses on designing inductors using sendust magnetic material for an *LCL*-filter in grid-connected operation of the VSI.

4.2 Material Selection

Core material selection can be identified as the first step to a successful inductor design. The following parameters characterize a particular core material, in which a designer can select the material based on the design requirements [26];

(1). Permeability of the material

(2). Level of estimated core loss compared to other materials

(3). Relative DC bias capability

(4). Saturation flux density

(5). Curie temperature

(6). Operating temperature range

(7). Stability of permeability with temperature

In addition to the material characteristics, the cost of these materials is a critical design constraint that needs the attention of designers. Table 4.1 shows a comparison of the above mentioned parameters for well-known inductor core materials available in the market [26]. There are different types of ferrite core materials available but only L-type material is considered here for the comparison. Except ferrites, other materials belong to the powder cores family.

The inductance of an inductor is a function of the permeability of the material, which is a function of the biasing current through the inductor. When it comes to powder cores, the initial permeability of the material changes gradually when compared to ferrites. This slow variation in permeability (soft saturation) in powder materials indicates that they saturate slowly but capable of maintaining a certain level of inductance as the biasing/load current increases. But inductors designed with ferrite materials will maintain a constant inductance value, almost closer to the unbiased value until it reaches the saturation limit. At the point of saturation, a sudden drop of

inductance is expected [26]. This phenomenon is shown in Figure 4.1.

In addition to the soft saturation offered by powder materials, they have higher saturation flux density compared to ferrite which provides higher energy storage capability and therefore smaller in volume. Also, in ferrites as the temperature increases there is a considerable drop in saturation flux density and temperature variation becomes a crucial factor in ferrite inductor design to avoid sudden saturation at elevated temperature. On the other hand, powder materials are capable of maintaining constant saturation flux density at an elevated temperature. Furthermore, ferrite materials with high initial permeability occupy an air gap (eg: EE inductor core) to reduce the effective permeability of the material to avoid saturation at high biasing currents [26]. Air-gaps contribute to fringing losses and complicate the inductor designing as the estimation of fringing losses are not straightforward [31]. In addition to the losses, fringing flux can interact with the winding of the core to increase the eddy currents in it. Most of the powder materials however inherit low permeability due to distributed air gap in the core as seen from the Table 4.1 and do not require any air gaps in the inductor design, which eliminates the fringing losses and gap EMI effects [26][31].

Based on the information analyzed above, cores made up of powder materials are preferred over ferrites to investigate their suitability and behavior in grid-connected inverter application.

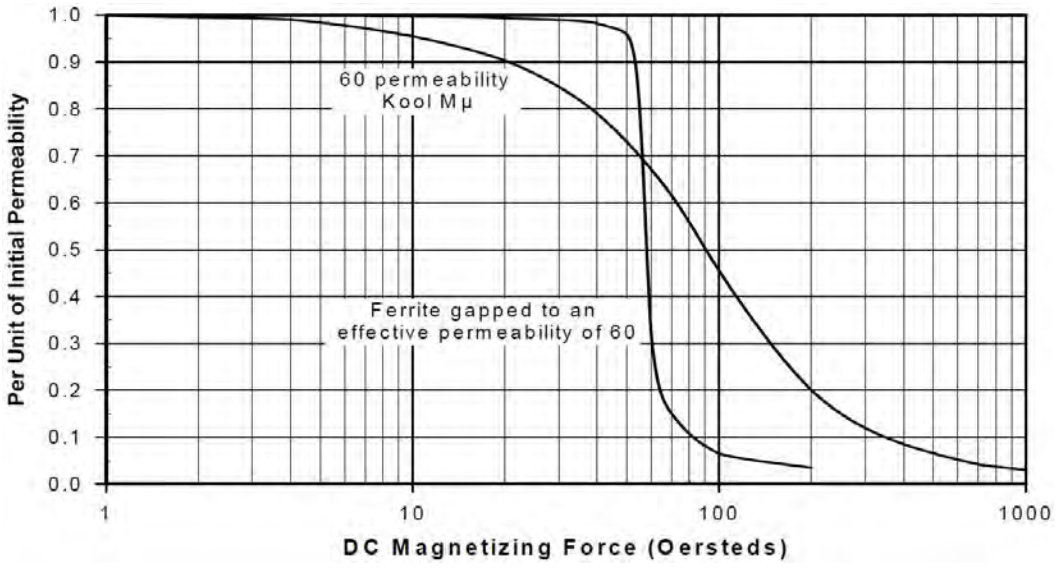


Figure 4.1 Variation of permeability in KoolMu(soft saturation Magnetic material) and ferrite material [26].

Inductors for grid-connected VSI have almost negligible dc component and inductors are designed to handle AC current. Therefore, core losses become a dominant factor in designing the inductors. According to the information given in Table 4.1, MPP, KoolMu and Amoflux have the least core losses. But when considering the saturation flux density, temperature stability and the cost, KoolMu becomes a perfect candidate for inductors in filters for inverter systems. This chapter analyzes the design of inductors with KoolMu material for grid-connected VSI. Inductor parameters of the *LCL*-filter presented in chapter 2 is considered in this chapter for further evaluation. Inductors are designed according to the guidelines provided by manufacturers [26]. All the key parameters are listed in Table 4.2.

Magnetic behavior of inductors designed using powder materials are rarely studied in literatures. In this section, the study of such inductors is done using ANSYS Maxwell and Simplorer to better understand their behavior under PWM switching.

Table 4.1 Magnetic Core Material Properties [2]

	Kool Mu	**MPP**	**High Flux**	**XFlux**	**AmoF lux**	**Powder**	**Ferrites (*L* material)**
Permeability	14-125	14-550	14-160	26-60	60	10-100	900±25 %
AC Core loss	Low	Very Low	Moderate	High	Low	Highest(variable)	Low
DC bias	Good	Better	Best	Best	Better	Good	NA
Saturation flux density(T)	1.0	0.75	1.5	1.6	1.5	1.2-1.4	0.42
Curie Temperature(^{0}C)	500	460	500	700	400	variable	300 ^{0}C
Operating Temperature(^{0}C)	-55~200	-55~200	-55~200	-55~200	-55~155	-55~variable	NA
Cost	Low	High	High	Low	Low	Low	Low

4.3 Inductor Modelling Using Maxwell and Simplorer

Inductor behavior in a filter of a grid-connected VSI is modelled using magnetic simulation software, ANSYS Maxwell. Simplorer package provided by it, helps to evaluate the behavior of magnetic components characteristics under the influence of power electronic circuits.

In ANSYS Maxwell, the designer assigns the properties of magnetic materials used for the cores and carryout simulations with it to a higher accuracy. ANSYS Maxwell identifies a particular magnetic material with following parameters: relative permeability, magnetic coercivity, composition and bulk conductivity. First three parameters define the magnetic properties of the material. This information is available from the core manufacturer [26]. In this analysis, KoolMu core material is added to ANSYS Maxwell to evaluate the behavior of the inductor in a harmonic filter.

Table 4.2 System Parameters

Parameters	*Value*
Rated power	3000 W
Rated grid voltage(rms)	75 V
Rated current(rms)	13.85 A
Switching/ Sampling frequencies	10 kHz/20 kHz
Capacitor	6 uF
Grid side/Inverter side inductor	2.10 mH/2.10 mH
KoolMu Core Type	00K8020E040
KoolMu Bobbin Number	00B802001
Number of Turns	145
Thickness of the wire	1.80 mm
DC resistance	0.13 Ω
Total Loss in an inductor	30 W

In Maxwell, transient field simulator is selected as it computes the time-domain magnetic fields in 3D. It is capable of solving magnetic fields, current distribution, and magnetic flux density. Quantities like energy, winding flux linkage, winding induced voltage can be derived from the above mentioned main quantities. Furthermore, it allows excitation of inductors with arbitrary currents and voltage waveforms while nonlinear BH (magnetic flux density (B) and magnetic field strength (H)) material dependencies are allowed. The inductor designed in Maxwell 3D is shown in Figure 4.2, where KoolMu core material is assigned as a new material to the simulator. Drawing copper windings individually is a time consuming process. In practice it is complex to realize a perfect winding therefore the region that occupies copper windings is defined based on the area of the wire intended to be in the design. After defining the area, number of wires that will occupy in the area can be defined.
Inductor can be excited internally by defined voltage waveforms or an external circuit designed in Simplorer or circuit editor available from ANSYS. In this study, inductor was excited externally using Simplorer simulation software.

Figure 4.3 shows the three-phase VSI used to excite the inductor. In which one inductor designed in Maxwell is used for the evaluation instead of 3 inductors for the inverter-side inductor to reduce the computational time. In the simulation setup, Simplorer generates the inductor exciting voltage and inductance is evaluated in Maxwell model at every step size defined in Simplorer.

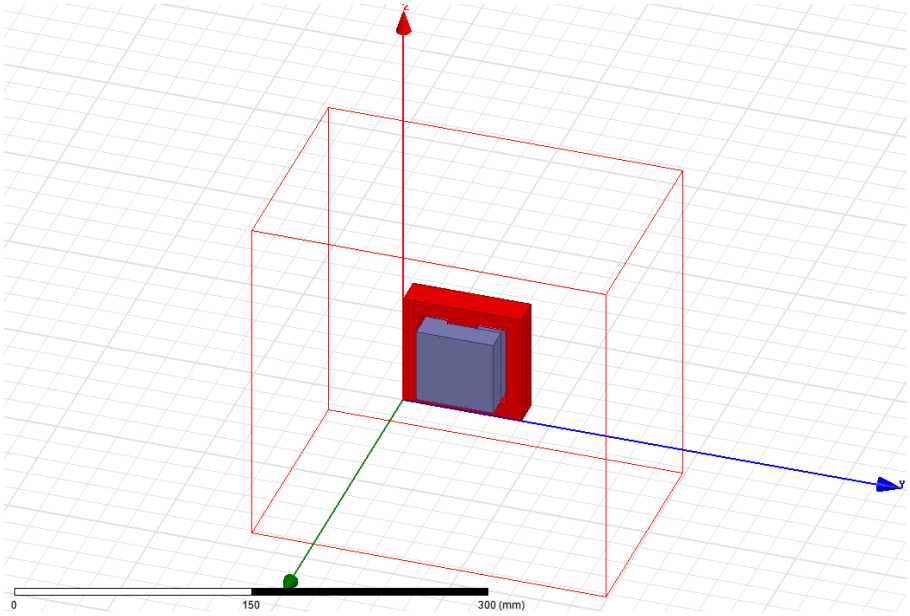


Figure 4.2 EE core inductor designed in Ansoft Maxwell using KoolMu core material

Figure 4.4 shows the current flowing through the winding and the induced voltage across the inductor. Here current flowing through the inductor is matched to the grid-connected inverter (~13.5A, RMS) using the load resistors and sinusoidal PWM with unity modulation index is used for the analysis. Furthermore, Figure 4.5 shows the amplified view of the current flowing through the inductor. It is observed that the high frequency switching does not necessarily take a triangular shape near zero crossing due to the influence of the other phase currents. Therefore, the estimation of high frequency core losses becomes a challenging task [28]. There are methods to estimate copper losses [32] but core losses are calculated based on the implemented inductors as dc pre-magnetization becomes significant in these kind of applications [28]. There is potential to develop core loss maps based on simulation for systems where dc pre-magnetization is significant. Individual loss estimation based on simulations is out of the scope of this research and needs rigorous studies, however losses are measured experimentally to verify the effectiveness of the design as shown in section 4.4.

Figure 4.6 shows the effective inductance of the inductor under sinusoidal current

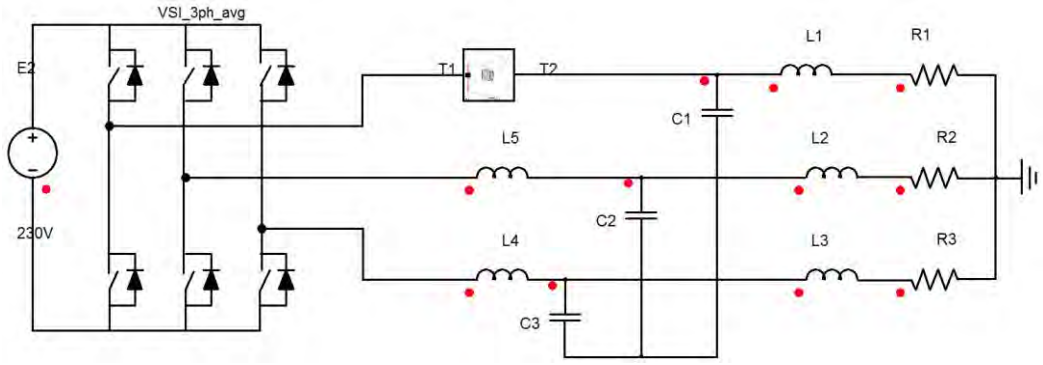


Figure 4.3 Three-phase VSI used for the excitation of the inductor under test

flow. It shows the soft saturation concept of the powder materials as the load current

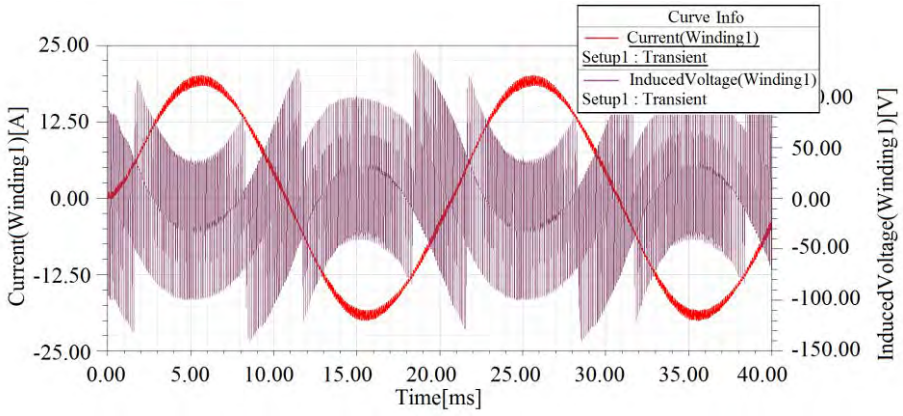


Figure 4.4 Current flowing through and voltage drop across the inductor due to voltage excitation under SPWM

increases as discussed in section 4.2. The inductance of the KoolMu material under low biasing current is around 3.7 mH and drops to 2.4 mH at the peak and 2.7 mH around the RMS value of the rated current.

The soft saturation nature of powder materials can be used for the benefit of inductor design for VSI. There is a minimum inductance that is required to filter high frequency switching components as listed in Table 4.2. Therefore, when designing inductors using powder material, the inductors are designed such that they maintain the minimum inductance requirement at the peak grid injected current level (effective inductance seen by switching components) rather than aiming for a constant inductance as in the case of an inductor designed using ferrites. In this study, minimum inductance at the peak is ensured to obtain the advantage of soft saturation offered by KoolMu material.

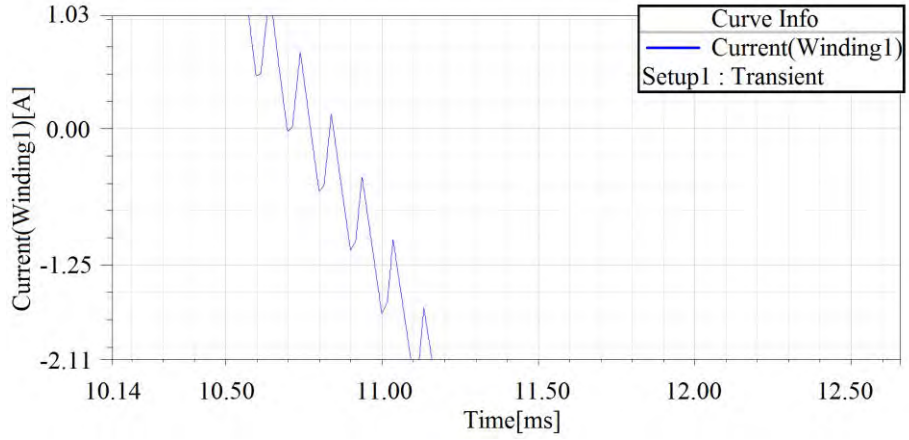


Figure 4.5 Amplified view of the current flowing through the inductor near zero crossing region

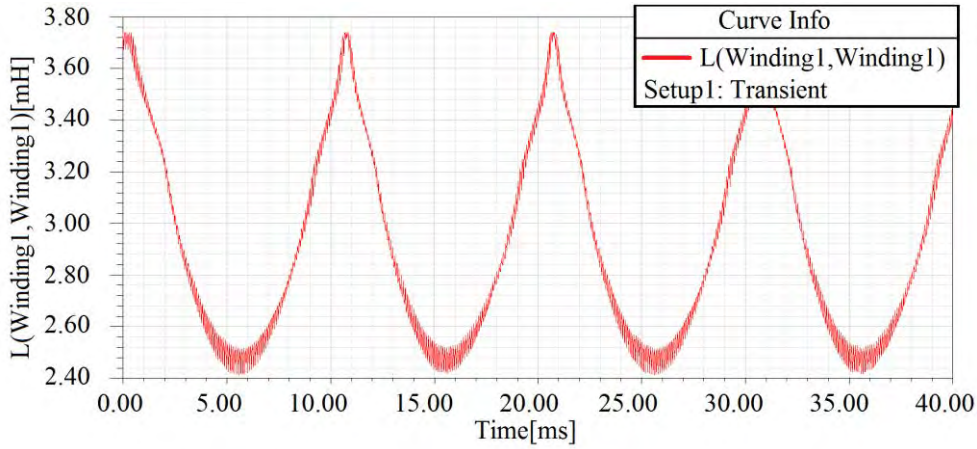


Figure 4.6 Variation of the inductance under varying load currents

4.4 Experimental Results

The experimental system consists of 3kW three-phase VSI connected to the 50 Hz grid through an *LCL*-filter as shown in Figure 2.11. The designed values of the passive components along with the other operating factors are listed in Table 4.2. The inductors are implemented based on the manufacturer guidelines to ensure minimum inductance required at the rated operating conditions [26]. The inductor implemented using KoolMu magnetic material is shown in Figure 2.10. The volume occupied by the inductor is approximately 360 cm^3, resulting in a reduced volume compared to ferrite material based cores [26].

Initially, variation of the inductance with the biasing current is observed. The inductor is connected to a variable sinusoidal voltage source, AE Techron Model LVC 5050 Linear Amplifier, which is used to bias the inductor at a particular sinusoidal current at 50 Hz. Yokogawa high precision power scope PX8000 was used to measure the inductance of the inductor at different biasing currents. The variation of inductance for the designed inductor vs bias currents are shown in Figure 4.7. A gradual drop in inductance with the biasing current highlights the soft saturation nature of the KoolMu material and the effective inductance at the RMS rated grid-injected current is around 2.4 mH. It is difficult to measure the inductance around the peak of the injected current as RMS values are used to compute inductance and inductor windings are designed to carry a current of 13.85 RMS. According to Figure 4.7 and considering the rate of inductance drop, inductance should be around 2.1 mH at the peak of the grid injected

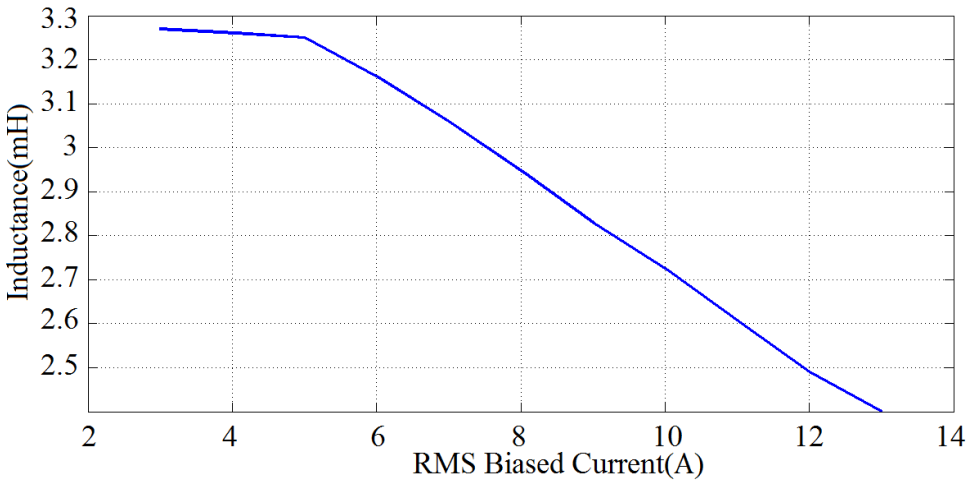


Figure 4.7 Variation of inductance with bias current

current as expected from theoretical calculations. Variation of simulation results from practical are mainly due to the fact that windings are assigned for a region but not drawn individually and actual core parameters may deviate from the parameters assigned in simulation due to tolerances.

The inductors are tested in a VSI connected to the grid. Figure 4.8 shows the current flowing through the inductor connected to the inverter-side and the voltage drop across it. The waveforms are almost similar to one shown in simulations. Power loss (P_L) of an inductor is given by;

$$P_L = P_{copper} + P_{core} \tag{4.1}$$

P_{copper} and P_{core} are copper losses and core losses respectively. Measuring individual losses is a challenging task as detailed in [28][32]. But Yokogawa PX8000 can be used to measure the total average loss during one cycle of low frequency current (50 Hz). The total measured loss of the inductor is around 30 W at rated operating conditions. *LCL*-filter consists of 6 inductors and the total loss across the entire filter is 180 W which constitutes to 6% of power loss across the filter in a 3 kW system. The power loss is mainly due to copper loss as the dc resistance of the inductor is around 0.13 Ω. Losses can be further reduced by adapting an inductor loss optimization strategy as proposed in [11] at the expense of slightly increased core geometry to reduce the copper losses [26]. The temperature stability of the inductors are measured using Testo 882 thermal imager and a maximum temperature of 43.4 ^{0}C recorded in the windings after the system operation for 30 minutes as shown in Figure 2.16.

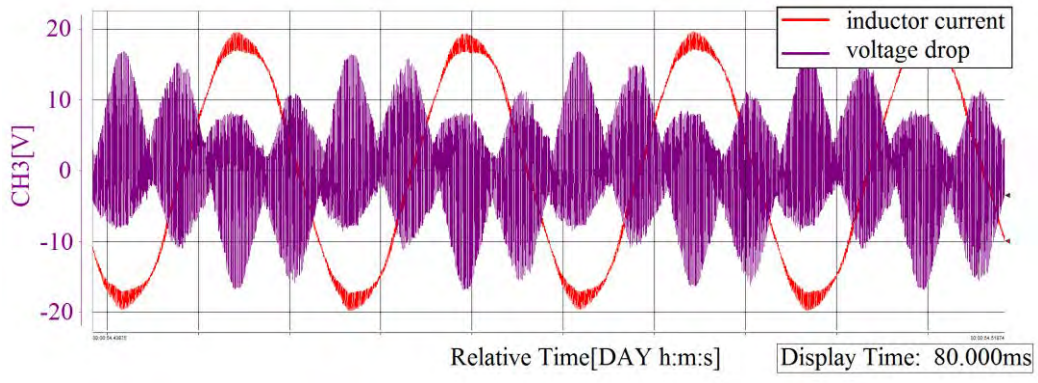


Figure 4.8 Current flowing through and voltage drop across the inductor due to voltage excitation under SPWM at rated operating conditions

4.5 Conclusion

This chapter presented the importance of utilizing KoolMu to design inductors used in grid-connected VSI. The designed inductors are based on manufacturer's guidelines and are simulated in ANSYS Maxwell and Simplorer in order to understand their behavior under PWM applications. Simulated results are justified by experimental results in terms of low losses, temperature stability and reduction in space requirements. For the improvement of reliability of VSI, KoolMu is a good replacement for ferrite based inductors.

5 Conclusion and Future work

5.1 Conclusions

In this dissertation, a detailed analysis was presented on *LCL*-filter design. The first design method highlighted the importance of resonance frequency and the selection of an appropriate ratio μ between the grid-side and inverter-side inductors, where $\mu=1$ contributes to a filter with minimum voltage drop across it, minimum stored energy, minimum reactive power produced by the *LCL*-filter capacitor, high power factor and robust to external parameter variations such as grid impedance. The second design highlighted the possible limits of passive components in an *LCL*-filter. Both designs complies with the IEEE-519 harmonic limitations, reactive power production limits and power factor operation of the inverter. Furthermore, the second design method discusses the importance of voltage drop across an *LCL*-filter in order to limit the switching losses in an inverter. The reactive power is compensated based on the control structure of the inverter rather than estimating it as a percentage of base capacitance in the case of design one. The research led to the following major conclusions:

- *LCL*-filter designing is highly subjective and dependent on the design requirements/goals.
- There are infinite solutions to an *LCL*-filter design as proven by both design methodologies. Therefore, it is a must to explore the possibilities of optimising them. One of such optimum operating point is presented in chapter 3 of this thesis.
- KoolMu magnetic material can be used as a replacement to ferrite for inductor design. Whereby the soft saturation nature of the magnetic material can be used as an advantage in inductor design.

5.2 Future Work

Following the conclusion discussed in section 5.1, there are areas of improvement which future research can be directed towards as far as the filter design subject is concerned and are listed as follows:

The analysis on the importance of resonance frequency can be extended for other higher order filters like *LC-LCL, LLCL* to further reduce the size of these passive filters.

- There are many solutions to an *LCL*-filter in terms of different passive components values as shown in both design methods that satisfy the required harmonic limitations, reactive power etc. Therefore, it is important to apply optimising strategies to improve the performance of the filter in terms of losses, cost of implementation, reliability etc.
- Developing techniques to estimate the core losses of inductors used in filters via a software such as ANSOFT Maxwell simulation.

REFERENCES

[1] Jalili, K.; Bernet, S., "Design of *LCL* Filters of Active-Front-End Two-Level Voltage-Source Converters," *Industrial Electronics, IEEE Transactions on* , vol.56, no.5, pp.1674,1689, May 2009.

[2] Pena-Alzola, R.; Liserre, M.; Blaabjerg, F.; Ordonez, M.; Yongheng Yang, "LCL-Filter Design for Robust Active Damping in Grid-Connected Converters," *Industrial Informatics, IEEE Transactions on* , vol.10, no.4, pp.2192,2203, Nov. 2014.

[3] Pena-Alzola, R.; Liserre, M.; Blaabjerg, F.; Sebastian, R.; Dannehl, J.; Fuchs, F.W., "Systematic Design of the Lead-Lag Network Method for Active Damping in LCL-Filter Based Three Phase Converters," *Industrial Informatics, IEEE Transactions on* , vol.10, no.1, pp.43,52, Feb. 2014.

[4] S. Jayalath and M. Hanif, "CL-filter design for grid-connected CSI," 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil, 2015, pp. 1-6.

[5] Liserre, M.; Blaabjerg, F.; Hansen, S., "Design and control of an LCL-filter-based three-phase active rectifier," *Industry Applications, IEEE Transactions on* , vol.41, no.5, pp.1281,1291, Sept.-Oct. 2005.

[6] M. Liserre, F. Blaabjerg, and A. DellAquila, “Step-by-step design procedure for a grid-connected three-phase PWM voltage source converter,”Int. J. Electron., vol. 91, no. 8, pp. 445–460, 2004.

[7] R. Peña-Alzola, M. Liserre, F. Blaabjerg, R. Sebastián, J. Dannehl and F. W. Fuchs, "Analysis of the Passive Damping Losses in LCL-Filter-Based Grid Converters," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2642-2646, June 2013.

[8] Donghua Pan; Xinbo Ruan; Chenlei Bao; Weiwei Li; Xuehua Wang, "Magnetic Integration of the LCL Filter in Grid-Connected Inverters," in Power Electronics, IEEE Transactions on , vol.29, no.4, pp.1573-1578, April 2014.

[9] Baumann, E.D.; Hammoud, A.N., "Operational characteristics of a 200°C LC parallel resonant circuit," in Electrical Insulation and Dielectric Phenomena, 1995. Annual Report., Conference on , vol., no., pp.270-273, 22-25 Oct 1995.

[10] Reznik, A.; Simoes, M.G.; Al-Durra, A.; Muyeen, S.M., "LCL Filter Design and Performance Analysis for Grid-Interconnected Systems," *Industry*

Applications, IEEE Transactions on , vol.50, no.2, pp.1225,1232, March-April 2014.

[11] Channegowda, P.; John, V., "Filter Optimization for Grid Interactive Voltage Source Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.12, pp.4106,4114, Dec. 2010.

[12] Hanif, M.; Khadkikar, V.; Weidong Xiao; Kirtley, J.L., "Two Degrees of Freedom Active Damping Technique for LCL Filter-Based Grid Connected PV Systems," in Industrial Electronics, IEEE Transactions on , vol.61, no.6, pp.2795-2803, June 2014.

[13] Sangin Lee; Kui-Jun Lee; Dong-seok Hyun, "Modeling and control of a grid connected VSI using a delta connected LCL filter," Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE , vol., no., pp.833,838, 10-13 Nov. 2008.

[14] S. G. Parker, B. P. McGrath and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 424-432, Jan.-Feb. 2014.

[15] Kantar, E.; Usluer, S.N.; Hava, A.M., "Design and performance analysis of a grid connected PWM-VSI system," *Electrical and Electronics Engineering (ELECO), 2013 8th International Conference on* , vol., no., pp.157,161, 28-30 Nov. 2013.

[16] Blasko, V.; Kaura, V., "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," Industry Applications, IEEE Transactions on , vol.33, no.2, pp.542,550, Mar/Apr 1997.

[17] Donghua Pan; Xinbo Ruan; Chenlei Bao; Weiwei Li; Xuehua Wang, "Optimized Controller Design for LCL -Type Grid-Connected Inverter to Achieve High Robustness Against Grid-Impedance Variation," Industrial Electronics, IEEE Transactions on , vol.62, no.3, pp.1537,1547, March 2015.

[18] Donghua Pan; Xinbo Ruan; Chenlei Bao; Weiwei Li; Xuehua Wang, "Capacitor-Current-Feedback Active Damping With Reduced Computation Delay for Improving Robustness of LCL-Type Grid-Connected Inverter," *Power Electronics, IEEE Transactions on* , vol.29, no.7, pp.3414,3427, July 2014.

[19] W. Wu, Y. He, T. Tang and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter," in

IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4339-4350, Oct. 2013.

[20] Kantar, E.; Usluer, S.N.; Hava, A.M., "Control strategies for grid connected PWM-VSI systems," Electrical and Electronics Engineering (ELECO), 2013 8th International Conference on , vol., no., pp.220,224, 28-30 Nov. 2013.

[21] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," in IEEE Std 519-2014 (Revision of IEEE Std 519-1992) , vol., no., pp.1-29, June 11 2014.

[22] Y. Jiao and F. C. Lee, "LCL Filter Design and Inductor Current Ripple Analysis for a Three-Level NPC Grid Interface Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4659-4668, Sept. 2015.

[23] Qian Liu; Li Peng; Yong Kang; Shiying Tang; Deliang Wu; Yu Qi, "A Novel Design and Optimization Method of an LCL Filter for a Shunt Active Power Filter," Industrial Electronics, IEEE Transactions on , vol.61, no.8, pp.4000,4010, Aug. 2014.

[24] Peng Zhan; Weixing Lin; Jinyu Wen; Meiqi Yao; Naihu Li, "Design of LCL filters for the back-to-back converter in a Doubly Fed Induction Generator," Innovative Smart Grid Technologies - Asia (ISGT Asia), 2012 IEEE , vol., no., pp.1,6, 21-24 May 2012.

[25] Xing Wei; Lan Xiao; Zhilei Yao; Chunying Gong, "Design of LCL filter for wind power inverter," World Non-Grid-Connected Wind Power and Energy Conference (WNWEC), 2010 , vol., no., pp.1,6, 5-7 Nov. 2010.

[26] mag-inc.com,‘2015 Magnetics Powder Core Catalog’[Online]. Available:http://www.mag-inc.com/design/technical-documents/powder-core-documents

[27] Kazmierkowski, M.P.; Jasinski, M.; Wrona, G., "DSP-Based Control of Grid-Connected Power Converters Operating Under Grid Distortions," *Industrial Informatics, IEEE Transactions on* , vol.7, no.2, pp.204,211, May 2011.

[28] Matsumori, H.; Shimizu, T.; Takano, K.; Ishii, H., "Evaluation of Iron Loss of AC Filter Inductor Used in Three-Phase PWM Inverters Based on an Iron Loss Analyzer," in Power Electronics, IEEE Transactions on , vol.31, no.4, pp.3080-3095, April 2016.

[29] H. G. Jeong, K. B. Lee, S. Choi and W. Choi, "Performance Improvement of LCL-Filter-Based Grid-Connected Inverters Using PQR Power Transformation,"

in IEEE Transactions on Power Electronics, vol. 25, no. 5, pp. 1320-1330, May 2010.

[30] Friebe, J.; Zacharias, P., "Review of Magnetic Material Degradation Characteristics for the Design of Premagnetized Inductors," in Magnetics, IEEE Transactions on , vol.50, no.3, pp.40-48, March 2014.

[31] Muhlethaler, J.; Schweizer, M.; Blattmann, R.; Kolar, J.W.; Ecklebe, A., "Optimal Design of LCL Harmonic Filters for Three-Phase PFC Rectifiers," in Power Electronics, IEEE Transactions on , vol.28, no.7, pp.3114-3125, July 2013.

[32] Shuo Wang; Dorrell, D.G., "Copper Loss Analysis of EV Charging Coupler," in Magnetics, IEEE Transactions on , vol.51, no.11, pp.1-4, Nov. 2015.

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Appendix A Derivation of Equations used in Chapter 2 of the thesis

Derivation of Equation (2.1),(2.2),(2.3)

Assumptions: Grid voltage doesn't contain the middle and high frequency components. Therefore, grid can be considered as a short circuit for middle and high frequencies. Inverter is considered as a voltage source $v_i(s)$, while the grid as $v_g(s)$, $i_i(s)$ is the inverter-side current and $i_g(s)$ is the grid-side current. Using the principle of superposition (Shorting $v_g(s)$ of Figure 2.1):

$$\boldsymbol{i_g(s) = \left(\frac{1/sC}{1/sC+sL_g}\right) i_i(s)} \qquad \text{(A. 1)}$$

$$\frac{i_g(s)}{i_i(s)} = \left(\frac{1}{1+sL_g sC}\right) \qquad \text{(A. 2)}$$

$$\boldsymbol{\frac{i_g(s)}{i_i(s)} = \left(\frac{1}{1+s^2L_gC}\right)} \qquad \text{(A. 3)=(2.3)}$$

$$\boldsymbol{v_i(s) = i_i(s)\left(sL_i + \frac{L_g s \frac{1}{sC} sC}{1+s^2L_gC}\right)} \qquad \text{(A. 4)}$$

$$\boldsymbol{\frac{v_i(s)}{i_i(s)} = \left(\frac{L_i s+L_iL_gCs^3+L_gs}{1+s^2L_gC}\right)} \qquad \text{(A. 5)}$$

$$\boldsymbol{\frac{i_i(s)}{v_i(s)} = \left(\frac{1+s^2L_gC}{L_iL_gCs^3+(L_g+L_i)s}\right)} \qquad \text{(A. 6)=(2.2)}$$

By using (A.2) and (A.6)

$$\boldsymbol{\frac{i_g(s)}{v_i(s)} = \left(\frac{1}{L_iL_gCs^3+(L_g+L_i)s}\right)} \qquad \text{(A. 7)=(2.1)}$$

Equation (2.6)

Resonance frequency (f_{res}) of the *LCL*-filter with Y-connected capacitor is given by :

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i L_g C}} \qquad \text{(A. 8)}$$

If the total inductance, $L_T = L_i + L_g$ and ratio $\mu = L_g/L_i$. Then $L_T = L_i(\mu+1)$ *and* $L_T = L_g(\mu+1)/\mu$

$$f_{res}^2 = \frac{1}{4\pi^2}\left(\frac{L_T}{\frac{L_T}{(\mu+1)}\frac{L_T \mu C}{(\mu+1)}}\right) \qquad \text{(A. 9)}$$

$$L_T C = \frac{1}{4\pi^2 f_{res}^2}\frac{(1+\mu)^2}{\mu} \qquad \text{(A. 10)}$$

Considering the ratio $k = f_{sw}/f_{res}$

$$L_T C = \frac{k^2}{4\pi^2 f_{sw}^2}\frac{(1+\mu)^2}{\mu} \qquad \text{(A. 11)=(2.6)}$$

Equation (2.22) and (2.23)

In deriving these transfer functions inverter is considered as a harmonic generator while the grid as a short circuit at high frequencies. The ratio of grid-side current to the inverter-side voltage at switching frequency $s = h = j\omega_{sw} = j2\pi f_{sw}$ deduced through (2.1)

$$\frac{i_g(h)}{v_i(h)} = \frac{1}{L_T(j2\pi f_{sw})\left(1 - \left(\frac{f_{sw}}{f_{res}}\right)^2\right)} \qquad \text{(A. 12)}$$

Considering the absolute value of (A.12)

$$\left|\frac{i_g(h)}{v_i(h)}\right| = \frac{1}{2\pi L_T f_{sw}|1-k^2|} = a_g \qquad \text{(A. 13)=(2.22)}$$

Where a_g is the grid-side current magnitude attenuation coefficient. The magnitude ratio of inverter-side current to the inverter-side voltage at switching frequency is given by (2.2),

$$\frac{i_i(s)}{v_i(s)} = \frac{s^2 L_g C + 1}{s^3 L_i L_g C + s(L_i + L_g)} \qquad \text{(A. 14)}$$

$$\frac{i_i(s)}{v_i(s)} = \frac{1 - \omega_{sw}^2 L_g C}{L_T\left(j2\pi f_{sw}\right)\left(1 - \left(\frac{f_{sw}}{f_{res}}\right)^2\right)} \qquad \text{(A. 15)}$$

$$L_g C = \frac{1}{4\pi^2 f_{res}^2}\left(1 + \mu\right) \qquad \text{(A. 16)}$$

$$\left|\frac{i_i(h)}{v_i(h)}\right| = \frac{|(1-k^2(1+\mu)|}{2\pi L_T f_{sw}|1-r^2|} = a_i \qquad \text{(A. 17)=(2.23)}$$

Equation (2.31)

Considering equation (A. 13) or (2.22)

$$\left|\frac{i_g(h)}{v_i(h)}\right| = \frac{1}{2\pi L_T f_{sw}|1-k^2|} \qquad \text{(A. 18)}$$

$$L_T = \frac{1}{2\pi f_{sw}\left|\frac{i_g(h)}{v_i(h)}\right||1-k^2|} \qquad \text{(A. 19)}$$

Dividing the above equation using base values (Basics of per unit derivation are given under Appendix B)

$$\frac{L_T}{L_b} = \frac{1}{\frac{2\pi f_{sw}}{2\pi f_b}\left|\frac{i_g(h)/i_g}{v_i(h)/v_g}\right||1-k^2|} \qquad \text{(A. 20)}$$

$$l_T = \frac{1}{h_{sw}\left|\frac{i_{pu}(h)}{v_{pu}(h)}\right||1-k^2|} \qquad \text{(A. 21)=(2.31)}$$

Above equation is also used in reference [11] of the thesis.

Appendix B Per Unit Derivation of *LCL*-filter parameters

System is designed based on per unit basis of the inverter rating. The advantage of the per unit method

1. Generalize the design procedure for a wide range of power levels
2. Design procedure compatible with the grid power system ratings where most impedances are usually expressed in per unit basis.

$V_{LN} = V_{base}$

3 phase power rating = $P_{r(base)}$

$V_{pu} = 1$

$P_r = 1$

$I_{actual} = I_{pu} x I_{base}$

$$I_{actual} = \frac{1}{3}\left(\frac{P_{r(pu)}}{V_{pu}}\right)\left(\frac{P_{r(base)}}{V_{base}}\right)$$

$$I_{pu} = \frac{P_{r(pu)}}{V_{pu}}$$

$$Z_{base} = \frac{V_{base}}{I_{base}}$$

$$Z_{pu} = \frac{V_{pu}}{I_{pu}}$$

$$L_{base} = \frac{Z_{base}}{2\pi f_{base}}$$

$$L_{pu} = \frac{L_{actual}}{L_{base}} = Z_{pu}$$

$$C_{base} = \frac{1}{Z_{base} x 2\pi f_{base}}$$

$$C_{pu} = \frac{C_{actual}}{C_{base}} = \frac{1}{Z_{pu}}$$

$$V_{dc(pu)} = \frac{V_{dc}}{V_{base}}$$

$$f_{sw(pu)} = \frac{f_{sw}}{f_{base}}$$

Appendix C Derivation of Equations used in Chapter 3 of the thesis

Equation (3.1)

Equation (A.10) of the Appendix B is considered here:

$$L_T C = \frac{1}{4\pi^2 f_{res}^2}\frac{(1+\mu)^2}{\mu} \qquad \text{(C. 1)}$$

Rearranging (1) using per unit definition. According to the definition of per unit system given in the Appendix B

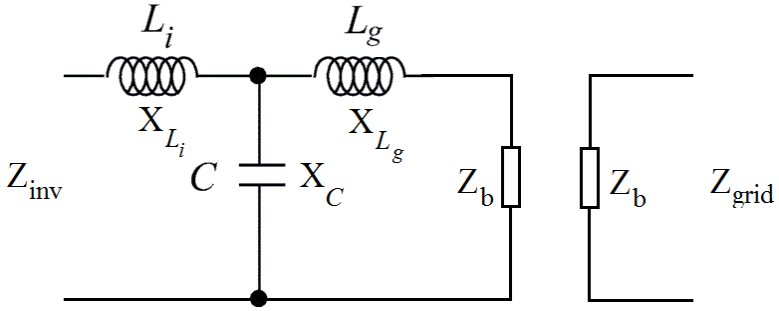
$$\left(\frac{l_T Z_b}{2\pi f_b}\right)\left(\frac{c}{2\pi f_b Z_b}\right) = \frac{1}{4\pi^2 f_{res}^2}\frac{(1+\mu)^2}{\mu} \qquad \text{(C. 2)}$$

$$l_T c = \frac{f_b^2}{f_{res}^2}\frac{(1+\mu)^2}{\mu} \qquad \text{(C. 3)=(3.1)}$$

Equation (3.11): Deriving the per unit output power of an inverter

Note: This is an approximated derivation but this derivation is in line with the derivation based on phasor voltages and currents by [6]

Sensing grid voltage to synchronised with grid current control



Impedance of grid

$$Z_{grid} = Z_b$$

$$\frac{Z_{grid}}{Z_b} = z_{g\_pu} = 1$$

Impedance of the inverter

Parallel combination of $(X_{L_g} + Z_b)$ and X_c

$$Z_x = \frac{jX_c(jX_{L_g} + Z_b)}{jX_c + jX_{L_g} + Z_b}$$

Impedance of the inverter (Z_{inv})

$$Z_{inv} = \frac{jX_c(jX_{L_g} + Z_b)}{jX_c + jX_{L_g} + Z_b} + jX_{L_i}$$

$$Z_{inv} = \frac{jX_c jX_{L_g}}{jX_c + jX_{L_g} + Z_b} + \frac{jX_c Z_b}{jX_c + jX_{L_g} + Z_b} + jX_{L_i}$$

$$Z_{inv} = Z_b \left(\frac{\frac{jX_c jX_{L_g}}{Z_b}}{jX_c + jX_{L_g} + Z_b} + \frac{\frac{jX_c Z_b}{Z_b}}{jX_c + jX_{L_g} + Z_b} + \frac{jX_{L_i}}{Z_b} \right)$$

$$\frac{Z_{inv}}{Z_b} = \left(\frac{\frac{jX_c jX_{L_g}}{Z_b Z_b}}{\frac{jX_c}{Z_b} + \frac{jX_{L_g}}{Z_b} + \frac{Z_b}{Z_b}} + \frac{\frac{jX_c}{Z_b}}{\frac{jX_c}{Z_b} + \frac{jX_{L_g}}{Z_b} + \frac{Z_b}{Z_b}} + \frac{jX_{L_i}}{Z_b} \right)$$

For a per unit system ($X_g=\omega L_g$) , ($X_i=\omega L_i$) and ($X_c=1/\omega C$) when expressed with pu of the base Z_b ,

$l_g=X_g/Z_b$, $l_i=X_i/Z_b$ and $c= -Z_b/ X_c$

$$z_{inv} = \left(\frac{-j\left(\frac{1}{c}\right) jl_g}{-j\left(\frac{1}{c}\right) + jl_g + 1} + \frac{-j\left(\frac{1}{c}\right)}{-j\left(\frac{1}{c}\right) + jl_g + 1} + jl_i \right)$$

$$z_{inv} = \left(\frac{jl_g}{1 - cl_g + jc} + \frac{1}{1 - cl_g + jc} + jl_i \right)$$

$$z_{inv} = \left(\frac{jl_g}{1 - cl_g + jc} + \frac{1}{1 - cl_g + jc} + jl_i \right)$$

If c<10% and l_g<10% cl_g<1% cl_g≈0

$$z_{inv} = \left(\frac{jl_g}{1 + jc} + \frac{1}{1 + jc} + jl_i \right)$$

Considering the conjugate

$$z_{inv} = \left(\frac{jl_g(1 - jc)}{1 + c^2} + \frac{(1 - jc)}{1 + c^2} + jl_i \right)$$

If c<10% and c^2<1% c^2≈0

$$z_{inv} = \left(jl_g + cl_g + 1 + -jc + jl_i \right)$$

$$z_{inv} = \left(1 + -jc + jl_g + jl_i\right)$$

If $l_i+l_g=l_T$

$$z_{inv} = 1 + j(l_T - c)$$

Power of the inverter

$$P_{inv} = \frac{V_{inv}^2}{Z_{inv}}$$

Base power

$$P_b = \frac{V_b^2}{Z_b}$$

Therefore for a per unit system (p)

$$\frac{P_{inv}}{P_b} = \frac{V_{inv}^2}{Z_{inv}} \frac{Z_b}{V_b^2}$$

$$V_{inv} \approx V_b$$

$$p = \frac{1}{Z_{inv}/Z_b}$$

Substituting the inverter per unit impedance derived

$$p = \frac{1}{1 + j(l_T - c)}$$

$$p = \frac{1 - j(l_T - c)}{1 + (l_T - c)^2}$$

$(l_T - c)^2 \approx 0$

$$p \approx 1 + j(c - l_T)$$

Or

$$p \approx 1 - j(l_T - c)$$

Therefore (1) corresponds to the unity active power transferred and $(l_T - c)$ corresponds to the reactive power transferred.

Equation (3.8)

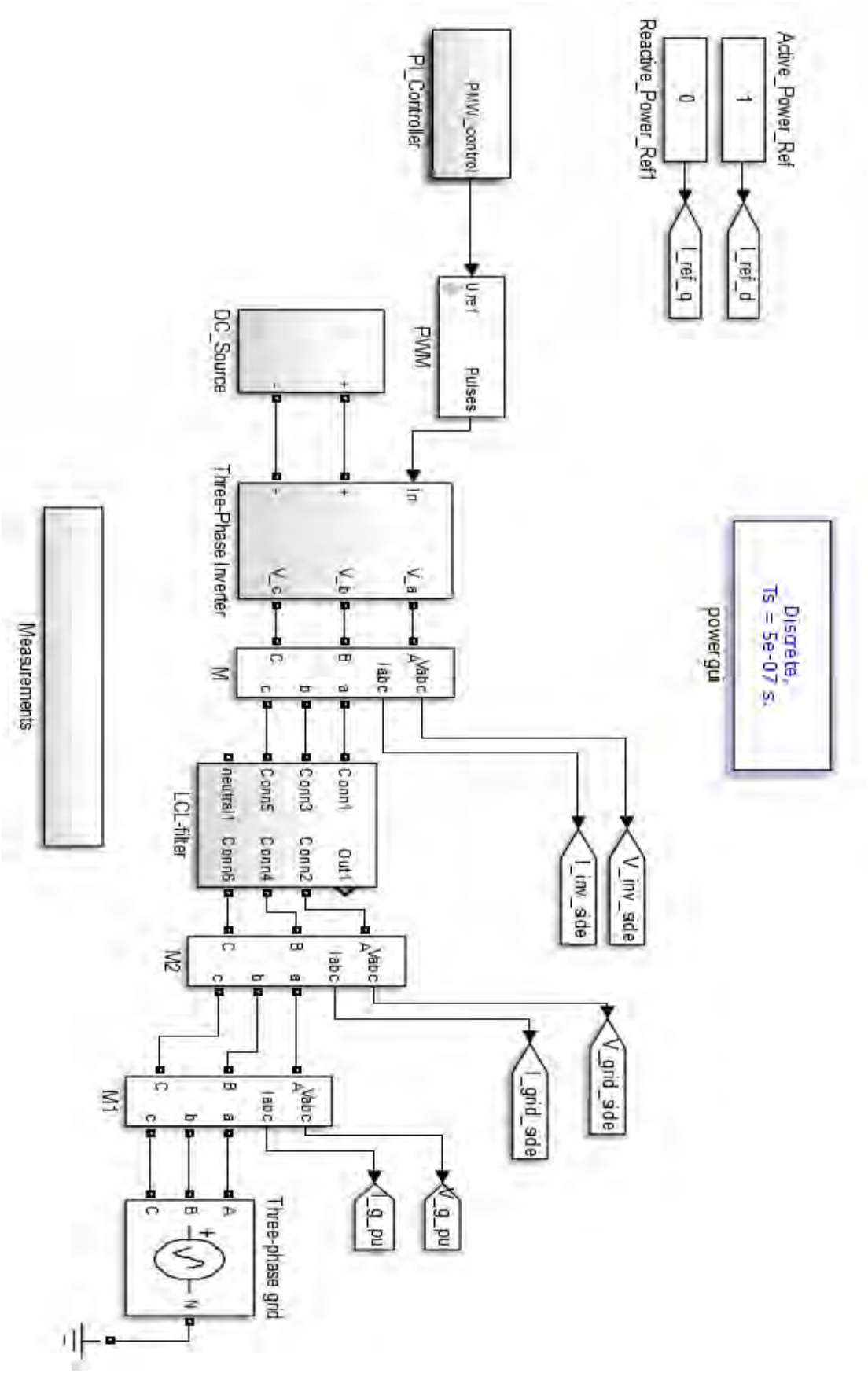
(3.8) is solved as a first order quadratic equation

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Therefore solutions becomes

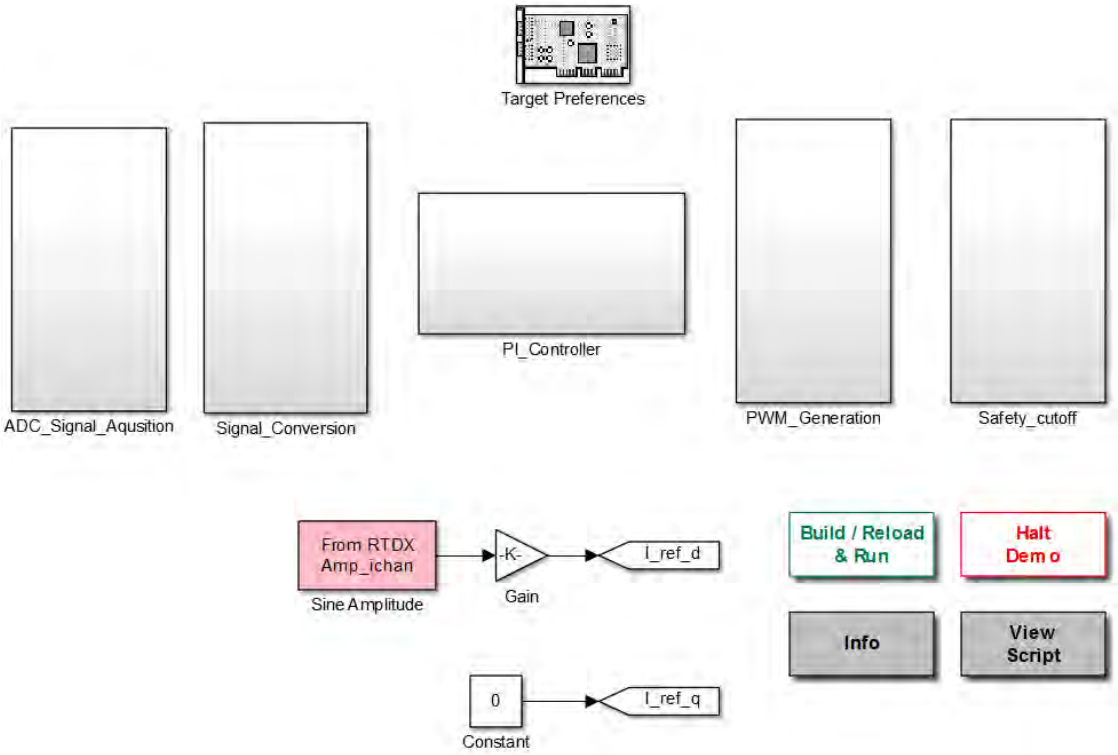
$$l_{Tmax1} = \frac{q_{min} \pm \sqrt{q_{min}^2 + 4\left(k^2 \left(\frac{f_b}{f_{res}}\right)^2 \frac{(1+\mu)^2}{\mu}\right)}}{2}$$

Appendix D MATLAB Simulink Simulation File

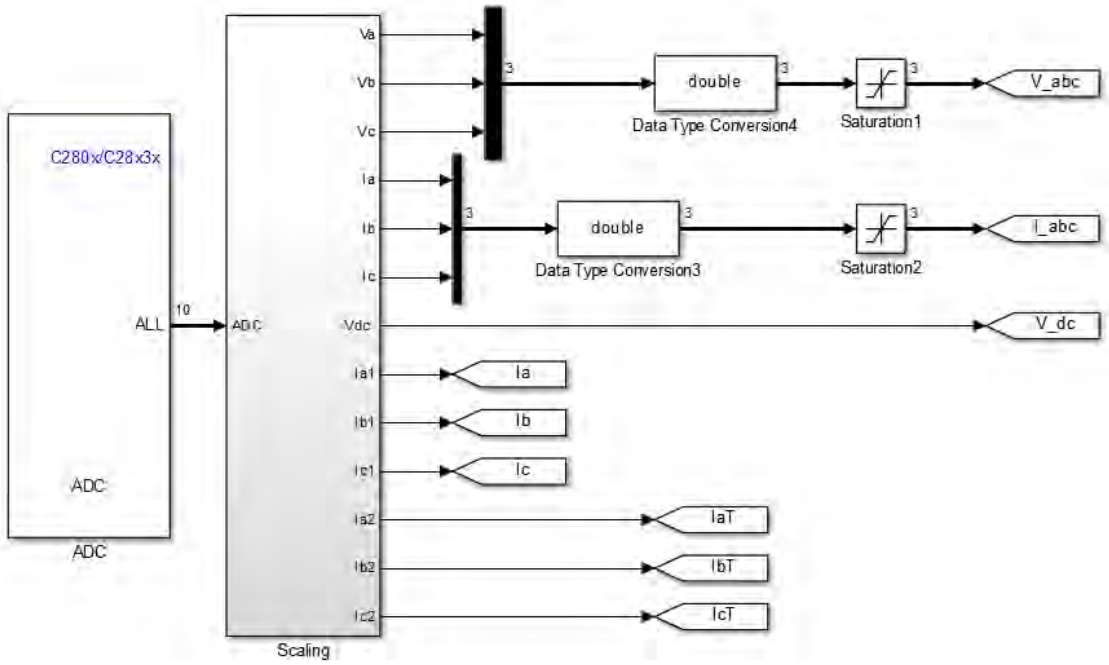


Appendix E Block Diagram of the Controller Implemented in F28335

Main Software Interface

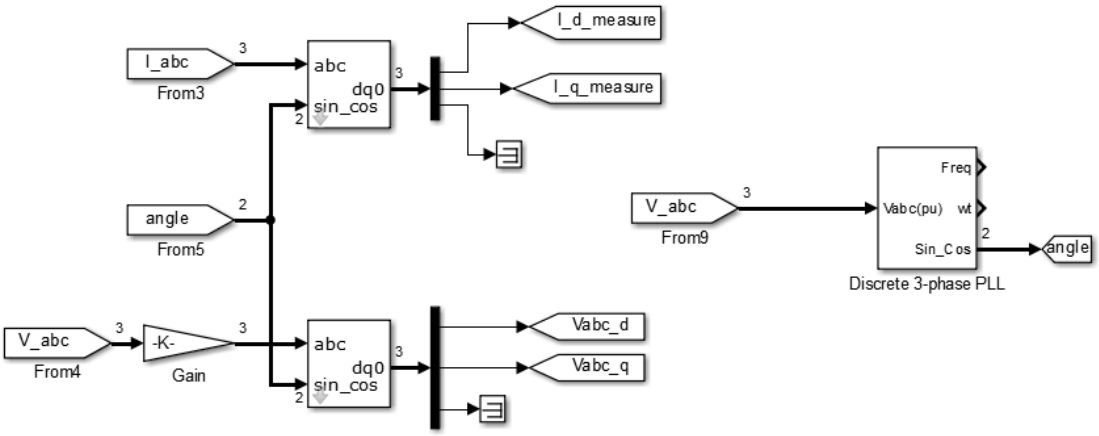


ADC Signal Acquisition



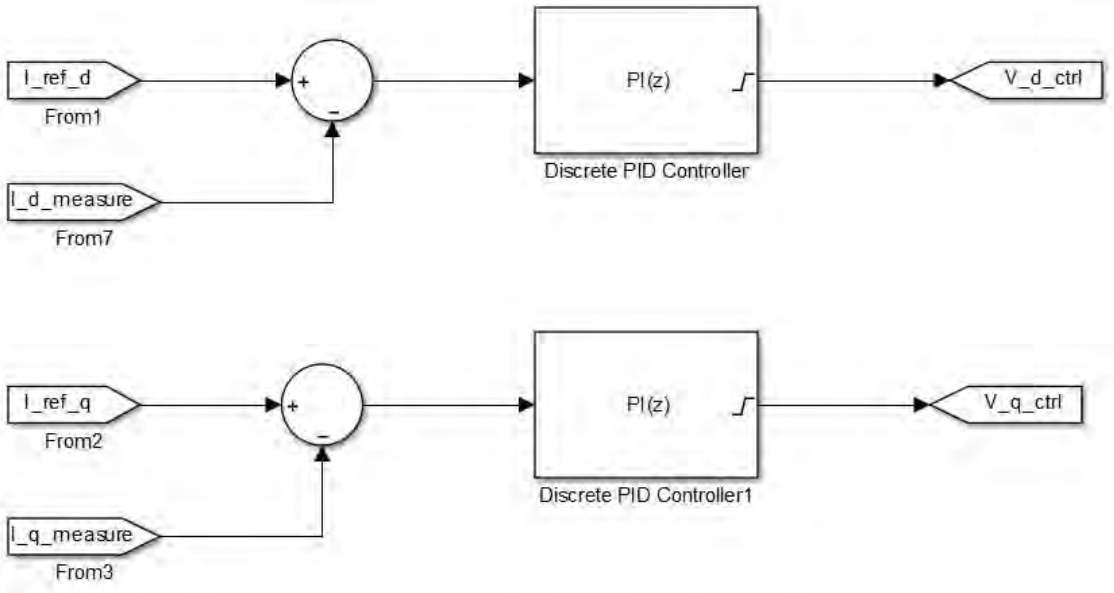
Measured analogue signals (3-phase currents and voltages) are converted to digital form and scaled to per unit measurements as explained in section 2.4.

Signal Conversion



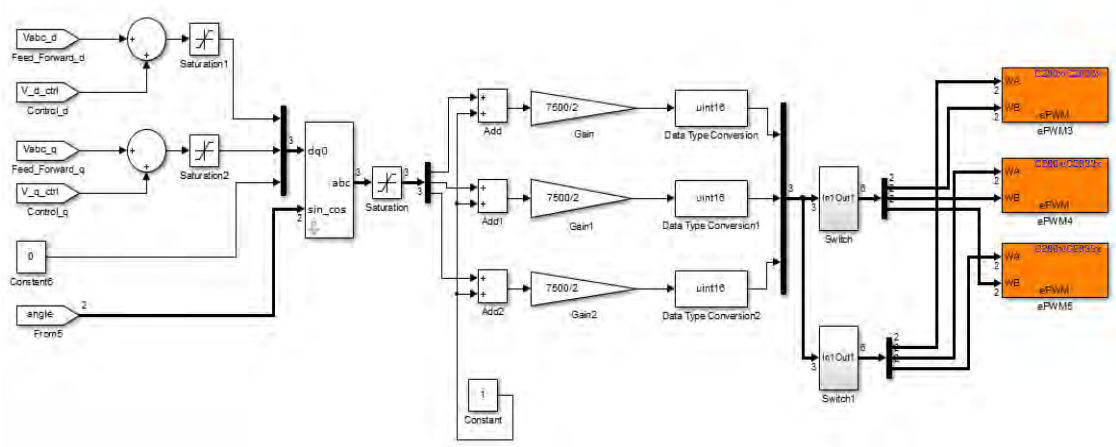
Transformation of three-phase abc signals (currents and voltages) to dq0 rotating reference frame and the "Discrete 3-phase PLL" block is the software phase lock loop which extracts the angle of grid voltage.

PI Controller



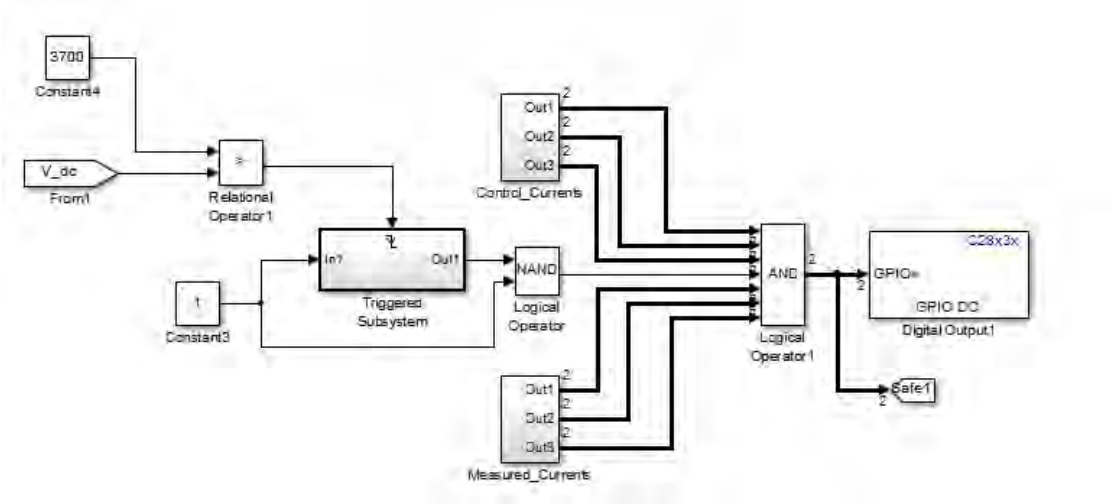
Discrete implementation of proportional Integral controller, where I_ref_d and I_ref_q are the d-axis and q-axis reference currents and I_d_measure and I_q_measure are the d-axis and q-axis measured currents. V_d_ctrl and V_q_ctrl are controlled outputs.

PWM Generation



Grid-voltage is feed-forward to the controlled signal. Pulse width modulated signal are generated using ePMWx blocks based on the controlled outputs from the controller.

Safety cut-off



dc bus voltage and grid-injected currents are continuously monitored to detect any faulty conditions. In a faulty event, inverter is disconnected from the grid.

Appendix F Description of the Experimental Prototype

Proposed *LCL*-filter designs for a grid-connected VSI are experimentally validated using a 3 kW prototyped. Block diagram of the experimental system is shown in Figure. 1.

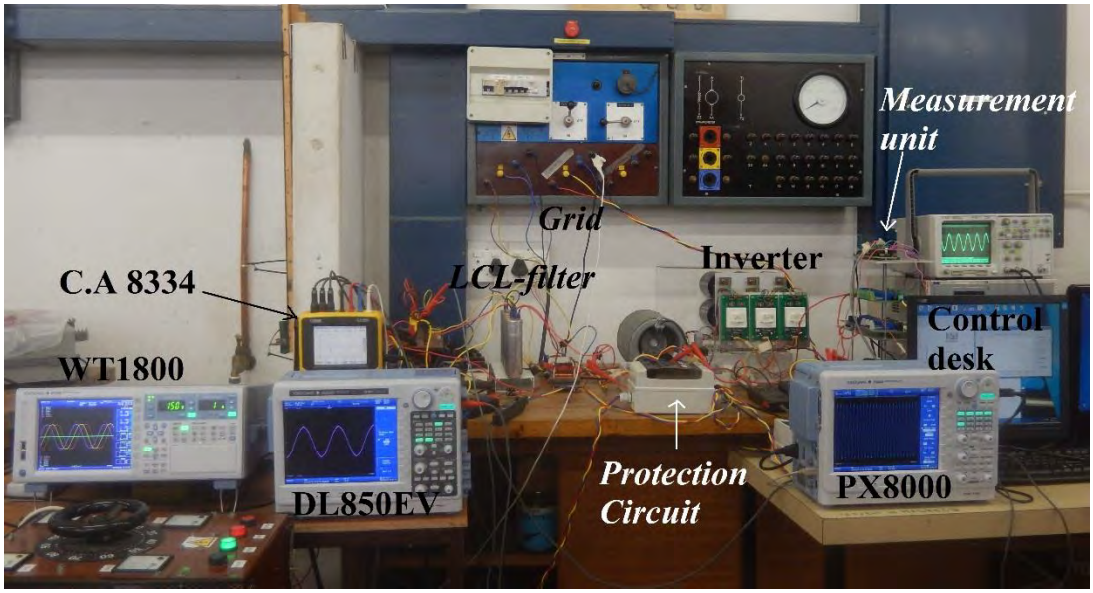


Figure 1 3 kW Experimental setup

Experimental setup can be divided in to following sub-sections based on the significance of operation of grid-connected inverter.

- Power stage
- Controller stage
- Current Measurement Circuitry
- Protection Circuitry
- Grid

Power Stage

- **DC bus**

The output of the variable three-phase ac-source as shown in Figure 2 is connected to the three-phase rectifier as shown in Figure 3 to realise the DC bus.

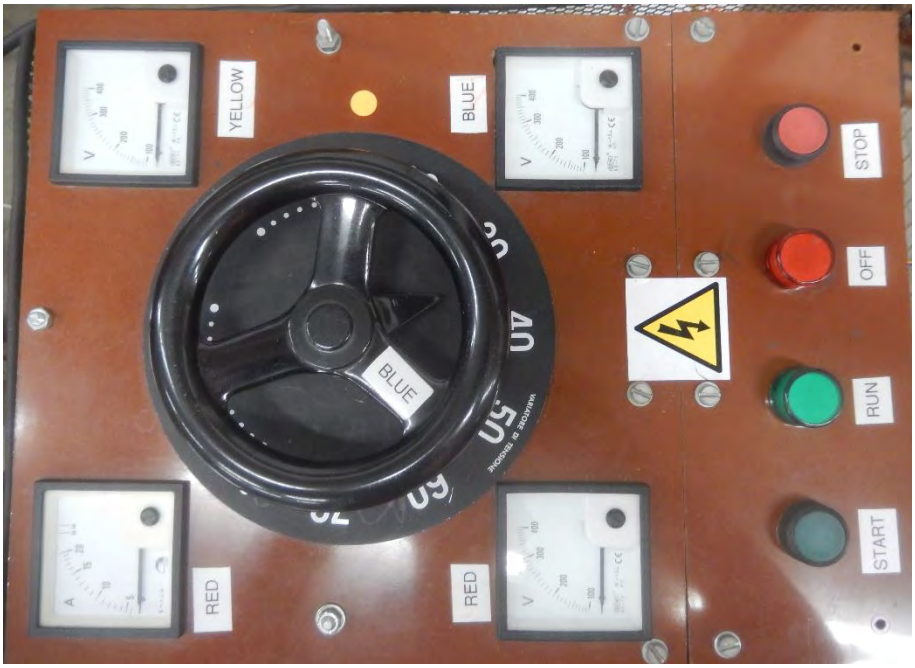


Figure 2 Variable ac supply

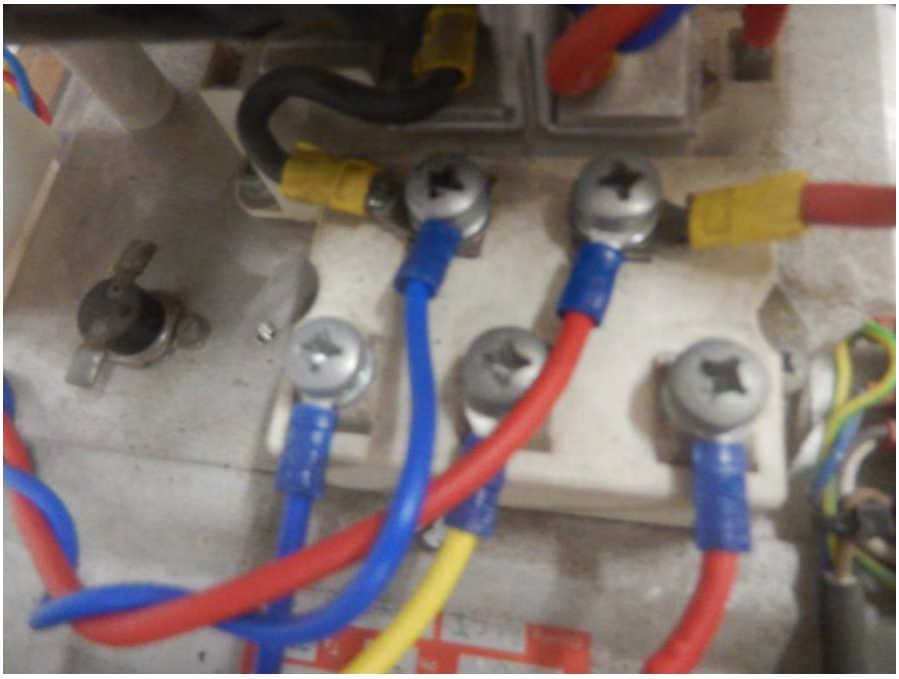


Figure 3 Three-phase rectifier (Diode-bride)

- **Voltage Source inverter (with DC bus capacitance)**

  The three phase inverter was constructed using IGBTs (Semikron (SKM 100GB123D). The converter has the option of accepting a direct DC voltage or rectifying a three-phase voltage input. Rectified voltage is connected across the capacitors with rating 600 V, to realise the DC bus as shown in Figure 4.

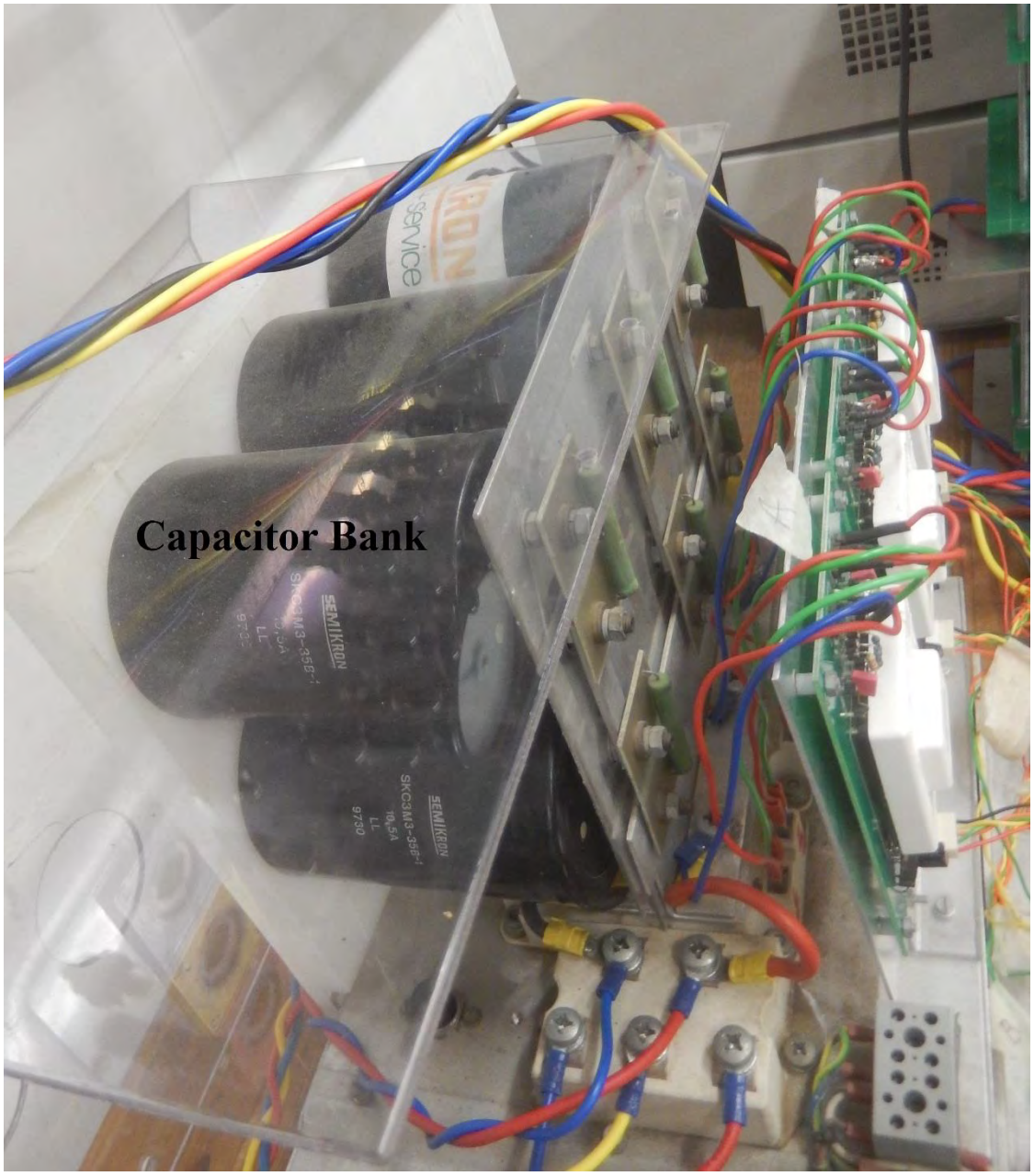


Figure 4 DC bus

Controller Stage

Controller was implemented in Texas Instruments TMS320F28335 DSP according to the guidance provided in Appendix E. Controller generates the PWM signals with the maximum output voltage of 3.3V. The driver circuit boost the voltage of PWM signals to 15V in order to drive the inverter. The electrical layout of the driver circuit is shown in Figure 5.

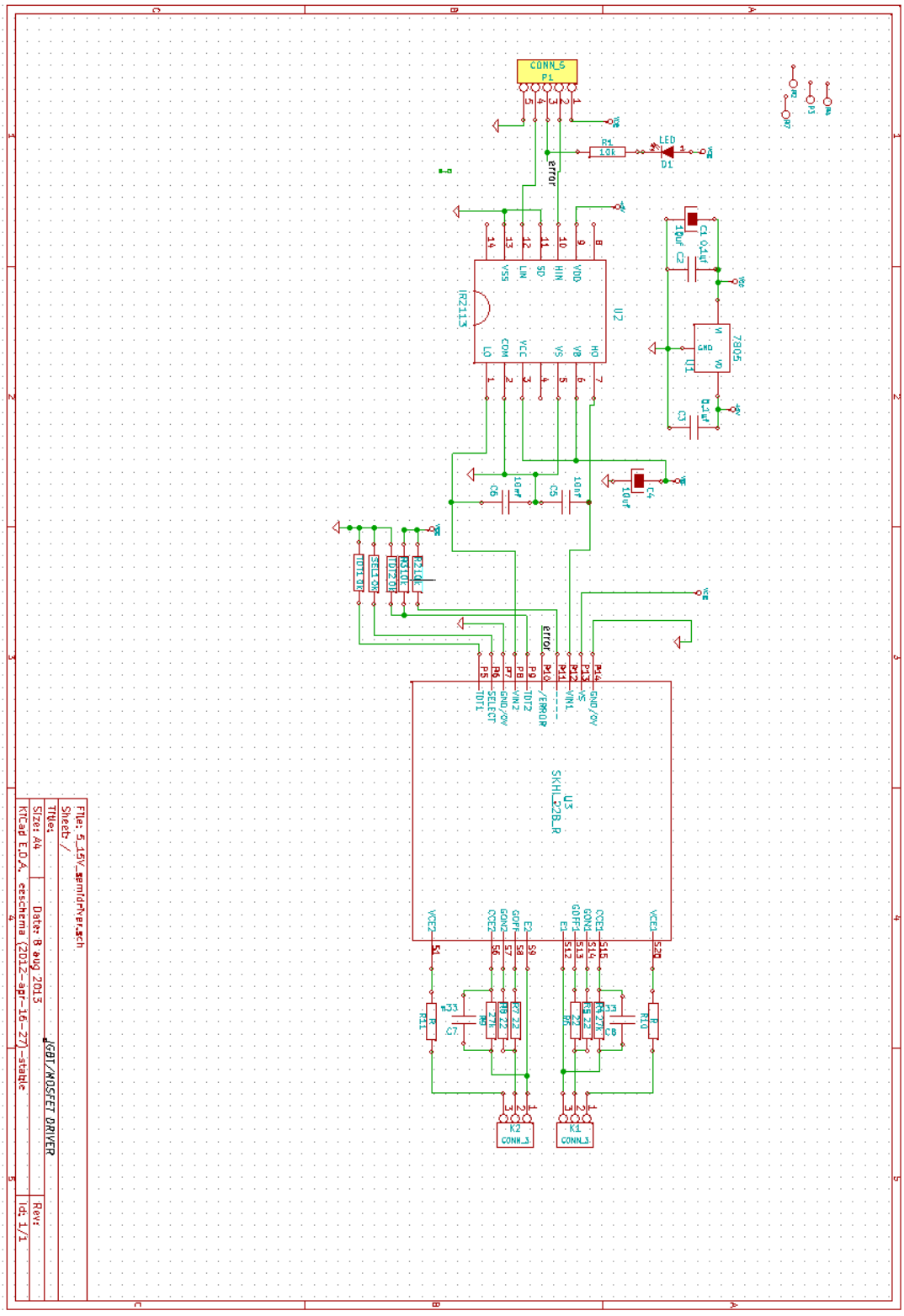


Figure 5 Electrical layout of the driver circuit

Current Measurement Circuitry

Phase currents are measured using LEM current transducers while the phase voltages are measured using LEM voltage transducers. The measured currents and voltages passed through a shifter and a gain circuit to make sure that the measured voltages and currents vary between 0-3 V, as the Analogue to Digital conversion unit of DSP is capable of acquiring signals within this range. The conversion unit is calibrated such that the maximum output of the unit is 3V and it represents the rated grid injected current and measure grid-voltage. The circuit used for three-phase measurements are shown in Figure 6 and the PCB layout of the measuring unit is shown in Figure 7.

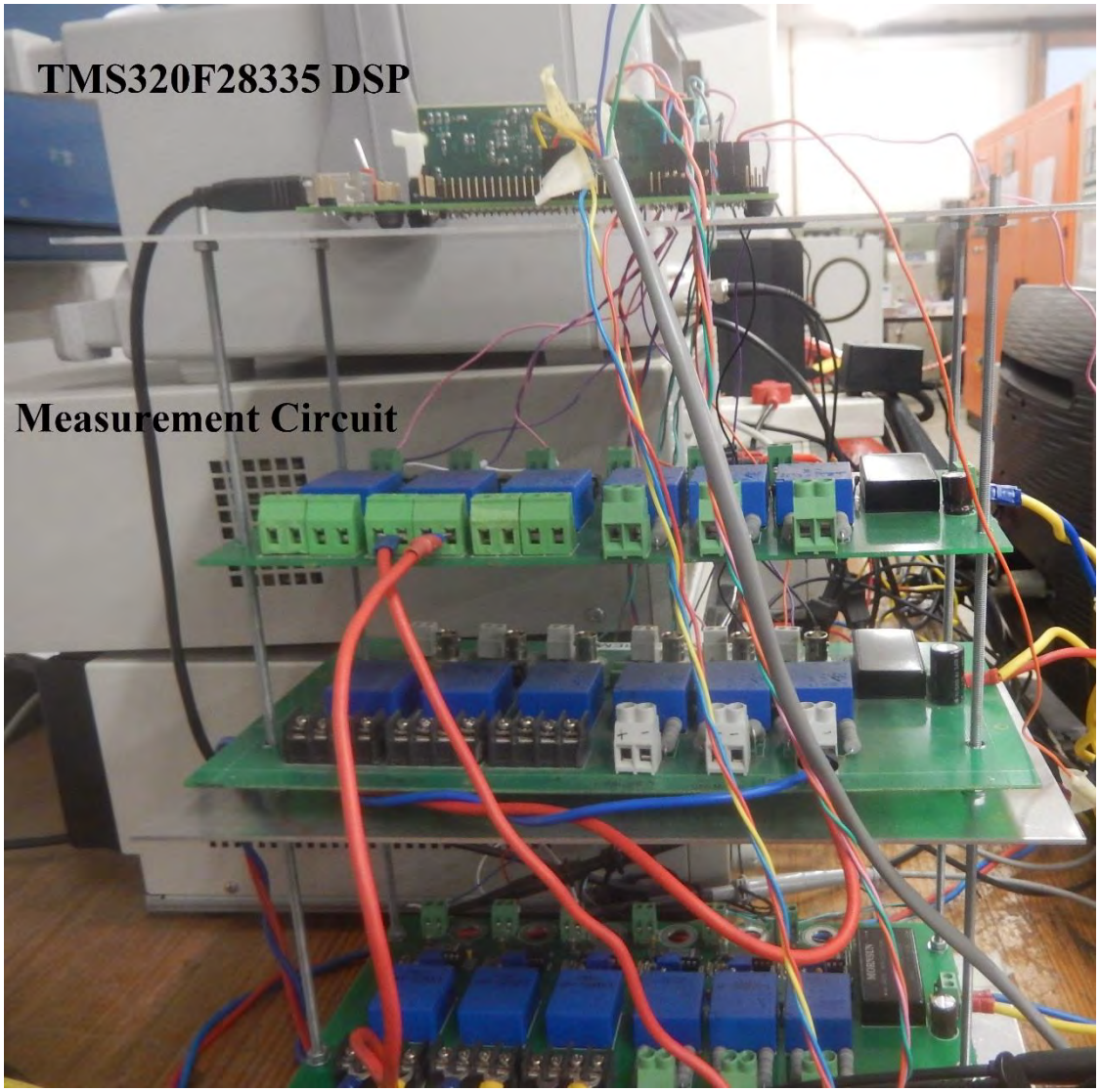


Figure 6 Measurement Circuits

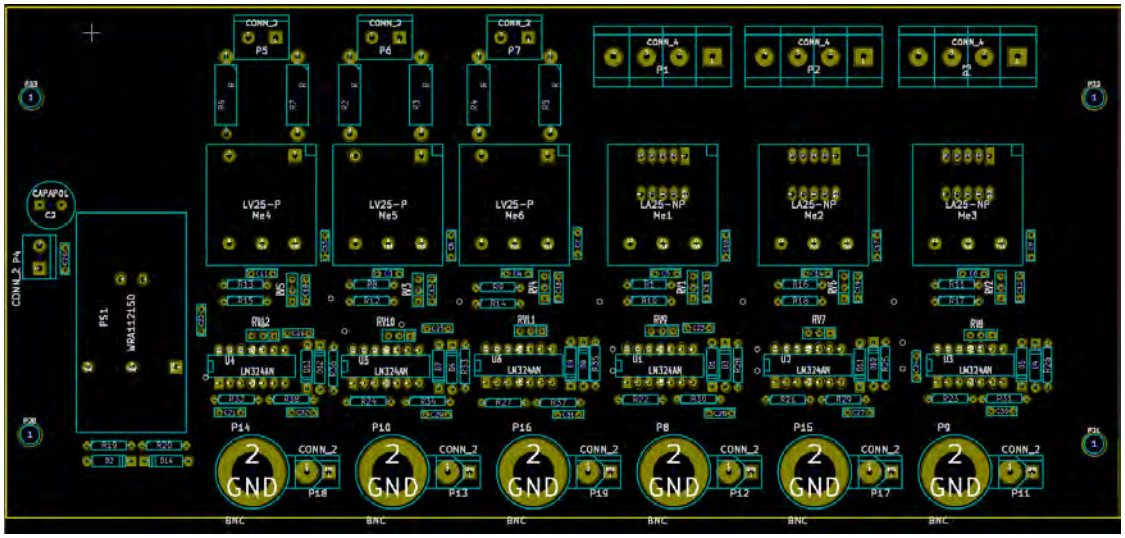


Figure 7 PCB layout of the measurement circuit board

Protection Circuitry

Inverter is protected from any faults using standard circuit breakers and a contactor circuit shown in Figure 8, driven by controller signals to cut-off the grid and dc bus in a case of fault. In addition to the hardware protections, it is also protected by the controller which stops the inverter switching if a fault is generated as described in Appendix E.

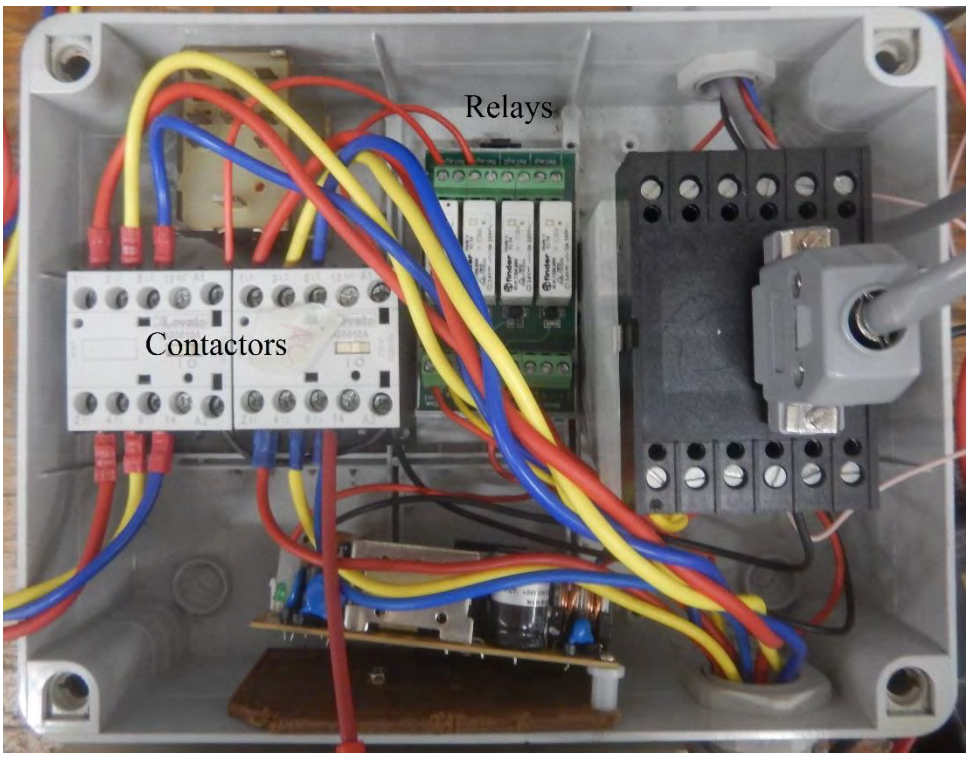


Figure 8 Contactor circuit

Grid

The inverter is connected to a grid with 76 Vrms and 65 Amps. The connection to the grid is available in the machine lab of University of Cape Town.

Appendix G Assessment of Ethics in research

EBE Faculty: Assessment of Ethics in Research Projects (Rev2)

Any person planning to undertake research in the Faculty of Engineering and the Built Environment at the University of Cape Town is required to complete this form before collecting or analysing data. When completed it should be submitted to the supervisor (where applicable) and from there to the Head of Department. If any of the questions below have been answered YES, and the applicant is NOT a fourth year student, the Head should forward this form for approval by the Faculty EIR committee: submit to Ms Zulpha Geyer (Zulpha.Geyer@uct.ac.za; Chem Eng Building, Ph 021 650 4791).
NB: A copy of this signed form must be included with the thesis/dissertation/report when it is submitted for examination

This form must only be completed once the most recent revision EBE EiR Handbook has been read.

Name of Principal Researcher/Student: **Amarasinghe Danapathi Arachchige Sampath Duminda Jayalath** Department: **Electrical Engineering**
Preferred email address of the applicant: **adasdjsampath@gmail.com**

If a Student: Degree: **Msc Electrical Engineering** Supervisor: **Dr. Moin Hanif**

If a Research Contract indicate source of funding/sponsorship: **NA**

Research Project Title: **Design of *LCL*-filters for Grid-Connected Voltage Source Inverters**

Overview of ethics issues in your research project:

Question 1: Is there a possibility that your research could cause harm to a third party (i.e. a person not involved in your project)?	YES	✓ NO
Question 2: Is your research making use of human subjects as sources of data? If your answer is YES, please complete Addendum 2.	YES	✓ NO
Question 3: Does your research involve the participation of or provision of services to communities? If your answer is YES, please complete Addendum 3.	YES	✓ NO
Question 4: If your research is sponsored, is there any potential for conflicts of interest? If your answer is YES, please complete Addendum 4.	YES	✓ NO

If you have answered YES to any of the above questions, please append a copy of your research proposal, as well as any interview schedules or questionnaires (Addendum 1) and please complete further addenda as appropriate. Ensure that you refer to the EiR Handbook to assist you in completing the documentation requirements for this form.

I hereby undertake to carry out my research in such a way that

- there is no apparent legal objection to the nature or the method of research; and
- the research will not compromise staff or students or the other responsibilities of the University;
- the stated objective will be achieved, and the findings will have a high degree of validity;
- limitations and alternative interpretations will be considered;
- the findings could be subject to peer review and publicly available; and
- I will comply with the conventions of copyright and avoid any practice that would constitute plagiarism.

Signed by:

	Full name and signature	Date
Principal Researcher/Student:	Amarasinghe Danapathi Arachchige S .D Jayalath	23 March 2016

This application is approved by:

Supervisor (if applicable):	Dr. Moin Hanif	23 March 2016
HOD (or delegated nominee): *Final authority for all assessments with NO to all questions and for all undergraduate research.*		23/3/16
Chair : Faculty EIR Committee For applicants other than undergraduate students who have answered YES to any of the above questions.		