Single Stage Boost Inverter for Standalone Fuel Cell Applications

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Declaration

This dissertation is submitted to the department of Electrical Engineering, University of Cape Town, in complete fulfilment of the requirements for the degree of Master of Science in Electrical Engineering. It has not been submitted before for any degree or examination at this or any other university. I know the meaning of plagiarism and declare that all the work in the document, save for which is properly acknowledged, is my own.

Name: **Otshepeng Johny Moraka**

Signature: Signed by candidate **Date:** 15 October 2015

Signature Removed

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Abstract

The proton exchange membrane fuel cell (PEMFC) is a promising technology that can be manufactured in South Africa because of the platinum catalyst required. South Africa is rich in platinum and, therefore, the PEMFC system can be cost-effectively produced. In residential stationary applications of the PEMFC a power conditioning system is required to convert the dc voltage output of the PEMFC to ac voltage. Therefore, the focus of this thesis is to analyse, simulate and design a power electronic dc-ac converter.

The power electronic dc-ac converter is based on a transformerless single stage power conversion scheme, which has better weight, volume and efficiency than the commonly used two stage power conversion schemes. The selected topology is the boost inverter that consists of two identical boost converters for boosting and inversion of the PEMFC dc voltage. Moreover, it achieves reliable operation under nonlinear loads, sudden load changes and inrush current, using a double loop control strategy. Initially, the double loop control strategy was introduced with proportional integral (PI) controllers. Recently, with the widespread use of proportional resonant PR controllers, the PI controllers were replaced with PR controllers to achieve zero steady state error for the ac components of the reference. However, during the implementation of the PR controllers on the boost inverter, a significant dc offset in the output voltage of the boost inverter was observed, which was due to the mismatch of the boost converters' parameters. The dc voltage affects pulsating torque AC machines, accuracy in domestic watt-meter and safety of residual current protection. Furthermore, the output voltages of the boost converters showed a clipping effect, which was caused by the deadtime of the switching devices used in the boost converters.

An integral term was added to the PR controller to form the controller here called the proportional integral resonant (PIR) controller. This controller achieved satisfactory results of dc and ac voltage reference following capability and maintains the same advantages of the PI controllers. However, the efficiency was not high due to the high resistance of the inductor used in the boost inverter system.

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List of Abbreviations

PEMFC	-	Proton Exchange Membrane Fuel Cell
FC	-	Fuel Cell
dc	-	direct current
ac	-	alternating current
HF	-	High Frequency
LF	-	Low Frequency
DSP	-	Digital Signal Processor
THD	-	Total Harmonic Distortion
AFC	-	Alkaline Fuel Cell
PAFC	-	Phosphoric Acid Fuel Cell
SOFC	-	Solid Oxide Fuel Cell
DMFC	-	Direct Methanol Fuel Cell
MCFC	-	Molten Carbonate Fuel Cell
LT-PEMFC	-	Low Temperature-Proton Exchange Membrane
HT-PEMFC	-	High Temperature-Proton Exchange Membrane
CHP	-	Combined Heat and Power
MW	-	Mega-Watts
kW	-	kiloWatts
UPS	-	Uninterrupted Power Supply
RAPS	-	Remote-Area Power Supply
PV	-	Photovoltaic
PCS	-	Power Conditioning System
EMI	-	Electromagnetic Interference
PWM	-	Pulse Width Modulation
IGBT	-	Insulated Gate Bipolar Transistor
ZVS	-	Zero Voltage Switching
ZCS	-	Zero Current Switching
DCM	-	Discontinuous Conduction Mode
ZVRT	-	Zero Voltage Resonant Transition

PR	-	Proportional Resonant
PIR	-	Proportional Integral Resonant

List of Symbols

H_2	-	Hydrogen gas
O_2	-	Oxygen gas
e^-	-	Electron
H^+	-	Hydrogen Ion
$V_{out\,fc}$	-	Fuel Cell Output Voltage
E	-	Ideal Fuel Cell Voltage
V_{act}	-	Activation Voltage Loss
V_{ohm}	-	Ohmic Voltage Loss
V_{vonc}	-	Concentration Voltage Loss
Hz	-	Hertz
Vrms	-	Voltage Root Mean Square
A	-	Amperes
V	-	Volts
K_{PR}	-	PR controller
K_p	-	propotional gain
K_R	-	resonant gain
ω_o	-	fundamental frequency
s	-	Laplace Operator
D	-	Duty Cycle
i_{Lpeak}	-	Peak Inductor current
i_{Lmin}	-	Minimum Inductor Current
i_L	-	Instantaneous Inductor Current
v_L	-	Instantaneous Inductor Voltage
T_s	-	Switching period
r_L	-	Inductor's series resistance
K_I	-	Integral gain
V_{DC}	-	DC voltage component
V_{50Hz}	-	50 Hz voltage component
S_d	-	Lower switch of bridge arm
S_u	-	Upper switch of bridge arm

Ω	-	Ohms

1. Introduction

1.1 Background to the study

The South African Department of Science and Technology has identified an opportunity to capitalise South Africa's natural resources in the field of proton exchange membrane fuel cell (PEMFC) systems. The most costly component of the PEMFC is the membrane electrode assembly, which contains platinum as a catalyst component. South Africa is one of the largest platinum producers of the world. Therefore, manufacturing PEMFC in South Africa could lead to a cost-effective production of the PEMFC system, economic benefit for the country and job creation.

The PEMFC's utilize an electrochemical process to convert chemical energy of a fuel into electrical energy. The electrical energy is direct current (dc) that needs to be converted to alternating current (ac) using a power electronic dc-ac converter.

1.2 Problem Statement

There are two main topology groups used for dc-ac conversion, namely, with and without galvanic isolation. Galvanic isolation is usually in the form of a transformer and offers a safety advantage. However, topologies without the transformer offer an increased efficiency of about 1 - 2%. Furthermore, a comparison of a database of more than 400 commercially available photovoltaic PV inverters is shown in Figure 1.1 below [1].

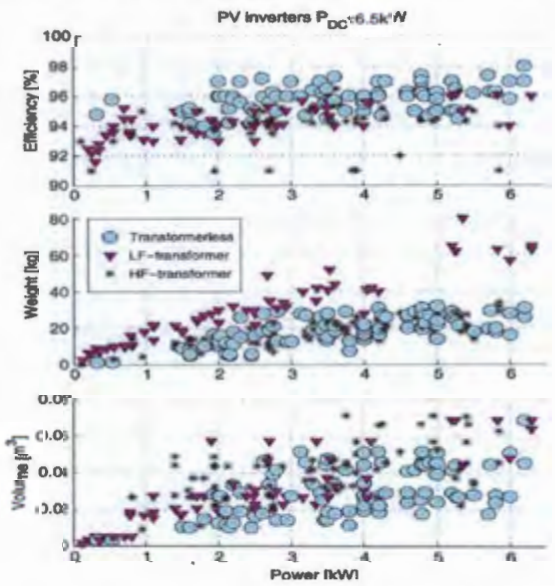


Figure 1.1: Comparison of inverters with and without galvanic isolation [1]

From the figure above, the transformerless inverters have higher efficiency and smaller weight and size than the inverters that use high frequency (HF) transformers and low frequency (LF) transformers. Thus, there is a growing interest for transfomerless topologies. In this thesis, the aim is to design a transformerless single stage power electronic inverter for a residential standalone FC system. The design of the inverter must consider its impact on the fuel cell (FC) and must provide power to typical standalone residential loads.

1.3 Objectives of Thesis

The objectives of this thesis are to:

- conduct literature review of the interaction between FCs and power electronic inverters;
- conduct literature review of transformerless single stage inverters and select an inverter to be designed;
- perform an analysis of the open loop response and closed loop strategy of the selected inverter;
- design, simulate and implement on hardware the selected inverter to verify analysis; and,
- identify typical residential standalone loads and demonstrate the handling capability of inverter for these loads.

1.4 Plan of development

Chapter 2 presents the literature review where the grid, standalone and fuel cell requirements are reviewed. The dc-ac converter that meets these requirements is selected and the aspects that are investigated for it are stated.

Chapter 3 presents a review of the existing techniques for steady-state modelling, dynamic modelling and control of single phase inverters. These techniques will be used to describe the boost inverter.

Chapter 4 covers the theoretical performance analysis of the boost inverter. The open loop and closed loop response are described. Furthermore, the deadtime effects on the open loop and closed loop response are presented.

Chapter 5 presents the design of the experimental setup of the boost inverter system. The experimental setup consists of a dc power supply, passive components, switching devices, transducers and DSP for implementation of the control system.

In chapter 6 the circuit model of the boost inverter is modelled in MATLAB Simulink such that it resembles the experimental setup as closely as possible. The simulations illustrate the open loop response, closed loop response and various disturbance rejection performance of the boost inverter system.

Chapter 7 presents the experimental results and discussions. The experimental results demonstrate the open loop response, closed loop response, various disturbance rejection performance, THD and efficiency of the boost inverter system.

In chapter 8 the conclusions are drawn from the results. Thereafter, recommendations are provided in chapter 9.

2. Literature Review

2.1 Fuel Cells

Fuel Cells (FCs) are devices that utilize an electrochemical process to convert chemical energy of a fuel into electrical energy. The fuel cell principle was discovered in 1839 by William R. Grove, a British physicist. In comparison to a battery, the battery reactants are stored internally and the battery has to be recharged or replaced when reactants are used up; whereas the reactants of the FC are stored externally and refilling fuel tanks requires less time than recharging batteries. When hydrogen, which is generated from a renewable resource, is used as fuel, the FC is considered a renewable energy technology because the reaction results in water and heat [2].

There are many types of fuels cells: alkaline fuel cell (AFC); proton exchange membrane fuel cell (PEMFC); phosphoric acid fuel cell (PAFC); solid oxide fuel cell (SOFC); direct methanol fuel cell (DMFC); and molten carbonate fuel cell (MCFC). The difference among these fuel cells is the type of electrolyte they use, which also dictates their operating temperature ranges, and the type of fuel. PEMFCs are most attractive in the South African context because of the platinum catalyst that is used. They are also a promising technology for many applications such as transportation, stationary power and backup generation. Furthermore, PEMFCs have high power density, a quick start, and the efficiency for electrical power only is in the 40-50% range [2].

The PEMFC consists of the LT-PEMFC (low temperature-proton exchange membrane) and HT-PEMFC (high temperature-proton exchange membrane). The LT-PEMFC (low temperature-proton exchange membrane) operates between 60 – 80 °C and is the most developed fuel cell and is already commercialized for backup generation [2]. The HT-PEMFC's temperature range is from 100 - 200 °C and is most suitable for residential fuel cell-based micro-CHP (Combined Heat and Power) because it offers many advantages over the LT-PEMFC: enhanced electrode electrochemical kinetics; higher efficiency; simplified water management and cooling system; waste heat can be recovered as a practical energy source [3], [4]. The HT-PEMFC is an attractive option for residential urban areas where the additional increase in capital cost can be tolerated [5].

2.1.1 *Basic Principle*

The PEMFC utilizes hydrogen and oxygen as its fuel. The structure and illustration of operation of the PEMFC is shown in Figure 2.1.

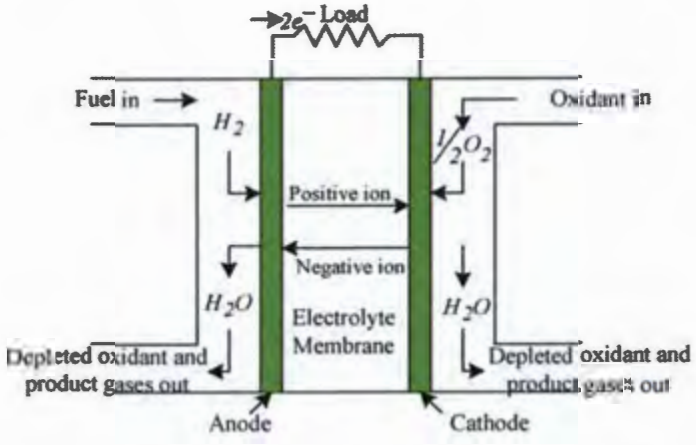


Figure 2.1: PEMFC structure and operation diagram [6].

The PEMFC's structure, in Figure 2.1, consists of two porous electrodes (cathode and anode) and an electrolyte sandwiched between the two electrodes. The electrolyte allows positive ions (protons) to pass through while blocking electrons. The hydrogen reacts with the anode electrode and the hydrogen atom is split into hydrogen ion (H^+) and electron (e^-), as shown in equation (2.1). The hydrogen ion passes through the membrane and the electrons move through the external circuit. At the cathode, the oxygen reacts with the electrons and hydrogen ions to form water and thermal energy, as shown in equation (2.2) [2], [7].

$$\text{Anode: } 2H_2 \Rightarrow 4H^+ + 4e^- \quad (2.1)$$

$$\text{Cathode: } O_2 + 4H^+ + 4e^- \Rightarrow 2H_2O \quad (2.2)$$

The difference between the structures of the HT-PEMFC and LT-PEMFC is the membrane. The LT-PEMFC uses a Nafion membrane which degrades at high temperature and passes through impurities that reduce the conductivity. However, the HT-PEMFC uses a polybenzimidazole (PBI) membrane which allows high temperature operation without drastic deterioration [8].

2.1.2 *Polarization curve*

A polarization curve, shown in Figure 2.2 represents the output voltage as a function of operating current of the PEMFC. The output voltage of a fuel cell can be written as:

$$V_{out} = E - V_{act} - V_{ohm} - V_{conc} \tag{2.3}$$

where V_{out} is the output voltage of a fuel cell, E the fuel cell ideal voltage, V_{act} the activation voltage loss, V_{ohm} the ohmic voltage loss, and V_{vonc} the concentration voltage loss [2].

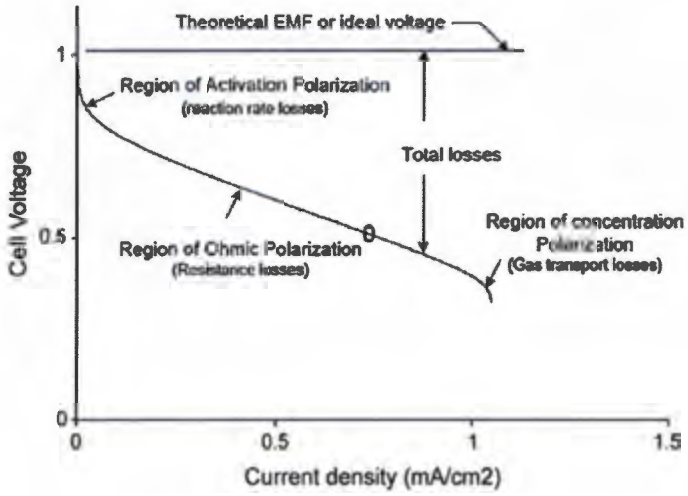


Figure 2.2: Fuel cell polarization curve [6].

The activation voltage loss is due to the slow reactions that occur at the surface of the electrodes and is larger than other voltage losses at low operating current. The concentration voltage loss is caused by the drop in concentration of the reactants of the reactants as they are consumed in the reaction. The concentration voltage loss is predominant at high operating currents. The ohmic voltage loss is caused by resistance to flow of H^+ ions through the electrolyte and the electrical resistance of the electrodes and external circuit. The ohmic voltage loss is most relevant between the activation and concentration voltage loss [7].

2.2 FC Applications and Markets

There are great efforts to commercialize fuels in the portable electronics, stationary power generation, and transportation industries. The global shipments of fuel cells increased by 214% between the years 2008 and 2011, and FCs are an emerging competitor in the back-up power for telecommunications networks market [9] and material handling market [10]. The

United States, Japan, Germany, South Korea, and Canada are leading the rest of the world in the development and commercialization FCs. Furthermore, the global FC industry market is expected to reach $19.2 billion by the year 2020 [11] and global sales are expected to grow 104% between 2010 and 2014 [12]. Figure 2.3-Figure 2.5 show the annual growth of fuel cells by application, region and fuel cell type, respectively, between the years 2008 and 2012 with respect to both number of units shipped and MWs (Mega-Watts) shipped [13].

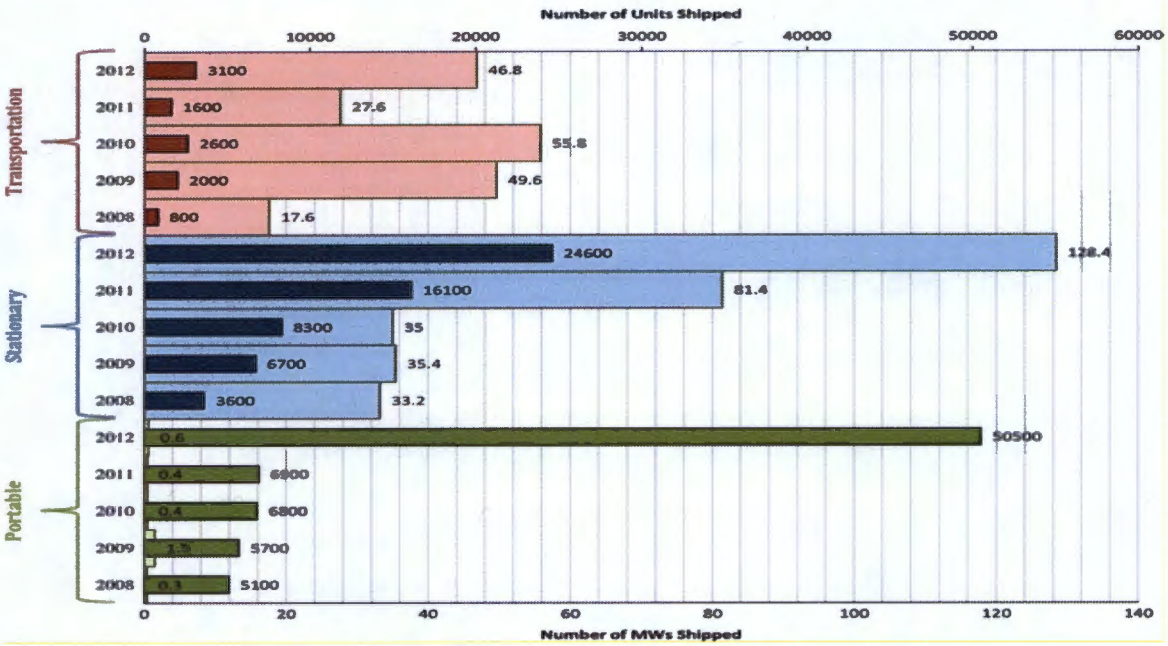


Figure 2.3: Annual growth in the FC industry between 2008 and 2012 by applications with respect to number of units (small bars) and number of MWs (large bars) shipped [13].

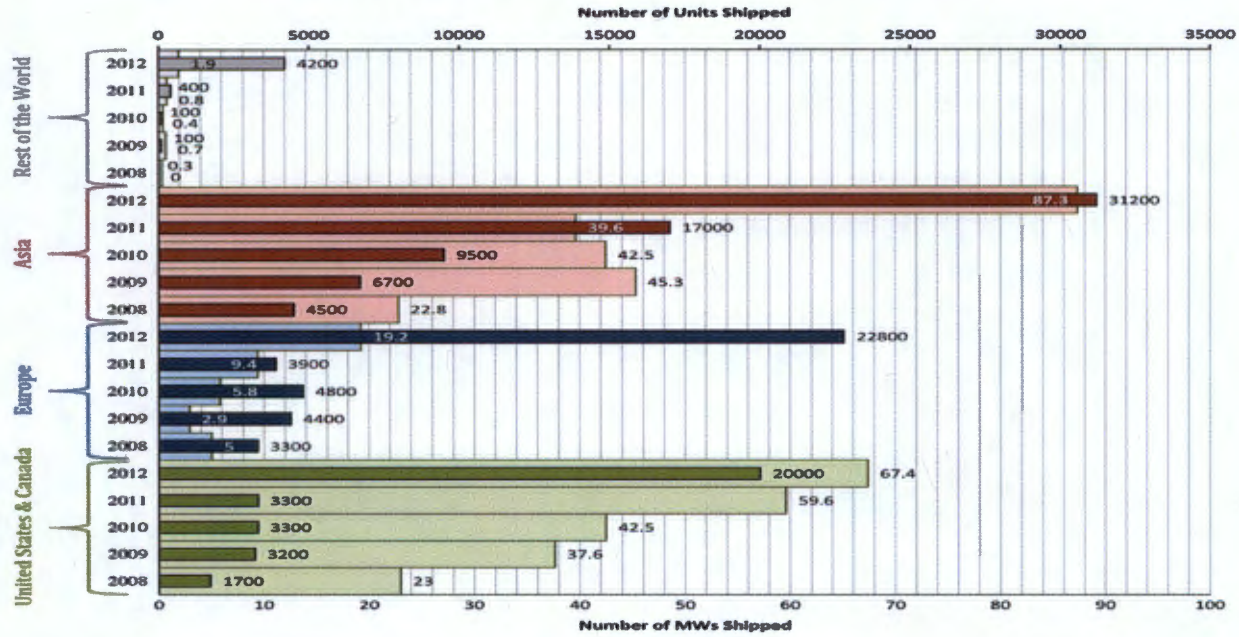


Figure 2.4: Annual growth in the FC industry between 2008 and 2012 by region with respect to number of units (small bars) and number of MWs (large bars) shipped. [13]

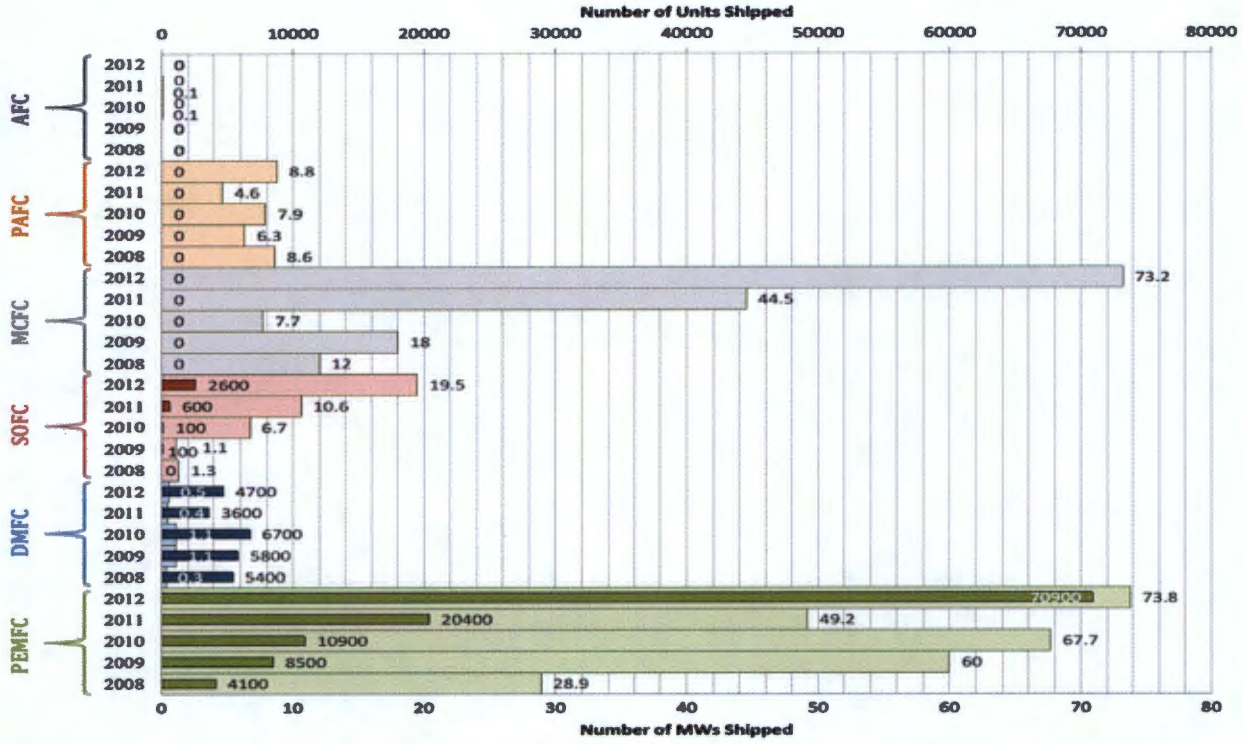


Figure 2.5: Annual growth in the FC industry between 2008 and 2012 by FC type with respect to number of units (small bars) and number of MWs (large bars) shipped. [13]

2.2.1 *Portable Applications*

The two main markets for FC portable applications are the portable power generators and consumer electronic devices. Portable power generators are designed for light outdoor personal uses such as camping, surveillance and power required for emergency relief efforts. Consumer electronic devices include laptops, cell phones, radios and basically any electronic device that traditionally operates from batteries. The modularity and high energy density of FCs, which is 5-10 times higher energy density than a typical rechargeable, make them a strong candidates for future portable personal electronics [5]. Typical power range of portable FCs is from 5 W to 20 kW [13], with micro-FCs having power outputs less than 5 W [5]. Furthermore, typical technologies used are the PEMFC and DMFC [13].

2.2.2 *Stationary Applications*

FCs in stationary applications are used to provide electricity and sometimes heat, but are not designed to be moved. They can be used as standalone and grid-connected power supplies and can play an essential role in residential, commercial, and industrial stationary power generation sectors. Stationary applications consist of uninterrupted power supply (UPS), remote-area power supply, and distributed or CHP generation [5]. Typical technologies used

in the stationary applications are the MCFC, PAFC, PEMFC, and SOFC. Moreover, the power range in this application is between 0.5 kW and 400 kW [13].

i. UPS

FCs are emerging solutions for replacing batteries in the UPS market, especially for telecommunications. In comparison to batteries, FCs have higher energy and power density, higher modularity, longer operation times (2-10 times longer than currently-used lead-acid batteries), more compact size, more reliable and ability to operate harsh ambient conditions [5], [9]. Other UPS markets are hospitals, data centres, banks and government agencies. The power range in all these markets is typically between 2 and 8 kW [5].

ii. Remote-area power supply (RAPS)

RAPS are used in grid-isolated areas, such as islands, deserts, forests, holiday resorts and remote research facilities. RAPS is a more economical solution than providing grid power lines to these locations. A RAPS can consist of a hydrogen system coupled with a renewable energy source, which typically consists of a water electrolyser, hydrogen storage mechanism, and a FC. The hydrogen system is used to compensate for the intermittency problems most renewable energy sources experience and therefore makes the system reliable and sustainable [5]. Battery storage is currently being used but there are some limitations: they can only store electrical energy for short periods (a few days) and require replacement after a few years; whereas hydrogen storage can provide low-loss of hydrogen and backup for long periods of time, such as season-to-season basis (six months or more), and can be designed for a lifetime of many years [14].

iii. Distributed power/ CHP generation

FCs are an attractive option for decentralized distributed generation. They offer advantages such as their static nature, low emissions, excellent load-following and high efficiency. FCs can be used for residential electric power or CHP distributed generation either on a household basis or a larger residential blocks basis [5]. It is estimated that by 2020, FCs could penetrate 50% of the world distributed generation market if cost and durability targets are met [15]. A residential CHP FC can provide electric power, space heating, and water heating. A CHP can reach overall efficiencies as high as 80% [5].

2.2.3 *Transportation Applications*

The transportation industry is responsible for 17% of the global greenhouse gas emissions every year. Thus, the industry needs technologies that can provide both significant reductions in harmful emissions and better conversion efficiencies. FCs are attractive solutions for both these needs because they provide nearly zero harmful emissions without compromising the efficiency of a vehicle's propulsion system [5]. Additionally, FCs are almost twice more efficient than conventional internal combustion engines [16], static in nature, offer fuel flexibility, modular, and require low maintenance. Thus, FCs are a potential solution for replacing combustion engines. However, this can be a reality if durability, cost, hydrogen infrastructure and technical targets are met on schedule [5]. Globally, the share of transportation related fuel cell shipment was about 35% and 25% of the total fuel cell systems shipment on a number of units basis and a MW-level basis, respectively, in 2010, with PEMFC as the main fuel cell type chosen [13]. The markets for the transportation industry are auxiliary power units, light traction vehicles, light duty FC vehicles, heavy-duty FC electric vehicles, aerial propulsion and marine propulsion [5].

2.3 Standalone FC Systems

Electricity is one of the most essential aspects of the success of a nation's economy. The growing electricity demands in both developed and developing countries creates grid instabilities or even outage. In developing countries where more than 50% of the population lives in rural regions, the cost of delivered electricity becomes very expensive and unaffordable to the rural poor, which causes reduced standard of living and social imbalances. The high costs of delivered electricity can be associated to the dependence on centralized energy systems that operate on mostly fossil fuels and require huge investments for establishing transmission and distribution grids that can penetrate remote regions. Furthermore, fossil fuels cause greenhouse gas emission problems [17].

Decentralized energy systems that use renewable energy sources are a solution that addresses both the economic and environmental issues. Decentralized energy systems can be operated in two ways, namely grid-connected or standalone. The grid-connected systems supply power to the local loads and any surplus generation is fed into the grid, and when there is shortage the electricity is drawn from the grid. On the other hand, standalone systems produce power independently of the utility grid [17]. These are more suitable for remote

locations where the grid cannot penetrate due to high installation costs and technical problems, such as rough terrains (forests and mountains, etc.) [5]. Moreover, the operational capacity is matched to the demand [17].

This thesis focuses on standalone fuel cell systems for remote areas. The hydrogen can be produced from renewable energy sources. An example of a hybrid system that consists of photovoltaic panels, auxiliary power source (such as ultracapacitors) and a FC system is shown in Figure 2.6.

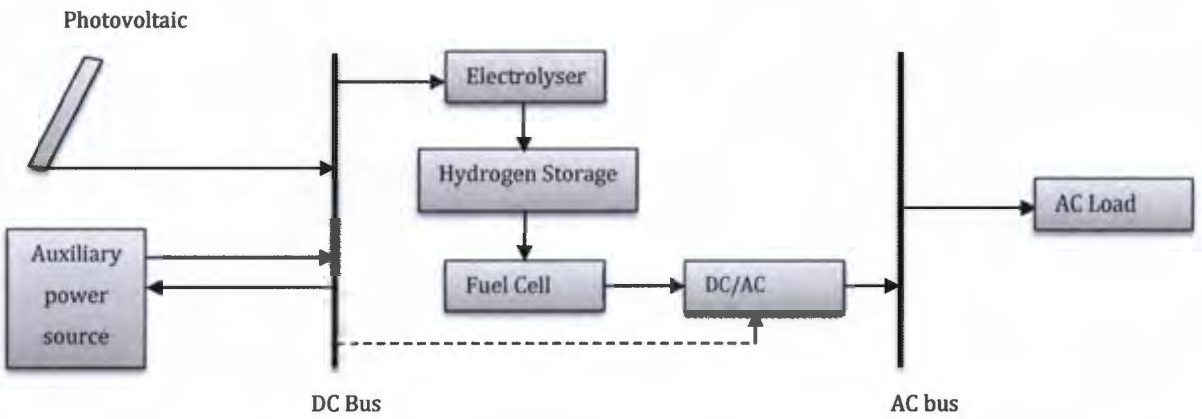


Figure 2.6: Solar-hydrogen/fuel cell hybrid energy system [18]

From the figure above, the PV panels may be used to charge the auxiliary power source and power the electrolyser. The auxiliary power supply is mainly used for short-energy supply. The electrolyser produces hydrogen that can be stored for usage in the fuel cell. The power from the fuel cell goes through a power condition system which converts the dc voltage output of the fuel cell to an ac voltage output [18].

The auxiliary power source is used to supply power during transient periods or peak demand periods. Without the auxiliary power source, the FC would have to supply all the power which increases the size and cost of the FC system. The auxiliary power source can be a battery, conventional capacitor or an ultracapacitor. However, ultracapacitors offer better energy densities than conventional capacitors and better power densities than conventional batteries. Furthermore, the charge and discharge times of ultracapacitors varies from fractions of a second to several minutes and require no maintenance. Additionally, ultracapacitors have the lowest cost per Farad and are environmentally safe. Thus, they are a cost effective for the auxiliary power source [19].

2.4 Power Conditioning System Features

The power conditioning system is an interface between the FC and the standalone load. Therefore, the requirements for the power conditioning system from the FC and standalone load are discussed.

2.4.1 FC Requirements

i. Low Frequency Current Harmonics

The instantaneous output power of single phase inverters (e.g. 220 Vrms, 50 Hz) consists of an average output power, which is constant, and a pulsating power at twice the line frequency. To maintain power balance, a FC needs to meet the power demand by drawing a current ripple at twice the line frequency [20]. However, this affects the fuel consumption and life span of the PEMFC [21]. Furthermore, hysteresis appears on the voltage and current characteristics when a PEMFC is perturbed with a 100 Hz current ripple around the dc operating point, as shown in Figure 2.7 [22].

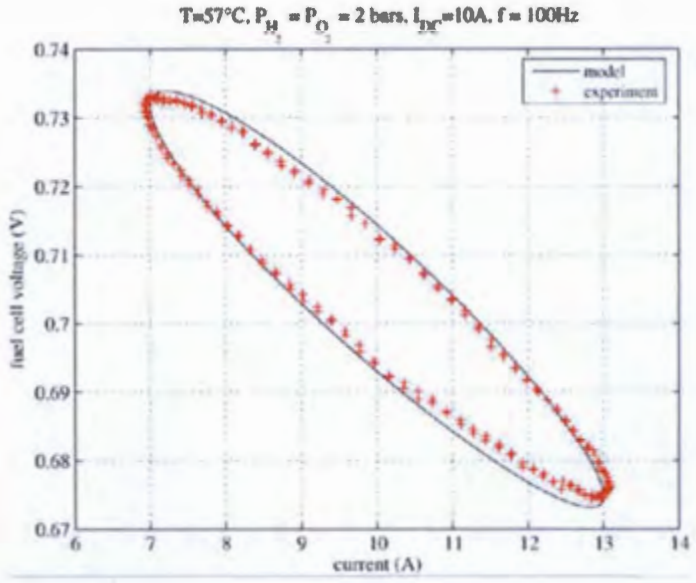


Figure 2.7: Voltage and current characteristics of a 100 Hz current perturbation around 10 A [22].

The hysteresis in Figure 2.7 is due to the time constant of the double charge layer capacitance (represents the dynamic phenomena) and the membrane resistance (represents the linear losses of the fuel cell model). These results were for a LT-PEMFC [22].

An energy storage device, such as a capacitor, is usually used for compensation (or decoupling) of the 100 Hz current harmonic [20], [23]. Other compensation methods depend on the topology selected for the power conditioning system. Single stage power conversion

topologies connected to low voltage sources such as FC and photovoltaic, result in large value electrolytic capacitors placed at voltage source side, which lower the PCS's lifetime. However, additional circuitry that allow lower value film capacitors usage can be added for compensation to increase the PCS's lifetime. Other topologies such as multi-stage power conversions, where a high voltage dc link is available, allow smaller value film capacitors to be used [20]. Furthermore, the capacitors can be further reduced by using complex control techniques that allow higher voltage ripple on the dc-link [21] .

ii. ***High Frequency Current ripples***

A PCS draws high frequency current because of the switching elements. The voltage and current characteristics are presented in Figure 2.8.

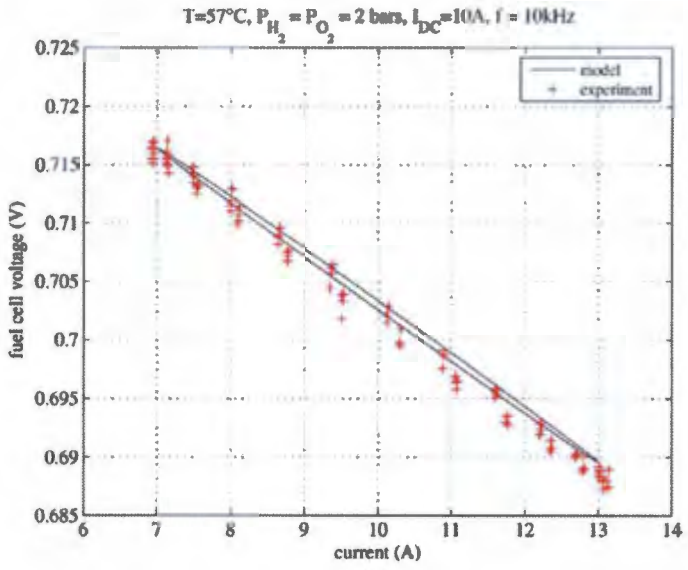


Figure 2.8: Voltage and current characteristics of a 10 kHz current perturbation around 10 A [22].

In Figure 2.8, there is no hysteresis effect around 10 kHz because the double layer capacitor does not have enough time to charge or discharge, which indicates good filtering. The voltage ripple is due to the membrane resistance [22].

2.4.2 ***Power Quality Requirements***

Most ac loads in residential households are designed to be connected to the grid, which is close to an ideal voltage source, i.e. pure sinusoidal voltage, zero internal impedance, unlimited output current, etc. Moreover, the grid has power quality standards, which include

voltage and frequency regulation, total harmonic distortion, large surge power capability, etc. However, standalone inverter systems are far from being ideal voltage sources because of limited output current, and there are no standards for standalone inverter systems, only standards for inverters connected to the grid [24].

The limitation of standards for standalone inverters is the operational differences between the grid and inverters. An example of the operational differences is illustrated in Figure 2.9 below, where start-up of a domestic drill (induction motor) is shown when it is connected to the grid in Figure 2.9(a) and to an inverter in Figure 2.9(b).

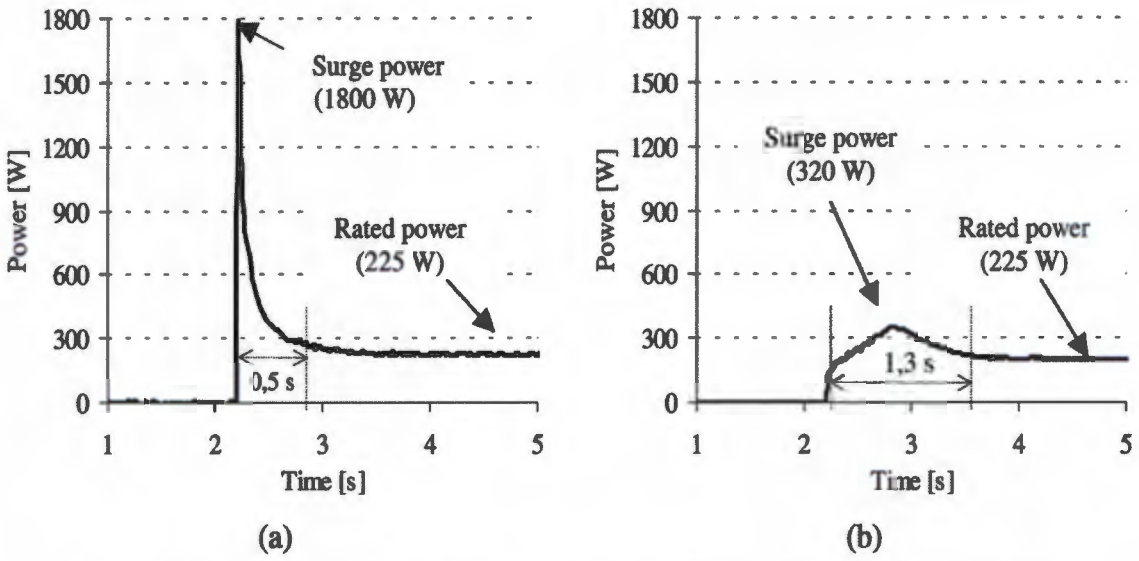


Figure 2.9: Start-up of domestic drill connected to the grid (a) and to an inverter (b) [24]

The surge power (1800 W) of the grid-connected drill is eight times greater than the rated power (225 W); whereas, the surge power of the drill connected to the inverter is reduced to (320 W), but the motor operates correctly. However, the start-up time of for the grid-connected drill is less. Therefore, performance specifications for a standalone inverter require knowledge of the AC loads that the inverter will be connected to. For cases where the AC loads are not known, the inverter can have a specification on the surge power capability based on the power switch devices [24]. However, this may lead to an oversized and costly inverter.

In literature, most performance specifications for standalone inverters are based on voltage and frequency regulation standards for the grid ([25], [26], [27]). This is because most loads have been designed and tested for grid compliance. The power quality standard EN 50160 "Voltage characteristics of electricity supplied by public distribution systems" is useful for

performance specifications. The voltage characteristics under steady state according to the standard are given in Table 2-1 and the values of the individual harmonic voltages at the supply terminals is shown in Table 2-2.

Table 2-1: Voltage Characteristics under steady state

Parameter	**Supply Voltage characteristics according to EN 501060**
Power Frequency	LV, MV: mean value of fundamental measured over 10 s $\pm$ 1% (49.5 – 50.5 *Hz*) for 99.5% of week −6%/+4% (47 – 52 *Hz*) for 100% of week
Voltage Magnitude variations	LV, MV: ±10% for 95% of week, mean 10 minutes rms values
Voltage Total Harmonic Distortion	<8%

Table 2-2: Values of individual harmonic voltages at the supply terminals

Odd harmonics				Even harmonics	
Not multiples of 3		Multiples of 3			
Order *h*	Relative voltage (%)	Order *h*	Relative voltage (%)	Order *h*	Relative voltage (%)
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.5	6 24	0.5
13	3	21	0.5		
17	2				
19	1.5				
23	1.5				
25	1.5				

The loads that are connected to the grid can be characterized on the basis of the standard EN 61000-3-2 "*Electromagnetic compatibility (EMC) part 3, limits: section 2: limits for harmonic current emissions (equipment input current ≤ 16 A per phase)*". Some loads may be non-linear and this standard provides limits for the harmonics. Therefore, standalone inverters must be designed to handle non-linear loads.

An uninterruptible power supply (UPS) is used to maintain a constant voltage and frequency supply under any nonlinear load condition and critical loads. A UPS provides good power quality because of the multiple loop control strategies that are mostly used. These include an inner capacitor or inductor current regulation feedback loop that provides fast compensation for any input disturbances and corrects for harmonic phase delays caused by the LC filter at the output stage of inverters. The reference for the current loop is generated by an outer voltage feedback regulation loop [28].

2.4.3 DC Current Requirement

The issue for allowing transfomerless inverters in grid-connected applications is the potential of dc current injection into the grid. The main concern is that distribution transformers will experience problems such as waveform distortions, excessive losses, overheating and reduced lifespan [29]. On the other hand, the main concerns of a transformerless inverter for a standalone FC system are the effects on the AC loads, which include the possibility of pulsating torque AC machines [30], accuracy problems in domestic watt-meter, safety concerns regarding residual current protection and dc enhanced metal corrosion [29]. For these reasons, standards are imposed on the level of dc current injected into the grid. For example, the EN 61000-3-2 provides a limit for dc current at 0.22A. An exception to the transformerless inverters that is inherently capable of preventing dc current injection into the load is the half-bridge inverter topology. The capacitors connected in series provide a stiff neutral point and for single phase connection and there is at least one capacitor on the output conduction path which blocks dc current. However, the half-bridge inverter requires a dc link voltage that is twice that of the full-bridge inverter. Therefore, the electrical components need to withstand high voltages [31].

There are two types of dc currents, common mode and differential mode. Common mode dc currents flow between the inverter output and dc stage. These are more common in PV inverters, where there exists a capacitance between the large surface area of the PV array and ground (shown in Figure 2.10) [32]. However, these are not common in inverters that use FCs as the main energy source [31].

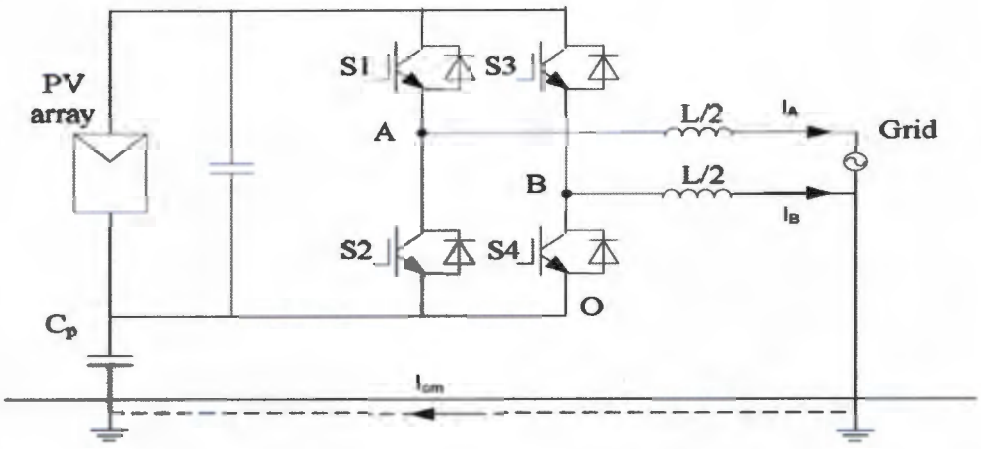


Figure 2.10: Common-mode leakage current model of single phase full-bridge inverter [32].

Differential mode dc current is caused by the offset errors in a closed-loop current measurement, which includes the errors in the analogue-to-digital converter and current sensors. The offset errors produce a slight asymmetry between the positive and negative half cycles of the current waveform, which results in differential mode dc current into the load [31]. This error is more common in inverters that use hall effect current transducers as these differential dc currents are difficult to detect compared to common mode dc currents [33]. Another source differential mode dc current, is the impedance mismatch of the two arms of the inverter bridge [34].

2.5 Power Conditioning System Architectures

The transformerless power conditioning system (PCS) architectures are discussed in this section. They are classified into three different groups: two-stage, pseudo-dc-link, and single stage topologies. Furthermore, power decoupling using a capacitor is also discussed for each architecture.

2.5.1 Two-stage Topology Architecture

The two-stage topology architecture is shown in Figure 2.11. It consists of a dc-dc converter that amplifies the FC's low voltage for the second stage. The second stage is a dc-ac converter that controls the voltage fed to the loads. The power decoupling capacitor is best placed at the dc-link because the high voltage allows a lower decoupling capacitance. A conventional configuration of such architecture consists of cascading a boost converter and a full bridge inverter [35].

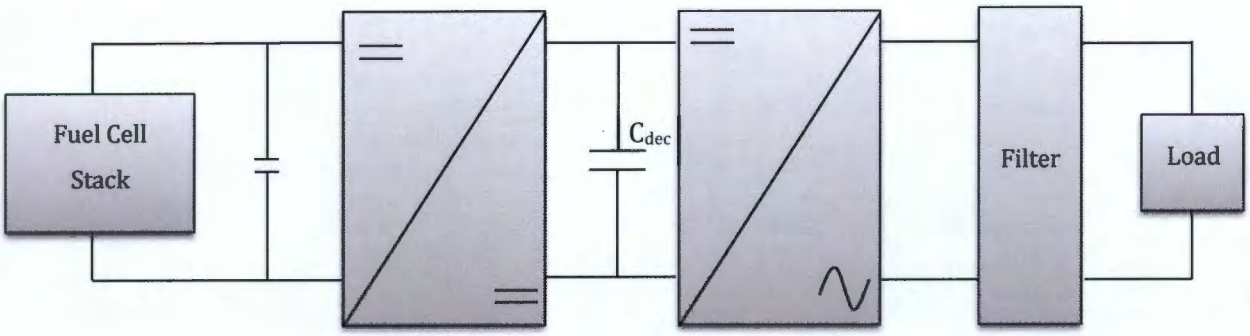


Figure 2.11: A PCS architecture for a two-stage topologies [35].

2.5.2 *Pseudo-dc-link Topology Architecture*

The pseudo-dc-link topology is shown in Figure 2.12. It consists of a dc-dc converter that produces a rectified sinusoidal voltage. The voltage is then unfolded by means of a line-switched bridge. The power decoupling capacitor is placed at the FC side. The voltage ripple of the capacitor has to be designed to be low, to avoid damaging the FC. Additionally, the FC low voltage leads to a large decoupling capacitance. In most cases, an electrolytic capacitor is used which may reduce the life span of the PCS [35].

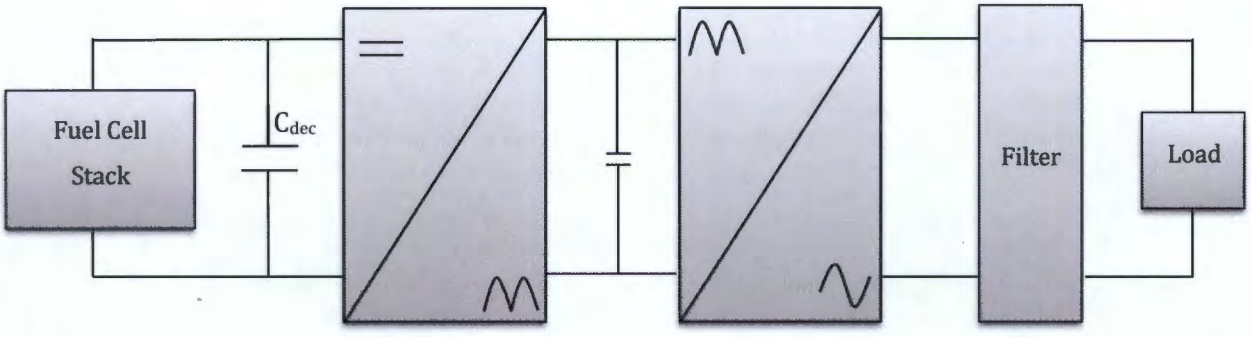


Figure 2.12: A PCS architecture for pseudo-dc-link topologies [35].

2.5.3 *Single-stage Topology Architecture*

In recent literature, the aim is to reduce the number of power stages in order to increase the overall efficiency, power density, reliability and to reduce the cost of the previous topologies discussed. The single-stage topology, shown in figure 2.13, is capable of amplifying and inverting the FC low voltage. The power decoupling capacitor is placed at the FC side, as in the pseudo-dc-link topology [35].

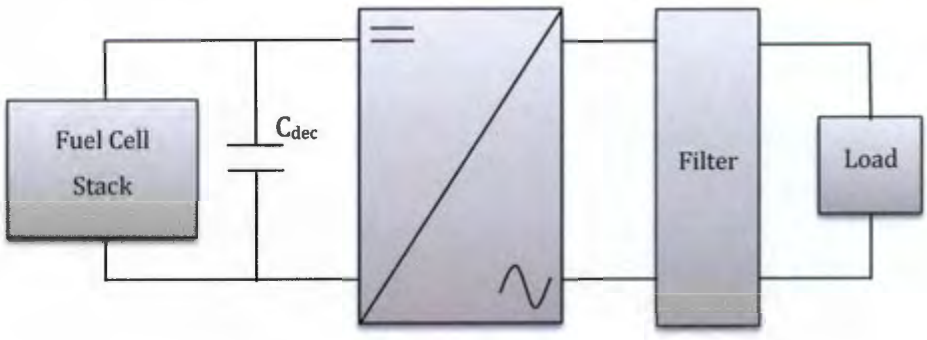


Figure 2.13: A PCS architecture for a single-stage topology [35].

2.6 Single Stage Transformerless Inverters Review

A nonisolated four-switch boost inverter, shown in Figure 2.1, uses two identical boost dc-dc converters connected in parallel to the dc source. Each boost converter produces a dc-biased sinusoidal output, which is 180° out of phase with the other, and the load is connected across the outputs of each converter. The load experiences a pure sinusoidal waveform. The output voltage of each boost converter has to be higher than the dc voltage source at every instant of the ac voltage [36].

A similar buck-boost inverter, Figure 2.15, that uses two buck-boost converters was proposed in [37]. The difference is that the output voltage of each converter has to be higher than zero volts. Therefore, lower voltage stress is obtained on the output capacitor and power switches [37].

An alternative buck-boost inverter, Figure 2.16, that requires a split dc input voltage has also been proposed. In this case, two buck-boost converters share the same output and operate at each half cycle with their own supply source [38].

The transformer used leads to an expensive solution [39], [40].

A zero-current-switching (ZCS) buck-boost inverter topology, shown in Figure 2.17, was proposed in [41].

Switches S1, S3 and diode D2 operate in the positive half cycle while switches S2, S4 and diode D1 operate in the negative half cycle. To achieve ZCS, switches S4 and S3 operate under discontinuous mode of operation [41].

A nonisolated six-switch, Figure 2.18, charges an energy-storage inductor from different directions in each half cycle, which generates an ac output. The additional switches facilitate the grounding of the grid and PV [42].

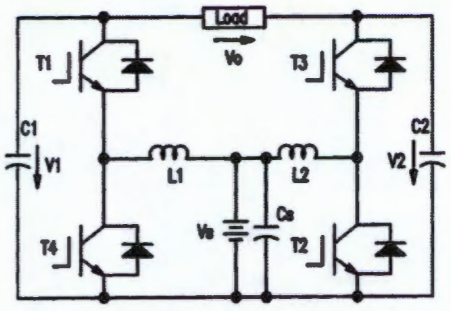


Figure 2.14: Four-switch boost inverter [36]

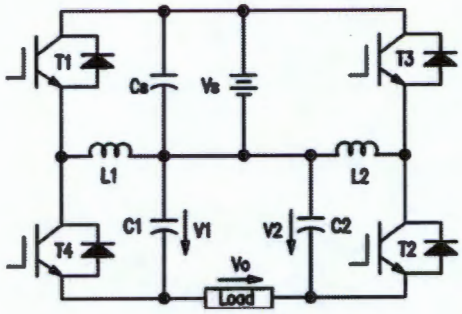


Figure 2.15: Four-switch buck-boost inverter [37]

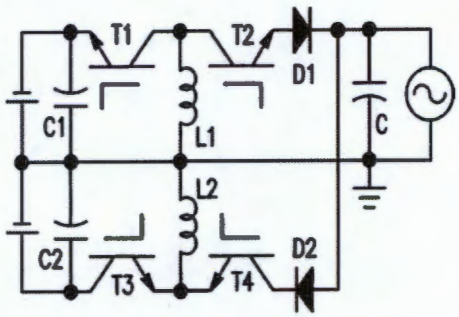


Figure 2.16: Four-switch split supply buck-boost inverter [38]

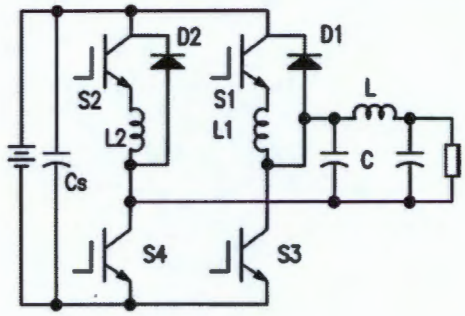


Figure 2.17: Four-switch resonant buck-boost inverter [41]

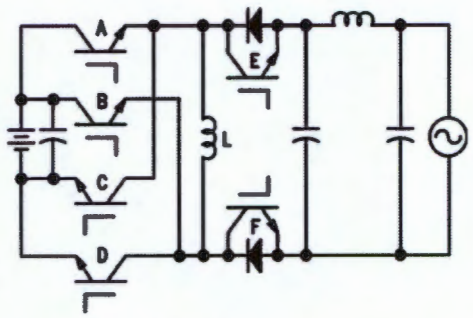


Figure 2.18: Six-switch buck-boost inverter [42]

From the topologies above, the boost inverter has been used for standalone and grid connected PEMFC applications with a backup unit for the low frequency current ripple and slow dynamics of the PEMFC compensation [43], [44]. Thus, the boost inverter is selected for further study. Furthermore, the boost inverter has been extended to a three-phase topology [45]. The boost inverter was introduced with sliding mode control [36].

2.7 Boost Inverter Review

2.7.1 Control of boost inverter

The boost converters of the boost inverter are controlled to give an ac voltage. The boost converter's controllers are usually designed to control around a dc operating point using a small-signal linear model. However, these methods are not valid for the boost converters of the inverter because the operation point experiences large variations around the dc operating point [46].

The sliding mode control was used when the boost inverter was proposed in [36]. The control strategy was able to produce good steady state results for variable operation of the boost converters. However, the sliding mode control has drawbacks: it requires complex theory; variable switching frequency; lack of inductor average-current control; parameter selection are limited by the controller; cannot deal with nonlinear loads, abrupt load variations and transient short circuit situations [46].

A double-loop control scheme that overcomes sliding mode disadvantages was proposed in [46]. It was proposed with proportional integral PI controllers in each loop. Recently, proportional resonant (PR) controllers were used in each of the loops [47]. The PR controllers were proposed for purely sinusoidal current control in a three phase conventional buck inverter and could also be applied to single phase buck inverters [48]. However, the boost converters of the boost inverter have to track a dc biased sinusoidal voltage, which might give unsatisfactory results in reaching zero steady error.

Three phase stationary frame control was regarded unsatisfactory because the PI controllers suffered from significant steady-state amplitude and phase errors. The synchronous frame *d-q* control was regarded as superior because zero steady-state can be achieved by acting on dc signals in the rotating reference frame. However, a synchronous frame control is more complex because of the transformation of the stationary frame ac current (or error) to rotating frame dc quantities and the transformation back to stationary frame for implementation. The PR controller was developed to be applied in the stationary frame control for single and three phase systems to achieve the same steady-state and transient performance as a synchronous frame PI controller. The PR controller was developed by exploring the relationship between stationary and synchronous frame controllers from a control system and signal processing point of view, and transforming the controller transfer

function instead of the ac current error [48]. The PR controller's transfer function can be written as [48]:

$$K_{PR} = K_p + \frac{2K_R s}{s^2 + \omega_o^2} \tag{2.4}$$

where K_p is the propotional gain, K_R is the resonant gain and ω_o is the reference signal frequency.

2.7.2 *Switching Techniques*

The demand for power inverters with low output harmonic distortion, improved dynamic performance and higher power density, can be met with operation of high switching frequencies. However, operation at high switching frequency is limited by: switching stresses (high voltage and current peaks) on the power devices during turn-on and turn-off; switching losses; high di/dt and dv/dt which produces electromagnetic interference (EMI) [49].

Various soft-switching techniques have been proposed in literature for the traditional buck inverter to achieve operation at high switching frequency. Soft-switching in the traditional buck inverter is achieved by adding an auxiliary resonant circuit on the dc link or ac link and can be zero current or/and zero current switching. The ac link soft-switching inverters offer the advantages of PWM control without additional voltage or current stress in the power devices over the dc link soft-switching inverter. Thus, the ac-link soft-switching inverters are the most promising and developed [50]. However, the number of components is increased with the application of ac-link soft-switching inverters, and the complexity is increased. Thus, they are not widely used in commercial applications [39].

Bidirectional dc-dc converters that can achieve soft-switching without additional circuitry have been proposed in literature [51], [52]. The boost inverter uses two bidirectional boost converters and the dc-dc bidirectional soft-switching converter (with the same topology as the bidirectional boost converter) techniques have not been used for the boost inverter. Thus, the dc-dc bidirectional soft-switching converter is reviewed in this sub-section. But, firstly a description of soft-switching is covered.

i. Soft-switching descriptions

The hard-switching operation of inverters, shown in Figure 2.19a, has several problems. During turn-on, the power switch's current rises to the load current with additional diode reverse recovery current and the needed current to charge and discharge the intrinsic capacitors of the power switch. During turn-off, the power switch's voltage rises to the dc bus

voltage with additional voltage overshoot, due to the leakage inductance in the circuit. The overlapping voltage and current result in high switching losses. Furthermore, the high current and voltage variation rates cause severe EMI during the switching periods [53], [49].

Soft-switching techniques reduce the switching losses by reducing the overlap between voltage and current during the switching period. Therefore, high switching frequency operation can be accomplished. Soft-switching techniques can be classified into zero voltage switching (ZVS) and zero current switching (ZCS) [49].

The ZVS operation is shown in Figure 2.19b. The power switch's voltage is zero at turn-on by the use of an auxiliary circuit or circuit parameters. The turn-off losses are also reduced by snubber capacitors which slow down the voltage rise. When IGBTs (Insulated Gate Bipolar Transistors) are used as the switching power device the turn-off losses caused by the tail current cannot be totally avoided [49], [51].

The ZCS switching waveform is shown in Figure 2.19c. The power switch's current is zero at turn-off by the use of the auxiliary circuit or circuit parameters. The turn-on losses are reduced by either an inductor or auxiliary circuit [49]. The ZCS is considered more effective than ZVS for slow IGBTs [54].

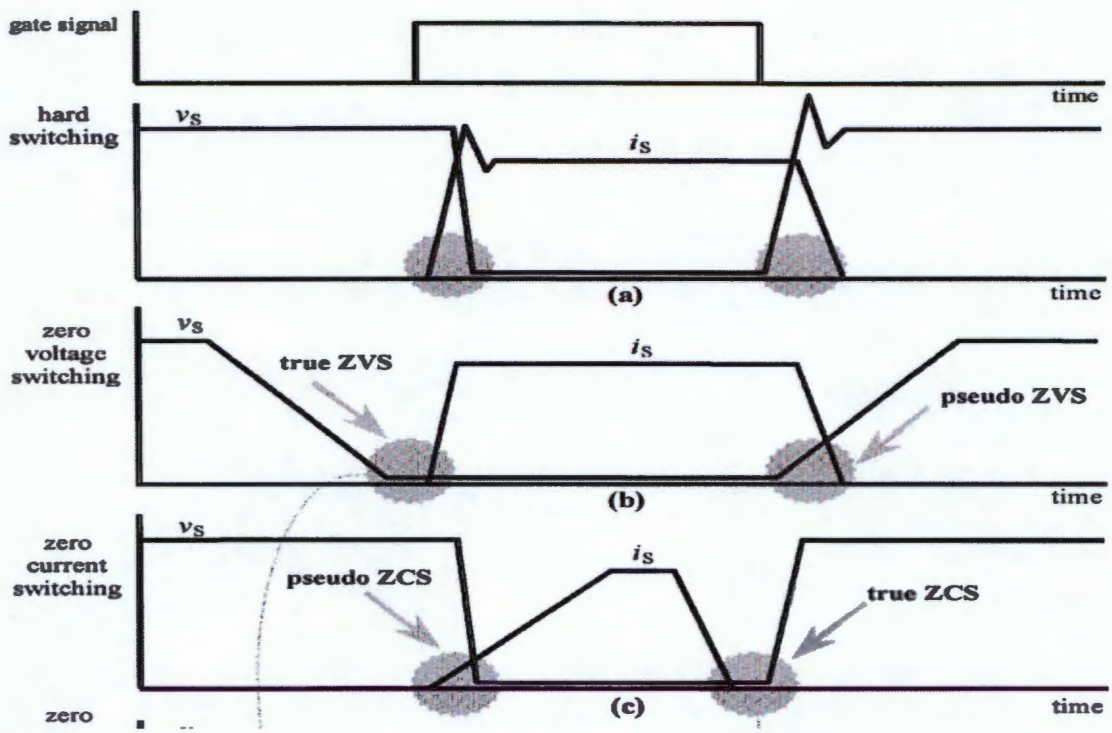


Figure 2.19: Switching waveforms [49]

ii. ***Bidirectional dc-dc converters***

The considered bidirectional dc-dc converter topology is shown in Figure 2.20. The multi-phase topology is for reducing IGBT stress and cancellation of current ripple. The ZVS operation can be obtained naturally in the bidirectional converter. The inductor is sized so that the current always starts from a negative value to obtain ZVS [51]. This operation will be described further in section 4.3.2. The efficiency of the converter has been further improved by using a multi-frequency PWM strategy [55], as shown in Figure 2.21. The discontinuous conduction mode (DCM) operation has also been explored. However, there was parasitic ringing between the power switch's capacitance and inductor [56].

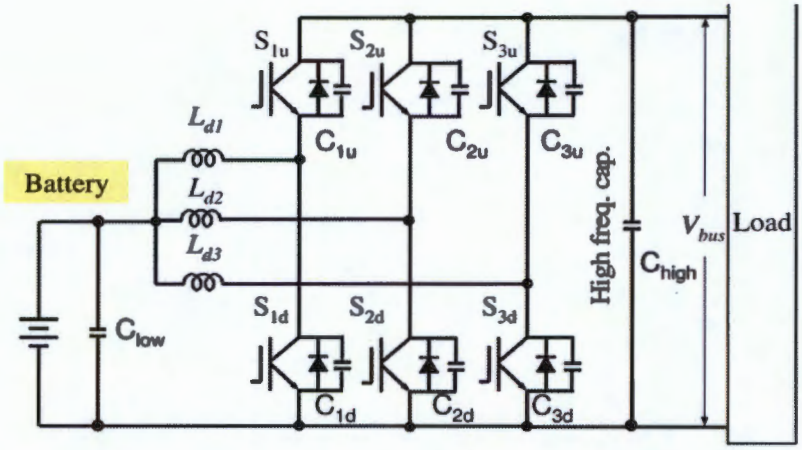


Figure 2.20: Three phase interleaved bidirectional converter [51]

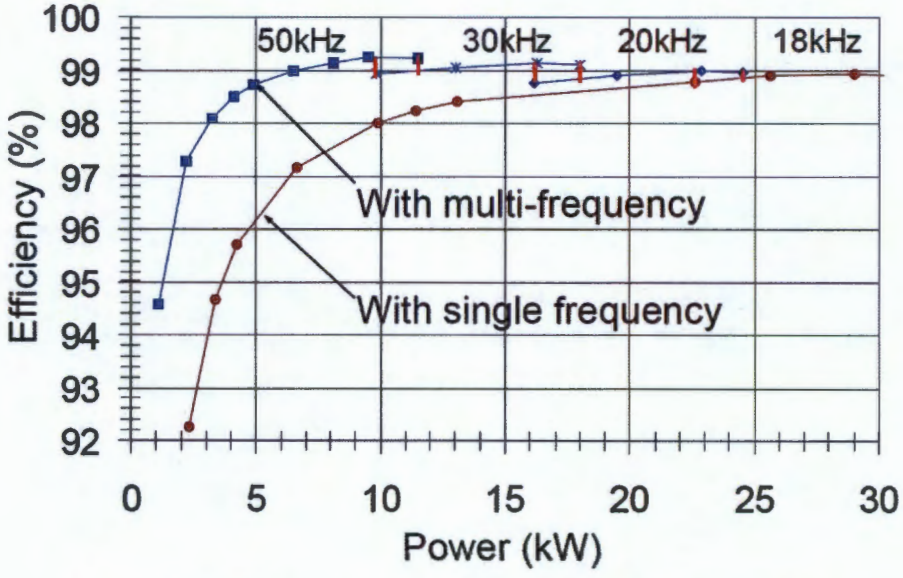


Figure 2.21: Efficiency results for different switching strategies [55]

2.7.3 *Passive Components of Boost Inverter*

Passive components in the boost inverter are designed based on high switching frequency current and voltage ripple specifications. In order to understand the performance of the passive components in the fundamental frequency range, the LCL filter sizing methods are reviewed. LCL filters are used for filtering in power inverters. LCL filters offer a better attenuation than LC filter given the similar size and are better solutions when a low switching is required because the size of the LC filter becomes large [57].

i. Inductor Sizing

The selection of the inductor size is based on the current ripple requirement. The ripple requirement is a trade-off among inductor, IGBT switching and conduction losses and core losses. The smaller the current ripple, the lower the IGBT switching and conduction losses, but the larger the inductor results in core losses. The current ripple is usually specified from 15 -25% of rated current [57].

ii. Capacitor Sizing

Reactive power of the capacitor is a criterion for specification of the capacitor size. A large capacitance results in more reactive power flowing into the capacitor. Therefore, current in the inductor and switches is increased, which lowers the efficiency [57].

2.8 Observations from Literature Review

The boost inverter is based on controlling two boost converters and the boost converter is widely used for many applications. Furthermore, the boost inverter has also been successfully applied to standalone fuel cell applications. Therefore, it is selected as the single stage inverter to be analysed, simulated and built in hardware for this thesis. However, the following aspects, which are covered for the traditional single phase buck inverter, were not found in literature:

a) The deadtime effect on the open loop response.

b) The switching techniques that the boost converters of the boost inverter undergo throughout the full cycle of the inductor current.

c) The ability of the PR controller to eliminate dc offsets on the boost inverter output.

These aspects are studied in this thesis. The approach of addressing these is to review the modelling and control of widely used single phase inverters, afterwhich similar methods will be applied to the boost inverter.

3. Overview of Single Phase Inverters

This chapter presents a review of the existing techniques for steady-state modelling, dynamic modelling and control of single phase inverters. Additionally, only the steady state modelling techniques for converters will be discussed because they will be used in chapter 4.

3.1 DC-DC Converters in Steady State

In power electronics, a steady state condition is reached when the circuit waveforms repeat with a time period T that depends on the specific nature of the circuit. The voltage and current waveforms of the circuit in steady state can be written as follows [58]:

$$v(0) = v(T) \tag{3.1}$$

$$i(0) = i(T) \tag{3.2}$$

The dc voltage and current components in a switching converter can be found by the use of two principles: the *inductor volt-second balance and capacitor charge balance* [59]. These principles are useful for analysing converters and will be presented in this subsection.

The principle of *inductor volt-second balance* can be shown by considering the circuit in Figure 3.1. The relationship of an inductor voltage ($v_L(t)$) and current ($i_L(t)$) is as follows:

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{3.3}$$

Further integrating over one switching period results in:

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)dt \tag{3.4}$$

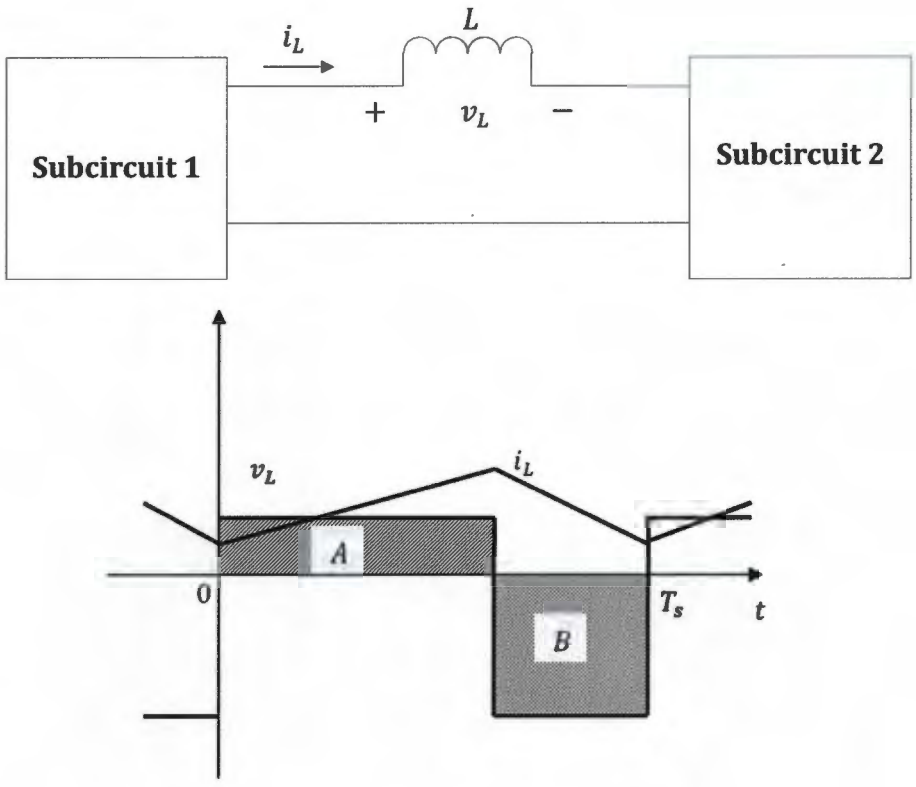


Figure 3.1: Inductor Response in steady state.

By substituting equation (3.2) into equation (3.4), yields

$$0 = \int_0^{Ts} v_L(t)dt \tag{3.5}$$

The right hand side of equation (3.5) has the units of volt-seconds or flux-linkages. Equation (3.5), which is the principle of inductor volt-second balance, states that the total area, or net volt-seconds, under the $v_L(t)$ waveform must be zero.

An equivalent form of equation (3.5) can be obtained by dividing both sides by the switching period.

$$0 = \frac{1}{T_s}\int_0^{Ts} v_L(t)dt \tag{3.6}$$

The right hand side represents the average value or dc component of the inductor voltage, which states that applied inductor voltage must have a zero dc component. Otherwise, the inductor flux will increase continuously and the inductor current would increase without

bound. The principle of *inductor volt-second* balance allows determination of the dc voltage components in any switching converter [59].

In a similar approach, the principle of *capacitor charge balance* is developed by considering Figure 3.2.

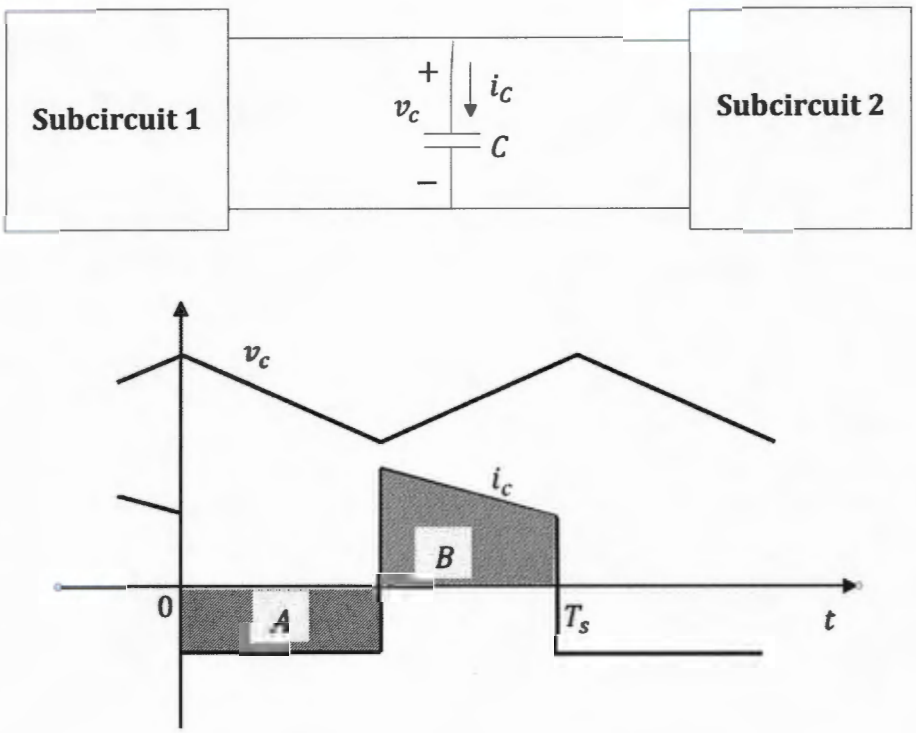


Figure 3.2: Capacitor response in steady state.

The relationship of a capacitor voltage ($v_C(t)$) and current ($i_C(t)$) is as follows:

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{3.7}$$

Further integrating over one switching period results in:

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{Ts} i_C(t)dt \tag{3.8}$$

By substituting equation (3.1) in equation (3.8), yields

$$0 = \int_0^{T_S} i_C(t)dt \tag{3.9}$$

The right hand side of equation (3.9) has the units of amp-seconds or charge. Equation (3.9), which is the principle of *capacitor charge balance*, states that the total area, or net amp-seconds, under the $i_C(t)$ waveform must be zero [59].

An equivalent form of equation (3.9) can be obtained by dividing both sides by the switching period.

$$0 = \frac{1}{T_s}\int_0^{T_S} i_C(t)dt \tag{3.10}$$

The right hand side represents the average value or dc component of the capacitor current, which states that applied capacitor current must have a zero dc component. Otherwise, the capacitor charge would increase continuously and the capacitor voltage would increase without bound. The principle of *capacitor charge balance* allows determination of the dc current components in any switching converter [59].

3.2 Steady-State Modelling of Inverters

The boost inverter uses a pulse width modulation (PWM) strategy to control the fundamental output voltage. Therefore, the focus of this subsection is on pulse width modulated inverters. The sinusoidal pulse-width-modulation (SPWM) strategy is similar to the boost inverter's PWM strategy. Other strategies, such as space vector PWM and square wave strategies are used for three-phase systems and motor type loads, respectively [58]. Therefore, only the SPWM is presented in this subsection. Additionally, an averaging-based method which is used to determine steady state conditions of SPWM inverters is covered.

3.2.1 Steady-State Model of SPWM Inverter

Sinusoidal PWM is a method of producing a sinusoidal output voltage waveform by comparing a sinusoidal control signal (also called modulating signal), v_{con}, at the desired frequency with a triangular waveform (also called carrier waveform), v_{tri}, as shown in Figure 3.3.

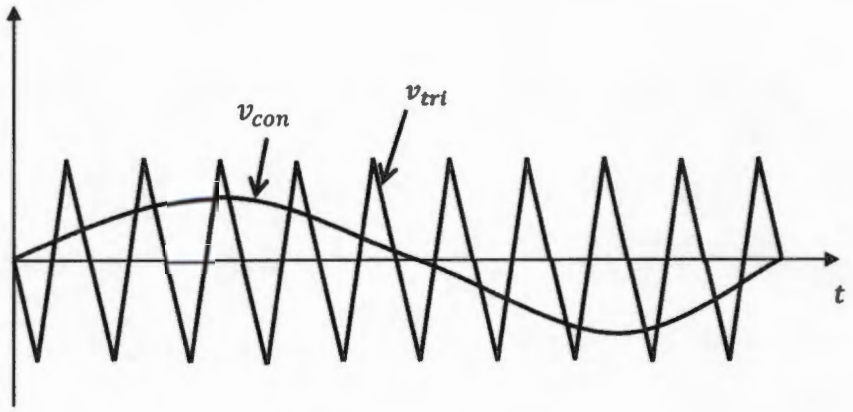


Figure 3.3: SPWM strategy.

The triangular waveform's frequency, f_s, is the switching frequency of the inverter, which is generally kept constant along with its amplitude. The control signal's frequency, f_1, is the desired fundamental frequency of the inverter voltage output and the signal is also used to modulate the switch duty ratio. The ratio between the amplitude of the control voltage, $V_{con\,pk}$, and the triangular waveform, $V_{tri\,pk}$, is defined as the amplitude modulation ratio, $m_a = V_{c\,pk}/V_{tri\,pk}$. Furthermore, the ratio between the switching frequency and the desired fundamental frequency is known as the frequency modulation ratio, $m_f = f_s/f_1$.

In order to further explain the SPWM, an example of its application is discussed using the one-leg switch-mode inverter shown in Figure 3.4.

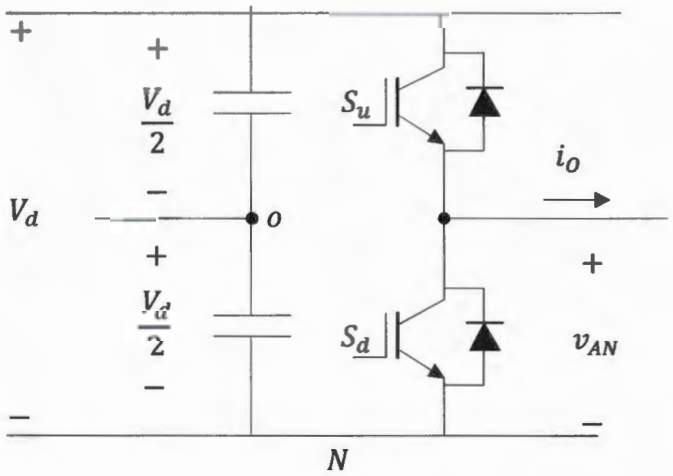


Figure 3.4: One-leg switch-mode inverter [58].

The switches S_u and S_d are controlled based on the comparison of v_{con} and v_{tri}. The output voltage is independent of the direction of the output current because of the bidirectional switches. Therefore, the output voltage is as follows:

$$v_c > v_{tri}, \quad S_u \text{ is on}, \quad v_{Ao} = \frac{1}{2}V_d \tag{3.11}$$

Or

$$v_c < v_{tri}, \quad S_d \text{ is on}, \quad v_{Ao} = -\frac{1}{2}V_d \tag{3.12}$$

The two switches are never switched on at the same time and results in an output voltage v_{Ao} that fluctuates between ($\frac{1}{2}V_d$ and $-\frac{1}{2}V_d$). The output voltage, v_{Ao}, and the desired fundamental frequency component, v_{AO1} are shown in Figure 3.5 (d), where $m_a \leq 1$.

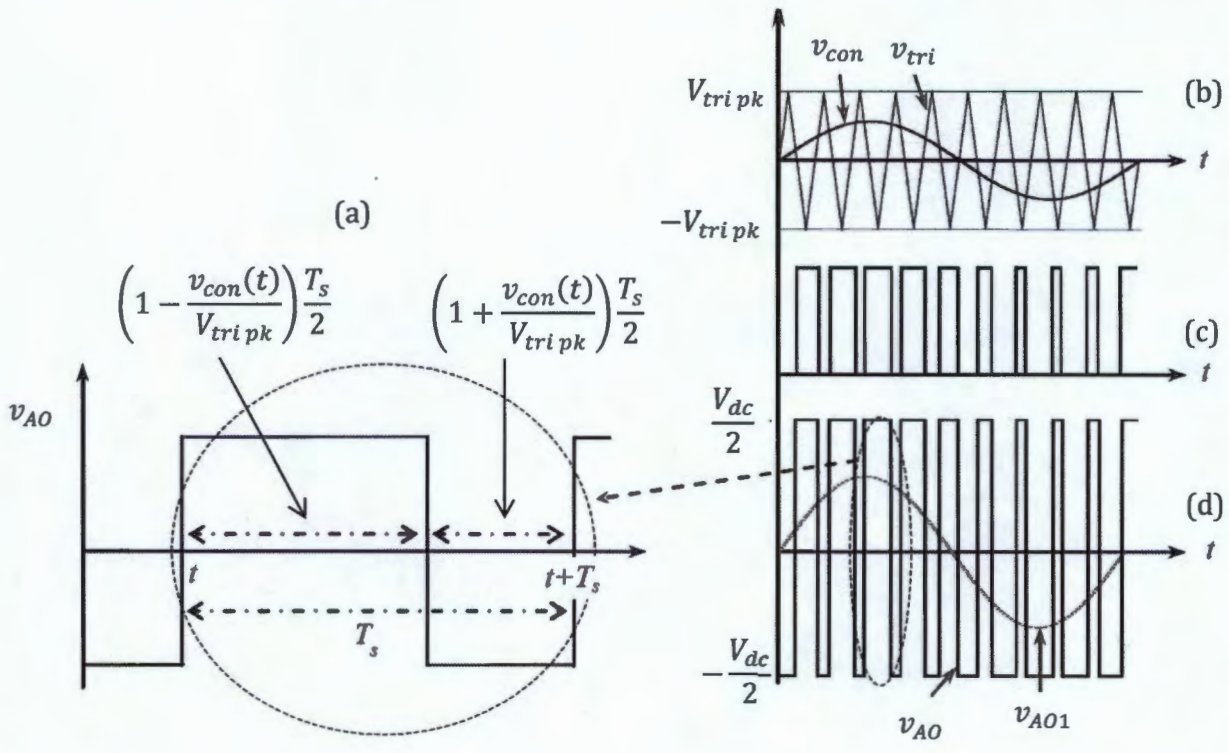


Figure 3.5: Steady state modelling of one-leg sinusoidal PWM inverter by averaging, a) v_{AO} over switching period, b) SPWM, c) PWM signal to switch and d) output voltage v_{AO} [60]

In order to determine the fundamental frequency component ($(v_{AO})_1$), the control signal is initially considered to be constant. The resulting average output voltage, V_{Ao}, over one switching period is shown in Figure 3.5 (a) and can be written as follows [60]:

$$V_{Ao} = \frac{1}{T_s}\left\{\left(1 - \frac{v_{con}(t)}{V_{tri\,pk}}\right)\frac{T_s}{2}\frac{V_{dc}}{2} - \left(1 + \frac{v_{con}(t)}{V_{tri\,pk}}\right)\frac{T_s}{2}\frac{V_{dc}}{2}\right\}$$
$$V_{AO} = \frac{v_{con}(t)}{V_{tri\,pk}}\frac{V_{dc}}{2} \tag{3.13}$$

where, $v_{con}(t)$ is constant. Furthermore, assuming that $v_{con}(t)$ varies very little during a switching period, which implies m_f is large. Hence, it can be assumed $v_{con}(t)$ to be constant over a switching period and equation (3.13) indicates how the 'instantaneous average' value of v_{AO} varies in every switching period. This 'instantaneous average' is the same as the fundamental-frequency component of v_{Ao}. Therefore, $v_{Con}(t)$ is chosen to be sinusoidal at the desired fundamental frequency of the inverter ([60], [58]):

$$v_{con}(t) = V_{c\,pk}\sin(2\pi f_1 t) \tag{3.14}$$

Where

$$V_{con\,pk} \leq V_{tri\,pk}$$

Therefore, using equation (3.13) and equation (3.14), results in:

$$(v_{AO})_1 = \frac{V_{con\,pk}}{V_{tri\,pk}}\sin(2\pi f_1 t)\frac{V_d}{2}$$
$$= m_a \sin(2\pi f_1 t)\frac{V_d}{2} \tag{3.15}$$

which indicates that the amplitude of the fundamental frequency component of the output voltage varies linearly with m_a, provided $m_a \leq 1$. Therefore the range of m_a from 0 to 1 is referred to as the linear range [58].

The harmonics in the output voltage, v_{Ao}, appears as sidebands, centered around switching frequency, f_S, and its multiples which is around the harmonic orders m_f, $2m_f$,$3m_f$ and so forth [58].

In order to further increase the possible amplitude of the fundamental frequency component, the amplitude can be increased beyond 1. The resulting relationship of the modulation ratio and the amplitude of the fundamental frequency component are shown in Figure 3.6.

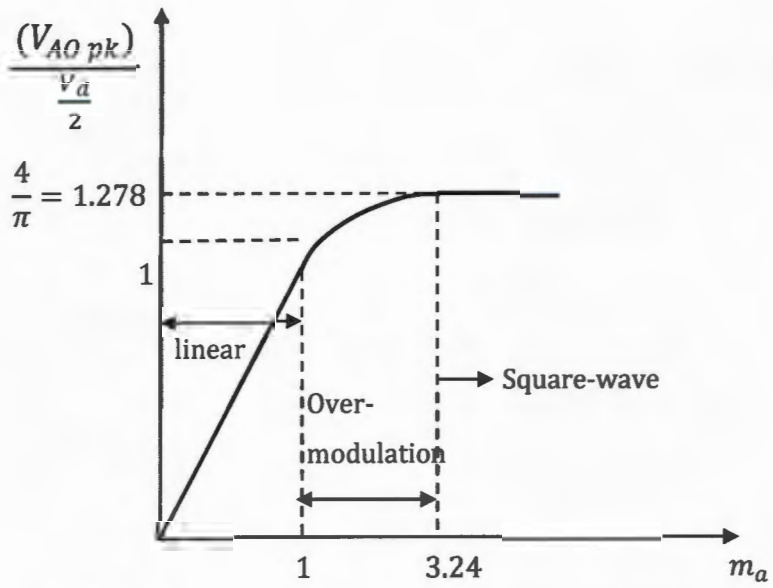


Figure 3.6: Voltage control by varying m_a (for $m_f = 15$) [58].

In the overmodulation region, the amplitude of the fundamental component does not vary linearly with the amplitude modulation ratio. Moreover, overmodulation causes the output voltage to contain more harmonics on the sidebands. Overmodulation is not used in uninterruptible power supplies because high power quality is required. It is normally used for induction motor drives. Furthermore, for large values of m_a the inverter output voltage waveform becomes a square wave [58].

3.2.2 Input Side Current

It was shown in section 2.4.1i, that the current ripple at twice the desired fundamental frequency damages the FC. This current ripple is explained in this section by considering the circuit in Figure 3.7.

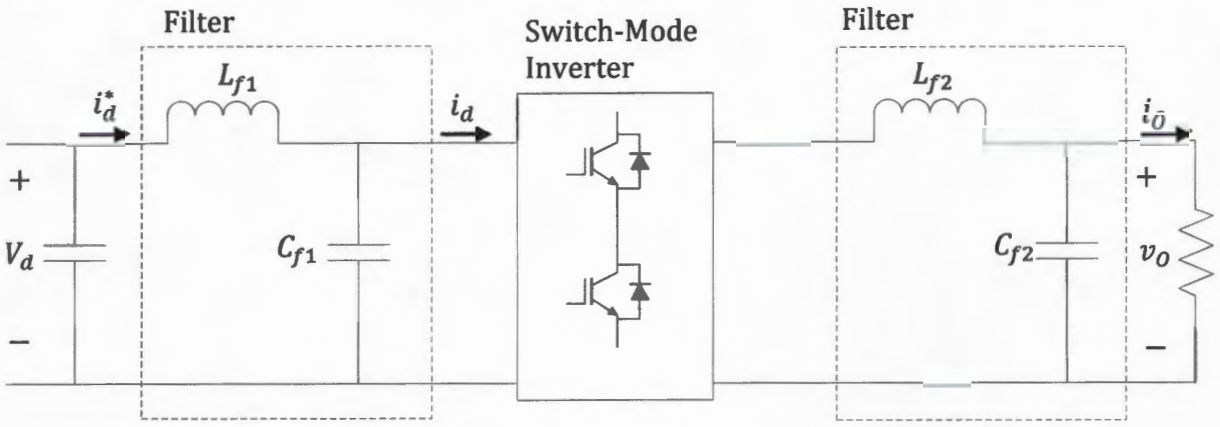


Figure 3.7: Inverter with fictitious filters [58].

In the figure above it is assumed that the switching frequency approaches infinity. Thus, the LC filters on the ac and dc side approach zero and the energy stored in filter is negligible. Furthermore, assuming the same inverter as in Figure 3.7, where there are no energy storage elements, the instantaneous power input must equal the instantaneous power output.
The foregoing assumptions result in a pure sine wave output:

$$v_{o1} = v_o = \sqrt{2}V_o \sin(\omega_1 t) \tag{3.16}$$

where $\omega_1 = 2\pi f_1$. Moreover, the output current for the resistive load is also sinusoidal and in phase with the output voltage:

$$i_o = \sqrt{2}I_o \sin(\omega_1 t) \tag{3.17}$$

On the dc side, the LC filter will filter high switching frequency in i_d and i_d^* would only consist of the low frequency and dc components.
Assuming no energy is stored in the filters,

$$V_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2}V_o \sin(\omega_1 t)\sqrt{2}I_o \sin(\omega_1 t) \tag{3.18}$$

Therefore

$$i_d^*(t) = \frac{V_o I_o}{V_d} - \frac{V_o I_o}{V_d}\cos(2\omega_1 t) \tag{3.19}$$

Equation (3.19) shows that i_d^* consists of a dc component and a sinusoidal component at twice the fundamental frequency which would damage the FC [58].

3.2.3 *Dead Time Effects*

In the previous sections the switches were assumed to be ideal, which meant that the switches in an inverter leg could be turned on and off instantly. However, in practice a switch has a finite turn-on and turn-off time. Therefore, in order to avoid cross conduction or shoot-through in an inverter leg, the turn-on of the other switch is delayed by a deadtime t_d.
During the deadtime period, both the switches of the inverter are off. Therefore, there is an effect on the output voltage. For demonstration purposes of the effect on the output voltage, the one leg of a single phase inverter is used in Figure 3.8, and the focus is only on one switching period [58].

Since both switches are off during the deadtime, V_{AN} during that interval depends on the direction of i_a as shown in Figure 3.8 (d) and (e) for $i_A > 0$ and $i_A < 0$, respectively. The ideal waveforms (without deadtime) are shown as dotted. The difference between the ideal and the actual output voltage is

$$v_e = (v_{AN})_{ideal} - (v_{AN})_{actual} \tag{3.20}$$

By averaging over one switching period, the resulting change in the output due to t_d is:

$$\Delta V_{AN} = \begin{cases} +\frac{t_d}{T_S} V_d & i_A > 0 \\ -\frac{t_d}{T_S} V_d & i_A < 0 \end{cases} \tag{3.21}$$

Equation (3.22) shows that the polarity of ΔV_{AN} depends only on the current direction. The magnitude of the current does not affect ΔV_{AN}. Moreover, ΔV_{AN} is propotional to the blanking time t_d and the switching frequency. Therefore, at higher switching frequencies the switching device has to allow for small deadtime [58].

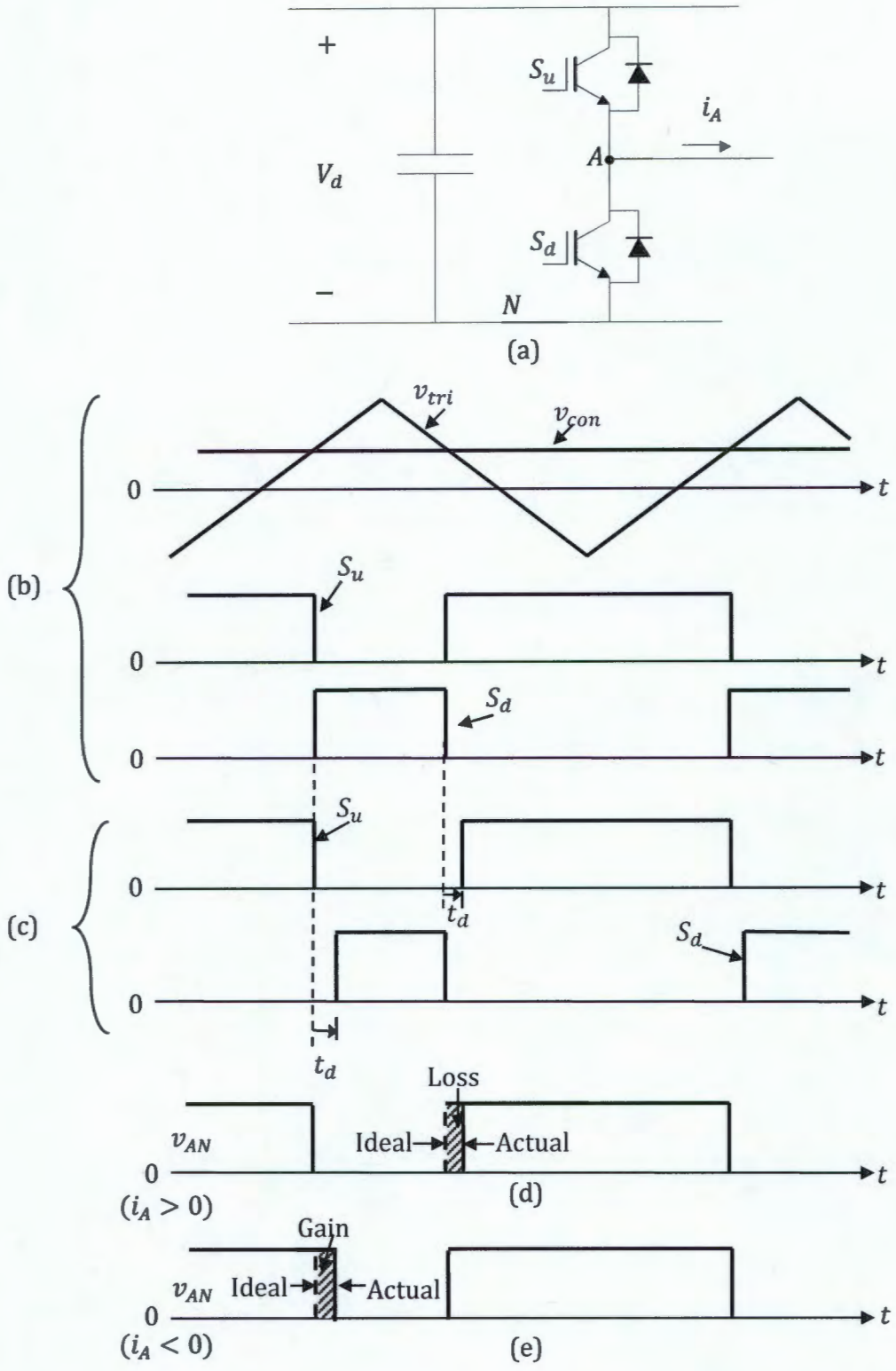


Figure 3.8: Effects of Deadtime [58].

3.3 Dynamic Modelling of the DC-AC converters/Inverter

The dynamic model of converters is mostly found using the state-space averaging technique. It requires all the switched networks to be identified in all switching cycles. Furthermore, the state-space averaging technique is simple to use if there are only few switched networks to sketch out if these networks are the same for all switching cycles. However, in PWM inverters the number of switched topologies is large and increases rapidly with the number of phases. Moreover, in a selected modulation strategy, the switched topologies in any one switching cycle can differ from those in any other cycle. Additionally, the whole pattern of switched topologies changes when another modulation strategy is used. Thus, in order to characterize low frequency behaviour of inverters the investigation of the switched topologies should be avoided. The derivation of the dynamic equations should be done by inspection of the inverter as a whole and by use of familiar electrical principles [61]. The averaging methods have been extended to modelling, analysis and control of inverters. The boost inverter's dynamic model was derived using these methods. Therefore, the averaging method used to find the dynamic model is covered in this subsection.

The averaging method for dynamic models is explained for phase a of the current source inverter (CSI) in Figure 3.9.

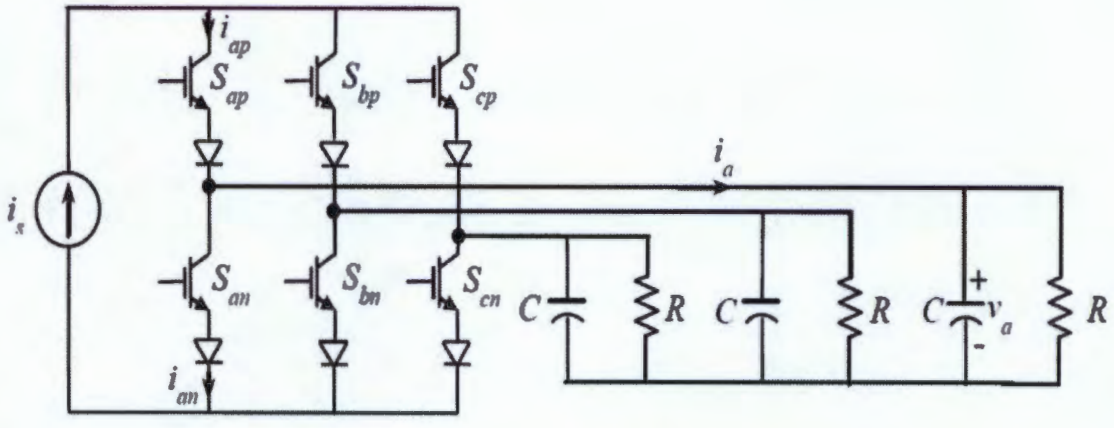


Figure 3.9: Current Source Inverter (CSI) [60].

The currents i_{ap}, i_{an}, and i_a can be written in terms of the source current, i_s, and the gate signals as follows:

$$i_{as} = s_{ap} i_s \tag{3.23}$$

$$i_{an} = s_{ap} i_s \tag{3.24}$$

Therefore

$$i_a = (s_{ap} - s_{an}) i_s \tag{3.25}$$

Where, s_{ap} and s_{an} are binary gate signals, which means they are either 1 or 0, to the switches S_{ap} and S_{an}, respectively. Therefore, the dynamic equation of phase a can be written as:

$$C\frac{dv_a}{dt} = (s_{ap} - s_{an}) i_s - \frac{v_a}{R} \tag{3.26}$$

The averaging method states that the dynamic equations can be approximated by replacement of the exact inputs and outputs by the low-frequency components of these terms, hence,

$$C\frac{d\bar{v}_a}{dt} = d_a \bar{i}_s - \frac{\bar{v}_a}{R} \tag{3.27}$$

Where, d_a is the duty ratio of phase a, which is defined as:

$$d_a = (\bar{s}_{ap} - \bar{s}_{an}) \tag{3.28}$$

Similarly, one can write the dynamic equations for the other phases and derive the averaged model of the CSI [60].

3.4 PR Controllers

PR controller is a controller that is suitable for single phase inverters. The PR controller has the form

$$K_{PR}(s) = K_p + \frac{K_R s}{s^2 + w_o^2} \tag{3.29}$$

where, K_P and K_R is the proportional and resonant gain. The controller provides infinite gain at the fundamental frequency of the reference voltage or current. In order to show this, the value of the controller at the fundamental frequency is ω_o is evaluated as follows:

$$K_{PR}(j\omega_o) = K_p + \frac{K_R(j\omega_o)}{(j\omega_0)^2 + \omega_o^2}$$

$$K_{PR}(j\omega_o) = K_p + \frac{K_R(j\omega_o)}{-\omega_0^2 + \omega_o^2} \tag{3.30}$$

$$K_{PR}(j\omega_o) = K_p + \infty$$

Therefore, the $K_{PR}(s)$ goes to infinity. The bode plot of the PR controller is shown in Figure 3.10.

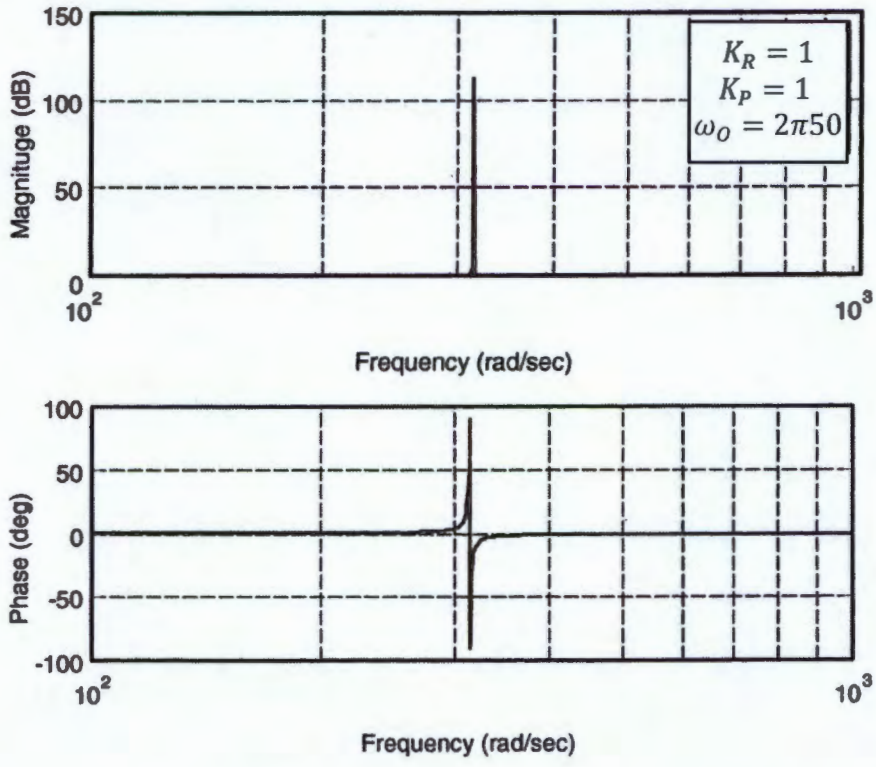


Figure 3.10: Bode plot of PR controller [48].

From Figure 3.10, the resonant term of the controller provides little gain outside the band-pass region due to the narrowband frequency response. The proportional term assists to achieve reasonable transient response. To tune the gains, a two-step design procedure for the PR controller can be used. Firstly, a proportional gain that achieves stable and good transient response must be selected. Lastly, the design of the resonant component that gives the desired steady-state phase and amplitude error without making the phase margin too small must be selected [48].

3.5 Total Harmonic Distortion

The amount of distortion at the output voltage is quantified by means of an index called total harmonic distortion (THD). The power quality standards from section 2 use the THD as a measure of performance for the grid. The method of determining the THD is shown in this subsection. The output voltage in steady state is the sum of its Fourier components as (assuming zero dc voltage) [58]:

$$v(t) = v_1(t) + \sum_{h\neq 1} v_h(t) \tag{3.31}$$

where $v_1(t)$ is the fundamental component and v_h(t) is the component at the h harmonic frequency. Furthermore, the harmonic components can be written as

$$v(t) = \sqrt{2}V_1 \sin(\omega_1 t) + \sum_{h\neq 1} \sqrt{2}V_h \sin(\omega_h t) \tag{3.32}$$

The rms value of $v(t)$ can be expressed as,

$$V_{rms} = \sqrt{\frac{1}{T_1}\int_0^{T_1} v^2(t)dt} \tag{3.33}$$

Substituting for v from equation and noting that the integrals of all the cross product terms are individually zero

$$V_{rms} = \sqrt{V_1^2 + \sum_{h\neq 1} V_h^2} \tag{3.34}$$

To determine the THD, the distortion component v_{dis} of the voltage from above is required and it can be expressed as:

$$v_{dis}(t) = v(t) - v_1(t) = \sum_{h\neq 1} v_h(t) \tag{3.35}$$

and in terms of the rms values it is written as,

$$V_{dis} = \sqrt{V_{rms}^2 - V_1^2} = \sum_{h \neq 1} V_h^2 \tag{3.36}$$

Therefore, the percentage of THD in the voltage is defined as [58]

$$\%THD = 100 \times \frac{V_{dis}}{V_1} \tag{3.37}$$

4. Single Phase Boost Inverter Analysis

This section presents the theoretical performance analysis of the boost inverter. The open loop and closed loop response is described. Furthermore, deadtime effects on the open loop and closed loop response will be covered.

4.1 Boost Inverter Principle of operation

The boost inverter is shown in Figure 4.1. It uses two identical boost dc-dc converters connected in parallel to the dc source and the outputs are connected across the load. The outputs of each converter and the combined outputs are described by:

$$V_1 = V_{dc} + \frac{1}{2}A_o \sin(2\pi ft) \tag{4.1}$$

$$V_2 = V_{dc} + \frac{1}{2}A_o \sin(2\pi ft - \pi) \tag{4.2}$$

$$\therefore V_{out} = V_1 - V_2 = A_0 \sin(2\pi ft) \tag{4.3}$$

$$V_{dc} > V_{in} + \frac{A_o}{2} \tag{4.4}$$

where V_{dc} is the dc bias of the of each converter and A_o is the peak amplitude of the voltage across the load that is required. The constraint (equation (4.4)), is required because each boost converter's output has to be greater than the input, otherwise the output saturates. The switching strategy used to achieve the required output is discussed in the next section.

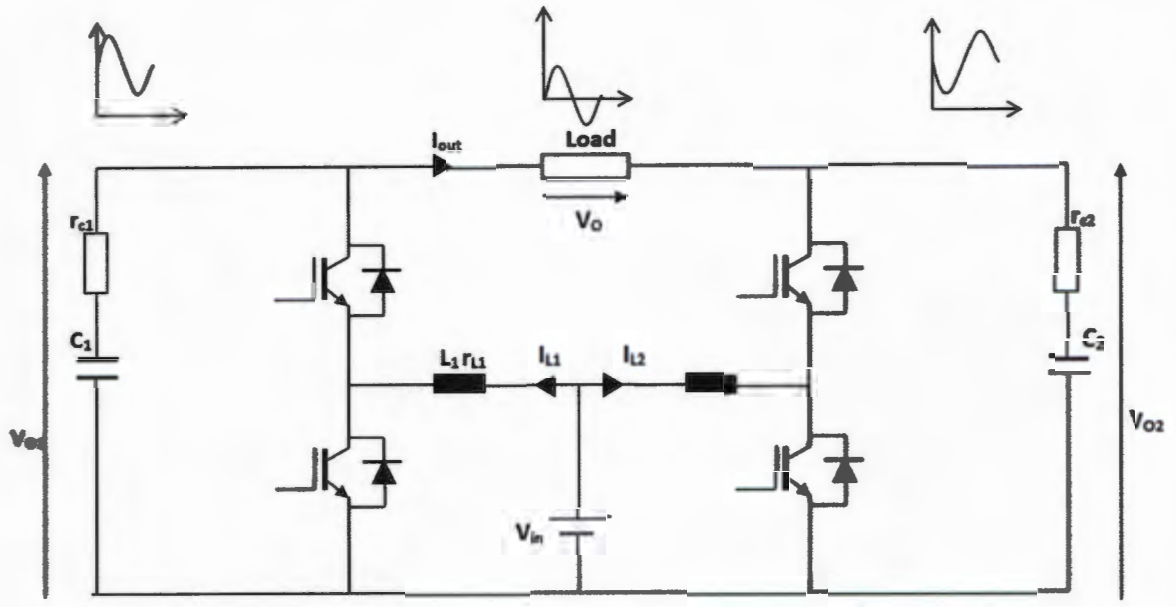


Figure 4.1: Boost inverter

4.2 Switching Strategy of a Boost Inverter

The boost inverter utilizes the PWM switching strategy. The switching strategy is similar to SPWM. The carrier waveforms are the same, except the modulating signal, v_{con}. This is due to the nonlinear gain of the output voltage. Thus, the modulating signal is derived in this section. The modulating signal will be derived by following a similar approach to the SPWM modulating signal derivation. Since two boost converters are used in the boost inverter, only one boost converter (Figure 4.2(a)) will be considered for simplicity. Moreover, the output capacitor is considered to be fairly large, which results in a fixed output voltage [58]. The ripple of the capacitor will be considered in the next section.

The modulating signal is initially considered to be constant and the principle of *inductor volt-second* will be used to determine the input-output average voltage relationship under continuous conduction mode. The steady state inductor voltage waveform is shown in Figure 4.2(b) and the total volt-seconds applied to the inductor over one switching period are:

$$\int_0^{T_S} v_L(t)dt = V_{in}DT_s + (V_{in} - V_{out})(1 - D)T_s \tag{4.5}$$

where D is the duty cycle, which represents the modulation signal. The left hand side of equation (4.5) is zero, based on the principle of *inductor volt-second,* which results in

$$V_{in}DT_s + (V_{in} - V_{out})(1 - D)T_s = 0 \tag{4.6}$$

Therefore, the output voltage can be written as:

$$V_{out} = \frac{V_{in}}{1 - D} \tag{4.7}$$

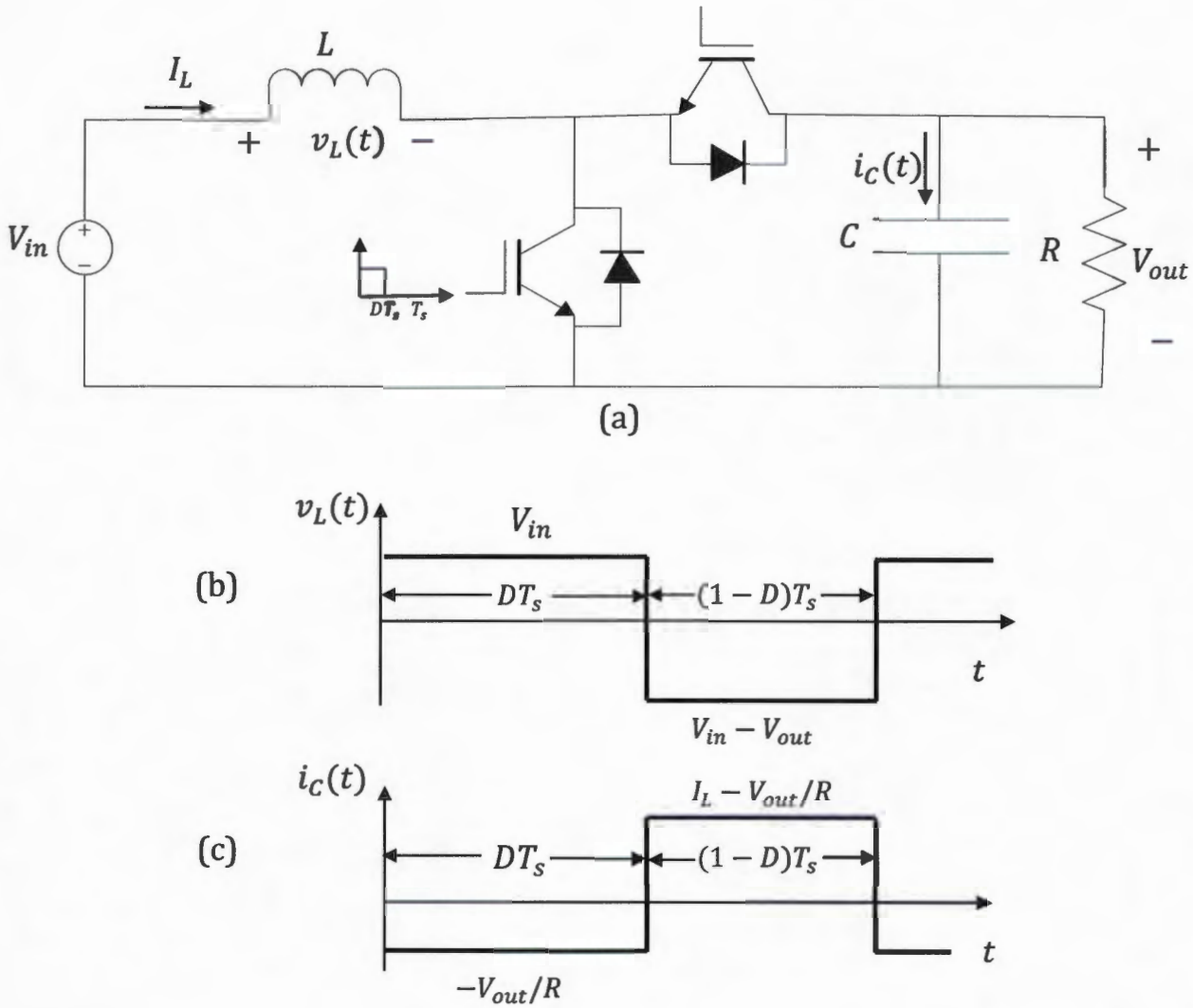


Figure 4.2: Boost converter under continuous conduction mode, (a) boost converter circuit topology, (b) inductor voltage waveform, (c) capacitor current waveform [59].

Equation (4.7) shows that the output voltage is nonlinear with respect to the duty cycle. Hence, SPWM cannot be used. Furthermore, the duty cycle cannot be equal to one because the output voltage would go to infinity, and components would get damaged. Furthermore, the duty cycle cannot be greater than one because the boost converter is used to provide an output voltage higher than the input voltage. Therefore, overmodulation is not used in this topology. The term $1/(1-D)$ is termed the gain of the boost converter and the gain can be controlled by varying the duty cycle. The gain is plotted in Figure 4.3 :

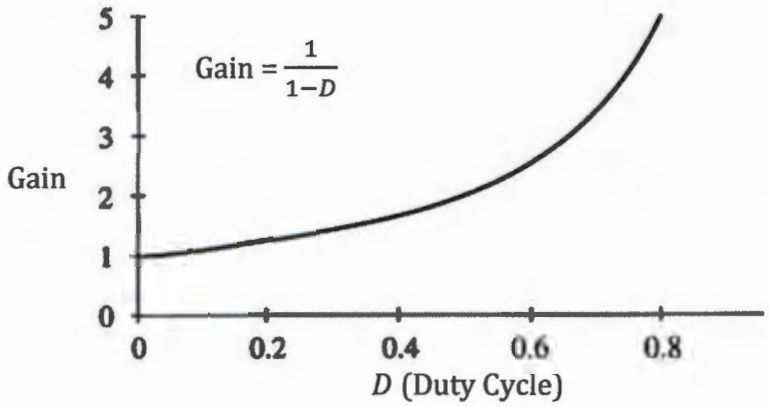


Figure 4.3: Output voltage gain control by varying the duty cycle (D) [59].

In a similar way to SPWM, the duty cycle can be assumed to vary very little during a switching period. Thus, equation (4.7) shows how the gain will vary in every switching period. Furthermore, the required duty cycle signal can be derived since the output voltage is known from equation (4.1) and assuming the input voltage is fixed and known. Therefore, substituting equation (4.1) into (4.7), results in:

$$(1-d(t)) = \frac{V_{in}}{V_{dc} + \frac{1}{2}A_o \sin(2\pi f t)} \tag{4.8}$$

Thus, the duty cycle signal is

$$d(t) = 1 - \frac{V_{in}}{V_{dc} + \frac{1}{2}A_o \sin(2\pi f t)} \tag{4.9}$$

The current input-output relationship is also derived using the the principle of *capacitor charge balance*. The ripple of the inductor is assumed to be very small, which requires a large inductor. The current ripple will be considered in the next chapter.

The integral of the net capacitor charge can be written as,

$$\int_0^{Ts} i_C(t)dt = \left(-\frac{V_{out}}{R}\right)DT_s + \left(I_L - \frac{V_{out}}{R}\right)(1-D)T_s \tag{4.10}$$

Furthermore, the left hand side is zero, thus

$$\left(-\frac{V_{out}}{R}\right)DT_s + \left(I_L - \frac{V_{out}}{R}\right)(1-D)T_s = 0 \tag{4.11}$$

and therefore,

$$I_L = \frac{V_{out}}{(1-D)R} \tag{4.12}$$

Moreover, V_{out}/R is the output current, hence

$$I_L = \frac{I_{out}}{1-D} \tag{4.13}$$

4.3 Switching Technique Modes of Boost Inverter

The boost inverter undergoes different switching technique modes throughout the period of the current and voltage waveforms. These switching technique modes of the boost inverter are identified and analysed under steady state in this subsection. The deadtime is included in the analysis and the passive components are considered lossless. In order to simplify the analysis, the switching technique modes are analysed using the equivalent circuit for the boost inverter shown in Figure 4.4, where only one boost converter is considered and the other one is represented by an ideal sinusoidal voltage source [62]. The capacitors C_d and C_u are the parasitic capacitance of the switching devices. The switching technique modes described from the one boost converter are the same as for the other modeled as the ideal sinusoidal voltage source.

The switching technique modes of the boost converter will be defined throughout the fundamental period of the current flowing through the inductor, by considering similar boost converters that have been used in literature for dc-dc conversion applications. Therefore, the switching technique modes are defined over a switching period at different instantaneous average inductor current magnitudes that cause the switching technique mode to change. The switching technique modes that are analysed in this subsection are the hard-switching and zero-voltage-resonant transition (ZVRT). These switching technique modes, for dc-dc conversion applications, were discussed in the literature review section 2.7.2.

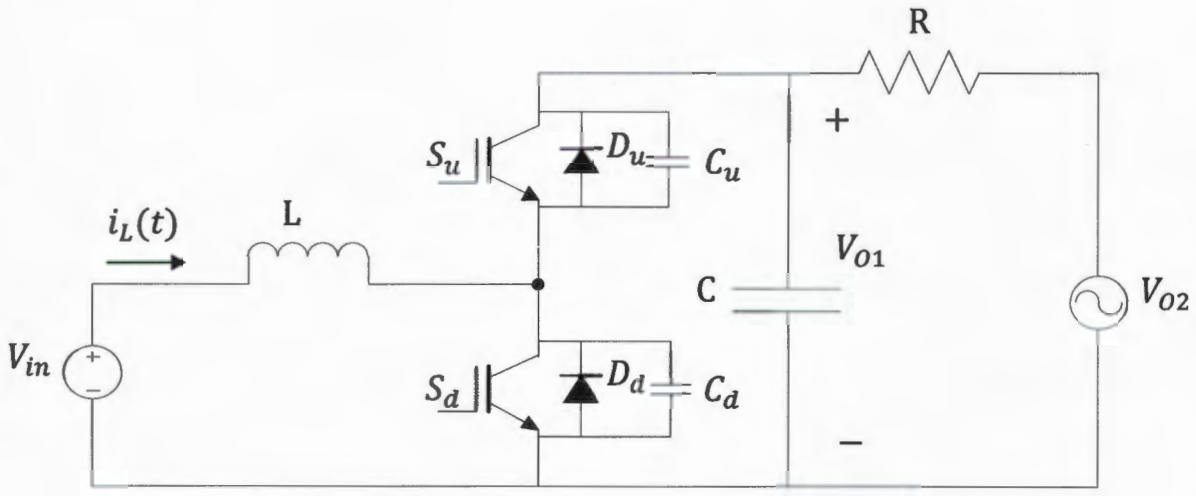


Figure 4.4: Equivalent circuit for boost inverter

4.3.1 *Hard-Switching Mode*

The boost converters of the boost inverter operate under continuous conduction mode, whereby the inductor current is conducted continuously through the inductor. The instantaneous average inductor current can be negative or positive depending on which voltage output ($V_{O1}(t)$ or $V_{O2}(t)$) is higher. The waveforms for the positive and negative instantaneous average inductor current are shown in Figure 4.5 (b) and Figure 4.5 (c), respectively. The description of the switching and conducting devices is given below for both positive and negative instantaneous inductor average current.

i. ***Positive Instantaneous Average Inductor Current***

Under this operational condition, the auxiliary switch S_u and the antiparallel diode D_d of the main switch do not conduct any current, as shown in Figure 4.5 (b). The boost converter of the boost inverter operates as a traditional boost converter.

Initially, when the main gate signal S_d is on, the inductor current rises from below the average current i_{Lmin} to a level above the average current i_{Lpeak}, while conducting through S_d. When

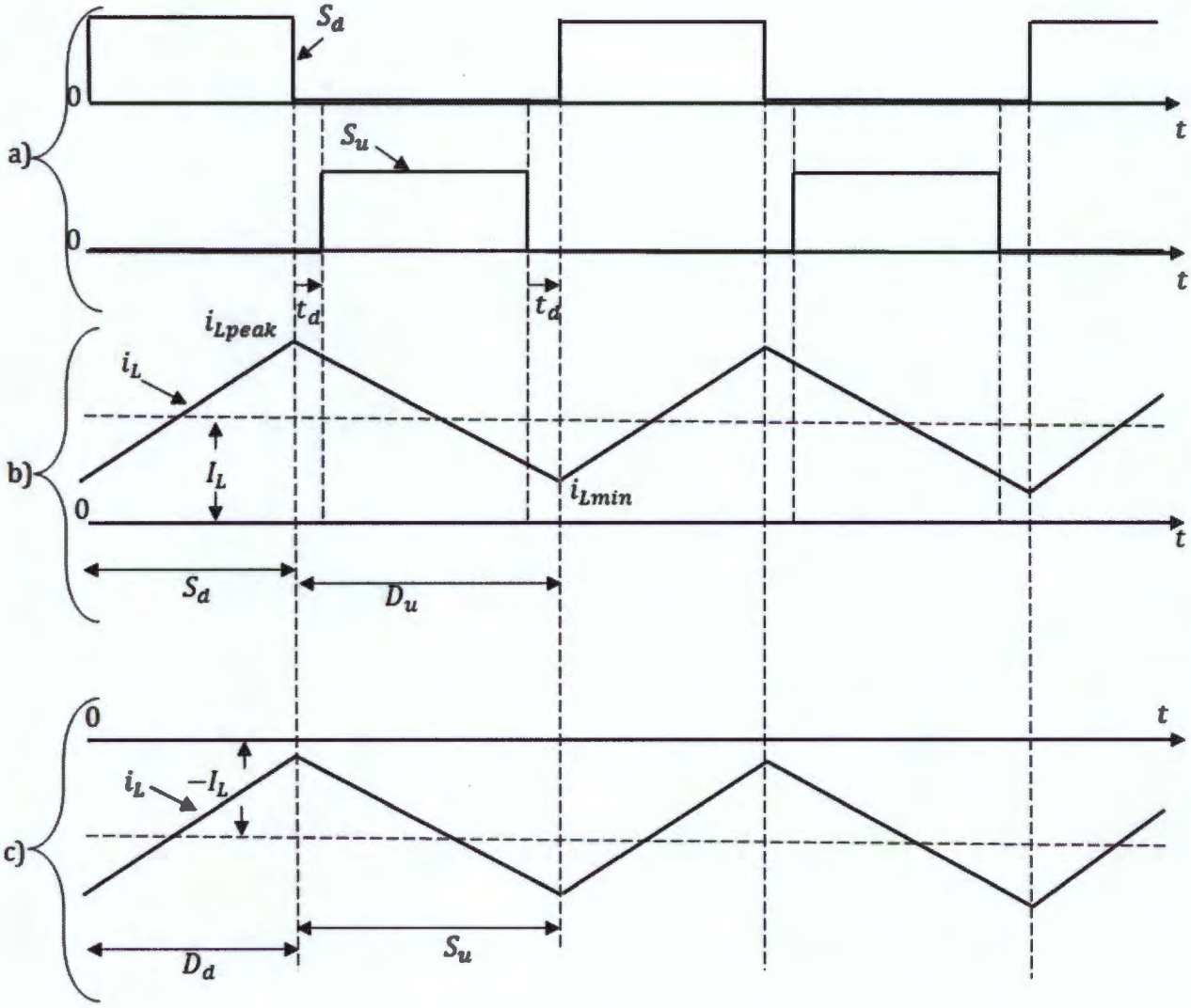


Figure 4.5: Continuous conduction mode of the boost converter waveforms of (a) switching signals and for (b) positive and (c) negative instantaneous average inductor current.

S_d turns off, there occurs a dead time period t_d, where all the switches are off [58]. Before the deadtime period ends, the inductor current commutates to the diode D_u. Therefore, S_d and D_u experience turn-off losses and turn-on losses, respectively. The auxiliary switch S_u turns on after the dead time with zero turn-on losses. The inductor current decrease until I_{Lmin}. At this

point, the auxiliary switch is turned off with zero turn-off losses, because D_u conducts the inductor currents during the deadtime period. After the dead time period, the main switch S_d turns on. Thus, the main switch experiences turn-on losses and there is a reverse recovery loss of the diode.

ii. ***Negative Instantaneous Average Inductor Current***

Under this operational condition, the main switch S_d and the antiparallel diode D_u of the auxiliary switch do conduct any current, as shown in Figure 4.5 (c). The boost converter of the boost inverter sinks current from the ideal voltage source.

Initially, when the main gate signal S_d is on, the inductor current rises from below the average current $-I_{Lmin}$ to a level above the average inductor current$-I_{Lmax}$, while conducting through D_d. When S_d turns off, there occurs a dead time period t_d, where all the switches are off. The switch S_d is turned off with zero turn-off losses, because D_d conducts for the deadtime period. After the deadtime period, S_u is turned on and experiences turn-on losses when there are reverse recovery losses of the diode. Then the inductor current decrease until I_{Lmin}. At this point, S_u is switched off. Before the deadtime period ends, the inductor current commutates to the diode D_d. Therefore, S_u and D_d experience turn-off losses and turn-on losses, respectively.

4.3.2 ZVRT Mode

The ZVRT operational mode is when the switching devices of the boost converter are switched on under zero voltage switching. Furthermore, inductor current is conducted continuously through the inductor. The instantaneous average inductor current can be negative or positive depending on which voltage output ($V_{O1}(t)$ or $V_{O2}(t)$) is high. The waveforms for the positive and negative instantaneous average inductor current are shown in Figure 4.6(b) and Figure 4.6 (c), respectively. The description of the switching and conducting devices is given below for both positive and negative instantaneous inductor average current.

i. ***Positive Instantaneous Average Inductor Current***

Initially, when the main gate signal S_d is on, the inductor current rises from below zero to a level equal to at least twice the dc current. When S_d turns off, there occurs a dead time period t_d, where all the switches turned off. During this period, the inductor current i_L will charge C_d and discharge C_u. The device voltage charge and discharge rates are slowed down by these capacitors if external capacitors are added, which would decrease the turn-off loss. After the

charging and discharging phase, V_{CEu} becomes zero and diode D_u begins to conduct the inductor current. The auxiliary switch S_u turns on after the dead time under zero-voltage condition, because diode D_u carries the freewheeling current. The output voltage V_o is against the inductor, and the inductor current continuously decreases

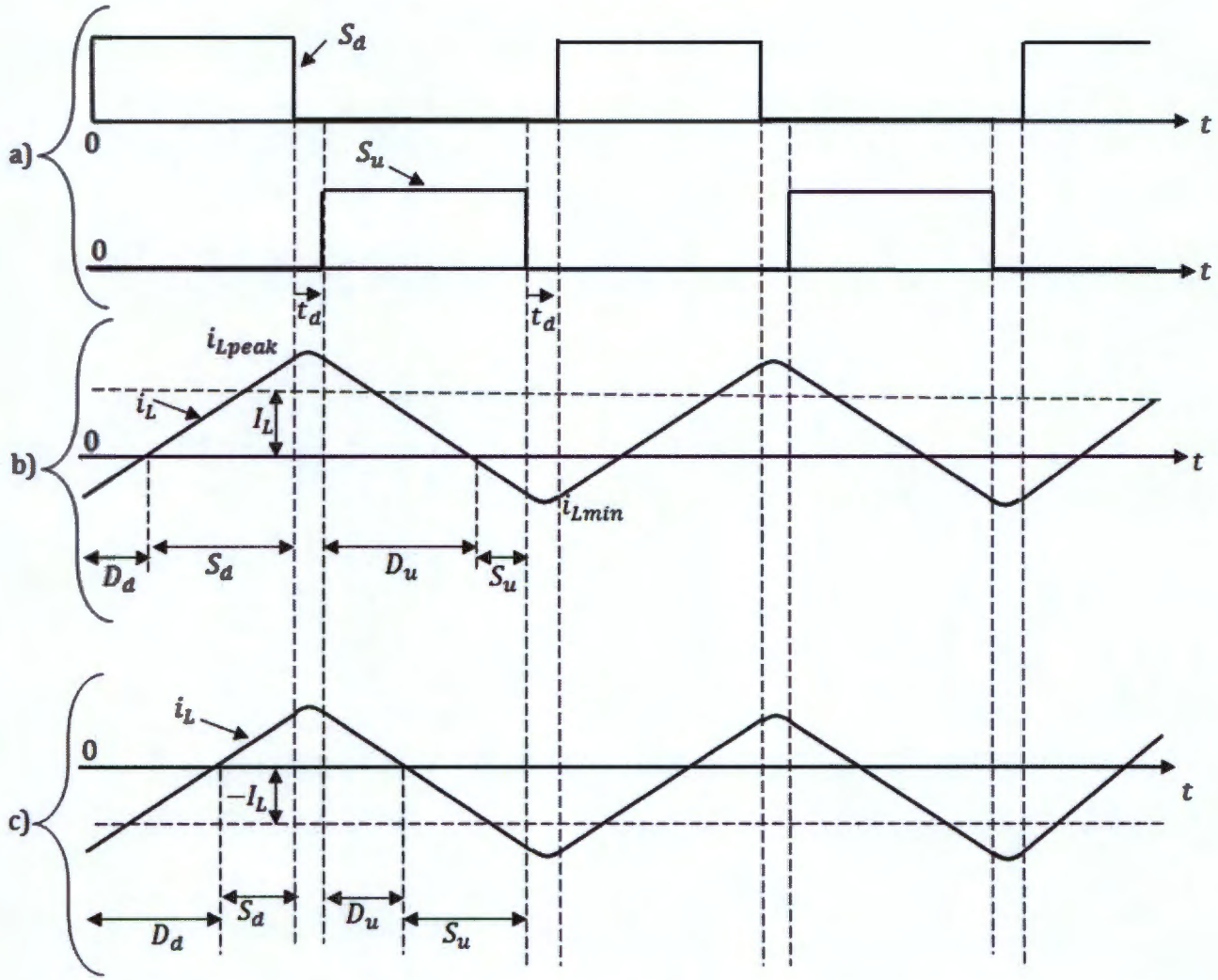


Figure 4.6: ZVRT mode of the boost converter waveforms of (a) switching signals and for (b) positive and (c) negative instantaneous average inductor current.

until it passes through zero and changes its direction. The inductor current will go through S_u once it has changed direction. Furthermore, the diode turns off naturally without having reverse recovery loss.

When S_u is turned off, the negative current flowing through S_u discharges C_d and charges C_u. The charging and discharging occurs during the dead time period. After the charging and discharging, the main switch V_{CEd} becomes zero and diode D_d will conduct the inductor negative current. Then, the main switch S_d turns on at zero-voltage condition. Thus both upper and lower switches are all turned on at zero voltage condition [51], [52]. To obtain

zero-voltage switching for S_d , the inductor current at i_{Lmin}, must be sufficiently negative. The following condition has to be met [52]

$$\frac{1}{2}Li_{Lmin}^2 > \frac{1}{2}C_dV_C^2 \tag{4.14}$$

ii. ***Negative Instantaneous Average Inductor Current***

When the instantaneous average current inductor current is negative there are only two differences from positive. The first difference is that, initially, when the main gate signal S_d is on, the inductor current rises from at least twice the instantaneous average current to a level below zero. Secondly, to obtain zero-voltage switching for S_u , the inductor current at i_{Lpeak}, must be sufficiently positive, therefore the following condition has to be met

$$\frac{1}{2}Li_{Lpeak}^2 > \frac{1}{2}C_dV_C^2 \tag{4.15}$$

As it can be seen from Figure 4.6(b) the devices conduct in the same sequence as in Figure 4.6(c).

4.4 Deadtime Effects on Output Voltage

The effect of deadtime on the input-output instantaneous average voltage of the boost inverter is considered in this subsection. Two different switching technique modes were determined in section 4.3 and, therefore, the input-output instantaneous average voltage in each switching technique mode will be derived. The equivalent boost inverter shown in Figure 4.4 is used.

4.4.1 Hard-Switching Mode Input-Output Instantaneous Average Voltage

The principle of *inductor volt-second* is used to determine the input-output instantaneous average voltage relationship. The ideal and deadtime switching signals are shown in Figure 4.7 (a) and Figure 4.7 (b) with deadtime. The inductor voltage waveform for positive and negative instantaneous average current is shown in Figure 4.7 (c) Figure 4.7 (d), respectively.

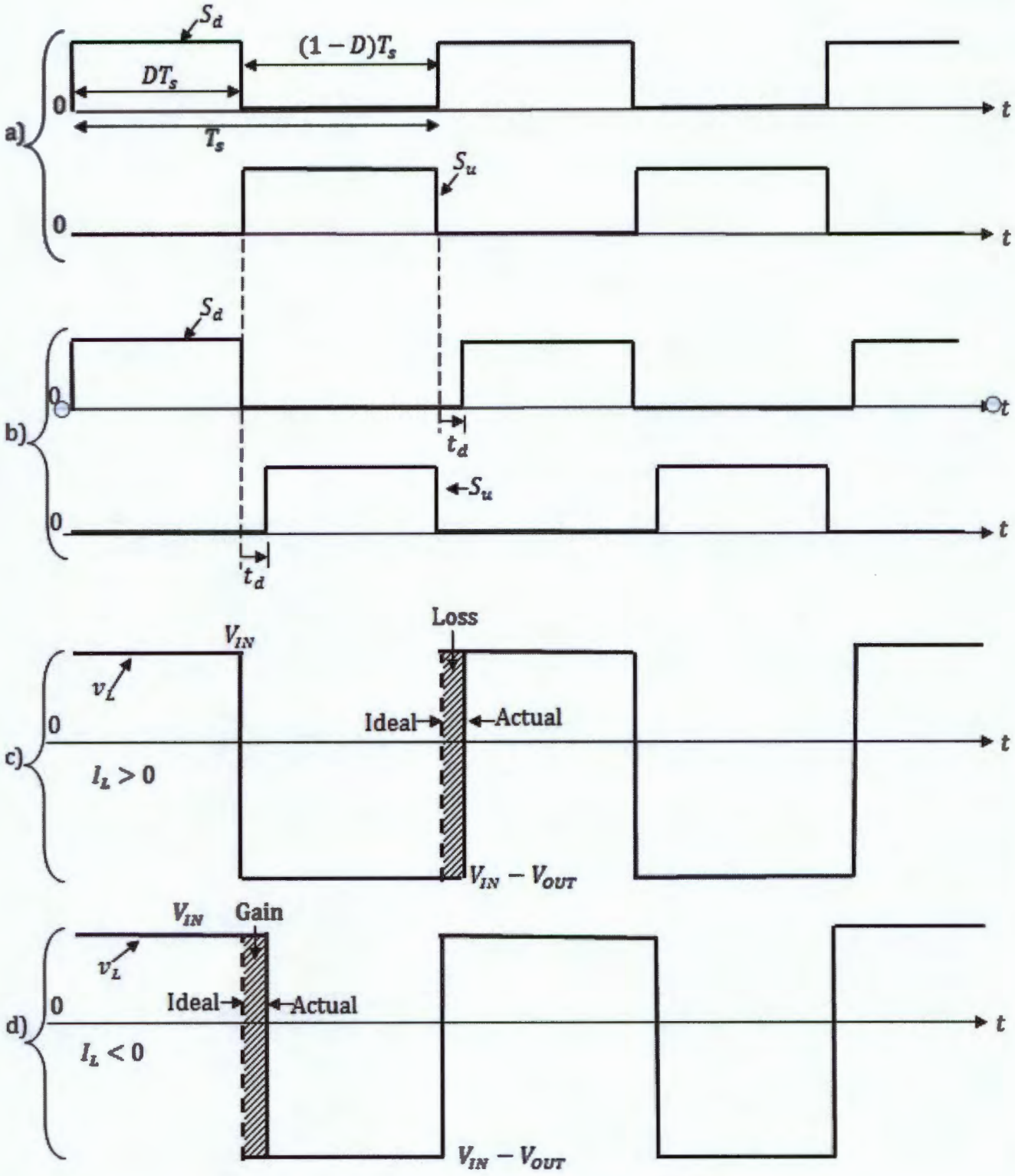


Figure 4.7: Continuous conduction mode deadtime effects

The derivation of the input-output instantaneous average voltage relationship for the positive and negative instantaneous inductor average currents is shown in this subsection. Furthermore, the following term is defined (duty cycle of deadtime) which will be used to determine input-output instantaneous average voltage,

$$D_{td} = \frac{t_d}{T_S} = t_d f_s \tag{4.16}$$

i. ***Positive Instantaneous Average Inductor Current***

The inductor volt-seconds of the waveform in Figure 4.7(c) are

$$\int_0^{T_S} v_L(t)dt = V_{in}(D - D_{td})T_s + (V_{in} - V_{out})(1 - D + D_{td})T_s \tag{4.17}$$

from the principle of inductor volt-second, the left hand integral is zero, therefore

$$V_{in}(D - D_{td})T_s + (V_{in} - V_{out})((1 - D) + D_{td})T_s = 0 \tag{4.18}$$

Solving for the instantaneous average output voltage, results in

$$\begin{gathered} V_{in}(D - D_{td})T_s + (V_{in} - V_{out})((1 - D) + D_{td})T_s = 0 \\ V_{out}((1 - D) + D_{td})T_s = V_{in}T_s \\ V_{out} = \frac{V_{in}}{(1 - D) + D_{td}} \end{gathered} \tag{4.19}$$

This result is similar to the result found in reference [63]. In Reference [63],other delay terms from the physical switches were added. If these are neglected, equation (4.19) is the same as in reference [63].Equation (4.19) can also be rearranged to be

$$V_{out} = \frac{V_{in}}{1 - (D - D_{td})} \tag{4.20}$$

Therefore, there is a loss of instantaneous average output voltage because the duty cycle is decreased by the duty cycle of the deadtime.

ii. ***Negative Instantaneous Average Inductor Current***

The inductor volt-seconds of the waveform in Figure 4.7 (d) are

$$\int_0^{T_S} v_L(t)dt = V_{in}(D + D_{td})T_s + (V_{in} - V_{out})(1 - D - D_{td})T_s \tag{4.21}$$

from the principle of inductor volt-second, the left hand integral is zero, therefore

$$V_{in}(D + D_{td})T_s + (V_{in} - V_{out})(1 - D - D_{td})T_s = 0 \tag{4.22}$$

Solving for the instantaneous average output voltage, results in

$$\begin{aligned} V_{in}(D + D_{td})T_s + (V_{in} - V_{out})(1 - D - D_{td})T_s &= 0 \\ V_{out}(1 - D + D_{td})T_s &= V_{in}T_s \\ V_{out} &= \frac{V_{in}}{1 - D - D_{td}} \end{aligned} \tag{4.23}$$

Equation (4.23) can also be rearranged to be

$$V_{out} = \frac{V_{in}}{1 - (D + D_{td})} \tag{4.24}$$

Therefore, there is a gain of the instantaneous average output voltage because the duty cycle is increased by the duty cycle of the deadtime.

The results can be summarized as follows:

$$V_{out} = \begin{cases} \dfrac{V_{in}}{1 - (D - D_{td})} & I_L > 0 \\ \dfrac{V_{in}}{1 - (D + D_{td})} & I_L < 0 \end{cases} \tag{4.25}$$

4.4.2 *ZVRT Mode Input-Output Instantaneous Average Voltage*

The ideal and deadtime switching signals are shown in Figure 4.8 (a) and Figure 4.8 (b), respectively. The inductor voltages for positive and negative instantaneous average current is shown in Figure 4.8 (c) and Figure 4.8 (d), respectively.

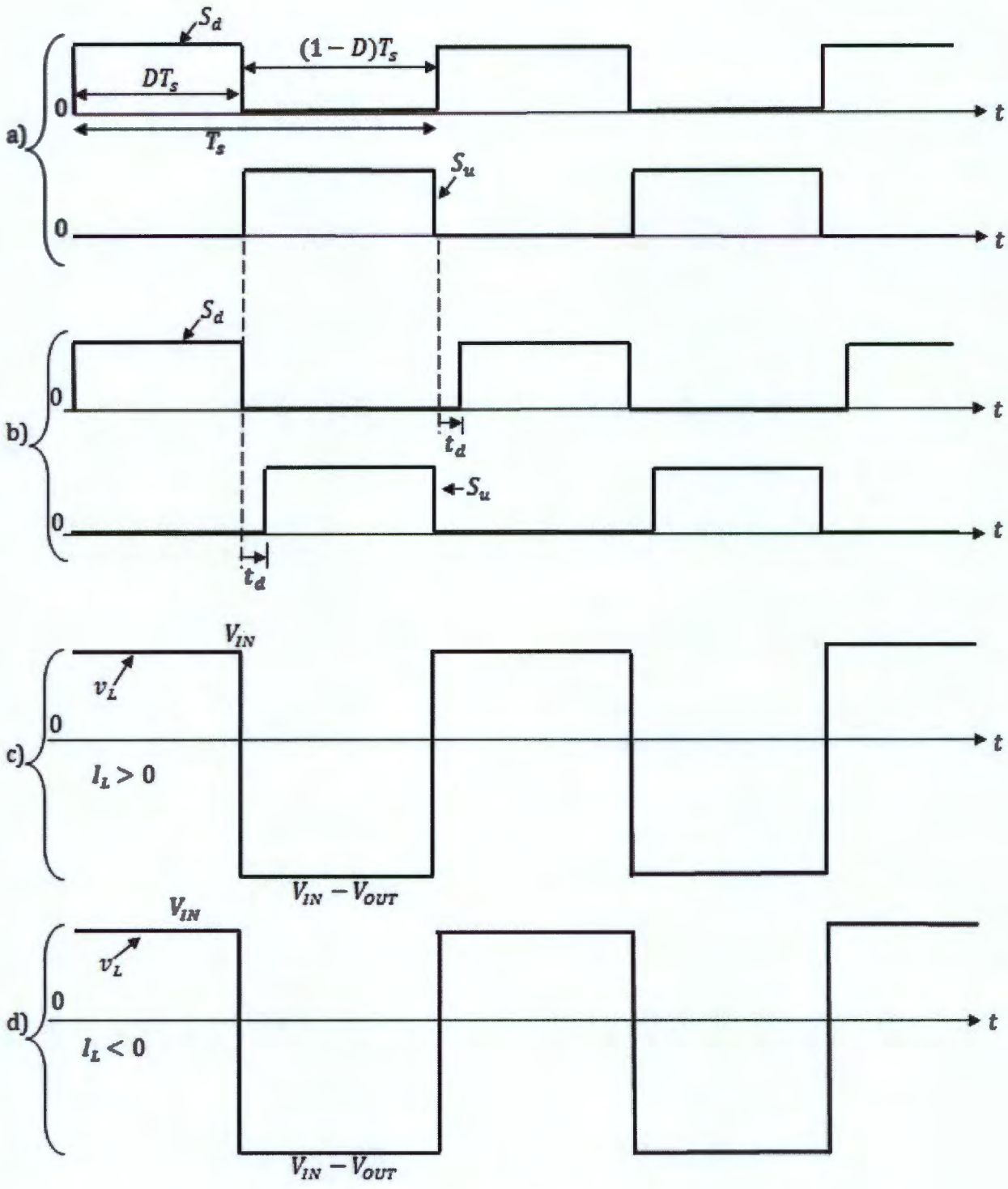


Figure 4.8: ZVRT mode deadtime effects

From Figure 4.8, the instantaneous average inductor voltage matches the ideal waveform for the traditional boost converter because the antiparallel diodes of the IGBT conduct during the deadtime period. The inductor current is always commutated to antiparallel diodes of the IGBT that is about to switched on. Thus, the deadtime does not affect the gain of the switch

during the deadtime period and the input-output instantaneous average voltage for this conduction can be written as:

$$V_{out} = \begin{cases} \dfrac{V_{in}}{1-D} & I_L > 0 \\ \dfrac{V_{in}}{1-D} & I_L < 0 \end{cases} \tag{4.26}$$

4.4.3 *Transition between ZVRT and Hard-Switching Operation*

During simulation runs and experimental testing, it was found that the transition between ZVRT and hard-switching operation does not happen instantly. In order to explain the phenomena that take place, a simple boost converter without parasitic capacitance on the switching devices is considered. On the edge of transition between hard-switching and ZVRT mode, the waveforms are shown in Figure 4.9 and Figure 4.10, respectively.

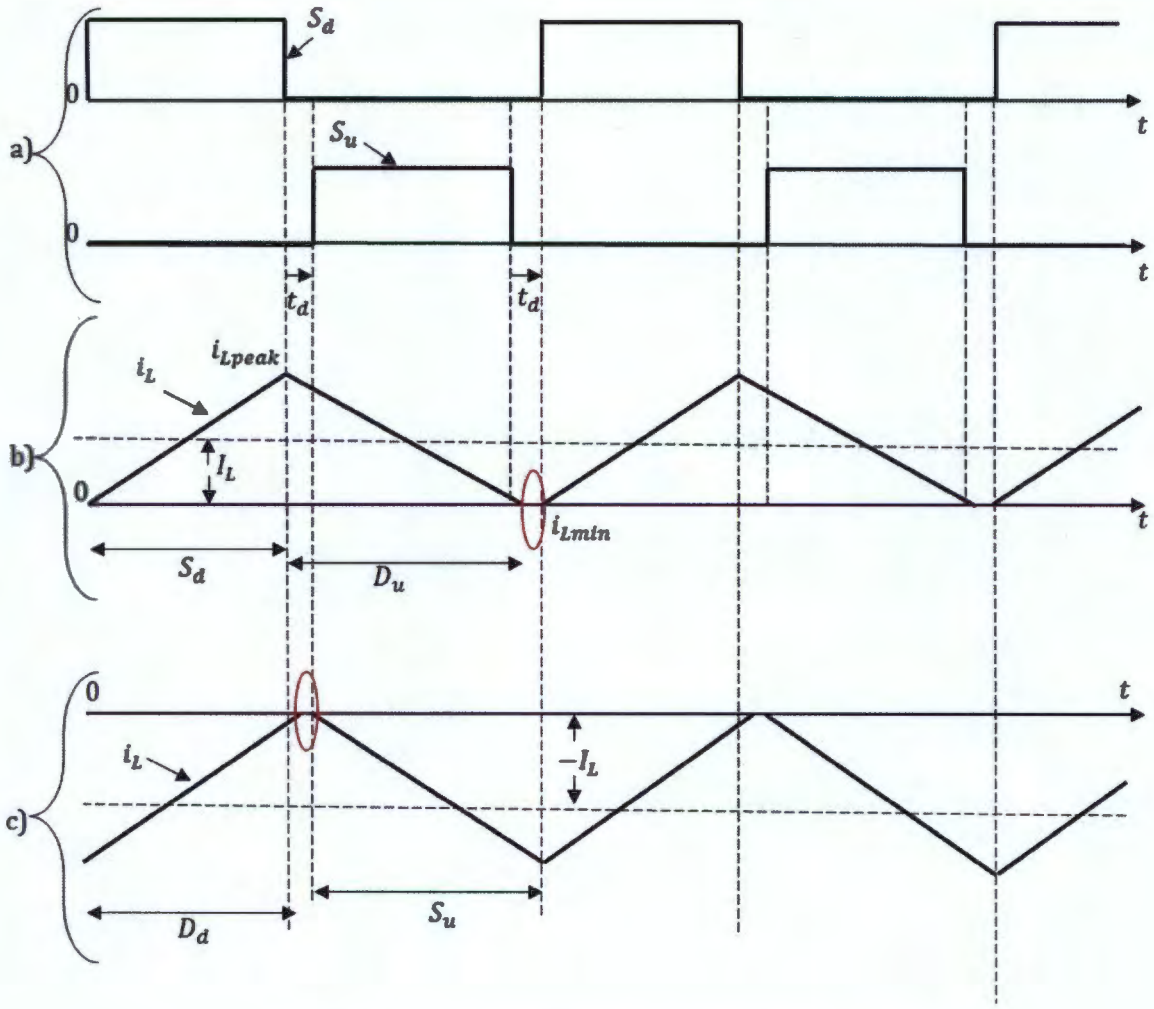


Figure 4.9: Hard-Switching mode edge of transitions waveforms.

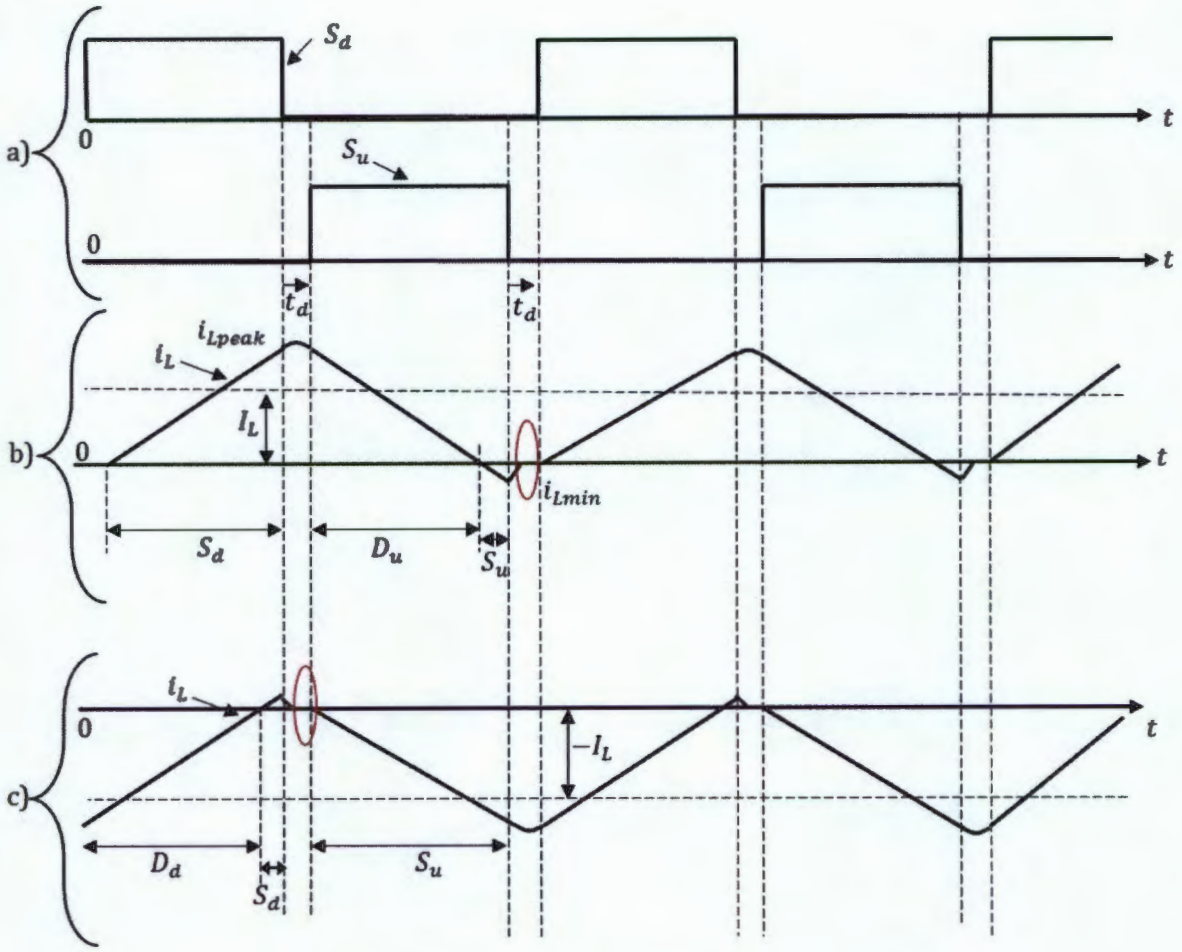


Figure 4.10: ZVRT mode edge of transitions waveforms.

From the figures above, the boost converter operates under a discontinuous mode for a portion of the deadtime period. However, when the parasitic capacitance on the switching devices is added, the parasitic capacitance would discharge or charge. The charging and discharging of the parasitic capacitance will cause the inductor voltage to rise or fall during the deadtime period, as show in Figure 4.11.

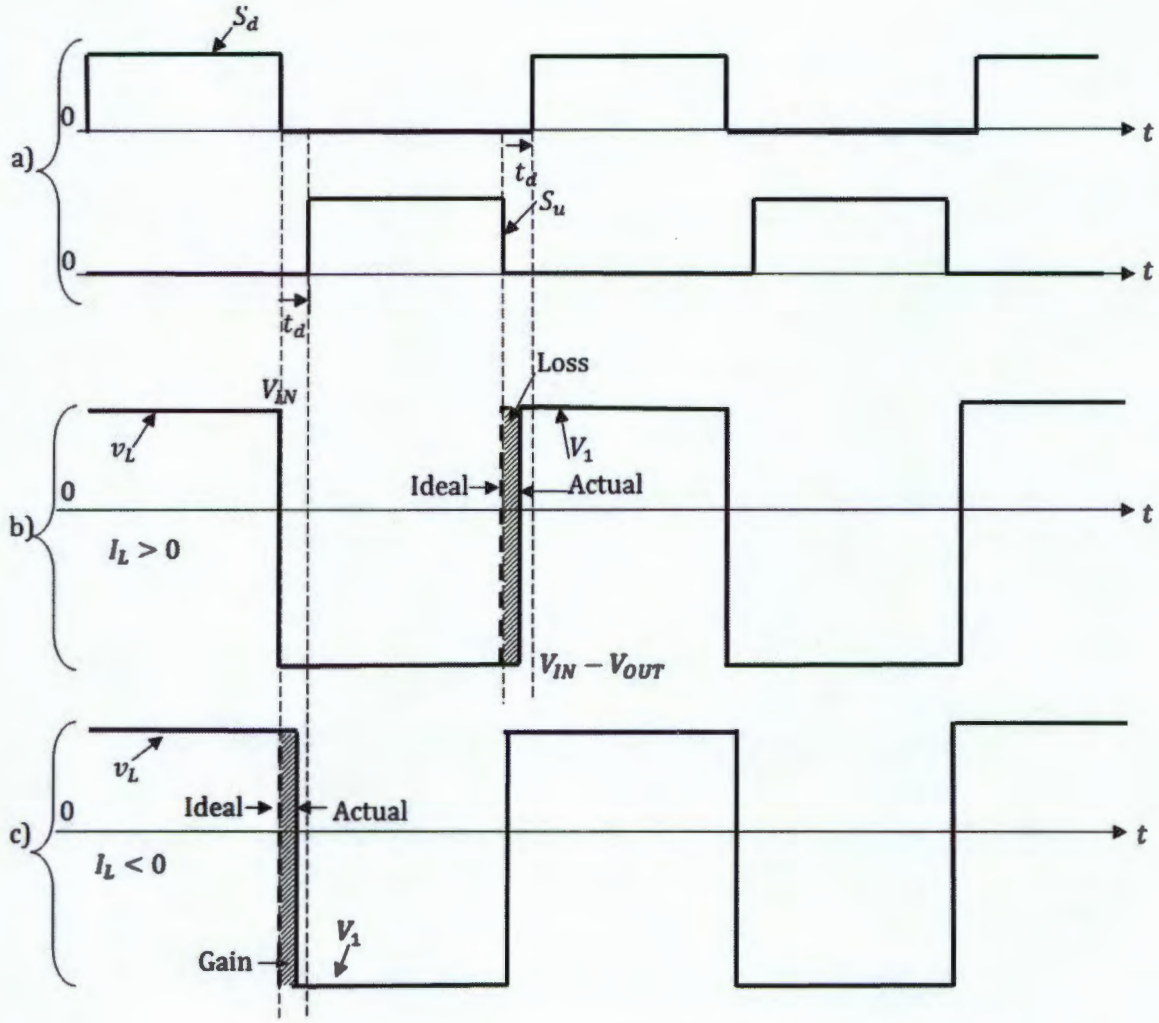


Figure 4.11: Inductor voltage for ZVRT and hard-switching mode transition edges.

From Figure 4.11, the parasitic capacitance on the switching devices will cause the inductor voltage to rise or fall, depending on the average instantaneous current during the deadtime period. This means that, the input-output voltage relationship will change. The change will not be caused by the full deadtime period, but a portion of the deadtime period depending where the voltage rises or falls. Therefore the relationship would be

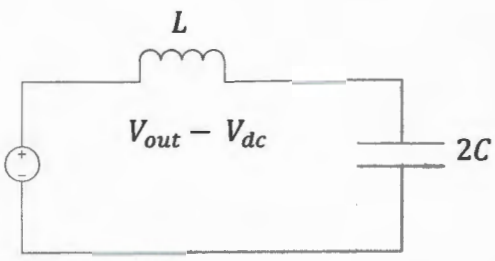
$$V_{out} = \begin{cases} \dfrac{V_{in}}{1-(D-\alpha D_{td})} & I_L > 0 \\ \dfrac{V_{in}}{1-(D+\alpha D_{td})} & I_L < 0 \end{cases} \tag{4.27}$$

Where

$$0 \leq \alpha < 1 \tag{4.28}$$

The variable α, depends on the instantaneous average inductor current magnitude, inductance and parasitic capacitance of the switching device. This shows that the transition between hard-switching and ZVRT mode is not instantaneous; instead it is a smooth transition.

During simulations and experimental testing, it was also noticed that during these intervals, resonance may occur. This resonance has been reported in literature for a boost converter operating in discontinuous mode [56]. During the deadtime period the following circuit is formed and resonance may take place.



The ringing frequency and the amplitude of the oscillation current are functions of the inductance and the parasitic capacitance of the switching device, which is expressed as

$$f = \frac{1}{2\pi\sqrt{2LC_{para}}} = \tag{4.29}$$

$$I = \frac{V_{out} - V_{in}}{\sqrt{\frac{L}{C_{para}}}} \tag{4.30}$$

This current will distort the inductor voltage. Therefore, the output voltage will be affected. Furthermore, the high frequency current will cause copper losses and the efficiency drops.

4.5 Conduction Losses Effects on Output Voltage

Conduction losses of the boost converter are caused by the voltage drop of the IGBT, diodes and series inductor resistance. The series inductor resistance is usually the dominant loss and the expression of the boost converter changes as follows [64].

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \times \frac{1}{1+\frac{r_{L1}}{(1-D)^2 \cdot R_L}} \tag{4.31}$$

Therefore, the boost inverter output voltage will also be affected by the conduction losses.

4.6 Modelling the Boost Inverter

The boost converter is usually modelled using the small signal linear model around a particular operation point. However, this modelling strategy is not appropriate for modelling the boost inverter, as discussed in section 2.7.1. The double-loop control scheme, which will be used for the boost inverter is based on modelling using the averaging concept, as discussed in section 3.3. Thus, the model of the boost inverter is derived in this subsection and the double loop control scheme is described. Furthermore, the performance of the PR controller's ability to eliminate dc offsets will be analysed.

4.6.1 Boost Inverter Dynamic Modelling

The dynamic modelling of the boost inverter is derived for one of the boost converters as shown in Figure 4.12. The series resistance of the inductor (r_{L1}) and capacitor (r_{C1}) are considered in the models.

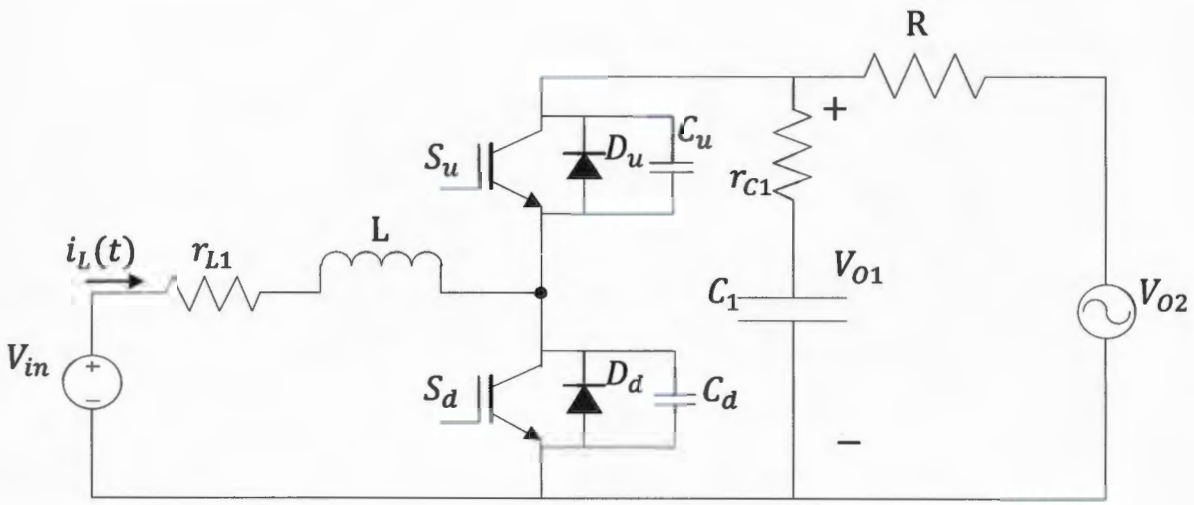


Figure 4.12: Boost inverter Equivalent Model for dynamic modelling.

The low-frequency components of the inductor voltage and capacitor current are [46]:

$$V_{L1}(t) = V_{in}(t) - \big(1 - D_1(t)\big) \cdot V_{O1}(t) \tag{4.32}$$

$$I_{C1} = (1 - D_1(t)) \cdot I_{L1}(t) - I_{out} \tag{4.33}$$

The dynamic equations of the inductor current and capacitor voltage differential equations are, respectively [46]:

$$V_{L1} = r_{L1} I_{L1}(t) + L_1 \frac{dI_{L1}(t)}{dt} \tag{4.34}$$

$$I_{C1} + r_{C1} C_1 \frac{dI_{C1}(t)}{dt} = C_1 \frac{dV_{O1}(t)}{dt} \tag{4.35}$$

Firstly, the inductor current open loop system and closed loop strategy is described. The inductor current open loop system can be found by substituting equation (4.32) into equation (4.36):

$$V_{in}(t) - \big(1 - D_1(t)\big) \cdot V_{o1}(t) = r_{L1} I_{L1}(t) + L_1 \frac{dI_{L1}(t)}{dt} \tag{4.36}$$

The Laplace transformation of equation (4.36) can be written as:

$$V_{in}(s) - \big(1 - D_1(s)\big) \cdot V_{o1}(s) = r_{L1} I_{L1}(s) + s L_1 I_{L1}(s) \tag{4.37}$$

Since the inductor current is the output that is has to be controlled, equation (4.37) can be rearranged as:

$$I_{L1}(s) = \frac{V_{in}(s) - \big(1 - D_1(s)\big) \cdot V_{o1}(s)}{r_{L1} + sL_1} \tag{4.38}$$

Therefore, the inductor current open loop system can be represented in a block diagram as shown in Figure 4.13 in the shaded block. In variable operation conditions, these equations are nonlinear because the inductor current depends on the output voltage $V_{O1}(t)$ which

causes the open loop system to have a variable gain. Therefore, the duty cycle cannot be used as the controller output for this system. Furthermore, the input voltage ($V_{in}(t)$, appears as an external disturbance [46].

To eliminate the nonlinear characteristics, the closed loop system uses the inductor voltage $V_{L1}(t)$ as the control variable. Thus, the plant seen by the converter becomes the equation (4.36). The duty cycle is then obtained by means of the following in which $V_{L1ref}(t)$ is the controller output [46]

$$1 - D_1(t) = \frac{V_{in}(t) - V_{L1ref}(t)}{V_{O1}(t)} \tag{4.39}$$

The inductor current closed loop system is shown in Figure 4.13. From a different point of view, this control strategy compensates the variable gain of the open loop system by means of a gain that is the inverse value of this output voltage. Additionally, it cancels the influence of the input voltage by adding to the control loop this disturbance with its opposite value. The compensation of the output voltage can be done due to the much higher current loop bandwidth in comparison with the output voltage bandwidth. The cancellation of the input voltage influence acts as feed-forward control. This cancellation would not be required if the current loop bandwidth is much faster than the input voltage dynamics. The variables are filtered and the duty cycle is limited in order to avoid short-circuiting. A freezing action can be activated if there is an integral term used in the controller [46].

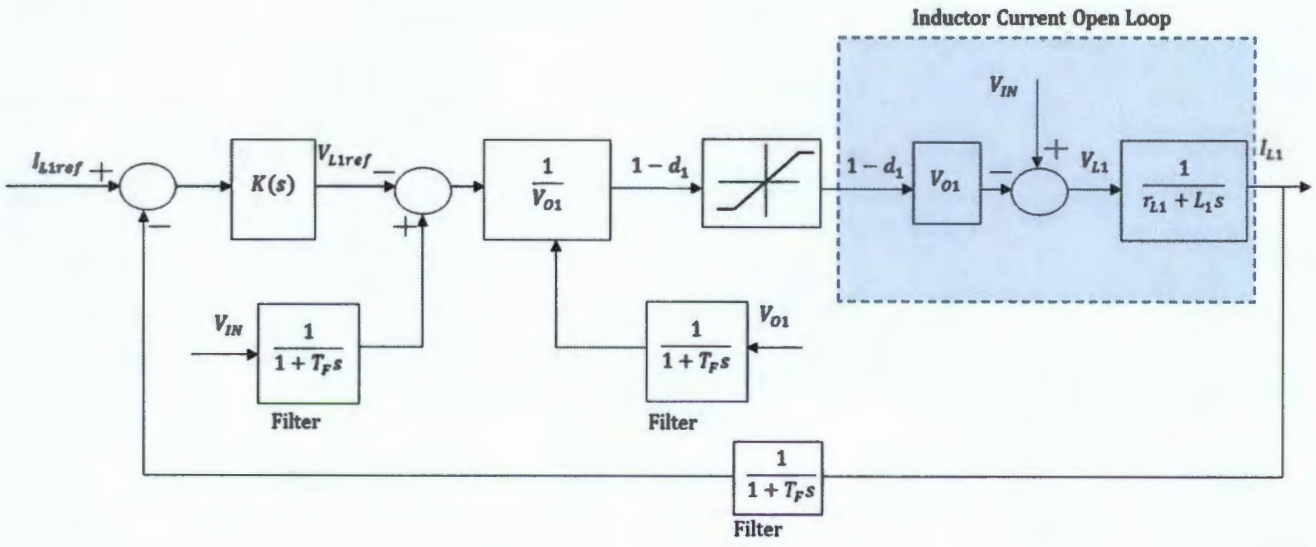


Figure 4.13: Inductor current closed loop system [46].

Lastly, the capacitor voltage open loop system and closed loop strategy is described. The capacitor voltage open loop system can be found by substituting equation (4.33) into equation (4.35):

$$\begin{aligned}\left(1 - D_1(t)\right) \cdot I_{L1}(t) - I_{out}(t) + r_{C1}C_1 \frac{d\left(\left(1 - D_1(t)\right) \cdot I_{L1}(t) - I_{out}(t)\right)}{dt} \\ = C_1 \frac{dV_{O1}(t)}{dt}\end{aligned} \tag{4.40}$$

The Laplace transformation of equation (4.40) can be written as:

$$\begin{aligned}\left(1 - D_1(s)\right) \cdot I_{L1}(s) - I_{out}(s) + r_{C1}C_1 s\left(\left(1 - D_1(s)\right) \cdot I_{L1}(s) - I_{out}(s)\right) \\ = C_1 s V_{O1}(s)\end{aligned} \tag{4.41}$$

Since the capacitor voltage is the output that has to be controlled, equation (4.41) can be rearranged as:

$$V_{O1}(s) = \frac{\left(\left(1 - D_1(s)\right) \cdot I_{L1}(s) - I_{out}(s) + r_{C1}C_1 s\left(\left(1 - D_1(s)\right) \cdot I_{L1}(s) - I_{out}(s)\right)\right)}{C_1 s} \tag{4.42}$$

Therefore, the capacitor voltage open loop system can be represented in a block diagram as shown in Figure 4.14 in the shaded block. The open loop system is nonlinear because the variable duty cycle term $\left(1 - D_1(t)\right)$ creates an open loop system with variable gain. Moreover, the output current acts as disturbance in the system.

To eliminate the nonlinear characteristics, the closed loop system (Figure 4.14) of the capacitor voltage uses the capacitor current as the control variable, which is based on the same philosophy of the inductor current closed loop. Thus, the plant seen by the control variable is the Laplace transformation of equation (4.35). The calculation of the inductor current reference from the capacitor current requires the use of the duty cycle, which appears inside the term $(1 - D_1(t)$ as in (4.33). However, the duty cycle dynamics is provided by the inner current loop, and its use in the inductor current reference calculation causes a coupling between both the inner and outer control loops and could make the system unstable. A strongly filtered value of the term $1/(1 - D_1(t))$ can give good results. However, this term can be approximated by $V_{o1}(t)/V_{in}$ if the inductor energy variations are neglected. This

approximation is valid due to the relatively small size of the inductance in power boost converters and it achieves more accurate and fast results. Furthermore, this compensation strategy can compensate duty cycle variations up to the voltage loop bandwidth. Therefore, the system will accurately track different voltage references up to the loop bandwidth. The inductor current reference is then given by the following equation:

$$I_{L1ref(t)} = \frac{I_{C1ref}(t) + I_{out}(t)}{1 - D_1(t)} \approx \frac{V_{O1}}{V_{in}}\left(I_{C1ref}(t) + I_{out}(t)\right) \tag{4.43}$$

This control strategy can be also seen as the result of compensating the plant variable gain (defined by$1/(1 - D_1(t))$) with $V_{o1}(t)/V_{in}$. Additionally, the output current disturbance is cancelled. The cancellation leads to good system performance during quick or sudden load variations. The final open loop system to be controlled consists of the capacitor transfer function provided by equation (4.35), and linear controllers can be designed by traditional techniques A freezing action can be activated if there is an integral term used in the controller [46].

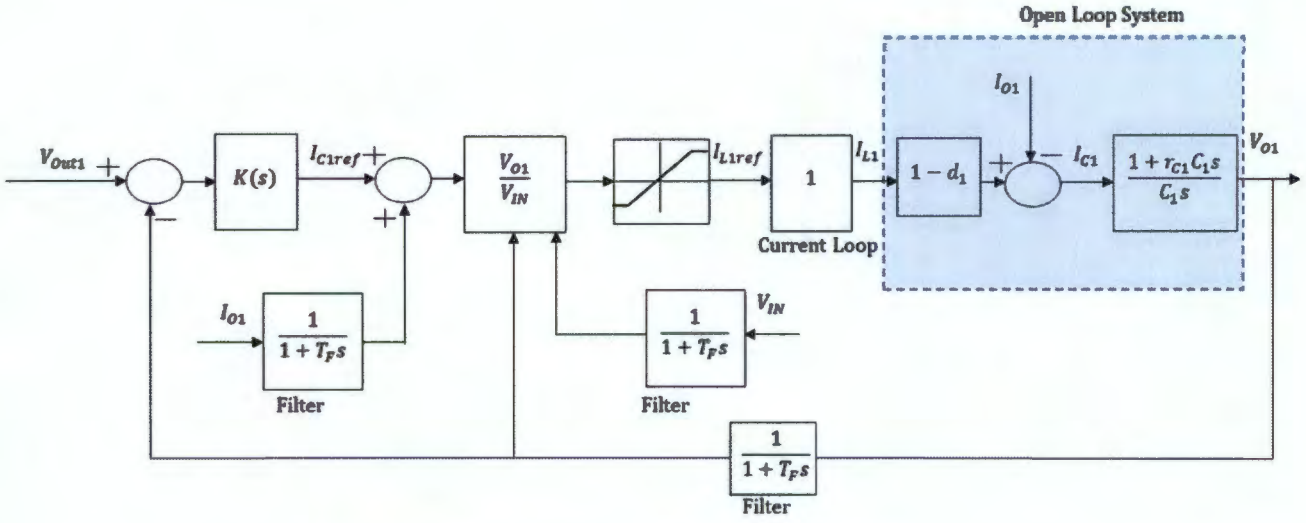


Figure 4.14: Capacitor voltage closed loop system [46].

4.6.2 *Boost Inverter's Controller DC Disturbance Analysis*

The boost converters model and control loops described in section 4.6.1 was derived by considering only lossy reactive passive components. The deadtime was not included in the derivations and it was shown in section 4.4 that the deadtime affects the input-output average voltage of the boost converter. Therefore, the inductor current control loop will experience variation of parameters and hence the compensation of nonlinearities will not be completely

eliminated. This scenario is represented here as a disturbance that occurs at the control input of the inductor current control inner loop as shown in Figure 4.15.

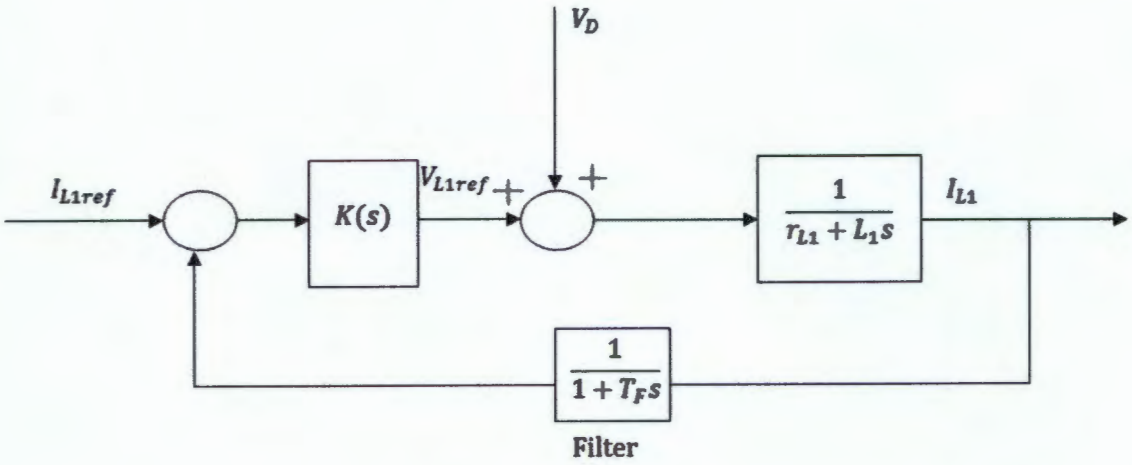


Figure 4.15: Inductor current control inner loop disturbance model.

The capacitor voltage control outer loop will also experience a disturbance due to parameter variations and measurement error. This scenario is also represented as a disturbance that occurs at the controller output of the capacitor voltage control outer loop. In order to simplify the overall control strategy, the inductor current control inner loop is represented by one and the disturbance effect at the control input of the inductor current control inner loop is represented as a disturbance at the output because the inductor current control inner loop has faster transients than the capacitor voltage control outer loop. The model of the capacitor voltage control loop is shown in Figure 4.16.

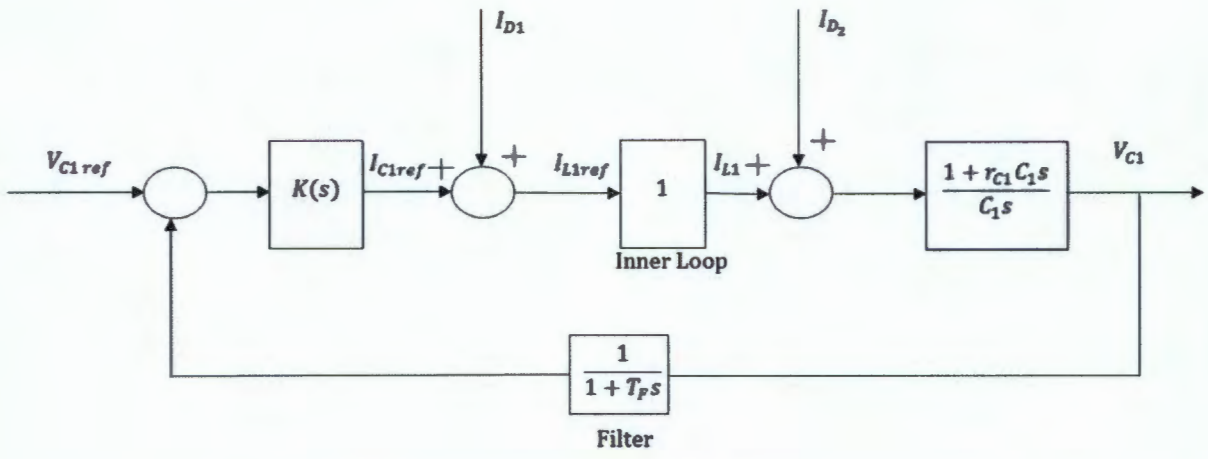


Figure 4.16: Capacitor voltage control outer loop disturbance model.

The disturbance rejection performance of the dc component is considered through analysis of the block diagram in Figure 4.16. The disturbance rejection performance of other frequency components of the disturbance is not considered through analysis. These will only be measured by considering the THD. From Figure 4.16, the two disturbance are lumped from block diagram algebra to form a single disturbance which is defined as follows

$$I_D = I_{D1} + I_{D2} \tag{4.44}$$

The reference (V_{C1ref}) of the model consists of dc and ac voltage component as discussed from section 4.1. The reference ac voltage component should be tracked accurately when a PR controller is used because of the infinite gain at the fundamental frequency. The capacitor voltage open loop transfer function is defined as

$$G(s) = \frac{1 + r_{c1}C_1 s}{C_1 s} \tag{4.45}$$

The equation above represents a Type 1 system, and, therefore, there is infinite gain at dc. Thus, a dc voltage reference is theoretically tracked with zero steady state error. However, with the introduction of the dc disturbance while using the PR controller, a steady-state error will exist. In order to demonstrate this, the gain at dc of the transfer function $D(s)$ between the disturbance and the output is determined. Furthermore, the reference is set to zero. The transfer function of $D(s)$ can be written as:

$$D(s) = \frac{V_{o1}}{I_D} = \frac{G}{1 + GK} \tag{4.46}$$

At dc $G(j0) \to \infty$ therefore $G(j0)K(j0) \gg 1$ then

$$D(j0) \to \frac{G(j0)}{G(j0)K(j0)} = \frac{1}{K(j0)} \tag{4.47}$$

Therefore, the gain of the $D(s)$ for the PR controller is

$$D(j0) = \frac{1}{K_p} \tag{4.48}$$

Therefore, the gain of $D(s)$ at dc depends on the proportional gain. The proportional gain value of PR controllers in reference [44] for the boost inverter was less than one, therefore a dc disturbance may be amplified. The proportional gain term is usually low to achieve a low bandwidth and hence a dc disturbance in the control input is amplified. In order to achieve zero gain at dc, the gain of the controller has to be infinite at dc. However, an integral term in the controller can be used to provide zero steady state error. This controller here is called the PIR controller and is written as:

$$K(s) = K_p + \frac{K_I}{s} + \frac{2K_R s}{s^2 + \omega_O^2} \tag{4.49}$$

where K_I is the integral term gain. The gain of $D(s)$ at dc when the PIR controller is used is

$$D(j0) = \frac{j0}{j0 \cdot K_p + K_I} = 0 \tag{4.50}$$

Therefore, the PIR controller can theoretically provide a zero steady-state error when a dc disturbance is present in the system.

5. Design of Boost Inverter System

This section presents the design of the experimental setup of the boost inverter system. The experimental setup consists of a dc power supply, passive components, switching devices, transducers and DSP for implementation of the control system. The block diagram of the boost inverter system is shown in
Figure 5.1.

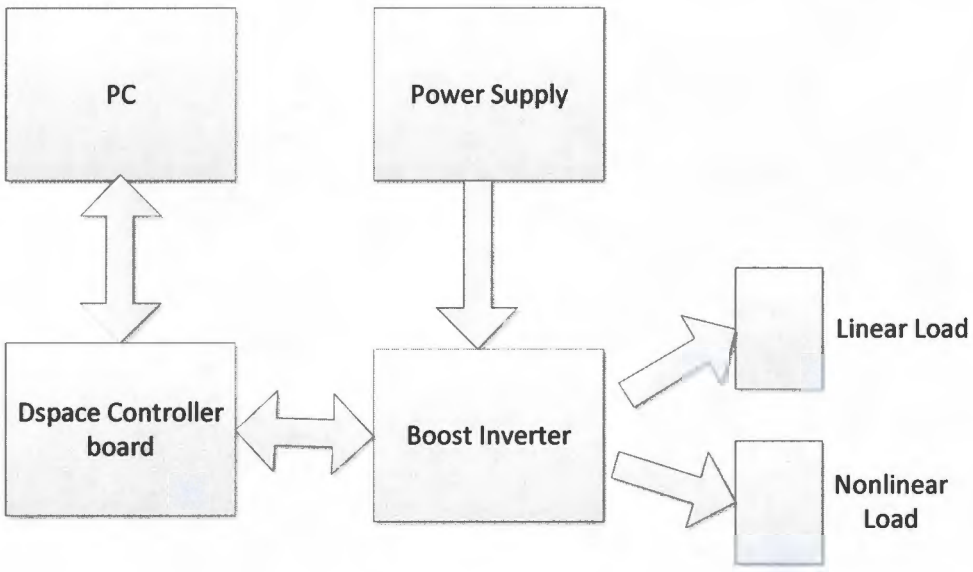


Figure 5.1: Block diagram of boost inverter system

5.1 Fuel Cell

The fuel cell in this system will be emulated using a DC Power Supply. The characteristics of the fuel cell that will be emulated are shown in the figure below. The fuel cell is rated at 1 kW. In this thesis the fuel cell is operated in the linear region of the voltage and current relationship. The voltage (V) and current (I) in the linear region is approximated by

$$V = -0.57I + 61.42 \tag{5.1}$$

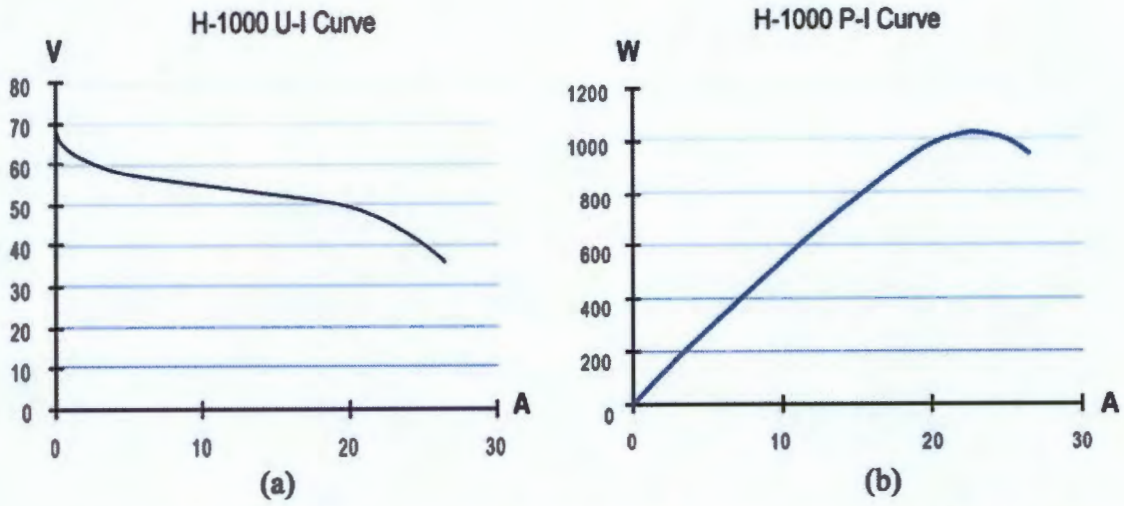


Figure 5.2: The 72 –cell PEMFC system showing (a) voltage-current characteristic and (b) power-current characteristic [65].

The voltage at rated power is approximately 50 V. In order to simplify experimental testing, 50 V will be used as the DC power supply voltage at loads lower than 1 kW for some experimental results. Thus, some of the experimental results will be a worst case scenario. However, for efficiency, THD, and output voltage regulation results, equation (5.1) will be used to determine the DC power supply voltage.

5.2 Passive Components Sizing of Boost inverter

This subsection shows the sizing of the inductor and capacitor of the boost inverter. The specifications for the passive components are shown in Table 5-1.

Table 5-1: Specifications for passive components design

FC Output Voltage	50 – 60 V_{DC}
AC Output Voltage	220 V_{AC} RMS, Single Phase, 50 Hz
Switching Frequency	20kHz
FC Output Power	1 kW
V_{in}	50 V(minimum)
r_L (inductor resistance)	< 90 mΩ
V_{1max}	380 V
V_{2min}	70 V
Δt_1 (maximum on time)	46 µs
Δi_L	< 30% of I_{Lmax}
ΔV_c	< 2% of V_{1max}
R_{Load}	48.4 Ω

The duty maximum on time is limited by the deadtime of the drivers, which is 2.7 μs, and some headroom has been provided in the specification above.

5.2.1 *Inductor Design*

The inductor current consists of two components. The first component is a low frequency component, which is the instantaneous average inductor current. The second component is a high frequency ripple caused by the switching. The maximum instantaneous average inductor current for the low frequency component is obtained by [36]:

$$I_{Lmax} = \frac{V_{in} - \sqrt{V_{in}^2 - 4r_L(-V_{1max}) \cdot (V_{2\min} - V_{1\max})/R_{Load}}}{2r_L} \tag{5.2}$$

where r_L is the inductor series resistance and R_{Load} is the load .The high-frequency ripple is given by [36]

$$\Delta i_L = \frac{(V_{in} - r_L I_{Lmax}) \cdot \Delta t_1}{L} \tag{5.3}$$

where Δi_L is the peak to peak amplitude of the high frequency component of the inductor current. The maximum instantaneous average inductor current (I_{Lmax}) is obtained from equation (5.2) by substituting parameters from Table 5-1 to give the following

$$I_{Lmax} = 53.9\,A \tag{5.4}$$

In order to determine the inductance required, equation (5.2) is rearranged as follows,

$$L = \frac{(V_{in} - r_L i_{Lmax}) \cdot \Delta t_1}{\Delta i_L} \tag{5.5}$$

The inductance was determined by

$$L = \frac{(V_{in} - R_a i_{Lmax}) \cdot \Delta t_1}{\Delta i_L} \tag{5.6}$$

By substituting the parameters from Table 5-1, the required inductance was 128 μH. The inductor was designed using the N87 E70/33/32 ferrite core and a multi-stranded wire was used. The designed inductance measured 135 μH with series resistance of 85 mΩ at a frequency of 20 kHz.

5.2.2 *Capacitor Sizing for the Boost inverter*

The control strategy of the boost converter drives the capacitor to follow the dc-biased low frequency sinusoidal voltage ($V_1(t)$). Additionally, there is a high frequency ripple caused by the switching that is imposed on $V_1(t)$. The high frequency ripple is given by [36]:

$$\Delta V_c = \left(\frac{(V_{1\max} - V_{2\min})}{CR_{load}}\right) \cdot \Delta t_1 \tag{5.7}$$

The reactive power of the capacitor can be obtained as follows:

$$Q = V_{rms}^2 2\pi f C \tag{5.8}$$

The capacitance required is determined by rearranging equation (5.7), as follows.

$$C = \left(\frac{(V_{1\max} - V_{2\min})}{\Delta V_c R_{load}}\right) \cdot \Delta t_1 \tag{5.9}$$

By substituting the parameters from Table 5-1, the required capacitance is 39 μF. Film capacitors of 50 μF were used because they were readily available in the laboratory and they met the specifications. The reactive power through this capacitor is 190.06 VAR, which is about 19% of rated power of the fuel cell. Furthermore, snubber capacitors of 0.47 μF were used to lower the overvoltages caused by the stray inductance.

5.3 Decoupling Capacitor

A decoupling capacitor was required for the DC power supply because the voltage fluctuates when a 100 Hz current is drawn. Furthermore, this decoupling would be required for a real FC in order to mitigate the hysteresis effect explained in section 2.4.1i.

The value of the decoupling capacitor size was determined by [20]

$$C_{decoup} = \frac{P_{rated}}{2\pi f V_{in} \Delta V_{in}} \tag{5.10}$$

where P_{rated} is the FC rated power, ΔV_{in} is the allowed peak-to-peak variation and f is the power frequency (100 Hz). In this case, ΔV_{in} was selected to be a maximum 7 V. This ripple was not considered an issue for stability or output voltage distortion for the boost inverter because there is a feed-forward in the control scheme for the boost inverter that compensates for these variations of input voltage, as described in section 4.6.1. By substituting the specifications from Table 5-1, the required capacitance is 4.546 mF. A 10mF capacitor was used because it was readily available from the laboratory and it also met the specifications.

5.4 Switching Device Selection

There are many semiconductor devices available in the market and it has become difficult to select the best device for different applications [66]. Figure 5.3 illustrates a basic selection guideline chart between IGBT and MOSFET.

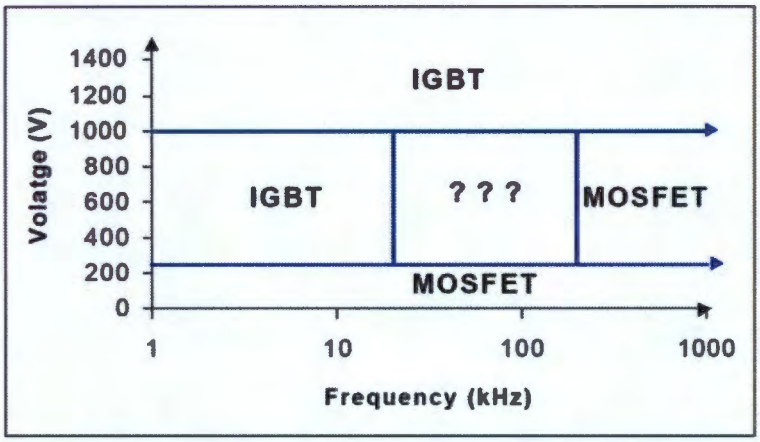


Figure 5.3: Selection guideline chart between IGBT and MOSFET [66].

From chart above, the IGBT is the most preferred at high voltages and low frequency. Therefore, for this application of the boost inverter the IGBT was selected.

The chosen switching device is SKM100GB125DNIGBT module, from SEMIKRON. It is capable of switching beyond 20 kHz and is rated 100 A and 1200 V.

5.5 PWM Board

An analog PWM board was built to generate the PWM signals that feed the driver modules. This board was built such that the switching frequency and duty cycle could be varied by an analog signal from a DAC. The functional block description of the PWM board is shown in Figure 5.4.

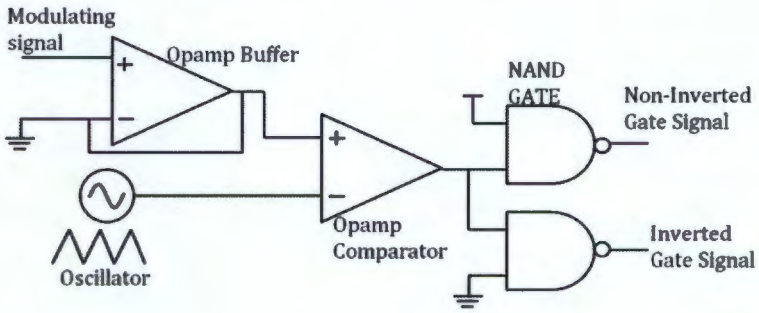


Figure 5.4: Functional block description of the PWM board.

From Figure 5.4, the modulating signal commands the required duty cycle, which is compared through an opamp with a high frequency carrier signal from the oscillator. The oscillator frequency can be varied by an analog signal. Furthermore, the Opamp comparator generates a PWM signal that gets inverted and non-inverted through a NAND gate logic chip. The non-inverted and inverted signal gate signals are shown in Figure 5.5 for 50% duty cycle with 50 kHz frequency.

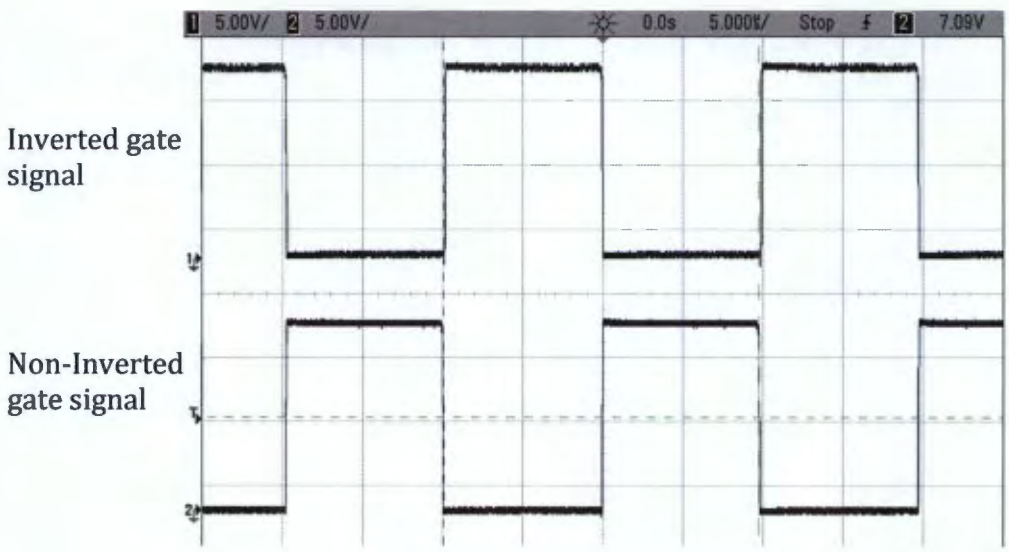


Figure 5.5: PWM signals from PWM Board.

5.6 Drivers

The drivers used for this application are the SKHI 21. These are double drivers for half bridge modules that have short circuit protection and have a drive interlock for the top and bottom of bridge leg. Furthermore, there is isolation through transformers and an adjustable deadtime. The deadtime was set to the absolute minimum of the driver's capability, which is 2.7 μs. This deadtime was set because the IGBT is an ultra-fast switching module, which has fast rise and fall switching times. The wires that were carrying the switching signals were twisted in order to avoid noise coupling issues. The wires were also made as short as possible to minimize the inductance.

5.7 Transducers

The transducers required to realize the control system which was discussed are as follows:

- 2 Current Transducers; range: -40 – 80 A.
- 1 Current Transducer; range: -10 – 10 A.
- 2 Voltage Transducers; range: 0- 500 V.
- 1 Voltage Transducer; range: 0 – 100 V.

The transducers that are required for the feedback signal must have very good linearity, high bandwidth, good common and external noise rejection ratios. The selected transducers are the LEM LV25P and LA55P because they provide good performance and are widely used.
Second order active filters were used on the two current transducers because of the relatively large high frequency inductor current ripple; high bandwidth of the inductor current control inner loop; and anti-aliasing. The filter used was a Sallen and Key filter, as shown in Figure 5.6.

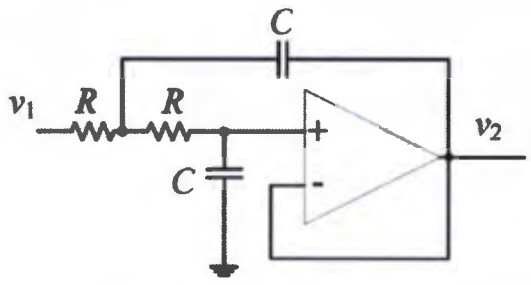


Figure 5.6: Sallen and Key filter.

The cut-off frequency of the Sallen and Key filter is

$$f_C = \frac{1}{2\pi RC} \tag{5.11}$$

The cut-off frequency was set to 5 kHz due to the high bandwidth of the inductor current control inner loop. A first order passive filter with a cut-off frequency at 1 kHz was used for the capacitor voltage control outer loop because the high frequency voltage ripple is small; the capacitor voltage control outer loop bandwidth is low; and anti-aliasing.

5.8 Closed Loop Design

In this subsection, the gain parameters of the PR and PIR controllers are determined. These controllers are designed for the control strategy described in section 4.6, whereby the controllers can be designed by considering only the dynamic equations of the inductor and capacitor for the inner and outer control loops. Thus, linear control theory methods are used to design the PR and PIR controllers. The performance of these controllers will be shown in circuit model of the boost inverter in MATLAB Simulink in section 6.

5.8.1 Controller Design Approach

The two-step design approach for PR controllers described in section 4.6.1 will be used to determine the proportional and resonant gains of both the PR and PIR controller. Furthermore, these controllers are implemented on a dSpace controller board which has a relatively high sampling rate. Thus, the plant and controllers are modelled by continuous transfer functions [67]. The proportional gain is designed using pole-zero methods, where the Characteristic Equation of the closed loop is firstly defined. Thereafter, the proportional gain that achieves the desired transient response and stability is determined. This proportional gain will be used to show the closed loop poles on the root locus to verify the transient response using the MATLAB SISOTOOL. The resulting bode plot of the open loop is also plotted to show the crossover frequency and stability margins. The crossover frequency is an approximation of the bandwidth of the closed loop system.

The resonant gain of the PR controller is designed by frequency response methods, where the bode plots of the open loop system are used. The proportional gain term would be defined at

this stage, and the resonant gain is selected to meet the phase margin, bandwidth and gain margin specifications. The integral gain of the PIR controller is also selected based on the phase margin, bandwidth and gain margin specification by using bode plots.

The closed loop specifications for the inner and outer loops are shown in Table 5-2.

Table 5-2: Closed loop specifications for inner and outer loops.

Inner Loop Bandwidth	2 kHz
Outer Loop Bandwidth	200 Hz
Phase margin for each loop	> 70°
Gain margin for each loop	> 6 dB

From the specifications above, the equation used to indicate the pole locations required on the negative real axis of the s-plane can be written as [67]:

$$pole = \frac{1}{T} = \omega = 2\pi \times B \tag{5.12}$$

where B is the bandwidth (Hz) and T is the time constant.

5.8.2 *Inner Loop Design*

The open loop plant of the inner loop can be expressed as:

$$G_L = \frac{1}{Ls + r_L} \tag{5.13}$$

The required position on the negative real axis of the s-plane for the inner loop's closed loop pole, as indicated in Table 5-2 is given as:

$$pole = 2\pi \times 2000 \tag{5.14}$$

i. Proportional Gain

The first step in the design is to determine the proportional gain. Therefore, the controller for the inner loop plant is written as:

$$K = K_P \tag{5.15}$$

Thus, the Characteristic Equation for the closed loop system is

$$\begin{aligned} Ls + K_p + r_L &= 0 \\ \therefore s &= -\frac{K_p + r_L}{L} \end{aligned} \tag{5.16}$$

The position of the closed loop pole is given in equation (5.14) and the proportional gain can be determined as follows from (5.16) (where $s = -pole = -\omega$) :

$$\begin{aligned} K_P &= \omega L - r_L \\ \therefore K_P &= 1.609 \end{aligned} \tag{5.17}$$

The root locus of the inner loop plant with the above proportional gain is shown in Figure 5.7.

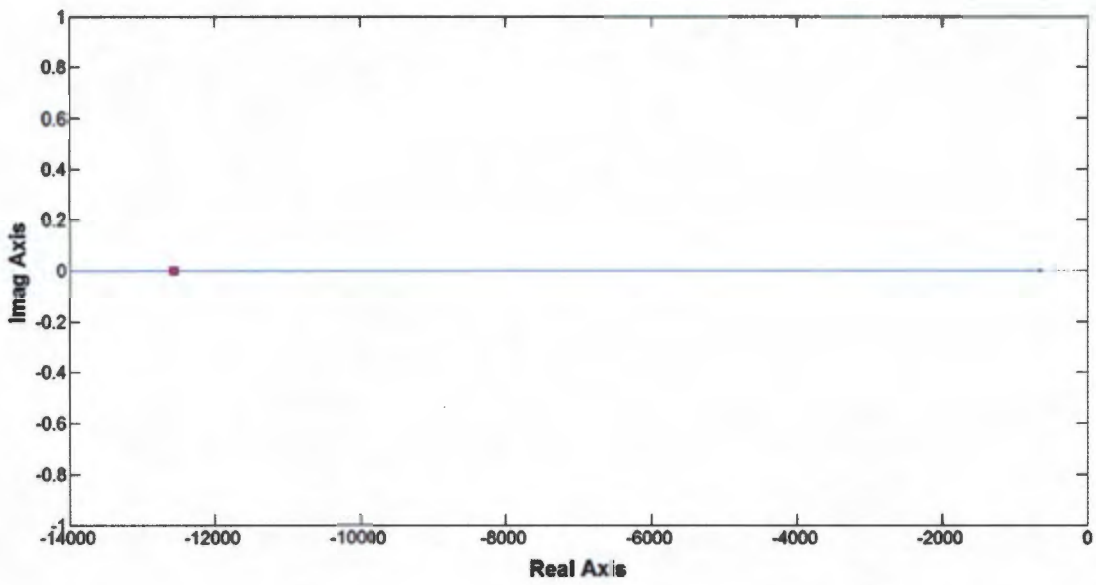


Figure 5.7: Root locus of inner loop.

For the propotional gain of 1.607, the closed loop pole is expected to be at 12566.37 on the s-plane. The closed loop pole position is represented by the cube in Figure 5.7 and it is at the desired pole location. Therefore, 1.607 was used as the proportional gain.

The bode plot of the inner loop plant with the proportional controller is shown in Figure 5.8. The gain margin is infinite and phase margin is 93.1°. Therefore, the stability margin specifications from Table 5-2 were met. The crossover frequency is at 1.89 kHz.

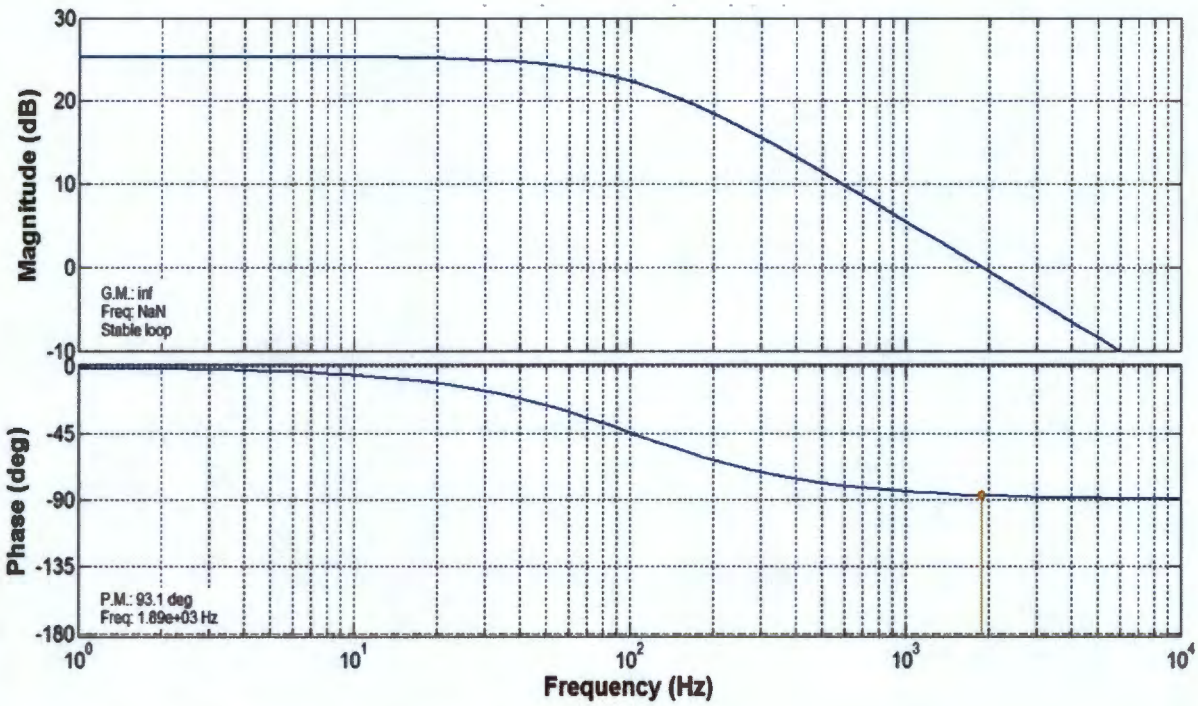


Figure 5.8: Bode plot of inner loop plant with proportional controller.

ii. ***Resonant Gain***

The resonant gain was found using the trial and error method on the bode plot of the inner loop until satisfactory results were achieved. The value that was used at the end of the process was 20. The resonant gain had a very small effect on the crossover frequency and gain margin because the resonant frequency is 40 times lower than the bandwidth. However, it did affect the phase margin in relatively small amounts. The bode plot of the inner loop plant with the PR controller is shown in Figure 5.9. The gain margin is infinite and phase margin is 92.8°. The crossover frequency is still 1.89 kHz. Therefore, the stability margins and bandwidth specifications from Table 5-2 were still met.

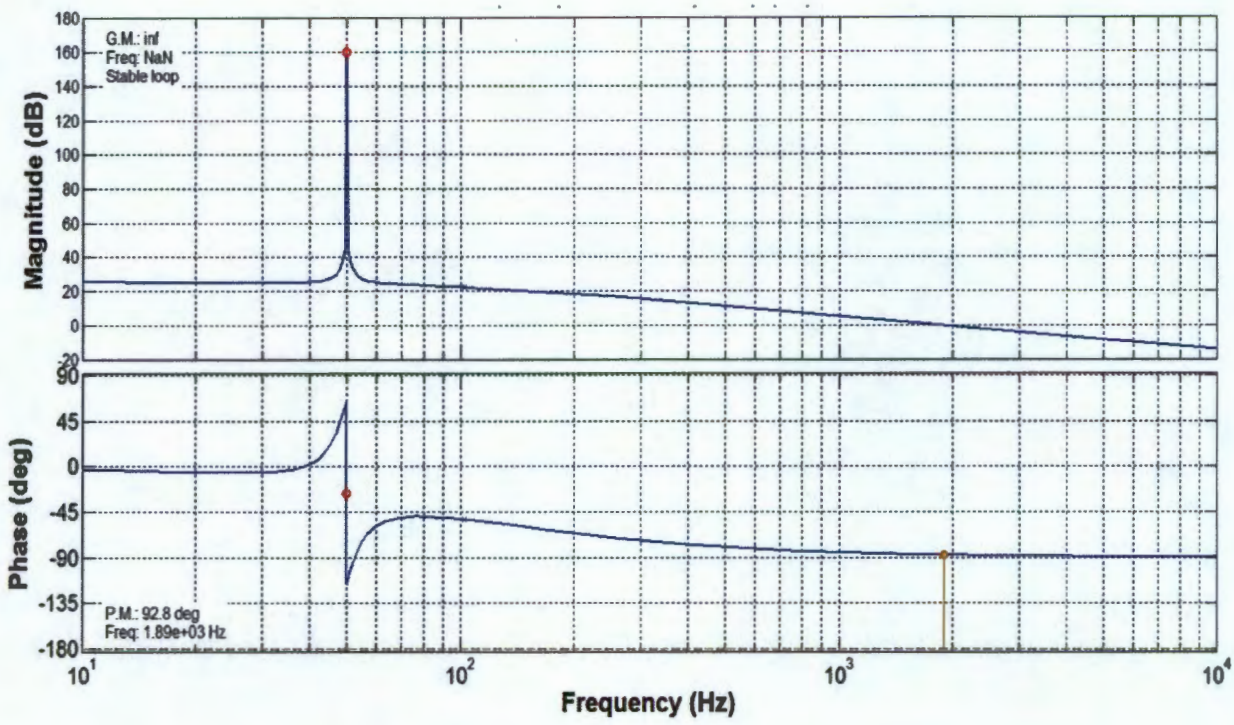


Figure 5.9: Bode plot of inner loop plant with PR controller.

5.8.3 Outer Loop Design

The outer loop's open loop plant can be written as:

$$G_2 = \frac{r_{C1}C_1 s + 1}{C_1 s} \tag{5.18}$$

The closed loop pole position, on the negative real axis of the s-plane, for the outer loop is given as:

$$pole = 2\pi \times 200 \tag{5.19}$$

i. Proportional Gain

The Characteristic Equation of the closed loop system with a proportional controller can be expressed as:

$$sC_1 + sK_P r_{C1} C_1 + K_p = 0$$
$$\therefore s = -\frac{K_P}{K_p r_{C1} C_1 + C_1} \tag{5.20}$$

The closed loop pole position is given in equation (5.19) and the proportional gain can be determined as follows:

$$K_P = \omega C_1 + \omega K_P r_{C1} C_1$$
$$\therefore K_P = 0.067 \tag{5.21}$$

The root locus of the outer loop plant has an open loop pole zero- pair. Therefore, the root locus begins at the pole position and ends at the zero position. The full and zoomed in root locus of the outer loop plant with the above proportional gain is shown Figure 5.10 and Figure 5.11, respectively.

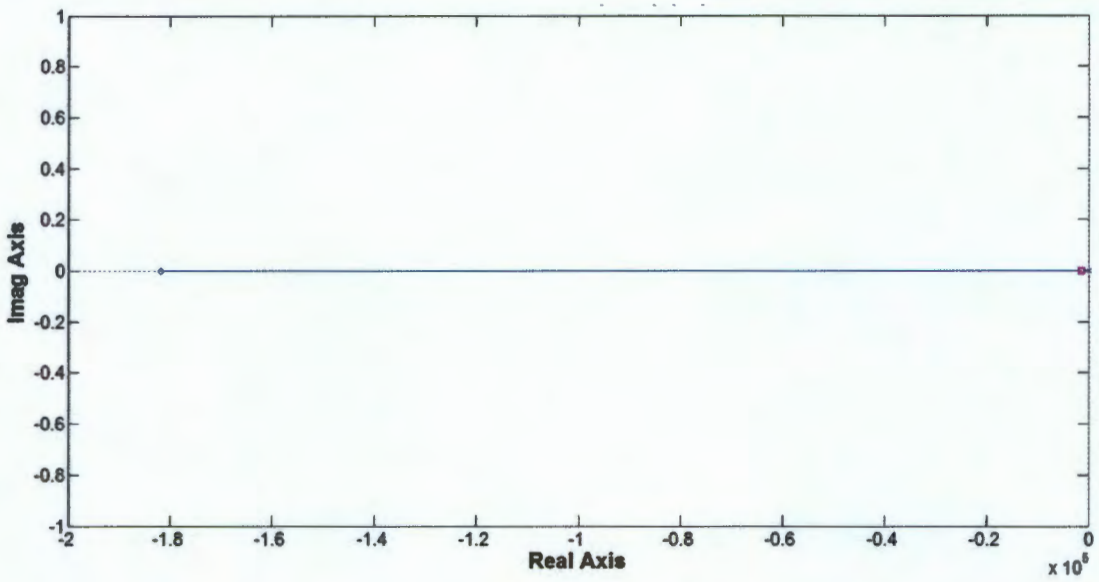


Figure 5.10: Root Locus of outer loop plant with proportional controller.

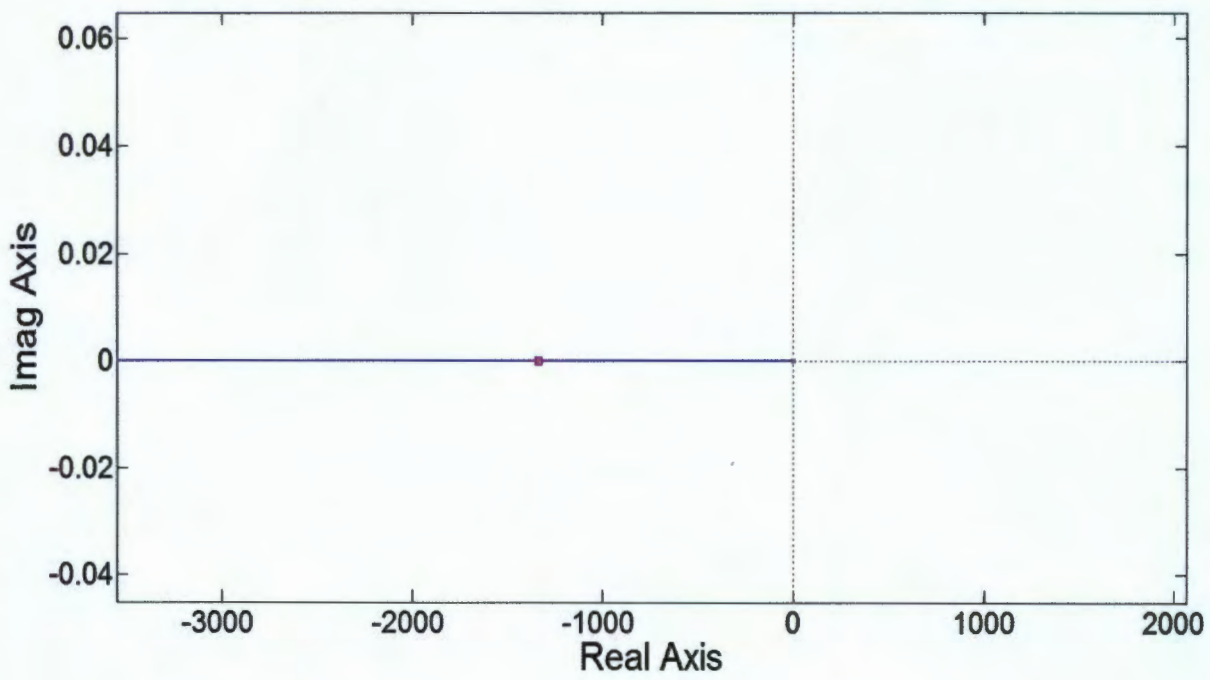


Figure 5.11: Zoomed in root locus of outer loop plant with proportional controller.

Figure 5.11 indicates the closed loop pole location is at the desired location of 1256.63. Therefore, 0.067was used as the proportional gain.

Figure 5.12 shows the bode plot of the outer loop plant with the proportional controller, which illustrates that the gain margin is infinite and phase margin is 90.4°. Thus, the stability margin specifications from Table 5-2 were met. Furthermore, the crossover frequency is at 213 Hz.

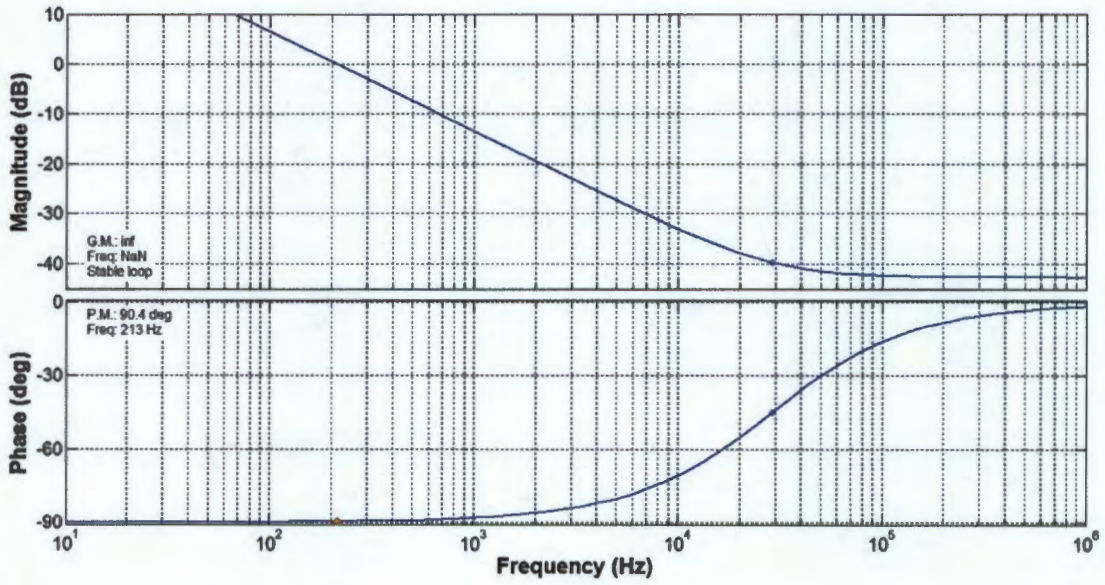


Figure 5.12: Bode plot of outer loop plant with proportional controller.

ii. ***Resonant Gain***

As mentioned previously, the resonant gain was found using trial and error with bode plots. The value that was used at the end of the process was 20. This gain was considered sufficient because the phase margin was easily affected by the gain since the resonant frequency is close to the bandwidth. The bode plot of the outer loop plant with the PR controller is shown in Figure 5.9.

The gain margin is infinite and phase margin is 77.5°, which meets the stability margin specifications. However, the crossover frequency is at 219 Hz, which indicates that the bandwidth has increased compared to outer loop plant with the proportional controller shown in Figure 5.12. However, this was considered a small increase (6 Hz) and no further changes were made.

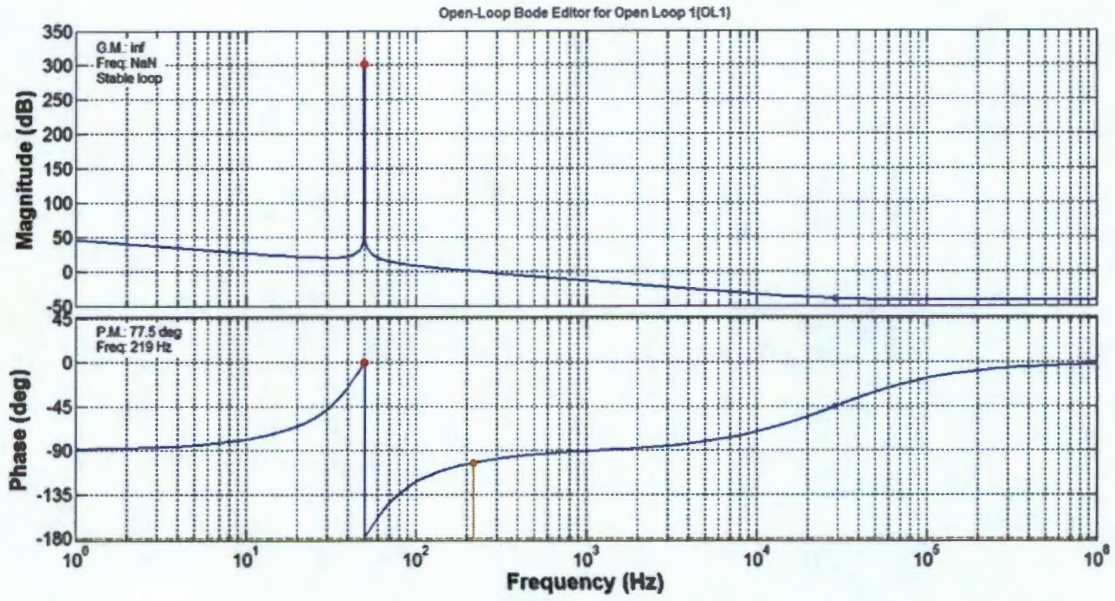


Figure 5.13: Bode plot of outer loop plant with PR controller.

iii. ***Integral Gain***

The integral gain term was found by trial and error on the bode plot until suitable results were attained. The gain selected was 5, because the gain affects the phase margin and crossover frequency. The bode plot is shown below Figure 5.14.

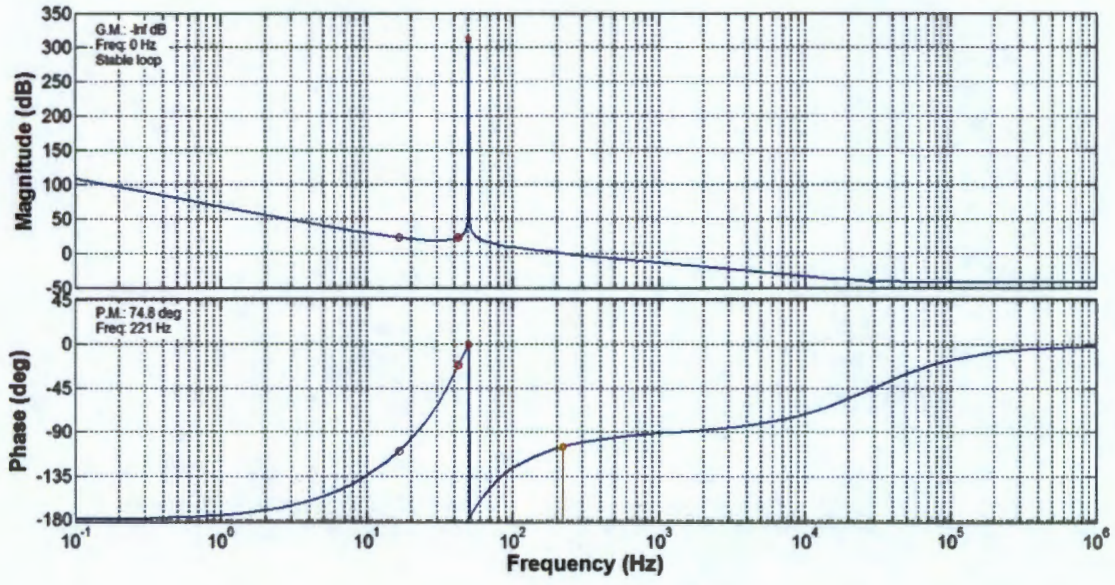


Figure 5.14: Bode plot of outer loop plant with PIR controller.

The phase margin is 74.8° and has decreased by 2.7° compared to Figure 5.13. The gain margin is also infinite, thus the stability margins specifications are met. The transient reponse is faster because the crossover frequency has increased by 2 Hz compared to Figure 5.13.

5.9 Implementation of Digital Control system

The digital controller was implemented on a dSpace DS1104 prototyping controller board. The dSpace kit achieves real time implementation and parameter variation. The DS1104 controller board has 250MHz Digital Signal Processor (DSP) with a 64 bit-floating point math processor. The control system for the boost inverter is created in MATLAB Simulink and C code is generated by the real time workshop. The C code is then loaded on the DSP and the sampling time is setup in the solver of Simulink.

The dSpace controller board has ADCs and DACs for interfacing to the transducers and creating the required analog signals. The data from the ADC and signals of the Simulink model can be saved while the control system is running.

5.10 Experimental Set-up

The experimental set-up is shown in Figure 5.15

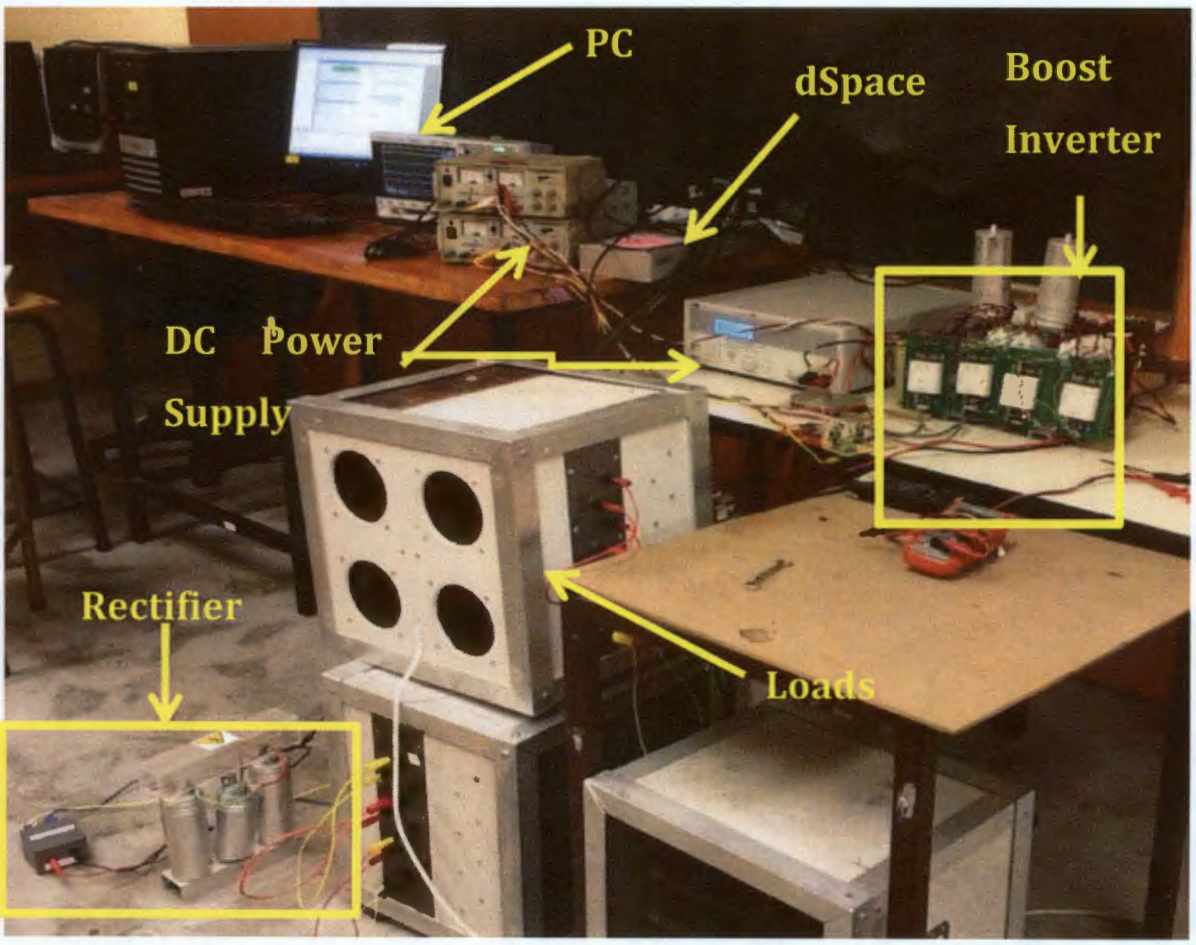


Figure 5.15: Experimental set-up.

6. Simulation Results of the Boost Inverter

In this section, the circuit model of the boost inverter is modelled in MATLAB Simulink such that it resembles the experimental setup as closely as possible. The simulations demonstrate the open loop response, closed loop response and various disturbance rejection performance of the boost inverter system.

6.1 Open Loop Simulation

These open loop simulations show how the boost inverter performs when the boost converters are driven by ideal duty cycle signals. These signals are given by equation (4.9) and the parameters are determined from Table 5-1. The resulting duty cycle signals are as follows

$$D_1(t) = 1 - \frac{50}{70 + \frac{1}{2}220\sin(2\pi 50t)} \tag{6.1}$$

$$D_2(t) = 1 - \frac{50}{70 + \frac{1}{2}220\sin(2\pi 50t - \pi)} \tag{6.2}$$

The dc offset (70 V) is determined from the worst case fuel cell voltage of 50 V with an additional offset of 20 V due to the minimum duty cycle that the gate drivers on the experimental setup can obtain and the low frequency ripple on the input side capacitor. The duty cycle waveforms are shown in Figure 6.1

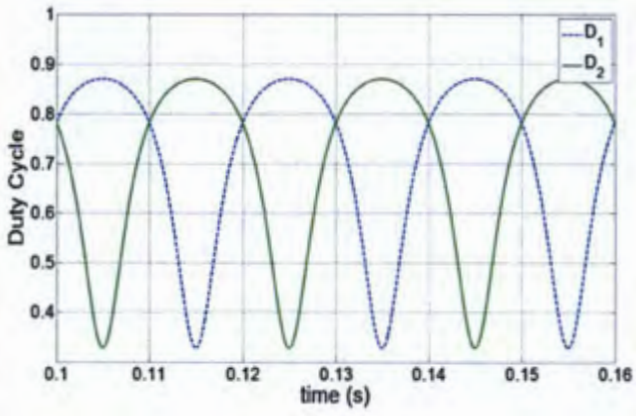
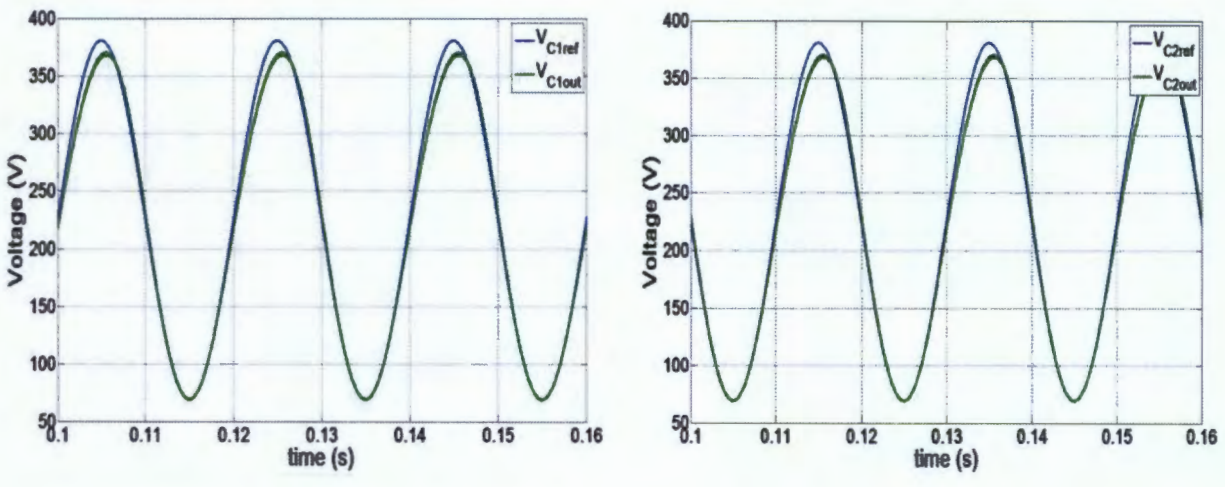


Figure 6.1: Duty cycle signals for each boost converter.

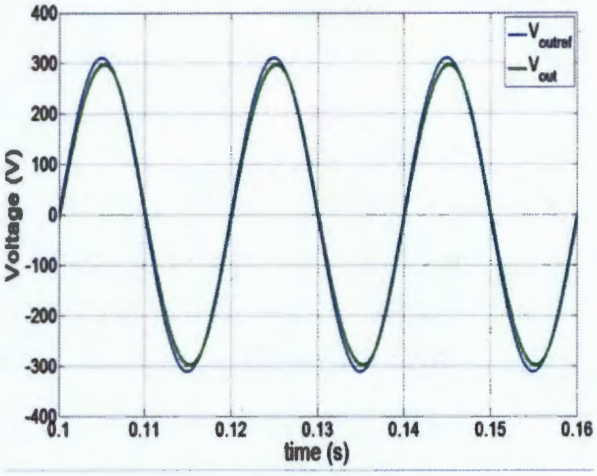
In order to demonstrate the contribution of the deadtime to the output voltage's distortion and magnitude difference between the ideal and simulated result, the boost inverter's open loop response is simulated in two different forms. The first simulation form considers the contribution from only lossy reactive components. Thus, the parasitic capacitance of the switching devices and deadtime is not accounted for in the simulation model. In the second form, the lossy reactive components are modelled along with parasitic capacitance of the switching devices and deadtime of the gate drivers. The second form of the simulation model closely represents the experimental boost inverter because the deadtime, parasitic capacitance and lossy reactive components parameters are found from datasheets and measurements of the experimental set-up components. Therefore, these simulation results will be compared with the experimental results. The simulation of the switching technique that the boost converters undergo, as discussed in section 4.3, also are presented. The boost inverter open loop simulation model has a dc voltage input of 50V and 68 Ω load.

6.1.1 Boost Inverter with Lossy Reactive Components

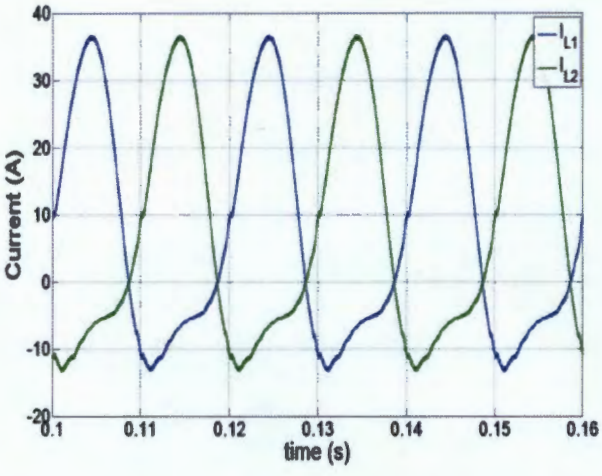
The boost inverter's simulation model with only lossy reactive components is shown in Appendix A.1. The simulation results are shown in Figure 6.2. The dc and fundamental output voltage magnitudes of the boost inverter simulation results are compared with the ideal output voltage magnitudes in Table 6-1.



(a) (b)



(c)



(d)

Figure 6.2: Simulation results of boost inverter with lossy reactive components of a) boost converter 1 output voltage and b) boost converter 2 output voltage c) voltage across load and d) inductor current of both converters.

Table 6-1: Comparison between simulation output voltages and ideal output voltages of boost inverter with lossy reactive components.

Output Voltage	$V_{DC\,SIM}$ $[V]$ ($V_{DC\,Ideal}[V]$)	$V_{50Hz\,SIM}$ $[V_{RMS}]$ ($V_{50Hz\,Ideal}[V_{RMS}]$)
V_{C1}	221.34 (225)	105.91 (110)
V_{C2}	221.34 (225)	105.91 (110)
V_{out}	0(0)	211.83 (220)

Table 6-1, illustrates that the boost converter's output voltage magnitude and the boost inverter's output voltage magnitude are relatively close to the ideal magnitudes. The THD of the output voltage (V_{out}) is 1.17%.

6.1.2 *Boost Inverter with Lossy Reactive Components, Switching Device Parasitic Capacitance and Deadtime*

The simulation results of the boost inverter with lossy reactive components, parasitic capacitance of the switching devices and deadtime are shown in Figure 6.3. Furthermore, the dc and fundamental output voltage magnitudes are compared with the ideal output voltage magnitudes in Table 6-2. The simulation model is shown in Appendix A.2.

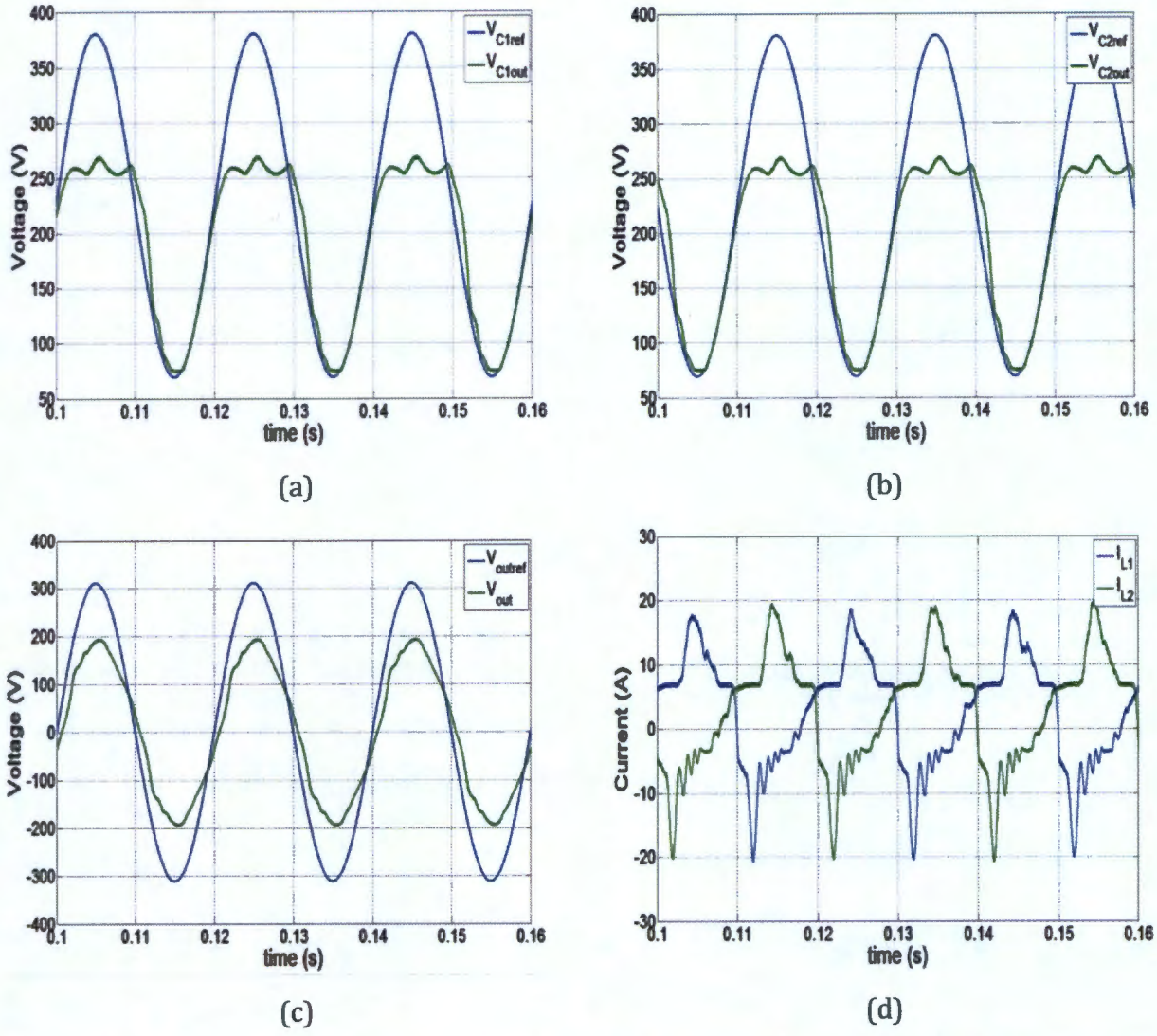


Figure 6.3: Simulation results of boost inverter with non-ideal elements added with rated load of filtered a) boost converter 1 output voltage and b) boost converter 2 output voltage c) voltage across load and d) inductor current of both converters

Table 6-2: Comparison between simulation output voltages and ideal output voltages of boost inverter with lossy reactive components, switching device parasitic capacitance and deadtime.

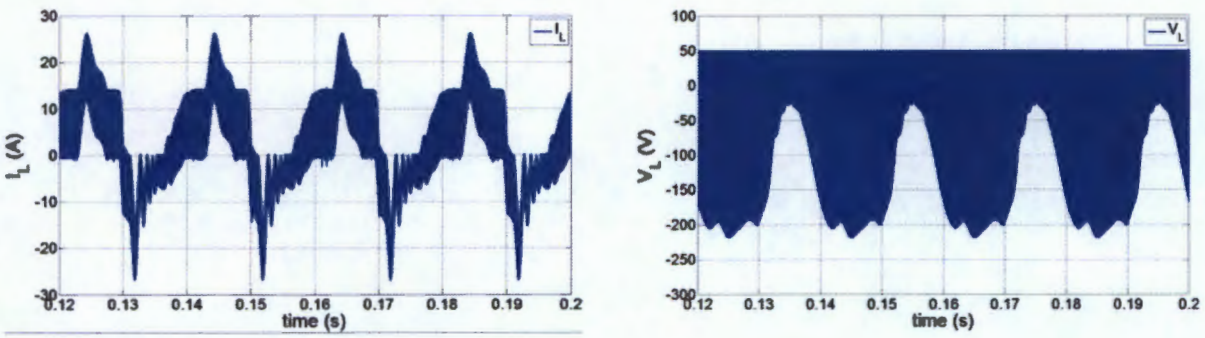
Output Voltage	$V_{DC\,SIM}$ $[V]$ ($V_{DC\,Ideal}[V]$)	$V_{50Hz\,SIM}$ $[V_{RMS}]$ ($V_{50Hz\,Ideal}[V_{RMS}]$)
V_{C1}	195.82 (225)	67.32 (110)
V_{C2}	195.81 (225)	67.31 (110)
V_{out}	0.01(0)	134.94(220)

The output voltage magnitudes of the boost converters and the boost inverter are not close to the ideal magnitudes, as shown in Table 6-2. The THD of the output voltage (V_{out}) is 6.76%.

Thus, the deadtime further distorts the output voltages of the boost inverter by 5.59% and it further decreases V_{out} by 76.89V from the results in section 6.1.1.

6.1.3 *Switching Technique Simulation Results*

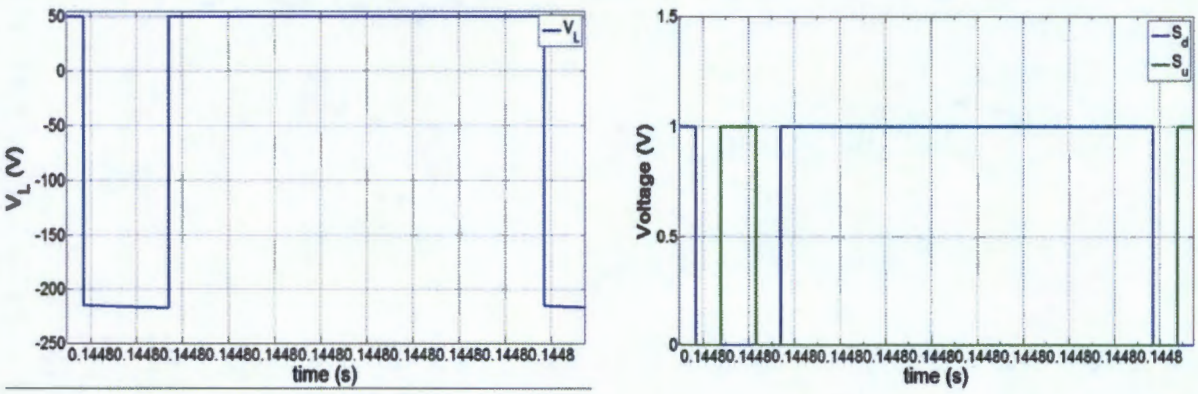
The boost converters undergo different switching techniques throughout the period of the inductor current, as suggested in section 4.3 and 4.4. The instantaneous inductor current and inductor voltage waveforms of boost converter 1 from the open loop response are shown in Figure 6.4.



(a) (b)

Figure 6.4: Simulation results of (a) instantaneous inductor current and (b) instantaneous inductor voltage for boost converter 1.

The switching techniques are shown by zooming in different regions of the inductor voltage and switching waveforms for boost converter 1. The hard-switching; ZVRT; transition between ZVRT and hard-switching; resonance between the inductor and parasitic capacitance of the IGBT is shown in Figure 6.5, Figure 6.6, Figure 6.7 and Figure 6.8, respectively. These results match the analysis conducted in section 4.4.



(a) (b)

Figure 6.5: Simulation results of hard-switching with zoomed-in instantaneous (a) inductor voltage and (b) switching signals S_d and S_u.

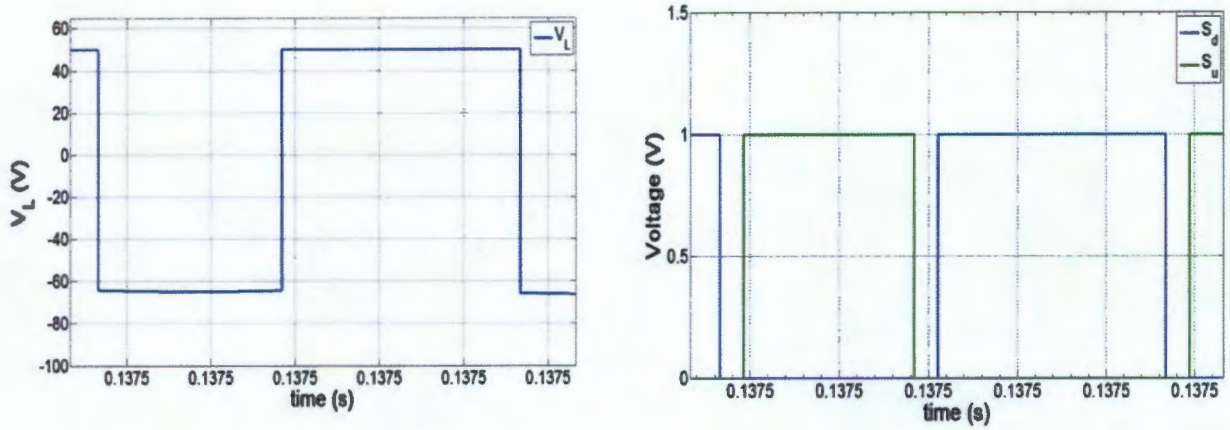
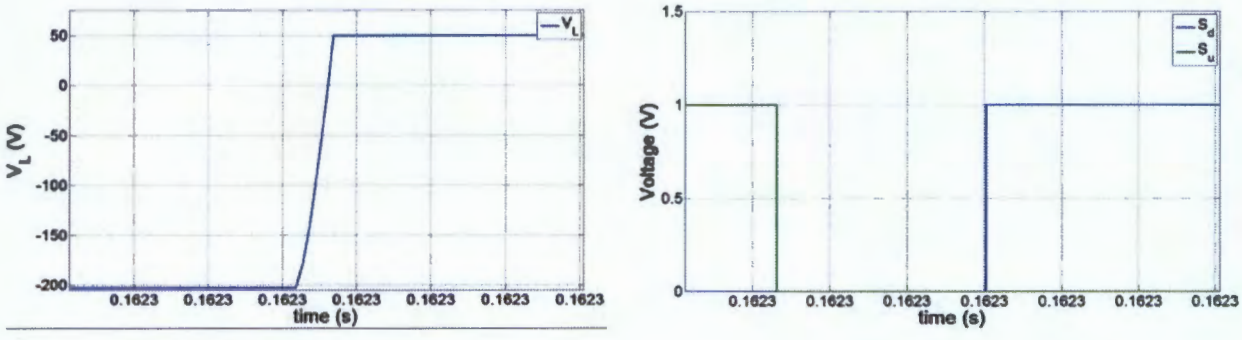
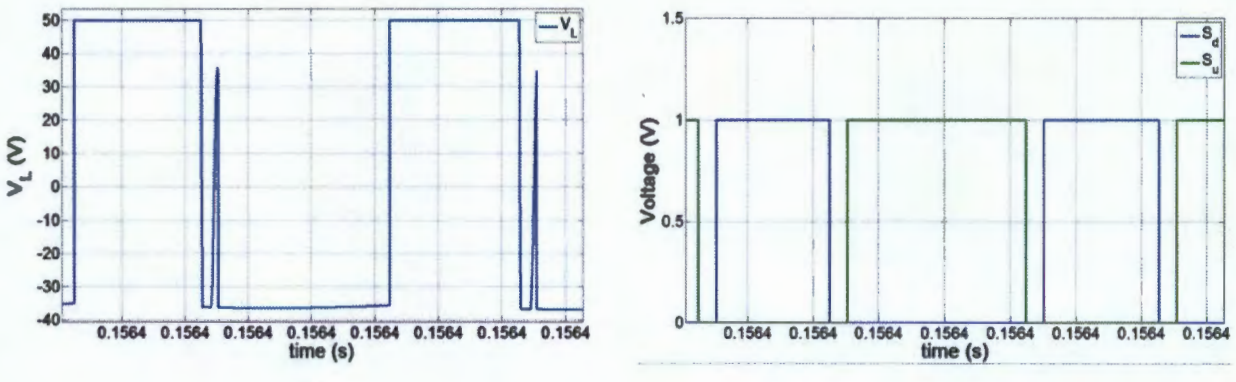


Figure 6.6: Simulation results of ZVRT with zoomed-in instantaneous (a) inductor voltage and (b) switching signals S_d and S_u.



(a) (b)

Figure 6.7: Simulation results of transition between ZVRT and hard-switching with zoomed-in instantaneous (a) inductor voltage and (b) switching signals S_d and S_u.



(a) (b)

Figure 6.8: Simulation results of resonance with zoomed-in instantaneous (a) inductor voltage and (b) switching signals S_d and S_u.

6.2 Closed loop Simulation of Boost inverter

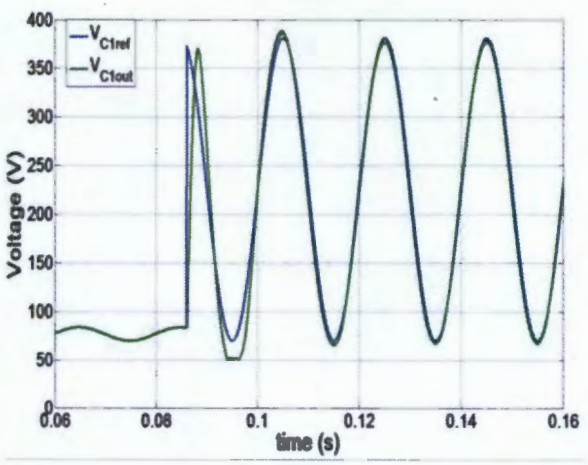
The closed loop simulation model in MATLAB Simulink contains only continuous-time blocks because the sampling frequency (30 kHz) of the dSpace controller board is much higher than the inner loop bandwidth (5 kHz). The closed loop simulations show the performance of the PR and PIR controllers with the control parameters determined in section 5.8.

6.2.1 PR Controller Simulations

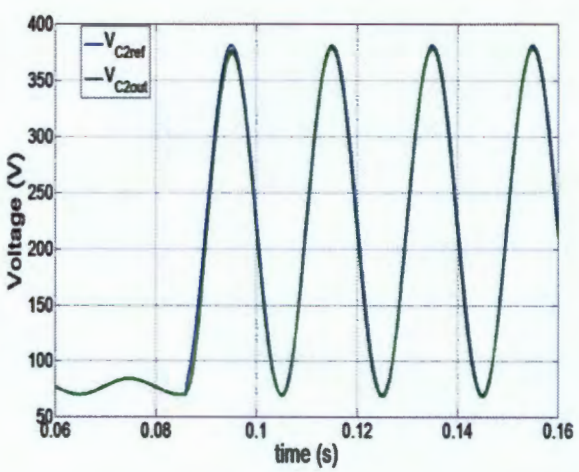
In the open loop simulations it was shown that the deadtime prevented the dc component output voltage of the boost converters from being tracked. Therefore, the PR controllers will experience poor dc disturbance rejection performance, as shown in section 4.6.2. The PR controller performance is shown in two different cases. In the first case, the model only considers lossy reactive components and in the second case, the deadtime, parasitic capacitance of the switching device is added. The boost inverter simulation model has 100 Ω load and the dc power source is set to 50V.

i. PR Controller with Lossy Reactive Components

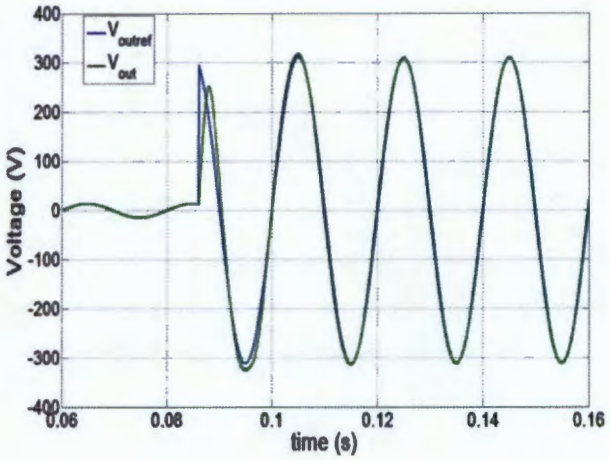
The simulation results of the boost inverter with lossy reactive components and PR controllers in the inner loop and outer loop are shown in Figure 6.9. Table 6-3 further shows the comparison of the simulation output voltages and the reference output voltages. The simulation model can be seen in Appendix A.3.2.



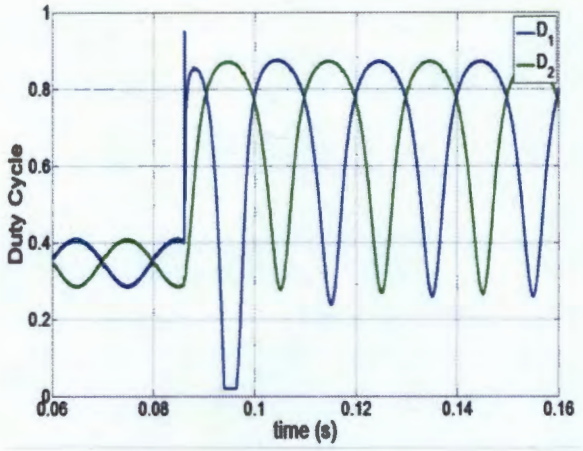
(a)



(b)



(c)



(d)

Figure 6.9: Simulation results of boost inverter with PR controller and lossy reactive components, of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) voltage across load. And d) duty cycle signals of both converter.

Table 6-3: Comparison of output voltages from simulation results with ideal results of boost inverter with PR controller and lossy reactive components.

Output Voltage	$V_{DC\ SIM}$ $[V]$ ($V_{DC\ Ref}[V]$)	$V_{50Hz\ SIM}$ $[V_{RMS}]$ ($V_{50Hz\ Ref}[V_{RMS}]$)
V_{C1}	225.86 (225)	110.03 (110)
V_{C2}	225.87 (225)	110.03 (110)
V_{out}	-0.01 (0)	220.08 (220)

The transients of the output voltages, Figure 6.9 (a)–(c), decay within a period of the fundamental voltage. This is expected because the bandwidth of the outer loop (200 Hz) is four times the fundamental. Furthermore, Table 6-3 shows that the reference voltages are closely tracked at steady state.

ii. *PR Controller with Lossy Reactive Components and Deadtime*

The boost inverter's simulation results with lossy reactive components, deadtime and PR controllers in the inner loop and outer loop are shown in Figure 6.10. Furthermore, Table 6-4 illustrates the comparison of the simulation output voltages and the reference output voltages. The simulation model is shown in Appendix A.3.3.

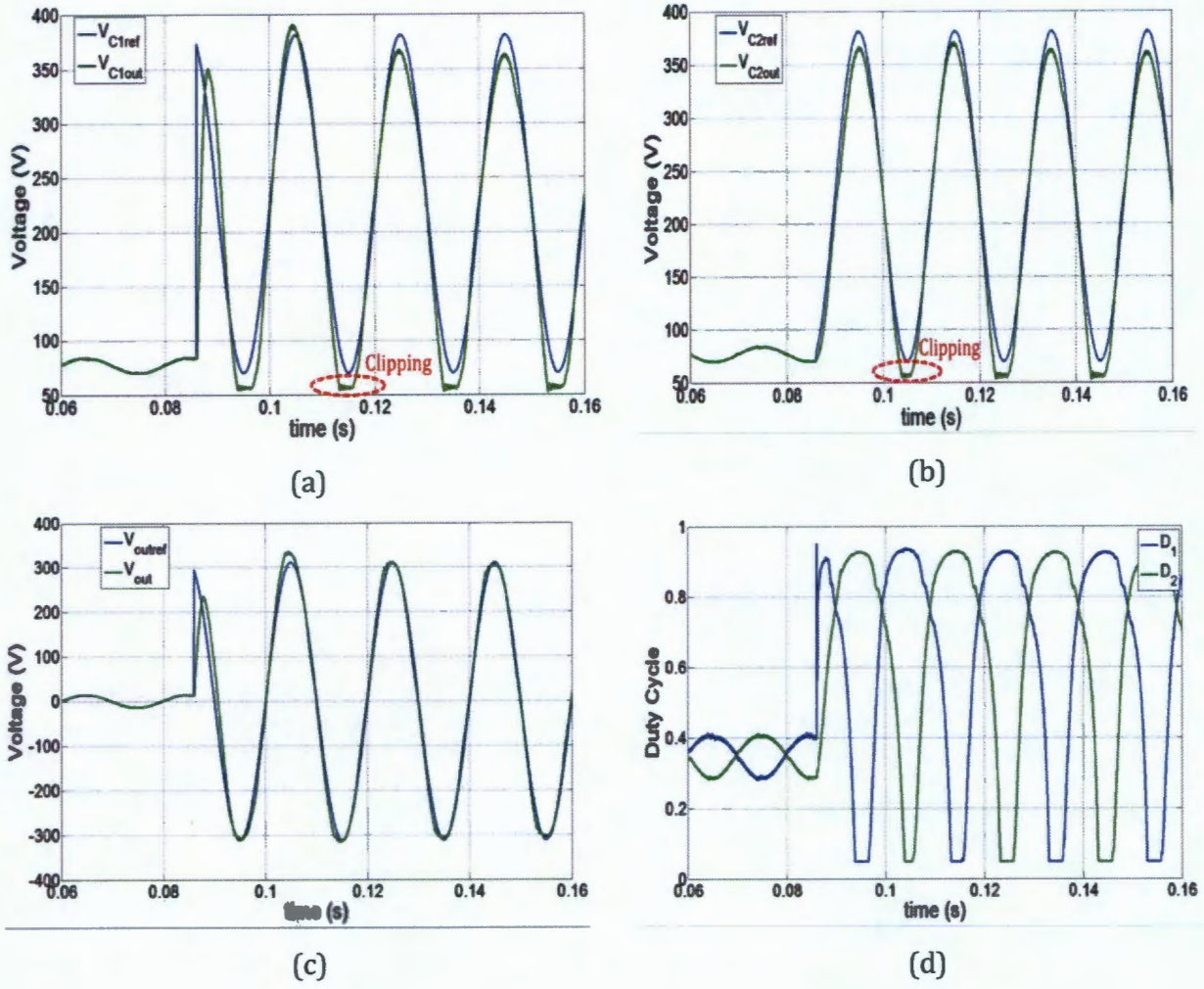


Figure 6.10: Simulation results of boost inverter, with PR controller, lossy reactive components and deadtime added, of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) voltage across load and d)duty cycle signals of both converters.

Table 6-4: : Comparison of output voltages from simulation results with their reference of boost inverter with PR controller, lossy reactive components and deadtime added.

Output Voltage	$V_{DC\,SIM}$ [V] ($V_{DC\,Ref}$[V])	$V_{50Hz\,SIM}$ [V_{RMS}] ($V_{50Hz\,Ref}$[V_{RMS}])
V_{C1}	209.94 (225)	110.12 (110)
V_{C2}	210.10 (225.)	110.01 (110)
V_{out}	-0.17 (0)	220.32 (220)

The output voltage's (Figure 6.9 (a)–(c)) transients also decay within a period of the fundamental voltage as in section 6.2.1i. Table 6-3 illustrates that the fundamental components of the reference voltages are also closely tracked. However, the dc component of

the boost converter's reference voltages was not closely tracked at steady state. Thus, a clipping effect is seen on the output voltages of the boost converters. A small dc component is also seen in the boost inverters output voltage.

6.2.2 *PIR Controller Simulations*

The PIR controller is used in the outer loop and the inner loop uses the PR controller as discussed in section 4.6.2 . The simulation results of this control configuration are shown in Figure 6.11. The boost inverter model used contains lossy reactive components and deadtime. Moreover, the comparison of the simulation output voltages and the reference output voltages is illustrated in Table 6-5. The simulation model can also be found in Appendix A.3.3.

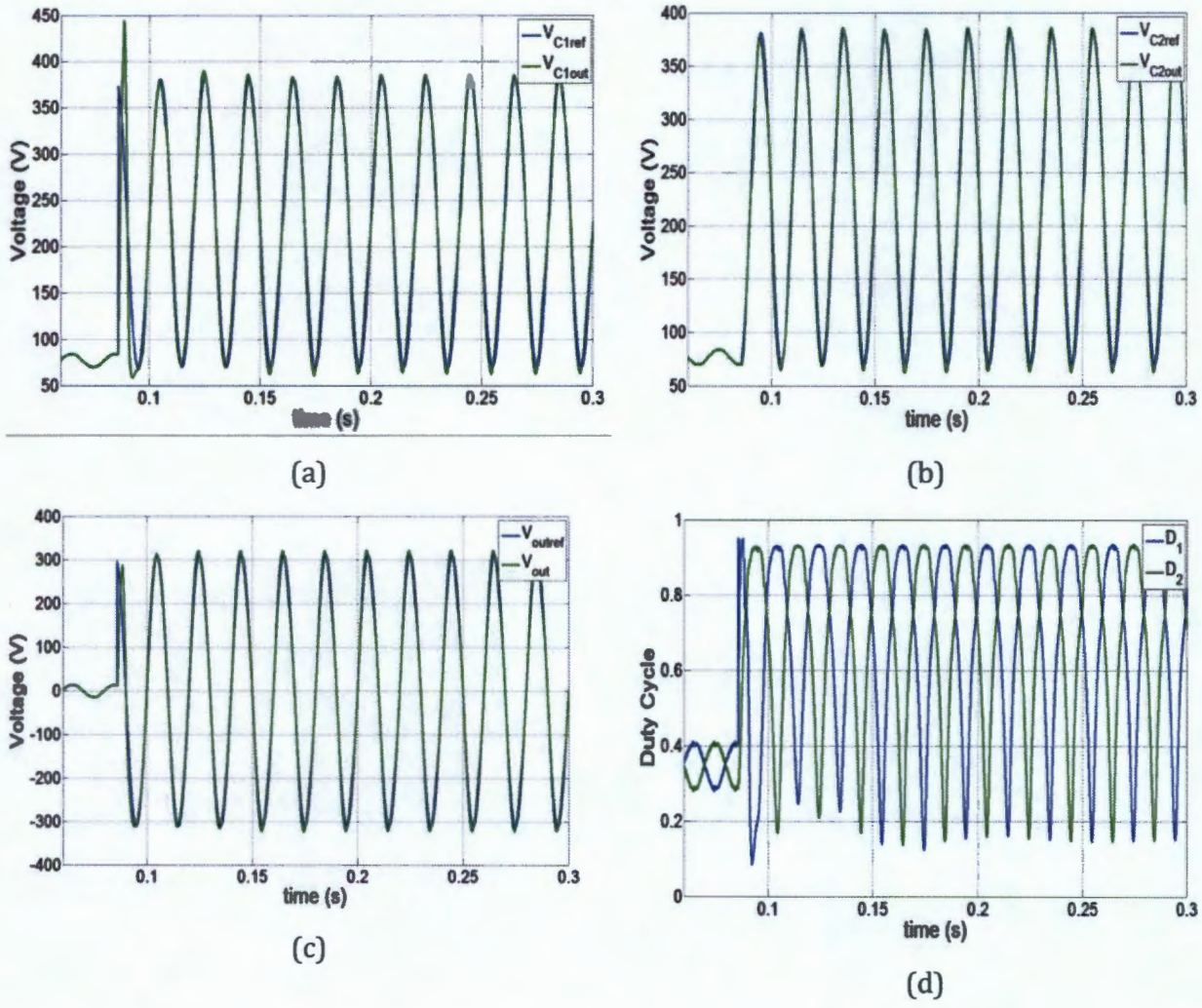


Figure 6.11: Simulation results of boost inverter with PIR controller, lossy reactive components and deadtime added, of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) inductor current and d) duty cycle signals of both converter and e) voltage across load.

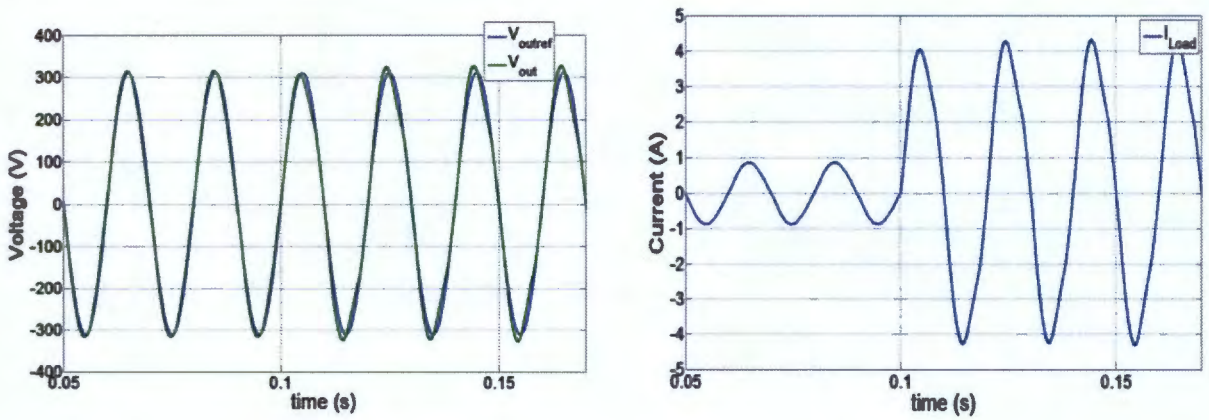
Table 6-5: : Comparison of output voltages from simulation results with ideal results of boost inverter with PR controller, lossy reactive components and deadtime added.

Output Voltage	$V_{DC\,SIM}$ [V] ($V_{DC\,Ideal}$[V])	$V_{50Hz\,SIM}$ [V_{RMS}] ($V_{50Hz\,Ideal}$[V_{RMS}])
V_{C1}	225.40(225)	110.00 (110)
V_{C2}	225.24 (225)	110.03 (110)
V_{out}	0.16 (0)	220.03 (220)

The transients of the output voltages, Figure 6.9 (a)–(c), also decay within a period of the fundamental voltage. Table 6-3 shows that the reference voltages are closely tracked at steady state. Thus, no clipping effect is seen on the output voltages of the boost converters. However, a small dc component still exists on V_{out}. Therefore, the PIR controller is used for the remaining simulation results that determine the performance of the boost inverter when it experiences disturbances.

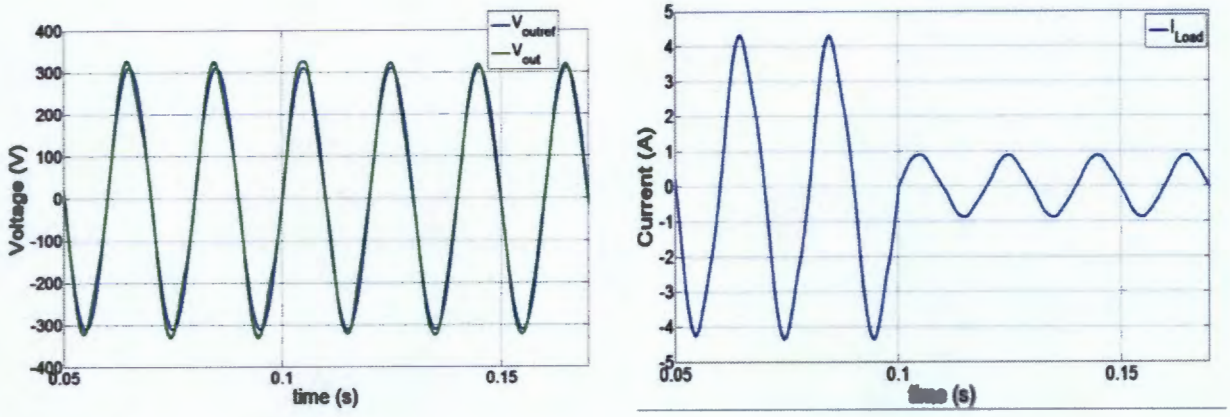
6.3 Linear Load Disturbance Simulations

The load disturbance is simulated as a sudden connection and disconnection of 76Ω to the boost inverter's output, which has a 366Ω load. The simulation model is shown in Appendix A.3.4. The simulation results of the connection and disconnection 76Ω are shown in Figure 6.12 and Figure 6.13, respectively. The output voltage waveform shows that the control strategy achieves load disturbance rejection with minimal variation in the output voltage magnitude variation.



(a) (b)

Figure 6.12: Simulation results of sudden connection of 76Ω to boost inverter output.

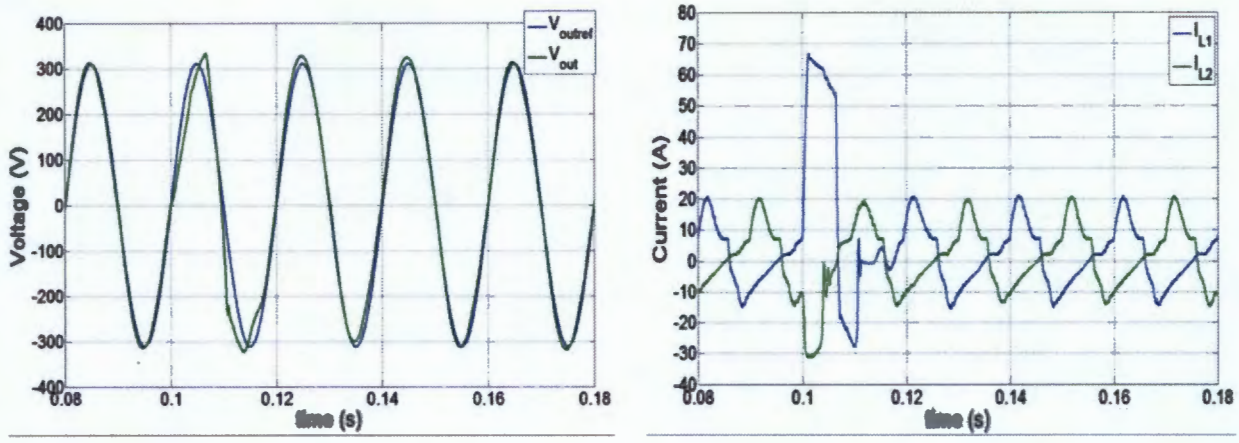


(a) (b)

Figure 6.13: Simulation results of sudden disconnection of 76Ω to boost inverter output.

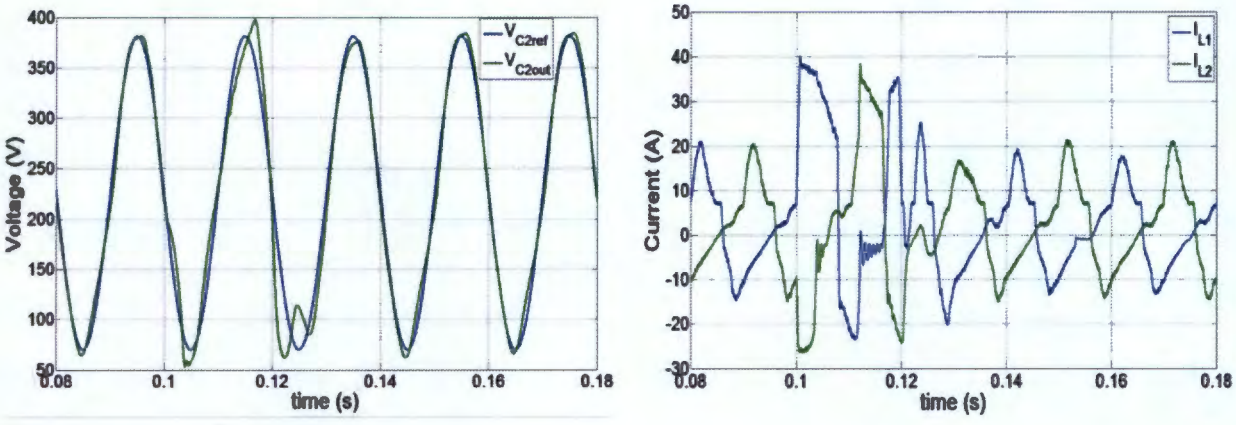
6.4 Inrush Current Simulation

The inrush current handling capability of the boost inverter is simulated by connecting the output of the boost inverter to a full bridge rectifier, which is connected to 125μF. The boost inverter output is also connected to a 400Ω linear load in parallel to the rectifier system. The simulation model is shown in Appendix A.3.5. Since inrush currents are high, the IGBTs have to be protected by limiting the inductor current. Furthermore, the protection distorts the output voltage and the distortion depends on the limit values. Thus, there are two sets of simulation results for two different upper and lower limits of the inductor current. The two sets of upper and lower limits are: 70A and -30A, respectively; 40A and -25A, respectively. The simulation results of the first and second limits are shown in Figure 6.14 and Figure 6.15, respectively.



(a) (b)

Figure 6.14: Simulation results of inrush current with inductor current limited between 70A and -30A.



(a) (b)

Figure 6.15: Simulation results of inrush current with inductor current limited between 40A and -25A.

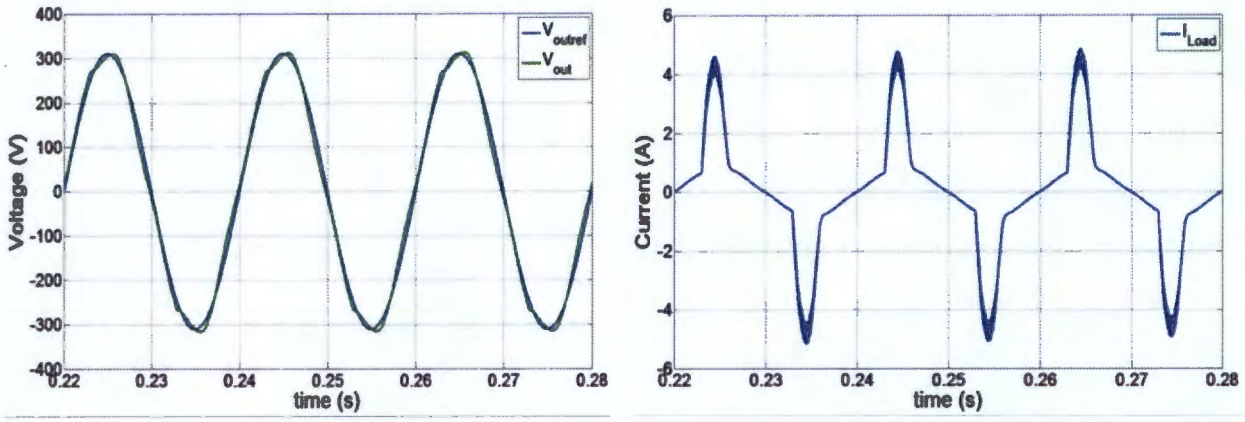
The inductor current is limited to the specified values. However, the output voltage becomes distorted when the inner loop limits the current. Furthermore, the distortion in the output voltage waveform increases as the limit magnitudes are decreased as seen in Figure 6.15. Nevertheless, the output voltage returns to normal steady state operation once the inrush current has decayed. The limits that were selected for the simulation model are the 70 A and -30 A because there is less distortion.

6.5 Nonlinear Load Simulations

The simulation model used for the nonlinear load simulation is the same as the inrush current model with an addition of a 375 Ω load connected on the output of the full bridge rectifier. The simulation model is shown in Appendix A.3.6. The steady state operation simulation results are shown in Figure 6.16 and Table 6-6 shows the comparison between the simulation output voltage and reference output voltage.

Table 6-6: : Comparison of output voltage from simulation results with ideal values of boost inverter with nonlinear load disturbance.

Output Voltage	$V_{DC\,SIM}\,[V]$ ($V_{DC\,REF}[V]$)	$V_{50Hz\,SIM}\,[V_{RMS}]$ ($V_{50Hz\,REF}[V_{RMS}]$)
V_{out}	0.12	220.20 (220)



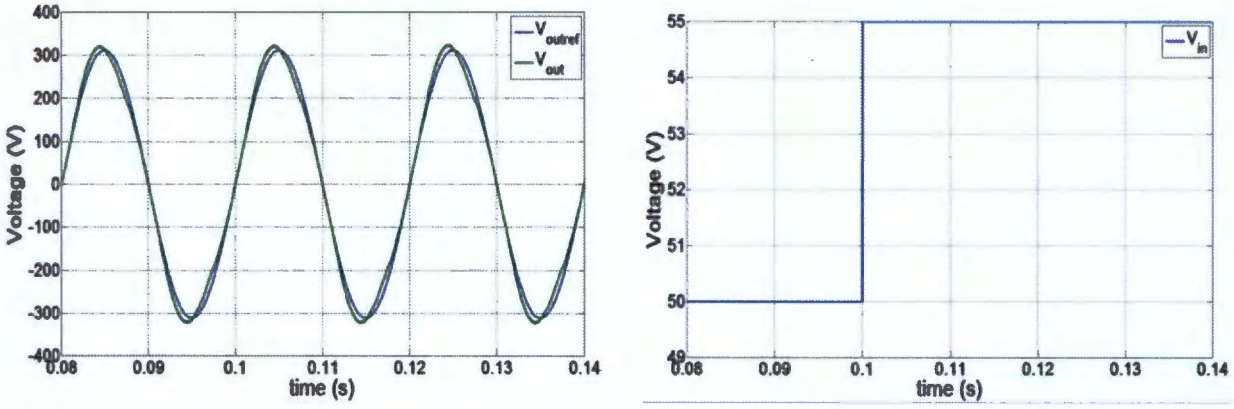
(a) (b)

Figure 6.16: Simulation results of nonlinear load disturbance performance of the boost inverter.

From Table 6-6, the reference output voltage is closely tracked and the THD is 4.80%. However, the output voltage is distorted around the peak magnitude of the output voltage, as illustrated in Figure 6.16 (a).

6.6 Input Voltage Disturbance Simulations

A controlled voltage source is used to simulate an input voltage disturbance. The voltage is stepped up from 50V to 55V. The boost inverter is connected to 100 Ω. The simulation model is shown in Appendix A.3.7. The simulation results are shown in Figure 6.17. It can be seen that the control system compensates for the input voltage disturbance and the output voltage closely tracks its reference.



(a) (b)

Figure 6.17: Simulation results of input voltage disturbance performance of the boost inverter.

7. Experimental Results and Discussions

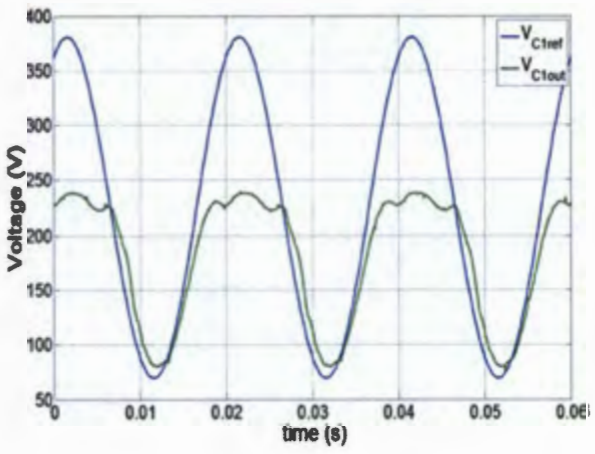
The experimental results and discussions are covered in this section. The experimental results demonstrate the open loop response, closed loop response, various disturbance rejection performances with system parameters that are similar to the simulation models. Furthermore, the THD and efficiency of the boost inverter system is covered.

7.1 Open Loop Response Results

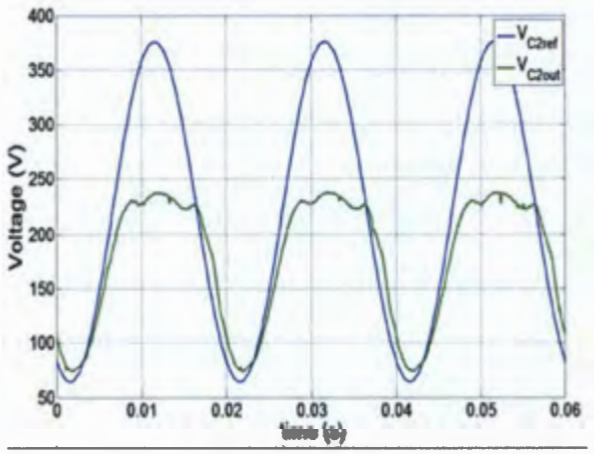
The open loop response of the boost inverter system is presented in this subsection. Furthermore, the switching technique that each boost converter undergoes is presented.

7.1.1 Boost Inverter System Open Loop Response

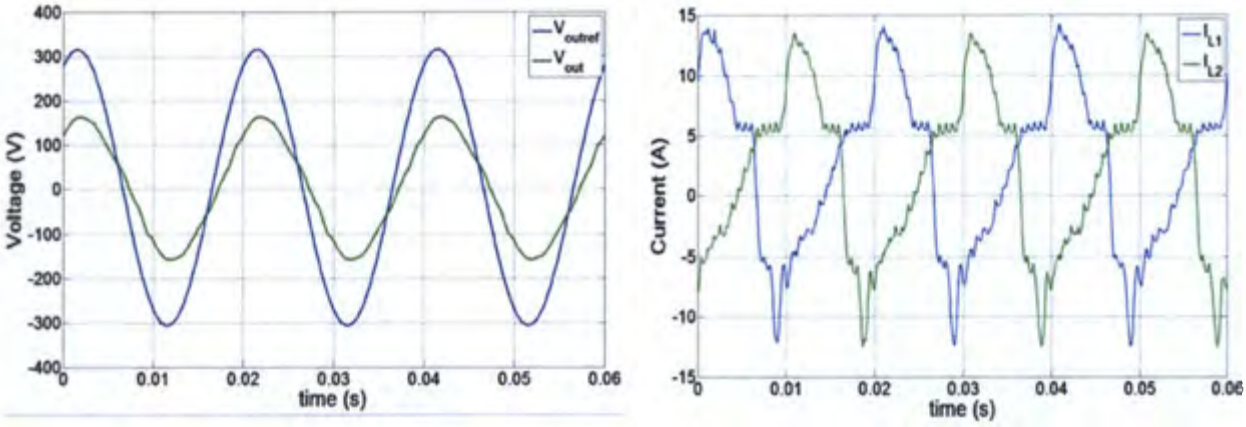
The voltage and current waveforms are shown in Figure 7.1 and the dc and fundamental output voltage magnitudes of the boost inverter's experimental results are compared with the ideal magnitudes in Table 7-1.



(a)



(b)



(c) (d)

Figure 7.1: Experimental results of open loop boost inverter of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) voltage across load inductor current and d) inductor currents.

Table 7-1: : Comparison of output voltages from experimental results with ideal results of open loop boost inverter.

Output Voltage	$V_{DC\ EXP}$ $[V]$ ($V_{DC\ Ideal}[V]$)	$V_{50Hz\ EXP}$ $[V_{RMS}]$ ($V_{50Hz\ Ideal}[V_{RMS}]$)
V_{C1}	180.45 (225)	54.02 (110)
V_{C2}	177.46 (225)	56.2 (110)
V_{out}	3 (0)	110.04 (220)

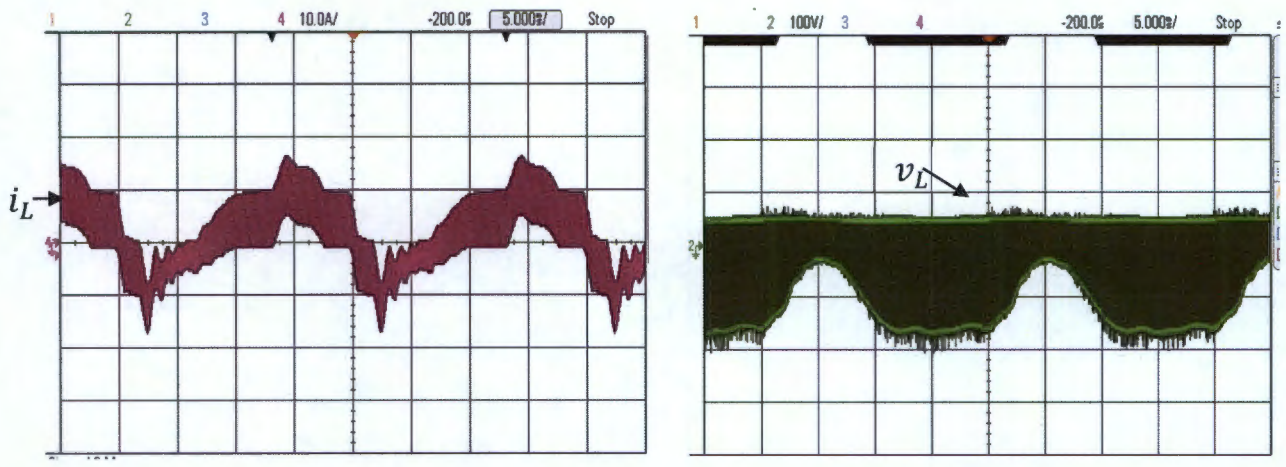
From Table 7-1, boost converter 1 varies from the ideal dc and fundamental voltage component by 44.5 V and 55.98 V, respectively, and boost converter 2 varies from the ideal dc and fundamental voltage component by 47.54 V and 53.8V, respectively. Thus, the dc and fundamental voltage components of each boost converter are not close to ideal voltages. Furthermore, the simulation result's dc and fundamental voltage components (195.8 V and 67.3 V, respectively) of the boost converters were also not close to the ideal voltages. The difference between the output voltages of the simulation and experimental results are caused by not accounting for all the experimental parameters. These experimental model parameters include: conduction losses and switching characteristics of the switching devices; skin effect losses, hysteresis and eddy current losses of the inductor.

The simulated boost converters showed output voltage differences of less than 0.02 V between each other. The boost converters in the simulation model are modelled with

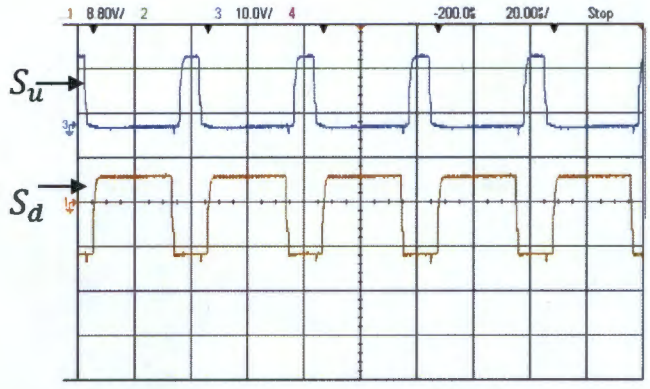
equivalent components. Therefore, the boost converters have almost identical output voltages. However, the experimental boost converters from Table 7-1 differ by more than 2 V. Therefore, the experimental boost converters have a much higher output voltages difference between each other. This is due to the difference of the experimental model parameters in each boost converter because of the mismatch between lengths of wires and components that are not manufactured and designed exactly the same. The mismatch of the experimental system led to a 3V dc voltage component in the output voltage (V_{out}) of the boost inverter. Moreover, the fundamental output voltage varied by 109.96 V from the ideal fundamental voltage. Thus, the dc and fundamental voltage component of the boost inverter's output voltage is not close to the ideal magnitude. The simulation result's fundamental component of V_{out} (134.94 V) was also not close to the ideal voltage. The THD of V_{out} is 4.82%, which is lower than the simulation results (6.76%).

7.1.2 *Switching Technique Mode Experimental Results*

The boost converter's switching techniques throughout the period of the inductor current are presented in this section. The instantaneous current, inductor voltage and switching waveforms are shown in Figure 7.2.



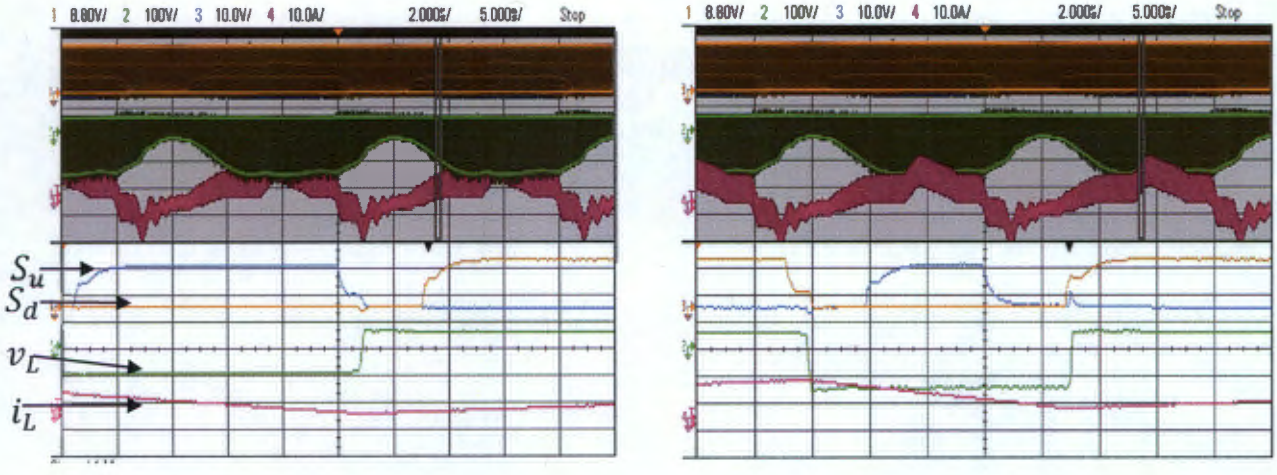
(a) (b)



(c)

Figure 7.2: Experimental results of instantaneous (a) inductor current, (b) inductor voltage and (c) gate switching waveforms for boost converter 1.

The switching techniques are shown by zooming in different regions of the inductor voltage and switching waveforms. The hard-switching; ZVRT; transition between ZVRT and hard-switching; resonance between the inductor and parasitic capacitance of the IGBT is shown in Figure 7.3(a), Figure 7.3(b), Figure 7.4(a) and Figure 7.4(b), respectively.



(a) (b)

Figure 7.3: Experimental results of (a) ZVRT and (b) hard-switching with zoomed-in instantaneous inductor voltage and current, and gate switching signals S_d and S_u.

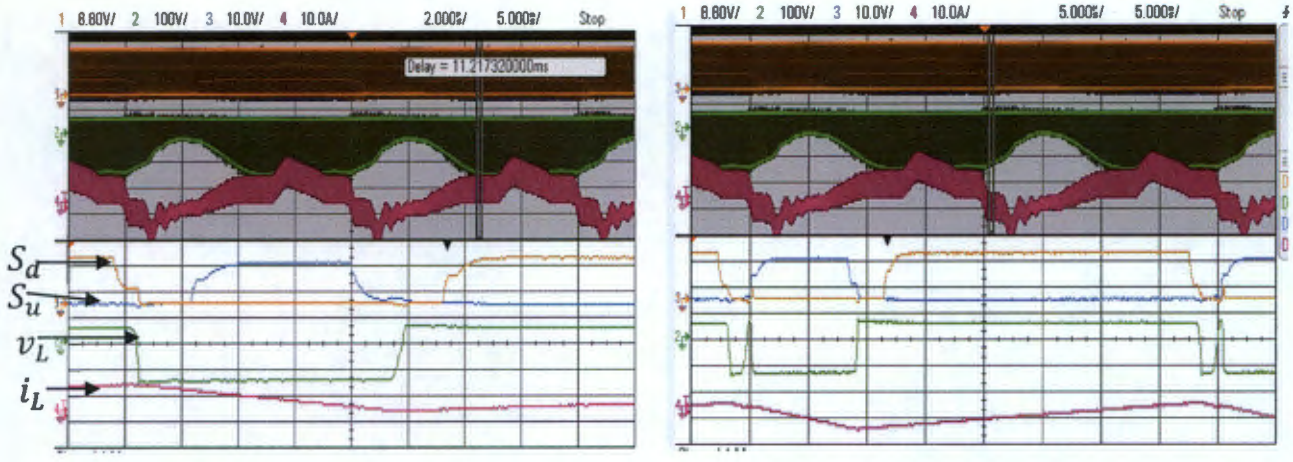


Figure 7.4: Experimental results of (a) transition between ZVRT and hard-switching and (b) resonance between inductor and parasitic capacitance with zoomed-in instantaneous inductor voltage and current, and gate switching signals S_d and S_u.

The ZVRT and hard-switching switching technique depend on the inductor current ripple as discussed in section 4.3. The resonance between the inductor and parasitic capacitance of the IGBT is caused by the deadtime as discussed in section 4.4.3. Furthermore, the hard-switching, resonance and transition between ZVRT and hard-switching cause the voltage distortion of the boost converter's output voltage and reduce the magnitude.

7.2 Closed Loop Response Results

The closed loop simulations show the performance of the PR and PIR controllers with the control parameters determined in section 5.8.

7.2.1 PR controller

The closed loop response experimental results, with PR controllers, are shown in Figure 7.5. Furthermore, Table 7-2 shows the comparison of the experimental output voltages and the reference output voltages.

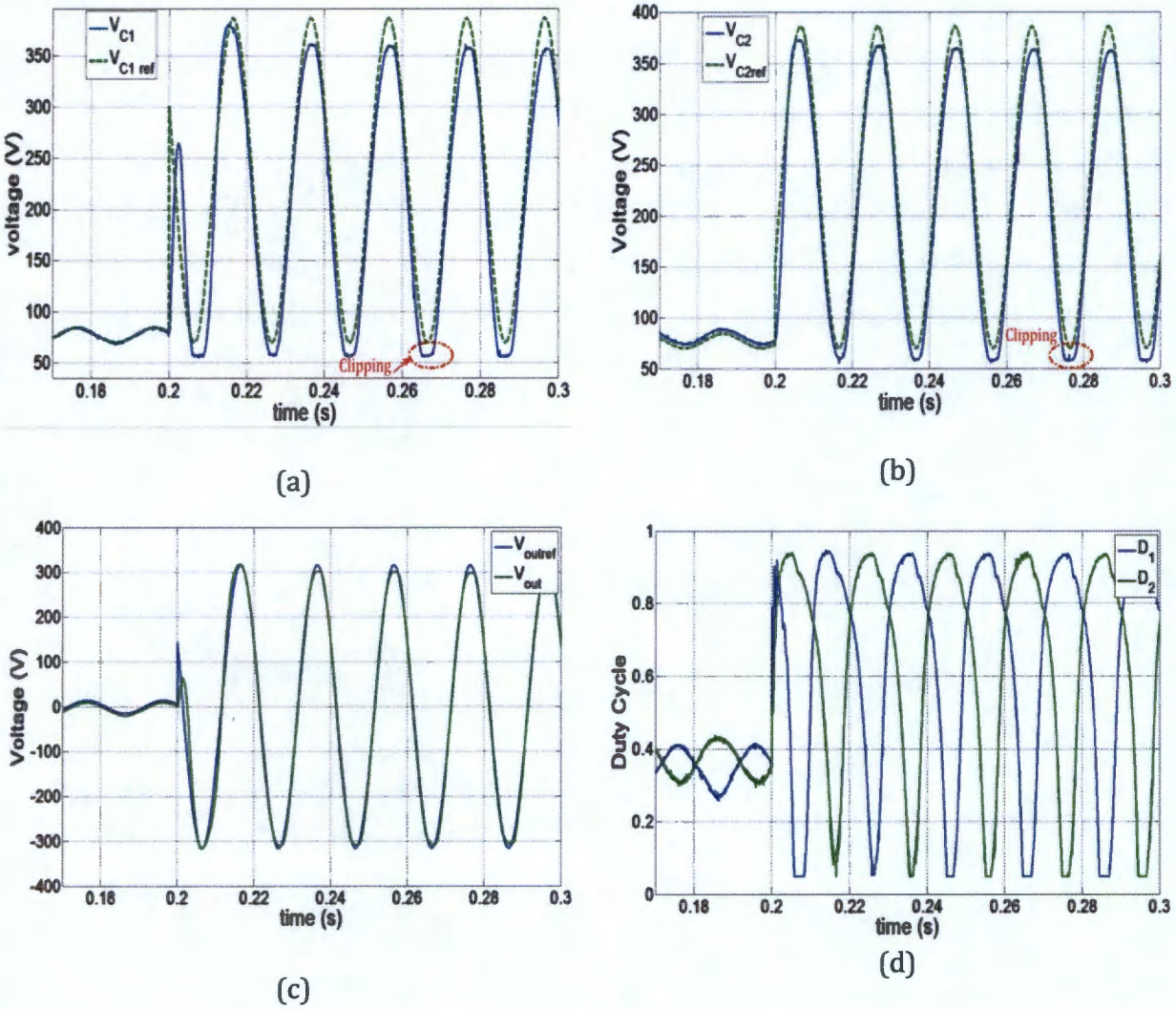


Figure 7.5: Experimental results of boost inverter with PR controller of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) voltage across load and d)duty cycle signals of both converter.

Table 7-2: Comparison of output voltages from experimental results with ideal (reference) results of boost inverter with PR controller and lossy reactive components.

Output Voltage	$V_{DC\ EXP}\ [V]$ ($V_{DC\ Ref}[V]$)	$V_{50Hz\ EXP}\ [V_{RMS}]$ ($V_{50Hz\ Ref}[V_{RMS}]$)
V_{C1}	195.99 (225)	110.14 (110)
V_{C2}	198.30 (225)	109.78 (110)
V_{out}	-2.31 (0)	219.93 (220)

The transients of the output voltages, Figure 7.5 (a) – (b), decay within a period of the fundamental voltage, as in the simulation results in section 6.2.1ii. Table 7-2 illustrates that boost converter 1 and boost converter 2 results differ from the reference dc voltage component by 29.01 V and 26.7 V, respectively; and differ from the reference fundamental

voltage component by 0.14 V and 0.22 V, respectively. Thus, the dc voltage component of each boost converter is not close to the reference dc voltage component and a clipping effect is observed on the output voltages of the boost converters. However, the fundamental voltage component of each boost converter is close to the reference fundamental voltage component. The performance of the experimental boost converters was similar to the simulation model results. The simulation model results of the dc and fundamental voltage components of boost converter 1 (206.74 V and 110.03, respectively) and boost converter 2 (206.76 V and 110.15 V, respectively) are not exactly equivalent to the experimental results. The difference is brought about by not accounting for experimental parameters, as discussed in section 7.1.1.

The dc voltage component of the boost inverter's output voltage (2.31 V) is not close to the reference magnitude (0 V) and hence a dc current exists. However, the fundamental output voltage is close to the reference fundamental voltage component because the difference between the magnitudes is 0.07 V. On the other hand, the simulation model results of both the dc and fundamental output voltage of the boost inverter closely matched the reference output voltage. The dc voltage component of V_{out} in the experimental setup is caused by the mismatch of the experimental model parameters between the boost converters.

The PR controller does not closely track the dc component of the reference of each boost converter because the deadtime introduces a dc disturbance, which the control system cannot compensate. It was shown in section 4.6.2 that the dc disturbance would be amplified if the proportional gain k_P was less than zero. This was the case due to the low bandwidth as shown in section 5.8.3.

7.2.2 PIR controller

The experimental results of the PIR controller implemented in the outer loop and PR controller implemented in the inner are shown in Figure 7.6. The comparison of the experimental output voltages and the reference output voltages is illustrated in Table 7-3.

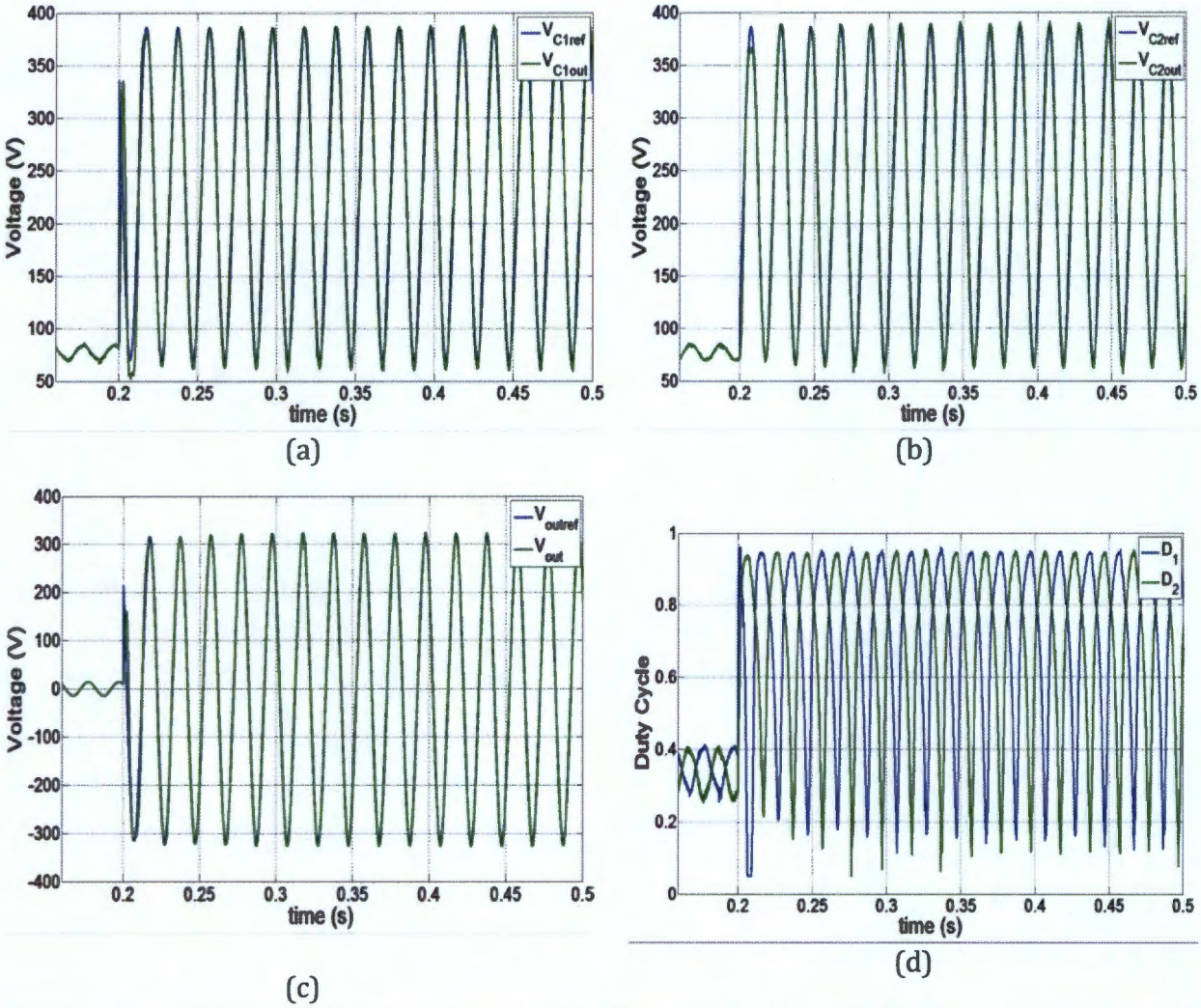


Figure 7.6: Experimental results of boost inverter with PIR controller of a) boost converter 1 output voltage, b) boost converter 2 output voltage, c) voltage across load.and d)duty cycle signals of both converter.

Table 7-3: : Comparison of output voltages from experimental results with ideal (reference) results of boost inverter with PIR controller.

Output Voltage	$V_{DC\,SIM}$ $[V]$ ($V_{DC\,Ref}[V]$)	$V_{50Hz\,SIM}$ $[V_{RMS}]$ ($V_{50Hz\,Ref}[V_{RMS}]$)
V_{C1}	225.24 (225)	110.31 (110)
V_{C2}	225.06 (225)	109.74 (110)
V_{out}	0.18	220.05 (220)

The boost inverter's transient output voltages, Figure 7.6(a) – (b), also decay within a period of the fundamental voltage as in section 7.2.2. From Table 7-3, boost converter 1 and boost converter 2 varies from the ideal dc voltage component by 0.24 V and 0.06 V, respectively. Furthermore, boost converter 1 and boost converter 2 varies from the reference the

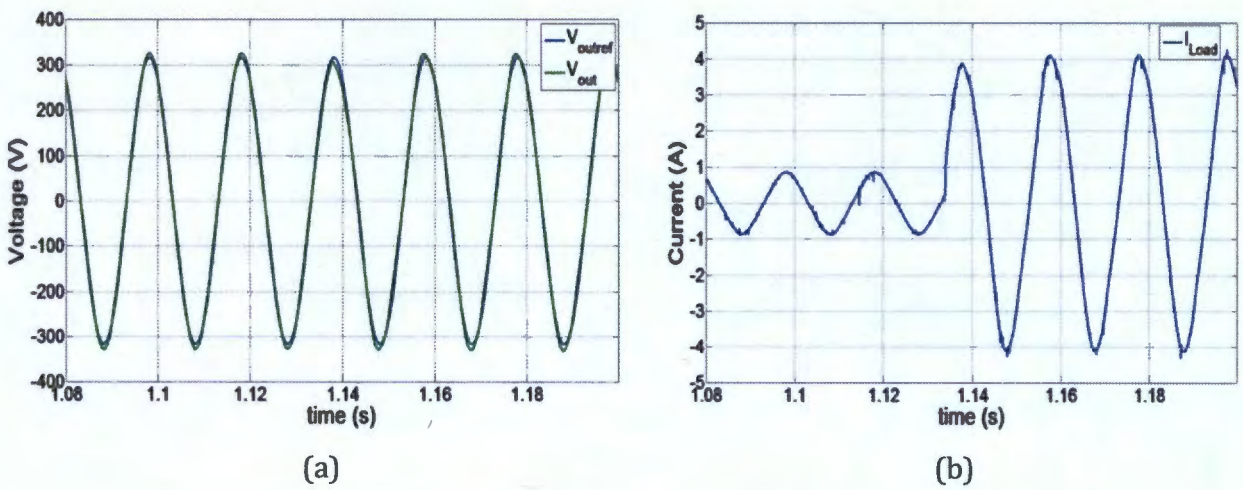
fundamental voltage component by 0.31 V and 0.26 V, respectively. Thus, the dc and fundamental voltage component of each boost converter is close to the ideal magnitude. The performance of the experimental boost converters was similar to the simulation model results. Furthermore, the simulation model results of the dc and fundamental voltage components of boost converter 1 (225.40 V and 110.00, respectively) and boost converter 2 (225.24 V and 110.03 V, respectively) are very close to the experimental results shown in Table 7-3.

The dc voltage component of the output voltage for the boost inverter varies from the ideal dc voltage component by 0.18 V. Furthermore, the fundamental output voltage varies from the ideal fundamental voltage component by 0.05 V. Thus, the dc and fundamental voltage components of the boost inverter's output voltage are close to the ideal magnitude. The dc component of V_{out} is lower than the in the previous results of the PR controller.

The PIR controller closely tracks the dc and fundamental component of the reference for each boost converter. The dc disturbance introduced by the deadtime was reduced by introducing the integral term, as was shown in section 4.6.2. The PIR controller is used in the forthcoming experimental results.

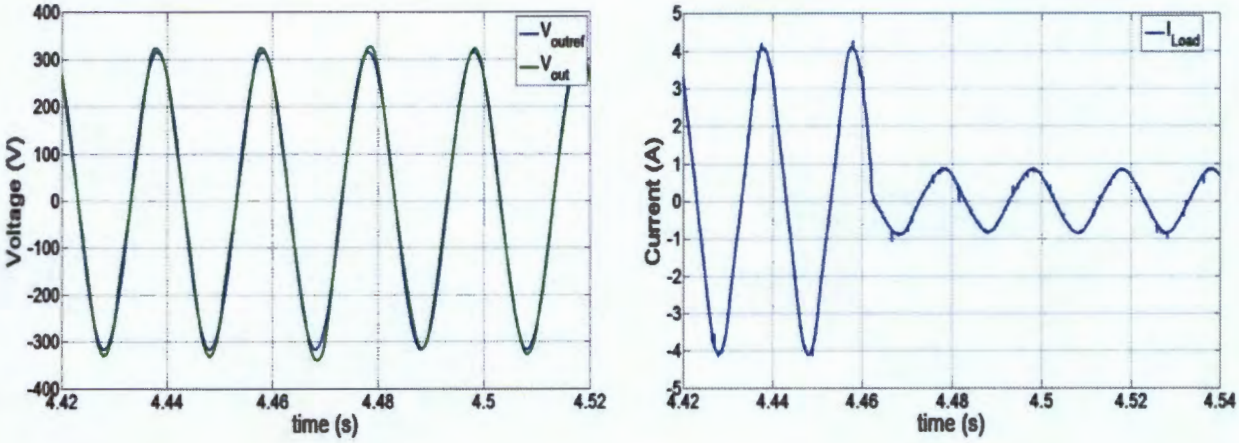
7.3 Load Disturbance

The experimental load disturbance results of sudden load connection and disconnection are shown in Figure 7.7 and Figure 7.8, respectively.



(a) (b)

Figure 7.7: Experimental results of sudden connection of 76Ω to boost inverter output.



(a) (b)

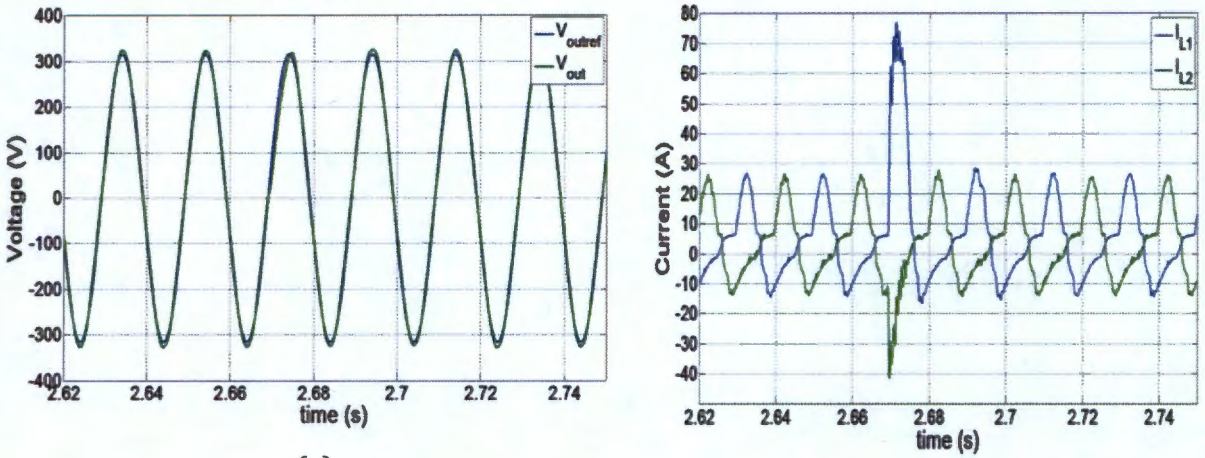
Figure 7.8: Experimental results of sudden disconnection of 76Ω to boost inverter output.

The control system rejects the load disturbance with minor deviation from the reference when the load is connected or disconnected. This performance is similar to the simulation model results in section 6.3.

The load disturbance rejection performance seen in Figure 7.7 and Figure 7.8, was due to the feed-forward control strategy. The feed-forward scheme directly measures the output current and compensates for disturbances introduced as explained in section 4.6.1. The small magnitude variation of the output voltage is caused by the mismatch between the measured and actual output current. The mismatch of the output currents is due to the filter on the measured current and ADC's quantization.

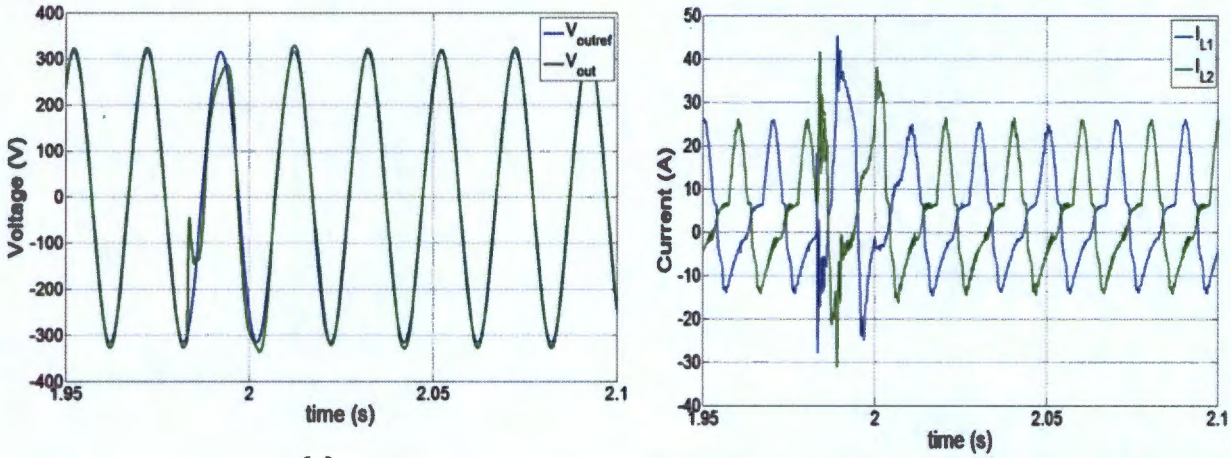
7.4 Inrush Current

The inrush current handling capability experimental results consist of two sets of results, shown in Figure 7.9 and Figure 7.10, where the limits of the inductor current are varied as in the simulation model in section 6.4.



(a) (b)

Figure 7.9: Experimental results of inrush current with inductor current limited between 70A and -30A.



(a) (b)

Figure 7.10: Experimental results of inrush current with inductor current limited between 40A and -25A.

Figure 7.9 (b) and Figure 7.10 (b) illustrate that the control system limits the inductor currents to the desired upper and lower levels, namely: 70A and -30A, respectively; 40A and -25A, respectively. As in the simulation results in section 6.4, the output voltage becomes distorted when the inductor current loop limits the current. Moreover, the distortion in the output voltage waveform increases as the inductor current limit magnitudes are decreased.

The sudden connection of the rectifier with the capacitor load represents a transient short circuit. This is due to the capacitor charging up. Once the capacitor was charged the boost inverter's output voltge control resumes to its steady state operation [46]. The distortion of the output voltage occurs because the boost inverter acts as a current source when the inductor current is limited [24]. This behaviour causes the output voltage to change to

whichever value that will provide the commanded limited inductor current. Therefore, the distortion worsens when the limits are low because a lower voltage is required to maintain the inductor current limit. Thus, 70 A and -30 A should be used to provide output voltages with low distortion.

7.5 Nonlinear load Disturbance

The steady state experimental results of the nonlinear load disturbance are shown in Figure 7.11 and Table 7-4 shows the comparison between the experimental output voltage and reference output voltage.

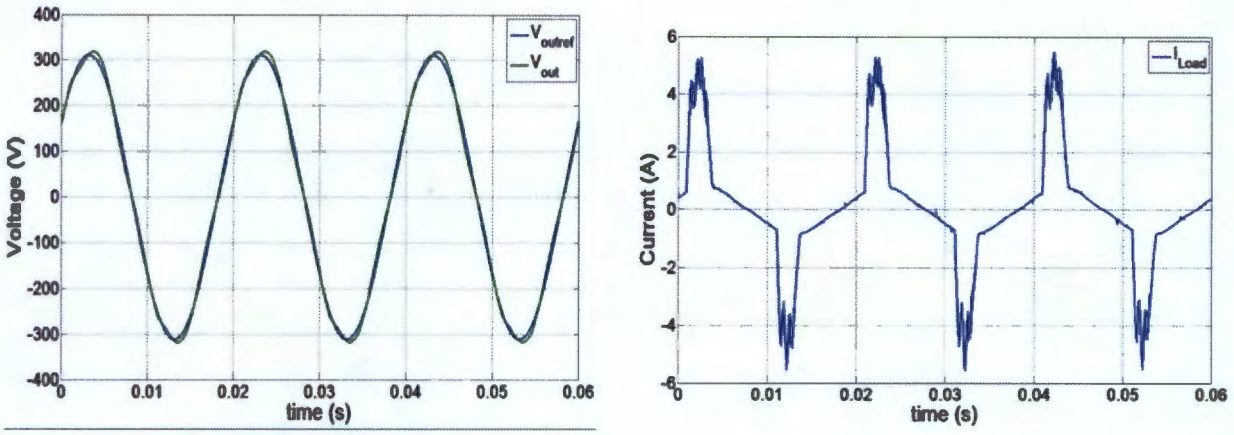


Figure 7.11: Experimental results of nonlinear load disturbance performance of the boost inverter.

Table 7-4: Comparison of output voltage from experimental results with ideal values of boost inverter with nonlinear load disturbance.

Output Voltage	$V_{DC\,EXP}$ [V] ($V_{DC\,REF}$[V])	$V_{50Hz\,EXP}$ [V_{RMS}] ($V_{50Hz\,REF}$[V_{RMS}])	THD [%]
V_{out}	0.02 (0)	219.88 (220)	4.82

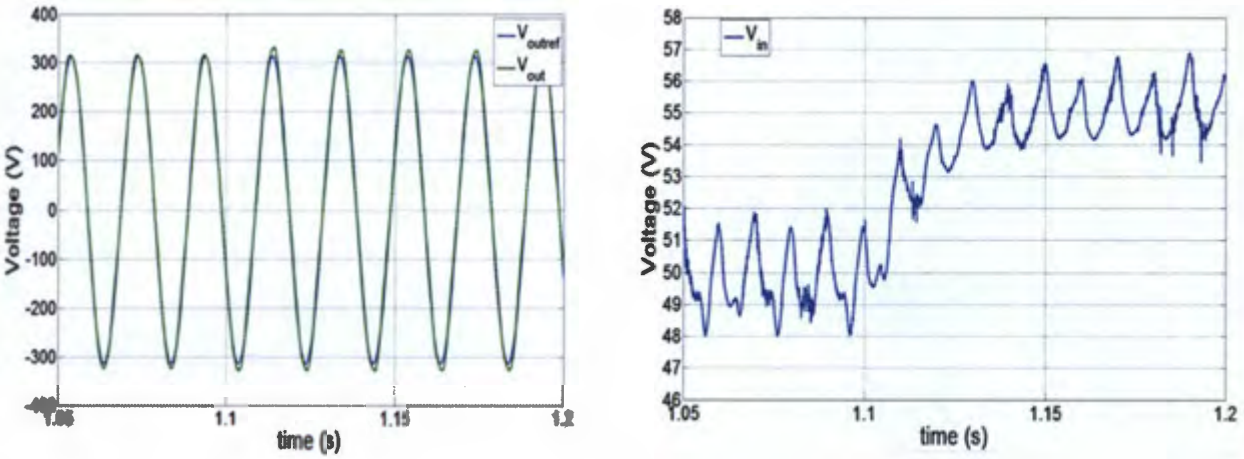
As in the simulation results, the reference output voltage is closely tracked and the experimental output voltage is distorted around the peak magnitude of the output voltage as shown in Figure 7.11 (a). The values of the output voltage from Table 7-4 are similar to the simulated values from Table 6-6.

The output voltage is distorted at the peaks because the capacitor connected on the output of the full bridge rectifier charges up. This charging current can be considered as a load

disturbance [46]. Thus, the output voltage magnitude will experience variations as discussed in section 7.3.

7.6 Input Voltage Disturbance

The input voltage disturbance experimental results are shown in Figure 7.12.



(a) (b)

Figure 7.12: Experimental results of input voltage disturbance performance of the boost inverter.

The measured input voltage, Figure 7.12 (b), contains a low frequency ripple voltage, and there is a small magnitude variation of output voltage as shown in Figure 7.12 (a). From the simulation results, in section 6.6, there was no low frequency ripple voltage input and no magnitude variation of the output voltage.

The measured ripple voltage is caused by the current that is drawn from the decoupling capacitor that was discussed in section 3.2.2, whereas, the simulation model consists of an ideal dc voltage source that did not require a decoupling capacitor. The change in input voltage, changes the reference voltage of each boost converter. Therefore, output voltage magnitude occurs due to the ADC quantization and filters.

7.7 Efficiency

The efficiency of the boost inverter was assessed by manually adjusting the dc voltage power supply voltage to give the characteristics of the fuel cell described in section 5.1. The efficiency, input voltage and current characteristics of dc voltage power supply are shown in Figure 7.13.

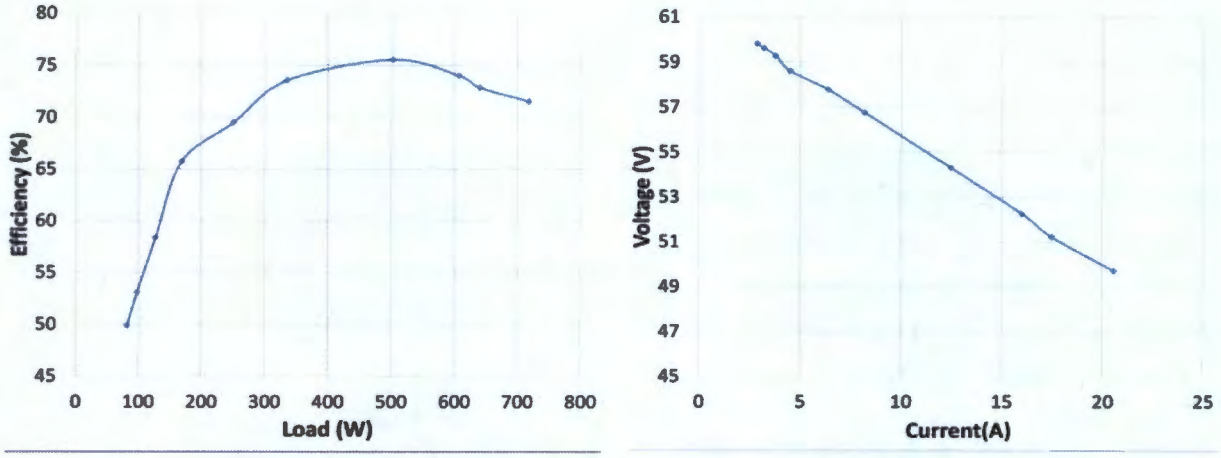


Figure 7.13: Experimental results of (a) efficiency of the boost inverter and (b) and input voltage and current characteristics of dc voltage power supply.

The peak efficiency is 75.5%. The efficiency of the boost inverter is not high due to the high series resistance of the inductor [43].The high frequency inductor ripple current also increases the switching losses.

7.8 Output Voltage Regulation and THD

The output voltage waveforms of the boost inverter were captured and saved during the efficiency tests conducted. Afterwards, the RMS and THD of the output voltage were evaluated in MATLAB. The results are shown in Figure 7.14.

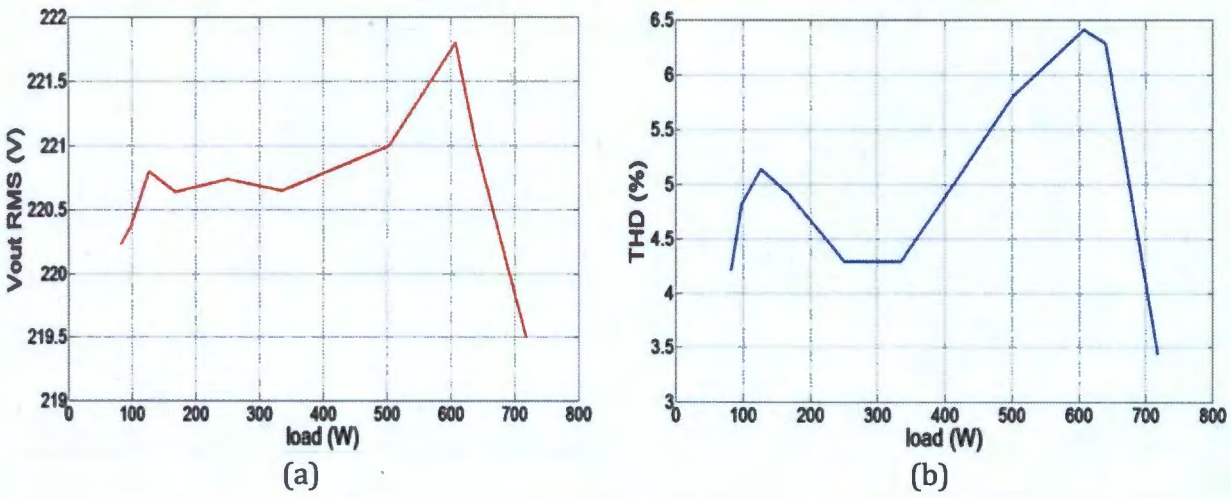


Figure 7.14: Output Voltage RMS (a) and THD (b) results of experimental boost inverter .

The highest and lowest output voltage is 221.8 V and 219.5 V, respectively. The highest and lowest THD is 6.54% and 3.41%. Therefore, the voltage regulation and THD of the boost inverter are within the EN501060's voltage regulation (±10%) and THD (<8%) limits.

8. Conclusions

The conclusions of the boost inverter are drawn in this section.

8.1 Poor Open Loop Performance

The boost inverter's open loop performance was poor because of the output voltage's high THD and low rms magnitude. This was due to the deadtime that it introduced to prevent shoot-through of switching devices. The open loop performance from the simulation model results was fairly close to the experimental set-up results.

8.2 PIR Controller Outperforms PR controller

The PIR controller outperforms the PR controller in rejecting dc disturbance rejection. The PR controller's main drawback is the significant dc voltage that it produces, which can damage sensitive loads. Thus, the PIR controller is better because it produces a less significant dc voltage. Furthermore, there is no clipping effect of the boost converters when PIR controllers are used. However, both controllers achieve good ac component tracking of the reference signal. The simulation results of the PR controller did not show a significant dc voltage because the boost converters' model parameters were exactly the same. However, the clipping effect was illustrated on the simulation model and validated on the experimental setup. Furthermore, the PIR controller simulation model results were successfully validated on the experimental setup.

8.3 Satisfactory Disturbance Rejection

The boost inverter's variation in voltage magnitude was low during linear and nonlinear disturbances because of the feed-forward scheme in the control strategy. Therefore, the linear and nonlinear load disturbance rejection performance was satisfactory. The inrush current was successfully limited by the control system. Therefore, the switching devices can be protected and saturation of the inductor can be avoided. However, other loads that are connected to the inverter, while an inrush current exists, will experience voltage interruptions. The experimental set-up results closely matched the simulation results.

8.4 THD and Voltage Regulation Satisfactory and Efficiency Unsatisfactory

The voltage regulation and THD of the boost inverter's output voltage was satisfactory because these were within the EN501060's voltage regulation (±10%) and THD (<8%) limits. The efficiency is unsatisfactory because much higher efficiency values (>90%) have been achieved in reference [43]. The low efficiency of the experimental set-up is caused by the high inductor series resistance and high current ripple.

9. Future Work

9.1 Efficiency Improvement

The inductors can be better designed by using thicker copper wires and larger magnetic materials. The inductor current ripple specification can also be reduced to achieve lower switching losses and skin effect losses. Furthermore, the deadtime of the boost inverter can be optimised to improve the THD.

9.2 Deadtime Compensation of Boost inverter

The deadtime can be compensated by monitoring the inductor current and cancelling the deadtime effect based on the switching technique each boost converter is operating under. Therefore, voltage measurement will not be required and will reduce the cost of the boost inverter. The protection of the switches can still be maintained because the inductor currents are always measured. This type of control for the boost inverter can be used for low cost applications where large output voltage variations can be tolerated.

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11. Appendices

Appendix A: MATLAB Simulink Models

The simulation type used was continuous and the ideal switches were enableed

Appendix A.1: Boost Inverter with Lossy reactive components.

The overall simulation model of the boost inverter with lossy components is shown in Figure A.1. Furthermore, the subsystems of the duty cycle generation block for each boost converter is shown in Figure A.2 and Figure A.3.

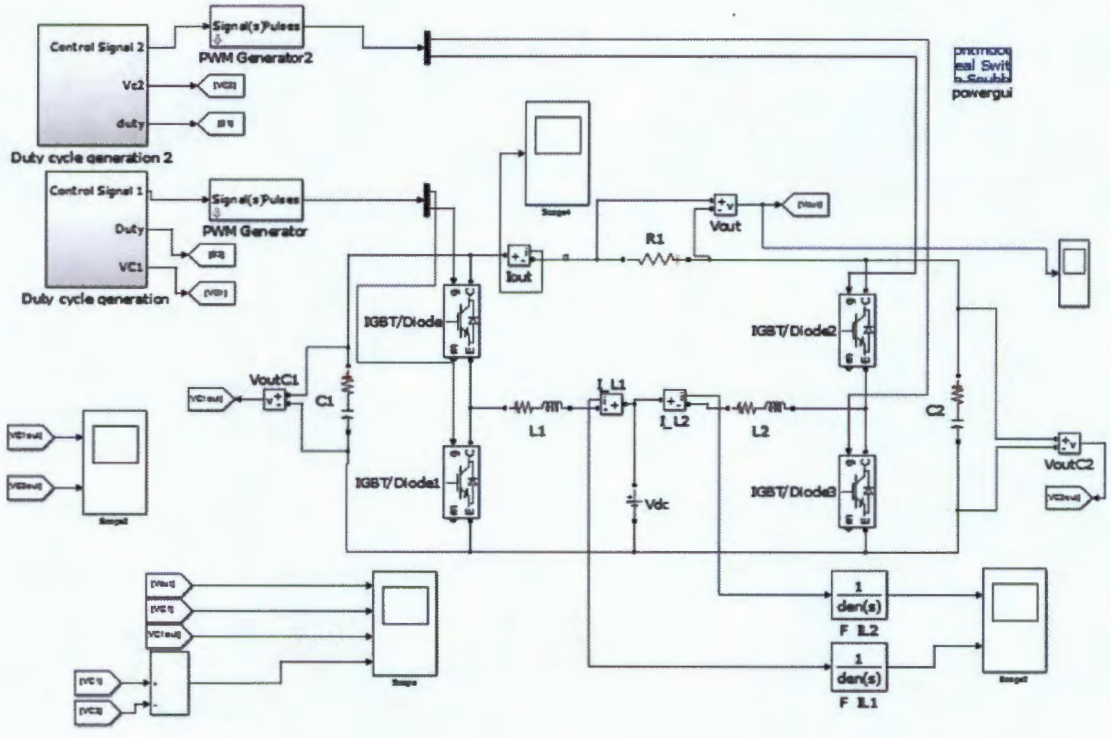

Figure A.1: Overall simulation model of boost inverter with lossy reactive components.

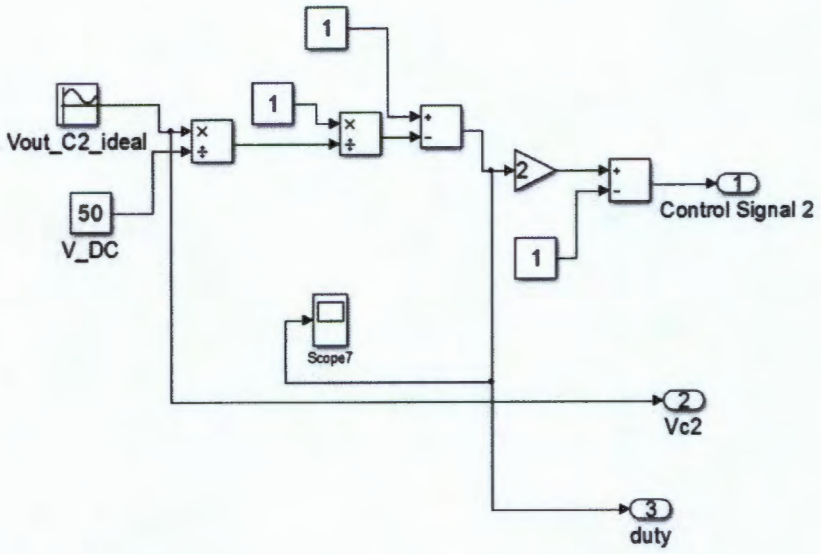

Figure A.2: Duty cycle generation 2 subsystem from overall simulation model of boost inverter with lossy reactive components.

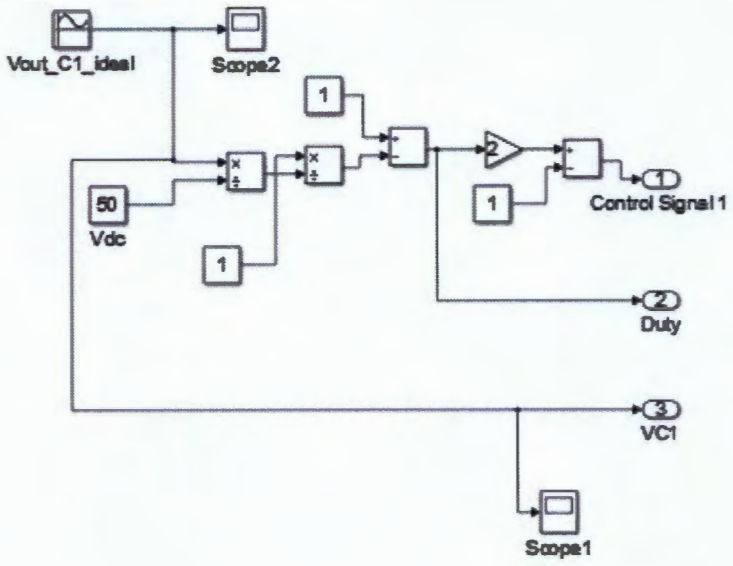

Figure A.3: Duty cycle generation subsystem from overall simulation model of boost inverter with lossy reactive components.

Appendix A.2: Boost Inverter with Lossy Reactive Components, Switching Device Sarasitic Capacitance and Deadtime.

The overall simulation model of the boost inverter with lossy reactive components, switching device parasitic capacitance and deadtime is shown in Figure A.4. The duty cycle generation blocks are the same as in Figure A.2 and Figure A.3.

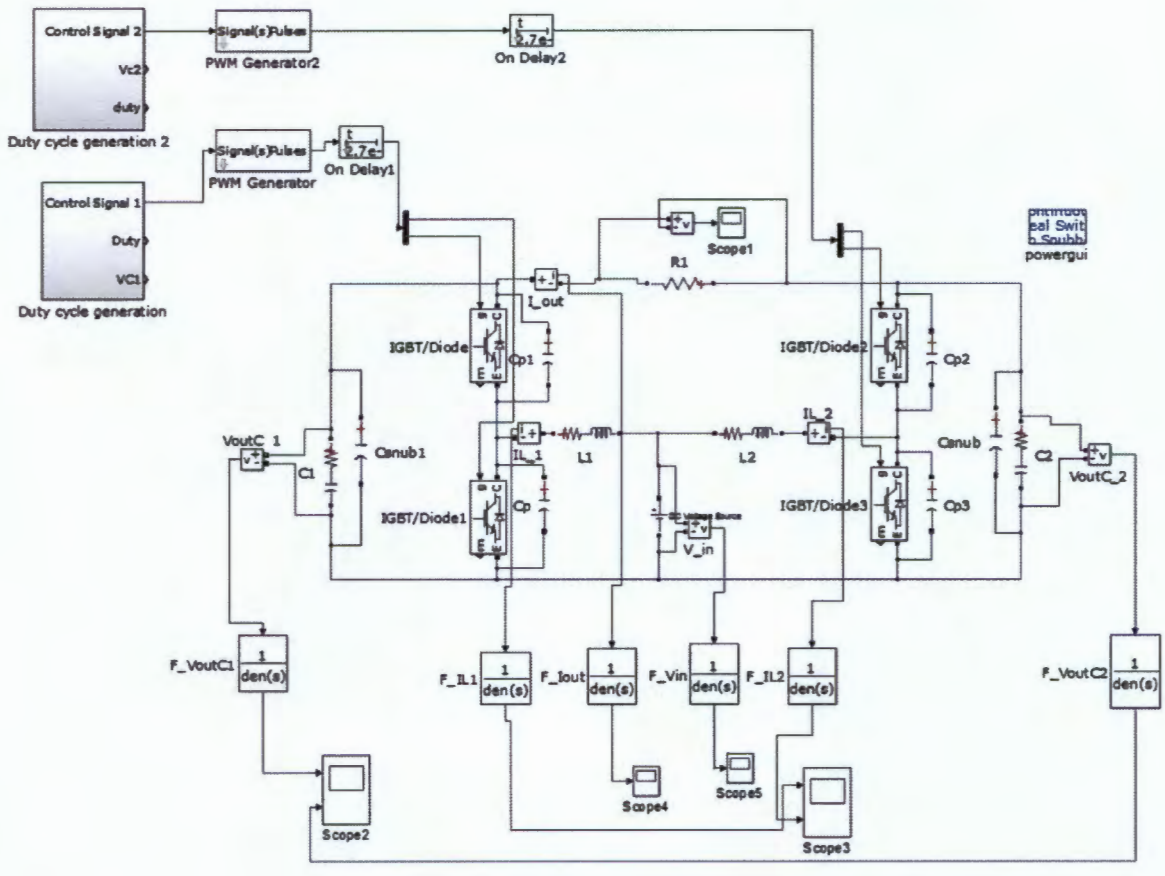

Figure A.4: Overall simulation model of boost inverter with lossy reactive components, switching device parasitic capacitance and deadtime.

Appendix A.3: Boost Inverter Closed loop Simulation models

The overall simulation model of the closed loop boost inverter system is shown in Figure A.5. The boost inverter circuit subsystem varies according to each simulation operation. The different subsystems that were simulated are described in this section.

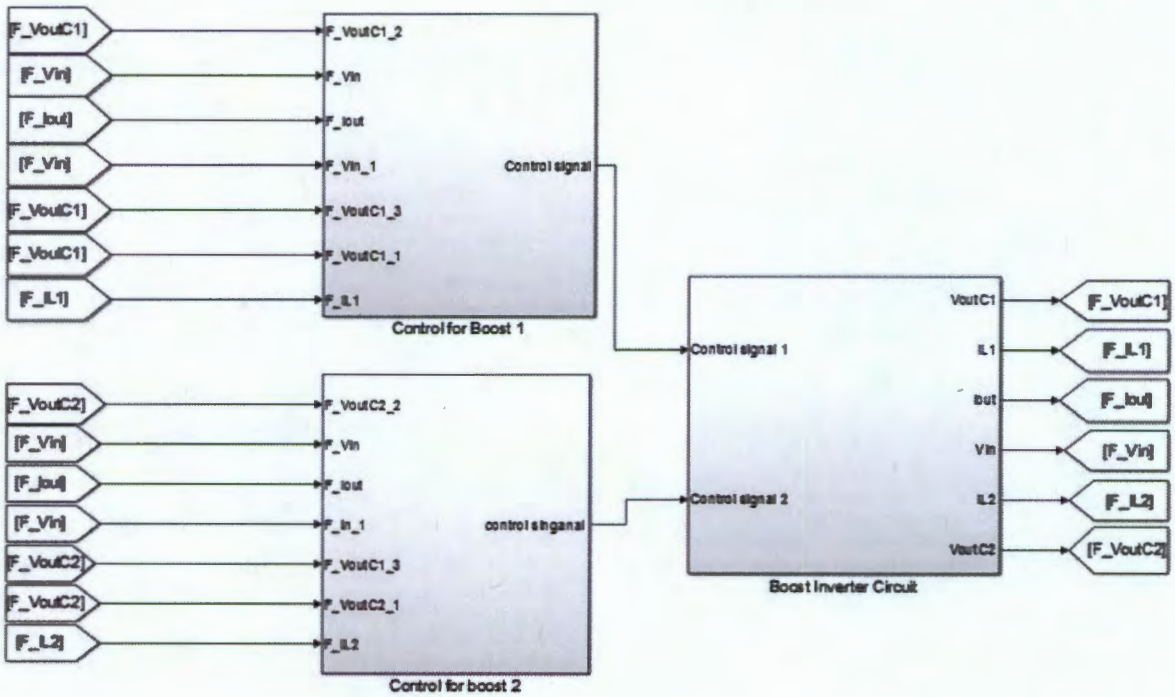

Figure A.5: Overall simulation model of the closed loop boost inverter system

Appendix A.3.1: Control Block Subsystems

The control block subsystems are shown in Figure A.6 and Figure A.7.

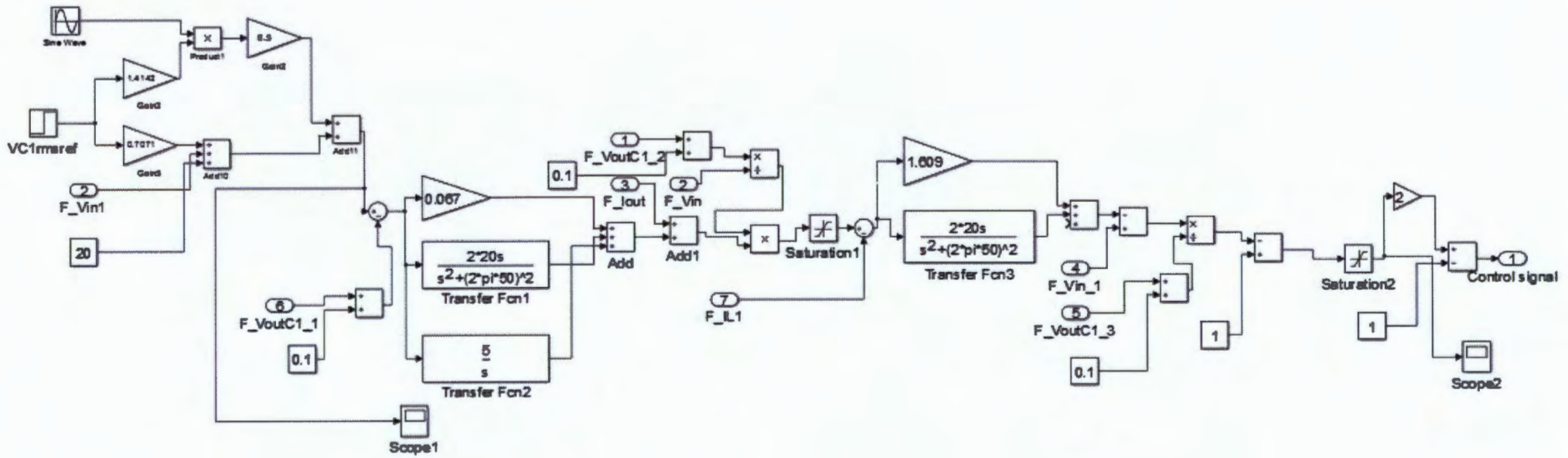

Figure A.6: Simulation model of the Control for Boost 1 subsystem.

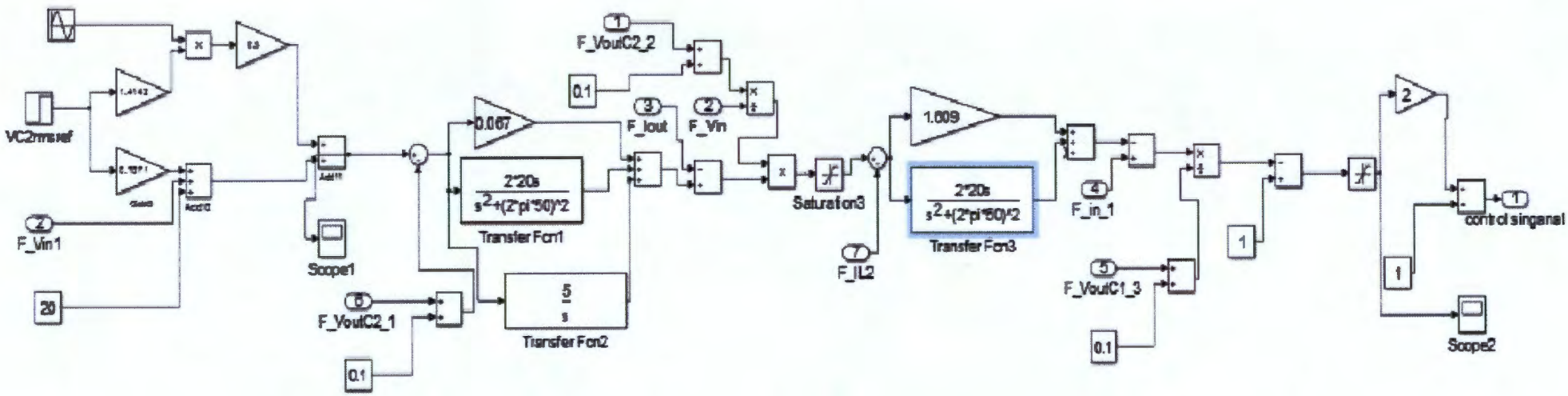

Figure A.7: Simulation model of the Control for Boost 2 subsystem.

Appendix A.3.2: PR Controller with Lossy Reactive Components.

The boost inverter circuit subsystem for the PR controller with lossy reactive components is shown in Figure A.8. The control blocks are shown in section A.3.1.

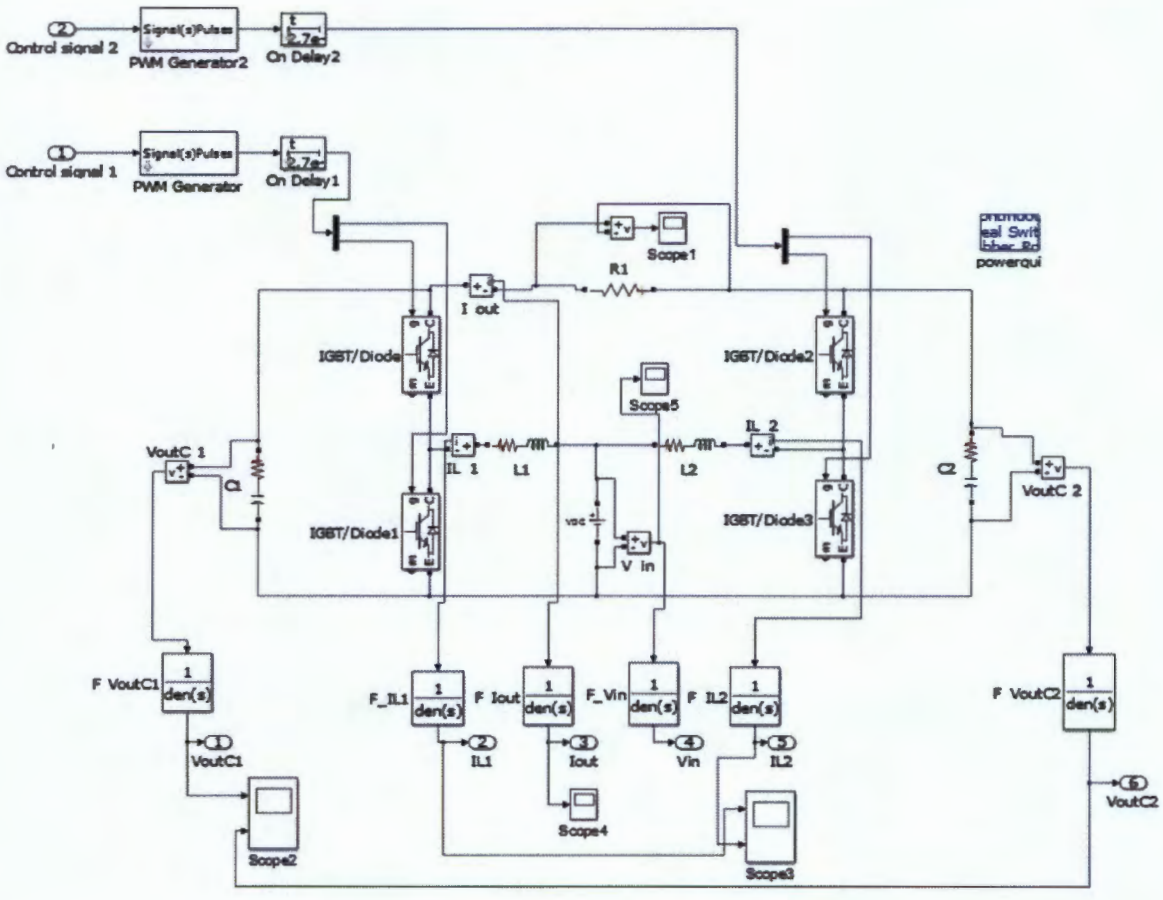

Figure A.8: Boost inverter circuit subsystem for the PR controller with lossy reactive components

Appendix A.3.3: PR and PIR Controller with Lossy Reactive Component, Switching Device Parasitic Capacitance and Deadtime.

The boost inverter circuit subsystem for the PR and PIR controller with lossy reactive component, switching device parasitic capacitance and deadtime is shown in Figure A.9. The control blocks are shown in section A.3.1.

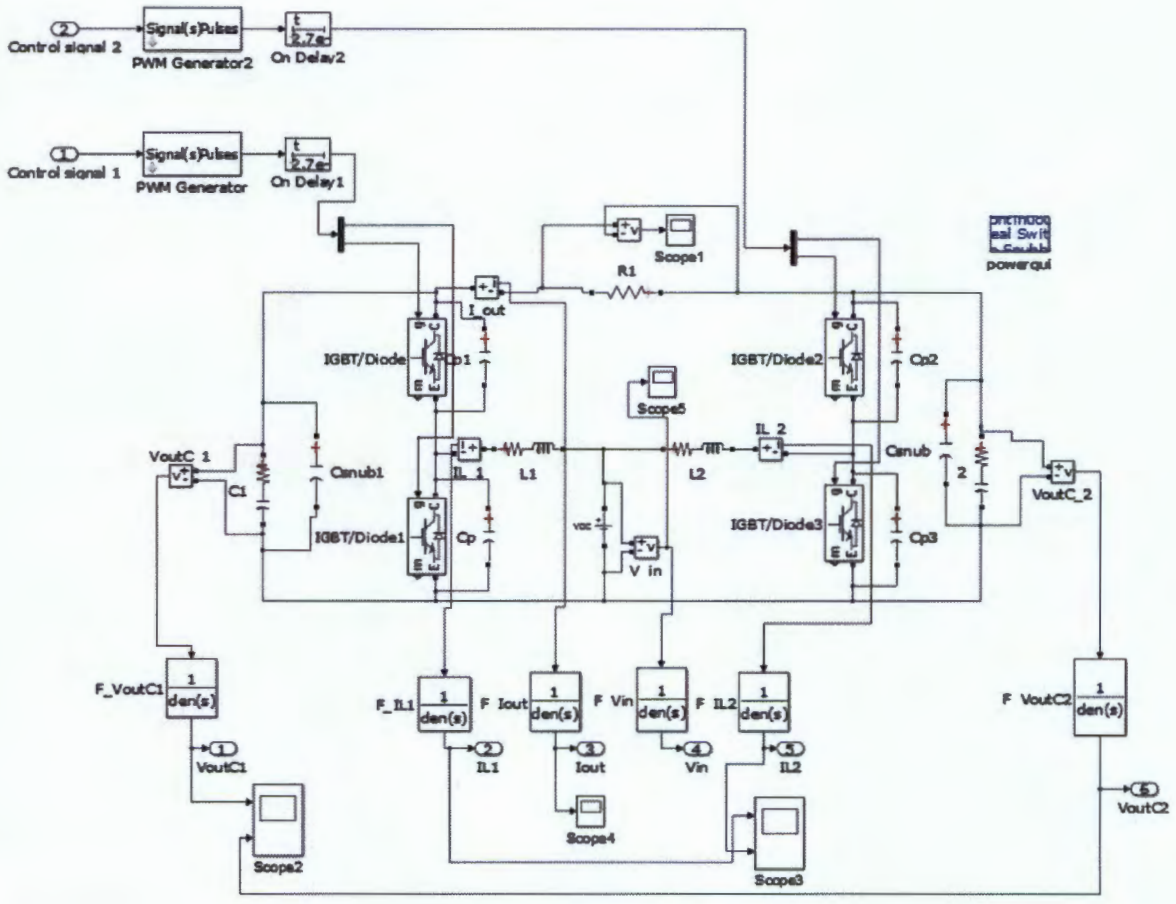

Figure A.9: Boost inverter circuit subsystem for the PR and PIR controller with lossy reactive component, switching device parasitic capacitance and deadtime

Appendix A.3.4: Linear Load Disturbance Boost Inverter Circuit Subsystem.

The linear load disturbance boost inverter circuit subsystem is shown in Figure A.10. The control blocks are shown in section A.3.1. The PIR controller was used.

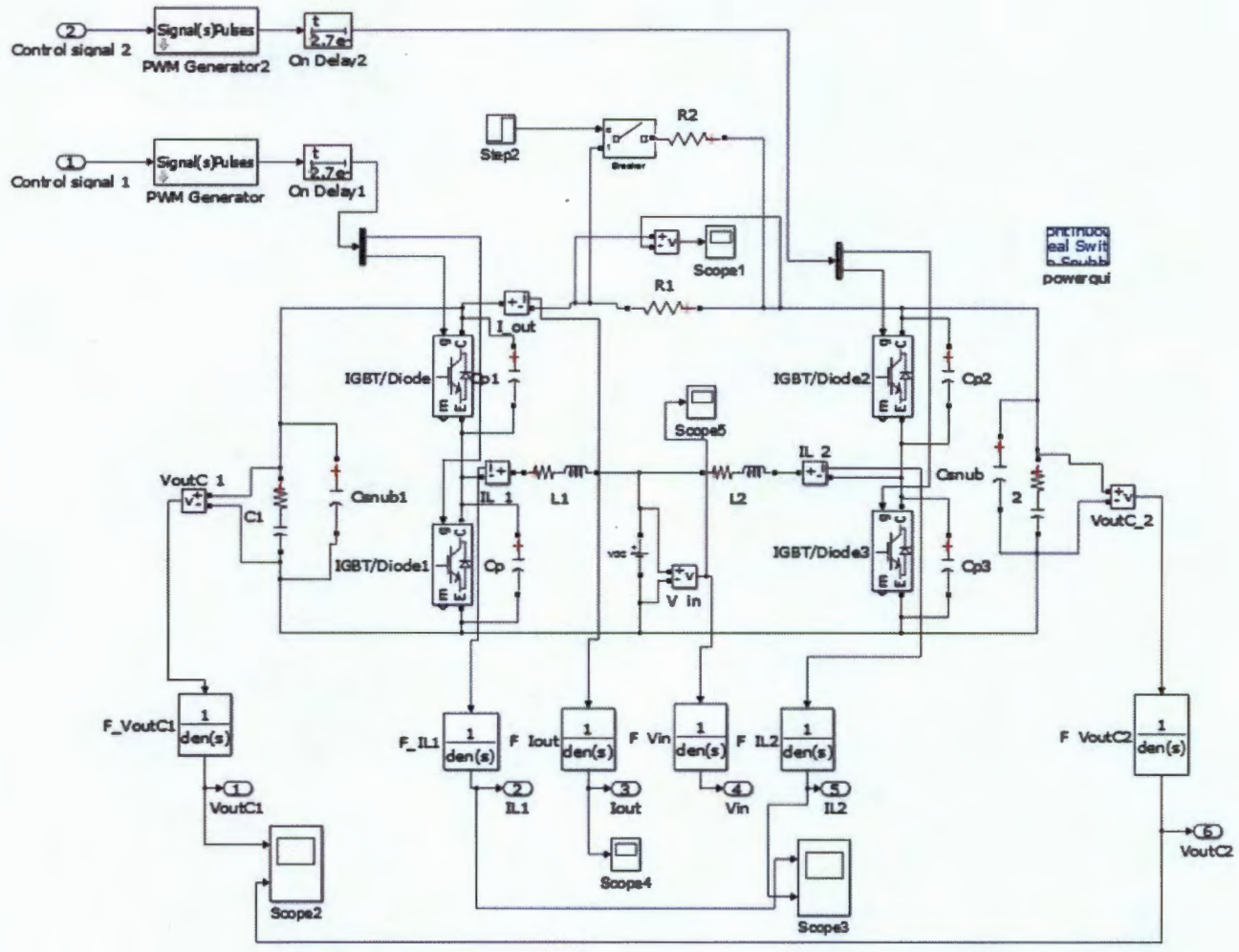

Figure A.10: Load Disturbance boost inverter circuit subsystem.

Appendix A.3.5: Inrush Current Boost Inverter Circuit Subsystem.

The boost inverter circuit subsystem for the PR controller with lossy reactive component, switching device parasitic capacitance and deadtime is shown in Figure A.11. The control blocks are shown in section A.3.1. The PIR controller was used.

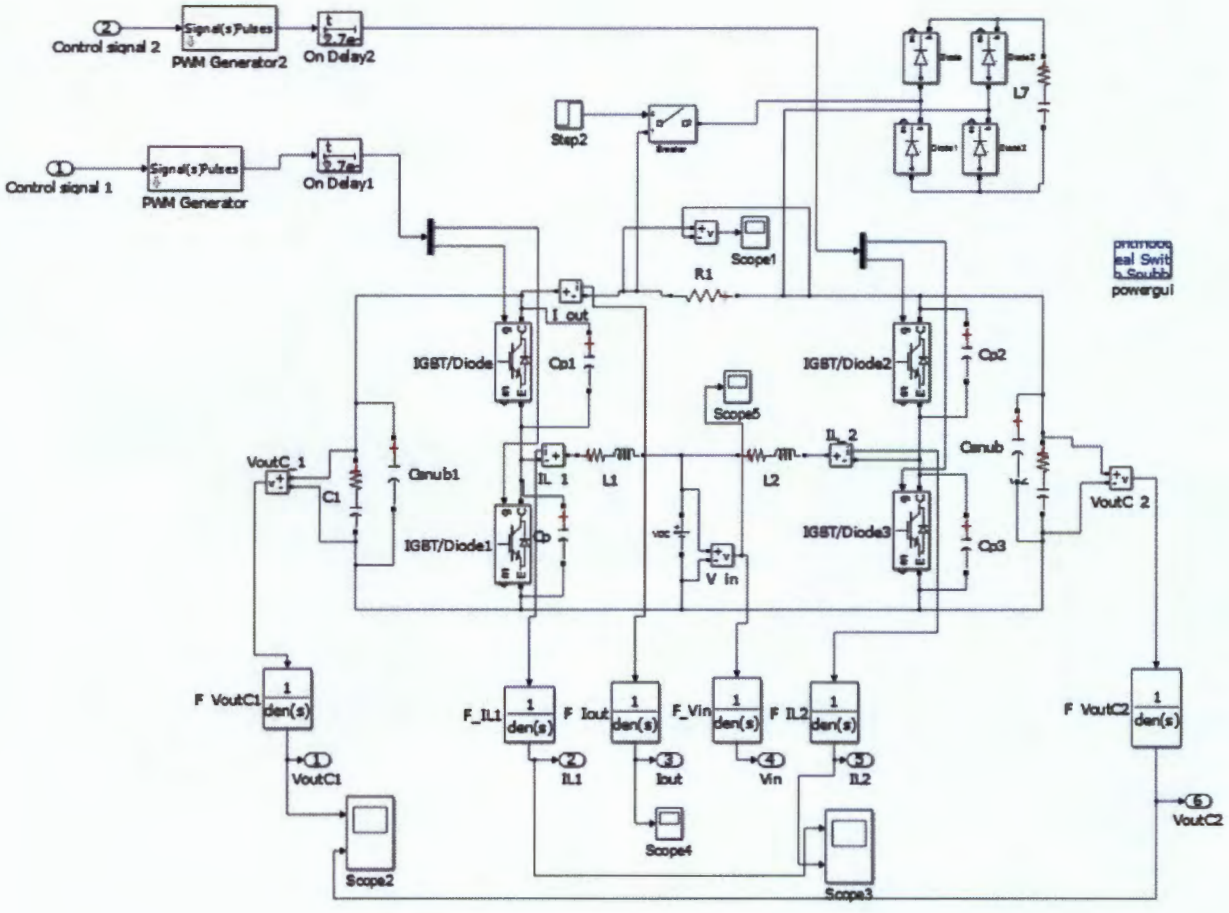

Figure A.11: Inrush current boost inverter circuit subsystem.

Appendix A.3.6: Nonlinear Load Disturbance Boost Inverter Circuit Subsystem.

The nonlinear load disturbance boost inverter circuit subsystem is shown in Figure A.12. The control blocks are shown in section A.3.1. The PIR controller was used.

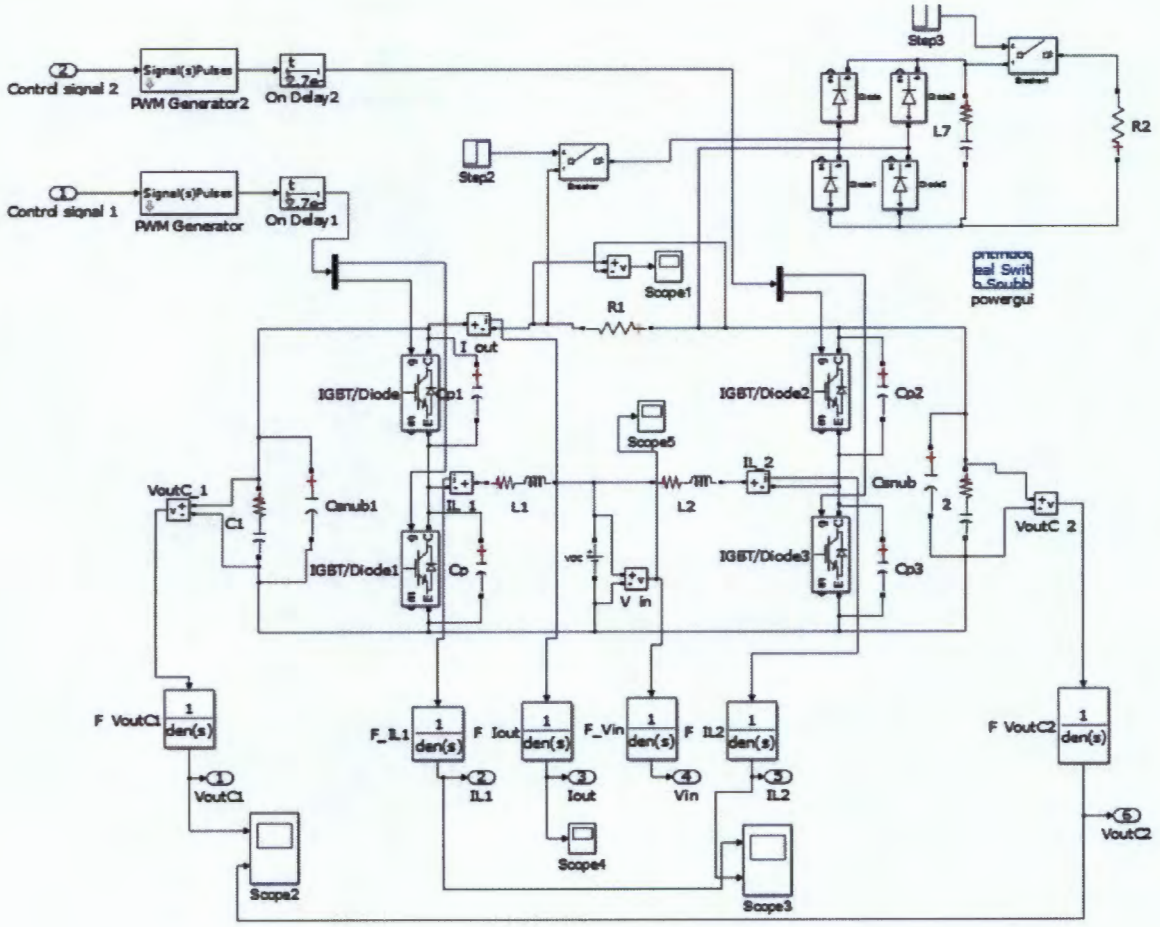

Figure A.12: Nonlinear load disturbance boost inverter circuit subsystem.

Appendix A.3.7: Input Voltage Disturbance Boost Inverter Circuit Subsystem.

The input voltage disturbance boost inverter circuit subsystem is shown in Figure A.13. The control blocks are shown in section A.3.1. The PIR controller was used.

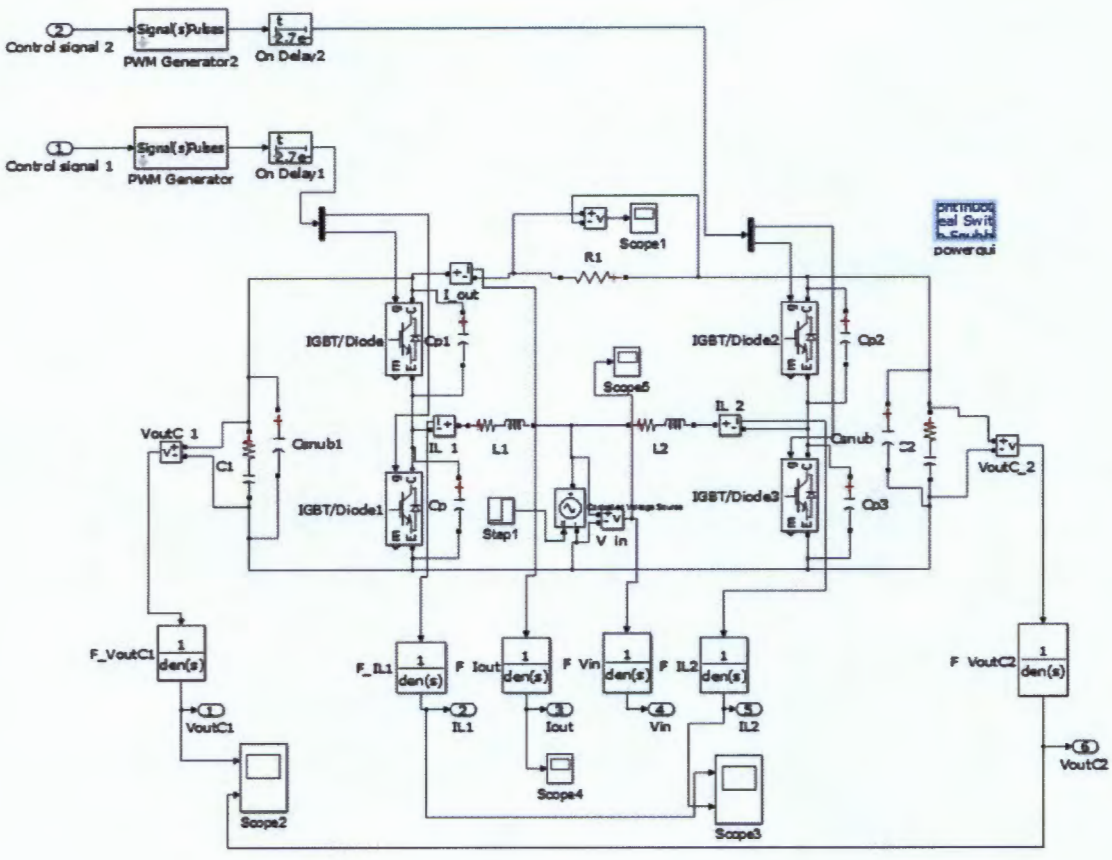

Figure A.13: Input voltage disturbance boost inverter circuit subsystem.

Appendix B: Experimental Set-up.

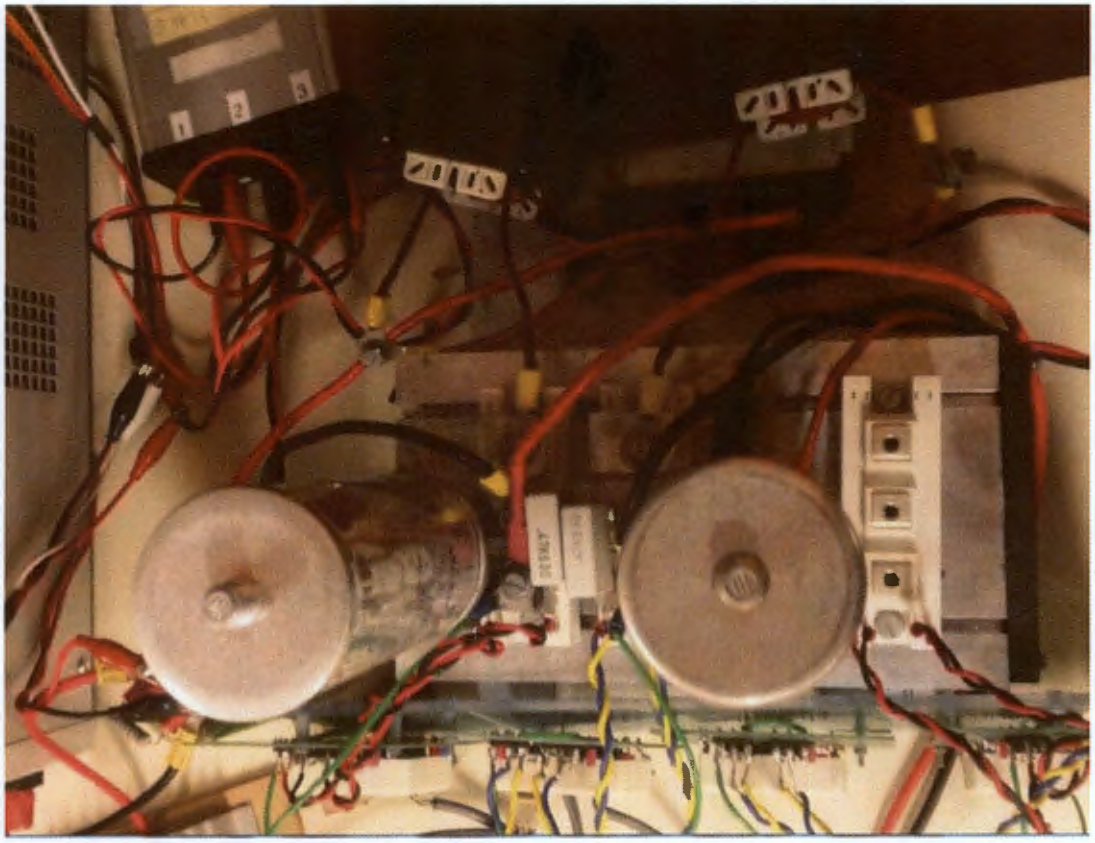

Figure B.1: Boost Inverter top view

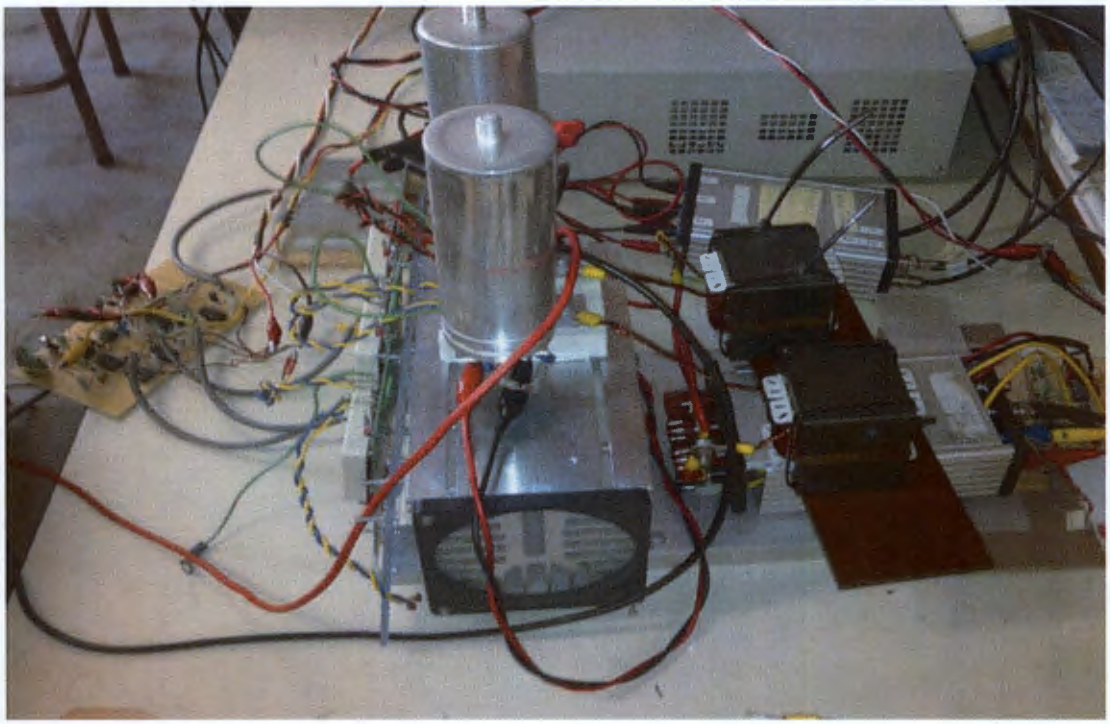

Figure B.2: Boost Inverter side view

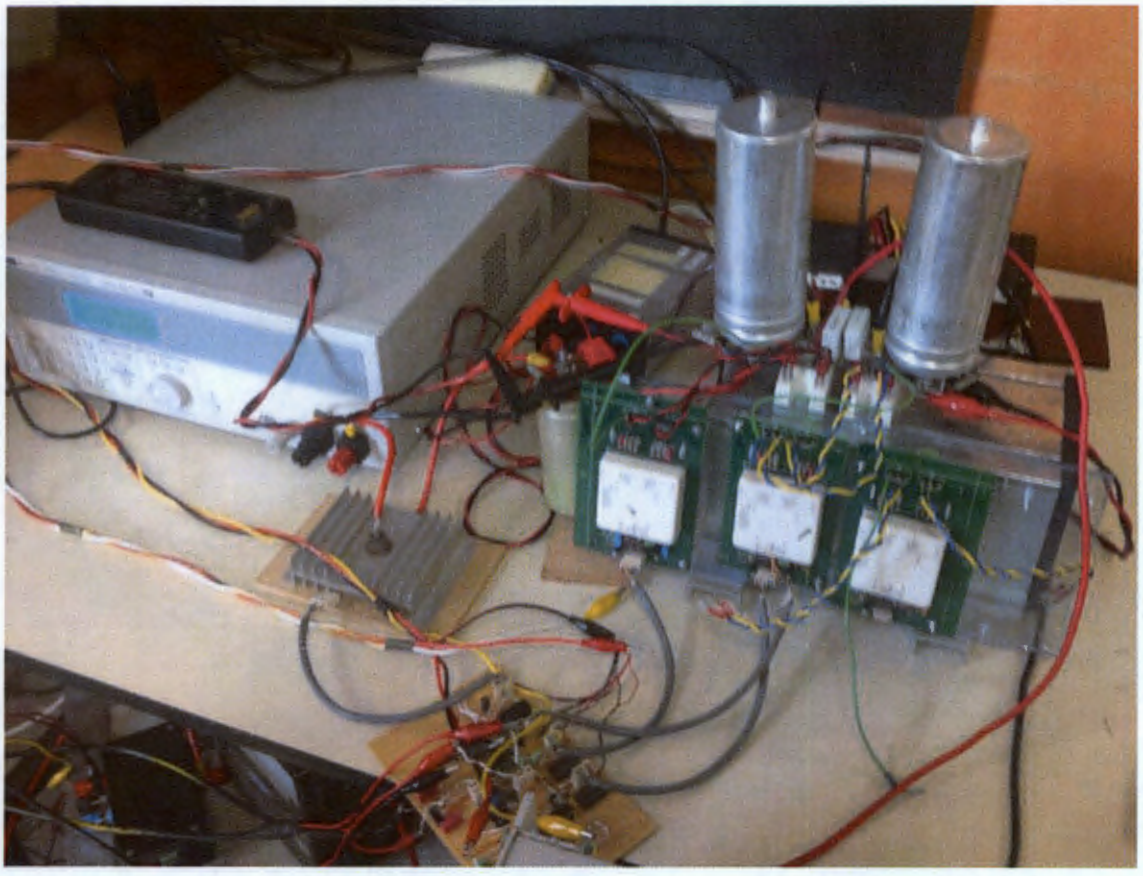

Figure B.3: Boost Inverter front view