AN INDUSTRIALIZED MICROPROCESSOR SYSTEM

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By

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A B S T R A C T

The aim of this project is to design and build an industrialized microprocessor system capable of testing the limits and capabilities of microprocessors in the industrial process control world. The system must be capable of operating in a data logging or control or supervisory capacity.

The system consists of a ruggerdized, electrically isolated unit, designed on a "black box" principle, with minimum operator controls. It is housed in a sealed crate with internal access via rows of input and output plugs and connecters.

The system has been designed on a modular basis in order to simplify expansion. It can be operated as a small dedicated controller or expanded by the addition of memory and/or industrial I/O modules to its full capacity.

The system is based on an INTEL 8080 microprocessor. The industrial interface consists of electrically isolated analog and digital input and output modules which can be selected under program control. There are also up to 64 asynchronous priority encoded alarm channels that can interrupt the control sequence at any time should an alarm condition arise. For debugging hardware and software a plug-on front panel unit is provided.

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SECTION I

INTRODUCTORY OVERVIEW

CHAPTER 1.

INTRODUCTION

1.1 THE LOGIC NOVEAU - MICROPROCESSORS

When the history of digital electronics is written, 1974 to 1976 will be recorded as the period when the microprocessor came of age. From humble beginnings, with only 2 products in 1971, an industry that had been predicted for at least a decade came into being. Now, a mere five years later, there are more than thirty different microprocessors available, announced, promised or under development.

Microprocessors are at present claiming the limelight in nearly every field of electronics. In calculators, point-of-sale terminals and graphics terminals, in traffic controllers and instrumentation, in electronic games and engine control units and finally in industrial process control where alone more than 40 applications of the microprocessor have been listed (ref. 1). The list grows every day as engineers find new applications of these remarkable elements.

The architecture of microprocessors is still in an evolutionary state, no two manufacturers agreeing on any one format, and each claiming superior qualities. As a result, microprocessors today have word lengths from 2 bits upwards and are manufactured using NMOS, CMOS, PMOS, VMOS, I^2L, SOS and bipolar technologies. Instruction sets likewise vary widely, each having its own virtues and restrictions.

For the digital designer the sudden rush of this "Logic Noveau" has come as something of a shock. Safely able to ignore the vagaries of software in the past, many engineers have begun to learn that many of their hard-won skills, such as in logic and later package minimization, are becoming obsolete overnight and that all the important logic is in the software.

However, once the designer has acclimatized to the microprocessor, he realises that, although microprocessors are no more a panacea than any other form of logic, they do offer numerous advantages, especially in the industrial process control world.

1.2 ADVANTAGES OF MICROPROCESSORS

A. Low Costs:

Their low cost allows many areas previously not economically viable for computer control to be brought under digital control. In fact, according to Intel Corporation Nichols (ref. 2), 20% of the areas in which microprocessors are being used at present are areas totally new to electronic instrumentation, and by 1980 this will grow to 80%.

B. Greater Efficiency:

By nature many of the control algorithms used to control industrial processes are relatively simple. Also, the time constants of these processes are often long, sometimes in the order of hours, compared to computer response times. Hence in many circumstances the computing power of a mini computer is an overkill with very little CPU time being devoted to controlling the process. This observation is borne out by the large amount of time available for background tasks on many process control computers. In these applications, a dedicated micro computer system would be a far more cost-effective solution.

C. Distributed Control Systems:

It is, however, in the field of distributed multi-microprocessor networks that microprocessor applications become really exciting. It is here that the microprocessor presents a direct challenge to the reign of the minicomputer in industrial process control.

There are two areas in which distributed multi-microprocessor systems have distinct advantages over minicomputers in industrial process control.

(i) IMPROVED SYSTEM RELIABILITY:
Firstly, there is improved overall system reliability gained by distributing the control of a complex process among a number of microprocessors each controlling a sub-section of a plant. In the traditional case where a central computer controls the complete process there is the problem that, should this machine fail, the entire process will come to a halt. A multi-microprocessor network gets around this problem as there is a low probability of all the microprocessors failing at once. If one fails, only a small section of the process is affected and manual takeover is minimal. The smaller number of component parts in a microprocessor also leads to high reliability and ease of maintenance.

The microcomputer may also be linked to a single supervisory minicomputer which may also have back up storage containing all the programs of the various microcomputers. Should any one of these fail, its entire program may be automatically reloaded from the central computer. This principle may also be extended to provide versatility inso-far as the microcomputer program may be dynamically altered by the central computer. The central computer can also provide mass data storage for the microcomputer. The central computer can also act as a "peripheral" to the microcomputer performing such needs as rapid multiplications and divisions for any arithmetic that need be done directly by the microcomputer.

(ii) REDUCED CABLING COSTS:
The second scoring point for a distributed microprocessor system is related to cabling expenses. These are most significant in processes that are distributed over a large area. With a centrally located computer, long runs of parallel wires connect the computer to the sensors and control points of the process, leading to high costs and noise problems.

The microprocessor, on the other hand, can be designed in a ruggardized industrial form to be located close to the process it controls, thus drastically reducing the length of parallel lines. A single serial line may then link the distributed controllers to other controllers or to a central computer. It has been calculated (ref. 3) that up to 76% of cabling costs can be saved by using this technique.

Reduced cabling and interconnections reduce the probability of noise pickup and again increases the overall system reliability. This incentive to improve reliability is the main reason for using microprocessors in industrial process control applications.

But how much of a viable proposition are multi-microprocessor networks and will they also not suffer from the problems of inter-processor communications of all other multi-processor systems in real-time environments? This attempt to define or establish the role and capabilities of micro-processors in industry in in fact the aim of this project as described in Chapter 2.

CHAPTER 2.

AIM OF PROJECT

2.1 THE ROLE OF MICROPROCESSORS

The exact role that microprocessors are destined to play is far from being defined. Will the rapid fire technological evolution see them channeled into small dedicated controllers or perhaps as fairly large-scale process controllers, or simply as intelligent building blocks? Most conceivably they will fulfill the requirements of all three categories as well as ceasing to be the sole property of the digital engineer and will be absorbed into the world of electronics as an available tool, to be used when really needed. It has been predicted (ref. 4) that the distribution of applications of microprocessors by 1978 will be :

(a) 25% of the market - replacement of hardwired random logic and analog controllers to upgrade existing systems;

(b) 10% of the market - filling the gap in cases where the mini computer was an overdesign;

(c) 65% of the market - totally new applications made possible by microprocessors' low cost and flexibility.

2.2 THE MEANS OF ESTABLISHING THIS ROLE

The aim of this project is to develop a low-cost microcomputer system capable of performing the following functions in typical industrial environments :

(a) Data capture and subsequent data processing and presentation;

(b) Supervision of a sub-section of a plant;

(c) Direct digital control of a sub-section of a plant.

The system is to be expandable, versatile and rugged enough to fulfill any or all of the above functions.

It is intended that this system assist in establishing the role of the microprocessor and evaluating its limitations.

Such an industrial process control microcomputer system could operate in any one of the three forseeable categories of application for microprocessors, i.e. :

(a) Replacing hardwired logic;
(b) Replacing underutilized minis;
(c) New areas in process control.

Many of the more subtle aspects of microprocessor applications are relatively unknown, for example reliability, memory requirements for a given job, language efficiency, programming techniques, the optimum degree of hardware/software trade-off, etc.

2.3 USING THE SYSTEM TO ESTABLISH THE ROLE

By designing a system to operate in an industrial environment, the reliability of a system may be fully verified. The expandibility of the system means that valuable comparisons may be made. A minimal system may be compared with a hardwired logic network, and a fully expanded system with its minicomputer equivalent.

The rigor of programming for a multitude of real time processes should put to full test the software capabilities of the machine.

In aiming at a low cost system investigations have been made into just how much "logic" can be performed by the software rather than by extra hardware, without overloading the demand on CPU time.

In order to build a system capable of investigating the capabilities of microprocessors in industrial applications, a particular design philosophy had to be adopted. This is covered in detail in Chapter 3.

CHAPTER 3.

DESIGN PHILOSOPHY

In formulating the design philosophy for the industrialized microcomputer system, two key factors were considered :

(a) The environment in which the system would be operating;

(b) The functions it would be required to fulfill in this environment.

Bearing these in mind, a design philosophy was formulated consisting of three specific concepts.

3.1 INDUSTRIAL RELIABILITY

The system must satisfy the requirements of industrial reliability. From the point of view of process control computers, an industrial environment implies an environment with a large degree of electro-magnetic noise as well as an atmosphere with a high percentage of corrosive gases and particles. Electrical supplies can also be expected to contain large amounts of noise such as line transients and dips or "brown-outs".

In order to operate successfully under these conditions, the following factors were considered fundamental to the design :

(a) The use of optical isolators to isolate the system from common mode noise induced on the signal lines connecting it to the industrial process;

(b) The use of constant voltage transformers and line filters on the power supply to isolate the system from line transients and dips. Also, battery backup for the volatile semi-conductor memory as well as the facility for a powerfail/restart routine was incorporated to cope with supply line "noise";

(c) The use of a crate to house the system which would provide electromagnetic and atmospheric isolation. Electromagnetic isolation is to be achieved by use of an aluminium crate lined with a ferromagnetic screen. The crate must also be sealed against a corrosive atmosphere. At the same time, heat from the power supply must be dissipated;

(d) The logic family (i.e. TTL, CMOS, etc.) to be used in building the system had to be carefully investigated as to which logic family provided the best trade-offs with regard to noise immunity, low power consumption and ease of use. The Low Power Schottky logic was ultimately selected for reasons described in Chapter 6.

The general architecture must be designed to minimise noise pickup and a termination facility of a suitable industrial standard must be provided.

3.2 EXPANDABILITY AND FLEXIBILITY

The microcomputer system must be capable of satisfying two extremes in process control requirements. These are :

(a) A minimal low cost stand alone system designed to control or monitor a small number of process parameters, say five or ten loops;

(b) A fully expanded system operating either on a stand alone basis or linked to a network and controlling or monitoring a large number of process parameters with a large amount of data formatting and handling. In the stand alone mode it must be capable of driving a full array of peripherals.

In order to achieve this, the microprocessor system consists of a basic "bare bones" layout consisting of a few essential cards of logic.

Expansion is then simply a matter of plugging on extra Input/Output or memory modules. The system may be expanded up to its full capacity of 256 input and 256 output ports, 65 kilowords of memory, a real time clock, and a full array of peripherals. In most applications the system used will be used somewhere between the minimal and fully expanded states.

3.3 THE BLACK BOX APPROACH

The system must be thought of as an industrial controller, and many of the traditional ideas of the computer-human interface must be discarded. The controller is housed in a rugged, electrically and environmentally isolated "box". The box has two rows of connectors for input and output. This control box needs no special airconditioned environment, unlike many classical computer systems.

In the interest of system security, this industrial controller/data logger has been designed for minimum operator interaction. Once the system has been installed there will be only two levels of access. The first is at the plant engineer or management level, where communication is provided via a keyboard which can be located in an office away from the "box" itself. From here, set-point changes, general program changes or initialization can take place, with an optional printout for every change that occurs and the time at which it took place.

The only other interaction is that of the maintenance engineer. This is achieved by means of a plug-in front panel which acts as a control and monitor device. There need only be one front panel for any number of processors, to be plugged into any computer system that requires attention.

With these concepts in mind, that is to build a "Black box" type of industrial controller/data logger, that is capable of operating in harsh industrial environments with minimum operator interaction and in a wide variety of applications, the viability of microprocessors in industrial applications may be fully investigated.

SYNOPSIS

In this section (Section 1), the "Logic Noveau" - the microprocessor, was introduced and some of its immediately apparent advantages in various engineering applications were delineated. The problem then is posed: What is the role of the microprocessor and what are its capabilities in a real time process control industry? To establish this is the aim and purpose of the project. The requirements for a system that would be capable of exploring such a role are expressed. The final chapter in the section then describes how such a system could be implemented and what the basic design requirement would be.

SECTION II

SYSTEM HARDWARE

CHAPTER 4.

INTRODUCTION TO HARDWARE

This section contains information concerning the design, operation and justification for choice of components in the Industrialized Microcomputer System. An overall block diagram and physical layout of the system is shown in figs. 1 and 2.

4.1 GENERAL ARCHITECTURE

The hardware design of the Industrialized Microcomputer system can be divided into three main sections :-

A. A Microcomputer: This consists of -

(1) A CPU module;

(2) 4 kiloword RAM memory module (expandable to 64 kilowords);

(3) Interrupt Control Unit and Real Time Clock;

(4) Peripheral Interface Unit.

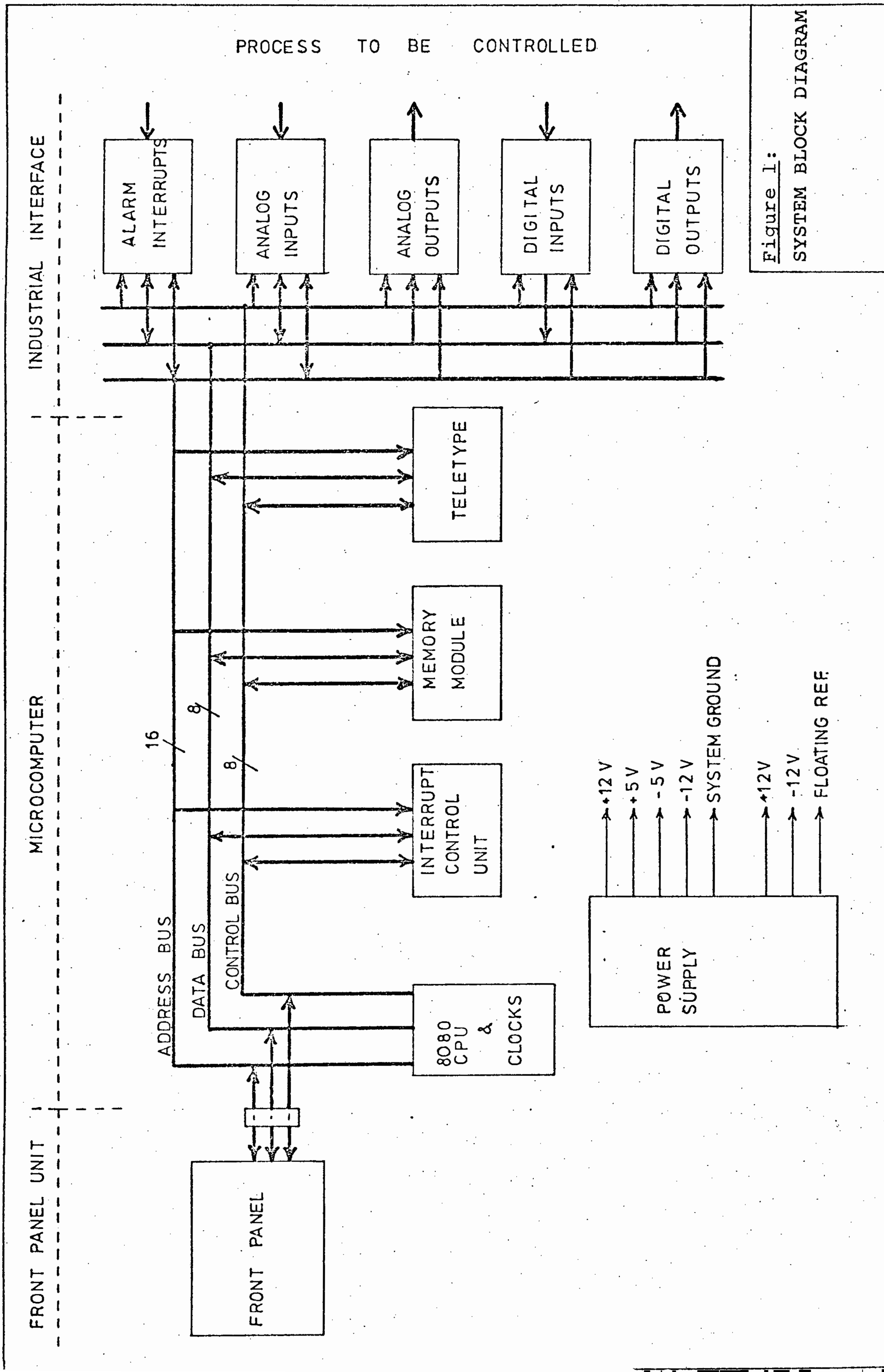
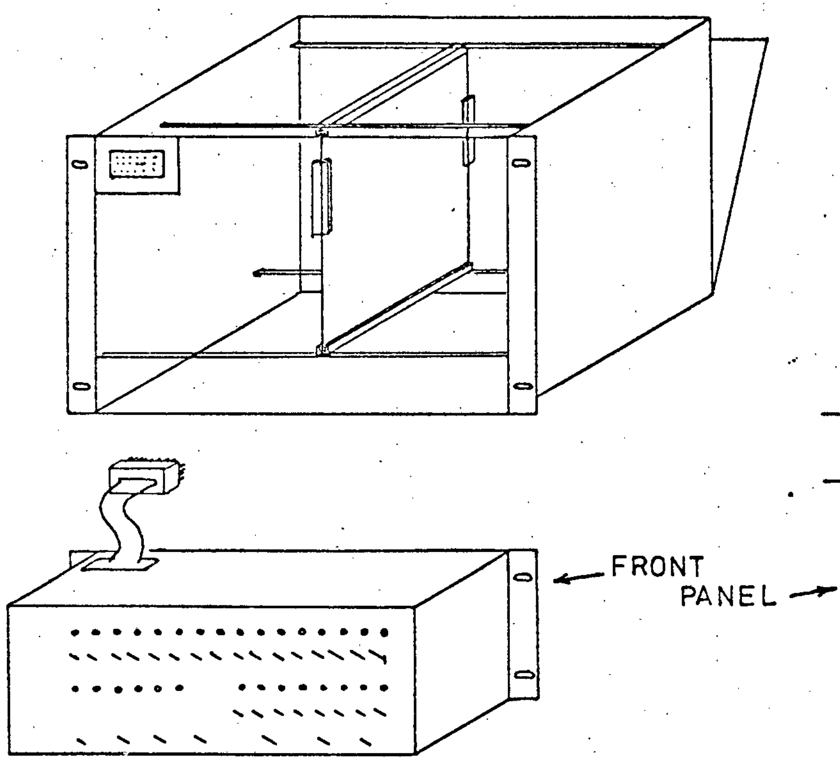
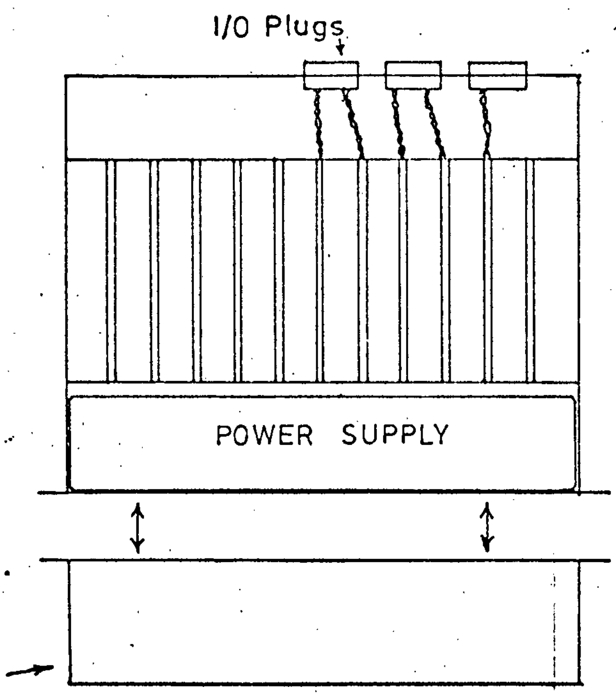


Figure 1: SYSTEM BLOCK DIAGRAM

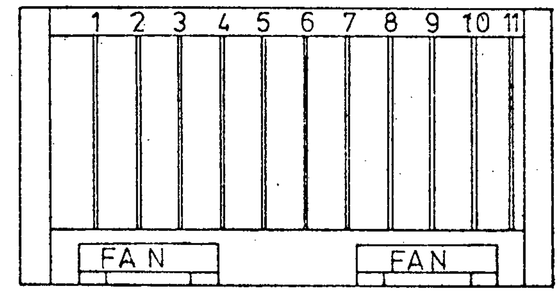
GENERAL VIEW



TOP VIEW



FRONT VIEW [without power supply]



SLOT NO.	DESCRIPTION
1	TTY. INTERFACE
2	Memory Module
3	CPU Module
4	Interrupt Control Unit
5	Analog Input Module
6	Relay Multiplexr
7	Alarm Interrupt Module
8	Analog Output Module
9	Digital Output Module
10	Digital Input Module
11	Spare

Figure 2: PHYSICAL LAYOUT OF SYSTEM

B. <u>A Front Panel Unit</u>: Consisting of -

(1) Led.'s displaying data bus, address bus, and control signals;

(2) Control lines to RESET, STEP or RUN the system;

(3) A front panel DMA channel.

C. <u>Industrial Interface</u>: This consists of -

(1) 16 Channel asynchronous Alarm Module;

(2) 32 bit digital Input Module;

(3) 32 Bit digital Output Module;

(4) 4 channel Analog Output Module;

(5) 16 channel Analog Input Module.

Analog input and output channels and digital input and output channels as well as Alarm interrupt channels are a sufficiently comprehensive interface to test the workability of the system in industry.

The system has been designed on a modular basis. The main purpose for this is that the system may be used with equal ease in both its minimal and fully expanded state. Each module or function in both the microcomputer section and the industrial interface section occupy one slot in the main frame, i.e. one card.

The front panel unit is a separate unit and is housed in its own sealed crate.

4.2 PRACTICAL LIMITATIONS

A. Size:

The system that has been built is the smallest system containing all the options in the industrial interface. That is to say, although the industrial interface may be expanded up to 256 input and 256 output channels and memory expanded up to 65 kilowords, these cards would require more space than is available in the crate. Thus only one module of each option has actually been built. This is sufficient to demonstrate the operation of the system. With adequate buffering expansion into further crates is straight forward.

B. Wire Wrap:

Although the system is intended for use in industrial environment, wire-wrapping techniques have been used for interconnections of the logic. The reason for this was the lack of adequate printed circuit manufacturing facilities. For a "one-off" job wire-wrapping is perfectly adequate and has two advantages over PC boards:

(1) Large ground and power planes can easily be provided;

(2) Interconnections can be kept shorter than on PC boards.

4.3 DEVELOPMENT PHASES

Hardware development of the system had three phases:

A. Selection of the electronic components - This consisted mainly of -

(1) Selection of the microprocessor - the Intel 8080;

(2) Selection of the logic family to be used - Low Power Schottky.

B. Construction of a hardware and software development system:- This was used to gain initial understanding of the microprocessor and was used later for the development of software.

C. Design and Construction of the Industrialized Microcomputer System:- This occurred in two stages -

(1) The design construction and testing of a microcomputer and front panel;

(2) The design construction and testing of the industrial interface using the microcomputer.

The entire system as it has been built covers ten cards in the main frame and a single card in the front panel unit. The relative location of these cards can be seen in fig. 2.

Justification for the various components used is given in the following chapters as well as a functional description of the various sections of hardware.

CHAPTER 5.

CHOICE OF MICROPROCESSOR

5.0 WHY THE INTEL 8080?

The choice of microprocessor to be used was made during the fourth quarter of 1974. The choice of microprocessor at that time was fairly limited (especially on the local market). See Appendix A The Intel 8080 was chosen for the following reasons :-

A. Previous experience with the Intel 8008 had shown this microprocessor to be suitable for industrial applications (Ref. 5) Most difficulties experienced with the 8008 had been sorted out in the second generation 8080 microprocessor.

B. The 8080 is particularly suitable for rapid handling of interrupts which are an advantage in this system.

C. The 8080 was considered fast enough for such an application and hence high speed bipolar microprocessors were not considered.

D. Good vendor commitment and ready availability of Intel products.

E. A powerful instruction set makes it worthwhile for future software development.

F. Although a CMOS based microprocessor may have been a better choice from the noise immunity consideration, no such processor was available at the time.

G. Second sourcing of 8080 by TI and Siemens ensures supply.

H. Good selection of compatible I/O and interface chips such as interrupt handlers and serial communication interface chips.

Ultimately the choice is governed by availability and at the time of selection the 8080 was one of the few microprocessors readily available. Since the time when the 8080 was originally chosen, the microcomputer market has exploded with a wide range of suitable products which may handle the job equally well, yet even now no one other microcomputer stands out as an obviously superior choice.

5.1 THE INTEL 8080 MICROPROCESSOR (fig. 3)

Intel's 8080 is an outgrowth of their experience with the 8008. Although there is much software compatibility many of the idiosyncracies in the 8008 (ref. 6) have been ironed out in the 8080.

The 8080 is manufactured as a single 40 pin NMOS chip. Architecturally, the 8080 has a three 16

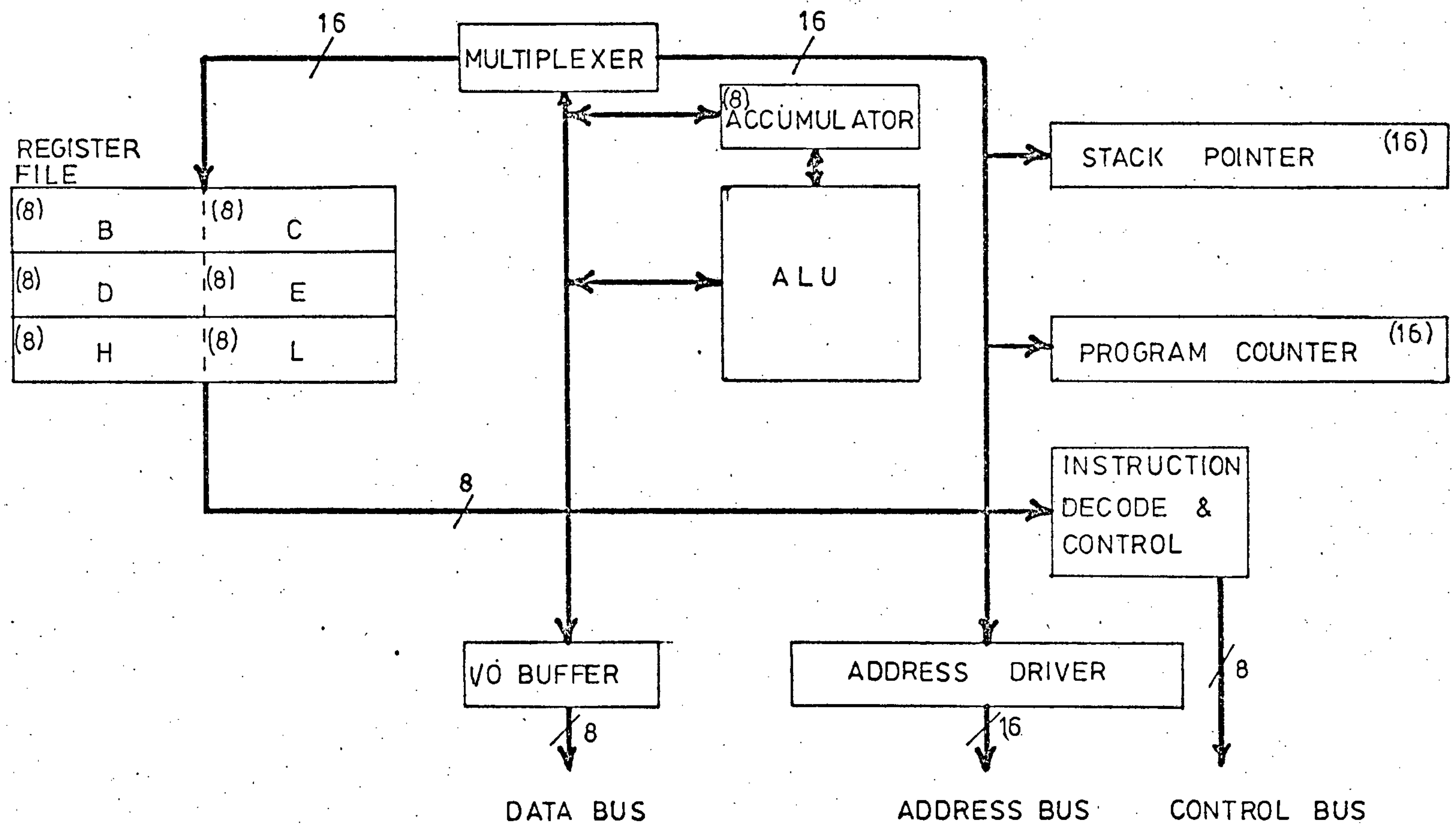


Figure 3:

8080 BLOCK DIAGRAM

bit register file and an eight bit accumulator. For compatibility with 8008 software many instructions treat these as seven separate eight-bit registers. The sixteen-bit stack pointer is used to place all return addresses in RAM, which means that the program counter must be a unique on-chip register. The address bus is sixteen bits wide and is entirely separate from the eight bit data bus.

The stack in RAM can also be used to store data and is of unlimited depth (to the limits of storage). The 8080 has instructions that permit explicit addressing of storage locations and allows any of the three main registers to hold and output an address when using register-indirect addressing.

The push down stack can be used to hold the status bits and important register contents for interrupt servicing.

Instruction execution times range from 2 to 9 microseconds for shortest and longest instructions. This is about ten times the speed of the 8008.

The 8080 has two potential disadvantages:

(1) From a software standpoint the lack of indexed addressing can be serious in some applications;

(2) From the hardware viewpoint, the need for a third power supply can be a disadvantage.

Details of operation and timing diagrams as well as a description of the control signals to and from the 8080 can be found in Appendix B.

CHAPTER 6.

CHOICE OF SYSTEM LOGIC FAMILY

A number of Logic Families were considered for the microprocessor system, i.e. the logic other than memory and the microprocessor itself. These are described below. Low Power Schottky was chosen ultimately for reasons discussed in 6.3.

6.1 CMOS

For an industrial environment where high noise immunity and low power consumption are invaluable credits to any logic family as well as its low price, CMOS seemed an obvious first choice. However, on closer examination CMOS was deemed unsuitable for the following reasons :

A. Incompatibility with rest of logic: The 8080 has output levels which are TTL compatible. CMOS cannot be driven by TTL levels. Furthermore, the memory chips, INTEL 5101's, although they are CMOS memories, also have TTL compatible inputs and outputs and are unsuited to drive CMOS.

This led to unnecessarily complicated logic if TTL-CMOS-TTL interfacing were introduced.

B. Excessive gate delays of more than 100 nano-seconds (for open drain gates) would have presented timing difficulties in the design.

C. Incomplete range of functions: A complete range of MSI functions was not available and certain key elements (such as 74148 and 74138) which are used frequently are not available in CMOS. These functions would then have to be implemented by SSI chips resulting in a far higher chip count.

6.2 STANDARD TTL

Standard TTL has proven itself many times (e.g. RTP Interface Systems (ref. 7)) to have adequate noise immunity to operate in an industrial environment provided reasonable precautions are taken. These include observing fan-out rules, keeping lines as short as possible, not leaving unused inputs floating, and providing adequate decoupling. The other well-known advantages of TTL are low cost, ready availability and a wide range of functions.

The only reason TTL has not been used throughout is that for nearly all the same advantages as standard TTL, Low Power Schottky TTL has an added primary advantage of having one-fifth the power consumption as well as many other secondary advantages.

6.3 LOW POWER SCHOTTKY TTL

See Appendix C.

Low Power Schottky TTL (LS TTL) was chosen as the logic family most suited to implement the industrialised microprocessor system. The reasons are as follows :-

A. LS TTL has many of the advantages of standard TTL such as ready availability and a wide range of functions. Its direct interchangeability with TTL means that anything not immediately available in LS could take a TTL substitute.

B. Lower supply current than TTL allows smaller cheaper power supplies, reducing system cost, size and weight.

C. Lower consumption means less heat is generated, which simplifies thermal design and cooling requirements can be reduced for equal packing densities.

D. Reliability is enhanced since lower dissipation causes less chip temperature rise above ambient; lower junction temperature increases MTBF. Also lower chip-current densities minimise metal related failure mechanisms.

E. Less noise is generated since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL. In addition load currents are only 25% of TTL, hence when a logic transition occurs current changes along signal lines are proportionately smaller as are changes in ground current.

F. Can use standard TTL as buffers giving a fan-out of 50.

The only disadvantage of LS TTL is that it is priced in the order of nearly double that of standard TTL. However, this was considered to be a temporary disadvantage as LS TTL prices will undoubtedly drop as popularity and demand increase.

CHAPTER 7.

GETTING STARTED IN MICROPROCESSORS

7.1 THE NEED FOR A DEVELOPMENT SYSTEM

Although at present the microprocessor is becoming yet another element in the electronics engineer's toolbag, it is still no ordinary component. It is a "programmable component" of considerable complexity especially when considered from the viewpoint of the engineer about to embark on the design of a microprocessor system, but having no previous microprocessor experience. From the hardware point of view, the microprocessor is too complex to be able to simply study the specifications and then to embark immediately on the design of a final product.

From the software point of view, a development system was warranted so that familiarity could be gained with the use of the instruction set. From this, estimates of memory requirements could be made for the final product. Also software development could continue while the final system was still being constructed.

7.2 APPROACHES TO A DEVELOPMENT SYSTEM

There are two basic alternatives when considering a microprocessor development system :-

A. Buying a vendor supplied development system;

B. Building one's own development system.

In the case of this project it was decided to build a development system from scratch. The reasons were as follows :-

A. At the time of consideration, development systems had just appeared on the market and prices were still high;

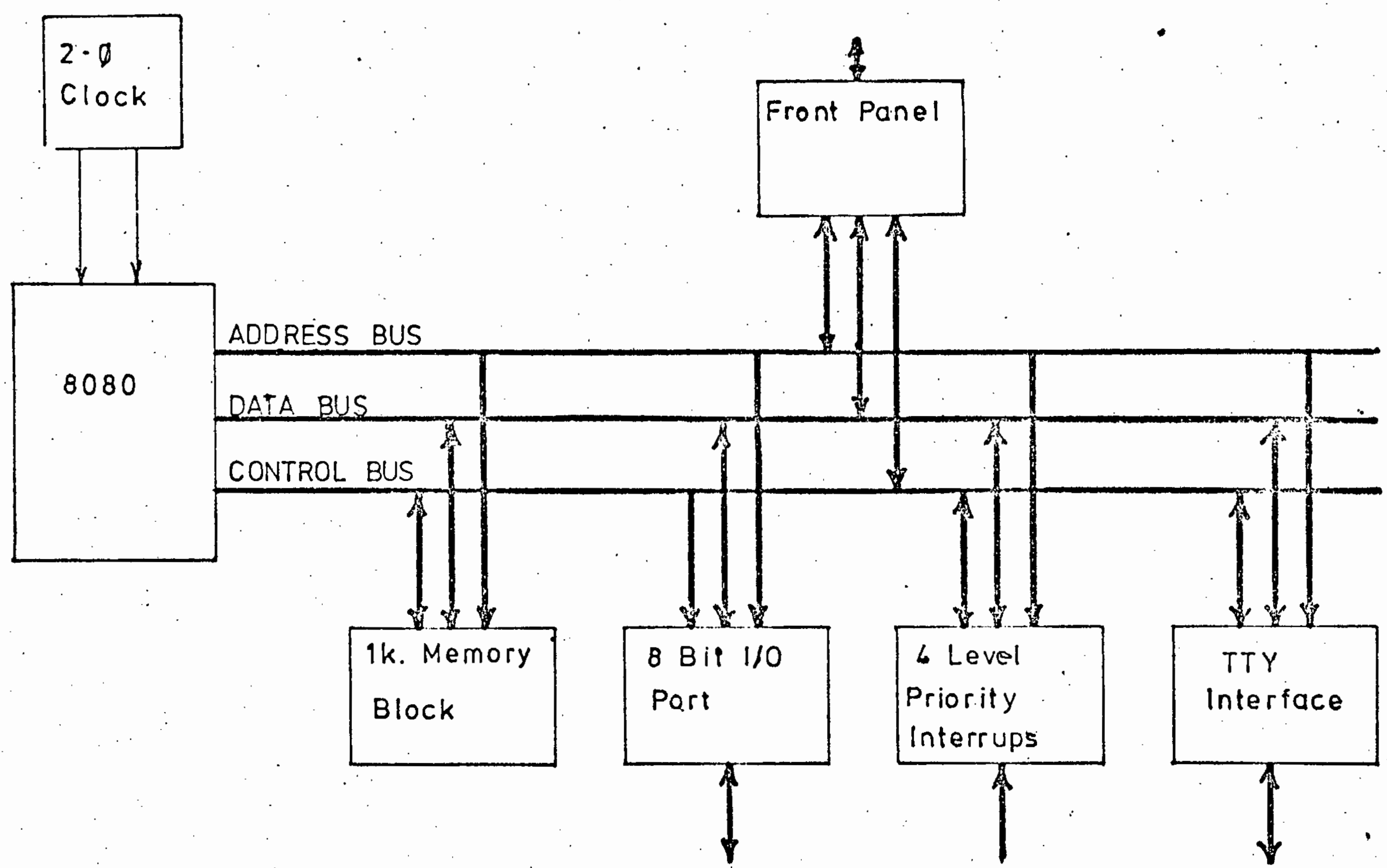
B. As one of the aims of the project was to increase knowhow, it was felt that a closer insight into the microprocessor could be gained by starting from the chip;

C. The hardware could be designed far closer to the final product thus considerably decreasing the final design time;

D. Software development would be largely unaffected by the choice.

7.3 DESCRIPTION OF THE DEVELOPMENT SYSTEM

The Development system is basically a simple micro-computer with a fairly comprehensive front panel. See (fig. 4).



<u>Figure 4</u>:

DEVELOPMENT SYSTEM
BLOCK DIAGRAM

It was constructed as a "computer on a card" and on one 9" x 7" wirewrap card there is the CPU, 1K x 8 bits RAM memory, a TTY interface, an 8 level vectored priority interrupt controller and one 8 bit I/O port.

The front panel displays the contents of the Address bus, data bus and Status and control information. The processor can be RUN, RESET or STEPPED from the front panel and there is also a Direct Memory Access (DMA) channel which allows the memory to be communicated with directly from the front panel.

The communication peripheral is an ASR 33 teletype with a 110 baud interface.

The entire system is housed in an open framework crate which gives easy access to all IC's to simplify the hardware debugging process.

7.4 BENEFITS OF THE DEVELOPMENT SYSTEM

A considerable amount of hardware and software was developed on the system, much of which was used unaltered in the final design. The benefits may be listed as follows :-

A. Hardware

(1) A thorough understanding of the hardware and timing requirements of the 8080 was developed;

(2) Memory and TTY interfaces were developed which were used virtually unaltered in the final design;

(3) The vectored interrupt system on the development system was built using mainly SSI chips. However, considerable chip saving was obtained by the use of MSI encoders in the final design;

(4) The exact requirements for a front panel that would be of assistance in both hardware and software development were investigated.

B. <u>Software</u>

(1) A thorough understanding of the 8080 instruction set was obtained by writing a number of fairly simple machine code programs;

(2) A resident 8080 AID debugging program was developed (ref. 8). This program occupies approximately 1 kiloword of memory and was run on the development system. It has proved to be an invaluable software aid.

CHAPTER 8.

THE MICROCOMPUTER - HARDWARE DESCRIPTION

The microcomputer part of the complete system is distributed over four cards and consists of the following :

A. CPU card;

B. Interrupt Control Unit and Real Time Clock (same card);

C. 4 kiloword RAM memory card;

D. Peripheral Interface Unit.

8.1 C.P.U. MODULE

Refer to fig. 5.

The CPU card consists of the following elements:

A. Intel 8080 CPU;

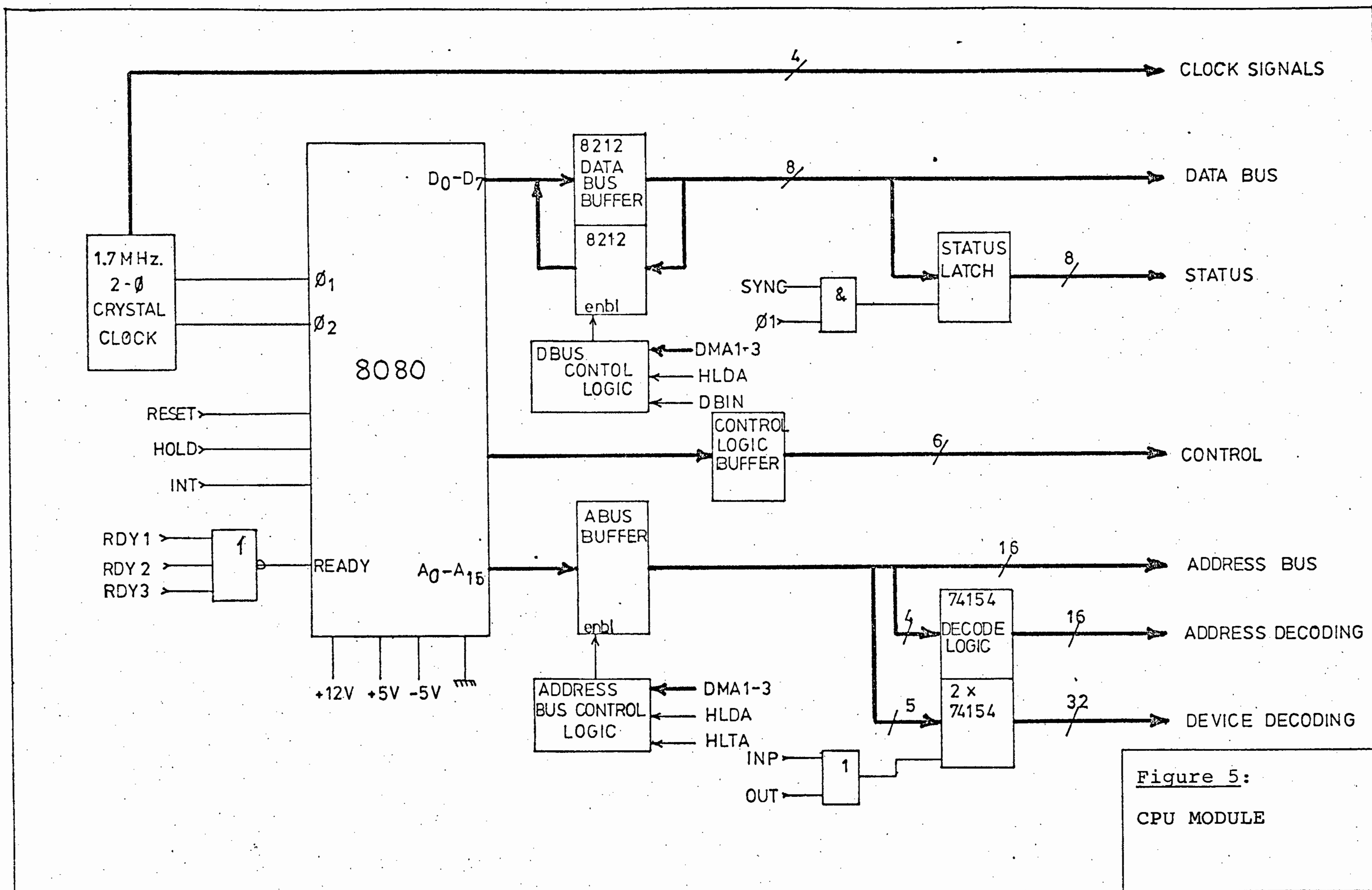


Figure 5:

CPU MODULE

B. Address bus and Data bus & Control signal buffering;

C. Status latching;

D. 2 phase clock;

E. Address bus decoding;

F. Device decoding.

8.1.1 <u>Intel 8080 CPU</u>:

For the details of the exact function of the various control lines see Appendix B.

A point of interest here is the READY line. When this line is active (high) the 8080 will RUN, and when inactive the CPU is in the STEPPED state. An important timing consideration not explicitly mentioned in the manufacturers specifications is the fact that the READY line must not be allowed to change state during Ø2, i.e. it must be clocked with Ø1. This is because the state of the READY line is examined during Ø2 and must be stationary during this time. The READY line may be accessed via three possible lines, RDY1 - RDY3. RDY1 is used by the front panel when manually STEPping or RUNning the computer. RDY2 is used by the memory interface to slow the 8080 down for the slow 1 micro-second Intel 2102 memory chips. RDY3 is a spare line and would be used by say DMA channels to stop the 8080 while a memory block transfer is taking place.

8.1.2 Buffering:

The address bus is buffered by two 8212 tri-state buffer chips. These chips only load the address bus by 0,25mA and have an output drive capability of 15mA/line. As most of the rest of the system is made up of low power Schottky (I_{OL}=0,25mA) the fan out is in the order of 60 which is sufficient.

The data bus is also buffered by 8212's. In both the Address bus and the data bus buffering, the tri-state ability of the 8212 is required. They are required to go into tri-state during DMA transfers from either the front panel or a peripheral when either one of these devices accesses memory. The data bus is a bi-directional bus and hence two 8212 are used back to back.

8.1.3 Status Latching:

At the beginning of each machine cycle, during SYNC time the 8080 sends out 8 bits of status information on the data bus. As the status is applicable during the whole of the machine cycle, not just during SYNC, it must be latched when it appears. This is done by the 8 bit latch as shown. As these signals are used throughout the system for control purposes, standard TTL chips are used in the latch to provide the added drive (fanout of 60 LSTTL).

8.1.4 Clock:

The 2 phase clock is a crystal controlled clock running at 1.7 MHz. It has an adjustible mark space ratio on each phase, as well as an adjustible phase relationship. This is necessary in order for the clock to comply to the 8080 requirement.

Six signals are derived from the clock :-

A. MOS level (0-12V) Ø1 and Ø2 for driving the 8080 directly;

B. TTL level Ø1 and Ø2 as well as $\overline{Ø1}$ and $\overline{Ø2}$ for timing requirements in the system itself.

8.1.5 Address Bus Decoding:

The 8080 can address 256 I/O devices directly, i.e. it has an eight bit address word. In order to derive a unique signal for each device an 8 to 256 line decoder is necessary. This is done as shown in fig. 6. The first level of decoding is done on the CPU board, and the second level is done on the I/O boards themselves, i.e. each I/O board will have a 4-16 line decoder.

This decoding is also required to address the INTEL 5101 memory chips. The advantage of having the first level of decoding on the CPU card is that each I/O or memory card requires only one 4-16 line decoder, not two.

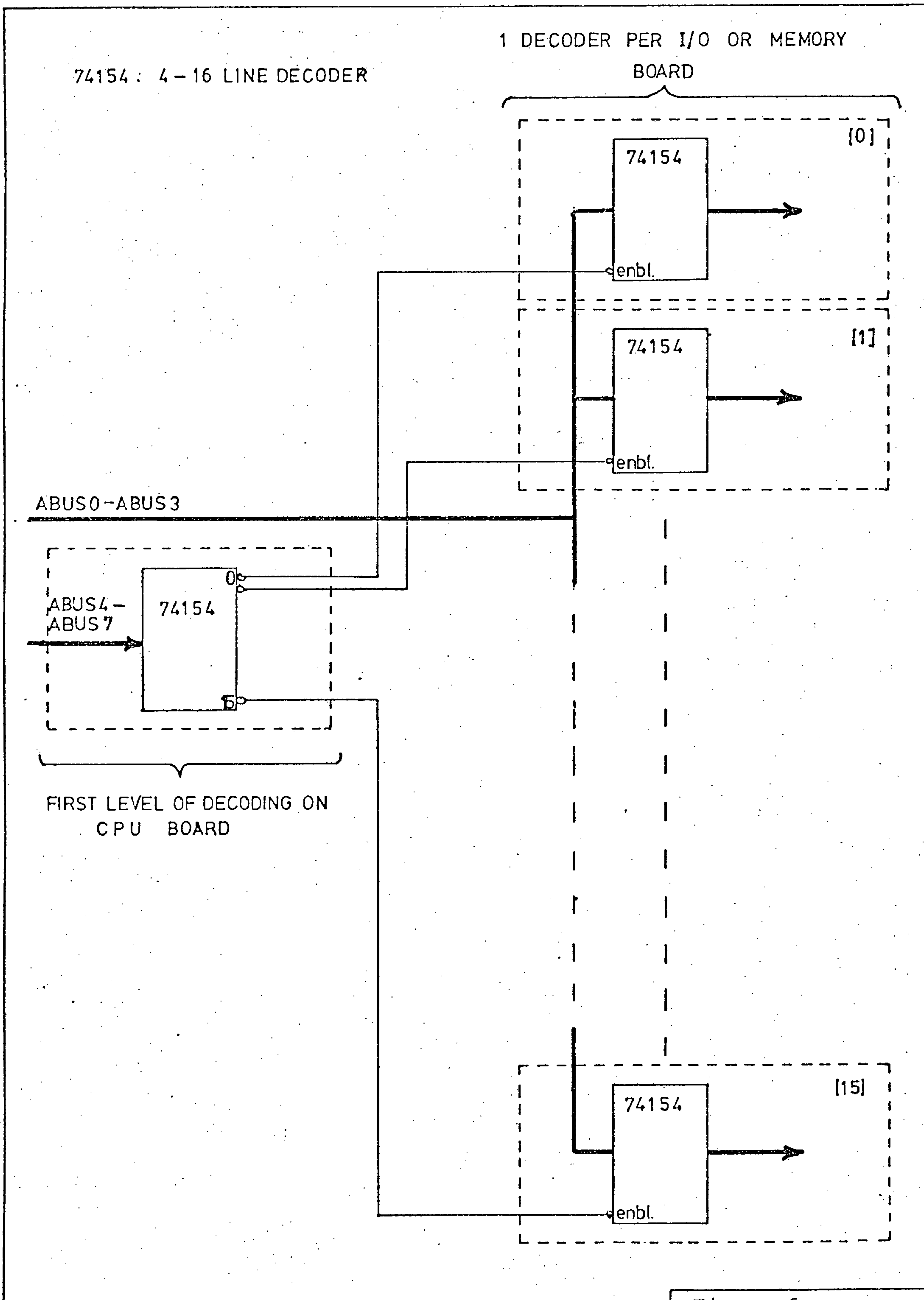


Figure 6:

DISTRIBUTED IMPLEMENTATION OF 8 - 256 LINE DECODER

8.1.6 Device Decoding:

Unique "enable" signals for the first 32 devices have been decoded on the CPU board as well. These are used for internal devices within the micro-computer itself such as the interrupt mask or tele-type, etc.

8.2 INTERRUPT CONTROL UNIT AND REAL TIME CLOCK

See fig. 7.

This unit stores accepts and then resets up to 256 vectored priority interrupts.

8.2.1 How the 8080 handles Interrupts:

For a detailed description and timing diagram see Appendix B.

Interrupt requests are communicated to the 8080 via a single line, the INT line. If the 8080 is in a position to accept interrupts and the INT line goes high, the following occurs :-

A. The current instruction is completed;

B. During the next instruction fetch cycle, the program counter is not incremented and a 1 byte instruction is jammed onto the bus;

C. The instruction used is the RESTART (RST)

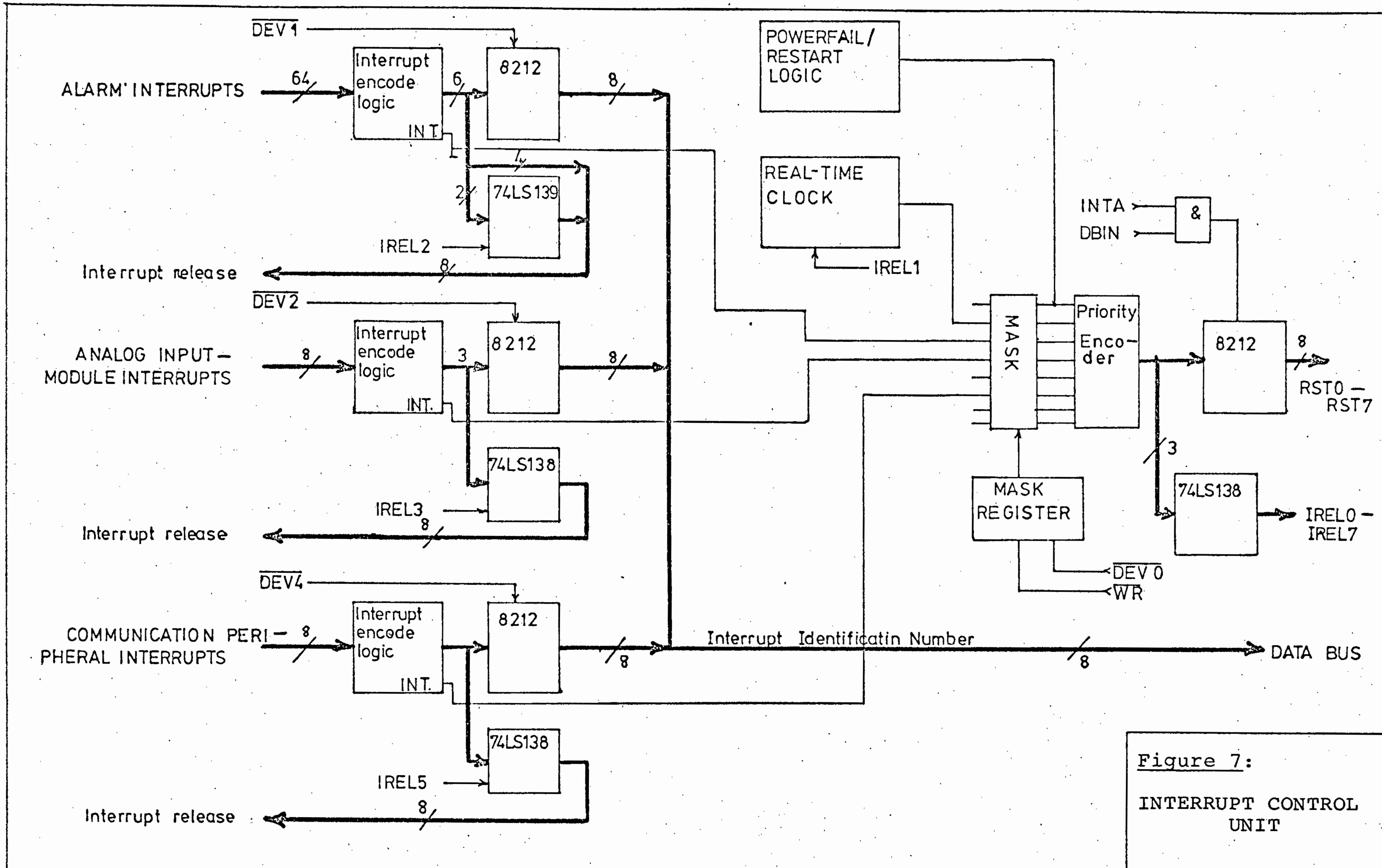


Figure 7:

INTERRUPT CONTROL UNIT

instruction which stores the program counter on the stack and then traps the 8080 to one of eight locations as specified in the variable field of the RST instruction.

8.2.2 <u>Function of the Interrupt Control Unit</u>:

The Interrupt Control Unit (ICU) is a two level hierachical interrupt handler that can accept and format up to 256 interrupts from the process being controlled. 256 was chosen as the maximum number as this gives a convenient single byte (8 bits) address. When an interrupt is received the ICU generates two addresses. The first is a three bit word which becomes part of the variable field of the RST instruction (see 8.2.1 above), causing the 8080 to branch to a specific location. This is the first level of the interrupt controller. Each of the eight levels specified by the RESTART instruction can now be split up into a further group of interrupts. Hence, from one of the eight trap locations (obtained from the RST instruction) the 8080 can input a further 8 bit address to establish the exact identity of the interrupt. Obviously if only one interrupt is connected to one of the eight levels then further splitting of this level is unnecessary.

If two interrupts occur simultaneously, the one with the highest priority is serviced first. All others are stored and serviced at the next available opportunity. Interrupts are reset as soon as they have been accepted. (For the organisation of priorities see 8.2.5 below).

The first level of the interrupt structure may be masked out by outputting the desired mask to a mask register. If any of the eight basic levels have been masked out, interrupts received on these levels are stored until the mask is removed. They are then serviced according to priority. This is useful for the times when the 8080 enters a non-interruptable state, but interrupt requests occurring during this time must be serviced as soon as this state has been left.

8.2.3 Implementation of the ICU:

Incoming interrupts on each of the eight levels are encoded by means of 8-3 line encoders (74148) which establish the unique address of that interrupt. This address is then latched by means of a tri-state 8 bit latch (8212) feeding onto the data bus. Each of these latches associated with the eight levels and containing the address of the interrupt on that level has a unique device address, so that the interrupt address may be inputted from it when required. Each latch is treated as a separate device, its own address being associated with the level of interrupt it is servicing.

The eight interrupt request signals are now fed to the next level in the ICU where they are again encoded into a 3 bit word by a 8-to-3 line encoder. The output of this last encoder forms the variable field of the RESTART instruction which has been hard-wired onto a tri-state latch feeding onto the data bus. When an interrupt occurs the RESTART instruction is jammed onto the bus at the appropriate time (when INTE.INTA.DBIN is true).

The output of this last encoder is also fed to a 3-to-8 line decoder which generates the "Interrupt release" signals IRELO to IREL7 which are used to reset the interrupt which has just been accepted.

In other words, any one of 256 interrupts is encoded into a three bit address and an eight bit address and then re-decoded, after it has been accepted, to give a unique line that will reset that particular interrupt.

8.2.4 Justification for the Method of Implementation:

Two alternatives to this method of implementation were considered :-

A. The first is a software implementation of the priority encoding. In this method when an interrupt on one of the eight possible levels occurs, all the interrupt lines to that level must be scanned and the priority of the interrupt ascertained by software means.

   This method was not used because it increased the interrupt response time without a compensatory decrease in chip count. Although more of the interrupt handling would have been under software control, the hardware required to implement this would have been more complex as the 8080 is not suited to this form of interrupt handling.

B. The second alternative would have been to use the Intel interrupt handling chip, the INTEL 8214. Although this chip is suited to use with the 8080, and using it would have resulted in a decrease in chip count, it has one serious drawback. It requires interrupting signals that are a change of level, not a pulse or edge triggered. An interrupting signal must go low and stay low until it has been serviced. If the interrupting signal is a pulse it may be missed and not serviced. Adding logic to allow it to accept pulse interrupts would remove the advantage of reduced chip count over the currently used system.

Edge or pulse triggered interrupts are essential when dealing with relatively slow interrupt sources such as relays. Otherwise the 8080 could receive and service an interrupt, and output a resetting signal to the interrupting device only to be interrupted by the same device before it has had a chance to reset itself.

8.2.5 <u>Specification of the ICU</u>:

The priority structure of the ICU is given in fig. 8.

An interrupt handling flow chart is given in fig. 9.

8.2.6 <u>Real Time Clock</u>:

The real time clock is a simple RC oscillator that interrupts the processor every 10 milli-seconds.

INTERRUPT SOURCE	PRIORITY LEVEL	RESTART INSTRUCTION	BRANCH ON INT. ADDRESS
POWERFAIL/RESTART	0	307	000
REAL-TIME CLOCK	1	317 (RST1)	010
64 ALARM INTERRUPT CHANNELS Interrupt Identification No. 0 - 63	2	327 (RST2)	020
8 ANALOG INPUT MODULE INTERRUPTS Interrupt Identification No. 200 - 207	3	337 (RST3)	030
SPARE INTERRUPT LINE	4	347 (RST4)	040
8 COMMUNICATION PERIPHERAL INTERRUPTS Interrupt Identification No. 210 - 217	5	357 (RST5)	050
SPARE INTERRUPT LINE	6	367 (RST6)	060
SPARE INTERRUPT LINE	7	377 (RST7)	070

Note: Priority 0 - highest priority

Fig. 8 INTERRUPT PRIORITY STRUCTURE

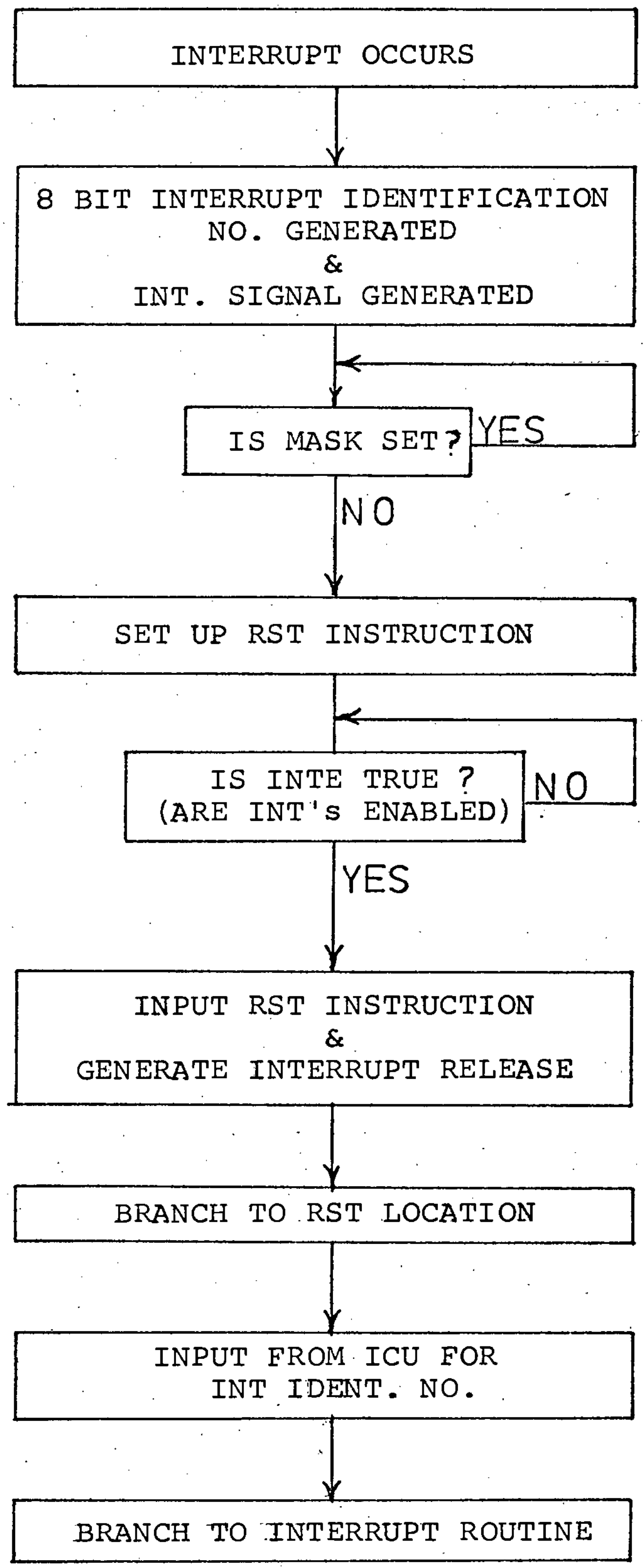


Fig. 9: SEQUENCE OF EVENTS ON OCCURANCE OF AN INTERRUPT

It is situated on the same card as the Interrupt Control Unit. It interrupts on level 1 and is hence the second highest priority interrupt (second only to power fail/restart on level 0). The reason for giving the Real Time Clock such a high priority is so that the processor will not lose time if there is a large amount of interrupt activity occurring. An interrupt from the Real Time Clock causes a branch to location 10 in memory, where the Real Time Clock driver may be found (See Chapter 13.3.6).

For an industrial process a time resolution of 10 milli-seconds was considered sufficient. Also the faster the clock, the greater the percentage of CPU time spent in handling it.

8.3 RAM MEMORY MODULE

8.3.1 Introduction:

The unpredictability of power failure in a volatile memory based system can result in a loss of irreplaceable information. All semiconductor read/write memories are volatile, i.e. information is lost when power is removed. In an industrial environment the occurrence of a "powerfail", even if it be of the nature of a short spike, is highly probable and will result in the loss of semi-conductor memory contents. In the industrialized micro-computer system most of the control program can be stored in Read only Memory (ROM) but there are many process variables and data that must be stored in RAM. Loss of these variables would disrupt the entire control program. Intel's 5101 CMOS static RAM with its extremely low standby power dissipation, typically 25µW, makes it feasible to retain information for weeks, using ordinary pen-light batteries, in a "battery standby" mode. The use of a simple battery subsystem to maintain information greatly increases the viability of semiconductor read/write memory in a process control system.

8.3.2 Organization:

The main elements of the memory module as shown in fig. 10 are :-

A. 4 kiloword x 8 bit memory block;
B. Memory interface hardware;
C. Battery backup subsystem.

4 Kiloword Memory Block:

Each memory module contains 4 kilowords x 8 bits of memory, organized in a block of 32 chips as shown in fig. 11. The chip used is the INTEL 5101-8 CMOS RAM as this was the only CMOS memory chip locally available at the time. The -8 version gives the best price/performance trade-off. They are 1000 bits/chip organized as 256 x 4 bits, hence 32 chips are required to give a 4 kiloword x 8 bit block.

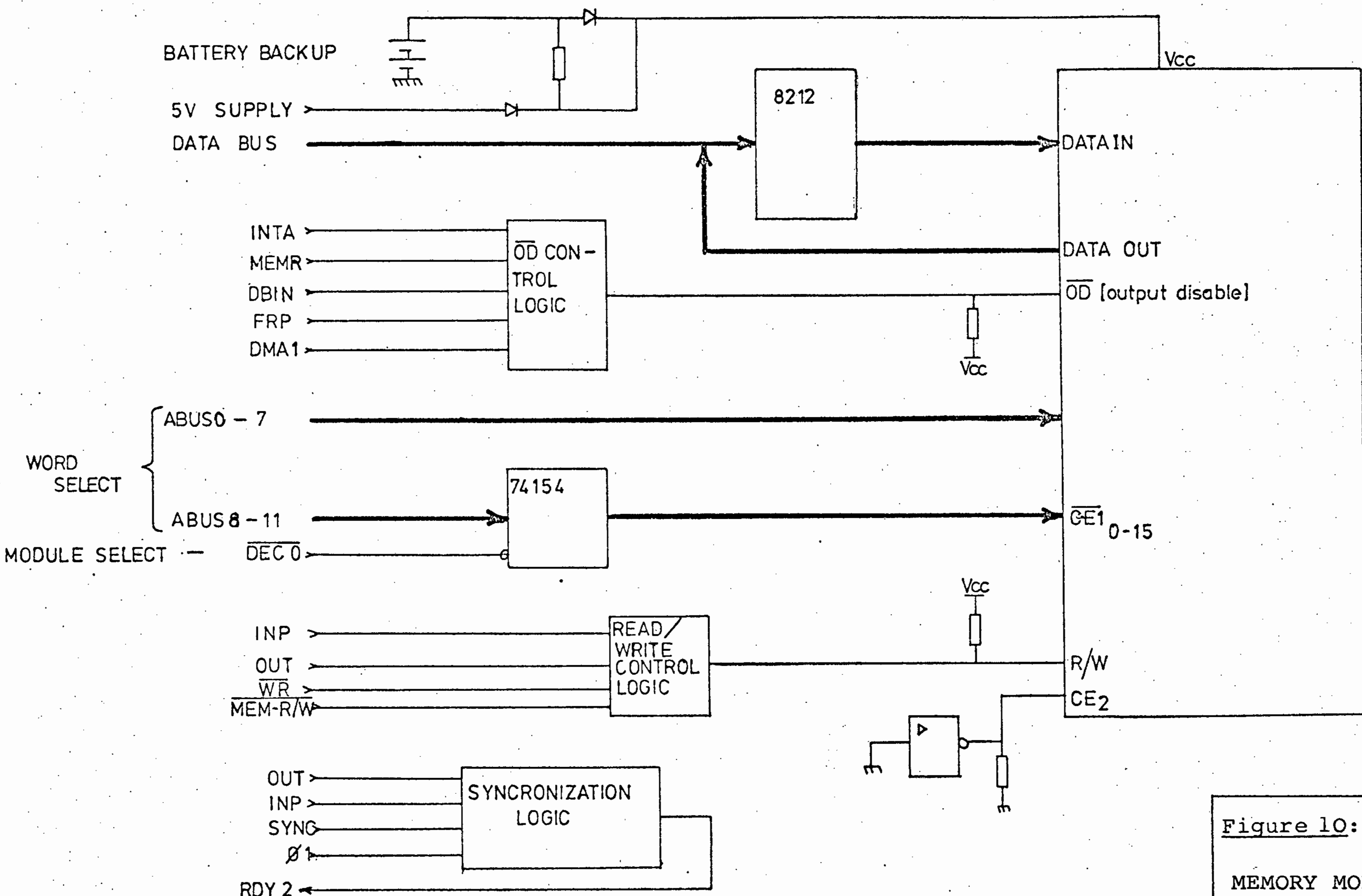


Figure 10:

MEMORY MODULE

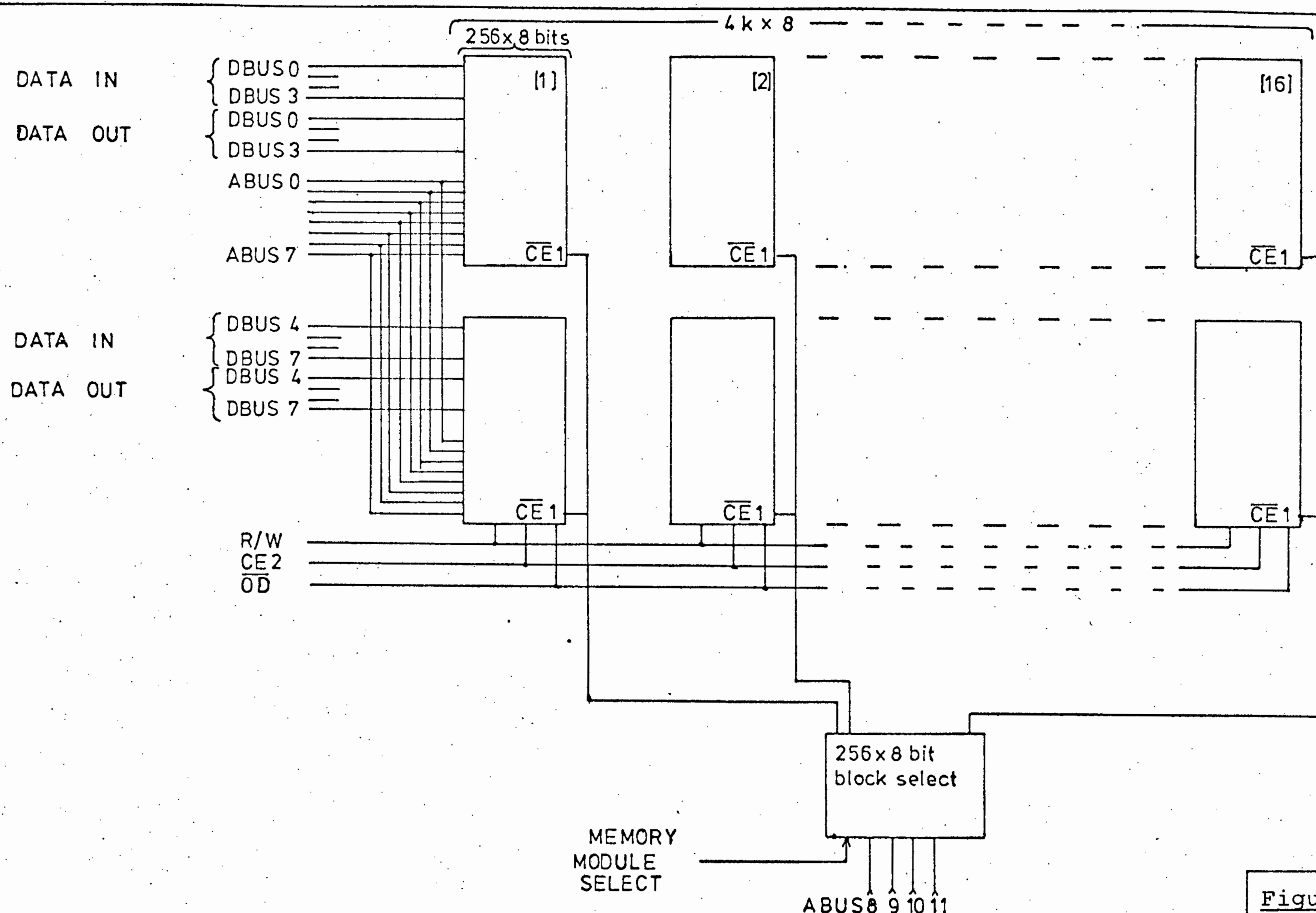


Figure 11:

MEMORY CHIP ORGANIZATION

8.3.3 Memory Interface Hardware:

Interface hardware contains data bus buffering, Read/Write control logic, address decoding and synchronization logic. The synchronization logic is required to slow the 8080 down for the memory which has read and write cycle times of 800 nSecs.

8.3.4 Battery Backup:

The battery backup system is shown in fig. 10.

The batteries used are pen light NiCads which are under continuous trickle charge. When the memory is in the "low power standby mode" these batteries can supply the memory block for a period of at least four weeks.

The 5101 has two chip enable lines. One of them, CE_2 may be used to place the memory in the ultra low power standby mode completely independent of the state of all other inputs. When this line (CE_2) is pulled LOW all internal decoders as well as input and output buffers are disabled. CE_2 is maintained in the HIGH state during normal operation by tying it to the output of an inverter that is forced HIGH. When the 5 volt supply is removed the line is pulled LOW by a pull down resistor to ground.

Other precautions taken to ensure integrity of memory contents after a power failure are as follows :-

A. The R/W line is held HIGH (Read mode) by a pull up resistor connected to the backed up 5 volt supply;

B. 20 micro F tantalum and 0.1 uF high frequency capacitors are used to decouple the supply from short switch-over spikes when the battery switches in.

C. The output buffer control line ($\overline{OD}$) is held HIGH by a pull up resistor connected to the backed up 5 volt supply.

8.4 PERIPHERAL INTERFACE UNIT

8.4.1 General:

The Peripheral Interface Unit is the card containing the interfaces to various communication peripherals. There are eight interrupt lines allowed to the PIU and since each peripheral communicates via an interrupt line, 8 peripherals are possible. In practice there may only be 4 peripherals, as a peripheral that reads and writes to the processor (i.e. TTY) utilizes two interrupts, one for reading, one for writing. On the current system only one peripheral, an ASR 33 teletype, is used as this is all that was available.

8.4.2 Teletype Interface:

The TTY interface is shown in fig. 12.

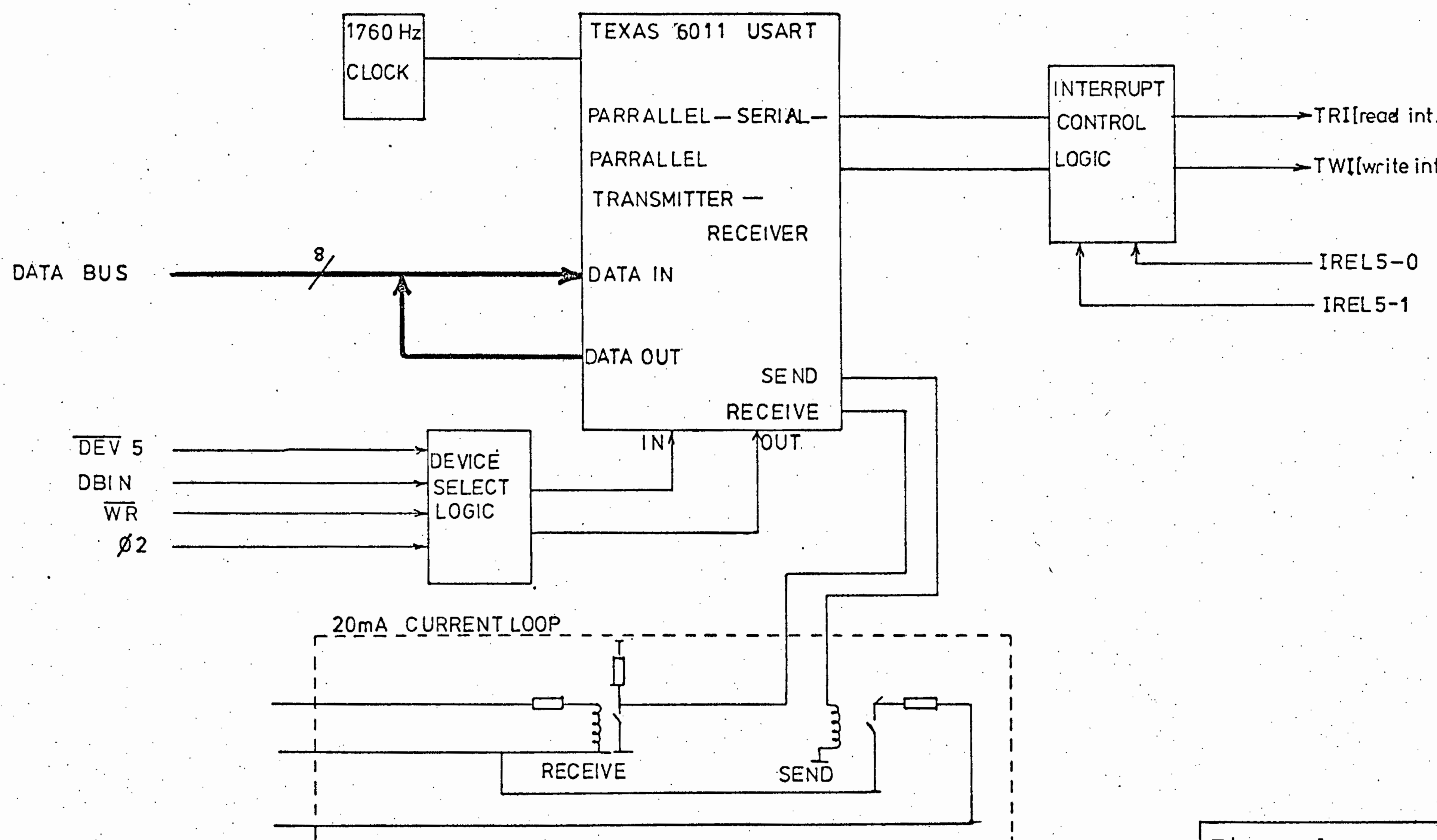


Figure 12:

TELETYPE INTERFACE

It is a parallel to serial interface utilizing the Texas 6011 USART. The link to the TTY is via a 20mA current loop. The battery to provide the current is situated in the TTY. For sending and receiving information from the TTY the current loop is broken by two relays. One for sending information, one for receiving information.
When transmitting to the TTY the 6011 USART converts the parallel data from the processor into a serial format. When receiving information from the TTY the 6011 converts the serial data into parallel data and stores it in a buffer register.

An interrupt is used to inform the processor when a word has been received from the TTY and is ready in the input buffer. Another interrupt is used to inform the processor that transmission to the TTY is complete and it is ready to accept another word. The teletype driver program (Chapter 13.3.5) handles these signals.

The TTY has been decoded as device Number 5.

CHAPTER 9.

FRONT PANEL UNIT - HARDWARE DESCRIPTION

The front panel is a plug on unit intended to be used as a hardware and software debugging aid. Once the hardware and software have been debugged, the front panel unit may be unplugged from the rest of the system and the Industrial Process controller can then run entirely on its own. Reasons for adopting this technique are discussed in Chapter 3 on the Design Philosophy. Fig. 13 shows a block diagram of the unit.

The front panel unit performs three basic functions listed below. For a detailed description on the operation and use of the front panel see Appendix D.

A. Display of Address Bus, Data bus and Control signal status:

All the above signal lines are brought out directly to the front panel unit where they

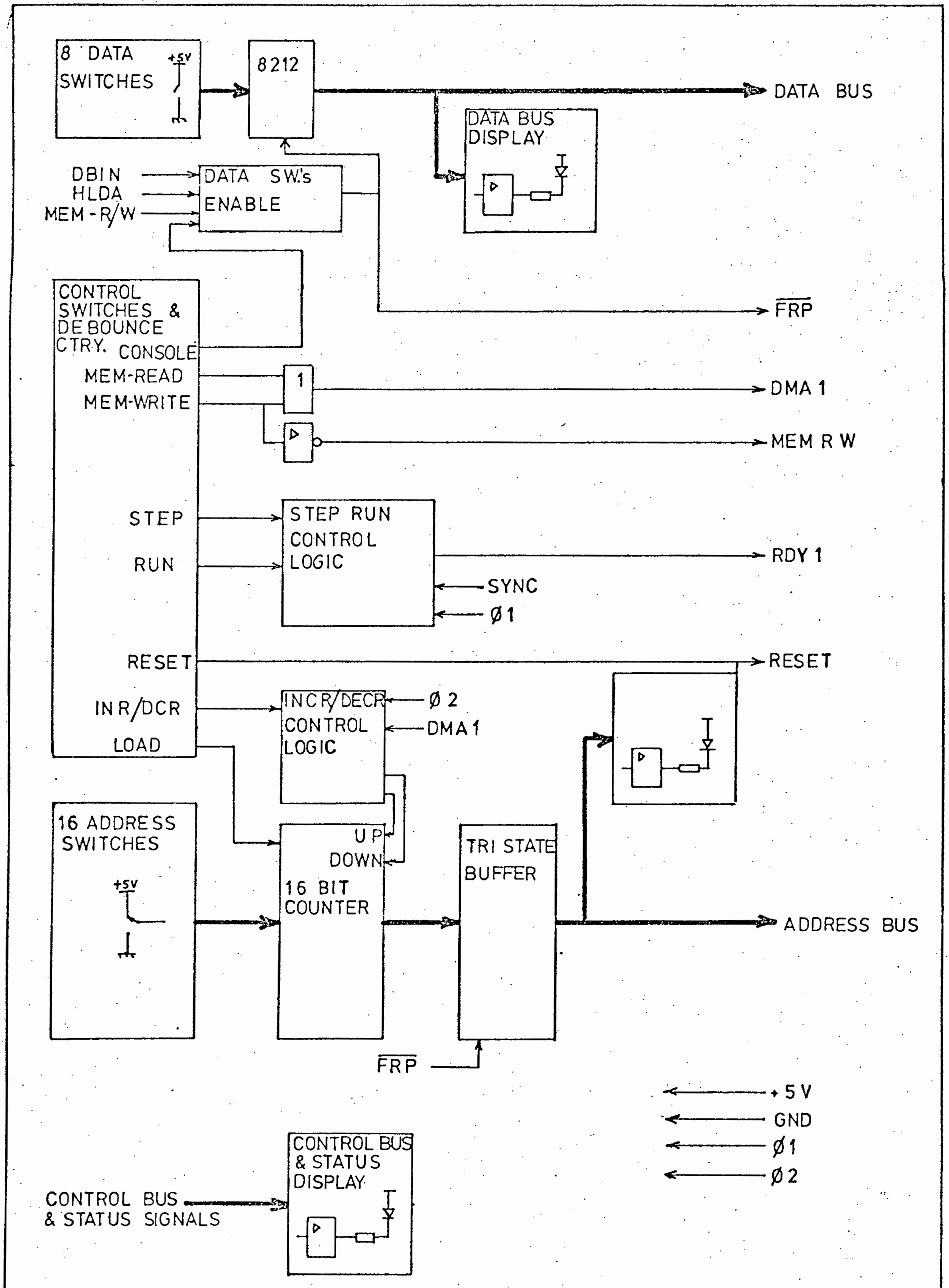


Figure 13:

FRONT PANE UNIT BLOCK DIAGRAM

are buffered to drive light emitting diods (l.e.d's) to indicate their status. The link to front panel unit is a short one (less than ½ metre) and hence no special buffering is done on the processor side.

B. Manual Control of Processor:

The processor may be RESET, STEPPED or RUN from the front panel. The reset switch basically resets the program counter to location 00 and provides the simplest means of starting the processor.

The STEP switch allows the processor to be STEPPED one instruction byte at a time. The RUN switch allows the processor to RUN.

C. Direct Memory Access Channel:

This provides a means of direct communication with the memory from the front panel unit.

CHAPTER 10.

INDUSTRIAL INTERFACE - HARDWARE DESCRIPTION

The industrial interface is distributed over six cards in the mainframe. The interface modules that have to be constructed are as follows :-

A. 16 Channel Alarm Interrupt Module;
B. 32 Channel Digital Input Module;
C. 32 Channel Digital Output Module;
D. 4 Channel Analog Output Module;
E. 16 Channel Analog Input Module (2 cards).

Detailed descriptions of each of these modules are given below.

10.1 ASYNCHRONOUS ALARM INTERRUPT MODULE

10.1.1 General:

Asynchronous interrupts are essential in the monitoring or control of a real time process. They provide the quickest response to contingent events which may occur at an unpredictable time.

The Asynchronous Alarm Interrupt Module shown in fig. 14 provides 16 individual isolated interrupt inputs with hardware priority. The system can support a maximum of four of these cards, totalling 64 individual interrupt lines. Each line is optically isolated from the process and can withstand a common mode voltage of 1.5 KV. The input signals can range between 4 and 40 volts allowing them to be driven from TTL or relays. An interrupt is generated by a positive going edge, say from 0 to 24 v. Signals originating from relays or other forms of closing contacts are de-bounced by means of filters. These filters have a time constant of 10 milli-seconds.

All interrupt lines have different priorities and this unit forms part of the second level of the hierarchical interrupt structure discussed under the Interrupt Control Unit.

If masking occurs, all interrupts are masked out and any incoming interrupt will be stored and serviced as soon as the mask is removed.

All interrupts may be manually reset from the front panel when the RESET switch is activated. This is necessary to remove any interrupts that may occur as a result of switching the system on.

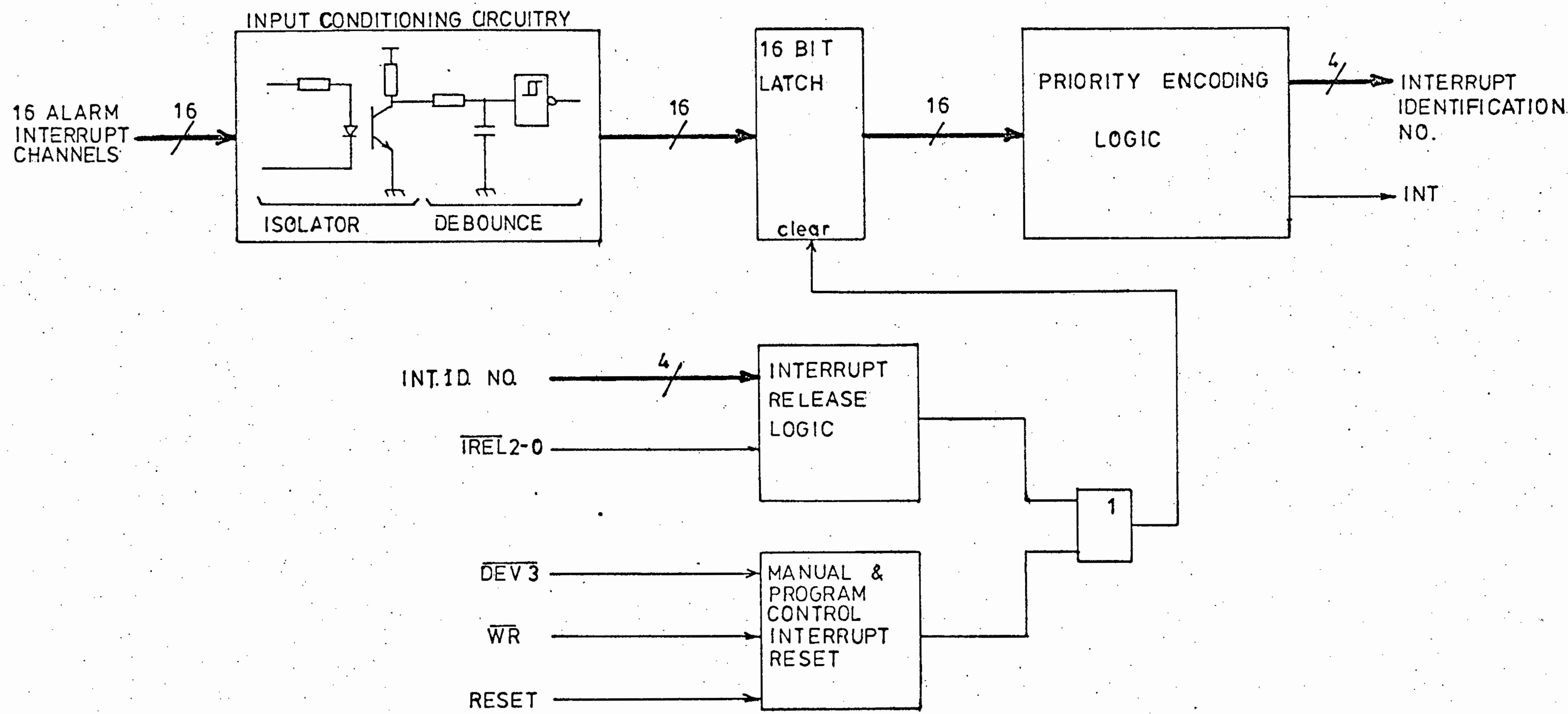


Figure 14:

ALARM INTERRUPT MODULE.

10.1.2 Circuitry:

The circuitry of the Asynchronous Alarm Interrupt Unit consists basically of input conditioning circuitry, interrupt storage register, priority and address encoding logic, and interrupt release logic and interrupt reset logic.

A. INPUT CONDITIONING LOGIC

The input conditioning logic is shown in fig. 14 and consists of an optical isolator giving 1.5 kV common mode voltage isolation and allowing input signals between 4 and 40 volts. There is also a bounce filter and a Schmitt trigger to make the resulting signal TTL compatible.

B. STORAGE REGISTER

The interrupt storage register consists of 16 flip-flops that are used to store the incoming interrupts.

C. PRIORITY AND ADDRESS ENCODING LOGIC

This consists essentially of two chips the SN74148, 8-to-3 line priority encoders. Two of them are coupled together by means of three NAND gates to give a four bit address and an interrupt request signal. If two interrupts arrive simultaneously, the address of the higher priority one is generated and remains until this interrupt is reset. Then the lower priority address is generated.

D. INTERRUPT RELEASE AND RESET LOGIC

The distinction between the release and reset is as follows :-

> After an interrupt has been accepted by the CPU an "interrupt release" signal IREL is generated which resets the appropriate interrupt. The reset is part of the manual System Reset and can be used after initial powering up.

10.2 ANALOG INPUT MODULE (Figure 15)

The industrialized microcomputer system is capable of handling eight separate Analog-to-Digital converter (ADC) units. Each unit is treated as an internal device. This means that there is decoding sufficient for 256 channels per ADC unit, - far in excess of what would be required in practice. The ADC units are interrupt based asynchronous devices. That is to say, the processor will select a particular channel and initialize the converter. The CPU is then free to continue with any other task, and when the input signal has been digitized and is ready to be inputted, the converter will interrupt the processor which can then respond when it is ready. This method of treating the ADC asynchronously via interrupts was chosen as ADC's have widely different conversion times and waiting for the ADC to complete

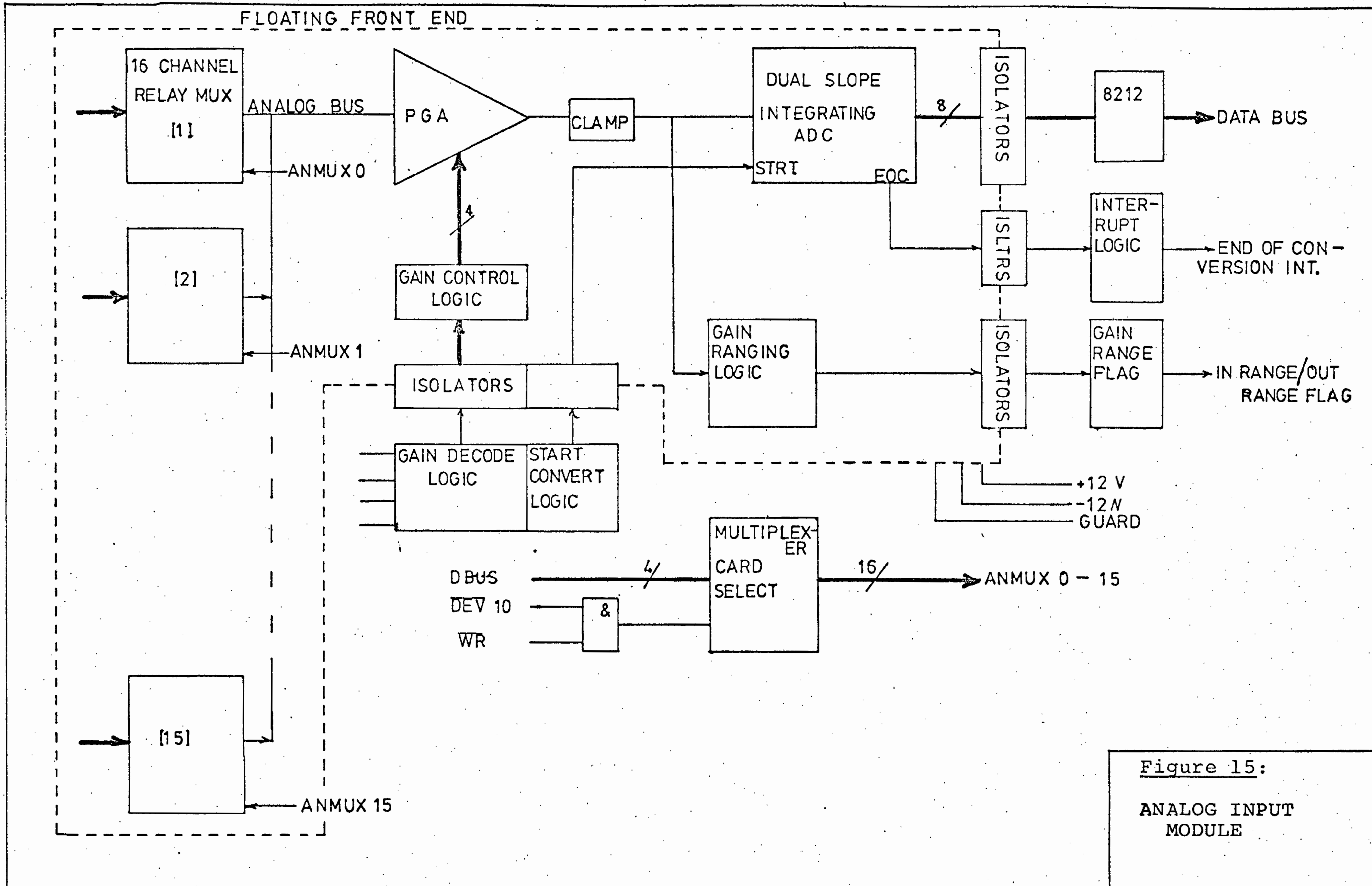


Figure 15:

ANALOG INPUT MODULE

conversion can result in large amounts of wasted CPU time.

In order to best cope with the problem of large common mode signals likely to be encountered in a noisy industrial environment the entire analog input front end is floated and takes its reference from the process to which it is connected. In this way common mode voltages of over 250 volts RMS can be tolerated.

For each ADC unit the organization is as follows:

There is one common equipment module which contains all the necessary hardware, except for the multiplexers and input signal conditioning. The multiplexer and input signal conditioning is then split up over a number of separate sixteen channel multiplexer cards feeding onto a common analog bus. The maximum extent of each multiplexer is 256 channels, i.e. 16 cards or modules each of 16 channels.

The minimal system is then a 16 channel analog input system which is contained on two cards, the common equipment module, and a 16 channel multiplexer. The system can be extended in steps of 16 channels.

The major elements of the Analog Input Module are as follows :

A. Signal conditioning circuitry;

B. A random access relay multiplexer;

C. A programmable gain amplifier (PGA);

D. A dual slope integrating analog to digital converter (ADC);

E. Isolating and latching circuitry;

F. Control logic.

10.2.1 Signal Conditioning Circuitry:

A single or double section RC filter can be used with a breakpoint at 10Hz. As most process variables have time constants far in excess of this, these filters can be used to eliminate spikes or mains frequency hum pickup on the signal lines.

10.2.2 Random Access Relay Multiplexer: (Figure 16)

Dry reed relays are used to gate the analog input signals to the programmable gain amplifier. There are three relay poles per channel. A single double pole relay gates the differential input signal and a further single pole relay is used to gate the GUARD signal. The guard signal references the floating analog input to the process. This effectively removes the common mode signal from the amplifier. The guard must be referenced to either the signal HIGH or the signal LOW at the source but must never be left unterminated.

A relay multiplexer was chosen in preference to a solid state multiplexer for the following reasons :-

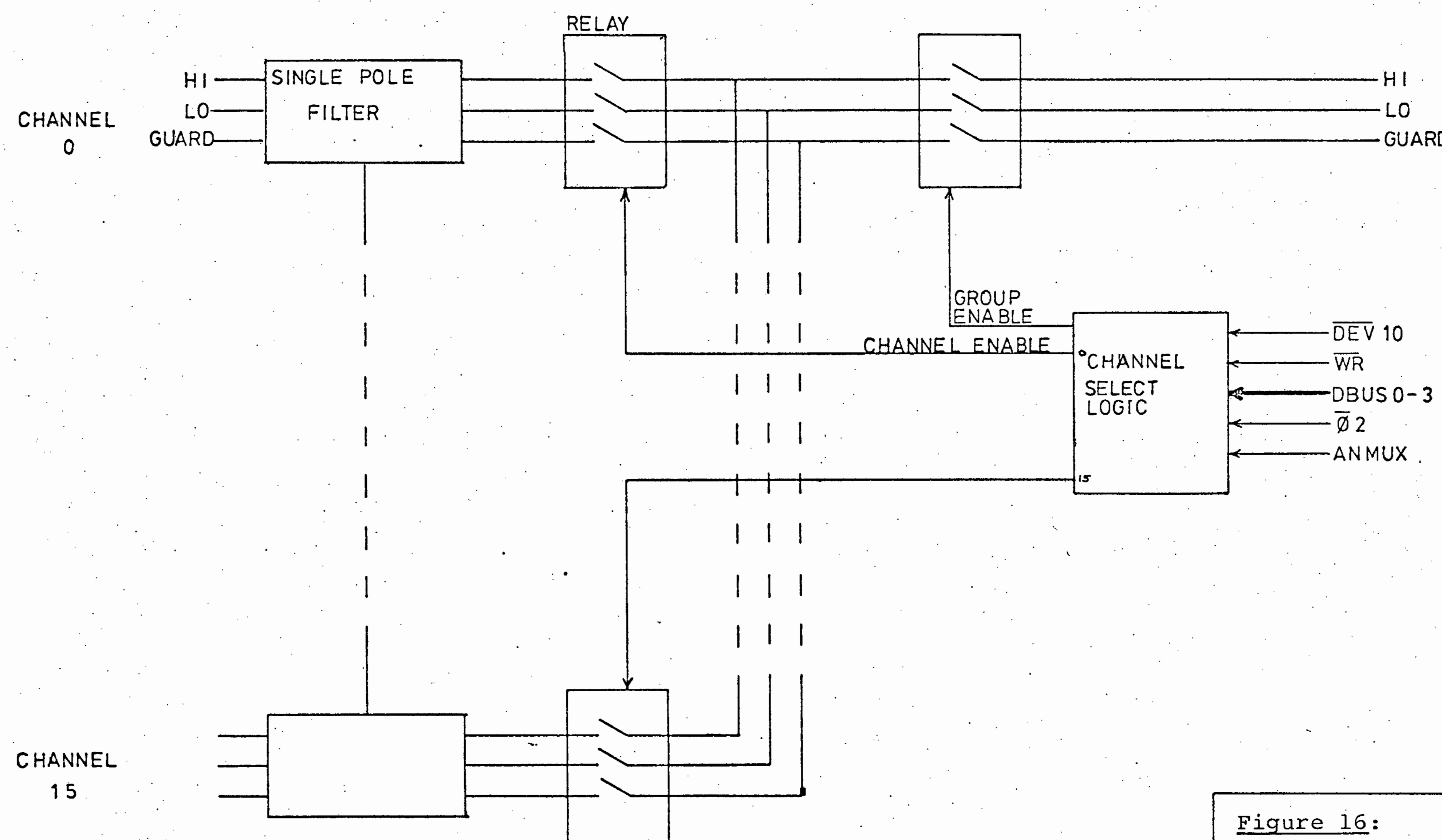


Figure 16:

16 CHANNEL RELAY MULTIPLEXER

A. Very high isolation between channels eliminates channel-to-channel crosstalk.

B. The ability to obtain very high common mode rejection by floating the entire multiplexer as it does not need a source of power as a solid state multiplexer would.

C. A very low "on" resistance and very high "off" resistance.

D. In an industrial application the limitation in switching speed in relays is not a problem.

E. A MTBF of 100 million operations gives a more than adequate lifetime for typical sampling rates in process control (usually less than 1Hz).

In an attempt to minimize hardware and obtain the best hardware/software trade-offs, settling time delays for the relay multiplexer must be implemented on a software basis. A settling time of approximately 1mS is required.

One of the most important considerations in ensuring long life in dry reed relays is proper loading. In a dry circuit (negligible current) the life of the relay will be several billion operations. However, with a differential multiplexer with high common mode voltage a problem occurs. The amplifier input has a shunt capacitance to ground due to its construction. The capacitance is charged by the common mode source through the multiplexer relay. Experience has shown (ref. 11) that this capacitive charging current can reduce reed relay life drastically. Hence, the small resistor that has been placed in series with the contacts limits this current and may extend the life of the relay.

Another type of multiplexer configuration considered was the flying capacitor multiplexer (See Ref. 12). This method was rejected as it is a form of sample-and-hold and the value obtained at the time of channel selection is an instantaneous one and hence the advantage of using a dual slope integrating ADC (see Chapter 10.2.4) are lost.

10.2.3 <u>Programmable Gain Amplifier</u>:

Fig. 17 shows a simplified block diagram of the PGA. The amplifier is a differential input direct DC coupled amplifier that is isolated from system ground and can be referenced to the source by a floating guard shield. Input and output control signals are coupled to and from the amplifier by optical isolators. The continuity of the guard shield is maintained through the amplifier to its output where it is connected to the input of the ADC.

The amplifier is a two stage amplifier. The first stage is a differential input to single ended output buffer amplifier having unity gain, and capable of operating with 100 volt common mode signals. The second stage controls the gain.

Input overvoltage protection is provided to prevent overloading the input to the amplifier.

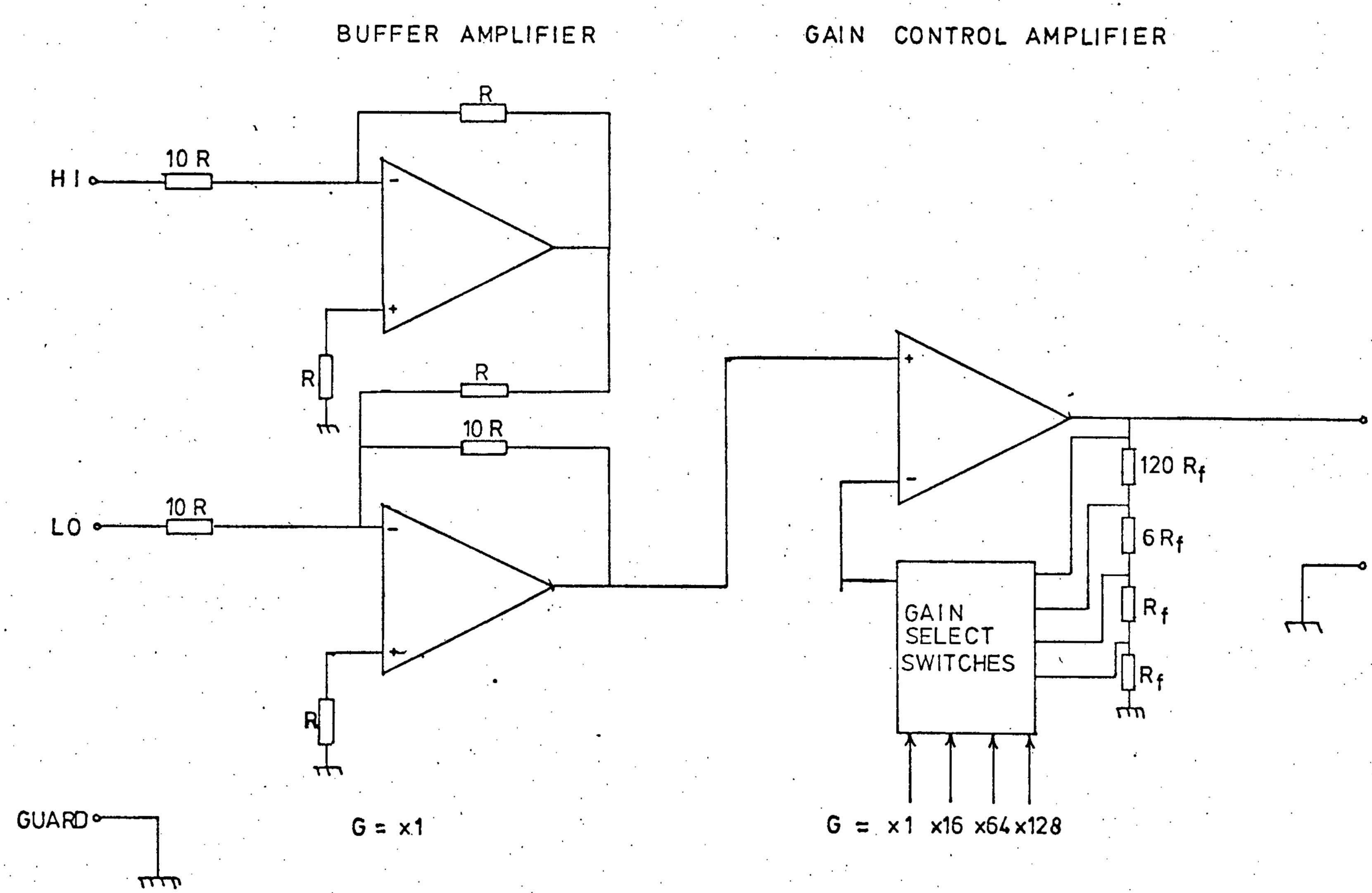


Figure 17:

PROGRAMMABLE GAIN AMPLIFIER

There are four possible gain ranges which may be randomly selected. These are gains of 1, 16, 64, 128. The full scale output voltage is $\pm$ 1 volt. This is a limitation imposed by the ADC. Hence maximum input voltage is $\pm$ 1 volt. The minimum voltage difference which the ADC can detect is 7.8 mV. Thus with a gain of 128 the maximum sensitivity of the system is 7.8/128 = 61 micro V. The gain ranges that are used were chosen to simplify scaling of the signals within the processor. Division or multiplication by these values amounts to simply shifting left or right a number of bits. (They can be expressed as integer powers of 2).

Gain ranging is done under software control in the following manner:

When a channel is selected, the highest gain (128) for the amplifier is also selected. If the output signal is greater than $\pm$ 1 volt the IN RANGE/OUT RANGE comparitor will set a hardware flag which is examined by the processor. The next lowest range is then selected and the same procedure repeated. This is repeated until the highest gain is found for which the signal is within range. The ADC may then be initiated and conversion begins. This method of gain ranging was chosen in preference to a fully hardware orientated gainranging system in which the ranging is done automatically by the hardware as soon as the channel has been selected. This again represents an effort to obtain an optimised hardware/ software trade-off in which CPU time is better utilized with a saving in hardware. This is in fact the basic principle of micro-processors in which hardware logic can be replaced by software logic. The extra time required to do the gain ranging by software (approx. 100μS) is insignificant compared to the total time required for conversion (approx. 100mSecs).

As low cost OP-AMP's have been used in the construction of the PGA, offsets do exist. These can be trimmed to zero for any one particular gain range, but not for all. However, when used with a microcomputer this effect is not a problem. The offsets at any given time can be read by the computer by using one channel as a calibration channel. The offsets that exist can be noted and subtracted from the values read for each particular gain. This allows a low cost amplifier to be used without any real sacrifice in accuracy.

10.2.4 Dual Slope Integrating Analog-to-Digital Converter:

The ADC used is a Datel ER8B eight bit dual slope integrating ADC. The ADC is powered from a floating supply that is referenced to the floating guard line which is extended through from the programmable gain amplifier. Control signals to and from the ADC are isolated from the system ground by means of optical isolators.

The purpose of the ADC is to convert analog signals within the range $\pm$ 1 volt to an eight bit digital word which may then be inputted to the microcomputer.

The operation of a dual slope integrating ADC is described in Appendix E.

Reasons for using a dual slope integrating ADC are as follows :-

A. The integration period can be set to correspond to one 50Hz cycle. This results in a high rejection of 50Hz hum or any components of 50Hz.

B. As the signal that is digitized is the average value of the input voltage over the integration period the effects of any high frequency noise is greatly reduced.

C. A sample-and-hold amplifier is not required to "latch" the analog input at the time of conversion. High quality sample-and-hold amplifiers are expensive items.

10.2.5 Isolating and Latching Circuitry:

The digitized analog input is isolated by means of optical isolators from the system ground. The eight bit digital word is latched into a tri-state latch feeding onto the data bus.

10.2.6 Control Logic:

Control signals to and from the floating analog input module are isolated by means of optical isolators. There are three important control signals.

A. IN RANGE/OUT RANGE FLAG

This is a hardware flag used to indicate whether the output voltage from the PGA is in the range $\pm$ 1 volt. A dual comparitor is used as shown in Appendix F. The status of the flag is latched and can be read by inputting from device 10. If the output is out of range the flag status is 0. In range the flag status is 1.

B. START SIGNAL

The START signal is used to initiate conversion on the analog-to-digital convertor. As the START signal, which is a positive going pulse must be coupled through an optical isolator, it must have a duration of at least 50 micro S owing to the limited bandwidth of the optical isolator. A 130 micro S pulse is used and is achieved by means of a monostable.

C. END OF CONVERSION SIGNAL

The END OF CONVERSIONS (EOC) signal occurs when the analog signal has been converted and the digital data is ready in the output buffer. The EOC signal is used to generate an interrupt to the processor. It is also optically isolated from the rest of the system logic.

10.3 ANALOG OUTPUT MODULE

The analog output system shown in fig. 18 offers a method of satisfying a large number of process control requirements. Applications such as :-

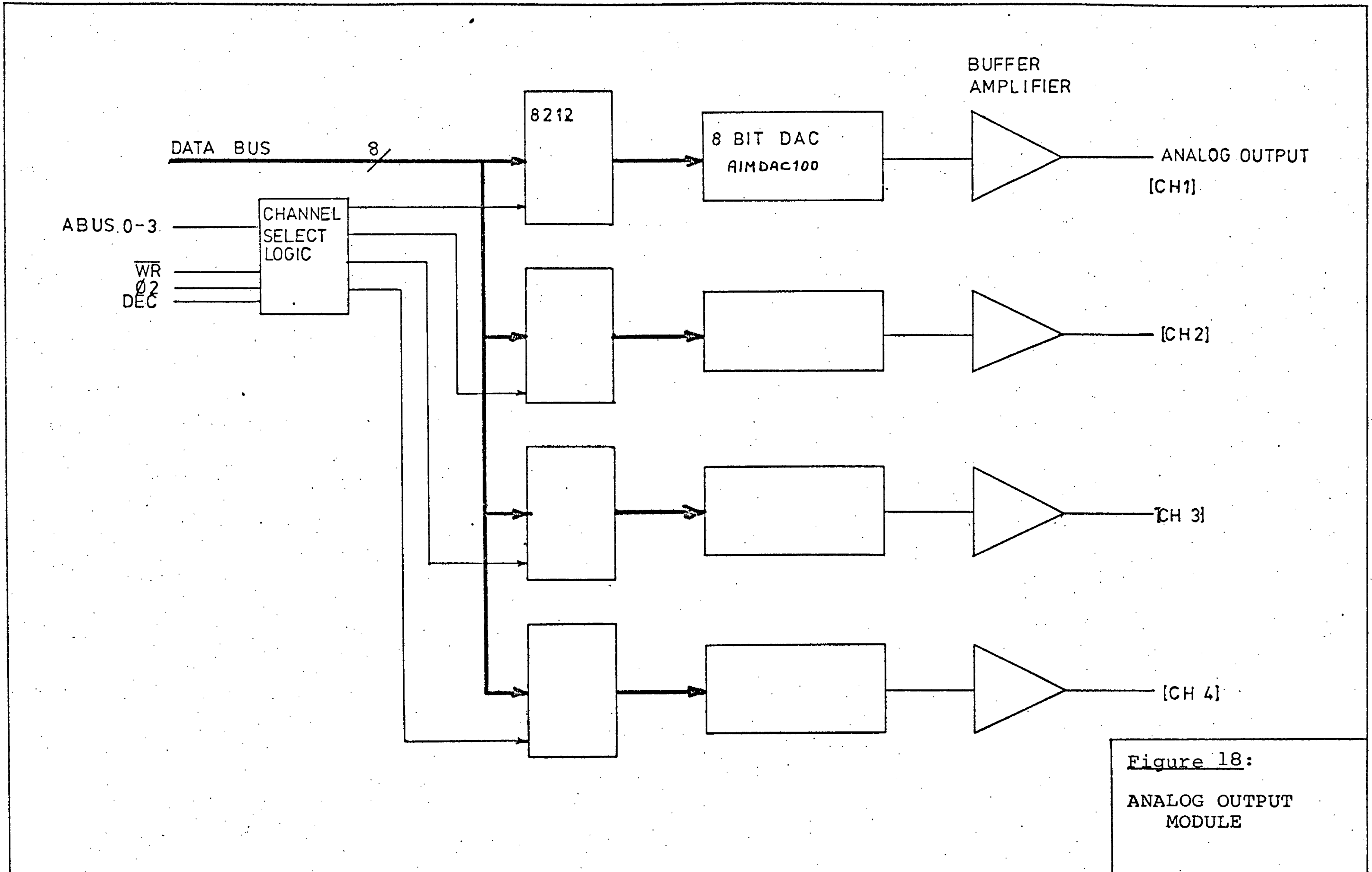


Figure 18:

ANALOG OUTPUT MODULE

A. Digital-Analog interface for systems that perform hybrid computations;

B. Direct digital control of analog processes;

C. Digital controlled test functions that require analog voltage inputs;

D. Drives for display, meters, plotters and oscilloscopes.

The analog output module is based on an eight-bit digital-to-analog converter. There are four analog channels per module and the system is capable of addressing a total of 224 channels.

There are two possible output configurations.

A. VOLTAGE OUTPUT:

A full scale range of $\pm$ 4 volts is provided. This range was chosen so as to give a convenient scaling factor (1/4) for signals that have been received via the analog input system which has a full scale range of $\pm$ 1 volt. Multiplying or dividing by four is easily achieved digitally by shifting two bits left and right respectively. The voltage outputs are short circuit protected.

B. CURRENT OUTPUT:

An industrial standard 4-20 milliamp current output can also be used, utilizing the National LH0045 two wire transmitter (Ref. 19).

The circuitry of the analog output module consists basically of :-

A. An eight-bit latch;

B. a ten-bit digital to analog converter (DAC) of which only eight bits are used;

C. Either a buffer amplifier giving a full scale voltage of $\pm$ 4 volts or a voltage to current converter giving 4-20 milli-amp output;

D. Channel selection logic.

10.3.1 Architectural Considerations:

There are basically two possible ways of achieving a multichannel analog output system. See fig. 19.

A. UNIQUE DAC PER CHANNEL

In this configuration there is a unique DAC per analog output channel. Data is stored in the digital mode in a latch. The latches are all fed in a multiplexed fashion off the data bus. This method is most suitable when there are long delays between updating of the analog output, as there is no loss or leakage of the signal as it is stored digitally. The practical feasibility of this method relies on the availability of low cost DAC's as a DAC is required for each channel.

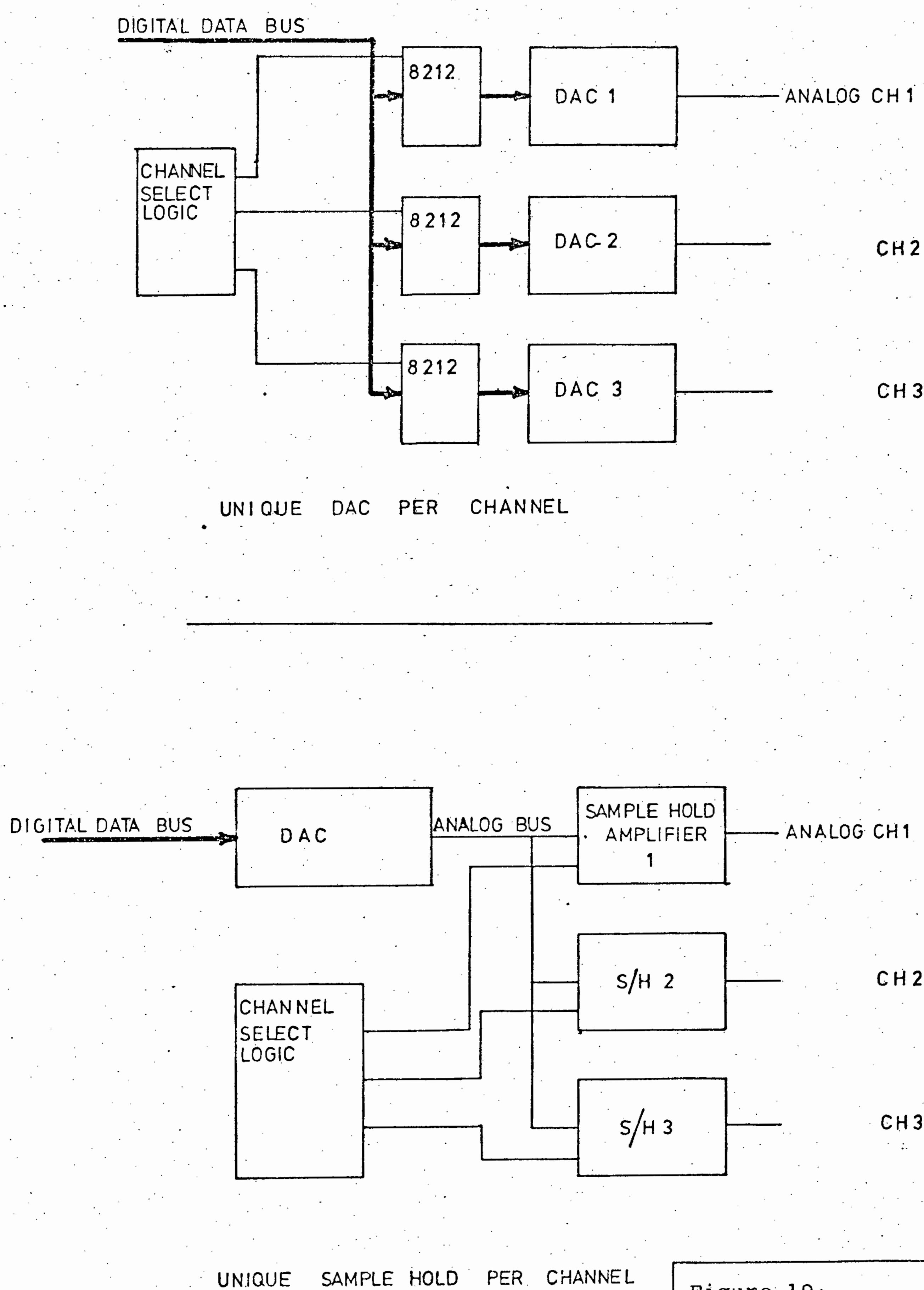


Figure 19:

ANALOG OUTPUT
MULTIPLEXING

B. UNIQUE ANALOG SAMPLE AND HOLD PER CHANNEL

In this configuration there is one DAC feeding directly off the data bus to all channels. The analog output of this DAC is then multiplexed via a number of Sample-and-Hold elements. The multiplexing and storage of analog data between updates is done on the analog level in this case. This method is most suitable where the analog output data is updated relatively frequently and hence any droop in the Sample-and-Hold element is trivial. This method of multiplexing is most useful where an ultra high accuracy and hence expensive DAC is required as only one DAC is required.

In the present system the unique DAC per channel method was used for the following reasons :-

A. Low cost DAC's were readily available;

B. Ultra high accuracy DAC's were not necessary for the required applications;

C. The relatively high cost of Sample-and-Hold elements.

10.3.2 Isolation Consideration

The analog output module is the only part of the Industrial interface that is not fully isolated from the rest of the system. The reason for this is that there is no really elegant method of isolating an analog output and still maintaining good accuracy and linearity. Optical isolators are far too non-linear, and although linearization techniques do exist, the linearizing circuitry itself needs to be powered from a stable source which is isolated from the system.

Ideally what is required is a separate transformer decoupled regulated $\pm$ 12 volt supply per channel with the supply referenced to the point in the process to which that analog output is connected. This means a separate transformer and supply per channel and with four channels per card, this is impractical.

A partial solution would be to have a separate supply per card, i.e. per four channels. This imposes the restriction that all analog outputs must run the same route to approximately the same point in the process so that any noise pick-up will be the same on all lines.

As neither of these solutions is particularly satisfactory neither was adopted. Instead the outputs are protected from spikes by "transtectors" (very fast switching zener diodes) which can absorb large current spikes for a short duration, as well as a fuse for any longer term overloads.

10.4 DIGITAL INPUT MODULE

The digital input module shown in fig. 20 provides 8 bit word based digital input capability. Each module contains four eight bit channels, i.e. 32 bits per card. The system is capable of addressing up

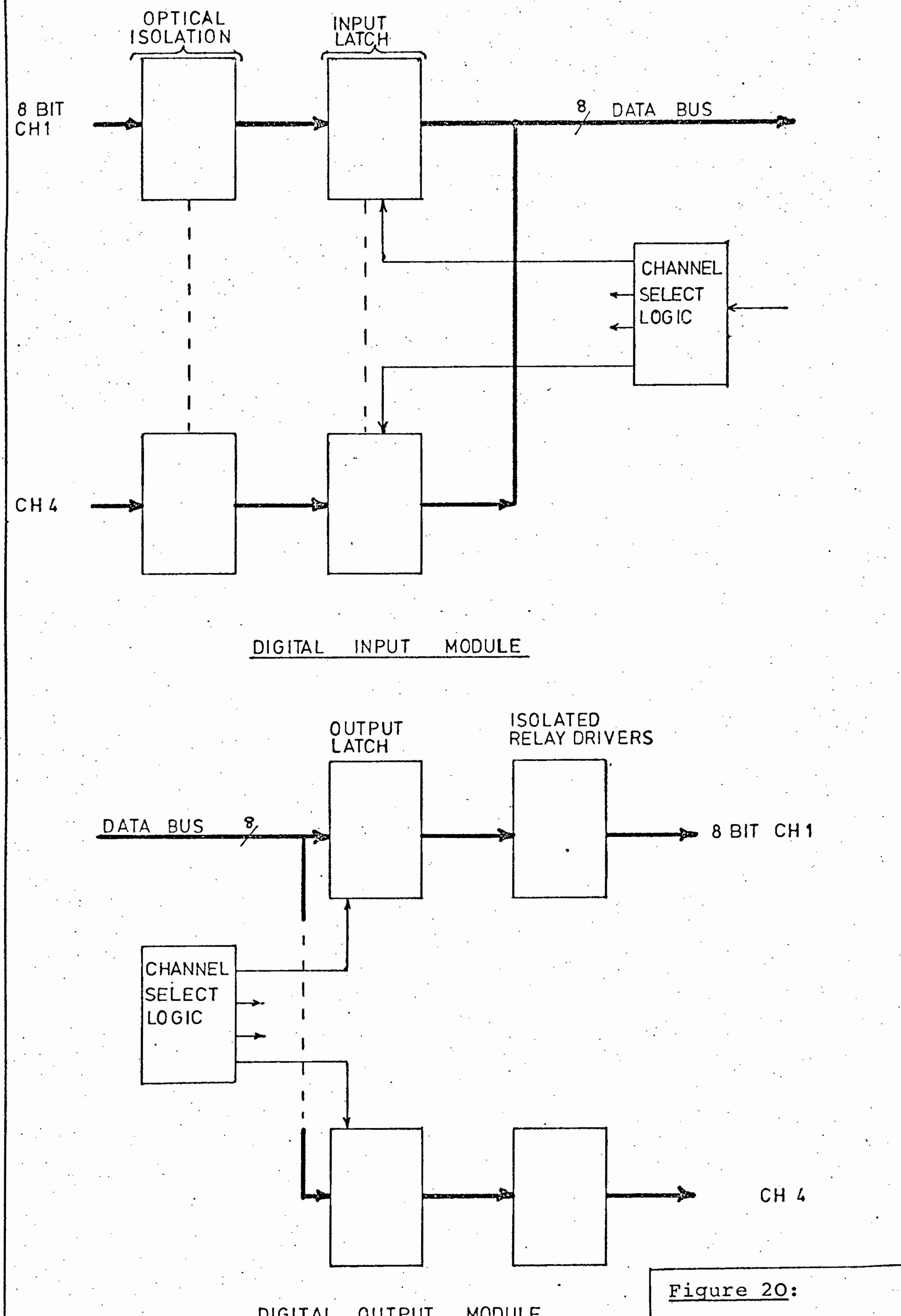


Figure 20:

DIGITAL INPUT/OUTPUT MODULES

to 224 eight-bit digital input channels, i.e. 1792 bits on 56 cards. Each bit is optically isolated and capable of withstanding 1.5kV of common mode voltage. Digital input signals can range from 4 to 40 volts hence allowing for TTL (equivalent to 10 TTL loads) or relay sources.

The digital input channels are not asynchronous but are scanned under program control at desired intervals. When any channel is scanned, the current status on the input lines is latched and inputted to the computer for comparison with desired values.

As the digital input channels are scanned at times determined by the software and not by the actual opening or closing of a relay contact as in the case with the Alarm Interrupts, no switch debouncing filters have been included as they are now unnecessary. The lines are protected against high frequency spikes, such as from TTL switching, by the natural frequency limitation (20kHz) of the optical isolators.

The circuitry of the digital input module consists of the following elements :-

A. Input conditioning:
Optical isolators give 1.5kV common mode isolation.

B. Data Latches:
Four 8 bit tri-state latches latch the data for the various channels and feed it to the data bus when a particular channel has been addressed.

C. Channel Selection Logic:
This provides an on card decoding of a part of

the address bus to give one of four "enable" signals to one of the four digital channels being addressed.

10.5 DIGITAL OUTPUT MODULE

Refer to fig. 20.

The digital output modules provide 8 bit word based digital output capability. Each module contains four eight bit channels, i.e. 32 bits per card. The system is capable of addressing 224 eight-bit digital output channels, i.e. 1792 bits on 56 cards. Each bit is optically isolated and capable of withstanding 1.5kV of common mode voltage. There are two output configurations.

A. RELAY DRIVER:

The output configuration is shown in Appendix F. The external supply to activate the relay coil is supplied by the user. The output transistor then switches this supply in or out to control the relay. The output can handle up to 50 volts and up to 500 mA and hence is compatible with most industrial relays.

B. TTL COMPATIBLE OUTPUT

This configuration is obtained by internally strapping the transistor to the 5V rail of the micro-processor, thus providing TTL level outputs to a system that has a common ground to the processor. This is useful for controlling external logic where an external 5V source to power the output is not available. The maximum clocking frequency for the digital output channel in this configuration is limited by the switching speed of the optical isolator to 20 kHz.

The circuitry of the digital output module consists of four eight-bit data latches, address decoding and various forms of output drive as mentioned above.

CHAPTER 11.

POWER SUPPLIES

For a process controller operating in an industrial environment the power supply is the most critical subsection of the system and its immunity to power-line transients and power dips (brownouts) is the single most important factor affecting the overall integrity. The power supplies can also represent the greatest single cost in the system. Bearing these two factors in mind considerable care must be taken in organizing power supplies so as to obtain an optimum price/performance ratio.

If cost were of no relevance a dedicated motor-generator set per industrialized microcomputer system would be the ideal solution. However, the excessive costs involved render this solution unrealistic.

A number of alternative supply configurations that have been considered are discussed below.

11.1 COMPLETE BATTERY SUPPLY (Figure 21 A)

In this case the complete processor is powered by a battery and is never directly connected to the mains supply. Two batteries and a switch-over network

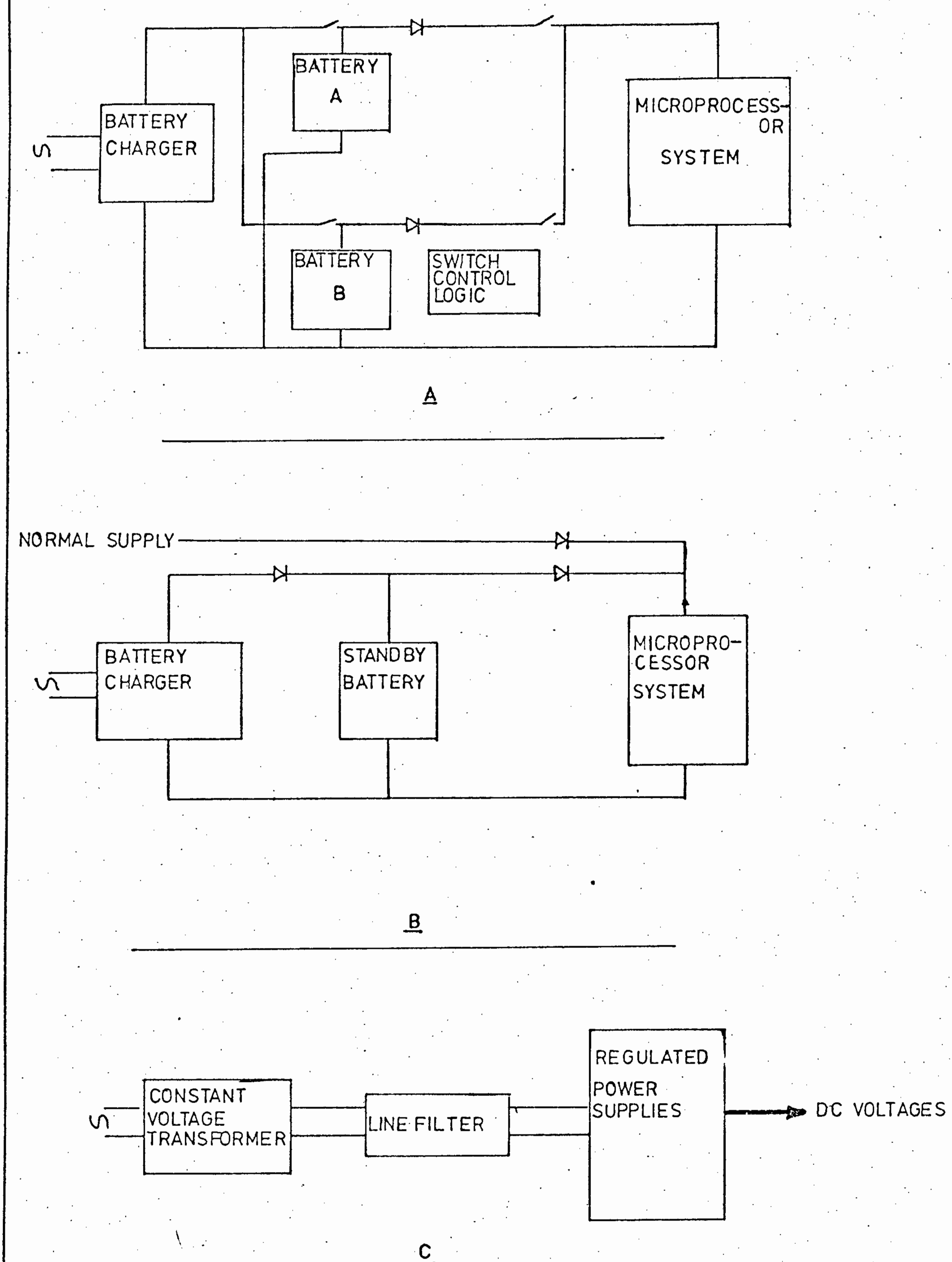


Figure 21:

POWER SUPPLY OPTIONS

would be required, one to supply the processor while the other is being charged. Operation would be as follows :

Battery A is connected to processor, B is charged. When A has discharged by a specified amount, B is first disconnected from the charger and connected to the processor. A is then disconnected from the processor and connected to the charger. In this way there is never a direct link from processor to mains supply.

Advantages:

A. Complete mains isolation;

B. Processor can operate even after a power failure. This could be useful for taking emergency measures during such an event.

Disadvantages:

A. Large amount of maintenance is required in battery upkeep, as well as replacing batteries after a finite number of cycles;

B. Fairly large batteries would be required so that the battery being charged would be fully charged before the battery being used has discharged.

This system was rejected on the basis of the above disadvantages as well as the fact that it is most often unnecessary to maintain power to the processor after the process has shut down due to a power failure.

11.2 STANDBY BATTERY SUPPLY (Figure 21 B)

In this configuration a battery is charged continuously from the AC mains. The battery is connected to the processor and switches in if the power fails. A variation of this configuration would be to have an inverter between the battery and the system. The inverter would then generate 220 volts A.C. which could be fed to the processor power supplies.

Advantages:

A. Good isolation from mains dips (brownouts);

B. The processor can operate for some time after a power failure. Power failures of a short duration would go unnoticed and the powerfail/ restart routine would be greatly simplified.

Disadvantages:

A. It has the same disadvantage as in the previous case of careful battery maintenance. This makes operation in inaccessible places for extended periods difficult.

11.3 REGULATED AND FILTERED AC MAINS SUPPLY (Figure 21 C)

This is the system that has been used in the industrialized microprocessor system. The supply is derived directly from AC mains. Protection against the vagaries of supply line noise are as follows :-

A. Constant Voltage Transformer: (See Appendix H)

(1) This gives good regulation against AC dips and when used in conjunction with a regulated power supply, DC supply can be maintained for AC drops as low as 100 volts;

(2) As the transformer is saturated at 220 volts, transient spikes in the supply will not pass easily through to the secondary;

(3) The only disadvantage of the CVT is that it is frequency sensitive. Any large deviations from 50Hz can cause the secondary voltage to drop.

B. Line Filters:

(1) A single pole filter with a breakpoint at 15 kHz is used to filter any high frequency noise from the supply line;

(2) After the rectifiers in the regulated power supplies, high frequency capacitors were added to the existing large electrolytic capacitors.

C. Regulated Power Supplies:

These were used to obtain ± 5 volts and ± 12 volt supplies. A further separate ± 12 volt supply is used for the floating analog input system. Large electrolytic capacitors just before the regulators are used to maintain power, after a power failure, long enough for a power-fail/restart routine to be executed.

D. Powerfail/Restart:

A powerfail/restart routine is the only safeguard against complete power failures. After a "power fail" has been detected the routine can be entered and the processor is shut down in an orderly fashion with all required variables stored in RAM memory with battery backup. Once the power has been resumed the "restart" part of the routine reloads the variables and begins operation again.

CHAPTER 12.

ENVIRONMENTAL ISOLATION

12.1 GENERAL

A typical control computer uses ambient air as the primary coolant for internal circuit components and electromechanical devices. Air from the ambient environment is introduced into the unit enclosure, routed to the internal component to be cooled by natural or forced convection, and is then exhausted to the room or computer area. Both the ambient air and airborne contaminants are thus brought into intimate contact with the internal functioning components of the computer system. In most computer systems, control of the basic air properties is therefore essential if satisfactory system performance and life are to be attained. This control is achieved by means of air-conditioning which is the control of specific air quality including its temperature, water content, contaminant level.

12.2 EFFECTS OF AIR PROPERTIES

Each of the basic properties of the air found in the industrial environment can cause temporary or permanent damage to electromechanical or electronic components and subassemblies. The effects of temperature, humidity and contaminant level are discussed below.

12.2.1 Temperature Effects:

Both electrical circuit parameters and dimensional stability of mechanical components are affected by changes in ambient temperature. These effects are often reversible when specified limits are not exceeded. The most prevalent effect of thermal stress on electronic components is a change in circuit impedance which can drastically affect the system accuracy especially in the analog subsystem. However, the most significant effect of thermal stress is the inverse relationship between component life and temperature. This is especially significant in a low maintenance system.

12.2.2 Relative Humidity Effects:

The effects of relative humidity of the ambient air are usually subjunctive, that is, the cause and effect relationship is usually indirect. Actual changes in relative humidity cause very small changes in circuit parameters. More important are sustained humidity levels in the range 0-20% and/or 60% and higher.

In the 0-20% range static electrical charges can easily be built up when contact is broken or friction exists between two surfaces. System malfunction can then be caused by the coupling of spark energy into electronic circuits.

In the 60-95% range the effects on airborne contaminants that are soluble in water or desiccant materials (absorb moisture) become pronounced and can cause severe corrosion of metal contacts. Another result of excessive humidity is degradation of common mode rejection performance as a result of reduced leakage impedances in the analog input subsystem.

12.2.3 Airborne Contaminants:

There are two categories of airborne contaminants, particulates and corrosive gases. The latter are extremely common in industrial processes and the former, when combined with a high humidity can also form corrosive solutions. The result of both of these is extreme corrosion of metal contacts such as edge connectors, and the degradation of insulating materials.

12.3 THE SOLUTION ADOPTED

The Industrialized Microprocessor System is designed to operate as close to the process as possible and hence will not have the protection of an air-conditioned computer room to protect it from the environment. An alternative solution, that has been adopted to protect the system has been to house it in a completely sealed crate. This solves the last two problems mentioned above, i.e. relative humidity and airborne contaminants, but aggravates the problem of cooling.

An attempt has been made to keep the general cooling requirements to a minimum by the use of Low Power Schottky logic wherever possible.

In order to maintain the system as close to ambient temperature as possible and to prevent hot spots from occurring anywhere within the crate, a number of precautions have been taken. There are two fans inside the sealed crate. They are used to circulate the air for two reasons. Firstly, so that no hot spots occur in the crate, and secondly, so that the moving air continually comes in contact with the walls and especially the roof of the crate. It is through the walls and roof of the crate that the main dissipation of heat occurs. The roof of the crate is made up of finned heat-sink to aid heat dissipation. The heat is transferred to the roof and walls by conduction and then radiated to the atmosphere. In order to facilitate the radiation the crate can be spray painted mat black. Naturally this only works in the situation where the ambient temperature is lower than that within the crate. If the system is operating in a very high ambient temperature a shiny reflective surface would be most suitable. In these conditions some sort of refrigeration would be necessary such as the use of thermoelectric heat pumps. Heat pumping at more than 200 BTU/hr is possible with a single thermoelectric element (ref. 9).

SECTION III.

SYSTEM SOFTWARE

CHAPTER 13.

SYSTEM SOFTWARE

13.1 SOFTWARE OBJECTIVES

The industrialized microprocessor system is intended to be a generalized industrial instrument capable of operating in any industrial process. As a result the writing of specific application software is not a part of this project. The software written must be purely to demonstrate that the system is capable of supporting such specific application programs and that the hardware is capable of executing them.

Details of the software system used for the development of the routines described below can be found in reference 10.

Source programs were prepared using the MOS EDIT routines on the Varian 620i mini computer and assembled using a Fortran based cross assembler to produce an object tape of 8080 machine code. These object tapes were then loaded into the microprocessor system via a teletype reader.

In order to demonstrate the viability of the system two types of software routines have been written. They are :-

A. General Utility Routines;

B. Hardware Driver and Exerciser Routines.

The utility programs are situated at the top of memory. The first 100 (octal) locations are devoted to interrupt handling. The space between these is used for the general programs. A memory map is shown in fig. 22.

A general description of the routines is given below.

13.2 GENERAL UTILITY ROUTINES

These are programs which facilitate the handling of software in the processor. They are not actually part of its function as an industrial controller/data logger, but are essential in making the pure hardware a viable intelligent system. These utility routines allow programs to be loaded into the processor and debugged and run from the teletype. The routines developed are as follows :-

A. Bootstrap Loader:
This loads the Binary Loader into the microprocessor from the teletype.

<u>Contents</u>:	<u>Location</u>:
BOOTSTRAP	
	3715
BINARY LOADER	
	3500
8080 AID ROUTINE: FAID	
	1550
TTY DRIVER	
	1500
GENERAL PROGRAM SPACE	
	0100
INTERRUPT HANDLING	
	000

Fig. 22 MEMORY MAP.

B. Binary Loader:
This routine loads any program into the processor.

C. 8080 AID System:
This is an AID type debugging program giving complete access and control of any program in memory from the teletype.

General descriptions of these programs are given below.

13.2.1 Bootstrap Loader:

The main bulk of this program is located in the top 40 locations in memory and is loaded via the front panel DMA channel. There is also a teletype handling routine in locations 50 to 57 and program initialisation in locations 0 to 10.

The object of the Bootstrap is to have a short program that can be easily loaded manually into the processor. This program will then read in the unformatted Binary Loader program. In order to keep the Bootstrap as short as possible no error checking is done and the Binary Loader tape is in an extremely simple format. Once the Binary Loader has been loaded into memory it can be used to load larger programs which have the normal Assembler output format and with error checking.

13.2.2 Binary Loader:

This program is loaded by the Bootstrap from the teletype into memory and occupies the 204 (Octal) locations below the Bootstrap. The object of the Binary Loader is to load programs from the teletype reader into memory. The Binary format of these paper tapes are the output format of the Macro - Assembler MAS (ref. 10). Normal parity error checking is performed on the loading of these tapes.

The Bootstrap program itself exists in an unformatted form on a paper tape. This is necessary to keep the Bootstrap Loader simple. The Binary format of the Bootstrap tape is as follows :

All the instructions of the Binary Loader are listed consecutively on the paper tape in binary. There are no addresses or parity checks. The start address of the Binary Loader is known to the Bootstrap and it simply loads each binary word from the paper tape in consecutive locations. A successful load is recognised by the processor halting at the end of the tape.

The Binary Loader performs three different error checks :

A. Checksum error check;
B. Correct start of data block character;
C. Correct end of tape character.

If one of the above errors is detected while loading the processor prints a number corresponding to the error type and then halts.

13.2.3 8080 Aid System:

The 8080 AID System, FAID, is a software routine that facilitates the loading of programs and the execution and debugging once in memory. FAID was developed to run on the Development System described in Section 7. Details of the nature and development of this routine can be found in Ref. 8.

Changes that have occurred between the Development System and the current system, such as changes in the teletype driver have resulted in the necessity to modify the input/output/sub-routines in FAID. A brief description of the nature and capabilities of FAID is given below.

FAID has been written to occupy one kiloword of ROM and as a result has completely separate instruction- and data-banks. However, as the current system has only Read/Write memory, this restriction is unnecessary. The current version of FAID lies at the top of memory below the Binary Loader.

FAID is made up of two distinct parts. The first contains the directory, which does no more than wait for a command from the teletype. On receipt of a valid command control is transferred to the required routine in the second section.

The second section contains all the rountines available to FAID. Most routines return to FAID once they have performed their function. The following routines exist for FAID: (for details see ref. 8.)

A. Display/change a memory location;

B. Display/change a register;

C. Search memory;

D. Initialize memory;

E. Visual Dump;

F. Trap through a program;

G. Execute a program;

H. Binary Load;

I. Binary Dump.

The original FAID also contained a Binary Loader and Dump. These have both been removed from the current version. The Binary Dump was removed as it was considered an unnecessary featureand also to save memory space. The Binary Loader was removed as it was originally written to load paper tapes with a different binary format to that which is currently used. The Binary loader used at present is the one described in 13.2.2.

13.3 DRIVER AND EXERCISER ROUTINES

These programs have been written for two specific purposes :-

A. To test a specific section of the system hardware and ensure that it interacts validly with the rest of the system;

B. To develop drivers for the various input/output modules and peripherals, which can then be used in any data logging or control program.

Drivers are software routines that enable the I/O modules to operate and are very closely linked to the hardware design of the system.

Most of the routines contain a simple output routine which visually displays results or readings taken by the exercising program. No attempt has been made to format this information in any sophisticated way as it would unnecessarily increase the length and complexity of the exercising program.

13.3.1 Analog Input Module Exerciser:

This program is designed to fully test all the hardware in the Analog Input Module. This includes the relay multiplexer, the Programmable Gain Amplifier (PGA) and the Analog-to-digital converter (ADC). It also tests the interaction of the Module with the rest of the system. The program has been written to take one analog reading and output the digital value of the input voltage as well as the gain setting of the PGA to the teletype. To read again a RESET must be generated (by activating the RESET switch on the front panel). The program can be made to read continuously by simply changing the halt instruction at the end to a branch to location 00. The program is made up of a driver for the ADC and a simple output routine.

A. ADC DRIVER:

Owing to the long conversion time of the ADC, it is not desirable to dedicate the processor to the Analog Input Module when an analog channel is to be read. Instead, during the 100 milli-seconds that the converter is busy, control is returned to the main program. Conversion is initiated by subroutine ADC1 which first selects the desired channel, does the autoranging on the PGA, and then starts the conversion. An exit is made from the subroutine to the main program.

After the 100 milli-seconds the Analog Input Module generates an interrupt which sets a flag to indicate that the conversion is complete and the data is ready. At the discretion of the main program subroutine ADCIN is called. This tests the flag to determine if the conversion is complete. When the conversion is complete, it inputs and stores the data.

B. ADC OUTPUT ROUTINE:

This routine is used to visually indicate the correct operation of the Analog Input Module. The print out is to the teletype and consists of the following information :

(1) The gain setting on the PGA;
(2) The polarity of the input voltage;
(3) An octal number equivalent of the input voltage.

A typical print out is as follows :

064 * -327

327 → octal number representing input voltage
\- → polarity of input voltage
* → "multiplied by"
064 → PGA gain setting.

13.3.2 Alarm Interrupt Module Exerciser:

This routine checks the alarm interrupt unit for valid operation. It consists of two parts. Firstly, a driver which locates the required alarm routine after an interrupt has been received. The alarm routines in this case are simply output routines to the teletype and constitute the second part of the exerciser routine.

A. DRIVER:

The driver routine accepts an interrupt from the Alarm Interrupt Module, stores all the current program information such as the registers and program counter on the stack, identifies the interrupt, and then branches to the required alarm routine. As the Alarm Interrupt Module may be expanded to 64 interrupt lines a routine is required that will rapidly identify the interrupt. If a straightforward search is made through a table to identify the interrupt some interrupts will be serviced quicker than others, depending on their position in the lookup table. This is unsatisfactory and an alternative method is used which gives equal identification times to all alarm interrupts. The identification time is shorter than the average identification time in the previous method. In this method the eight bit number received from the Interrupt Control Unit that corresponds to the interrupting channel is used to form part of the address of a jump instruction. On branching to this address the processor will find the address of the required alarm routine. The advantage of this method is that the entire driver may be located in ROM with the addresses of the alarm routines forming the only variable to be stored in RAM.

B. OUTPUT ROUTINE:

The alarm routines for the exercising program are simply output routines to the teletype. In the exerciser the main program consists of outputting a string of "@" to the teletype. When alarm interrupts are received the following output to the teletype occurs :

INTO types out ten 0's
INT1 types out ten 1's
INT2 types out ten 2's
INT3 types out ten 3's

With this output format the ability of a higher priority alarm to interrupt a lower priority alarm routine can clearly be demonstrated. For example if INT2 is busy typing 2's and higher priority alarm INTO interrupts, it will stop typing 2's and type 10 zero's and then return and complete the required number of two's.

13.3.3 Analog Output Module Exerciser:

The analog outputs do not require a driver routine. Only one machine code instruction (OUT) is required to output the contents of the accumulator to the digital-to-analog converter (DAC). The DAC accepts 2's complement coding on the digital input to obtain positive and negative output voltages.

The analog output module exerciser runs together with the analog input module exerciser described in Section 13.3.1. The digital input from the ADC is first normalized by dividing by the gain of the PGA. As the gains of the PGA in octal are 1, 20, 100, and 200, this division is obtained by shifting the eight bit word, 0, 4, 6, and 7 places to the right respectively. The normalized octal equivalent of the analog input voltage is then converted to twos complement and output to the DAC where it can be monitored by an oscilloscope or voltmeter.

13.3.4 Digital Input/Output Exerciser:

The digital inputs and outputs are so simple that drivers are unnecessary. To input or output a digital word, only 1 machine code instruction is required, i.e.

```
OUT  50
```

This will output the 8 bit contents of the accumulator to device 50.

However, a simple program was written to test the digital Input/Output and is described below for the sake of completeness.

The eight bit word that is input from or output to the digital channel is also output to the TTY in binary format. If the word 0307 is input the TTY will print

```
DI  11000111
```

Similarly for digital outputs, with DO preceding the 8 bit word.

13.3.5 Teletype Driver:

The teletype driver consists of an interrupt handling routine and an Input/Output routine. The TTY interface is designed for an interrupt based Input/Output. The teletype driver consists of a subroutine TFLAG which sets the appropriate input or output flag, and input and output routines TYIN and TYOUT respectively.

A. INPUT:

When a character has been received from the TTY an interrupt is generated which causes a branch to subroutine TFLAG which will set the input flag. An exit is made to the main program. At the discretion of the main program the input subroutine TYIN can be called. This subroutine first checks the status of the input flag. If the flag has been set it knows that a word has been received and is ready to be input. If the flag is reset it will wait until the flag is set. Once the flag has been set it will input the word from the TTY, reset the input flag, and return to the main program.

B. OUTPUT:

This is the converse of the input operation. If the flag is reset it means that transmission of the previous character is still underway and it must wait. When transmission to the TTY ceases and the TTY is ready for the next character, an interrupt is generated. This causes a branch to subroutine TFLAG which sets the output flag and then returns to the main program. At the discretion of the main program the output routine TYOUT is entered. The output flag is first checked and if it is set (the TTY is ready to receive another character) then the word is outputted. If not, it waits for the output flag to be reset as mentioned above. Having output the word the output flag is reset indicating that transmission is underway. Control is then returned to the main program.

13.3.6 Real Time Clock Driver:

There are two possible modes of operation of the real time clock :-

A. As an interval timer

B. Time of day clock.

Software for a priority structured multiple interval timer has been developed elsewhere (ref. 10).

(1) DRIVER

A routine for a time of day clock was required. The real time clock interrupts the processor every 10 milli-seconds. This causes a branch to subroutine TODC, the time-of-day-clock driver. The time-of-day clock consists of four eight bit words. The highest order word contains the hours, the next minutes, the third seconds. The last word is incremented every time the RTC interrupts, that is, every 10 milli-seconds. When this byte contains 200 (octal) it is zeroed and the seconds byte is incremented. Similarly when the seconds byte equals ~~96~~ 76 (octal) it is zeroed and the minutes byte in incremented. The hours byte is incremented when the minutes byte is equal to ~~96~~ 76 (octal). As it is a 24 hour clock, the hours byte will count up to 28 (octal) before being zeroed.

The clock is initialized by loading the three memory locations representing the hours, minutes and seconds bytes with the current time. The fourth byte is zeroed. The system can then run and the correct time will be maintained.

(2) OUTPUT ROUTINE:

The time of day is printed every 30 seconds on the teletype as follows :-

HH MM SS

SECTION IV.

OVERALL PROJECT EVALUATION

CHAPTER 14.

HARDWARE EVALUATION

Viewing the hardware system in retrospect, a number of valuable insights can be obtained. The rapid advancement of microprocessor and related technologies over the last year has perhaps made certain of the aspects of the hardware appear redundant. However, a lot of valuable know-how has been generated by building the system from the basic elements.

The three hardware aspects of the system, that is, the microcomputer, the front panel unit, and the industrial interface are reviewed below.

14.1 MICROCOMPUTER

The architecture of the microcomputer part of the system is distributed over four separate cards. This architecture may be questioned as being the most suitable. Certainly it achieves the original goal of flexibility but with the wisdom of hindsight it can be seen that a more efficient architecture would be a single card microcomputer system complete with peripheral interface and limited decoding (similar to INTEL SDK 80 kit). If expansion to a larger system is required then a "SYSTEM EXPANDER" card with full I/O decoding could be added. The advantage of this format is that when configured as a small system (say two I/O modules) hardware overheads for the microcomputer are limited to a single card.

14.1.1 Intel 8080 CPU:

Since the time when the 8080 was selected a vast number of microcomputers have become available that would be quite capable of doing the job. However, no one of these has proven to be in any way superior to the 8080, and a number are a lot worse for reasons ranging from poor instruction sets to poor vendor support and availability.

There is also a trend by which the 8080 is becoming the unofficial industry standard. At the last count there were 6 manufacturers of 8080's (AMD, NEC, TI, Siemens, National, Intel). Also, most of the early industrial microprocessor projects were based on the 8008 (ref. 13) and hence there is a trend when updating these systems to go to the 8080 as much of the software is then compatible and hence of the popular 8 bit microprocessors the 8080 has made the greatest penetration into the processor control world (ref. 14). The 8080 has also proven itself to be an extremely reliable chip and tests indicate that failure rates are as low as 0.04% per 1000 hours at a 90% confidence level (ref. 15).

In view of these facts it is felt that the 8080 was a highly successful choice for the microprocessor.

14.1.2 Memory System:

The CMOS memory (INTEL 5101's) has proven to be extremely successsful in providing non volatile memory storage. This is done by means of battery backup for the memory chips. Battery life appears to be close on shelf life of the batteries. In the two months that 2.5 kilowords of memory were backed up by pen light batteries there was no detectable drop in battery voltage.

However, once the control program has been written and debugged commitment to EPROM is the best solution in view of the incorruptible nature of EPROMS. In this system EPROMS were not used as the system was not intended to be used in any specific control application and hence a specific control program could not be written.

14.1.3 Interrupt System:

The use of interrupts in an industrial microprocessor system is a double edged sword. Vastly improved CPU utilization can be obtained for the price of increased software complexity. The alternative to an interrupt based system is one in which "SENSE" loops are used such as on the VARIAN mini-computer (ref. 16). For a large scale process control microcomputer this would be a highly impractical situation. However, for a small scale dedicated microcomputer system it becomes worth consideration.

If the microcomputer system is used only in applications of direct digital control, or data logging then an interrupt based I/O can be dispensed with.

In a supervisory capacity interrupts are essential to any process control computer unless its task is small enough that the delay in detecting a change of state on any input is sufficiently short. The handling of peripherals such as a TTY could also be done without recourse to interrupts.

However, in the 8080 and with the current ICU the increase in software complexity is small and the advantages of improved CPU utilization outweigh the advantages of the "SENSE" loop type of system. As this system is a generalized system and does not have a predetermined role it is essential that an alarm interrupt facility be provided.

14.I.3 Communication Peripherals:

The system has facilities for up to eight peripherals. Only an ASR 33 teletype was used as this was immediately available and had the advantage of providing a keyboard, printer and paper tape reader and punch in one unit. For industrial use a more ruggardized form of printer such as the Spectronics TP20 thermal printer would greatly facilitate the loading of long programs. A punch is not really required. Some means of mass data storage may be required however. There are two possible ways of achieving this. One is to link the microprocessor system to a supervisory minicomputer if one is available and use the mini's mass data storage facilities e.g. disk or magnetic tapes. The second is for the microprocessor system to have its own mass data storage peripheral such as a cassette recorder or floppy disk. Serial links to either the mass data storage device or the minicomputer are the most suitable in view of reduced cabling and noise pickup.

14.2 FRONT PANEL UNIT

The front panel unit performed very well and gave a wide range of control over the system. A facility well worth considering and which would serve as an aid to software debugging is a hardware trap. This would allow the user to trap from one location in memory to another without having to single step through the instructions byte by byte.

14.3 INDUSTRIAL INTERFACE

The industrial interface achieved the goal of being a low cost interface of suitable reliability and flexibility to test the viability of a microprocessor system in industry. Many other interface modules could have been built but the basic analog and digital input and output modules were considered sufficient.

An evaluation of the various modules is given below.

14.3.1 Analog Input Module:

Isolation of the floating front end of this module was good and millivolt signals could easily be measured with 260 volts RMS common mode noise.

The current ADC system used, dual slope integrating unit, gives very good noise immunity but has the problem of being extremely slow, with a maximum sampling rate of ten samples per second. This is adequate for certain data logging applications and extremely slow industrial processes. However for processes where direct digital control is required a faster successive approximation ADC sampling at say 100 samples/sec. would best be used. For example it has been recommended that for a microprocessor based batching system an ADC converter speed of at least 100 microseconds is required (ref. 17).

An analog input module demonstrates clearly one advantage of a microprocessor based system: That of replacing hardware logic by software control. Firstly the Programmable Gain Amplifier. The autoranging in many systems (e.g. RTP) is done by means of complex hardware. In this system the autoranging is done successfully under software control and adds at most 100 microseconds to an ADC conversion time of 100 milli-seconds. Secondly, the PGA is a low cost device and has inherent offsets on the output. This does not affect the accuracy of the system, because, under software control, the offsets may be input and subtracted from the actual readings taken later with the result of no loss in accuracy.

14.3.2 <u>Analog Output Module</u>:

There is the question whether 8 bits (seven bits plus a sign bit) is sufficient accuracy for the analog output. The seven magnitude bits give a resolution of 0,78%. As the system is a generalized one and has not been designed for a specific process, accuracy requirements cannot really be evaluated. The current system establishes the workability of the analog output module. If greater accuracy is required it can be obtained by outputting two bytes of data to each DAC module thus achieving up to 16 bit accuracy. This can be implemented in two ways. Firstly, by treating each DAC as two devices and outputting first the high order data to the one device and then the lower order data to the second device. This has the disadvantage of halving the number of DAC modules that can be addressed, but would be simple to implement hardware wise. The second approach would involve more complex hardware. This is to output both bytes of data to the same device address but to decode by extra hardware which byte is high order and low order. In the interests of reduced hardware and better CPU utilization the first approach is the most suitable.

14.3.3 Alarm Interrupt Module:

An asynchronous link to the process is essential in any process controller where supervision is required. The only time interrupts could be dispensed with, is if the microcomputer system is dedicated to a small process, and services each channel with sufficient frequency that a change of state will be detected within the required time limit. For any processor handling more than one complex, or time consuming task, interrupts to an alarm task is essential.

The input conditioning circuitry of the Alarm Interrupt Module was tested up to 260 volts common mode voltages and found to work satisfactorily.

14.3.4 Digital I/O Modules:

Both modules were tested for isolation to 260 volts and found to work satisfactorily. In a process there may be applications where digital I/O configurations, other than what has been built, are required. However, the current configuration was considered sufficient for testing the viability of the system.

14.4 GENERAL HARDWARE

There are three other aspects of the hardware which need to be evaluated. They are given below.

14.4.1 Back-Plane Wiring:

A non-standard back-plane was used. The advantage being that it is the most economical on the number of edge-connectors required. It has the disadvantage that each card in the system must go into a particular slot. A more ideal solution would have been to have standard back-plane wiring for the industrial interface section of the system, thus allowing any I/O options to be used in any slots. The microcomputer section which does not alter could remain as it is.

14.4.2 Low Power Schottky Logic:

The LS TTL proved to be extremely easy to design with and if prices drop it could quite easily usurp the role of TTL in digital systems. The low power requirements and dissipation were largely instrumental in allowing the use of a sealed crate to house the system. For the entire system only 90 watts of power is consumed and very little heat is generated.

14.4.3 Power Supply:

Tests conducted in the laboratory indicate that the power supply is extremely immune to supply line noise. The constant voltage transformer allowed the system to operate satisfactorily with AC supply voltages as low as 100 volts RMS. The circuit in fig. 24 was used to induce spikes on the supply line. Opening and closing switch S1 causes current surges through the inductor L which cause voltage spikes on the supply. The system could not be made to fail by this method as the spikes were sufficiently attenuated by the CVT and the various filters described in Chapter 11.3.

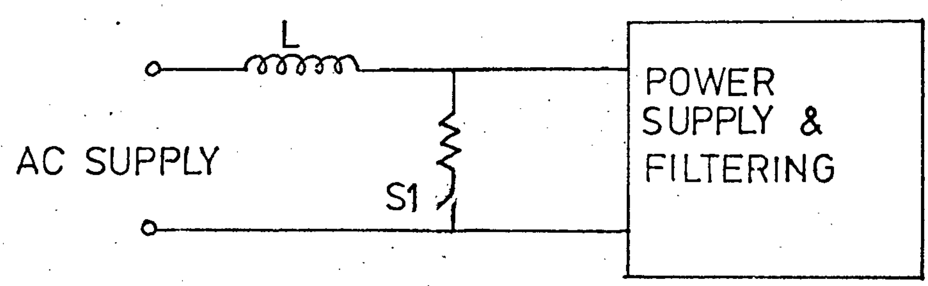


Fig. 24: CIRCUIT FOR INDUCING NOISE ON SUPPLY LINE

CHAPTER 15.

SOFTWARE EVALUATION

15.1 GENERAL

The aim of this project is to build an industrialized microcomputer system. The system is not designed for any specific process and hence the software developed is not specific application control or data logging programs. The system must, however, be capable of supporting any such programs. Work on a software development system to aid the development of such programs has been done elsewhere (ref. 10).

The software that has been written has been to assist in the development and validation of the hardware and in this respect it has been successful in its objectives.

The software consists of two types of routines, drivers for the various I/O modules and peripherals and General Utility Programs to assist in this development.

These are evaluated below.

15.2 GENERAL UTILITY ROUTINES

These routines were prerequisites to the development of any other software. They allow the programs to be loaded into memory and once loaded, to be debugged or run from the TTY. The bootstrap routine and Binary Loader were used successfully for loading programs. The most important of the utility routines is the 8080 AID program FAID. This gave complete control of the program to the TTY once the program had been loaded and was found to be almost essential when debugging long programs. Ideally, FAID should have been on an EPROM with only a small data bank in RAM as this would have prevented any possible corruption of the program. This is true of the Bootstrap and Binary Loader as well.

Although FAID will fit into less than 1 kiloword of memory, it is extremely versatile and greatly improves the viability of the system.

15.3 DRIVER AND EXERCIZER ROUTINES

The exercizer routines were successful in aiding in the debugging and development of the various I/O modules. The programs were fairly simple so as not to confuse hardware and software bugs during the debugging process.

A lot of use was made of the TTY driver which was found to work well. The drivers for the Analog Input Module and Alarm Interrupt Module worked satisfactorily but with more specific applications in mind, variations to these drivers may be found to be more suitable. For example, if only a few Alarm Interrupts are to be used a simple search through a table may be a better means of identifying the alarm program than the more generalized routine described in 13.3.2

CHAPTER 16.

SYSTEM EVALUATION

There were two basic objectives in the motivation for the development of this industrialized microprocessor system. Firstly and fundamentally, there was the need to develop know-how in the field of microprocessors and their industrial application. The second objective, which is really the way in which the first manifested itself, is to establish the viability and capabilities of a microprocessor in an industrial process control application.

In order to do this, that is, to fully investigate the capabilities of microprocessors the system that was built was based on three basic design criteria.

These are :-

A. The basic requirements of industrial reliability must be met.

B. The system must be flexible enough in its architecture to investigate the viability of the system in its various configurations.

C. The system must be designed for low maintenance and minimum operator interaction.

These three objectives are now evaluated.

16.1 INDUSTRIAL RELIABILITY

The real acid test of any industrial system is whether it will operate in the conditions under which it is meant to actually work. That is in an industrial process. However, circumstances prevented this from actually being done and so doubt may validly be cast on the true industrial reliability of the system. However, tests were run under laboratory conditions to simulate what was considered to be the three main sources of industrial noise. These are "pick up" of common mode noise of the signal lines, supply line noise and noise induced by EM radiation. Tests carried out indicate that the system does have a high degree of noise immunity. The system could not be made to fail or malfunction when noise was induced simultaneously on the supply line and the signal lines. Immunity to electro-magnetic radiation was tested qualitatively by wrapping the leads of an arc welder running at 120 amps around the processor and then welding a piece of scrap iron while a short program was run repetitively in the processor. The system could not be made to fail under these conditions. Although these tests do not guarantee faultless performance of the system when exposed to the often unpredictable vagaries of industrial noise, they do indicate that the system does have an inherent degree of noise immunity.

16.2 FLEXIBILITY

The purpose of designing an architecturally flexible system is that one may construct the system either as a minimal "bare bones" system or as a fully expanded system with a large amount of memory or I/O. It is in this field that perhaps the project was most successful. That is in indicating what the sensible limits of a microprocessor system ought to be. The system constructed can support an extremely wide range of I/O. Analog and Digital inputs and outputs are available and decoding is available for up to 65k of memory as well as 1000 analog input channels and hundreds of digital I/O channels. However, a price is paid for this flexibility, that of hardware overheads. The hardware required to support such a large system becomes a liability when only a small system is actually required. In the present system the basic microprocessor, which would be required for any amount of I/O, is four cards. This is too much. The entire microcomputer, and peripheral interfaces should be on one card. The only extension to the microcomputer should be in the form of memory cards.

The basic mistake in the approach to the current microprocessor system is to treat it as a downgraded mini-computer with associated flexibility. The forte of the microprocessor lies in its ability to be used as an intelligent dedicated device, and this must be reflected in the hardware architecture. One microcomputer system should not be trying to compete with a mini computer by being so flexible that it can be expanded to handle 1000 analog inputs. Software wise this is unrealistic. The Industrialized Microprocessor System must have limited I/O size. Say three I/O cards, from which may be selected the analog and digital I/O options. If more I/O channels are required then another microprocessor system must be used. This viability for multiple dedicated systems is a big advantage of microprocessors. These multiple distributed systems need not in fact be spatially distributed but could all plug in as units to a common crate with interprocessor links. On the other hand spatial distribution is equally acceptable.

Thus it is in the sphere of establishing the size and nature of microprocessors in industry that the greatest learning in the project occured. Although the current system is based more on the concept of a downgraded mini computer than on the concept of small scale dedicated distributed systems mentioned above, the project can still be regarded as successful as it stimulated the evolution of ideas to their current form.

16.3 BLACK BOX APPROACH

As mentioned in the section of Aims of the project (Chapter 3.3) an attempt was made to create a system with minimal maintenance and operator interaction. The usual human interface associated with a computer were dispensed with. This is consistent with the approach that the microprocessor system must not be considered as a computer system. It is more an intelligent controller/data logger, an instrument operating close to the process. Once the system is operating correctly the only interaction is to initiate programs or alter program parameters. This can be done either via a remotely located keyboard or central computer, hence no actual control switches are required directly on the system. This gives an added security advantage, for there are no switches or buttons to be tampered with once the system is running. When installing the system on a plant little attention need be given to accessibility as all the required access can be done remotely.

Should the microprocessor system fail access can then be obtained to busses and control lines via a plug on debugging front panel. This front panel is not unique to any microprocessor system.

In its present form the system can only be initiated on site by RESETting and RUNning the system from the front panel. A more ideal situation would be a single twisted pair running from the microprocessor system to a central control point. The microprocessor may then be initiated remotely.

Besides the signal lines connecting the microprocessor system to the process, only two twisted pairs to a central location would be required. One a serial link to a keyboard and printer or mini computer, and secondly a line to initiate the system.

16.4 THE ROLE OF THE MICROPROCESSOR - IMPACT ON INDUSTRY

The problem with microcomputers at their present stage of evolution is that anything that can be written about them is obsolete by the time the ink has dried on the paper. This rapid rate of development makes standardization very difficult or even undesirable as standardization can act as a brake on new ideas, although it makes good economic sense.

However, some attempt must be made to see a pattern and to define the role in the industrial process control world to which microprocessors are most suited.

At the top end of the scale are the large process control computers. At present the microprocessor is not a challenge to these and may never be one. At the bottom end of the scale is the programmable logic controllers and data logging instruments. The microprocessor system is not needed here. But between these extremes is a large loosely defined area where the capabilities of a full scale mini computer are unnecessary but where the control algorithms are too complex for the limited programming capabilities of the programmable logic controllers. This is where the microprocessor system in its present state belongs. In small scale dedicated control of complex processes. "Small scale", in the sense that no single microprocessor should attempt to do too much. If more control loops are required, add another microprocessor. In this way true distributed control can be achieved. The ability to increase the reliability of a control or data logging system is really what makes microprocessors attractive. The increase on reliability can be achieved by this distribution.

Although distributed process control by microprocessor networks offers a wide range of advantages (ref. 18) over a centralized minicomputer system the problems and added complexities of interprocessor communication could easily override the benefits. To minimise these complexities distributed control by microprocessors must be on a fairly autonomous basis with minimal links and communication requirements between processors.

However, although the reign of the centralized process control mini computer may be challenged by distributed microprocessor networks in the future, their reign in this field is secure at present owing to the facts that at the time of writing no industrialized microcomputer systems are commercially available locally and that there are still unanswered questions and difficulties as mentioned above in multimicroprocessor networks. These are both facts which only reflect the current state of art in microprocessor systems and are not fundamental limitations in the microprocessors themselves. Hence reversal of either of the above two factors could see microprocessor systems advancing beyond the level of small scale dedicated controllers.

C O N C L U S I O N

The system has shown that a low cost solution to a digital process controller/data logger does exist in a microprocessor system. The advantages of using a microprocessor in such a system, namely: low costs, flexibility and reliability were established.

Hardware costs were kept to a minimum by executing a large proportion of the logic under the software control of the microprocessor. Also the "intelligence" of the microprocessor could be used to minimise any offsets in some low cost I/O modules, thus again minimising hardware costs.

The flexibility of the system allows it to be used as a small dedicated stand-alone unit or simply, by the addition of more memory and I/O modules, to merge with the low end of the minicomputer range of capabilities.

Tests done on the reliability of the system indicate that it is suitable for industrial use but a thorough verification of this is yet to be done.

The industrialized microcomputer system that has been built has, as laid out in the objectives, provided a means by which the full capabilities and limitations of a microprocessor system can be evaluated in industrial applications.

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APPENDIX A

MICROPROCESSOR SCORECARD

MICROPROCESSOR SCORECARD

MICROPROCESSOR SCORECARD	CLASSIFICATION	TECHNOLOGY	PARTS FAMILY: Clock Driver	I/O Interface	UART/USRT	RAM	ROM/PROM	Interface	FEATURES: Interrupts	One-Chip CPU	Microprogrammed	Accessible Stack	DMA Ability	BCD Arithmetic
BURROUGHS MINI-D	8-Bit CPU	PMOS								✓				
ELECTRONIC ARRAYS	8 Bit CPU	NMOS		✓		✓	✓		✓	✓		✓	✓	✓
FAIRCHILD F-8	8 Bit CPU	NMOS	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
FAIRCHILD PPS-25	4 Bit CPU	PMOS		✓		✓	✓							✓
INTEL 4004	4 Bit CPU	PMOS	✓	✓		✓	✓	✓		✓				✓
INTEL 4040	4 Bit CPU	PMOS	✓	✓		✓	✓	✓	✓	✓				✓
INTEL 8008-1	8 Bit CPU	PMOS	✓	✓	✓	✓	✓	✓	✓	✓				
INTEL 8080	8 Bit CPU	NMOS	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
INTEL 3001	2 Bit Slice	Bipolar				✓	✓	✓	✓		✓		✓	
INTERSIL 6100	12-Bit CPU	CMOS	✓			✓			✓	✓			✓	
MONOLITHIC MEMORIES 6701	4-Bit RALU	Bipolar									✓			
MOSTEK 5065	8 Bit CPU	PMOS							✓	✓		✓	✓	
MOTOROLA 6800	8 Bit CPU	NMOS		✓	✓	✓	✓		✓	✓		✓	✓	✓
NATIONAL CMP-8	8-Bit CPU	NMOS		✓	✓	✓	✓	✓	✓	✓		✓	✓	
NATIONAL GPC/P	4 Bit Slice	PMOS									✓	✓	✓	
NATIONAL IMP-4	4 Bit CPU	PMOS						✓	✓		✓			✓
NATIONAL IMP-8	8 Bit CPU	PMOS							✓		✓	✓	✓	
NATIONAL IMP-16	16 Bit CPU	PMOS							✓		✓	✓	✓	
RAYTHEON RP-16	4 Bit Slice	Bipolar							✓		✓			
RCA COSMAC	8 Bit CPU	CMOS							✓	✓		✓	✓	✓
ROCKWELL PPS-4	4 Bit CPU	PMOS	✓	✓	✓	✓	✓			✓		✓		✓
ROCKWELL PPS-8	8-Bit CPU	PMOS	✓	✓	✓	✓	✓		✓	✓		✓	✓	✓
SIGNETICS 2650	8 Bit CPU	NMOS							✓	✓				✓
TOSHIBA TLCS-12	12 Bit CPU	NMOS		✓		✓	✓		✓	✓	✓			
TRANSITRON TMC/1601	4 Bit Slice	Bipolar							✓		✓	✓	✓	

MICROPROCESSOR SCORECARD	WORD SIZE (Data Instruction)	ADDRESS CAPACITY (Program Words)	CLOCK (kHz/Phases)	REGISTER ADD TIME (μsec per Data Word)	NUMBER OF CPU REGISTERS: ALU	XR	GP	RETURN-STACK SIZE (Nr x Bits)	VOLTAGES REQUIRED	POWER DISSIPATION	OPERATING TEMPERATURE RANGE (°C)	PACKAGE SIZES (DIP Pins)	PRICE RANGE (approx.: 100 qty: CPU)	STATUS: First Samples	First Deliveries	REMARKS
BURROUGHS MINI-D	8/12	256	1000/1	9	3		1	1 x 8	−12, +5		0 ~ 70	16	$ 60	2073	3073	ROM on CPU
ELECTRONIC ARRAYS	8/8	64K	1000/2		1	1	15	7 x 18				40		3075		16-Byte String Operations
FAIRCHILD F-8	8/8	64K	2000/0	2	65			(RAM)	+5, +12	6	0 ~ 70	40	$ 75	4074	1075	Clock on Chip
FAIRCHILD PPS-25	4 x 25/12	6656	400/2	62.5	1			4 x 12	−9, +5	8	0 ~ 70	16,18,24,40	$ 60		2071	
INTEL 4004	4/8	4K	740/2	10.8	1		16	3 x 12	15 or (−10,+5)	1.0	0 ~ 70	16	$ 30	2071	4071	
INTEL 4040	4/8	4K	740/2	10.8	1		24	7 x 12	15 or (−10,+5)	10	0 ~ 70	16, 24	$ 40	4074	4074	8K Program Space in Two Banks
INTEL 8008-1	8/8	16K	800/2	12.5	1		8	7 x 14	−9, +5	10	0 ~ 70	18	$ 80	4071	1072	Second Source: MIL
INTEL 8080	8/8	64K	2083/2	2	1		8	(RAM)	−5,+5,+12	10	0 ~ 70	40	$ 200	4073	2074	
INTEL 3001	2N/18+	512	6061/1	165	2		10	(NONE)	5	4.5	0 ~ 70	28, 40	$ 550	3074	3074	
INTERSIL 6100	12/12	4K	4000/0	5	1		1	Modifies Program	5	.01	−55 ~ +125	28, 40	$ 175	4074	1075	PDP-8 Code; Clock on Chip
MONOLITHIC MEMORIES 6701	4/17		6666/1	2	3		19	(NONE)	+5	1.	0 ~ 75	40	$ 95	1074	2074	
MOSTEK 5065	8/8	32K	1400/3	10	3			(RAM)	−12, −5, +5	.7	0 ~ 50	40	$ 100	1074	3074	3-State CPU
MOTOROLA 6800	8/8	64K	1000/2	2	2	1		(RAM)	5	.25	0 ~ 70	24, 40	$ 150	2074	4074	Second Source: AMI
NATIONAL CMP-8	8/8	64K	/2	18	2	2		(RAM)				40		1075	2075	
NATIONAL GPC/P	4N/23	100	715/4	14	8			16 x 4N	−12, +5	.7	0 ~ 70	22, 24	$ 150	1073	3073	1 ≤ N ≤ 8
NATIONAL IMP-4	4/4	4096	500/4	12	4			7 x 12	−12, +5	10	0 ~ 70	24, 40	$ 150	3074	4074	16 x 4 Data Stack
NATIONAL IMP-8	8/8	64K	715/4	4.8	3	1		16 x 8	−12, +5	10	0 ~ 70	22, 24	$ 230	4073	1074	
NATIONAL IMP-16	16/16	64K	715/4	4.8	2	2		16 x 16	−12, +5	14	0 ~ 70	22, 24	$ 310	1073	3073	
RAYTHEON RP-16	4N/48	64K	5000/1	1	1	1	2	(RAM)	5		−55 ~ +125	48		4074		
RCA COSMAC	8/8	64K	2670/1	8	1		p	r x 16	5 ~ 12	01	−55 ~ +125	28, 40	$ 300	4074	2075	(p+2r) ≤ 30
ROCKWELL PPS-4	4/8	4K	200/2	5	[illegible]		1	2 x 12	17	225	0 ~ 70	42	$ 45	1072	3072	8K Program Space in Two Banks
ROCKWELL PPS-8	8/8	16K	256/2	4	1	1	2	(RAM)	17	3	0 ~ 70	42	$ 47	4074	1075	
SIGNETICS 2650	8/8	32K	1200/1	4.8	7			8 x 15	5	.5	0 ~ 70	40	$ 120	4074	1075	
TOSHIBA TLCS-12	12/12	4K	1000/3	13	4		6	(RAM)	−5, +5	8	−20 ~ +80	18,24,28,42	$ 215	2074	3074	
TRANSITRON TMC/1601	16/16	32K		.4	a	v		(RAM)				40		2075	3075	(a+v) ≤ 8

Microcomputer Technique Inc

APPENDIX B

THE 8080 MICROPROCESSOR

1. INTRODUCTION

The 8080 is a complete 8-bit parallel central processing unit (CPU) for use in general purpose digital computer systems. It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process, thus offering much higher performance than conventional microprocessors (2μs instruction cycle). A complete micro computer system is formed when the 8080 CPU is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semi-conductor memory.

Although significantly higher in performance than existing microprocessors, the 8080 has been designed to be software compatible at the source code level with Intel's 8008 micro-processor. Like the 8008, the 8080 contains six 8-bit data registers, an 8-bit accumulator, four 8-bit temporary registers, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The 8080 also provides decimal arithmetic capability, and it includes sixteen bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The 8080 has a stack architecture wherein any portion of the external memory can be used as a last in/first out stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The 8080 also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can easily be saved when an interrupt occurs and then be restored after the interrupt. Another major advantage is that almost unlimited subroutine nesting is possible.

This processor has been designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are used to allow direct interface to memories and I/O ports. Control signals, which require no decoding, are provided directly by the processor. All busses, including control, are TTL compatible.

Communication on the address lines and the data lines can be interlocked by using the HOLD input. When the HLDA (Hold Acknowledge) signal is issued by the CPU, CPU operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits "OR-tying" the address and data busses with other devices such as direct memory access channels (DMA).

The 8080 has many instructions which are extremely useful and extend the range of applicability of the CPU. The instruction groups are as follows:

- Data register and memory transfers
- Conditional or unconditional branches and subroutine calls
- I/O operations
- Direct Load/Store Accumulator
- Save, Restore Data Registers, Accumulator and Flags
- Double Length Operation in Data Registers
  - Increment/Decrement/Addition
  - Direct Load/Store (H and L)
  - Load Immediate
  - Index Register Modification
- Indirect Jump
- Stack Pointer Modification
- Logical Operations
- Binary Arithmetic
- Decimal Arithmetic
- Set and reset interrupt enable flip-flop
- Increment/Decrement Memory or data registers

The purpose of this publication is to present the basic microprocessor operation, instruction set, and electrical characteristics. In addition, other memory and peripheral circuits which have been designed, and specified for use with the 8080 are presented.

8080 ADDRESSING MODES:
- DIRECT
- REGISTER
- REGISTER INDIRECT
- IMMEDIATE

2. PROCESSOR TIMING

The following describes the function of all of the 8080 I/O pins. Several of the descriptions refer to internal timing periods. For a definition of the timing periods refer to section 2-3.

2-1. Pin Configuration and Control Signal
The pin configuration is shown in Figure 1.

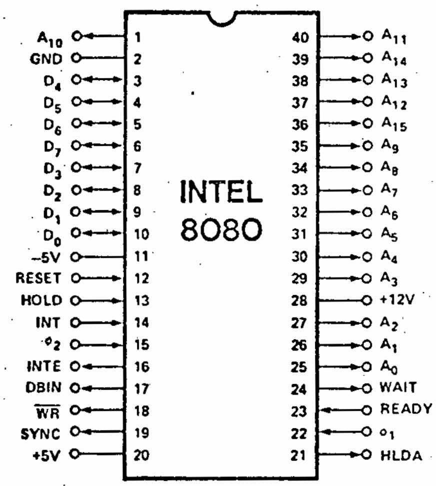


Figure 1. Pin Configuration

PIN DEFINITION

Symbols	Meaning
A_{15}-A_0 (output tri-state)	ADDRESS BUS: the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.
D_7-D_0 (input/output) tri-state	DATA BUS; the data bus provides bidirectional communication between memory and I/O devices for instructions and data transfers. D_0 is the least significant bit.
SYNC (output)	SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle. (Instructions can be executed in 1, 2, 3, 4 or 5 machine cycles, and the status information of each machine cycle is sent to external latches at SYNC time.) See 2-2.
DBIN (output)	DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080 data bus from memory or I/O.
READY (input)	READY; the READY signal indicates to the 8080 that valid memory or input data is available on the 8080 data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080 does not receive a READY input, the 8080 will enter a WAIT state for as long as the READY line is low.
WAIT (output)	WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.
$\overline{WR}$ (output)	WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
HOLD (input)	HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080 address and data bus as soon as the 8080 has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • the CPU is in the HALT state • the CPU is in the T2 or TW state and the READY signal is active As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin. See Figure 3. The CPU will always finish the execution of the current machine cycle. When the HOLD signal is removed, the operation will resume from the T1 time of the next machine cycle. (See attached timing charts, Figures 3 and h in Appendix III.)

Symbols	Meaning
HLDA (output)	HOLD ACKNOWLEDGE: the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: T3 for READ memory or input The Clock Period following T3 for WRITE memory or OUTPUT operation In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2. See Appendix III-f for timing diagram and $\overline{WO}$ status information for mode determination.
INTE (output)	INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the EI and DI instructions and inhibits interrupts from being accepted by the CPU if it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.
INT (input)	INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request. The CPU acknowledges acceptance of an interrupt by sending out the INTA (Interrupt Acknowledge) status signal at SYNC time. During the next instruction fetch cycle the program counter is not advanced and a 1 byte instruction (usually RESTART) can be inserted. See Appendix I.
RESET (input)	RESET; while the RESET signal is activated, the content of the program counter is cleared and the instruction register is set to 0. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, and registers are not cleared as with the 8008. The HL and DE registers may be exchanged.
V_{ss}	Ground Reference.
V_{dd}	$+12 \pm 5\%$ Volts
V_{cc}	$+5 \pm 5\%$ Volts
V_{bb}	$-5 \pm 5\%$ Volts (substrate bias)
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

2-2. Status Information

Instructions for the 8080 require from one to five machine cycles for complete execution. The 8080 sends out 8 bit of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
HLTA	D_3	Acknowledge signal for HALT instruction.
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO} = 0$). Otherwise, a READ memory or INPUT operation will be executed.

*These three status bits can be used to control the flow of data onto the 8080 data bus.

A5

N.B

2-3. Timing

Instructions in the 8080 contain one to three bytes. Each instruction requires from one to five machine or memory cycles for fetching and execution. Machine cycles are called M1, M2, . . . , M5. Each machine cycle requires from three to five states T1, T2, . . . , T5 for its completion. Each state has the duration of one clock period (0.5 micro-second). There are three other states (WAIT, HOLD, and HALT) which last one to an indefinite number of clock periods, as controlled by external signals. Machine cycle M1 is always the operation-code fetch cycle and lasts four or five clock periods. Machine cycles M2, M3, M4, and M5 normally last three clock periods each.

To understand the basic operation of the 8080, refer to the simplified state diagram shown in Figure 3 and the timing diagram of Figure 2.

During T1 the content of the program counter is sent to the address bus, SYNC is true, and the data bus contains the status information pertaining to the cycle that is currently being initiated. T1 is always followed by another state, T2, during which the condition of the READY, HOLD and HALT Acknowledge Signals are tested. If READY is true, T3 can be entered; otherwise, the CPU will go into the wait state (TW) and stay there for as long as READY is false.

READY thus allows the CPU speed to be synchronized to a memory with any access time or to any input device. Furthermore, by properly controlling the READY line, the user can single-step through his program.

During T3, the data coming from memory is available on the data bus and is transferred into the instruction register (during M1 only) as shown in the 8080 block diagram of Figure 4. The instruction decoder and control sections then generate the basic signals to control the internal data transfers, the timing, and the machine cycle requirements of the new instructions.

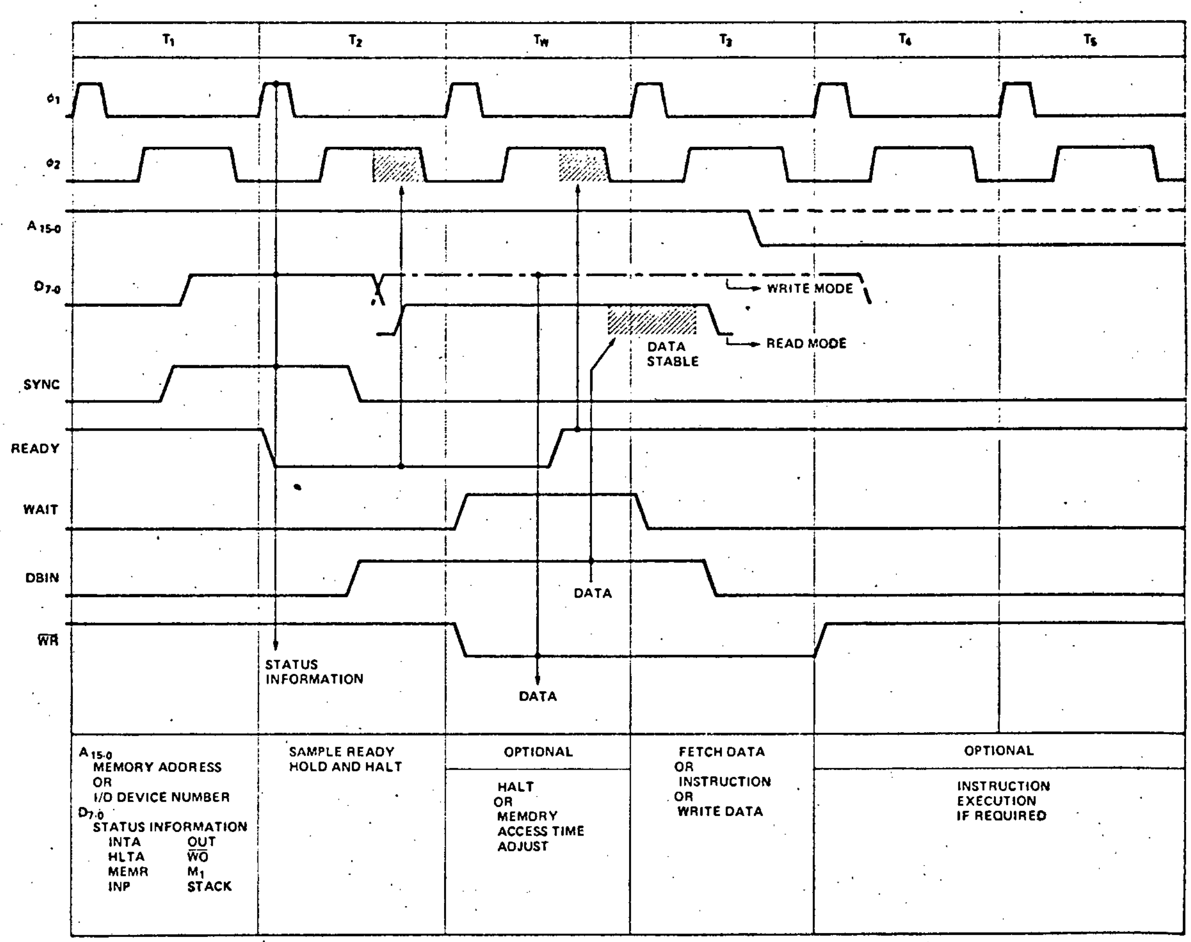


Figure 2. Basic 8080 Instruction Cycle

At the end of T4, if the cycle is complete, or else at the end of T5, the 8080 goes back to T1 and enters machine cycle M2, unless the instruction required only one machine cycle for its execution. In such cases, a new M1 cycle is entered. The loop is repeated for as many cycles and states as required by the instruction.

It is only during the last state of the last machine cycle that the interrupt request line is tested and a special M1 cycle is entered, during which no program-counter incrementing takes place and INTERRUPT ACKNOWLEDGE status is sent out. During this cycle, one of eight possible restart instructions will be sent to the CPU by the interrupting device.

Instruction state requirements range from a minimum of four states for non-memory referencing instructions, like register and accumulator arithmetic instructions, up to a maximum of 18 states for the most complex instructions (exchange the contents of registers H and L with the content of the top two locations of the stack). At the maximum clock frequency of 2 megahertz, this means that all instructions will be executed in intervals ranging from 2 μs to 9 μs. If a HALT instruction is executed, the processor enters a WAIT state and remains there until an interrupt is received.

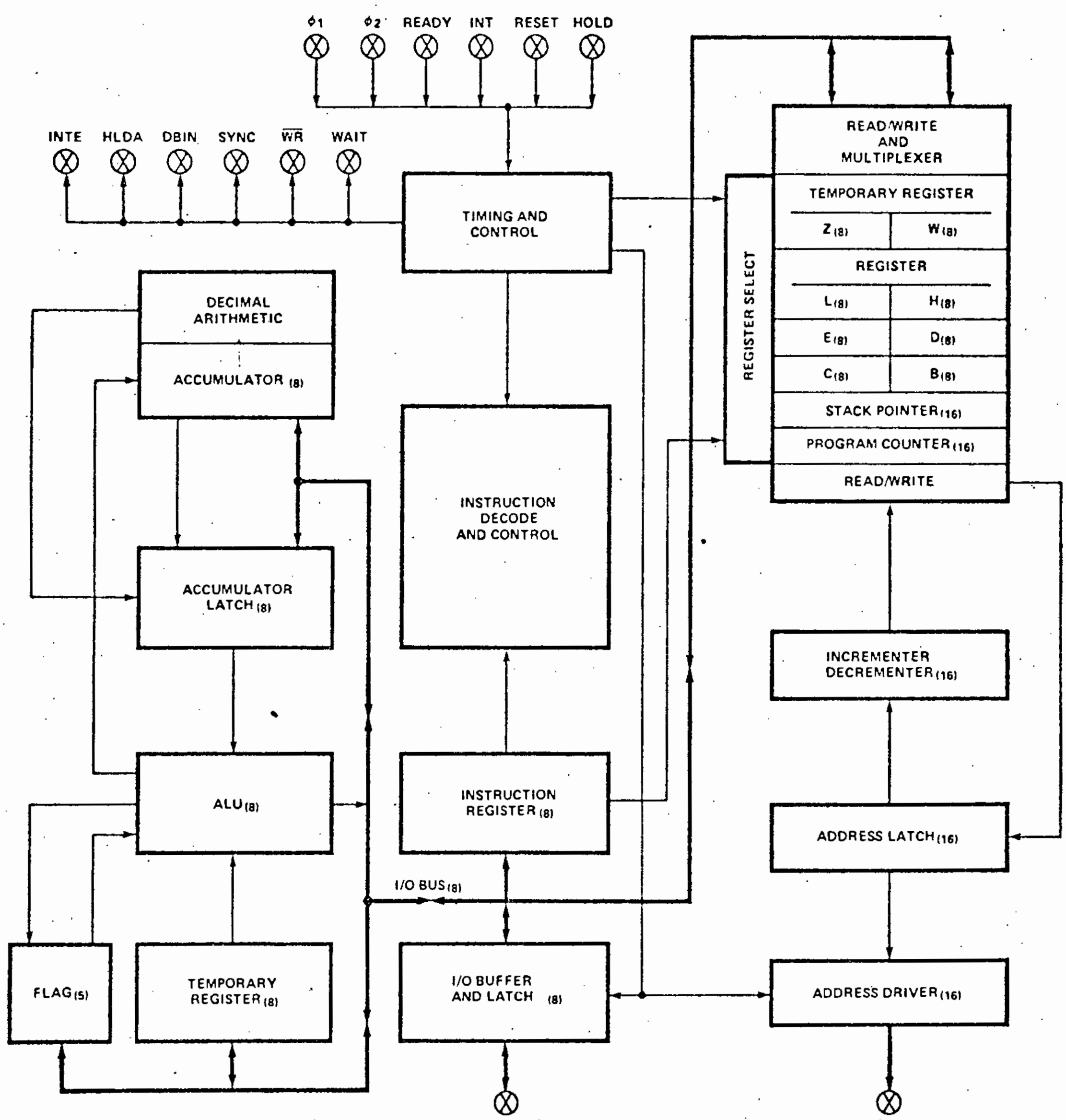


Figure 4. 8080 Block Diagram

INTERRUPT SEQUENCES

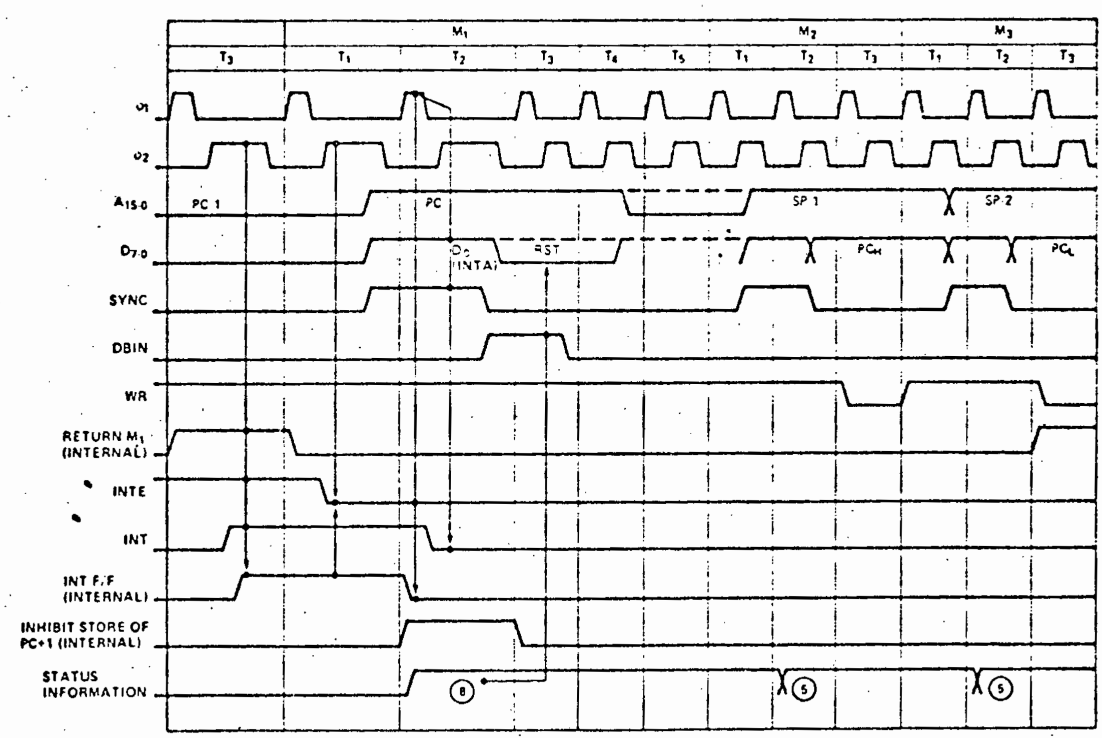
The 8080 has the built-in capacity to handle external interrupt requests. A peripheral device can initiate an interrupt simply by driving the processor's interrupt (INT) line high.

The interrupt (INT) input is asynchronous, and a request may therefore originate at any time during any instruction cycle. Internal logic re-clocks the external request, so that a proper correspondence with the driving clock is established. As Figure 2-8 shows, an interrupt request (INT) arriving during the time that the interrupt enable line (INTE) is high, acts in coincidence with the ϕ_2 clock to set the internal interrupt latch. This event takes place during the last state of the instruction cycle in which the request occurs, thus ensuring that any instruction in progress is completed before the interrupt can be processed.

The INTERRUPT machine cycle which follows the arrival of an enabled interrupt request resembles an ordinary FETCH machine cycle in most respects. The M_1 status bit is transmitted as usual during the SYNC interval. It is accompanied, however, by an INTA status bit (D_0) which acknowledges the external request. The contents of the program counter are latched onto the CPU's address lines during T_1, but the counter itself is not incremented during the INTERRUPT machine cycle, as it otherwise would be. In this way, the pre-interrupt status of the program counter is preserved, so that data in the counter may be restored by the interrupted program after the interrupt request has been processed.

The interrupt cycle is otherwise indistinguishable from an ordinary FETCH machine cycle. The processor itself takes no further special action. It is the responsibility of the peripheral logic to see that an eight-bit interrupt instruction is "jammed" onto the processor's data bus during state T_3. In a typical system, this means that the data-in bus from memory must be temporarily disconnected from the processor's main data bus, so that the interrupting device can command the main bus without interference.

The 8080's instruction set provides a special one-byte call which facilitates the processing of interrupts (the ordinary program Call takes three bytes). This is the RESTART instruction (RST). A variable three-bit field embedded in the eight-bit field of the RST enables the interruoting device to direct a Call to one of eight fixed memory locations. The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK.



NOTE: Ⓝ Refer to Status Word Chart on Page 2-6.

Figure 2-8. Interrupt Timing

APPENDIX V
ELECTRICAL SPECIFICATIONS

NOTE: This electrical and timing specification is only preliminary. No assurance can be given at this time that some changes will not occur during the engineering testing and characterization of this product. The final specification will be released in late May, 1974.

Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . −65°C to +150°C
All Input or Output Voltages with respect to the most negative supply voltage, V_{BB} . . . . +25V to −0.3V
Supply Voltages V_{DD} and V_{SS} with respect to V_{BB} . . . . +20V to −0.3V
Power Dissipation 1.0W

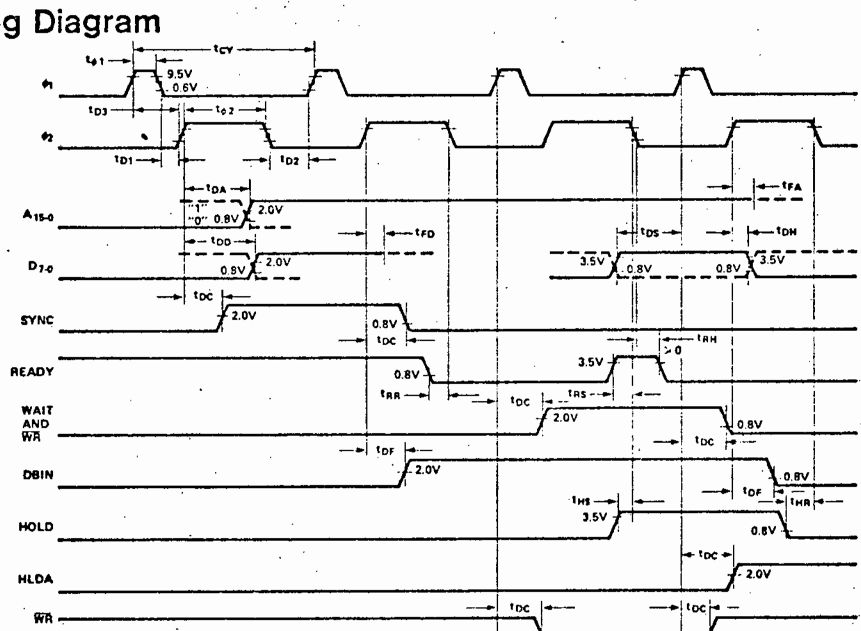
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1.0$		0.6	V	
V_{IHC}	Clock Input High Voltage	10.4		V_{DD}	V	
V_{IL}	Input Low Voltage	V_{SS}		0.8	V	I_{OL} = 1.7mA On Data Bus
V_{IH}	Input High Voltage	3.3		V_{CC}	V	I_{OL} = 0.75mA On All Others
V_{OL}	Output Low Voltage			0.45	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 100μA
I_{DD1}	Power Supply Current (V_{DD}) during $\overline{HOLD}$			60	mA	Continuous Operation T_A = 25°C T_{CY} = 480ns
I_{DD2}	Power Supply Current (V_{DD}) during HOLD			67	mA	
I_{CC1}	Power Supply Current (V_{CC}) during $\overline{HOLD}$			75	mA	
I_{CC2}	Power Supply Current (V_{CC}) during HOLD			73	mA	
I_{BB}	Power Supply Current			1	mA	

Timing Diagram



A. C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.48		2.0	μs	
$t_R t_F$	Clock Rise and Fall Times			50	ns	
$t_{\phi 1}$	Pulse Width of ϕ_1	60			ns	
$t_{\phi 2}$	Pulse Width of ϕ_2	220			ns	
t_{D1}	Clock Delay between ϕ_1 and ϕ_2	0			ns	
t_{D2}	Clock Delay between ϕ_2 and ϕ_1	70			ns	
t_{DA}	Address Output Delay from ϕ_2			200	ns	
t_{DD}	Data Output Delay from ϕ_2			220	ns	
t_{DC}	Control Signal Output Delay from ϕ_1 or ϕ_2 (SYNC, $\overline{WR}$, WAIT and HLDA)			120	ns	1 T^2L and CL=50pF
t_{DF}	DBIN Output Delay from ϕ_2	25		140	ns	
t_{D3}	Clock Delay ϕ_1 to ϕ_2	130			ns	
t_{DS}	Data Setup Time to ϕ_1 during DBIN	20			ns	
t_{DH}	Data Hold Time from ϕ_2 during DBIN	t_{DF}			ns	
t_{RR}	Ready Reset Time during ϕ_2	120			ns	
t_{RS}	Ready Setup Time during ϕ_2	110			ns	
t_{HR}	Hold Reset Time during ϕ_2	110			ns	
t_{HS}	Hold Setup Time during ϕ_2	70			ns	
t_{FA}	Address Delay to Enter Hold State			150	ns	
t_{FD}	Data Delay to Enter Hold State			150	ns	

Capacitance $T_A = 25°C$; Unmeasured Pins Grounded

Symbol	Test	Limit (pF) Typ.	Max.
$C_{\phi 1}$	Clock 1 Capacitance	10	20
$C_{\phi 2}$	Clock 2 Capacitance	10	20
C_{IN}	Input Capacitance	4	8
C_{OUT}	Output Capacitance (Address In High Impedance State)	5	10

MNEMONIC	OP CODE $D_7D_6D_5D_4$	OP CODE $D_3D_2D_1D_0$	M1[1] T1	M1 T2[2]	M1 T3	M1 T4	M1 T5	M2 T1	M2 T2[2]	M2 T3
MOV r1,r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	0 1 1 0				X[3]		HL OUT STATUS[6]	DATA	→DDD
MOV M, r	0 1 1 1	0 S S S				(SSS)→TMP		HL OUT STATUS[7]	(TMP)	→DATA BUS
SPHL	1 1 1 1	1 0 0 1				(HL)	→SP			
MVI r, data	0 0 D D	D 1 1 0				X		PC OUT STATUS[6]	B2	→DDD
MVI M, data	0 0 1 1	0 1 1 0				X			B2	→TMP
LXI rp, data	0 0 R P	0 0 0 1				X			PC = PC + 1 B2	→rl
LDA addr	0 0 1 1	1 0 1 0				X			PC = PC + 1 B2	→Z
STA addr	0 0 1 1	0 0 1 0				X			PC = PC + 1 B2	→Z
LHLD addr	0 0 1 0	1 0 1 0				X			PC = PC + 1 B2	→Z
SHLD addr	0 0 1 0	0 0 1 0				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
LDAX rp[4]	0 0 R P	1 0 1 0				X		rp OUT STATUS[6]	DATA	→A
STAX rp[4]	0 0 R P	0 0 1 0				X		rp OUT STATUS[7]	(A)	→DATA BUS
XCHG	1 1 1 0	1 0 1 1				(HL)↔(DE)				
ADD r	1 0 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
ADI data	1 1 0 0	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
ADC r	1 0 0 0	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
ACI data	1 1 0 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
SUB r	1 0 0 1	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
SUI data	1 1 0 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
SBB r	1 0 0 1	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
SBI data	1 1 0 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
INR r	0 0 D D	D 1 0 0				(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0				X		HL OUT STATUS[6]	DATA (TMP)+1	→TMP →ALU
DCR r	0 0 D D	D 1 0 1				(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1				X		HL OUT STATUS[6]	DATA (TMP)-1	→TMP →ALU
INX rp	0 0 R P	0 0 1 1				(RP) + 1	→RP			
DCX rp	0 0 R P	1 0 1 1				(RP) - 1	→RP			
DAD rp[8]	0 0 R P	1 0 0 1				X		(rl)→ACT	(L)→TMP, (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1				DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]	DATA	→TMP

MNEMONIC	OP CODE $D_7D_6D_5D_4$	OP CODE $D_3D_2D_1D_0$	M3 T1	M3 T2[2]	M3 T3	M4 T1	M4 T2[2]	M4 T3	M5 T1	M5 T2[2]	M5 T3	M5 T4	M5 T5
MOV r1,r2	0 1 D D	D S S S											
MOV r, M	0 1 D D	0 1 1 0											
MOV M, r	0 1 1 1	0 S S S											
SPHL	1 1 1 1	1 0 0 1											
MVI r, data	0 0 D D	D 1 1 0											
MVI M, data	0 0 1 1	0 1 1 0	HL OUT STATUS[7]	(TMP)	→DATA BUS								
LXI rp, data	0 0 R P	0 0 0 1	PC OUT STATUS[6]	PC = PC + 1 B3	→rh								
LDA addr	0 0 1 1	1 0 1 0		PC = PC + 1 B3	→W	WZ OUT STATUS[6]	DATA	→A					
STA addr	0 0 1 1	0 0 1 0		PC = PC + 1 B3	→W	WZ OUT STATUS[7]	(A)	→DATA BUS					
LHLD addr	0 0 1 0	1 0 1 0		PC = PC + 1 B3	→W	WZ OUT STATUS[6]	DATA WZ = WZ + 1	→L	WZ OUT STATUS[6]	DATA	→H		
SHLD addr	0 0 1 0	0 0 1 0	PC OUT STATUS[6]	PC = PC + 1 B3	→W	WZ OUT STATUS[7]	(L) WZ = WZ + 1	→DATA BUS	WZ OUT STATUS[7]	(H)	→DATA BUS		
LDAX rp[4]	0 0 R P	1 0 1 0											
STAX rp[4]	0 0 R P	0 0 1 0											
XCHG	1 1 1 0	1 0 1 1											
ADD r	1 0 0 0	0 S S S											
ADD M	1 0 0 0	0 1 1 0	[9]	(ACT)+(TMP)→A									
ADI data	1 1 0 0	0 1 1 0	[9]	(ACT)+(TMP)→A									
ADC r	1 0 0 0	1 S S S											
ADC M	1 0 0 0	1 1 1 0	[9]	(ACT)+(TMP)+CY→A									
ACI data	1 1 0 0	1 1 1 0	[9]	(ACT)+(TMP)+CY→A									
SUB r	1 0 0 1	0 S S S											
SUB M	1 0 0 1	0 1 1 0	[9]	(ACT)-(TMP)→A									
SUI data	1 1 0 1	0 1 1 0	[9]	(ACT)-(TMP)→A									
SBB r	1 0 0 1	1 S S S											
SBB M	1 0 0 1	1 1 1 0	[9]	(ACT)-(TMP)-CY→A									
SBI data	1 1 0 1	1 1 1 0	[9]	(ACT)-(TMP)-CY→A									
INR r	0 0 D D	D 1 0 0											
INR M	0 0 1 1	0 1 0 0	HL OUT STATUS[7]	ALU	→DATA BUS								
DCR r	0 0 D D	D 1 0 1											
DCR M	0 0 1 1	0 1 0 1	HL OUT STATUS[7]	ALU	→DATA BUS								
INX rp	0 0 R P	0 0 1 1											
DCX rp	0 0 R P	1 0 1 1											
DAD rp[8]	0 0 R P	1 0 0 1	(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
DAA	0 0 1 0	0 1 1 1											
ANA r	1 0 1 0	0 S S S											
ANA M	1 0 1 0	0 1 1 0	[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE $D_7D_6D_5D_4$	OP CODE $D_3D_2D_1D_0$	M1[1] T1	M1 T2[2]	M1 T3	M1 T4	M1 T5	M2 T1	M2 T2[2]	M2 T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC ← PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC ← PC + 1 B2	→TMP
XRA r	1 0 1 0	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC ← PC + 1 B2	→TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC ← PC + 1 B2	→TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)-(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC ← PC + 1 B2	→TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				$(\bar{A})$→A				
CMC	0 0 1 1	1 1 1 1				$\overline{CY}$→CY				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z
CALL addr	1 1 0 0	1 1 0 1				SP ← SP - 1		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP ← SP - 1		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP ← SP + 1 DATA	→Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP ← SP + 1 DATA	→Z
RST n	1 1 N N	N 1 1 1			φ→W INST→TMP/IR	SP ← SP - 1		SP OUT STATUS[16]	SP ← SP - 1 (PCH)	→DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL)	→PC			
PUSH rp	1 1 R P	0 1 0 1				SP ← SP - 1		SP OUT STATUS[16]	SP ← SP - 1 (rh)	→DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP ← SP - 1		SP OUT STATUS[16]	SP ← SP - 1 (A)	→DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP ← SP + 1 DATA	→rl
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP ← SP + 1 DATA	→FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP ← SP + 1 DATA	→Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC ← PC + 1 B2	→Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0				X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC ← PC + 1	INST→TMP/IR	X				

MNEMONIC	M3 T1	M3 T2[2]	M3 T3	M4 T1	M4 T2[2]	M4 T3	M5 T1	M5 T2[2]	M5 T3	M5 T4	M5 T5		
ANI data	[9]	(ACT)+(TMP)→A											
XRA r													
XRA M	[9]	(ACT)+(TMP)→A											
XRI data	[9]	(ACT)+(TMP)→A											
ORA r													
ORA M	[9]	(ACT)+(TMP)→A											
ORI data	[9]	(ACT)+(TMP)→A											
CMP r													
CMP M	[9]	(ACT)-(TMP); FLAGS											
CPI data	[9]	(ACT)-(TMP); FLAGS											
RLC													
RRC													
RAL													
RAR													
CMA													
CMC													
STC													
JMP addr	PC OUT STATUS[6]	PC ← PC + 1 B3	→W									WZ OUT STATUS[11]	(WZ) + 1 → PC
J cond addr[17]	PC OUT STATUS[6]	PC ← PC + 1 B3	→W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
CALL addr	PC OUT STATUS[6]	PC ← PC + 1 B3	→W	SP OUT STATUS[16]	(PCH) SP ← SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL)	→DATA BUS			WZ OUT STATUS[11]	(WZ) + 1 → PC
C cond addr[17]	PC OUT STATUS[6]	PC ← PC + 1 B3	→W[13]	SP OUT STATUS[16]	(PCH) SP ← SP - 1	→DATA BUS	SP OUT STATUS[16]	(PCL)	→DATA BUS			WZ OUT STATUS[11,12]	(WZ) + 1 → PC
RET	SP OUT STATUS[15]	SP ← SP + 1 DATA	→W									WZ OUT STATUS[11]	(WZ) + 1 → PC
R cond addr[17]	SP OUT STATUS[15]	SP ← SP + 1 DATA	→W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
RST n	SP OUT STATUS[16]	(TMP = 00NNN000) (PCL)	→Z →DATA BUS									WZ OUT STATUS[11]	(WZ) + 1 → PC
PCHL													
PUSH rp	SP OUT STATUS[16]	(rl)	→DATA BUS										
PUSH PSW	SP OUT STATUS[16]	FLAGS	→DATA BUS										
POP rp	SP OUT STATUS[15]	SP ← SP + 1 DATA	→rh										
POP PSW	SP OUT STATUS[15]	SP ← SP + 1 DATA	→A										
XTHL	SP OUT STATUS[15]	DATA	→W	SP OUT STATUS[16]	(H)	→DATA BUS	SP OUT STATUS[16]	(L)	→DATA BUS	(WZ)	→HL		
IN port	WZ OUT STATUS[18]	DATA	→A										
OUT port	WZ OUT STATUS[18]	(A)	→DATA BUS										
EI													
DI													
HLT													
NOP													

NOTES:

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines (A_{0-15}) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17. CONDITION

CONDITION	CCC
NZ — not zero (Z = 0)	000
Z — zero (Z = 1)	001
NC — no carry (CY = 0)	010
C — carry (CY = 1)	011
PO — parity odd (P = 0)	100
PE — parity even (P = 1)	101
P — plus (S = 0)	110
M — minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 (A_{0-7}) and 8-15 (A_{8-15}).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).

SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

APPENDIX C.

LOW POWER SCHOTTKY TTL

Ref. 20.

Introduction:

For many years TTL has been the most popular digital integrated circuit technology. As the average IC complexity has increased to MSI (medium scale integration) the cost and size of the power supply and the difficulty of removing heat dissipated in TTL circuits, have become increasingly important factors. Recent improvements in semi-conductor processing have lead to low power Schottky TTL making it possible not only to reduce TTL power consumption significantly but also to improve the speed over that of Standard TTL.

The Schottky Diode:

A Schottky diode, also called a hot carrier diode, offers two big advantages over the conventional P-N junction diode - very high speed due to extremely short recovery time and a substantially lower forward voltage drop for a given current. (About 300 mV less than a P-N junction diode). A Schottky diode is formed by the metal-to-semiconductor contact at the surface of the semi-conductor crystal and relies on majority carriers for current transport (minority carriers used in P-N junctions diodes). Charge storage is negligible and forward-to-reverse recovery is extremely fast. There are two classes of metal-semi conductor contacts. Those with linear characteristics and those with non-linear ones. The Schottky barrier diode has a non-linear rectifying characteristic. The linearity is a function of the metal, the semiconductor and the doping level.

Schottky TTL:

With the use of Schottky diodes, the saturation delay normally encountered in saturated logic (e.g. TTL) can be avoided. Saturated logic operates by turning the transistors either fully on or fully off. The amount of base current to do this is critical. Too little will not turn the base current on sufficiently, too much will drive the transistor into saturation and it will continue to conduct when the base current has been removed, until excess charge in the base disappears, usually through thermal recombination. Conventional TTL circuits use gold doping to increase the probability of thermal base-charge recombination thus decreasing saturation delays. This also lowers the transistors current gain (beta) and makes the circuit less efficient.

A circuit trick, the Baker clamp was developed to overcome this problem. A diode is connected between the base and the collector. If the diode has a very low forward voltage drop it starts conducting when the base is forward biased with respect to the collector. Excess current applied to the base flows to the collector and the transistor only receives the base current necessary to pull the collector into the "soft saturation" region.

There is no excess charge and hence saturation delay is non-existent. The Schottky Barrier diode has the desirable characteristics for the diode in the Baker clamp.

These Schottky TTL circuits are very fast, but since emphasis is on speed they consume more power than normal TTL. Low power Schottky TTL consumes one-quarter the current of conventional TTL and uses Schottky diode clamping and advanced processing techniques to produce better switching transistors than TTL.

CIRCUIT CHARACTERISTICS:

While the logic function and base structure of low power Schottky are the same as TTL, there are also significant differences.

Input Configuration:

LSTTL is considered part of the TTL family but does not use the multi-emitter input structure that originally gave TTL its name. A DTL type input circuit with Schottky diodes to perform the AND function is employed. This increases the input breakdown voltage to 15V. The inputs also have Schottky clamping diodes which terminate negative going signals and thus minimise ringing. The effective capacitance of an LSTTL input is approximately 3.3pf.

Unused Inputs:

For best noise immunity and switching speed unused inputs should not be left floating. They can be handled in two ways :-

A. Connect unused input to Vcc. No series resistor is required as in TTL as LSTTL has an input break-down voltage of about 15V.

B. Connect the unused input to the output of an unused gate that is forced HIGH.

Unused inputs should not be connected to other inputs of the same gate as in TTL as AC noise immunity will be reduced due to increased input capacitance.

Output Configuration:

There are a number of changes in the design of the output stage of the LS gate which make for more efficient switch, but the most significant variation from the TTL output is the Schottky diode in series with the Darlington collector resistor. This allows the output to be pulled higher than Vcc, say to 10V, convenient for interfacing to CMOS. Early designs of LS had the output clamped one diode drop above Vcc.

The output impedance of LSTTL is closer to the characteristic impedance of the interconnections commonly used with TTL than standard TTL thus reducing ringing.

Output Waveforms:

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting edge rate is approximately 0,4V/nS with a 15 pF load and 0,25V/nS with a 50pF load. For analytical purposes the waveform can be approximated by the following expression

$$V(t) = V_{OL} + 3,7\ (1 - \exp\ (-t/T)$$

$$\text{where } T = 8\text{ns for } C_L = 15 \text{ pF}$$

$$16\text{nS for } C_L = 50 \text{ pF}$$

The falling output signal waveform resembles that part of cosine wave between 0 and 180 degrees. Fall times from 90% to 10% are approximately 4.5nS with a 15pF load and 8,5nS with a 50pF load. Equivalent edge rates are approximately 0,8 and 0,4 V/nS respectively. For analytical purposes the output waveform can be approximated by the following :

$$V(t) = V_{OL} + 1,9\ u(t)\ (1 + \cos wt) - 1,9u\ (t-a)(.1+\cos w\ (t-u))$$

where

$$u(t) = 0 \text{ for } t<0 \quad \text{and } u(t-a) = 0 \text{ for } t < a$$

$$= 1 \text{ for } t>0 \qquad\qquad = 1 \text{ for } t > a$$

For t in nanoseconds and C_L = 15 pf & C_L = 50 pf

	a = 7,5 nS	a = 14 nS
	w = 0,42	W = 0,23

AC Switching Characteristics:

Low power Schottky gates have an average propagation delay of 5nS at a 15 pF load. This increases at approximately 0,1nS/pF. Although some drive capability is lost by using high value resistors and small transistor geometries in LSTTL, this is counter balanced by using non-gold doped transistors with much higher current gain than those in conventional TTL. At say 200 pf loads LSTTL is still faster than conventional TTL.

Under static conditions only CMOS uses less power than LSTTL, but CMOS loses this advantage over a few 100 kHz. At speeds over 1 MHz, LSTTL is the most efficient logic.

The delay times of LSTTL are very insensitive to temperature and power supply variations, varying by only 2nS and 1nS respectively over the entire military ranges. In conventional TTL 6nS variations over temperature range and several nS over supply voltage range are typical.

APPENDIX D.

USE AND OPERATION OF THE FRONT PANEL UNIT

This appendix describes the two basic functions that can be performed from the front panel, namely, control of the microprocessor, and use of the DMA facility.

A. CONTROL OF THE MICROPROCESSOR

This is done by three switches, RUN, STEP and RESET.

Reset:

Depressing this switch generates a HIGH on the RESET line of the 8080. The line goes LOW again when the switch is released. While the reset signal is activated the content of the program counter is cleared and the instruction register is set to 0. The INTE and HLDA flip flops are also reset. After the reset the program will start in location 0 in memory. This is the most convenient way of starting the processor running.

Step/Run:

These two switches control the state of the READY line. When the RUN switch is depressed the READY line goes HIGH and the processor will run from where-ever the program counter is at the time. For initiating a program a RESET then RUN sequence must be used.

When the STEP switch is depressed the READY line goes low at the end of the current instruction and the 8080 enters the WAIT state. Each subsequent activation of the STEP switch thereafter results in the execution of one instruction byte. This is useful for STEPPING through a program, byte by byte, and observing all information on the busses to debug either the program or the hardware. After each step the data and address buses and status bus contain the information of the next instruction. This is because the 8080 goes into the WAIT state after the instruction fetch cycle but before the execution cycle.

B. FRONT PANEL DMA CHANNEL

It is possible via the front panel direct memory access (DMA) channel to communicate directly with the processor's memory.

Write Mode:

When writing into a memory location the following steps must be performed :-

(1) CONSOLE switch ON - This enables the address bus and data bus switches.

(2) Set up memory address on address bus switches.

(3) Depress LOAD switch - This enters the memory switches in a register.

(4) Set up data or instruction on data bus switches.

(5) Press WRITE - The contents are now entered into memory.

The address register is automatically incremented. This is a useful feature when loading sequential memory location as only the data bus need be altered for each new instruction.

Read Mode:

When reading a memory location, the following steps must be performed :-

(1) Follow steps (1) to (4) for WRITE MODE.

(2) Press READ - The contents of the memory location will be displayed on the data bus. The next byte in memory may be read by simply pressing the READ switch again.

NOTE: (a) The CONSOLE switch must be OFF before attempting to RUN or STEP through a program.

(b) The DMA facility will not operate if the processor is in the middle of an output (OUT) instruction.

APPENDIX E.

DUAL SLOPE INTEGRATING

ANALOG - DIGITAL CONVERTERS

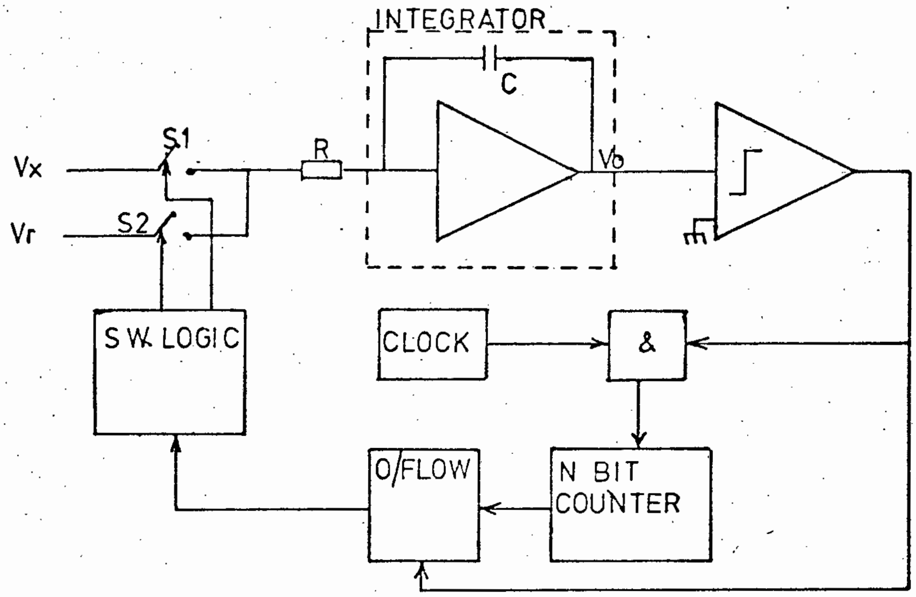
A block diagram of a dual slope integrating ADC is shown in fig. 23 A.

The conversion cycle consists of two distinct phases, as indicated by the up and down portions of the integrator output waveform shown in fig. 23 B. At time $t = 0$, the output of the integrator is equal to the effective comparitor threshold voltage, Vi. The control logic resets the counter to zero and closes switch S1 which connects the unknown voltage VX to the integrator input. The voltage Vx is integrated for a fixed time interval $(0, T_1)$ which is established by counting a fixed number of clock pulses. Although not necessary, it is convenient to have the number of pulses equal to the full scale count of 2^n in the case of an n-bit counter, so that the overflow pulse can be used to trigger subsequent operations.

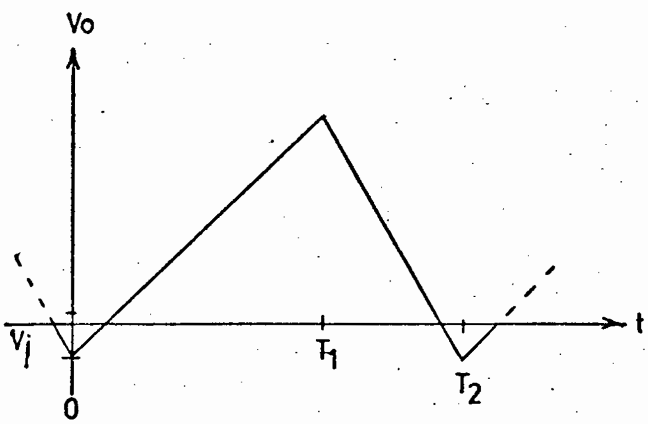
At time T_1, the integrator output is

$$Vo = \frac{1}{RC} \int_0^{T_1} Vx \, dt - Vi = \frac{1}{RC} \overline{V}x \; T_1 - Vi \qquad (1)$$

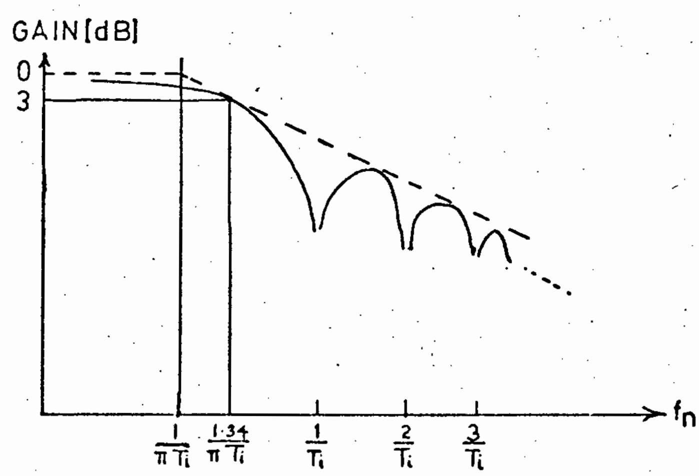
where $\overline{V}_x$ is the average value of Vx over the interval. The overflow pulse from the counter at time T_1 turns switch S1 off, and turns switch S2 on, thereby connecting the reference voltage -Vr to the integrator. The



(a) DUAL SLOPE INTEGRATING ADC



(b) ADC WAVEFORM



(c) ADC FREQUENCY RESPONSE

FIG. 23

output of the integrator during integration of -Vr is

$$Vo = -Vi + \frac{1}{RC} \overline{Vx}\, T_1 - \frac{1}{RC} \int_{T_1}^{t} Vr\, dt \qquad (2)$$

The integration continues until the comparitor changes state. At this time the integrator output voltage is equal to -Vi so that Eq. (2) becomes

$$-Vi = -Vi + \frac{1}{RC} \overline{Vx}\, T_1 - \frac{1}{RC} Vr\, (T_2 - T_1) \qquad (3)$$

where the reference voltage Vr is assumed constant. The Vi's drop out and the integration constant $\frac{1}{RC}$ cancels in the remaining terms. Solving for the average of the input signal

$$\overline{Vx} = Vr\, (T_2 - T_1) \;/\; T_1 \qquad (4)$$

If N is the number on the counter at time T_2 then $T_2 - T_1 = N/f_c$, where f_c is the clock frequency. Since $T_1 = 2^n/f_c$, Eq. (4) reduces to $Vx = Vr \frac{N}{2^n}$ (5)

Thus, the average value of the input voltage is proportional to the number in the counter at time T_2.

The cancellations that take place during the derivation are of considerable practical importance. The elimination of Vi in Eq. (3) shows that long term offset drift has no effect on the accuracy of the converter. Similarly the clock frequency F_c cancelled out of the final expression showing that long term frequency variations do not effect the result.

The cancellation of the integration constant $\frac{1}{RC}$ shows that neither the value of the RC product nor its variation with time and temperature, affects the operation of the converter. This is of considerable practical significance since low temperature coefficient capacitors and resistors are expensive components.

Another advantage of an integrating converter when compared with successive approximation and conventional ramp ADC's is less noise sensitivity. The other ADC's are noise sensitive because the comparison takes place between the instantaneous value of the input signal and reference voltage. In the dual slope integrating converter the comparison is between the reference and the time integral of the input voltage. If a noise perturbation has a small time integral compared to Vx T_1, it has only a slight effect on the comparison. In essence the input signal is being heavily filtered as a result of the integration. In addition the dual slope integrating ADC is isolated from the signal source at the time of comparison since S1 is off. This further decreases sensitivity to noise on the input signal.

The quantitative measure of noise rejection is derived by integrating a sine-wave over the converter integration period. If the rejection ratio Rn is defined as the attenuation resulting from integration this calculation results in

$$Rn = 20 \log T_1 / RC \quad + \quad 20 \log \frac{\mathrm{Sin}^2 \pi T_1 \, fn}{\pi T_1 \, fn}$$

where T_1 is the integration time and fn the frequency of the noise. The first term is a constant and can be compensated by adjustment of the ADC gain. The normalized attenuation characteristic is shown in fig. 23 C. As expected from physical reasoning, the rejection is infinite when the integration interval is an exact multiple of the period of the noise.

APPENDIX F.

LOGIC DRAWINGS

This appendix contains logic diagrams for -

(i) The Industrialized Microprocessor System;

(ii) Development System.

Exact wiring diagrams and parts lists can be found in the library of the Department of Electrical Engineering at the University of Cape Town.

Logic convensions used in the diagrams are :

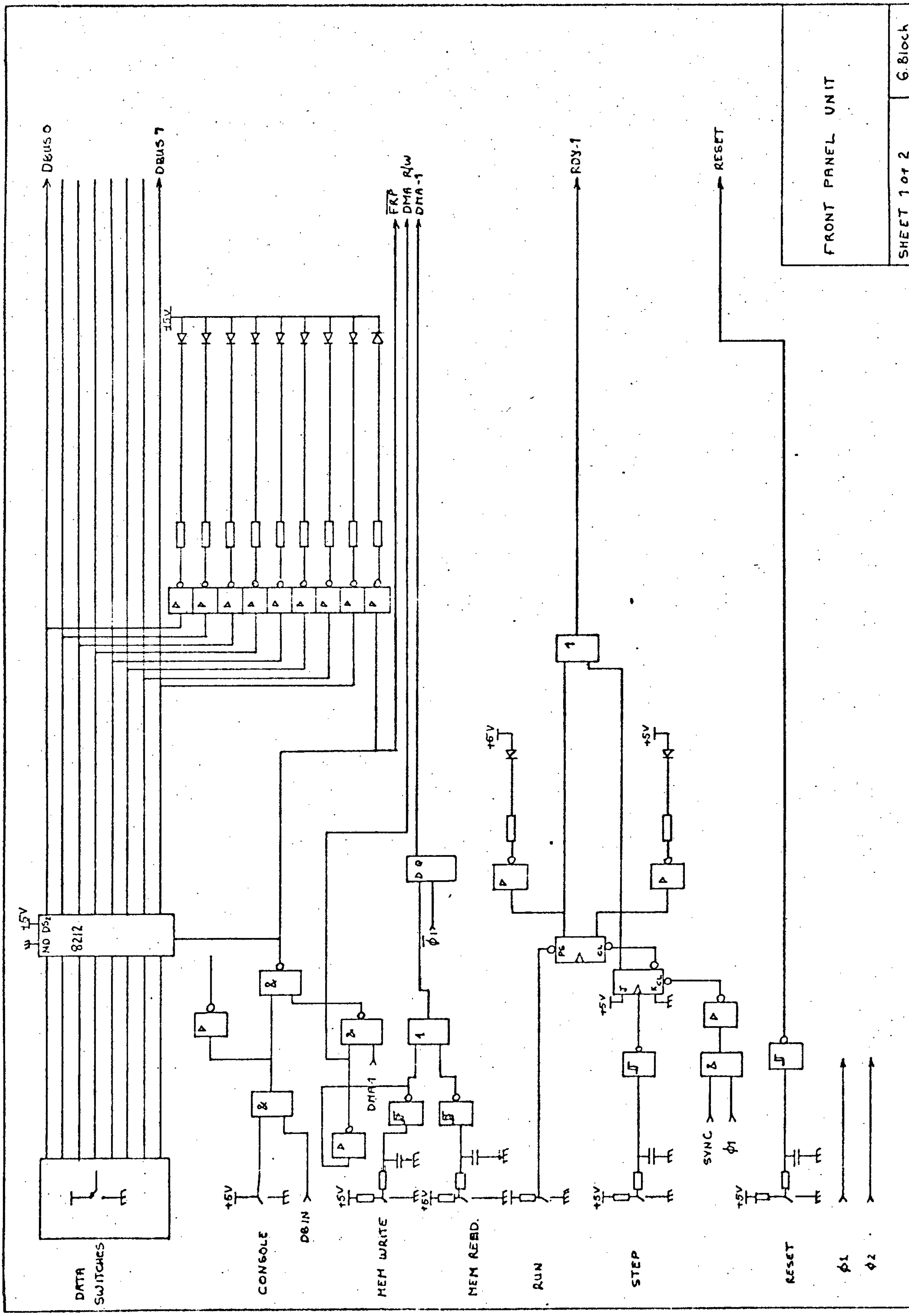
(i) Negative logic lines (lines that are normally HI and active LOW) have circles at each end.

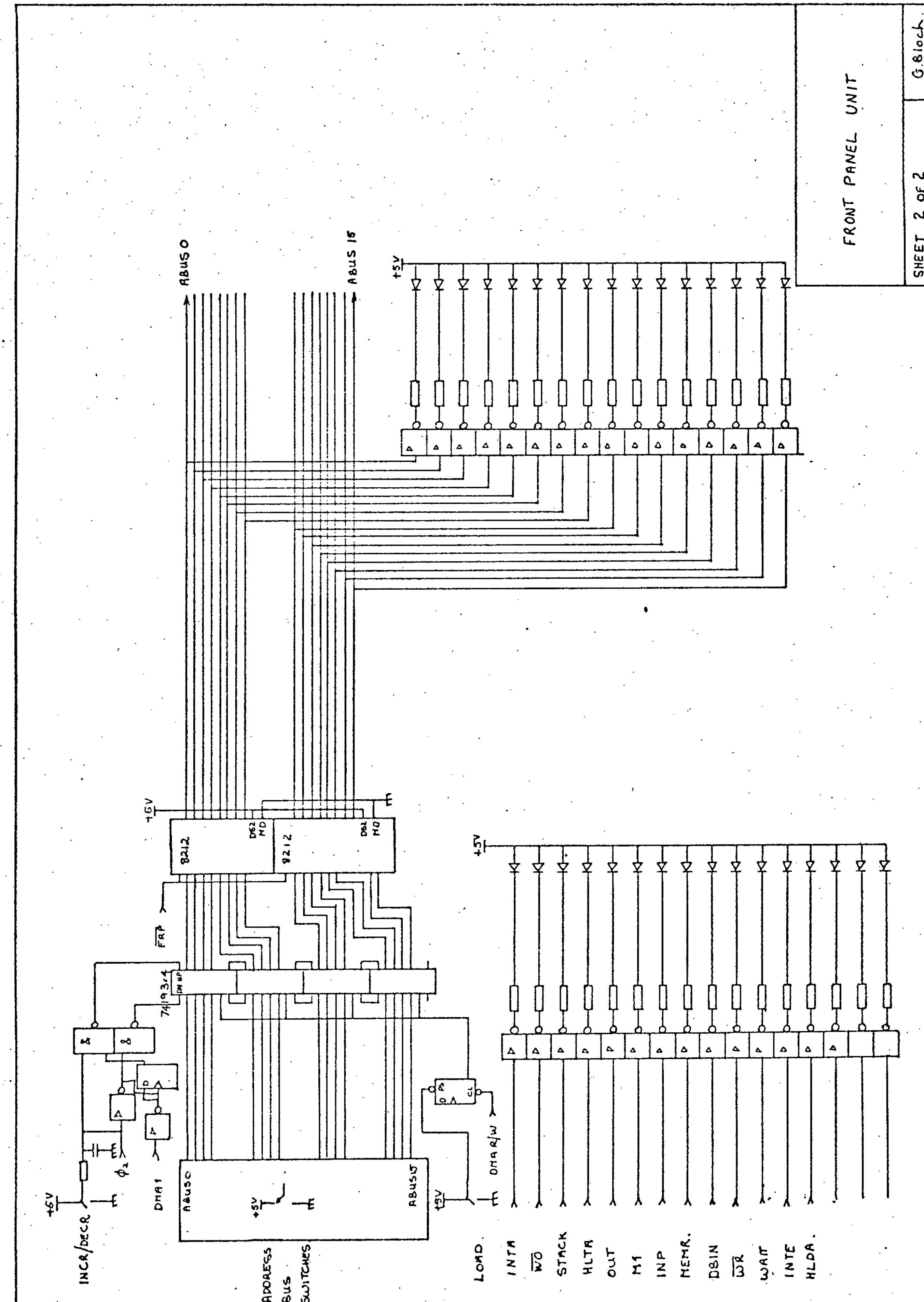
(ii) As a result of (i), gates that have been drawn for their logic meaning but are not directly implementable by TTL have the equivalent TTL gate numbers written above them.

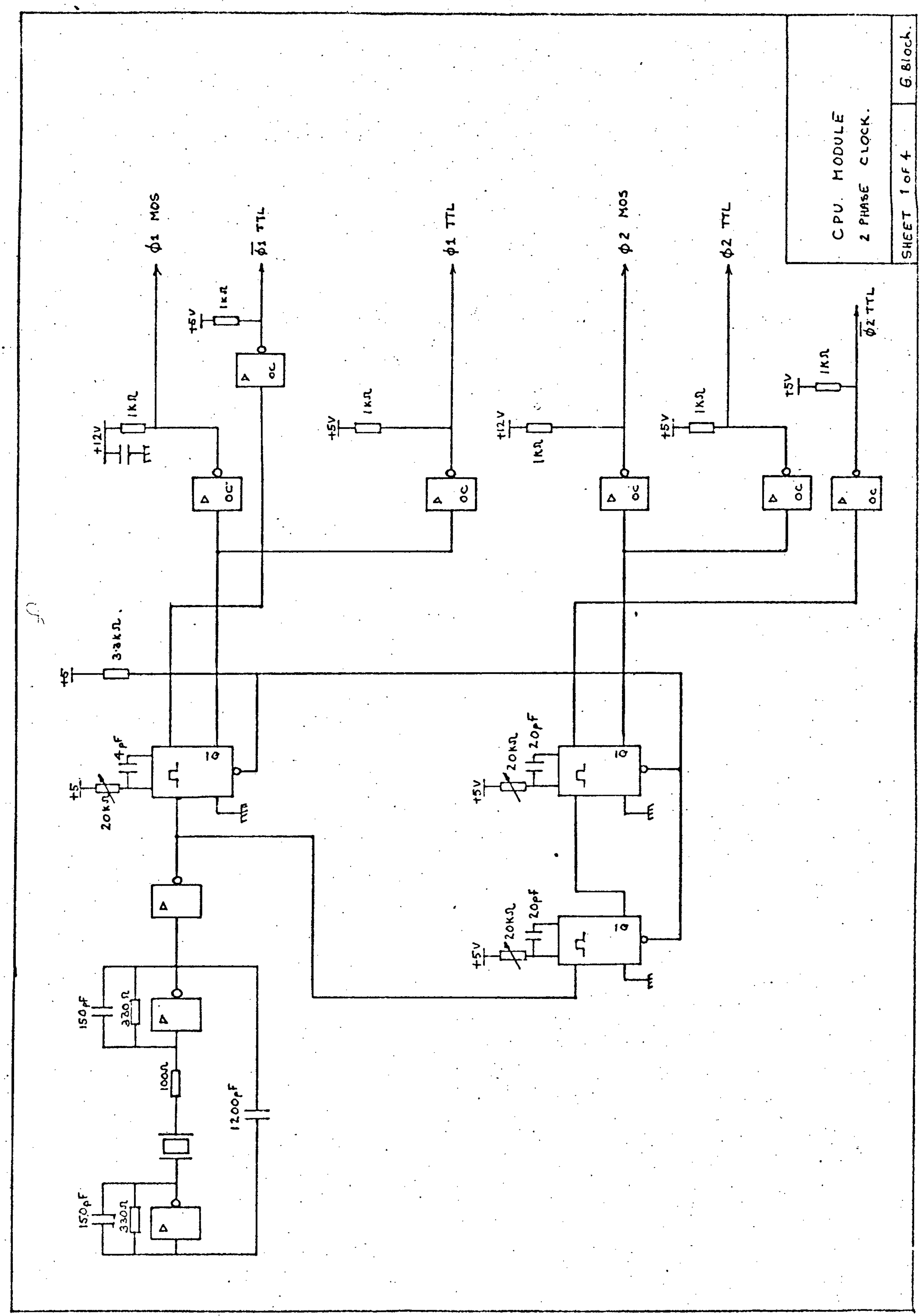
(iii) Gates or latches that have their outputs connected together are tri-state devices.

Appendix F (i)

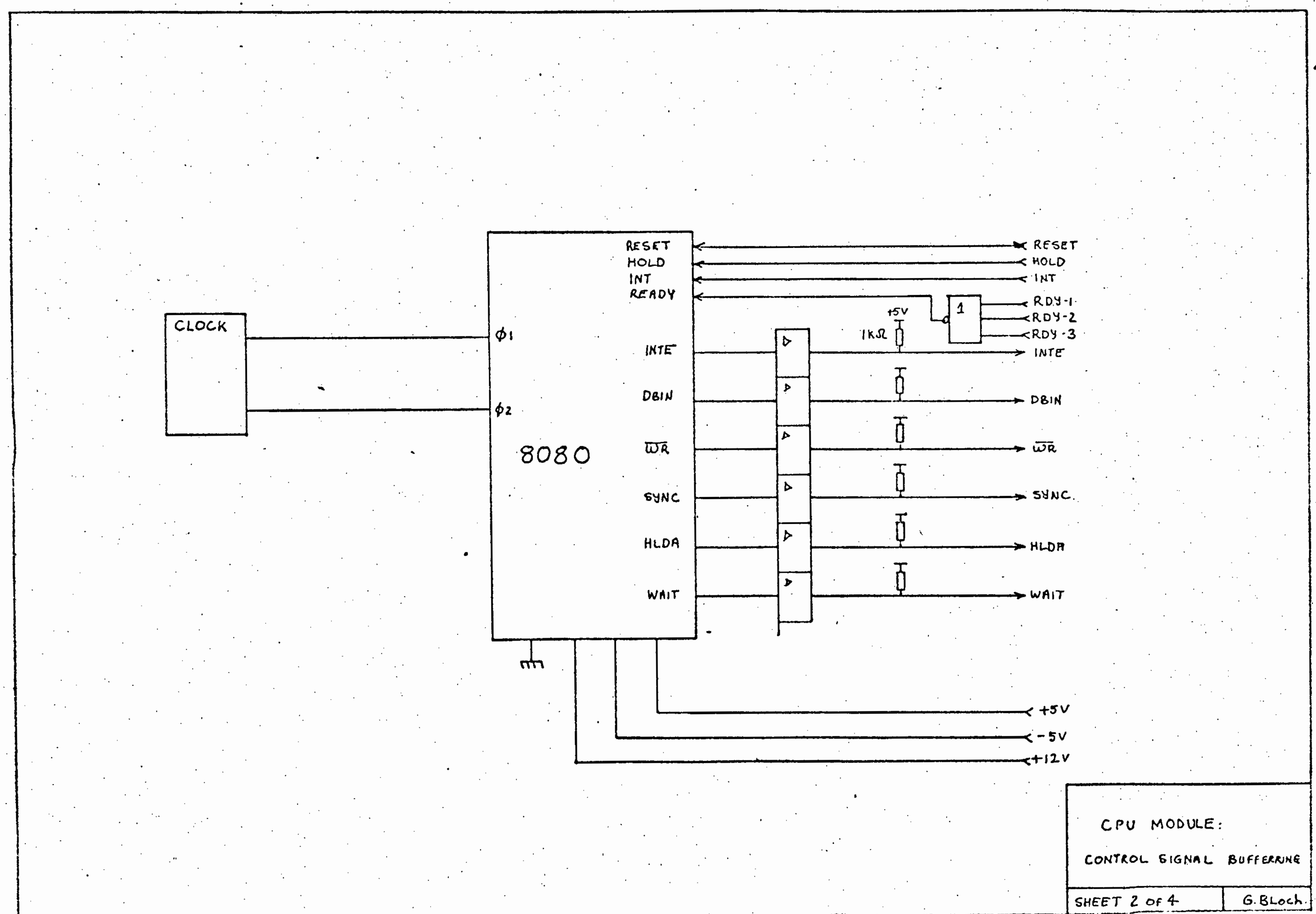
INDUSTRIALIZED MICROPROCESSOR SYSTEM - LOGIC DRAWINGS.

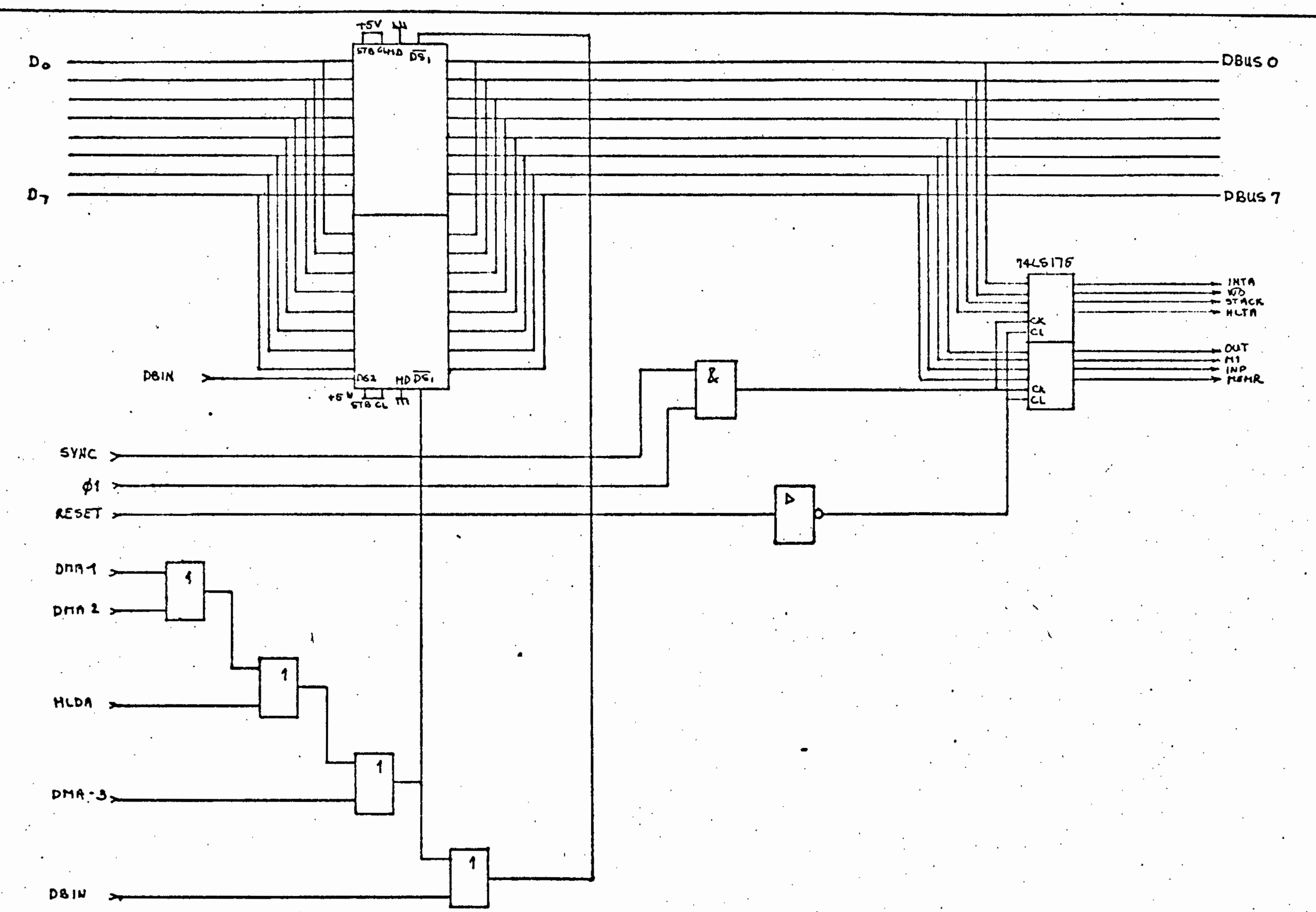

FRONT PANEL UNIT
SHEET 1 of 2
G. Bloch
DBUS 0
DBUS 7
FRP
DMA R/W
DMA-1
RDY-1
RESET
+5V
8212
ND DS2
$\overline{\phi 1}$
DMA-1
SYNC
φ1
DATA SWITCHES
CONSOLE
DBIN
MEM WRITE
MEM READ
RUN
STEP
RESET
φ1
φ2


FRONT PANEL UNIT
SHEET 2 of 2
G.Block
ABUS 0
ABUS 15
+5V
8212
8212
DS2 MD
DS1 MD
74193
FRP
INCR/DECR
+6V
φ2
DMA1
ABUS0
ABUS15
ADDRESS BUS SWITCHES
DMAR/W
LOAD
INTA
WO
STACK
HLTA
OUT
M1
INP
MEMR.
DBIN
WR
WAIT
INTE
HLDA.



CPU. MODULE
2 PHASE CLOCK.
SHEET 1 of 4
G. Bloch.
ϕ1 MOS
$\overline{ϕ1}$ TTL
ϕ1 TTL
ϕ2 MOS
ϕ2 TTL
$\overline{ϕ2}$ TTL
+12V
+5V
1KΩ
OC
3·3KΩ
20KΩ
4pF
20pF
150pF
330Ω
100Ω
1200pF

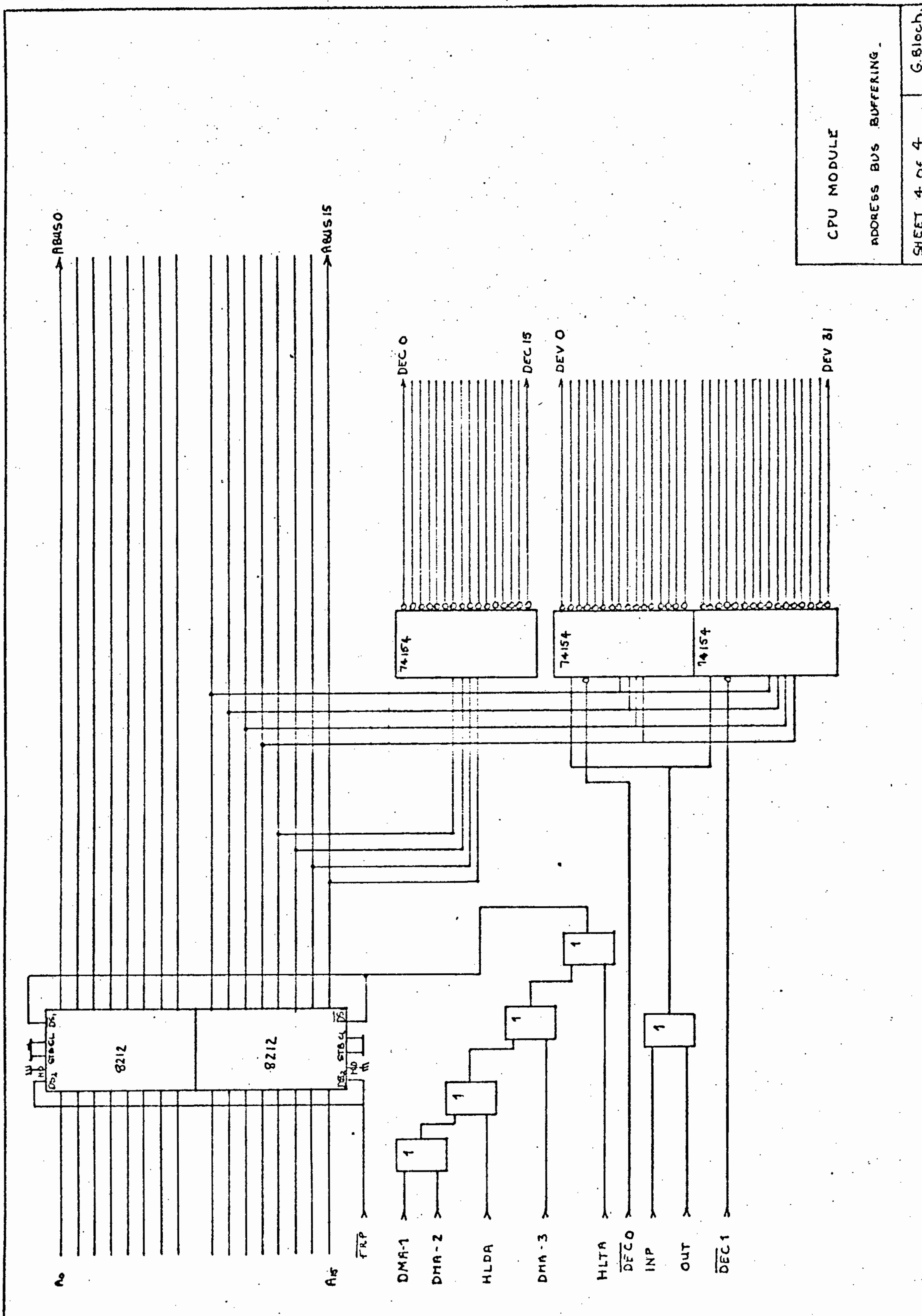

CLOCK
φ1
φ2
8080
RESET
HOLD
INT
READY
INTE
DBIN
WR
SYNC
HLDA
WAIT
+5V
1kΩ
1
RDY-1
RDY-2
RDY-3
+5V
-5V
+12V
CPU MODULE:
CONTROL SIGNAL BUFFERRING
SHEET 2 OF 4
G. Bloch.

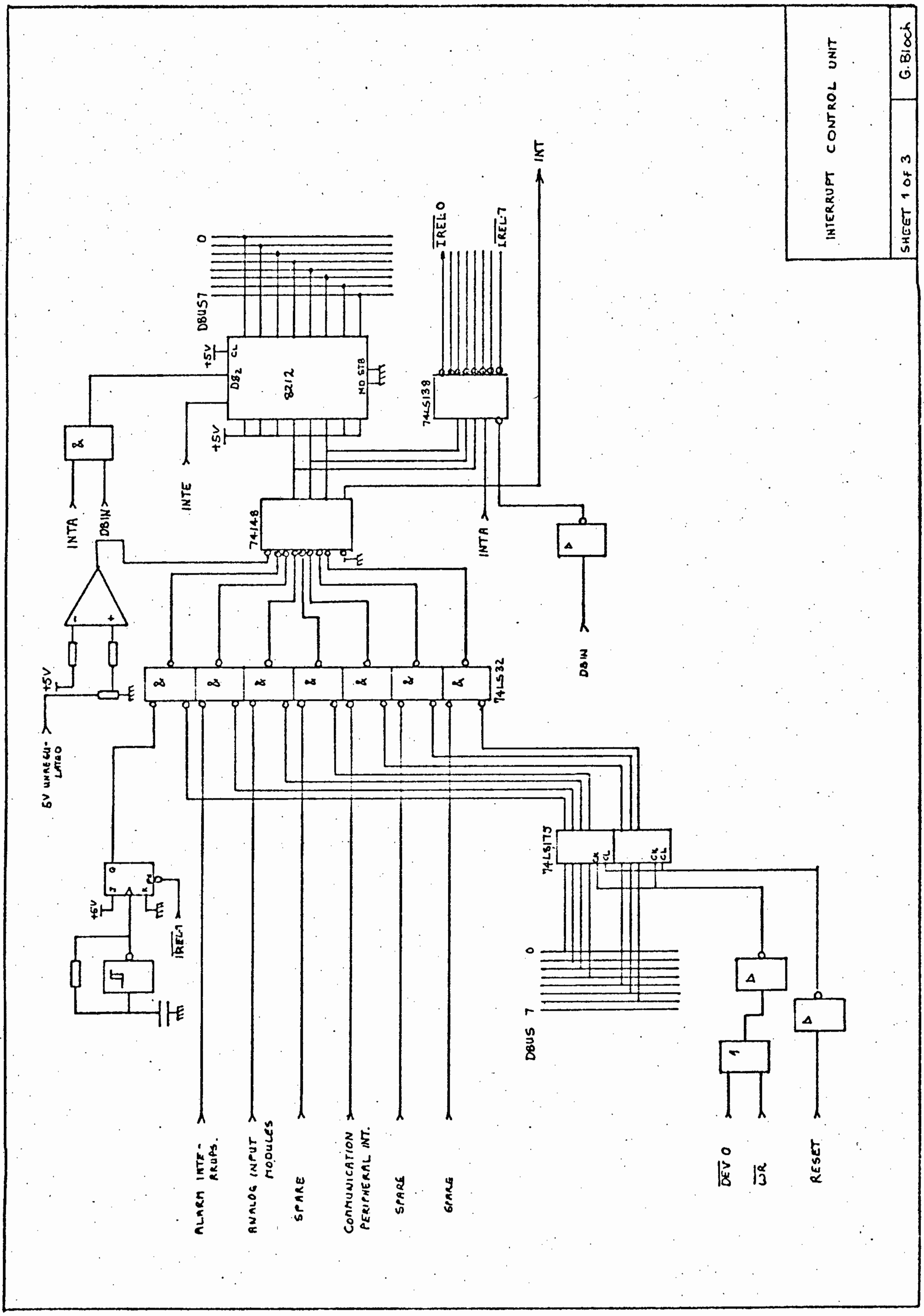


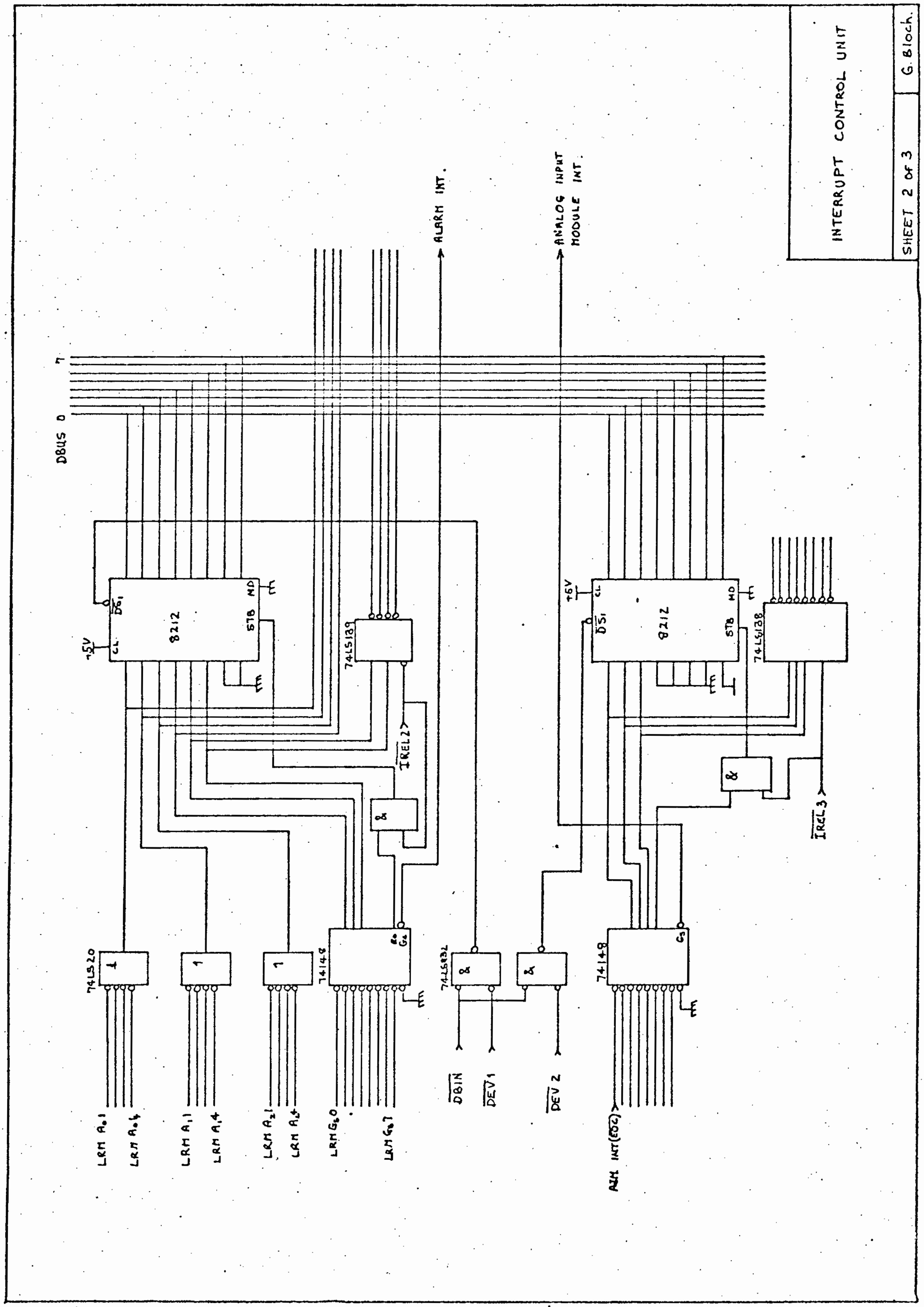
CPU MODULE.

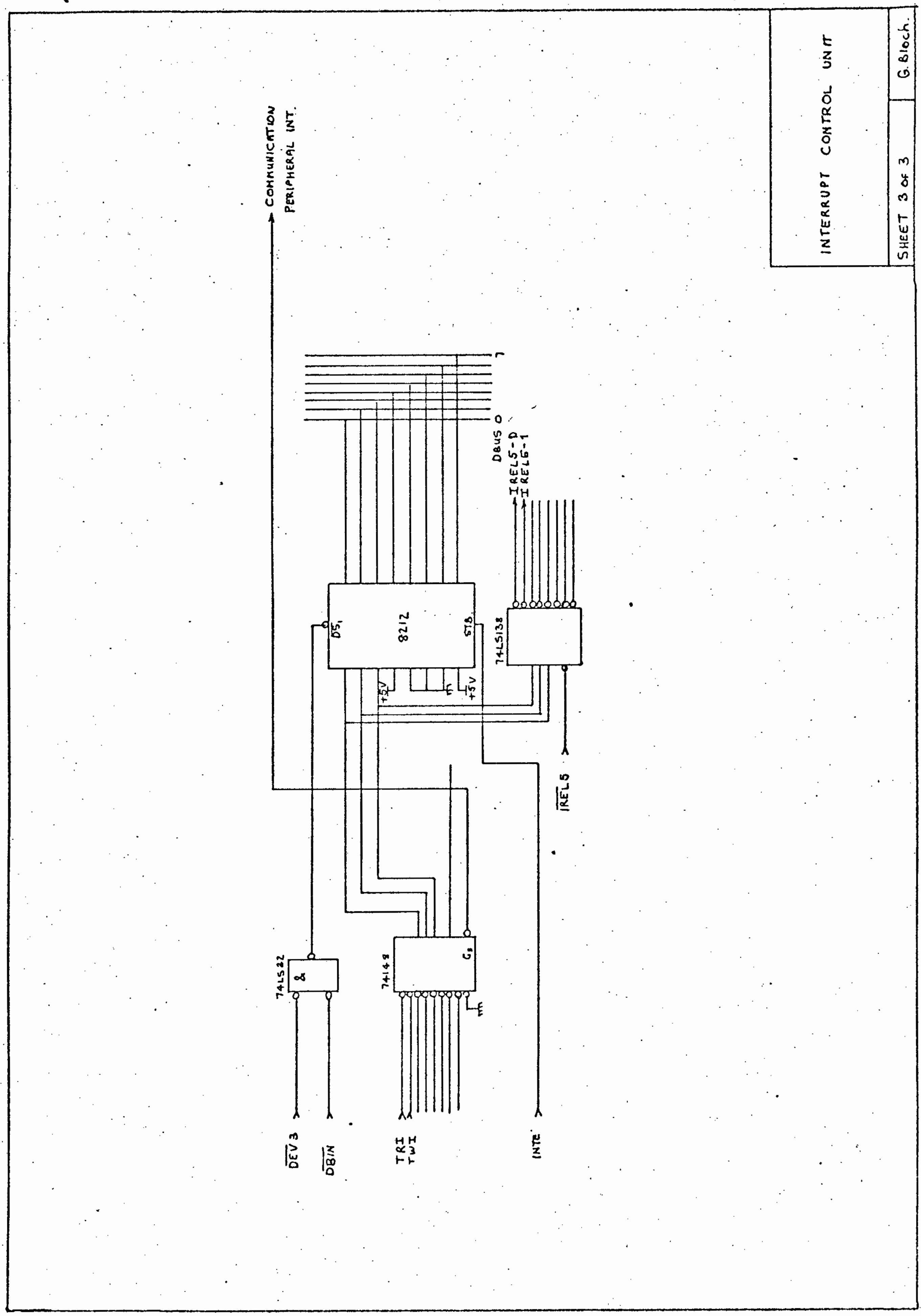
DATA BUS BUFFERING.

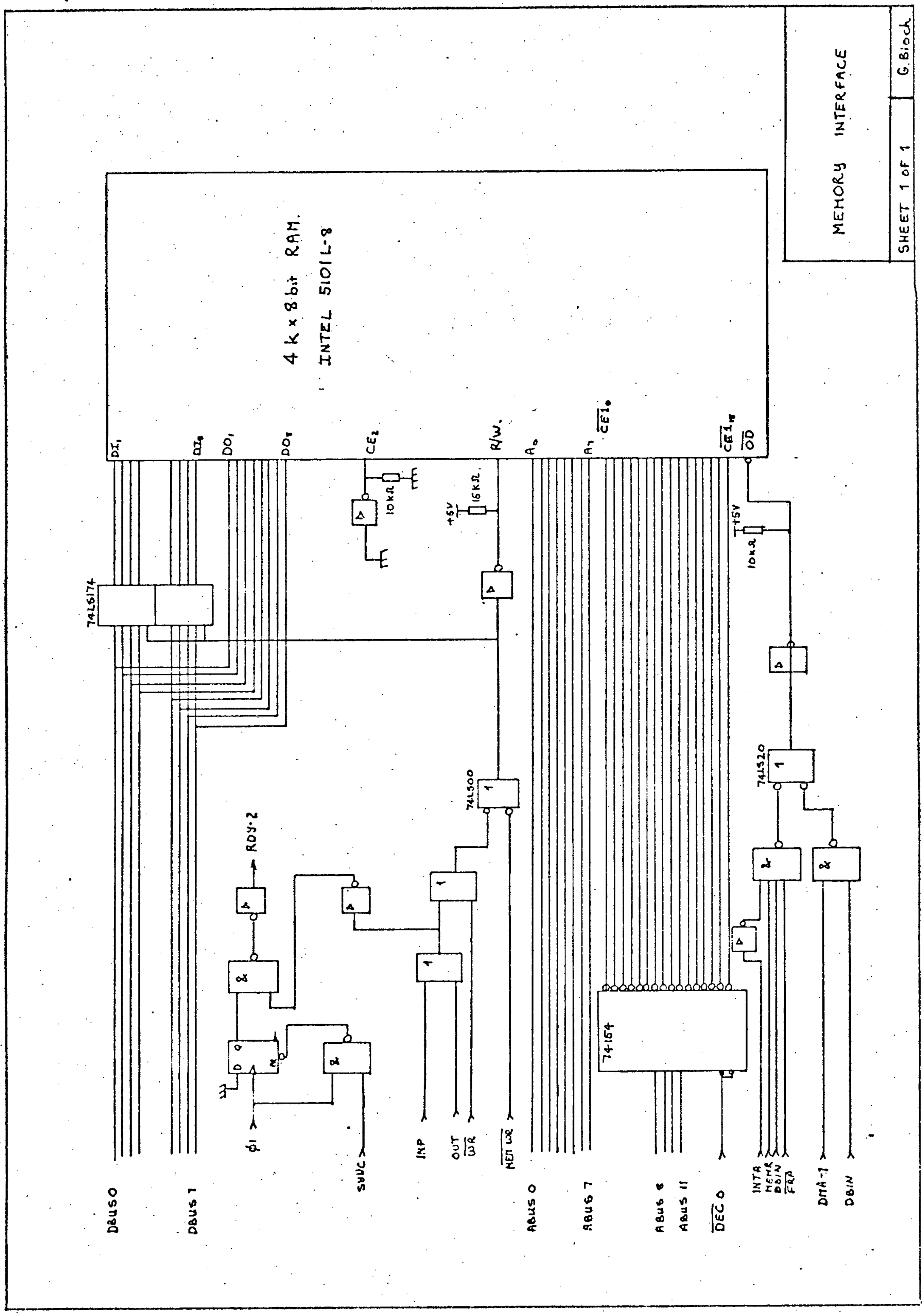
SHEET 3 of 4 | G. Bloch.

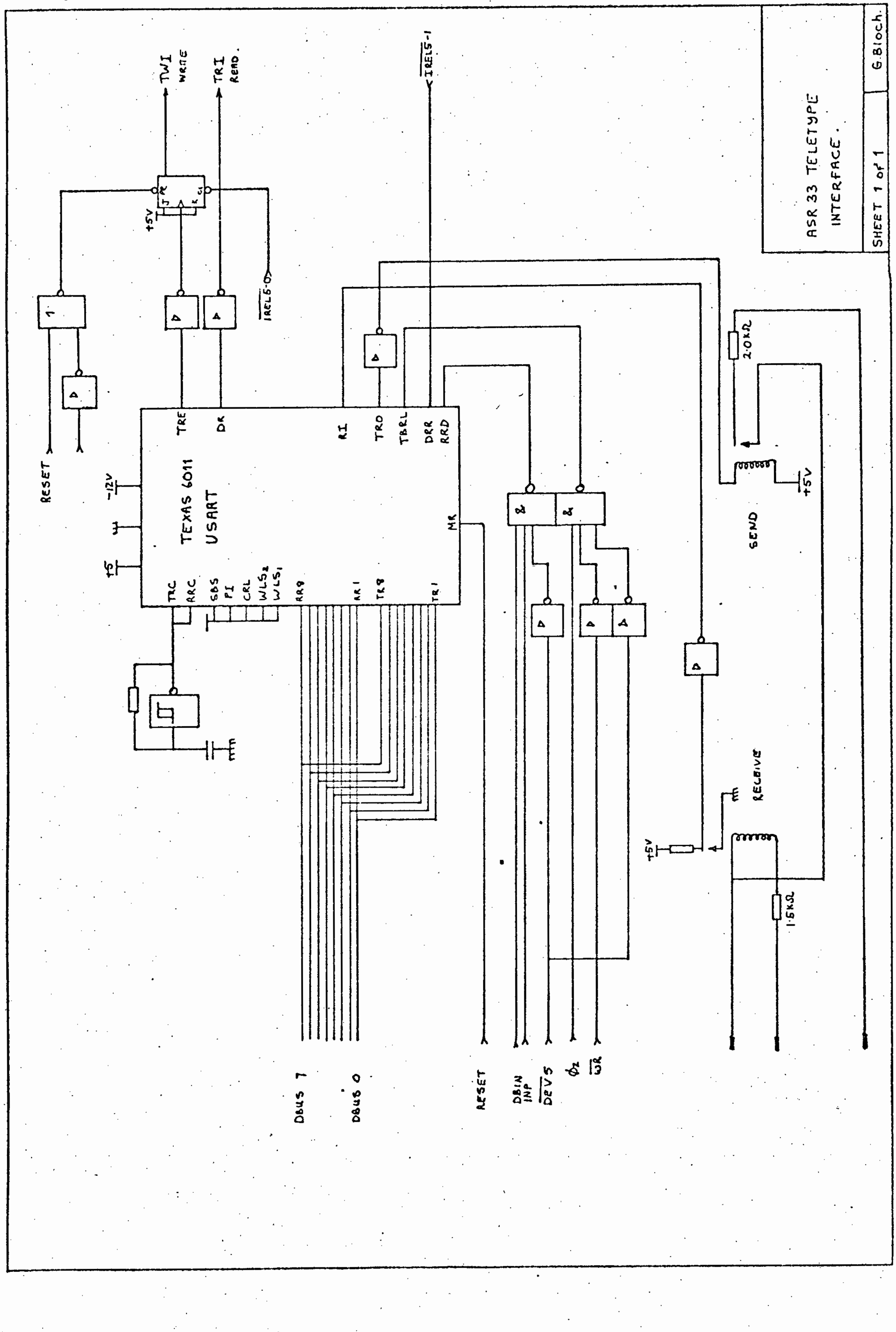

CPU MODULE
ADDRESS BUS BUFFERING
SHEET 4 of 4
G.Bloch.
ABUS0
ABUS15
DEC 0
DEC 15
DEV 0
DEV 31
74154
74154
74154
8212
8212
A0
A15
TRP
DMA-1
DMA-2
HLDA
DMA-3
HLTA
DEC0
INP
OUT
DEC1

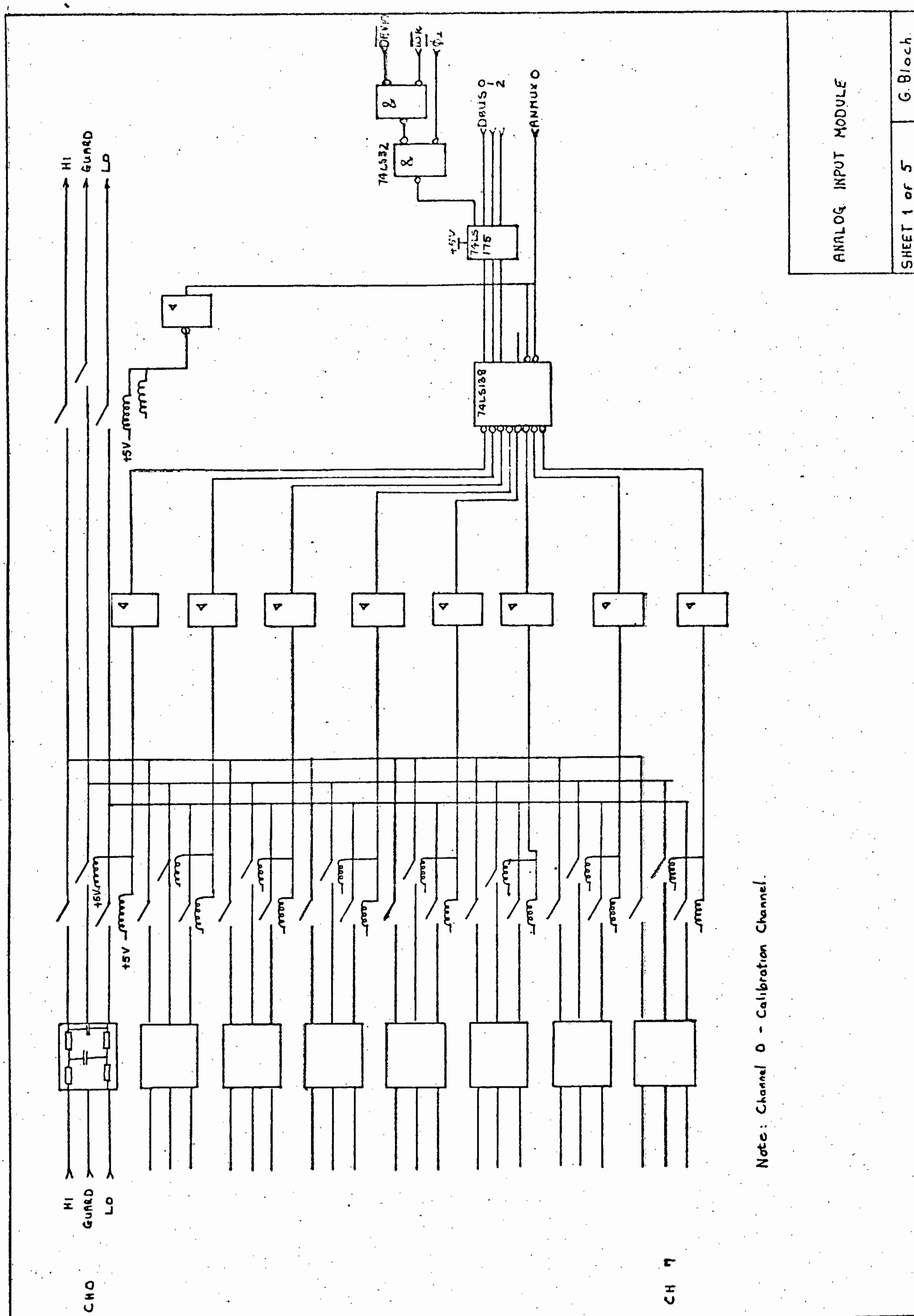

INTERRUPT CONTROL UNIT
G. Bloch
SHEET 1 OF 3
INT
IREL 0
IREL 7
DBUS 7
0
+5V
CL
DB2
8212
MD STB
74LS138
+5V
INTE
&
INTA
DBIN
74148
INTA
DBIN
+5V
5V UNREGU-LATED
74LS32
74LS175
CK
CL
+5V
IREL 7
0
7
DBUS
ALARM INTE-RRUPS.
ANALOG INPUT MODULES
SPARE
COMMUNICATION PERIPHERAL INT.
SPARE
SPARE
DEV 0
WR
RESET

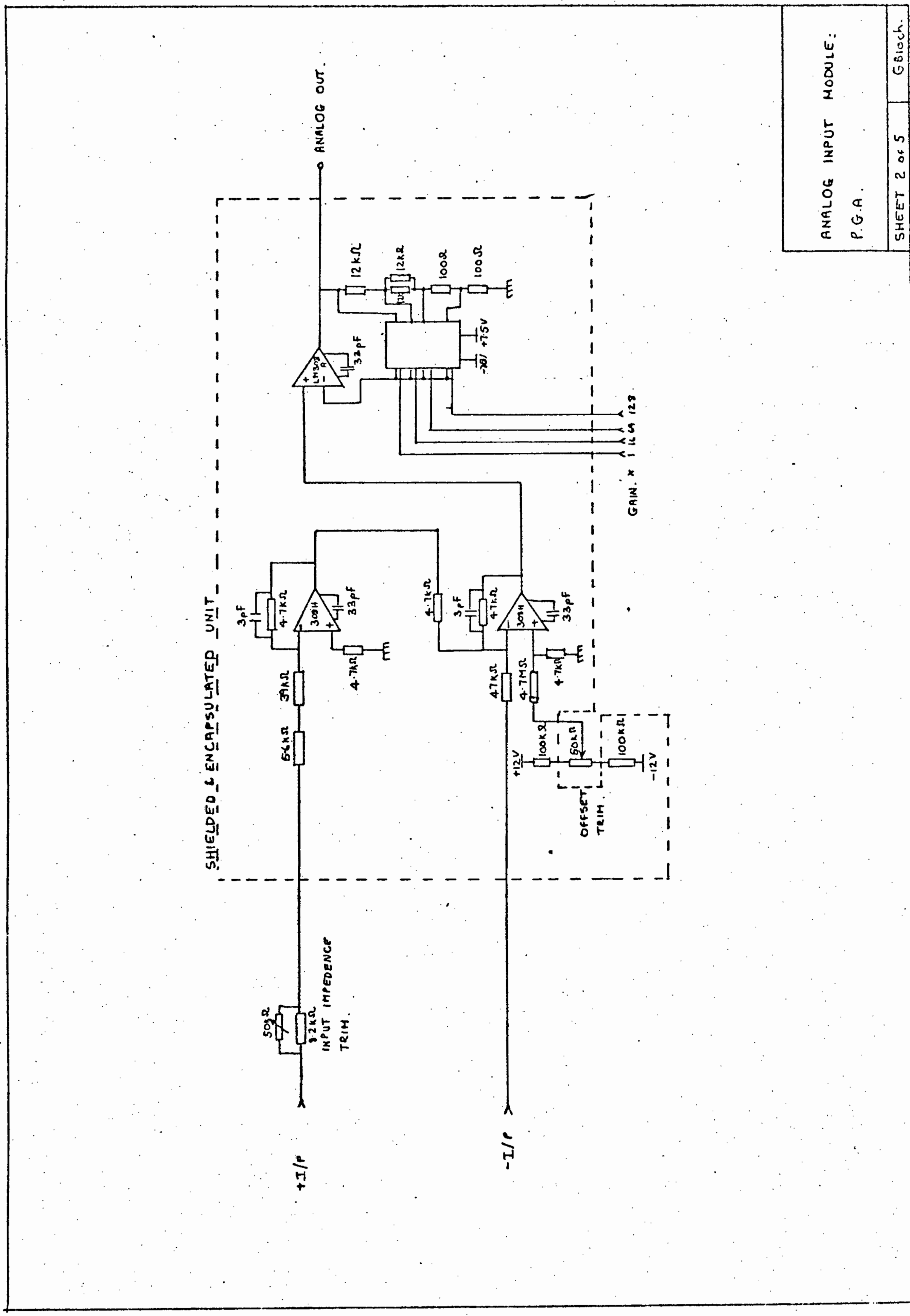

INTERRUPT CONTROL UNIT
G. Bloch.
SHEET 2 of 3
ALARM INT.
ANALOG INPUT
MODULE INT.
DBUS 0
7
8212
8212
74LS139
74LS138
74LS20
74148
74148
74LS32
+5V
+5V
DBIN
DEV 1
DEV 2
IREL 2
IREL 3

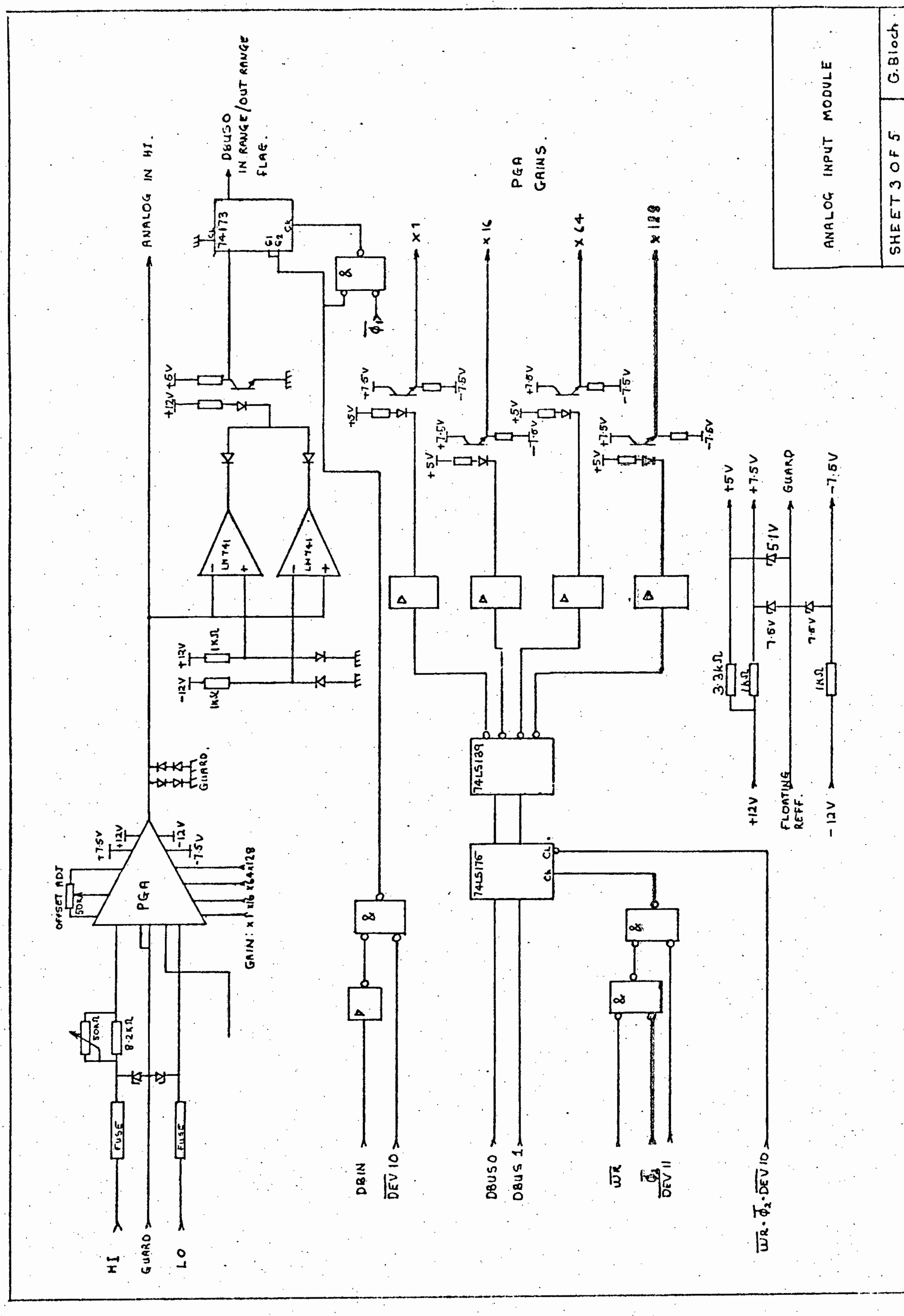

INTERRUPT CONTROL UNIT
G. Bloch.
SHEET 3 of 3
COMMUNICATION
PERIPHERAL INT.
DBUS
0
7
IREL5-0
IREL6-1
8212
DS1
STB
+5V
74LS138
IREL5
74LS22
&
74148
GS
DEV3
DBIN
TRI
TWI
INTE

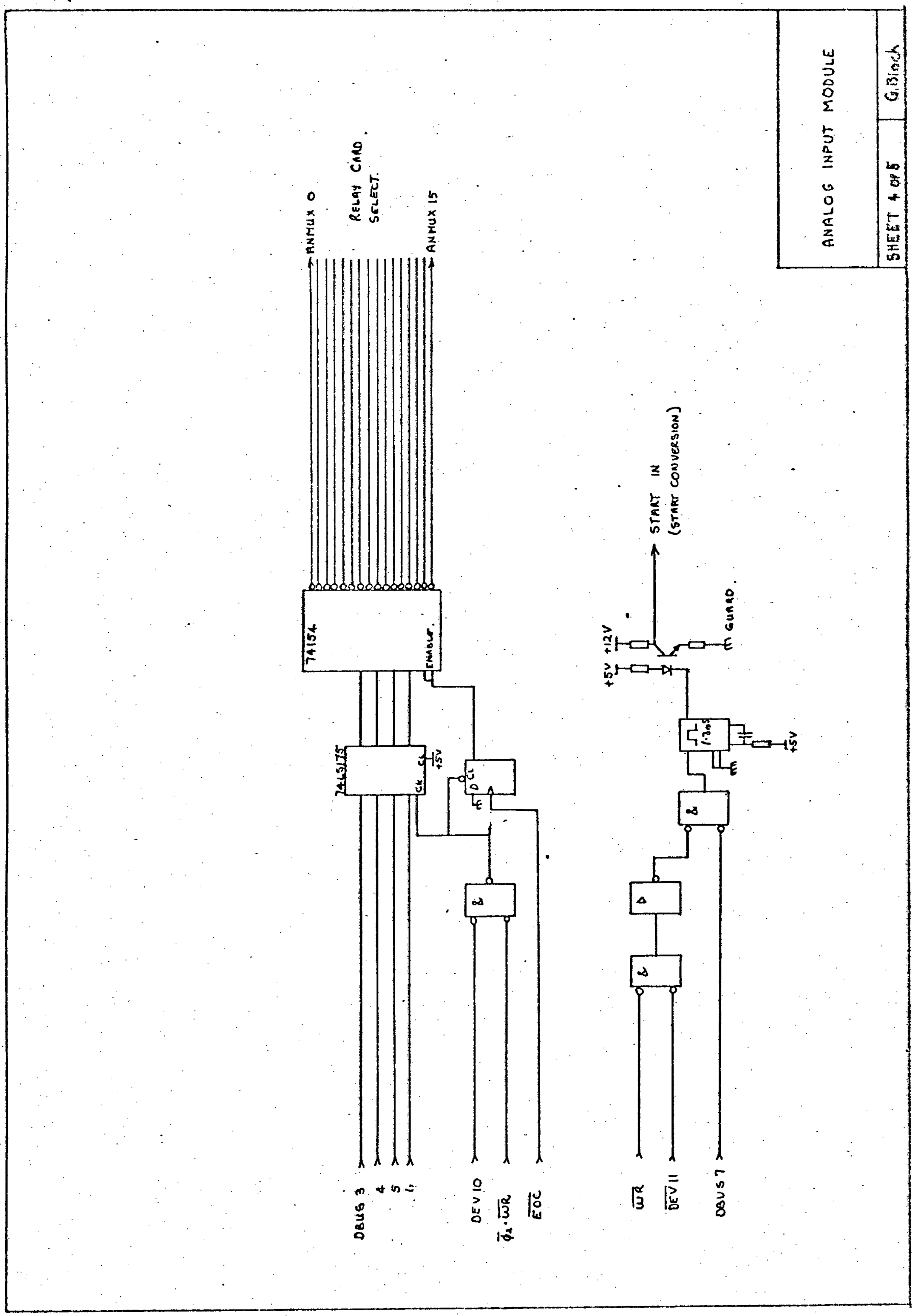

MEMORY INTERFACE
SHEET 1 OF 1
G. Bloch
4 k x 8 bit RAM.
INTEL 5101 L-8
74LS174
74LS00
74LS20
74-154
RDY-2
10kΩ
15kΩ
+5V
DBUS 0
DBUS 7
φ1
SYNC
INP
OUT WR
MEM WR
ABUS 0
ABUS 7
ABUS 8
ABUS 11
DEC 0
INTA
MEMR
DBIN
DMA-1
DBIN

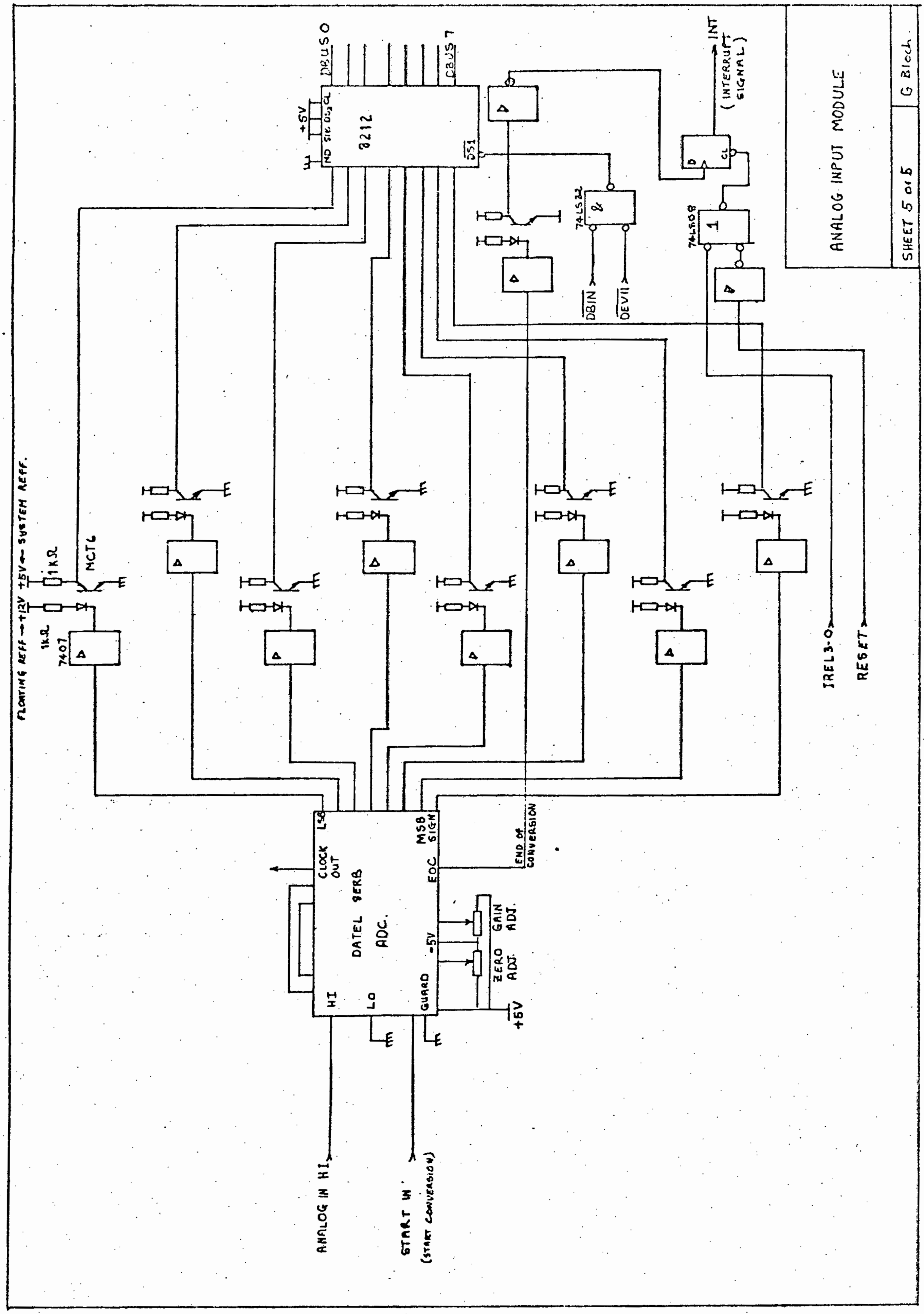

ASR 33 TELETYPE
INTERFACE.
G. Bloch.
SHEET 1 of 1
TEXAS 6011
USART
TWI
WRITE
TRI
READ
IREL5-1
IREL5-0
RESET
-12V
+5
TRE
DR
RI
TRO
TBRL
DRR
RRD
MR
TRC
RRC
SBS
PI
CRL
WLS2
WLS1
RR8
RR1
TR8
TR1
DBUS 7
DBUS 0
RESET
DBIN
INP
DEVS
φ2
WR
SEND
RECEIVE
2.0kΩ
1.5kΩ
+5V


ANALOG INPUT MODULE
SHEET 1 of 5
G. Bloch
74LS32
74LS175
74LS138
+5V
DBUS 0
1
2
KANMUX 0
HI
GUARD
LO
CH 0
CH 7
Note: Channel 0 - Calibration Channel.

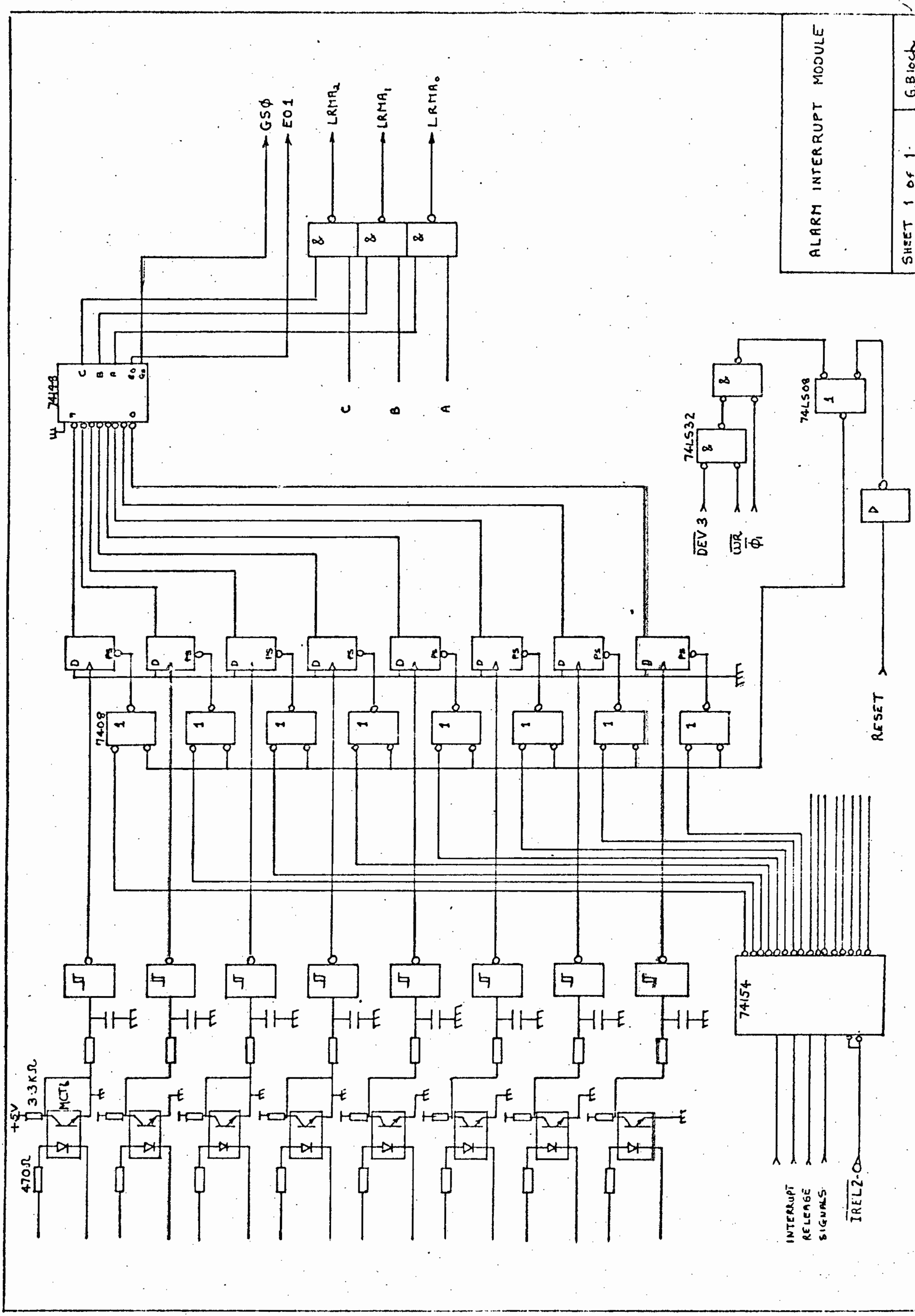

ANALOG INPUT MODULE:
P.G.A.
SHEET 2 of 5
G.Bloch.
ANALOG OUT.
SHIELDED & ENCAPSULATED UNIT
12kΩ
12kΩ
100Ω
100Ω
+7.5V
33pF
3pF
4.7kΩ
33pF
4.7kΩ
39kΩ
56kΩ
47kΩ
4.7MΩ
100kΩ
50kΩ
100kΩ
+12V
-12V
OFFSET TRIM.
INPUT IMPEDENCE TRIM.
+I/P
-I/P

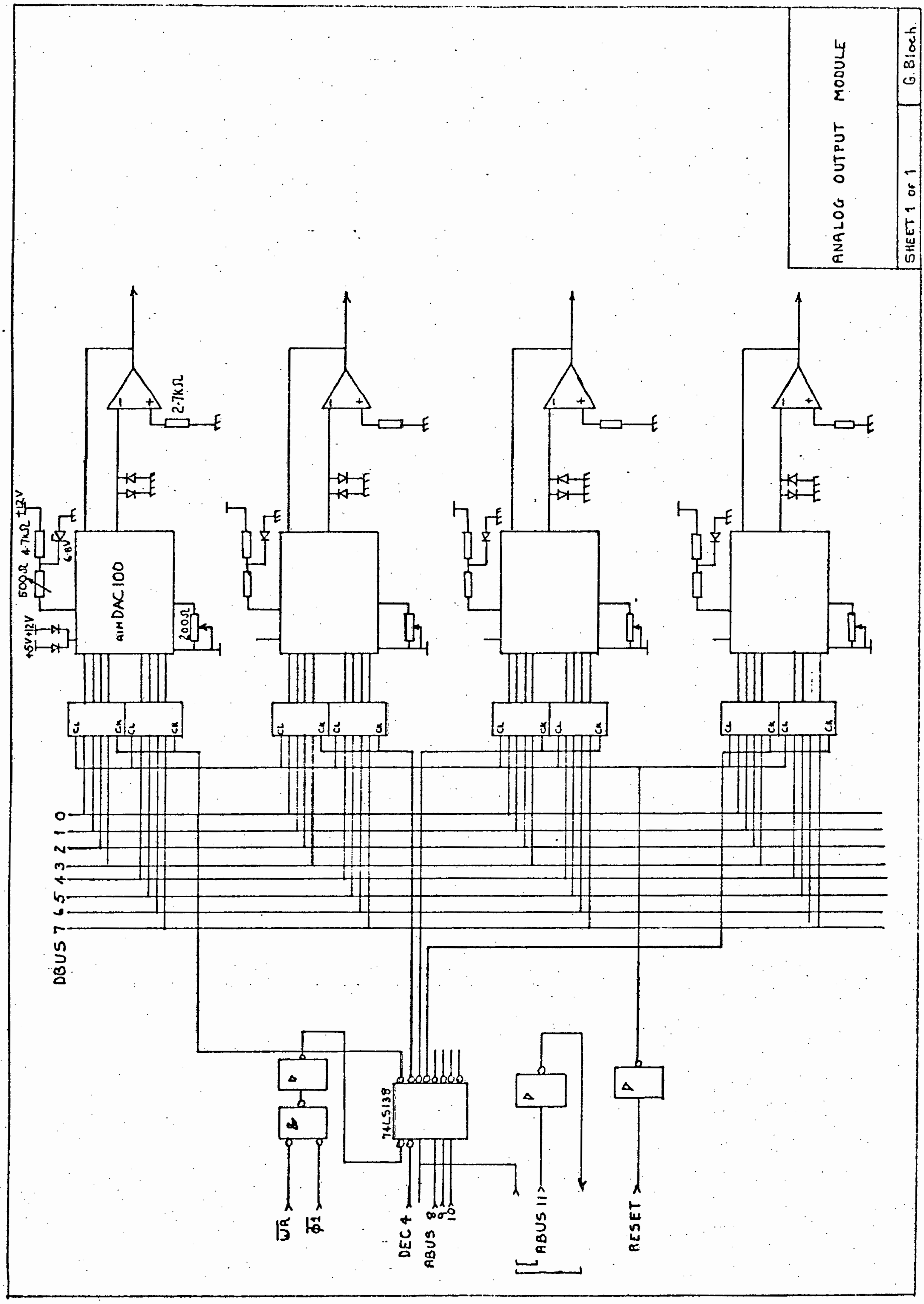

ANALOG INPUT MODULE
SHEET 3 OF 5
G.Bloch
DBUSO
IN RANGE/OUT RANGE FLAG.
ANALOG IN HI.
74173
PGA GAINS.
x 1
x 16
x 64
x 128
LM741
74LS139
74LS175
PGA
OFFSET ADJ
50kΩ
8.2kΩ
FUSE
GAIN: x1 x16 x64 x128
GUARD
HI
LO
DBIN
DEV 10
DBUS 0
DBUS 1
WR
DEV 11
WR·Φ2·DEV 10
+5V
+7.5V
-7.5V
+12V
-12V
5.1V
7.5V
3.3kΩ
1kΩ
FLOATING REFF.

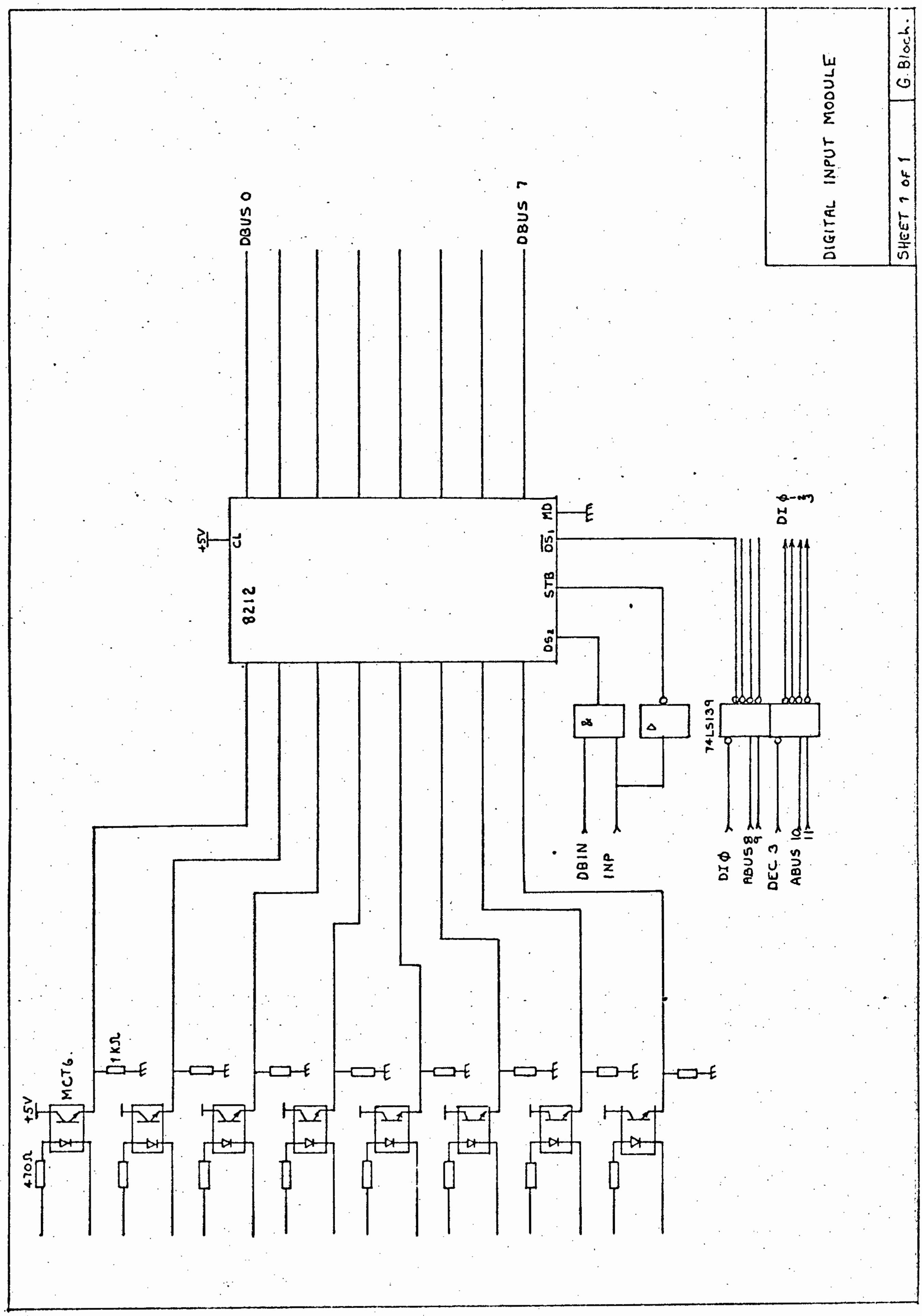

ANALOG INPUT MODULE
SHEET 4 OF 5
G.Bloch
ANMUX 0
RELAY CARD SELECT.
ANMUX 15
74154
ENABLE
74LS175
+5V
START IN
(START CONVERSION)
GUARD
+12V
+5V
DBUS 3
4
5
6
DEV 10
EOC
WR
DEV 11
DBUS 7

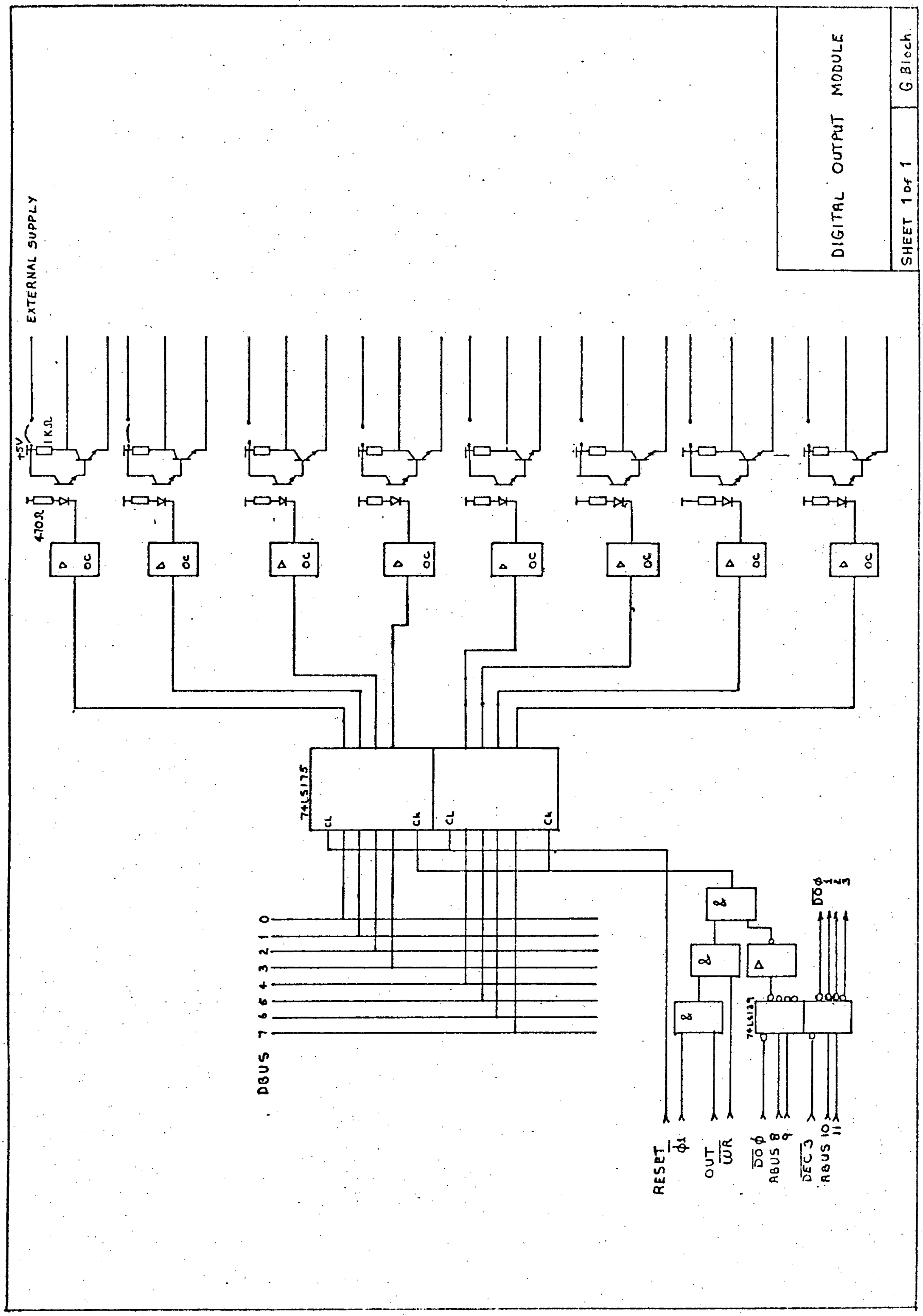


ANALOG INPUT MODULE
SHEET 5 of 5
G Bloch
8212
DBUS 0
DBUS 7
+5V
DS1
INT
(INTERRUPT SIGNAL)
D
CL
74LS32
74LS08
DBIN
DEVII
IREL3-0
RESET
FLOATING REFF → +12V +5V ← SYSTEM REFF.
1kΩ
1kΩ
MCT6
7407
DATEL 8ERB
ADC.
CLOCK OUT
LSB
MSB SIGN
EOC
END OF CONVERSION
GAIN ADJ.
ZERO ADJ.
-5V
+5V
HI
LO
GUARD
ANALOG IN HI
START IN
(START CONVERSION)


ALARM INTERRUPT MODULE
SHEET 1 of 1
G.Bloch
GSØ
EO1
LRMA2
LRMA1
LRMA0
74148
C
B
A
74LS32
74LS08
DEV 3
WR
Φ1
RESET
7408
74154
+5V
3.3KΩ
MCT6
470Ω
INTERRUPT RELEASE SIGNALS
IREL2


ANALOG OUTPUT MODULE
G. Bloch
SHEET 1 OF 1
AIM DAC 100
2·7kΩ
4·7kΩ
+12V
6·8V
500Ω
+5V +12V
200Ω
DBUS 7 6 5 4 3 2 1 0
74LS138
WR
Φ1
DEC 4
ABUS 8 9 10
ABUS 11
RESET

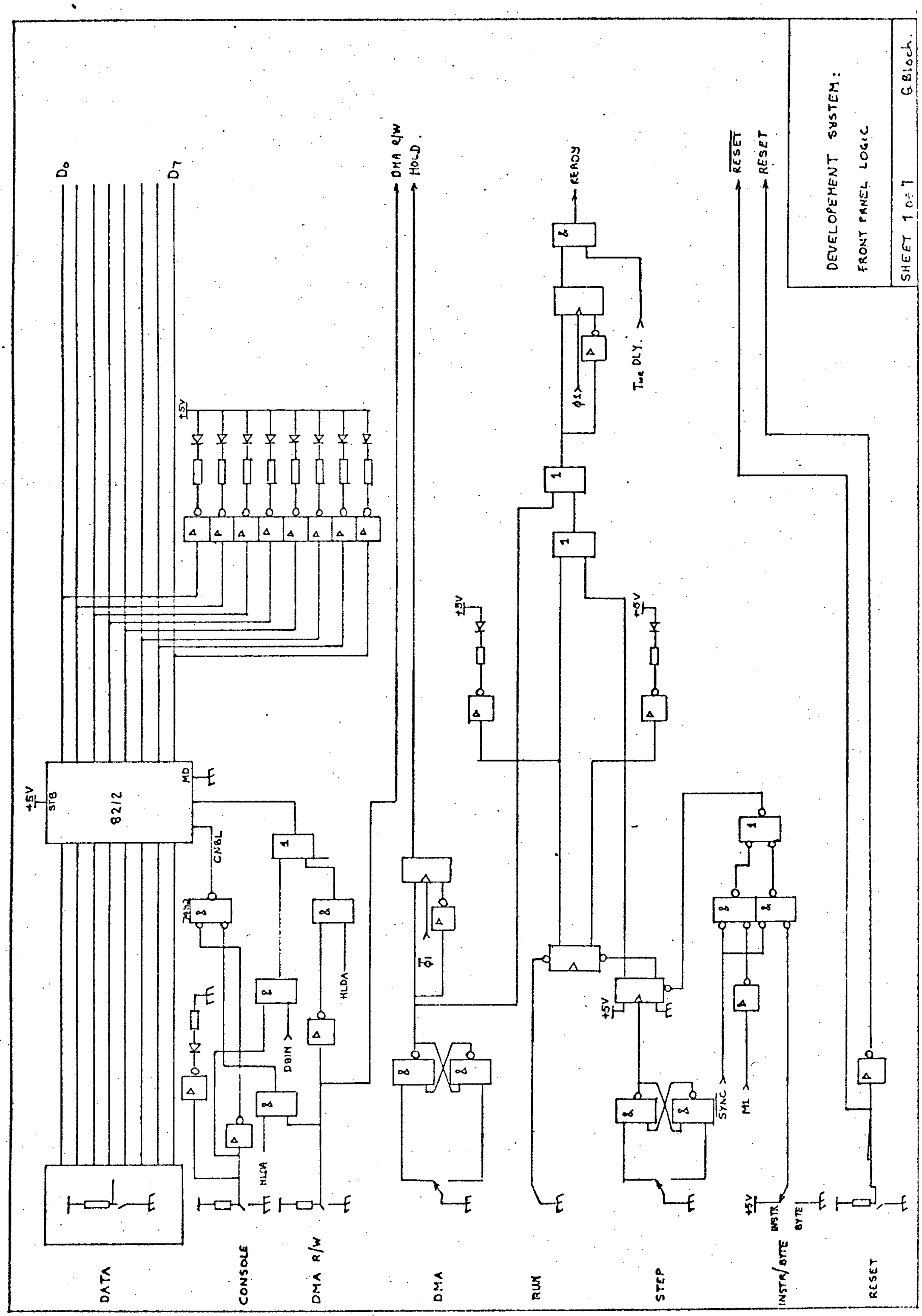

DIGITAL INPUT MODULE
SHEET 1 of 1
G. Bloch.
DBUS 0
DBUS 7
8212
+5V
CL
MD
DS1
STB
DS2
74LS139
DI Φ – 3
DBIN
INP
DI Φ
ABUS 8
9
DEC 3
ABUS 10
11
MCT6.
1KΩ
+5V
470Ω

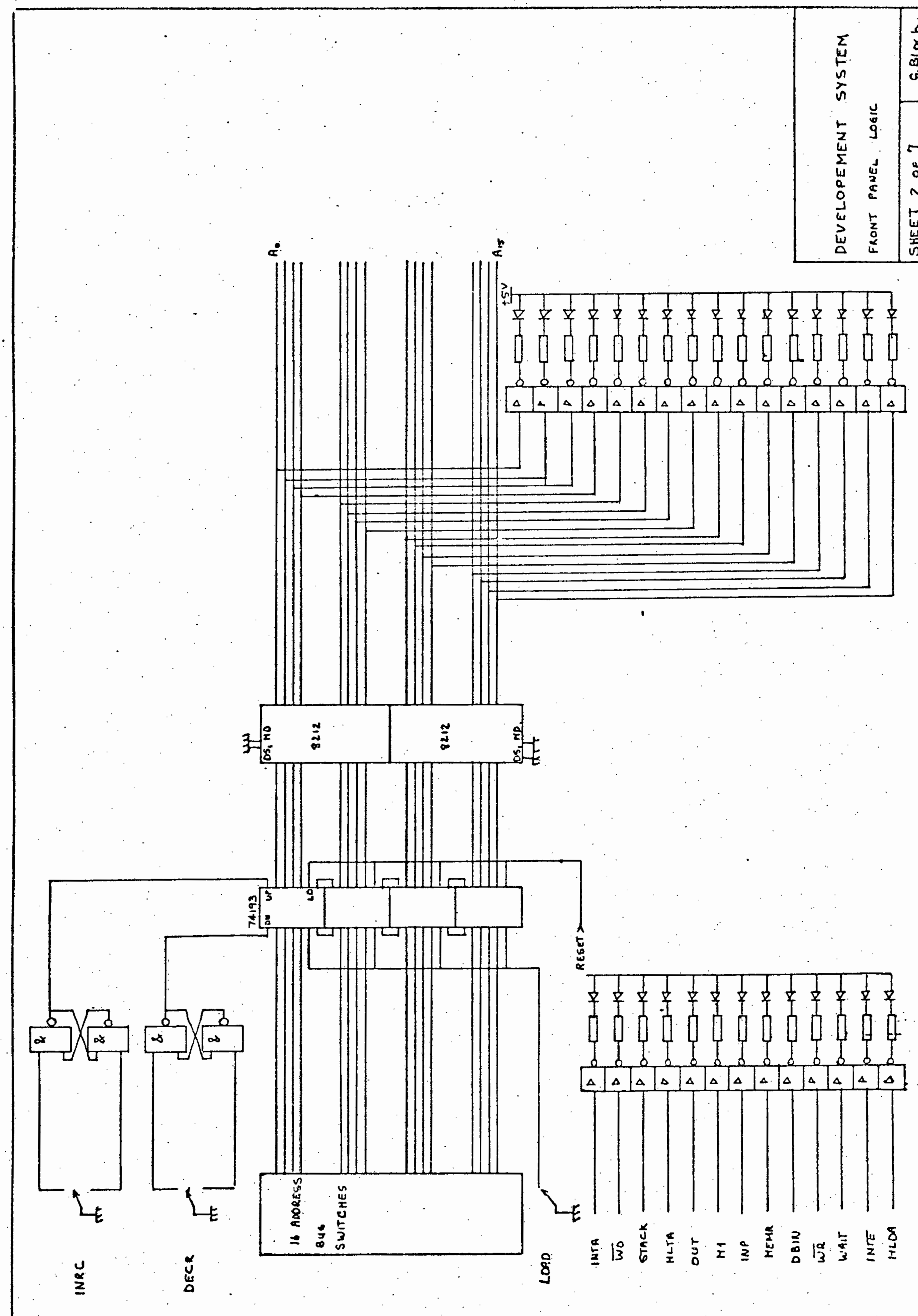

DIGITAL OUTPUT MODULE
SHEET 1 of 1
G. Bloch.
EXTERNAL SUPPLY
+5V
1KΩ
470Ω
D OC
74LS175
CL
Ck
DBUS
0
1
2
3
4
5
6
7
&
D
74LS139
RESET
φ1
OUT
WR
DO φ
ABUS 8
9
DEC 3
ABUS 10
11
DO φ
1
2
3

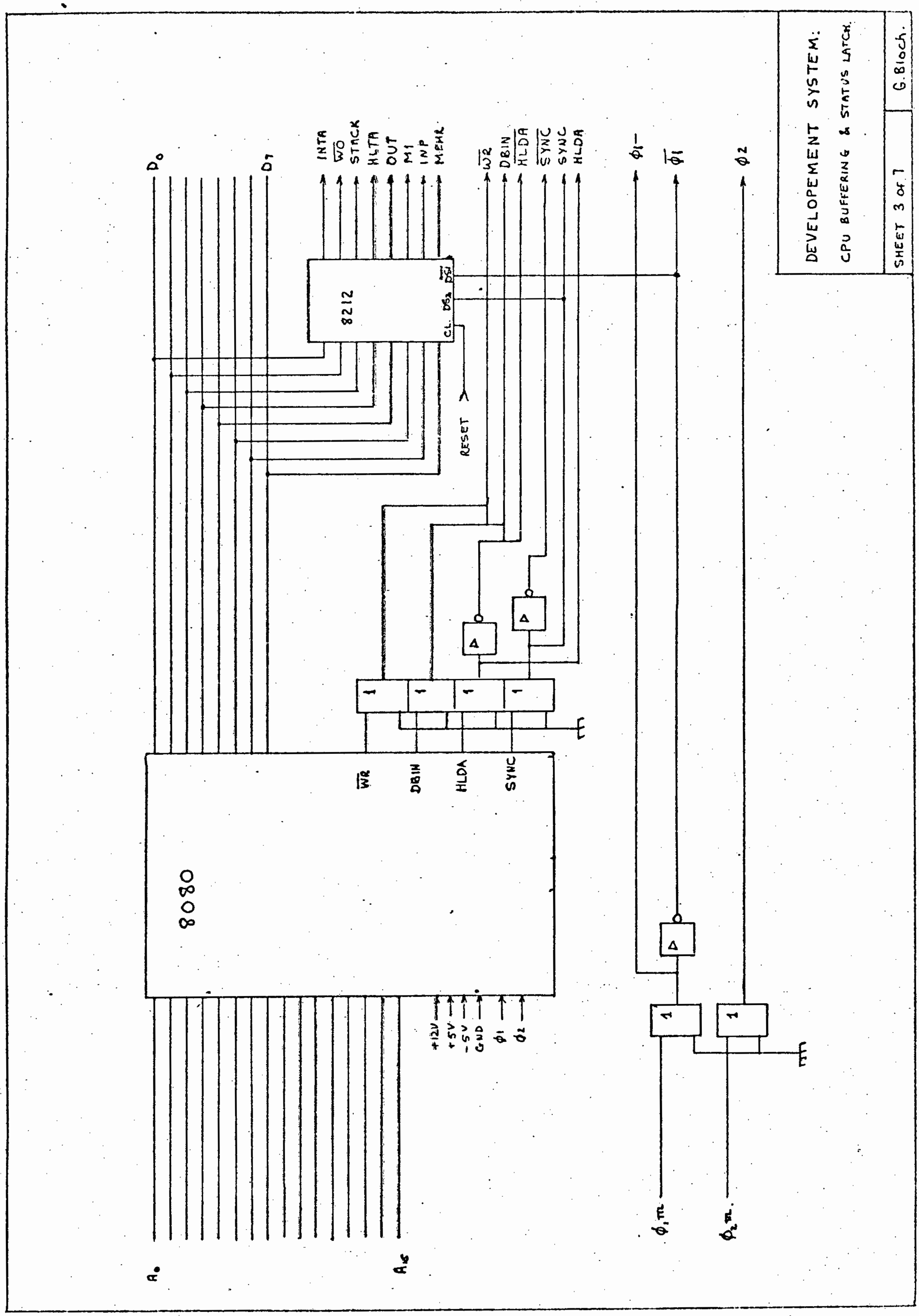
Appendix F (ii)

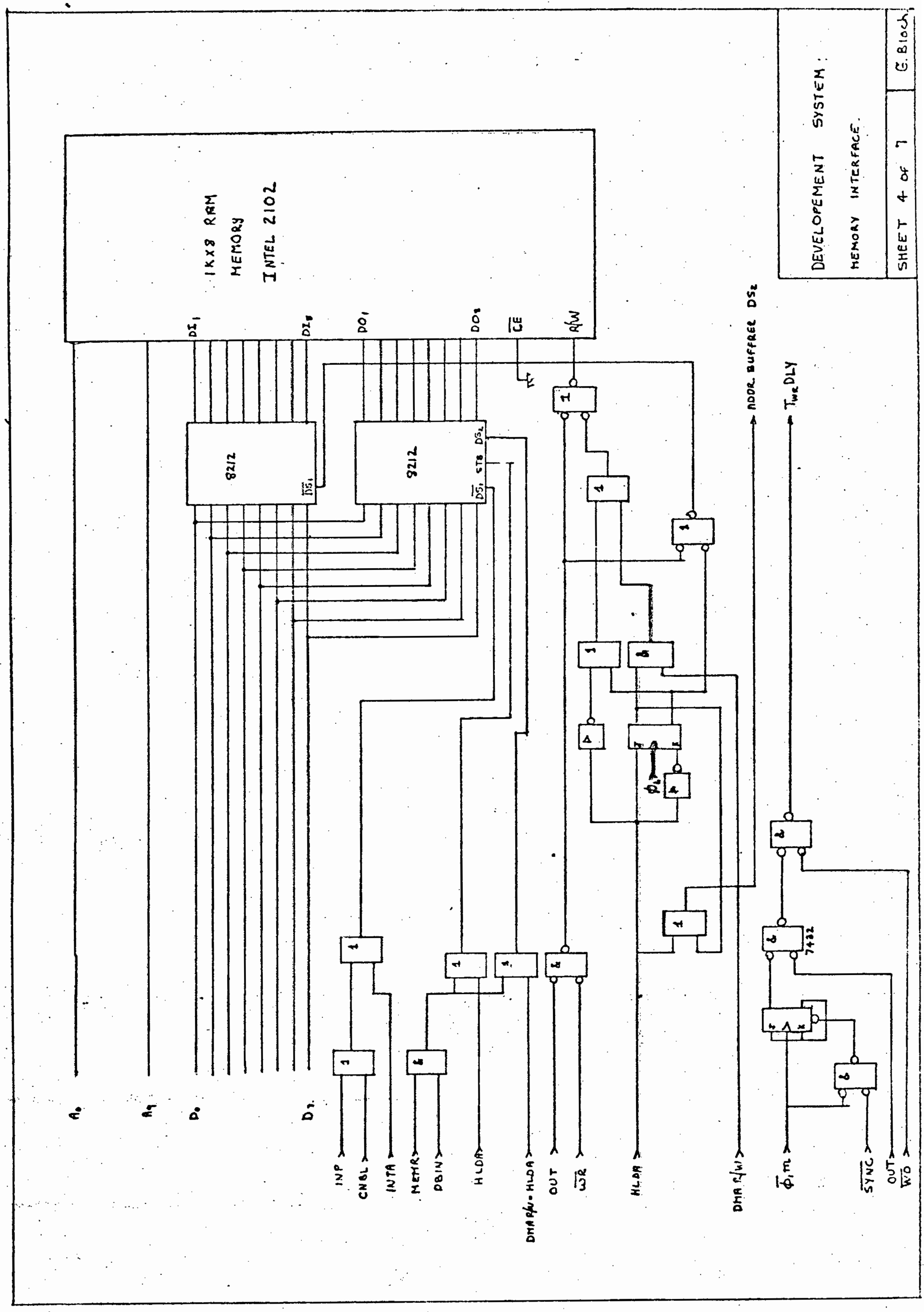
DEVELOPMENT SYSTEM

- LOGIC DRAWINGS.


DEVELOPEMENT SYSTEM:
FRONT PANEL LOGIC
SHEET 1 of 7
G. Bloch.
D_0
D_7
DMA R/W
HOLD
READY
T_W DLY.
$\phi 1$
$\overline{RESET}$
RESET
+5V
8212
STB
MD
CNBL
HLDA
DBIN
$\overline{\phi 1}$
SYNC
M1
INSTR
BYTE
DATA
CONSOLE
DMA R/W
DMA
RUN
STEP
INSTR/BYTE
RESET


DEVELOPEMENT SYSTEM
FRONT PANEL LOGIC
SHEET 2 OF 7
G. Bloch.
A0
A15
+5V
8212
8212
DS, MD
DS, MD
74193
UP
DN
LD
RESET
16 ADDRESS BUS SWITCHES
INRC
DECR
LOAD
INTA
WO
STACK
HLTA
OUT
M1
INP
MEMR
DBIN
WR
WAIT
INTE
HLDA


DEVELOPEMENT SYSTEM:
CPU BUFFERING & STATUS LATCH.
SHEET 3 OF 7
G. Bloch.
8080
8212
D0
D7
A0
A15
INTA
WO
STACK
HLTA
OUT
M1
INP
MEMR
WR
DBIN
HLDA
SYNC
SYNC
HLDA
DS1
DS2
CL.
RESET
φ1
φ1
φ2
+12V
+5V
-5V
GND
φ1
φ2
φ1 TTL
φ2 TTL

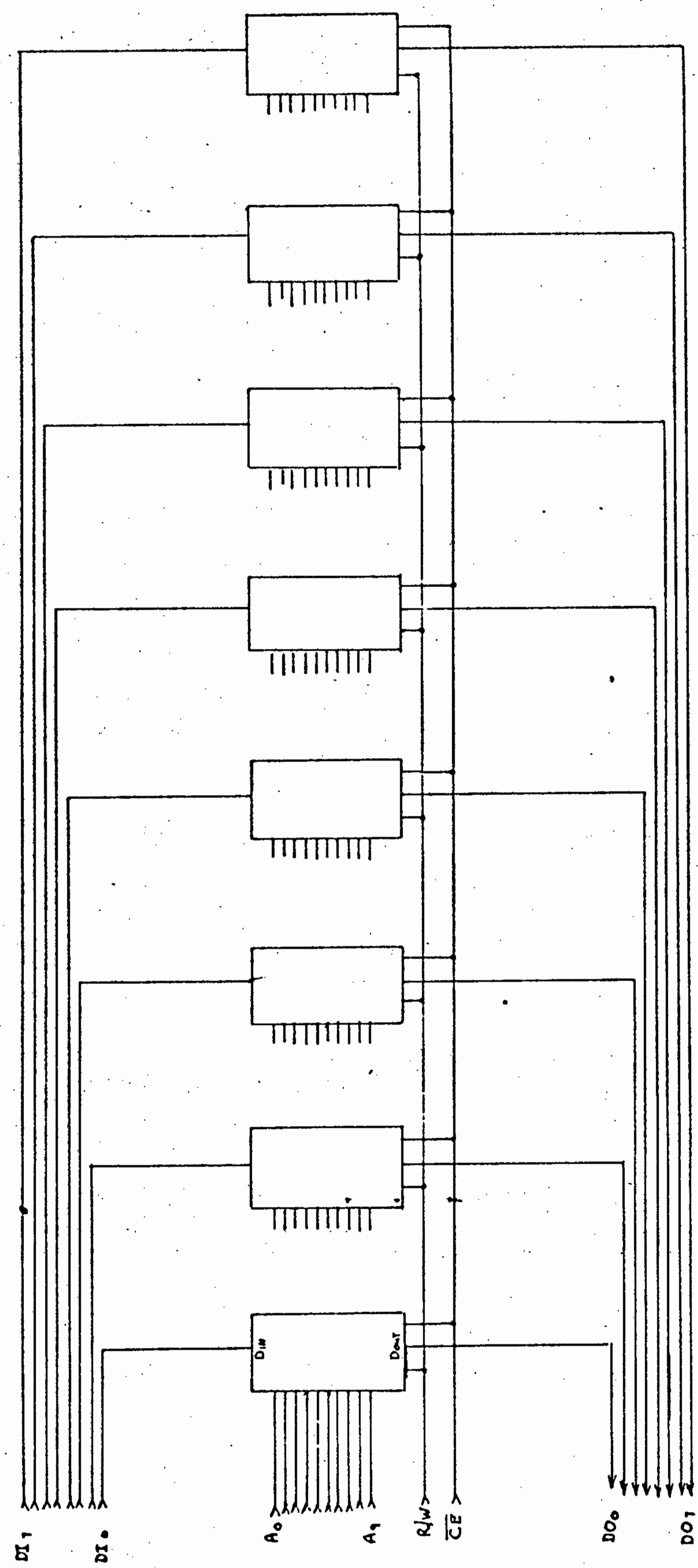

DEVELOPEMENT SYSTEM :
MEMORY INTERFACE.
SHEET 4 OF 7
G. Bloch
1KX8 RAM
MEMORY
INTEL 2102
DI1
DI8
DO1
DO8
CE
R/W
8212
8212
DS1
DS2
STB
ADDR. BUFFREE DS2
TWR DLY
7432
A0
A9
D0
D7
INP
CNBL
INTA
MEMR
DBIN
HLDA
DMAR/W·HLDA
OUT
WR
HLDA
DMA r/w
Φ1 TTL
SYNC
OUT WO

DEVELOPEMENT SYSTEM

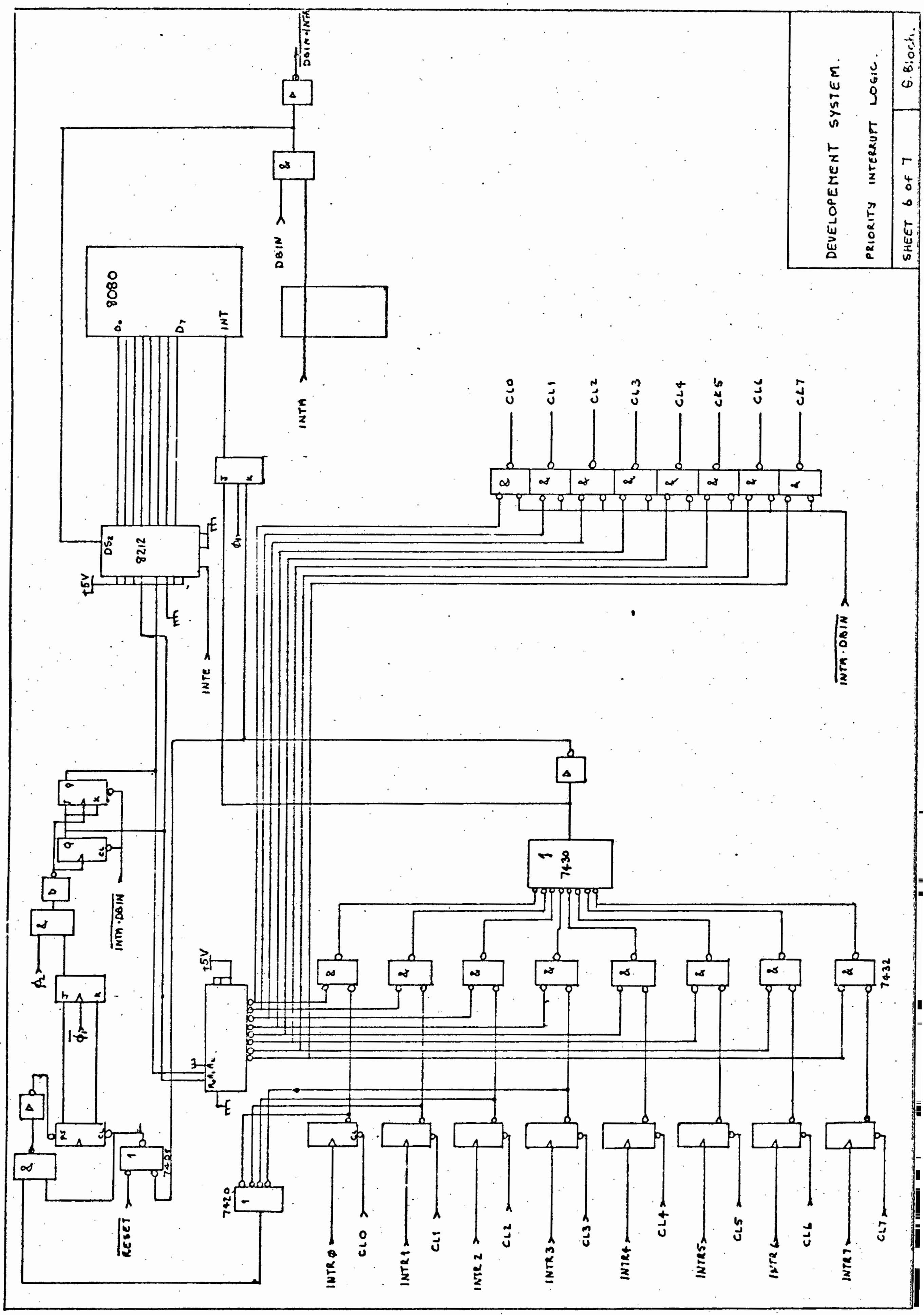
MEMORY CHIP INTERCONNECTION.

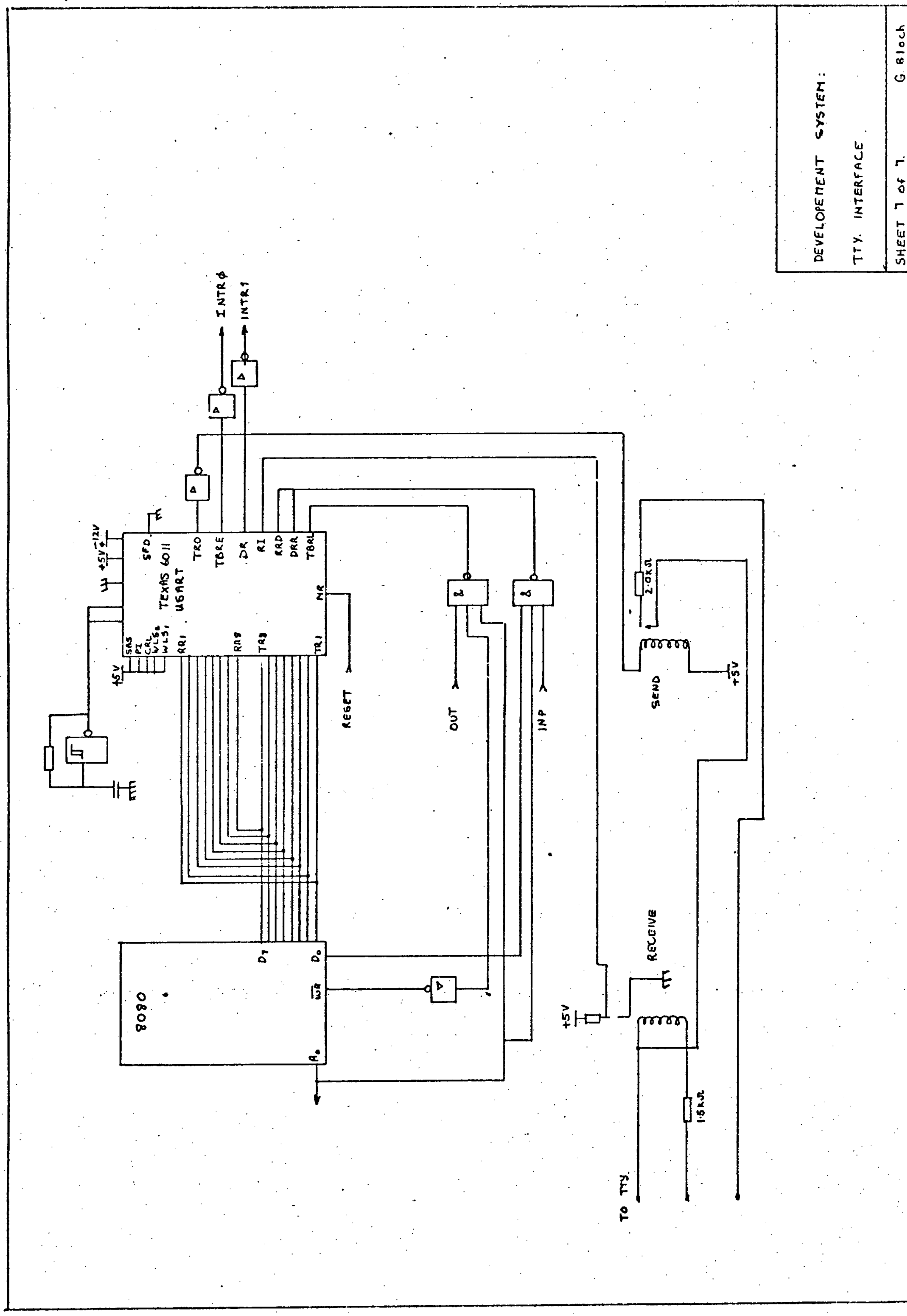
SHEET 5 of 7

G. Bloch.



Note: All A_i ($i = 0-9$) common


DEVELOPEMENT SYSTEM.
PRIORITY INTERRUPT LOGIC.
SHEET 6 of 7
G. Bioch.
8080
INT
8212
+5V
INTE
INTA
DBIN
INTA · DBIN
7430
7432
7420
RESET
INTR 0
INTR 1
INTR 2
INTR 3
INTR 4
INTR 5
INTR 6
INTR 7
CL0
CL1
CL2
CL3
CL4
CL5
CL6
CL7


DEVELOPEMENT SYSTEM:
TTY. INTERFACE
SHEET 7 of 7.
G. Bloch
TEXAS 6011
UART
SFD
TRO
TBRE
DR
RI
RRD
DRR
TBRL
MR
RR1
RR8
TR8
TR1
+5V
-12V
INTR0
INTR1
RESET
OUT
INP
8080
D7
D0
WR
A0
2.0kΩ
SEND
RECEIVE
1.5kΩ
TO TTY

APPENDIX G.

(i)

Schottky Bipolar 8212

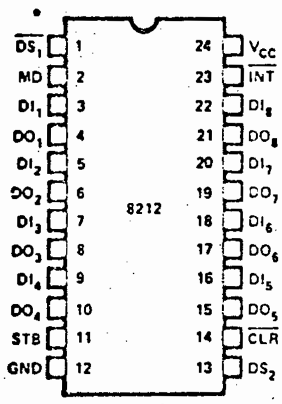
EIGHT-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Micro-computer Systems
- Reduces System Package Count

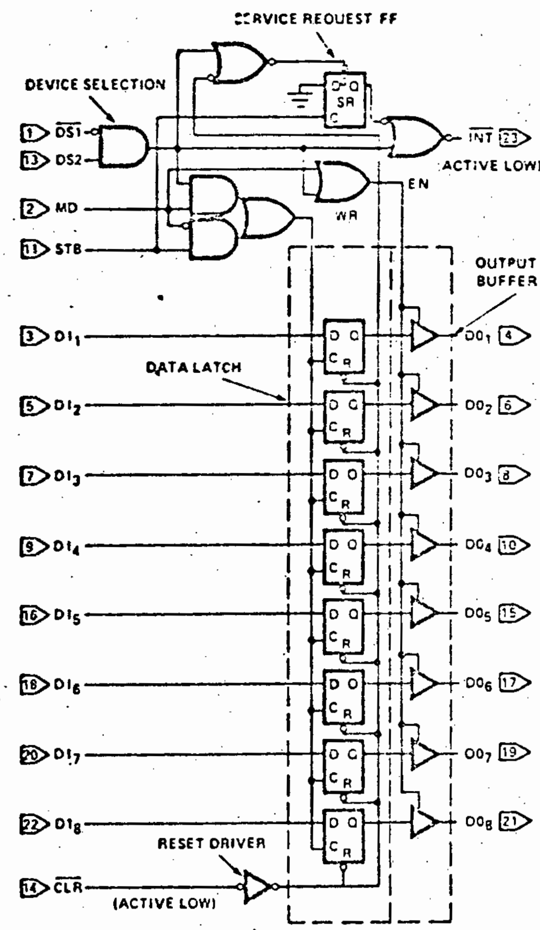
The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

SCHOTTKY BIPOLAR 8212

Functional Description

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN): this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

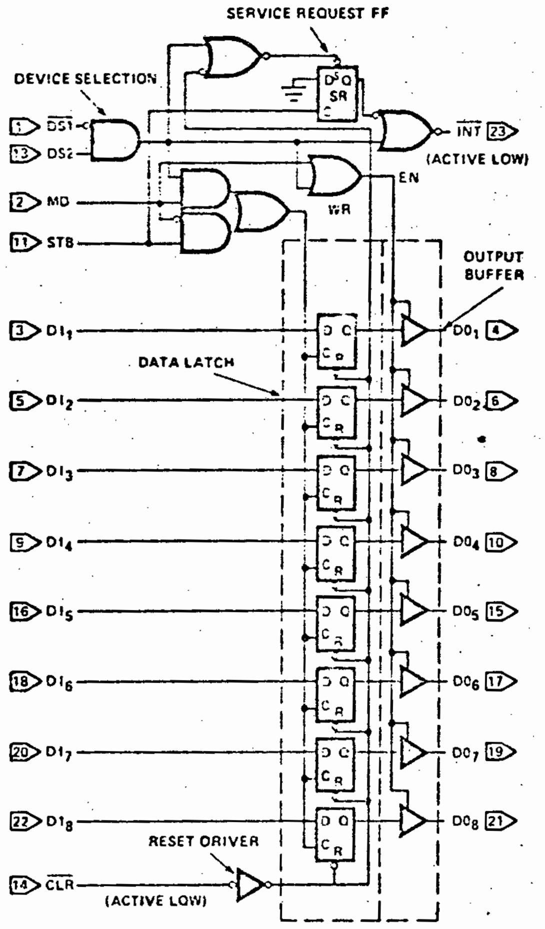
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	3 STATE
1	0	0	3 STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

CLR	$(\overline{DS_1} \cdot DS_2)$	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP-FLOP

Appendix G (ii)

intel® Silicon Gate CMOS 5101, 5101-3, 5101L, 5101L-3

1024 BIT (256 x 4) STATIC CMOS RAM

*Ultra Low Standby Current: 15 nA/Bit for the 5101

- Fast Access Time — 650 ns
- Single +5 V Power Supply
- Directly TTL Compatible — All Inputs and Outputs
- Three-State Output

The Intel® 5101 and 5101-3 are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. Minimum standby current is drawn by these devices when CE_2 is at a low level. When deselected the 5101 and 5101-3 draw from the single 5 volt supply only 15 microamps and 200 microamps, respectively. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 and 5101-3 use fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 and 5101-3 have separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

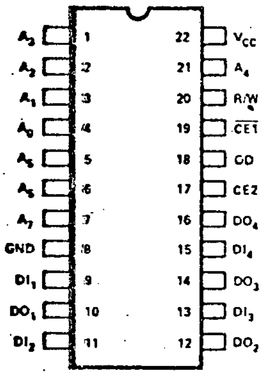
The 5101L and 5101L-3 are identical to the 5101 and 5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

A pin compatible N-channel static RAM, the Intel 2101, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.

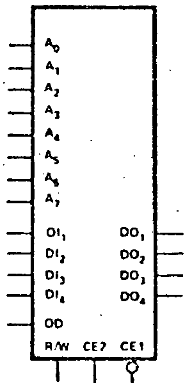
PIN CONFIGURATION

5101



LOGIC SYMBOL

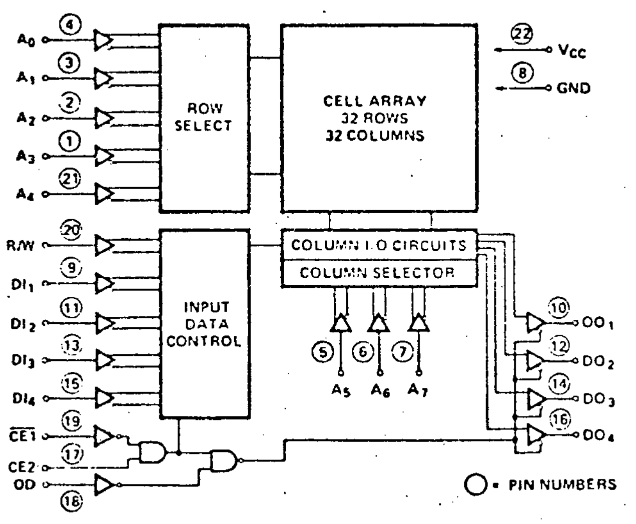
5101



PIN NAMES

$DI_1 - DI_4$	DATA INPUT	OD	OUTPUT DISABLE
$A_0 - A_7$	ADDRESS INPUTS	$DO_1 - DO_4$	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



2

SILICON GATE CMOS 5101, 5101-3, 5101L, 5101L-3

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . +7.0V
Power Dissipation . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for 5101, 5101-3, 5101L, 5101L-3

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

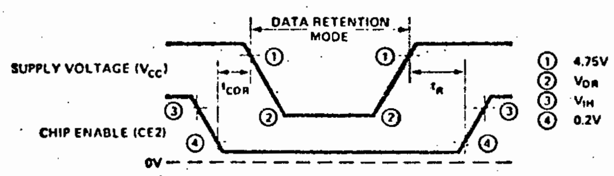
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		5		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		9	22	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤ 0.01 Outputs Open
I_{CC2}	Operating Current		13	27	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤ 0.01 Outputs Open
5101 I_{CCL}[2]	Standby Current		0.2	15	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
5101-3 I_{CCL}[2]	Standby Current		1	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = 1.0mA

Low V_{CC} Data Retention Characteristics (For 5101L and 5101L-3) T_A = 0°C to 70°C

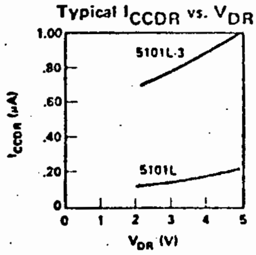
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	
5101L I_{CCDR}	Data Retention Current		0.14		μA		V_{DR} = 2.0V
5101L-3 I_{CCDR}	Data Retention Current		0.70		μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL} measurement. 3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveforms



Typical I_{CCDR} vs. V_{DR}



SILICON GATE CMOS 5101, 5101-3, 5101L, 5101L-3

A.C. Characteristics for 5101, 5101-3, 5101L, 5101L-3

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	(See below)
t_A	Access Time			650	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			600	ns	
t_{CO2}	Chip Enable (CE2) to Output			700	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

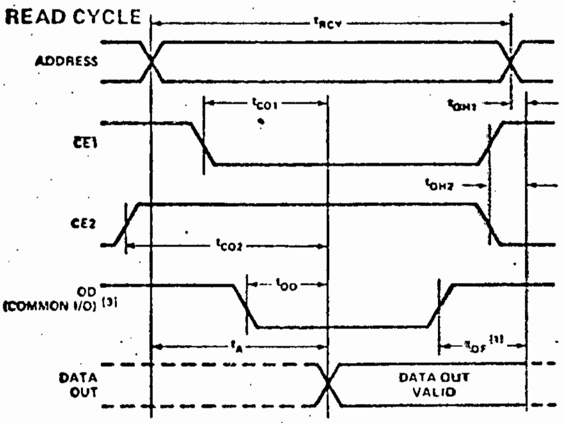
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] $T_A = 25°C$, f = 1MHz

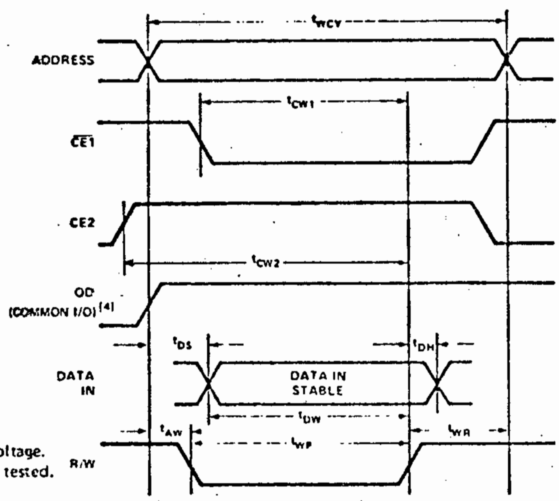
Symbol	Test	Limits (pF) Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Appendix G (iii)

Monsanto

DUAL PHOTOTRANSISTOR OPTO-ISOLATOR

MCT6

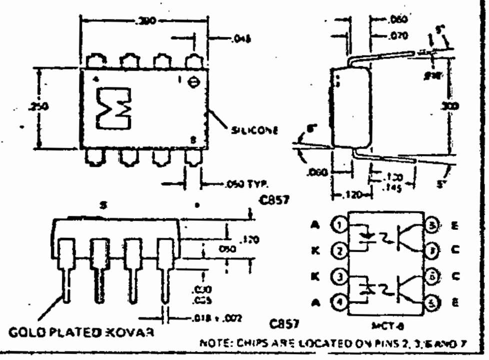
PRODUCT DESCRIPTION

The MCT6 opto-isolator has two channels for high density applications. For four channel applications, two-packages fit into a standard 16-pin DIP socket.

At the input, a GaAsLITE emitting diode generates infrared light proportional to current passing through the diode in the forward direction. At the output, a silicon phototransistor detects and amplifies the photocurrent generated in its photosensitive base region. Light coupling electrically isolates the input from the output.

PACKAGE DIMENSIONS

ALL DIMENSIONS IN INCHES



FEATURES

- Two isolated channels per package
- Two packages fit into a 16 lead DIP socket
- Same basic electrical characteristics as MCT2
- 1500 volt isolation
- 50% typical current transfer ratio

APPLICATIONS

- AC Line/Digital Logic . . . . Isolate high voltage transients
- Digital Logic/Digital Logic . . . . Eliminate spurious grounds
- Digital Logic/AC Triac Control . . . . Isolate high voltage transients
- Twisted pair line receiver. . . . . Eliminate ground loop feedthrough
- Telephone/Telegraph line receiver. . . Isolate high voltage transients
- High Frequency Power Supply Feedback Control. . . . . Maintain floating ground
- Relay contact monitor . . . . Isolate floating grounds and transients
- Power Supply Monitor . . . . Isolate transients

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -55°C to 150°C
Operating Temperature -55°C to 100°C
Lead Temperature (soldering, 10 sec.) 250°C

INPUT DIODE (each channel)

Rated forward current, DC	60 mA
Peak reverse current	10 µA
Peak forward current (1µs pulse, 300 pps)	3 A
Power dissipation at 25°C ambient	100 mW
Derate linearly from 50°C	2 mW/°C

OUTPUT TRANSISTOR (each channel)

Power dissipation @ 25°C ambient	150 mW
Derate linearly from 25°C	2 mW/°C
Collector Current	30 mA

COUPLED

Input to output breakdown voltage	1500 volts DC
Total package power dissipation @ 25°C ambient	400 mW
Derate linearly from 25°C	5.33 mW/°C

ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
INPUT DIODE					
Threshold forward voltage		0.7		V	$\Delta I_C = 1$ nA
Rated forward voltage		1.25	1.50	V	$I_F = 60$ mA
Reverse voltage	3.0	5		V	$I_R = 10$ µA
Reverse current		.001	10	µA	$V_R = 3.0$ V
Junction capacitance		100		pF	$V_F = 0$ V
		300		pF	$V_F = 1$ V
Rise time, fall time		10		ns	$I_F = 50$ mA, 50Ω system
OUTPUT TRANSISTOR ($I_F = 0$)					
Breakdown voltage, collector to emitter	30	65		V	$I_C = 1.0$ mA
Breakdown voltage, emitter to collector	6	13		V	$I_C = 100$ µA
Leakage current, collector to emitter		1	100	nA	$V_{CE} = 10$ V
Capacitance collector to emitter		8		pF	$V_{CE} = 0$ V
COUPLED					
DC current transfer ratio (I_C/I_F)	20	50		%	$V_{CE} = 10$ V, $I_F = 10$ mA
Isolation voltage	1500	2500		V	
Isolation resistance	10^{11}	10^{12}		Ω	$V_{I-O} = 500$ V
Isolation capacitance		0.5		pF	f = 1 MHz
Breakdown voltage — channel-to-channel		1500		V	Relative humidity = 40%
Capacitance between channels		0.4		pF	f = 1 MHz
Saturation voltage — collector to emitter			.40	V	$I_C = 2$ mA, $I_F = 16$ mA
Bandwidth		150		KHz	$I_C = 2$ mA, $V_{CC} = 10$ V, $R_L = 100\ \Omega$

ELECTRO-OPTICAL CHARACTERISTICS (Con't)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
SWITCHING TIMES, OUTPUT TRANSISTOR					
Non-saturated rise time, fall time		2.4		μs	I_C = 2 mA, V_{CE} = 10 V, R_L = 100Ω
Non-saturated rise time, fall time		15		μs	I_C = 2 mA, V_{CE} = 10 V, R_L = 1 KΩ
Saturated turn-on time (from 5.0 V to 0.8 V)		5		μs	R_L = 2 KΩ, I_F = 15 mA
Saturated turn-off time (from saturation to 2.0 V)		25		μs	R_L = 2 KΩ, I_F = 15 mA

TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES (25°C Free Air Temperature Unless Otherwise Specified)

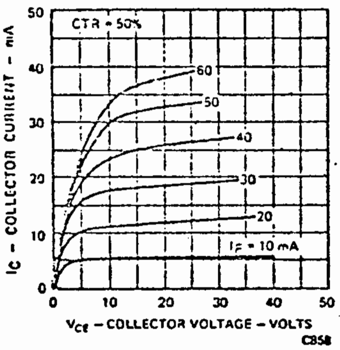


Figure 1 I-V Curve of Phototransistor

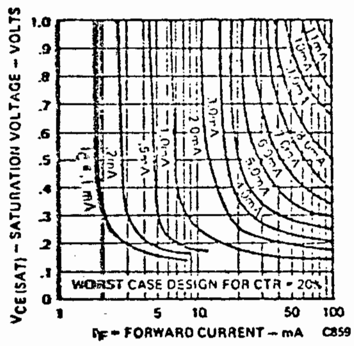


Figure 2 I-V Curve in Saturation

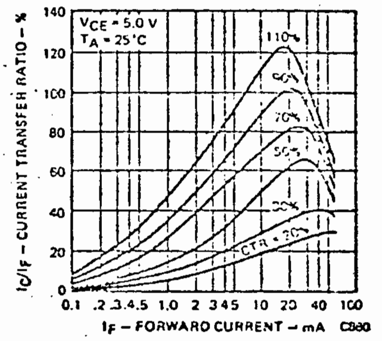


Figure 3 CTR vs. Forward Current

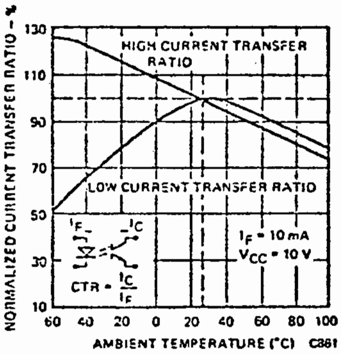


Figure 4 Current Transfer Ratio vs. Temperature

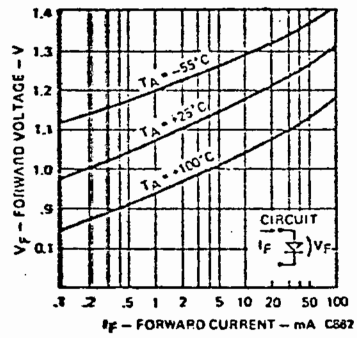


Figure 5 I-V Curve of LED vs. Temperature

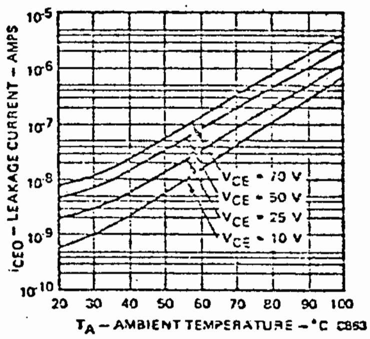


Figure 6 Leakage Current vs. Temperature vs. Collector Voltage

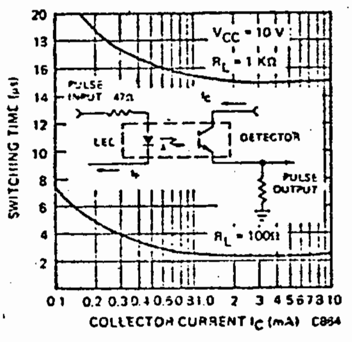


Figure 7 Switching Time vs. Collector Current

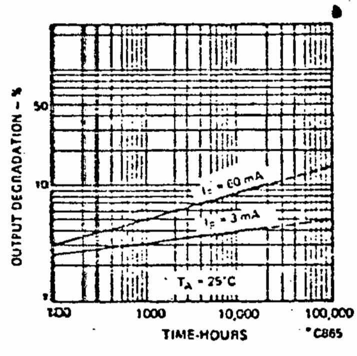


Figure 8 Lifetime vs. Forward Current (Note 1)

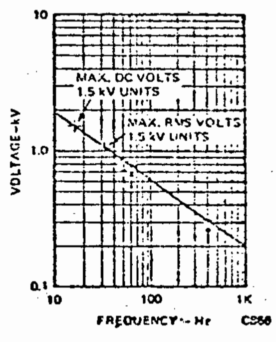


Fig. 9. Steady-State AC Voltage Limit of Isolation Dielectric

NOTES

1. Normalized CTR degradation = $\frac{CTR_o - CTR}{CTR_o}$

2. For more applications detail, see Application Notes Handbook.

Appendix G (iv)

DATEL SYSTEMS, INC.

RATIOMETRIC DUAL SLOPE ANALOG TO DIGITAL CONVERTERS

ADC-ER SERIES

FEATURES

- 4 Wire Ratiometric Operation
- Single +5V Power Requirement
- Differential Inputs
- 40 dB Normal Mode Noise Rejection
- 70 dB Common Mode Rejection
- Binary or BCD Coding

GENERAL DESCRIPTION

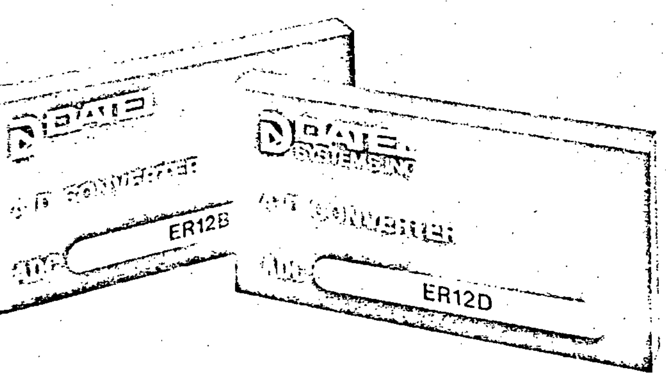
The ADC-ER series dual slope A/D converters feature ratiometric operation powered by a single +5 volt logic supply. Four-wire differential inputs give high common mode rejection with the useful capability of operating with input signal and external reference at different common mode levels; the external reference voltage can be varied over ±50% of nominal reference value. In addition, the conversion time can be externally adjusted to a 50 or 60 Hz period to give 40 dB minimum normal mode rejection of AC power line noise.

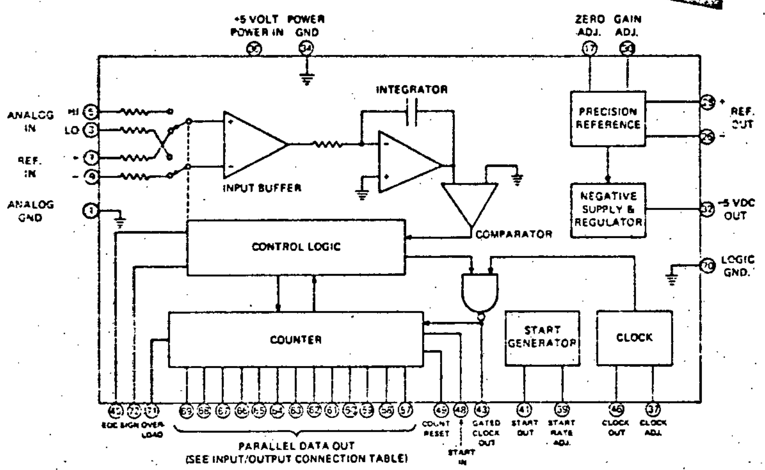
This series is available in 5 different models with resolutions of 8, 10, or 12 binary bits and sign and 2-1/2 or 3-1/2 BCD digits and sign. Important applications for these converters include test and instrumentation systems and signal conversion at transducer locations. Other operating features include: a gated clock output with a counter reset pulse for transmitting data to an external counter; an internal start pulse generator with externally adjustable rate; and a -5VDC power output supplying up to 5mA for externally powering a transducer bridge or auxiliary amplifier.

This combination of features makes the ADC-ER an extremely versatile A/D converter for systems applications. It contains an internal precision reference of 1V for binary models and 2V for BCD models which is used for normal, non-ratiometric operation. In ratiometric operation the input switches between input signal and external reference during the conversion cycle. Full scale input signal is ±1V for binary and ±2V for BCD; the input common mode voltage range is ±3V.

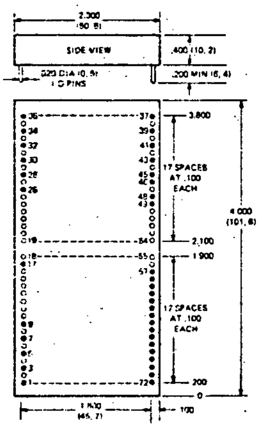
The external reference voltage range is 0.5 to 1.5V for binary models and 1 to 3V for BCD models. Common mode rejection for both signal and reference inputs is 70 dB minimum. Optimum normal mode AC line noise rejection is achieved by external adjustment of the clock frequency to synchronize the signal integration time to either 50 Hz or 60 Hz line period. Sign-magnitude coding is used in all models.

Input power requirement is +5VDC at 250mA maximum and the module size is a low profile 4 x 2 x 0.4 inches.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	DIGITAL OUTPUTS				
			BINARY BIT			BCD DIGIT	
			8B	10B	12B	8D	12D
1	ANALOG GROUND						
3	ANALOG IN, LO						
5	ANALOG IN, HI	57	X	X	X	X	1
7	+ REFERENCE IN	58	X	X	12	X	2
9	- REFERENCE IN	59	X	X	11	X	4
17	ZERO ADJUST	60	X	10	10	X	8
26	- REFERENCE OUT	61	X	9	9	1	10
28	+ REFERENCE OUT	62	8	8	8	2	20
30	GAIN ADJ.	63	7	7	7	4	40
32	-5VDC OUT	64	6	6	6	8	80
34	POWER GROUND	65	5	5	5	10	100
36	+5V POWER IN	66	4	4	4	20	200
37	CLOCK ADJUST	67	3	3	3	40	400
39	START RATE ADJ.	68	2	2	2	80	800
41	START OUT	69	1	1	1	100	1000
43	GATED CLOCK OUT						
45	E.O.C. (STATUS)						
46	CLOCK OUT						
48	START CONVERT						
49	COUNTER RESET						
70	LOGIC GROUND						
71	OVERLOAD						
72	SIGN						

X INDICATES NO PIN

Notes:
1. Open dots designate omitted pins
2. 0.100 inch = 2.5mm
3. Pin position tolerance is ±0.005" from datum, non-accumulative
4. Analog Ground, Power Ground, and Logic Ground are all connected together internally.

ELECTRICAL CHARACTERISTICS:

These specifications apply for $V_S = \pm15V$, $-25°C \leq T_A \leq +85°C$ for Q1, Q2 and N1 devices; $0°C \leq T_A \leq +70°C$; for Q3, Q4, T1 and T2 devices, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		10	10	10	bits
Linearity	"A" option (± ½ LSB –10 bits)	–	–	0.05	% I_{FS}
	"B" option (± ½ LSB –9 bits)	–	–	0.1	% I_{FS}
	"C" option (± ½ LSB –8 bits)	–	–	0.2	% I_{FS}
	"D" option (± ¾ LSB –8 bits)	–	–	0.3	% I_{FS}
Full Scale Tempco of I_{FS}	"A" option	–	–	15	ppm/°C
	"B" option	–	–	30	ppm/°C
	"C" option	–	–	60	ppm/°C
	"D" option	–	–	120	ppm/°C
	(For available linearity/tempco combinations, see Ordering Information)				
Settling Time	T_A = 25°C, to 0.05%	–	–	375	ns
	T_A = 25°C, to 0.1%	–	–	300	ns
	T_A = 25°C, to 0.2%	–	–	225	ns
	T_A = 25°C, to 0.4%	–	–	150	ns
	T_A = 25°C, to 0.8%	–	–	100	ns
Full Scale Output Voltage	Connect FS Adjust to V–				
	10V Models (Q1, Q3, T1, N1)	10	–	11.1	V
	5V Models (Q2, Q4, T2, N1)	5	–	5.55	V
	(Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω trimpot between FS Adjust and V–.)				
Zero Scale Output Voltage		–	–	0.006	% FS
Logic Inputs	Measured with respect to output pin				
High		2.1	–	–	V
Low		–	–	0.7	V
Logic Input Current, Each Input	V_{IN} = 0 to +6V	–	–	5	μA
Logic Input Resistance	V_{IN} = 0 to +6V	–	3	–	MΩ
Logic Input Capacitance		–	2	–	pF
Output Resistance		–	100	–	kΩ
Output Capacitance		–	13	–	pF
Applied Power Supplies:					
V+	Linearity within specification	+6	–	+18	V
V–	Linearity within specification	–6	–	–18	V
Power Supply Rejection	V_s = ±6V to ±18V	–	–	0.01	%per %
Power Consumption					
Q1, Q2, N1 models	V_s = ±6V	–	80	100	mW
	V_s = ±15V	–	200	250	mW
Q3, Q4, T1, T2 models	V_s = ±15V	–	200	300	mW

	ADC-ER8B/10B/12B (BINARY)	ADC-ER8D/10D/12D (BCD)
INPUTS		
Analog Input Range	±1V	±2V
Reference Input Range	+0.5 to +1.5V	+1 to +3V
Input Overvoltage, no damage	±20V	*
Input Impedance, both inputs	100 Meg. min.	*
Input Bias Current, both inputs	45nA typ., 500 nA max.	*
Common Mode Input Range	±3V min.	*
Common Mode Rejection, DC-60Hz	70 dB min.	*
Normal Mode Rejection, 50 or 60Hz	40 dB min.	*
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 μsec. min. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load	
OUTPUTS		
Parallel Output Data	8/10/12 parallel lines	8/12 parallel lines and overrange
	Output data held until next start convert pulse. Vout ("0") < +0.4V Vout ("1") > +2.4V Loading: 6 TTL loads	
Sign	Output HI for positive input Loading: 10 TTL loads	
Overload	Output HI for ± input > FS	
E.O.C. (Status)	Output HI during reset and conversion and LO when conversion is complete Loading: 4 TTL loads	
Gated Clock	Output pulse train giving:	
	N+4096 pulses	N+2000 pulses
	where N is converted count Loading: 8 TTL loads	
Counter Reset	Pulse HI for resetting external counters Loading: 4 TTL loads	
Clock Output	Continuous clock pulses with nominal frequency of 100 kHz Loading: 1 TTL load	
Start Output	Internally generated 100 nsec. start convert pulse at 2/sec. Can be externally adjusted for faster rate.	
Power Output	−5VDC ±5% @ 5mA max.	
PERFORMANCE		
Error, max.	.05% Reading ±1 count	*
Resolution	8/10/12 Bits	2½/3½ Digits
Coding	Sign-Mag. Binary	Sign-Mag. BCD
Temp. Coeff. of Gain, converter	±5ppm/°C max.	*
Temp. Coeff. of Gain, reference	±30ppm/°C max.	*
Temp. Coeff. of Zero	±30 μV/°C max.	*
Internal Reference	1V ±0.1%	2V ±0.1%
Power Supply Rejection	.01%/% max.	*
Conversion Time, 60Hz period	76.6 msec. max.	43.3 msec. max.
50Hz period	90.0 msec. max.	50.0 msec. max.
Warm Up Time	5 minutes	*
POWER REQUIREMENT	+5.0VDC ±5% @ 250mA max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C	*
Storage Temperature Range	−55°C to +85°C	*
Relative Humidity	Up to 100% non-condensing	
Case Size	4 X 2 X 0.4 inches (101,6 X 50,8 X 10,2 mm)	
Case Material	Black diallyl phthalate per MIL-M-14	
Pins	.020" round, gold plated, .200" lg. min.	
Weight	4 oz. max. (114 g.)	

*Specifications same as first column.

1. Both analog input signal and external reference look into identical differential inputs with an electronic switch switching between the two during the conversion cycle. A bias current of typically 45nA flows out of the input terminals and must be returned to ground. For single-ended operation Analog LO and either reference input should be connected to Analog Ground. Only one reference is required for either polarity of analog input.
2. Zero adjustment is required for either ratiometric or normal operation, but the gain adjustment is required only for normal operation (using internal reference) or applications where the internally trimmed accuracy of 0.1% is insufficient.
3. Optimum normal mode noise rejection for AC line frequencies is obtained by externally adjusting the clock frequency to give a signal integration time equal to the line frequency period of 50 or 60 Hz. This most easily done by using a digital counter connected to the Clock Output (pin 46). If normal mode noise is negligible or of high frequency, the adjustment is not necessary. For short term measurements an adjustment to within 0.1% of line period can be achieved, resulting in 60 dB of rejection. For longer term measurements, both line frequency and clock frequency drift slightly and a more reasonable match to within 1% results in 40 dB rejection.
4. The start rate adjustment allows operating at an internally set rate of 2 conversions/sec. or at faster rates up to 23/sec.

ORDERING INFORMATION

ADC-ER__

NO. OF BITS & CODING
8B = 8 Binary Bits
10B = 10 Binary Bits
12B = 12 Binary Bits
8D = 2½ BCD Digits
12D = 3½ BCD Digits

PRICES (1-9)

ADC-ER8B $79.00
ADC-ER10B $89.00
ADC-ER12B $99.00
ADC-ER8D $79.00
ADC-ER12D $99.00

Mating Sockets: DILS-2 (4/module) $5.00/pair
Trimming Potentiometers:
TP100K, TP10K at $3.00 each

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing and delivery.

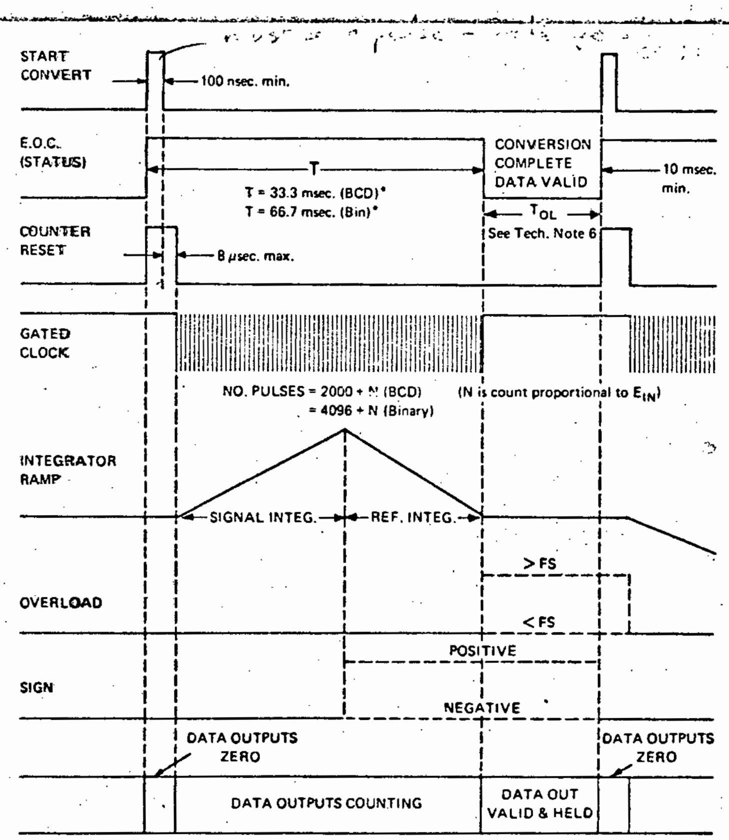
-EX −25° to +85°C operation
-EXX-HS −55°C to +85°C operation with hermetically sealed semiconductor components.

The ADC-ER Series Converters are covered by GSA Contract No. GS-00S-27959, FSC Group 66, Part II Section H, period 3-1-75 through 2-29-76.

(BCD) or 13/sec. (Binary) by external adjustment. To operate with the internal start convert, pin 41 must be connected to pin 48. The converter may also be started externally by means of a 100 nsec. min. start convert pulse applied directly to pin 48.

5. The −5V power output from the converter may be used to power a transducer bridge or an auxiliary input amplifier such as μA776, LM308, or 4250 in conjunction with the +5V input power. The 5mA maximum output should not be exceeded or it will affect the operation of the converter. *This output is short circuit protected to ground but should not under any circumstance be connected to +5V or any other power supply output voltage since damage to the converter will result.* The −5V output is regulated to give a constant 10V difference with respect to the +5V power input with a typical tempco of ±100ppm/°C.

6. Analog inputs exceeding the ±5V supply voltage, although they will not cause any damage up to ±20V, will cause the input switch to malfunction. This will cause the overload output to remain high and the sign output may be invalid. If inputs exceeding ±5V are to be encountered in an application, it is recommended that clamping diodes be used from the inputs to ±5V. Overload recovery time, T_{OL}, after a ±5V input overload is 30 msec. for all BCD models and 50 msec. for all binary models. See timing diagram.



*When synchronized to 60 Hz period. For 50 Hz period: T = 50.0 msec. (BCD)
T = 90.0 msec. (Bin)

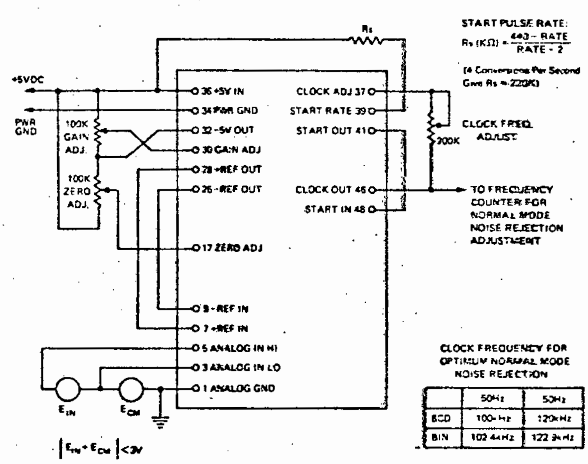
BCD CODING

SCALE	2 1/2 DIGIT		3 1/2 DIGIT	
	INPUT (±)	OUTPUT CODE	INPUT (±)	OUTPUT CODE
FS-1 LSD	1.99V	1 1001 1001	1.999V	1 1001 1001 1001
3/4 FS	1.50V	1 0101 0000	1.500V	1 0101 0000 0000
1/2 FS	1.00V	1 0000 0000	1.000V	1 0000 0000 0000
1/2 FS-1 LSD	0.99V	0 1001 1001	0.999V	0 1001 1001 1001
1/4 FS	0.50V	0 0101 0000	0.500V	0 0101 0000 0000
1 LSD	0.01V	0 0000 0001	0.001V	0 0000 0000 0001
0	0.00V	0 0000 0000	0.000V	0 0000 0000 0000

BINARY CODING

SCALE	8 BIT		10 BIT		12 BIT	
	INPUT (±)	CODE	INPUT (±)	CODE	INPUT (±)	CODE
FS-1 LSB	.996V	1111 1111	.9990V	1111 1111 11	.99976V	1111 1111 1111
7/8 FS	.875V	1110 0000	.8750V	1110 0000 00	.87500V	1110 0000 0000
3/4 FS	.750V	1100 0000	.7500V	1100 0000 00	.75000V	1100 0000 0000
1/2 FS	.500V	1000 0000	.5000V	1000 0000 00	.50000V	1000 0000 0000
1/4 FS	.250V	0100 0000	.2500V	0100 0000 00	.25000V	0100 0000 0000
1/8 FS	.125V	0010 0000	.1250V	0010 0000 00	.12500V	0010 0000 0000
1 LSB	.004V	0000 0001	.0010V	0000 0000 01	.00024V	0000 0000 0001
0	.000V	0000 0000	.0000V	0000 0000 00	.00000V	0000 0000 0000

STANDARD CONNECTIONS AND CALIBRATION



	50Hz	60Hz
BCD	100kHz	120kHz
BIN	102.4kHz	122.9kHz

CALIBRATION

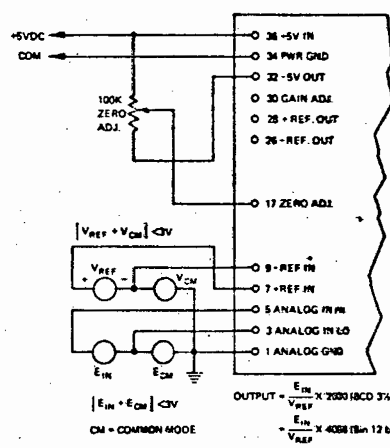
1. Connect the converter as shown in the diagram. Allow a 5 minute warm-up before making final adjustments.
2. Zero Adjustment. Short together Analog In HI (pin 5), Analog In LO (pin 3), and Analog Ground (pin 1). Adjust zero trimming potentiometer to obtain a flickering Sign (pin 72) and logic zero on all parallel data output lines.
3. Gain Adjustment. Apply a precision reference input voltage between Analog In HI (pin 5) and Analog In LO (pin 3) with the latter connected to Analog Ground (pin 1). Set the precision reference to a voltage near full scale (see coding tables) and adjust the gain trimming potentiometer to give the correct digital output code.

NOTE: The gain adjustment is internally trimmed to within ±0.1% accuracy. If this accuracy is sufficient, then pin 30 should be left open. The gain adjustment is not necessary for ratiometric operation.

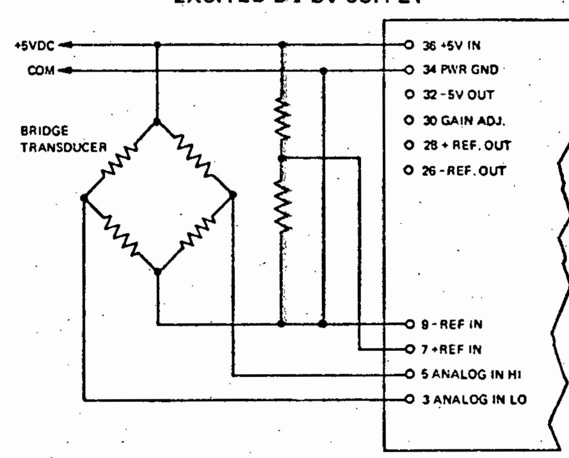
ADJUSTMENT OF CLOCK FREQUENCY AND START RATE

1. To obtain optimum normal mode noise rejection at either 50 or 60 Hz, the Clock Frequency Adjust potentiometer should be adjusted to give the appropriate clock frequency shown in the table. This is most easily done using a frequency counter connected to the Clock Out (pin 46). Although a 200K adjustment potentiometer gives a full range of adjustment, most accurate adjustment is achieved by a 10K trimming potentiometer in series with an appropriate fixed resistor value.
2. The internal start pulse generator operates at a nominal rate of 2 pulses/second with no connection to pin 39. To increase the conversion rate a resistor may be connected as shown from pin 39 to +5V as illustrated in the calibration diagram.

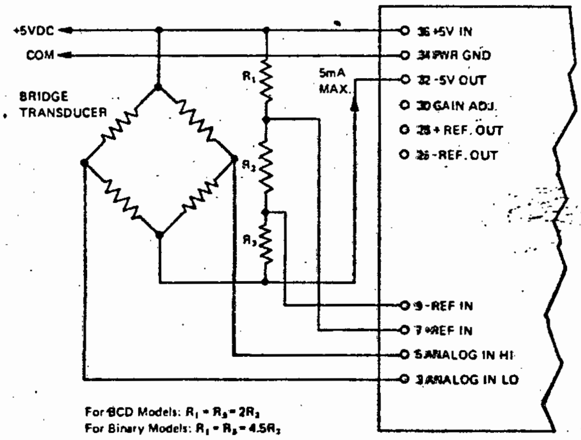
RATIOMETRIC OPERATION



USING WITH BRIDGE TRANSDUCER EXCITED BY 5V SUPPLY

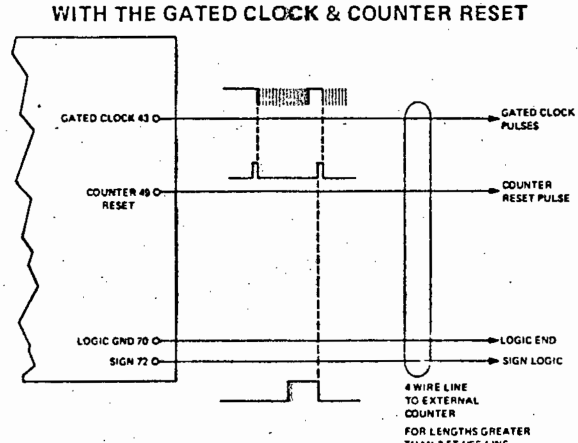


USING WITH BRIDGE TRANSDUCER AND -5V OUTPUT TO MINIMIZE INPUT COMMON-MODE VOLTAGE



For BCD Models: $R_1 = R_3 = 2R_2$
For Binary Models: $R_1 = R_3 = 4.5R_2$

DRIVING AN EXTERNAL COUNTER WITH THE GATED CLOCK & COUNTER RESET



PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

DATEL SYSTEMS, INC. 1020 TURNPIKE STREET, CANTON, MASS. 02021

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(213) 933-7256

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5/75 BULLETIN AER-L10504

Appendix G (v)

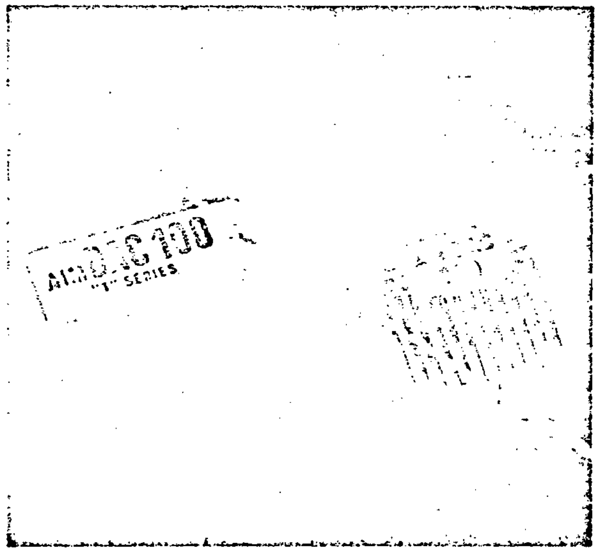
TECHNICAL SPECIFICATIONS NOVEMBER 1973

AIM DAC100

8 & 10 BIT I.C. DIGITAL-TO-ANALOG CONVERTER SERIES

FEATURES:

- COMPLETE .... INCLUDES REFERENCE, CURRENT SOURCES LADDER, SWITCHES
- COMPACT .... 16 PIN DIP OR 24 PIN FLATPACK
- COMPATIBLE .... TTL, DTL LOGIC LEVELS
- LOW POWER .... 80mW TYP AT ±6V
- WIDE SUPPLY RANGE .... ±6V TO ±18V
- FAST SETTLING .... 225nS (8 BITS), 375nS (10 BITS)
- 8 & 10 BIT MODELS............. WIDE CHOICE OF SPECIFICATIONS
- FLEXIBLE .... HIGH SPEED 0-2mA OUTPUT
- RELIABLE .... 100% POWER BURN-IN @ 125°C
- STABLE .... TEMPCOS TO ±15ppM/°C MAX
- HIGH LINEARITY .. TO 0.05% MAX, –25°C TO +85°C
- WIDE OPERATING TEMP RANGE ... –55°/+125° AND 0°/+70°C

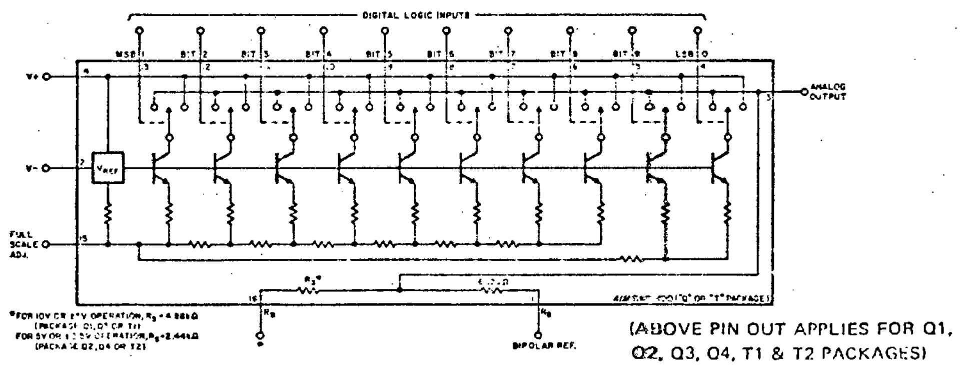


GENERAL DESCRIPTION

The AIMDAC 100 series are complete 10 bit resolution Digital-to-Analog converters constructed on two monolithic chips in a single 16 pin DIP or 24 pin flatpack. Featuring excellent linearity vs. temperature performance, the AIMDAC 100 includes a low tempco voltage reference, 10 current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, and matched bipolar offset and feedback resistors are included for use with an external op amp for voltage output applications. Although all units have 10 bit resolution, a wide choice of linearity and tempco options are provided to allow optimization of price/performance ratio.

The small size, wide operating temperature range, low power consumption and high reliability construction make the AIMDAC100 ideal for aerospace applications, with MIL-M-38510 processing available. Low cost 0°/+70°C versions are available for all industrial requirements. Applications for the AIM DAC100 series include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power suppliers, analog meter movement drivers, waveform generators and in high speed Analog-to-Digital converters.

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM (DUAL-IN-LINE PACKAGES)



(ABOVE PIN OUT APPLIES FOR Q1, Q2, Q3, Q4, T1 & T2 PACKAGES)

The premium performance of this product is achieved through an advanced processing technology. All Precision Monolithics products are guaranteed to meet or exceed published specifications.

PRECISION MONOLITHICS INCORPORATED

AIM DAC100 8 & 10 BIT IC D/A CONVERTER SERIES

GENERAL INFORMATION:

1. The AIMDAC100 series are digital-to-analog current converters; voltage outputs may be easily implemented by using an external operational amplifier with the internally provided feedback resistor. For clarity and convenience, most specifications will reference full scale output voltage rather than full scale output current, assuming an "ideal" op amp has been utilized for conversion.

2. The logic coding used for driving the AIMDAC 100 should be complementary binary or offset complementary binary to obtain unipolar and bipolar analog outputs, respectively.

3. The AIMDAC 100 series provides a wide variety of worst-case linearity and full-scale tempco combination options. All devices have 10 bits of resolution; the linearity options of 0.05%, 0.1%, 0.2% and 0.3% guarantee monotonic operation for resolutions of 10, 9, 8, and 7 bits respectively. When less than the full 10 bits are utilized, the unused logic inputs must be connected to a "high" logic level.

4. AIMDAC 100 devices in Q1, Q2 and N1 packages receive many of the 100% processing steps specified by MIL-M-38510, including visual inspection per 883-2010 1B and 96 hours of burn-in at +125°C. Devices completely processed in compliance with 38510 levels A and B are available. All AIMDAC 100 devices specified for 0°C to +70° operation receive at least 72 hours of burn-in.

ABSOLUTE MAXIMUM RATINGS:

V+ Supply to V− Supply	0 to +36V
V+ Supply to Output	0 to +18V
V− Supply to Output	0 to −18V
Logic Inputs to Output	−6V to +6V
Logic Inputs to V+ Supply (Note 1)	−18V to 0V
Logics Inputs to V− Supply (Note 1)	0 to +18V
Power Dissipation (Note 2)	500mW

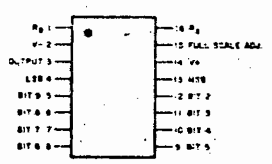
Operating Temperature Range	
Q1, Q2 and N Packages (Note 2)	−55°C to +125°C
Q3, Q4 and T Packages	0°C to +70°C
Storage Temperature Range	
Q and N Packages	−65°C to +150°C
T Packages	−55°C to +125°C
Lead Temperature (Soldering)	
Q and N Packages	+300°C (60 sec)
T Packages	+260°(10 sec)

NOTES:

1. Important: see Applications section for information on improper power supply/logic input combinations

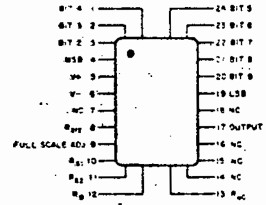
2. Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.

PIN CONNECTIONS: (TOP VIEW)



16 PIN DIP (Q OR T SUFFIX)

Q1, Q2, Q3, Q4, T1, T2



24 PIN FLATPACK (N SUFFIX)

N1,

ORDERING INFORMATION:

AIMDAC100 devices are available in a wide variety of package/temperature range/linearity/tempco/output voltage combinations. The complete part number includes suffixes which indicate the specific parameter selected, as shown below:

ORDER NUMBER: AIMDAC-100 X X X X

LINEARITY		F.S. TEMPCO		PACKAGE, TEMP RANGE AND OUTPUT VOLTAGE	
0.05% MAX	A	15 ppm/°C MAX	A	16 Pin Hermetic Dip, −55/+125°C, 10V and ±5V	Q1
0.1% MAX	B	30 ppm/°C MAX	B	16 Pin Hermetic Dip, −55/+125°C, 5V and ±2.5V	Q2
0.2% MAX	C	60 ppm/°C MAX	C	24 Pin Hermetic Flatpack, −55/+125°C, 10V, 5V, ±5V, ±2.5V	N1
0.3% MAX	D	120 ppm/°C MAX	D	24 Pin Hermetic Flatpack, −55/+125°C, 10V, 5V, ±5V, ±2.5V	N2*
				16 Pin Hermetic Dip, 0/+70°C, 10V and ±5V	Q3
				16 Pin Hermetic Dip, 0/+70°C, 5V and ±2.5V	Q4
				16 Pin Plastic Dip, 0/+70°C, 10V and ±5V	T1
				16 Pin Plastic Dip, 0/+70°C, 5V and ±2.5V	T2

SPECIAL NOTE: The following linearity/tempco option combinations are available for the above −55/+125°C (Q1, Q2, N1) models: AA, AC, AD, BA, BB, BC, CC, DD.

The following linearity/tempco option combinations are available for the above 0/+70°C (Q3, Q4, T1, T2) models: AC, BC, CC, DD.

*N2 device similar to N1 except pin-for-pin replacement for µA722 and companion resistor network.

AIM DAC100 APPLICATION NOTES

LOGIC CODING – The AIM DAC100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full scale output, while an all "ones" input produces a zero scale output. The output may be easily modified to accommodate complementary offset binary, complementary one's complement and complementary two's complementary codes.

LOGIC COMPATIBILITY – The input logic levels are directly compatible with DTL and TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

LOWER RESOLUTION APPLICATIONS – The AIM DAC100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs *must* be tied to the high logic for proper operation. "Floating" logic inputs can cause improper operation.

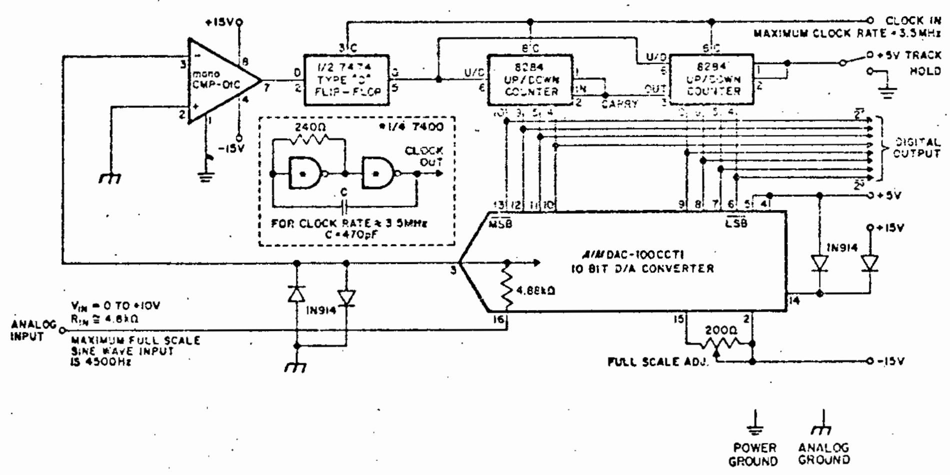
FULL SCALE OUTPUT ADJUSTMENT – The output current of the AIM DAC100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the Full Scale Adjust pin and V–. Adjustment should be made with an input of all "zeroes."

BIPOLAR OPERATION – The AIM DAC100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volt reference. Trimming procedure is as follows: with inputs set to all "ones", adjust Bipolar Offset pot to desired negative Full Scale Voltage; with inputs set to all "zeroes," adjust Full Scale pot to desired positive Full Scale Voltage. (Make certain correct end point voltages are used with one's and two's complement codings.)

VOLTAGE AT OUTPUT PIN – The AIM DAC100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output ground is a convenient way of clamping the output to this limit.

POWER SUPPLY SEQUENCING – **IMPORTANT** – Occasional early AIM DAC100 devices may suffer temporary malfunction and possible permanent damage if voltage is present at the logic inputs before the V+ supply is available. A simple protection circuit may be implemented by using two silicon diodes to clamp the V+ terminal to the logic supply as shown in the diagram on page 7.

LOW COST 8 BIT TRACKING A/D CONVERTER



(FOR FULL DETAILS, REQUEST APPLICATION NOTE: "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER")

Appendix G (vi)

INSTRUCTION MANUAL

REGULATED POWER SUPPLIES

LOS W SERIES

SPECIFICATIONS AND FEATURES

DC OUTPUT — Voltage regulated for line and load. For voltage and current ratings see table I below.

TABLE I

MODEL	VOLTAGE RANGE	MAXIMUM CURRENT (AMPS) AT AMBIENT TEMPERATURE		
		40°C	50°C	60°C
LOS-W-2	2 ± 5%	12.0	10.5	8.5
LOS-W-5	5 ± 5%	12.0	10.5	8.5
LOS-W-6	6 ± 5%	10.0	9.0	7.3
LOS-W-12	12 ± 5%	7.0	5.8	4.6
LOS-W-15	15 ± 5%	6.3	5.2	4.0
LOS-W-20	20 ± 5%	5.2	4.2	3.2
LOS-W-24	24 ± 5%	4.8	3.8	2.8
LOS-W-28	28 ± 5%	4.2	3.3	2.4

Current range must be chosen to suit the appropriate maximum ambient temperature. Current ratings apply for entire voltage range.

REGULATED VOLTAGE OUTPUT

Regulation (line) .... 0.15% for input variations from 105-125, 125-105, 210-250, or 250-210 volts AC.

Regulation (load) .... 0.15% for load variations from no load to full load or full load to no load.

Ripple and Noise .... 1.5mV rms, 5mV peak to peak with either positive or negative terminal grounded.

Temperature Coefficient .... 0.03%/°C

Remote Programming

External Resistor

LOS-W-2 .... Nominal 1000 ohms/volt output. The programming coefficient is negative. Increasing resistance decreases output voltage. Use a low temperature coefficient resistor to assure most stable operation.

LOS-W-5 through LOS-W-28 .... Nominal 200 ohms/volt output. Increasing resistance increases output voltage. Use a low temperature coefficient resistor to assure most stable operation.

Programming Voltage .... One-to-one voltage change. The programming supply must have a reverse current capability of 6 ma min. Programming supply need not have reverse current capability when programming LOS-W-2.

Remote Sensing .... Provision is made for remote sensing to eliminate the effect of power output lead resistance on DC regulation. Sensing leads should be a twisted pair to minimize AC pickup. A 2.5 mf elect. capacitor may be required between output terminals and sense terminals to reduce noise pickup.

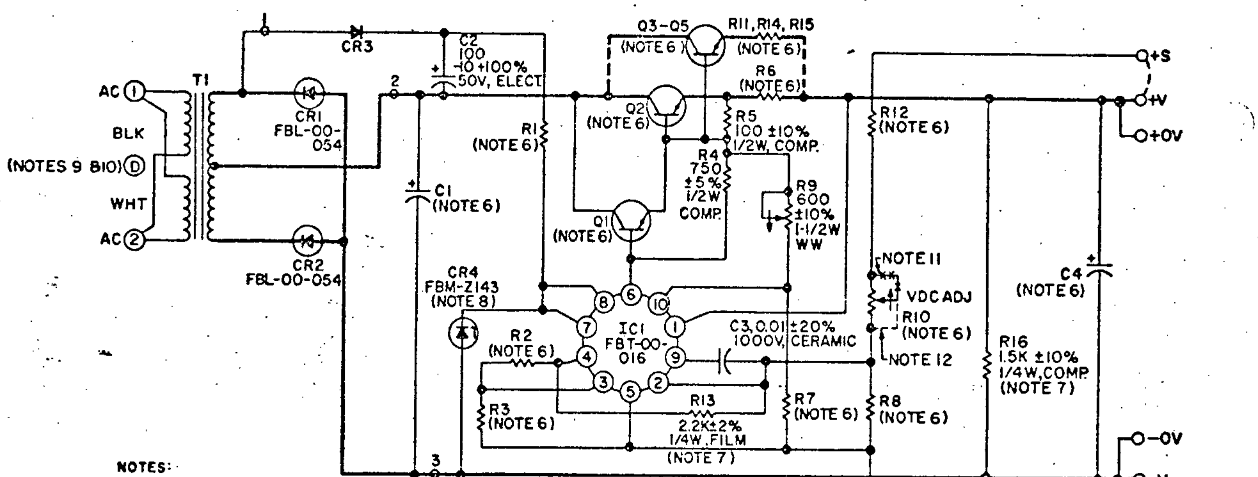
OVERSHOOT — No overshoot under conditions of power turn-on, turn-off, or power failure

AC INPUT — 105-125 or 210-250 volts AC at 47-440 Hz. Standard LOS-W power supplies are factory wired for 105-125 volt input but can be rewired for 210-250 volt input. See figure 1 and schematic diagram for rewiring of AC input. Input power: 240 Watts*. Ratings apply for 57-63 Hz input. For 47-53 Hz input derate current 10% for each ambient temperature given in table I. For 63-440 Hz input consult factory.

*With output loaded to full current rating and input voltage 125 volts AC, 60 Hz.

OVERLOAD PROTECTION — Automatic electronic current limiting circuit, limits output current to a safe value, protecting load and power supply when external overloads and direct shorts occur.

G-9094-5



NOTES:

1. RESISTOR VALUES ARE IN OHMS.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. DESIGNATIONS ARE LAMBDA PART NUMBERS.
4. SYMBOLS:
   - INDICATES CLOCKWISE ROTATION OF SHAFT.
   - INDICATES CONNECTION TO CHASSIS.
   - LAMBDA PART NO. FBL-00-030, USE IN4002 DIODE FOR REPLACEMENT UNLESS OTHERWISE NOTED.
   - INDICATES TERMINAL ON PRINTED CIRCUIT BOARD.
   - INDICATES ACTUAL UNIT MARKING.
5. FOR OPERATION AT 47-53Hz, DERATE CURRENT BY 10%. FOR OPERATION AT 63-440Hz, CONSULT FACTORY.
6. SEE TABLE II FOR COMPONENT VALUES.
7. R13 & R15 ONLY USED ON MODEL LOS-W-2.
8. CR4 ONLY USED ON MODELS LOS-W-12 THRU LOS-W-28.
9. T1 PRIMARY CONNECTION SHOWN IS FOR 105-125VAC INPUT. FOR 210-250VAC INPUT: DISCONNECT BLK & WHT TRANSFORMER LEADS FROM TERM'S AC1 & AC2 AND RECONNECT BOTH LEADS TO TERM D.
10. "J" OPTION UNITS HAVE SINGLE T1 PRIMARY. AC INPUT IS 90-110 VAC.
11. NOT USED ON MODEL LOS-W-2.
12. ONLY USED ON MODEL LOS-W-2.

FOR WIRING OF POWER SUPPLY TO LOAD REFER TO SUPPLY-TO-LOAD WIRING DIAGRAMS.

DOTTED CONNECTIONS SHOWN INDICATE JUMPERS IN PLACE FOR LOCAL SENSING CONNECTION.

SCHEMATIC DIAGRAM
REGULATED POWER SUPPLY

MODELS
LOS-W SERIES

LAMBDA
ELECTRONICS CORP.
MELVILLE, NEW YORK
A Veeco SUBSIDIARY

TABLE II
SCHEMATIC DATA REFERENCES
MODELS LOS-W-2 THRU LOS-W-28

Models	Schematic Components														
	C1	C4	Q1-Q4	Q5	R1	R2	R3	R6	R7	R8	R10	R11	R12	R14	R15
	-10+100% ELECT	-10+75% ELECT	*FBN-	*FBN-	±10% COMP	FILM	1/4W FILM	±5% 2W WW	1/2W COMP	1/4W FILM	±10% 1-1/2W WW	±5% 2W WW	1/4W FILM	±5% 2W WW	±5% 2W WW
LOS-W-2	15,000 mf 15 vdc	600 mf 16 vdc	L157	L157	68 1/2W	4.7K ±2% 1/4W	2.2K ±2%	0.10	750 ±5%	2.2K ±2%	600	0.10	Jumper	0.10	0.10
LOS-W-5	26,000 mf 15 vdc	600 mf 16 vdc	L157	L157	470 1/2W	2.49K ±1% 1/2W	3.83K ±1%	0.10	2.2K ±5%	825 ±1%	600	0.10	Jumper	0.10	0.10
LOS-W-6	16,000 mf 15 vdc	600 mf 16 vdc	L157	L157	470 1/2W	2.49K ±1% 1/2W	3.83K ±1%	0.15	2.2K ±5%	825 ±1%	600	0.15	Jumper	0.15	0.15
LOS-W-12	9000 mf 30 vdc	350 mf 25 vdc	L156	L156	2.2K 1W	619 ±1% 1/4W	Not Used	0.30	5.6K ±10%	1.47K ±1%	600	0.30	768 ±1%	0.30	0.30
LOS-W-15	9000 mf 30 vdc	350 mf 25 vdc	L156	L156	2.2K 1W	619 ±1% 1/4W	Not Used	0.30	7.5K ±5%	1.47K ±1%	1.2K	0.30	1.21K ±1%	0.30	0.30
LOS-W-20	6600 mf 50 vdc	250 mf 50 vdc	L156	Not Used	4.7K 2W	1K ±1% 1/2W	Not Used	0.30	10K ±5%	1.47K ±1%	1.2K	0.30	2.2K ±2%	0.30	Not Used
LOS-W-24	6600 mf 50 vdc	250 mf 50 vdc	L156	Not Used	4.7K 2W	1K ±1% 1/2W	Not Used	0.30	13K ±5%	1.47K ±1%	1.2K	0.30	3.01K ±1%	0.30	Not Used
LOS-W-28	6600 mf 50 vdc	250 mf 50 vdc	L156	Not Used	6.8K 2W	1K ±1% 1/2W	Not Used	0.30	15K ±5%	1.47K ±1%	1.8K	0.30	3.48K ±1%	0.30	Not Used

*Lambda part no.

INSTRUCTION MANUAL

REGULATED POWER SUPPLIES

LOD-Y-152,LOD-Z-152

SPECIFICATIONS AND FEATURES

DC OUTPUT — Voltage regulated for line and load. For voltage and current ratings see table I

TABLE I

MODEL	VOLTAGE RANGE	MAXIMUM CURRENT (mA) AT AMBIENT TEMPERATURE		
		40°C	50°C	60°C
LOD-Y-152	±12 to ±15	1000	750	500
LOD-Z-152	±12 to ±15	500	375	250

Current range must be chosen to suit the appropriate maximum ambient temperature. Current ratings apply for entire voltage range.

REGULATED VOLTAGE OUTPUT (each side)
- Regulation (line) .... 0.15% for input variations from 105-125 or 125-105 volts AC.
- Regulation (load) .... 0.15% for load variations from no load to full load or full load to no load.
- Ripple and Noise .... 1.5mV rms, 5mV peak to peak.
- Temperature Coefficient .... 0.03%/°C
- Remote Sensing .... Provision is made for remote sensing to minimize the effect of power output lead resistance on DC regulation. Sensing leads should be a twisted pair to minimize AC pickup. A 2.5 mf elect., capacitor may be required between output terminals and sense terminals to reduce noise pickup.

OVERSHOOT — No overshoot under conditions of power turn-on, turn-off, or power failure.

AC INPUT — 105-125 or 210-250 volts AC at 47-440 Hz. Standard LOD-Y and LOD-Z power supplies are factory wired for 105-125 volt input, but can be rewired for 210-250 volt input. See Figure 1 and schematic diagram for rewiring of AC input. Input power*: 75 Watts (LOD-Y) 40 Watts (LOD-Z). Power factor*: 0.7. Ratings apply for 57-63Hz input. For 47-53Hz input derate current 10% for each ambient temperature given in table I. For 63-440 Hz input consult factory.
*With output loaded to full current rating and input voltage 125 volts AC, 60Hz.

TRACKING — Absolute difference between negative and positive outputs within 2%; 0.2% change for all conditions of line, load, and temperature.

OVERLOAD PROTECTION — Automatic electronic current limiting circuit, limits output current to a safe value, protecting load and power supply when overloads and direct shorts occur.

INPUT AND OUTPUT CONNECTIONS — See outline drawing for location.
- AC input .... Terminals on transformer
- Ground .... Terminal on transformer
- DC output .... Turret terminal on printed circuit board
- Sensing .... Turret terminal on printed circuit board
- Overvoltage Protector .... Quick disconnect terminal on printed circuit board with mating connector attached.

OPERATING AMBIENT TEMPERATURE RANGE AND DUTY CYCLE — Continuous duty from 0°C to +60°C ambient with corresponding load current ratings for all modes of operation.

STORAGE TEMPERATURE — -20°C to +85°C

DC OUTPUT CONTROL — Screwdriver voltage adjust control permits adjustment of DC output voltage. See outline drawing for location of control.

GUARANTEE — 60 day guarantee from date of shipment ..... materials and labor.

PHYSICAL DATA
- Size .... LOD-Y: 5-5/8" x 4-7/8" x 2-1/2"; LOD-Z: 4-7/8" x 4" x 1-5/8"
- Weight .... LOD-Y: 3-3/4 lbs. net; 4 lbs. shipping; LOD-Z: 1-7/8 lbs. net; 2-1/8 lbs. shipping.
- Finish .... Gray, FED. STD. 595 No. 26081

MOUNTING — Three surfaces, each with clearance mounting holes, can be utilized for mounting this unit. Air circulation is required when unit is mounted in confined areas. Refer to Outline Drawing for mounting details.

"J" OPTION — Standard LOD-Y and LOD-Z power supplies can be obtained for 90-110 VAC, 47-440 Hz input. For 47-53 Hz input derate current 10% for each ambient temperature given in table I. For 63-440 Hz input consult factory.

OVERVOLTAGE PROTECTOR ACCESSORY
- Adjustable .... Externally mounted Overvoltage Protector LMOV-3 is available. Additional wire must be added to the Overvoltage Protector leads in order to reach the power supply output terminals.

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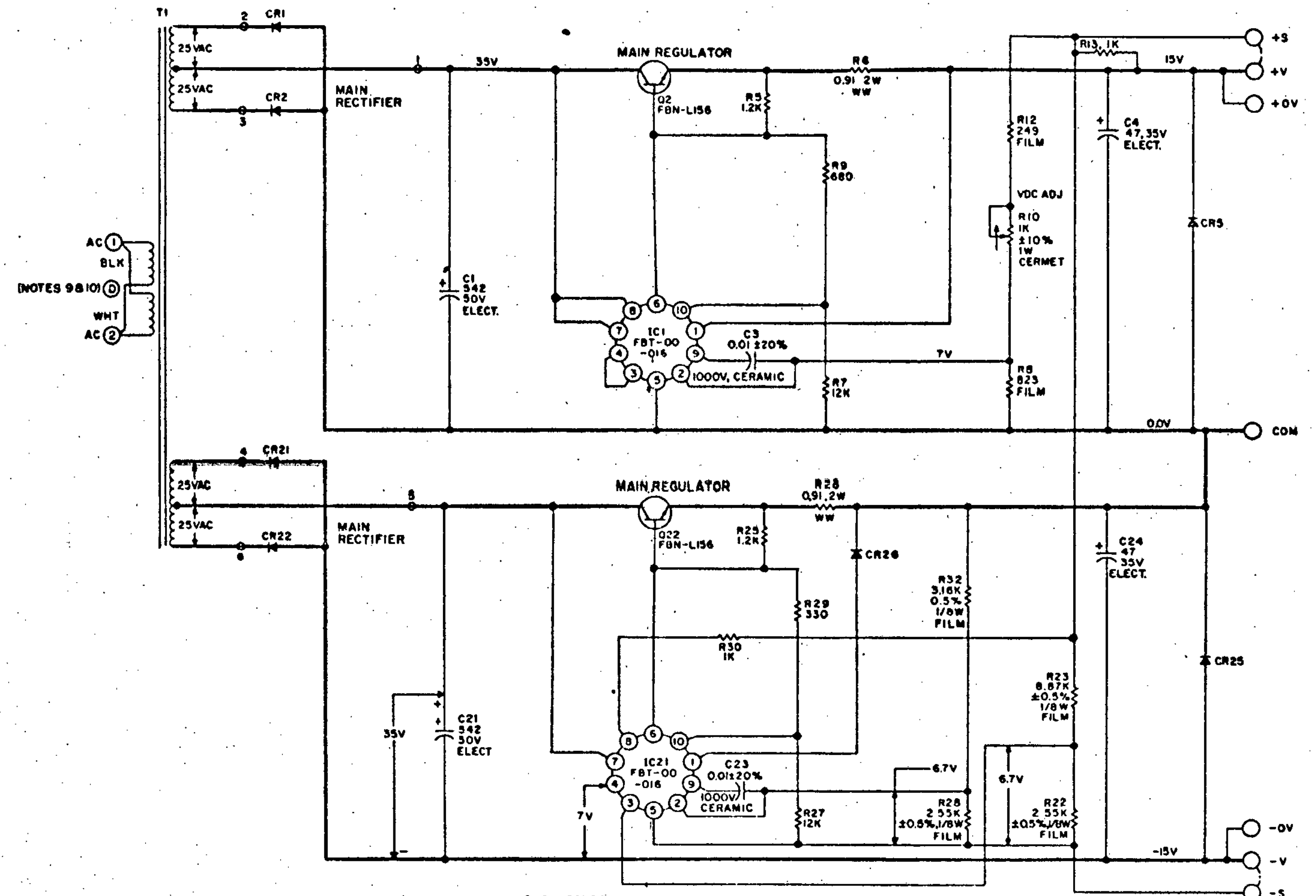

FOR WIRING OF POWER SUPPLY TO LOAD REFER TO SUPPLY-TO-LOAD WIRING DIAGRAMS.
DOTTED CONNECTIONS SHOWN INDICATE JUMPERS IN PLACE FOR LOCAL SENSING CONNECTION.

SCHEMATIC DIAGRAM
REGULATED POWER SUPPLY

LOD-Z-152

LAMBDA

ELECTRONICS CORP.
MELVILLE, NEW YORK

A Veeco SUBSIDIARY

NOTES:

1. RESISTORS ARE COMP. 1/4W WITH VALUES IN OHMS, UNLESS OTHERWISE NOTED.
2. RESISTOR TOLERANCES: COMP. ±10%, FILM ±1%, WIREWOUND ±5%, UNLESS OTHERWISE NOTED.
3. CAPACITOR VALUES ARE IN MICROFARADS.
4. CAPACITOR TOLERANCES: ELECTROLYTIC -10 +75%.
5. DESIGNATIONS ARE LAMBDA PART NUMBERS.
6. SYMBOLS:
   - INDICATES CLOCKWISE ROTATION OF SHAFT.
   - INDICATES CONNECTION TO CHASSIS.
   - LAMBDA PART NO FBL-00-030; USE IN4002 DIODE FOR REPLACEMENT UNLESS OTHERWISE NOTED.
   - INDICATES TERMINAL ON PRINTED CIRCUIT BOARD.
   - INDICATES ACTUAL UNIT MARKING.
7. CONDITIONS FOR CIRCUIT POINT MEASUREMENTS: INPUT: 115VAC, 60 Hz. MAX. RATED VOLTAGE NO LOAD. INDICATED VOLTAGES ARE TYPICAL VALUES AND ARE D.C. UNLESS OTHERWISE NOTED. D.C. MEASUREMENTS TAKEN WITH 20,000 OHMS/V VOLTMETER BETWEEN COM. AND INDICATED POINTS UNLESS OTHERWISE NOTED.
8. DERATE CURRENT 10% FOR 47-53Hz INPUT, FOR 63-440Hz INPUT CONSULT FACTORY.
9. T1 PRIMARY CONNECTION SHOWN IS FOR 105-125 VAC INPUT. FOR 210-250 VAC INPUT: DISCONNECT BLK & WHT TRANSFORMER LEADS FROM TERMINALS AC1 & AC2. RECONNECT BOTH LEADS TO TERM. D
10. "J" OPTION UNITS HAVE SINGLE T1 PRIMARY. AC INPUT IS 90-110 VAC.

APPENDIX H.

THEORY OF OPERATION OF A CONSTANT VOLTAGE TRANSFORMER (PARAMETRIC TRANSFORMER)

(For detailed derivations and formulae see Ref. 21).

The phenomenon of parametric oscillations is of frequent occurrance in physical systems and has been recognized for a long time. In an electric circuit consisting of a resistence, inductance and capacitance if, by some means, either the inductance or the capacitance is made to vary periodically at twice the natural frequency of the circuit, parametric oscillations start to build up. In the absence of a limiting device or mechanism, amplitude of both current and voltage will continue to increase until some component breaks down. This kind of oscillation can generally be described by a second-order linear differential equation with a periodically time-varying coefficient of the Hill's or Mathieu's type. The presence of some non-linearity in the actual system may cause the oscillations to stabilize at a finite steady amplitude.

A method of obtaining the required double-frequency variation in the inductance is through the interaction between the magnetic field of two stationary iron-cored circuits. The resulting device may be termed a "parametric transformer" since it is capable of transforming electrical energy from one circuit to another through parametric excitation.

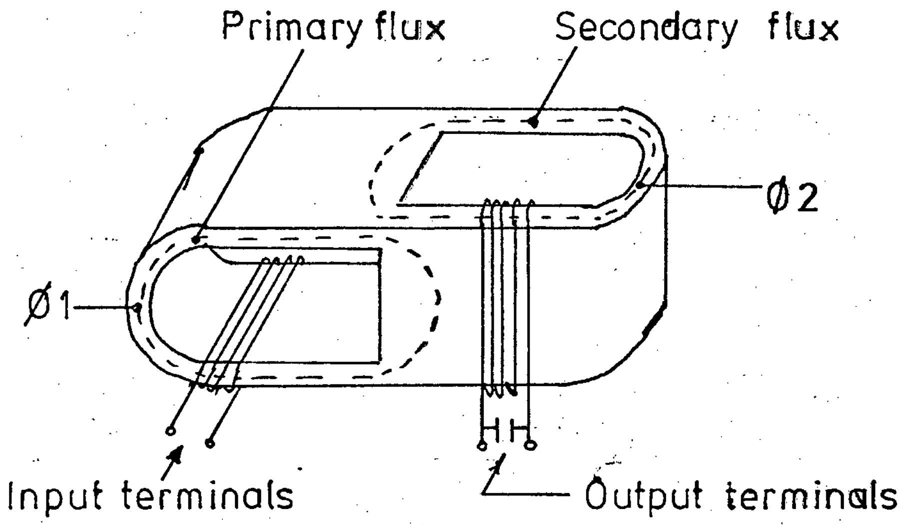

FIG. 25

Figure 25 depicts the cores and windings arrangement of a parametric power transformer. The two cores are 90 degrees relative to each other in space and so are the windings. The mutual inductance between the two circuits in, therefore, practically zero; and a capacitor is connected across the secondary winding. Since parts of the magnetic circuit are common to both cores, the flux Ø1 can produce a change in the reluctance and hence, the inductance of the secondary circuit. A sinusoisally varying primary flux at a frequency W_1 can therefore, produce a periodic variation in the secondary inductance at the double frequency $2W_1$.

If the inductance of the secondary is made to vary at double the frequency to which the circuit is tuned, and provided certain oscillatory requirements are met, parametric oscillations will build up. Because of saturation of the secondary core, the secondary inductance will be modified and the amplitude of oscillations will stabilize at a finite steady value.

The required double frequency variation in inductance is produced by the primary flux. The secondary side by itself, therefore, constitutes a parametric power oscillator which must be "pumped" at twice its output frequency. The energy dissipated in the secondary circuit as losses as well as the load connected across the secondary terminals, has to be supplied by the "pump". But since the secondary has no direct external source for its excitation, the primary side has to act as a pump, drawing energy from the main supply and delivering it to the secondary indirectly, through the degree of variation of the parameter which is the secondary inductance.

O load across the terminals of the secondary has a damping effect on the secondary oscillations causing detuning and lowering of the Q-factor of the circuit. The secondary voltage is at the same frequency but 90° out of phase with the primary voltage.

Unlike the conventional transformer, the secondary of a parametric transformer operates like an oscillator and its output voltage is produced through parametric oscillations and not through electromagnetic induction. The secondary voltage is, therefore, largely independent of the harmonics in the primary voltage. This feature makes the parametric transformer an excellent natural line filter and regulator.