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**UNIVERSITY OF CAPE TOWN**

**VIABILITY STUDY TO IMPLEMENT PEAK LOAD  
SHAVING AT UCT MEDICAL SCHOOL**

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Thesis presented for the degree of Master of Science in Engineering. In the  
Department of Electrical Engineering University of Cape Town, March 2007

## **Declaration**

I know the meaning of plagiarism and declare that all of the work in the document, save for that which is properly acknowledged, is my own

signature removed  
Antonio.M.M.Cornelio

31 March 2007

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## Synopsis

This Master thesis investigates the application of Peak Load Shaving (PLS) at University of Cape Town Medical School (UCTMS). The purpose was to decrease the monthly maximum demand (MMD) in kVA such that UCTMS monthly electricity bill is decreased. It was purposed that implementing a three-phase inverter in conjunction with a lead-acid battery at UCTMS for PLS is technical and financial viable.

Five-year UCTMS MMD data history was gathered from UCT maintenance office as well as eight-month UCTMS load profile, which was gathered using the available electrical meter at Electrical Department Substation for Medical School at Falmouth Road.

Control strategies studies from previous works enabled the quickly synchronization of the three-phase inverter to a three-phase grid. It gave a good quality balanced control of the three-phase currents through the filter inductors, consequently gave a good quality control of the real and reactive power.

Secondly a PLS algorithm (PLSA) was developed, which had the aim of setting a threshold point (TP) to prevent the MMD supplied to UCTMS to surpass the TP. In addition, the PLSA in conjunction with designed controllers would charge the battery at unity power factor (PF), whenever the MD is below the set TP and discharge at the same PF conversely, hence limiting the MMD at the TP.

To test the purposed PLS topology, simplorer simulator was used, where two daily UCTMS load profile were simulated. The controls design and PLSA were implemented and the result showed that implementing PLS at UCTMS is technical viable. In practice, a prototype was built to show the synchronization of the three-phase inverter with three-phase grid by using a digital phase locked loop PI-based controller implemented in a DSP chip.

100kVA lead-acid battery system with 12-year lifetime was sized using UCTMS load profile. The initial capital cost to install 100kVA PLS system was R1,353,000.00. With 2004 tariff structure, the MD yearly saving was R23,016.00. After investigating different scenarios, it was concluded that the project would be financially viable at demand charge of R142.36 or higher and percentage increase of demand charge of 3.51%.

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## List of abbreviations

AC	Alternate Current
ADC	Analog-to-Digital Converter
BESS	Battery Energy Storage System
CSI	Current Source Inverter
CT	Current Transformer
CTM	Cape Town Municipality
DAC	Digital-to-Analogue Converter
DC	Direct Current
DG	Distributed Generation
DSM	Demand Side Management
DOD	Depth of discharge
DSP	Digital Signal Process
FES	Flywheel Energy Storage
FNB	First National Battery
IGBT	Insulated Gate Bipolar Transistor
MD	Maximum Demand
PF	Power Factor
PI	Proportional plus Integral
PLL	Phase-Locked Loop
PLS	Peak Load Shaving
rms	root mean square
SSM	Supply-Side Management
S/H	Sample-and-Hold
SMES	Superconducting Magnetic Energy Storage
SVPWM	Space Vector Pulse Width Modulation
UCTMS	University of Cape Town Medical School
VSI	Voltage Source Inverter
VT	Voltage Transformer
ZOH	Zero Order Hold

## List of Abbreviations

---

PV	Present Value
FV	Future Value
NPV	Net Present Value

## List of symbols

Symbol	Unit	Definition
$P$	[W]	Real power
$Q$	[Var]	Reactive power
$S$	[kVAr]	Apparent power
$p, q$	[W, Var]	setpoint for power calculator
$\delta$	[degree]	Power angle
$\theta$	[degree]	Theta, the three-phase grid phase angle
$\gamma$	[degree]	Gamma, the three-phase inverter phase angle
$X_{Link}$	[ $\Omega$ ]	Link inductor reactance
$V_{Conv}$	[V]	Converter Voltage
$V_{Grid}$	[V]	Grid Voltage
$V_a, V_b, V_c$	[V]	Three-phase phase grid voltage A, B, C
$V_\alpha, V_\beta$	[V]	Stationary orthogonal voltage, alpha and beta
$V_d, V_q$	[V]	Rotating orthogonal voltage.
$V_L$	[V]	Inductor Voltage
$V_{Conv\_abc}$	[V]	Inverter variable voltage representation for the three phases
$V_{Grid\_abc}$	[V]	Grid variable voltage representation for the three phases
$V_{L\_abc}$	[V]	Inductor variable voltage representation for the three phases
$i_{L_\alpha}, i_{L_\beta}$	[A]	Stationary orthogonal currents for the inductors filter
$I_d, I_q$	[A]	Rotating orthogonal current

$I_{L_d}, I_{L_q}$	[A]	Rotating orthogonal currents for the inductor filter
$g(s)$	[-]	Plant transfer function on s-plane
$k(s)$	[-]	Controller transfer function on s-plane
$q(s)$	[-]	Open loop transfer function on s-plane
$h(s)$	[-]	Zero order Hold transfer function on s-plane
$S(t)$	[-]	Signal on time domain
$g(z)$	[-]	Plant transfer function on z-domain
$k(z)$	[-]	Controller transfer function on -z-domain
$u(z)$	[-]	PI controller output signal on z-domain
$e(z)$	[-]	Error signal on z-domain
$y(z)$	[-]	plant output signal on z-domain.
$K_{p\_pll}$	[-]	Phase Locked Loop proportional gain
$K_{I\_pll}$	[-]	Phase Locked Loop integral gain
$K_I$	[-]	Plant, $g(s)$ , integral gain
$T_{pll}$	[s]	Phase Locked Loop PI controller sample time
$T_s$	[s]	System sample time
$\omega_c$	[rad]	Crossover frequency
$\alpha$	[-]	Normalizing factor
$k$	[-]	present value in discrete domain
$k+1$	[-]	next value in discrete domain
$z$	[-]	Symbol for z-plane
$u_k$	[-]	Present value of the PI output signal in discrete or digital form.
$u_{k-1}$	[-]	Previous value of the PI output signal in discrete or digital form.
$y_k$	[-]	Present value of the plant output signal in discrete or digital form.
$y_{k-1}$	[-]	Previous value of the plant output signal in discrete or digital form.
$e_k$	[-]	Present value of the error signal in discrete or

		digital form.
$e_{k-1}$	[-]	Previous value of the error signal in discrete or digital form.
$theta\_PLL\_diff$	[-]	Angle difference between the three-phase inverter and the three-phase grid in C code
$Fdbck\_PLL$	[-]	Feedback signal of the PLL in C code
$err\_k\_PLL$	[-]	Present error value representation in the C code
$err\_k1\_PLL$	[-]	Previous error value representation in the C code
$Setpoint\_PLL$	[-]	setpoint representation in C code
$U\_PLL$	[-]	Present PI output value representation of PLL in the C code
$U\_k1\_PLL$	[-]	Previous PI output value representation of PLL in the C code
$Y\_PLL$	[-]	Present integral output value representation of PLL in the C code
$Y\_k1\_PLL$	[-]	Previous integral output value representation of PLL in the C code
$S\_Source$	[VA]	Three-phase grid apparent power variable representation in Simplorer
$S\_Load$	[VA]	Three-phase load apparent power variable representation in Simplorer
$S\_conv\_dummy$	[VA]	Three-phase inverter apparent power dummy variable to change the inverter setpoint power in Simplorer
$Thresh\_new$	[VA]	the threshold value used in simplorer.

# 1 Introduction

## 1.1 Subject of This Thesis

The subject of this thesis is to investigate the application of Peak Load Shaving (PLS) technique to reduce the electricity bill at the University of Cape Town Medical School (UCTMS).

## 1.2 Background to the study

Electricity demand around the world has increased due to many reasons. In South Africa, rural electrification, commercial and industrial demand due to technological advancement, put a lot of stress on the supplier to increase generation capacity. In addition, new generation plants have to be commissioned to cater for the increased maximum demand (MD).

This action is called Supply-Side Management (SSM) [1]. The disadvantages of doing SSM are the following: Customers will continue to be ignorant of their usage of electricity, i.e. they would be using more electricity at peak time. Consequently, supplier has to spend huge amount of money to construct new generation plants or peak plants. Therefore, the peak plants would increase the MD charges seen by the customers.

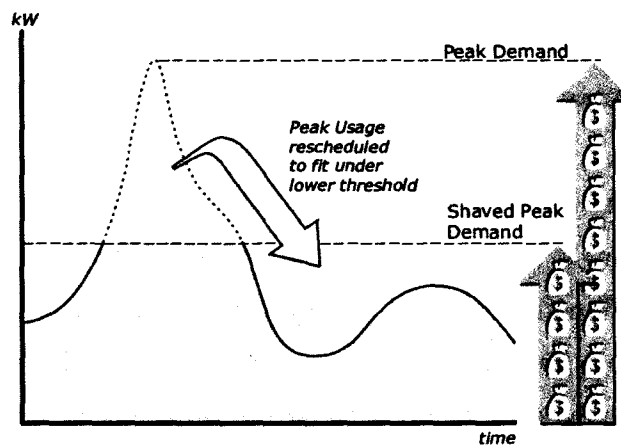
Many commercial and industrial consumers are charged by the public utilities on the MD either in watts [W] or [VA]. According to Eskom's definition, (Eskom is a South African national Electricity Supplier), MD is "*the highest demand measured in a billing month during the chargeable times periods specified for each specific tariff*" [2]. The reason behind it is to enable the public utilities to have enough money to be able to pay for the extra cost of maintaining the running of the peak substation [3]. The higher the MD or peak loads the more consumers causing this MD, must pay.

The UCTMS is such a consumer. They are charged by Cape Town municipality on the MD in kVA, as well as on the energy and service charges at the end of each month at specific tariff [4].

The process of managing the peak or energy consumption on the customer side, to ensure that the MD is below a set threshold and that the system reliability is always acceptable, is called Demand Side Management (DSM) [1]. Thus, DSM has an important role to play. According to the American Department of Energy, the definition of DSM is “actions taken on the customer’s side of the meter to change the amount or timing of energy consumption. Utility DSM programs offer a variety of measures that can reduce energy consumption and consumer energy expenses. Electricity DSM strategies have the goal of maximizing end-use efficiency to avoid or postpone the construction of new generating plants” [1].

In DSM, customers understand their demand usages during a day, a month or a year period. This helps them to manage it properly, thus avoiding paying the MD charges.

Figure 1.2-1 shows the savings that can be obtained by shaving a peak MD.



**Figure 1.2-1: Maximum demand shaved substantially to decrease the expense to the customer [5].**

Different PLS techniques can be used by consumers to avoid the higher peaks such as [5]: Load scheduling, generation and load shedding.

### 1.2.1 Load Scheduling

Load scheduling is a technique whereby customer loads that would cause the MD to exceed a set threshold are scheduled on different time of the day to prevent the MD from going above the set threshold. The information of load usage or timing is very essential for better implementation of this technique [5]. Figure 1.2.1-1 illustrates the load schedule scenario.

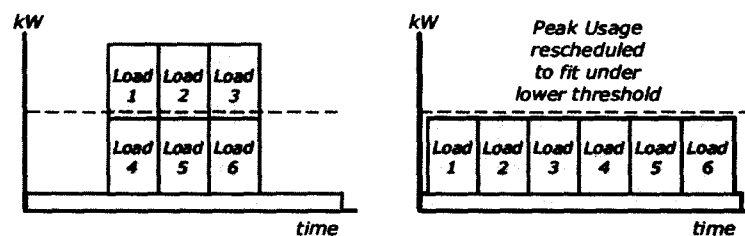


Figure 1.2.1-1: Peak shaving using the load schedule technique [5]

The most obvious advantage of load scheduling is that the load peak power never goes above the set threshold. Thus this means that the utility machinery would be protected against the overloading effect it would be under if the MD would go above the set threshold line.

This is prevented by customer load being carefully planned to be spread throughout different times of the day. In this way, the MD would not go above the set threshold, which means that the supplier would supply constant power throughout the day.

Consequently, money would be saved on the cost of repairing or replacing the damaged items in the unit under stress and on the peak substation, as well as on the customer bill.

Load Scheduling has a huge disadvantage on consumers where the load is continuously critical and the entire load must be on all the time. For instance in case of life support systems, hospitals and other equipment.

### **1.2.2 Generation**

In the generation technique, the customer would set up an onsite generator that would be ready to supply the available power to cater for the extra power needed. Although the customer might exceed the MD, the public utility would see the power demand by the customer as below the set threshold. To be able to implement this technique so that it can be cost effective, a financial feasibility study of the fuel of the generator against the cost of a higher demand charge would need to be done [5].

If well implemented the generation technique would be a win-win situation for both customers and supplier. For the supplier the set threshold would not be surpassed by the customers MD even though in reality it did surpassed. However, this additional demand would be supplied by the backup generator.

Customers MD would be met even though the supplier would not be able to supply it. It has huge advantages for customers, who have all their loads as critical. Therefore, there would be no need to shed or schedule any load, as it would be on every time it would be needed because of the generation.

If the financial feasibility study of the generator fuel versus the cost of MD charge is not well implemented more expense will occur than saving.

### **1.2.3 Load Shedding**

In load shedding, non-critical loads are the first to be disconnected whenever the MD is about to reach the set threshold. Figure 1.2.3-1 illustrates the scenario [5].

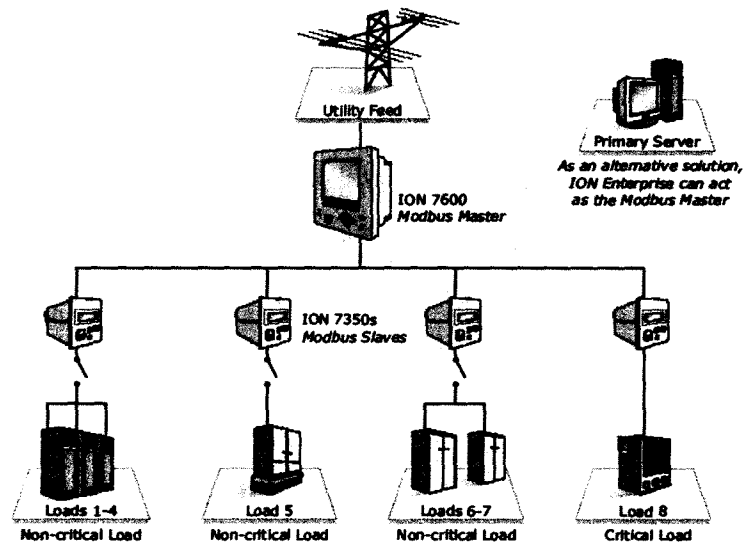


Figure 1.2.3-1: non-critical load being disconnected when maximum demand is reached [5]

This procedure would enable customer critical load to be on continuously, which would increase customer site operation and reliability as well as public utility operation reliability. In addition, blackouts would be prevented.

The disadvantage of load shedding technique is that, it cannot be implemented in the customer site that has the entire load as critical.

### 1.2.4 University of Cape Town Medical School

University of Cape Town medical school (UCTMS) uses three substations and two individual transformers situated at specific buildings. They are all used to supply UCTMS loads. These substations and the individual transformers receive their power from the Cape Town Municipality supplier at a specific point at 11kV bus bar and step it down to 380V to supply the loads. This point is called the Electrical Department Substation for Medical School at Falmouth road (it will be discussed in detail in section 2.1). It is at this point that the tariffs charges are applied by the municipality.

The substations names are:

- Wolfsen Pavilion Substation, it has a total capacity of 1MVA.

In this substation, there is a plan to install a new transformer with a total capacity of 1MVA. This will add to a total capacity of 2MVA.

- Werner & Beit (North) Substation, it has a total capacity of 0.8MVA.
- Anatomy building Substation, it has a total capacity of 1MVA.
- The individual transformers, one is located at Barnard Fuller building, with total capacity of 0.5MVA and the other is situated at Chris Barnard building, with total capacity of 1MVA.

The combined capacity of all the substations and the individual transformers as well as the proposed future transformer at Wolfsen Pavilion Substation adds to 5.3MVA. From reference [4], UCTMS was considered as a Very Large Power User. The tariff charges were allocated, as it will be shown in table 2.4-1 in section 2-4 [4].

From the interview with the Facility Project Engineer Manager responsible for UCTMS energy supply, Chris Briers, it was discovered that the municipality had agreed once off at beginning of the contract on a maximum threshold of 2.5MVA. Moreover, he added that all loads supplied by the electrical department substation for UCTMS at Falmouth road are critical. Table 1.2.4-1 shows MD history of UCTMS from 2000 to 2005 and figure 1.2.4-1 focus only in the year 2000 and 2005 data, to illustrate the MD increasing from 2000 to 2005.

Table 1.2.4-1: 6 year MD history for UCTMS

1752	1602	1737	1725	1896	2046
1700	1773	1956	1935	1873	2070
1680	1752	1935	1860	1873	2127
1512	1563	1623	1689	1716	1977
1224	1509	1605	1665	1632	1818
1422	1485	1602	1746	1640	1953
1575	1557	1436	1686	1650	1833
1488	1590	1662	1749	1899	1995
1473	1550	1518	1668	1731	2004
1494	1503	1560	1776	1785	2037
1575	1656	1569	1701	1950	1941
1476	1485	1665	1668	1839	1911

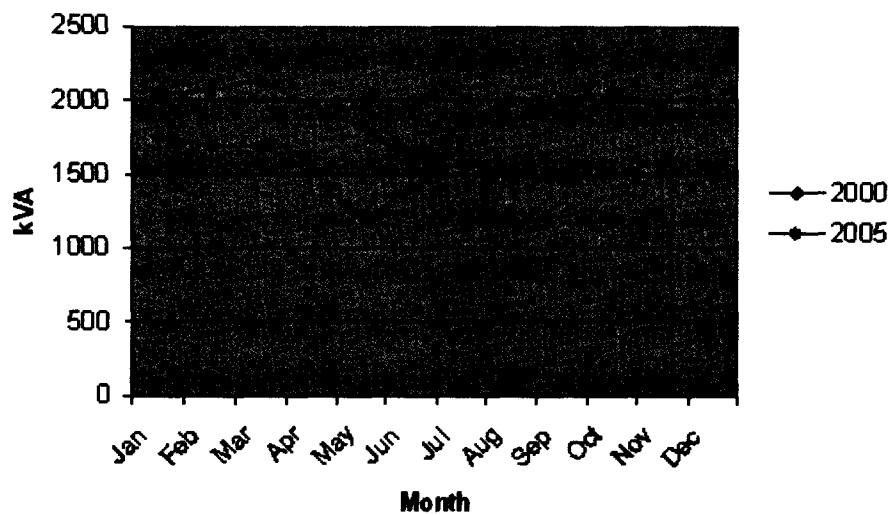


Figure 1.2.4-1: 2000 and 2005 load profile for UCTMS

Table 1.2.4-1 MD values were recorded using the monthly bill received by the UCT maintenance office. Analyzing table 1.2.4-1 it was understood that the MD in the five years illustrated occurred on the following months:

- January 2000, MD was 1.75MVA
- February 2001, MD was 1.77MVA
- February 2002, MD was 1.96MVA

- February 2003, MD was 1.94MVA,
- November 2004, MD was 1.95MVA,
- March 2005, MD was 2.13MVA.

The MD of UCTMS has been increasing for the past five years. Maybe three or five years from now the consumption might reach or exceed the set threshold of 2.5MVA.

Comparing the total power capacity of UCTMS with the set threshold, one can notice that not all transformers are working close to their maximum capacity and maybe never will, unless the CTM set a new threshold in this case above 5.3MVA. If this happens, it will mean that the UCTMS MD charge will increase by 53% above the current threshold.

A load problem was evident from recent events in the city of Cape Town, whereby the incident of the Koeberg nuclear power station (at beginning of 2006); meant that one unit was out of service due to negligence in the maintenance. The incident left the city of Cape Town grasping for air to avoid major blackouts. There was a shortage of 965MVA [6], which meant that the city was reaching the maximum capacity of the remaining unit. Eskom came up with the following different strategies to avoid a major blackout:

- Load shedding
- Decreasing the percentage of MD by running a program of changing the customer ordinary lamps of 45, 60 and 100W (DSM), with the new energy saver lamps, which draw less power but emit a reasonable amount of light. For example, a new energy saver lamp of 14W has the capacity of delivering light as the ordinary 100W lamp.
- Awareness campaigns, urging consumers around the city to use energy wisely during peak hours to avoid unnecessary load shedding.

Nevertheless, from the interview conducted with Chris Briers, it was confirmed that the transformers were not working hard, which meant that the huge investment on the transformers (R150000 for the 1MVA, which is R150/kVA) are not being paid off, reason being that the price of the transformer is directly proportional to its total capacity.

From the above discussion, it is clear that load scheduling and shedding is not an option for UCTMS, which leaves us with only generation technique, in other word an onsite generator.

There are different ways to accomplish the generation technique to decrease MD, which are:

- Onsite diesel generator or,
- Renewable source of energy such: solar, wind or water energy
- Peak Load Shaving storage systems.

For this thesis, PLS storage systems will be the focus of the investigation. The idea would be to use the battery to store energy from the grid at low values of MD below the chosen threshold line and then release back the stored energy to the grid at peak power above the set threshold line [5].

### **1.3 Hypothesis to be tested**

The hypothesis for this research is that using a lead-acid battery and three-phase inverter for PLS of the electricity supply at the UCTMS is technically and financially viable.

### **1.4 Objectives**

To test this hypothesis the following objectives should be accomplished:

- Collect and analyze UCTMS load profile data to identify possible PLS installation.
- Review and implement the most appropriate control design using a three-phase inverter in conjunction with battery storage synchronized with a three-phase source.
- Simulate the designed topology in simplorer package, such that PLS at UCTMS can be accomplished.

- Build a prototype to test the simulated results practically in the lab.
- Do a financial analysis of the project, and check its viability being implemented at UCTMS

## 1.5 Limitations

This project encountered several limitations such as:

- Simulation package license for simplorer V7 full version expired before the completion of the project, which prevented several test to be done for the phase locked loop control, current control and peak shaving algorithm in the three-phase inverter topology, see figure 4.7-1.
- Thus, the PLS simulation was tested only at University of Cape Town load profile at steady state condition as discussed in chapter 4.
- Simplorer student version packaged, which is a free student edition, has limited number of component to be used in simulation. Thus, the topology of figure 4.7-1 could not be implemented in student version.
- Because of the time, only the phase locked loop control was implemented in practice.

## **2 Sizing a Three-phase Inverter and Battery system for Peak Load Shaving for University of Cape Town Medical School**

As discussed on chapter 1 section 1.2.4, the UCTMS has all their loads as critical, which meant that the only possible PLS technique to be used was the generation technique. This chapter will start by looking into UCTMS substations schematic described in section 2.1. It will follow then with the description of the type of loads that those substations supply, discussed in section 2.2. Then in depth analysis, in the produced load profile will be done in section 2.3. Section 2.4 will use the result of section 2.3 to size the lead acid battery.

### **2.1 Electrical Department Substation for Medical School at Falmouth Road**

There are two feeders coming out from the Electrical Department Substation for Medical School at Falmouth Road, which are Wolfesen Pavilion and Anatomy Block. The transformers in all substations are connected as  $\Delta$  in the high voltage side and as Y in the low voltage side. According to Sen, [7]  $\Delta$ -Y transformers are commonly used to step up the voltage. In this case however, it was used to step down the voltage because a neutral point was needed in the low side of the three-phase transformer. Figure 2.1-1 illustrates the UCTMS schematic.

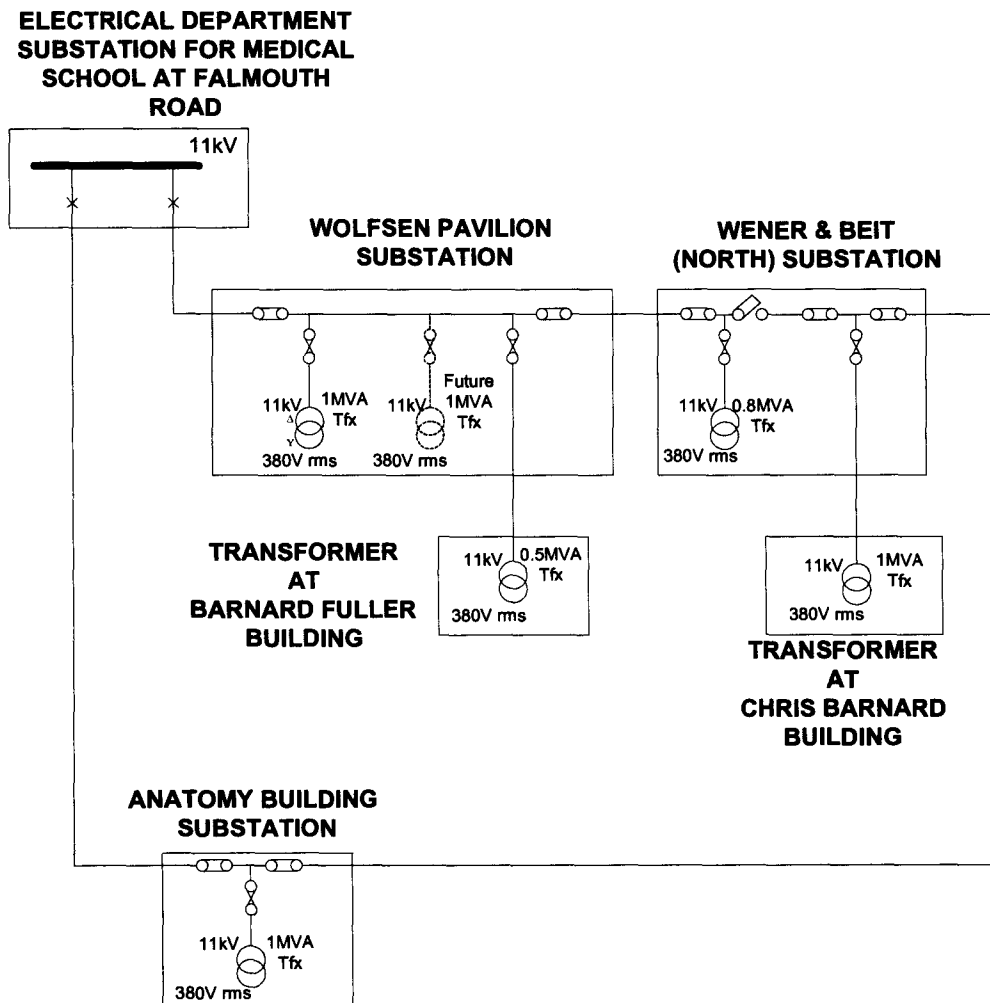


Figure 2.1-1: Schematic of the electrical department substation for medical school at Falmouth road

**The Wolfsen Pavilion feeder feeds the following substations:**

- *Wolfsen Pavilion Substation*

There is one active transformer with the following rated values: 1MVA 11kV/380V rms LL. There was a plan to put one additional transformer with the same capacity of the former one, as discussed in chapter 1 section 1.2.4, which now is active.

- *Transformer at Barnard Fuller Building (it is fed through the Wolfsen Pavilion Substation)*

There is one transformer with following rate: 0.5MVA 11kV/380V rms LL.

- *Werner & Beit (North) Substation*

There is one transformer with following rate: 0.8MVA 11kV/380V rms LL.

**The Anatomy Block feeder feeds the followings transformers:**

- *Anatomy building Substation*

There is one transformer with following rate: 1MVA 11kV/380V rms LL

- *Transformer at Chris Barnard Building (it is fed through Werner & Beit (North) Substation)*

This transformer has the following rate: 1MVA 11kV/380 rms LL

## **2.2 University of Cape Town Medical School Load**

From the interviews with Chris Briers, it was said that the entire loads are all critical, which meant that they must be on continuously. The types of load used at UCTMS in the different substations are briefly discussed as was mentioned by Briers:

- The Wolfsen pavilion substation supplies energy to animal houses,
- Wener & Beit (North) substation supplies energy to deep fridges,
- The transformer at Chris Barnard building supplies energy in the animal houses, air conditioner and deep fridge,
- The Anatomy building substation supplies energy to the air conditioner.

Given the critical nature of the UCTMS load, the most suitable PLS technique that could be used to decrease the MD as discussed in section 1-2-4, was the generation technique. The proposed technique falls well in this category, whereby a three-phase inverter will charge a battery at off-peak or rather below a set threshold and then release the energy back to the grid at peak time or above the set threshold by discharging the battery, the latter action will decrease the MD.

With this proposed solution, there would not be a need to disconnect none of the UCTMS critical loads at peak time. However, the most important aspect to look into is the capacity of the generator or of the battery. Similarly to the generator technique the capacity of the battery is the fuel of the three-phase inverter system.

The greater the battery energy capacity, the longer time the system can supply the energy. However, it also means the bigger and more expensive the battery would be. Therefore, a careful analysis at the customer load profile is very essential to ensure a proper sizing of the battery system and inverter.

### **2.3 University of Cape Town Medical School data analysis**

As was discussed in section 1.2 about DSM, it was important to understand the customer's consumption to implement a financial viable system that would decrease the MD effectively.

Thus, an electrical monitoring system, such as the one that was used in accessing data for this project was an essential part. It enabled the gathering of all the relevant information, such as load profile and power factor (PF) [5].

Eight months of data (from November 2004 to June 2005) were gathered with help of Mr. Edsel Ford, the senior professional officer for bulk metering operation in the city of Cape Town South Africa.

The place of data collection was at Electrical Department Substation for Medical School at Falmouth Road. As was discussed in section 2-1 that point was the entrance point, which supplies the entire UCTMS substations.

The metering system used was able to calculate the following:

- Current average demand +A in line 1, in kW
- Current average demand +A in line 3, in kW

- Current average demand +A, in kW. This value is the three-phase power of UCTMS. In addition it is the summation of line 1 and line 2
- Current average demand +Ri, in kVar. This value is the three-phase lagging reactive power drawn by UCTMS,
- Current average demand +VA, in kVA. This value is the three-phase apparent power drawn by UCTMS

Figure 2.3-1 shows the eight-month period load profile for UCTMS.

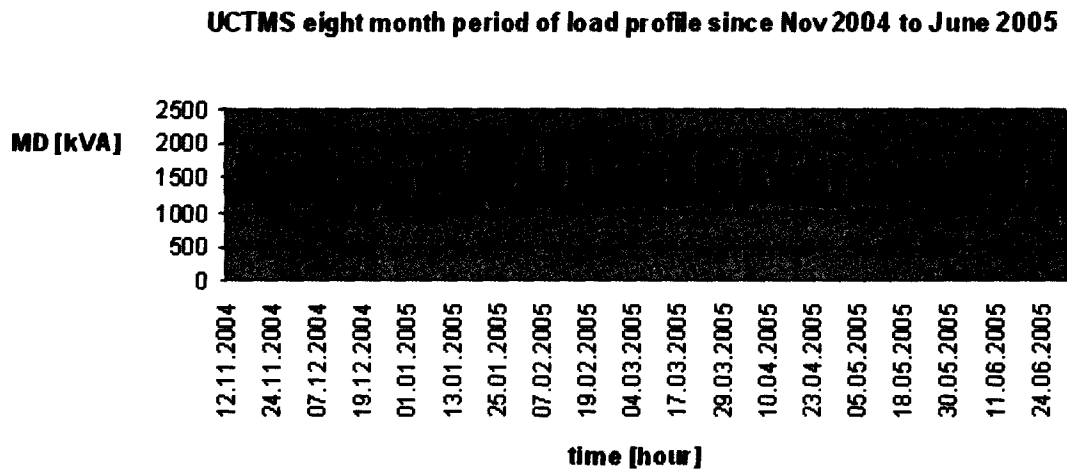


Figure 2.3-1: UCTMS eight month period of load profile

For the purpose of the thesis the load profile analysis was done only in one month, the chosen month was December 2004. Figure 2.3-2 shows December load profile.

Table 1.2.4-1: 6 year MD history for UCTMS

METER No. 677642						
	kVa	kVa	kVa	kVa	kVa	kVa
	2000	2001	2002	2003	2004	2005
Jan	1752	1602	1737	1725	1896	2046
Feb	1700	1773	1956	1935	1873	2070
Mar	1680	1752	1935	1860	1873	2127
Apr	1512	1563	1623	1689	1716	1977
May	1224	1509	1605	1665	1632	1818
Jun	1422	1485	1602	1746	1640	1953
Jul	1575	1557	1436	1686	1650	1833
Aug	1488	1590	1662	1749	1899	1995
Sep	1473	1550	1518	1668	1731	2004
Oct	1494	1503	1560	1776	1785	2037
Nov	1575	1656	1569	1701	1950	1941
Dec	1476	1485	1665	1668	1839	1911

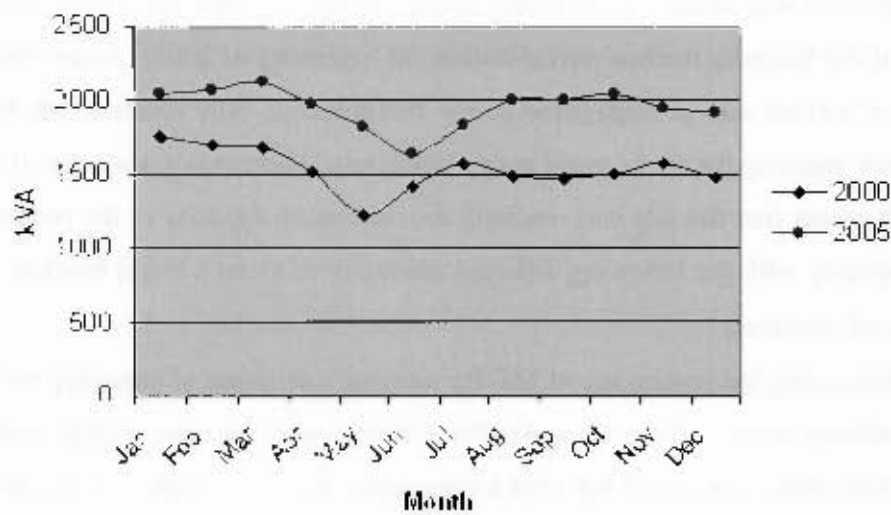


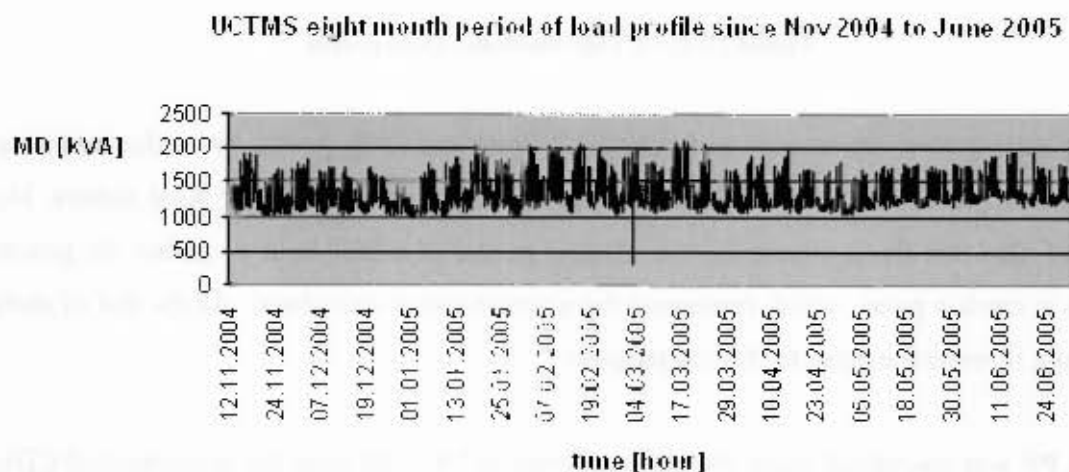
Figure 1.2.4-1: 2000 and 2005 load profile for UCTMS

Table 1.2.4-1 MD values were recorded using the monthly bill received by the UCT maintenance office. Analyzing table 1.2.4-1 it was understood that the MD in the five years illustrated occurred on the following months:

- January 2000, MD was 1.75MVA
- February 2001, MD was 1.77MVA
- February 2002, MD was 1.96MVA

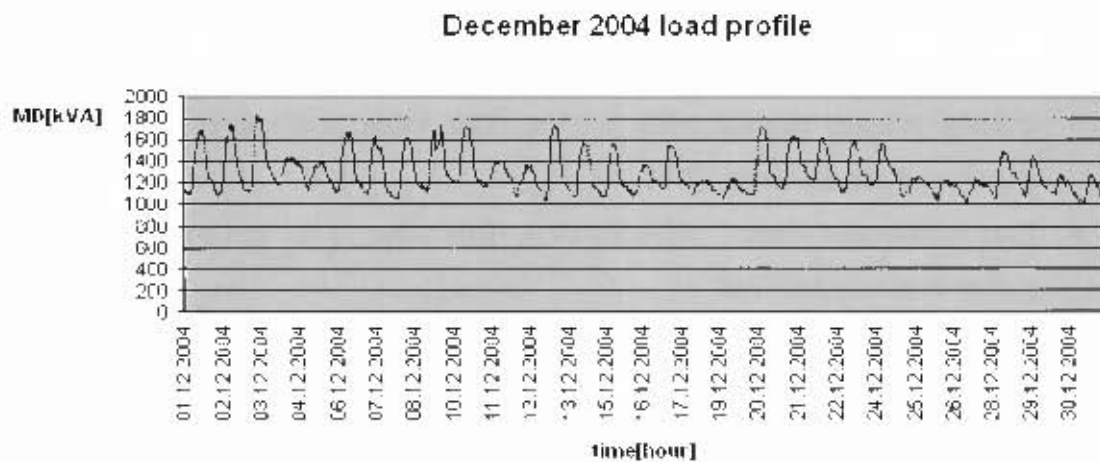
- Current average demand  $+P_A$ , in kW. This value is the three-phase power of UCTMS. In addition it is the summation of line 1 and line 2
- Current average demand  $+R_i$ , in kVar. This value is the three-phase lagging reactive power drawn by UCTMS,
- Current average demand  $-VA$ , in kVA. This value is the three-phase apparent power drawn by UCTMS

Figure 2.3-1 shows the eight-month period load profile for UCTMS.



**Figure 2.3-1: UCTMS eight month period of load profile**

For the purpose of the thesis the load profile analysis was done only in one month, the chosen month was December 2004, Figure 2.3-2 shows December load profile.



**Figure 2.3-2: UCTMS December Load profile**

Each peak power represented in figure 2.3-2 illustrates daily peaks. From the interview held with Edsel Ford, it was found out that UCTMS uses the Elster Kent meters. He added also that those meters have a window period of a half hour to gather the power then it sends a pulse, which represents the average power calculated. At the end of each month, it resets the pulse for billing purpose.

The PF was calculated using the data gathered at UCTMS (see the accompanied CD); equation (2.3-1) was used to accomplish this.

$$P = S \cdot \text{Cos}(\theta) \quad (2.3-1)$$

Where  $\text{Cos}(\theta)$  equal to PF. It can be seen that the customer draws the peak power at a low load PF. The average PF for the month of December was calculated to be 0.83. Figure 2.3-2 shows that the MD occurred on the third day. The MD obtained for the month of December was 1.84MVA.

The CFM charges UCTMS on the peak apparent power or total capacity power. As already mentioned UCTMS is considered as a very large power user [4]. The tariffs used are shown in table 2.3-1 [4].

Table 2.3-1: Electricity tariffs for commercial consumers [4]

VERY LARGE POWER USERS		2003/04	2004/05	Increase %
Service Charge - (monthly)	R per month	R45, 900.00	See Note	
Service Charge - (daily)	R per day	R1, 509.04	R1, 561.86	3.50%
Energy charge - (daily)	c/kWh	12.72	13.17	3.54%
Demand charge	R/kVA	R18.53	R19.18	3.51%

**Note:**

All figures exclude VAT

Monthly Service Charges calculated as Daily Service Charge multiplied by number of days in billing period

From table 2.3-1 it can be seen that savings can be achieved in demand charge by limiting the CTM peak power to the set threshold. This means that the peak shaving technique that this thesis is proposing to implement will have to supply the peak MD power in kVA. To ensure that the CTM peak power in kVA would decreased optimally.

Therefore assuming a 100kVA and 200kVA three-phase inverter for analysis, then the total capacity in kVA that the CTM would supply to UCTMS would drop from *1.84MVA* to *1.74MVA* and *1.64MVA* respectively.

In addition, the percentage shaved would be 5.4% and 10.9% for the 100kVA and 200kVA three-phase inverter respectively. However, to decrease the peak power in kVA is not as simple as it seems because the peak power is composed of the real and reactive power as shown in the equation (2.3-2).

$$S = P + jQ \quad (2.3-2)$$

Where  $S$  is the apparent power in [kVA],  $P$  is the real power in [kW] and  $Q$  is the reactive power in [kVar].

Graphically equation 2.3-2 is represented as show in figure 2.3-3.

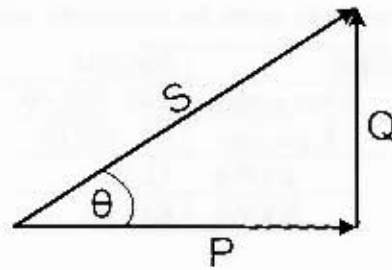


Figure 2.3-3: Graphical representation of Apparent, real and reactive power

Therefore to decrease  $S$  from 1.84MVA to 1.74MVA or 1.64MVA, there is a need to decrease  $P$  and  $Q$  such that  $S$  would be decreased optimally.

### 2.3.1 Optimum Peak Load Shaving for UCTMS

As was pointed out from the previous section the apparent power,  $S$ , is the parameter that should be decreased at the CTM, in this way the peak shaving would be done optimally. Ideally,  $S$  should be drawn by the load at unity PF. However, many of the loads are made of induction motors, which draw power at PF less than unity or lagging PF [7]. This is the case for the loads at UCTMS.

The circle in figure 2.3.1-1 represents the ideal scenario that the CTM would want to have for the total capacity drawn by the load. Because in the scenario the PF is unity, i.e.,  $\theta$  is zero, which would mean from equation 2.3-1 that the CTM would only deliver the real power demanded by the consumer.

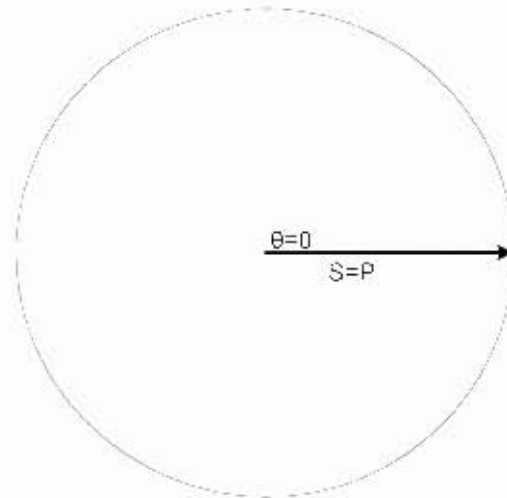


Figure 2.3.1-1: Apparent power at unity power factor

However, the power triangle that UCTMS has is shown in figure 2.3-3 and 2.3.1-2

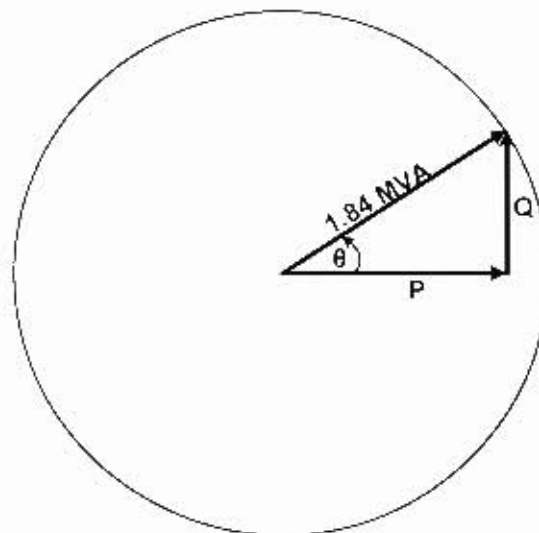


Figure 2.3.1-2: Total capacity drawn by UCTMS load on day 3

Recalling that the average PF of customer for the month of December was 0.83 and assuming it to be constant for simplicity, therefore the real and reactive power flow was calculated to be  $P=1.53\text{MW}$  and  $Q=1.03\text{Mvar}$ .

Three scenarios will be discussed to illustrate the optimum PLS that must be implemented at UCTMS. Scenario 1 will look into the case of only supplying real power from the inverter. Scenario 2 in another hand will analyze the effect of only doing PF correction, i.e., delivering reactive power only, and finally scenario 3 will analyze the effect of supplying the apparent power from the inverter at the same PF as the CTM, which mean that the three-phase inverter would supply both real and reactive power.

a) **Scenario 1: Only real power delivered from the inverter.**

Assuming the use of the three-phase inverters at unity PF, the inverter in conjunction with the battery system would supply only the real power. The 100kVA and 200kVA inverter would supply 100kW and 200kW respectively if the respective battery system were sized to supply 100kW and 200kW for the required time. This in turn would decrease CTM real power from  $1.53MW$  to  $1.43MW$  and  $1.33MW$  respectively.

The reactive power supplied from CTM to UCTM would remain the same. Thus, the total system capacity  $S$  would be  $1.76MVA$  and  $1.68MVA$  for the 100kVA and 200kVA inverter respectively. The new  $S$  is calculated using the equation (2.3.1-1) and it is illustrated graphically in figure 2.3.1-3 for the 100kVA three-phase inverter in the left and 200kVA three-phase inverter in the right.

$$S = \sqrt{P^2 + Q^2} \quad (2.3.1-1)$$

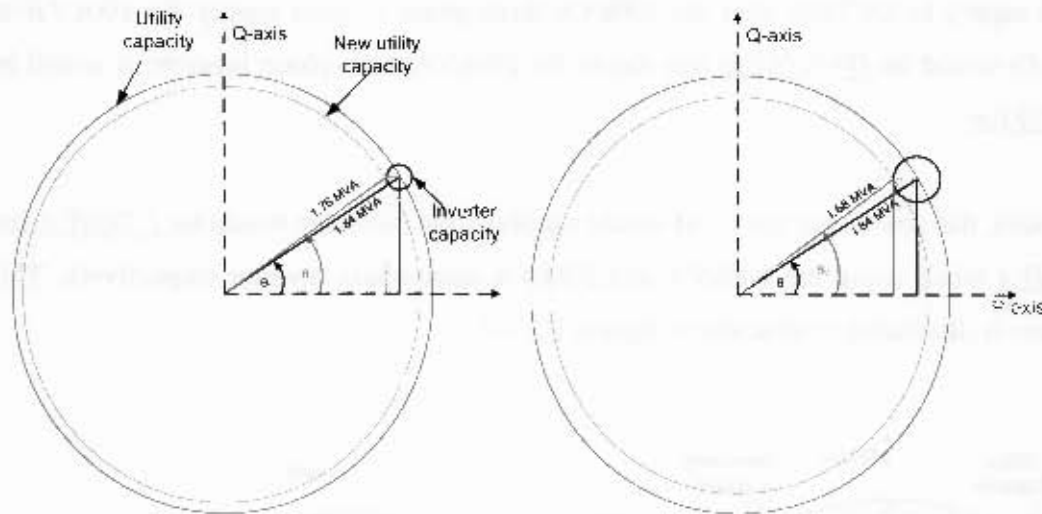


Figure 2.3.1-3: New system capacity for UCTMS after supplying power from 100kVA and 200kVA 3-phase inverter at unity PF respectively.

From figure 2.3.1-3, one can see that by supplying only real power the PF gets worse. This can be confirmed mathematically using equation (2.3.1-2).

$$PF = \text{Cos}(\text{Tan}^{-1} \frac{Q}{P}) \quad (2.3.1-2)$$

Table 2.3.1 1 illustrates the new PF the CTM would have if 100kW and 200kW were supplied by the 100kVA and 200kVA three-phase inverter respectively.

Table 2.3.1-1: New public utility power factor after using the three-phase inverters at unity PF

	CTM PF	CTM PF after the 100kVA three-phase inverter supplies 100kW	CTM PF after the 100kVA three-phase inverter supplies 200kW
PF	0.83	0.81	0.79

**b) Scenerai02: Only reactive power delivered from the inverter.**

Assuming that the three-phase inverters supplies only reactive power to CTMS, then this mean that it was performing PF correction only. The new reactive power that CTM

would supply to UCTMS after the 100kVA three-phase inverter supply the 100kVar to UCTMS would be  $Q=930kVar$  and due to the 200kVA three-phase inverter, it would be  $Q=830kVar$ .

Therefore, the new  $S$  that the CTM would supply to the customer would be  $1.79MVA$  and  $1.74MVA$  while using the 100kVA and 200kVA three-phase inverter respectively. This scenario is illustrated graphically in figures 2.3.1-4

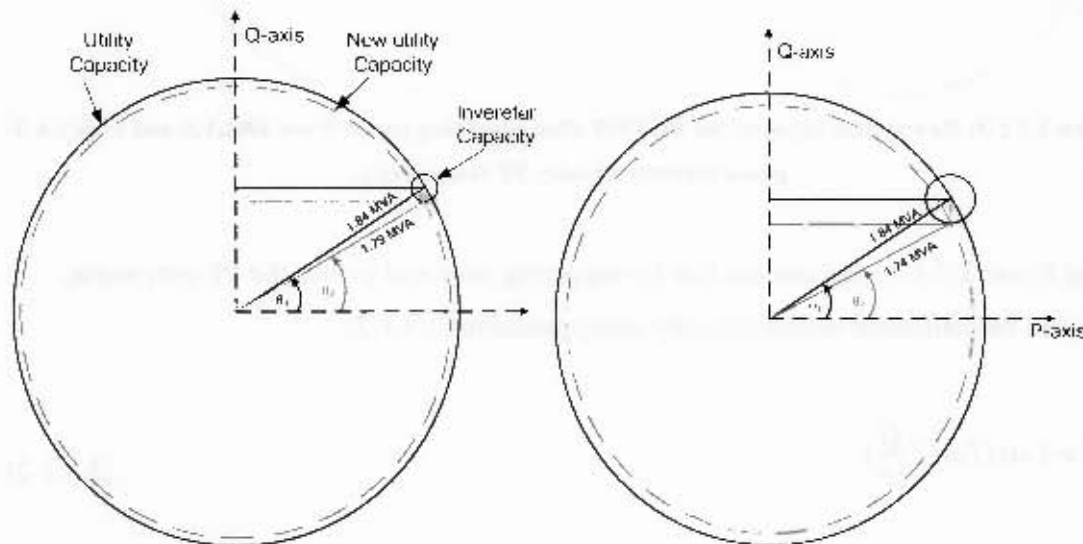


Figure 2.3.1-4: New system capacity for UCTMS after supplying power from 100kVA and 200kVA three-phase inverter at zero PF respectively

The new system PF after using the 100kVA and 200kVA three-phase inverter as PF correction would be as shown in table 2.3.1-2.

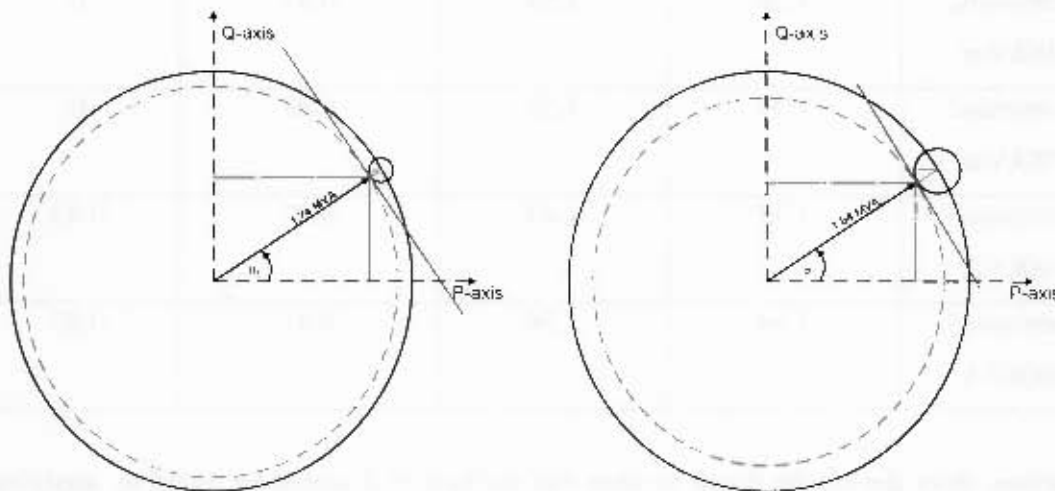
Table 2.3.1-2: New public utility power factor after using the three-phase inverters as PF correction unit

	CTM PF	CTM PF after the 100kVA three-phase inverter supplies 100kVar	CTM PF after the 200kVA three-phase inverter supplies 200kVar
PF	0.83	0.85	0.88

c) **Scenario3: Combination of real and reactive power delivered from the inverter.**

The third scenario was the possibility of finding the best point where CTM peak power in kVA could be decreased to a minimum value by using the three-phase inverter. Analyzing figure 2.3.1-3 and figure 2.3.1-4 there is a point on the three-phase inverter circle that would give the minimum CTM peak power.

This point was where the three-phase inverter circle and the CTM new circle meet in a tangent. Practically, this would be only possible if the three-phase inverter would supply  $S$  at the same PF as the CTM. Thus, the new CTM capacities,  $S$ , when using the third scenario for the 100kVA and 200kVA three-phase inverter would be 1.74MVA and 1.64MVA respectively. Figure 2.3.1-5 shows the scenario.



**Figure 2.3.1-5: New system capacity for UCTMS for the best peak shaving due to 100kVA and 200kVA three-phase inverter respectively**

Table 2.3.1-3 illustrates the response of each of the scenario in relation with CTM supplying UCTMS without the three-phase inverter.

**Table 2.3.1-3: Table to illustrate the different scenarios of PLS to be able to choose the optimum peak shaving for UCTMS**

	<b>Apparent Power [MVA]</b>	<b>Real Power [MW]</b>	<b>Reactive Power [MVar]</b>	<b>PF</b>
Cape Town municipality without the three-phase inverter	1.84	1.53	1.03	0.83
Sceneraio1 100kW	1.76	1.43	1.03	1
Sceneraio1 200kW	1.68	1.33	1.03	1
Sceneraio2 100kVar	1.79	1.53	0.93	0
Sceneraio2 200kVar	1.74	1.53	0.83	0
Sceneraio3 100kVA	1.74	1.44	0.97	0.83
Sceneraio3 200kVA	1.64	1.36	0.91	0.83

Therefore, from the results it can be seen that the best PLS would be found by applying the third scenario. As discussed the three-phase inverter in this scenario would supply the apparent power at the same PF as CTM is supplying UCTMS. In this way the minimum MD that CTM would supply UCTMS would be achieved.

### **2.3.2 University of Cape Town Medical School monthly saving by using 100kVA or 200kVA three-phase inverter**

From tables 2.3-1 it could be seen that CTM charges UCTMS in three ways: service charge, energy charge and demand charge. The monthly bill that UCTMS has to pay CTM is composed of the summation of those charges. However, the only charge that would be affected when a three-phase inverter in conjunction with battery storage is used would be the demand charge.

The energy charge that CTM imposed on UCTMS would not be affected because the energy that the three-phase inverter in conjunction with battery storage would deliver to UCTMS at peak time, would be the same energy that UCTMS would buy from CTM at off-peak time or below the threshold point, to store or charge the battery. Thus the energy that CTM supply UCTMS at peak time would merely be transferred to the off-peak time.

Once again, analyzing table 2.3-1 it was noticed that the demand charge in 2004 was R19.18/kVA. Continuing with the month of December analysis, the demand charge contribution in the December monthly bill was R35,272.02. It was calculated using equation (2.3.2-1).

$$\text{Monthly MD Charge} = \text{Monthly MD} \times \text{Demand Charge} \quad (2.3.2-1)$$

Where, *Monthly MD* is the maximum daily peak, which would occur within a month, the *Monthly MD Charge* is the charge that UCTMS must pay to CTM due to the daily MD in a month. The December *Monthly MD* was 1839kVA or 1.84MVA as illustrated in tables 1.2.4-1 and 2.3.1-3 respectively.

Moreover, using scenario 3 in table 2.3.1-3 and equation (2.3.2-1), the new *Monthly MD Charge* that UCTMS would pay to CTM would be R33,354.02 and R31,436.02 for the 100kVA and 200kVA three-phase inverter respectively.

Consequently, the monthly savings that UCTMS would make would be R1,918.00 and R3,836.00 respectively. Thus the yearly saving would be *R23,016.00* and *R46,032.00* by using the 100kVA and 200kVA three-phase inverter respectively in 2004.

It is evident that with 200kVA three-phase inverter the savings would be greater. In fact the bigger the three-phase inverter capacity, the greater the savings. Thus, the 200kVA three-phase inverter could be considered as the best choice for the design.

However, before considering the 200kVA three-phase inverter as the best choice, simply because it would result in greater savings, some points were considered, such as:

- UCTMS load profile curve should be analyzed to check for how long the shaving period would occur for the specific inverter in use.
- Then that would help to see the total energy that the battery storage would need to supply the required energy demanded at peak time.
- Recall that energy is equal to the product of the power and the time.
- The total energy at peak time or above the threshold point would help to size the battery capacity.
- In addition, the bigger the battery capacity, the more expensive it would be.

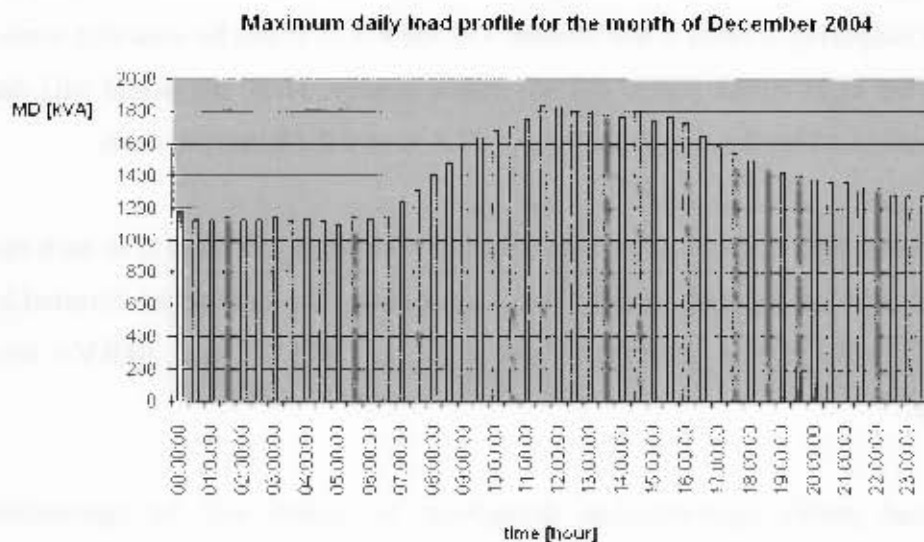
Thus from the above points, it was understood that, the choice of the right size of the three-phase inverter for UCTMS, depends on the shape of the UCTMS load profile curve as well the energy required at peak time i.e. the battery capacity. Therefore, the 100kVA and 200kVA will be used in the analysis to size the battery storage. The cheapest battery storage will be used in the financial analysis to check for financial viability.

### 2.3.3 Energy required to supply the UCT Medical School at peak time using the 100kVA and 200kVA Inverter.

In section 2.3, the data gathered by the metering system was discussed. Those data points were the important load measurements done by the metering system at half hour intervals for PLS analysis. Each signal gathered was averaged during this half hour period.

The measurement done by the metering system was undertaken at voltage level of 110V and maximum current flow of 5A, because the metering system uses voltage transformer (VT) of the following ratio 11000V/110V and current transformer (CT) of 150A/5A. All the measurements had to be transformed to the actual values at 11kV and 150A for analysis as seen on the bus bar feeder. This was accomplished by using the ratio of the VT and CT, which is 100 for VT and 30 for CT. By multiplying them, it yields 3000; this value is multiplied by each measured value to transform back to actual values on the high side of VT and CT.

Figure 2.3.3-1 illustrates the maximum daily load profile of UCTMS, which happen in the third day. Each strip represents half an hour “current average demand”.



**Figure 2.3.3-1: Maximum daily load profile for the month of December represented as half an hour strip**

The energy in one strip is the product of the peak of the strip and its width, the width period was a set to half an hour. Therefore the total energy would be the summation of the energy in each strip.

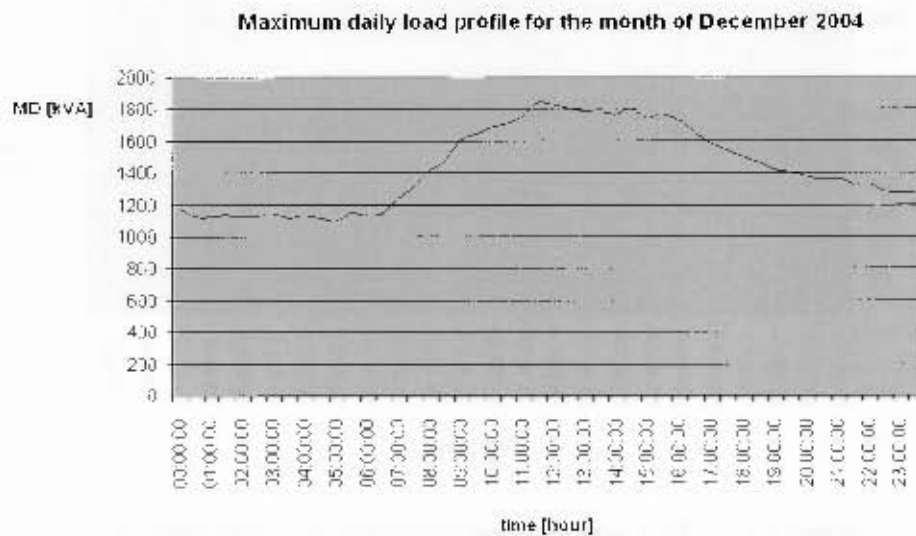
In addition, having the above argument in mind, the energy at peak time was calculated by summing the portion of the energy in each strip at peak time i.e. above the threshold line. Ideal monthly PLS throughout one month was assumed for simplicity.

Ideal monthly PLS would happen when the threshold point would be set at begin of each month in such way that the maximum peak within a month, would be the only peak power that the three-phase inverter would supply its full capacity in 30 minutes. The rest of time, the three-phase inverter would supply the required power in the range of zero and less its full capacity.

From the above discussion, the threshold for each relevant month throughout the eight months period was calculated using values from table 1.2.4-1. Table A-1 in appendix A shows the values of table 1.2.4-1 for the relevant eight months on column 2 as well as the actual data gathered from the metering system, which is represented in table A-1 in column 3. Comparing column 2 and column 3 of table A-1, it can be seen that some MD throughout the eight-month period did not match exactly. Thus, the actual MD data in column 3 were used for the energy analysis of PLS to size the battery system.

Using the actual data in table A-1 and subtracting 100kVA and 200kVA in each month, the ideal thresholds for each month were calculated. The calculated thresholds are illustrated in table A-2 in columns 3 and 4 for the 100kVA and 200kVA inverter respectively.

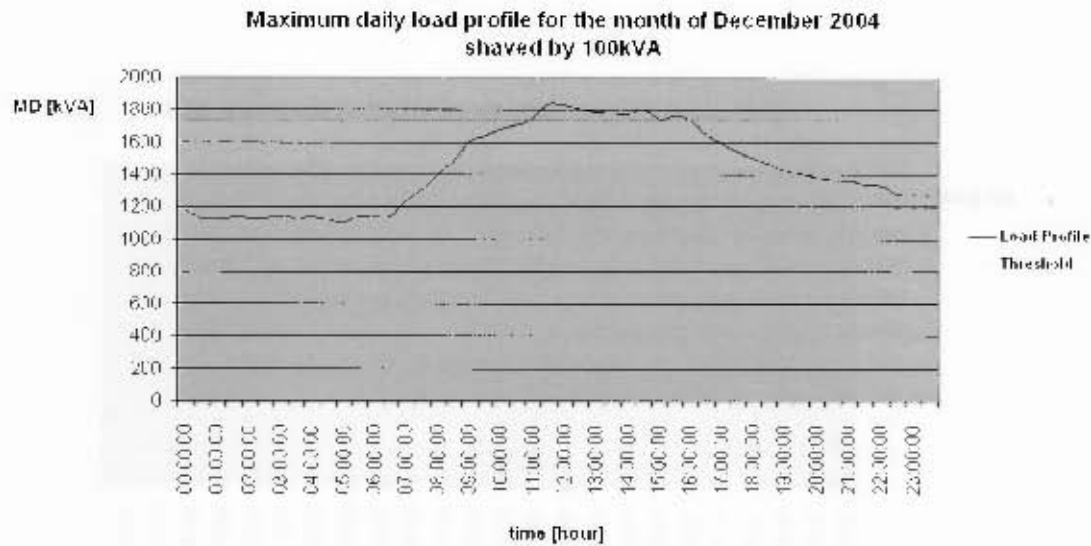
UCTMS load profile representation throughout the report will be represented as continuous line as illustrated in figure 2.3.3-2 for simplicity. Figure 2.3.3-2 illustrates the maximum daily load profile for the month of December.



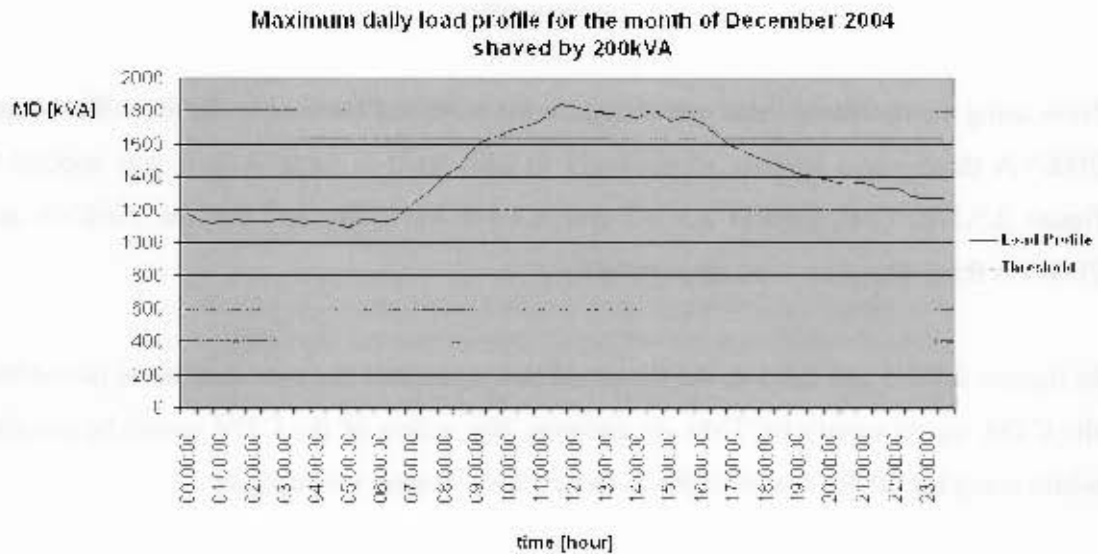
**Figure 2.3.3-2: Maximum daily load profile for the month of December for UCTMS represented as continuous line.**

Now using the threshold value calculated for the month of December for the 100kVA and 200kVA three-phase inverter respectively as illustrated in table A-2, it was applied to figure 2.3.3-2. Thus, figures 2.3.3-3 and 2.3.3-4 were obtained for the 100kVA and 200kVA three-phase inverter respectively.

In figures 2.3.3-3 and 2.3.3-4, the threshold line represents the new maximum power that the CTM would supply UCTMS. In addition, this action of the CTM would be possible while using the 100kVA and 200kVA three-phase inverter respectively.



**Figure 2.3.3-3: UCT medical school load profile shaved by 100kVA**



**Figure 2.3.3-4: UCT medical school load profile shaved by 200kVA**

Tables A-3 and A-4 shows the period where the load is above the threshold line as well as the three-phase inverter capacity needed to supply the power above the threshold line for the 100kVA and 200kVA respectively. Tables A-3 and A-4 also shows the inverter capacity in kVA, however to size the battery the real power in [kW] is need instead.

Therefore, tables A-5 and A-6 illustrates the real and reactive power that the three-phase inverters would supply at different PF above the threshold line as well as the period that load would be above the threshold line.

In keeping with the half an hourly measurement period, the energy in kWh supplied by the three-phase inverter for that period in each strips above the threshold line were added together. Thus, the total energy above the threshold line is presented in tables A-7 and A-8 for the third day for the 100kVA and 200kVA three-phase inverter respectively.

Analyzing table A-5 to A-8, it can be seen that for the third day of December the battery storage system would have to supply 209.81kWh for 5hour and 733.55 kWh for 7.5 hour, for the 100kVA and 200kVA three-phase inverter respectively. The same analysis as above was done for the other days throughout the eight months.

Table A-9 and A-10 shows the maximum daily energy that the battery storage would supply in each month and its duration for the 100kVA and 200kVA three-phase inverter respectively. As mentioned above the battery storage would have to be sized for the worst-case scenario. Therefore, from tables A-9 and A-10 the maximum energy in kWh and the maximum time duration was chosen to size the battery storage.

Tables A-11 and A-12 shows the maximum daily energy in the worst month, which happen to be in February, and present the maximum duration time when using 100kVA and 200kVA three-phase inverter respectively.

The purpose of this research was to use the three-phase inverter to supply the kVA power at the same PF as the three-phase source. Thus, ensuring that the best peak load shaving could be achieved as discussed previously in section 2.3.1.

However, to size the battery, a unity PF discharging was assumed to make sure that the battery would be sized to deliver the full inverter capacity in kW. This decision was taken

because it was noticed from the data gathered that the PF throughout the eight month period changed from 0.80 to 0.94.

Continuing with the analysis in the worst case scenario as discussed in tables A-11 and A-12, table A-13 illustrates the energy that the 100kVA three-phase inverter would supply if it had to deliver the power at same PF as the supplier.

Table A-14 however shows the maximum energy the 100kVA three-phase inverter would supply to the grid at unity PF. Similarly, table A-15 and A-16 presents the result for the 200kVA three-phase inverter using the same analyze used to calculate the values in table A-13 and table A-14.

Comparing the energy delivered by the three-phase inverters in table A-13 to table A-16 it is clear that it was wise to size the battery to deliver the full power at unity PF, which is the worst-case scenario. The focus of the analysis is now shifted to tables A-14 and A-16.

Now to make the analysis more realistic the three-phase inverter is assumed to deliver the power to the three-phase grid at efficiency of 90%. From tables A-14 and A-16 the average power that would be delivered by the 100kVA and 200kVA three-phase inverter are 75.56kW for 5.5hour and 142.73kW for 7.5hour respectively.

Thus at efficiency of 90% of the three-phase inverter, it would mean that the battery storages must supply average power of 83.96kW for 5.5hour and 158.59kW for 7.5 hour to the 100kVA and 200kVA three-phase inverter respectively.

## **2.4 Batteries Sizing**

### **2.4.1 Different energy storage**

The Battery Energy Storage Systems (BESS) are a type of energy storage device that store energy electrochemically. The other types of energy storage available are:

- Superconducting Magnetic Energy Storage (SMES) has the aim to store energy magnetically, when a dc current flows through a superconducting coil [8].
- Advanced Capacitors are a type of device that store electrical energy when positive or negative charges, are stored on their plates [8].
- Flywheel energy storage (FES) is a type of storage device that store electrical energy kinetically, when couple to an electrical machine [8].

In terms of fast response and high efficiency, the SMES is leading the energy storage devices with a charge-discharge efficiency of 95%. However, it is the most costly from them all [8]. The BESS compared to the others energy storage, are the most cost effective energy storage around and very easily accessible [8].

Looking deeper in the BESS technology, specifically the different batteries technology around. for example: the lead acid batteries, nickel-metal hydride batteries, nickel-cadmium batteries, and lithium-ion batteries, which according to the authors of reference [8], they were being investigated for large-scale energy storage application.

Important factors to consider when choosing a BESS for a storage application are the following: high energy density, high energy capability, round trip efficiency, cycling capability, life span and initial cost [8].

Lead-acid batteries has the lower energy density capability and limited life cycle compared with the rest discussed batteries, however it's lower cost and the easiness of being accessed for replacement as well as being already a stable technology, make them the first choice of many storage application [8].

Based in the above discussion the lead-acid battery was the choice for this thesis. The lead-acid battery used to do the financial feasibility study analysis was a battery manufactured by the First National Battery (FNB), which is a South Africa company, [9].

### 2.4.2 First National Battery Lead-Acid Batteries

Due to the nature of the project, which was PLS, it meant that the battery bank that must be used, has to be always ready or at standby mode whenever it is needed and also must be able to handle high cycling.

FNB has different range of batteries cell such as:

- FNB have batteries cells that can do high cycling, for instance the Raylite M-Solar or Tubular RSO [9].
- Batteries cells that can operate in a float mode or standby operation, for instance the Chloride Faure-x enclosed cells [9].
- Moreover, batteries cells that can do both high cycling and operating on standby mode, for instance the Raylite tubular cells RCT [9].

The FNB battery that was considered to be used for this project for the financial analysis, which would be able to do both high cycling and operating in a standby mode, was the Raylite tubular RCT.

#### 2.4.2.1 Raylite Tubular Cells

It was discussed that *"the tubular cell offers outstanding reliability over an expected working life of 10 to 12 years in float charge applications. These cells are capable of high cycling. It offers a greater surface area for a specific plate dimension, affording higher energy density."*[9].

From the interview with the technical services manager of First National Battery, Cliff Hardman, it was found out that the raylite tubular cells high cycling capability goes as low as 80% of depth of discharge (DOD). It was added that this is due to the amount of acid residing in the tubular cells, which it's quantity are high enough to allow for those high cycling.

The raylite tubular cells applications, design features, product and service benefits can be found in Raylite Tubular Cells datasheet, appendix B

Next section will discuss the charging scheme, which would enable the lead-acid battery to be at standby mode.

### **2.4.3 Multi-stage charging of a lead-acid battery**

Lead acid battery does not like to be left in discharge mode for long, because it would cause sulfation on the negative plate, however if it is overcharged, it would cause grid corrosion on the positive plates as well as the temperature would rise and gassing would happen. The gassing would result in venting, which mean that the electrolyte in the battery would evaporate .Consequently, the capacity as well as the lifetime of the battery would decrease [10]. Thus, it is important to fully charge the lead-acid battery and at same time avoiding overcharging.

To charge a lead-acid battery for this type of project, the worst-case scenario of charging the battery must be considered. The worst-case scenario would happen when the lead - acid battery has to be discharged daily and fully discharged i.e. 80%. Then this would mean that the battery bank would have to be charged between the daily duties or daily peaks.

The total available time to charge the battery when using the 100kVA and 200kVA three-phase inverter respectively as discussed in section 2.3.3 would be 18.5 hour and 16.5 hour respectively. However, from literature, it was discussed that for larger batteries capacity, such as the sealed lead-acid batteries the charging would last up to 36 hours when charging the battery at constant voltage limited only [10]. From reference [10], it was discussed that by using higher charge current and multi-stage charge methods the charge time can be decreased dramatically down to 10 hours or less.

The multi-stage charge for the lead-acid battery discussed in [10] has three stages. The first stage is known as constant current stage and last for 5 hours, in this stage the current is held at initial constant value while the voltage rises to a preset value, this preset value

is known as boost voltage and it can be in range of 2.3- 2.45V per cell. The correct settings of the boost voltage depend greatly in the temperature. When the voltage reaches its preset voltage, it was discussed that the battery is 70% fully charged [10]. At this point, the second stage is reached and is known as constant voltage.

For the battery to be 100% fully charged the preset voltage limit has to be held at that value while the current is reducing until it reaches 3% of its rated value. It was discussed that this stage would last for 5 hours, in addition it was mentioned that once the battery reaches the preset voltage it would be saturating [10].

However, it was affirmed that it is very important for the well-being of the battery for the voltage to be held at that constant preset voltage while the current is being decreased toward 3% of its rated value, this action would allow all battery cells to be fully charged [10].

At this point the last stage is reached. Now to prevent self-discharging the current is held at 3% of its rated current while the voltage would drop so that overcharge can be prevented, the float voltage would be set to 2.25V at temperature of 25° [10]. This last stage is known as float charge stage, it was discussed that the battery can stay at this stage forever without being damaged [10]. However, just like human beings, the battery ages, and that would limit its lifetime.

Figure 2.4.3-1 illustrates the lead-acid multi-stage charging [10].

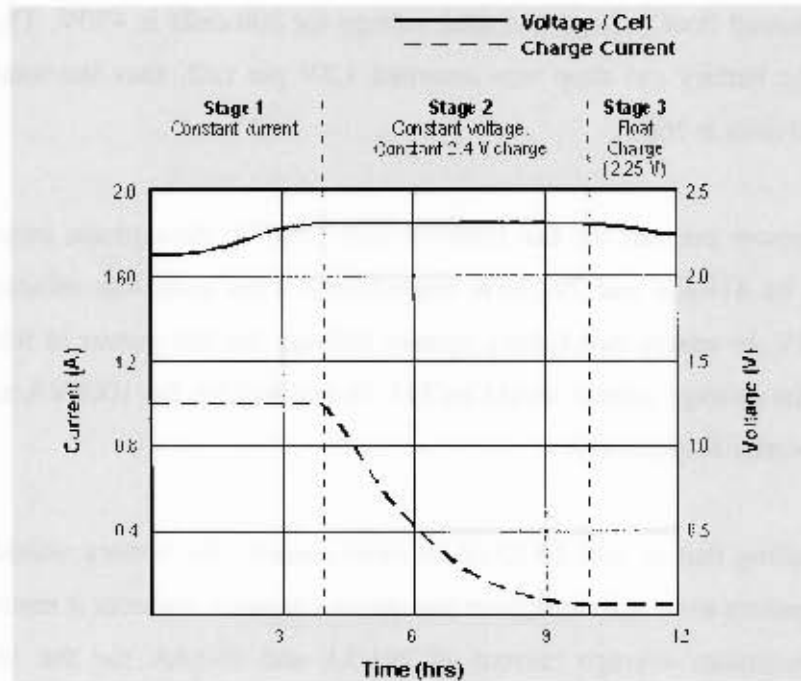


Figure 2.4.3-1: lead-acid battery multi-stage charging [10]

Therefore, the multi-stage charge discussed above is ideal for this project, because between heavy daily duties the battery would be able to be fully charge and stay in standby mode or float charge.

#### 2.4.4 Raylite battery Capacity Calculation

Recalling from section 2.3.3 that the 100kVA three-phase inverter battery system would supply an average power of 83.96kW for 5.5hour and the 200kVA three-phase inverter battery system would supply an average power of 158.59kW for 7.5 hour to the 100kVA and 200kVA three-phase inverter respectively.

Assuming a DC bus nominal voltage of 400V, thus with a nominal voltage per cell of 2 V then the number of cells would be 200 cells. Assuming a good ventilated room, the maximum boost voltage per cell can be set to 2.45V [10], which would give a total voltage of 490V for 200 cells.

Using the discussed float voltage, the total voltage for 200 cells is 450V. The minimum voltage that the battery can drop was assumed 1.8V per cell, thus the total minimum voltage for 200 cells is 360V.

The average power per cell for the 100kVA and 200kVA three-phase inverter battery system would be 419.8W and 792.95W respectively. Thus using the minimum voltage per cell of 1.8V, to ensure that battery system delivers the full power at this minimum voltage, thus the average current would be 233.2A and 440.5A for 100kVA and 200kVA three-phase inverter respectively.

However, recalling that at 80% DOD of its rated capacity the battery would be empty. Then for the battery to be able to deliver the above discussed currents it must be rated to deliver the maximum average current of 291.5A and 550.6A for the 100kVA and 200kVA three-phase inverter system respectively.

Therefore the 100kVA and 200kVA three-phase inverter battery system capacity in Ah would be 1603.25Ah 5.5h and 4129.69Ah 7.5h.

## 2.5 Chapter Summary

From the above discussion, the following points are summarized:

- UCTMS has all its load as critical
- Therefore the only PLS technique that must be implemented at UCTMS was the generation technique or distributed generation, which for this project was the three-phase inverter in conjunction with a lead-acid battery.
- By comparing two specific three-phase inverter battery system, 100kVA and 200kVA, it was concluded that the bigger the three-phase inverter the more savings can be obtained.
- It was noticed that because UCTMS load profile was too flat, a higher inverter would increase the discharging period, hence the battery energy would increase a lot.

- Using UCTMS load profile, the battery storage device, lead-acid battery, was sized for the 100kVA and 200kVA three-phase inverter.

The next chapter will discuss the choice of the three-phase inverter topology for UCTMS, as well as its control design to analyze its technical feasibility.

### 3 Choice of the Three-Phase Inverter Topology

In chapter 2, UCTMS loads were discussed; it was found out that the loads are all critical. Thus, from the several PLS techniques discussed previously in chapter 1, the generation technique was the chosen one, which for the purpose of this thesis is seen as a three-phase inverter in conjunction with a BESS.

The quality of power transfer is very important when connecting a three-phase inverter system with a three-phase grid, especially when supplying loads such as those required at UCTMS. The installed system must increase the quality of the overall system, instead of bringing additional problems.

Thus, the choice of the type of three-phase inverter to be used is very important [11]. The first sections of this chapter will discuss the two different types of inverters, the voltage source inverter (VSI), and the current source inverter (CSI), its advantage and disadvantage. Thereafter, the one most suitable for this application will be chosen. Furthermore, a control design to accomplish the PLS scheme will be discussed.

#### 3.1 Introduction

The three-phase inverter can be used either as VSI or as CSI. In VSI connection, the three-phase inverter input signal is a direct current (DC) voltage, while in the CSI the input signal is a DC current source [12].

The output signal in the VSI is an alternate current (AC) voltage signal with a controllable amplitude and phase [12]. Thus, the active and reactive power can be controlled bi-directionally by controlling the three-phase inverter phase angle and voltage magnitude respectively [7, 13]. Moreover, in this setup a proper design of a link inductor is very important for a good real and reactive power control. Equations (3.1-1) and (3.1-2) illustrate this.

$$P = \frac{V_{Conv} \cdot V_{Grid} \cdot \sin\delta}{X_{Link}} \quad (3.1-1)$$

$$Q = \frac{(V_{Conv}^2 - V_{Conv} V_{Grid} \cos\delta)}{X_{Link}} \quad (3.1-2)$$

Where,  $P$  and  $Q$  represent the real and reactive phase power of the three-phase inverter respectively.  $P$  and  $Q$  can flow bidirectional by controlling  $V_{conv}$  and  $\delta$  respectively.  $V_{conv}$  is the three-phase inverter magnitude voltage and  $\delta$  is the power angle of the three-phase inverter. The angle  $\delta$  is the angle between  $V_{conv}$  and  $V_{Grid}$ .  $V_{Grid}$  is the voltage of the grid.  $X_{Link}$  is the reactance of the link inductor.

However, in CSI the output controllable signal is the filter inductor current [11]. In this setup, the active and reactive power control is achieved by controlling the real and imaginary component or the d-component and q-component of the output inductor filter current respectively.

### 3.2 Voltage Source and Current Source Inverter for Power Quality

This section will look into the difference of using the three-phase inverter as VSI in relation of using it as CSI for power quality.

Prodanovic and Green, [11], discussed that when using the three-phase inverter as VSI, *“the output current and power quality depends on the grid voltage quality”* [11]. Thus, any grid voltage distortion would automatically decrease the output power and current quality. In addition, it was also discussed by Prodanovic and Green that in this configuration the three-phase converter system would behave as low impedance to the already present grid voltage distortion. Consequently, the power quality would be poor.

However, by operating the three-phase inverter as CSI, it was argued and shown experimentally that the power quality would be a lot better [11], because output current quality is not substantially affected by the grid voltage quality.

It was also stated that, *“the main advantage of using a CSI instead of a VSI is that within the control frequency range, higher output impedance is observed from the point of view of the grid voltage”*[11]. This action had the result of decreasing the influence of voltage harmonics on the output current, so power quality would be high.

For this thesis the three-phase inverter was used as CSI to ensure high output current quality and subsequently power quality [11]. In addition, the three-phase inverter input source signal used for this thesis was a DC voltage signal (from a battery bank) across a capacitor instead of a DC current signal as discussed by Mohan, [12].

Nevertheless, by connecting the battery bank on the input of the three-phase inverter across a capacitor, this configuration of the three-phase inverter is known as a VSI as discussed previously. However, by controlling the current through the output filter inductor, the VSI was made to behave as CSI [11].

### 3.3 Three-phase inverter Topology

From the above discussion, the real and reactive power can also be controlled bi-directionally by controlling the filter inductor current, real and imaginary part respectively.

Therefore, for this thesis, in simulation, the three-phase inverter was operated as CSI. The topology in figure 3.3-1 was designed without the link inductor; it was implemented in simulation design and in practice.

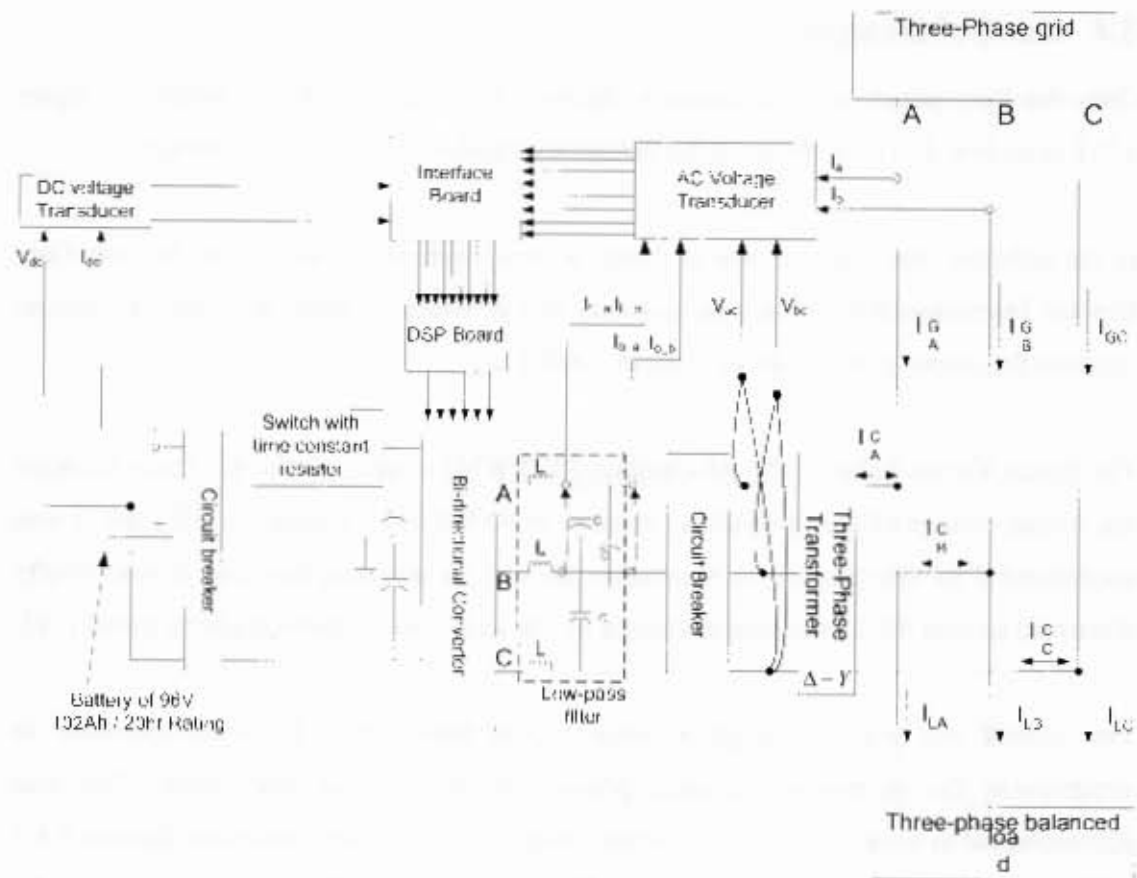


Figure 3.3-1: Three-phase inverter topology

The next section will look into different control designs for the chosen three-phase topology.

The three-phase inverter had to be connected with the three-phase grid in such a way that it would not cause any disturbance on the moment of connection. Thus, for it to be possible a phase-locked loop using a proportional plus integral (PI) controller was used to synchronize the three-phase inverter frequency with the three-phase grid frequency [14].

Moreover as was discussed above that the three-phase voltage source inverter was used as CSI by controlling the inductor filter current, so a control design using a PI controller also. was investigated with the guidance of the literature [11, 15] to control the current flowing through the inductors filter.

### 3.4 Control Design

Once the three-phase inverter topology, figure 3.3-1, was modeled in simplorer, figure 4.7-1 in section 4.7-1, the focus of the project was shifted to the software design.

In the software, the first aim was to design a switch scheme to switch the Insulate Gate Bipolar Transistor (IGBT) gates in such way that it would decrease the switching losses; increase the output modulation as close to 100% [16].

The Space Vector Pulse Width Modulation (SVPWM) is such a scheme. It can increase the output voltage of the three-phase inverter to 90.6% of its capability [17], and it was implemented in this project, in simulation as well in practice, however it was briefly discussed section 4.9.2, as it was discussed by the author in his undergraduate thesis [18].

The second aim was to design a phase locked loop (PLL) PI-based controller to synchronize the three-phase inverter phase with three-phase grid phase. This was accomplished in simulation and in practice using a PLL PI-based controller. Section 3.4.1 will discuss the PLL PI-based controller. The result of the PLL PI-based controller, the three-phase inverter phase angle, was very important, because it helped to calculate the three-phase inverter signals such as, the voltage and the current, in the rotating reference plane using the Parke Transformation.

The third aim was to design and implement a minor loop current controller using a PI controller to control the inductor filter currents. This was possible by using the respective signals in rotating reference plane as discussed above. Furthermore the signals in the rotating reference plane behave as DC signals, which made the implementation of a PI controller easy [19]. The minor loop current controller was only accomplished in simulation and not in practice due to time constrain. The minor loop current controller design is discussed in section 3.4.2.

The fourth and last aim was to use the minor loop current controller to accomplish bidirectional real and reactive power flow. Thus, a power calculator [11, 20] was used to produce current reference for the minor loop current controller.

### 3.4.1 Phase Locked Loop Controller

Phase locked loop (PLL) is a very important concept, as the name implies it happens when an arbitrary device or system is able to adjust its phase or frequency to the same phase or frequency of the main system, and then locking to it [21].

Kaura and Blasko, [14], discussed that the PLL PI-based controller can be designed in the rotating reference plane. Figure 3.4.1-1 illustrates the block diagram proposed by Kaura and Blasko.

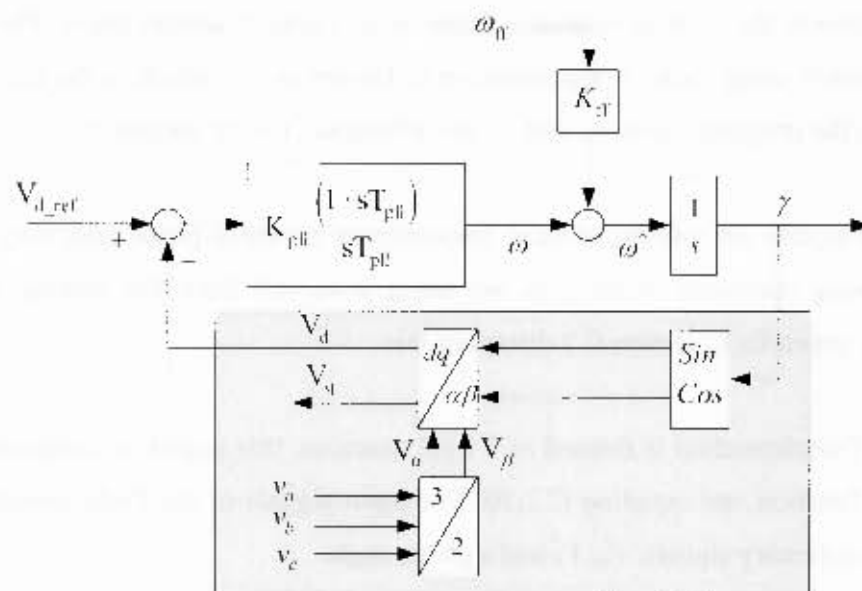


Figure 3.4.1-1: Block diagram of PLL PI-based controller [14]

In this technique the three-phase grid voltages,  $V_a$ ,  $V_b$  and  $V_c$  are conditioned and transformed to the stationary reference plane by using Clark Transformation. The Clark Transformation is made of a 2 by 3 matrix, which receives the three-phase grid voltages

as input and outputs two signals orthogonal to each other, see equation C.1-13 or C.1-14 in the appendix C.

The obtained signals are known as voltage alpha ( $V_\alpha$ ) and voltage beta ( $V_\beta$ ), where  $V_\alpha$  is the real part and is in phase with grid phase to neutral voltage  $V_m$ , and  $V_\beta$  is the imaginary part and is at  $90^\circ$  out phase to  $V_\alpha$ . The voltage  $V_\beta$  can either lag or lead  $V_\alpha$  by  $90^\circ$ .

The lagging or leading effect, depends on the following: if the three-phase grid connection is done in positive sequence as illustrated in figure C.2-1 in the appendix C and the positive sequence forward Clark transformation, equation C.1-13 is used, then  $V_\beta$  lags  $V_\alpha$ , refer to figure C.2-2. On the other hand if negative sequence forward Clark Transformation, equation C.1-14, is applied instead,  $V_\beta$  leads  $V_\alpha$ , refer to figure C.2-3.

Now the next step was to transform the obtained voltage signals from the stationary reference plane to the rotating reference frame using Parke Transformation. The voltages signals obtained using Parke Transformation is known as  $V_d$ , which is the real part and  $V_q$ , which is the imaginary part.  $V_d$  and  $V_q$  are orthogonal to one another too.

When these signals are rotating at same frequency as the three-phase grid, they have the effect of being stationary when they are being observed from the rotating reference frame, [22], appendix C section C.2 discusses this.

The Parke Transformation is formed of 2 by 2 matrices; this matrix is composed of sine and cosine function, see equation C.2-20. The input signals of the Parke transformation are the two stationary signals,  $V_\alpha$ ,  $V_\beta$  and a phase angle.

This phase angle,  $\gamma$ , is the three-phase inverter phase angle, which was obtained by using a PI controller and an integral function, see figure 3.4.1-1. The input of the PI controller is an error signal, made of the difference of the setpoint and the signal  $V_d$ .

The set point was set to zero, which would force  $V_d$  to zero. When  $V_d$  tracks the set point to zero, it was argued that the three-phase inverter phase angle would be the same as the three-phase grid phase angle,  $\theta$ , i.e. the two systems would be at the same frequency [14]. The PI controller output signal was a frequency signal; this frequency in turn was integrated into the required angle by the integrator plant, see figure 3.4.1-1.

Therefore, the same principle was used for this research. In addition, the PLL PI-based controller discussed in [14] was argued to be simple to be implemented in a digital signal processor (DSP), fast and robust for the three-phase utility applications even if the utility voltage is distorted.

### 3.4.1.1 Design of PLL PI-based using Clarke and Park Transformation

Following the work of Kaura and Blasko [14], a PLL PI-based controller was derived from basic principle derivation for this research. Some variables will be defined for the analysis. The symbol  $\theta$  known as theta was defined as the three-phase grid phase angle, which rotates at 50Hz and the symbol  $\gamma$  known as gamma was defined as the three-phase inverter phase angle.

The fundamental aim of the PLL PI-based controller is to equate  $\gamma$  to  $\theta$  and then lock it there. Now using equation (C-1) and all those equations discussed in section C.2 in appendix C, equation (3.4.1.1-1) was obtained [14].

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = -V \begin{pmatrix} \sin(\gamma - \theta) \\ \cos(\gamma - \theta) \end{pmatrix} \quad (3.4.1.1-1)$$

The full derivation of equation (3.4.1.1-1) can be found in appendix D.

Thus from equation (3.4.1.1-1), it was clear that when  $\gamma$  was equal to  $\theta$ ,  $V_d=0$ , which validates the discussion in the previous section. Kaura and Blasko, [14] also mentioned

that by regulating  $V_d$  to zero the possibility of rapidly locking the inverter voltage to utility voltage was high.

Using equation (3.4.1.1-1) and focusing the attention to  $V_d$ , the simplified control model of the PLL PI-based system in figure 3.4.1-1 is presented in figure 3.4.1.1-1 [14].

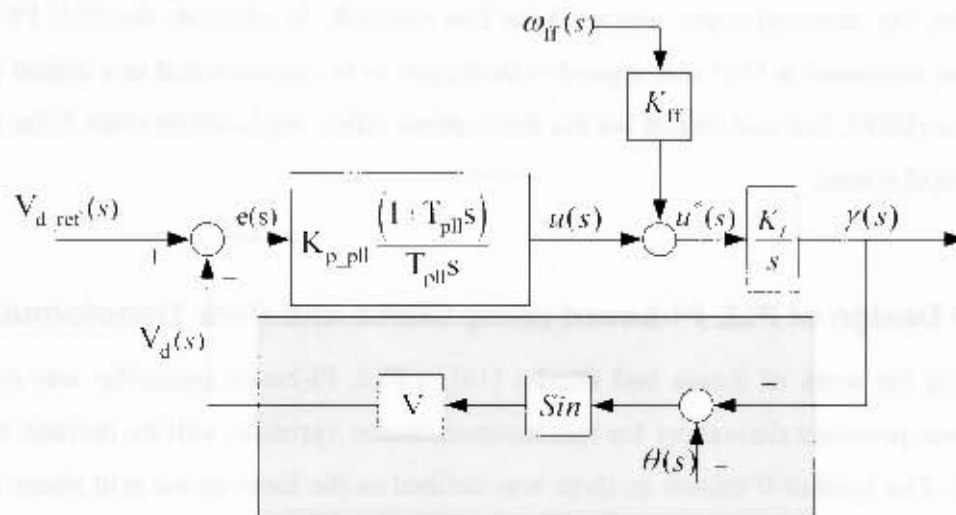


Figure 3.4.1.1-1: Simplified block diagram for PLL PI-based Controller [14]

The grid phase angle “ $\theta$ ” was calculated using equation (3.4.1.1-2)

$$\theta = \text{atan} 2(V_\alpha, V_\beta) \quad (3.4.1.1-2)$$

Therefore, figure 3.4.1.1-1 was used to implement the PLL PI-based controller for this project. The feedforward signal,  $\omega_{ff}$ , as it is illustrated in figure 3.4.1.1-1 is used to help regulating the tracking error due to any system frequency change [14]. However, for this thesis in practice,  $\omega_{ff}$  was not used, because the utility grid frequency was quite stiff.

Calculating the open loop transfer functions from figure 3.4.1-1, equations (3.4.1.1-3) to (3.4.1.1-5) were obtained.

$$q(s) = k(s)g(s) = K_{p\_pll} \left( \frac{1 - T_{pi}s}{T_{pi}s} \right) \left( \frac{K_i}{s} \right) \quad (3.4.1.1-3)$$

$$k(s) = K_{p\_pll} \left( \frac{1 + T_{pi}s}{T_{pi}s} \right) \quad (3.4.1.1-4)$$

$$g(s) = K_i \left( \frac{1}{s} \right) \quad (3.4.1.1-5)$$

Expanding equation (3.4.1.1-4), equation (3.4.1.1-6) was obtained.

$$k(s) = \frac{K_{p\_pll}}{T_{pi}s} + K_{p\_pll} = \frac{K_i - K_{p\_pll}s}{s} \quad (3.4.1.1-6)$$

Where  $q(s)$  is the open loop transfer function,  $k(s)$  is the PI control; it is a type I control, which means that it is made of only one integrator [19]. The transfer function  $g(s)$  is the integrator plant. The variable  $K_{p\_pll}$  is the proportional gain, its function is to set the high frequency gain.  $T_{pi}$  is the integrator time constant. The integrator gain,  $K_i$  is equal to the ratio of the proportional gain over the integral time constant.

In addition, the integral gain sets the low frequency gain of the open loop system,  $q(s)$ . Martin Braae [19], mentioned that this action would enable the close loop system to track the setpoint with good precision

It was mentioned that because the PLL PI-based controller had two integrators connected in series see figure 3.4.1.1-1, where the first one is the integrator part of the PI control and the other one is the PLL PI-based controller plant,  $g(s)$  [14]. Consequently, the PLL PI-based controller could be used as a filter too, so this would help to block any unwanted noise in the output of the PLL PI-based controller, which would enter with the sampled voltages [14].

### 3.4.1.2 PLL PI-based controller gain parameters calculation

Figure 3.4.1.1-1 can be treated as a linear control system due to the fact that  $\sin(\gamma - \theta)$  behaves in a linear manner for small values of  $(\gamma - \theta)$ , thus  $\sin(\gamma - \theta)$  can be approximated to  $(\gamma - \theta)$  [14].

Methods such as root-locus or nyquist design can be used to calculate the PI controller gains [19], however the method used in reference [14] was the method of symmetrical optimum. The equations (3.4.1.2-1) to (3.4.1.2-3) were derived from this method [14], and were used to calculate the gain for this thesis.

$$\omega_c = \frac{1}{\alpha T_s} \quad (3.4.1.2-1)$$

$$T_{pi} = \alpha^2 T_s \quad (3.4.1.2-2)$$

$$K_{p \text{ pi}} = \left( \frac{1}{\alpha} \right) \left( \frac{1}{VT_s} \right) \quad (3.4.1.2-3)$$

Where,  $\alpha$  known as alpha was defined as the normalizing factor,  $T_s$  the system sampling time, and  $V$  the grid amplitude voltage [14].

For this thesis the switch frequency was chosen to be 10 kHz, which meant  $T_s = 100\mu s$ . The grid voltage was sampled at the lower side of the three-phase transformer, at rms line-to-line voltage of 55.4 V, thus  $V_{\max LL} = 45.234V$ , but  $V = \frac{1}{\sqrt{2}} V_{\max LL}$  for equation (3.4.1.2-3).

The normalizing factor used in reference [14] was chosen to be 2.4 or 30. It was discussed that with  $\alpha=2.4$ , it would enable the PLL PI-based controller to quickly lock to a distorted utility voltage, however its output signal would be full of harmonics. On other

hand with  $\alpha=30$  the locking is not as quick but gives a clean output signal on the PLL PI-based controller.

Thus the same values of  $\alpha$  were used for this project, table 3.4.1.2-1 illustrate the PI controller gains and its bandwidth frequency.

**Table 3.4.1.2-1: Table of the PI controller gains and constant**

$\alpha$	$\omega_c$ (rad/s)	$\omega_c$ (Hz)	$K_{p\_pi}$	$T_{pi}$ (msec)	$K_{i\_pi}$
2.4	4166.67	663.14	92.11	0.576	159913.2
30	333.33	53.05	7.37	90	81.9

From table 3.4.1.2-1, it can be seen that with  $\alpha=2.4$  the proportional and integral gains were much bigger compared with  $\alpha=30$ , specially the integral gain, which helped to understand why  $\alpha=2.4$  had a fast tracking compared with  $\alpha=30$ .

Kaura and Blasko, [14], added that in practice both values could be used,  $\alpha$  equal to 2.4 would be used to quickly lock to the utility grid voltage because of its high bandwidth and then, changing to  $\alpha$  equals to 30 to give a clean PLL output signals.

Figure 3.4.1.1-1, represent the control loop in continuous time domain, it was implemented in this way in the simulation. However, in practice, due to nature of the DSP chip, which is in digital form, where the signals are sampled or discrete, thus figure 3.4.1.1-1 was changed to discrete time domain. The next section will discuss this.

### 3.4.1.3 PLL PI-based Controller in digital form

In the DSP chip, the signals used were sampled and quantized from its continuous counterpart signals [23]. This was possible by using analog to digital converter (ADC) in conjunction with a sample-and-hold (S/H) device. The S/H had the aim to allow the signal to keep entering the ADC while it was being converted [23].

However to convert back to analog signals, a digital to analog converter (DAC) in conjunction with a zero order hold (ZOH) was used. The ZOH was the digital equivalent of the S/H. The ZOH had the aim of holding the last sampled signals until the next sample happens [23, 24]. Figure 3.4.1.3-1 shows this.

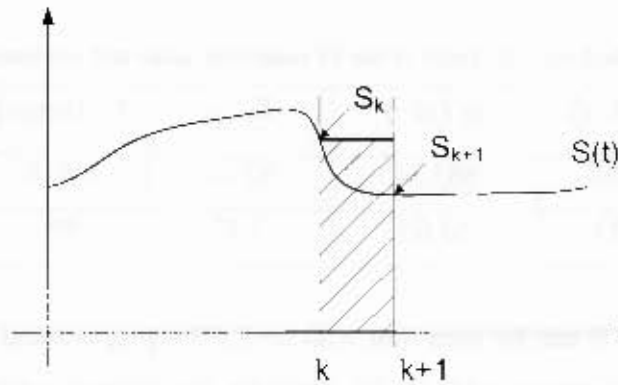


Figure 3.4.1.3-1: Representation of ZOH approximation [24].

In figure 3.4.1.3-1, variable “ $k$ ” represents the present value being sampled, “ $k+1$ ” is the next sampled value at sample time  $T_s$ , and  $S(t)$  is the signal being sampled [24].

The PLL PI-based controller transfer function  $k(s)$  and  $g(s)$  were transformed to discrete form by using  $z$ -transformation, this process enable the PLL PI-based controller to be implemented digitally in a very simple away.

However, for those transfer functions to be operated successfully digitally, the ZOH function should be implemented with them. As discussed above it holds the sampled signals entering each transfer function for a time  $T_s$  and updates to the next sampled value in the next period.

The transfer function of the ZOH was defined as shown in equation (3.4.1.3-1) [19].

$$h(s) = \frac{1 - e^{-sT}}{s} \quad (3.4.1.3-1)$$

Applying the z-transform to the transfer function  $k(s)$  and  $g(s)$  in conjunction with equation (3.4.1.3-1), equations (3.4.1.3-2) and (3.4.1.3-3) were obtained.

$$k(z) = z \left[ k(s) \cdot h(s) \right] \quad (3.4.1.3-2)$$

$$g(z) = z \left[ g(s) \cdot h(s) \right] \quad (3.4.1.3-3)$$

Substituting equations (3.4.1.2-5), (3.4.1.2-6) and (3.4.1.3-1) into (3.4.1.3-2) and (3.4.1.3-3) and after a bit of simplification, equations (3.4.1.3-4) and (3.4.1.3-5) were obtained [19].

$$k(z) = z \left[ \frac{(K_I - p_{ii} + K_P - p_{ii}s)}{s^2} \right] = z \left[ \frac{(K_I - p_{ii} + K_P - p_{ii}s)e^{-sT}}{s^2} \right] \quad (3.4.1.3-4)$$

$$g(z) = z \left[ \frac{K_I}{s^2} \right] = z \left[ \frac{K_I e^{-sT}}{s^2} \right] \quad (3.4.1.3-5)$$

In addition, using real translation principle, equations (3.4.1.3-6) and (3.4.1.3-7) were obtained [19].

$$k(z) = (1 - z^{-1})z \left[ \frac{(K_I - p_{ii} + K_P - p_{ii}s)}{s^2} \right] \quad (3.4.1.3-6)$$

$$g(z) = (1 - z^{-1})z \left[ \frac{K_I}{s^2} \right] \quad (3.4.1.3-7)$$

Using the z-transform table, [19], equations (3.4.1.3-6) and (3.4.1.3-7) were transformed to equations (3.4.1.3-8) and (3.4.1.3-9).

$$k(z) = \frac{K_{I\_p^{ii}}T_s - K_{P\_p^{ii}}(z-1)}{(z-1)} \quad (3.4.1.3-8)$$

$$g(z) = \frac{K_I T_s}{(z-1)} \quad (3.4.1.3-9)$$

Moreover representing  $k(z)$  and  $g(z)$  in terms of its input and output, and neglecting the feedforward input,  $\omega_{ff}(s)$  due to the reason explained above, equations (3.4.1.3-10) and (3.4.1.3-11) were obtained.

$$\frac{u(z)}{e(z)} = \frac{K_{I\_p^{ii}}T_s + K_{P\_p^{ii}}(z-1)}{(z-1)} \quad (3.4.1.3-10)$$

$$\frac{y(z)}{u(z)} = \frac{K_I T_s}{(z-1)} \quad (3.4.1.3-11)$$

Applying cross multiplication in the equations (3.4.1.3-10) and (3.4.1.3-11), equations (3.4.1.3-12) and (3.4.1.3-13) were obtained.

$$zu(z) = K_{I\_p^{ii}}T_s e(z) + zK_{P\_p^{ii}}e(z) - K_{P\_p^{ii}}e(z) \cdot u(z) \quad (3.4.1.3-12)$$

$$zy(z) = K_I T_s u(z) + y(z) \quad (3.4.1.3-13)$$

Dividing equations (3.4.1.3-12) and (3.4.1.3-13) by  $z$  and applying the inverse z-transformation it yields the difference equations, as illustrated in equations (3.4.1.3-14) and (3.4.1.3-15) [19].

$$u_k = K_{i\_pll} T_s e_{k-1} + K_{p\_pll} e_k - K_{p\_pll} e_{k-1} + u_{k-1} \quad (3.4.1.3-14)$$

$$y_k = K_i T_s u_{k-1} + y_{k-1} \quad (3.4.1.3-15)$$

Where  $u_k$ ,  $e_k$ , and  $y_k$  represent the present values, and  $u_{k-1}$ ,  $e_{k-1}$ , and  $y_{k-1}$  represents the previous values.

The variable  $u_k$  is the PI controller output equation in digital form and  $y_k$  is the integral function output equation in digital form. The PLL PI-based control had initial conditions and it was important to initialize them for a good operation of the system.

A good initial value to be implemented was zero, however, it was noted that the digital integral representation, equation (3.4.1.3-15), was only composed by previous values variables as discussed before. Thus the initial condition created a response delay in the equation (3.4.1.3-15) of  $T_s$  period [14].

#### 3.4.1.4 PLL PI-based algorithm implementation

This section will illustrate, the block diagram of simplified controller of PLL PI-based controller, figure 3.4.1.1-1 in code form, also it will discuss its implementation in DSP chip, using a high-level language C.

Figure 3.4.1.1-1 has three comparators, which were: the error comparator  $e(s)$ , i.e. the difference between the setpoint and the feedback signal. The next comparator was the phase difference between the three-phase inverter phase angle and the three-phase grid phase angle.

Finally, the last comparator was the feedforward ( $\omega_{ff}(s)$ ) comparator. The feedforward comparator was neglected due to the reasons explained above. The aim of a comparator was to add or subtract signals.

One important thing to understand was that when the software is implemented, the compiler reads the code line by line from top down, therefore it was important to write the code in such way that the compiler execute exactly what it was supposed to do.

On that note, because  $\theta(s)$  was the only calculated sampled signal coming into the control loop and it was joined by required signal  $\gamma(s)$  in the comparator as discussed above, thus the PLL PI-based algorithm code was started in the feedback loop, and equation (3.4.1.4-1) illustrates this.

$$theta\_PLL\_diff = \gamma - \theta ; \quad (3.4.1.4-1)$$

The next equation (3.4.1.4-2) was defined as “*Fdbck\_PLL*”, which was composed of a sinusoidal function, which takes as argument the angle difference illustrated in the equation (3.4.1.4-1)

$$Fdbck\_PLL = \sin(theta\_PLL\_diff) ; \quad (3.4.1.4-2)$$

The voltage amplitude,  $V$ , in feedback path as illustrated in figure 3.4.1.1-1 was neglected and left as unity for simplicity in equation (3.4.1.4-2). This was because, it was mentioned that if variable  $V$  is used, then any grid voltage distortion such as a voltage dip or voltage unbalance, would result in the loss of  $V$  in the control loop [14].

Equation (3.4.1.4-2) was the feedback signal  $V_d$  as discussed in section 3.4.1.1, recalling the argument made in the previous section, that by forcing  $V_d$  to zero the three-phase inverter phase angle would tracks the three-phase grid phase angle, thus the setpoint as discussed previously was set to zero.

Equation (3.4.1.4-3) presents the error signal. This error signal was the input signal for the PI controller.

$$err\_k\_PII = Setpoint\_PLL - Fdbck\_PLL ; \quad (3.4.1.4-3)$$

The digital PI controller derived in section 3.4.1.3, equation (3.4.1.3-14) was implemented in practice. Where  $u_k$  in the code was defined as  $U\_PLL$ ,  $u_{k-1}$  was defined as  $U\_k1\_PLL$ ,  $e_k$  was defined as  $err\_k\_PLL$  and finally  $e_{k-1}$  was defined as  $err\_k1\_PLL$ .

The product of integral gain  $K_I$  with  $T_s$ , and the proportional gain,  $K_P$  were represented as fraction with the denominator having a maximum value of  $2^{16-1}$ . This number representation,  $2^{16-1}$ , is an integer representation, which is very important in a digital signal processor fixed-point chip. The theory of fixed-point number representation will be dealt in the software chapter, section 5.2.3.6.

Finally, next step was to use the integrator digital equation, as derived in section 3.4.1.3, equation (3.4.1.3-15). Where  $y_k$  in the code was defined as  $Y\_PLL$  and  $y_{k-1}$  was defined as  $Y\_k1\_PLL$ . With this equation, the block diagram of figure 3.4.1.1-1 was complete in the code.

At this point in the code, the previous values were set to the present values, so that in the next entrance in the code they can be used accurately. They are illustrated in equations (3.4.1.4-5), (3.4.1.4-6) and (3.4.1.4-7).

$$e_{k-1} = e_k; \quad (3.4.1.4-5)$$

$$u_{k-1} = u_k; \quad (3.4.1.4-6)$$

$$y_{k-1} = y_k; \quad (3.4.1.4-7)$$

However, when the code was run for the first time, the above equations were initialized to zero in the main code routine, to ensure proper operation of the PLL control algorithm as discussed previously, refer to appendix J too.

In practice equation (3.4.1.3-15) was changed to equation (3.4.1.4-8)

control the real and reactive power respectively [11].  
 reference plane respectively. By controlling  $I_{Lr}$  and  $I_{Lq}$  individually, it was possible to  
 Where,  $I_{Lr}$  and  $I_{Lq}$  are the real and imaginary inductor current component in the rotating  
 $I_{Lr}$  and  $I_{Lq}$  currents using a PI controller and discrete techniques.

The focus of the minor loop current controller is to control the low-pass filter inductor  
 current. Prodanovic and Green, [11], accomplished it by controlling the filter inductor  
**3.4.2 Minor Loop Current Controller**

three-phase inverter by using the voltage drop across the inductor low pass filter.  
 The next section will discuss the derivation of the minor loop current controller of the  
 initial value of zero, hence the plant response would be zero.

response, equation (3.4.1.3-15), which at this point its input variable  $u_k$  and  $y_k$  had  
 $e_k$  to zero, however this first change of the PI controller would not affect the plant  
 Practically it meant that the PI controller responded in such way to decrease the change in

equation (3.4.1.4-3), which was one of the inputs of equation (3.4.1.3-14).  
 PI1. PI-based controller algorithm,  $u_k$ , equation (3.4.1.3-14) becomes non-zero due to  $e_k$ .  
 In other hand, if equation (3.4.1.3-15) were used instead, then in the first entrance in the  
 non-zero value in the first run.

of the code. This can be better understood by noticing that  $u_k$ , equation (3.4.1.3-14) had a  
 15) i.e. the integral output response, equation (3.4.1.4-8) would not be zero in the first run  
 action helped to eliminate the sample delay in integral output response, equation (3.4.1.3-  
 Where instead of using the previous value,  $u_{k-1}$ , the present value,  $u_k$ , was used. This

$$y_k = K_I T_s u_k + y_{k-1} \quad (3.4.1.4-8)$$

Figure 3.4.2-1 illustrates a single-phase inverter connected to a single-phase grid through a LC filter. Figure 3.4.2-1 was used to derive the inner current controller from basic principle derivation for this thesis as discussed in [15].

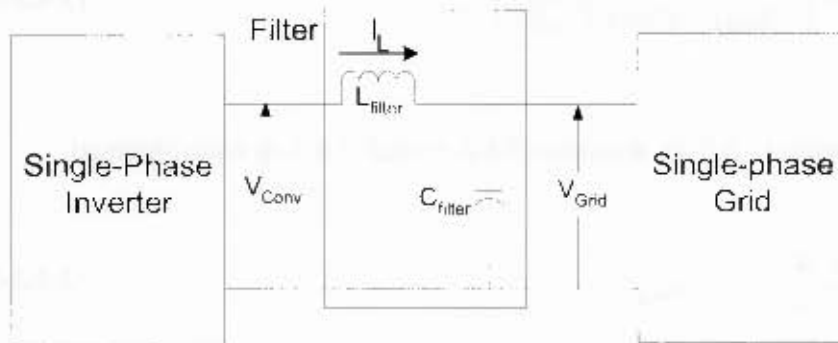


Figure 3.4.2-1: single-phase grid-tie inverter

Assuming the positive direction of the current to be from the converter to the grid, thus the inductor voltage drop is represented as equation (3.4.2-1)

$$V_{Conv} - V_{Grid} = V_L \quad (3.4.2-1)$$

Where,  $V_L$  is the voltage drop across the inductor filter. In addition, equation (3.4.2-1) was modified to equation (3.4.2-2) to represent the three-phase inverter system.

$$V_{Conv\_abc} - V_{Grid\_abc} = V_{L\_abc} \quad (3.4.2-2)$$

The inductor voltage drop was represented also as shown in equation (3.4.2-3).

$$V_L = L \frac{di_L}{dt} \quad (3.4.2-3)$$

Furthermore, substituting equation (3.4.2-3) into equation (3.4.2-2) and applying positive sequence Clarke Transformation, equation (C.1-13) as well as Park Transformation,

equation (C.2-20) to equations (3.4.2-2), equation (3.4.2-4) was obtained, refer to equation (E-7) appendix E.

$$\begin{pmatrix} V_{Conv_d} \\ V_{Conv_q} \end{pmatrix} = \begin{pmatrix} V_{Grid_d} \\ V_{Grid_q} \end{pmatrix} = \begin{pmatrix} \cos\gamma & \sin\gamma \\ -\sin\gamma & \cos\gamma \end{pmatrix} L \frac{d}{dt} \begin{pmatrix} i_{L_d} \\ i_{L_q} \end{pmatrix} \quad (3.4.2-4)$$

After evaluating equation (3.4.2-4), equation (3.4.2-5) and (3.4.2-6) were obtained.

$$V_{Conv_d} = -\omega L i_{L_q} + L \frac{d}{dt} i_{L_d} + V_{Grid_d} \quad (3.4.2-5)$$

$$V_{Conv_q} = \omega L i_{L_d} + L \frac{d}{dt} i_{L_q} + V_{Grid_q} \quad (3.4.2-6)$$

Where,  $V_{Conv_d}$ ,  $i_{L_d}$  and  $V_{Conv_q}$ ,  $i_{L_q}$  were the real and imaginary component in rotating reference plane of the three-phase inverter voltage and current respectively.  $V_{Conv_d}$ ,  $V_{Conv_q}$  once inverted back to the stationary reference frame, by using the inverse Parke Transformation, expression (C.2-22), they were used as input to the space vector pulse width modulation (SVPWM) to produce the switching signals for the three-phase inverter.

The detail of derivation of equations (3.4.2-5) and (3.4.2-6) from equation (3.4.2-4) can be found in appendix E. Using equations (3.4.2-5) and (3.4.2-6), the control block diagram of figure 3.4.2-2 was obtained.

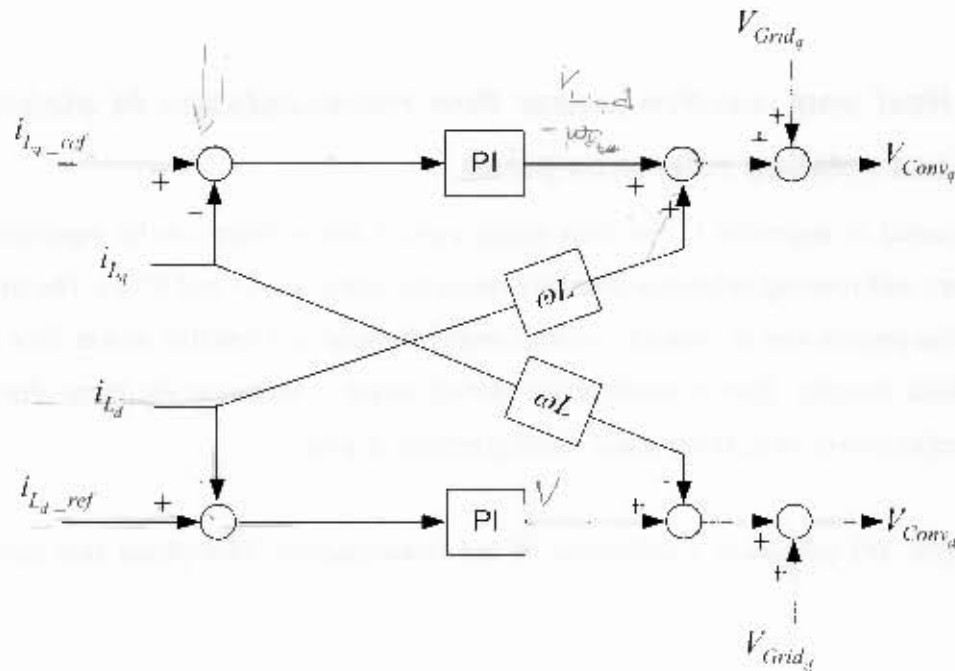


Figure 3.4.2-2: Block diagram of current controller

For this thesis the current controller as presented in figure 3.4.2-2 was only applied in simulation design, chapter 4, due to time constrain. Thus, a discrete analysis for the current controller to be implemented in the DSP chip is not presented here, but can be found in reference [11].

The components  $-\omega L i_{L_q}$  and  $\omega L i_{L_d}$ , as illustrated in figure 3.4.2-2, are known as cross-coupling [15, 25], which means that a sudden big change in the  $i_{L_d-ref}$ , the reference setpoint, in relation to  $i_{L_d}$  would not only cause a change in  $V_{Conv_d}$ , but also in  $V_{Conv_q}$ , the same argument applies for  $i_{L_q}$ .

For this thesis, a step test was not done for the current loop PI control because of type of load profile UCTMS has, which does not change suddenly but increases gradually throughout the day until it reaches its MD and then comes back to its minimum value as illustrated in figure 2.3-1. A normal operation without blackout was assumed too for simplicity.

### 3.4.3 Real and reactive power flow representation in stationary and rotating reference plane

As discussed in appendix C the three-phase current and voltage can be represented in stationary and rotating reference plane by using equations (C-1) and (C-2). The ultimate aim of the project was to control bi-directionally the real and reactive power flow of the three-phase inverter, thus it would make perfect sense to represent the three-phase real and reactive power in stationary and rotating reference plane.

Akagi [20, 26] proposed a definition of the instantaneous three-phase real power as follow:

$$p = v_a i_a + v_\beta i_\beta \quad (3.4.3-1)$$

Malinowski, [20] claims that this definition of the instantaneous power is the same as the standard definition of instantaneous three-phase power, which is illustrated in the equation 3.4.3-2.

$$p(t) = v_a(t) \cdot i_a(t) + v_b(t) \cdot i_b(t) + v_c(t) \cdot i_c(t) \quad (3.4.3-2)$$

For the instantaneous reactive power,  $q$ , Akagi [20, 26] proposed that,

$$q = v_\alpha \times i_\beta + v_\beta \times i_\alpha \quad (3.4.3-3)$$

Now representing equations (3.4.3-1) and (3.4.3-3) in matrix form, equation (3.4.3-4) was obtained [20].

$$\begin{pmatrix} p \\ q \end{pmatrix} = \begin{pmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \quad (3.4.3-4)$$

Where,  $p$  represents the total three-phase real power, and  $q$  the total three-phase reactive power.

The Clarke transformation to calculate the voltage and the current, to represent the instantaneous real and reactive power, as defined in the equation (3.4.3-4) differs from the one defined in equation (C-1) appendix C. This difference has to do with the multiplication of the coefficient, which in this case must be multiplied by  $\sqrt{\frac{2}{3}}$  instead of  $\frac{2}{3}$  [20]. Equation (3.4.3-5) shows this.

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \quad (3.4.3-5)$$

This action had the effect of making the instantaneous real and imaginary power of equation (3.4.3-4) to be equal to the conventional instantaneous real and imaginary three-phase power, [20].

Now applying Parke Transformation in the voltage and current signals alpha and beta of equation (3.4.3-4) and using as the input angle the three-phase inverter phase angle,  $\gamma$ , and at same time solving for the current signals, thus equation (3.4.3-5) was obtained.

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \frac{1}{V_\alpha^2 + V_q^2} \begin{pmatrix} v_\alpha & -v_q \\ v_q & v_\alpha \end{pmatrix} \begin{pmatrix} p \\ q \end{pmatrix} \quad (3.4.3-6)$$

One thing to notice is that the real and reactive power calculated using the voltage and current signals either in stationary or rotating reference plane would be the same.

Equation (3.4.3-5) was represented in block diagram as presented in figure 3.4.3-1

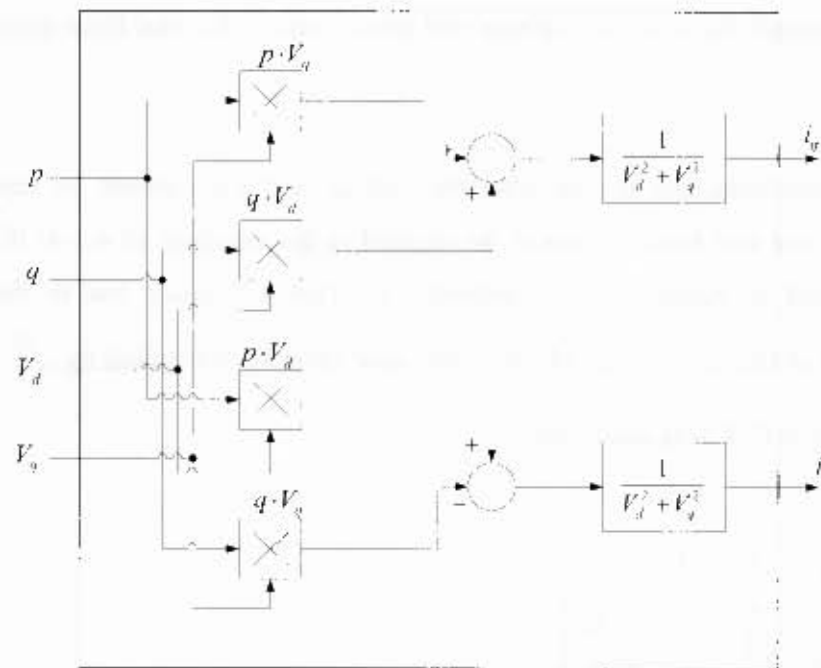


Figure 3.4.3-1: Power Calculator

For the project,  $p$  and  $q$  were the setpoint powers i.e. the powers that the three-phase inverter must deliver. The variables  $V_d$  and  $V_q$  were the output voltage signals of the three-phase inverter after the low-pass filter and  $i_d$  and  $i_q$  were the produced output setpoint currents, also after the LC low pass filter [11].

From the above discussion, figure 3.4.3-1 was combined with figure 3.4.2-2, which produced figure 3.4.3-2.

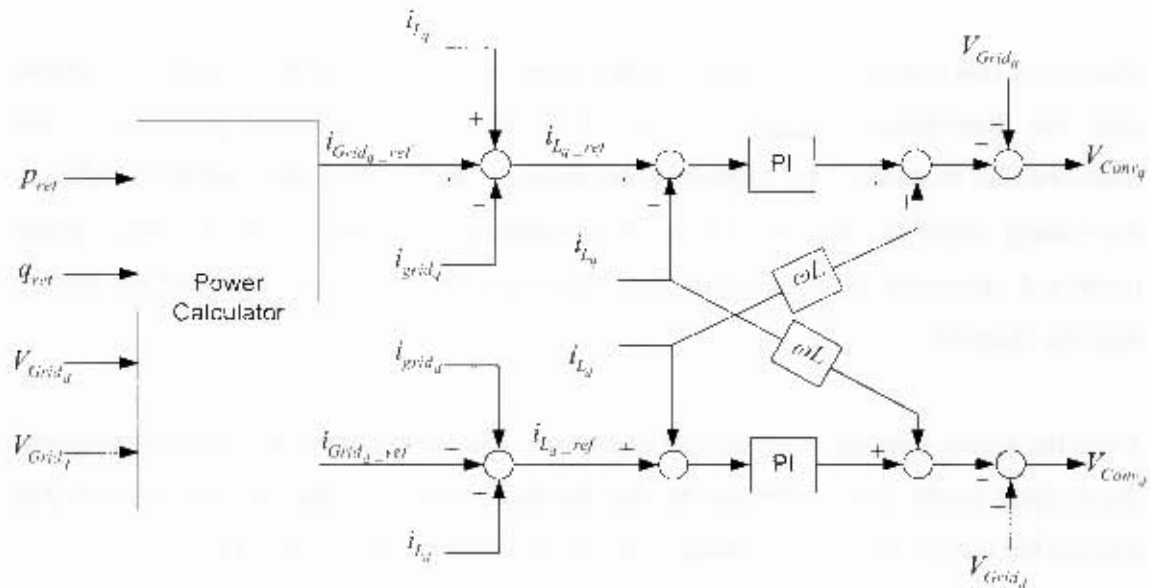


Figure 3.4.3-2: Minor loop current controller in conjunction with power calculator

Figure 3.4.3-2 is very important results because it helps to realize the bi-directional flow of real and reactive power by using the minor loop current controller in rotating reference plane.

Using reference [11], the reference currents,  $i_{L_d\_ref}$  and  $i_{L_q\_ref}$ , see figure 3.4.2-2 above, were able to be calculated from the power calculator by adding the inductor filter current,  $i_{L_d}$  and  $i_{L_q}$  and subtracting the LC filter output current  $i_{Grid_d}$  and  $i_{Grid_q}$  respectively, from the power calculator reference output currents,  $i_{Grid_d\_ref}$   $i_{Grid_q\_ref}$  respectively.

### 3.4.4 Peak Load shaving Algorithm

The Peak Load Shaving algorithm was developed from the theory discussed in section 2.3.1, whereby the focus was to decrease the real and reactive power of the three-phase inverter, in such way that the apparent power is decreased optimally. As discussed, that would be possible by delivering the apparent power from the three-phase inverter at the same PF as the three-phase grid.

Moreover, this action would mean that the three-phase grid currents would be in phase with the three-phase inverter currents. In addition, it was argued previously; that whenever the customer load happens to be above a set threshold, the power available in the battery must be delivered to the three-phase grid through a DC-AC three-phase inverter. Conversely, if the customer load happens to be below a set threshold the battery must be charged.

From the above discussion it could be understood that the battery activities (charging and discharging mode) were governed by the threshold settings. Thus, the next section will discuss the threshold algorithm design and its implementation in simplorer.

#### 3.4.4.1 Threshold algorithm

In section 2.3.3, the setting of an ideal monthly threshold value was assumed in such way, which only the maximum monthly peak would be shaved. This assumption helped to simplify the battery sizing analysis.

However, in reality the monthly peak load would not be known before hand, so it would be hard to choose a threshold value that would only decrease the maximum monthly peak at full capacity of the three-phase inverter. Thus, different method can be used to predict monthly peak load, for instance load forecasting [27].

For this project, however, a new method was developed. This method uses the previous history of the maximum monthly peak power; see table 1.2.4-1, to choose a reasonable initial threshold setting for a specific month.

Thereafter, it has the aim of preventing the difference between the maximum customer daily peak load and the set threshold value to exceed the inverter capacity. Thus, the threshold value would follow the changes of the maximum customer daily peak load in

such way to keep the difference the same as the inverter capacity or a desired percentage shaving.

Once the maximum daily customer peak load for that month is surpassed and reach a new maximum value for that month, the new threshold value would be calculated and held constant as long the difference between the new MD and the threshold value is less or equal to the three-phase inverter capacity.

This new threshold value would be the maximum value that the three-phase grid would reach in that month and consequently it would be the new MD for billing purpose. Figure 3.4.4.1-1 presents the discussion.

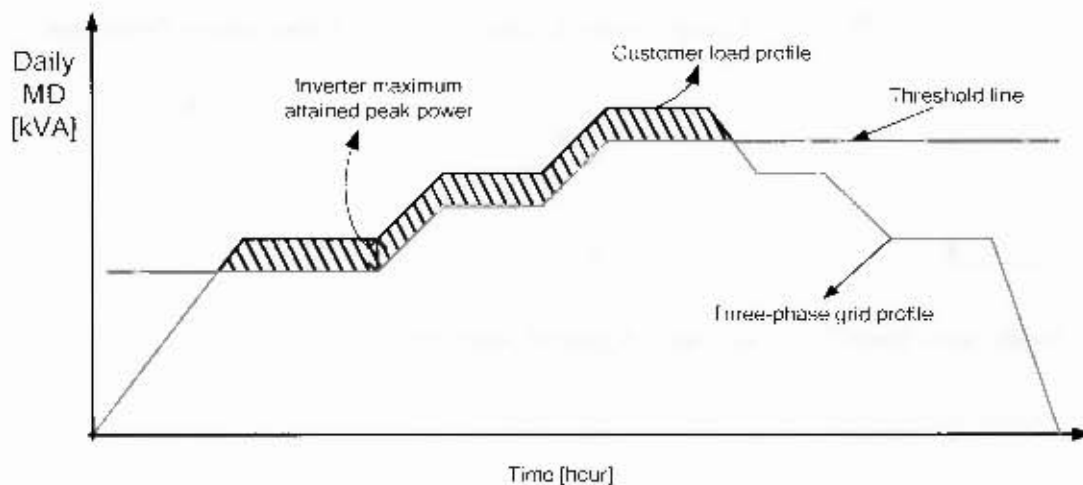


Figure 3.4.4.1-1: Threshold settings profile

Once the following month would be reached, the threshold value is reset to an acceptable value for that specific month using the UCTMS history MD, as presented in section 1.2.4 in table 1.2.4-1. Note that the analysis presented in figure 3.4.4.1-1 does not take in consideration the battery capacity. The focus was the threshold value settings only.

Using the analysis discussed in the previous paragraphs, the threshold settings algorithm was implemented in simplorer for 5% shaving refer to appendix G.6 to see the code. Figure 3.4.4.1-2 shows the threshold setting algorithm flow chart.

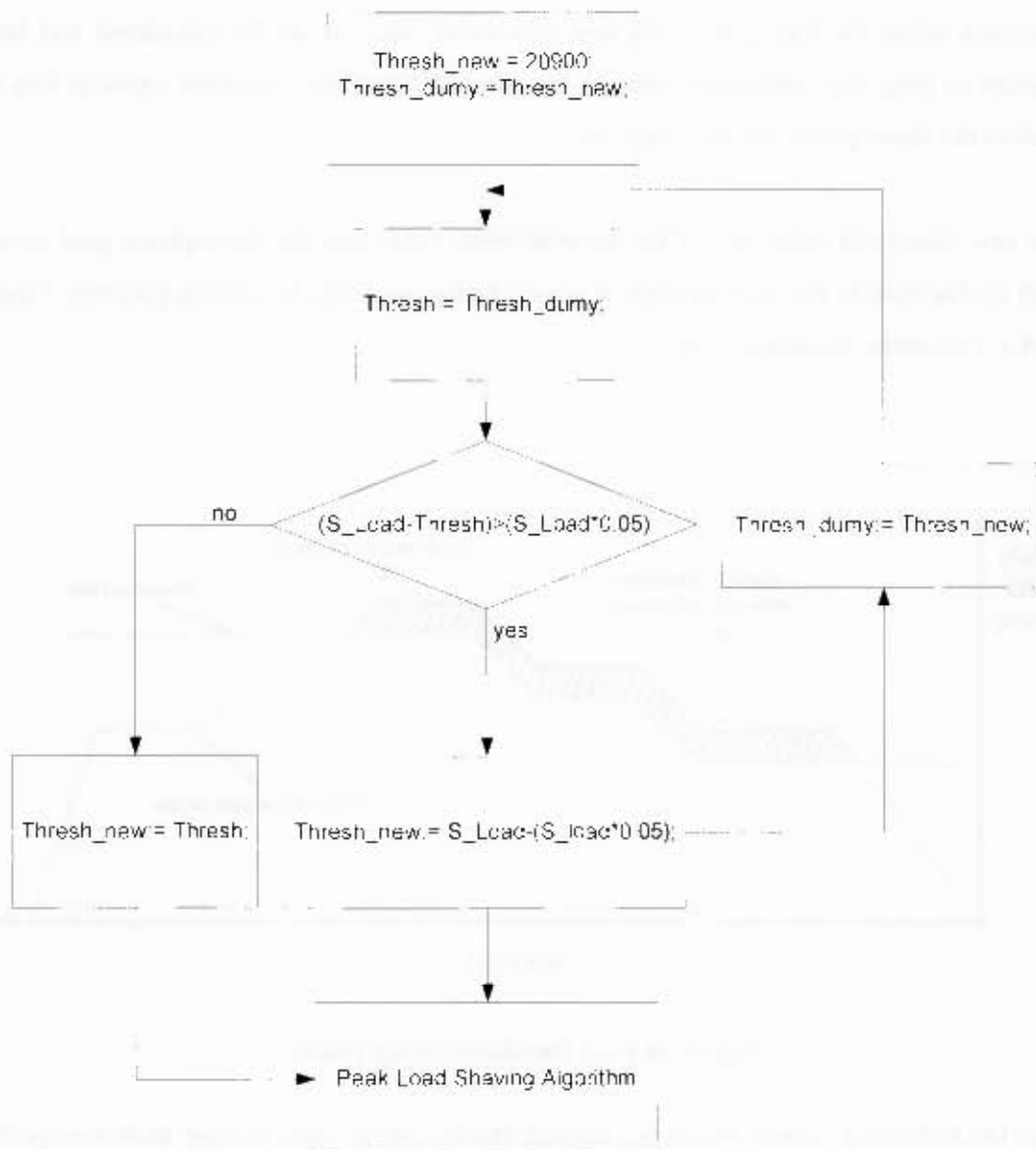


Figure 3.4.4.1-2: Threshold algorithm flow chart



Figure 3.4.4.2-1 illustrates the flow chart of charging and discharge implementation of the lead-acid battery in SIMPLOR. The flow of power was chosen to be positive from the three-phase inverter towards the three-phase grid.

The discharging of the lead-acid battery toward the three-phase grid through a three-phase inverter is equivalent of doing PLS of the real power. To accomplish the purpose PLS as discussed in section 2.3.1 the same PF as the grid was used to calculate the respective real and reactive power that the three-phase inverter must deliver to decrease the three-phase grid apparent power optimally. An algorithm to simulate discharge of the battery was written and implemented in SIMPLOR, see appendix C.6.

However, a basic algorithm was developed to illustrate the flow of real power into the battery (charging) as well as an algorithm that would decrease the flow of real power towards the battery to zero as the three-phase grid apparent power would reach 98% of the threshold value (see appendix C.6). Those algorithms were active whenever the three-phase source apparent power,  $S_{Source}$ , would be below the threshold point,  $Thresh_{new}$ .

### 3.4.4.2 Battery charging and discharging algorithm

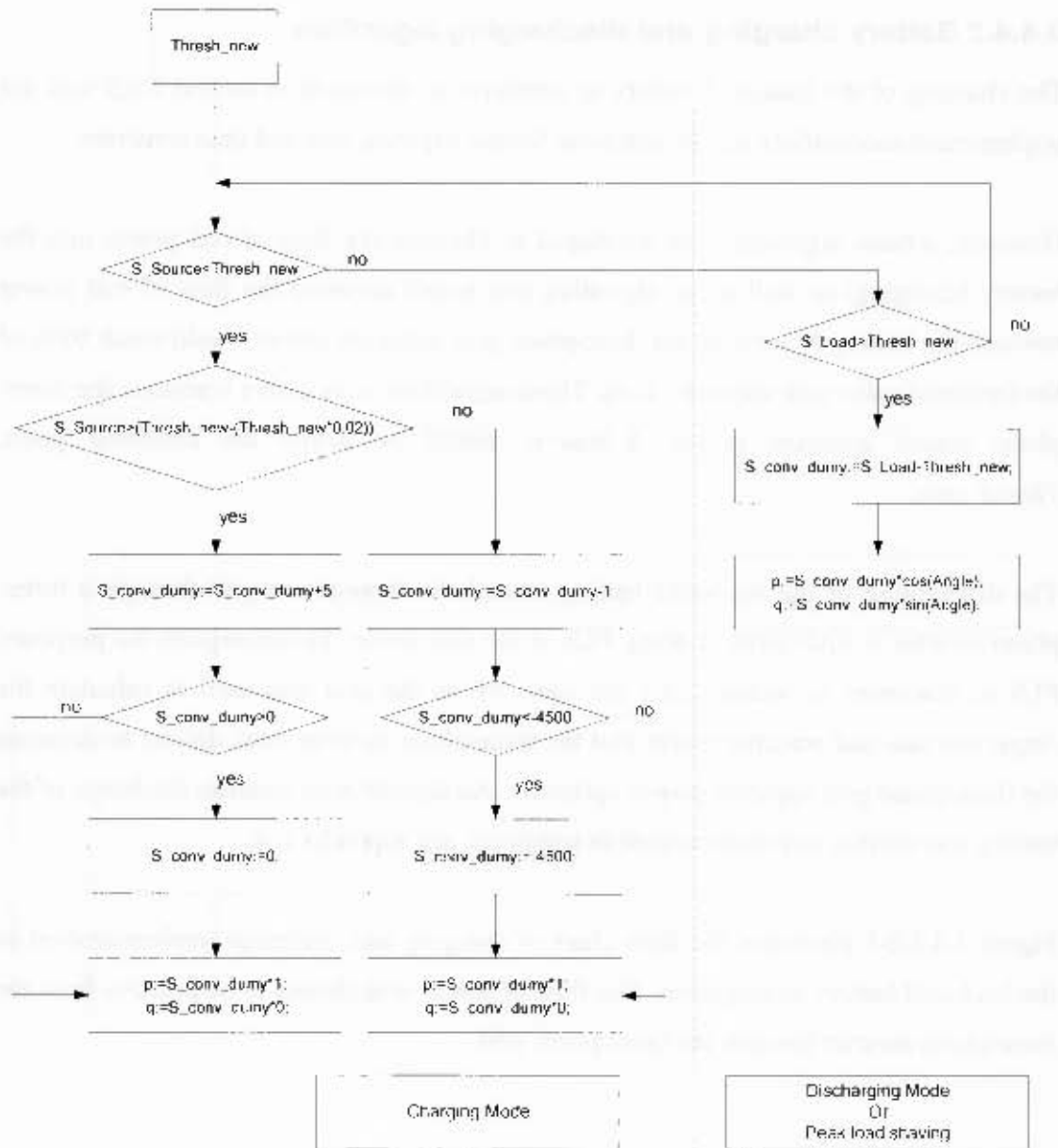


Figure 3.4.4.2-1: Peak Load Shaving algorithm flow chart

The algorithms as illustrated in figure 3.4.4.2-1 had as input the three-phase source apparent power,  $S_{Source}$ , the three-phase load apparent power,  $S_{Load}$  and the threshold value,  $Thresh\_new$ . The three-phase grid apparent power and the three-phase load apparent power were calculated as describe in appendix G.2 and G.3 respectively.

Its output variables were the real and reactive power  $p$  and  $q$ . These output variables were used as input to figure 3.4.3-2. In this way the real and reactive power were controlled bi-directionally by operating the three-phase inverter as CSI. Figure 3.4.4.2-2 illustrates the complete closed loop control design.

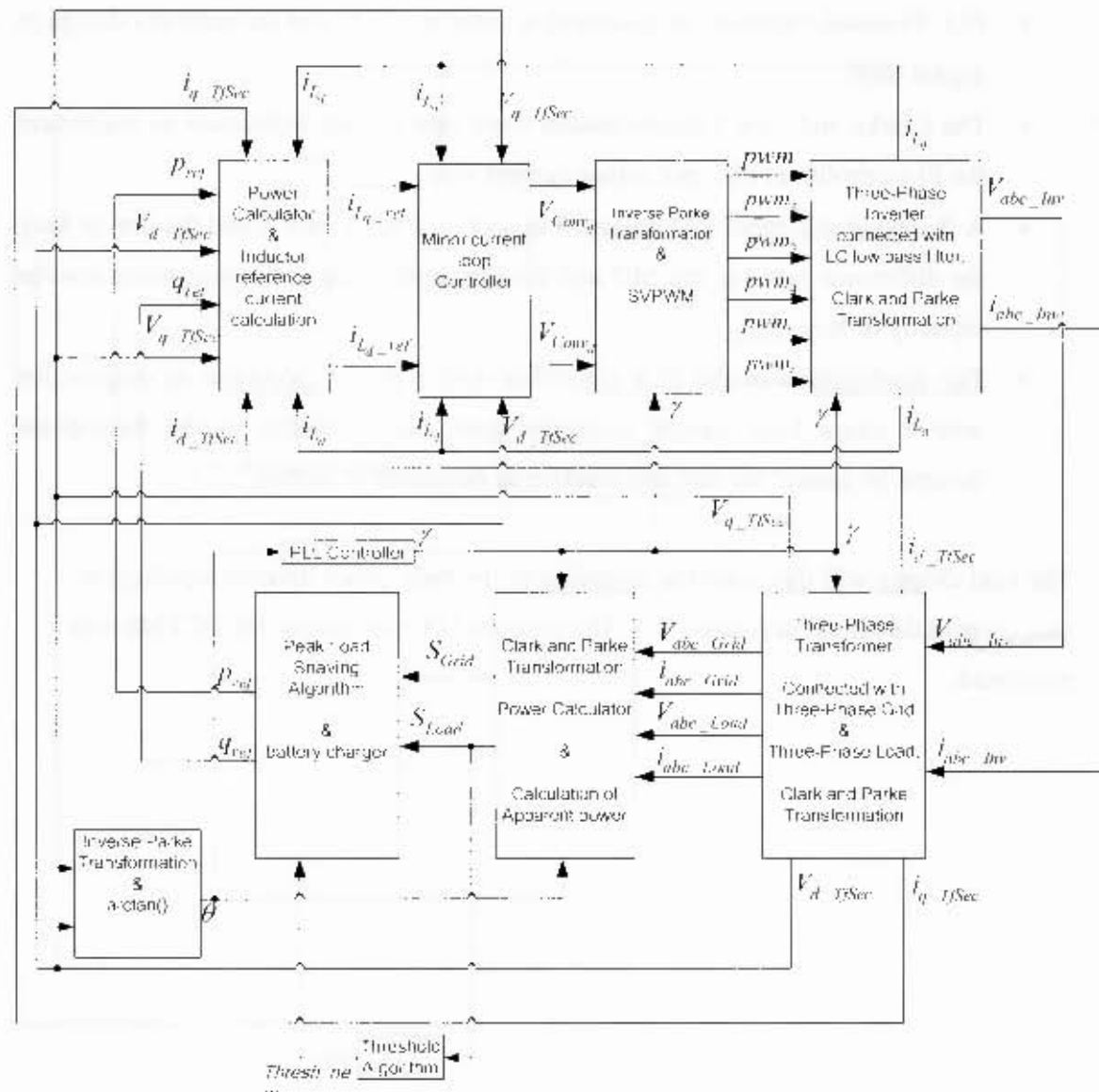


Figure 3.4.4.2-2: complete control design block diagram for peak load shaving

### 3.5 Chapter Summary

From the above discussion, the following points are summarized:

- Using the three-phase inverter as CSI, improves the three-phase inverter current quality and hence the power quality being delivered by the three-phase inverter as discussed in reference [11].
- PLL PI-based controller as discussed in reference [14] was successfully design in digital form.
- The Clarke and Park Transformation were very crucial techniques to implement the PI controller in PLL and minor current loop.
- A threshold algorithm was designed in section 3.4.4.1, and it had the aim to keep the difference between the MD and the threshold value at the maximum inverter capacity or less.
- The combination of the PLS algorithm with a power calculator in conjunction with a minor loop current controller gave the possibility of the three-phase inverter to control the real and reactive as discussed in section 2.3.1

The next chapter will discussed the modeling of the three-phase inverter topology in simplorer as described in figure 3.3-1. The proposed PLS technique for UCTMS was simulated.

## **4 Modeling and simulation of chosen topology in Simplorer Version 7 to identify control algorithm for peak shaving and provide foundation for control software**

The procedure to simulate the chosen three-phase topology for PLS followed the followings steps:

- Modeling of the three-phase supply as will be discussed in section 4.1.
- Modeling of the three-phase load as will be discussed in section 4.2
- Modeling of the three-phase inverter as will be discussed in section 4.3.
- Modeling of the three-phase transformers as will be discussed in section 4.4
- Modeling of the battery as will be discussed in section 4.5
- Finally, modeling of the low pass filter as will be discussed in section 4.6.

When the entire models were ready and assembled, the next step was to simulate the following: PLL PI-based controller as was discussed in section 3.4.1.2 in continuous mode. Simulation of the inner current controller i.e. the low pass filter inductors currents as was discussed in section 3.4.2. Simulation of the real and reactive power as was discussed in section 3.4.3.

Thereafter, simulation of the SVPWM to switch the IGBT gates; finally, simulation of the PLS by charging the battery below a set threshold and discharge the battery when the load demand goes above the set threshold as discussed in section 3.4.4.

### **4.1 Modeling of the three-phase supply**

The three-phase source was modeled with a three single-phase sources, phase shifted by 120 degree from each other. Positive sequence connection was chosen to reflect the actual three-phase source connection, refer photo 5.1.1-1. In positive sequence connection,  $V_A$  leads  $V_B$  by  $120^\circ$  and in turn,  $V_B$  leads  $V_C$  by  $120^\circ$  (where  $V_A$ ,  $V_B$

and  $V_C$  are line to neutral voltage), Figure 4.1-1 below, shows the connection of the three-phase source in the simplorer.

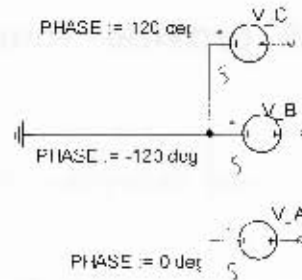


Figure 4.1-1: three-phase source representation in Simplorer

The red dots represent the flow of the current in this case from left to right [28]. Figure 4.1-2 shows the voltage source input parameter panel.

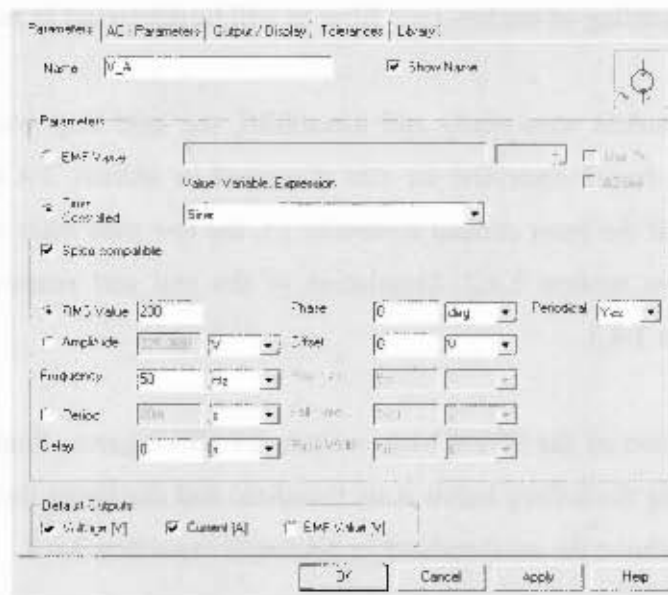


Figure 4.1-2: Voltage source input parameter in simplorer simulation

The three-phase source as it is shown on the figure 4.1-1 was set to 230V rms line to neutral with frequency of 50Hz in the voltage source panel in figure 4.1-2. The three-phase voltage signals are illustrated on figure 4.1-3.

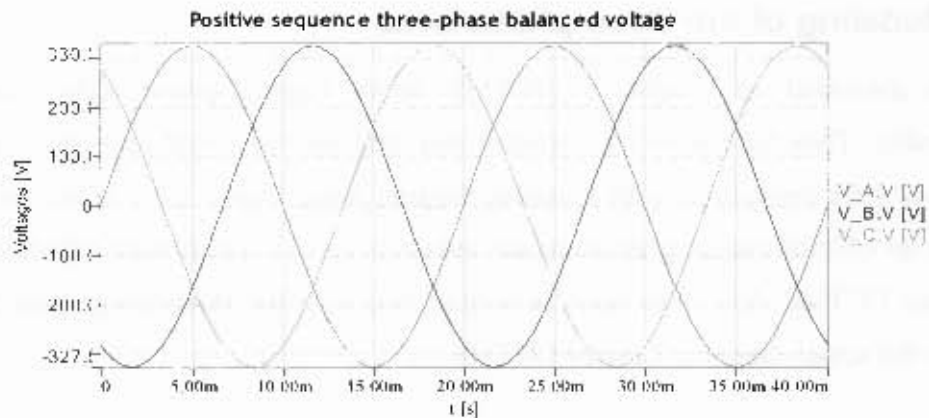


Figure 4.1-3: Positive sequence Three-phase Balanced Source

From figure 4.1-3, it can be seen that the three-phase supply was following positive sequence connection as described above. The signals for calculation were acquired using the meters provided by simplorer such as the voltmeter, ammeter. Table 4.1-1 was taking directly from reference [28].

Table 4.1-1 shows the meters and electrical sources, it helps to see the direction flow of the current and the voltage direction in each element simplorer uses. The results of table 4.1-1 were very important one for the control design.

Table 4.1-1: Simplorer Reference arrows system [28]

	Voltage Sources	Current Sources	Passive Components
Electrical			
Meters	<b>Voltmeter</b> 	<b>Ammeter</b> 	<b>Wattmeter</b> 

The three-phase source was modeled as ideal voltage source for simplicity. In the next section, we will discuss the three-phase load modeling.

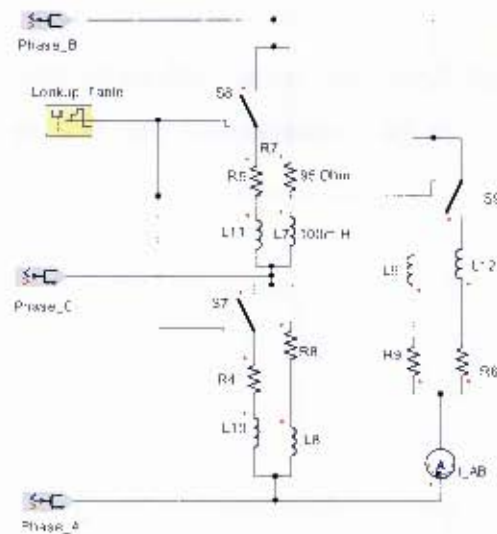


Figure 4.2.1-1: Three-phase Delta connected Load modeled in simplorer

The switches to increase the load in figure 4.2.1-1 were controlled by a look-up table. The good thing about look-up tables was that it could produce any shape of signals, from a sinusoidal waveform, polynomial, etc. to random shape depending on the user choice. Thus, the waveform used was a simple pulse, which gave zero (off) and one (on) to the switches. Figure 4.2.1-2 shows the look-up table panel.

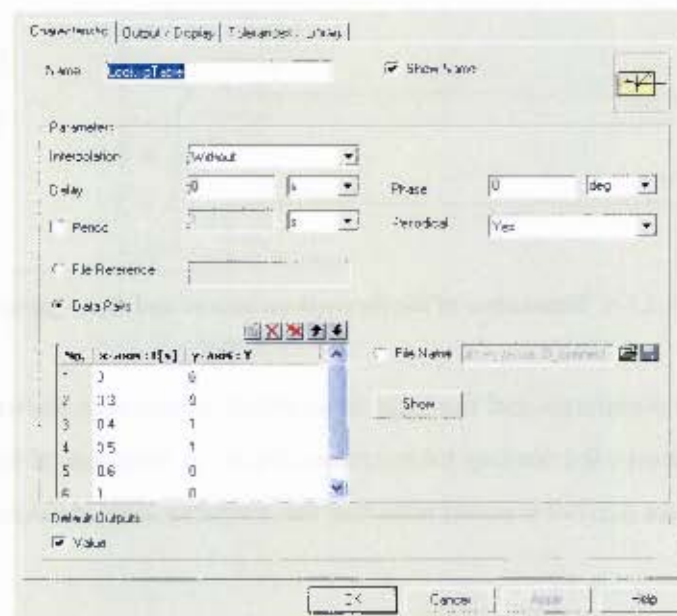


Figure 4.2.1-2: Look up table properties panel in Simplorer

In figure 4.2.1-2, the interpolation was set to without to allow the transaction of the switch from “off” to “on” to be instantaneous. The look-up table characteristic is illustrated in figure 4.2.1-3



Figure 4.2.1-3: Pulse signal to switch the extra load on and off

The three-phase source and load were ready to be connected; figure 4.2.1-4 shows their connection.

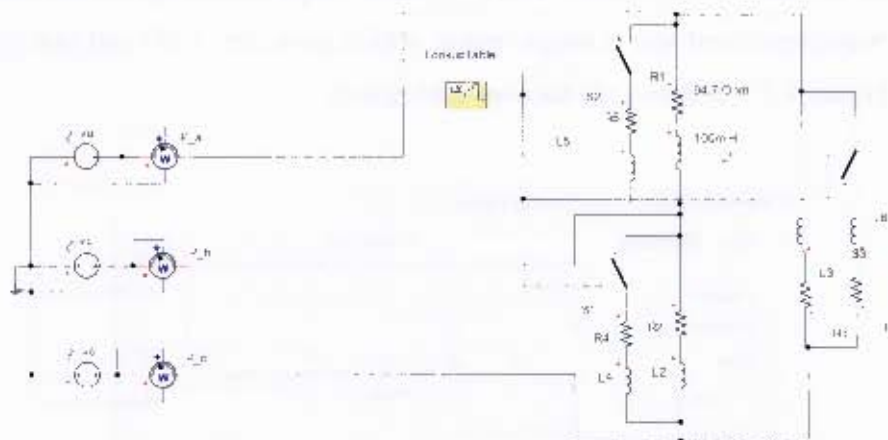


Figure 4.2.1-4: Simulation of the three-phase source and three-phase load

Figure 4.2.1-4 was simulated and the total three-phase power was shown in figure 4.2.1-5. Figure 4.2.1-6 shows the lookup table characteristic as function of time. When it was compared with figure 4.2.1-4 it could be seen that the switches were working fine.

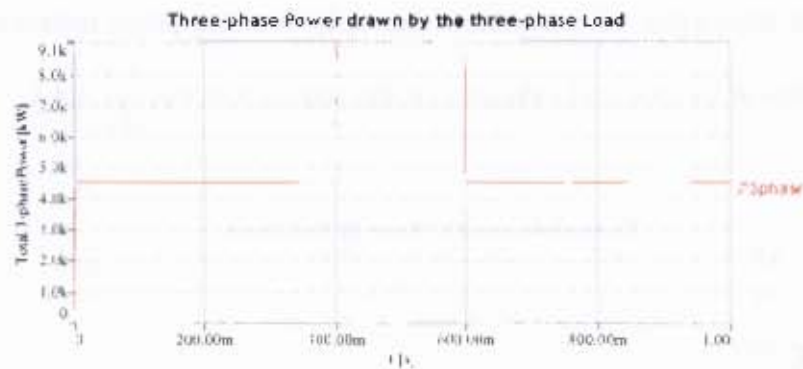


Figure 4.2.1-5: Three-phase Power drawn by the three-phase Load

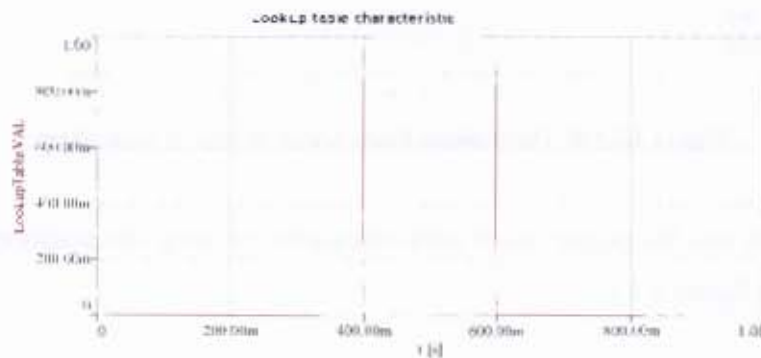


Figure 4.2.1-6: Lookup table pulse characteristic

Figure 4.2.1-7 depicts the PF that the chosen resistor and inductor yielded.

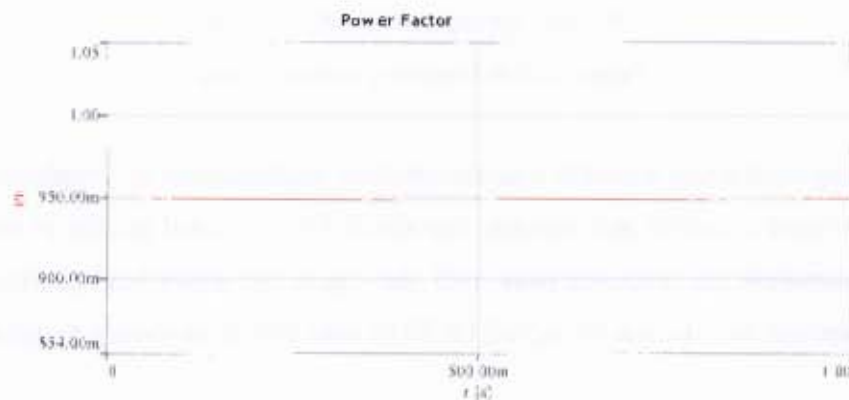


Figure 4.2.1-7: Simulated power factor of 0.95

Figure 4.2.1-8 shows that the rms current drawn by the each phase inductor was below the rated current of the practical inductors i.e. the rms current was  $\frac{5.7}{\sqrt{2}} = 4.4$ .

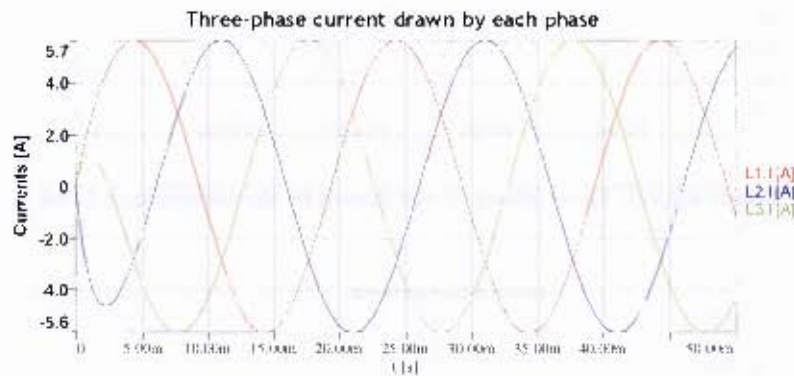


Figure 4.2.1-8: Three-phase load current drawn by each phase

The total power and the power factor were calculated by using the equation block, which is illustrated in figure 4.2.1-9.

Equation\_Block

EQU

$$P_{3\text{phase}} = P_{a.P} + P_{b.P} + P_{c.P}$$

$$X_L = 2 \cdot \pi \cdot 50 \cdot L \cdot L$$

$$PF = \cos( ( \pi \cdot \text{deg}(\text{atan}( X_L / R1.R )) ) / 180$$

Figure 4.2.1-9: Simplorer equation block

The changing load using a switch was successfully implemented in Simplorer; however, there was a need to model and simulate the actual UCTMS load profile in simplorer, to be able to simulate the proposed peak load shaving in the actual load profile. Thus, the following section will discuss the actual UCTMS load profile modeling in detail.

#### **4.2.2 Modeling of the actual changing load profile of UCTMS in Simplorer**

Using the actual data and specifically the December load profile data, the resistor and the inductor values were calculated (refer to the accompanied CD). These changing resistors and inductors values represent the total changing of the equivalent load impedance for all UCTMS substations, seen as one load. The procedure taken will be described below.

From section 2.3.3, it was discussed that the metering system gathered the three-phase average apparent, real and reactive power for UCTMS for a period of eight month. Furthermore, it was discussed that the PF was calculated using equation (2.3-1). For this section, the three-phase real and reactive power and the PF for the December month were used to calculate the changing in resistors and inductors.

The power entering the bus bar in electrical department substation for medical school, see figure 2.1-1 section 2.1, comes from the CTM. Figure 4.2.2-1 illustrates the CTM and all UCTMS substations as illustrated in figure 2.1-1 in section 2-1

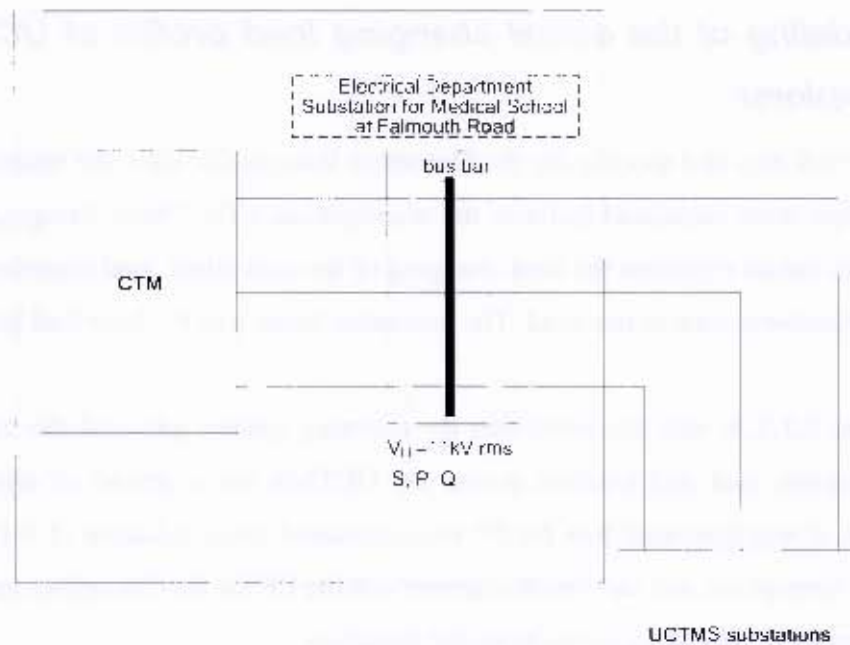


Figure 4.2.2-1: Simplified UCT medical school substation represented as block diagram

As was discussed previously in chapter 2, the measurements were done at the bus bar point as shown in figure 4.2.2-1. The bus bar can be seen as the new supply point for the UCTMS loads. Thus, figure 4.2.2-1 can be represented as figure 4.2.2-2.

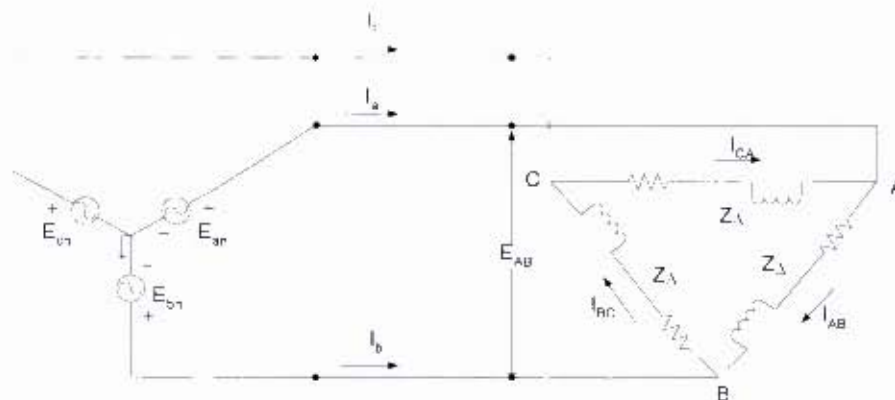


Figure 4.2.2-2: Simplified UCT medical school substation represented as circuit diagram

In this configuration, the CTM and the bus bar were shown as a balanced-Y three-phase source. All UCTMS substations were illustrated as a three-phase balanced- $\Delta$  load, and

this was because the high sides of the three-phase transformers as illustrated in figure 2.1-1 in section 2.1, were connected as delta configuration and its voltage line to line was 11kV rms. In figure 4.2.2-2  $E_{AB}=11\text{kV rms}$ .

The total load impedance,  $Z_{\Delta}$  is defined as shown in equation (4.2.2-1)

$$Z_{\Delta} = R + jX_L \quad (4.2.2-1)$$

The inductor values was calculated using equation (4.2.2-2) at frequency of 50Hz

$$X_L = 2\pi \cdot f \cdot L \quad (4.2.2-2)$$

In balanced three-phase delta load, the three-phase apparent power was equal to the sum of the phase's apparent power [7, 29]. Assuming a balanced three-phase delta load, the three-phase apparent power was represented as shown in equation (4.2.2-3).

$$S_{3-\theta} = S_{AB} + S_{BC} + S_{CA} = 3 \cdot S_{AB} \quad (4.2.2-3)$$

Where  $S_{AB}=S_{BC}=S_{CA}$  for balanced three-phase delta load. The apparent power in phase AB was defined as shown in equation (4.2.2-4) [29].

$$S_{AB} = P_{AB} + jQ_{AB} \quad (4.2.2-4)$$

Where,  $P_{AB}$  and  $Q_{AB}$  are the real and reactive power of the phase AB, which could also be defined as illustrated in equations (4.2.2-5) and (4.2.2-6) [29].

$$P_{AB} = V_{AB_R} \cdot I_{AB} = R_{AB} \cdot I_{AB}^2 = \frac{V_{AB_R}^2}{R_{AB}} \quad (4.2.2-5)$$

$$Q_{AB} = V_{AB_{XL}} \cdot I_{AB} = X_{L_{AB}} \cdot I_{AB}^2 = \frac{V_{AB_{XL}}^2}{X_{L_{AB}}} \quad (4.2.2-6)$$

Noticing that in the series connected circuit, the current is the same for both components, but the voltage is shared between them. Thus looking on branch AB of figure 4.2.2-2, the voltage across it was defined as shown in equation (4.2.2-7).

$$V_{AB} = V_{AB_R} + jV_{AB_{XL}} \quad (4.2.2-7)$$

Where for a balanced three-phase delta load,  $V_{AB}=V_{BC}=V_{CA}$ . The voltage  $V_{AB_R}$  and  $V_{AB_{XL}}$  represents the voltage across the resistor and the inductor respectively.

From literature the phase angle between the voltage current triangle is the same as the power triangle and as well as the angle between the resistor component and the reactance [29]. As discussed above the current flowing through for both resistor and inductor in each phase was the same. Consequently it was chosen as the reference for the voltage current triangle shown in figure 4.2.2-3.

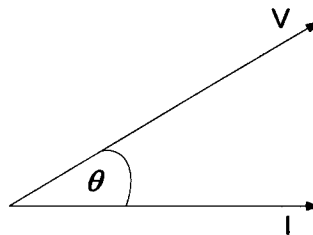


Figure 4.2.2-3: Voltage Current triangle

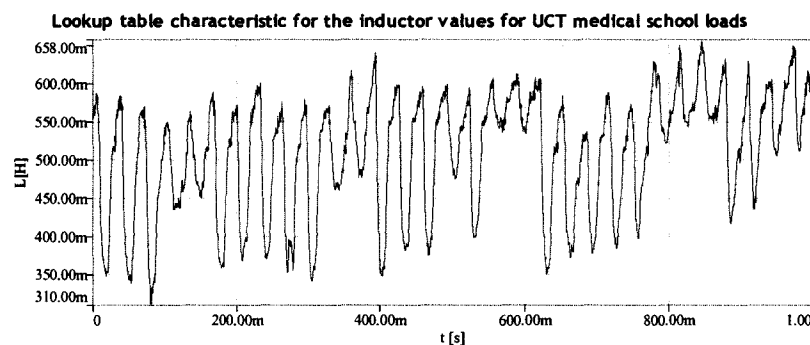
The angle  $\theta$  is the PF angle. With this in mind, the resistor voltage and the reactance voltage were calculated for each value of the PF using the equations (4.2.2-8) and (4.2.2-9).

$$V_{AB_R} = V_{AB} \cdot \cos \theta \quad (4.2.2-8)$$

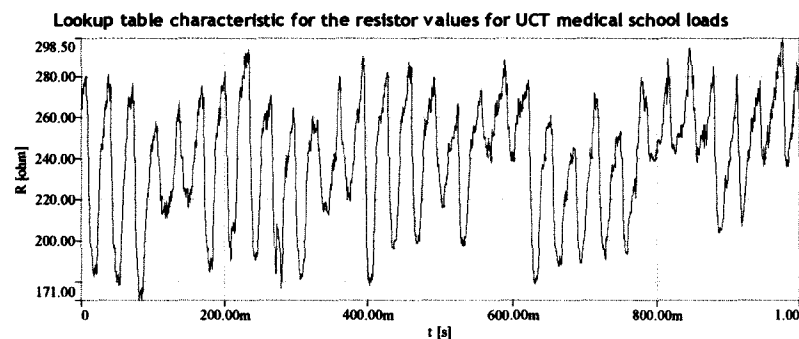
$$V_{AB_{XL}} = V_{AB} \cdot \sin \theta \quad (4.2.2-9)$$

Using the above equations (4.2.2-2), (4.2.2-5), (4.2.2-6), (4.2.2-8) and (4.2.2-9)  $R_{AB}$  and  $L_{AB}$  were calculated. The resistor and reactance for the other branches used the same value as branch AB because a balanced three-phase load was assumed.

The resistors and inductors values were loaded in a lookup table to be able to change the load resistors and inductors in each phase of the three-phase delta load. This procedure helped to mimic UCTMS load profile. Figures 4.2.2-4 and 4.2.2-5 shows the inductors and resistors characteristic values respectively.



**Figure 4.2.2-4: UCTMS load inductor values**



**Figure 4.2.2-5: UCTMS load resistor values**

Figure 4.2.1-4 was changed to figure 4.2.2-6. In this configuration, the load inductor and resistor values were changed according to figure 4.2.2-4 and 4.2.2-5 respectively.

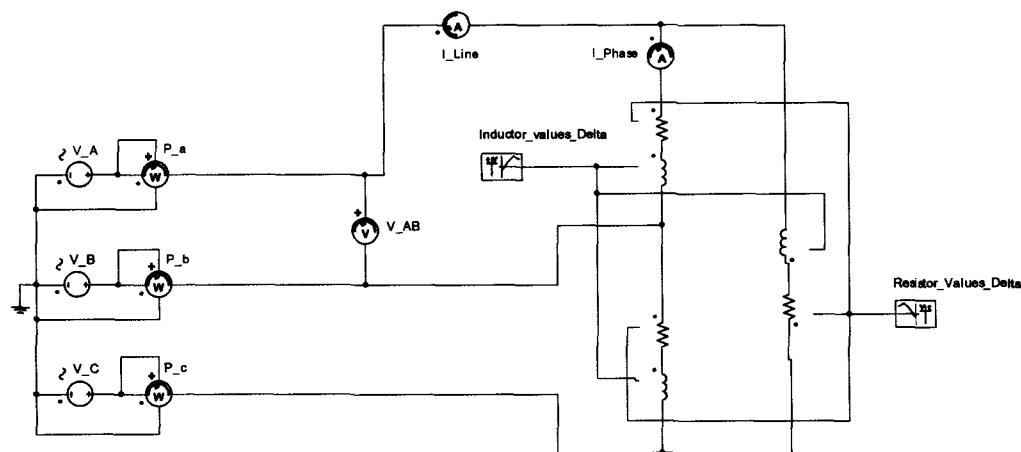


Figure 4.2.2-6: Simulation of UCT medical school load profile

The voltage line to neutral  $V_A$ ,  $V_B$  and  $V_C$  was changed to  $\frac{11k}{\sqrt{3}}$  V rms. The three-phase power drawn by the load was the summation of  $P_a$ ,  $P_b$  and  $P_c$  as illustrated in figure 4.2.1-8. Figure 4.2.2-6 was run and the three-phase power drawn by the load was shown in figure 4.2.2-7.

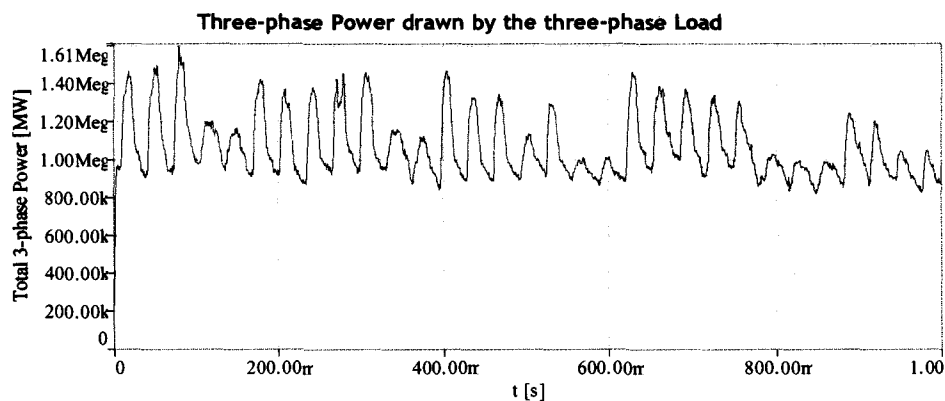


Figure 4.2.2-7: Simulated three-phase real power drawn by UCT medical school

Using the real data for UCTMS, the real three-phase power, drawn by the UCTMS for the month of December was plotted in excel, so that it could be compared with simulated one. Figure 4.2.2-8 shows this.

### Real three-phase power delivered by the public utility

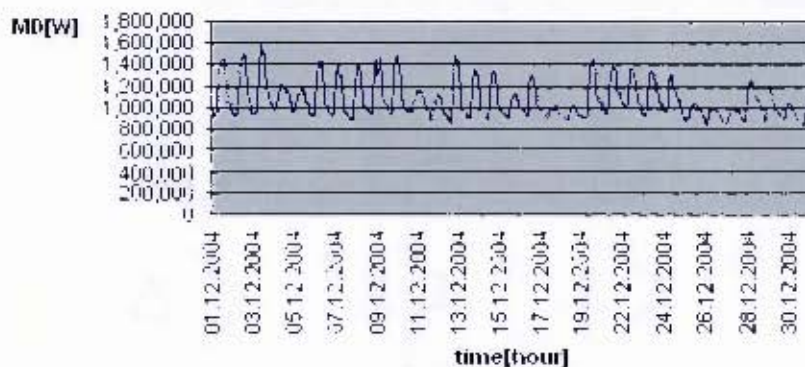


Figure 4.2.2-8: Three-phase real power drawn by UCT medical school

From the above discussion, UCTMS load profile was successfully simulated in simplorer. In the next section, the modeling of the three-phase inverter will be discussed.

### 4.3 Modeling of the three-phase Inverter

The three-phase inverter used in practice was made of Insulated Gate Bipolar Transistors (IGBT) semiconductors manufactured by SEMIKRON. Simplorer offers SEMIKRON model and surprisingly the same type used in practice, the SKM 200GB123D. Figure 4.3-1 illustrates this.

SKM200GB123D1

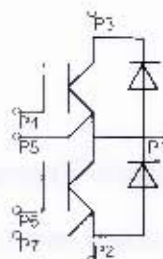


Figure 4.3-1: Simplorer IGBT SEMIKRON model SKM 200GB123D

Several attempts were taken to incorporate the IGBT SEMIKRON model to the simulation but with no success. Because of time constraint, simple IGBTs and diodes

components were used to construct the three-phase inverter. Using reference [12] the three-phase inverter was constructed. Figure 4.3-2 illustrates this.

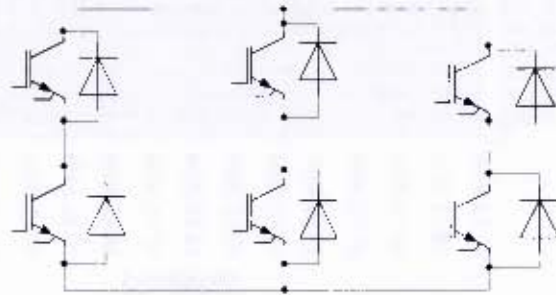


Figure 4.3-2: three-phase inverter models in Simplerer

The IGBTs and diodes components used were of systems level type and from simplerer online help [30] it was stated that they were used to simulate static voltage-current relation. In addition, it was also mentioned, “each voltage causes a corresponding current depending on the selected characteristic” [30].

Moreover it was claimed that the “predefined characteristics defined within the component dialog guarantee a high calculation speed” [30]. Therefore, figure 4.3-2 was used in the simulation. The characteristic used for both IGBTs and diodes components were an exponential predefined characteristic.

The SPWM was used in conjunction with a 10kHz triangle waveform to switch the IGBT gates. It will be discussed later.

#### 4.4 Modeling of the three-phase Transformer

The three-phase transformer used in practice had the following rating: 4.5kVA 400/55.4 Y-A line-to-line rms. It was composed by three single-phase three winding transformer with followings ratings: 1.5kVA 230/55.4.

No-Load test and short circuited test were done in each one of the single-phase three winding transformer, refer to appendix F section F.3. Furthermore, modeling the

transformers in Simplorer, the No-Load and shorted circuit test results were used. The no-load and shorted circuit result are presented in appendix F section F.3.

#### 4.4.1 Single-Phase Transformer in Simplorer

In the hardware section, the practical single-phase three windings transformer, even though it had three windings, only two windings were used; refer to photo 5.1.6-1. For this reason, in Simplorer a linear two windings transformer was used in simulation.

Figure 4.4.1-1 illustrates the linear two winding transformer schematic in Simplorer.

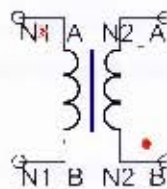


Figure 4.4.1-1: linear two winding transformer

Figure 4.4.1-1 in fact represents a practical single-phase two winding transformer. Using reference [31], the linear two winding transformer of figure 4.4.1-1 was explained in detail. Figure 4.4.1-2 illustrates figure 4.4.1-1 content as discussed in reference [31].

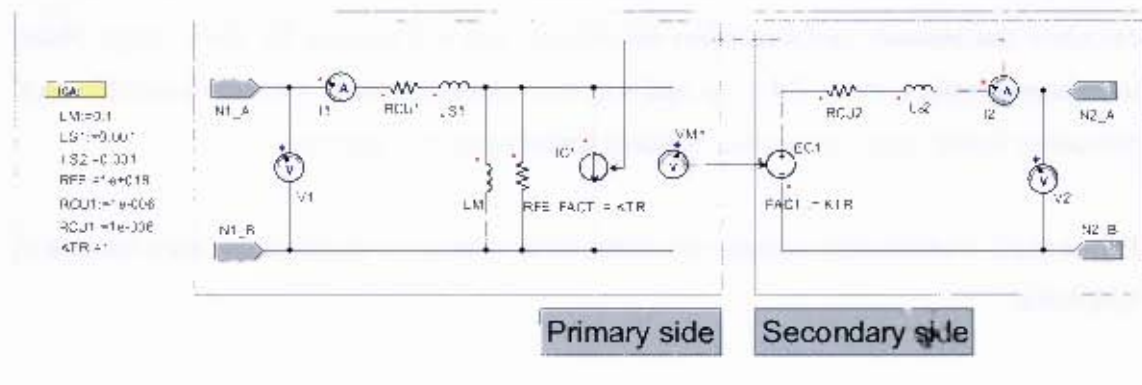


Figure 4.4.1-2: linear two winding transformer contents, [31]

Figure 4.4.1-3 shows the input parameters panel of figure 4.4.1-1 and figure 4.4.1-2.

Figure 4.4.1-3: Linear Two-winding transformer input panel for transformer A

In figure 4.4.1-3,  $KTR$  is the turn ratio, which was defined as

$$KTR = \frac{W2}{W1} = \frac{55.4V}{230V} \quad (4.4.1-27)$$

Each respective calculated No-load and shorted-circuit parameters values for the practical single-phase transformer A, B and C, see tables F.3.2-1 to table F.3.2-3 , were used to calculate the primary and secondary resistances and inductances for each single phase transformer, refer to table F.4-1. In addition, the values of table F.4-1 were loaded in each respective linear single-phase two-winding transformer in simplorer.

Figure 4.4.1-4 shows the connections of the three individual single-phase transformers in simplorer.

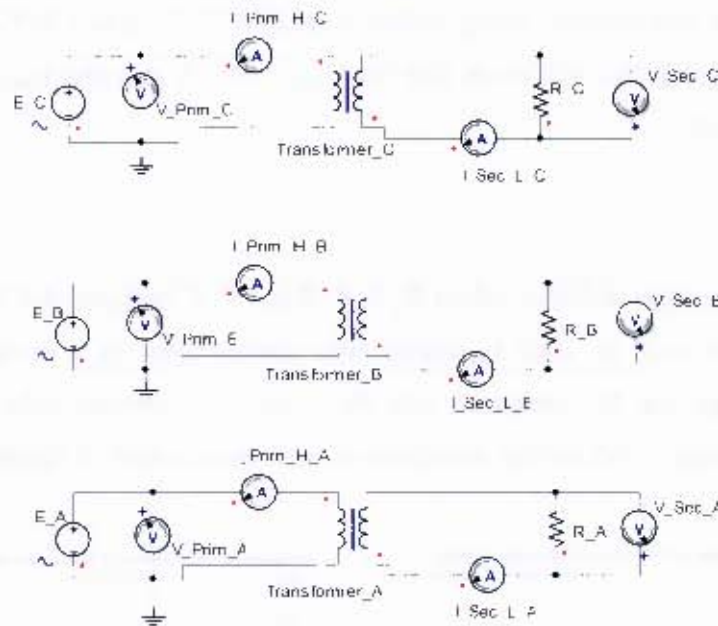


Figure 4.4.1-4: Single-phase transformers A, B and C

The sinusoidal AC source in each transformer was set to 230V rms and was connected to the primary side of each transformer. The measurement sensors, the voltmeter, ammeter and passive component, resistors were connected in the way shown in figure 4.4.1-4 to obey the rule of the current flow and voltage direction as illustrated in table 4.1-1.

Moreover, the current entering the red dot of the primary side of the single-phase transformer is in phase with current leaving the red dot on the secondary side of the single-phase transformer [7]. Similarly, the voltage on the primary side is in phase with the voltage in secondary side when measured from the red dot respectively as shown in figure 4.4.1-4.

Two scenarios were tested in simulation to check if the responses coincide with real single-phase transformer behavior in terms of primary and secondary voltages relation as well as primary and secondary current relation.

The single-phase transformers rating values were 230/55.4V rms 1.5kVA as mentioned previously. Therefore this will mean that the  $I_{1,max} = 6.52A$  rms and  $I_{2,max} = 27.07A$  rms, where  $I_1 = I_2 \cdot KTR$ .

### Scenario1:

In the first scenario the resistors values  $R_A$ ,  $R_B$  and  $R_C$  in figure 4.4.1-4 were set to a very big number such as  $1G\Omega$  to mimic zero current flow or a no-load so that the secondary voltage can be compared with the voltage in primary side. Figure 4.4.1-5 illustrates the voltages and current waveform of each transformer of figure 4.4.1-4.

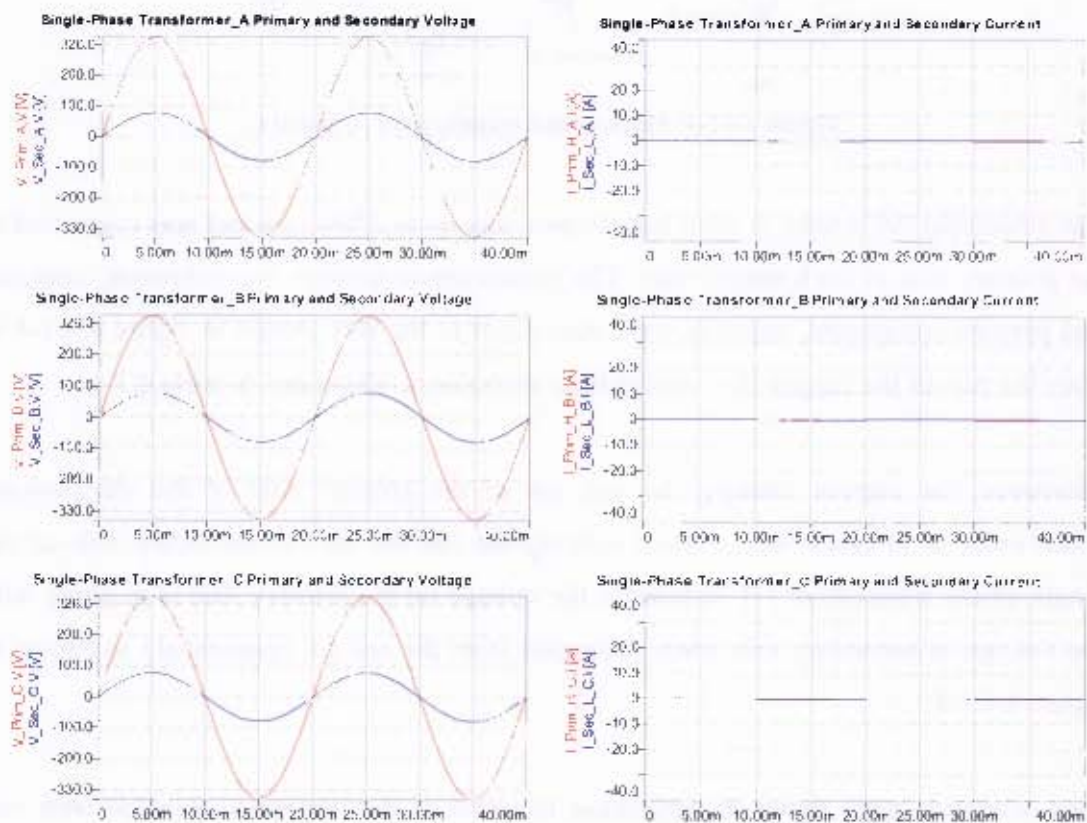


Figure 4.4.1-5: Single-phase transformers A, B and C voltage and current waveform at no-load

Figure 4.4.1-6 shows the voltage and current rms value and many more. However, the focus in figure 4.4.1-6 is the rms values of the voltages and currents.

	V_Primary[V]	V_Sec_C[V]	V_Sec_B[V]	V_Primary[V]	V_Sec_A[V]	V_Primary[V]
Maximum	325.247744416728	78.1661919486118	78.375197199265	325.247744416728	78.3597647753783	325.247744416728
Minimum	-325.127019308068	-78.1627597514254	-78.3724330964042	-325.127019308068	-78.3826262921678	-325.127019308068
Peak to Peak	650.374763724796	156.348951700037	156.747630295669	650.374763724796	156.742391067546	650.374763724796
Mean Value	-85.2203020008356m	-42.8176677102465m	-33.4377876144533m	-85.2203020008356m	-46.0007516475932m	-85.2203020008356m
Rectified Mean	206.783087171416	49.7101521992123	49.8369728367891	206.783087171416	49.8352249007115	206.783087171416
R.M.S. value	229.879123895151	55.2623729609931	55.4033623281837	229.879123895151	55.4014148956321	229.879123895151
R.M.S. AC	229.879123895171	55.2623563732765	55.4033522377696	229.879123895171	55.4013957580195	229.879123895171

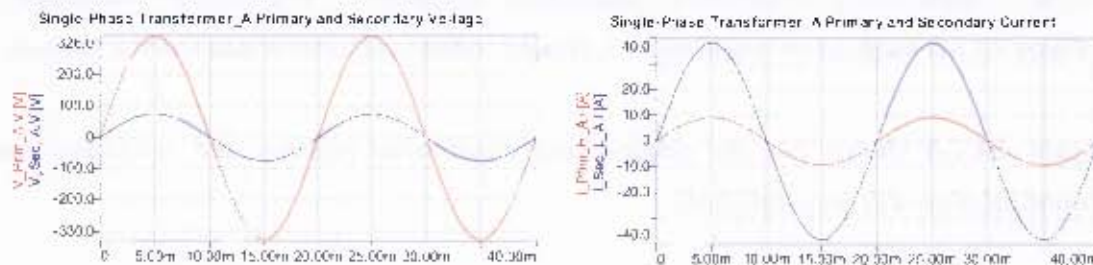
	I_Primary[A]	I_Sec_C[A]	I_Primary[A]	I_Sec_B[A]	I_Primary[A]	I_Sec_A[A]
Maximum	217.909247892569m	78.1661919486118m	141.321069864337m	78.375197199265m	262.047728475714m	78.3597647753783m
Minimum	-12.52155429627...m	-78.1827597514255m	-17.2924347974031m	-78.3724330964042m	-10.7377718797194m	-78.3826262921678m
Peak to Peak	230.430802138545m	156.348951700037m	158.61350466174m	156.747630295663m	272.785500355433m	156.742391067546m
Mean Value	102.756615488734m	-42.8176677165479p	62.02467655026203m	-33.4377876144217p	125.724414329846m	-46.0007516477639p
Rectified Mean	105.196645064849m	49.7101521992113m	66.8898177795285m	49.8369728367892m	127.481150578128m	49.8352249007109m
R.M.S. value	131.082748871431m	55.2623729609927m	83.5950800281399m	55.4033623281837m	156.371358058793m	55.401414895632m
R.M.S. AC	81.3865162357455m	55.2623563732781m	56.0486311947419m	55.4033522377695m	96.3060677951933m	55.4013957580144m

Figure 4.4.1-6: Single-phase transformers A, B and C voltage and current data result at no-load

In figure 4.4.1-6, it was noticed that the primary rms voltages in each transformer were the same but the secondary rms voltages were not and this was because of the difference in the parameter values that were set in each transformer. Nevertheless, the primary and secondary voltage relation was accomplished.

### Scenario 2:

In scenario 2, a resistor value was chosen to give the rated maximum current of the single-phase transformers. The resistor value chosen was  $1.955\Omega$ . Figure 4.4.1-7 illustrates each transformer result at full load.



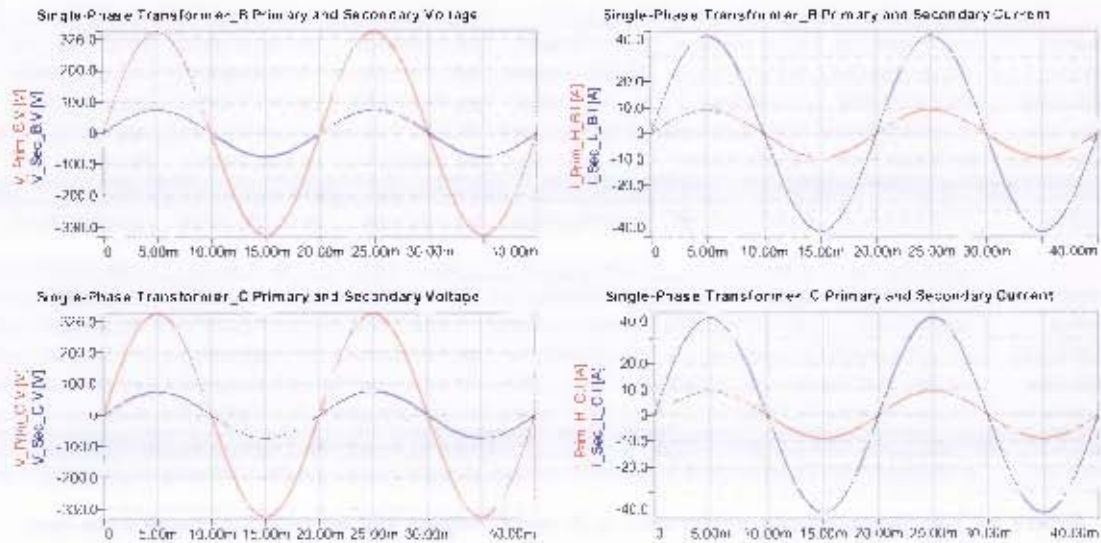


Figure 4.4.1-7: Single-phase transformers A, B and C voltage and current waveform at full-load

	V_Primary[V]	V_Secondary[V]	V_Secondary[V]	V_Primary[V]	V_Secondary[V]	V_Primary[V]
Maximum	325.228717911556	74.1923478741255	74.5530294322575	325.228717911558	74.6361097703314	325.228717911558
Minimum	-325.248548435185	-74.2340067729359	-74.5788665005469	-325.248548435185	-74.67726375045	-325.248548435185
Peak to Peak	650.477266346743	148.426354647061	149.13169932804	650.477266346743	149.313373520781	650.477266346743
Mean Value	-10.7057321038946m	-23.066875316783m	-14.4095373889667m	-10.7057321038946m	-25.9171146821422m	-10.7057321038946m
Rectified Mean	206.710647604089	47.16731656162	47.3914778206922	206.710647604089	47.4475081079504	206.710647604089
R.M.S. value	229.807248560414	52.4374641259367	52.6886662329171	229.807248560414	52.751122674437	229.807248560414
R.M.S. AC	229.807248311047	52.4374590515777	52.688664262449	229.807248311047	52.7511163078275	229.807248311047

	I_Primary[A]	I_Secondary[A]	I_Primary[A]	I_Secondary[A]	I_Primary[A]	I_Secondary[A]
Maximum	9.27595941325108	37.9500500634913	9.30146273007227	38.1345419090831	9.37663620426902	38.1770382456938
Minimum	-9.07984695241238	-37.9713589631386	-9.18220600570647	-38.147655499001	-9.13649332351531	-38.1980888749105
Peak to Peak	18.3558054656635	75.9214092266299	18.4836687357787	76.2821974080841	18.5131295278043	76.3751271206043
Mean Value	97.4429653832538m	-11.7999362234155m	58.8137552672393m	-7.37060766699212m	119.696174749072m	-13.2564361545494m
Rectified Mean	5.83315156169678	24.1265046350997	5.87369961782949	24.2411651256738	5.88322537789373	24.2708482905322
R.M.S. value	6.48524948064223	26.8222322394817	6.53029465168389	26.9497013979115	6.54102316684363	26.9826714447504
R.M.S. AC	6.48451739132772	26.8222296939016	6.53002979931365	26.9497003899995	6.53992789675855	26.982668168147

Figure 4.4.1-8: Single-phase transformers A, B and C, voltage and current data result at full-load

Figure 4.4.1-8 shows that the single-phase transformer primary and secondary rms current relation was accomplished.

The three single-phase transformers were ready to be connected as Y- $\Delta$  three-phase transformer. The following section will briefly discuss its connection.

#### 4.4.2 Three-Phase Y- $\Delta$ Transformer in Simpler

The three-phase Y- $\Delta$  transformer was connected as explained in [7] and illustrated in appendix F section F.5. Figure 4.4.2-1 illustrates the connection in simpler.

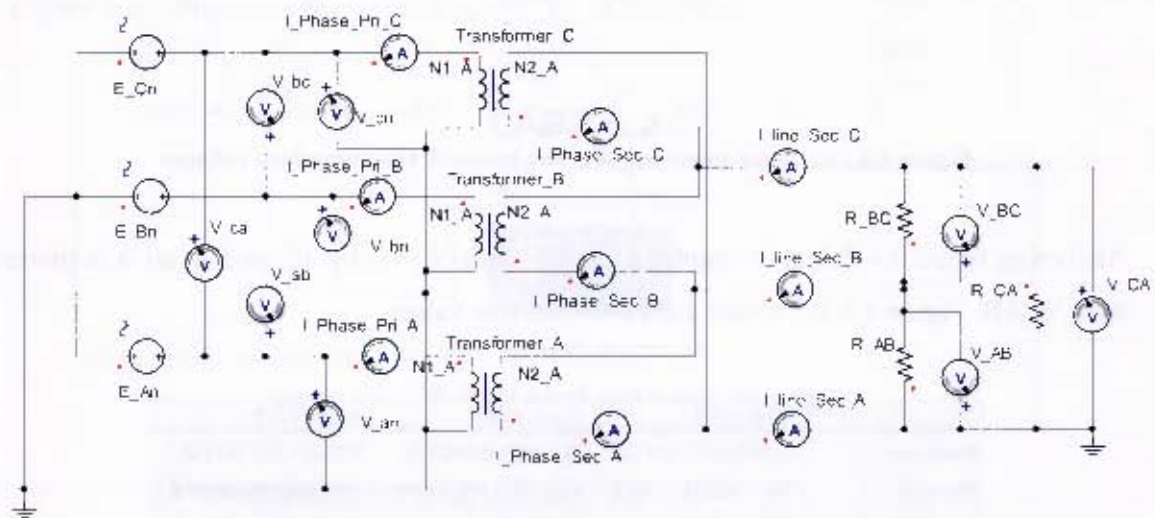


Figure 4.4.2-1: Three-phase Y- $\Delta$  transformer in Simpler, it was assembled using three single-phase linear transformers.

From reference [7] was discussed that in the three-phase Y- $\Delta$  transformer the Y line to line voltage,  $V_{ab}$ , leads the  $\Delta$  line to line voltage  $V_{AB}$  by  $30^\circ$ , however it was also stated that the Y line to neutral voltage,  $V_{an}$ , is in phase with  $\Delta$  phase voltage  $V_{AB}$ . It is good to notice that the  $\Delta$  line-to-line voltage is the same as the  $\Delta$  phase voltage [7]. Figure 4.4.2-2 shows the Y line-to-line voltage,  $V_{ab}$ , the Y line to neutral or phase voltage,  $V_{an}$  and the  $\Delta$  line to line or phase voltage,  $V_{AB}$ .

practice. The battery in practice had a capacity of 102Ah for 20h, thus the mean value of the discharging current was 5.1A per hour.

In Simpler the lead-acid battery model, its capacity was rated for 10h, which would give 10.2A per hour. The mean value of discharge current was set 10.2A. The initial value of charge rate was set to 30% of the rated capacity of the battery, which came to be 30.6Ah.

#### 4.6 Modeling of the low pass filter

The aim of low pass filter was to block high frequency to go through and allow only the frequency below the cut-off frequency to go through, which ideally had to be only the fundamental frequency. The low pass filter used was made of inductors and capacitors.

Figure 4.6-1 below illustrates a single-phase LC low-pass filter.

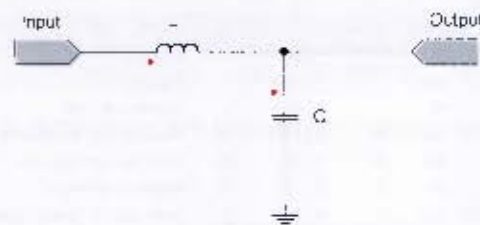


Figure 4.6-1: Single-phase representation of LC low pass filter

In figure 4.6-1, the input signal came from the three-phase inverter, and it is composed of the fundamental frequency plus the switch frequency signal and its harmonics. The choice of the inductor and capacitor values had to be such that only the fundamental goes through with a little distortion possible.

The inductor and the capacitor can also be represented as impedances. Equations (4.6-1) and (4.6-2) illustrates this.

$$X_L = \omega L = 2\pi fL \quad (4.6-1)$$

$$X_c = \frac{1}{\omega C} = \frac{1}{2\pi fC} \quad (4.6-2)$$

The capacitor of 50 $\mu$ F was chosen due to its availability in practice. The fundamental frequency of the signal was 50Hz; the switch frequency was chosen to be 10 kHz as mentioned before.

The cut-off frequency has to be big enough to allow the fundamental frequency signal through and small enough to prevent the unwanted harmonic at switch frequency to pass through. A cut-off frequency of 1 kHz was chosen, which by using equation (4.6-3) below, yielded  $L=506.6 \times 10^{-6}$  H

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (4.6-3)$$

When the value of L and C as calculated above are used in the equations (4.6-1) and (4.6-2) respectively, at fundamental frequency, it could be seen that the capacitor had a big value of the reactance compared with the inductor. This meant that the big capacitor reactance would prevent the fundamental current signal to flow through the capacitor, thus the fundamental current signal would be transferred to output through the inductor.

Conversely, at switch frequency the capacitor would behave as a short circuit with a very small reactance value, while the inductor reactance value would be much bigger in relation with the capacitor reactance, thus the opposite would happen.

Figure 4.6-2 shows the low pass filter response as discussed in [33]

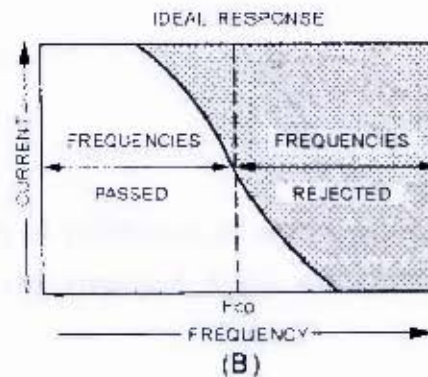


Figure 4.6-2: Low-pass filter response [33]

#### 4.6.1 Three-phase Low-pass filter

The three-phase low-pass filter in a three-phase system can be assembled in two ways: firstly, the filter capacitor can be connected to the neutral point, which would mean that the voltages across the capacitors would be the line to neutral voltages, or secondly, each capacitor could be connected across two phases in the three-phase system not requiring a neutral point. In this way the capacitors connections would form a delta connection, which would go well with the three-phase transformer delta connection. The topology is illustrated in figure 4.6.1-1.

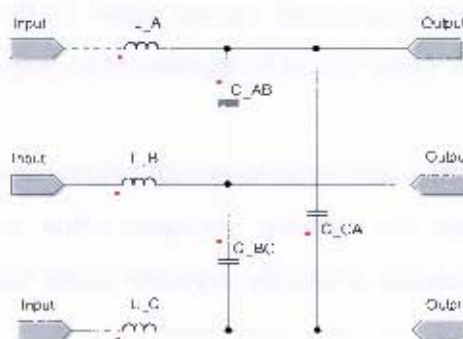


Figure 4.6.1-1: Three-phase LC low-pass filter

One thing to notice was that the inductors and capacitors in figure 4.6.1-1 were ideal components. In the simulation for the low pass filter to have a good damping response, a small resistor was connected in series with the inductor to reflect the practical inductor.

Moreover, the actual inductor value used in simulation was not the same one calculated in previous section but instead the designed in practice, which had the average value of 440 $\mu$ H.

It was discussed in reference [34], that in the RLC low pass filter circuit, the output voltage, lags the input voltage. This was because of the voltage drop across the resistor. Thus, it is important that the resistor be smaller enough just to introduce the necessary damping, Figure 4.6.1-2 illustrates the discussion.

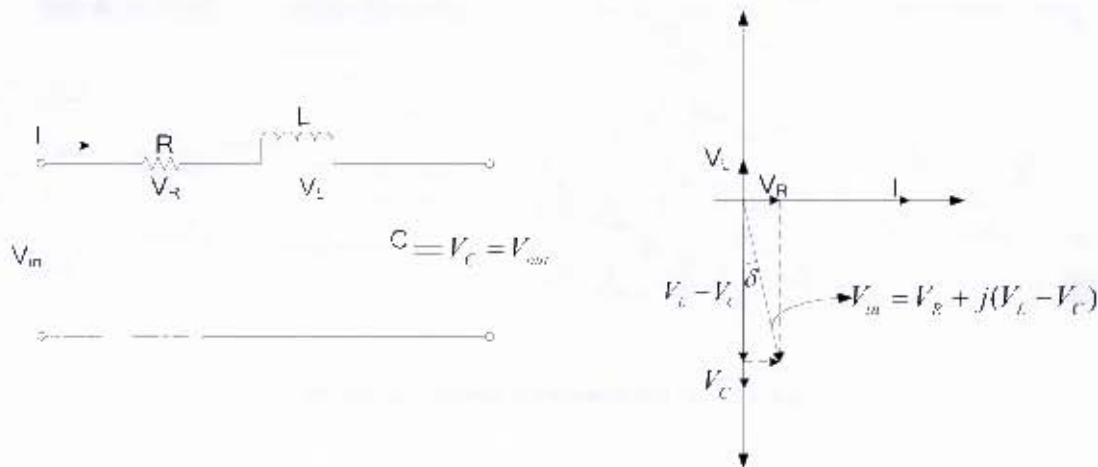


Figure 4.6.1-2: Three-phase LC low-pass filter

In the next section, the entire models will be connected together, to form the complete topology.

## 4.7 Full simulation Models connected

All the models were successfully implemented as discussed in previous section. In this section, the entire models were assembled together. They are presented in figure 4.7-1 in conjunction with all control model and equation blocks, which will be discussed in later sections.

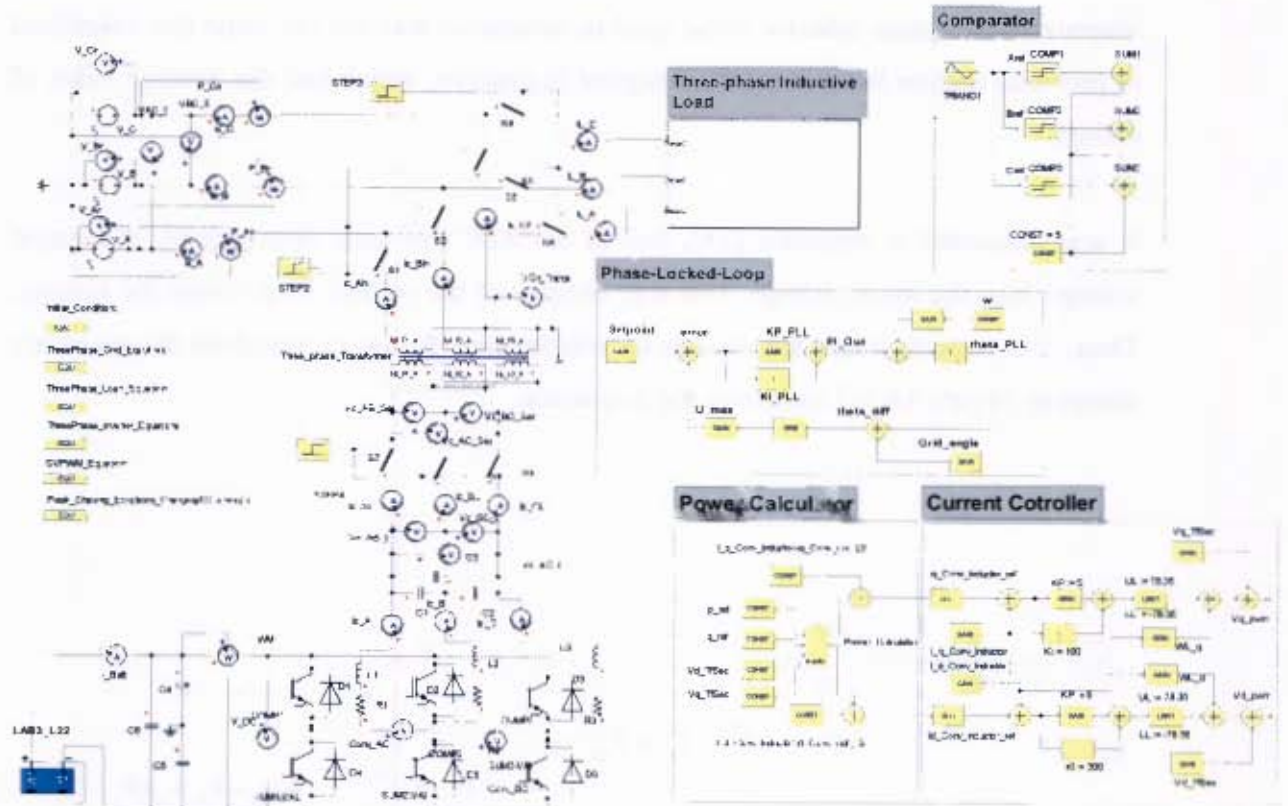
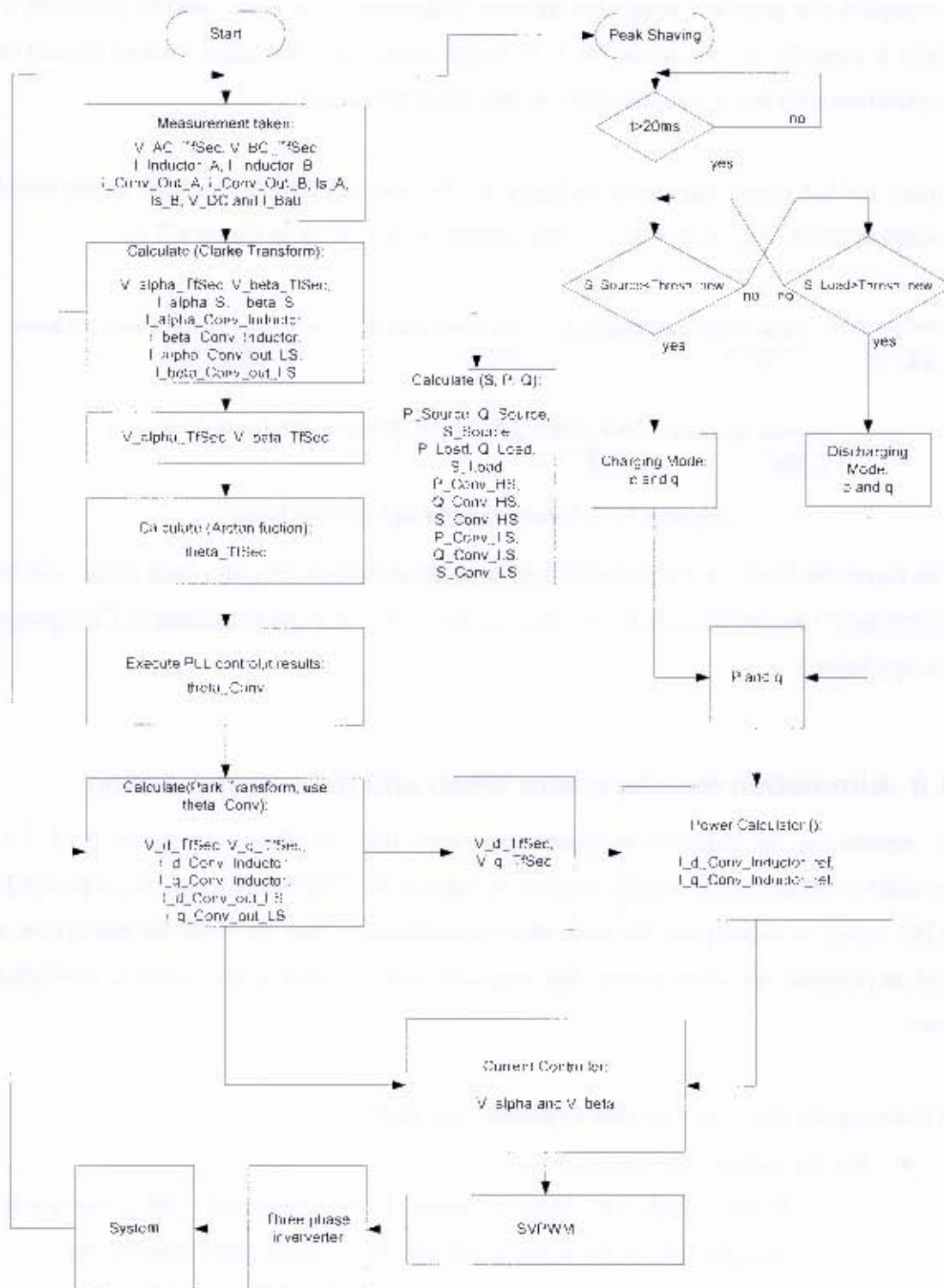


Figure 4.7-1: full simulation models connected

The three-phase load of figure 4.2.2-6 was assembled inside block as shown in figure 4.7-1. The next section will discuss the simulation sequence flow to accomplish the purposed PLS.

## 4.7.1 Simulation sequence flow



4.7.1-1: Simulation flow chart

- $I_{Batt}$ , the battery current,  $I_{inductor\_A}$  and  $I_{inductor\_B}$  are the inductor filter currents measured at “phase a” and “phase b” respectively.  $I_{Conv\_Out\_A\_LS}$  and  $I_{Conv\_Out\_B\_LS}$  are the currents measured on the output of the LC filter, at “phase a” and “phase b” respectively also. Finally  $I_{Source\_A}$  and  $I_{Source\_B}$ , which are the source current measured at “phase a” and “phase b”.

Following the sequence of figure 4.7.1-1, the next step was to transform all the three-phase measured signals to the stationary reference plane by using the positive sequence forward Clarke transformation. One thing to notice was that, the Clarke transformation as was discussed in appendix C, takes three input signals, however only two signals were measured for the voltages and two for the currents.

Furthermore, real and reactive power control was what was supposed to be accomplished, therefore as was discussed in section 3.4.3, the positive forward Clarke transformer instead of using  $\frac{2}{3}$  as coefficient; it used  $\sqrt{\frac{2}{3}}$ .

The coefficient  $\sqrt{\frac{2}{3}}$  aim as discussed before was to scale the stationary reference obtained signal, the current and the voltage, to a magnitude that would enable the exact calculation of the magnitude of the instantaneous three-phase power.

Therefore, the positive forward Clarke transform used to calculate  $V_\alpha$  and  $V_\beta$  is shown in equation (4.8-1).

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} V_{AC} \\ V_{BC} \end{pmatrix} \quad (4.8-1)$$

For the current, it is shown in equation (4.8-2)

$$\begin{pmatrix} I_\alpha \\ I_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{3}{2} & 0 \\ \frac{\sqrt{3}}{2} & \sqrt{3} \end{pmatrix} \begin{pmatrix} I_a \\ I_b \end{pmatrix} \quad (4.8-2)$$

Equation (4.8-2) was only valid for balanced system whereby  $(I_a+I_b+I_c=0)$  [35].

Now using Park transform expression C2.20 section C.2, the stationary reference frame was changed to rotating reference frame, appendix G.2 to G.4 illustrate the application of Parke Transformation in simplorer.

## 4.9 Simulation of Control Design

Two controls loop were implemented in the simulation to accomplish the PLS as discussed in chapter 3. The first one was a PLL PI-based -controller as discussed in section 3.4.1, with aim to synchronize the three-phase inverter with the three-phase grid.

The second one was an inner current loop control using a PI controller also; the aim was to control the low-pass filter inductor current so that the real and reactive power control could be achieved. They are both implemented in the rotating reference frame or dq-plane.

### 4.9.1 Phase Locked Loop PI-based Control Simulation

In previous section 3.4.1, the control design of PLL control was discussed for the continuous and discrete modeling, however the PLL PI-based controller used in simulation was the continuous controller because of its easy implementation as well as the easy tuning of the PI controller gains. Figure 4.9.1-1 illustrates its implementation in simplorer.

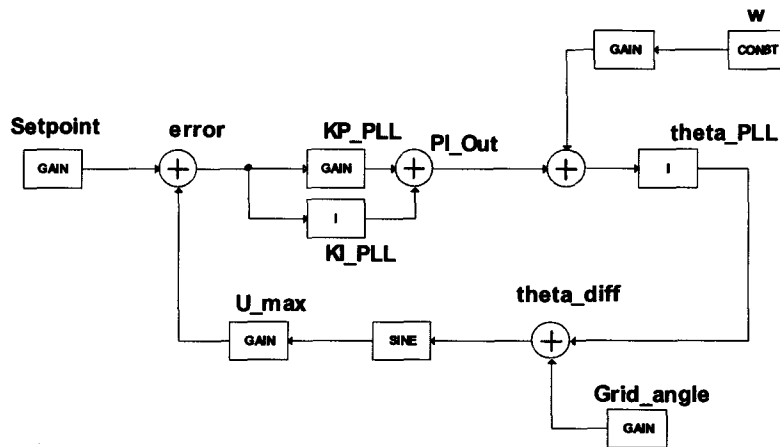
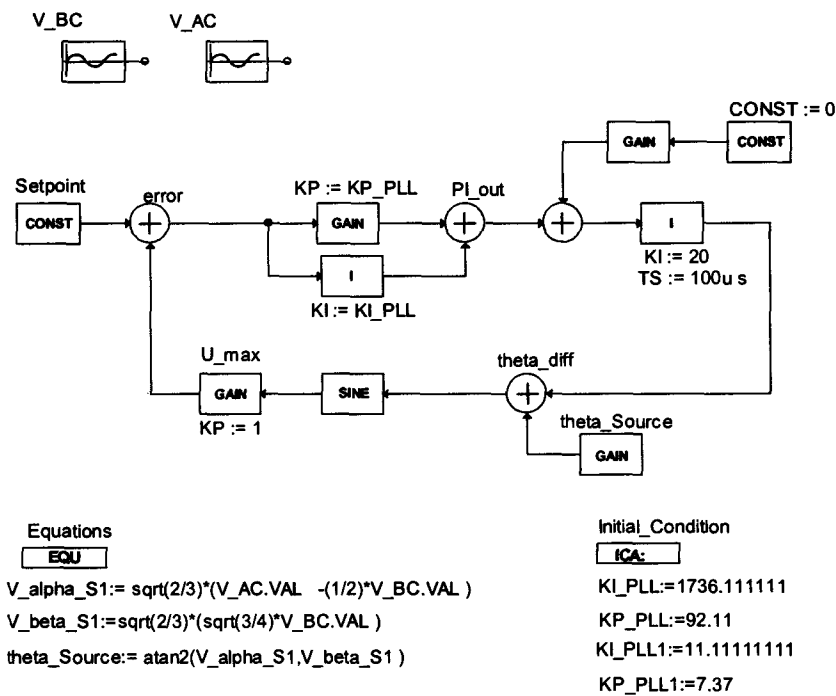


Figure 4.9.1-1: Block diagram of PLL PI-based controller in Simplerer

Due to the limitation of simplorer license, the full simulation model, figure 4.7-1 stopped working in simulation by the time the discrete PLL PI-based control algorithm as discussed in section 3.4.1.3 and 3.4.1.4 was ready to be implemented in the DSP chip in the lab.

However, to improve the practical result of the PLL PI-based controller, a portion of the simulated model, the PLL PI-based controller model, see figure 4.9.1-1, was simulated in simplorer student version on its own.

The simplorer student version packaged as mentioned in beginning has a limited numbers of elements to be used. Thus, few elements were used to simulate the PLL PI-based controller such as two sinusoidal function blocks, which was set to produce voltage line-to-line  $V_{ac}$  and  $V_{bc}$ . An equation block to calculate the voltage  $V_{\alpha}$  and  $V_{\beta}$  as well as the phase angle, theta. Moreover, an initial condition block, where the PLL PI gains, for  $\alpha=2.4$  and  $\alpha=30$  were set. Figure 4.9.1-2 shows this.



**Figure 4.9.1-2: PLL PI-based controller simulated in simplorer student version**

Some change was made in the PLL PI-based controller in practice, those change were simulated in the model of figure 4.9.1-2 above. The changes were the following: the gain KI was set to 20 for the integral plant in practice, thus same was done for the simulated model. The feedforward,  $w$ , was not used in practice, thus it was set to zero in the simulated model. The feedback voltage gain,  $U\_max$ , was set to unity in practice, so the same was done in the simulation too.

Moreover, because this new model was not being simulated in conjunction with the full model as it was before the license expired, see figure 4.7-1, then the simulated dynamic response of the new model of the PLL PI-based controller, figure 4.9.2-2 was different from the practical dynamic response. Noting that figure 4.7-1 was similar to the practical model in the lab; see figure 5-1.

Therefore the focus of the new simulated model of the PLL PI-based control was to improve the practical design of the PLL PI-based controller in term of the choice of the gains as discussed previously.

The integral block is defined in simplorer as shown in figure 4.9.1-3, [30].

$$y(k) = y(k-1) + KI \cdot TS \cdot x(k) \quad \text{or} \quad G(s) = \frac{KI}{s}$$

$$KI = \frac{1}{T_R} \quad T_R = \text{Integral-Action Time} \quad TS = \text{Sample Time}$$

Figure 4.9.1-3: simplorer integral block definition [30]

From table 3.4.1.2-1,  $\alpha=2.4$  the PLL PI-based controller proportional gain,  $KP\_PLL$  was 92.11 and the integral-action time was 0.576m sec. Using figure 4.9.1-3 the PLL integral gain,  $KI\_PLL$  was 1736.11. The second integral gain in figure 4.9.1-2 was set to 20, which meant that the integral time constant was 50ms. Figure 4.9.1-4 illustrates the response of the PLL with  $\alpha=2.4$ . It can be seen that the PLL response, quickly tracks the three-phase source phase as was discussed in section 3.4.1.

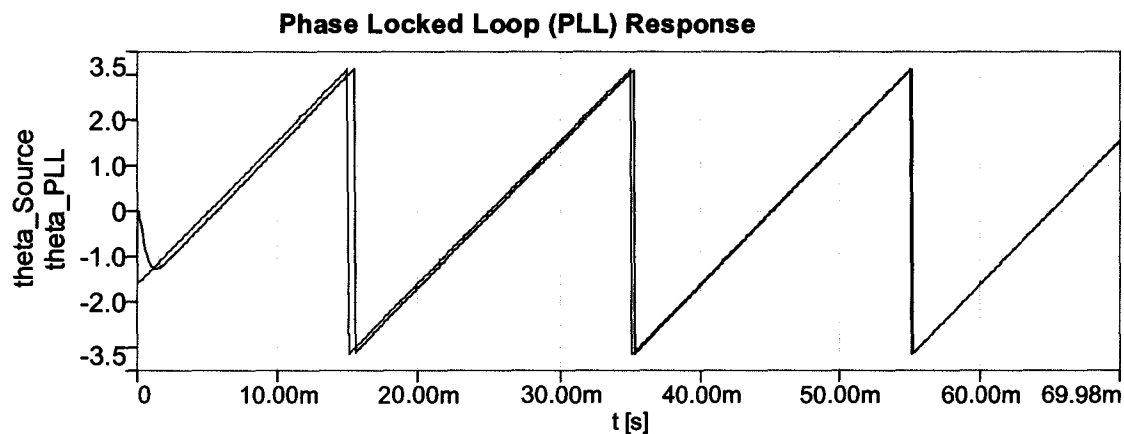


Figure 4.9.1-4: Phase locked loop response with alpha equals to 2.4

In addition, applying  $\alpha=30$ ,  $KP\_PLL$  was 7.37 and the integral time constant was 90m sec as discussed in section 3.4.1. Using figure 4.9.1-3 the integral gain,  $KI\_PLL$  was 11.11. Maintaining the same integral gain for the second integral, the PLL response for  $\alpha=30$  was presented in figure 4.9.1-5.

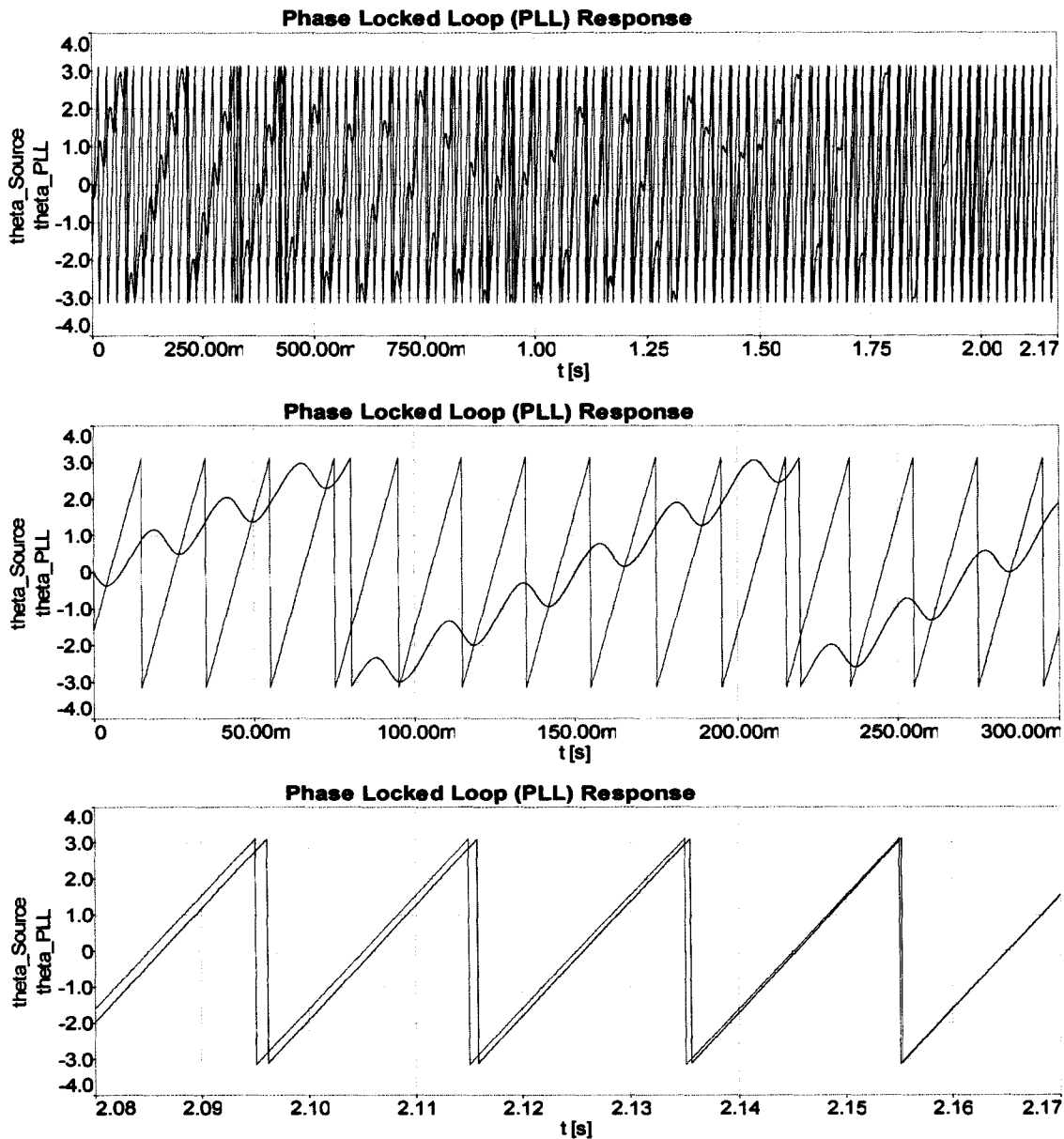


Figure 4.9.1-5: Phase locked loop response with alpha equals to 30

### 4.9.2 Simulation of Space Vector Pulse Width Modulation

The Space Vector Pulse Width Modulation algorithm was written in an equation block in simplorer, see appendix G.5. The SVPWM algorithm had as inputs the voltage signals alpha and beta and as output three voltage reference at 50Hz and  $120^\circ$  out phase. These three voltages reference were compared with a triangle waveform signal with a frequency

value of 10kHz. Consequently, this comparison resulted in pulse signals known as SVPWM, which control the three-phase inverter IGBT's gates switching.

The SVPWM algorithm in appendix G was subdivided in two parts. The first part was the calculation of the sectors, where the Space Vector voltage reference rotates to change the states of the three-phase inverter switches [17]. The second part was the calculation of the switching times for each state, whereas these switching times were combined in such way to form the three-phase voltage reference,  $A_{ref}$ ,  $B_{ref}$  and  $C_{ref}$  of the SVPWM, see appendix G.5. Those voltages are phase shifted by  $120^\circ$  from each other.

The three-phase VSI switches have eight operating states; this can be better understood by analyzing the three top switches. The bottom switches were neglected in the analysis, because by changing the top switches, the bottom switches automatically were affected [17]. Table 4.9.2-1 illustrates the eight possible states as describe in reference [17].

**Table 4.9.2-1: three-phase VSI switches states**

States	Sw1 Top	Sw2 Top	Sw3 Top
$V_0$	0	0	0
$V_5$	0	0	1
$V_3$	0	1	0
$V_4$	0	1	1
$V_1$	1	0	0
$V_6$	1	0	1
$V_2$	1	1	0
$V_7$	1	1	1

Where, 0 represent "off" and 1 "on". There were two zero vectors, which are  $V_0$  and  $V_7$  and six non-zero vectors, which are  $V_1$  to  $V_6$ . When the Space Vector voltage reference travels through each state, it forms a hexagonal shape with six sectors; figure 4.9.2-1 shows this.

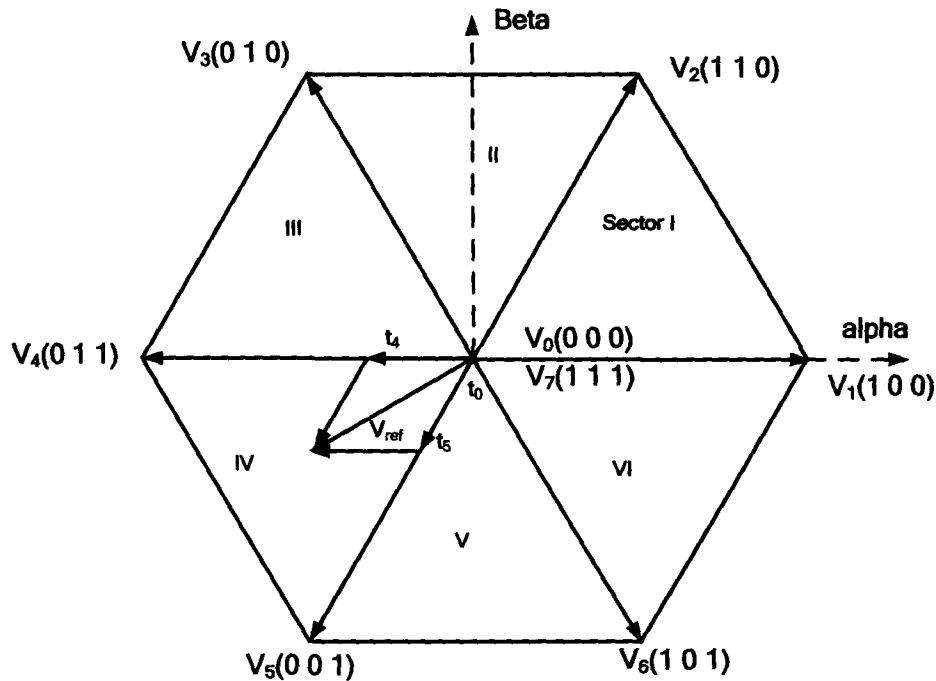


Figure 4.9.2-1: Representation of the three-phase inverter switching states in the stationary reference plane [17].

“In order to maintain the effective switching frequency of the power devices at minimum, the sequence of toggling between these vectors is organized such that only one leg is affected in every step” [17]. Thus, this procedure helped to form the six sectors illustrated in figure 4.9.2-1.

In Analog devices [17], it was discussed that the calculation of the time that the non-zero and zero states takes, was “the central part of space vector modulation strategy”. Equations 4.9.2-1 and 4.9.2-2 shows the equations used to calculate the times that each non-zero and zero states would take respectively.

$$\begin{pmatrix} T_k \\ T_{k+1} \end{pmatrix} = \frac{\sqrt{3}}{2} \frac{T_s}{V_{DC}} \cdot \begin{bmatrix} \sin \frac{k\pi}{3} & -\cos \frac{k\pi}{3} \\ -\sin \frac{(k-1)\pi}{3} & \cos \frac{(k-1)\pi}{3} \end{bmatrix} \cdot \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \quad (4.9.2-1)$$

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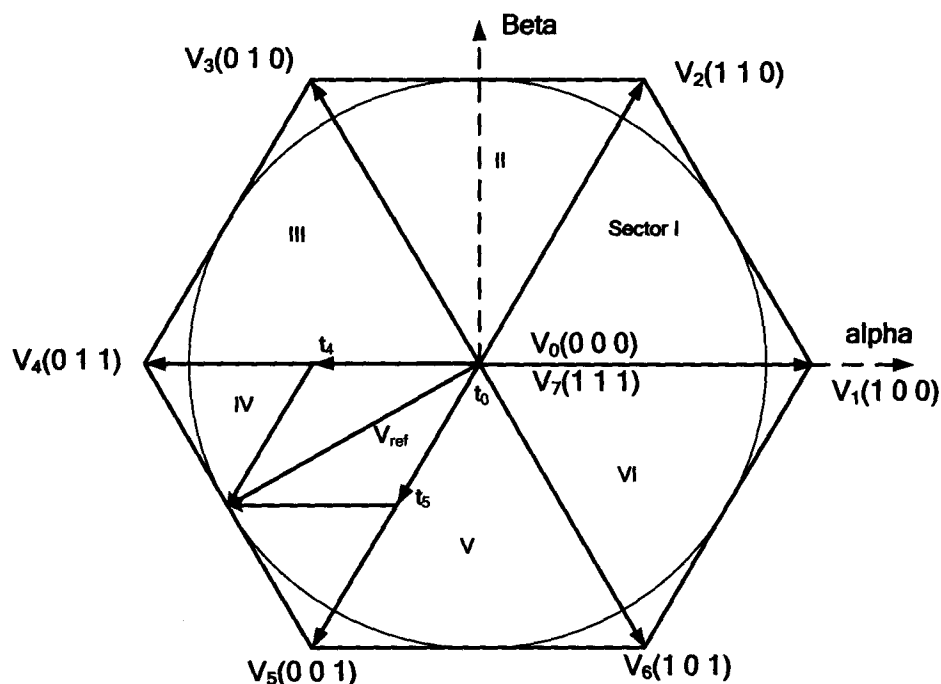
$$T_0 = \frac{T_s}{2} - (T_k + T_{k+1}) \quad (4.9.2-2)$$

Where  $T_k$  and  $T_{k+1}$  represent the time of the non-zero states in each sector, the sector selection is governed by the variable  $k$ , which goes from 1 to 6. When  $k=6$ ,  $k+1$  is set to 1 [17].  $T_0$  is the time that the non-zero states takes,  $T_s$  is the period and  $V_{DC}$  is the battery voltage. Table 4.9.2-2 illustrates the relation between the times of each top switches states of the three-phase inverter in each sector.

Table 4.9.2-2: states time relation in each sector

Sector	Time	States	Sw1 Top	Sw2 Top	Sw3 Top
1	$T_0/2$	$V_0$	0	0	0
	$T_1$	$V_1$	1	0	0
	$T_2$	$V_2$	1	1	0
	$T_0$	$V_7$	1	1	1
	$T_2$	$V_2$	1	1	0
	$T_1$	$V_1$	1	0	0
	$T_0/2$	$V_0$	0	0	0
2	$T_0/2$	$V_0$	0	0	0
	$T_3$	$V_3$	0	1	0
	$T_2$	$V_2$	1	1	0
	$T_0$	$V_7$	1	1	1
	$T_2$	$V_2$	1	1	0
	$T_3$	$V_3$	0	1	0
	$T_0/2$	$V_0$	0	0	0
3	$T_0/2$	$V_0$	0	0	0
	$T_3$	$V_3$	0	1	0
	$T_4$	$V_4$	0	1	1
	$T_0$	$V_7$	1	1	1
	$T_4$	$V_4$	0	1	1
	$T_3$	$V_3$	0	1	0
	$T_0/2$	$V_0$	0	0	0
4	$T_0/2$	$V_0$	0	0	0
	$T_5$	$V_5$	0	0	1
	$T_4$	$V_4$	0	1	1
	$T_0$	$V_7$	1	1	1
	$T_4$	$V_4$	0	1	1
	$T_5$	$V_5$	0	0	1
	$T_0/2$	$V_0$	0	0	0
5	$T_0/2$	$V_0$	0	0	0
	$T_5$	$V_5$	0	0	1
	$T_6$	$V_6$	1	0	1
	$T_0$	$V_7$	1	1	1
	$T_6$	$V_6$	1	0	1
	$T_5$	$V_5$	0	0	1
	$T_0/2$	$V_0$	0	0	0
6	$T_0/2$	$V_0$	0	0	0
	$T_1$	$V_1$	1	0	0
	$T_6$	$V_6$	1	0	1
	$T_0$	$V_7$	1	1	1
	$T_6$	$V_6$	1	0	1
	$T_1$	$V_1$	1	0	0
	$T_0/2$	$V_0$	0	0	0

The maximum modulation index with a continuous SVPWM as mentioned in section 3.4 was 90.6% [17]. Furthermore, at this modulation index, the reference vector,  $V_{ref}$ , has locus that would follow a circle inscribed within the hexagon [17]. Figure 4.9.2-2 shows this.



**Figure 4.9.2-2: Representation of the three-phase inverter switching states in the stationary reference plane for the maximum modulation index [17]**

If the reference vector happens to be outside the hexagon, it was discussed from reference [17] that the summation of  $T_k$  and  $T_{k+1}$  in equation (4.9.2-2), would result in a value bigger than  $\frac{T_s}{2}$ , which would result  $T_0$  to be negative. This negative result would be meaningless for the time duration of the zero-state vectors [17].

To overcome this predicament, the active time  $T_k$  and  $T_{k+1}$  were rescaled to new values,  $T_{k\_new}$  and  $T_{k+1\_new}$ , such that their summation is always equal to  $\frac{T_s}{2}$  whenever the active times happens to be greater than  $\frac{T_s}{2}$ . Equations (4.9.2-3) to (4.9.2-5) show this [17].

$$T_{k\_new} := \frac{T_s}{2} \cdot \frac{T_k}{(T_k + T_{k+1})}; \quad (4.9.2-3)$$

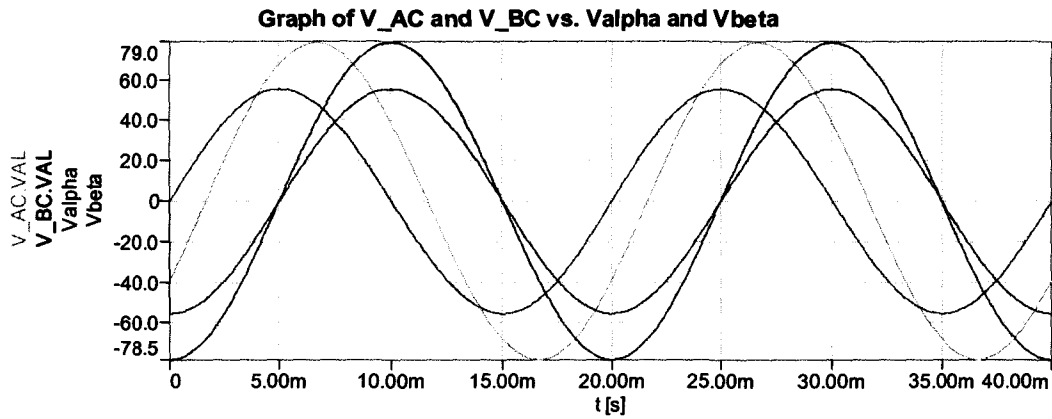
$$T_{k+1\_new} := \frac{T_s}{2} \cdot \frac{T_{k+1}}{(T_k + T_{k+1})}; \quad (4.9.2-4)$$

$$T_{k\_new} + T_{k+1\_new} := \frac{T_s}{2}; \quad (4.9.2-5)$$

With this rescaling method,  $T_0$  would always be zero whenever the SVPWM would be over modulating, and so,  $V_{ref}$  locus would follow the hexagon peripheral. However, this action would reduce the output fundamental voltage [17].

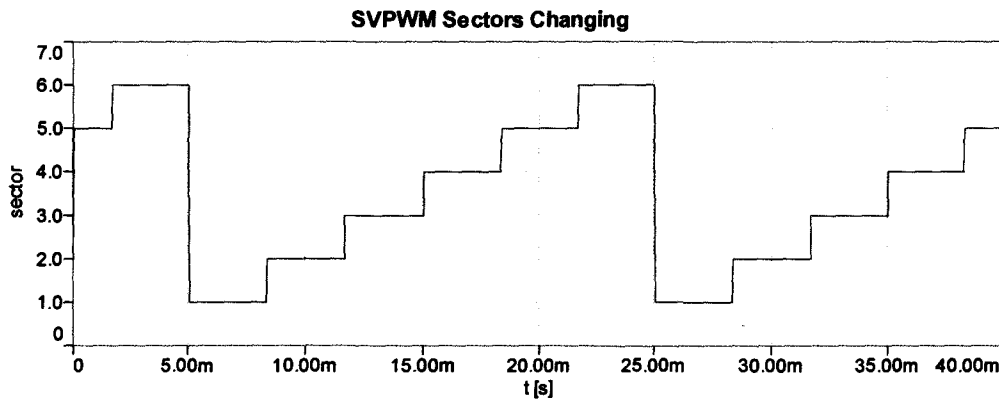
Nevertheless, as discussed previously in section 3.4.2 the minor loop current controller has as output a voltage signals in rotating reference plane, dq-plane. Moreover, after inverted to the stationary reference plane,  $\alpha\beta$ -plane by using the inverse Parke transformation, it was discussed in same section, that these signals could be used as input to the SVPWM algorithm.

However, before implemented as discussed above, the SVPWM algorithm was tested by using  $V_\alpha$  and  $V_\beta$  as input, which were calculated from Clark transformation, and which had as input the three-phase source line to line voltage signals  $V_{AC}$  and  $V_{BC}$ . Figure 4.9.2-3 illustrates the voltages signals.



**Figure 4.9.2-3: line-to-line voltage signals and voltage signals in the stationary reference**

Figure 4.9.2-4 illustrates the results of SVPWM sector selection.



**Figure 4.9.2-4: SVPWM sector selection**

When a sector is selected, the switching times are calculated for the specific state in that sector as discussed above. Table 4.9.2-3 illustrates this.

Table 4.9.2-3: Space Vector reference voltages for each phase.

Sector	Reference Signal	Time
1	$A_{ref}$	$T_0/2 + T_2 + T_1$
	$B_{ref}$	$T_0/2 + T_2$
	$C_{ref}$	$T_0/2$
2	$A_{ref}$	$T_0/2 + T_2$
	$B_{ref}$	$T_0/2 + T_2 + T_3$
	$C_{ref}$	$T_0/2$
3	$A_{ref}$	$T_0/2$
	$B_{ref}$	$T_0/2 + T_4 + T_3$
	$C_{ref}$	$T_0/2 + T_4$
4	$A_{ref}$	$T_0/2$
	$B_{ref}$	$T_0/2 + T_4$
	$C_{ref}$	$T_0/2 + T_4 + T_5$
5	$A_{ref}$	$T_0/2 + T_6$
	$B_{ref}$	$T_0/2$
	$C_{ref}$	$T_0/2 + T_6 + T_5$
6	$A_{ref}$	$T_0/2 + T_6 + T_1$
	$B_{ref}$	$T_0/2$
	$C_{ref}$	$T_0/2 + T_6$

Figure 4.9.2-5 presents the SVPWM reference signals of table 4.9.2-3 in simpler simulation.

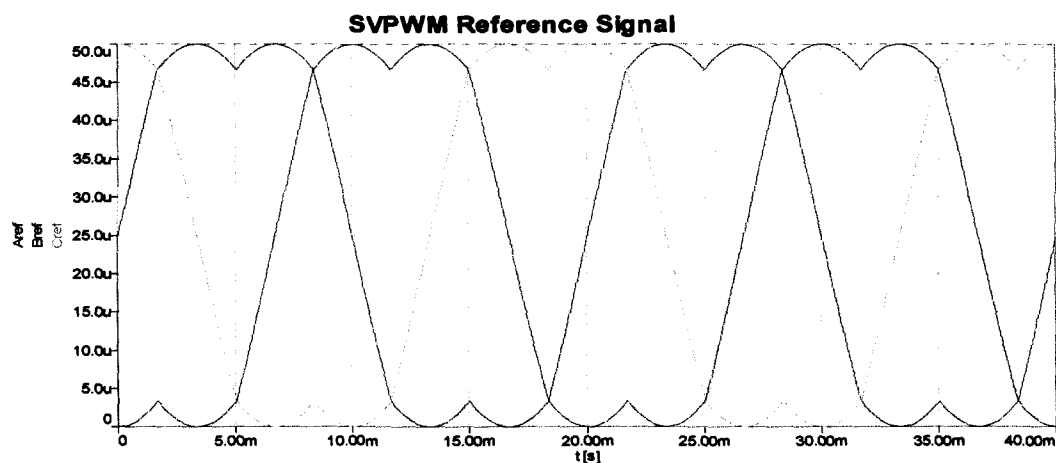


Figure 4.9.2-5: SVPWM reference signals

These reference signals were compared with a high frequency triangle wave to produce the PWM signal. Figure 4.9.2-6 presents the module used to compare the SVPWM reference signals with the triangle wave.

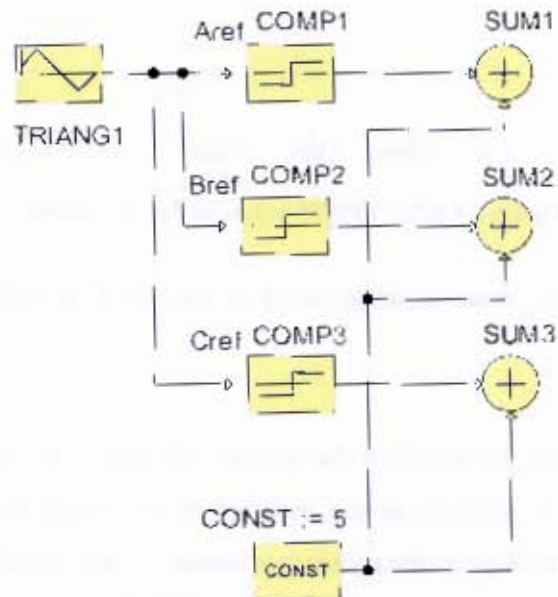


Figure 4.9.2-6: comparison of the reference signals with a high frequency triangle waveform

Figure 4.9.2-7 shows the result of the SVPWM pulse in the first sector:

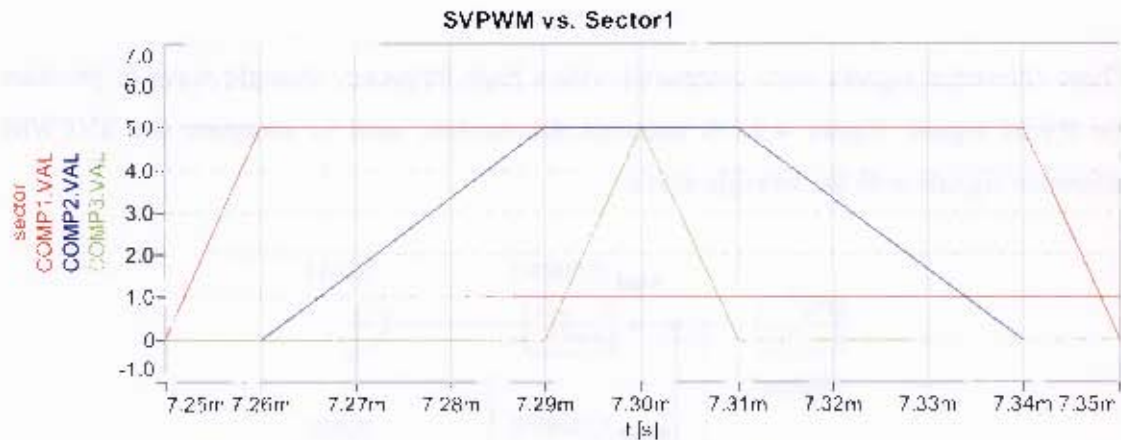


Figure 4.9.2-7: SVPWM pulses in the first sector

With this result the three-phase inverter could be switched on and off in very efficient way.

Next section will present the result of the power calculator in conjunction with minor loop current controller. In addition as was mentioned previously the results of the minor loop controller was the voltage in the rotating reference plane, which after inverted to the stationary reference plane, was sent as input to the SVPWM algorithm.

### 4.9.3 Current Loop Control and power calculator Simulation

Figure 4.9.3-1 shows the result of the three-phase inverter being synchronized with three-phase grid. This result was gathered from the simulation of the full model, figure 4.7-1, before the license was expired.

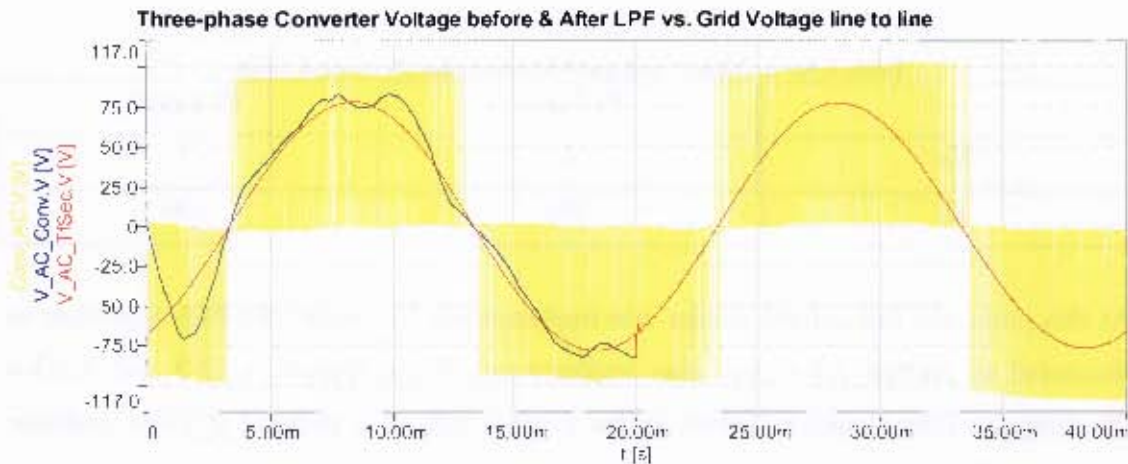


Figure 4.9.3-1: Three-phase inverter voltage phase locked with the three-phase grid

Simultaneously the power calculator in conjunction with the minor loop was implemented with  $p_{ref}$  and  $q_{ref}$  initially set to zero to force the filter inductor current to zero. Figure 4.9.3-2 illustrates the power calculator in conjunction with minor loop as discussed in section 3.4.3. The PI control gains were set by trial and error method, table 4.9.3-1 shows the minor loop current PI gains.

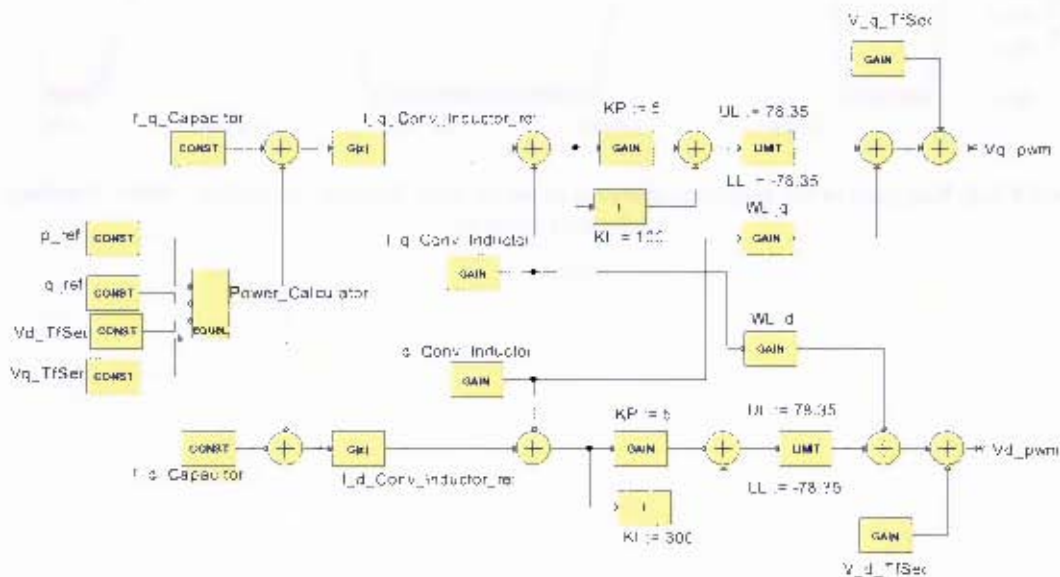


Figure 4.9.3-2: Power calculator in conjunction with minor loop current controller implemented in simplorer.

Table 4.9.3-1: Minor loop current controller PI control gains

	PI d-part	PI q-part
$K_p$	5	5
$K_i$	300	100

At this point, the full control design was implemented. Moreover, the PLS algorithm as discussed in section 3.4.4 was also implemented. Thus, figures 4.9.3-3 and 4.9.3-4 illustrate the filter inductor current in the rotating reference plane,  $I_d$  Conv Inductor and  $I_q$  Conv Inductor, tracking the changing setpoint or reference current,  $I_d$  Conv Inductor\_ref.VAL and  $I_q$  Conv Inductor\_ref.VAL, respectively.

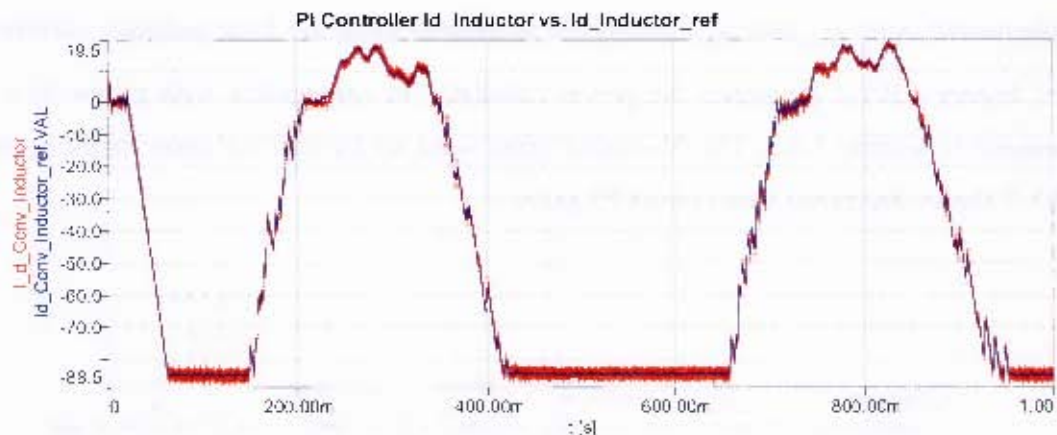


Figure 4.9.3-3: Real part of the rotating reference plane current through the inductor filter tracking a reference current

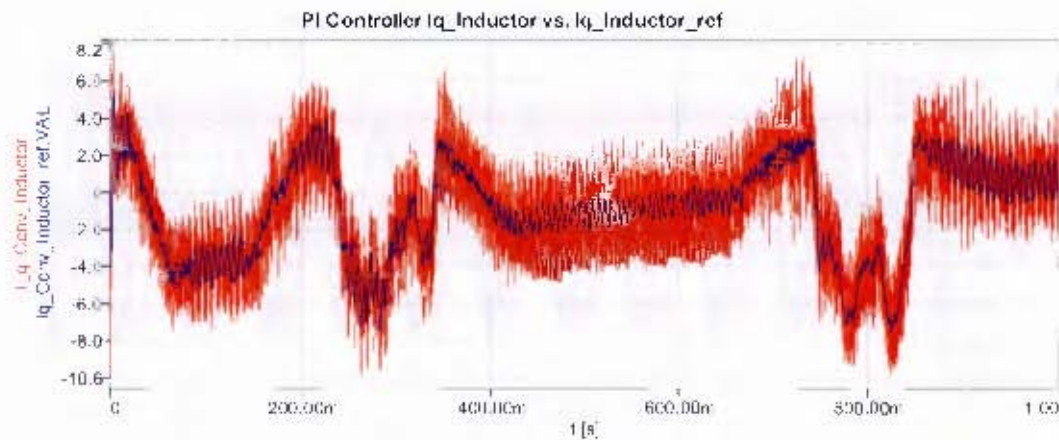
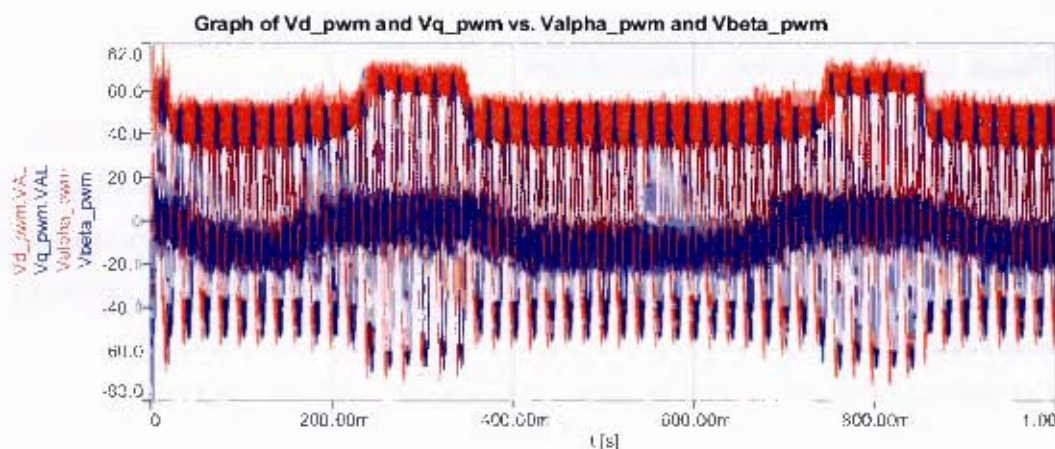


Figure 4.9.3-4: Imaginary part of the rotating reference plane current through the inductor filter tracking a reference current

These reference currents changed as illustrated above because of the peak load shaving algorithm, so that the charging and discharging of the battery could be accomplished.

Figure 4.9.3-5 shows the minor loop signals results, which were the following: the voltage signals in the rotating reference plane,  $Vd\_pwm.VAL$  and  $Vq\_pwm.VAL$ , and the voltage signals in the stationary reference plane after inverted,  $Valpha\_pwm$  and  $Vbeta\_pwm$ .



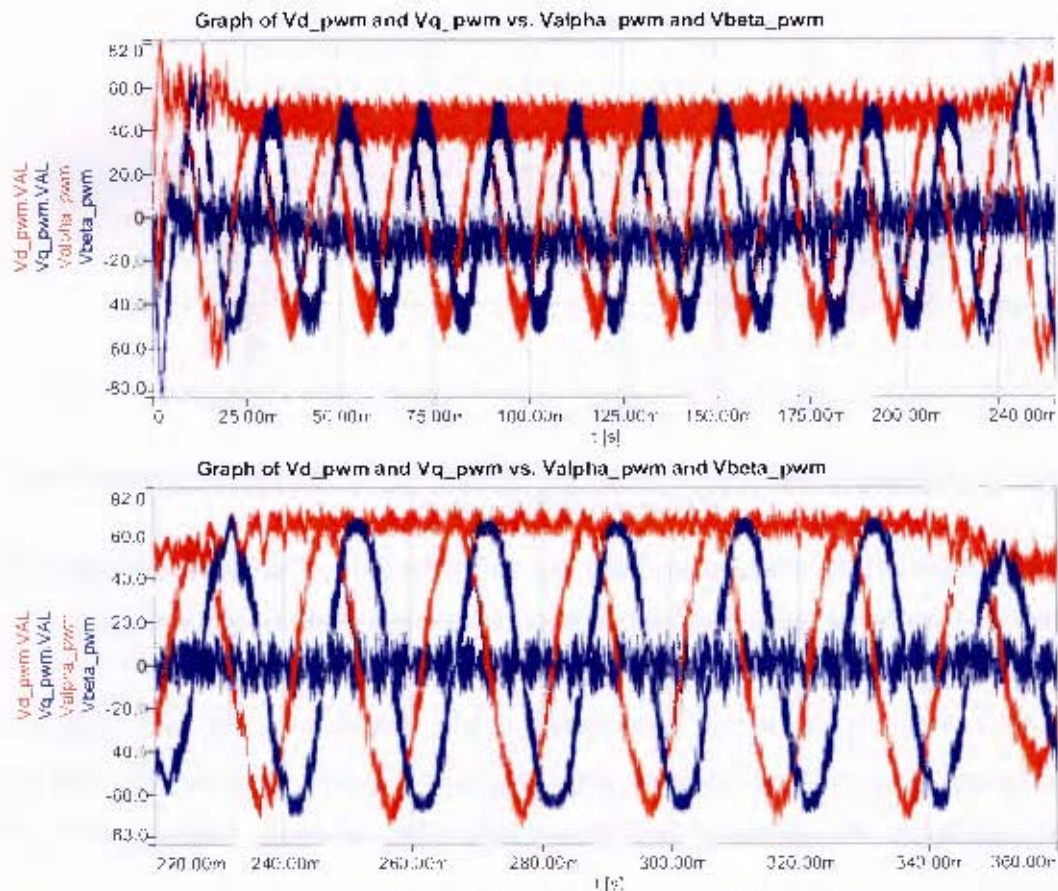


Figure 4.9.3-5: Minor loop current controller results

#### 4.10 Peak Load Shaving Simulation

This section will present the PLS simulation of UCTMS load profile. Figure 4.10-1 shows two daily peaks of UCTMS load profile and the set threshold, which as discussed in section 3.4.4.1 had the aim to decrease the peak power by 5%. The power values were scaled from mega watts to kilowatts, because the three-phase source was set to 400V LL instead of 11kV LL.

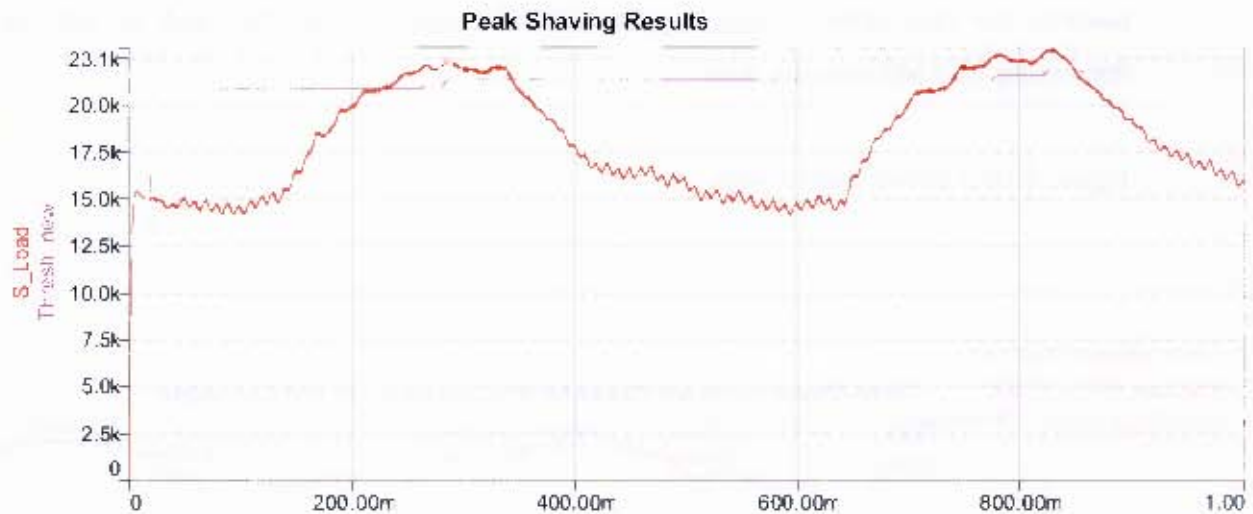


Figure 4.10-1: Two days load profile for UCTMS and the set threshold

Recalling from the previous discussion, that whenever UCTMS load is below the threshold point, the PI.S algorithm was set up in such way that it would enable the three-phase inverter to charge the battery. This would mean that the three-phase grid or source apparent power would be higher than the UCTMS load, so that it could be able to supply both UCTMS load and the battery storage system.

At this point, the three-phase inverter system behaves as load, buying electricity from the grid and contributing on the MD peak power. However the three-phase source apparent power is monitored in the peak load shaving algorithm, as describe in section 3.4.4.2 in such way that whenever it would reach 98% of the threshold point, the three-phase inverter would decrease the flow of power toward the battery storage to zero.

However, as soon as UCTMS load profile would be above the threshold point, the peak load shaving algorithm as discussed previously, was written in such way to enable the three-phase inverter to supply the apparent power at the same PF as the three-phase grid.

Consequently decreasing the three-phase source apparent power optimally and holding it at the threshold point. The three-phase inverter at this point was behaving as distributed generation (DG) system, which would mean that it would be positively contributing

towards the three-phase source supply reliability and sustainability and as well as decreasing UCTMS monthly bills.

Figure 4.10-2 shows these results

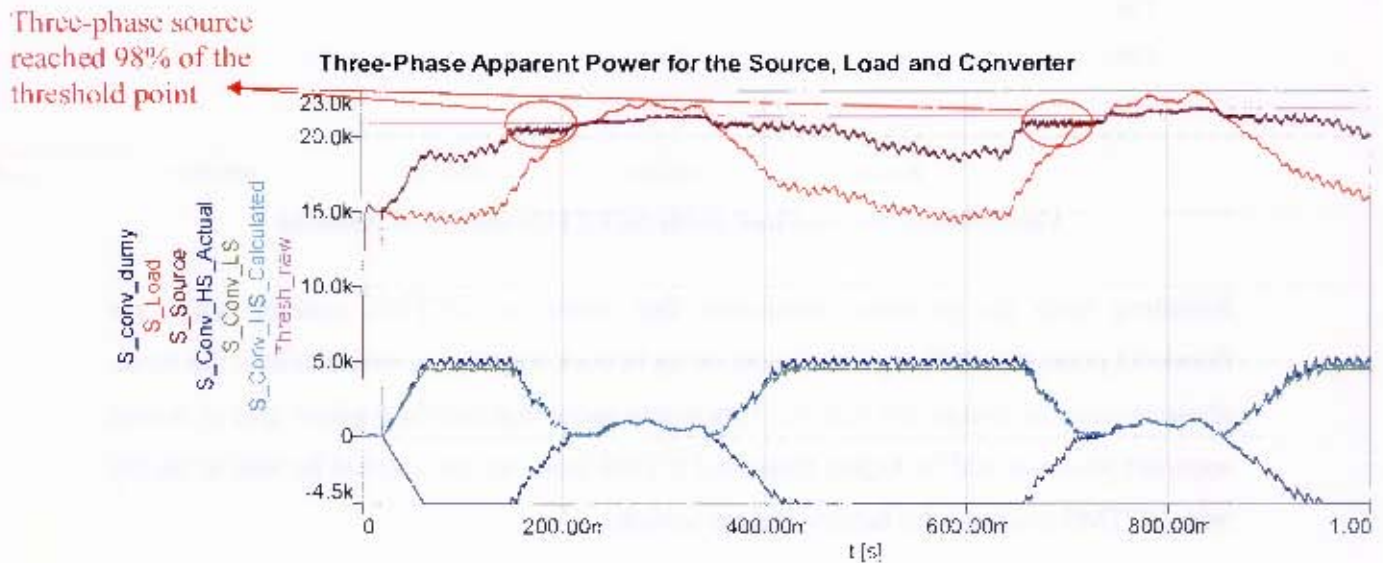


Figure 4.10-2: peak load shaved

As was mentioned previously in section 3.4.4.2 the battery charger algorithm was not implemented in this thesis, then the focus in this section, however was to show the three-phase source MD,  $S_{Source}$ , been shaved, which was accomplished successfully. From figure 4.10-2, it could be seen that the consumer load,  $S_{Load}$ , was being supplied by the battery storage.

In figure 4.10-2,  $S_{conv\_dummy}$  is the peak load shaving algorithm control apparent power variable. see appendix G.6. In addition, as was mentioned previously, positive flow of power was chosen from the three-phase inverter towards the three-phase grid.

Thus, the  $S_{conv\_dummy}$  was allowed to be positive or negative, see figure 4.10-2, in this way whenever  $S_{conv\_dummy}$  was negative the three-phase inverter would be charging the

battery. Conversely, it would be discharging the battery. While charging,  $S_{conv\_dummy}$  was not allowed to go more than the three-phase transformer maximum capacity, which was 4.5kVA. Figure 4.10-3 shows the result of the battery charge and discharging mode.

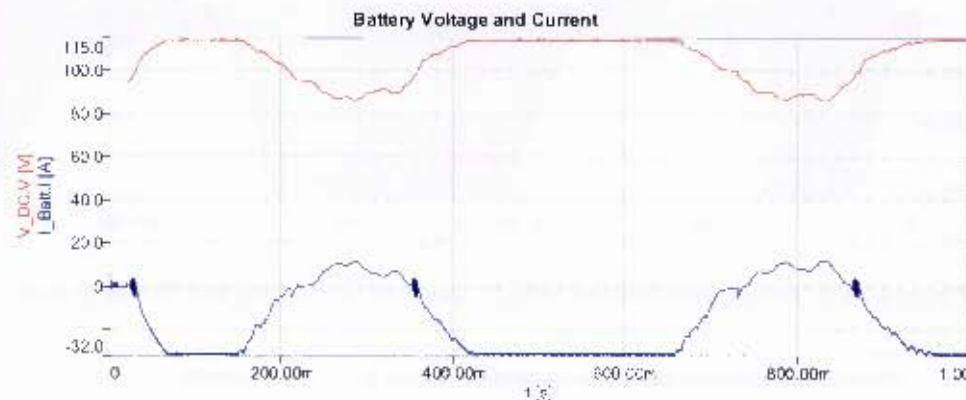


Figure 4.10-3: Battery voltage and current results

The variable  $S_{Conv\_HS\_Actual}$  in figure 4.10-2 is the three-phase inverter apparent power calculated from the measurement taken from the high side of the three-phase transformer.  $S_{Conv\_LS}$  in other hand is the three-phase inverter apparent power calculated from the measurement taken from the low side of the three-phase transformer. Finally  $S_{Conv\_HS\_Calculated}$  is the three-phase inverter apparent power calculated from the voltage and current signals that were not measured but instead calculated from the lower side signals of the three-phase transformer voltage and current signals, see appendix G.2 and G.3 for more detail.

From chapter 3, it was discussed that when the three-phase VSI is made to behave as CSI by using a minor current loop, it would produce good quality three-phase inverter currents. Figures 4.10-4, 4.10-5 and 4.10-6 confirm the discussion: it shows the three-phase inverter currents through an inductor filter. It can be seen that the current was well controlled and balanced.

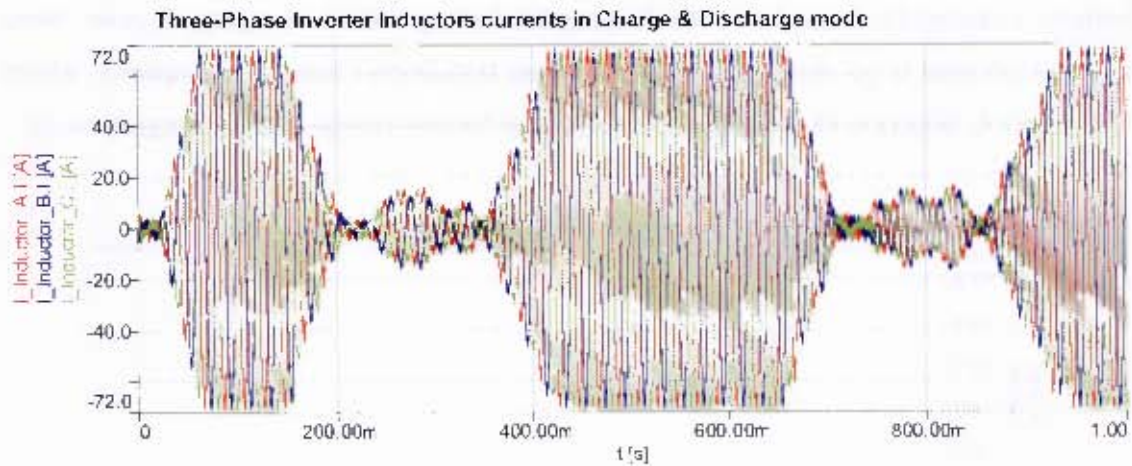


Figure 4.10-4: Three-phase inverter inductor currents at charging and discharge mode

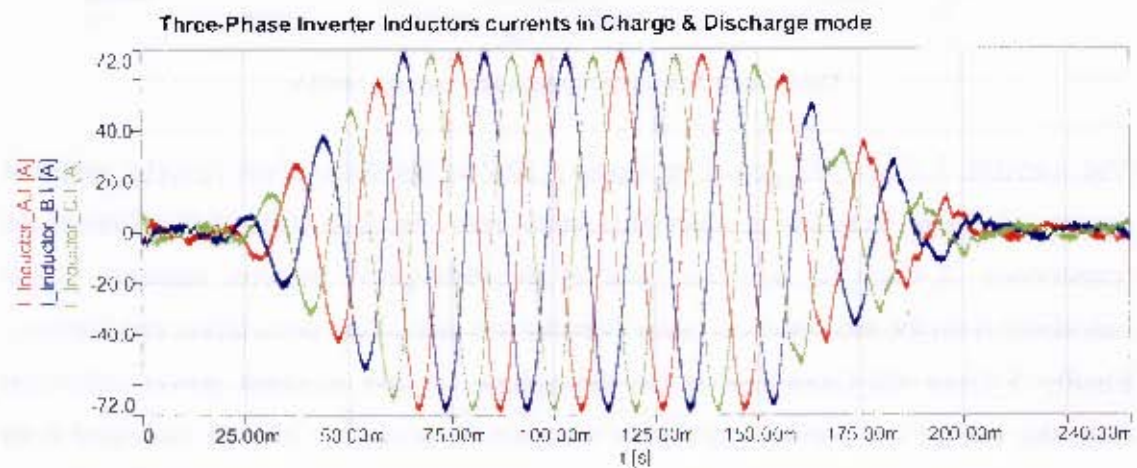


Figure 4.10-5: Three-phase inverter inductor currents at charging mode

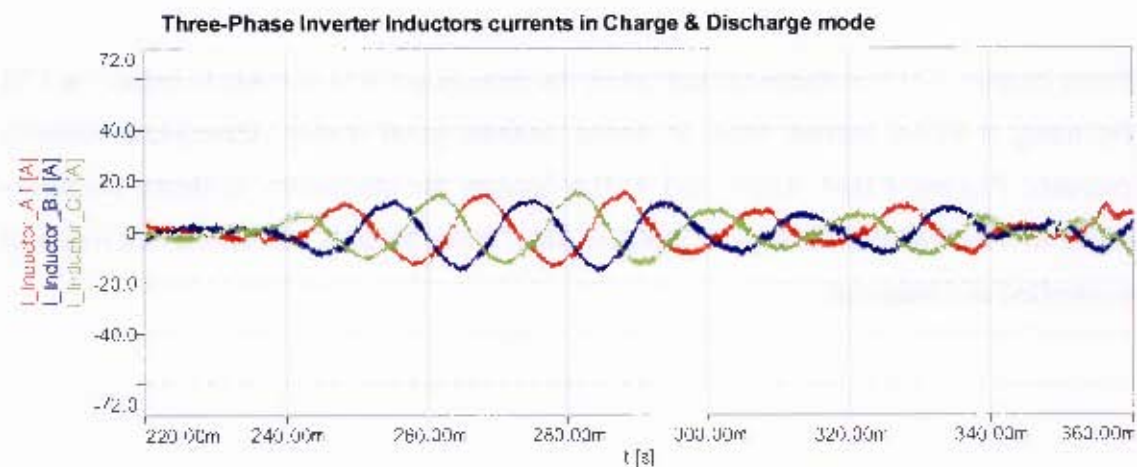
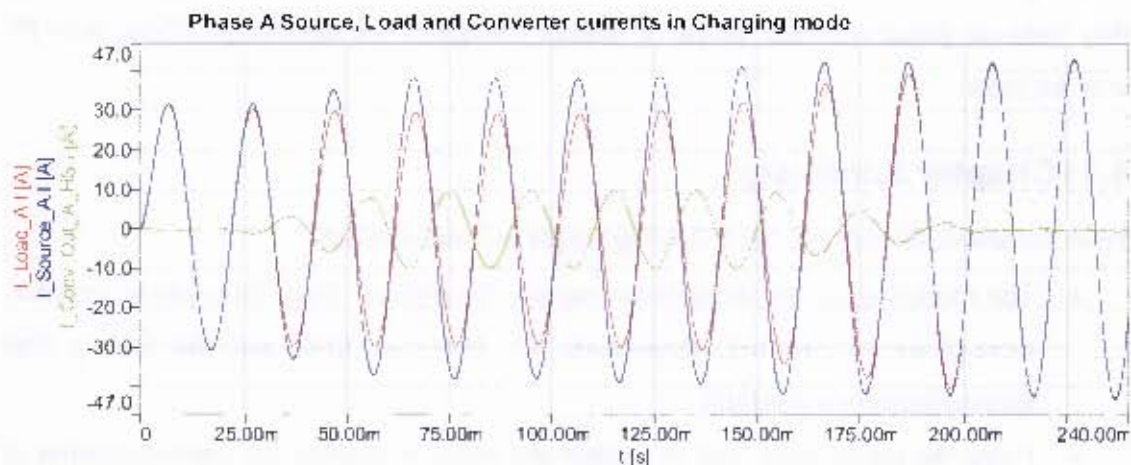


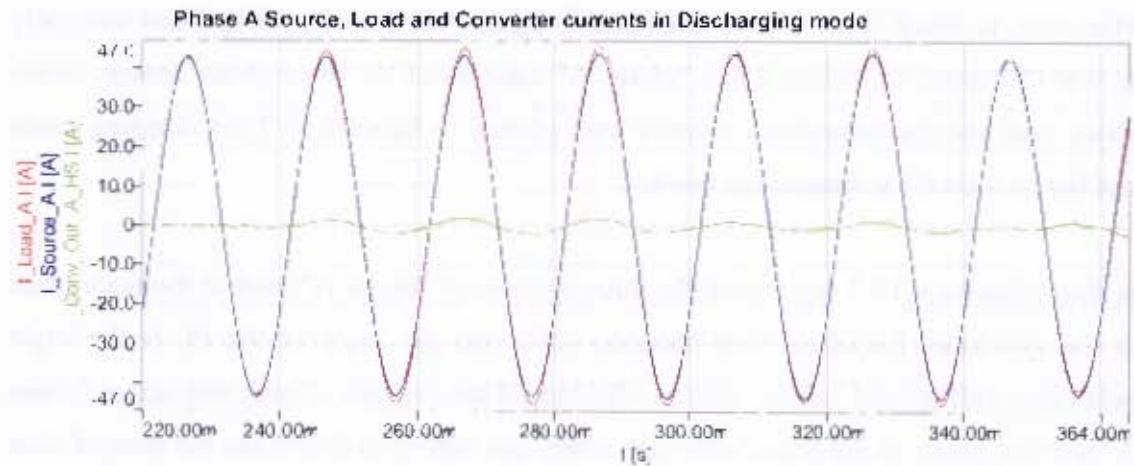
Figure 4.10-6: Three-phase inverter inductor currents at discharging mode

Moreover, to check if the PLS as illustrated in figure 4.10-2 was accomplished optimally as was discussed in section 2.3.1, “phase A” currents of the three-phase source, three-phase load and the three-phase inverter were plotted in figure 4.10-7 for charging mode and figure 4.10-8 for discharging mode.

In those figures 4.10-7 and 4.10-8 the three currents of “phase A”, met at the node point in the grid side. Recalling from literature [29], that the angle of the PF is the angle between a voltage and current, then by checking if the currents of each respective “phase A” were in phase or out phase with each other, that helped to determine the state of their PF in relation with source voltage.



**Figure 4.10-7: Three-phase source, three-phase inverter and three-phase load phase A currents at charging mode**



**Figure 4.10-8: Three-phase source, three-phase inverter and three-phase load phase A currents at discharging mode.**

From figure 4.10-8, it can be seen that the three currents were in phase, which meant that they were out phase with the “phase A” source voltage by the same angle. Thus, their PF was the same.

## 4.11 Chapter Summary

From the above discussion, the following points are summarized:

- The modeling of the three-phase supply, three-phase load, three-phase inverter, three-phase transformer, three-phase LC low-pass filter and the battery was accomplished successfully.
- Using the three-phase load as resistor and inductor enabled the implementation of the actual UCTMS load in simulation.
- The PLL PI-based controller was successfully implemented in simulation in the continuous mode. It was shown that by using the right gains of the PI controller the three-phase phase angle was track successfully and quickly.
- The calculation of the three-phase inverter phase angle,  $\gamma$ , by using the PLL PI-based controller was very crucial; it helped to calculate the three-phase inverter signals in the rotating reference plane.
- Consequently, the minor current loop controller was successfully implemented.

- Using the power calculator and PLS algorithm in conjunction with the minor loop current controller gave the possibility of implementing the purposed peak load shaving at UCTMS load.
- Therefore, with this result the proposed peak load shaving was accomplished successfully in simulation, which meant that the project is technically viable.

## 5 Hardware and Software Design

The full Peak Load Shaving technique proposed in this thesis in chapter 2 was completely implemented in simulation as discussed in chapter 4. Due to time constrain however, the focus in practice was to implement the digital PLL PI-based control only as discussed in chapter 3, section 3.4.1.

Thus, this chapter will deal with the hardware and software design of the proposed topology, figure 3.3-1, with a goal in mind of implementing the digital PLL PI-based controller.

Open loop controllers were done simply by controlling manually two potentiometers, whereby one controls the power angle bi-directionally, which control the real power, and the other controls the three-phase amplitude voltage, which controls the reactive power as discussed in chapter 3 section 3.1, which in the sense was the same as using the three-phase inverter as VSI.

Photo 5-1 shows the hardware connection in the laboratory.



Photo 5-1: Laboratory prototype

## 5.1 Hardware design

### 5.1.1 Three-phase supply

The three-phase voltages used in practice came from a three-phase mains supply located at machine laboratory at UCT in the electrical engineering department. The voltage rating was 400 V line-to-line rms. Photo 5.1.1-1 shows the three-phase mains supply.

DS1104 SL - DSP - PWM SV

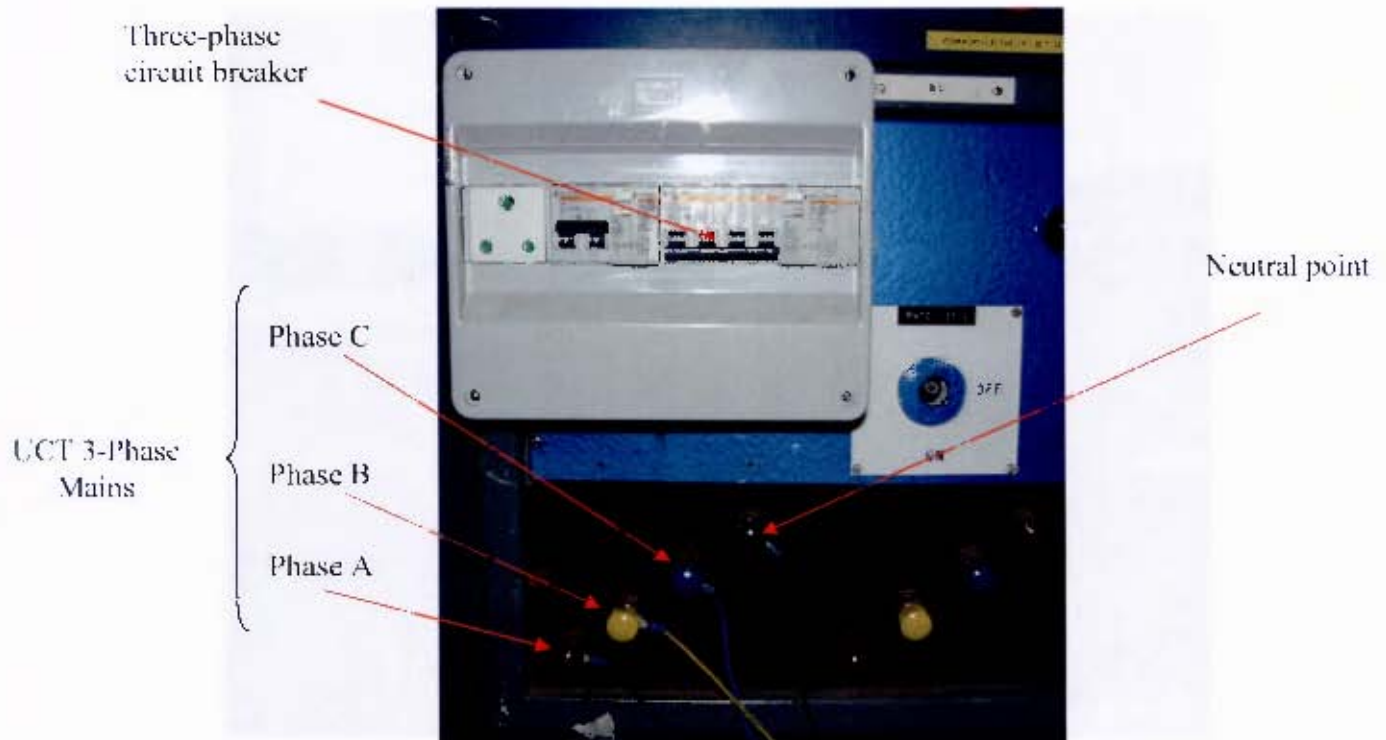
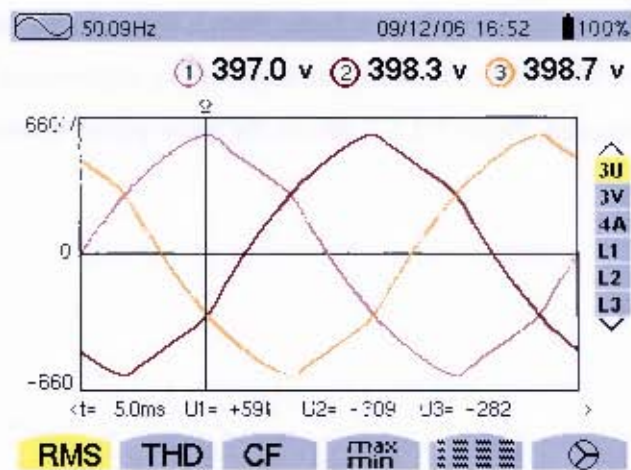


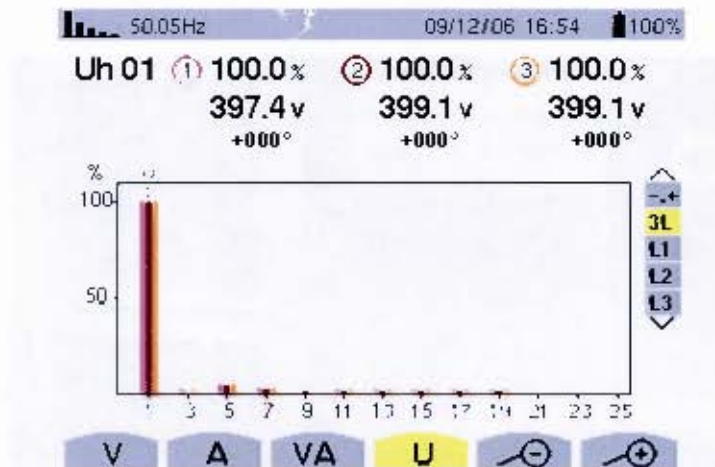
Photo 5.1.1-1: UCT machine laboratory three-phase supply, connected in positive sequence.

The three-phase voltage signals produced at UCT machine lab was not an ideal sinusoidal signal. Power\_Analyser\_Result 5.1.1-1 shows this.



Power\_Analyser\_Result 5.1.1-1: UCT machine lab line-to-line three-phase voltage.

Power\_Analyser\_Result 5.1.1-2 shows the harmonics which UCT machine lab line to line voltage has.



Power\_Analyser\_Result 5.1.1-2: Harmonics content at UCT machine laboratory three-phase supply voltage

Those harmonics were the one responsible for the peak shape in the three-phase voltage of the Power\_Analyser\_Result 5.1.1-1. Those harmonics were originated from the following source:

- The power electronics devices, such as: AC and DC machines drivers, rectifiers, inverters
- Fluorescent lights, computer

### 5.1.2 Three-Phase Load Design

The three-phase load was configured in delta connection; each phase was made of resistors and inductors connected in series as was discussed in section 4.2. To increase the load however the same configuration of resistor and inductor in series were connected in parallel with each phase and in series with a switch. The total capacity was of 8kVA at PF of 0.96.

The inductors and resistors had the following values: 100mH at 5A and average resistor of  $94\Omega$  respectively. Photo 5.1.2-1 illustrates the three-phase load connection done in the lab.

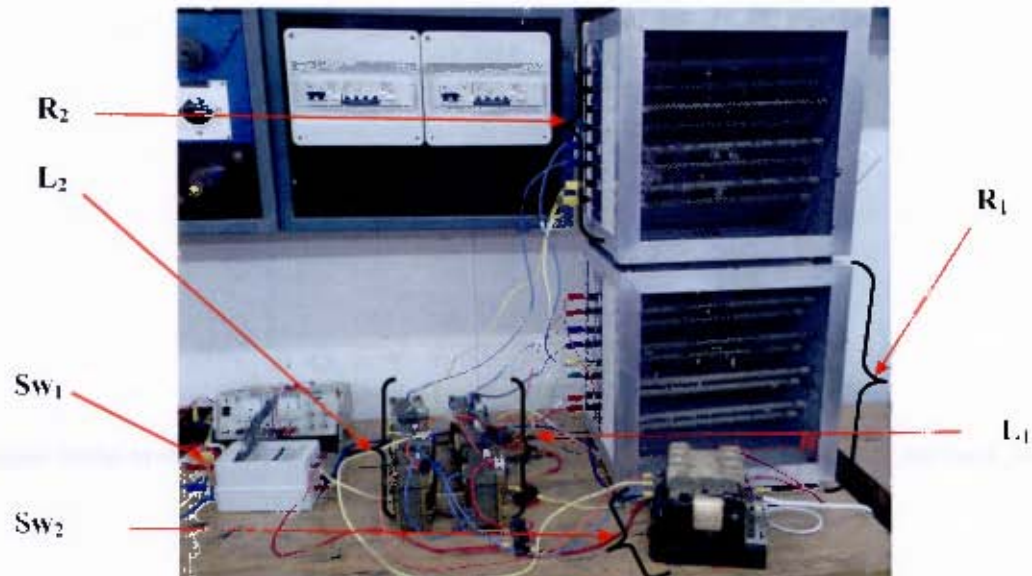


Photo 5.1.2-1: Three-phase Load made of resistors and inductors

Where  $R_1$  and  $L_1$  illustrate the first combination of the three-phase load delta connection, the manual circuit breaker,  $SW_1$ , was used to connect the three-phase load to the three-phase grid. The resistors and inductors  $R_2$  and  $L_2$  were connected in same configuration as  $R_1$  and  $L_1$ .  $SW_2$  is an electrical switch, which its function was to increase the load in each phase. Power\_Analyser\_Result 5.1.2-1 shows the three-phase load power capacity and the PF, before and after closing  $SW_2$



Power\_Analyser\_Result 5.1.2-1: Three-phase load capacity before and after closing  $S_{W2}$

### 5.1.3 Battery storage

The batteries used in the lab were a combination of lead-acid batteries of 12 volts from two different manufactures, First National Battery and Delkor. See photo 5.1.3-1.



Photo 5.1.3-1: Lead-acid battery used in the lab for this thesis

The reason was that there were not enough batteries of the same type available in the lab, however they had the same rating capacities therefore they were compatible to be used together.



Photo 5.1.3-2: Eight Lead-acid batteries assembled to make 96V dc bus

The batteries had the following rating: 12V 102Ah 20 hour. In total, they were 8 batteries connected in series, which increased the total voltage to 96V.

#### 5.1.4 Three-Phase Inverter

The three-phase inverter available had a total capacity of 120kVA. It is made of IGBT's modules, the SKM 200GB123D, see figure 5.1.4-1. Those modules were manufacture by Semikron.

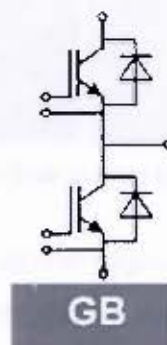


Figure 5.1.4-1: Semikron IGBT modules, the SKM200GB123D

It has a total maximum voltage range of 1200V, at temperature of 25°C, its maximum current capability at temperature of 25°C is 200A and at temperature of 85°C is 180A. Consult the datasheet in accompanied CD.

Photo 5.1.4-1 shows the practical three-phase inverter.

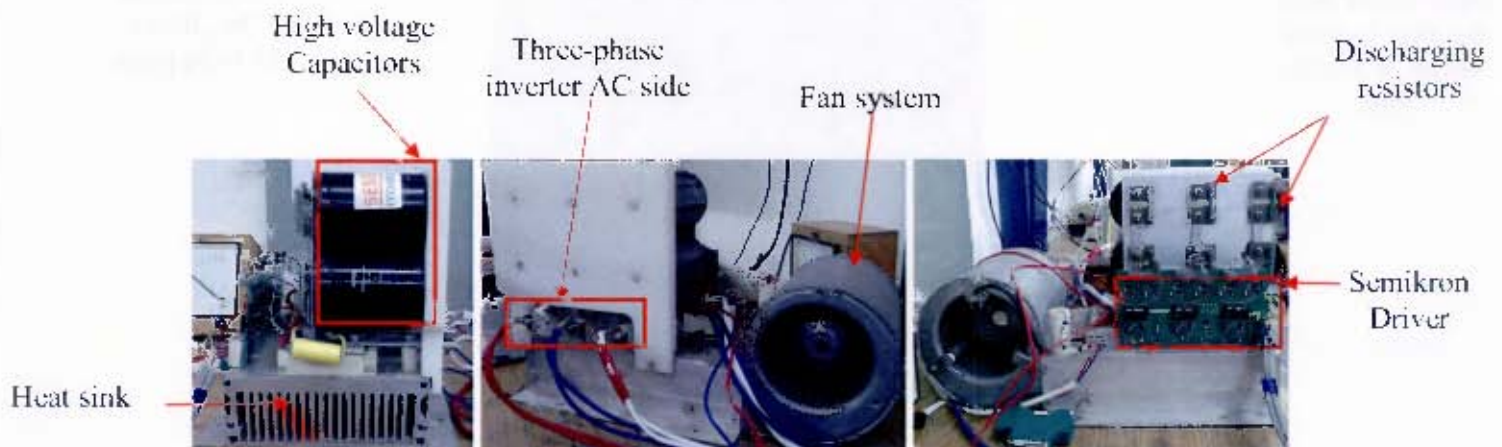


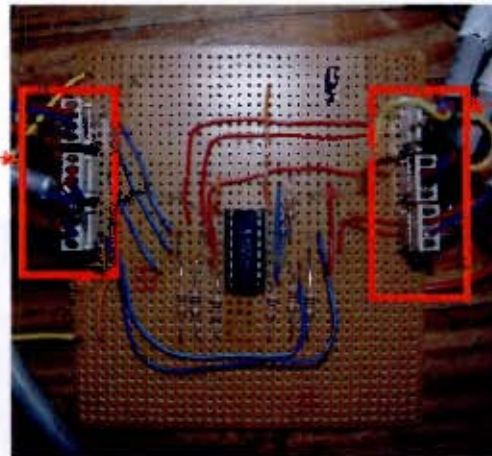
Photo 5.1.4-1: Three-phase inverter used in the lab

The three-phase inverter is composed of following:

- Six high voltage capacitors with 3.3mF each, they are black in color. Its function is to hold the DC bus voltage.
- Heat sink assembled with a fan system, to cool down the SKM200GB123D modules, which were assembled on the heat sink.
- Across the DC bus there is a small capacitor of 0.47uF, yellow in color. Its function is to decrease the voltage ripple of the DC bus voltage.
- Each high voltage capacitors has connected across it a discharge resistors with value of  $22k\Omega$  10W.
- A Semikron driver, which has the function of fire up the IGBT gate with the SVPWM signals coming from the DSP chip. The Semikron driver input voltage was 15V.

However, the signal coming from the DSP had voltage level of 5V. Therefore, to fix the problem a voltage level shifter was built by the author to shift the DSP voltage signal from 5V to 15V. Photo 5.1.4-2 illustrates this.

Input signal from the DSP to level shifter at 5 volts peak



Output signal to the Driver a 15 volts peak

Photo 5.1.4-2: voltage level shifter

### 5.1.5 Three-phase low pass filter

The practical inductors had value of  $440\mu\text{H}$  and a small resistor value due to the inductor windings, the capacitor had value of  $50\mu\text{F}$ . Figure 5.1.5-1 illustrates the LC low pass filter used in practice.



Photo 5.1.5-1: Low-pass filter inductor

Using equation 4.6-3 the cut-off frequency was calculated to be  $1073\text{Hz}$ . As discussed the switch frequency was set to  $10\text{kHz}$ . Thus, the cut-off frequency was 10 times smaller than the switch frequency. Therefore with this cut-off frequency the harmonics frequency were filtered out substantially.

### 5.1.6 Three-Phase Transformer

The three-phase transformer in the lab as discussed previously was made of three single-phase three winding toroidal transformers with the following ratings: 230/54V, 1.5kVA. In appendix F, the single-phase three windings transformer was discuss in detail. In addition, it was concluded that it could be used as a single-phase two windings transformer, just by leaving the third winding open.

No-load test and short circuit test was done in each of the single-phase three windings transformer using only two windings, appendix F section F.3 discussed this. The no-load and short-circuit test result were used to model the single-phase transformer in simulation as discussed in previous chapter. The three single-phase three windings transformer were assembled together to form the three-phase Y- $\Delta$  transformer, as discussed in appendix F section F.5. Photo 5.1.6-1 shows this.

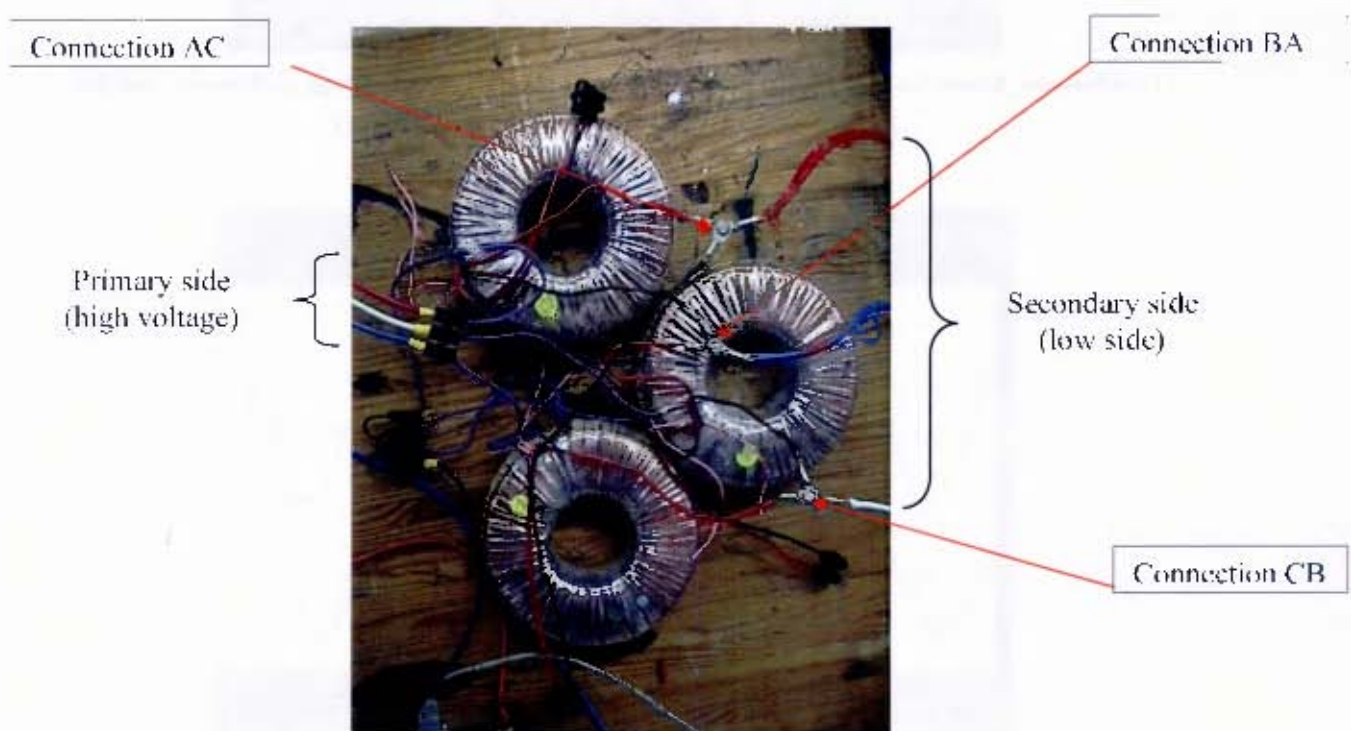
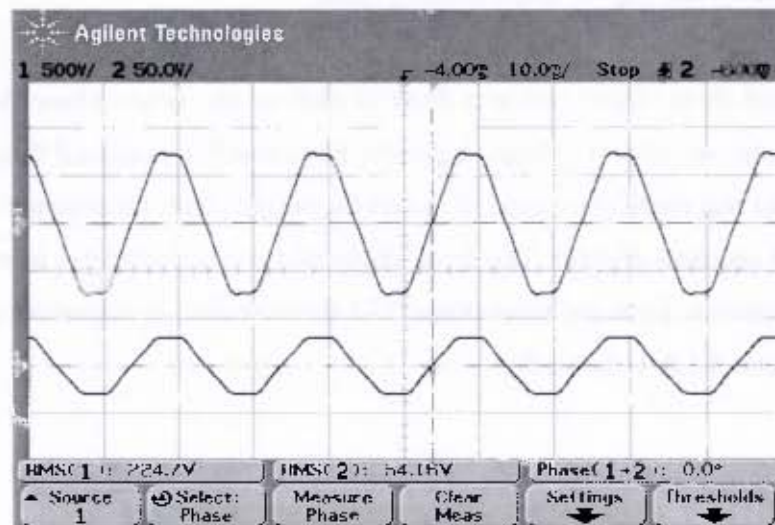
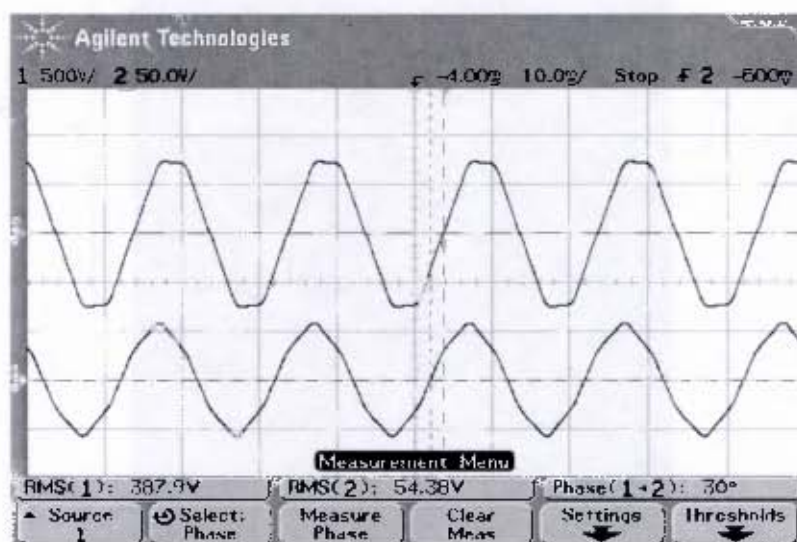


Photo 5.1.6-1: practical single-phase three winding transformer connected as Y- $\Delta$  three-phase transformer

After the connection, a three phase voltage from a three-phase grid of 400V line-line, was applied to the three-phase transformer Y-connection (primary side), while the  $\Delta$ -connection was left unconnected to the three-phase inverter AC side to check if the relation of voltages of the primary and secondary side corresponds with the theory of reference [7] and [29]. The results are shown in Oscilloscope Results 5.6.5-1 and 5.6.5-2.



Oscilloscope\_Result 5.1.6-1: Three-phase transformer primary phase voltage in channel 1 and the corresponded secondary phase voltage in channel 2



Oscilloscope\_Result 5.1.6-2: Three-phase transformer primary voltage line to line in channel 1 and corresponded secondary voltage line to line in channel 2

From the Oscilloscope\_Result 5.1.6-1 and 5.1.6-2 it can be seen that the three-phase transformer was successfully connected from the three single-phase three winding transformers. Recalling from the theory of the Y- $\Delta$  three-phase transformer [7], the delta line-to-line voltage ( $V_{AC}$ ) is in phase with the Y line to neutral voltage ( $V_{an}$ ) and out phase by 30 degree with Y line-to-line voltage ( $V_{ae}$ ).

## 5.2 Software design

The brain of the project was the DSP chip, thus all the signals were loaded into it to be processed. The DSP used was very sensitive to voltage level. The range of voltage level it accepted was between 0 and 3.3V. Therefore, a voltage level out of this range would damage the DSP.

Therefore LEM transducers were used to step down the high signals to low signals either to a peak-to-peak signal of 3.3V if it is an AC signal or to maximum voltage of 3.3V if it is a DC signals.

The peak-to-peak signal before it was sent into the DSP chip it had to be shifted up to lie between zero and a maximum voltage of 3.3V. To accomplish this, an interface board was used, which will be discussed in much detail later.

Recalling that in the practice, the aim was only to implement the PLL PI-based controller as discussed in section 3.4.1, due to time constrains; therefore, the only LEM transducer used was the voltage transducer.

To accomplish the PLL PI-based controller successfully, different steps had to be taken such as:

- Implementation of SVPWM algorithm as discussed before, which had the aim of switching on and off the three-phase inverter, in such way that the magnitude and phase of the three-phase inverter voltage would be controlled. The SVPWM algorithm used in practice was an adaptation of code written in the DSP chip by a

previous student [36]. The signals that were needed to implement the SVPWM algorithm were the battery voltage and the voltages in stationary reference plane,  $V_\alpha$  and  $V_\beta$ .

- Clark transformation algorithm was an essential piece of code. It helped to obtain the signals  $V_\alpha$  and  $V_\beta$ . The Clark transformation used in this thesis was written by the author. It used as input two line to line three-phase grid voltages  $V_{ac}$  and  $V_{bc}$  and they were  $60^\circ$  out phase from each other.
- Parke transformation algorithm was also written by the author and it was implemented successfully in the DSP chip. As discussed in appendix C, it transformed  $V_\alpha$  and  $V_\beta$  from the stationary reference plane to the rotating reference plane,  $V_d$  and  $V_q$ . Consequently, with this algorithm there was a freedom to control manually the three-phase inverter phase and magnitude.

The next section will discuss the implementation of the voltage transducer to step down the voltage signals needed in the DSP chip.

### **5.2.1 Voltage sensors design**

The type of voltage transducer used was manufactured by LEM Components. The choice of the voltage transducer range depended mainly on the voltage range. As was discussed in previous section, the topology used for this project, made the use of Y- $\Delta$  three-phase transformer, which is step down transformer.

The voltage measurements needed to accomplish the PLL PI-based controller in practice, were taken in low side ( $\Delta$ -side) of the three-phase transformer as well as on the DC bus of the battery storage. Recalling the three-phase transformer voltage had value of 55.4V line to line and the battery nominal voltage of 96V. Therefore, the voltage transducer used was the LV 25-P, which its voltage range was from 10 to 500V, see appendix H.

As explained on the datasheet appendix H, the voltage transducer LV25-P is used for electronic measurement of voltages either DC or AC signal. It has a built in galvanic

isolation between the high voltage side and the electronics side (lower voltage side). Its advantage and Applications are stated in appendix H.

### 5.2.1.1 AC voltage transducer LEM design

From appendix H, the LV 25-P electrical connection is represented schematically as shown in figure 5.2.1.1-1.

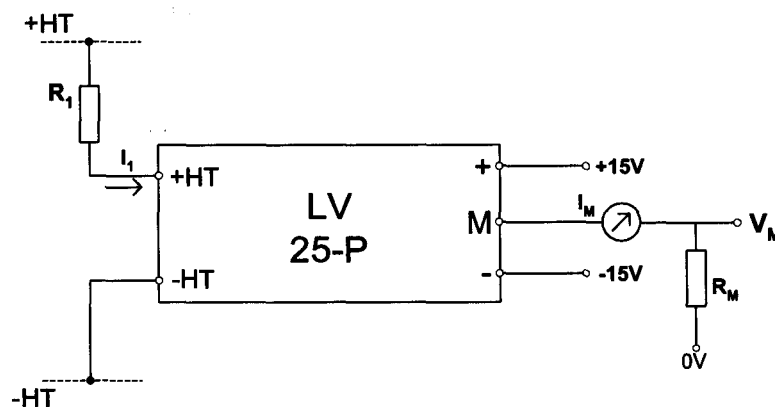


Figure 5.2.1.1-1: Voltage LEM Connection drawing

Where, +HT and -HT is the high or primary side terminal input voltage, whereby the terminal +HT is defined with respect to -HT. For instance if +HT receives phase A voltage and -HT receives phase B voltage, then the voltage entering in, would be defined as  $V_{AB}$ . The variable  $R_1$  and  $I_1$  are the primary side resistor and current respectively, where  $R_1$  is the variable to be calculated and  $I_1$  has nominal rms current of 10mA, see appendix H.

The voltage values of +15V, -15V and 0V are the output voltage of a 15 volt split DC power supply, which the LV 25-P would need to be able to operate. This LV 25-P can also operate with a DC voltage level of +12V, -12V and 0V, refer appendix H, however the measurement resistor,  $R_M$ , would have different operating range of resistors values.

Variable  $I_M$  and  $V_M$  are the measurement current and voltage of the secondary side of the LV 25-P respectively.  $V_M$  is the input voltage level of the secondary device, which in this case is the DSP chip, which has maximum voltage of 3.3V as discussed previously.

The secondary nominal rms current is 25mA. LV 25-P conversion ratio was defined to be 2500:1000 in appendix H. Therefore, the relation between the primary and secondary current is defined as shown in equation (5.2.1.1-1). The value of  $R_M$  must be chosen such that the current flowing through it produces the required input voltage of the secondary device.

$$I_M = 2.5 \cdot I_1 \quad (5.2.1.1-1)$$

Equation 5.2.1.1-1 helped to relate the primary and the secondary side of the LV 25-P, see figure 5.2.1.1-1. The equation in primary side of the voltage transducer is defined by ohms law as it is shown in equation 5.2.1.1-2.

$$V_1 = R_1 \cdot I_1 \quad (5.2.1.1-2)$$

In addition, the secondary equation was defined as illustrated in equation 5.2.1.1-3.

$$V_M = R_M \cdot I_M \quad (5.2.1.1-3)$$

Now substituting equation (5.2.1.1-1) into (5.2.1.1-3), equation (5.2.1.1-4) was obtained.

$$V_M = R_M \cdot 2.5 \cdot I_1 \quad (5.2.1.1-4)$$

Moreover solving for  $I_1$  in the equation (5.2.1.1-2) and then substituting into the equation (5.2.1.1-4), and at same time solving for the high side voltage  $V_1$ , equation (5.2.1.1-5) was obtained.

$$V_1 = \frac{R_1 \cdot V_M}{R_M \cdot 2.5} \quad (5.2.1.1-5)$$

The voltage transducer operates at its optimum accuracy when nominal primary current is drawn. Therefore from appendix H it was advised that  $R_I$  should be calculated in such way that the primary voltage been applied should force a current of 10mA to flow. With this criteria and nominal voltage of 55.4 V line to line,  $R_I$  was calculated to be 5.5 k $\Omega$ .

From previous section, it was seen that the DSP only accept voltage between 0 and 3.3V, which mean that the  $V_M$  peak to peak voltage (for AC voltage signal) has to have a value of 3.3V. Using the conversion ratio, the secondary rms current that would flow through  $R_M$  is 25mA.

To calculate the accurate value of  $R_M$  the peak-to-peak voltage should be changed to r.m.s value or conversely the current should be change to peak-to-peak current. Thus having the voltage and the current in one form only, the  $R_M$  calculated was 47 $\Omega$ .

However, from the electric data on the data sheet, appendix H, the minimum measurement resistor  $R_M$  when using a supply voltage of +15 and -15 V must be 100 $\Omega$ . Therefore using the minimum advisable measurement resistor value of 100 $\Omega$  the secondary rms current using equation 5.2.1.1-3 was calculated to be 11.67mA r.m.s.

With this new secondary current, the primary current was calculated to be 4.67mA, which from the data sheet a primary current drawing current of 5mA has accuracy of  $\pm 1.6\%$  at 25 $^{\circ}$ C. The primary current of 4.67mA is very close to the advisable optimum accuracy. So the primary resistor  $R_I$  for the primary voltage of 55.4 V and current of 4.67mA was calculated to be 11.86 k $\Omega$ . Table 5.2.1.1-1 and 5.2.1.1-2 below illustrate the calculated and actual values.

Table 5.2.1.1-1: AC voltage transducer calculated parameters

Given			Calculated			
$V_{AC}$ [V]r.m.s	$V_M$ [V] pk-pk	Current Ratio	$I_I$ [mA]r.m.s	$I_M$ [mA]r.m.s	$R_M$ [ $\Omega$ ]	$R_I$ [k $\Omega$ ]
55.4	3.3	2.5	4.67	11.67	100	11.86

Table 5.2.1.1-2: AC voltage transducer actual parameters

Given			Calculated			
$V_{BC}$ [V]r.m.s	$V_M$ [V] pk-pk	Current Ratio	$I_I$ [mA]r.m.s	$I_M$ [mA]r.m.s	$R_M$ [ $\Omega$ ]	$R_I$ [k $\Omega$ ]
55.4	3.3	2.5	4.54	11.29	103.3	12.2

However, using the actual resistor in practice the peak-to-peak voltage,  $V_M$ , due to the noise was higher than 3.3V pk-pk. So  $R_I$  was calculated to ensure that the  $V_M$  was below 3.3V. Thus,  $R_I$  was calculated to be 13.7k $\Omega$ . Two voltages LEM were designed, which had as input voltage two line-to-line voltages  $V_{AC}$ ,  $V_{BC}$ .

### 5.2.1.2 DC voltage transducer LEM design

The same procedure used to calculate the parameters for the AC LEM voltage transducer was used to calculate the parameter for the DC LEM voltage transducer. Thus, the same LV 25-P LEM module was used.

The DC voltage source was from a bank of lead acid batteries of 12 voltages each. As discussed in section 5.1.3, the total number of batteries connected in series was 8, which brought up the nominal DC voltage to 96 V.

However, the choice of the DC voltage to design the LEM voltage transducer parameter had to be the maximum possible voltage that the battery would raise. In this way, the DSP maximum voltage would not be surpassed.

In section 2.4.3, it was discussed that when the battery is being charged, it reaches the constant voltage region with a value ranging from 2.3- 2.45V per cell, or 13.8-14.7 for the 12 volts battery. The choice of the specific voltage depends on the battery temperature as discussed previously. Thus for 8 batteries connected in series, its boost voltages would range from 110.4-117.6V.

Furthermore, if equalization is needed the voltage can be raised to a value of 15 V (for a battery of 12 voltage) per battery [10], thus for 8 batteries connected in series, the voltage would be 120 V. In light of the above, 120 V was used as the maximum input primary voltage for the DC voltage transducer.

Using equation 5.2.1.1-2 and the nominal primary current of 10mA,  $R_i$  was calculated to a value of 12 k $\Omega$ . The secondary current  $I_M$  was set to 25mA by using the current conversion ratio of 2.5. Knowing the maximum nominal input voltage that DSP can handle, the measurement resistor was calculated to a value of 132  $\Omega$ . The calculated resistor value is within the range of  $R_{Mmax}$  and  $R_{Mmin}$  see appendix H. The calculated values and the actual values are illustrated in table 5.2.1.2-1 and table 5.2.1.2-2.

**Table 5.2.1.2-1: DC voltage transducer calculated parameters**

Given			Calculated			
$V_{DC}[V]$	$V_M[V]$ max	Current Ratio	$I_i[mA]$ r.m.s	$I_M[mA]$ r.m.s	$R_M[\Omega]$	$R_i[\Omega]$
120	3.3	2.5	10mA	25mA	132	12k

**Table 5.2.1.2-2: DC voltage transducer actual parameters**

Given			Calculated			
$V_i[V]$	$V_M[V]$ max	Current Ratio	$I_i[mA]$ r.m.s	$I_M[mA]$ r.m.s	$R_M[\Omega]$	$R_i[\Omega]$
120	3.3	2.5	10mA	25mA	132	12.2k

### 5.2.2 Interface board design

Once the voltage transducers were designed and implemented as discussed previously, the three-phase grid voltage line to line,  $V_{AC}$  and  $V_{BC}$  as well as the battery voltage,  $V_{DC}$ , were step down to the DSP input voltage range.

However, those signals could not be sent directly into the DSP, because of the noise level contained in the signals. In addition, for the AC signals, it was also because the peak-to-peak voltages were attaining negative values.

Therefore, an interface board was a very essential part for the software design, because it helped for the conditioning of the voltage signals. Such that the noise level could be decreased and the voltage level shifted to fit into the DSP input voltage range. Photo 5.2.2-1 shows the interface board used for this project.



TL064

Photo 5.2.2-1: interface board

This interface board was made of four chips, the TL064 (a low power J-FET quad operational amplifier), as well as potentiometers, resistors, capacitors, transistors, relays and diodes. Each TL064 has built inside four Op-Amps, which were assembled in pair to form two inverting Op-Amps in series. Figure 5.2.2-1 illustrates this.

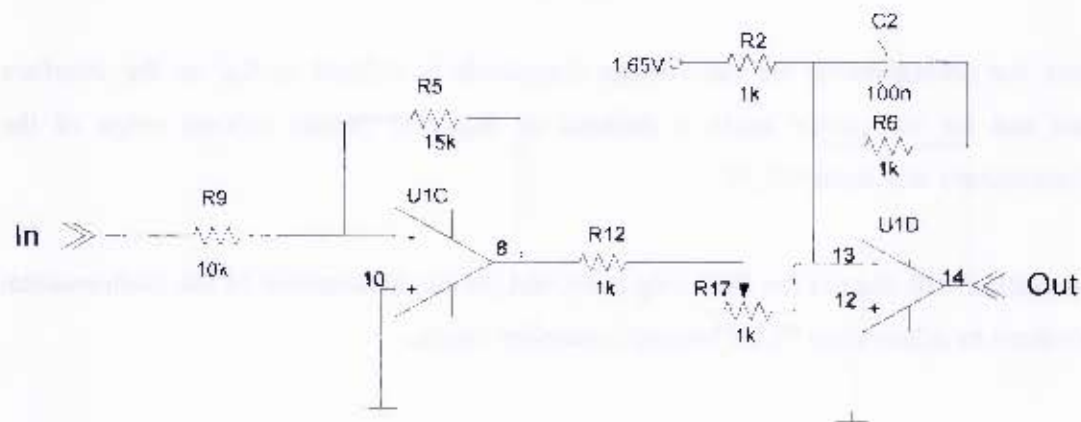


Figure 5.2.2-1: Inverting amplifiers assembled on the interface board

The two inverting Op-Amps were connected together as shown in figure 5.2.2-1, to eliminate the effect of sending into the DSP the inverted original signal while the interface board was conditioning the voltage signals.

The noise in the voltage signals were substantially reduced by using the capacitor  $C_2$ . Resistor  $R_2$  was used to level shift the peak-to-peak AC signal voltage to be above zero and below 3.3V, however for the DC signal  $R_2$  was removed. Resistor  $R_{17}$ , a potentiometer, was used to adjust the output Op-Amp (U1D) voltage gain, such that the output voltage was adjusted to be within the DSP acceptable voltage range.

Once the voltage signals were conditioned, they were ready to be sent into the DSP chip, which was done. However, beside these calculated signals, two other signals were sent into the DSP, which were the two signals coming from two potentiometers that are located on the interface board; photo 5.2.2-2 illustrates the potentiometers.

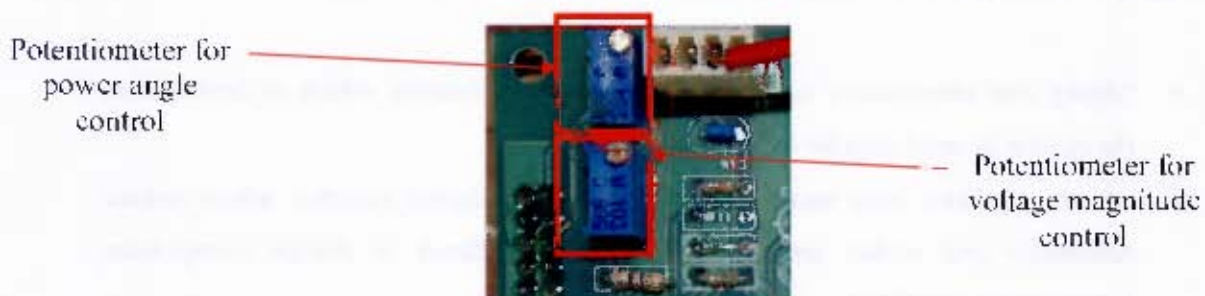


Photo 5.2.2-2: Potentiometers for power angle and voltage magnitude control

Where the potentiometer for the voltage magnitude is defined as  $R_{90}$  on the interface board and for the power angle is defined as  $R_{88}$ . The output voltage range of the potentiometers was from 0-3.3V.

Next section will discuss the DSP chip used and the implementation of the mathematical algorithms to achieve the PLL PI-based controller results.

### **5.2.3 Digital signal processor controller**

The digital signal processor (DSP) controller used for this project was manufactured by Texas Instruments [37]. However, the control design for this project could also be accomplished by using analog systems design or microcontrollers. Thus, why then using the DSP chip?

K.M.Chung, A.Wu, and T.Hidajat [38], discussed that by comparing the analog controller with digital systems, it was seen that the “*analog controls offer two distinct advantages over the digital systems*”, which are:

- “*Higher speed control by processing input data in real time.*” [38]
- “*Higher resolution over wider bandwidths because of infinite sampling times.*” [38]

However, the analog systems have some disadvantages, which made the choice of using analog system design unattractive one. The disadvantages are listed below:

- “*Aging and temperature can cause component variations, which in turn causes the system to need regular adjustment.*”[38]
- “*Analog systems have more physical parts than digital systems, which reduce reliability and makes analog systems more difficult to design (component tolerance issues).*”[38]

- *“Upgrades are difficult because the design is hardwired.”*[38]

The microcontrollers in other hand have the following advantages:

- *“Drift is eliminated since most functions are performed digitally.”*[38]
- *“Upgrades are easily made in software.”*[38]
- *“Part count is reduced because the microcontroller can handle several function on-chip.”*[38]

It was said that the *“microcontroller are good for systems that do not require high speed or precision”* [38]. Therefore, for systems, that does require high speed or precision, the microcontroller fails to be an eligible choice.

Chung, Wu and Hidajat [38] however, stated that the DSP-based controllers are a fusion of the advantages of the microcontrollers and the analog systems, which consequently enabled the DSP-based controller to be able to implement math-intensive algorithms; as a result, the system cost was lowered.

Some benefits of the DSP-based controller as stated by Chung, Wu and Hidajat are shown below, the rest can be found in reference [38].

- *“Control power switching inverters and generate high-resolution PWM outputs.”*  
[38]
- *“System cost reduction by an efficient control in all speed ranges, implying right dimensioning of power device circuits.”*[38]
- *“Reduced harmonics using enhanced algorithms to meet easier requirements and reduce filter cost.”*[38]
- *“Single chip control system.”*[38]

Photo 5.2.3-1 shows the Texas Instrument DSP-based controller used for this project, the TMS320LF2407A.



Photo 5.2.3-1: Texas Instrument DSP, TMS320LF2407A

The TMS320LF2407A chip was assembled in the board as shown in the photo 5-12 by a MLT Drives. MLT Drives is a renewable source of energy South African company, based in Cape Town [39].

### 5.2.3.1 The TMS320LF2407A

The TMS320LF2407A belongs to the TMS230 family of chip, specifically the 16-bit fixed-point one. The TMS230 family consists of the following family members: Fixed-point, Floating-point, Multiprocessor DSPs and Fixed-point DSP controllers [37].

The TMS230 family architecture design is used for real time signal processing. Moreover, the combination of the real time signal processing with the controller peripherals gave rise for the 240xA series of DSP controller. They are ideal chips to be used for application solution of control system; its characteristics are described below [37]:

- “*Very flexible instruction set.*”[37]
- “*Inherent operational flexibility.*”[37]
- “*High-speed performance.*”[37]
- “*Innovative parallel architecture.*”[37]
- “*Cost effectiveness.*”[37]

Figure 5.2.3.1-1 shows the 240xA devices architecture as discussed in [37].

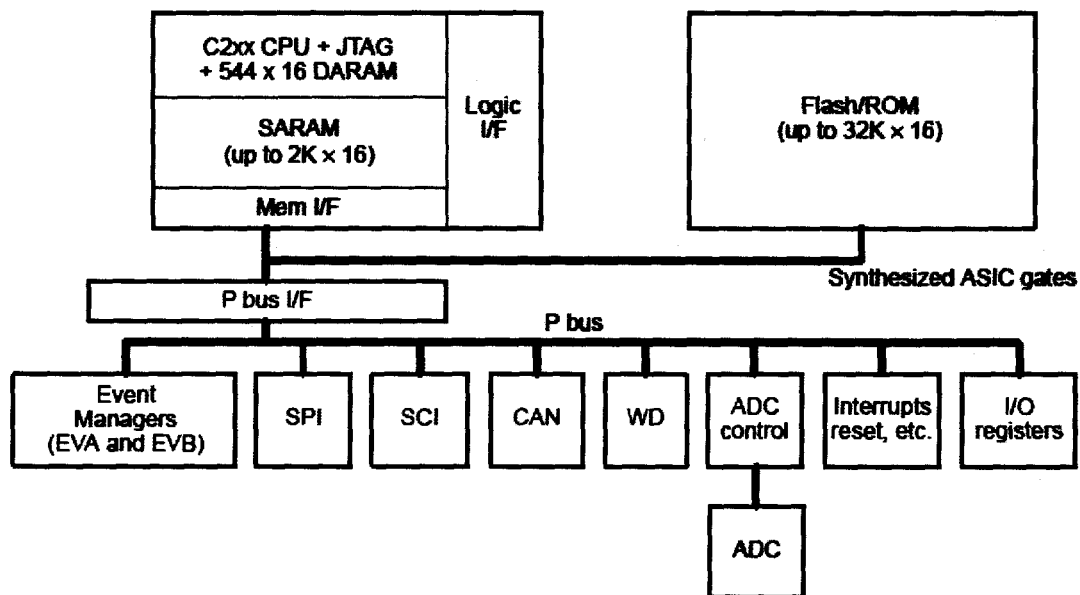


Figure 5.2.3.1-1: 240xA Device Architecture [37]

The TMS320LF2407A features are discussed in reference [40]; however, some relevant ones are listed below:

- A 10-bit analog-to-digital converter (ADC) control,
- I/O registers, which used the \*MCRA register to set the PWM1-6 output pins.
- Event Managers EVA, which used the register \*EVAIMRA (interrupt mask register A) to enable the timer1 underflow interrupt.
- Serial peripheral interrupter (SPI) had the function to set up the 8-bit digital-to-analog converter (DAC), for debugging the code.

The TMS320LF2407A can be programmed either in assembly language, which is a low language or machine language [37, 38, 41] or in high level language [41]. The high level language used to program the DSP chip for this thesis was a C++ language, which used a C compiler to program the chip.

### 5.2.3.2 Digital representation of all the signals

As was discussed previously, the output signals on the secondary side of the voltage transducer are voltage signals that range from zero to 3.3V. These signals were the input of the ADC in the DSP chip.

The ADC as mentioned previously is 10-bit, which meant that it would resolve the input voltage [0-3.3V] into [0-1024count] levels inside the DSP, where  $1024 = 2^{10}$ . The equation (5.2.3.2-1) relates the output voltage of the ADC and its input voltage.

$$V_{DIG} = \frac{1024}{3.3} \cdot V_M \quad (5.2.3.2-1)$$

Where  $V_{DIG}$  is the ADC output voltage and  $V_M$  is the ADC input voltage, which as discussed previously is also defined as the output of the voltage LEM.

### 5.2.3.3 Signals Transformation to real values inside the DSP

Once the signals were inside the DSP chip they were in the range of 0 to 1024 counts, which as discussed before, in voltage it were in range of 0 to 3.3V. However, for calculation purpose, those signals must be transformed back to their real values.

Recalling from section 5.2.2, the signals used were the following:  $V_{AC}$ ,  $V_{BC}$ ,  $V_{DC}$ , the power angle potentiometer (pot<sub>1</sub>) and the voltage magnitude potentiometer (pot<sub>2</sub>).

Substituting equation (5.2.3.2-1) into (5.2.1.1-5), equation (5.2.3.3-1) was obtained.

$$V_1 = \frac{R_1 \cdot 3.3 \cdot V_{DIG}}{R_M \cdot 2.5 \cdot 1024} \quad (5.2.3.3-1)$$

The real voltage signal  $V_{AC}$ ,  $V_{BC}$  and  $V_{DC}$  were represented inside the DSP as shown in equation (5.2.3.3-2) and (5.2.3.3-3). Notice though that  $V_{BC}$  has the same value as  $V_{AC}$  because the resistances  $R_I$  and  $R_M$  for  $V_{AC}$  and  $V_{BC}$  had identical values.

$$V_{AC} = V_{BC} = \frac{175}{1024} \cdot V_{DIG} \quad (5.2.3.3-2)$$

$$V_{DC} = \frac{122}{1024} \cdot V_{DIG} \quad (5.2.3.3-3)$$

However, before scaling the AC digital signals to their real values, they must be level shifted to lie between a negative maximum value and a positive maximum value, refer to appendix J.

#### 5.2.3.4 DSP Fixed-Point arithmetic

From the DSP section it was discussed that the DSP chip used was a 16-bit fixed-point processor, which meant that its number representation for calculation purposed must have an integer format, a whole number [42].

A digital number inside the DSP chip is represented in binary format as  $2^N$ , where N is the number of bit. Thus, the maximum value for this processor is 65,536 ( $2^{16}$ ) [42]. However, usually the 16-bit processor is used as two's complement representation, to ensure that the DSP chip would handle negative values [42, 43]. In this format, the maximum negative and positive values are represented as illustrated in the equation (5.2.3.4-1).

$$-2^{16-1} < i < 2^{16-1} - 1 \rightarrow -32,768 < i < 32,767 \quad (5.2.3.4-1)$$

However if two integers numbers are multiplied together, whereby their values happen to be at their maximum point as equation (5.2.3.4-1), then the result would be a 32 bit,

chip. To overcome this situation sample time was redefined using Q format. Equation (5.2.3.4-3) represents this.

$$K_I \cdot T_s = 0.002 \cdot 2^{15} = 66 \quad \text{Q15} \quad (5.2.3.4-3)$$

Equation (5.2.3.4-4) presents how equation (5.2.3.4-2) was written in the code.

$$Y\_PLL = (\text{int}) ((66 * (\text{long int}) U\_PLL) / 32768 + (\text{long int}) Y\_kI\_PLL); \quad (5.2.3.4-4)$$

In equation (5.2.3.4-4) as mentioned above,  $Y\_PLL$ ,  $U\_PLL$ , and  $Y\_kI\_PLL$  were defined as integer. The variable  $U\_PLL$  and  $Y\_kI\_PLL$  were converted to long integer temporarily for calculation purpose. As illustrate in equation (5.2.3.4-4), once the calculation is done the results is converted back to integer by typecasting it.

### 5.3 Chapter Summary

From the above discussion, the following points are summarized:

- The prototype to implement the peak load shaving was successfully designed and implemented in the lab with a changed three-phase resistive and inductive load. The load could be changed from 4.3kVA at PF of 0.96 to 8.9kVA at PF of 0.96.
- However, due to time constrain only PLL PI-based controller would be implemented in the lab. Therefore, the only LEM transducers that were built were the voltage transducers.
- The signals for PLL PI-based controller,  $V_{AC}$ ,  $V_{BC}$  and  $V_{DC}$  were successfully conditioned by the interface board and sent to the DSP at the right voltage range.
- Fixed-point arithmetic Q-format was used successfully in DSP chip, which help to represent float number as integer numbers.

which wouldn't fit inside the 16 bit register or an integer variable. Consequently, some information would be lost.

Thus, to prevent this from happening, a C-language function, the typecasting [44], was used as well as some fixed-point arithmetic manipulation, such as Q format. Typecasting has the function to convert any C data type to another data type.

Reference [42] (page 4 of 5), states that “*Q-format is a technique for tracking the relative location of the radix point within arithmetic input and operation results*”. In addition, “*this is important since certain operations such as multiplication can shift the location of the radix point in the operation result.*”

Recall from section 3.4.1.4, the PLL PI-based controller integral equation (3.4.1.4-8)

$$y_k = K_I T_s u_k + y_{k-1} \quad (5.2.3.4-2)$$

Thus for the 16 bit system the maximum Q-format is represented as Q15 or  $2^{15}$ . Now to represent the product  $K_I \cdot T_s$  on Q-format, Q15 was multiplied to it. Moreover by multiplying by Q15 it is the same as shifting a bit to the left 15 times, which meant that if the number that was being multiplied was already 15 bit, therefore it would increase to 32 bits.

Conversely, by dividing by Q15 is the same as shifting a bit to the right 15 times [43]. Thus for an integer variable to be able to store the bits that were shifted to the left or multiplied, they had to be converted to a long integer temporarily using the typecasting function. The long integer variables are 32 bits.

Recall that the sample time,  $T_s=100\mu\text{s}$ , the integral gain from the simulation was set to  $K_I=20$ . In the code  $y_k$ ,  $u_k$  and  $y_{k-1}$  were defined as integer, see appendix J. The sample time was a float number, 0.000001s, in this way it cannot be used in fixed-point DSP

chip. To overcome this situation sample time was redefined using Q format. Equation (5.2.3.4-3) represents this.

$$K_f \cdot T_s = 0.002 \cdot 2^{15} = 66 \quad \text{Q15} \quad (5.2.3.4-3)$$

Equation (5.2.3.4-4) presents how equation (5.2.3.4-2) was written in the code.

$$Y_{PLL} = (\text{int}) ((66 * (\text{long int}) U_{PLL}) / 32768) (\text{long int}) Y_{kl\_PLL}; \quad (5.2.3.4-4)$$

In equation (5.2.3.4-4) as mentioned above,  $Y_{PLL}$ ,  $U_{PLL}$ , and  $Y_{kl\_PLL}$  were defined as integer. The variable  $U_{PLL}$  and  $Y_{kl\_PLL}$  were converted to long integer temporarily for calculation purpose. As illustrate in equation (5.2.3.4-4), once the calculation is done the results is converted back to integer by typecasting it.

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From the above discussion, the following points are summarized:

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- Fixed-point arithmetic Q-format was used successfully in DSP chip, which help to represent float number as integer numbers.

Next chapter will show the laboratory result focusing mainly on the PLL PI-based controller.

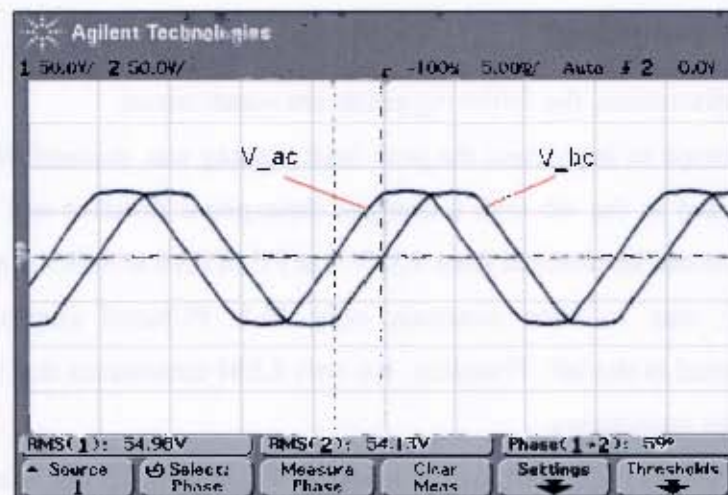
## 6 Result and discussion

This section will discuss firstly the laboratory results of the three-phase inverter in conjunction with lead acid battery, focusing mainly in the implementation of digital PLL PI-based controller, section 6.1. Thus, its technical viability can be shown practically. Secondly, section 6.2 will discuss whether the project at UCTMS will be financial viable or whether it will not be.

### 6.1 Laboratory Result

#### 6.1.1 Three-Phase transformer line to line voltage from lower side

Oscilloscope\_Result 6.1.1-1 illustrates the result of the three-phase transformer secondary (lower side) line-to-line voltage,  $V_{AC}$  and  $V_{BC}$ .



Oscilloscope\_Result 6.1.1-1: Three-phase transformer line-to-line secondary voltage

The voltage  $V_{AC}$  and  $V_{BC}$  were then sent into the voltage transducer to be stepped down as discussed previously. Once all the relevant signals,  $V_{AC}$ ,  $V_{BC}$  and  $V_{DC}$  were conditioned and sent into the DSP chip, the discussed algorithms such as Clarke Transformation, Park Transformation, SVPWM and PLL PI-based control were implemented. The following sections will present their results

### 6.1.2 Clarke transformation result

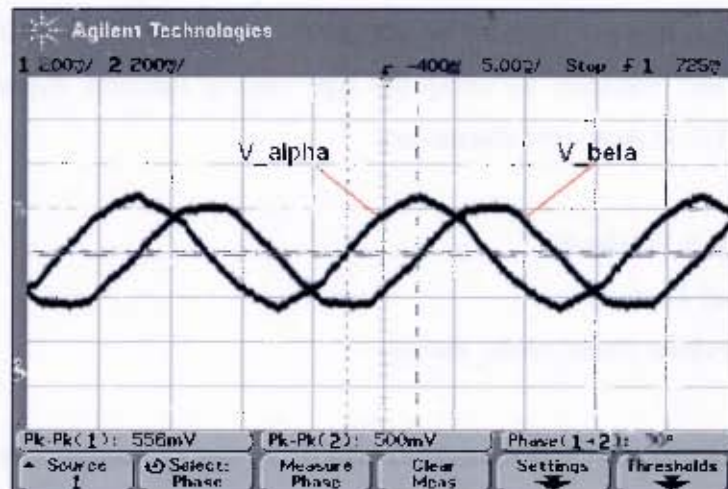
The Clarke transformation was already implemented by the author in his under graded thesis, using equation (4.8-1) without the coefficient  $\sqrt{\frac{2}{3}}$ . This was because there was a difficult implementing equation (4.8-1) in C coding. However, for this Master thesis, equation (4.8-1) was implemented successfully together with the coefficient, equations (6.1.2-1) and (6.1.2-2) illustrates how they were implemented in C coding, appendix J.

$$V_{alpha} = (VaRealV * 13377) / 16384 - (VbRealV * 6688) / 16384; \quad (6.1.2-1)$$

$$V_{beta} = (VbRealV * 11585) / 16384; \quad (6.1.2-2)$$

Where, the ratio  $\frac{13377}{16384} = \frac{\sqrt{2}}{\sqrt{3}}$ ,  $\frac{6688}{16384} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{1}{2}$  and  $\frac{11585}{16384} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{\sqrt{3}}{2}$ .

The variable  $V_{alpha}$ ,  $V_{beta}$ ,  $VaReal$  and  $VbReal$  were defined as long integer, to ensure that the multiplication with a big number would not overflow the maximum available bit space in the variables. In addition,  $VaReal$  and  $VbReal$  represent  $V_{AC}$  and  $V_{BC}$  respectively, Oscilloscope Result 6.1.2-1 shows the result of equations (6.1.2-1) and (6.1.2-2).



Oscilloscope Result 6.1.2-1: Result of Clarke Transformation

Comparing the waveform results of Oscilloscope Result 6.1.2-1 with the result of figure 7 in the literature [17], page 22, it was understood that the SVPWM was operating at full modulation index,  $m=1$ . At this modulation index it was added as discussed previously that the output fundamental voltage would be reduced compared with desired voltage value. Later section will show this.

### 6.1.3 Three-phase grid phase angle result

Recalling equation (3.4.1.1-2) in section 3.4.1.1, it was used to calculate the three-phase grid angle in simulation as well as in practice. As it was illustrated, it receives as input the two signals calculated previously,  $V_\alpha$  and  $V_\beta$ .

In the code an arctan function, “*int arctan (int Re, int Im)*”, was used, refer to appendix J. As it can be seen from above sentence, this function input and output values were defined as integer. The variables “*Re*” and “*Im*” represent  $V_\alpha$  and  $V_\beta$  respectively. However as discussed in the previous section  $V_\alpha$  and  $V_\beta$  were defined as long integer, which meant that if they were inserted in the arctan function as long integer it wouldn't work.

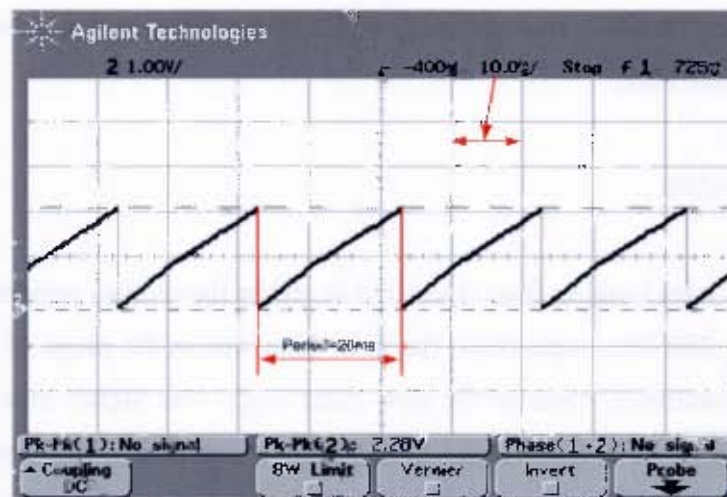
Thus, the values of  $V_\alpha$  and  $V_\beta$  calculated from the previous section were divided by 4, so that the result could fit inside the arctan function integer variable (for this project dividing by 4 was sufficient, however it could be a number higher than 4). In addition, they were converted into “*int*” variables by using the type casting function. Equations (6.1.3-1), (6.1.3-2) and (6.1.3-3) shows the discussion.

$$valpha\_dummy = (int) Valpha/4; \quad (6.1.3-1)$$

$$vbeta\_dummy = (int) Vbeta/4; \quad (6.1.3-2)$$

$$theta = arctan (valpha\_dummy, vbeta\_dummy); \quad (6.1.3-3)$$

Oscilloscope\_Result 6.1.3-1 illustrates the result of the three-phase grid angle, equation (6.1.3-3).



Oscilloscope\_Result 6.1.3-1: Three-phase grid angle, theta

It can be seen from Oscilloscope\_Result 6.1.3-1 above, that the waveform had period of 20ms, which meant that, the angle was rotating at 50Hz. Therefore, the calculation of angle theta was accomplished successfully.

#### 6.1.4 Parke Transformation result

To implement the Parke transformation as presented in equation (C.2-20) in C code language, some tricks had to be done. This was because, not all element of equation (C.2-20) were available to calculate  $V_d$  and  $V_q$ . There was no math function in the DSP library to calculate the cosine of the angle for this project. However, there was a look up table for the sinusoidal function. The look up table had the following range: the x-values ranged from zero to 1024 and the y-values from -1024 to 1024 [18].

Moreover, to implement the cosine of the angle, the angle  $\theta$  was shifted by  $90^\circ$ . Using equation (6.1.4-1), which represented the relation between the angles in degree to the numbers inside the computer, thus  $90^\circ$  was equivalent to 256 counts.

$$\frac{angle[Count]}{1024} = \frac{angle[degree]}{360^\circ} \quad (6.1.4-1)$$

Therefore equation (6.1.4-2) was obtained, which shows how the angle  $\theta$  was shifted by  $90^\circ$  degree in the code.

$$\theta_{\text{acos1}} = \theta + 256; \quad (6.1.4-2)$$

The  $\theta$  values were ranging from 0 to 1023 in arctan function as presented appendix J. Thus, by adding 256 into angle  $\theta$ , the new  $\theta$  was in the range of 256 and 1279. Moreover, the maximum value of the new  $\theta$  angle was higher than the maximum value of the x-value of the sinusoidal look up table function, which practically would produce a distorted cosine waveform. Thus, it was important to scale the new  $\theta$  angle to be in the range of 0 to 1023.

The piece of code below did the trick:

$$\text{if}(\theta_{\text{acos1}} > 1023) \theta_{\text{acos1}} = \theta_{\text{acos1}} - 1023;$$

From the above piece of code, it can be seen that whenever the new angle was above 1023, 1023 was subtracted from it, which resulted the new angle  $\theta$  being in the range of 0 to 1023.

Thus the sine of  $\theta$  and the sine of the new  $\theta$ ,  $\theta_{\text{acos1}}$ , which is equal to cosine of  $\theta$ , were calculated in the C code as shown in equations (6.1.4-3) and (6.1.4-4)

$$\sin\theta_{\text{eta1}} = \text{sine}(\theta); \quad (6.1.4-3)$$

$$\cos\theta_{\text{eta1}} = \text{sine}(\theta_{\text{acos1}}); \quad (6.1.4-4)$$

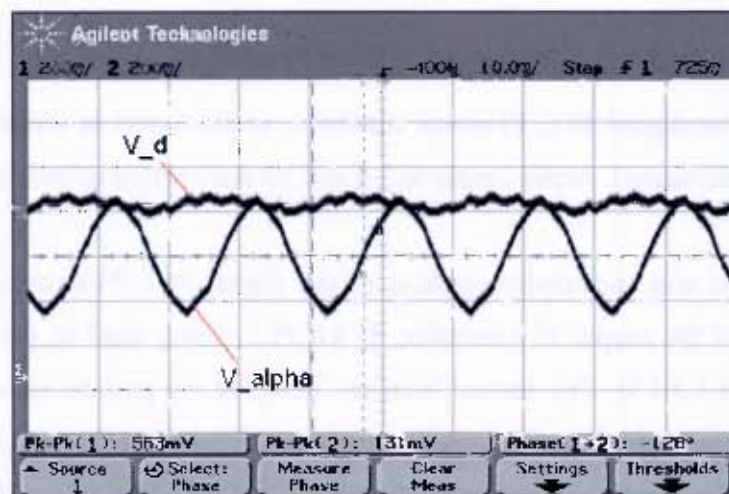
The  $\sin\theta_{\text{eta1}}$  and  $\cos\theta_{\text{eta1}}$  are the sine and the cosine of the three-phase grid angle. There were defined once at this point in the code to prevent using the sinusoidal look up table several times in the code, which consequently would deteriorate the speed performance of running the code.

Equations 6.1.4-5 and 6.1.4-6, presents how Park transformation was implemented in C code.

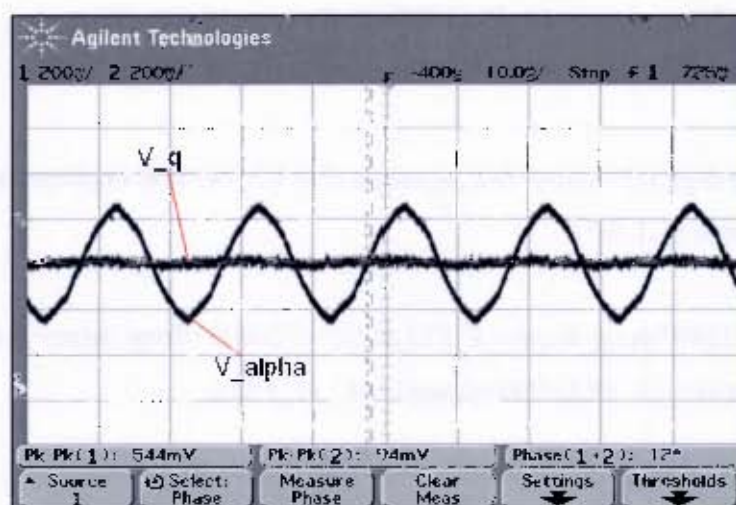
$$V_d\_grid = (V_{\alpha} * (\text{long int}) \cos \theta) / 1024 + (V_{\beta} * (\text{long int}) \sin \theta) / 1024; \quad (6.1.4-5)$$

$$V_q\_grid = -(V_{\alpha} * (\text{long int}) \sin \theta) / 1024 + (V_{\beta} * (\text{long int}) \cos \theta) / 1024; \quad (6.1.4-6)$$

Oscilloscope Results 6.1.4-1 and 6.1.4-2, presents the Park Transformation results. The rotating reference plane signals,  $V_d$  and  $V_q$ , are shown in relation with stationary reference plane signal,  $V_{\alpha}$ .



Oscilloscope Result 6.1.4-1: Result of the three-phase grid  $V_{\alpha}$  and  $V_d$



Oscilloscope Result 6.1.4-2: Result of the three-phase grid  $V_{\alpha}$  and  $V_q$

From Oscilloscope\_Results 6.1.4-1 and 6.1.4-2, it was visible that the Parke Transformation was implemented successfully. As discussed in appendix C, it transformed the voltage signals,  $V_\alpha$  and  $V_\beta$  from stationary reference plane to rotating reference plane, whereby  $V_d$  and  $V_q$  look like a DC signals.

However  $V_d$  in figure 6.1.4-1 does not look as perfect DC signal because  $V_\alpha$  and  $V_\beta$  did not have the same amplitude, refer to Oscilloscope\_Result 6.1.2-1. The inverse Park Transformation was also implemented in the code just by changing the signs of equation (6.1.4-5) and (6.1.4-6) as discussed in appendix C section C.2, equation (C.2-22).

### 6.1.5 Phase Locked Loop controller result

In this section, the digital PLL PI-based controller as discussed in sections 3.4.1.3 and 3.4.1.4 were implemented. Alpha equals to 2.4 and 30 were tested in two scenarios.

The first scenario was the implementation of the digital PLL PI-based controller with previous value of the output PI controller,  $U_{kl\_PLL}$ , being used in the integral plant, see equation (3.4.1.3-15). The second scenario however the present value,  $U_{PLL}$  was used instead, see equation (3.4.1.4-8). Equation (3.4.1.3-15) or (3.4.1.4-8) was implemented in C coding as shown in equations (6.1.5-1) and (6.1.5-2) respectively.

$$Y_{PLL} = (int)((66 * (long int)U_{kl\_PLL}) / 32768 + (long int)Y_{kl\_PLL}); \quad (6.1.5-1)$$

$$Y_{PLL} = (int)((66 * (long int)U_{PLL}) / 32768 - (long int)Y_{kl\_PLL}); \quad (6.1.5-2)$$

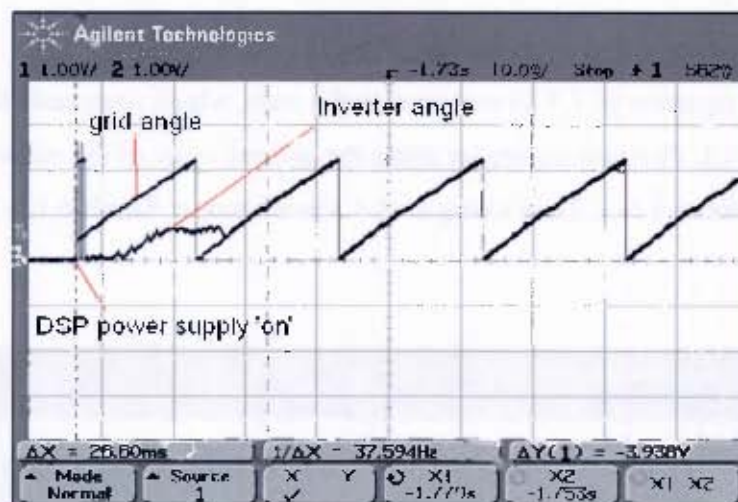
Furthermore, the digital PI controller, equation (3.4.1.3-14) was implemented in C coding as show in equation (6.1.5-3).

$$U_{PLL} = (int)((23580 * (long int)err_k\_PLL) / 256 \vee (524003 * (long int)err_{kl\_PLL}) / 32768 - (23580 * (long int)err_{kl\_PLL}) / 256 \vee (long int)U_{kl\_PLL}); \quad (6.1.5-3)$$

Where the ratio  $23580/256$  is equal to  $92.11$ , this is the proportional gain,  $K_{p\_pll}$ , note that the denominator is  $2^8$ , which mean that the  $K_{p\_pll}$  was multiplied by Q-format of Q8. The ratio  $524003/32768$  is equal to  $15.99$ , this value is the product of the integral gain,  $K_{i\_pll}$ , and the sample time  $T_s=100\mu s$ . The gain values of equation (6.1.5-3) were implemented for  $\alpha=2.4$ , refer to table 3.4.1.2-1 in section 3.4.1.2.

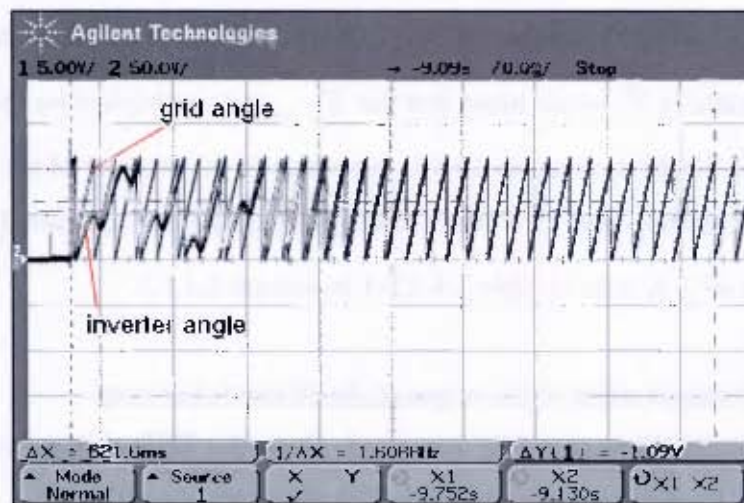
*b) Scenario 1: Previous value of the output of the PI controller used*

Thus for  $\alpha=2.4$ , equations (6.1.5-3) was used. Once the DSP chip power supply was switched on,  $\gamma$  tracked  $\theta$  with a delay. Oscilloscope Result 6.1.5-1 confirms the discussion.



Oscilloscope\_Result 6.1.5-1: Result of the  $\gamma$  synchronizing with  $\theta$ , using  $\alpha=2.4$  and the previous value of the output of the PI controller

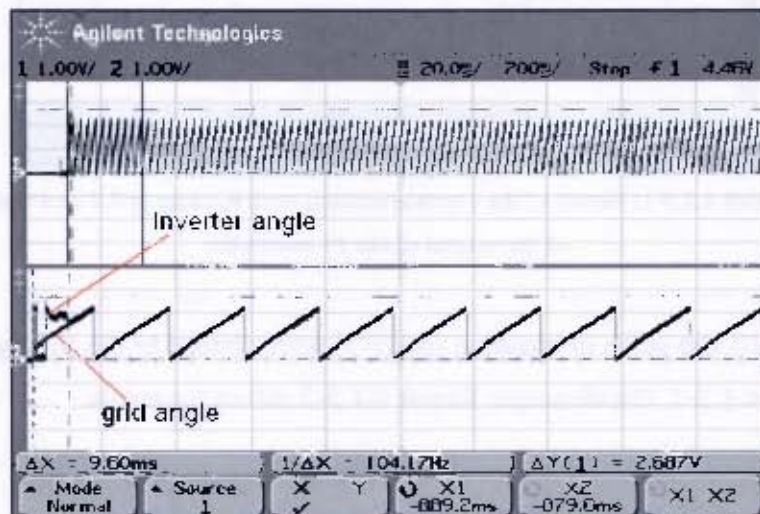
Using now  $\alpha=3\theta$ , the gains of equation (6.1.5-3) were change to the right gains of  $\alpha=3\theta$ , refer to table 3.4.1.2-1. Oscilloscope\_Result 6.1.5-2 shows the result.



Oscilloscope\_Result 6.1.5-2: Result of the  $\gamma$  synchronizing with  $\theta$ , using  $\alpha=30$  and the previous value of the output of the PI controller

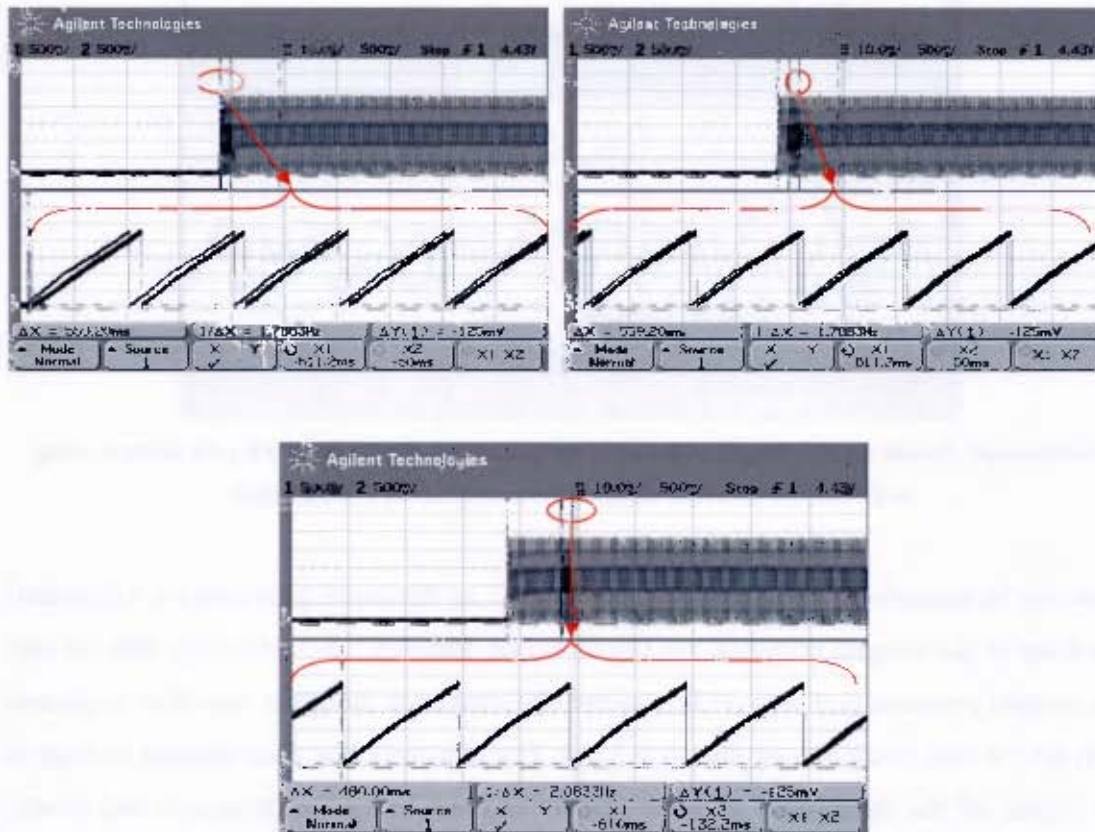
*b) Scenario 2: Present value of the output of the PI controller used*

In this scenario, equation (6.1.5-2) was used in the code, which represents the integral function of the PLL PI-based controller using the present value of the output of the PI controller, equation 6.1.5-3. Thus Using  $\alpha=2.4$ , Oscilloscope\_Result 6.1.5-3 shows the result.



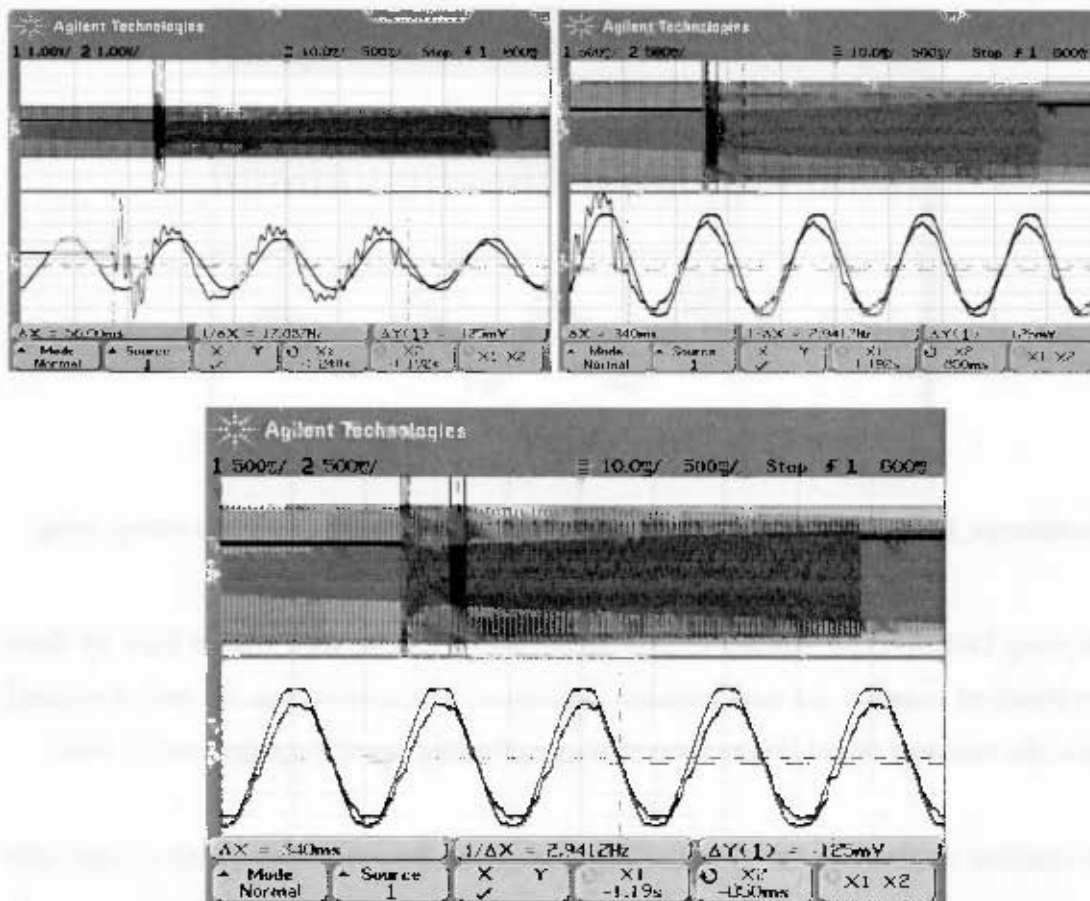
Oscilloscope\_Result 6.1.5-3: Result of the  $\gamma$  synchronizing with  $\theta$ , using  $\alpha=2.4$  and the present value of the output of the PI controller

Using  $\alpha=30$ , Oscilloscope\_Result 6.1.5-4 shows the result



Oscilloscope\_Result 6.1.5-4: Result of the  $\gamma$  synchronizing with  $\theta$ , using  $\alpha=30$  and the present value of the output of the PI controller.

Analyzing the two scenarios, when the previous value is used, scenario 1, it can be seen that it introduced a delay on the integral response as discussed previously, but also that delay when  $\alpha=30$  was used, it distorted the  $\gamma$  on the start up, refer to Oscilloscope\_Result 6.1.5-2. Consequently, the distorted  $\gamma$  when used produced a distorted fundamental inverter voltage initially with frequency higher than the fundamental frequency, 50Hz. Oscilloscope\_Result 6.1.5-5 shows this.



Oscilloscope\_Result 6.1.5-6: Result of the inverter voltage synchronizing with grid voltage, using  $\alpha=30$  and the present value of the output of the PI controller.

Oscilloscope\_Result 6.1.5-7 shows the three-phase inverter fundamental voltage for scenario 2 for  $\alpha=2.4$ . It shows how quickly the inverter voltage tracks the grid voltage.

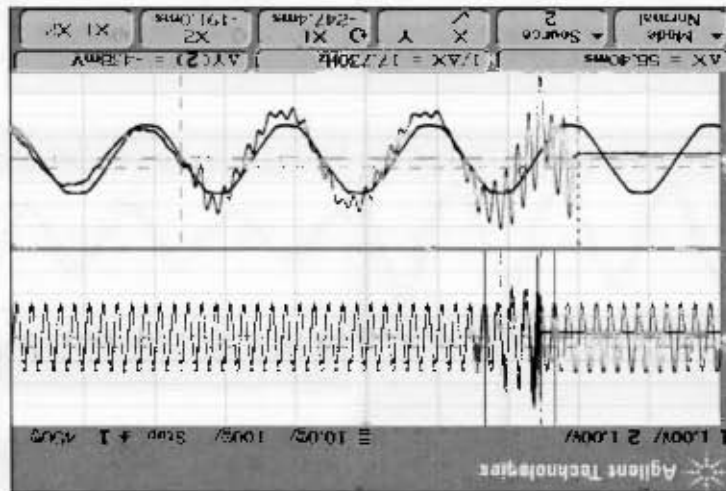
After the transient state, i.e. at steady state, it can be seen that the three-phase inverter voltage magnitude was smaller than the three-phase grid magnitude voltage. As discussed

The disadvantage of increasing the filter inductor small resistor is that, it will introduce phase angle between the LC filter output voltage and the input voltage as discussed before. Nevertheless, from Oscilloscope Result 6.1.5-7, it can be seen that the three-phase fundamental voltage was lagging the grid voltage.

The transient response in the output of the three-phase inverter fundamental voltage was because of the uncontrollable inrush current through the inductor of the LC filter towards the capacitor at start up. The transient response can be improved by increasing the damping factor. This can be done by either increasing the inductor resistor or using a minor loop current controller to control the inductor current toward zero as discussed previously in simulation chapter.

Analyzing Oscilloscope Results 6.1.5-5 to 6.1.5-7, it can be seen that at start up there were transient response for each scenario. Moreover, it was noted that for each discussed figure, the transient lasted for the same time roughly 5ms until it reached steady state.

Oscilloscope Result 6.1.5-7: Result of the inverter voltage synchronizing with grid voltage, using  $\alpha=2.4$  and the present value of the PI controller.

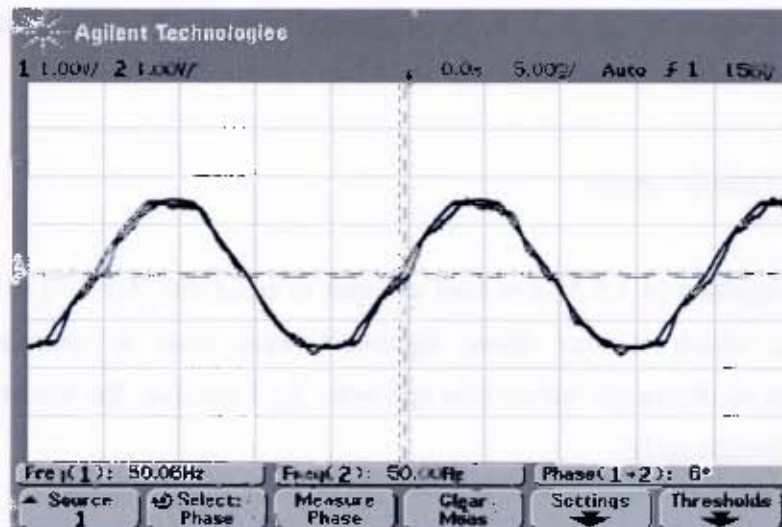


previously that was caused by the modulation index been set to full modulation of 1 by using equations (4.9.2-3) to (4.9.2-5), such that over modulation could be avoided.

Therefore the DC bus should be increased to prevent the over modulation to occur and hence preventing the decreasing of the fundamental voltage.

Now to be able to connect the three-phase inverter with the three-phase grid such that no current either real or reactive should flow, the three-phase inverter voltage has to be equal in phase and magnitude with the three-phase grid voltage. However, that was not the case in Oscilloscope\_Result 6.1.5-7.

Thus, as discussed, the two potentiometers, which control the real power or the  $\delta$  and reactive power or magnitude, were used to adjust the inverter voltage angle and magnitude to match as close as possible to the three-phase grid voltage. Oscilloscope Result 6.1.5-8 shows this.



Oscilloscope Result 6.1.5-8: Result of the inverter voltage synchronizing with grid voltage, using  $\alpha=2.4$  and the present value of the output of the PI controller.

To understand better how the manual control was done, recall from section 5.2.2, it was discussed that the potentiometers voltage were from 0 to 3.3V, where in digital form, goes from 0 to 1024.

$$ma = pot1; \quad (6.1.5-5)$$

Where,  $ma$  was defined as the modulation index in the code and ranging from 0 to 1024 counts. The rotating reference voltages, equations (6.1.4-5) and (6.1.4-6) were transformed back to stationary reference plane by using the inverse Park Transformation see appendix J.

In the code, those stationary sinusoidal orthogonal signals had a maximum peak magnitude of 512 counts. Moreover, they were used as input to the SPWM algorithm. In addition, to be able to control the voltage magnitude such that would go above or below 512 counts, the variable  $ma$  was multiplied to it, and then the product was divided by 512. Equations (6.1.5-6) and (6.1.5-7) shows this

$$VdRef = (ma * vd\_inv) / 512; \quad (6.1.5-6)$$

$$VqRef = (ma * vq\_inv) / 512; \quad (6.1.5-7)$$

Furthermore,  $ma$  was limited not to rise above 804 counts using the piece of code below

$$\text{If } (ma > 804) \text{ } ma = 804;$$

Thus, the values of modulation index was from 0 to 1.57, where  $804/512=1.57$ .

Therefore, the inverter voltage magnitude was controlled bi-directionally.

## 6.2 Financial look in the project

In this section, a financial cost analysis will be done for the 100kVA three-phase inverter battery system only as it was the one with less battery capacity as discussed in section 2.4.4.

The cost of the battery for the 100kVA three-phase inverter battery system will be done in section 6.2.1. Section 6.2.2 will discuss the battery maintenance cost. Section 6.2.3 will look into the battery recovery cost.

Furthermore, section 6.2.4 will discuss the total capital cost to have the system up and running. Section 6.2.5 will present all the yearly saving incurred by 100kVA battery system during the lifetime of the battery system.

Finally, a net-present value and break-even analysis will be done in section 6.2.6 to investigate if the 100kVA three-phase inverter battery system savings would payoff the initial capital cost, before the life time of the battery system, which is the part of the 100kVA three-phase inverter battery system that has the shortest life time.

### **6.2.1 Battery Cost**

The rating of the 100kVA three-phase inverter battery system as calculated in section 2.4.4 was 1603.25Ah/5.5hr/1.8V per cell /25° C. Recalling from section 2.4.2 that the chosen FNB battery was the Raylite Tubular RCT. The Raylite Tubular RCT has different types of cell range for different capacities i.e. maximum current discharged at minimum voltage and different period; see the table of standby power-Raylite Tubular RCT constant current discharge in appendix B.

From section 2.4.4, the maximum average current that the battery would supply for the 100kVA three-phase inverter was calculated to be 291.5A for 5.5hour. Using the constant current discharge data in appendix B, the chosen tubular cell was the 14RCT1750. From the appendix B, it can be seen that the 14RCT1750 is able to deliver the average current for 5.5hour with a minimum voltage of 1.8V.

Moreover, the meeting held with Cliff Hardman and Mervin Barry, the sales engineer of the First National Battery (FNB) South Africa Company, it was discussed that the 14RCT1750 cell at 1.8V for 5.5hr, has capacity of 1595Ah, which is close enough to the

calculated one. Furthermore, the cost per cell for this battery is R6,000.00 thus for the 200 cells the total cost was R1,200,000.00. This is 2007 price as given by Barry.

### **6.2.2 Battery maintenance cost**

Mervin Barry said that the Raylite Tubular RCT batteries would need 3 times maintenances in a year. The maintenance cost is made of the following steps: traveling fees, checking of each cells voltage, water topping and labors hour, which in a year adds up to 15 hour. The labors work is subdivided into the following task: skill report writing and skilled technical labor.

In addition, it was added by Barry that, currently the cost of maintenance of 55 cell battery is R350 per visit. Thus the maintenance per cell in one visit is R6.36/cell, which for 200 cells it would be R1,272.73. Therefore, the yearly maintenance would be R3,818.18. The yearly maintenance cost was assumed constant throughout the lifetime of the battery for simplicity.

### **6.2.3 Raylite Tubular cell battery scrap recovery value**

The scrap recovery value is the value that the battery would be worth after its lifetime. To calculate the scrap recovery value the following was done: Using the RAYLITE tubular cells datasheet in appendix B, more specifically in the tubular capacities, weights and dimensions section, the weight of a cell completed filled of the 14RCT1750 tubular cell type is 144.1kg.

The Rand/kg rate as discussed with the sale engineer of FNB is R1.70/kg. Therefore, the scrap recovery value per cell in Rand would be R244.97, which for 200 cells it would be R48,994.00.

### 6.2.4 Total capital cost

The capital cost to have the 100kVA three-phase inverter battery system installed at UCTMS on the 11kV bus bar, see figure 2.1-1, was estimated with help of Peter Burden, a general manager (sales and production) of MLT Drives.

The main components of the system are listed below:

- 100kVA three-phase inverter.
- 100kVA line to line 380/11kV rms  $\Delta$ -Y three-phase transformer
- Battery system

From the interview with Burden, the cost of 100kVA three-phase inverter, the cabling system cost, the cost of installing the full system and the transportation cost were given as shown in table 6.2.4-1.

**Table 6.2.4-1: Some system item cost**

Items	Cost
100kVA three-phase inverter	R100,000.00
Installation	R20,000.00
Cabling	R3,000.00
Transportation	R15,000.00

From section 1.2.4 the costs of UCTMS three-phase transformer were discussed, the rate per kVA was given as R150/kVA. Thus using the same ratio, the 100kVA three-phase transformer for this project would cost R15,000.00. Furthermore, from section 6.2.1, the battery system cost was calculated to be R1,200,000.00.

Therefore, adding all the above discussed costs, the Initial capital cost or cash outflow of the system would be R1,353,000.00.

### **6.2.5 Yearly savings calculation**

Recalling from section 2.3.2, the yearly saving for the 100kVA three-phase inverter in 2004 was calculated to be R23,016.00. From table 2.3-1 the percentage rate of increase of UCTMS annual demand charge was 3.51%. The demand charge rate of increase was assumed the same throughout the lifetime of the batteries storage. The battery storage lifetime as discussed in section 2.4.2.1 was 12 years.

Furthermore, assuming the project was started in 2004, the first yearly saving or cash inflow of the project would be at end of 2004. The rest of the yearly cash inflow was calculated using equation (6.2.5-1). Moreover, recalling from table 2.3-1 in section 2.3, that the demand charge in 2004 was R19.18, then the future demand charge were also calculated using equation (6.2.5-1)

$$FV = PV(1+r)^n \quad (6.2.5-1)$$

Where  $r$  is the percentage rate of increase of demand charge,  $n$  is the number of year,  $FV$  is future value and  $PV$  defined as the present value. Table 6.2.5-1 shows the result of the FV yearly savings that the project would have and its respective demand charges.

**Table 6.2.5-1: Project yearly saving and demand charge for the period of 12 years**

Year	Yearly saving [R]	Demand Charge [R]	n	r (Increase ) [%]
2004	R 23,016.00	R 19.18	1	3.51
2005	R 23,823.86	R 19.85	2	
2006	R 24,660.08	R 20.55	3	
2007	R 25,525.65	R 21.27	4	
2008	R 26,421.60	R 22.02	5	
2009	R 27,349.00	R 22.79	6	
2010	R 28,308.95	R 23.59	7	
2011	R 29,302.59	R 24.42	8	
2012	R 30,331.11	R 25.28	9	
2013	R 31,395.73	R 26.16	10	
2014	R 32,497.72	R 27.08	11	
2015	R 33,638.39	R 28.03	12	

The PV value in equation (6.2.5-1) to calculate the FV of yearly saving and demand charge from 2005 to 2015 were set to 2004 values, R23,016.00 and R19.18 respectively.

### **6.2.6 Net present value and break-even analysis**

The Net Present Value (NPV) is “*the difference between the present value of cash inflows and the present value of cash outflows*” [45]. For the project to be financial viable, NPV must be greater or equal to zero. In addition after the break-even point, the savings must be enough to self-sustain the installed system for any system part replacement and maintenance.

The yearly saving calculated as illustrated in table 6.2.5-1 must be used in each respective year to pay for the battery maintenance cost or any system expense, which for this project for simplicity the only expense or cash outflow was assumed to be the battery maintenance cost, R3,818.18.

The recovery value of battery, which was calculated to be R48,994.00, would be added in the last year cash inflow. Therefore the overall future cash inflow for each respective year, taking in consideration the battery maintenance cost and battery recovery value as discussed above, would be as presented in table 6.2.6-1.

**Table 6.2.6-1: Project cash inflow for the period of 12 years**

Year	Cash inflow ( $C_n$ ) [R]	N
2004	R 19,197.82	1
2005	R 20,005.68	2
2006	R 20,841.90	3
2007	R 21,707.47	4
2008	R 22,603.42	5
2009	R 23,530.82	6
2010	R 24,490.77	7
2011	R 25,484.41	8
2012	R 26,512.93	9
2013	R 27,577.55	10
2014	R 28,679.54	11
2015	R 78,814.21	12

As mentioned above the NPV is defined as shown in equation (6.2.6-1)

$$NPV = C_i - C_o \quad (6.2.6-1)$$

Where  $C_i$  is defined as “the present value of cash inflows” [45], and  $C_o$  is “the present value of cash outflows” [45].

The lump sum of the present value cash inflows for table 6.2.6-1 was calculated using equation (6.2.6-2), at discount rate,  $r$ , of 10%.

$$C_i = \sum_{n=1}^{12} \frac{C_n}{(1+r)^n} \quad (6.2.6-2)$$

$$= R173,286.34$$

Where,  $C_n$  is the cash inflow for each respective year and  $n$  as discussed before is the number of year.

$C_o$  was set to the initial capital cost, R1,353,000.00, which is the present value cash outflow of the project.

Thus, using equation (6.2.6-2) with value of  $C_i$  and  $C_o$  as discussed above, the result of NPV is presented below.

$$\begin{aligned} NPV &= R173,286.34 - R1,353,000.00 \\ &= -R1,179,713.66 \end{aligned} \quad (6.2.6-3)$$

The NPV attained a negative result, therefore it can be conclude that the project would not be financial viable at this present condition of demand charge and percentage rate of demand charge, which means that at the end of the battery life time the initial capital cost would not be fully paid off. However, a question could be asked such as, what changes should be done or happen to make the project financial viable in future?

To answer this question, two scenarios can be investigated such as the project internal changes and external changes. The internal changes are changes that can be controllable by investor of the project, for instance, decreasing the initial capital cost by looking for alternative and cheaper components to install the 100kVA three-phase inverter battery system.

The external changes are changes that cannot be controllable by the project, however, it influences the turn over of the project. For instance, the change on the demand charge tariff and the percentage rate increase of the demand charge are controlled by the National Electricity Regulator (NER) in South Africa [46].

#### Scenario 1: Project internal change

If the initial capital cost is considered to be decreased by looking for alternative and cheaper way to install the system as discussed before. However, the present value cash

inflow due to the installation of 100kVA three-phase battery system was calculated to be R173,286.34.

Moreover, NPV to be greater or equal to zero, the initial capital cost would have to be decreased at least by 87.2%, which realistically it is impossible. Because it would mean that the battery and the three-phase inverter cost for example would have to be decreased from R1,200,000.00 and R100,000.00 to R153,600.00 and R12,800.00 respectively. At this new price, the battery and the three-phase inverter would not be the same one with same capacity in Ah and kVA respectively. Therefore, scenario1 would not be the right option.

#### Scenario 2: Project external changes

a) In this part of scenario 2, the change is only done in the percentage rate increase of demand charge, such that it would be increased by 48.24% while keeping the initial capital cost and demand charge the same. Increasing  $r$  to 51.75% would ensure that NPV be positive and with enough return to buy new sets of battery after its lifetime. Table 6.2.6-2 shows the changes that happen by setting  $r=51.75\%$ .

**Table 6.2.6-2: Scenario2 percentage rate increased of demand charge**

Year	Yearly saving [Rand]	Cash inflow [Rand]	Demand Charge [Rand]	n	r (Increase ) [%]
2004	23,016.00	17,452.56	19.18	1	51.75
2005	34,926.78	25,706.59	29.11	2	
2006	53,001.39	36,952.07	44.17	3	
2007	80,429.61	52,326.64	67.02	4	
2008	122,051.93	73,413.86	101.71	5	
2009	185,213.80	102,393.10	154.34	6	
2010	281,061.95	142,269.89	234.22	7	
2011	426,511.50	197,189.55	355.43	8	
2012	647,231.20	272,869.93	539.36	9	
2013	982,173.35	377,198.27	818.48	10	
2014	1,490,448.06	521,054.70	1,242.04	11	
2015	2,261,754.93	735,059.23	1,884.80	12	

The lump-sum of the  $C_I = R2,553,889.40$ , thus the result of NPV is shown in (6.2.6-5)

$$\begin{aligned} NPV &= R2,553,889.40 - R1,353,000.00 \\ &= R1,200,889.40 \end{aligned} \quad (6.2.6-5)$$

However, in practice this increase would be impracticable because at the end of the battery lifetime, every consumer, which uses the same tariff structure as UCTMS, their demand charge would jump from R19.18 to R1,884.80 for 48.24% increase. Therefore scenario 2 (a) would not be the right one.

b) The change is done now in the demand charge, while keeping the initial capital cost and the percentage rate increase of demand charge the same. For the project to be self sustained in its first year of installation ( $NPV > 0$ ) in such way that at end of the battery life time, it could pay off the initial capital cost and at same time buy its new set of battery, then the demand charge would have to be started at R269.00. Table 6.2.6-3 shows the changes that happen by setting the demand charge to R269.00. However, the project would just be viable ( $NPV = 0$ ) if the demand would have to be started at R142.36.

**Table 6.2.6-3: Scenario2 increase in demand charge only**

Year	Yearly saving [Rand]	Cash inflow [Rand]	Demand Charge [Rand]	n	r (Increase) [%]
2004	322,800.00	289,983.47	269.00	1	3.51
2005	334,130.28	272,985.21	278.44	2	
2006	345,858.25	256,979.77	288.22	3	
2007	357,997.88	241,909.50	298.33	4	
2008	370,563.60	227,720.05	308.80	5	
2009	383,570.39	214,360.22	319.64	6	
2010	397,033.71	201,781.74	330.86	7	
2011	410,969.59	189,939.14	342.47	8	
2012	425,394.62	178,789.56	354.50	9	
2013	440,325.97	168,292.65	366.94	10	
2014	455,781.41	158,410.36	379.82	11	
2015	471,779.34	164,717.85	393.15	12	

The lump-sum of the  $C_i=R2,565,869.52$ , so the result of NPV for this scenario is presented in (6.2.6-6)

$$\begin{aligned} NPV &= R2,565,869.52 - R1,353,000.00 \\ &= R1,212,869.52 \end{aligned} \tag{6.2.6-6}$$

In this scenario, the demand charge would increase from R269 in 2004 to R393.15 by 2015, which compared with line (a) it gives a better results and more realistic one. Therefore scenario 2 (b) would be the right choice that would make the project financial viable.

Appendix K shows the break-even results of the scenario 2 (b). It can be seen that at this scenario the project would pay the initial capital cost between the year 5 and 6.

From the above discussion, the project would be financially viable if by the time the project is started, the electricity pricing would reflect scenario 2 (b). Furthermore, in reality, both demand charge and the percentage rate increase of demand charge are increasing due to economic regulation [47], construction of new power utility [48].

### 6.3 Chapter Summary

From the above discussion, the following points are summarized:

- The Clarke Transformation algorithm using  $\sqrt{\frac{2}{3}}$  as coefficient was successfully implemented.
- The three-phase grid phase angle,  $\theta$  was successfully calculated using the arctan2 function algorithm. The algorithm had as input the results of the Clarke Transformation,  $V_\alpha$  and  $V_\beta$ .
- The digital PLL PI-based controller algorithm was successfully implemented in practice. The new produced phase (three-phase inverter phase) tracked the three-phase grid phase. This was a very important result because it helped to transform the orthogonal stationary signals of the three-phase inverter into the rotating reference plane using Park Transformation, and then back to the stationary

reference plane using inverse Park Transformation as presented in simulation as well as in practice.

- It was shown practically that by using the present value,  $U_{PLL}$ , of the output of the PI controller of PLL PI-based controller in the integrator function eliminates the delay that would be introduced by the previous value,  $U_{k1\_PLL}$ , if is used instead.
- The Park Transformation and inverse Park Transformation developed algorithm was successfully implemented in the DSP chip. This result is a very crucial step to implement practically the minor loop current controller as presented in simulation chapter.
- The NPV and Break-Even analysis showed that external change or the dynamic change in the electricity market plays a big role in determine the financial viability of the project.

## **7 Conclusion**

Recalling that the hypothesis for this research was that, using a lead-acid battery and three-phase inverter for PLS of the electricity supply at the UCTMS is technically and financially viable.

From the result of the research done, it is concluded that the project is technically and financially viable.

The technical viability was shown by simulating UCTMS load profile in simplorer simulator, where two dailies MD were demonstrated being shaved towards a set threshold. As well as implementing practically the digital PLL PI-based controller in lab.

The financial viability however, would depend on status of the electricity market at the time the project would be commissioned, which would make it possible to be implemented.

## **8 Recommendation**

Based on the results and conclusions of this research the following recommendations are suggested:

- Develop a multi-stage charging of lead-acid battery algorithm as discussed in section 2.4.3 to be implemented with PLS algorithm.
- Use the continuous minor loop current controller to derive the digital version so that it can be implemented in the DSP chip.
- Use a DSP chip with more ADC input to sense more signals to implement the PLS in practice successfully.

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## **Appendices**

- A. UCTMS tables results for the load profile analysis
- B. Raylite Tubular RCT datasheet
- C. Clarke and Park Transformation Analysis
- D. PLL equation derivation
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- F. Three-phase transformer, No-Load and shorted circuit test
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# APPENDIX A

## A UCTMS tables results for the load profile analysis

**Table A-1: UCT Medical school MD data recorded from Electricity bills and actual data**

	UCT Medical School MD data recorded from Electricity bills	UCT Medical School actual MD data recorded from the meters
Nov 04	1950	1951.20
Dec 04	1839	1839.60
Jan 05	2046	2046.00
Feb 05	2070	2070.90
Mar 05	2127	2129.10
Apr 05	1977	1978.80
May 05	1818	1818.00
June 05	1953	1953.00

**Table A-2: UCT Medical school Ideal Threshold Line for each Month for 100kVA three-phase inverter**

	UCT Medical School actual MD data recorded from the meters	UCT Medical school Ideal Threshold Line for each Month for 100kVA three-phase inverter	UCT Medical school ideal threshold Line for each Month for 200kVA three-phase inverter
Nov 04	1951.20	1851.20	1751.20
Dec 04	1839.60	1739.60	1639.60
Jan 05	2046.00	1946.00	1846.00
Feb 05	2070.90	1970.90	1870.90
Mar 05	2129.10	2029.10	1929.10
Apr 05	1978.80	1878.80	1778.80
May 05	1818.00	1718.00	1618.00
June 05	1953.00	1853.00	1753.00

**Table A-3: Inverter capacity used for the 100kVA three-phase inverter on 3<sup>rd</sup> of December**

Day of the Week	Time [hour]	MD [kVA]	Threshold Line [kVA]	New MD [kVA]	Inverter Capacity [kVA]
Friday	03.12.2004 10:30:00	1,707.90	1739.60	1,707.90	0.0
Friday	03.12.2004 11:00:00	1,755.60	1739.60	1,739.60	16.0
Friday	03.12.2004 11:30:00	1,839.60	1739.60	1,739.60	100.0
Friday	03.12.2004 12:00:00	1,831.20	1739.60	1,739.60	91.6
Friday	03.12.2004 12:30:00	1,800.30	1739.60	1,739.60	60.7
Friday	03.12.2004 13:00:00	1,788.90	1739.60	1,739.60	49.3
Friday	03.12.2004 13:30:00	1,780.20	1739.60	1,739.60	40.6
Friday	03.12.2004 14:00:00	1,770.90	1739.60	1,739.60	31.3
Friday	03.12.2004 14:30:00	1,802.70	1739.60	1,739.60	63.1
Friday	03.12.2004 15:00:00	1,744.80	1739.60	1,739.60	5.2
Friday	03.12.2004 15:30:00	1,768.20	1739.60	1,739.60	28.6
Friday	03.12.2004 16:00:00	1,735.50	1739.60	1,735.50	0.0

**Table A-4: Inverter capacity used for the 200kVA three-phase inverter on 3<sup>rd</sup> of December**

Day of the week	Time [hour]	MD [kVA]	Threshold Line [kVA]	New MD [kVA]	Inverter Capacity [kVA]
Friday	03.12.2004 09:00:00	1,601.70	1,639.60	1,601.70	0.0
Friday	03.12.2004 09:30:00	1,642.80	1,639.60	1,639.60	3.2
Friday	03.12.2004 10:00:00	1,682.70	1,639.60	1,639.60	43.1
Friday	03.12.2004 10:30:00	1,707.90	1,639.60	1,639.60	68.3
Friday	03.12.2004 11:00:00	1,755.60	1,639.60	1,639.60	116.0
Friday	03.12.2004 11:30:00	1,839.60	1,639.60	1,639.60	200.0
Friday	03.12.2004 12:00:00	1,831.20	1,639.60	1,639.60	191.6
Friday	03.12.2004 12:30:00	1,800.30	1,639.60	1,639.60	160.7
Friday	03.12.2004 13:00:00	1,788.90	1,639.60	1,639.60	149.3
Friday	03.12.2004 13:30:00	1,780.20	1,639.60	1,639.60	140.6
Friday	03.12.2004 14:00:00	1,770.90	1,639.60	1,639.60	131.3
Friday	03.12.2004 14:30:00	1,802.70	1,639.60	1,639.60	163.1
Friday	03.12.2004 15:00:00	1,744.80	1,639.60	1,639.60	105.2
Friday	03.12.2004 15:30:00	1,768.20	1,639.60	1,639.60	128.6
Friday	03.12.2004 16:00:00	1,735.50	1,639.60	1,639.60	95.9
Friday	03.12.2004 16:30:00	1,647.90	1,639.60	1,639.60	8.3
Friday	03.12.2004 17:00:00	1,587.30	1,639.60	1,587.30	0.0

**Table A-5: 100kVA Three-phase inverter at different PF**

Time [hour]	Inverter Capacity [kVA]	PF	Real Power [kW]	Reactive Power [kVar]	Duration [hour]
03.12.2004 11:00:00	16.0	0.86	13.77	8.14	5
03.12.2004 11:30:00	100.0	0.87	86.79	49.67	
03.12.2004 12:00:00	91.6	0.87	79.74	45.07	
03.12.2004 12:30:00	60.7	0.87	52.62	30.26	
03.12.2004 13:00:00	49.3	0.86	42.24	25.42	
03.12.2004 13:30:00	40.6	0.86	35.11	20.39	
03.12.2004 14:00:00	31.3	0.86	26.85	16.08	
03.12.2004 14:30:00	63.1	0.85	53.65	33.22	
03.12.2004 15:00:00	5.2	0.85	4.43	2.72	
03.12.2004 15:30:00	28.6	0.85	24.42	14.89	

**Table A-6: 200kVA Three-phase inverter at different PF**

Time [hour]	Inverter Capacity [kVA]	PF	Real Power [kW]	Reactive Power [kVar]	Duration [hour]
03.12.2004 09:30:00	3.2	0.86	2.75	1.63	7.5
03.12.2004 10:00:00	43.1	0.86	37.15	21.85	
03.12.2004 10:30:00	68.3	0.86	58.91	34.57	
03.12.2004 11:00:00	116.0	0.86	99.84	59.05	
03.12.2004 11:30:00	200.0	0.87	173.58	99.35	
03.12.2004 12:00:00	191.6	0.87	166.80	94.27	
03.12.2004 12:30:00	160.7	0.87	139.30	80.12	
03.12.2004 13:00:00	149.3	0.86	127.92	76.99	
03.12.2004 13:30:00	140.6	0.86	121.57	70.63	
03.12.2004 14:00:00	131.3	0.86	112.64	67.47	
03.12.2004 14:30:00	163.1	0.85	138.67	85.86	
03.12.2004 15:00:00	105.2	0.85	89.66	55.02	
03.12.2004 15:30:00	128.6	0.85	109.79	66.96	
03.12.2004 16:00:00	95.9	0.85	81.44	50.63	
03.12.2004 16:30:00	8.3	0.85	7.05	4.37	

**Table A-7: Energy supplied by the 100kVA three-phase inverter for the 3<sup>rd</sup> day of December**

Time [hour]	Real Power [kW]	Energy [kWh]	Total Energy [kWh]
03.12.2004 11:00:00	13.77	6.89	209.81
03.12.2004 11:30:00	86.79	43.40	
03.12.2004 12:00:00	79.74	39.87	
03.12.2004 12:30:00	52.62	26.31	
03.12.2004 13:00:00	42.24	21.12	
03.12.2004 13:30:00	35.11	17.55	
03.12.2004 14:00:00	26.85	13.43	
03.12.2004 14:30:00	53.65	26.82	
03.12.2004 15:00:00	4.43	2.22	
03.12.2004 15:30:00	24.42	12.21	

**Table A-8: Energy supplied by the 200kVA three-phase inverter for the 3<sup>rd</sup> day of December**

Time [hour]	Real Power [kW]	Energy [kWh]	Total Energy [kWh]
03.12.2004 09:30:00	2.75	1.63	733.55
03.12.2004 10:00:00	37.15	21.85	
03.12.2004 10:30:00	58.91	34.57	
03.12.2004 11:00:00	99.84	59.05	
03.12.2004 11:30:00	173.58	99.35	
03.12.2004 12:00:00	166.80	94.27	
03.12.2004 12:30:00	139.30	80.12	
03.12.2004 13:00:00	127.92	76.99	
03.12.2004 13:30:00	121.57	70.63	
03.12.2004 14:00:00	112.64	67.47	
03.12.2004 14:30:00	138.67	85.86	
03.12.2004 15:00:00	89.66	55.02	
03.12.2004 15:30:00	109.79	66.96	
03.12.2004 16:00:00	81.44	50.63	
03.12.2004 16:30:00	7.05	4.37	

**Table A-9: Maximum energy in kWh supplied by 100kVA three-phase inverter**

	Nov 2004	Dec 2004	Jan 2005	Feb 2005	Mar 2005	Apr 2005	May 2005	Jun 2005
Energy [kWh]	226.70	209.81	157.87	361.16	95.77	126.06	228.23	170.55
Duration [hour]	5.5	5	4	5.5	2.5	3.5	5.5	4

**Table A-10: Maximum energy in kWh supplied by 200kVA three-phase inverter**

	Nov 2004	Dec 2004	Jan 2005	Feb 2005	Mar 2005	Apr 2005	May 2005	Jun 2005
Energy [kWh]	720.54	733.55	623.92	930.06	455.39	563.14	850.68	696.99
Duration [hour]	7	7.5	6.5	7.5	5.5	6.5	8	7.5

**Table A-11: Maximum energy supplied by the 100kVA three-phase inverter through the eight month period and its time duration**

Maximum Energy Supply [kWh]	Maximum duration time [hour]
361.16	5.5

**Table A-12: Maximum energy supplied by the 200kVA three-phase inverter through the eight month period and its time duration**

Maximum Energy Supply [kWh]	Maximum duration time [hour]
930.06	8

**Table A-13: Maximum daily Energy supplied by the 100kVA inverter at same PF as the source**

Time [hour]	Inverter Capacity [kVA]	PF	Inverter Capacity [kW]	Energy [kWh]	Total Energy [kWh]	Duration [hour]
16.02.2005 11:00:00	8.5	0.87	7.39	3.69	361.16	5.5
16.02.2005 11:30:00	27.1	0.87	23.65	11.82		
16.02.2005 12:00:00	77.8	0.87	67.95	33.97		
16.02.2005 12:30:00	87.1	0.87	75.70	37.85		
16.02.2005 13:00:00	100.0	0.87	87.03	43.52		
16.02.2005 13:30:00	92.5	0.87	80.42	40.21		
16.02.2005 14:00:00	99.4	0.87	86.18	43.09		
16.02.2005 14:30:00	91.9	0.87	79.63	39.82		
16.02.2005 15:00:00	94.9	0.87	82.58	41.29		
16.02.2005 15:30:00	82.0	0.87	71.12	35.56		
16.02.2005 16:00:00	70.0	0.87	60.67	30.33		

**Table A-14: Maximum daily Energy supplied by the 100kVA inverter at unity PF**

Time [hour]	Inverter Capacity [kVA]	PF	Inverter Capacity [kW]	Energy [kWh]	Total Energy [kWh]	Duration [hour]
16.02.2005 11:00:00	8.5	1	8.5	4.25	415.60	5.5
16.02.2005 11:30:00	27.1	1	27.1	13.55		
16.02.2005 12:00:00	77.8	1	77.8	38.90		
16.02.2005 12:30:00	87.1	1	87.1	43.55		
16.02.2005 13:00:00	100.0	1	100.0	50.00		
16.02.2005 13:30:00	92.5	1	92.5	46.25		
16.02.2005 14:00:00	99.4	1	99.4	49.70		
16.02.2005 14:30:00	91.9	1	91.9	45.95		
16.02.2005 15:00:00	94.9	1	94.9	47.45		
16.02.2005 15:30:00	82.0	1	82.0	41.00		
16.02.2005 16:00:00	70.0	1	70.0	35.00		

**Table A-15: Maximum daily Energy supplied by the 200kVA inverter at same PF as the source**

Time [hour]	Inverter Capacity [kVA]	PF	Inverter Capacity [kW]	Energy [kWh]	Total Energy [kWh]	Duration [hour]
16.02.2005 10:00:00	49.4	0.87	42.76	21.38	930.06	7.5
16.02.2005 10:30:00	72.5	0.87	63.14	31.57		
16.02.2005 11:00:00	108.5	0.87	94.29	47.15		
16.02.2005 11:30:00	127.1	0.87	110.92	55.46		
16.02.2005 12:00:00	177.8	0.87	155.28	77.64		
16.02.2005 12:30:00	187.1	0.87	162.61	81.30		
16.02.2005 13:00:00	200.0	0.87	174.07	87.03		
16.02.2005 13:30:00	192.5	0.87	167.37	83.68		
16.02.2005 14:00:00	199.4	0.87	172.87	86.44		
16.02.2005 14:30:00	191.9	0.87	166.28	83.14		
16.02.2005 15:00:00	194.9	0.87	169.60	84.80		
16.02.2005 15:30:00	182.0	0.87	157.85	78.93		
16.02.2005 16:00:00	170.0	0.87	147.33	73.67		
16.02.2005 16:30:00	87.8	0.86	75.74	37.87		

**Table A-16: Maximum daily Energy supplied by the 200kVA inverter at unity PF**

Time [hour]	Inverter Capacity [kVA]	PF	Inverter Capacity [kW]	Energy [kWh]	Total Energy [kWh]	Duration [hour]
16.02.2005 10:00:00	49.4	1	49.4	24.70	1070.45	7.5
16.02.2005 10:30:00	72.5	1	72.5	36.25		
16.02.2005 11:00:00	108.5	1	108.5	54.25		
16.02.2005 11:30:00	127.1	1	127.1	63.55		
16.02.2005 12:00:00	177.8	1	177.8	88.90		
16.02.2005 12:30:00	187.1	1	187.1	93.55		
16.02.2005 13:00:00	200.0	1	200.0	100.00		
16.02.2005 13:30:00	192.5	1	192.5	96.25		
16.02.2005 14:00:00	199.4	1	199.4	99.70		
16.02.2005 14:30:00	191.9	1	191.9	95.95		
16.02.2005 15:00:00	194.9	1	194.9	97.45		
16.02.2005 15:30:00	182.0	1	182.0	91.00		
16.02.2005 16:00:00	170.0	1	170.0	85.00		
16.02.2005 16:30:00	87.8	1	87.8	43.90		

# APPENDIX B

## B Raylite Tubular RCT datasheet



**FIRST  
NATIONAL  
BATTERY**

THROUGH CARING WE LEAD  
FIRST NATIONAL BATTERY  
INDUSTRIAL (Pty) Ltd

**RAYLITE**

## Tubular Cells



ISO 14001  
ISO 9001: 2000  
ISO/TS 16949: 2002

Complies with: SABS IEC 60896-1,2: 1987

*± 12 years.*

## Applications:

- Emergency Lighting
- Telecommunications
- Railway Signalling
- DC Emergency System

The RAYLITE Tubular Cell offers outstanding reliability over an expected working life of 10 to 12 years in float charge applications. These cells are capable of high cycling.

The round tube has the following advantages over the square tube:

- it offers a more uniform active material distribution around the supporting spines, resulting in more efficient utilisation of materials.
- it is less prone to distortion under operating conditions

## Design Features

### POSITIVE PLATE

The tubular gauntlet plate construction consists of special lead alloy spines in complete contact with superior active material, effectively retained by woven terylene tubes. The terylene gauntlets, which are resin impregnated, combine high tensile strength with resilience, retaining the active material while enabling the electrolyte to penetrate freely. This ensures a high power output per unit volume.

### NEGATIVE PLATE

The negative plate is of a special alloy grid, pasted with a highly-porous paste formulation, giving a balanced performance and life, and complementing the positive plate construction.

### VENT PLUGS

The special design effectively returns all acid spray to the cell, yet permits free exit of oxygen and hydrogen.

### CONTAINER

Moulded, DIN standard, transparent styrene acrylonitrile, giving very high insulating properties which eliminate the use of insulators. Age or acid contact will not cause deterioration.

### LIDS

Moulded from opaque styrene acrylonitrile.

### END BUFFERS

PVC end buffers provide additional lateral support at each end of the element, ensuring a compact assembly to prevent the plates from splaying.

### SEPARATORS

High quality, microporous rubber separators. Chemically-inert, with a high degree of porosity, they offer minimum internal resistance. The sleeve separators prevent short-circuiting caused by mousing.

## Product and Service Benefits

- **Locally-Manufactured Range**  
Manufactured by a South African company, proven under South African conditions.
- **Premier Quality**  
Conforms to DIN and IEC standards and manufactured to ISO 9001:2000 quality standards.
- **Nationwide After-Sales Support**  
Countrywide network of branches and agencies, with access to information to ensure sound technical backup.
- **Proven Reliability**  
Used successfully, achieving claimed life, in numerous applications.
- **Customer Care**  
Every Raylite standby cell carries a comprehensive product warranty backed by the industry leader and supported by a national distributor network.



## Tubular Capacities, Weights And Dimensions

Type	Capacity in amp-hours at 25°C when discharged in			Initial Charge Current	Weight		Approx. quantity of acid 1.250 spg	External dimensions of cell container			Overall height of cells	Centres of cells	Width of single row stillage or stand	Width of double row stillage or stand
	10 Hrs	3 Hrs	1 Hr		Cell compl. filled	Acid only 1.250 spg		Length	Width	Height				
Final voltage	1.85	1.80	1.75	Amps	Kg	Kg	Litres	mm	mm	mm	mm	mm	mm	mm
3RCT150	150	108	51	10.5	16.3	4.6	3.8	103	206	355	435	113	376	649
4RCT200	200	144	68	14.0	19.9	4.6	3.7	103	206	355	435	113	376	649
5RCT250	250	180	85	17.5	24.8	5.6	4.5	124	206	355	435	134	376	649
6RCT300	300	216	102	21.0	29.8	6.5	5.4	145	206	355	435	155	376	649
5RCT350	350	260	120	24.5	34.7	7.9	5.3	124	206	471	551	134	376	649
6RCT420	420	312	216	29.4	41.2	9.0	7.2	145	206	471	551	155	376	649
7RCT490	490	364	252	34.3	48.0	10.4	5.3	166	206	471	551	176	376	649
6RCT600	600	432	284	42.0	42.4	9.0	7.2	145	206	646	726	216	376	649
7RCT700	700	504	343	49.0	57.1	15.1	14.5	191	210	646	726	220	361	687
8RCT800	800	576	392	56.0	61.1	15.5	13.3	191	210	646	726	220	361	687
9RCT900	900	648	441	63.0	73.0	22.0	18.3	233	210	646	726	220	403	756
10RCT1000	1000	720	490	70.0	77.1	21.4	17.1	233	210	646	726	220	403	756
11RCT1100	1100	792	539	77.0	88.1	26.9	21.5	275	210	646	726	220	445	840
12RCT1200	1200	864	588	84.0	92.2	25.4	20.3	275	210	646	726	220	445	840
11RCT1375	1375	990	660	96.3	108.8	32.3	25.8	275	210	771	851	220	275	620
12RCT 1500	1500	1080	720	106.0	114.7	31.2	25.0	275	210	771	851	220	275	620
13RCT1625	1625	1170	780	113.8	138.3	46.8	37.4	397	212	771	851	222	397	864
14RCT1750	1750	1260	840	122.5	144.1	45.6	36.5	397	212	771	851	222	397	864
15RCT1875	1875	1350	900	131.3	150.5	44.9	35.9	397	212	771	851	222	397	864
16RCT2000	2000	1440	960	140.0	156.3	44.1	35.3	397	212	771	851	222	397	864
17RCT2125	2125	1530	1020	148.8	181.0	61.3	49.0	487	212	771	851	222	487	1094
18RCT2250	2250	1620	1080	157.5	185.1	58.4	46.9	487	212	771	851	222	487	1094
19RCT2375	2375	1710	1140	166.3	188.9	55.1	44.1	487	212	771	851	222	487	1094
20RCT2500	2500	1800	1200	175.0	194.3	53.5	42.6	487	212	771	851	222	487	1094
24RCT3000	3000	2160	1440	210.0	244.0	55.0	44.0	576	212	771	851	222	-	-

# First National Battery

ESTABLISHED IN 1931, FIRST NATIONAL BATTERY IS A LEADING MANUFACTURER OF LEAD ACID BATTERIES IN SOUTH AFRICA.

THE COMPANY PRODUCES MORE THAN 2 000 000 BATTERIES ANNUALLY TO PROVIDE ELECTRICAL POWER FOR PASSENGER CARS, TRUCKS, TRACTORS, FORKLIFT TRUCKS, BOATS, RAILWAY LOCOMOTIVES AND COACHES, UNDERGROUND LOCOMOTIVES AND MINERS' CAP LAMPS, POWER STATIONS, SWITCH YARDS, FARM LIGHTING, SOLAR SYSTEMS, COMPUTERS, TELECOMMUNICATIONS EQUIPMENT ... AND A HOST OF OTHER USES.

FIRST NATIONAL BATTERY ACKNOWLEDGES THAT SUPERIOR TECHNOLOGY, CONSISTENT PRODUCT QUALITY AND DEDICATED CUSTOMER SERVICE ARE MINIMUM REQUIREMENTS TO ENABLE THE COMPANY TO MAINTAIN ITS POSITION AS AN INDUSTRY LEADER

THE COMPANY'S VALUES ARE REPRESENTED BY ITS MOTTO: THROUGH CARING WE LEAD

PROOF OF THESE VALUES IS TO BE FOUND IN THE MANY PRODUCT AND SERVICE QUALITY AWARDS AND CERTIFICATES PRESENTED TO FIRST NATIONAL BATTERY OVER MANY YEARS OF SERVICE TO BATTERY USERS  
TRACTION BATTERIES AND CELLS ARE MANUFACTURED AND COMPLY WITH ISO 9001:2000, IEC 60254-1 AND 2 (1997)

## 4 DEDICATED MANUFACTURING SITES

BUFFALO VIEW ROAD, EAST LONDON 6 000M<sup>2</sup> FACTORY  
ISO 9001:2000 AND ISO 14001 CERTIFIED  
INDUSTRIAL BATTERY MANUFACTURING  
FORKTRUCK BATTERIES: STANDBY BATTERIES: MINING BATTERIES

SETTLERS WAY, EAST LONDON 9 200M<sup>2</sup> FACTORY  
ISO/TS 16949:2002 AND ISO 14001 CERTIFIED  
AUTOMOTIVE BATTERY MANUFACTURING  
7 000 BATTERIES PER DAY  
ALSO TECHNICAL CENTRE

FORT JACKSON 5 000M<sup>2</sup> FACTORY  
ISO/TS 16949:2002 AND ISO 14001 CERTIFIED  
PLASTIC INJECTION MOULDING  
50 TON-860 TON INJECTION MOULDING MACHINES  
18 MILLION PIECES PER ANNUM  
ALSO TOOLROOM

LIVERPOOL ROAD BENONI  
ISO/TS 16949:2002 AND ISO 14001 CERTIFIED  
LEAD SMELTER  
8 000 TONS RECYCLED LEAD PER ANNUM  
ALSO WAREHOUSING & DISTRIBUTION  
FORMATION & FINISHING LINE  
MARKETING & FINANCE DIVISIONS



THROUGH CARING WE LEAD  
FIRST NATIONAL BATTERY  
INDUSTRIAL (Pty) Ltd

FIRST NATIONAL BATTERY WILL REMAIN THE EXCLUSIVE MANUFACTURER OF BATTERIES AND SUPPLIER OF PRODUCTS AND SERVICES TO FIRST NATIONAL BATTERY INDUSTRIAL. IN KEEPING WITH THEIR OBJECTIVE TOWARDS TRUE BLACK EMPOWERMENT THEY PLAN TO FURTHER INCREASE

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FIRST NATIONAL BATTERY IS THE REGISTERED USER OF THE TRADEMARK RAYLITE™ IN SOUTH AFRICA

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**Standby Power - Raylite Tubular RCT**  
**Constant Current Discharge Data (amps at 25°C )**

Click Cell type to view or print additional detail and discharge data for a specific cell. To view data for entire range, click here: [Specification : Constant Power](#)

10RCT1000	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1200	1150	1080	977	820	697	590	370	263	173	155	127	100
	1.65	1100	1040	970	898	780	667	560	370	263	173	155	127	100
	1.70	967	920	870	817	730	620	520	360	258	173	155	127	100
	1.75	842	800	760	718	650	566	490	330	255	173	155	127	100
	1.80	733	690	650	620	570	500	430	300	240	172	155	127	100
	1.85	527	520	510	502	480	430	380	270	225	167	150	125	100
11RCT1100	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1320	1265	1188	1074	902	766	649	407	290	190	171	139	110
	1.65	1210	1144	1067	988	858	733	616	407	290	190	171	139	110
	1.70	1063	1012	957	898	803	682	572	396	284	190	171	139	110
	1.75	926	880	836	790	715	623	539	363	281	190	171	139	110
	1.80	807	759	715	682	627	550	473	330	264	189	171	139	110
	1.85	579	572	561	552	528	473	418	297	248	183	165	138	110
11RCT1375	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1500	1408	1320	1240	1111	952	803	517	363	242	214	174	138
	1.65	1400	1287	1188	1127	1023	890	759	495	363	242	214	174	138
	1.70	1120	1111	1078	1007	891	796	715	495	363	242	214	174	138
	1.75	907	902	886	852	792	724	660	457	345	240	208	171	138
	1.80	772	769	765	740	692	637	583	440	330	231	208	171	138
	1.85	646	643	627	605	561	516	473	363	290	220	200	168	138
12RCT1200	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1440	1380	1296	1172	984	836	708	444	316	208	186	152	120
	1.65	1320	1248	1164	1078	936	800	672	444	316	208	186	152	120
	1.70	1160	1104	1044	980	876	744	624	432	310	208	186	152	120
	1.75	1010	960	912	862	780	680	588	396	306	208	186	152	120
	1.80	880	828	780	744	684	600	516	360	288	206	186	152	120
	1.85	632	624	612	602	576	516	456	324	270	200	180	150	120
12RCT1500	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1636	1536	1440	1353	1212	1039	876	564	396	264	233	190	150
	1.65	1527	1404	1296	1229	1116	971	828	540	396	264	233	190	150
	1.70	1222	1212	1176	1099	972	868	780	540	396	264	233	190	150
	1.75	989	984	966	929	864	790	720	498	376	262	227	187	150
	1.80	842	839	834	807	756	695	636	480	360	252	227	187	150
	1.85	705	701	684	660	612	563	516	396	316	240	218	183	150
13RCT1625	VpC	5 Min	10 Min	15 Min	20 Min	30 Min	45 Min	1 Hr	2 Hr	3 Hr	5 Hr	6 Hr	8 Hr	10 Hr
	1.60	1773	1664	1560	1465	1313	1125	949	611	429	286	253	206	163
	1.65	1655	1521	1404	1332	1209	1052	897	585	429	286	253	206	163
	1.70	1324	1313	1274	1190	1053	941	845	585	429	286	253	206	163

	1.75	1072	1066	1047	1007	936	856	780	540	408	284	246	202	163
	1.80	912	909	904	875	819	753	689	520	390	273	246	202	163
	1.85	763	760	741	715	663	610	559	429	343	260	236	199	163
<b>14RCT1750</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	1909	1792	1680	1578	1414	1212	1022	658	462	308	272	221	175
	1.65	1782	1638	1512	1434	1302	1133	966	630	462	308	272	221	175
	1.70	1425	1414	1372	1282	1134	1013	910	630	462	308	272	221	175
	1.75	1154	1148	1127	1084	1008	921	840	581	439	305	265	218	175
	1.80	983	979	973	942	882	811	742	560	420	294	265	218	175
	1.85	822	818	798	770	714	657	602	462	369	280	255	214	175
<b>15RCT1875</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2045	1920	1800	1691	1515	1298	1095	705	495	330	292	237	188
	1.65	1909	1755	1620	1537	1395	1214	1035	675	495	330	292	237	188
	1.70	1527	1515	1470	1373	1215	1085	975	675	495	330	292	237	188
	1.75	1237	1230	1206	1162	1080	987	900	623	470	327	284	233	188
	1.80	1053	1049	1043	1009	945	869	795	600	450	315	284	233	188
	1.85	881	877	855	825	765	704	645	495	395	300	273	229	188
<b>16RCT2000</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2182	2048	1920	1804	1616	1385	1168	752	528	352	311	253	200
	1.65	2036	1872	1728	1639	1488	1295	1104	720	528	352	311	253	200
	1.70	1629	1616	1568	1465	1296	1158	1040	720	528	352	311	253	200
	1.75	1319	1312	1288	1239	1152	1053	960	664	502	349	303	249	200
	1.80	1123	1119	1112	1076	1008	927	848	640	480	336	303	249	200
	1.85	940	935	912	880	816	751	688	528	422	320	291	244	200
<b>17RCT2125</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2318	2176	2040	1916	1717	1471	1241	799	561	374	331	269	213
	1.65	2164	1989	1836	1742	1581	1375	1173	765	561	374	331	269	213
	1.70	1731	1717	1666	1556	1377	1230	1105	765	561	374	331	269	213
	1.75	1402	1394	1369	1317	1224	1119	1020	706	533	371	321	264	213
	1.80	1193	1188	1182	1144	1071	984	901	680	510	357	321	264	213
	1.85	998	994	969	935	867	797	731	561	448	340	309	260	213
<b>18RCT2250</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2455	2304	2160	2029	1818	1558	1314	846	594	396	350	285	225
	1.65	2291	2106	1944	1844	1674	1456	1242	810	594	396	350	285	225
	1.70	1833	1818	1764	1648	1458	1303	1170	810	594	396	350	285	225
	1.75	1484	1476	1449	1394	1296	1185	1080	747	565	393	340	280	225
	1.80	1263	1258	1251	1211	1134	1042	954	720	540	378	340	280	225
	1.85	1057	1052	1026	990	918	844	774	594	475	360	327	275	225
<b>19RCT2375</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2591	2432	2280	2142	1919	1644	1387	893	627	418	370	301	238
	1.65	2418	2223	2052	1947	1767	1537	1311	855	627	418	370	301	238
	1.70	1935	1919	1862	1739	1539	1375	1235	855	627	418	370	301	238
	1.75	1567	1558	1530	1472	1368	1251	1140	789	596	415	359	295	238

	1.80	1333	1328	1321	1278	1197	1100	1007	760	570	399	359	295	238
	1.85	1116	1111	1083	1045	969	891	817	627	501	380	345	290	238
<b>20RCT2500</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	2727	2560	2400	2255	2020	1731	1460	940	660	440	389	316	250
	1.65	2545	2340	2160	2049	1860	1618	1380	900	660	440	389	316	250
	1.70	2036	2020	1960	1831	1620	1447	1300	900	660	440	389	316	250
	1.75	1649	1640	1610	1549	1440	1316	1200	830	627	436	378	311	250
	1.80	1404	1398	1390	1345	1260	1158	1060	800	600	420	378	311	250
	1.85	1175	1169	1140	1100	1020	938	860	660	527	400	364	305	250
<b>3RCT150</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	245	207	180	159	129	106	87.0	51.0	39.0	25.2	22.5	18.7	15.0
	1.65	200	186	168	150	122	100	84.0	50.1	39.0	25.2	22.5	18.7	15.0
	1.70	192	171	150	135	114	96.0	81.0	49.5	39.0	25.2	22.5	18.7	15.0
	1.75	165	150	135	122	105	89.0	75.0	48.3	39.0	25.2	22.5	18.7	15.0
	1.80	132	129	120	111	96.0	80.0	66.0	45.9	36.0	25.0	22.5	18.7	15.0
	1.85	108	105	99.0	92.0	81.0	70.0	60.0	43.5	33.0	22.0	19.9	17.0	15.0
<b>4RCT200</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	326	276	240	212	172	141	116	66.0	52.0	33.6	30.0	25.0	20.0
	1.65	266	248	224	200	162	133	112	66.8	52.0	33.6	30.0	25.0	20.0
	1.70	256	228	200	180	152	128	108	65.0	52.0	33.6	30.0	25.0	20.0
	1.75	220	200	180	163	140	119	100	64.4	52.0	33.6	30.0	25.0	20.0
	1.80	176	172	160	147	128	107	88.0	61.2	48.0	33.3	30.0	25.0	20.0
	1.85	144	140	132	123	108	93.3	80.0	58.0	44.0	29.3	26.5	22.6	20.0
<b>5RCT250</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	408	345	300	265	215	176	145	85.0	65.0	42.0	37.5	31.2	25.0
	1.65	333	310	280	250	203	167	140	83.5	65.0	42.0	37.5	31.2	25.0
	1.70	320	285	250	225	190	160	135	82.5	65.0	42.0	37.5	31.2	25.0
	1.75	275	250	225	203	175	148	125	80.5	65.0	42.0	37.5	31.2	25.0
	1.80	220	215	200	184	160	133	110	76.5	60.0	41.6	37.5	31.2	25.0
	1.85	180	175	165	153	135	117	100	72.5	55.0	36.6	33.1	28.3	25.0
<b>5RCT350</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	505	455	408	367	305	258	240	120	90.0	60.6	54.0	44.2	35.0
	1.65	450	410	375	340	290	248	210	120	90.0	60.6	54.0	44.2	35.0
	1.70	386	360	335	307	265	223	188	120	90.0	60.6	54.0	44.2	35.0
	1.75	313	310	298	277	243	210	180	120	90.0	60.6	54.0	44.2	35.0
	1.80	273	265	253	236	210	186	165	115	87.5	60.6	54.0	44.2	35.0
	1.85	210	210	205	193	175	158	143	100	77.5	58.0	53.0	44.0	35.0
<b>6RCT300</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	490	414	350	318	258	212	174	102	78.0	50.4	45.0	37.5	30.0
	1.65	400	372	336	300	243	200	168	100	78.0	50.4	45.0	37.5	30.0
	1.70	384	342	300	270	228	192	162	99.0	78.0	50.4	45.0	37.5	30.0
	1.75	330	300	270	244	210	178	150	96.6	78.0	50.4	45.0	37.5	30.0
	1.80	264	258	240	221	192	160	132	91.8	72.0	50.0	45.0	37.5	30.0

	1.85	216	210	198	184	162	140	120	87.0	66.0	44.0	39.8	34.0	30.0
<b>6RCT420</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	606	546	490	440	366	310	288	144	108	72.6	64.8	53.1	42.0
	1.65	540	492	450	408	348	297	252	144	108	72.6	64.8	53.1	42.0
	1.70	463	432	402	369	318	267	225	144	108	72.6	64.8	53.1	42.0
	1.75	375	372	357	332	291	252	216	144	108	72.6	64.8	53.1	42.0
	1.80	327	318	303	283	252	223	198	138	105	72.6	64.8	53.1	42.0
	1.85	252	252	246	231	210	190	171	120	93.0	69.6	63.6	52.8	42.0
<b>6RCT600</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	720	690	648	586	492	418	354	222	158	104	93.0	76.0	60.0
	1.65	660	624	582	539	468	400	336	222	158	104	93.0	76.0	60.0
	1.70	580	552	522	490	438	372	312	216	155	104	93.0	76.0	60.0
	1.75	505	480	456	431	390	340	294	198	153	104	93.0	76.0	60.0
	1.80	440	414	390	372	342	300	258	180	144	103	93.0	76.0	60.0
	1.85	316	312	306	301	288	258	228	162	135	100	90.0	75.0	60.0
<b>7RCT490</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	707	637	572	513	427	362	336	168	126	84.8	75.6	62.0	49.0
	1.65	630	574	525	476	406	347	294	168	126	84.8	75.6	62.0	49.0
	1.70	540	504	469	430	371	312	263	168	126	84.8	75.6	62.0	49.0
	1.75	438	434	417	387	340	294	252	168	126	84.8	75.6	62.0	49.0
	1.80	382	371	354	330	294	260	231	161	123	84.8	75.6	62.0	49.0
	1.85	294	294	287	270	245	222	200	140	109	81.2	74.2	61.6	49.0
<b>7RCT700</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	840	805	756	684	574	488	413	259	184	121	109	88.7	70.0
	1.65	770	728	679	629	546	467	392	259	184	121	109	88.7	70.0
	1.70	677	644	609	572	511	434	364	252	181	121	109	88.7	70.0
	1.75	589	560	532	503	455	396	343	231	175	121	109	88.7	70.0
	1.80	513	483	455	434	399	350	301	210	168	120	109	88.7	70.0
	1.85	369	364	357	351	336	301	266	189	158	117	105	87.5	70.0
<b>8RCT800</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	960	920	864	781	656	557	472	296	211	138	124	101	80.0
	1.65	880	832	776	719	624	533	448	296	211	138	124	101	80.0
	1.70	773	736	696	653	584	496	416	288	207	138	124	101	80.0
	1.75	673	640	608	575	520	453	392	264	204	138	124	101	80.0
	1.80	587	552	520	496	456	400	344	240	192	137	124	101	80.0
	1.85	421	416	408	401	384	344	304	216	180	133	120	100	80.0
<b>9RCT900</b>	<b>VpC</b>	<b>5 Min</b>	<b>10 Min</b>	<b>15 Min</b>	<b>20 Min</b>	<b>30 Min</b>	<b>45 Min</b>	<b>1 Hr</b>	<b>2 Hr</b>	<b>3 Hr</b>	<b>5 Hr</b>	<b>6 Hr</b>	<b>8 Hr</b>	<b>10 Hr</b>
	1.60	1080	1035	972	879	738	627	531	333	237	156	140	114	90.0
	1.65	990	936	873	809	702	600	504	333	237	156	140	114	90.0
	1.70	870	828	783	735	657	558	468	324	233	156	140	114	90.0
	1.75	758	720	684	647	585	510	441	297	230	156	140	114	90.0
	1.80	660	621	585	558	513	450	387	270	216	155	140	114	90.0
	1.85	474	468	459	452	432	387	342	243	203	150	135	113	90.0



# APPENDIX B

## B Raylite Tubular RCT datasheet

# APPENDIX C

## C Clarke and Park Transformation Analysis

The AC system was first designed and implemented in 1885 by William Stanly. In 1888, the three-phase induction motor was designed by Nikola Tesla, which has since become the workhorse of the industry [29]. Since then the three-phase AC system has become the normal application for generation, transmission and distribution of electricity around the world.

However, in terms of control design DC system signals are much easier to control than AC system signals simply because the DC signal is a constant. For example in control engineering to track a step function a high level mathematical analysis is not required, a simple PI control type 1 would be adequate [19]. Thus, new techniques such as Clarke and Park Transform were developed to enable the transformation of the three-phase AC signal into DC signals.

Clarke Transformation takes the three-phase static signals and represent it as two signals on a stationary reference plane, orthogonal to each other, from Texas instruments report literature [34]. It was stated that due to this transformation, the real and imaginary part of the three-phase was obtained.

The Park Transformation on the other hand takes these two signals and puts on a rotating reference plane, it rotates at the same frequency as the three-phase signals, which in this case have the value of 50Hz. This last transformation has the effect of representing the real and the imaginary part of the three-phase signal, as DC values.

The Clarke transform results in reference plane known as alpha-beta plane; where alpha ( $\alpha$ ) is the real part and beta ( $\beta$ ) the imaginary part. Clarke Transformation is used to transform either a voltage or a current therefore a neutral variable,  $x$ , was used in equation (C-1).

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \quad (\text{C-1})$$

The Park transformation results in reference plane known as d-q plane. The Park Transformation equation is represented in equation (C-2). The d-component is the real part and q-component the imaginary part.

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} \quad (\text{C-2})$$

Therefore, throughout this thesis report, Clarke transform will be treated as  $\alpha$ - $\beta$  and Park transform as d-q.

### C.1 Derivation of Clarke Transform

From Glover and Sarma analysis [29], it was noticed that the equation (C-1) was used for positive sequence three-phase connection. The analyses below will illustrate this.

There are three types of sequence on a three-phase source: zero-sequence, positive-sequence, and negative-sequence. It was explained that according to Fortescue (the founder of the method of symmetrical components, in 1918) the phase voltage or current can be resolved into the sequence discussed above and are defined as follows [29]:

- *“Zero-sequence components, consisting of three phasors with equal magnitudes and with zero phase displacement.”*[29]
- *“Positive-sequence components, consisting of three phasors with equal magnitudes,  $\pm 120^\circ$  phase displacement and positive sequence.”*[29]

- “Negative-sequence components, consisting of three phasors with equal magnitudes,  $\pm 120^\circ$  phase displacement and negative sequence.”[29]

Figure C.1-1 below shows the sequences, the zero, positive and negative respectively as discussed in [29].

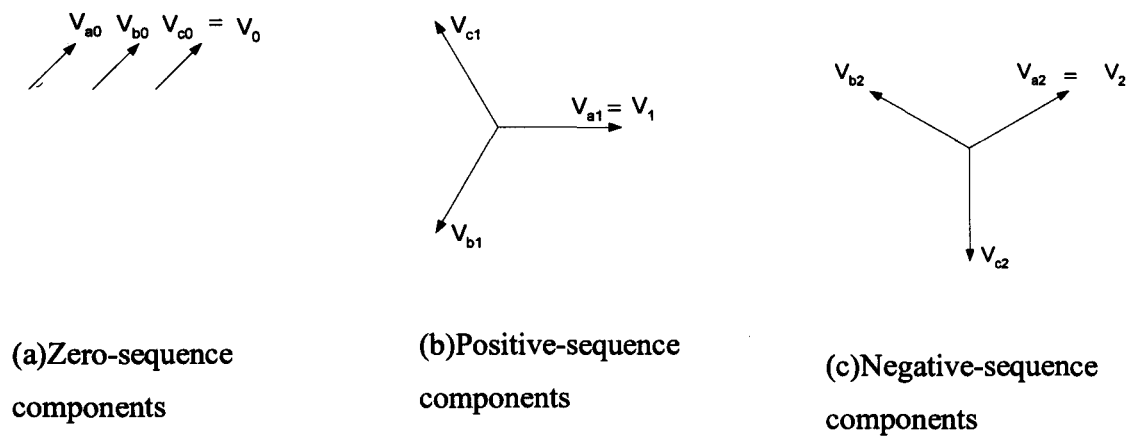


Figure C.1-1: Zero, Positive and Negative sequence phasor [29].

The sequences as illustrated in figure C.1-1 are defined mathematically as shown in the equation (C.1-1) [29].

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix} \begin{pmatrix} V_0 \\ V_1 \\ V_2 \end{pmatrix} \tag{C.1-1}$$

Where  $\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix}$  represent the phase voltages,  $\begin{pmatrix} V_0 \\ V_1 \\ V_2 \end{pmatrix}$  illustrates the sequence voltages and the

3×3 matrix  $\begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix}$  represent the transformation matrix [29].

Solving for the sequences voltages from equation (C.1-1), equation (C.1-2) was obtained.

$$\begin{pmatrix} V_0 \\ V_1 \\ V_2 \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (\text{C.1-2})$$

The constant  $\frac{1}{3}$  in the 3×3 matrix of equation (C.1-2) was the result of taking the inverse of the 3×3 matrix of equation (C.1-1) [29].

Now solving for each sequence voltage individually from equation (C.1-2), equations (C.1-3), (C.1-4) and (C.1-5) were obtained.

$$V_0 = \frac{1}{3}(V_a + V_b + V_c) \quad (\text{C.1-3})$$

$$V_1 = \frac{1}{3}(V_a + aV_b + a^2V_c) \quad (\text{C.1-4})$$

$$V_2 = \frac{1}{3}(V_a + a^2V_b + aV_c) \quad (\text{C.1-5})$$

The letter “a” was defined as illustrated in equation (C.1-6) [29].

$$a = 1\angle 120^\circ = \frac{-1}{2} + j\frac{\sqrt{3}}{2} \quad (\text{C.1-6})$$

It was also mentioned that if a phasor would be multiplied by “a”, then it would be rotated by 120° in a counter clockwise direction [29]. Substitute equation (C.1-6) into equations (C.1-4) and (C.1-5), equations (C.1-7) and (C.1-8) were obtained.

$$V_1 = \frac{1}{3} \left( V_a + \left( \frac{-1}{2} + j \frac{\sqrt{3}}{2} \right) V_b + \left( \frac{-1}{2} + j \frac{\sqrt{3}}{2} \right)^2 V_c \right) \quad (C.1-7)$$

$$V_2 = \frac{1}{3} \left( V_a + \left( \frac{-1}{2} + j \frac{\sqrt{3}}{2} \right)^2 V_b + \left( \frac{-1}{2} + j \frac{\sqrt{3}}{2} \right) V_c \right) \quad (C.1-8)$$

Expanding the square part of equations (C.1-7) and (C.1-8), equations (C.1-9) and (C.1-10) were obtained for  $V_1$  and  $V_2$  respectively.

$$V_1 = \frac{1}{3} \left( V_a + \left( -\frac{1}{2} + j \frac{\sqrt{3}}{2} \right) V_b + \left( -\frac{1}{2} - j \frac{\sqrt{3}}{2} \right) V_c \right) \quad (C.1-9)$$

$$V_2 = \frac{1}{3} \left( V_a + \left( -\frac{1}{2} - j \frac{\sqrt{3}}{2} \right) V_b + \left( -\frac{1}{2} + j \frac{\sqrt{3}}{2} \right) V_c \right) \quad (C.1-10)$$

Continuing with analysis and representing  $V_1$  and  $V_2$  with its real and imaginary components  $V_\alpha$  and  $V_\beta$  respectively, equations (C.1-11), (C.1-12), (C.1-13) and (C.1-14) were obtained.

$$V_1 = V_\alpha + jV_\beta = \frac{1}{3} \left( \left( V_a - \frac{1}{2} V_b - \frac{1}{2} V_c \right) + j \left( \frac{\sqrt{3}}{2} V_b - \frac{\sqrt{3}}{2} V_c \right) \right) \quad (C.1-11)$$

$$V_2 = V_\alpha + jV_\beta = \frac{1}{3} \left( \left( V_a - \frac{1}{2}V_b - \frac{1}{2}V_c \right) + j \left( -\frac{\sqrt{3}}{2}V_b + \frac{\sqrt{3}}{2}V_c \right) \right) \quad (\text{C.1-12})$$

$$V_1 = \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (\text{C.1-13})$$

$$V_2 = \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (\text{C.1-14})$$

Equations (C.1-13) and (C.1-14) represent the forward Clarke Transformation for positive and negative sequence connection respectively ignoring the zero sequence part.

Therefore positive sequence forward Clarke transform equation (C.1-13) will be used throughout this thesis because the three-phase source connection used was positive sequence, whereby the phase voltage  $V_a$  leads  $V_b$  by  $120^\circ$  and lags  $V_c$  by  $120^\circ$  see figure C.2-1.

## C.2 Derivation of Park Transform

Let the phase voltage  $V_a$ ,  $V_b$  and  $V_c$  be defined as represented in the following equations:

$$V_a = \sin(\omega t) \quad (\text{C.2-1})$$

$$V_b = \sin\left(\omega t - \frac{2\pi}{3}\right) \quad (\text{C.2-2})$$

Now using equation (C.1-13) on figure C.2-1 the three-phase voltage  $V_a$ ,  $V_b$  and  $V_c$ , which are  $120^\circ$  from each other in positive sequence were transformed to two-phase voltage  $V_\alpha$  and  $V_\beta$  orthogonal to each other.

One thing that should be noted was that when using the positive sequence forward Clarke Transformation, equation (C.1-13), on a positive three-phase voltage connection,  $V_\alpha$  leads  $V_\beta$  by  $90^\circ$ . Figure C.2-2 illustrates this. However, if equation (C.1-14), the negative forward Clarke Transformation, were used instead,  $V_\beta$  would lead  $V_\alpha$  by  $90^\circ$ , figure C.2-3 illustrate the scenario.

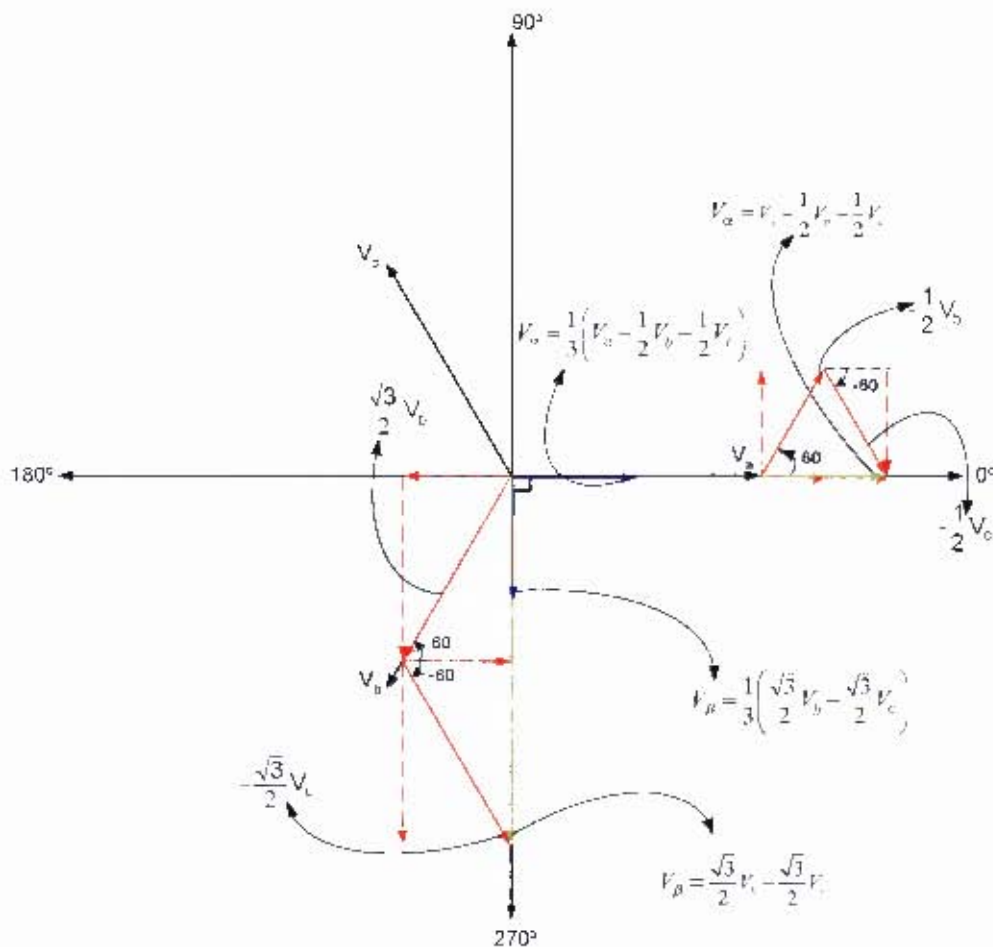


Figure C.2-2: Positive Clarke Transformation applied on a positive sequence three-phase connection

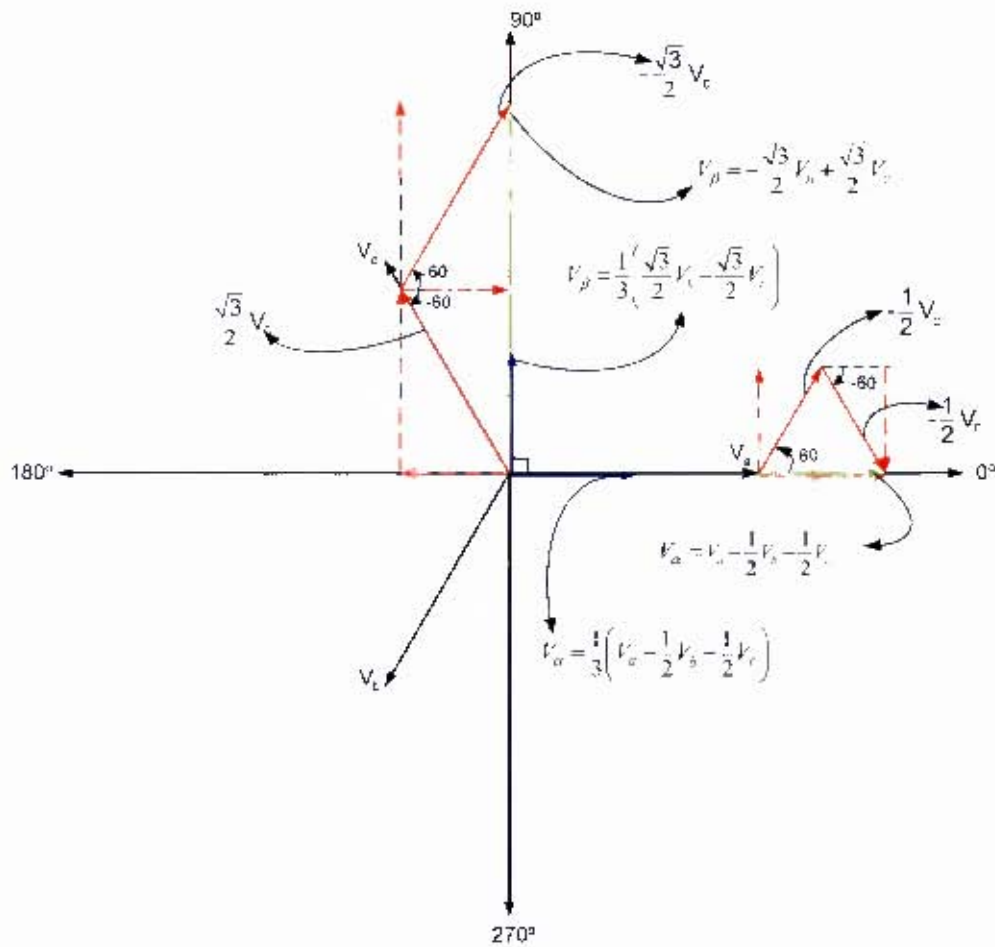


Figure C.2-3: Negative Clarke Transformation applied on a positive sequence three-phase connection

Using equation (C.1-13), equations (C.2-5) and (C.2-6) were obtained.

$$\vec{V}_\alpha = \frac{1}{3} \left( \vec{V}_a - \frac{1}{2} \vec{V}_b - \frac{1}{2} \vec{V}_c \right) \quad (\text{C.2-5})$$

$$\vec{V}_\beta = \frac{1}{3} \left( \frac{\sqrt{3}}{2} \vec{V}_b - \frac{\sqrt{3}}{2} \vec{V}_c \right) \quad (\text{C.2-6})$$

Moreover, in most literature about Clarke Transformation, [34, 17], the coefficient of Clarke transformer instead of being  $\frac{1}{3}$  as discussed before, was  $\frac{2}{3}$ . The reason behind was to make  $V_\alpha$  equals to  $V_a$  in magnitude.

Looking carefully at figure C.2-2 we can see that  $V_\alpha$  and  $V_\beta$  are formed by adding their respective phase vectors in vector summation. In addition, it can be seen that in the  $V_\alpha$  equation,  $V_a$  was at zero degrees,  $-\frac{1}{2}V_b$  was at  $60^\circ$ , and  $-\frac{1}{2}V_c$  was at  $-60^\circ$ , however  $V_b$  and  $V_c$  were phase shifted from  $V_a$  by  $-120$  and  $-240$  respectively. Moreover in equation (C.2-6)  $\frac{\sqrt{3}}{2}V_b$  was at  $60^\circ$  and  $-\frac{\sqrt{3}}{2}V_c$  was at  $-60^\circ$ .

Assuming, for argument sake, that  $V_a$ ,  $V_b$  and  $V_c$  magnitude is unity. Now using the above discussed in equations (C.2-5) and (C.2-6), equations (C.2-7) and (C.2-8) were obtained.

$$\vec{V}_\alpha = \frac{1}{3} \left( 1 \angle 0^\circ - \frac{1}{2} \angle -120^\circ - \frac{1}{2} \angle -240^\circ \right) \quad (C.2-7)$$

$$\vec{V}_\beta = \frac{1}{3} \left( \frac{\sqrt{3}}{2} \angle -120^\circ - \frac{\sqrt{3}}{2} \angle -240^\circ \right) \quad (C.2-8)$$

Decomposing equations (C.2-7) and (C.2-8), which were in polar form, to rectangular form, the equations below, were yielded

$$\vec{V}_\alpha = \frac{1}{3} \left( \left( 1 + \frac{1}{4} + \frac{1}{4} \right) + j \left( \frac{\sqrt{3}}{4} - \frac{\sqrt{3}}{4} \right) \right) \quad (C.2-9)$$

$$\vec{V}_\beta = \frac{1}{3} \left( \left( \cancel{-\frac{\sqrt{3}}{4}} + \frac{\sqrt{3}}{4} \right) + j \left( -\frac{3}{4} - \frac{3}{4} \right) \right) \quad (\text{C.2-10})$$

$$\vec{V}_\alpha = \frac{1}{3} \left( \frac{3}{2} \right) \quad (\text{C.2-11})$$

$$\vec{V}_\beta = \frac{1}{3} \left( -j \frac{3}{2} \right) \quad (\text{C.2-12})$$

As was mentioned above, by multiplying the Clarke Transformation equation by a coefficient of  $\frac{2}{3}$ , it would result in  $V_\alpha$  and  $V_a$  being equal. Applying now this argument to equations (C.2-11) and (C.2-12), equations (C.2-13) and (C.2-14) were obtained.

$$\vec{V}_\alpha = \frac{2}{3} \left( \frac{3}{2} \right) = 1 \quad (\text{C.2-13})$$

$$\vec{V}_\beta = \frac{2}{3} \left( -j \frac{3}{2} \right) = -j1 \quad (\text{C.2-14})$$

From equation (C.2-13), it was confirmed that  $V_\alpha$  equal to  $V_a$  when multiplied by  $\frac{2}{3}$ , recall that  $V_a$  was assumed to be unity in magnitude. Now replacing  $\frac{1}{3}$  by  $\frac{2}{3}$  in the equation (C.1-12) and using figure C.2-2 on first quadrant only, figure C.2-4 was drawn.

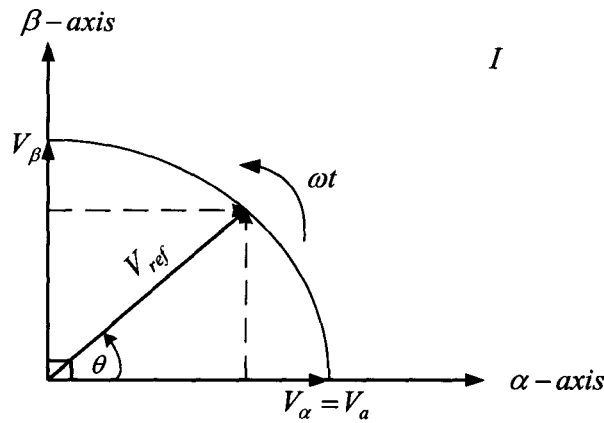


Figure C.2-4: Alpha-Beta reference frame

In figure C.2-4, the space-phasor  $V_{ref}$  was rotating at a speed of  $\omega t$ , where  $\omega=2\pi f$ ,  $f=50\text{Hz}$  and  $\theta=\omega t$ . From the literature [22], it was stated that the stator current space-phasor can be decomposed into components along two perpendicular axes (dq reference frame) that are stationary relative to the rotor.

Thus assuming that the dq reference frame was leading the  $\alpha\beta$  reference frame by  $\theta_1$  and lagging the space-phasor  $V_{ref}$  by  $\theta-\theta_1$ , figure C.2-5 was obtained.

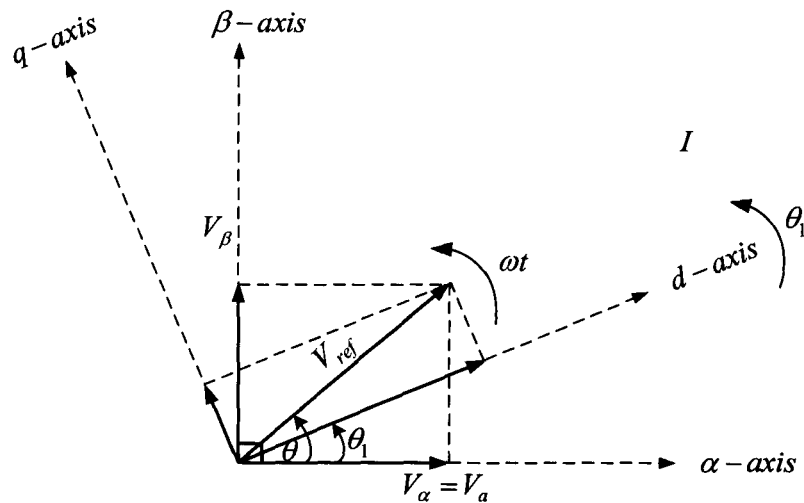


Figure C.2-5: Rotating reference frame (dq) and Stationary reference frame ( $\alpha\beta$ ).[22]

In addition, it was mentioned that dq reference frame was related with  $\alpha\beta$  reference frame by the instantaneous angle formed between the two reference planes [22]. The rotation of the space-phasor  $V_{ref}$  and the rotating reference plane (dq) was in counter-clockwise direction when observed from the stationary reference frame ( $\alpha\beta$ ).

However, when the observation was done from the (dq) reference plane,  $V_{ref}$  appears stationary and ( $\alpha\beta$ ) reference plane rotates in the clockwise direction [22]. Choosing positive direction the counterclockwise direction, thus the dq-plane is related to the  $\alpha\beta$ -plane by the following equation.

$$\text{dq-plane} = \alpha\beta\text{-plane} \times e^{-j\theta_1} \quad (\text{C.2-16})$$

Using the components projected on each reference plane from the space-phasor,  $V_{ref}$ , in figure C.2-5, equation (C.2-17) was obtained.

$$V_d + jV_q = (V_\alpha + jV_\beta) \cdot e^{-j\theta_1} \quad (\text{C.2-17})$$

Recalling from Euler definition [49],

$$e^{j\theta} = \text{Cos}\theta + j\text{Sin}\theta \quad (\text{C.2-18})$$

Therefore applying equation (C.2-18) to equation (C.2-17),

$$V_d + jV_q = (V_\alpha + jV_\beta) \cdot (\text{Cos}\theta_1 - j\text{Sin}\theta_1) \quad (\text{C.2-19})$$

Now representing the equation (C.2-19) in matrix form, equation (C.2-20) was obtained.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\theta_1 & \text{Sin}\theta_1 \\ -\text{Sin}\theta_1 & \text{Cos}\theta_1 \end{pmatrix} \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \quad (\text{C.2-20})$$

Now solving for the vector  $\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix}$  in the equation (C.2-20), equations (C.2-21) and (C.2-21) were obtained.

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \begin{pmatrix} \cos\theta_1 & \sin\theta_1 \\ -\sin\theta_1 & \cos\theta_1 \end{pmatrix}^{-1} \begin{pmatrix} V_d \\ V_q \end{pmatrix} \quad (\text{C.2-21})$$

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \begin{pmatrix} \cos\theta_1 & -\sin\theta_1 \\ \sin\theta_1 & \cos\theta_1 \end{pmatrix} \begin{pmatrix} V_d \\ V_q \end{pmatrix} \quad (\text{C.2-22})$$

Equation (C.2.22) is known as inverse Parke Transformation [22].



# APPENDIX D

## D PLL Equation Derivation

$$\begin{aligned}
 v_a &= V \cdot \sin\theta \\
 v_b &= V \cdot \sin\left(\theta - \frac{2\pi}{3}\right) \\
 v_c &= V \cdot \sin\left(\theta - \frac{4\pi}{3}\right)
 \end{aligned} \tag{D-1}$$

Arrange (D-1) in matrix form, equation (D-2) was obtained.

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = \begin{pmatrix} V \cdot \sin\theta \\ V \cdot \sin\left(\theta - \frac{2\pi}{3}\right) \\ V \cdot \sin\left(\theta - \frac{4\pi}{3}\right) \end{pmatrix} \tag{D-2}$$

Recalling equation (C-1) and substituting equation (D-2) into equation (C-1), equation (D-3) was obtained.

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{2}{3} \begin{pmatrix} v_a & -\frac{1}{2}v_b & -\frac{1}{2}v_c \\ 0 & \frac{\sqrt{3}}{2}v_b & -\frac{\sqrt{3}}{2}v_c \end{pmatrix} \tag{D-3}$$

Solving for  $V_\alpha$  and  $V_\beta$  individually, equations (D-4) and (D-5) were obtained.

$$V_\alpha = \frac{2}{3} \left( v_a - \frac{1}{2}v_b - \frac{1}{2}v_c \right) \tag{D-4}$$

$$V_\beta = \frac{2}{3} \left( \frac{\sqrt{3}}{2}v_b - \frac{\sqrt{3}}{2}v_c \right) \tag{D-5}$$

From section C.2, it was discussed that when the coefficient of the Clarke transformation is  $\frac{2}{3}$ ,  $V_\alpha$  would be equal to  $V_a$  in magnitude. Then equation (D-3) becomes equation (D-6).

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \begin{pmatrix} va \\ \frac{(vb - vc)}{\sqrt{3}} \end{pmatrix} \quad (D-6)$$

Recalling equation (C-2), the Park transformation equation and using the phase angle defined for the three-phase inverter in section 3.4.1.1, equation (D-7) was defined.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \quad (D-7)$$

Substituting (D-6) into (D-7), equation (D-8) was obtained.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} va \\ \frac{(vb - vc)}{\sqrt{3}} \end{pmatrix} \quad (D-8)$$

Expanding equation (D-8), equation (D-9) was obtained.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma \cdot va + \text{Sin}\gamma \cdot \frac{(vb - vc)}{\sqrt{3}} \\ -\text{Sin}\gamma \cdot va + \text{Cos}\gamma \cdot \frac{(vb - vc)}{\sqrt{3}} \end{pmatrix} \quad (D-9)$$

Now substitute equation (D-1) to equation (D-9), resulted in equation (D-10).

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma \cdot V \text{Sin}\theta + \frac{V}{\sqrt{3}} \text{Sin}\gamma \left( \text{Sin}\left(\theta - \frac{2\pi}{3}\right) - \text{Sin}\left(\theta - \frac{4\pi}{3}\right) \right) \\ -\text{Sin}\gamma \cdot V \text{Sin}\theta + \frac{V}{\sqrt{3}} \text{Cos}\gamma \left( \text{Sin}\left(\theta - \frac{2\pi}{3}\right) - \text{Sin}\left(\theta - \frac{4\pi}{3}\right) \right) \end{pmatrix} \quad (\text{D-10})$$

From James Stewart [49],

$$\text{Sin}(\varphi - \beta) = \text{Sin}\varphi \text{Cos}\beta - \text{Cos}\varphi \text{Sin}\beta \quad (\text{D-11})$$

Then substituting equation (D-11) to equation (D-10), and simplifying it, equations (D-12)-(D-14) were obtained.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma \cdot V \text{Sin}\theta - \frac{V}{\sqrt{3}} \text{Sin}\gamma \text{Cos}\theta \cdot \sqrt{3} \\ -\text{Sin}\gamma \cdot V \text{Sin}\theta - \frac{V}{\sqrt{3}} \text{Cos}\gamma \text{Cos}\theta \cdot \sqrt{3} \end{pmatrix} \quad (\text{D-12})$$

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = V \begin{pmatrix} \text{Cos}\gamma \text{Sin}\theta - \text{Sin}\gamma \text{Cos}\theta \\ -\text{Sin}\gamma \text{Sin}\theta - \text{Cos}\gamma \text{Cos}\theta \end{pmatrix} \quad (\text{D-13})$$

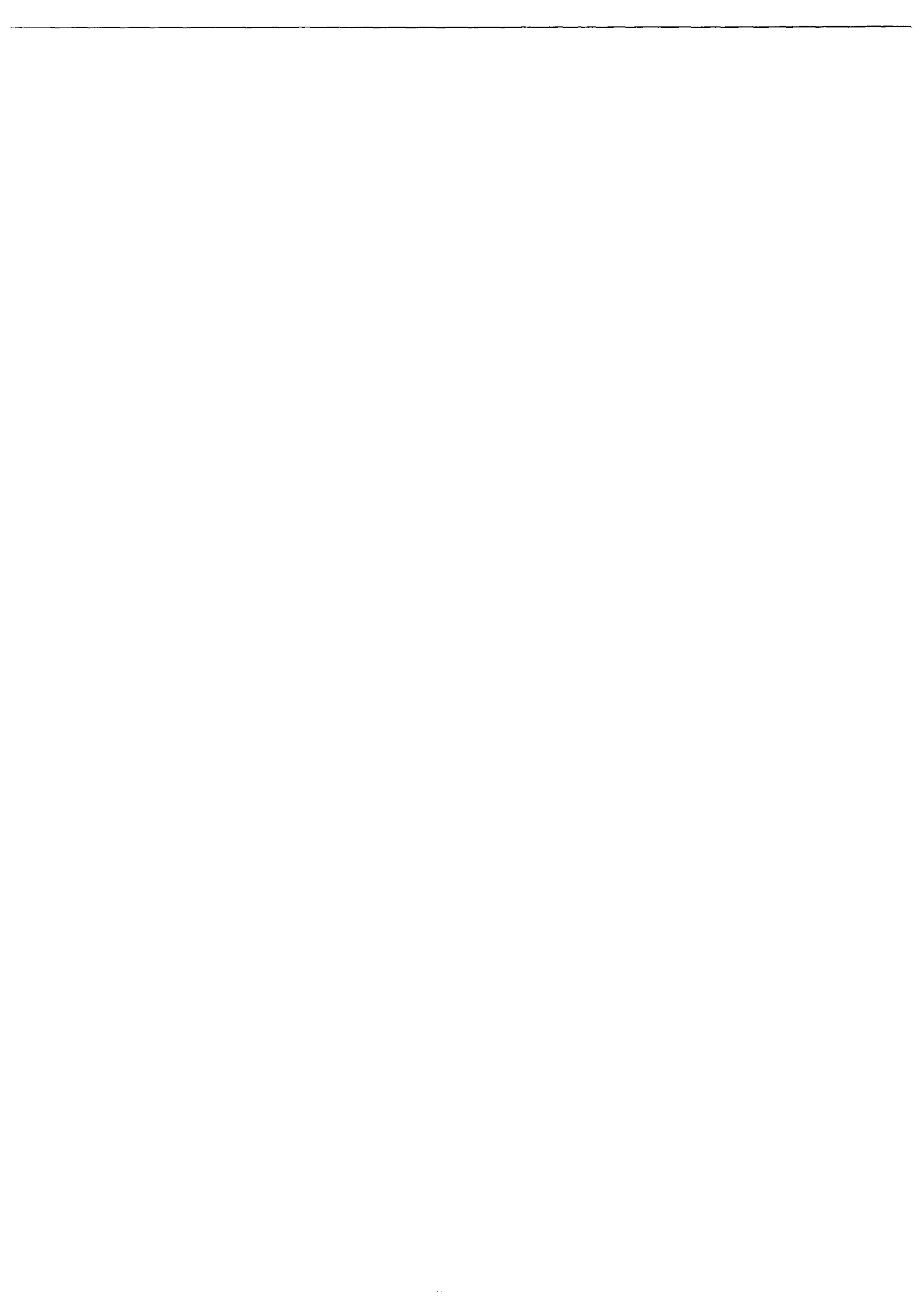
$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = -V \begin{pmatrix} \text{Sin}\gamma \text{Cos}\theta - \text{Cos}\gamma \text{Sin}\theta \\ \text{Cos}\gamma \text{Cos}\theta + \text{Sin}\gamma \text{Sin}\theta \end{pmatrix} \quad (\text{D-14})$$

Also from James Stewart [49],

$$\text{Cos}(\varphi - \beta) = \text{Cos}\varphi \text{Cos}\beta + \text{Sin}\varphi \text{Sin}\beta \quad (\text{D-15})$$

Therefore, equation (D-16) was obtained.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = -V \begin{pmatrix} \sin(\gamma - \theta) \\ \cos(\gamma - \theta) \end{pmatrix} \quad (\text{D-16})$$



# APPENDIX E

## E Current Controller Equation Derivation

As was discussed in section 3.4.2 the current controller was implemented in the rotating reference plane. In this section the full derivation of the current controller equation from the voltage drop across the filter inductor, using the Clark and Parke Transformation will be discussed.

Using figure 3.4.2-3 in section 3.4.2, the voltage drop of the phase filter inductor is illustrated in equation (E-1).

$$V_{Conv} - V_{Grid} = V_L \quad (E-1)$$

Where  $V_L$  is the inductor voltage drop,  $V_{Conv}$  is the inverter output voltage, which is applied to the low pass filter and  $V_{Grid}$  is the grid voltage.  $V_L$  is defined as illustrated in equation (E-2) [7, 12].

$$V_L = L \frac{di_L}{dt} \quad (E-2)$$

Substituting equation (E-2) into (E-1) and representing equation (E-1) for a three-phase system, equation (E-3) was obtained.

$$V_{Conv_{abc}} - V_{grid_{abc}} = L \frac{di_{L_{abc}}}{dt} \quad (E-3)$$

Recalling from appendix C, for power calculation, Clark Transformation was defined as shown in equation (E-4).

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \quad (E-4)$$

Now applying equation (E-4) to equation (E-3), equation (E-5) was obtained, which as discussed in section 3.4.1 and appendix C, it represents the signals in the stationary reference plane.

$$V_{Conv_{\alpha\beta}} - V_{grid_{\alpha\beta}} = L \frac{di_{L_{\alpha\beta}}}{dt} \quad (E-5)$$

Thereafter applying Parke Transformation in the equation (E-5), equation (E-6) was obtained. Equation (E-6) represents the signals on the rotating reference plane.

$$\begin{pmatrix} V_{Conv_d} \\ V_{Conv_q} \end{pmatrix} - \begin{pmatrix} V_{grid_d} \\ V_{grid_q} \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} L \frac{di_{L_\alpha}}{dt} \\ L \frac{di_{L_\beta}}{dt} \end{pmatrix} \quad (E-6)$$

Continuing with equation (E-6), equation (E-7) was obtained.

$$\begin{pmatrix} V_{Conv_d} \\ V_{Conv_q} \end{pmatrix} - \begin{pmatrix} V_{grid_d} \\ V_{grid_q} \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} L \frac{d}{dt} \begin{pmatrix} i_{L_\alpha} \\ i_{L_\beta} \end{pmatrix} \quad (E-7)$$

Where, the symbol  $\gamma$  as discussed in section 3.4.1 is the output of the PLL PI-based controller angle.

In equation (E-7), the vector  $\begin{pmatrix} i_{L_\alpha} \\ i_{L_\beta} \end{pmatrix}$  can be defined as expression (E-8)

$$\begin{pmatrix} i_{L_\alpha} \\ i_{L_\beta} \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma \cdot i_{L_d} - \text{Sin}\gamma \cdot i_{L_q} \\ \text{Sin}\gamma \cdot i_{L_d} + \text{Cos}\gamma \cdot i_{L_q} \end{pmatrix} \quad (E-9)$$

Where, equation (E-9) is the inverse Parke Transformation. Substituting equation (E-9) to equation (E-8), equation (E-10) was obtained.

$$\begin{pmatrix} V_{Conv_d} \\ V_{Conv_q} \end{pmatrix} - \begin{pmatrix} V_{grid_d} \\ V_{grid_q} \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} L \frac{d}{dt} \begin{pmatrix} \text{Cos}\gamma \cdot i_{L_d} - \text{Sin}\gamma \cdot i_{L_q} \\ \text{Sin}\gamma \cdot i_{L_d} + \text{Cos}\gamma \cdot i_{L_q} \end{pmatrix} \quad (\text{E-10})$$

Let:

$$A = L \frac{d}{dt} \begin{pmatrix} \text{Cos}\gamma \cdot i_{L_d} - \text{Sin}\gamma \cdot i_{L_q} \\ \text{Sin}\gamma \cdot i_{L_d} + \text{Cos}\gamma \cdot i_{L_q} \end{pmatrix} \quad (\text{E-11})$$

Equation (E.10) was redefined to equation (E.12)

$$\begin{pmatrix} V_{Conv_d} \\ V_{Conv_q} \end{pmatrix} - \begin{pmatrix} V_{grid_d} \\ V_{grid_q} \end{pmatrix} = \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \cdot A \quad (\text{E-12})$$

Now applying the derivative in equation (E-11), equation (E-13) was obtained.

$$A = L \begin{pmatrix} (-\omega \cdot \text{Sin}\gamma \cdot i_{L_d} + \text{Cos}\gamma \cdot \frac{di_{L_d}}{dt}) - (\omega \cdot \text{Cos}\gamma \cdot i_{L_q} + \text{Sin}\gamma \cdot \frac{di_{L_q}}{dt}) \\ (\omega \cdot \text{Cos}\gamma \cdot i_{L_d} + \text{Sin}\gamma \cdot \frac{di_{L_d}}{dt}) + (-\omega \cdot \text{Sin}\gamma \cdot i_{L_q} + \text{Cos}\gamma \cdot \frac{di_{L_q}}{dt}) \end{pmatrix} \quad (\text{E-13})$$

Now factorizing  $\omega$ , equation (E-14) was obtained.

$$A = L \begin{pmatrix} \omega(-\text{Sin}\gamma \cdot i_{L_d} - \text{Cos}\gamma \cdot i_{L_q}) + (\text{Cos}\gamma \cdot \frac{di_{L_d}}{dt} - \text{Sin}\gamma \cdot \frac{di_{L_q}}{dt}) \\ \omega(\text{Cos}\gamma \cdot i_{L_d} - \text{Sin}\gamma \cdot i_{L_q}) + (\text{Sin}\gamma \cdot \frac{di_{L_d}}{dt} + \text{Cos}\gamma \cdot \frac{di_{L_q}}{dt}) \end{pmatrix} \quad (\text{E-14})$$

Equation (E-14) was group in matrix form as shown in equation (E-15)

$$A = L \left( \omega \begin{pmatrix} -\text{Cos}\gamma & -\text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} i_{L_q} \\ i_{L_d} \end{pmatrix} + \begin{pmatrix} \text{Cos}\gamma & -\text{Sin}\gamma \\ \text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} \frac{di_{L_d}}{dt} \\ \frac{di_{L_q}}{dt} \end{pmatrix} \right) \quad (\text{E-15})$$

Notice that equation (E-15) is composed of a summation of two Park Transformation; in fact the second part of the summation is the inverse Park Transformation. The matrix of first part of the summation of the equation (E-15) was also set as the matrix of the second part of equation (E-15). Equation (E-16) shows this.

$$A = L \left( \omega \begin{pmatrix} \text{Cos}\gamma & -\text{Sin}\gamma \\ \text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} -i_{L_q} \\ i_{L_d} \end{pmatrix} + \begin{pmatrix} \text{Cos}\gamma & -\text{Sin}\gamma \\ \text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix} \begin{pmatrix} \frac{di_{L_d}}{dt} \\ \frac{di_{L_q}}{dt} \end{pmatrix} \right) \quad (\text{E-16})$$

Equation (E-16) can also be rewritten as shown in equation (E-17)

$$A = L \left( \omega \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix}^{-1} \begin{pmatrix} -i_{L_q} \\ i_{L_d} \end{pmatrix} + \begin{pmatrix} \text{Cos}\gamma & \text{Sin}\gamma \\ -\text{Sin}\gamma & \text{Cos}\gamma \end{pmatrix}^{-1} \begin{pmatrix} \frac{di_{L_d}}{dt} \\ \frac{di_{L_q}}{dt} \end{pmatrix} \right) \quad (\text{E-17})$$

Substituting equation (E-17) to equation (E-10) and simplifying it, equation (E-18) was obtained.

$$\begin{pmatrix} V_{\text{Conv}_d} \\ V_{\text{Conv}_q} \end{pmatrix} - \begin{pmatrix} V_{\text{grid}_d} \\ V_{\text{grid}_q} \end{pmatrix} = \omega L \begin{pmatrix} -i_{L_q} \\ i_{L_d} \end{pmatrix} + L \frac{d}{dt} \begin{pmatrix} i_{L_d} \\ i_{L_q} \end{pmatrix} \quad (\text{E-18})$$

Furthermore solving for  $V_{\text{Conv}_d}$  and  $V_{\text{Conv}_q}$  equation (E-19) was obtained.

$$V_{Conv_d} = -\omega L i_{L_q} + L \frac{d}{dt} i_{L_d} + V_{Grid_d}$$

$$V_{Conv_q} = \omega L i_{L_d} + L \frac{d}{dt} i_{L_q} + V_{Grid_q}$$

(E-19)

# APPENDIX F

## F Three-phase transformer analysis

The aim of a three-phase transformer is to step up or step down voltages so that, different power systems with different voltages values can be connected together [7]. In addition, it can be used as electrical isolator between two systems.

The three-phase transformer used in practice was a combination of three single-phase transformers, more specifically a single-phase three winding transformer of the following ratings 230/55.4, 1.5kVA.

In the sections to follow, the single-phase three-winding transformer connections will be discussed. It will focus on no-load, shorted circuit test and the construction of the three-phase transformer.

### F.1 Single-Phase three winding transformer

As was mentioned the single-phase transformer that was used had three winding, one on the primary side and two on the secondary side. The winding on the primary side voltage was rated at 230V. The two winding on the secondary side, their voltages were rated at 54V. Photo F.1-1 show this.



Photo F.1-1:Single-phase three winding transformer information plate

The single-phase transformer were made has toroidal core material. Toroidal transformers are more advantageous than the other type of transformer cores, for instance the EI core. Photo F.1-2 shows the photo of the single-phase three winding transformer used in the project.

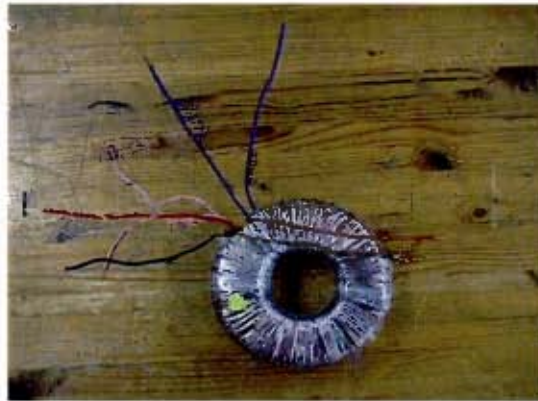


Photo F.1-2:Single-phase three winding transformer photo

From photo F.1-2 the primary side is colored as purple and the secondary side as black and red.

Figure F.1-1 below illustrates an ideal single-phase three winding transformer.

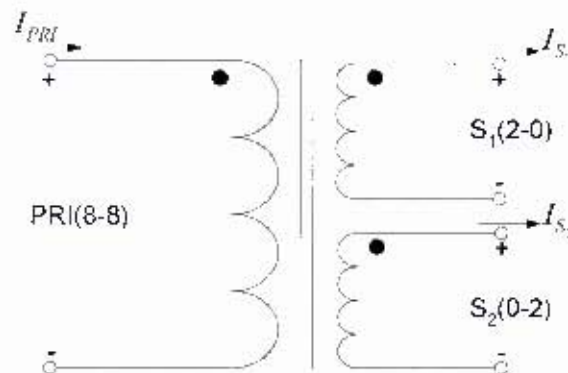


Figure F.1-1: schematic representation of the ideal single-phase three winding transformer

For a transformer to be ideal some assumptions had to be made, the assumptions given are the following [29]:

- *“The windings have zero resistance; therefore, the  $I^2R$  losses in the windings are zero.”[29]*
- *“The core permeability  $\mu_c$  is infinite, which corresponds to zero core reluctance.”[29]*
- *“There is no leakage flux; that is, the entire flux  $\Phi_c$  is confined to the core and links both windings.”[29]*
- *“There are no core losses.”[29]*

Those assumptions are important because they enable the use of Ampere and Faraday’s laws to derive the ideal transformer relationships. In the ideal single-phase two winding transformer, the Ampere’s law is defined as shown in expression (F.1-1) [29].

$$\oint H_{\text{tot}} dl = I_{\text{enclosed}} \quad (\text{F.1-1})$$

It was used to derive the relationship between the number of turns and the current through it of the primary side and secondary side. Equation (E.1-2) was obtained

$$N_1 I_1 = N_2 I_2 \quad (\text{F.1-2})$$

Faraday’s law was defined as shown in equation (F.1-3) [29].

$$e(t) = N \frac{d\phi(t)}{dt} \quad (\text{F.1-3})$$

It was used to derive the relationship between the number of turns and the voltage across it of the primary side and secondary side windings. Equation (F.1-4) shows this

$$\frac{E_1}{N_1} = \frac{E_2}{N_2} \quad (\text{F.1-4})$$

The same analysis done above for the ideal single-phase two winding transformer was done for the ideal single-phase three winding transformer, which yielded the following equations (F.1-5) and (F.1-6) [29].

$$N_1 I_1 = N_2 I_2 + N_3 I_3 \quad (\text{F.1-5})$$

$$\frac{E_1}{N_1} = \frac{E_2}{N_2} = \frac{E_3}{N_3} \quad (\text{F.1-6})$$

However, figure F.1-1 cannot be used to analyze the practical transformer illustrated in photo F.1-1.

In [29] it was mentioned that the single-phase three winding transformer can operate as single-phase two winding transformer just by leaving one of the windings open, it was also added that due to this fact, a standard No-Load and short-circuit test can be performed to evaluate the leakage impedances.

The practical transformer differs from ideal transformer in the following points [29]:

- *“The winding have resistance.”*[29]
- *“The core permeability  $\mu_c$  is finite.”*[29]
- *“The magnetic flux is not entirely confined to the core.”*[29]
- *“There are real and reactive power losses in the core.”*[29]

## **F.2 Practical single-phase three winding transformer**

In previous section the ideal single-phase three winding transformer schematic was illustrated in figure F.1-1, however it was conclude that it cannot be used to analyze the practical transformer. From reference [7, 29] the practical single-phase three winding transformer schematic was derived. figure F.2-1 illustrate this.

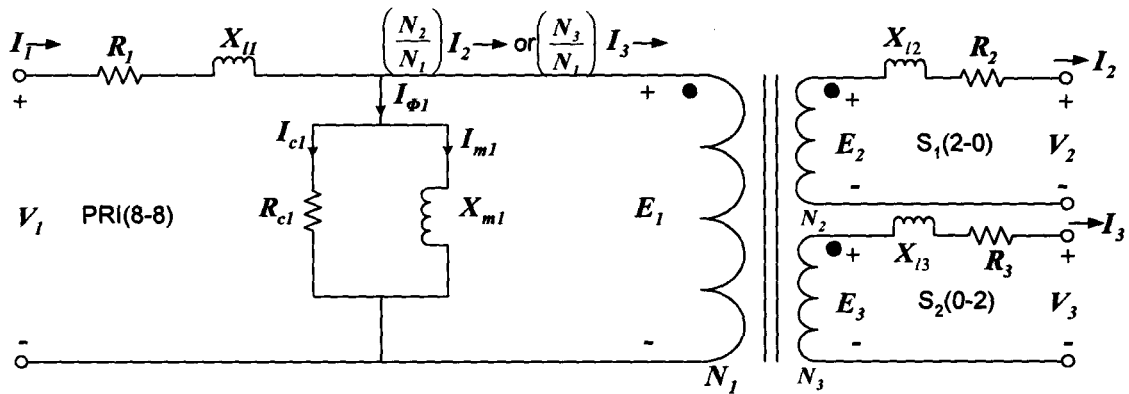


Figure F.2-1: schematic representation of the practical single-phase three winding transformer

It was also discussed that the single-phase three winding transformer can be used as single-phase two winding transformer, this can also be proved mathematically by using equation (F.1-5) whereby  $I_3$  is set to zero, this action yielded equation (F.1-2). Equation (F.1-6) can be represented as equation (F.1-4) by ignoring the last equality of the equation (F.1-6).

In light of the above discussion the third winding of the single-phase three winding transformer was left open. Figure F.2-2 illustrates the practical single-phase three winding transformer as a practical single-phase two winding transformer.

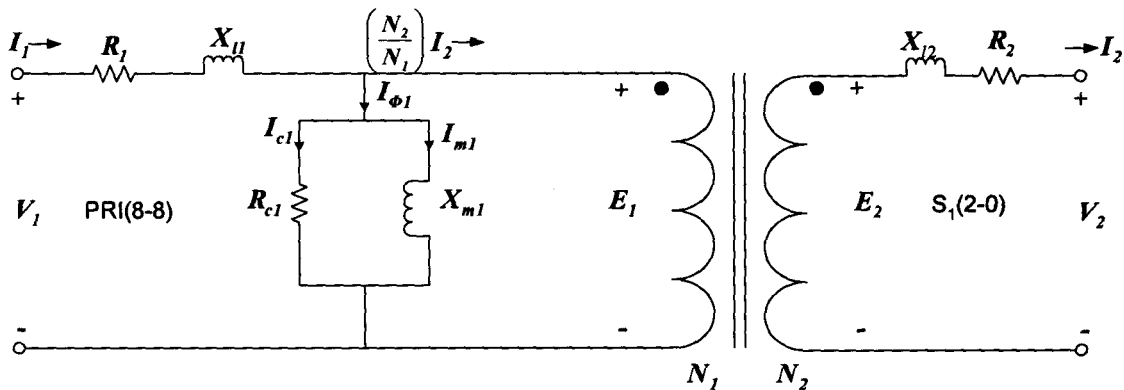


Figure F.2-2: schematic representation of the practical single-phase two winding transformer

The no-load and shorted-circuit test was performed on the single-phase three winding transformer, so that the practical resistors and inductors of figure F.2-2 could be

calculated to be used in the simulation. In the next section the no-load and shorted-circuit test for the three single-phase three windings transformers used in the practice were done.

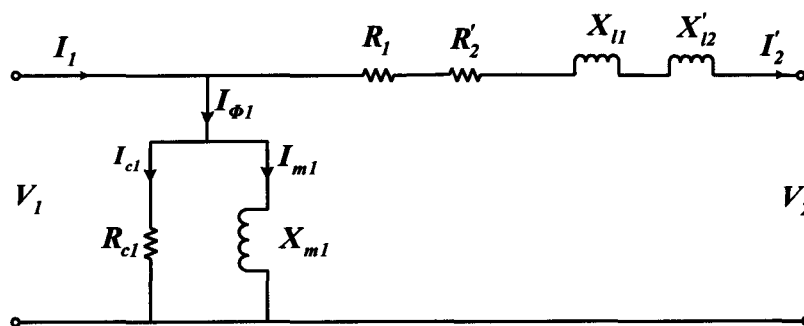
### F.3 No-Load and Shorted-circuit Test

No-load test and shorted circuit test were done in the three practical single-phase three winding transformers. Table F.3-1 shows the result.

**Table F.3-1: No-load and shorted circuit test result for the three single-phase three winding transformer**

	Transformer A		Transformer B		Transformer C	
	No-Load Test (HV open)	Short-circuit Test (LV shorted)	No-Load Test (HV open)	Short-circuit Test (LV shorted)	No-Load Test (HV open)	Short-circuit Test (LV shorted)
Voltmeter	55.4 V	11 V	55.5 V	11.22 V	55.4 V	11.4 V
Ammeter	0.4 A	6.5 A	0.233 A	6.5 A	0.338 A	6.3 A
Wattmeter	8.3 W	70.99 W	8 W	72.89 W	8.3 W	71.74 W

Using reference [7, 29], figure F.2-2 was transformed to the approximated equivalent circuit shown in figure F.3-1, to simplify the calculation of the resistors and inductors.



**Figure F.3-1: Approximate equivalent circuits**

The transformers are rated as 230/55.4V 1.5kVA as mentioned previously. The transformers turn ratio is calculated using the equation (F.1-4); its result is shown in equation (F.3-1)

$$\text{Turn ratio} = \frac{230}{55.4} = 4.152 = a \quad (\text{F.3-1})$$

In figure F.3-1 the secondary side parameters (lower side) were referred to the primary side (high side), thus equations (F.3-2), (F.3-3) and (F.3-4) were obtained.

$$V_2' = aV_2 \quad (\text{F.3-2})$$

$$R_2' = a^2 R_2 \quad (\text{F.3-3})$$

$$X_{l2}' = a^2 X_{l2} \quad (\text{F.3-4})$$

In reference [7], it was stated that when performing the No-load test, the core losses would be the same if the voltage was applied in either side of the transformer. And this is because the core losses is determined by using the maximum value of the flux in the core, which was stated to be the same whether the voltage is applied on the high side or whether the voltage is applied on the lower side. Therefore, for convenience the voltage was applied on the lower side.

For the shorted circuit test the voltage was adjust on the high side to set the rated current in the primary winding while the lower side winding was shorted.

### ***F.3.1 No-Load Test:***

As was discussed previously, for the No-load test the voltage was applied on the lower side of the single-phase three winding transformer. The No-load test result for each transformer is shown in table F.3-1. Using figure F.3-1 and reference [7] the No-load equivalent circuit is illustrated in figure F.3.1-1.

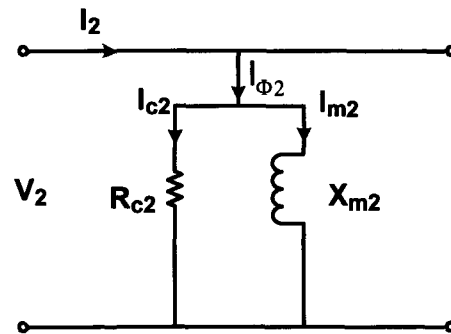


Figure F.3.1-1: No-load equivalent circuit [7]

The equations used to calculate the No-load equivalent parameters are shown below [7].

$$P_{No-Load} = \frac{V_2^2}{R_{c2}} \quad (\text{F.3.1-1})$$

$$I_2 = \sqrt{(I_{c2}^2 + I_{m2}^2)} \quad (\text{F.3.1-2})$$

$$X_{m2} = \frac{V_2}{I_{m2}} \quad (\text{F.3.1-3})$$

$$R_{c1} = a^2 \cdot R_{c2} \quad (\text{F.3.1-4})$$

$$X_{m1} = a^2 \cdot X_{m2} \quad (\text{F.3.1-5})$$

### F.3.2 Shorted-Circuit Test:

Following with the shorted circuit test, the lower side was shorted, while the high side voltage was adjusted to bring the primary current winding to its rated current value as discussed previously. Using figure F.3-1 and reference [7], the equivalent circuit of the shorted-circuit is illustrated in figure F.3.2-1.

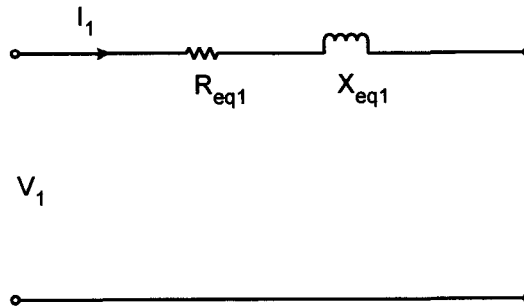


Figure F.3.2-1: Equivalent circuit derived by shorted-circuit test [7]

The equations used to calculate the shorted circuit parameters are shown below;

$$R_{eq1} = R_1 + R'_{l2} \quad (\text{F.3.2-1})$$

$$X_{eq1} = X_{l1} + X'_{l2} \quad (\text{F.3.2-2})$$

$$P_{sc} = I_1^2 R_{eq1} \quad (\text{F.3.2-3})$$

$$Z_{eq1} = \frac{V_1}{I_1} \quad (\text{F.3.2-4})$$

$$Z_{eq1} = \sqrt{(R_{eq1}^2 + X_{eq1}^2)} \quad (\text{F.3.2-5})$$

$$R_{eq2} = \frac{R_{eq1}}{a^2} \quad (\text{F.3.2-6})$$

$$X_{eq2} = \frac{X_{eq1}}{a^2} \quad (\text{F.3.2-7})$$

$$L = \frac{X}{2\pi f} \quad (\text{F.3.2-8})$$

Using table F.3-1 and the equations of No-load test and shorted-circuit test, table F.3.2-1, F.3.2-2 and F.3.2-3 illustrates the calculated results for each single-phase transformer.

**Table F.3.2-1: Practical Single-Phase Transformer A**

Result of No-Load Test				Result of Shorted-Circuit Test			
High Side		Low Side		High Side		Low Side	
$R_{c1\_A}$	$L_{m1\_A}$	$R_{c2\_A}$	$L_{m2\_A}$	$R_{eq1\_A}$	$L_{eq1\_A}$	$R_{eq2\_A}$	$L_{eq2\_A}$
[ $\Omega$ ]	[H]	[ $\Omega$ ]	[mH]	[ $\Omega$ ]	[uH]	[m $\Omega$ ]	[uH]
6405.1	8.2	371.61	475.09	1.68	640.36	97.49	37.152

**Table F.3.2-2: Practical Single-Phase Transformer B**

Result of No-Load Test				Result of Shorted-Circuit Test			
High Side		Low Side		High Side		Low Side	
$R_{c1\_B}$	$L_{m1\_B}$	$R_{c2\_B}$	$L_{m2\_B}$	$R_{eq1\_B}$	$L_{eq1\_B}$	$R_{eq2\_B}$	$L_{eq2\_B}$
[ $\Omega$ ]	[H]	[ $\Omega$ ]	[mH]	[ $\Omega$ ]	[uH]	[m $\Omega$ ]	[uH]
6612.5	16.6	385.03	963.97	1.73	177.39	100.1	10.292

**Table F.3.2-3: Practical Single-Phase Transformer C**

Result of No-Load Test				Result of Shorted-Circuit Test			
High Side		Low Side		High Side		Low Side	
$R_{c1\_C}$	$L_{m1\_C}$	$R_{c2\_C}$	$L_{m2\_C}$	$R_{eq1\_C}$	$L_{eq1\_C}$	$R_{eq2\_C}$	$L_{eq2\_C}$
[ $\Omega$ ]	[H]	[ $\Omega$ ]	[mH]	[ $\Omega$ ]	[uH]	[m $\Omega$ ]	[uH]
6401.3	10.0	371.39	581.42	1.81	271.79	104.87	15.77

Tables F.3.2-1 to F.3.2-3 results illustrates the values of the respective single-phase equivalent circuit. The equivalent circuit calculated parameters for each transformer were used in the simulation. Next section will discuss simpler single-phase transformer implementation.

#### **F.4 Implementation of the practical single-phase transformer parameter into simplorer single-phase transformer**

Figure 4.4.1-2 in section 4.4.1, as discussed previously represents the model of practical linear single-phase transformer provided by simplorer. For it to operate as close to the practical transformer in practice, it requires that all the parameters input as describe in figure 4.4.1-2 or figure 4.4.1-3 in section 4.4.1 be inputted correctly.

However the no-load and short –circuit test parameters values were calculated using the approximated equivalent circuit, figure F.3-1. This method results in an equivalent resistor and reactance referred to only one side of the single-phase transformer. In this way, it cannot be implemented in simplorer model.

In reference [7] was discussed that in well-designed transformer  $R_2' = a^2 R_2 = R_1$  and  $X_{l2}' = a^2 X_{l2} = X_{l1}$ . Therefore assuming that each single-phase transformer was well designed, equations (F.4-1) and (F.4-2) were used.

$$a^2 R_2 = R_1 = \frac{R_{eq1}}{2} \quad (F.4-1)$$

$$a^2 X_{l2} = X_{l1} = \frac{X_{eq1}}{2} \quad (F.4-2)$$

Using table F.3.2-1 to F.3.2-3 and using equations (F.4-1) and (F.4-2), the winding resistances and leakage inductance for each of the single-phase transformer in the primary as well as in secondary were calculated. Table F.4-1 shows this.

Table F.4-1: winding resistance and inductance for the three single-phase transformers

Primary side						Secondary side					
A	B	C	A	B	C	A	B	C	A	B	C
R1	R1	R1	L1	L1	L1	R2	R2	R2	L2	L2	L2
[mΩ]	[mΩ]	[mΩ]	[μH]	[μH]	[μH]	[mΩ]	[mΩ]	[mΩ]	[μH]	[μH]	[μH]
840	865	905	320.2	88.7	135.9	48.8	50.3	52.6	18.6	5.2	7.9

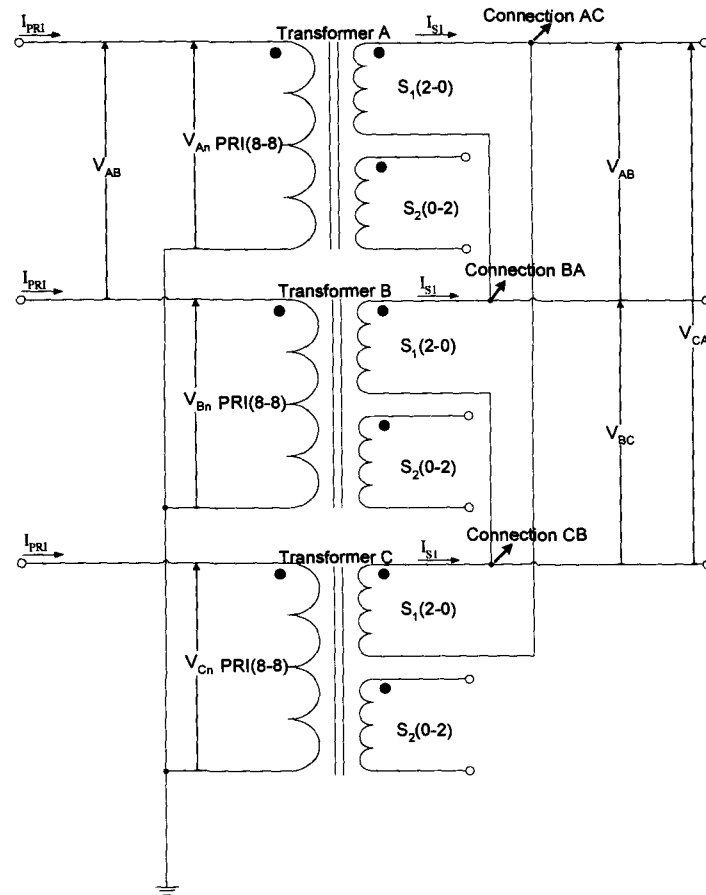
Therefore, tables F.3.2-1 to F.3.2-3 and table F.4-1 were used to implement the single-phase transformer in simulation.

The next section will discuss the assembly of the three-phase transformer from the single-phase three windings transformer.

### ***F.5 Construction of the three-phase Transformer from the single-phase transformers***

The three-phase transformer was chosen to be connected as Y-Δ. The Δ-connected side of the three-phase transformer was the side connected with the AC side of the three-phase inverter, which was the lower side of the three-phase transformer. The Y-connected side was the side connected with three-phase grid, with neutral point.

Figure F.5-1 illustrates the three-phase transformer Y-Δ connection using three single-phase transformers



**Figure F.5-1: Y-Δ three-phase transformer connections**

From [7, 29] it was mentioned that in the Y-Δ or Δ-Y three-phase transformer, the corresponded primary and secondary line to line voltages are phase shifted by  $30^\circ$ , however the corresponded primary and secondary phase voltages are in phase.

# APPENDIX G

## G Simplorer Block functions

### G.1 Initial conditions block

```

INTERN EQU {
w:=2*pi*50 ;
p:=0;           // active power variable control for the power calculator
q:=0;           // reactive power variable control for the power calculator
switch:=0;      //this variable was set to zero to keep the synchronize
                 switch open until the phase are synchronized
KI_PLL:=1736.111111 ; // PLL integral gain
KP_PLL:=92.11 ;     //PLL proportional gain
Thresh_new:=20900 ; // initial threshold point
Thresh_dumy:=Thresh_new ; // threshold variable to be manipulated in the code.
S_conv_dumy:=0 ;    // apparent power variable control to be manipulated in the
                   code
turn_ratio:=4.151624549 ; // three-phase transformer turn ratio.
}

```

### G.2 Three-Phase Grid Equation Block

In the three-phase grid supply side, the only measured signals were the currents in phase “a” and “b”, which were used to calculate  $I_{\alpha\_S}$  and  $I_{\beta\_S}$  by using equation (4.8-2). However, the three-phase grid supply phase angle (*Angle\_Source*),  $V_{\alpha\_source\_Calculated}$  and  $V_{\beta\_source\_Calculated}$  were calculated from the lower side of the three-phase transformer measurements.

In lower side of the three-phase transformer the line to line voltage  $V_{AC\_TfSec.V}$  and  $V_{BC\_TfSec.V}$  were measured and  $V_{\alpha\_TfSec}$  and  $V_{\beta\_TfSec}$  were calculated by using equation (4.8-1), and  $\theta_{TfSec}$  was calculated by using equation (3.4.1.1-2), see

code section G.3. Knowing the fact that the line-to-line voltage of the Y-part of the three-phase transformer leads the corresponded  $\Delta$ -part by  $30^\circ$  as discussed previously, thus  $30^\circ$  was added to  $theta\_TfSec$  to produce the  $Angle\_Source$  of the Y-part of the three-phase Y- $\Delta$  transformer.

Moreover  $\sqrt{3}$  was multiplied to a constant value of 230, which represent the grid rms line to neutral voltage. This action resulted in a value, which in the internal equation was defined as  $Amp\_S$ , which was equivalent to the amplitude of  $V_\alpha$  or  $V_\beta$  when the Clarke transformation had as coefficient  $\sqrt{\frac{2}{3}}$ .

The calculated angle of the three-phase grid,  $Angle\_Source$ , was used in a sine and a cosine function having as amplitude the calculated  $Amp\_S$ . It resulted obviously to two sinusoidal signals orthogonal to each other, due to fact that cosine and sine signal are phase sifted by 90 degree. This result was very good because it was as if  $V_\alpha$  and  $V_\beta$  were calculated. Comparing the calculated waveform with the  $V_\alpha$  and  $V_\beta$ , calculated by using equation (4.8-1) and the two input line to line signal discussed above, it was noticed that  $V_\alpha$  was equal to  $Amp\_S \cos(Angle\_Source)$  and  $V_\beta$  was equal to  $Amp\_S \sin(Angle\_Source)$ . Therefore  $Amp\_S \cos(Angle\_Source)$  was used as the grid voltage alpha and  $Amp\_S \sin(Angle\_Source)$  as grid voltage beta

For the purposed of PLS, the apparent three-phase grid power,  $S\_Source$ , was calculated by using equation (2.3.1-1). The three-phase grid real power,  $P\_Source$  and the three-phase reactive power,  $Q\_Source$ , used to calculate  $S\_Source$ , were calculated by using equation (C.3-4), which used as input  $V\_alpha\_TfSec$ ,  $V\_beta\_TfSec$ ,  $I\_alpha\_S$  and  $I\_beta\_S$ .

The internal equations below illustrate the above description.

```
INTERN EQU {
Amp_S:=55.4*turn_ratio*sqrt(3); // Calculating the amplitude voltage of grid Valpha
```

```

                                and Vbeta
Angle_Source:=theta_TfSec +rad(30) ; // Calculation of high side grid phase angle from
                                the calculated lower side phase angle of the
                                three-phase transformer.
sin_source:=sin(Angle_Source) ; // calculating the sine of the grid Angle_Source
                                once in the code to be used elsewhere in the code.
cos_source:=cos(Angle_Source) ; //calculating the cosine of the grid Angle_Source
                                once in the code to be used elsewhere in the code.
Valpha_source_Calculated:=Amp_S*cos_source ;
Vbeta_source_Calculated:=Amp_S*sin_source ;
V_d_Source:=Valpha_source_Calculated*cos_source+Vbeta_source_Calculated*sin_sou
rce;
V_q_Source:=-Valpha_source_Calculated*sin_source+Vbeta_source_Calculated*
cos_source;
I_alpha_S:=sqrt(3/2)*I_Source_A.I;
I_beta_S:=sqrt(3/2)*(sqrt(1/3)*I_Source_A.I+sqrt(4/3)*I_Source_B.I);
I_d_S:=I_alpha_S*cos_source+I_beta_S*sin_source;
I_q_S:=-I_alpha_S*sin_source+I_beta_S*cos_source;
P_Source:=Valpha_source*I_alpha_S+Vbeta_source*I_beta_S;
Q_Source:=-Vbeta_source*I_alpha_S+Valpha_source*I_beta_S;
PF:=cos((pi*deg(atan(Q_Source/P_Source)))/180);
S_Source:=sqrt(P_Source^2+Q_Source^2);
}

```

### **G.3 Three-phase load equation block**

In the practical experiment, due to the limited numbers of the ADC input, no measurements were done for the three-phase load current signals to be used in the DSP chip as discussed previously. However to accomplish the purposed peak load shaving in simulation, the apparent power of the three-phase load had to be used. Thus to calculate the three-phase load apparent power, the load current and voltage alpha and beta had to be known, so that as discussed before, equation (C.3-4), could be used to calculate the

three-phase load real and reactive power, and hence by using equation (2.3.1-1) discussed in section 2.3.1, the three-phase load apparent power would be calculated.

To accomplish what was discussed in previous paragraph without sensing the signals at the load side, a little trick was done in simulation to calculate the load current values alpha and beta. The trick was done as follow, knowing that the three-phase grid supply line currents, the three-phase load line currents and the three-phase inverter output line currents in the high side of the three-phase transformer, met in a node point, see figure 4.7-1, then the Kirchoff's current Law (KCL) could be applied.

The KCL states that, “at any node of a circuit, at every instant of time, the sum of the currents into the node is equal to the sum of the currents out of the node” [50]. The direction flow of the grid, load and inverter current were illustrated in figure 3.3-1.

Therefore applying the KCL to the three-phase grid supply current alpha and beta, as well as to the three-phase inverter output current alpha and beta of the high side of the three-phase transformer, when the three-phase inverter was in the charge mode, equations (G.3-1) and (G.3-2) were obtained for the three-phase load current alpha and beta.

$$I_{Load\_alpha} = I_{grid\_alpha} - I_{Inv\_alpha} \quad (G.3-1)$$

$$I_{Load\_beta} = I_{grid\_beta} - I_{Inv\_beta} \quad (G.3-2)$$

In addition, when it was in the discharge mode, equations (G.3-3) and (G.3-4) were obtained.

$$I_{Load\_alpha} = I_{grid\_alpha} + I_{Inv\_alpha} \quad (G.3-3)$$

$$I_{Load\_beta} = I_{grid\_beta} + I_{Inv\_beta} \quad (G.3-4)$$

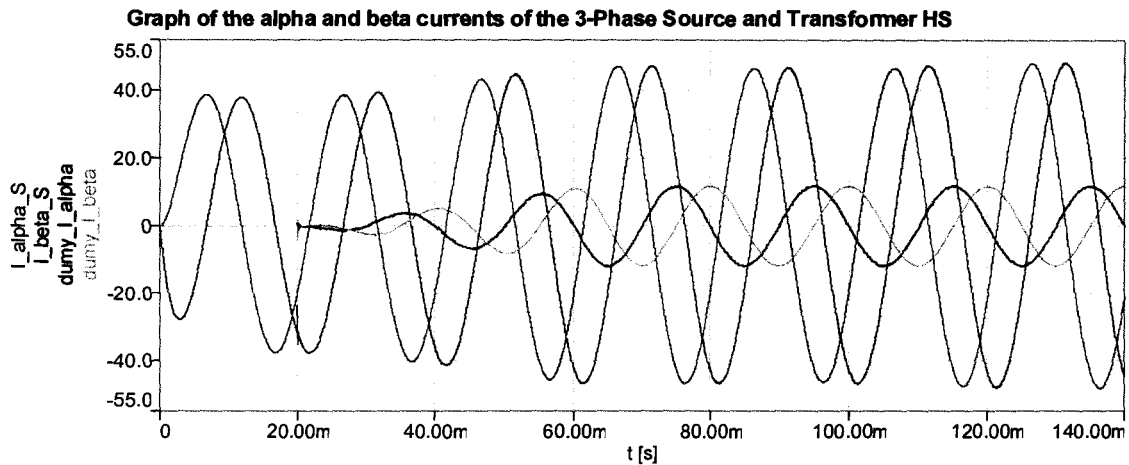
Note that the three-phase inverter currents measurements were done only in the lower side of the three-phase transformer, therefore its alpha and beta values could not be used

to calculate the three-phase load current alpha and beta as discussed in above paragraphs. This was because of the nature of the three-phase Y- $\Delta$  transformer in term of its phase angle relation between the primary and secondary corresponded line-to-line voltages as discussed previously.

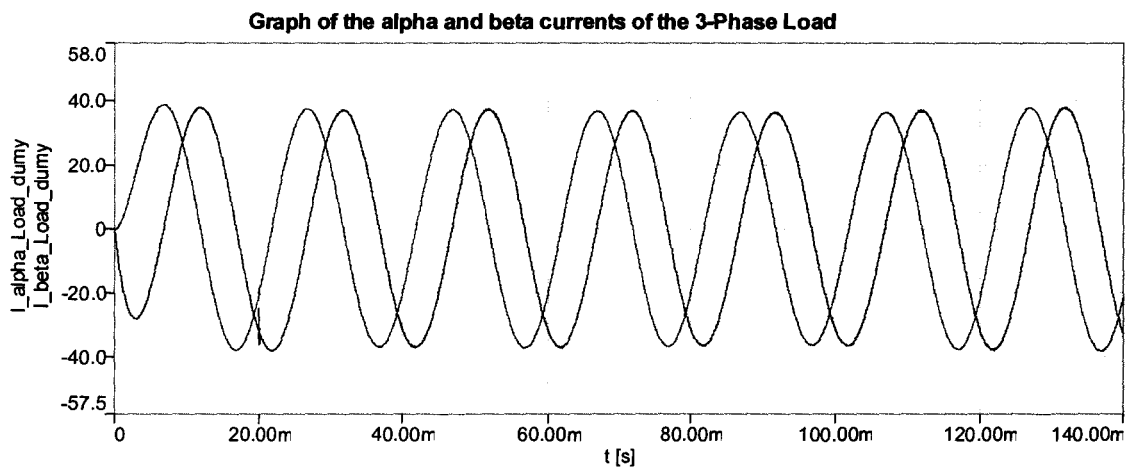
In addition, similarly to the voltage phase angle calculation as discussed in section G.2, the phase angle of the three-phase transformer line current in the lower side was calculated using equation (3.4.1.1-2). The difference between the voltage phase angle and the current phase angle in the lower side of the three-phase transformer is the PF phase angle, which has the same value in the high side of the three-phase transformer [29]. This means that the current phase angle in the lower side of the three-phase transformer would be phase sifted by  $30^\circ$  when it is observed from the high side.

To calculate the amplitude of the alpha and beta current in the high side of the three-phase transformer two steps were taken: firstly the magnitude of the three-phase transformer alpha and beta line current in the lower side was calculated using Pythagorean equation (2.3.1-1), however, having as input the alpha and beta line current. Lastly the magnitude of the alpha and beta line current in the high side of the three-phase transformer was calculated by dividing it by the three-phase transformer turn ratio and  $\sqrt{3}$  [7].

Figure G.3-1 and G.3-2 illustrates the result of equations (G.3-1) and (G.3-2) when the three-phase inverter is in the charge mode.



**Figure G.3-1: Three-phase grid supply current alpha and beta and three-phase inverter current alpha and beta**



**Figure G.3-2: Calculated three-phase load current alpha and beta**

```

INTERN EQU {
dummy_I_alpha:=(I_Amp/(turn_ratio*sqrt(3))) *cos(theta_Current_LS_to_HS); //
//calculated three-phase inverter output current alpha on the
//high side of the three-phase inverter.
dummy_I_beta:=(I_Amp/(turn_ratio*sqrt(3))) *sin(theta_Current_LS_to_HS); //
//calculated three-phase inverter output current beta on the
//high side of the three-phase inverter.
IF (((I_alpha_Conv_out_HS_Calculated>0) AND (I_alpha_S<0))
OR ((I_beta_Conv_out_HS_Calculated>0) AND (I_beta_S<0))

```

```

OR ((I_alpha_Conv_out_HS_Calculated<0) AND (I_alpha_S>0))
OR ((I_beta_Conv_out_HS_Calculated<0) AND (I_beta_S>0)))
// this if statement condition
// is used to calculated the load
// current alpha and beta from
// the grid and inverter current
// alpha and beta.

{ // in this bracket the dummy alpha and beta current are negative i.e. the three-phase
inverter is in the charge mode.
I_alpha_Load_dumy:=I_alpha_S+dummy_I_alpha ;
I_beta_Load_dumy:=I_beta_S+dummy_I_beta;
}
ELSE{ // in this bracket the dummy alpha and beta current are positive i.e. the three-phase
inverter is in the discharge mode.
I_alpha_Load_dumy:=I_alpha_S+dumy_I_alpha ;
I_beta_Load_dumy:=I_beta_S+dumy_I_beta;
};
I_alpha_Load_Calculated:=I_alpha_Load_dumy ;
I_beta_Load_Calculated:=I_beta_Load_dumy ;
I_d_Load:=I_alpha_Load_Calculated*cos_source+I_beta_Load_Calculated*sin_source ;
I_q_Load:=-I_alpha_Load_Calculated*sin_source+I_beta_Load_Calculated*cos_source;
P_Load:=Valpha_source_Calculated *I_alpha_Load_Calculated
+Vbeta_source_Calculated *I_beta_Load_Calculated;
Q_Load:=-Vbeta_source_Calculated*I_alpha_Load_Calculated
+Valpha_source_Calculated *I_beta_Load_Calculated;
S_Load:=sqrt(P_Load^2+Q_Load^2);
I_Amp:=sqrt(I_d_Conv_out_LS^2+I_q_Conv_out_LS^2);
P_Load_dumy:=Valpha_source_Calculated*I_alpha_Load_dumy+Vbeta_source_Calculated*I_beta_Load_dumy;
Q_Load_dumy:=-Vbeta_source_Calculated*I_alpha_Load_dumy+

```

```

Valpha_source_Calculated*I_beta_Load_dumy;
S_Load_dumy:=sqrt(P_Load_dumy^2+Q_Load_dumy^2);}

```

#### **G.4 Three-phase inverter equation block**

```

INTERN EQU {
V_alpha_TfSec:= sqrt(2/3)*(V_AC_TfSec.V -(1/2)*V_BC_TfSec.V) ;
V_beta_TfSec:=sqrt(2/3)*(sqrt(3/4)*V_BC_TfSec.V) ;
theta_TfSec:= atan2(V_alpha_TfSec,V_beta_TfSec) ;
theta_Conv:=theta_PLL.VAL ;
sintheta:=sin(theta_Conv) ;
costheta:=cos(theta_Conv) ;
V_d_TfSec:= V_alpha_TfSec*costheta+V_beta_TfSec*sintheta ;
V_q_TfSec:= -V_alpha_TfSec*sintheta+V_beta_TfSec*costheta ;
V_alpha_Conv:= sqrt(2/3)*(V_AC_Conv.V -(1/2)*V_BC_Conv.V) ;
V_beta_Conv:=sqrt(2/3)*(sqrt(3/4)*V_BC_Conv.V) ;
V_d_Conv:= V_alpha_Conv*costheta+V_beta_Conv*sintheta ;
V_q_Conv:= -V_alpha_Conv*sintheta+V_beta_Conv*costheta ;
I_alpha_Conv_Inductor:=sqrt(3/2)*I_Inductor_A.I ;
I_beta_Conv_Inductor:=sqrt(3/2)*(sqrt(1/3)*I_Inductor_A.I +sqrt(4/3)*I_Inductor_B.I) ;
I_d_Conv_Inductor:= I_alpha_Conv_Inductor*costheta+I_beta_Conv_Inductor*sintheta;
I_q_Conv_Inductor:= -I_alpha_Conv_Inductor*sintheta+I_beta_Conv_Inductor*costheta
;
I_alpha_Conv_out_LS:=sqrt(3/2)*I_Conv_Out_A_LS.I ;
I_beta_Conv_out_LS:=sqrt(3/2)*(sqrt(1/3)*I_Conv_Out_A_LS.I
+sqrt(4/3)*I_Conv_Out_B_LS.I) ;
I_d_Conv_out_LS:= I_alpha_Conv_out_LS*costheta+I_beta_Conv_out_LS*sintheta ;
I_q_Conv_out_LS:= -I_alpha_Conv_out_LS*sintheta+I_beta_Conv_out_LS*costheta ;
I_alpha_Conv_out_HS_Actual:=sqrt(3/2)*I_Conv_Out_A_HS.I ;

```

---

```

I_beta_Conv_out_HS_Actual:=sqrt(3/2)*(sqrt(1/3)*I_Conv_Out_A_HS.I+sqrt(4/3)*I_Conv_Out_B_HS.I);
I_d_Conv_out_HS_Actual:=I_alpha_Conv_out_HS_Actual*cos_source+I_beta_Conv_out_HS_Actual*sin_source;
I_q_Conv_out_HS_Actual:=-I_alpha_Conv_out_HS_Actual*sin_source+I_beta_Conv_out_HS_Actual*cos_source;
P_Conv_LS:=V_alpha_TfSec*I_alpha_Conv_out_LS+V_beta_TfSec*I_beta_Conv_out_LS;
Q_Conv_LS:=-V_beta_TfSec*I_alpha_Conv_out_LS+V_alpha_TfSec*I_beta_Conv_out_LS;
P_Conv_HS_Actual:=Valpha_source_Calculated*I_alpha_Conv_out_HS_Actual+Vbeta_source_Calculated*I_beta_Conv_out_HS_Actual;
Q_Conv_HS_Actual:=-Vbeta_source_Calculated*I_alpha_Conv_out_HS_Actual+Valpha_source_Calculated*I_beta_Conv_out_HS_Actual;
S_Conv_HS_Actual:=sqrt(P_Conv_HS_Actual^2+Q_Conv_HS_Actual^2);
S_Conv_LS:=sqrt(P_Conv_LS^2+Q_Conv_LS^2);
theta_Current_LS_to_HS:=theta_Current_LS+angle_rad;
angle_rad:=rad(30);
PLLCos:=55.4*cos(theta_PLL.VAL);
PLLSin:=55.4*sin(theta_PLL.VAL);
theta_Current_LS:=atan2(I_alpha_Conv_out_LS,I_beta_Conv_out_LS);
theta_Current_HS_Actual:=atan2(I_alpha_Conv_out_HS_Actual,I_beta_Conv_out_HS_Actual);
Magnitude_I_LS:=sqrt(I_alpha_Conv_out_LS^2+I_beta_Conv_out_LS^2);
I_alpha_Conv_out_LS_Calculated_PhaseShifted:=Magnitude_I_LS*cos(theta_Current_LS_to_HS);
I_beta_Conv_out_LS_Calculated_PhaseShifted:=Magnitude_I_LS*sin(theta_Current_LS_to_HS);
I_alpha_Conv_out_HS_Calculated:=I_alpha_Conv_out_LS_Calculated_PhaseShifted/(turn_ratio*sqrt(3));

```

```

I_beta_Conv_out_HS_Calculated:=I_beta_Conv_out_LS_Calculated_PhaseShifted
/(turn_ratio*sqrt(3));
P_Conv_HS_Calculated:=Valpha_source_Calculated*I_alpha_Conv_out_HS_Calculated
+Vbeta_source_Calculated *I_beta_Conv_out_HS_Calculated ;
Q_Conv_HS_Calculated:=-Vbeta_source_Calculated*I_alpha_Conv_out_HS_Calculated
+Valpha_source_Calculated *I_beta_Conv_out_HS_Calculated ;
S_Conv_HS_Calculated:=sqrt( P_Conv_HS_Calculated^2+Q_Conv_HS_Calculated^2 )
;}}

```

### **G.5 SVPWM equation block**

```

INTERN EQU {
    Valpha_pwm1:= Vd_pwm.VAL *costheta-Vq_pwm.VAL *sintheta ;
    Vbeta_pwm1:= Vd_pwm.VAL *sintheta+Vq_pwm.VAL*costheta ;
    Valpha:=Valpha_pwm1 ;
    Vbeta:=Vbeta_pwm1 ;
    Vabs_alpha:=abs( Valpha ) ;

```

#### Sector Selection

```

IF( Vbeta>=0 )
{
    IF(Vbeta>=tan(rad(60))*Vabs_alpha )
    {
        sector:=2;
    }
    ELSE IF(Vbeta<tan(rad(60))*Vabs_alpha )
    {
        IF(Valpha>=0)
        {
            sector:=1;

```

```
    }
    ELSE
    {
        sector:=3;
    }
}

ELSE IF (Vbeta<0)
{
    IF(Vbeta<=-tan(rad(60))*Vabs_alpha )
    {
        sector:=5;
    }
    ELSE IF(Vbeta>-tan(rad(60))*Vabs_alpha )
    {
        IF(Valpha>=0)
        {
            sector:=6;
        }
        ELSE
        {
            sector:=4;
        }
    }
};

Period:=TRIANG1.TPERIO ;
Vdc:= V_DC.V ; ;
```

```

IF (sector=1)
{
  t1:=(Period/(2*Vdc))*(sqrt(3/2)*Valpha-sqrt(1/2)*Vbeta);
  t2:=(Period/(2*Vdc))*(sqrt(2)*Vbeta);
  IF((t1+t2)>(Period /2) )
  {
    t1new:=(t1*(Period /2) )/(t1+t2);
    t2new:=(t2*(Period /2) )/(t1+t2);
    overmod:=1;
    t1:=t1new;
    t2:=t2new;
  }
ELSE
{
  overmod:=0;
}
t0:=(Period /2)-(t1+t2);
Aref:=t0/2+t2+t1;
Bref:= t0/2+t2;
Cref:=t0/2;
}

ELSE IF (sector=2)
{
  t2:=(Period/(2*Vdc))*(sqrt(3/2)*Valpha+sqrt(1/2)*Vbeta);
  t3:=(Period/(2*Vdc))*(-sqrt(3/2)*Valpha+sqrt(1/2)*Vbeta);
  IF((t2+t3)>(Period/2) )
  {
    t2new:=(t2*(Period/2) )/(t2+t3);
    t3new:=(t3*(Period /2) )/(t2+t3);
  }
}

```

```

        overmod:=1;
        t2:=t2new;
        t3:=t3new;
    }
ELSE
    {
        overmod:=0;
    }
t0:=(Period /2)-(t2+t3);
Bref:=t0/2+t2+t3;
Aref:= t0/2+t2;
Cref:=t0/2;
}

ELSE IF (sector=3)
{
t3:=(Period/(2*Vdc))*(sqrt(2)*Vbeta);
t4:=(Period/(2*Vdc))*(-sqrt(3/2)*Valpha-sqrt(1/2)*Vbeta );
IF((t3+t4)>(Period /2) )
    {
        t3new:=(t3*(Period /2) )/(t3+t4);
        t4new:=(t4*(Period /2) )/(t3+t4);
        overmod:=1;
        t3:=t3new;
        t4:=t4new;
    }
ELSE
    {
        overmod:=0;
    }
t0:=(Period /2)-(t3+t4);

```

```

    Bref:=t0/2+t4+t3;
    Cref:= t0/2+t4;
    Aref:=t0/2;
}

```

ELSE IF (sector=4)

```

{
    t4:=(Period/(2*Vdc))*(-sqrt(3/2)*Valpha+sqrt(1/2)*Vbeta);
    t5:=(Period/(2*Vdc))*(-sqrt(2)*Vbeta);
    IF((t4+t5)>(Period /2) )
    {
        t4new:=(t4*(Period /2) )/(t4+t5);
        t5new:=(t5*(Period /2) )/(t4+t5);
        overmod:=1;
        t4:=t4new;
        t5:=t5new;
    }
    ELSE
    {
        overmod:=0;
    }
    t0:=(Period /2)-(t4+t5);
    Cref:=t0/2+t4+t5;
    Bref:= t0/2+t4;
    Aref:=t0/2;
}

```

ELSE IF (sector=5)

```

{
    t5:=(Period/(2*Vdc))*(-sqrt(3/2)*Valpha-sqrt(1/2)*Vbeta);
    t6:=(Period/(2*Vdc))*(sqrt(3/2)*Valpha-sqrt(1/2)*Vbeta);

```

```

IF((t5+t6)>(Period /2) )
{
t5new:=(t5*(Period/2) )/(t5+t6);
t6new:=(t6*(Period/2) )/(t5+t6);
overmod:=1;
t5:=t5new;
t6:=t6new;
}
ELSE
{
overmod:=0;
}
t0:=(Period /2)-(t5+t6);
Cref:=t0/2+t6+t5;
Aref:= t0/2+t6;
Bref:=t0/2;
}

ELSE IF (sector=6)
{
t6:=(Period/(2*Vdc))*(-sqrt(2)*Vbeta);
t1:=(Period/(2*Vdc))*(sqrt(3/2)*Valpha+sqrt(1/2)*Vbeta);
IF((t6+t1)>(Period /2) )
{
t6new:=(t6*(Period/2) )/(t6+t1);
t1new:=(t1*(Period/2) )/(t6+t1);
overmod:=1;
t6:=t6new;
t1:=t1new;
}
}

```

```

ELSE
  {
    overmod:=0;
  }
t0:=(Period/2)-(t6+t1);
Aref:=t0/2+t6+t1;
Cref:= t0/2+t6;
Bref:=t0/2;
} ;}

```

## **G.6 Peak shaving equations charging and discharging block**

```

INTERN EQU {
IF( t >20m)
{
  switch:=1;
  KI_dumy:=11.1111;
  KP_dumy:=7.37;
  IF(switch=1)
  {
    KP_PLL:=KP_dumy;
    KI_PLL:=KI_dumy;
  }
  S_conv:=4500;
  Angle:=-acos(PF) ;
  /*******setting the threshold line*****
  Thresh:=Thresh_dumy;
  IF( (S_Load-Thresh) >(S_Load*0.05))
  {

```

```

    Thresh_new:=S_Load-(S_Load*0.05);
    Thresh_dumy:=Thresh_new;
}
ELSE {Thresh_new:=Thresh;}

```

```

//*****charging Mode*****
IF(S_Source<Thresh_new) //if three-phase grid apparent power is below the
                        threshold line, thus start charging the battery
{
    IF(S_Source>(Thresh_new-(Thresh_new*0.02))) // check if three-phase grid
                                                apparent power is greater
                                                than 98% of the threshold
                                                point
    {
        S_conv_dumy:=S_conv_dumy+5 //decrease the flow of apparent power
                                    into the three-phase inverter.
        IF(S_conv_dumy>0){S_conv_dumy:=0;} //while the three-phase grid power
                                                is below the threshold and above
                                                98% of the threshold point, and the
                                                inverter apparent power is trying to
                                                flow in the positive direction, then
                                                hold it at zero value.
    }
}
ELSE
{
    S_conv_dumy:=S_conv_dumy-1 // increase the flow of apparent power
                                towards the three-phase inverter
    IF(S_conv_dumy<-4500){S_conv_dumy:=-4500;} //while the three-phase
                                                grid power is below the

```

98% of the threshold point  
and the inverter apparent  
power reached the maximum  
capacity, then hold it at  
maximum capacity.

```

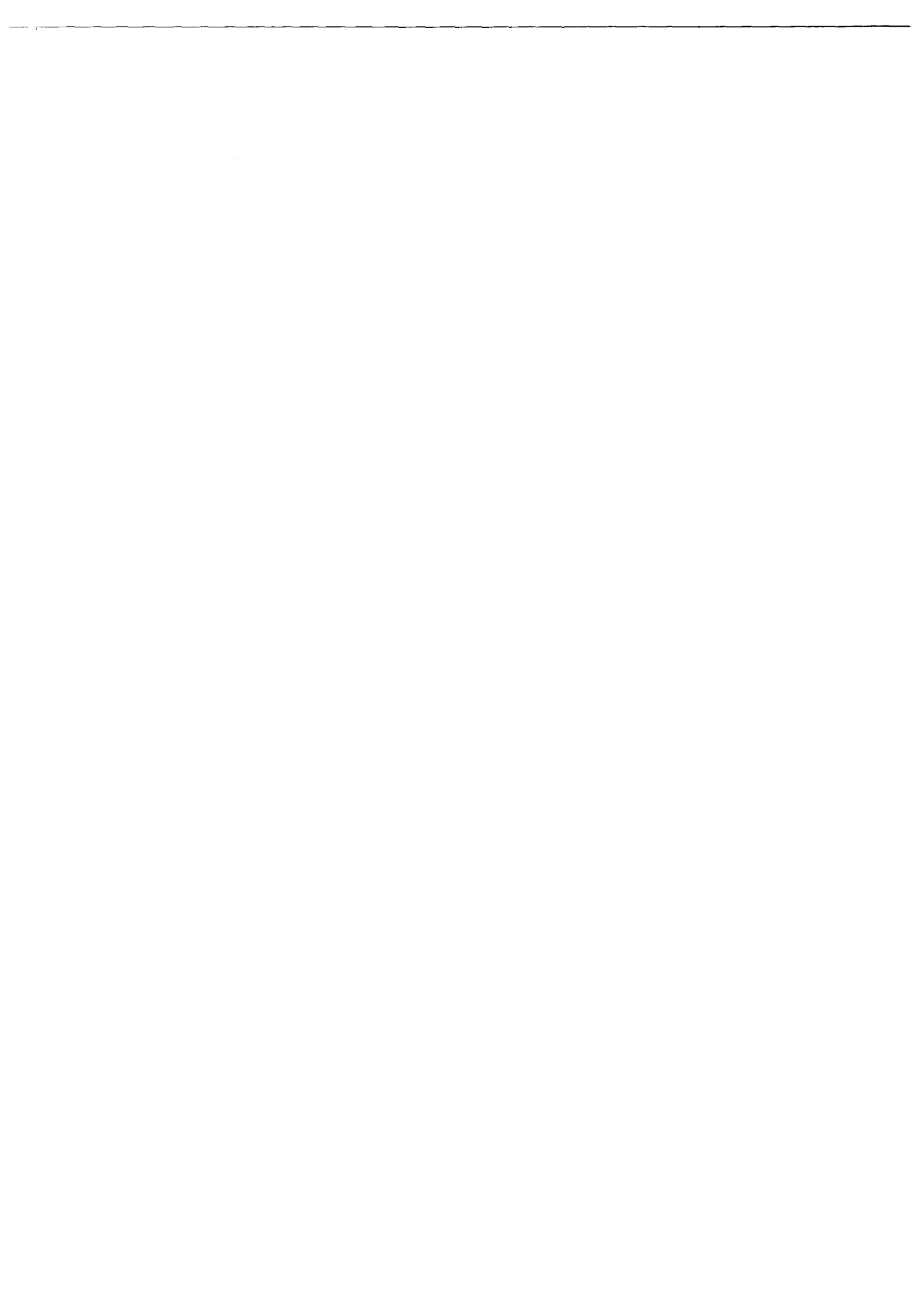
}
p:=S_conv_dumy*1; // set the total apparent power as real power, which mean
                    PF was set to unity
q:=S_conv_dumy*0; // set the reactive power to zero.
}
}
//*****Discharging Mode *****
IF(S_Load>Thresh_new) //the customer apparent load power is greater than the
                    threshold line, thus discharge the battery for peak load
                    shaving
{
S_conv_dumy:=S_Load-Thresh_new; //this is the apparent power that the
                    three-phase inverter must deliver
                    whenever the customer load is above the
                    threshold point
p:=S_conv_dumy*cos(Angle); //deliver the real power to the three-phase grid
                    depending on the three-phase grid PF.
q:=S_conv_dumy*sin(Angle); //deliver the reactive power to the three-phase grid
                    depending on the three-phase grid PF.
}
};

```



# APPENDIX H

## H Voltage Transducer LV 25-P



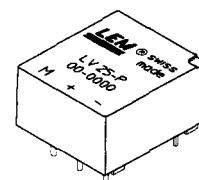
## Voltage Transducer LV 25-P

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



$$I_{PN} = 10 \text{ mA}$$

$$V_{PN} = 10 \dots 500 \text{ V}$$



### Electrical data

$I_{PN}$	Primary nominal r.m.s. current	10	mA			
$I_P$	Primary current, measuring range	0 .. $\pm 14$	mA			
$R_M$	Measuring resistance	$R_{Mmin}$	$R_{Mmax}$			
				with $\pm 12 \text{ V}$	@ $\pm 10 \text{ mA}_{max}$	30
			@ $\pm 14 \text{ mA}_{max}$	30	100	$\Omega$
		with $\pm 15 \text{ V}$	@ $\pm 10 \text{ mA}_{max}$	100	350	$\Omega$
	@ $\pm 14 \text{ mA}_{max}$	100	190	$\Omega$		
$I_{SN}$	Secondary nominal r.m.s. current	25	mA			
$K_N$	Conversion ratio	2500 : 1000				
$V_C$	Supply voltage ( $\pm 5 \%$ )	$\pm 12 \dots 15$	V			
$I_C$	Current consumption	$10 (@ \pm 15 \text{ V}) + I_S$	mA			
$V_d$	R.m.s. voltage for AC isolation test <sup>1)</sup> , 50 Hz, 1 mn	2.5	kV			

### Accuracy - Dynamic performance data

$X_G$	Overall Accuracy @ $I_{PN}, T_A = 25^\circ\text{C}$	@ $\pm 12 \dots 15 \text{ V}$	$\pm 0.9$	%
		@ $\pm 15 \text{ V} (\pm 5 \%)$	$\pm 0.8$	%
$\epsilon_L$	Linearity		< 0.2	%
$I_O$	Offset current @ $I_P = 0, T_A = 25^\circ\text{C}$		Typ	Max
$I_{OT}$	Thermal drift of $I_O$	0 $^\circ\text{C}$ .. + 25 $^\circ\text{C}$	$\pm 0.06$	$\pm 0.25$ mA
		+ 25 $^\circ\text{C}$ .. + 70 $^\circ\text{C}$	$\pm 0.10$	$\pm 0.35$ mA
$t_r$	Response time <sup>2)</sup> @ 90 % of $V_{Pmax}$		40	$\mu\text{s}$

### General data

$T_A$	Ambient operating temperature	0 .. + 70	$^\circ\text{C}$
$T_S$	Ambient storage temperature	- 25 .. + 85	$^\circ\text{C}$
$R_P$	Primary coil resistance @ $T_A = 70^\circ\text{C}$	250	$\Omega$
$R_S$	Secondary coil resistance @ $T_A = 70^\circ\text{C}$	110	$\Omega$
$m$	Mass	22	g
	Standards <sup>3)</sup>	EN 50178	

### Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

### Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor  $R$ , which is selected by the user and installed in series with the primary circuit of the transducer.

### Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

### Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

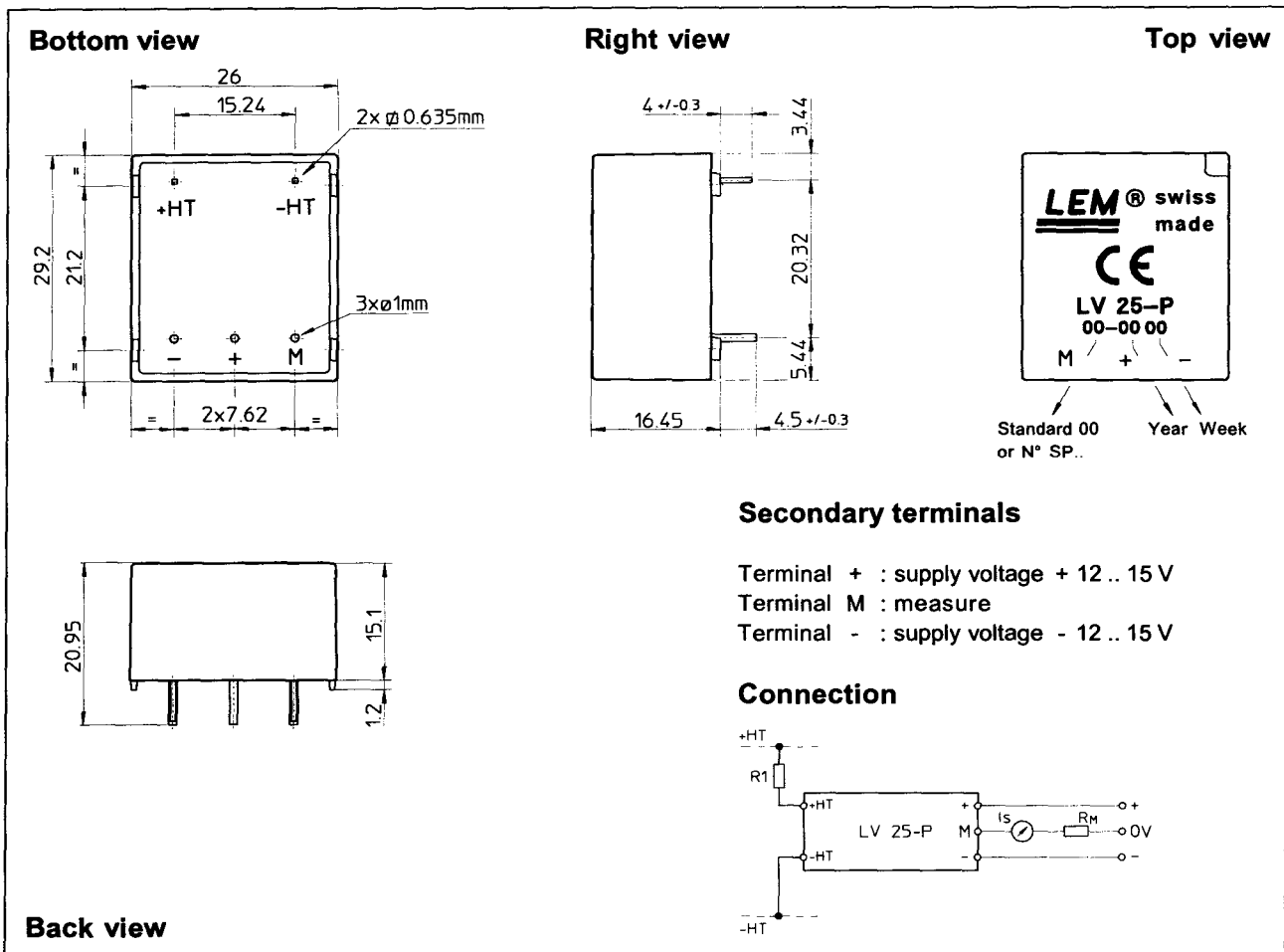
**Notes :** <sup>1)</sup> Between primary and secondary

<sup>2)</sup>  $R_1 = 25 \text{ k}\Omega$  (L/R constant, produced by the resistance and inductance of the primary circuit)

<sup>3)</sup> A list of corresponding tests is available

981125/14

## Dimensions LV 25-P (in mm. 1 mm = 0.0394 inch)



### Mechanical characteristics

- General tolerance  $\pm 0.2$  mm
- Fastening & connection of primary 2 pins  
0.635 x 0.635 mm
- Fastening & connection of secondary 3 pins  $\varnothing 1$  mm
- Recommended PCB hole 1.2 mm

### Remarks

- $I_S$  is positive when  $V_P$  is applied on terminal +HT.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

### Instructions for use of the voltage transducer model LV 25-P

Primary resistor  $R_1$  : the transducer's optimum accuracy is obtained at the nominal primary current. As far as possible,  $R_1$  should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Example: Voltage to be measured  $V_{PN} = 250$  V

a) $R_1 = 25$ k $\Omega$ / 2.5 W, $I_p = 10$ mA	Accuracy = $\pm 0.8$ % of $V_{PN}$ (@ $T_A = +25^\circ\text{C}$ )
b) $R_1 = 50$ k $\Omega$ / 1.25 W, $I_p = 5$ mA	Accuracy = $\pm 1.6$ % of $V_{PN}$ (@ $T_A = +25^\circ\text{C}$ )

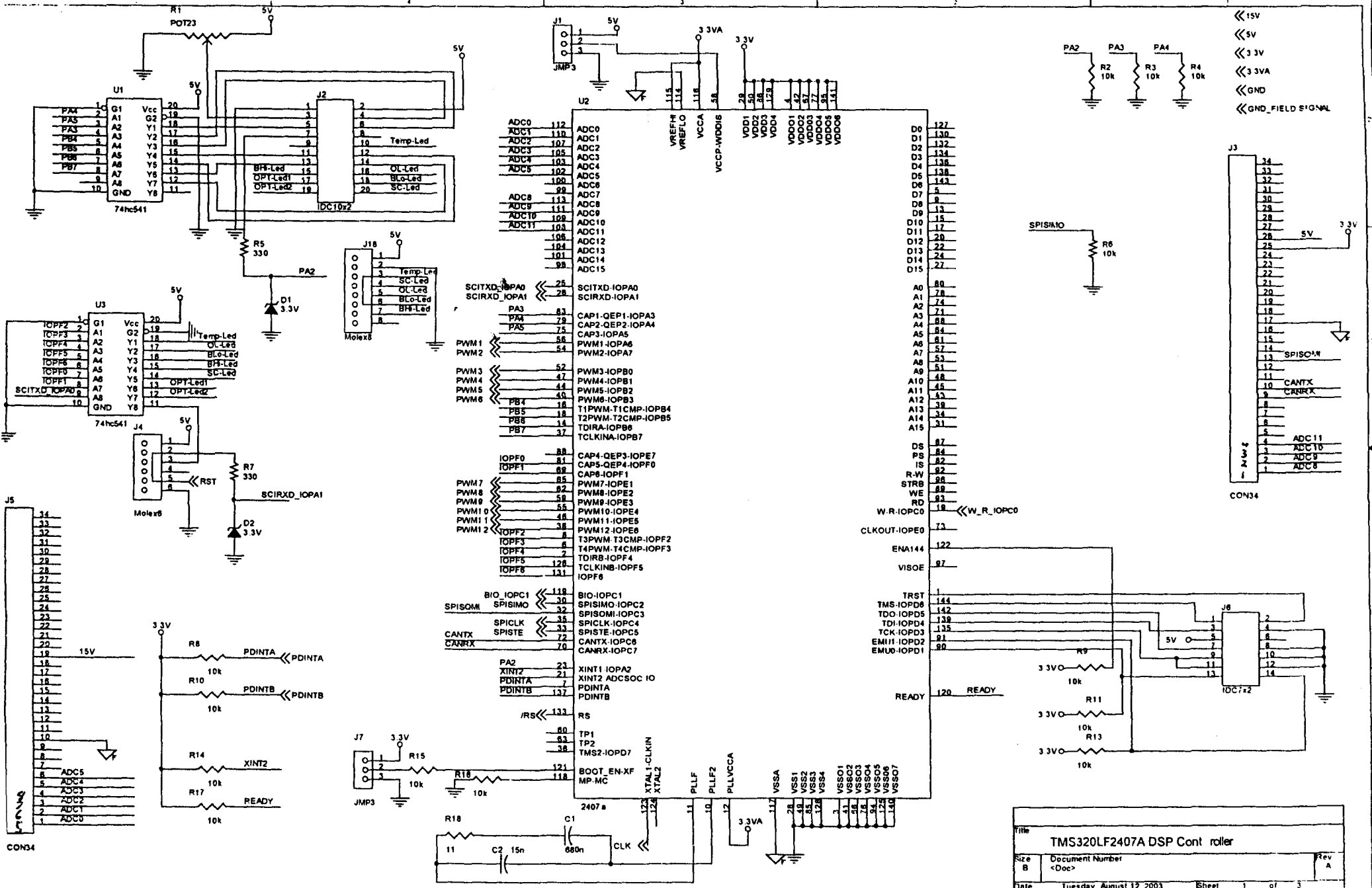
Operating range (recommended) : taking into account the resistance of the primary windings (which must remain low compared to  $R_1$  in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

LEM reserves the right to carry out modifications on its transducers, in order to improve them, without previous notice.

# APPENDIX I

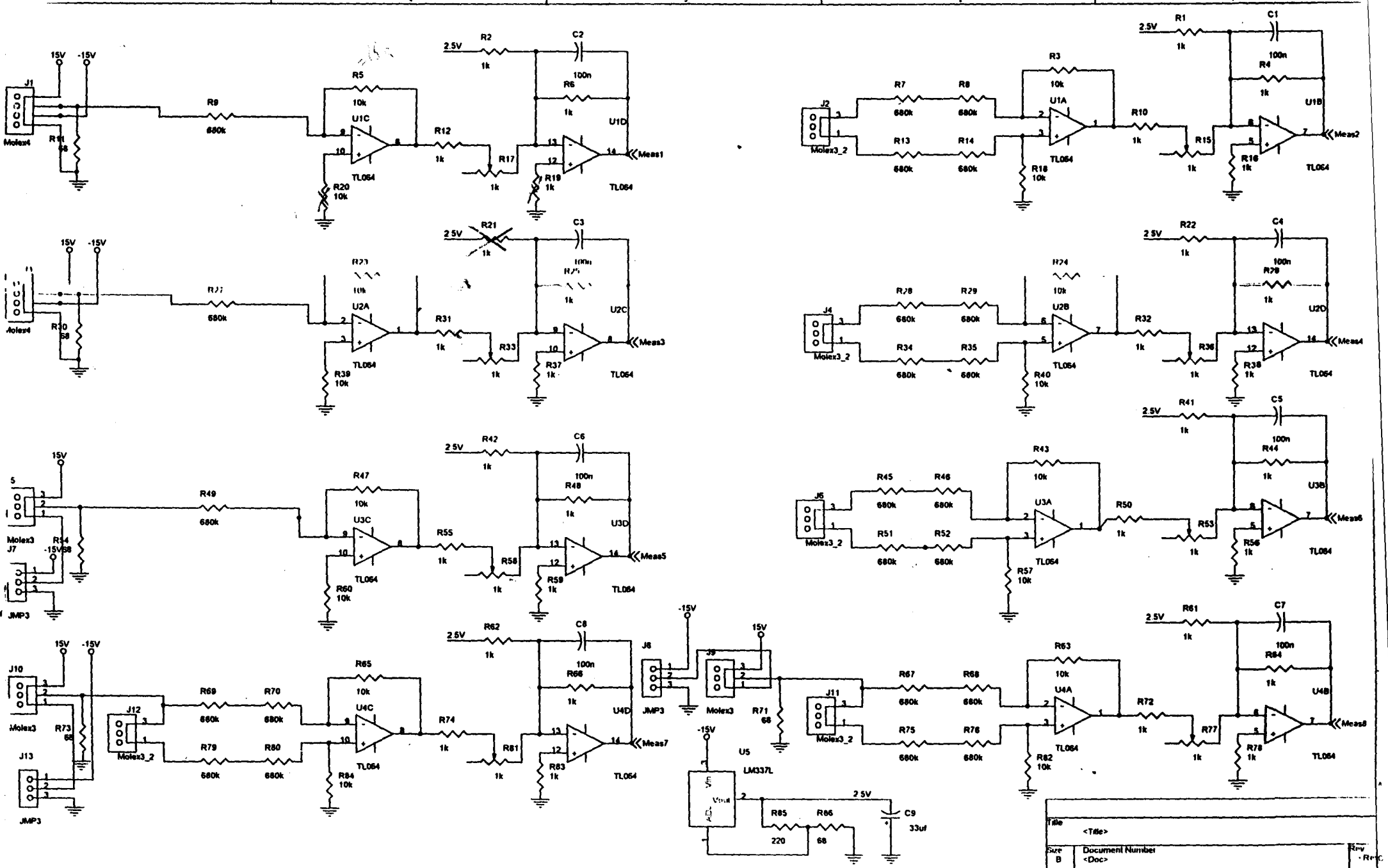
## I DSP board and interface circuit diagram





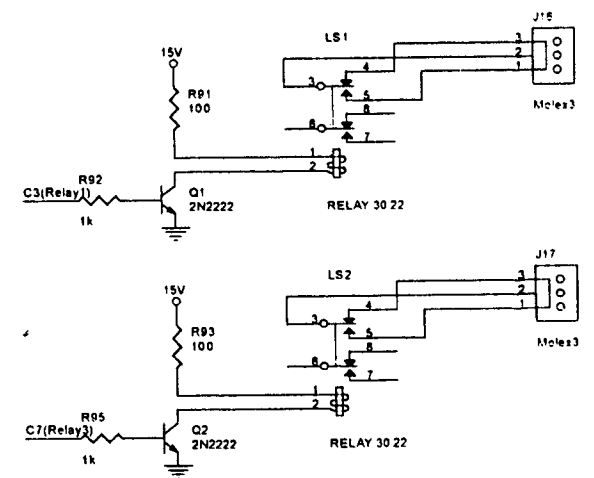
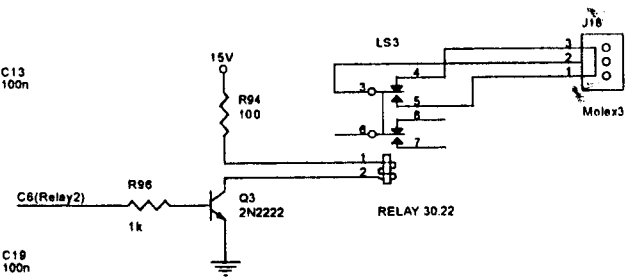
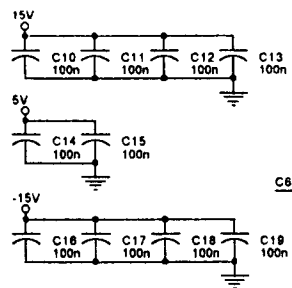
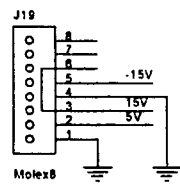
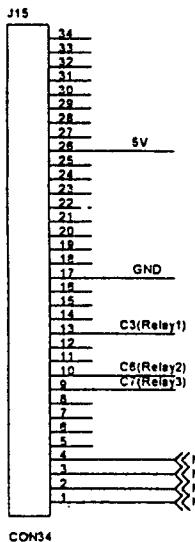
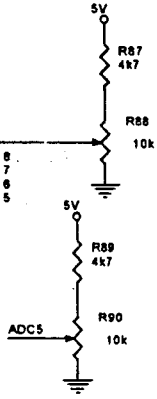
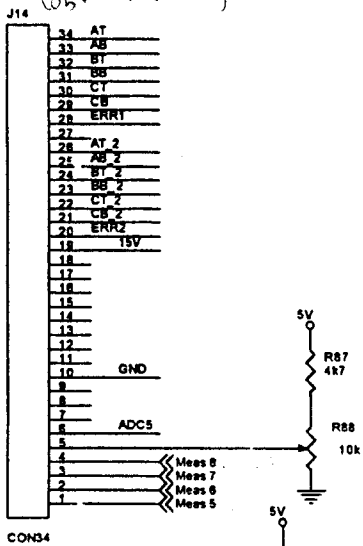
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Date	Tuesday, August 12, 2003	Sheet 1 of 3





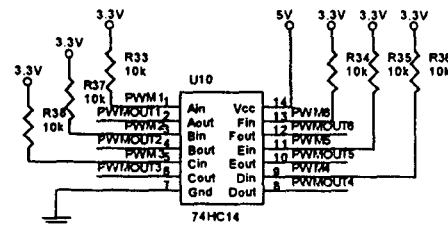
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Date	Tuesday, August 24, 2004	Sheet	1 of 2

(S5 m DSP Board)

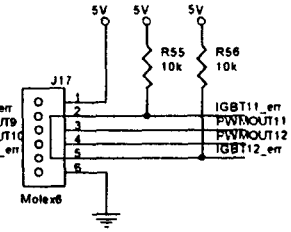
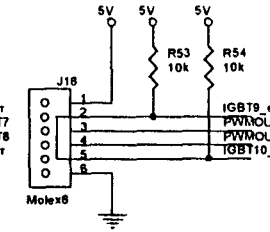
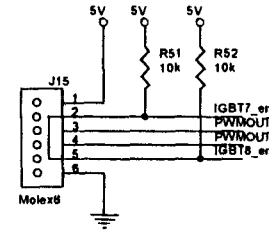
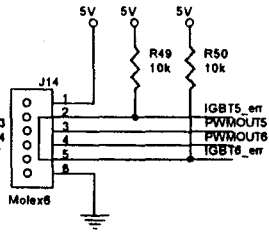
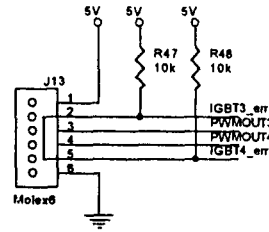
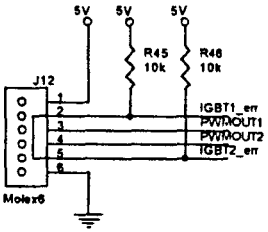
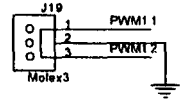
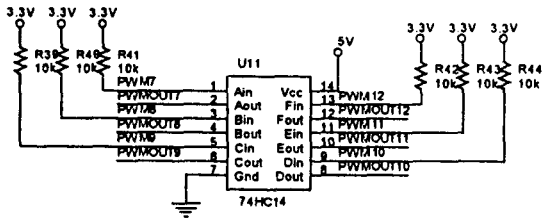


(S3 on DSP Board)

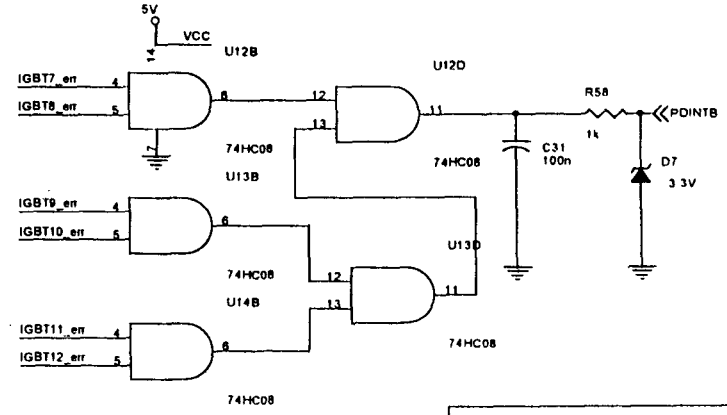
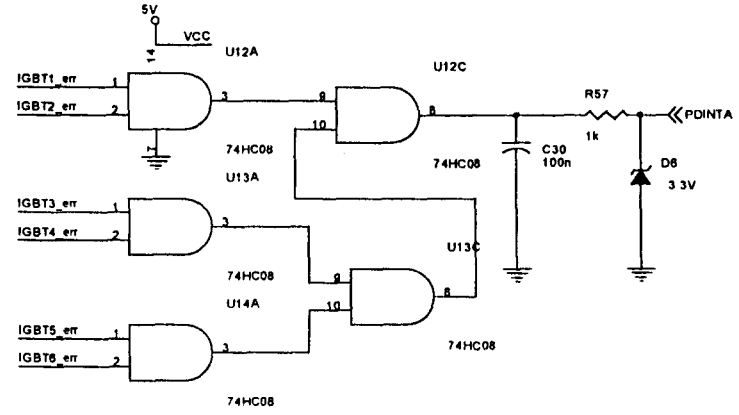
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Date	Friday, May 23, 2003
Sheet	2 of 2



- PWM1 <<< PWM7
- PWM2 <<< PWM8
- PWM3 <<< PWM9
- PWM4 <<< PWM10
- PWM5 <<< PWM11
- PWM6 <<< PWM12



- << 15V
- << 5V
- << 3.3V
- << 3.3VA
- << GND
- << GND\_FIELD SIGNAL



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Date	Tuesday, August 12, 2003 Sheet 3 of 3



# APPENDIX J

## J C-language PLL PI-based controller algorithm code



PLL\_C\_code.c

```

/*****
/* written by Antonio Conelio
/* Date: NOV 2006
/* Title: PLL PI-based control
/*
/* Comments:
/* This code implements phase-locked loop PI control
/* for a three-phase inverter.
/* the function of the controller is to produce
/* the three-phase inverter phase and synchronize with
/* the three-phase grid phase.
/* phase angle
/*
*****/

```

/\*Initialising pointers\*/

```

volatile unsigned int *COMCONA = (volatile unsigned int *) 0x7411;
volatile unsigned int *GPTCONA = (volatile unsigned int *) 0x7400;
volatile unsigned int *ACTRA = (volatile unsigned int *) 0x7413;
volatile unsigned int *DBTCONA = (volatile unsigned int *) 0x7415;

volatile unsigned int *CMPR1 = (volatile unsigned int *) 0x7417;
volatile unsigned int *CMPR2 = (volatile unsigned int *) 0x7418;
volatile unsigned int *CMPR3 = (volatile unsigned int *) 0x7419;

volatile unsigned int *T1CON = (volatile unsigned int *) 0x7404;
volatile unsigned int *T2CON = (volatile unsigned int *) 0x7408;
volatile unsigned int *T1PR = (volatile unsigned int *) 0x7403;
volatile unsigned int *T1CNT = (volatile unsigned int *) 0x7401;
volatile unsigned int *T2PR = (volatile unsigned int *) 0x7407;
volatile unsigned int *T2CNT = (volatile unsigned int *) 0x7405;

volatile unsigned int *MCRA = (volatile unsigned int *) 0x7090;
volatile unsigned int *MCRB = (volatile unsigned int *) 0x7092;
volatile unsigned int *MCRC = (volatile unsigned int *) 0x7094;
volatile unsigned int *PADATDIR = (volatile unsigned int *) 0x7098;
volatile unsigned int *PBDATDIR = (volatile unsigned int *) 0x709A;
volatile unsigned int *PCDATDIR = (volatile unsigned int *) 0x709C;
volatile unsigned int *PFDATDIR = (volatile unsigned int *) 0x7096;

volatile unsigned int *EVAIMRA = (volatile unsigned int *) 0x742C;
volatile unsigned int *IMR = (volatile unsigned int *) 0x0004;
volatile unsigned int *IFR = (volatile unsigned int *) 0x0006;
volatile unsigned int *EVAIFRA = (volatile unsigned int *) 0x742F;

volatile unsigned int *SPICCR = (volatile unsigned int *) 0x7040;
volatile unsigned int *SPICTL = (volatile unsigned int *) 0x7041;
volatile unsigned int *SPISTS = (volatile unsigned int *) 0x7042;
volatile unsigned int *SPIBRR = (volatile unsigned int *) 0x7044;
volatile unsigned int *SPIRXEMU = (volatile unsigned int *) 0x7046;
volatile unsigned int *SPIRXBUF = (volatile unsigned int *) 0x7047;
volatile unsigned int *SPITXBUF = (volatile unsigned int *) 0x7048;
volatile unsigned int *SPIDAT = (volatile unsigned int *) 0x7049;
volatile unsigned int *SPIPRI = (volatile unsigned int *) 0x704F;

volatile unsigned int *SCSR1 = (volatile unsigned int *) 0x7018;

volatile unsigned int *ADCTRL1 = (volatile unsigned int *) 0x70A0;
volatile unsigned int *ADCTRL2 = (volatile unsigned int *) 0x70A1;
volatile unsigned int *MAXCONV = (volatile unsigned int *) 0x70A2;
volatile unsigned int *CHSELSEQ1 = (volatile unsigned int *) 0x70A3;
volatile unsigned int *CHSELSEQ2 = (volatile unsigned int *) 0x70A4;
volatile unsigned int *CHSELSEQ3 = (volatile unsigned int *) 0x70A5;
volatile unsigned int *CHSELSEQ4 = (volatile unsigned int *) 0x70A6;
volatile unsigned int *AUTO_SEQ_SR = (volatile unsigned int *) 0x70A7;
volatile unsigned int *RESULT0 = (volatile unsigned int *) 0x70A8;
volatile unsigned int *RESULT1 = (volatile unsigned int *) 0x70A9;
volatile unsigned int *RESULT2 = (volatile unsigned int *) 0x70AA;
volatile unsigned int *RESULT3 = (volatile unsigned int *) 0x70AB;
volatile unsigned int *RESULT4 = (volatile unsigned int *) 0x70AC;
volatile unsigned int *RESULT5 = (volatile unsigned int *) 0x70AD;
volatile unsigned int *RESULT6 = (volatile unsigned int *) 0x70AE;

```



```

-----*/
long int Vd_grid,Vq_grid,Vd_Conv_Transf,Vq_Conv_Transf;
/*-----
-----
-----
-----*/

int
Angle,angled,angleq,sector,A,B,C,D,swfr,Aref,Bref,Cref,overmod,Valpha_dumy,Valpha_dumy
_off,vbeta_dumy,vbeta_dumy_off,thetacos,thetacos1,sintheta,costheta,sintheta1,costheta
1;
long int
angledtemp,period,temp,VdRef,VqRef,VdRefAbs,t0,t1,t2,t1new,t2new,ModIndex,samplecount,
counter,vd_inv,vq_inv;

extern int sine(); /*calling up a look up table sine function*/
extern int atan(); /*calling up a look up table arctan function*/

/*-----
-----
-----
-----*/

starting point for the interrupters
-----
-----*/

interrupt void Test1(void)
{
}

/*-----
-----
-----
-----*/

Subroutine to calculate the inverse tan of an angle.
Input to subroutine are Valpha and Vbeta.
-----
-----*/

int arctan(int Re, int Im)
{
    int y1;
    if (Re==0) Re = 1;
    if (Im==0) Im = 1;

    if ((Re>0) & (Im>0)) /* Sektor 1 */
    {
        if (Re>=Im) {y1 = atan((127*Im/Re));}
        else {y1 = 255 - atan((127*Re/Im));}
        return(y1);
    }

    if ((Im>0) & (Re<0)) /* Sektor 2 */
    {
        if (-Re>=Im) {y1 = 511 - atan(127*Im/(-Re));}
        else {y1 = 255 + atan((-127*Re)/Im);}
        return(y1);
    }

    if ((Im<0) & (Re<0)) /* Sektor 3 */
    {
        if (-Re>=-Im) {y1 = 511 + atan(127*Im/Re);}
        else {y1 = 767 - atan(127*Re/Im);}
        return(y1);
    }

    if ((Im<0) & (Re>0)) /* Sektor 4 */
    {
        if (-Im>=Re) {y1 = 767 + atan(127*Re/(-Im));}
        else {y1 = 1023 - atan((-127*Im)/Re);}
    }
}

```



```
pot2 &= 0x03FF;
```

```
DCBus = *RESULT1;
DCBus = DCBus>>6;
DCBus &= 0x03FF;
```

```
power_angle = pot2-500; /*angle between d-q and alpha-beta plane*/
```

```
ma = pot1;
```

```
/*-----
-----
-----
scaling down to zero reference to remove offset
-----
-----*/
```

```
Va = Va-512;
Vb = Vb-512;
```

```
/*-----
-----
-----
converting back to real (analogue) values
-----
-----*/
```

```
DCBusRealV = ((long int)DCBus*3904)/32768; /*Rin=12.2kohm;Ro=132ohms; Q15*/
DCBusSum = DCBusSum + DCBusRealV;
if(samplecount == 256) /* to average the DC voltage*/
{
    DCBusAvg = DCBusSum/256;
    DCBusSum = 0;
    samplecount = 0;
}
```

```
VaRealV = ((long int)Va*5600)/32768; /* 5600/32768, Q15:conversion factor from
LEM measurements */
VbRealV = ((long int)Vb*5600)/32768; /*Rin=54kohms ; Ro= 317ohms */
```

```
/*-----
-----
-----
Clarke Transform
-----
-----*/
```

```
/******Clarke Transform******/
/* vac and vbc are integer data type, to be used in the clarke transform equations
they need to be of type long, because first of all valpha and vbeta are of type
long
secondly they limitations of the value(-32767 to 32768) is overflow due to
the multiplication
with the fractions number. therefore a technique call typecasting must be
done to
temporarily change the integer to long for calculation purpose otherwise
valuable information
is lost*/
```

```
valpha= (VaRealV*13377)/16384-(VbRealV*6688)/16384; /*(13377/16384)=sqrt(2/3),
```

PLL\_C\_code.c

```
(6688/16384)=1/sqrt(6)*/  
  vbeta=(VbRealV*11585)/16384; /*14189/16384=sqrt(3)/2;9459/16384=sqrt(3)/3;  
11585/16384=sqrt(2)/2*/
```

```
/*-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----*/
```

Calculation of the grid Angle From the grid valpha and vbeta

```
/*-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----*/
```

```
/******phase angle for parke transform*****/  
valpha_dumy=(int)valpha/4;  
vbeta_dumy= (int)vbeta/4;  
  
theta = arctan(valpha_dumy,vbeta_dumy);  
  
if(theta>1023) theta=theta-1023;  
if(theta<0) theta=theta+1023;
```

```
/*-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----*/
```

Calculation of the grid Vd and Vq

```
/*-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----*/
```

```
/******parke Transform*****/  
  
sintheta1=sine(theta);/* define sine(theta) once in the code at this point*/  
thetacos1=theta+256;/*phase shift the angle theta by 90 degree */  
if(thetacos1>1023) thetacos1=thetacos1-1023;/*prevent angle to go more than  
1024, which is equivalent to 360 degree*/  
if(thetacos1<0) thetacos1=thetacos1+1023;/*prevent angle to go negative  
because the sine look up table function only accept values from 0 to 1024*/  
costheta1=sine(thetacos1);/* define cos(theta) once in the code at this  
point*/  
  
Vd_grid= (valpha*(long int)costheta1)/1024+(vbeta*(long  
int)sintheta1)/1024;/*Vd and Vq of the grid*/  
Vq_grid=- (valpha*(long int)sintheta1)/1024+(vbeta*(long int)costheta1)/1024;
```

```
/*-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----  
-----*/
```

Phase Locked Loop Controller with PI controller

```
theta_PLL_diff=Y_PLL-theta;  
if(theta_PLL_diff>1023) theta_PLL_diff=theta_PLL_diff-1023;  
if(theta_PLL_diff<0) theta_PLL_diff=theta_PLL_diff+1023;  
Fdbck_PLL= sine(theta_PLL_diff);  
  
err_k_PLL=Step_point_PLL-Fdbck_PLL;/* error calculation*/  
  
U_PLL=(int)((23580*(long int)err_k_PLL)/256+(524003*(long  
int)err_k1_PLL)/32768-(23580*(long int)err_k1_PLL)/256+(long int)U_k1_PLL);/*  
proportional and intergral in discrite*/  
/*U_PLL=(int)((30720*(long int)err_k_PLL)/1024); /*proportional only*/  
  
if(U_PLL>32766) U_PLL=32766; /*U_PLL_MAX*/  
else if(U_PLL<-32767) U_PLL=-32767; /*U_PLL_MIN*/
```

PLL\_C\_code.c

Y\_PLL=(int)((66\*(long int)U\_PLL)/32768+(long int)Y\_k1\_PLL); /\*The function represent the integral part in discrete form. Y\_PLL represents the inverter phase angle\*/

if(Y\_PLL>1023) Y\_PLL=Y\_PLL-1023;  
if(Y\_PLL<0) Y\_PLL=Y\_PLL+1023;

B\_test=sine(Y\_PLL);  
A\_test=sine(theta);

err\_k1\_PLL=err\_k\_PLL; /\*previous error\*/  
U\_k1\_PLL=U\_PLL;  
Y\_k1\_PLL=Y\_PLL;

/\*-----  
-----  
-----  
Park Transform  
-----  
-----\*/

/\*this piece of code its function is to control the inverter power angle by controlling a potentiometer\*/

if(power\_angle > 200) power\_angle = 200;  
if(power\_angle < -200) power\_angle = -200;

\*\*\*\*\*  
\*\*\*\*\*/

/\*Theta=Y\_PLL+power\_angle;\*/

Theta=Y\_PLL;

if(Theta>1023) Theta=Theta-1023;  
if(Theta<0) Theta=Theta+1023;  
sintheta=sine(Theta);

thetacos=Theta+256;  
if(thetacos>1023) thetacos=thetacos-1023;  
if(thetacos<0) thetacos=thetacos+1023;

costheta=sine(thetacos);

Vd\_Conv\_Transf= (Valpha\*(long int)costheta)/1024+(Vbeta\*(long int)sintheta)/1024;  
Vq\_Conv\_Transf=-(Valpha\*(long int)sintheta)/1024+(Vbeta\*(long int)costheta)/1024;

\*\*\*\*\*Inverse Parke Transform\*\*\*\*\*  
vd\_inv=(Vd\_Conv\_Transf\*(long int)costheta1)/1024-(Vq\_Conv\_Transf\*(long int)sintheta1)/1024;  
vq\_inv=(Vd\_Conv\_Transf\*(long int)sintheta1)/1024+(Vq\_Conv\_Transf\*(long int)costheta1)/1024;

\*\*\*\*\*  
\*\*\*\*\*/

PLL\_C\_code.c

/\*\*\*\*\* this piece of code its function is to control the magnitude of inverter voltage by controlling a potentiometer \*\*\*\*\*/

```

/*if (ma>804) ma=804;
VdRef = (ma*vd_inv)/512;
VqRef = (ma*vq_inv)/512;

```

\*\*\*\*\*  
 \*\*\*\*\*/

```

*/
VdRef = vd_inv;
VqRef = vq_inv;

```

```

/*-----
-----
-----
-----
-----
-----
-----*/

```

searching for the sectors

```

if(VdRef >= 0) A = 1;
else A = 0;
if(VqRef >= 0) B = 1;
else B = 0;

VdRefAbs = VdRef;

if(VdRef < 0) VdRefAbs = -VdRef;
if(VqRef >= ((14189*VdRefAbs)/8192)) C = 1; /* Vq=Vd*tan(60)*/
else C = 0;
if(VqRef <= (-(14189*VdRefAbs)/8192)) D = 1;
else D = 0;

if((B == 1) && (C == 0) && (A == 1)) sector = 1;
if((B == 1) && (C == 1)) sector = 2;
if((B == 1) && (C == 0) && (A == 0)) sector = 3;
if((B == 0) && (D == 0) && (A == 0)) sector = 4;
if((B == 0) && (D == 1)) sector = 5;
if((B == 0) && (D == 0) && (A == 1)) sector = 6;

```

```

/*-----
-----
-----
-----
-----
-----
-----*/

```

calculation of the Duty cycles

```

if(sector == 1)
{
t1 = ((VdRef - (591*VqRef)/1024)*swfr)/DCBusAvg;
t2 = (((591*VqRef)/512)*swfr)/DCBusAvg;
if((t1 + t2) > swfr)
{
t1new = (t1*swfr)/(t1 + t2);
t2new = (t2*swfr)/(t1 + t2);
overmod = 1;
t1 = t1new;
t2 = t2new;
}
else overmod = 0;
t0 = swfr - (t1 + t2);
Aref = t0/2 + t1 + t2;
Bref = t0/2 + t2;
Cref = t0/2;
}

if(sector == 2)
{

```

```

                                PLL_C_code.c
t1 = ((VdRef + (591*VqRef)/1024)*swfr)/DCBusAvg;
t2 = ((-VdRef + (591*VqRef)/1024)*swfr)/DCBusAvg;
if((t1 + t2) > swfr)
{
    t1new = (t1*swfr)/(t1 + t2);
    t2new = (t2*swfr)/(t1 + t2);
    overmod = 1;
    t1 = t1new;
    t2 = t2new;
}
else overmod = 0;
t0 = swfr - (t1 + t2);
Bref = t0/2 + t1 + t2;
Aref = t0/2 + t1;
Cref = t0/2;
}

if(sector == 3)
{
    t1 = (((591*VqRef)/512)*swfr)/DCBusAvg;
    t2 = ((-VdRef - (591*VqRef)/1024)*swfr)/DCBusAvg;
    if((t1 + t2) > swfr)
    {
        t1new = (t1*swfr)/(t1 + t2);
        t2new = (t2*swfr)/(t1 + t2);
        overmod = 1;
        t1 = t1new;
        t2 = t2new;
    }
    else overmod = 0;
    t0 = swfr - (t1 + t2);
    Bref = t0/2 + t1 + t2;
    Cref = t0/2 + t2;
    Aref = t0/2;
}

if(sector == 4)
{
    t1 = ((-VdRef + (591*VqRef)/1024)*swfr)/DCBusAvg;
    t2 = (((591*VqRef)/512)*swfr)/DCBusAvg;
    if((t1 + t2) > swfr)
    {
        t1new = (t1*swfr)/(t1 + t2);
        t2new = (t2*swfr)/(t1 + t2);
        overmod = 1;
        t1 = t1new;
        t2 = t2new;
    }
    else overmod = 0;
    t0 = swfr - (t1 + t2);
    Cref = t0/2 + t1 + t2;
    Bref = t0/2 + t1;
    Aref = t0/2;
}

if(sector == 5)
{
    t1 = ((-VdRef - (591*VqRef)/1024)*swfr)/DCBusAvg;
    t2 = ((VdRef - (591*VqRef)/1024)*swfr)/DCBusAvg;
    if((t1 + t2) > swfr)
    {
        t1new = (t1*swfr)/(t1 + t2);
        t2new = (t2*swfr)/(t1 + t2);
        overmod = 1;
        t1 = t1new;
        t2 = t2new;
    }
    else overmod = 0;
    t0 = swfr - (t1 + t2);
    Cref = t0/2 + t1 + t2;
    Aref = t0/2 + t2;
    Bref = t0/2;
}
}

```

PLL\_C\_code.c

```

if(sector == 6)
{
    t1 = ((- (591*VqRef)/512)*swfr)/DCBusAvg;
    t2 = ((VdRef + (591*VqRef)/1024)*swfr)/DCBusAvg;
    if((t1 + t2) > swfr)
    {
        t1new = (t1*swfr)/(t1 + t2);
        t2new = (t2*swfr)/(t1 + t2);
        overmod = 1;
        t1 = t1new;
        t2 = t2new;
    }
    else overmod = 0;
    t0 = swfr - (t1 + t2);
    Aref = t0/2 + t1 + t2;
    Cref = t0/2 + t1;
    Bref = t0/2;
}

```

```

/*-----
-----
-----
-----
-----
-----
-----
-----
-----
-----*/

```

generating switch signal

```

*CMPR1 = Aref;
*CMPR2 = Bref;
*CMPR3 = Cref;

```

```

/*-----
-----
-----
-----
-----
-----
-----
-----
-----
-----*/

```

sending data to DAC for debugging purposes

```

DAC1 = (Va/2+512)/4;
DAC1 = DAC1<<4; /*shift for bits to the left*/
DAC1 &= 0x0FFF; /*clear DAC1*/
DAC1 |= 0x0000;
*SPITXBUF = DAC1; /*store the next character to be transmitted*/
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC2 = (Vb/2+512)/4;
DAC2 = DAC2<<4;
DAC2 &= 0x0FFF;
DAC2 |= 0x2000;
*SPITXBUF = DAC2; /*store the next character to be transmitted*/
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC3 =valpha/2+62;
DAC3 = DAC3<<4;
DAC3 &= 0x0FFF;
DAC3 |= 0x4000;
*SPITXBUF = DAC3; /*store the next character to be transmitted*/
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

DAC4 =vbeta/2+62;

```

PLL\_C\_code.c

```

DAC4 = DAC4<<4;
DAC4 &= 0x0FFF;
DAC4 |= 0x6000;
*SPITXBUF = DAC4;
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

```

```

DAC5 = VaRealV/2+87;

```

```

DAC5 = DAC5<<4;
DAC5 &= 0x0FFF;
DAC5 |= 0x8000;
*SPITXBUF = DAC5;
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

```

```

DAC6 =VbRealV/2+87;
DAC6 = DAC6<<4;
DAC6 &= 0x0FFF;
DAC6 |= 0xA000;
*SPITXBUF = DAC6;
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

```

```

DAC7 = DCBusRealV;
DAC7 = DAC7<<4;
DAC7 &= 0x0FFF;
DAC7 |= 0xC000;
*SPITXBUF = DAC7;
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

```

```

DAC8 = DCBusAvg;
DAC8 = DAC8<<4; /*multiply by 2^4*/
DAC8 &= 0x0FFF;
DAC8 |= 0xE000;
*SPITXBUF = DAC8;
for (i=0; i<4; i++) {}
*PCDATDIR &= 0x0FFDF;
*PCDATDIR |= 0x0020;

```

```

if(samplecount < 30000)samplecount++;

```

```

*EVAIFRA |= 0x0200;

```

```

*PFDATDIR |= 0x0004;

```

```

}

```

```

interrupt void Test3(void)
{
}

```

```

interrupt void Test4(void)
{
}

```

```

interrupt void Test5(void)
{
}

```

```

interrupt void XINT2(void) /* ADCInterrupt, external interrupt pin in high-priority
mode */
{
}

```

PLL\_C\_code.c  
int Row)

```
int Display_Letter(int Col,  
{  
    *PADATDIR |= 0x0028;  
    *PBDATDIR = 0xFF0F + 16*Col;  
    *PADATDIR &= 0xFFDF;  
    *PADATDIR |= 0x0020;  
    *PBDATDIR = 0xFF05 + 16*Row;  
    *PADATDIR &= 0xFFDF;  
}
```

```
/*int Set_LCD_Position(int line,      int pos)  
{  
    /* Set DDRAM */  
    /*  
    *PADATDIR &= 0xFFC7;  
    *PADATDIR |= 0x0020;  
    if (line==2) *PBDATDIR = 0xFFCF;  
    else *PBDATDIR = 0xFF8F;  
  
    *PADATDIR &= 0xFFDF;  
    *PADATDIR |= 0x0020;  
    *PBDATDIR = 0xFF0F + 16*pos;  
    *PADATDIR &= 0xFFDF;  
} */
```

```
/*-----  
-----  
starting of main program  
-----  
-----*/
```

```
void main(void)  
{
```

```
/*-----  
-----  
interrupt setup  
-----  
-----*/
```

```
*MCRA |= 0x0FC0; /*I/O Mux Control Register A (MCRA), set the six PWM output
```

```
*/  
/*  
bit 15      0:      0=IOPB7,      1=TCLKINA  
bit 14      0:      0=IOPB6,      1=TDIRA  
bit 13      0:      0=IOPB5,      1=T2PWM/T2CMP  
bit 12      0:      0=IOPB4,      1=T1PWM/T1CMP  
bit 11      1:      0=IOPB3,      1=PWM6  
bit 10      1:      0=IOPB2,      1=PWM5  
bit 9       1:      0=IOPB1,      1=PWM4  
bit 8       1:      0=IOPB0,      1=PWM3  
bit 7       1:      0=IOPA7,      1=PWM2  
bit 6       1:      0=IOPA6,      1=PWM1  
bit 5       0:      0=IOPA5,      1=CAP3  
bit 4       0:      0=IOPA4,      1=CAP2/QEP2  
bit 3       0:      0=IOPA3,      1=CAP1/QEP1  
bit 2       0:      0=IOPA2,      1=XINT1  
bit 1       0:      0=IOPA1,      1=SCIRXD  
bit 0       0:      0=IOPA0,      1=SCITXD  
*/
```

```
*SCSR1 = 0x00AC; /*configure the system Control and Status Registers 1*/
```

```
/*  
bit 15      0:      reserved  
bit 14      0:      CLKOUT = CPUCLK  
bit 13-12   00:     IDLE1 selected for low-power mode  
bit 11-9    000:    PLL x4 mode
```



PLL\_C\_code.c

```

the reset condition.
the next character.
bit 6          1;      CLOCK POLARITY. Shift Clock Polarity.
                    0      Data is output on rising edge and
input on falling edge.

                    1      Data is output on falling edge and
input on rising edge.
bits 5-4       00;     Reserved. Reads return zero; writes have no effect.
bits 3-0       0111;   SPI CHAR3-SPI CHAR0. Character Length Control Bits 3-0. These
four bits                               determine the number of bits to be shifted in
or out as a single character during      one shift sequence.
by the bit values.                       Table 9-3 lists the character length selected
*/

```

```
*MCRB |= 0xFE1C;
```

```

/*
bit 15        1:      0=reserved, 1=TMS2 (always write as 1)
bit 14        1:      0=reserved, 1=TMS  (always write as 1)
bit 13        1:      0=reserved, 1=TD0  (always write as 1)
bit 12        1:      0=reserved, 1=TDI  (always write as 1)
bit 11        1:      0=reserved, 1=TCK  (always write as 1)
bit 10        1:      0=reserved, 1=EMU1 (always write as 1)
bit 9         1:      0=reserved, 1=EMU0 (always write as 1)
bit 8         0:      0=IOPD0,  1=XINT2/ADCSOC
bit 7         0:      0=IOPC7,  1=CANRX
bit 6         0:      0=IOPC6,  1=CANTX
bit 5         0:      0=IOPC5,  1=SPISTE
bit 4         1:      0=IOPC4,  1=SPICLK
bit 3         1:      0=IOPC3,  1=SPISOMI
bit 2         1:      0=IOPC2,  1=SPISIMO
bit 1         0:      0=IOPC1,  1=BIO*
bit 0         0:      0=IOPC0,  1=W/R*
*/

```

```

/*SPICCR |= 0x000B; /*Serial Peripheral Interface Configuration Control
Register(SPICCR)*/

```

```

/*
bit 7          0;      SPI SW RESET. SPI Software Reset.
                    0      Initializes the SPI operating flags to
the reset condition.
                    1      SPI is ready to transmit or receive
the next character.

bit 6          0;      CLOCK POLARITY. Shift Clock Polarity.
                    0      Data is output on rising edge and
input on falling edge.

                    1      Data is output on falling edge
and input on rising edge.

bits 5-4       00;     Reserved. Reads return zero; writes have no effect.
bits 3-0       1011;   SPI CHAR3-SPI CHAR0. Character Length Control Bits 3-0. These
four bits                               determine the number of bits to be shifted in
or out as a single character during      one shift sequence.
by the bit values.                       Table 9-3 lists the character length selected
*/

```





```

PLL_C_code.c
0      Dual-sequencer mode. SEQ1 and
      8-state sequencers.
1      Cascaded mode. SEQ1 and SEQ2
      16-state sequencer (SEQ).

bit 3      0;      CAL ENA. Offset calibration enable
input channel      When set to 1, CAL ENA disables the
calibration reference      multiplexer, and connects the
to the ADC core      selected by the bits HI/LO and BRG ENA
then be started      inputs. The calibration conversion can
(STRT CAL) to 1.      by setting bit 14 of ADCTRL2 register
first before the      Note that CAL ENA should be set to 1
bit should not be      STRT CAL bit can be used. Note: This
                        set to 1 if STEST ENA = 1
                        0      Calibration mode disabled
                        1      Calibration mode enabled

bit 2      0;      BRG ENA. Bridge enable
allows a reference      Together with the HI/LO bit, BRG ENA
mode.      voltage to be converted in calibration
for reference      See the description of the HI/LO bit
calibration.0 Full reference      voltage selections during
A reference midpoint      voltage is applied to the ADC input 1
                        voltage is applied to the ADC input

bit 1      0;      HI/LO. VREFHI/VREFLO selection
enabled (STEST ENA = 1),      When the fail self-test mode is
connected. In      HI/LO defines the test voltage to be
reference source      calibration mode, HI/LO defines the
operating mode,      polarity; see Table 7-5. In normal
                        HI/LO has no effect.
                        0      VREFLO is used as precharge
                        1      VREFHI is used as precharge

bit 0      0;      STEST ENA. Self-test function enable
                        0      Self-test mode disabled
                        1      Self-test mode enabled

*/

/*ADCTRL2 = 0x0000;      /*ADC control register 2*/

/*
bit 15      0;      EVB SOC SEQ. EVB SOC enable for
cascaded sequencer      (Note: This bit is active only
in cascaded mode.)      0      No action
                        1      Setting this bit
allows the cascaded      sequencer to be
started by an Event Manager B signal.      The Event Manager can
be programmed to start a conversion      on various events. See

```







PLL\_C\_code.c

CONV2\_2 - 0 are used.  
 CONV1\_3 - 0 are used.  
 always starts with the  
 sequentially until the  
 result buffer is filled in  
 of conversions between  
 programmed for a session.  
 \*/

. For SEQ2 operation, bits MAX  
 . For SEQ operation, bits MAX  
 An autoconversion session  
 initial state and continues  
 end state if allowed. The  
 a sequential order. Any number  
 1 and (MAX CONVN +1) can be

/\* CHSELSEQ1 = 0x0001; \*/

-----  
 -----  
 registers for PWM generation  
 -----  
 -----\*/

\*MCRA |=0x0FC0;

/\*  
 bit 15 0: 0=IOPB7, 1=TCLKINA  
 bit 14 0: 0=IOPB6, 1=TDIRA  
 bit 13 0: 0=IOPB5, 1=T2PWM/T2CMP  
 bit 12 0: 0=IOPB4, 1=T1PWM/T1CMP  
 bit 11 1: 0=IOPB3, 1=PWM6  
 bit 10 1: 0=IOPB2, 1=PWM5  
 bit 9 1: 0=IOPB1, 1=PWM4  
 bit 8 1: 0=IOPB0, 1=PWM3  
 bit 7 1: 0=IOPA7, 1=PWM2  
 bit 6 1: 0=IOPA6, 1=PWM1  
 bit 5 0: 0=IOPA5, 1=CAP3  
 bit 4 0: 0=IOPA4, 1=CAP2/QEP2  
 bit 3 0: 0=IOPA3, 1=CAP1/QEP1  
 bit 2 0: 0=IOPA2, 1=XINT1  
 bit 1 0: 0=IOPA1, 1=SCIRXD  
 bit 0 0: 0=IOPA0, 1=SCITXD  
 \*/

\*ACTRA = 0x0666; /\*Compare Action Control Register A (ACTRA)\*/

/\*  
 bit 15 0; SVRDIR. Space vector PWM rotation  
 direction. Used only in space vector PWM output generation.  
 0 Positive (CCW)  
 1 Negative (CW)  
 bits 14-12 000; D2-D0. Basic space vector bits. Used only in  
 space vector PWM output generation.  
 bits 11-10 01; CMP6ACT1-0. Action on compare output pin 6,  
 CMP6.  
 00 Forced low  
 01 Active low  
 10 Active high  
 11 Forced high  
 bits 9-8 10; CMP5ACT1-0. Action on compare output pin 5,  
 CMP5.  
 00 Forced low  
 01 Active low  
 10 Active high  
 11 Forced high

PLL\_C\_code.c

```

bits 7-6          01;          CMP4ACT1-0. Action on compare output pin 4,
CMP4.
                00          Forced low
                01          Active low
                10          Active high
                11          Forced high

bits 5-4          10;          CMP3ACT1-0. Action on compare output pin 3,
CMP3.
                00          Forced low
                01          Active low
                10          Active high
                11          Forced high

bits 3-2          01;          CMP2ACT1-0. Action on compare output pin 2,
CMP2.
                00          Forced low
                01          Active low
                10          Active high
                11          Forced high

bits 1-0          10;          CMP1ACT1-0. Action on compare output pin 1,
CMP1.
                00          Forced low
                01          Active low
                10          Active high
                11          Forced high

*/
/*      *DBTCON = 0x0AE0;  */

      *DBTCONA = 0;  /*Dead-Band Timer Control Registers A(DBTCONA) no need - set
on driver board */

/*
bits 15-12        0000;      Reserved. Reads return zero; writes have no effect.

bits 11-8         0000;      DBT3 (MSB)-DBT0 (LSB). Dead-band timer period. These
bits
                        define the period value of the three
4-bit dead-band
                        timers.

bit 7             0;          EDBT3. Dead-band timer 3 enable (for pins PWM5
and PWM6
                        of Compare Unit 3).
                        0          Disable
                        1          Enable

bit 6             0;          EDBT2. Dead-band timer 2 enable (for pins PWM3
and PWM4
                        of CompareUnit 2).
                        0          Disable
                        1          Enable

bit 5             0;          EDBT1. Dead-band timer 1 enable (for pins PWM1
and PWM2
                        of Compare Unit 1).
                        0          Disable
                        1          Enable

bits 4-2          000;      DBTPS2 to DBTPS0. Dead-band timer prescaler.
                000          x/1
                001          x/2
                010          x/4
                011          x/8
                100          x/16
                101          x/32
                110          x/32
                111          x/32

frequency
x = Device (CPU) clock

```



```

bits 14-13      00;      PLL_C_code.c
underflow)      CLD1, CLD0.Compare register CMPRX reload condition.
T1PR (that is, on          00      When T1CNT = 0 (that is, on
unpredictable          01      When T1CNT = 0 or T1CNT =
                          10      underflow or period match)
                          11      Immediately
                          Reserved; result is
bit 12          0;      SVENABLE. Space vector PWM mode enable.
mode            0      Disables space vector PWM
                1      Enables space vector PWM mode
bits 11-10      00;      ACTRLD1, ACTRLD0. Action control register
reload condition.          00      When T1CNT = 0 (on underflow)
T1PR (on underflow or          01      When T1CNT = 0 or T1CNT =
period match)          10      Immediately
                          11      Reserved
bit 9          1;      FCOMPOE. Compare output enable. Active PDPINTA
clears            this bit to zero.
high-impedance state;          0      PWM output pins are in
high-impedance state;          1      PWM output pins are not in
that is, they are disabled
that is, they are enabled
bit 8          1;      PDPINTA STATUS. This bit reflects the current
status of          the PDPINTA pin.(This bit is
applicable to 240xA devices    only - it is reserved on 240x devices
and returns a zero            when read.)
bits 7-0        0000-0000;  Reserved. Read returns zero; writes have no effect.

*/

swfr = 2048;
*T1PR = swfr; /* timer period register, Period = 2048*25nsec*2 = 102usec;
freq 10kHz */

*T1CNT = 0x0; /* timer1 Counter registers:This register stores
the current value of the counter and keeps
incrementing          or decrementing depending on the direction of
counting*/

/*
*T1CON = 0x8802; /* Timer 1 control register, up/down continuous mode */
bits 15-14      10;      Free, Soft. Emulation control bits.
suspend          00      Stop immediately on emulation
complete on emulation suspend 01      Stop after current timer period is
emulation suspend 10      Operation is not affected by
emulation suspend 11      Operation is not affected by
bit 13          0;      Reserved. Reads return zero, writes have no
effect.

```

bits 12-11	01;	PLL_C_code.c TMODE1-TMODE0. Count Mode Selection. 00 Stop/Hold 01 Continuous-Up/-Down Count Mode 10 Continuous-Up Count Mode 11 Directional-Up/-Down Count Mode
bits 10-8	000;	TPS2-TPS0. 3 t, 000 x/1                    100 x/16 001 x/2                    101 x/32 010 x/4                    110 x/64 011 x/8                    111 x/128 x = device (CPU) clock
frequency		
bit 7 T2SWT1.	0;	T2SWT1. In the case of EVA, this bit is (GP timer 2 start with GP timer 1.) GP timer 1's timer enable bit. This T1CON. T4SWT3. In the case of EVB, this bit (GP timer 4 start with GP timer 3.) GP timer 3's timer enable bit. This T3CON. 0            Use own TENABLE bit 1            Use TENABLE bit of T1CON (in (in case of EVB) to enable own TENABLE bit
Start GP timer 2 with bit is reserved in is T4SWT3. Start GP timer 4 with bit is reserved in case of EVA) or T3CON and disable operation ignoring		
bit 6	0;	TENABLE. Timer enable. 0            Disable timer operation (the and the prescaler counter is 1            Enable timer operations
timer is put in hold reset)		
bits 5-4	00;	TCLKS1, TCLKS0. Clock source select. 5-4            Source 0 0            Internal 0 1            External 1 0            Reserved 1 1            QEP Circuit† (in case of Timer Reserved (in case of Timer + This option is valid only if SELT1PR
2/Timer 4) 1/Timer 3) = 0		
bits 3-2 Condition.	00;	TCLD1, TCLD0. Timer Compare Register Reload 00            when counter is 0 01            when counter value is 0 or 10            Immediately 11            Reserved
equals period register value		
bit 1 operation	1;	TECMPR. Timer compare enable. 0            Disable timer compare 1            Enable timer compare operation
bit 0 SELT1PR (Period T2CON, the period register ignoring the period	0;	SELT1PR. In the case of EVA, this bit is register select).When set to 1 in of Timer 1 is chosen for Timer 2 also,

PLL\_C\_code.c

reserved bit in T1CON.  
 is SELT3PR (Period  
 T4CON, the period  
 Timer 4 also, ignoring  
 bit is a reserved  
 1 Use T1PR  
 EVB) as period  
 \*/

register of Timer 2. This bit is a  
 SELT3PR. In the case of EVB, this bit  
 register select).when set to 1 in  
 register of Timer 3 is chosen for  
 the period register of Timer 4. This  
 bit in T3CON.0 Use own period register  
 (in case of EVA) or T3PR (in case of  
 register ignoring own period register

```

    period = 6250;
    *T2PR = period ;    /* Period = 6250*25nsec*128 = 20msec or 50Hz */
    *T2CNT = 0x0;
    *T2CON = 0x9702; /* set in cont up, and set clock prescaler to 128 */
    /*
    bits 15-14          10;
    suspend
    complete on emulation suspend
    emulation suspend
    emulation suspend
    bit 13              0;
    effect.
    bits 12-11         10;
    bits 10-8          111;
    frequency
    bit 7              0;
    T2SWT1.
    Start GP timer 2 with
    bit is reserved in
    is T4SWT3.
    Start GP timer 4 with
    bit is reserved in
    case of EVA) or T3CON
    and disable operation ignoring
    bit 6              0;
    
```

```

    Free, Soft. Emulation control bits.
    00 stop immediately on emulation
    01 Stop after current timer period is
    10 Operation is not affected by
    11 Operation is not affected by
    Reserved. Reads return zero, writes have no
    TMODE1-TMODE0. Count Mode Selection.
    00 Stop/Hold
    01 Continuous-Up/-Down Count Mode
    10 Continuous-Up Count Mode
    11 Directional-Up/-Down Count Mode
    TPS2-TPS0. Input Clock Prescaler.
    000 x/1          100 x/16
    001 x/2          101 x/32
    010 x/4          110 x/64
    011 x/8          111 x/128
    x = device (CPU) clock
    T2SWT1. In the case of EVA, this bit is
    (GP timer 2 start with GP timer 1.)
    GP timer 1's timer enable bit. This
    T1CON.
    T4SWT3. In the case of EVB, this bit
    (GP timer 4 start with GP timer 3.)
    GP timer 3's timer enable bit. This
    T3CON.
    0 Use own TENABLE bit
    1 Use TENABLE bit of T1CON (in
    (in case of EVB) to enable
    own TENABLE bit
    TENABLE. Timer enable.
    0 Disable timer operation (the
    
```

PLL\_C\_code.c

```

timer is put in hold
reset)
                                1      Enable timer operations
bits 5-4          00;          TCLKS1, TCLKS0. Clock source select.
                                5-4      Source
                                0 0      Internal
                                0 1      External
                                1 0      Reserved
                                1 1      QEP Circuit† (in case of Timer
2/Timer 4)
                                Reserved (in case of Timer
1/Timer 3)
                                + This option is valid only if SELT1PR
= 0
bits 3-2          00;          TCLD1, TCLD0. Timer Compare Register Reload
Condition.
                                00      when counter is 0
                                01      when counter value is 0 or
equals period register value
                                10      Immediately
                                11      Reserved
bit 1             1;          TECMPR. Timer compare enable.
operation
                                0      Disable timer compare
                                1      Enable timer compare operation
bit 0             0;          SELT1PR. In the case of EVA, this bit is
SELT1PR (Period
                                register select).When set to 1 in
T2CON, the period register
                                of Timer 1 is chosen for Timer 2 also,
ignoring the period
                                register of Timer 2. This bit is a
reserved bit in T1CON.
                                SELT3PR. In the case of EVB, this bit
is SELT3PR (Period
                                register select).When set to 1 in
T4CON, the period
                                register of Timer 3 is chosen for
Timer 4 also, ignoring
                                the period register of Timer 4. This
bit is a reserved
                                bit in T3CON.0 Use own period register
1 Use T1PR
                                (in case of EVA) or T3PR (in case of
EVB) as period
                                register ignoring own period register
*/
/*
    *T1CON = 0x8842; /* start the clock */
/*
bit 15-14      10:      Operation is not affected by emulation suspend
bit 13         0:      reserved
bit 12-11      01:      01 = continous-up/down count mode
bit 10-8       000:     000 = x/1 prescaler
bit 7          0:      reserved in T1CON
bit 6          1:      TENABLE, 1 = enable timer
bit 5-4        00:      00 = CPUCLK is clock source
bit 3-2        00:      00 = reload compare reg on underflow
bit 1          1:      1 = enable timer compare
bit 0          0:      reserved in T1CON
*/
/*
    *T2CON = 0x9742;
/*
bit 15-14      10:      stop immediately on emulator suspend
bit 13         0:      reserved
bit 12-11      10:      10 = continous-up count mode
bit 10-8       111:     111 = x/128 prescaler
bit 7          0:      T2SWT1, 0 = use own TENABLE bit
bit 6          1:      TENABLE, 1 = enable timer

```

PLL\_C\_code.c

bit 5-4      00:      00 = CPUCLK is clock source  
bit 3-2      00:      00 = reload compare reg on underflow  
bit 1        1:        1 = enable timer compare  
bit 0        0:        SELT1PR, 0 = use own period register

```
*/  
/*-----  
-----  
-----
```

assign value to constant

```
-----  
-----  
-----*/
```

```
/*-----DC bus voltage variable initialization-----*/  
DCBusSum = 0;  
DCBusAvg = 0;
```

```
/*-----PLL variables initialization-----*/  
err_k_PLL=0;  
err_k1_PLL=0;  
U_k1_PLL=0;  
U_PLL=0;  
Y_k1_PLL=0;  
Y_PLL=0;  
Step_point_PLL=0;  
Fdbck_PLL=0;  
theta_PLL_diff=0;  
U_PLL_MAX=32767;  
U_PLL_MIN=-32766;
```

```
for (;;)   
{
```

```
}
```

# APPENDIX K

## **K Net Present Value and Break-Even results**

**Scenario 2: b) Demand charge started at R269 at begin of the project.**

Year	Start 2004 0	End 2004 1	End 2005 2	End 2006 3	End 2007 4	End 2008 5	End 2009 6	End 2010 7	End 2011 8	End 2012 9	End 2013 10	End 2014 11	End 2015 12
<b>Initial Investment:</b>													
Inverter	-R 100,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Battery	-R 1,200,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Battery Maintenance	R 0.00	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18	-R 3,818.18
Installation fees	-R 20,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Transformer	-R 15,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Transportation	-R 15,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Cabling	-R 3,000.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00
Battery Recovery Value	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 0.00	R 48,994.00
100kVA Yearly Saving	R 0.00	R 322,800.00	R 334,130.28	R 345,858.25	R 357,997.88	R 370,563.60	R 383,570.39	R 397,033.71	R 410,969.59	R 425,394.62	R 440,325.97	R 455,781.41	R 471,779.34
<b>Total Cash Flow</b>	-R 1,353,000.00	R 318,981.82	R 330,312.10	R 342,040.07	R 354,179.70	R 366,745.42	R 379,752.21	R 393,215.53	R 407,151.41	R 421,576.44	R 436,507.79	R 451,963.23	R 516,955.16
<b>Present Value (PV)</b>	-R 1,353,000.00	R 289,983.47	R 272,985.21	R 256,979.77	R 241,909.50	R 227,720.05	R 214,360.22	R 201,781.74	R 189,939.14	R 178,789.56	R 168,292.65	R 158,410.36	R 164,717.85
<b>Net Present Value</b>	<b>R 1,212,869.52</b>												
<b>Break-Even</b>		-R 1,063,016.53	-R 790,031.32	-R 533,051.55	-R 291,142.05	-R 63,422.00	R 150,938.22	R 352,719.96	R 542,659.10	R 721,448.66	R 889,741.31	R 1,048,151.67	R 1,212,869.52