DEVELOPMENT OF A MULTILEVEL CONVERTER TOPOLOGY FOR TRANSFORMER-LESS CONNECTION OF RENEWABLE ENERGY SYSTEMS

Thesis by:

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Declaration

I, at this moment, state that I am the only author of this presented thesis. Furthermore, I have a good understanding and knowledge of plagiarism and have ensured the main body of work presented is my original research findings, apart from those referenced from existing literature. Therefore, this thesis is submitted to the Department of Electrical Engineering, Faculty of Engineering and Built Environment, University of Cape Town, in complete fulfilment of my Doctor of Philosophy degree. However, parts of this presented work have been presented in peer-reviewed journals and conference proceedings.

The total word count of the main chapters of the thesis is within the prescribed limit of the Doctoral Degrees Board.

Abstract

The global need to reduce dependence on fossil fuels for electricity production has become an ongoing research theme in the last decade. Clean energy sources (such as wind energy and solar energy) have considerable potential to reduce reliance on fossil fuels and mitigate climate change. However, wind energy is going to become more mainstream due to technological advancement and geographical availability. Therefore, various technologies exist to maximize the inherent advantages of using wind energy conversion systems (WECSs) to generate electrical power. One important technology is the power electronics interface that enables the transfer and effective control of electrical power from the renewable energy source to the grid is through the filter and isolation transformer. However, the transformer is bulky, generates losses, and is also very costly. Therefore, the term "transformer-less connection" refers to eliminating a step-up transformer from the WECS, while the power conversion stage performs the conventional functions of a transformer.

Existing power converter configurations for transformer-less connection of a WECS are either based on the generator-converter configuration or three-stage power converter configuration. These configurations consist of conventional multilevel converter topologies and two-stage power conversion between the generator-side converter topology and the high-order filter connected to the collection point of the wind power plant (WPP). Thus, the complexity and cost of these existing configurations are significant at higher voltage and power ratings.

Therefore, a single-stage multilevel converter topology is proposed to simplify the power conversion stage of a transformer-less WECS. Furthermore, the primary design challenges – such as multiple clamping devices, multiple dc-link capacitors, series-connected power semiconductor devices – have been mitigated by the proposed converter topology. The proposed converter topology, known as the "**tapped inductor quasi-Z-source nested neutral-point-clamped (NNPC) converter,**" has been analyzed, designed, and a prototype of the topology developed for experimental verification. A field-programmable gate array (FPGA)-based modulation technique and voltage balancing control technique for maintaining the clamping capacitor voltages was developed. Hence, the proposed converter topology presents a single-stage power conversion configuration. Efficiency analysis of the proposed converter topology has been studied and compared to the intermediate and grid-side converter topology of a three-stage power converter configuration. A direct current (DC) component minimization

technique to minimize the dc component generated by the proposed converter topology was investigated, developed, and verified experimentally. The proposed dc component minimization technique consists of a sensing and measurement circuitry with a digital notch filter.

This thesis presents a detailed and comprehensive overview of the existing power converter configurations developed for transformer-less WECS applications. Based on the developed comparative benchmark factor (CBF), the merits and demerits of each power converter configuration in terms of the component counts and grid compliance have been presented. In terms of cost comparison, the three-stage power converter configuration is more cost-effective than the generator-converter configuration. Furthermore, the cost-benefit analysis of deploying a transformer-less WECSs in a WPP is evaluated and compared with conventional WECS in a WPP based on power converter configurations and collection system. Overall, the total cost of the collection system of WPP with transformer-less WECSs is about 23% less than the total cost of WPP with conventional WECs.

The derivation and theoretical analysis of the proposed five-level tapped inductor quasi-Z-source NNPC converter topology have been presented, emphasizing its operating principles, steady-state analysis, and deriving equations to calculate its inductance and capacitance values. Furthermore, the FPGA implementation of the proposed converter topology was verified experimentally with a developed prototype of the topology. The efficiency of the proposed converter topology has been evaluated by varying the switching frequency and loads. Furthermore, the proposed converter topology is more efficient than the five-level DC-DC converter with a five-level diode-clamped converter (DCC) topology under the three-stage power converter configuration. Also, the cost analysis of the proposed converter topology and the conventional converter topology shows that it is more economical to deploy the proposed converter topology at the grid-side of a transformer-less WECS.

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I dedicate this work to all my forebearers in power electronics whose research outputs gave me the inspiration and necessary knowledge to carry out the presented work and the loving memory of my late sister, Dr Adeoluwa Oyindamola Ajayi-Obe.

List of Publications

Journal Paper Published:

[1] **Akinola A. Ajayi-Obe**, M. A. Khan, and P. Barendse, "Techno-Economic Evaluation of Five-Level Nested Neutral Point Clamped (NNPC) Converter Topology for Transformer-less Connection of High-Power Wind Energy Conversion Systems" Journal of Energy in Southern Africa (JESA), Vol. 3, No. 3, pp.33-43, August 2019**.**

Paper in Refereed Conference Proceeding:

[2] **Akinola A. Ajayi-Obe**, and M. A. Khan, "Analysis and Design of a Quasi-Proportional-Resonant Based Voltage Balancing Control for Grid-Connected Nested Neutral Point Clamped Converter" in IEEE-Energy Conversion Congress Exposition (ECCE) 2018 Proceeding, pp. 2982-2987, December 2018.

[3] **Akinola A. Ajayi-Obe** and M. A. Khan, "Analysis of a Five-Level Dual Tapped Inductor Quasi Impedance Source-Nested Neutral Point Clamped Converter" in IEEE-Energy Conversion Congress Exposition (ECCE) 2017 Proceeding, pp. 2150-2155, November 2017.

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[5] **Akinola A. Ajayi-Obe**, M. A. Khan, and P. Barendse, "Impact of Voltage Sags on a Transformer-less Wind Energy Conversion System", 9^{th} Renewable Energy Postgraduate Symposium, University of Stellenbosch, Cape Town, South Africa, 13^{th} – 14^{th} September 2018.

[6] **Akinola A. Ajayi-Obe**, M. A. Khan, and P. Barendse, "Comparative Evaluation of Transformer-less Configurations for Wind Energy Conversion Systems", WindAC 2017, Cape Town, South Africa.

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Glossary of Abbreviations and Symbols

Abbreviations

1ph	One-Phase
3ph	Three-Phase
6ph	Six-Phase
2L	Two-Level
3L	Three-Level
4L	Four-Level
5L	Five-Level
7L	Seven-Level
AC	Alternating Current
ANPC	Active Neutral-Point-Clamped
CBF	Comparative Benchmark Factor
DAB	Dual Active Bridge
DAQ	Data Acquisition
DC	Direct Current
DCC	Diode-Clamped Converter
DD	Direct Drive
DFIG	Doubly-Fed Induction Generator
FC	Flying Capacitor
FPGA	Field Programmable Gate Array
GW	Gigawatt
HIL	Hardware-In-Loop
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
IPCC	Intergovernmental Panel on Climate Change
LCC	Life Cycle Cost
LUT	Look-up Table
LV	Low Voltage

MMC	Modular Multilevel Converter
MSC	Modular Switched Capacitor
MV	Medium Voltage
MW	Megawatt
NI	National Instruments
NNPC	Nested Neutral-Point-Clamped
PCC	Point of Common Coupling
PF	Power Factor
PMSG	Permanent Magnet Synchronous Generator
PS-PWM	Phase-Shifted Pulse-Width Modulation
QZS	Quasi-Z-Source
RT	Real-time
ST	Substation Transformer
THD	Total Harmonic Distortion
VCR	Voltage Conversion Ratio
VSC	Voltage Source Converter
WECS	Wind Energy Conversion System
WPP	Wind Power Plant

Symbols

α	No-load loss cost rate
$A_{increment}$	Accumulator increment
A_{PS}	Accumulator phase shift
β	Load loss cost rate
ΔY_g	Grounded wye/delta connection
σ_e	Shear stress of the airgap
B_f	Boost factor
β_s	Tip speed ratio
B_{pk}	Peak operating flux density
C_{assoc}	Cost of associated substation equipment

C_{cap}	Capacitor cost
C_{cable}	Connecting cable cost
C_{cc}	Component cost
C_{core}	Core cost
$C_{core/weight}$	Cost per weight for the core
C_{csc}	Cooling system cost
C_e	Energy cost
$C_{FC_{core}}$	Fixed cost of the core
C_{FC_W}	Fixed cost of the winding
C_{FC_l}	Fixed cost of labour
C_{HV_c}	Cost of the high voltage cable
C_i	Initial cost
C_{IGBT}	IGBT cost
C_{ind}	Inductor cost
C_{ins}	Cost of installation
C_{inv}	Capital cost
C_l	Labour cost
$C_{l/weight}$	Cost per weight for labour
C_{loss}	Power loss cost
$C_{loss,WT}$	Cost of WT Transformer losses
$C_{loss,cable}$	Cost of connecting cable losses
$C_{loss,ST}$	Cost of ST transformer losses
C_{MV_c}	Cost of the medium voltage cable
C_0	Filter capacitor
C_{op}	Operation and maintenance cost
C_p	Power coefficient
C_r	Rated capacitance
C_{re}	Resonant Capacitor
C_{ST}	Cost of the ST transformer

C_{sub}	Cost of substation equipment
C_{tran}	Cost of transportation
C_w	Winding cost
$C_{w/weight}$	Cost per weight for the winding
C_{WT}	Cost of wind turbine transformer
CEL_f	Component for each level factor
D_{nst}	Duty cycle of the NST mode
D_{PS}	Phase shift in degrees
D_{st}	Duty cycle of the ST mode
D_r	Resonant duty cycle
DF	Discount factor
E_e	Energy cost per unit
f_s	Switching frequency
f_g	Grid frequency
f_{res}	Resonance frequency
G_M	Gross margin
GC_f	Grid compliance factor
i	Interest rate
$I_{CAL-IGBT}$	Calculated current rating
I_{Diode}	Current rating of the clamping diode
I_g	Grid current
I_{HV_c}	Current flowing through the high voltage connecting cable
I_{IGBT}	Current rating of the IGBT
I_{MV_c}	Current flowing through the medium voltage connecting cable
I_p	Peak output current
I_{ph}	Maximum phase current
K_p	Proportional gain
K_r	Resonant gain
k_u	Window utilization factor
l_e	Length of the airgap

L_g	Inductance of the grid-side filter
L_k	Leakage inductance of the transformer
L_{loss}	Load loss of the transformer
L_r	Resonant inductor
L_s	Length of each string
L_{hv}	Length of high voltage cable
m_a	Modulation index
N	Expected lifetime of the WPP/transformer
N_A	Number of turns of the active bridge
N_{cap}	Number of capacitors
N_D	Number of turns of the diode-bridge
N_{Diode}	Number of diodes
N_f	Number of feeders
N_{IGBT}	Number of IGBTs
N_{ind}	Number of inductors
N_L	Number of voltage levels
n_s	Stacking factor of the cores
n_{ST}	Number of substations in the WPP
N_{samp}	Number of samples
N_{ss}	Number of switching states
N_{sub}	Number of substations
N_s	Number of strings
NE_{IGBT}	Equivalent number of IGBTs
NE_{Diode}	Equivalent number of diodes
NE_{cap}	Equivalent number of capacitors
NE_{ind}	Equivalent number of inductors
n_{WT}	Number of WECSs in the WPP
O_{pa}	Transformer operating hours per annum
ρ	Air density
$P_{C(IGBT)}$	Conduction losses associated with IGBTs

$P_{C(diode)}$	Conduction losses associated with diodes
P_D	Maximum allowable dissipation
P_g	Active power between the converter and the grid
P_{WECS}	Active power of the WECS
P_{WT}	Unit price of a WT transformer
P_{LS}	Power losses associated with power semiconductor devices
P_{LP}	Power losses associated with passive devices
$P_{Loss,ind}$	Power losses associated with inductors
$P_{Loss,cap}$	Power losses associated with capacitors
P_{ST}	Unit price of a substation transformer
$P_{sw(igbt)}$	Switching losses associated with IGBTs
$P_{sw(rec)}$	Switching losses associated with diodes
P_R	Active power rating of the WECS
Q_g	Reactive power between the converter and the grid
r	Radius
R_θ	Thermal resistance of the core
R_f	Feeder resistance
R_g	Resistance of the grid-side filter
R_s	Source resistance
R_{MV_c}	Resistance of the medium voltage connecting cable
R_{HV_c}	Resistance of the high voltage connecting cable
R_{THh}	Thermal resistance of the heatsink
R_{THJ-C}	Thermal resistance of junction to case
R_{THC-H}	Thermal resistance of case to heatsink
SS_f	Switching state factor
T_a	Ambient temperature
T_e	Electrical torque
T_j	Junction temperature
T_m	Mechanical torque

T_{nst}	Switching period during the NST mode
T_{sh}	Switching period during the ST mode
v	Wind speed
v_A	Output ac voltage of the single-phase active bridge
v_D	Input ac voltage of the single-phase diode-bridge
V_a, V_b, V_c	Three-phase grid voltage
V_{cap}	Voltage rating of capacitors
$V_{CAL-IGBT}$	Calculated voltage rating
V_{dc}	DC-link voltage
V_{dc_max}	Maximum dc-link voltage
V_{dc_s}	DC-link voltage of series-connected pair of a diode rectifier and single-switch boost converter.
$V_{dc\_voltage}$	Maximum dc voltage due to cosmic radiation
V_{Diode}	Voltage rating of diodes
V_g	Grid voltage
V_{IGBT}	Voltage rating of IGBTs
V_{ind}	Voltage rating of inductors
V_{in}	Input voltage
V_{LL}	Line-to-line voltage level of the collection point
$V_{Min.-Com}$	Minimum commutation voltage
V_o	Output voltage
$V_{o,cell1}$	Output voltage of the upper diode rectifier and single-switch boost converter
$V_{o,cell2}$	Output voltage of the lower diode rectifier and single-switch boost converter
V_{out}	Phase output voltage
ω_c	Cut-off angular frequency
ω_o	Resonant angular frequency
ω_{WECS}	Rotational speed of the WECS
X_f	Feeder reactance
X_s	Source reactance

$Y_g\Delta Y_g$	Grounded-wye/grounded-wye/delta connection
Z_c	Collector impedance
Z_f	Feeder impedance
Z_l	Load impedance
Z_s	Source impedance

Chapter 1

Introduction

The awareness of global warming has increased significantly in the last two decades, with international organizations producing technical assessment reports that highlights the causes and impacts of global warming [1], [2]. These reports show that global warming will continue due to increasing global energy demand [1]. The significant increase in global energy demand is due to economic and population growth, with overdependence on fossil fuel for electricity generation and transportation being a critical factor [1]-[3]. With a projected 48% increase in global energy demand from year 2020 to year 2050, sustainable and efficient energy sources must be developed and deployed [3]. Therefore, the most sustainable solution to minimize global warming is systems based on renewable energy sources [1]-[3].

Among the various emerging renewable energy sources deployed in recent times for electricity generation, wind energy and solar energy are the two most well-known renewable energy sources [1]-[6]. However, geographical availability, technological advancement, and cost have made wind energy very prominent in the last decade [3], [5]-[7]. The installed global wind power capacity is currently about 98 Gigawatt (GW), as shown in Figure 1.1 [6], [8]. In addition, the installed global wind power capacity is projected to increase by 17% from year 2021 to year 2026 [8]. Furthermore, the total installed global wind power capacity is expected to be about 300GW in about a decade, as shown in Figure 1.1 [8]. This global trend of increasing installed wind energy conversion systems (WECSs) has resulted in the development of high-power systems because the maximum power produced by a WECS increases linearly with air density and swept area of the rotor blades [6], [8], [9]. Furthermore, the power capacity of commercially available WECSs is projected to be about $15MW$ to $20\ MW$ in the next decade [6]. However, operating a WECS at such a high-power range with a low voltage (LV) level will result in the transmission of excessive electric current in the system [6], [10]-[11]. The power conversion stage of the system will consist of several power semiconductor devices connected in parallel to handle the high current value within its topologies [10]-[13]. Also, the associated cable losses and the connecting cables' cost are increased significantly [6]. Therefore, the electric current transmitted in a high-power WECS operated at a much higher voltage level results in reduced cable losses and cost [6].

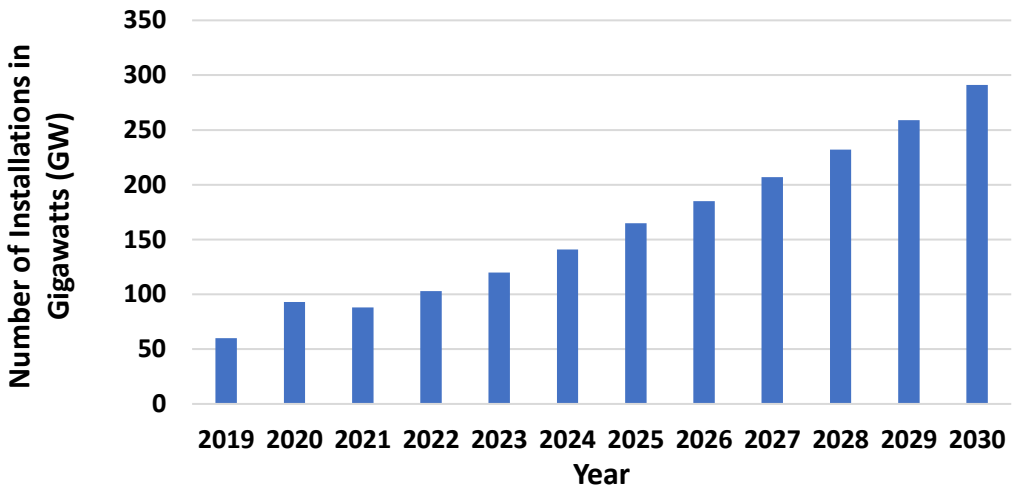


Figure 1.1: Global installed wind power capacity from year 2019 to year 2030 [8].

The efficiency of a high-power WECS can be enhanced by increasing its voltage level to the medium voltage (MV) range and simultaneously reduce its electric current rating. However, it requires more complex subsystems, such as a medium voltage electric generator and multilevel power converter topology utilized in the system [6], [10]-[12]. The medium voltage electric generators are available within $3kV$ to $6.6\ kV$ and $2MW$ to $10\ MW$ voltage and power ratings, respectively [6]. A multilevel power converter topology is preferred because it is possible to produce higher output voltage amplitude irrespective of the voltage ratings of the power semiconductor devices deployed in the topology [12]-[15]. Also, the multilevel converter topology produces output voltage and current waveform with less harmonic distortion [13]-[18].

Therefore, this research explores the possibility of eliminating the need for a wind turbine transformer by developing a grid-side multilevel converter configuration that can operate at a medium voltage (MV) level [6], [14]. This thesis presents the analysis, design and development of a novel single-stage converter topology deployed at the grid-side of the transformer-less WECS. Furthermore, the theoretical analysis, control algorithm, real-time implementation, and prototyping of the proposed converter topology have been investigated extensively.

Therefore, the organization of Chapter 1 is as follows: a brief overview of reliability studies on existing WECSs is discussed in Section 1.1, and a detailed explanation of the motivation for carrying out this research is presented in Section 1.2. The objectives of this research work have been outlined in Section 1.3. Finally, the outline and organizational structure of this thesis are summarized in Section 1.4.

1.1. Overview of Reliability Studies on WECS

The increased penetration of WECSs has resulted in the development of large-scale onshore and offshore WPP, as discussed earlier [6]-[19]. However, most of the large-scale WPP development will be situated offshore in the coming decades [8]. The wind energy resources available in offshore regions far exceeds onshore wind resources [19]. However, the cost of installation and operation of an offshore WPP is estimated to be about eight times more than an onshore WPP because the components of an offshore WECS are more prone to failure due to the harsh environmental conditions and system complexity [19]-[21].

Various reliability studies on installed WECSs have been presented in the literature [20]-[25]. A detailed survey on the failure statistics of WECSs in WPPs situated in Finland, Germany, and Sweden was carried out in [24]. This survey was based on operational statistics collected on the WPPs, to identify the most critical subsystem for both failure rate and downtime [24]. The electrical subsystem showed the highest failure rate in both onshore and offshore WPPs, as illustrated in Figure 1.2 [24]. Simultaneously, the multistage gearbox subsystem was identified as the component with the highest downtime [24]. Furthermore, this survey showed that WECS rated above $1MW$ tends to have higher failure frequency, and the control subsystem was identified to have the second-highest failure rate, as shown in Figure 1.2 [24]. Another reliability study was carried out based on the electric generator technology deployed in WECS [25]. This study investigated about 2,000 WECSs consisting mainly of doubly fed induction generator (DFIG)-based WECSs and permanent magnet synchronous generator (PMSG)-based WECSs [25]. The DFIG-based WECS was more susceptible to failure than its PMSG counterpart due to gearbox and auxiliary system-related issues [25].

Furthermore, a comprehensive reliability analysis on the subsystem of 6,000 WECSs in Denmark and Germany was carried out based on the bathtub curve concept and analysed data collected over 11 years from the WIND STATS survey [23]. In this study, the subsystems with the highest failure rate in descending order are electrical subsystems, rotor, converter, electric generator, hydraulics, and gearbox [23]. From the results and discussion presented, high-power WECSs are prone to more failure due to their high complexity and direct-drive (gearless) WECS is more reliable than the geared WECS [23]. The power converter configuration of direct-drive and geared WECS exhibits a high failure rate due to environmental conditions [23]. Also, the electrical subsystem is the least reliable subcomponent of the WECS, as stated in [23]. The electrical subsystem consists of the transformer, power feeder cable, grid-side

filter, switchgear, power protection unit, circuit breaker, and surge arrestor [23]. Finally, the failure rate of high-power WECS increases with the system's operational years [20]-[25], as indicated in Figure 1.3. Therefore, the subsequent sections focus on the reliability-related issues associated with the electric generators, power converter topologies and electrical subsystem deployed in direct-drive WECSs of a WPP.

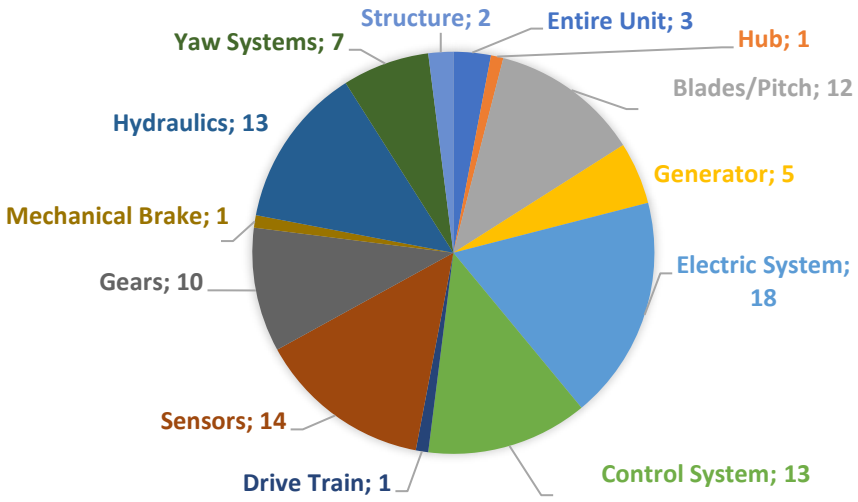


Figure 1.2: Breakdown of the number of failures in various components of a WECS connected in an onshore Swedish WPPs [24].

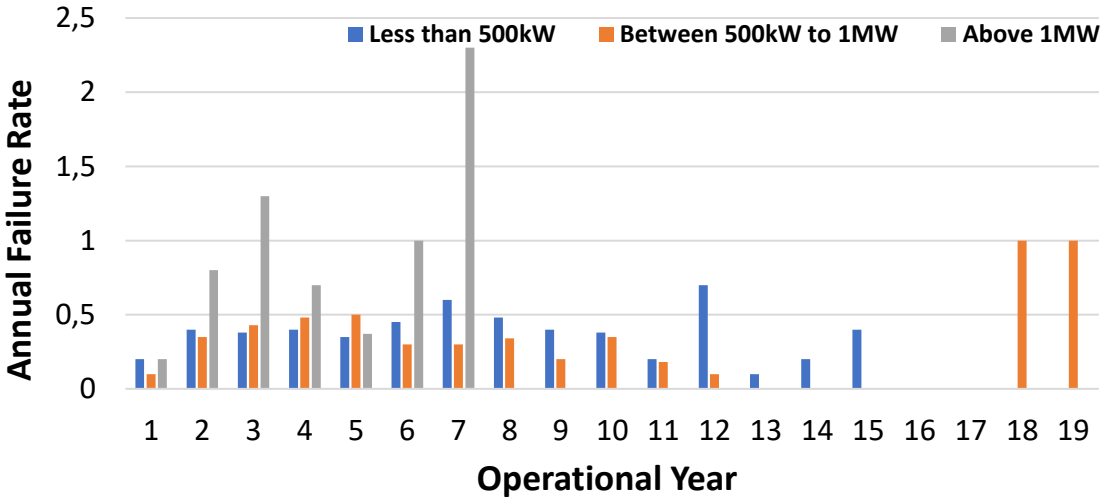


Figure 1.3: Failure rate with the respective rated power capacity of WECS showing their operational years [24].

1.1.1. Electric Generators

Most of the widely used direct-drive WECSs consist of synchronous generators with electrical excitation [6], [26]. The main advantage of a direct-drive PMSG (DD-PMSG) in WECSs is its high level of reliability [6], [25]-[29]. However, due to the direct coupling of the generator rotor shaft to the turbine, DD-PMSG operates at low speed with high torque, which directly increases the physical size of the generator [6], [26]-[28]. The radial-flux PMSG is a preferred choice for high-power direct-drive WECS due to its reduced weight and cost, as shown by the cost/torque and mass/torque optimization technique in [28]. Furthermore, 400 DD-PMSG WECSs were analysed based on the manufacturer's data on scheduled maintenance report in [25]. This analysis showed that most of the failures associated with DD-PMSG were related to the lubrication and cooling system of the generator, which is classified as "**minor repairs**" because they are inexpensive [25]. Overall, the DD-PMSG has higher efficiency, reliability and requires low maintenance [25]-[28].

Compared with other conventional electric generators deployed in WECS, the DD-PMSG is more expensive in terms of the initial capital cost outlay [26]. However, the operational and maintenance cost of the DD-PMSG is minimized when compared to geared-electric generators [26]. Furthermore, current research studies in the optimization of DD-PMSG will result in the cost-effectiveness and efficiency of the WECS [6], [25]-[28]. The power converter topologies deployed in DD-PMSG-based WECSs are discussed in the next section.

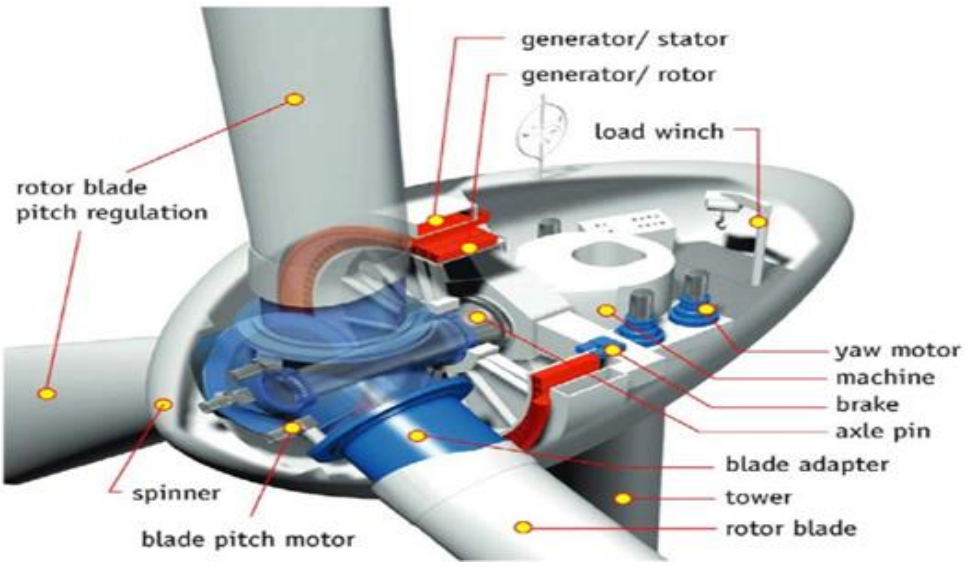


Figure 1.4: A direct drive WECS [27].

1.1.2. Power Converter Topologies

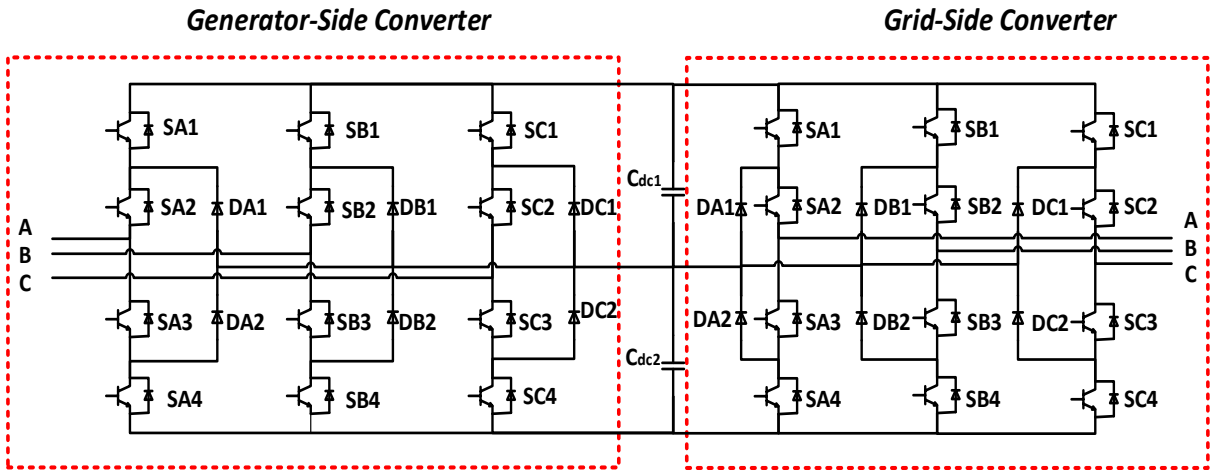
A DD-PMSG WECS consist of a fully rated power conversion stage that enables the generator-side converter topology to be operated independently of the grid-side converter topology [6], [12]-[15], [30]. The generator-side converter topology ensures maximum power is extracted from the wind via the generator, and the grid-side converter topology maintains the dc-link voltage of the power conversion stage [6], [12]-[15]. Furthermore, the grid-side converter supports the power factor by controlling the active and reactive power of the system [6], [12]-[15], [30].

The conventional multilevel converter topologies applied to the power conversion stage of WECSs are diode-clamped converter (DCC), flying-capacitor (FC) converter, modular multilevel converter (MMC), and active neutral-point-clamped (ANPC) converter [6], [14], [31]-[34], as shown in Figures 1.5(a) to 1.5(d). The most popular multilevel converter topology is the three-level DCC (3L-DCC) because of its simple circuitry and cost-effectiveness [12]-[14]. However, its major drawback is the asymmetrical distribution of losses amongst its power semiconductor devices [15], [35]. The three-level ANPC (3L-ANPC) topology improved the highlighted drawback of the 3L-DCC topology [35], [36]. Simultaneously, the MMC topology consists of either a half-bridge or full-bridge cell cascaded to attain the output voltage range of the topology [13], [34]. A medium voltage DD-PMSG WECS made up of power converter configuration with MMC topology have been presented in [34].

The main components contributing most to the failure rate in a WECS power converter configuration have been highlighted [25]. The cooling system contributed about 30% of the observed failure rate in the converter [25]. Therefore, an accurate assessment of the heat dissipated from the power semiconductor devices and environmental conditions will minimize the cooling system's failure rate [30], [37]. Based on data obtained from 2734 wind turbines field-data and damage analysis evaluated, the capacitors, power semiconductor devices, and gate drivers cause most of the failures in a power converter configuration [30], [37], as illustrated in Figure 1.6.

The insulated gate bipolar transistor (IGBT) is widely used in the power converter configuration of a WECS, as stated in the literature [6], [14]. The IGBT is often classified based on its packaging technology; it can either be module-based or press-pack-based [38]-[40], as shown in Table 1.1. The integrated gate-commutated thyristor (IGCT) is rarely used in high power application because of its high cost and complex gate driver circuitry [14]. Most power

converter configuration consists of IGBT modules due to the cost and ease of mounting in the circuitry [39]. However, the IGBT module is prone to failure due to wire-bond lift-off, breakdown of the die insulation, and cracks in the solder joint [6], [14]. The gate driver circuitry required for switching the IGBT module is often affected by environmental conditions such as dust and moisture [30]. Also, capacitors used in the dc-link and for voltage clamping purposes are subjected to continuous electrical and thermal stress because of the variable nature of wind and compliance to grid codes [6], [39], [41]-[43]. A reliable and efficient power converter configuration should have minimal clamping devices, a dc-link split configuration, and minimal series-connected power semiconductor devices [6], [12]-[15]. Furthermore, other components associated with the operation of the power converter configuration sometimes termed "other power-converter components" in existing literature, have been classified as components in the electrical subsystem of the WECS in the thesis [22]-[25], [30], [44]-[47].



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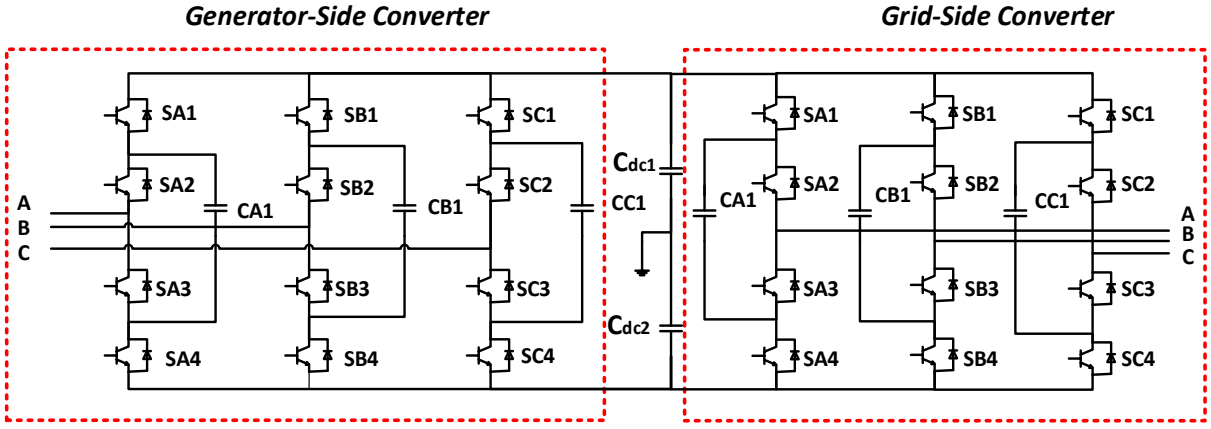

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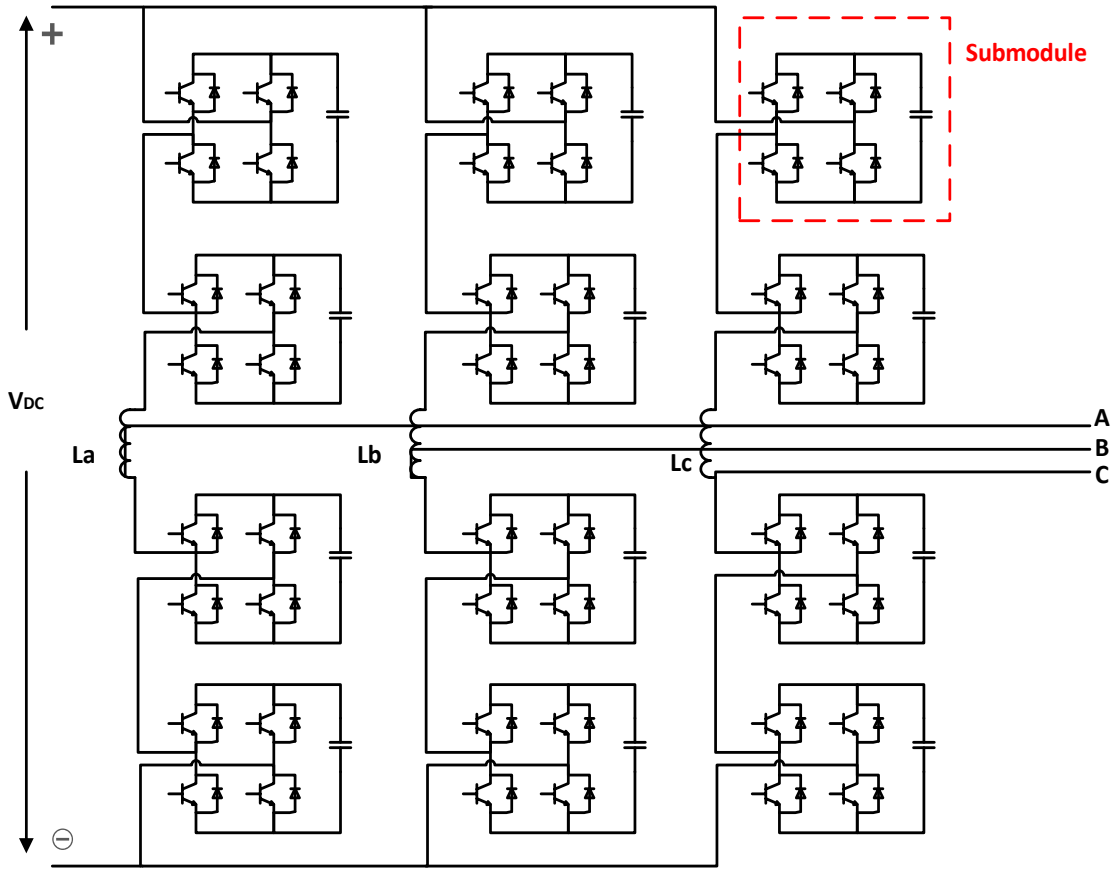

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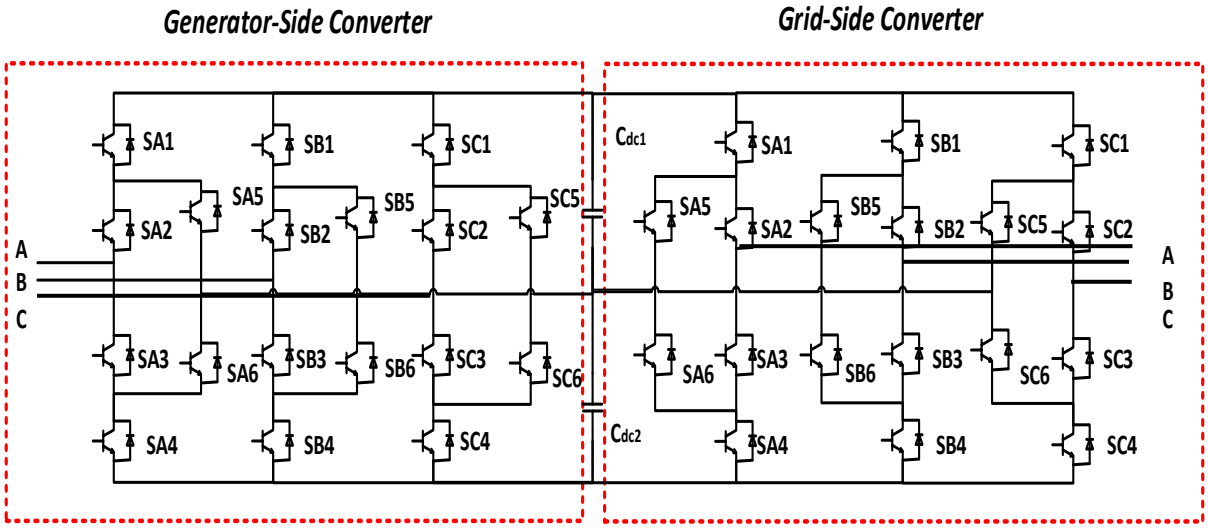


(d)

Figure 1.5: Different multilevel topologies. (a) 3L-DCC, (b) 3L-FC, (c) 5L-MMC, (d) 3L-ANPC.

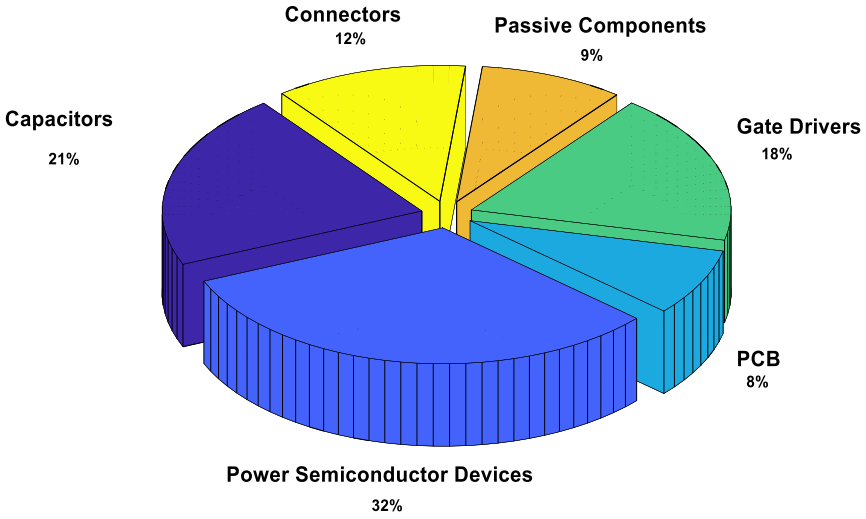


Figure 1.6: Fragile components in a power converter configuration [30], [37].

Table 1.1: Main power semiconductor devices voltage and current ratings [14]

	IGBT Module	IGBT Press-pack	IGCT Press-pack
Medium voltage ratings (kV)	3.3 kV/4.5 kV /6.5kV	2.5 kV/4.5 kV	4.5 kV/6.5 kV /10kV
Maximum current ratings (kA)	1.5 kA/1.2 kA /0.75 kA	2.3 kA/2.4 kA	3.6 kA/3.8 kA /2 kA
Switching loss	Low	Low	Moderate
Conduction loss	High	High	Moderate
Gate driver	Small	Small	Large
Cost	Moderate	High	High

1.1.3. Electrical Subsystem

Based on existing reliability studies on installed WECS in the literature, the electrical subsystem is considered the least reliable subsystem [22]-[25]. The electrical subsystem consists of the transformer, power feeder cable, grid-side filter, switchgear, power protection unit, circuit breaker, and surge arrestor [44]-[47]. In Figure 1.7, the failure rates and associated downtime of the main parts of the electrical subsystem are illustrated [29]. Based on their descending order of significance, the components with the highest failure rate are as follows [29]:

- Power protection unit
- Power feeder cable
- Transformer
- Switchgear
- Power cabinet

Also, based on their descending order of significance, the components with the highest downtime rate are as follows [29]:

- Transformer
- Power protection unit
- Power cabinet
- Power feeder cable
- Switchgear

Furthermore, the transformer is one of the most expensive electrical subsystem components, as shown in Figure 1.8 [22]. Simultaneously, the size of a transformer remains a significant factor in an installed WECS.

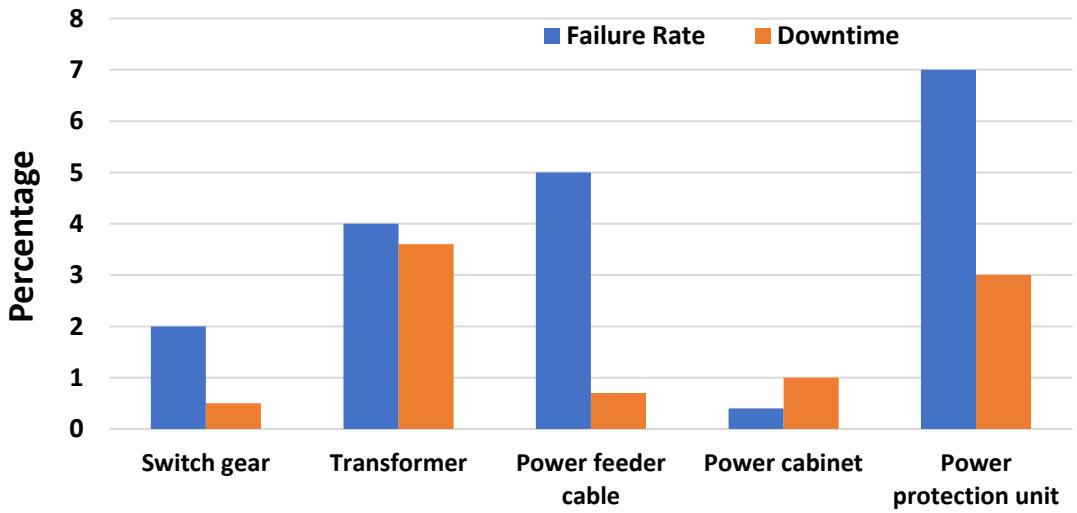


Figure 1.7: Breakdown of the failure rates and downtimes of electrical subsystem components of direct drive WECS [29].

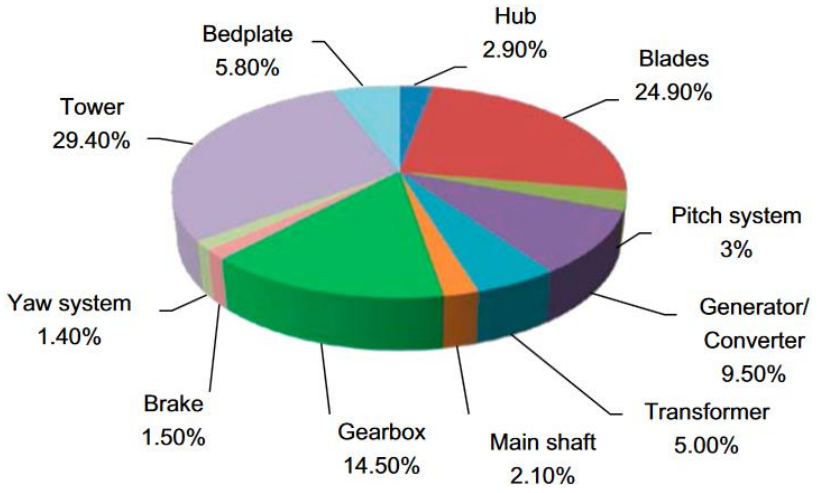


Figure 1.8: Breakdown of the component costs of a WECS [22].

The transformer is bulky, and it accounts for about 5% of the total cost of procurement of a high-power WECS, as shown in Figure 1.8 [22]. Apart from cost and reliability related issues, another drawback of the transformer is the restriction of its maximum output voltage to 34.5 kV (which is the highest voltage level of the collection point of a WPP based on ANSI C84.1 standard) [6], [12], [44]. This restriction is due to the significant increase in the physical size at higher voltage levels, making it challenging to mount the transformer close to the WECS tower [44]. The main functions of a transformer have been analyzed extensively in Chapter 2 of the thesis, as reviewed in the literature [48]-[63].

The main reasons for the failure of a transformer are the variable nature of wind, utilization of conventional distribution transformer, and compliance to grid codes [64], [65]. The loading factor of a conventional distribution transformer utilized in a WECS is low (within $20\% - 30\%$), leading to more core losses and multiple loading cycles [64], [65]. Furthermore, the transformer experiences a significant inrush current during voltage sags (i.e., grid voltage unbalance) leading to electrical and thermal stress on the transformer windings [16]-[18], [64]. By utilizing specific transformers in a WECS, the stated drawbacks are further minimized [50], [64]. Therefore, the types of transformers designed and developed specifically for WECS are as follows, and a comparison of their features is presented in Table 1.2 [48]-[50], [66], [67]-[70].

- Vacuum cast coil dry-type transformer.
- Liquid-immersed transformer.
- Bio-SLIM transformer.

Table 1.2: Comparison of transformers [48]-[50], [66], [67]-[70]

	Vacuum Cast Coil	Liquid-Immersed	Bio-SLIM
Size	High	Moderate	Moderate
No-load losses	High	Average	Low
Full-load losses	Average	Average	Average
Reliability	Low	Moderate	High
Cost	Moderate	Moderate	High

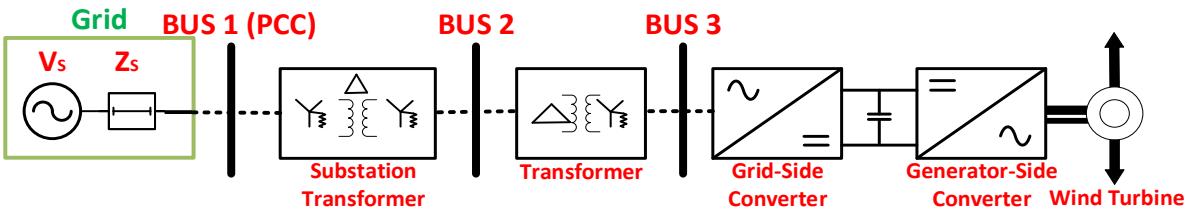
1.2. Motivation for Research

The projected increase in the power capacity of installed WECSs will require more efficient electric generators and power converter topologies which are the two main subsystems of the WECS. One of the main approaches to minimizing power losses in a WECS is reducing electric current transmission by operating at a medium voltage (MV) level [6], as previously stated. A conventional WECS requires a step-up transformer to transform its output voltage to the point of common coupling (PCC), which results in high procurement and installation costs resulting from its enormous weight and size. For example, a standard $0.69/33kV$, $2.5MVA$ transformer weighs about eight tonnes $(8t)$ with a volume of $9m^3$ [64]. Therefore, the weight and volume of the transformer will increase with the projected power capacity of installed WECSs [6]. While, most WPP will be situated offshore in the future, which will increase the procurement, installation, and maintenance cost about eight times more than an onshore WPP [19]-[21]. The associated maintenance cost of an offshore WPP is estimated to be about $2.3\ cents/kWh$ [19]-[21], [64]. Based on the stated cost components, research efforts have been directed to minimizing the related cost by eliminating the transformer.

Furthermore, running a high-power WECS at a medium voltage (MV) level brings about the possibility of eliminating the need for a step-up transformer (i.e., transformer-less connection) by connecting the system directly to the collection point through a grid-side filter [6], [14]. Based on a comprehensive literature review presented in Chapter 2, previous studies have focused on developing medium-voltage electric generators and utilizing conventional multilevel converter configurations to achieve a transformer-less connection of the system [6]. However, this research seeks to investigate a novel single-stage power converter topology that enables the transformer-less connection of a WECS to the collection point of a WPP.

1.2.1. Problem Statement

The power converter configuration deployed in a transformer-less WECS must perform most of the primary functions attributed to conventional transformer. Figure 1.9(a) shows a conventional WPP with WECSs connected to the collection point with transformers. Figure 1.9(b) also illustrates WPP with WECSs connected to the collection point without transformers. The operating voltage level of a transformer-less WECS is yet to be standardized, but it is likely to increase with the projected power ratings of WECS [6]. However, the operating voltage can be based on the collection point voltage levels of WPP classified by their regions, as stated in Table 1.3 [47].



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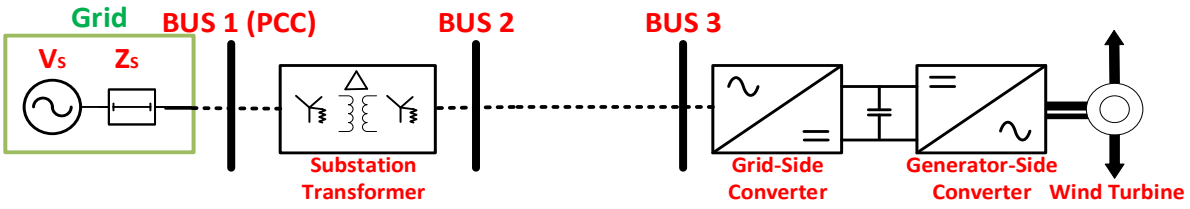


(b)

Figure 1.9: Different WPP models; (a) A conventional WPP with wind turbine transformer, (b) A WPP without wind turbine transformer.

Table 1.3: Medium voltage (MV) level of the collection point by region [47]

Region	Standard	Medium voltage level
Europe	IEC 60038	$6.6\ kV - 33\ kV$
North America	ANSI C84.1	$6.9\ kV - 34.5\ kV$

The concept of a transformer-less WECS was first discussed in [12] by introducing the DD-PMSG by both Enercon and Siemens Wind Power [6]. The power conversion stage of the DD-PMSG can be operated from a low-voltage (LV) level to a medium voltage (MV) level [6], [14]. The conventional power converter topologies discussed previously are suggested and expected to be deployed in the power conversion stage of a transformer-less WECS [6], [12]-

[15], [30]-[36]. However, the complexity of these power converter topologies increases in terms of the number of power semiconductor devices, clamping devices, control algorithm, and grid compliance [6], [14]. Therefore, the following issues must be addressed whilst designing a grid-side converter topology that connects directly to the collection point of a WPP:

- Voltage conversion ratio between the generator-side and the collection point
- Voltage rating of the modern power semiconductor devices and number of clamping devices
- Minimization of dc component
- Cost-effectiveness

A. Voltage conversion ratio between the generator-side and the collection point

A summary of the commercial DD-PMSG based WECSs, and their associated power ratings are highlighted in Table 1.4. It can be observed that increasing the voltage level of the WECS will reduce the current ratings of the system [6]. The trend of MV-rated WECSs will become prevalent in the distant future because cable losses and significantly reduced [6]. [14]. Furthermore, the voltage conversion ratio (VCR) between the generator-side converter of the MV-rated WECS and the medium voltage (MV) level of the collection point of the WPP is reduced compared to their LV-rated WECS counterpart, as indicated in Table 1.4.

Based on the VCR between the generator-side converter of a LV-rated WECS and the collection point, the voltage level of the WECS must be increased about 10 times for a transformer-less connection to the 6.6kV collection point of the WPP. While a MV-rated WECS requires the voltage level of the generator-side converter to be increased between 1.65 to 2.2 times for a transformer-less connection to the 6.6kV collection point of the WPP. Therefore, the power conversion stage of a transformer-less WECS will require some level of voltage boosting between its generator-side converter and grid-side converter topologies. A conventional transformer-less WECS will be based on a three-stage power conversion stage consisting of a generator-side converter, boost converter and grid-side converter [6], [12], [14]. The complexity of a three-stage power conversion stage in a transformer-less WECS is

increased with the VCR in terms of power semiconductor devices count, clamping devices and complex control algorithms [6], [12]-[15]. This research seeks to address this issue by analysing, designing, and developing a multilevel grid-side converter topology with voltage boosting capability.

Table 1.4: List of Commercial DD-PMSG based WECS and their associated VCR between the generator-side and the collection point of the WPP.

Manufacturer/ Model No.	Power/ Voltage Rating	Current Rating	$VCR_{6.6}$	VCR_{11}	VCR_{22}	VCR_{33}
Avantis/ AV928	$2.5MW/0.69kV$	$2.1\ kA$	10	16	32	48
CCWE/ 3000-103D	$3MW/0.69kV$	$2.6\ kA$	10	16	32	48
EWT DW96	$2MW/0.69kV$	$1.7\ kA$	10	16	32	48
GE Energy GE4.1-113	$4.1MW/0.69kV$	$3.5\ kA$	10	16	32	48
IMPSA V-77	$1.5MW/0.69kV$	$1.3\ kA$	10	16	32	48
Shandong YZ113-3	$3MW/3kV$	$0.6\ kA$	2.2	3.7	7.3	11
XEMC-Darwind XD115	$4.5MW/3kV$	$0.88\ kA$	2.2	3.7	7.3	11
XEMC-Darwind XE/DD128	$5MW/3kV$	$0.97\ kA$	2.2	3.7	7.3	11
Zephyros Z72	$2MW/4kV$	$0.3\ kA$	1.65	2.75	5.5	8.25
Marvento M3.6-118	$3.6MW/3.9kV$	$0.55\ kA$	1.69	2.8	5.64	8.46
Nordex N150/6000	$6MW/3.3kV$	$1.05\ kA$	2	3.33	6.67	10

$VCR_{6.6}$ represents voltage conversion ratio between the WECS and the 6.6kV collection-point.

VCR_{11} represents voltage conversion ratio between the WECS and the 11kV collection-point.

VCR_{22} represents voltage conversion ratio between the WECS and the 22kV collection-point.

VCR_{33} represents voltage conversion ratio between the WECS and the 33kV collection-point

B. Voltage rating of the power semiconductor devices and number of clamping devices

The IGBT module frequently used in high-power applications is rated at 2.5 kV to 6.5 kV [14], [71]-[75]. The desired output voltage, efficiency, and cost are the primary considerations when selecting a power semiconductor device [71]. As discussed in Section 1.1.2, 3L-DCC topology is the most used topology in high-power WECS [12]-[14]. Therefore, a 3L-DCC topology applied to a transformer-less WECS will require several series-connected IGBT modules to operate at the MV level of the collection point [72], [73]. These series-connected IGBT modules will require additional voltage balancing techniques to ensure equal voltage distribution amongst the series-connected modules [72], [73]. However, an increase in switching and conduction losses is a usual occurrence in series-connected modules [71].

Conventional multilevel converter topologies with higher voltage levels minimized the need for series-connected power semiconductor devices [6], [12]. However, the number of clamping devices (such as capacitors, diodes, and inductors) in a higher-order multilevel topology is significant [6], [14], [31]-[36]. For example, a 3L-DCC, 4L-DCC and 5L-DCC converter topologies in a three-phase structure consist of six, eighteen, and thirty-six clamping diodes, respectively. These clamping devices require additional control methods for voltage balancing and minimization of circulating current in the converter topology [6], [14], [31]-[36]. Also, the losses associated with the converter topology is significantly increased.

Based on the generalized multilevel converter topology, the clamping devices in topology can be minimized at the derivation stage [6], [12]-[14], [31]-[36]. This research extends the generalized multilevel converter topology method to analyse emerging topologies with minimal clamping devices and minimal series-connected power semiconductor devices. A novel multilevel converter topology with minimal clamping devices and series-connected power semiconductor devices has been proposed from the analysis. Furthermore, the power losses associated with commercially available power semiconductor devices have been studied in the thesis for the emerging topologies deployed in a transformer-less WECS.

C. Minimization of DC Component

Grid-connected power converter always produces unwanted dc components due to the variation in the characteristics and switching times of its power semiconductor devices and the offset and non-linearity of the current and voltage sensors [76], [77]. The galvanic isolation existing

between the windings of the transformer minimizes the injection of dc components into the grid [63]. Therefore, a transformer-less WECS will inject about three times more dc components than a conventional WECS connected to the collection point through a wind turbine transformer [78]. Therefore, the excessive injection of dc component into the collection point of a WPP will eventually lead to the corrosion of feeder cables, the substation transformer's saturation, and inaccurate estimation of the parameters of the grid by automatic synchronization algorithms [79] [80].

According to the IEEE 1547(a)-2020 standard, the dc component injected into the grid should be less than one percent of the output current of the converter [81]. Several methods have been presented in the literature to reduce the injected dc component within its stipulated range. The most widely applied method is inserting a capacitor in series at the converter's output [77], [79]. Furthermore, another well-established approach is the current sensing and control technique which utilizes a current controller to minimize the injected dc component [79], [82], [83].

The effectiveness of these stated methods has been studied in this research work, and associated merits and demerits have been highlighted in this thesis. Based on the study, this research presents a dc component minimization technique for the proposed converter topology.

D. Cost-Effectiveness

One of the major advantages of a transformer-less WECS is the overall reduced cost from the system-level perspective [14]. However, the cost associated with the power conversion stage of a transformer-less WECS is increased when compared with the power conversion stage of a conventional WECS [6], [14]. Based on the additional functionality of the power conversion stage in a transformer-less WECS, the higher multilevel converter topology and additional control algorithm extend the cost of the power conversion stage.

In section 1.1.2, the different conventional multilevel converter topologies deployed in the back-to-back power conversion stage of a conventional WECS have been highlighted. However, the component counts of these topologies will increase significantly in a transformer-less WECS [14]. Therefore, the associated cost of the power stage of a transformer-less WECS should be less than the cost of a wind turbine transformer. Furthermore, the cost-benefit analysis of deploying transformer-less WECSs in a WPP must be studied.

1.2.2. Research Questions

According to the highlighted issues from the previous section, this research work seeks to address the following questions:

- **What are the existing power converter configurations of a transformer-less WECS connected via a grid-side filter to the collection point of a WPP?**
- **What is the cost-benefit advantage of adopting a transformer-less WECS as compared to a conventional WECS?**
- **What type of power converter configuration is more suitable for a transformer-less WECS, which can effectively mitigate the drawbacks identified in the existing structure, such as excessive clamping devices, and multiple series-connected power semiconductor devices?**
- **What is the most appropriate technique for minimizing the injected dc component in a three-phase transformer-less WECS?**

1.3. Research Objectives

Based on the highlighted research questions in section 1.2.2, the objectives of the research work are summarized as follows:

- Review existing power converter configurations and discuss their features and drawbacks for transformer-less WECS applications.
- Carry out a cost-benefit analysis of the proposed power converter configuration and existing power converter configuration of a transformer-less WECS.
- Design and develop a novel single-stage grid-side power converter with minimal series-connected power semiconductor devices, minimal clamping devices, and voltage boosting capability.
- Develop an experimental testing rig for verification based on a power hardware-in-loop (PHIL) configuration.

1.4. Thesis Outline

The presented research work is organized into seven chapters. The work carried out in each chapter is summarized as follows:

Chapter-1: An overview of reliability studies on WECS is presented with additional discussion on DD-PMSG, power converter topologies, and electrical subsystem of high-power WECS. The design challenges for deploying a multilevel converter topology at the grid-side of the power converter configuration of the transformer-less WECS.

Chapter-2: This Chapter presents a comprehensive review of existing power converter configurations for transformer-less WECS. These configurations are grouped into the following categories, namely: generator-converter configuration and three-stage power converter configuration. The operating principles, advantages, and drawbacks of these power converter configurations are presented in this chapter. Furthermore, the cost-benefit analysis of a WPP with transformer-less WECS is studied using the life-cycle cost analysis of the existing power converter configurations and collection systems of a WPP.

Research Outputs from Chapter 2:

Journal Paper Published:

Akinola A. Ajayi-Obe, M. A. Khan, and P. Barendse, "Techno-Economic Evaluation of Five-Level Nested Neutral Point Clamped (NNPC) Converter Topology for Transformer-less Connection of High-Power Wind Energy Conversion Systems" Journal of Energy in Southern Africa (JESA), Vol. 3, No. 3, pp.33-43, August 2019.

Conference Papers Presented:

Akinola A. Ajayi-Obe, M. A. Khan, and P. Barendse, "Techno-Economic Evaluation of Five-Level Nested Neutral Point Clamped (NNPC) Converter Topology for Transformer-less Connection of High-Power Wind Energy Conversion System" WindAC 2018, Cape Town, South Africa, 5^{th} – 6^{th} November 2018.

Akinola A. Ajayi-Obe, M. A. Khan, and P. Barendse, "Comparative Evaluation of Transformer-less Configurations for Wind Energy Conversion Systems" WindAC 2017, Cape Town, South Africa.

Chapter-3: In this chapter, the generalized multilevel converter topology method for deriving a four-level Nested Neutral-Point-Clamped (4L-NNPC) and five-level NNPC (5L-NNPC) converter deployed as the grid-side converter topology of a transformer-less WECS is presented. Furthermore, combining the generalized multilevel topology method and the parallel-series cell method to derive a seven-level Modified Nested Neutral-Point-Clamped (7L-MNNPC) converter topology is discussed extensively. Simulations are used to verify the presented theoretical analysis and design for the 4L-NNPC, 5L-NNPC and 7L-MNNPC topologies. Furthermore, the grid-connection scenarios of deploying a transformer-less WECSs in a WPP are studied and verified through simulations.

Chapter-4: This chapter presents the proposed tapped inductor quasi-Z-source (qZS)-NNPC converter topology. The theoretical derivation, steady-state analysis, design of the tapped inductor is discussed. The proposed modulation technique and voltage balancing control technique of the proposed converter topology are discussed. The implementation of these techniques on a field-programmable gate array (FPGA)-based platform is presented. The feasibility of the proposed converter topology and the FPGA realization for the modulation and voltage balancing control techniques are verified through the developed experimental test rig.

Research Outputs from Chapter 4:

Akinola A. Ajayi-Obe, and M. A. Khan, "Analysis and Design of a Quasi-Proportional-Resonant Based Voltage Balancing Control for Grid-Connected Nested Neutral Point Clamped Converter" in IEEE-Energy Conversion Congress Exposition (ECCE) 2018 Proceeding, pp. 2982-2987, December 2018.

Akinola A. Ajayi-Obe and M. A. Khan, "Analysis of a Five-Level Dual Tapped Inductor Quasi Impedance Source-Nested Neutral Point Clamped Converter" in IEEE-Energy Conversion Congress Exposition (ECCE) 2017 Proceeding, pp. 2150-2155, November 2017.

Chapter-5: The proposed modified voltage filtering technique reduces the dc component produced by the proposed converter topology. Analysis, design, and experimental results are presented to verify the method.

Chapter-6: In this chapter, the development of power hardware-in-loop (PHIL) configuration for the experimental verification of the proposed converter topology is discussed. Furthermore, the prototyping process and grid connection of the proposed converter topology is presented.

The efficiency and cost-benefit analysis of the proposed converter topology are discussed in detail compared to a three-stage power converter configuration.

Chapter-7: The main contributions of the conducted research are summarized in this chapter. Therefore, the main contributions of this presented work are stated as follows:

- A comprehensive overview of the existing power converter configurations for transformer-less WECS was carried out. Furthermore, a comparative benchmark factor was developed to evaluate the topologies deployed in these configurations; MMC-based topologies are less efficient and reliable because of their high number of power semiconductor devices, while higher voltage-level DCC topology combined with simple voltage boosting topology is more efficient and reliable for a transformer-less WECS.
- Theoretical derivations and simulation results of a three-phase four-level NNPC, five-level NNPC and seven-level MNNPC converter topologies deployed as the grid-side converter topology of a transformer-less WECS have been presented. Furthermore, the severity of the grid voltage unbalances (i.e., voltage sag) on the transformer-less WECS have been studied and investigated.
- Analysis, design, and development of a three-phase five-level tapped inductor quasi-Z-source-NNPC converter topology. The proposed converter topology is more efficient and more cost-effective than the conventional converter topology used in a transformer-less WECS.

Chapter 2

Power Converter Configuration Overview and Cost-Benefit Analysis

This chapter highlights the functions of a wind turbine transformer and presents an extensive overview of the power converter configurations deployed in the existing transformer-less WECS. These current power converter configurations are evaluated based on the conventional functions of a wind turbine transformer. Therefore, this chapter is organized as follows: the functions of a wind turbine transformer in a conventional WECS is discussed in Section 2.1. The classification of power converter configurations is presented in Section 2.2. Furthermore, the comparative evaluation of the power converter configurations is discussed in Section 2.3. Finally, the cost-benefit analysis of deploying a transformer-less WECS is presented in Section 2.4.

2.1. Functions of Transformers in a WPP

The main functions of the transformer in a WPP are as follows:

- Voltage level transformation.
- Grounding.
- Voltage sag transformation.
- Minimization of dc component.

A. Voltage level transformation

The primary function of a transformer is the voltage transformation of the WECS from its LV level to the MV level of the collection point [6], [48]-[50]. The majority of WECS are still rated at $690\ V$, while the voltage of the collection point is within $6.6\ kV$-$34.5\ kV$[6]. During the voltage transformation, associated losses are produced by the transformer [6], [14].

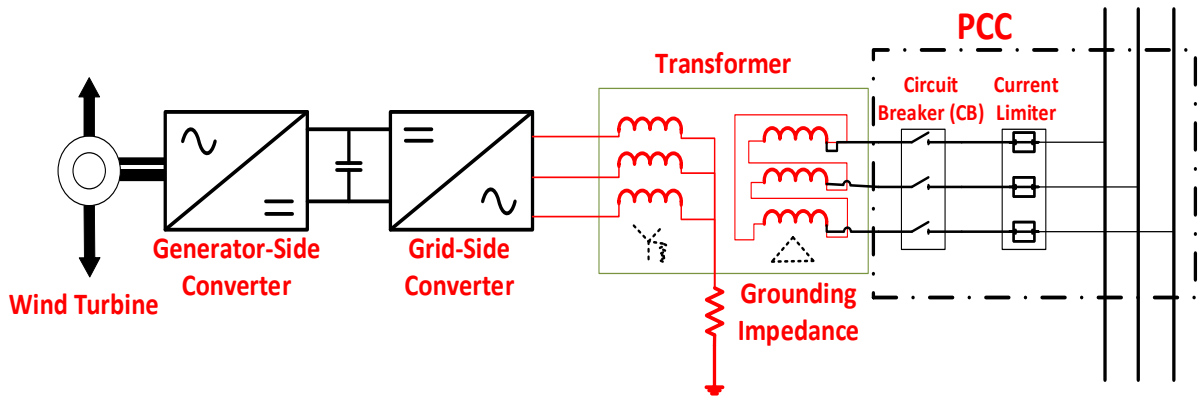


Figure 2.1: A grid connected WECS with its transformer winding connection.

B. Grounding

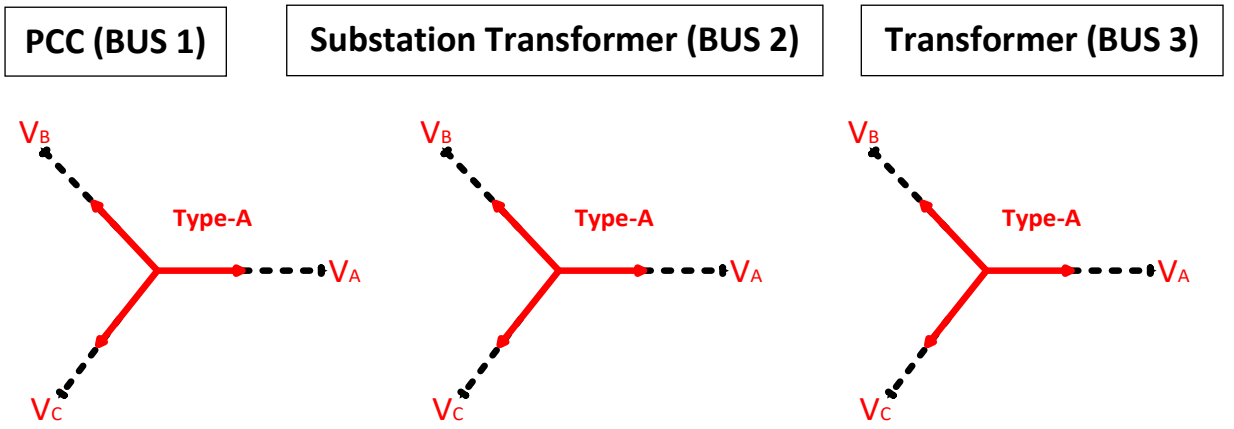
A typical transformer used in a WECS comprises a grounded wye/delta winding connection [48], [49]. The grounded wye winding connection provides the low impedance path for fault current [51]. Therefore, excess fault electric current can be transmitted efficiently to the ground without causing much damage to sensitive components and personnel working on the WPP [52]-[54]. The winding connection of the transformer of a conventional WECS is shown in Figure 2.1.

C. Voltage sag transformation

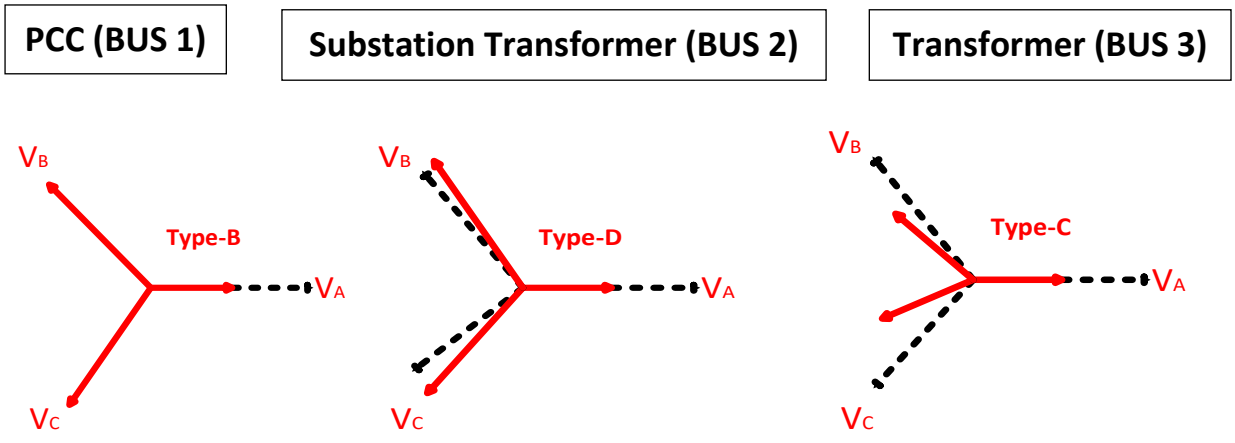
Existing grid codes for grid connected WPP stipulates that the WPP must maintain its connection to the grid whenever a voltage sag occurs [6], [55]. The original voltage sags that arise due to short circuit faults in the grid are Types A, B, C, and E [49], [55]-[57]. The other types of voltage sags (i.e., Type D, Type F, and Type G) are derived from the original sag based on the transformer winding connections that exist between the fault location and the terminal of the WECS [49], [55]-[57]. A conventional WPP consists of two types of transformers: substation transformer and the transformer used in the WECS [48], [49], as shown in Figure 1.9. The transformer winding connections are selected based on the need to provide adequate grounding and effective zero-sequence component isolation from the original fault [48], [49]. While the substation transformer is made up of the grounded-wye/grounded-wye/delta connection ($Y_g\Delta Y_g$) [48]. While the transformer consists of two winding connections, which is the grounded wye/delta (ΔY_g) [48], [49], as shown in Figure 2.1. Due to the presence of the delta winding connections in both transformers, the zero-sequence component from Types B and E sags is eliminated [49], [55]-[57]. These sags are then transformed into other types of sags, as illustrated in Figure 2.2. Moreover, the magnitude, duration, and phase angle jump

define each voltage sag [55]-[60]. In Figure 2.2, the phasor diagram of each voltage sag is shown with their respective magnitude and phase angle jump. The transformer windings connection helps sustain the magnitude of the voltage within one-third of its initial value, even if the voltage sag with its magnitude being zero appeared on its secondary winding [56].

The phase angle jump is affected by the impedance of the transformer, substation transformer, and feeder cables of the WPP [55], [57]. From Figure 2.3, source impedance (Z_s) is the high-voltage transmission/distribution network of the grid, while the feeder impedance (Z_f) is a combination of feeder cables and substation transformer [55], [57]. Therefore, Z_s is greater than Z_f in a conventional WPP; the difference between the X_s/R_s ratio of the Z_s and the X_f/R_f ratio of the Z_f is increased in a transformer-less configuration, which results in a significant phase angle jump when asymmetrical voltage sags occur [55]-[62]. An overshoot of about 60% and 40% was observed on the dc-link voltage and grid current during asymmetrical sags [57]. Further discussion on the impact of the presented voltage sags on a transformer-less WECS is presented in Section 3.4.2 of Chapter 3.



(a)



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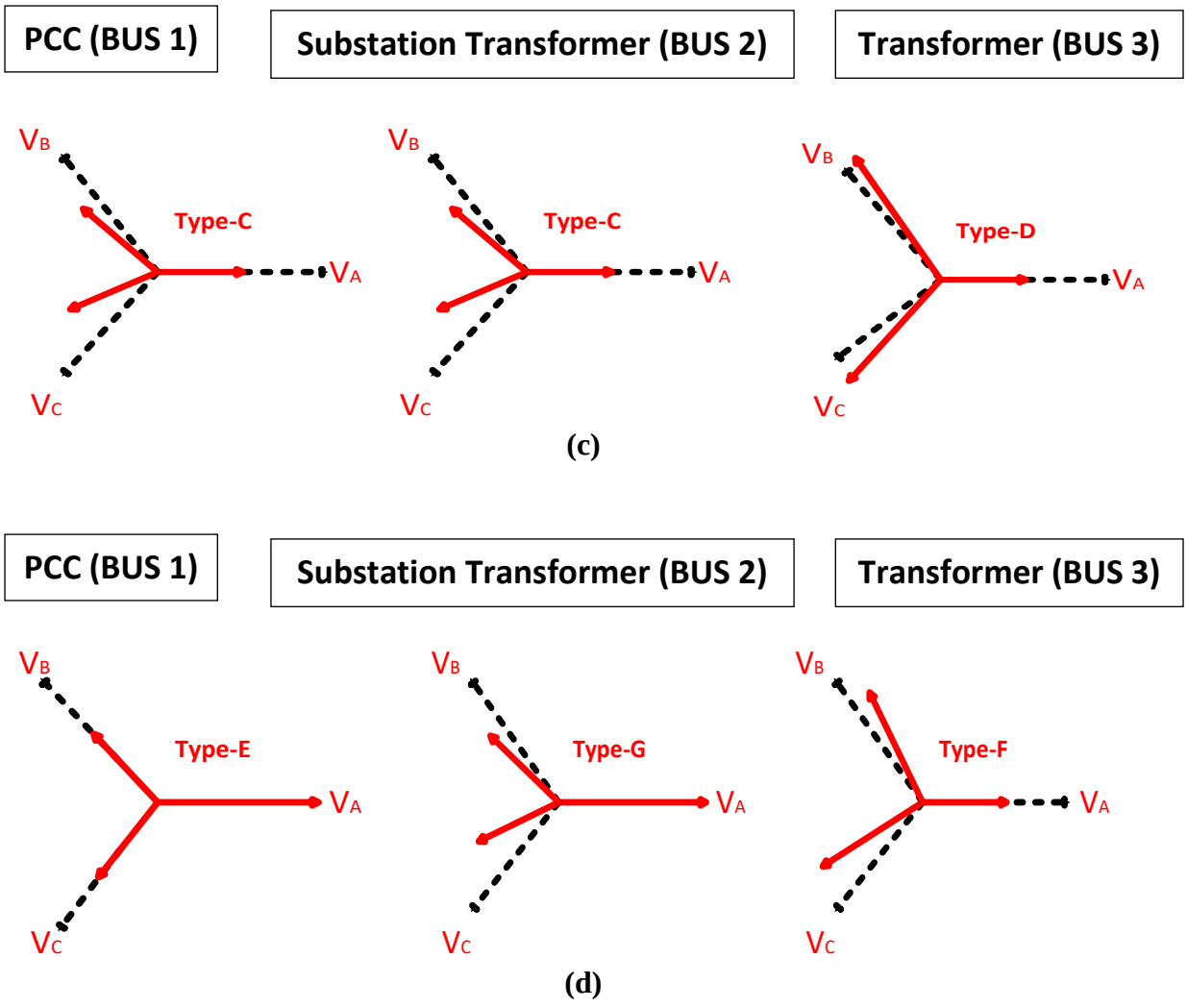


Figure 2.2: Phasor diagram of different voltage sags transformation from PCC to transformer in a WECS. (a) Type-A sag at PCC transformed to Type-A at transformer terminal, (b) Type-B sag at PCC transformed to Type-C at transformer terminal, (c) Type-C sag at PCC transformed to Type-D at transformer terminal, and (d) Type-E sag at PCC transformed to Type-F at transformer terminal.

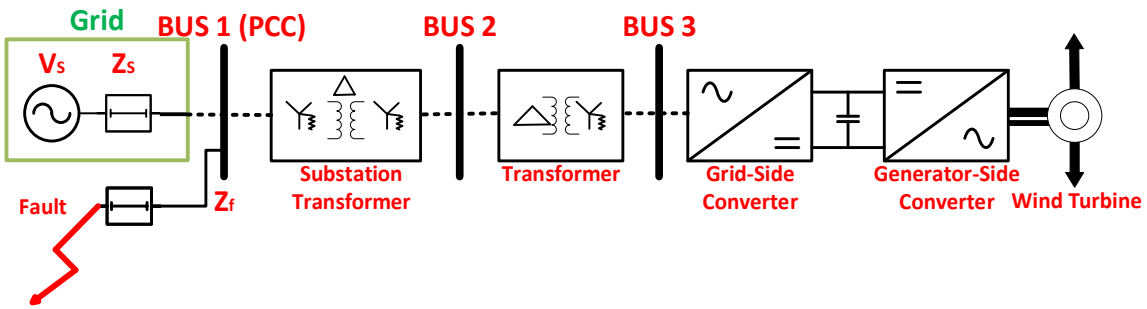


Figure 2.3: A conventional WPP model with a short circuit fault at PCC.

D. Minimization of DC component

The galvanic isolation between the grounded-wye primary windings and the secondary windings will minimize the injected dc component from WECS into the grid [63]. The minimization of the dc component with a wind turbine transformer has been previously discussed in Section 1.2.1.

2.2. Classification of Power Converter Configurations

The power converter configurations are classified into two categories, namely: generator-converter configuration and three-stage power converter configuration, as illustrated in Figure 2.4. The generator-converter configuration consists of a modular structure of multiple isolated generator coils and MMC topology, which allows the cascading of the modules to the required MV level of the collection point in a WPP [84]-[87]. The three-stage power converter configuration consists of a conventional electric generator and a three-stage power conversion that boost the voltage level of the generator-side converter to the MV level of the grid-side converter [88]-[90].

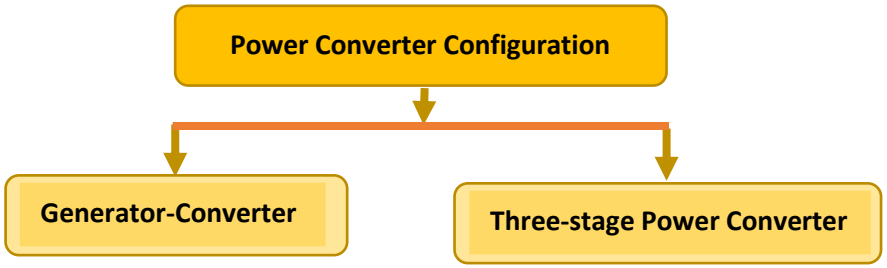


Figure 2.4: Classification of power converter configurations.

2.2.1. Generator-Converter Configuration

An air-cored DD-PMSG (A-DD-PMSG) is used in the generator-converter configuration because the iron core in the generator stator is replaced with composite material to produce a lightweight generator for high-power WECS [84]-[87]. A significant drawback associated with eliminating the stator iron core is reducing the airgap flux density, which lowers the shear stress and torque producing capability of a generator [84], [85]. The required torque will be generated by increasing the diameter of an A-DD-PMSG [84], [85]. The relationship between mechanical torque (T_m) and the output power of the WECS is expressed in (2.1) to (2.4) as follows:

$$P_{WECS} = 0.5 \cdot \rho \cdot v^3 \cdot \pi r^2 \cdot C_p \tag{2.1}$$

$$\omega_{WECS} = \frac{v \cdot \beta_s}{r} \tag{2.2}$$

$$T_m = \frac{P_{WECS}}{\omega_{WECS}} \tag{2.3}$$

$$\therefore, T_m = \frac{0.5 \cdot \pi \cdot \rho \cdot v^2 \cdot r^3 \cdot C_p}{\beta} \tag{2.4}$$

where ρ is the air density (kgm^{-3}), v is the wind speed (ms^{-1}), r is the radius (m), C_p is power coefficient, β_s is the tip speed ratio and ω_{WECS} is the rotational speed. Theoretical, the electric generator will produce the same amount of electrical torque (T_e) as the mechanical torque (T_m). The relationship between the electrical torque (T_e), shear stress(σ_e) and length of the air gap(l_e) is expressed in (2.5) [84].

$$T_e = \sigma_e \cdot 2\pi r^2 \cdot l_e \tag{2.5}$$

The power conversion stage of the generator-converter configuration is based on an MMC topology [86], [87]. A module of the MMC topology is made up of the generator-side converter and grid-side converter topologies, as shown in Figure 2.5. The stator coils of the generator are connected directly to the generator-side converter [86], [87]. Therefore, the stator coil voltage is rectified through the generator-side converter topology, as illustrated in Figure 2.5. The generator-side converter topology can either be a single-phase (1ph) diode rectifier or an active rectifier. In contrast, the grid-side converter topology can either be a 1ph H-bridge topology or a 1ph three-level DCC (3L-DCC) H-bridge topology [86], [87]. These modules are cascaded to the MV level of the collection point [86], [87]. The different types of generator-converter configurations presented in the literature can be further classified based on the power conversion stages in each configuration as follows: three-stage generator-converter configuration and two-stage generator-converter configuration [86], [87].

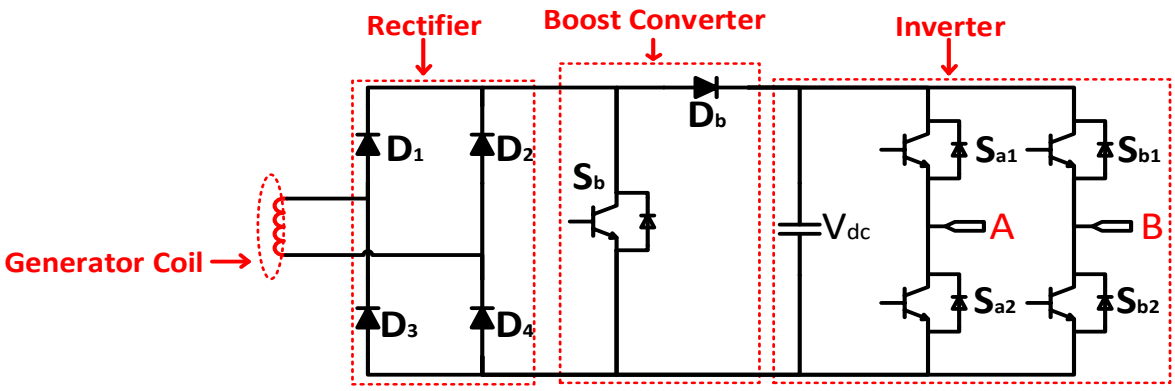


Figure 2.5: A three-stage generator-converter module.

A. Three-Stage Generator-Converter Configuration

This configuration is based on the connection of a three-stage generator-converter module in each phase [86], as shown in Figure 2.6. A multiphase, lightweight, iron-less stator, modular PM generator is deployed in each module [85]-[86]. The PM generator is a six-phase (6ph), multiple poles direct-drive, with a dual-three phase winding arrangement consisting of a 30 degrees displacement between each phase of the winding structure [86], [91], as illustrated in Figure 2.7.

The utilization of a 6ph PM generator enables the fault-tolerance capability and improves the efficiency of each module [84]-[87], [91]. Due to the direct-drive composition of the generator-converter configuration the stator frequency is rated at about $15\ Hz$ [6], [26]-[28], [86]. This low stator frequency results in ac components being prevalent at the generator-side converter output resulting in torque pulsation [86]. These ac components can be eliminated through the dual-three phase winding arrangement because a pair of the stator coils with 90 degrees displacement is fed to the input of the 1ph rectifier [86]. A three-stage generator-converter module is made up of a 1ph diode rectifier, a single-switch boost converter, and either a H-bridge inverter topology or a 3L-DCC H-bridge inverter topology [86], as illustrated in Figures 2.8(a) and 2.8(b), respectively. Due to the dual-three phase winding arrangement, each module comprises a pair of 1ph diode rectifiers and a single-switch boost converter [86]. The stator coil voltages are rectified through the 1ph diode-rectifier, while the single-switch boost converter ensures that the dc-link voltage is stabilized and free of voltage ripples [86].

The pair of diode rectifiers and single-switch boost converter can be connected to the dc-link either through a series or parallel connection, based on the type of inverter topology deployed in the module [86], as illustrated in Figures 2.8(a) and 2.8(b) respectively. The relationship between the series connection of a pair of diode rectifiers and a single-switch boost converter and the dc-link voltage of the generator-converter module is expressed in (2.6) to (2.8).

$$V_{dc\_s} = V_{o,cell1} + V_{o,cell2} \tag{2.6}$$

$$V_{o,cell1} = V_{o,cell2} = V_{o,cell} \tag{2.7}$$

$$\therefore, V_{dc\_s} = 2V_{o,cell} \tag{2.8}$$

where V_{dc_s} is the dc-link voltage of series-connected pair of a diode rectifier and single-switch boost converter, $V_{o,cell1}$ is the output voltage of the upper diode rectifier and single-switch

boost converter, and $V_{o,cell2}$ is the output voltage of the lower diode rectifier and single-switch boost converter.

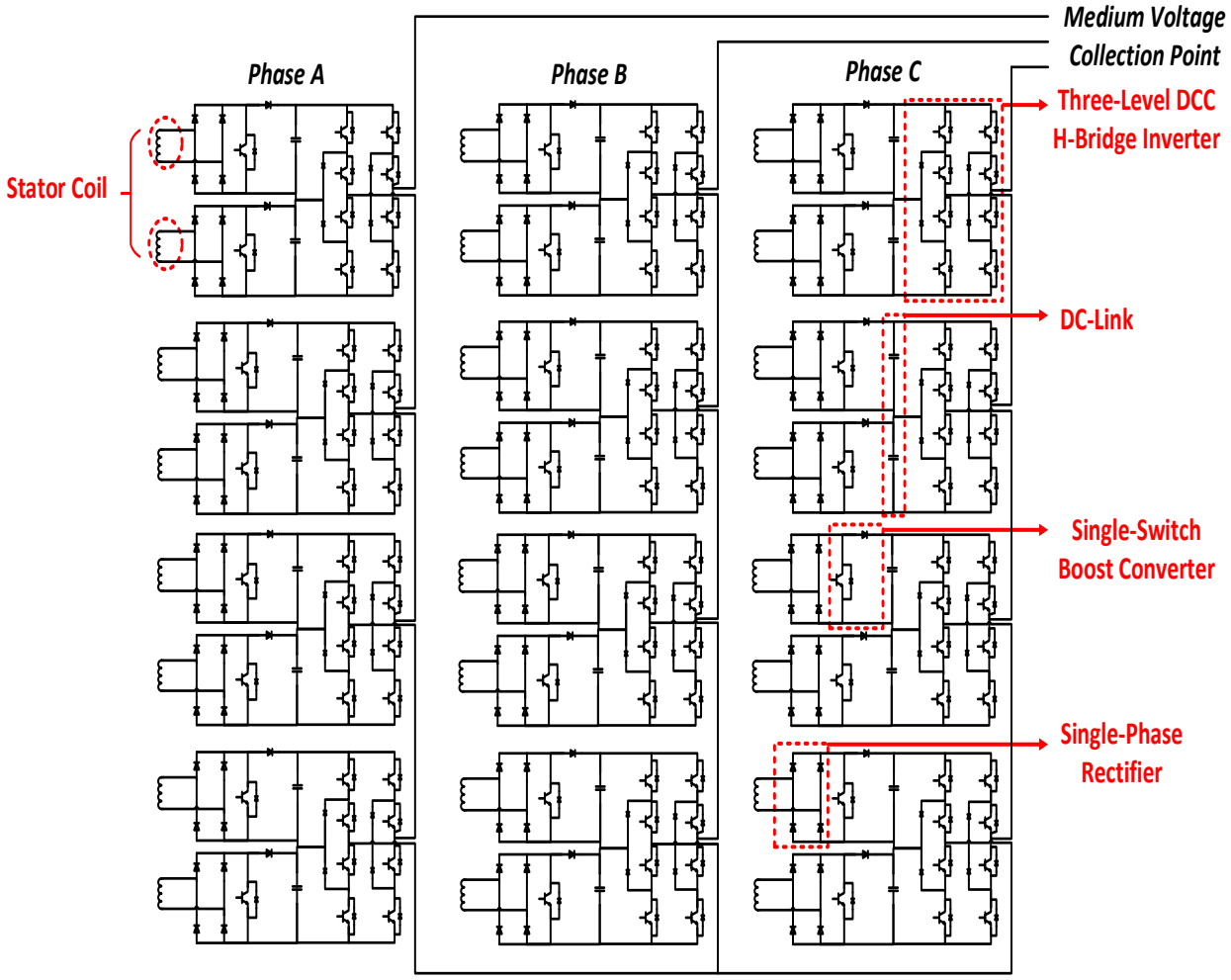


Figure 2.6: A 3ph three-stage generator-converter configuration.

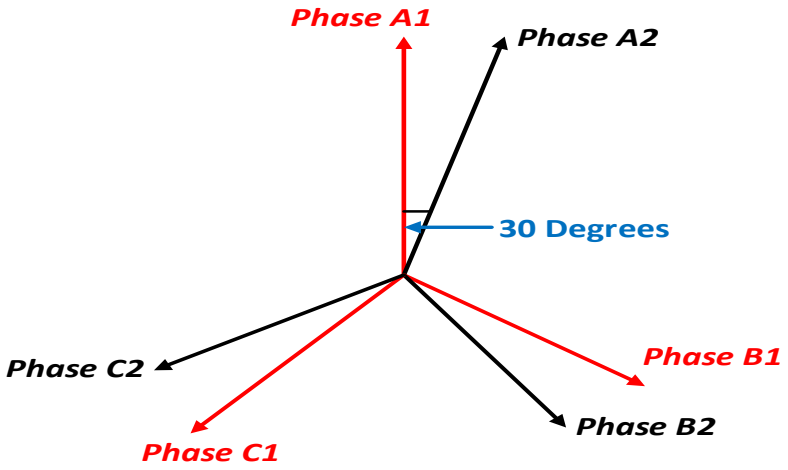
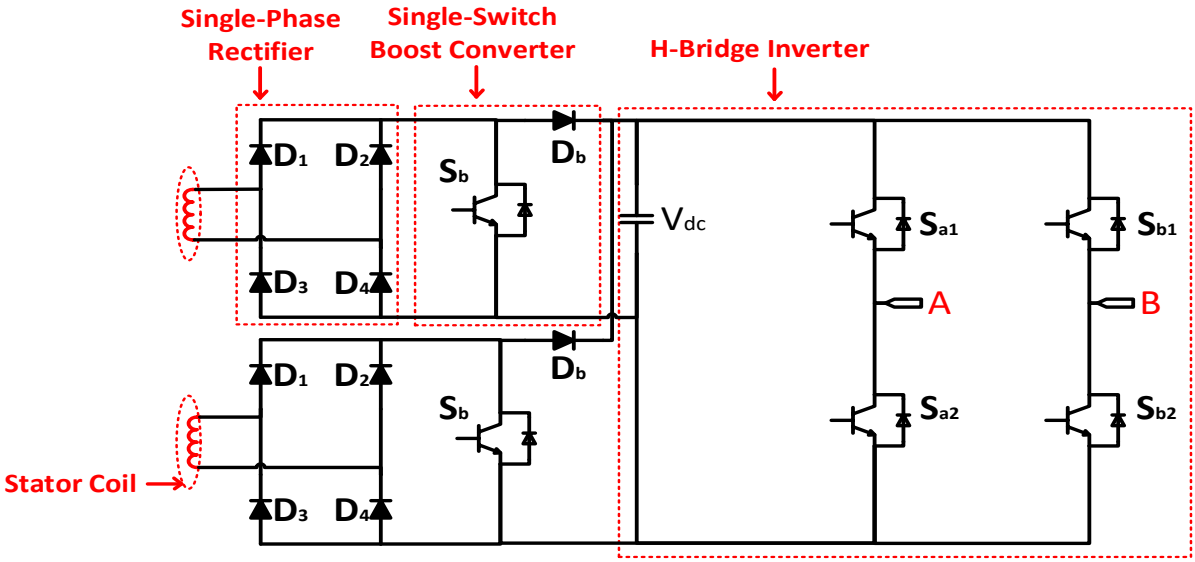
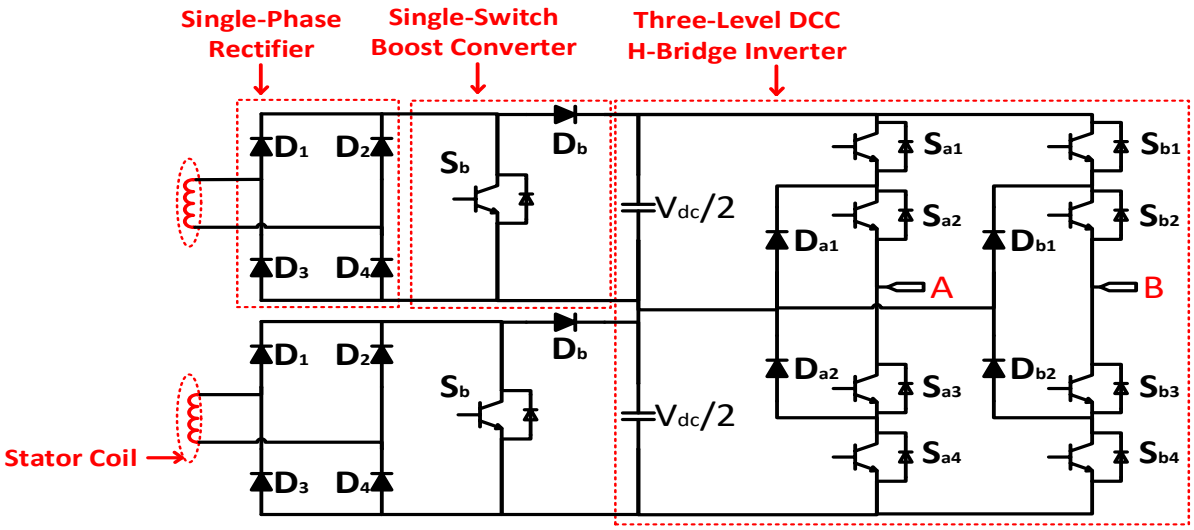


Figure 2.7: Dual three-phase winding arrangement of a 6ph PM generator.



(a)



(b)

Figure 2.8: Converter module with two stator coils connected in parallel or in series and the corresponding rectifier and inverter topology. (a) Parallel rectifier and a H-bridge inverter topology. (b) Series rectifier and a three-level DCC H-Bridge inverter topology.

In Figure 2.8(a), the two stator coils and their respective single-switch boost converters are connected in parallel with the generator side supplying constant power to the dc-link capacitors [86]. Alternatively, the two stator coils and their respective single-switch boost converters are connected in series with the dc-link capacitors, which implies the size of the dc-link is double the previous structure as shown in Figure 2.8(b). Therefore, the structure in Figure 2.8(b) can adopt a three-level DCC H-bridge inverter at the grid-side of the module [86]. The main advantage of deploying the structure in Figure 2.8(b) is that the dc-link voltage of each module

is doubled. Therefore, the number of modules required to reach the medium voltage level of the collection point is reduced by half when compared to the structure in Figure 2.8(a).

A significant drawback of this configuration is the complexity of its generator insulation [86]. Three-layered insulation (strand, turn, and ground insulations) is required due to the adopted form-wound coil at the generator stator because the coil turns are square or rectangular-shaped and arranged with precision to minimize the potential difference between the turns [86], [92]. Therefore, ground-wall insulation is more susceptible to electrical stress [92]. The special stator winding arrangement increases the cost of three-stage generator-converter configuration.

B. Two-Stage Generator-Converter Configuration

This configuration is based on a two-stage generator-converter modules in a 3ph system [87], as shown in Figure 2.9. A two-stage generator-converter module is made up of a 1ph active rectifier and H-bridge inverter, respectively [87], as illustrated in Figure 2.10.

This parallel connection of the active rectifiers requires a lower dc-link voltage when compared to the three-stage generator-converter alternative. As a result, more modules are cascaded to reach the MV level of the collection point when compared to the three-stage generator-converter configuration [86], [87]. The modules of the structure are connected in a 3ph star (wye) connection with a common ground to ensure the detection types E, F, and G voltage sags [54]-[59], [87]. The drawbacks of this configuration are the same as the three-stage generator-converter configuration discussed previously [86], [87].

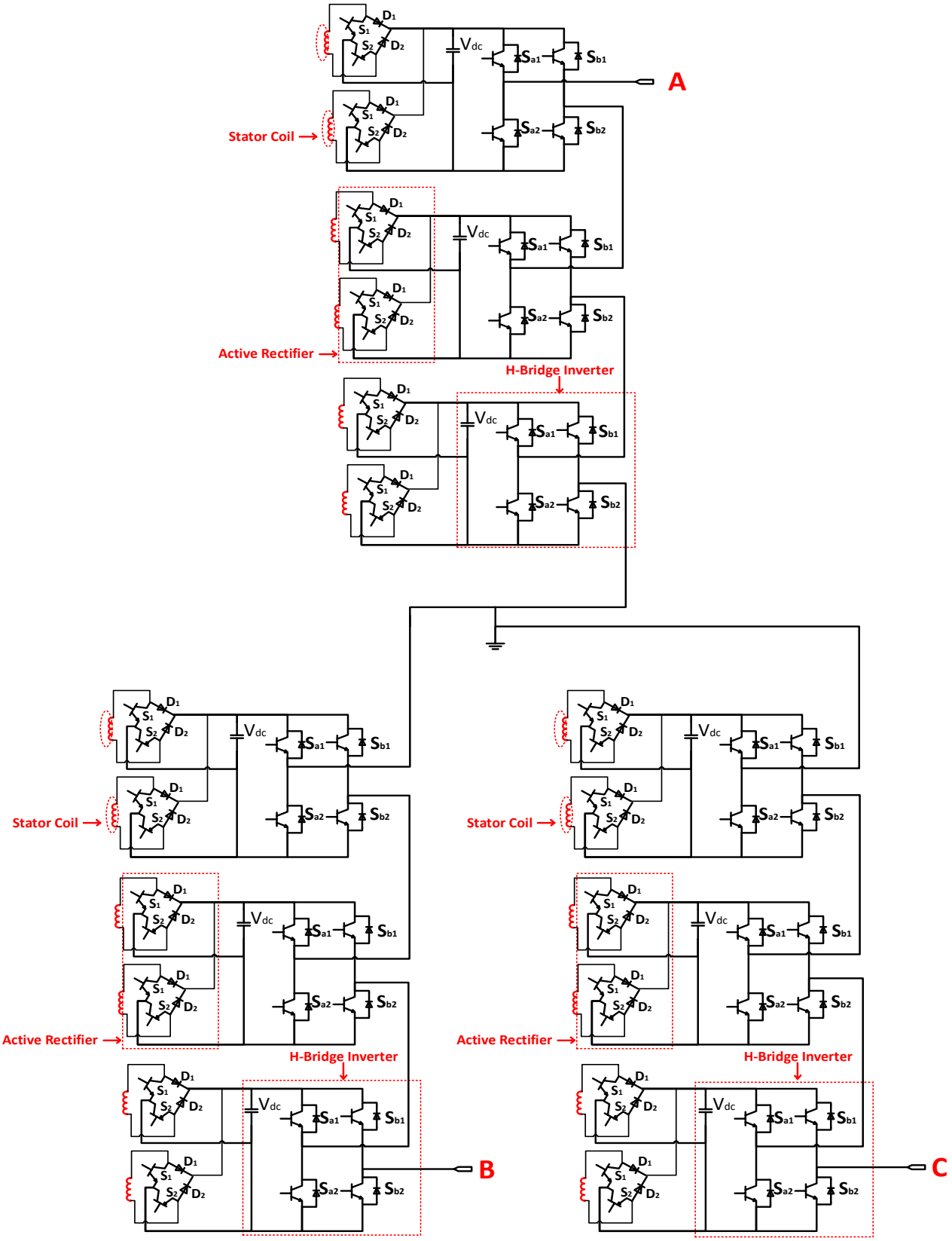


Figure 2.9: A 3ph two-stage generator-converter configuration.

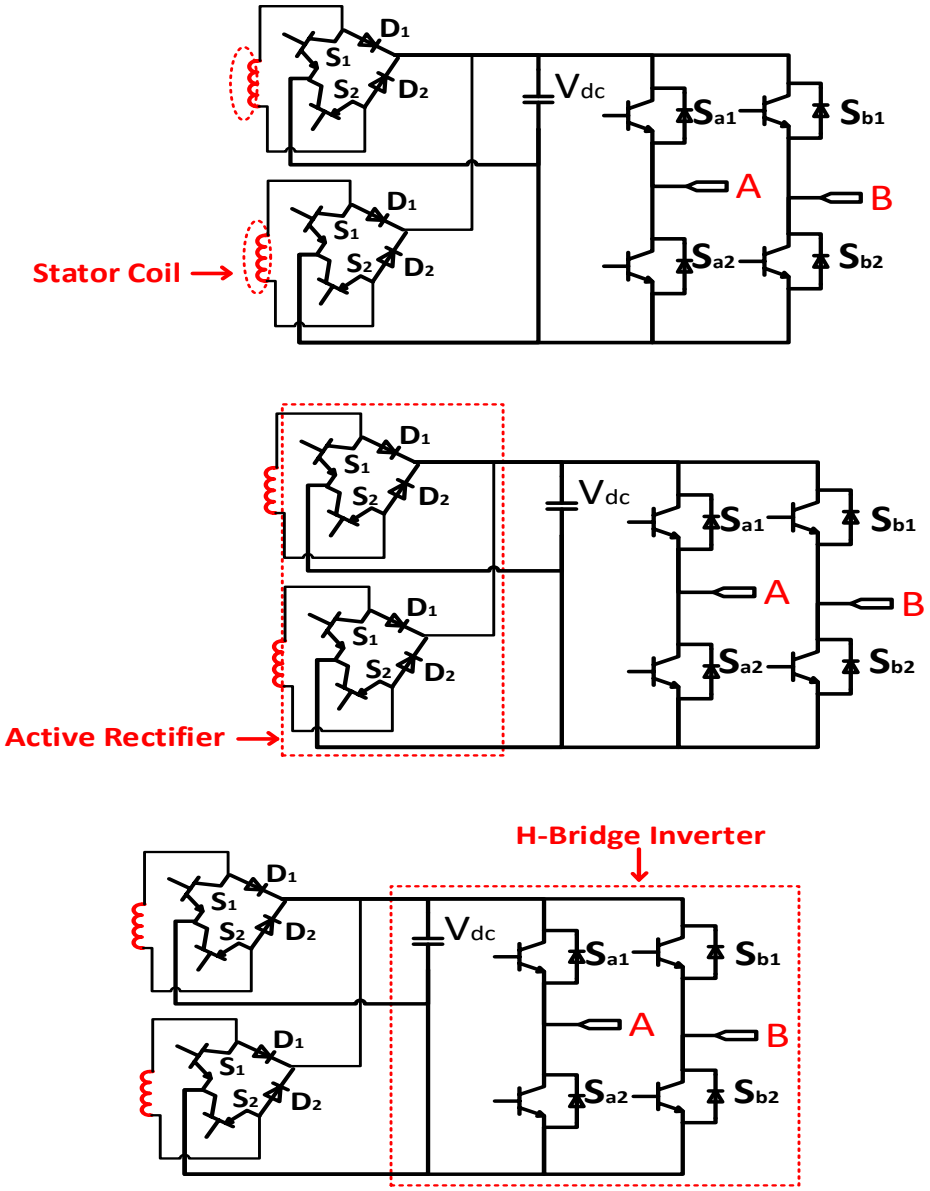


Figure 2.10: A two-stage generator-converter module.

2.2.2. Three-Stage Power Converter Configuration

This configuration allows the use of conventional DD-PMSG in the WECS [88]-[90]. The three-stage power converter configuration consists of the generator-side converter topology, an intermediate boost stage topology, and a grid-side converter topology [88]-[90]. The different types of three-stage power converter configurations discussed in this section are as follows: passive generator-side with a four-level dc-dc converter (4L DC-DC) and four-level DCC (4L-DCC) configuration, high frequency-link multilevel cascaded medium voltage converter

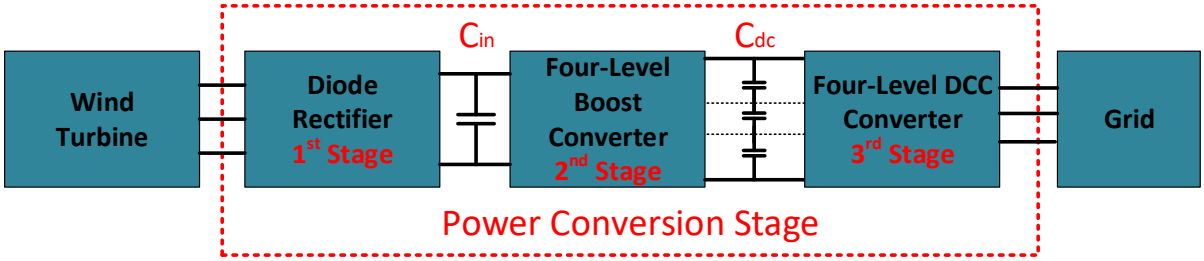
configuration, and two-level voltage source converter (2L-VSC) with modular switched-capacitor (MSC) based resonant converter and three-level DCC (3L-DCC) configuration.

A. Passive Generator-Side with 4L DC-DC Converter and 4L-DCC

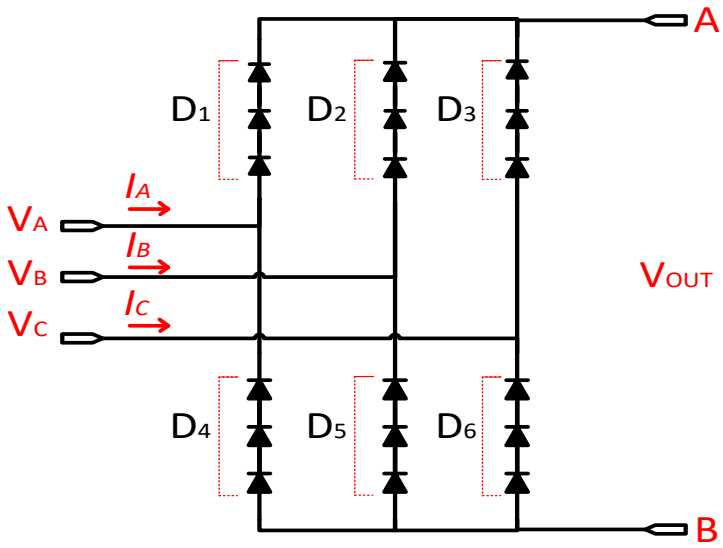
Due to the unidirectional power flow in DD-PMSG-based WECS, a simple diode rectifier is deployed on the generator side, as shown in Figure 2.11 [88]. The intermediate boost stage is made up of a 4L DC-DC converter, and a 4L-DCC topology is deployed in the grid-side converter [88], as illustrated in Figure 2.11. The diode rectifier is deployed in the WECS to reduce the cost and complexity [88]. A significant drawback of the diode rectifier is the presence of low-order harmonics in the stator current of the generator, which results in misalignment of the shaft [14], [88], [93]. This drawback can be mitigated by using a look-up table to determine the reference point of the generator-side converter and using a linear controller to regulate the ripples [93].

The main advantage of a 4L DC-DC converter is the reduced voltage rating of the power semiconductor devices, rated at one-third of the converter output voltage [94]. In Figures 2.12(a) to 2.12(e), the five different modes of operation of the 4L DC-DC converter topology are illustrated. The input voltage (V_{in}) represents the output voltage of the generator-side converter, which is the source of the 4L DC-DC converter topology, the input inductors (L_1 and L_2) represents the boost inductance of the converter, the output capacitors (C_1 to C_3) of the converter represents the dc-link capacitors of the 4L-DCC topology and the load resistors (R_1 to R_3) represents the topology, as illustrated in Figures 2.12(a) to 2.12(e). The branch of the 4L DC-DC converter topology circuit highlighted in red; shows the current path through the circuit during different switching states, the black branch of the circuit shows the non-conducting components of the circuit, and the blue branch of the circuit shows the current path in the RC network [88], [94], [95]. One of the demerits of the 4L DC-DC converter is the uneven distribution of power losses in the IGBT and diode modules because S_1 and S_3 are switched ON simultaneously in four of the five modes of operation [88], [94], [95], as illustrated in Figures 2.12(a) to 2.12(d). Therefore, this drawback reduces the power utilization of the IGBT modules [39], [71]. Another disadvantage of the 4L DC-DC converter topology is the output capacitor voltage unbalance due to the associated switching states of the IGBT modules. Furthermore, the capacitor voltage balancing scheme presented in the three-stage power converter configuration shown in Figure 2.11 is directly dependent on the switching states of the 4L DC-DC converter [88], [94], [95]. A model predictive control strategy was

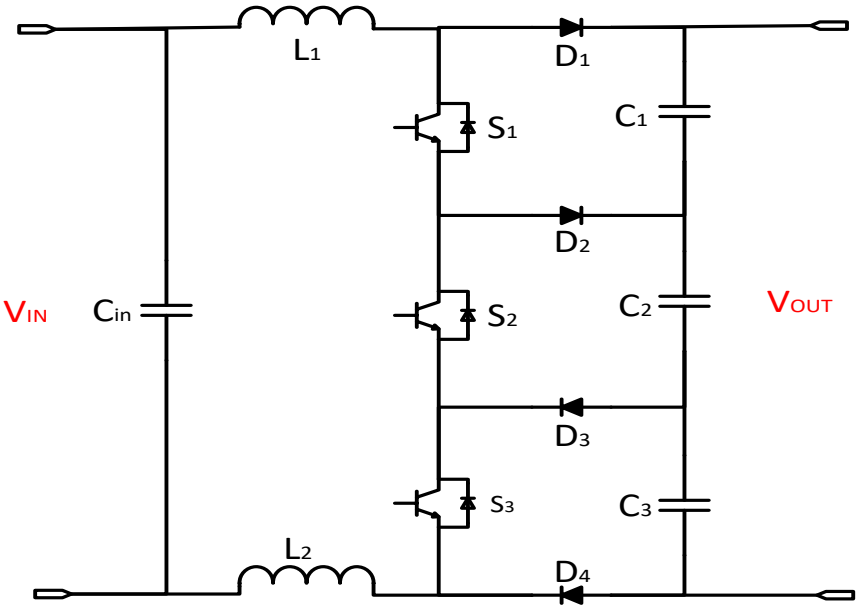
deployed to regulate the 4L DC-DC boost converter and 4L-DCC topology [88], [95], [96]. However, the variable switching frequency of the model predictive control strategy results in increased harmonics in the output current [97].



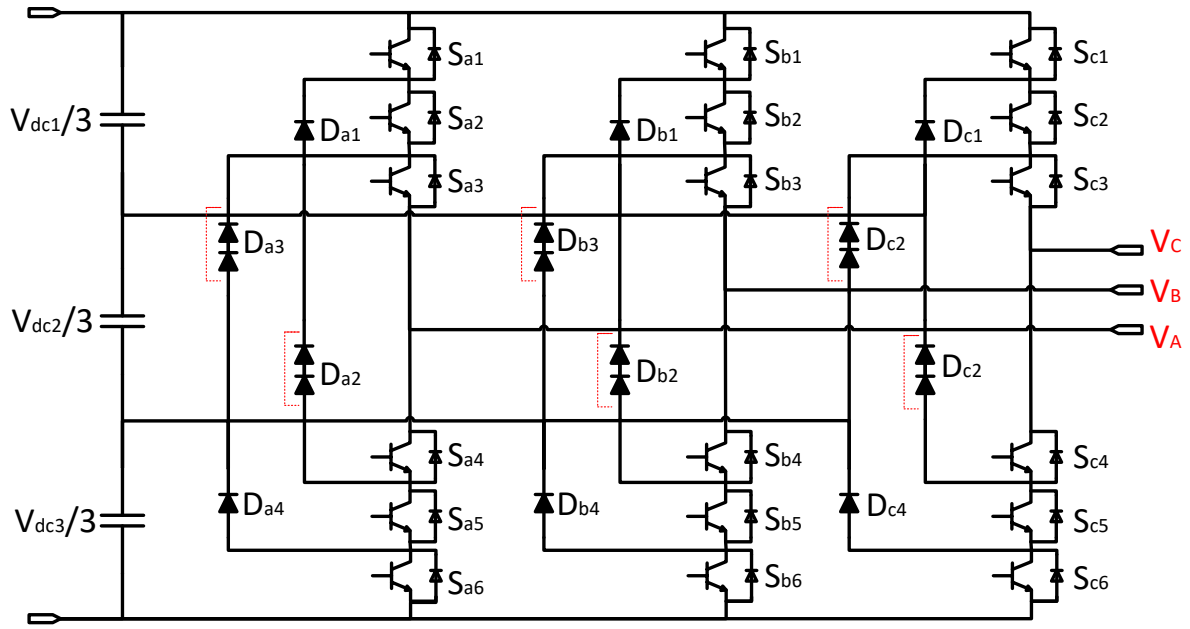
(a)



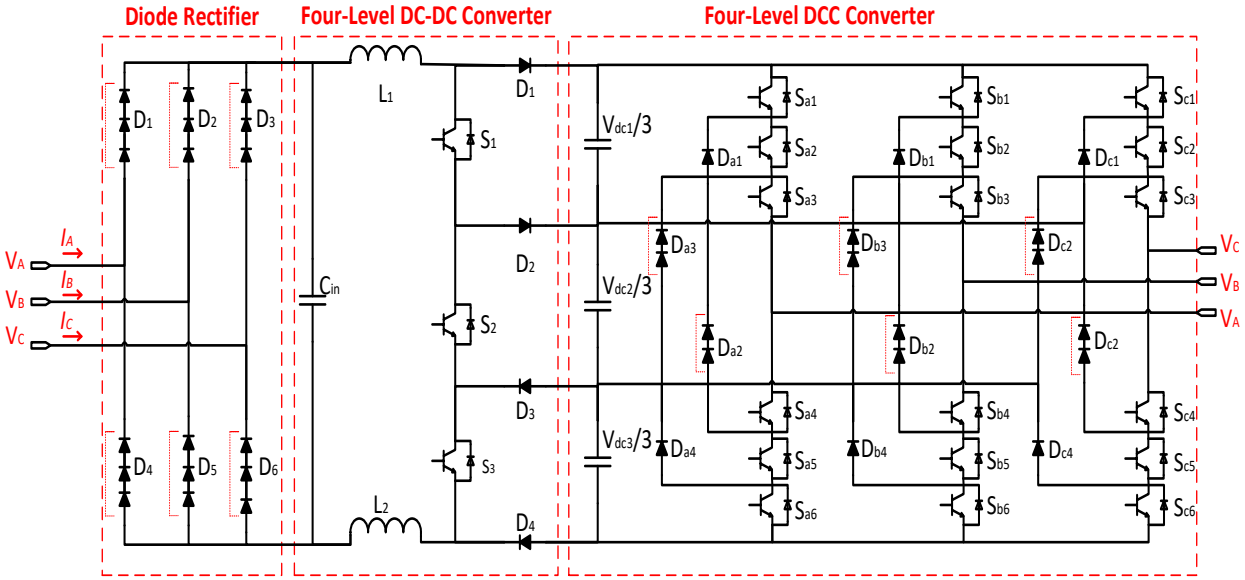
(b)



(c)

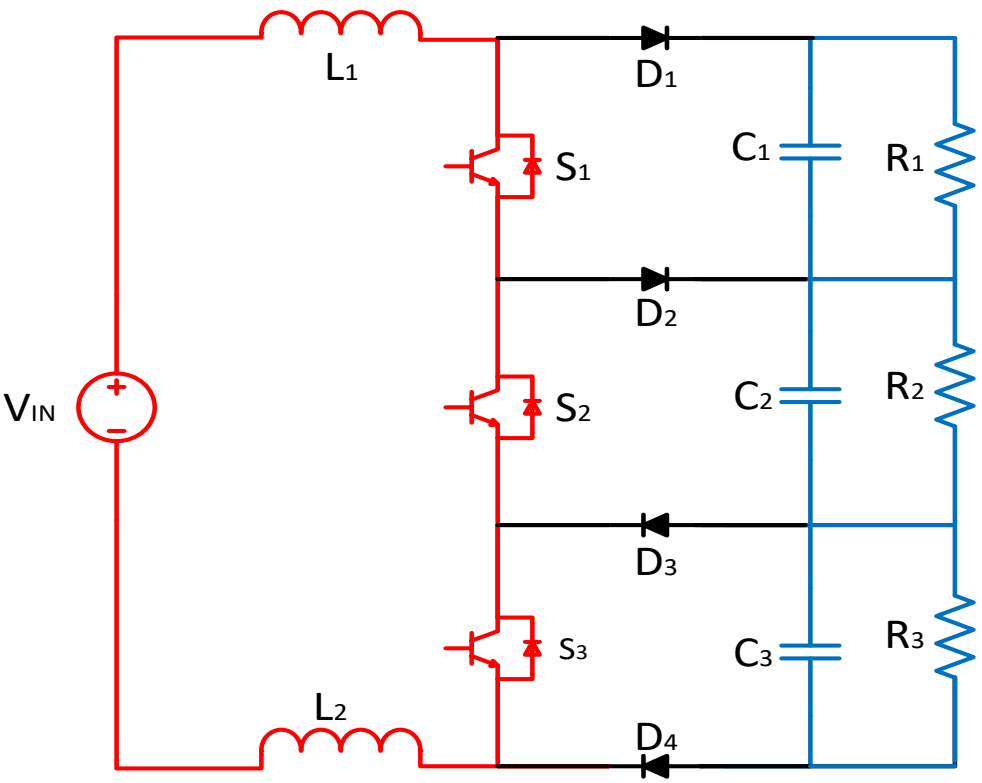


(d)

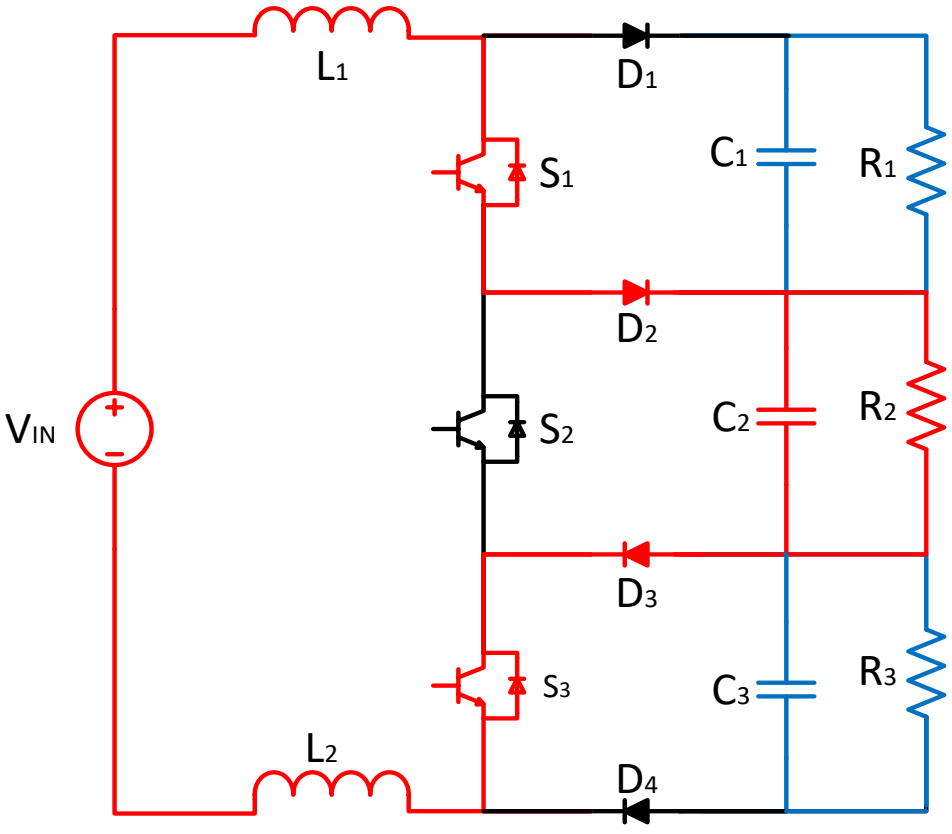


(e)

Figure 2.11: A diode rectifier, 4L DC-DC boost converter, and 4L-DCC configuration. (a) block diagram of the configuration, (b) three-phase diode rectifier, (c) four-level dc-dc boost converter, (d) four-level DCC topology, and (e) circuit of the configuration.


L1
D1
S1
C1
R1
D2
VIN
S2
C2
R2
D3
S3
C3
R3
L2
D4

(a)


L1
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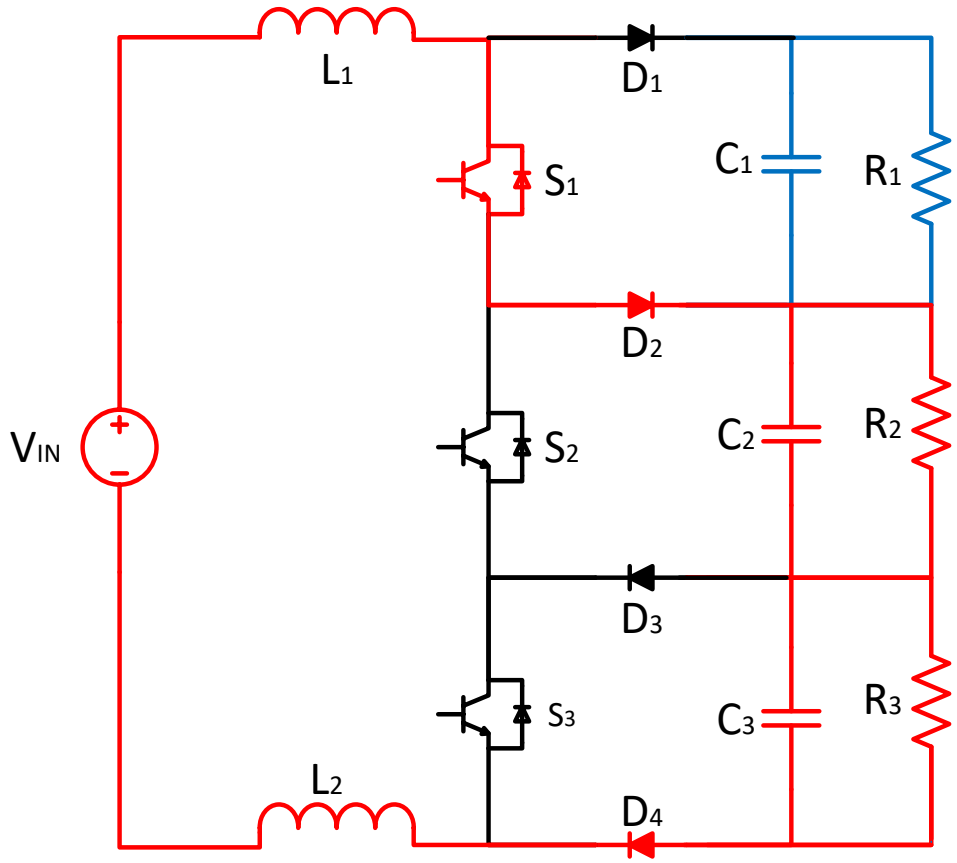
(b)


L1
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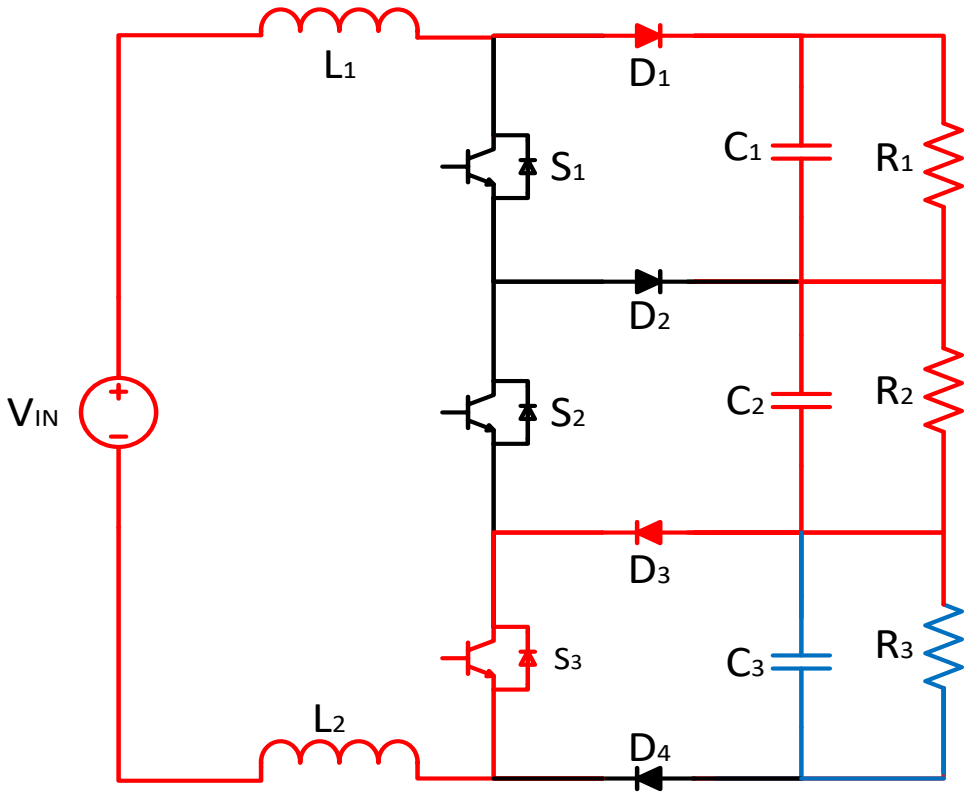
(c)


L1
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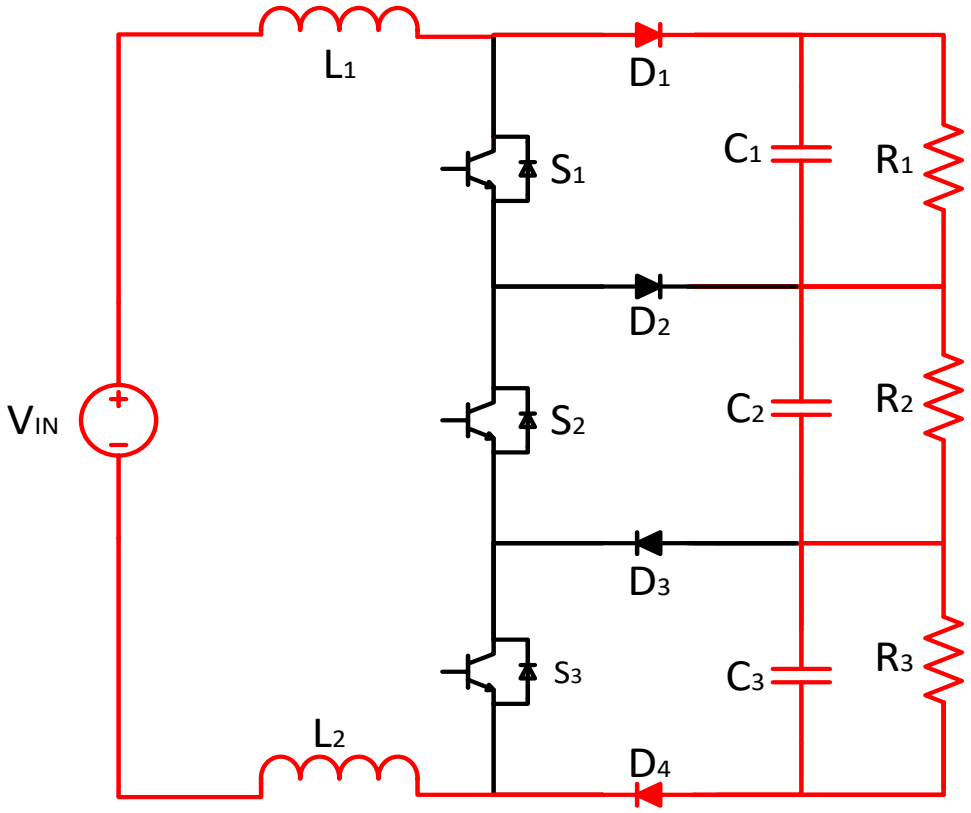
(d)



(e)

Figure 2.12: Different modes of operation of a 4L DC-DC converter. (a) the first mode, (b) second mode, (c) third mode, (d) fourth mode, and (e) fifth mode.

B. High Frequency-Link Multilevel Cascaded Medium-Voltage Converter

This configuration is based on the scalable feature of the MMC topology and the small magnetic cores and winding of a high-frequency transformer [89], as illustrated in Figure 2.13. The generator-side converter is made up of a diode rectifier and high-frequency H-bridge inverter connected to the rectifier via a capacitor; to supply the primary windings of a common multi-winding link, which replaced the conventional dc-link capacitors [89]. The secondary windings are connected to the diode bridge rectifier and H-bridge inverter in a back-to-back connection [89]. The primary windings inverter and secondary windings rectifier form a dual active bridge (DAB) topology [89]. However, the core losses and coupling of the DAB windings will reduce the efficiency of the configuration. The DAB converter utilized in the configuration is an isolated, unidirectional step-up topology shown in Figure 2.14. The advantages of the DAB converter topology in the configuration are higher switching frequency operation, low-voltage power semiconductor device ratings, and minimal switching losses.

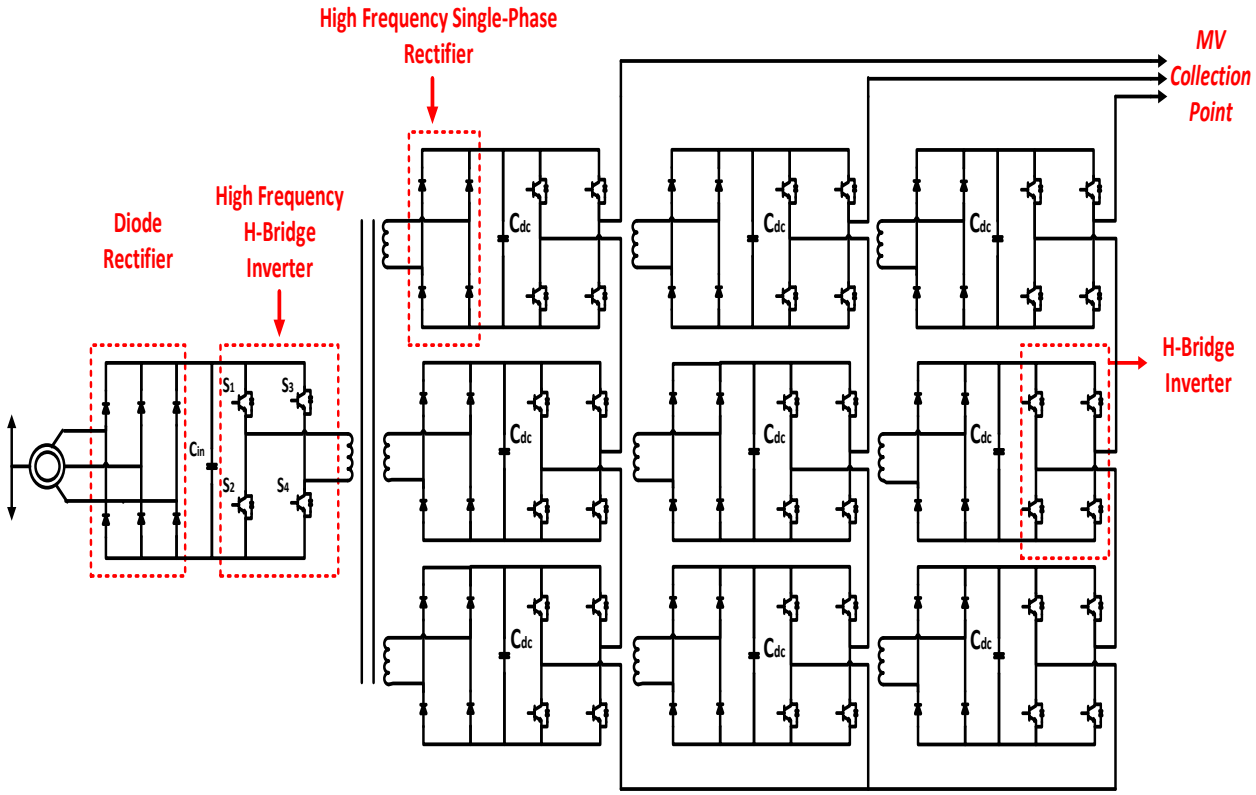


Figure 2.13: High frequency-link multilevel cascaded MV converter configuration.

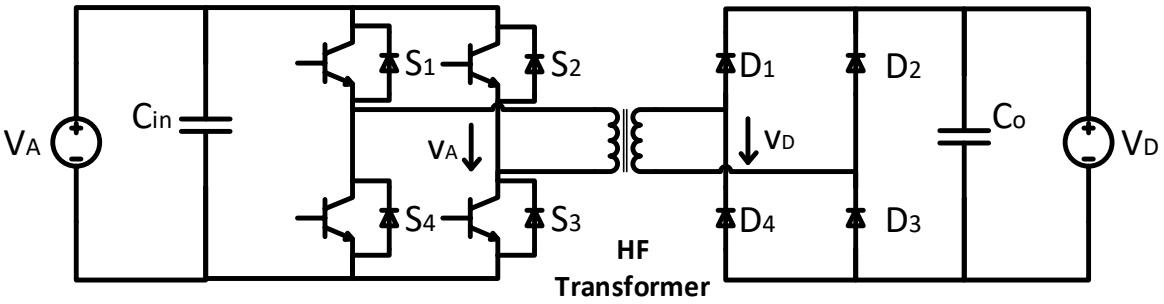


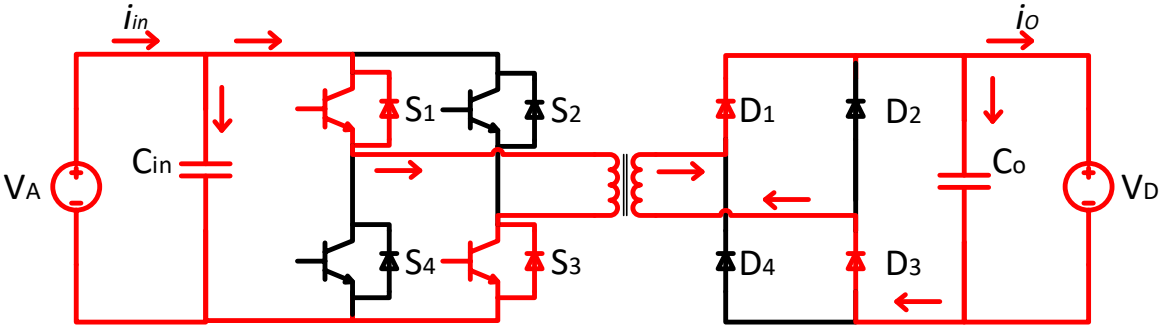
Figure 2.14: The DAB converter topology.

The DAB converter topology consists of a 1ph active bridge and a 1ph diode bridge coupled via the high-frequency transformer. The output ac voltage of the 1ph active bridge (v_A) and input ac voltage of the 1ph diode bridge (v_D) are phase-shifted from each other at an angle θ, to control power flow through the leakage inductance of the transformer [89]. Therefore, the power flow in the DAB converter is expressed in (2.9).

$$P = \frac{V_A V_D}{n\omega L_k}\theta\left(1 - \frac{|\theta|}{\pi}\right) \tag{2.9}$$

where $n = N_A/N_D$ is the high-frequency transformer turn ratio; N_A is the number of turns of the active bridge; N_D is the number of turns of the diode-bridge, $\omega = 2\pi f_s$; f_s is switching frequency, and L_k is leakage inductance of the transformer.

Figures 2.15(a) to 2.15(d) shows the different modes of operation of the DAB converter utilized in the high frequency-link multilevel cascaded medium voltage converter configuration. The low-voltage (LV) side of the DAB converter is the 1ph active-bridge and high-voltage (HV) side of the DAB converter is the 1ph diode-bridge [89]. The current flow in the LV side (i_{in}) and current flow in the HV side (i_o) is highlighted with the red line in Figures 2.15(a) to 2.15(d). In the first mode of operation shown in Figure 2.15(a), the IGBT modules (S_1 and S_3) are switched ON during this interval in the LV side, and the diode modules (D_1 and D_3) are forward biased in the HV side. While in the second mode of operation, the diode modules (D_2 and D_4) are conducting in the HV side of the topology, as shown in Figure 2.15(b). In the third mode of operation, the IGBT modules (S_2 and S_4) are switched ON, and the diode modules (D_1 and D_3) are conducting in the HV side, as depicted in Figure 2.15(c). Furthermore, in the fourth mode of operation, the diode modules (D_2 and D_4) are conducting in the HV side of the converter, as shown in Figure 2.15(d). Due to the voltage conversion between the LV side and HV side, the high number of turns in the high-frequency transformer ratio results in the poor coupling, core losses, and dielectric losses in the insulation [89], [98]. The grid-side converter is based on the MMC topology (as shown in Figure 2.13), which can be scaled up to the required MV level of the collection point [6], [89]. Therefore, low voltage rated semiconductor devices are utilized in this topology, and the need for a grid filter can be eliminated [89].



(a)

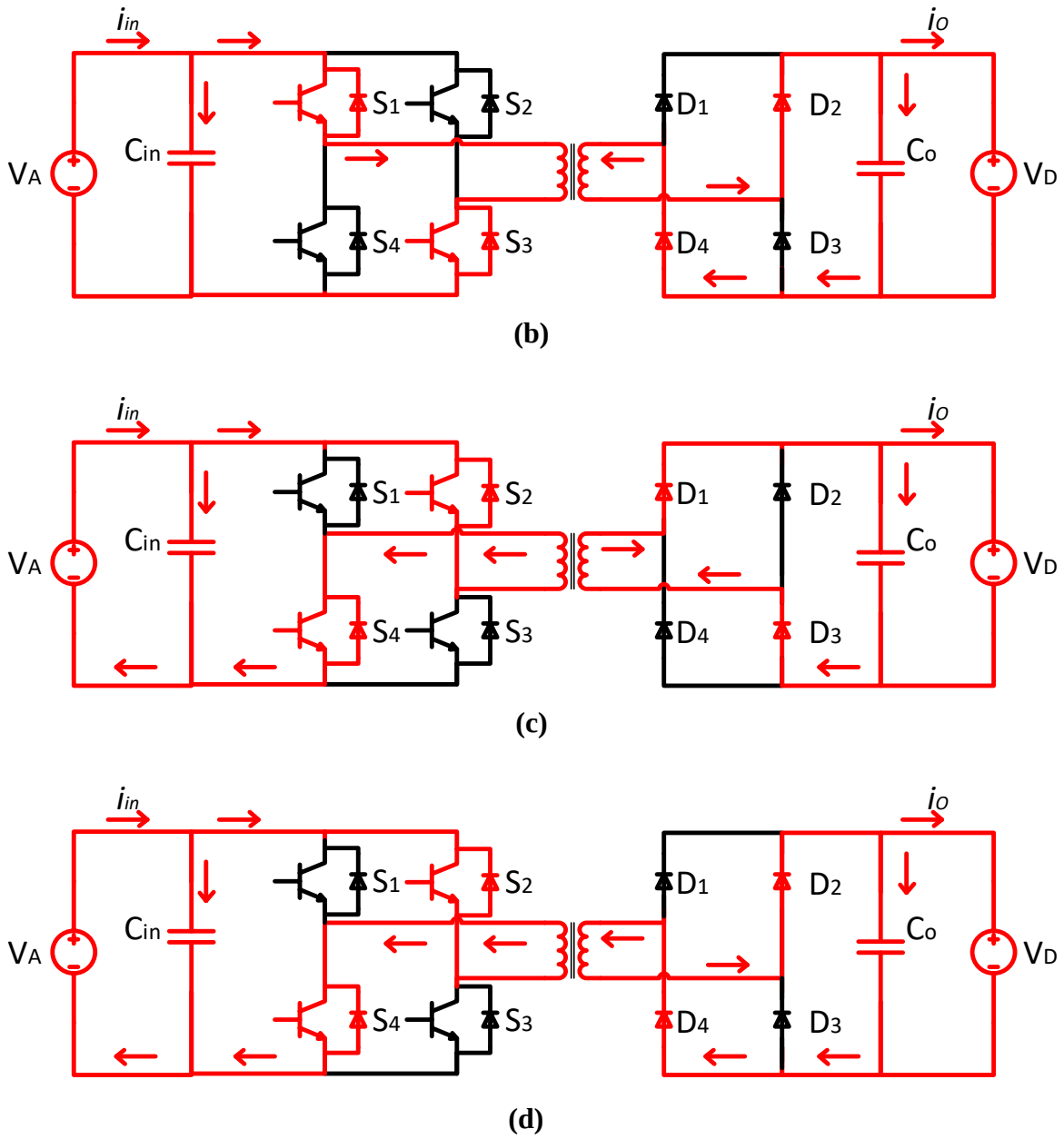
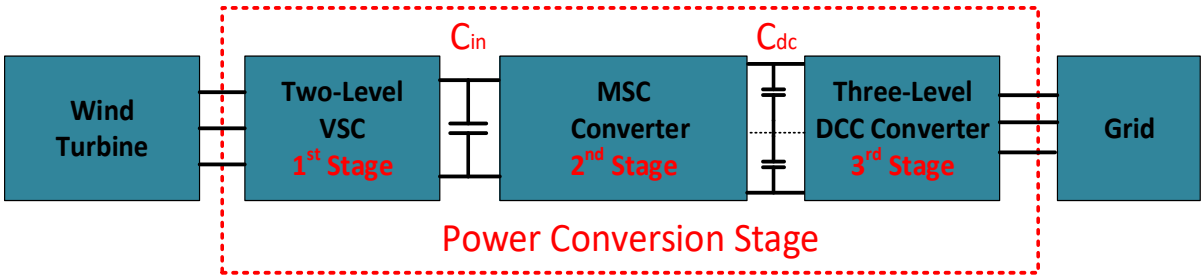


Figure 2.15: Different modes of operation of the DAB converter. (a) the first mode, (b) second mode, (c) third mode, and (d) fourth mode.

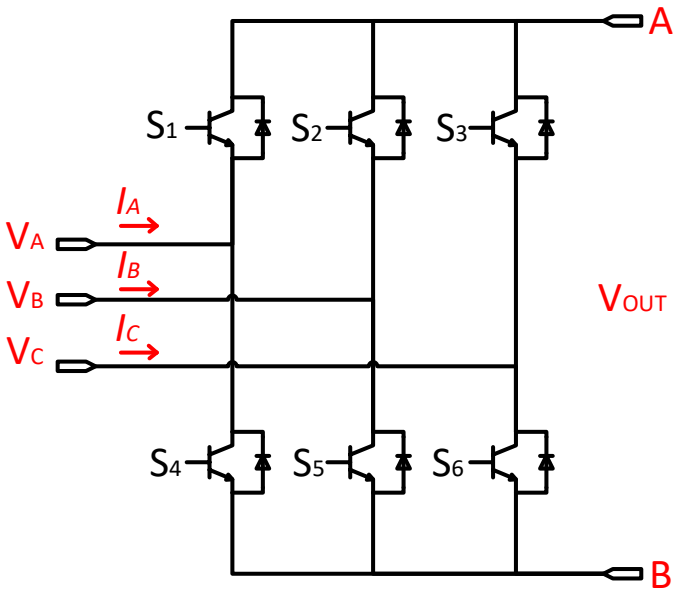
C. 2L-VSC with MSC-Based Resonant Converter and 3L-DCC

This configuration is based on a 2L-VSC topology at the generator-side, an MSC-based resonant converter at the intermediate boost stage, and a 3L-DCC topology at the grid-side [90], as shown in Figures 2.16(a) to 2.16(e). The MSC-based resonant converter is based on a modular structure with two diode modules (D_1 and D_2), a filter capacitor (C_0), a resonant capacitor (C_{re}) and a resonant inductor (L_r), as depicted in Figure 2.17. The module is connected to the dc-link positive and negative rail, as shown in Figure 2.16(c). Also, it operates

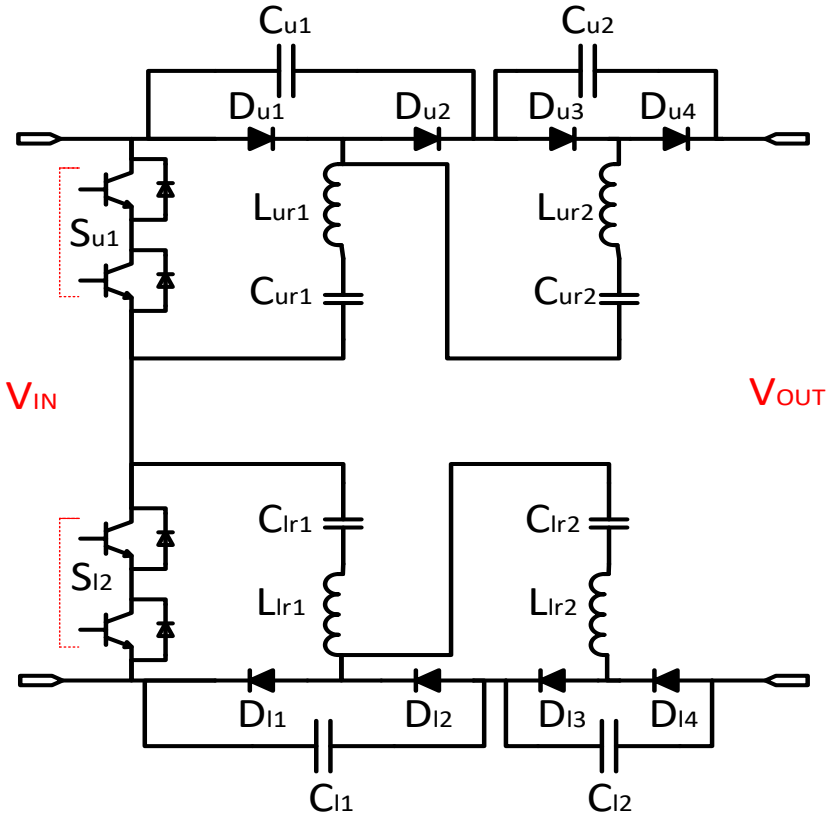
on a zero-current-switching principle which minimizes switching losses and allows the operation of the resonant converter at a high switching frequency [98]. The 3L-DCC topology consists of series-connected IGBT modules that need voltage balancing to maintain equal voltage distribution [72], [73], [90]. In Figures 2.18(a) and 2.18(b), the operation of the modular switched-capacitor resonant converter in the three-stage power converter configuration (shown in Figure 2.16(e)) is illustrated. The IGBT modules (S_{1+} & S_{1-}) operates complementarily at a 50% duty cycle which controls the operation of the positive modular cells and negative modular cells independently [98]. When S_{1-} is switched ON (highlighted in red) and S_{1+} is switched OFF (highlighted in black), the resonant capacitors in the positive rail ($C_{re1+}\ to\ C_{ren+}$) are charged up by the input voltage source (V_{in}) and the filter capacitors ($C_{01+}\ to\ C_{0n+}$) via the resonant inductors in the positive rail ($L_{r1+}\ to\ L_{rn+}$) as shown in Figure 2.18(a). While S_{1+} is switched ON (highlighted in red) and S_{1-} is switched OFF (highlighted in black), the resonant capacitors in the negative rail ($C_{re1-}\ to\ C_{ren-}$) are charged up by the input voltage source (V_{in}) and the filter capacitors ($C_{01-}\ to\ C_{0n-}$) via the resonant inductors in the negative rail ($L_{r1-}\ to\ L_{rn-}$) as shown in Figure 2.18(b). The modular switched-capacitor resonant converter has high efficiency due to its zero-current switching technique, as discussed in [90] and [98]. However, the high number of components in the modular switched-capacitor resonant converter topology is a significant drawback that increases the power converter configuration's associated cost [98]. Also, the switched-capacitor component of the converter cell results in poor voltage regulation, which is further magnified during grid voltage sags [90]. Also, the design of the resonant inductors is complex due to the required high switching frequency of the converter [98].



(a)


A
S1
S2
S3
IA
VA
IB
VB
VOUT
IC
VC
S4
S5
S6
B

(b)


Cu1
Cu2
Du1
Du2
Du3
Du4
Su1
Lur1
Lur2
Cur1
Cur2
VIN
VOUT
Clr1
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Sl2
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Dl4
Cl1
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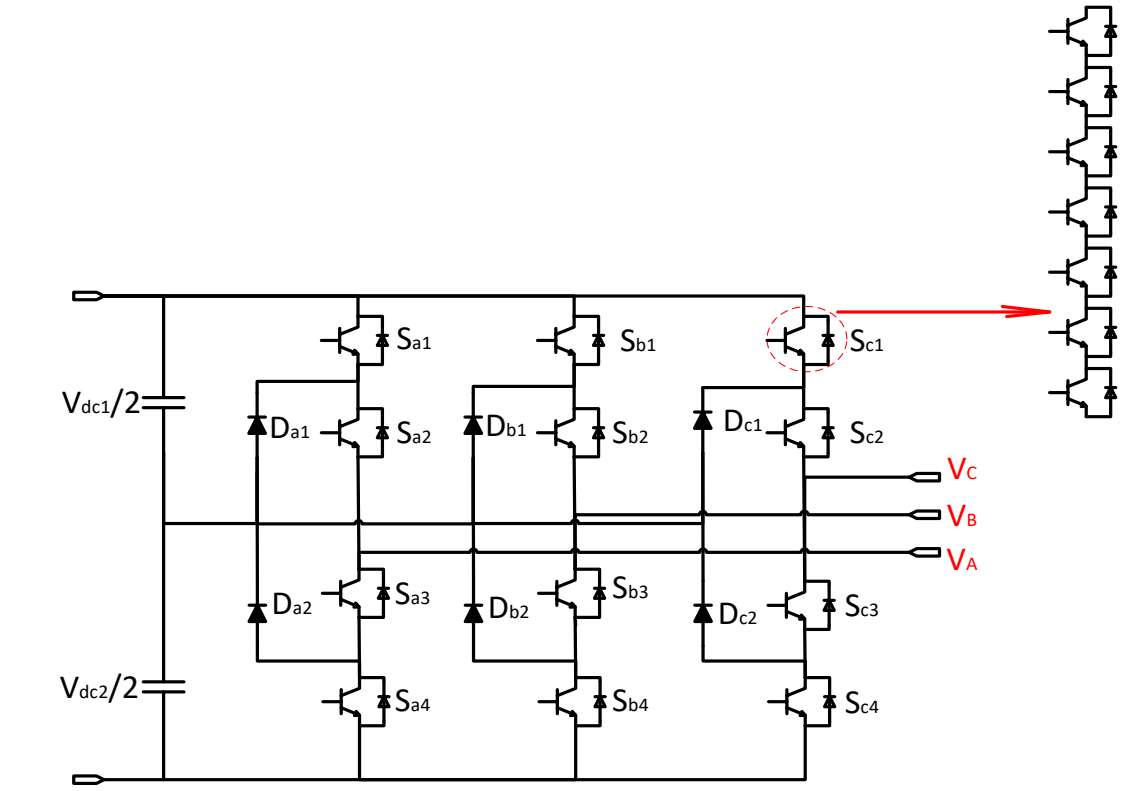
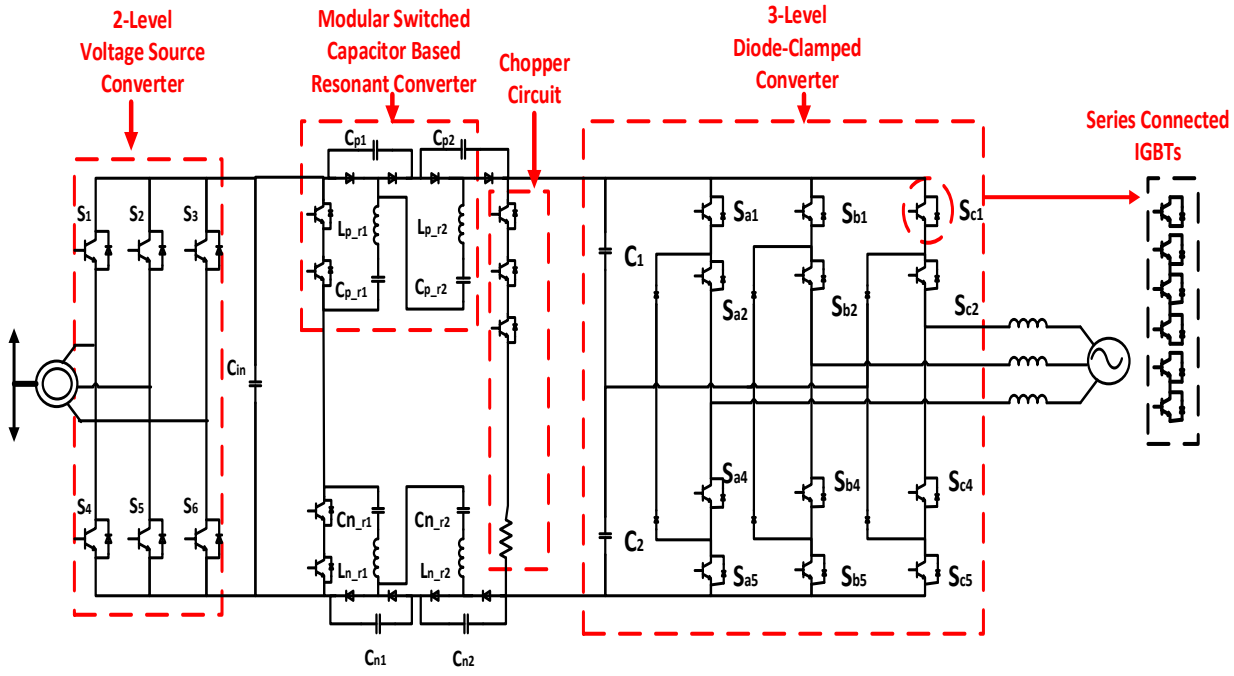
(c)



(d)



(e)

Figure 2.16: A 2L-VSC, MSC-based resonant converter with 3L-DCC configuration. (a) block diagram of the configuration, (b) three-phase 2L-VSC, (c) MSC-based resonant converter, (d) three-level DCC topology, and (e) circuit of the configuration.

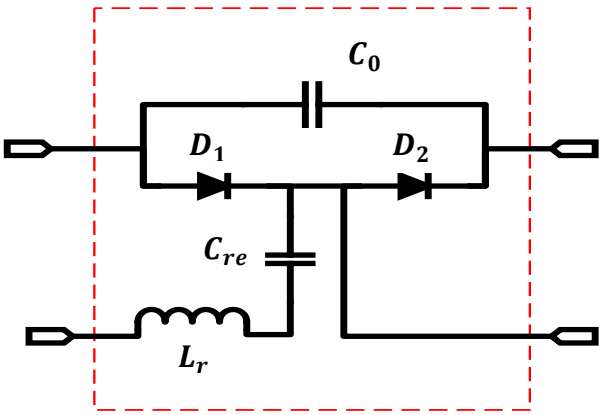
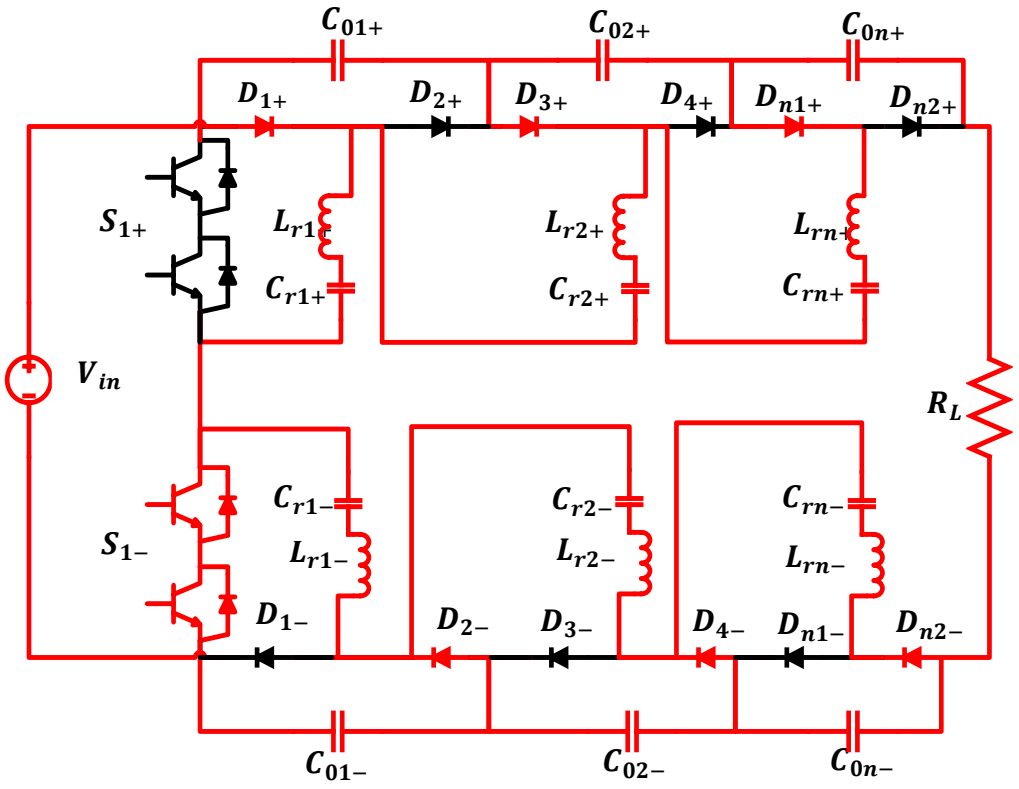
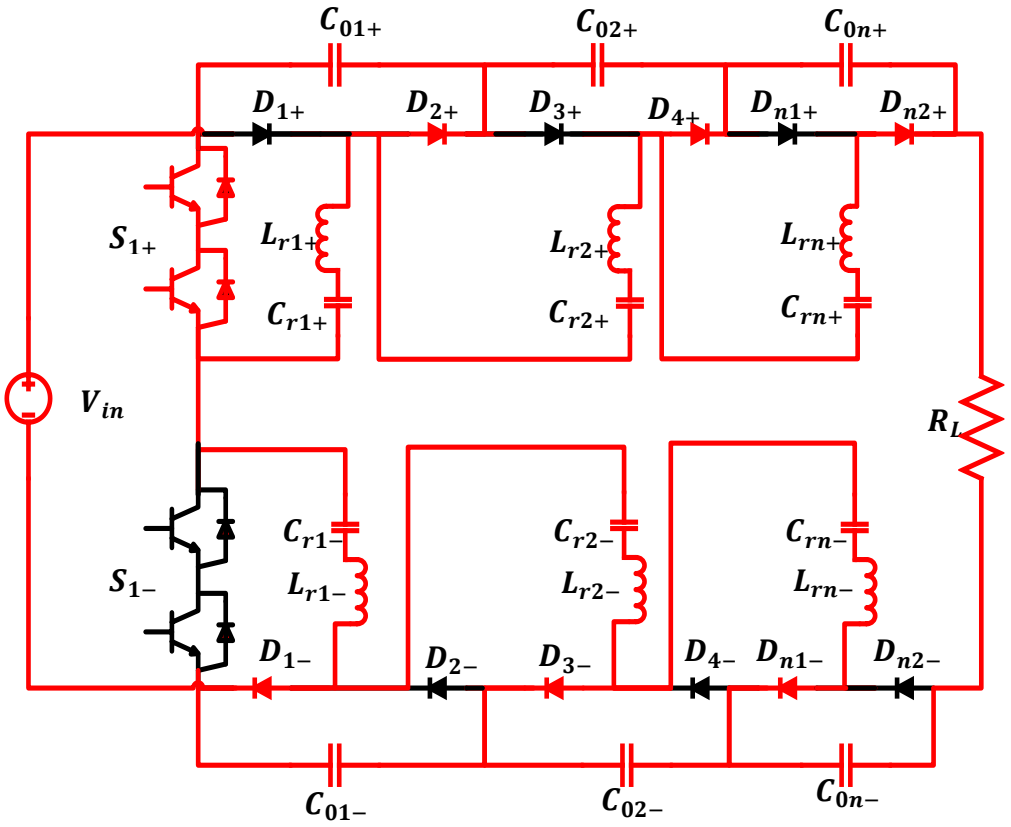


Figure 2.17: A modular switched-capacitor resonant converter cell.



(a)



(b)

Figure 2.18: Equivalent circuit highlighting the operating modes of the converter. (a) S_{1-} is switched ON, and (b) S_{1+} is switched ON.

2.3. Comparative Evaluation

In Tables 2.1 and 2.2, the parameters of the generator-converter configurations and three-stage power converter configurations are highlighted as presented in the literature [86]-[90]. The power converter configurations are evaluated in terms of the device count, voltage boost topology, and grid compliance.

Table 2.1: Parameters of the generator-converter configuration

Parameters	Three-Stage Generator-Converter	Two-Stage Generator-Converter
Rated Power	2 MW	2 MW
Line-to-Line Output Voltage	11 kV	11 kV
Grid Frequency	50 Hz	50 Hz
Number of Generator Coils per phase	24	72
Number of modules per phase	4	24
IGBT voltage rating per module	2.5 kV	1.7 kV
IGBT current rating per module	1.5 kA	300 A
Clamping diode voltage rating per module	2.5 kV	–
Clamping diode current rating per module	1.5 kA	–
Diode voltage rating per module	1.7 kV	–
Diode current rating per module	3.6 kA	–
Single switch boost converter IGBT voltage rating	1.7 kV	–
Single switch boost converter IGBT current rating	3.6 kA	–
Converter Module DC-Link Voltage	2.8 kV	800 V
Converter Module DC-Link Capacitance	8,000 μF	2,200 μF
Switching Frequency	1.2 kHz	600 Hz

Table 2.2: Parameters of the three-stage power converter configuration

Parameters	Passive + 4L DC-DC+ 4L-DCC	High Frequency-Link multilevel cascaded MV Converter	2L VSC. + MSC-based Resonant + 3L-DCC
Rated Power	5 MW	4.76 MW	10 MW
Line-to-Line Output Voltage	4.16 kV	11 kV	20 kV
Grid Frequency	50 Hz	50 Hz	50 Hz
Number of Grid-Side Converter Module per phase	–	10	–
Number of DC-DC Module per phase	–	–	6
Input Capacitance	8,300 μF	–	330 μF
Boost Filter Inductance	2.9 mH	–	–
DC-Link Capacitance	3,500 μF	–	1,000 μF
DC-Link Voltage	7.35 kV	–	36 kV
Grid-Side Converter Module DC-Link Voltage	–	809 V	–
Grid-Side Converter Module DC-Link Capacitance	–	600 μF	–
Switching Frequency	850 Hz	2 kHz	1.05 kHz
IGBT voltage rating	4.5 kV	1.7 kV	4.5 kV
IGBT current rating	1.2 kA	0.5 kA	0.65 kA
Diode voltage rating	4.5 kV	1.7 kV	4.5 kV
Diode current rating	1.2 kA	0.5 kA	0.65 kA

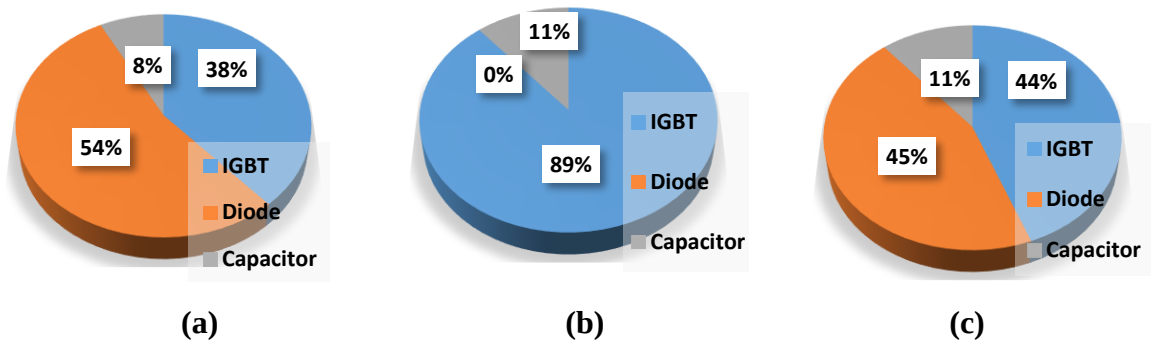
2.3.1. Device Count

The power converter configurations consist of two main categories of devices: active and passive devices, as stated previously [86]-[90]. The active device group consists of IGBTs and diodes, while the passive device group consists of capacitors, resistors, and inductors [86]-[90]. The device count directly affects the power converter configuration's reliability and cost, as illustrated in Figure 1.6. In Table 2.3, the number of devices in each of the presented power converter configuration is broken down into the number of IGBTs (N_{IGBT}), number of diodes (N_{Diode}), number of capacitors (N_{Cap}), and number of inductors (N_{ind}). The power converter configurations based on any form of modular multilevel converter (MMC) topology consists

of more active devices than its counterpart with other forms of multilevel topologies, as illustrated in Figure 2.19. Therefore, the generator-converter configurations are more susceptible to failure and higher cost because of the higher device count [99]-[108].

Table 2.3: Comparison of device count

Configuration	N_{IGBT}	N_{Diode}	N_{Cap}	N_{ind}
3ph three-stage generator-converter	120	120	24	72
3ph two-stage generator-converter	576	0	72	216
Passive + 4L DC-DC+ 4L-DCC	21	40	4	2
High Frequency-Link multilevel cascaded MV converter	124	126	31	31
2L VSC. + MSC-based resonant converter + 3L-DCC	94	108	14	14



(a) **(b)** **(c)**

Figure 2.19: Components in an MMC-based configuration, (a) 3-ph three-stage generator-converter, (b) 3ph two-stage generator-converter, and (c) high frequency-link multilevel cascaded MV converter.

2.3.2. Voltage Boosting Topology

The voltage boosting topology of the existing configurations is classified into the following [109] and illustrated in Figure 2.20.

- Non-isolated dc-dc converter.
- Isolated dc-dc converter.
- Soft-switching dc-dc converter.

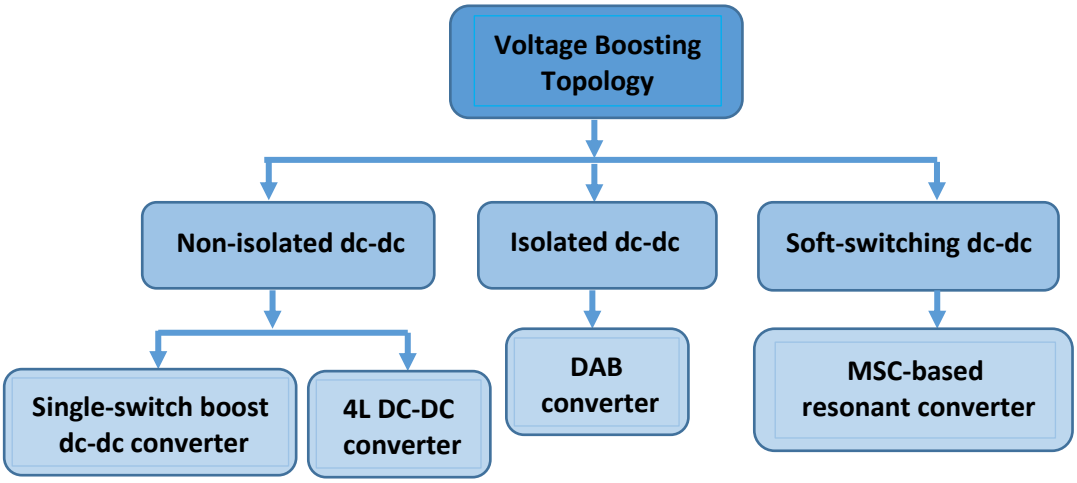


Figure 2.20: Voltage boosting topology.

A. Non-isolated DC-DC Converter

In Figures 2.5, 2.6, and 2.7, a single-switch dc-dc boost converter is shown in the generator-converter module and three-stage generator-converter configuration. The single-switch converter presented in the three-stage generator-converter configuration is based on unidirectional power flow from the stator coil to the grid-side converter [86]. This topology is a simple structure that allows a simple control algorithm, as discussed in [86]. Nonetheless, the 4L DC-DC converter is more complex with three IGBT modules, four diode modules, and an inductor, as shown in Figure 2.11.

The control of the single-switch converter is based on the conventional phase-shifted PWM (PS-PWM) technique which makes it a hard-switched converter [86], [109]. A single-phase configuration consists of eight modules of single-switch converters, increasing the overall switching losses due to hard-switching. Furthermore, both the single-switch converter and 4L DC-DC converter topologies have low-voltage gain with minimal duty cycle, making these topologies less reliable for medium voltage, high-power applications [86], [88].

B. Isolated DC-DC Converter

The DAB converter utilized in the high frequency-link multilevel cascaded medium-voltage converter configuration is classified under the isolated dc-dc converter topology category [109], as illustrated in Figures 2.13 to 2.15. Figure 2.15 shows a DAB converter, a unidirectional variant of an isolated dc-dc converter topology [109]-[112]. One of the significant merits of a DAB converter is its high efficiency, which is reduced under non-ideal

operating conditions, such as voltage sags [112]. Furthermore, dead time during the switching intervals of the IGBTs at the LV side of the DAB converter (as shown in Figure 2.15(a) to 2.15(d)) introduces an additional undesired phase shift [112]. This negative effect inherently limits the power flow between the LV-side and HV-side of the DAB converter [109]-[112]. Also, the DAB converter is characterized by large voltage spikes due to leakage inductance [109].

C. Soft-switching DC-DC Converter

Figures 2.16 to 2.18 shows the MSC-based resonant converter, which is based on soft-switching dc-dc converter topology, by utilizing the zero-current switching technique discussed previously [90], [98], [109]. The merit of the MSC-based resonant converter is its reduced size and weight because of its high switching frequency [90], [98]. However, the effective operation of the converter is dependent on its resonant frequency, which can adversely affect the power converter configuration under asymmetrical voltage sags [109].

2.3.3. Grid Compliance

In Chapter 1, one of the critical issues that must be addressed for the effective grid-connection of a transformer-less WECS has been stated to minimize the injected dc component [76]-[83]. The following criteria must be within the grid compliance standard [81], [90], [113].

- Injected current harmonic level
- Total harmonic distortion (THD)
- Voltage and fundamental frequency level
- Grounding

In Table 2.4, the standards that stipulate the level of injected dc components in the grid have been highlighted. Furthermore, the power converter configurations are compared in Table 2.5, based on the conventional functions of the wind turbine transformer.

Table 2.4: Injected DC current level

IEC61727	IEEE1547	IEEE929
$<$ 1% of rated current	$<$ 0.5% of rated current	$<$ 0.5% of rated current

Table 2.5: Comparison of the existing power converter configurations

Functions of a wind turbine transformer	Three-Stage Generator-Converter	Two-Stage Generator-Converter	Passive + 4L DC-DC+ 4L-DCC	HF-Link multilevel cascaded MV Converter	2L VSC. + MSC-based Resonant + 3L-DCC
Increase voltage level	Yes	Yes	Yes	Yes	Yes
Grounding	No	Yes	No	No	Yes
Voltage sag transformation	Yes	Yes	No	No	No
Minimization of DC component	No	No	No	No	No

Table 2.6: Reactive power requirements in specific grid codes [16]-[18].

Region	Reactive Power Requirement Location	Reactive Power Range (p.u. of rated output)	Equivalent Power Factor
Denmark	PCC	$-0.33\ to\ 0.33$	$0.9\ to\ 0.95$
United Kingdom	Grid connection point	$-0.33\ to\ 0.33$	0.95
Ireland	Low-voltage side of transformer	$-0.33\ to\ 0.33$	0.95
Spain	Not specified	$-0.3\ to\ 0.3$	Not specified
Texas	PCC	Not specified	0.95
Alberta	Low-voltage side of transformer	Not specified	$0.9\ to\ 0.95$
Ontario	PCC	$-0.33\ to\ 0.33$	Not specified
ENTSO-E	High-voltage side of transformer	$-0.5\ to\ 0.65$	$-0.838\ to\ 0.894$
Australia	PCC	0.395	Not specified

Another important grid compliance parameter for the grid-connection of a transformer-less WECS is the ability to provide the necessary reactive power support during both steady-state and transient conditions of the grid [16]-[18]. The reactive power requirements extracted from existing grid codes is often based on the voltage level of connection, the PCC, the measurement of the reactive power in terms of the power factor or the rated power, and the region where the system is suited [16]-[18]. In Table 2.6, the reactive power requirements in specific grid codes existing in Europe and North America have been highlighted. For example, in the southern part

of Australia, the WPP should have power factor within the range of $-0.93\ to\ 0.93$ at full load at the PCC, and 50% reactive power capability should be available in the WPP [16]. The recommended reactive power support components in WPP are stated as follows; On-Load Tap Changer (OLTC) transformer, capacitor banks, energy storage systems, static synchronous compensator (STATCOM), and static VAR compensator (SVR) [16]-[18].

The elimination of the step-up transformer in the transformer-less WECS configuration reduces the overall reactive power capability of the WPP. However, the reactive power capability of the converter configuration can be improved by through advanced modulation and control techniques [16].

2.3.4. Comparative Benchmark Factor (CBF)

The three comparative factors discussed in the previous section are deployed into a comparative benchmark factor (CBF) to assess the suitability of a particular power converter configuration for transformer-less WECS applications. Therefore, the component for each level factor (CEL_f) presented in [114] is extended to the generator-side converter, intermediate boost converter, and grid-side converter of the configuration. Also, the grid compliance factor (GC_f) is introduced and presented in this section.

A. Component for each Level Factor (CEL_f)

The CEL_f considers the number of power semiconductor devices and passive devices based on their respective voltage ratings [114], [115]. The equivalent number of IGBTs (NE_{IGBT}), diodes (NE_{Diode}), capacitors (NE_{cap}), and inductors (NE_{ind}) are calculated using (2.10) to (2.13).

$$NE_{IGBT} = \frac{\sum_{n=1}^{N_{IGBT}} V_{IGBT}}{V_b} \tag{2.10}$$

$$NE_{Diode} = \frac{\sum_{n=1}^{N_{Diode}} V_{Diode}}{V_b} \tag{2.11}$$

$$NE_{cap} = \frac{\sum_{n=1}^{N_{cap}} V_{cap}}{V_b} \tag{2.12}$$

$$NE_{ind} = \frac{\sum_{n=1}^{N_{ind}} V_{ind}}{V_b} \tag{2.13}$$

where N_{IGBT}, N_{Diode}, N_{cap}, N_{ind} are the number of IGBTs, diodes, capacitors, and inductors, respectively, V_{IGBT}, V_{Diode}, V_{cap}, V_{ind} are the voltage ratings of the IGBTs, diodes, capacitors, and inductors, and V_b is the base voltage, which is represented by the dc-link voltage (V_{dc}), input voltage (V_{in}), and output voltage (V_o).

Table 2.7 to Table 2.9 highlights N_{IGBT}, N_{Diode}, N_{cap}, N_{ind}, V_{IGBT}, V_{Diode}, V_{cap}, and V_{ind} of the power converter configurations. From Tables 2.7 to 2.9, the value of V_b is dependent on the part of the configuration the component is situated (i.e., grid-side converter topology will have V_b to be V_{dc}, while the intermediate boost converter topology will have both V_{in} and V_o representing V_b based on topology and the component). Therefore, the total equivalent number of components and the associated CEL_f is obtained using (2.14) to (2.15).

$$NE_{total} = NE_{IGBT} + NE_{Diode} + NE_{cap} + NE_{ind} \tag{2.14}$$

$$CEL_f = \frac{NE_{total}}{N_L} \tag{2.15}$$

where N_L is the number of voltage levels of the converter topology. Also, the CEL_f of the power converter configuration is highlighted in Table 2.10.

Table 2.7: Comparison of the components and voltage rating in the grid-side converter topology

Topology	N_{IGBT}	V_{IGBT}	N_{Diode}	V_{Diode}	N_{cap}	V_{cap}
Bridge cell	288	V_{dc}	–	–	72	V_{dc}
3L-DCC Bridge cell	96	$V_{dc}/2$	48	$V_{dc}/2$	24	$V_{dc}/2$
4L-DCC	18	$V_{dc}/3$	18	$V_{dc}/3$	3	$V_{dc}/3$
Bridge cell	120	V_{dc}	–	–	30	V_{dc}
3L-DCC	84	$V_{dc}/2$	42	$V_{dc}/2$	2	$V_{dc}/2$

Table 2.8: Comparison of the components and voltage rating in the boost converter topology

Topology	N_{IGBT}	V_{IGBT}	N_{Diode}	V_{Diode}	N_{cap}	V_{cap}	N_{ind}	V_{ind}
Single-switch dc-dc converter	24	$V_o/2$	24	$V_o/2$	–	–	–	–
4L-DC DC	3	$V_o/3$	4	$V_0/3$	–	–	2	$V_{in}/2$
DAB converter	4	V_{in}	120	V_0	–	–	1	V_{in}
							30	V_0
MSR converter	4	$V_{in}/4$	12	V_{in}	12	V_{in}	6	V_{in}

Table 2.9: Comparison of the components and voltage rating in the generator-side converter topology

Topology	N_{IGBT}	V_{IGBT}	N_{Diode}	V_{Diode}	N_{cap}	V_{cap}	N_{ind}	V_{ind}
1ph diode rectifier	–	–	96	V_{in}	–	–	24	V_{in}
1ph active rectifier	288	V_{in}	–	–	–	–	144	V_{in}
3ph diode rectifier	–	–	18	V_{in}	–	–	–	–
3ph diode rectifier	–	–	6	V_{in}	–	–	–	–
2L-VSC	6	V_{in}	–	–	–	–	–	–

Table 2.10: Comparison of the CEL_f

Configuration	$CEL_{f,R}$	$CEL_{f,B}$	$CEL_{f,G}$
3ph three-stage generator-converter	7.06	1.41	21.2
3ph two-stage generator-converter	17.3	0	14.4
Passive + 4L DC-DC+ 4L-DCC	9	1.08	3.75
High frequency-link multilevel cascaded MV converter	3	8.21	7.14
2L VSC. + Mod. Switch Resonant + 3L-DCC	3	3.17	21.3

*$CEL_{f,R}$ – *generator-side converter* CEL_f.; $CEL_{f,B}$ – *intermediate boost converter* CEL_f. $CEL_{f,G}$ – *grid-side converter* CEL_f.

C. Grid Compliance Factor (GC_f)

The GC_f is proposed to compare the level of grid compliance of the power converter configurations. Amongst the four critical factors that the grid compliance standards stipulate;

the injection of dc components is directly related to the asymmetrical characteristics of the switching power semiconductor devices (i.e., IGBTs), and THD is related to the number of voltage levels at the grid-side converter topology of the power converter configuration [76]-[83], [90], [113].

The multilevel converter topology is a combination of two-level converter switching cell, as discussed extensively in Chapter 3, and illustrated in Figure 2.21(a). Therefore, the grid-side converter topology of each configuration can be simplified into their primary switching cells, as shown in Figures 2.21(b) to 2.21(d). Each switching cell represents a specific switching state that will produce dc components due to a slight difference in the electrical characteristics (i.e., on-state resistance and junction capacitance, etc.) of the IGBT pair. The switching state factor (SS_f) represents the switching state at each voltage level of the topology. However, the current flowing through the grid-converter topology is assumed to be constant, as stated in [114]. Therefore, the number of IGBTs switching ($N_{IGBT,s}$) and their respective voltage ratings (V_{IGBT}) at a particular voltage level ($V_{L,s}$) is used to derive SS_f as expressed in (2.16).

$$SS_f = \frac{\sum_{n,s=1}^{N_{IGBT,s}} V_{IGBT}}{V_{L,s}} \tag{2.16}$$

While SS_f gives a quick assessment of the switching power semiconductor devices at a specific voltage level, it is used to calculate the GC_f which considers the entire voltage levels of the output voltage waveform, as stated in (2.17).

$$GC_f = \frac{\sum_{n=1}^{N_{SS}} SS_f}{N_L} \tag{2.17}$$

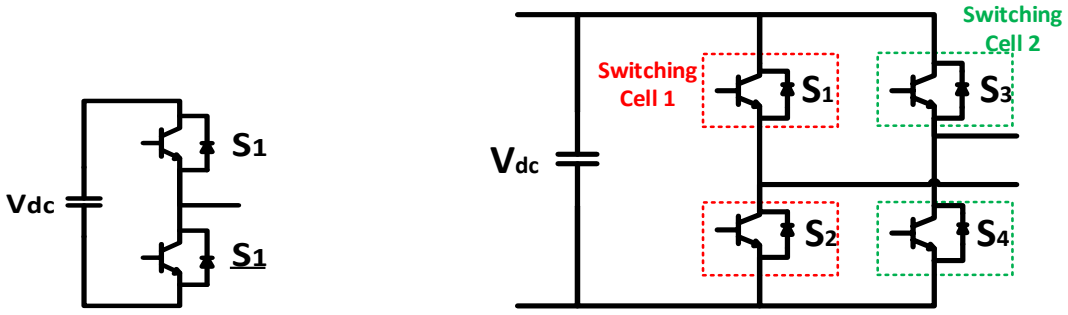
where N_{ss} is the number of switching states, and N_L is the number of voltage levels of the grid-side converter topology.

The SS_f represents the produced dc components at a switching instant and the GC_f represents the THD of the output voltage waveform. In Table 2.11, a comparison of the GC_f in the presented power converter configurations are stated for the entire voltage levels of the grid-side converter topology. From Table 2.11, the power converter configurations with higher voltage levels have lower THD, as highlighted with the 3ph two-stage generator-converter configuration. Furthermore, the power converter configurations with higher $CEL_{f,R}$, $CEL_{f,B}$, $CEL_{f,G}$ (i.e., ≥ 15) will be more susceptible to failure and associated higher cost, as shown in

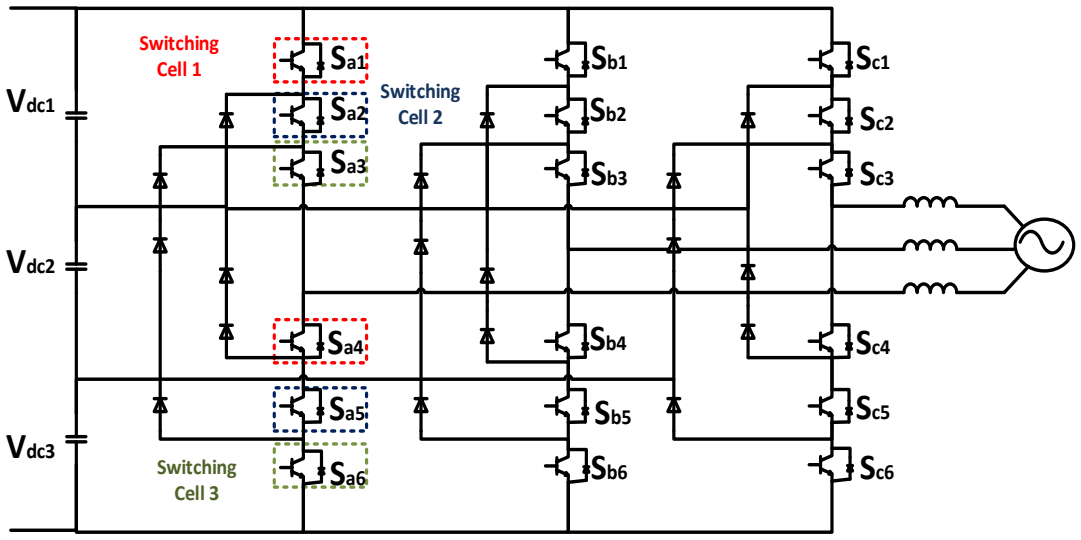
Figure 2.22. The highlighted demerit is mainly due to its higher component counts because of the MMC topology and the high number of series connected IGBTs [116].

Table 2.11: Comparison of the GC_f

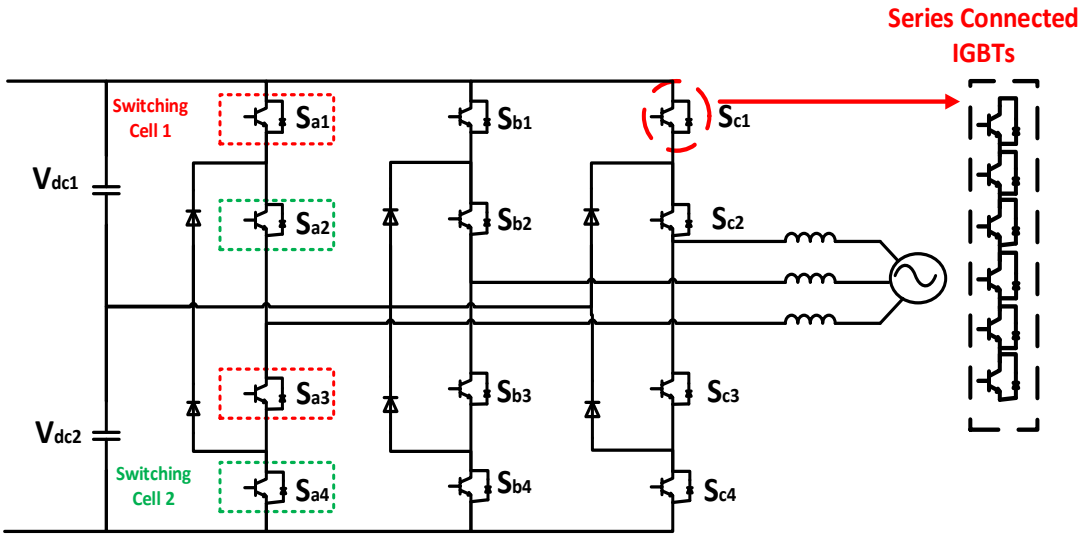
Configuration	Voltage levels	GC_f
3ph three-stage generator-converter	$0, 1/16\,V_{dc}, 1/8\,V_{dc}, 3/16\,V_{dc}, 1/4\,V_{dc}, 5/16\,V_{dc}, 3/8\,V_{dc}, 7/16\,V_{dc}, 1/2\,V_{dc}, 9/16\,V_{dc}, 5/8\,V_{dc}, 11/16\,V_{dc}, 3/4\,V_{dc}, 13/16\,V_{dc}, 7/8\,V_{dc}, 15/16\,V_{dc}, V_{dc}$	2.596
3ph two-stage generator-converter	$0, 1/24\,V_{dc}, 1/12\,V_{dc}, 1/8\,V_{dc}, 1/6\,V_{dc}, 5/24\,V_{dc}, 1/4\,V_{dc}, 7/24\,V_{dc}, 1/3\,V_{dc}, 9/24\,V_{dc}, 5/12\,V_{dc}, 11/24\,V_{dc}, 1/2\,V_{dc}, 13/24\,V_{dc}, 7/12\,V_{dc}, 15/24\,V_{dc}, 4/6\,V_{dc}, 1\,7/24\,V_{dc}, 3/4\,V_{dc}, 19/24\,V_{dc}, 5/6\,V_{dc}, 21/24\,V_{dc}, 11/12\,V_{dc}, 23/24\,V_{dc}, V_{dc}$	0.0624
Passive + 4L DC-DC+ 4L-DCC	$0, 1/3\,V_{dc}, 2/3\,V_{dc}, V_{dc}$	4.14
High frequency-link multilevel cascaded MV converter	$0, 1/20\,V_{dc}, 1/10\,V_{dc}, 3/20\,V_{dc}, 1/5\,V_{dc}, 1/4\,V_{dc}, 3/10\,V_{dc}, 7/20\,V_{dc}, 4/10\,V_{dc}, 9/20\,V_{dc}, 1/2\,V_{dc}, 11/20\,V_{dc}, 3/5\,V_{dc}, 13/20\,V_{dc}, 7/10\,V_{dc}, 3/4\,V_{dc}, 4/5\,V_{dc}, 1\,7/20\,V_{dc}, 9/10\,V_{dc}, 19/20\,V_{dc}, V_{dc}$	1.027
2L VSC. + MSC + 3L-DCC	$0, 1/2\,V_{dc}\,, V_{dc}$	21



(a) **(b)**



(c)



(d)

Figure 2.21: Switching cells of the grid-side converter topology. (a) primary switching cell, (b) bridge switching cell, (c) 3ph 4L-DCC switching cells, and (d) 3ph 3L-DCC switching cells.

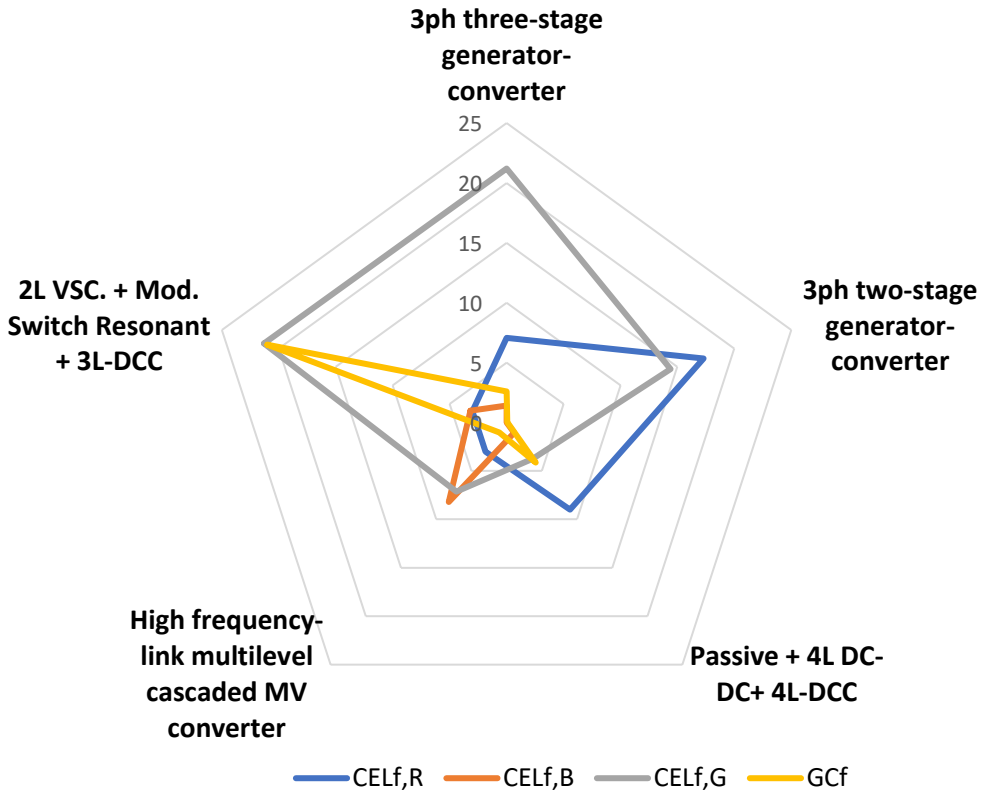


Figure 2.22: Comparison of CEL_f and GC_f.

D. Summary of the Comparative Benchmark Factor

The CEL_f and GC_f evaluation carried out on the presented power converter configurations studied in this chapter has highlighted the merits and demerits of each configuration in terms of the components count, topology, and grid compliance. In Table 2.10, the generator-converter configuration has more components count due to the MMC-based structure of the configuration. On the other hand, the generator-converter configuration is more grid compliant than the three-stage power converter configuration because they have higher voltage levels because of the MMC-based structure of the configuration.

According to the CEL_f and GC_f evaluation carried out on the three-stage power converter configuration, the passive generator-side with 4L DC-DC converter and 4L-DCC configuration have least components count when compared to other configurations within the same category and the generator-converter configuration. Also, the passive generator-side with 4L DC-DC converter and 4L-DCC configuration is still more grid compliant when compared to the 2L-VSC with MSC-based resonant converter and 3L-DCC configuration. Based on the stated facts, the ideal power converter configuration should have a multilevel converter topology with a

minimum of four voltage-levels (or higher) and multiple power semiconductor devices should not be series-connected. For instance, the 2L-VSC with MSC-based resonant converter and 3L-DCC configuration have six series-connected switching power semiconductor devices at the grid-side converter topology as shown in Figure 2.21(d). The impact of the six series-connected switching power semiconductor devices further increased the components count will adds to the complexity of the configuration.

2.4. Cost-Benefit Analysis

The life cycle cost (LCC) analysis of the power converter configuration in a transformer-less WECS is compared with the power converter configuration in a conventional WECS. Furthermore, the LCC analysis of the collection system of a WPP with transformer-less WECSs and a conventional WECSs is presented to obtain the cost-benefit of a WPP with transformer-less WECSs. Therefore, sensitivity analysis is studied to understand the variability of specific parameters.

2.4.1. LCC Analysis of the Power Converter Configurations

The total cost of the power converter configuration is classified into three main components, namely, initial cost (C_i), operation & maintenance cost ($C_{O\&M}$), and energy cost (C_e). The total estimated LCC of the power converter configuration (LCC_{PCC}) is expressed in (2.18).

$$LCC_{PCC} = C_i + C_{O\&M} + C_e \tag{2.18}$$

A. Initial Cost (C_i)

C_i is mainly the capital cost of procuring the power converter configuration, which consists of component cost (C_{cc}) and cooling system cost (C_{csc}), which is assumed to be 10% of the component cost [103]. Therefore, within this study, C_i is expressed in (2.19).

$$C_i = C_{cc} + C_{csc} \tag{2.19}$$

$$C_{cc} = n_l C_{IGBT} + n_d C_d + n_{ind} C_{ind} + n_c C_{cap} \tag{2.20}$$

$$C_{csc} = 10\% \times C_{cc} \tag{2.21}$$

where,

$$C_{ind} = \frac{1}{G_M}(C_{core} + C_w + C_l) \tag{2.22}$$

$$C_{core} = n_s C_{FC_{core}} + C_{\,Core/weight} \tag{2.23}$$

$$C_w = C_{FC_w} + C_{\,w/weight} \tag{2.24}$$

$$C_l = C_{FC_l} + C_{\,l/weight} \tag{2.25}$$

$$C_{cap} = \mathcal{B}_a V_r + \mathrm{C}_a C_r V_r^2 \tag{2.26}$$

where n_I, n_d, n_{ind}, and n_c represent the number of IGBT modules, diode modules, inductors, and capacitors. C_{IGBT}, C_d, C_{ind}, and C_{cap} represent the cost per unit of an IGBT module, diode module, inductor, and capacitor. C_{core}, C_w, and C_l represent the cost of core, winding, and labour. $C_{FC_{core}}$, C_{FC_w}, and C_{FC_l} represents fixed costs for the core, winding, and labour. $C_{\,Core/weight}$, $C_{\,w/weight}$, and $C_{\,l/weight}$ represent cost per weight for core, winding, and labour. n_s is the stacking factor of the cores, and G_M represent gross margin of the component, which is equal to 0.75 [117]. The values of inductor cost data are highlighted in Table 2.12 [117]-[119]. V_r is the rated capacitor voltage and C_r is the rated capacitance. The values of $\mathcal{B}_a$ and C_a is highlighted in Table 2.13 [118].

Table 2.12: Cost component of an inductor

Core: Winding:	2605SA1 U-shaped core Round	N87 E-shaped core Litz	KoolMu E-shaped core Round	Vitroperm Coated toroid Round
$C_{FC_{Core}}$ (USD)	5.77	0.090	0.68	1.19
$C_{\,Core/weight}$ (USD/kg)	15.94	8.48	11.53	55.29
C_{FC_w} (USD)	1.13	0.28	0.28	0.057
$C_{\,w/weight}$ (USD/kg)	11.31	36.74	11.31	11.31
C_{FC_l} (USD)	0.85	0.85	0.85	1.13
$C_{\,l/weight}$ (USD/kg)	7.91	7.91	7.91	10.53

Table 2.13: Cost component of an aluminium electrolytic capacitor

	$\mathcal{B}_a$	C_a
AL Cap	$1.566 \times 10^{-3}\ USD/V$	$2.698 \times 10^{-3}\ USD/\mu F \cdot V^2$

B. Operation and Maintenance Cost ($C_{O\&M}$)

$C_{O\&M}$ represents the scheduled maintenance, unscheduled maintenance, and downtime costs, respectively [103]. The annual $C_{O\&M}(C_{O\&M,a})$ is given as 5% of the initial cost of the power converter configuration as defined in (2.27) [103], [120]. However, $C_{O\&M}$ is considered for the estimated lifetime of the power converter configuration and the current time value of money [121], [122]. Therefore, $C_{O\&M}$ is expressed in (2.28):

$$C_{O\&M,a} = 5\% \times C_i \tag{2.27}$$

$$C_{O\&M} = \sum_{n=1}^{N} \frac{5\% \times C_{initial}}{(1+DF)^n} \tag{2.28}$$

where N is the expected lifetime of the power converter configuration, which equals t25 years, n represents the current year, and DF represents the discount factor, which is a combination of the interest and inflation rates. The value of the discount factor is given as 2.5% for WECS [122].

C. Energy Cost (C_e)

C_e is determined by the expected operational life of the converter, the total power losses associated with the converter (P_L), and the cost of energy produced per unit ($C_{e,per\ unit}$)[121], [122]. Therefore, C_e is calculated with the expression in (2.29):

$$C_e = \sum_{n=1}^{N} \frac{P_L \cdot C_{e,per\ unit}}{(1+DF)^n} \tag{2.29}$$

where,

$$P_L = P_{LS} + P_{LP} \tag{2.30}$$

$$P_{LS} = P_{C(module)} + P_{sw(module)}$$

$$\therefore P_{LS} = (P_{C(IGBT)} + P_{C(diode)}) + (P_{sw(igbt)} + P_{sw(rec)}) \tag{2.31}$$

$$P_{LP} = P_{Loss,ind} + P_{Loss,cap}$$

$$\therefore P_{LP} = I_{rms}^2(R_{ind} + R_{ESR}) \tag{2.32}$$

where, P_{LS}, P_{LP}, $P_{Loss,ind}$ and $P_{Loss,cap}$ are the total power losses associated with the power semiconductor devices, passive devices, inductors and capacitors, respectively. $P_{C(module)}$ and $P_{sw(module)}$ represents the total conduction switching losses. $P_{C(IGBT)}$ and $P_{C(diode)}$ represents the total conduction losses associated with IGBT and power diode modules, respectively.

$P_{sw(igbt)}$ and $P_{sw(rec)}$ represents the switching losses associated with IGBT and power diode modules, respectively.

D. Cost Comparison and Discussion

The cost estimates of the power converter configurations in a transformer-less WECS and a conventional WECS are compared in this section based on the LCC model presented in (2.18). The calculation and comparison are based on the parameters stated in Tables 2.1, 2.2, and 2.14, respectively. A back-to-back power converter configuration based on a 3L-DCC topology (as shown in Figure 1.5(a)) is deployed in the conventional WECS. Also, the cost per unit of each power semiconductor device (i.e., the IGBT module and clamping diode module) are obtained from [123] and [124], respectively.

Table 2.14: Parameters of the back-to-back converter configuration

Parameters	**Symbol**	**Value**
Rated Power	P_{rated}	3 MW
Rated DC-Link Voltage	V_{dc_rated}	2 kV
Line-to-Line Output Voltage	V_{LL}	0.69 kV
Phase Current	I_{ph}	2.51 kA
Grid Frequency	F_g	50 Hz
Switching Frequency	F_{sw}	1.8 kHz
IGBT voltage rating	V_{IGBT}	1.7 kV
IGBT current rating	I_{IGBT}	3.6 kA
IGBT on-state resistance	$R_{on,IGBT}$	0.5$m\Omega$
Freewheeling diode on-state resistance	$R_{on,diode}$	0.17$m\Omega$
Clamping diode voltage rating	V_{Diode}	1.7 kV
Clamping diode current rating	I_{Diode}	3.6 kA
Upper DC-Link Capacitance	C_{dc1}	9300 μF
Lower DC-Link Capacitance	C_{dc2}	9300 μF

In Figure 2.23, the cost comparison for various power converter configurations is presented, where "A" represents the 3ph three-stage generator-converter, "B" represents the 3ph two-stage generator-converter, "C" represents the passive generator-side with 4L DC-DC converter and 4L-DCC, "D" represents the high frequency-link multilevel cascaded MV converter, "E"

represents the 2L-VSC with MSC-based resonant converter and 3L-DCC, and "F" is the back-to-back 3L-DCC. Based on Figure 2.22, the three-phase three-stage generator-converter configuration is the most expensive due to its MMC topology and high-power ratings of its power semiconductor devices. On the other hand, the passive generator-side with 4L DC-DC converter and 4L-DCC configuration is the least expensive amongst configurations deployed in a transformer-less WECS. Furthermore, the two-level converter with modular switched-capacitor based resonant converter and 3L-DCC configuration is costly because of the significant amount of series-connected IGBT modules.

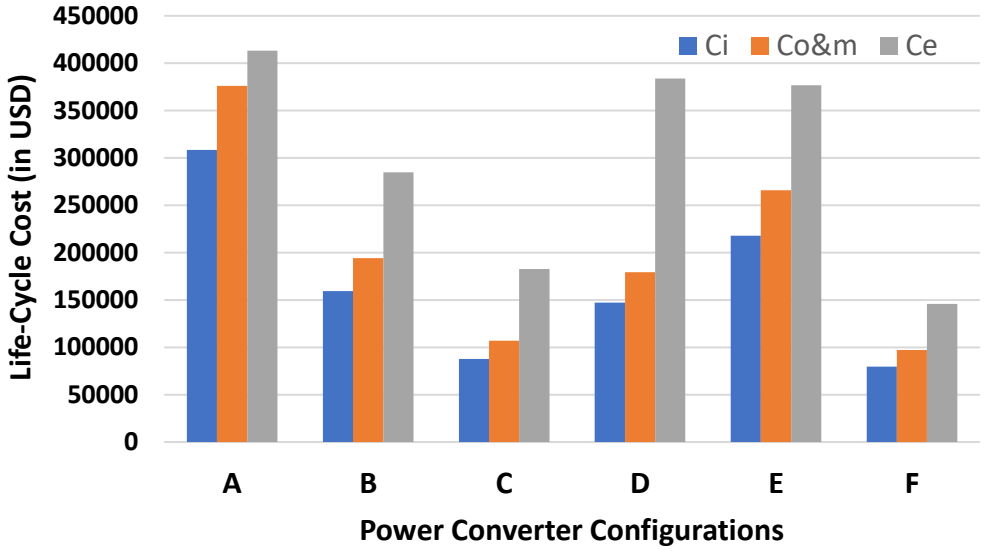


Figure 2.23: Cost comparison for various power converter configuration.

E. Summary of the Cost Benefit Analysis

From the CEL_f and GC_f evaluation carried out in the previous section, the passive generator-side with 4L DC-DC converter and 4L-DCC configuration have the least components count and acceptable grid compliance. While the 3ph three-stage generator-converter, 3ph two-stage generator-converter, and high frequency-link multilevel cascaded MV converter have higher components count than the other configurations. Furthermore, the number of components in each configuration directly affects the overall cost of the configuration. From Figure 2.23, the 3ph three-stage generator-converter configuration have the highest cost due to its high number of components and the power ratings of each component. The same trend is observed with the high frequency-link multilevel cascaded MV converter with the second highest cost component as shown in Figure 2.23.

Although, the number of switching power semiconductor devices in the 3ph two-stage generator-converter exceeds both the 3ph three-stage generator-converter configuration and high frequency-link multilevel cascaded MV converter configuration. However, the overall cost associated with the 3ph two-stage generator-converter configuration is about 42% less than the overall cost of the 3ph three-stage generator-converter configuration, as shown in Figure 2.23. The same trend occurs with the overall cost associated with the 3ph two-stage generator-converter configuration being about 10% less than the overall cost of the high frequency-link multilevel cascaded MV converter configuration, as shown in Figure 2.23. This trend is because lower rated power semiconductor devices are cheaper than higher rated power semiconductor devices.

2.4.2. LCC Analysis of the Collection system of a WPP

The LCC analysis of the collection system of a WPP is based on the developmental stage and operating period of the WPP, which consists of the capital cost (during the developmental stage (i.e., construction stage)), operation and maintenance cost, and power loss cost (during the operating period) [125], as shown in Figure 2.24.

According to Figure 2.24, the LCC of the collection system of a WPP is expressed in (2.33).

$$LCC_{col} = C_{inv} + C_{op} + C_{loss} \tag{2.33}$$

where C_{inv} is the capital cost, C_{op} is the operation and maintenance cost, and C_{loss} represents the power loss cost.

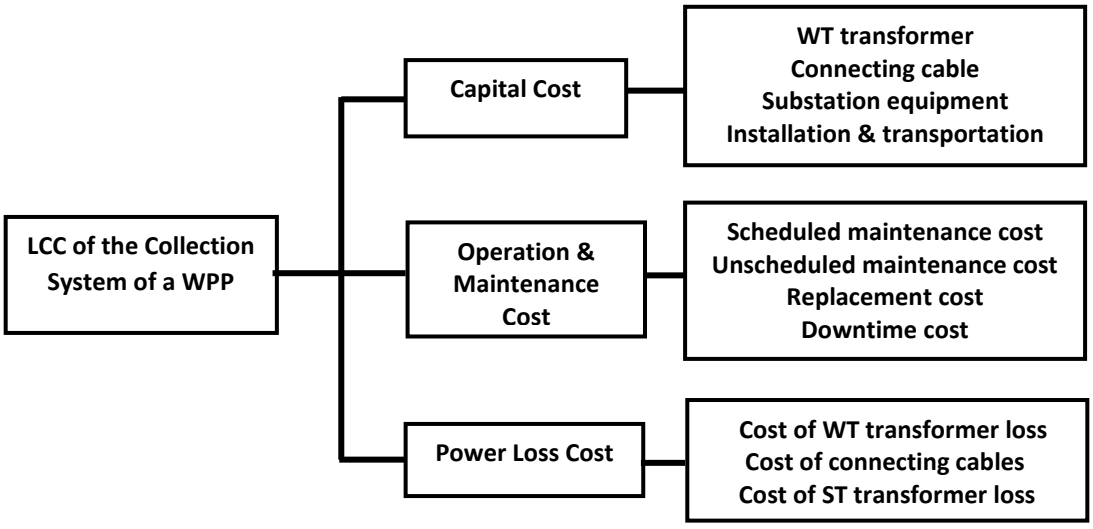


Figure 2.24: Cost structure of the collection point of a WPP.

A. Capital Cost (C_{inv})

C_{inv} of the collection system of a WPP includes the cost of transformers (C_T), the cost of connecting cable (C_{cable}), and the cost of substation equipment (i.e., substation (ST) transformer and associated equipment) (C_{sub}) [44]-[46]. Therefore, C_{inv} can be obtained, as expressed in (2.34).

$$C_{inv} = C_T + C_{cable} + C_{sub} \tag{2.34}$$

The cost of transformers (C_T) in a conventional WPP is expressed in (2.35) as stated below.

$$C_{WT} = n_T P_T \tag{2.35}$$

where, n_T is the number of WECSs in the WPP and P_T is the face value of a transformer.

The cost of connecting cable (C_{cable}) of the collection system consists of the cost of the medium voltage cable (C_{MV_c}), the cost of the high voltage cable (C_{HV_c}), the cost of installation (C_{ins}) and the cost of transportation (C_{tran}) [44]-[46]. Therefore, C_{cable} is expressed in (2.36) as stated.

$$C_{cable} = C_{MV_c} + C_{HV_c} + C_{ins} + C_{tran} \tag{2.36}$$

$$C_{MV_c} = \left(\sum_{f=1}^{N_f} \sum_{s=1}^{N_s} C_{mv_{unit}} L_s\right) \tag{2.37}$$

$$C_{HV_c} = \left(\sum_{sub=1}^{N_{sub}} C_{hv_{unit}} L_{hv}\right) \tag{2.38}$$

where, N_{sub}, N_f, and N_s are the numbers of the substation, the number of feeders and the number of strings connected in a feeder, $C_{mv_{unit}}$ and $C_{hv_{unit}}$ are the unit price of the medium voltage cable and the unit price of the high voltage cable, L_s is the length of each string, and L_{hv} is the length of the high voltage cable.

The cost of substation equipment (C_{sub}) mainly consists of the cost of the substation transformer (C_{ST}) and the cost of associated substation equipment ($C_{assoc.}$) (such as switch gears, protection relays and control devices) [45]. Therefore, C_{sub} is expressed in (2.31).

$$C_{sub} = \sum_{sub=1}^{N_{sub}} n_{ST} P_{ST} + C_{assoc.} \tag{2.39}$$

where, n_{ST} is the number of substations in the WPP and P_{ST} is the unit price of a substation transformer.

B. Operation and Maintenance Cost (C_{op})

C_{op} of the collection system of a WPP includes scheduled maintenance cost, unscheduled maintenance cost, replacement cost and downtime cost [44]-[46], [103]. Based on the literature, the operation and maintenance cost are about 15% of the capital cost annually [120]. The annual operation and maintenance cost ($C_{op,a}$) of the collection system is expressed in (2.40).

$$C_{op,a} = 15\% \times C_{inv} \tag{2.40}$$

Also, the operation and maintenance cost of the collection system from its developmental stage of the WPP to the end-of-life period of the WPP is expressed in (2.41).

$$C_{op} = \sum_{n=0}^{N-1} \frac{15\% \times C_{inv}}{(1+DF)^n} \tag{2.41}$$

where N is the expected lifetime of the WPP which equals to 25 years, n represent the current year, and DF represents the discount factor, which is a combination of the interest and inflation rates. The value of the discount factor is given as 2.5% for WECS [122], [126].

C. Power Loss Cost (C_{loss})

The power loss cost of the collection point of a WPP consists of the cost of transformer losses ($C_{loss,T}$), the cost of connecting cable losses ($C_{loss,cable}$), and cost of substation transformer losses ($C_{loss,ST}$), as expressed in (2.42) [127], [128].

$$C_{loss} = C_{loss,T} + C_{loss,cable} + C_{loss,ST} \tag{2.42}$$

$$C_{loss,WT} = \alpha NL_{loss} + \beta L_{loss} \tag{2.43}$$

$$C_{loss,cable} = \sum_{sub=1}^{N_{sub}} \left[\sum_{f=1}^{N_f} \sum_{s=1}^{N_s} \left(I_{MV_c}^2 R_{MV_c} + I_{HV_c}^2 R_{HV_c} \right) \right] tP_{grid} \tag{2.44}$$

Where,

$$\alpha = E_e \times O_{pa} \times \frac{[(1+i)^N - 1]}{i \times (1+i)^N} \times 10^{-6} \tag{2.45}$$

$$\beta = \alpha \times L^2 \tag{2.46}$$

where α is the no-load loss cost rate, NL_{loss} is the no-load loss of the transformer, β is the load loss cost rate, L_{loss} is the load loss of the transformer, I_{MV_c} is the current flowing through the medium voltage connecting cable, R_{MV_c} is the resistance of the MV connecting cable, I_{HV_c} is the current flowing through the HV connecting cable, R_{HV_c} is the resistance of the HV

connecting cable, E_e energy cost per unit, O_{pa} is the transformer operating hours per annum, i is the interest rate, N is the expected lifetime of the transformer, and L is the transformer loading.

2.4.3. Case Study

In this section, the LCC model presented in section 2.4.2 is used to analyse the associated cost of the collection system of two existing WPPs (i.e., WPP-A and WPP-B). The derived cost of the WPPs is compared with WPPs with transformer-less WECSs. The main parameters of WPP-A and WPP-B are stated in Table 2.15, as obtained from [44] and [45].

Table 2.15: Parameters of the collection system of WPP-A and WPP-B [44], [45]

Parameters	**WPP-A**	**WPP-B**
Number of Wind Turbines	280	259
Power Rating of each turbine	2 MW	3.6 MW
Number of Transformer	280	259
Transformer Power Rating	2.2 MVA	4.1 MVA
Transformer Voltage Rating	35 kV	35 kV
Collector Cable (MV) Voltage Rating	35 kV	35 kV
Transmission Cable (HV) Voltage Rating	150 kV	220 kV
Collector Cable (MV) Length	339.12 km	517 km
Transmission Cable (HV) Length	15 km	50 km
Number of Substation Transformer	4	6
Substation Transformer Power Rating	150 MVA	220 MVA
Number of Medium Voltage GIS	28	56
Number of High Voltage GIS	4	6
Collection System Topology	Radial	Double-sided Ring

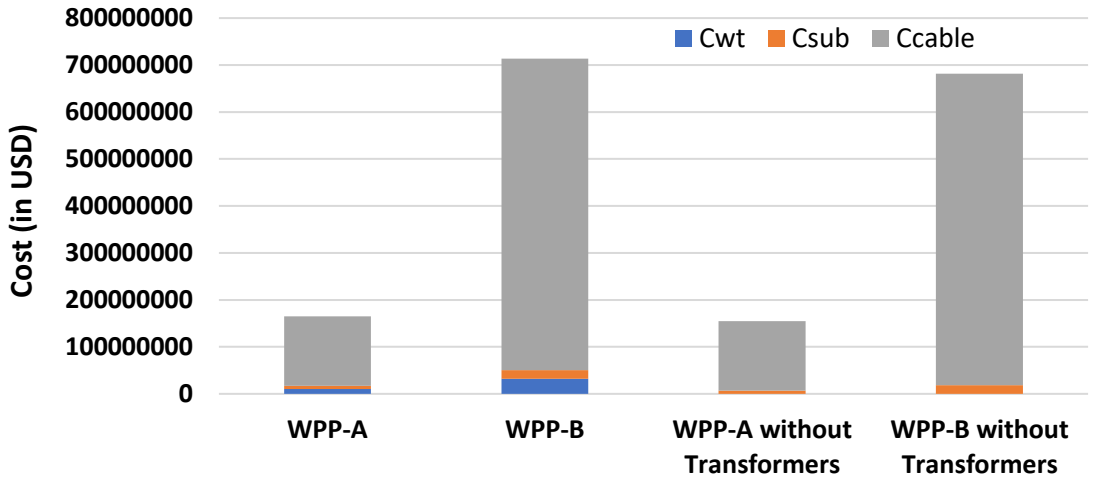
A. Comparative Evaluation

From the cost model of the collector system presented in [44] and [45], the capital cost, operation and maintenance cost, and power loss cost of two existing WPPs (i.e., WPP-A and WPP-B) and counterpart WPPs without transformers are compared and evaluated. The initial capital cost of deploying the collection system of WPP-A, WPP-B, WPP-A without transformers, and WPP-B without transformers, respectively, is illustrated in Figure 2.25(a). The C_{cable} of the WPP-B is about four times more than that of the WPP-A because of the double-sided ring topology and the extensive length of the connecting cable [45]. The double-

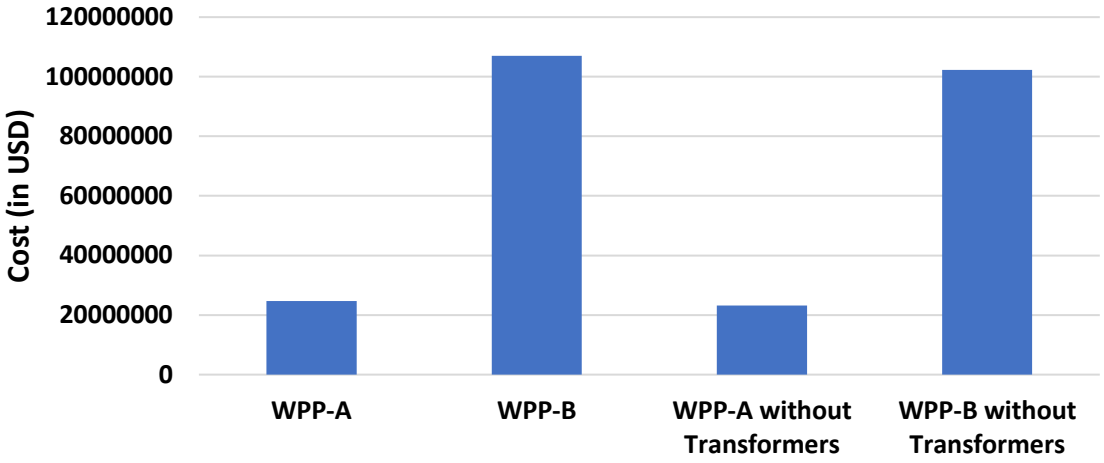
sided ring topology provides a dual power flow path in the collection system, allowing a redundancy level in the system [45].

Furthermore, the C_{inv} of a WPP-B without transformers is about 5% less than that of WPP-B. While the C_{inv} of a WPP-A without transformers is about 7% less than that of WPP-A because the number of wind turbines in WPP-A is greater than WPP-B, as stated in Table 2.10. A similar trend is observed in the annual $C_{op,a}$ of the WPP-A, WPP-B, WPP-A without transformers, and WPP-B without transformers, respectively, as shown in Figure 2.25(b).

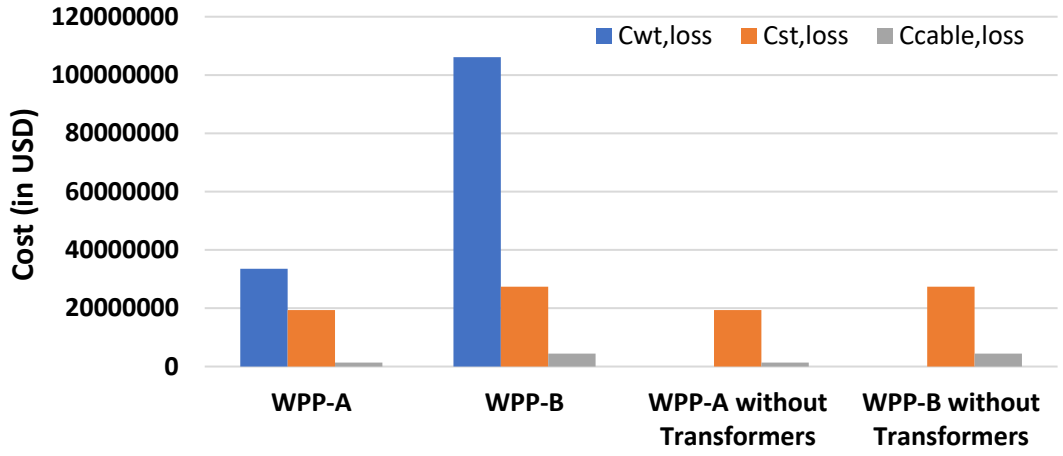
The breakdown of the power loss cost associated with the collection system of WPP-A, WPP-B, WPP-A without transformers, and WPP-B without transformers is illustrated in Figure 2.25(c). The power loss cost associated with the collection system of WPP-B is almost three times greater than the power loss cost of WPP-A because of the more significant power ratings of both its transformer and substation transformer. The collector cable length of WPP-B is almost twice the length of WPP-A. The power loss cost of the collection system of WPP-A without transformers is nearly three times the power loss cost of the collection system of WPP-A. Furthermore, the power loss cost of the collection system of WPP-B without transformers is about four times the power loss cost of the collection system of WPP-B. The total cost of the collection system of WPP-B is four times greater than the collection system of WPP-A, mainly due to the established factors discussed in the paragraph above. While the total cost of the collection system of WPP-A without transformers is about 23% less than the total cost of the collection system of WPP-A, as shown in Figure 2.25(d). Furthermore, the total cost of the collection system of WPP-B without transformers is about 18% less than the total cost of the collection system of WPP-B.



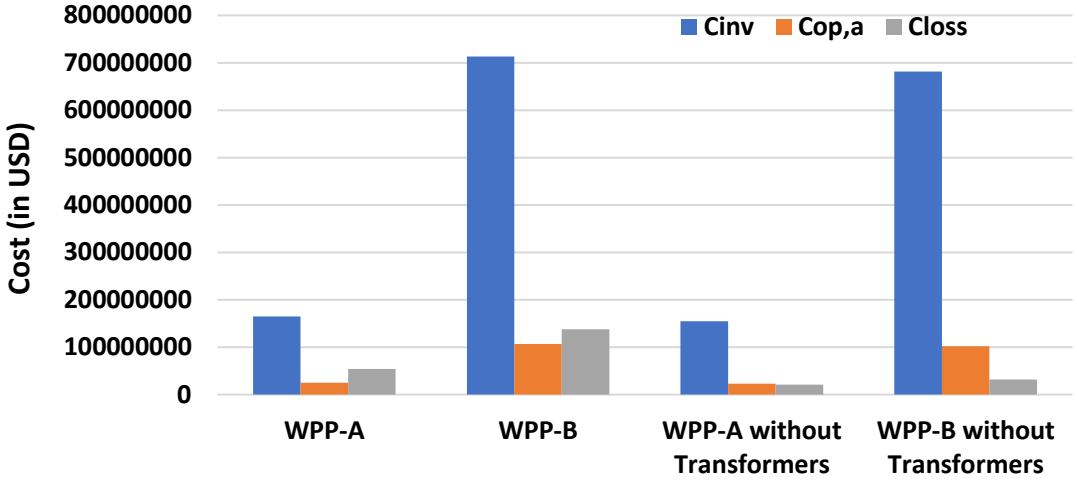
(a)



(b)



(c)



(d)

Figure 2.25: Cost comparison of the four different types of WPP, (a) capital cost, (b) annual operation and maintenance cost, (c) yearly power loss cost, and (d) total cost.

A. Sensitivity Analysis

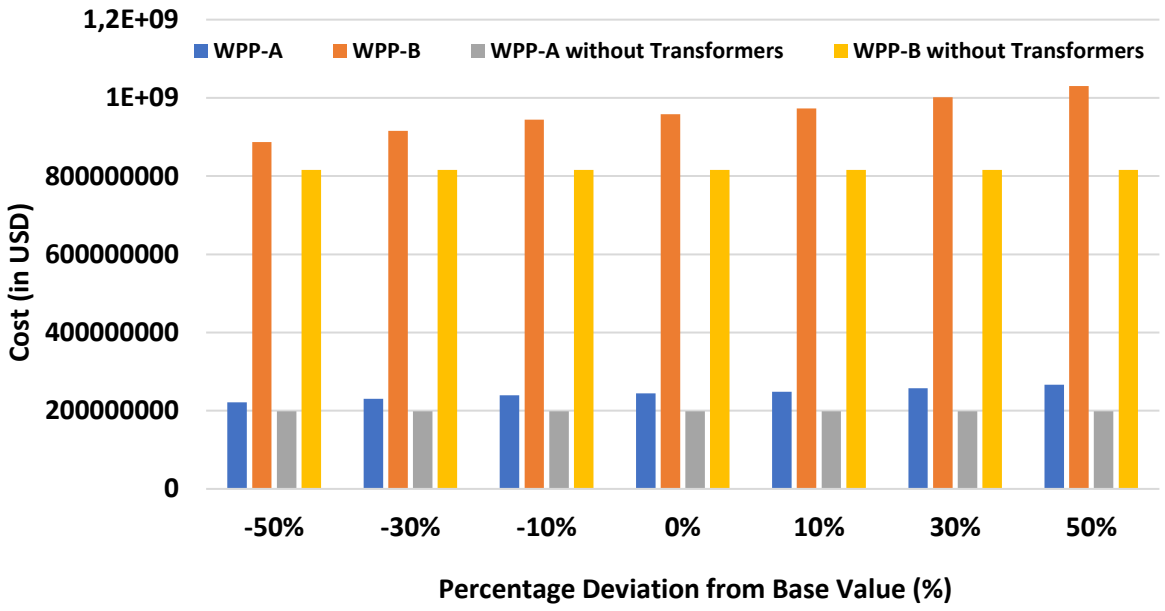
In the previous cost analyses, fixed values were obtained from the LCC model's main components (2.25). These values vary for different WPPs based on changes in specific parameters [45]. As discussed previously, the main parameters that affect the cost components are stated as follows: the number of wind turbines, power ratings of the wind turbine, collector cable length, and the cost of substation equipment.

Figures 2.26(a) to 2.26(d) illustrate the sensitivity bar graphs for the number of wind turbines, power ratings of the wind turbine, collector cable length, and cost of substation equipment, respectively, as functions of percentage deviation from the base value (which is the total overall cost presented in Figure 2.25(d)). From the presented graphs, the following observations were obtained from the four highlighted parameters:

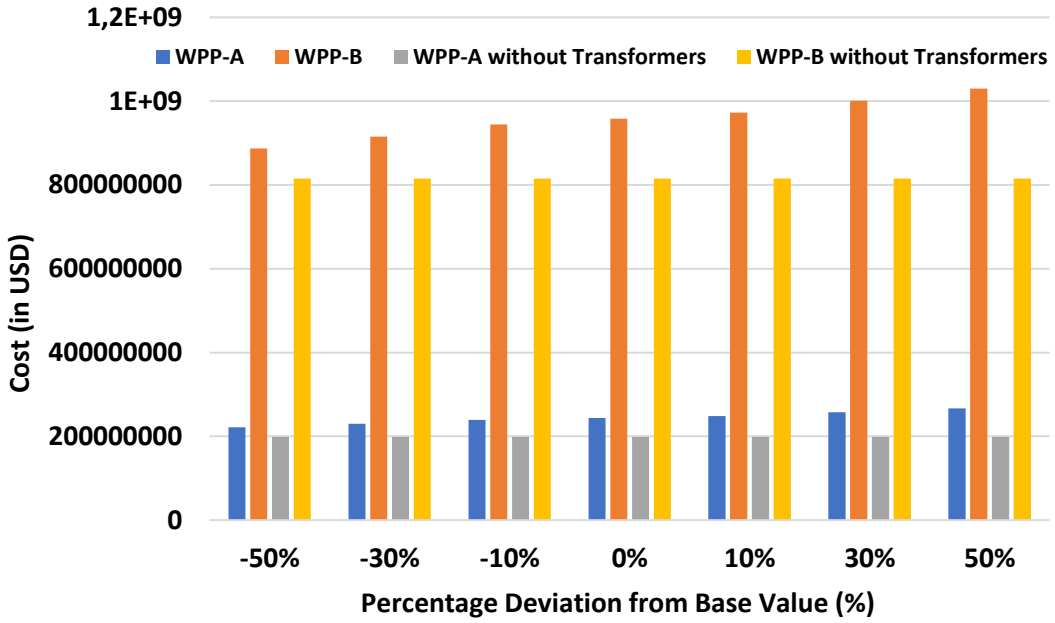
1) By increasing the number of wind turbines in WPP-A from 280 to 420 (i.e., 50% increase), the total cost of the collection system of WPP-A without transformers is about 34% less than the total cost of the collection system of WPP-A. On the other hand, by decreasing the number of wind turbines in WPP-A by 50%, the total cost of the collection system of WPP-A without transformers is about 11% less than the total cost of the collection system of WPP-A, as illustrated in Figure 2.26(a).
2) Using higher power rated wind turbines in WPP-B (i.e., 4.7 MW), or by deploying lower power rated wind turbines (i.e., 2.52 MW), the transformers deployed in WPP-B will be rated at 5.33 MVA, and 2.87 MVA, respectively. A comparative evaluation of the total cost of the collection system of a WPP-B with a 5.33 MVA transformers and a total cost of the collection system of a WPP-B without a 5.33 MVA transformers show a 23% decrease in total cost as shown in Figure 2.26(b).
3) By increasing the collector cable length by 10% in WPP-A and WPP-A without transformers, the total cost of the collection system of WPP-A without transformers is about 20.9% less than the total cost of the collection system of WPP-A. While increasing the collector cable length by 50% in WPP-A and WPP-A without transformers, respectively, results in the total cost of the collection system of WPP-A without transformers being about 15.8% less than the total cost of the collection system of WPP-A, as illustrated in Figure 2.26(c). On the other hand, decreasing the collector cable length by 50% in WPP-B and WPP-B without transformers results in the total cost of WPP-B without transformers being about 33% less than the total cost of the

collection system of WPP-B. Furthermore, decreasing the collector cable length by 30% in WPP-B and WPP-B without transformers results in the total cost of WPP-B without transformers being about 24.4% less than the total cost of the collection system of WPP-B.

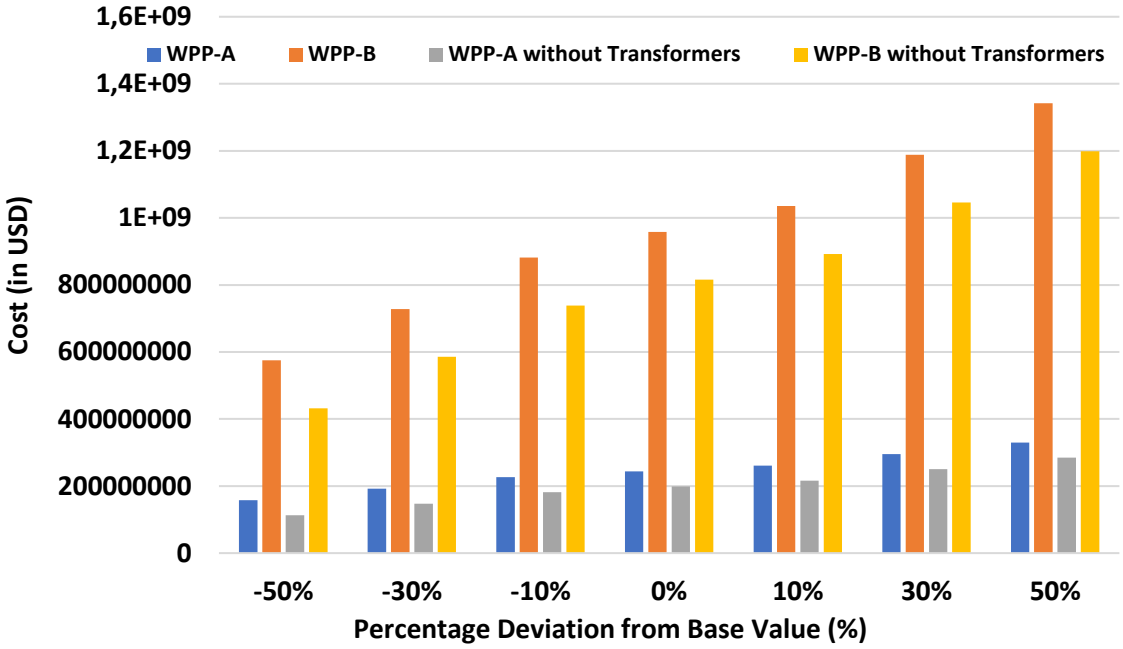
4) The cost of substation equipment (C_{sub}) is another critical parameter that affects the total of the collection point, as illustrated in Figure 2.26(d). A 50% increase in C_{sub} WPP-A and WPP-A without transformers, respectively, results in the total cost of the collection system of WPP-A without transformers being about 22.2% less than the total cost of the collection system WPP-A. While a 30% increase in C_{sub} of WPP-A and WPP-A without transformers, respectively, results in the total cost of the collection system of WPP-A without transformers being about 22.4% less than the total cost of the collection system WPP-A. Furthermore, a 50% increase in C_{sub} of WPP-B and WPP-B without transformers, respectively, results in the total cost of the collection system of WPP-B without transformers being about 17.2% less than the total cost of the collection system of WPP-B. On the other hand, a 50% decrease in C_{sub} of WPP-B and WPP-B without transformers, respectively, results in the total cost of the collection system of WPP-B without transformers being about 17.7% less than the total cost of the collection system of WPP-B.



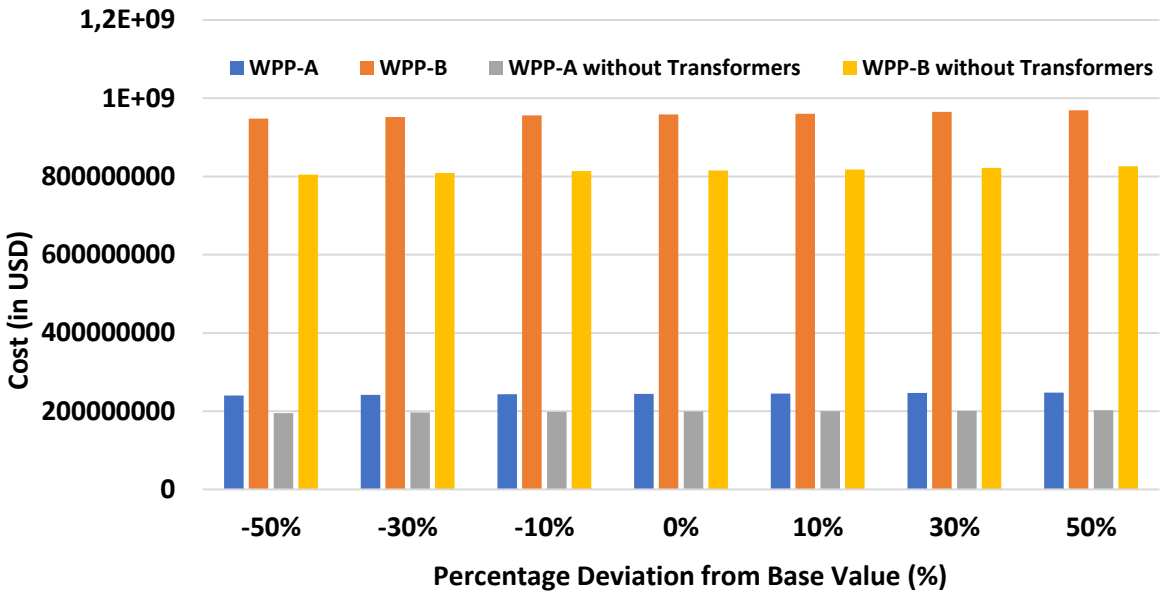
(a)


1,2E+09
1E+09
800000000
600000000
400000000
200000000
0
Cost (in USD)
WPP-A
WPP-B
WPP-A without Transformers
WPP-B without Transformers
-50%
-30%
-10%
0%
10%
30%
50%
Percentage Deviation from Base Value (%)

(b)


1,6E+09
1,4E+09
1,2E+09
1E+09
800000000
600000000
400000000
200000000
0
Cost (in USD)
WPP-A
WPP-B
WPP-A without Transformers
WPP-B without Transformers
-50%
-30%
-10%
0%
10%
30%
50%
Percentage Deviation from Base Value (%)

(c)



(d)

Figure 2.26: Sensitivity bar graphs of four parameters, (a) number of wind turbines, (b) power ratings, (c) collector cable length, and (d) cost of substation equipment.

2.5. Conclusion

This chapter introduced the power converter configurations overview of existing transformer-less WECS by classifying them into two categories: generator-converter configuration and three-stage power converter configuration. The features and drawbacks of the various power converter configurations under each classified category have been discussed extensively.

A comparative benchmark factor (CBF) has been proposed to assess the existing power converter configuration suitability for transformer-less WECS application. Therefore, the number of active and passive devices, the voltage level of the respective topology, and the total number of switching states of the active devices have been used to assess the reliability, cost, and grid compliance of the configuration.

In terms of cost comparison, the three-stage power converter configuration is more cost-effective than the generator-converter configuration. Furthermore, the cost-benefit analysis of deploying a transformer-less WECSs in a WPP is evaluated and compared with conventional WECS in a WPP based on power converter configurations and collection system. Overall, the total cost of the collection system of WPP with transformer-less WECSs is about 23% less than the total cost of WPP with conventional WECs (i.e., with wind turbine transformers).

Also, a sensitivity analysis on four main parameters (namely: number of wind turbines, power ratings of the wind turbine, collector cable length, and the cost of substation equipment) that affect the total cost of the collection system of a WPP was studied. The two most sensitive parameters are the number of wind turbines and collector cable length.

Chapter 3

Nested Neutral-Point-Clamped (NNPC) and Modified NNPC Converter (MNNPC)

This chapter examines the theoretical analysis, design, and simulation of the NNPC and MNNPC converter topologies deployed in a transformer-less WECS configuration. In the previous chapter, the power converter configuration with a 4L-DCC topology at its grid-side has better reliability, cost-effectiveness, and efficiency. However, the clamping diodes and dc-link capacitors of the DCC topology increases significantly at higher voltage levels ($V_L \geq 4$) [31], [71], [88], [95]. These highlighted drawbacks could be minimized by deploying either an NNPC converter topology [129], [130] or an MNNPC converter topology at the power conversion stage of a transformer-less WECS. While the 4L-NNPC and 5L-NNPC converter topology has been presented in the literature [129], [130], a theoretical analysis of their derivation and design for transformer-less WECS application is an existing gap in the literature. Furthermore, a novel 7L-MNNPC converter topology is derived using a 4L-NNPC converter topology as building cells. Furthermore, the impacts of different voltage sag propagation in a WPP with transformer-less WECS and conventional WECS are presented in this chapter.

Therefore, the main parts of this chapter are organized as follows: background and derivations of the NNPC and MNNPC converter topology are presented in Section 3.1. The converter design for a transformer-less WECS is presented in Section 3.2. Also, the grid-connected converter model is presented in Section 3.3. The simulation results to validate the converter design and grid-connection scenarios have been presented in Section 3.4.

3.1. Background and Derivations

An NNPC converter topology is a combination of a DCC and FC converter topologies to create a multilevel topology with minimized clamping devices (i.e., clamping diodes and clamping capacitors) and split dc-link capacitor configuration [129], [130]. The NNPC converter topology can also be utilized as a converter cell to derive other topology variants.

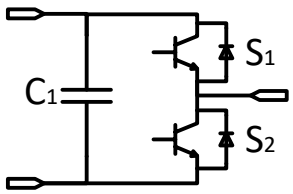
The NNPC converter topology is directly derived from the generalized multilevel topology method presented in [131]. The generalized multilevel topology consists of two-level converter cells with complementary IGBT modules, as shown in Figure 3.1(a). These two-level converter cells are connected in parallel for each structure and cascaded in a series connection to achieve a specific voltage level, as depicted in Figure 3.1(b). Due to the excessive utilization of IGBT modules, clamping capacitors, and dc-link capacitors, the generalized topology is simplified according to the following derivation principles [132]:

1. The IGBT devices in the outer structure must not be eliminated to enable the current flow from the dc-link voltage to the converter output during the first and final switching interval, stated in Table 3.1.

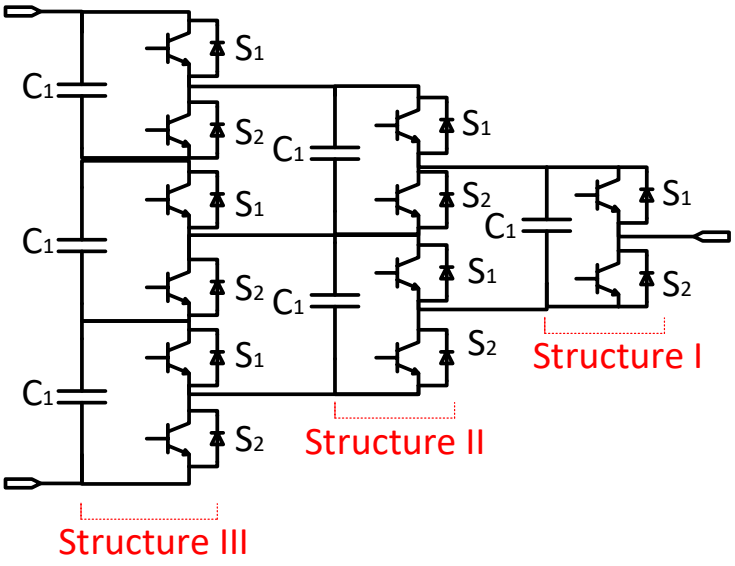
2. The inner IGBT devices in structure III is eliminated, and internal IGBT devices in structure II is replaced with clamping diodes to create a current path. Also, the inner clamping capacitor in the structure gets eliminated.

3. A current path must exist that allows the bi-directional flow from the dc-link to the output and vice-versa. Therefore, the current flowing into the midpoint of the dc-link must be equal to the current flowing out.

4. The dc-link capacitors must be simplified into two capacitors forming a split configuration.



(a)



(b)

Figure 3.1: Generalized multilevel topology (a) two-level converter cell. (b) a 1ph four-level generalized multilevel topology.

3.1.1. Derivation of a Four-Level NNPC Converter Topology

Based on the 1ph four-level (4L) generalized multilevel topology shown in Figure 3.1(b) and the derivation principles stated, a 1ph 4L-NNPC converter topology is derived with minimized clamping devices [129], [132]. This topology consists of three pairs of complementary IGBTs, a couple of clamping capacitors, and a pair of clamping diodes, as shown in Figure 3.2.

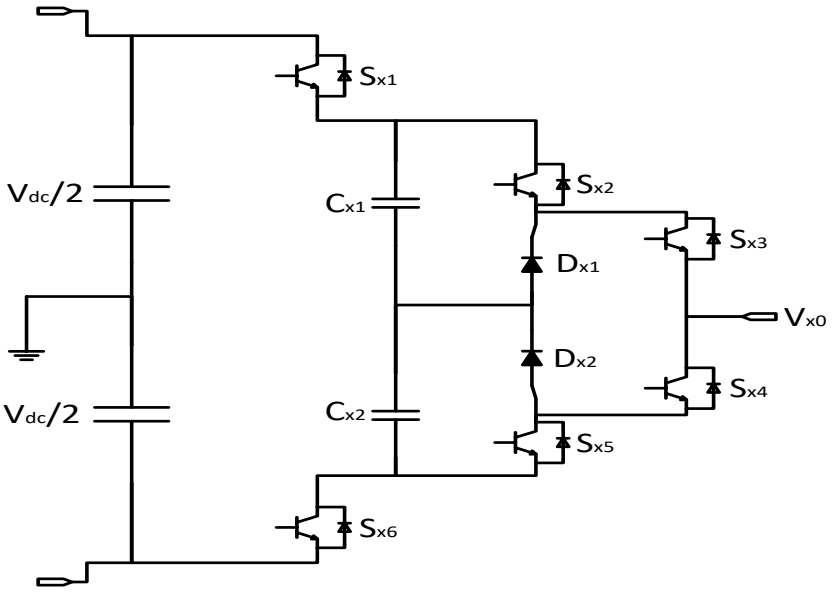


Figure 3.2: 1ph 4L-NNPC converter topology.

A. Operating Principle

The six possible switching states of the IGBTs generates the four-level voltage levels [129], as stated in Table 3.1. The voltage across the IGBTs and clamping capacitors are rated at one-third of the dc-link voltage [129]. Also, the impact of the ac-side current on the clamping capacitor voltages (V_{cx1} & V_{cx2}) is highlighted in Table 3.1. The extra switching states of the converter topology in voltage levels; $V_{dc}/6$ and $-V_{dc}/6$ which are utilized for voltage balancing control and fault-tolerant schemes [133].

Table 3.1: Switching states of a 4L-NNPC converter.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{cx1}	V_{cx2}	V_{xo}	Switching State
1	1	1	0	0	0	N	N	$V_{dc}/2$	1
1	0	1	1	0	0	C	N	$V_{dc}/6$	2
0	1	1	0	0	1	D	D	$V_{dc}/6$	2.1
1	0	0	1	1	0	C	C	$-V_{dc}/6$	3
0	0	1	1	0	1	N	D	$-V_{dc}/6$	3.1
0	0	0	1	1	1	N	N	$-V_{dc}/2$	4

N: No Impact; C: Charging; D: Discharging

B. Mathematical Model

The output phase voltage (V_{xo}) of the converter, with x represent the phase (a, b, or c) is expressed in (3.1) [133].

$$V_{xo} = [S_{x1}\frac{V_{dc}}{2} + (1 - S_{x1})(V_{cx1} + V_{cx2}) + (S_{x2} - 1)V_{cx1} + (S_{x3} - 1)V_{cx2}] \quad (3.1)$$

The current flowing through the clamping capacitors C_{x1} and C_{x2} is expressed in (3.2) and (3.3).

$$i_{Cx1} = (S_{x1} - S_{x2}) \cdot i_x \quad (3.2)$$

$$i_{Cx2} = (S_{x6} - S_{x5}) \cdot i_x \quad (3.3)$$

where S_{x1}, S_{x2}, S_{x3}, S_{x5} and S_{x6} are the power switches, i_{Cx1} and i_{Cx2} are the current flowing through C_{x1} and C_{x2}, V_{dc} represents the dc-link voltage, V_{cx1} and V_{cx2} are the voltage across each clamping capacitors C_{x1} and C_{x2}, and i_x is the output phase current of the converter. Therefore, a 3ph 4L-NNPC converter topology is shown in Figure 3.3.

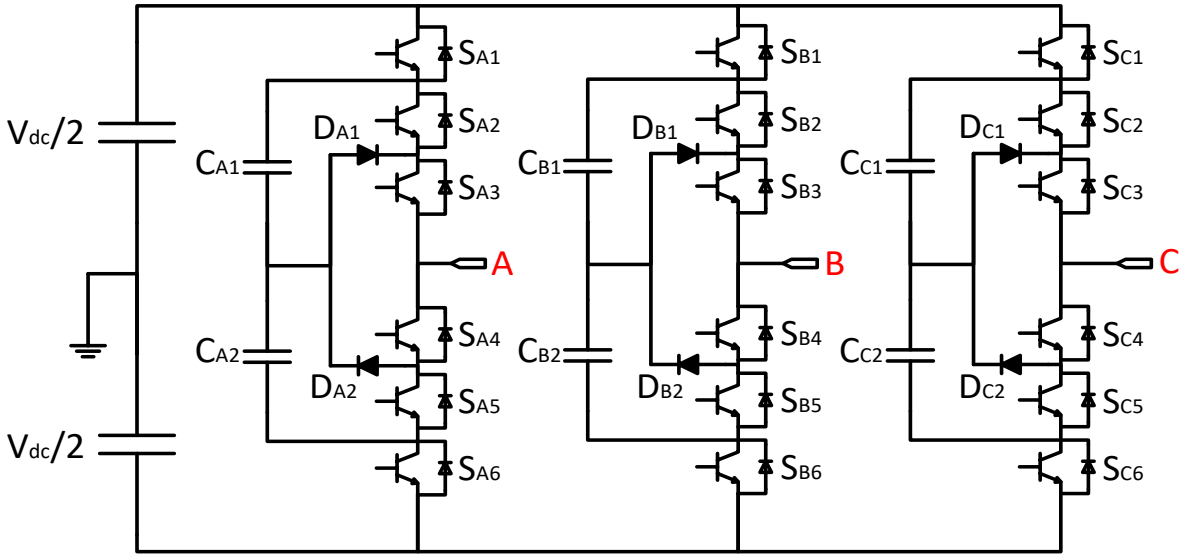
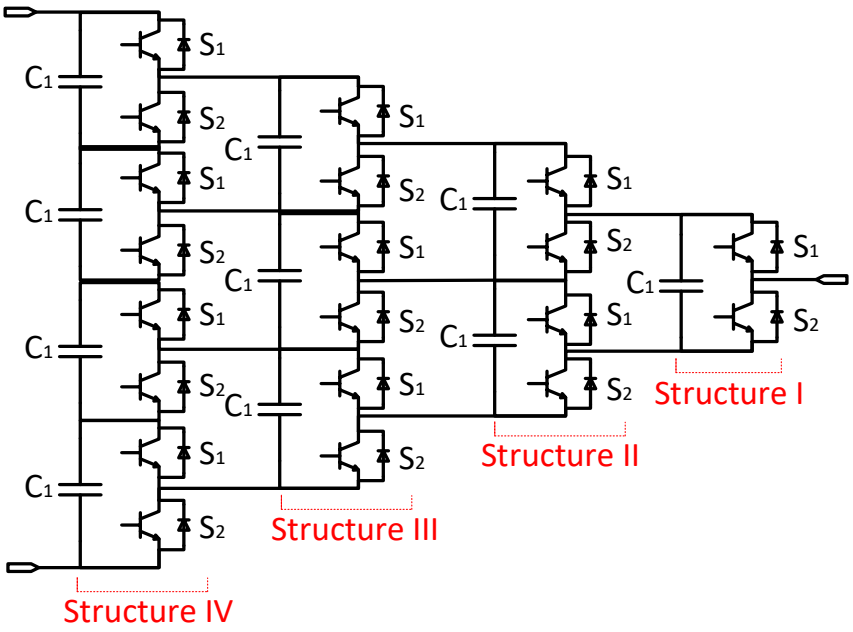


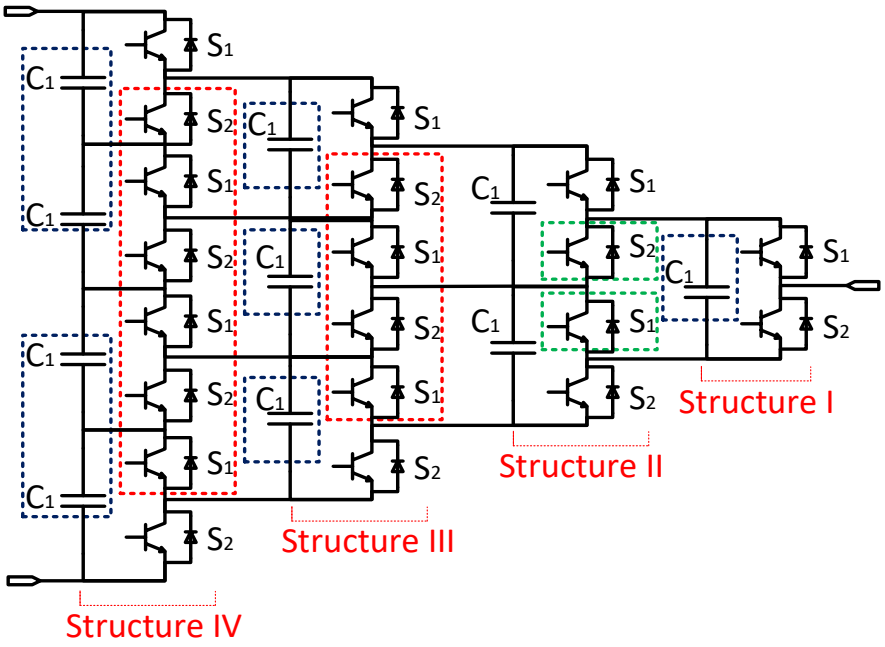
Figure 3.3: 3ph 4L-NNPC converter topology.

3.1.2. Derivation of a Five-Level NNPC Converter Topology

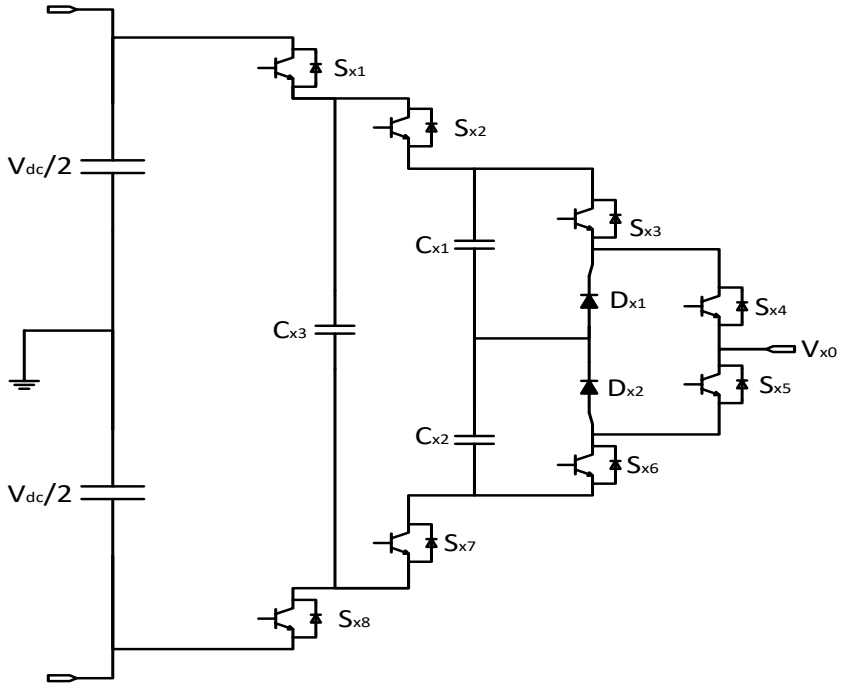
A 1ph 5L-NNPC converter topology is derived from a 1ph five-level (5L) generalized multilevel converter topology and the derivation principles presented previously, as depicted in Figures 3.4(a) to 3.4(c). According to the second derivation principle, the power switches within structure IV is eliminated to simplify the topology, as illustrated in Figure 3.4(b). Also, the capacitors in structure IV are combined to form the split-link dc-bus configuration, while the series-connected clamping capacitors in structure III are combined to form C_{x3} and the clamping capacitor in structure I is eliminated, as illustrated in Figure 3.4(c). The inner most power switches in structure II are replaced by two clamping diodes (D_{x1}, D_{x2}) to create a current flow path from inner clamping capacitors (C_{x1}, C_{x2}) to the other parts of the converter topology, as shown in Figure 3.4(c). The switching states of the 5L-NNPC converter topology is highlighted in Table 3.2.


C1
S1
S2
Structure I
Structure II
Structure III
Structure IV

(a)


C1
S1
S2
Structure I
Structure II
Structure III
Structure IV

(b)



(c)

Figure 3.4: Derivation of a 1ph 5L-NNPC converter topology. (a) generalized multilevel topology. (b) eliminated components from the generalized multilevel topology. (b) a 1ph 5L-NNPC converter topology.

Table 3.2: Switching states of a 5L-NNPC converter.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{cx1}	V_{cx2}	V_{cx3}	V_{xo}	Switching State
1	1	1	1	0	0	0	0	N	N	N	$V_{dc}/2$	1
1	1	0	1	1	0	0	0	C	N	N	$V_{dc}/4$	2
0	1	1	1	0	0	0	1	N	N	D	$V_{dc}/4$	2.1
1	0	1	1	0	0	1	0	D	D	C	$V_{dc}/4$	2.2
1	1	0	0	1	1	0	0	C	C	N	0	3
1	0	0	1	1	0	1	0	N	D	C	0	3.1
0	1	0	1	1	0	0	1	C	N	D	0	3.2
0	0	1	1	0	0	1	1	D	D	N	0	3.3
0	0	0	1	1	0	1	1	N	D	N	$-V_{dc}/4$	4
1	0	0	0	1	1	1	0	N	N	C	$-V_{dc}/4$	4.1
0	1	0	0	1	1	0	1	C	C	D	$-V_{dc}/4$	4.2
0	0	0	0	1	1	1	1	N	N	N	$-V_{dc}/2$	5

N: No Impact; C: Charging; D: Discharging.

A. Operating Principle

This topology consists of four pairs of complementary power switches, three clamping capacitors, and a pair of clamping diodes, as illustrated in Figure 3.4(b). Each IGBT of the topology is rated at a quarter of the dc-link voltage, while the inner clamping capacitors ($C_{x1}$and

C_{x2}) are also rated at a quarter of the dc-link voltage and the outer clamping capacitor (C_{x3}) is rated at three-quarters of the dc-link voltage [130]. According to Table 3.2, the impact of highlighted switching states and positive phase current on the clamping capacitor voltages is stated.

B. Mathematical Model

The output phase voltage (V_{xo}) where x represents the phase (a, b, or c) is given below.

$$V_{xo} = [S_{x1}\frac{V_{dc}}{2} + (S_{x1} + S_{x2})V_{cx3} + S_{x2}(V_{cx1} + V_{cx2}) + (S_{x3} - 1)V_{cx1} + (S_{x4} - 1)V_{cx2}] \quad (3.4)$$

The current flowing through the clamping capacitors C_{x1}, C_{x2}, and C_{x2} are expressed as follows.

$$i_{Cx3} = (S_{x1} - S_{x2}) \cdot i_x \quad (3.5)$$

$$i_{Cx1} = (S_{x2} - S_{x3}) \cdot i_x \quad (3.6)$$

$$i_{Cx2} = (S_{x7} - S_{x6}) \cdot i_x \quad (3.7)$$

where S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x6} and S_{x7} are the power switches, i_{Cx1}, i_{Cx2}, and i_{Cx3} are the current flowing through C_{x1}, C_{x2}, and C_{x3}; V_{dc} is the dc-link voltage; V_{cx1}, V_{cx2}, and V_{cx3} are the voltages across the clamping capacitors and i_x represents the output phase current. A 3ph 5L-NNPC converter topology is shown in Figure 3.5.

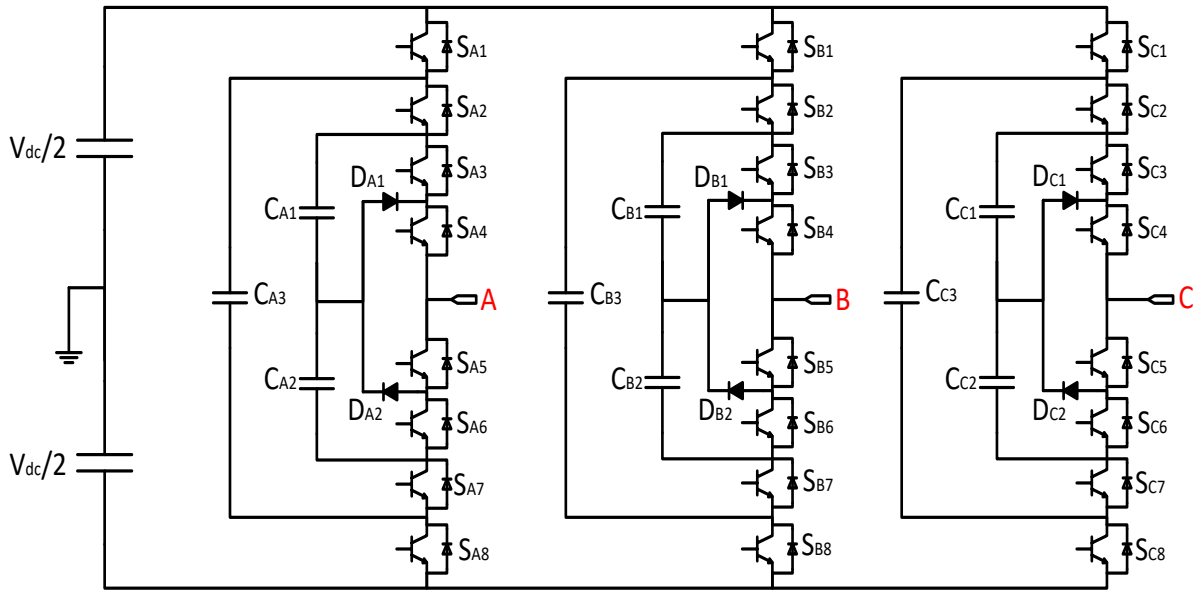


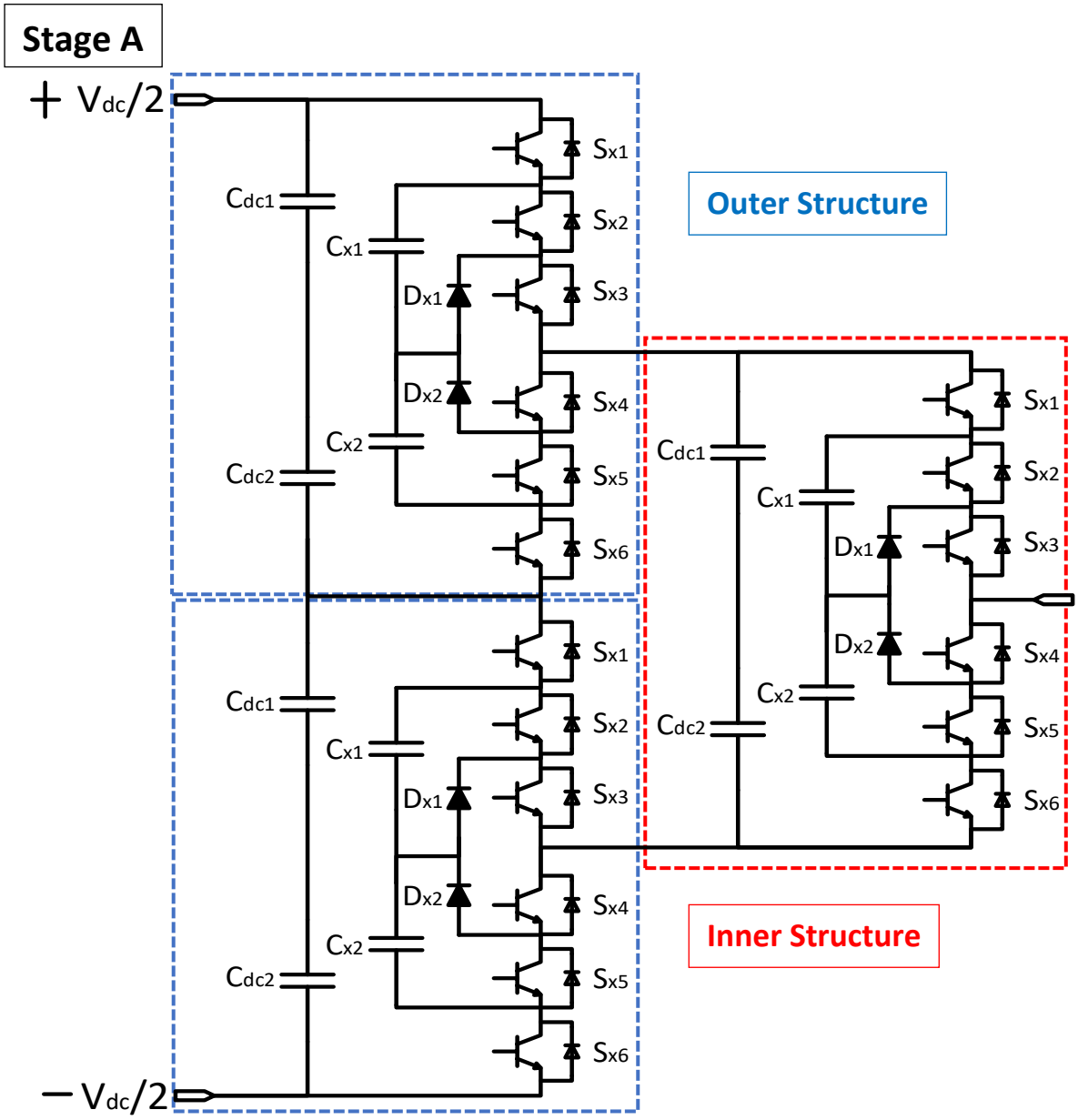
Figure 3.5: 3ph 5L-NNPC converter topology.

3.1.3. Derivation of a Seven-Level MNNPC Converter Topology

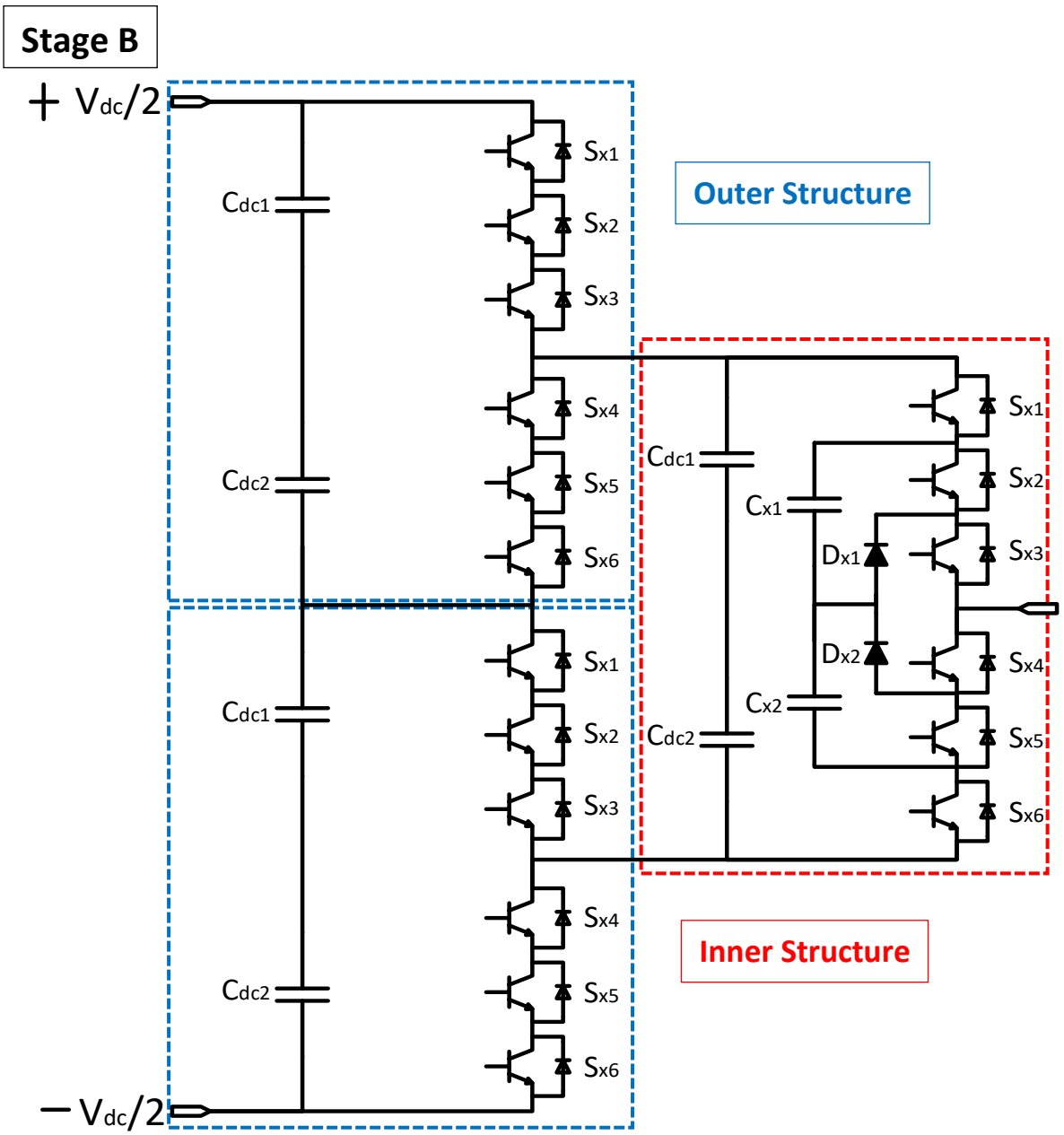
The MNNPC converter topology is derived from an extended version of the generalized multilevel converter topology based on the parallel-series connection of existing NNPC converter cells. Therefore, the MNNPC converter topology reduces the clamping capacitors in a higher-order multilevel converter topology.

The 7L-MNNPC converter topology is derived using the parallel-series connection method, deploying a 4L-NNPC converter topology as the primary cell because bi-directional current flow exists between its dc-link and output terminal, as stated previously. These 4L-NNPC converter cells are arranged into two structures: inner structure and outer structure, as illustrated in Figure 3.6(a). Hence, the derivation of a 1ph 7L-MNNPC converter topology is obtained in three stages: stage A, stage B, and stage C. In stage A, the outer structure consists of two 4L-NNPC cells connected in parallel, while the inner structure comprises one 4L-NNPC cell connected in series to the external structure. Figure 3.6(a) shows that the converter topology structure consists of multiple components that make it impractical for industrial applications.

According to the simplification principles of a generalized converter topology discussed in Section 3.1, the converter topology structure is further simplified in Stages B and C, respectively. In Stage B, the outermost power semiconductor devices must be maintained in the generalized converter topology to enable current flow from the dc-link to the converter output [132]. The clamping diodes and capacitors in the two 4L-NNPC converter cells of the outer structure are eliminated according to principles stated in Section 3.1 (as discussed earlier), as depicted in Figure 3.8(b). Also, the capacitors of the external structure are reduced to two series-connected capacitors based on principle four stated previously, as shown in Figure 3.6(b). In the final stage, the pair of clamping diodes of the 4L-NNPC converter cell in the inner structure is replaced with two IGBTs to create a bi-directional current path from the outer structure to the output of the internal structure, as depicted in Figure 3.6(c). The clamping capacitors in the inner structure are retained to maintain a current flow path in the modified converter topology. Therefore, the IGBTs in the outer structure is three times the voltage ratings of the inner structure.


Stage A
+ Vdc/2
Cdc1
Cx1
Dx1
Dx2
Cx2
Cdc2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Outer Structure
Inner Structure
− Vdc/2

(a)


Stage B
+ Vdc/2
Cdc1
Cdc2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Outer Structure
Cdc1
Cdc2
Cx1
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Inner Structure
Cdc1
Cdc2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
− Vdc/2

(b)

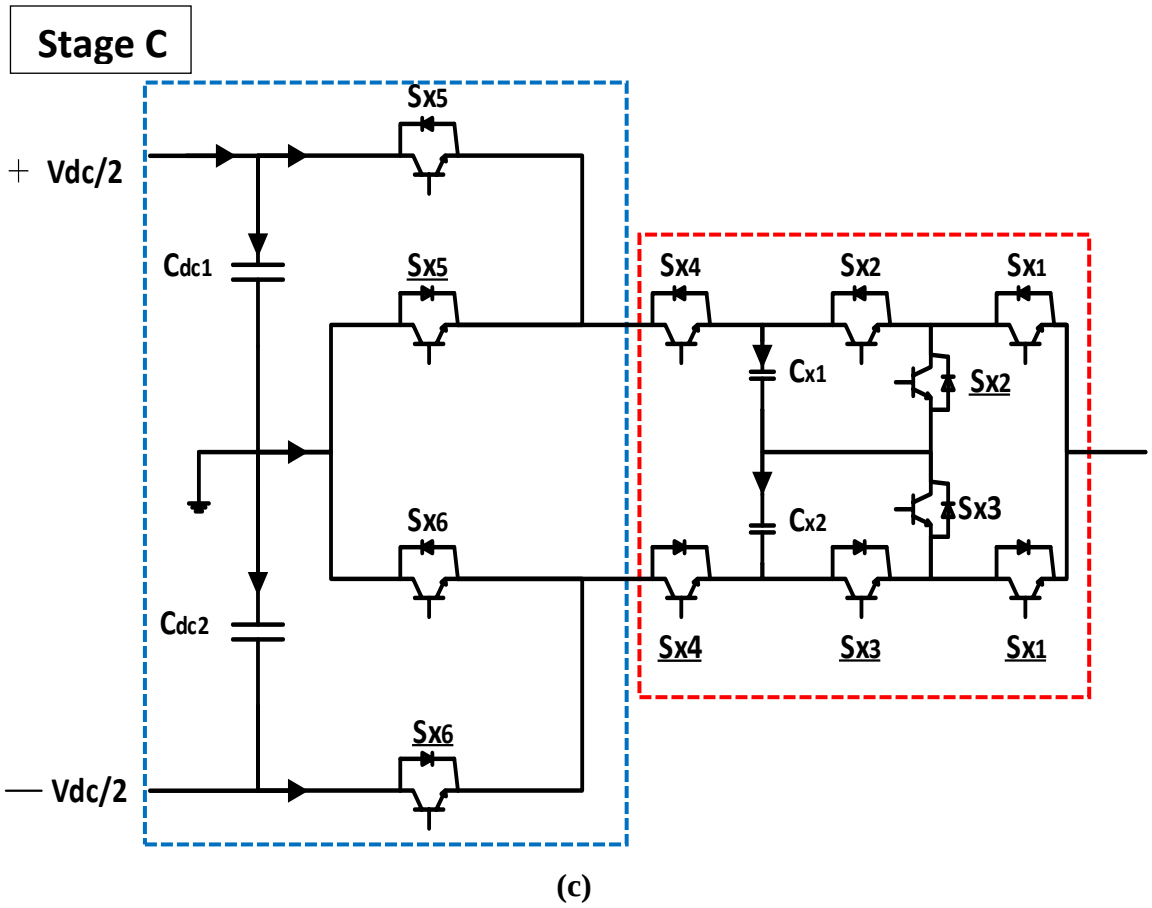


Figure 3.6: Derivation of a 1ph 7L-MNNPC converter topology. (a) stage A, (b) stage B, (c) stage C.

A. Operating Principle

The 7L-MNNPC converter topology consists of twelve power semiconductor devices and two clamping capacitors per phase. The two pairs of outer IGBT devices (S_{x5} – $\underline{S_{x5}}$, and S_{x6} – $\underline{S_{x6}}$) are three times the voltage rating of the inner IGBT devices, as illustrated in Figure 3.6(b). The clamping capacitors (C_{x1} and C_{x2}) are each estimated at one-sixth of the dc-link voltage ($V_{dc}/6$). The switching state combinations to achieve the output voltage waveform of a 7L-MNNPC converter topology are presented in Table 3.3. It consists of sixteen switching states, with redundant switching states available in the internal output voltage levels ($V_{dc}/3\,, V_{dc}/6\,, 0, -V_{dc}/3\,, -V_{dc}/6$). These redundant switching states are useful for minimizing the clamping capacitor's voltage deviation and developing a fault-tolerant scheme for the topology [134].

Table 3.3: Switching states of a 7L-MNNPC converter.

S_{x6}	S_{x5}	S_{x4}	S_{x3}	S_{x2}	S_{x1}	$\underline{S_{x6}}$	$\underline{S_{x5}}$	$\underline{S_{x4}}$	$\underline{S_{x3}}$	$\underline{S_{x2}}$	$\underline{S_{x1}}$	V_{cx1}	V_{cx2}	V_{xo}	Switching State
1	1	1	1	1	1	0	0	0	0	0	0	N	N	$V_{dc}/2$	1
1	1	1	1	1	0	0	0	0	0	0	1	C	N	$V_{dc}/3$	2
1	1	1	0	0	1	0	0	0	1	1	0	C	N	$V_{dc}/3$	2.1
1	1	0	1	1	0	0	0	1	0	0	1	N	D	$V_{dc}/3$	2.2
1	1	0	0	0	1	0	0	1	1	1	0	N	D	$V_{dc}/3$	2.3
1	1	1	0	0	0	0	0	0	1	1	1	C	C	$V_{dc}/6$	3
1	1	0	0	1	1	0	0	1	1	0	0	D	D	$V_{dc}/6$	3.1
1	1	0	0	0	0	0	0	1	1	1	1	N	N	0	4
0	0	1	1	1	1	1	1	0	0	0	0	N	N	0	4.1
0	0	1	1	0	0	1	1	0	0	1	1	C	C	$-V_{dc}/6$	5
0	0	0	1	1	1	1	1	1	0	0	0	D	D	$-V_{dc}/6$	5.1
0	0	1	0	0	1	1	1	0	1	1	0	C	N	$-V_{dc}/3$	6
0	0	1	1	1	0	1	1	0	0	0	1	C	N	$-V_{dc}/3$	6.1
0	0	0	1	1	0	1	1	1	0	0	1	N	D	$-V_{dc}/3$	6.2
0	0	0	0	0	1	1	1	1	1	1	0	N	D	$-V_{dc}/3$	6.3
0	0	0	0	0	0	1	1	1	1	1	1	N	N	$-V_{dc}/2$	7

N: No Impact; C: Charging; D: Discharging

B. Mathematical Model

The output phase voltage (V_{xo}), where x represents phase (a, b, or c) as expressed in (3.8).

$$V_{xo} = \left[(S_{x5} - 1)\frac{V_{dc}}{2} + S_{x4}(V_{cx1} + V_{cx2}) + (S_{x3} - 1)V_{cx2} + (S_{x2} - 1)V_{cx1} + S_{x1}V_{cx1}\right] \quad (3.8)$$

The current flowing through the clamping capacitors C_{x1} and C_{x2} is expressed by (3.9) and (3.10).

$$i_{Cx1} = (S_{x4} - S_{x2}) \cdot i_x \quad (3.9)$$

$$i_{Cx2} = \left(\underline{S_{x4}} - \underline{S_{x3}}\right) \cdot i_x \quad (3.10)$$

where S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, $\underline{S_{x4}}$ and $\underline{S_{x3}}$ are the switching power semiconductor devices; i_{Cx1} and i_{Cx2} is the current flowing through $C_{x1}$and C_{x2}; V_{cx1} and V_{cx2} are the voltages across the clamping capacitors (C_{x1} and C_{x2}); and i_x is the output phase current.

The equivalent circuit of a 3ph 7L-MNNPC converter topology is shown in Figure 3.7. In Figure 3.8, a 3ph 7L-MNNPC converter topology has the lowest number of power

semiconductor devices, clamping capacitors and clamping diodes compared to the seven-level flying capacitor (FC) converter, seven-level diode-clamped converter (DCC), and seven-level modular multilevel converter (MMC) topologies. Therefore, the 7L-MNNPC converter topology will have much better performance in cost, reliability, and efficiency.

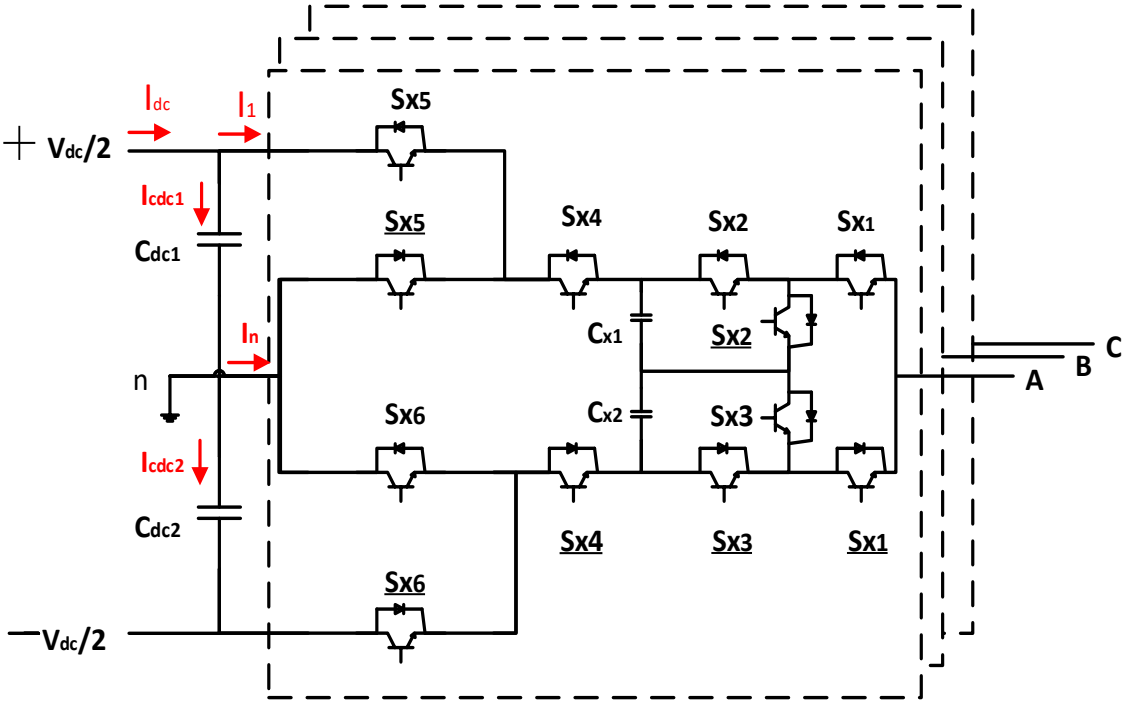


Figure 3.7: 3ph 7L-MNNPC converter topology.

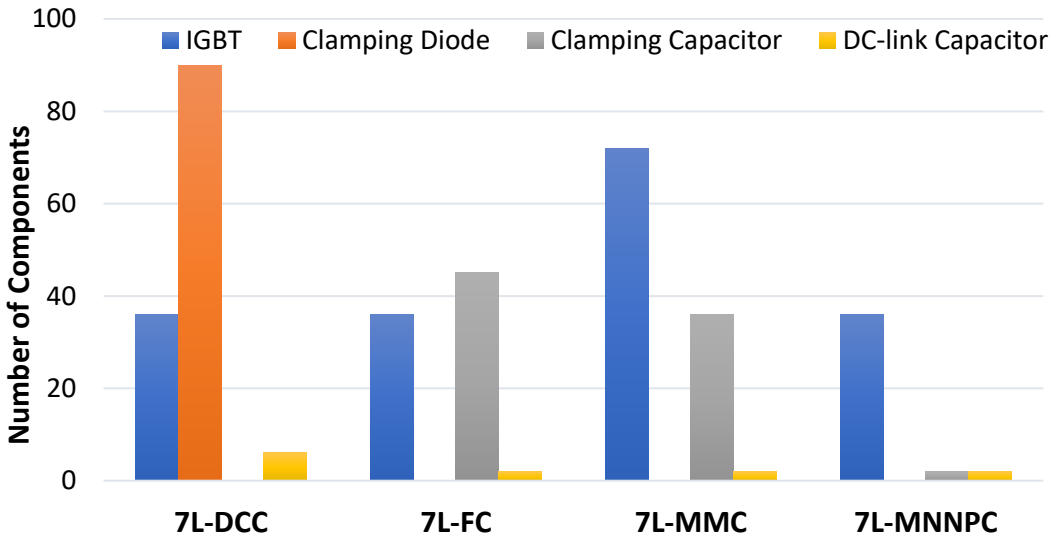


Figure 3.8: Component comparison of seven-level multilevel converter topologies.

3.2. Converter Design

This section presents the design specification and associated constraints of the converter topologies utilized as a grid-side converter in a transformer-less WECS. The average model of these converter topologies is analysed and discussed in this section.

3.2.1. Specification and Constraints

The first step of the NNPC converter design for transformer-less WECS is defining its specifications into two main categories: primary and secondary specifications [135].

A. Primary Specifications

These are the parameters determined by the voltage level (V_{LL}) of the collection point, the active power rating (P_R) of the transformer-less WECS, the maximum phase current (I_{ph}), and grid frequency (F_g) [47], [71]. The MV range of the collection point of a WPP based on the IEC 60038 standard is stated in Table 1.3, as stated previously [47]. A medium voltage, high-power WECS is suitable for a transformer-less WECS due to the minimized transmitted electric current [6], [86]. Therefore, the transformer-less configuration is an attractive concept for emerging WECSs [6], [86]. The parameters of Nordex N150/6000 DD-PMSG was considered for the power conversion stage presented in this section [6]. These specifications set the converter topology input and output ratings, as stated in Table 3.4, and the equations for deriving the stated values are provided in Appendix A.2.

Table 3.4: Primary specifications

Parameters	Collection Point- A	Collection Point- B	Collection Point- C	Collection Point- D
V_{LL}	6.6 kV	11 kV	22 kV	33 kV
P_R	6 MW	6 MW	6 MW	6 MW
S_A	6.7 MVA	6.7 MVA	6.7 MVA	6.7 MVA
$cos\,\theta$	0.9	0.9	0.9	0.9
I_{ph}	583.2 A	350 A	175 A	117 A
F_g	50 Hz	50 Hz	50 Hz	50 Hz

Table 3.5: Values of maximum dc-link voltage

Parameters	Collection Point- A	Collection Point- B	Collection Point- C	Collection Point- D
V_{LL}	6.6 kV	11 kV	22 kV	33 kV
V_{dc_max}	10 kV	16.5 kV	32.7 kV	49 kV

B. Secondary Specifications

These specifications set the design guidelines of the converter based on the primary specifications. These guidelines determine the internal parameters of the topology, such as maximum dc-link voltage, active and passive components ratings, switching frequency, and values of the passive components of the grid-side filter topology [40], [71], [135]-[139]. These parameters can be optimized and constrained to minimize cost and simultaneously increase efficiency.

The maximum dc-link voltage (V_{dc_max}) necessary to achieve the MV level of the collection point, with a sinusoidal pulse-width modulation (SPWM) technique and a third order grid-side filter is calculated using (3.11) [71], [136].

$$V_{dc\_max} = \sqrt{2} \cdot V_{LL} \cdot 1.05 \tag{3.11}$$

A voltage reserve of 5% is taking into consideration to account for the voltage drop across the inductive components in the high-order grid-side filter [71], [136]-[138]. In Table 3.5, the values of V_{dc_max} for the voltage level range of the collection point is highlighted. While the switching frequency of a grid-side converter topology depends on V_{LL}, P_R and type of power semiconductor device deployed in the topology [140], [141]. Due to the medium voltage level of the proposed transformer-less WECS, dv/dt of the power semiconductor device is often more than $10\,kV/\mu s$ [140], [141]. Therefore, operating the switching power semiconductor device at a high-frequency rate will increase the feeder cables' electromagnetic emission and switching losses [140]. Based on the highlighted factors, the operating switching frequency of the utilized switching power semiconductor device is restricted to less than $1kHz$ [140], [141].

3.2.2. Modelling and Control Strategy

This sub-section presents the averaged mathematical model of the 4L-NNPC, 5L-NNPC and 7L-MNNPC converter topologies, respectively. Also, the voltage balancing control strategy of the clamping capacitors in a 5L-NNPC converter topology is presented. Furthermore, the grid-side control strategy deployed is presented later in the sub-section.

A. Averaged Mathematical Model

The averaged NNPC and MNNPC converter models presented shows the relationship between the switching power semiconductor devices, the redundant switching states and its associated duty cycles [142], [143].

1) 4L-NNPC Converter Topology

Figure 3.3 shows the circuit diagram of a 3ph 4L-NNPC converter topology which consist of two clamping capacitors per phase, C_{x1} and C_{x2} (where x represents a, b, c of each converter phase leg) and a neutral-point. Each clamping capacitor voltage must be maintained at one-third of the dc-link voltage. The switch control functions s_{xy} (where y represents $1, \dots, 6$), which shows the position of each switching power semiconductor device in the converter topology. The switch control function states the operational switching state of the converter topology highlighted in Table 3.1.

Based on the mathematical model of a 1ph 4L-NNPC converter topology presented in equations (3.1) to (3.3), the average representation of the output phase voltage (3.1) and the current flowing through the clamping capacitors C_{x1} and C_{x2} $(i.e.\, i_{Cx1}$ and $i_{Cx2})$ {(3.2) to (3.3)} obtained over a switching period are expressed below as follows [142].

$$\hat{v}_{xo} = [d_{x1}\frac{V_{dc}}{2} + (1 - d_{x1})(\hat{v}_{cx1} + \hat{v}_{cx2}) + (d_{x2} - 1)\hat{v}_{cx1} + (d_{x3} - 1)\hat{v}_{cx2}] \tag{3.12}$$

$$\hat{\imath}_{Cx1} = (d_{x3} - d_{x2}) \cdot \hat{\imath}_x \tag{3.13}$$

$$\hat{\imath}_{Cx2} = (d_{x6} - d_{x5}) \cdot \hat{\imath}_x \tag{3.14}$$

where $\hat{v}_{cx1}$ and $\hat{v}_{cx2}$ are the averaged voltages of the clamping capacitors C_{x1} and C_{x2} , $\hat{\imath}_{Cx1}$ and $\hat{\imath}_{Cx2}$ are the averaged currents flowing through the clamping capacitors C_{x1} and C_{x2}, $\hat{\imath}_x$ is the averaged output current, and d_{x1}, d_{x2}, d_{x3}, d_{x5} and d_{x6} are the duty cycles of the respective switch control functions S_{x1}, S_{x2}, S_{x3}, S_{x5} and S_{x6}. Furthermore, the average voltage of the clamping capacitors can be expressed as follows:

$$\hat{v}_{cx1} = \frac{1}{C_{x1}} \int_0^t \hat{\imath}_{Cx1} dt + V_{cx1} \tag{3.15}$$

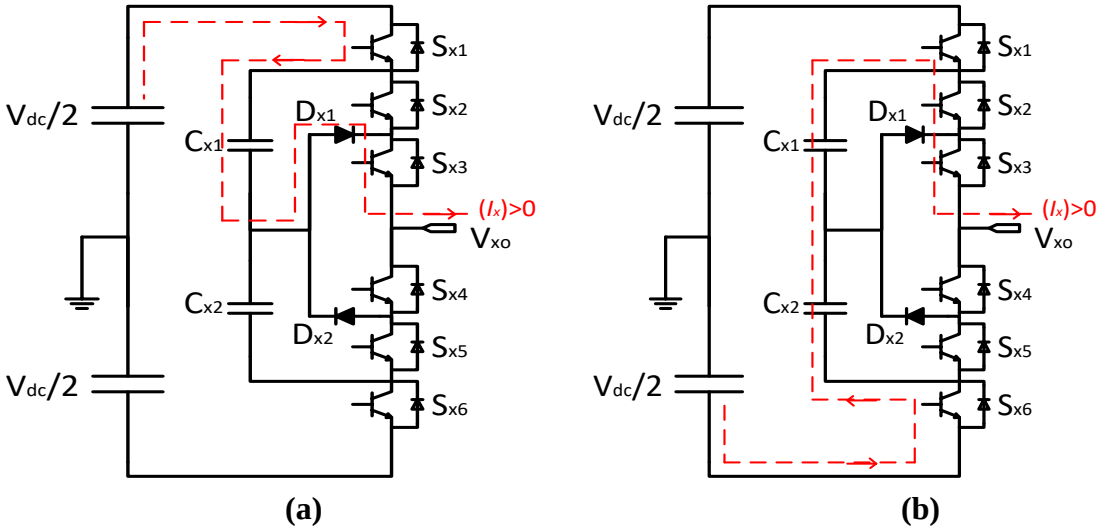
$$\hat{v}_{cx2} = \frac{1}{C_{x2}} \int_0^t \hat{\imath}_{Cx2} dt + V_{cx2} \tag{3.16}$$

where V_{cx1} and V_{cx2} are the initial voltage values of the clamping capacitors C_{x1} and C_{x2}.

In Table 3.6, the switching state control function of each switching state have been highlighted. The switching state control function l_m (where m represents $1, \ldots, 4$), which shows the actual switching state of a specific voltage level of the converter topology. Furthermore, some switching states have an extra state within a particular voltage level known as redundant switching state. Therefore, the redundant switch state control function $l_{m.n}$, where m represents the actual switching state (as previously stated) and n represents the redundant switching state of a specific voltage level of the converter topology (where $n = 1$). Figures 3.9(a) to 3.9(d) shows the switching states and redundant switching states of each voltage level that affect the clamping capacitor voltage.

Table 3.6: Highlighting Switching State Control Functions of a 4L-NNPC converter.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{xo}	Switching State	Switching State Control Function
1	1	1	0	0	0	$V_{dc}/2$	1	l_1
1	0	1	1	0	0	$V_{dc}/6$	2	l_2
0	1	1	0	0	1	$V_{dc}/6$	2.1	$l_{2.1}$
1	0	0	1	1	0	$-V_{dc}/6$	3	l_3
0	0	1	1	0	1	$-V_{dc}/6$	3.1	$l_{3.1}$
0	0	0	1	1	1	$-V_{dc}/2$	4	l_4



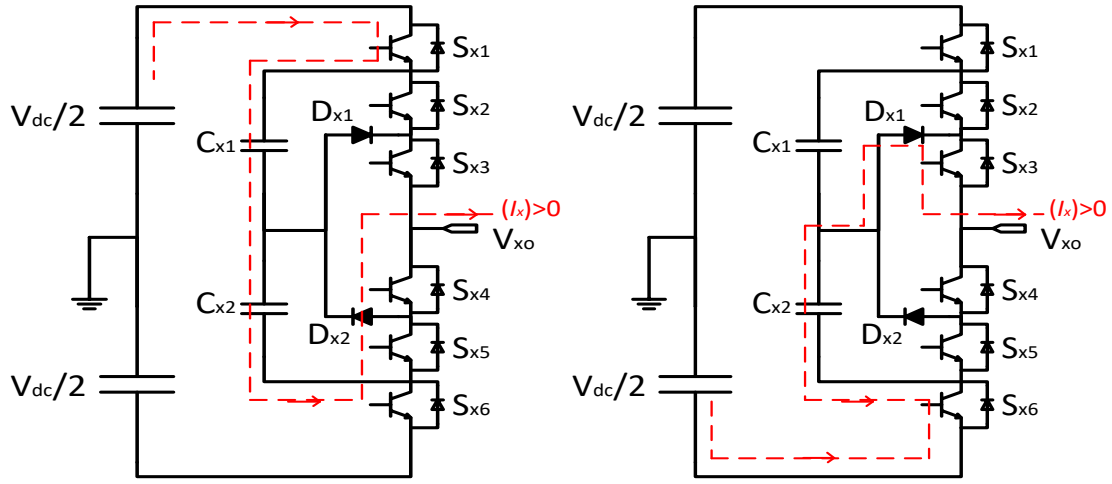


Figure 3.9: Impact of switching states and positive phase current on the clamping capacitor voltages in a 4L-NNPC converter. (a) state 2. (b) state 2.1. (c) state 3. (d) state 3.1.

Therefore, the average output voltage and clamping capacitors current in (3.12) to (3.14) can be expressed in terms of the duty cycle of the voltage level and the switch state control function, as stated below.

$$\hat{v}_{xo} = [\frac{V_{dc}}{2}(l_1 d_{xl1} + l_2 d_{xl2} + d_{xl3}) + (1 - l_1 d_{xl1})(\hat{v}_{cx1} + \hat{v}_{cx2}) + [(l_2 - l_{2.1})d_{xl2} - 1]\hat{v}_{cx1} + (d_{xl3} - 1)\hat{v}_{cx2}] \quad (3.17)$$

$$\hat{\imath}_{Cx1} = (l_1 d_{xl1} - (l_2 - l_{2.1})d_{xl2}) \cdot \hat{\imath}_x \quad (3.18)$$

$$\hat{\imath}_{Cx2} = \left((l_3 - l_{3.1})d_{xl3} + l_{2.1} d_{xl2}\right) \cdot \hat{\imath}_x \quad (3.19)$$

where l_1, l_2, and l_3 are the switching state control functions; while $l_{2.1}$ and $l_{3.1}$ are the redundant switching state control functions as stated in Table 3.6. The switching state is activated by the switching state control function being represented by the value '1', when deactivated by the value '0'. The duty cycles of the voltage levels 1 to 4 are represented by the variables d_{xl1}, d_{xl2}, d_{xl3} and d_{xl4}, respectively. Therefore, the redundant switching state to be selected for the voltage balancing control technique of the clamping capacitor voltage will be carried out by activating the redundant switching state control function. Also, the voltage balancing control technique of the clamping capacitor voltage can be achieved by adjusting the duty cycle of the voltage levels through the duty cycle of the switching power semiconductor devices. Therefore, the switch control functions in equations (3.1) to (3.3) are replaced by the product of the switching state control functions and associated duty cycle variables of the voltage level when

the clamping capacitor is charging as presented in equations (3.17) to (3.19), as extracted from Table 3.1 and Table 3.6.

2) 5L-NNPC Converter Topology

Figure 3.5 shows the circuit diagram of a 3ph 5L-NNPC converter topology which consist of three clamping capacitors per phase, C_{x1}, C_{x2}, and C_{x3} (where x represents a, b, c of each converter phase leg) and a neutral-point. The innermost clamping capacitor voltage must be maintained at a quarter of the dc-link voltage and the outermost clamping capacitor must be maintained at three-quarter of the dc-link voltage. The switch control functions s_{xy} (where y represents $1, \dots, 8$), which shows the position of each switching power semiconductor device in the converter topology. The switch control function states the operational switching state of the converter topology highlighted in Table 3.2.

Based on the mathematical model of a 1ph 5L-NNPC converter topology presented in equations (3.4) to (3.7), the average representation of the output phase voltage (3.4) and the current flowing through the clamping capacitors C_{x1}, C_{x2} and C_{x3} ($i.e. i_{Cx1}$, i_{Cx2} and i_{Cx3}){(3.5) to (3.7)} obtained over a switching period are expressed below as follows.

$$\hat{v}_{xo} = [d_{x1}\frac{V_{dc}}{2} + (d_{x1} + d_{x2})\hat{v}_{cx3} + d_{x2}(\hat{v}_{cx1} + \hat{v}_{cx2}) + (d_{x3} - 1)\hat{v}_{cx1} + (d_{x4} - 1)\hat{v}_{cx2}] \quad (3.20)$$

`

$$\hat{\imath}_{Cx3} = (d_{x1} - d_{x2}) \cdot \hat{\imath}_x \quad (3.21)$$

$$\hat{\imath}_{Cx1} = (d_{x2} - d_{x3}) \cdot \hat{\imath}_x \quad (3.22)$$

$$\hat{\imath}_{Cx2} = (d_{x7} - d_{x6}) \cdot \hat{\imath}_x \quad (3.23)$$

where $\hat{v}_{cx1}$, $\hat{v}_{cx2}$ and $\hat{v}_{cx3}$ are the average voltages of the clamping capacitors C_{x1}, C_{x2}, and C_{x3}, respectively. $\hat{\imath}_{Cx1}$, $\hat{\imath}_{Cx2}$ and $\hat{\imath}_{Cx3}$ are the average currents flowing through the clamping capacitors C_{x1}, C_{x2}, and C_{x3}. $\hat{\imath}_{xn}$ is the average output current, and d_{x1}, d_{x2}, d_{x3}, d_{x4}, d_{x6} and d_{x7} are the duty cycles of the switching functions S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x6} and S_{x7}. The average voltage of the clamping capacitors can be expressed as follows:

$$\hat{v}_{cx1} = \frac{1}{C_{x1}}\int_0^t \hat{\imath}_{Cx1}dt + V_{cx1} \quad (3.24)$$

$$\hat{v}_{cx2} = \frac{1}{C_{x2}}\int_0^t \hat{\imath}_{Cx2}dt + V_{cx2} \quad (3.25)$$

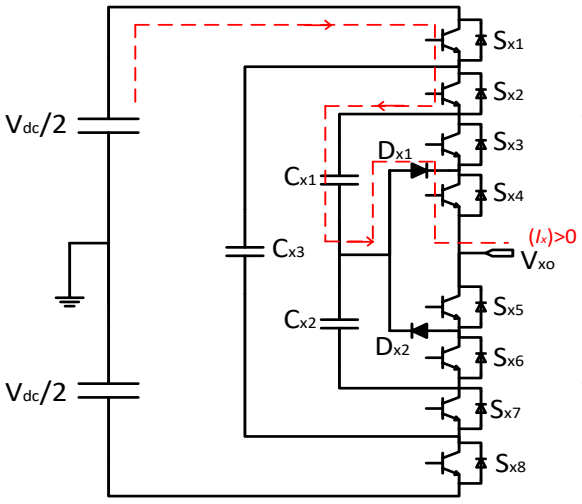
$$\hat{v}_{cx3} = \frac{1}{C_{x3}}\int_0^t \hat{\imath}_{Cx3}dt + V_{cx3} \quad (3.26)$$

where V_{cx1}, V_{cx2} and V_{cx3} are the initial voltage values of the clamping capacitors C_{x1}, C_{x2} and C_{x3}.

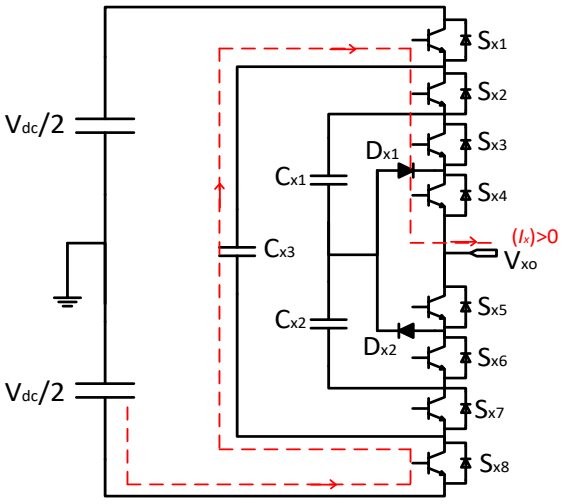
In Table 3.7, the switching state control function of each switching state have been highlighted. The switch state control function l_m (where m represents $1, \dots, 5$), which show the actual switching state of a specific voltage level of the converter topology. Furthermore, some switching states have an extra state within a particular voltage level known as redundant switching state. Therefore, the redundant switch state control function $l_{m.n}$, where m represents the actual switching state (as previously stated) and n represents the redundant switching state of a specific voltage level of the converter topology (where $n = 1, 2$). Figures 3.10(a) to 3.10(j) shows the switching states and redundant switching states of each voltage level that affect the clamping capacitor voltage.

Table 3.7: Highlighting Switching State Control Functions of a 5L-NNPC converter.

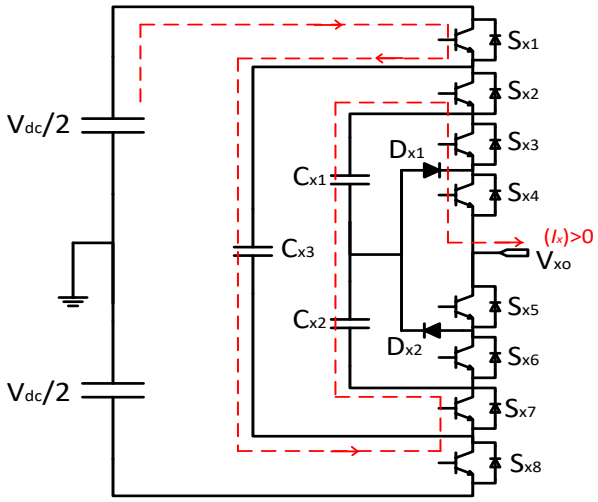
S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{xo}	Switching State	Switching State Control Function
1	1	1	1	0	0	0	0	$V_{dc}/2$	1	l_1
1	1	0	1	1	0	0	0	$V_{dc}/4$	2	l_2
0	1	1	1	0	0	0	1	$V_{dc}/4$	2.1	$l_{2.1}$
1	0	1	1	0	0	1	0	$V_{dc}/4$	2.2	$l_{2.2}$
1	1	0	0	1	1	0	0	0	3	l_3
1	0	0	1	1	0	1	0	0	3.1	$l_{3.1}$
0	1	0	1	1	0	0	1	0	3.2	$l_{3.2}$
0	0	1	1	0	0	1	1	0	3.3	$l_{3.3}$
0	0	0	1	1	0	1	1	$-V_{dc}/4$	4	l_4
1	0	0	0	1	1	1	0	$-V_{dc}/4$	4.1	$l_{4.1}$
0	1	0	0	1	1	0	1	$-V_{dc}/4$	4.2	$l_{4.2}$
0	0	0	0	1	1	1	1	$-V_{dc}/2$	5	l_5


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

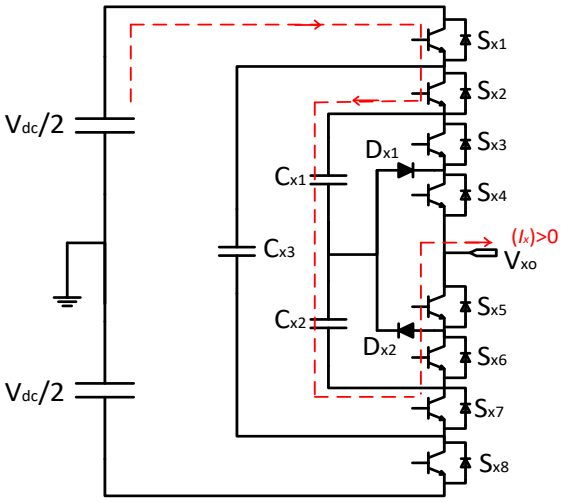
(a)


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

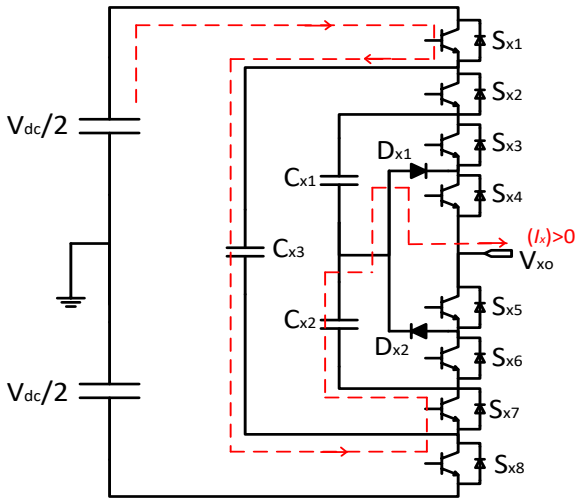
(b)


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

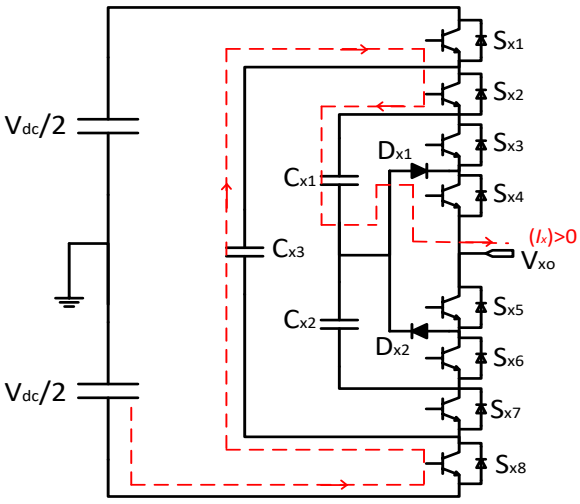
(c)


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

(d)


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

(e)


Vdc/2
Vdc/2
Cx1
Cx3
Cx2
Dx1
Dx2
Sx1
Sx2
Sx3
Sx4
Sx5
Sx6
Sx7
Sx8
(Ix)>0
Vxo

(f)

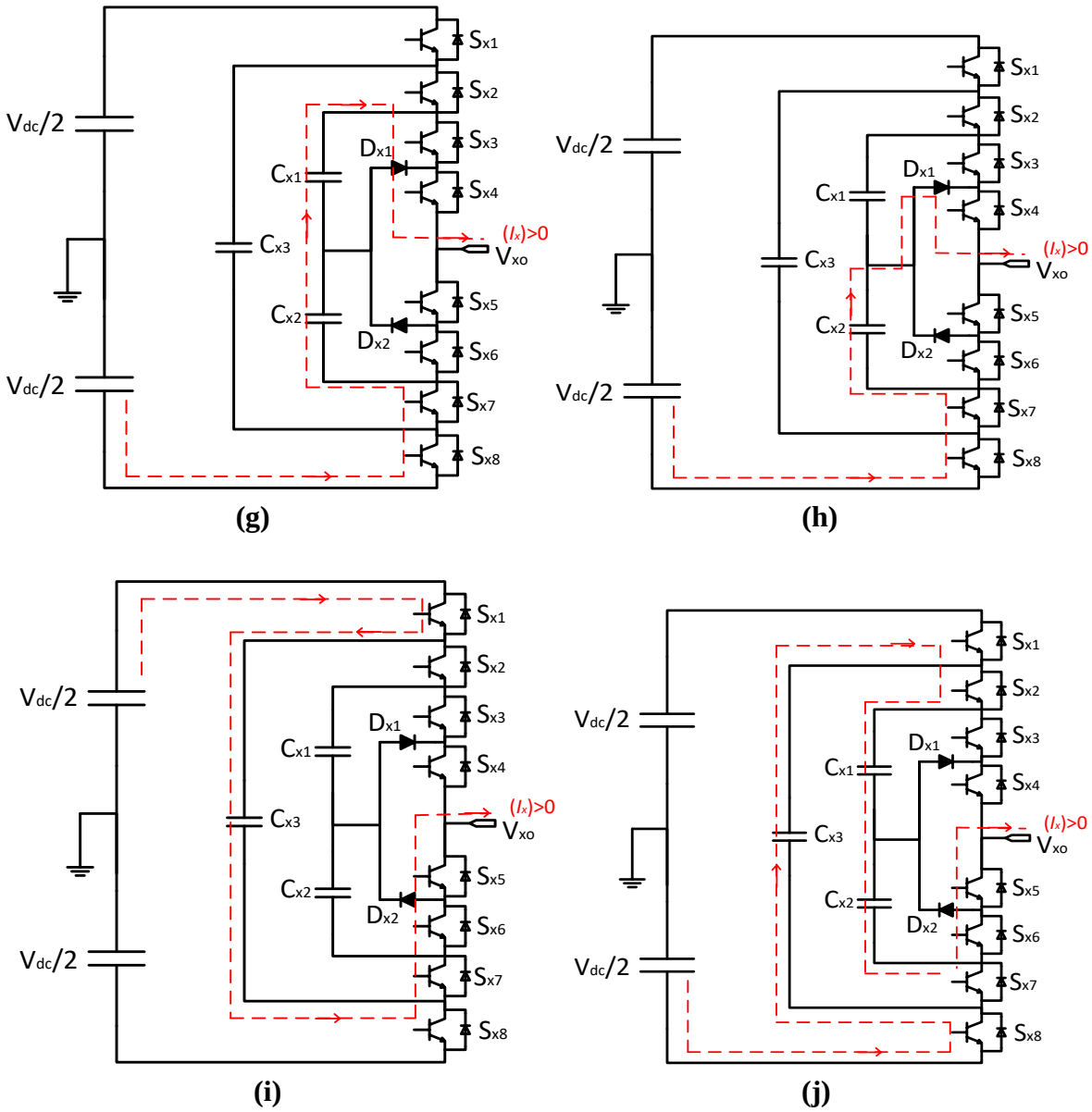


Figure 3.10: Impact of switching states and positive phase current on the clamping capacitor voltages. (a) state 2. (b) state 2.1. (c) state 2.2. (d) state 3. I state 3.1. (f) state 3.2. (g) state 3.3. (h) state 4. (i) state 4.1. (j) state 4.2.

Therefore, the average output voltage and clamping capacitors current in (3.20) to (3.23) can be expressed in terms of the duty cycle of each switching state as stated:

$$\hat{v}_{xo} = [\frac{V_{dc}}{2}(l_1 d_{xl1} + l_2 d_{xl2} + l_3 d_{xl3} + d_{xl4}) + (l_{2.2} d_{xl2} + l_{3.1} d_{xl3})\hat{v}_{cx3} + l_3 d_{xl3}(\hat{v}_{cx1} + \hat{v}_{cx2}) + (l_{4.2} d_{xl4} - 1)\hat{v}_{cx1} + (l_{4.2} d_{xl4} - 1)\hat{v}_{cx2}] \quad (3.27)$$

$$\hat{\imath}_{Cx3} = [(-l_{2.1} + l_{2.2})d_{xl2} + (l_{3.1} - l_{3.2})d_{xl3} + (l_{4.1} - l_{4.2})d_{xl4}] \cdot \hat{\imath}_{xn} \quad (3.28)$$

$$\hat{\imath}_{Cx1} = [(l_2 - l_{2.2})d_{xl2} + (l_3 - l_{3.3})d_{xl3} + l_{4.2} d_{xl4}] \cdot \hat{\imath}_{xn} \quad (3.29)$$

$$\hat{\imath}_{Cx2} = [-l_{2.2}d_{xl2} + (l_3 - l_{3.1})d_{xl3} + (-l_4 + l_{4.2})d_{xl4}] \cdot \hat{\imath}_x \quad (3.30)$$

where l_1, l_2, l_3, and l_4 are the switching state control functions; while $l_{2.1}$, $l_{2.2}$, $l_{3.1}$, $l_{3.2}$, $l_{3.3}$, $l_{4.1}$ and $l_{4.2}$ are the redundant switching state control functions as stated in Table 3.7. The switching state is activated by the switching state control function being represented by the value '1', when deactivated by the value '0'. The duty cycles of the voltage levels 1 to 5 are represented by the variables d_{xl1}, d_{xl2}, d_{xl3}, d_{xl4} and d_{xl5}, respectively. Therefore, the redundant switching state to be selected for the voltage balancing control technique of the clamping capacitor voltage will be carried out by activating the redundant switching state control function. Also, the voltage balancing control technique of the clamping capacitor voltage can be achieved by adjusting the duty cycle of the voltage levels through the duty cycle of the switching power semiconductor devices. Therefore, the switch control functions in equations (3.4) to (3.7) are replaced by the product of the switching state control functions and associated duty cycle variables of the voltage level when the clamping capacitor is charging as presented in equations (3.27) to (3.30), as extracted from Table 3.2 and Table 3.7.

3) 7L-MNNPC Converter Topology

Figure 3.7 shows the circuit diagram of a 3ph 7L-MNNPC converter topology which consist of two clamping capacitors per phase, C_{x1} and C_{x2} (where x represents a, b, c of each converter phase leg) and a neutral-point. The clamping capacitor voltage must be maintained at one-sixth of the dc-link voltage. The switch control functions s_{xy} (where y represents $1, \dots, 8$), which shows the position of each switching power semiconductor device in the converter topology. The switch control function states the operational switching state of the converter topology highlighted in Table 3.3.

Based on the mathematical model of a 1ph 7L-MNNPC converter topology presented in equations (3.8) to (3.10), the average representation of the output phase voltage (3.8) and the current flowing through the clamping capacitors C_{x1}, and C_{x2} ($i.e. i_{Cx1}$, and i_{Cx2}) {(3.9) to (3.10)} obtained over a switching period are expressed below.

$$\hat{v}_{xo} = \left[(d_{x5} - 1)\frac{V_{dc}}{2} + d_{x4}(\hat{v}_{cx1} + \hat{v}_{cx2}) + (d_{x3} - 1)\hat{v}_{cx2} + (d_{x2} - 1)\hat{v}_{cx1} + d_{x1}\hat{v}_{cx1}\right] \quad (3.31)$$

$$\hat{\imath}_{Cx1} = (d_{x4} - d_{x2}) \cdot \hat{\imath}_{xn} \quad (3.32)$$

$$\hat{\imath}_{Cx2} = \left(\underline{d_{x4}} - \underline{d_{x3}}\right) \cdot \hat{\imath}_{xn} \quad (3.33)$$

where $\hat{v}_{cx1}$ and $\hat{v}_{cx2}$ are the average voltages of the clamping capacitors C_{x1} and C_{x2}, respectively. $\hat{\imath}_{Cx1}$ and $\hat{\imath}_{Cx2}$ are the average currents flowing through the clamping capacitors C_{x1} and C_{x2}. $\hat{\imath}_{xn}$ is the average output current, and d_{x1}, d_{x2}, d_{x3}, d_{x4}, d_{x5}, $\underline{d_{x3}}$ and $\underline{d_{x2}}$ are the duty cycles of the switching functions S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, $\underline{S_{x3}}$ and $\underline{S_{x2}}$, respectively. The average voltage of the clamping capacitors can be expressed as:

$$\hat{v}_{cx1} = \frac{1}{C_{x1}} \int_0^t \hat{\imath}_{Cx1} dt + V_{cx1} \tag{3.34}$$

$$\hat{v}_{cx2} = \frac{1}{C_{x2}} \int_0^t \hat{\imath}_{Cx2} dt + V_{cx2} \tag{3.35}$$

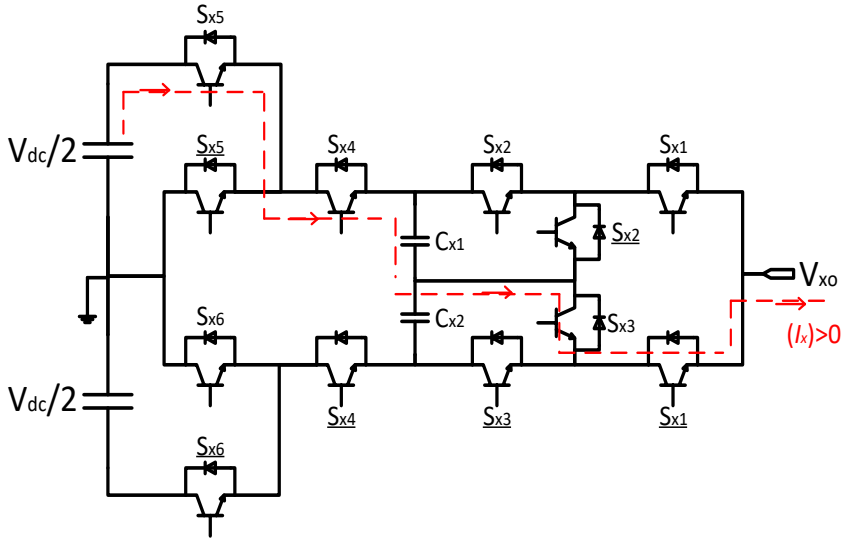
where V_{cx1} and V_{cx2} are the initial voltage values of the clamping capacitors C_{x1} and C_{x2}.

Table 3.8: Highlighting Switching State Control Functions of a 7L-MNNPC converter.

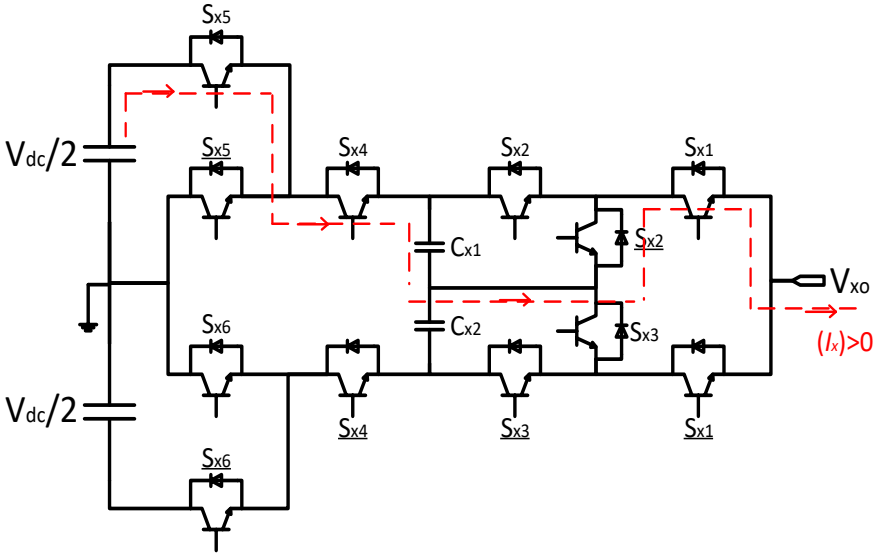
S_{x6}	S_{x5}	S_{x4}	S_{x3}	S_{x2}	S_{x1}	$\underline{S_{x6}}$	$\underline{S_{x5}}$	$\underline{S_{x4}}$	$\underline{S_{x3}}$	$\underline{S_{x2}}$	$\underline{S_{x1}}$	V_{xo}	Switching State	Switching State Control Function
1	1	1	1	1	1	0	0	0	0	0	0	$V_{dc}/2$	1	l_1
1	1	1	1	1	0	0	0	0	0	0	1	$V_{dc}/3$	2	l_2
1	1	1	0	0	1	0	0	0	1	1	0	$V_{dc}/3$	2.1	$l_{2.1}$
1	1	0	1	1	0	0	0	1	0	0	1	$V_{dc}/3$	2.2	$l_{2.2}$
1	1	0	0	0	1	0	0	1	1	1	0	$V_{dc}/3$	2.3	$l_{2.3}$
1	1	1	0	0	0	0	0	0	1	1	1	$V_{dc}/6$	3	l_3
1	1	0	0	1	1	0	0	1	1	0	0	$V_{dc}/6$	3.1	$l_{3.1}$
1	1	0	0	0	0	0	0	1	1	1	1	0	4	l_4
0	0	1	1	1	1	1	1	0	0	0	0	0	4.1	$l_{4.1}$
0	0	1	1	0	0	1	1	0	0	1	1	$-V_{dc}/6$	5	l_5
0	0	0	1	1	1	1	1	1	0	0	0	$-V_{dc}/6$	5.1	$l_{5.1}$
0	0	1	0	0	1	1	1	0	1	1	0	$-V_{dc}/3$	6	l_6
0	0	1	1	1	0	1	1	0	0	0	1	$-V_{dc}/3$	6.1	$l_{6.1}$
0	0	0	1	1	0	1	1	1	0	0	1	$-V_{dc}/3$	6.2	$l_{6.2}$
0	0	0	0	0	1	1	1	1	1	1	0	$-V_{dc}/3$	6.3	$l_{6.3}$
0	0	0	0	0	0	1	1	1	1	1	1	$-V_{dc}/2$	7	l_7

Table 3.8, the switching state control function of each switching state have been highlighted. The switch state control function l_m (where m represents $1, \ldots, 7$), which show the actual switching state of a specific voltage level of the converter topology. Furthermore, some switching states have an extra state within a particular voltage level known as redundant

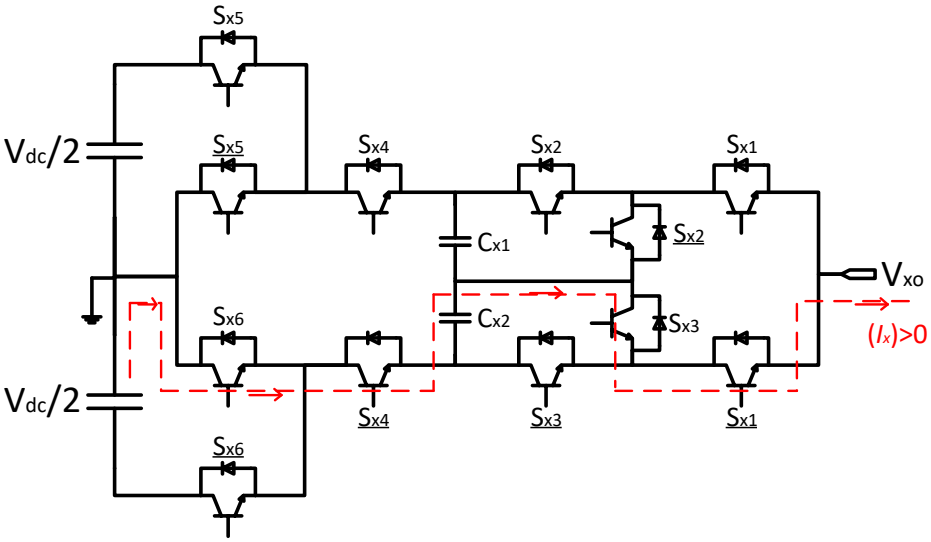
switching state. Therefore, the redundant switch state control function $l_{m.n}$, where m represents the actual switching state (as previously stated) and n represents the redundant switching state of a specific voltage level of the converter topology (where $n = 1, 2, 3$). Figures 3.11(a) to 3.11(l) shows the switching states and redundant switching states of each voltage level that affect the clamping capacitor voltage.



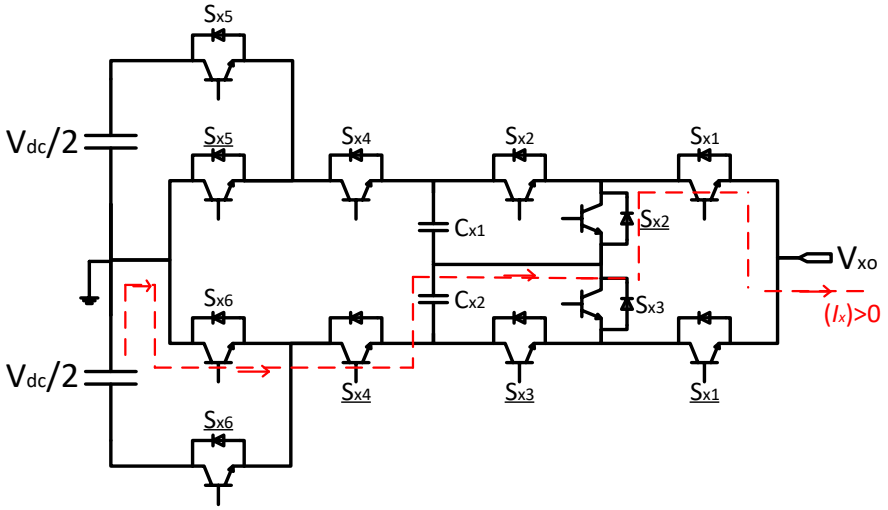
(a)



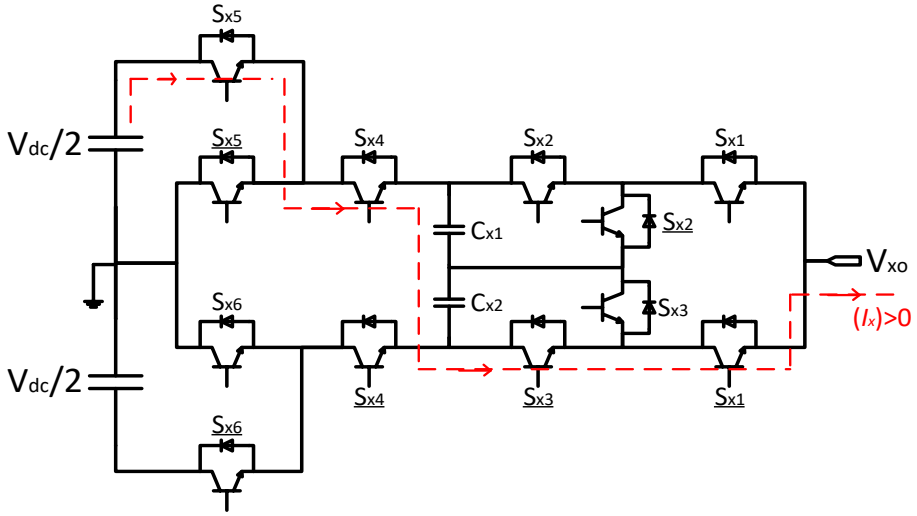
(b)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

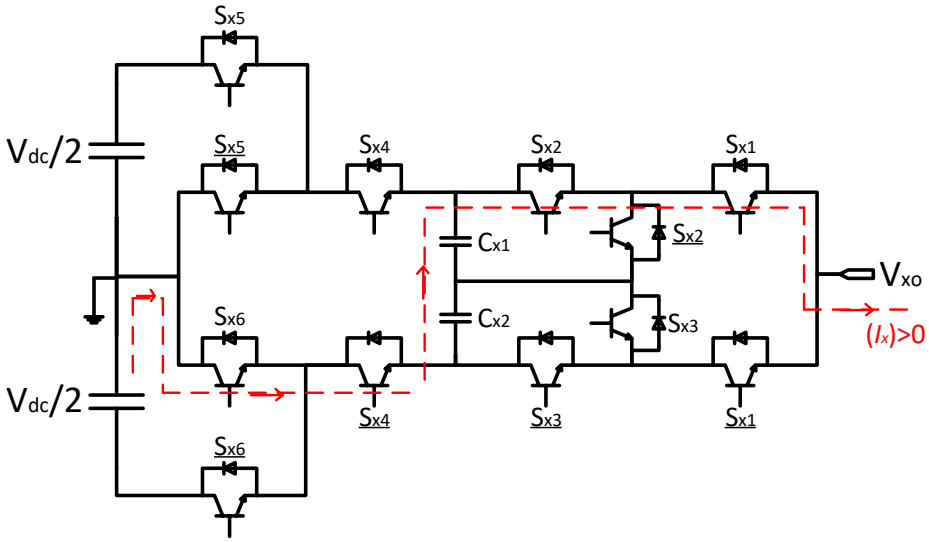
(c)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

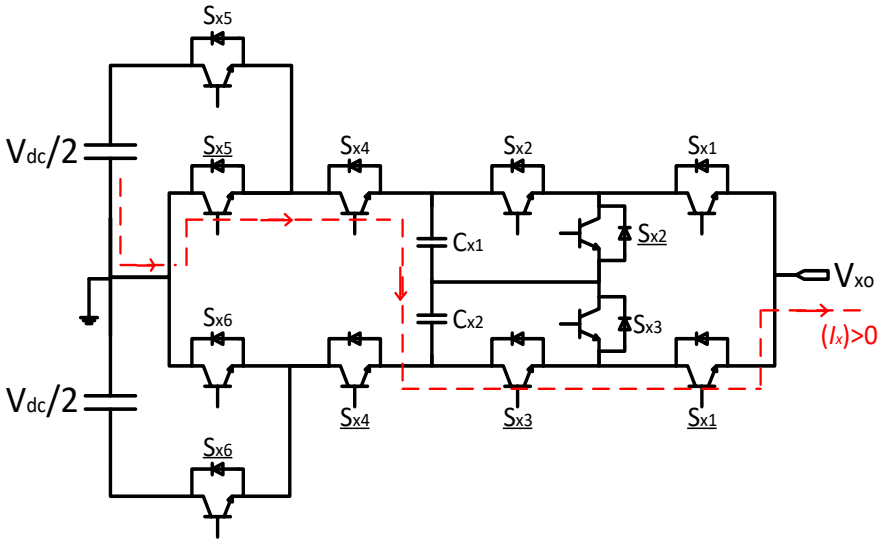
(d)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

(e)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

(f)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
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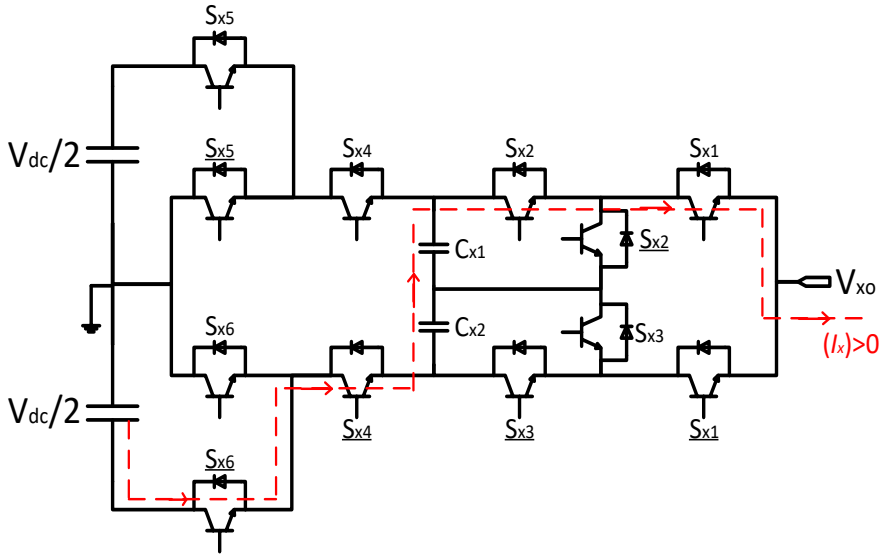
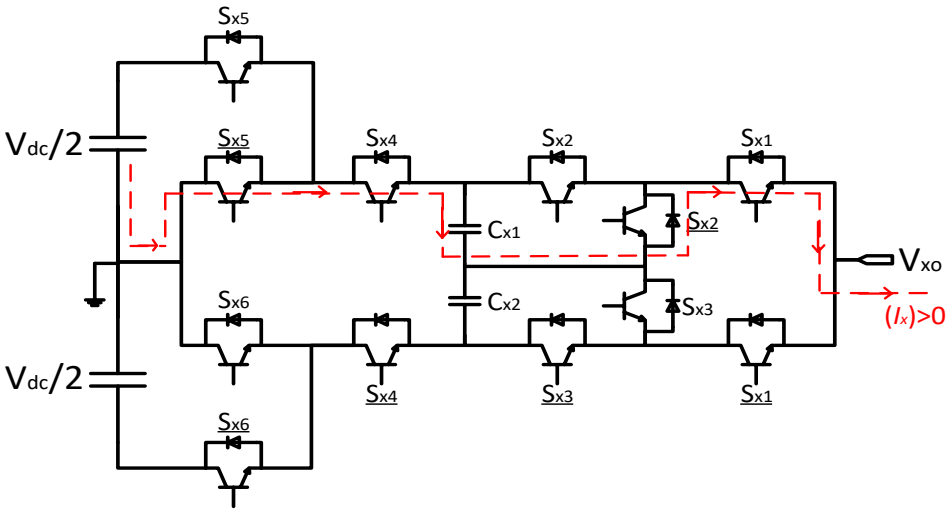
Vdc/2
Sx4
Sx3
Sx1
Sx6

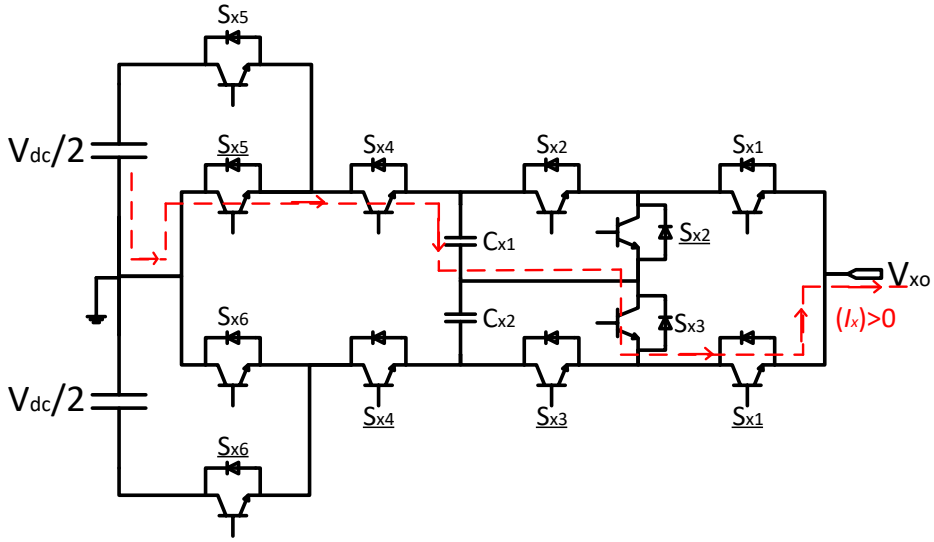
(g)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

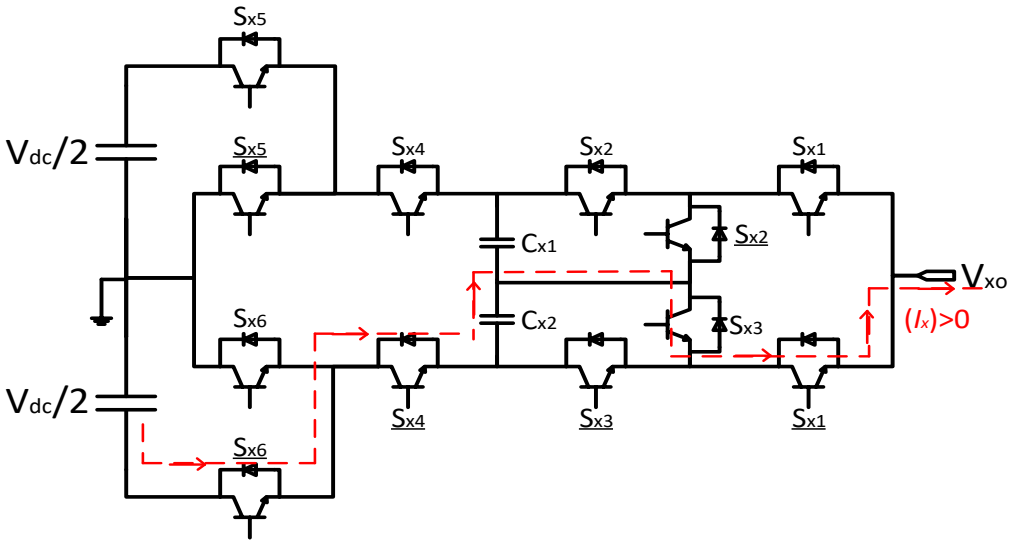
(h)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

(i)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

(j)


Sx5
Vdc/2
Sx5
Sx4
Sx2
Sx1
Cx1
Sx2
Vxo
Sx6
Cx2
Sx3
(Ix)>0
Vdc/2
Sx4
Sx3
Sx1
Sx6

(k)

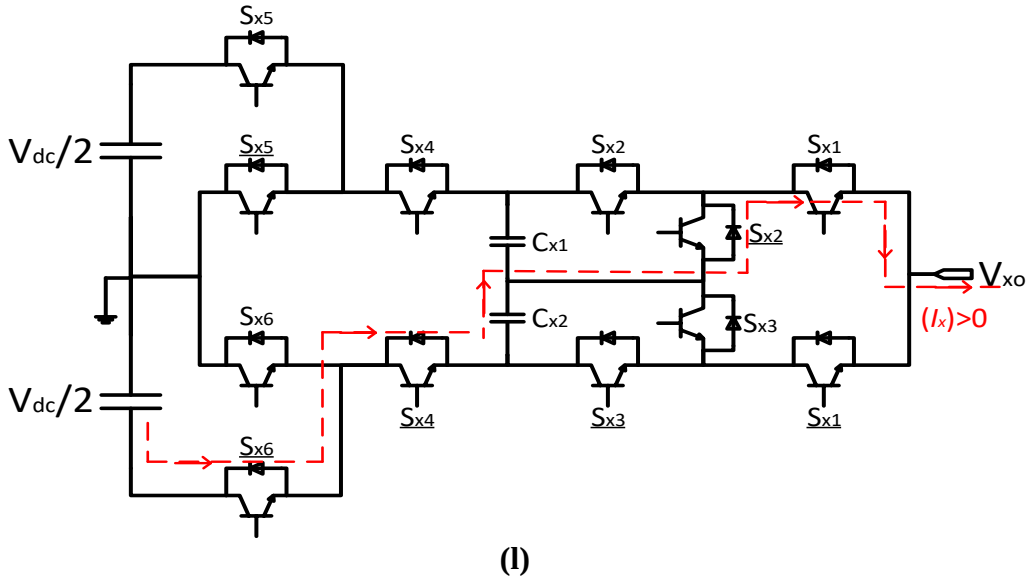


Figure 3.11: Impact of switching states and positive phase current on the clamping capacitor voltages in a 7L-MNNPC converter. (a) State 2. (b) State 2.1. (c) State 2.2. (d) State 2.3. (e) State 3. (f) State 3.1. (g) State 5. (h) State 5.1 (i) State 6. (j) State 6.1. (k) State 6.2. and (l) State 6.3.

Therefore, the average output voltage and clamping capacitors current in (3.31) to (3.33) can be expressed in terms of the duty cycle of each switching state, as stated below.

$$\hat{v}_{xo} = \left[\left((l_4 d_{xl4} + l_3 d_{xl3} + l_2 d_{xl2} + d_{xl1}) - 1\right)\frac{V_{dc}}{2} + \left(\left((l_{2.1} - l_2)d_{xl2}\right)\hat{v}_{cx1} + \left((l_{2.1} - l_{2.2})d_{xl2}\right)\hat{v}_{cx2}\right) + \left(\left((l_3 - l_{3.1})d_{xl3}\right) - 1\right)\hat{v}_{cx2} + \left(\left((l_5 - l_{5.1})d_{xl5}\right) - 1\right)\hat{v}_{cx1} + \left((l_{6.1} - l_{6.2})d_{xl6}\right)\hat{v}_{cx1}\right] \quad (3.36)$$

$$\hat{\imath}_{Cx1} = [l_{2.1} d_{xl2} + (l_3 - l_{3.1})d_{xl3} + (l_5 - l_{5.1})d_{xl5} + l_6 d_{xl6}] \cdot \hat{\imath}_{xn} \quad (3.37)$$

$$\hat{\imath}_{Cx2} = [l_{2.2} d_{xl2} + (l_3 - l_{3.1})d_{xl3} + (l_5 - l_{5.1})d_{xl5} + l_{6.2} d_{xl6}] \cdot \hat{\imath}_{xn} \quad (3.38)$$

where l_1, l_2, l_3, l_4, l_5, and l_6 are the switching state control functions; while $l_{2.1}$, $l_{2.2}$, $l_{2.3}$, $l_{3.1}$, $l_{4.1}$, $l_{5.1}$, $l_{6.1}$, $l_{6.2}$ and $l_{6.3}$ are the redundant switching state control functions as stated in Table 3.8. The switching state is activated by the switching state control function being represented by the value '1', when deactivated by the value '0'. The duty cycles of the voltage levels 1 to 7 are represented by the variables d_{xl1}, d_{xl2}, d_{xl3}, d_{xl4}, d_{xl5}, d_{xl6} and d_{xl7}, respectively. Therefore, the redundant switching state to be selected for the voltage balancing control technique of the clamping capacitor voltage will be carried out by activating the redundant switching state control function. Also, the voltage balancing control technique of the clamping capacitor voltage can be achieved by adjusting the duty cycle of the voltage levels through the

duty cycle of the switching power semiconductor devices. Therefore, the switch control functions in equations (3.8) to (3.10) are replaced by the product of the switching state control functions and associated duty cycle variables of the voltage level when the clamping capacitor is charging as presented in equations (3.36) to (3.38), as extracted from Table 3.3 and Table 3.8.

B. Voltage Balancing Control Strategy for Clamping Capacitor

This sub-section focuses on the voltage balancing control strategy of the clamping capacitor voltages of a 3ph 5L-NNPC converter topology. Each phase leg of the converter topology consists of three clamping capacitors rated at two different voltage levels (i.e., $V_{dc}/4$ and $3V_{dc}/4$). Therefore, the voltage balancing control of these clamping capacitor voltages is quite complex when compared to another conventional converter topology.

The switching power semiconductor devices of the 5L-NNPC converter topology can be controlled either through the phase-shifted pulse-width modulation (PS-PWM) technique or the phase disposition pulse-width modulation (PD-PWM) technique [129]-[131]. The PS-PWM technique is utilized to generate the output voltage, the common assumption is PS-PWM technique provides natural balancing to the clamping capacitor voltages of a multilevel converter topology under ideal conditions [129]-[131]. Although, the actual switching states of the switching sequence and the type of output load affects the voltage balancing of the clamping capacitor voltage [71], [129]. The PS-PWM technique for a single-phase five-level NNPC converter topology consists of four carrier signals (triangular waveforms) and a modulating signal (sinusoidal waveform) as shown in Figure 3.12. A 90° phase-shift exists between the carrier waveforms as obtained (3.39):

$$phase\ shift = \frac{2\pi}{N_{VL}-1} \tag{3.39}$$

where N_{VL} is the number of voltage levels in the converter topology.

Under the PS-PWM technique, the modulating signal that generates the reference voltage (v_{refx}) for the switching power semiconductor devices remains constant over a switching period. Hence, the duty cycles of the switching power semiconductor devices (S_{x1}, S_{x2}, S_{x3}, and S_{x4}) over a switching period can be expressed as follows:

$$d_{x1} = d_{x2} = d_{x3} = d_{x4} = v_{refx} \tag{3.40}$$

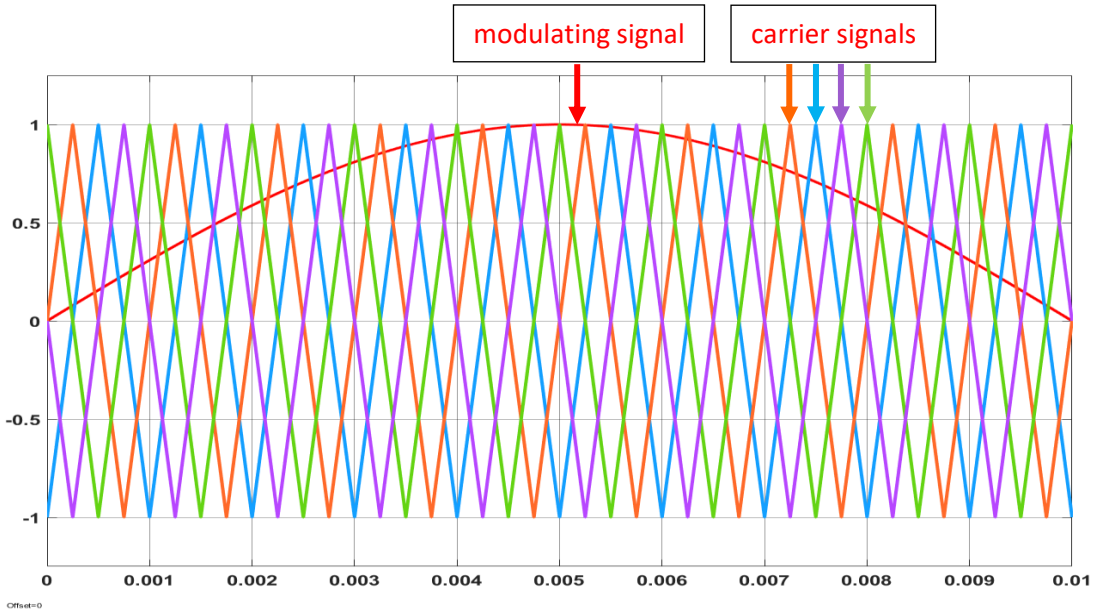


Figure 3.12: PS-PWM technique for a 5L-NNPC converter topology.

Based on the mathematical model of a 1ph 5L-NNPC converter topology presented in equations (3.4) to (3.7), the average representation of the output phase voltage and the current flowing through the clamping capacitors is presented in equations (3.20) to (3.23), the average clamping capacitor current over a switching period will be zero. Therefore, the clamping capacitor voltages of the converter topology would be naturally balanced under ideal conditions. Although, the clamping capacitor voltage deviates from its rated value under non-ideal conditions. Therefore, the average current flowing through the clamping capacitors can be controlled by slightly modifying its associated duty cycle of the switching power semiconductor devices as expressed in (3.21) to (3.23). In a nutshell, by modifying the PS-PWM technique, the change in the clamping capacitor voltage under non-ideal conditions can be minimized.

For example, the current flowing the clamping capacitor C_{x3} of the five-level NNPC converter topology (i_{cx3}) expressed in (3.5) is dependent on the switching power semiconductor devices S_{x1} and S_{x2}. Therefore, if the duty cycle of S_{x1} (d_{x1}) is increased by Δd_{xn}, to minimize the clamping capacitor voltage unbalance without affecting the output voltage, the duty cycle of S_{x2} (d_{x2}) is decreased by $\Delta d_{xn}/2$. Hence, the modified duty cycles of the switching power semiconductor devices are stated as follows:

$$d_{x1}{}^{*} = d_{x1} + \Delta d_{xn} = v_{refx} + \Delta d_{xn} \tag{3.41}$$

$$d_{x2}{}^{*} = d_{x2} - \Delta d_{xn}/2 = v_{refx} - \Delta d_{xn}/2 \tag{3.42}$$

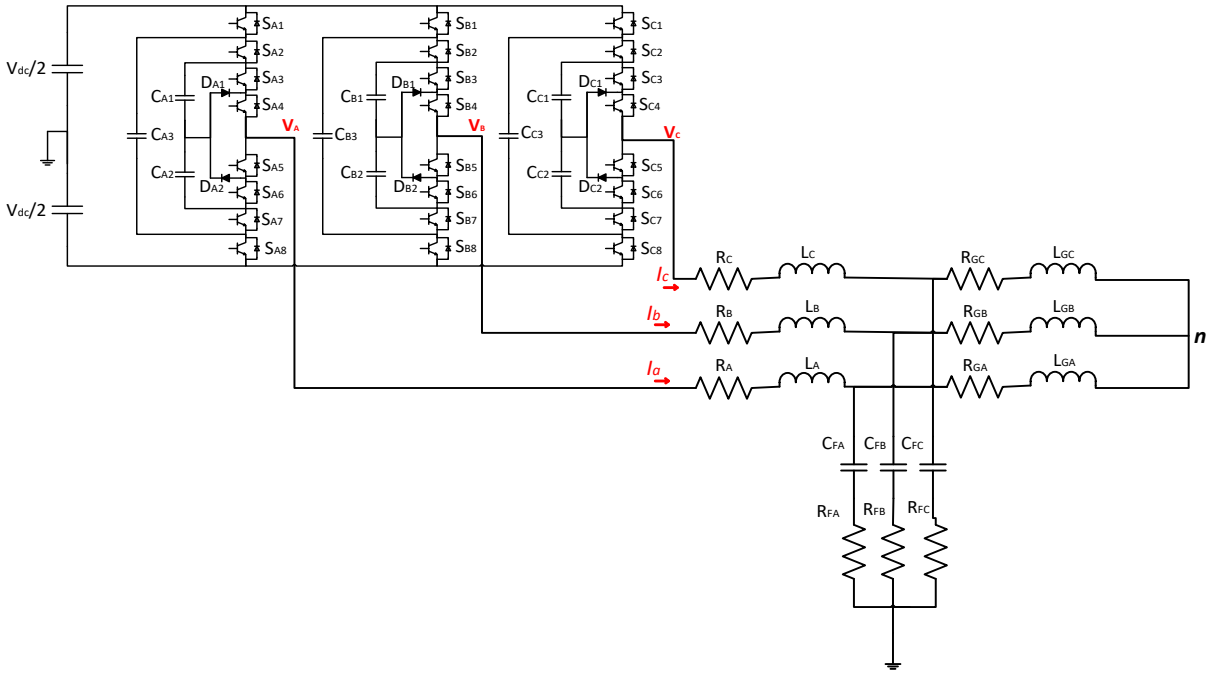
By substituting (3.41) and (3.42) into (3.21), the modified average clamping capacitor current ($\hat{\imath}_{Cx3}{}^{*}$) is stated below.

$$\hat{\imath}_{Cx3}{}^{*} = (d_{x1}{}^{*} - d_{x2}{}^{*}) \cdot \hat{\imath}_{x} = (3\Delta d_{xn}/2) \cdot \hat{\imath}_{x} \tag{3.43}$$

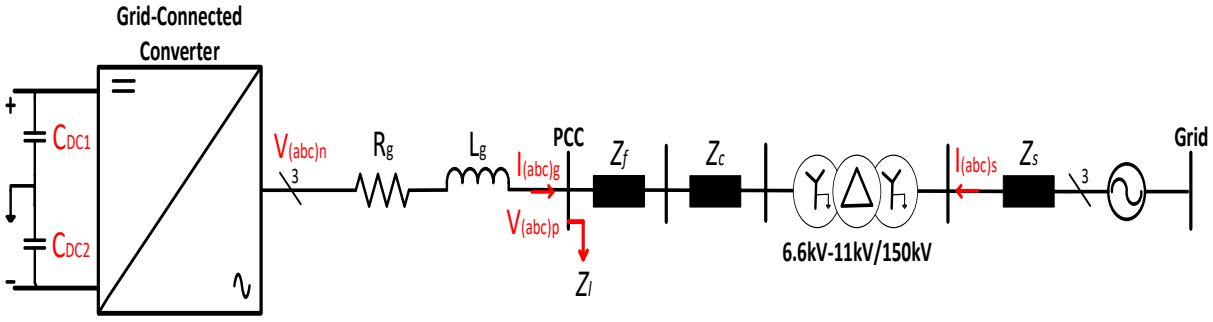
Therefore, the small change in Δd_{xn} can be controlled by using a linear controller, which is further explained in Chapter 4. The main advantage of this voltage balancing strategy is the reduced computational resources required to keep the clamping capacitor voltage within its rated value.

C. Grid-side Control Strategy

The configuration of a 3ph 5L-NNPC converter topology connected to the grid through a third order (LCL) filter is shown in Figure 3.13(a). While Figure 3.13(b) illustrates a simplified grid-connected converter in a transformer-less WECS configuration; where Z_f, Z_c , Z_l and Z_s denotes the feeder, collector, load, and source impedances, respectively. The phase voltages at the PCC are represented by v_{pa}, v_{pb}, and v_{pc}. The converter output phase voltages and currents are represented by v_{an}, v_{bn}, v_{cn} and i_{an}, i_{bn}, i_{cn} respectively. The resistance and inductance of the grid-side filter are denoted by R_g (where; $R_{GA} = R_{GB} = R_{GC} = R_A = R_B = R_C = R_g$) and L_g (where; $L_{GA} = L_{GB} = L_{GC} = L_A = L_B = L_C = L_g$) respectively.



(a)



(b)

Figure 3.13: Simplified schematic of the grid-connected converter. (a) 3ph 5L-NNPC converter with LCL filter. (b) grid-connected converter in a transformer-less WECS configuration.

In actuality, the grid-side filter is based on the LCL filter topology [136]-[139]; a simple L-filter topology is utilized to simplify the mathematical model presented. Therefore, the mathematical model that denotes the behaviour of voltages at the PCC is stated in (3.44) to (3.46).

$$v_{an} = R_g i_{an} + L_g \frac{d}{dt}(i_{an}) + v_{pa} \tag{3.44}$$

$$v_{bn} = R_g i_{bn} + L_g \frac{d}{dt}(i_{bn}) + v_{pb} \tag{3.45}$$

$$v_{cn} = R_g i_{cn} + L_g \frac{d}{dt}(i_{cn}) + v_{pc} \tag{3.46}$$

The variables presented in (3.44) to (3.46) are transformed into the synchronous reference frame (dq) as expressed below [32], [88]:

$$\begin{bmatrix} v_{nd} - v_{pd} \\ v_{nq} - v_{pq} \end{bmatrix} = \begin{bmatrix} R_g + L_g \frac{d}{dt} & -\omega L_g \\ \omega L_g & R_g + L_g \frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_{nd} \\ i_{nq} \end{bmatrix} \tag{3.47}$$

The active and reactive currents (i_{nd} and i_{nq}) are used to control the active and reactive power transferred to the grid. The voltage changes at the PCC because of the active and reactive power transferred between the converter and the grid and the load power is expressed in (3.48) [32].

$$\Delta V = \left| \frac{R_s(P_p - P_g) + X_s(Q_p - Q_g)}{V_p} - \frac{jX_s(P_p - P_g) - R_s(Q_p - Q_g)}{V_p} \right| \tag{3.48}$$

where P_g, Q_g are the active and reactive power transferred between the converter and the grid, and P_p, Q_p are the active and reactive power of the load, R_s and X_s represents the source

resistive and source reactive impedances, respectively. The relationship between the source voltage (V_s) and the PCC voltage is expressed in (3.49).

$$V_s^2 = \left[\frac{R_s(P_p - P_g) + X_s(Q_p - Q_g)}{V_p}\right]^2 + \left[\frac{jX_s(P_p - P_g) - R_s(Q_p - Q_g)}{V_p}\right]^2 \quad (3.49)$$

Therefore, the active and reactive powers transferred to the grid can be obtained as follows:

$$P_g = 3V_g I_g \cos \emptyset_g \quad (3.50)$$

$$Q_g = 3V_g I_g \sin \emptyset_g \quad (3.51)$$

where $\emptyset_g$ is the grid power factor angle. The angle between the grid voltage and current vectors is measured as $\emptyset_g$. Therefore, the grid power factor can be unity, lagging, or leading, as illustrated below [88]:

Unity power factor: $\emptyset_g = 0°$

Lagging power factor: $\emptyset_g = 0 - 90°$

Leading power factor: $\emptyset_g = 0 + 90°$

The grid-side control strategy is based on the conventional cascaded control loops which consists of the inner loops and outer loops [32], [88]. The inner loops control the currents injected to the grid using current controller and the outer loops regulate the dc-link voltage and the reactive power delivered to the grid [32]. The dynamics of the dc-link capacitor power balance is stated as follows:

$$P_{dc}(t) - P_g(t) = C_{dc,total} V_{dc} \left(\frac{dV_{dc}(t)}{dt}\right) \quad (3.52)$$

where $P_{dc}(t)$ is the total active power generated from WECS, $P_g(t)$ is the is the total power injected into the grid, and $C_{dc,total}$ (i.e., $C_{dc,total} = \frac{C_{dc} \cdot C_{dc}}{C_{dc} + C_{dc}} = \frac{C_{dc}}{2}$) is the total dc-link capacitance of the converter topology.

The active power reference ($P_g{}^*$) is obtained from the maximum power point tracking (MPPT) as discussed in [32]. In addition, the reactive power reference ($Q_g{}^*$) is set to be 0 for unity power factor. The generator-side converter is assumed to keep the dc-link voltage constant, and the neutral-point voltage balanced. Furthermore, the clamping capacitor voltage level, the

direction of converter output current, and the reference voltage are used in the modified PS-PWM technique for the clamping capacitor voltage control as discussed previously.

D. Reactive Power Capability

The reactive power capability of the 5L-NNPC converter topology is illustrated considering the non-unity power factor operation of the topology when the polarity of the output voltage is opposite its phase current. Therefore, the converter topology is operating within the negative power region. Based on the stated operating condition, the switching states of the converter topology is illustrated in Figure 3.14. Due to the impact of the clamping diodes, the converter topology operates as a three-level converter topology because only four switching power semiconductor devices are functional, as shown in Figure 3.14.

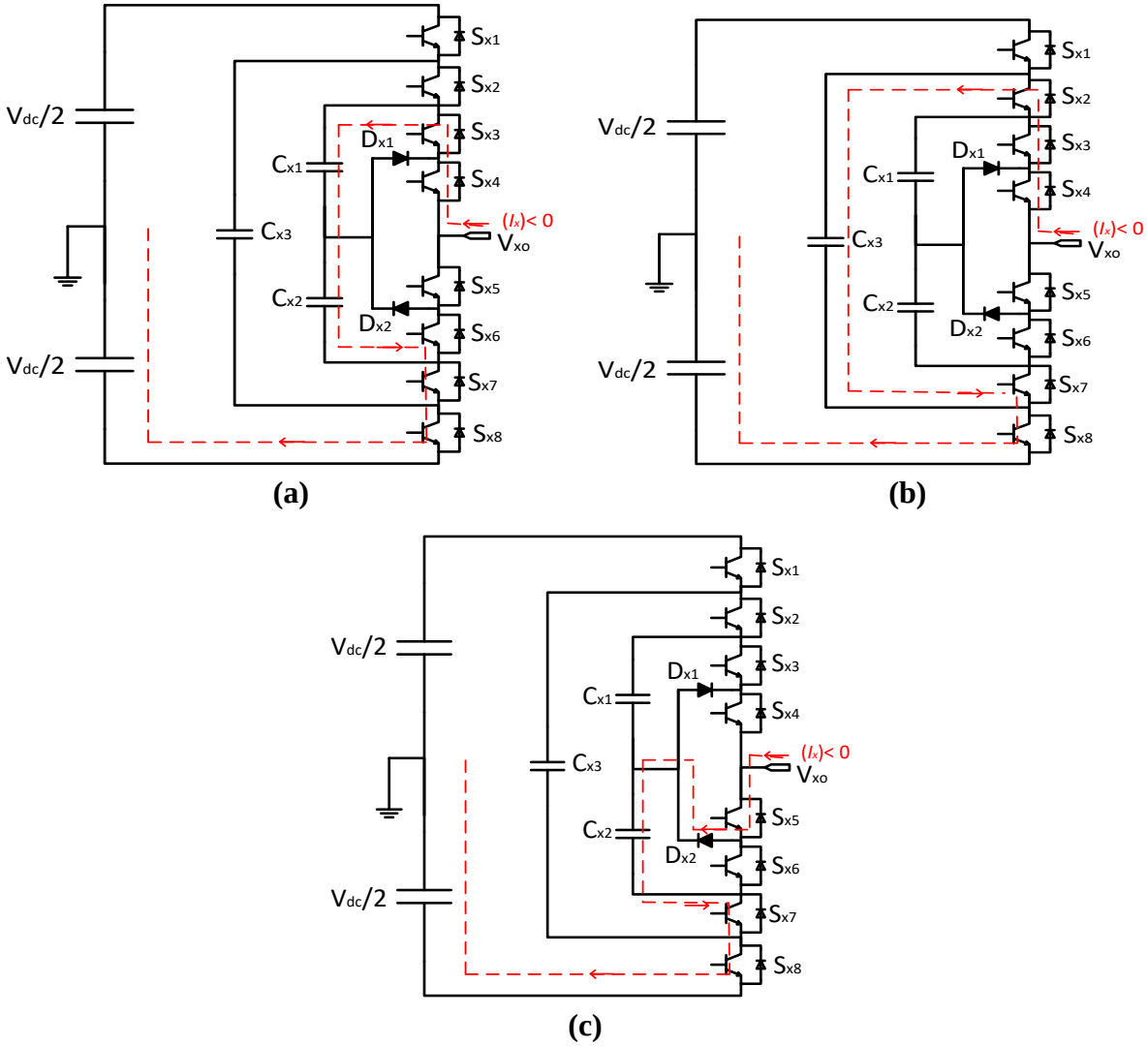


Figure 3.14: Switching states of the 5L-NNPC converter topology in non-unity power factor operation. (a) State I. (b) State II. (c) State III.

3.2.3. Component Rating Analysis

This section provides the equations and methods deployed to obtain the power semiconductor devices and clamping capacitors ratings.

A. Power Semiconductor Device Ratings

The NNPC and MNNPC converter topologies shown in Figures 3.3, 3.5, and 3.7 consists of IGBT modules, clamping diodes, and clamping capacitors. Therefore, the voltage rating of the IGBT module used in the converter topologies is based on the following criterion [71], [135], [136], [145]-[147].

- Maximum dc-link voltage (V_{dc_max})
- Minimum commutation voltage ($V_{Min.-Com}$).
- Maximum dc voltage due to cosmic radiation ($V_{dc\_voltage}$).
- Maximum voltage rating (V_{IGBT}).

The $V_{Min.-Com}$ represents the voltage across each IGBT module of the topology, which is dependent on V_{dc_max} and the number of voltage levels in the converter topology (N_{VL}) [71], [135]. Therefore, the value of $V_{Min.-Com}$ can be obtained by using (3.53).

$$V_{Min.-Com} = \frac{V_{dc\_max}}{N_{VL}-1} \tag{3.53}$$

Also, $V_{dc\_voltage}$ is the voltage rating of the IGBT module that can withstand cosmic radiation without failing for 1×10^9 operational hours [71], [135]. Therefore, the value of $V_{dc\_voltage}$ is obtained from the IGBT module datasheet [71], [135]. Furthermore, the calculated voltage rating ($V_{CAL-IGBT}$) of the IGBT module is obtained using (3.54) [71], [135], [136], [145]-[147].

$$V_{CAL-IGBT} = V_{Min.-Com} \times \left(1 + \frac{Safety\ Margin}{100}\right) \tag{3.54}$$

where the safety margin for medium voltage, the high-power application is given as 60% [146]. The value of V_{IGBT} is selected based on the next highest collector-emitter voltage rating [145]-[147]. In Table 3.9, the values of V_{dc_max}, $V_{Min.-Com}$, $V_{CAL-IGBT}$, $V_{dc\_voltage}$ and V_{IGBT} are stated for the respective medium voltage levels of the collection point.

The values of I_{ph} presented in Table 3.4, are the RMS values of the output current of the converter topologies at each of the specified medium voltage level. The current rating (I_{IGBT})

of the IGBT module is based on the peak output current (I_p) and a safety margin of about 35% for overcurrent transient [97], [148]. The values of I_p and the calculated current rating ($I_{CAL-IGBT}$) of the IGBT modules are obtained using (3.55) and (3.56), respectively.

$$I_p = \sqrt{2} \cdot I_{ph} \tag{3.55}$$

$$I_{CAL-IGBT} = 1.35 \cdot I_p \tag{3.56}$$

Therefore, the value of I_{IGBT} is selected based on the next highest rated collector current module [149], as shown in Table 3.10. The values of V_{IGBT} and I_{IGBT} are used to determine the voltage rating (V_{Diode}) and current rating (I_{Diode}) of the clamping diode module [135]. Therefore, V_{Diode} and I_{Diode} for each medium voltage level of the collection point is highlighted in Table 3.11.

Table 3.9: Specification of the voltage rating of IGBT modules

V_{LL}	V_{dc_max}	N_{VL}	$V_{Min.-Com}$	$V_{CAL-IGBT}$	$V_{dc\_voltage}$	V_{IGBT}
6.6 kV	10 kV	5-Level	2.5 kV	4 kV	2.8 kV	4.5 kV
11 kV	16.5 kV	7-Level	2.75 kV	4.4 kV	2.8 kV	4.5 kV
22 kV	32.7 kV	13-Level	2.73 kV	4.4 kV	2.8 kV	4.5 kV
33 kV	49 kV	15-Level	3.3 kV	5.3 kV	3.6 kV	6.5 kV

Table 3.10: Specification of the current rating of IGBT modules

V_{LL}	I_{ph}	I_p	$I_{CAL.-IGBT}$	I_{IGBT}
6.6 kV	583.2 A	825 A	1114 A	1.2 kA
11 kV	350 A	495 A	668 A	800 A
22 kV	175 A	248 A	335 A	400 A
33 kV	117 A	165 A	223 A	400 A

Table 3.11: Specification of the voltage and current ratings of clamping diode modules

V_{LL}	V_{Diode}	I_{Diode}
6.6 kV	4.5 kV	1.2 kA
11 kV	4.5 kV	800 A
22 kV	4.5 kV	400 A
33 kV	6.5 kV	400 A

B. Selection of Power Semiconductor Devices

The suitable IGBT modules for the converter topology are selected from the three leading manufacturers of $4.5kV/1.2kA$, $4.5kV/800A$, $4.5kV/400A$, and $6.5\,kV/400A$ modules, namely, ABB, Infineon Technologies, and Dynex Semiconductors [40], [71], [135]. In Table 3.12, the existing IGBT module reference number under the voltage and current rating class highlighted in Tables 3.9 and 3.10 as presented [150]-[160]. The conduction losses, switching losses, and thermal resistances attributed to the IGBT modules are calculated based on their electrical characteristics as obtained from their respective datasheets, and their equations can be found in Appendix A.3 [148], [150]-[160]. In Tables 3.13 to 3.15, the calculated conduction losses, switching losses, and estimated power losses of the presented IGBT modules are stated.

Table 3.12: IGBT modules reference number and manufacturer names

V_{LL}	ABB	INFINEON	DYNEX
$6.6\,kV$	5SNA1200G450300	FZ1200R45HL3	DIM1200ASM45 − TS001
$11\,kV$	5SNA0800J450300	FZ800R45KL3_B5	DIM800XSM45 − TS001
$22\,kV$	5SNA0650J450300	FZ800R45KL3_B5	DIM400XSM45 − TS001
$33\,kV$	5SNA0400J650100	FZ400R65KE3	DIM500XSM65 − TS

Table 3.13: Calculated conduction losses of the IGBT modules

Company	IGBT Module Ref. No.	V_{LL}	$P_{C(IGBT)}$	$P_{C(diode)}$	$P_{C(module)}$
ABB	5SNA1200G450300	$6.6\,kV$	$654\,W$	$223.6\,W$	$877.6\,W$
Infineon	FZ1200R45HL3	$6.6\,kV$	$602.33\,W$	$193.56\,W$	$795.9\,W$
Dynex	DIM1200ASM45 − TS001	$6.6\,kV$	$562\,W$	$151.06\,W$	$713\,W$
ABB	5SNA0800J450300	$11\,kV$	$428.4\,W$	$117.02\,W$	$545.4\,W$
Infineon	FZ800R45KL3_B5	$11\,kV$	$403.8\,W$	$117.47\,W$	$521.3\,W$
Dynex	DIM800XSM45 − TS001	$11\,kV$	$471.23\,W$	$98.06\,W$	$569.3\,W$
ABB	5SNA0650J450300	$22kV$	$161.68\,W$	$59.48\,W$	$221.2\,W$
Infineon	FZ800R45KL3_B5	$22kV$	$140.85\,W$	$54.25\,W$	$195.1\,W$
Dynex	DIM400XSM45 − TS001	$22kV$	$290.91\,W$	$51.06\,W$	$341.97\,W$
ABB	5SNA0400J650100	$33\,kV$	$186.86\,W$	$47.45\,W$	$234.3\,W$
Infineon	FZ400R65KE3	$33\,kV$	$107.68\,W$	$53.3\,W$	$161\,W$
Dynex	DIM500XSM65 − TS	$33\,kV$	$115.83\,W$	$41.68\,W$	$157.5\,W$

Table 3.14: Calculated switching losses of the IGBT modules

Company	IGBT Module Ref. No.	V_{LL}	E_{on}	E_{off}	E_{total}	E_{rec}
ABB	5SNA1200G450300	6.6 kV	4350mJ	6000mJ	7623mJ	1675.7mJ
Infineon	FZ1200R45HL3	6.6 kV	5300mJ	5300mJ	7808mJ	1964.2mJ
Dynex	DIM1200ASM45 − TS001	6.6 kV	6450mJ	4650mJ	8176mJ	2301.8mJ
ABB	5SNA0800J450300	11 kV	2580mJ	3780mJ	4554mJ	1121.8mJ
Infineon	FZ800R45KL3_B5	11 kV	4100mJ	3400 mJ	5352.3mJ	1432.1mJ
Dynex	DIM800XSM45 − TS001	11 kV	4300mJ	3100 mJ	5298.7mJ	1491.8mJ
ABB	5SNA0650J450300	22kV	2100mJ	2900mJ	2718mJ	729.3mJ
Infineon	FZ800R45KL3_B5	22kV	4100mJ	3400 mJ	4077mJ	1087.2mJ
Dynex	DIM400XSM45 − TS001	22kV	2200mJ	1600mJ	2066mJ	566.3mJ
ABB	5SNA0400J650100	33 kV	2800mJ	2120mJ	2232.5mJ	521.8mJ
Infineon	FZ400R65KE3	33 kV	3450mJ	2250mJ	2586.2mJ	604.96mJ
Dynex	DIM500XSM65 − TS	33 kV	3000mJ	4700mJ	2795.1mJ	877.3mJ

Table 3.15: Estimated power losses of the IGBT modules

Company	IGBT Module Ref. No.	V_{LL}	$P_{C(module)}$	$P_{sw(igbt)}$	$P_{sw(rec)}$	P_{tot}
ABB	5SNA1200G450300	6.6 kV	877.6 W	1213 W	266.7 W	2357.3 W
Infineon	FZ1200R45HL3	6.6 kV	795.9 W	1243 W	312.6 W	2351.5 W
Dynex	DIM1200ASM45 − TS001	6.6 kV	713 W	1301 W	366.3 W	2380.3 W
ABB	5SNA0800J450300	11 kV	545.4 W	725 W	178.5 W	1448.9 W
Infineon	FZ800R45KL3_B5	11 kV	521.3 W	851.7 W	227.9 W	1600.9 W
Dynex	DIM800XSM45 − TS001	11 kV	569.3 W	843.2 W	237.4 W	1649.9 W
ABB	5SNA0650J450300	22kV	221.2 W	432.5 W	116.1 W	769.8 W
Infineon	FZ800R45KL3_B5	22kV	195.1 W	648.8 W	173 W	1016.9 W
Dynex	DIM400XSM45 − TS001	22kV	341.97 W	328.8 W	90.1 W	760.9 W
ABB	5SNA0400J650100	33 kV	234.3 W	355.3 W	83.04 W	672.6 W
Infineon	FZ400R65KE3	33 kV	161 W	411.6 W	96.3 W	668.9 W
Dynex	DIM500XSM65 − TS	33 kV	157.5 W	444.8 W	139.6 W	741.9 W

The heat dissipation in an IGBT module is distributed within its junction, case, heatsink, and ambient [148], due to their respective thermal resistance, as illustrated in Figure 3.15. The value of the thermal resistance of a heatsink (R_{THh}) is dependent on T_j, the ambient temperature (T_a) and the associated thermal resistance of the IGBT module, as shown in Figure 3.15. The calculated values of R_{THJ-C}, R_{THC-H} and R_{THh} for the different IGBT modules are presented in Tables 3.16 and 3.17 (derived equation can be found in Appendix A.3). From the analyses presented in this section, the most suitable IGBT modules for an NNPC and MNNPC converter topology directly connected to the collection points of a WPP are stated in Table 3.18.

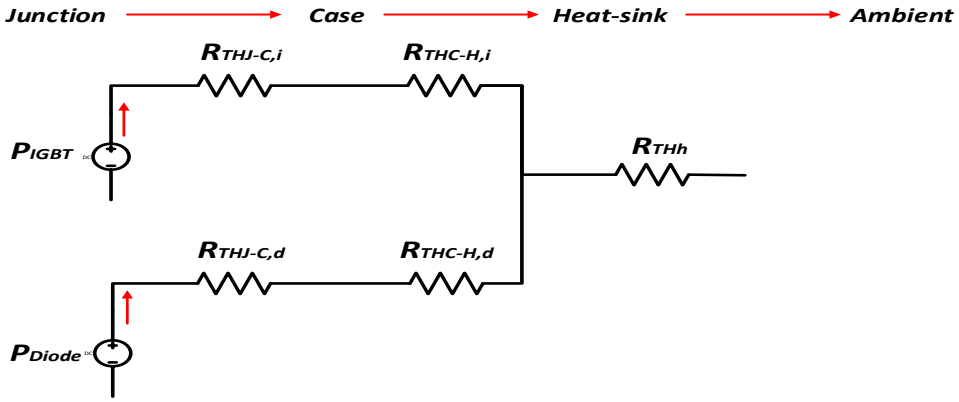


Figure 3.15: Thermal model of an IGBT module.

Table 3.16: Thermal resistance of the IGBT modules

Company	IGBT Module Ref. No.	$R_{THJ-C,i}$ (k/W)	$R_{THJ-C,d}$ (k/W)	R_{THJ-C} (k/W)	$R_{THC-H,i}$ (k/W)	$R_{THC-H,d}$ (k/W)	R_{THC-H} (k/W)
ABB	5SNA1200G450300	0.0095	0.019	0.0063	0.009	0.018	0.006
Infineon	FZ1200R45HL3	0.0082	0.014	0.0051	0.010	0.011	0.0063
Dynex	DIM1200ASM45 – TS001	0.008	0.016	0.0053	0.009	0.018	0.006
ABB	5SNA0800J450300	0.014	0.028	0.0093	0.013	0.027	0.0087
Infineon	FZ800R45KL3_B5	0.011	0.026	0.0077	0.014	0.021	0.0094
Dynex	DIM800XSM45 – TS001	0.012	0.024	0.008	0.012	0.024	0.008
ABB	5SNA0650J450300	0.015	0.03	0.01	0.013	0.027	0.0087
Infineon	FZ800R45KL3_B5	0.011	0.026	0.0077	0.014	0.021	0.0094
Dynex	DIM400XSM45 – TS001	0.024	0.048	0.016	0.024	0.048	0.008
ABB	5SNA0400J650100	0.016	0.032	0.0106	0.014	0.024	0.008
Infineon	FZ400R65KE3	0.015	0.033	0.0143	0.014	0.022	0.0132
Dynex	DIM500XSM65 – TS	0.014	0.027	0.009	0.0012	0.0024	0.008

Table 3.17: Thermal resistance of the heatsink.

Company	IGBT Module Ref. No.	V_{LL}	P_{tot}	R_{THh}(k/W)
ABB	5SNA1200G450300	6.6 kV	2357.3 W	0.024
Infineon	FZ1200R45HL3	6.6 kV	2351.5 W	0.025
Dynex	DIM1200ASM45 − TS001	6.6 kV	2380.3 W	0.024
ABB	5SNA0800J450300	11 kV	1448.9 W	0.041
Infineon	FZ800R45KL3_B5	11 kV	1600.9 W	0.036
Dynex	DIM800XSM45 − TS001	11 kV	1649.9 W	0.036
ABB	5SNA0650J450300	22kV	769.8 W	0.04
Infineon	FZ800R45KL3_B5	22kV	1016.9 W	0.027
Dynex	DIM400XSM45 − TS001	22kV	760.9 W	0.035
ABB	5SNA0400J650100	33 kV	672.6 W	0.108
Infineon	FZ400R65KE3	33 kV	668.9 W	0.09
Dynex	DIM500XSM65 − TS	33 kV	741.9 W	0.098

Table 3.18: Suitable IGBT modules

Company	IGBT Module Ref. No.	V_{LL}
Infineon	FZ1200R45HL3	6.6 kV
ABB	5SNA0800J450300	11 kV
Dynex	DIM400XSM45 − TS001	22kV
Infineon	FZ400R65KE3	33 kV

C. Clamping Capacitors

The capacitance of the clamping capacitors in the 4L-NNPC converter topology (as shown in Figure 3.2) is obtained (3.57). The maximum allowable voltage ripple is 15% for the NNPC and MNNPC converter topologies, as stated in [71], [129], [130].

$$C_{fx\_4L} = \frac{3I_{ph}}{0.15V_{dc\_max} \cdot f_{sw}} \tag{3.57}$$

where C_{fx_4L} represents the capacitance of each clamping capacitor C_{fx1} and C_{fx2} (i.e. $C_{fx1} = C_{fx2}$) in a 4L-NNPC converter topology.

The capacitance of the clamping capacitors in the 5L-NNPC converter topology (as shown in Figure 3.4(c)) is obtained from (3.58) to (3.59).

$$C_{x3\_5L} = \frac{4I_{ph}}{0.45V_{dc\_max} \cdot f_{sw}} \tag{3.58}$$

$$C_{x\_5L} = \frac{4I_{ph}}{0.15V_{dc\_max} \cdot f_{sw}} \tag{3.59}$$

where C_{x3_5L} represents the capacitance of the outer clamping capacitor C_{x3} (as shown in Figure 3.4(c)); C_{x_5L} represents the capacitance of the inner clamping capacitor C_{x1} and C_{x2} (i.e., $C_{x1} = C_{x2}$) in a 5L-NNPC converter topology.

The capacitance of the clamping capacitors in the 7L-MNNPC converter topology (as shown in Figure 3.6(c)) is obtained from (3.60).

$$C_{x\_7L} = \frac{6I_{ph}}{0.15V_{dc\_max} \cdot f_{sw}} \tag{3.60}$$

where C_{x_7L} represents the capacitance of the clamping capacitor C_{x1} and C_{x2} (i.e., $C_{x1} = C_{x2}$) in a 7L-MNNPC converter topology.

D. DC-Link Capacitors

Both the NNPC and MNNPC converter topologies are based on the split dc-link capacitor configuration, as shown in Figures 3.3, 3.5, 3.7, respectively. In Figure 3.7, the current flowing into and out of the dc-link capacitors of a 3ph 7L-MNNPC converter topology; with i_{dc} representing the dc-link current flowing from the generator-side converter, i_{cdc1} and i_{cdc2} are current flowing into C_{dc1} and C_{dc2}, i_n is the neutral-point current, and i_1 is the dc-link current flowing into the grid-side converter, as illustrated. Due to the series connection of the dc-link capacitors with the capacitance value being equal ($i.e. C_{dc1} = C_{dc2} = C_{dc}$), the total dc-link capacitance ($C_{dc,total}$) as shown in Figure 3.16(a) [162], is expressed in (3.61).

$$C_{dc,total} = \frac{C_{dc} \cdot C_{dc}}{C_{dc} + C_{dc}} = \frac{C_{dc}}{2} \tag{3.61}$$

According to the dynamic model of the dc-link capacitors of an NNPC and MNNPC converter topology shown in Figure 3.16(b), the capacitors are in parallel connection when considering the neutral-point virtually [162], as expressed in (3.62).

$$C_{dc,NP} = C_{dc1} + C_{dc2} = 2C_{dc} \tag{3.62}$$

Therefore, the dc-link capacitor current (i_{cdc}) shown in Figure 3.16(a) can be derived using Kirchhoff Current Law, as stated in (3.63).

$$i_{cdc} = i_{dc} - i_1 \tag{3.63}$$

Furthermore, i_{cdc}, i_{dc} and i_1 can be classified into average and ripple components which can be represented by $\bar{I}_{cdc}$ and $\hat{\imath}_{cdc}$, $\bar{I}_{dc}$ and $\hat{\imath}_{dc}$, and $\bar{I}_1$ and $\hat{\imath}_1$, respectively [163]. Therefore, (3.63) can be rewritten as (3.64).

$$\bar{I}_{cdc} + \hat{\imath}_{cdc} = \bar{I}_{dc} + \hat{\imath}_{dc} - \bar{I}_1 - \hat{\imath}_1 \tag{3.64}$$

The main factors affecting the dc-link voltage ripple of a split dc-link capacitor configuration of a multilevel converter topology have been presented in [136]. The value of the dc-link capacitance of the NNPC and MNNPC converter deploying in the grid-side converter of a transformer-less WECS is affected by the ripple due to grid frequency as expressed in (3.65) [136].

$$C_{dc\_freq} \geq \frac{S_A}{2\omega_g V_{dc\_max} \Delta V_{dc}} \tag{3.65}$$

where C_{dc_freq} is the capacitance of the dc-link because of ripples due to grid frequency, ω_g is the grid frequency in rad/sec, and ΔV_{dc} is the maximum dc-link voltage ripple which is given as 30% [136].

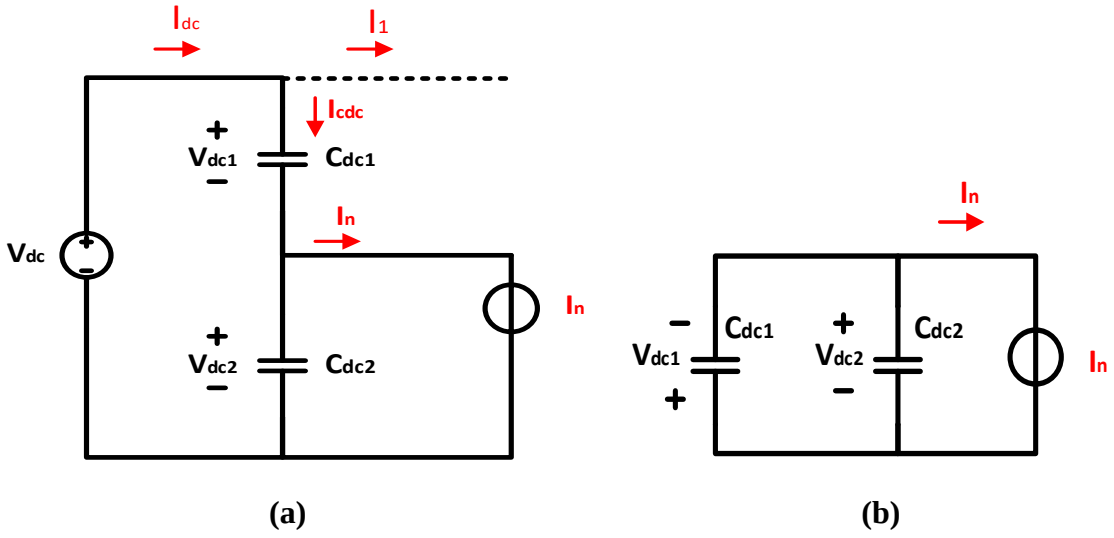


Figure 3.16: Equivalent circuit of the neutral point connection of NNPC and MNNPC converter topologies. (a) physical connection, (b) virtual connection.

3.3. Simulation Results

To verify the converter design and analysed the grid-connected scenarios of the 4L-NNPC, 5L-NNPC, and 7L-MNNPC converter topologies deployed in a transformer-less WECS configuration, simulations are carried out using MATLAB/Simulink with the parameters stated

in Table 3.19 and previously in Table 3.7 to Table 3.9. The simulation presented in this section is based on the ideal components. The maximum dc-link voltage of the NNPC and MNNPC converter topologies is assumed to be constant in the presented simulation results. Therefore, the simulation results are shown in two main sections to verify the theoretical analysis and derivations stated previously in the chapter:

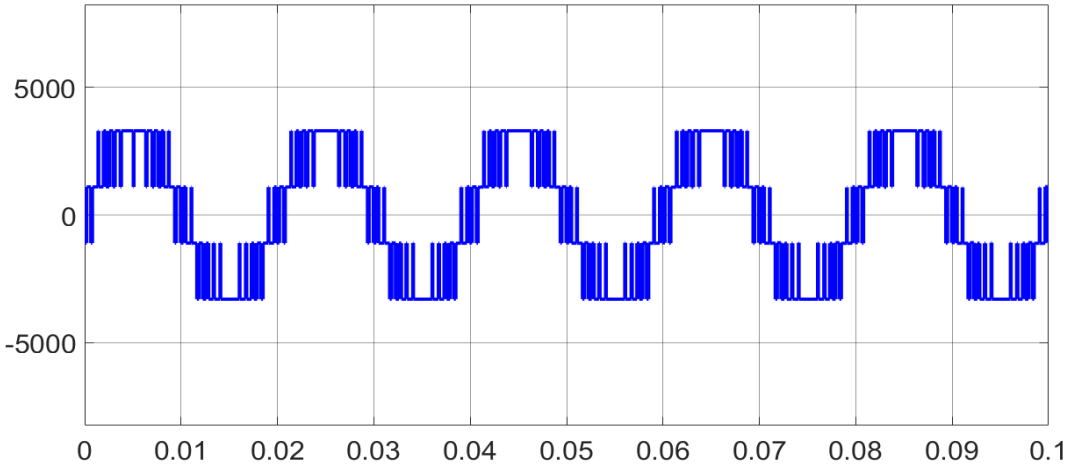
- Design verification: Section 3.3.1 provides the NNPC and MNNPC converter topologies' voltage waveforms to validate their respective operating principles stated in Sections 3.1.1 to 3.1.3.
- Grid connection scenarios: Section 3.3.2 presents the voltage sag transformation take in a conventional WPP and a WPP with substation transformer and transformer-less WECSs. Furthermore, the impact of asymmetrical voltage sags on the dc-link voltage is analysed in the section.

Table 3.19: Parameters of the NNPC and MNNPC

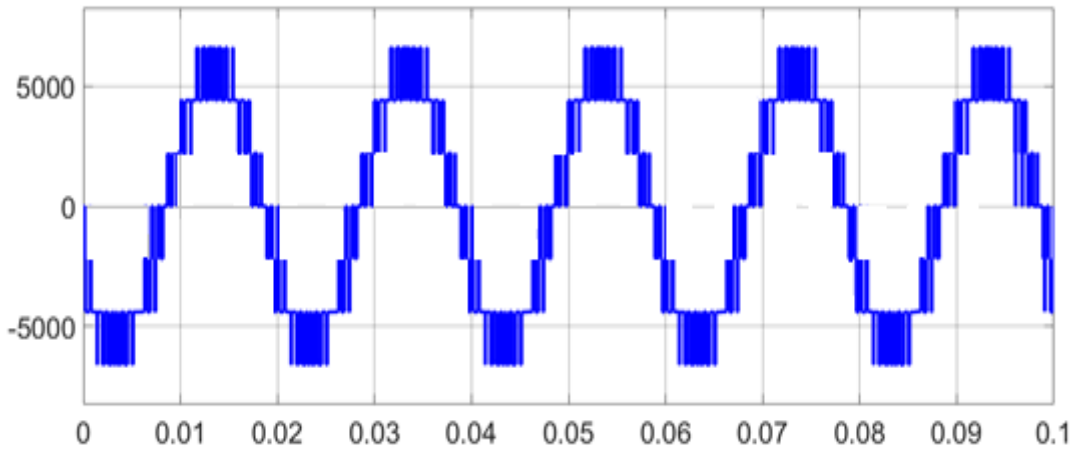
Symbol	Description	4L-NNPC	5L-NNPC	7L-MNNPC
S_A	Apparent power rating	6.7 MVA	6.7 MVA	6.7 MVA
V_{LL}	Line voltage	6.6 kV	6.6 kV	11 kV
I_{ph}	Phase current	583.2 A	583.2 A	350 A
C_{DC}	DC-link capacitor	355 μF	355 μF	131 μF
V_{dc_max}	DC-link voltage	10 kV	10 kV	16.5 kV
C_{fx_4L}	Clamping capacitor	233 μF	–	–
C_{x3_5L}	Outer clamping capacitor	–	1036 μF	–
C_{x_5L}	Inner clamping capacitor	–	311 μF	–
C_{x_7L}	Clamping capacitor	–	–	1697 μF
L_g	Grid-side inductance	0.46 H	0.46 H	1.28 H
R_g	Grid-side resistance	14 Ω	14 Ω	67.2 Ω
f_{sw}	Switching frequency	500 Hz	500 Hz	500 Hz

3.3.1. Design Verification

Figure 3.17 to Figure 3.19 shows the phase and line voltage waveforms of the NNPC and MNNPC converter topologies, respectively. The THD of the NNPC and MNNPC converter topologies is shown in Figure 3.20.

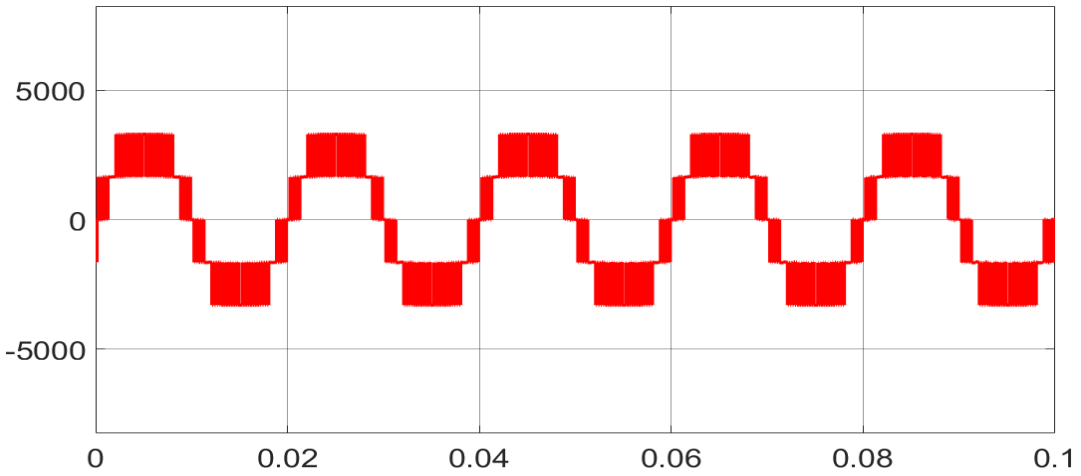


(a)

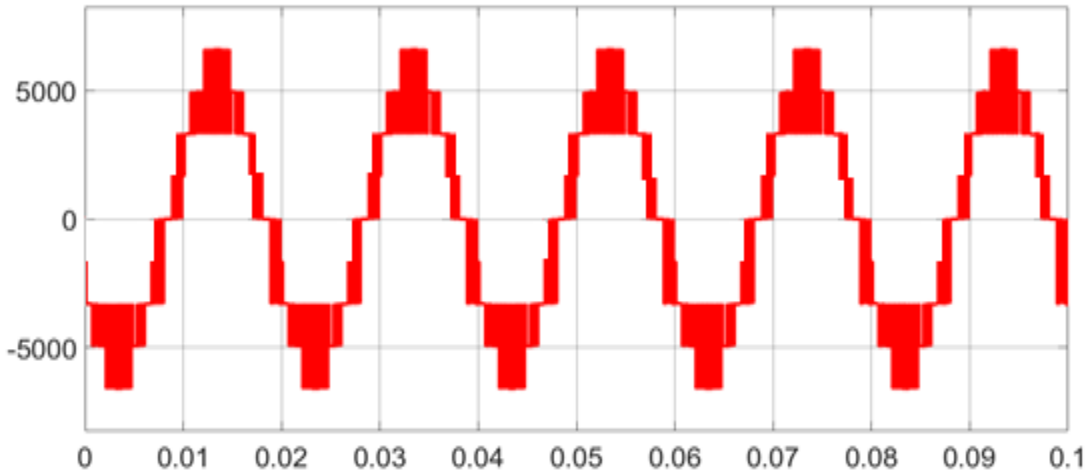


(b)

Figure 3.17: Output voltage waveform of a 4L-NNPC converter topology. (a) phase voltage waveform, and (b) line voltage waveform.

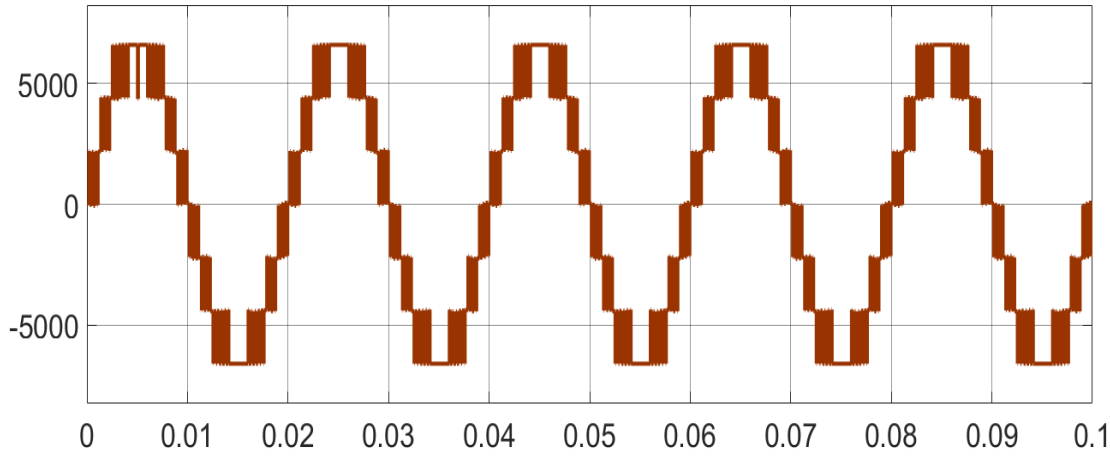


(a)

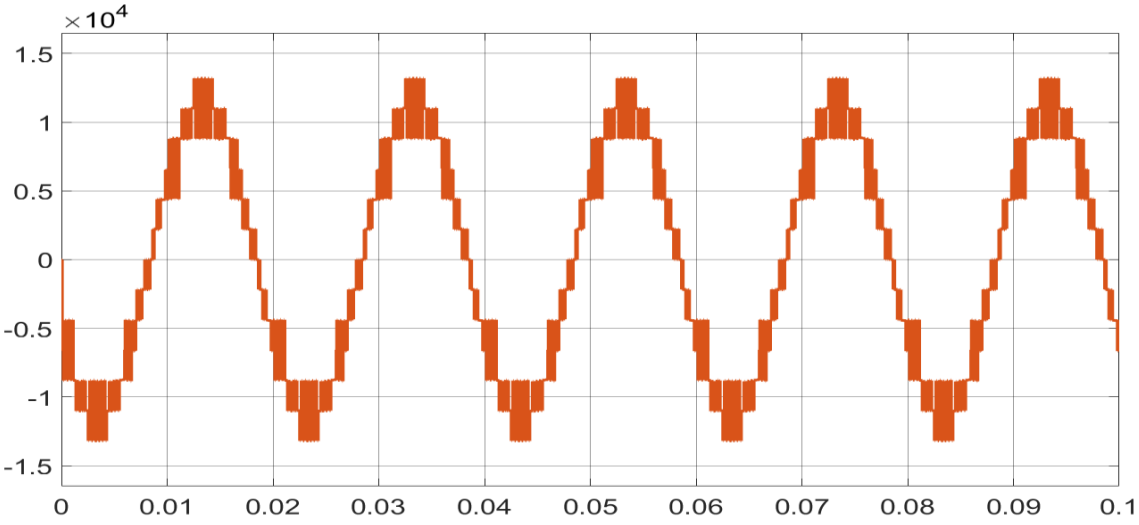


(b)

Figure 3.18: Output voltage waveform of a 5L-NNPC converter topology. (a) phase voltage waveform, and (b) line voltage waveform.

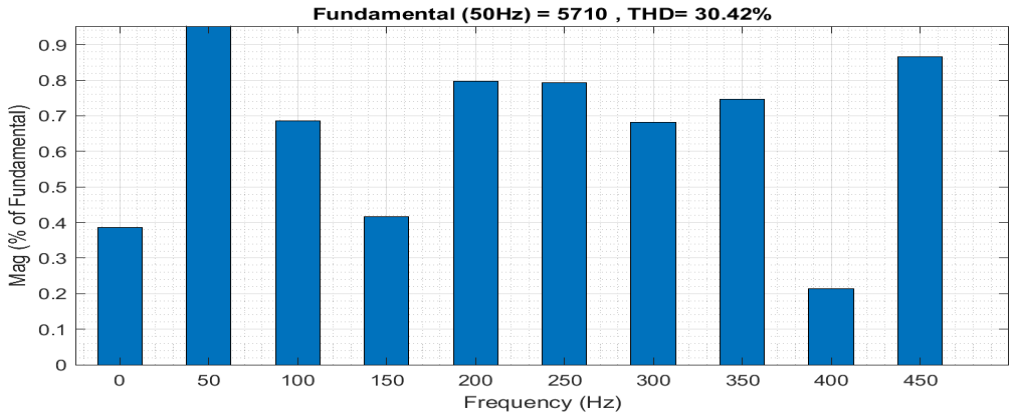


(a)

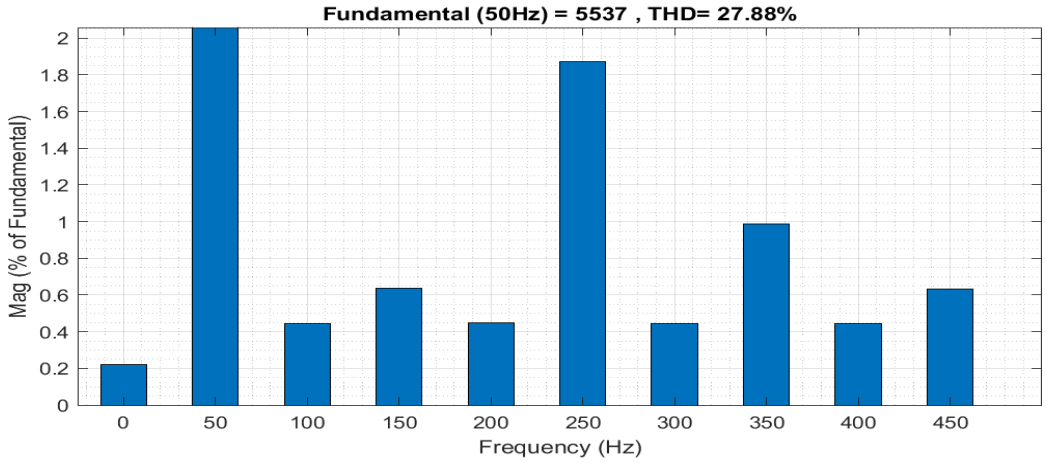


(b)

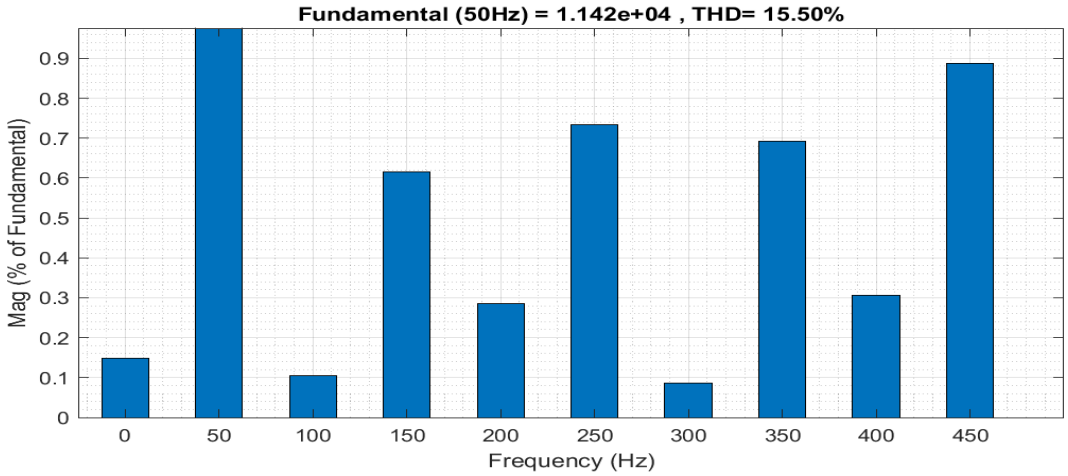
Figure 3.19: Output voltage waveform of a 7L-MNNPC converter topology. (a) phase voltage waveform, and (b) line voltage waveform.



(a)



(b)



(c)

Figure 3.20: Total harmonic distortion (THD). (a) 3ph 4L-NNPC, (b) 3ph 5L-NNPC, and (c) 3ph 7L-MNNPC.

3.3.2. Grid connection scenarios

In Chapter 2, the voltage sag transformation within a conventional WPP has been discussed briefly. Detailed analysis of the voltage sag transformation within a conventional WPP and a WPP with transformer-less WECS is presented based on simulations carried out in the MATLAB/Simulink environment. The results are carried out and observed under three distinct scenarios, namely: (a) voltage sag propagation in a conventional WPP, (b) voltage sag propagation in a WPP with transformer-less WECS, and (c) impact of voltage sags on the dc-link voltage of the grid-side converter.

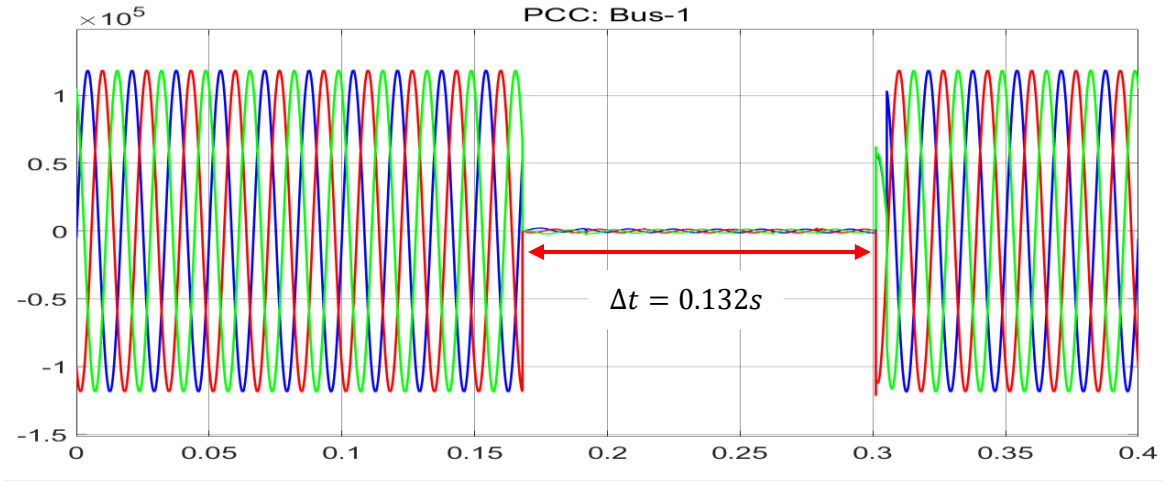
A. Voltage Sag Propagation in a Conventional WPP

Figure 2.3 illustrates a conventional WPP model with a short-circuit fault at the PCC between the grid and the WPP; the three notable buses of the model are as follows, Bus-1 represents the PCC, Bus-2 represents the collection point: and Bus-3 represents WECS. In Table 3.20, the impacts of both symmetrical and asymmetrical voltage sags on the WECS terminal in a conventional WPP is highlighted.

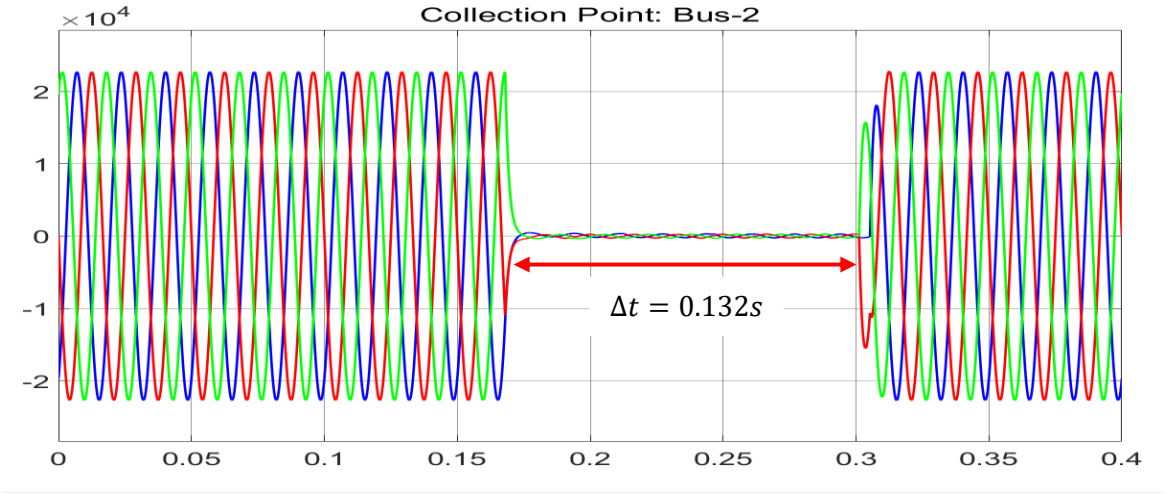
The respective waveforms of the voltage sag propagated within a conventional WPP are shown in Figures 3.21 to 3.24. Type-A sag is a symmetrical voltage sag that affects the entire three-phases voltage magnitude (3ph) with an estimated 96% voltage drop [55]. While the original Type-B sag is transformed to Type-D sag at the WECS terminal, with voltage drops in two phases and phase-angle jump in two phases. Amongst the asymmetrical voltage sags, the Type-E sag (in Bus-1) transformed to Type-G sag (in Bus-3) showed the highest severity with a 57.4% voltage drop in two phases and a severe phase-angle jump.

Table 3.20: Impact of voltage sags on the WECS in a conventional WPP.

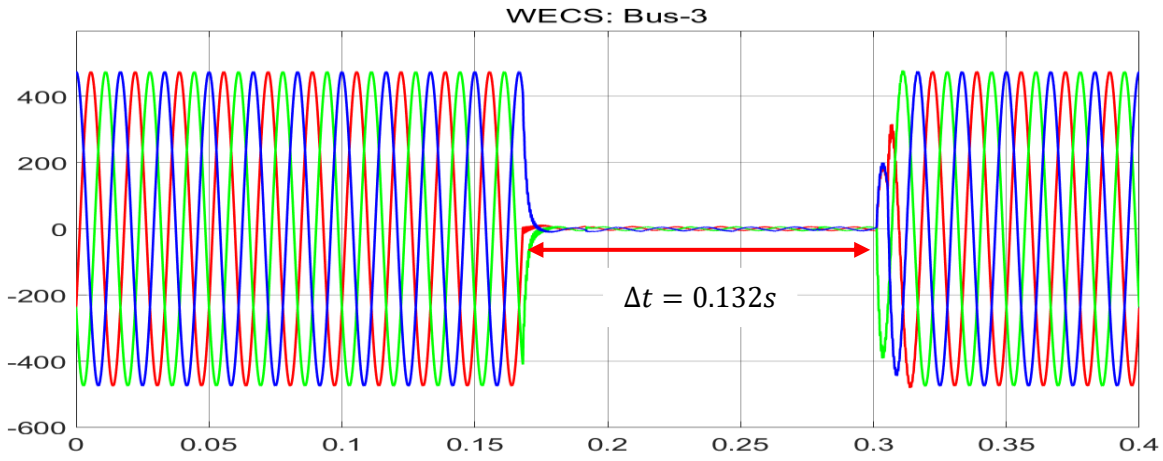
Bus-1	Bus-2	Bus-3	Voltage drop at WECS terminal	Phase-angle jump at WECS terminal
Type-A	Type-A	Type-A	96% in 3ph	none
Type-B	Type-C	Type-D	8.5% in 2ph	mild
			47% in 1ph	
Type-C	Type-D	Type-C	5.3% in 2ph	mild
Type-E	Type-F	Type-G	14.7% in 1ph	severe
			57.4% in 2ph	



(a)

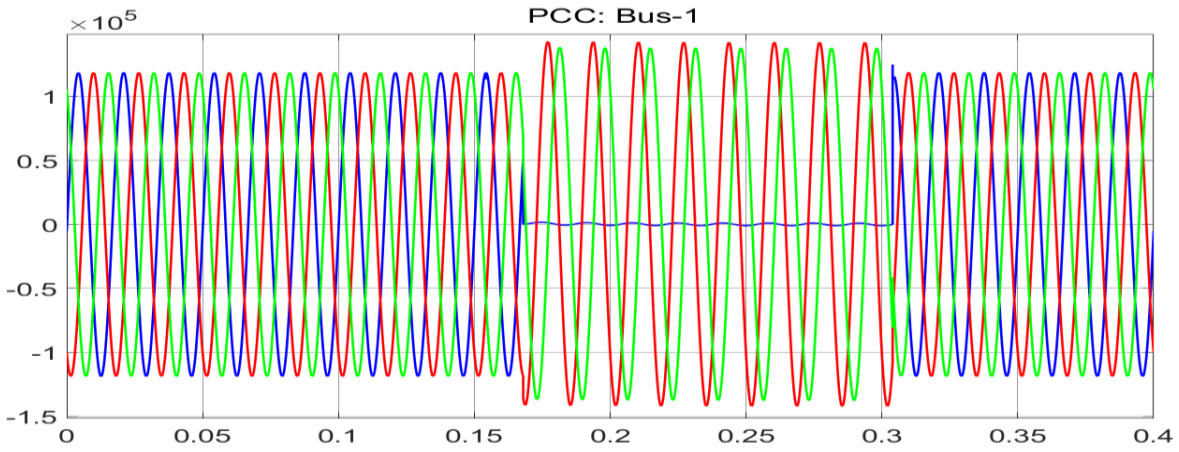


(b)

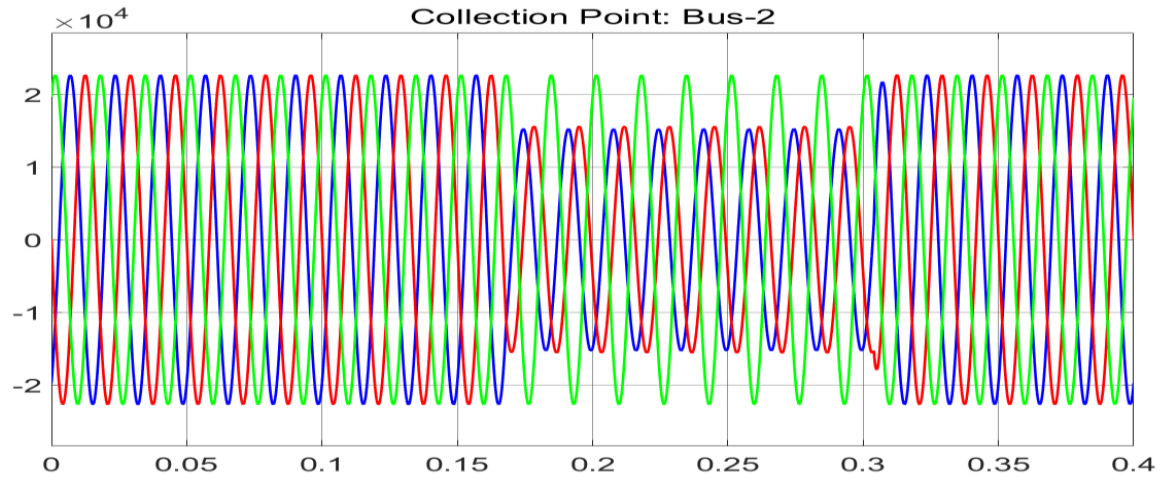


(c)

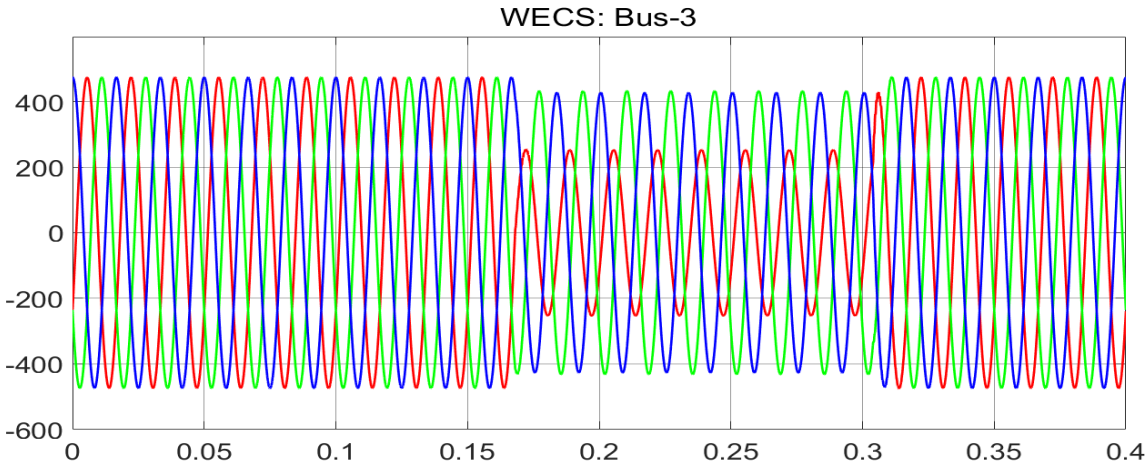
Figure 3.21: Type A (symmetrical) sag in a conventional WPP. (a) Bus -1 (b) Bus-2, and (c) Bus-3.



(a)

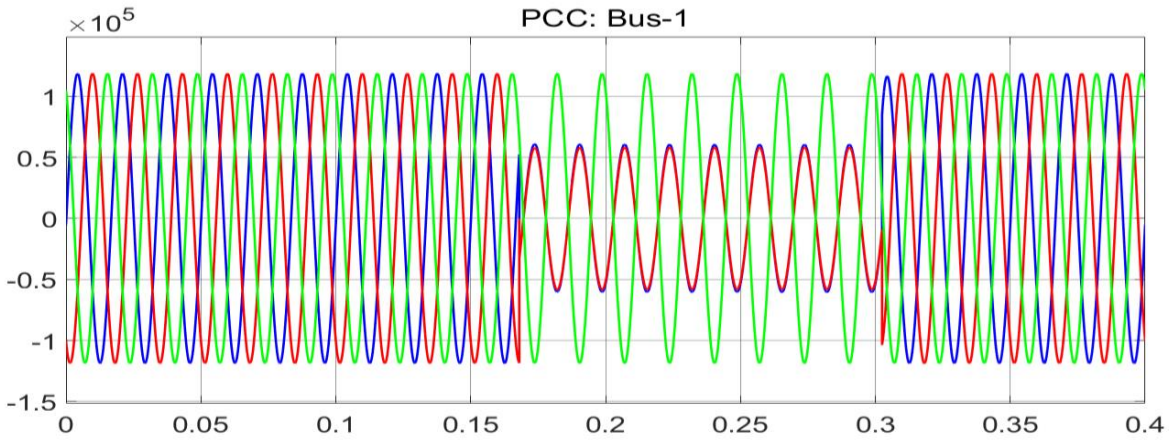


(b)

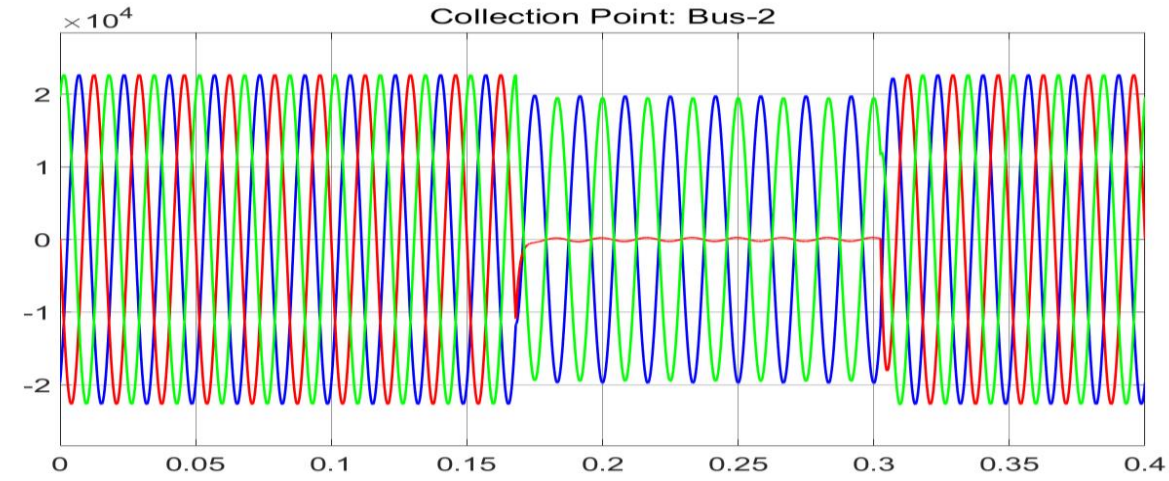


(c)

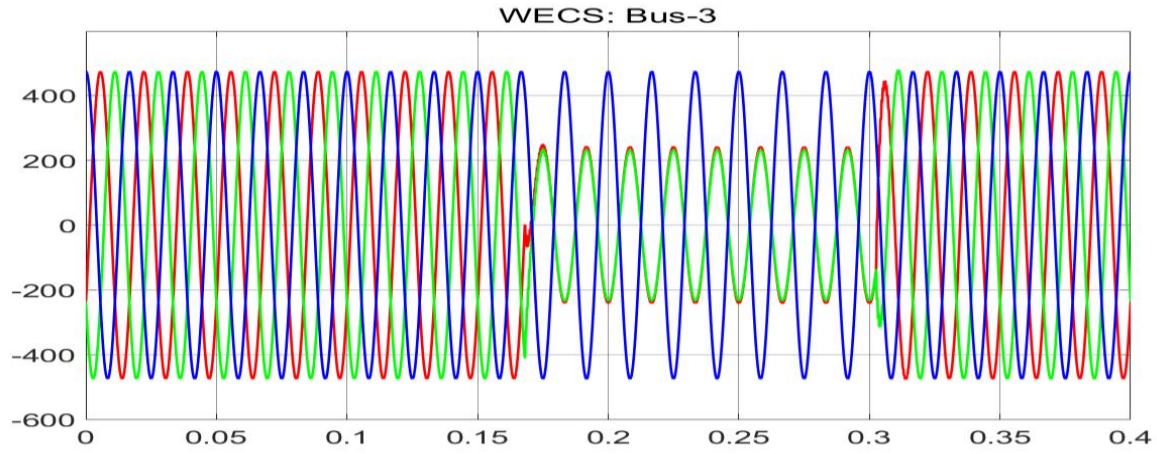
Figure 3.22: Type B (single-phase to ground) sag in a conventional WPP. (a) Bus-1 (b) Bus-2, and (c) Bus-3.



(a)

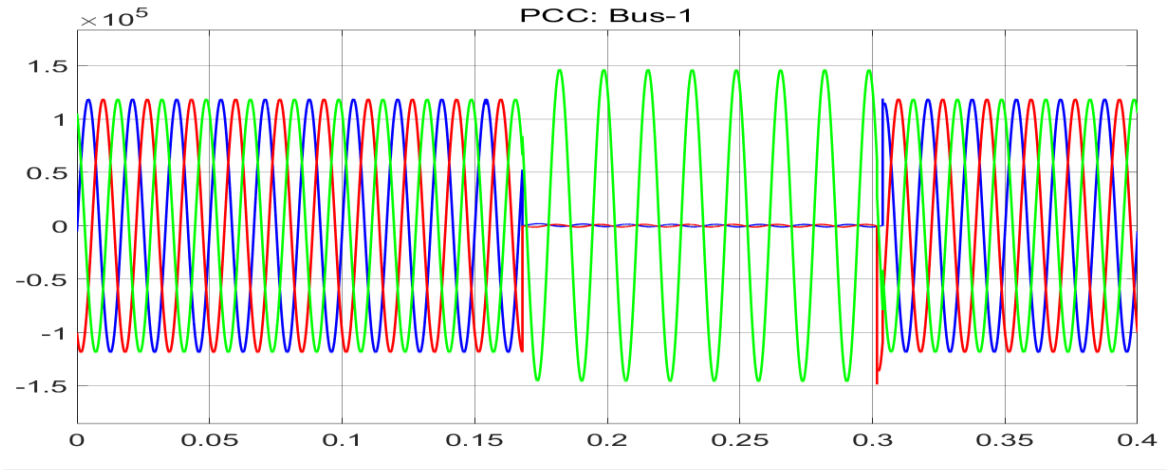


(b)

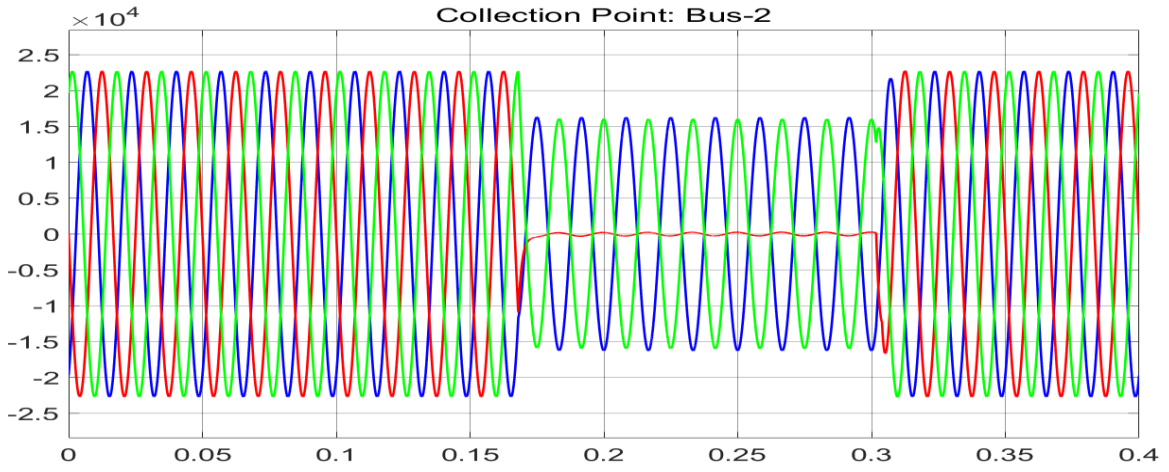


(c)

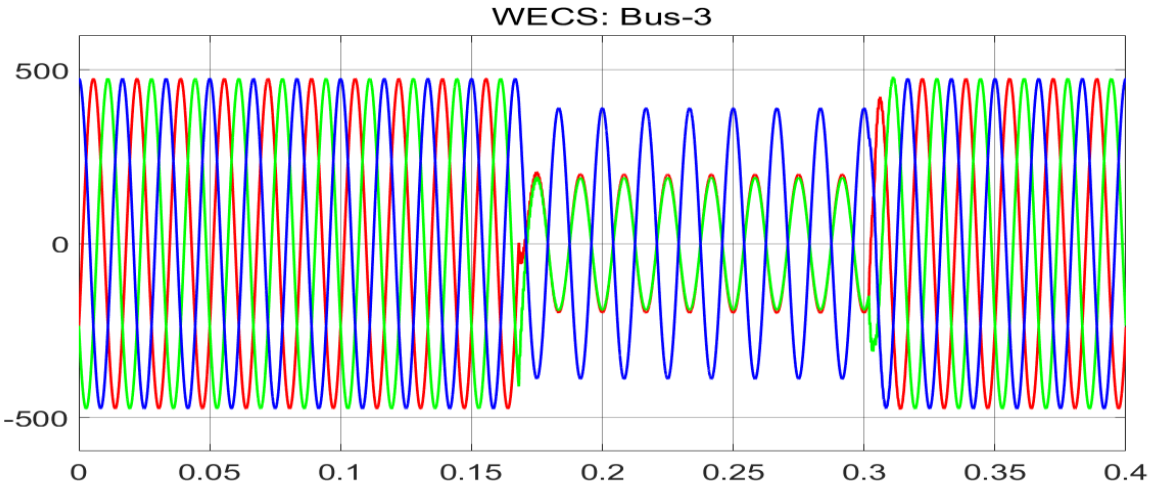
Figure 3.23: Type C (phase-to-phase) sag in a conventional WPP. (a) Bus-1 (b) Bus -2, and (c) Bus-3.



(a)



(b)



(c)

Figure 3.24: Type E (two-phase to ground voltage sag) in a conventional WPP. (a) Bus-1 (b) Bus-2, and (c) Bus-3.

B. Voltage Sag Propagation in a WPP with Transformer-less WECS

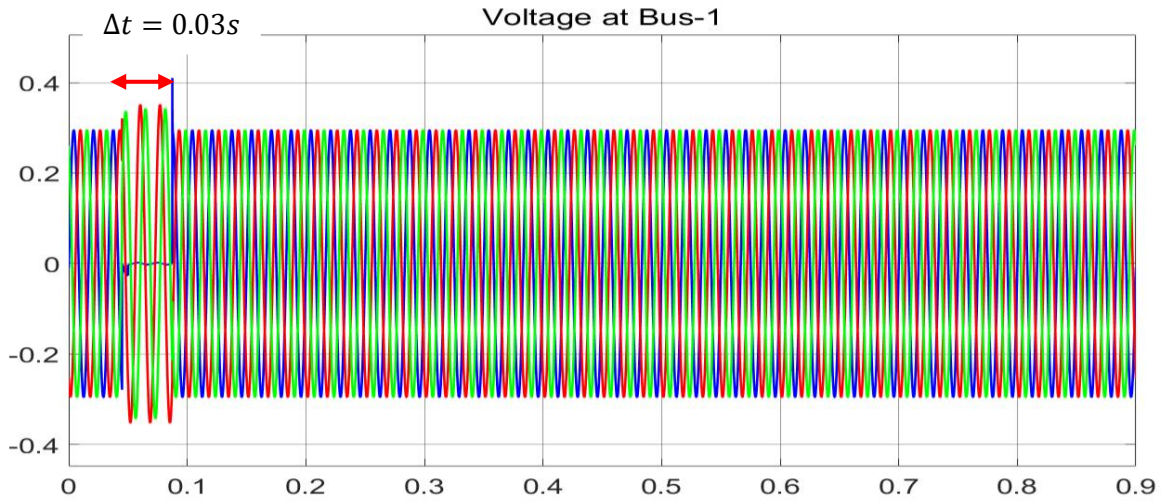
In Table 3.21, the impact of voltage sags propagated within a WPP with transformer-less WECSs has been highlighted. Due to the elimination of the transformer, the severity of the asymmetrical voltage sags is observed in the high phase-angle jump and voltage drops across the WECS terminals. Since the WECS is directly connected to the collection point via a grid-side filter topology, the voltage sag at the Bus-2 (as shown in Figures 3.21(b), 3.22(b), 3.23(b), and 3.24(b), respectively) will directly affect the transformer-less WECS terminal.

C. Impact of Voltage Sags on the DC-Link Voltage of the Grid-side Converter

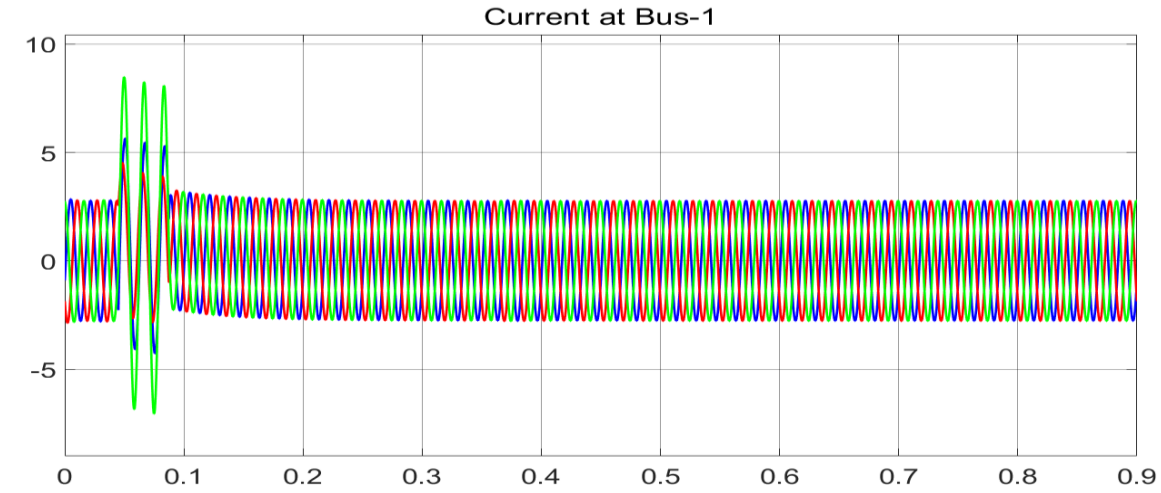
The impact of the voltage sags on the dc-link voltage of the grid-side converter topology in a transformer-less WECS is presented in this section. A five-level NNPC converter topology with a maximum dc-link voltage of $11kV$ was deployed in the grid-side of the transformer-less WECS configuration. The associated voltage and current waveforms at each bus of the WPP with transformer-less WECS are shown in Figures 3.25 to 3.27. After the initial overshoot, the percentage overshoot of the dc-link voltage during the different asymmetrical voltage sags is highlighted in Figure 3.25(e), Figure 3.26(e), and Figure 3.27(e), respectively. The voltage sags with phase-angle jumps and voltage drop have shown the highest level of dc-link voltage overshoot with 43.6% (Type-D sag at the collection point as shown in Figure 3.26(e)), and 48.2% (Type-F sag at the collection point as shown in Figure 3.27(e)). Therefore, severe voltage overshoot will be experienced by the IGBTs in the grid-side converter during Type-D sag and Type-F sag.

Table 3.21: Impact of voltage sags on the transformer-less WECS in a WPP.

Bus-1	Bus-2	Voltage drop at WECS terminal	Phase-angle jump at WECS terminal
Type-A	Type-A	96% in 3ph	none
Type-B	Type-C	20% in 2ph	mild
Type-C	Type-D	20% in 2ph 96% in 1ph	severe
Type-E	Type-F	36% in 2ph 96% in 1ph	severe


$\Delta t = 0.03s$
Voltage at Bus-1
0.4
0.2
0
-0.2
-0.4
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

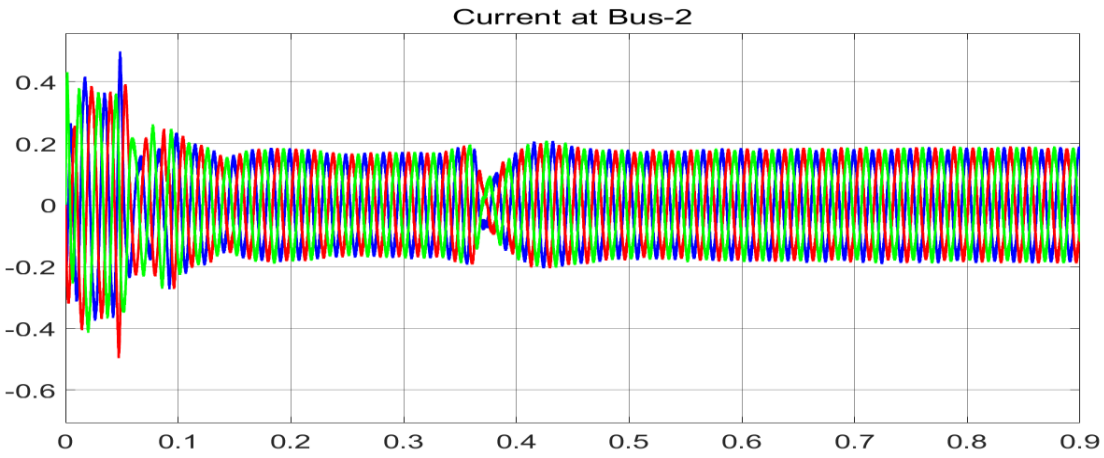
(a)


Current at Bus-1
10
5
0
-5
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

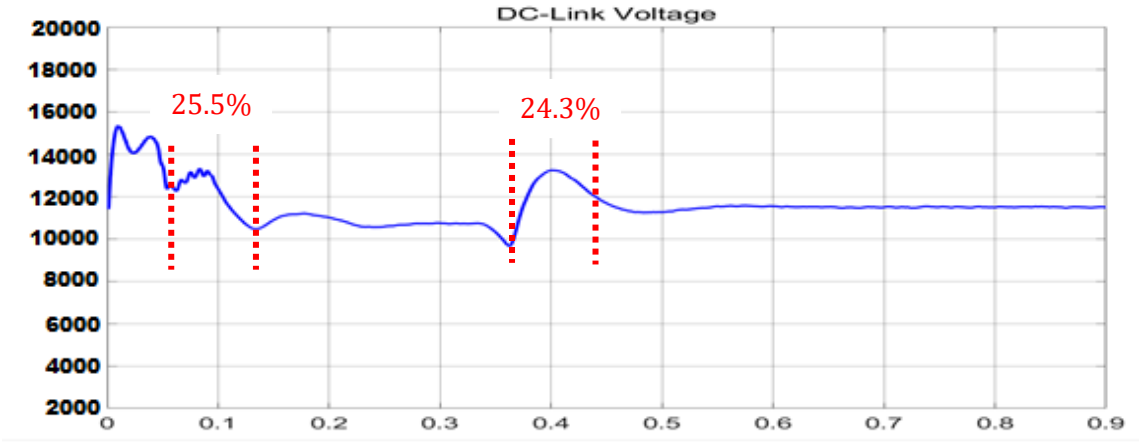
(b)


Voltage at Bus-2
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

(c)

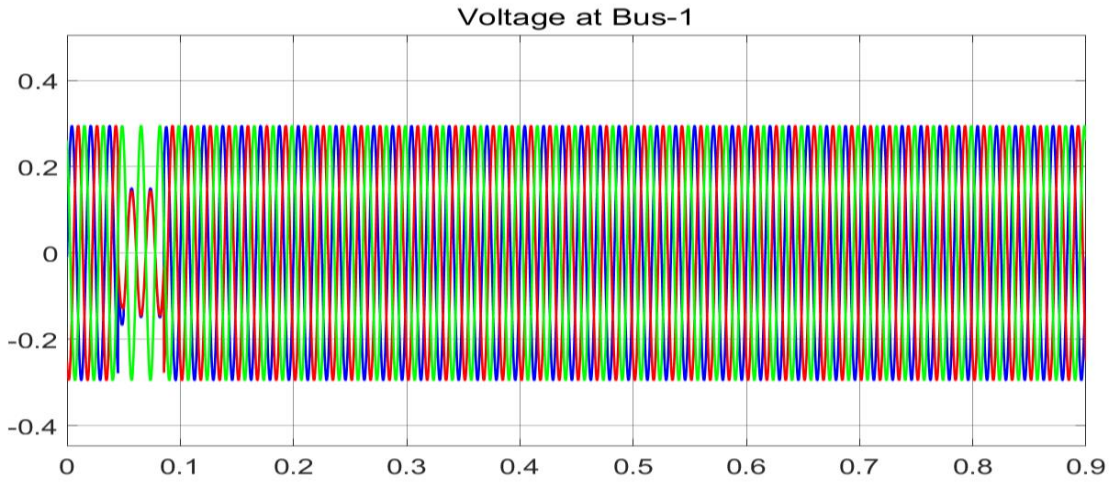


(d)

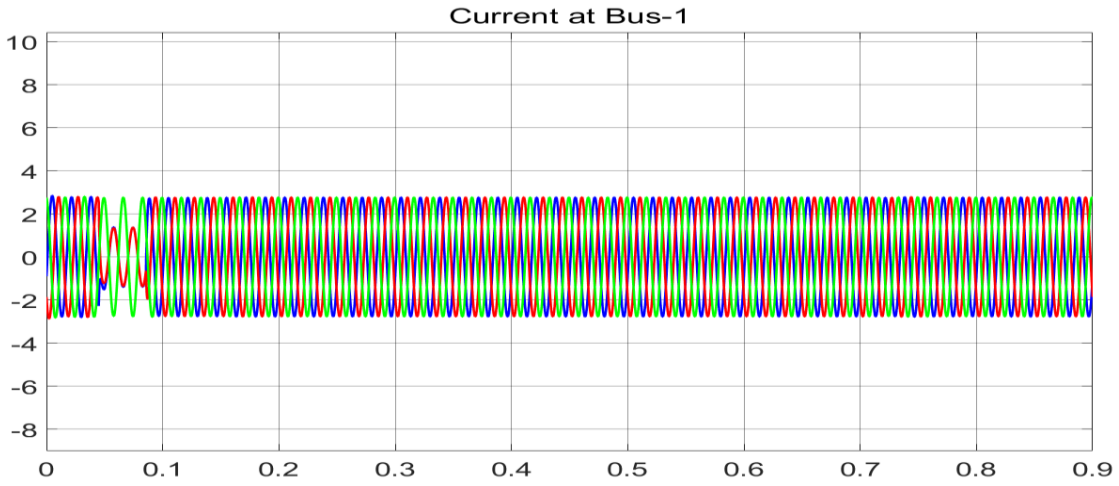


(e)

Figure 3.25: Type B sag in a WPP with transformer-less WECS. (a) voltage at Bus-1, (b) current at Bus-1, (c) voltage at Bus-2, (d) current at Bus-2, and (e) dc-link voltage.



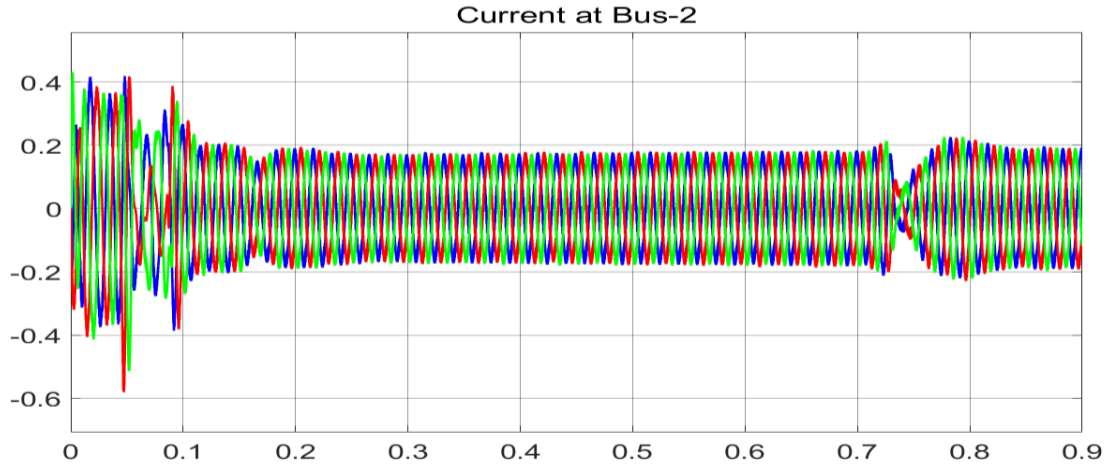
(a)


Current at Bus-1
10
8
6
4
2
0
-2
-4
-6
-8
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

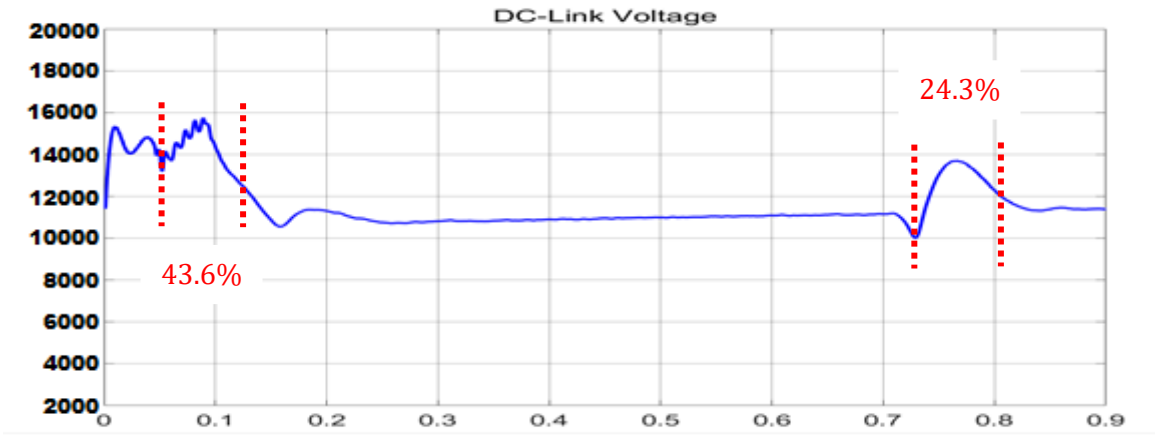
(b)


Voltage at Bus-2
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

(c)

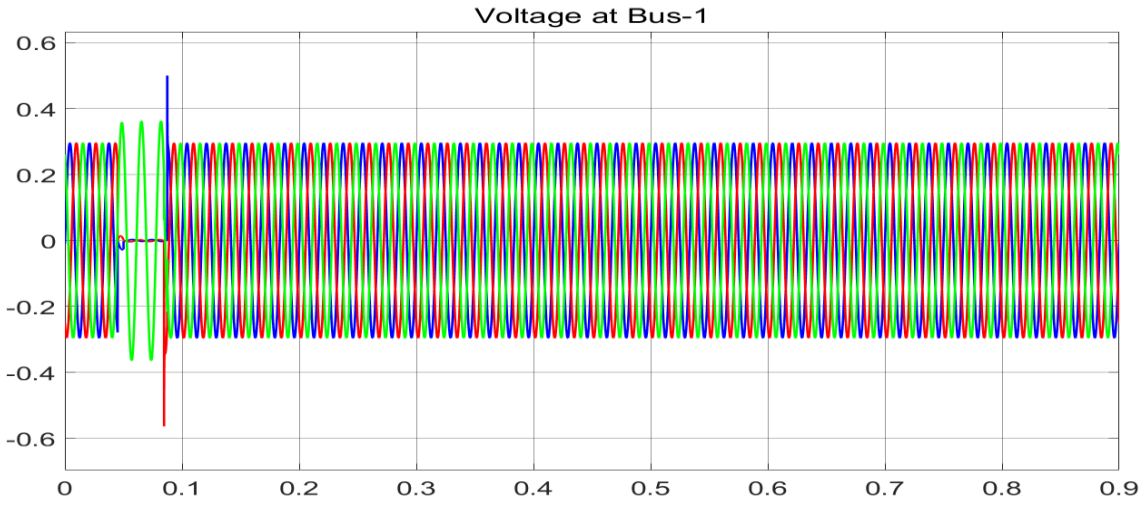

Current at Bus-2
0.4
0.2
0
-0.2
-0.4
-0.6
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

(d)

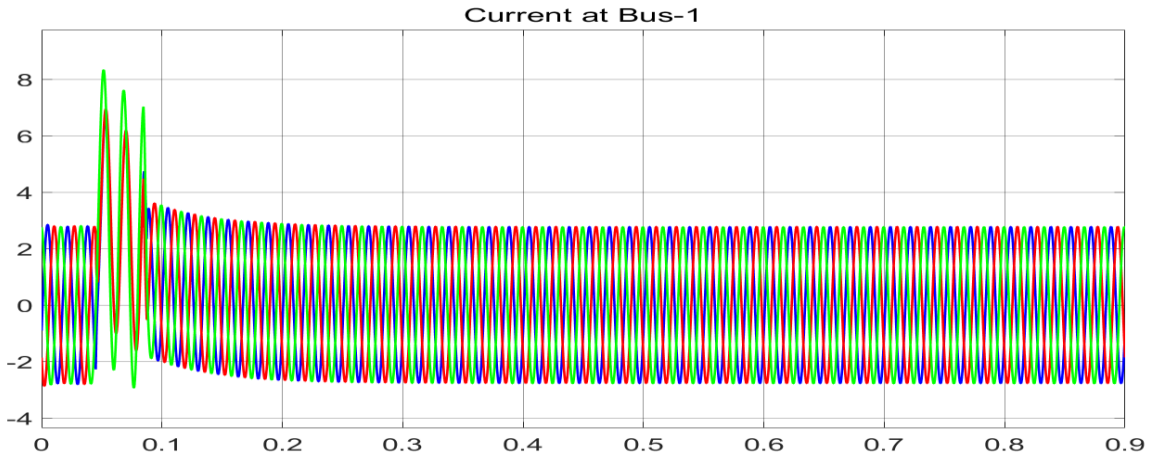


(e)

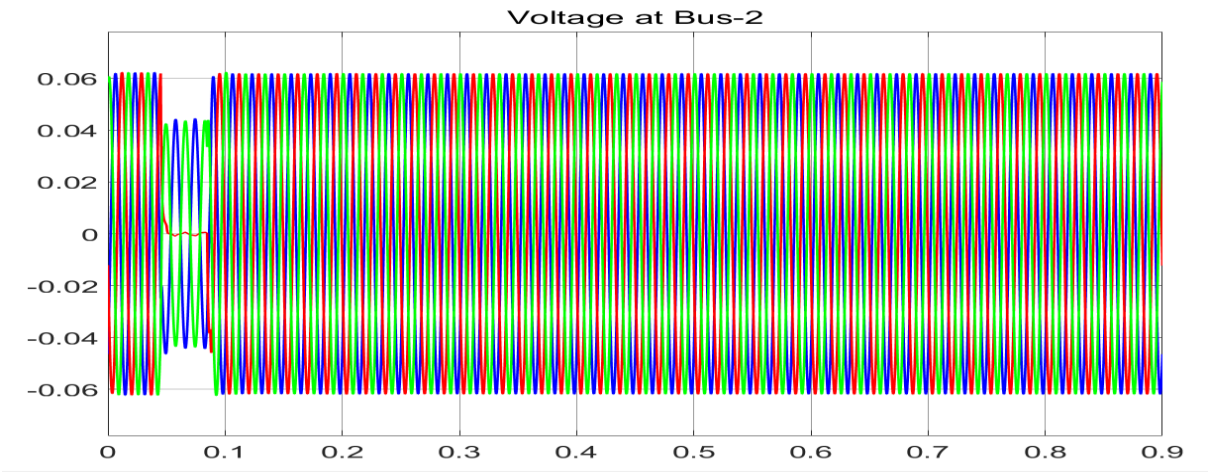
Figure 3.26: Type C sag in a WPP with transformer-less WECS. (a) voltage at Bus-1, (b) current at Bus-1, (c) voltage at Bus-2, (d) current at Bus-2, and (e) dc-link voltage.



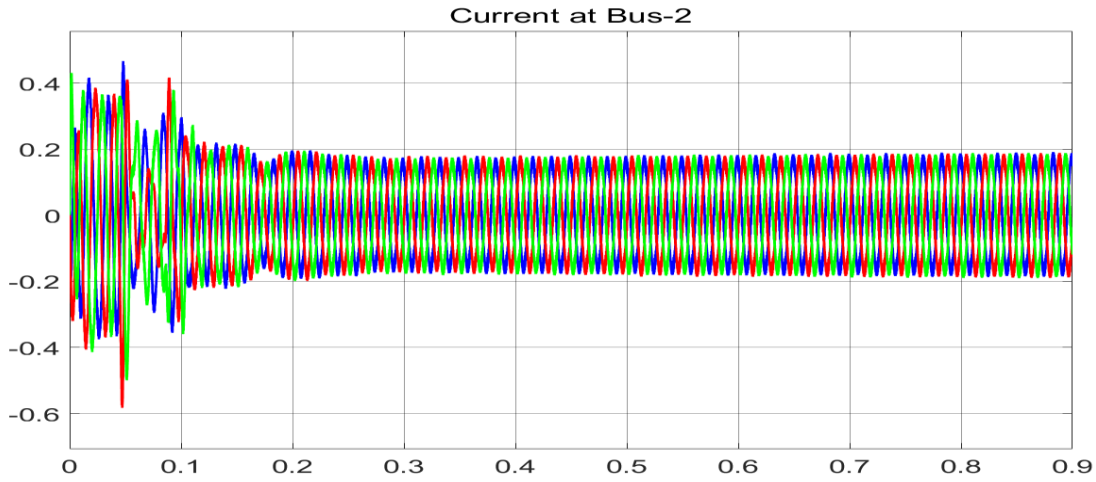
(a)



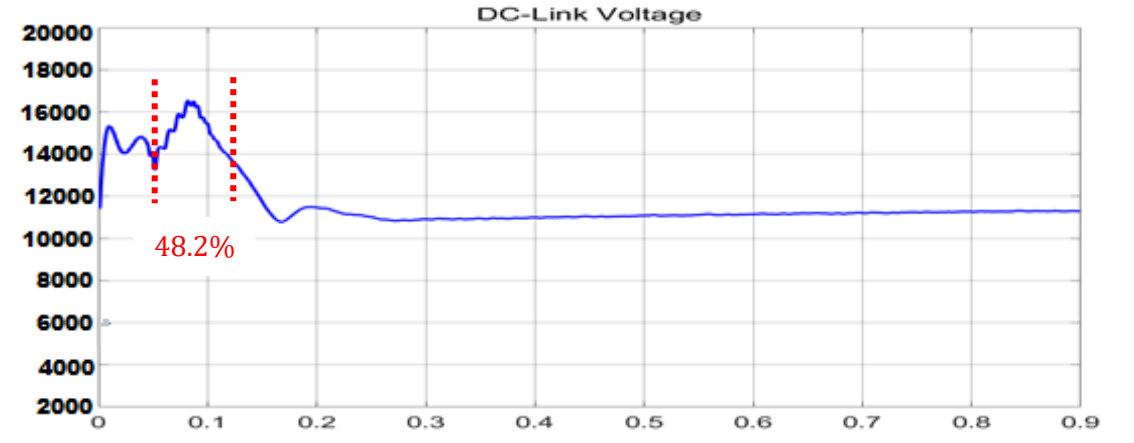
(b)



(c)



(d)



(e)

Figure 3.27: Type E sag in a WPP with transformer-less WECS. (a) voltage at Bus-1, (b) current at Bus-1, (c) voltage at Bus-2, (d) current at Bus-2, and (e) dc-link voltage.

3.4. Conclusion

In this chapter, an NNPC and MNNPC converter topology is proposed for the grid-side converter of a transformer-less WECS configuration. The theoretical analysis and simulation of the NNPC and MNNPC converter topology deployed in the grid-side of a transformer-less WECS configuration is presented. Therefore, this chapter has made the following contributions to the overall research work:

- The derivation of a 4L-NNPC and 5L-NNPC converter topology highlighting its operating principles and mathematical model.
- The derivation of a novel 7L-MNNPC converter topology using a 4L-NNPC converter as building cells is discussed extensively. Its switching states, operating principles, and mathematical model has been presented.
- The detailed converter design for the NNPC and MNNPC converter topology deployed to the grid-side of a transformer-less WECS configuration showing its specifications, average model, and component rating analysis. Detailed simulation results are presented for design verifications and grid-connected scenarios.

Chapter 4

Tapped Inductor Quasi-Z-Source NNPC Converter Topology

The review of existing power converter configurations was presented in Chapter 2, which shows that a three-stage power converter configuration is more reliable, cost-effective, and efficient than its other counterpart. However, a three-stage power converter configuration requires an intermediate boost converter between its generator-side converter and grid-side converter, which increases its complexity. Furthermore, NNPC and MNNPC converter topologies with minimal clamping devices and series connected IGBTs have been presented in Chapter 3. The NNPC and MNNPC converter topologies are classified as voltage source converter (VSC) which implies they are conventional buck converter. Therefore, the two highlighted drawbacks are mitigated by the proposed tapped inductor quasi-Z-source NNPC converter topology with boosting capability in a single stage.

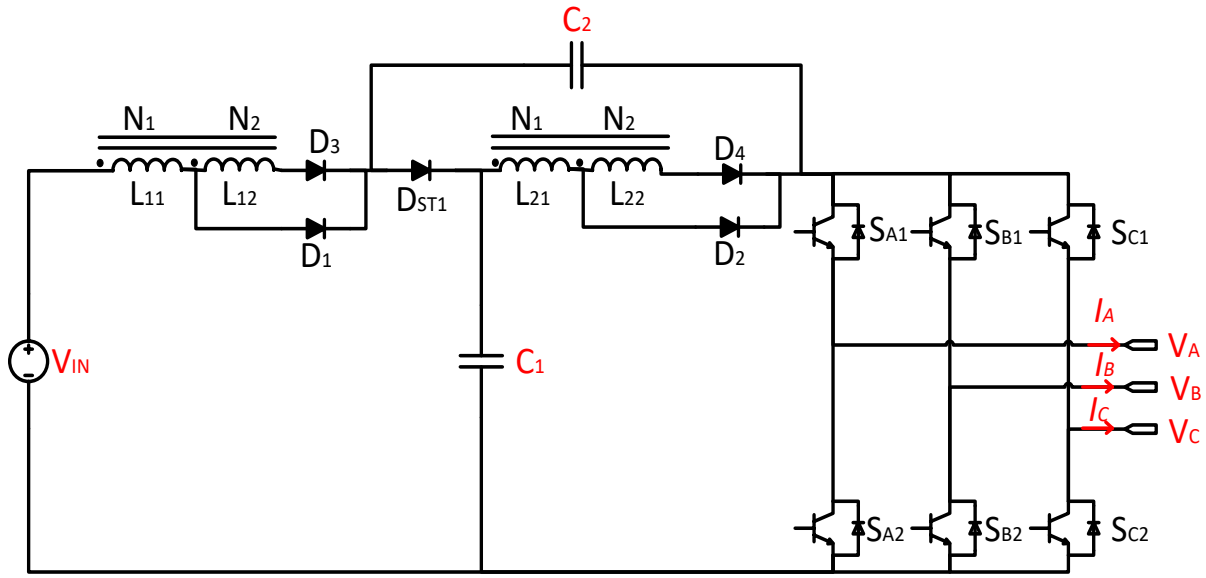
Therefore, this chapter is organized as follows: Introduction to the tapped inductor quasi-Z-source NNPC converter topology is presented in Section 4.1. The design of the tapped inductor quasi-Z-source network is presented in Section 4.2. The modulation technique for a five-level (5L) tapped inductor qZS-NNPC converter topology is shown in Section 4.3. The results and discussions verifying the operating principles, theoretical analysis, and field-programmable gate array (FPGA) implementation of the proposed converter topology are presented in Section 4.4.

4.1. Introduction

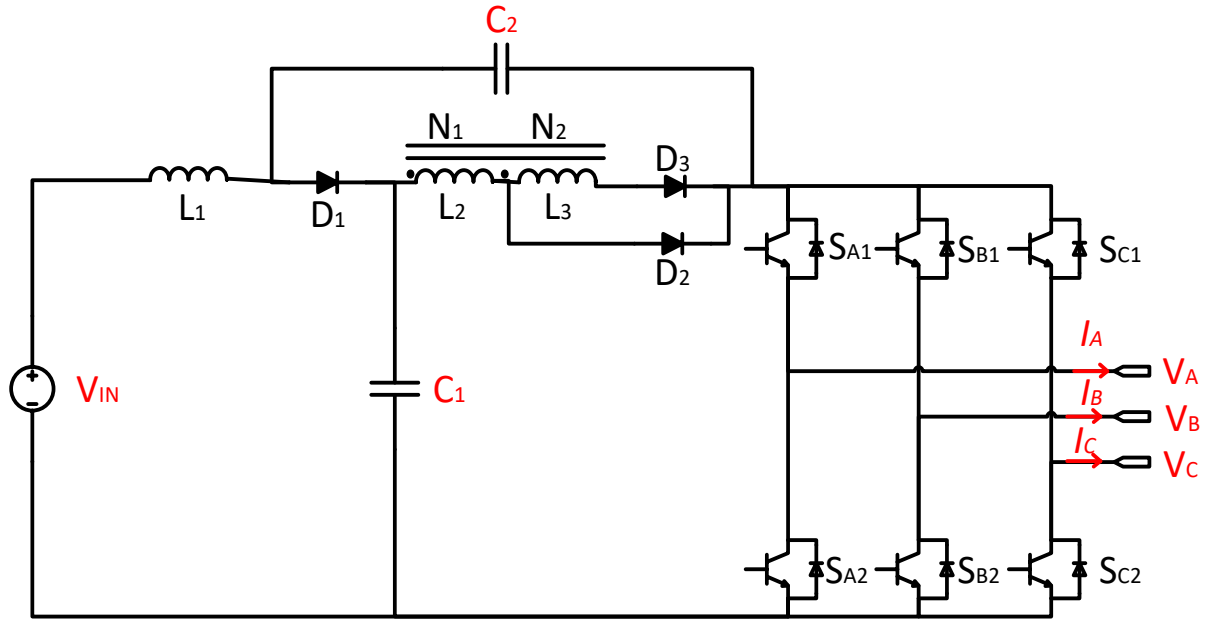
An impedance-source converter topology was first proposed to mitigate and improve the drawbacks associated with both voltage source converter (VSC) and current source converter (CSC) topologies, respectively [169]-[179]. By replacing the passive component of the dc-link (i.e., either the dc-link capacitor or dc-link inductor) with an impedance source network, enables the dc-link voltage to be operated within a voltage range [169]-[179]. The impedance source network provides additional energy storage whilst switching the power semiconductor

devices during the shoot-through period [169]-[179]. A significant drawback of a conventional impedance-source converter topology is its discontinuous conduction mode of operation [169]-[173]. Therefore, a quasi-Z-source converter was proposed to enable continuous conduction mode (CCM) of operation [171], [180].

The quasi-Z-source converter comprises a quasi-impedance-source network and power semiconductor devices, as illustrated in [171]. A significant advantage of the quasi-impedance-source network is its capability to increase the dc-link voltage infinitely [171]. Although, this infinite boosting ability is impeded by significantly high voltage stress across its power semiconductor devices and its low modulation index (*M*) [171], [174]-[177], [180]. Therefore, the boosting ability of a quasi-Z-source converter is improved either through a modulation technique or by utilizing a coupled inductor which requires increasing its turn ratio [174], [175], [177]. A dual-tapped inductor quasi-Z-source converter topology (as shown in Figure 4.1(a)) was deployed for a low-voltage solar photovoltaic (PV) application because it provides a high boost factor whilst keeping a relatively significant modulation index [176]. Also, the voltage gain can be further increased by adjusting the turn ratio of the tapped inductor [176]. Moreover, a simplified tapped inductor quasi-Z-source converter was presented in [181], as shown in Figure 4.1(b). Furthermore, two tapped inductor quasi-impedance-source networks can replace the two dc-link capacitors of a multilevel converter topology with a split dc-link configuration, as shown in Figure 4.2. Therefore, a single-stage power converter configuration combines both a quasi-impedance-source network and a multilevel converter topology [176], [180]. Accordingly, the presented NNPC and MNNPC converter topologies shown in the previous chapter are modified to derive the proposed tapped inductor quasi-Z-source NNPC converter topology. This chapter focuses on the design and development of a 5L-tapped inductor qZS-NNPC converter topology.



(a)



(b)

Figure 4.1: Different versions of the quasi-Z-source converter (a) dual-tapped inductor quasi-Z-source converter. (b) tapped inductor quasi-Z-source converter.

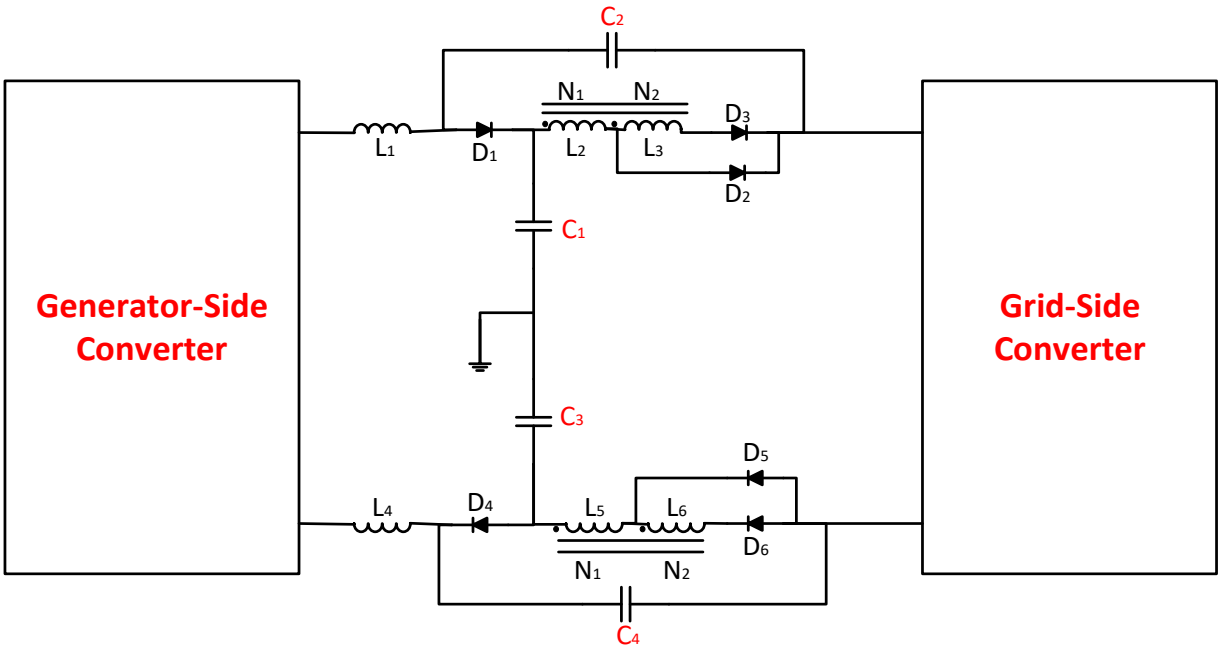


Figure 4.2: Two tapped inductor quasi-impedance source networks in a power conversion stage.

(a) **(b)**

Figure 4.3: Tapped inductor (a) tapped inductor cell. (b) equivalent circuit of the tapped inductor.

4.1.1. Operating Principle

The two tapped inductor quasi-z-source (qZS) network consists of two inductors, two tapped inductor (TI) cells (a TI cell consists of a coupled inductor and two diodes as shown in Figure 4.3(a)), two shoot-through diodes (D_1 and D_4) and four capacitors (C_1, C_2, C_3 and C_4), as shown in Figure 4.2. These tapped inductor quasi-impedance source networks are arranged into a "T-shape" network in the positive and negative rail of the converter topology.

The power conversion stage will operate in two modes, namely, non-shoot-through (NST) mode (which consists of the normal active states and normal zero states) and shoot-through

(ST) mode (boosting state). The two tapped inductor quasi-impedance-source networks are assumed to be symmetrical; hence, the following relationships are derived:

$$L_1 = L_4;\ L_2 + L_3 = L_5 + L_6 \tag{4.1}$$

$$C_2 = C_4;\ C_1 = C_3 \tag{4.2}$$

$$N = N_2/N_1 \tag{4.3}$$

When $D_1 = 1$, $D_4 = 1$ (conducting).

$$V_{in} = V_{L1} + V_{C1} + V_{C3} + V_{L4} \tag{4.4}$$

$$I_{L1} = I_{c1} \tag{4.5}$$

When $D_1 = 0$, $D_4 = 0$ (not conducting).

$$V_{in} = V_{L1} + V_{L4} - V_{C2} - V_{C4} + V_o \tag{4.6}$$

$$I_{L1} = I_{c2};\ I_{L4} = I_{c4};\ \ I_{L5} = I_{c3};\ I_{L2} = I_{c1}; \tag{4.7}$$

When $D_2 = 1$, $D_5 = 1$, while $D_1 = 1$, $D_4 = 1$ (conducting).

$$V_{L2} = -V_{C2};\ V_{L5} = -V_{C4} \tag{4.8}$$

$$I_{D2} = -I_{c2};\ I_{D5} = I_{c4} \tag{4.9}$$

$$I_{D1} = I_{c1} + I_{D2};\ I_{D4} = I_{c1} + I_{D5} \tag{4.10}$$

When $D_2 = 1$, $D_5 = 1$; while $D_1 = 0$, $D_4 = 0$

$$V_{C1} = V_{L2} + V_0;\ V_{C3} = V_{L5} + V_0 \tag{4.11}$$

$$I_{D2} = -I_{c1};\ I_{D5} = -I_{c3} \tag{4.12}$$

When $D_3 = 1$, $D_6 = 1$; while $D_1 = 1$, $D_4 = 1$

$$(1 + 1/N)V_{L3} = -V_{C2};\ (1 + 1/N)V_{L6} = -V_{C4} \tag{4.13}$$

$$I_{D3} = I_{L3} - I_{c2};\ I_{D6} = I_{c4} - I_{L5} \tag{4.14}$$

$$I_{D1} = I_{L1} - I_{c2};\ I_{D4} = I_{L4} - I_{c4} \tag{4.15}$$

When $D_3 = 1$, $D_6 = 1$; while $D_1 = 0$, $D_4 = 0$

$$V_{C1} = (1 + 1/N)V_{L3} + V_0;\ V_{C3} = (1 + 1/N)V_{L6} + V_0 \tag{4.16}$$

$$I_{D3} = -I_{c1};\ I_{D6} = -I_{c3} \tag{4.17}$$

where N_1 is the number of turns of L_2, L_5, and N_2 is the number of turns of L_3, L_6; V_{L1} and I_{L1}, V_{L4} and I_{L4} are the voltage and current of the inductor L_4; V_{L2} and I_{L2}, V_{L5} and I_{L5} are the voltage and current of the primary winding of the tapped inductors L_2 and L_5; V_{L3} and I_{L3}, V_{L6} and I_{L6} are the voltage and current of the secondary winding of the tapped inductors L_3 and L_6; V_{C1} and I_{c1}, V_{C2} and I_{c2}, V_{C3} and I_{c3}, V_{C4} and I_{c4} are the voltages and currents of capacitors $C_1, C_2,\ C_3, C_4$; $I_{D1},\ I_{D2},\ I_{D3},\ I_{D4},\ I_{D5}$ and I_{D6} are the current flowing through diodes $D_1, D_2, D_3, D_4, D_5,$ and D_4; V_o and I_o are the voltage and current of the output point of the converter. A 3ph 5L-tapped inductor qZS-NNPC converter topology is shown in Figure 4.4 below. Table 4.1 shows all the switching states of a 1ph 5L-tapped inductor qZS-NNPC converter topology.

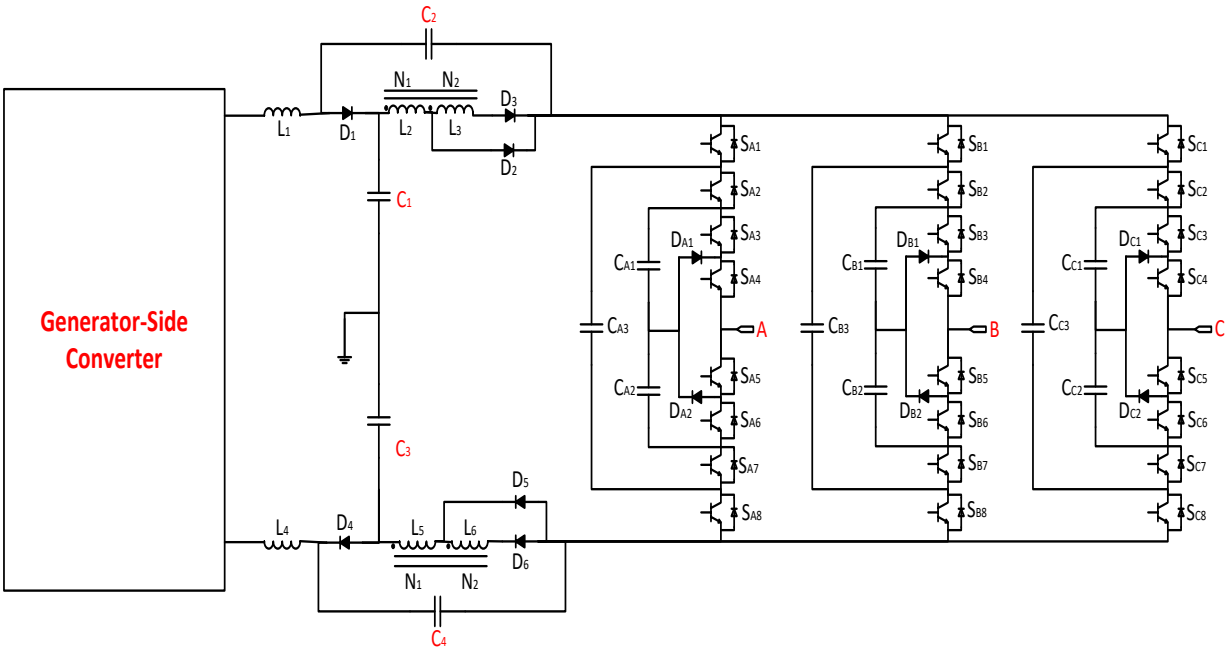


Figure 4.4: 3ph 5L-tapped inductor qZS-NNPC converter topology.

Table 4.1: Switching states of a 5L-tapped inductor qZS-NNPC converter.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{cx1}	V_{cx2}	V_{cx3}	V_{xo}	Switching State	Mode
1	1	1	1	0	0	0	0	N	N	N	$V_{dc}/2$	1	NST
1	1	0	1	1	0	0	0	C	N	N	$V_{dc}/4$	2	NST
0	1	1	1	0	0	0	1	N	N	D	$V_{dc}/4$	2.1	NST
1	0	1	1	0	0	1	0	D	D	C	$V_{dc}/4$	2.2	NST
1	1	0	0	1	1	0	0	C	C	N	0	3	NST
1	0	0	1	1	0	1	0	N	D	C	0	3.1	NST
0	1	0	1	1	0	0	1	C	N	D	0	3.2	NST
0	0	1	1	0	0	1	1	D	D	N	0	3.3	NST
0	0	0	1	1	0	1	1	N	D	N	$-V_{dc}/4$	4	NST
1	0	0	0	1	1	1	0	N	N	C	$-V_{dc}/4$	4.1	NST
0	1	0	0	1	1	0	1	C	C	D	$-V_{dc}/4$	4.2	NST
0	0	0	0	1	1	1	1	N	N	N	$-V_{dc}/2$	5	NST
1	1	1	1	1	1	1	1	N	N	N	0	6	ST

N-No impact; C-Charging; D-Discharging.

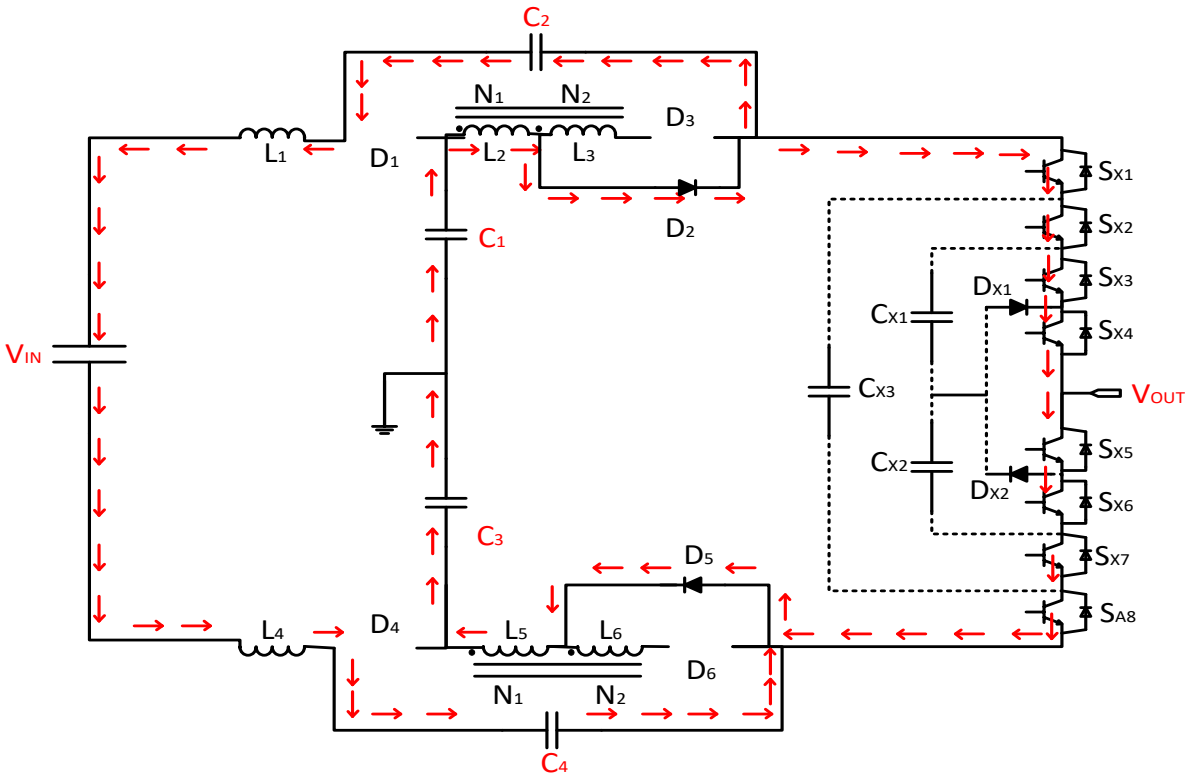
A. Shoot-Through (ST) Mode

In Figure 4.5(a) and Figure 4.5(b), the ST mode of the proposed converter topology is illustrated based on the switching states highlighted in Table 4.1. During the ST mode, the split dc-link of the converter is short-circuited with all the IGBT devices switched ON in a single-phase leg of the topology. The diodes D_1, D_3, D_4 and D_6 are OFF, whereas the diodes D_2 and D_5 are ON. The winding N_1 of inductor L_2 is charged by C_1, while the energy stored in winding N_1 of inductor L_5 is transferred into C_3. Based on Kirchhoff's voltage law (KVL) to the circuit in Figure 4.5(a), the voltage relationship amongst the inductors and capacitors is expressed in (4.18) to (4.20).

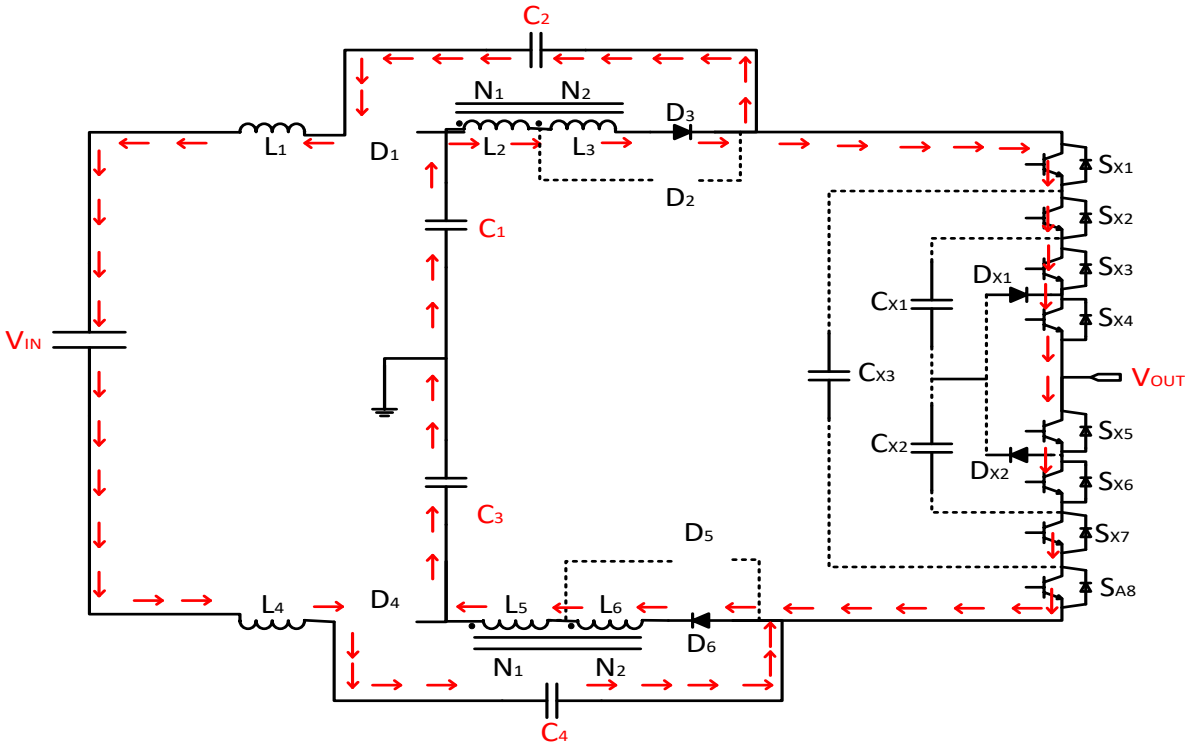
$$V_{L1} + V_{L4} = V_{in} + V_{C2} + V_{C4} \tag{4.18}$$

$$V_{L2} + V_{L5} = V_{C1} + V_{C3} \tag{4.19}$$

$$V_{L3} = NV_{C2};\ V_{L6} = NV_{C4}\ \ (N = 1) \tag{4.20}$$



(a)



(b)

Figure 4.5: Equivalent circuit of a 1ph 5L-tapped inductor qZS-NNPC converter topology at ST mode. (a) Mode A. (b) Mode B.

B. *Non-Shoot-Through (NST) Mode*

The NST mode consists of the normal active states and normal zero states of a conventional 1ph 5L-NNPC converter, as shown in Table 3.2. However, the normal active states and normal zero states of a 1ph 5L-tapped inductor qZS-NNPC converter topology are illustrated in Table 4.1.

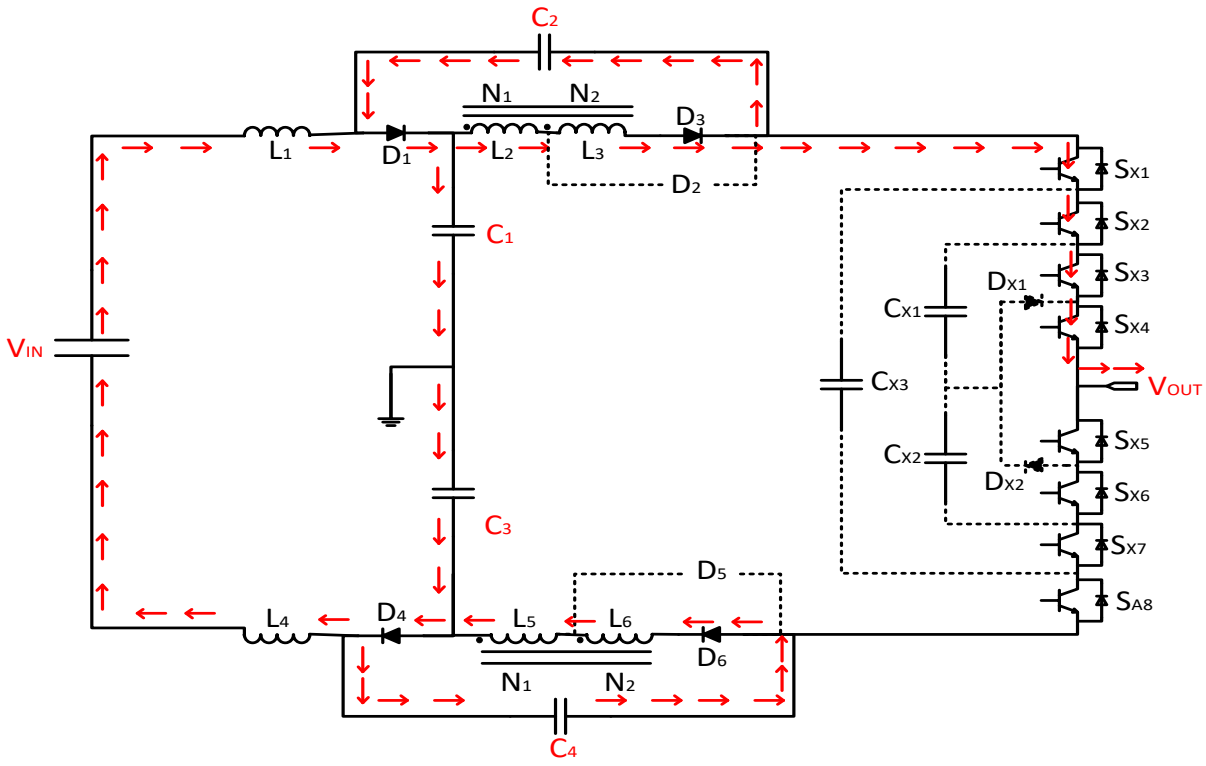
Normal Active States and Normal Zero States

Figure 4.6(a) to 4.6(h), the eight normal active states are highlighted based on Table 4.1. During this state, diodes D_1, D_3, D_4 and D_6 are ON, while the diodes D_2 and D_5 are OFF. Capacitors C_1, C_2, C_3, and C_4 are charged through the inductors, as illustrated in Figures 4.6(a) to 4.6(h). Furthermore, the normal zero states of the converter topology have been presented in Figures 4.7(a) to 4.7(d). Based on KVL, the voltage relationship amongst the inductors and capacitors is expressed in (4.21) to (4.23).

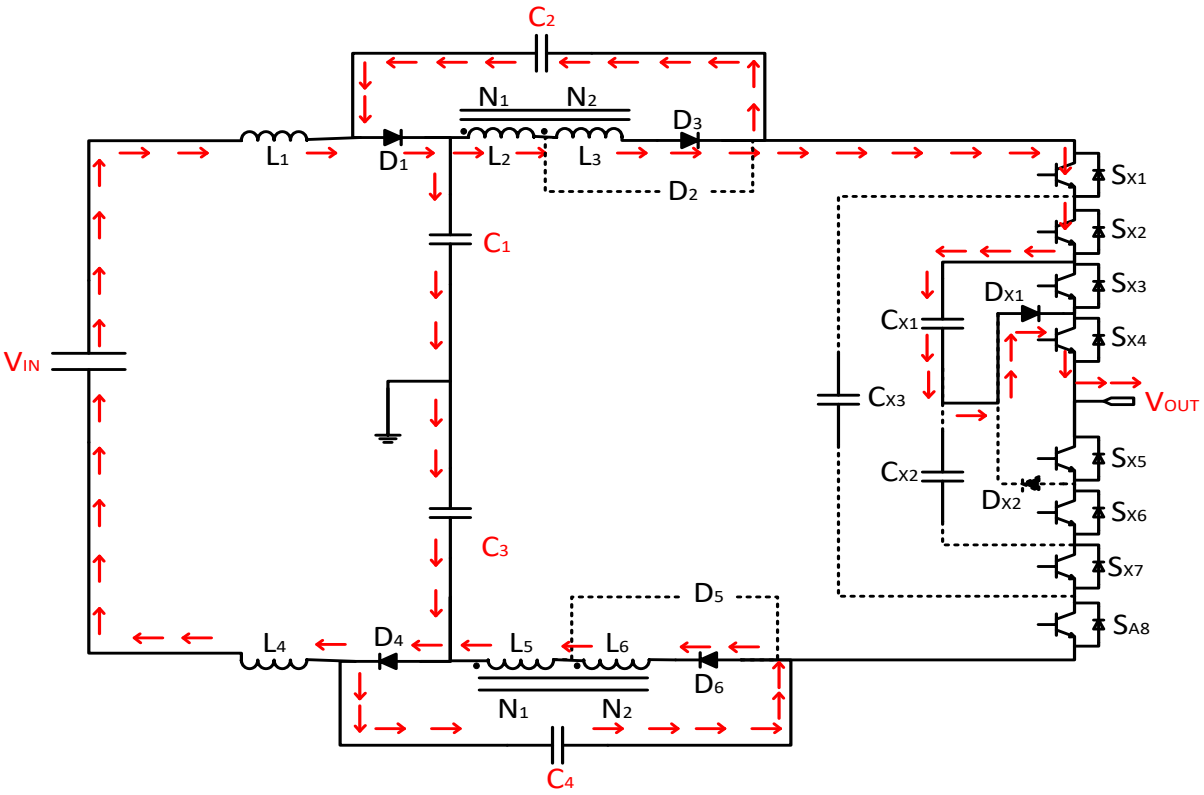
$$V_{in} - (V_{L1} + V_{L4}) = V_{C1} + V_{C3} \tag{4.21}$$

$$V_{L2} + V_{L3} = V_{c2};\ V_{L5} + V_{L6} = V_{C4} \tag{4.22}$$

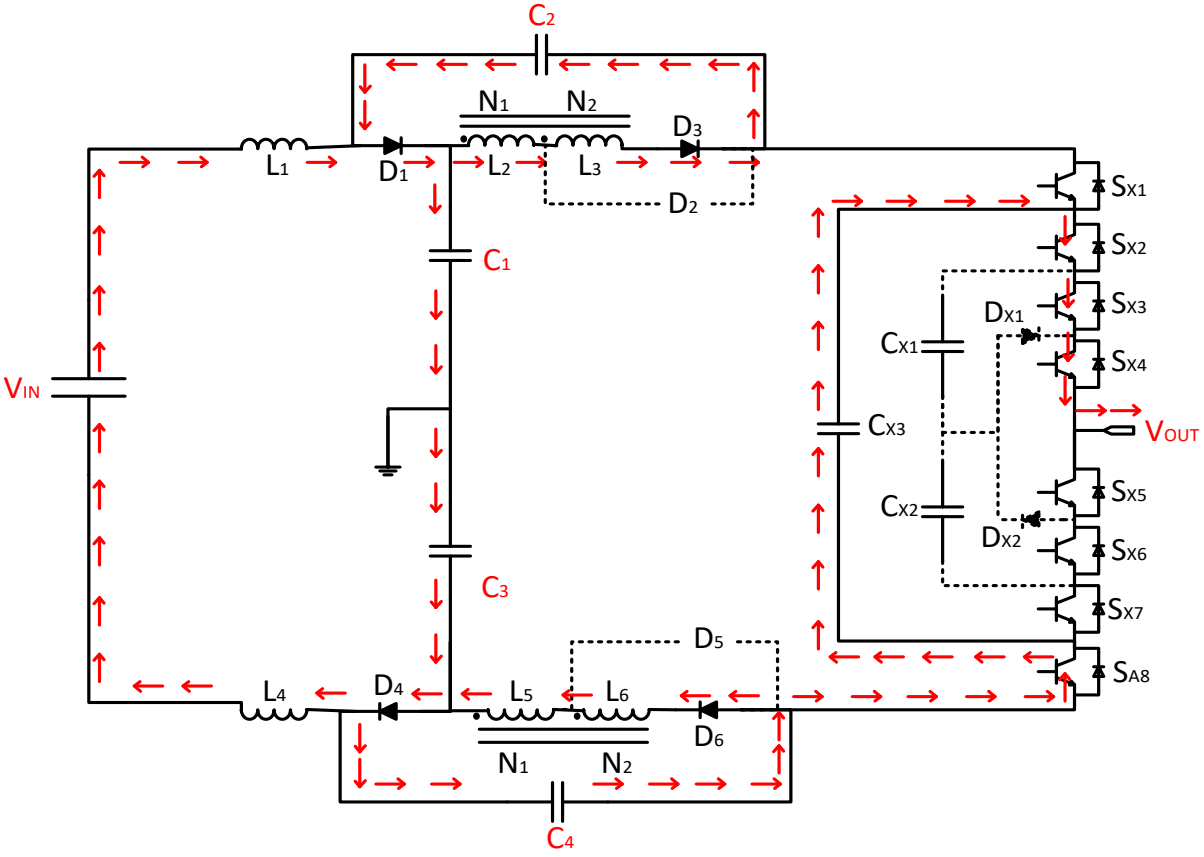
$$V_{dc} = V_{C1} + V_{C3} + V_{C2} + V_{C4} \tag{4.23}$$



(a)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Dx1
Cx1
Sx4
Cx3
VOUT
Cx2
Dx2
Sx5
Sx6
C3
Sx7
D5
SA8
L4
D4
L5
L6
D6
N1
N2
C4

(b)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Dx1
Cx1
Sx4
Cx3
VOUT
Cx2
Dx2
Sx5
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D5
SA8
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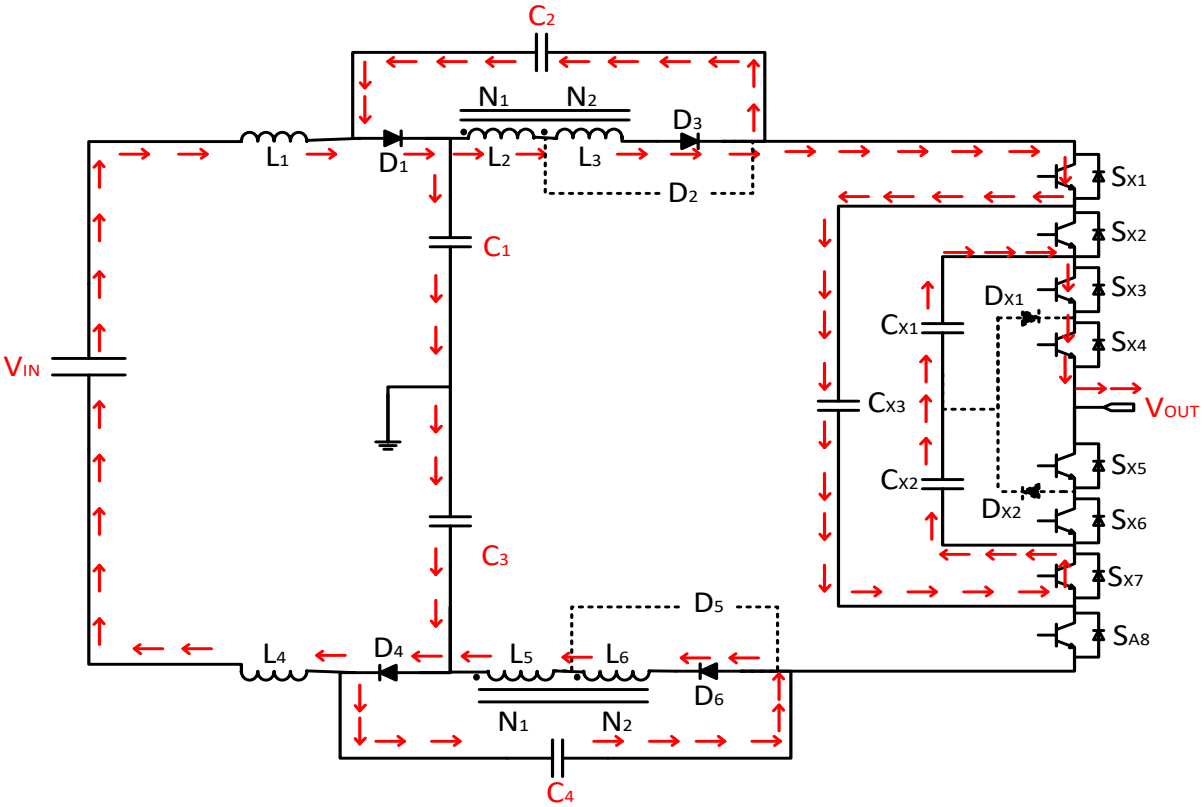
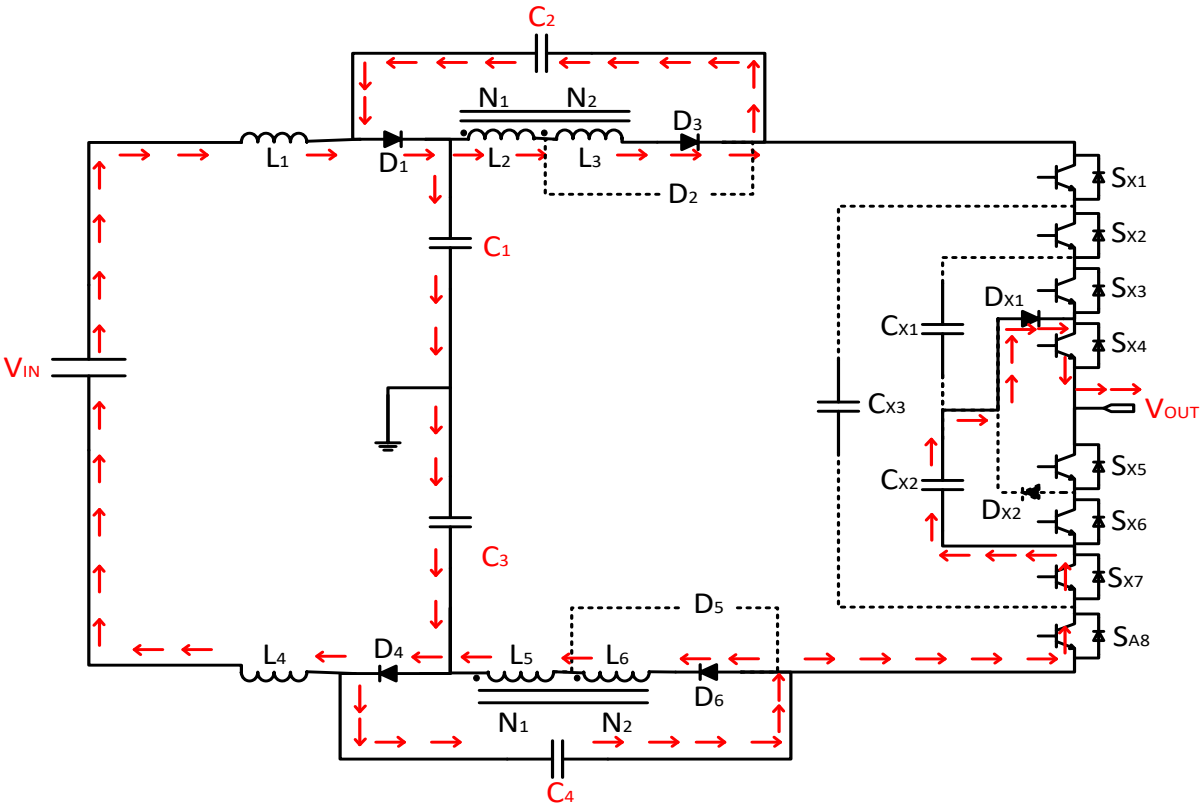
L5
L6
D6
N1
N2
C4

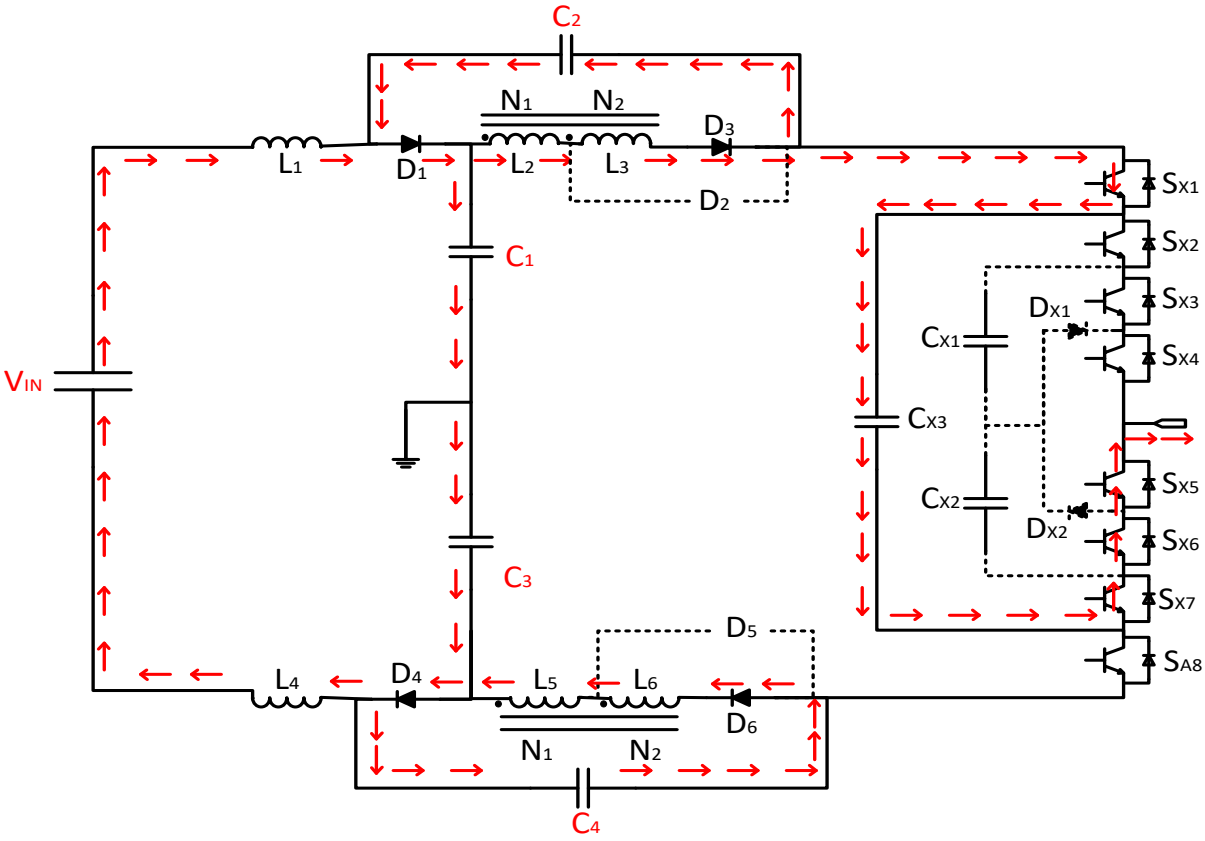
(c)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Sx4
Dx1
Cx1
Cx3
VOUT
Cx2
Dx2
Sx5
Sx6
Sx7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

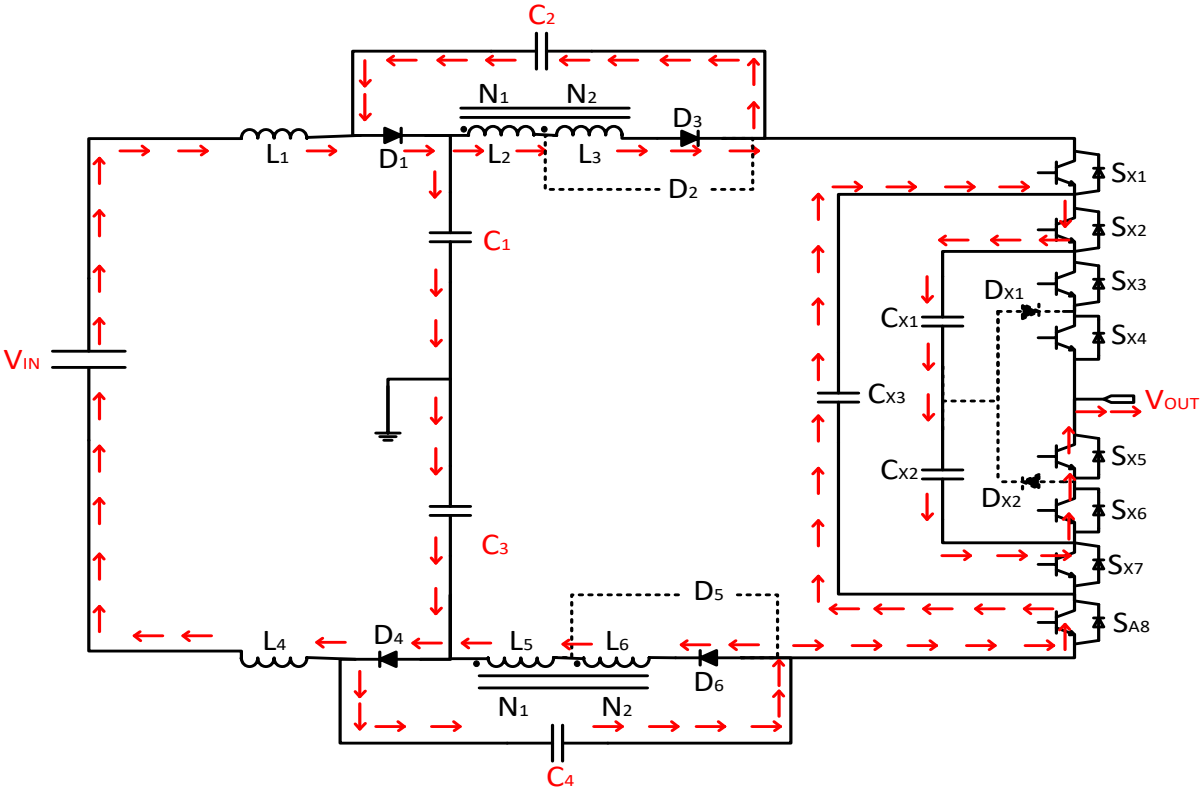
(d)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Sx4
Dx1
Cx1
Cx3
VOUT
Cx2
Dx2
Sx5
Sx6
Sx7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

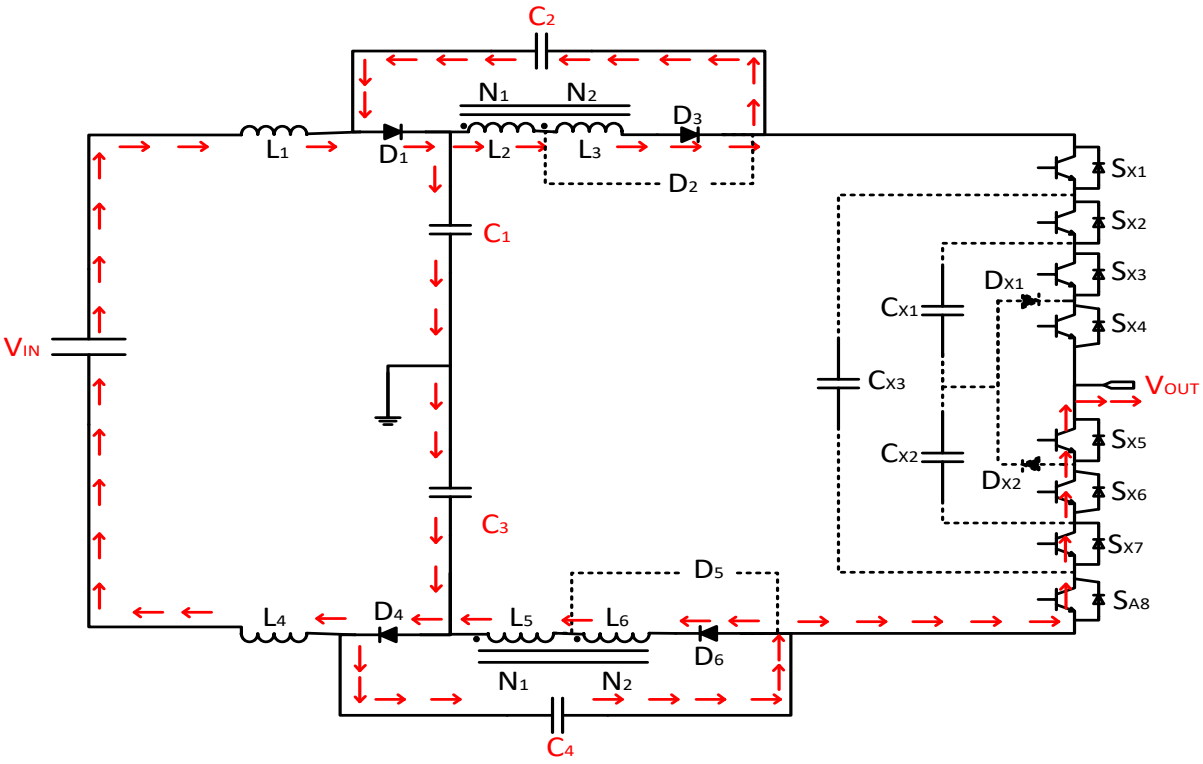
(e)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
SX1
SX2
SX3
SX4
DX1
CX1
CX3
CX2
DX2
SX5
SX6
SX7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

(f)

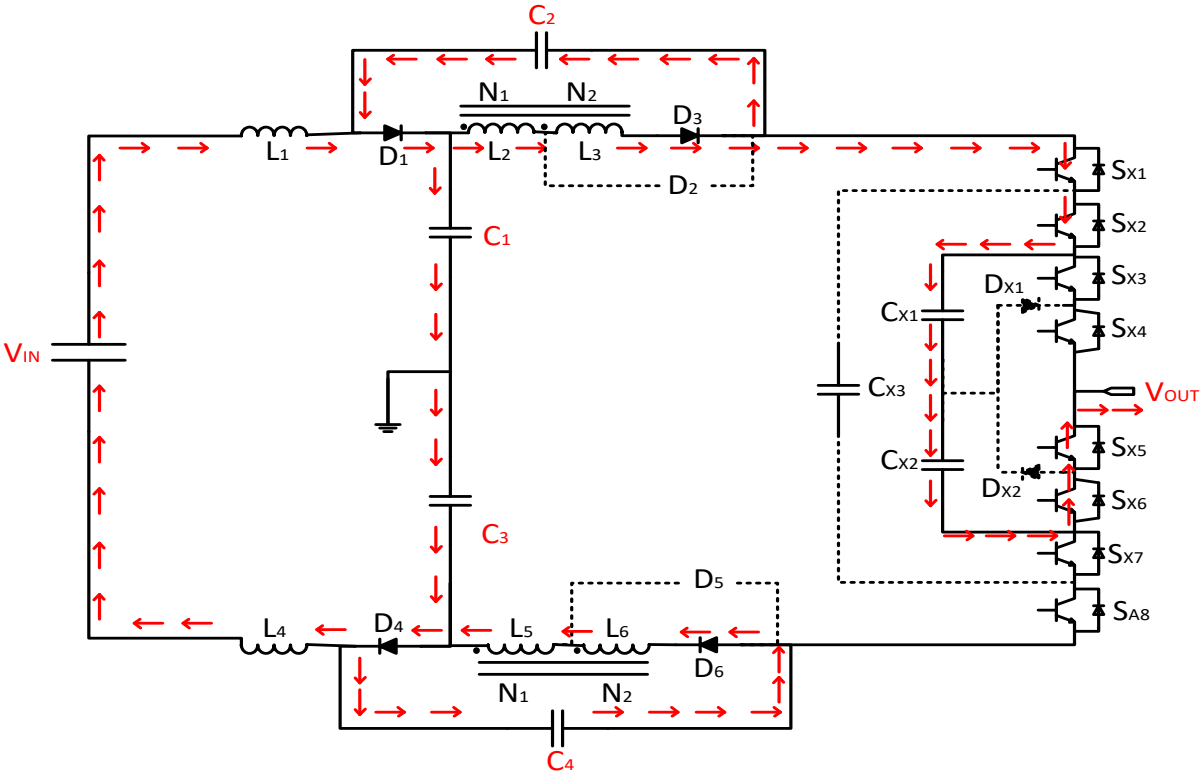

C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
SX1
SX2
SX3
SX4
DX1
CX1
CX3
VOUT
CX2
DX2
SX5
SX6
SX7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

(g)

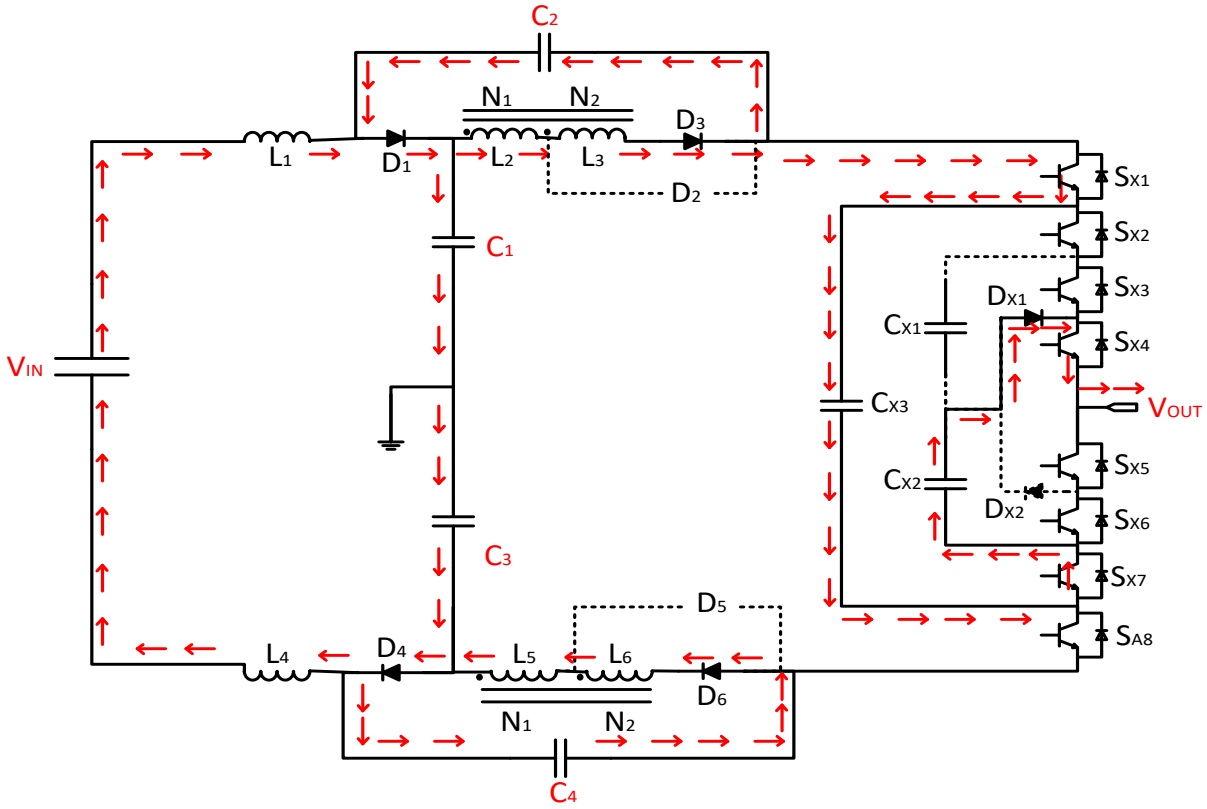


(h)

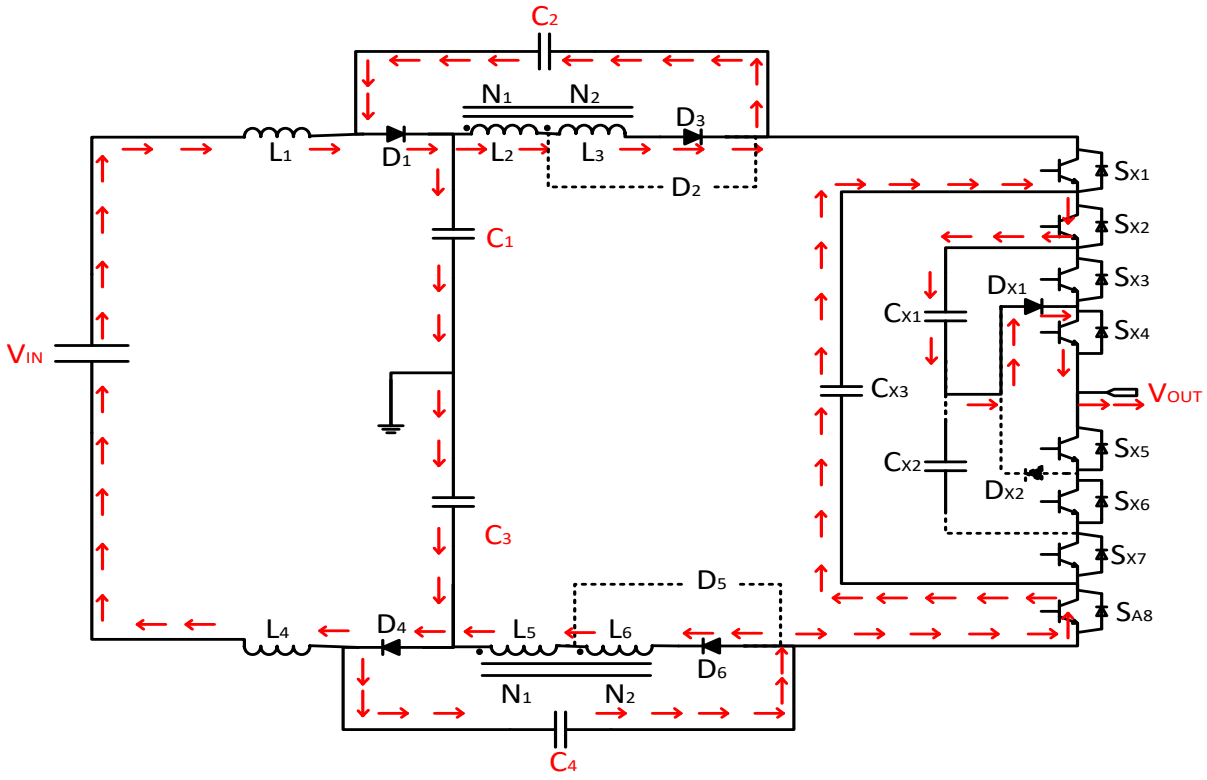
Figure 4.6: Equivalent circuit of a 1ph 5L-tapped inductor qZS-NNPC converter topology at NST mode (normal active states). (a) state 1. (b) state 2. (c) state 2.1. (d) state 2.2. (e) state 4. (f) state 4.1. (g) state 4.2. (h) state 5.



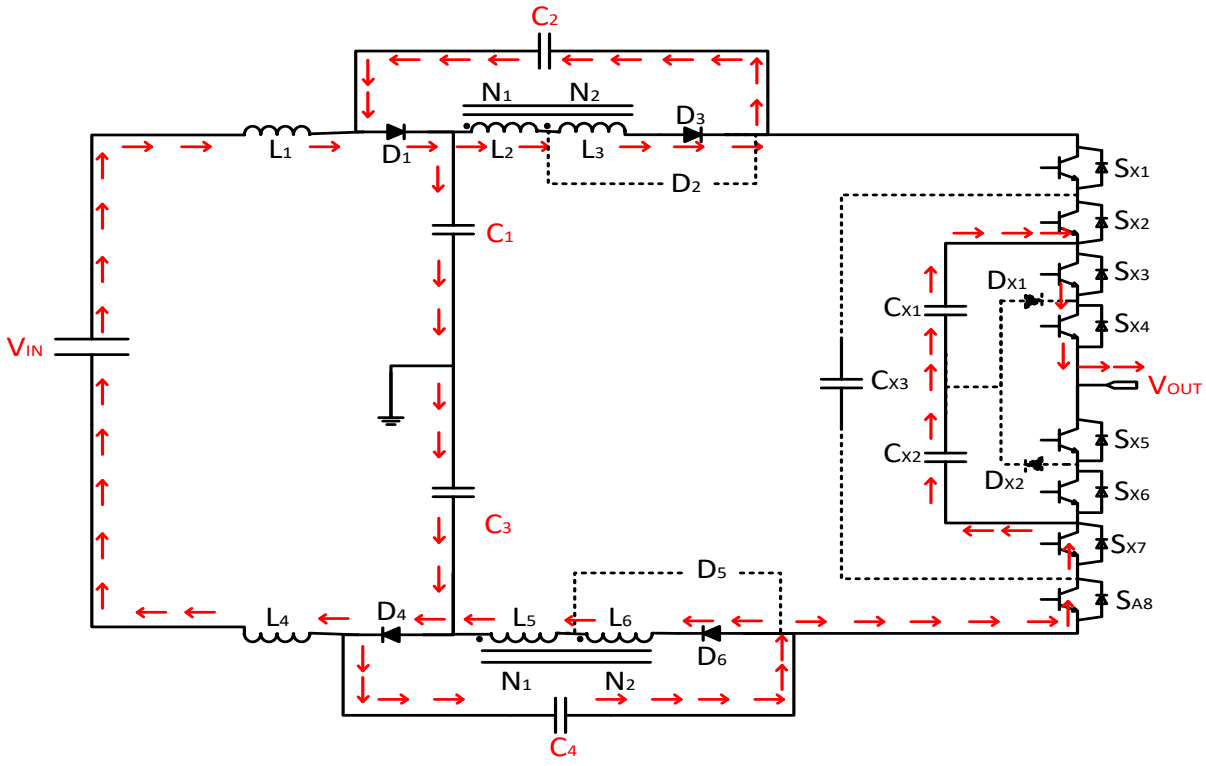
(a)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Sx4
Dx1
Cx1
Cx3
VOUT
Cx2
Dx2
Sx5
Sx6
Sx7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

(b)


C2
N1
N2
D3
L1
D1
L2
L3
D2
C1
VIN
Sx1
Sx2
Sx3
Sx4
Dx1
Cx1
Cx3
VOUT
Cx2
Dx2
Sx5
Sx6
Sx7
SA8
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4

(c)



(d)

Figure 4.7: Equivalent circuit of a 1ph 5L-tapped inductor qZS-NNPC converter topology at NST mode (normal zero states). (a) state 3. (b) state 3.1. (c) state 3.2. (d) state 3.3.

4.1.2. Steady-state Analysis

The output phase voltage of the converter topology has five voltage levels, namely: $B_f \cdot V_{dc}/2$, $B_f \cdot V_{dc}/4$, 0, $-B_f \cdot V_{dc}/4$, $-B_f \cdot V_{dc}/2$, with B_f representing the boost factor of the converter. This steady-state analysis is carried out under the continuous conduction mode (CCM) of the topology (as previously stated in section 4.1). The switching period of the proposed **5L-tapped inductor qZS-NNPC converter topology** is categorized into two switching modes (as expressed in 4.24) and thirteen possible switching states, as illustrated in Table 4.1.

$$T = T_{nst} + T_{st} \tag{4.24}$$

$$\frac{T_{nst}}{T} + \frac{T_{st}}{T} = D_{nst} + D_{st} = 1 \tag{4.25}$$

where T_{nst} is the switching period during the NST mode, T_{sh} is the switching period during the ST mode, D_{nst} is the duty cycle of the NST mode, and D_{st} is the duty cycle of the ST mode.

During the ST mode, C_1 charges the primary winding (N_1) of the tapped inductor L_2 , with the voltage across N_1 defined as stated in (4.26).

$$v_{L2} = V_{C1} \tag{4.26}$$

Furthermore, the leakage inductance of the tapped inductor results in a resonant time interval ($T_r = D_r T$) with C_2 [181]. Therefore, the voltage across N_1 during T_r as stated in (4.27).

$$v_{L2} = V_{C2} \tag{4.27}$$

Following T_r, the winding N_2 reverses its polarity and its in series connection with N_1 [181]. The non-shoot-through time interval $T_{nst} = (1 - D_{st} - D_r)$. Therefore, the voltage across of winding of N_1 can be expressed in (4.28).

$$v_{L2} = V_{C2} - v_{L3} = V_{C2} - Nk^2 v_{L2} \tag{4.28}$$

Therefore,

$$v_{L2} = \frac{V_{C2}}{1+Nk^2} \tag{4.29}$$

The average voltage across N_1 is expressed in (4.30) [181].

$$D_{st}V_{C1} - D_r V_{C2} - (1 - D_{st} - D_r)\frac{V_{C2}}{1+Nk^2} = 0 \tag{4.30}$$

where k is the coupling coefficient, and N is the turn ratio of the tapped inductor.

Therefore, the steady-state analysis assumes that the average voltage across the inductors and average current flowing through the capacitors is equal to zero [181], [182], as expressed in (4.31).

$$\frac{1}{T}\int V_{L1}(t)dt = 0;\ \frac{1}{T}\int i_{C1}(t) = 0 \tag{4.31}$$

The average voltage of the inductor L_1 can be expressed, as stated in (4.32).

$$\frac{1}{T}\int V_{L1}(t)dt = \frac{1}{T}\left(\frac{V_{in}}{2} + V_{C2}\right)T_{st} + \left(\frac{V_{in}}{2} - V_{C1}\right)T_{nst} = 0 \tag{4.32}$$

$$= \left(\frac{V_{in}}{2} + V_{C2}\right)D_{st} + \left(\frac{V_{in}}{2} - V_{C1}\right)(1 - D_{st}) = 0 \tag{4.33}$$

Combining (4.30) and (4.33), the voltage across C_1 and C_2 are obtained as follows.

$$V_{C1} = \frac{V_{in}[D_r Nk^2 + 1 - D_{st}]}{2[Nk^2(-D_{st}^2 + D_r - D_{st}D_r) + 1 - 2D_{st}]} \tag{4.34}$$

$$V_{C2} = \frac{V_{in}[D_{st}+D_{st}Nk^2]}{2[Nk^2(-D_{st}^2+D_r-D_{st}D_r)+1-2D_{st}]} \quad (4.35)$$

$$V_{C1} = V_{C3};\ V_{C2} = V_{C4} \quad (4.36)$$

The boost factor ($B_f = V_{dc}/V_{in}$) can be derived from (4.23), (4.34) to (4.36).

$$B_f = \frac{V_{dc}}{V_{in}} = \frac{V_{C1}+V_{C3}+V_{C2}+V_{C4}}{V_{in}} \quad (4.37)$$

$$B_f = \frac{[D_rNk^2+1+D_{st}Nk^2]}{[Nk^2(-D_{st}^2+D_r-D_{st}D_r)+1-2D_{st}]} \quad (4.38)$$

where,

$$D_r \approx \frac{(Nk^2D_{st}^2+2D_{st}-1)V_{dc}+(Nk^2D_{st}+1)V_{in}}{Nk^2(1-D_{st})V_{dc}-Nk^2V_{in}} \quad (4.39)$$

The resonant duty cycle (D_r) is due to the leakage inductance of the tapped inductor [181]. The tapped inductor is tightly coupled with k being unity ($k = 1$), under this condition D_r is negligible [181]. Therefore, B_f is further simplified, as expressed in (4.40).

$$B_f = \frac{[1+D_{st}N]}{[N(-D_{st}^2)+1-2D_{st}]} \quad (4.40)$$

For the 3ph proposed converter topology shown in Figure 4.4, the phase output voltage is expressed (4.41) [182].

$$V_{out} = m_a \frac{V_{dc}}{2\sqrt{2}} \quad (4.41)$$

where, m_a represents the modulation index; $m_a \leq 1 - D_{st}$ [182]. While (4.41) can be further expanded with (4.40) to obtain (4.42):

$$V_{out} = m_a \frac{V_{dc}}{2\sqrt{2}} = (1 - D_{st}) \frac{[1+D_{st}N]V_{in}}{2\sqrt{2}[N(-D_{st}^2)+1-2D_{st}]} \quad (4.42)$$

Therefore, the voltage gain (G) of the proposed converter topology is expressed in (4.43).

$$G = \frac{V_{out}}{V_{in}} = \frac{(1-D_{st})(1+D_{st}N)}{2\sqrt{2}[N(-D_{st}^2)+1-2D_{st}]} \quad (4.43)$$

Figure 4.8 compares the voltage gain (G) of the proposed converter topology with a conventional qZS converter topology. Also, Figure 4.8 shows that the G increases consistently with an increase in D_{st} from 0.1 to 0.5, while the conventional multilevel qZS converter topology increases from 0.1 to 0.3. After reaching D_{st} of 0.3, the voltage gain of a conventional

multilevel qZS converter topology will reduce and remain constant for the next couple of shoot-through points, as illustrated in Figure 4.8. Furthermore, the proposed converter topology will have a significant increase in its voltage conversion ratio when the turn ratio of the tapped inductors is greater than the unity $(N \geq 1)$.

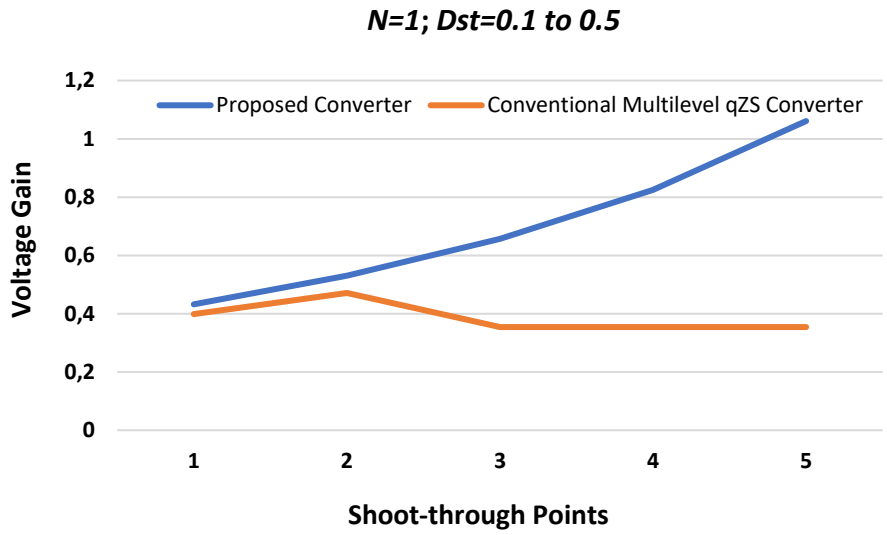


Figure 4.8: Plot of voltage gain *G* versus shoot-through points.

4.2. Design of the tapped inductor quasi-Z-source network

The proposed converter topology has input inductors (L_1 and L_4) connected to the input voltage source (V_{in}) which results in the generation of continuous input current (I_{in}). Therefore, the average inductor current ($\bar{I}_{L1}$) flowing through L_1 is equal to I_{in} [182], [183]. However, the D_{st} interval results in a significant current ripple flowing through the inductors, often estimated to be about 60% peak to peak [183]. The value of current ripple (ΔI_{L1}) flowing through the inductors during the D_{st} interval is obtained using (4.44).

$$\Delta I_{L1} = \int_0^{T_{st}D_{st}} \frac{di_{L1}}{dt} = \int_0^{T_{st}D_{st}} \left(\frac{V_{in} + \bar{V}_{C2} + \bar{V}_{C4}}{2L_1} \right) dt$$

$$= \frac{V_{in}+\bar{V}_{C2}+\bar{V}_{C4}}{2L_1} T_{st} D_{st} \qquad (4.44)$$

The average values of capacitor voltages $\bar{V}_{C1}$, $\bar{V}_{C2}$, $\bar{V}_{C3}$ and $\bar{V}_{C4}$ can be derived from (4.34) to (4.36), under the condition that $k = 1$, as expressed in (4.45) to (4.47).

$$\bar{V}_{C1} = \frac{V_{in}[1-D_{st}]}{2[N(-D_{st}^2)+1-2D_{st}]} \qquad (4.45)$$

$$\bar{V}_{C2} = \frac{V_{in}[D_{st}+D_{st}N]}{2[N(-D_{st}^2)+1-2D_{st}]} \tag{4.46}$$

$$\bar{V}_{C1} = \bar{V}_{C3};\ \bar{V}_{C2} = \bar{V}_{C4} \tag{4.47}$$

Based on the assumption that the power losses associated with the converter are negligible, the instantaneous input power is equal to the rated dc-link power transmitted to the ac-side of the converter [181]-[183], as stated in (4.48).

$$V_{in}\bar{I}_{L1} = V_{dc}I_o(1-D_{st}) = (3/2)V_{out}I_{ac}\cos\varphi \tag{4.48}$$

Therefore, (4.23), (4.45), and (4.46) can be substituted into (4.48) as expressed in (4.49).

$$V_{in}\bar{I}_{L1} = (\bar{V}_{C1}+\bar{V}_{C3}+\bar{V}_{C2}+\bar{V}_{C4})I_o(1-D_{st}) \tag{4.49}$$

$$V_{in}\bar{I}_{L1} = \frac{V_{in}[(1+D_{st}N)(1-D_{st})I_o]}{[N(-D_{st}^2)+1-2D_{st}]} \tag{4.50}$$

Therefore,

$$\bar{I}_{L1}/I_o = \frac{(1+D_{st}N)(1-D_{st})}{[N(-D_{st}^2)+1-2D_{st}]} \tag{4.51}$$

4.2.1. Deriving the Values of the Capacitance and Inductance

Considering the capacitor voltage ripple and average values for C_1 to C_4 and the current flowing through the input inductors L_1 and L_4 are represented as ΔV_{C1}, ΔV_{C2}, ΔV_{C3}, ΔV_{C4}, $\bar{V}_{C1}$, $\bar{V}_{C2}$, $\bar{V}_{C3}$, $\bar{V}_{C4}$, ΔI_{L1}, ΔI_{L4}, $\bar{I}_{L1}$, and $\bar{I}_{L4}$, respectively. Due to the symmetrical nature of the network, the maximum and minimum values of C_1, C_2 and L_1 are derived as follows [181]:

$$V_{C1_{max}} = \bar{V}_{C1} + \Delta V_{C1} = (1+f_{C1})\bar{V}_{C1}$$

$$V_{C2_{max}} = \bar{V}_{C2} + \Delta V_{C2} = (1+f_{C2})\bar{V}_{C2} \tag{4.52}$$

$$I_{L1_{max}} = \bar{I}_{L1} + \Delta I_{L1} = (1+f_{L1})\bar{I}_{L1}$$

$$V_{C1_{max}} = V_{C3_{max}};\ V_{C2_{max}} = V_{C4_{max}};\ I_{L1_{max}} = I_{L4_{max}}$$

$$V_{C1_{min}} = \bar{V}_{C1} - \Delta V_{C1} = (1-f_{C1})\bar{V}_{C1}$$

$$V_{C2_{min}} = \bar{V}_{C2} - \Delta V_{C2} = (1-f_{C2})\bar{V}_{C2} \tag{4.53}$$

$$I_{L1_{min}} = \bar{I}_{L1} - \Delta I_{L1} = (1-f_{L1})\bar{I}_{L1}$$

where $f_{C1} = \Delta V_{C1}/\bar{V}_{C1}$, $f_{C2} = \Delta V_{C2}/\bar{V}_{C2}$, $f_{L1} = \Delta I_{L1}/\bar{I}_{L1}$.

From (4.45) to (4.48), and (4.51) to (4.53), the values of C_1, C_2, C_3, C_4, L_1 and L_4 are derived as follows.

$$C_1 = \frac{[3I_{ac}m_a \cos\varphi]\cdot[(1+D_{st}N)(1-D_{st})]T_{st}}{2(f_{C1})(1-D_{st})V_{in}} \tag{4.54}$$

$$C_2 = \frac{[3I_{ac}m_a \cos\varphi]\cdot[(1+D_{st}N)(D_{st})]T_{st}}{2(f_{C2})[((1+N)D_{st})V_{in}]} \tag{4.55}$$

$$L_1 = \frac{2[(D_{st}-2N{D_{st}}^2)](1-D_{st})T_{st}V_{in}}{[3I_{ac}m_a \cos\varphi f_{L1}]\cdot[(1+D_{st}N)(1-D_{st})]} \tag{4.56}$$

$$C_1 = C_3;\ C_2 = C_4$$

$$L_1 = L_4$$

The primary side of the tapped inductor L_2 with winding N_1 can be expressed as follows.

$$L_2 = \frac{V_{L2}\Delta t}{I_{2max}-I_{2min}} \tag{4.57}$$

During ST mode, v_{L2} is equal to V_{C1} as stated in (4.26), therefore (4.57) can be expressed as follows.

$$L_2 = \frac{V_{C1}\Delta t}{I_{2max}-I_{2min}} = \frac{V_{in}[1-D_{st}]}{2[N(-D_{st}^2)+1-2D_{st}]} \cdot \frac{T_{st}D_{st}}{I_{2max}-I_{2min}} \tag{4.58}$$

Values of the quasi-Z-source network components obtained from the set equations above are summarized in Table 4.2.

Table 4.2: Values of tapped inductor quasi-Z-source network

Symbol	Description	Value
V_{in}	Input voltage	$100V$
$I_{in} = I_{L1}$	Input current	$5A$
$L_1 = L_4$	Input inductor	$88\mu H$
$L_2 + L_3 = L_5 + L_6$	Coupled inductor	$31.74\mu H$
$C_1 = C_3$	Capacitance C_1 & C_3	$243.2\mu F$
$C_2 = C_4$	Capacitance C_2 & C_4	$270.3\mu F$
$\bar{V}_{C1} = \bar{V}_{C3}$	Voltage across C_1 & C_3	$55.6V$
$\bar{V}_{C2} = \bar{V}_{C4}$	Voltage across C_2 & C_4	$12.4V$
ΔI_{L1}	Ripple current through L_1	$3A$

4.2.2. Inductor and Tapped Inductor Design

This section presents the step-by-step process for the input inductor and tapped inductor design based on area-product (A_p) method [184]-[186], as illustrated in Figure 4.9. Therefore, the analytical expressions presented are computed using a developed MATLAB program found in Appendix B.4.

A. Specification

The inductance value (L_1), rated peak current (I_{pk}), rated DC (I_{dc}), rated RMS current (I_{rms}), phase current (I_{ac}) and switching frequency (f_{sw}) are obtained from the operation of the proposed converter topology as discussed in the previous section. Furthermore, the maximum surface temperature and maximum ambient temperature are based on established values [76]. The window utilization factor (k_u) is within the range of 0.2 to 0.8, the selected normalized k_u ($k_u = 0.4$) is based on the standard wire insulation, wire fill factor, effective window area, insulation between winding, and quality [184]. The values of these parameters are summarized in Table 4.3.

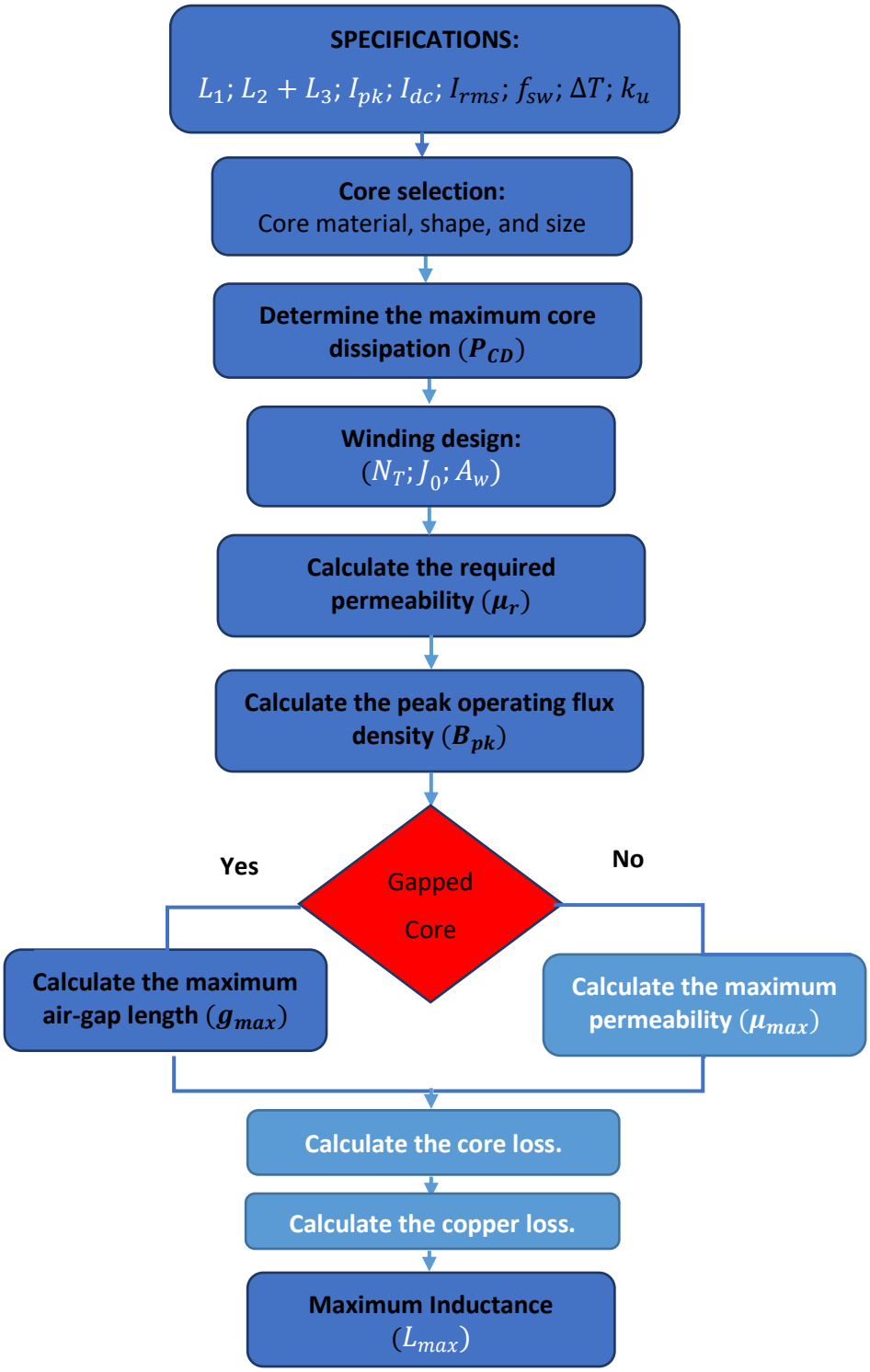


Figure 4.9: Inductor and tapped inductor design flowchart.

Table 4.3: Specifications of the inductor and tapped inductor design.

Symbol	Description	Value
L_1	Input inductor	$88\mu H$
$L_2 + L_3$	Coupled inductor	$31.74\mu H$
$I_{pk} = I_{L1} + \frac{I_{ac}}{2}$	Rate peak current	$6.83A$
I_{rms}	Rate rms current	$5.7A$
I_{ac}	Phase current	$2.73A$
f_{sw}	Switching frequency	$5kHz$
T_s	Maximum surface temperature	100℃
T_a	Maximum ambient temperature	40℃
k_u	Window utilization factor	0.8

B. Core Selection

The maximum stored energy in the inductor resulting from the dc and ac currents is obtained (4.59).

$$E = 1/2\,(LI_{pk}{}^2) \tag{4.59}$$

Therefore, the core size is selected based on the estimated stored energy [76]. Afterwards, the choice of core material utilized for the inductor and the tapped inductor is determined based on loss performance, cost, operating frequency, and tensile strength [76], [187], [188]. The properties of various core materials are highlighted in Table 4.4. The ferrites are suitable for cores operating at high frequencies due to low eddy current loss [76]. However, its low flux density and brittleness are major drawbacks [76], [188]. An amorphous alloy – 2605SC has a much higher flux density than a ferrite core, but its high sensitivity to mechanical stress and cost is a significant disadvantage [188]. A nanocrystalline alloy provides the highest loss performance, but it is the most expensive magnetic material [187], [188]. On the other hand, the grain-oriented silicon steel has very high flux density, low noise, low cost, and relatively good loss performance [187], [188]., making it a suitable choice for the inductor and tapped inductor as stated in Table 4.4.

Table 4.4: Core material properties [187]

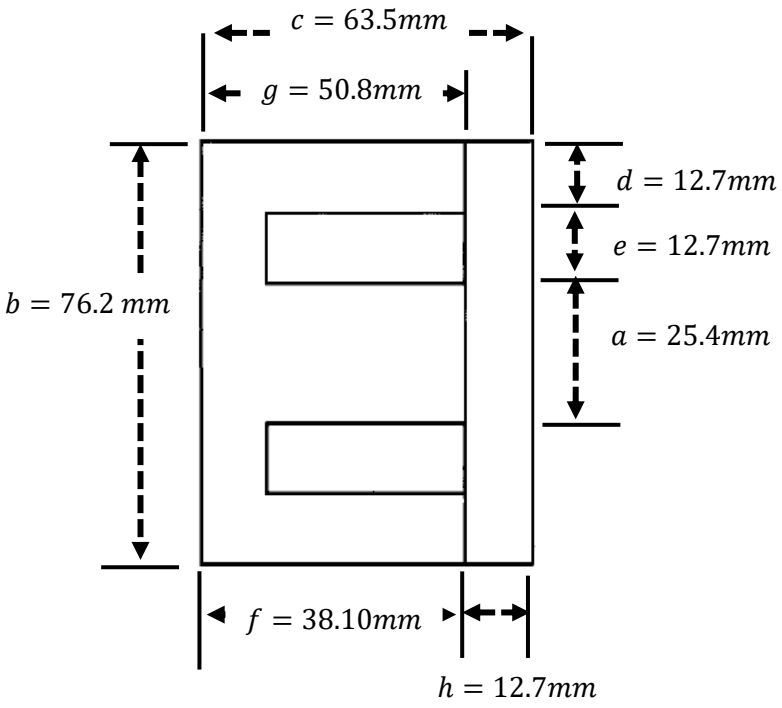
Material Name	Composition	Flux density (T)	Permeability (μ_i)	Operating Frequency (Hz)	Cost
Silicon steel	3-97 SiFe	$1.5-1.8$	1500	$50-5k$	Low
Ferrite	MnZn	$0.3-0.5$	$0.75-15k$	$10k-2M$	Low
Ferrite	NiZn	$0.3-0.4$	$0.2-1.5k$	$0.2M-100M$	Low
Amorphous	2605SC	$1.5-1.6$	1500	$250k$	Medium
Amorphous	2714A	$0.5-6.5$	20000	$250k$	High
Amorphous	Nanocrystalline	$1.0-1.2$	30000	$250k$	High

The calculated value of A_P determines the core by connecting its parameters obtained from the core manufacturers database with the magnetic and electrical parameters [184]-[186]. Therefore, A_P is obtained using (4.60) [186].

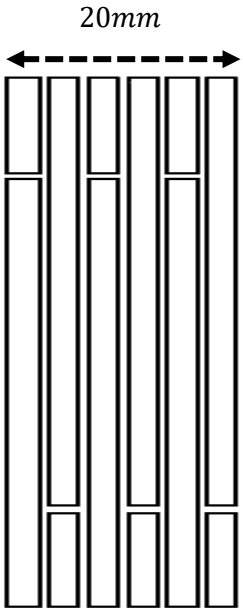
$$A_P = \left[\frac{LI_{pk}{}^2}{B_m K_t \sqrt{k_u (T_s - T_a)}}\right]^{8/7} \times 10^8 \tag{4.60}$$

where L is the calculated inductance value, I_{pk} is the peak current, B_m is the maximum operating flux density ($B_m = 1.5T$), K_t is a dimensionless constant given as 4.82×10^3, k_u is the window utilization factor, and $(T_s - T_a)$ is the temperature change between maximum surface temperature and maximum ambient temperature. Therefore, the core specification obtained from the manufacturers' database presented in [184] are as follows; effective cross-section (A_c), window winding area (W_a), mean length turn (MLT), magnetic path length (MPL) and the core volume (V_c).

Based on the calculated value of A_P, EI-76 lamination is suitable for the inductor and tapped inductor, as discussed previously [184]. The lamination dimension and stacking arrangement are shown in Figures 4.10(a) and 4.10(b), respectively. Furthermore, an interleave one-by-one stacking arrangement is utilized in the lamination to improve the overall permeability [188], as shown in Figure 4.10(b).



(a)



(b)

Figure 4.10: EI lamination. (a) outline with dimensions, (b) stacking arrangement.

C. Maximum Core Dissipation ($\boldsymbol{P_{CD}}$)

The maximum core dissipation (P_{CD}) is based on the value of the core thermal resistance ($R_{C\theta}$) which conforms to both the maximum surface temperature (T_s) and ambient temperature (T_a). The value of $R_{C\theta}$ have been provided on the core datasheet found in Appendix D.1. Therefore, P_{CD} is obtained from (4.61) [186].

$$P_{CD} = \frac{(T_s - T_a)}{R_{C\theta}} \tag{4.61}$$

D. Winding Design

The three main parameters required for the winding design are current density (J_o), wire selection, and number of turns (N_T) [184], [186]. The inductor and tapped inductor winding design are based on solid round winding, which resists the current stress attributed to the current density [185]. The current density determines the wire size of the winding and the RMS current (I_{rms}) flowing through the winding. Therefore, the value of J_o is obtained as given in (4.62) [184], [186].

$$J_o = K_t \cdot \frac{\sqrt{(T_s - T_a)}}{\sqrt{k_u} \cdot \sqrt[8]{A_P}} \times 10^{-4} \tag{4.62}$$

The required cross-sectional area of the wire (A_w) is obtained using (4.63).

$$A_w = \frac{I_{rms}}{J_o} \tag{4.63}$$

Therefore, the wire selected based on the calculated A_w is obtained from the wire table in [184]. The solid round wire is chosen for the inductor winding design [184]-[186]. Afterwards, the effective window area W_e is then determined based on the product of the effective window (S_w) and window area (W_a) as expressed in (4.64) [184].

$$W_e = S_w \cdot W_a \tag{4.64}$$

The value of W_a is selected from the core specification obtained from A_P in step 2, as previously stated [184]. Furthermore, a typical value for S_w with a single bobbin (as utilized in the presented inductor design) is 0.75 [184]. Hence, the number of turns (N_T) is obtained from the (4.65) as stated in [184], [186]:

$$N_T = \frac{W_e \cdot S_f}{A_w} \tag{4.65}$$

where S_f is the fill factor of the windings with a typical value of 0.6 [184].

E. Required Permeability ($\boldsymbol{\mu_r}$)

The selected core parameters determine the value of the required permeability (μ_r) as expressed in (4.66) [184].

$$\mu_r = \frac{B_m(MPL)}{0.4\pi W_a J_o k_u} \times 10^4 \tag{4.66}$$

F. Peak Flux Density ($\boldsymbol{B_{pk}}$)

The maximum values of the direct current flux density (B_{dc}) and alternating current flux density (B_{ac}) must be obtained to ensure that the selected core is operating below its saturation point [186]. In case the value of B_{pk} exceeds B_m, an air gap is included in the core [184]-[186]. However, the value of B_{pk} for both inductor and tapped inductor designs are less than B_m as stated in Table 4.5. The expression for deriving air gap length has been presented in [184] and [186], respectively. The value of B_{pk} is obtained using (4.67) [184].

$$B_{pk} = \frac{0.4\pi N_T\left(I_{dc}+\frac{Iac}{2}\right)\mu_r}{MPL} \times 10^{-4} \tag{4.67}$$

G. Maximum Permeability ($\boldsymbol{\mu_{max}}$)

The selected core operates at a flux density less than B_m, which implies that the μ_{max} should be greater than μ_r to prevent overheating [186]. Thus, the value of μ_{max} is obtained using (4.68).

$$\mu_{max} = \frac{{B_m}^2(MPL)A_c}{\mu_o L {I_{pk}}^2} \tag{4.68}$$

where μ_o is the permeability of free space.

H. Core Loss

The flux density swing (ΔB) of the inductor is calculated using Faraday's law [186] by modifying (4.44) as expressed in (4.69).

$$\Delta B = \frac{V_{in}+\bar{V}_{C2}+\bar{V}_{C4}}{2N_T A_c} T_{st} D_{st} \tag{4.69}$$

Based on the Steinmetz empirical equation presented in [184]-[186], half of the flux density swing B_{cm} is $\Delta B/2$, and the core loss is expressed in (4.70).

$$P_{fe} = V_c K_c f^{\alpha} {B_{cm}}^{\beta} \tag{4.70}$$

where V_c is the core volume, K_c is the loss coefficient, f is the switching frequency, α and β are the Steinmetz empirical coefficients stated in [186].

I. Copper Loss

First, the winding resistance (R_w) is calculated based on (4.71) as stated in [184]. Therefore, the associated copper loss (P_{cu}) is calculated using (4.72) [184]-[186].

$$R_w = (MLT)(N_T)\left(\frac{\mu\Omega}{cm}\right)(10^{-6}) \tag{4.71}$$

$$P_{cu} = {I_{rms}}^2 R_w \tag{4.72}$$

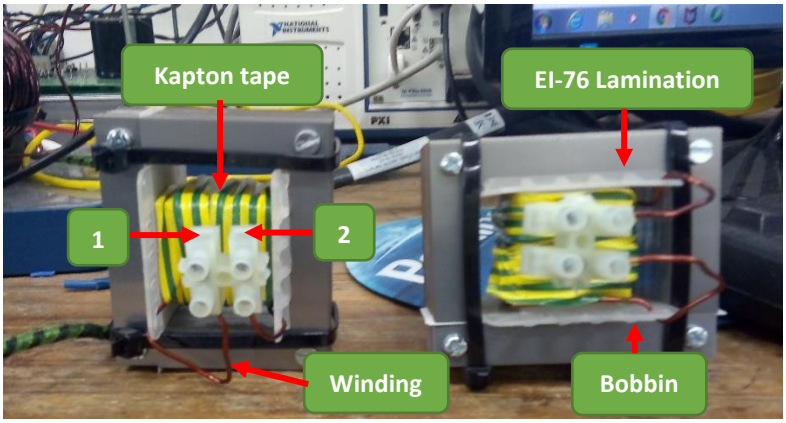
where $\frac{\mu\Omega}{cm}$ is the micro-ohms per centimetre of the solid round wire.

J. Maximum Inductance $(\boldsymbol{L_{max}})$

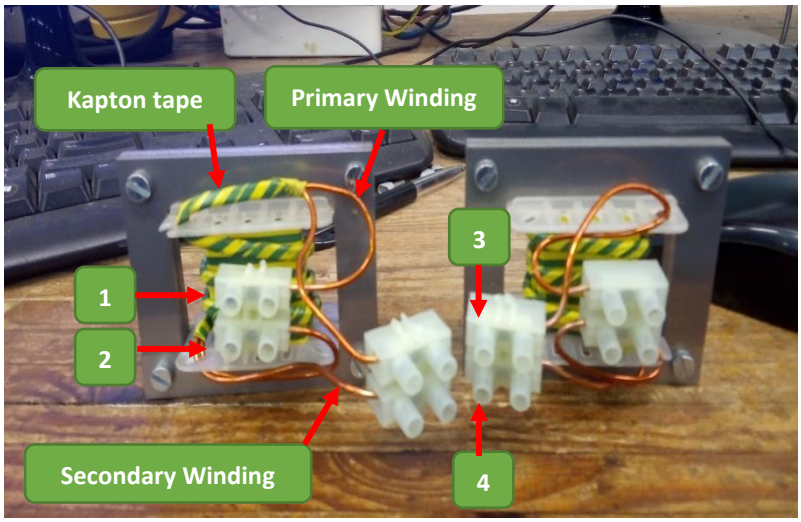
From the steps highlighted previously, the value of the calculated inductance value is less than the measured maximum value (L_{max}) as stated in Table 4.5. While the value of L_{max} can be reduced by either inserting an air gap in the core or decreasing the number of turns [76]. The first approach will reduce core loss while the copper loss will become significant [186]. On the other hand, decreasing the number of turns will reduce the copper weight and volume resulting in a substantial core dissipation [76]. Based on the highlighted drawbacks, the final value of the input inductors and tapped inductors are stated in Table 4.5 and the structure shown in Figure 4.11.

Table 4.5: Inductor design parameters

Inductor Type	Parameter	Calculated Value	Measured Value
Input inductor	L_1, L_4	$88\mu H$	$98.2\mu H$
	B_{pk}	$0.578T$	$0.639T$
	N_T	5	5
Tapped inductor	$L_2 + L_3, L_5 + L_6$	$31.74\mu H$	$35.4\mu H$
	B_{pk}	$0.332T$	$0.384T$
	$N_{T,p} = N_{T,S}$	3	3



(a)



(b)

Figure 4.11: Structure of inductor and tapped inductor. (a) input inductor hardware. (b) tapped inductor hardware.

4.3. Modulation and Voltage Balancing Control Technique

This section presents a modified phase-shifted pulse-width modulation technique that enables the even distribution of the ST modes in the **5L-tapped inductor qZS-NNPC converter topology**. The additional switching state that highlights the operating principle of the ST mode has been presented in Table 4.1. Furthermore, a voltage balancing control technique for maintaining the clamping capacitor voltages in the proposed converter topology has been given. Both methods are implemented on a field-programmable gate array (FPGA)-based platform within the hardware-in-loop experimental configuration described in Chapter 6.

4.3.1. Modulation Technique

The modulation technique used in the proposed converter topology is a phase-shifted sinusoidal PWM (PS-PWM) algorithm. However, due to the tapped inductor quasi-Z-source network in the proposed converter, a shoot-through modulation reference is inserted into an additional zero state, as highlighted in Table 4.1. Therefore, this modulation technique consists of three sinusoidal modulation waveforms for each phase of the topology and four high-frequency carrier waveforms phase-shifted at 90^0 between each other [189], [190]. The shoot-through modulation references (ST_p and ST_n) are represented by two straight lines at the upper and lower points of the PS-PWM technique, as shown in Figure 4.12.

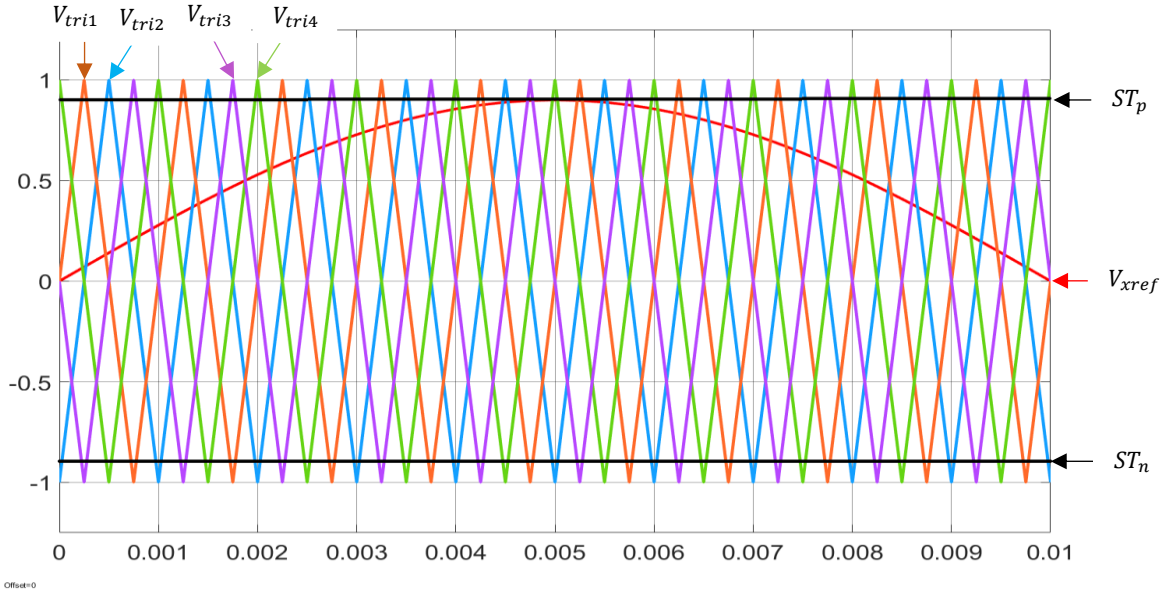


Figure 4.12: Simulated modified PS-PWM technique.

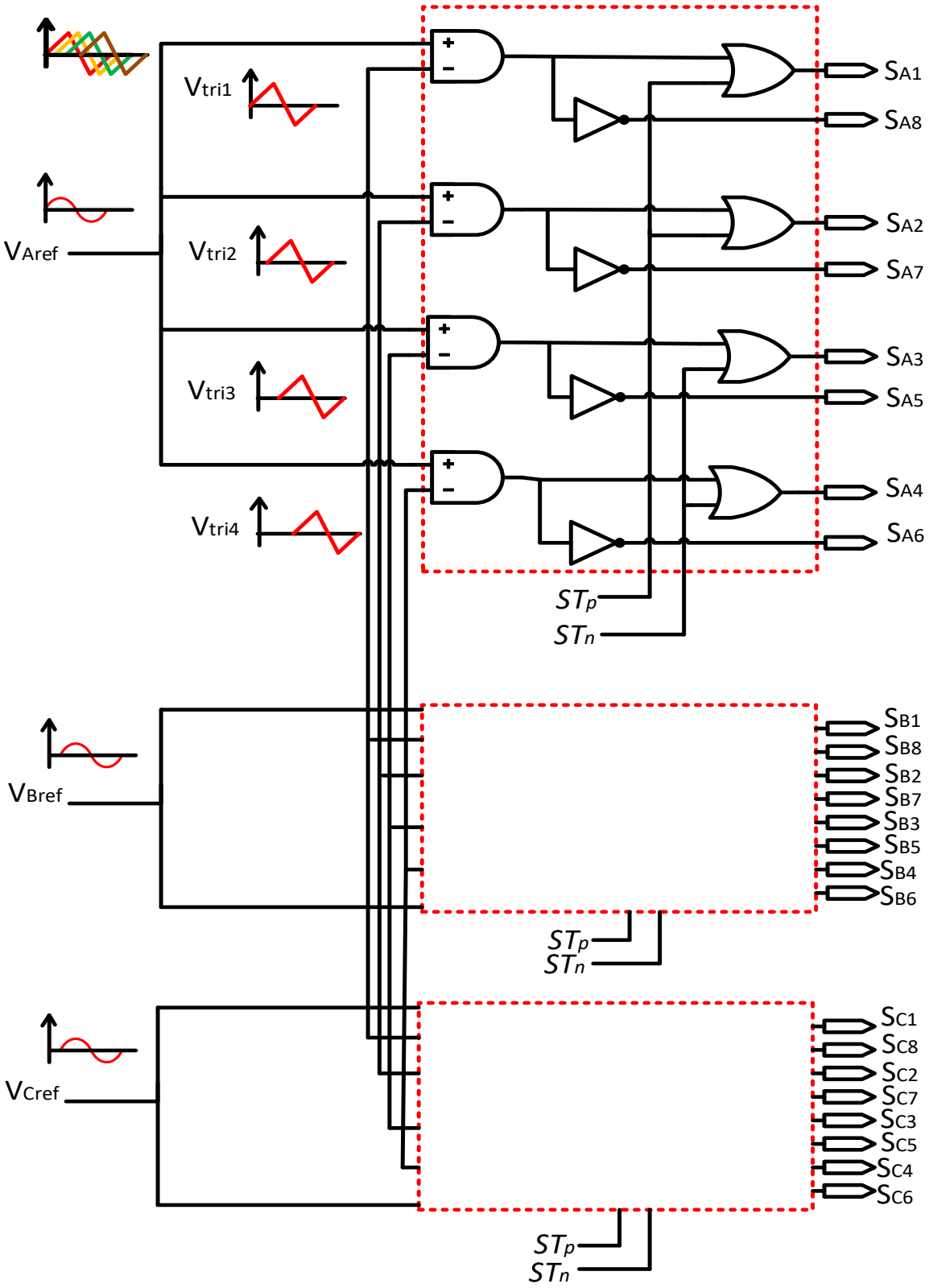
Three sinusoidal modulating signals per phase $(V_{xref}; where\ x\ is\ a, b, c)$ and four triangular carrier signals $(V_{tri1}, V_{tri2}, V_{tri3}, V_{tri4})$ are compared to activate the different switching states within the NST mode, as illustrated in Table 4.1. Based on this operation, the five voltage levels (i.e., $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$) of the proposed converter topology are obtained. The shoot-through modulation references ST_p and ST_n are used to generate the shoot-through states within the ST mode of the proposed converter topology. Therefore, evenly distributed shoot-through states with constant width are obtained throughout the output voltage waveform. Furthermore, the addition of the shoot-through states results in the modification output phase voltage which results in a slight change in the volt-second average because the shoot-through states are not introduced during the normal zero states [190]. Therefore, minimizing the change

in the volt-second average and ascertaining the reference state, the normal active and normal zero states are reconfigured by shifting the interleaved carriers by half of the D_{st}. This implies that each phase of the proposed converter topology applies half of the dc-link voltage more times during the positive and negative half-cycles during normal operation [190].

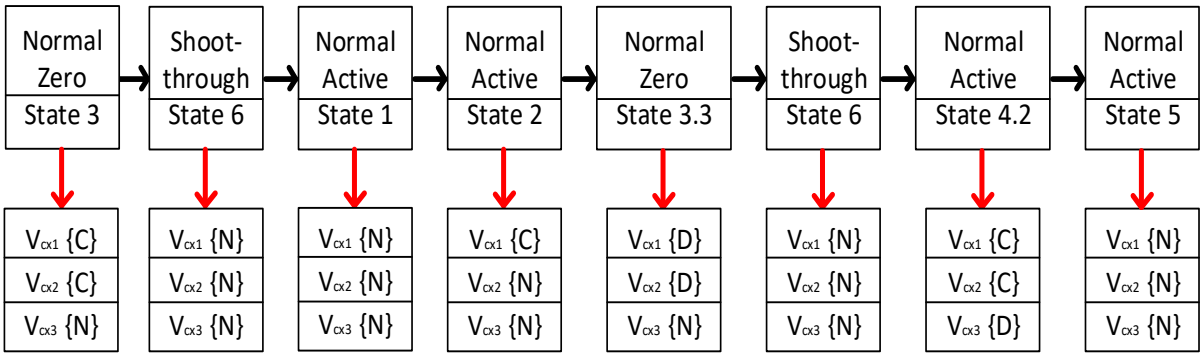
Figure 4.13(a) shows the logic circuit of the modified PS-PWM strategy of the proposed converter topology. The positive and negative shoot-through modulation references ST_p and ST_n are obtained from the three-phase modulating signals. The normal active states and normal zero states are generated by comparing the modulating signal with a carrier signal. While the pulse-width modulation (PWM) signals for the shoot-through state are generated by comparing the either the shoot-through modulation reference (ST_p) or shoot-through modulation reference (ST_n) and a carrier signal (i.e., V_{tri1}). Furthermore, the shoot-through state (i.e., State 6 as presented in Table 4.1) is an additional zero state that is inserted after the normal zero state as illustrated in Figure 4.13(b). The switching pattern is based on considerations of the natural switching states of the proposed converter topology.

According to Table 4.1, each switching state have a direct impact on the clamping capacitor voltages. Based on the nature of the proposed converter topology, the switching pattern of the converter was developed as shown in Figure 4.13(b). The switching pattern begins with a normal zero state (i.e., State 3) with the clamping capacitor voltages (V_{cx1} & V_{cx2}) charging and V_{cx3} remaining constant. Afterwards, the shoot-through state (i.e., State 6) is inserted in the switching pattern with no impact on the clamping capacitor voltages. During the shoot-through state, the boost mode of the converter topology is activated, the normal active state (i.e., State 1) is inserted into the switching pattern with no impact on the clamping capacitor voltage, as shown in Figure 4.13(b). This is closely followed by another normal active state (i.e., State 2) with the clamping capacitor voltage (V_{cx1}) being charged and clamping capacitor voltages (V_{cx2} & V_{cx3}) remain constant. Then, the switching interval of another normal zero state (i.e., State 3.3) with the clamping capacitor voltages (V_{cx1} & V_{cx2}) discharging and V_{cx3} remaining constant. Also, the shoot-through state (i.e., State 6) is inserted in the switching pattern, due to the slight build in the clamping capacitor voltage (V_{cx3}). Therefore, a switching state that ensures the discharging of the clamping capacitor voltage (V_{cx3}) is inserted, as shown in Figure 4.13(b). In addition, the normal active state (i.e., State 5) is inserted into the switching pattern to complete a switching interval, as shown in Figure 4.13(b). The duty cycle of the shoot-through (ST) mode (D_{st}) is generated using the indirect dc-link control technique [177].

The dc-link voltage control loop consists of an integral controller, which adjusts D_{st} based on the error value between the reference value for of the dc-link voltage (V_{dc}^{*}) and the measure dc-link voltage ($V_{dc,m}$) [177].



(a)



(b)

Figure 4.13: Modulation Logic and Switching Pattern. (a) Modified PS-PWM Logic Circuit and (b) Switching Pattern of the Converter.

4.3.2. Voltage Balancing Control Technique

In Table 4.1, the impact of the switching states on the clamping capacitor voltages has been illustrated. The voltage balancing technique is necessary to maintain the nominal clamping capacitor voltages of the converter [166]-[168]. Previous voltage balancing techniques presented in the literature are classified into passive balancing and active voltage balancing techniques, respectively [166]-[168], [189]-[194]. The active voltage balancing technique mitigates the highlighted drawbacks associated with natural balancing and passive voltage balancing techniques by either utilizing the inherent redundant switching state of the topology or by adjusting the duty cycle of the switching power semiconductor devices to compensate for the clamping capacitor voltage drift from the nominal value of the clamping capacitor voltage [189]-[194].

The inherent redundant switching state approach requires extensive computational resources to accommodate the cost function associated with each switching state [129], [130], [192]. The alternative method of adjusting the duty cycle of the switching power semiconductor devices is dependent on using linear controllers, such as P and PI controllers [189], [193], [194]. A significant drawback of using linear controllers is the slow dynamics response of maintaining the clamping capacitor voltages at their rated value [189], [193], [194]. Also, linear controllers require proper tuning for effective mitigation of the deviations in the clamping capacitor voltages, which is often very complicated to achieve [189], [193], [194]. Furthermore, the steady-state error of the PI controller results in an overshoot in the clamping capacitor voltage during start-up [195]. Most of the conventional PI controller-based voltage balancing control

schemes for clamping capacitors in a multilevel converter are implemented on a digital signal processor (DSP) platform [193], [194]. However, a time delay exists between acquiring real-time measurements, analogue to digital (A/D) conversions, and actual execution of the voltage balancing control scheme on DSP [193], [194], [196]. The time delay can be mitigated by implementing the voltage balancing control scheme on the FPGA platform, as shown in [189].

The drawbacks associated with linear controllers can be mitigated by deploying a quasi-proportional-resonant (quasi-PR) controller. This controller can modify the PS-PWM technique to achieve effective clamping capacitor voltage balancing with minimal computational resources [197]. Therefore, a mathematical formula for obtaining the quasi-PR controller parameters eliminates the need for complex tuning methods for obtaining the controller gains. The development of an effective voltage balancing control technique that requires minimal computational resources on a field-programmable gate array (FPGA) platform is presented.

Design of the Quasi-PR Controller:

The transfer function of a quasi-PR controller, as stated in (4.73) [198].

$$TF_{quasi-PR}(s) = K_p + K_r \cdot \frac{2(\omega_c)s}{s^2+2(\omega_c)s+\omega_0^2} \tag{4.73}$$

where K_p is the proportional gain, K_r is the resonant gain, ω_c is the cut-off angular frequency and ω_o is the resonant angular frequency. K_p determines the transient response of the controller. Therefore, the final value of K_p is dependent on voltage balancing dynamics of the clamping capacitor which is expressed in (4.74):

$$i_{cxn} = C_{xn} \cdot \frac{dV_{cxn}}{dt} \tag{4.74}$$

where i_{cxn} is the current flowing through the clamping capacitor, C_{xn} is the capacitance of the clamping capacitor, V_{cxn} is the voltage across the clamping capacitor (where subscript x represents the phase identification { i.e., $x = a, b, c$ } and where n represents the particular power semiconductor device and clamping device in the phase leg x of the proposed converter topology {i.e., $n = 1, \ldots\ldots, 8$}.

Furthermore, i_{cxn} is dependent on the state of the switching power semiconductor devices (s_{xn+1}, s_{xn}) as expressed in (4.75):

$$i_{cxn} = (s_{xn+1} - s_{xn}) \cdot i_x \tag{4.75}$$

where i_x is the output current of each phase leg x of the proposed converter topology. Therefore, the current flowing through the clamping capacitor (i_{cxn}) over a switching period is expressed in (4.76).

$$i_{cxn} = (d_{xn+1} - d_{xn}) \cdot i_x \tag{4.76}$$

where d_{xn+1} and d_{xn} represents the duty cycles for power semiconductor devices s_{xn+1} and s_{xn}, respectively.

Moreover, when i_x is positive (i.e., $|i_x| > 0$), i_{cxn} is increased by adjusting (i.e., increasing) d_{xn+1} and when d_{xn} is increase at $|i_x| > 0$, i_{cxn} is reduced. Therefore, when the voltage across the clamping capacitor (V_{cxn}) is greater than its reference value ($V_{cxn}{}^*$), a negative current flow through the clamping capacitor which implies that d_{xn+1} and d_{xn} should be decreased and increased accordingly. When i_x is negative (i.e., $|i_x| < 0$), the duty cycles (d_{xn+1} and d_{xn}) are adjusted in the opposite direction (i.e., reducing d_{xn+1} and increasing d_{xn}) to balance the clamping capacitor voltage. From the voltage balancing dynamics presented in (4.74), the equation can be rearranged as follows in (4.77):

$$\frac{dV_{cxn}}{dt} = \frac{i_{cxn}}{C_{xn}} \tag{4.77}$$

By substituting (4.75) into (4.77), the relationship between the change in voltage across the clamping capacitor being dependent on the state of the switching power semiconductor devices as established in (4.78):

$$\frac{dV_{cxn}}{dt} = \frac{(s_{xn+1} - s_{xn}) \cdot i_x}{C_{xn}} \tag{4.78}$$

Furthermore, substituting (4.76) into (4.77), highlights the relationship between the change in voltage across the clamping capacitor being dependent on the duty cycle of the switching power semiconductor devices as established in (4.79):

$$\frac{dV_{cxn}}{dt} = \frac{(d_{xn+1} - d_{xn}) \cdot i_x}{C_{xn}} \tag{4.79}$$

Therefore;

$$d_{xn+1} = d_i + \Delta d_{xn+1} \tag{4.80}$$

$$d_{xn} = d_i + \Delta d_{xn} \tag{4.81}$$

where d_i is the initial duty cycle of the switching power semiconductor devices (d_{xn+1}, d_{xn}), Δd_{xn+1} is the change in d_{xn+1}, and Δd_{xn} is the change in d_{xn}.

Based on (4.80) and (4.81), the duty cycles of the switching power semiconductor devices are determined from the initial duty cycle (d_i) and the change in the duty cycle associated with the controller (i.e., Δd_{x1}, ……, Δd_{xn}, Δd_{xn+1}). Whenever, the clamping capacitor voltage is unbalanced, the PWM is modified to accommodate the unbalanced clamping capacitor voltage [194]. When the voltage across the clamping capacitor (V_{cxn}) is well-balanced; V_{cxn} is equal to its reference value ($V_{cxn}{}^*$), variations in the duty cycle (i.e., Δd_{x1}, ……, Δd_{xn}, Δd_{xn+1}) will be equal to zero under this operating condition. However, when V_{cxn} is unbalanced, the variation of the duty cycle is expressed by substituting (4.80) and (4.81) into (4.79) to derive (4.82) as stated below.

$$\frac{\Delta V_{cxn}}{\Delta t} = \frac{(\Delta d_{xn+1} - \Delta d_{xn}) \cdot i_x}{C_{xn}} \tag{4.82}$$

Therefore, the variation of the duty cycles is dependent on the proportional gain (K_p) of the controller as expressed in (4.83) and (4.84) below:

$$\Delta d_{xn+1} = (\pm i_x) \cdot (\epsilon_{xn} - \epsilon_{xn+1}) \cdot (K_p) \tag{4.83}$$

$$\Delta d_{xn} = (\pm i_x) \cdot (\epsilon_{xn-1} - \epsilon_{xn}) \cdot (K_p) \tag{4.84}$$

where ϵ_{xn-1}, ϵ_{xn}, and ϵ_{xn+1} represents the voltage errors in the clamping capacitors C_{xn-1}, C_{xn}, and C_{xn+1}, respectively. $\pm i_x$ represents the polarity of the output current (i.e., " $+$ " when $|i_x| > 0$ and " $-$ " when $|i_x| < 0$).

By substituting (4.83) and (4.84) into (4.82) to obtain (4.85) which is expressed as follows:

$$\frac{\Delta V_{cxn}}{\Delta t} = \frac{|i_x| \cdot (2\epsilon_{xn} - \epsilon_{xn+1} - \epsilon_{xn-1}) \cdot (K_p)}{C_{xn}} \tag{4.85}$$

Therefore, the value of K_p can be estimated from (4.85), as stated below in (4.86):

$$K_p = \frac{\Delta V_{cxn} \cdot C_{xn}}{\Delta t \cdot |i_x| \cdot (2\epsilon_{xn} - \epsilon_{xn+1} - \epsilon_{xn-1})} \tag{4.86}$$

Furthermore, values of the voltage errors in (4.86) is defined as follows; the clamping capacitor voltage error is defined as $\Delta V_{cxn} = V_{cxn}{}^* - V_{cxn} = \epsilon_{xn}$, and the value of the unbalanced clamping capacitor C_{xn} is assumed to be $|\epsilon_{xn}| = V_{dc}/(n_{VL} - 1)$. Based on the presented assumptions, (4.86) can be simplified in (4.87) as follows:

$$K_p = \frac{C_{xn} \cdot f}{(2) \cdot i_x} \tag{4.87}$$

where f is the fundamental frequency of the converter topology.

To minimize the overshoot in the clamping capacitor voltage based on the operation of the controller, the steady-state error will be eliminated by proper tuning of the resonant gain (K_r) of the controller. In [199], the relationship between K_p and K_r was established through K_{factor} to eliminate the phase and magnitude steady-state error of the controller as expressed in (4.88).

$$K_{factor} = \frac{K_r}{K_p} \tag{4.88}$$

Also, in [198], the value of ω_c and ω_o are obtained from (4.89) and (4.90).

$$\omega_c = 2 \cdot \pi \cdot (0.02f) \tag{4.89}$$

$$\omega_0 = 2 \cdot \pi \cdot (3f) \tag{4.90}$$

The proposed quasi-PR voltage balancing control for the clamping capacitor voltage of the proposed converter topology is shown Figure 4.14.

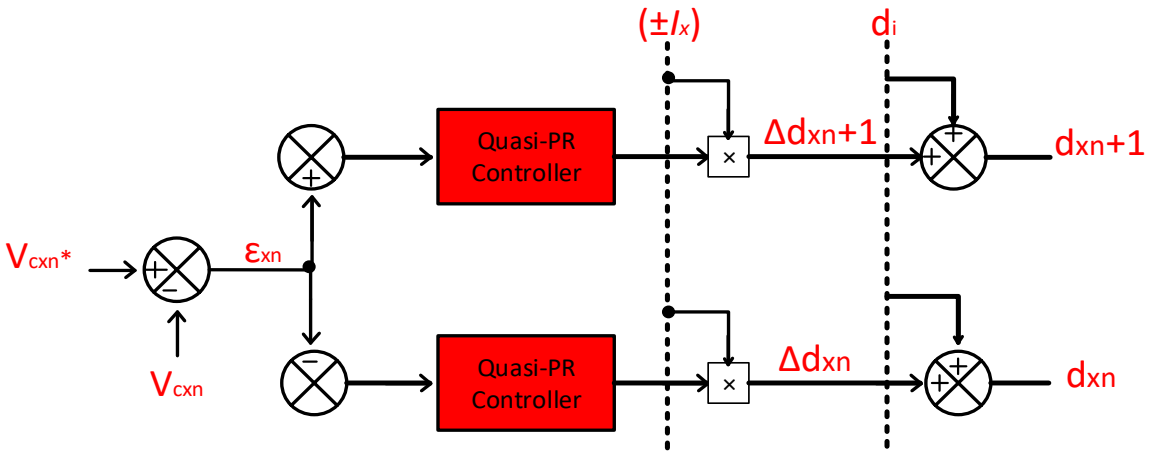
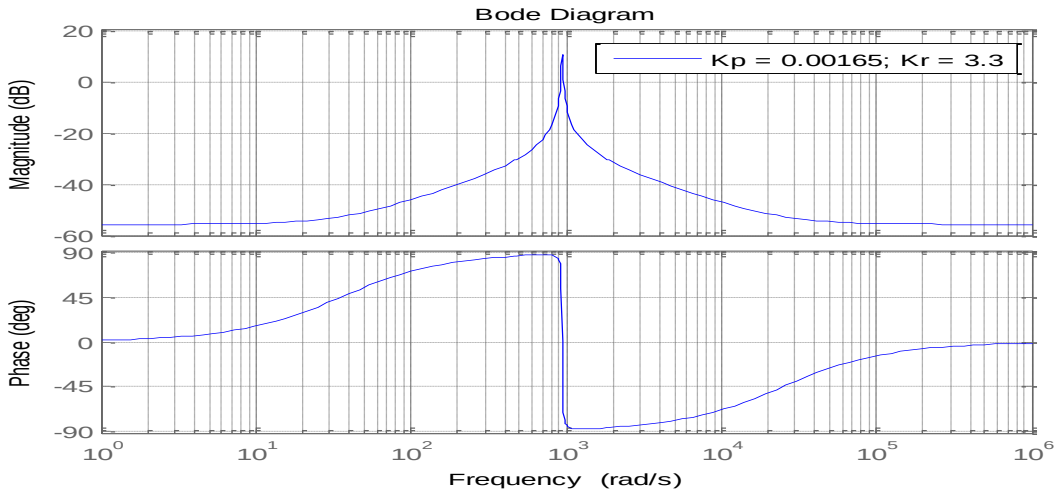


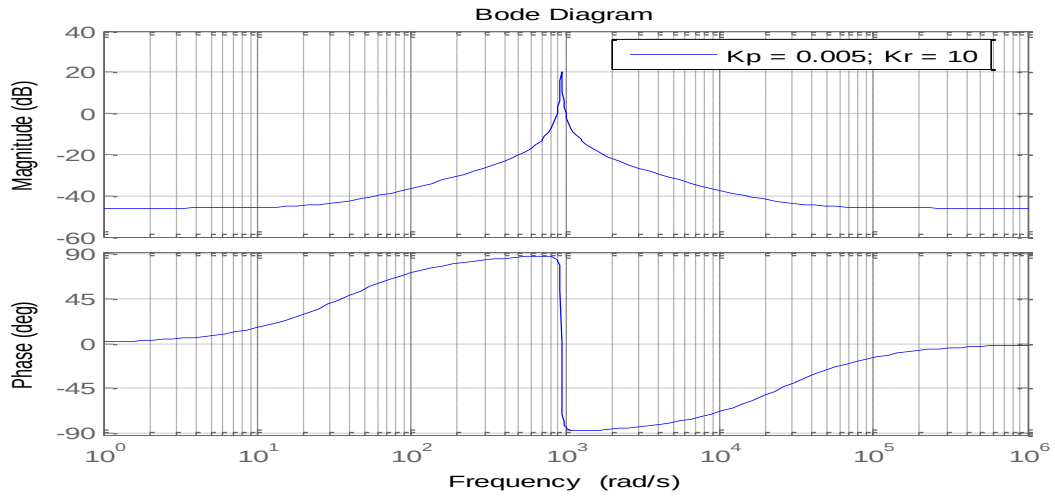
Figure 4.14: Block diagram of the proposed voltage balancing control technique.

The design of the quasi-PR controller is analyzed through the open-loop bode diagram shown in Figure 4.15. The value of K_p is obtained from parameters in Table 4.6 using (4.88), while K_{factor} is fixed to 2000 to obtain the value of K_r [199], which reduces the steady-state error. The reduced steady-state error minimizes the overshoot during the pre-charging and balancing of the clamping capacitor voltage. Furthermore, the impact of output frequency variation on the controller is considered in the design through a $\pm 2\%$ margin in the cut-off angular

frequency (ω_c) [198]. The FPGA implementation of the voltage balancing control strategy is presented in detail in Chapter 6 [200]-[205].



(a)



(b)

Figure 4.15: Bode diagram of the open-loop transfer function of the quasi-PR controller for clamping capacitors (C_{x3}, C_{x2}, C_{x1}). (a) C_{x3}; with $K_p = 0.00165, K_r = 3.3$. (b) $C_{x2} = C_{x1}$; with $K_p = 0.005, K_r = 10$.

4.4. Results and Discussions

This section presents the experimental results of the proposed converter topology. Figure 4.16 shows the experimental prototype highlighting the tapped inductor quasi-Z-source network, the five-level NNPC converter topology, output filter, NI-PXIe-1071 platform, and loads. The values of the components used in the experimental prototype are stated in Table 4.6.

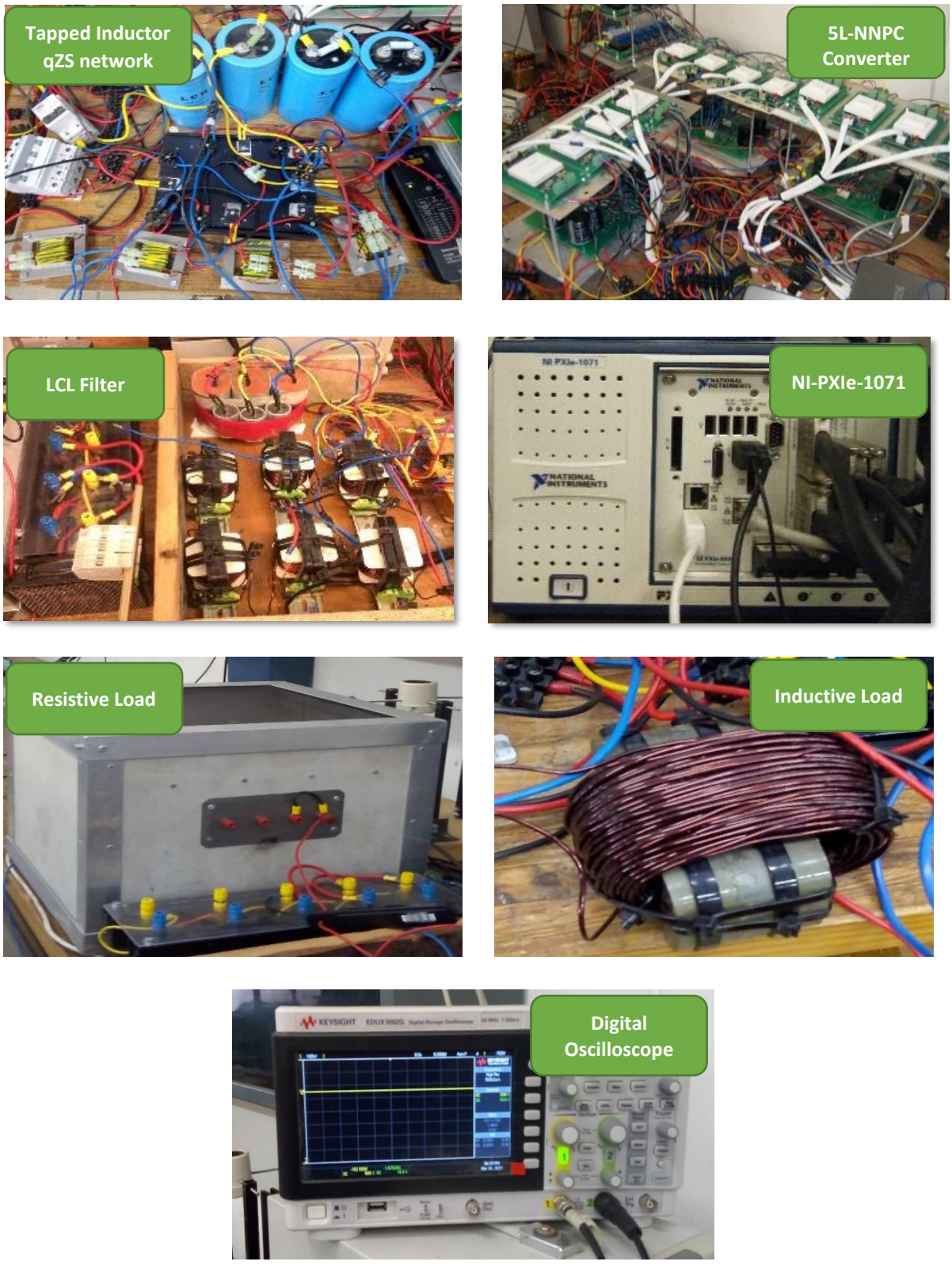


Figure 4.16: Experimental prototype of the 5L-tapped inductor qZS-NNPC converter.

Table 4.6: Experimental Parameters

Parameters	Values
Input dc source voltage (V_{in})	$100\ V$
qZS network input inductors	$98\mu H$
qZS network tapped inductors	$32\mu H$
qZS network capacitor (C_1, C_2, C_3, C_4)	$330\mu F$
Outer clamping capacitor (C_{x3})	$470\ \mu F$
Inner clamping capacitors (C_{x2} and C_{x1})	$1000\ \mu F$
Output frequency	$50\ Hz$
Switching frequency	$5kHz$
Proportional Gain for C_{x3} (K_p)	0.00165
Proportional Gain for C_{x2} and C_{x1} (K_p)	0.005
Resonant Gain for C_{x3} (K_r)	3.3
Resonant Gain for C_{x2} and C_{x1} (K_r)	10
Converter-side inductor filter (L_c)	$2.1mH$
Load-side inductor filter (L_l)	$2.1mH$
Filter capacitor (C_f)	$6\mu F$
Damping resistor (R_d)	4.41Ω
Inductive Load	$5mH$
Resistive Load	10Ω

The switching power semiconductor devices and gate driver circuitry are developed using Infineon Technologies 47N60C3 and Semikron SKHI22AH4R. A nichicon electrolytic capacitor is used for the dc-link capacitors, clamping capacitors, and qZS network capacitors.

The clamping capacitor voltages and load current were measured by LEM LV25-P and LA25-NP transducers, respectively. The NI PXI-7842R FPGA module implements the modulation and voltage balancing control schemes. The gating signals are sent to the gate driver circuit via the NI SCB-68A interface board (as discussed in Chapter 6). Also, the measured data is acquired by the NI PXIe-6363 DAQ module, which is programmed using LabVIEW real-time. Both the NI PXI-7842R FPGA and NI PXIe-6363 DAQ modules are connected to the NI PXIe-1071 chassis.

The output waveforms are measured and presented through the two channels EDUX-1002G digital oscilloscope with a Tektronix P5200 high voltage differential probe and PT-350 high-frequency current probe. Furthermore, the experimental verification was carried out on every phase instantly and confirmed on all the other phases. In this section, the experimental result validates the theoretical analysis, simulation (carried out in MATLAB/Simulink environment), and FPGA realization of the proposed converter topology. Therefore, the results are presented in two main categories, namely: boosting capability and performance analysis.

4.4.1. Boosting Capability

The switching waveform of the converter topology based on the modulation technique presented in section 4.3 and implemented through the FPGA-based platform, under the condition of $m_a = 0.9$ and $D_{st} = 0.1$. The generated PWM waveforms sent from the PXI system (discussed in Chapter 6) via the interface board to the gate driver circuitry shown in Figure 4.17(a) to 4.17(d).

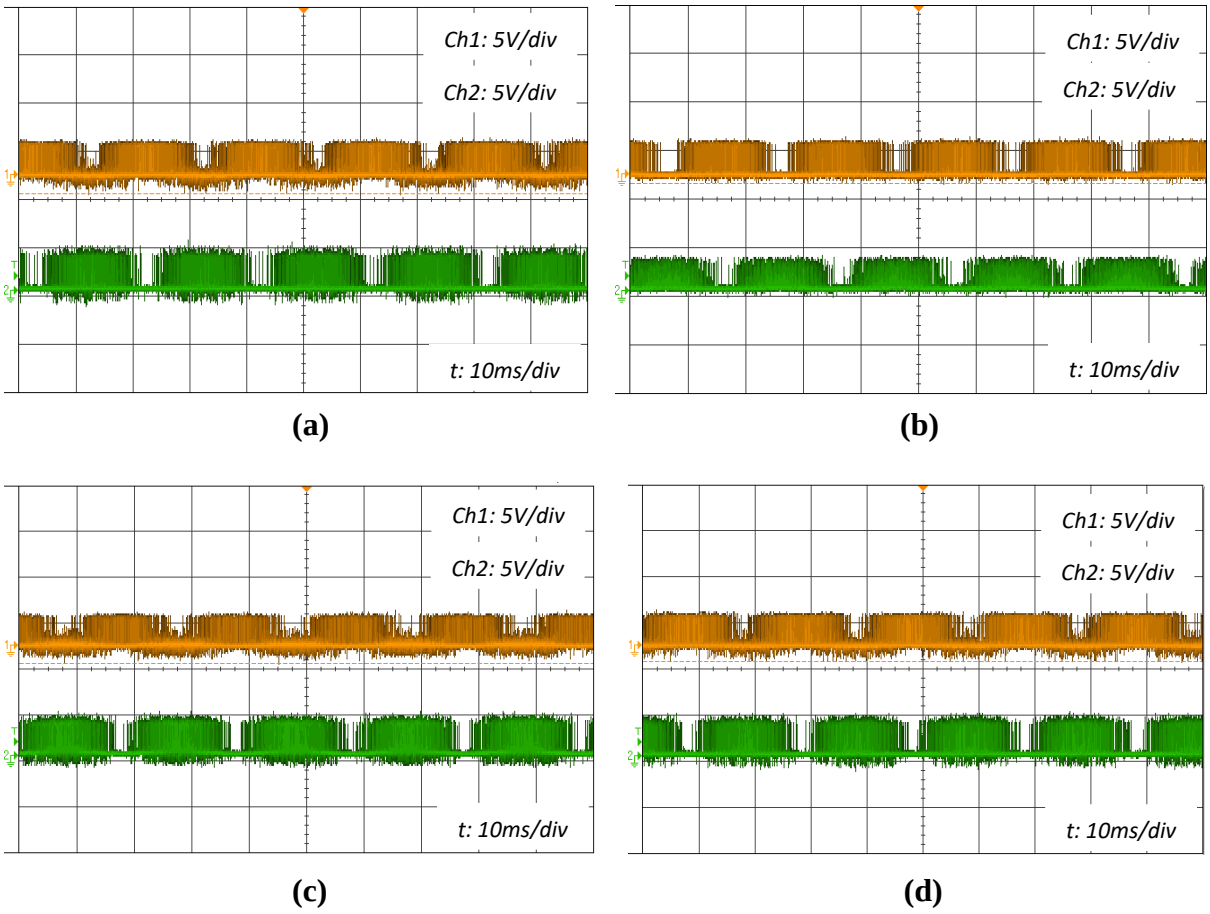
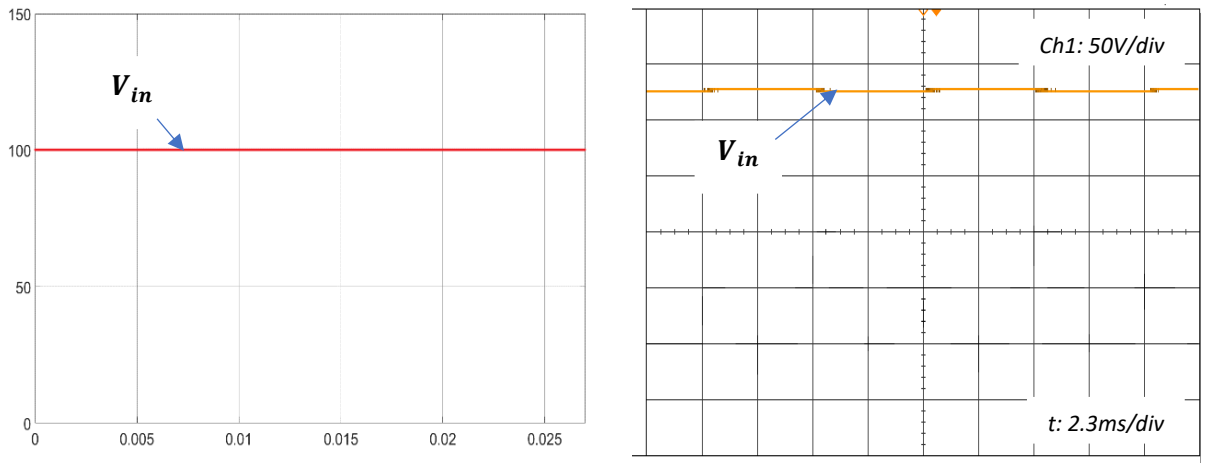


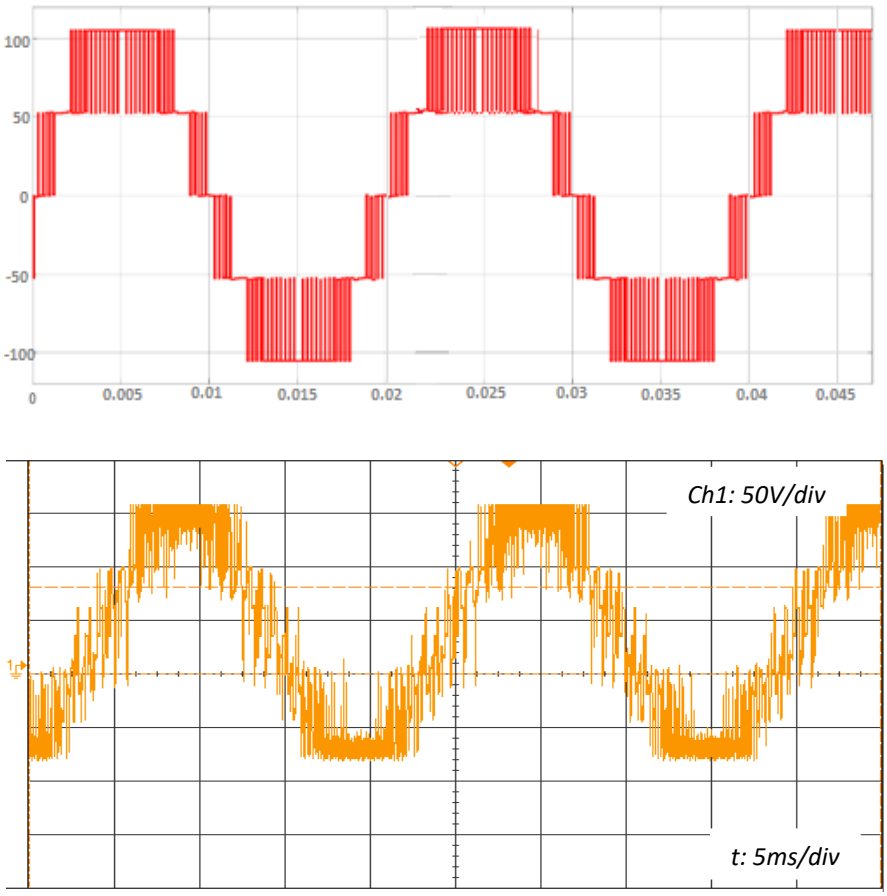
Figure 4.17: Switching waveforms of the power semiconductor devices. (a) S_1 & S_8 , (b) S_2 & S_7, (c) S_3 & S_5, (d) S_4 & S_6.

The input dc source voltage (V_{in}) is $100V$, and the converter is operated at a switching frequency $5kHz$, as stated in Table 4.9. The simple boost control technique is deployed to modulate the topology, as discussed in Section 4.3. The simulated and experimental input dc source voltage (V_{in}) have been illustrated in Figure 4.18(a). According to the boost factor (B_f) stated in (4.37), and values presented in Table 4.2, the phase voltage of the converter should increase by a factor of 1.36. From the simulation result, the phase voltage measured is about $119V$, as shown in Figure 4.18(b). Furthermore, the measured phase voltage from the experimental result is about $112.3V$, as shown in Figure 4.18(b).

The boosting capability of the converter topology can be further expanded by either increasing the turns ratio (N) or increasing D_{st}. While $N = 1$ from the experimental prototype presented in this section, an increase in the turns ratio by a factor of five would result in the experimental phase voltage being estimated to be $152.9V$, representing a boost factor of 1.76, as illustrated in Figure 4.19(a). Also, when $N = 5$, the phase voltage should be about $154V$, as shown in Figure 4.19(a). When the duty cycle of the ST mode (i.e., $D_{st} = 0.2$) is doubled with $N = 5$; the voltage level of the converter topology is increased by a factor of 3, as depicted in Figure 4.19(b). However, an increase in D_{st} will further reduce m_a resulting in more distortion of the output voltage waveform [182].

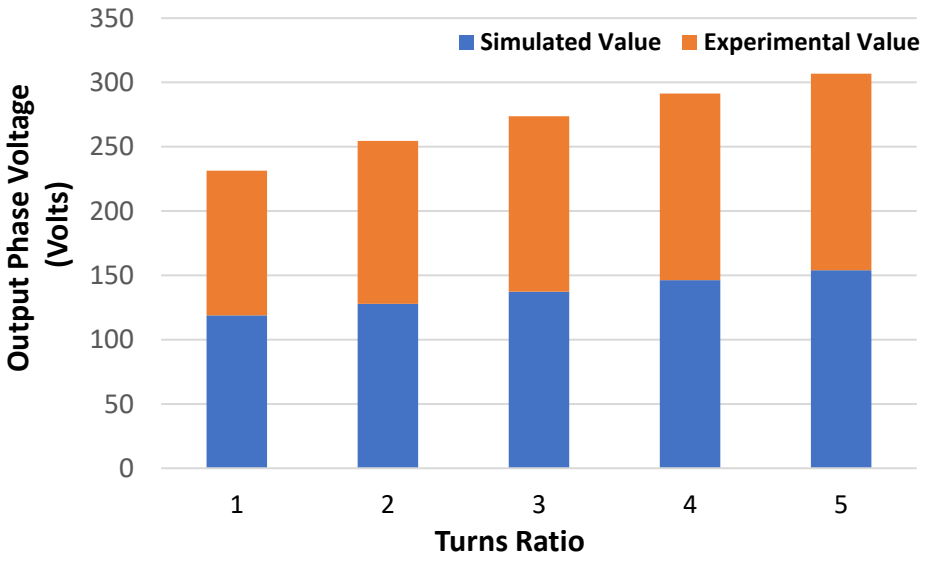


(a)

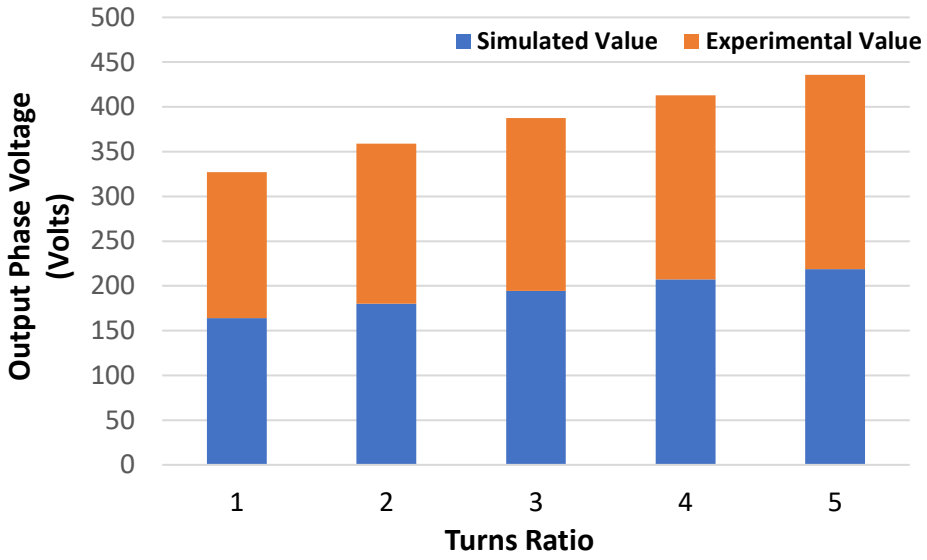


(b)

Figure 4.18: Simulated and experimental input dc voltage and output phase voltage. (a) dc input voltage, (b) output phase voltage.



(a)

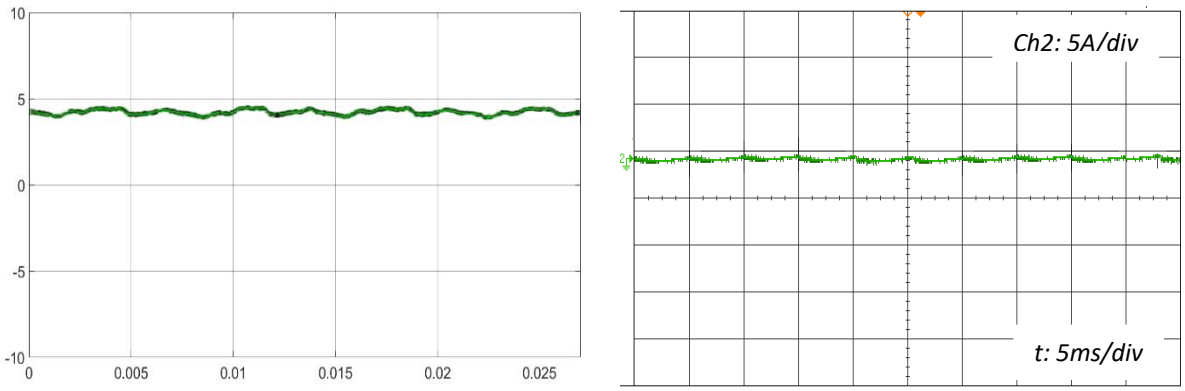


(b)

Figure 4.19: Voltage gain. (a) change in turns ratio, (b) change in turns ratio with increase shoot-through duty ratio.

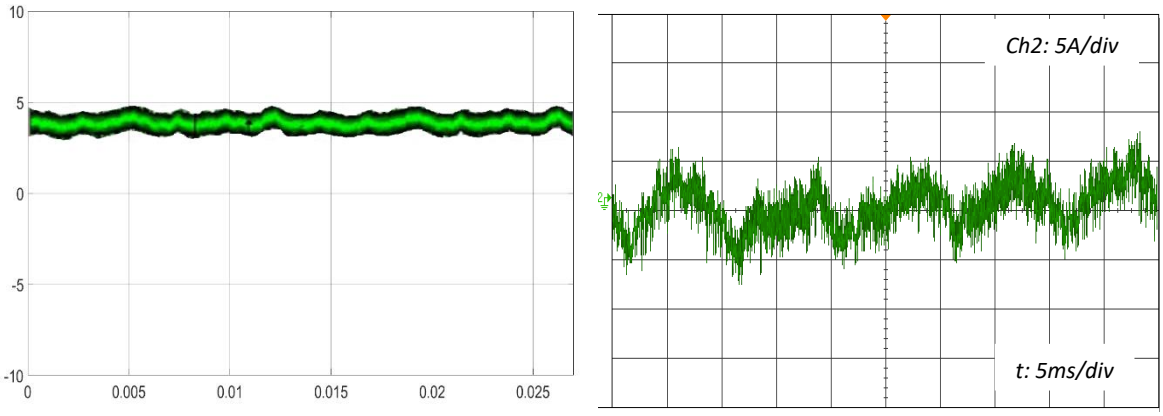
Furthermore, the input current flowing through the inductor (L_1) is flowing continuously (CCM), and the current ripple is eliminated due to the inductance value stated in Table 4.5, as shown in Figures 4.20(a) and 4.20(b). The current flow is observed during the converter topology NST mode, validated with both simulation and experimental waveforms presented in Figures 4.20(a) and 4.20(b). However, during the ST mode, the current flowing through the inductors shows the current ripple of about 5%, but it is still flowing continuously, as shown in Figures 4.21(a) and 4.21(b). The ripple during the ST mode is due to the disparity between the output filter and the connected load; the output filter was developed for a grid connection, as explained in Chapter 6. Identical waveforms were observed with current flowing through inductor (L_4) and the tapped inductors ($L_2 + L_3, L_5 + L_6$).

The sum of the capacitor voltages $V_{C1} + V_{C3}$ is constant both in the ST and NST modes, as shown in Figures 4.22(a) to 4.22(c). The stable capacitor voltages maintain the constant output voltage and current as illustrated in Figures 4.23(a) to 4.23(b).



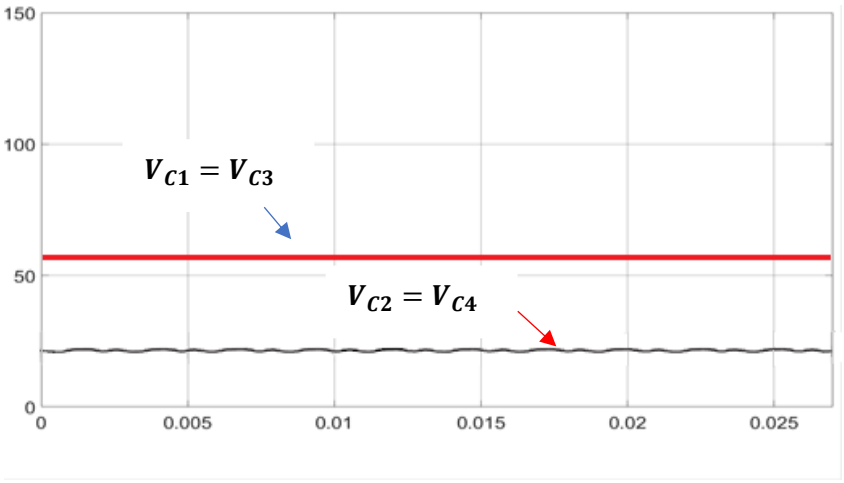
(a) **(b)**

Figure 4.20: Current flowing through the input inductor (L_1) during NST mode. (a) simulated waveform, (b) experimental waveform.

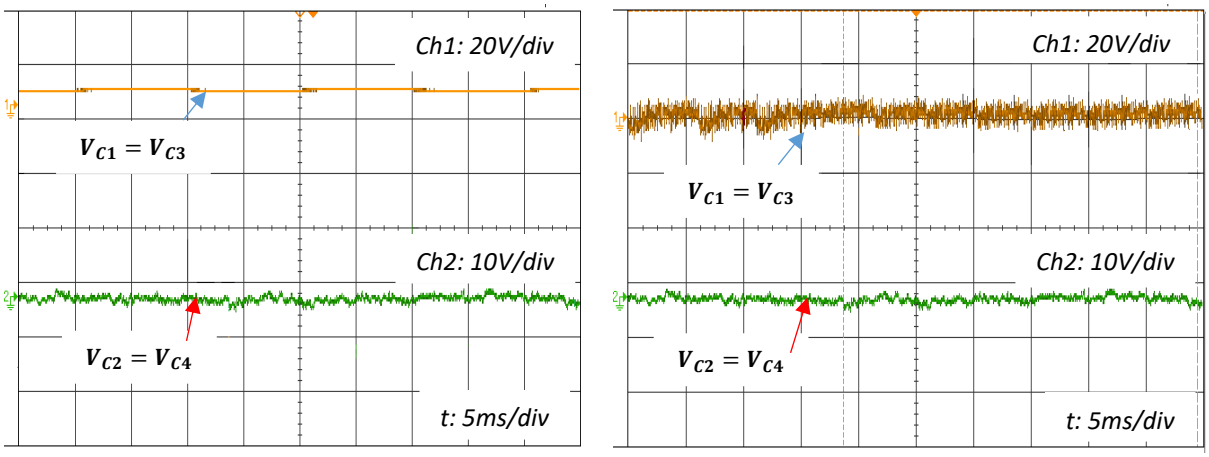


(a) **(b)**

Figure 4.21: Current flowing through the input inductor (L_1) during ST mode. (a) simulated waveform, (b) experimental waveform.

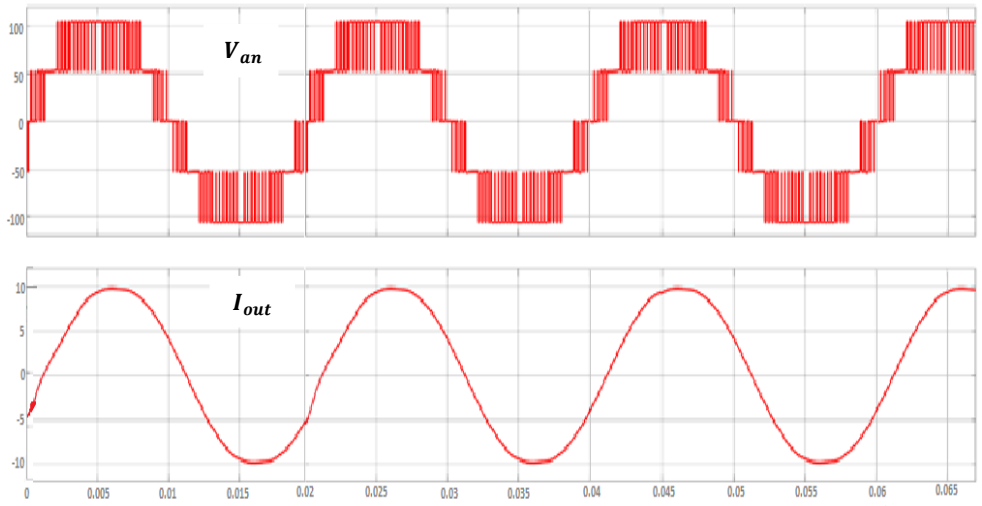


(a)

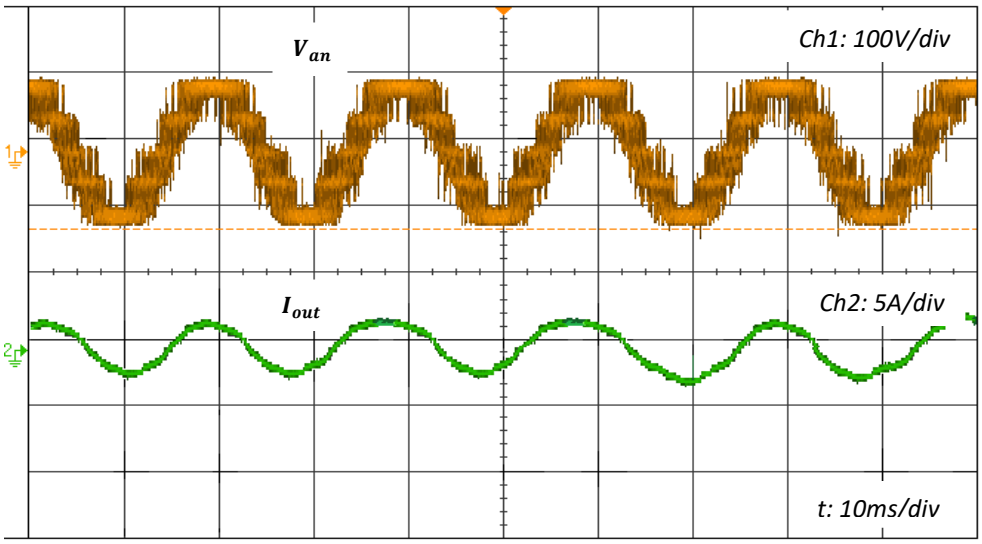


(b) **(c)**

Figure 4.22: Voltage across qZS network capacitors. (a) simulated waveform during NST mode, (b) experimental waveform during NST mode, (c) experimental waveform during ST mode.



(a)



(b)

Figure 4.23: Output phase voltage and output current. (a) simulated phase voltage and output curent, (b) actual phase voltage and output current.

4.4.2. Performance Analysis

This section evaluates the performance of the proposed converter topology by analyzing the voltage balancing control technique and highlighting the inherent fault-tolerant characteristics during the open-circuit failure of the switching power semiconductor devices. Therefore, the theoretical and FPGA implementation of the voltage balancing control and switching sequence of the proposed converter topology is verified experimentally.

A. Voltage Balancing Control Technique

In Table 4.1, the switching states have been highlighted in both NST and ST modes of operation. However, the impact of each switching state on the clamping capacitor voltages occurs at the switching states within the following voltage levels, $V_{dc}/4$, 0, and $-V_{dc}/4$. These switching states are implemented in the LabVIEW FPGA environment, as illustrated in Figure 4.24 (the back end of the code is found in Appendix C.2). Therefore, different switching sequences consisting of a combination of the highlighted switched states can be activated to study their impact on the clamping capacitor voltages. Furthermore, there are twenty-eight possible switching sequences to produce the five-level output voltage of the converter topology. The effectiveness of the voltage balancing control technique is studied under three different switching sequences, and the impact of the continuous discharge of the clamping capacitor voltage is studied. Therefore, the converter topology is connected to a resistive-

inductive (RL) load between its midpoint and output (i.e., values of the resistor and inductor load).

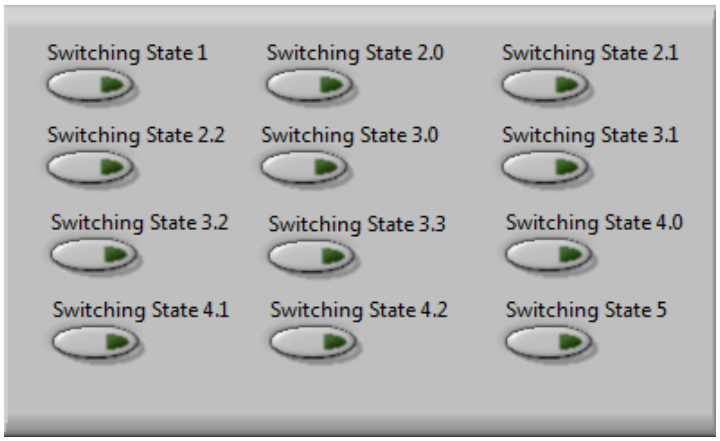


Figure 4.24: Front panel of the switching states in LabVIEW FPGA.

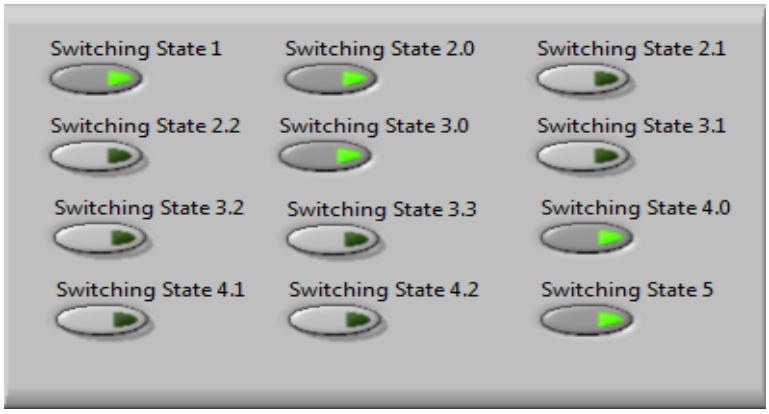
Switching Sequence-1: *State 1-State 2-State 3-State 4-State 5*

According to the switching states in Table 4.1, the selected sequence activated in the real-time LabVIEW environment (shown in Figure 4.25(a)) has no impact (N) on the three clamping capacitor voltages of the converter topology. The effect of the switching sequence on the

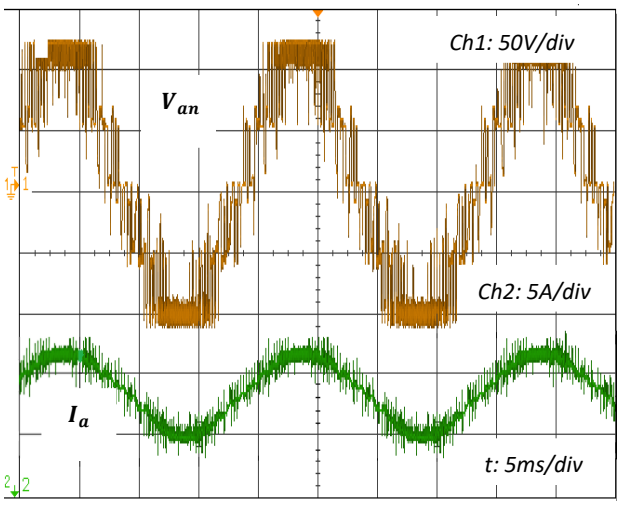
Table 4.7: Impact of switching sequence 1 on clamping capacitor voltages.

Clamping Capacitor Voltage	State 1	State 2	State 3	State 4	State 5	Overall State
$\boldsymbol{V_{cx1}}$	N	C	C	N	N	N
$\boldsymbol{V_{cx2}}$	N	N	C	D	N	N
$\boldsymbol{V_{cx3}}$	N	N	N	N	N	N

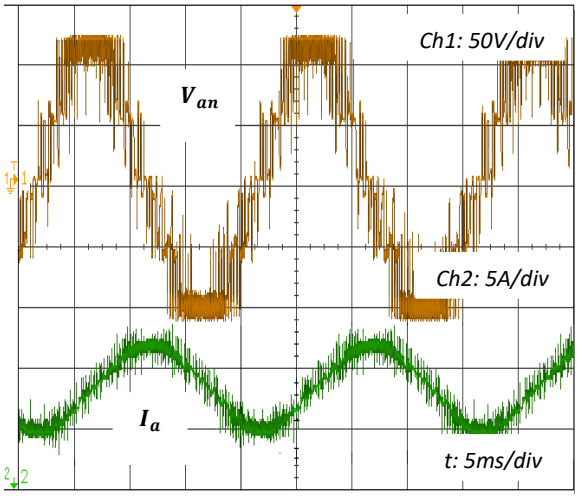
clamping capacitor is illustrated in Table 4.7. Theoretically, when the phase current of the converter topology is more significant than zero($i_a > 0$), the clamping capacitor voltages remain constant at this switching sequence with no impact (N) on their respective voltages. The natural balancing phenomenon associated with the PS-PWM technique is achieved mainly due to the high modulation index ($m_a = 0.9$) of the converter [166]-[168]. The voltage balancing of the clamping capacitors is stable with the connected RL load under unity power factor ($PF = 1$) and lagging power factor (PF=0.78lagging), as shown in Figures 4.25(b) and 4.25(c).



(a)



(b)



(c)

Figure 4.25: Natural balancing phenomenon. (a) the activated sequence in LabVIEW RT, (b) output voltage and load current with unity PF, (c) output voltage and load current with 0.78 lagging PF.

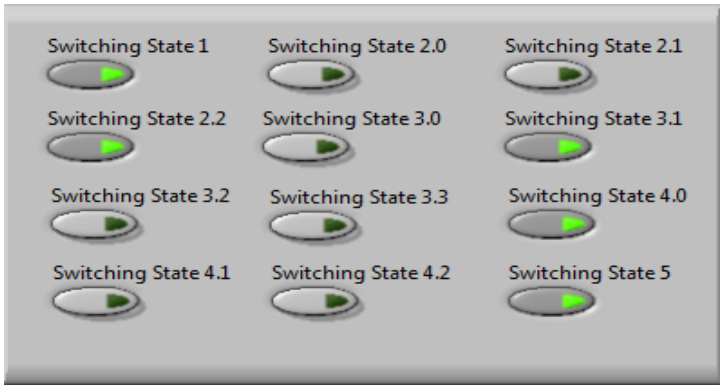
Switching Sequence-2: *State 1-State 2.2-State 3.1-State 4-State 5*

This selected sequence (shown in Figure 4.26(a)) results in a continuous discharge of the inner clamping capacitor voltage (V_{Cx2}). In Table 4.8, V_{Cx2} is discharged within three switching instants of the sequence, which results in its voltage reduced by 40%. In Figure 4.26(b), the output voltage of the converter shows a four-level voltage waveform because of V_{Cx2} being continuously discharged as depicted.

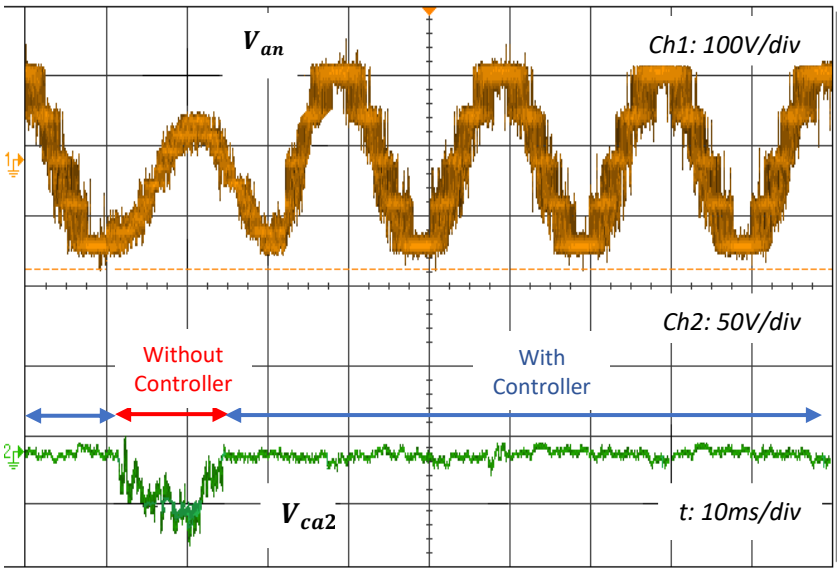
After the voltage balancing technique is activated, the value of V_{Cx2} is within its rated range, which is about one-quarter of the dc-link voltage, as previously stated. Figure 4.26(c) shows the output voltage (V_{an}) and V_{Ca2} waveforms of the converter topology after the voltage balancing technique is activated. The response voltage ripple is minimal due to the non-existence of the steady-state error, as discussed previously.

Table 4.8: Impact of switching sequence 2 on clamping capacitor voltages.

Clamping Capacitor Voltage	State 1	State 2.2	State 3.1	State 4	State 5	Overall State
V_{cx1}	N	D	N	N	N	N
V_{cx2}	N	D	D	D	N	D
V_{cx3}	N	C	C	N	N	N



(a)



(b)

Figure 4.26: Voltage balancing of V_{Cx2}. (a) activated sequence in LabVIEW RT, (b) output voltage and clamping capacitor voltage waveform during discharge and after balancing.

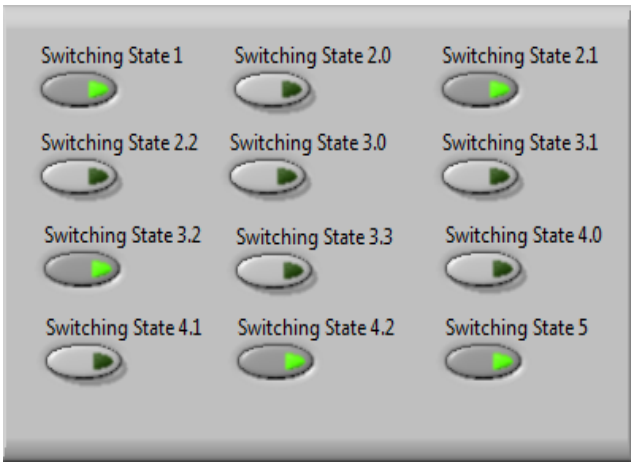
Switching Sequence-3: *State 1-State 2.1-State 3.2-State 4-State 5*

This selected sequence (shown in Figure 4.27(a)) results in a continuous discharge of the outer clamping capacitor voltage (V_{Cx3}). In Table 4.9, V_{Cx3} is discharged within three switching instants of the sequence. In Figure 4.27(b), the output voltage waveform of the converter while V_{Cx3} is being continuously discharged as depicted.

After the voltage balancing technique is activated, the value of V_{Cx3} is within its rated range, which is about three-quarters of the dc-link voltage, as previously stated. Figure 4.27(c) shows the output voltage (V_{an}) and V_{Ca2} waveforms of the converter topology after the voltage balancing technique is activated.

Table 4.9: Impact of switching sequence 3 on clamping capacitor voltages.

Clamping Capacitor Voltage	State 1	State 2.1	State 3.2	State 4.2	State 5	Overall State
$\boldsymbol{V_{cx1}}$	N	N	C	C	N	N
$\boldsymbol{V_{cx2}}$	N	N	N	C	N	N
$\boldsymbol{V_{cx3}}$	N	D	D	D	N	D



(a)

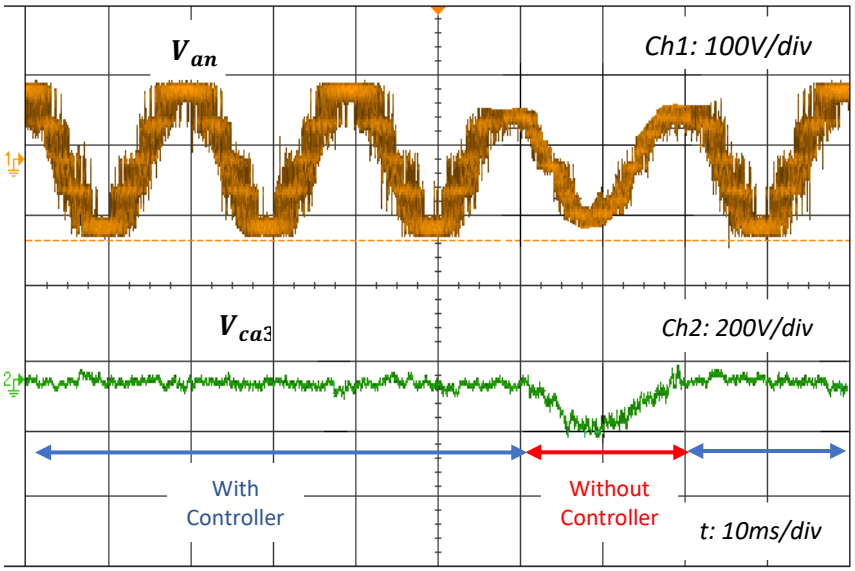
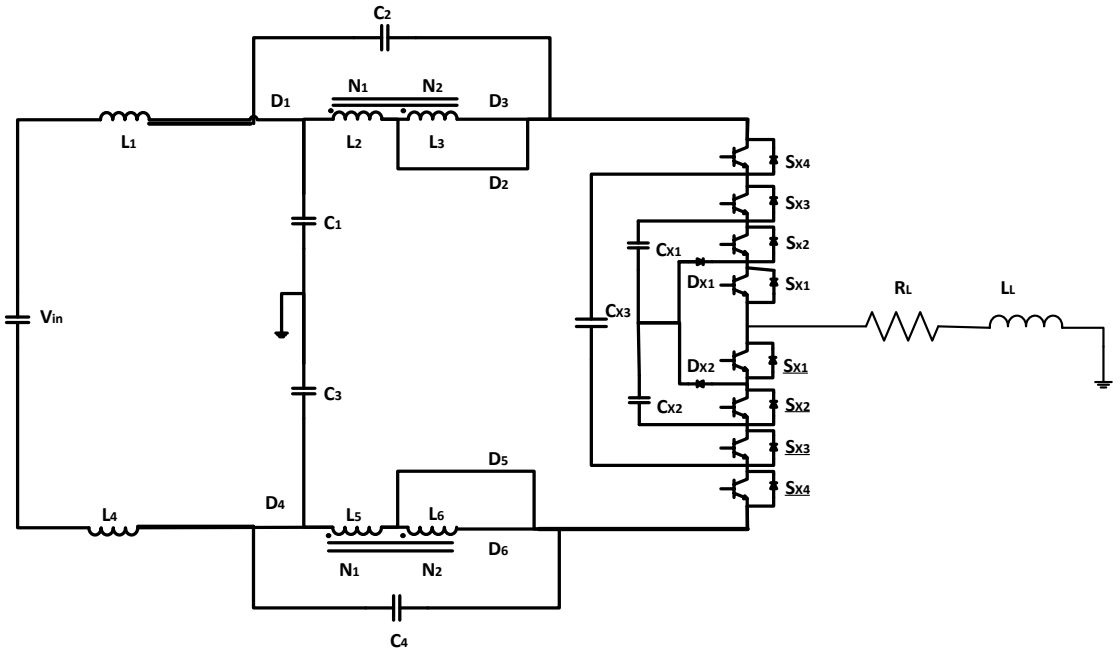


Figure 4.27: Voltage balancing of V_{Cx3}. (a) activated sequence in LabVIEW RT, (b) output voltage and clamping capacitor voltage waveform during discharge and after balancing.

B. Fault-Tolerant Characteristics

The two main types of failure associated with the switching power semiconductor devices of a converter topology are stated as follows: open-circuit fault and short-circuit fault [170]. Due to the addition of the qZS network to the presented converter topology, the impact of a short-circuit failure is minimized when compared to conventional voltage source converter topologies [170], [206]. Therefore, the inherent fault-tolerant characteristics of the proposed five-level tapped inductor quasi-Z-source NNPC converter topology is presented in this section.

The impact of a single switching power semiconductor device on the five-level tapped inductor quasi-Z-source NNPC converter in the upper and lower parts of the topology have been investigated under the switching sequence-1 scenario. The equivalent circuit of a healthy and faulty converter topology is shown in Figure 4.28(a) to 4.28(c). Each of the open-circuit failures was implemented in the LabVIEW FPGA environment with the faulty switching power semiconductor device eliminated from the switching state sequence to represent an open-circuit failure each switching instant.


C2
D1
N1
N2
D3
L1
L2
L3
D2
C1
Vin
C3
D5
D4
L4
L5
L6
D6
N1
N2
C4
Sx4
Sx3
Sx2
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Cx2
Sx2
Sx3
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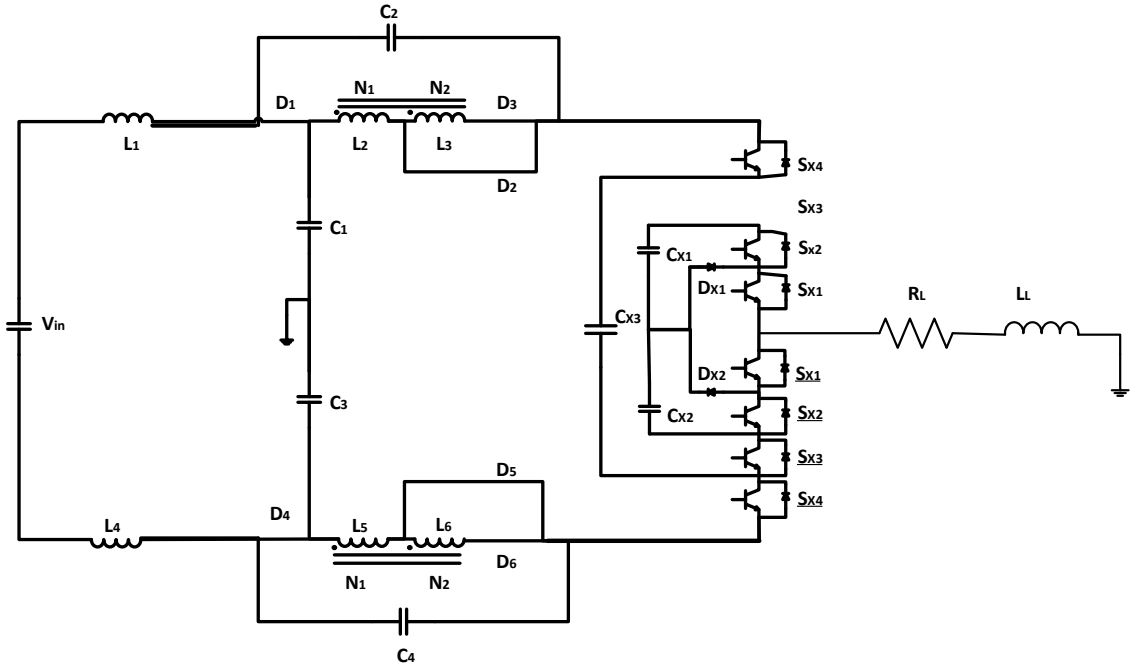
(a)


C2
D1
N1
N2
D3
L1
L2
L3
D2
C1
Vin
C3
D5
D4
L4
L5
L6
D6
N1
N2
C4
Sx4
Sx3
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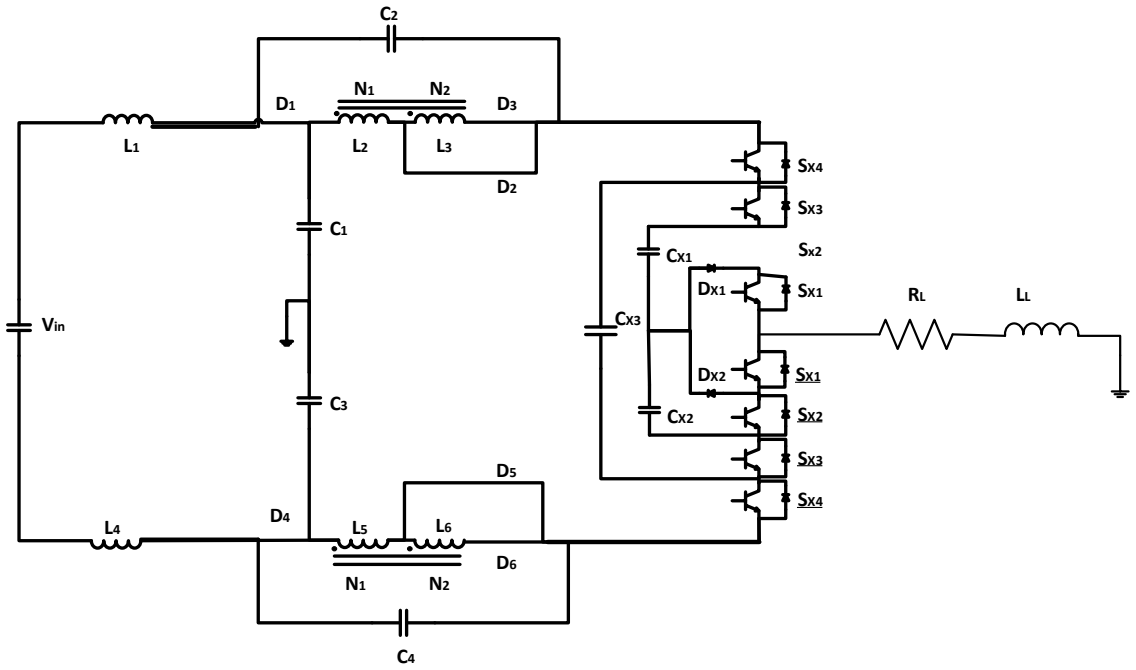
Cx2
Sx2
Sx3
Sx4

(b)



(c)

Figure 4.28: Equivalent circuit of healthy and faulty converter topology. (a) normal (healthy) converter topology, (b) open-circuit fault in S_{x3}, (c) open-circuit fault in S_{x2}.

When S_{x3} is faulty due to an open-circuit failure, the output voltage and load current waveforms that occurs during the switching sequence is shown in Figure 4.29(a). The level of distortion in the waveforms is increased after the faulty condition. This further increases the total harmonic distortion (THD) of the produced waveforms, as stated in Table 4.10. Also, the level of distortions in the output voltage and load current waveforms when S_{x2} is faulty, as shown in Figure 4.29(b). Furthermore, the voltage level is reduced from five levels to just two levels in the faulty converter, as shown in Figure 4.29(b).

The reduced voltage and current amplitude after the failure has occurred can be compensated by adjusting the modulation index (m_a) and duty cycle of the ST mode (D_{st}) as presented in [206]. Based on the relationship between m_a and D_{st}, the values of m_a and D_{st} are 0.9 and 0.1 before the fault occurs. By adjusting m_a and D_{st}, to be 0.848 and 0.152, the output voltage and load currents are increased after the S_{x3} and S_{x2} failures. Therefore, with the adjusted modulation index, the converter can be operated as a four-level converter after the S_{x3} failure, as shown in Figure 4.29(c). Also, the converter is operated as a three-level converter after the S_{x2} failures, as shown in Figure 4.29(d).

Table 4.10: THD of the converter output voltage and load current.

Condition	Load Current THD (%)	Output Voltage THD (%)
Healthy converter	2.3	23.83
S_{x3} fault without adjusted m_a	23.45	40.22
S_{x3} fault with adjusted m_a	3.49	33.2
S_{x2} fault without adjusted m_a	12.67	46.8
S_{x2} fault with adjusted m_a	4.45	38.7

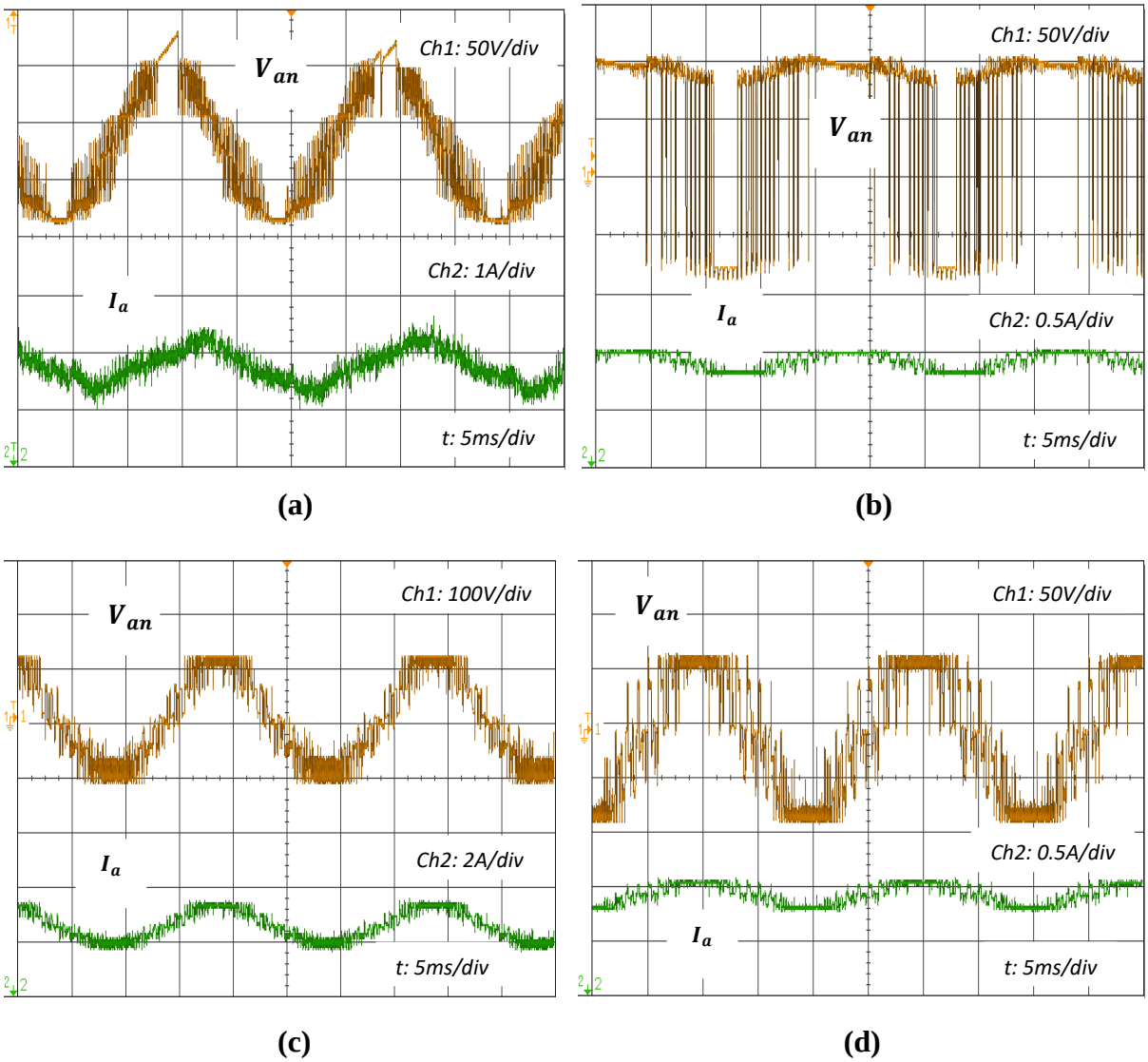


Figure 4.29: Experimental results of the open-circuit faults in the converter (a) voltage and current waveform with the fault in S_{x3} , (b) voltage and current waveform with the fault in S_{x2} (c) voltage and current waveform with the fault in S_{x3} and adjusted m_a, (d) voltage and current waveform with the fault in S_{x2} and adjusted m_a.

C. Efficiency Analysis

The measured efficiency of the proposed five-level tapped inductor quasi-Z-source NNPC converter topology prototype connected to the RL load is presented in this sub-section. The maximum efficiency is achieved while operating the converter with a modulation index (m_a) of unity without the shoot-through duty cycle(D_{st}), as shown in Figure 4.30. Furthermore, the curve illustrates that an increase in the D_{st} will decrease the efficiency of the converter topology. A significant advantage of the proposed converter topology is the turns ratio of the tapped inductor can be adjusted to increase its boosting capability without adjusting D_{st} beyond 0.1.

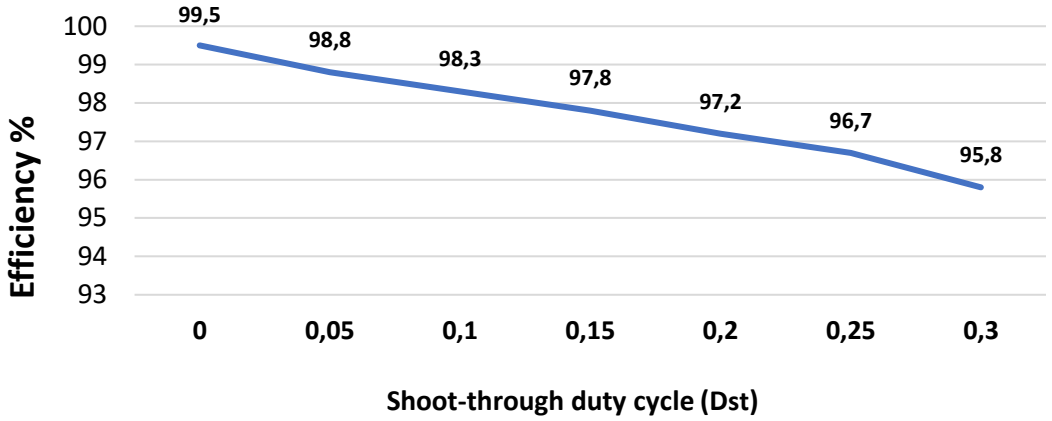


Figure 4.30: Measured efficiency of the proposed converter topology.

4.5. Conclusion

In this chapter, the tapped inductor quasi-Z-source NNPC converter topology is presented. The significant contributions of the work carried out in this chapter are summarized as follows:

- The derivation and theoretical analysis of the five-level tapped inductor quasi-Z-source NNPC converter topology have been presented, emphasizing its operating principles, steady-state analysis, and deriving equations to calculate its inductance and capacitance values.
- The modulation technique of the converter topology and voltage balancing control technique of the clamping capacitor voltage has been presented.
- The theoretical analysis and FPGA implementation of the proposed converter topology was verified experimentally with a developed prototype of the topology.

Chapter 5

DC Component Minimization Technique

The dc component injection into the grid is one of the significant drawbacks of deploying transformer-less WECSs in a WPP, as discussed previously in Chapter 1. Firstly, this chapter discusses the primary sources of the generated dc components in the proposed multilevel converter topology. Secondly, the contribution of the switching power semiconductor devices' asymmetrical characteristics towards the dc component generation is analyzed. Thirdly, a discussion on the comparative evaluation of the existing dc component minimization technique in the literature is presented in the chapter. This chapter proposes a dc component minimization technique that combines detection hardware with a digital filtering method. Finally, experimental results are presented to validate the proposed dc component minimization method.

5.1. Introduction

Transformer-less connections of grid-connected converter topologies have the following advantages: low cost, increased efficiency, and compact size [77]-[80]. However, a transformer-less grid-connected converter generates dc components due to the asymmetrical switching characteristics of its switching power semiconductor devices, the nonlinearity of the transducers, sampling errors, and unbalanced grid voltage [77]-[80], [207]-[215]. Therefore, the proliferation of transformer-less grid-connected converter topologies on the grid will result in the saturation of substation transformers, corrosion of the connecting cables, and grid synchronization irregularities [77]-[80], [207]-[215].

The generation of dc components because of the non-uniformity in the switching power semiconductor devices often occurs due to the asymmetrical nature of the gate driver circuitry and the asymmetrical characteristics of the power semiconductor devices [77]-[80], [207], [208]. The gating signals generated from the gate-driver circuitry are asymmetrical because of slightly different time delays [207], [208]. This feature is more evident in the proposed converter topology due to its dual mode of operation and multiple clamping devices.

Furthermore, the slight variation in power semiconductor devices' characteristics – in terms of on-state resistance, collector-emitter saturation voltage, and junction capacitance –contributes to its asymmetrical nature [207], [208]. Therefore, multilevel converter topologies with numerous power semiconductor devices would generate more dc components than a conventional two-level converter.

The current reference in a closed-loop control algorithm contains dc components due to disparity in the voltage feedback loop [207]. Simultaneously, the voltage feedback loop regulates the outer voltage loop that provides the current loop's reference [207]. Therefore, the current reference will contain dc components due to the voltage feedback loop [207]. Furthermore, the LEM voltage and current sensors that measure the grid voltage and grid current operate on the hall-effect principle [83]. However, a hall-effect-based sensor's drawbacks are gain drift, offset, and nonlinearity whenever ac outputs are measured [209]. These highlighted disadvantages result in the generation of dc components and further amplified by the controller [83], [207]. Another source of dc component in the proposed converter topology is sampling error within the analogue-to-digital (A/D) conversion when the measured parameters are digitalized and transferred to the digital control algorithm [207]. Figure 5.1 shows the various sources of the dc components in a grid-connected converter.

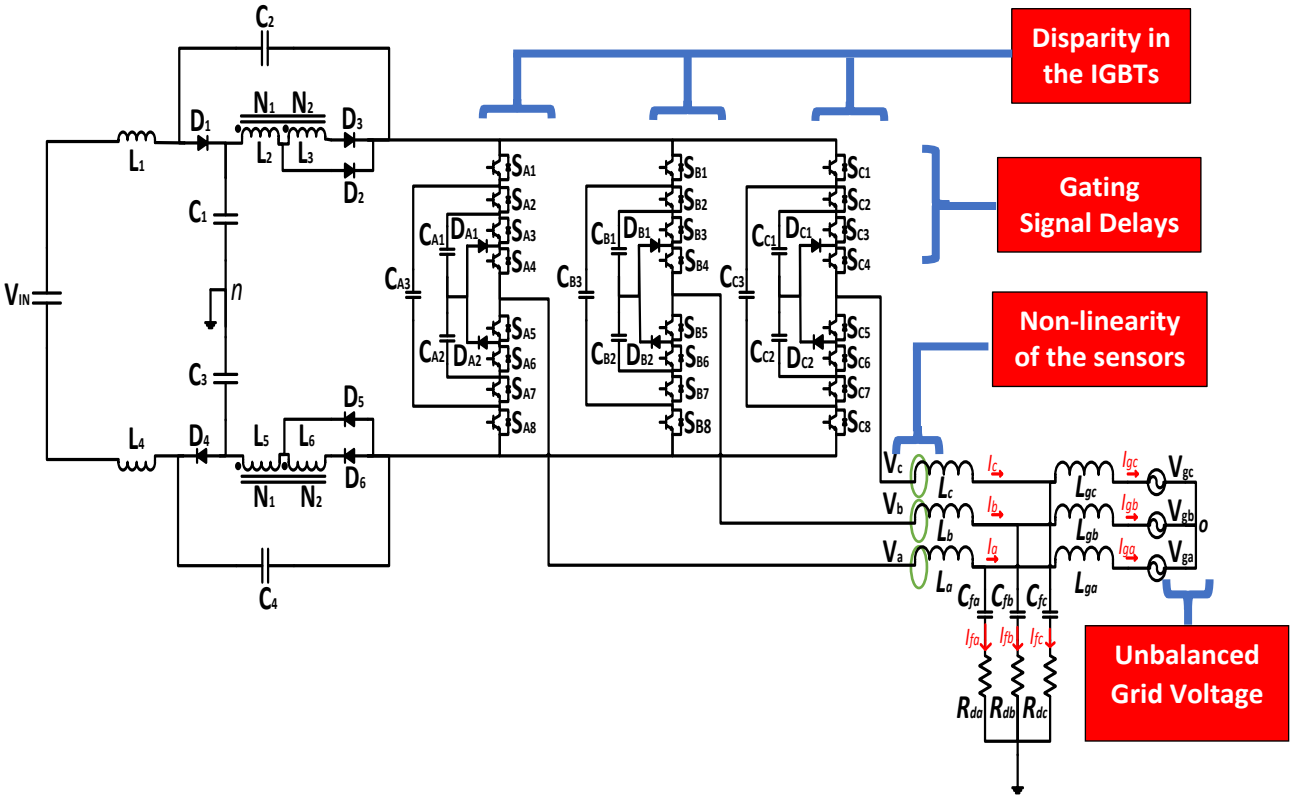


Figure 5.1: Sources of dc component in a grid-connected converter.

5.2. DC Component Generation Analysis

This section presents a detailed analysis of the generation of dc components from the asymmetrical characteristics of switching power semiconductor devices by considering the delay in the gating signals and disparity in the switching power semiconductor devices.

5.2.1. Delay in the Generated Gating Signals

A complementary switching pair of power semiconductor devices are controlled by the gating signals generated from the gate driver circuitry. Due to a certain level of imperfection in the gate driver circuitry, slight delays occur in the switching period of the power semiconductor devices [208].

The impact of the delay in generated gating signals is analyzed in a single phase of the proposed converter topology (i.e., phase A) (as shown in Figure 5.1) and switching state 1 (as stated in Table 4.1). During the switching state 1, S_{a1} to S_{a4} is switched on, and the average output voltage obtained at this switching instant is given as $\bar{V}_{ao} = V_{dc}/2$ at the positive half-cycle of the voltage waveform. The turn-on time associated with S_{a4} to S_{a1} within the switching period of state 1 is t_1, t_2, t_3, and t_4, respectively. Furthermore, a summation of the turn-on time of S_{a4} to S_{a1} is represented by $4t_U$ (i.e., $t_1 + t_2 + t_3 + t_4$) to simplify the analysis.

While at the negative half-cycle of the voltage waveform, $\underline{S_{a4}}$ to $\underline{S_{a1}}$ is switched on, and the converter output voltage is given as $\bar{V}_{ao} = -V_{dc}/2$, at the negative half-cycle of the voltage waveform. The turn-on time associated with $\underline{S_{a4}}$ *to* $\underline{S_{a1}}$ within switching period of state 1 are $\underline{t_1}, \underline{t_2}, \underline{t_3}$, and $\underline{t_4}$, respectively. Furthermore, a summation of the turn-on time of S_{a4} to S_{a1} is represented by $4t_L$ (i.e., $\underline{t_1} + \underline{t_2} + \underline{t_3} + \underline{t_4}$) to simplify the analysis.

Therefore, the average output voltage of phases B and C are similar to phase A. The line-to-line voltage for V_{ab}, V_{bc}, and V_{ca} can be obtained from the following set of equation [206]:

$$\begin{aligned} V_{ab} &= V_{ao} - V_{bo} \\ V_{bc} &= V_{bo} - V_{co} \\ V_{ca} &= V_{co} - V_{ao} \end{aligned} \tag{5.1}$$

Therefore, the converter output voltage per phase can be derived as follows:

$$V_{an} = V_{ao} - V_{no}$$

$$V_{bn} = V_{bo} - V_{no} \tag{5.2}$$

$$V_{cn} = V_{co} - V_{no}$$

Under balanced grid voltage conditions, the voltage between n and o (V_{no}) can be expressed in (5.3).

$$V_{no} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) \tag{5.3}$$

Therefore, $\bar{V}_{ao}$ in the positive half-cycle of the grid voltage waveform is expressed in (5.4) as follows:

$$\bar{V}_{ao} = \frac{V_{dc}}{2} \cdot \left(\frac{4t_U}{T_s}\right) - \frac{V_{dc}}{2} \cdot \left(\frac{T_s-(4t_L)}{T_s}\right) = i_{ga}^{+} + L \cdot \frac{di_{ga}^{+}}{dt} + V_{ga} + V_{no} \tag{5.4}$$

where V_{ga} is the grid voltage of phase A.

Therefore, the injected grid current in the positive half-cycle is obtained by solving (5.4) to get (5.5).

$$\overline{i_{ga}^{+}} = \int_0^{\frac{T_s}{2}} \frac{V_{dc}}{2LT_s} \cdot [(4t_U) - T_s + (4t_L)]dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{no}\, dt$$

$$= \frac{V_{dc}}{4L} \cdot [(4t_U) - T_s + (4t_L)] - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{36L} V_{dc} T_s \tag{5.5}$$

Therefore, $\bar{V}_{ao}$ in the negative half-cycle of the grid voltage waveform is expressed in (5.6) as follows:

$$\bar{V}_{ao} = -\frac{V_{dc}}{2} \cdot \left(\frac{4t_L}{T_s}\right) + \frac{V_{dc}}{2} \cdot \left(\frac{T_s-(4t_U)}{T_s}\right) = i_{ga}^{-} + L \cdot \frac{di_{ga}^{-}}{dt} + V_{ga} + V_{no} \tag{5.6}$$

Therefore, the injected grid current in the negative half-cycle is obtained by solving the equation (5.6) to get (5.7).

$$\overline{i_{ga}^{-}} = \int_0^{\frac{T_s}{2}} \frac{V_{dc}}{2LT_s} \cdot [-(4t_L) + T_s - (4t_U)]dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{no}\, dt$$

$$= \frac{V_{dc}}{4L} \cdot [-(4t_L) + T_s - (4t_U)] - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt + \frac{1}{36L} V_{dc} T_s \tag{5.7}$$

By adding (5.5) with (5.7), the phase current (i_{ga}) can be expressed in (5.8) as follows:

$$i_{ga} = \overline{i_{ga}^{+}} + \overline{i_{ga}^{-}} = -\frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{no}\, dt = -\frac{1}{L} V_{ga} T_s \tag{5.8}$$

The associated delays ($4\Delta t_U$) at the respective turn-on times ($4t_U$) is included in (5.4) and rewritten as (5.9). Furthermore, the delays are added into (5.6) and rewritten as (5.10).

$$\bar{V}_{ao} = \frac{V_{dc}}{2} \cdot \left(\frac{(4t_U)+(4\Delta t_U)}{T_s}\right) - \frac{V_{dc}}{2} \cdot \left(\frac{T_s-(4t_L)-(4\Delta t_U)}{T_s}\right) = i_{ga}^{+} + L \cdot \frac{di_{ga}^{+}}{dt} + V_{ga} + V_{no} \quad (5.9)$$

$$\bar{V}_{ao} = -\frac{V_{dc}}{2} \cdot \left(\frac{(4t_L)+(4\Delta t_L)}{T_s}\right) + \frac{V_{dc}}{2}\left(\frac{T_s-(4t_U)-(4\Delta t_L)}{T_s}\right) = i_{ga}^{-} + L \cdot \frac{di_{ga}^{-}}{dt} + V_{ga} + V_{no} \quad (5.10)$$

Therefore, the grid current (i_{ga}^{+}) in the positive half-cycle of the grid voltage, is expressed in (5.11).

$$\overline{i_{ga}^{+}} = \int_0^{\frac{T_s}{2}} \frac{V_{dc}}{2LT_s} \cdot [(4t_U) + (8\Delta t_U) - T_s + (4t_L)]dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{no}\, dt$$

$$= \frac{V_{dc}}{4L} \cdot [(4t_U) - T_s + (\,4t_L) + (8\Delta t_U)] - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{36L} V_{dc} T_s \quad (5.11)$$

Therefore, the grid current (i_{ga}^{-}) in the negative half-cycle of the grid voltage, is expressed in (5.12).

$$\overline{i_{ga}^{-}} = \int_0^{\frac{T_s}{2}} \frac{V_{dc}}{2LT_s} \cdot [-(4t_L) + (8\Delta t_L) + T_s - (4t_U)]dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{no}\, dt$$

$$= \frac{V_{dc}}{4L} \cdot [-(4t_L) + T_s - (\,4t_U) - (8\Delta t_L)] - \frac{1}{L}\int_0^{\frac{T_s}{2}} V_{ga}\, dt + \frac{1}{36L} V_{dc} T_s \quad (5.12)$$

By adding (5.11) with (5.12), the phase current (i_{ga}) can be expressed in (5.13) as follows:

$$i_{ga} = \overline{i_{ga}^{+}} + \overline{i_{ga}^{-}} = \frac{V_{dc}}{4L} \cdot [2(4\Delta t_U) - 2(4\Delta t_L)] - \frac{1}{L} V_{ga} T_s \quad (5.13)$$

Therefore, (5.13) can be simplified as (5.14).

$$i_{ga} = \frac{V_{dc}}{4L} \cdot [8(\Delta t_U - \Delta t_L)] - \frac{1}{L} V_{ga} T_s \quad (5.14)$$

From (5.14), i_{ga} will contain dc components if Δt_U is not equal to Δt_L (i. e. , $\Delta t_u \neq \Delta t_l$). However, if gating signals are without delays, Δt_U is equal to Δt_L ($\Delta t_U = \Delta t_L$) under this condition, the i_{ga} will not contain dc components.

5.2.2. Disparity in the Switching Power Semiconductor Devices

The switching power semiconductor devices in the converter topology have asymmetrical characteristics, such as voltage drop due to on-state resistance and leakage current [208]. Based

on switching state 1 (as highlighted in Table 4.1), the voltage drops across S_{a1} to S_{a4} in the positive half-cycle of the output waveform, and the voltage drops across S_{a5} to S_{a8} in the negative half-cycle of the output waveform, are considered for the analysis of the asymmetrical characteristics of switching power semiconductor devices.

The turn-on time of the power semiconductor devices in the positive half-cycle of the output waveform has been stated as $4t_U$ in the previous section. The turn-on time of the power semiconductor devices in the negative half-cycle of the output waveform has been stated as $4t_L$. Therefore, the voltage drops across S_{a1} to S_{a4} are represented by ΔV_{a1}, ΔV_{a2}, ΔV_{a3}, and ΔV_{a4} and the voltage drops across S_{a5} to S_{a8} are represented by ΔV_{a5}, ΔV_{a6}, ΔV_{a7}, and ΔV_{a8}. To further simplify the analysis, the voltage drops across S_{a1} to S_{a4} will be represented by $4\Delta V_U$ (i.e., ΔV_{a1} + ΔV_{a2} + ΔV_{a3} + ΔV_{a4}) and the voltage drops across S_{a5} to S_{a8} will be represented by $4\Delta V_L$ (i.e., ΔV_{a5} + ΔV_{a6} + ΔV_{a7} + ΔV_{a8}). Based on the presented assumptions, $\bar{V}_{ao}$ in the positive half-cycle of the grid voltage waveform is expressed in (5.15) as follows:

$$\bar{V}_{ao} = \frac{V_{dc}-4\Delta V_U}{2} \cdot \left(\frac{4\Delta t_U}{T_s}\right) - \frac{V_{dc}-4\Delta V_L}{2} \cdot \left(\frac{T_s-4\Delta t_L}{T_s}\right) = i_{ga}^{+} + L \cdot \frac{di_{ga}^{+}}{dt} + V_{ga} + V_{no} \qquad (5.15)$$

Therefore, $\bar{V}_{ao}$ in the negative half-cycle of the grid voltage waveform is expressed in (5.16) as follows:

$$\bar{V}_{ao} = -\frac{V_{dc}-4\Delta V_L}{2} \cdot \left(\frac{4\Delta t_L}{T_s}\right) + \frac{V_{dc}-4\Delta V_U}{2} \cdot \left(\frac{T_s-4\Delta t_U}{T_s}\right) = i_{ga}^{+} + L \cdot \frac{di_{ga}^{+}}{dt} + V_{ga} + V_{no} \qquad (5.16)$$

Also, (5.16) and (5.15) are combined to establish the relationship between i_{ga}, $4\Delta t_U$ and $4\Delta t_L$ is expressed in (5.17):

$$i_{ga} = \frac{1}{L}\int_0^{T_s}\left(\bar{V}_{ao} - V_{ga} - V_{no}\right)dt = \frac{1}{L}\int_0^{\frac{T_s}{2}}\left(\bar{V}_{ao} - V_{ga}V_{no}\right)dt + \frac{1}{L}\int_{\frac{T_s}{2}}^{T_s}\left(\bar{V}_{ao} - V_{ga}V_{no}\right)dt$$

$$\therefore, i_{ga} = \frac{1}{4}[4\Delta V_U(8\Delta t_U - T_s) + 4\Delta V_L(8\Delta t_L - T_s)] - \frac{1}{L}V_{ga}T_s \qquad (5.17)$$

From (5.17), the switching power semiconductor devices do not have similar characteristics, which results in i_{ga} containing dc components.

5.3. Comparison of DC component minimization methods

An overview of dc component minimization methods has been presented in [207], which only highlighted techniques applied to transformer-less grid-connected photovoltaic systems. The dc component minimization methods are classified into four main categories, namely: virtual capacitor concept [77], [82], [207], [210], dc-link sensing [83], [211], compensation method [208], [212], [213] and voltage filtering approach [214], [215], as illustrated in Figure 5.2.

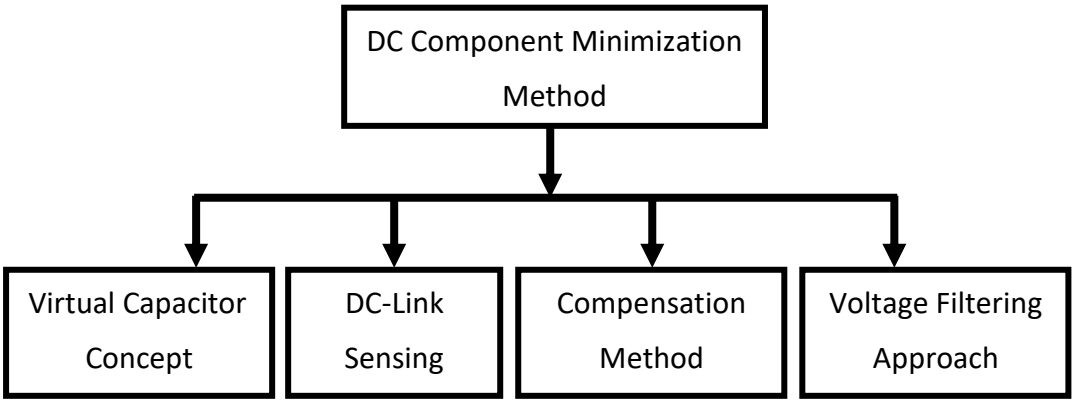


Figure 5.2: Classification of DC component minimization methods.

5.3.1. Classification

A. Virtual Capacitor Concept

The conventional method utilized to minimize dc component in a transformer-less configuration is through the insertion of an ac capacitor at the output of the converter topology [77], [82], [207], [210]. However, the capacitance value must be very high enough to block the low-frequency dc component [77]. The series-connected capacitor will reduce the overall dynamic response of the converter topology [77]. Therefore, the capacitor can be replaced by the virtual capacitor concept through an advanced control strategy [77]. However, the concept's effectiveness depends on the accuracy of the current sensor [82].

A. DC-Link Sensing Method

Also, the dc-link sensing method utilizes either the dc-link voltage ripples or the dc-link current to mitigate the dc component of the output current [82], [211]. It has been established that the dc component of the output current is indirectly proportional to the dc-link voltage ripple, which consists of the dc component, double line-frequency, and line-frequency components

[82]. The line-frequency component is utilized to detect the dc component injected by the converter [82]. Therefore, the line-frequency component of the dc-link voltage ripple is reinjected into the control loop through the developed indirect dc feedback loop to mitigate the DC component at the output current [82]. Furthermore, the line-frequency component of the dc-link current was extracted and feedforward to the current reference of the current control loop [211].

B. Compensation Method

A dc component compensation technique was proposed based on the adaptive backpropagation (BP) neural network proportional-integral-derivative (PID) controller [208]. The current reference of the control loop was divided into two main parts, with one part dedicated to tracking the output current of the control loop and the other devoted to dc component suppression control loop [208]. On the other hand, a current control algorithm based on the proportional resonant and repetitive controller was designed to mitigate the DC components in the output current in both [212] and [213].

C. Voltage Filtering Approach

The voltage filtering approach is based on detecting the dc component either from the output voltage or dc-link voltage [214], [215]. This approach is dependent on extensive hardware and digital filtering technique to extract the dc components [214], [215]. Mainly, the dc component is detected through a second-order RC low-pass filter or a combination of differential amplifier circuit with a first-order RC low-pass filter [214], [215]. While it is challenging to extract the dc component from the ac output voltage, [214] proposed a voltage filtering method using a first-order RC low-pass filter combined with a sample-based moving average filter (MAF). On the other hand, the method proposed in [215] consists of a hardware attenuation circuit (mainly; differential amplifier circuit and low-pass filter), an analogue-to-digital converter and a proportional-integral controller.

5.3.2. Comparative Evaluation

In Table 5.1, the main features of the discussed dc component minimization methods are compared based on the software detection method required to extract the dc component [77], [82], [207], [208], the additional hardware deployed to detect the dc component [213], [214], and the level of accuracy of the method [77]-[82], [207]-[215]. Both the virtual capacitor concept and dc-link sensing techniques require an additional dc component extraction

algorithm which introduces time-delay to dc component minimization method [77], [82], [207], [211]. Moreover, the accuracy of these methods is dependent on the linearity of the sensor, which is subject to gain-drift, as previously discussed [209]. Furthermore, the voltage filtering approach tends to have a better accuracy level than the other three counterparts due to the combination of hardware attenuation circuit and digital filtering technique [214], [215]. The voltage filtering approach detects and minimizes the dc voltage offset through an additional dc component suppression loop [214], [215].

Table 5.1: Comparison between dc component minimization methods

Method	Software-based Detection	Auxiliary Hardware	Level of Accuracy
Virtual capacitor concept	Yes	None	Moderate
DC-link sensing	Yes	None	Moderate
Compensation method	None	None	Moderate
Voltage filtering approach	None	Yes	High

5.4. Proposed DC Component Minimization Method

The proposed dc component minimization method presented in this section is based on a sensing and voltage measurement circuit with a digital notch filter technique. Therefore, the structure of the dc component minimization method is illustrated in Figure 5.3.

5.4.1. Sensing and Voltage Measurement Circuit

The dc component generated from the converter is detected through the output voltage measured from the converter midpoint to the output of each phase of the topology. The dc component was detected for the output voltage because of the converter's low output current in Chapter 4.

A voltage filtering approach has been presented in the literature to mitigate dc components in a grid-connected inverter [214]. A first-order low-pass filter was deployed to scale down the inverter output value to the microcontroller's low-voltage input range, which still requires an additional voltage measurement and isolation circuit, as stated in [214]. Therefore, this existing approach is a two-stage sensing and voltage measurement technique [214].

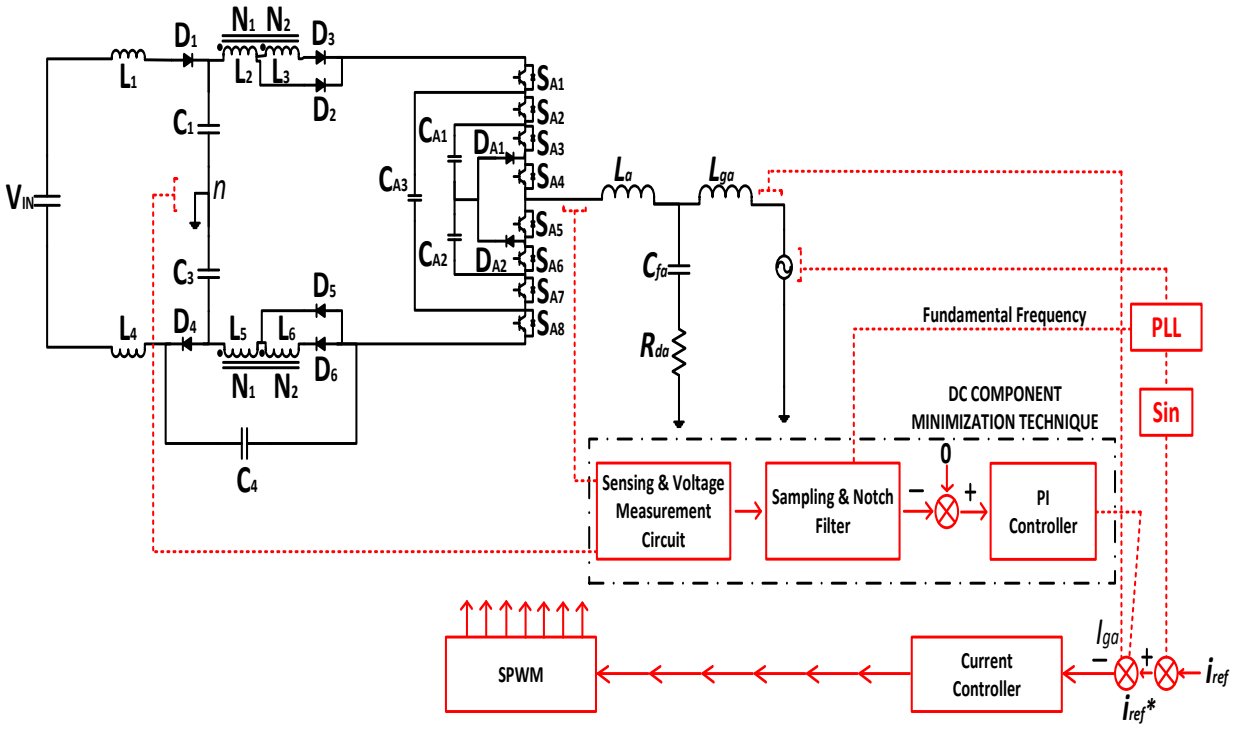
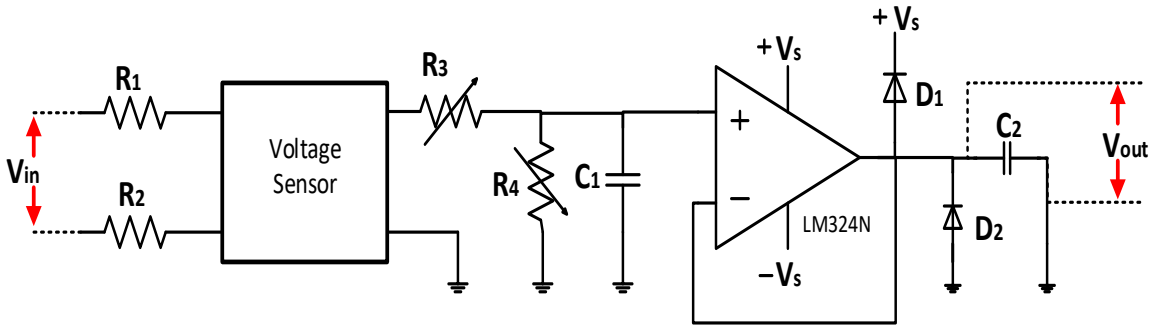
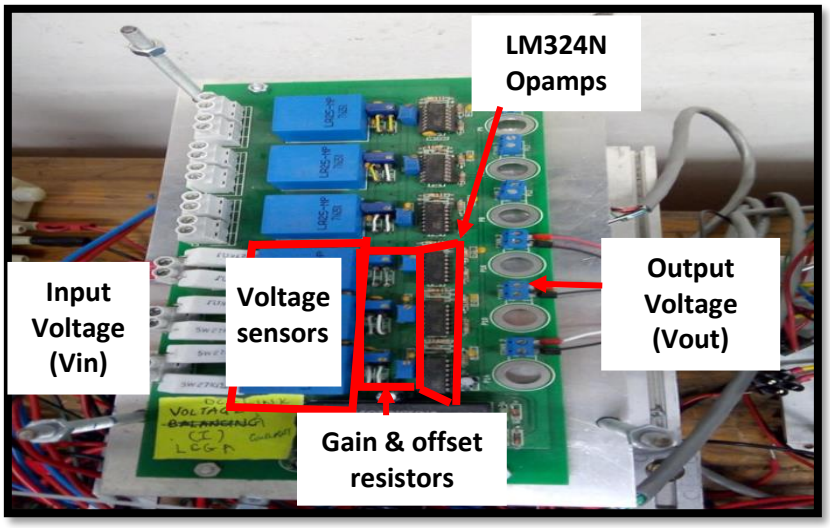


Figure 5.3: Diagram of the proposed dc component minimization technique.

The proposed method is based on a sensing and voltage measurement circuit that excludes the initial first-order low-pass filter. The main components of the circuit are three voltage transducers (LV-25P), six potentiometers and three LM234N quad-operational amplifiers, as shown in Figures 5.4(a) and 5.4(b). The voltage transducer measures the converter output voltage within the range of $10V$ to $500V$ per phase. An input resistor (R_1) is connected to the input side of the transducer to limit the input current and ensure the measured voltage corresponds to the nominal primary current of the transducer. The value of R_1 utilized in the circuit is $27k\Omega/\ 5W$, for a maximum measured voltage of $350V$. Furthermore, a potentiometer (R_3) is connected at the output of the transducer to adjust the scaling factor of the measured voltage, and the other potentiometer (R_4) is used to regulate the offset range of the measured voltage. The LM324N quad operational amplifier modifies the measured parameter for the input voltage range (within $+1V$ to $+10V$) of the data acquisition (DAQ) module, which provides the interface between hardware and the digital control algorithm.



(a)



(b)

Figure 5.4: Sensing and voltage measurement circuit. (a) schematic, (b) hardware.

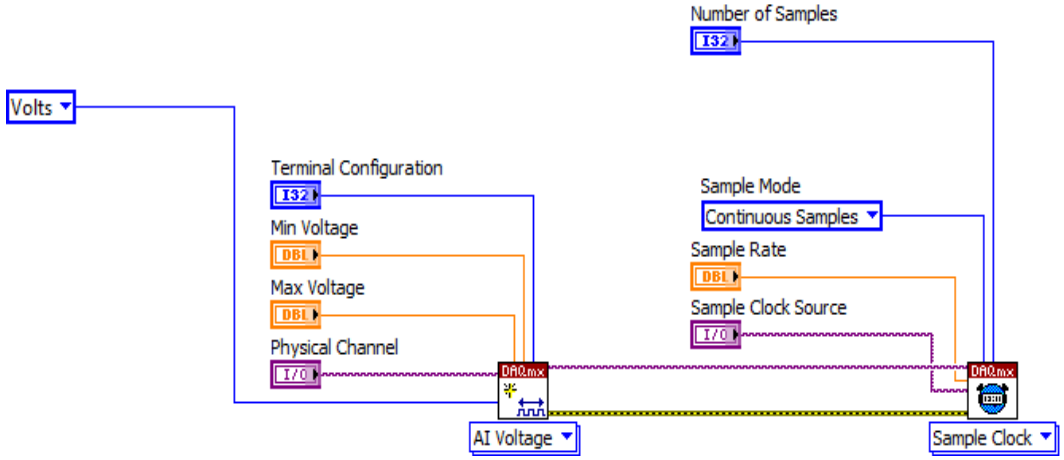
The converter's output voltage measured and detected by the sensing and voltage measurement circuit consists of both ac and dc components, as expressed in (5.18).

$$V_{xn}(t) = V_{ac}(t) + V_{dc} \tag{5.18}$$

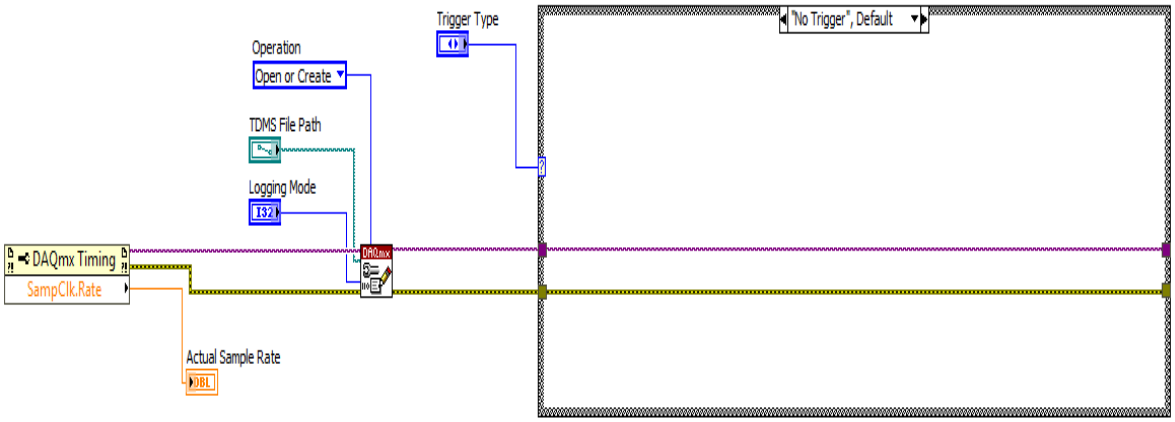
where, V_{xn} is the output phase voltage of the converter, V_{ac} is the ac component of the output voltage, and V_{dc} is the dc component of the output voltage.

The sampling of the measured output phase voltage of the converter is carried out digitally within the LabVIEW RT environment in three stages, namely: channel and timing setting, triggering setting, and data acquisition, as illustrated in Figures 5.5(a) to 5.5(e). The channel and timing setting establishes the sensing and voltage measurement circuit connected to the DAQ module via the SCB-68A interface board (as mentioned in Chapter 4). The triggering

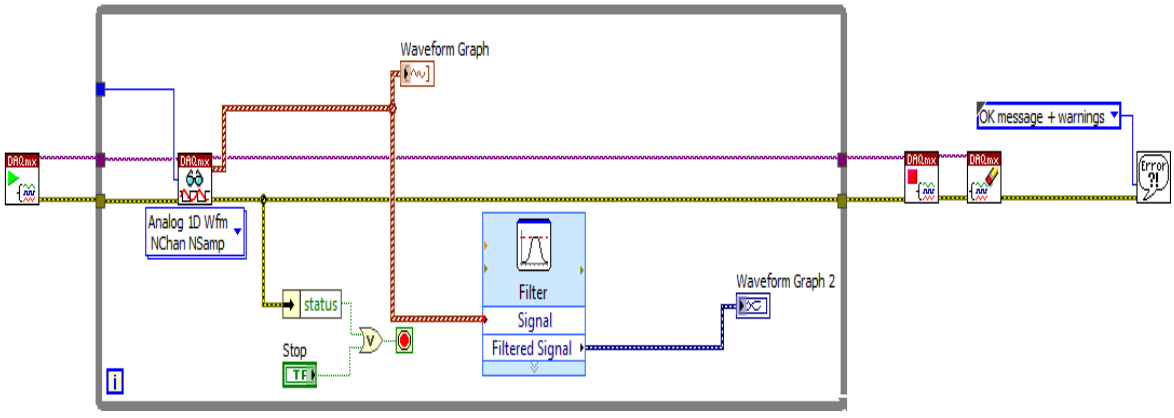
setting activates the A/D conversion immediately after the measured voltage is sampled. Furthermore, the measured voltage is acquired through the read and write control operation in the While Loop structure and attenuated, as shown in Figure 5.5(d). Also, the attenuated voltage is further filtered through a digital low-pass filter, as shown in Figure 5.5(e).



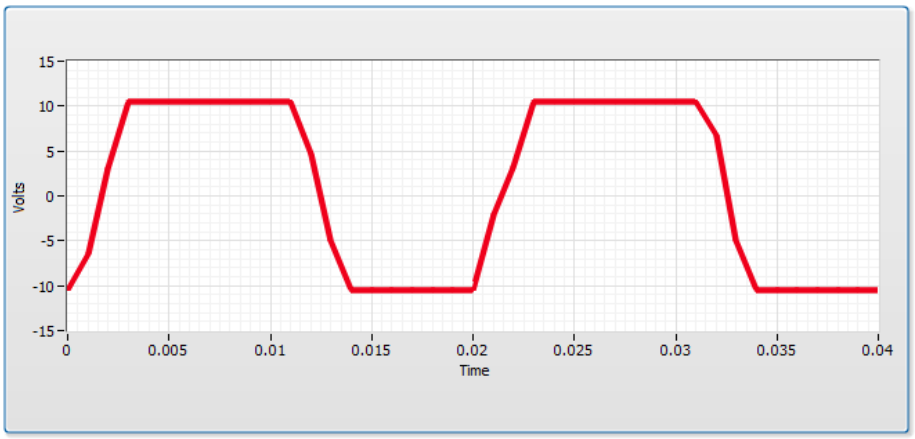
(a)



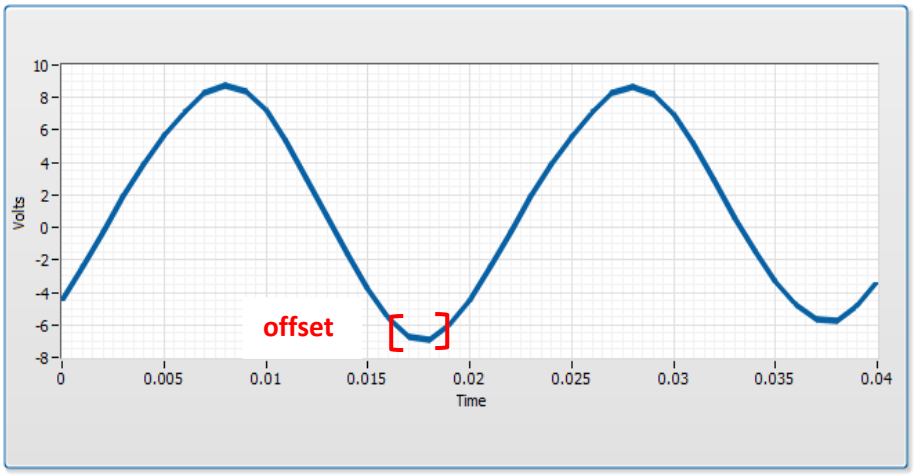
(b)



(c)



(d)



(e)

Figure 5.5: Sampling stages of the measured output voltage in LabVIEW RT. (a) channel and timing setting, (b) triggering settling, (c) data acquisition, (d) attenuated measured voltage, (e) filtered attenuated measured voltage.

5.4.2. Notch Filter

The second stage of the presented dc component elimination technique is based on a band rejection filter that attenuates the signal from the sensing and voltage measurement board within a specific frequency band. The band rejection filter deployed is a notch filter, as stated with the transfer function in (5.19) [216].

$$NF(s) = \frac{s^2+\omega_{NF}^2}{s^2+(\omega_{NF}/Q)s+\omega_{NF}^2} \tag{5.19}$$

where, ω_{NF} is the notch frequency, and Q is the damping factor.

Figure 5.6 shows the frequency response of $NF(s)$ with five different values of Q. The $NF(s)$ provides reasonable attenuation within a narrow frequency band, which implies $\omega_{NF} = 2\pi 50$ rad/s for the dc component sensed at the fundamental frequency. Furthermore, the value of Q is selected based on the expected variations at the fundamental frequency [216]. Therefore, the value of Q is selected to be 0.8, which makes the bandwidth of the notch filter is $\left(\frac{50}{0.8}\right) Hz$ [216]-[218].

Therefore, the open-loop transfer function can be expressed as follows in (5.20).

$$G_{ol}(s) = \frac{s^2+\omega_{NF}^2}{s^2+(\omega_{NF}/Q)s+\omega_{NF}^2} \cdot \left(\frac{k_p}{s} + \frac{k_i}{s^2}\right) \tag{5.20}$$

Based on the symmetrical optimum method, values of k_p and k_i are obtained from (5.21).

$$k_p = Q\omega_{NF}/b;\ k_i = (Q\omega_{NF})^2/b^3 \tag{5.21}$$

where b is a design constant based on the trade-off between transient and stability of the controller [218]. Therefore, $k_p = 104.73$, and $k_i = 4570$.

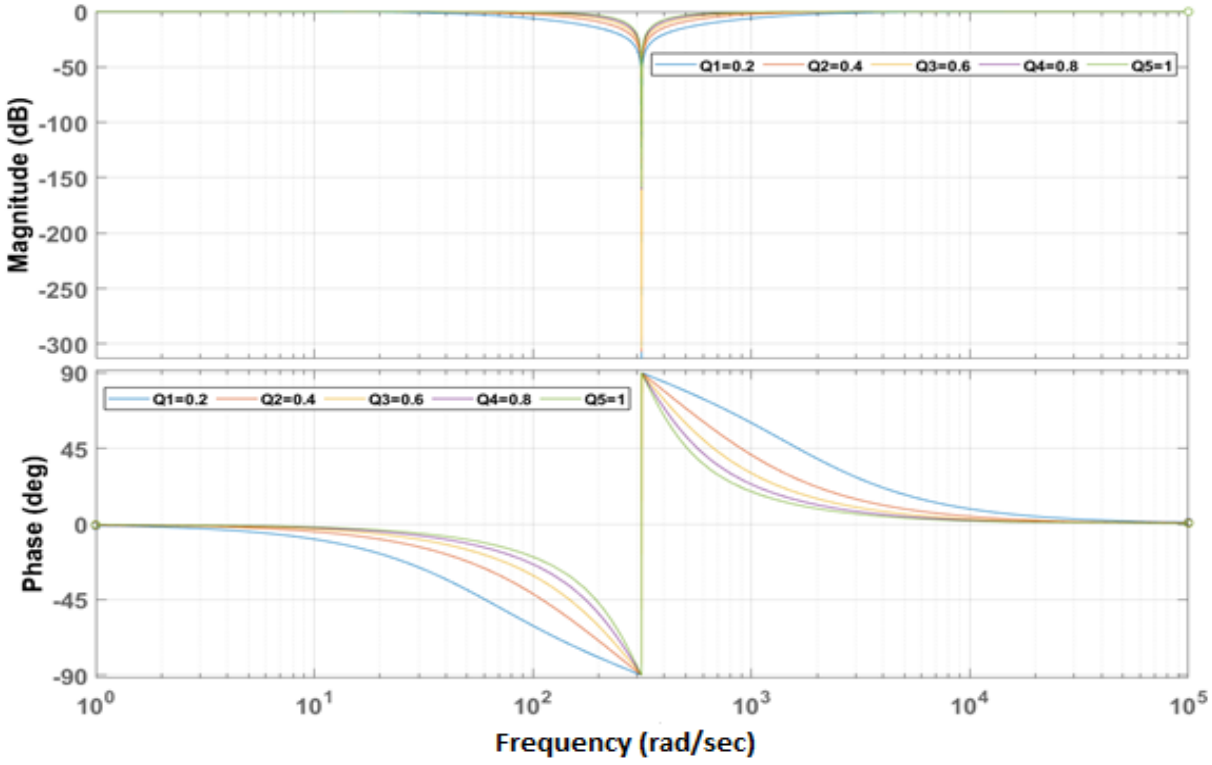
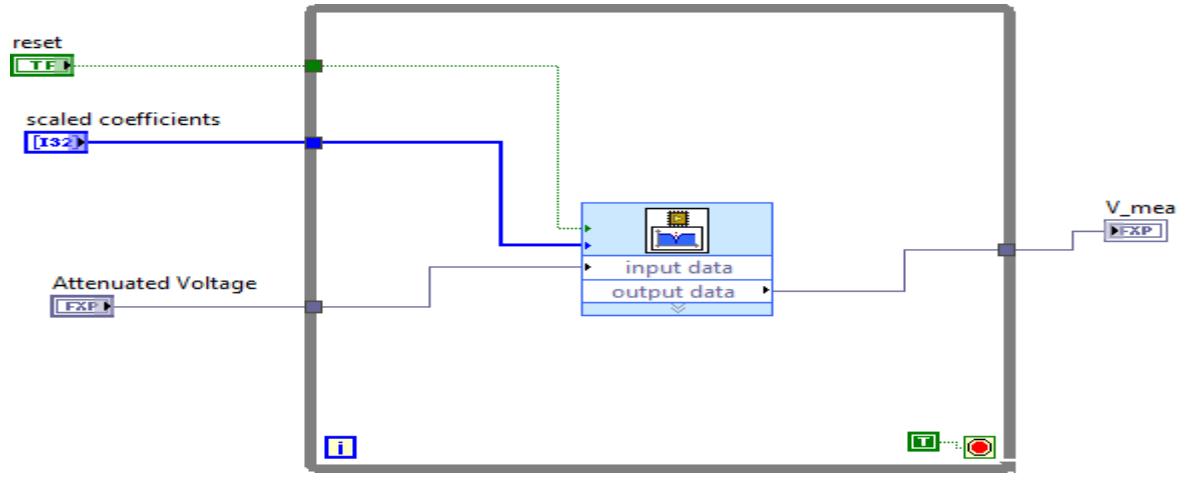
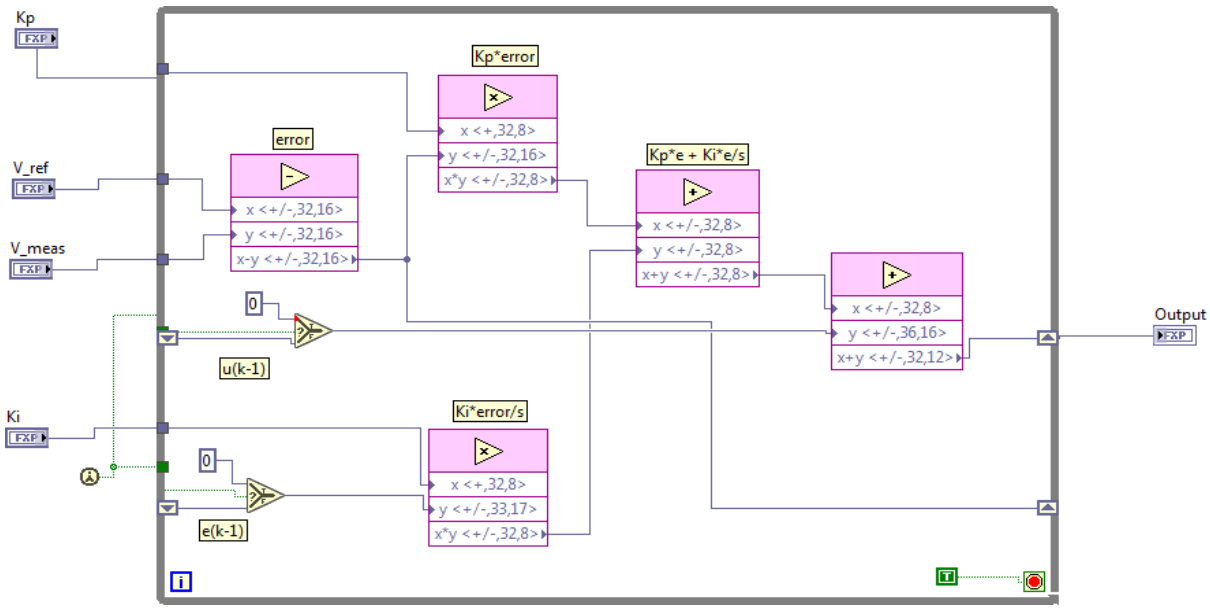


Figure 5.6: Frequency response of the notch filter.

The notch filter and PI controller of the dc component minimization technique implemented within the LabVIEW RT environment are shown in Figures 5.7(a) and 5.7(b). The attenuated voltage measured (described in Section 5.4.1 and illustrated in Figure 5.3) is fed into the notch filter with a Q factor of 0.8 (scaled coefficient), as shown in Figure 5.7(a). Furthermore, the output of the notch filter is fed into the PI controller (shown in Figure 5.7(b)), the values of the proportional (k_p) and integral (k_i) gains have been stated previously.



(a)



(b)

Figure 5.7: Second stage of dc component minimization technique in LabVIEW RT. (a) notch filter, (b) PI controller.

5.5. Results and Discussions

The prototype of the converter topology and system parameters presented in Chapter 4 has been utilised to validate the effectiveness of the proposed dc component minimisation technique. The results and discussions are presented in two categories: asymmetrical switching characteristics of the power semiconductor devices and FFT analysis of the output voltage and output current waveform.

5.5.1. Asymmetrical Switching Characteristics

The gating signal waveforms associated with the four pairs of switching power semiconductor devices in a single phase of the proposed converter topology is shown in Figures 5.8(a) to (d). The waveforms obtained from the output-side of the gate driver circuitry represents the gating signals that directly control the switching power semiconductor devices. From the analysis presented in Section 5.2, the gating delays in the circuitry contributes to the nonlinearities in the switching power semiconductor devices in theory. By observing the actual generated gating signals driving the power semiconductor devices, causes of asymmetrical switching can be established.

Figure 5.8(a) shows the complementary switching pair of S_{x1} and S_{x8} power semiconductor devices; with the high switching-side being S_{x1} and the low-side being S_{x8}. These complementary switching pair are the two outermost switching power semiconductor devices connected via a clamping capacitor (V_{cx3}). The difference in rising and fall times of the complementary pair is illustrated in Figure 5.8(a). Furthermore, the complementary switching pair of S_{x2} and S_{x7} show that the asymmetrical switching nature of the power semiconductor is affected by the series-connected clamping capacitor between the switching pair, as shown in Figure 5.8(b). Therefore, the clamping device between a complementary switching pair of a converter is a source of dc component. There is a direct correlation between the clamping capacitor and the dc component generated by a transformer-less converter topology [82], [83].

Based on the relationship between the current flowing through the clamping capacitor $(I_{cx}(t))$, the switching function of the complementary switching pair $(S_c(t))$ and grid-side current $\left(I_{gx}(t)\right)$, the dc component generated is analyzed in (5.22) to (5.26) [83]:

$$I_{gx}(t) = I_{ac}\cos(\omega_0 t + \theta_c) + I_{dc} \tag{5.22}$$

$$S_c(t) = m_a \cos\left(\omega_0 t + \theta_f\right) \tag{5.23}$$

$$I_{cx}(t) = I_{gx}(t) \cdot S_c(t) \tag{5.24}$$

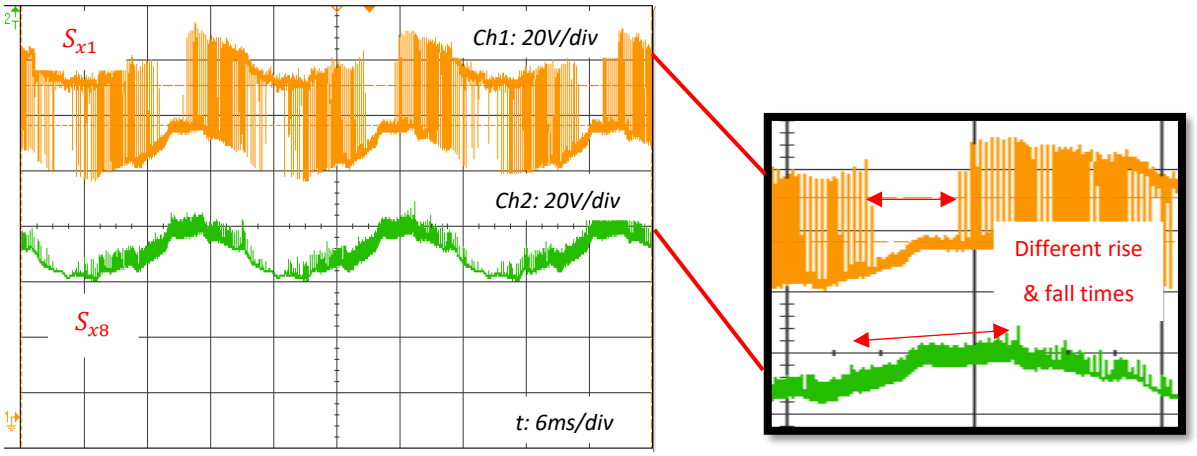
Therefore,

$$I_{cx}(t) = [I_{ac}\, cos(\omega_0 t + \theta_c) + I_{dc}] \cdot \left[m_a \cos\left(\omega_0 t + \theta_f\right)\right] \tag{5.25}$$

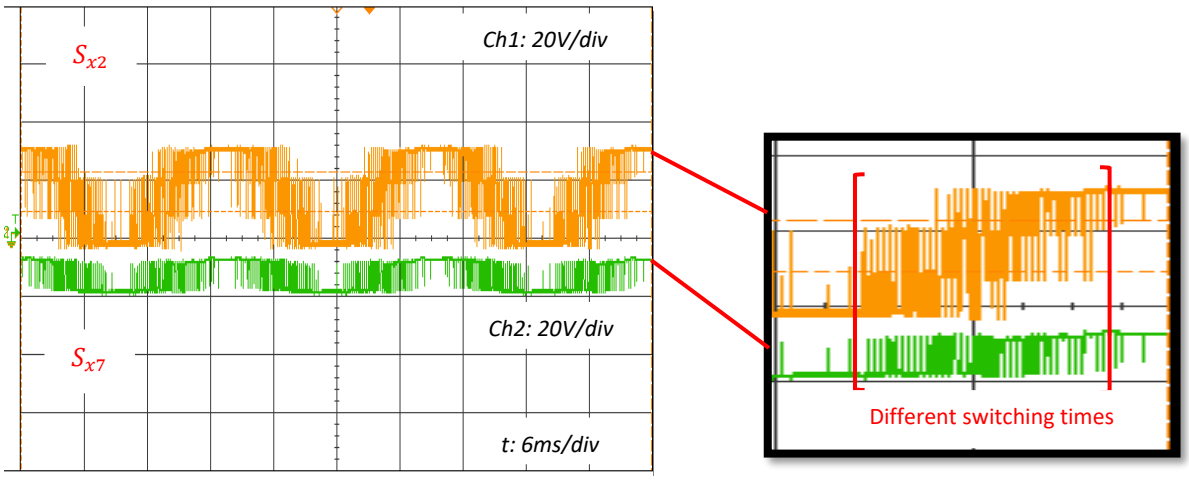
$$I_{cx}(t) = \frac{I_{ac} m_a}{2}\left[\cos\left(\theta_c - \theta_f\right) + cos\left(2\omega_0 t + \theta_c + \theta_f\right)\right] + I_{dc} m_a\, cos\left(\omega_0 t + \theta_f\right) \tag{5.26}$$

where, I_{ac} is the ac component of the grid current, I_{dc} is the dc component of the grid current, ω_0 is the angular frequency of the grid, θ_c is the phase angle of the output current, θ_f is the phase angle of the fundamental component of the switching function, and m_a is the modulation index of the switching function.

Therefore, the complementary switching pairs of S_{x2} and $\underline{S_{x1}}$, and S_{x1} and $\underline{S_{x2}}$ shows different asymmetrical switching characteristics due to the clamping capacitors and clamping diodes between the power semiconductor devices, as shown in Figures 5.8(c) and 5.8(d).



(a)



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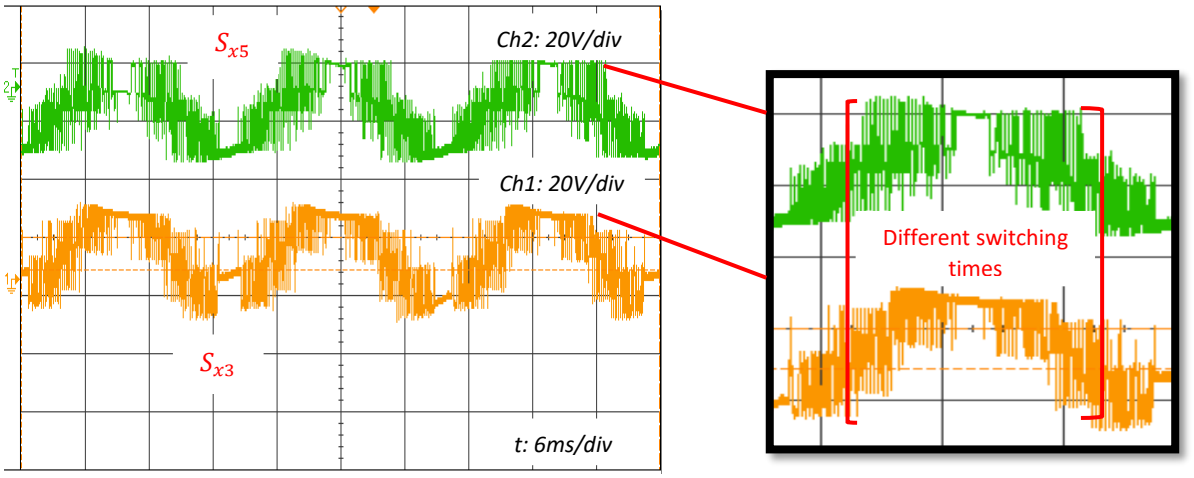
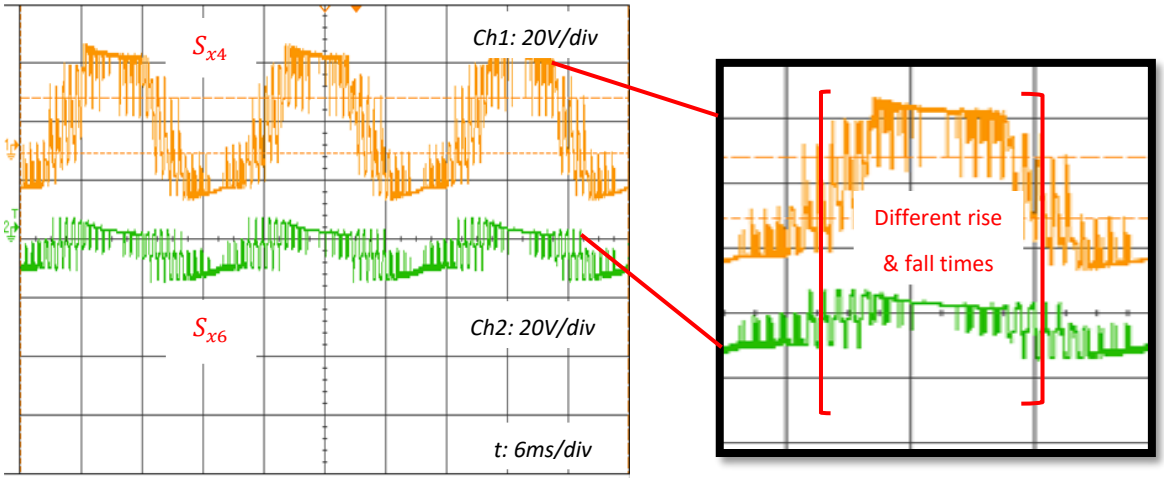


(c)

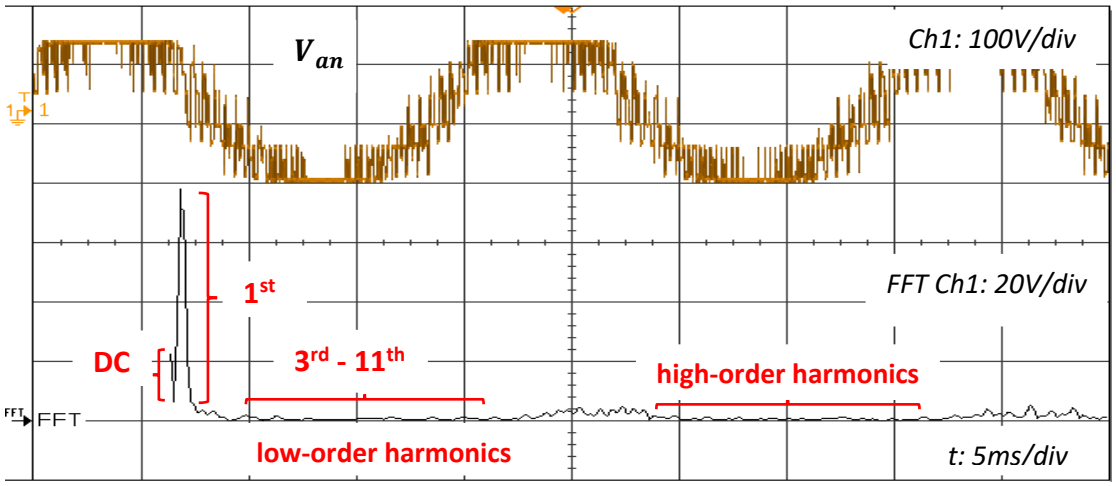


(d)

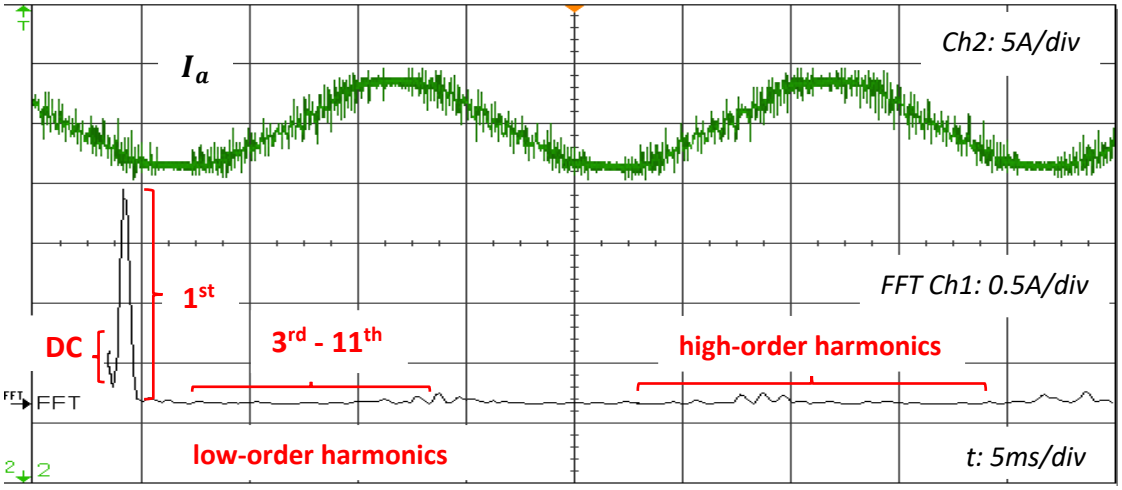
Figure 5.8: Asymmetrical switching characteristics of the complementary switching pair. (a) S_{x1} & S_{x8}, (b) S_{x2} & S_{x7}, (c) S_{x3} & S_{x5}, (d) S_{x4} & S_{x6}.

5.5.2. FFT Analysis

The experimental set-up is operated from a $100V$ input voltage at $5kHz$ switching frequency, generating about 2.5A RMS current injected into the grid. The experimental setup parameters have been presented in Chapter 4, and its main components are discussed in Chapter 6. Figures 5.9(a) and 5.9(b) show the converter output voltage and current phase A of converter topology detected and measured before the grid-side filter topology. Furthermore, the FFT spectrum of the inverter output voltage and current shows the dc components, low-order harmonics, and high-order harmonics of the respective waveforms in Figures 5.9(a) and 5.9(b).



(a)



(b)

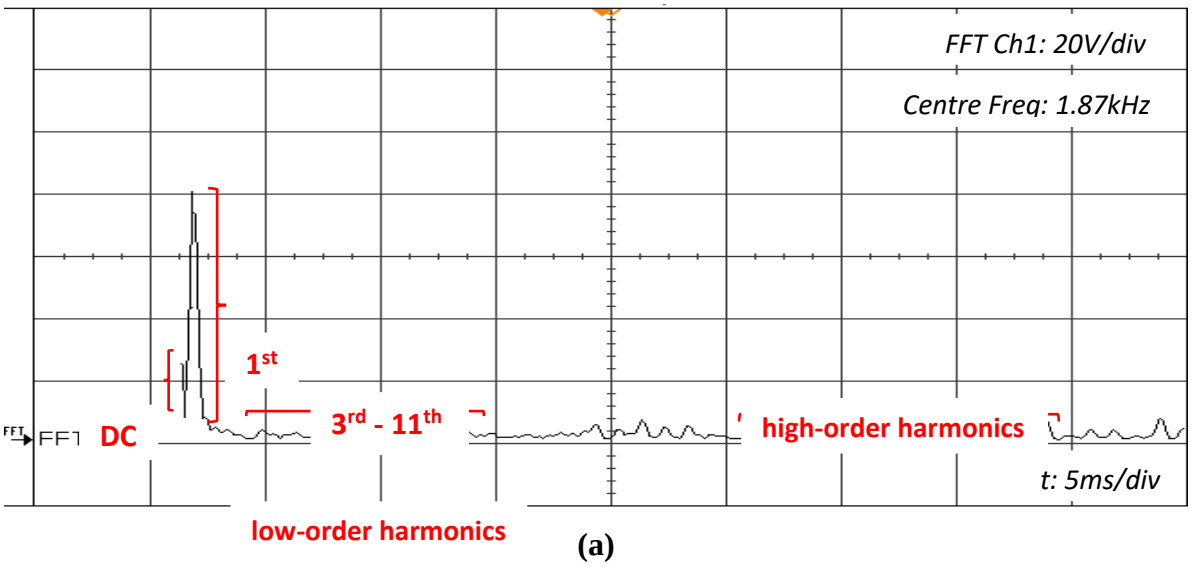
Figure 5.9: FFT spectrum of the converter output voltage and current. (a) the converter output voltage, (b) converter output current.

Furthermore, the FFT spectrum of the phase and line voltage of the converter topology highlighting their frequency components are shown in Figures 5.10(a) to 5.10(d). Figures 5.10(a) and 5.10(c) depicts the FFT spectrum of the phase and line voltage before the proposed dc component minimization technique was applied. Furthermore, a dc component minimization technique using the presented sensing and voltage measurement circuit with a sample-based moving average filter (MAF) shows a reduced dc component in the FFT spectrums of Figures 5.10(b) and 5.10(d). The effectiveness of this technique is minimized due to the reduced window frequency of the MAF because of the switching frequency(f_{sw}) of the

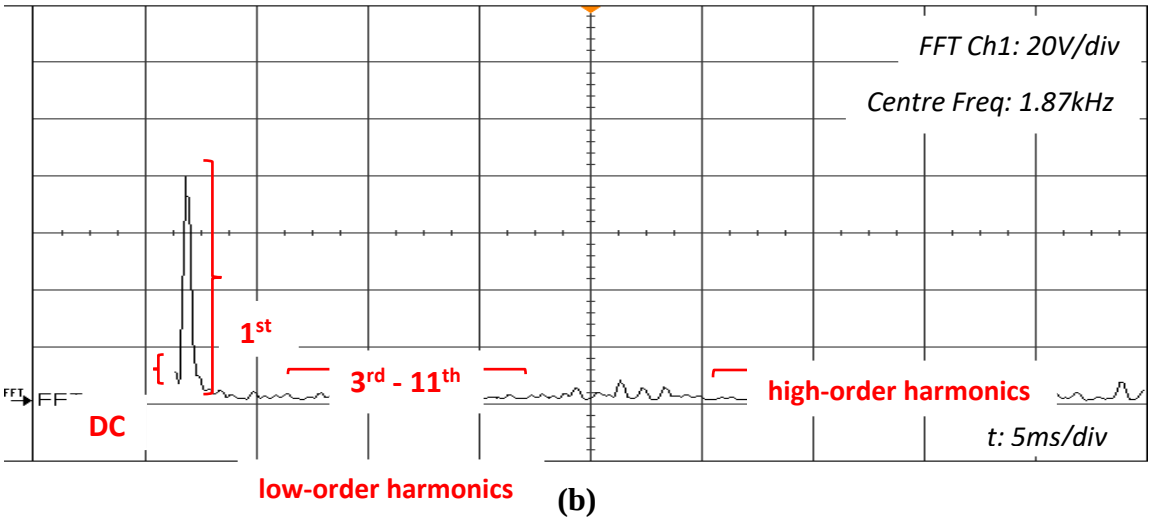
converter, which reduces its number of samples (N_{samp}) over the grid frequency (f_g). Therefore, N_{samp} is obtained using (5.27) as follows:

$$N_{samp} = \frac{f_{sw}}{f_g} \tag{5.27}$$

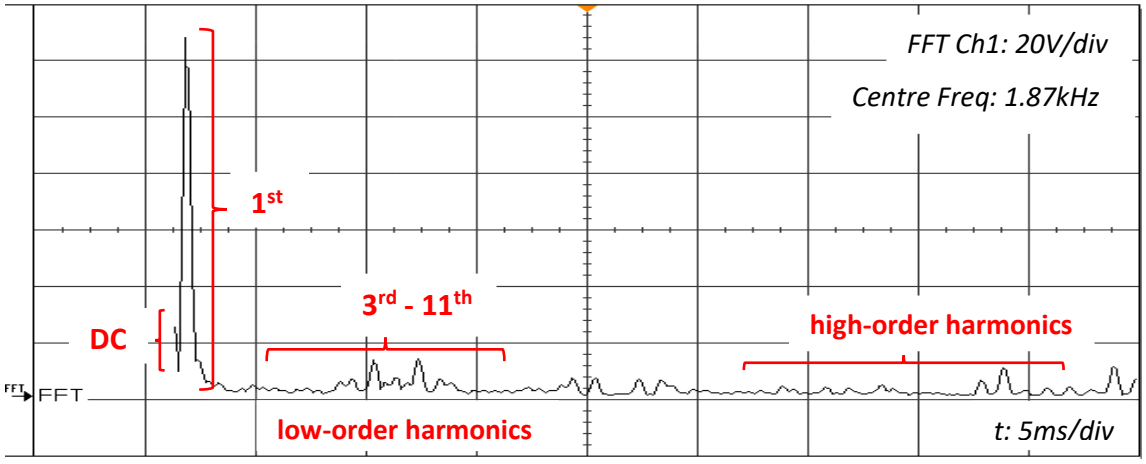
Figures 5.11(a) and 5.11(b) shows the dc component present in the converter output voltage and the output current has been further reduced. By adding the extracted dc component into the current reference of the current controller, the dc component at the output voltage and output current is almost zero. The impact of the proposed dc component minimization technique on the converter topology during an unbalanced grid voltage scenario is discussed in Chapter 6.



(a)



(b)



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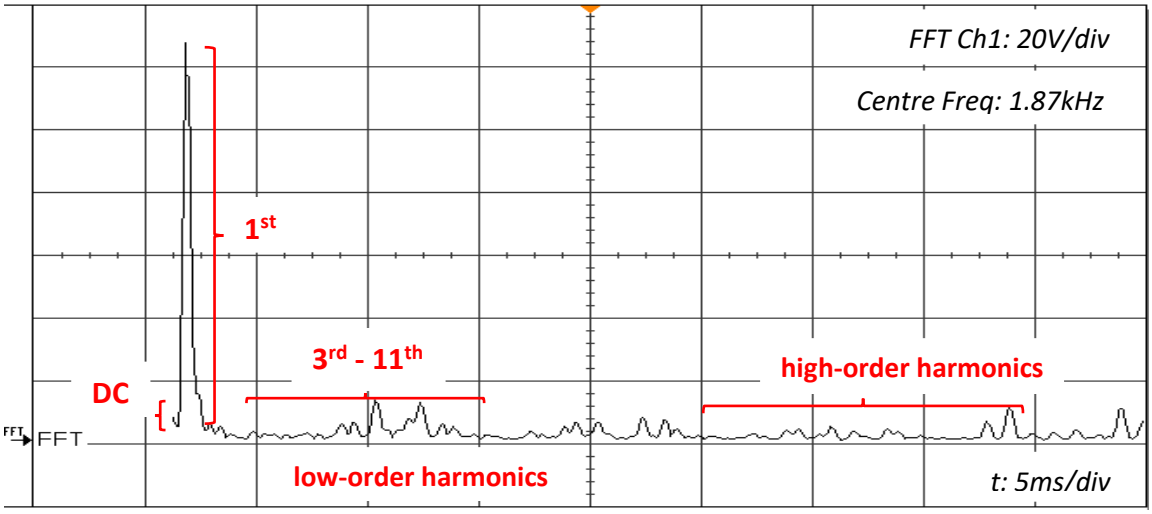
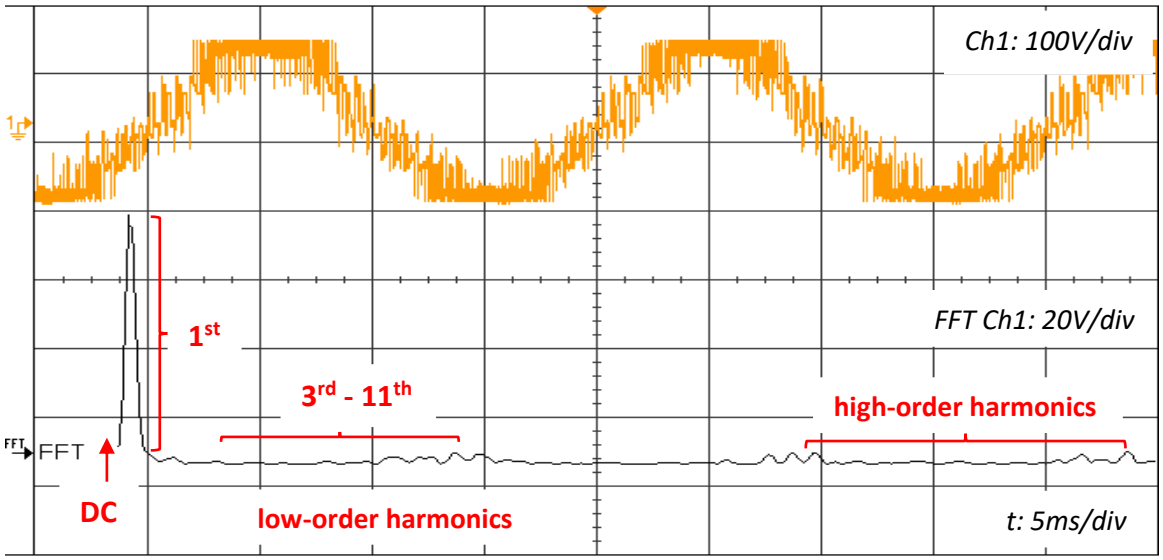
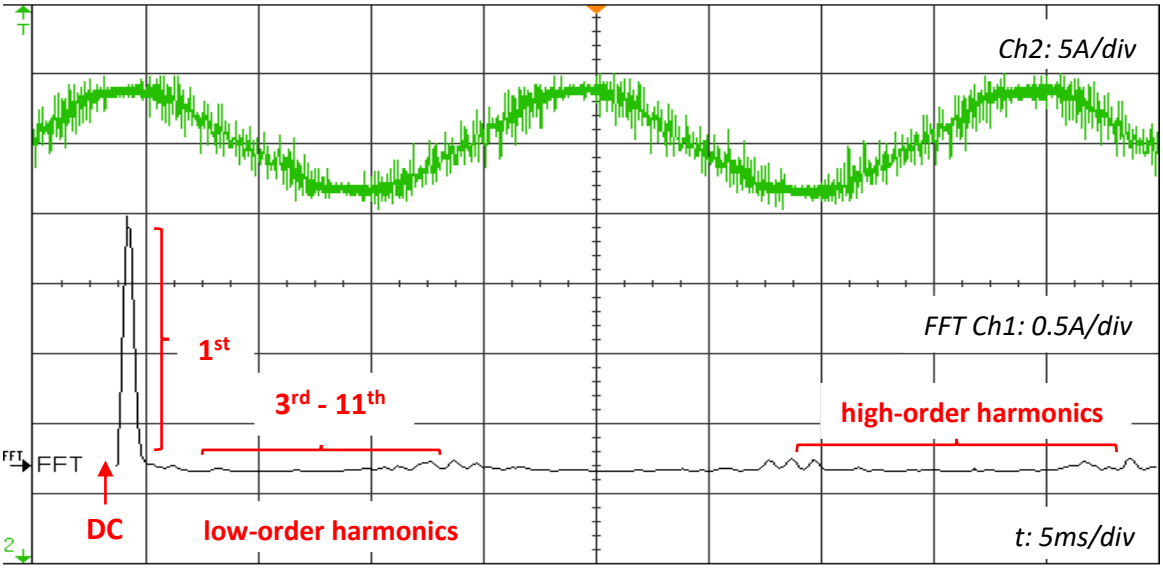


(d)

Figure 5.10: FFT spectrum of the phase and line voltage. (a) phase voltage without dc component minimization technique, (b) line voltage without dc component minimization technique, (c) phase voltage with dc component minimization technique using MAF, (d) line voltage with dc component minimization technique using MAF.



(a)



(b)

Figure 5.11: FFT spectrum of the converter output voltage and current with the proposed dc component minimization technique. (a) phase voltage (b) output current.

5.6. Conclusion

In this chapter, the modified voltage filtering dc component minimization method is presented. The significant contributions of the work carried out in this chapter are summarized as follows:

- The theoretical analysis of the dc component generated because of the asymmetrical switching characteristics of the power semiconductor devices in the proposed converter topology. The two main factors considered are the delay in gating signals and disparity in the switching power semiconductor devices.
- A comparative evaluation of the existing dc component minimization techniques has been presented in Section 5.3. The classification and comparative assessment of the dc component minimization techniques.
- The theoretical analysis, design and development of the proposed modified voltage filtering dc component minimization technique were presented. Therefore, the FFT spectrum of the inverter voltage and inverter current have been analysed without the proposed dc component minimization technique and with the proposed dc component minimization technique.

Chapter 6

Prototyping, Grid Connection and Analysis

This chapter presents the prototyping, grid connection and analysis of the proposed converter topology within the developed power hardware-in-loop (PHIL) configuration. The hardware and software components of the PHIL configuration is discussed extensively, and their respective functions are highlighted. The procedure for obtaining experimental parameters is discussed extensively. Furthermore, practical implementation-related issues are discussed, and the necessary considerations carried out are highlighted. The acquired waveforms have been obtained in the LabVIEW real-time (RT) environment. Furthermore, the efficiency, loss distribution, and cost analysis of the proposed converter topology are evaluated and compared with the conventional converter topology.

6.1. Overview of Experimental Test Bench

In Figure 6.1, the entire experimental test bench for the proposed converter topology is depicted. Based on the hardware components illustrated, a brief description of the functionality of each component is stated as follows:

- Each measurement board consists of three voltage transducers and current transducers for real-time voltage and current measurements.
- All the system operations presented in previous chapters are carried out through a National Instrument (NI) PXI system, which is a PXIe-1071 chassis consisting of an embedded controller (NI-PXIe-8840), field-programmable gate array (FPGA) module (NI-PXI-7842R) and data acquisition (DAQ) module (NI-PXIe-6363).
- NI-PXI-7842R and NI-PXIe-6363 modules are connected to the gate driver circuitry and measurement boards through an SHC68-68-RMIO shielded cable reconfigurable multifunctional input/output (RMIO) connector and an SCB-68A interface board.
- The 3ph 5L-NNPC converter circuitry is developed on three separate PCB boards, with each board representing a phase of the converter. Each single-phase consists of four

gate driver circuitry boards. The qZS network front is connected between the dc-link supply and the 3ph 5L-NNPC converter topology.

- A high-order grid filter based on the LCL topology was utilized to mitigate the switching harmonics from the converter topology. A passive damping technique was implemented to minimize the resonance frequency.

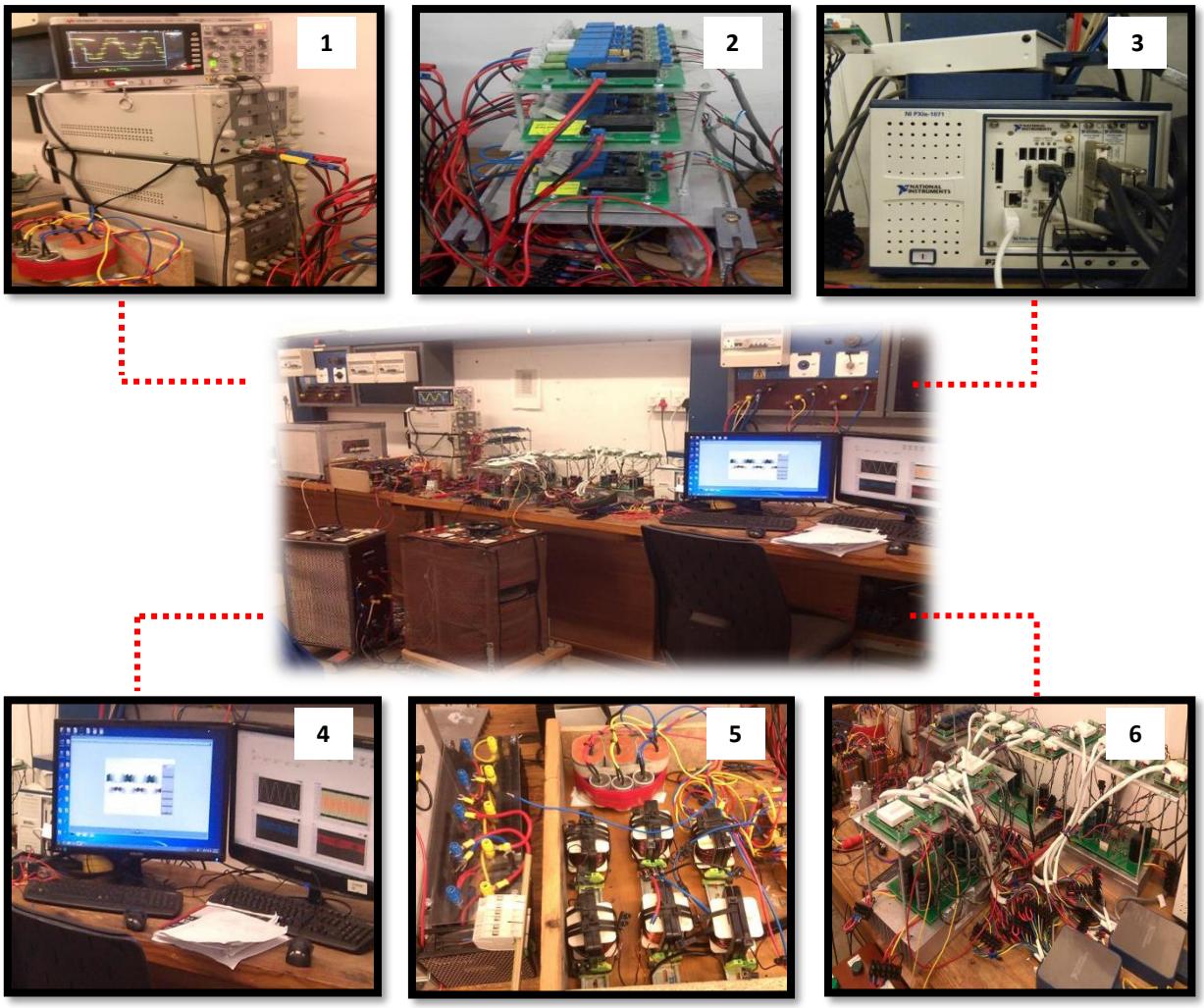


Figure 6.1. Overall experimental set-up: (1) digital oscilloscope and power supplies, (2) measurement boards, (3) NI PXI system, (4) Host PC, (5) high-order grid filter and (6) three-phase converter topology.

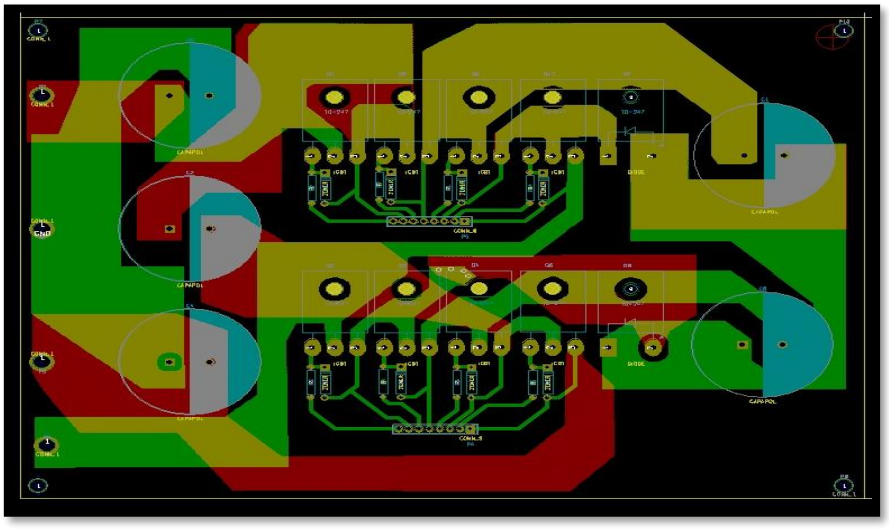
6.2. Prototyping

This section presents the prototyping process of the converter circuitry, gate circuitry, measurement board circuitry and LCL filter deployed in the experimental test bench.

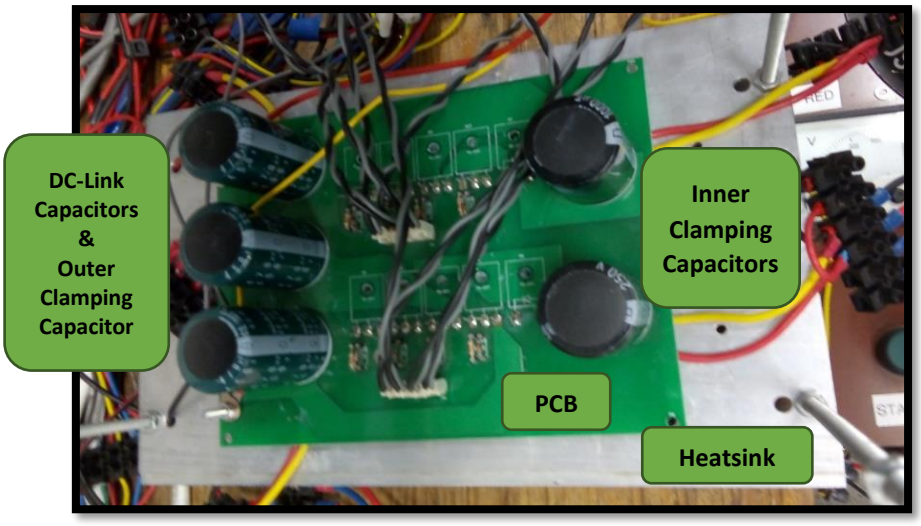
6.2.1. Converter Circuitry

The design of the tapped inductor quasi-Z-source network front-end of the converter topology has been discussed extensively in Chapter 4. Therefore, the prototyping process of the back end (i.e., 3ph 5L-NNPC converter) of the converter topology is presented in this section. The converter circuitry is developed based on a modular approach with each phase built on an individual PCB layout, as illustrated in Figures 6.2(a) to 6.2(c). Furthermore, the converter circuitry's schematic diagram developed within the KiCAD EDA environment is found in Appendix D.2.

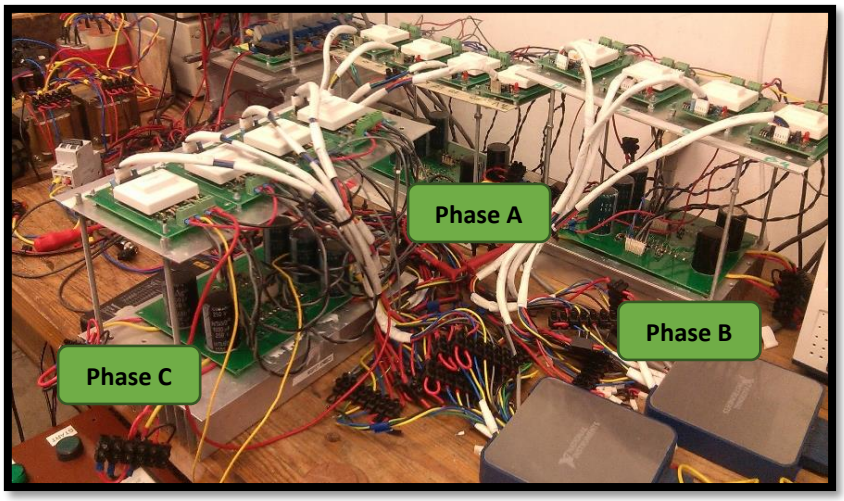
Each phase consists of two dc-link capacitors rated at $470\mu F/470V$, an external clamping capacitor rated at $470\mu F/470V$, two inner clamping capacitors rated at $1000\mu F/250V$, eight 47N60C3 switching power semiconductor devices (rated at $650V/47A$), and two IDP30E65D1 clamping diodes (rated at $650V/30A$). The switching power semiconductor devices and clamping diodes were selected based on the defined operation parameters of the topology. The datasheet of the switching power semiconductor devices is found in Appendix D.3. Each phase of the 5L-NNPC converter circuitry is developed on a multi-layered PCB shown in Figure 6.2(a). A single-phase and three-phase 5L-NNPC converter topology is depicted in Figures 6.2(b) and 6.2(c), respectively.



(a)



(b)



(c)

Figure 6.2: 5L-NNPC converter circuitry. (a) multi-layered PCB, (b) single-phase converter circuitry, (c) three-phase converter circuitry.

6.2.2. Gate Driver Circuitry

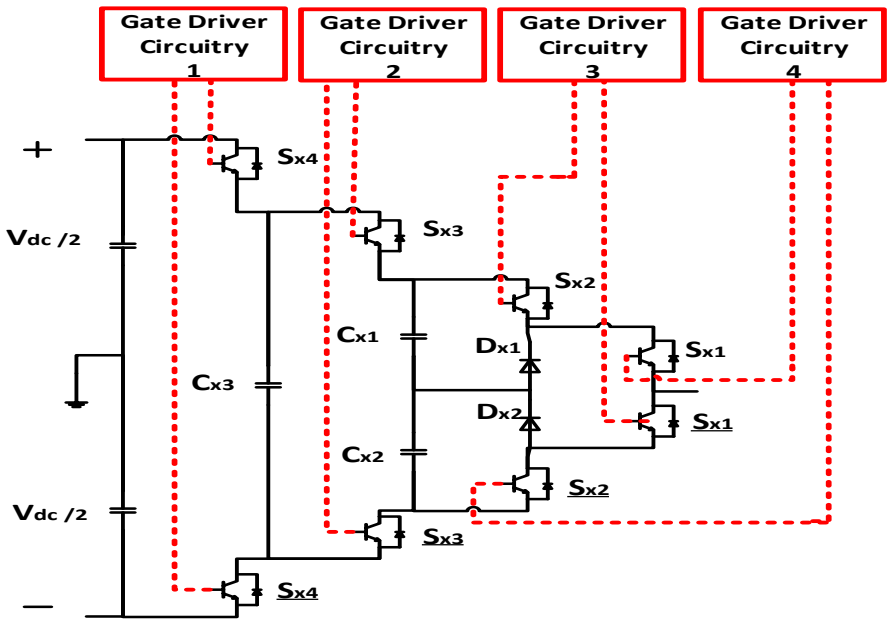
Each phase of the converter topology consists of four gate driver circuits, as illustrated in Figures 6.3(a) and 6.3(b). Furthermore, the schematic diagram of the gate driver circuitry is found in Appendix D.4. The main component of the gate driver circuitry is the Semikron SKHI22AH4R. Therefore, the Semikron SKHI22AH4R driver boards are used to generate gating signals for a pair of switching power semiconductor devices (datasheets of the SKHI22AH4R is found in Appendix D.5). The PCB of the gate driver circuitry is shown in Figure 6.4(a).

The main features and functionality of the gate driver circuitry with its built-in protection mechanism are highlighted and discussed as follows:

- The supply voltage (V_s) of each gate driver circuitry is $+15V$, which is also the primary side supply voltage of the Semikron SKHI22AH4R driver. Therefore, at the input side of the circuitry, we have the following: supply voltage (V_s) gating signal 1, error signal, complementary gating signal 1, and the ground, as shown in Figure 6.4(b). The error signal is triggered whenever a short circuit is detected on the driver board, with a corresponding signal indicated on the LED highlighted in Figure 6.4(c).

- The gating signals for the driver board are generated from the FPGA module, as stated previously. The logic output voltage from the FPGA module is $+5V$ to turn on and $0V$ to turn off. However, the SKHI22AH4R driver input voltage requirement is $+15V$ to turn on the switching power semiconductor devices and $0V$ to turn off the switching power semiconductor devices. Therefore, the voltage level of the gating signals is shifted using the IR2113 IC, which is supplied by regulating the voltage supply with LM7805, as shown in Figure 6.4(c).

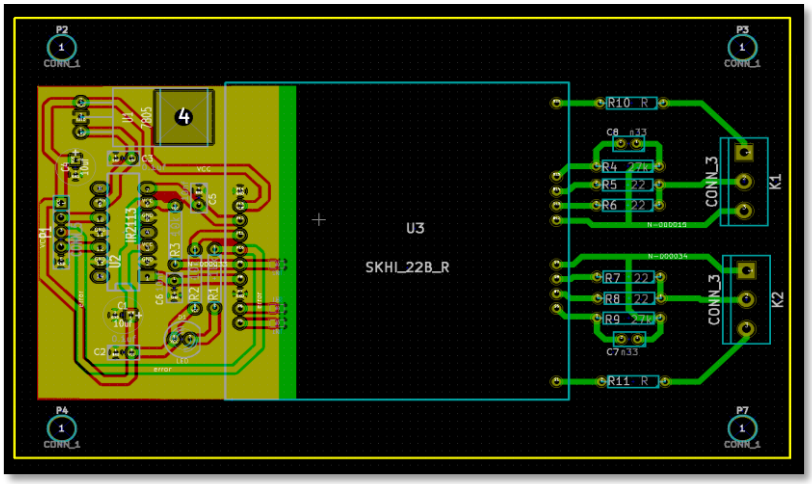
- The values of the gate turn-on and turn-off resistors (R_{ON} and R_{OFF}) are extracted from the datasheet as summarized in Table 6.1. Also, the values of the collector-emitter capacitor (C_{CE}) and collector-emitter resistor (R_{CE}) are highlighted in Table 6.1. These external components are highlighted in Figure 6.4(d).



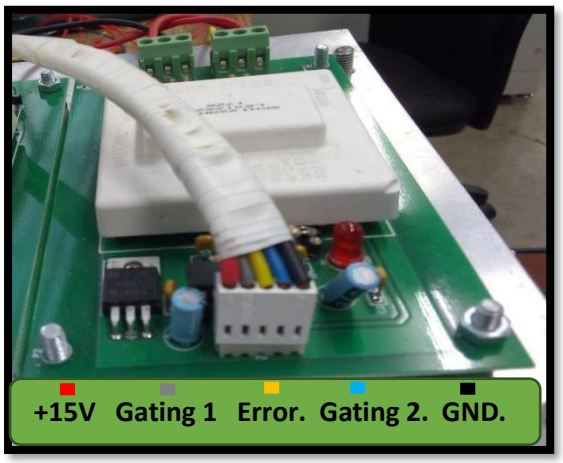
(a)

(b)

Figure 6.3. Gate driver circuitry connection in a 1ph 5L-NNPC converter topology. (a) schematic diagram. (b) actual physical connection.



(a)



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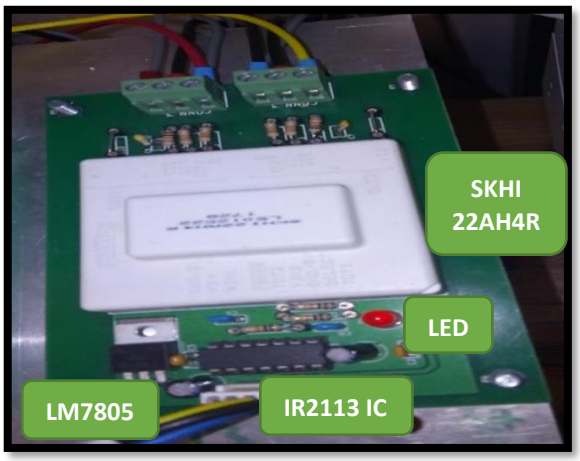

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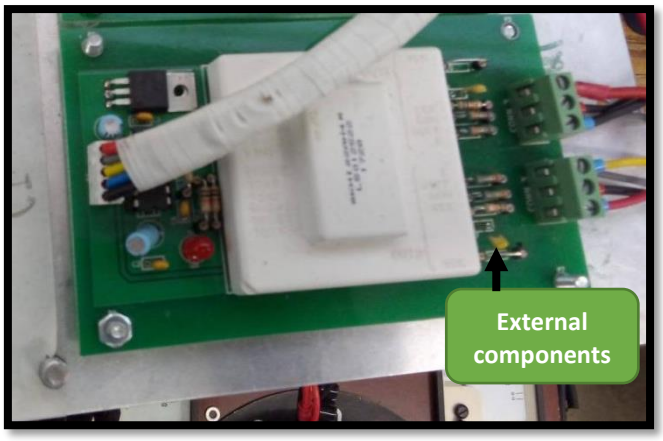


(d)

Figure 6.4. Gate driver circuitry. (a) PCB. (b) front view. (c) top view. (d) side view.

Table 6.1: External Components of Gate Driver Circuitry

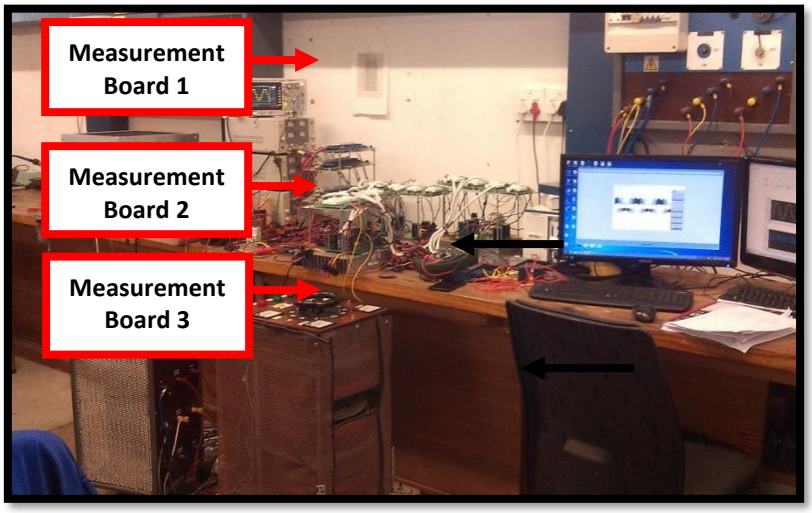
Parameter	Function	Value Derivation
R_{CE}	Collector-emitter threshold voltage	$V_{CEstat} = \frac{10R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1.4$
C_{CE}	Blanking time of V_{CE} monitoring	$t_m = \tau_{CE} \ln\left(\frac{15 - V_{CEstat}}{10 - V_{CEstat}}\right)$ $\tau_{CE} = C_{CE} \frac{10R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$
R_{ON}	Gate turn-on time	$R_{ON} > 3\Omega$
R_{OFF}	Gate turn-off time	$R_{OFF} > 3\Omega$

6.2.3. Measurement Board

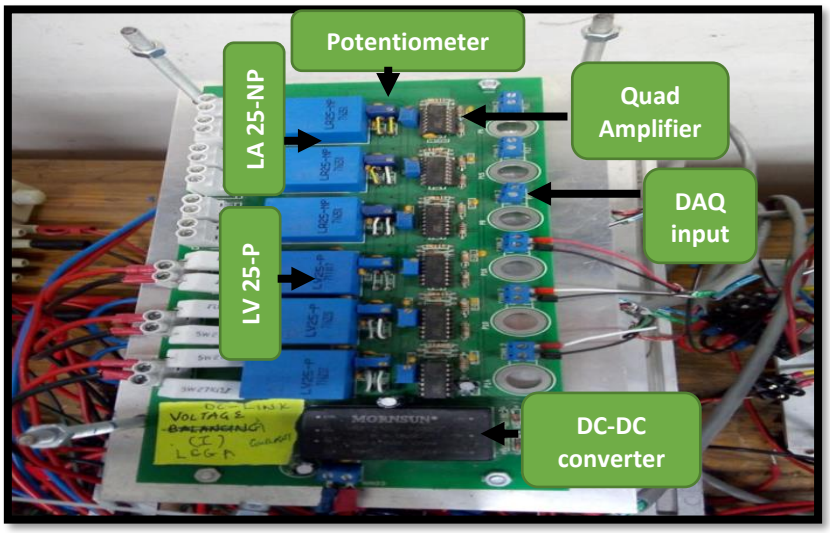
Voltage and current measurements are performed with LEM voltage and current transducers, as shown in Figures 6.5(a) and 6.5(b). A stack of three measurement boards is utilized in the experimental set-up as illustrated in Figure 6.5(a); measurement board 1 is used to measure the phase voltage and phase current of each phase of the converter, measurement board 2 is used to measure the clamping capacitor voltages and currents of a single-phase per time. Measurement board 3 is used to measure the three-phase grid voltages and currents. Each measurement board consists of three LEM voltage transducers (LV 25-P) and three LEM

current transducers (LA 25-NP) to measure various related system parameters, as shown in Figure 6.5(b). These transducers are mounted on a PCB shown in Figure 6.5(c). The schematic diagram of the measurement board circuitry is found in Appendix D.6.

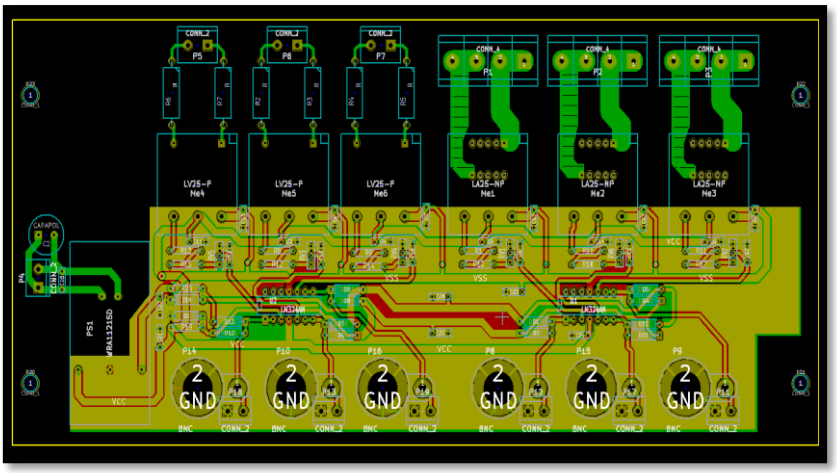
The potentiometers are inserted after the transducer modules to regulate the gain and offset of the measured parameter. The quad amplifier modifies the measured parameter for the input voltage range of the DAQ module connected from the measurement board's output through the NI SCB-68A. The dc-dc converter regulates the power supply from a voltage range of $9V \sim 18V$ to the required voltage level of $15V$.



(a)



(b)



(c)

Figure 6.5. Measurement board. (a) a stack of measurement boards, (b) a labelled measurement board, (c) PCB

A. LEM LV-25P

The voltage transducer can measure the nominal voltage range from $10V$ to $500V$, and the nominal primary current of the transducer is $10mA$, as stated in the datasheet found in Appendix E. An input resistor (R_1) is connected to the primary side of the LEM to limit the input current and ensure the measured voltage corresponds to the nominal primary current (stated previously). The internal circuitry of the LV-25P is shown in Figure 6.6(a). Therefore, the value of R_1 utilized in the measurement board is $27k\Omega / 5W$, for a maximum measured voltage of $350V$.

The conversion ratio of the LEM module between its secondary and primary side current is 2.5, as indicated on the datasheet in Appendix D.7. A resistor (R_M) is connected at the secondary side of the module to adjust the scaling factor and limit the output current. This resistor is a potentiometer, as stated previously and highlighted in Figure 6.5(b).

B. LEM LA-25NP

The current transducers have nominal current ratings of $25A$ and $25mA$ for their primary and secondary sides, respectively, as stated in the datasheet found in Appendix D.8. The internal circuitry of the LA-25NP is shown in Figure 6.6(b). The conversion ratio of the LEM module between its secondary and primary side current is $1:1000$, as indicated on the datasheet. A potentiometer is also connected at the secondary side of the module to adjust the scaling factor and limit the output current.

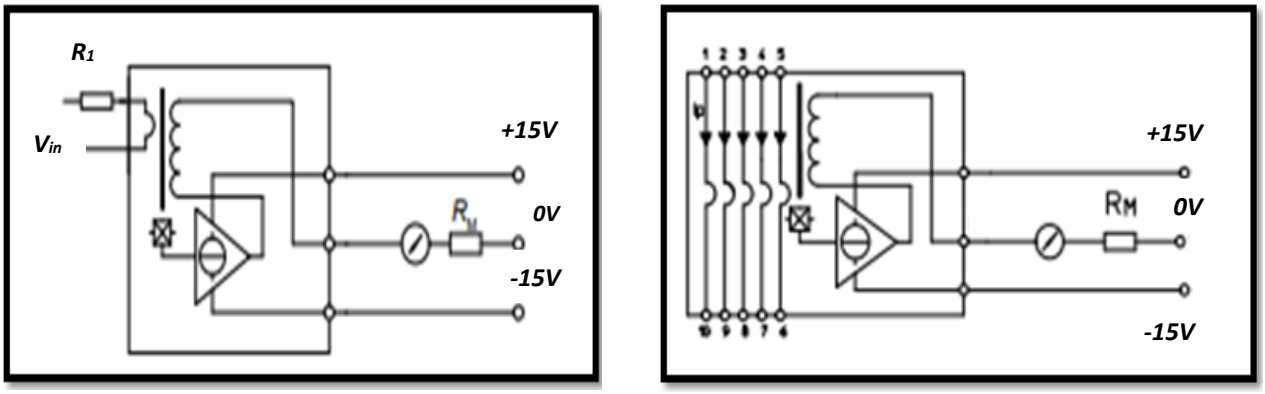


Figure 6.6. Internal circuitry of the LEM module. (a) LEM LV-25P, (b) LEM LA-25NP.

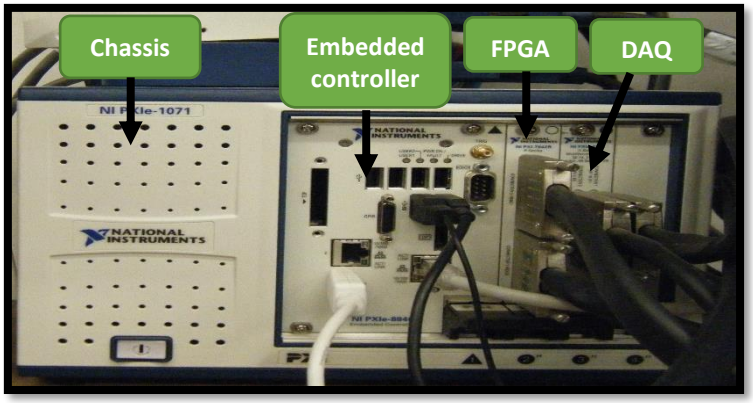


Figure 6.7. NI PXI System

6.2.4. NI PXI System

The PXI system is a flexible modular instrumentation platform that enables real-time control operations in the developed hardware-in-loop (HIL) configuration. A PXI system mainly provides power supply, cooling, and communication bus for the peripheral modules [195]-[198]. These modules are controlled through the embedded controller and configured with the LabVIEW and LabVIEW FPGA software tools. Therefore, the PXI system used in the presented experimental set-up consists of a PXIe-1071 chassis, PXIe-8840 embedded controller, PXI-7842R FPGA module, and PXIe-6363 DAQ module, as illustrated in Figure 6.7.

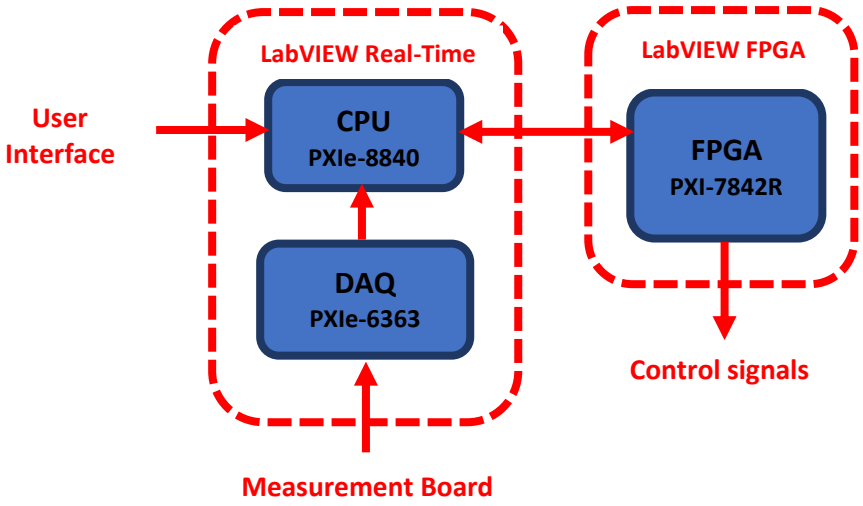


Figure 6.8. The communication link between PXI modules and LabVIEW software tools.

A. PXIe-1071 Chassis

The PXIe-1071 chassis is a four-slot chassis with 3gigabyte per second (Gb/s) system bandwidth; it allows the usage of an embedded controller that supports three peripheral PXI/PXIe modules, which are connected through a backplane connector [195]. The PXIe-8840 embedded controller is inserted in the first slot of the chassis; the first slot's backplane links the other peripheral modules to the PXIe bridge providing a 32-bit/33 MHz bus [195]. The PXI-7842R FPGA and PXIe-6363 DAQ modules are inserted in the chassis' second and third slots, respectively. These modules are connected to the other components of the experimental setup through the SCB-68A interface board.

B. PXIe-8840 Embedded Controller

The PXIe-8840 is a $2.75GHz$ dual-core processor that supports a $1600MHz$ small-outline dual inline memory module (SODIMM) [196]. It is used to synchronize communication with the other two peripheral modules and provide a reliable user interface, as illustrated in Figure 6.8.

C. PXI-7842R FPGA

The PXI-7842R module is a Virtex-5 LX50 field-programmable gate array (FPGA) with a maximum clock frequency rate of $40MHz$ and reconfigurable input/output nodes consisting of 8 analogue input (AI) channels, 8 analogue output (AO) channels, and 96 digital input/output (DIO) lines [197]. A significant benefit of implementing the overall controller on the PXI-

7842R FPGA module is the short execution time and parallel processing capability [171]. Due to its high clock frequency rate, control tasks can be carried out at a maximum speed of 25ns resolution. Thus, the PXI-7842R module is configured with the LabVIEW FPGA software tool for implementing control and switching operations. The control algorithm and switching operations configured on LabVIEW FPGA software are compiled via the Xilinx compilation tool. Furthermore, the LabVIEW FPGA program is interfaced with the LabVIEW real-time software to link the measurement operation and control algorithm with other external devices via the SCB-68A interface board. Furthermore, the DIO available on the module can be configured as inputs and outputs interfaced with other experimental set-up components via the SCB-68A interface board, as illustrated in Figure 6.9.

A significant drawback of the NI-PXI 7842R FPGA module is its limited available resources highlighted in Table 6.2 and previously illustrated in Chapter 4. Therefore, efficient use of the block RAM (BRAM) and digital signal processor (DSP48s) was carefully considered when configuring the NI-PXI 7842R FPGA module. The entire LabVIEW FPGA program and interface LabVIEW real-time program can be found in Appendix C.

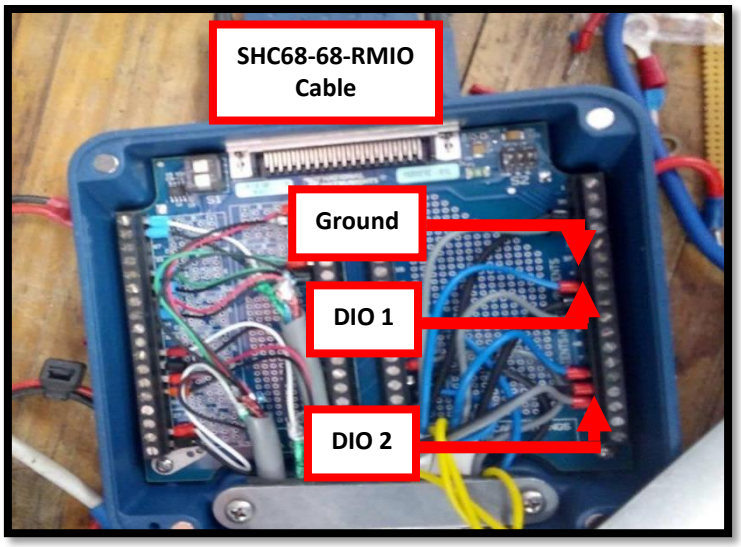


Figure 6.9. SCB-68A interface board connected to an external device.

Table 6.2: FPGA Resources for PXI-7842R Module

Device Utilization	Available Resources
Total Slices	7200
Slice Registers	28800
Slice LUTs	28800
Block RAMs	48
DSP48s	48

D. PXIe-6363 DAQ

The DAQ module is a multifunctional inputs/outputs (I/O) made up of analogue I/O, digital I/O, and four 32-bit counters [198]. It consists of 16 differential analogue input channels with a maximum sample rate of 1MS/s [198]. Furthermore, the module has 4 analogues and 48 digital output channels with maximum data rates of 2.88 Ms/s and 10 Ms/s. The system measurements carried out with the DAQ module is stated as follows:

- Three-phase grid voltage
- Three-phase grid current
- Clamping capacitor voltage
- Clamping capacitor current
- Converter output phase voltage
- Converter output phase current
- The dc-link voltage across the top capacitor and bottom capacitor

Measurement signals obtained from the measurement boards are interfaced to the DAQ through the SCB-68A interface board. Therefore, the pin-out connection of the PXIe-6363 and PXI-7842R is found in Appendices D.9 to D.12.

6.2.5. FPGA Implementation

The NI PXIe-1071 platform is a four-slot chassis with 3gigabyte per second (Gb/s) system bandwidth; it allows the usage of an embedded controller and supports three peripheral PXI/PXIe modules [200]. The NI PXIe-1071 platform utilized consists of NI PXIe-8840 embedded controller, NI PXI-7842R module, and NI PXIe-6363 module [200]-[203], as shown in Figure 6.10. The NI PXI-7842R module is a Virtex-5 LX50 field-programmable gate array

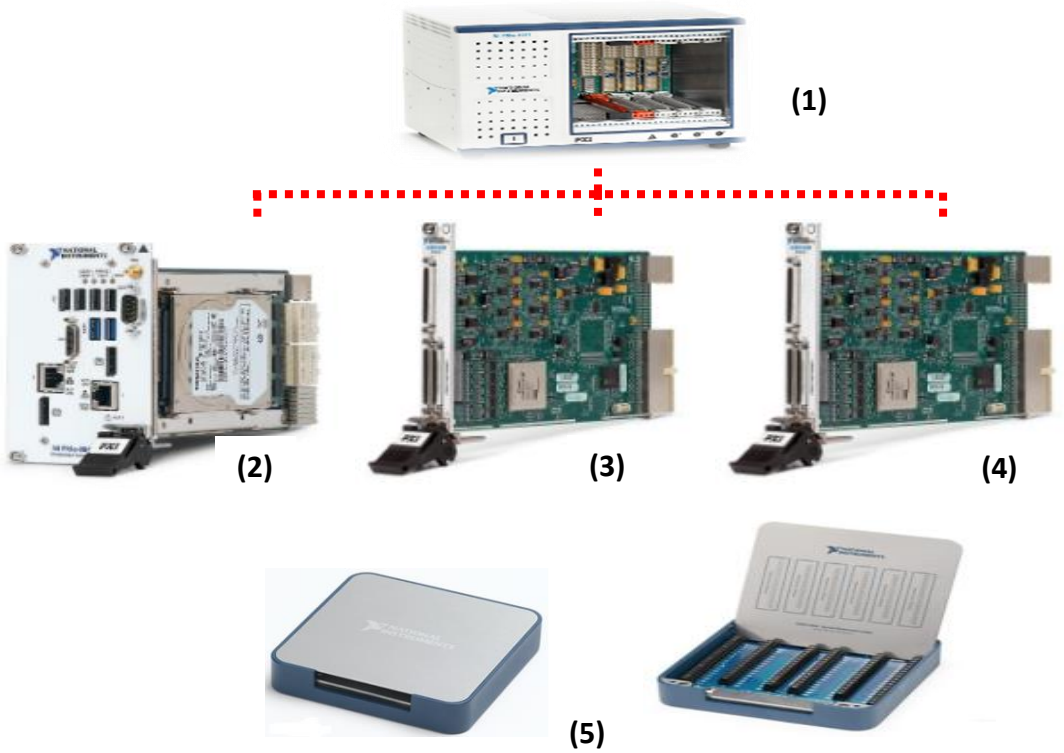


Figure 6.10: PXI system (1) PXIe-1071 chassis, (2) PXIe-8840 embedded controller, (3) PXI-7842R FPGA module, (4) PXIe-6363 DAQ module and (5) SCB-68A interface board.

(FPGA) with multifunctional reconfigurable input/output blocks [202]. The NI PXI-7842R module is configured with LabVIEW FPGA programming language to develop the modulation and voltage balancing control technique of the topology. Therefore, the FPGA implementation of the modulation and proposed voltage balancing control scheme is discussed in this section.

A. Direct Digital Synthesis-Based Modulation

The carrier, modulating, and shoot-through waveforms are created in the LabVIEW FPGA environment using a direct digital synthesis (DDS) method. The DDS is a look-up table (LUT)-based approach used to produce analogue signals using stored digital samples [204], [205]. The DDS method presented consists of an accumulator and a waveform LUT [205]. The accumulator is a 32-bit counter that stores the present phase value of the produced waveform specified by the accumulator increment [205]. Furthermore, the update rate of the accumulator and accumulator increment values determines the frequency of the waveform [204], [205]. A complete cycle of the carrier and modulating waveforms (i.e., 0 to 360 degrees) is represented within the accumulator phase value of 0 to 4.29×10^9 [205].

An 11-bit LUT with 2048 digital sample points representing the actual waveform produced is used to present the current waveform as updated from the accumulator phase value, as shown in Figures 6.11(a) and 6.11(b). Therefore, the number of times the accumulator counts for the frequency of the established waveform is obtained using (6.1):

$$N_a = Freq_W \times 2^b \tag{6.1}$$

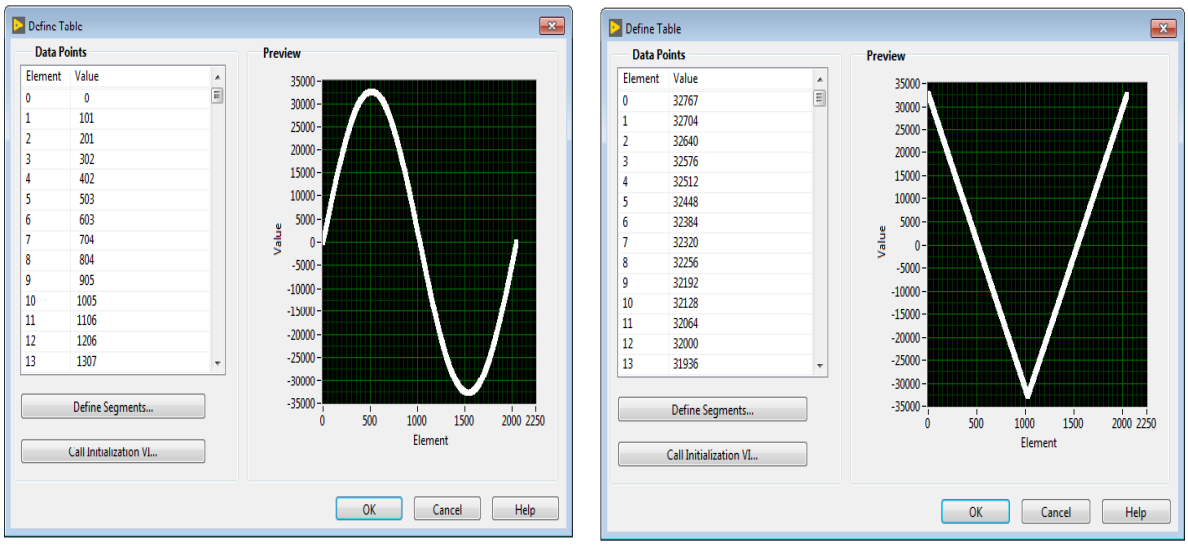
where N_a is the number of accumulators counts per seconds, $Freq_w$ is the frequency of the waveform and b is the number of bits of the accumulator, the accumulator increment ($A_{increment}$) is calculated using (6.2):

$$A_{increment} = \frac{N_a}{Loop\ Rate} \tag{6.2}$$

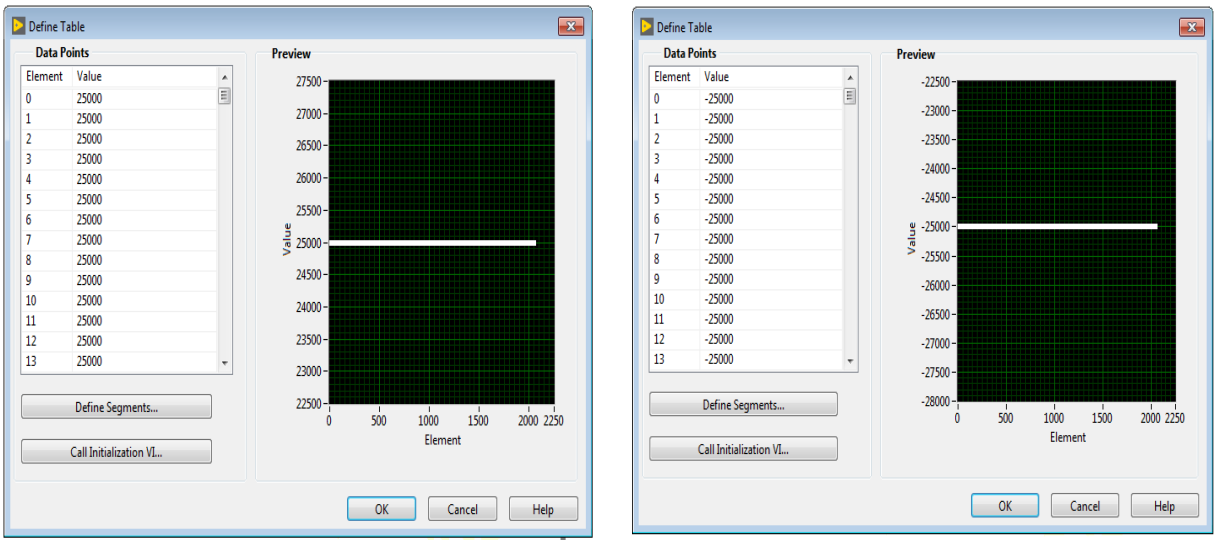
where the loop rate is given as 1MHz, as stated in [200]. The phase shift of the accumulator must be within the range of a full cycle waveform (0 to 4.29×10^9) [205]. Therefore, the conversion of the phase shift in degrees (D_{PS}) to their respective accumulator phase shift value (A_{PS}) is obtained by (6.3):

$$A_{PS} = \left(\frac{D_{PS}}{360}\right) \times 2^b \tag{6.3}$$

The values of A_{PS} for the proposed converter topology with four carrier waveforms phase-shifted by 90° is stated in Table 6.3. The datatype of the modulating and carrier waveforms are converted from a 16-bit integer (I16) number to a fixed-point (FXP) number for better FPGA resource utilization and Boolean operation. Also, the comparison between modulating, carrier, and shoot-through waveforms is carried out with a logic block of "greater than or equals to (≥)". Simultaneously, the pair of complementary switching power semiconductor devices are identified with a Boolean indicator. Each switching power semiconductor device is mapped to a specific pin of the NI PXI-7842R module connector through the FPGA I/O node.



(a) **(b)**



(c) **(d)**

Figure 6.11: Configured LUT. (a)sinusoidal waveform, (b) triangular waveform, (d) positive shoot-through constant, and (d) negative shoot-through constant.

Table 6.3: Calculated values of A_{PS}

Carrier	D_{PS}	A_{PS}
a	0	0
b	90°	1.072×10^{9}
c	180°	2.145×10^{9}
d	270°	3.22×10^{9}

Table 6.4 shows the FPGA resources utilized to develop the modulation in a 3ph 5L-tapped inductor qZS-NNPC converter topology. After completing the LabVIEW FPGA compilation, the program was interface through a read/write control function to the LabVIEW environment. By enabling the real-time connection of the LabVIEW FPGA to the converter topology hardware. The modulation for a 1ph 5L-tapped inductor qZS-NNPC converter topology within the real-time LabVIEW environment is shown in Figure 6.12. The switching waveform for the switching power semiconductor devices acquired in real-time in the LabVIEW environment is shown in Figures 6.13(a) to 6.13(d), respectively.

Table 6.4: FPGA resources for the 3ph modulation technique

Device Utilization	Utilized Resources	Available Resources	Percentage of Utilized Resources
Total Slices	3765	7200	52.3 %
Slice Registers	7931	28800	27.5 %
Slice LUTs	7050	28800	24.5 %
Block RAMs	7	48	14.6 %
DSP48s	14	48	29.2 %

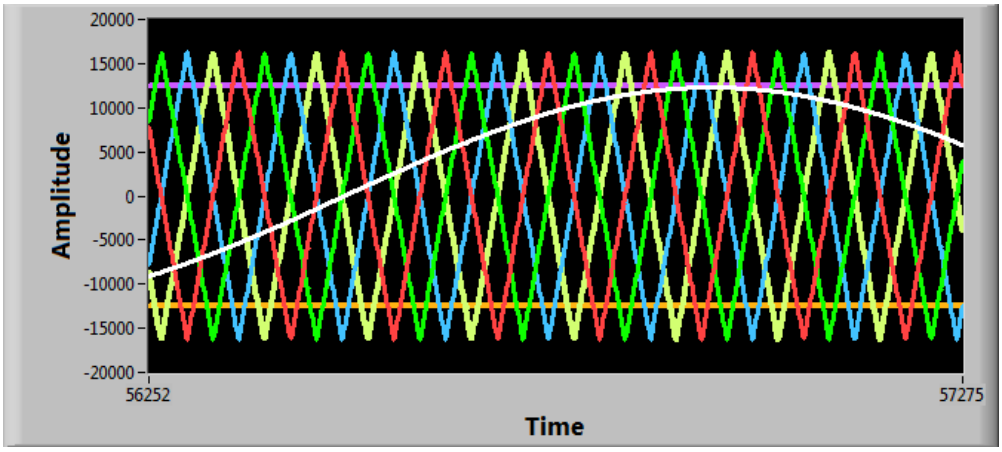
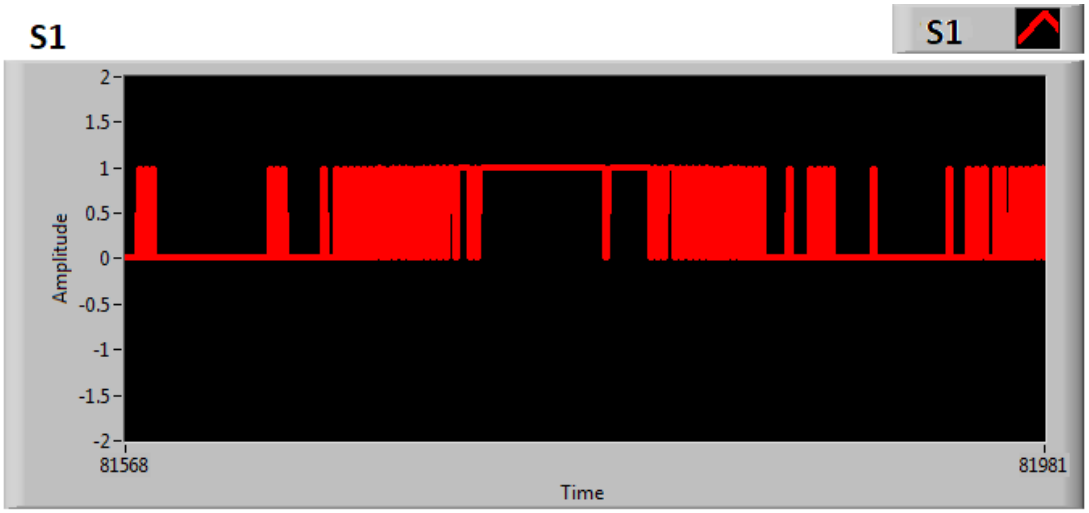
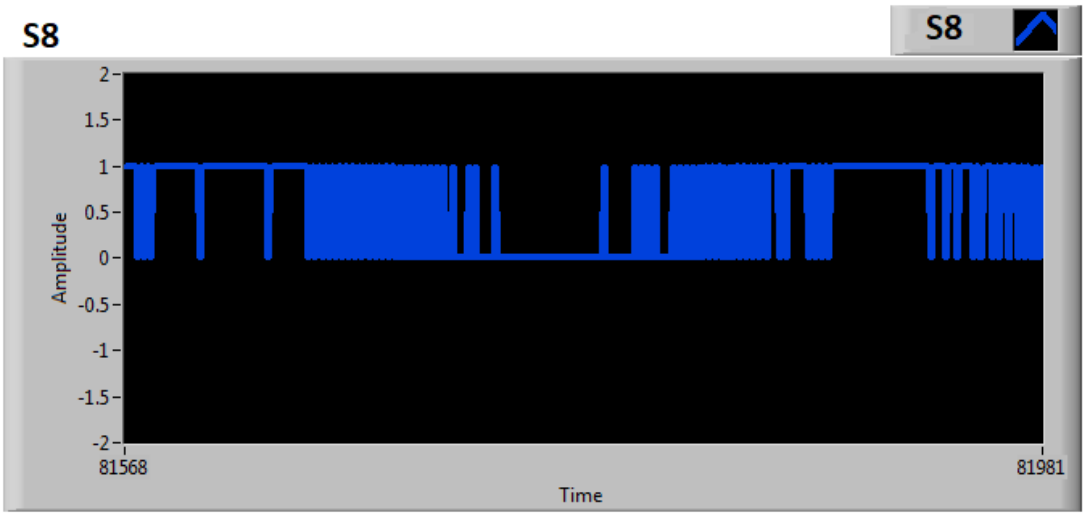
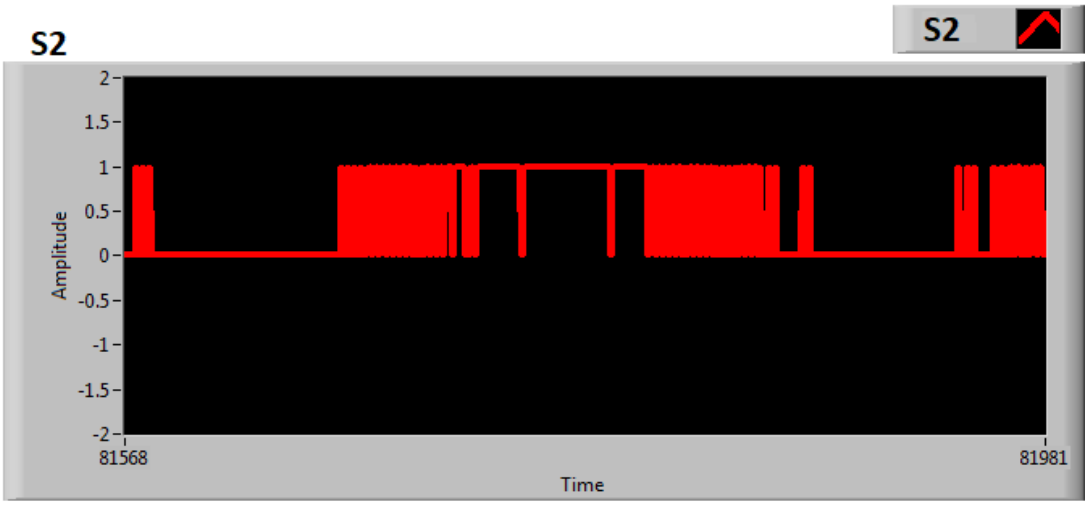


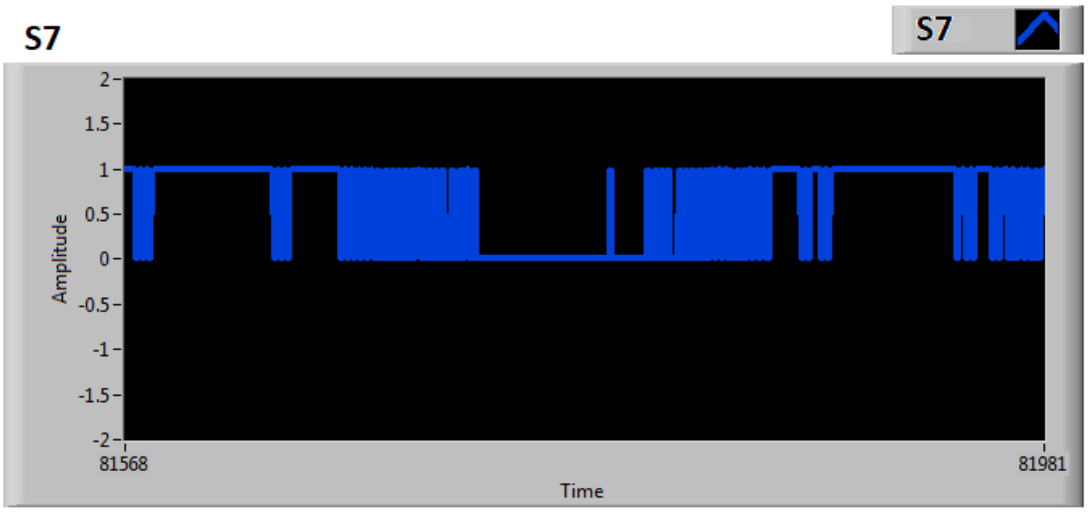
Figure 6.12: Generated modulation signal in real-time LabVIEW environment.


S1
S1
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time

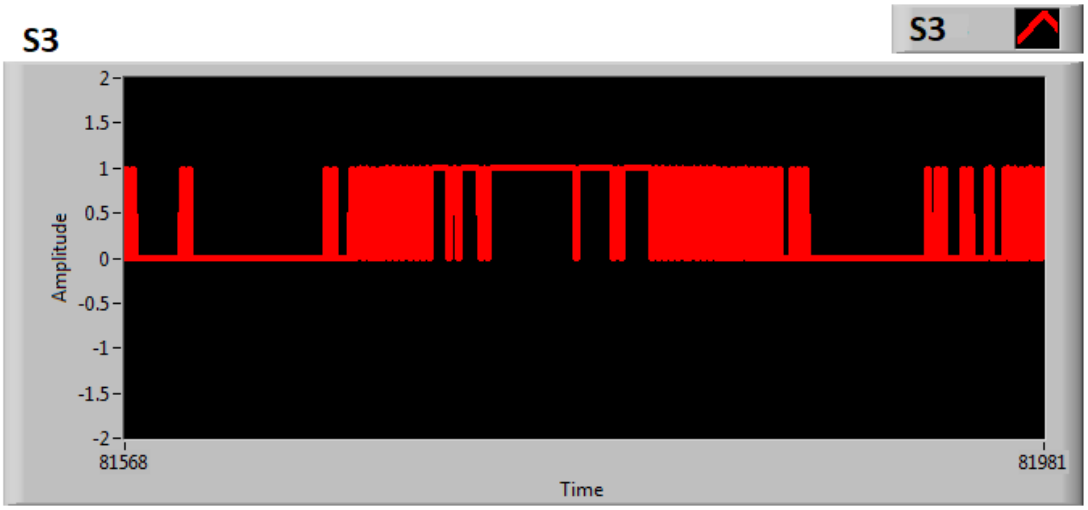

S8
S8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time

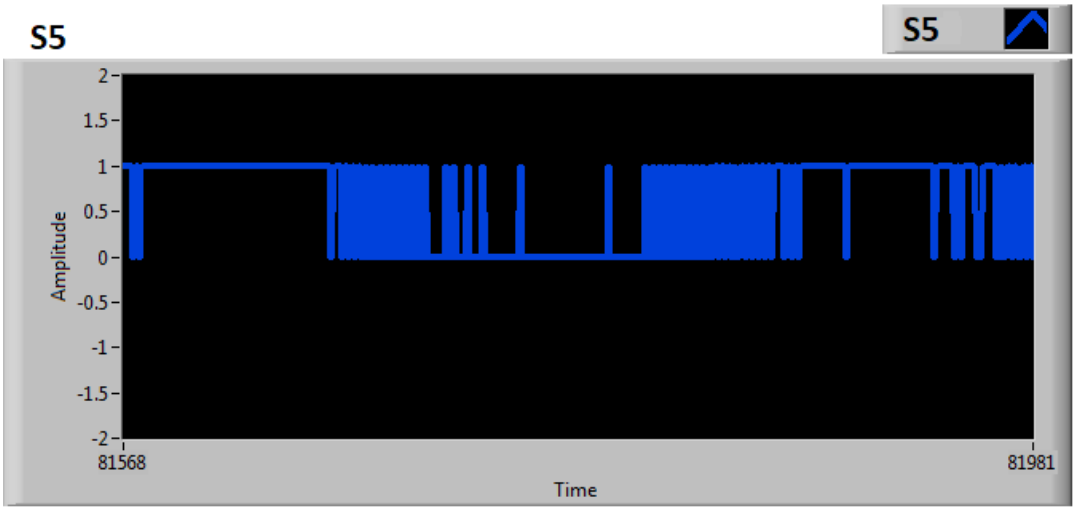
(a)


S2
S2
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time

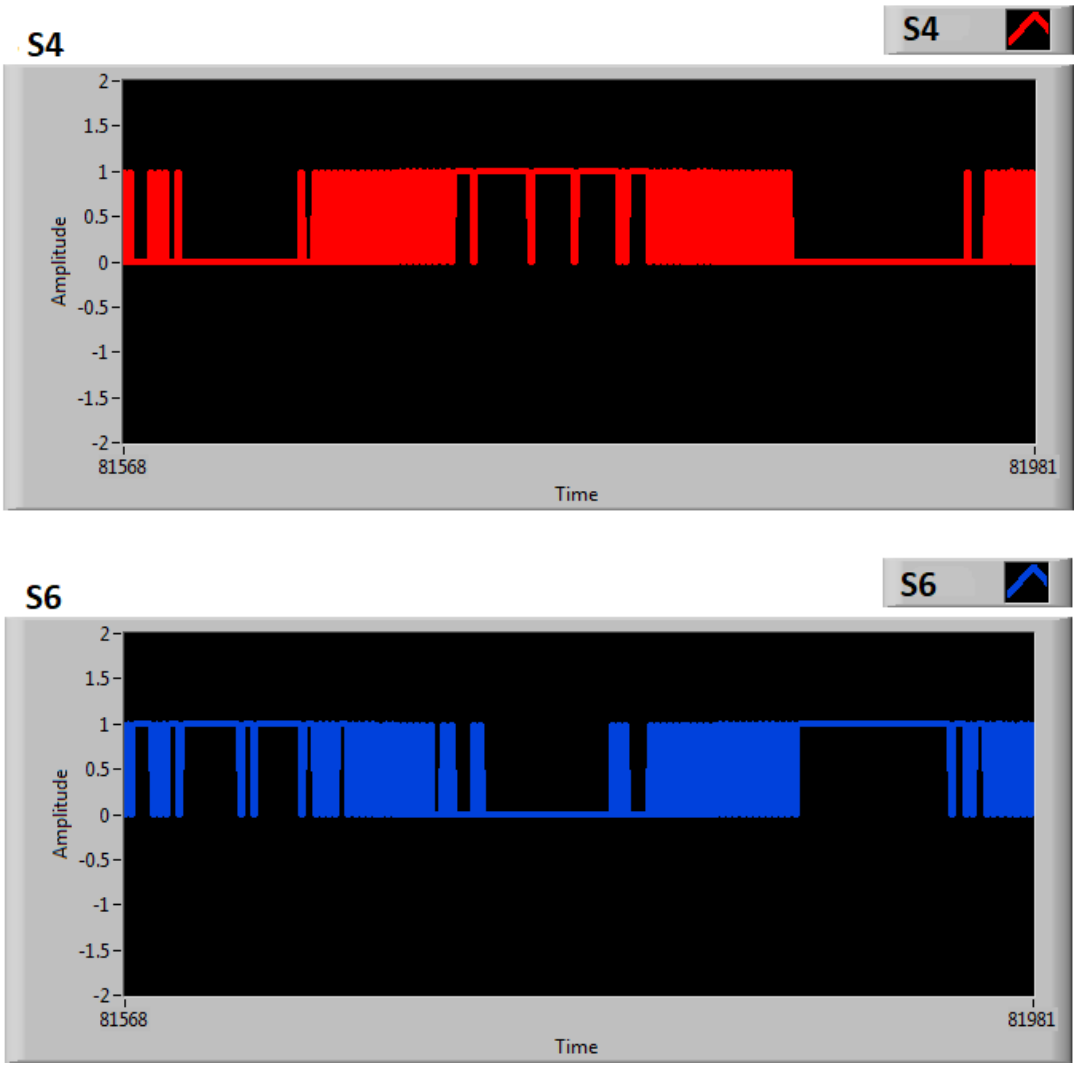

S7
S7
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time

(b)


S3
S3
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time


S5
S5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Amplitude
81568
81981
Time

(c)



(d)

Figure 6.13: Switching waveform obtained in real-time LabVIEW environment. (a) S_1 & S_8, (b) S_2 & S_7, (c) S_3 & S_5, (d) S_4 & S_6.

B. Voltage Balancing Control Technique

The block diagram of the voltage balancing control technique discussed in section 4.3.2 is illustrated in Figure 6.14. Each of the quasi-PR controller highlighted has been developed as a smaller subroutine (known as subVI in a LabVIEW environment) within the voltage balancing control algorithm. Each subroutine (subVI) is implemented using a While Loop structure executed in 3 ticks (i.e., 750μs) in each iteration. While the FPGA top-level clock is 40MHz, and one tick is represented by $1/40MHz$ which is equivalent to $25ns$. The main functionality of the presented subVI is the execution of the controller algorithm based on the transfer

function shown in (4.73), as illustrated in Figure 6.14. Therefore, the control operation is implemented in the following sequence:

- The computation of the error signal is obtained from the difference between the measured voltage value and the nominal voltage value (reference value). The measured voltage value of the clamping capacitor voltage is obtained through the measurement board. The nominal voltage value is obtained as a fraction of the dc-link voltage.
- The output of the error signal operation is multiplied to both K_p and K_r to carry out further control computation. The values of K_p and K_r are obtained from (4.82) and (4.83).
- The output of the multiplied K_p and error signals are fed to an integral operation with the upper limit and lower limit set manually. Furthermore, the output of the multiplied K_r and error signals are fed into a feedforward node that defines the output to the fundamental frequency. An anti-windup operation is included in the control algorithm through the feedback node. The reset button is added to reset the computation in case of an overflow operation manually.
- The output of the control algorithm is achieved by the computation of the proportional gain, resonant gain and variation of the fundamental frequency is summed up through a coupled of select operators operated manually through the reset button.
- The output of the quasi-PR controller is fed into the duty cycle modifier algorithm shown in Figure 6.15. Furthermore, the FPGA resources utilized for the voltage balancing control technique is highlighted in Table 6.5.

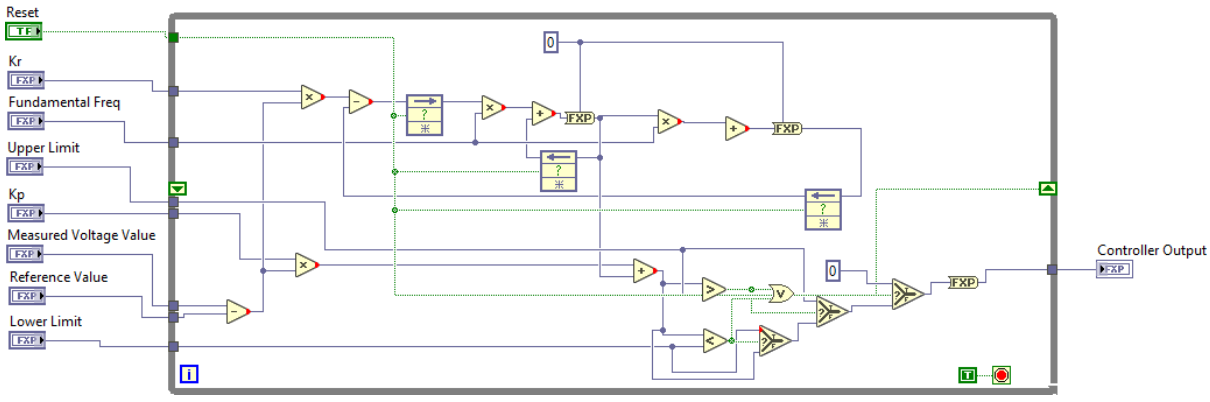


Figure 6.14: Quasi-PR control algorithm in LabVIEW FPGA environment

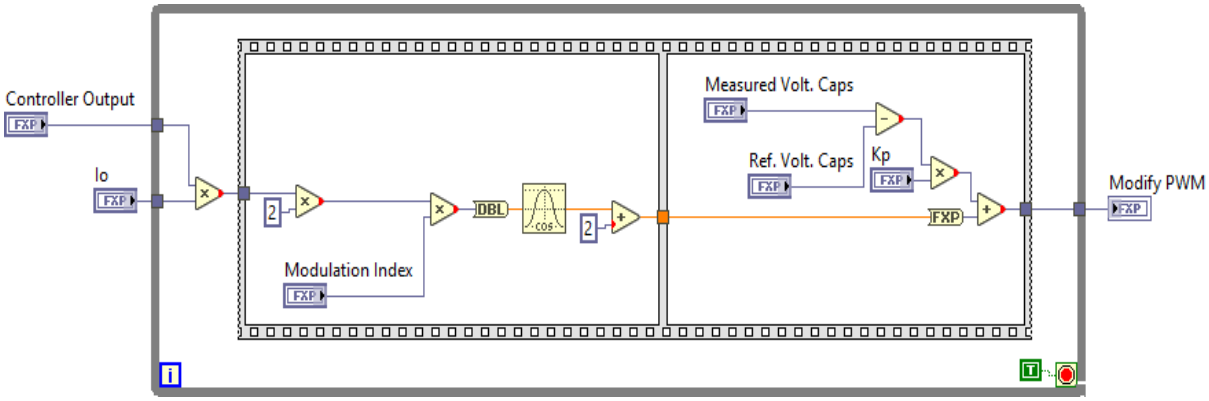


Figure 6.15: Duty cycle modifier algorithm in LabVIEW FPGA environment

Table 6.5: FPGA resources for the voltage balancing control technique.

Device Utilization	Utilized Resources	Available Resources	Percentage of Utilized Resources
Total Slices	1142	7200	15.86 %
Slice Registers	2514	28800	8.73 %
Slice LUTs	2165	28800	7.52 %
Block RAMs	0	48	0 %
DSP48s	11	48	29.2 %

6.2.6. LCL Filter

The single-phase equivalent circuit of the *LCL* filter topology deployed at the converter output, as shown in Figure 6.16. From the figure, v_o is the output voltage of the grid-side converter, v_g is the grid voltage, L_c is the converter-side inductor, L_g is the grid-side inductor, L_{grid} is the grid inductance, R_d is the damping resistor, i_{ph} is the current flowing at the converter output through the converter-side filter inductor, i_{cf} is the current flowing through the filter capacitor, and i_g is the current flowing through the grid-side inductor, as illustrated.

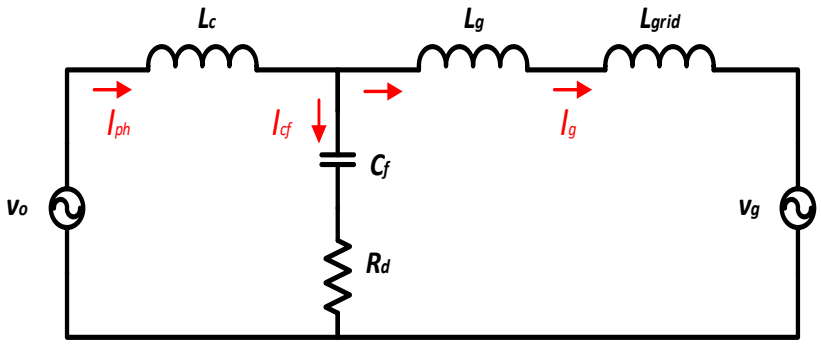


Figure 6.16: Equivalent circuit of a single-phase *LCL* filter.

A significant drawback of the *LCL* filter topology is the presence of a resonance frequency (f_{res}) because of the frequency components of the filter inductance and capacitance [136]-[139], [165]. Due to the limited switching frequency of the power converter configuration, the established criterion ($10f_g < f_{res} < 0.5f_s$) for selecting the resonance frequency is not applicable because f_{res} is bound to interact with sideband harmonics of the PS-PWM resulting in the instability of the current control loop [137], [138]. The resonance frequency of the grid-connected converter based on the generalized design algorithm must satisfy the following criterion stated below [165]:

$$f_b < f_{res} < 0.5f_s \tag{6.4}$$

where f_b is the bandwidth frequency of the controller, which is given by $f_b \approx f_s/6\pi$ [165], and f_s is the sampling frequency which is given by $f_s = f_{sw}$. Therefore, f_{res} is given as expressed in (6.5).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_c+L_g}{L_cL_gC_f}} \tag{6.5}$$

A. Filter Inductance Design

The value of the filter inductance is based on the following factors [136]-[139], [165]:

1) Maximum dc-link voltage is expressed in (3.11).
2) Reactive power compensation limit [136]-[138].
3) Attenuation limits stated in IEEE-519 standard [138], [165].
4) The ratio between the grid-side (L_g) and converter-side (L_c) inductance [165].

Therefore, (6.5) is further modified into (6.6) as follows.

$$L_{tot} = \frac{\alpha^2(1+\gamma)^2}{4\pi^2 f_{sw}^2 \gamma C_f} \tag{6.6}$$

where $L_{tot} = L_c + L_g$ is the total inductance of the filter, ratio $\alpha = f_{sw}/f_{res}$, and ratio $\gamma = L_g/L_c$. The value range of both α and γ has been established in [165], with $\gamma = 1$.

B. Filter Capacitance Design

The filter capacitance value is selected to sustain the power factor and minimize the reactive power production of the converter [137], [165]. Therefore, the base impedance (Z_b) and base capacitance (C_b) of the *LCL* filter is expressed in (6.7) and (6.8).

$$Z_b = \frac{V_{LL}^2}{P_R} \tag{6.7}$$

$$C_b = \frac{1}{(2\pi f_g)\cdot Z_b} \tag{6.8}$$

A factor of 5% limits filter capacitance to ensure the power factor is not further reduced [137], [165]. This is expressed in (6.9).

$$C_f = 0.05 C_b \tag{6.9}$$

C. Damping Resistance

The resonance frequency of the *LCL* filter can be mitigated by either the active damping technique or the passive damping technique [136]-[139], [165]. Due to the limited control bandwidth of the converter topology, a passive damping technique is deployed in the *LCL* filter topology [136]-[139], [165]. Therefore, the transfer function that relates the grid current (i_g) with the converter output voltage (v_o) stated in (3.53), is modified to include the damping resistor (R_d) as expressed in (6.10).

$$\frac{i_g(s)}{v_o(s)} = \frac{R_d C_f s + 1}{s^3 L_c L_g C_f + s^2 (L_c + L_g) R_d C_f + s(L_c + L_g)} \tag{6.10}$$

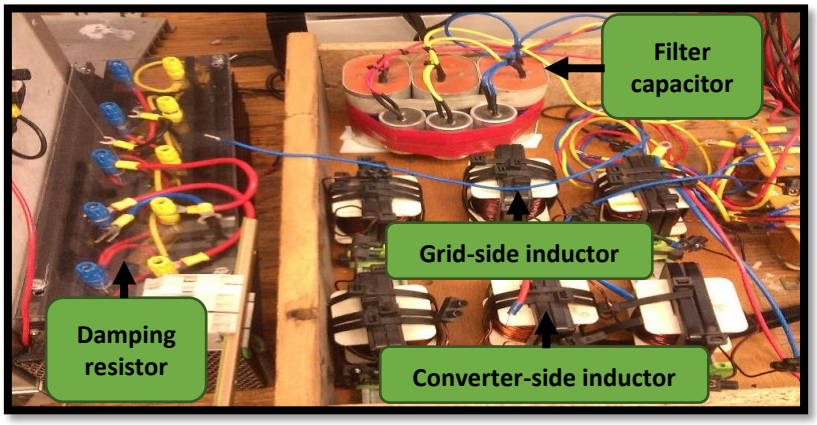
The value of the passive damping resistor (R_d) is obtained from (6.11) [165].

$$R_d = \frac{1}{18.85 f_{res} C_f} \tag{6.11}$$

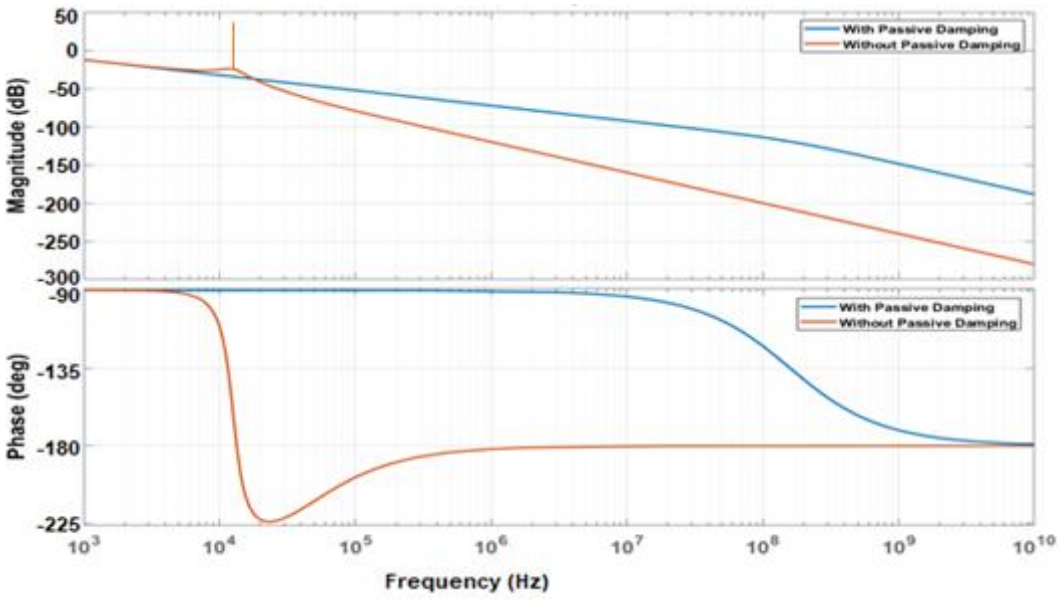
Furthermore, the values of the components of the *LCL* filter are stated in Table 6.6. The three-phase *LCL* filter topology utilized in the experimental set-up and associated bode diagram are shown in Figures 6.17(a) and 6.17(b).

Table 6.6: Values of LCL Filter

Parameters	Value
Grid-side inductor (L_g)	$2.1mH$
Converter-side inductor (L_c)	$2.1mH$
Filter capacitor (C_f)	$6\mu F$
Damping resistor (R_d)	4.41Ω



(a)



(b)

Figure 6.17: Filter hardware and bode diagram. (a) three-phase *LCL* filter. (b) bode plot with and without passive damping.

6.3. Grid Connection

The prototype and experimental rig presented in the previous sections is utilized to test the topology based on the hardware-in-loop configuration in grid-connected mode. Figure 6.18 highlights the measurement and sensing of the three-phase grid voltage in the experimental rig. The grid voltage and rectifier input voltage are obtained from the $380V$ three-phase supply connected to the grid and rectifier input variacs, respectively.

6.3.1. Grid Synchronization

The three-phase grid voltages are assumed to be balanced in the presented scenario. Therefore, the synchronous reference frame phase-locked loop (SRF-PLL) technique is used for grid synchronization [219], [220], as shown in Figure 6.19. While the grid frequency is relatively stable at $50Hz$, the sampled grid voltages obtained within the LabVIEW real-time (RT) environment consist of notches shown in Figure 6.20(a). Therefore, the proper tuning of the proportional gain (k_p) and integral gain (k_i) of the PI controller in the SRF-PLL will reduce the harmonics caused by notches [219]. The normalizing factor (α_f) is utilized to set the amplitude of k_p and k_i about the crossover frequency (ω_c) and all its related equations are found in [219]. By properly selecting α_f, the bandwidth and damping of the controller can be improved [219], [220]. The value of α_f is recommended to be 5 as presented in the LabVIEW FPGA environment [197], as stated in Table 6.7. Due to the notches in the grid voltages and the slight offset in phase B (as shown in Figure 6.20(a)), the PLL output (phase angle) is distorted, as shown in Figure 6.20(b). By selecting α_f to be 2.4 as suggested in [219], the PLL output distortion is eliminated, as shown in Figure 6.20(c).

Table 6.7: Parameters of the SRF-PLL

α_f	ω_c	k_p	k_i
5	$1000Hz$	12	200
2.4	$2083Hz$	22.4	868

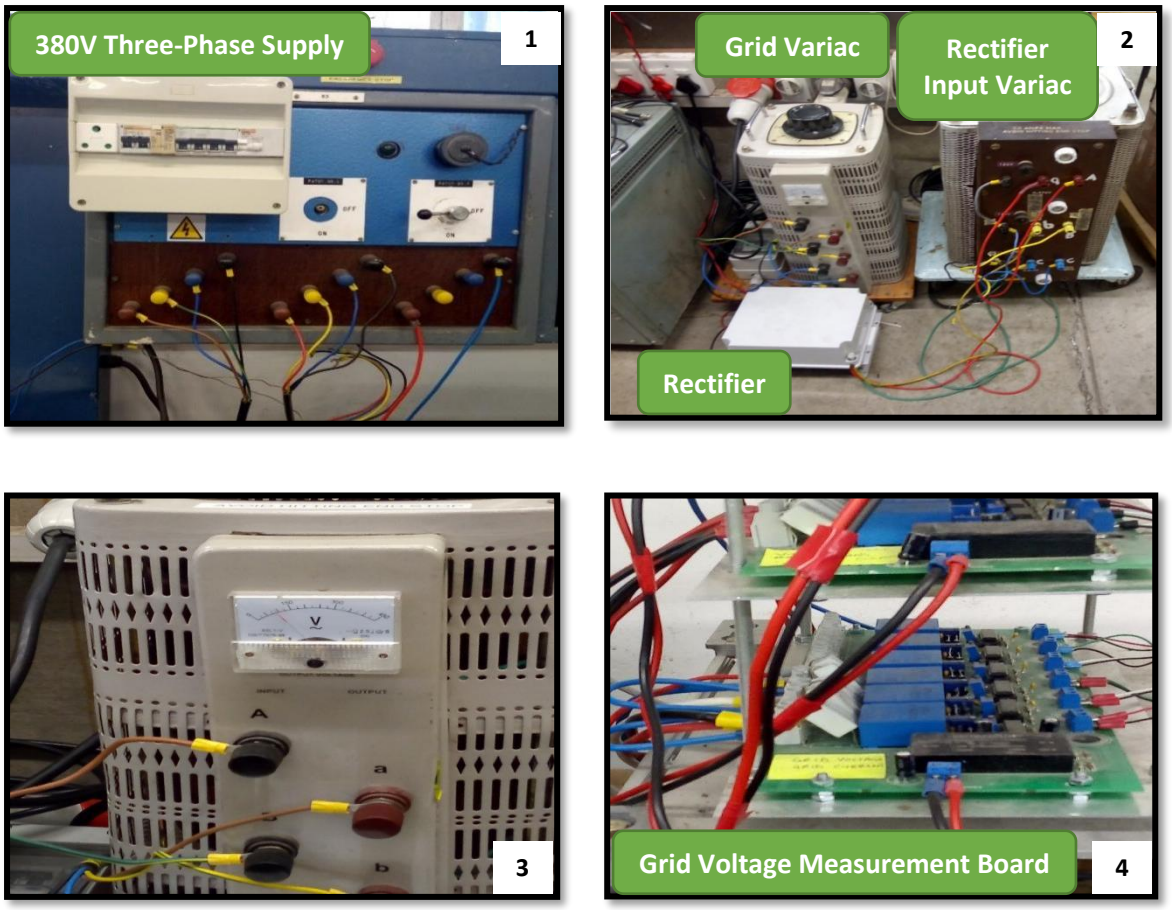


Figure 6.18: Measurement and sensing of the grid voltage: (1) 380*V* three-phase supply, (2) grid variac; rectifier input variac; and rectifier, (3) grid variac at about 100*V*, and (4) grid voltage measurement board.

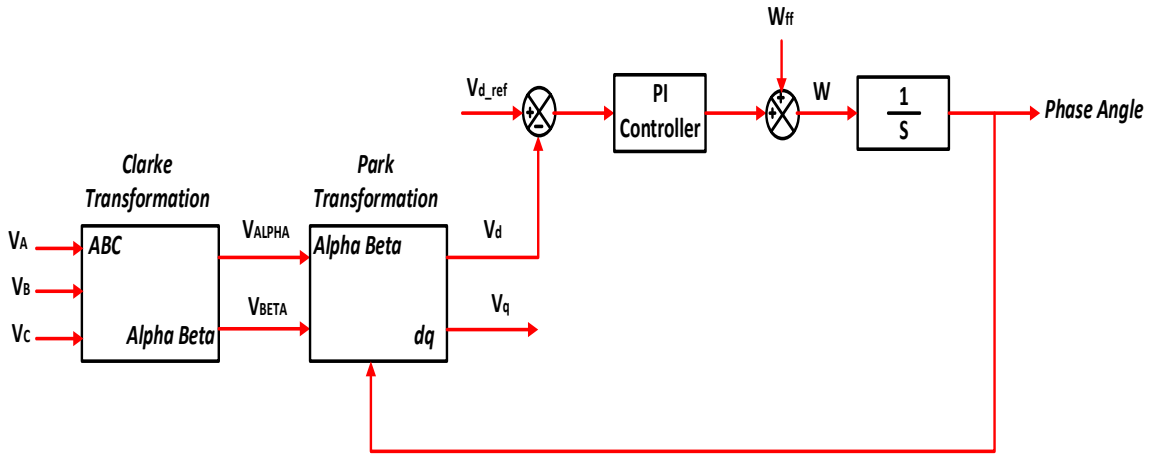
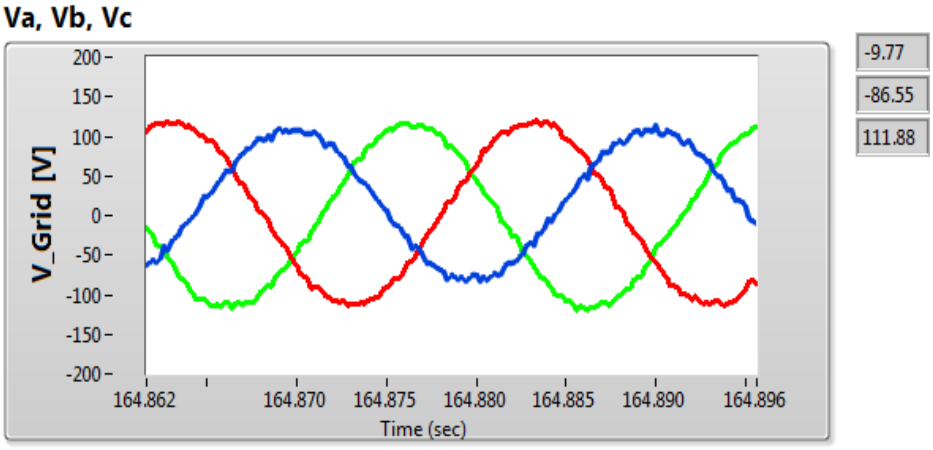
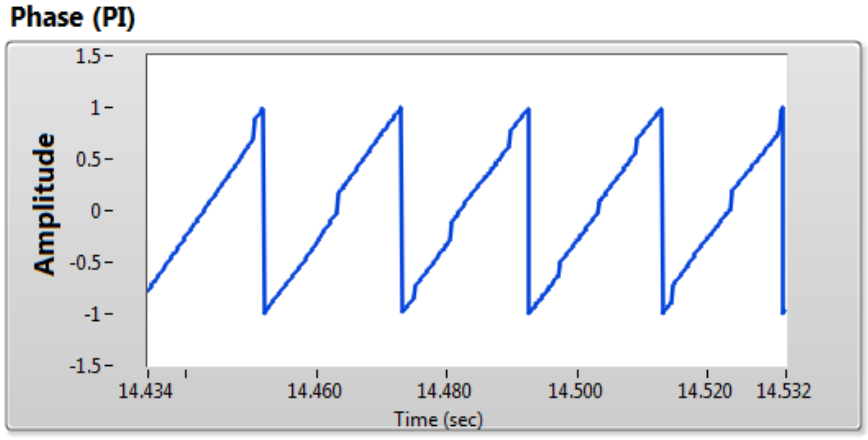


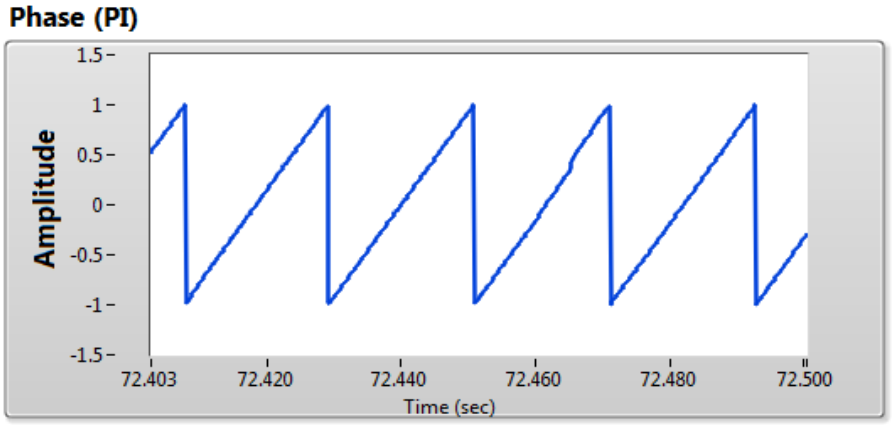
Figure 6.19. Three-phase SRF-PLL



(a)



(b)



(c)

Figure 6.20: Grid synchronization in LabVIEW RT. (a) distorted three-phase grid voltages, (b) distorted PLL output at $\alpha_f = 5$, (c) PLL output at $\alpha_f = 2.4$.

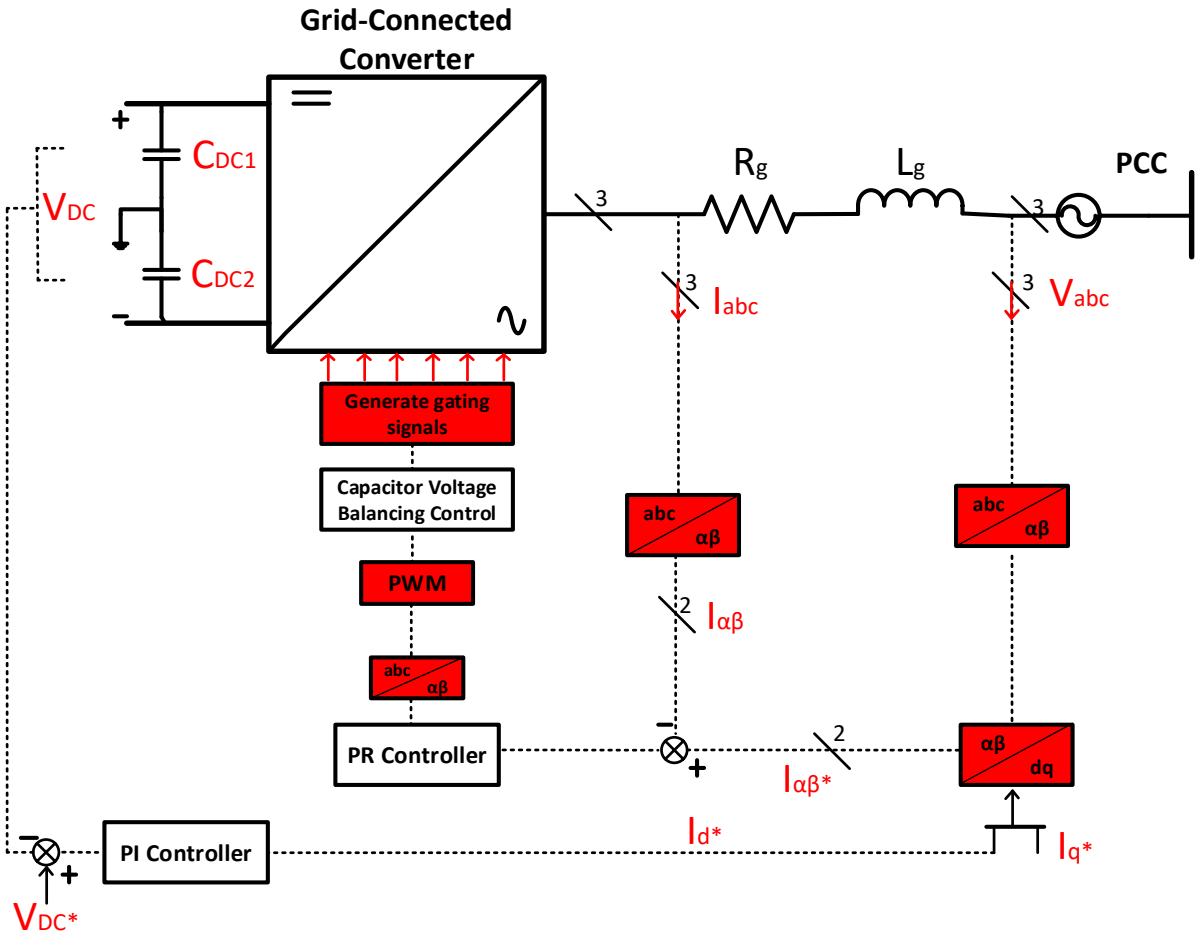


Figure 6.21: Overview of the control structure of the grid-connected converter.

6.3.2. Design of the Closed-loop Controller

In Figure 6.21, the grid-side converter control based on a cascaded control structure with the dc-link voltage control and current control loops highlighted. The outer dc-link voltage loop regulates the dc-link voltage to a reference voltage (V_{DC}^{*}). The inner current loop controls the active and reactive currents in a stationary reference frame that aligns to the grid voltage. Therefore, the design and analysis of the cascaded control loop are presented in this section.

The dc-link voltage control loop based on the proportional-integral (PI) controller, generates the references of the inner control loop (which is based on proportional-resonant (PR) controller) [221]. The PR controller is a good choice because the computational burden of the cascaded control structure is reduced by eliminating coordinate transformations in the discrete-time implementation [222]. Furthermore, the PR controller allows tracking of reference current without steady-state error [223].

The control algorithm is executed during the switching period and the sampling is carried out at the same rate (i.e., $T_{sw} = T_s$). The PI controller is tuned based on the symmetrical optimum method presented in [221], and the PR controller is tuned based on the guidelines presented in [223]. The transfer functions of the PI controller $\left(G_{PI(s)} = G_{V(s)}\right)$ and PR controller ($G_{PR(s)} = G_{C(s)}$) are given by (6.12) and (6.13) as follows:

$$G_{PI(s)} = G_{V(s)} = k_{p,v} + \frac{k_{i,v}}{s} \tag{6.12}$$

$$G_{PR(s)} = G_{C(s)} = k_{p,c} + \frac{2k_{r,c}s}{s^2+\omega_0^2} \tag{6.13}$$

where, $k_{p,v}$ and $k_{p,c}$ represents the proportional gain of the PI and PR controller respectively; $k_{i,v}$ represents the integral gain of the PI controller, and $k_{r,c}$ represents the resonant gain of the PR controller. Therefore, the values of these parameters are stated in Table 6.8.

The block diagram of the current control loop of the converter is depicted in Figure 6.22, where $G_{C(s)}$, $G_{PWM(s)}$, and $G_{LCL(s)}$ are the discrete transfer functions of the current controller (stated in 6.10), PWM unit, and LCL filter (stated in 6.7). $G_{PWM(s)}$ is described based on the computational delay, continuous sampling, and zero-order hold (ZOH) as highlighted in [193]. Therefore, the transfer function of the PWM unit is expressed in (6.14).

$$G_{PWM(s)} = \frac{e^{-T_s \cdot s}\left(1-e^{-T_s \cdot s}\right)}{T_s \cdot s} \tag{6.14}$$

where T_s is the sampling period of the controller. The Pade approximation was utilized to simplify $G_{PWM(s)}$ as stated in (6.15) to (6.16).

$$e^{-T_s \cdot s} \approx \frac{1-0.5 \cdot T_s \cdot s}{1+0.5 \cdot T_s \cdot s} \tag{6.15}$$

Therefore, substituting (6.15) into (6.14) results in (6.16).

$$G_{PWM(s)} = \frac{e^{-T_s \cdot s}\left(1-e^{-T_s \cdot s}\right)}{T_s \cdot s} \approx \frac{1-0.5 \cdot T_s \cdot s}{(1+0.5 \cdot T_s \cdot s)^2} \tag{6.16}$$

According to Figure 6.22, the open-loop ($G_{ol(s)}$) and closed-loop ($G_{cl(s)}$) transfer functions of the current control loop are obtained in (6.17) and (6.18).

$$G_{ol(s)} = G_{C(s)} \cdot G_{PWM(s)} \cdot G_{LCL(s)} \tag{6.17}$$

$$G_{cl(s)} = \frac{G_{C(s)} \cdot G_{PWM(s)} \cdot G_{LCL(s)}}{1+G_{C(s)} \cdot G_{PWM(s)} \cdot G_{LCL(s)}} \tag{6.18}$$

Therefore, the measured waveforms obtained in the LabVIEW RT environment are illustrated in Figures 6.23.

Table 6.8: Values of the PI and PR controller gains

$k_{p,v}$	$k_{i,v}$	$k_{p,c}$	$k_{r,c}$
44	138.8	10.97	261.3

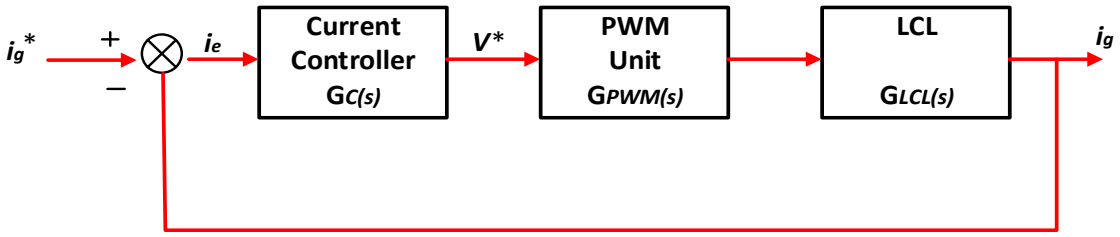


Figure 6.22. Block diagram of the current control loop in the proposed converter topology.

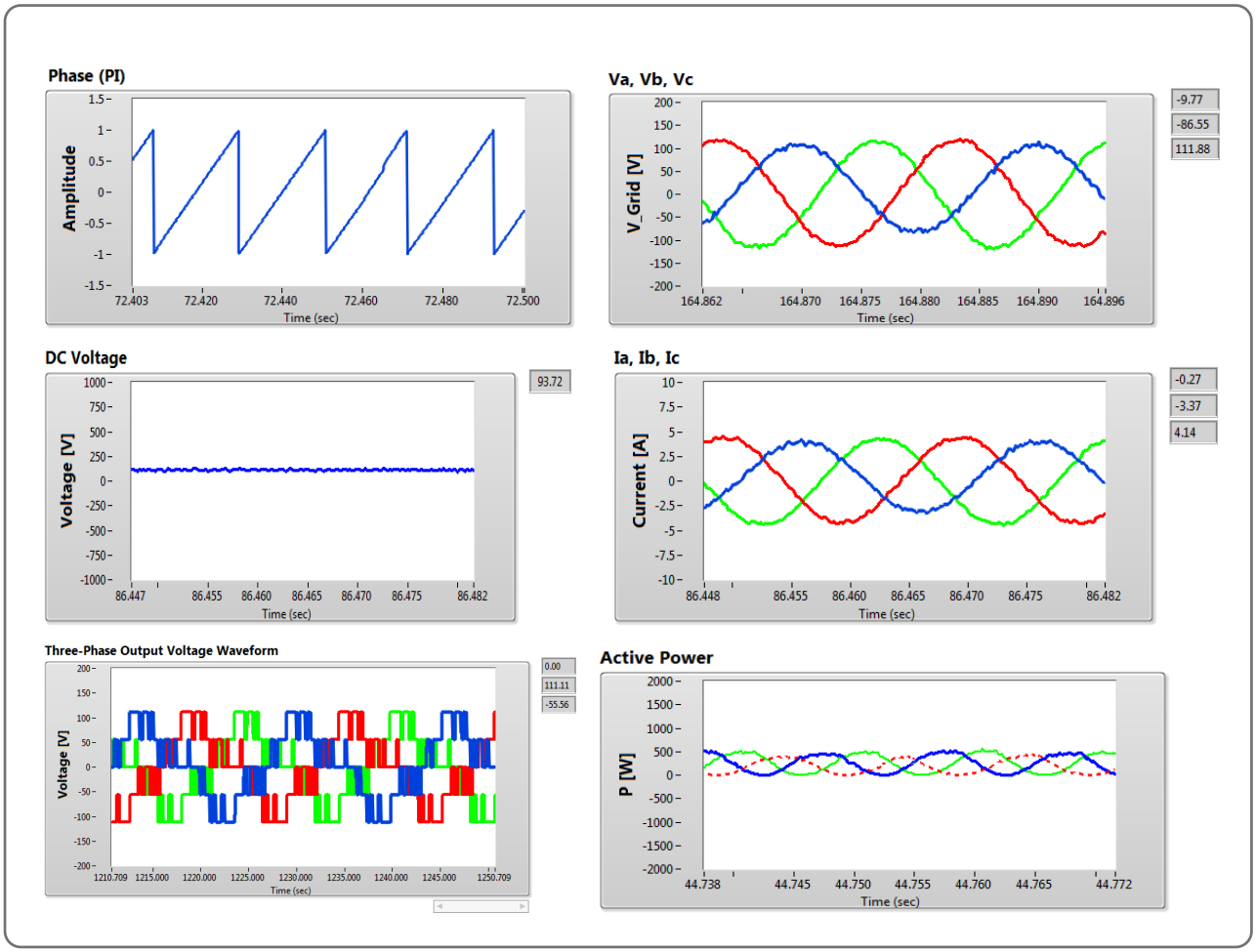
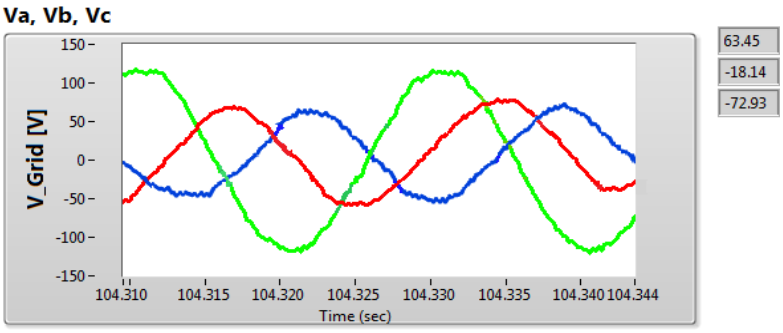


Figure 6.23: Measured waveforms in LabVIEW RT.

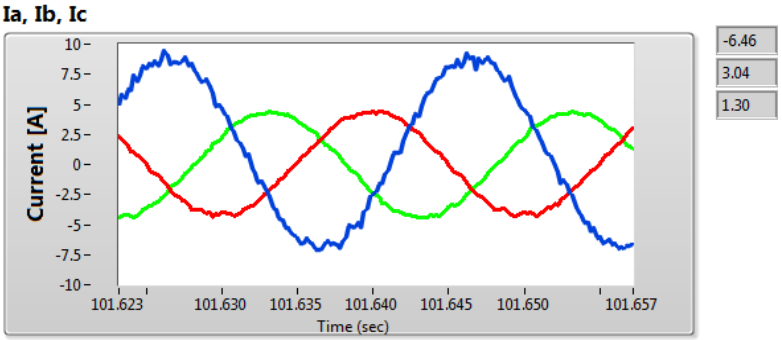
6.3.3. Discussions

In this section, the impact of the dc component minimization technique on the proposed grid-connected converter is shown when two main grid voltage sags occur. According to the simulation results in section 3.4.2, both the single-phase (Type-B) and phase-to-phase (Type-C) voltage sags are the two most frequent asymmetrical voltage sags that occur in the grid. While the impact of the substation transformer winding connection results in a Type-B voltage sag being transformed into a Type-C* voltage sag, and a Type-C is transformed into a Type-D voltage sag, as highlighted in Table 3.18.

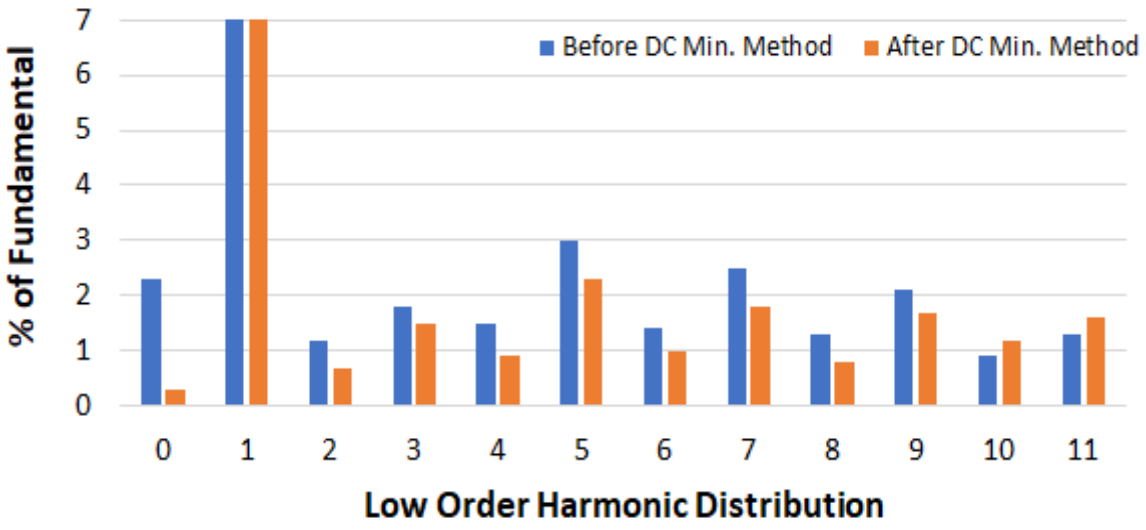
Figures 6.24(a) to 6.24(b) shows grid voltage and grid current during a Type-C* voltage sag. Furthermore, the low-order harmonic distribution of the grid current during a Type-C* voltage sag is compared before and after the dc component minimization technique is applied to the FFT analysis, as shown in Figure 6.24(c). The odd harmonics of grid current during a Type-C* voltage sag is significant with average THD estimated at 6.8% before the dc component minimization technique is activated. The proposed dc component minimization technique reduces the dc component of the distorted grid currents to about 0.3%, as shown in Figure 6.24(c). Therefore, the THD is estimated to be about 4.7%, after activating the dc component minimization technique.



(a)



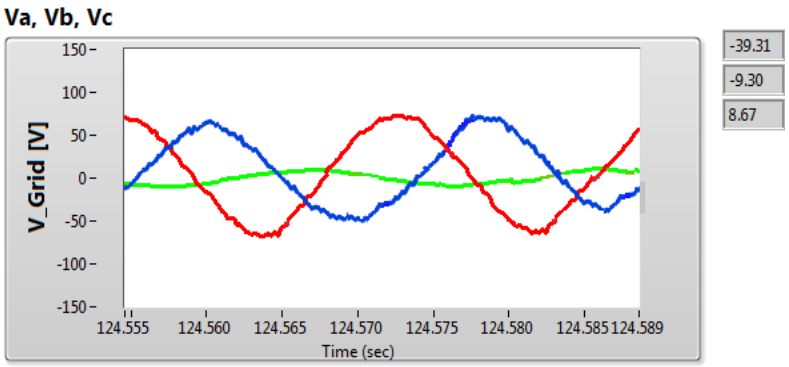
(b)



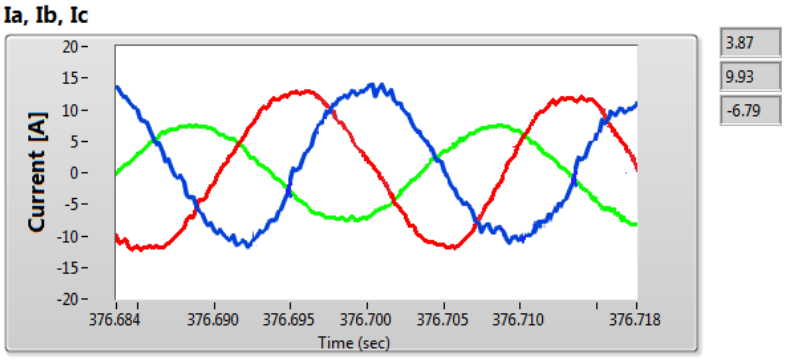
(c)

Figure 6.24: Waveforms and harmonic distribution in LabVIEW RT during Type-C* voltage sag. (a) grid voltage, (b) grid current, (c) harmonic distribution of grid current.

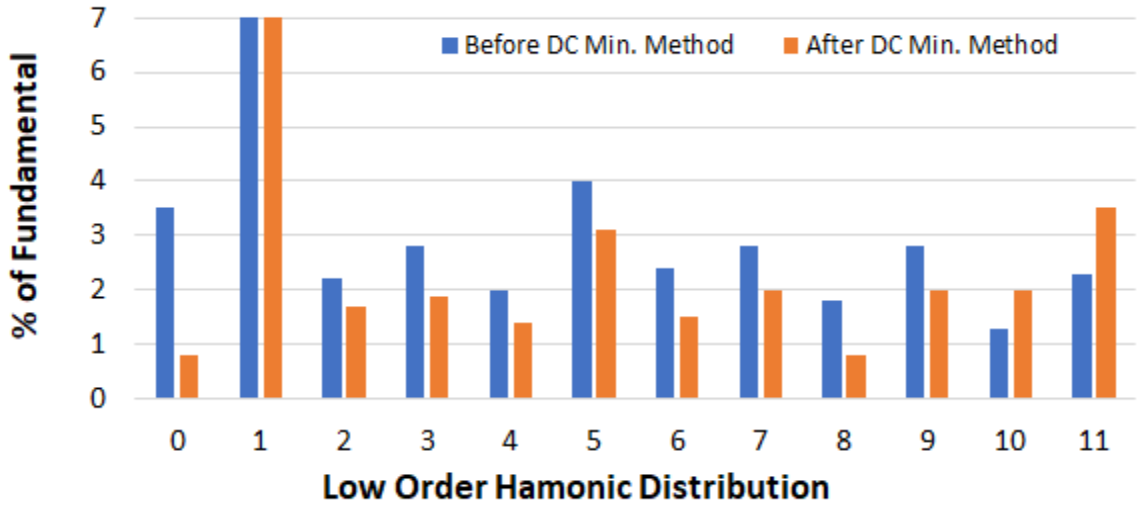
Figures 6.25(a) to 6.25(b) shows grid voltage and grid current during Type-D voltage sag. Furthermore, the low-order harmonic distribution of the grid current during a Type-D voltage sag is compared before and after the dc component minimization technique is applied to the FFT analysis, as shown in Figure 6.25(c). The odd harmonics of grid current during a Type-D voltage sag is significant with average THD estimated at 8.2% before the dc component minimization technique is activated. The proposed dc component minimization technique reduces the dc component of the distorted grid currents to about 0.8%, as shown in Figure 6.25(c). Therefore, the THD is estimated to be about 5.4%, after activating the dc component minimization technique.



(a)



(b)



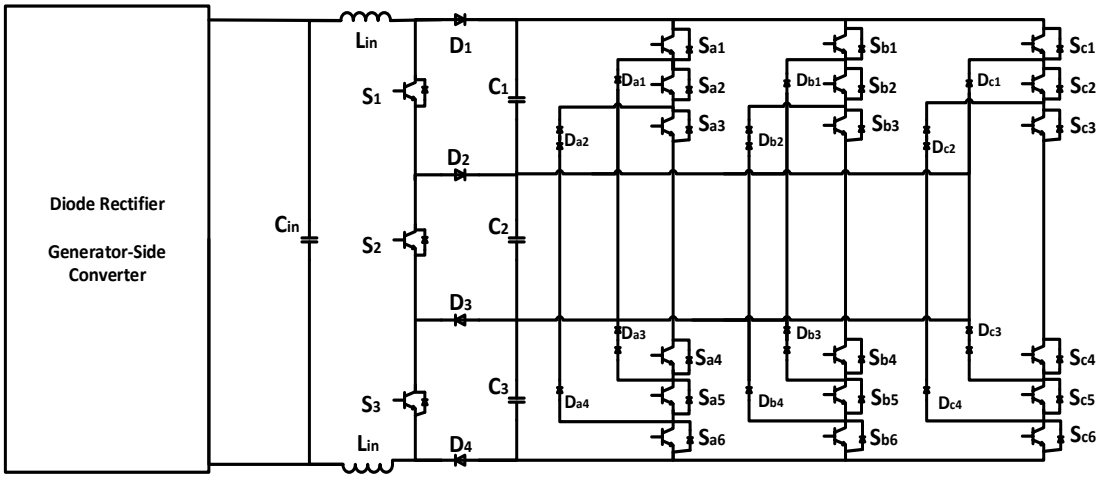
(c)

Figure 6.25: Waveforms and harmonic distribution in LabVIEW RT during Type-D voltage sag. (a) grid voltage, (b) grid current, (c) harmonic distribution of grid current.

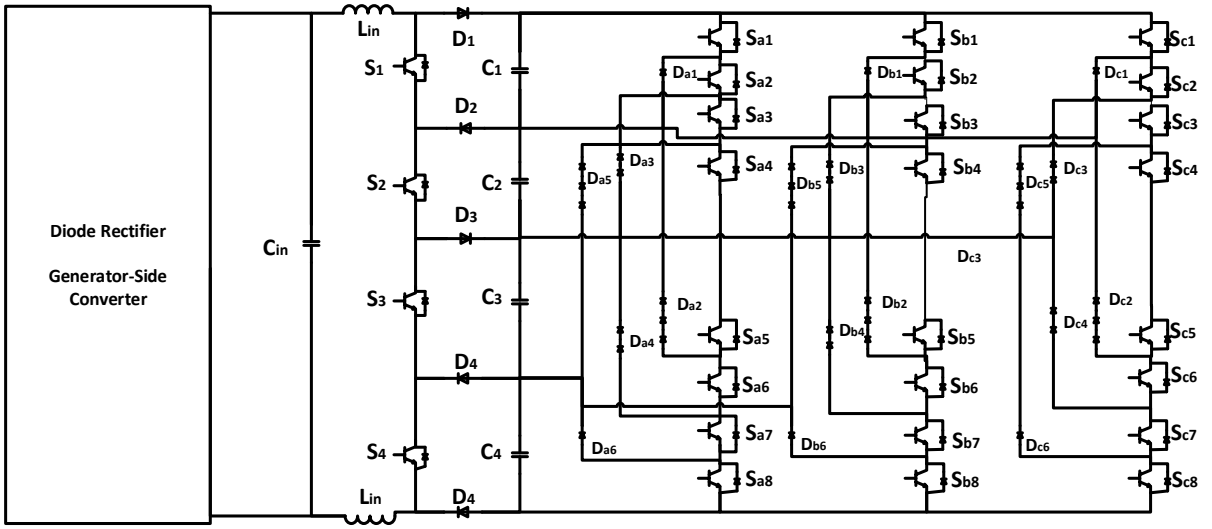
6.4. Analysis

The existing power converter configuration proposed for transformer-less WECS has been discussed and compared in Chapter 2. From the comparative evaluation carried out, the three-stage power converter configuration with a passive generator-side converter topology, 4L DC-DC converter topology and 4L-DCC grid-side converter topology (shown in Figure 6.26(a)) is estimated to have the highest efficiency, reliability, and it is cost-effective. Therefore, the five-level (5L) and seven-level (7L) variants of the configuration is illustrated in Figures 6.26(b) and 6.26(c), respectively. Therefore, the proposed converter topology is compared to the three-stage power converter configuration, emphasising the intermediate stage and grid-side converter topology.

In Chapter 3, the derivations of the 4L-NNPC, 5L-NNPC and 7L-MNNPC converter topologies have been discussed and presented. Due to these converter topologies' split dc-link configuration, the dc-link capacitors can be replaced with a tapped inductor quasi-Z-source network as discussed and presented in Chapter 4. Therefore, the 4L and 5L-tapped inductor qZS-NNPC converter topologies and 7L-tapped inductor qZS-MNNPC converter topology have been shown in Figures 6.27(a) to 6.27(c), respectively. In this section, the 4L, 5L and 7L tapped inductor qZS-NNPC & MNNPC converter topologies are compared with the existing three-stage power converter configuration shown in Figures 6.26(a) to 6.26(c). The 4L and 5L variants of both converter configurations can be deployed to the grid-side topology of a transformer-less WECS connected to a 6.6kV collection point. Also, the 7L variant of both converter configurations can be deployed to the grid-side topology of a transformer-less WECS connected to an 11kV collection point. In a nutshell, the salient features of the proposed converter topology are clarified in this section.



(a)



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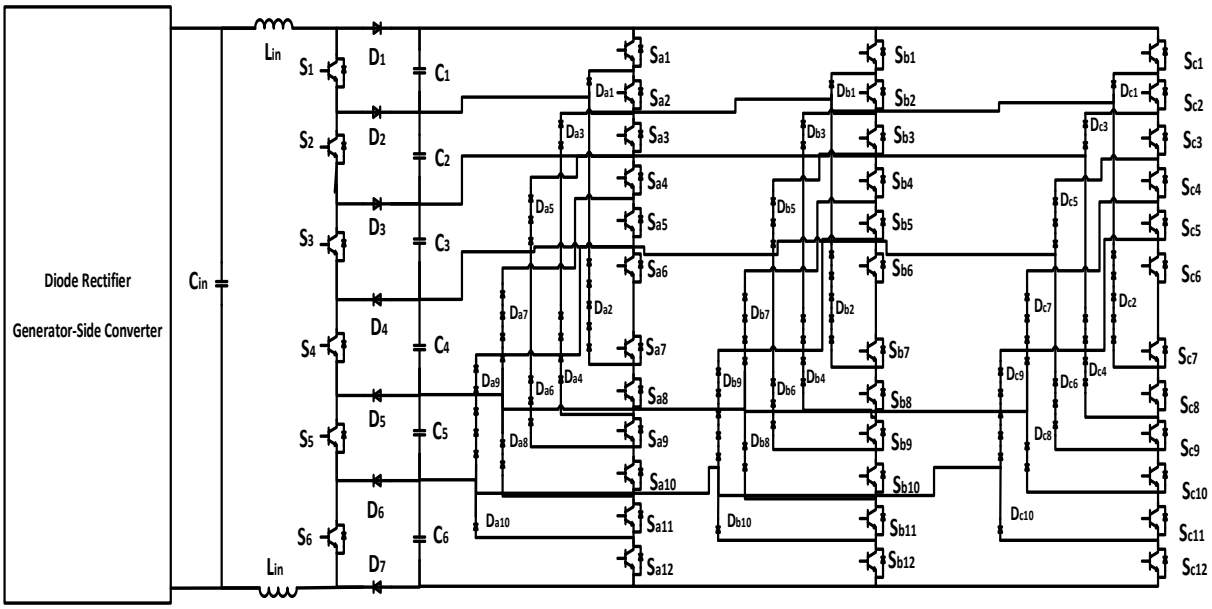
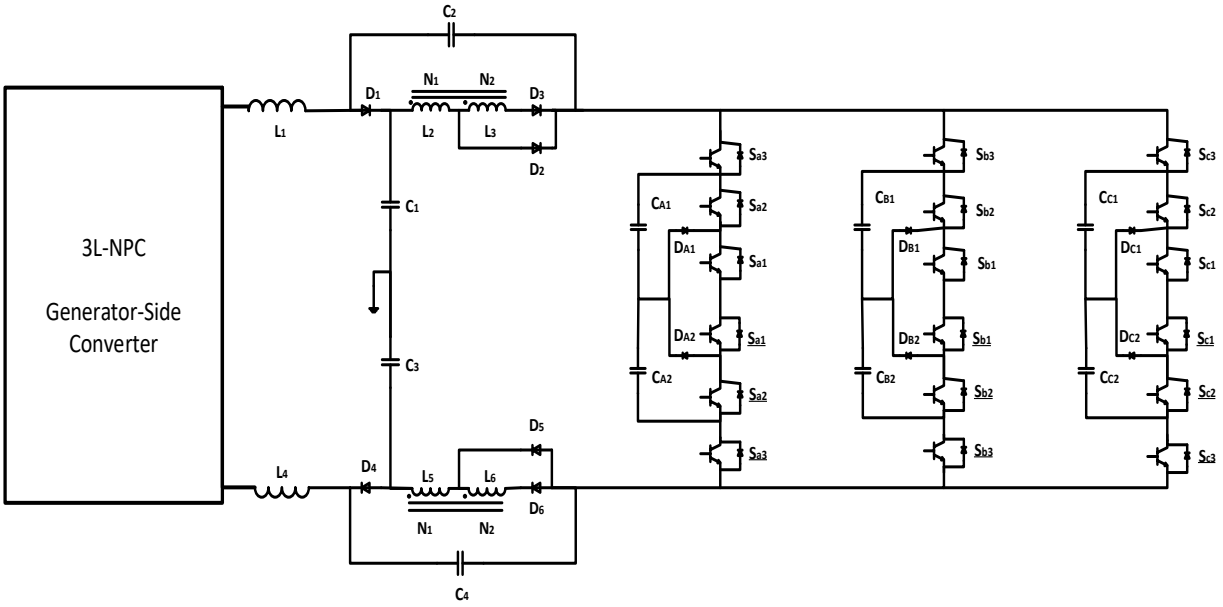
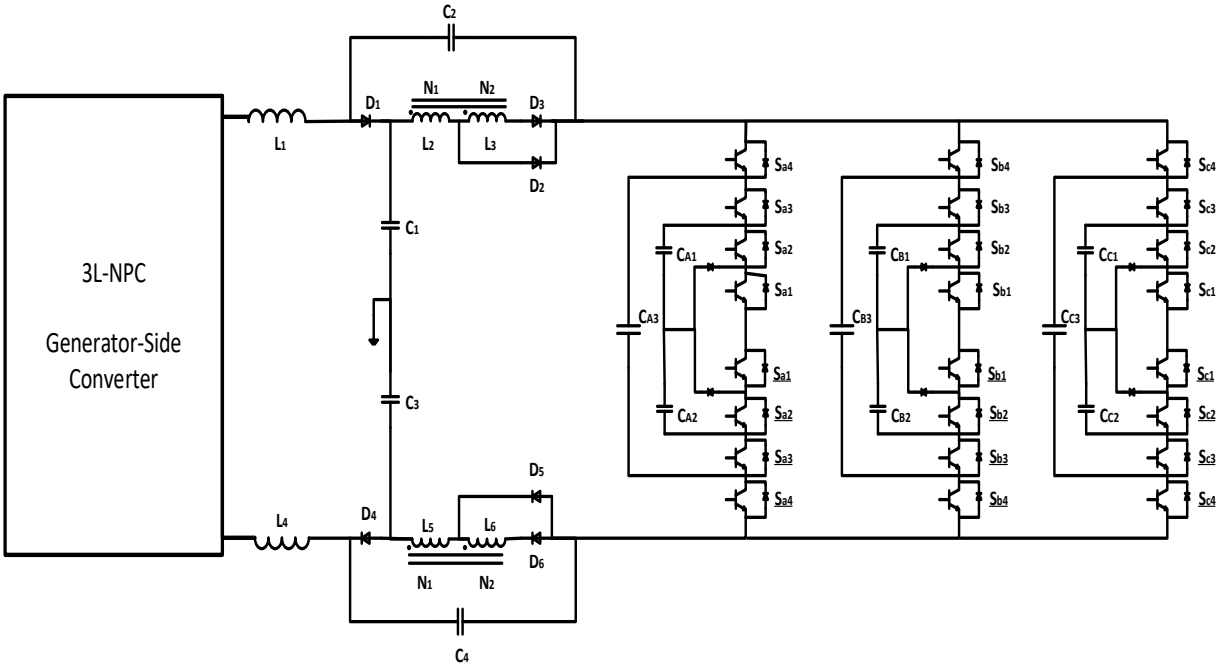


(c)

Figure 6.26. Variants of the conventional converter topology. (a) 4L DC-DC + 4L-DCC, (b) 5L DC-DC + 5L-DCC, (c) 7L DC-DC + 7L-DCC.


3L-NPC
Generator-Side
Converter
C2
N1
N2
D1
D3
L1
L2
L3
D2
C1
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4
Sa3
Sa2
Sa1
Sa1
Sa2
Sa3
CA1
CA2
DA1
DA2
Sb3
Sb2
Sb1
Sb1
Sb2
Sb3
CB1
CB2
DB1
DB2
Sc3
Sc2
Sc1
Sc1
Sc2
Sc3
CC1
CC2
DC1
DC2

(a)


3L-NPC
Generator-Side
Converter
C2
N1
N2
D1
D3
L1
L2
L3
D2
C1
C3
D5
L4
D4
L5
L6
D6
N1
N2
C4
Sa4
Sa3
Sa2
Sa1
Sa1
Sa2
Sa3
Sa4
CA1
CA2
CA3
Sb4
Sb3
Sb2
Sb1
Sb1
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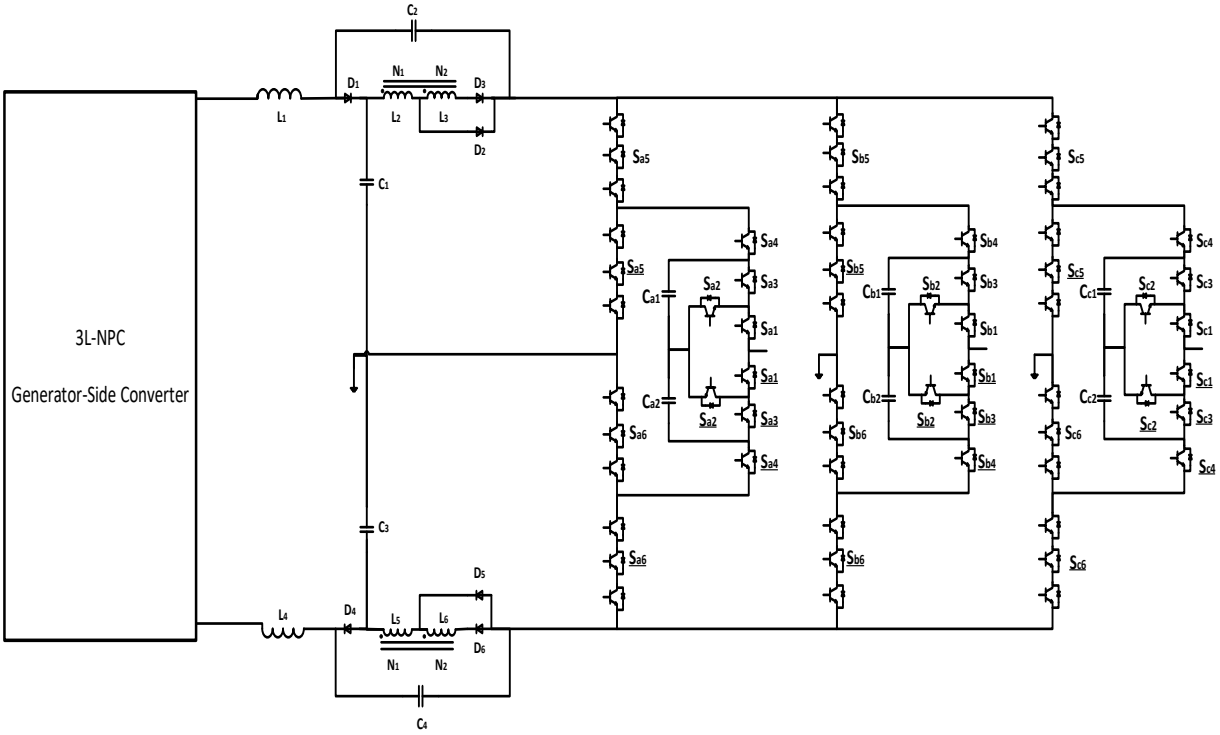
(b)



(c)

Figure 6.27: Variants of the proposed converter topology. (a) 4L tapped inductor qZS-NNPC, (b) 5L tapped inductor qZS-NNPC, (c) 7L tapped inductor qZS-MNNPC.

Table 6.9: Comparison of the proposed converter topology with a conventional converter topology in terms of component count.

Configuration	N_{ind}	N_{Diode}	N_{IGBT}	N_{cap}	$CEL_{f,c}$
	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}, \frac{V_{dc}}{2}, \frac{V_{dc}}{3}, \frac{V_{dc}}{4}, \frac{V_{dc}}{6}$	$\frac{V_{dc}}{3}, \frac{V_{dc}}{4}, \frac{V_{dc}}{6}$	$\frac{V_{dc}}{2}, \frac{V_{dc}}{3}, \frac{V_{dc}}{4}, \frac{3V_{dc}}{4}, \frac{V_{dc}}{6}$	
C1	2	$-; -; 22; -; -$	$22; -; -$	$-; 3; -; -; -$	4.13
C1*	4	$2; 4; 6; -; -$	$18; -; -$	$4; 3; -; -; -$	4
C2	2	$-; -; -; 41; -$	$-; 28; -$	$-; -; 4; -; -$	3.85
C2*	4	$2; 4; -; 6; -$	$-; 24; -$	$4; -; 6; 3; -$	3.65
C3	2	$-; -; -; -; 97$	$-; 42; -$	$-; -; -; -; 5$	8.36
C3*	2	$2; 4; -; -; -$	$-; 60; -$	$-; -; -; -; 6$	2.86

Table 6.9 summarizes a comparison of the component counts in the 3ph configurations of the proposed converter topologies and the existing power converter configurations. The comparison is carried out in terms of device counts such as inductors (N_{ind}), power semiconductor devices (N_{IGBT}), diodes (N_{Diode}), and capacitors (N_{cap}). Each device category

is based on its voltage rating while the current rating is assumed to be equal for all devices. Furthermore, the 4L DC-DC + 4L-DCC, proposed 4L-tapped inductor qZS-NNPC, 5L DC-DC + 5L-DCC, proposed 5L-tapped inductor qZS-NNPC, 7L DC-DC + 7L-DCC, and proposed 7L-tapped inductor qZS-MNNPC are represented with C1, C1*, C2, C2*, C3, and C3*, respectively in Table 6.9. The number of components counts in the existing configurations have been compared with the proposed converter topologies using the $CEL_{f,c}$ in Table 6.9. The $CEL_{f,c}$ have been presented in Chapter 2 under the comparative benchmark factor (CBF). Therefore, the 4L DC-DC + 4L-DCC has about 3.25% more components than the proposed 4L-tapped inductor qZS-NNPC. Also, the 5L DC-DC + 5L-DCC has about 5.48% more components than the proposed 5L-tapped inductor qZS-NNPC. While the 7L DC-DC + 7L-DCC have more than twice the number of components present in the proposed 7L-tapped inductor qZS-MNNPC. Based on the $CEL_{f,c}$, the proposed converter topology should be more efficient and reliable than its compared counterpart.

6.4.1. Efficiency and Loss Distribution Analysis

A. Efficiency Analysis

The efficiency of the proposed 5L-tapped inductor qZS-NNPC converter topology is studied under different switching frequencies and loads. The switching frequency is varied from $1kHz$ to $5kHz$ in intervals of $2kHz$, while the load is changed from $0.1kW$ to $1kW$ in intervals of $0.1kW$. Figure 6.28 shows the efficiency of the proposed converter topology at different output powers and switching frequencies. The efficiency of the proposed converter topology is increased with increasing load conditions, while the efficiency is reduced with increasing switching frequency. While the proposed converter topology was operated at a switching frequency of $5kHz$, its efficiency is increased from 83% to 96.2% whilst the load is increased from $0.1kW$ to $1kW$. However, the efficiency of the proposed converter topology is decreased from 95.9% to 92.1% when the switching frequency is increased from $1kHz$ to $5kHz$ at $0.5kW$ load. Furthermore, the system specifications utilized for the efficiency analysis are based on parameters stated in Table 6.10. The specifications of the inductors and capacitors used in the proposed converter topology have already been defined in Table 4.9. Therefore, all the system parameters were kept constant while investigating the impacts of different switching frequencies and loads on the overall efficiency.

Based on the previous component evaluation, the 5L DC-DC and 5L-DCC converter topology are the closest to the proposed converter topology based on voltage level and topological structure. Therefore, the efficiencies of both converter topologies are evaluated using the same parameters under different loads, as illustrated in Figure 6.29. From the comparative evaluation, the proposed topology showed a higher efficiency under all the load conditions while operating at a switching frequency of $5kHz$.

Table 6.10: Specifications of power semiconductor devices utilized in the efficiency analysis.

Component	Parameter	Value
47N60C3	Drain-source voltage (V_{DS})	$650V$
	Gate threshold voltage $(V_{GS(th)})$	$3V$
	On-state resistance $(R_{DS(on)})$	0.16Ω
	Junction temperature (T_j)	$150℃$
IDP30E65D1	Repetitive peak reverse voltage (V_{RMM})	$650V$
	Diode forward voltage (V_F)	$1.7V$
	Diode on-state resistance (R_{on})	0.08Ω
	Switching frequency (f_{sw})	$1, 3, 5\ kHz$
	Modulation index (m_a)	0.9
	Maximum output power (P_{out})	$1kW$

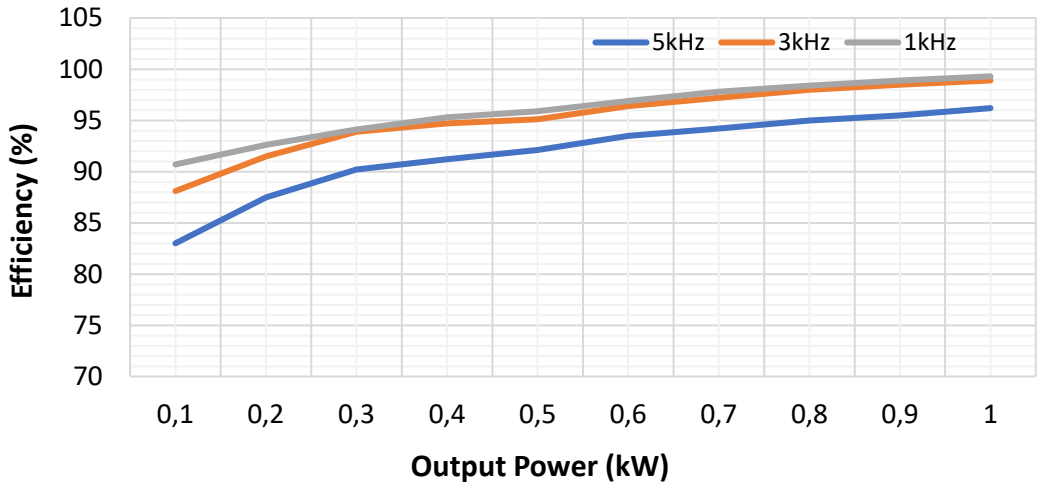


Figure 6.28: Efficiency evaluation of the proposed converter topology at the different switching frequency and output power.

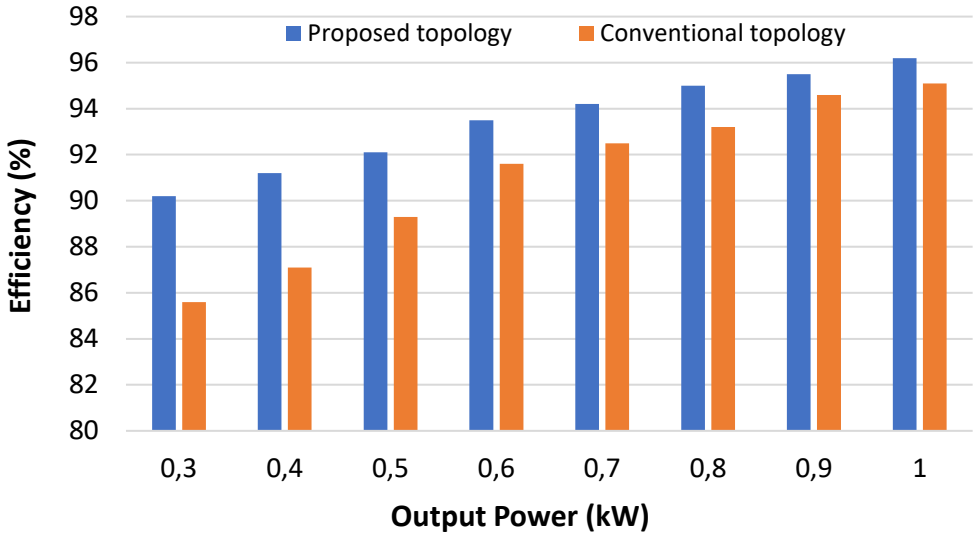


Figure 6.29: Efficiency comparison between the proposed converter topology and conventional converter topology.

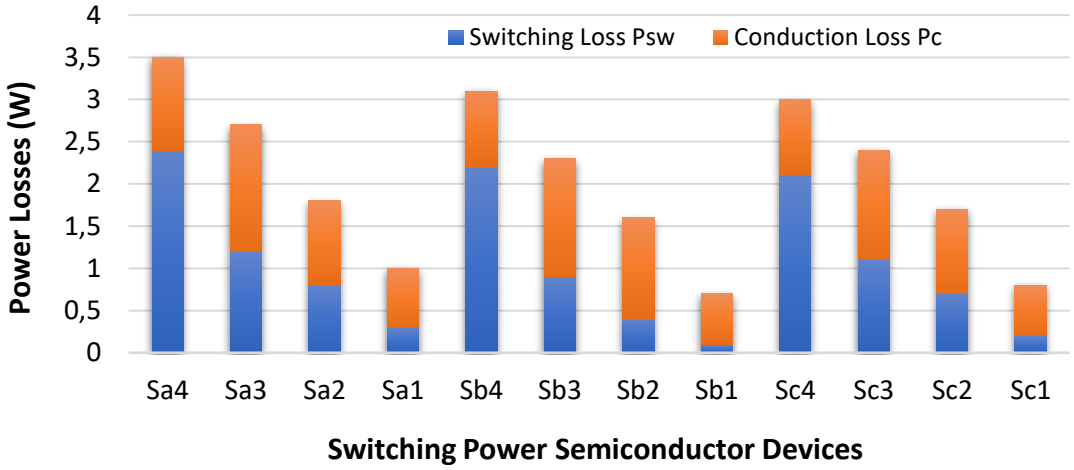


Figure 6.30: Loss distribution in the switching power semiconductor devices at 5kHz switching frequency and 1kW output power.

B. Loss Distribution Analysis

The dominant losses in the proposed converter topology are generated from the power semiconductor devices through switching (P_{sw}) and conduction losses (P_c), respectively [145]-[149]. Therefore, the loss distribution of the switching power semiconductor devices of a 3ph 5L-tapped inductor qZS-NNPC converter topology is investigated and classified into switching and conduction losses. Figure 6.30 shows the loss distribution amongst the switching power semiconductor devices while operating at a switching frequency of $5kHz$ and the output

power of $1kW$. From the loss distribution illustrated in Figure 6.30, the conduction period and voltage level at the switching instant is directly proportional to the switching and conduction losses of the converter topology. The switching losses in S_{a4}, S_{b4}, and S_{c4} are much higher than the other switching power semiconductor devices in the topology due to the higher blocking voltage. On the other hand, the switching power semiconductor devices S_{a3}, S_{b3}, and S_{c3} have higher conduction losses because of the extended conduction period due to the clamping devices in the current path of the topology. However, S_{a1}, S_{b1}, and S_{c1} shows both lower switching and conduction losses.

The measured loss distribution of all the components of the proposed converter topology at the output power of $1kW$ is illustrated in Figure 6.31. The switching power semiconductor devices (47N60C3) contributes more than 40% of the total losses in the proposed converter topology. The losses associated with switching power semiconductor devices can be minimized using lower voltage rated with low on-state resistance devices [145]-[149]. Also, the clamping diodes and qZS network diodes contribute almost 30% to the overall losses in the proposed converter topology. Furthermore, the calculated losses in the proposed converter topology are compared to the conventional topology using equations presented in [148], [149], [224], [225] and system specification presented in Table 6.10 and Table 4.9, respectively. It is obvious from Figure 6.32, that the total power loss of the proposed converter topology is less than the conventional topology.

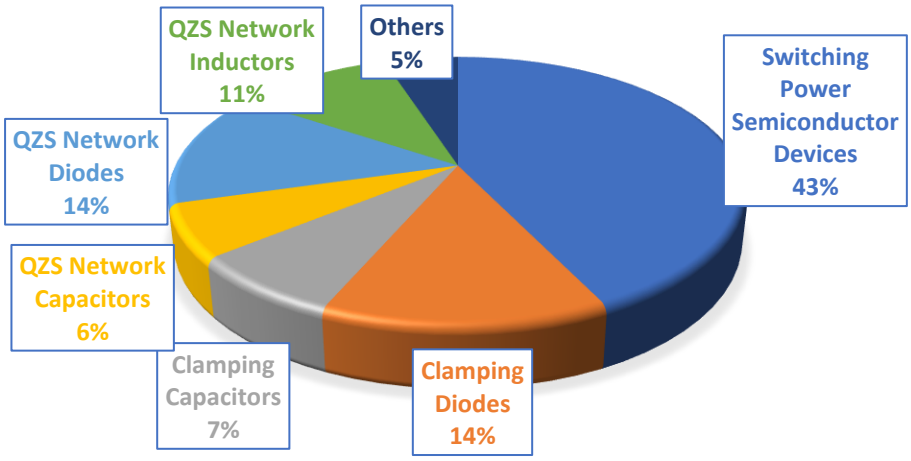


Figure 6.31: Measured loss distribution of the proposed converter topology at 1kW output power.

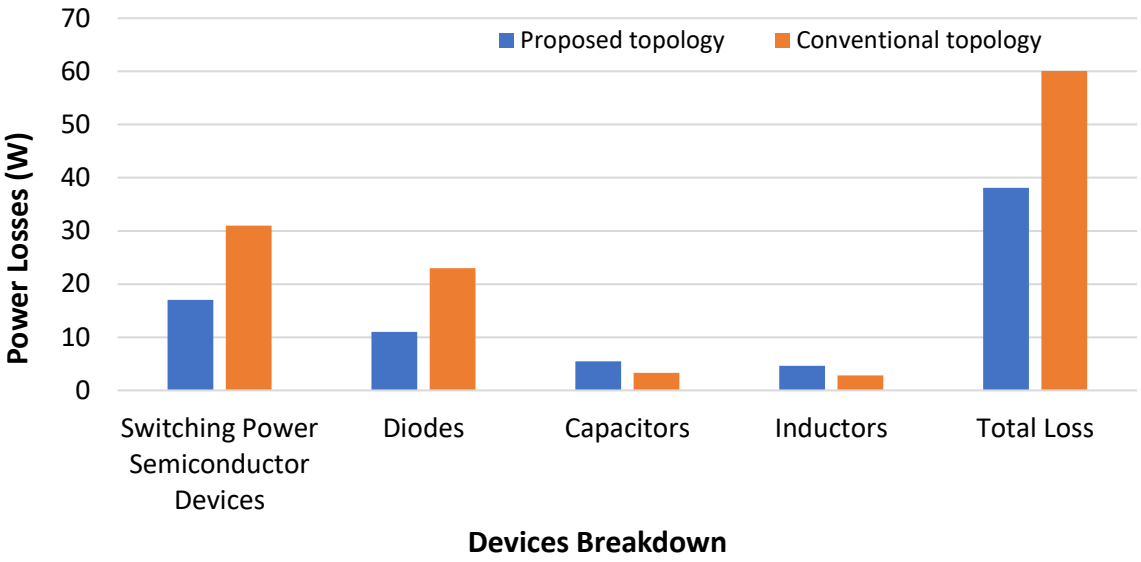


Figure 6.32: Calculated loss distribution of the proposed converter topology and conventional converter topology.

6.4.2. Cost Analysis

In this section, the associated cost of the proposed converter topology is evaluated and compared with the conventional converter topology presented in the previous sections. Therefore, the total cost of the proposed converter topology consists of the initial cost, operational and maintenance (O&M) cost and power loss cost [103].

The initial cost of the proposed converter topology includes the summation of its critical components (i.e., power semiconductor devices, capacitors, and inductors) and auxiliary components (i.e., cooling system, printed circuit boards (PCBs) and housing system). The cost associated with the auxiliary components is assumed to be 10% of the total cost of the critical components [103], [117], [118]. The critical component cost model is based on specifications obtained from the manufacturers' database on power semiconductor devices, capacitors, and inductors presented in [117]. Therefore, the cost models of the power semiconductor device, capacitor, and inductor in [117] are stated as follows:

$$\sum psd = \sum_n \sigma_c A_c + \sum pack \tag{6.19}$$

$$\sum ind = \sum \mathrm{M} + \sum \mathcal{L} \tag{6.20}$$

$$\sum cap = \mathcal{B}_a V_r + \mathrm{C}_a C_r V_r^2 \tag{6.21}$$

where σ_c is the unit price per chip area based on the semiconductor technology, A_c is the chip area of the power semiconductor device, $\sum pack$ is package technology price, $\sum \mathrm{M}$ represents the material cost of the inductor, $\sum \mathcal{L}$ is the labour cost associated with the manufacturing of the inductor, V_r is the rated capacitor (i.e., clamping capacitor and dc-link capacitor) voltage, and C_r is the rated capacitance of the clamping capacitor and dc-link capacitor. A typical value for $\mathcal{B}_a$ and C_a are $1.566 \times 10^{-3}\ \$/V$ and $2.698 \times 10^{-3}\ \$/\mu F \cdot V^2$, as stated in Table 2.12. Also, the associated cost components of the inductor have been indicated in Table 2.11, as obtained from [117]-[119].

Therefore, the average cost per chip size of the power semiconductor devices (47N60C3 and IDP30E65D1) deployed in the converter topologies are highlighted in Table 6.11 [117]. The chip area is based on the current rating of the converter topology and the current density of the power semiconductor device [117], [119]. Therefore, 47N60C3 and IDP30E65D1 are based on the TO-247 and TO-220 package types stated on their respective datasheets, with their unit price being $\$0.66/\text{unit}$, and $\$0.25/\text{unit}$, respectively [117]. Figure 6.33 shows the comparative evaluation of the initial cost associated with the proposed converter topology and conventional converter topology. Due to the low operating switching frequency of the proposed converter topology, the passive components (i.e., capacitor and inductor) within the critical component category have a relatively higher cost value. However, the active components (i.e., switching power semiconductor devices and diodes) of the conventional converter topology have a much higher cost value when compared to the proposed converter topology. Furthermore, the overall initial cost of the proposed converter topology is about 0.4% higher than the conventional converter topology.

Table 6.11: Average cost per chip size for 47N60C3 & IDP30E65D1

Device	Cost
Silicon MOSFET (47N60C3)	$\$0.15/mm^2$
Silicon Diode (IDP30E65D1)	$\$0.05/mm^2$

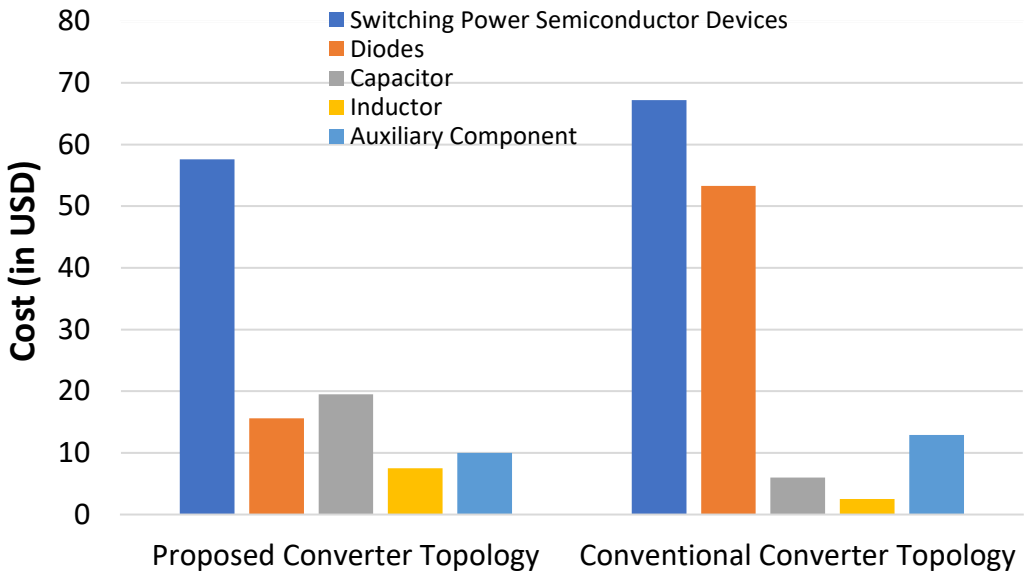


Figure 6.33: Cost breakdown of the critical components and auxiliary components of the proposed converter topology and conventional converter topology.

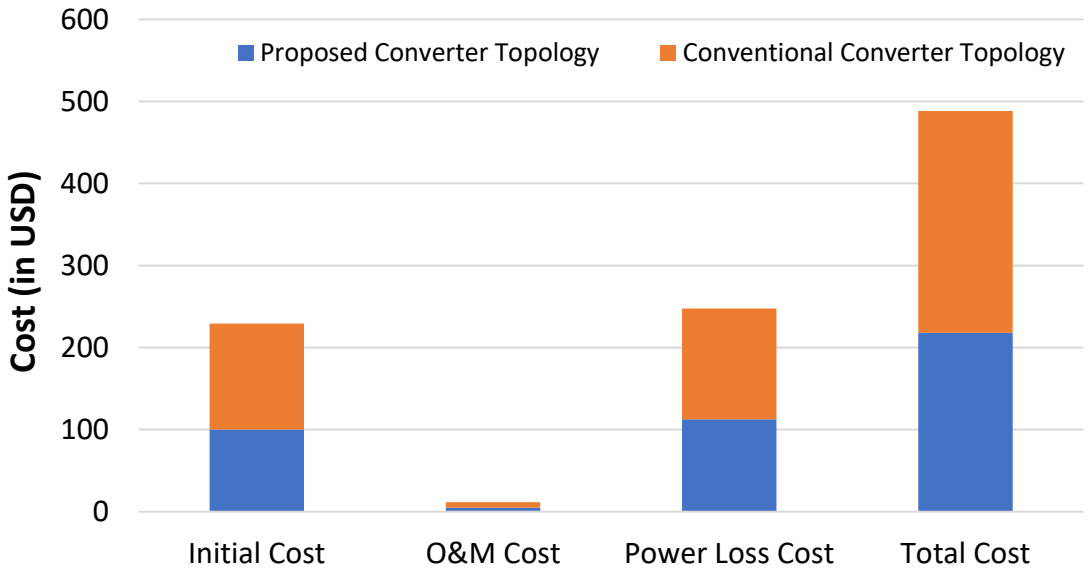


Figure 6.34: Total cost comparison of the proposed converter topology and conventional converter topology.

The annual O&M cost of the converter topology is estimated to be about 5% to 6% of the initial cost as stated in [103]. Furthermore, the power loss cost of the converter topology is assumed to be 10cents/kWh [103], the annual power loss cost of the converter topology has been presented in Section 2.4.1, as obtained from [103]. Figure 6.34 shows that the total cost

of the proposed converter topology is about 19% less than the conventional converter topology. The high-cost component of the conventional converter topology is because of the high count of power semiconductor devices as indicated in Table 6.9.

6.5. Conclusion

In this chapter, the power hardware-in-loop (PHIL) configuration of the experimental test rig has been described extensively. The technical requirements for the design and development of the converter circuitry, gate driver circuitry and measurement board circuitry have been presented. Also, the specific parameters of the NI-PXI system have been highlighted extensively. Furthermore, the design and development of the LCL grid-side filter topology were presented.

Secondly, the grid connection of the proposed converter topology in the PHIL configuration has been discussed extensively. The main considerations for the design and development of the grid synchronization and closed-loop control algorithm within the LabVIEW FPGA and LabVIEW RT environment have been presented.

Thirdly, the efficiency of the proposed converter topology has been evaluated by varying the switching frequency and loads. For instance, the efficiency is decreased from 95.9% to 92.1% when the switching frequency is increased from $1kHz$ to $5kHz$ at $0.5kW$ load. Furthermore, the proposed converter topology is more efficient than the 5L DC-DC + 5L-DCC topology (i.e., the conventional converter topology). Also, the cost analysis of the proposed converter topology and the conventional converter topology shows that it is more economical to deploy the proposed converter topology at the grid-side of a transformer-less WECS.

Chapter 7

This chapter summarizes the research work carried out in this thesis by highlighting the main contributions and how the research addresses the outlined power converter topology-related design issues in a transformer-less WECS, as stated in Chapter 1. Furthermore, the main contributions and recommendations for future work regarding critical research areas have been presented in this chapter.

7.1. Summary

The research work carried out focuses on the analysis, design, and development of a single-stage multilevel power converter topology applied to the grid-side of transformer-less renewable energy systems. The main objective of this thesis was to present a power converter topology with improved efficiency and cost-effectiveness for transformer-less WECS applications. The thesis proposes a novel five-level converter topology with two tapped inductor quasi-impedance-source networks replacing its two dc-link capacitors in a split dc-link configuration. Furthermore, the power conversion stage in a transformer-less WECS is reduced to two stages from the generator-side converter to the grid-side converter topologies. By reducing the power conversion stages, the cost of the power conversion stage can be reduced 19% and efficiency can be improved to 97% when compared to a conventional converter configuration. However, optimization of the tapped inductor quasi-impedance-source networks would be required to further reduce the size and efficiency of the converter topology.

The grid compliance of the proposed converter topology was studied and investigated by first reviewing existing dc component minimization techniques. Secondly, the detailed analysis of the generation of dc components from the asymmetrical characteristics of switching power semiconductor devices by considering the delay in the gating signals and disparity in the switching power semiconductor devices. Thirdly, the proposed dc component minimization technique that combines detection hardware with a digital filtering method was presented and validated through theoretical analysis and experimental verification. However, the accuracy of the dc component minimization technique can be further improved by developing a customized current sensor to detect the dc components before minimize the injected dc current.

7.2. Main Contributions

The achievements and contributions of the presented research work are stated as follows:

- **An overview of the existing power converter configurations for transformer-less WECS is presented:**

  A comprehensive review is presented by classifying the existing power converter configuration into two categories: generator-converter configuration and three-stage power converter configuration. The features, technical issues, and associated drawbacks of each power converter configuration have been analysed and discussed extensively.

  These existing power converter configurations are compared and evaluated in a transformer-less WECS in device count, voltage boosting topology, and grid compliance. Furthermore, a comparative benchmark factor (CBF) was proposed to compare and evaluate the existing power converter configurations for transformer-less WECS configuration.

- **Four-level NNPC and Five-level NNPC converter topology are proposed for 6.6kV transformer-less WECS:**

  The theoretical derivations of the four-level and five-level NNPC converter topology deployed as the grid-side converter topology in a transformer-less WECS have been presented. Furthermore, these topologies' design specifications and constraints for a transformer-less WECS application were discussed extensively in Chapter 3. The design specifications were verified through simulations carried out using MATLAB/Simulink software.

- **Seven-level MNNPC converter topology is proposed for 11kV transformer-less WECS:**

  - The theoretical derivation of a novel seven-level MNNPC converter topology by using three cells of the four-level NNPC converter topology was presented. Furthermore, the design specifications and constraints of the topology for a transformer-less WECS application was discussed extensively in Chapter 3. The design specifications were verified through simulations carried out using MATLAB/Simulink software. The detailed converter design for the NNPC and MNNPC converter topology deployed to the grid-side of a transformer-less WECS configuration showing its specifications,

average model, and component rating analysis have been presented. Detailed simulation results are presented for design verifications and grid-connected scenarios.

- **Tapped inductor quasi-Z-source NNPC converter topology:**

  The theoretical analysis and derivation of a tapped inductor quasi-Z-source NNPC converter topology have been presented in the thesis. The switching states of a five-level tapped inductor quasi-Z-source NNPC converter topology was presented. The theoretical analysis, design, and development of the tapped inductor quasi-Z-source network component of the proposed converter topology is presented. A modulation technique based on the direct digital synthesis method and voltage balancing control scheme for the clamping capacitors was introduced and implemented through the NI-FPGA platform.

- **DC component minimization technique:**

  A review of the existing dc component minimization techniques for three-phase grid-connected converter topologies has been compared and evaluated based on their detection method, auxiliary hardware addition, and accuracy level. Furthermore, a mathematical analysis of the dc component generated by the five-level tapped inductor quasi-Z-source NNPC converter topology was presented. A dc component minimization technique consisting of a sensing and voltage measurement circuit with a digital notch filter was introduced in Chapter 5.

- **Simulation and experimental verifications of the proposed converter topology:**

  All the simulations carried out were done within the MATLAB/Simulink environment. These simulation results were presented in Chapter 3 and Chapter 4 of the thesis.

  A low-power prototype of the proposed three-phase five-level tapped inductor quasi-Z-source NNPC converter topology has been developed and tested in the power hardware-in-loop (PHIL) experimental rig. The digital control algorithm was developed in the NI-FPGA platform.

7.3. Future Work

Therefore, further work can be carried out in the following areas:

- Optimization of the tapped inductor quasi-Z-source network further improves the efficiency and cost of the novel tapped inductor quasi-Z-source NNPC converter topology. This would be an essential contribution to the ongoing research in power converter configurations for transformer-less WECS.

- Analysis, design, and development of a back-to-back power converter configuration with the proposed converter topology at the grid-side of the transformer-less WECS and conventional multilevel converter topology (such as 3L-DCC, 4L-NNPC, and 5L-NNPC) at the generator-side of the transformer-less WECS. The performance of the proposed converter topology combined with generator-side converter topology must be studied and analysed to understand further the limitation and area of improvements of the topology in a transformer-less WECS.

- Analysis, design, and development of a space vector modulation (SVM) scheme for the proposed converter topology. The SVM scheme provides a much higher voltage utilization and better output waveforms. The upper and lower shoot-through states would be inserted within the switching sequence. Due to the high number of possible switching states, the computational burden will be further increased. Therefore, optimization techniques will be required for the FPGA implementation of an SVM scheme.

- Investigation of other high-order grid-side filter topologies employed in a transformer-less WECS. The low switching frequency attributed to high-power, medium voltage converter topology results in the high value of both the inductive and capacitive components of the filter topology. The LCL filter topology has been utilized in this presented research work. However, other existing filter topologies, such as LCCL and LLCL [139], can be investigated for transformer-less WECS configurations.

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Appendix A

Equations for Defined Operating Conditions, Estimated Power Losses and Thermal Resistance:

A.1. Introduction

This appendix presents the mathematical equations used to obtain the defined operating conditions of the transformer-less WECS stated in Table 3.1. Furthermore, the mathematical equations for the estimated power losses and thermal resistance of the power semiconductor devices obtained through numerical calculation in MATLAB is presented in this appendix.

A.2. Equations for defined operating conditions

The parameters presented in Table 3.1 for the defined operating conditions are obtained using the following equations:

Apparent Power (S_A)

From the rated active power (P_R), the apparent power (S_A) of the system can be obtained using (A.1).

$$S_A = \frac{P_R}{cos\,\theta} \tag{A.1}$$

Where $\cos\theta$ is the power factor which is given as 0.9.

Maximum Phase Current (I_{ph})

I_{ph} is obtained using (A.2).

$$I_{ph} = \frac{S_A}{\sqrt{3}\cdot V_{LL}} \tag{A.2}$$

Where V_{LL} is the line-to-line voltage of the converter.

A.3. Equations for estimated power losses and thermal resistance of the power semiconductor devices

The conduction losses, switching losses and thermal resistances attributed to the IGBT modules are calculated based on their electrical characteristics as obtained from their respective datasheets [149], [150]-[160].

Conduction Loss:

The conduction loss of an IGBT module can be obtained using (A.3) to (A.9).

$$P_{C(module)} = P_{C(IGBT)} + P_{C(diode)} \tag{A.3}$$

$$P_{C(IGBT)} = V_{on} I_{(avg)} + R_C I_{ph}^2 \tag{A.4}$$

$$P_{C(diode)} = V_F I_{d(avg)} + R_d I_{d(rms)}^2 \tag{A.5}$$

$$I_{(avg)} = I_p \left(\frac{1}{2\pi} + \frac{m_a \cos\theta}{8} \right) \tag{A.6}$$

$$I_{d(avg)} = I_p \left(\frac{1}{2\pi} - \frac{m_a \cos\theta}{8} \right) \tag{A.7}$$

$$I_{d(rms)} = I_p \sqrt{\left(\frac{1}{8} - \frac{m_a \cos\theta}{3\pi} \right)} \tag{A.8}$$

$$m_a = \frac{V_{LL}}{\sqrt{3} \cdot (V_{dc\_max}/2)} \tag{A.9}$$

Where $P_{C(module)}$ is the total conduction loss, $P_{C(IGBT)}$ is the conduction loss of the IGBT, $P_{C(diode)}$ is the conduction loss of the freewheeling diode, V_{on} is the on-state voltage of the IGBT, R_C is the on-state resistance of the IGBT, $I_{(avg)}$ is the average current of the converter, V_F is the forward voltage of the freewheeling diode, I_d is the forward current of the freewheeling diode, R_d is the on-state resistance of the freewheeling diode and m_a is the modulation index.

The value of V_{on} is obtained from the typical on-state characteristics presented in the datasheet [150]-[160], as illustrated in Figure A.1(a). While the value of R_C is obtained from the ratio of change in voltage to change in current of the output characteristics [150]-[160], as shown in Figure A.1(b). Furthermore, the values of V_F and R_d are obtained from the diode forward characteristics as shown in Figures A.1(c) and A.1(d) respectively.

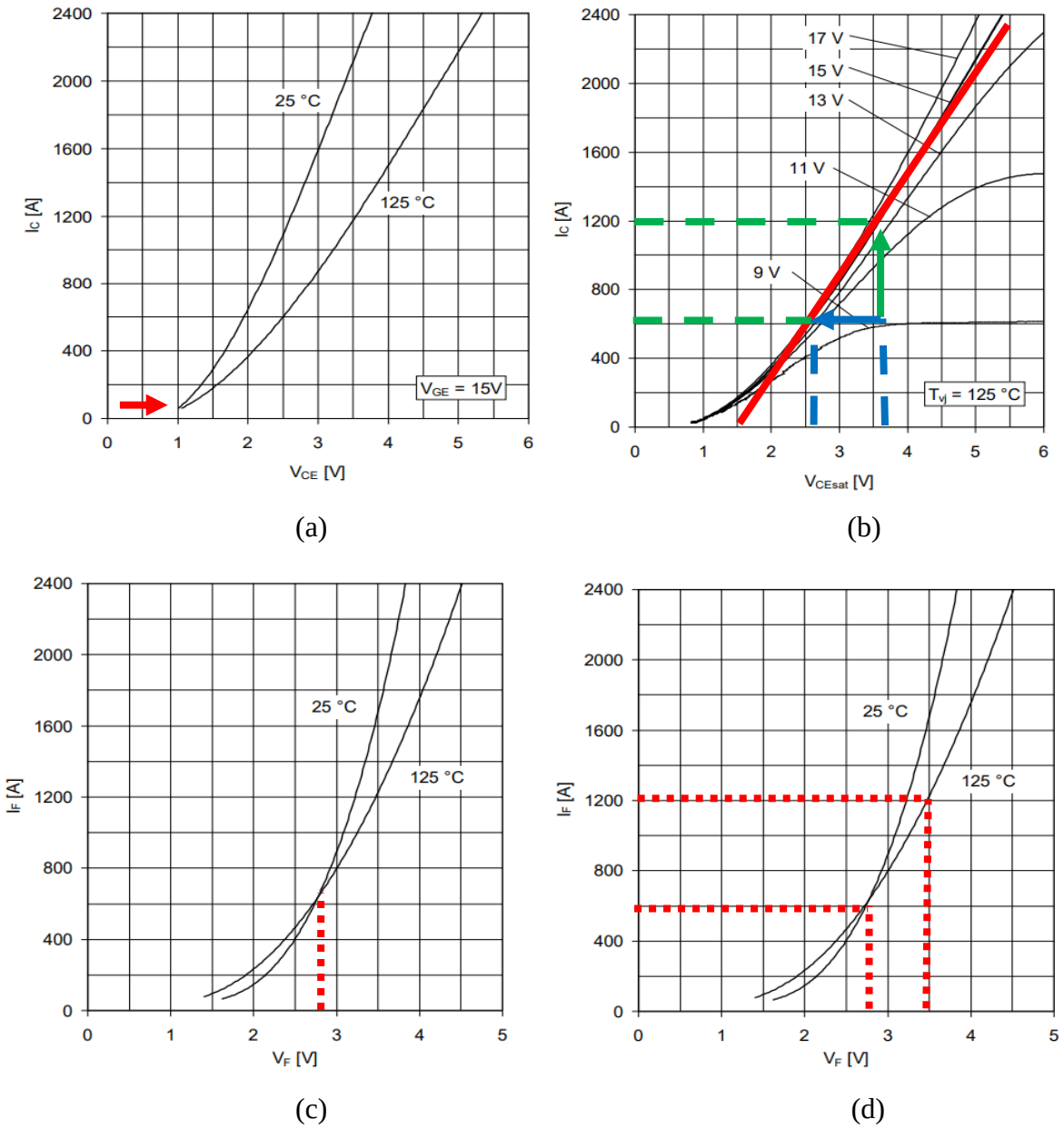


Figure A.1: The typical IGBT and freewheeling diode characteristics of 5SNA1200G450300 module. (a) On-state characteristic. (b) Output characteristic. (c) Diode forward characteristic. (d) On-state resistance of diode.

Switching Loss:

Therefore, the value of the total switching loss of an IGBT module is based on the turn-on energy loss (E_{on}), turn-off energy loss (E_{off}), and diode reverse recovery loss (E_{rec}) [76], [149]. These switching loss parameters are calculated using (A.10) to (A.12).

$$E_{on} = \frac{1}{2} V_{dc\_voltage} I_p t_{c(on)} \quad \text{(A.10)}$$

$$E_{off} = \frac{1}{2} V_{dc\_voltage} I_p t_{c(off)} \quad \text{(A.11)}$$

$$E_{rec} = E_{rec(given)} \frac{V_{Min.-Com} \cdot I_p}{V_{dc\_voltage} \cdot I_{IGBT}} \quad \text{(A.12)}$$

where $t_{c(on)}$ and $t_{c(off)}$ are defined as:

$$t_{c(on)} = t_{ri} + t_{fv} \quad \text{(A.13)}$$

$$t_{c(off)} = t_{rv} + t_{fi} \quad \text{(A.14)}$$

Where $t_{c(on)}$ is the sum of the rise time of the current during the on-state (t_{ri}) and the fall time of the voltage during the on-state (t_{fv}), $t_{c(off)}$ is the sum of the rise time of the voltage during the off-state (t_{rv}) and the fall time of the current during the off-state $(t_{fi}), E_{rec(given)}$ is the value of the diode reverse recovery loss given on the datasheet of the module. Furthermore, the power losses associated with the switching energy$(P_{sw(igbt)})$ and the diode reverse recovery $(P_{sw(igbt)})$ are obtained using (A.15) to (A.17).

$$P_{sw(igbt)} = \frac{E_{total}}{\pi} \cdot f_s \quad \text{(A.15)}$$

$$P_{sw(rec)} = \frac{E_{rec}}{\pi} \cdot f_s \quad \text{(A.16)}$$

Where E_{total} is defined as:

$$E_{total} = 1.2(E_{on} + E_{off}) \frac{V_{Min.-Com} \cdot I_p}{V_{dc\_voltage} \cdot I_{IGBT}} \quad \text{(A.17)}$$

Where f_s is the switching frequency of the grid-side converter and E_{total} is the total energy loss of the IGBT modules.

Thermal Resistance:

The values of the thermal resistance can be calculated using (A.18) to (A.22) [149].

$$R_{THJ-C} = \frac{R_{THJ-C,i} \times R_{THJ-C,d}}{R_{THJ-C,i} + R_{THJ-C,d}} \quad \text{(A.18)}$$

$$R_{THC-H,i} = \frac{R_{THJ-C,i} + R_{THJ-C,d}}{R_{THJ-C,d}} \times R_{THC-H} \quad \text{(A.19)}$$

$$R_{THC-H,d} = \frac{R_{THJ-C,i} + R_{THJ-C,d}}{R_{THJ-C,i}} \times R_{THC-H} \quad \text{(A.20)}$$

$$R_{THC-H} = \frac{R_{THJ-C} \times R_{THC-H,i}}{R_{THJ-C,i}} \quad \text{(A.22)}$$

$$R_{THh} = \frac{T_j - T_a - (P_{tot} R_{THJ-C}) - (P_{tot} R_{THC-H})}{P_{tot}} \quad \text{(A.21)}$$

where R_{THJ-C} is the thermal resistance junction-to-case, $R_{THJ-C,i}$ is the IGBT thermal resistance junction-to-case, $R_{THJ-C,d}$ is the diode thermal resistance junction-to-case, R_{THC-H} is the thermal resistance case-to-heatsink, $R_{THC-H,i}$ is the IGBT thermal resistance case-to-heatsink, and $R_{THC-H,d}$ is the diode thermal resistance case-to-heatsink. The values of $R_{THJ-C,i}$, $R_{THJ-C,d}$, $R_{THC-H,i}$ and $R_{THC-H,d}$ are stated on their respective datasheets [150]-[160].

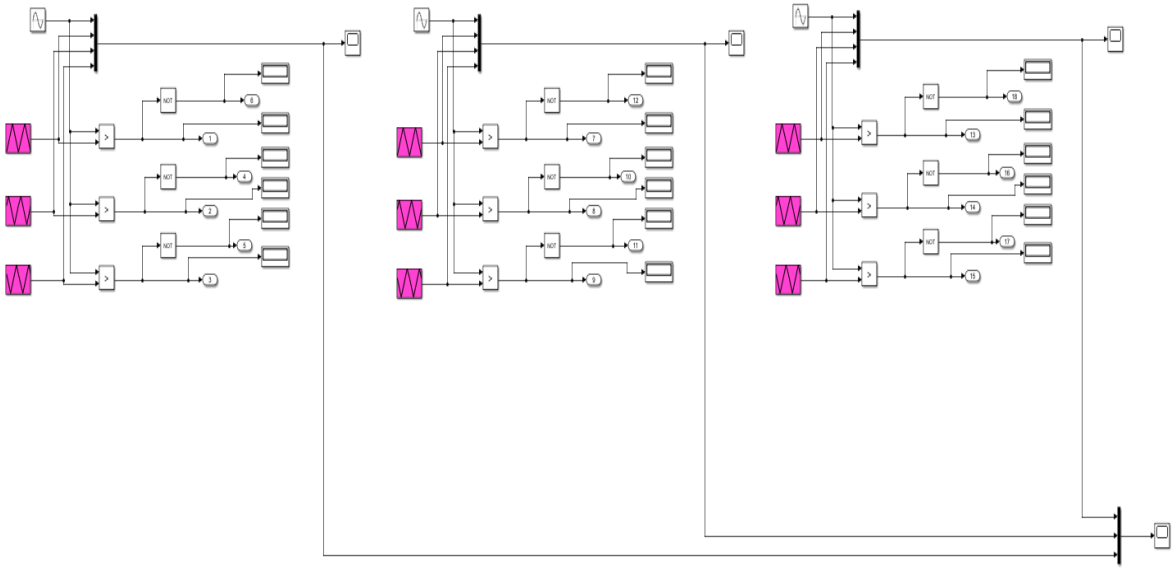
Appendix B

MATLAB/SIMULINK MODEL

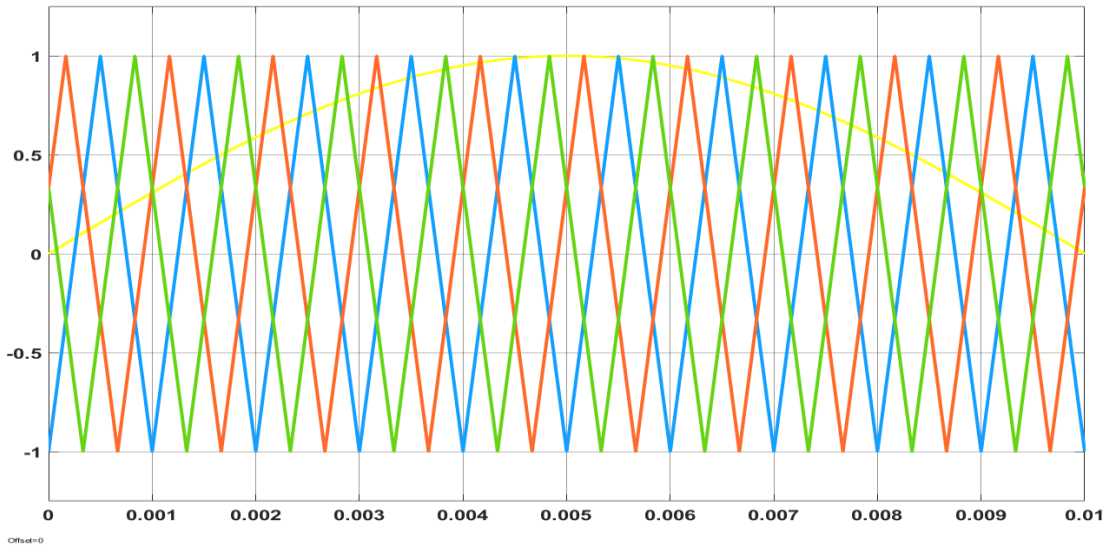
B.1. Introduction

This appendix presents the MATLAB/Simulink of the PS-PWM models of the three-phase four-level NNPC converter topology, three-phase five NNPC converter topology and three-phase seven-level MNNPC converter topology. Furthermore, the inductor design mathscript is presented.

B.2. PS-PWM Model

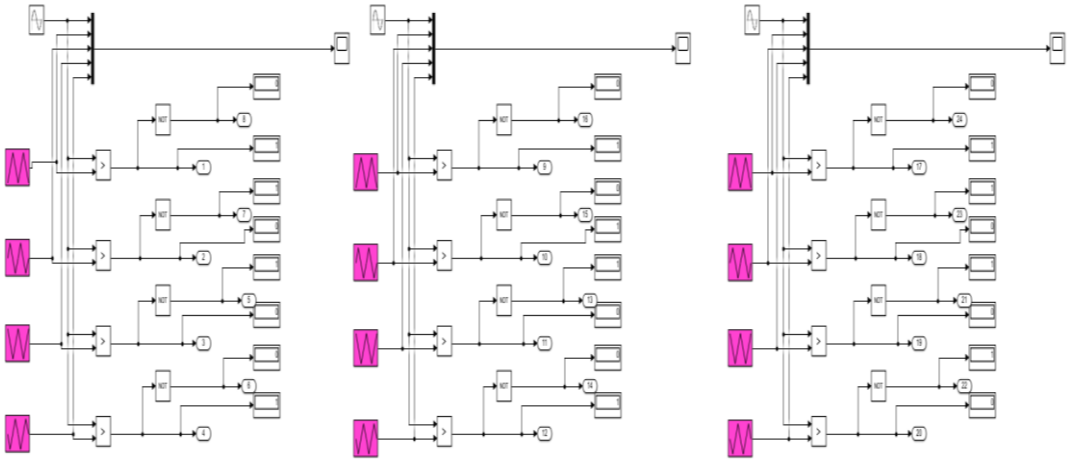


(a)

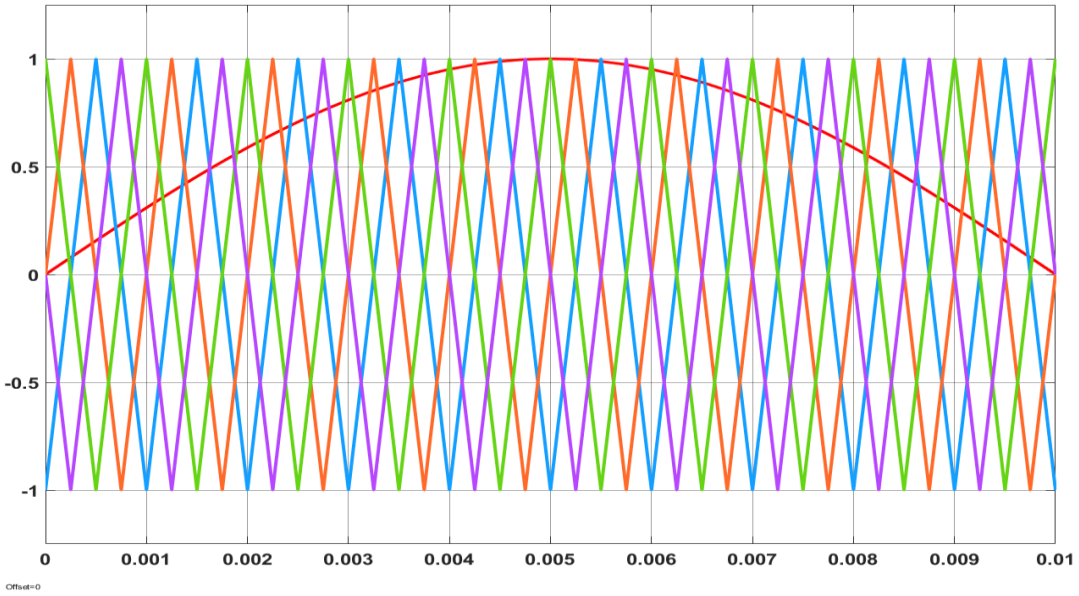


(b)

Figure B.1: Simulated PS-PWM technique for a four-level NNPC Converter. (a) Simulink model, (b) PS-PWM waveform.

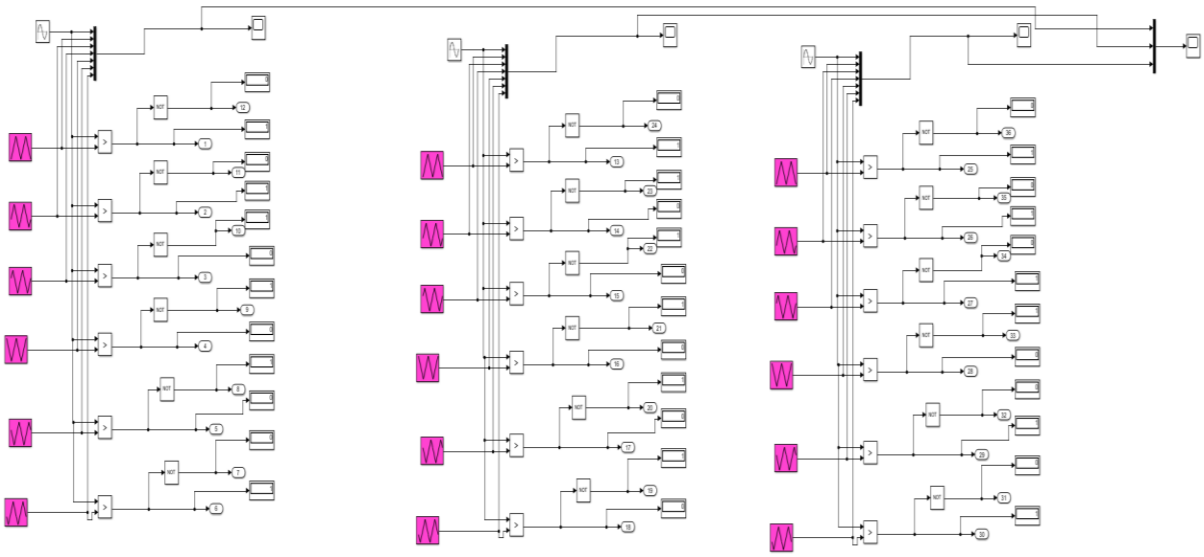


(a)

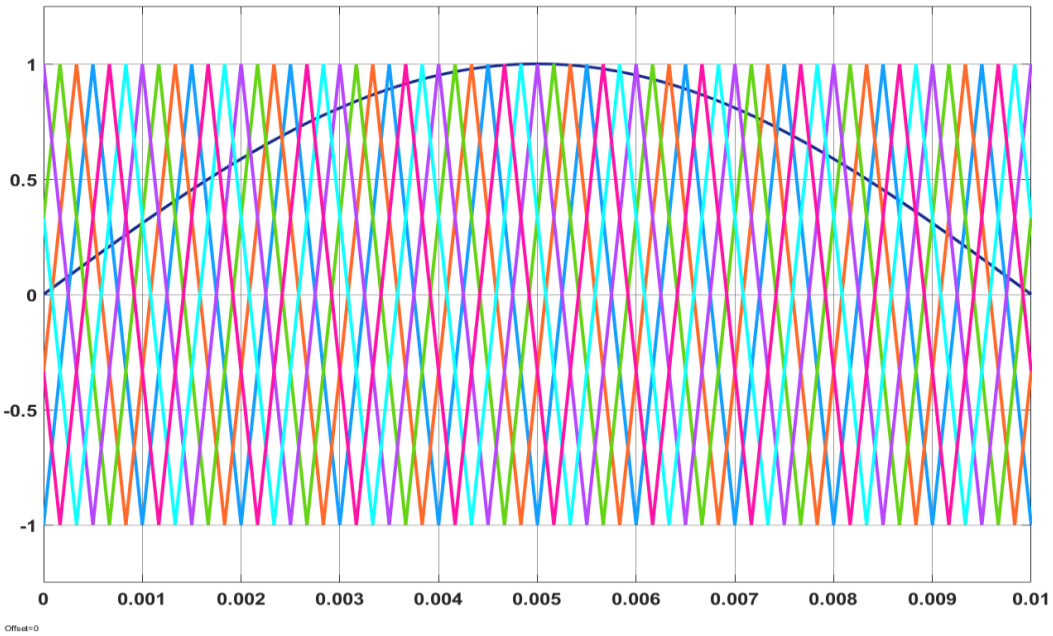


(b)

Figure B.2: Simulated PS-PWM technique for a five-level NNPC Converter. (a) Simulink model, (b) PS-PWM waveform.



(a)



(b)

Figure B.3: Simulated PS-PWM technique for a seven-level MNNPC Converter. (a) Simulink model, (b) PS-PWM waveform.

B.3 Inductor Design Mathscript

```
% Inductance calculation using EI silicon steel laminations %
% Akinola Ajayi-Obe %


%% laminations parameter

A=25.4;
B=76.2;
C=63.5;
D=12.7;
E=12.7;
F=38.1;
G=50.8;
H=12.7;

%%  Design parameters

coreDepth=30;          % core Depth in mm %
g=0;                 % air gap in mm %
N=5;                   % Number of Turns %
MurAlley=322;              % Relative Permibility of laminatioon%
MurAir=1;
MuO = 4*pi*(10^(-7));                   %relative permibility of air%
I=7;

%% Paths Length calculations & Flux area

lA= (((G-F)/2)+F)+(((B-D)/2)/2);
lB= (((B-D)/2)/2)+ (H/2);
lC= H/2;
lG=g;
lD= (((G-F)/2)+F);

Aa=D*coreDepth;
Ab=D*coreDepth;
Ac=A*coreDepth;
Ad=A*coreDepth;
Ag=A*coreDepth;


%% Reluctances calculations

RA=((10^3)*lA)/(MuO*MurAlley*Aa);
RB=((10^3)*lB)/(MuO*MurAlley*Ab);
RC=((10^3)*lC)/(MuO*MurAlley*Ac);
RG=((10^3)*lG)/(MuO*MurAir*Ag);
RD=((10^3)*lD)/(MuO*MurAlley*Ad);

%% Inductance calculation

R1T=(RA+RB+RG)/2;
R2T=RD+RC+RG;
RT=R1T+R2T;
LT=(N^2)/RT
```

```
PHi1=(N*I)/(RA+RB+RG);
PHi2=PHi1;
PHi3 = PHi1+PHi2;
Bi1=(10^6)*PHi1/Aa
Bi2=Bi1
Bi3=(10^6)*PHi3/Ad
```

Appendix C

LabVIEW FPGA Code and LabVIEW RT Code

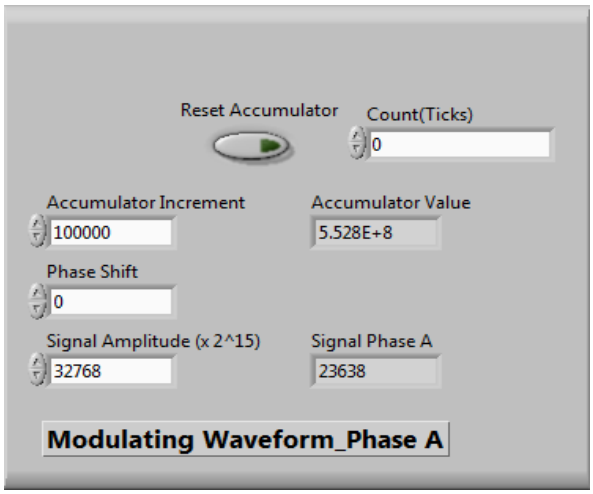
C.1. Introduction

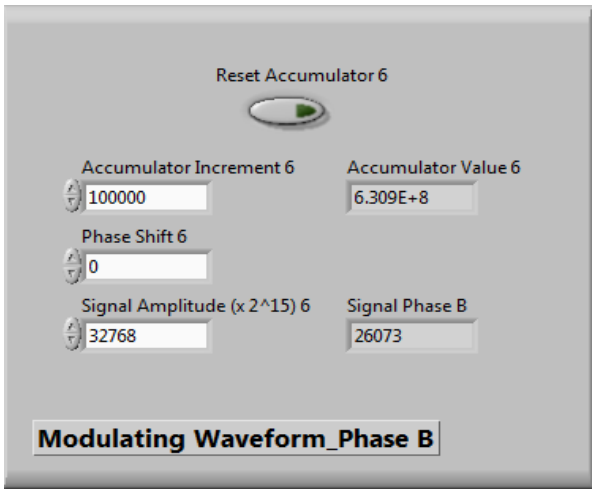
This appendix presents the LabVIEW FPGA codes for the FPGA implementation of the direct digital synthesis modulation technique based on the PS-PWM method for the proposed converter topology. The LabVIEW FPGA codes for the PLL, voltage and current control of the proposed converter topology is shown. Finally the LabVIEW RT code is shown.

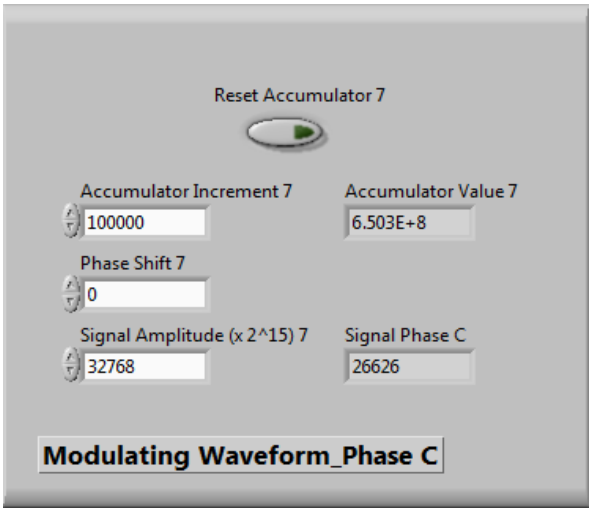
C.2. Direct Digital Synthesis Modulation

The following parts of the LabVIEW FPGA code of a direct synthesis modulation technique for the proposed converter topology is highlighted:

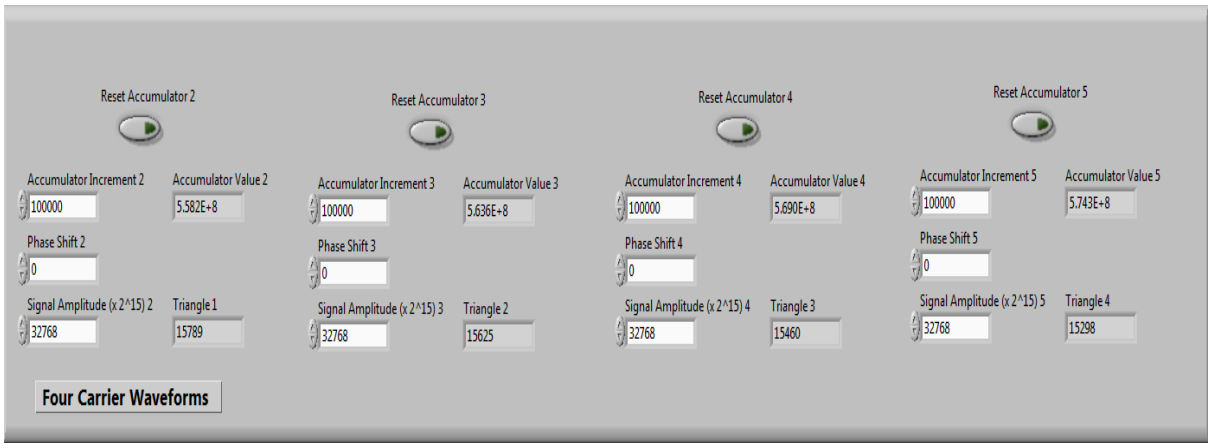
- Front panel of the three-phase direct digital synthesis modulation
- Back end of the three-phase direct digital synthesis modulation





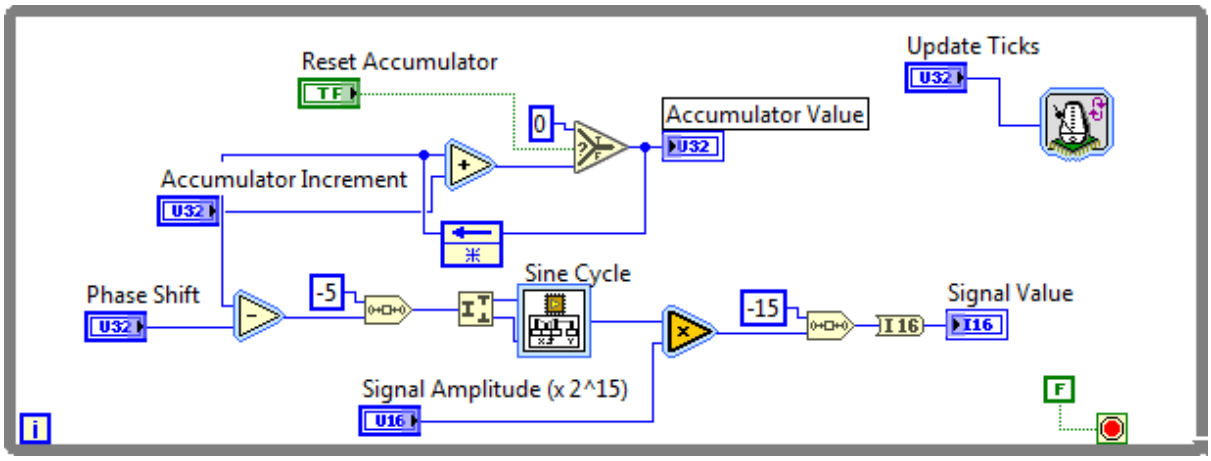


(a)

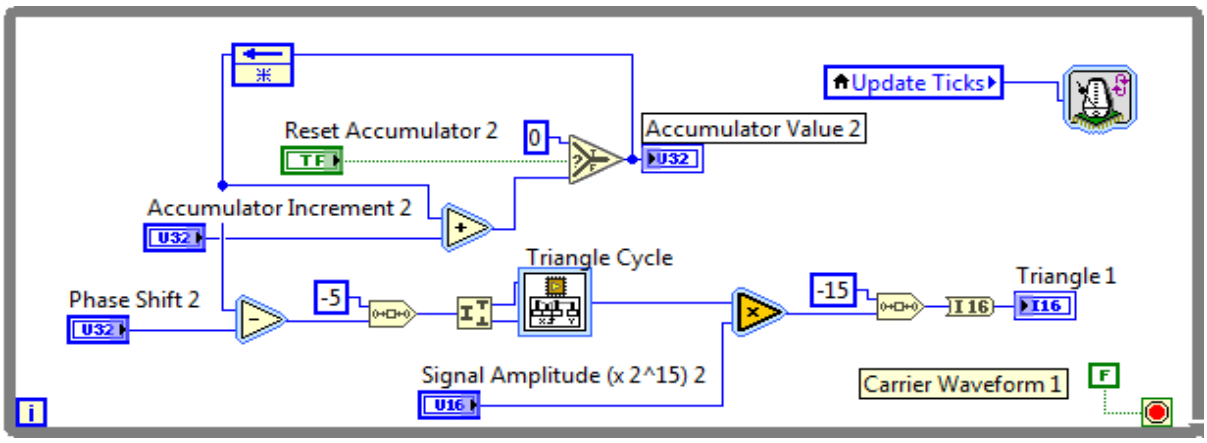


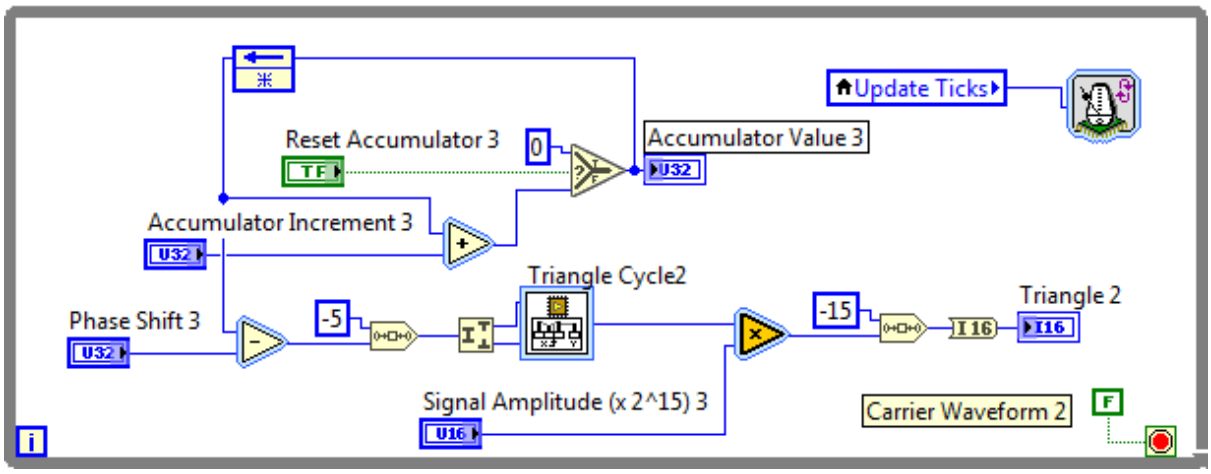
(b)

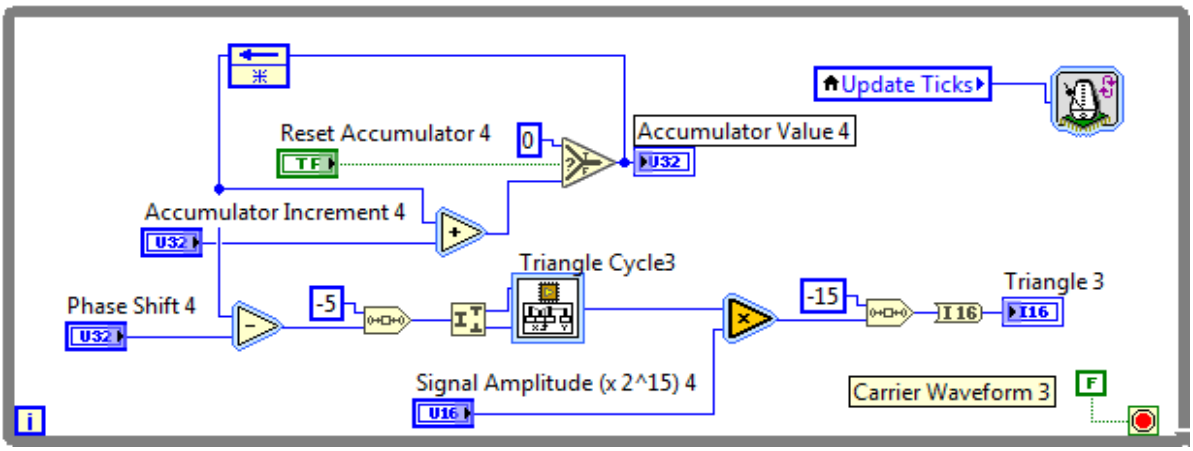
Figure C.1: Front panel of the modulation technique. (a) three-phase modulating waveforms, (b) carrier waveforms.

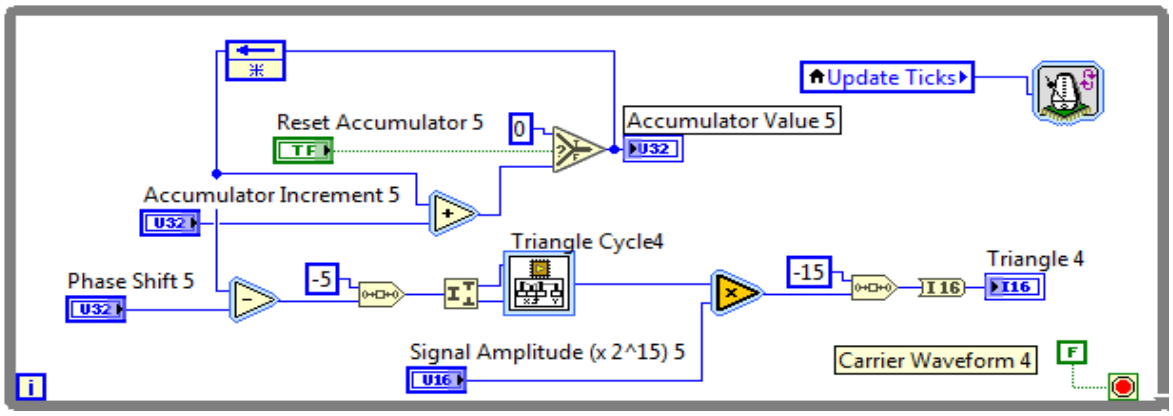


(a)

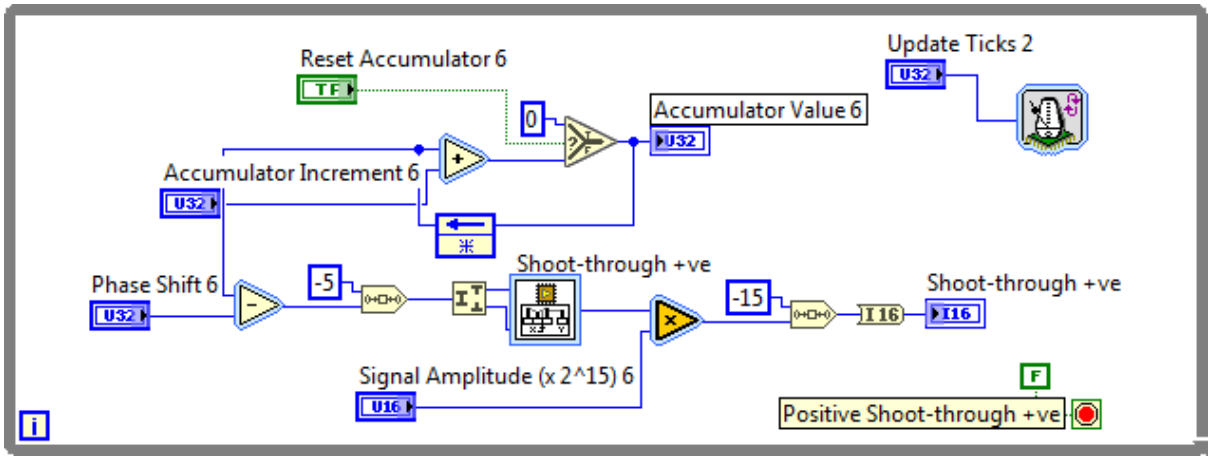

Update Ticks
Reset Accumulator 2
TF
0
Accumulator Value 2
U32
Accumulator Increment 2
U32
Triangle Cycle
Phase Shift 2
U32
-5
-15
I16
Triangle 1
Signal Amplitude (x 2^15) 2
U16
Carrier Waveform 1
F
i


Update Ticks
Reset Accumulator 3
TF
0
Accumulator Value 3
U32
Accumulator Increment 3
U32
Triangle Cycle2
Phase Shift 3
U32
-5
-15
I16
Triangle 2
Signal Amplitude (x 2^15) 3
U16
Carrier Waveform 2
F
i

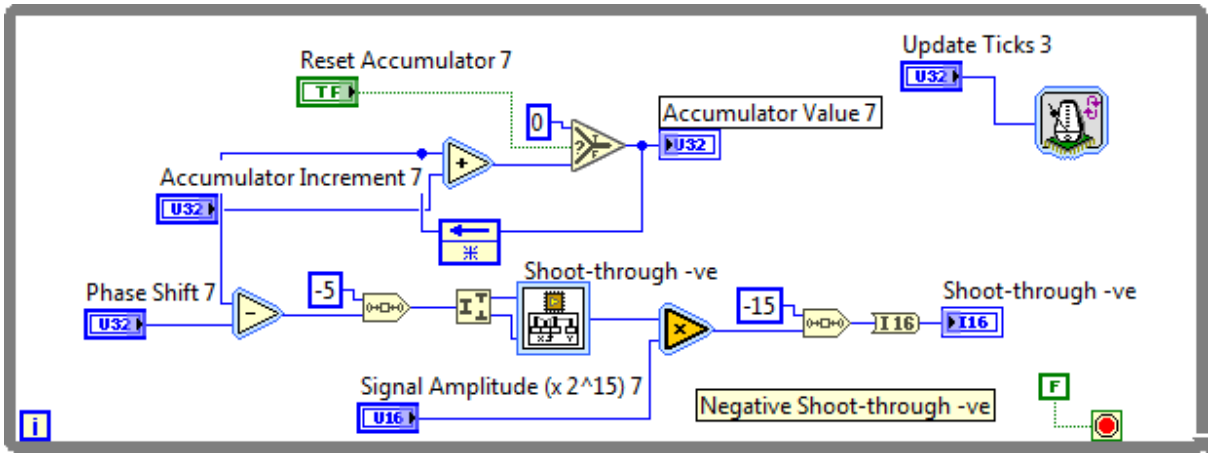

Update Ticks
Reset Accumulator 4
TF
0
Accumulator Value 4
U32
Accumulator Increment 4
U32
Triangle Cycle3
Phase Shift 4
U32
-5
-15
I16
Triangle 3
Signal Amplitude (x 2^15) 4
U16
Carrier Waveform 3
F
i


Update Ticks
Reset Accumulator 5
TF
0
Accumulator Value 5
U32
Accumulator Increment 5
U32
Triangle Cycle4
Phase Shift 5
U32
-5
-15
I16
Triangle 4
Signal Amplitude (x 2^15) 5
U16
Carrier Waveform 4
F
i

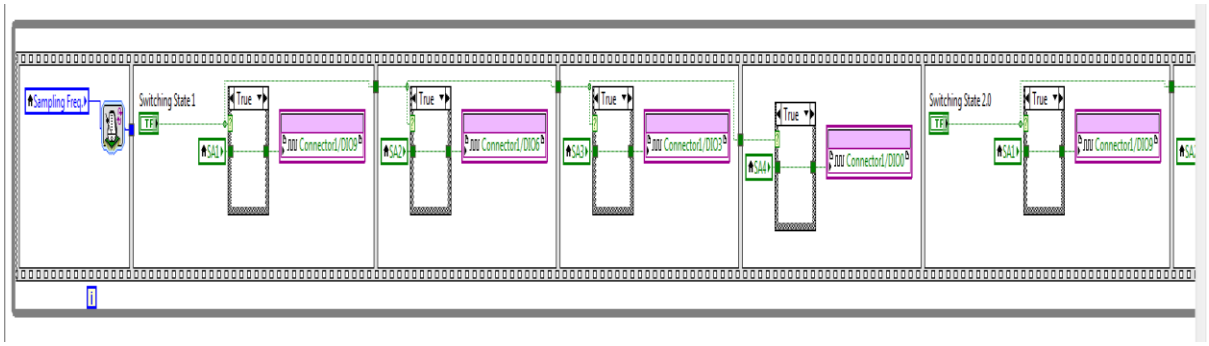
(b)

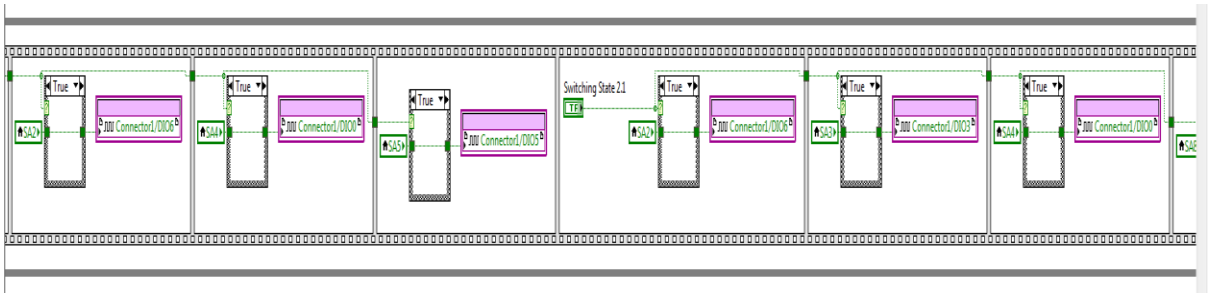

Reset Accumulator 6
TF
0
Update Ticks 2
U32
Accumulator Value 6
U32
Accumulator Increment 6
U32
Shoot-through +ve
Phase Shift 6
U32
-5
-15
I16
Shoot-through +ve
Signal Amplitude (x 2^15) 6
U16
F
Positive Shoot-through +ve
i

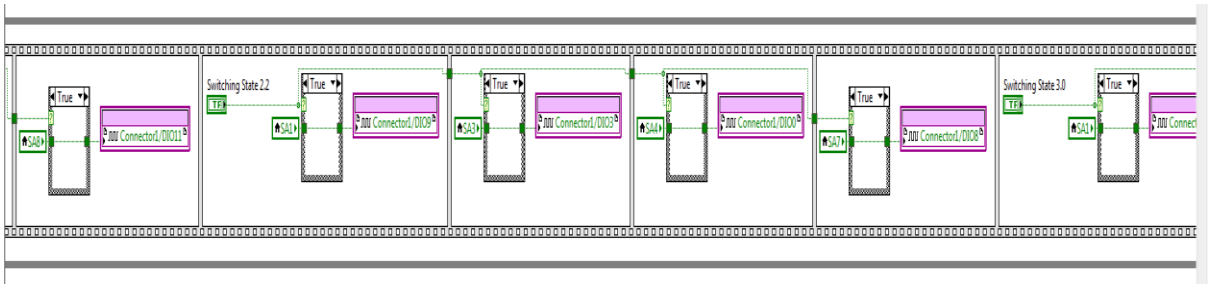
(c)

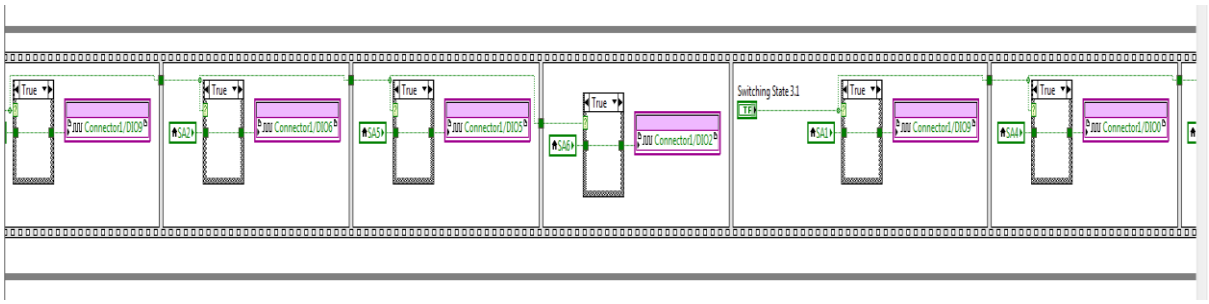

Reset Accumulator 7
TF
0
Update Ticks 3
U32
Accumulator Value 7
U32
Accumulator Increment 7
U32
Shoot-through -ve
Phase Shift 7
U32
-5
-15
I16
Shoot-through -ve
Signal Amplitude (x 2^15) 7
U16
Negative Shoot-through -ve
F
i

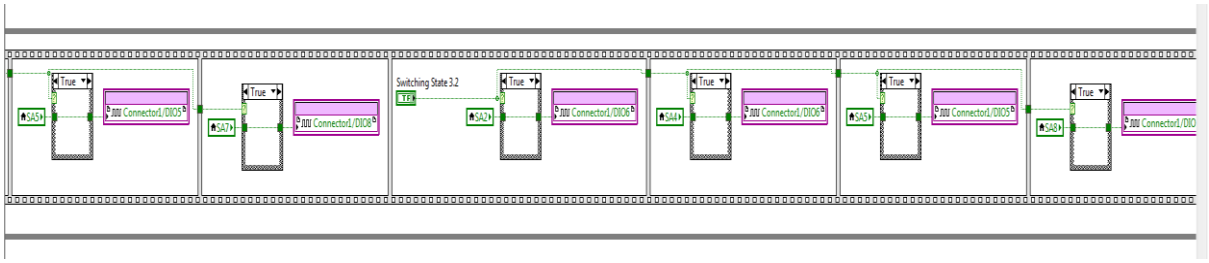
(d)

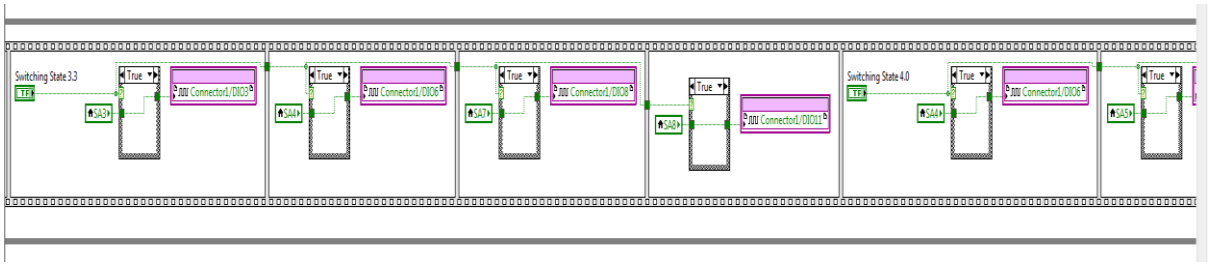

Sampling Freq
Switching State 1
Switching State 2.0
Connector1/DIO9
Connector1/DIO6
Connector1/DIO3
Connector1/DIO0

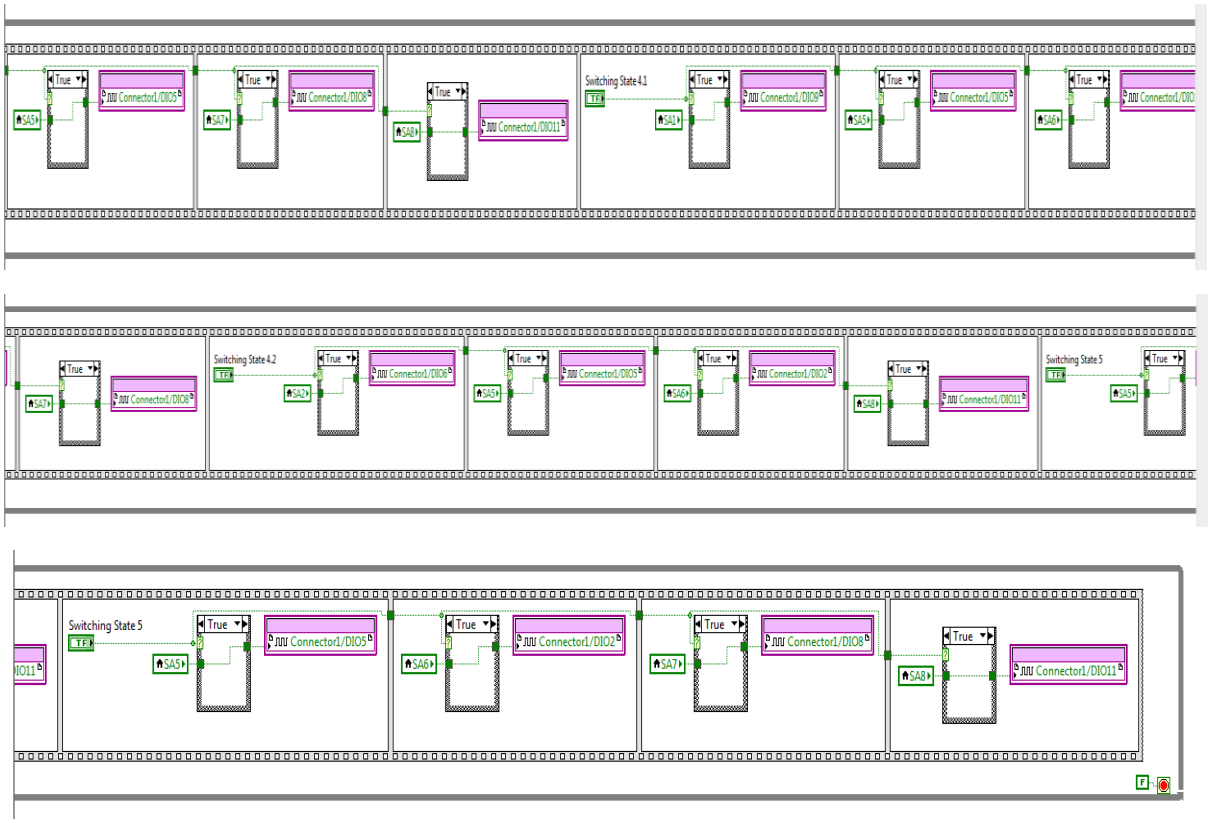

Switching State 2.1
Connector1/DIO6
Connector1/DIO0
Connector1/DIO5
Connector1/DIO3


Switching State 2.2
Switching State 3.0
Connector1/DIO11
Connector1/DIO8
Connector1/DIO3
Connector1/DIO0
Connector1/DIO6


Switching State 3.1
Connector1/DIO9
Connector1/DIO6
Connector1/DIO5
Connector1/DIO3
Connector1/DIO0


Switching State 3.2
Connector1/DIO5
Connector1/DIO8
Connector1/DIO6
Connector1/DIO5


Switching State 3.3
Switching State 4.0
Connector1/DIO3
Connector1/DIO6
Connector1/DIO6
Connector1/DIO11
Connector1/DIO6



(e)

Figure C.2: Back end of the modulation technique. (a) modulating waveform, (b) carrier waveforms 1 to 4, (c) positive shoot-through waveform, (d) negative shoot-through waveform, and (e) switching sequence.

C.3. Phase Locked Loop

The LabVIEW FPGA code of the PLL is shown below:

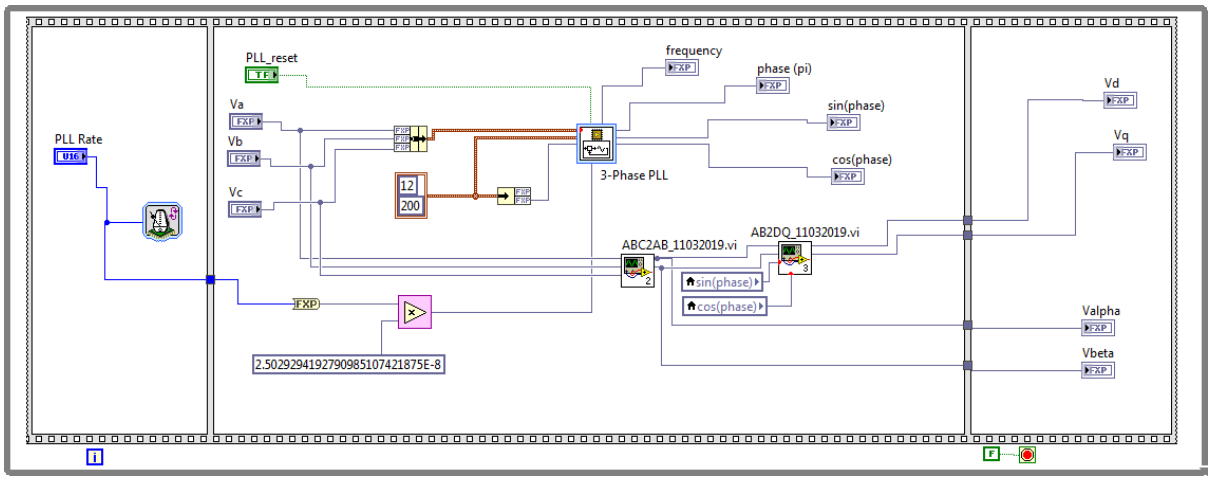
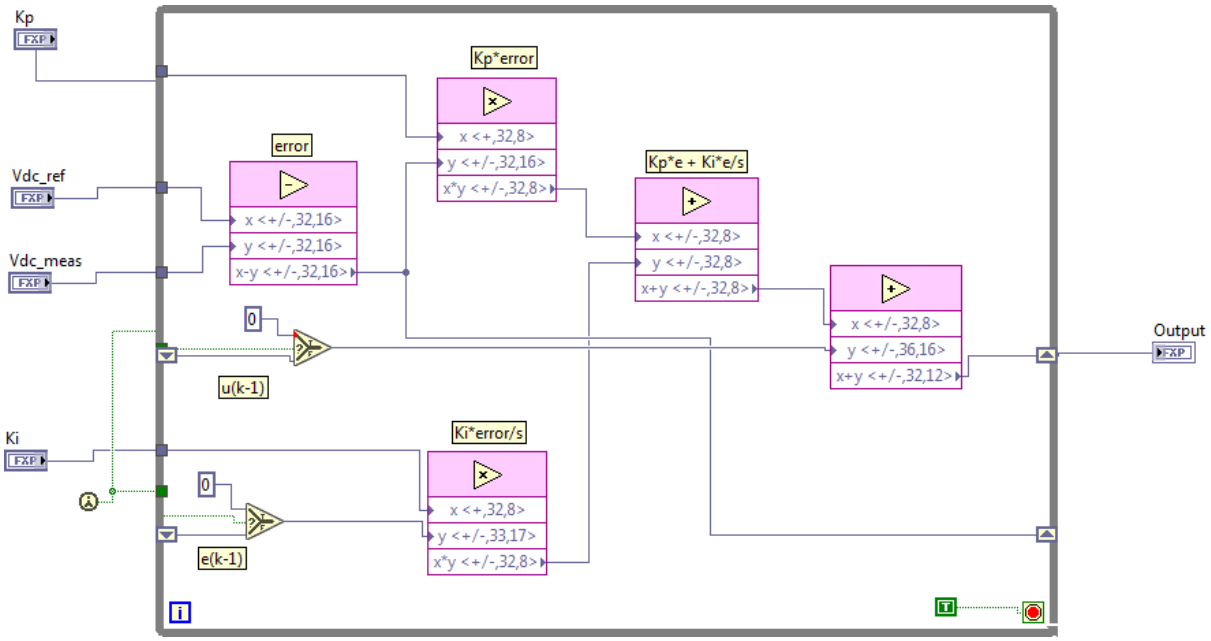


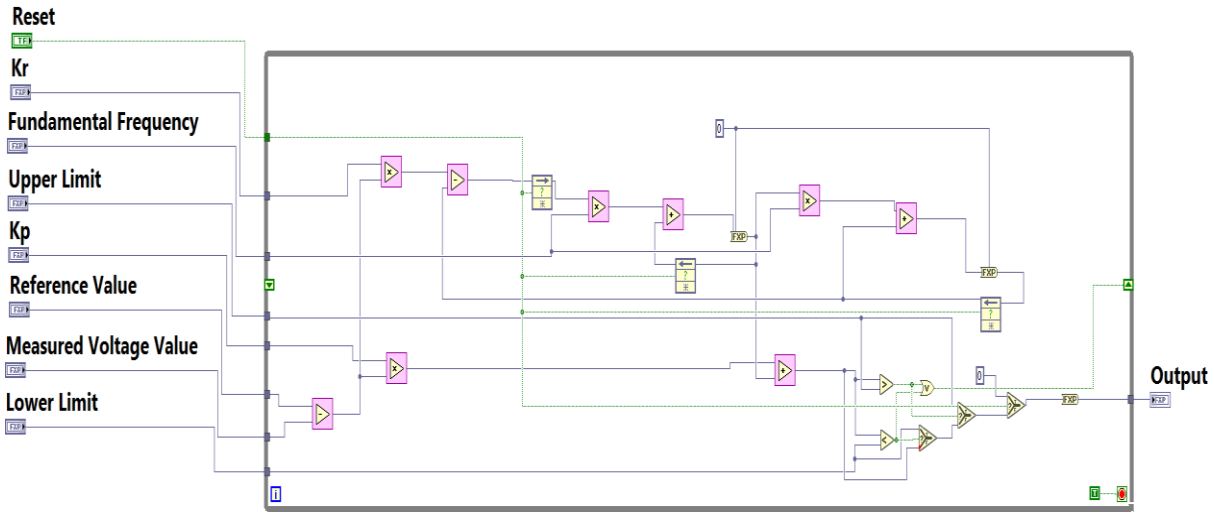
Figure C.3: Grid synchronization code.

C.4. Voltage and Current Control

The LabVIEW FPGA code of the PI and PR controller is shown below:



(a)



(b)

Figure C.4: Voltage and current control code. (a) PI controller, (b) PR controller.

C.5. LabVIEW RT

The LabVIEW RT code that connects the LabVIEW FPGA to the RT environment is shown below:

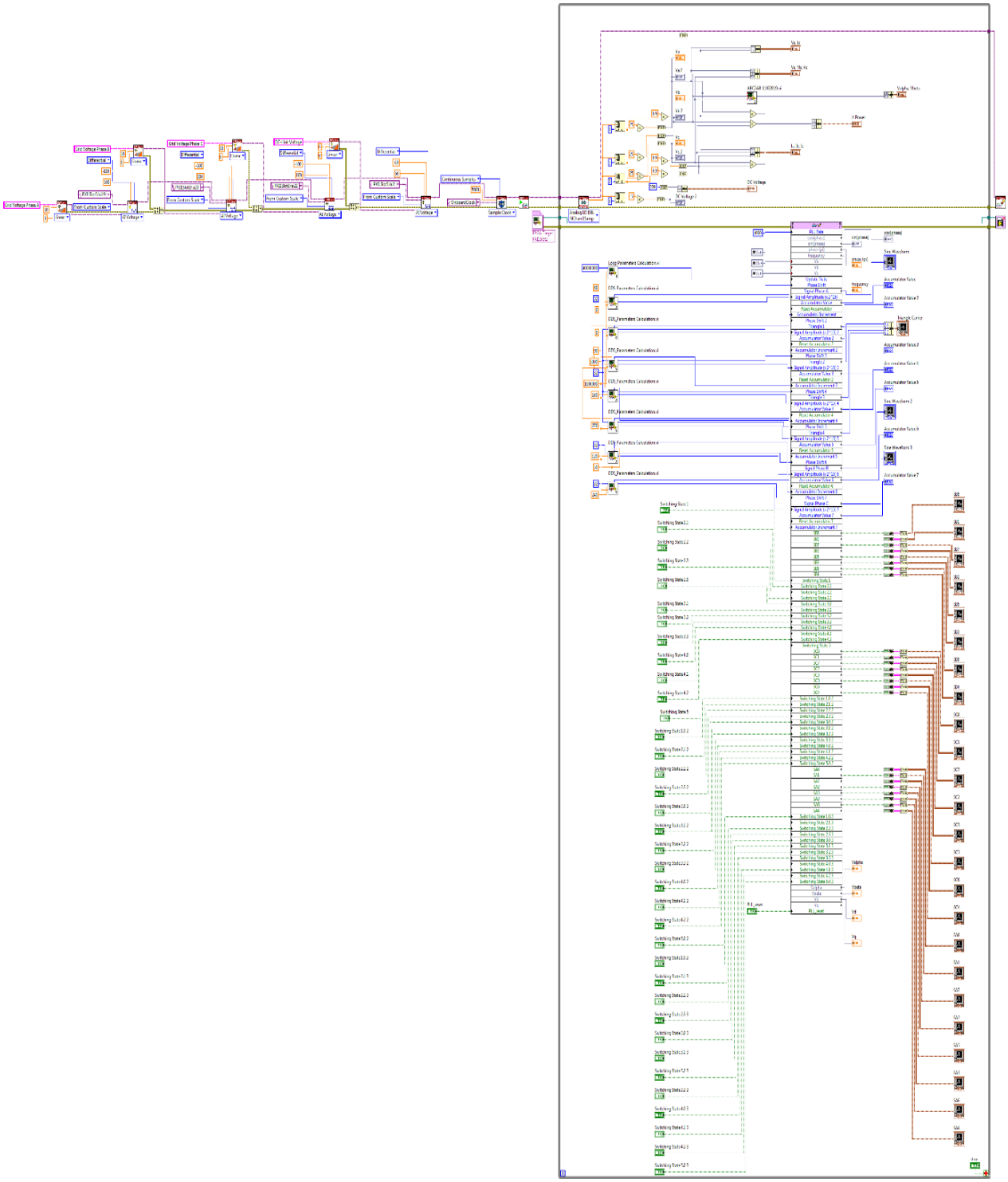


Figure C.5: LabVIEW RT code

Appendix D

Schematic Diagrams, Datasheets and Pin-Out Connections

D.1. Introduction

In this Appendix, the schematic diagrams of the converter circuitry, gate driver circuitry and measurement board circuitry are presented. Also, the datasheets of the switching power semiconductor devices, Semikron SKHI-22AH4R, voltage and current transducers was presented. Furthermore, the pin-out connection of the NI-PXI 7842R and NI-PXIe 6363 modules, highlighting the connector pin assignment and interface pin assignment have been presented.

D.2. Converter Circuitry Schematic

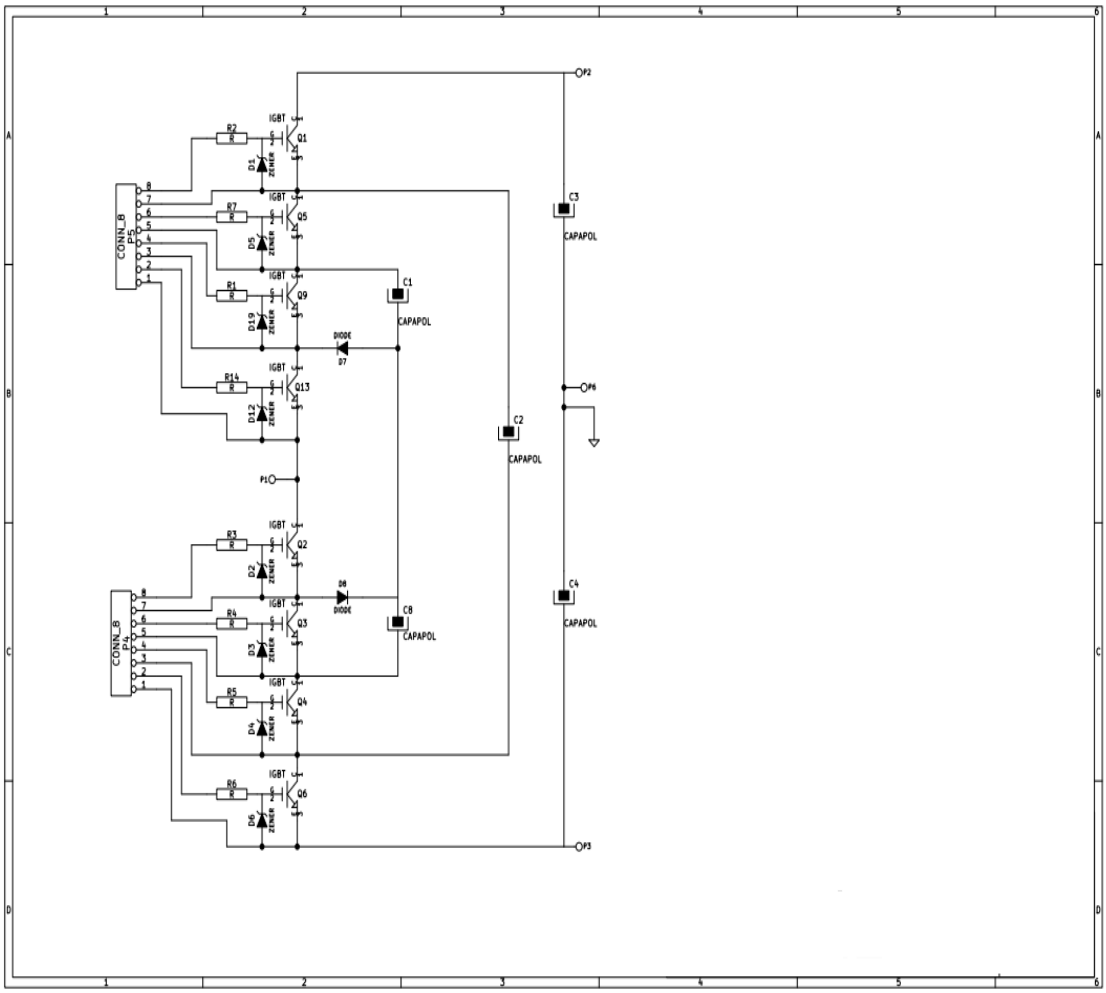


Figure D.1: Schematic diagram of the converter circuitry.

D.3. Datasheet for 47N60C3

Infineon

SPW47N60C3

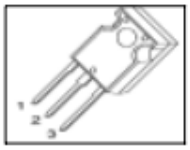
Cool MOS™ Power Transistor

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	0.07	Ω
I_D	47	A

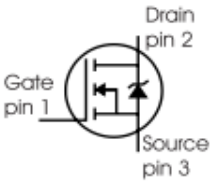
Feature

- New revolutionary high voltage technology
- Worldwide best $R_{DS(on)}$ in TO 247
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- Ultra low effective capacitances
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

PG-TO247



Type	Package	Ordering Code	Marking
SPW47N60C3	PG-TO247	Q67040-S4491	47N60C3



Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 47 30	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\ puls}$	141	
Avalanche energy, single pulse I_D = 10 A, V_{DD} = 50 V	E_{AS}	1800	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[1] I_D = 20 A, V_{DD} = 50 V	E_{AR}	1	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	20	A
Gate source voltage static	V_{GS}	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	
Power dissipation, T_C = 25°C	P_{tot}	415	W
Operating and storage temperature	T_j, T_{stg}	-55... +150	°C
Reverse diode dv/dt [4)]	dv/dt	15	V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope V_{DS} = 480 V, I_D = 47 A, T_j = 125 °C	d*v*/d*t*	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	0.3	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s	T_{sold}	-	-	260	°C

Electrical Characteristics, at T_j=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=20A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=2700µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C, T_j=150°C	 - -	 0.5 -	 25 250	µA
Gate-source leakage current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=30A, T_j=25°C T_j=150°C	 - -	 0.06 0.16	 0.07 -	Ω
Gate input resistance	R_G	*f*=1MHz, open Drain	-	0.62	-	

D.4. Gate Driver Circuitry Schematic

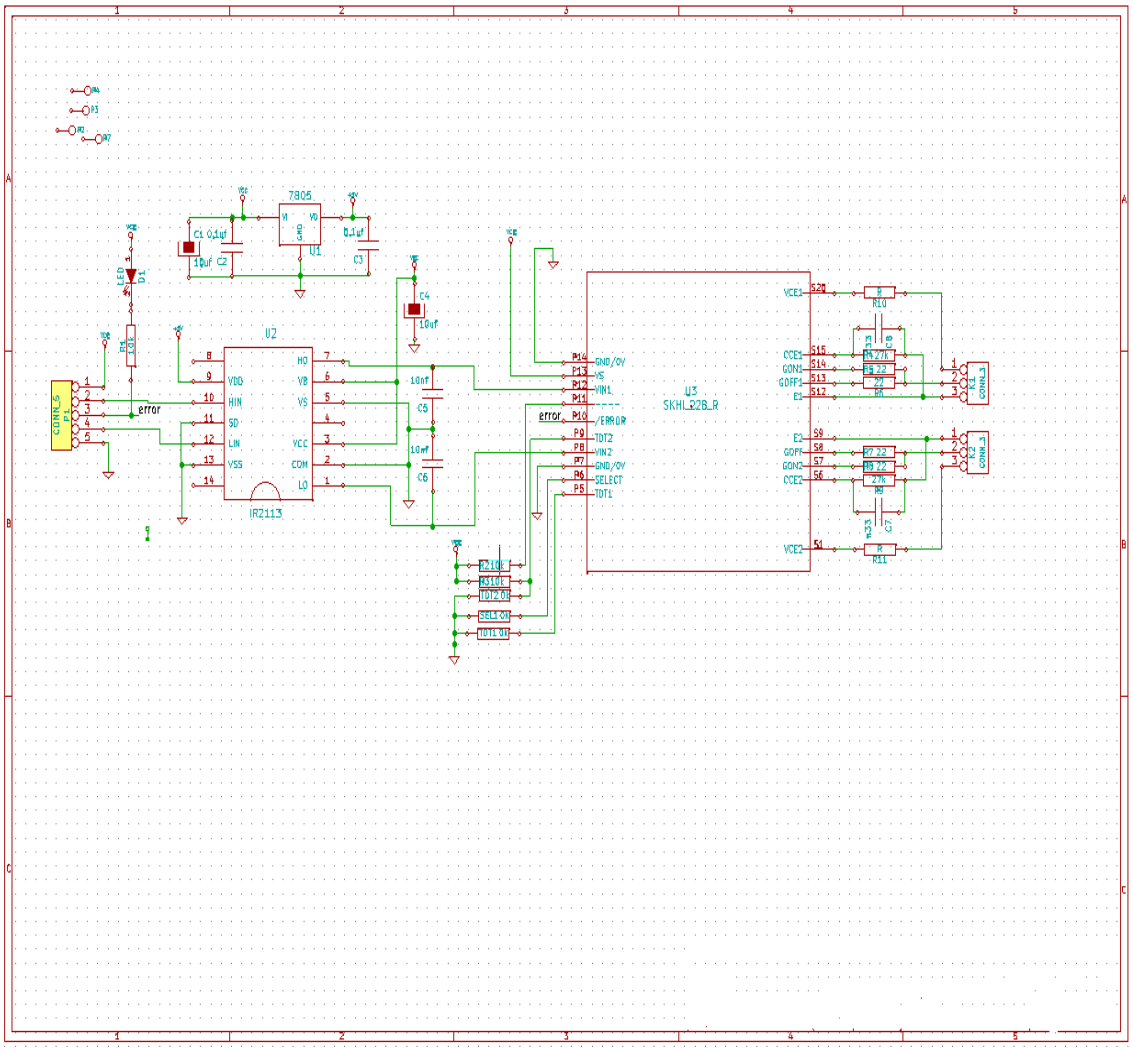


Figure D.2: Schematic diagram of the gate driver circuitry.

D.5. Datasheet for Semikron SKHI-22AH4R

SKHI 22 A / B H4 (R) ...

SEMIDRIVER™

Hybrid Dual IGBT Driver

SKHI 22 A / B H4 (R)

Features

- Double driver for halfbridge IGBT modules
- SKHI 22A H4 is compatible to old SKHI 22 H4
- SKHI 22B H4 has additional functionality
- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and switch off
- Drive interlock top / bottom
- Isolation by transformers
- Supply under voltage protection (13V)
- Error latch / output

Typical Applications

- Driver for IGBT modules in bridge circuits in industrial applications
- DC bus voltage up to 1200 V

1) see fig. 6

2) At R_{CE} = 36 kΩ, C_{CE} = 470 pF, R_{VCE} = 1 kΩ

Absolute Maximum Ratings

Symbol	Conditions	Values	Units
V_S	Supply voltage prim.	18	V
V_{iH}	Input signal volt. (High) SKHI 22A H4	V_S + 0,3	V
	SKHI 22B H4	5 + 0,3	V
$Iout_{PEAK}$	Output peak current	8	A
$Iout_{AVmax}$	Output average current	40	mA
f_{max}	max. switching frequency	50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT	1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	50	kV/µs
V_{isolIO}	Isolation test voltage input - output (2 sec. AC)	4000	Vac
V_{isol12}	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
R_{Gonmin}	Minimum rating for R_{Gon}	3	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	3	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse	4[1)]	µC
T_{op}	Operating temperature	- 40 ... + 85	°C
T_{stg}	Storage temperature	- 40 ... + 85	°C

Characteristics T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary side	14,4	15	15,6	V
I_{SO}	Supply current primary side (no load)		80		mA
	Supply current primary side (max.)			290	mA
V_i	Input signal voltage SKHI 22A H4 on/off		15 / 0		V
	SKHI 22B H4 on/off		5 / 0		V
V_{iT+}	Input threshold volt. (High) SKHI 22A H4			12,5	V
	SKHI 22B H4			3,9	V
V_{iT-}	Input threshold volt. (Low) SKHI 22A H4	4,5			V
	SKHI 22B H4	1,5			V
R_{in}	Input resistance SKHI 22A H4		10		kΩ
	SKHI 22B H4		3,3		kΩ
$V_{G(on)}$	Turn on gate voltage output		+ 15		V
$V_{G(off)}$	Turn off gate voltage output		- 7		V
R_{GE}	Internal gate-emitter resistance		22		kΩ
f_{ASIC}	Asic system switching frequency		8		MHz
$t_{d(on)IO}$	Input-output turn-on propagation time	0,85	1	1,15	µs
$t_{d(off)IO}$	Input-output turn-off propagation time	0,85	1	1,15	µs
$t_{d(err)}$	Error input-output propagation time		0,6		µs
$t_{pERRRESET}$	Error reset time		9		µs
t_{TD}	Top-Bot Interl. Dead Time SKHI 22A H4		4,3		µs
	SKHI 22B H4	no interlock		4,7	µs
V_{CEsat}	Reference voltage for V_{CE}-monitoring		5[2)]	10	V
C_{ps}	Coupling capacitance primary secondary		12		pF
MTBF	Mean Time Between Failure T_a = 40°C		2,0		10^6 h
w	weight		45		g

External Components

Component	Function	Recommended Value
R_{CE}	Reference voltage for V_{CE}-monitoring $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}4$ (1) with R_{VCE} = 1kΩ (1700V IGBT): $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1{,}8$ (1.1)	10kΩ < R_{CE} < 100kΩ 18kΩ for SKM XX 123 (1200V) 36kΩ for SKM XX 173 (1700V)
C_{CE}	Inhibit time for V_{CE} - monitoring $t_{min} = \tau_{CE} \cdot \ln\left[\frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)}\right]$ (2) $\tau_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$ (3)	C_{CE} < 2,7nF 0,33nF for SKM XX 123 (1200V) 0,47nF for SKM XX 173 (1700V) 0,5µs < t_{min} < 10µs
R_{VCE}	Collector series resistance for 1700V IGBT-operation	1kΩ / 0,4W
R_{ERROR}	Pull-up resistance at error output $\frac{U_{Pull-Up}}{R_{ERROR}} < 15mA$	1kΩ < R_{ERROR} < 10kΩ
R_{GON}	Turn-on speed of the IGBT [4]	R_{GON} > 3Ω
R_{GOFF}	Turn-off speed of the IGBT [5]	R_{GOFF} > 3Ω

[4] Higher resistance reduces free-wheeling diode peak recovery current, increases IGBT turn-on time.
[5] Higher resistance reduces turn-off peak voltage, increases turn-off time and turn-off power dissipation

D.6. Measurement Board Circuitry Schematic

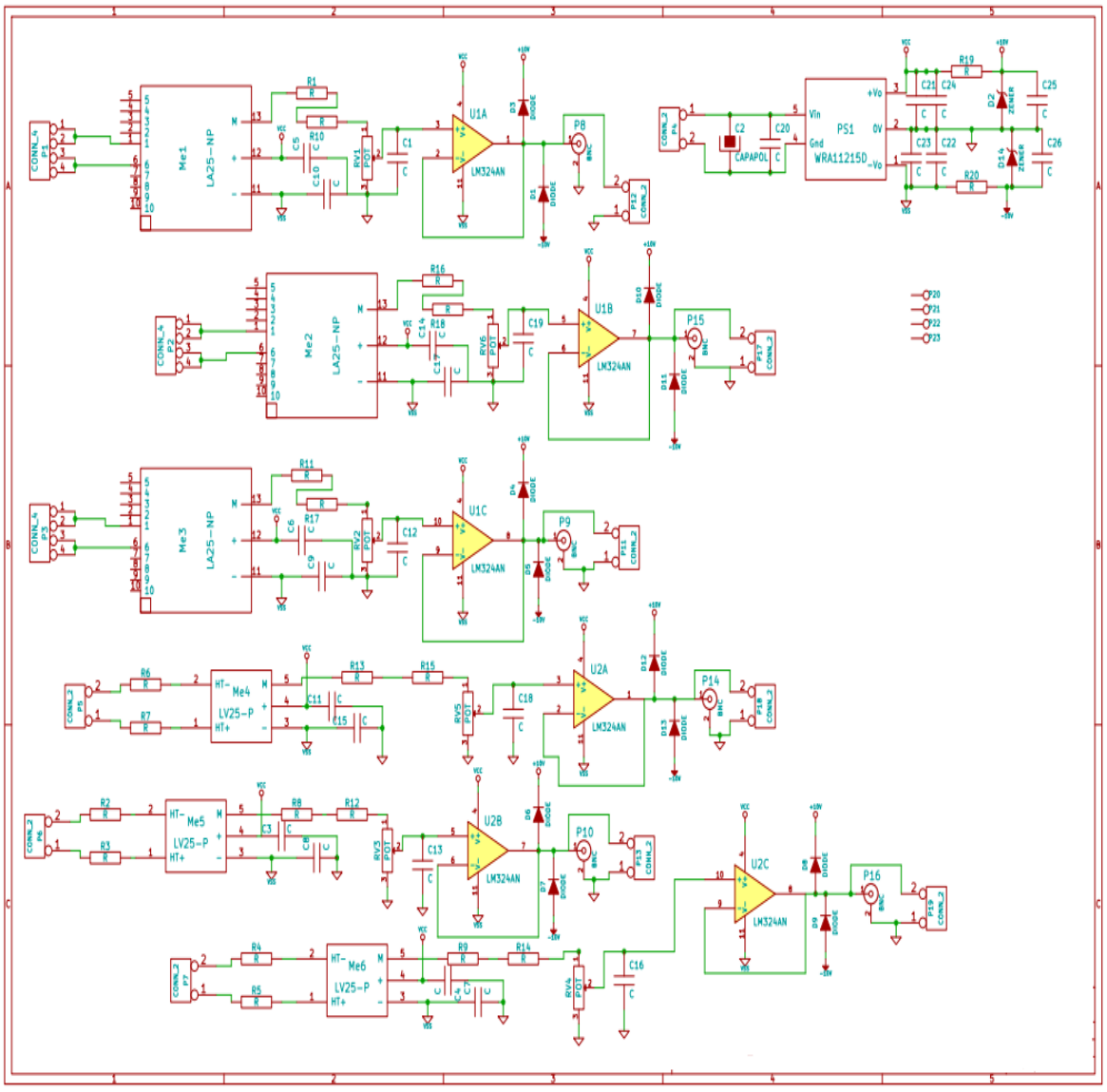


Figure D.3: Schematic Diagram of the measurement board circuitry.

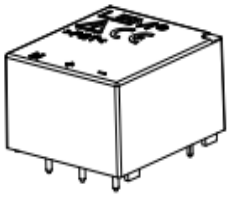
D.7. Datasheet for LV 25-P

Voltage Transducer LV 25-P

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic separation between the primary circuit and the secondary circuit.

I_{PN} = 10 mA

V_{PN} = 10 .. 500 V



Electrical data

I_{PN}	Primary nominal rms current		10		mA
I_{PM}	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA$_{max}$	30	190	Ω
		@ ± 14 mA$_{max}$	30	100	Ω
	with ± 15 V	@ ± 10 mA$_{max}$	100	350	Ω
		@ ± 14 mA$_{max}$	100	190	Ω
I_{SN}	Secondary nominal rms current		25		mA
K_N	Conversion ratio		2500 : 1000		
U_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@ ± 15 V) + I_S		mA

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN}, T_A = 25 °C @ ± 12 .. 15 V		± 0.9		%
	@ ± 15 V (± 5 %)		± 0.8		%
ε_L	Linearity error		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25 °C			± 0.15	mA
I_{OT}	Temperature variation of I_O	0 °C .. + 25 °C	± 0.06	± 0.25	mA
		+ 25 °C .. + 70 °C	± 0.10	± 0.35	mA
t_r	Step response time [1] to 90 % of I_{PN}		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Resistance of primary winding	@ T_A = 70 °C	250	Ω
R_S	Resistance of secondary winding	@ T_A = 70 °C	110	Ω
m	Mass		22	g
	Standards		EN 50178: 1997 UL 508: 2010	

Note: [1] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit).

Features

- Closed loop (compensated) current transducer using the Hall effect
- Insulating plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

Application domain

D.8. Datasheet for LA 25-NP

Current Transducer LA 25-NP

I_{PN} = 5-6-8-12-25 At

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic isolation between the primary circuit and the secondary circuit.

16080

Electrical data

I_{PN}	Primary nominal current rms			25			At
I_{PM}	Primary current, measuring range			0 .. ± 36			At
R_M	Measuring resistance @		T_A = 70°C		T_A = 85°C		
			$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$	
	with ± 15 V	@ ± 25 At $_{max}$	100	320	100	315	Ω
		@ ± 36 At $_{max}$	100	190	100	185	Ω
I_{SN}	Secondary nominal current rms			25			mA
K_N	Conversion ratio			1-2-3-4-5 : 1000			
V_C	Supply voltage (± 5 %)			± 15			V
I_C	Current consumption			10 + I_S			mA

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C		± 0.5		%
ε_L	Linearity error		< 0.2		%
			Typ	Max	
I_O	Offset current [1] @ I_P = 0, T_A = 25°C		± 0.05	± 0.15	mA
I_{OM}	Magnetic offset current [2] @ I_P = 0 and specified R_M, after an overload of 3 x I_{PN}		± 0.05	± 0.15	mA
I_{OT}	Temperature variation of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
		- 25°C .. + 85°C		± 0.5	mA
		- 40°C .. + 85°C		± 1.2	mA
t_r	Response time [3] to 90 % of I_{PN} step		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
BW	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature		- 40 .. + 85	°C
T_S	Ambient storage temperature		- 45 .. + 90	°C
R_P	Primary coil resistance per turn	@ T_A = 25°C	< 1.25	mΩ
R_S	Secondary coil resistance	@ T_A = 70°C	110	Ω
		@ T_A = 85°C	115	Ω
R_{IS}	Isolation resistance @ 500 V, T_A = 25°C		> 1500	MΩ
m	Mass		22	g
	Standards		EN 50178: 1997	

Features

- Closed loop (compensated) current transducer using the Hall effect
- Isolated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

D.9. NI-PXI 7842R Pin-Out

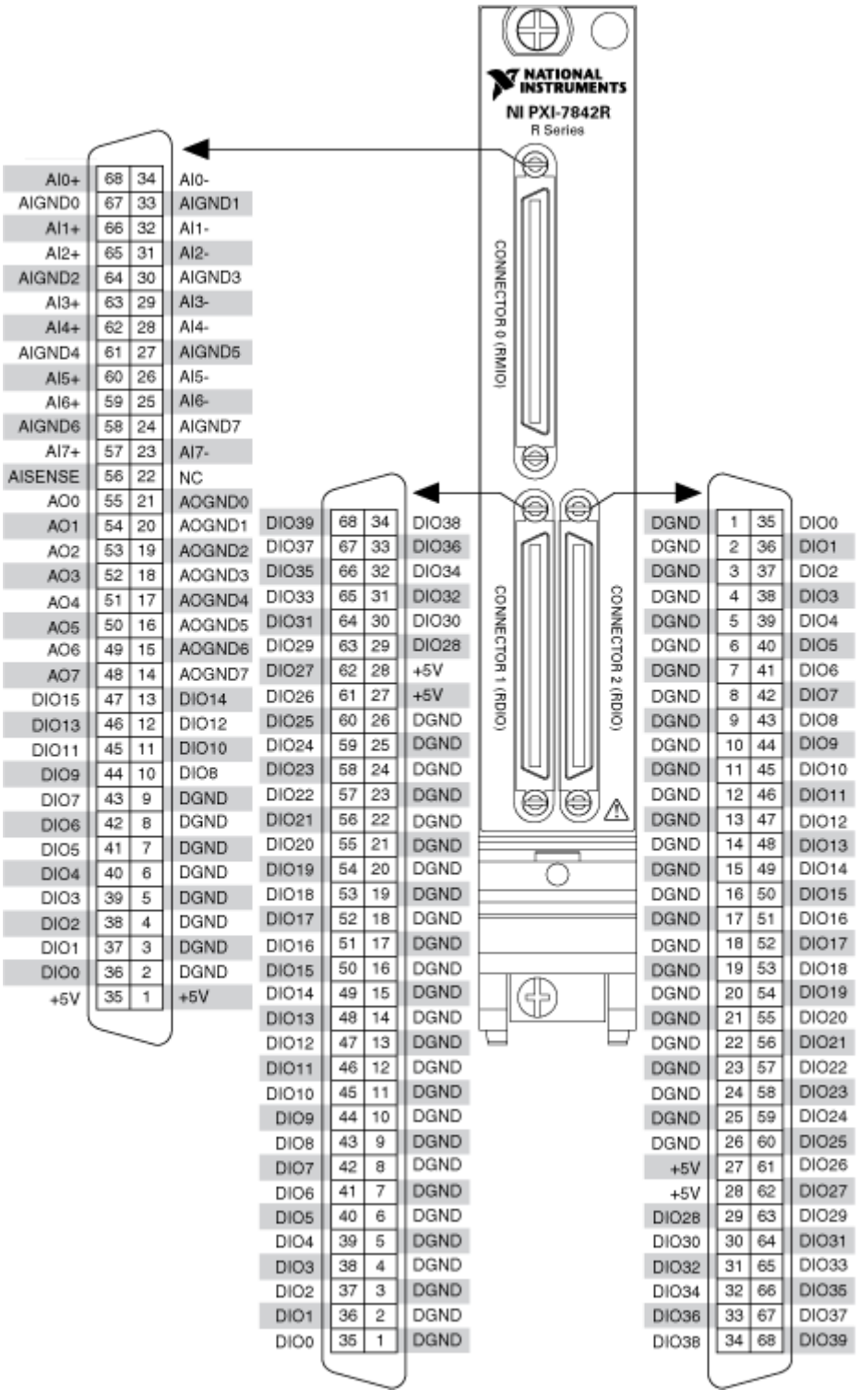


Figure D.4: NI-PXI 7842R connector pin assignment and location.

D.10. NI-PXI 7842R Pin-Out Labels for SCB-68A Interface

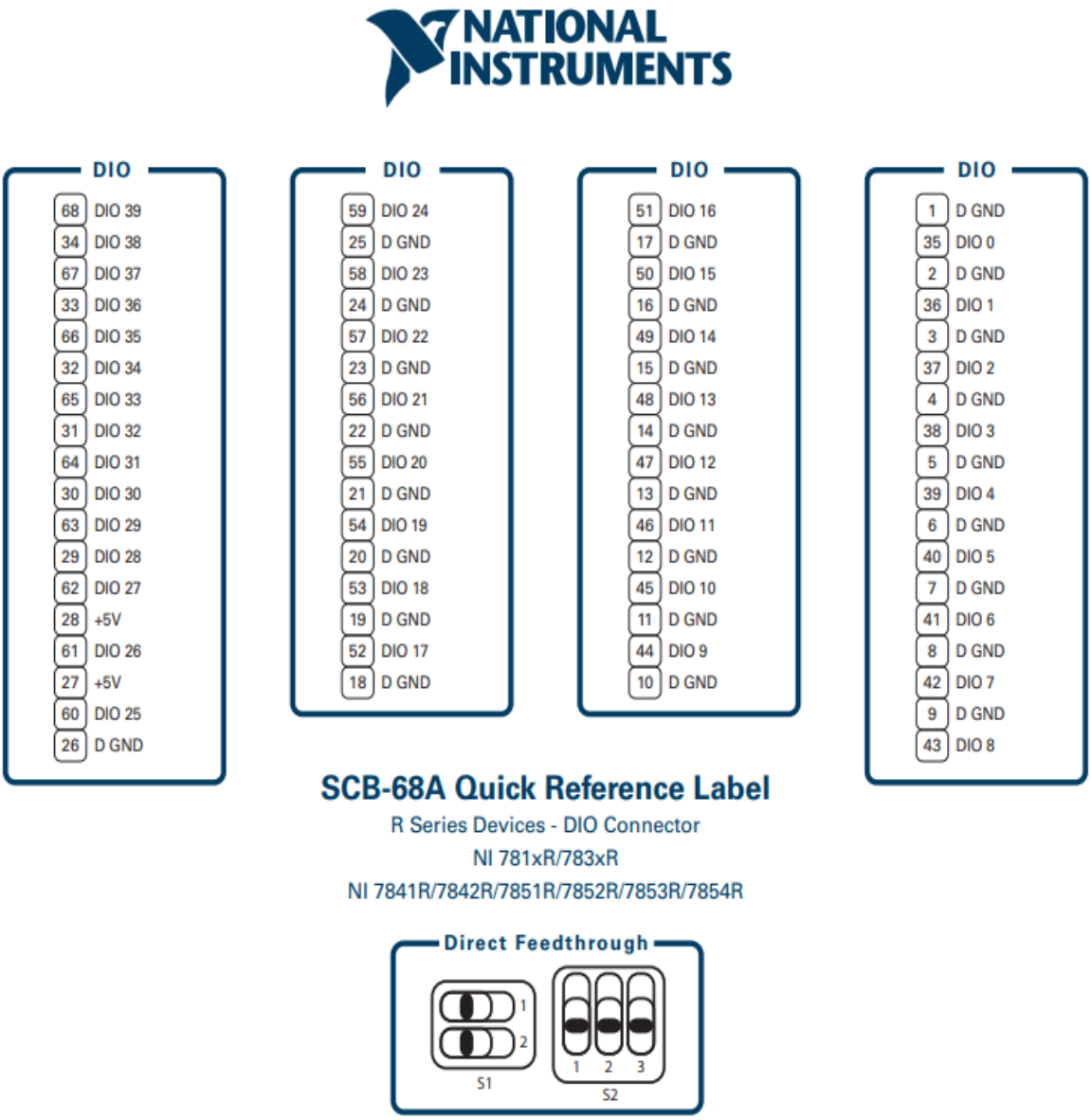


Figure D.5: NI-PXI 7842R connector pin to SCB-68A interface.

D.11. NI-PXIe 6363 Pin-Out

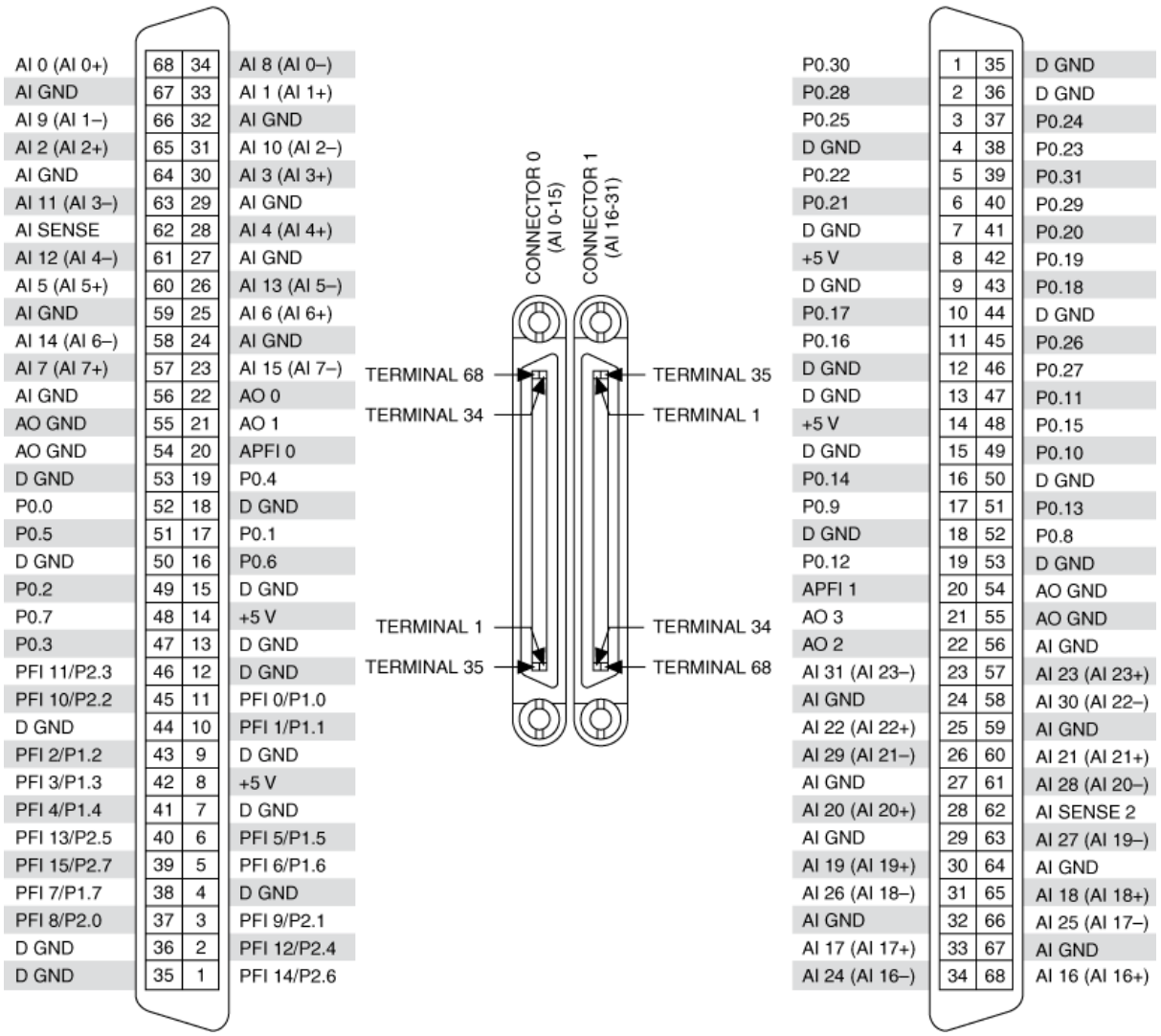


Figure D.6: NI-PXIe 6363 Connector Pin Assignment and Location.

D.12. NI-PXIe 6363 Pin-Out Labels for SCB-68A Interface

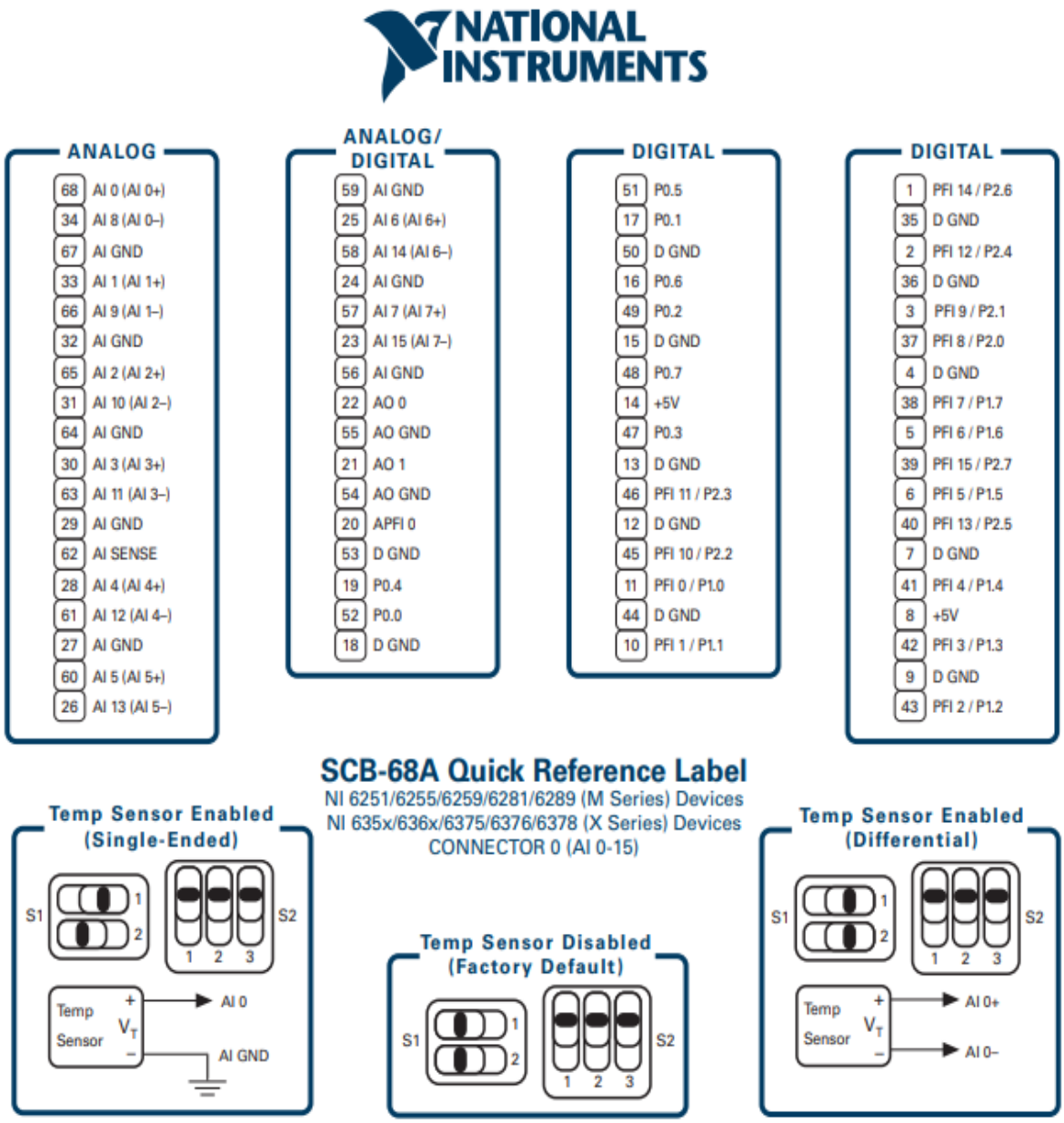


Figure D.7: NI-PXIe 6363 Connector Pin to SCB-68A Interface.