INTERFACE CONVERSION BETWEEN CCITT RECOMMENDATIONS X.21 AND V.24

by

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ABSTRACT

The subject of this thesis concerns conversion between the interfaces specified by CCITT recommendations X.21 and V.24.

The evolution of public data networks against the background of data communications using the telephone network is outlined. The DTE/DCE interface is identified as being of particular importance and is explained in terms of the ISO model for Open Systems interconnection (OSI).

CCITT recommendation X.21 is described in detail using the OSI layered approach. Finite state machine (FSM) terminology is defined and the concept of an interface machine introduced.

CCITT recommendation V.24 is described in terms of the physical layer of the OSI model. Only those aspects of V.24 relevant to the subject of this thesis are examined.

Interface conversion between X.21 and V.24 is discussed in detail and the design of devices to perform the conversion described. A microprocessor-based translator to perform interface conversion between a V.24 DTE and a X.21 DCE for switched circuit use is designed, using the FSM approach. A preliminary model of such a translator, implemented on a development system, is described. Its hardware and software are outlined and areas for further work identified.

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TABLE OF CONTENTS

LIST OF TABLES

1. INTRODUCTION

1.1 BACKGROUND

Data transmission between data processing devices requires some form of communications network, unless distances between devices are trivial. Traditionally, the public telephone network (PTN) has been used to this end and users have had the choice of a dial-up service, or the use of dedicated lines.

The telephone network, being designed specifically to enable voice communication and not to meet the more stringent requirements of data transmission, suffers from various inherent drawbacks. Some of these are: circuit interruptions, impulse noise, bandwidth limitations, frequency shifts, amplitude distortion, envelope delay distortion and white noise of which the first three tend to cause problems most frequently. These shortcomings have resulted in most network administrations opting for the introduction of public data networks (PDNs). PDNs may be divided into three categories : dedicated lines only, circuit switched, or packet switched. Networks providing dedicated lines only are limited in flexibility and find their main application with heavy data traffic between users. Circuit switched networks are most efficient when long bursts of data traffic are common, while packet switched networks come into their own when traffic is sporadic and of low volume.

As the data terminal equipment (DTE) connected to networks and the networks themselves belong to two different parties, and the network is intended for multi-user applications, the method of connection requires careful definition and specification, and has resulted in the birth of a host of interface specifications and communication protocols.

This thesis deals with translation between two different interface specifications. The interfaces in question are defined by CCITT recommendations V.24 and X.21. A conversion unit is required to allow equipment designed for use with either interface to be used with the other.

CCITT recommendation V.24 has its roots in the beginnings of data transmission over the telephone network and has become the most commonly used interface for data transmission internationally. The X.21 interface is a more recent development associated with the emergence of public data networks such as those of the Nordic countries and Japan. It is intended for use on synchronous, circuit switched public data networks and offers numerous advantages over other interfaces previously used for the same application. The most significant of these is that it allows fast, efficient circuit switching through the same interface used for data transmission. (For the same application, V.24 requires the use of a separate interface for call control). X.21 is well suited for call establishment under DTE control, with or without human intervention. Further than this it allows the user access to various network facilities such as call progress signals, calling/called line identification, charge information and the establishment of closed user groups.

When introducing a new interface such as X.21, which has network layer features, the administration concerned is faced with an immediate problem in that the majority of its users will not be able to subscribe to the new service, because their equipment only implements the V.24 physical layer interface. (The concept of different layers, such as network and physical, is explained in section 2.2). With this difficulty in mind, the CCITT has published a recommendation (X.21 bis) intended as an interim measure during the period of transition to X.21. Recommendation X.21 bis encourages the use of DCE (data circuit-terminating equipment) presenting the user with a physical layer V.24 interface, implemented so as to allow him some of the advantages of a public data network which he did not enjoy on the telephone network. The user may be allowed to bypass the V.24 interface by, for example, having a keypad and display on the DCE to realise some of the network layer features characteristic of X.21. Typical of this situation is the newly-developed Nordic Data Network. This network is full duplex circuit switched and supports the X.21 DTE/DCE interface. The Swedish manufacturers Standard Radio and Telefon AB, produce a range of DCE for this network (1) which is divided into three classes. Class X supports pure X.21, while classes VP and VPC implement V.24 synchronous and asynchronous interfaces respectively. The VP and VPC equipment incorporates a keypad and display which allow direct user-network interaction. The VP equipment has been designed to conform to CCITT recommendation X.21 bis.

Manufacturers of data terminal equipment on the other hand tend to look for ways of upgrading their products so as to take best advantage of the power offered by the new interface. Typical of this tendency is the IBM reaction to the introduction of X.21 in Japan. X.21 has been found to be compatible with the lower layer of IBM's Systems Network Architecture (2). IBM have taken the approach of upgrading their product line for Japan to gain X.21 compatibility, allowing their equipment full interaction with the data network.

1.2 LITERATURE SURVEY

In preference to isolating specific source documents at this stage, the literature used as source material for this thesis is grouped into two general categories. The first is that of the international standards produced by organisations such as the CCITT and ISO. A sound comprehension of the CCITT recommendations on the V.24 and X.21 DTE/DCE interfaces forms a fundamental requirement for the work undertaken here. The ISO model for "Open Systems Interconnection" (OSI), which has a strong bearing on current work done in the areas of distributed computing and digital communications, was also studied in some depth.

The second category consists of literature produced as a result of the first. Much of it is tutorial by nature, the authors being closely associated with development of the standards in question. Their contributions aid in grasping the concepts behind the standards. Examples are H.C. Folts who was instrumental in the development of X.21, and H. Zimmerman who chaired the ISO committee on Open Systems Interconnection. Many of the other authors represent PTTs and manufacturers who are concerned with the implementation of the standards of interest. Their contribution is valuable when forming an opinion as to the capabilities and limitations of the proposed standards.

1.3 OBJECTIVE

The aim of this thesis is to design and construct a unit to do conversion between the X.21 and V.24 interfaces. This unit should be able to operate in the following two modes:

a) X.21 interfacing to a DCE and V.24 interfacing to a DTE, and

b) X.21 interfacing to a DTE and V.24 interfacing to a DCE.

The unit should allow data transmission at the speeds of 1200 bits/sec, 2400 bits/sec, 4800 bits/sec and 9600 bits/sec, and should give an indication of the current state of the interfaces.

2. COMMUNICATION ACROSS THE DTE/DCE INTERFACE

2.1 BACKGROUND

The DTE/DCE interface is traditionally defined as existing at the line of demarcation of responsibility between the users of data terminal equipment (typically data processing systems composed of anything from simple terminals to host computers) and the administration providing the data circuit terminating equipment (such as modems and associated equipment). This line of demarcation of responsibility is referred to as the interface point or interchange point, and its physical position is usually associated with the connector joining the cable between DTE and DCE.

Communication across the interchange point is in binary digits and data may be transferred either in serial or parallel form, although serial transmission is the norm. Information transmission across the interchange point is on interchange circuits which carry up to three kinds of information : data, control and timing. The timing and control circuits are required to transmit the information on the data circuits across the interface. Where timing information is not transmitted, communication is known as asynchronous. Synchronous communication (used for higher volume traffic) requires the transfer of timing information across the interface.

The behaviour and significance of the signals transmitted on the interchange circuits is governed by a set of rules known as a communications protocol. Various protocols exist and their use depends on several factors, such as the equipment manufacturer, the application, the rate of data transfer required and the type of network being used. Until recently, the popular medium for data transmission was the public telephone network, and emerging protocols were designed with this in mind. Serial data is transmitted over the PTN in three ways:

i) duplex (full duplex) or two-way simultaneous transmission;

ii) half duplex or two-way alternate transmission; and

iii) simplex or one-way only transmission

(With an international increase in the volume of data transmitted, several PDNs have emerged and with them, protocols designed specifically for PDNs. The tendency has been for these networks to be full duplex, which is reflected in the DTE/DCE interface).

Data transmission over the telephone network may employ three methods of call establishment:

i) manual dialling, where an operator will dial the telephone number of his destination address (eg. a host computer) and switch his terminal equipment to line once the call is established;

ii) automatic dialling and answering, where the dialling function is performed using a separate DCE interface such as V.25 (not supported in this country) to that used by the DCE; and

iii) the use of dedicated lines

When dedicated lines are used, the general trend is for a private network to develop using the dedicated lines as trunks. With such a network, the routing and switching of calls becomes a function which is performed by terminal equipment. This results in the user carrying an overhead which is the responsibility of network administrations when dial-up facilities are used. CCITT recommendation

V.24 has evolved with data transmission over the telephone network and therefore satisfies related criteria. It does not attempt to cater for switching or routing functions, assuming the presence of dial-up facilities or leased lines.

Public data networks have emerged to fulfil switching and routing functions, taking this overhead away from the user and again making it the responsibility of the network administration. Apart from this, the administration may decide to give its network value added features which are not available on the telephone network. CCITT recommendation X.21 makes allowance for the implementation of the following value added network features:

i) facility registration or cancellation;
ii) direct calling, or "hotline" facilities;
iii) abbreviated addressing;
iv) multiple address calling;
v) called line identification;
vi) calling line identification;
vii) closed user groups;
viii) redirection of calls; and
ix) the provision of charge advice

2.2 STANDARDISATION

International standardisation did not play a strong role in the design of early communications protocols, resulting in a large number of protocols with many variations and inconsistancies. Some manufacturers' protocols emerged as de facto standards, examples being IBM's SDLC (synchronous data link control) and BSC (binary synchronous communication) protocols. With the advent of PDNs, the tendency has been for protocols to be developed by or under the auspices of international standardisation bodies such as the CCITT[1] and ISO[2].

1) International Telegraph and Telephone Consultative Committee

2) International Organisation for Standardisation

Adopting such standards results in manufacturers designing equipment according to a widely recognised specification with great compatibility advantages over older protocols.

The CCITT is an organisation composed of representatives of the PTT administrations of the various member countries. It forms a part of the International Telecommunications Union of the UNESCO. The CCITT publishes relevant standards in the form of recommendations which are the work of a number of study groups. Two of these groups are of particular interest to the subject of this thesis : study group XVII, which publishes the V-series recommendations for data transmission over the telephone network, and study group VII which publishes the X-series recommendations for data transmission over data networks.

The ISO is an independent organisation composed of representatives of the standardisation bodies of the member countries and does much work on standardisation in the data processing world in general. The CCITT and ISO co-ordinate their work to avoid duplication of effort. A recent ISO publication (3,4) reflects modern trends in network architectures, and should be used in definition and design of protocols and networks.

This publication, produced by subcommittee 16 of ISO technical committee 97 (data processing) describes a basic reference model for "Open Systems Interconnection". This document defines the concept of layered network architectures, which is central in the definition of modern communications protocols. Some of the basic concepts of the OSI reference model are described in the following paragraphs.

The OSI reference model may be considered as a modular approach to computer network architecture, breaking a network or end-user system into seven hierarchical modules or <u>layers</u>. Communication between layers of the same system is only allowed up or down the hierarchy between adjacent layers. Communication between systems is only allowed on the basis of "peer pair" relationships: layers in one system may only communicate with layers of equal hierarchical rank in other systems.

The top of the hierarchy (level 7 : the application layer) is associated with a user application. Examples of the application layer are:

i) the operator of an automated banking terminal (a manual application process); and

ii) a programme running in a computer centre and accessing a remote data base (a computerised application process).

By way of example, if the automated banking terminal is directly connected to the host computer, the following sequence of events might take place. The operator would logon to the host computer and, after receiving an appropriate response enter an account number.

The computer could respond with the name associated with the account number and its balance. The operator could now enter transaction data, to which the computer would respond with an updated balance. Having completed the transaction the operator would logoff.

A remote user of the same system would go through the same procedure except that he might switch his terminal on-line and off-line in addition to logging on and off the system. The remote user, while part of the application process, would be unaware of the presence of a network between himself and the host. The connection between his terminal and the host could be a dedicated line, a circuit switched circuit or a packet switched virtual circuit without it effecting the application process in any way. The terminal application layer would communicate with the layer immediately below it. This layer would similarly communicate with the layer immediately below it and in this way a chain of communication between adjacent layers would be established down to the third level of the OSI model, which is responsible for call establishment across a network. (It is at this level that the distinction between different ways of establishing a connection becomes obvious).

At the host computer side of the network, the reverse process takes place, where communication is upwards to the application programme, again via consecutive layers of the OSI hierarchy.

The lower levels provide level 7 with the services required by the application. Layer 7 provides a "window" through which the application process communicates with other application processes, without being aware of the presence or function of the lower layers. Each layer "adds value" to the services provided by the layers below it.

Of particular interest to those involved with PDNs are the lower three layers, as these provide the medium for transport of the data generated and received by communicating application processes and therefore must be provided by the PDN. The description of protocols for information interchange across the DTE/DCE interface covers areas falling into all three of the lower layers. The following definitions of the network, data link and physical layers are from reference (3).

LAYER 3 : THE NETWORK LAYER

This layer provides the means to establish, maintain and terminate network connections between separate systems, the application processes of which require communication with each other. In doing so, it relieves higher layers of the routing and switching consideration associated with the establishment of a given network connection. It makes invisible to the higher layers how the network layer uses underlying resources, such as data-link connections, to provide network connection.

LAYER 2 : THE DATA LINK LAYER

This layer provides the functional and procedural means to establish, maintain and release data-link connections (built up of one or more physical connections) among network entities. Its objective is to detect and, where possible, correct errors which may occur in the physical layer. This layer gives the network layer the ability to request assembly of data circuits within the physical layer (i.e. to control circuit-switching).

LAYER 1 : THE PHYSICAL LAYER

The physical layer provides mechanical, electrical, functional and procedural characteristics to activate, maintain and deactivate physical connections for transmission of bitstreams between the entities of a data link. This is the lowest level of the OSI hierarchy.

The description of the physical layer in terms of the four characteristics mentioned above is common practise and is adopted here. It is important to realise that functional and procedural characteristics of an interface are not restricted to the physical layer only, but may cover higher layers as well.

3. X.21 : DESCRIPTION

3.1 OVERVIEW

CCITT recommendation X.21 describes an interface suitable for use on synchronous, circuit switched full duplex public data networks. The interface is described in terms of a quiescent phase and a call control phase. The call control phase is divided into call establishment, data transfer and call clearing.

The quiescent phase, describing the interface when no data is being transferred and no attempt is being made at establishing or answering a call, falls within the physical layer of the OSI model. When both sides of the interface are ready, a transition may be made from the quiescent phase to the call control phase. This happens either when the DTE indicates a call request or the DCE indicates the presence of an incoming call. Once a call has been established the data transfer phase is entered.

Exit from the data transfer phase is via the call clearing phase, after which the interface reverts to the quiescent phase. The call control phase is covered by the link and network layers of the OSI model. During data transfer however, all link and network level functions fall away, leaving a full duplex physical circuit between end-users. The significance of this is that end-users are free to implement any higher level protocol they wish to during data transfer.

In this chapter, X.21 is described in terms of the OSI model rather than emphasising the split between quiescent and call control phases.

3.2 THE X.21 DOCUMENT

The 1980 revision of CCITT recommendation X.21 is a document consisting of:

i) descriptive text covering the physical and call control elements of the interface;

ii) a series of state diagrams formally describing the procedural elements of the protocol; and

iii) a series of annexes of secondary importance to understanding the protocol, but essential for its implementation. These annexes cover such aspects as DTE time-limits and DCE time-outs, format of selection signals and recognised transitions between states.

The main elements of procedure are defined in terms of the state diagrams, with the text serving only as a backup and not as formal definition of the protocol. The text often refers to other standards and recommendations. Table 3.1 provides a cross reference listing all recommendations referred to by X.21, along with the context in which the reference was made.

RECOMMENDATION OR STANDARD	CONTEXT IN WHICH REFERENCE WAS MADE
CCITT V.3 : INTERNATIONAL ALPHABET NO. 5	ALIGNMENT OF CALL CONTROL CHARACTERS; ERROR CHECKING
CCITT X.1 : INTERNATIONAL USER CLASSES OF SERVICE IN PUBLIC DATA NETWORKS	SERVICES TO BE PROVIDED BY PUBLIC DATA NETWORKS
CCITT X.2 : INTERNATIONAL USER SERVICES AND FACILITIES IN PUBLIC DATA NETWORKS	FACILITIES TO BE PROVIDED BY PUBLIC DATA NETWORKS
CCITT X.4 : GENERAL STRUCTURE OF SIGNALS OF IA 5 CODE FOR DATA TRANSMISSION OVER PDNs	ERROR CHECKING
CCITT X.21 BIS: USE ON PDNs OF DTE DESIGNED FOR INTERFACING TO SYNCHRONOUS V-SERIES MODEMS	INTERWORKING BETWEEN X.21 AND V.24-TYPE DTE
CCITT X.24 : LIST OF DEFINITIONS FOR INTERCHANGE CIRCUITS BETWEEN DTE AND DCE ON PDNs	DEFINITION OF FUNCTIONAL CHARACTERISTICS FOR X.21
CCITT X.26: ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT	DEFINITION OF ELECTRICAL CHARACTERISTICS FOR X.21; FAULT CONDITIONS ON INTERCHANGE CIRCUITS
CCITT X.27: ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH I.C. EQUIPMENT	DEFINITION OF ELECTRICAL CHARACTERISTICS FOR X.21; FAULT CONDITIONS ON INTERCHANGE CIRCUITS
CCITT X.29 : HYPOTHETICAL REFERENCE CONNECTIONS FOR SYNCHRONOUS PDNs	REFERENCE CONNECTIONS FOR PDNs
CCITT X.96: CALL PROGRESS SIGNALS IN PDNs	DEFINITION OF X.21 CALL PROGRESS SIGNALS

TABLE 3.1 (CONTINUED OVERLEAF)

RECOMMENDATION OR STANDARD	CONTEXT IN WHICH REFERENCE WAS MADE
CCITT X.121 : INTERNATIONAL NUMBERING PLAN FOR PDNs	INFORMATION CONTENT AND CODING OF SELECTION SIGNALS
CCITT X.150 : DTE AND DCE TEST LOOPS FOR PDNs	DEFINITION OF TEST LOOPS
ISO 4903 : DATA COMMUNICATION 15-PIN DTE/DCE INTERFACE CONNECTOR AND PIN ASSIGNMENTS	DEFINITION OF MECHANICAL CHARACTERISTICS FOR X.21

TABLE 3.1 (CONTINUED)

RECOMMENDATIONS AND STANDARDS REFERRED TO BY X.21

3.3 THE PHYSICAL LAYER

The physical layer of this interface is defined mainly by reference to other standards and recommendations.

3.3.1 MECHANICAL CHARACTERISTICS

The most basic elements of the physical layer are its mechanical characteristics. One of the most important mechanical characteristics for standardisation is the DTE/DCE interface connector defined by ISO 4903 (5). Figure 1 illustrates the DCE half of this connector in detail. The pin assignments of the interface connector defined by ISO 4903 also form part of the mechanical characteristics, and are listed in Appendix D.

A further mechanical characteristic for definition is the position of the interface connector, defining the line of demarcation of responsibility between DTE and DCE. CCITT recommendation X.24 uses the connector to define the physical position of the interface. X.24 goes further to say that the connector need not physically be attached to the DCE, but may be mounted in a fixed position near the DTE. The female part of the connector belongs to the DCE.

An interconnecting cable is normally provided with the DTE. Its length is defined with the electrical characteristics of the interchange circuits, as cable length is a factor governing the maximum attainable data transmission speeds across the interface.

3.3.2 ELECTRICAL CHARACTERISTICS

The electrical characteristics of the interface are specified by reference to CCITT recommendations X.26 and X.27, which describe electrical characteristics for double-current interchange circuits (6,7).

These recommendations differ in that X.27 specifies a balanced interchange circuit allowing higher transmission speeds than X.26 where the interchange circuits are unbalanced. The two recommendations are compatible and may interwork when transmission speeds inside the X.26 range are adhered to. These speeds are specified in CCITT recommendation X.1, and are listed in Table 3.2 below.

USER CLASS OF SERVICE	DATA SIGNALLING RATE	ADDRESS SELECTION AND CALL PROGRESS SIGNALS
3	600 bits/sec	600 bits/sec, IA5+
4	2400 bits/sec	2400 bits/sec, IA5
5	4800 bits/sec	4800 bits/sec, IA5
6	9600 bits/sec	9600 bits/sec, IA5
7	48000 bits/sec	48000 bits/sec, IA5

+ IA5 : INTERNATIONAL ALPHABET NO. 5, AS IN CCITT RECOMMENDATION V.3 (10).

TABLE 3.2

Both recommendations describe the interface in terms of generators, interconnecting cable and receivers. Both describe the same balanced (differential) receiver, but X.26 has an unbalanced generator as opposed to the balanced generator of X.27. X.27 uses a signal conductor and a return conductor for each interchange circuit, while X.26 uses one signal conductor per interchange circuit and a common return in each direction of transmission. X.26 allows transmission speeds up to 100 k bits/sec with a cable length of 10 metres and up to 1 k bit/sec at 1000 metres. X.27 allows transmission speeds up to 10 Mbit/sec at 10 metres, and 100 k bit/sec at 1000 metres. (These are conservative estimates based on empirical data). Both recommendations are intended for DTEs and DCEs implemented in integrated circuit technology.

The data signal condition 0 (space) on an interchange circuit is indicated by a voltage positive with respect to the return conductor, while a 1 (mark) is represented by a negative voltage. On timing and control circuits, binary 1 and 0 indicate OFF and ON conditions respectively. Signal conditions in both recommendations are specified at the generators and at the receivers but not at the interchange point forming the line of demarcation of responsibility between DTE and DCE. This has been identified as a potential source of conflict between the owners of DTE and DCE respectively (8).

Recommendation X.21 specifies the use of X.27 on the DCE side of the interface at all times, and at the DTE side of the interface for transmission speeds above 9600 bits/sec. Up to 9600 bits/sec the DTE may conform to either X.26 or X.27.

3.3.3 FUNCTIONAL CHARACTERISTICS

The functional characteristics of the X.21 interface are defined by reference to recommendation X.24.

Table 3.3 is taken from the X.24 recommendation, and lists the interchange circuits with which the X.21 interface is implemented.

INTERCHANGE CIRCUIT DESIGNATION	INTERCHANGE CIRCUIT NAME	DATA		CONTROL		TIMING	
		FROM DCE	TO DCE	FROM DCE	TO DCE	FROM DCE	TO DCE
G	Signal Ground or Common Return						
Ga	DTE Common Return				X		
T	Transmit		X		X		
R	Receive	X		X			
C	Control				X		
I	Indication			X			
S	Signal Element Timing					X	
B	Byte Timing					X	

TABLE 3.3

X.21 INTERCHANGE CIRCUITS

CIRCUITS G AND Ga:

Circuit G is used to connect the zero-volt reference point of a generator to that of a receiver. This connection is not used with X.26 and is optional with X.27. When used, it may be connected to protective ground at will within the DCE, to minimise noise or to meet with national safety regulations.
Ga forms the DTE common return when implementing X.26.

CIRCUITS T AND C:

When C is ON, the signals on T are data being transmitted to the DCE. When C is OFF, T transmits control signals. Both these circuits are monitored by the DCE for electrical fault conditions.

CIRCUITS R AND I:

When I is ON, the signals on R should be interpreted by the DTE as data relayed by the DCE from the distant DTE. When I is OFF, the DCE transmits control signals to the DTE on R. The DTE should monitor both signals for electrical fault conditions.

CIRCUITS S AND B:

The DCE transmits timing information (i.e. a clock signal) on S at all times that the timing source is capable of generating this information. The DTE presents binary signals on T and conditions on C in which the transitions occur when S goes from OFF to ON.
The same conditions apply to the DCE signals on R and I. Circuit B is provided to give 8 bit byte timing information. It is optional with X.21 and will only be used by some administrations. Its use is not generally required, as character synchronisation will be provided by the network's transmission of synchronisation characters over R in the control state.

3.3.4 PROCEDURAL CHARACTERISTICS

3.3.4.1 EXPLANATION

The state diagrams used by the CCITT in defining the X.21 interface are associated with the concept of an interface machine. Although the recommendation makes no mention of this, the use of an interface machine implies that each side of the interface has been represented as a finite state machine (FSM) formally defined as a set with five elements.

FSM = (S, IS, OS, FNS, FOUT), where

S is a finite set of all the states permitted to occur during the operation of the interface;

IS is a finite set of all the legitimate inputs to the FSM;

OS is a finite set of all the legitimate outputs from the FSM;

FNS : S.I → S' is the next state function, mapping current (state, input) pairs into the next state; and

FOUT : S.I → OS is the output function, mapping current (state, input) pairs into the current output. (Static output as well as pulsed output signals, such as messages, are allowed).

Each valid combination of inputs from IS and outputs from OS defines a unique state belonging to S. The combination of the current state and a change in inputs results in the FSM being mapped into a new state by FNS, the next state function. A corresponding set of outputs determined by FOUT is simultaneously generated.

The X.21 interface may be represented as two finite state machines with the following input and output sets:

DTE : IS = (r,i) , OS = (t,c)
DCE : IS = (t,c) , OS = (r,i)

where t,c,r,i, represent the signals on circuits T,C,R and I respectively. The sets FNS and FOUT determine the behaviour of the DTE and DCE, being derived from the X.21 definition.

The behaviour of an interface may be modelled using the concept of an interface machine (9) and represented graphically using state transition diagrams. The interface machine uses the signals generated by both sides of the interface as its input set and has no outputs. Its behaviour is mapped by a finite set of states connected by a finite number of legitimate transitions which may be initiated by either side of the interface. A transition is caused by a change in the input set to the interface machine. The use of the interface machine is limited to situations where the transmission medium does not introduce delays and where communication is in the half duplex mode. On the whole, these conditions are met by the X.21 interface, where transmission delays may be ignored and transitions between states are initiated by either side of the interface in two-way alternate fashion.

When both sides of the interface act simultaneously, causing a "collision" as in state 15 of figure 3, the interface machine gives a poor representation of the behaviour of the interface.

3.3.4.2 DESCRIPTION

The physical layer procedural aspects of X.21 cover the following areas:

- the X.21 quiescent phase;
- the data transfer phase;
- the call clearing phase, which involves physical level handshaking across the DTE/DCE interface; and
- the implementation of dedicated circuit interfaces which only operate on the physical level.

These four areas are covered in this section.

a) The Quiescent Phase

Figure 2(a) gives an explanation of the state diagrams used by the CCITT in defining the behaviour of the X.21 interface machine. Figure 2(b) shows the set of valid states for the X.21 quiescent phase, as well as legitimate inter-state transitions. The quiescent phase may be entered after termination of the call control or data transfer phases by call clearing, or as a result of fault conditions. It may only be left via the READY STATE.

Figure 2(b) shows that both the DTE and DCE finite state machines may generate outputs corresponding to READY and NOT READY conditions, with the DTE being either CONTROLLED or UNCONTROLLED while NOT READY. This creates six valid quiescent states.

X.21 does not suggest uses for the CONTROLLED NOT READY condition. Two instances when this condition would be likely to apply are:

i) when the DTE is in local mode; and

ii) when the DTE is involved in interaction with an operator to generate selection signals.

Table 3.4 (below) summarises some of the information of figure 2(b), using FSM/interface machine notation.

DTE FSM		INTERFACE MACHINE	DCE FSM	
IS(r,i)	OS (t,c)	S	IS (t,c)	OS (r,i)
1,OFF	1,OFF	READY	1,OFF	1,OFF
1,OFF	01,OFF	DTE CONTROLLED NOT READY DCE READY	01,OFF	1,OFF
1,OFF	0,OFF	DTE UNCONTROLLED NOT READY, DCE READY	0,OFF	1,OFF
0,OFF	1,OFF	DTE READY,DCE NOT READY	1,OFF	0,OFF
0,OFF	01,OFF	DTE CONTROLLED NOT READY, DCE NOT READY	01,OFF	0,OFF
0,OFF	0,OFF	DTE UNCONTROLLED NOT READY, DCE NOT READY	0,OFF	0,OFF

TABLE 3.4

INPUT AND OUTPUT STATE SETS FOR DTE AND DCE DURING QUIESCENT PHASE

For the conditions on t,c,r,i to be interpreted as valid, they must be kept steady for at least 24 periods of the signal on S, or detected for at least 16 periods.

b) The Data Transfer Phase

The interface may leave the quiescent phase to enter the X.21 call control phase. This makes use of link and network layer features, which fall away completely once data transfer is reached. The X.21 protocol is designed to provide a transparent full duplex circuit during data transfer, allowing users the freedom of choosing any higher level protocols or network architecture they wish to. This favours the use of X.21 as the physical layer of different protocols and network architectures, such as X.25 and SNA (10,2).

Although X.21 is primarily intended to provide a full duplex circuit between end-users, half duplex operation is also supported.

Figure 6 shows how a two point dedicated line is implemented, as well as illustrating how half duplex operation may be achieved. If state 13 (DATA TRANSFER) is omitted, figure 6 represents an interface implementing half duplex data transfer. The idle state is the X.21 READY condition with both sides transmitting (1,OFF). Either side of the interface may transmit data (D,ON), provided that the other side is presenting the READY condition.

Recommendation X.21 treats the case of half duplex data transfer on the switched circuit service in the context of V.24 equipment being coupled to the network via a X.21 bis interface, where the possibility of half duplex operation arises on the DTE side. Two solutions are allowed to this problem.

i) <u>During the data transfer phase</u> X.21 bis circuits 109 (CARRIER DETECTED) and 105 (REQUEST TO SEND) are logically connected with X.21 circuits C and I respectively, via the data network, as shown in figure 5. X.21 does not specify how this "logical connection" is established. By implication it is left to the network to establish by whatever method suits the signalling system used. The implementation of this logical connection allows the realisation of half duplex transmission as described above for the case of leased lines. When the X.21 DTE signals (t, c) = (D, ON) to transmit data, the network will cause the X.21 bis DCE to signal circuit 109 (CARRIER DETECTED) ON, indicating that the V.24 DTE should expect to receive data. When the V.24 DTE signals circuit 105 (REQUEST TO SEND) ON on the X.21 bis interface, the network will cause the X.21 DCE to signal (r, i) = (D, ON). The X.21 DTE should now signal (t, c) = (1, OFF) if it is not already doing so, causing the network to switch the X.21 bis DCE circuit 109 (CARRIER DETECTED) OFF. The X.21 DTE should now be ready to receive data from the network. When the V.24 DTE signals circuit 105 (REQUEST TO SEND) OFF on the X.21 bis interface, the network should cause the X.21 DCE to signal (r, i) = (1, OFF).

ii) Alternatively, the X.21 DTE shall signal READY FOR DATA (t, c) = (1, ON), when the X.21 bis DTE signals circuit 105 (REQUEST TO SEND) OFF, effectively substituting the condition (1, ON) for (1,OFF), in figure 6. This permits half duplex working for DTEs not requiring circuit 109 (CARRIER DETECTED) to be off before signalling 105 (REQUEST TO SEND) ON.

As recommendation X.21 does not define explicit procedures for the implementation of half duplex interfaces on the switched service, but only gives the above guidelines in the context of implementing a X.21 bis interface, it is up to the local administration to decide on the exact method of realising half duplex transmission on the switched service.

c) The Call Clearing Phase

The data transfer phase may be terminated either by the DTE or by the DCE (i.e. by the remote DTE). When the DTE initiates clearing, it transmits a CLEAR REQUEST (0,OFF). The DCE responds with CLEAR CONFIRMATION (0,OFF), followed by DCE READY (1,OFF). The DTE then signals READY (1,OFF) and the interface assumes the READY state, as shown in figure 4.

The DCE clears by signalling CLEAR INDICATION (0,OFF). The DTE responds with CLEAR CONFIRMATION (0,OFF) after which the DCE indicates READY. The DTE follows suit and the interface again enters the READY state.

The clearing sequence may be entered from any state except READY, and may be initiated by either side of the interface.

d) Dedicated Circuits

The X.21 dedicated circuit interface of figure 6 covers only the physical layer of the OSI model, containing no link or network layer features. This interface allows the implementation of point to point and centralised multipoint dedicated circuits. With centralised multipoint working (the configuration of figure 7) the data transmitted by the central DTE is delivered to all remote DTEs and the data transmitted by the remote DTEs (one by one as determined by the data link protocol) is delivered to the central DTE. While the transmitting party is in state 13 S, the receiving party is in state 13 R of figure 6. During state 13 the central DTE sends data to all remote DTEs while the remote DTEs transmit to the central station, one by one as determined by the data link protocol.

3.4 THE LINK LAYER

3.4.1 SYNCHRONISATION

The handshaking protocol of the call control phase shown in figure 3 is character orientated. Synchronisation between DTE and DCE is required to ensure that characters are defined between specific limits and also so that entry and exit from states may be made on character boundaries. The byte timing information provided by the DCE of some networks on circuit B may be used to this end, but is not of general value as it will not be universally adopted. Recommendation X.21 requires all networks to transmit synchronisation information on circuit R at the start of the call control phase. The IA5 characters "+" and "BEL" in states 3 and 8 of figure 3 must be preceded by a minimum of two "SYN" characters. These should be used by the DTE to align itself with the DCE for the rest of the call control phase. Subsequent "SYN" transmissions by the DCE may be used by the DTE to check synchronisation.

Once the end to end connection has been established and both DTEs are in the DATA TRANSFER PHASE (state 13), they are responsible for establishing their own alignment as X.21 link layer functions fall away once the call has been set up.

3.4.2 ERROR DETECTION AND CORRECTION

Besides being responsible for synchronisation, the link layer must detect and possibly correct errors which may occur within the physical layer. Normally, the link layer is required to perform its functions on a data link between two points having a significant physical separation. In the case of X.21, the link layer operates across the interface between DTE and DCE, which is usually only a small distance. The probability of errors occurring on this short link is minimal under normal working conditions.

CCITT recommendation X.21 specifies the use of IA5 characters with one parity bit (odd parity) for error checking. No provision is made for error correction, other than the possibility of clearing the call and retrying, as a result of incorrect (or no) responses being received on transition to a new state. This action is further explained in section 3.5.

Once the end-to-end connection has been established and both DTEs are in the DATA TRANSFER PHASE (state 13), they are responsible for establishing their own error detecting and correcting procedures.

3.5 THE NETWORK LAYER

The network layer of X.21 provides a call control phase (figure 3) which is entered from the quiescent phase via the READY state. The call control phase is normally terminated by the data transfer phase, when all link and network layer features of X.21 fall away.

At any stage during call establishment, the clearing phase may be entered and the interface returned to the quiescent phase.

The call establishment phase of figure 3 appears to be based on the way a normal dial-up telephone call is established. The READY state corresponds to the on-hook condition, and the CALL REQUEST and INCOMING CALL states to someone lifting a handset off-hook before dialling, and a telephone ringing. Selection signals correspond to dialling impulses, and the states immediately preceding data transfer may be compared to the various tones generated by a telephone network. The CALL ACCEPTED state corresponds to a person lifting the handset off-hook when answering a ringing telephone.

In the following paragraphs, call establishment, facilities available with X.21, and the role of time-limits in controlling the network layer are discussed.

3.5.1 CALL ESTABLISHMENT

The call establishment procedure starts with the interface in the READY state. From this point a call may be either requested or received.

When a call is to be made the DTE initiates the procedure by signalling CALL REQUEST (0,ON). The DCE responds with PROCEED TO SELECT (+,OFF). The DTE now transmits SELECTION SIGNALS (IA5,ON) to indicate the address of the called party and other relevant information, followed by DTE WAITING (1,ON).

The DTE now waits for the DCE to respond with READY FOR DATA (1,ON). If the DCE does so, data transfer can take place (state 13). However, while the network is busy connecting the call, the DCE may provide the DTE with information as to how the call is progressing (states 6,7/10 and 11 : DCE WAITING, DCE PROVIDED INFORMATION, CONNECTION IN PROGRESS respectively).

Depending on how long it takes to connect the call and on the facilities requested by the DTE, all or some of these states may be entered into and the relevant information transmitted to the DTE before state 12, READY FOR DATA, is entered.

In the event of the DCE being unable to establish a call requested by the DTE, it will provide information in the form of CALL PROGRESS SIGNALS to the DTE, indicating why the call is not being established. These CALL PROGRESS SIGNALS (state 7/10) may be followed either by a DCE CLEAR INDICATION or by DCE WAITING, depending on what the factors impairing call establishment are. (Appendix C contains a list of CALL PROGRESS SIGNALS with their codes, while Appendix B shows the format of all DCE provided information). The DCE PROVIDED INFORMATION (state 7/10) may also include CALLED LINE IDENTIFICATION if requested by the DTE.
(See Section 3.5.2 : Facilities).

With an incoming call, the sequence again starts with the interface in the READY state. The DCE signals INCOMING CALL (BEL,OFF) and the DTE responds with CALL ACCEPTED (1,ON). As before the DCE could respond to this with READY FOR DATA, but it could also go through states 6, 10 bis and 11 (DCE WAITING, DCE PROVIDED INFORMATION, CONNECTION IN PROGRESS) before entering state 12, depending on how long it takes to connect the call and on the facilities provided by the DCE.

The DCE PROVIDED INFORMATION may include CALLING LINE IDENTIFICATION or CHARGING ADVICE.

In the event of a CALL COLLISION (state 15), where an INCOMING CALL coincides with a CALL REQUEST, the DTE is given preference and the incoming call refused. State 3, PROCEED TO SELECT, then follows the collision and the normal call request sequence is completed.

3.5.2 FACILITIES

Recommendation X.21 allows the user to take advantage of a number of optional facilities provided by the network. These facilities are:

i) facility registration and cancellation;

ii) direct call;

iii) abbreviated addressing;

iv) multiple address calling;

v) called line identification;

vi) calling line identification;

vii) closed user group;

viii) redirection of calls; and

ix) charge advice.

Depending on the network implementation of X.21 and on the facility concerned, the user may activate the desired facility either when subscribing to the network, or via his terminal at any time he wishes to.

FACILITY REGISTRATION OR CANCELLATION:

This is done by the DTE making a call to the network. During state 4, SELECTION SIGNALS, the DTE indicates the nature of the facility required by using a special selection sequence. The network responds with the appropriate CALL PROGRESS SIGNAL to indicate acceptance or rejection of the registration/cancellation actions, and then terminates the call by signalling CLEAR INDICATION.

DIRECT CALL:

A user who is registered for the direct call facility can make direct calls to a predetermined address by responding to PROCEED TO SELECT (state 3) with DTE WAITING (state 5), instead of giving SELECTION SIGNALS (state 4). When this facility is provided on a per-call basis the user may either go through the normal selection sequence, or make direct calls.

ABBREVIATED ADDRESSING:

This is used to represent a designated full address with a reduced number of characters. This facility would be used where the designated addresses are frequently accessed by the DTE.

MULTIPLE ADDRESS CALLING:

This facility may be used to establish conference or broadcast types of communication.

CALLED LINE IDENTIFICATION

When this is requested, the network verifies the address of the called party during state 7/10 : DCE PROVIDED INFORMATION. This allows the user to detect when his call is being redirected.

CALLING LINE IDENTIFICATION:

This feature enables a DTE to prevent calling parties from gaining unauthorised access to its address. The network identifies the calling party during state 10 bis : DCE PROVIDED INFORMATION.

CLOSED USER GROUP:

A subscriber in a closed user group generally communicates only with other members of his group. He does not have free access to the rest of the network, nor can the rest of the network access him. (There are variations of this concept, allowing some members of the group outside communication).

REDIRECTION OF CALLS:

The subscriber may have the network redirect all incoming calls to another address (eg.outside normal office hours), by prior arrangement with the network.

CHARGE ADVICE:

If desired, the network will call the DTE within 200m Sec of the termination of an outgoing call and indicate the cost of the call during state 10 bis : DCE PROVIDED INFORMATION.

Apart from the facilities already defined, new facilities may be added to the network as the need is identified.

3.5.3 DTE TIME-LIMITS AND DCE TIME-OUTS

X. 21 contains details of time-limits and time-outs to be used to resolve deadlock situations resulting from equipment malfunctions on either side of the interface, or from infrequently encountered collisions on the interface. The following examples illustrate their use.

After the DTE signals CALL REQUEST, the network should respond within three seconds with PROCEED TO SELECT. If this signal is not received within the specified time-limit, the DTE should return to the READY condition. Another example is the two second time-limit imposed on the DCE to respond to CALL ACCEPTED (state 9) either with READY FOR DATA or with DCE CLEAR INDICATION. If the DCE responds with DCE PROVIDED INFORMATION (state 10 bis) the time-limit is reset. If this time-limit expires, the DTE should signal DTE CLEAR REQUEST.

After the DCE signals PROCEED TO SELECT (state 3), two simultaneous time-outs are started. The DTE has 36 seconds to send the complete selection signal, and 6 seconds within which to respond with the first selection character. The 6 second time-out is reset every time a selection character is received. If either time-out expires, the DCE will signal DCE CLEAR INDICATION, which may be preceded by an appropriate CALL PROGRESS SIGNAL.

The shortest time-out is started by a DCE CLEAR INDICATION. The DTE has 100 ms to respond with a CLEAR CONFIRMATION. The DTE must also respond with READY, inside 100 ms of the DCE indicating DCE READY.

A full list of time-limits and time-outs is given in Appendix E.

3.6 TEST LOOPS

To assist with the location of faults on interconnections, X.21 specifies three test loops from recommendation X.150, which defines a family of test loops. These test loops are illustrated in figure 8 and serve the following functions.

LOCAL TEST LOOP - LOOP 3

Signals (t,c) are presented on circuits (R,I) of the local DTE/DCE interface when this loop is activated. The DTE uses it to verify operation of the DTE/DCE interface. At present, manual control of this loop from the DCE is suggested, with automatic operation being a possible future extension.

NETWORK TEST LOOP - LOOP 2

This loop is activated in the remote DCE. Again, (t,c) are presented on (R,I). The DTE uses this loop to verify operation of the network circuit as far as the remote DCE. It may be controlled manually from the DCE, automatically from the network or automatically from the remote DTE. The method for automatic control of this loop is left as a national option.

DTE TEST LOOP - LOOP 1

This loop is activated inside the DTE itself and is under full control of the DTE. It is used to verify operation of the local DTE.

3.7 ADVANTAGES AND SHORTCOMINGS

One of the major advantages in the use of X.21 as opposed to existing protocols is that it has been developed specifically for use with public data networks. This makes it possible to take advantage of facilities offered by a PDN, as shown in section 3.5.2.

As most administrations developing circuit switched PDNs are showing a strong interest in the X.21 interface, it appears likely to become at least very widely, if not universally accepted. This offers a significant compatibility advantage.

The following factors are obvious advantages over any alternatives for the same application (8, 11, 12).

i) <u>Improved physical layer characteristics</u>

X.21 uses a smaller interface connector than any other standard because it requires fewer interchange circuits. This results in fewer generators and receivers being required and translates to a cheaper interface, particularly on the DCE side.

X.21 has superior electrical characteristics to other interfaces, allowing higher data rates and far longer interface cables.

ii) <u>Link Layer Features</u>

The use of a link layer in support of the network layer results in a character-orientated handshaking protocol with the ability to detect errors in data transferred during call establishment. The link layer supports the network layer in allowing the transfer of characters across the interface to achieve fast, efficient call set-up (typically 200 to 500 mSec) and direct user-network communication. (Older standards require a separate interface for call set-up).

iii) <u>Network Layer Features</u>

The most significant network layer feature of X.21 is the ability to perform call establishment using the same physical layer interface as used for data transmission. Apart from this, the user may interpret call progress signals and use the facilities mentioned in section 3.5.2 with his terminal. As new value-added network features become available, they may easily be passed on to the user.

iv) Documentation

The use of state transition diagrams in the formal definition of this recommendation, serves to provide a clear and comprehensive definition of the interface. There are few ambiguous areas.

Apart from the obvious disadvantage of the lack of compatibility between X.21 and existing equipment, for which X.21 bis is intended as an intermediate solution, the following shortcomings have been mentioned regarding this protocol.

i) The DTE is not aware of other calls queueing during the data transfer phase, nor is there any facility for network recall (13) (the ability of the terminal to communicate with the network during data transfer). Network recall would however detract from the transparent nature of this protocol after call setup.

ii) A more significant shortcoming is that the DTE cannot be made aware of incoming calls or queueing while CONTROLLED NOT READY (14). This is a relevant criticism as the CONTROLLED NOT READY state can be used to indicate that the DTE is in local mode, when it might be desireable to switch the DTE to line to service an incoming call.

iii) The use of time-outs to resolve deadlock situations has been criticised. Razouk and Estrin (14) have developed a modified interface machine for X.21 which does away with the need for time-outs by introducing a small number of additional states.

iv) The method used by the DCE to indicate charge advice could be improved on (13). A more elegant solution would have been the incorporation of this facility as an option during the clearing phase.

v) Yanoschak (11) points out that poor use is made of the network by allowing the DTE to take priority in resolving call collisions. This is true, but is done in case the DTE call is a matter of urgency. As the probability of a collision occurring is small, network overhead due to this feature is negligible.

vi) West and Zafiropulo (15) point out that the state transition diagrams used to define X.21 do not represent the behaviour of the interface correctly during collisions. A better representation would have been gained by using separate state transition diagrams for DTE and DCE, representing each as a finite state machine.

These criticisms are justified and their consideration in future revisions of X.21 would further enhance the protocol. Even without their inclusion, however, X.21 remains the most effective interface for connecting a DTE to a synchronous, circuit switched public data network.

4. V.24:DESCRIPTION

4.1 OVERVIEW

CCITT recommendation V.24 (16) is a general purpose DTE/DCE interface for serial binary data communication over the public telephone network. Rather than being an interface definition, it is a collection of circuit definitions from which a selection must be made to implement a given interface.

V.24 covers the so-called 100-series of interchange circuits for use with general applications, as well as the 200-series intended for use with automatic calling equipment. The use of automatic calling equipment requires a separate interface (V.25, not used in this country) to be installed along with the V.24 interface. As only the 100-series of circuits are relevant to DTE/DCE interfacing in this country, the 200-series will not be discussed.

The first publication of V.24, in 1964, was based on the American EIA standard, RS-232. V.24 and RS-232 have evolved together over the years and cover similar ground but are by no means identical. The current and final version of the EIA standard is RS-232-C and forms a formal interface definition (17).

In this chapter V.24 is described in terms of the physical layer of the OSI model, as it does not have any link or network layer features.

4.2 V.24 DOCUMENTATION

The 1980 revision of CCITT Recommendation V.24 consists of descriptive text covering the functional and procedural aspects of the protocol. The text refers the reader to ISO standard 2110 for the interface mechanical characteristics, while permissible electrical characteristics are defined in recommendations V.10, V.11 and V.28. In several modem recommendations implementing a V.24 interface, the reader is referred to ISO 4902 (25) for the mechanical characteristics to be used with V.10 or V.11 electrical characteristics.

Table 4.1 lists the CCITT recommendations and ISO standards referred to in the V.24 text, as well as the context in which the reference was made.

RECOMMENDATION OR STANDARD	CONTEXT IN WHICH REFERENCE WAS MADE
ISO 2110 : Data Communication-25-pin DTE/DCE interface connector and pin assignments.	Mechanical characteristics for V.24 interface.
ISO 4902: Data Communication-27-pin and 9-pin DTE/DCE interface connectors and pin assignments.	Mechanical characteristics of interface for automatic calling equipment.
CCITT S16: Connection to the telex network of an automatic terminal using a V.24 DTE/DCE interface.	Connection of automatic terminals to the telex network.
CCITT V.10, V.11, V.28 and V.31: Electrical characteristics of single and double-current interchange circuits.	Electrical characteristics of signal ground and common return conductors.
CCITT V.35: Data transmission at 48 k-bits/sec using 60-108 kHz group band circuits.	Electrical characteristics of signal ground and common return conductors.
CCITT V.21: 300 b/sec duplex modem for use in general switched telephone network.	Original usage of circuits 126 and 127.
CCITT V.25: Automatic calling equipment on general switched telephone network.	Procedures for automatic calling equipment.
CCITT V.54: Loop test devices for modems.	Loop test conditions for maintenance testing.

Table 4.1 RECOMMENDATIONS AND STANDARDS REFERRED TO BY V.24

4.3 INTERFACE DEFINITION

This protocol exists only in the physical layer, as opposed to X.21 which covers the three lower layers of the OSI model. The network level function of addressing is left either to V.25 (Automatic Calling and/or Answering Equipment), or to an operator doing manual dialling. A common application is with the use of dedicated lines, where the addressing function is not required. As with X.21, the physical layer is broken into its mechanical, electrical, functional and procedural characteristics for the purposes of description.

4.3.1 MECHANICAL CHARACTERISTICS

V.24 has traditionally made use of a 25-pin D-type connector as opposed to the 15-pin connector used with X.21. This connector (shown in figure 9) is specified by reference to ISO 2110 (21). The pin assignments for the interface are listed in Appendix D. The conventions for the position and significance of the interface connector are as with X.21.

The latest V-series recommendations for DCE allow the use of mechanical characteristics as laid down by ISO 4902 (25), provided electrical characteristics conforming to V.10 or V.11 are implemented.

The use of an ISO 2110 25-pin connector with V.24 circuits shall be assumed here, as this is relevant to V.24 equipment currently in use in this country.

4.3.2 ELECTRICAL CHARACTERISTICS

The electrical characteristics commonly associated with V.24 interfaces are described in recommendation V.28. Recommendation V.10 and V.11 (8), (9) describe electrical characteristics which are implemented in some newer equipment. (CCITT recommendations X.26 and X.27, describing the X.21 electrical characteristics, consist solely of a reference to the texts of V.10 and V.11 respectively).

The latest V-series DCE recommendations make allowance for the use of V.10/V.11 electrical characteristics, and state that CCITT policy is to encourage phasing out V.28 in favour of a V.11/ISO 4902 type interface. However, as most existing equipment implements V.28, interchange circuits shall here be assumed to have V.28 electrical characteristics.

The V.28 characteristics allow data rates up to 20 kbits/sec for a cable not exceeding 15 metres in length. Unbalanced interchange circuits employing a common return conductor for both directions of transmission are described. Apart from describing load and source characteristics, voltage levels and signal characteristics at the interchange point are also specified. For data circuits, binary 1 is represented by a voltage less than minus 3 volts, and binary 0 by a voltage greater than plus 3 volts. For control and timing circuits, the ON condition is represented by a voltage greater than plus 3 volts, and the OFF condition by a voltage less than minus 3 volts.

As the case of synchronous working is the only one of interest here, the same synchronous speeds mentioned with X.21 (table 3.2) are also appropriate, except that 48 kbits/sec is too high for V.24.

4.3.3 FUNCTIONAL CHARACTERISTICS

The current revision of V.24 (16) lists some 43 interchange circuits (see appendix D). It is not intended that all these circuits be used in one interface but rather that a selection be made to suit a particular application. The V-series modem recommendations all contain subsets of V.24 to be used in the DTE/DCE interface. The V.24 circuits required for use in most practical interfaces correspond to those defined in ISO 2110, listed in table 4.2. The fact that these circuits are all defined as a standard interface does not imply that they all have to be used in a given piece of equipment. As with the wider range of V.24 circuits, the intention is that a selection be made to suit a given application. Table 4.3 is a selection of commonly used interchange circuits encountered on synchronous equipment in this country. In the following sections the approach has been to use the circuits of Table 4.3 as a small common denominator of frequently used circuits essential to the correct functioning of the interface.

In describing the use of the more common circuits, it is convenient to group them in terms of specific functions. All the circuits (excepting the common return) carry binary signals, with the functions below being true for the ON condition, unless stated otherwise.

PIN NO.	CIRCUIT NO.	NAME	GROUND	DATA		CONTROL		TIMING	
				FROM DCE	TO DCE	FROM DCE	TO DCE	FROM DCE	TO DCE
1		Note 1							
2	103	Transmitted data			x				
3	104	Received date		x					
4	105	Request to send					x		
5	106	Ready for sending				x			
6	107	Data set ready				x			
7	102	Signal ground	x						
8	109	Received line signal detector (RLSD)				x			
9		Note 2							
10		Note 2							
11		Note 2							
12	122	Backward channel RLSD				x			
13	121	Backward channel ready				x			
14	118	Transmitted backward channel data			x				
15	114	Transmitter signal element timing (DCE)						x	
16	119	Received backward channel data	x						
17	115	Receiver signal element timing (DCE)						x	
18	141	Local loopback					x		
19	120	Transmit backward line signal					x		
20	108/2	Data terminal ready					x		
21	140	Loopback/maintenance test					x		
22	125	Calling indicator				x			
23	111	Data signal rate selector (DTE)					x		
24	113	Transmitter signal element timing (DTE)							x
25	142	Test indicator				x			

TABLE 4.2 25-PIN V.24 INTERFACE ACCORDING TO ISO 2110

NOTES TO TABLE 4.2

NOTE 1: When shielded interface cable is used, the shield is connected to this pin.

NOTE 2: National option.

INTERCHANGE CIRCUIT NUMBER	NAME	GROUND	DATA		CONTROL		TIMING	
			FROM DCE	TO DCE	FROM DCE	TO DCE	FROM DCE	TO DCE
102	Signal ground or common return	x						
103	Transmitted data			x				
104	Received data		x					
105	Request to send					x		
106	Ready for sending				x			
107	Data set ready				x			
108/2	Data terminal ready					x		
109	Data channel received line signal detector				x			
114	Transmitter signal element timing (DCE)						x	
115	Receiver signal element timing (DCE)						x	

TABLE 4.3

COMMONLY USED V.24 INTERCHANGE CIRCUITS

Equipment readiness

Data Terminal Ready (DTR) and Data Set Ready (DSR) circuits 108/2 and 107, are used to indicate the state of readiness of the interface. DTR is used by the terminal to prepare the DCE to connect to line. Where the line connectoin is established by supplementary means, DTR maintains this connection. The terminal is permitted to present this signal whenever it is ready to transmit or receive data. DTR OFF causes the DCE to disconnect from line. In dedicated line applicatoins, this signal should always be ON.

DSR is considered as a response to DTR. DSR indicates that the DCE is connected to line and is ready to exchange further control signals to initiate data transfer. DSR OFF indicates that the DCE is not ready to operate. When DTR is turned OFF, it may not go ON again until the DCE turns DSR OFF.

The conditions on other circuits (apart from the Ring Indicator, circuit 125) are not valid until both DTR and DSR are ON.

Call Establishment

Request To Send (RTS), Clear To Send (CTS) and Carrier Detected (CD) are the signals used for call establishment. (CD and CTS are respectively named Data Channel Received Line Signal Detector and Ready for Sending by the CCITT: popular abbreviatoins are used here for convenience). RTS is a DTE signal causing the DCE to assume the transmit mode. In half duplex operation, RTS OFF puts the DCE into the receive mode. CTS is a DCE response to RTS, indicating that the DCE is prepared to transmit data presented by the DTE across the network, as a data channel has been established to the remote DCE[3].

3) In some modems, CTS means that the remote DTE is ready to receive data. Usually however, CTS has no end-to-end significance, and the status of the remote DCE and/or DTE is only determined on the link layer.

CD is a DCE signal indicating that a line signal from the remote DCE is being received within appropriate limits as specified in relevant DCE recommendations. CD OFF implies that data presented by the DCE to the DTE is not valid.

Once the DCE responds to RTS with CTS, the DTE may transmit data. RTS may not be turned off until the last DTE data bit has crossed the interface. After it has been turned OFF, RTS may not be turned ON again until CTS has been turned OFF.

Direction of Transmission

When full duplex transmission is employed, the signals DTR, DSR, RTS, CTS and CD should all be ON during data transfer.

With half duplex transmission, RTS conditions the DCE to transmit data across the network. CTS is the required DCE response, indicating that the DTE may transmit data. When the DTE has finished its transmission it turns RTS OFF, putting the DCE into the receive mode. The DCE should respond by turning CTS OFF. When it detects a valid data signal from the remote DCE, CD signals the DTE to expect data. During half duplex transmission, CD may not be ON simultaneously with RTS/CTS.

Data Circuits

Transmitted Data (TXD) and Received Data (RXD), circuits 103 and 104, are used to transfer data between DTE and DCE across the interface in serial bitstreams. The format of these bitstreams is outside the scope of V.24.

The **DTE** may only transfer data on TXD when DTR, DSR, RTS and CTS are all ON.

When these circuits are all ON and there is no data to transmit on TXD, the DTE may transmit binary 1, line reversals or other sequences to maintain timing synchronisation. When RTS and CTS are both OFF, TXD must be held at binary 1. The DCE must always hold RXD at binary 1 when CD is OFF. With half duplex transmission, RXD must be binary 1 and CD OFF when RTS is ON.

Timing Circuits

Transmitter Signal Element Timing (TSET) and Receiver Signal Element Timing (RSET), circuits 114 and 115 respectively, are the only DCE circuits normally used to provide the DTE with timing information for synchronous transmission. Both signals have nominally equal ON and OFF periods. The DCE should provide timing information on both circuits at all times, although the accuracy and stability of RSET are only critical when CD is ON.

The DTE presents a data signal on TXD in which the transitions between signal elements coincide with OFF to ON transitions on TSET. The OFF to ON transitions of RSET indicate the nominal centres of signal elements on RXD.

Common Return

Signal Ground (Circuit 102) establishes a common return conductor for both directions of transmission when V.28 is adhered to. When implementing V.10 or V.11 it is used as the d.c. reference potential.

Miscellaneous Circuits

The Ring Indicator, circuit 125, is a DCE signal used with automatic calling and answering equipment to indicate the presence of an incoming call on the switched service. This is the only signal to be considered valid when DTR and DSR are OFF. Its use is not supported in this country.

There are three test circuits which may be implemented in V.24 equipment:

i) Loopback/Maintenance Test (circuit 140), used by the DTE to initiate loopback or other conditions;

ii) Local Loopback (circuit 141), used by the DTE to establish a local loopback (i.e., to test the DTE/DCE interface); and

iii) Test Indicator (circuit 142), used by the DCE to indicate when it is under test.

Secondary Channel

Table 4.2 shows the use of a secondary channel (circuits 118, 119, 120, 121 and 122). The circuits in question fulfil the same function as their similarly named counterparts in the primary channel described in this chapter. The secondary channel operates at a lower speed than the primary channel, and is normally used for maintenance and test purposes and verification of the integrity of data transmitted on the primary channel. It may be used to establish a form of duplex working in some applications.

4.3.4 PROCEDURAL CHARACTERISTICS

The procedural characteristics of the V.24 interface may be split into two categories; switched services and dedicated lines. The switched case consists of call establishment, data transfer and call clearing, while call establishment and clearing do not apply to dedicated lines.

4.3.4.1 SWITCHED SERVICE

Figure 10 shows the different phases a V.24 interface goes through to realise data transfer. Being purely a physical level protocol, V.24 depends on some external means of establishing the physical circuit between endusers. This function may be fulfilled either by a human operator or by using a separate V.25 interface with automatic calling and answering equipment.

In both cases the external method of call establishment fulfils network layer functions, the V.24 interface only being used for physical layer elements of handshaking and data transfer. As automatic calling equipment is not used on the telephone network in this country, figure 10 shows the procedure followed by a human operator in establishing the physical circuit between end users and connecting the DCE to line.

Before the DCE is connected to line, it must signal the OFF condition on DSR (circuit 107), so that none of the signals on the interface may be considered valid. (See the paragraph "equipment readiness" in section 4.3.3). After the DCE has been connected to line, handshaking beings across the interface. Once circuits DTR and DSR (108/2 and 107) are both ON, either side of the interface may continue the handshaking. If the DTE wishes to transmit data, it switches RTS ON and waits for the DCE to respond with the ON condition on CTS before transmitting data. If the DCE wishes to transmit data, it signals the ON condition on CD and is then free to transmit. Figure 10 shows line turnaround during data transfer when half duplex transmission is used. (See the paragraph "direction of transmission" in section 4.3.3).

Figure 11 shows how call clearing is achieved on the switched service. At any stage after the DCE has been connected to line and the signals DTR and DSR are ON the DTE may initiate a clearing sequence by signalling OFF on DTR. The DCE responds by signalling OFF on DSR, indicating that it is now disconnected from the line. On the switched service, exit from the data transfer phase is always via this clearing sequence.

4.3.4.2 DEDICATED LINES

Figure 12 shows the phases a V.24 interface goes through when used with a dedicated line. In dedicated line applications, circuit DTR (108/2) should always be ON while the DTE is powered up. As the DCE is permanently connected to line circuit DSR (107) should also always be ON in response to DTR.

Further handshaking is similar to the switched service, except that there is no call clearing sequence. Exit from the data transfer phase is either by the DCE signalling OFF on CD, or by the DTE signalling OFF on RTS.

4.4 CCITT RECOMMENDATION X.21 BIS (19)

CCITT recommendation X.21 bis is intended as an interim measure to facilitate smooth introduction of public data networks on which the X.21 interface is to be made available.

To fulfil this purpose, it describes a V.24 interface which differs from table 4.3 only in that the test circuits (140, 141 and 142; see section 4.3.3) are included in the interface to be used with dedicated lines. In addition, the ring indicator is included in the switched service interface. Where it is desired to use automatic calling and answering equipment, the implementation of a V.25 interface in conjunction with the X.21 bis interface is described.

X.21 bis claims to conform to V.24 and appropriate modem recommendations in its implementation of the V.24 circuits utilised, so that its operation corresponds to the V.24 interface described in this chapter. Duplex working is assumed, with half duplex operation being treated as a special case.

A secondary channel is not implemented.

The X.21 bis interface only operates in the physical layer of the OSI model, depending on automatic calling/answering equipment with a V.25 interface, or on manual operation to realise the network layer.

5. TRANSLATING BETWEEN X.21 AND V. 24

5.1 OVERVIEW

5.1.1 X.21 DTE TO V.24 DCE TRANSLATION

As the V.24 interface only covers the physical layer, V.24 DCEs cannot provide the network layer functions required during the call control phase of the X.21 switched service. If these network layer functions are required, they may be provided in either of the following two ways:

i) automatic calling and answering equipment with a V.25 interface may be used; or

ii) one may use manual operation for call control, as is done with the present dial-up system over the telephone network.

The first possibility, requiring X.21 to V.25 conversion for call control and X.21 to V.24 conversion for data transfer, is discarded because the V.25 interface is not supported in this country.

The second possibility may be used with relative ease by configuring the X.21 DTE to operate on a dedicated line, in accordance with the state diagram of figure 6. Translation between the X.21 and V.24 interfaces may then be done using an interface adaptor consisting of simple logical connections between the two interfaces.

The implementation of dedicated circuit services is straightforward, requiring only the above adaptor.

X.21 features such as direct calling, call progress signals or other DCE provided information will not be available to the X.21 DTE, as these are essentially features of the data networks which support the X.21 interface. It is assumed that where it is required to interface a X.21 DTE to a V.24 DCE, the DCE belongs to a telephone network and not to a data network.

5.1.2 V.24 DTE TO X.21 DCE TRANSLATION

V.24 DTEs cannot operate within the network layer to interact with X.21 DCEs, as required during call control on the X.21 switched service. The translation process must therefore provide the X.21 DCE with network layer information such as selection signals, and be capable of interpreting and processing DCE provided information.

This leads to a microprocessor-based device performing the necessary translation, as in figure 13. This translator appears as a V.24 DCE to the terminal, and as a X.21 DTE to the network. It also requires an operator interface consisting of a keypad and display, to allow an operator to initiate X.21 call control procedures as required.

Hardware and software for a preliminary model of such a translator, developed on an evaluation system, are described later in this chapter.

Where the V.24 DTE requires only dedicated line facilities on the X.21 network, translation may be done using an adaptor consisting of logical connections between the two interfaces. This adaptor operates on the physical level only, as the X.21 protocol for dedicated lines does not operate in the network or link layers.

5.2 X.21 DTE TO V.24 DCE TRANSLATION

As has been stated in section 5.1.1, the translation between a X.21 DTE and V.24 DCE may be based on an interface adaptor which expects the DTE to be configured for use on a dedicated circuit, according to the state diagram of figure 6. Subject to the constraints outlined below, such a circuit may be either full or half duplex. Where the V.24 DCE is not connected to a dedicated circuit, dial up facilities are assumed to establish the circuit between end-users. The adaptor operates within the physical layer only, as network and link layer functions are not required.

The state diagram of figure 6 shows a X.21 interface which may be used either for full or half duplex transmission. If state 13, DATA TRANSFER, is never entered, half duplex transmission is being used. This differs from the half duplex transmission normally associated with a V.24 interface, in that figure 6 assumes the use of a standard X.21 four-wire circuit across the network, supporting full duplex transmission across the DTE/DCE interface. The transition from SEND DATA to RECEIVE DATA (states 13S and 13R) may therefore be comparatively fast, because no allowance needs to be made for the time taken by line turn-around across the network, as must be done with the two-wire circuits commonly used with V.24 half duplex interfaces.

Figure 14 shows an interface adaptor which takes account of the above factors. When full duplex (four-wire) transmission is used, this adaptor implements the main state diagram of figure 6 exactly. When half duplex transmission is used, the adaptor signals DCE NOT READY to the X.21 terminal during line turn-around, after which it proceeds as normal. For those cases when line turn-around is effectively instantaneous (as when half duplex transmission is implemented over a four-wire circuit and RTS is looped back to CTS in the V.24 DCE) the adaptor does not generate the DCE NOT READY condition.

The adaptor of figure 14 was designed by taking the definitive state diagram of figure 6 and identifying V.24 conditions equivalent to the X.21 states. This information was consolidated in truth tables in terms of inputs and outputs. Boolean expressions for the outputs were then derived and translated into the combinational logic circuit of figure 14.

Table 5.1 (below) gives the X.21 states described by figure 6 and the equivalent V.24 conditions. The eventuality of the X.21 DTE signalling UNCONTROLLED NOT READY (as it would when powered down) has also been included in the table, as has the case of line turn-around. The latter case arises while waiting for CTS to respond to RTS on the V.24 interface, while line turn-around is being accomplished with half duplex transmission. It was decided that during this period the DCE signal on the X.21 interface should be NOT READY. The X.21 state diagram of figure 6, indicates that this is a valid procedure and that the X.21 DTE condition remains constant while the DCE signals R, I = 0, OFF. When CTS goes ON, R must go from 0 to 1 so that the interfaces revert to the condition shown in the second line of table 5.1 (state 13S : SEND DATA).

Should the X.21 DTE signal UNCONTROLLED NOT READY, this will be translated as DTR OFF on the V.24 interface. Where dial-up facilities have been used to establish a circuit across the network from the local interface, this signal will result in the DCE releasing the call and responding with DSR OFF.

	X.21 INTERFACE				V.24 INTERFACE						
X.21 STATE	T	C	R	I	TXD	RTS	DTR	RXD	CD	CTS	DSR
1: READY	1	OFF	1	OFF	1	OFF	ON	1	OFF	OFF	ON
13S: SEND DATA	D	ON	1	OFF	D	ON	ON	1	OFF	ON	ON
13R: RECEIVE DATA	1	OFF	D	ON	1	OFF	ON	D	ON	OFF	ON
13: DATA TRANSFER	D	ON	D	ON	D	ON	ON	D	ON	ON	ON
DCE NOT READY	-	-	0	OFF	-	-	-	X	X	X	OFF
DTE UNC. NOT READY	0	OFF	-	-	X	X	OFF	-	-	-	-
TURN-AROUND	D	ON	0	OFF	D	ON	ON	1	OFF	OFF	ON

TABLE 5.1 X.21/V.24 EQUIVALENT STATES

The information of table 5.1 may be used to draw up truth tables in terms of inputs and outputs from which the boolean expressions required for the adaptor may be derived. The outputs may be divided into two groups. The first consists of V.24 outputs TXD, RTS and DTR, caused by X.21 inputs T and C. The second group consists of X.21 outputs R and I and is caused by V.24 inputs RXD, CD, CTS and DSR and the V.24 signal RTS, an output from the first group. Inspection of table 5.1 shows that the expression RTS = C is always valid, so that the second group of outputs may be said to be caused by V.24 inputs RXD, CD, CTS and DSR and the X.21 input C. (This is a slightly more elegant statement than the first). Tables 5.2 (a) and 5.2 (b) are based on the above : table 5.2 (a) refers to the first group of outputs and 5.2 (b) to the second.

	INPUTS		OUTPUTS		
X.21 STATE	T	C	TXD	RTS	DTR
1: READY	1	OFF	1	OFF	ON
13S: SEND DATA	D	ON	D	ON	ON
13R: RECEIVE DATA	1	OFF	1	OFF	ON
13: DATA TRANSFER	D	ON	D	ON	ON
DCE NOT READY	-	-	-	-	-
DTE UNC. NOT READY	0	OFF	X	X	OFF
TURN-AROUND	D	ON	D	ON	ON

TABLE 5.2 (a)

	INPUTS					OUTPUTS	
X.21 STATE	C	RXD	CD	CTS	DSR	R	I
1: READY	OFF	1	OFF	OFF	ON	1	OFF
13S:SEND DATA	ON	1	OFF	ON	ON	1	OFF
13R:RECEIVE DATA	OFF	D	ON	OFF	ON	D	ON
13:DATA TRANSFER	ON	D	ON	ON	ON	D	ON
DCE NOT READY	X	X	X	X	OFF	0	OFF
DTE UNC NOT READY	-	-	-	-	-	-	-
TURN-AROUND	ON	1	OFF	OFF	ON	0	OFF

TABLE 5.2 (b)

	INPUTS		OUTPUTS		
X.21 STATE	T	C	TXD	RTS	DTR
1:READY	1	1	1	1	0
13S:SEND DATA	D	0	D	0	0
13R:RECEIVE DATA	1	1	1	1	0
13:DATA TRANSFER	D	0	D	0	0
DCE NOT READY	-	-	-	-	-
DTE UNC. NOT READY	0	1	X	X	1
TURN-AROUND	D	0	D	0	0

TABLE 5.3 (a)

	INPUTS					OUTPUTS	
X.21 STATE	C	RXD	CD	CTS	DSR	R	I
1:READY	1	1	1	1	0	1	1
13S:SEND DATA	0	1	1	0	0	1	1
13R:RECEIVE DATA	1	D	0	1	0	D	0
13:DATA TRANSFER	0	D	0	0	0	D	0
DCE NOT READY	X	X	X	X	1	0	1
DTE UNC.NOT READY	-	-	-	-	-	-	-
TURN-AROUND	0	1	1	1	0	0	1

TABLE 5.3 (b)

NOTE: ON = 0 and OFF = 1 for control circuits

Tables 5.3 (a) and (b) contain the same information as tables 5.2 (a) and (b), but in the form used to derive the boolean expressions on which figure 14 is based. These expressions (in their simplest form) are as follows:-

table 5.3 (a)

$$\begin{aligned} TXD &= T; \\ RTS &= C; \\ DTR &= \overline{T}.C = \overline{T + \overline{C}}; \end{aligned}$$

table 5.3 (b)

$$R = \overline{DSR}.RXD.(\overline{CTS + C} + CTS.C); \quad \text{and}$$
$$I = RXD.CD.CTS.\overline{DSR} + DSR$$

Combining the above five expressions gives rise to the circuit of figure 14. The V.24 signal TSET may be directly connected to the X.21 signal S (after matching electrical characteristics) to provide timing information for the X.21 DTE. (See figure 19).

5.3 V.24 DTE TO X.21 DCE TRANSLATION

5.3.1 METHOD

Interface translation between a V.24 DTE and a X.21 DCE falls into two classes, depending on whether dedicated circuits or switched circuits are used. With dedicated circuits, the X.21 interface always operates within the physical layer and translation between V.24 and X.21 is straightforward. An interface adaptor consisting of logical connections may be used and is described later in this chapter.

Translation between V.24 and X.21 for the X.21 switched service is more complex because the translation process must interact with the X.21 DCE on the network layer. This leads to the translator outlined in section 5.1.2, which was developed on an evaluation system. The system console was used as operator interface, allowing X.21 selection signals to be generated and DCE provided information to be displayed. Hardware was built to allow the evaluation system access to the V.24 and X.21 interfaces. Software was developed to implement the translation process.

The possibility of direct DTE/translator communication (eliminating the operator/translator interface) initially appeared attractive. However, this would have required the translator to be compatible with a multitude of higher level protocols (such as SDLC, BSC, HDLC, BDLC, etc) to make it suitable for general application.

Achieving such a level of compatibility seemed beyond the scope of this thesis.

The V.24 interface between the translator and DTE was implemented by using the same interface signals as would be used on a V.24 DTE/DCE interface for a dedicated circuit. This was done because the idle condition on such an interface has the DTE signalling DTR ON with the DCE response of DSR ON. This condition corresponds to the X.21 READY state (X.21 state 1) where both sides of the X.21 interface signal READY. Apart from this advantage, using the dedicated circuit interface allows the translator to implement automatic call answering. Software was written to make the translator appear as a V.24 DCE to the terminal.

Whereas the V.24 interface operates within the physical layer only, the X.21 interface covers the physical,link and network layers. The X.21 interface was implemented by writing software to make the translator appear as a X.21 terminal to the X.21 network. The network and link layer functions required by the X.21 interface were provided by the translator itself, in conjunction with the operator interface.

The software developed for the translator results in the following process taking place. During the X.21 quiescent phase, which falls within the physical layer, conditions on the V.24 interface are translated to equivalent conditions on the X.21 interface, and vice versa.

During the X.21 call control phase, which incorporates link and network layer features, the translator interacts with the operator when necessary, via the system console, to implement X.21 procedures such as generating selection signals.

When the data transfer phase is reached, logical connections are established between V.24 circuit TXD (103) and X.21 circuit T, as well as X.21 circuit R and V.24 circuit RXD (104). Link and network layer features fall away while data transfer between the V.24 DTE and X.21 DCE takes place. The translator monitors the interfaces and implements line turn-around when required for half duplex V.24 equipment. When necessary, the translator carries out X.21 call clearing procedures and brings the interfaces back to the quiescent phase.

The major software task is the implementation of the X.21 interface. The V.24 interface is straightforward to implement. Figure 15 shows the translator and the two interfaces in terms of the OSI model.

When deciding on the actual software structure, two popular approaches to implementing interfaces defined by state diagrams are encountered. The first approach involves tabulating all the valid interstate transitions and writing corresponding routines to cope with each transition. The interface is monitored to determine the current state. When a transition between states is detected, it is identified by comparing it to the entries in the transition table. The appropriate transition routine is then executed. This approach is best suited to situations where the next state is likely to be any one of a number of possible states. For instance, if the interface is in the X.21 READY state, the next state could be any one of six possibilities (states 14, 18, 24, 2, 8 or 15 of figures 2(b) and 3). The likelyhood of any one of these states occurring rather than another, varies according to factors outside the designer's control. (Such factors include the volume of traffic across the interface, the reliability of the DTE and DCE, and the amount of time the DTE is used offline). This situation is conveniently handled with the Pascal construct <u>case</u> ..... <u>of</u>, as follows:

```
case next state of
    state 14:  ......... ;
    state 18:  ......... ;
    state 24:  ......... ;
    state  2:  ......... ;
    state  8:  ......... ;
    state 15:  ......... ;
end
```

The second approach is best suited to situations where it is known with a reasonable degree of certainty what the next state is going to be. When a transition to a new state is detected, the new state is compared to the expected one and appropriate action is taken. This action will involve the execution either of the appropriate transition routine, or of an error routine. As an example, if the current state is the X.21 CALL REQUEST STATE (state 2 of figure 3), the next expected state is PROCEED TO SELECT. If the DCE does not respond with this signal within a predetermined time, the X.21 DTE must execute an error routine after the CALL REQUEST state, rather than generating selection signals.

As suggested by the above examples, both approaches have been used in writing software for the translator. The X.21 quiescent phase of figure 2(b) (which falls within the physical layer), is best handled using the first approach, while the call control phase of figures 3 and 4 is best handled by the second.

Generating software which implements the X.21 state diagrams accurately may be done using an approach suggested by West and Zafiropulo (15). The X.21 state diagrams used to define the protocol are split into two sections, one for the DTE and one for the DCE. These sections now define the behaviour of each side of the interface as a finite state machine.

The signals defining each finite state machine are grouped into inputs and outputs. The FSM behaviour is then described in terms of sending its outputs and receiving its inputs. Figure 16 shows how the DTE behaviour is derived during the X.21 quiescent phase. The writing next to each transition in this figure denotes the action which must be taken by the DTE for the interface to behave according to the X.21 definition. The letters S and R denote send and receive (output and input) sets for the DTE, referring to the signals on (T,C) and (R,I) respectively. Figure 17 shows the behaviour of the X.21 DTE during the quiescent and call establishment phases, and is used in writing translator software.

It is a fairly straightforward exercise to generate software from the above diagrams, provided that a block structured language such as Pascal is used.

During the X.21 call control phase, the X.21 network sees the translator as a sequential logic system with each state influencing the next, as it emulates a X.21 DTE. This is the translator's only task during the call control phase, the V.24 interface being held static pending call establishment. It is therefore necessary to treat the translator as a finite state machine, with its inputs and outputs grouped separately. This makes it easy to implement the X.21 interface using the send and receive pairs mentioned earlier.

During the quiescent phase there is a one to one mapping between X.21 and V.24 states, as only physical layer procedures are involved. The problem of translating between the X.21 and V.24 interfaces could be solved by using combinational logic implemented either in software or hardware. Alternatively, the FSM approach used for the call control phase could be extended to cover the quiescent phase as well. This would result in the translator's input and output sets being composed of elements from both interfaces. The hardware configuration decided on for the translator, described in section 5.3.4.1, favours the adoption of the FSM approach. This has proved convenient to implement, as the translator's entire operation is covered by the realisation of one FSM.

The state machine approach to quiescent phase translation results in the state diagram of figure 18, where the translator is defined as a FSM with:

input set : IS = (TXD, RTS, DTR, R,I); and
output set: OS = (RXD, CD, CTS, DSR, T, C)

Figure 18 shows the set of possible states with legitimate inter-state transitions for translation during the quiescent phase.

During the X.21 call control phase, the V.24 interface remains static (DTR and DSR both at binary 1) until data transfer. The X.21 state diagrams of figure 17 describe translator behaviour during the call control phase, as it is essentially a X.21 DTE for this period.

5.3.2 AREAS REQUIRING CAUTION

5.3.2.1 COLLISIONS

West and Zafiropulo's work on automated validation of the X.21 protocol (15) reveals a number of interesting facts about collisions on the interface. Although their work was based on the 1976 revision of X.21 and the weaknesses they discovered have largely been attended to in the 1980 version, many of the points they raise are still relevant to the design of X.21 equipment. Some of these are mentioned below.

i) The state diagrams derived for a X.21 DTE or DCE by using send and receive pairs should consist of the same states and transitions as the definitive diagram from which they were derived. This was found to allow an undesirable transition in the DTE state diagram, namely that from INCOMING CALL (state 8 of figure 3) to CALL COLLISION (state 15). This transition implies that the DTE may signal a call request after receiving the DCE signal INCOMING CALL. This is obviously not the intention of the X.21 protocol designers, as is mentioned in the 1980 revision of X.21. For this reason the transition in question does not appear in figure 17. The X.21 recommendation still has grey areas in this regard, as it contains a table of valid DTE interstate transitions which permits the transition from state 8 to state 15. When reading the state diagram of figure 3 (which forms the formal definition of the X.21 call control phase) it is by no means obvious that the transition in question is usually illegal.

(The difficulty in defining this particular area of X.21 arises from the use of the interface machine as a conceptual tool. Danthine (9) notes that the interface machine should be restricted to the use of half duplex

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procedures. Half duplex in this context means that actions on either side of the X.21 interface must follow on each other in two-way alternate action-reaction sequences. Collisions are an obvious contravention of this rule, in that both sides of the interface act simultaneously. The interface machine concept is not suitable for defining the behaviour of the interface under these conditions. West and Zafiropulo's suggestion of defining X.21 in terms of separate DTE and DCE state diagrams makes good sense in this context).

ii) Other possible collisions occur when the DTE makes a transition from the READY state to UNCONTROLLED NOT READY simultaneously with the DCE signalling INCOMING CALL, or when the DCE makes a transition from READY to NOT READY simultaneously with a DTE CALL REQUEST. In both cases the transition to NOT READY will be misinterpreted as intention to clear the call, and a clearing sequence will be initiated. In the latter case the DTE will respond with CLEAR CONFIRMATION and wait for the DCE to respond with READY, which it is unlikely to do. This deadlock should be satisfactorily resolved by the expiration of DTE time-limit T6, which results in the DTE considering the DCE as NOT READY. Nonetheless, a sequence of events forming part of the normal operation of the X.21 interface can result in an error condition. This possibility could be relevant to DTE design.

iii) Another collision which has potential for causing confusion occurs when the DCE gives a valid response to DTE signals simultaneously with the DTE signalling CLEAR REQUEST. The DCE response would then arrive at the DTE before the DCE CLEAR CONFIRMATION. This eventually could be said to be covered by the (X,X) condition of (r,i) during state 16, but it may not be obvious that (X,X) could also cover changing conditions.

of (r, i). Problems in this respect may be avoided by ensuring that the DTE only responds to the (0,OFF) condition of (r, i).

5.3.2.2 MISCELLANEOUS FACTORS

Various other factors requiring careful treatment may be gleaned from the X.21 text.

i) The DCE is permitted to insert SYN characters at random between DCE PROVIDED INFORMATION characters. This should not interfere with whatever processing the DTE does to DCE provided information.

ii) Some areas of X.21 are left as matters of national option. These include the number of automatic retries permitted per call and the minimum delay permitted between such retries.

iii) Future extensions to X.21 might well include the use of additional IA5 characters, new transitions between states or additional states. This should be borne in mind while designing the DTE.

5.3.2.3 ERROR RECOVERY

So far it has been assumed that the DCE operates without making any errors, according to the X.21 protocol. Any realistic DTE implementation should however take into account the possibility of DCE malfunctions and take adequate precautionary measures where justified. Some of the possible error conditions which might conceivably occur are:

i) the DTE receiving characters other than "+" or "BEL" in these character streams during states 3 or 8;

ii) circuit I going ON at some stage during the call control phase when it is not supposed to; and

iii) DCE provided information being received with format violations.

Any of the following alternatives may be decided on as an adequate precautionary measure:

i) the DTE may ignore the error and rely on the appropriate time-limit to expire and resolve the situation;

ii) the DTE may initiate a clear and retry sequence; or

iii) where appropriate, the DTE may initiate a clearing sequence and then wait until the DCE interface recovers from its error condition before initiating another call.

(For the purpose of implementing a preliminary model of the translator, it was decided to rely on the DTE time-limits to resolve possible error conditions. This would aid in gaining a deeper understanding of the protocol as it would show whether or not the time-limits adequately catered for failures on the interface).

One possible error which is not taken into account by any of the DTE time-limits is also mentioned by Yanoschak. In state 8, DCE INCOMING CALL, the DCE could conceivably transmit a continuous string of "SYN" characters without following these by "BEL". This would effectively hang up the interface without starting any timers to resolve the deadlock. This condition could be catered for by including an extra DTE time-limit with an appropriate error message on its expiration to be started on receipt of a DCE "SYN" character, and stopped on receipt of the first DCE "BEL".

5.3.3 IMPLEMENTATION

5.3.3.1 PHYSICAL LAYER

The physical layer design of the translator is outlined here in terms of mechanical, electrical, functional and procedural characteristics to maintain compatibility with the physical layer descriptions of the X.21 and V.24 protocols in sections 3.3 and 4.3 respectively.

Mechanical Characteristics

The translator's V.24 mechanical interface consists of a 25-pin D-type connector with female contacts, as the translator is a DCE to the V.24 terminal.

The X.21 mechanical interface consists of a 15-pin D-type connector with male contacts, as the translator is a DTE to the X.21 DCE.

Electrical Characteristics

The V.24 electrical characteristics conform to the V.28 recommendation (unbalanced double-current interchange circuits), while the X.21 electrical characteristics conform to X.27 (balanced double-current interchange circuits).

The bit rates are determined by the clock signal generated by the X.21 interface and may vary from 1 200 bits/sec to 9 600 bits/sec.

Functional Characteristics

The V.24 interface generates the DCE signals RXD, CD, CTS, DSR, TSET and RSET, and responds to the DTE signals TXD, RTS and DTR. (See table 4.3).

The X.21 interface generates the DTE signals T and C and responds to the DCE signals R, I and S. (See table 3.3).

Figure 19, giving the relationship between X.21 and V.24 timing information,shows that X.21 circuit S may be used to generate V.24 timing information. In the translator, the V.24 timing signals TSET and RSET are generated by making a logical connection from S.

X.21 circuit G corresponds to the V.24 circuit signal ground (circuit 102). These two circuits should be directly connected.

Procedural Characteristics

The procedural aspects of translation on the physical level cover the following areas:

- the X.21 quiescent phase, which fulfills similar functions to the procedural aspects of V.24;
- the data transfer phase, during which X.21 link and network layer aspects fall away;
- the X.21 call clearing phase, which involves handshaking across the DTE/DCE interface on the physical level; and
- the implementation of dedicated circuit interfaces,which only operate on the physical level.

These four areas are covered below.

i) THE X.21 QUIESCENT PHASE

During this phase, signals on the V.24 interface are converted to equivalent conditions on the X.21 interface and vice versa. The V.24 signals DTR ON and DTR OFF are translated as X.21 conditions DTE READY and DTE UNCONTROLLED NOT READY respectively. The X.21 conditions DCE READY and DCE NOT READY are translated as ON and OFF conditions respectively on V.24 circuit DSR.

The X.21 condition DTE CONTROLLED NOT READY has no equivalent on the V.24 interface and will therefore never be initiated by the V.24 DTE. The translator generates this condition however, while it is receiving selection signals from the operator console.

Applying the above conditions allows the translator's X.21 interface to operate according to the state diagram of figure 2(b) during the X.21 quiescent phase.

The translator's operation is summarised in figure 18, which was used to write the quiescent phase translation software. This figure represents the translator as a FSM, with

input set: IS = (TXD, RTS, DTR, R, I); and
output set: OS = (RXD, CD, CTS, DSR, T, C)

The translator's main software task during the X.21 quiescent phase is to monitor its inputs and generate appropriate output conditions.

The translator's operation during the quiescent phase is summarised in table 5.4 below.

X.21 NETWORK	TRANSLATOR					V.24 TERMINAL			
X.21 DCE	X.21 DTE	V.24 DCE				V.24 DTE			
		RXD	CD	CTS	DSR	TXD	RTS	DTR	
READY	READY	1	OFF	OFF	ON	1	OFF	ON	
NOT READY	READY	1	OFF	OFF	OFF	1	OFF	ON	
READY	UNCONTROLLED NOT READY	1	OFF	OFF	ON	1	OFF	OFF	
NOT READY	UNCONTROLLED NOT READY	1	OFF	OFF	OFF	1	OFF	OFF	
READY	CONTROLLED NOT READY	1	OFF	OFF	ON	1	OFF	ON	
NOT READY	CONTROLLED NOT READY	1	OFF	OFF	OFF	1	OFF	ON	

TABLE 5.4 : QUIESCENT PHASE TRANSLATION

ii) THE DATA TRANSFER PHASE

During the X.21 call control phase, the V.24 interface is held idle, with the translator generating OFF conditions on circuits CTS and CD. Circuit DSR should be ON in response to DTR.

Once the data transfer phase is reached, the network and link layer aspects of X.21 fall away and only a physical level interface exists between DTE and DCE. During data transfer therefore, the translator only operates within the physical layer. For full duplex transmission, ON conditions are signalled on V.24 circuits CD and CTS, while a logical connection is established between X.21 circuit R and V.24 circuit RXD, as well as V.24 circuit TXD and X.21 circuit T. The translator holds X.21 circuit C in the ON condition.

With half duplex transmission, the same connections between TXD and T and RXD and R are made. "Line turn-around" is achieved by switching CTS ON and OFF in response to RTS. CD is always given the opposite condition to CTS. This assumes that the remote terminal also operates in half duplex mode, so that although the translator's X.21 interface remains full duplex, data will never be travelling across the network in both directions at once. This solution avoids problems due to the loosely defined areas of X.21 mentioned in section 3.5.2.2.

iii) CALL CLEARING

The translator continuously monitors the X.21 interface, looking for a DCE CLEAR INDICATION. When this occurs, the translator disconnects circuit TXD from T and R from RXD, and puts OFF conditions on V.24 circuits CTS and CD. DSR is set to either ON or OFF depending on the condition of DTR, and the X.21 interface is moved through the call clearing procedure of figure 4.

A similar sequence of actions is followed when the operator initiates a DTE CLEAR REQUEST on the X.21 interface via his console, or if the V.24 signal DTR goes OFF as would happen if the DTE were powered down, or under certain fault conditions.

iv) DEDICATED CIRCUITS

When only a dedicated circuit is required by a V.24 terminal on a X.21 network, the X.21 interface is constrained to functioning as in figure 6, and only operates in the physical layer. Because the V.24 interface also only operates in the physical layer, an interface adaptor similar to the one developed in section 5.2 may be used. The equivalence between X.21 and V.24 states shown in table 5.1 is also valid for this adaptor, and may be used to draw up truth tables from which the circuit for the adaptor can be derived. Table 5.5, below, is based on table 5.1 and shows the relationship between the X.21 and V.24 interfaces. This is a simpler case than the one in section 5.2, in that no allowance need be made for the time taken by line turn-around with half duplex working, as the X.21 interface is associated with a full duplex circuit. The V.24 circuit RTS may be looped back to CTS inside the adaptor to give the necessary response to the V.24 terminal, so that the expression CTS = RTS holds true.

	INPUTS			OUTPUTS	
X.21 STATE	TXD	RTS	DTR	T	C
1 : READY	1	1	0	1	1
13S: SEND DATA	D	0	0	D	0
13R: RECEIVE DATA	1	1	0	1	1
13: DATA TRANSFER	D	0	0	D	0
DCE NOT READY	–	–	–	–	–
DTE UNC. NOT READY	X	X	1	0	1

TABLE 5.5 (a)

	INPUTS		OUTPUTS		
X.21 STATE	R	I	RXD	CD	DSR
1: READY	1	1	1	1	0
13S: SEND DATA	1	1	1	1	0
13R: RECEIVE DATA	D	0	D	0	0
13: DATA TRANSFER	D	0	D	0	0
DCE NOT READY	0	1	X	X	1
DTE UNC. NOT READY	-	-	-	-	-

TABLE 5.5 (b)

NOTE : 1) CTS = RTS
2) ON = 0 and OFF = 1 for control circuits.

Tables 5.5 (a) and (b) produce the following boolean expressions:

$T = TXD.\overline{DTR}$
$C = RTS.\ \overline{DTR} + DTR$

$RXD = R$
$CD = I$
$DSR = \overline{R}.I$

Combining these expressions results in the circuit of figure 20 : an adaptor which allows a V.24 terminal to use a X.21 dedicated circuit interface.

5.3.3.2 LINK LAYER

The V.24 interface being a physical layer interface only is not involved in link layer procedures. The link layer is based on synchronous data transmission across the X.21 interface, using seven-bit IA5 characters. An eighth bit is used as a parity bit to allow error checking. Odd parity is supported.

The link layer comes into effect during the X.21 states PROCEED TO SELECT and INCOMING CALL (states 3 and 8 of figure 3), both of which herald the start of DCE involvement in the call control phase. The X.21 protocol requires the DCE to preceed the IA5 characters "+" and "BEL" in states 3 and 8 of figure 3 with a minimum of two synchronisation characters. The IA5 character "SYN" is used. Further character transmission from both sides of the interface should fall within the character boundaries indicated by the DCE.

Whereas some administrations allow character synchronisation between DTE and DCE to be based on the X.21 circuit B (see section 3.3.3), this is not mandatory with X.21 and is therefore not used in the translator.

The translator hardware has been designed so that it can be programmed to support the X.21 link layer features outlined above.

5.3.3.3 NETWORK LAYER IMPLEMENTATION

Exit from the quiescent phase on the X.21 interface is to the call control phase via the READY state, and may be due to either an incoming call or an operator (DTE) call request. Return to the quiescent phase is only via the call clearing phase.

For the duration of the call control phase, the DTE time-limits of Appendix E are in operation. Appropriate action is taken on their expiry.

Call Request

From the time a call request is initiated until the X.21 interface reaches state 12, READY FOR DATA, the V.24 interface is kept inactive by translator signals DSR ON and CTS and CD OFF.

A call request may be initiated via the operator interface, and should be preceded by interaction with the operator to obtain the selection signals required during X.21 state 4. (During the course of this interaction in the quiescent phase, the translator presents the DCE with the DTE CONTROLLED NOT READY signal). The translator indicates CALL REQUEST by signalling (t, c = 0,ON) and waits for the DCE to respond with (r, i = +, OFF). (The "+" transmission will be preceded by at least two "SYN" characters, which will be used by the translator on the link layer to get "in step" with DCE characters). The translator now responds with the selection signals of state 4, which are preceded by synchronisation characters. If the operator has specified direct calling, state 4 is bypassed and the translator signals DTE WAITING (1, ON). The translator now waits for the DCE to signal READY FOR DATA (1, ON). All relevant DCE provided information which may precede this state is displayed on the operator console. When required to, the translator will take appropriate action (such as clearing a call) on receiving call progress signals.

Incoming Call

The translator detects the "SYN" characters preceding the DCE signal INCOMING CALL (BEL, OFF) and then waits until it detects "BEL" before signalling CALL ACCEPTED (1, ON). It waits for the DCE to signal READY

FOR DATA (1, ON), while displaying all relevant DCE provided information on the console. As before, the translator will take appropriate action on receiving call progress signals.

Until the translator detects the READY FOR DATA signal, it signals DSR ON, CTS and CD OFF to the V.24 DTE.

The events initiated by either a call request or an incoming call usually result in the data transfer phase, during which the link and network layer aspects of X.21 fall away. The data transfer phase is not entered if call progress signals indicate that clearing should take place, or if call clearing follows in the normal course of events, such as when the DCE initiates an incoming call to provide charge advice.

At any stage during the call control phase, the interface may be returned to the quiescent phase by entering the call clearing procedure described in section 5.3.3.1 (iii).

5.3.4 THE PRELIMINARY MODEL

5.3.4.1 HARDWARE

The hardware developed for the preliminary model consists of a wire-wrapped card which is connected to the motherboard of the SABUS computer used as an evaluation system. The circuitry is shown in block diagram form in figure 21. The hardware presents a DCE interface to the V.24 DTE and a X.21 DTE interface to the DCE. The main hardware components are two parallel ports, a USRT (universal synchronous receiver/transmitter) and two timers. These devices are addressed from the system address bus after address decoding has been done. Some miscellaneous hardware devices (such as multiplexors) are used to implement functions specific to the translator. Line driver and receiver circuits are used to implement the electrical characteristics specified for the two interfaces.

Parallel Ports

These ports, one for input and one for output, are used to detect and present conditions on the two interfaces simultaneously. The ports convey this information to and from the system data bus. The output port is clocked using the X.21 signal S, so that changes on circuits T and C occur on bit boundaries as specified by the X.21 recommendation.

Bits 6 and 5 of the output port are used to control a 4-line to 1-line multiplexor. This multiplexor presents one out of four input signals on X.21 circuit T, depending on the condition of its two control inputs. The four multiplexor inputs are the USRT transmitter data output, the V.24 signal TXD, an alternate sequence of ones and zeros (obtained by halving the frequency of S), and bit 4 of the output port, which may be either logic one or zero and is set under programme control.

Bit 3 of the output port is used to generate the condition on X.21 circuit C.

Bits 2,1 and 0 of the output port are used to generate the conditions on V.24 circuits CD, CTS and DSR respectively. The condition of CD is also used to control a 2-line to 1-line multiplexor which has as its output the V.24 circuit RXD. The two inputs are the X.21 circuit R and a steady binary 1. (V.24 states that RXD should be at binary 1 while CD is OFF).

Bits 3 to 0 of the parallel input port are used to sample X.21 circuits R and I and V.24 circuits RTS and DTR respectively.

Universal Synchronous Receiver Transmitter

The USRT is also clocked by the X.21 signal S. It receives data from X.21 circuit R, presenting it to the data bus, and transmits data from the data bus to the 4-line to 1-line multiplexor for presentation on X.21 circuit T. The USRT is used for link level functions such as detecting and generating synchronisation characters and detecting parity errors in received data. It also generates a parity bit on data transmitted to the DCE.

Timers

Two timers are used. The first is used in conjunction with the "clear detector" of figure 21 to detect a valid DCE CLEAR INDICATION on X.21 circuits R and I. The second is used for the implementation of the X.21 time-limits of Appendix E. The counters produce an output after counting a value previously loaded from the system data bus down to zero. These outputs are tied to two of the evaluation system's CPU interrupt lines.

The Clear Detector

The criterion for a valid DCE CLEAR INDICATION is that it should last for a minimum of 16 bit-periods and its duration should be at least 10 mSec. Over the translator's operational range (1 200 b/sec, 2 400 b/sec, 4 800 b/sec and 9 600 b/sec), the 16-bit period lasts from 13,3 m Sec to 1,7 m Sec. It is only at 1 200 b/sec that the 16-bit period exceeds the 10 m Sec criterion which would apply when detecting a valid DCE CLEAR INDICATION. On the preliminary model it was found convenient to apply a single criterion of 15 mSec before accepting a DCE CLEAR INDICATION as valid. This is an arbitrary value chosen to satisfy all bitrates in the translator's operational range. As X.21 only specifies a lower limit of 10 mSec and no upper limit, the 15 mSec period is not in conflict with the recommendation.

The clear detector detects the (0,OFF) condition on X.21 circuits R and I and starts a downcount on timer TA, which has been pre-loaded with a value corresponding to 15 mSec. Should the (0,OFF) condition change before the 15 mSec period expires, the down-count stops and the timer reverts to its original count value without CPU intervention. If terminal count is reached, timer TA generates an interrupt which is serviced by the system's CPU.

As a DCE CLEAR INDICATION may occur at any stage outside the X.21 quiescent phase and must last for a set time-limit, it is much easier to implement the timer in hardware than in software.

DTE clearing is also catered for, by allowing an ON to OFF transition of the V.24 signal DTR to trigger the same interrupt used by the DCE clear detector. On receiving the interrupt, the CPU should interrogate the parallel input port to see whether the DTE or DCE initiated clearing.

The "Steady Binary" Convertor

The steady binary convertor has as its inputs the X.21 signals R, I and S. It monitors the conditions of R and I and regenerates these same conditions as outputs, provided they have remained steady for 16 periods of S. This ensures that the values of R and I read by the CPU from the parallel input port are steady. In the event of the convertor being presented with a continuously varying input (as when there is a data signal on R), the last steady binary value is latched on the corresponding output.

Implementation of X.21 Time-Limits

The X.21 DTE time-limits of appendix E could conceivably be implemented either in hardware or in software, but the hardware implementation is far more convenient. As justification for this, the example of implementing X.21 DTE time-limit T2 may be used. T2 is a 20 second time-limit which is started in the X.21 state DTE WAITING (state 5 of figure 3). It may be stopped after the DTE receives call progress signals resulting in the call being cleared, or if the DTE receives a DCE CLEAR INDICATION, or if the interface moves through to the READY FOR DATA condition (state 12 of figure 3). Before this time-limit is terminated, the translator could be required to process several interstate transitions. Implementing the down-count of a software timer while this is being done, would be a tedious process. Using a hardware timer simplifies matters considerably, as instructions equivalent to "start timer" and "stop timer" can be used where appropriate, while the down-count is performed by an external clock.

Address Decoding

Signals on the system address bus, in conjunction with conditions on the

I/O read and write lines, are decoded to address the above devices as required by the translator software.

Line Drivers and Receivers

Two classes of drivers and receivers are used. One implements X.27 electrical characteristics for the X.21 interface, while the other implements V.28 characteristics for the V.24 interface.

X.21 circuits T and C are presented to a 15-pin D-type connector by the X.27 line drivers, while X.21 circuits S, R and I are taken from this connector as inputs for the X.27 line receivers. These drivers and receivers convert between TTL voltage levels and X.27 line signals.

In similar fashion, the V.28 line drivers present V.24 signals RXD, CD, CTS, DSR, TSET and RSET to the V.24 25-pin D-type connector, while receiving signals TXD, RTS and DTR.

General

On the V.24 interface, circuits TSET and RSET are derived directly from X.21 circuit S, while the V.24 signal ground (circuit 102) is tied to the translator hardware's circuit ground. As S is also used to clock the USRT and the parallel output port, the translator may be used at any clock rate presented on S, without requiring any adjustment.

Operation

During the X.21 quiescent phase, the USRT and timers are not used. Bits 6 and 5 of the parallel output port are set so that bits 4 and 3 control the conditions of X.21 circuits T and C respectively. Bits 2 to 0 control the conditions of V.24 circuits CD, CTS and DSR respectively, while bit 2 (CD) also controls V.24 circuit RXD, as explained under the subheading "parallel ports" earlier in this section. The signals connected to bits 3 to 0 of the parallel input port(CR, I, RTS and DTR respectively) are inputs to the translator from both interfaces. These inputs are monitored and used to determine what conditions should be presented on bits 4 to 0 of the output port. This hardware configuration allows the FSM of figure 18 to be implemented.

While selection signals are being entered from the operator's console, the "01" condition is generated on X.21 circuit T by an appropriate setting of bits 6 and 5 of the parallel output port, allowing the condition DTE CONTROLLED NOT READY to be implemented.

During X.21 call setup, bits 6 and 5 of the parallel output port are set so that the USRT may be used to generate IA5 characters on circuit T. The USRT also presents IA5 characters received on X.21 circuit R to the system data bus.

Timers TA and TB come into operation as soon as the X.21 quiescent phase is left, being used to detect the DCE CLEAR INDICATION and implement X.21 DTE time-limits.

During the data transfer phase, bits 6 and 5 of the parallel output port are set so that V.24 circuit TXD is connected to X.21 circuit T. X.21 circuit R is connected to V.24 circuit RXD by setting bit 2 of the parallel output port ON, which simultaneously puts an ON condition onto V.24 circuit CD. This is valid for implementing full duplex transmission. The conditions on bits 2 to 0 may also be used to implement half duplex transmission as described in section 5.3.3.1 (ii).

5.3.4.2 SOFTWARE

In implementing the translation process along the lines described in section 5.3.3, software functions may also be divided into the physical, link and network layers. In section 5.3.3 the physical layer aspects of translation were grouped into four categories, namely the X.21 quiescent phase, the data transfer phase, the call clearing procedure and the case of dedicated circuits. The case of dedicated circuits has been treated in section 5.3.3.1, where the interface adaptor of figure 20 is used to perform the translation. It is convenient to group the data transfer phase software with that of the network layer, as it follows on naturally from the call control phase. The call clearing procedure is also grouped with network layer software, as it is invoked only from the call control and data transfer phases. The X.21 quiescent phase is therefore the only aspect of translation treated directly under the physical level.

The link layer features of character format, synchronisation and error detection are provided by the USRT described in the previous section. Related software is concerned with initialising the USRT to provide the necessary features and, if required, interrogating it to determine the validity of incoming data.

On the network layer, translator software must implement the X.21 call control phase, culminating in data transfer unless the call clearing procedure is invoked during call establishment. The call control phase is naturally divided into a call request procedure and an incoming call procedure. Network layer software serves to make the translator emulate a X.21 DTE during call control, while presenting the V.24 DTE with an ON signal on DSR and OFF signals on both CTS and CD. Interaction with an operator (via the console) is required to generate selection signals for use while implementing a X.21 call request. The translator achieves automatic answering of calls when the DCE indicates an incoming call on the X.21 interface.

To support the main software tasks mentioned so far, several auxiliary routines are required. These include procedures to start and stop X.21 DTE time-limits, and a procedure to display messages reflecting the status of the interfaces on the console.

a) The Physical Layer

The nature of circuit switched traffic is such that the DTE/DCE interface will spend most time in the quiescent phase. The translator software (<u>programme</u> translator) has been developed along similar lines, with the basic function being translation during the X.21 quiescent phase. Exit from the quiescent phase may be made to the call control phase, during the X.21 READY state.

The basic hardware unit used during quiescent phase translation is the parallel I/O section of figure 21, explained in section 5.3.4.1. The input port is used to determine the status of the V.24 DTE (bits 0 and 1) and the X.21 DCE (bits 2 and 3). Using FSM terminology, this port monitors the translator's input set. Depending on the value of the input set (IS), translator software will determine an appropriate output set (OS) and write this to the output port. Bits 0, 1 and 2 of the output port control the V.24 interface and bits 3 to 6 the X.21 interface.

Table 5.6 (below) based on table 5.4 and the state diagram of figure 18, lists the mnemonics used to represent different conditions of IS and the corresponding desired value of OS as implemented by <u>programme</u> translator. The numbers in these mnemonics and in figure 18 refer to the corresponding states of the X.21 interface. The only output set

EQUIPMENT STATE		INPUT SET (IS)		CORRESPONDING OUTPUT SET (OS)	
V.24 DTE	X.21 DCE	RTS,DTR,R,I	MNEMONIC	CD, CTS, DSR, T, C	MNEMONIC
READY	READY	OFF ON 1 OFF	IS1	OFF OFF ON 1 OFF	OS1
READY	NOT READY	OFF ON 0 OFF	IS18	OFF OFF OFF 1 OFF	OS18
NOT READY	READY	OFF OFF 1 OFF	IS24	OFF OFF ON 0 OFF	OS24
NOT READY	NOT READY	OFF OFF 0 OFF	IS22	OFF OFF OFF 0 OFF	OS22
REQUEST TO SEND (1)	READY	ON ON 1 OFF	IS2	OFF OFF ON 01 OFF	OS14[2]
UNDEFINED		- - - -	-	OFF OFF OFF 0 OFF	OS22

NOTES:

1) Only when the translator interacts with the console to receive X.21 selection signals.

2) The V.24 signals CD, CTS and DSR in this output set reflect the condition of the X.21 DCE before this state was assumed, and persist for the duration of procedure selsigs.

TABLE 5.6

which is generated as a result of factors other than the input set is OS 14, corresponding to DTE CONTROLLED NOT READY on the X.21 interface. This condition is generated by the translator while selection signals are being received from the console, as is explained later in this section.

In the event of the input set not corresponding to any of the first four possibilities reflected in table 5.6, an unidentified quiescent state is detected and the translator indicates NOT READY to both interfaces. If the X.21 DCE is in the call control or data transfer phase at this point, as could happen if the translator were reset during call control or data transfer, the translator signal will be interpreted by the network as a DTE CLEAR REQUEST and the DCE will respond with a DCE CLEAR CONFIRMATION in accordance with the state diagram of figure 4.

The translator continues to transmit NOT READY to both interfaces until the DCE signals READY. When this happens, normal operation is resumed and the translator converts conditions on one interface to appropriate conditions on the other. When the X.21 interface is in state 1 again (DTE, DCE READY), the interrupted call may be re-established.

While executing the "undefined input set" procedure, the V.24 DTE is presented with the true state of the X.21 DCE, while the X.21 DCE is presented with the condition DTE NOT READY regardless of the DTE condition. This has no adverse effect on the interfaces as it results from a correct implementation of the X.21 call clearing procedure.

If the unidentified state is due to the DTE or to persistant fault conditions, the translator's NOT READY signals to both interfaces will continue until the fault is cleared.

When the DTE signals ON on V.24 circuit DTR and the DCE signals READY, translator software tests for the presence of an incoming call or a call request. Either possibility results in exit from the quiescent phase to the call control phase.

An incoming call is detected by the USRT when it receives two or more contiguous SYN characters from the DCE. Translator software interrogates the USRT and on finding that SYN characters have been detected, sets a boolean variable (INCOM). If no SYN characters have been detected, the variable is reset. The value of INCOM is used to determine whether an incoming call should be serviced during the READY state.

If the DTE signals ON on RTS during the X.21 READY state (IS 2), the translator enters a procedure to receive selection signals from the console (<u>procedure</u> selsigs). These signals are echoed to the console and stored in a buffer area of memory called SELBUF for use during X.21 call establishment (state 4 of figure 3 : SELECTION SIGNALS). During the execution of <u>procedure</u> selsigs, the translator generates the DTE CONTROLLED NOT READY condition on the X.21 interface (OS14).

If a "#" is typed at any stage during selsigs, the boolean variable ABORT is set to true and the procedure terminated. When ABORT is true, translator software ignores the contents of SELBUF and <u>procedure</u> selsigs may be re-entered. This allows the operator to correct incorrect selection signals inadvertantly entered.

The format of selection signals must be as in appendix B, the sequence being terminated with a "+". If the first character is a "+", <u>procedure</u> selsigs is terminated and the boolean variable DIRECT set to true, indicating that the translator should implement a direct call rather than generating selection signals during call establishment. If a " - " is encountered during the selection sequence (see appendix B), the selection signals are scanned to see if they contain a request for the charge information facility. If the corresponding code is found, the boolean variable CHARGEINF is set to true. (If CHARGEINF is true, time-limit T7 is set during call clearing. The DCE must then respond with the required charge information before this time-limit expires). If the conditions for ABORT, DIRECT and CHARGEINF to be set to true are not met, these variables are set to false when procedure selsigs is terminated. If ABORT is false when procedure selsigs is terminated, the translator initiates a call request if both DTE and DCE are READY. (This is explained in greater detail under network layer software).

A description of procedure selsigs using a mixture of English and Pascal constructs is given below.

```
procedure selsigs;

const
         lim = predetermined value;
         true = 1;
         false = 0;

type
         osvalue = as in table 5.6;
         boolean = false..true;
         character = IA5;

var
         OS : osvalue;
         selbuf: array (0..lim) of character;
         abort, direct, chargeinf : boolean;

begin    timestart (T sigs);
         OS : = OS14
         message : = "SELECTION SIGNALS";
         chargeinf, abort, direct : = false;
         read first console character;
         store character in selbuf;
         write character back to console;
         if character = "#" then
            begin
               abort : = true;
               message : = "ABORTED";
            end
```

```
else
   begin
      if  character = '+' then
          begin  direct : = true;
                 message : = "DIRECT CALL";
                 end
          else
                 begin
                    repeat
                       read next console character;
                       store in selbuf;
                       write character back to console,
                    until character = "#" or "+";
                    if  last character = "#" then
                        begin
                           abort : = true
                           message : = "ABORTED";
                        end
                    else
                        begin
                           scan selbuf for "-";
                           if "-" is found then
                              begin
                                scan preceding
                                characters for
                                "61" code;
                                if "61" found then
                                   begin
                                     chargeinf : = true;
                                   end
                              end
                        end
                 end
      end

end.  timestop;
```

If the boolean variable RETRY is found set during the READY state, the call request procedure is executed immediately and the selection signals from the last call attempt re-used. RETRY is set after group 2 or group 6 call progress signals (see appendix C) are received by the translator during call establishment. After receiving these call progress signals a X.21 DTE is expected to clear the call and make another attempt after waiting for a period defined on a national basis.

Potential problems due to call collisions (state 15 of figure 3) are avoided by examining the status of RETRY and RTS before that of INCOM. This results in the DTE being given preference in the event of a call collision taking place.

The functions outlined so far are summarised below, using a mixture of Pascal constructs and English. The mnemonics for input and output sets are from table 5.2. The statement "message" calls a routine to write the appropriate message to the console.

```
     programme translator;

     const      false = 0;
                true  = 1;

     type       boolean = false .. true;
                isvalue, osvalue = as in table 5.6;

     var        incom, retry : boolean;
                IS : isvalue;
                OS : osvalue;
     label      start;
     begin
start: repeat

          incom : = false;
          interrogate USRT;
          if SYN characters received then
            begin incom : = true end;
          read input set (IS);
          case IS of
            IS1 : OS : = OS1;
                  message : = "DTE READY, DCE READY";
                  if retry : = true then
                     begin execute call request end;
                  else
                     begin
                        if RTS = ON then
                          begin
                             service console; (procedure selsigs)
                             execute call request;
                          end
                        else
                          begin
                             if incom = true then
                               begin
                                 service incoming call;
                               end
                          end
                     end
```

```
            IS18:   OS : = OS18;
                    message : = "DTE READY, DCE NOT READY";

            IS24:   OS : = OS24;
                    message : = "DTE NOT READY, DCE READY";

            IS22:   OS : = OS22;
                    message : = "DTE NOT READY, DCE NOT READY";

            unde-
            fined:  OS : = OS22;
                    message : ="undefined quiescent state";
                    repeat    read IS  until IS = IS1 or = IS 24;
          end

    until forever

end
```

b) The Link Layer

Translator software functions for X.21 link layer implementation consist of correct USRT initialisation.

The USRT is initialised to transmit and receive characters consisting of seven data bits plus one parity bit. Odd parity is used.

The USRT indicates the occurrence of parity errors in data received from the DCE during call establishment, making this information available to translator software on a character by character basis.

The USRT is programmed with IA5 character 1/16 (SYN) as synchronisation character. To comply with X.21 requirements, two contiguous SYN characters are specified. (See section 3.4.1).

c) The Network Layer

Translator software implementing X.21 network layer functions is divided into three main routines. The call request procedure covers implementation of X.21 states 2, 3, 4 and 5 of figure 3 : CALL REQUEST, PROCEED TO SELECT, SELECTION SIGNALS and DTE WAITING.

The incoming call procedure covers X.21 states 8 and 9 of figure 3: INCOMING CALL and CALL ACCEPTED. X.21 states 6 to 13 (excluding states 8 and 9) are covered by a single procedure which follows from the call request and incoming call procedures and leads up to data transfer. This has been called the character identification routine, as its primary function is to identify characters transmitted by the DCE and take appropriate action.

Table 5.7, which lists the mnemonics used for the input and output sets in these routines, should be used in conjunction with the explanation which follows.

In the following programme descriptions, X.21 time-limits are started by calling a procedure named timestart, and stopped by one named timestop. In the Pascal/English notation used, the specific time-limit started follows the call on timestart in parentheses. For example, "timestart (T 7)" loads the value corresponding to time-limit T7 into the time-limit timer and starts a down-count. "Timestop" stops the downcount. These procedures are explained in greater detail in section 5.3.4.2 (c)(v).

(i) The call request routine (<u>procedure</u> calreq).

<u>Procedure</u> calreq uses information generated by the selection signal routine (<u>procedure</u> selsigs) while implementing a X.21 call request. The procedure first signals CALL REQUEST on the X.21 interface (OS2) and then waits for the DCE to respond with PROCEED TO SELECT (IS3). If the boolean variable DIRECT is false, the selection signals contained in SELBUF are transmitted to the DCE (OS4). This is followed by signalling DTE WAITING. If DIRECT is true, the procedure signals DTE WAITING (OS5) immediately after the DCE signals PROCEED TO SELECT, effectively bypassing state 4 of figure 3.

EQUIPMENT STATE		INPUT SET (IS)		CORRESPONDING OUTPUT SET (OS)	
V.24 DTE	X.21 DCE	RTS, DTR, R, I	MNEMONIC	CD, CTS, DSR, T, C	MNEMONIC
Request To Send(1)	Ready	On On 1 Off	IS2	Off Off On 0 On	OS2
"	Proceed To Select	On On + Off	IS3	Off Off On IA5 On	OS4
"	"	On On + Off	IS3	Off Off On 1 On	OS5
"	DCE Waiting	On On SYN Off	IS6A	Off Off On 1 On	OS5
"	DCE Provi- ded Information	On On IA5 Off	IS7/10	Off Off On 1 On	OS5
"	Connection in Progress	On On 1 Off	IS11CR	Off Off On 1 On	OS5
"	Ready for Data	On On 1 On	IS12CR	On On On 1 On	OS12CR[2]
Ready	Incoming Call[3]	Off On BEL Off	IS8	On Off On 1 On	OS9
"	DCE Waiting	Off On SYN Off	IS6B	On Off On 1 On	OS9
"	Connection in Progress	Off On 1 Off	IS11IC	On Off On 1 On	OS9
"	Ready for Data	Off On 1 On	IS12IC	On Off(4) On 1 On	OS12IC[2]

NOTES:

1. The states which follow are associated with a DTE CALL REQUEST.
2. At this point, the connections from X.21 circuit R to V.24 circuit RXD and V.24 circuit TXD to X.21 circuit T are established. This output set refers to full duplex transmission only.
3. The states which follow are associated with the DCE indicating an INCOMING CALL.
4. Whe RTS goes on, this circuit also signals ON.

TABLE 5.7

This procedure may be outlined using a mixture of Pascal constructs and English as follows.

```
procedure       calreq;

const           false  =  0;
                true   =  1;

type            boolean  =  false ... true;
                char     =  IA5;
                osvalue, isvalue  =  as in table 5.7;

var             direct : boolean;
                selbuf: array (0 .. limit) of char;
                OS: osvalue;
                IS: isvalue;

begin           OS:    =   OS2;
                timestart (T1);
                repeat
                       read IS;
                until  IS  =  IS3;
                timestop;
                if   direct  =  false then
                   begin
                        transmit selbuf to DCE;
                   end
                OS  :  =  OS5
                timestart (T2);
                repeat
                        read IS;
                until  IS <>  IS3;
end.
```

ii) The incoming call routine (procedure incal)

Procedure incal waits for the DCE to signal INCOMING CALL (IS8) and then responds by signalling CALL ACCEPTED. Simultaneously, V.24 circuit CD is set ON, to avoid the DTE initiating a call request after the translator has accepted an incoming call from the DCE (OS9). Execution is continued when the DCE stops signalling INCOMING CALL and takes the interface to a new state.

Using the same constant and variable declarations as with procedure calreq, this routine is outlined below.

```
procedure     incal;
begin

     timestop;
     timestart (TSYN);
     repeat

          read IS;

     until   IS  =  IS8;
     timestop;
     OS   :=   OS9;
     timestart (T4);
     repeat

          read IS;

     until  IS  <>  IS8;

end.
```

(iii) The character identification routine (procedure charid).

Procedure charid may be executed either after procedure calreq or after procedure incal. On exit from these routines, the X.21 circuit R may be transmitting characters from IA5 (if the interface is in states 6, 7 or 10 of figure 3: DCE WAITING, CALL PROGRESS

SIGNALS or DCE PROVIDED INFORMATION), or it may be held at a steady binary 1 if the interface is in state 11 (CONNECTION IN PROGRESS) or 12 (READY FOR DATA).

While R is not at binary 1, procedure charid uses the information on R to determine whether the interface is in state 6, 7 or 10 and generates appropriate information for display on the console. This information may take the form of call progress signals, charge information or called/calling line identification. Call progress signals are transmitted by the DCE as a block of numeric characters, charge information as numeric characters preceded by a solidus ("/") and called/calling line identification as numeric characters preceded by either one or two asterisks ("*")depending on whether or not the line identification includes DNIC or DCC (see appendices A and B).

In the case of call progress signals this procedure determines whether any special action (i.e. "clear" or "clear and retry") should be taken by the translator and, when required, sets the appropriate variables (CLEAR? and RETRY) for processing at a later stage. The boolean variable RETRY is reset when procedure charid is entered, to avoid undesired call attempts being made by programme translator. The integer variable CLEAR? is used by the call clearing procedure (procedure clear) when implementing the X.21 call clearing process. Call progress signals are stored in a buffer in memory called CPBUF and displayed on the console.

When charge information is supplied by the DCE, it is displayed on the console. The boolean variable CHARGEINF which was set during procedure selsigs, is reset to false to avoid time-limit T7 (see appendix E) being started when the call is cleared.

Calling/called line identification is displayed on the console after the heading "REMOTE PARTY".

In the event of an unidentifiable character being received on R, it is displayed on the console with an appropriate error message.

When DCE circuit R is at binary 1, circuit I is tested to determine whether the interface is in state 11 or 12 (CONNECTION IN PROGRESS or READY FOR DATA). Once circuit I goes ON (READY FOR DATA), data transfer is enabled by connecting X.21 circuit R to V.24 circuit RXD and V.24 circuit TXD to X.21 circuit T (OS12). For full duplex data transfer, the ON condition is applied to V.24 circuit CD. The ON condition is also applied to CTS if RTS is ON (OS12CR). If RTS is OFF, CTS is held OFF until RTS goes ON, as could happen when an incoming call is being serviced (OS12IC).

As discussed in section 3.3.4.2(b), the implementation of half duplex transmission on a X.21 interface is essentially a matter of national option. For the preliminary model, the X.21 interface was treated as full duplex and on the V.24 interface, circuit CTS was switched ON and OFF in response to the DTE signal RTS. Circuit CD was given the opposite condition to CTS for the duration of data transfer. Figure 21 shows that this results in the correct conditions on V.24 circuit RXD for the implementation of half duplex transmission. It is assumed that the remote DTE is also operating in half duplex mode, as the translator requirements do not specify half duplex to full duplex conversion, and this has not been catered for.

Exit from procedure charid takes place after the necessity to clear the call has been indicated. This may be done by the DTE, via the console, after the expiry of some DTE time-limits, in response to call progress signals received from the DCE, or after translator hardware has detected a DCE CLEAR INDICATION. The integer variable CLEAR?, which is set to false on entering procedure charid, will be set to a value indicating whether DTE or DCE initiated clearing. When the value of CLEAR? is changed from false, procedure charid is terminated. The call clearing procedure (procedure clear) is then entered and depending on the value of CLEAR?, either a DTE CLEAR REQUEST or a DCE CLEAR INDICATION is executed on the X.21 interface. Simultaneously, OFF conditions are indicated on circuits CD and CTS on the V.24 interface and the connections between R and RXD, and TXD and T are broken.

In the following Pascal/English outline of procedure charid, the mnemonics for input and output sets are from table 5.7.

```
procedure     charid;

const         false  =  0;
              true   =  1;
              dteflag = arbitrary;

type          boolean = false .. true;
              isvalue, osvalue  =  as in table 5.7;
              char    =  IA5;

var           retry, chargeinf :  boolean;
              clear?  :  integer;
              IS  :  isvalue;
              OS  :  osvalue;
              cpbuf  :  array  (0 .. lim) of char;

begin
     retry, clear?    :=  false;
     while  R <> 1   and   clear?   =   false  do
          begin
               if  character  =  SYN  then
                 begin
                      message  :=  "DCE WAITING";
                 end
               else
                 begin  timestop;
                        timestart (T3A);
                    case  character  of
                       0..9 :   receive call progress signals
                                from USRT;  reset T3A after each
                                            call progress signal;
                                store in cpbuf;
                                send cpbuf to console;
                                If necessary, set clear? and
                                retry;
```

```
                        "/":     receive charge information;
                                 display on console;

                        "*":     receive called/calling line
                                 identification;
                                 display on console;
                        unidentified : display character with
                                       error message;

                    end    (case)
                end      (else)

            read next character from USRT;
        end   (while)
      if clear?  =  false then
        begin
            read IS;
            if I  =  OFF then
              begin
                  message  :=  "CONNECTION IN PROGRESS";
                  repeat
                       read IS;
                  until   I  =  ON;
              end
            timestop;
            message   :=  "READY FOR DATA";
            OS  :=  OS12;
            message   :=  "DATA TRANSFER";
            repeat
                 implement data transfer;
                 if console character = # then
                   begin clear? : = dteflag end
            until clear? < > false;
      end (if)
   end. (begin)
```

iv) The call clearing routines

Call clearing can be initiated either by an external interrupt or by a software instruction calling for execution of the call clearing routine, procedure clear.

The external interrupt, which should only be enabled once the X.21 interface is outside the quiescent phase, indicates that either the DTE or the DCE has initiated the clearing sequence. An ON to OFF transition of the V.24 signal DTR (as would occur if the DTE were switched OFF), or a persistent DCE signal of R, I = 0,OFF (indicating a DCE CLEAR INDICATION) would be responsible for this interrupt. In either event, an interrupt service routine, procedure clearserve, is executed. This routine stops the time-limit timer and then reads the input set to determine whether the DTE or DCE has initiated clearing. The integer variable CLEAR? is set to the constant value DTEFLAG if DTR is OFF and to DCEFLAG if DTR is ON.

Procedure clearserve next calls procedure clear to implement the X.21 call clearing procedure as defined in figure 4. Once this has been completed, procedure clearserve forces execution back to the start of programme translator.

The need to initiate call clearing with a software instruction arises from the X.21 requirement that a X.21 DTE must clear the call in progress after the DCE has transmitted certain call progress signals (see Appendix C). Depending on the call progress signals received, procedure charid may set CLEAR? to DTEFLAG. Charid is then terminated and procedure clear is called to implement the X.21 call clearing sequence. Execution is then returned to the start of programme translator. The translator software also allows a call to be cleared from the console during the data transfer phase. If the IA5 character "#" is typed from the console during data transfer, CLEAR? is set to DTEFLAG and charid is terminated as before.

A Pascal/English description of procedure clearserve is given below.

```
procedure clearserve;

const
        dteflag, dceflag = arbitrary constants;
        OFF = binary 1;
        ON = binary 0;

type
        boolean = OFF.. ON;
        isvalue = as in tables 5.6, 5.7;

var
        clear? : integer;
        DTR    : boolean;
        IS     : isvalue;

label
        start;

begin
        timestop
        tidy up present routine;
        read IS;
        if DTR = OFF then
          begin
              clear? = dteflag;
          end
        else
          begin
              clear? = dceflag;
          end
        clear;
        goto  start;
end
```

As with procedure clearserve, procedure clear, which is described below, begins by stopping the timelimit timer. Procedure clear then sets the output set to OS16/20 of table 5.8. This will be interpreted by the DCE either as a DTE CLEAR REQUEST or as a DTE CLEAR CONFIRMATION, depending on the DCE signal on R, I.

Procedure clear next tests the integer variable CLEAR? and if this is set to DCEFLAG the message "DCE CLEAR INDICATION" is sent to the console. Timelimit T6 is started and the translator waits for the DCE to signal READY (state 21 of figure 4/IS21 of table 5.8), after which the timer is stopped.

EQUIPMENT STATE		INPUT SET (IS)		CORRESPONDING OUTPUT SET (OS)	
V.24 DTE	X.21 DCE	RTS,DTR, R, I	MNEM	CD, CTS, DSR, T, C	MNEMONIC
X	X	- - - -	-	OFF, OFF, ON O, OFF	OS16/20
X	DCE CLEAR CONFIR-MATION	X X 0,OFF	IS17	OFF, OFF, ON, O, OFF	OS16/20
X	DCE READY	X X 1,OFF	IS21	N.A.	-

TABLE 5.8

If CLEAR? is not set to DCEFLAG the message "DTE CLEAR REQUEST" is sent to the console and timelimit T5 is started. The translator waits for the DCE to respond with IS17 of table 5.8 and then signals "DCE CLEAR CONFIRMATION" to the console. When the DCE signals READY (IS21 of table 5.8/state 21 of figure 4) the timer is stopped.

Having received the DCE READY signal, procedure clear checks the boolean variable CHARGEINF (see section 5.3.4.2 (a)). If it is set to true, timelimit T7 is started and CHARGEINF is reset to false. Before procedure clear is terminated and execution is returned to the calling routine, the integer variable CLEAR? is set to false. The calling routine returns execution to quiescent phase translation, which will result in the X.21 interface returning to state 1 if the DTE condition permits it.

A Pascal/English description of procedure clear follows.

```
procedure  clear;

const
        dceflag = arbitrary constant;
        true = 1;
        false = 0;

type
        boolean = false.. true;
        isvalue, osvalue = as in table 5.8;

var
        OS: osvalue;
        IS: isvalue;
        clear?: integer;
        chargeinf:  boolean;

begin
        timestop;
        OS : = OS16/20;
        if clear? = dceflag then
           begin
               message : = "DCE CLEAR INDICATION";
               timestart (T6);
           end
        else
           begin
               message : = "DTE CLEAR REQUEST";
               timestart (T5);
               repeat
                    read IS;
               until IS = IS17;
               message : = "DCE CLEAR CONFIRMATION";
           end
        repeat
           read IS;
        until IS: = IS21;
        timestop;
        if  chargeinf = true then
           begin
               timestart (T 7);
               chargeinf : = false;
           end
        clear? : = false;
end.
```

(v) Implementation of time-limits.

All the time-limits of appendix E are implemented using the two procedures timestart and timestop.

Procedure timestart loads timer TB (See Section 5.3.4.1) with a value corresponding to the time-limit being started and starts the timer counting down. It also sets the integer variable TIME LIMIT to a value corresponding to the appropriate time-limit, for processing at a later stage. Procedure time-stop stops timer TB counting down.

If timer TB reaches its terminal count, it generates an interrupt which forces execution to a service routine. This routine examines TIME LIMIT to determine which time-limit has expired. It then takes action as specified in table E.1 of appendix E before returning execution to programme translator. Such action could, for example, consist of setting the integer variable CLEAR? to the value appropriate for a DTE CLEAR INDICATION and then calling procedure clear.

Procedure timestart is called whenever a DTE time-limit is specified in table E.1. Procedure timestop is called whenever the appropriate terminating state is entered. For instance, after procedure calreq signals a call request, it calls procedure timestart to load timer TB with a 3 second count value. When the DCE signals PROCEED TO SELECT, calreq calls procedure timestop to stop the downcount.

A new time-limit, TSYN, has been introduced in addition to those of table E.1. It caters for the possibility of the DCE transmitting a continuous string of "SYN" characters in state 8 (INCOMING CALL), as mentioned at the end of section 5.3.2.3.

The interrupt service routine, procedure timeserve, is described below. Note that actions in table E.1 such as "DTE signals DTE READY (state 1)" are fulfilled by returning execution to programme translator.

```
procedure     timeserve;
const         dteflag = arbitrary;
var           time limit, clear? : integer;

begin
              case time limit of
                  T1, T5, T6, TSYN:  appropriate message to console,
                                     e.g., "T ... expired";
                  T2, T3, T4      :  clear?   :=   dte flag;
                                     clear;    (call procedure clear);

                  T7              :  message  :=  "no charge information
                                     received";
              end
              return execution to programme translator;
end.
```

d) Software Summary

To summarise section 5.3.4.2, the version of programme translator developed in the section on physical layer software may be extended to include the link and network layer procedures described above. This summary, in the Pascal/English notation previously used, was refined to a purely Pascal version and then translated into assembly language for the preliminary model of the translator.

```
programme      translator;

const          false  =  0;
               true   =  1;

type           boolean  =  false  ..  true;
               isvalue, osvalue  =  as in tables 5.6 and 5.7;

var            incom, retry, abort: boolean;
               IS:   isvalue;
               OS:   osvalue;
label          start;
begin
     initialise USRT;
start: repeat
         incom    :=  false;
         interrogate USRT;
         if SYN characters received then
           begin incom   :=  true  end
         read IS;
         case IS of
```

```
IS1:    OS  :=  OS1;
        message  :=  "DTE READY, DCE READY";
        if retry  =  true then
          begin
            retry  :=  false;
            calreq;
            charid;
            clear;
          end
        else
          begin
            if RTS  =  ON then
              begin
                selsigs;
                if abort  =  false then
                  begin
                    calreq;
                    charid;
                    clear;
                  end
              end
            else
              begin
                if incom  =  true then
                  begin
                    incal;
                    charid;
                    clear;
                  end
              end
        end
```

```
IS18:     OS  :=  OS18;

          message  :=  "DTE READY, DCE NOT READY";


IS24:     OS  :=  OS24;

          message:  =  "DTE NOT READY, DCE READY";


IS22:     OS  :=  OS22;

          message  :=  "DTE NOT READY, DCE NOT READY";

undefined:OS  :=  OS22;

          message  :=  "undefined quiescent state";
          repeat read IS until IS = IS1 or = IS24;

  end   (case)

until forever;

end.
```

6. CONCLUSION

6.1 PRESENT STATUS OF DEVELOPMENT

The current status of work done on protocol conversion between the X.21 and V.24 interfaces is as follows:

i) For conversion between a X.21 DTE and a V.24 DCE a simple interface adaptor has been designed. Use of this adaptor assumes the presence of either dedicated circuits or dial-up facilities with the V.24 interface to cater for the network layer function of call establishment. The adaptor performs X.21 to V.24 translation on the physical level only.

ii) For conversion between a V.24 DTE and a X.21 DCE, two cases have been treated separately. The first is that of dedicated circuits, for which an interface adaptor has been designed. This adaptor, similar to that mentioned above, performs translation on the physical level only as the implementation of X.21 dedicated circuits involves no link or network layer features.

The second case concerns translation between a V.24 DTE and X.21 DCE on the circuit switched service, covering the three lower layers of the OSI model. A microprocessor-based device has been designed on a development system as a preliminary version of this translator. The DTE operator is presented with a console allowing interaction with the DCE to realise network layer features (such as call establishment) associated with the X.21 interface. This unit requires the DTE operator to generate selection signals from the console to establish outgoing calls and allows automatic answering of incoming calls.

6.2 FURTHER DEVELOPMENT

The major portion of any further development would be directed at the microprocessor-based device performing translation between the V.24 DTE and X.21 DCE. This work would be directed at building a stand-alone version of the translator based on the preliminary model, which presently exists on a development system only. A significant part of this work would consist of designing a suitable operator console, which could consist of a 16-way keypad and 7-segment displays. Apart from this, other areas for further development are listed below.

i) The software developed for the V.24 DTE/X.21 DCE translator could easily be extended to cover dedicated circuit working. This has not been done for the preliminary model as a simple hardware solution has been developed. However, the microprocessor-based version could be made more universal with minimal effort, to cover the case of a DTE requiring access to both dedicated and circuit switched circuits.

ii) A limited degree of automatic calling could be realised by extending <u>procedure</u> selsigs, which receives selection signals from the console for use during call establishment. Presently, <u>procedure</u> selsigs is entered when the DTE signals ON on RTS. The operator then types in his selection signal sequence from the console and on termination of the sequence, <u>procedure</u> selsigs is ended and a call request generated by the translator.

It would be a fairly simple matter to extend <u>procedure</u> selsigs to allow one or more buffers of selection signals to be entered into the translator before the DTE signals a call request. When the DTE then signals ON on RTS, the translator could generate a call request without operator intervention. When the translator is holding more than one buffer of selection signals, successive OFF to ON transitions on RTS could be used to generate a number of call requests in succession without operator intervention. This extension to procedure selsigs would give the V.24 DTE the ability to perform a limited amount of automatic calling when connected to a X.21 network, which is a significant advantage over operation with a V.24 DCE, with which automatic calling cannot be realised in this country.

6.3 SUMMARY

In this thesis, some basic trends in data communications have been outlined. The tendency to move away from data transmission over the PTN to public data networks has been identified, and the importance of the DTE/DCE interface and related communications protocols stressed. The V.24 interface has been described as the traditional DTE/DCE interface, having evolved with data communications over the public telephone network. The CCITT X.21 recommendation has been associated with the emergence of PDNs and identified as a popular new DTE/DCE interface allowing such features as automatic call establishment, which are not available with V.24 equipment in this country. The need for a device to perform translation between X.21 and V.24 interfaces has been described, and requirements for such a translator identified. The ISO's model for open systems interconnection has been described where it is relevant to PDNs and the DTE/DCE interface.

The X.21 interface as defined by the CCITT has been described in some detail, using the layered concept suggested by the OSI model. Advantages and shortcomings associated with the use of X.21 have been identified. The traditional V.24 interface has also been described, in terms of the physical layer of the OSI model.

Interface adaptors using combinational logic have been developed for translation from a X.21 to DTE to V.24 DCE interface, and a V.24 DTE to X.21 DCE with a dedicated circuit interface. A microprocessor-based translator has been developed along the lines of a finite state machine to perform translation between a V.24 DTE and X.21 DCE on the switched circuit service. Design method, hardware and software for this device have been outlined, and areas for further work identified.

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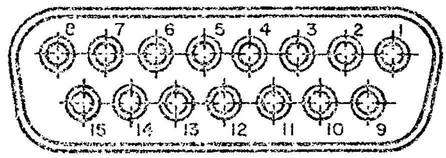
15. C.H. West and P. Zafiropulo, "Automated Validation of a Communications Protocol : The CCITT X.21 Recommendation", IBM Journal of Research and Development, Vol 22, No. 1, Jan 1978, pp 60-71.

16. CCITT Study Group XVII, Recommendation V.24, CCITT Yellow Book, Fascicle VIII.1, Geneva, Switzerland, 1980, pp 97-112.

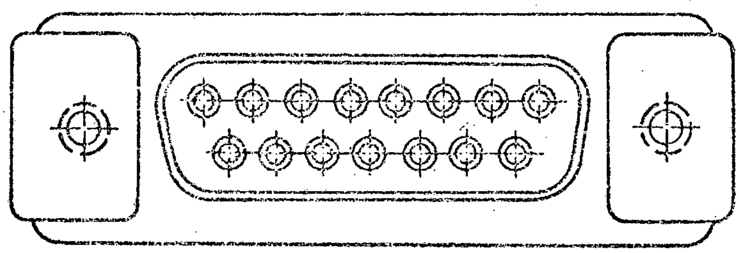
17. EIA Standard RS-232-C, "Interface between DTE and DCE employing serial binary data interchange", August 1969.

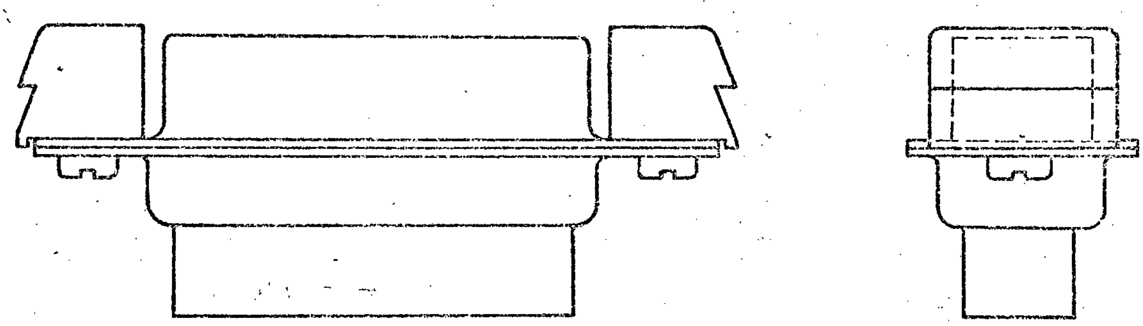
18. Industrial Electronics Bulletin No. 9, "Application Notes for EIA Standard RS-232-C", May 1971.

19. CCITT Study Group VII, Recommendation X.21 bis, CCITT Yellow Book, Fascicle VIII.2, Geneva, Switzerland, 1980, pp 82-91.



DCE CONNECTOR FACE
CONTACT NUMBERING

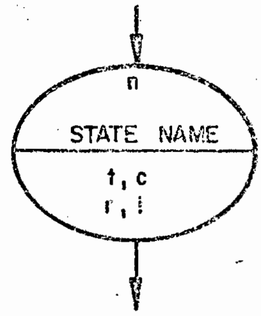




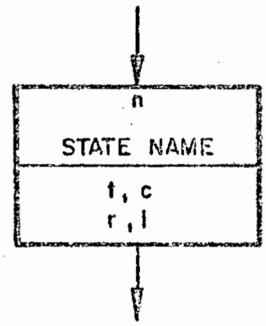
DCE INTERFACE CONNECTOR

(Not to scale)

FIGURE - 1



STATE WITH ONE SET OF DTE/DCE SIGNALS



STATE WITH FAMILY OF DTE/DCE SIGNALS.

DEFINITION OF STATE DIAGRAMS

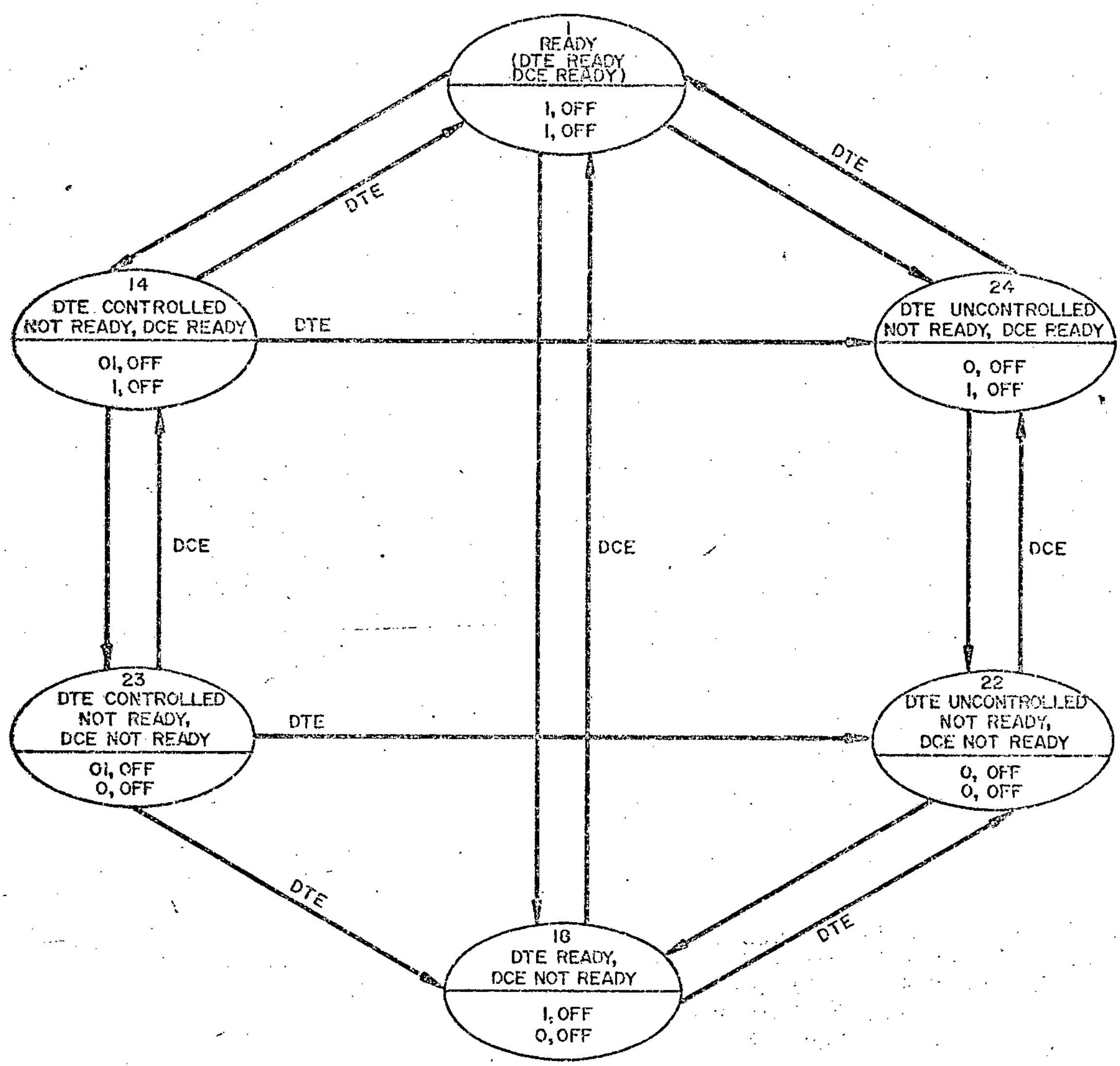
FIGURE 2(a)

Legend

n	State number
t,c,r,i	signals on circuits T,C,R, and I respectively
(t,c)	DTE output set/DCE input set
(r,i)	DCE output set/DTE input set
↓	Inter-state transition with indication showing whether DTE or DCE initiates transition.

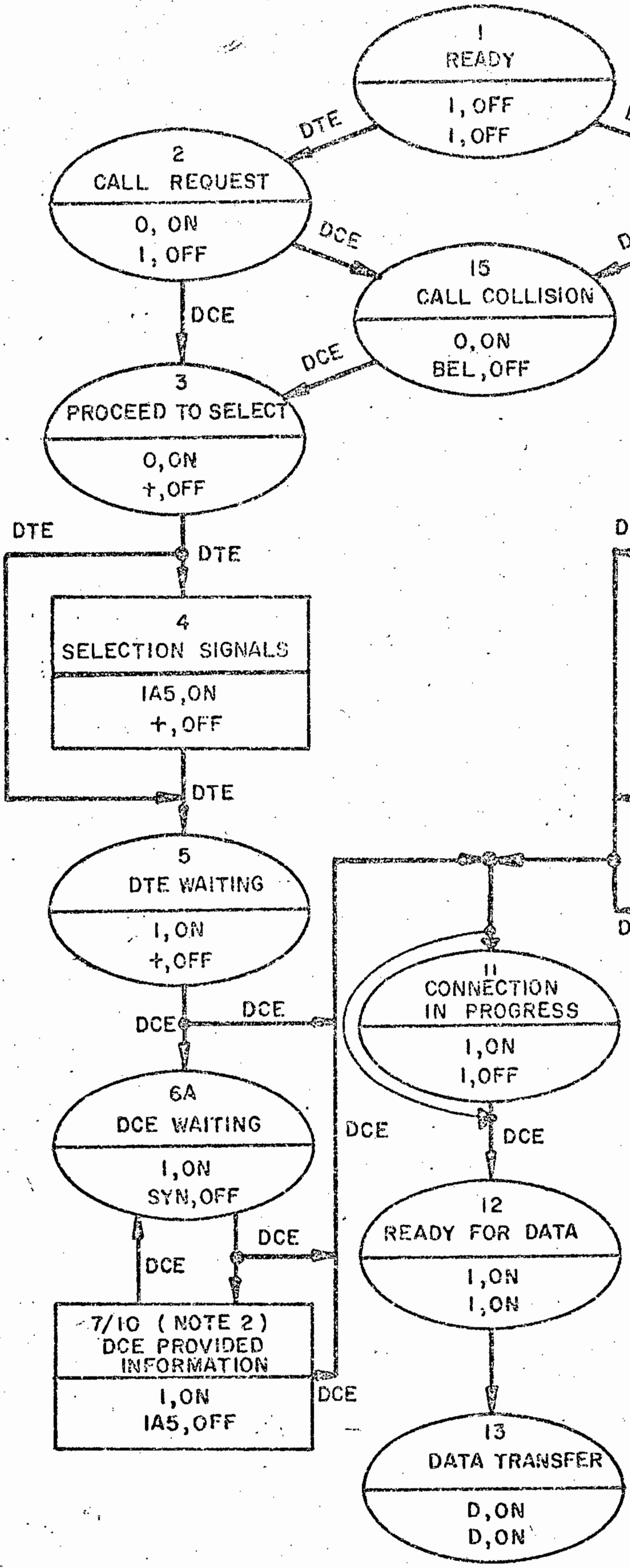
Signal Definitions

0 and 1	Steady binary conditions
01	Alternate transmission of binary 0 and binary 1
ON and OFF	continuous ON and OFF conditions: steady binary 0 and 1 respectively.
X	Any value (not necessarily steady)
IA5	Character strings from International Alphabet No. 5, as defined in CCITT recommendation V.3.
+,BEL,SYN	Continuous transmissions of these IA5 characters, two characters being the minimum duration permitted for such transmissions.
D	DTE or DCE data signals



QUIESCENT STATES

FIGURE 2(b)

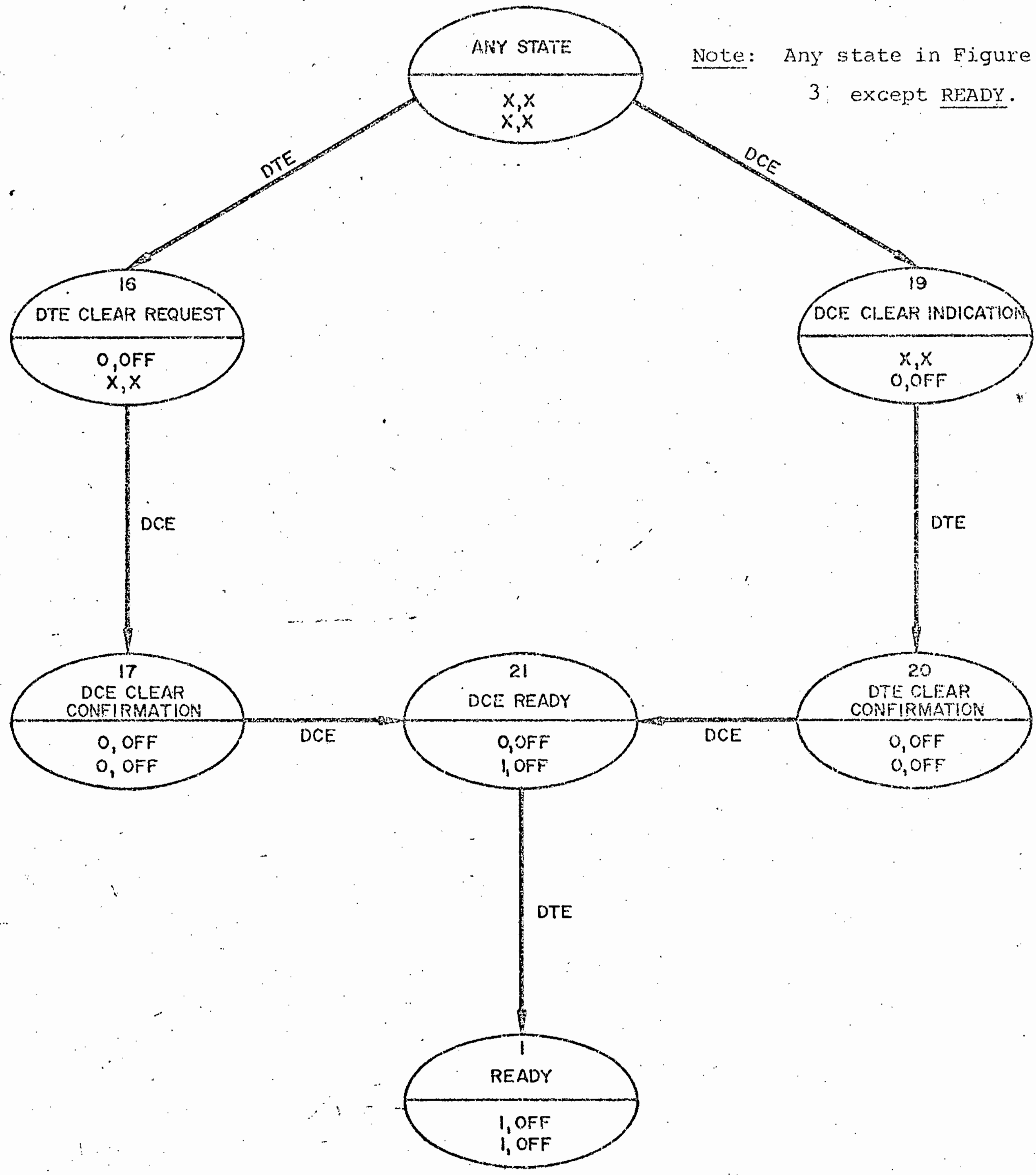


Note 1: As indicated in Figure 4 , the DCE may enter state 19 from any state, and the DTE may enter state 16 from any state except READY.

Note 2: For simplification of the state diagram, state 7 (CALL PROGRESS SIGNALS) is merged with state 10 (DCE PROVIDED INFORMATION).

CALL CONTROL PHASE FOR CIRCUIT — SWITCHED SERVICE

FIGURE 3



CLEARING PHASE

FIGURE 4

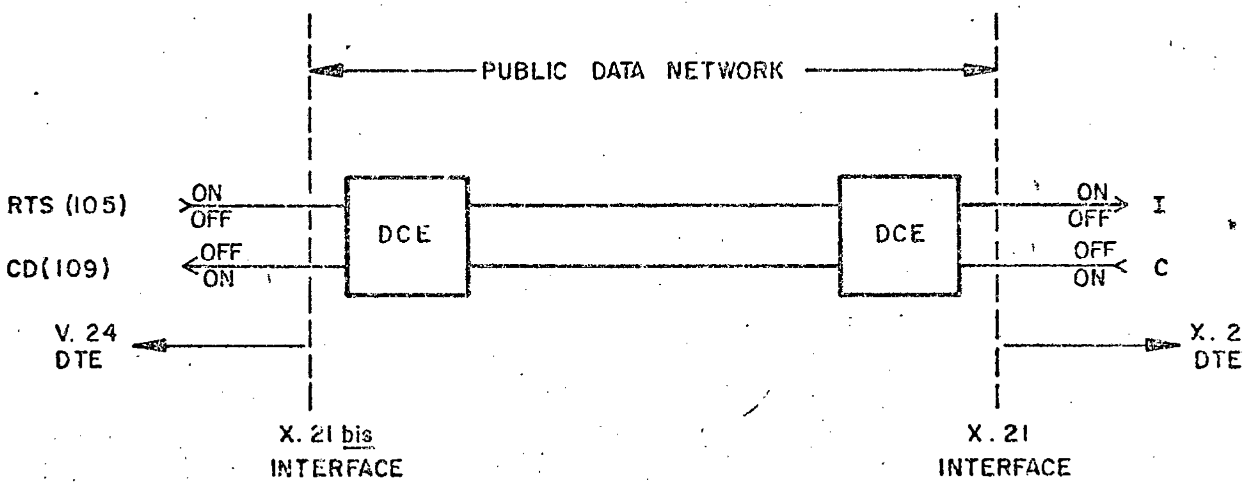
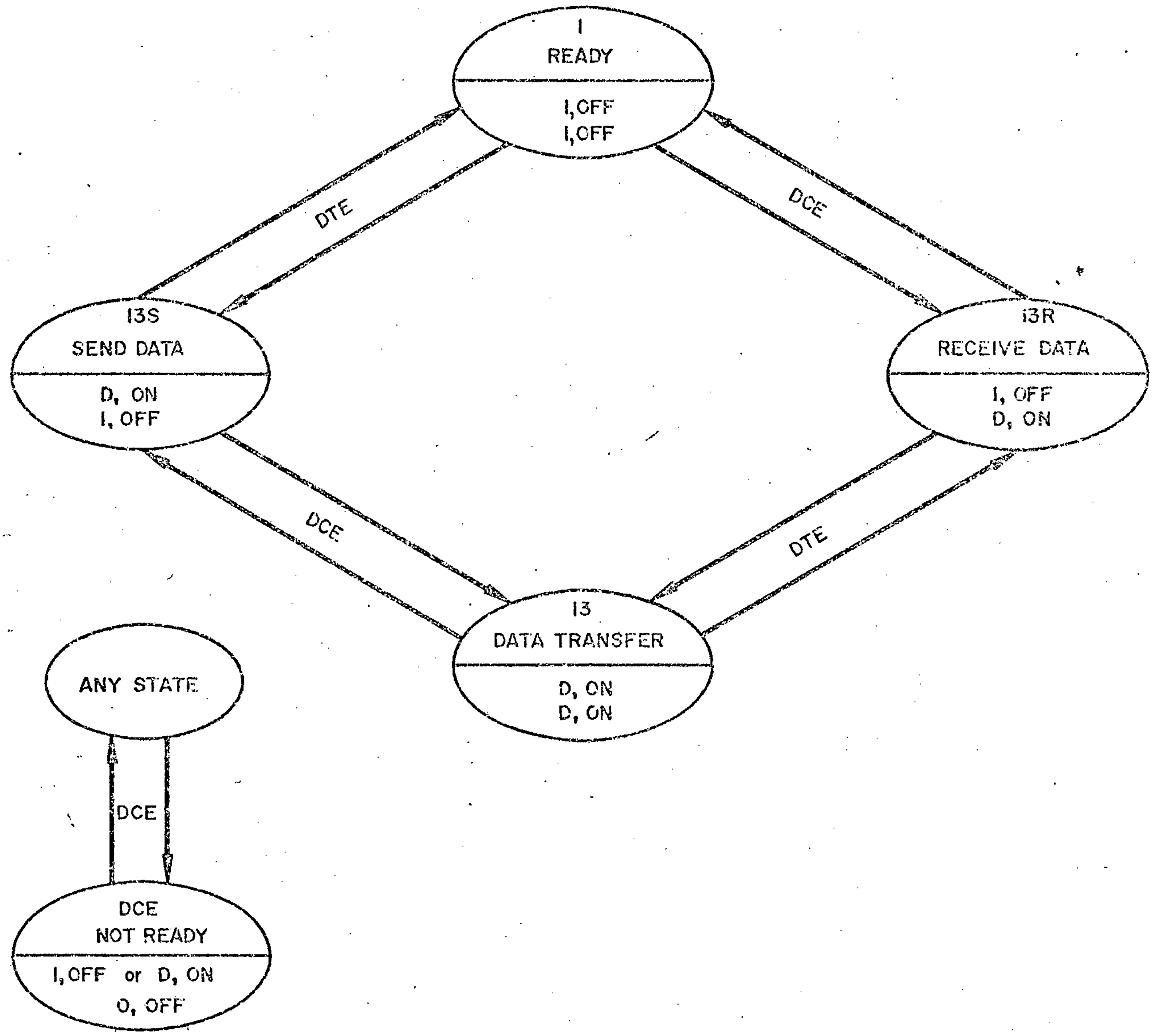

PUBLIC DATA NETWORK
RTS (105)
ON
OFF
CD(109)
OFF
ON
DCE
DCE
ON
OFF
I
OFF
ON
C
V. 24
DTE
X. 21
DTE
X. 21 bis
INTERFACE
X. 21
INTERFACE

FIGURE 5



LEASED CIRCUIT SERVICE
FIGURE 6

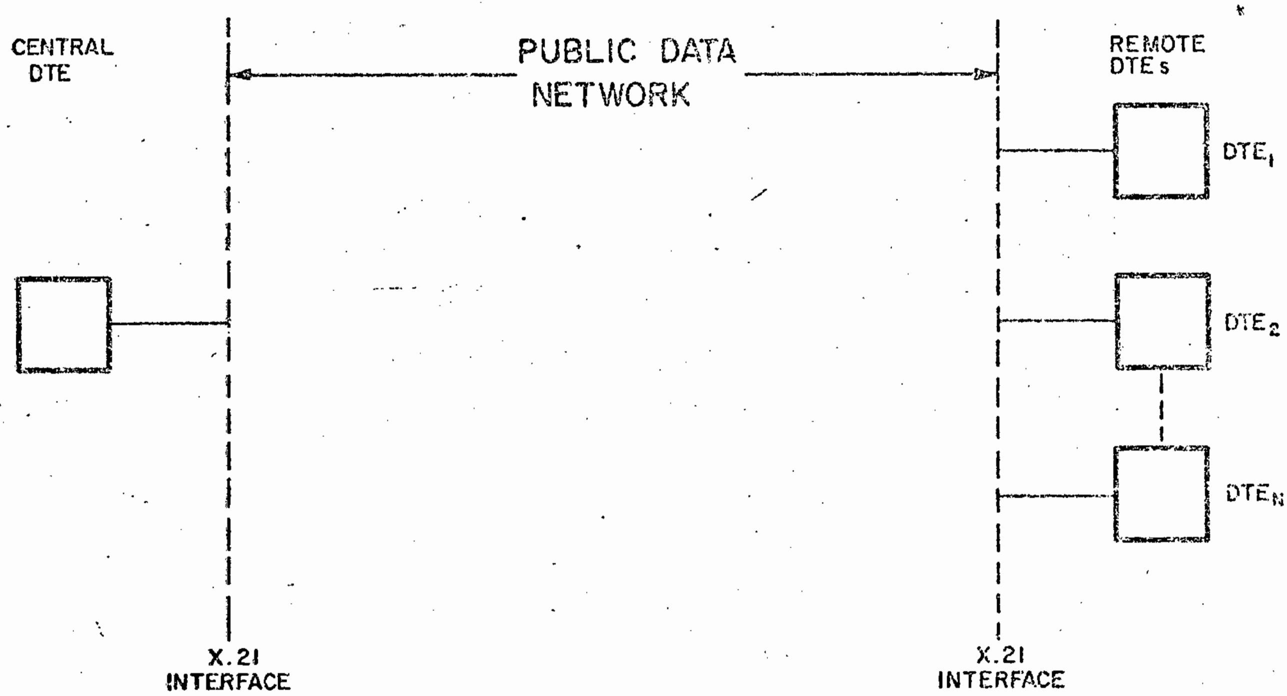

CENTRAL
DTE
PUBLIC DATA
NETWORK
REMOTE
DTE s
DTE_1
DTE_2
DTE_N
X.21
INTERFACE
X.21
INTERFACE

FIGURE 7

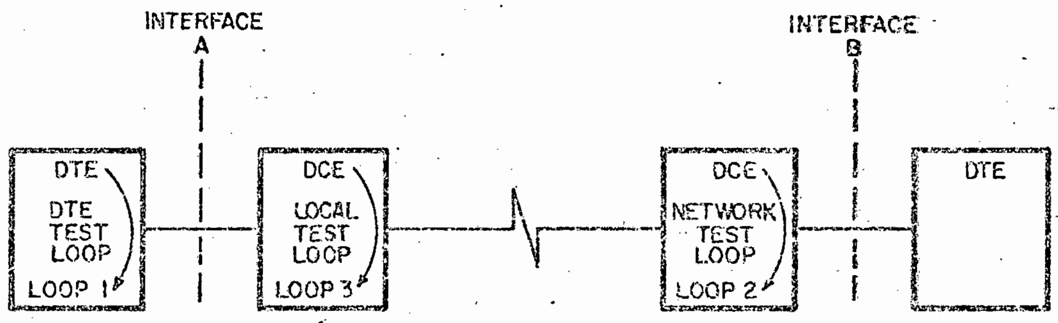
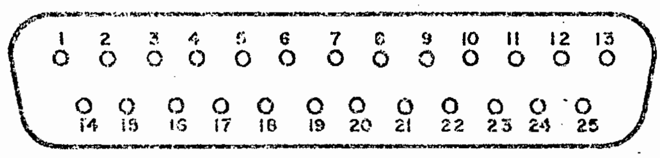
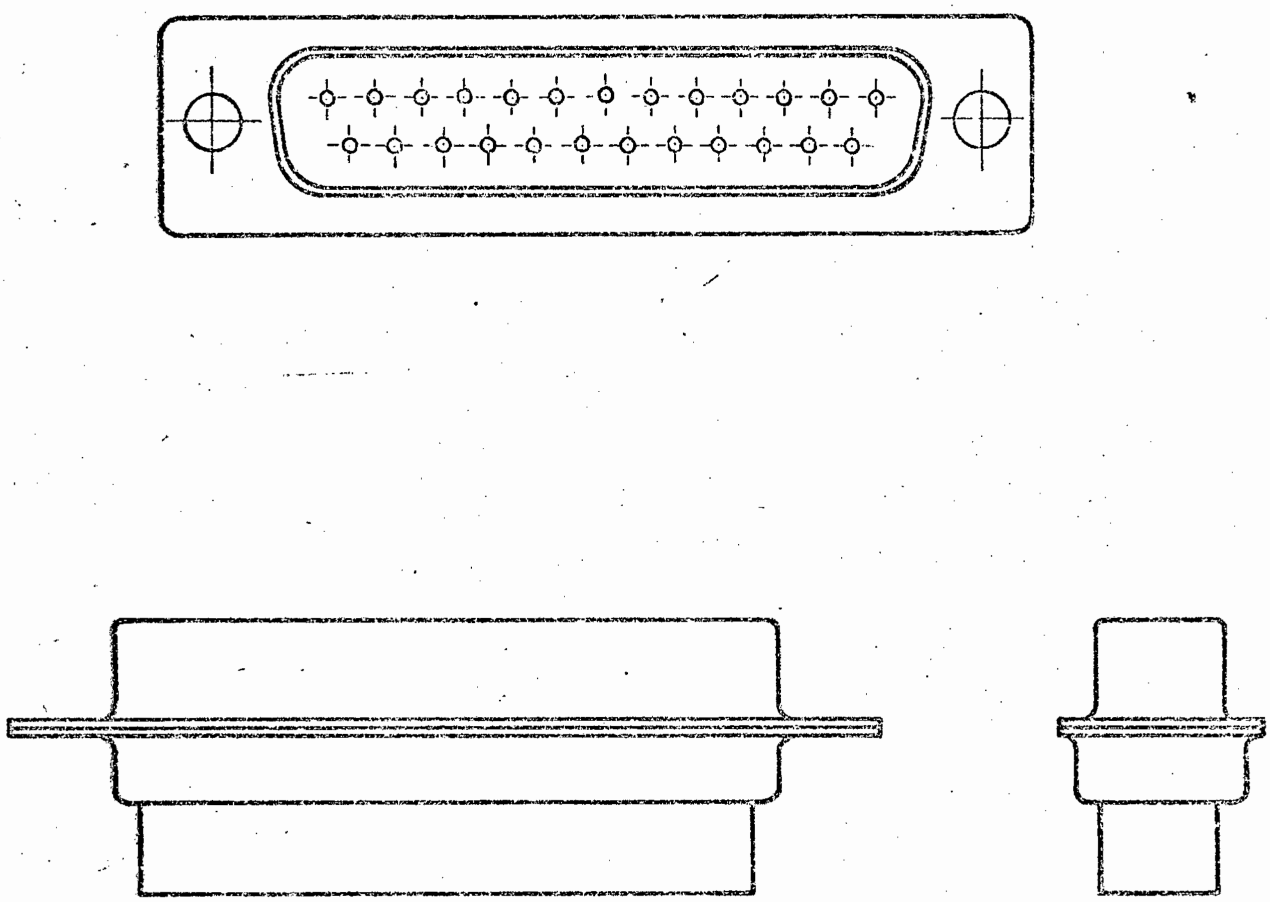


Figure 8 Test Loops

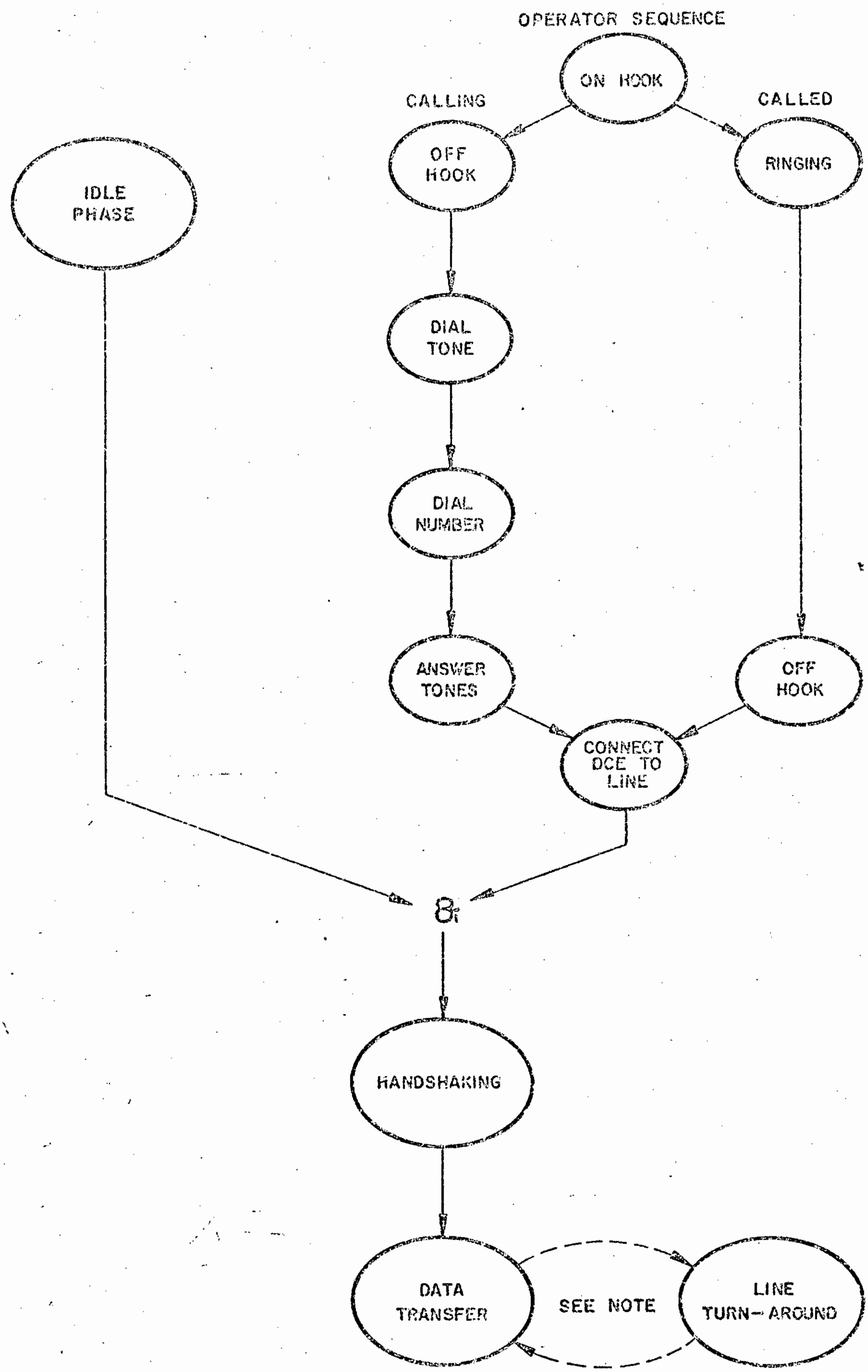


DTE CONNECTOR FACE
CONTACT NUMBERING



DTE INTERFACE CONNECTOR
(NOT TO SCALE)

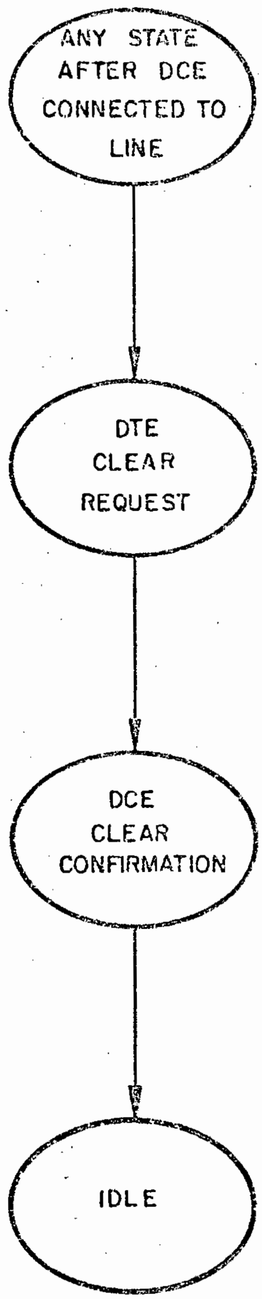
FIGURE 9.



NOTE :- ONLY FOR HALF DUPLEX TRANSMISSION

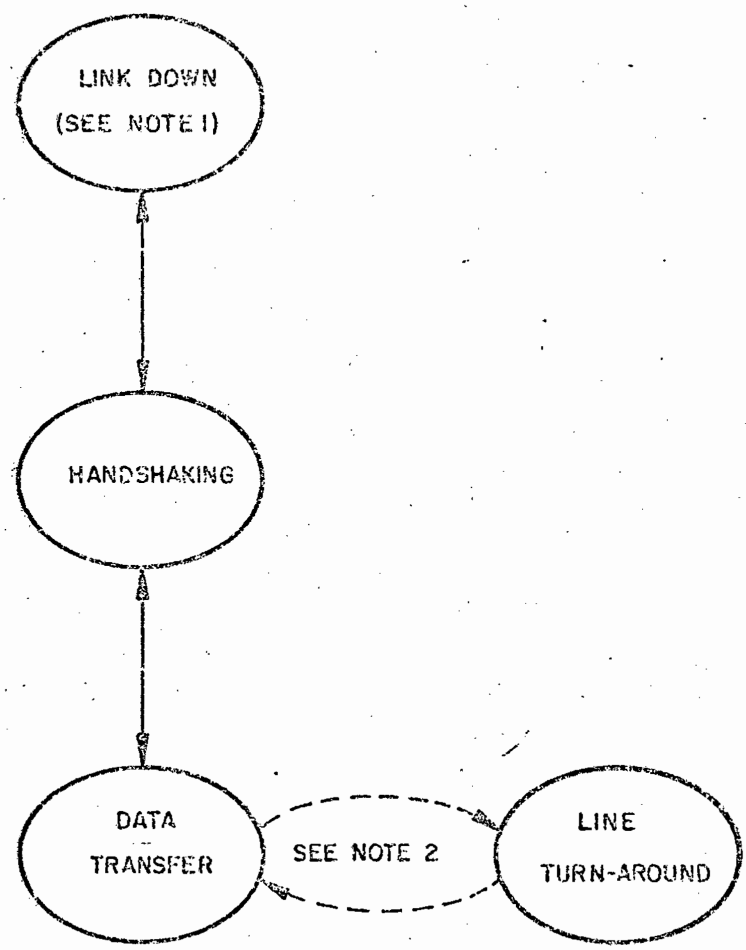
CALL ESTABLISHMENT WITH A V.24 INTERFACE ON A SWITCHED SERVICE

FIGURE 10



CALL CLEARING WITH A V. 24 INTERFACE ON THE SWITCHED SERVICE.

FIGURE 11



NOTES:

1) THIS ONLY OCCURS WITH EQUIPMENT OR POWER FAILURE
2) ONLY FOR HALF DUPLEX TRANSMISSION.

V. 24 INTERFACE AS USED FOR A DEDICATED CIRCUIT

FIGURE 12

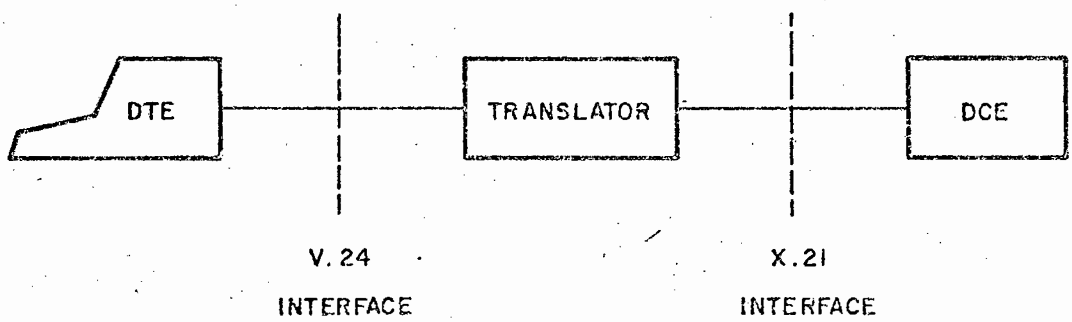
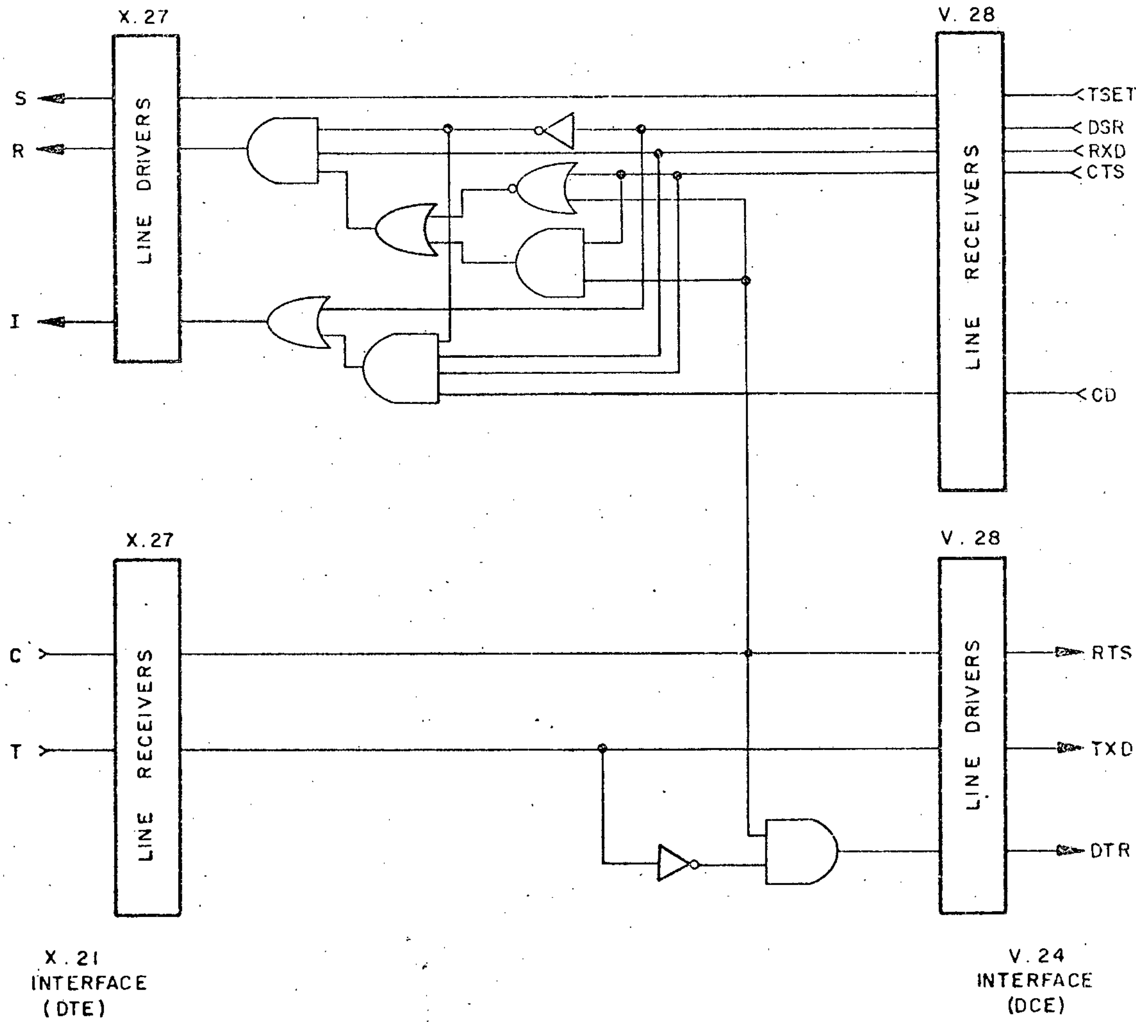
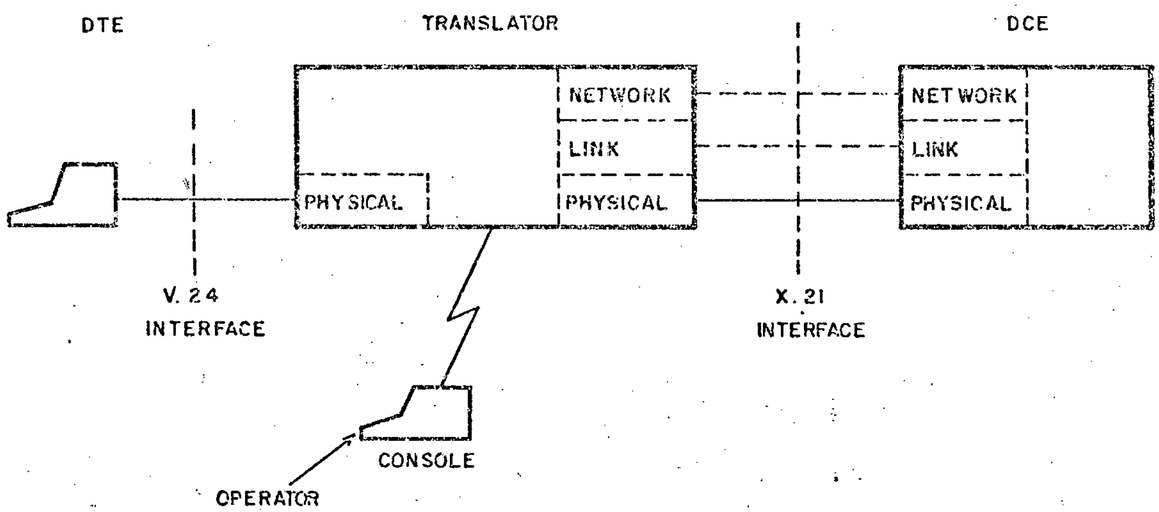


FIGURE 13



INTERFACE ADAPTOR FOR USE WITH A X.21 DTE CONNECTED TO A V.24 DCE

FIGURE 14

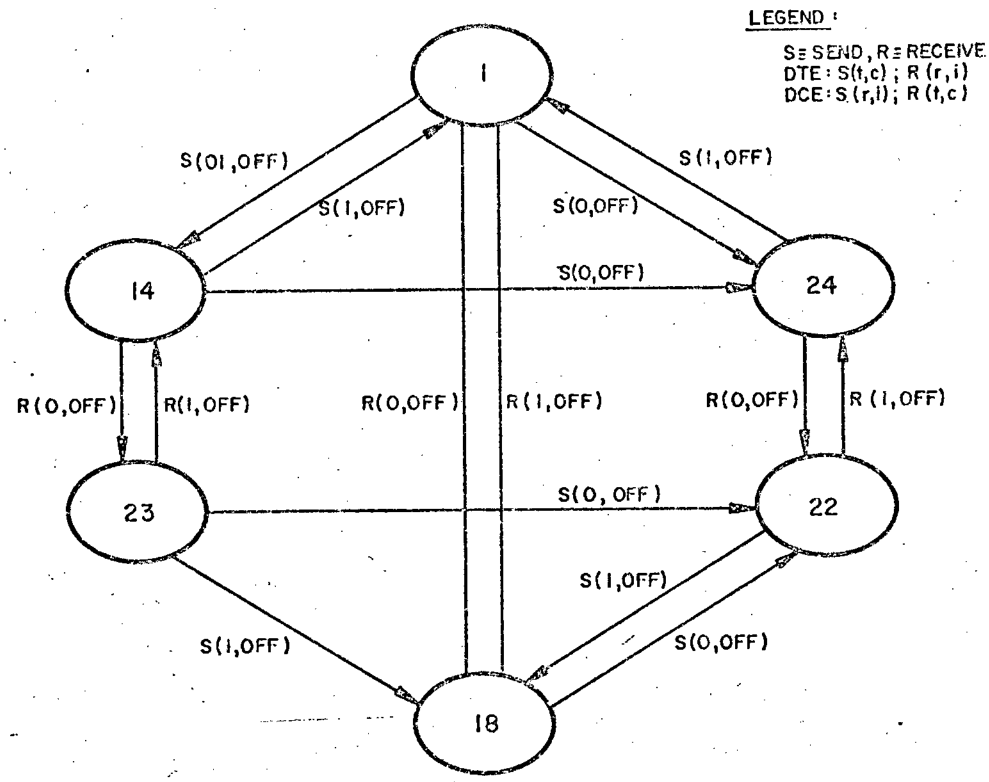


THE TRANSLATOR IN TERMS OF THE O.S.I. MODEL

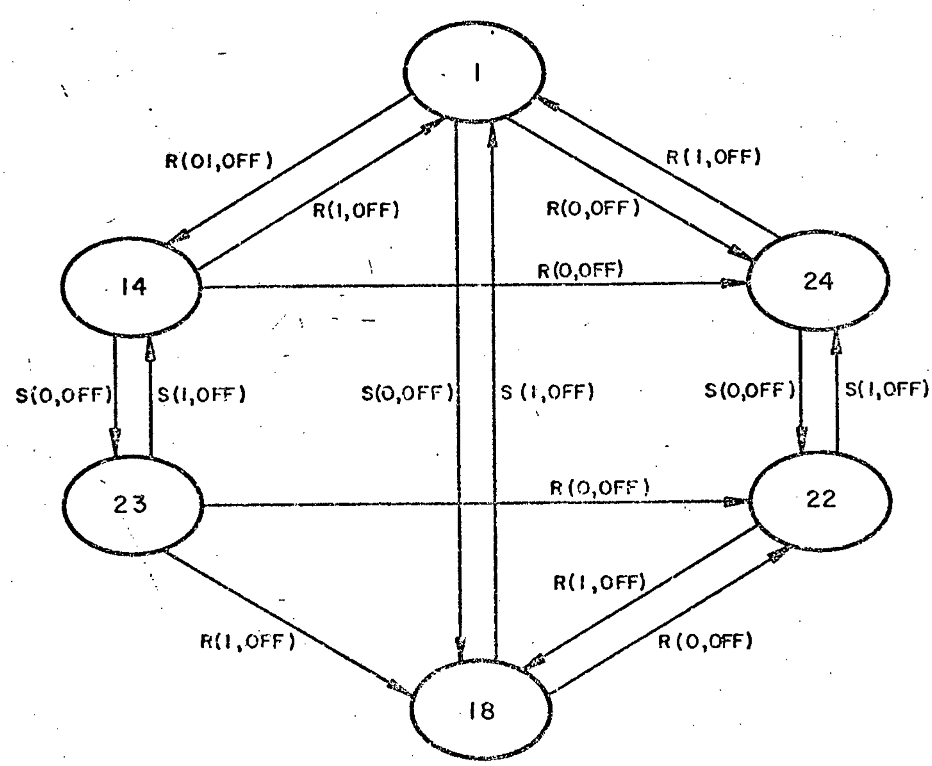
FIGURE 15

X.21 STATE NUMBERS AND NAMES

STATE 1:	DTE READY, DCE READY
STATE 14:	DTE CONTROLLED NOT READY, DCE READY
STATE 18:	DTE READY, DCE NOT READY
STATE 22:	DTE UNCONTROLLED NOT READY, DCE NOT READY
STATE 23:	DTE CONTROLLED NOT READY, DCE NOT READY
STATE 24:	DTE UNCONTROLLED NOT READY, DCE READY

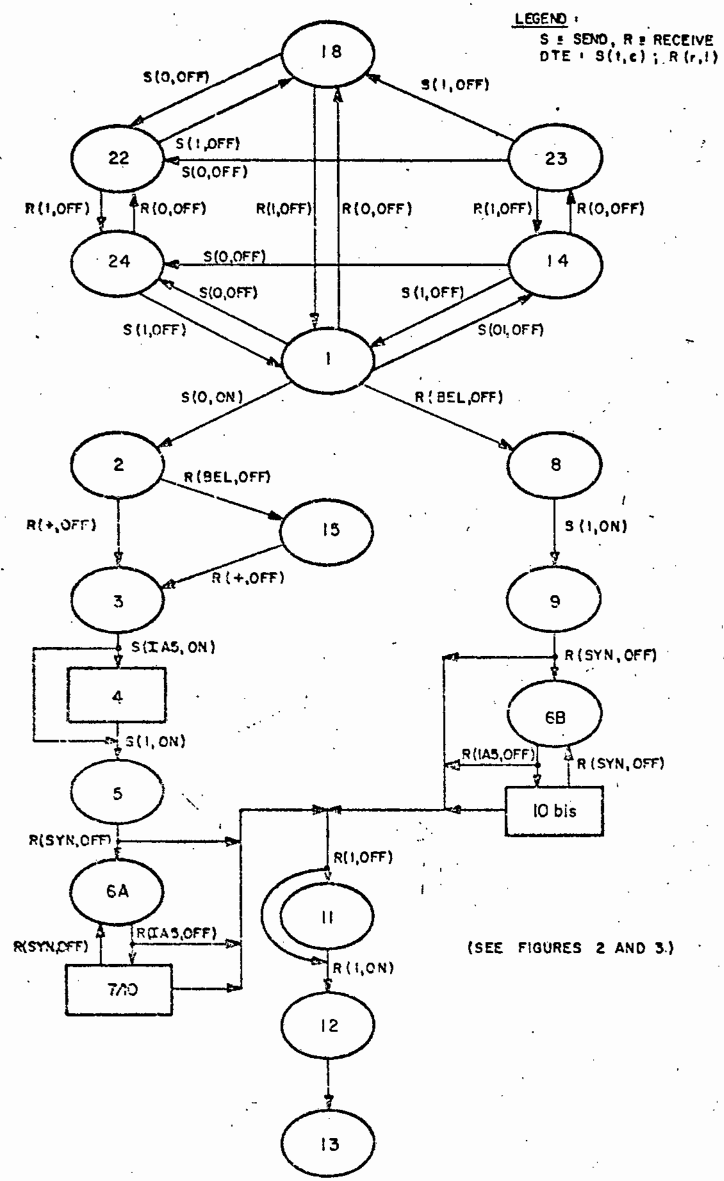


DERIVED STATE DIAGRAM FOR X.21 DTE IN QUIESCENT PHASE
(SEE FIGURE 2)



DERIVED STATE DIAGRAM FOR X.21 DCE IN QUIESCENT PHASE
(SEE FIGURE 2)

FIGURE 16



DERIVED STATE DIAGRAM SHOWING OPERATIONAL SEQUENCE FOR X.21 DTE

FIGURE 17

X. 21 STATE NUMBERS AND NAMES

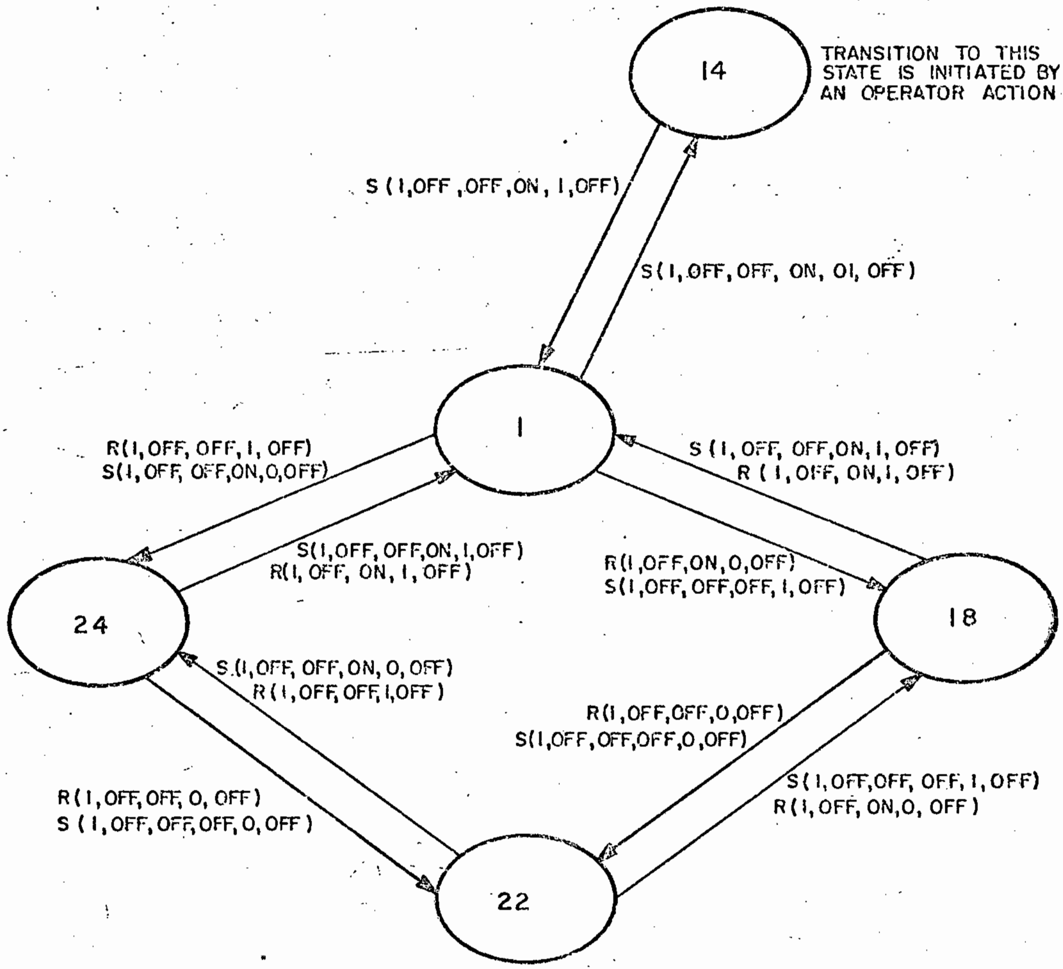
STATE 1:	DTE READY, DCE READY
STATE 2:	CALL REQUEST
STATE 3:	PROCEED TO SELECT
STATE 4:	SELECTION SIGNALS
STATE 5:	DTE WAITING
STATE 6A:	DCE WAITING
STATE 6B:	DCE WAITING
STATE 7:	CALL PROGRESS SIGNALS
STATE 8:	INCOMING CALL
STATE 9:	CALL ACCEPTED
STATE 10:	DCE PROVIDED INFORMATION
STATE 10 bis:	DCE PROVIDED INFORMATION
STATE 11:	CONNECTION IN PROGRESS
STATE 12:	READY FOR DATA
STATE 13:	DATA TRANSFER
STATE 14:	DTE CONTROLLED NOT READY, DCE READY
STATE 15:	CALL COLLISION
STATE 18:	DTE READY, DCE NOT READY
STATE 22:	DTE UNCONTROLLED NOT READY, DCE NOT READY
STATE 23:	DTE CONTROLLED NOT READY, DCE NOT READY
STATE 24:	DTE UNCONTROLLED NOT READY, DCE READY

X.21 STATE NUMBERS AND NAMES

STATE 1: DTE READY, DCE READY
STATE 14: DTE CONTROLLED NOT READY, DCE READY
STATE 18: DTE READY, DCE NOT READY
STATE 22: DTE UNCONTROLLED NOT READY, DCE NOT READY
STATE 24: DTE UNCONTROLLED NOT READY, DCE READY

LEGEND
S ≡ SEND , R ≡ RECEIVE
TRANSLATOR : S(RXD, CD, CTS, DSR, T, C) ; R(TXD, RTS, DTR, R, I)

NOTE : THE TRANSITIONARY EVENTS MUST OCCUR IN THE SEQUENCE INDICATED BY THE ARROWS.



STATE DIAGRAMS REPRESENTING THE TRANSLATOR AS A FINITE STATE MACHINE DURING THE QUIESCENT PHASE.

FIGURE 18

NOTE :- THE SAME SEQUENCE OF ALTERNATE 1's AND 0's IS BEING TRANSMITTED ON CIRCUITS R, T, 103 AND 104

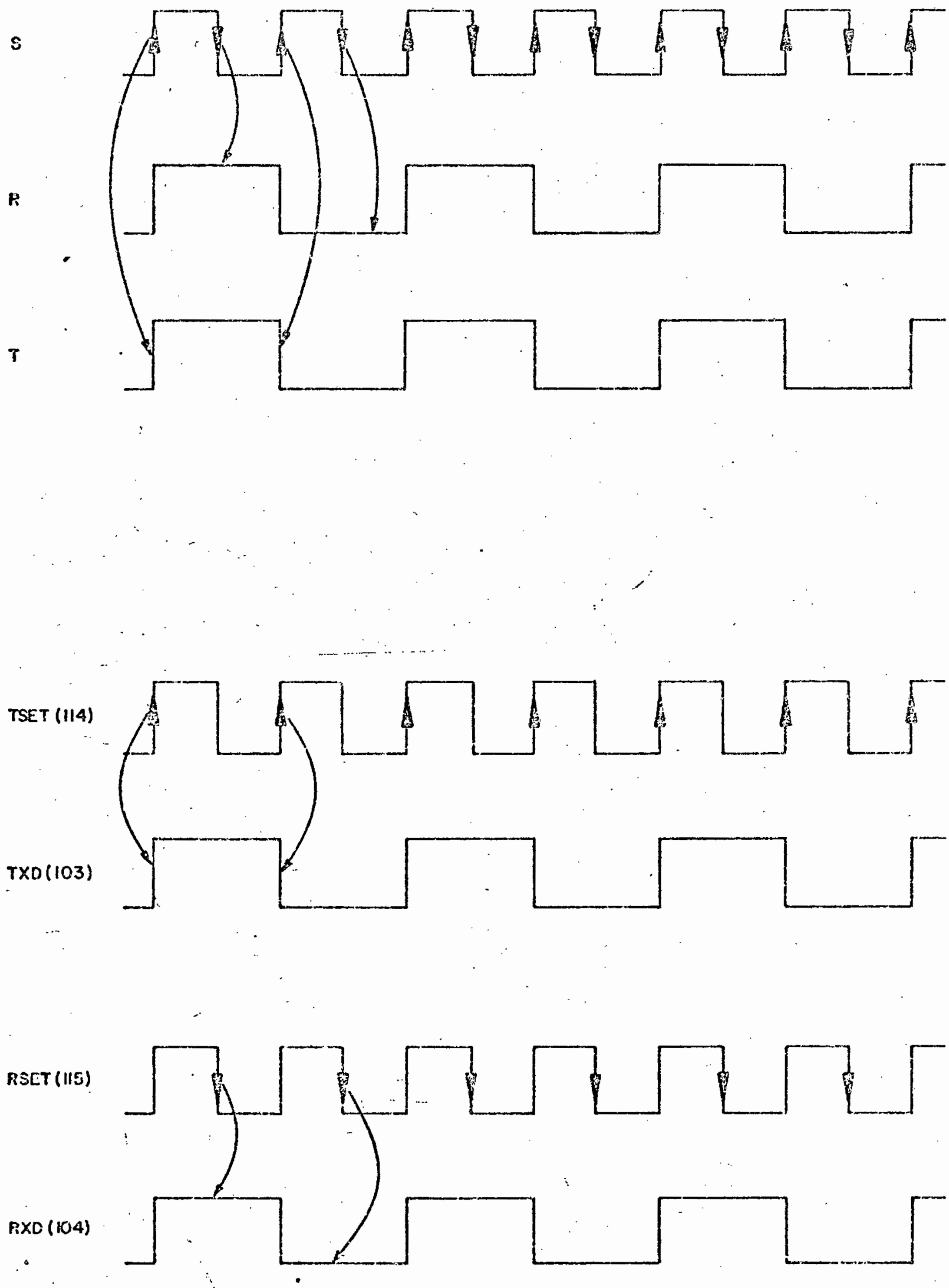
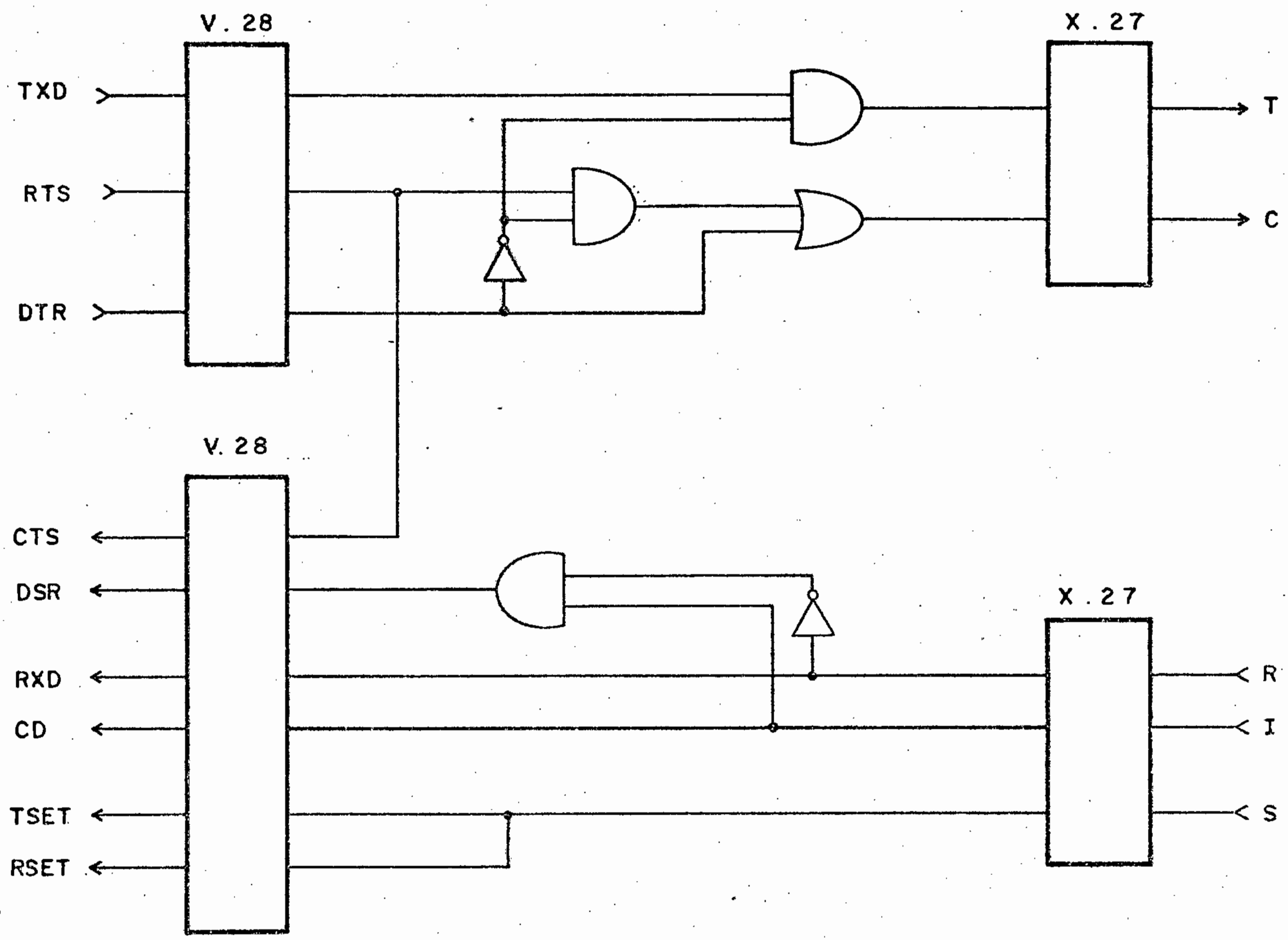
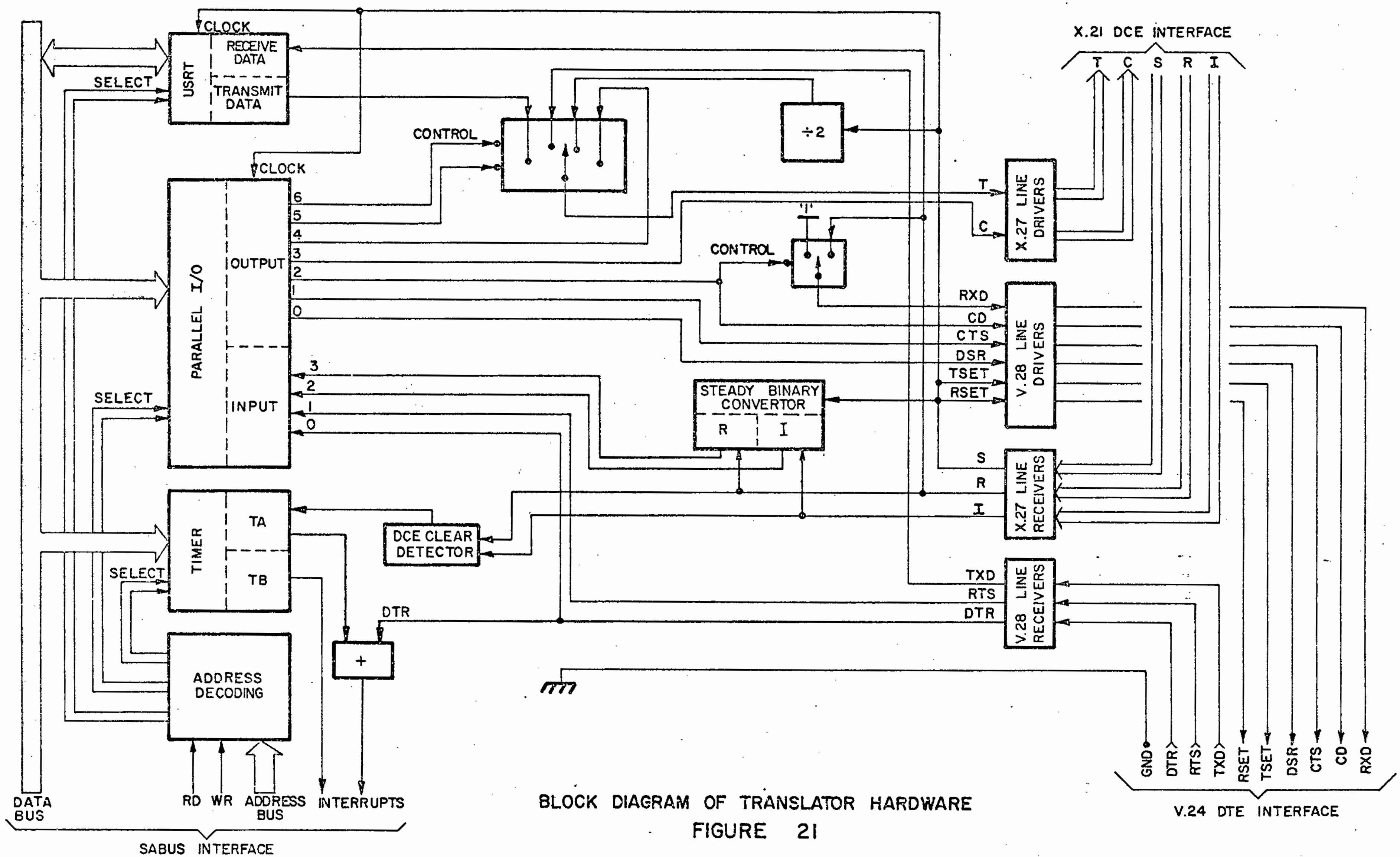


FIGURE 19
RELATIONSHIP BETWEEN X.21 AND V.24 TIMING INFORMATION



INTERFACE ADAPTOR FOR USE WITH A V.24 DTE CONNECTED TO A X.21 DCE USING A DEDICATED LINE INTERFACE.

FIGURE 20.



BLOCK DIAGRAM OF TRANSLATOR HARDWARE

FIGURE 21

$$\underbrace{\boxed{DDDD}}_{DNIC}\underbrace{\boxed{NNNNNNNNNN}}_{NTN}$$

DNIC = DATA NETWORK IDENTIFICATION CODE
NTN = NETWORK TERMINAL NUMBER
D,N = BCD digits

Figure A-1 : International Data Number

$$\underbrace{\boxed{ZXX}}_{DCC}\underbrace{\boxed{X}}_{N}$$

DCC = DATA COUNTRY CODE
N = NETWORK IDENTIFIER
Z = Any BCD digit from 2 to 7
0,1 are reserved
8 is used for interworking with the telex network
9 is used for interworking with the telephone network
X = Any BCD digit from 0 to 9

Figure A-2 : Data Network Identification Code

$$\underbrace{\boxed{DDD}}_{DCC}\underbrace{\boxed{NNNNNNNNNNN}}_{NN}$$

DCC = DATA COUNTRY CODE
NN = NATIONAL NUMBER
D,N = BCD digits

Figure A-3 : International Data Numbers for Integrated Numbering Schemes

APPENDIX A : FORMAT OF ADDRESS SIGNALS

The selection signals used to address endusers in a circuit-switched PDN using X.21, must conform to the international numbering scheme described by CCITT recommendation X.121. This recommendation describes the format of an international data number which may be up to 14 BCD digits long.

The first 4 digits of the international data number are known as the Data Network Identification Code (DNIC) and serve to uniquely identify a data network. The rest of the number, which may be up to 10 digits long, is known as the Network Terminal Number (NTN). (See figure A-1).

The first 3 DNIC digits serve to identify the country or geographical region in which a PDN is located. These digits are known as the Data Country Code (DCC). Each country is allocated 10 possible PDNs, which are identified by the fourth DNIC digit. (See figure A-2). Countries or regions with more than 10 PDNs qualify for a second DCC.

In countries where an integrated numbering scheme is used, the fourth DNIC digit is prefixed to the NTN, giving a National Number (NN) of up to 11 digits. (See figure A-3).

Inside a PDN or country, only the NTN or NN will be used to identify endusers. The numbering scheme used is a national matter, of which the CCITT should be kept informed. Outgoing calls from a PDN are indicated to the network by an international prefix or access code. Again, this prefixing is decided on a national basis and has no significance outside the PDN in question.

Each PDN must be able to interpret the DCC on an outgoing call, for routing purposes. Receiving countries or geographical regions must receive the complete international data number, suppressing the DCC when necessary.

APPENDIX B: FORMATS OF SELECTION AND DCE PROVIDED INFORMATION SIGNALS

The following description uses Backus-Naur Form as the formalism for syntactic description. A vertical line "|" separates alternatives.

<*> :: = IA 5 character 2/10
<+> :: = IA 5 character 2/11
<,> :: = IA 5 character 2/12
<-> :: = IA 5 character 2/13
<.> :: = IA 5 character 2/14
</> :: = IA 5 character 2/15
<n> :: = IA 5 characters 3/1, 3/2, or 3/3

The above signals are combined as follows:

<Address signal> :: = <Full address signal> |<.> <Abbreviated address signal>

<Address block> :: = <Address signal>|<Address block><,><Address signal>

<Facility registration/cancellation signal> :: = <Facility request code></> <Indicator> </> <Registration parameter></><Address signal>

<Facility registration/cancellation block> :: = <Facility registration/cancellation signal>| <facility registration/cancellation block> <,> <Facility registration/cancellation signal>

<Facility request signal> :: = <Facility request code>|<Facility request signal> </> <Facility parameter>

<Facility request block> :: = <Facility request signal>|<Facility request block><,><Facility request signal>

<Selection sequence> :: = <Facility request block><-><Address block> <+> | <Facility request block> <-> <+> | <Address block><+>|<Facility registration/cancellation block> <-> <+>

<Call progress block> :: = <Call progress signal><+> |<Call progress signal> <,> <Call progress block>

<Calling line identification> :: = <*><Calling line identification signal> <+>

<Calling line identification (with DNIC or DCC)> :: = <**><Calling line identification signal> <+>

<Called line identification block> :: = <Called line identification signal>|<Called line identification block><,><Called line identification signal>

<Called line identification> :: = <*><Called line identification block> <+>

<Called line identification (with DNIC or DCC)> :: = <**><Called line identification block> <+>

<Dummy line identification> :: = <*> <+>

<Charging information block> :: = </> <n> </><Charging information signal> <+>

APPENDIX C: CODING OF CALL PROGRESS SIGNALS

CODE GROUP SEE NOTE 1	CODE	SIGNIFICANCE	CATEGORY
0	00 01 02 03	Note 2 Terminal called Redirected call Connect when free	Without clearing
2	20 21 22 23	No connection Number busy Selection signals procedure error Selection signals transmission error	With clearing due to short-term conditions
4 and 5	41 42 43 44 45 46 47 48 49 51 52	Accessed barred Changed number Not obtainable Out of Order Controlled not ready Uncontrolled not ready DCE power off Invalid facility request Network fault in local loop Call information service Incompatible user class of service	With clearing due to long-term conditions
6	61	Network congestion	With clearing due to network short-term conditions
7	71 72	Long-term network congestion RPOA (Recognised Private Operating Agency) out of order	With clearing due to network long-term conditions
8	81 82 83	Registration/cancellation confirmed Redirection activated Redirection deactivated	With clearing due to DTE-network procedure

NOTE 1 - From the DTE point of view group 0 means "wait", groups 2 and 6 mean "try again, nexttry may result in a call set-up", groups 4 and 5, and 7 mean "there is no reason for the DTE to try again because the answer will be the same for a longer period of time". Since group 8 results from a procedure between the DTE and the network, no special action is expected to be taken by the DTE.

NOTE 2 - Reserved for future use.

APPENDIX D : X.21 BIS AND V.24; PIN ASSIGNMENTS AND INTERCHANGE CIRCUITS

D.1 X.21 PIN ASSIGNMENTS ACCORDING TO ISO 4903

PIN NUMBER SEE NOTE 2	INTERCHANGE CIRCUIT ASSIGNMENT X.21	
	X26	X27
1	See note 1	See note 1
2	T	T(A)
3	C	C(A)
4	R(A)	R(A)
5	I(A)	I(A)
6	S(A)	S(A)
7	B(A)	B(A)
8	G	G
9	Ga	T(B)
10	Ga	C(B)
11	R(B)	R(B)
12	I(B)	I(B)
13	S(B)	S(B)
14	B(B)	B(B)
15	Reserved for future international use	

TABLE D.1 : PIN ASSIGNMENTS FOR CCITT RECOMMENDATION X.21

CIRCUIT DESIGNATION	DESCRIPTION
G	Signal ground or common return
Ga	DTE common return
T	Transmit
R	Receive
C	Control
I	Indication
S	Signal element timing
B	Byte timing

TABLE D.2 : LIST OF INTERCHANGE CIRCUITS

NOTES

1. Pin 1 is assigned for connecting the shields between tandem sections of shielded interface cable. The shield may be connected either to protective ground or to signal ground at either the DTE or DCE or both in accordance with national regulations.

   Signal ground may be further connected to protective ground in accordance with national safety regulations. Caution should be exercised to prevent establishment of ground loops carrying high currents.

2. The pin assigments have been aligned to specify pairing and connection to multipaired interconnecting cable. Respective paired pins are 2 and 9, 3 and 10, ..., 8 and 15.

3. Where balanced circuits are concerned, the associated pairs are designated "A" and "B" in X.27.

D.2 V.24 INTERCHANGE CIRCUITS AND RECOMMENDED PIN ASSIGNMENTS ACCORDING TO ISO 2110

Circuit Number	Description
102	Signal ground or common return
103	Transmitted data
104	Received data
105	Request to send
106	Ready for sending
107	Data set ready
108/1	Connect data set to line
108/2	Data terminal ready
109	Data channel received line signal detector
110	Data signal quality detector
111	Data signalling rate selector (DTE source)
113	Transmitter signal element timing (DTE source)
114	Transmitter signal element timing (DCE source)
115	Receiver signal element timing (DCE source)
116	Select standby
118	Transmitted backward channel data
119	Received backward channel data
120	Transmit backward channel line signal
121	Backward channel ready
122	Backward channel received line signal detector
124	Select frequency groups
125	Calling indicator
126	Select transmit frequency
129	Request to receive
130	Transmit backward tone
131	Received character timing
132	Return to non-data mode
140	Remote loopback for point to point circuits
141	Local loopback
142	Test indicator
191	Transmitted voice answer
192	Received voice answer
201	Signal ground or common return
202	Call request
203	Data line occupied
204	Distant station connected
205	Abandon call
206	Digit signal (2^0)
207	Digit signal (2^1)
208	Digit signal (2^2)
209	Digit signal (2^3)
210	Present next digit
211	Digit present
213	Power indication

TABLE D.3 : V.24 INTERCHANGE CIRCUITS

PIN NUMBER	INTERCHANGE CIRCUIT NUMBER
1	See note 1
2	103
3	104
4	105
5	106
6	107
7	102
8	109
9	N
10	N
11	N
12	122
13	121
14	118
15	114
16	119
17	115
18	141
19	120
20	108 (see note 2)
21	140
22	125
23	111
24	113 (see note 3)
25	142

TABLE D.4 : PIN ASSIGNMENTS FOR CCITT RECOMMENDATION V.24

LEGEND : N - Pin number permanently reserved for national use.

NOTES

1. Pin 1 is assigned for connecting the shields between tandem sections of shielded interface cable. The shield may be connected either to protective ground or to signal ground at either the DTE or DCE or both in accordance with national regulations. Signal ground may be further connected to protective ground in accordance with national safety regulations. Caution should be exercised to prevent establishment of ground loops carrying high currents.
2. Either circuit 108/1 or 108/2.
3. In some countries pin 24 is allocated to another interchange circuit such as circuit 116 (select standby)

D.3 INTERCHANGE CIRCUITS FOR USE WITH X.21 BIS INTERFACES

V.24 INTERCHANGE CIRCUIT NO.	DESIGNATION
102	Signal ground or common return
103	Transmitted data
104	Received data
105	Request to send
106	Ready for sending
107	Data set ready
108/1	Connect data set to line
109	Data channel received line signal detector
114	Transmitter signal element timing (DCE)
115	Receiver signal element timing (DCE)
140	Remote loopback for point to point circuits
141	Local loopback
142	Test indicator (DCE)

TABLE D.5 : X.21 BIS INTERFACE FOR DEDICATED CIRCUIT USE

NOTE: CIRCUIT 108/1 SHOULD BE USED AS AN INDICATION THAT THE DTE IS OPERATIONAL

V.24 INTERCHANGE CIRCUIT NO.	DESIGNATION
102	Signal ground or common return
103	Transmitted data
104	Received data
105	Request to send
106	Ready for sending
107	Data set ready
108/1 or	Connect data set to line
108/2	Data terminal ready
109	Data channel received line signal detector
114	Transmitter signal element timing (DCE)
115	Receiver signal element timing (DCE)
125	Calling indicator
141	Local loopback
142	Test indicator

TABLE D.6 : X.21 BIS INTERFACE FOR SWITCHED CIRCUIT USE

APPENDIX E : DTE time-limits and DCE time-outs

E.1 DTE time-limits

Under certain circumstances this Recommendation requires the DCE to respond to a signal from the DTE within a stated maximum time. If any of these maximum times is exceeded, the DTE should initiate the action indicated in Table E.1. To maximize efficiency, the DTE should incorporate time-limits to send the appropriate signal under the defined circumstances summarized in Table E.1. The time-limits given in the first column are the maximum times allowed for the DCE to respond and are consequently the lower limits of the times a DTE must allow for proper network operation. A time-limit longer than the time shown may be optionally used in the DTE; for example, all DTE time-limits could have one single value equal to or greater than the longest time-limit shown in this table. However, the use of a longer time-limit will result in reduced efficiency of network utilization. The actual DCE response time should be as short as is consistent with the implementing technology and in normal operation should be well within the specified time-limit. The rare situation where a time-limit is exceeded should only occur when there is a failure in DCE operation.

TABLE E.1 DTE time-limits

Time-limit	Time-limit number	Started by	Normally terminated by	Preferred action to be taken when time-limit exceeded
3 s	T1	Signalling of call request (state 2)	Reception of proceed-to-select (state 3)	DTE signals DTE ready (state 1)
20 s	T2	Signalling end-of selection or DTE waiting (direct call) (state 5)	Reception of call progress signals, DCE provided information, ready for data or DCE clear indication (states 7,10,12 or 19)	DTE signals DTE clear request (state 16)
2 s	T3A	Reception of call progress signals, or DCE provided information (states 7 or 10)	Reception of ready for data or DCE clear indication (state 12 or 19)	
60 s	T3B (see note)	Reception of applicable call progress signals (state 7)	Reset by additional call progress signals, or DCE provided information (states 7 or 10)	

(CONTINUED OVERLEAF)

(TABLE E.1 CONTINUED)

Time-limit	Time-limit number	Started by	Normally terminated by	Preferred action to be taken when time-limit exceeded
2 s	T4	Change of state to call accepted (state 9)	Reception of ready for data or DCE clear indication (state 12 or 19) Reset by DCE provided information (state 10 bis)	DTE signals DTE clear request (state 16)
2 s	T5	Change of state to DTE clear request (state 16)	Change of state to DCE ready (state 21)	DTE regards the DCE as DCE not ready and signals DTE ready (state 18)
2 s	T6	Change of state to DTE clear confirmation (state 20)	Reception of DCE ready (state 21)	
200 ms	T7	Change of state to ready (state 1) when the charge information (state 10 bis) has been requested	Reception of incoming call (state 8)	DTE returns to normal operation and may note absence of Charge information (state 10 bis)

Note - 60 s (T3B) applies for manual answering DTEs.

E.2 DCE Time-outs

Under certain circumstances this Recommendation requires the DTE to respond to a signal from the DCE within a stated maximum time. If any of these maximum times is exceeded, a time-out in the DCE will initiate the actions summarized in Table E.2. These constraints must be taken into account in the DTE design. The time-outs given in the first column of the table are the minimum time-out values used in the DCE for the appropriate DTE response and are consequently the maximum times available to the DTE for response to the indicated DCE action. The actual DTE response time should be as short as is consistent with the implementing technology and in normal operation should be within the specified time-out. The rare situation where a time-out is exceeded should only occur when there is a failure in the DTE operation.

TABLE E.2 DCE time-outs

Time-out	Time-out Number	Started by	Normally terminated by	Action to be taken when time-out expires
36 s	T11 (see note 1)	DCE signalling of proceed-to-select (state 3)	DCE reception of end-of-selection signal	DCE will signal DCE clear indication (state 19) or transmit appropriate call progress signal followed by DCE clear indication (state 19)
6 s	T12	DCE signalling of proceed-to-select (state 3)	DCE reception of first selection character or in the case of direct call, DTE waiting (state 5)	
6 s	T13 (see note 1)	DCE reception of nth selection character (state 4)	DCE reception of (n + 1)th selection character or end-of-selection signal	
500 ms	T14A	DCE signalling of incoming call (state 8)	Change of state to call accepted (state 9) or call collision (state 15)	The DTE is noted as not answering. The DCE will signal ready (state 1).
60 s (see note 2)	T14B			
100 ms	T15	Change of state to DCE clear indication (state 19)	Change of state to DTE clear confirmation (state 20)	DCE will signal DCE ready and mark DTE uncontrolled not ready (state 24).
100 ms	T16	Change of state to DCE ready (state 21)	Change of state to ready (state 1)	DCE will mark DTE uncontrolled not ready (state 24)

Note 1 - T11 and T13 do not apply in the case of a direct call.
Note 2 - T14B will be provided when manual answering DTEs are allowed.

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