# Characterizing Single Event Upsets within the lpGBT-based End-of-Substructure Card


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Submitted to the Department of Electrical Engineering at the University of Cape Town in fulfilment of the academic requirements for a Master of Science degree in Electrical Engineering

**June 7, 2021**

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# Acknowledgements

To my supervisors Dr. Jane Wyngaard and Dr. James Keaveney who have supported me throughout this journey. I sincerely appreciate all the time and effort you gave to our weekly meetings, my questions on Mattermost, career advice and so much more. Thank you especially for patience during my many mistakes and set backs. Under your guidance I have learnt a tremendous amount which I am excited to use whilst pursuing a career in engineering.

To the ATLAS-DESY team who graciously answered all of my questions. I would like to give special mention to Dr. Rickard Ström and Dr. Stefan Schmitt for all your additional guidance and support. Thank you all for making me feel a part of team and for affording me the amazing opportunity to represent the team with a poster presentation at the IEEE Nuclear Science International Conference and for allowing me to contribute to your work. I am hopeful that you will find this research helpful.

To Dr. Tom Leadbeater and Dr. Tanya Hutton at the n-lab for their guidance and for allowing us to safely use the neutron source.

To my colleague and friend Max van der Merwe without whom this thesis would not be possible. Thank you for your patience, support and for creating a setup for which we could use to work remotely. I wish you only the very best in your research in find even more interesting behaviour with the system.

To my parents and brother, Matthew, for all your support and prayer during the year.

To my friends Ndumiso, Sama, Hobbes, Ben and Stefan for your great conversations, advice and motivation to finish.

Finally I would like to thank to God for His grace in helping me complete this research and being with me every step of the way.

# Abstract

The CERN ATLAS particle physics experiment is currently undergoing a significant system upgrade (ATLAS Phase II upgrade). As a result of the upgrade the experiment's Inner Tracker (ITk) and the front-end electronics of the ITk are being redesigned to handle increased data rates and a higher radiation environment. Within the ITk, the End Of Substructure (EoS) card is a new custom designed digital board that will provide the data, command, and power interface between on and off-detector electronics. Each EoS card makes use of one or two custom CERN designed low power Gigabit Transceivers (lpGBTs) ASICS that have been created for the purposes of supporting high bandwidth optical links in high radiation environments throughout CERN experiments. An estimated 1552 EoS cards will be installed in the ITk, each representing a potential point of failure. Given the complexity and quantity of new hardware designs involved, and that the EoS cards will be not be accessible or serviceable after the upgrade has been completed, there is a need for rigorous quality assurance (QA) and quality control (QC) testing.

This thesis therefore describes an independent test setup commissioned, by the author, at the University of Cape Town (UCT) Physics Department for characterising aspects of EoS card's operation under representative radiation conditions. Specifically, the radiation environment of the ITk poses a challenge to electronics as energetic particles can deposit their energy within the circuit material resulting in an erroneous change in logic known as a Single Event Upset (SEU). The lpGBT is a radiation tolerant ASIC and employs digital signal processing (DSP) and triple modular redundancy (TMR) techniques to mitigate against the effects of SEUs on transmitted data. This thesis presents an experiment setup which tests this hypothesis that the DSP stages are susceptible to data corruption caused by SEUs. In addition the setup also attempts to characterize the susceptibility of the scrambler, encoder, and interleaver stages within the lpGBT to SEUs. This experiment is carried out by actively irradiating an EoS card with a neutron source (energy spectrum of up to 11 MeV), while emulating each stage on a non-irradiated off-board FPGA. Additionally and in support of this experiment, the existing firmware and LabView automation software developed at DESY are extended.

Results from this thesis indicate that the DSP stages within the lpGBT are susceptible to data corruption caused by SEUs. It was also shown that the susceptibility of the experiment itself did not effect the measured SEU rates. Finally, preliminary results suggest that susceptibility of the DSP stages within the lpGBT can be characterized as the Bit Error Rate (BER) increases depending on the number of active stages.

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## 0.1 Abbreviations and Acronyms

| | |
|---|---|
| ASIC | Application Specific Integrated Circuit |
| BER | Bit Error Rate |
| CDR | Clock Data Recovery |
| CLPS | CERN Low Power Signalling |
| CML | Current Mode Logic |
| CMOS | Complementary Metal Oxide Semiconductor |
| CRC | Cyclic Redundancy Check |
| DAF | Detector Assembly Facility |
| DSP | Digital Signal Processing |
| EMI | Electromagnetic Interference |
| EoS | End of Substructure |
| FEC | Feedforward Error Correction |
| FELIX | Front End Link eXchange |
| FPGA | Field Programmable Gate Array |
| GBT | Gigabit Transceiver |
| GPIO | General Purpose Input Output |
| HL-LHC | High Luminosity Large Hadron Collider |
| ITk | Inner Tracker |
| lpGBT | low powered Gigabit Transceiver |
| NRZ | Non Return to Zero |
| OSI | Open Systems Interconnection |
| PCB | Printed Circuit Board |
| PRBS7 | Pseudo-Random Binary Sequence |
| QA | Quality Assurance |
| QC | Quality Control |
| RS | Reed Solomon [encoding] |
| SEE | Single Event Effect |
| SEU | Single Event Upset |
| SV | Sensitive Volume |
| TDAQ | Trigger and Data Acquisition |
| TID | Total Ionizing Dose |
| TMR | Triple Modular Redundancy |
| VCO | Voltage Controlled Oscillator |
| VI | Virtual Instrument |
| VL+ | Versatile Link Plus |

## 0.2 Nomenclature

| | |
|---|---|
| Cross-Section | Probability of an specific event occurring |
| Downlink | Data path from off-detector systems to front-end electronics |
| E-Link | Hardware layer used for communication between the front-end electronics and the lpGBT |
| EoS Card | Custom designed optical transceiver card which houses the lpGBT |
| Event | Interaction between elementary particles |
| Flux | Number of neutrons which pass through a given volume every second |
| Fluence | Flux integrated over time |
| HL-LHC | Upgrade to the LHC |
| I2C | Serial communication bus for short distance embedded systems communication |
| lpGBT | low powered Gigabit Transceiver responsible for serializing and processing data between the front-end electronics and off-detector systems |
| Parity | Redundant information appended to message for error detection and/or correction |
| Single Event Upset | Erroneous change in logic state cause by the passage of an energetic particle |
| SV | Sensitive Volume in which charge can collect and cause an erroneous change of logic |
| Thermal Neutrons | Low Energy Neutrons |
| Uplink | Data path from front-end electronics to off-detector systems |

## 0.3 Symbols

| | |
|---|---|
| $E_d$ | Energy Deposited |
| GF(p) | Galois Field |
| MeV | Mega Electron Volts |
| mod | Modulus function |
| n | Neutron particles |
| rad | Radiated absorbed dose |
| T | Tesla |

| | |
|---|---|
| $\alpha$ | Primitive element |
| $\gamma$ | Gamma particles |
| $\mu$ | Charge Mobility |
| $\phi(E)$ | Neutron fluence |
| $\sigma$ | Cross-section |

# Chapter 1

# Introduction

This thesis investigates the robustness of a custom designed transceiver card in the presence of radiation. This chapter provides background information regarding this transceiver and presents the hypothesis of this study. Chapter 2 builds technical knowledge for the operation of the card, the environment in which it operates as well investigate other similar studies. Chapter 3 provides background to the test setup used and the modifications to this setup is outlined in Chapter 4. The results of this study are discussed in Chapter 5. Finally the conclusion and recommendations for future work is provided in Chapter 6.

## 1.1 Background and Context

The Large Hadron Collider (LHC) is the world's most energetic proton-proton collider ever constructed. It accelerates and collides protons at high energies to observe the interactions between the subatomic particles. There are many different types of interactions, otherwise known as *events*, that can occur at varying probabilities referred to as *cross-section* $\sigma_p$. From studying the debris of these collisions the ATLAS experiment, at the LHC, aims to answer the fundamental questions about the workings of nature.

The High Luminosity LHC (HL-LHC) is the current major upgrade to the LHC, increasing the proton collision rate by an order of magnitude. The rate at which particle interactions can occur in a collider experiment depends on the intensity of the colliding beams and is quantified as Luminosity $\mathcal{L}$. Luminosity is defined in Equation 1.1 as the proportion of change in the number of events $R$ in relation to cross-section $\sigma_p$ [1]. The HL-LHC is designed to increase the luminosity of the collider to $\mathcal{L} = 7.5 \times 10^{34} cm^{-2} s^{-1}$ thereby increasing the number of events produced and hence increasing the data set collected [2].

$$\mathcal{L} = \frac{1}{\sigma_p} \frac{dR}{dt} \tag{1.1}$$

The ATLAS experiment will also undergo a major upgrade, referred to as the ATLAS Phase II upgrade, to maximally exploit this increase data rate and measure particle physics phenomena with greater precision. The most challenging aspect of the ATLAS upgrade is the complete replacement of the Inner Detector (ID). The ID is a *tracker* which estimates the momenta of charged particles by reconstructing their trajectories in a strong magnetic field. The ID is replaced by a new all-silicon Inner Tracker (ITk) and requires a redesign of the ATLAS Trigger and Data Acquisition (TDAQ) system. The HL-LHC increases the capabilities of the accelerator far beyond the LHC and hence various systems are being redesigned to cope in the new environment. The two challenges facing the ITk and TDAQ systems is managing the increased data rates whilst operating in a higher radiation environment as compared to the LHC. The Phase II upgrade is expected to be operational in 2026 [2].

The ITk consists of pixel detectors which are closest to the interaction point and is enclosed by strip detectors. These strip detectors are built with modules which consists of the sensor and one or two Printed Circuit Boards (PCBs), called hybrids, which host the readout Application Specific Integrated Circuits (ASICs). These front end modules are supported by carbon-fibre substructures. The substructures supporting the outer barrel are referred to as *staves* whilst those supporting the forward/backward end-cap regions (perpendicular to the beam) are referred to as *petals*. Bus tapes bonded to the substructure will provide power and signal distribution to the modules. The end of each stave and petal substructure will host an End-Of-Substructure card (EoS) illustrated in Figure 1.1, which will transfer data, power and control signals between the bus tapes and the off-detector electronics. In terms of the Phase II TDAQ system, the EoS card forms part of the front-end detector electronics as shown in Figure 1.2 [2]. In short, the EoS card facilitates the communication between the off-detector systems and front end modules, and is the subject of this thesis.

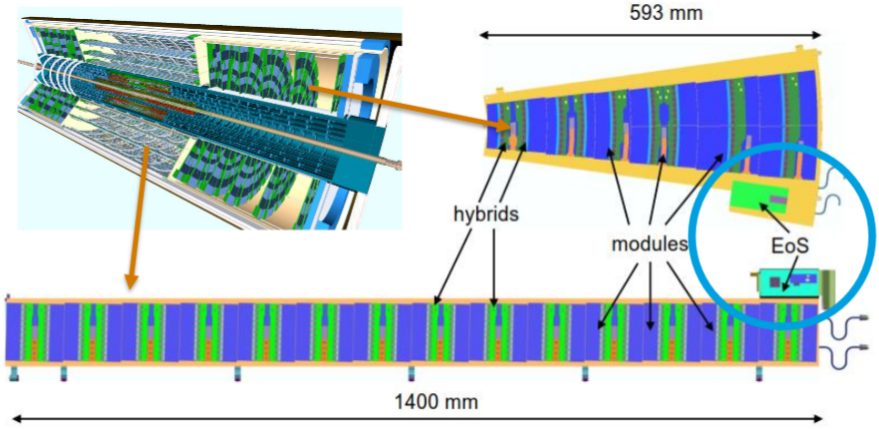



Figure 1.1: 3-D computer generated drawing of the ITk. Detail views of the stave and petal substructures are provided with their position in the ITk structure as indicated. The position of the EoS card in relation to Stave and Petal substructures is also indicated [3].

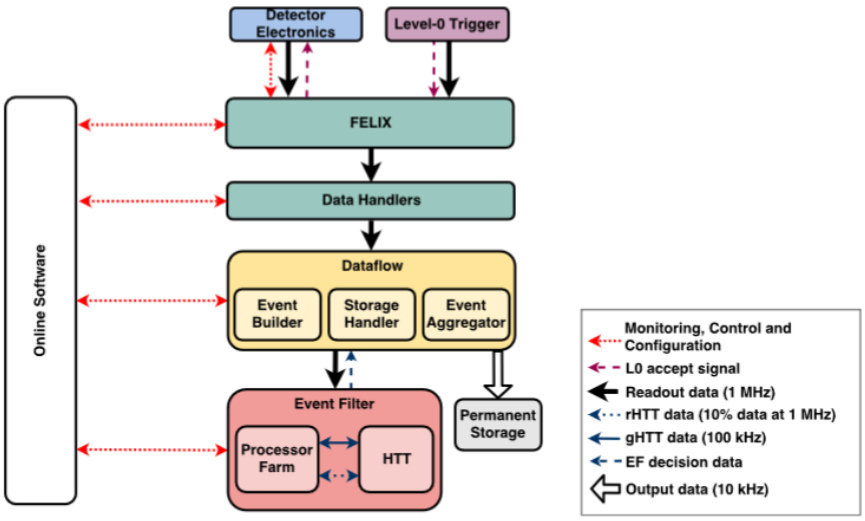



Figure 1.2: Functional overview of the TDAQ system, illustrating the data flow from the detector electronics and the permanent storage. The EoS card forms part of the detector electronics functional block in blue [2].

Figure 1.3 shows the EoS card connected to a stave which has 5 of the 14 short strip modules populated. The ITk strip detector system will house 1552 EoS cards. Each EoS Card represents a single point of failure for an entire petal or slave and will not be accessible or serviceable after the ATLAS Phase II upgrade has been completed [3], [4]. Hence extensive and thorough Quality Assurance (QA) and Quality Control (QC) testing is required before final installation.

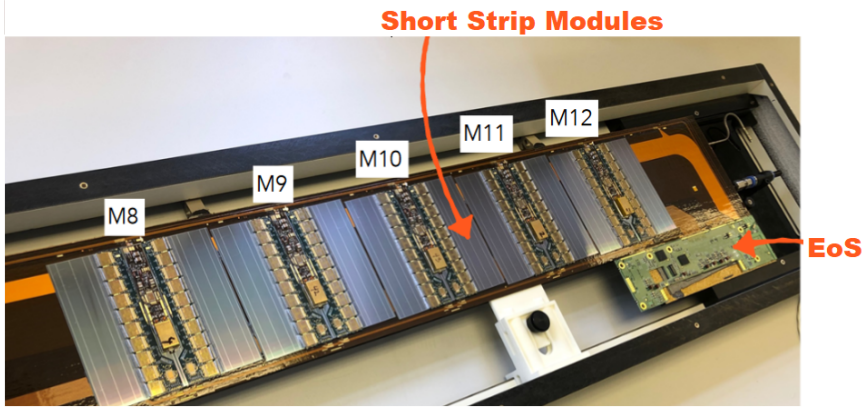
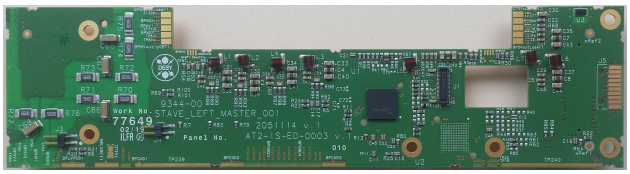
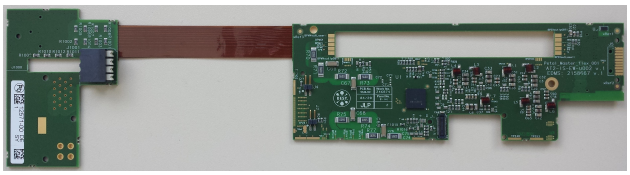



Figure 1.3: EoS card and 5 of the 14 modules populated on a stave substructure

A Master or Slave EoS card is hosted on one of either sides of the substructure and are connected via a High Density (HD) connector. Ten layouts of the EoS card are designed to satisfy the different geometrical requirements of the detector. Examples of layouts are given in 1.4.



(i) Stave Master EoS Card



(ii) Petal Master EoS Card

Figure 1.4: Two different examples of EoS cards with different geometrical layouts for the stave and petal substructures.

The EoS card connects up to 28 front-end (FE) electronics via "E-Link" data lines to one or two low powered Gigabit Transceivers (lpGBT), i.e. 14 E-Links per lpGBT. The lpGBT will be able to receive data from each E-Link at 640 Mbit/s and will serialize and digitally process the data to be transmitted via a 10 Gbit/s optical link to off-detector components ($28 \times 640$ Mbit/s (excluding control data) $\approx$ 10Gbit/s). This data path from front-end sensors to off-detector systems is referred to as the *uplink* channel. The reverse is known as the *downlink*.

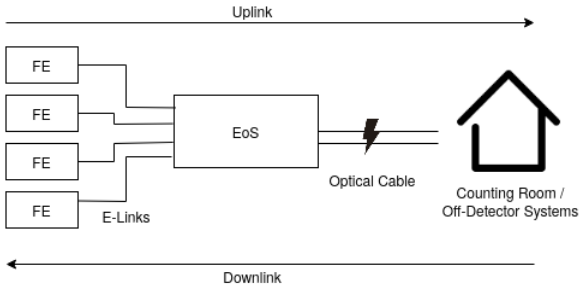



Figure 1.5: Figure illustrating the Uplink and Downlink data paths between the detector electronics and off-detector systems for the ITk detector within the ATLAS experiment at CERN. The EoS card serializing the data from multiple front end modules to a single optical channel is also shown

Alongside the lpGBT, the EoS is powered by a two stage DC-DC convertor which generates 2.5V and 1.2V and is mounted on a custom designed daughter board to meet physical constraints. A Versatile Link Plus (VL+) is responsible for the conversion between the electrical and optical signals. A populated EoS card with a DC-DC convertor, lpGBTs and VL+ are shown in Figure 1.6.

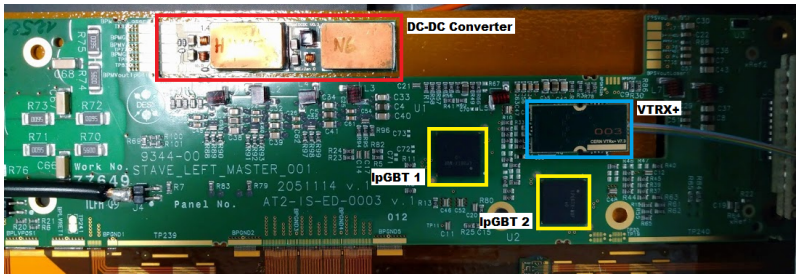



Figure 1.6: Figure identifying the active components on the EoS card. Specifically identifying the lpGBT ASICs in yellow.

A small number of prototype EoS cards has already undergone thorough testing and been through a dedicated quality assurance procedure at the Detector Assembly Facility (DAF) at DESY, Hamburg. The tests performed include: testing under extreme temperatures ($-40°C$ to $30°C$), testing on populated sub-structures (See Figure 1.3), performance testing under 2 Tesla magnetic field, and performance testing after prolonged irradiation with a Cobalt-60 source. The signal quality tests are of particular interest and are performed with the aid of an Xilinx Kintex-7 Field Programmable Gate Array (FPGA) with built-in optical transceiver modules.

The FPGA, in the aforementioned signal quality tests, acts as an experiment test bench for the EoS card under test. The FPGA is used to generate a pseudo-random binary sequence (PBRS7), which simulates the data generated by the front-end module sensors and is transmitted to the EoS card at 640 Mbit/s per E-Link. After serializing and processing the data the EoS card transmits the data optically back to the FPGA which compares the received data to generated data, counting the Bit Error Rate (BER). A BER shown in Equation 1.2 is defined as the ratio of erroneous bits received to total number of bits transmitted. Alongside executing the Bit Error Rate test, the FPGA test bench may act as an I2C Master to enable configuration of the lpGBT and VL+ configuration registers.

$$\text{BER} = \frac{\text{No. Erroneous bits received}}{\text{Total bits received}} \tag{1.2}$$

## 1.2 Hypothesis

As previously mentioned, past testing of the EoS electronics and the lpGBT ASIC has included testing the operation of the ASIC after exposing it to its lifespan equivalent dose of radiation. This is accomplished by first irradiating the card for approximately 52 days using a Cobalt-60 source and then testing the performance. No electrical or functional issues were found after running a BER test with the irradiated card. This research presents a complimentary experiment which performs the BER test whilst actively irradiating the lpGBT ASIC with a neutron source. As such, this experiment does not test the deterioration of the ASIC material

due to radiation exposure but tests whether the EoS card is susceptible to temporary upsets (known as Single Event Upsets [SEUs]) in the data flow. A simplified overview of this experiment setup is presented in Figure 1.7.

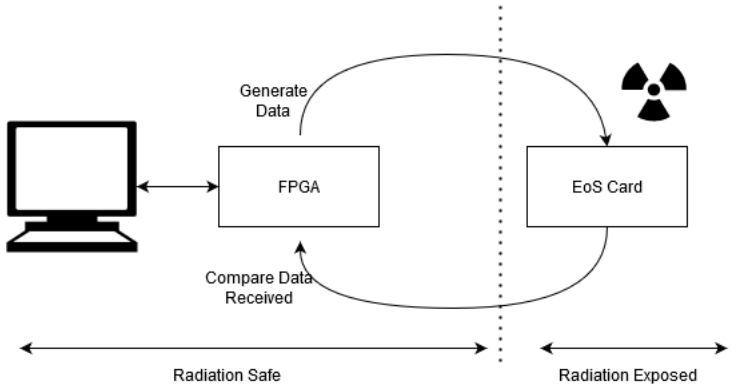



Figure 1.7: Functional overview of experiment showing FPGA test bench generated data for an actively irradiated EoS card and then comparing the received data producing a BER which can be monitored from a control PC.

One of the primary functions of the lpGBT is to apply digital signal processing (DSP) techniques to the data to ensure reliable transmission across the *optical link* to and from the off-detector systems. These DSP stages help mitigate against sources of signal disruption during transmission, however the stages themselves are susceptible to SEUs. This thesis presents a hypothesis that the lpGBT DSP stages are susceptible to data corruption via SEUs. This thesis presents a test setup which not only tests this hypothesis but also capable of characterizing the susceptibility of the individual stages.

This setup is realized by first replacing all the DSP stages with radiation immune replacement hardware on the FPGA test bench. This experiment then incrementally re-introduces these stages to the irradiated lpGBT and removing the radiation immune counterpart to keep the data path intact. The results from these incremental tests then aids in the effort to characterize susceptibility of the individual DSP stages of the lpGBT. The DSP techniques used are used in conjunction with Triple Modular Redundancy (TMR) architecture. Hence this experiment setup accounts for the effects of TMR as well as the susceptibility of the FPGA test bench in characterizing the DSP stages.

## 1.3 Scope and Limitations

- The lpGBT is a highly versatile ASIC which allows the user to modify the configuration of multiple sub-components involved in the transmission of data. These include changing the Forward Error Correction (FEC) encoding, scrambler configuration, data rate and number of data channels. This investigation

is limited to using the configuration intended for use in the ITk and does not investigate the impact of altering the configuration of these sub-components. This experiment is performed with the uplink data rate set to 10.24 Gbps and the encoding scheme set to FEC5.

- The EoS card is a highly interconnected system connected to all front end modules/electronics, DC-DC converter, and housing various components including the lpGBT and VTRx+ optical transceiver. While bit errors can be introduced at multiple points in the system, this setup is focused on the characterization of errors within the lpGBT only, with reasonable measures taken to correct for other potential sources of error.

- This experiment assumes its execution is carried out in an environment that is representative of the expected operating environment in the ITk. This includes: a stable room temperature environment, no significant EM interference, and stable power supplies.

- To minimize the uncertainty of data corruption occurring with the E-Links due to SEUs, the EoS card will be tested without the E-Links. This setup is different to that of the DESY experiments and presented limitations to the randomness of the pattern used. These limitations are discussed fully in Section 4.3.

- This work modifies or extends the work done by the ATLAS-DESY team. All work was done in consultation with them.

## 1.4 Chapter Summary

In summary the HL-LHC and ATLAS Phase II upgrade presents two challenges to electronic systems design, namely; increased data rates and increased levels of radiation exposure. This thesis presents a hypothesis that the lpGBT, and the DSP stages within, is susceptible to data corruption caused by SEUs. This experiment hopes to characterize the lpGBT's susceptibility to SEUs in real time under representative conditions. Results from this investigation will provide recommendations on possible lpGBT configuration settings, and PCB layout such that it may reduce the SEU rate in future iterations of the lpGBT or EoS.

# Chapter 2

# Literature Review

Chapter 1 presented a brief overview of the intended operation of the EoS within the ITk upgrade and the hypothesis of this thesis. Given this hypothesis the following chapter will build on the theory required to effectively design the experiment. Descriptions and results for similar past investigations on the SEU rate for various electronic devices will also be given. Alongside their experimental results, alternative simulation methods and their limitations to quantify electronic device susceptibility to SEUs will also be explored. Finally this section describes the current techniques employed by the lpGBT to mitigate against radiation effects.

## 2.1 Introduction to Digital Communication Theory

The EoS card facilitates the transportation of digital data between the front-end modules to the off-detector systems (also referred to as the *"counting room"*). This Section will discuss the implementation of various OSI (Open Systems Interconnection) layers on the EoS card as are relevant to this research. The OSI model provides a standardized framework to describe the concepts for digital communication. Reliable data transmission ensures the message transmitted correctly appears at the receiving node. Each layer provides functionality for the receiver to correctly receive and interpret the signal to recover the transmitted message. To achieve the required performance, in a number of cases CERN has internally developed custom solutions as opposed to using more widely used industry standards. These are described in the following sections. Specifically, the EoS supports custom optical interface layers for the off-detector systems as well as a low bandwidth digital interface, for the front-end modules, termed *E-Links*. The characteristics of each is summarized in Table 2.1 and described in the following sections. Although the E-Link interface will not be used in this experiment, the reason for which is given in Section 4.3, the physical layer is still discussed providing context to the EoS card configuration and hence the testing configuration.

| OSI Model | Optical Link | E-Link |
|---|---|---|
| Physical Layer | Custom Line Code to Laser Driver<br>Clock Extraction<br>Equalizer | CERN Low Power Signalling (CLPS)<br>Dedicated Clock Line |
| Data Link Layer | Reed-Solomon Encoding<br>Scrambling<br>Interleaving<br>GBT Protocol | Does not impact the work of this thesis |

Table 2.1: Summary of the OSI Layers and Subsequent Protocols Discussed

### 2.1.1 Physical Layer

The physical layer is the lowest OSI layer and refers to the physical characteristics of the transmission medium such as the voltage amplitudes, transfer rate and maximum distance [5]. A look into the physical characteristics of the optical link and E-Link interfaces hopes to provide an intuition on how these interfaces are realised from a first principles basis, enabling later discussion into the EoS card setup in the ITk and digital signal processing techniques employed by the EoS card.

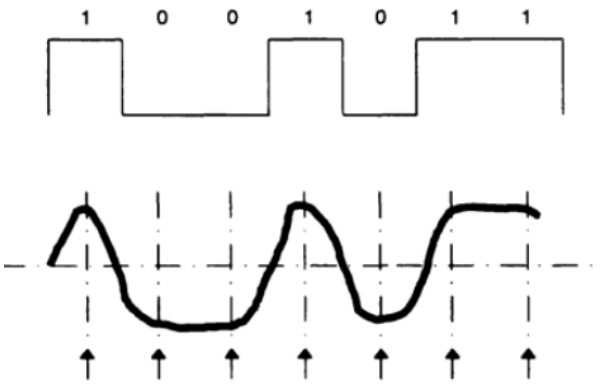



Figure 2.1: Example of digital data represented as a bitstream being mapped to an analogue signal for transmission [6]

#### Line Codes

Information represented as a bit sequence will need to be mapped to a physical waveform signal. For example a bit can be mapped to a voltage value (voltage mode), current value (current mode) or optical signal which can then be transmitted through a physical channel. This mapping is referred to as a line, or channel, code and is illustrated in Figure 2.1. The choice of line code affects physical properties such as power and

bandwidth usage. The line codes utilised by the EoS are described below.

**E-Links** The EoS card interfaces with two different physical network mediums; E-Links provide a low bandwith command and control connections to the front-end, while a high bandwith optical link provides the data path to the off-detector systems. On the EoS the E-Links are divided into groups with each group containing up to 4 channels. The number of active channels depends on the configuration. The E-Links use CERN's Low Power Signalling (CLPS) which offers a maximum data rate per channel of 1.28 Gbps (Non Return to Zero [NRZ] signalling) [7]. In the case of the EoS, the E-Links are configured such that one E-Link group generates data for 2 E-Link channels at 640 Mb/s. See Section 4.3. With all 8 E-Link groups active, the total data rate is 10.24 Gbps.

**Optical Link** Communication between the off-detector systems and EoS is realized through optical links. The optical signal is driven by current mode logic (CML) signals to a laser driver within the optical transceiver module. Current Mode Logic (CML) levels are shown to be suitable for applications in fast, low power devices such as the EoS card [7], [8]. There is a possible bandwidth limitation between the line driver and the laser driver as a band-limited transmission line will attenuate high frequencies before reaching the input of the laser driver. To combat this attenuation, modulator and pre-emphasis stages are added in parallel before reaching the laser driver. Both stages converts the serial data signal to current whilst the pre-emphasis stage also generates a signal with spectral contents at high frequencies. This is accomplished by adding an inverted, scaled and delayed signal to the original serial data line [7]. The resulting signal after pre-emphasis will then have a high amplitude and narrow pulse width at the start of each bit and for every bit transition as depicted in Figure 2.2.

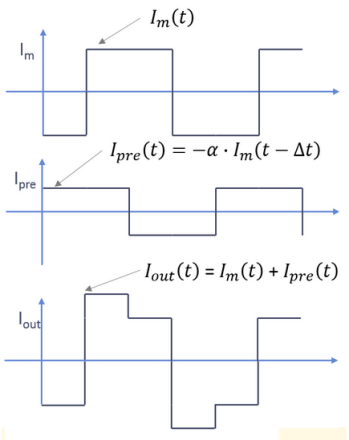



Figure 2.2: Illustration of the Pre-Emphasis Algorithm used by the lpGBT laser driver to combat attenuation due to transmission along the optical line [7]

### Clock Extraction and Timing

Clock extraction as defined by [6] is the process of extracting a synchronizing signal to enable better decisions. Figure 2.1 shows that a receiver is most likely to correctly interpret the RF signal when sampling at the correct frequency and when the sampled value is furthest from the threshold/decision value. As is the case with any line coding scheme, the sampling time is vital to reliable digital transmission. Timing information can either be extracted from the incoming data stream (reference-less) or supplied by a reference external clock synchronizing the transmitter and receiver.

**E-Links** The E-Links transmit a dedicated clock signal in conjunction with data. This enables communication between the EoS and front-end modules to be synchronized.

**Optical Links** There is no dedicated clock signal transmitted optically between the EoS and off-detector systems. Data and clock recovery on the EoS are done with the aid of a LC-Tank Voltage Controlled Oscillator (VCO) which begins oscillating at frequency upon startup. The VCO frequency is then calibrated, to match the desired frequency, as illustrated in Figure 2.3. Reference-less clock recovery is possible if the downlink signal is Non Return to Zero (NRZ) and DC-balanced (i.e. equal number of ones and zeros). In the test setup the EoS card extracts timing information (reference-less) from the downlink data stream.

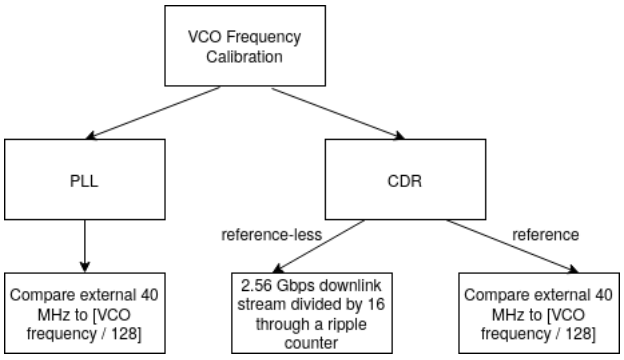



Figure 2.3: Overview of the different techniques the lpGBT employs to extract timing information from the optical link. The EoS card will recover the clock signal through reference-less Clock Data Recovery (CDR) circuit mode

In reference-less mode, comparing the two frequency signals is done using counters clocked by the two signals respectively and are raced against each other. If the counter from the VCO finishes first (i.e. the VCO frequency is higher), then frequency is decreased by increasing the capacitance of the oscillator. The depth of these counters can be calibrated for higher precision. See Figure 2.3.

In reference-less CDR mode, as used in this experiment's setup, the frame aligner (See Section 2.1.2) provides the lock signal.

#### Equalizer

Signals traveling along the communication channel could result in attenuation of the signal as well as introduce Inter-Symbol Interference (ISI) as symbols begin to overlap due to the frequency response of the channel. The equalizer therefore restores the signal levels as well as restore spectral content to reduce the amount of ISI and jitter resulting in an improved BER [7].

**Optical Link** As previously mentioned, the optical interface is driven by a current mode logic (CML) signal. Optical information is received on differential signal pins (HSINP and HSINN) before passing through the equalizer restoring the CML levels. The lpGBT offers the ability to tune the equalizer such that the optimal performance is achieved.

**E-Links** Features programmable equalization that is configured through lpGBT registers. The details of which are not relevant to this thesis.

### 2.1.2 Data Link

The Data Link Layer is the second layer in the OSI model which specifies how the data will be mapped to the physical layer. It is responsible for ensuring reliable data transmission over unreliable physical communication lines [5]. The ITk poses a harsh environment for the EoS card and data lines increasing the likelihood of an external disturbance during transmission. The EoS makes use of the lpGBT ASIC which is responsible for the Data Link layer by applying DSP techniques on the transported data to protect against the disturbances when traveling along the optical link only. Disturbances could cause a single erroneous bit flip or effect multiple consecutive bits known as a *burst error*. These DSP techniques map to individual stages within the lpGBT. The hypothesis of this experiment is that these stages are susceptible to data corruption due to SEUs. Thus the techniques employed by these stages is described to further develop an experiment to test the hypothesis.

In the case of the E-Links, the specifics of the data layer does not impact the work of this thesis, and the interaction between the Front-End modules and EoS was not examined.

#### Feed-forward Error Correction

Feed-forward Error correction is a encoding technique which allows for the detection and correction of errors received in a packet due to a noisy transmission channel. As mentioned previously the lpGBT ASIC is responsible for applying this encoding technique. The lpGBT designers elected to implement Reed-Solomon encoding [7] which is therefore describe here. Reed–Solomon (RS) encoding makes it possible for a receiver to detect and correct multiple symbol errors in real-time for the cost of adding additional parity bits. The capabilities and limitations of RS encoding is exposed by summarizing the theory behind this technique.

Understanding the limitations of RS encoding enables more thorough interpretation of the Bit Error Rate results.

RS codes are built on the underlying principles of finite fields otherwise known as *Galois Fields* (GF). Finite fields are defined as a set of elements for which the arithmetic operations: addition and multiplication between any two elements obey the following criteria:

- Associative
- Commutative
- An inverse element exists
- Closed. That is to say that performing an arithmetic operation on any two elements within the set will produce a result that is contained within the set.

It is this last criteria which differentiates finite fields from the typical addition and multiplication operations between any two natural numbers. Finite fields are defined as $GF(n)$ where $n$ indicates the number of elements within the field starting from 0. The simplest finite field to consider is $GF(2)$ which contains the elements 0 and 1. The addition and multiplication operations are therefore defined in Equations 2.1 and 2.2 respectively. It is interesting to note that addition and multiplication in $GF(2)$ correspond to and represented by XOR and AND logic gates respectively.

$$a \oplus b = (a + b) \bmod 2 \tag{2.1}$$

$$a \odot b = (ab) \bmod 2 \tag{2.2}$$

With these structures in mind consider a larger finite field $GF(16)$. This field could contain elements which correspond to the natural numbers 0 to 15. However the elements could be used to represent coefficient of a polynomial $i(x)$. For example the 6th element could have a binary representation of $0110_2$ and therefore represent $0X^3 + 1X^2 + 1X^1 + 0X^0$. It is for this reason finite fields are expressed as $GF(p^n)$, where $p$ is some prime number and $n$ is a positive integer, given the simplicity of finding roots of polynomials with degree $p$. In the previous example $GF(16) = GF(2^4)$. Finally every element within the set is labelled $\alpha_i$.

Any polynomial is the product of its irreducible polynomials whereby an irreducible polynomial can only be divisible by 1 and itself. This is analogous to prime factorization of natural numbers. Additionally, for any finite field $GF(p^n)$ one can define a primitive polynomial which can be used to generate all other elements within the field. Generation of a field is done with a primitive polynomial and some primitive element $\alpha^i$. For $GF(2^1)$ the choice of $\alpha$ is 0 or 1. Primitive polynomials have a special property of generating all the elements in the finite field in a cyclic but pseudo-random nature. This is property is dependant on the choice of $\alpha$ as different primitive elements will produce isomorphic fields. The special property of primitive

polynomials led to the application of Linear Feedback Shift Registers (LFSRs) used to implement RS codes digitally.

The transmitted message is intuitively defined by Equation 2.3, where $X^{n-k}$ shifts the bits of message word $M(x)$ such that they don't overlap with appended parity check symbols $CK(x)$. Parity check symbols $CK(x)$ is calculated as the original message $M(x)$ modulo the generator polynomial $G(x)$ as shown in Equation 2.4.

$$C(X) = X^{n-k}M(X) + CK(X) \tag{2.3}$$

$$CK(X) = X^{n-k}M(x) \bmod g(x) \tag{2.4}$$

RS codes requires 2 parity check bits to locate and correct the value of an error $E(X)$ from the received word $R(X)$ (see Equation 2.5, hence the Equation 2.6 defines the number of errors $t$ any given RS(n,k) can correct. It is desirable for $t$ to approach n (i.e. correctable symbols is equal number of symbols in original message) whilst maximising the code rate $r = k/n$. The decoding process is summarized into the following 5 stages [9]:

1. Calculating syndrome components $s(X)$ (i.e. components which characterize an error)
2. Find error-locator polynomial $\sigma(X)$
3. Locate the errors using error-locator numbers $x_i$
4. Calculate the error values $y_i$ and hence estimate error $E(X)'$
5. Find decoded word $C(X)'$

$$R(X) = C(X) + E(X) \tag{2.5}$$

$$n - k = 2t \tag{2.6}$$

Two ways to calculate the syndrome are described in [9]. The process of calculating the syndrome is labeled as a Cyclic Redundancy Check (CRC) in the setup. In the case of the lpGBT the first of these methods as shown by Equation 2.8 where $R(X)$ is the received word and, as previously discussed, $\alpha^i$ is a chosen primitive element is used to calculate the first and second syndromes. The error locator polynomial and its reciprocal (preferred as its roots are more easily found) are defined as $\sigma(X)$ and $\sigma_r(X)$ respectively. The error locator polynomial is found using the Berlekamp's algorithm however for simplicity consider $\sigma(X)$ as the Greatest Common Denominator between $S(X)$ (See Equation 2.7) and $X^{2t}$ found using Euclid's Division Algorithm. Syndromes $S_i$ are related to error values $y_i$ by the set of linear Equations 2.9, and can be solved directly. In the case no error has occurred, the syndrome calculated will be zero.

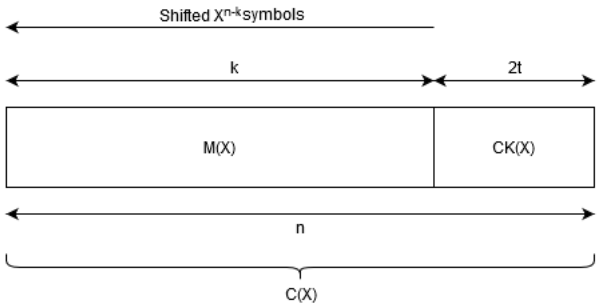



Figure 2.4: Graphical depiction of coding message structure showing the message being shifted by up and the appended parity bits. The widths of the of different parts of the message is also shown.

$$S(X) = \sum_{i=0}^{2t} S_i X^{i-1} \tag{2.7}$$

$$S_i = R(\alpha^i) \tag{2.8}$$

$$S_i = \sum_{j=1}^{t} y_j {z_j}^i \tag{2.9}$$

The roots of $\sigma_r(X)$ are labeled as $z_i$. Finally with the error values and error locations can be approximated with Equation 2.10 and hence the corrected code-word $C(X)$ is determined with Equation 2.11.

$$E(X)' = \sum^{T} y_i x_i \tag{2.10}$$

$$C(X)' = R(X) + E(X)' \tag{2.11}$$

RS encoding corrects an entire symbol regardless if one bit or multiple bits are erroneous. It is for this reason RS encoding works well in correcting burst errors as long was the number of bits in error are $\leq t$.

**Scrambling**

As previously mentioned, reliable digital transmission occurs when the receiver correctly evaluates the incoming RF signal at its expected peaks and at the correct frequency. Digital communication links that do not transmit the clock on a dedicated line make use of clock extraction on the data line to keep the clock rate synchronised between the transmitter and receiver. The techniques mentioned for clock extraction rely on frequent bit transitions (ideally these transitions will mimic the transmission frequency). Extended sequences of either zero or one bits on a data line could result in an incorrect extracted frequency resulting in increasing clock drift and increased potential for misreading data. A scrambler is a circuit which pseudo-randomizes

the data to increase the number of bit transitions that occur within the transmitted data thereby enabling a more accurate clock extraction and greater synchronisation of clocks between devices.

The uplink scrambler in the lpGBT on the EoS pseudo-randomizes the transmitted data frame for the the off-detector systems. For the uplink data path, operating at 10.24 Gbps, three 58 bit order 58 scramblers and one 60 bit order 58 scrambler are used. Equation 2.12 provides the recursive equation for the uplink scrambler.

$$S_i = D_i \text{ xnor } S_{i-39} \text{ xnor } S_{i-58} \tag{2.12}$$

**Interleaving**

Digital connections that are anticipated to be subject to burst errors (such as the EoS Optical link) commonly make use of a further standard technique for reducing errors. Specifically, Forward Error Correction (FEC) systems work more effectively when the signal is passed through an interleaver.

An uplink transmission speed at 10.25Gbps with FEC5 will use two RS(31, 29) encoders with a symbol bit-width of 5 bits. Interleaving the output of these two encoders will increases the maximum correctable burst error to a size of 10 bits. This is accomplished as interleaving breaks up and rearranges the message as shown in Figure A.2. Splitting the message, spreads the burst error to affect a smaller portion of symbols increasing the effectiveness of the error correction. For example an encoding scheme that can correct $t = 1$ symbols with symbol bit-width of 5 will lose the whole message if a burst error with bit-width of 6 bits occurred. However no information is lost if the same burst error affected 3 bits of 2 different messages despite the number of erroneous bits being the same. The interleaving algorithm is dependant on the size of the frame (the lpGBT changes the size of the message frame depending on uplink transmission speed) and the FEC scheme. The RS FEC encoder can correct up to $t$ symbols for every $n$ symbols. Considering the bit-width within the lpGBT is 5 bits this provides error correction capabilities of up to 10 bits.

**GBT Protocol**

Front-end electronics use the Gigabit Transceiver (GBT) protocol to interface with the Front End Link eXchange (FELIX) components, as discussed previously. The protocol specifies the frame structure of the transmitted data from the GBT. Depending on the data path, namely uplink or downlink path, the protocol is as follows:

**Uplink** The structure of the uplink data frame is dependent on the configuration of the lpGBT. Configured to be transmitting at 10.25 Gbps and using FEC5 encoding, the structure of the uplink data frame consists of a total of 256 bits. The first 2 bits are reserved for the header. The next 10 bits are reserved for the Internal Control (IC) data and is explained below. The next 224 bits are for the data transmitted from

the FE modules (via E-Links). There are two bytes (16 bits) for 14 E-Links. Finally leaving 20 parity bits from the encoder. See Figure A.1. With a total of 256 bits per frame, the lpGBT is configured to transmit $40 \times 10^6$ frames per second [10].

It must be noted that the 10 bits IC data and E-Link data (totalling 234) are scrambled before being inserted into the frame. The parity bits are calculated from these scrambled bits effectively protecting both the IC data and E-Link data. Finally after passing through the interleaver the structure is rearranged and is illustrated in Figure A.2.

**Downlink** Although similar to the uplink, the downlink frame structure consists of 64 bits. The header, IC and EC are expected to be already be "interleaved" before passing through the interleaver and will make up the 8 bits. Four bytes (32 bits) are reserved for data with each byte corresponding to one of four E-Link groups. The final 24 parity bits are introduced after encoding. The downlink frame structure for before and after interleaving are illustrated in Figures A.3 and A.4 respectively.

**Internal Control (IC)** The downlink and uplink frames have 2 dedicated Internal Control (IC) bits for the internal register configuration of the lpGBT. Reading and writing register data require the lpGBT be configured in transceiver mode, i.e. both the downlink and uplink channels are operational. These IC bits are collected (demultiplexed) to form 8-bit words. The frame constructed from these words will have the structure outlined in Figure 2.5. Register access can also be achieved using the lpGBT I2C interface. When configuring via I2C, the IC field is set to $2b'11$ [7]. Thus experiment requires register access with both the optical and I2C interfaces.

| ID | Description | Parity check |
|---|---|---|
| A | Frame delimiter 8'b 01111110 | No |
| B | Reserved | No |
| C | lpGBT address (7 bits) + R/W bit = 0 | No |
| D | Command [7:0] | Yes |
| E | Number of data words n[7:0] | Yes |
| E | Number of data words n[15:8] | Yes |
| F | Memory address [7:0] | Yes |
| F | Memory address [15:8] | Yes |
| G | 1st data (8 bits) | Yes |
| G | . . . | Yes |
| G | nth data (8 bits) | Yes |
| H | Parity word (8 bits) | Yes |
| A | Frame delimiter 8'b 01111110 | No |

Figure 2.5: Frame Structure after the IC bits have been collected and thus illustrating how register configuration via optical link of the lpGBT is realized [7].

## 2.2 The challenging environment of the HL-LHC

As discussed, the EoS card forms part of the HL-LHC upgrade which aims to increase the energy collisions within the collider to $13TeV$. Increasing the capabilities of the LHC will increase number of collisions performed increasing the physicists ability to detect particles which only exist in extremely short fractions of time. Figure 2.6 provides an indication of the expected radiation within the ITk outer barrels as a function of distance from the beam [11]. There are 3 sources of radiation, as identified by [12], which can effect the performance of the electronics namely:

- Collision debris
- Interactions of beam with collimaters (device which narrows beam)
- Beam residual gas interaction

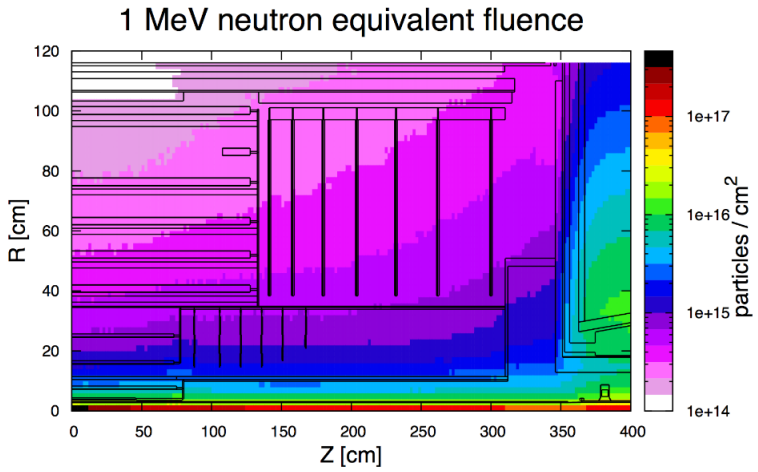



Figure 2.6: The expected radiation levels in the ITk expressed as a 1MeV neutron equivalent fluence as a function of distance from the beam [11]. It is seen that the fluence drops by orders of magnitude within a few cm from the beam however it is still a significant challenge to the front-end electronics

Radiation exposure introduces two challenges for electronic devices. They must overcome long-term failure due to Total Ionizing Dose (TID) which degrades the physical structure of the device whilst also overcoming instantaneous Single Event Effects (SEEs) which suddenly upsets the performance of the device. Subsection 2.2.1 will provide an introduction to the nuclear mechanisms which are common to both TID damage and SEEs whilst subsections 2.2.2 and 2.2.3 will provide greater detail into these challenges respectively.

### 2.2.1 Introduction to Nuclear Mechanisms which cause SEUs

The lpGBT is a 65nm Complementary Metal Oxide Semiconductor [CMOS] (uses both p and n type MOSFETs) Ball Grid Array [BGA] chip [7]. As an ionizing particle passes through a material, such as $Si/SiO_2$ which is typically used in ASIC fabrication process, it will lose and deposit its energy $E_d$ within the material [13]. In the case of heavy ion or charged particle radiation, the ionizing particle is introduced directly. In the case of neutron (neutrally charged particles) radiation, as used for this experiment to characterize the lpGBT, the ionizing particles are the charged recoil nucleus created from the neutron interacting with the nuclei of the incident material. Charged particles need enough energy to overcome repulsion of the nucleus (i.e. overcome the Coulomb Barrier). A neutron has no charge and hence do not require as much energy to create a nuclear reaction. A charged recoil nucleus can also be produced from protons exceeding 15 MeV. As Coulomb repulsion is the major difference between proton and neutron radiation, it is assumed that no significant difference in SEU rate exists between proton and neutron radiation at high energies exceeding tens of MeV [14].

As the name suggests, the deposited energy of the ionizing particle is sufficient to cause a electron-hole pairs to form. These initial electrons released are referred to as primary electrons or $\delta$-electrons and generally have enough energy to cause secondary electron-hole pairs within surrounding atoms [13], [15]. The deposit of energy from the charged particle over distance traveled $\frac{E_d}{dx}$ is commonly known as the Linear Energy Transfer (LET) and is dependant on the incident material. The LET is described using the Beth-Bloch formula which intuitively illustrates that the change in $E_d$ is low for particles with high energy and vice versa [14], [16].

The deposit of energy from charge particles from neutron radiation can have cumulative effects on the physical structure (See 2.2.2) of the circuit and instantaneous Single Event Effects (See 2.2.3). Neutron radiation testing is quantified by various parameters. Free neutrons are classified by their kinetic energies. A summary of neutron energy classifications are given in Figure 2.7. Other prominent quantities include *neutron flux* which is defined as the total number of neutrons which pass through a given volume every second and expressed as $n/cm^2 \cdot s$ and *neutron fluence* $\phi(E)$ which is the flux integrated over certain period of time [17]. Susceptibility to SEUs are typically defined by the SEU cross-section which is calculated in Equation 2.13. The relationship between the aforementioned parameters and SEU rate is investigated in Section 2.3 such that an appropriate experiment setup can be constructed.

$$\sigma_{SEU} = \frac{Num.BitFlips}{\phi(E)} \tag{2.13}$$

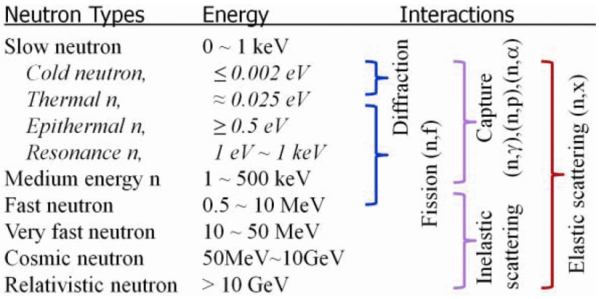



Figure 2.7: Summary of neutron energy classifications. Note fast neutron type with energies between 0.5 MeV to 10 MeV [17].

### 2.2.2 Total Ionizing Dose (TID)

TID mechanisms are extensively discussed in [13], [18] and illustrated in Figure 2.8. In short, after the energetic particle produces electron-hole pairs, the electron-hole pairs will recombine. Recombination is dependant on the density of electron-hole pairs created, temperature and if there is applied electric field. Holes typically travel slower than electrons in $SiO_2$. Some holes will not recombine as their electron counterparts are within the tunnelling regions of the gate and therefore tunnel out. The remaining holes will then drift into a trapped state which could last for years. It is the introduction of these trapped charges which cause changes in the physical characteristics of the device such as change in threshold voltage. The velocity $\mathcal{V}_d$ at which these holes travel is expressed by Equation 2.14 where $\mu$ is a charge mobility factor [13].

$$\mathcal{V}_d = \mu E \tag{2.14}$$

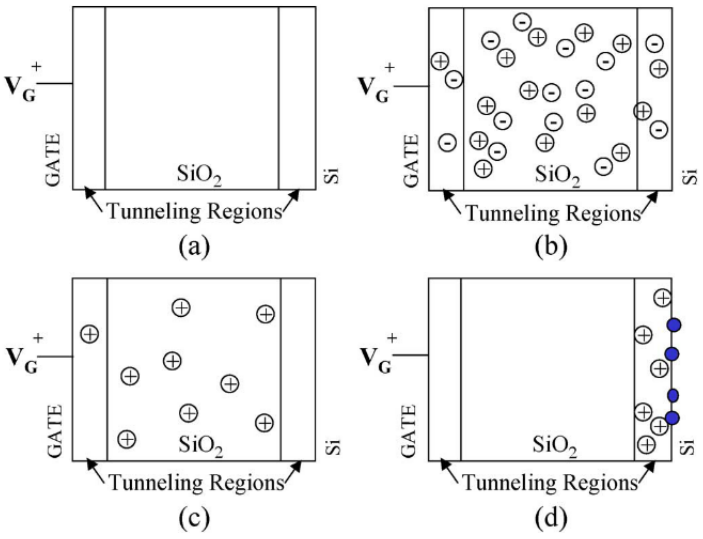


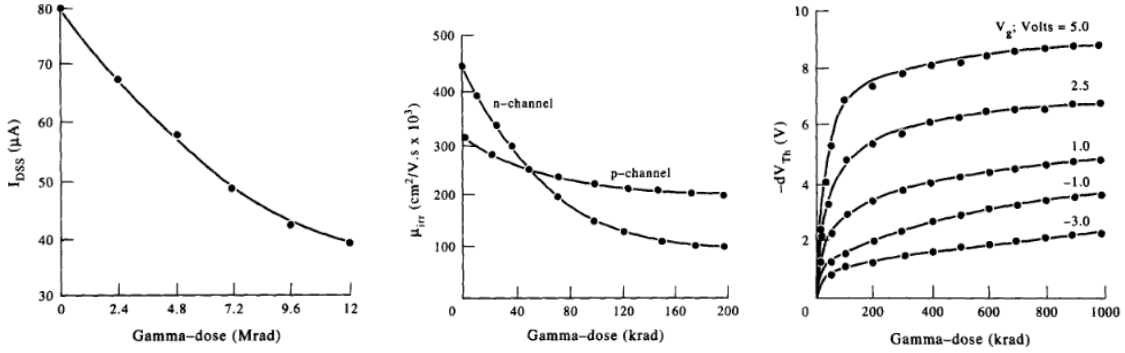

Figure 2.8: Illustration of physical mechanism of TID exposure [13]. It can be seen that by the final stage only holes are left in the transistor. These trapped charges change the electrical characteristics of the device.

Typically TID aging is done be irradiated the device with $\gamma$ rays [19]–[21]. The effects of $\gamma$ ray exposure on MOSFET devices was investigated in [19]. Results showed $\gamma$ ray exposure degraded the physical characteristics of the device in the following three ways:

1. Decrease in Drain Current ($I_d$). See Figure 2.9i
2. Decrease in Charge Carrier Mobility. See Figure 2.9ii. The study presents an additional mobility factor $\mu_{irr}$ due to the introduction of a energetic particle. $\mu_{irr}$ is therefore a function of the measured mobility before $\mu_{pre}$ and $\mu_{post}$ irradiation and is expressed in Equation 2.15.

$$\mu_{irr} = \frac{\mu_{pre} \times \mu_{post}}{\mu_{pre} - \mu_{post}} \tag{2.15}$$

3. Change in Threshold Voltage. See Figure 2.9iii. This results in requiring more applied voltage is required to keep nominal operation
4. Increase in Leakage Current (Current measured when expected 0A)




(i) Decrease in Drain Current (ii) Decrease in Charge Mobility (iii) Change in Threshold Voltage

Figure 2.9: Results showing decreases in drain current, charge mobility and increase in threshold voltage for devices with increasing TID exposure [19]

TID is measured in *rad* (radiation absorbed dose). The lpGBT is expected to operate with a TID of 200 Mrad but was observed to operate at TID of 415 Mrad without any clock degradation [22].

### 2.2.3 Single Event Effects

The process which results in SEEs is described as follows. The free electron-hole pairs created by the ionizing particle will recombine due Coulomb attraction. Furthermore electron-hole pairs are subjected to an applied electric field and hence the charge carriers will drift in response to the field. The rate of charge carrier drift is a transient current which forms $I \equiv \frac{dQ}{dt}$. Should sufficient amount of charge collect in a sensitive volume (SV) of the circuit; an erroneous change in the logic state within the circuit will occur. The parts of the circuit which are most sensitive to SEUs are the reversed biased p/n junctions and the amount of charge required to cause change of logic state is defined as $Q_c$ [14].

SEEs are classified as either hard or soft, whereby hard SEEs cause permanent damage to the electronic device. Table 2.2 provides a description of commonly occurring SEEs as defined by Joint Electron Device Engineering Council (JEDEC) Global Standards [23] and ASTM standard [24]. Although sounding similar, Single Event Upsets and Single Event Transients differ with SETs being a momentary bit flip which is quickly corrected whereas a SEU is change in the stored logic value, in a flip-flop for instance.

| **Type** | **Name** | **Description** |
|---|---|---|
| Soft | Single Event Upsets (SEU) | A soft error (an erroneous change of logic state which would have to be rewritten thereafter) caused by the passage of a single energetic particle |
| | Single Event Functionality Interrupt | A soft error caused by a single ion striking a special node causing it to malfunction in a detectable way and does not need a power cycle to resume normal operation |
| | Single Event Transient (SET) | Momentary voltage spike caused by the passage of a single ion strike |
| Hard | Single Event Latchup (SEL) | A single energetic particle causes a high current state resulting in a loss of device functionality (may require power cycle to resume normal operation) |
| | Single Event Burnout (SEB) | A single ion strike induces a localized high current state (similar to SEL) but can cause permanent device destruction |
| | Single Event Gate Rapture (SEGR) | A single ion strike which breaks down of a conducting path through the gate oxide of a MOSFET |

Table 2.2: Summary of Single Event Effects adapted from [23], [24]

## 2.3 Device Testing of Neutron-Induced SEUs

The EoS card test setup comprises of different electronic devices namely: the lpGBT ASIC, VTRx+ optical transceiver and the FPGA testbench. This Section investigates the susceptibility these different electronic device types have to neutron-induced SEUs.

### 2.3.1 Susceptibility of ASICs to SEUs

Section 2.2 described the environment in which the lpGBT will be installed and the nuclear mechanisms which challenge the performance of the ASIC. This section begins by describing past radiation testing procedures which qualify ASIC device performance and their findings. There are multiple parameters which are interesting to characterizing the performance of an electronic device exposed to radiation. The following studies are presented with specific emphasis on the parameters listed in Table 2.3. The motivation for each is also given.

| **Focus Area** | **Relation to this Experiment** |
|---|---|
| Experimental Setup and Duration of Testing | Provides a guideline on how to setup this experiment |
| Technology Architecture | Targeting studies with a similar architecture size of 65nm to provide more applicable results |
| Neutron source and Spectrum of Energies of the source used to irradiated the device | Allows for a comparison between previous sources used and the one for this experiment |
| SEU rate / SEU cross-section / Error Count | Provides an expectation of results for this experiment |

Table 2.3: Parameters of Interest for Previous Studies Investigated

Four types of devices with single and double bit error correction codes were tested when exposed to $14MeV$ neutron source [25]. Of these four the Cypress 3.3 V SRAM: CY7C1061GE30 is of interest being designed with a 65nm architecture and SEU mitigation techniques such as encoding and TMR [26]. Similar to this report's experimental setup, the test setup involved connecting the Device Under Test (DUT) to an FPGA control board which was shielded using a combination of polyethylene (see 2.10) and a lead/aluminum box. Four Cypress 3.3V SRAM devices were tested with two being irradiated at a distance of 5.7 cm from the source until a total fluence of $1 \times 10^{11} n/cm^2$ was reached. The other 2 were irradiated with a moderated and unmoderated source to test for SEUs due to thermal neutrons. These were placed at a distance of 19cm and irradiated until a fluence of $1 \times 10^{11} n/cm^2$ was reached. The DUTs were configured to read, write and correct data to and from each other. This device saw both single and multiple bit upsets however the probability of observing errors was substantially small with error rates of $2.8 \times 10^{-16}$ and $1.2 \times 10^{-19}$ respectively. The study also concluded that there was no noticeable difference considering the moderated and unmoderated source.

A study shown described in [27] investigated two low power 65nm flip-flop devices. Both devices were built with Dual Interlocked Storage Cell (DICE) technology, with the first being a conventional device and

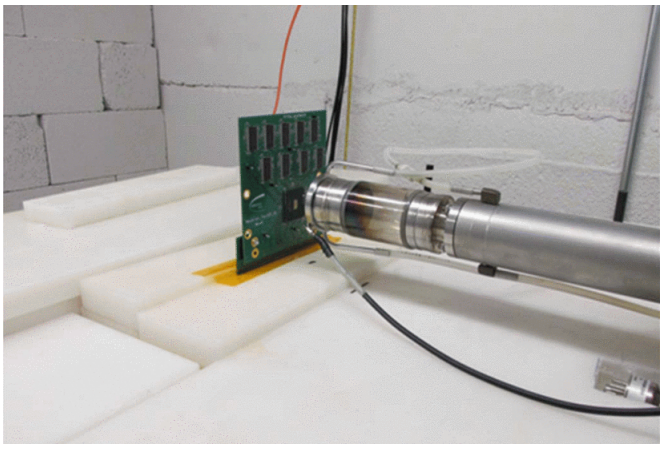
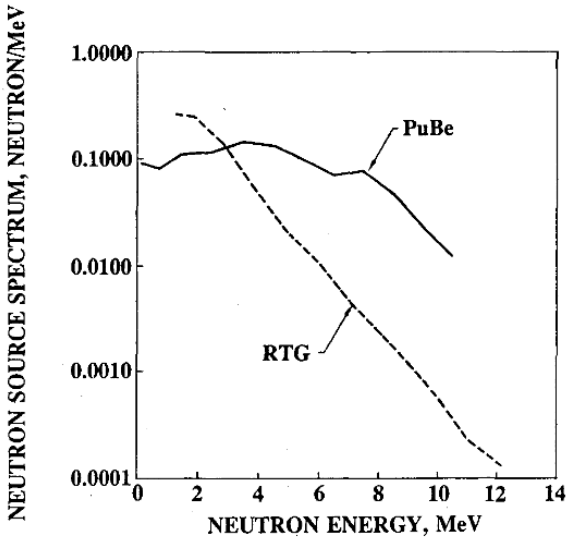


Figure 2.10: Experiment setup for performing a BER test for SRAM DUT irradiated by neutron beam at a distance of 5.7cm [25]

the second also including Adaptive Coupling (ACFF). The lpGBT also features DICE technology which is described in greater detail in Section 2.5. It is the conventional device which is of interest as it more closely resembles the lpGBT device. The study observed 194 errors after irradiating the device for 19 hours using the neutron beam at Research Center for Nuclear Physics, Osaka University facility. The work presented in this thesis hopes to characterize the susceptibility of the DSP stages with the lpGBT only and efforts were made to effectively turn off the TMR as such. However unlike TMR, DICE is a cell level technique [28] and cannot be turned off. As such, following the results presented in [27] it is promising to see SEUs being observed for DICE devices.

In another relevant study, authors in [29] carried out radiation testing of RAM and microprocessor devices using a PuBe source. The experiment opted to used a source that produced a spectrum of energies as opposed to a mono-energetic 14 MeV source. The energy spectrum of the source is depicted in Figure 2.11i with more than 40% of the neutrons having an energy of at least 4.5MeV. This is comparable to the source used to characterize the lpGBT presented in this thesis. The source was placed 1 cm away from the DUTs and the entire experiment was shielded with thick concrete. The DUTs were configured with a predetermined constant pattern and read at regular intervals. The results and descriptions of the DUTs are depicted in Figure 2.11ii and shows varying SEU susceptibility amongst the DUTs. These results were compared to Burst Generation Rate simulation methods which is further discussed in Section 2.4.1. The results from this study detected substantially less errors than previously mentioned. Furthermore results showed no correlation between duration of irradiation test and SEU rate.

The aforementioned studies investigated SEU rates using sources with spectrum of energies. The study performed in [30] took an alternate approach investigating the relation between SEU rates of bulk SRAM devices and neutron energies using a mono-energetic source beams. Unfortunately the device closest in




(i) Energy Spectrum of the PuBe Source presented in illustrating a range energies of up to 10 MeV similar to the source used to characterize the lpGBT. [29]

| Device | Description | Exposure (Hrs) | Neutron fluence (n/cm2) | Upsets S/N | Upsets # |
|---|---|---|---|---|---|
| MM54C929 | 1K word by 1 bit CMOS static RAM DC 13160SOCN | 185.5 | 1.3E11 | 1-4 | 0 |
| | | 15* | 1.1E10 | 1-4 | 0 |
| AM29705APC | 16 word by 4 bit dual port static RAM 2 die configurations | | | | |
| | DC (old) 8138D | (old) 49 | 3.5E10 | 1-4 | 0 |
| | DC (new) 8546FPE | (new) 438 | 3.2E11 | 1 | 1 |
| | | | | 2 | 1 |
| | | | | 3 | 4 |
| | | | | 4 | 3 |
| AM2901BPC | 4 bit Bipolar Microprocessor Slice DC 8211DM | 168 | 1.2E11 | 1 | 0 |
| 93L422 | 1K word by 1 bit | 23 | 1.7E10 | 1-4 | 17 |

* Low power stand-by mode
DC = Date code
S/N = Serial Number

(ii) Table of Results presented by [29] showing a wide and uncorrelated range of irradiation durations to observe SEU errors

Figure 2.11: Experimental Results from [29]

architecture size to the lpGBT is 180nm. Nonetheless the results of the study show a significant 19% of 180nm SEUs are contributed by neutrons with energies between 1 and 10 MeV. More specifically results illustrated in Figure 2.12 show SEU cross-section peaks at 14MeV however cross-sections at 4 and 6 MeV are still significant. This is promising as the source used in [30] emit most neutrons at 4 and 6 MeV. See Section 4.9.

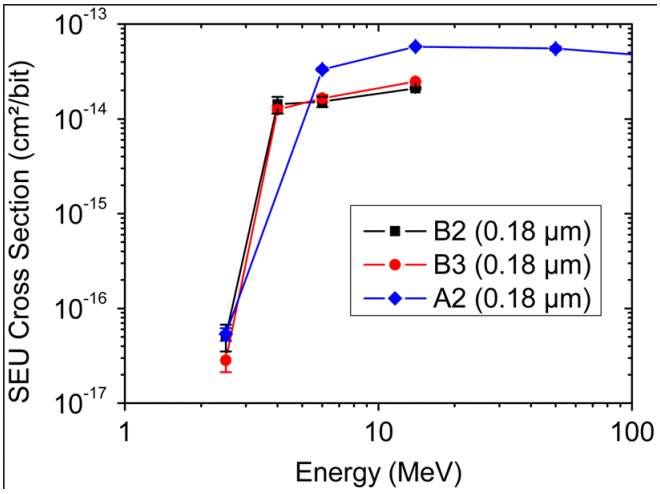
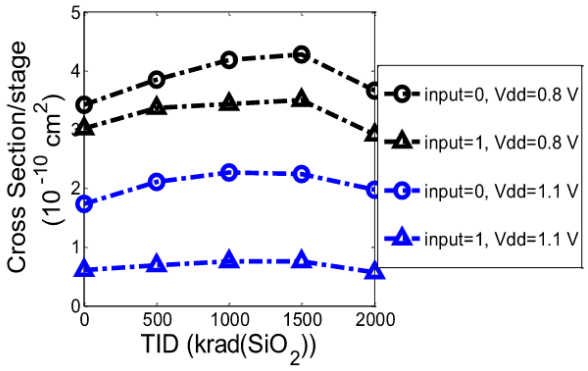



Figure 2.12: Experimental Results from Mono-Energetic Neutron Testing showing 4 and 6 MeV neutrons playing a significant role in SEU cross-section [30]

Thus the experimental setup used in this investigation is comparable to previous studies. However unlike previous study, methodology presented in this thesis also aims to characterize the susceptibility of the stages within an ASIC device as opposed to looking at the overall SEU rate. Finally, limitations of the aforementioned studies to be considered include the randomness of the pattern used. Testing with a more random pattern will produce results more indicative of real-world applications. The experiment presented in this dissertation is similarly limited as discussed in Section 4.3.

### 2.3.2 The Effect of TID on SEU Rate

Section 2.2.2 provided a brief introduction to how TID exposure changes the physical characteristics of a device. This section discusses the effect TID damage effects the SEU rate. A study provided by [31] measured the SEU rate for 4 Mb SRAM with 192, 561 and 796$krad$ $\gamma$ ray dose to simulate the TID aging process. The DUT was irradiated for an average time of 158 hours. Their findings are presented in Figure 2.13ii.




(i) General increase in SEU Cross-section due to TID exposure [20]

| Irradiation time with neutrons (s) | Gama accumulated dose (krad) | Neutrons fluency ($10^9$ n.cm$^2$) | Bit flips | Cross section ($10^{-8}$ cm$^2$) |
|---|---|---|---|---|
| 535039 | 0 | 4.21 ± 0.13 | 138 | 3.28 ± 0.30 |
| 535552 | 192 | 4.21 ± 0.13 | 145 | 3.44 ± 0.30 |
| 702934 | 561 | 5.53 ± 0.17 | 208 | 3.76 ± 0.28 |
| 511084 | 796 | 4.02 ± 0.12 | 157 | 3.90 ± 0.33 |

(ii) Results indicating general increase in SEU rate due to TID exposure [31]

Figure 2.13: Studies showing a general small increase in SEU rate due to increase in TID exposure

In another study [20] a device was irradiated with 10-keV X-rays for 72 hours resulting in a dose of 525 rad. The DUT was a chain of D-type flip flops fabricated with a newer 40nm architecture and operated at a clock frequency of 1 MHz. Results showed, as expected, increases in leakage current. Even after an annealing process whereby the leakage current decreased 10% the damage was still observable. Consequently the SEU rate also generally increased with TID exposure, with errors being detected within the first 10 minutes of testing, much less duration than [31].

Although the experiment presented in this thesis aims to characterize the effects of SEUs on the lpGBT device it is difficult to exclude the effects of TID due to exposure for both types of radiation [20]. However,

given the results from [20], [31] the effects of TID exposure for the purposes of this thesis is deemed to be minor. Thus the effects of TID exposure will be excluded from analysis from the performed experiment.

In summary, researchers in [25] presented results after irradiating a type of SRAM device, which shares similarities with the lpGBT in architecture size, use of encoding techniques and TMR. Results show substantially small error rates but provides a guideline for an experimental setup. Alternately a study shown in [27] showed 194 errors when irradiating a device that like the lpGBT is built with DICE technology, illustrating that this technology is also susceptible to SEUs. The study presented in [29] provides an indication that duration of irradiation is largely uncorrelated with errors being observed with 23 hours or no errors after 168 hours. Furthermore [30] illustrated promising results to observe SEUs with a source of 4 to 6 MeV comparable the source used to characterize the lpGBT. Finally results [20], [31] show the effects of TID for the purposes of characterizing the lpGBT can be ignored.

### 2.3.3 Susceptibility of FPGAs to SEUs

The current BER test setup utilizes a FPGA testbench. Whilst the susceptibility of the EoS card is to neutron radiation is being investigated, the susceptibility of the FPGA testbench is also called into question as this may impact the SEU rate of the EoS card. In addition to characterizing the lpGBT an investigation into the susceptibility of the FPGA testbench to SEUs was also conducted and is described in Section 4.6.

The combined effects of TID, SEUs and Electromagnetic Interference (EMI) on a Xilinx Spartan 3E FPGA were investigated in [21]. The FPGA was programmed to run a bubble sort algorithm on a LEON3 softcore processor. The effects of EMI was induced by injecting noise on the power supply. The injected noise was characterized to have voltage dips up to 16.67% and 25% with frequencies at 10 kHz and 5 kHz respectively. The effects of SEUs was induced using a neutron AmBe source. The first with an FPGA exposed to a TID of 750 krad and a second "fresh" FPGA to be used as a reference. The AmBe source emitted neutrons at energies of 2 MeV to 11 MeV and had a flux of $9 \times 10^4$ neutrons per $cm^2/s$. The Figure 2.14 illustrates their test setup with the AmBe source.

Results showed the FPGA exposed to a TID had an increase in number of errors per hour (7.43) as compared to the fresh FPGA (5.98). It was also found that the errors that transition from $0 \rightarrow 1$ is higher than of transitions from $1 \rightarrow 0$.

Experiments investigating just the effects of neutron-induced SEUs were performed by [32]. Their results are summarized in Table 2.4 and show despite using high energy neutron sources and higher flux, no SEU errors were shown. As a result one could conclude that the effects of TID and EMI played a larger role for the errors shown in [21]. However, it must be noted that [32] was a study done in 1998 and therefore improvements in technology should be considered in this comparison.

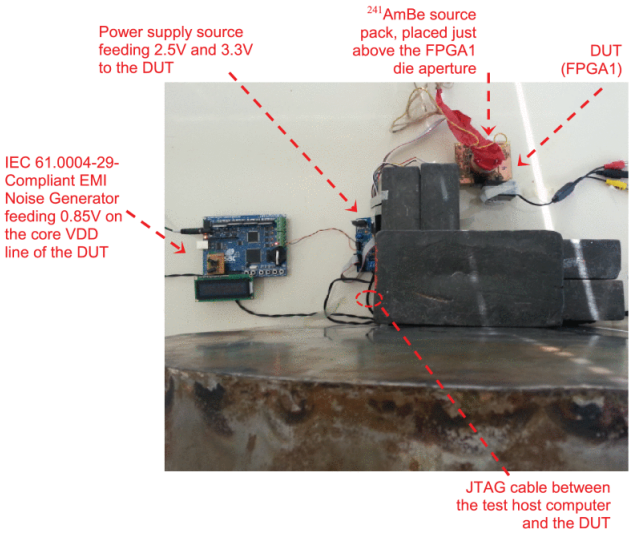



Figure 2.14: FPGA LEON3 softcore BER test whilst being irradiated with AmBe source placed directly on the DUT (right) [21]

| Device | Neutron Energy (MeV) | Neutron FLux ($cm^{-2}s{-}1$) | Irradiation Time (hours) | Number of Devices | Number of SEUs |
|---|---|---|---|---|---|
| XC4OIOE | 0 to 11 | $5.6 \times 10^3$ | 256 | 16 | 0 |
| XC4OIOE | 14 | $6 \times 10^6$ | 4 | 4 | 0 |
| XC4OIOE | 100 | $9.3 \times 10^3$ | 9 | 8 | 1 |
| XC4OIOXL | 100 | $9.3 \times 10^3$ | 9 | 8 | 4 |

Table 2.4: Experiment Results from [32] indicating no SEUs detected for FPGA after a duration 256 hours with a source that as an energy spectrum of up to 11 MeV

### 2.3.4 Susceptibility of Optical Transceivers to SEUs

The EoS cards' main function is to serialize and prepare the data collected from the front-end modules and transport the data optically which is received by an optical transceiver on the FPGA test bench. This Section will explore the susceptibility of optical transceivers to SEUs.

Radiation testing of the Glenair 050-301 optical transceivers were performed by [33]. The transceivers were installed on a Virtex-6 FPGA test bench which facilitated a loopback test with a PRBS7 pattern. A summary of the setup is provided in Table 2.5. The optical transceiver was exposed to a TID of up to 250 krad with a Cobalt-60 source. Results from the study showed the optical transceiver to operate nominally after irradiated with a neutron source with energies of 0.1 MeV to 10 MeV, for a duration of 181 minutes and a fluence of $2.5 \times 10^{12}$ neutrons per $cm^2$. No errors due to irradiation were observed with the neutron

source indicating the test bench transciever will not effect the SEU rate. This was experimentally tested in Section 4.6.

| Property | Glenair Setup | EoS Transceiver Setup |
|---|---|---|
| Device | Glenair 050-301 | VTRx+ |
| Evaluation Board | Virtex-6 | Kintex-7 |
| Optical fibre | Multinode 850nm | Multinode 850nm |
| Clock | 125 MHz | 160 MHz |
| Data Rate | Parallel 5 Gbps (×8) | 10.25 Gbps (up) 2.56 Gbps (down) |
| Encoding | 8b/10b | RS(224, 234) |

Table 2.5: Comparison showing the similarity between the optical transceiver studied in [33] and the optical transceiver used in the BER setup for the EoS card

## 2.4 Simulation Methods to determine SEU rate

SEU rates can be quantified through simulation or experimentation. Difficulties to recreate the harsh radiation environment of the HL-LHC for which the electronic devices are expected to operate, provides motivation to investigate simulation techniques previously used to quantify the SEU rates. Simulation is limited by the amount of information which is provided to the system. Advanced information of the physical environment and information relating to the lpGBT such as the materials used and the circuit topology are not available and hence provide the rationale to perform a physical experiment instead. However, by looking at the models used to estimate the physical environment one can identify the parameters which influence the SEU rate the most and need to be accommodated in the experiment.

### 2.4.1 Computational Methods

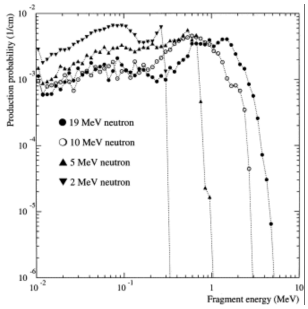
#### From First Principles

A computational method to estimate the SEU rate within electronic devices is proposed in [14] in order to avoid in-depth knowledge of the circuit being tested. The method considers high energy ($> 20MeV$) and low energy ($< 20MeV$) nuclear interactions. For simulations with low energies ($< 20MeV$, as will be the case for this experiment) calculations were performed using ENDFB-VI cross-section data.

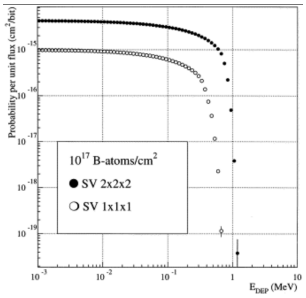
The geometry of the device was modelled as a single SV with sharp edges. Only silicon is considered the SV volume and it is assumed the results will be identical for $SiO_2$. The model assumes the particle hit the irradiated surface at 90 deg. Typically metals close to the SV region should be also modelled however was not in this case. Finally by running the simulation method, results are presented in Figure 2.15i as

the probability of depositing energy versus neutron energy. Following these results SEUs are determined if and only if the energy deposited $E_{dep}$ within the SV is greater than $E_{crit}$, hence the strong dependence on the choice of $E_{crit}$. Thus the first limitation of the method is apparent as finding $E_{crit}$ for the EoS card is outside the scope of this dissertation.

Ideally, an accurate model should also include the effects of thermal neutrons. However, SEUs due to thermal neutrons is linearly effected by the concentration and distribution (i.e. doping profile) of boron within the semiconductor. The second limitation is apparent with no way to estimate these concentrations. The method proposed in [14] would rerun the simulations by guessing a concentration of $10^{17}$ atoms per $cm^2$ for their varying SV regions. However, when comparing the probabilities of energy deposition for low energy neutrons for typical SV (Figure 2.15i) and boron doped SV (Figure 2.15ii) at this concentration thermal neutrons do not make a significant impact to SEU rate and thus these effects could be disregarded.




(i) Probabilities that Low Energy Neutrons will deposit their energy to cause an SEU. To be compared to thermal neutrons on the right.




(ii) Results indicating unlikely probability in thermal neutrons depositing their energy in with Boron Doped SV especially when compared to probabilities with higher energy neutrons depicted on the left

Figure 2.15: Energy Deposition Results from [14]

Further limitations to this method are apparent in Figure 2.16 when irradiating devices at 14MeV, with clear discrepancies between simulation results and experimental data. The study goes on to state this discrepancy is expected to get worse for neutron sources at lower energies as in the case with the sources available for this experiment.

### Burst Generation Rate (BGR)

Burst Generation Rate (BGR) is another computational simulation method, like the method proposed in [14], and is described as a conversion factor between neutron flux and SEU rate [34]. BGR functions are a collection of functions (illustrated in Figure 2.17i) which provide the probability of an incident particle with energy $< 50MeV$ interacting with a material which results in producing a nuclear interaction greater than

| Device | Experimental | 1x1x0.5 | 1x1x1 | 1x1x2 | 2x2x2 |
|---|---|---|---|---|---|
| M5M5408_B | $2.5\times10^{-13}$ | $4.3\times10^{-13}$ | $2.1\times10^{-13}$ | $5.0\times10^{-14}$ | $1.2\times10^{-13}$ |
| IDT71256 | $2.7\times10^{-14}$ | $1.1\times10^{-13}$ | $3.4\times10^{-14}$ | $3.8\times10^{-15}$ | $1.3\times10^{-14}$ |
| MCM6246 | $8.2\times10^{-15}$ | $1.7\times10^{-14}$ | $3.1\times10^{-15}$ | $8.1\times10^{-17}$ | $6.5\times10^{-16}$ |
| MHS65608E | $3.3\times10^{-14}$ | $3.4\times10^{-14}$ | $1.1\times10^{-14}$ | $1.2\times10^{-15}$ | $3.9\times10^{-15}$ |
| Minimum predicted/Experimental | | 1.0 | 0.33 | 0.0099 | 0.079 |
| Maximum predicted/Experimental | | 4.1 | 1.3 | 0.20 | 0.48 |
| Average predicted/Experimental | | 2.2 | 0.70 | 0.098 | 0.29 |

Figure 2.16: Prediction vs Experimental Results for Method Proposed in [14] showing decrease in accuracy for neutron sources with lower energies.

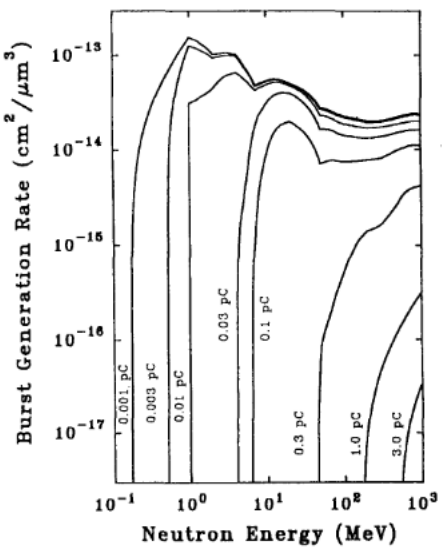
$E_{crit}$ and hence causing a SEU. BGR functions calculated using the Evaluated Nuclear Data Files (ENDF-V) for neutron interactions with Silicon. For energies $> 50MeV$, the High Energy Transport Code (HETC) can be used instead.

Estimating the upper limit to the SEU error rate using the BGR method requires input knowledge of the critical charge $Q_c$ (dependant on the device circuitry), SV thickness of the device, the energy spectrum and fluence ($\phi(E)$) of the radiation source used. Extensions to the BRG method are proposed in [35] which introduces an additional parameter "collection efficiency," since unlike the assumption made in [14] not all energy deposited will result in an SEU. Following the BRG functions, the Neutron Induced Error (NIE) function is determined by integrating the appropriate BRG function shown in Figure 2.17i multiplied by the appropriate energy spectrum of the source. Resulting NIE functions from the method proposed in [34] are shown in Figure 2.17ii. The predicted number of SEU induced errors is determined by applying the appropriate NIE function, SV and neutron fluence to Equation 2.16. The method proposed in [34] validated their findings against experimental data by irradiating a 1 kbit SRAM device using a PuBe neutron source with a fluence of $1.3\times10^{11}cm^{-2}$. Simulation results matched experimental results when observing no errors. Alongside this study [29] compared also compared their experimental results to BGR predictions for RAM and microprocessor devices and found BGR predictions were often 6 times the experimental results.

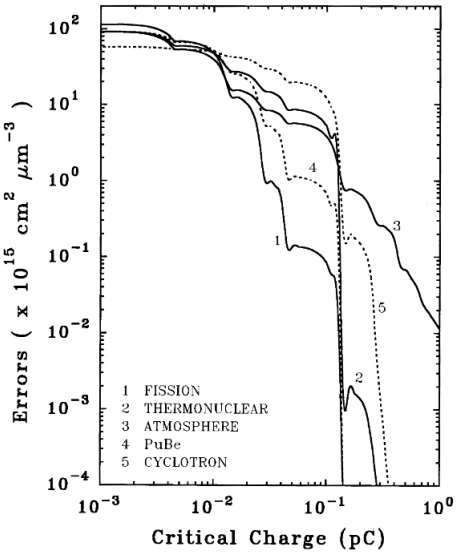
$$Errors\,per\,device = \phi(E) \times SV \times NIE \tag{2.16}$$

### TCAD

Sentaurus Technology Computer Aided Design (TCAD) Device software combines both physics and circuit models to simulate by numerical methods the SEE rate within devices [36]. The tool presented in [36] requires the user to identify the electron-hole pair generation model $g_{pair}$. Finding this parameter model is outside the engineering domain of this experiment. The tool offers packages for modelling both 2D and 3D circuits. However, modelling an NMOS transistor, for instance, would require knowledge of the doping profiles from




(i) Burst Generation Rates in Silicon for different values of $Q_c$ [34]




(ii) Neutron Induced Error (NIE) Rate for various $Q_c$ for unit volume of Silicon [34]

Figure 2.17: Burst Generation Rate and Neutron Induced Error (NIE) functions used to predict SEU error rate as proposed in [34]

the ASIC foundry. In the case of the EoS card this knowledge is unknown. Benefits to using this tool include the ability to find the energy threshold within a particular circuit which causes SEUs. Simulation results are presented in [36] with an energy threshold at $41pJ$ is similar when compared to experimental results $55pJ$ for laser pulsed radiation of a AMIS C5 CMOS inverter circuit.

### 2.4.2 Monte Carlo Simulations

Monte Carlo simulations simplify the need to model complex solutions [37] by illustrating SEE phenomena as a probability distribution [38]. A comparative list of Monte-Carlo simulation tools which simulate how sensitive a device is to SEEs is described below. Numerous Monte Carlo models have been developed including Geant4, FLUKA, SEMM-2 and Monte Carlo Radiative Energy Deposition (MRED) [37]. This thesis briefly introduces one.

**GEANT4** Geant4 is an open-source object orientated Monte Carlo simulation tool which provides electromagnetic physics models, the ability to model particle transport in complex 3D models and is extensible for other simulation engines. Input data for the tool is the width, length and thickness of the DUT's SV as well as any shielding material. It is noted that the thickness of the SV could be inferred from the $Q_{crit}$, however neither parameters are available for the active components within the EoS. Benefits of the tool include simulation of hadrons (family of particles including neutrons) with energies of 1keV up to 100TeV

and modularity allowing easily include more parameters [39], [40].

### 2.4.3 SEE Simulation Tools for Early Circuit Design

The following tools simulate the SEU rate of RTL circuit designs, such that robustness of the design against SEUs can be improved before fabrication. These tools were explored whilst developing an experiment to characterize SEU rate for the lpGBT.

**SEEG** The Single Event Effect Generator (SEEG) is a tool within the TMRG toolset [41]. The TMRG toolset is discussed in detail in the Section 2.5.4. The SEEG tool is included in the toolchain to verify the triplicated netlist. The tool simulates SEEs through Verilog testbench module by forcing specific wires within DUT to a specific value.

**YOSEEG** The Yosys SEEG (YOSEEG) tool was designed to replace the SEEG tool in the TMRG toolset. It has identical functionality to SEEG but is based upon the Yosys Synthesis suite (an alternate open source synthesis tool which supports Verilog-2005). It expects a fully TMRG annotated file as input [42].

**Analog Fault Tolerant University of Seville Debugging System (AFTU)** Another tool developed for the rapid testing of circuit design to SEE is documented in [38]. The AFTU tool is complementary to that of [36] and [39], however focuses specifically on SET sensitivity as opposed to SEU. As previously described in Table 2.2, SET are described as a momentary "glitch" in logic whereas an SEU specifically is a change in stored logic value.

In summary, the previous 3 sections explored various methods to simulate the SEU rate for different DUTs. The methods by first principles, Monte Carlo and BGR requires detailed knowledge of the $Q_c$ and SV of the device under test. These are difficult parameters to obtain as values such as the circuit's technology and topology effect these values significantly. Furthermore to simulate the SEU rate on the EoS card by modeling the HL-LHC environment directly and would require vastly increased knowledge outside the domain of this thesis. The tools such as SEEG and AFTU are specifically used for circuit design and are not applicable to test susceptibility after fabrication, as in the case of the EoS card. It is for these reasons simulation tests were not performed.

## 2.5 lpGBT Architecture

Until now the digital communication functions, ITk environment and previous SEU studies were discussed as it relates to the lpGBT. This section will provide a detailed overview of the lpGBT, challenges and test features considered when designing experiment centered around the lpGBT.

### 2.5.1 Overview

An overview of the lpGBT architecture is shown in Figure 2.18. Depicted on the left are the front-end modules which will be connected to the EoS (and subsequently the lpGBT) via E-Links whereas on far right shows the optical link up and downlink connections. The data flow from left to right shows the module data needing to pass through the scrambler, encoder and interleaver DSP stages before moving to the line driver before being transmitted optically. The inverse process is shown when moving right to left (i.e. downlink). Finally the bottom right illustrates the additional I2C and ADC modules to configure and monitor the operation of the lpGBT chip itself.

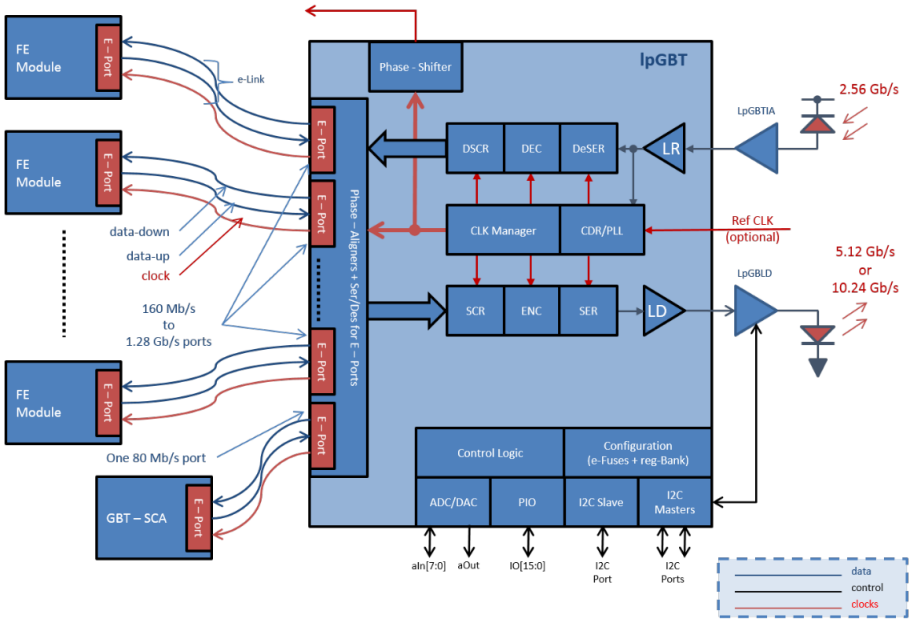



Figure 2.18: Internal Architecture of the lpGBT. Note the DSP stages in the middle marked “SCR”, “ENC” and “SER” [7]

### 2.5.2 ASIC Testing Challenges and Constraints

In order to develop an experiment with the lpGBT, the following considerations were identified. Bit Error Rate testing is a simplistic and prominent test used to characterize the performance of communications systems. Challenges facing BER testing is very long testing time in order to see any bit errors occur. For example, initial testing of the EoS boards took 24 hours to find a BER of $8.3 \times 10^{-14}$, transmitting at approximately 10 Gbps [43]. Furthermore it is very difficult to replicate the operating environment to effectively perform a BER test, as is the case with the lpGBT within the HL-LHC. However without access to the lpGBT I/O pins or internal layout of the design, developing an experiment to characterize the EoS card is therefore constrained to a BER test.

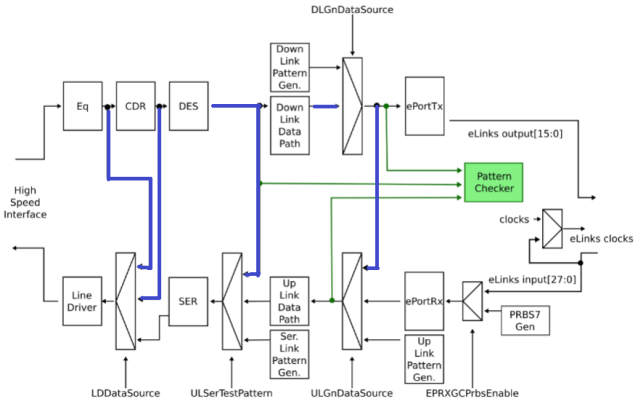



Figure 2.19: lpGBT Loopback testing paths highlighted in blue. The Pattern Checker (green) can be configured to monitor the data on one of these paths [7].

### 2.5.3 lpGBT Test Features

The lpGBT includes a number of test features to test the performance of the ASIC. These test features were initially explored in the development of this thesis.

**Loopback Testing** The lpGBT also offers loopback tests for the Front End electronics. Loopback tests for testing the functionality of a individual stage by comparing the result looped back to an expected result. Loopback data paths are indicated in blue in Figure 2.19.

**Pattern Checker** The lpGBT contains an internal pattern checker register which can be configured to monitor data pattern at various points (Figure 2.19 highlights available points in green). An initial experiment proposal was to read the register upon receiving a bit error. If the pattern is identical to what was received it could be concluded that the error had to have occurred before the monitored point. However register read speeds were too slow to keep up with the data rate of the lpGBT.

**Pattern Generation** The lpGBT can inject a pattern at various points along the uplink or downlink data path. Figure 2.20 illustrates these points along the uplink path. This is a powerful feature used in this experiment to inject a known constant 32 bit pattern for each ePortRX group. This results in realizing a BER test without the need for eLink connections, minimizing uncertainties due to eLink exposure to radiation and simplifying test setup.

### 2.5.4 SEU Mitigation Techniques

The lpGBT employs the following design techniques to mitigate against the effect of SEUs. A brief look into these techniques provides deeper insight to analysing the BER measured from this experiment and possibly correcting for their effects.

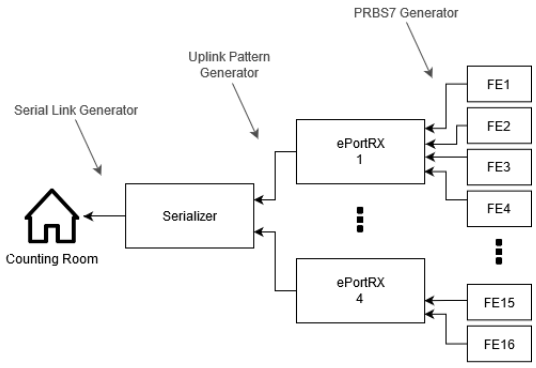



Figure 2.20: Points along the lpGBT uplink data path for which a data pattern can be injected. This experiment will inject a constant pattern for each ePortRX group bypassing the need to use E-Link connections.

**Encoding** Encoding techniques enable the ability to correct a corrupted message by adding redundancy to the message. The Reed-Solomon algorithm was employed in the lpGBT and the already discussed in Section 2.1.

**Triple Modular Redundancy (TMR)** TMR is implemented on the lpGBT through the TMRG Python tool which is used to introduce triplication during the RTL design process. Signals and combination logic is triplicated such that a SEU will only effect one of the three branches. The different architectures in which triplication is accomplished is shown in Figure 2.21. To avoid an SEU effecting two redundant cells at the same time, effectively causing an upset in majority voter, the cells are physically placed as far away from each other as possible. Triplication comes at the cost of more power consumption and increased in the amount of area the logic circuit occupies. Therefore, running the tool once does not produce a final design as there are multiple design considerations which need to be handled first, such as which combinational logic sections and signals will be triplicated. The design flow for the TMRG tool set is illustrated in Figure A.6.

The lpGBT has functionality to turn off different branches of the TMR design, effectively removing the effects of TMR when observing SEU rate [7]. In order to remove the effect of TMR when characterizing the individual stages of the lpGBT this feature was exploited. See Section 4.2.

**Watchdog** The lpGBT has a startup configuration sequence which is controlled by a Finite State Machine (FSM), depicted in Figure A.5. The lpGBT includes a watchdog process which monitors the values at various sub-blocks within the device. In the case a fault is detected causing a sub-block to stop functioning correctly, the watchdog process will run a re-configuration process on the effected sub-block until the it is operational (i.e. the watchdog will "scrub" the sub-block) by resetting the FSM. It was discovered that in the event of an SEU, the lpGBT will recover to its operational state regardless if the watchdog process is enabled. However, the recovery process is longer when the watchdog is enabled which subsequently may cause more

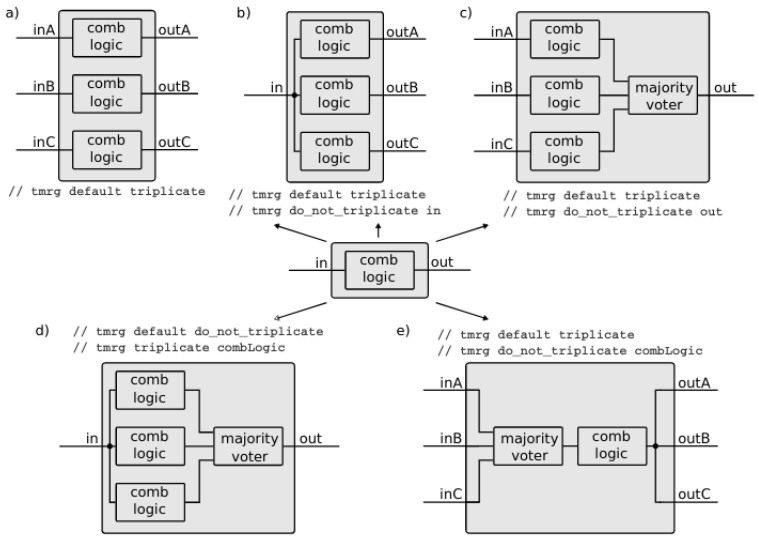



Figure 2.21: Graphical Illustration for Different Triplication Designs [41]. It is shown that choosing to triplicate the signals and/or combinational logic within the lpGBT will result in different circuit architectures.

errors [7]. As such this experiment will run without watchdog enabled.

**Dual Interlocked Cell (DICE)** The encoding and TMR *system* level techniques introduce latency and more power dissipation to implement on a digital device. Dual Interlocked Cell (DICE) technology is a *cell* level technique that was developed to offer SEU immunity without the aforementioned drawbacks [28]. DICE logic introduces redundancy to the logic design as illustrated in Figure 2.22. The logic outputs are labeled $X_i$ and each output is controlled by their respective diagonal. (e.g. $X_1$ and $X_3$). The invertors are N and P type transistors and are labelled $N_i$ and $P_i$ accordingly. Table 2.6 summarizes the behaviour of the circuit and shows the isolated latch pair that forms depending on the logic state. Since these latch pairs are isolated, an upset at $X_i$ will not effect its corresponding node storing the same value due to the feedback system. Hence the effected node will be corrected after a small propagation delay. It is possible for an upset to effect two nodes at once causing a permanent upset to the system, however the likelihood of this can be reduced by physical spacing of the nodes [44]. DICE is a cell level technique and as such cannot be activated/deactivated such as the TMR or the watchdog.

| Logic | Conducting Transistor Pairs | Blocked Transistor Pairs | Isolated Latch Pair |
|---|---|---|---|
| $0 = X_{0...3} = 0101$ | $(N_0 - P_1)$ and $(N_2 - P_3)$ | $(N_1 - P_2)$ and $(N_3 - P_0)$ | $(X_0 - X_1)$ horizontally isolated from $(X_2 - X_3)$ |
| $1 = X_{0...3} = 1010$ | $(N_1 - P_2)$ and $(N_3 - P_0)$ | $(N_0 - P_1)$ and $(N_2 - P_3)$ | $(X_0 - X_3)$ vertically isolated from $(X_1 - X_2)$ |

Table 2.6: Different scenarios for DICE Cell Circuit shown in Figure 2.22

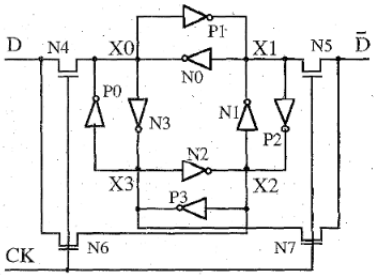



Figure 2.22: Principle of DICE Cell Architecture [44]. The output logic value of cell is determined at points $X_i$ and is controlled by its diagonal node. An upset in one is quickly recovered by the corresponding diagonal.

# Chapter 3

# Development of Research

Chapter 2 introduced the theory behind the operation of the lpGBT device and the mechanisms and factors behind SEU rates. Furthermore, the chapter illustrated similar investigations into SEU rates of various electronic devices. This chapter presents the technical knowledge behind the existing BER test setup used by DESY and serves as a basis for this experiment.

## 3.1 Overview of Existing BER Test Setup

This experiment began by first commissioning an independent setup similar to that of DESY at the Department of Physics, UCT. The following chapter will outline the modifications made to this setup. A Xilinx KC705 Evaluation board which houses a Xilinx Kintex 7 FPGA acts as the experiment's test bench between the EoS and the user. The test bench is responsible for running the BER test whilst a control PC will monitor the results through a UART connection with the FPGA test bench. The test bench will also facilitate the configuration of the EoS card (lpGBT) through an I2C connection. This I2C connection was facilitated with the addition of a FPGA Mezzanine Card (FMC). The test bench receives data from the EoS card through

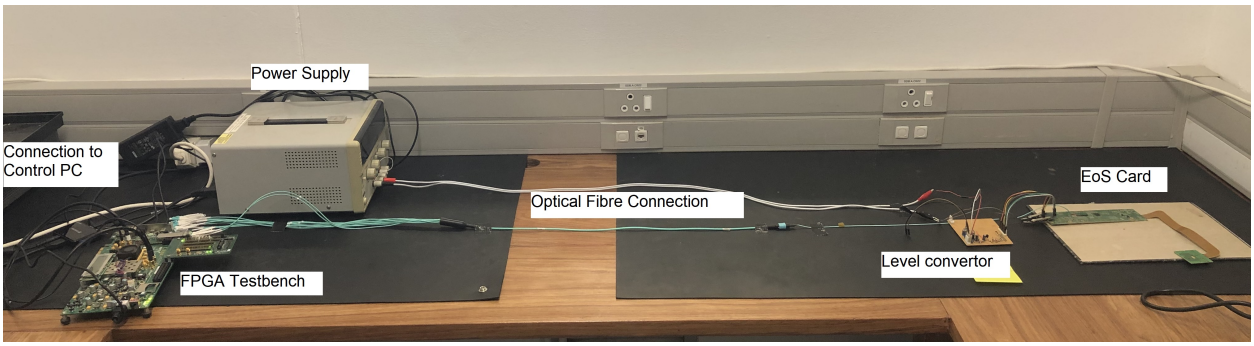



Figure 3.1: Illustrating the main components of the setup commissioned by the author in the UCT Physics Department. Specific emphasis is placed on the FPGA test bench (left) and EoS card (right)

optical link connections. An additional SFP+ 10 Gigabit optical transceiver is required to connect to the control board.

## 3.2 FPGA Test Bench Firmware

The objectives of the firmware is summarized in the list below. Each sub-objective is realised by a module in the firmware. To facilitate a full description of the experimental setup, an overview of the modules (i.e. the firmware architecture) is provided in Figure 3.2. The following paragraphs will examine the functionality of each module in further detail.

1. Generate Data for up to 14 E-Link Channels
2. Receive data packet via optical links and apply digital signal processing to retrieve original message
3. Compare the message received to the generated message and track the number of erroneous bits
4. Configure the lpGBT via I2C interface using the FPGA GPIO pins or using the VL+ optical protocol
5. Start and stop the BER test
6. Configure the BER test parameters such as setting the number of active E-Link channels and data pattern to be generated
7. Generate 160MHz clock for the integrated optical transceiver

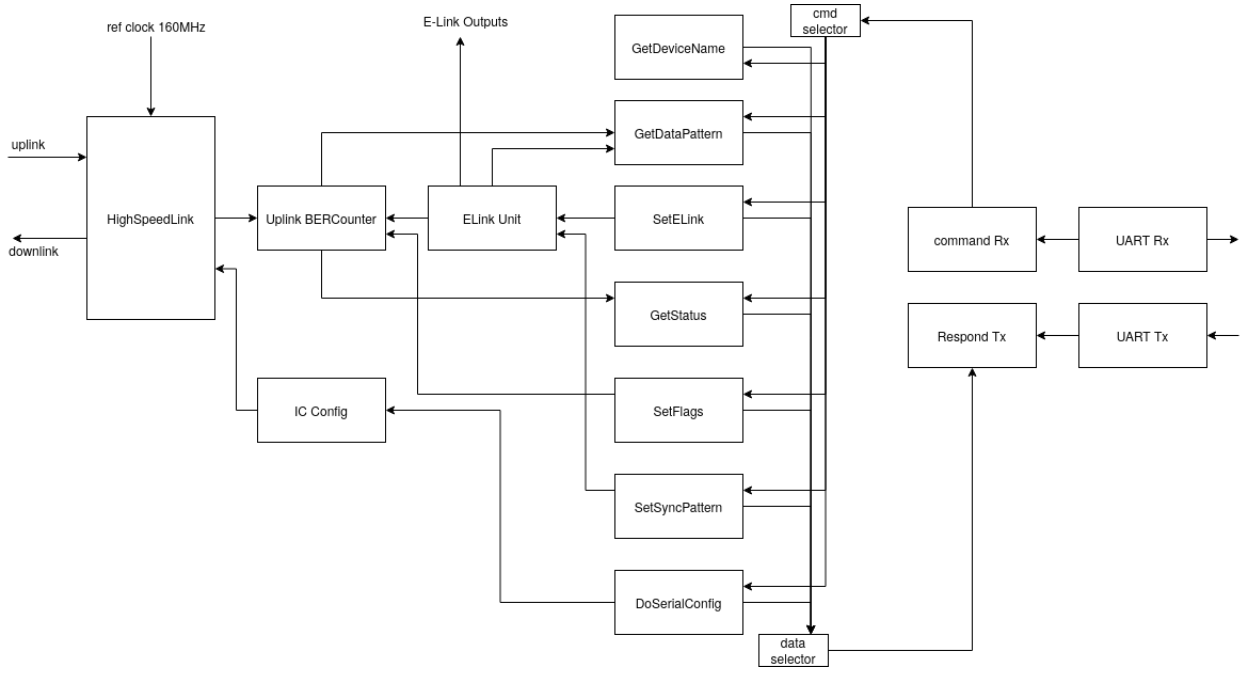



Figure 3.2: Simplified block diagram of the firmware modules relevant to the BER test. Full diagram is available at [10] Take note of the HighSpeedLink (left), Uplink BERCounter and ELink Unit modules

**High Speed Link** The High Speed Link module is responsible for facilitating the optical link communication between the EoS card and the front end modules. It is responsible for both downlink and uplink data preparation. In the case of downlink path, the module is required to scramble, encode and interleaver data before transmitting. Conversely receiving data from the uplink path will require deinterleaving, decoding and descrambling to process the data. To reiterate, this experiment aims to detect SEUs within the DSP stages of lpGBT. For reasons detailed later, the uplink data path within the lpGBT will be modified and thus the original uplink data path within the FPGA is illustrated in Figure 3.3. For completeness, an illustration of the downlink is provided in Figure A.7.

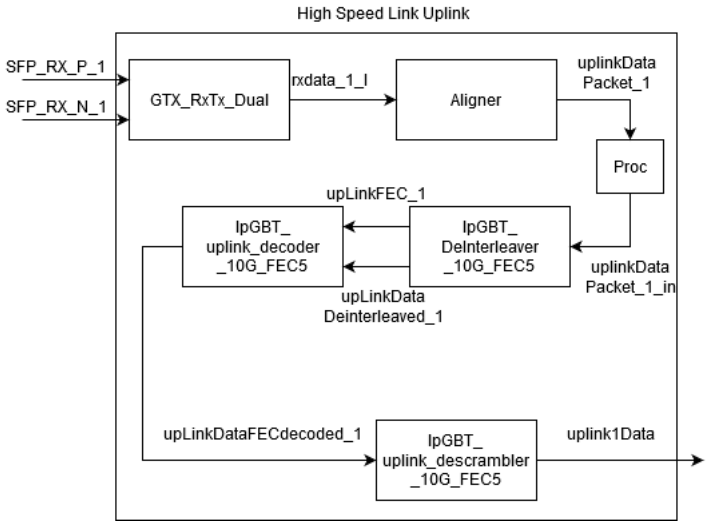



Figure 3.3: Detailed Architecture of the uplink High Speed Link data flow showing how the data received by the SFP optical links must be processed before comparison

**ELinkUnit and SetELink** There are a number of configuration settings that are available for the existing BER test firmware. This includes setting which E-Link channels the control board will generate data for and what type of generated data will be transmitted for each E-Link (e.g. a pseudo random binary sequence or constant pattern). The data transmitted is stored in a First In First Out (FIFO) structure, illustrated in Figure 3.4. Such E-Link controls are configured by the SetELink module and must be configured before running a BER test. When the BER test runs it is the ELinkUnit which generates data that is both sent to the ELink output (i.e. a GPIO output pin) and sent to the BER Counter module to be evaluated to the received data. There is a delay from transmission between generating the data and receiving the data due to the test bench firmware, length of wires etc. This delay is not known a priori and must be set using the SetELink module by transmitting and comparing a known pattern referred to as a SyncPattern. The algorithm to set the delay is illustrated in Figure 3.5.

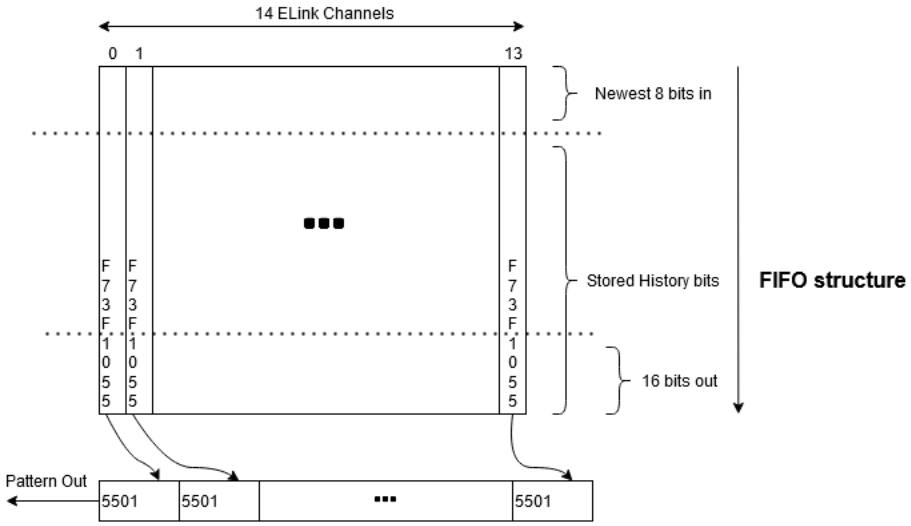



Figure 3.4: Graphical illustration of E-Link Data Generation FIFO. Every clock cycle 16 bits from each of the 14 E-Links is used to construct a data frame ("pattern out")

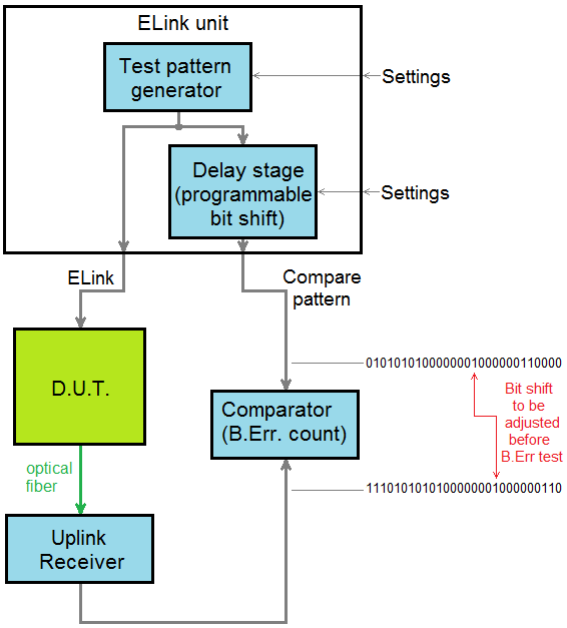



Figure 3.5: Algorithm to set the E-Link Delay [10]. A known pattern must be sent to the DUT and then compared using the BER Counter to manually set the delay. This process is repeated until patterns match.

**BER Counter** After the message from uplink frame as been extracted it is immediately sent to the BER Counter module. The received message is then compared to generated data from the ELinkUnit through a bitwise XOR comparison. The number of errors for each ELink is then stored in an internal buffer and can be access via the GetStatus module. Furthermore, the BER counter will also count the number of misaligned frames and number of corrected frames from de-interleaver and decoder modules further upstream. Finally,

upon the detecting first error the received data is locked in an internal buffer and can be accessed by the GetPattern module.

**GetStatus** This module returns the following BER test status information:

- Bit Error count for each E-Link
- How many of the last 15 uplink/downlink packets match the generated pattern
- Running status of BER test. Running or stopped.
- CRC and alignment status of the uplink packet
- Whether the uplink pattern is currently locked (i.e. error was detected between received data and generated data). To be requested with the GetPattern module.

**GetPattern** The GetPattern command module stores the data frame received of both the generated data frame and the received data frame for each ELink the first time an error occurred in that specific ELink.

**Command Receive (cmd_rx)** The firmware communicates to the control PC via UART. The cmd_rx module is responsible for converting the received data to a "command word." As shown in Figure 3.6, the main process of the firmware will continually evaluate the command word and enable the appropriate module accordingly. Depending on the activated module a multiplexer will select appropriate parameter data to the module. (e.g. SetSyncPattern module receives sync pattern parameter data as illustrated in Figure 3.7).

```
process(clk100) begin
if rising_edge(clk100) then
    if cmd_received = '1' and cmd_received_old = '0' then              -- New command received: set command flag:
        case cmd_word is
        when X"0001" => cmd_rxenable <= '0'; GetDeviceName <= '1';
        when X"0006" => cmd_rxenable <= '0'; GetStatus <= '1';
        when X"0007" => cmd_rxenable <= '0'; I2CWriteData0 <= '1';
        when X"000A" => cmd_rxenable <= '0'; I2CReadData0 <= '1';
```

Figure 3.6: Code Snippet illustrating that the command word is used to enable the respective modules

```
-- Connect specific module to the response unit, according to received command:
datatxcmdbus <= datatxcmdbus_GetDeviceName    when GetDeviceName = '1'
           else datatxcmdbus_GetStatus        when GetStatus = '1'
           else datatxcmdbus_GetDataPattern   when GetDataPattern = '1'
           else datatxcmdbus_GetSettings      when GetSettings = '1'
```

Figure 3.7: Code Snippet illustrating a shared datatxcmdbus for passing data back to control PC. The module currently transmitting is dependant which module is activated.

**SetSyncPattern** As aforementioned the SyncPattern is used to determine the delay needed for the BER test. It was discovered the SyncPattern could be exploited to also run a BER without E-Links. This module was added to modify the SyncPattern to serve this purpose and is further explained in Section 4.3.

**GetDeviceName** Returns a string of characters to identify the current firmware version running on the test bench.

**Clock Generation** The KC705 Evaluation board houses a SiT9102AI 200 MHz oscillator which is used for clock generation. [45] Xilinx provides a Clock Wizard IP core [46] which can provide user defined clock signals using the internal or external clock signal. In this case, the 200 MHz clock will be used to generate the other required clock signals. The FPGA test bench uses a 100 MHz system clock for all the main modules such as the UART communication protocol and a 160 MHz reference clock for the optical transmission. This 160 MHz reference clock is generated, converted to a differential signal using a Differential Signal Output Buffer (OBDS) primitive element [47] and fed back to the integrated optical transceivers using an male-male SMA cables.

## 3.3 Overview of Existing LabView Software

As mentioned, a dedicated quality control setup is currently being developed at the Detector Assembly Facility (DAF) at DESY, Hamburg. The final procedure will rely on a number of devices for QC measurements. Devices include the Kintex-7 FPGA control board used for the BER test, Wiener Crate for power supply measurements, climate chamber for temperature cycles etc. As of writing, a LabView test bench application is currently under development to automate the monitoring, configuration and execution of these testing devices. Of these devices only the Kintex-7 FPGA control board is applicable to this experiment.

LabView is a graphical programming language that incorporates elements of object-orientated design. Details regarding the LabView development and design is provided in Section 4.5. The application provides a graphical interface to monitor and configure the connected devices. Configuration commands and test instructions are automated and stored in a text file referred to as the *sequence file*. LabView uses the sequence file to determine which commands to issue to the FPGA test bench. Sequence commands will then issue an instruction to one of the corresponding firmware modules as described in Section 3.2.

Figure 3.8 is a screenshot of the main LabView screen (view) that is used for this experiment. Table 3.1 provides a description of main components relevant to this experiment. A description of the rest components are provided in Table A.1. To summarize, the top half of the front panel provides a view of the sequences loaded from the sequence file. The bottom half provides a status overview relating to the BER test, specifically the number of correctable and non-correctable errors that have occurred as well as the number of

transmitted frames.

| Label | Name | Description |
|---|---|---|
| 1 | Load Sequences Button | Enables the user to browse and select the sequence file |
| 2 | Start Sequences Button | Begins the execution of the sequences file |
| 5 | Device Status Indicators | Indicates the status of devices to be connected. Specifically a successful connection to the optical links (Uplink 1) and FPGA control board (FPGA status) is indicated in green |
| 7 | Sequence File Display | Displays the list of sequences from the sequence files alongside the result and execution time |
| 9 | ELink Error Indicators | Array of 14 indicators counting the number of errors detected from each E-Link. |
| 10 | FPGA Status Indicator | Indicates a successful connection to the FPGA test bench |
| 11 | Firmware Version Indicator | Indicates the firmware version loaded on the FPGA which is defined in the GetName module of the firmware. This helped differentiate between tests. |
| 12 | Uplink 1 Align Errors | Number of frames received for which the header bits were not found. |
| 13 | Uplink 1 CRC Errors | Number of frames received for which errors were detected (i.e. calculated syndrome $\neq 0$) |
| 14 | Frame Counter Indicator | Indicates the number of frames that have been transmitted during the Bit Error Rate Test. Increases by $40 \times 10^6 frames/s$ |
| 16 | Start BER Test Button | Button the begin execution of the BER Test |

Table 3.1: Description the main LabView front panel components shown in Figure 3.8. The descriptions are completed in Table A.1

## 3.4 Powering the EoS Card

The EoS card is powered by a 1.2V and 2.5V line. A detailed power budget is provided in Table 3.2. The lpGBT requires a 1.2V whilst the VL+ requires both a 1.2V and 2.5V input. A level-converter circuit simplifies the setup by producing 1.2V and 2.5V outputs from a more common 3.3V input. This 3.3V was supplied from an external power supply. The level-converter circuit is shown in Figure 3.9i. This level-converter also served an additional purpose to bridge the I2C signals from the FPGA GPIO pins to the EoS card as well as offer a switch to toggle between I2C or optical configuration. See Section 3.5.

Power Budget

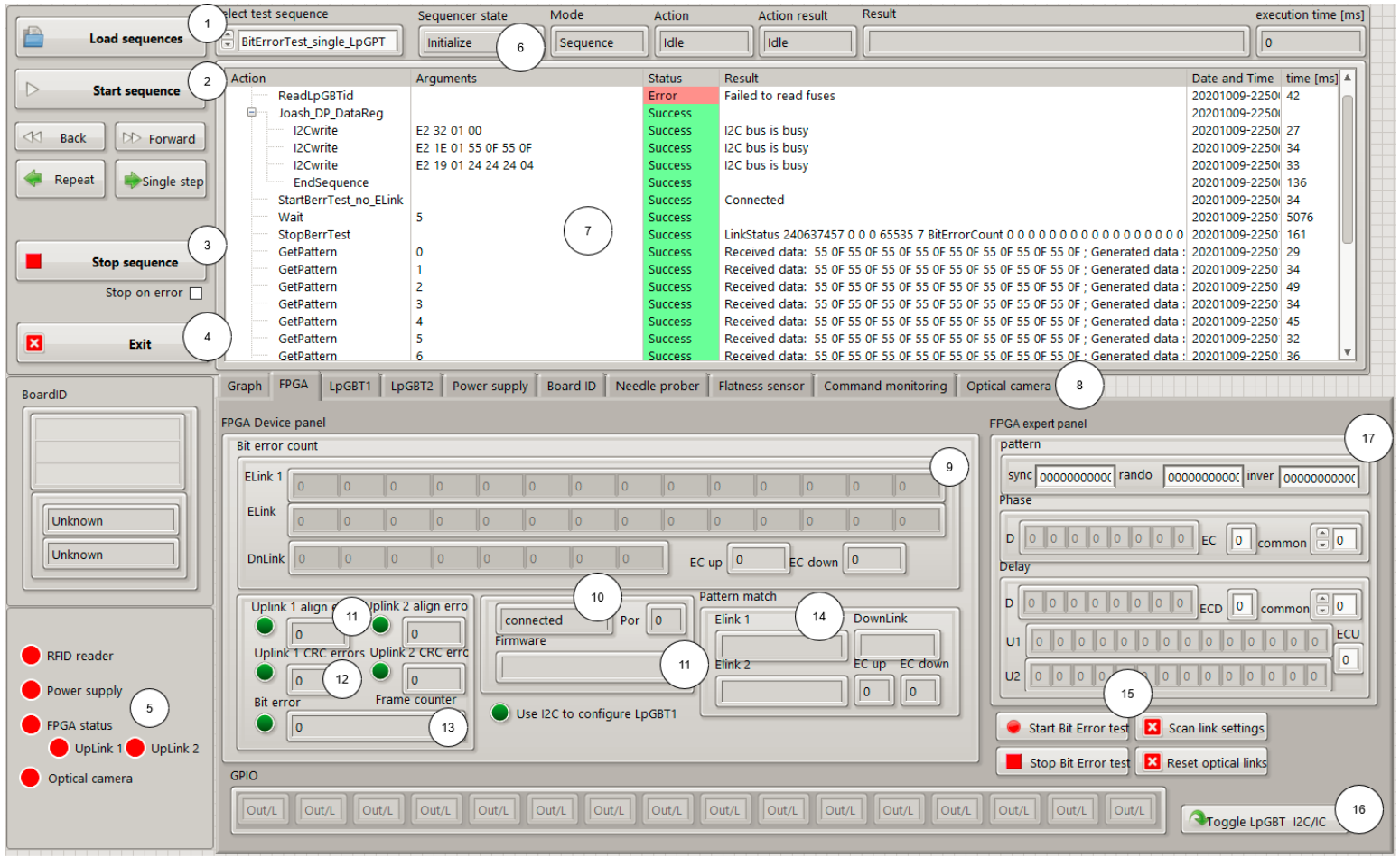



Figure 3.8: LabView Automation Software Front Panel Interface. Labelled items are described in the following Table

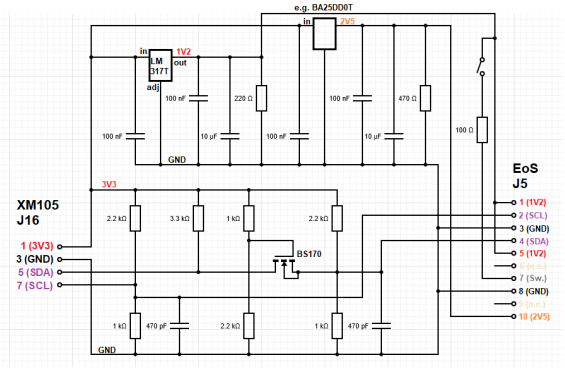
| Component | Current Drawn |
|---|---|
| lpGBT (without ADC) | 380mA [@1.2V] |
| ADC (lpGBT) | 1mA |
| Additional IO (lpGBT) | 10mA |
| VL+ | 180mA [40mA (Rx) + 14x10mA (Tx)] [@2.5V] |
| Total | 571mA |

Table 3.2: Detailed Power Budget for the EoS Card [48]

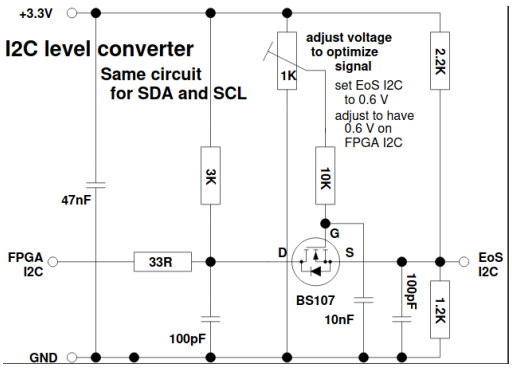
## 3.5 EoS card Configuration

The FPGA control board is the primary testing device for this experiment. The control board also provides access to the configuration registers of lpGBT. These configuration registers can be configured either through I2C or optical links. The lpGBT contains 3 independent I2C masters. The VTRx+ can only be configured through an I2C connection using the lpGBT I2C interface.

I2C configuration between the FPGA control board and the EoS card is facilitated through a bridging circuit. Initially the circuit design in Figure 3.9i was used, however it was discovered that the I2C connection was unstable and often requiring multiple I2C write transactions before a successful transaction. The I2C design was updated to Figure 3.9ii whilst the original circuit would still be used to produce the 1.2V and 2.5V power signals and toggle I2C/optical configuration. Although similar, the addition of the 33Ω resistor provided the added benefit of improved signal quality. Performance could also be tuned with a potentiometer such that the FPGA I2C signal matches the EoS I2C signal at 0.6V. Two of these updated circuits were created for both SDA and SCL I2C signals respectively.




(i) FPGA to EoS Level Converter, converting 3.3V to 1.2 and 2.5V, and I2C Bridging Circuit




(ii) Updated I2C Bridging Circuit with added 33Ω resistor for increased stability

Figure 3.9: Circuit Diagrams to Power and Connect the EoS card

### 3.5.1 I2C Bus

The lpGBT contains 3 independent I2C masters. The VTRx+ can also be configured through an I2C connection but only through the lpGBT. This experiment is performed on an EoS card which contains only one lpGBT master operating with only one I2C master interface.

### 3.5.2 Optical Links

Optical link configuration is enabled by an external switch as depicted on Figure 3.9i. When the switch is closed, the user can only configure via optical link and not through I2C and vice versa. Future revisions of the LabView software enabled the switch to be driven by a FPGA GPIO pin, allowing the user greater flexibility when choosing between the two configuration options. The protocol for optical link register configuration has been discussed in Section 2.1.2.

### 3.5.3 E-Fusing Procedure

The lpGBT allows for a default configuration for specific registers. This default configuration is loaded when the chip is powered on and is achieved by burning values in E-Fuses. E-Fusing is a delicate procedure since it momentarily exposes the lpGBT to high 2.5V line. The lpGBT is only rated for an total integrated time of 1 second at 2.5V. However the benefits of burning e-fuses are apparent. For example, the initial registers to configure optical link could be loaded upon startup without the need for the I2C bus. All register access can instead be accomplished though the IC protocol described in Section 3.5.2. Despite the benefit, the e-fusing functionality is still under development and would not be used in this experimental setup.

# Chapter 4

# Methodology

## 4.1 Main Experiment Design

The aim of the performed experiment is to demonstrate that the DSP stages within the lpGBT ASIC is susceptible to data corruption due to SEUs, therefore proving the hypothesis. The SEU rate is determined by the number of erroneous bits received as compared to known bits transmitted hence producing a Bit Error Rate. The uplink data path has 3 DSP stages of interest, namely the Scrambler, Encoder and Interleaver. Additionally the setup is constructed in a way, to detect SEUs within the stages themselves. To individually characterize the SEU rate for each stage, 3 additional BER tests are required.

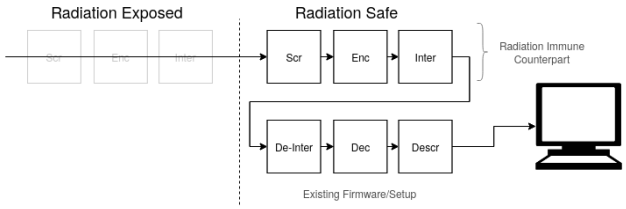
The additional BER tests developed provide radiation immune counterparts of the DSP stages emulated on the FPGA test bench. Each test iteratively activates stages on the irradiation lpGBT and deactivates the corresponding counter part on the test bench, thereby keeping the data path intact. By increasing the number of activated stages on the lpGBT, it is expected the SEU would also increase. The difference in SEU rates between tests could provide an indication whether an SEU occurred within a particular stage. The BER test are described in Table 4.1 and illustrated in Figure 4.1 whereby the stage characterized is indicated in green.

Alongside these main tests, this thesis also investigated the susceptibility of the FPGA test bench to SEUs. This was done to aid the main experiment and factor in possible SEUs that might have been induced in the FPGA test bench before characterizing the DSP stages. The methodology to test the test bench is described in Section 4.6.

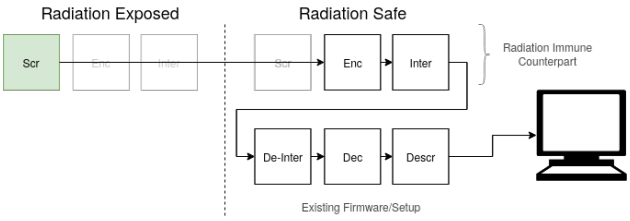
To realize these BER tests, both the firmware and LabView automation was developed and is discussed in Sections 4.4 and 4.5 respectively. Following which, the setup for the irradiation environment, in which the BER tests will be performed is discussed in Section 4.9.

| Test Number | Emulated Stages | Stage Tested |
|---|---|---|
| 1 | Scrambler, Encoder, Interleaver | Baseline |
| 2 | Encoder, Interleaver | Scrambler |
| 3 | Interleaver | Encoder |
| 4 | None | Interleaver |

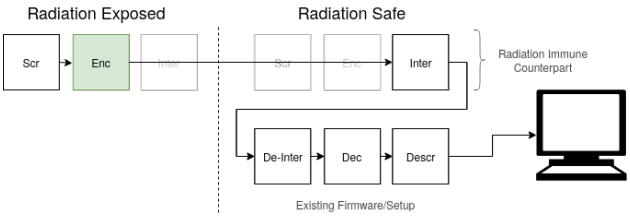
Table 4.1: Experiment Descriptions



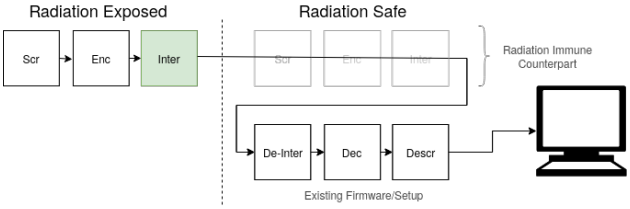

(i) Block Illustration of Test 1




(ii) Block Illustration of Test 2




(iii) Block Illustration of Test 3




(iv) Illustration of Test 4

Figure 4.1: Block illustrations for the 4 SEU characterization tests performed. By comparing the SEU rate to the previous test, the current test characterizes the SEU of the stage highlighted in green.

## 4.2 Bypassing DSP Stages and Turning TMR Off

The proposed experiment requires configuration of the lpGBT to be realized. The individual DSP stages within the lpGBT can be deactivated by means of the *Data Path* register [7]. Thus each test will require configuring this register with the desired value given in Table 4.2. The appropriate register value can then be plugged into the following sequence command.

I2CWrite E2 32 01 [User input]

| Experiment | Data Path Register Value | Stages Activated on the lpGBT |
|---|---|---|
| Test 1 | $0x07$ | None |
| Test 2 | $0x05$ | Scrambler |
| Test 3 | $0x04$ | Scrambler, Encoder |
| Test 4 | $0x00$ | Scrambler, Encoder, Interleaver |

Table 4.2: Experiment and Associated Data Path Register Value

Similarly the TMR functionality (described in Section 2.5.4) can be "deactivated" by disabling the clock for only one of the three branches at a time. Initially an investigation into turning off all but one of the branches was made, however closer inspection of the specifications proved this to be impossible. However, operating with only 2 branches effectively removes the effects of TMR on the BER rate as it can longer suppress errors by taking a majority vote. Further discussion of removing the effects of TMR are given in Section 5.2. The clocks for these branches are controlled by the *CLKTree* register [7]. The sequence command to deactivate one of the three branch clocks is given below.

I2CWrite E2 31 01 AC

## 4.3 Realizing a BER Test without E-Links

Emphasis was placed on reducing the uncertainty of observing SEUs (i.e. bit errors) from sources outside of the lpGBT and it's internal stages specifically. This would require distancing and or shielding the FPGA control board and PC from the irradiated EoS card. As aforementioned the typical BER test required a random pattern to be generated by the FPGA and sent to the lpGBT via E-Links. However using E-Links would create uncertainty should radiation interrupt the data transmission in the E-Links. Therefore it was decided that the lpGBT would be configured to send a constant pattern stored within internal registers of the lpGBT which would bypass the need to connect E-Links to the device.

Changing the test setup could be realised by exploiting the pattern syncing operation used to set the delay required for each E-Link. The lpGBT allows for a constant pattern of 32 bits to be transmitted for every E-Link. Initially the proposed pattern was "$55013F7F_{16}$" since this pattern provides an equal amount of 1 and 0 bits and matched a hard-coded sync pattern set within previous versions of the firmware. However it was discovered that the lpGBT was configured with a clock of 40MHz at 640 bits per second, this meant that the lpGBT was only transmitting 16 bits per clock cycle. Discussions with the DESY team led to modifications of the firmware which added functionality to modify the internal sync pattern. It was decided that both the internal sync pattern and internal constant pattern would be set to a $2 \times 16$ bit pattern instead. Hence the sync and internal constant pattern was set to "$550F550F_{16}$". It is noted that using a constant pattern imposes limitations on the experiment since a constant pattern does not mimic real-world operations as closely as a random pattern. However, this limitation is unavoidable as there is a fixed number of internal registers to store the data pattern nor a way change the behaviour of the lpGBT's pattern generation to anything other than what is defined in the specifications.

The steps to achieve a BER Test without E-Links are summarized as follows. The sequence instructions written to configure the lpGBT for operation without E-Links is provided in Listing A.2.

| **Step** | **Action** |
|---|---|
| Configure the LabView software to set the constant pattern and delay within the FPGA control board | Manually configured in the "Start_BerrTest_noElink" command. (See Section 4.5.2 for details) |
| Configure the DPDataPattern register to the constant pattern via I2C sequence command | I2Cwrite E2 1E 01 55 0F 55 0F |
| Configure the 7 UPLinkDataGroup registers to transmit a constant pattern | I2Cwrite E2 19 01 24 24 24 04 |
| Depending on the test being run, bypass the appropriate uplink stages | See Section 4.2 |
| Redo the above steps until the delay has been correctly set | The correct delay is evaluated with the aid of the "GetPattern" command (See Section 4.5.2 for details) |

Table 4.3: Summary of Steps and Associated Actions Required to Realize BER Test without E-Links

## 4.4 Firmware Development

The standard FPGA test bench firmware expects to receive a data packet that is scrambled, encoded and interleaved (See Section 2.1.2). However this will not be the case for most of the test iterations of the

performed experiment. Bypassing stages within the lpGBT will require the FPGA to emulate the operations outside of the lpGBT. CERN's GBTx team made available firmware modules which emulate the uplink stages in the lpGBT for testing purposes. Before the emulation firmware modules can be merged to the existing firmware, one needs to consider the order and size of the transmitted message at different stages of the uplink process and adapt the modules accordingly.

First consider the existing firmware which buffers incoming data packets of 64 bits in the lpGBT_Aligner firmware module. These packets of 64 bits are buffered over 4 clock cycles to construct a data packet of 256 bits. Using this data packet, the header bits are then located. The packet is then released if the header bits are found otherwise an empty packet is transmitted (packet consisting of "0" bits) and the data_aligned signal goes low. It is at this stage the data packet is descrambled, decoded and de-interleaved to recover the raw data. Consequently emulation of the scrambling, encoding and interleaving stages must be done after the lpGBT_Aligner but before the descrambler.

As described in Subsection 4.4.2, simulations demonstrated that the uplink frame is transmitted most significant bit (MSB) first, i.e. order of bits of the message is reversed during transmission. Therefore the messaged received would need to be reversed initially as to undo the effect of transmission. After scrambling, encoding and interleaving the message would then again have to be reversed to simulate transmitting the message. Listing 4.1 depicts the typical firmware code used to reverse the message.

Listing 4.1: Message Reversal Firmware

```
-- Reverse the message
for_gen_1 : for i in 0 to 255 generate
    upLinkDataPacket_1_rx_R(i) <= upLinkDataPacket_1_rx(255-i);
end generate;
```

As previously mentioned the encoder and interleaving stages contribute parity and header bits to the data frame. The structure of the uplink data frame is given in Figure A.1. This experiment will exploit the lpGBT ability to bypass these stages so that they may instead be emulated on the FPGA control board. It was confirmed by the lpGBT support group that the message frame size will not be altered if these uplink stages where bypassed. Thus the header and parity bits will always be appended to the message regardless of which stages were bypassed. In the case the encoder was bypassed the "dummy" parity bits appended could be ignored.

With these considerations in mind and depending on the test, the emulated DSP stages can be added as embedded modules to the "HighSpeedLink" firmware modules. These would be included after the Aligner but before the de-interleaver, decoder and descrambler embedded modules shown in Figure 3.3. Three

additional firmware variants were also created by the author to realise the tests expressed in Table 4.1 Note Test 4 is equivalent to the original firmware setup.

### 4.4.1 Summary of Firmware Development Required

The modifications to the firmware can therefore be summarized into the following steps:

1. Receive and locate the header bits using lpGBT_Aligner module
2. Reverse the message
3. Depending on the test performed, transform the message using the emulated stages
4. Reverse the message to simulate the transmission from the lpGBT
5. Undo the transformations by passing the message through the existing firmware stages

### 4.4.2 Simulation

In order to validate the firmware modifications, the firmware data path was simulated in Vivado to test behavioural correctness. The simulation was done by creating a VHDL "testbench" module. The testbench module instantiated the respective emulation modules as well as the descrambler, decoder and de-interleaver. Furthermore the BERCounter module was also included in the testbench module to ensure timing between the modules was correct. The testbench module requires simulated data that would resemble the output of the lpGBT. Simulating the data was done using a finite state machine within the testbench module for which every clock cycle would generate a packet of 64 bits. These 64 bit packets would then be reversed (to simulate the transmission of the frame from the lpGBT, as previously mentioned) and sent to the lpGBT_Aligner module to buffer the data and produce a full 256 bit frame every four clock cycles. The code of the 64 bit packet generation is shown in Listing 4.2. The structure of full frame after aligning is discussed in the GBT Protocol for Section 2.1.2. The header is set to the expected "$10_2$", the IC_Data is set a constant pattern of zeros and since the encoder is turned off the FEC data is also set to a constant pattern of zeros. Finally, as explained in Section 4.3, the pattern itself is set to "$550F_{16}$"

Listing 4.2: State Machine to Simulate Input Data

```
stim_proc : process(RXUSRCLK2_1)
begin
    if rising_edge(RXUSRCLK2_1)
    then
        case sim_cntrl is
        when b"00" => rxdata_1 <= HEADER(1 downto 0) & DUMMY_IC_DATA(9 downto 0) & PATTERN
            (63 downto 12);
```

```
        when b"01" => rxdata_1 <= PATTERN(11 downto 0) & PATTERN(63 downto 12);
        when b"10" => rxdata_1 <= PATTERN(11 downto 0) & PATTERN(63 downto 12);
        when b"11" => rxdata_1 <= PATTERN(11 downto 0) & PATTERN(63 downto 32) & DUMMY_FEC
            (19 downto 0);
        when others =>
        end case;
        sim_cntrl <= sim_cntrl + 1;
    end if;
end process;
```

The results from the simulation are illustrated in Figure 4.2. The uplinkDataPacket_1_rx signal represents the "transmitted" (order reversed) generated data. Moving down the signal list, we see the data stepping through all the DSP stages with the highlighted signal indicating the correctly recovered data. Furthermore, BERCnt is zero indicating that the BitErrorCounter module is also functioning correctly with this modified firmware.

Note the simulation described above corresponds to Test 1 which emulates all the DSP stages. The tests thereafter will incrementally remove stages whilst the stages left emulated would still expect data that is processed by the removed stages. Thus keeping the data path intact. Therefore simulation results for all tests are identical to Figure 4.2 as the testbench module would still need to include the "removed" stages to keep the data path intact.

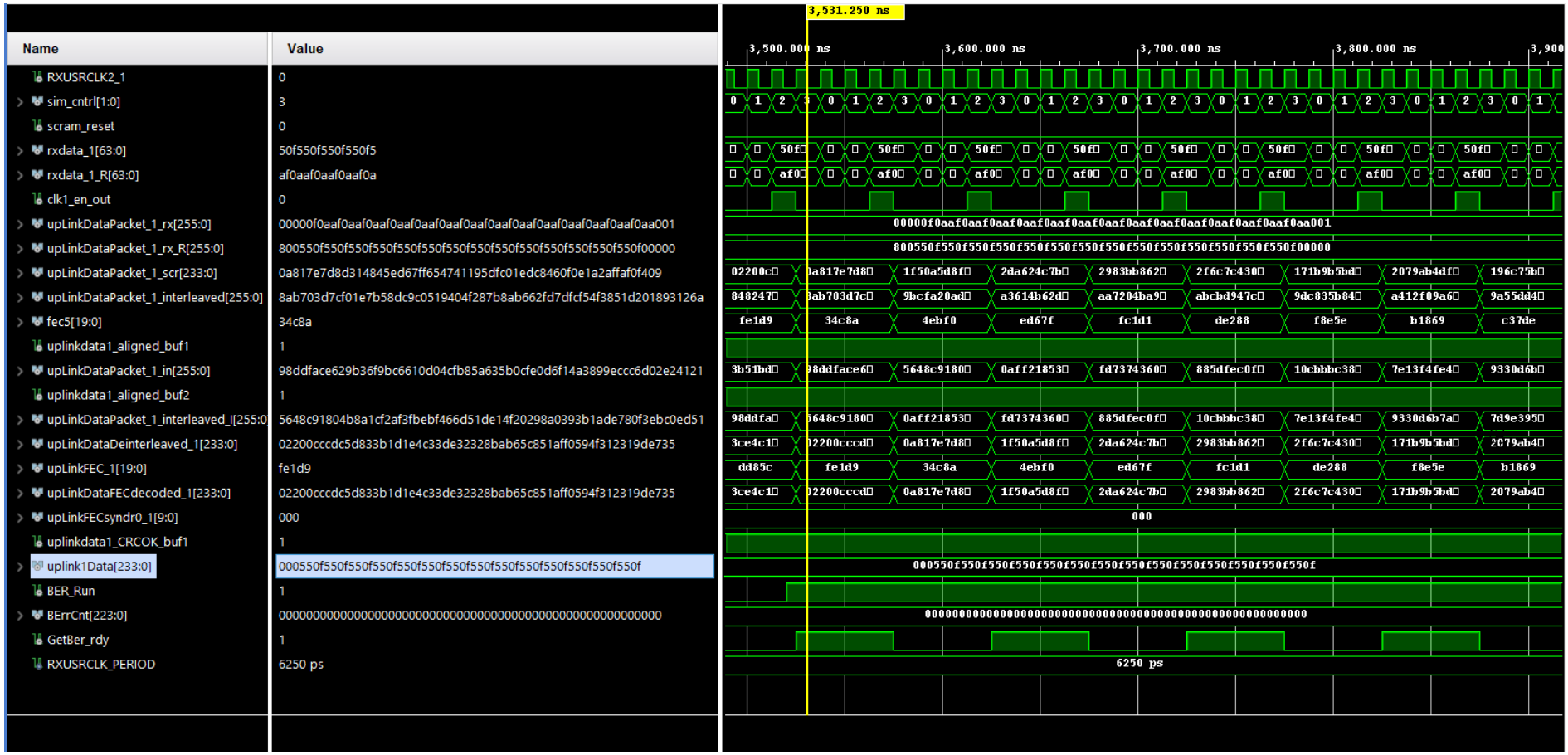



Figure 4.2: Simulation result from Test 1 setup illustrating from top to bottom the data flow of the DSP processing stages within lpGBT and then recovery by the FPGA. The highlighted signal in blue shows the fully recovered expected message after all DSP stages.

## 4.5 LabView Development

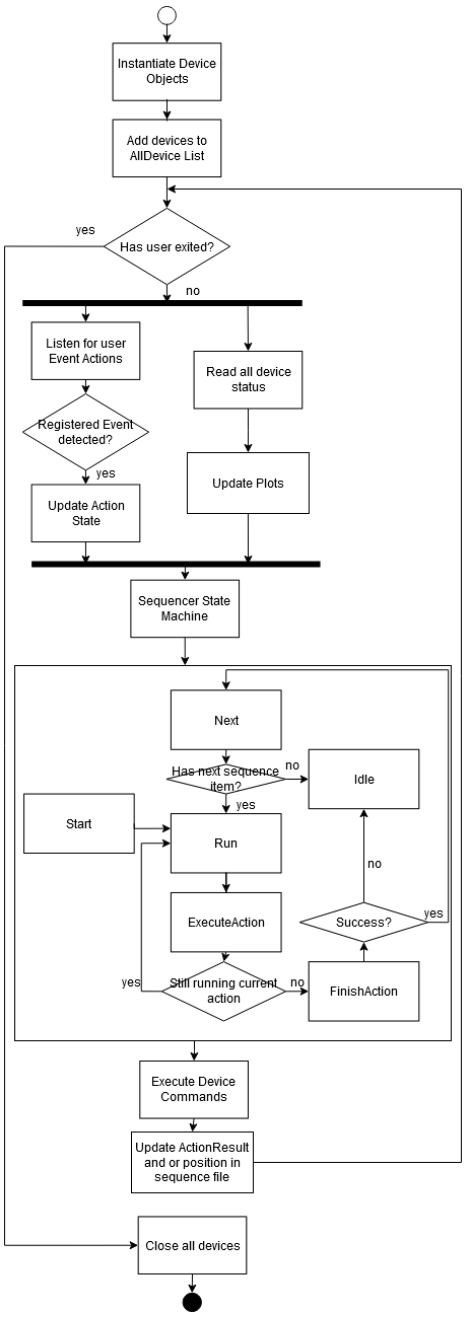



Figure 4.3: LabView Main Program Algorithm. Action State holds the current sequence or action to be executed. The sequencer state machine monitors the status of the action from "Initialization" to "Finish."

As of writing, a LabView test bench application is under development to automate the testing configuration and procedures for the EoS cards at production. This Section provides an overview of the modifications and extensions made to the LabView software for the purposes of this experiment. These can be summarized to achieve the following 3 items.

1. Extended the list of LabView supported list of sequences to realize a BER test without E-Links
2. Log and timestamps BER status information
3. Extract, log and timestamp internal temperature and voltage information using the lpGBT's internal temperature sensor and 10 bit ADC

### 4.5.1 Overview

Typically each device connected (e.g. KintexBoard, Climate Chamber etc.) has a dedicated LabView class which inherits from a parent Device class. The devices relating to the BER test include the EoS card (Kintex_lpGBT module) and the Kintex FPGA control board. Although the Kintex FPGA control board is a single device it is split into two modules namely the Kintex_BERT and Kintex_FPGA modules. The BERT module handles the functionality relating to the configuring and monitoring the BER test whereas the FPGA module specifically handles making the initial connection to the board at startup. The Kintex control board has multiple input/output connections to the EoS card including the I2C, optical link and E-Link interfaces. These input/output connections are handled by a separate KintexIO module. A simplified class diagram for the LabView classes is provided in Figure 4.4.

At the start of the main program all available devices are instantiated and added to an AllDevices object. Devices classes generally inherit and implement their own DeviceRead and DeviceCommand modules associated with them. The AllDevices

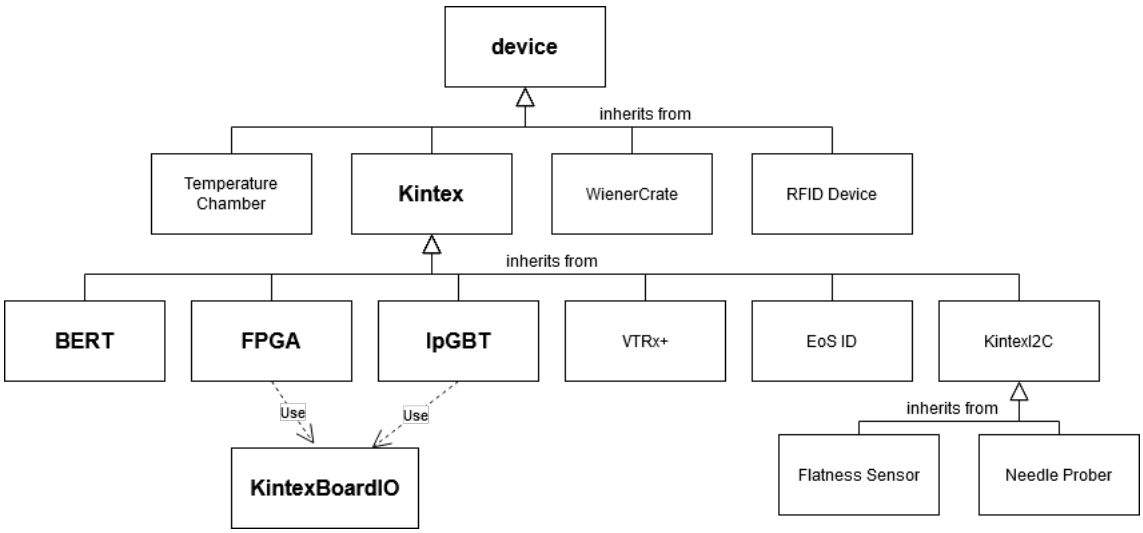



Figure 4.4: Simplified UML Class Diagram for LabView Objects. The device classes used by this experiment is highlighted in bold.

object simplifies the task of reading, plotting values and executing commands for all devices by having a single module to cycle through the instantiated devices when needing to read, plot or execute device commands.

The main program runs in a while loop which will terminate when the user exits the program. User interactions map to events for which the program will respond. An event structure in the main loop of the program handles the interrupts from user and will map the interaction to an appropriate device command through a ActionState typedef. The ActionState typedef is an alias for a LabView enum object (identical to a enum in C). Alongside user interactions the ActionState can be selected from the Sequence file functionality discussed in Section 3.3. Once the appropriate ActionState has been selected from either user interaction or iterating through sequences in the loaded sequence file, a Sequencer State Machine is tasked with executing the task from Initialization to Finish. If iterating through the sequence file, the state machine will update the ActionState to the corresponding next action. This is shown in Figure 4.3 which provides a graphical overview of the main program algorithm.

Functionality for loading application specific configuration data was provided by DESY. Upon startup this configuration file will provide configuration data such as the directory to store data logs, default sequences file, options for optical vs I2C configuration etc. An example of this configuration file is provided in Listing A.4.

### 4.5.2 Realizing BER Tests

The Labview software was modified to include the GetPattern and SetSyncPattern commands as documented in [10] in order to realize the proposed BER tests. Modifications allows the user to call these commands

through a sequence entry as described in Section 3.3. These commands were added by first updating the Actions enum type and adding the subsequent cases to case structure within the Kintex_BERT DeviceCommand VI. The SetSyncPattern command was bundled into a new sequence entry "StartBerrTest_no_Elink" which configured and started the BER test.

As explained in [10] there will be a delay between pattern generator and the data from the E-Links. This delay is not known a priori, hence the purpose of the GetPattern command. If the received pattern for any ELink channel does not match the generated expected pattern, for instance due to the delay, then both received and generated patterns will be "locked" into a FPGA register. The locked patterns can be unlocked by setting the unlock bit for the SetELink parameter data. The locked pattern for each ELink can be retreived using the GetPattern command and hence the delay can required can be determined. The delay and sync pattern are hard-coded in the "StartBerrTest_no_Elink" case statement in Kintex_BERT DeviceCommand (highlighted in red in Figure 4.6).

### 4.5.3 ADC Module Development

The lpGBT features a 10 bit ADC. Monitoring of the lpGBT internal temperature and voltage during the BER test is useful to identify external disturbances which may induce errors. As such the LabView software was extended to read and log the lpGBT internal ADC during the BER test. The user can configure the ADC by selecting both the positive and negative channels and the gain of the ADC. Configuring and reading the ADC is achieved through the following register access procedure.

1. Configure the ADC
2. Enable the ADC and start the transaction
3. Wait for the ADC conversion bit to finish
4. Read the result which is spread over two registers

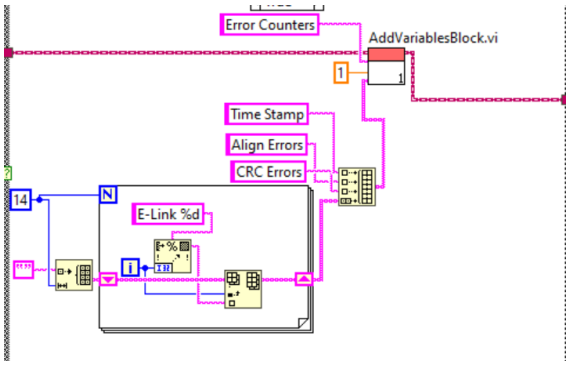
The ADC functionality was achieved through a new LabView module, "ADCRead" belonging to the lpGBT class. See Figure 4.6. Additional functionality to cycle between multiple ADC channels was also included. The register access to the ADC was done with the KintexLPGBTRegister write and read modules in the KintexBoardIO class. These modules will either use optical link or I2C interface depending on the register access mode selected.

### 4.5.4 Log and Timestamp Information

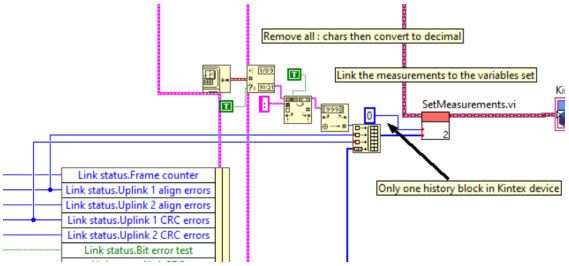
Existing functionality to log data with the LabView software was provided by the parent device class and composite DataHistory class. The software modifications required to add a measurement to log is outlined below. The UML diagram in Figure 4.6 highlights the effected Virtual Instrument files (VIs) in green.

1. Edit the configure channels VI to create measurement block for when device object is instantiated. See Figure 4.5i. A measurement block is an arbitrary collection of measurement values

2. Add measurement to the appropriate DeviceRead command. Essentially the values obtained by the DeviceRead command are passed and stored in the selected measurement block. An excerpt is provided in Figure 4.5ii to illustrate this further.




(i) LabView code excerpt to add measurement block. Here the empty variables "Time Stamp", "Align Errors", "CRC Errors" and an array of 14 E-Links is added to a variables block called "Error Counters"




(ii) LabView Code excerpt to log the time, align and CRC to the previously defined "Error Counters" variables block

Figure 4.5: LabView Excerpts to Accomplish BER status Logging

At runtime the measurement functionality is executed in the following steps:

1. On instantiating, the devices' configure channels method is called adding the corresponding measurement blocks to the device

2. On every cycle the DeviceRead command is executed for connected devices

3. Within the device read command are calls to the add values to the corresponding measurement block

4. Thus every clock cycle the device will write to measurement values to a log file

### 4.5.5 Additional Contributions

Additional contributions towards a graphical interface for register configuration included changes to the front panel, "FormatBitInput" and "FormatRegInput" helper classes and new device commands in the "Kintex_lpGBT" class to handle user interactions. All these changes are highlighted in blue in Figure 4.6. A screenshot of the panel is provided in Figure A.8. These contributions significantly simplify the register configuration process for use cases such as this experiment. As a result, this work has been adopted

and integrated into the DESY production test stand stack and will see use beyond the conclusion of this investigation.

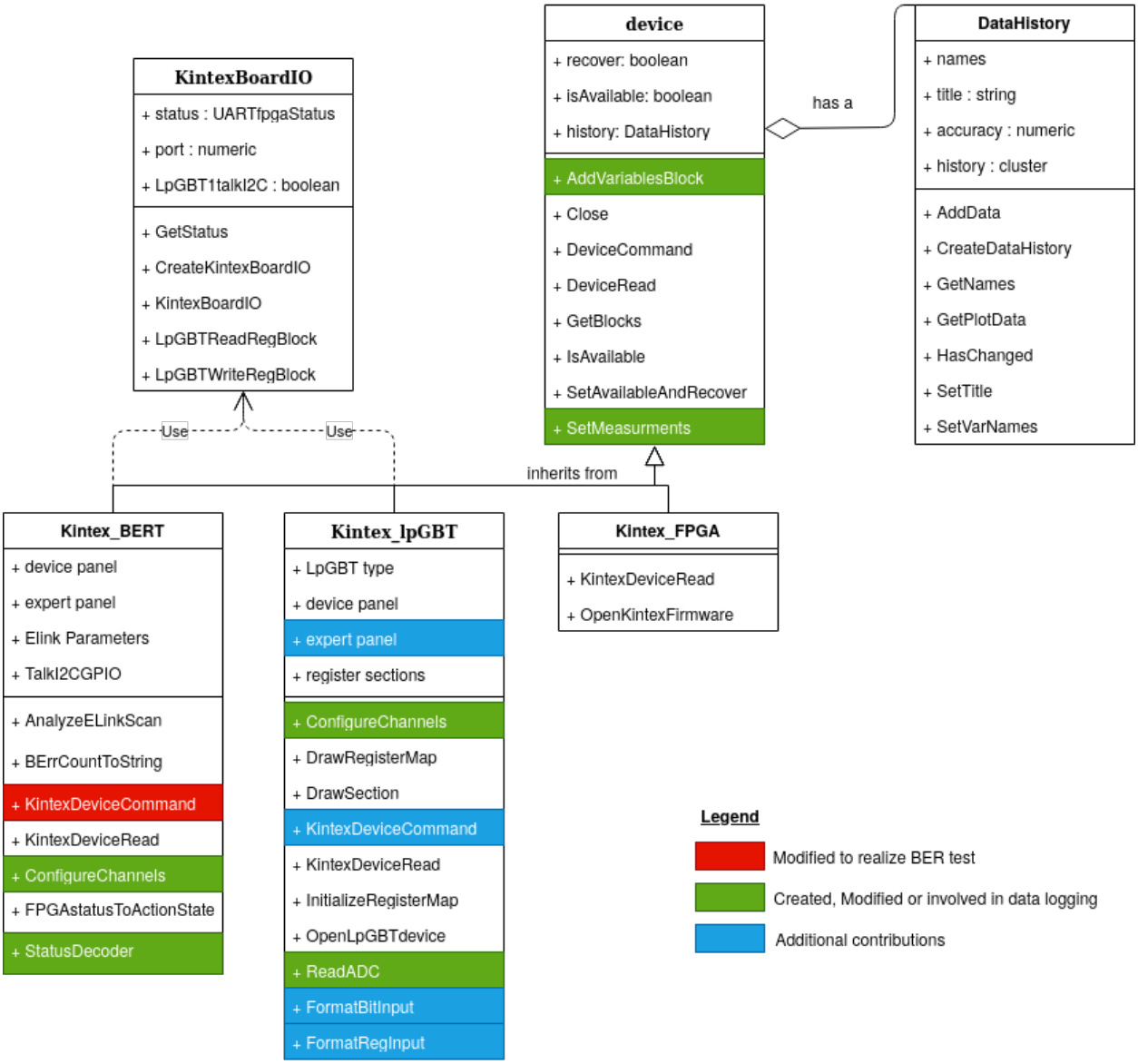



Figure 4.6: Detailed UML Diagram of LabView Classes Used/Modified. VIs highlighted in red were modified to configure the BER test without E-Links. VIs highlighted in green were modified for the logging the BER test data in real time. Finally VIs highlighted in blue added functionality for the register GUI.

## 4.6 Characterizing SEUs for the Testbench Equipment

This experiment was realized with the aid of a second Xilinx KC705 Evaluation FPGA board. The second FPGA emulates the entirety of the uplink path for the EoS card including generating, preparing and optically

transmitting the data to the original testbench FPGA. Its purpose is to demonstrate that the FPGA is invulnerable to radiation while running under the same conditions that the emulation tests will be performed. The following sections briefly describe the setup stages required.

### 4.6.1 Data Generation

Data generation for both the BER tests, described in 4.1, was done in the ELink module. This module could be reused to generate data for the emulation FPGA. The ELink module is a highly configurable module which originally accepts parameter data from the SetELink module. To reduce complexity the SetLink module was omitted and the following parameter data was hard-coded into the ELink module. The values for this parameter is found in Table 4.4. Furthermore, to increase randomness, the SyncPattern was modified from a single 64 bit pattern to $4 \times 64$ bit patterns. The ELink module was further modified to iteratively transmit the 4 patterns with the use of a "pattern_contrl" signal, as shown in Listing 4.3.

| **Parameter** | **Value** |
|---|---|
| Delay | 0 |
| SyncPattern | X"550103070F1F3F7F",X"FFFFFFFF00000000",X"0F1F3F7F55010307", X"00000000FFFFFFFF" |
| SyncPatGen_on | All ELinks to transmit the Sync Pattern |
| TestPatGen_on | Ignored |
| HighInv | Ignored |

Table 4.4: Hard-coded BER parameter values for FPGA to FPGA setup

Listing 4.3: Pattern Generation

```
type t_4x64 is array(3 downto 0) of std_logic_vector(63 downto 0);
constant PATTERN_MATRIX : t_4x64 := (X"550103070F1F3F7F",
                                     X"FFFFFFFF00000000",
                                     X"0F1F3F7F55010307",
                                     X"00000000FFFFFFFF");
signal pattern_cntrl : std_logic_vector(1 downto 0) := B"00";

process (clk160) begin
if rising_edge(clk160) then
    if clk_en = '1' then cnt <= B"01";
    else cnt <= cnt + 1; end if;

    if cnt(0) = '0' then
```

```
pattern_cntrl <= pattern_cntrl + 1;

for j in 0 to 13 loop -- For every ELink
    for i in 0 to 7 loop -- For every byte in sync pattern (8x8bits=64bits)
        data_selio(i*14+j) <= PATTERN_MATRIX(conv_integer(pattern_cntrl))(63-
            conv_integer(SyncCount)*8-i);
        -- Sort the elink bits to each group:
        data_elinks(j)(i) <= data_selio(i*14+j);
```

### 4.6.2 Data Preparation

The data preparation stages (i.e. scrambler, encoder and interleaver) are provided by CERN and are implemented identically to Test 1 of the main experiment. (See Table 4.1) Finally, before reaching the transceiver the message was reversed as shown in Listing 4.1 to emulate the behaviour of the EoS when transmitting data.

### 4.6.3 Optical Transceiver

The generated and prepared data was transmitted optically using the KC705 integrated transceiver. Interfacing with the transceiver was performed using HDL wrapper provided by the LogiCore 7 Series FPGA transceivers Wizard [49]. The wizard was configured to transmit a frame of 64 bits at a rate of 10.24 Gbps. The two FPGAs are connected using 5m LC/LC optical fibre cable.

### 4.6.4 Clock Sharing

Unlike with the EoS card, this setup did not support clock recovery as the lpGBT team did not provide clock recovery IP cores. Thus both transmitting and receiving FPGA transceivers required a 160 MHz differential signal clock pair. The original control bench would generate two 160MHz differential signal clocks. The first used for its own transceiver whilst the second pair was connected to the emulating FPGA via 30cm male/male SMA cables. The setup clock connection and optical link is illustrated in Figure 4.7.

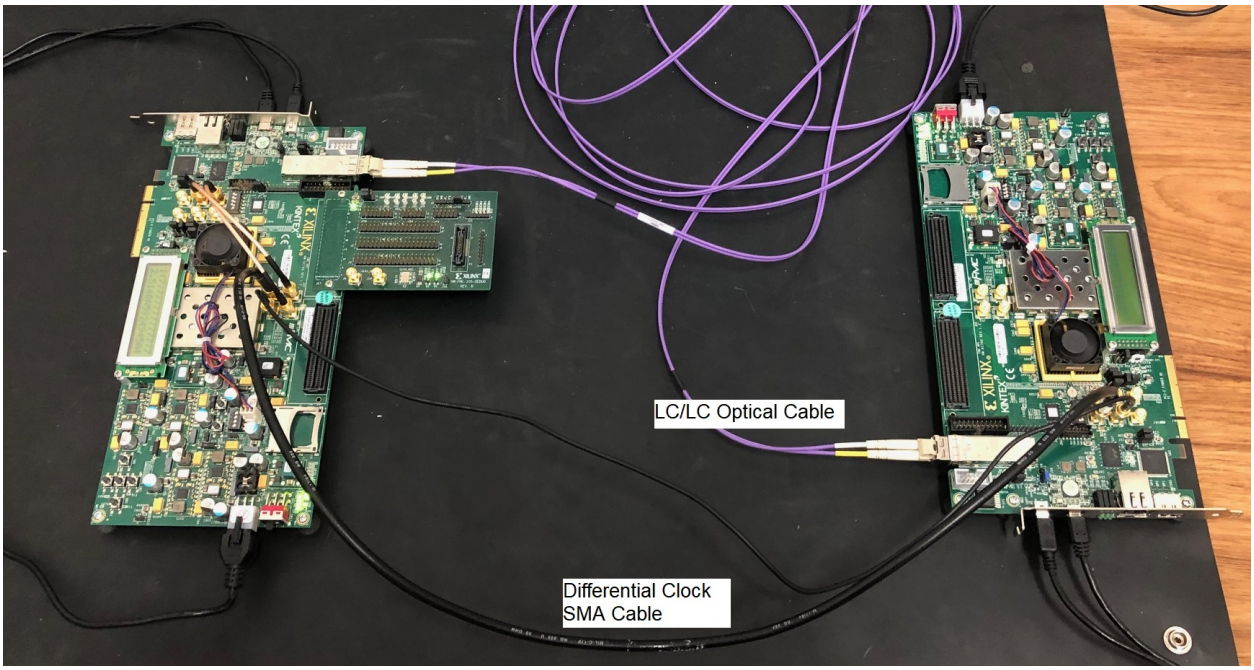



Figure 4.7: FPGA to FPGA BER setup with a shared clock signal since the FPGA emulating the EoS card does not recover a clock signal from the downlink

## 4.7 Sequence Files

After all the aforementioned firmware and LabView modifications were made the resulting sequence files used to configure the irradiation tests for the EoS are provided in Listings A.1, A.2 and A.3. The FPGA to FPGA BER setup used a sequence file similar to Listing A.3.

## 4.8 Stability of the Test Setups

Stability runs for the four tests were run without irradiating the lpGBT for average of 9 hours per test. This was done to observe that the setup was indeed stable and that no external disturbances would effect the results. Furthermore, obtaining a BER for each of the tests without radiation provides a baseline result which can be used to compare to the results with radiation, therefore distinguishing between errors caused by external disturbances and errors caused by SEUs.

### 4.8.1 FPGA GPIO Power Supply Challenges

As previously mentioned in Section 3.4 the EoS card can be powered from a single 3.3V with the aid of a level-converter circuit. Initially the 3.3V was supplied by a GPIO pin from the FPGA control bench. Running a BER test for 3 hours to test the stability of setup produced results illustrated in Figure 4.8.

The number of correctable errors has a maximum of 65535. Using an oscilloscope trigger it was discovered the signal supplied by the FPGA control board would momentarily drop 12% lower than the expected 3.3V during the BER test. This directly effected the expected outputs of the level-converter. The $V_{DD}$ of the lpGBT has a tolerance of 10% [7]. Thus the sudden burst in errors could be attributed to the lpGBT operating below specification. Changing the source of the 3.3V to an external power supply corrected the issue and produced stable results for 56 hours as recorded for Test 4 in Table 5.3.

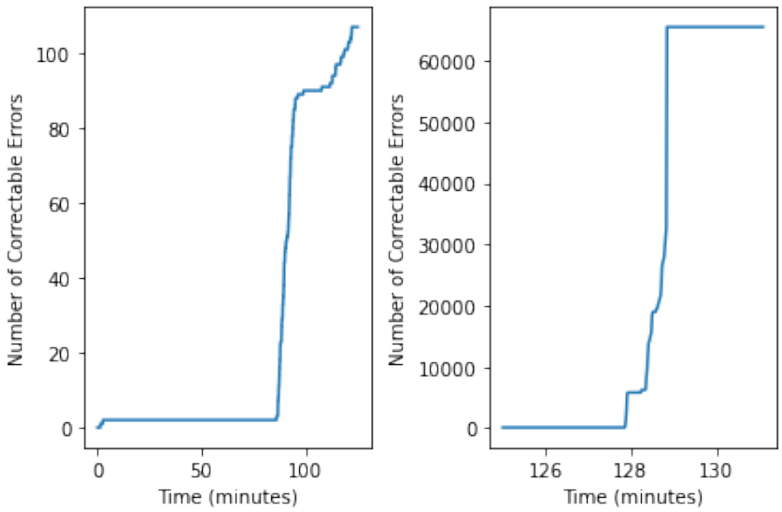



Figure 4.8: Number of correctable errors increases in two short spikes from FPGA GPIO Powered EoS Card

### 4.8.2 E-Link Challenges

To test the correctness of the experimental setup, BER tests were performed without exposure to radiation. The results from those tests are presented in Table 5.3. The test bench with firmware emulating the scrambler initially produced corrupt data for 3 E-Links. This is shown in Figure 4.9. The cause of this problem was not resolved and this behaviour was consistent between two different EoS cards. Thus a BER test with only 11 active channels was performed. This required modification of the LabView "Start_BERTest_no_elink" sequence command to configure the firmware to only evaluate data received by the working 11 E-Links. Calculating the BER rate would therefore substitute in 11 active E-Links as opposed to the expected 14 for all tests.

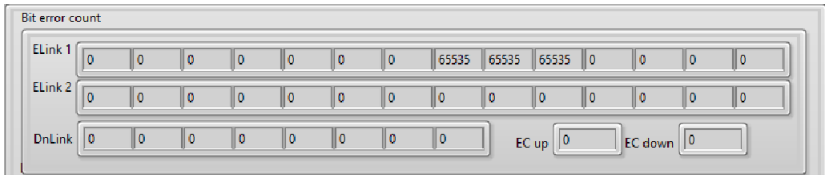



Figure 4.9: LabView Screenshot illustrating 3 E-Links not working when bypassing the scrambler on the lpGBT

After addressing the aforementioned challenges, the results for final stability tests are presented in Section 5.3. It was concluded the setup was stable and that data corruption due to external disturbances would not influence the irradiation BER results.

## 4.9 Irradiation Environment Experiment Setup

The irradiation test was performed in the n-lab at the University of Cape Town with the Department Physics. The n-lab offers two neutron sources namely; an MP Sealed Tube Neutron Generator (STNG) and a 220 GBq Americium-Beryllium (AmBe) radioscopic source. The AmBe source was chosen as it offers a board spectrum of energies from thermal neutrons to 11 MeV as opposed to the monoenergetic 14 MeV STNG beam. As discussed earlier this is in alignment with neutron sources used in [29], [30].

**Source** Neutrons can be obtained from an Americium-Beryllium radionuclide source (shown in Figure 4.11) due to the chemical processes illustrated in Equations 4.1 and 4.2. In summary, the Americium (Am) undergoes $\gamma$ decay. It is the released $\alpha$ particle which then reacts with Be to produce a neutron. The source produces $10^5$ neutrons a second for a solid angle of $4\pi$ steradians (i.e. radiating spherically) [50]. The energy spectrum of the source is illustrated in Figure 4.10 and shows most neutrons emitted having an energy of approximately 4 MeV and up to a maximum 11 MeV.

$$^{241}_{95}\mathrm{Am} \longrightarrow {}^{237}_{93}\mathrm{Np} + {}^{4}_{2}\alpha^{2+} + \gamma 59.5\mathrm{keV} \tag{4.1}$$

$$^{9}_{4}\mathrm{Be} + {}^{4}_{2}\alpha^{2+} \longrightarrow {}^{12}_{6}\mathrm{C} + {}^{1}_{0}\mathrm{n} + \gamma \tag{4.2}$$

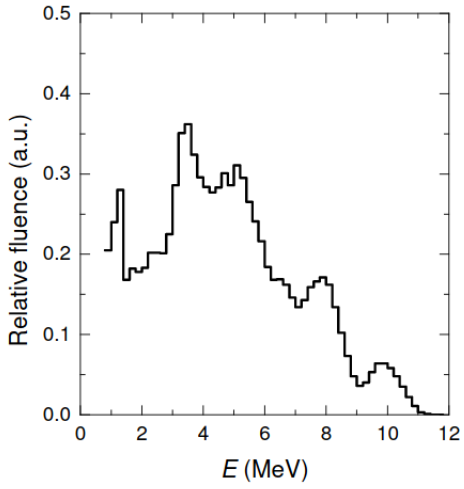



Figure 4.10: Energy Spectrum of AmBe Neutron Source [50]


Figure 4.11: Americium-Beryllium cylindrical source placed on a FPGA emulating the EoS lpGBT stages

**Fluence** The lpGBT has a surface area of $9 \times 9mm^2$ [7]. The source is placed directly on the lpGBT however for simplicity the distance between the lpGBT ASIC and source is taken to be 1cm. At 1cm one steradian has an surface area of $1cm^2$. Dividing the area of the lpGBT by the surface area of a steradian at 1cm $A_{1cm}$ produces the steradians subtended by the lpGBT. As previously discussed, the source produces $\frac{10^5}{4\pi} = 7958$ neutrons per steradian per second [50]. Therefore multiplying the steradians subtended by the lpGBT by the neutrons produced per steradian per second results in the flux through the lpGBT as shown in Equation 4.3.

$$Flux_{\,lpGBT} = \frac{A_{lpGBT}}{A_{1cm}} \times Neutrons\,per\,steradian\,per second \tag{4.3}$$

This results in the lpGBT being exposed to 6445.78 neutrons per second. For reasons discussed in Section 5.5 each radiation test runs for 36 hours or 129600 seconds. Thus the fluence of exposed lpGBT per BER test is calculated to be $835.37 \times 10^6$ neutrons per $cm^2$.

Figure 2.6 illustrates that at a distance of 120cm from the beam (the white area) within the ATLAS ITk has an expected total fluence of $10^{14}$ neutrons per $cm^2$. Assuming this fluence is produced over 5 years ($10^8$ seconds) the flux of this region can be calculated to $10^6$ neutrons per $cm^2$ per second. Therefore ignoring neutron energy effects, the total radiation dose received by the lpGBT in a BER test corresponds to 1 second of nominal ATLAS ITk data taking account this calculation is a rough order-of-magnitude estimate for the

region in which radiation flux is minimal.

**Shielding** For testing involving radiation, the source and device under tested needed to be shielded with paraffin wax blocks and blocks coated with boron. Shielding provided safety to persons within the lab as well as shield the test bench from being susceptible to SEUs. Figure 4.12 illustrates the shielded experiment setup.

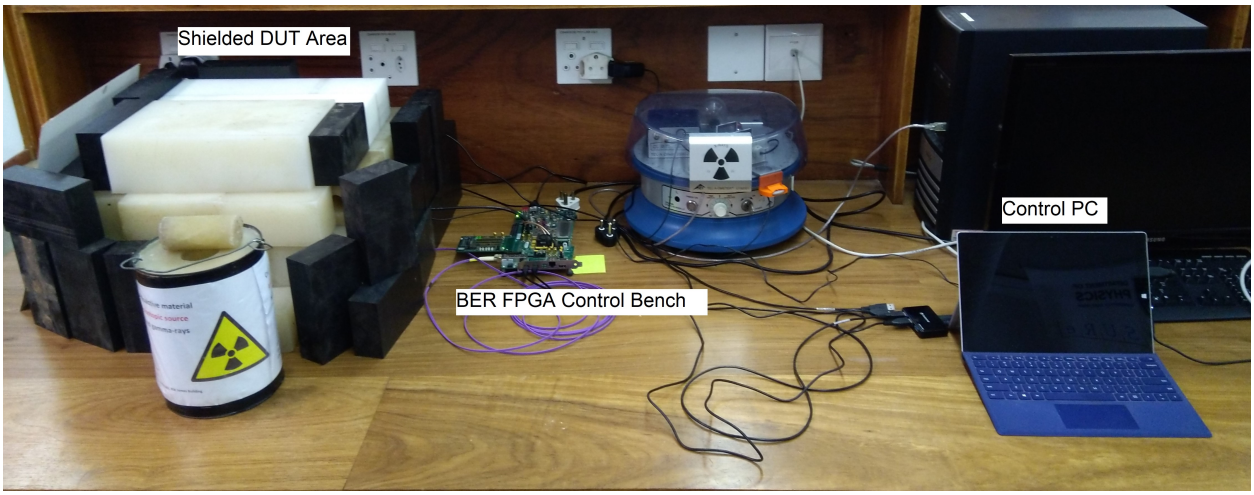



Figure 4.12: Experiment setup with the shielded area which houses the irradiated EoS card or FPGA emulating the EoS shown on the left

# Chapter 5

# Results and Discussion

Chapter 4 outlined the current test bench setup and the modifications required to realize this experiment setup. This chapter presents the results obtained from the experiment. The Bit Error Rate is expressed as a fraction of number of errors by total number of bits transmitted. The LabView setup quotes the total number of frames transmitted hence the multiplying by the total number of active data bits in the frame (frame structure remains the same even when deactivating E-Links) will produce the total number of bits transmitted. Note the number of frames increases at a rate of $40 \times 10^6$ (discussed in detail in Section 2.1.2). In the case no errors occurred, the BER is quoted as an upper limit instead of an exact figure.

$$BitErrorRate = \frac{No.Errors}{No.Frames \times (No.activechannels \times 16bit/channel)} \tag{5.1}$$

## 5.1 Interpreting Correctable, Non-Correctable and Alignment Errors

A *correctable error* counts the number of times a frame is corrected by the RS decoder. More specifically when the calculated syndrome is non-zero, causing the CRC error counter to increase, and assuming the size of the burst error is within the error correction capabilities of the encoding scheme. These errors are meant to be indicative of an upset occurring during optical transmission (unless the burst error is larger than the error correction abilities of the lpGBT).

*Non-correctable errors* are counted per E-Link. The maximum numbers of errors counted per E-Link is 65535. These errors are counted by comparing the received and decoded pattern to the expected pattern. The aim of this experiment is to test the susceptibility of the individual DSP stages itself. In the case an SEU occurs within the DSP circuitry it is expected this will result in a non-correctable error. For example, errors occurring within the encoder stage will result in the incorrect calculation of the parity bits and thus

cannot be restored on the receiving end. This follows for the scrambler and interleaver as an upset here will fail to be correctly reversed on the receiving end. An upset which effects the majority voter of TMR will also show up as a non-correctable error.

*Alignment errors* are frames counted when the header ($10_2$) of a frame is not detected by the Aligner firmware module. Alignment errors have a significant impact on BER since if the frame is not aligned the whole frame is lost. It should also be noted that if a frame is lost due to alignment, the number of non-correctable errors will not increase. Therefore errors due to misalignment must be calculated using Equation 5.2 and added to non-correctable errors counted.

$$AlignmentErrors = FramesMisaligned \times ActiveChannels \times 16bit/channel \tag{5.2}$$

Table 5.1 provides a summary of the possible outcomes from running a BER test.

| **CRC Errors** | **Non-correctable Errors** | **Alignment Errors** | **Scenario** |
|---|---|---|---|
| Yes | No | No | Error was detected but corrected before being compared to expected pattern |
| No | Yes | No | Although the decoder did not detect any errors in the received message; the message did not match the expected pattern. This could be due to wrong expected pattern set, incorrect delay set or corruption of data before the encoding process |
| Yes | Yes | No | Possibilities include misconfigured lpGBT/firmware or burst error larger than the correcting capabilities of the encoding process. |
| Yes | No | Yes | Upset within the header bits of frame |
| Yes | Yes | Yes | Optical link disconnected |

Table 5.1: Summary of possible scenarios that can be inferred from the BER test error results

## 5.2 Considering the Effects of TMR on the BER Result

Deactivating one of the three effectively removes effects of TMR from the experiment as the majority voter cannot fully suppress errors with only 2 branches. Deactivating a TMR branch is accomplished by stopping one of the triplicated clocks through a register configuration [7]. However it is worth considering the possible

outcomes for the majority voter in Figure 5.1 and Table 5.2. Consider A is the deactivated branch, B is the expected branch and C is the branch for which a SEU is introduced. Given branch A is indeterminate it is assumed there is a 50% chance A will match B, thus causing errors to go undetected due to the majority voter. This effect can be corrected for by multiplying the number of errors detected by 2. However for simplicity this adjustment was not made for the BER results given in the following sections.

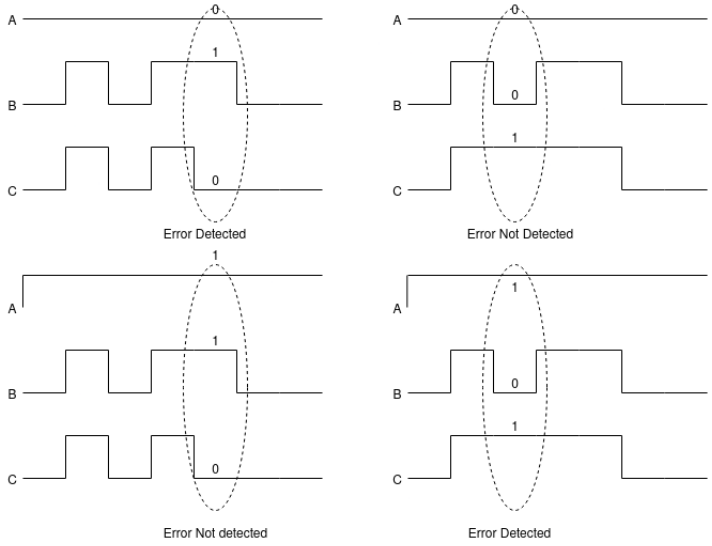



Figure 5.1: Timing Diagram Showing the Possible Outcomes for TMR with 2 Activate Branches

| A | B | C | Outcome |
|---|---|---|---|
| 0 | 1 | 1 | Error Detected |
| 0 | 0 | 1 | Error Not Detected |
| 1 | 1 | 0 | Error Not Detected |
| 1 | 0 | 1 | Error Detected |

Table 5.2: Truth Table illustrating the possible outcomes for TMR with Activated branches

## 5.3 Results before Radiation (Setup Stability)

Stability tests without radiation are presented in Table 5.3. Note for reasons previously discussed in section 4.8, the BER was calculated considering only 11 of the 14 E-Links. No errors were observed after running the tests for an average time of 8 h 57 m 36 s per test. Although more extensive stability tests are needed, the results here indicate that the error rate from noise or ambient effects is negligible and is thus assumed to be 0.

| Measurement | Test 1 | Test 2 | Test 3 | Test 4 |
|---|---|---|---|---|
| Delay Set | 0x0C | 0x07 | 0x07 | 0x07 |
| Test Duration | 9 h 9 m 10 s | 8 h 26 m 59 s | 8 h 42 m 39 s | 9 h 31 m 36 s |
| Number of Frames Transmitted | $1.318 \times 10^{12}$ | $1.217 \times 10^{12}$ | $1.254 \times 10^{12}$ | $1.372 \times 10^{12}$ |
| No. Frames w/ Correctable Errors | 0 | 0 | 0 | 0 |
| Number of Non-Correctable Errors | 0 | 0 | 0 | 0 |
| Bit Error Rate | $< 4.31 \times 10^{-15}$ | $< 4.67 \times 10^{-15}$ | $< 4.53 \times 10^{-15}$ | $< 4.14 \times 10^{-15}$ |

Table 5.3: Table summarizing test bench Stability Tests

## 5.4 Test bench SEU Susceptibility Results

Table 5.4 presents the test bench's susceptibility to SEUs using the FPGA-FPGA test setup as described in Section 4.6. Note the FPGA-FPGA setup generated data for all 14 E-Links unlike the previous stability tests were only 11 E-Links were used. Following the calculation presented in Section 4.9 the total fluence for the this susceptibility test is calculated to $1.1 \times 10^9$ neutrons per $cm^2$. No errors appeared for the irradiated FPGA and is identical to findings [21], [32] presented in Section 2.3.3. Following these results it is concluded that no SEUs will be induced in the test bench.

| Measurement | Test bench Susceptibility Test |
|---|---|
| Irradiated Time | 2 d 0 h 35 m 47 s |
| Delay Set | 0x08 |
| No. of Frames Transmitted | $6.998 \times 10^{12}$ |
| No. Frames w/ Correctable Errors | 0 |
| No. of Non-Correctable Errors | 0 |
| Bit Error Rate | $< 6.38 \times 10^{-16}$ |

Table 5.4: Table summarizing test bench susceptibility to SEU results

## 5.5 Main Experiment Results

The duration of the irradiation tests was chosen to be identical in order to simplify analysis of the BER and SEU cross-section rates. Test 4 was run first, since according to the hypothesis, is the most likely observe SEUs. By 36 hours there was significant results regarding the errors measured. Hence 36 hours was the chosen duration for the rest of the experiments and equates to $5.184 \times 10^{12}$ frames transmitted and a fluence of $835.37 \times 10^6$ neutrons per $cm^2$ calculated for each test. This duration is comparable to the DESY BER tests which run until BER of $10^{-15}$ is produced, which is three orders of magnitude above specification [43].

This result can be reproduced in 36 hours. Furthermore, this duration is comparable to the setups looked at in [27], [29], [30]. Finally, the SEU cross-section $\sigma_{SEU}$ was calculated with the Equation 2.13 given in Section 2.2. Note that the number of errors counted do not automatically equate to the number of bit flips observed. See the discussion for each test.

| Measurement | Test 1 | Test 2 | Test 3 | Test 4 Iteration 1 | Test 4 Iteration 2 |
|---|---|---|---|---|---|
| Delay Set | 0x0C | 0x07 | 0x07 | 0x07 | 0x07 |
| No. Frames w/ Alignment Errors | 0 | 0 | 0 | 65535 (Max) | 0 |
| No. Frames w/ Correctable Errors | 0 | 0 | 0 | 65535 (Max) | 68 |
| Number of Non-Correctable Errors | 0 | 3 | 0 | 36808 | 0 |
| Bit Error Rate | $< 1.10 \times 10^{-15}$ | $3.29 \times 10^{-15}$ | $< 1.10 \times 10^{-15}$ | $4.03 \times 10^{-11}$ | $< 1.10 \times 10^{-15}$ |
| $\sigma_{SEU}$ | $< 1.19 \times 10^{-9}$ | $3.59 \times 10^{-9}$ | $< 1.19 \times 10^{-9}$ | See discussion | $8.14 \times 10^{-8}$ |

Table 5.5: Main experiment test results showing substantial change in either the BER or $\sigma_{SEU}$ for test 4 as compared to the other tests. The following subsections provide detailed analysis of the results.

### 5.5.1 Test 4 Iteration 1

Zero correctable or non-correctable errors were observed until the time 24 h 54 m 45 s was reached. At this point a sudden spike of 434 CRC errors was observed. The errors settled for 1 m 28 s before maxing out the alignment errors. As previously discussed the alignment errors are counted when the header bits of the frame cannot be found. As the header bits are introduced during the interleaving phase may suggest an upset occurring within this stage. This behaviour of observing alignment errors and the quick recovery thereof was not observed in the other tests and previous dealings with the setup, without the radiation source.

Alongside the alignment errors the non-correctable errors was rapidly increased but stopped within 13 m 8s. Note that non-correctable errors are not considered during an alignment error. Given the large number of non-correctable errors, it suggested that the source of errors could be a result of a SEU causing one of the lpGBT sub-processes (Illustrated in Figure A.5) to fail. This includes the possibility of the clock recovery circuit losing lock. Recovery of these sub-processes are described in [7] (See Watchdog Section). Furthermore SEU testing with the watchdog process, described in [7], are identical to the behavioural findings of this test iteration.

A SEU upsetting a single bit in either the configuration registers or lpGBT sub-process could have indeterminate effect on the number of errors observed. It is for this reason cross-section for SEU calculated for this test iteration is not given as the number of bit-flips due to SEUs cannot be determined.

From this test, the BER produced is $4.03 \times 10^{-11}$. Considerations when calculating this BER include adding the number of errors that would have been counted due to misalignment. A maximum of 65535 misaligned frames with 11 active channels correspond to $11.5 \times 10^6$ bits in error to be added to the non-correctable errors. The BER calculated is an order of magnitude under specification, however it must be noted that one of the branches for TMR was turned off and EoS card is not expected to generate it's own data internally when installed in the ITk. The results however showed promise in relation to the experiment hypothesis.

### 5.5.2 Test 3

Test 3 replaces the interleaving process from the lpGBT and with a radiation immune counterpart on FPGA test bench. Results after running for the required 36 hours, showed no errors detected. This is inline with the experiment hypothesis as the number of radiation exposed stages had reduced. The lack of errors were found indicated that the presence of the interleaver in Test 4 increases the SEU error rate. Given there were no detected errors for Test 3, and in accordance with the hypothesis, no SEUs were expected for Tests 1 and 2. For this reason before completing Test 1 and 2, a second iteration of Test 4 was performed to then try replicate the initial results.

### 5.5.3 Test 4 Iteration 2

It was promising to see 68 correctable errors within 7h 45m 21s. The progression to 68 errors was inline with the expected behaviour of a sudden upset. With the jump from 0 to 11 errors occurring within 40s and the final jump from 11 to 68 errors in 5s. Although correctable errors do not effect the BER, they do give an indication of how many bit flips may have occurred. A conservative estimate is at least one bit flip occurred per frame resulting in a total of 68 bit flips. The upper bound of this estimate relies on the interleaver and encoder being able to correct up to 10 bits per frame resulting in a total of 680 bit flips. Therefore the number of bit flips for both iterations of test 4 are substantially higher than the rest the other tests. This strongly suggests that the interleaver is more susceptible to SEUs than the other stages.

### 5.5.4 Test 2

This test emulates the encoder and interleaver on the FPGA leaving only the scrambler activated on the lpGBT. Results show 3 non-correctable errors with no alignment or correctable errors for the entire 36 hour duration of the test. Having non-correctable errors alongside no correctable errors is significant as this means the upset occurred before the encoder emulated on the FPGA test bench. Therefore the data would have

been upset before reaching the encoder, and the parity bits appended would be applicable to the incorrect data. As such the decoder would not detect or correct any errors with respect to the erroneous data. The decoded message would then only be flagged when compared to the generated data as a non-correctable error. Since the scrambler is the only activated stage within the lpGBT at this stage it is assumed that the upset was introduced within this stage, given it was shown the FPGA test bench is not vulnerable to SEUs.

It is apparent the SEUs observed in this test should have also been seen in test 3 which also irradiated the scrambler stage. This experiment is limited in its ability to isolate each stage individually due to the design of the lpGBT. It is hoped that with further iterations of the tests an average number of non-correctable errors will be produced which includes errors induced in the scrambler. See Section 5.7.

### 5.5.5 Test 1

Zero correctable or non-correctable errors were observed during this test. This was expected as none of the DSP stages within the irradiated lpGBT were activated.

## 5.6 Non-Correctable Errors in Relation to E-Links

Results from this setup can be used to further characterize the SEU susceptibility of the data paths for the individual E-Links. Of the tests performed only Test 4 Iteration 1 produced non-correctable errors. These errors are presented in Figure 5.2, note the first 3 E-Links are excluded due to the aforementioned challenges. These preliminary results provide no clear distinction between E-Links. Although presented, these results cannot be used to definitively characterize the susceptibility of each E-Link.

## 5.7 Summary of Results

In order to quantitatively characterize the change each stage introduces to the BER, many more repetitions for each test needed to be performed. This was not possible within the time constraints of this experiment. However, the results of this experiment show:

1. A setup can be created which will produce SEUs. This is of notable value to the DESY team or anyone else who wishes to validate the resilience of the lpGBT on the EoS card under anticipated ITk operating environment

2. The resilience of the lpGBT to SEUs was demonstrated with the BER rate for 4 of the 5 tests being three orders of magnitude above specification despite having TMR disabled

3. Confirms the hypothesis, an increase in number of SEUs is shown with the introduction of more DSP stages

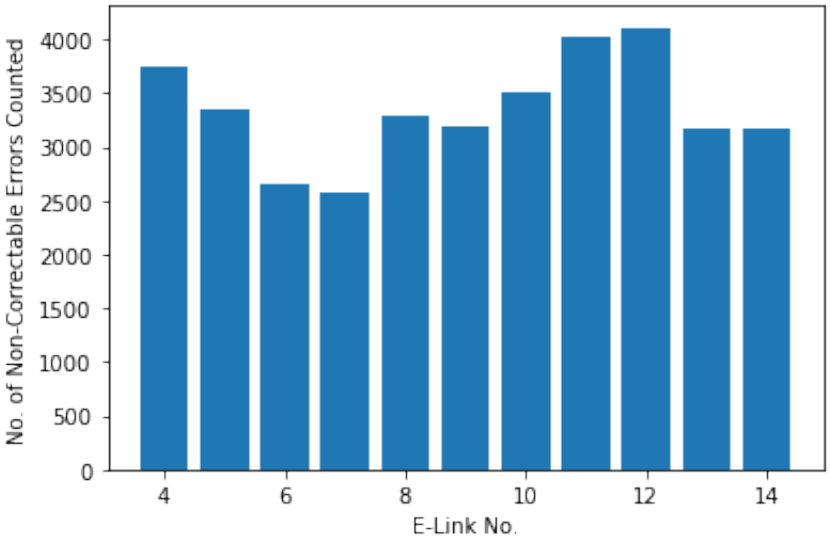



Figure 5.2: Number of non-correctable errors counted for each E-Link. No clear distinction between the E-Links can be inferred

4. Preliminary results indicate the interleaver is more susceptible to SEUs than the other stages

It is noted that ideally the stability tests should have also be run for a similar duration to the irradiation tests. However duration to observe SEUs was unknown until the first radiation results were obtained. Despite this Test 4 Iteration 2 and Test 2 produced errors within the bounds of the stability test motivating that the errors observed were indeed due to the presence of radiation.

Furthermore, ideally more iterations per test are required to decisively confirm the change in BER due to the introduction of stages. As evident by the two different iterations of Test 4. This includes more iterations of the stability tests. As discussed in Section 2.5.2 the challenges of running multiple tests is the total amount of time it requires as well as introducing the effects of TID to the BER (previously discussed in Section 2.3.2).

# Chapter 6

# Conclusion and Recommendations

## 6.1 Conclusion

This thesis provided a brief overview to the ATLAS Phase II upgrade, the strip detector system and describes the functionality of the EoS card to provide power, signal and control information to the 14 or 28 front-end modules as well as serialize and prepare the data it receives to be transported to the off-detector systems [2]. Furthermore, the EoS will operate in an increased radiation environment thus presenting the possibility of data corruption caused by SEUs.

One of the active components of the EoS card is the lpGBT ASIC. The lpGBT utilizes a number of techniques to mitigate against the effects of SEUs during transmission. Techniques discussed include Triple Modular Redundancy (TMR) and scrambling, Reed-Solomon encoding and interleaving DSP stages. This experiment set out to prove the hypothesis that the DSP stages within the lpGBT are susceptible to data corruption caused by SEUs. This is inline with previous studies [25], [27], [29] which investigated the devices similar to the lpGBT, and indicated that SEUs can be observed by irradiating ASIC devices with neutron energies similar to the source provided by the n-lab. In addition, the experiment setup created is able to indicate to some degree the susceptibility of the individual DSP stages.

Thus the experiment describes a test setup that was commissioned by the author at the Department of Physics, UCT to test this hypothesis. This setup is similar to the setup at DESY [10], [43] and setup described in [25]. The experiment consisted of 4 tests which iteratively activated the DSP stages on the irradiated lpGBT. It was expected that the BER rate would increase as more stages were introduced. This experiment not only tested the hypothesis but also provided a way to characterize the individual stages by comparing the BER rates of the 4 tests. Specifically, this thesis also outlined the extensions made to the DESY setup, software and firmware to enable these tests and therefore also contributes to DESY's ongoing work in validating the EoS card for operation.

Furthermore, an additional setup was created to test the susceptibility of the FPGA test bench itself. No errors were observed with this setup when irradiating a Kintex7 FPGA with an optical transceiver setup transmitting at a data rate of 10.25 Gbps. This was in accordance with the results discussed in [21], [32], [33] showing that similar FPGAs and an optical transceiver were not susceptible to SEUs. These results in addition to testing the stability of the 4 tests proved that errors caused by outside disturbances would not factor into the irradiation tests.

The results from the irradiation tests proved the hypothesis that the DSP stages within the lpGBT ASIC are susceptible to data corruption caused by SEUs. Tests 1 and 3 produced a BER of $< 1.10 \times 10^{-15}$ and $\sigma_{SEU}$ of $< 1.19 \times 10^{9}$. Test 2 observed 3 non-correctable errors thereby slightly increasing both the BER and SEU cross-section to $3.29 \times 10^{-15}$ and $3.59 \times 10^{-9}$ respectively. The first iteration of test 4 saw a large increase alignment errors and non-correctable errors thereby increasing the BER rate to $4.03 \times 10^{-11}$. This result indicates an SEU temporarily interrupted either a configuration register or a lpGBT sub-process (e.g. the clock recovery circuit losing clock). The second iteration of test 4 observed 68 correctable errors increasing $\sigma_{SEU}$ to at least $8.14 \times 10^{-8}$. Since these errors were correctable, the BER rate was identical to Test 1 and 2. These results are summarized Table 5.5.

The results of the 4 tests indicate that there is a large change in either BER and SEU cross-section when activating the interleaver on the irradiated lpGBT. More iterations of these 4 tests including iterations without the neutron source would be required to accurately quantify this change.

## 6.2 Recommendations for Future Work

**Multiple Iterations** Chapter 5 discussed the limitations of this experiment. It is recommended more iterations for each test be performed including the stability tests. The average of these results will provide a more accurate characterization of the DSP stages within the lpGBT.

**Downlink Stages Susceptibility** This experiment focused primarily on the characterizing the susceptibility of the uplink stages to SEUs. This test can easily be extended to characterizing the downlink stages. It is expected that like the uplink stages, the downlink DSP stages are susceptible to data corruption caused by SEUs. The following steps illustrate how a setup to test this can be achieved:

1. Generate and prepare data for the downlink with the FPGA control bench firmware. The control bench already has this functionality
2. Configuring the LDDataSource register (See Figure 6.1) to loop the optical link data back
3. Deactivating all the Uplink DSP stages and removing the reverse operation stages on the FPGA control bench. This eliminates uncertainty from additional activated stages within the lpGBT

4. Irradiate the lpGBT as described in this thesis
5. Compare the data received to the generated data to determine if the downlink stages are functioning optimally
6. Similarly to the method presented in this thesis, the individual downlink DSP stages can be iteratively (de)activated on the lpGBT and emulated on the test bench firmware using IP cores provided by the GBTx team enabling the characterization of individual stages

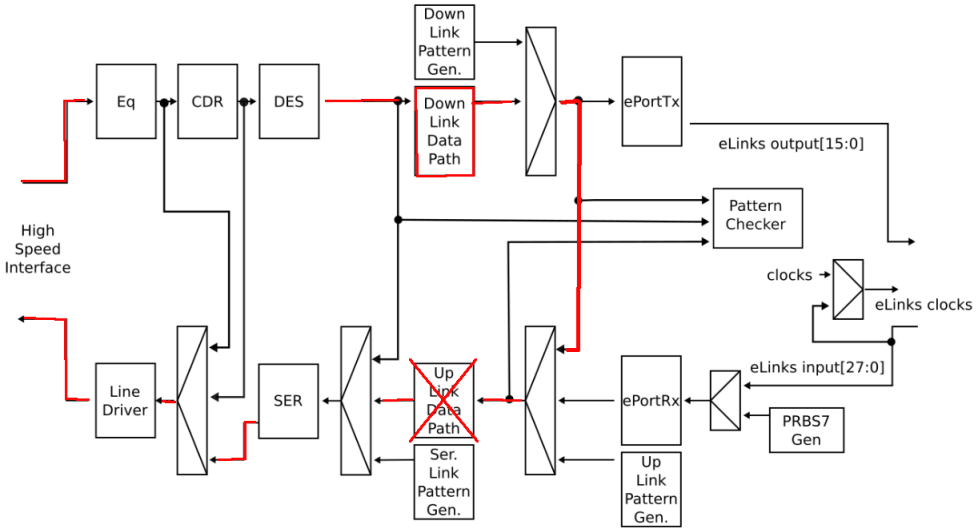



Figure 6.1: Data Path for proposed downlink testing highlighted in red. Downlink data is generated by the FPGA test bench processed by the lpGBT and transmitted back. The DSP stages within the downlink path can be emulated on the FPGA before reaching the lpGBT resulting in a test setup similar to the one outlined in this experiment.

**SEU Testing with TID and EMI** Literature has shown that SEU rate increases after TID exposure [18], [20], [31]. As a result, it is recommended this test be repeated with a lpGBT device that has been aged by TID. This has been previously done with a $^{60}Co$ source. Furthermore, as indicated by [21], injecting noise (EMI) in the power supply gives a higher expectation of observing SEUs.

**Testing with E-Link Connections** One of the limitations identified at the beginning of this experiment was the use of a constant pattern as opposed to a random data for data generation. Data that is more random provides a clearer view of the performance of the system as it is more indicative of the real world. Testing with E-Link connections allows for more random data to be generated and compared. As previously discussed testing with the E-Links was not included in this experiment to reduce uncertainty as to where SEUs may be introduced. Results from running an experiment with E-Links could then be compared to the results of this experiment to possibly also characterize the susceptibility of the E-Links.

**Quantifying the Clock and Phase Recovery Loop** As mentioned in Section 2.1, the optical link extracts the clock information from the downlink channel to synchronize with the off-detector systems. Incorrect clock recovery may lead to clock drift and incorrect reading of the data and as such characterizing the susceptibility of the clock recovery loop is relevant.

**Future versions of the lpGBT** This experiment was performed on the lpGBTv0. The lpGBTv1 is expected to be made available by the end of 2020. These new chips will be incorporated in the EoS post-production cards. Despite the change in register addresses, the method and code contributed in this thesis is compatible with the newer lpGBT version.

**Testing with the DCDC converter** Initial results indicated a noisy/unreliable power supply can effect the number of errors induced in the lpGBT. Performing the SEU test with the DCDC converter provides a setup that more closely resembles that of the EoS within the ITk.

**Different variant of the EoS** The EoS card can be populated with either one or two lpGBT devices. This experiment quantified the EoS card consisting of only one lpGBT. This test can be extended to quantify an EoS card with two lpGBT chips. The firmware already supports BER testing cards with two lpGBTs however extending this experiment to two lpGBTs will require modification of the second channel as outlined in Section 4.4.

# References


[1] W. Herr and B. Muratori, "Concept of luminosity," 2006. DOI: 10.5170/CERN-2006-002.361. [Online]. Available: https://cds.cern.ch/record/941318.

[2] A. Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System," CERN, Geneva, Tech. Rep. CERN-LHCC-2017-020. ATLAS-TDR-029, Sep. 2017. [Online]. Available: https://cds.cern.ch/record/2285584.

[3] C. Wanotayaroj, H. Ceslik, H. Colbow, S. Diez, P. Goettlicher, A. Melnik, M. Stanitzki, and J. Wolff, "The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment," in *Proceedings of Topical Workshop on Electronics for Particle Physics—PoS(TWEPP2018)*, vol. 343, 2019, p. 130. DOI: 10.22323/1.343.0130.

[4] S. A. Stucci, "ATLAS ITk Strip Detector for High-Luminosity LHC," in *Proceedings of The 39th International Conference on High Energy Physics—PoS(ICHEP2018)*, vol. 340, 2019, p. 083. DOI: 10.22323/1.340.0083.

[5] Y. Li, D. Li, W. Cui, and R. Zhang, "Research based on osi model," in *2011 IEEE 3rd International Conference on Communication Software and Networks*, 2011, pp. 554–557. DOI: 10.1109/ICCSN.2011.6014631.

[6] F. F. Mazda and E. V. Jones, *Telecommunications Engineer's Reference Book*. Elsevier Science, 2014, 28/1 to 29/1.

[7] lpGBT Design Team, *Lpgbt documentation*, English, Nov. 13, 2019, 337 pp., release.

[8] M. Mizuno, M. Yamashina, K. Furuta, H. Igura, H. Abiko, K. Okabe, A. Ono, and H. Yamada, "A ghz mos adaptive pipeline technique using mos current-mode logic," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 6, pp. 784–791, 1996. DOI: 10.1109/4.509864.

[9] W. A. Geisel, *Tutorial on reed-solomon error-correction coding*, Houston, TX, United States, 1996. [Online]. Available: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19900019023.pdf.

[10] A. Boebel, *Atlas eos pcb test firmware*, English, version 1.3, DESY Hamburg, Jul. 3, 2020, 31 pp.

[11] C. Riegel, M. Backhaus, J. Hoorne, T. Kugathasan, L. Musa, H. Pernegger, P. Riedler, D. Schaefer, W. Snoeys, and W. Wagner, "Radiation hardness and timing studies of a monolithic towerjazz pixel design for the new atlas inner tracker," *Journal of Instrumentation*, vol. 12, pp. C01015–C01015, Jan. 2017. DOI: 10.1088/1748-0221/12/01/C01015.

[12] M. Cecchetto, P. Fernández-Martínez, R. G. Alía, R. Ferraro, S. Danzeca, F. Wrobel, C. Cazzaniga, and C. D. Frost, "See flux and spectral hardness calibration of neutron spallation and mixed-field facilities," *IEEE Transactions on Nuclear Science*, vol. 66, no. 7, pp. 1532–1540, 2019.

[13] R. C. Lacoe, "Improving integrated circuit performance through the application of hardness by design methodology," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1903–1925, 2008.

[14] M. Huhtinen and F. Faccio, "Computational method to estimate single event upset rates in an accelerator environment," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 450, no. 1, pp. 155–172, 2000, ISSN: 0168-9002. DOI: https://doi.org/10.1016/S0168-9002(00)00155-8. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900200001558.

[15] H. Li, J. Deng, and D. Chang, "Monte carlo calculation of the cross-section of single event upset induced by 14mev neutrons," *Radiation Measurements*, vol. 39, no. 4, pp. 401–407, 2005, ISSN: 1350-4487. DOI: https://doi.org/10.1016/j.radmeas.2004.05.005. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1350448704001404.

[16] E. L. Petersen, J. C. Pickel, J. H. Adams, and E. C. Smith, "Rate prediction for single event effects-a critique," *IEEE Transactions on Nuclear Science*, vol. 39, no. 6, pp. 1577–1599, 1992.

[17] C. Chen and D. Y. Hu, "Analysis of affecting factors in neutron interactions with gate oxide in cmos transistors," in *2018 China Semiconductor Technology International Conference (CSTIC)*, 2018, pp. 1–3.

[18] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in mos oxides and devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 483–499, 2003. DOI: 10.1109/TNS.2003.812927.

[19] F. Soliman, A. Al-Kabbani, M. Rageh, and K. Sharshar, "Effects of electron-hole generation, transport and trapping in mosfets due to γ-ray exposure," *Applied Radiation and Isotopes*, vol. 46, no. 12, pp. 1337–1343, 1995. DOI: https://doi.org/10.1016/0969-8043(95)00211-U. [Online]. Available: http://www.sciencedirect.com/science/article/pii/096980439500211U.

[20] R. M. Chen, Z. J. Diggins, N. N. Mahatme, L. Wang, E. X. Zhang, Y. P. Chen, Y. N. Liu, B. Narasimham, A. F. Witulski, B. L. Bhuva, and D. M. Fleetwood, "Effects of total-ionizing-dose irradiation on seu- and set-induced soft errors in bulk 40-nm sequential circuits," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 471–476, 2017.

[21] J. Benfica, B. Green, B. C. Porcher, L. B. Poehls, F. Vargas, N. H. Medina, N. Added, V. A. P. de Aguiar, E. L. A. Macchione, F. Aguirre, M. A. G. Silveira, M. Perez, M. Sofo Haro, I. Sidelnik, J. Blostein, J. Lipovetzky, and E. A. Bezerra, "Analysis of sram-based fpga seu sensitivity to combined emi and tid-imprinted effects," *IEEE Transactions on Nuclear Science*, vol. 63, no. 2, pp. 1294–1300, 2016. DOI: 10.1109/TNS.2016.2523458.

[22] S. Biereigel, S. Kulis, R. Francisco, P. V. Leitao, P. Leroux, P. Moreira, and J. Prinzie, "The lpGBT PLL and CDR Architecture, Performance and SEE Robustness," in *Proceedings of Topical Workshop on Electronics for Particle Physics—PoS(TWEPP2019)*, vol. 370, 2020, p. 034. DOI: 10.22323/1.370.0034.

[23] "Test method for real-time soft error rate," JEDEC Solid State Technology Association, 2500 Wilson Boulevard Arlington, VA, Tech. Rep., Oct. 2007.

[24] *Standard guide for the measurement of single event phenomena (SEP) induced by heavy ion irradiation of semiconductor devices*. West Conshohocken, PA: ASTM, 2006, Reapproved 2006. [Online]. Available: https://cds.cern.ch/record/1373436.

[25] J. M. Bird, M. K. Peters, T. Z. Fullem, M. J. Tostanoski, T. F. Deaton, K. Hartojo, and R. E. Strayer, "Neutron induced single event upset (seu) testing of commercial memory devices with embedded error correction codes (ecc)," in *2017 IEEE Radiation Effects Data Workshop (REDW)*, 2017, pp. 1–8.

[26] N. Badodekar, *Mitigating single-event upsets using cypress's 65-nm asynchronous sram*, https://www.cypress.com/file/141291/download, Application Notes, 2016.

[27] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera, "A low-power and area-efficient radiation-hard redundant flip-flop, dice acff, in a 65 nm thin-box fd-soi," *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1881–1888, 2014. DOI: 10.1109/TNS.2014.2318326.

[28] S. Kulis, "Single Event Effects mitigation with TMRG tool," *JINST*, vol. 12, no. 01, C01082. 7 p, 2017. DOI: 10.1088/1748-0221/12/01/C01082. [Online]. Available: https://cds.cern.ch/record/2275130.

[29] E. Normand, J. L. Wert, W. R. Doherty, D. L. Oberg, P. R. Measel, and T. L. Criswell, "Use of pube source to simulate neutron-induced single event upsets in static rams," *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1523–1528, 1988. DOI: 10.1109/23.25491.

[30] J. Baggio, D. Lambert, V. Ferlet-Cavrois, P. Paillet, C. Marcandella, and O. Duhamel, "Single event upsets induced by 1–10 mev neutrons in static-rams using mono-energetic neutron sources," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2149–2155, 2007. DOI: 10.1109/TNS.2007.910039.

[31] E. C. F. Pereira, O. L. Gonçalez, R. G. Vaz, C. A. Federico, T. H. Both, and G. I. Wirth, "The effects of total ionizing dose on the neutron seu cross section of a 130 nm 4 mb sram memory," in *2014 15th Latin American Test Workshop - LATW*, 2014, pp. 1–4. DOI: 10.1109/LATW.2014.6841919.

[32] M. Ohlsson, P. Dyreklev, K. Johansson, and P. Alfke, "Neutron single event upsets in sram-based fpgas," in *1998 IEEE Radiation Effects Data Workshop. NSREC 98. Workshop Record. Held in conjunction with IEEE Nuclear and Space Radiation Effects Conference (Cat. No.98TH8385)*, 1998, pp. 177–180. DOI: 10.1109/REDW.1998.731500.

[33] R. T. Logan, S. Zargari, E. Chua, A. Chua, R. Wyss, J. J. Schaefer, I. A. Troxel, and M. Gruber, "Radiation test results for glenair 5 gbps and 40 gbps (4x10 gbps) optical transceivers," in *2019 IEEE Radiation Effects Data Workshop*, 2019, pp. 1–8. DOI: 10.1109/REDW.2019.8906588.

[34] J. R. Letaw and E. Normand, "Guidelines for predicting single-event upsets in neutron environments (ram devices)," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1500–1506, 1991. DOI: 10.1109/23.124138.

[35] E. Normand, "Extensions of the burst generation rate method for wider application to proton/neutron-induced single event effects," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2904–2914, 1998. DOI: 10.1109/23.736546.

[36] F. R. Palomo, J. M. Mogollon, J. Napoles, and M. A. Aguirre, "Mixed-mode simulation of bit-flip with pulsed laser," *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 1884–1891, 2010. DOI: 10.1109/TNS.2010.2050603.

[37] R. A. Weller, M. H. Mendenhall, R. A. Reed, R. D. Schrimpf, K. M. Warren, B. D. Sierawski, and L. W. Massengill, "Monte carlo simulation of single event effects," *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 1726–1746, 2010.

[38] F. Márquez, F. Muñoz, F. R. Palomo, L. Sanz, E. López-Morillo, M. A. Aguirre, and A. Jiménez, "Automatic single event effects sensitivity analysis of a 13-bit successive approximation adc," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1609–1616, 2015. DOI: 10.1109/TNS.2015.2456831.

[39] G. Santin, V. Ivanchenko, H. Evans, P. Nieminen, and E. Daly, "Gras: A general-purpose 3-d modular simulation tool for space environment effects analysis," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2294–2299, 2005. DOI: 10.1109/TNS.2005.860749.

[40] C. Inguimbert and S. Duzellier, "Seu rate calculation with geant4 (comparison with creme 86)," *IEEE Transactions on Nuclear Science*, vol. 51, no. 5, pp. 2805–2810, 2004. DOI: 10.1109/TNS.2004.836524.

[41] S. Kulis, "Single event effects mitigation with tmrg tool," *Journal of Instrumentation*, vol. 12, no. 01, p. C01082, 2017. [Online]. Available: http://stacks.iop.org/1748-0221/12/i=01/a=C01082.

[42] S. Biereigel, *Yoseeg*, https://gitlab.cern.ch/tmrg/yoseeg, 2020.

[43] H. Ceslik, *Eos qc/qa design validation tests*, Presentation at EoS ITk FDR Meeting, 16 March, 2020.

[44] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2874–2878, 1996. DOI: 10.1109/23.556880.

[45] Xilinx, *Kc705 evaluation board for the kintex-7 fpga user guide*, English, Xilinx, Feb. 4, 2019, 98 pp. [Online]. Available: https://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf, release.

[46] Xilinx, *Logicore clocking wizard product guide*, 2012. [Online]. Available: https://www.xilinx.com/support/documentation/ip_documentation/clk_wiz/v4_2/pg065-clk-wiz.pdf.

[47] Xilinx, *Xilinx 7 series fpga libraries guide for hdl designs*, 2011. [Online]. Available: https://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/7series_hdl.pdf.

[48] P. Moreira, *The lpgbt: A radiation tolerant asic for data, timing, trigger and control applications in hl-lhc*, 2019. [Online]. Available: https://espace.cern.ch/GBT-Project/LpGBT/Presentations/lpGBT20190903.pdf.

[49] X. D. Suite, *7 series fpgas transceivers wizard v3.5*, 2015. [Online]. Available: https://www.xilinx.com/support/documentation/ip_documentation/gtwizard/v3_5/pg168-gtwizard.pdf.

[50] UCT, *Phy3004w laboratory: Neutron radiation from ambe*, Unpublished, 2016.

# Appendix A

# Appendix

## A.1 lpGBT Uplink Frame Structure

### A.1.1 Before Interleaving

| Frame | Function | I/O Group |
|---|---|---|
| FRMUP[9:0] | FEC[9:0] | |
| FRMUP[19:10] | FEC[19:10] | |
| FRMUP[35:20] | Data[15:0] | 0 |
| FRMUP[51:36] | Data[31:16] | 0 |
| FRMUP[67:52] | Data[47:32] | 1 |
| FRMUP[83:68] | Data[63:48] | 1 |
| FRMUP[99:84] | Data[79:64] | 2 |
| FRMUP[115:100] | Data[95:80] | 2 |
| FRMUP[131:116] | Data[111:96] | 3 |
| FRMUP[147:132] | Data[127:112] | 3 |
| FRMUP[163:148] | Data[143:128] | 4 |
| FRMUP[179:164] | Data[159:144] | 4 |
| FRMUP[195:180] | Data[175:160] | 5 |
| FRMUP[211:196] | Data[191:176] | 5 |
| FRMUP[227:212] | Data[207:192] | 6 |
| FRMUP[243:228] | Data[223:208] | 6 |
| FRMUP[249:244] | {4'b0, DownIC[1:0]} | See text |
| FRMUP[251:250] | EC[1:0] | |
| FRMUP[253:252] | IC[1:0] | |
| FRMUP[255:254] | H[1:0] | HFH[1:0] = 2'b10 |

Figure A.1: Uplink Frame Structure Before Interleaving [7]

### A.1.2 After Interleaving

| 10G24 FEC5 Frame Interleaving | | |
|---|---|---|
| Interleaved Frame | Assignment | Code group |
| IFRMUP[4:0] | FEC[4:0] | 0 |
| IFRMUP[9:5] | FEC[14:10] | 1 |
| IFRMUP[14:10] | FEC[9:5] | 0 |
| IFRMUP[19:15] | FEC[19:15] | 1 |
| IFRMUP[24:20] | FRMUP[24:20] | 0 |
| IFRMUP[29:25] | FRMUP[141:137] | 1 |
| IFRMUP[34:30] | FRMUP[29:25] | 0 |
| IFRMUP[39:35] | FRMUP[146:142] | 1 |
| IFRMUP[44:40] | FRMUP[34:30] | 0 |
| IFRMUP[49:45] | FRMUP[151:147] | 1 |
| IFRMUP[54:50] | FRMUP[39:35] | 0 |
| IFRMUP[59:55] | FRMUP[156:152] | 1 |
| IFRMUP[64:60] | FRMUP[44:40] | 0 |
| IFRMUP[69:65] | FRMUP[161:157] | 1 |
| IFRMUP[74:70] | FRMUP[49:45] | 0 |
| IFRMUP[79:75] | FRMUP[166:162] | 1 |
| IFRMUP[84:80] | FRMUP[54:50] | 0 |
| IFRMUP[89:85] | FRMUP[171:167] | 1 |
| IFRMUP[94:90] | FRMUP[59:55] | 0 |
| IFRMUP[99:95] | FRMUP[176:172] | 1 |
| IFRMUP[104:100] | FRMUP[64:60] | 0 |
| IFRMUP[109:105] | FRMUP[181:177] | 1 |
| IFRMUP[114:110] | FRMUP[69:65] | 0 |
| IFRMUP[119:115] | FRMUP[186:182] | 1 |
| IFRMUP[124:120] | FRMUP[74:70] | 0 |
| IFRMUP[129:125] | FRMUP[191:187] | 1 |
| IFRMUP[134:130] | FRMUP[79:75] | 0 |
| IFRMUP[139:135] | FRMUP[196:192] | 1 |
| IFRMUP[144:140] | FRMUP[84:80] | 0 |
| IFRMUP[149:145] | FRMUP[201:197] | 1 |
| IFRMUP[154:150] | FRMUP[89:85] | 0 |
| IFRMUP[159:155] | FRMUP[206:202] | 1 |
| IFRMUP[164:160] | FRMUP[94:90] | 0 |
| IFRMUP[169:165] | FRMUP[211:207] | 1 |
| IFRMUP[174:170] | FRMUP[99:95] | 0 |
| IFRMUP[179:175] | FRMUP[216:212] | 1 |
| IFRMUP[184:180] | FRMUP[104:100] | 0 |
| IFRMUP[189:185] | FRMUP[221:217] | 1 |
| IFRMUP[194:190] | FRMUP[109:105] | 0 |
| IFRMUP[199:195] | FRMUP[226:222] | 1 |
| IFRMUP[204:200] | FRMUP[114:110] | 0 |
| IFRMUP[209:205] | FRMUP[231:227] | 1 |
| IFRMUP[214:210] | FRMUP[119:115] | 0 |
| IFRMUP[219:215] | FRMUP[236:232] | 1 |
| IFRMUP[224:220] | FRMUP[124:120] | 0 |
| IFRMUP[229:225] | FRMUP[241:237] | 1 |
| IFRMUP[234:230] | FRMUP[129:125] | 0 |
| IFRMUP[239:235] | FRMUP[246:242] | 1 |
| IFRMUP[244:240] | FRMUP[134:130] | 0 |
| IFRMUP[249:245] | FRMUP[251:247] | 1 |
| IFRMUP[253:250] | {FRMUP[253:252], FRMUP[136:135]} | 0 |
| IFRMUP[255:254] | H[1:0] = 2'b10 | HEADER |

Figure A.2: Uplink Interleaver Frame Structure [7]

## A.2 lpGBT Downlink Frame Structure

### A.2.1 Before Interleaving

| Frame | Function | I/O Group |
|---|---|---|
| FRMDWN[23:0] | FEC[23:0] | |
| FRMDWN[31:24] | Data[7:0] | 0 |
| FRMDWN[39:32] | Data[15:8] | 1 |
| FRMDWN[47:40] | Data[23:16] | 2 |
| FRMDWN[55:48] | Data[31:24] | 3 |
| FRMDWN[56] | EC[0] | EC |
| FRMDWN[57] | H[0] | |
| FRMDWN[58] | EC[1] | EC |
| FRMDWN[59] | H[1] | |
| FRMDWN[60] | IC[0] | |
| FRMDWN[61] | H[2] | |
| FRMDWN[62] | IC[1] | |
| FRMDWN[63] | H[3] | H[3:0] = 4'b1001 |

Figure A.3: Downlink Frame Structure Before Interleaving [7]

### A.2.2 After Interleaving

| Interleaved Frame | | |
|---|---|---|
| **Interleaved Frame** | **Assignment** | **Code group** |
| IFRMDWN[2:0] | FEC[2:0] | 0 |
| IFRMDWN[5:3] | FEC[8:6] | 1 |
| IFRMDWN[8:6] | FEC[14:12] | 2 |
| IFRMDWN[11:9] | FEC[20:18] | 3 |
| IFRMDWN[14:12] | FEC[5:3] | 0 |
| IFRMDWN[17:15] | FEC[11:9] | 1 |
| IFRMDWN[20:18] | FEC[17:15] | 2 |
| IFRMDWN[23:21] | FEC[23:21] | 3 |
| IFRMDWN[26:24] | Data[2:0] | 0 |
| IFRMDWN[29:27] | Data[14:12] | 1 |
| IFRMDWN[32:30] | Data[26:24] | 2 |
| IFRMDWN[35:33] | Data[11:9] | 3 |
| IFRMDWN[38:36] | Data[5:3] | 0 |
| IFRMDWN[41:39] | Data[17:15] | 1 |
| IFRMDWN[44:42] | Data[29:27] | 2 |
| IFRMDWN[47:45] | Data[23:21] | 3 |
| IFRMDWN[50:48] | Data[8:6] | 0 |
| IFRMDWN[53:51] | Data[20:18] | 1 |
| IFRMDWN[56:54] | {EC[0], Data[31:30]} | 2 |
| IFRMDWN[59:57] | {H[1], EC[1], H[0]} | HEADER, 3 |
| IFRMDWN[63:60] | {H[3], IC[1], H[2], IC[0]} | HEADER, 3 |

Figure A.4: Downlink Frame Structure Before Interleaving [7]

## A.3 lpGBT Power-On Finite State Machine

See attached the Finite State Machine Procedure discussed in Section 2.5.4.

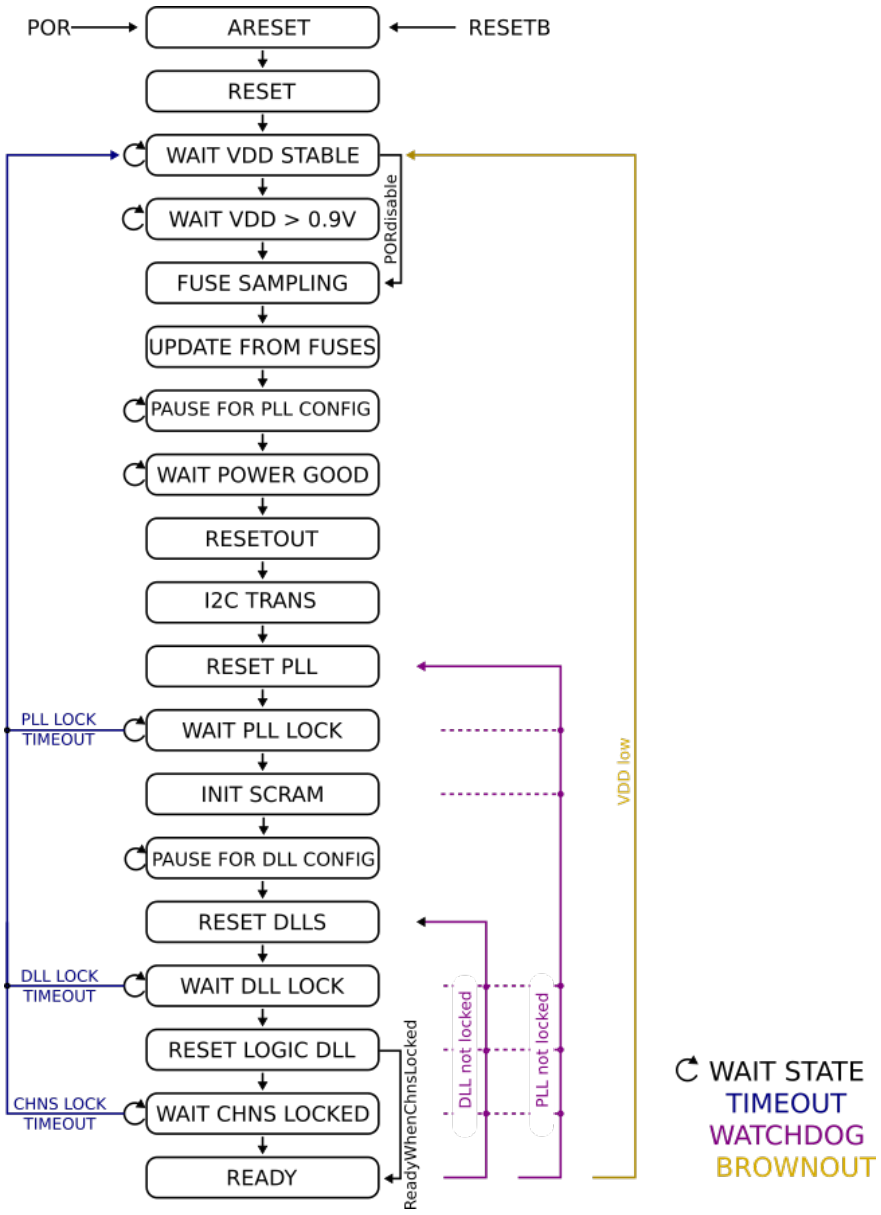



Figure A.5: lpGBT FSM Procedure [7]

## A.4 Design Flow of TMRG Tool

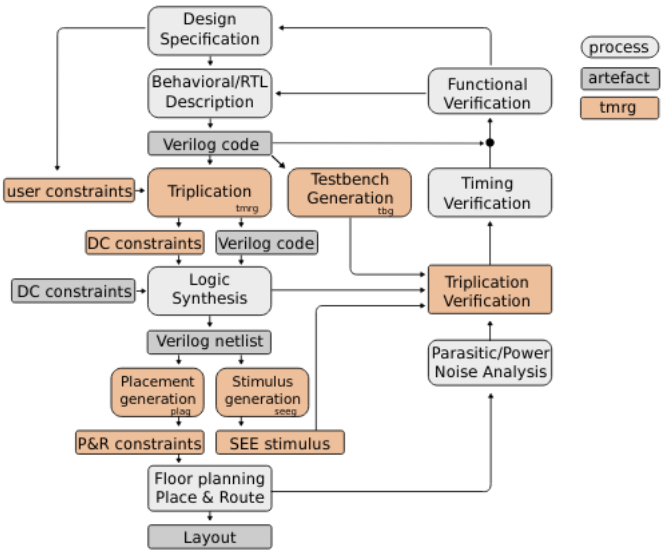



Figure A.6: Design Flow for the TMRG tool set incl. SEEG [41]. Diagram shows after original Verilog code has been created the triplication tool will produce synthesizable Verilog module. Furthermore the tool can generate a testbench which simulates SEEs to test the produced module.

## A.5 High Speed Link Donwlink Overview

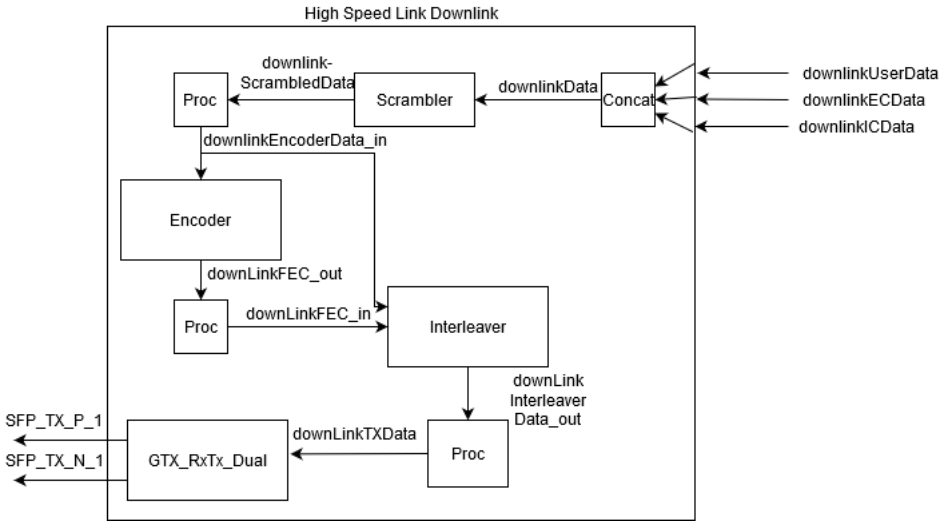



Figure A.7: Detailed Architecture of the Downlink High Speed Link Data Flow

## A.6 Descriptions of LabView Front Panel continued

| Label | Name | Description |
|---|---|---|
| 3 | Stop Sequences Button | Stops execution of the sequence file |
| 4 | Exit Button | Ends the LabView programme |
| 6 | Sequence State Indicator | Displays the current state of the sequence |
| 8 | Device Panel Tabs | Devices have different device panels which offer finer grained control and status information over their configuration settings. Particular interest is given the the FPGA panel which is currently displayed |
| 15 | Pattern Match Indicator | Hexadecimal number which indicate the number of bits per E-Link received which are correct. $F_{16}$ represents if all 16 bits from one E-Link is correct |
| 17 | Toggle LpGBT I2C/IC Button | Choose lpGBT configuration via I2C or through the optical link. See Section 3.5 |
| 18 | FPGA expert panel | Graphical configuration of the BER test such as sync pattern and delay for the BER test |

Table A.1: Description the LabView Front Panel Interface continued

## A.7 LabView Additional Contributions

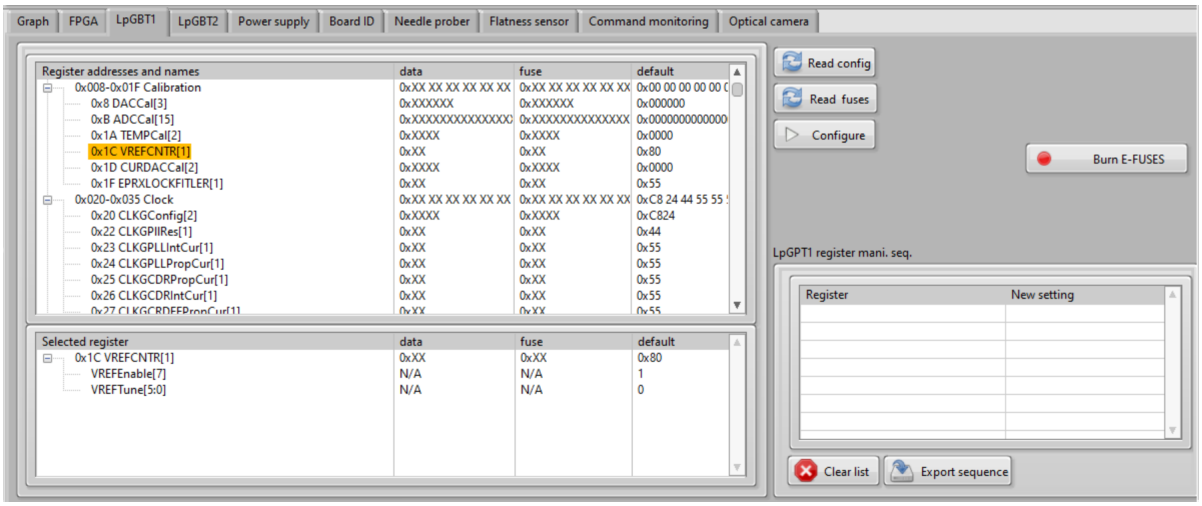



Figure A.8: Screenshot of Register GUI for which additional contributions were made. Register can be selected in the top half panel and the bit values of the register can be modified in the bottom panel

## A.8 Initial lpGBT Configuration Sequence File

Listing A.1: Sequence File for Initial lpGBT Configuration

```
DefineSequence BitErrorTest_single_LpGPT
#Loop #volt=0.2,1.2,0.2 Sequence DummyTest lpGBT=#volt
#PowerOn 1 2 3 4
#Photo
#IRpicture
#Loop ##MUX=0xf,0xff,0x10 Sequence Read_ADC_LpGPT1 #MUX=##MUX
ReadLpGBTid
Sequence Configure_LpGPT1
Sequence Read_ADC_LpGPT1 #MUX=DF
Sequence Read_ADC_LpGPT1 #MUX=EF
PowerOff 1 2 3 4

DefineSequence FuseTest
BurnFuses 12345678

DefineSequence WienerTest
PowerOn 1 101
Wait 30
PowerOff 1 101

DefineSequence DummyTest lpGBT=1
PowerOn lpGBT
PowerOff

DefineSequence Configure_LpGPT1
I2Cwrite E2 0000
#
# basic settings 1c 1e 20 22 24 26 28 2a 2c 2e 30 32 34 36 38 3a 3c 3e
I2Cwrite E2 1c00 8000 0055 C824 4455 5555 5555 0F00 0000 4429 990A 0A0A 0A55 5100 0000
    0020 0000 0000 00
#
# I2C master 3f 40 42 44 46 48 4a 4c 4e 50
#I2Cwrite E2 3F00 00 0000 0000 0000 0000 0000 0000 0000 0000 0000
```

```
#
#parallel port 52 54 56 58 5a
I2Cwrite E2 5200 0180 0180 0000 0000 0101
#
# phase shifter 5c 5f 62 65
I2Cwrite E2 5c00 1C0000 1C0000 1C0000 1C0000
#
# DAC 68 6a
#I2Cwrite E2 6800 0000 0000
#
# ePort clk 6c 6e 70 72 74 76 78 7a 7c 7e 80 82 84 86 88 8a 8c 8e 90 92 94 96 98 9a 9c 9e
     a0 a2 a4
I2Cwrite E2 6c00 1C00 1C00 1C00 1C00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
    0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 1900
#
# ePort Tx a7 a9 ab ac ae b0 b2 b4 b6 b8 ba bc be c0 c2
I2Cwrite E2 a700 AA10 FFFF 03 0303 0303 0303 0303 0303 0303 0303 0300 0000 0000 0000 0000
# ePort Rx, powerup c4 c6 c8 ca cc ce d0 d2 d4 d6 d8 da dc de e0 e2 e4 e6 e8 ea ec ee
I2Cwrite E2 C400 FAFA FAFA FAFA FA02 0200 0200 0200 0200 0200 0200 0200 0200 0200 0200
    0200 0200 0200 0200 0300 0000 0000 0006
# basic settings
I2Cwrite E2 1c00
I2Cverify E2 8000 0055 C824 4455 5555 5555 0F00 0000 4429 990A 0A0A 0A55 5100 0000 0020
    0000 0000 00
# I2C master
#I2Cwrite E2 3F00
#I2Cverify E2 0000 0000 0000 0000 0000 0000 0000 0000 0000 00
# parallel port
I2Cwrite E2 5200
I2Cverify E2 01 8001 8000 0000 0001 01
# phase shifter
I2Cwrite E2 5c00
I2Cverify E2 1C0000 1C0000 1C0000 1C0000
# DAC
#I2Cwrite E2 6800
#I2Cverify E2 00 00 00 00
```

```
# eport clk
I2Cwrite E2 6c00
I2Cverify E2 1C 001C 001C 001C 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
    0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0019 00
# Eport Tx
I2Cwrite E2 a700
I2Cverify E2 AA10 FFFF 0303 0303 0303 0303 0303 0303 0303 0303 0000 0000 0000 0000 00
# eport rx, power-up
I2Cwrite E2 C400
I2Cverify E2 FA FAFA FAFA FAFA 0202 0002 0002 0002 0002 0002 0002 0002 0002 0002 0002
    0002 0002 0002 0003 0000 0000 0000 06

DefineSequence Read_ADC_LpGPT1 #MUX=0
I2Cwrite E2 1101 #MUX 20 04
I2Cwrite E2 1301 84
I2Cwrite E2 b801
I2Cread E2 01

DefineSequence Read_IOREG
I2Cwrite E2 5600 ffff 0000
I2Cwrite E2 9f01
I2Cread E2 01
I2Cwrite E2 5800 ffff
I2Cwrite E2 9f01
I2Cread E2 01
I2Cwrite E2 5600 0000 0000
I2Cwrite E2 9f01
I2Cread E2 01
```

## A.9 Sequence File for lpGBT Configuration for this Experiment

Listing A.2: Sequence File for experiment specific configuration

```
DefineSequence BitErrorTest_single_LpGPT
ReadLpGBTid
Sequence Joash_DP_DataReg
```

```
PowerOff 1 2 3 4


DefineSequence Joash_DP_DataReg
I2Cwrite E2 31 01 AC # TMR
I2Cwrite E2 32 01 00 # Set lpGBT Data path
I2Cwrite E2 1E 01 55 0F 55 0F # Set constant pattern
I2Cwrite E2 19 01 24 24 24 04 # Turn on all uplink groups within lpGBT
```

## A.10 Sequence File to test BER Configuration

Listing A.3: Configuration File for default LabView parameters

```
DefineSequence BitErrorTest_single_LpGPT
StartBerrTest_no_ELink
Wait 5
StopBerrTest
GetPattern 0
GetPattern 1
GetPattern 2
GetPattern 3
GetPattern 4
GetPattern 5
GetPattern 6
GetPattern 7
GetPattern 8
GetPattern 9
GetPattern A
GetPattern B
GetPattern C
GetPattern D
PowerOff 1 2 3 4
```

## A.11 Sequence File to test BER Configuration

Listing A.4: Configuration File for default LabView Parameters

```
[database]
basePath = "/C/Users/ATLASremote/Documents/LabVIEW Data/testbench"

[devices]
haveFlatnessSensor = FALSE
GPIOforITalkI2Cpin = 15
LpGBTregisterDescriptionPath = "/C/Users/ATLASremote/Documents/Joash/teststand_labview/
    lpgbt-register.txt"
haveRFIDreader = TRUE
busMasterForSecondaryLpGBT = 2
haveWienerCrate = FALSE
secondaryLpGBTaddress = 224
useSecondI2CbusForLpGBT = FALSE
primaryLpGBTtalkI2C = FALSE

[sequence]
loadDefaultSequence = FALSE
defaultPath = "/C/Users/joash/Documents/LabVIEW Data/testbench"
```