Production and Characterisation of Nanoparticulate Silicon Photovoltaic Devices

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Declaration

I know the meaning of plagiarism and declare that all of the work in the document, save for that which is properly acknowledged, is my own.

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Abstract

A first approach in fabricating electronically functional nanoparticulate silicon solar cells, by using low cost screen printing on paper substrates, has been developed. The semiconductor materials used consisted of n- and p-type silicon nanoparticles produced by means of high energy mechanical milling, as well as commercially sourced nanophase intrinsic silicon powder.

Results from microscopy revealed that the nanoparticles had formed clusters that were capable of transporting charge through the device. Results from the electrical characterisation show that the printed devices exhibit electrical properties characteristic of silicon PV devices, confirming that the experimental process followed resulted in the successful production of a functional silicon solar cell.

This thesis outlines the particle production process, ink formulation technique, and the device fabrication process. Results from the physical characterisation of the nanopowders and printed layers using optical and scanning electron microscopy, as well as an analysis of the electrical performance of the printed devices are also presented.

Contents

1. Introduction

The pursuit of efficient, affordable and environmentally friendly sources of energy remains at the forefront of scientific research today. With soaring oil prices, global warming, and oil reserves approaching peak production limits, fossil fuels are increasingly becoming an unpopular choice for global energy supply. Current estimates suggest that proven oil and gas reserves will begin to decline from around 2030 [1]. Various alternatives have been put forward either as a replacement for or an alternative to conventional fossil fuels.

Research into solar, geothermal, hydrogen fuel cells, biofuels and other solar dependent sources of energy has made tremendous gains over the past few years, yielding encouraging results [1]. In many western countries, renewable energy sources are being integrated into the main electricity supply in order to augment the conventional national grid. In this regard, whole neighbourhoods have been built, in the Netherlands for example, that rely only on solar energy for their domestic energy supply [1]. In the developing world, however, photovoltaics do not play a major role in meeting energy demands. One of the major reasons is the cost of implementation of solar panels for large scale energy supply. In spite of this, there has been successful implementation of solar powered homes and devices in countries like China, India, Indonesia, Kenya, Mexico and Zimbabwe [2]. Implementation of these pilot projects on a wider scale remains a challenge. The obstacles to the development and widescale utilisation of renewable energy sources, including photovoltaics, lie mainly with the cost of implementation and the efficiency of energy conversion [1]. Current estimates put the potential power available from solar radiation to be about 10,000 times more than the rate of fossil and nuclear fuels consumption in 2002 [1]. Although photovoltaic systems may not be able to replace fossil fuels for large energy installations at present, it can prove to be a viable alternative for small scale energy needs.

Research is also being carried out on producing non-conventional photovoltaics. In large scale conventional photovoltaic systems, crystalline silicon has been the dominant material used, and the cost of production is relatively high [3]. Progress has been made in research involving thin film photovoltaics using amorphous silicon and compound semiconductors like copper indium diselenide ($CuInSe_2$) [4]. Organic semiconductors have also been used in the fabrication of solar cells with encouraging results [5]. Photoelectrochemical cells [6] and other innovative designs like multi junction (or tandem) solar cells have opened up the field of research leading to the development of photovoltaics based on nanotechnology [6, 7].

The aim of this work is to produce a fully functional photovoltaic device, using nanoparticulate

silicon inks, at low cost by screen printing on paper substrates. In order for this to be achieved, the silicon material has to be prepared in the form of a nanopowder, which could then be mixed with other reagents to produce a printable ink. The next chapter discusses the theoretical background of photovoltaics, discussing the various materials and methods used in producing different types of solar cells. Chapter 3 discusses the means by which silicon nanoparticles can be produced, as well as the experimental milling procedure employed to produce the silicon nanoparticles used in fabricating the PV devices in this thesis. Micrographs of the milled particles are also presented. Chapter 4 describes the process of ink making and the printing procedure used in depositing the different layers used in the PV device fabrication process. The results obtained from the physical characterization of the printed layers using optical and scanning electron microscopy are also presented in chapter 4. Chapter 5 presents the results obtained from the electrical characterisation of the PV devices. This is followed by a discussion of these results in chapter 6. Chapter 7 summarizes the work done with suggestions for further work and improvements on the devices produced.

2. Photovoltaic Energy Conversion

The term photovoltaic is a combination of two words: **photo** which is Greek for light, and **volt** the unit of electric potential named after Alessandro Volta. In essence, the word **photovoltaic** implies the direct conversion of light into electricity. Edmund Becquerel first reported the discovery of the photovoltaic effect in 1839 [1, 8], when he observed that silver coated electrodes immersed in an electrolyte produced a current when exposed to light. William G. Adams and Richard E. Day first reported the generation of a photocurrent in a solid state device, when they observed the spontaneous generation of a photocurrent in a selenium sample, placed between heated platinum contacts, on exposure to light in 1876 [1, 8]. In 1883, Charles E. Fritts constructed what is regarded by many as the first solar cell, using a thin wafer of selenium, pressed between a thin grid of gold wires and a protective glass sheet [1, 8]. The efficiency of this device, however, was less than 1%. Selenium cells, therefore, were not used as power supply devices but mainly as photographic light meters due to their photoconductivity [1, 8].

In 1954, Chapin, Fuller and Pearson produced the first reported silicon photovoltaic device that had an efficiency of 6% [9]. However, the technology was not actively pursued at that time, due to the availability of a cheaper alternative in fossil fuels. Most photovoltaic research was directed towards producing solar panels for extra terrestrial missions, for which the cost of production was not a consideration. The global energy crisis of the 1970s led to a renewed interest in photovoltaics and other sources of alternative energy. This has led to the development of solar cells with efficiencies as high as 24%, and modules with efficiencies in the order of 17% with expectations of even higher efficiency [1, 10].

2.1 Principles of Photovoltaics

The photovoltaic (PV) effect is an equivalent process to the photoelectric effect, in which light is able to provide sufficient energy for electrons to escape from the surface of a metal, as explained by Einstein in 1905 [8]. When light shines on the surface of a material, photons having energy $E = hf$ (where h is Planck's constant and f the frequency of the incident light), can cause electrons to be emitted from the surface of the material if their energy is greater than the *work function* of the material. The work function Φ_w, is defined as the minimum energy required to remove an electron from the surface of a material [11]. Thus, it is the *frequency* of the incident light that determines if electrons will be excited from the surface of the material and not the

intensity of the incident light. These excited electrons cause a *photocurrent* to be generated which can be collected by means of a metal contact.

In a solid state PV device, absorption of photons of energy E greater than the energy band gap E_g of the material, causes the generation of electron-hole pairs within the semiconductor material. These charge carriers are then caused to move freely by means of a mechanism built into the PV device that allows for charge separation before the charge carriers can recombine. The charge carriers can then be collected by an external load. Charge separation can be achieved by means of two dissimilar semiconductors brought into electrical contact with each other, which creates an internal electric field allowing the charges to flow to the external load [12].

2.2 Semiconductors

Before discussing photovoltaics in detail, it is necessary to have an understanding of the materials that are used in most solid state PV devices: semiconductors. A semiconductor can be loosely defined as a material whose electrical characteristics lie between those of a conductor and an insulator. A conductor is a material that offers very little resistance to the flow of current, while insulators are materials that block the flow of current almost completely. Thus, a semiconductor is a material which will behave like a conductor under given physical conditions (e.g. when exposed to light or an increase in temperature) and as an insulator under differing conditions [1].

When atoms are brought together to form a molecule or solid structure, their individual atomic energy levels split to form a band of allowed energy levels. These bands of energy levels may or may not overlap, depending on the properties of the atoms, the relative strength of their atomic bonding, and their geometric arrangement. The highest occupied band is referred to as the **valence** band (VB) while the lowest unoccupied energy band is referred to as the **conduction** band (CB) [13]. Materials with partially filled valence bands or overlapping valence and conduction bands are metals. In the case of semiconductors and insulators, the valence band is completely filled and separated from the conduction band by an energy gap, E_g as shown in figure 2.1. The difference between semiconductors and insulators is that in semiconductors, the energy gap is small enough ($0.5 \leq E_g \leq 3.0$ eV) for electrons to be thermally excited into the conduction band at normal temperatures [13].

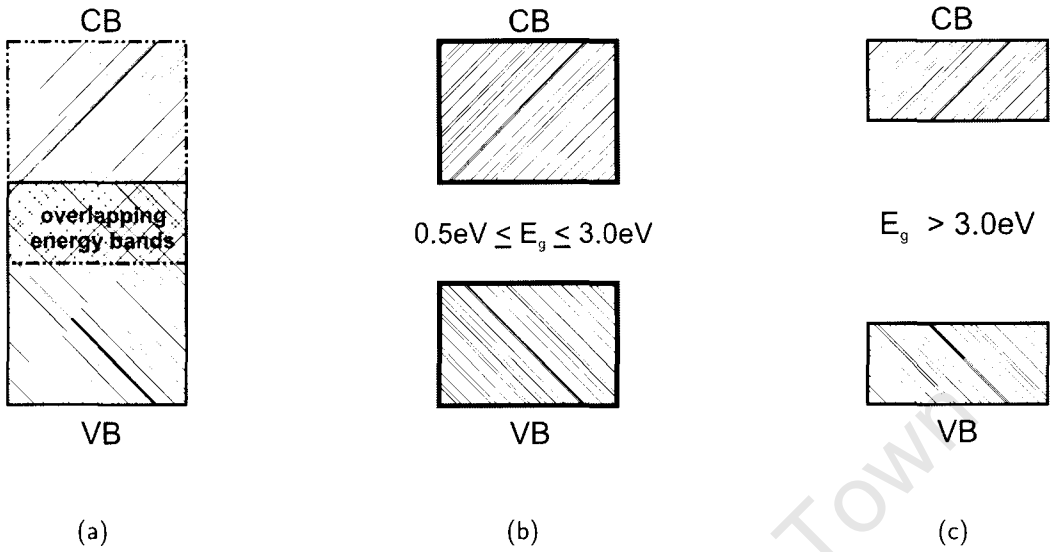


Figure 2.1: Energy band gap diagrams for (a) metals, (b) semiconductors and (c) insulators. In (a) the conduction and valence bands overlap while in (b) and (c), there is an energy gap.

2.2.1 Intrinsic Semiconductors

At a temperature of absolute zero, a pure or **intrinsic** semiconductor would not conduct electricity because all of its electrons are involved in bonding and, hence, the conduction band is empty as shown in figure 2.2(a). With increasing temperature, the electrons in the valence band gain kinetic energy and are able to move into the conduction band, where they are able to transport charge and energy [11]. When this happens, the electrons leave behind a positively charged hole in the valence band. Further increase in temperature causes more electrons to be promoted to the conduction band and there is a corresponding and equal increase in the number of holes in the valence band as illustrated in figure 2.2(b).

In the presence of an electric field, conduction electrons can move, with a corresponding movement of holes in the valence band. Electrons can also be promoted to the conduction band if photons of the right energy are absorbed; a phenomenon referred to as *photoconductivity* [8]. If $f(\mathbf{k},\mathbf{r})$ is the probability that at a point $\mathbf{r}$, the electron state of a wave vector $\mathbf{k}$ is occupied, then the electron density in the conduction band over all $\mathbf{k}$ states in the reciprocal space volume $\mathbf{d^3k}$ is given by [8]

$$n(\mathbf{r}) = \int_{\text{conduction band } \mathbf{k}} g_c(\mathbf{k}) f(\mathbf{k},\mathbf{r}) \mathbf{d^3k} \quad . \tag{2.1}$$

(a) (b)

Figure 2.2: (a) The band diagram for a semiconductor in the ground state; the valence band is completely filled. After excitation, the electrons move into the conduction band leaving behind holes in the valence band as shown in (b).

Similarly, since a hole is an unoccupied electron state, the hole density is given by [8]

$$p(\mathbf{r}) = \int_{\text{valence band } \mathbf{k}} g_v(\mathbf{k})(1 - f(\mathbf{k}, \mathbf{r}))\mathbf{d^3k} \quad . \tag{2.2}$$

where g_c and g_v are the densities of states in the conduction and valence bands respectively.

Using Fermi-Dirac statistics, at an ambient temperature T, f is dependent on the wave vector $\mathbf{k}$ and independent of position, and we have [14]

$$f(\mathbf{k}, \mathbf{r}) = f_0(E(\mathbf{k}), E_F, T) \quad . \tag{2.3}$$

$f_0(E(\mathbf{k}), E_F, T)$ is the Fermi-Dirac distribution function, which gives the probability that at a given energy E, an electron state is occupied at a temperature T, and is given as [14]

$$f_0(E(\mathbf{k}), E_F, T) = \frac{1}{e^{(E-E_F)/k_BT} + 1} \quad . \tag{2.4}$$

where k_B is Boltzmann's constant and the Fermi level E_F, is the chemical potential of the electron distribution. In equilibrium, the density $n(E)$ of electrons with energy in the range E to $E + dE$ in a system having density of states $g(E)$ is given by [8]

$$n(E)dE = g(E)f_0(E, E_F, T)dE \quad . \tag{2.5}$$

Thus, the total density of electrons in the conduction band of minimum energy E_c is

$$n = \int_{E_c}^{\infty} g_c(E)f_0(E, E_F, T)dE \quad , \tag{2.6}$$

and for holes in the valence band of maximum energy E_v, the density is given by

$$p = \int_{-\infty}^{E_v} g_v(E)(1 - f_0(E, E_F, T))dE \quad . \tag{2.7}$$

Using Maxwell-Boltzmann's approximation, in the conduction band, if $E \gg E_F$, then from (2.4),

$$f_0(E, E_F, T) \approx e^{(E_F - E)/k_B T} \quad , \tag{2.8}$$

and in the valence band, $E \ll E_F$, so

$$1 - f_0(E, E_F, T) \approx e^{(E - E_F)/k_B T} \quad . \tag{2.9}$$

The parabolic band approximations for $g_c(E)$ and $g_v(E)$ are given by [8]

$$g_c(E) = \frac{1}{2\pi^2}\left(\frac{2m_c^*}{\hbar^2}\right)^{3/2}(E - E_{c_0})^{3/2} \quad , \tag{2.10}$$

and

$$g_v(E) = \frac{1}{2\pi^2}\left(\frac{2m_v^*}{\hbar^2}\right)^{3/2}(E - E_{v_0})^{3/2} \quad , \tag{2.11}$$

where m_c^* and m_v^* are the effective masses of electrons and holes respectively, E_{c_0} is the minimum energy in the conduction band, and E_{v_0} is the maximum energy in the valence band with $\hbar = h/2\pi$, where h is Planck's constant. Using these expressions for $g_c(E)$ and $g_v(E)$, and equations (2.8), (2.9) in equations (2.6) and (2.7), we obtain the electron density to be

$$n = N_c \exp[(E_F - E_c)/k_B T] \quad , \tag{2.12}$$

where N_c is a constant referred to as the effective conduction band density of states given by

$$N_c = 2\left(\frac{m_c^* k_B T}{2\pi\hbar^2}\right)^{3/2} \quad . \tag{2.13}$$

Similarly, the hole density is

$$p = N_v \exp[(E_v - E_F)/k_B T] \quad , \tag{2.14}$$

with the constant N_v, the effective valence band density of states given by

$$N_v = 2\left(\frac{m_v^* k_B T}{2\pi\hbar^2}\right)^{3/2} \quad . \tag{2.15}$$

Thus, we can deduce from equations (2.12) and (2.14) that in a semiconductor, the electron and hole densities vary exponentially with the position of their Fermi levels in the band gap.

Furthermore, we can see that the product of the electron and hole densities at a given temperature for a given material with energy gap E_g

$$np = N_c N_v e^{-E_g/k_B T} \quad , \tag{2.16}$$

is a constant. This relationship is referred to as the law of mass action, and the intrinsic carrier density n_i [11] is a property of the material,

$$n_i^2 = np = N_c N_v e^{-E_g/k_B T} \quad . \tag{2.17}$$

The conductivity of the intrinsic semiconducting material is given by [15]

$$\sigma = q\mu_n n + q\mu_p p \quad , \tag{2.18}$$

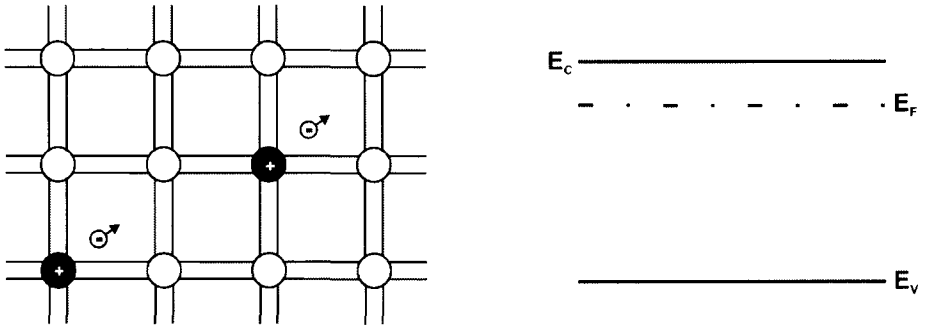
where q is the electronic charge, μ_n and μ_p are the mobilities of the electrons and holes respectively. Thus, we see from equation (2.18), that conduction in a semiconductor is determined by the mobilities of the charge carriers and their densities (which in turn depend on the band gap of the material). Hence, the conductivity of a semiconductor can be increased by altering, in some way, the respective concentrations of electrons and holes within the semiconductor. The process by which an 'impurity' or 'defect' is introduced into an intrinsic semiconductor in order to enhance its electrical properties is referred to as **doping** [15].

2.2.2 Extrinsic Semiconductors

If an intrinsic semiconductor such as silicon, is doped with a pentavalent element like phosphorous, the density of electrons relative to that of holes can be greatly increased, leading to an excess of free electrons. Such a semiconductor is called **n**-type (n being negative) as shown in figure 2.3(a) [1, 15].

In an intrinsic semiconductor the Fermi level lies roughly midway between the conduction band energy E_c, and the valence band energy E_v. However, after n-type doping, as shown in figure 2.3, the donor electrons from the dopant cause the Fermi level to shift toward the conduction band [8, 16]. Conduction in n-type semiconductors is primarily by electrons and if the density of dopants N_d is varied, the carrier density can be controlled. If $N_d \gg n_i$ and the donors are fully ionised at room temperature, then the free electron concentration is [8, 15]

$$n \approx N_d \quad . \tag{2.19}$$



(a) (b)

Figure 2.3: Schematic diagrams of the (a) crystal structure and (b) energy band diagram of an n-type semiconductor. The excess electrons result in a net increase in negative charge carriers, and a shift of the Fermi level towards the CB.

From equation (2.17), the hole concentration is

$$p = \frac{n_i^2}{N_d} \quad . \tag{2.20}$$

Electrons are called the majority carriers and holes the minority carriers and the **total** density of carriers in the semiconductor is increased greatly leading to an increase in conductivity by equation (2.18).

On the other hand, as shown in figure 2.4(a), if an intrinsic semiconductor is doped with a trivalent element such as boron, we have an excess of holes and the semiconductor is referred to as a **p** (positive) type semiconductor.

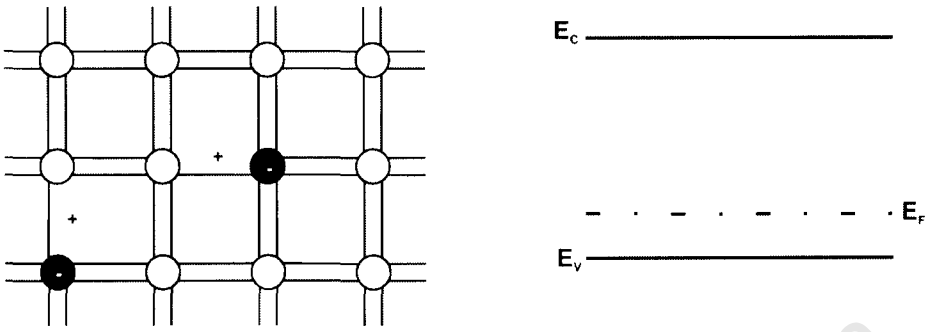
In this case, the Fermi level shifts toward the valence band [8]. Holes are the primary charge carriers in p-type semiconductors. The density of dopants is N_a, and if the doping density $N_a \gg n_i$, then the hole concentration

$$p \approx N_a \quad , \tag{2.21}$$

and by equation (2.17), the electron concentration is

$$n = \frac{n_i^2}{N_a} \quad . \tag{2.22}$$

As in n-type semiconductors, the total carrier density is increased, leading to an increased conductivity in the semiconductor. Thus, doping is a way of increasing conductivity in a semiconductor



(a) (b)

Figure 2.4: Schematic diagrams showing the (a) crystal structure of a p-type semiconductor and (b) the corresponding energy band diagram. The deficit of electrons leaves a hole resulting in a net increase in positive charge carriers and a shift of the Fermi level towards the VB.

at equilibrium without requiring a constant input of energy [8]. For heavily doped semiconductors, imperfections arise which appear as states in the band gap close to the conduction and valence band edges. This leads to the formation of an Urbach tail [8] causing the intrinsic carrier density to increase because thermal excitation across the band gap is easier [8]. However, heavy doping also results in an increase in the number of defect states which act as centres for carrier trapping or recombination [8].

2.2.3 Photovoltaic Effect

Semiconductors are good materials for producing photovoltaic devices because of the band gap in their electronic structure which allows photons of a suitable energy to cause an electron to be excited across the gap [8]. In equilibrium, there is no net flow of carriers, and electron and hole currents are zero. As mentioned in section 2.1, when light shines on a semiconductor, generation of excess charges occurs within the semiconductor. The electron and hole densities are increased above their equilibrium values so that equation (2.17) no longer holds. Assuming the deviation from the equilibrium distribution is not too large nor changing very quickly, the electron and hole populations relax and achieve a state of **quasi-thermal** equilibrium [8]. The distribution

functions for electrons and holes are now given by [11]

$$f_c(\mathbf{k},\mathbf{r}) \approx f_0(E, E_{F_n}, T_n) \quad , \tag{2.23}$$

and

$$f_v(\mathbf{k},\mathbf{r}) \approx f_0(E, E_{F_p}, T_p) \tag{2.24}$$

respectively. E_{F_n} and E_{F_p} are referred to as the quasi Fermi levels of electrons and holes respectively. If we consider the conduction band, since f_c cannot be completely described by the quasi-thermal equilibrium distribution function, an additional term f_A is added to f_0 so that [8]

$$f_c(\mathbf{k},\mathbf{r}) = f_0(E, E_{F_n}, T_n) + f_A(\mathbf{k},\mathbf{r}) \quad . \tag{2.25}$$

where

$$f_0(E, E_{F_n}, T_n) = \frac{1}{e^{(E-E_{F_n})/k_B T_n} + 1} \quad . \tag{2.26}$$

f_A can be found using the Boltzmann transport equation and is given by [8, 11]

$$f_A = -f_0 \frac{\tau \mathbf{v}}{k_B T} \cdot \nabla E_{F_n} \quad , \tag{2.27}$$

where $\mathbf{v}$ is the velocity of the carriers and τ is a characteristic time constant. Thus, the semiconductor has been biased by the action of the light. In this state of quasi thermal equilibrium, the electron and hole densities given in equations (2.12) and (2.14) become

$$n = N_c \exp[(E_{F_n} - E_c)/k_B T_n] \tag{2.28}$$

and

$$p = N_v \exp[(E_v - E_{F_p})/k_B T_p] \quad . \tag{2.29}$$

where T_n and T_p are the effective electron and hole temperatures respectively. Electrons with T_n greater than the ambient temperature, are referred to as hot electrons [8], and usually arise under strong electric fields. In this formulation however, it is assumed that this condition does not arise, so that $T_n = T_p = T$. As before, using Boltzmann's statistics where $E_{F_n} - E_c \gg k_B T$ and $E_v - E_{F_p} \gg k_B T$, then

$$np = n_i^2 e^{\Delta\mu/k_B T} \tag{2.30}$$

with

$$\Delta\mu = E_{F_n} - E_{F_p} \quad . \tag{2.31}$$

Using the Boltzmann's transport equation to solve equation (2.25), it is noted that under biasing due to light, the electron and hole current densities are given by [8]

$$J_n(\mathbf{r}) = \mu_n n \nabla E_{F_n} \quad , \tag{2.32}$$

and

$$J_p(\mathbf{r}) = \mu_p p \nabla E_{F_p} \quad , \tag{2.33}$$

so that the net current at any given point $\mathbf{r}$ is given by

$$\begin{aligned} J &= J_n(\mathbf{r}) + J_n(\mathbf{r}) \\ &= \mu_n n \nabla E_{F_n} + \mu_p p \nabla E_{F_p} \quad . \end{aligned} \tag{2.34}$$

Drift and Diffusion Currents

By expressing equations (2.28) and (2.29) in terms of E_{F_n} and E_{F_p}, setting $T_n = T_p = T$ and differentiating, we obtain

$$\nabla E_{F_n} = \nabla E_c - k_B T \nabla \ln N_c + \frac{k_B T}{n} \nabla n \tag{2.35}$$

and

$$\nabla E_{F_p} = \nabla E_v - k_B T \nabla \ln N_v + \frac{k_B T}{p} \nabla p \quad . \tag{2.36}$$

The gradients ∇E_c and ∇E_v in the conduction and valence band edges are a result of an electric field F and the gradient in the electron affinity χ in the band gap, so that [8]

$$\nabla E_c = qF - \nabla \chi \quad . \tag{2.37}$$

and

$$\nabla E_v = qF - \nabla \chi - \nabla E_g \quad . \tag{2.38}$$

Using the expressions above, equations (2.32) and (2.33) can be written as

$$J_n = \mu_n k_B T \nabla n + \mu_n n (qF - \nabla \chi - k_B T \nabla \ln N_c) \quad , \tag{2.39}$$

and

$$J_p = -\mu_p k_B T \nabla p + \mu_p p (qF - \nabla \chi - \nabla E_g + k_B T \nabla \ln N_v) \quad . \tag{2.40}$$

In a material where χ, E_g, N_c and N_v are constant, their derivatives will equal zero [8]. Using that result together with the Einstein relations [15]

$$\frac{D_n}{\mu_n} = \frac{k_B T}{q} \quad \text{and} \quad \frac{D_p}{\mu_p} = \frac{k_B T}{q} \quad ,$$

where D_n and D_p are the diffusion constants, equations (2.39) and (2.40) reduce to

$$J_n(\mathbf{r}) = q D_n \nabla n + q \mu_n F n \quad , \tag{2.41}$$

and

$$J_p(\mathbf{r}) = -qD_p\nabla p + q\mu_p Fp \quad . \tag{2.42}$$

Looking at equations (2.41) and (2.42), we see that the current flow in a biased semiconductor can be broken up into two parts: a drift current set up by an electric field, and a diffusion current which is driven by gradients in the concentrations of the electrons and holes [14]. If the concentration of electrons and holes are similar, there will be no net diffusion current in the semiconductor. Current flow within the semiconductor will only be due to the electric field applied across the semiconductor. However, if there is no electric field applied across the semiconductor and there exists a large imbalance in the electron and hole concentrations, a diffusion current will arise within the semiconductor. Thus, when light shines on a semiconductor, there is a deviation from the equilibrium and quasi-equilibrium Fermi levels, resulting in a drift current being generated. This phenomena of photocurrent generation can then be exploited in the design of photovoltaic devices.

2.3 Photovoltaic Devices

A PV cell is designed primarily for the generation of a photocurrent, whose magnitude is determined by factors such as light absorption, current generation and charge recombination. **Photogeneration** is the principal carrier generation mechanism in PV cells, and is defined as the generation of mobile electrons and holes through light absorbed in a semiconductor [8]. Photogeneration requires the dissociation of an excited state, and it is not the same as light absorption in some materials, where dissociation is not complete [8]. In a material, the total generation rate is given by [8]

$$G(x) = \int g(E,x)dE \quad , \tag{2.43}$$

where $g(E,x)$ is the rate of carrier generation per unit volume at a depth x below the surface. The major charge recombination processes are [8, 11]:

- **Radiative recombination** which is due to the relaxation of an electron across the energy band gap accompanied by the emission of a photon. It is of great importance in direct band gap semiconductors [16].
- **Auger recombination**, which occurs when a charge carrier relaxes causing the excitation of another carrier to a higher energy state within the band. Auger recombination is dependent on charge carrier densities and is dominant when those densities are high.

- **Trap assisted recombination** occurs in multiple steps involving intermediate states within the band gap. The rate at which this occurs is dependent on the position and density of the intermediate states and on the relative densities of electrons and holes.

2.3.1 PV Working Principles

For a light absorbing device to function as a PV cell, it must not only generate a photocurrent as a result of photogeneration and charge transport, but there must also be a mechanism for charge separation [12]. This mechanism is crucial for PV energy conversion and involves an electric field or physical variation within the device. This mechanism could also be achieved by applying an external potential difference across the semiconductor [8].

The current at a point in a semiconductor under a light induced bias is given by equation (2.34). In equilibrium, E_{F_n} and E_{F_p} are constant and, therefore, the current J, is zero everywhere. In order to achieve photovoltaic action, there must be a light induced gradient within the quasi Fermi level. We can then write equations (2.39) and (2.40) as

$$J_n = qD_n\nabla(n-n_0) + \mu_n(n-n_0)(qF - \nabla\chi - k_BT\nabla\ln N_c) \quad , \tag{2.44}$$

and

$$J_p = -qD_p\nabla(p-p_0) + \mu_p(p-p_0)(qF - \nabla\chi - \nabla E_g + k_BT\nabla\ln N_v) \quad , \tag{2.45}$$

with n_0 and p_0 being the equilibrium carrier densities. When the PV device is illuminated, $n > n_0$ and $p > p_0$. Thus, in a non-zero electric field, we have a drift current and in the absence of an applied electric field, but with a gradient in the carrier densities, a diffusion current will dominate within the semiconductor. As a result, charge carrier separation can be achieved by [8]:

- a gradient in the work function of the materials that make up the PV device,
- a gradient in the electron affinity χ, or
- a gradient in the band gap of the material.

These conditions can be obtained by means of an interface between two different materials, or, in semiconductors, by varying the doping levels in a single semiconductor [12]. These are referred to as a heterojunction and homojunction respectively, and will be discussed in section 2.3.3.

2.3.2 PV Junctions

Simply defined, the work function Φ_w, of a material is the energy required to remove the least tightly bound electron in the material, and is given by [8]

$$\Phi_w = (E_{vac} - E_F) \quad , \tag{2.46}$$

where E_{vac} is the vacuum potential to which all energies in the crystal are referenced. In metals, Φ_w is the same as the electron affinity χ, while in semiconductors, the work function can be controlled by means of doping. In equilibrium, E_F is constant, so in order to create a gradient, two materials of differing affinities can be brought together to form a heterojunction, or two layers can be created within the *same* semiconductor material by doping it differently in order to form a homojunction [11]. The difference in work functions creates an electrostatic field which obeys [8]

$$q\int_{x_-}^{x_+} F dx = \Phi_w(x_+) - \Phi_w(x_-) = \Delta\Phi_w \quad , \tag{2.47}$$

where x_+ and x_- are the positions far from the junctions. This results in a distribution of charge within the junction.

2.3.3 P-N Junctions

The p-n junction represents the most common structure used in designing solar cells and can exist as a p-n **heterojunction** or **homojunction**. The p-n homojunction is widely used in PV cell fabrication and can be created by continuously varying the doping levels of a single crystal wafer during or after its growth [17]. The p-n heterojunction can be created by bringing two separate layers of n- and p-type semiconductors together. The heterojunction design variation can improve carrier collection within the device [8].

The selective doping of different sides of a silicon wafer to form a homojunction leads to the formation of a potential barrier, since the work function for a p-type material is higher than that of an n-type material. This leads to an electric field being established at the junction. Thus, photogenerated electrons drift across the semiconductor toward the n-side of the junction, and holes toward the p-side [1]. Equilibrium is reached when the diffusion of majority carriers is balanced by the drift of minority carriers due to a built in bias given by [15]

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right) \quad . \tag{2.48}$$

where N_d and N_a are the n and p doping levels, and n_i is the intrinsic carrier concentration as discussed earlier.

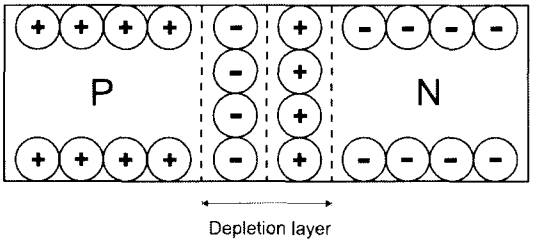


Figure 2.5: Formation of a depletion layer in a p-n junction. Electrons dominate on the p-type region of the junction while holes dominate in the n-type region. Outside the depletion region, holes dominate on the p-type region while electrons dominate the n-type region.

As shown in figure 2.5, the movement of carriers across the junction creates a depletion layer at the junction, which results in two regions being formed; one with a higher concentration of holes, and the other one with a higher concentration of electrons. Minority carriers that are photogenerated in the p and n layers reach the junction by diffusion [1].

When the PV cell is illuminated, photogenerated holes build up on the p-side and electrons on the n-side. This flow of charge carriers is, by definition, an electric current which flows out of the semiconductor by means of the metal contacts of the PV cell. The p-n junction is reverse biased (i. e. the voltage across the junction is in the negative direction) [16] and if an external bias voltage V is applied, the Fermi level on one side of the junction is raised with respect to the other and the potential across the junction becomes [8]

$$V_j = V_{bi} - V \quad . \tag{2.49}$$

A negative value of V will result in an increase in the width of the depletion layer, while a positive value reduces the depletion layer and if V is large enough, cancels out the potential step, eliminating the PV effect [8]. Figure 2.6 shows the band profile of a p-n junction device, illustrating how the Fermi levels of the p- and n-type semiconductors align when a p-n junction is formed.

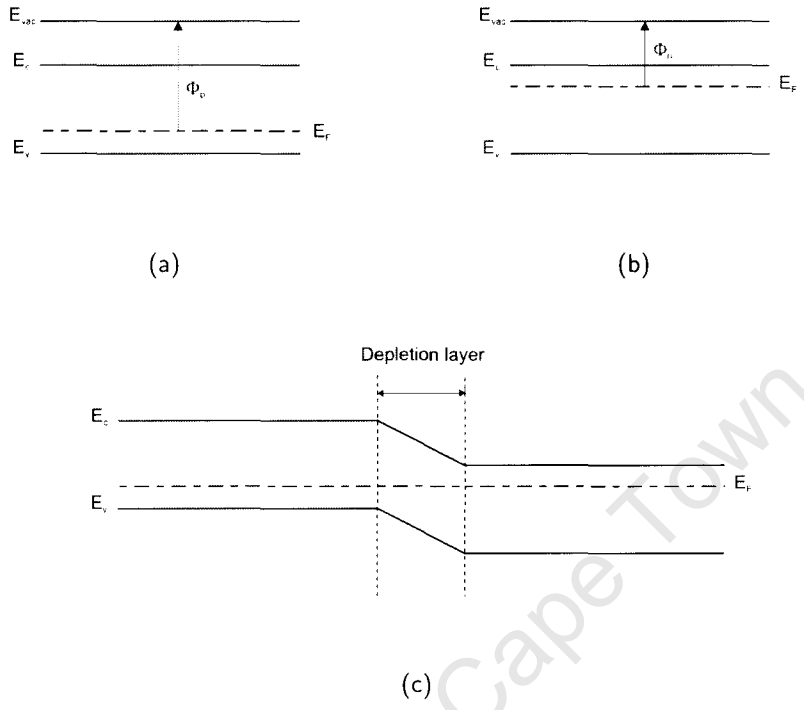


Figure 2.6: Band profiles of (a) p- and (b) n-type semiconductors and (c) the p-n junction in equilibrium.

2.3.4 Other PV Junctions

Although p-n junctions are the most common configuration used in designing PV devices, other types of junctions also exist. Some of these are described below.

Metal-Semiconductor Junction

When an n-type semiconductor of work function Φ_n, is brought together in electronic contact with a metal of work function Φ_m, a metal-semiconductor junction is created as shown in figure 2.7. Electrons flow from the semiconductor to the metal resulting in a layer of positive charge in the semiconductor, and a negative image charge on the metal [8]. In thermal equilibrium, a charge gradient is built up until there is no more further flow of charges. Due to the fact that metals are not good for charge storage, most of the potential difference is dropped in the semiconductor. A space charge region is formed from the junction to a point within the semiconductor where, beyond this region, the electric field falls to zero [11]. This joining of the semiconductor to a metal of a larger work function creates a field close to the interface resulting in charge separation.

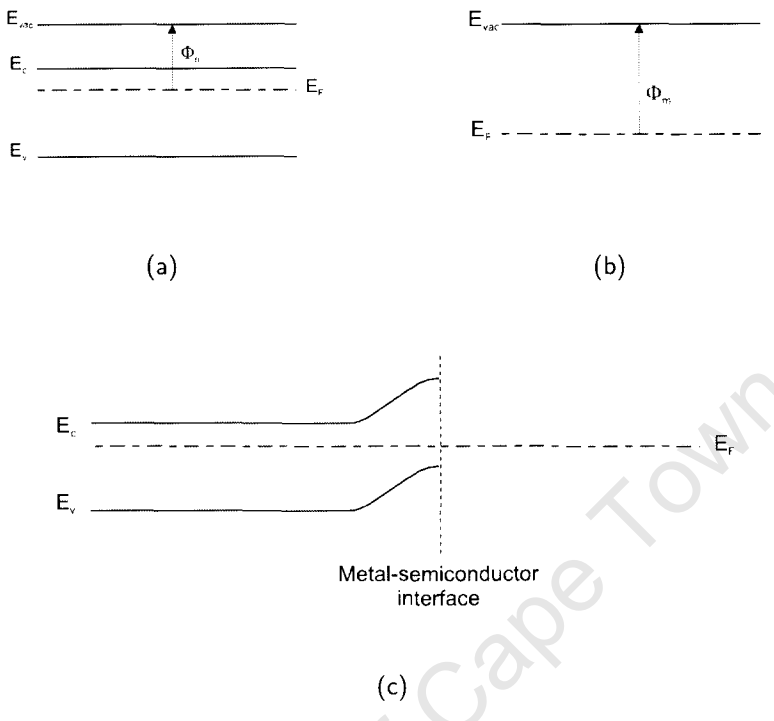


Figure 2.7: Band profiles of (a) an n-type semiconductor and (b) a metal, and (c) the metal-semiconductor junction in equilibrium.

A potential barrier is set up at the metal-semiconductor interface due to the difference in the work functions of the metal and semiconductor. This barrier is referred to as a Schottky barrier [16] which presents a lower resistance path for holes than electrons.

This sort of behaviour is similar if a p-type semiconductor is used in the formation of the junction, the difference being that $\Phi_p > \Phi_m$ and the band bends downwards toward the interface and the semiconductor becomes negatively charged [11]. Unlike the p-n junction, a metal-semiconductor junction produces lower photovoltages due to the formation of an inversion layer which occurs when minority carriers dominate at the surface of the semiconductor, and tunnelling through the Schottky barrier [8].

Electrochemical Junctions

An electrochemical junction involves the establishment of a potential barrier between a semiconductor and a liquid electrolyte containing a redox couple capable of transporting charges to and from the semiconducting surface [6].

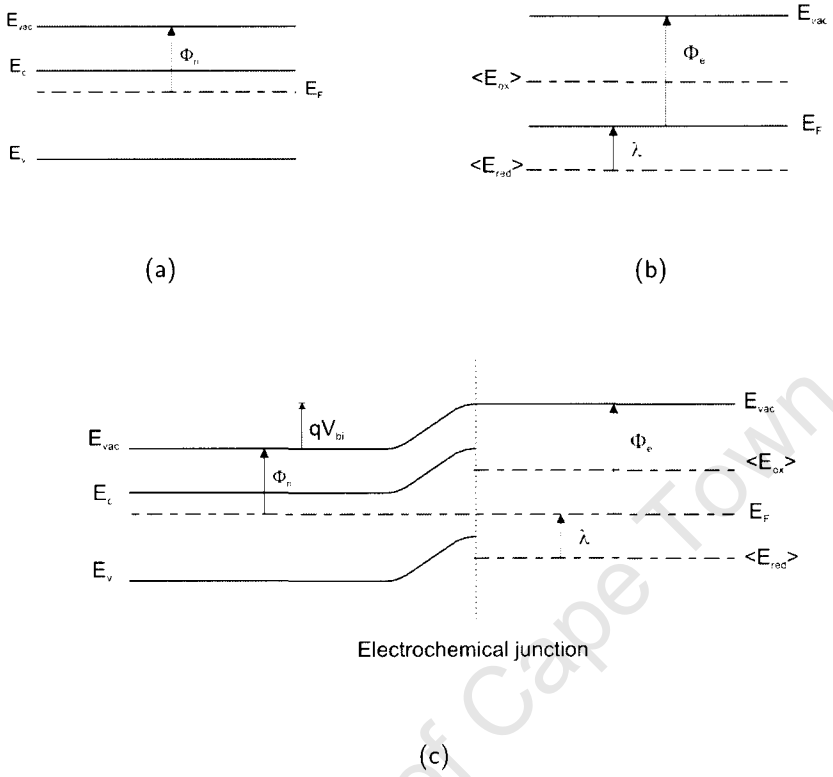


Figure 2.8: The band profiles of (a) an n-type semiconductor, (b) a redox electrolyte and (c) electrochemical junction in equilibrium. λ is the reorganisation energy.

When these materials are brought in contact, electrons flow from the semiconductor into the electrolyte until, at equilibrium, the Fermi levels equalize, resulting in a positive space-charge layer in the semiconductor, and an electric field at the interface, driving charge separation as shown in figure 2.8. The difference between the redox potential and the mean energy of the reduced state of the electrolyte is referred to as the reorganisation energy λ [8]. The electrochemical junction has a field that is established spontaneously when the electrolyte comes in contact with the semiconductor surface, but usually a chemical reaction occurs between the two materials during illumination which degrades the performance of the PV cell [6].

P-I-N Junction

The p-i-n junction is a variation of the p-n junction but with a layer of intrinsic semiconductor in between the p and n layers. This can be achieved by means of heterojunctions or homojunctions (in which a region between the p and n layers is left undoped in a wafer). The behaviour is similar

to the p-n PV cell but the electric field generated extends over a wider region (figure 2.9). This design is most commonly used with materials that have a short minority carrier diffusion length, so that carriers generated within the p and n layers do not make much of a contribution to the photocurrent [8]. With the addition of the intrinsic layer, more carriers are available for charge transport. However, the i-layer has poorer conductivity and a greater probability for recombination in forward-bias, which may cause the field to fall to zero in the intrinsic region. This design is used mostly in amorphous silicon (a-Si) based solar cells [12, 18].

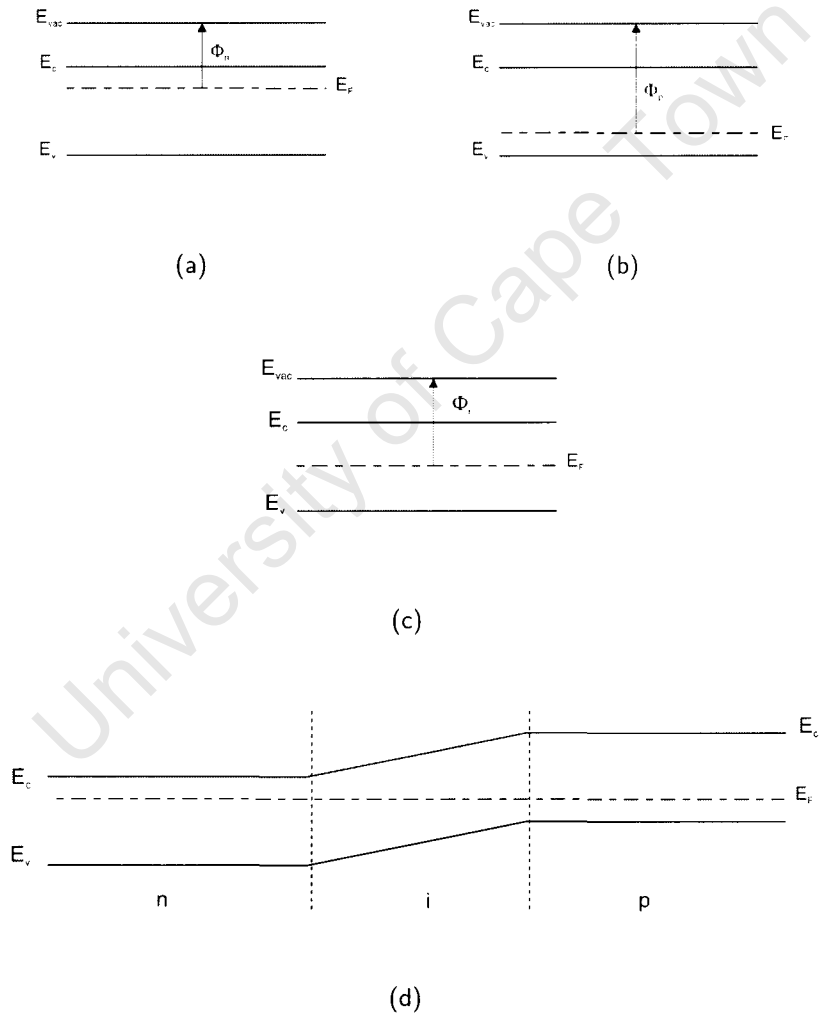


Figure 2.9: The band profiles of (a) n, (b) p, and (c) intrinsic semiconductors. (d) shows the band profile of the p-i-n junction in equilibrium.

2.4 Characteristics of Solar Cells

A PV cell has a number of properties which must be considered in its design. Some of these have been mentioned earlier. Following below is a description of some of the major characteristics of PV cells.

2.4.1 Photocurrent and Quantum Efficiency

When a p-n junction PV device is illuminated, electron-hole pairs are generated, leading to the development of a photocurrent depending on the intensity of the incident light [16]. The net photocurrent is given by [8]

$$J_{sc} = \int_0^\infty j_{sc}(E)dE \quad , \tag{2.50}$$

where

$$j_{sc}(E) = -j_n(E, -w_p) - j_p(E, w_n) - j_{gen}(E) \quad . \tag{2.51}$$

is the short circuit photocurrent for radiation with photons of energy E, where j_n and j_p are the photocurrents in the neutral n and p regions of the junction, and j_{gen} is the current in the space charge region or depletion layer. The quantum efficiency QE, of the PV cell is defined as the probability that a photon of energy E, incident on the cell will liberate an electron to the external circuit and is given by [16]

$$QE(E) = \frac{j_{sc}}{qb_s(E)} \quad , \tag{2.52}$$

where $b_s(E)$ is the incident spectral photon flux density, which is the number of photons in the range E to $E + dE$ incident on a unit area in unit time. Thus, the photocurrent density can be written as

$$J_{sc} = q\int_0^\infty b_s(E)QE(E)dE \quad . \tag{2.53}$$

The quantum efficiency is dependent on the absorption coefficient of the PV material and the efficiency of charge separation and collection within the device. Thus, it is very important in describing the performance of a PV cell having different material properties such as the thickness of the material, transmissivity and reflectivity at the surface of the PV device [8].

2.4.2 Dark current, Open Circuit Voltage

The dark current J_{dark}, is defined as the current which flows in the PV cell under an applied bias without illumination. When connected to an external load, a potential difference is developed

between the terminals of the solar cell which acts in a direction opposite to the photocurrent, and the net current within the cell is reduced from the short circuit current J_{sc}. The dark current is given by [19]

$$J_{dark} \approx J_0(e^{qV/mk_BT} - 1) \quad , \tag{2.54}$$

where J_0 is a constant and m is the ideality factor. For an ideal diode, $m = 1$ and is the most commonly used expression when modelling ideal PV cells [19, 20]. Equation (2.54) is referred to as the non-ideal diode equation and the effect of $m > 1$ is to reduce the fill factor of the cell. If $e^{qV/mk_BT} \gg 1, m$ can be determined from [8]

$$\frac{1}{m} = \frac{k_BT}{q}\frac{d}{dV}\ln J_{dark} \quad . \tag{2.55}$$

The overall current-voltage (I-V) response of the PV cell, referred to as its I-V characteristics, is approximated as the sum of J_{sc} and J_{dark} and is termed the **superposition approximation** [8]. J_{dark} is conventionally taken to be in the opposite sense to J_{sc}, thus for a PV cell [16]

$$J(V) \quad = \quad J_{sc} - J_{dark}(V) \approx J_{sc} - J_0(e^{qV/mk_BT} - 1) \quad . \tag{2.56}$$

The open circuit voltage V_{oc}, is the potential difference which develops between the terminals when no current flows through the illuminated PV cell [16] and can be obtained from equation (2.56) as

$$V_{oc} = \frac{mk_BT}{q}\ln\left(\frac{J_{sc}}{J_0} + 1\right) \quad . \tag{2.57}$$

V_{oc} increases logarithmically with increase in light intensity. A photovoltage is generated in forward bias when the applied voltage $V > 0$. However, when $V < 0$, the PV cell acts a photodetector, consuming power rather than generating it [8].

The ideal solar cell $(m = 1)$ is equivalent to a current generator connected in parallel to a diode [8, 16] as shown in figure 2.10.

2.4.3 Efficiency

The PV cell operates in a region where it delivers power when under bias. The power density is [8, 16]

$$P = JV \quad . \tag{2.58}$$

The output power is maximum when the cell operates at the maximum power point. This occurs at a voltage V_m corresponding to a current J_m as shown in figure 2.11.

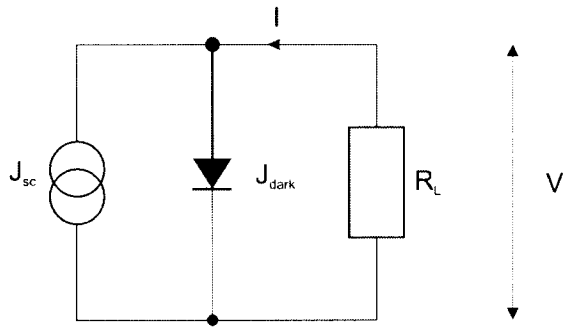


Figure 2.10: Ideal solar cell circuit diagram under illumination. R_L is the load resistance across the cell.

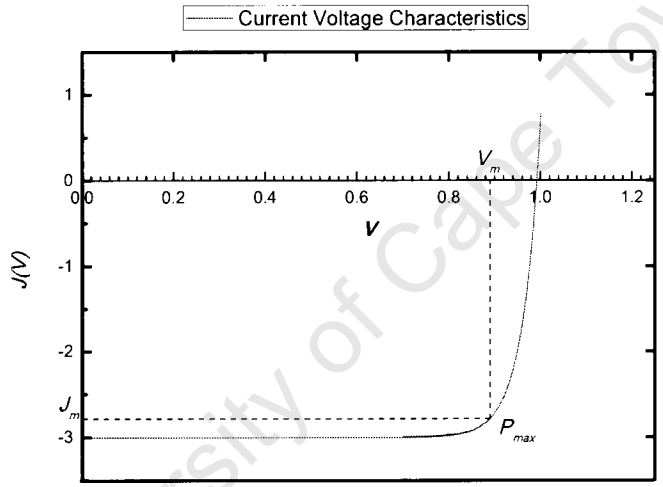


Figure 2.11: Characteristic I-V curve of a practical solar cell. P_{max} is the maximum power point.

The measure of the "squareness" of the J-V curve is described by a quantity called the fill factor, which is given by the ratio [21]

$$FF = \frac{J_m V_m}{J_{sc} V_{oc}} \quad . \tag{2.59}$$

The efficiency of the solar cell is defined by the power density delivered at the maximum power point, as a fraction of the incident light power density P_s, given by [16]

$$\eta = \frac{J_m V_m}{P_s} \quad ; \tag{2.60}$$

and, using equation (2.59), it can then be written as

$$\eta = \frac{J_{sc} V_{oc} FF}{P_s} \quad . \tag{2.61}$$

The short circuit current J_{sc}, open circuit voltage V_{oc}, fill factor FF and efficiency η are the key performance characteristics of a solar cell.

2.4.4 Parasitic Resistances

In a practical solar cell, power is dissipated through **series** and **shunt** resistances [22]. The corresponding circuit diagram is as shown in figure 2.12. Series resistances (R_s) occur as a result of resistance to current flow within the semiconducting material and the contacts between the layers in the PV device. This results in a potential drop between the junction and the applied potential difference across the terminals. The series resistance is of particular importance at high current densities. Shunt resistances (R_{sh}) arise from leakage of current through the cell, around the PV device edges and between contacts of different polarity. The shunt resistance is particularly important in poorly rectifying devices [8].

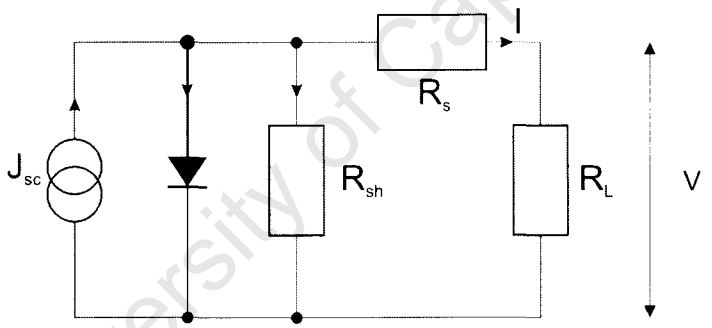


Figure 2.12: Equivalent circuit of a practical solar cell, taking into account the series and shunt resistances, R_s and R_{sh}.

Taking R_s and R_{sh} into account, equation (2.56) becomes [23, 24]

$$J = J_{sc} - J_0(e^{q(V+JR_s)/k_BT} - 1) - \frac{V + JR_s}{R_{sh}} \quad , \tag{2.62}$$

where JR_s is the potential drop between the junction and the applied potential difference V_{app} at the terminals and is given by [8]

$$JR_s = V - V_{app} \quad . \tag{2.63}$$

Hence, to boost efficiencies, the series resistance should be made as small as possible and the shunt resistance as large as possible [23]. Current methods used in modelling solar cell I-V

characteristics involve the use of the double diode equation [25] in which a second exponential current term is subtracted from equation (2.62) so that the solar cell is described by [26, 27]

$$J = J_{sc} - J_{0_1}(e^{q(V+JR_s)/m_1k_BT} - 1) - J_{0_2}(e^{q(V+JR_s)/m_2k_BT} - 1) - \frac{V + JR_s}{R_{sh}} \quad , \qquad (2.64)$$

where J_{0_1}, J_{0_2} are the diode saturation currents and m_1, m_2 are their corresponding ideality factors.

2.4.5 Other Effects

Other factors such as higher irradiation and high temperatures affect the performance of PV devices. Higher irradiation leads to an increase in series resistances resulting in an increase in the temperature of the device. This causes a degradation in its performance [28]. This means that the PV cell has an optimum efficiency at a finite solar concentration.

Increasing temperature also leads to an increase in the dark current J_{dark}, due to the increase in the intrinsic carrier concentration n_i, which in turn leads to a reduction in open circuit voltage V_{oc} [27, 28]. It also results in a reduction in the band gap, increasing the photocurrent. However, the net effect is a reduced efficiency of the PV cell [28].

2.5 Types of Solar Cells

The different methods employed in the fabrication of solar cells depend mainly on the type of semiconductor used in the device. The focus of this research involves the implementation of a new design and fabrication technique for manufacturing solar cells. In order to highlight the uniqueness of this approach, some of the more common design and fabrication methods are outlined and discussed in this section.

2.5.1 Bulk Crystalline Solar Cells

Currently, the most common solar cells are based on crystalline silicon. In a crystalline structure, the atoms are arranged in a well-ordered manner, represented by a periodic array of points in space called a lattice, with atoms or group of atoms at each point [29]. Solar cells fabricated using bulk crystalline semiconductors are based on wafer technology, which was originally developed

for the production of integrated circuits. Solar cells based on crystalline materials are usually referred to as *first generation* photovoltaics [1, 17]. These type of solar cells can be categorised on whether they are produced using monocrystalline, poly (multi) crystalline silicon, or gallium arsenide (GaAs) [1, 3].

Wafer Production Methods

To date, the most efficient silicon solar cells are those made from monocrystalline material [6, 10]. The two most common methods used in producing silicon wafers are the Czochralski and float zone processes [1, 8]. Both the Czochralski and float zone processes are fairly expensive but have the advantage of producing high quality electronic grade silicon crystals [1] in the form of ingots. During the crystal growth process, the silicon is usually doped p-type by the addition of boron before the silicon ingot is cut into wafers by sawing [30]. The wafers have thicknesses in the range of 230-250 μm [3].

Polycrystalline silicon wafers are produced by the controlled casting of molten crystalline Si into cube shaped ingots which exhibit a polycrystalline structure. These ingots are then cut into thin square wafers [1, 12]. Compared to monocrystalline silicon wafers, which are usually circular, polycrystalline silicon wafers give the advantage of a higher packing density when making solar modules, and a higher utilization of the silicon materials [3]. However, at the cell level, polycrystalline cells are less efficient than monocrystalline silicon, due to charge recombination at the grain boundaries of the silicon material [12]. In order to optimize the power output from multicrystalline cells, larger sized grains with the proper orientation of the crystal structure are used, which allows light to penetrate deeper into the device, increasing its efficiency [1, 8].

In order to save costs and reduce wastage of the silicon source material, methods have been developed in order to go from the stage of having a silicon melt to the wafer state, in the form of ribbons or sheets, without the need for casting the silicon material as ingots. The main approach used is termed **edge-defined, film fed growth (EFG)** [1, 3, 30]. In EFG, a hollow, polygonal (usually 8-9 sided) tube of polycrystalline material is grown from a silicon melt using a carbon die of the desired shape. The hollow tube is then cut through using a laser, and flattened into sheets [1, 3, 30].

Cell Fabrication

Once the required silicon wafers have been fabricated using any of the methods described above, the solar cell is then fabricated. Figure 2.13 shows a schematic representation of the basic design of a crystalline solar cell. In order to create the p-n junction required for the material to function as a solar cell, an n-type dopant, e. g. phosphorous is allowed to diffuse into the wafer surface region by means of heating it in the presence of a phosphorous source. The wafer can also be doped by means of ion implantation, where ions are accelerated at energies high enough to allow them to penetrate beneath the surface of the semiconductor. The surface of the crystalline wafers is also etched to reduce its reflectivity and an anti-reflective coating, such as silicon nitride (Si_3Ni_4) or titania (TiO_2), is deposited onto the etched surface [8]. The anti-reflective coating serves to increase the amount of photons absorbed in the device [17]. Front and rear contacts are added to complete the device using metal particles suspended in a paste. In the earlier designs of silicon solar cells, aluminium was used as the rear contact. However, silver is the predominant material used today [17]. The most common means of applying these contacts is by screen printing. This has the advantage of being cheap; but this usually causes more of the area of the cell to be obscured, when compared to other deposition methods, and results in the degrading of the conductivity of the device [17]. After printing the antireflective coating and, the front and rear contacts, the paste is dried and fired.

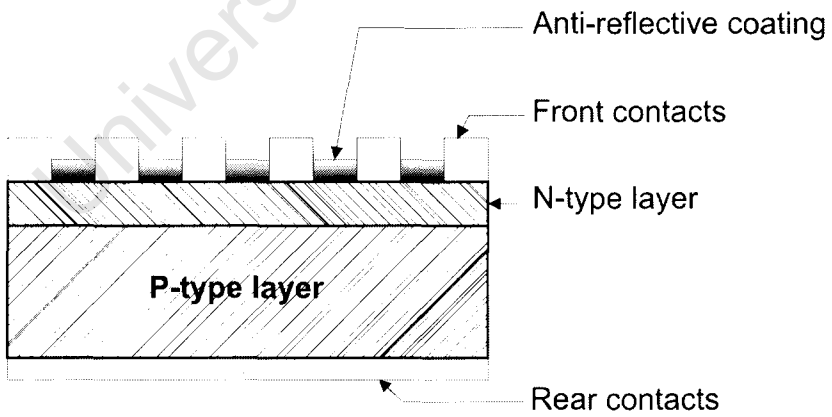


Figure 2.13: Structure of a typical crystalline solar cell.

Over recent years, various designs of solar cells based on crystalline silicon have been developed in order to boost efficiencies. These include black cells [8], passivated emitter cells (PESC) [31], rear point contact cells, buried contact cells [17], and passivated emitter, rear locally diffused

(PERL) [10] cells. These designs have produced solar cells with efficiencies ranging from 17-20%. Efficiencies of devices made from polycrystalline Si solar cells are in the order of 18% [6]. A novel approach in the fabrication of polycrystalline silicon PV cells is the creation of porous silicon layers on p-type monocrystalline Si wafers by means of electro-chemical etching [32].

Gallium Arsenide(GaAs)-based crystalline solar cells

Though silicon is the most widely used semiconductor in fabricating bulk crystalline solar cells, it is not the most ideal. One reason is due to its less than optimum energy band gap (1.1eV as opposed to 1.4eV) and, being an indirect band gap material, its absorption coefficient requires the PV cell to have a thick layer of silicon [3]. These, as well as other factors, such as temperature-dependent performance factors, have led to the exploration of the use of other semiconducting materials in producing wafers for making crystalline solar cells.

The most popular alternative crystalline semiconductor is gallium arsenide (GaAs), which has a similar crystal structure to silicon, and has been found to be the most suitable material for PV energy conversion [1, 8]. GaAs has a direct band gap of $\sim$1.42eV at room temperature and due to the closeness of this value to the theoretical optimum for PV conversion, a theoretical efficiency of 31% [33, 34]. GaAs has been used in producing a solar cell with an efficiency of 25.1% [8]. As it is a direct band gap material, the active layers for PV devices made using GaAs do not need to be as thick as those made using crystalline silicon as the active layer. Thus, the weight of the PV modules or arrays is greatly reduced in applications where weight is a priority [8]. GaAs has a better temperature coefficient than silicon and, as a result, performs better than silicon modules at high temperatures, under concentrated sunlight, and in space [1]. However, GaAs costs 5 to 10 times more than Si, which limits its use to extraterrestrial applications and in systems where cost is no object [1].

2.5.2 Thin Film Photovoltaics

In thin film photovoltaics, thin layers of the semiconductor material are deposited onto a substrate such as glass, plastic or foil. This leads to a significant reduction in production costs, as the thickness of the material is 100 to 1000 times less than the thickness of wafered crystalline Si material [17]. Thin film photovoltaics have the advantage of being able to deposit the semiconductor material over a large surface area, and offer the potential of fabricating connected modules during film deposition [8]. Solar cells made using thin film technology are usually referred to as

second generation solar cells.

The most common materials used as the active semiconductor layer in thin film solar cells are hydrogenated amorphous silicon (a-Si:H), cadmium telluride (CdTe), copper indium diselenide (CIS) and copper indium gallium diselenide (CIGS) [4]. In amorphous silicon, there is no long-range order in the structural arrangement of its atoms [29]. This leads to the formation of extra energy levels in the forbidden gap, making it difficult to dope the semiconductor, or to obtain high currents in a solar cell [35]. However, the addition of atomic hydrogen to amorphous silicon, to a level of 5-10%, saturates the dangling bonds and improves the quality of the material, enabling it to be used in the fabrication of thin film photovoltaic devices [35].

Deposition techniques and device fabrication methods

In fabricating thin film solar cells, the method of depositing the semiconducting layer and fabricating the solar cell is dependent on the properties of the semiconductor being used. The most common methods employed in the deposition of the semiconductor materials used in thin film solar cells are [4]:

i. Chemical Vapour Deposition (CVD),

ii. Sputter Deposition (SD),

iii. Plasma Enhanced Chemical Vapour Deposition (PECVD),

iv. Atomic Layer Epitaxy (ALE),

v. Evaporation, Multisource Deposition (MSD),

vi. Closed Space Sublimation (CSS),

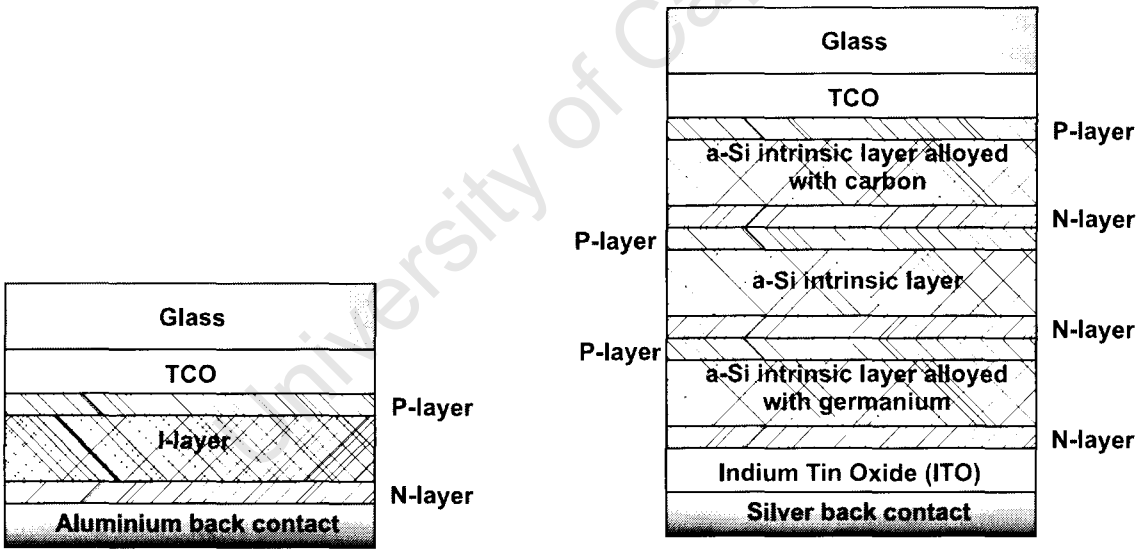
vii. Spray Pyrolysis (SPL),

viii. Electrodeposition (ED) and

ix. Chemical Bath Deposition (CBD).

Amorphous silicon is the most common semiconductor material used for thin films [17, 30]. Unlike crystalline and polycrystalline Si, amorphous Si does not possess any long range order in its crystal structure [36]. Compared to crystalline Si, it offers much better light absorption

and can be deposited at lower temperatures. Usually, amorphous silicon is deposited onto glass substrates using plasma enhanced chemical vapour deposition (PECVD), with silane (SiH_4) as the silicon precursor [4]. New methods such as hot wire CVD [25] have also been employed as deposition techniques. The substrate serves as a support structure for the active layers of the PV device. The substrate is transparent and coated with a transparent conducting oxide (TCO), usually indium-doped tin oxide (ITO), and also serves as an electrode for the device [4]. Due to its amorphous nature, the deposited silicon material has a lower electronic quality and exhibits poorer charge transport characteristics. In order to get around this, when designing cells made using *a*-Si:H, instead of the p-n homojunction used in most crystalline cells, a p-i-n structure is used. As shown in figure 2.14(a), a layer of intrinsic silicon is deposited between the p- and n-type silicon layers. In this structure, photocarriers are collected by drift rather than diffusion [30]. Thus, the i-region serves to aid the collection of photogenerated charge carriers, thereby boosting the performance of the cell [30].



(a) (b)

Figure 2.14: Structure of (a) an amorphous silicon solar cell and (b) a multijunction or tandem solar cell.

Variations of the solar cell design illustrated in figure 2.14(b) have been used in fabricating a-Si solar cells. This is referred to as the stacked or tandem solar cell [4, 30]. *a*-Si:H solar cells are most commonly used in hand-held calculators and other consumer electronic devices. In

general, the challenge involved in outdoor applications of a-Si:H based solar cells is the Staebler-Wronski effect, which is the reversible light induced performance degradation of the PV devices [4]. Reported efficiencies of solar cells made from a-Si are in the order of 13% [6].

Compound semiconductor materials, such as CdTe, CIS and CIGS can also be used to produce thin film solar cells. These semiconductor compounds produce more efficient solar cells [37] because they are direct band gap semiconductors [8, 30]. CdTe has a band gap of 1.44eV, very high optical absorption properties, and can be easily doped as either n- or p-type. It is usually utilised in a heterojunction cell structure with CdS as the n-side, and CdTe as the p-side of the junction [38] as shown in figure 2.15. The active layers are deposited using electrodeposition methods or chemical bath deposition [4, 39]. Development of cells using CdTe however, has faced opposition mainly due to the toxicity of the materials used which places stringent procedures on disposal methods [17]. Cells made using the CdS-CdTe structure have efficiencies in the order of 16.4%.

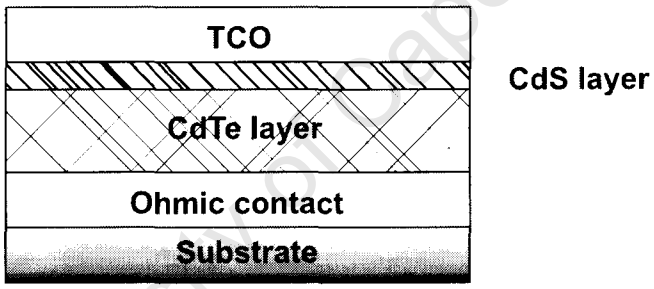


Figure 2.15: Device structure of a CdS-CdTe solar cell.

The most promising of the compound semiconductors used in fabricating PV cells are CIS and CIGS. Figure 2.16 shows the general design structure of CIGS solar cells. As in the case of CdTe, a heterojunction structure is used with CdS serving as the n-side of the junction [17, 39]. The heterojunction allows high energy photons to be collected efficiently due to the short diffusion lengths [8]. CIGS has been used in producing solar cells with efficiencies of up to 19% [6]. Another drawback to the widespread use of CdTe and CIGS in PV device fabrication apart from toxicity, is the relative scarcity of the materials which makes them more expensive than *a*-Si:H [4, 17].

Other thin-film technologies

Other thin film PV devices involve the use of microcrystalline Si, and are fabricated using similar techniques as those employed in polycrystalline Si preparation such as EFG [8]. The optical

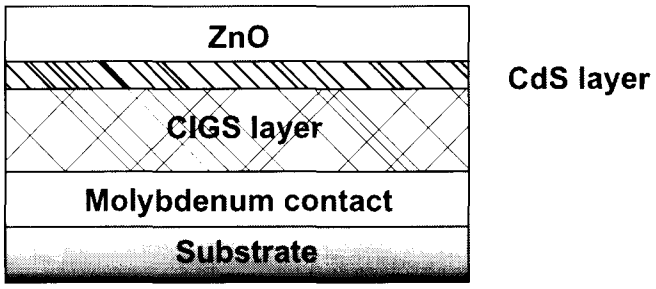


Figure 2.16: Device structure of a CdS-CIGS solar cell.

path length within the cell is increased using light trapping techniques, such as the stacked cell structure shown in figure 2.14(b) [12].

Another method referred to as "high temperature" deposition, is used in making thin-film solar cells from polycrystalline silicon [17]. In this method, the silicon material is deposited at high temperatures beyond 1000°C, onto a substrate [40]. Alternatively, the silicon material is first deposited and then either melted at temperatures around 1420°C [40] or recrystallised at intermediate temperatures to obtain the final thin film [17]. Other technologies include nanostructured PV cells, used to enhance the performance of cells based on thin film technology, and these include [41]:

- Quantum dot nanostructures, which engineer the band structure of Si based materials. This involves the fabrication of silicon nanocrystals embedded in an SiO_2 or Si_3N_4 matrix. When these quantum dots are sufficiently spaced, their overlapping wave functions result in a superlattice being formed, allowing a wide band gap to be generated.
- Hot carrier cells which are governed by the principle of slowing down the rate of photoexcited carrier cooling, due to phonon interactions in the superlattice.

2.5.3 Photoelectrochemical Cells

Unlike other types of solar cells discussed so far, photoelectrochemical cells exploit the PV effect at the junction between a semiconductor and an electrolyte. This is in line with Becquerel's photovoltaic experiment where devices used were liquid, and not solid based [1, 6]. The principle of operation has been discussed earlier in section 2.3.4. There are two main types of photoelectrochemical cells [6]:

- **Regenerative cells** which convert light to electrical energy without any chemical change in the cell. Conversion efficiencies of up to 19.6% have been reported for multijunction regenerative cells [6, 42].

- **Photosynthetic cells** which have two redox systems unlike in regenerative cells which have only one redox system. One redox system reacts with holes at the semiconductor surface while the second system reacts with electrons going into the counter electrode.

However, most promising photoelectrochemical cells with a suitable band gap are unstable against photocorrosion [6]. In order to circumvent this limitation, dye-sensitized solar cells have been developed [43]. Figure 2.17 shows a schematic diagram of a photoelectrochemical or Grätzel cell. The sensitizer dye has the effect of absorbing visible light to inject charge carriers into the semiconductor-electrolyte junction and produces a more stable device.

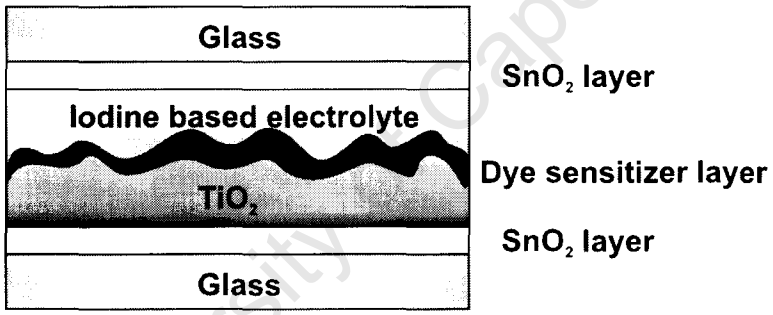


Figure 2.17: Design of a photoelectrochemical 'Grätzel' cell.

Different variations in the design of the electrochemical cell have been investigated such as nanocrystalline junctions and tandem cells [43, 44]. Dye sensitized nanostructured PV cells have reported efficiencies of up to 11% [6].

2.5.4 Other PV Technologies

Although solar cells made using wafer and thin film technologies dominate the PV industry, new methods and materials are being developed in the design and fabrication of solar cells. These technologies are generally referred to as *third generation* photovoltaics, and include polymer-based organic solar cells [45, 46, 47], and nanostructured photovoltaics [6, 41, 43]. Another approach to the production of solar cells involves the use of screen printing technology [48, 49].

Plastic (Organic) Solar Cells

Plastic solar cells are fabricated using semiconducting polymer materials. PV devices based on this technology are usually classified into two parts [47]: **Bulk Heterojunction (BHJ)** solar cells made from conjugated semiconducting polymers such as polyphenylenevinylene (PPV), (1-3-methoxycarbonyl) propyl-1-phenyl[6,6]C_{61}) (PCBM), poly(3-hexylthiophene) (P3HT), and their derivatives [50]. The other category of plastic solar cells is referred to as **bilayer heterojunction** structures and these are made using small organic molecules such as copper phthalocyanine (CuPc), tetracene and pentacene [47], in conjunction with buckminsterfullerene (C_{60}) molecules. The principle of operation of plastic solar cells is similar to that of inorganic solid state PV devices. A photon is absorbed by the semiconducting polymer material, leading to the formation of electron-hole pairs. The electron-hole pairs then diffuse within the material to a region within the device where charge separation takes place and the charge carriers are then collected by means of electrodes connected to the active material. In this case, conjugated polymers serve as electron donors while another material (usually a fullerene) serves as the acceptor material to form the active layer [46, 50]. Figure 2.18 shows the device structure of a BHJ organic solar cell.

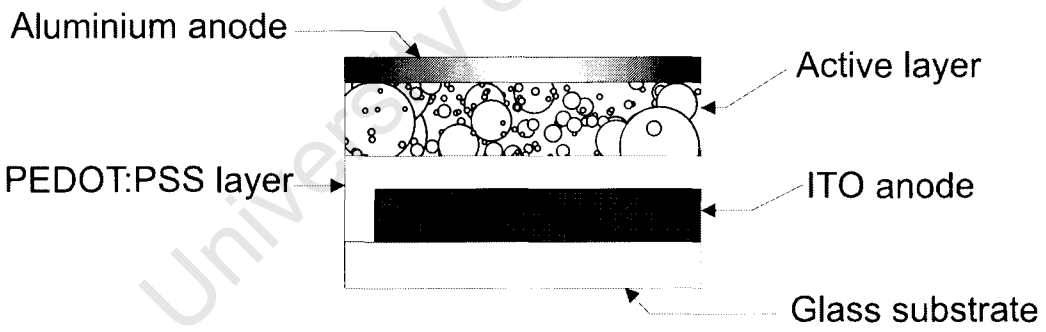


Figure 2.18: Device structure of a BHJ organic solar cell.

To fabricate the bulk heterojunction organic PV cell, the conducting polymer and fullerene material are blended together in solution. This polymer-fullerene blend is then deposited onto a glass substrate which had previously being coated with a transparent conducting layer of indium tin oxide (ITO). Thus, the substrate also serves as an electrode for the cell. The substrate is then coated with polyethylene-dioxythiophene, doped with polystyrenesulphonic acid (PEDOT:PSS). This PEDOT:PSS layer is used to improve the surface quality of the ITO electrode and boosting the hole injection/extraction within the device [50]. The deposition methods commonly used

include spin coating, doctor blading, screen printing and ink jet printing. After deposition of the active layer, the cathode is evaporated onto the active layer to form the "sandwich" structure illustrated in figure 2.18 above [47, 50]. The typical thickness of the devices is in the order of ~200 nm [46].

In the case of the bilayer heterojunction structure organic solar cells, the donor and acceptor layers are deposited sequentially by vacuum deposition techniques [47, 50]. The device structure is as shown in figure 2.19 below. The conducting substrate anode, and cathode are fabricated using techniques similar to those used in fabricating BHJ organic solar cells. Reported efficiencies for organic solar cells range from 2-6% [6, 47].

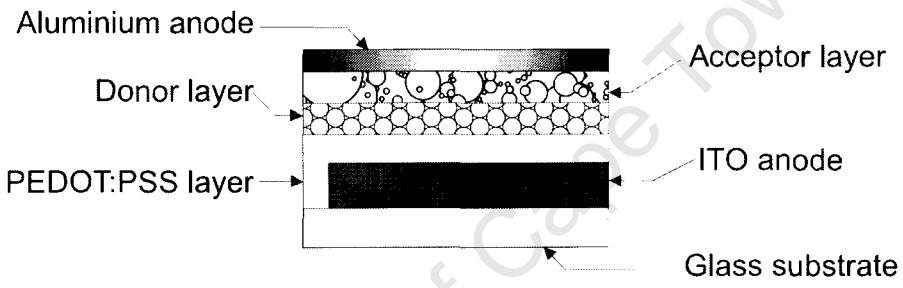


Figure 2.19: Device structure of a bilayer heterojunction organic solar cell.

Printed PV devices

As discussed earlier in this chapter, cost reduction is a major motivation in the development of novel PV materials, as well as new fabrication techniques. One of these approaches involves the use of screen printing in the fabrication of the PV device. In solar cell device fabrication, screen printing has been used in depositing metal contacts for crystalline solar cells [30] and dye sensitized solar cells [51]. Screen printing has also been used in depositing the active semiconducting layer in BHJ plastic solar cells [52]. Techniques have also been developed where silicon materials have been diffused into metal pastes via PECVD and then screen printed onto substrates in order to fabricate the PV device [49]. Screen printing has not been actively pursued as the *sole* deposition technique in the fabrication of solar cells. As a deposition technique, screen printing offers great savings in terms of cost and complexity, as it is a common method used in the microelectronics industry for fabricating electronic devices. The next chapters will discuss the experimental procedure used in fabricating the silicon solar cells using screen printing.

3. Nanoparticle Production

As mentioned in chapter 1, the focus of this thesis is to explore the possibility of fabricating a PV device, using nanoparticles, in a cost efficient way. In order to do this, a fabrication technique that allows the nanoparticles to be utilised has to be explored. The method used is screen printing, a technique already used in the electronics industry [52], in which inks containing the semiconducting nanoparticles are printed to form semiconducting layers. This chapter discusses the production methods used in synthesising nanoparticles in general, followed by a description of the particular experimental procedure used to produce the silicon nanoparticles and their characterisation.

3.1 Nanoparticle Production Methods

Nanomaterials are defined as those which have at least one of their dimensions in the order of 100 nm [53, 54]. The dimension may refer to the thickness of a layer in terms of layered (1-D) nanomaterials such as films and coatings [55]. 2-dimensional nanomaterials are those in which the width (or diameter) of the material is in nanometres, and examples include rod-like or filamentary nanomaterials such as carbon nanotubes and nanowires [55]. 3-dimensional nanomaterials have their dimensions in all directions in the order of nanometres and include nanoparticles, quantum dots, and hollow spheres [53].

Nanomaterials exhibit physical, mechanical and chemical characteristics which differ from those observed in their corresponding bulk form. Examples of the changed properties of nanomaterials include an increase in their mechanical strength, electrical resistance and specific heat [56]. These distinct properties of nanomaterials are due to their high surface-to-volume ratio, ultra-fine grain sizes and interface boundaries [56, 29].

Nanoparticles can be synthesized using methods that are generally classified into *bottom-up* and *top-down* processes. **Bottom up** syntheses involve the production of a material by building the nanostructure one atom, layer or cluster at a time. Thus, the bottom up approach is an additive process in which the final material is produced by the build up of smaller particles [57, 58]. On the other hand, **top-down** processes involve breaking down a bulk material into smaller units having dimensions of nanometers [55, 57, 58].

3.1.1 Bottom-up Synthesis

The techniques used in the bottom-up synthesis of nanomaterials can be generally classified into vapour- and liquid-state based methods. The most common of these are:

i. Physical vapour deposition (PVD) [58, 59] methods involving the production of a vapour of the desired material by means of thermal evaporation, laser beam ablation or ion sputtering. The most common PVD process for producing nanoparticles is **inert gas condensation**, which involves the production of nanoparticles using vapour from a precursor material. The precursor material is vaporised using electron beam heating, ion sputtering, laser or electron beam heating. The vaporization is carried out in a ultra high vacuum (UHV) chamber filled with a cooler inert gas, usually helium. Using the inert gas condensation technique, crystal sizes of a few nanometres, having narrow size distributions (2 - 25 nm) can be produced. Nanocrystals of aluminium and titanium oxide (TiO_2) have been produced using this technique. Other physical vapour deposition techniques operate on principles similar to inert gas condensation, and include laser ablation and sputtering, which are capable of vaporizing materials that cannot be readily evaporated by thermal means [60].

ii. Chemical vapour deposition (CVD) [56, 60], is a technique that uses a chemical reaction which results in the nucleation and growth of the nanoparticles. CVD is a common method for producing semiconductor nanoparticles and can be used in producing very fine particles having high purity. CVD is generally characterized as thermally activated, plasma-enhanced or laser-assisted. Thermally assisted CVD has been used in producing silicon carbide nanorods and silicon nanoparticles. Plasma enhanced CVD is utilised in producing silicon carbide (SiC) nanoparticles, silicon nanowires and carbon nanotubes [59]. Laser assisted CVD (laser pyrolysis) is used in synthesizing silicon, tungsten and silicon carbide nanoparticles.

iii. Wet chemical synthesis [56, 61] refers to processing techniques that synthesize nanoparticles by decomposition of chemical precursors, liquid phase chemical reduction, and the precipitation of solids from a supersaturated solution. Techniques based on wet chemical synthesis can be easily adapted to different materials, involve simple processes and utilise low cost precursors which are readily available. This method is used in producing silicon nanoparticles, metal nanoparticles, and chalcogenides [56]. However, the yield of silicon nanoparticles using this method is about 10% and the procedure is quite difficult

[62].

iv. Spray conversion processing [55, 63] is a process in which a precursor material is made into very small droplets which are dispersed very rapidly in a gaseous medium. The atomized droplets (or aerosols) then move into a heated reactor, where they form nanoparticles by means of evaporation or combustion. The most commonly used form of this technique is spray pyrolysis, which has been used in producing metal oxide nanoparticles like zinc oxide and aluminium oxide [56].

v. Other bottom-up processes include

a. *Sol-gel* [53] processes which involve the use of colloidal suspensions to produce solid materials and viscous gels. It requires the hydrolysis of molecular precursor materials, which results in the formation of oxides or hydroxide networks. This is followed by condensation and polymerization reactions. The polymerization of the precursor material is followed by the growth of the nanoparticles which then link up to form a chain that solidifies into a gel. Sol-gel processes are used in the production of nanosized ceramics [56].

b. *Electrodeposition* [61], in which nanoparticles are deposited unto a surface of a material by means of electrophoresis. The electrodeposition technique is governed by the materials used as the electrodes, as well as the electrolyte [59].

3.1.2 Top-down Synthesis

While the majority of bottom-up synthesis methods are fairly common, and tend to produce highly pure nanomaterials, a large amount of nanoparticles cannot be produced at a time [54]. In the top-down approach however, it is possible to synthesize commercial quantities of nanoparticles fairly cheaply [57, 56]. The top-down approaches used in producing nanostructured materials include *lithographic* and *machining* techniques [61]. Lithographic processes involve the formation of a nanostructure on a substrate using methods similar to those employed in the photographic industry [53, 61], and are used in the fabrication of two dimensional nanostructures. Machining allows three dimensional patterns to be formed, mainly using focused ion beams [61]. Lithography and machining are commonly used in fabricating nanoelectronics and devices [53, 61]. For the synthesis of *nanoparticles* however, the most common top-down technique used is mechanical milling [58, 56, 59].

3.1.3 Mechanical Milling

Mechanical milling is a process in which a bulk material can be reduced to very small grain sizes of nanometre dimensions, by means of the impartation of energy in a mechanical mill [57]. The bulk material is subjected to repeated grinding in a protected atmosphere using mills such as attritor, vibrating ball, and shaker mills. In mechanical milling, the bulk material to be milled is made up of a *single* constituent. On the other hand, mechanical alloying and mechanochemical synthesis start off with *blended or mixed* constituents which are ground into smaller nanoparticles [53, 59]. Mechanochemical synthesis involves the utilisation of mechanical milling as a means of catalysing chemical reactions to produce nanoparticles [64]. Thus, as the bulk material is being broken down into smaller grain sizes, chemical reactions can occur that will result in the formation of nanoparticles. In order to obtain the desired nanoparticles, the chemical reactants and precursor materials are selected as required. The major advantage of mechanochemical synthesis lies in the possibility of forming separated nanoparticles in a solid matrix. Metal, oxide, carbonate and sulphide nanoparticles have been synthesized using this technique [64].

Milling is governed by the principle of energy impartation to the bulk material as the milling media impact each other. The material (usually of micron dimensions) to be crushed, is placed in a mill which contains media used in crushing the material to smaller sizes. These media are generally termed 'milling balls' or 'pestles' and may be spherical or cylindrical in shape [57]. As the mill vibrates rigorously, the particles collide with each other and also with the milling device, resulting in their being crushed into smaller sized grains. This grinding can be as a result of the particles colliding with each other, or by the impact of the milling media (ball or pestle), or between the walls of the mill and the pestles [57]. The size reduction process is divided into two stages. The first stage involves the rearrangement of particles as they hammer and grind against each other, without causing a great deal of deformation or fracture. In the second stage, fracture and cleavage occur, leading to plastic deformation of the particles as they are crushed in the mill. It is possible to obtain higher energy forces in the milling procedure by means of high frequencies and low vibrational amplitudes [53]. This high energy milling results in a further refinement in the size of the particles to nanometre scale. Types of milling devices used in producing nanoparticles include shaker mills, planetary mills, and attritor mills. The basic principle involved in milling in these different types of mills remains the same, but the differences lie mainly with the operation, capacity and efficiency of the mill [57, 61].

The sizes of milled particles have been found to decrease with milling time until a limiting value is reached [65, 66]. This limiting value of the size of the material scales inversely with its melting

temperature [56]. Current studies also suggest that by reducing the milling temperature, smaller grain sizes can be achieved [65]. This has led to a development of a novel milling process referred to as *cryomilling*, where liquid nitrogen is used in cooling the milling environment [66]. The size of milled particles could also be controlled by the milling procedure (i.e. continuous or discontinuous milling), the sizes of the milling balls, milling temperature, and milling speed [59]. Milling offers the advantage of being able to produce nanoparticles from a wide variety of materials including composites, alloys, compounds and elements. The main disadvantage of the milling technique is the high probability of contamination of samples by the milling atmosphere, or by the equipment used in milling (especially in the case of ball mills made from iron). Milling also does not offer great control over the size distribution of the particles produced [53].

3.2 Experimental Milling Procedure

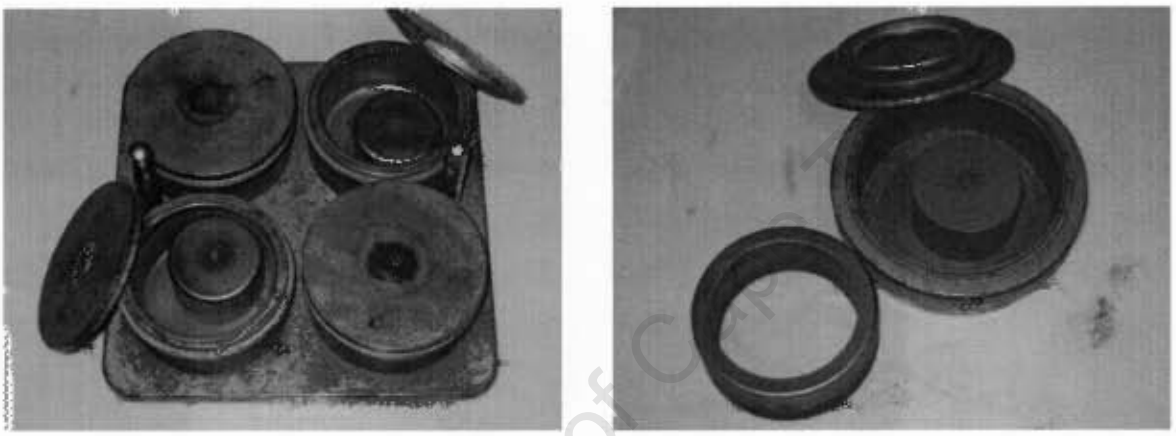
The experimental procedure followed in the fabrication of solar cells required the production of nanoparticulate silicon powders. In order to obtain a high volume of powders and due to its relatively cheap costs, availability, and simplicity of operation, mechanical milling was selected as the method of synthesis. The milling was carried out by means of mechanical attrition in an orbital pulverizer. The experimental procedure followed in the milling of powders is described in this section.

Materials

The selected semiconductor was silicon due to its availability, and relatively cheap cost when compared with other semiconductor materials used in the PV industry. Three types of silicon feedstock were used. Monocrystalline n and p type silicon wafers were obtained commercially from Siltronix, Archamps, France. The silicon wafers were in the form of 1-5 inch diameter wafers made via the Czochralski crystal pulling process and single-side polished (SSP). The n-type silicon wafers were phosphorous doped, (100) and (111) oriented with a resistivity $>$ 10 Ωcm, per the manufacturer's specifications. P-type silicon wafers were boron doped, had orientations of (100) and (111) as well, but with resistivities ranging from 0.005 to 0.007 Ωcm. Bulk 2503 grade metallurgical silicon was provided by Silicon Smelters (Pty) Ltd, Polokwane, South Africa. According to manufacture's specifications, the material purity was 99.4% with the major impurities being iron and aluminium with concentrations of 0.21% and 0.144% respectively.

Milling

An 800W Siebtechnik laboratory orbital disc pulverizer was used in the milling of the nanoparticles. The mill had sets of pots (or mortars) containing 52100 chrome steel pestles as shown in figure 3.1. In the case of the n- and p-type wafers, a four pot milling station was used. In the case of the metallurgical grade silicon, a single pot was used which was capable of milling up to 50 g of the material in a single milling cycle.



(a) (b)

Figure 3.1: Photographs of (a) a four pot milling station and (b) single pot milling station used in the pulverization of the silicon feedstock.

The operation of the mill involved the orbital motion of the milling pots, which resulted in the movement of the pestles in both rotational and lateral directions. Thus, the bulk material was subjected to repeated grinding due to the impact of the pestles and the walls of the milling pot.

Wafer Milling

Once the raw materials had been obtained from the commercial suppliers, the desired quantities of the n- and p-type wafers to be milled were weighed out using a Vibra AFR220E electronic balance, and then stored in paper envelopes. The mortars (or pots) and pestles were first cleaned by milling a small quantity of fine quartz sand for a period of about 10 mins. This was carried out in order to remove any potential solid contaminants. The pots were then emptied, cleaned and rinsed in turn using water, acetone and ethanol. At each stage of the cleaning process, the

mortars and pestles were blow dried using a high pressure stream of air. This was to avoid any particles being left in the mortar.

After cleaning was completed, the wafers were then placed in each pot in predetermined amounts. When milling the n-type wafers, only n-type material was placed in the four pots. After being placed in the pots, the wafers were then broken into fragments of millimetre dimensions, using the pestles and then covered with their respective lids. The pots were labelled 1 - 4. Once this had been done, the station was then placed in the pulverizer (see figure 3.2) and the machine lid closed. Milling was carried out for 5 hours. Precautions were taken during milling to avoid overheating of the machine, and potential loss of the milled materials by checking on the machine at regular intervals, and milling in cycles of 1 hour with 30 minute breaks after each cycle.

Figure 3.2: Photograph of a single pot containing the silicon feedstock, clamped into place in the mill.

Once milling was completed, the powder was allowed to cool overnight before being transferred into plastic storage containers. Before milling the p-type wafers, the same rigorous cleaning procedure was repeated and the same milling process carried out. Each milling run yielded approximately 80 g of powder.

Metallurgical Silicon

In the case of the metallurgical silicon, the same cleaning procedure described above was carried out. However, a single pestle and mortar set, as shown in figures 3.1 and 3.2, was used, and only about 50 g of powder was milled per run. In all cases, the work area was kept as clean as possible by wiping with a clean paper towel and ethanol. Instruments used, like stainless steel spatulas, were cleaned properly with acetone and ethanol before and after being used in powder transfer. The milled metallurgical silicon particles were also stored in properly labelled plastic containers.

3.3 Microscopy

Scanning electron microscopy was carried out on the milled silicon powders. This was in order to be able to characterize the nanoparticles with regard to their size and other physical characteristics. The nanopowders were prepared for scanning electron microscopy by the production of pellets of the silicon nanoparticles, which were then mounted in a Leica Stereoscan S440i scanning electron microscope. Intrinsic silicon, nanophase powders obtained from MTI Corp., Richmond, California, USA, were also characterised for comparison with the milled powders. The intrinsic silicon powder was to be used in the formation of the intrinsic silicon layer in the devices to be produced. The particles were produced by means of laser pyrolysis of pure silane and the average particle size was of the order of 50 nm. The purity of the material was specified by the manufacturer to be >98% and hence, was taken to be intrinsic type silicon.

Experimental Results

Images obtained from the scanning electron microscope, as shown in figures 3.3 and 3.6, were analysed using Image J, a free image analysis software.

To determine the average particle size distribution, line scans of the micrographs were used in producing plot profiles of the particles as shown in figure 3.4. The width of each peak was then determined for each plot, and the data used in producing a histogram as shown in figure 3.5. This was then used to determine the average particle size distribution.

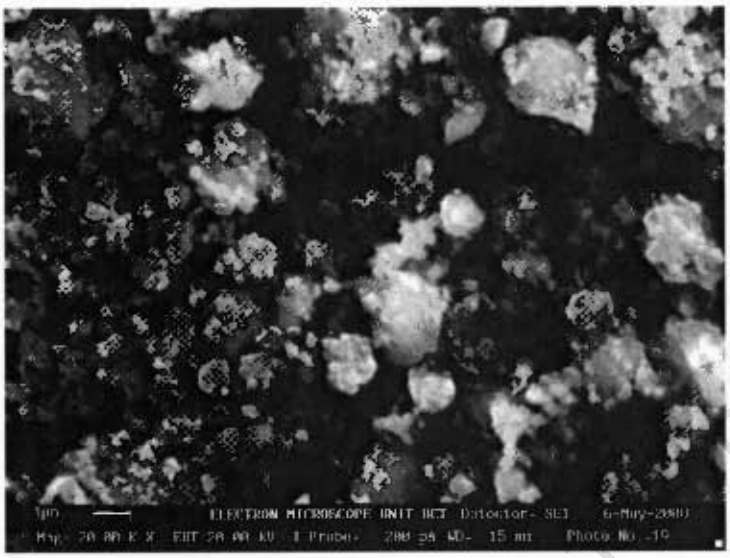


Figure 3.3: Scanning electron micrograph of the milled metallurgical silicon nanoparticles.

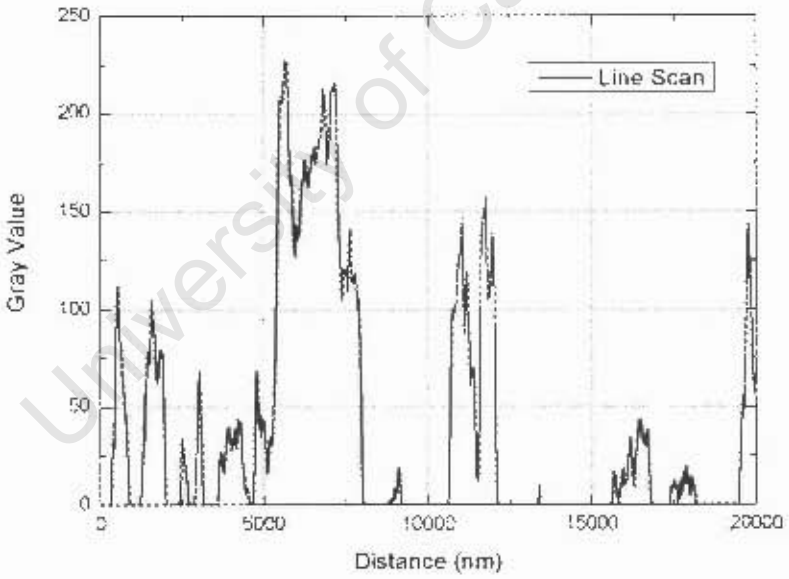


Figure 3.4: Typical line scan plot profile for metallurgical silicon.

The metallurgical silicon nanoparticles had irregular shapes, which were roughly spheroidal. From a higher magnification image as shown in figure 3.6, it was observed that the silicon nanoparticles tended to agglomerate into clusters of sizes in the order of 1.7 ± 0.8 μm. The particles had a non-uniform size distribution with average particle sizes of 115 ±3 nm.

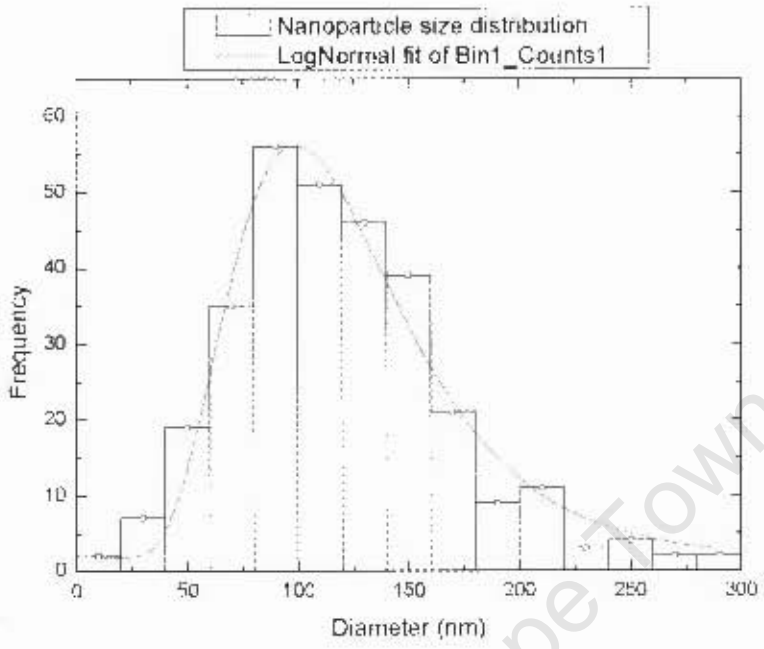


Figure 3.5: Histogram of the nanoparticle size distribution.

Figure 3.6: Images of the 5hr milled metallurgical silicon powder.

The milled n- and p-type silicon nanopowders are also spheroidal, and exhibited a similar clustering phenomenon observed in the metallurgical silicon powders. The average particle size for the n-Si powder was 215±86 nm, while the p-type silicon powders had an average particle size of 190⊥73

nm. Figures 3.7 and 3.8 are scanning electron micrographs taken of the n- and p-type silicon nanopowders.

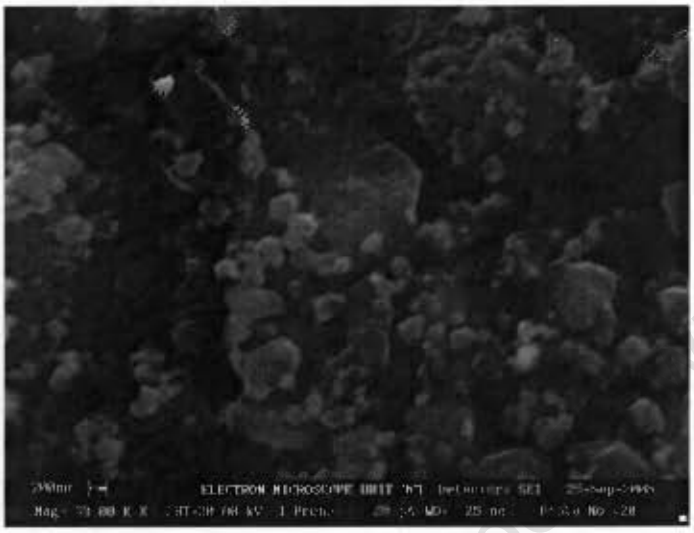


Figure 3.7: Scanning electron micrograph of 5 hr milled n Si powders

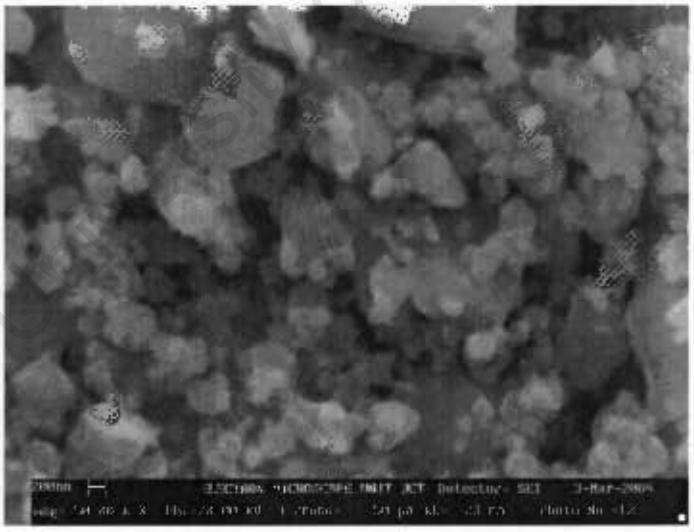


Figure 3.8: Scanning electron micrograph of 5 hr milled p-Si powders.

The intrinsic silicon nanopowder had a fairly uniform size distribution and an average particle size of 80±15 nm. The intrinsic nanopowders were of a more regular spherical shape. Shown in figure 3.9 is a micrograph taken of the intrinsic silicon nanopowder. At higher magnifications, individual particle features could not be clearly distinguished using the scanning electron microscope.

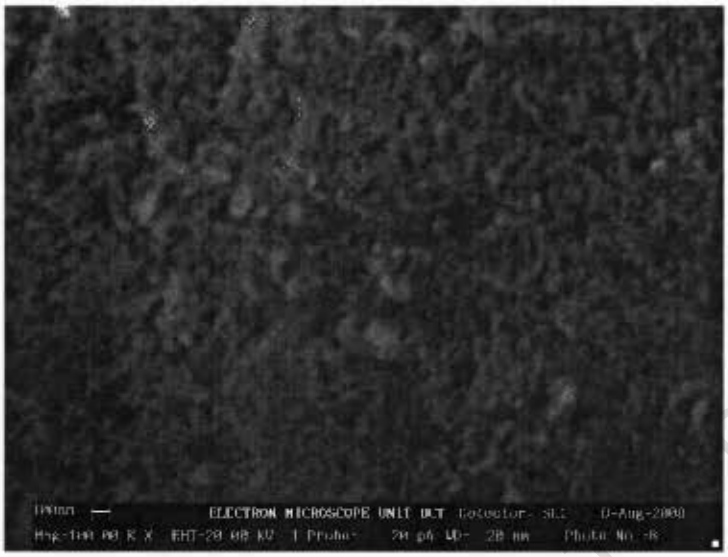


Figure 3.9: Scanning electron micrograph of the commercial intrinsic silicon nanopowder.

The inability to clearly distinguish between individual intrinsic silicon nanoparticles was due to the preparation procedure, as the high pressures used in compacting the powders into pellets resulted in their agglomeration. The results obtained however, are not inconsistent with the manufacturer's specification of 50 : 10 nm.

4. Ink Preparation and Printing of Nanoparticulate Silicon Layers

This chapter discusses the process of ink making and screen printing technology. The experimental procedure followed in producing inks using the nanoparticles produced, as described in chapter 3, and the printing of the PV devices is discussed. Results obtained from contact angle measurements of inks prepared, and optical and scanning electron microscopy of the printed layers produced, are also presented.

4.1 Printing of Electronic Devices

Printing has been used in the production of newspapers, graphic designs, and a host of other media that are used in today's world. Printing technologies have also been used in the production of electronic devices [67, 68]. A **printed circuit** is defined as a predetermined electrical circuit made by means of printing, or the formation of an electrically conducting pattern onto a substrate [69]. The printed pattern may be electrical components, or an interconnecting path between components that have already been fabricated. In general, most printing technologies (see figure 4.1) can be classified into [70, 71]

i. *Raised, relief or typographic* printing, in which the ink is deposited onto the raised surface of a printing plate, which forms the pattern, while the lower regions of the surface are not printed upon.

ii. *Planographic or planar* printing techniques, where the ink is deposited onto a flat or planar surface. In this technique, the surface of the substrate is specially treated so that the ink adheres only to the regions where the print pattern is desired.

iii. *Depressed or intaglio* printing. In this technique, the surface of a printing plate contains depressions that correspond to the desired print pattern. Ink is then applied to the plate and the surface of the plate is then scraped to remove any excess ink. The pattern is then transferred onto a substrate from the plate, by means of applied pressure.

iv. *Stencil based* printing technologies. In this method, the surface of the substrate is covered with a stencil bearing the print design. Ink is then applied onto this stencil and

forced through, by means of an applied pressure. The print pattern is formed only in regions that are not covered by the stencil.

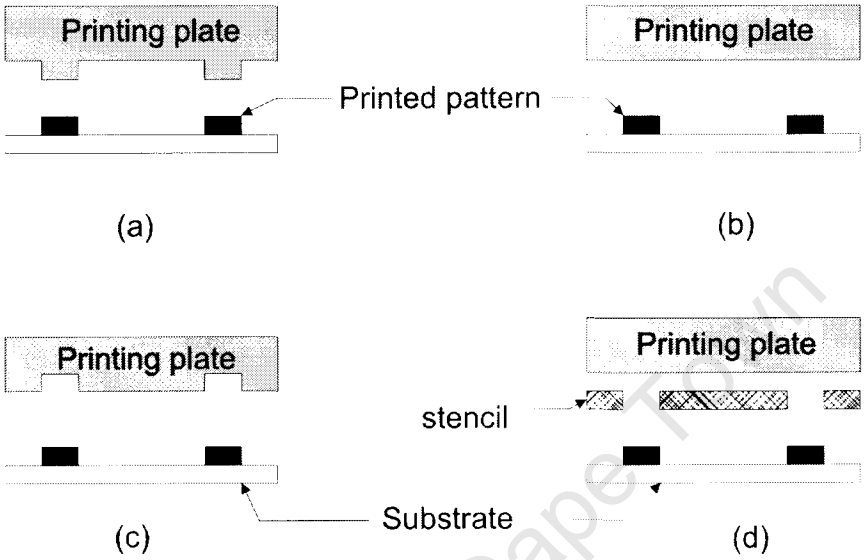


Figure 4.1: Diagram illustrating the different printing techniques: (a) Raised or relief, (b) Planographic, (c) Intaglio, and (d) Stencil-based printing.

Thick film electronics refers to the fabrication of passive electronic components by means of techniques such as screen printing [67, 69]. Devices fabricated by means of thick film technology require post processing techniques such as sintering, annealing and laser scribing before the final device is completed [67, 68]. Other common techniques used in thick film technology include spraying and stamping [69].

Printed electronics however, refers to the fabrication of electronic devices in which all components are fabricated by printing onto substrates such as paper and plastic, with minimal post processing procedures [72, 73]. It is an *additive* process, where the final device is obtained by the deposition of each component, layer by layer.

In recent times, new printing techniques have been used, especially in the field of organic electronics [74]. Some of these methods are mainly modifications of the techniques used in the electronics industry, adapted to new systems and substrates. The most widely used of these techniques are inkjet printing, thermal transfer printing, and microcontact printing [75]. In **inkjet printing**, the electronic devices are fabricated by depositing inks onto substrates, forming the device pattern, by means of ejection through a nozzle [75]. The deposition process can be in the form of the continuous spraying of the ink, or on a drop-by-drop basis [75, 76]. This method of printing of

electronic devices is limited by challenges in its reproducibility, uniformity of deposited layers, and the inks that can be used [75].

Thermal transfer printing, is a technique in which the material to be printed is first of all formed as a film on a stamp or donor substrate [74, 77]. The stamp is then placed in contact with the device substrate; a process referred to as 'dry printing' [74]. In thermal transfer printing, the donor substrate is heated selectively with a laser beam, which then results in the heated regions of the film adhering to the substrate in the desired electronic device pattern, before the stamp is then lifted off [74, 77]. Thermal transfer printing has been used in fabricating transistors made from carbon nanotubes, and silicon wires, onto both rigid and flexible substrates [74, 77].

Microcontact printing is a technique which is similar to rubber stamping [75, 78]. The ink to be printed is deposited onto the surface of a rubber stamp which bears the print pattern of the device. The pattern is then transferred onto a substrate from the stamp, by bringing the stamp into contact with the substrate for less than $\sim$0.5 s under pressure [74, 75]. A modified version of this technique, called *nanotransfer printing* or *nanoimprint lithography*, has been used to fabricate nanoelectronic devices [78, 79].

In PV cells, screen printing has mainly been used for metal contact deposition [30] and has, in recent times, being used as the sole method of metal deposition for PV cells on glass and plastic substrates [51, 52]. It has been shown that nanoparticulate silicon composites can be printed on paper substrates as well [48]. In novel PV devices such as plastic and organic solar cells, the methods of microcontact printing, ink-jet printing, thermal transfer printing and screen printing have been used [74, 75]. Screen printing however, offers greater versatility and has been employed in one form or the other, not only in the fabrication of printed electronic devices in general, but also solar cells in particular [51, 52].

4.1.1 Screen Printing

Screen printing is a stencil based, thick film printing technique, in which a desired pattern is formed on a substrate by means of forcing an ink or paste through the open areas of a mesh reinforced stencil or screen [67]. Using this method, it is possible to make finely detailed circuit designs over small and large areas in a cheap and reliable manner [51, 69]. The thickness of the films obtained is greater than that from other methods such as inkjet printing, and is controllable [67]. Screen printing employs the use of a printing screen which is made up of a stretched fabric mesh, tautly attached to a frame. The screen mesh has open regions corresponding to the printed

pattern, while the rest of the mesh is blocked out.

The early methods of screen printing were developed by the Chinese for producing graphic designs and decorations about 2000 - 3000 years ago [67]. Silk was used as the screen mesh due to its resilience, and the fine diameters of its fibres, which were 5-10 μm in diameter [67]. With the advent of the Second World War, greater advances were made in screen printing technology as it was used in printing proximity fuses in mortar shells [51, 67]. After the war, the birth of the microelectronics industry led to further advances in printing technology with the development of printed circuit boards and integrated circuits. Screen printing has firmly established itself as a viable method for producing printed electronic circuitry and delivers high performance in terms of reliability, environmental friendliness, thermal constraints and economy [67]. This has led to its application in the PV industry [4, 17, 52].

The fundamental materials required in order to carry out screen printing are a substrate, an ink (or paste), a screen and a squeegee. Figure 4.2 shows a schematic diagram of the essential screen printing process. Figure 4.2(a) shows the set-up before the squeegee carries out the print stroke. In figure 4.2(b), the ink is forced through the print pattern by shear forces, with the screen making contact with the substrate at the point where the squeegee presses down on the screen. Figure 4.2(c) shows the screen returning to its previous state, and the print pattern formed on the substrate.

Screens

The printing screen consists of a piece of woven mesh, made from materials such as stainless steel, polyester and nylon, which has been stretched tautly and mounted onto a frame [67, 69]. The entire surface of the screen is blocked or filled out, and the only regions with open areas are those regions bearing the printed design (referred to as the stencil), which allow the ink to be forced through onto a substrate using a squeegee [67, 69]. Screens are made from different fabrics depending on the type of printing required. For printed electronics, the most common screens are stainless steel, phosphor bronze, nylon, and polyester monofilament materials. In general, monofilament fabrics are durable, do not absorb inks, have a greater open region for printing, and are most practical for precision printing [69].

The tension in the screen should be such that it will allow the screen to readily peel away from the surface of the substrate after a print stroke, and retain its previous tension without breaking [67]. Screens with incorrect tension settings will result in the poor registration of the print pattern

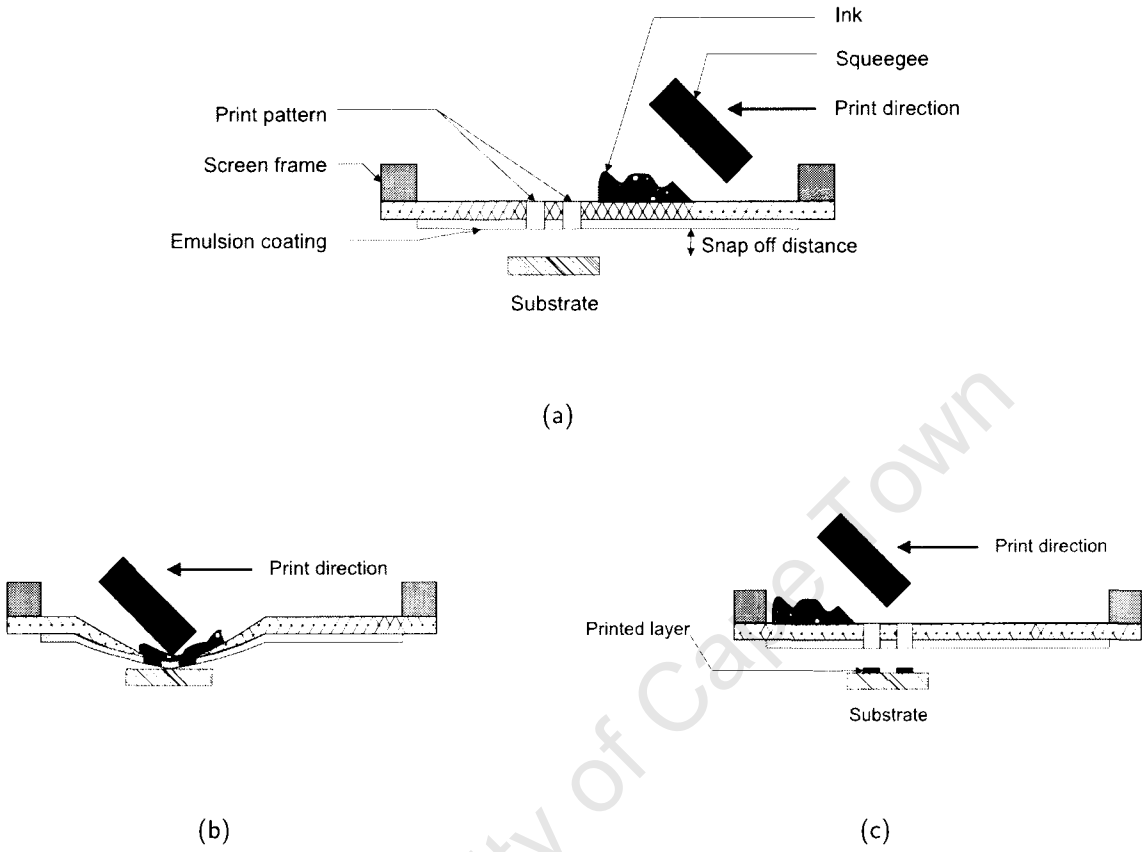


Figure 4.2: Principle of the screen printing process (a) before printing (b) during a print stroke, and (c) after completing a print stroke, after [67].

[69]. Most screens used in thick film electronic printing are coated with an emulsion which, in conjunction with other parameters, determines the thickness of the printed layer [67, 69]. Thus, the inks will only pass through the screen under the influence of shear forces. Printing is carried out in two modes: **on-** or **full contact** printing, in which the entire surface of the screen is in contact with the substrate when a print stroke is carried out; and **off-contact** printing, where the only region of the screen in contact with the substrate during a print stroke is at the point where the squeegee presses down on the screen, which is the most common method used in thick film printing [67, 69]. This means that, in off-contact printing, there is a slight gap between the screen and the surface of the substrate which is referred to as the *snap off distance* [67, 69]. Furthermore, in off contact printing, since the only part of the screen that comes in contact with the substrate is the point at which the squeegee pushes down, the screen fabric is restored to its original position after each impression, allowing the formation of very sharp print patterns [69].

Squeegees

The squeegee is a blade, usually made of polyurethane, which is used to press the screen into line contact with the substrate, push the printing ink through the stencil onto the substrate, and ensure the paste is level on top of the screen [67]. The required hardness of the squeegee is dependent on the nature of prints required. The 'angle of attack' refers to the angle at which the squeegee tip comes in contact with the printing ink when a print stroke is carried out as shown in figure 4.3 and, in order to get very good prints, is normally set to about 45° [67].

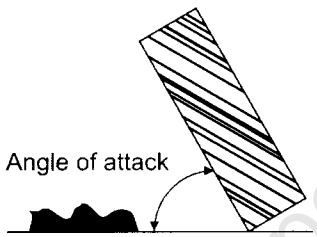


Figure 4.3: Diagram illustrating the angle of attack of a squeegee during the print stroke.

The two most common squeegee shapes used are the diamond and trailing edge sections as shown in figure 4.4 [67]. Due to its inherent flexibility, which allows it to print well on uneven substrates, the trailing edge squeegee is the most commonly used. It also exerts pressure uniformly on the surface of the screen, resulting in very uniform print thickness [67].

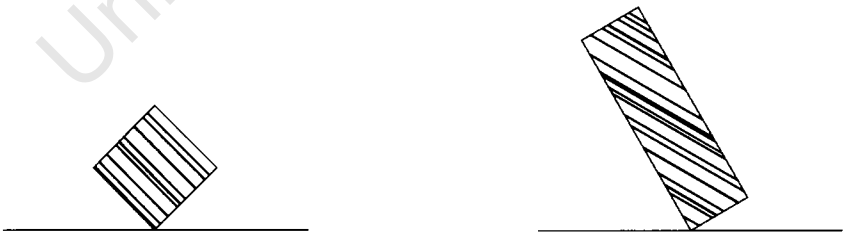


Figure 4.4: Common squeegee shapes used in screen printing for thick film electronics: (a) diamond edge squeegee and (b) trailing edge squeegee.

Modern printing machines are equipped with a flood bar for scooping up residual ink left on the screen after a print stroke. The components outlined above give the essential components used

in screen printing electronic devices. For best results, an automated print machine is used, which allows greater control over the print process, and enables various parameters such as squeegee speed, squeegee pressure, etc., to be varied in order to achieve best results in a reproducible manner.

Substrates

In printed electronics, the substrate refers to the material on which the desired circuit or electronic component is printed. Ceramic substrates are the most commonly used due to their high thermal conductivity, strength, stability and electrical properties [67]. Other substrates commonly used are glass and steatite [51, 52, 69]. Recent research has also explored the viability of the use of bond paper and plastic, as substrates for printed electronics [48, 75]. In general, the desired properties of substrates used in screen printing are as follows [67]:

i. Consistent surface properties.

ii. Good compatibility with the printed ink in order to form layers.

iii. Provision of a strong, stable support for the printed components.

iv. Reproducible characteristics when manufactured i.e. different batches of the same substrate should have the same properties and not differ significantly from one batch to the next.

The choice of substrate is, therefore, very important in screen printing, as the wrong choice could lead to undesirable performance characteristics of the printed device. In screen printing, it is also required that the substrate be clean and free from contaminants that might affect the performance of the printed device.

4.2 Inks

In general, thick film inks are viscous screen printing pastes which are made up of the material to be printed suspended in a suitable vehicle, which is usually a two-part organic material consisting of a volatile solvent and a binder [67, 69]. Inks can be made to desired specifications and compositions, depending on their application. The solvents used in ink preparation serve the

dual purpose of dissolving the binder, and adjusting the viscosity of the ink [69, 80]. The most common solvents used are ketones, acetones, alcohols, aromatics, and chlorinated solvents [69]. Common binder materials include vinyl resins, vegetable oils, and acrylic emulsions [48, 69]. It is possible to prepare screen printable inks from any desired material, as long as the parameters involved in the preparation can be optimized [48, 51]. The binder properties are important in the adhering properties, and quality of the printed layer, while the liquid solvent ensures that the ink is fluid enough to be printed [69].

The rheology of a material refers to its flow and deformation behaviour under an applied force [81, 82]. In order to determine, therefore, the rheological properties of an ink, it must be subjected to an applied stress, and its flow and deformation behaviour characterized [83]. If the shear stress τ, between two parallel planes of a liquid is proportional to its velocity gradient (or *shear rate*) $\dot{\gamma}$, the liquid is said to be Newtonian, and the relationship is described by [83, 84]

$$\tau = \eta\dot{\gamma} \quad , \tag{4.1}$$

where η is the coefficient of viscosity of the liquid. Hence, for Newtonian liquids, the viscosity is constant for a given temperature and pressure, and is independent of its shear stress and shear rate [84]. Due to their complex compositions and the addition of solid particles, inks, however, generally exhibit a non-Newtonian rheology [85] and their viscosity is dependent on their shear rate $\dot{\gamma}$ [83]. Viscoelasticity refers to the characteristics of an ink that lie between viscous and elastic and is a property of most screen printing inks [67, 83]. The behaviour of non-Newtonian fluids under shear stress can be either dependent or independent of time [83]. If a material becomes rapidly less viscous under the application of a shear stress, such behaviour is referred to as *shear thinning* and is independent of time [83]. On the other hand, if the liquid becomes rapidly more viscous under shear stress, such behaviour is referred to as *shear thickening* or *dilatancy* and is also independent of time [83]. *Thixotropy* is an example of shear thinning behaviour in a material, but which is dependent on time. The material regains its initial properties some time after the shear stress has been removed [82]. An example of a material that exhibits thixotropic behaviour is quicksand. The reverse scenario is referred to as *rheopexy*, in which the material thickens under a shear stress but regains its initial properties after some time has elapsed [82]. An example a material with rheopectic behaviour is whipped cream.

Surface tension is defined as the force that acts perpendicularly on a surface and acts inwards from the boundaries of that surface, with the effect of decreasing the area of the interface [83, 86]. It is also referred to as the *surface free energy*, and is defined as the work done per unit area in producing a new surface [83, 86]. In screen printing, the non-Newtonian behaviour and surface

tension of inks, are critical because they prevent the inks from passing through the open areas of the screen mesh, until the application of a controlled and repeatable external force from the squeegee blade [67]. The non-Newtonian behaviour of the inks also ensures that the printed ink settles and smooths out with a minimum amount of 'side flow' or 'edge slumping', and without the agglomeration of the suspended solid particles within the ink after a layer has been printed [67]. Hence, the screen printing ink must not only have the characteristic of being fluid enough so as to pass through the mesh apertures when forced through with the squeegee, but must also be capable of wetting the surface of the substrate, and adhering to it when the print stroke is completed. This property is determined by its surface tension [67, 80].

During the print stroke, each ink column must pull through the screen mesh without breaking apart, and leave only slight traces within the fabric of the screen. This, therefore, places the requirement that the ink must have the property of becoming rapidly less viscous when being forced through the mesh onto the substrate, and then regaining an intermediate level of its initial properties after printing has occurred [67]. The ink left on the screen must also regain an intermediate value of its viscosity after each print stroke, to ensure that the printed patterns are uniform for each print batch. The balance that must be obtained in the viscous and elastic properties of an ink can be expressed in terms of a *loss factor*, $\tan\delta$, given by [82]

$$\tan\delta = \frac{G''}{G'} \quad . \tag{4.2}$$

G'' is the *loss modulus* of the ink and it is a measure of how viscous the ink is, while G' is referred to as the *storage modulus* which is a measure of the elasticity of the ink [82]. Thus, there must be a balance between the storage and loss moduli of the ink, in order to have the desired viscoelastic properties.

The surface tension of the ink must be such that it exhibits greater adherence to the substrate than to the screen mesh, or no print will be formed and the mesh openings will become blocked [67]. Although the flow of the screen printing ink is generally characterised by its viscosity [83], the property of the ink that ensures that it does not flow through the screen mesh without an applied force is its interfacial tension [83, 87]. When the ink is placed on the screen prior to the print stroke, it spreads over the surface of the screen without adhering strongly to it. Once the print stroke is applied and the ink passes through the mesh, it then adheres to the substrate without remaining in the screen mesh. Thus, the interfacial tensions between the ink, substrate and screen are key parameters to be taken into account when preparing screen printing inks as these determine whether or not the print pattern will be formed after each print stroke [83, 87].

4.2.1 Ink Preparation

The binder material used in preparing the semiconductor inks was an acrylic screen printing base obtained commercially from Marchem (Pty) Ltd, Cape Town, South Africa. This was chosen as it is one of the most commonly used polymer binders in the screen printing industry [48]. As a solvent, 1-2-Propandiol (propylene glycol) obtained from Sigma-Aldrich Chemie GmbH, Stenheim, Germany was used. 1-2-Propandiol is a low volatility hygroscopic organic solvent, which serves as a means of controlling the fluid properties of the prepared ink mixtures. The inks were prepared at room temperature.

First, the preparation area and all apparatus to be used, such as spatulas and glass mixing bowls, were cleaned. Different binder-to-particle ratios were experimented with in order to achieve a balance between the amount of silicon nanoparticles, and binder concentration that would result in an ink that could be screen printed. A silicon particle loading of 80% by weight (as received) was decided upon in the ink formulation as this resulted in good printing results.

The required amount of silicon powder was transferred into a glass mixing bowl, and weighed using a Vibra AFR220E electronic balance. In the case of n-type, p-type and metallurgical grade silicon nanopowders, 10 ± 0.001g of powder was used for each preparation session. The proportional amount of binder material was then decanted into another glass bowl and weighed as well. Having weighed out the correct proportions for the ink formulation, the nanopowder was then added to the binder in very small quantities. The nanopowder was then stirred into the binder using a stainless steel spatula. The stirring was carried out vigorously until a smooth paste was obtained. The addition and stirring cycle was repeated until all the nanopowder had been added into the binder. Due to the larger volume of nanopowder compared to the binder material, the solvent was added at regular intervals whenever the paste became too thick for stirring. Table 4.2.1 shows the general binder to particle compositions and the corresponding amount of solvent used in ink preparation for each of the different nanopowders. .

silicon type	Mass of silicon (g)	Binder mass (g)	Solvent volume (ml)
P	10.0	2.50	4.10
N	10.0	2.50	5.00
M	10.0	2.50	6.60
I	2.0	0.50	3.80

Table 4.1: Quantity of the constituents used in preparing the nanoparticulate silicon inks. 'M' denotes metallurgical silicon.

Unlike the n, p and metallurgical type silicon nanopowders, the intrinsic silicon nanopowders had a much higher powder volume, thus a much smaller mass of powder was used in the ink preparation, with a proportionate reduction in the amount of binder used.

4.2.2 Contact Angle Measurements

As discussed earlier in section 4.2, the viscosity and surface tension of screen printing inks determine to a great degree, the printability of the ink. The quantities of ink prepared experimentally were insufficient for the viscosity to be determined using a viscometer. It was also observed that the commercial inks obtained for printing had wide differences in their observed viscosity but could be printed with similar results. In preparing the inks, after each formulation, a test run was carried out and it was also observed that although the viscosity of the ink was important, it was not the only parameter that determined the printability of the ink. It was therefore necessary to obtain another means of benchmarking the prepared inks, so as to have fairly uniform results between different batches of inks used in producing the printed semiconductor layers.

As mentioned earlier, the surface tension of the prepared nanoparticulate ink was found to be a key parameter in its printing performance. The surface tension of a liquid can be determined experimentally using the *maximum bubble pressure, ring* and *drop-weight* methods [83]. The surface tension of a liquid can also be determined by measuring its *contact angle* [86, 88]. When a liquid drop is placed in contact with a surface, it forms a meniscus, the shape of which is determined by its surface tension [83]. The contact angle θ, is defined as the angle formed by the meniscus of the ink drop and a flat surface as illustrated in figure 4.5 [83, 89].

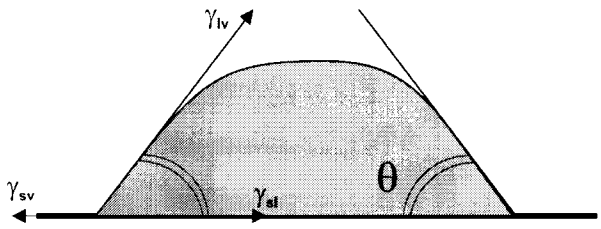


Figure 4.5: Diagram illustrating the contact angle of a drop of ink on a flat surface. θ is the contact angle.

Since the drop is in equilibrium, the forces are balanced so that [83, 90]

$$\gamma_{lv} \cos\theta = \gamma_{sv} - \gamma_{sl} \quad , \tag{4.3}$$

where $\gamma_{sv}, \gamma_{sl}, \gamma_{lv}$ are the solid-vapour surface tension, solid-liquid interfacial tension, and liquid-vapour surface tension respectively. Equation (4.3) is referred to as the Young-Dupré equation [83, 87], and the contact angle θ can thus be deduced from

$$\cos\theta = \frac{\gamma_{sv} - \gamma_{sl}}{\gamma_{lv}} \quad . \tag{4.4}$$

Using the relationship in equation (4.4) it is possible to benchmark the measured contact angle of a screen printing ink on a particular substrate to standard quantities, thus obtaining a reasonable comparison of the surface tension of the prepared inks. This enables the preparation of different batches of semiconducting inks having similar print qualities.

Depending on the experimental setup, the surface tension of a liquid can be determined from its contact angle, using techniques such as the tilted plate, Wilhelmy, and capillary rise methods [83]. In the *tilted plate* method, a flat solid plate is inserted into a liquid and its angle of inclination tilted until the liquid makes horizontal contact with the surface of the solid plate, and the angle can then be measured by using an optical interferometer and camera [83, 91]. In the *Wilhelmy plate* technique, a (usually) rectangular plate, suspended from a *Wilhelmy balance*, is immersed into the liquid [92] from where the contact angle can be determined. The surface tension γ, is deduced by using its relationship to the weight w, and contact angle θ of a given liquid given by [92, 93]

$$w = P\gamma\cos\theta \quad . \tag{4.5}$$

where P is the perimeter of the plate used. The *capillary rise* method uses the relationship between the capillary rise of a liquid in a tube to determine its surface tension [83]. In this work, the contact angle was determined using the *goniometer* technique [94], in which a drop of the liquid being investigated is placed on a flat surface. The contact angle between the *sessile* (or stationary) drop can then be determined visually using a protractor, or its image can be captured with a camera and the contact angle determined using image analysis software [94]. New techniques are being developed to determine the dynamic (rather than stationary) contact angles [91, 95, 96], a discussion of which is outside the scope of this thesis.

Contact Angle Measurement Procedure

An ink droplet was placed on a glass slide which had been cleaned using acetone and ethanol. Once this was done, the glass slide bearing the drop was then placed on a sample stage as shown in figure 4.6.

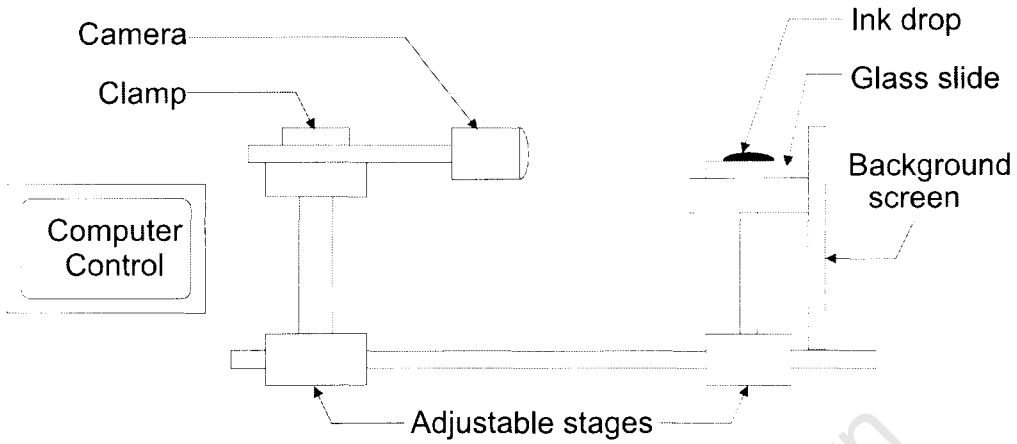
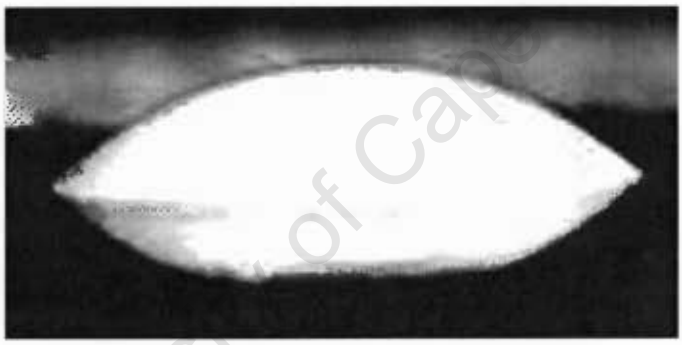


Figure 4.6: Experimental setup used in measuring the contact angle of inks.

The ink droplet was then viewed using a Logitech webcam having a resolution of up to 8 mega pixels. The camera was controlled by means of a laptop computer. The image was then brought into focus in one of two ways. The first means was by use of the adjustable stages which allowed the sample stage or camera to be moved as illustrated in figure 4.6. If a good focus was obtained, the image was then viewed at higher magnifications. The focus could then be further adjusted using the computer control of the webcam. Once a good image was obtained, photographs were taken. The measurement setup was also fitted with either a black or white background screen in order to obtain good contrast when taking photographs. Typical pictures of ink drops taken with the digital camera are shown in figure 4.7.

The photographs taken were analysed using a freely available image processing software (Image J) to determine the contact angles of the prepared inks. Once a batch of a semiconductor ink had been prepared, a test print run was carried out to observe its performance. Some batches of prepared ink were too 'thin', requiring several prints before a layer was properly printed, or too 'thick' which would result in the ink blocking the screen. From these tests, it was observed that very thick inks had high contact angle (i.e. $> 60°$), while an ink with good printable properties had contact angles in the range of $45 - 55°$. Thinner inks had contact angles below $45°$. Hence, by means of the contact angle measurements of the prepared inks, it was possible to ascertain to a reasonable level, the quality of prints to be expected before printing layers. This allowed the ink quality to be benchmarked, resulting in similar quality between different batches of inks.

(a)



(b)

Figure 4.7: Photographs of ink drops, in order to determine the contact angle between the drop and the glass slide. (a) shows a poorly printing ink while (b) shows a well printable ink.

4.3 Printing Procedure

The basic printing procedure for the PV devices was to deposit successive layers of silicon in rectangular strips, on printed silver contacts, to form heterojunctions.

Printing Materials and Equipment

The substrate material selected was plain 80 g/m^2 A4 paper. No special treatment was applied to the substrates except for general cleanliness and preventive cross-contamination procedures.

DuPont 5000 silver conducting ink was used for printing the metal contacts of the PV devices, and the top transparent conducting oxide layer was printed with DuPont Luxprint 7152E ink. The substrates, and commercial inks were used in their as-received condition. For printing, an ATMA AT-60PD Digital Electric Flat Screen Printer, shown in figure 4.8, was used. The printer was equipped with a flat vacuum bed to hold the substrate, and had a maximum print area of 40×60 cm^2, with a maximum screen frame size of 70×80 cm^2. A compressor was used as a supply of compressed air for the pneumatic and vacuum systems of the printer. Regions of the vacuum bed that were not covered by the substrate were blocked off using a cardboard mask. The printer had both manual and digital control settings, which facilitated good control over the printing process. Squeegee speed, off-contact, and print stroke settings were adjusted digitally while other settings such as the squeegee pressure, position of the substrate, and vacuum table, were adjusted manually by means of micrometer screws. The printing operation was fully automated, except for the application of ink onto the screen, and positioning the substrate on the print bed. The printer was also equipped with a flood bar for spreading residual ink between print strokes.

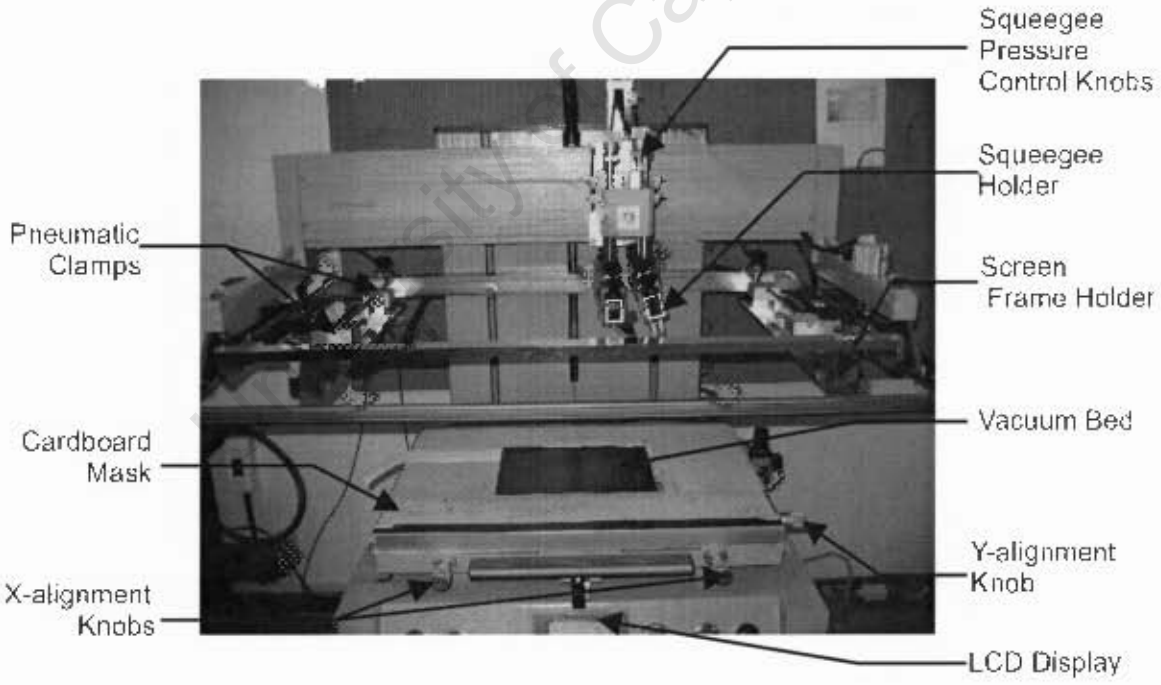


Figure 4.8: Photograph of the screen printer without the screen, indicating the important components.

Screens were made according to the design requirements, by Register Screen (Pty) Ltd, Cape Town, South Africa. The screens were made from a stretched polyester mesh of 150 lines/cm, and a fibre diameter of 31 μm. The tension of each screen was controlled within a range of 19

- 23 N.cm^{-1}. The sizes of the aluminium screen frames used were ~50×81 cm^2, with the print design stencilled on the mesh occupying an area of 10 cm^2. A typical screen used is shown in figure 4.9. When printing, the relevant screen was placed in the frame holder, and held firmly in position by pneumatic clamps.

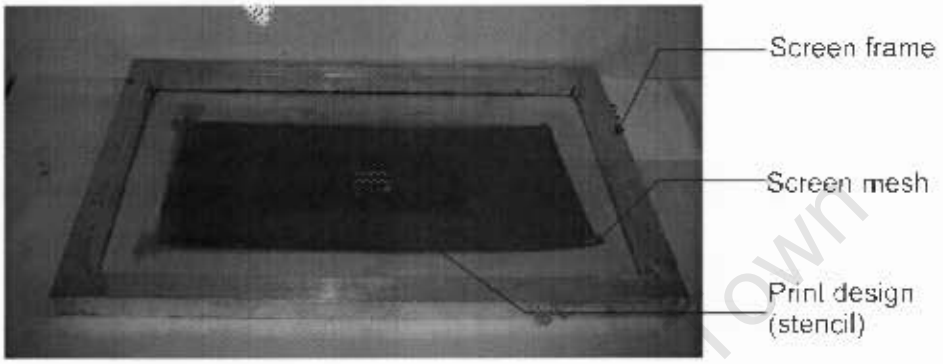


Figure 4.9: Typical screen used in the printing of layers. The darker regions are sealed and the ink is forced through the stencil pattern shown in the centre of the screen.

4.3.1 Printing of Layers

After the printer had been set up with the screen bearing the pattern of the layer to be printed clamped into place, the print pattern had to be registered to the substrate. *Registration* is a term used in printing to describe the process by which subsequent print layers are properly aligned, so that the final printed pattern will have all the layers printed in their proper positions. In order to carry out the registration of the screen to the substrate, a template was prepared as shown in figure 4.10, using the print pattern of the silver layer, printed using a commercial non-drying ink. The registration marks consisted of four cross hairs as shown in figure 4.10, with an additional five rectangular strips to the left hand side of the printed layers, and a scale bar, as shown in figure 4.10.

The screen with the design to be printed was lowered to a distance of approximately 0.1 mm above the template, and using the X- and Y-alignment screws of the vacuum table, the substrate was then moved into proper position. The four cross hairs were used in aligning the screen to ensure that the printed pattern would not be skewed or shifted. The cross hair patterns from subsequent layers had to be parallel to those from previous layers, overlapping with them within the desired tolerance of 0.1 mm. The rectangular strips provided rough information regarding the alignment

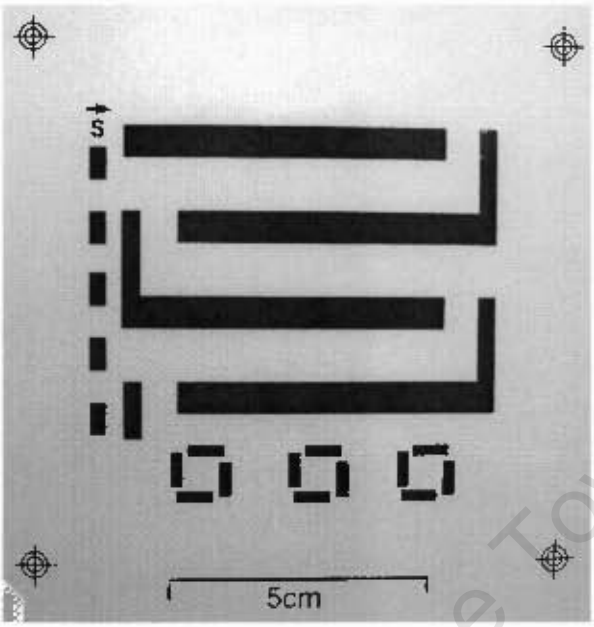


Figure 4.10: Photograph of the template used in the registration of subsequent prints.

of the printed layers in the x- and y-directions. As there were predetermined positions for each layer, once the rectangular strip for that layer was out of position, it immediately provided an indication of the adjustments necessary in order to get the screen into proper alignment. The scale bar was also used in a similar fashion to the cross hairs. Thus, with these three sets of registration marks, the different layers to be printed in the design of a device structure would be deposited in their proper positions. Once the substrate was registered to within the required tolerance, the screen was reset to its standby position, and then cleaned using ethanol and acetone. The squeegee and flood bar were also cleaned using ethanol and acetone. The print settings of the machine were then adjusted as required. Unlike in graphic printing where edge definition and coverage are of utmost importance [71], the thickness of printed layers of the PV devices has to be uniform over the entire area of the device, and consistent between different prints. To be able to achieve this consistency, the printer settings were adjusted after each print until reproducible prints were achieved. For the printing of the different layers of the device, the squeegee speed was set to 200 $mm.s^{-1}$, and the same setting was used for the flood bar. The snap-off distance was set to 0.1 mm.

The ink was then applied to the screen, just before the print pattern using a stainless steel spatula, in order to conserve ink. During a print cycle, the screen moves down from its standby position, stopping at the preset snap-off distance. The squeegee then carries out the required number of

print strokes. The number of strokes depended on both the required thickness of the layer to be printed, and the performance of the ink during printing. The printed layer was examined after the first print, and if the registration was poor, the registration was corrected until it was within the desired tolerance. Each printed layer was also inspected visually to check if there was sufficient coverage and if there were pinholes. Layers that did not meet the minimum quality desired were discarded. By repeating this process of inspection and benchmarking the silicon inks as discussed in section 4.2.2, it was possible to obtain a reasonable degree of consistency between the different batches of printed layers.

After trying out the different print modes of the machine that resulted in the printing of good quality layers, the following scheme was used:

i. When printing silver layers, a **double stroke, single print (DSSP)** was used. This means that the squeegee traverses the screen in two separate strokes, without the screen returning to the standby position. The first stroke deposits the first layer of ink before the flood bar spreads any ink residue. Still in position, the squeegee then applies a second coat of ink onto the previous layer. This process was carried out very quickly.

ii. For the silicon layers, the same mode was generally used as well. In some cases however, **single stroke**, **single stroke overprint (SSOP)**, or **double stroke overprint (DSOP)** was used. For a single stroke print, the squeegee performs only one print stroke on the screen, and then the screen returns to the standby position. For overprints, however, the print was carried out a *second* time before removing the substrate.

iii. In the case of the Luxprint 7152E ink, a **single stroke (SSSP)** was used. This was because it served as the top contact of the PV device, and was required to be as thin as possible in order to allow light penetration into the cell.

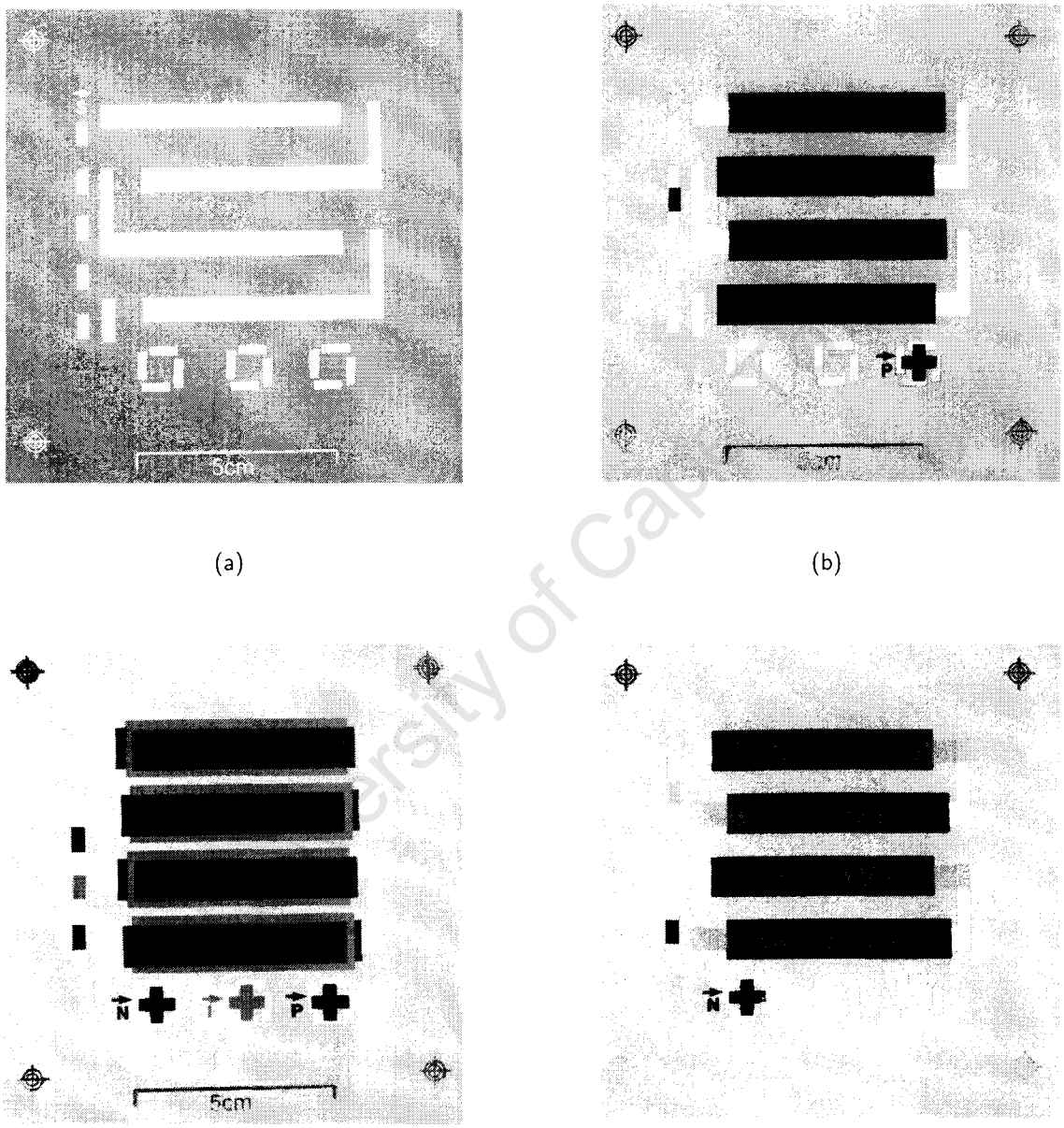
For the silver layers, it was observed under preliminary examination, that the layers appeared to have been printed well. The ink did not block the screen, and exhibited good thixotropic properties. When printing these layers, typically less than 2% of the layers had to be discarded. The silicon inks behaved in a markedly different manner to the silver ink. The metallurgical silicon inks were observed to be gritty when subjected to a shear force by the squeegee. This was most likely due to the presence of large clusters as discussed in section 3.3. These inks also exhibited shear thinning behaviour, without regaining their original properties once the shear force was removed. Thus, it was observed that the quality of the printed layers deteriorated as more layers were printed; typically after 15 to 20 prints. The edge definition of the printed layers was fairly

good, but pinholes sometimes appeared in the layers which suggested either a screen blockage or insufficient ink. If the screen was blocked, it was cleaned using acetone and ethanol before printing resumed with a fresh batch of ink. Typically, about 5% of the printed metallurgical silicon layers had to be discarded due to bad quality prints.

The n- and p-type silicon inks exhibited a similar behaviour to that of the metallurgical silicon inks. However, these inks were considerably less gritty due to their smaller cluster sizes as discussed in section 3.3. The n- and p-type silicon inks printed better than the metallurgical silicon ink, and the occurrence of pinholes or screen blockage was less frequent. The quality of the printed layers also appeared better when inspected, but was not as good as the silver layers. Pattern registration always presented a challenge, and so the amount of layers that had to be discarded was approximately the same as in the case of metallurgical silicon layers. The intrinsic silicon ink behaved differently to the other semiconductor inks. It was more fluid and very difficult to print, requiring several overprints before a good layer could be obtained. Only a few good layers could be printed before the ink quality deteriorated.

Differing results were obtained when printing different layer combinations. This required that the screen pressure, off contact, and squeegee speed settings had to be adjusted to obtain good printed layers. Printing a semiconductor layer directly on top of a silver layer usually produced relatively good results, except for the occasional appearance of pinholes within the printed semiconductor layer. The printing of semiconductor layers over each other presented a number of challenges. For example, if the bottom semiconductor layer was not properly dried, the surface of the layer could be damaged when another layer was printed on it. In extreme cases, the top surface of the bottom layer was lifted off onto the underside of the screen. Too high or too low squeegee pressure settings also resulted in a damaged bottom layer, or poor adhesion between the different semiconductor layers. Due to these challenges, a number of printed structures (15 - 20%) had to be discarded if they involved the printing of different layer combinations. The commercial TCO ink exhibited good thixotropic characteristics when printed. The ink produced good quality layers when printed directly onto the paper substrate with good edge definition. However, when deposited onto a semiconductor layer, the results obtained were different. The TCO layer would adhere to the semiconductor layer but the print machine settings had to be adjusted several times to avoid damaging the layer below, by either lowering the squeegee pressure or increasing the snap-off distance. Various combinations of the semiconductor layers were printed. As the printing was carried out on a layer by layer basis, each layer was allowed to dry for at least 24 hrs before another layer was deposited on top of it to avoid damaging the layers in subsequent overprints. The entire printing procedure was carried out at room temperature and about 500 structures were

printed using the different schemes described above. Figure 4.11 shows photographs of typical printed layers of different layer combinations, taken at different stages of the printing process.



(a) (b)

(c) (d)

Figure 4.11: (a) a printed silver layer, (b) printed p-type silicon layer on silver, (c) printed p-i-n layers, and (d) a TCO layer printed on an n-type silicon layer.

In all cases, silver was printed first as the back metal contact, and consisted of 'L' shaped strips,

as shown in figure 4.11(a). The longer section of the strips had an area of 6×60 mm^2. As discussed earlier, the cross hairs and the five rectangular strips served as the registration marks during printing. As the printing process described above was not completely automated, and required manual intervention when placing the substrate in place, not all prints were properly registered. However, within the tolerance of 0.1 mm, the majority of the printed layers were good enough for the deposition of more layers.

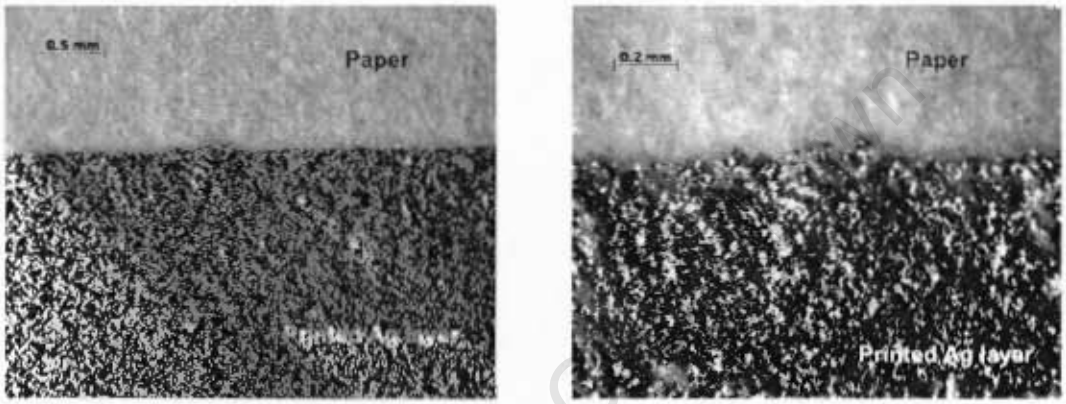
The p- and n-type silicon layers in the design of the printed solar cell consisted of four strips of dimensions 10×55 mm^2, shown in figure 4.11(b). As shown in figure 4.11(c), the middle intrinsic silicon layer was also rectangular, but had an area of 14×55 mm^2. The final layers to be printed were the transparent conducting oxide (TCO) layers which were rectangular strips of area 6×60 mm^2. A TCO layer printed on a n-type silicon semiconductor layer is shown in figure 5.1. Once printing was completed, the screen, squeegee and flood bar were cleaned with paper, acetone and ethanol, and the screen dismounted and stored. The storage area for the printed devices, and the general work area were kept as clean and free from contaminants as possible.

4.4 Morphology of Printed Layers

From the printed structures, samples were selected for optical and scanning electron microscopy in order to investigate their physical characteristics. A Wild Photomakroskop M400 optical microscope was used for optical microscopy, to investigate the quality of the printed layers, and obtain information about how the printed structures appeared when more than one layer was printed. Once the printed layers had dried, they were placed on the sample stage of the optical microscope and the top surface of the printed layers were examined. Optical micrographs were taken at magnifications of 6.5, 12.5, and 32 times.

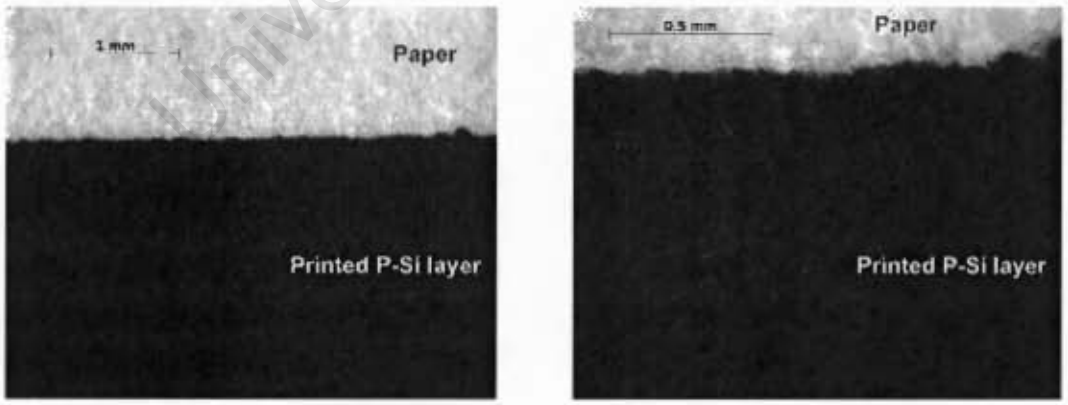
For scanning electron microscopy, a Leica Stereoscan S440i scanning electron microscope was used. The scanning electron microscope was used in the secondary electron mode, at an operating beam energy of 20 keV. The samples to be investigated were rectangular strips having dimensions of approximately 0.5×0.5 cm^2, cut from the printed layers using a stainless steel scalpel. The square strips were then mounted on aluminium stubs, using carbon glue to hold the samples in place. The surface of the samples were then coated with a thin film of gold palladium. After this, the stubs were mounted on a carousel, and placed on the sample stage of the scanning electron microscope, and micrographs were taken at magnifications of 100× and 6000×.

It was observed, using optical microscopy, that the printed silver layer had a fairly uniform surface roughness as shown in figure 4.12. The layers did not appear to have a relief pattern from the paper substrate. As the figure 4.12 shows, the edge definition of the printed silver layers was within the tolerance of 0.1 mm. Due to the design structure of the PV devices, this edge definition was acceptable, as the design of the PV cells did not require the printing of fine lines, which would have placed greater demands on the edge definition.



(a) (b)

Figure 4.12: Micrographs of a printed silver layer on a paper substrate at different magnifications.



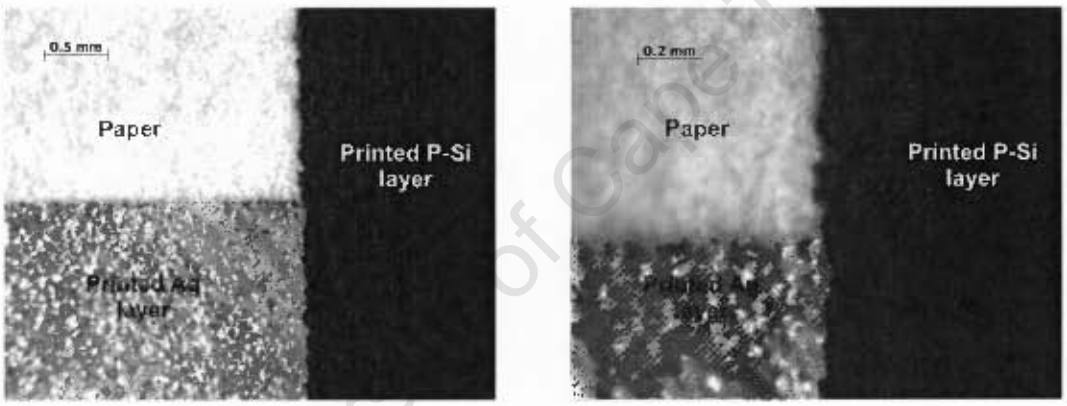
(a) (b)

Figure 4.13: Micrographs of a printed p-type silicon layer on a paper substrate at different magnifications.

The appearance of a printed p-type silicon layer was also investigated using the optical microscope.

Figure 4.13 shows pictures taken of such a layer at different magnifications. Unlike the silver layer, the surface of the p silicon layer was generally rough, with the appearance of ridge like structures on the surface of the layer. This ridge like pattern appeared to have been transferred from the screen mesh and not the paper substrate. The ridge like structure was not observed on the silver layer, probably due to the fact that the layer gave off a very strong reflection when viewed under the microscope, precluding the ability to properly discern surface features. Another reason might be because it was not present due to the difference in the rheologies of the silver and silicon inks. Pinholes also appeared within the printed layer but these were of negligible dimensions.

The quality of the edge definition between a p-type silicon layer, printed on a silver layer was also investigated and micrographs are presented in figure 4.14.

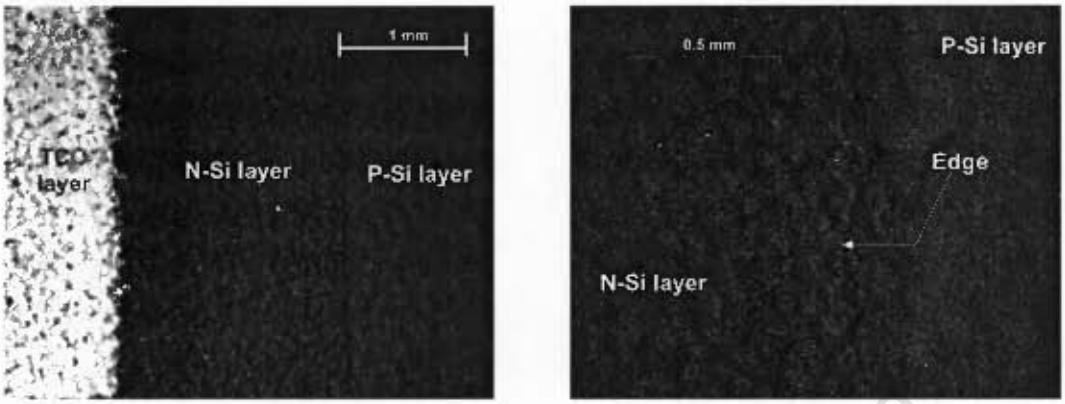


(a) (b)

Figure 4.14: Micrographs showing the edge definition of a p-type silicon layer, printed on a silver layer on a paper substrate at different magnifications.

As figure 4.14 shows, the p-type silicon layer printed well on the silver layer. It can be seen that the edge definition of the p-type silicon layer appears better on silver, than on paper. This is because the silver layer provided a much firmer surface for the p-type silicon layer to be printed on. The ridge like features still appeared across the entire p-type silicon layer, even for regions that were in contact only with the paper substrate. This would suggest that these features were more likely to have been transferred from the screen mesh rather than the paper substrate.

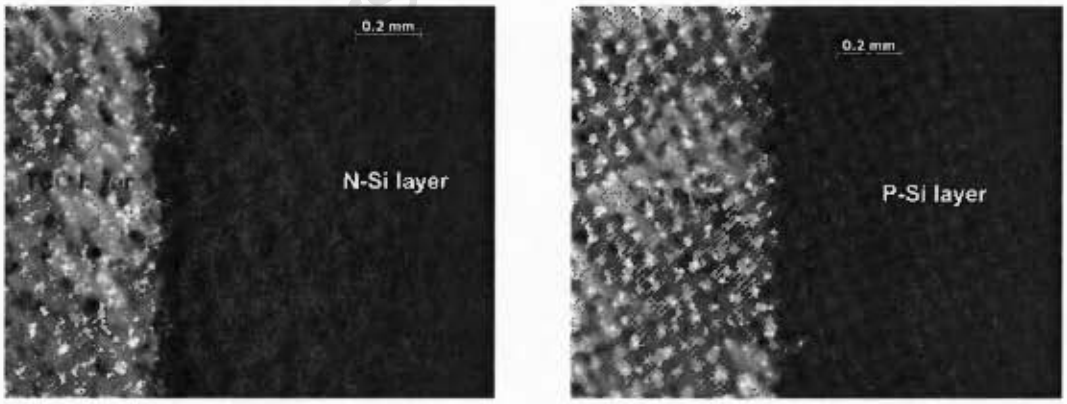
Figure 4.15 shows the quality of the edge definition of an n-type silicon layer printed on a p-type silicon layer. It can be seen that there is a clear separation between the two layers as indicated by the edge of the n-type silicon layer. However, the definition of this edge is not as previously



(a) (b)

Figure 4.15: Micrographs showing the edge definition of an n-type silicon layer, printed on a p-type silicon layer at different magnifications.

observed in figure 4.14. The edges appear more feathered, and may be as a result of the p-type silicon layer not providing a base as firm as the silver layer when printing successive layers. The ridge like pattern was also observed, and appears more pronounced on the n-type silicon layer than on the p-type silicon layer as shown in figure 4.15(b).



(a) (b)

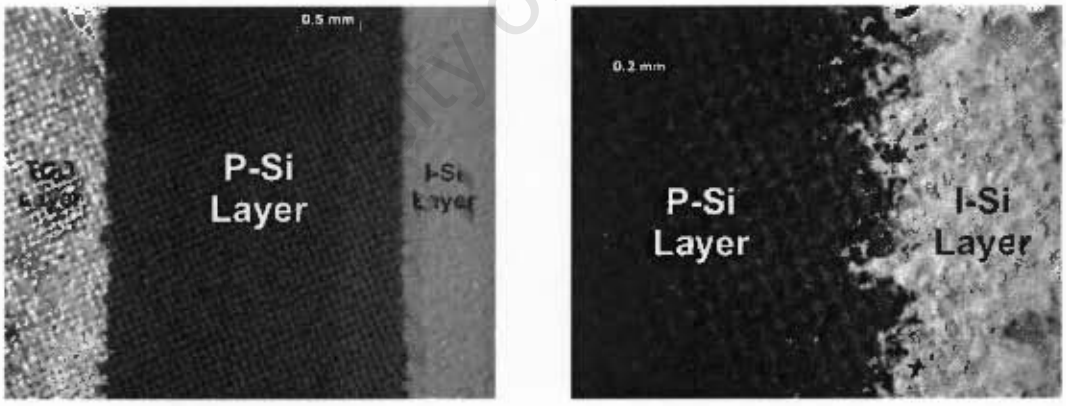
Figure 4.16: Micrographs of a TCO layer printed on (a) an n-type silicon layer and (b) p i-n silicon layers taken at similar magnifications.

The edges of the transparent conducting oxide (TCO) layer printed on two different types of

layer combinations were also investigated. The first structure consisted of a single n-type silicon layer, printed on a silver layer (SNO structure). The edges of the printed TCO layer and the n-type silicon layer were then investigated and a micrograph is presented in figure 4.16(a). It was observed that there was slight feathering at the edges between the two layers, but overall, the edge definition was acceptable and the TCO layer covered the entire layer below it, with the appearance of a few pinholes.

Figure 4.16(b) shows the appearance of the TCO layer printed on p-i-n silicon layers. In this case, the feathering at the edges of the TCO layer was more pronounced than in figure 4.16(a). The ridge like pattern that had been observed in previous layers investigated was also evident in the SNO structure (figure 4.16(a)), but is more pronounced and better defined in figure 4.16(b). Thus, the ridge like structure appears to have been transferred from the screen mesh, and was probably more defined in the case of figure 4.16(b) because of the presence of more layers between the top silicon layer and the bottom silver layer.

Figure 4.17 shows an optical micrograph of the top view of a printed p-i-n structure, with the silver layer as the back contact.



(a) (b)

Figure 4.17: Micrographs of (a) a TCO printed on p-type silicon and intrinsic silicon layers and (b) edge definition between the p-type and intrinsic silicon printed layers.

As discussed in section 4.3.1, each layer was deposited successively in an additive process described in section 4.3. At higher magnifications, the surface of the printed layer appeared relatively rough, as shown in figures 4.17(a) and 4.17(b). The printed layer had a surface morphology that was net-like due to the mesh pattern of the printing screen being transferred during printing. The

mesh pattern appeared uniform across all the layers suggesting that each subsequent layer that was printed formed a pattern taken from the previously printed layers.

From the top view, the layers were clearly defined, and were deposited uniformly on each other. At the edges, as shown in figure 4.17(b), the edges of each layer could be clearly seen. The edge definition between the intrinsic silicon and other silicon layers was not sharp but appeared more diffuse or feathered as compared to previous structures investigated. This was most likely as a result of the difference between the intrinsic and other silicon inks as described earlier in section 4.2.1. In order to obtain higher resolution images of the surface morphology of the printed devices, scanning electron micrographs of the device structure were also taken.

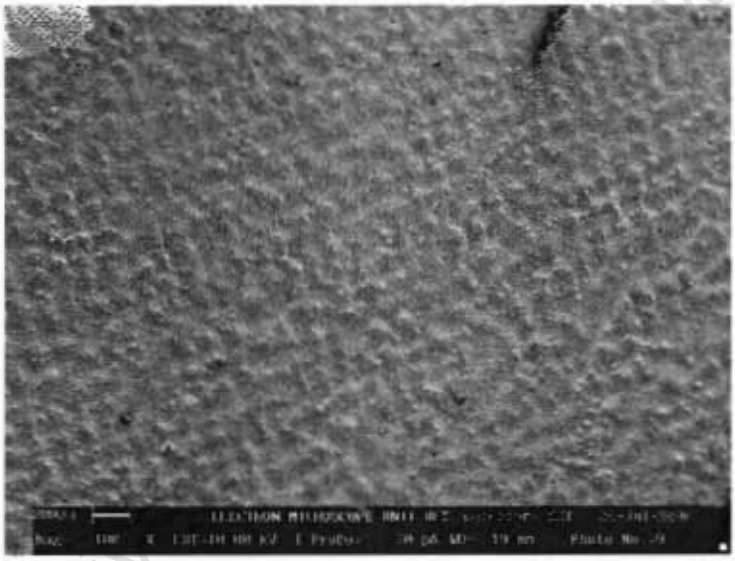


Figure 4.18: Scanning electron micrograph of the surface of a printed silicon layer.

Figure 4.18 shows the surface morphology of a printed silicon layer as viewed through the scanning electron microscope. The mesh pattern of the screen observed in optical microscopy, was also observed at this magnification as well. At a higher magnification, the structure of the printed nanoparticle clusters could be seen on the surface of the paper substrate as shown in figure 4.19. Individual nanoparticles had agglomerated into clusters and the printed layer was composed of tightly packed silicon particles.

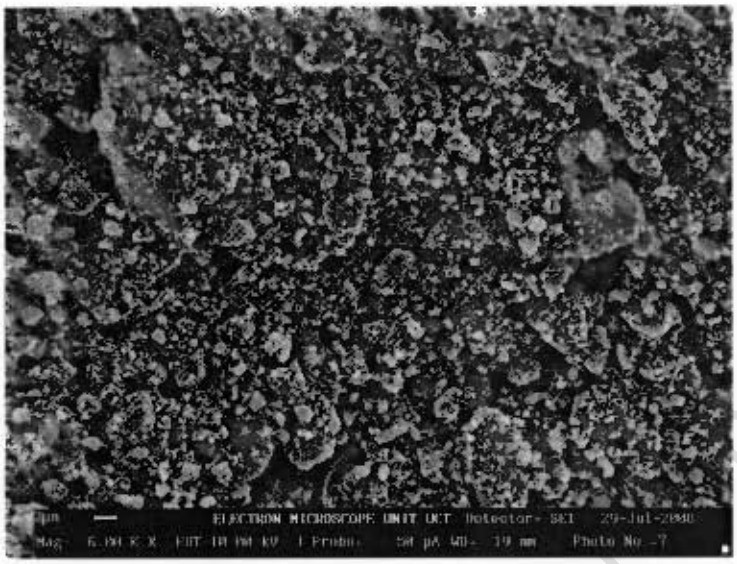


Figure 4.19: Higher magnification scanning electron micrograph of the printed silicon layer.

4.5 Internal Structure of Printed Layers

The cross sections of the printed layers were investigated using a Leica Stereoscan S440i scanning electron microscope, and micrographs were taken. This was carried out in order to analyse the thicknesses and internal structure of the printed layers, as well as to observe the interface between layers that had been printed on top of one another. The scanning electron microscope was used in the secondary electron mode, at an operating beam energy of 20 keV, and in order to obtain images with better contrasts between the various layers, the back scatter mode of scanning electron microscope was also used. Samples for cross sectional investigation were prepared using a Reichert Leica Ultracut S Microtome, shown in figure 4.20, equipped with a glass knife. The process involved first cutting out narrow rectangular strips using a clean stainless steel industrial blade. The strips were then placed in a mould containing epoxy resin. After this, the resin was cured at 100°C for 24 hrs in an oven. Figure 4.21 shows how the sample appeared when encased in the epoxy resin. The resin cast was then removed from the mould, and the region of the cast encasing the top most part of the sample was shaved off using the microtome. This was done so that the cross section of the printed layers could be viewed.

The glass knives were made using an LKB 7801 Knife Maker. To prepare the knives, a clean rectangular strip of glass was placed in the sample holder of the knife maker and clamped into place. The glass strips were then cut down into triangular shaped pieces as shown in figure 4.22.

Figure 4.20: Photograph of the microtome used in preparing samples.

Once the knives had been made, the resin cast containing the sample was placed in the sample holder of the microtome, and the process of shaving began.

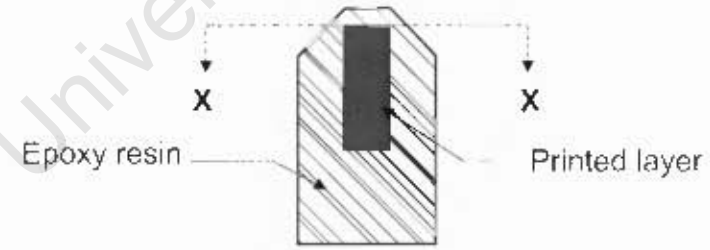


Figure 4.21: Schematic diagram of the sample prepared for cross-sectional scanning electron investigation. X-X is the direction of view.

Rough shaving was carried out using a stainless steel blade to remove regions of the resin surrounding the sample to reduce the amount of resin surrounding the sample, as shown in figure 4.23, thereby reducing the possibility of the knife becoming blunt. Once the rough shaving was completed, the knife edge was brought close to the edge of the resin cast and clamped into place, as shown schematically in figure 4.22. The sample was then moved in a continuous up and down

motion by means of a rotating handle.

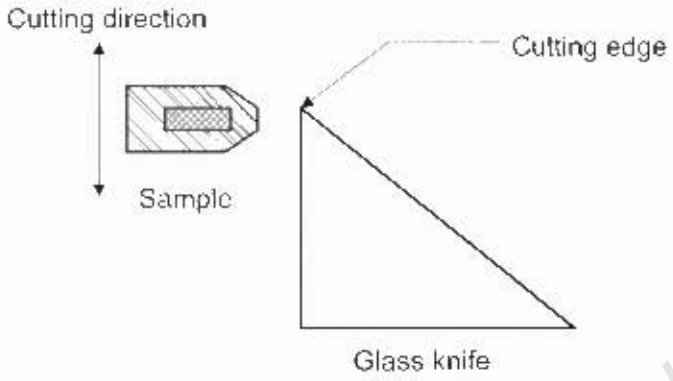


Figure 4.22: Schematic diagram of the glass cutting knife, illustrating how the epoxy cast encasing the sample would be cut.

As the sample moved up and down, the resin was shaved off in predetermined step sizes until the cross section of the printed layers could be seen under the microscope as shown in figure 4.23.

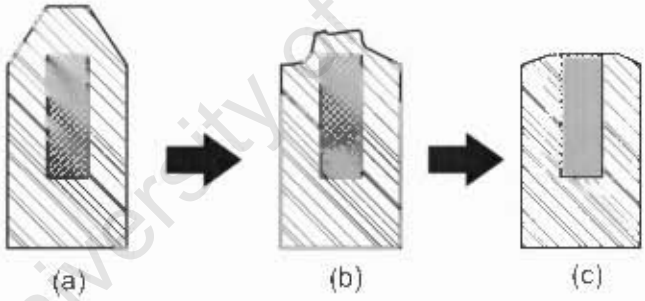


Figure 4.23: Diagram of the various stages of the cutting procedure,(a) before cutting, (b) after rough shaving, and (c) after fine shaving with the glass knife.

The direction of shaving relative to the printed layers differed. As shown in figure 4.24, one direction was across the printed layers while the second direction was along the layers. During the shaving process, it was observed that shaving across the printed layers resulted in the samples being damaged, and hence, the shaving direction was chosen to be along the printed layers.

The prepared samples were then placed perpendicularly on aluminium stubs using carbon glue, and coated with gold palladium as described earlier in section 4.4.

Figure 4.25 is a scanning electron micrograph of the cross section of a printed silicon layer. The micrograph was taken using the back scatter detector (QBSD) of the scanning electron

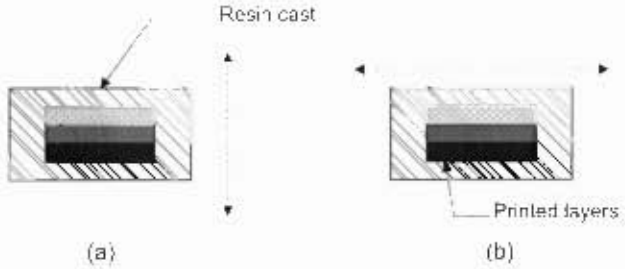


Figure 4.24: Diagram showing the shaving direction during sample preparation, (a) across the printed layers and (b) along the printed layers.

microscope. The silicon layer was deposited evenly over the paper substrate, and had a thickness of 14.5±1.0 μm. At higher resolutions, it was observed that the nanoparticles clustered together

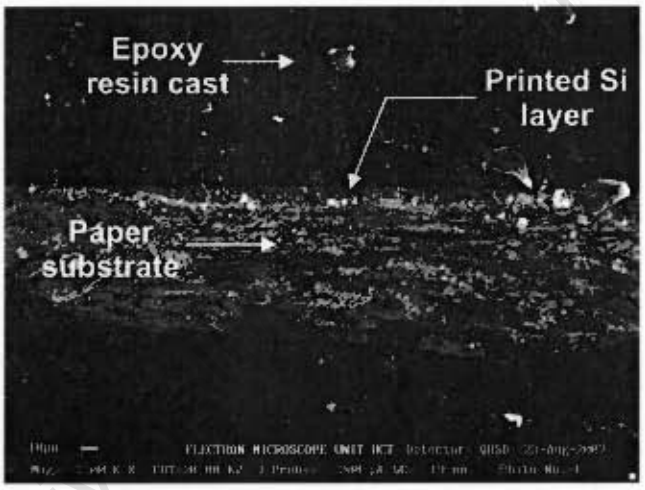


Figure 4.25: Scanning electron micrograph of the cross section of a printed layer taken using a QBSD detector

to form a layer over the substrate. This is shown in figure 4.26.

However, due to the process of shaving with the microtome as discussed earlier, some features of the samples were damaged as can be seen in figure 4.26. Another sample preparation method was used in which the layer structure was not damaged. The samples were prepared by cutting out rectangular strips from printed layers. Unlike the procedure described earlier, where the strips were encased in an epoxy resin cast, the samples were glued onto aluminium stubs in a perpendicular position without being cast in resin. The cross sections of these samples, for different layer combinations were then investigated with a scanning electron microscope as described earlier. Figure 4.27 show a p-type silicon layer printed on a paper substrate. The silicon layer had a thickness of 102.3±13.4 μm. Unlike the samples prepared using the microtome, the printed

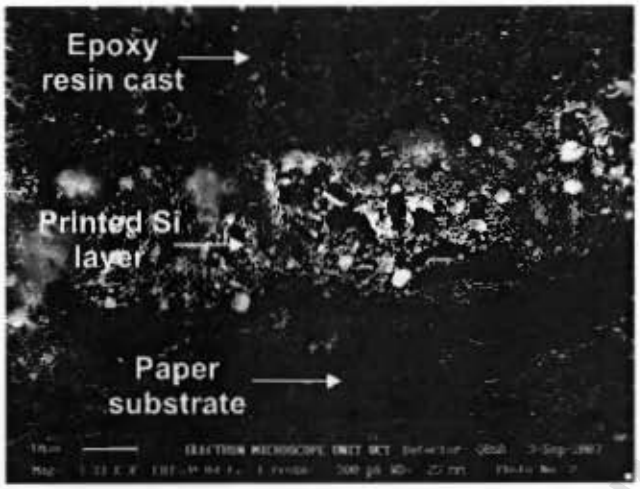


Figure 4.26: Higher magnification micrograph of the cross section of the printed device.

layers had thicker layers due to the difference in the pressure settings when the layers were printed, and the absence of the resin used in encasing the layers prepared using the microtome.

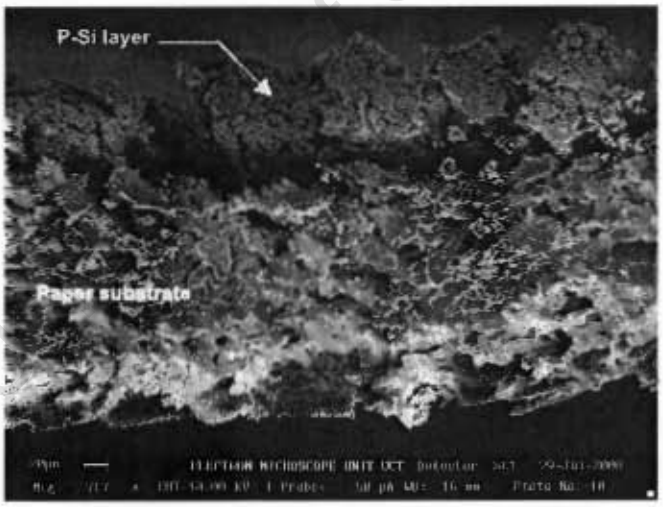


Figure 4.27: Cross-sectional image of a printed p-type silicon layer on a paper substrate.

The printed silicon layer had a wavy appearance, which was due to the mesh pattern observed when investigating the top view, thus agreeing with the previous observation described in section 4.4. Figure 4.28 shows a scanning electron micrograph of a printed silver layer, on which was printed an intrinsic silicon and then, a p-type silicon layer. The bottom silver contact had a layer thickness of 31.5 ± 3.1 μm, while the middle intrinsic silicon layer had a thickness of 61.8±7.4

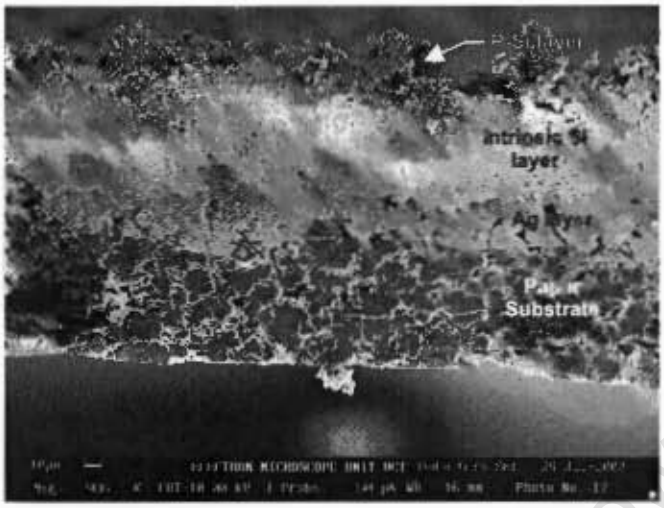


Figure 4.28: Scanning electron micrograph of a p-type and intrinsic silicon layer printed on silver with a paper substrate.

μm. The top layer of p-type silicon had a thickness of 32.1±8.7 μm.

For p-i-n printed layers, the different silicon layers could not be easily distinguished, and had a combined layer thickness of 35.8±5.1 μm as shown in figure 4.29. The printed silver layer had a thickness of 51.8±13.7 μm.

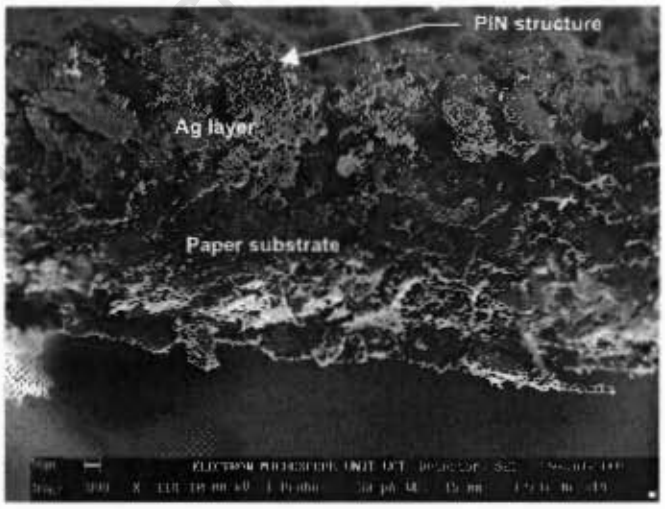


Figure 4.29: Cross sectional scanning electron microscope of a PIN layer printed on a silver contact

From the investigations of the layers made using both optical and scanning electron microscopy, it was observed that the use of screen printing as a technique for fabricating devices has much

promise. From the micrographs taken, it was observed that each layer of the final PV structure had been deposited as a continuous layer with very little inhomogeneity and provided a route for charge transport *across* the layers. The cross sectional views of the layers also showed that there was adhesion *between* different layers, providing the possibility of good electrical contact and charge transport from one layer to another.

5. Characterisation of Printed PV Devices

Using the nanoparticulate silicon inks developed in this work, solar modules were produced by screen printing on paper substrates. The device structure, as shown in figure 5.1, consisted of four individual cells connected end-to-end in series, to form a module. Also shown in figure 5.1 are a test structure used for other studies of the Hall effect, registration marks and, a scale bar as described in section 4.3.1.

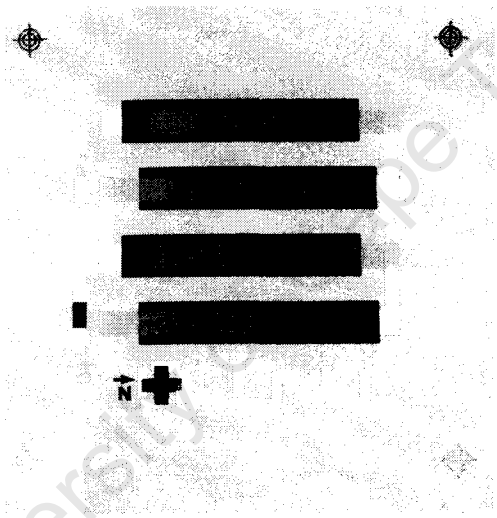


Figure 5.1: A typical printed device structure, in this case with n-type silicon as the active semiconducting layer.

The first layers of the solar module printed were silver base contacts, consisting of 'L' shaped strips, having an area of 6×60 mm^2. The resistance of the printed silver layers, measured using a digital multimeter, was found to be $3.00 \pm 0.28\ \Omega$. This was determined by selecting 10 samples at random from a print batch and measuring the resistance across each strip. A schematic diagram, showing the cross sectional and top view of a single cell is given in figure 5.2. As discussed previously, the active silicon layers were printed in different combinations to produce different device architectures which are summarised in table 5.1. The symbols "S" and "O" refer to the base silver contact and transparent conducting oxide (TCO) layer respectively. I, M, N, and P stand for intrinsic, metallurgical, n-, and p-type silicon respectively. Each device was labelled according to the sequence in which the layers were printed, beginning with the silver layer and ending with the TCO layer. The abbreviations DSSP, DSOP, SSOP stand for double stroke

single print, double stroke overprint, and single stroke overprint modes respectively, as described in section 4.3.1. The silver layers were printed using a double stroke single print, while the TCO layer was printed with a single stroke single print as described in section 4.3.1.

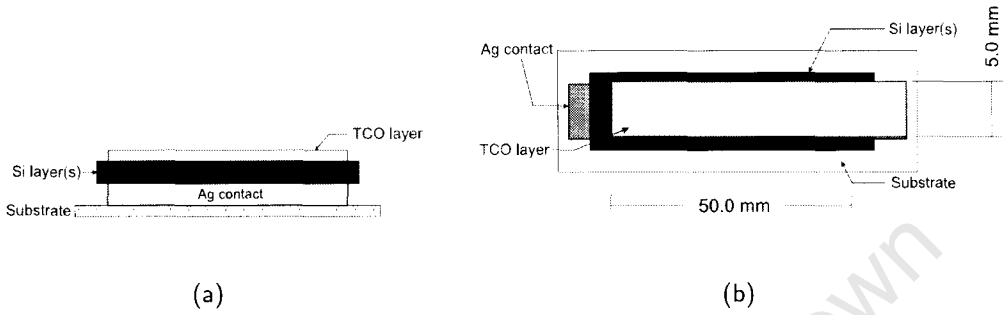


Figure 5.2: Schematic diagrams of the (a) cross-sectional and (b) top view of a printed solar cell.

The thickness of the printed silicon layer was dependent on the print mode used. The thicknesses of these layers, obtained from scanning electron microscopy have been presented earlier in section 4.4. Devices with only a single silicon layer had this layer printed on top of the printed silver base contact. The dimension of the silicon layer was 10×55 mm^2. For heterojunction devices, a different approach was used. The p-n junction, required for the device to function as a solar cell, was produced by first printing the p-type silicon layer on the silver base contact. If the layer was not properly printed, a second print stroke was carried out. The print mode used depended on the quality of the first layer, as discussed in section 4.3.1. Once this layer had cured, the second silicon layer was then printed over it. If this layer was printed with insufficient coverage, a second print stroke was carried out. The print mode used depended on the quality of the initial print. Different print modes had to be experimented with to obtain good quality layers. As a result, device architectures with more than one silicon layer had a low yield of working devices. Metallurgical silicon was also used as a second silicon layer when heterojunction devices were printed, and a similar yield to p-n junction devices was obtained.

The different silicon layers had equal dimensions, but the top silicon layer was printed with an offset of approximately 1 mm. The printed silicon layers were of larger dimensions than the base and top contacts due to registration considerations, and to avoid a short circuit occurring in the device. The active area of each PV cell was 2.5 cm^2 as shown in figure 5.2(b). Once the printed silicon layer(s) had cured, the top contact which connected the printed cells in series in order to form a module, as shown in figure 5.1, was printed. The top contact was a transparent conducting oxide (TCO) which allowed light penetration into the silicon layer(s). The TCO layer

had dimensions of 6×60 mm^2.

Device	Si layer(s)	Si layer(s) print mode(s)	No. of devices characterised
SPO	p-type	DSSP	19
SNO	n-type	DSSP	6
SMO	metallurgical	DSSP	19
SIO	intrinsic	DSSP, DSOP	12
SPNO	p-n junction	DSSP, SSOP, DSOP	2
SPMO	p-metallurgical junction	DSSP, SSOP, DSOP	2

Table 5.1: Summary of printed devices characterised. DSSP, DSOP and, SSOP are the different print modes used.

5.1 Electrical Characterisation Experiments

The printed solar cells were characterized using a Keithley 4200 Semiconductor Characterization System (SCS), as shown schematically in figure 5.3, which had a current and voltage resolution of 1 pA and 2 μV respectively. The SCS could be configured to run different electrical characterization tests for semiconductor devices and test structures using an interactive test environment application program (KITE).

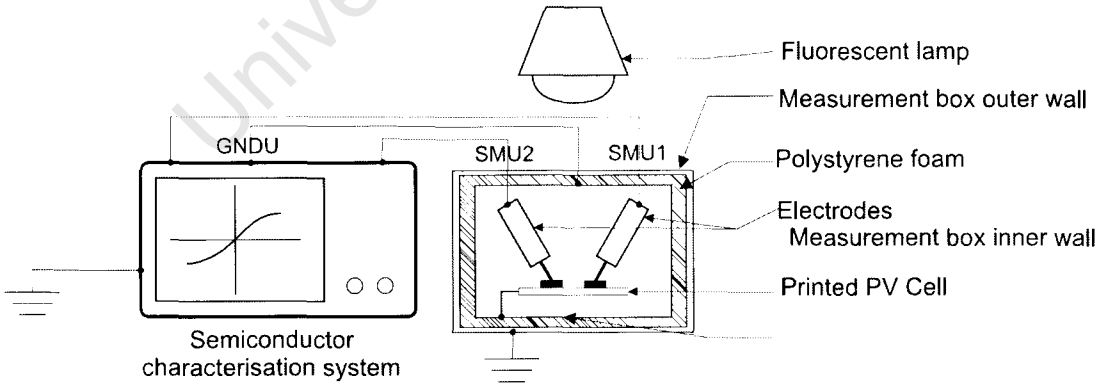


Figure 5.3: Schematic diagram showing the experimental set up for I-V and photoresponse measurements made with the Keithley SCS.

The source and measurement functions carried out using the SCS, were performed by Source-Measurement Units (SMUs) which could be used simultaneously for sourcing or measuring the

current through, or voltage across a device. The SCS also had a ground unit (GNDU) which was used for making ground connections. The connections from the SMU and GNDU to the devices tested were made via gold and tungsten probes, labelled SMU1, SMU2 and GNDU. A sample box [97], consisting of a sample stage, in a double walled enclosure, in which devices to be characterized were placed, was connected to the SCS as shown in figure 5.3. The walls of the box were separated from each other with a layer of polystyrene. The sample box was essentially a double Faraday cage, designed in order to minimize the effect of electrical noise when characterizing devices. The outer box was connected to the common earth, while the inner box was connected to the GNDU connection of the SCS.

The data obtained from measurements could also be plotted in the form of response curves, by the KITE software, and the output viewed simultaneously on the monitor in real time. As the Keithley SCS was originally designed for the characterization of devices such as transistors, and was not equipped with its own light source, an 18 W fluorescent light bulb was used as a light source when investigating the illuminated I-V characteristics of the printed devices. The intensity of the light source, measured using a Testo 545 digital light meter, was 21.3 $W.m^{-2}$. A schematic diagram of the measurement set up is as shown in figure 5.3.

A Spi-Cell Tester Solar I-V measurement system, as shown in figure 5.4, was also used in the electrical characterization of the printed devices. The Spi-Cell Tester was able to provide simulated Air Mass 1.5 Global terrestrial conditions [8], using a 1 KW Xenon lamp of intensity 700 - 1100 $W.m^{-2}$, equipped with an optical filter. The Spi-Cell system included a calibrated reference solar cell. This reference cell was also used to monitor the intensity of illumination from the xenon lamp.

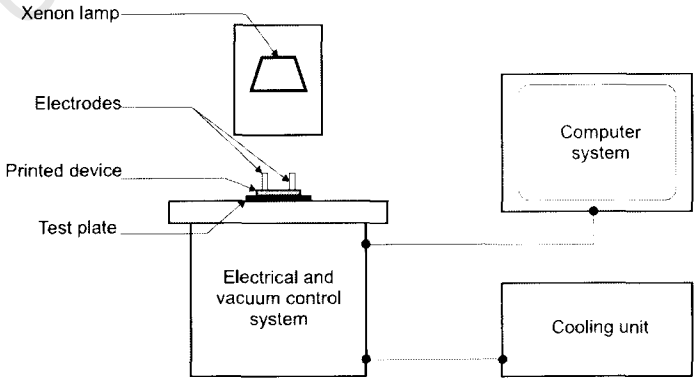


Figure 5.4: Schematic diagram of the Spi-Cell Tester set-up.

The solar cell tester also had an external computerised control system which was used for operating the machine, as well as for viewing, and saving data obtained from measurements taken. The solar tester also had a stand-alone temperature control unit which was used for maintaining a fairly constant temperature for the test plate, on which devices were placed when carrying out measurements. In its standard configuration, the Spi-Cell Tester had four pairs of electrodes, in the form of gold probes, connected in parallel, which served as the positive terminals while the test plate on which devices were placed, served as the negative terminal. This initial design of the system had to be modified in order to carry out the electrical characterization of the printed devices produced. As both the positive and negative contacts of the printed devices were on top of the substrate, no current and voltage probes were required at the back of the cell, unlike in most crystalline silicon solar cell designs. Therefore, only two of the four pairs of gold probes were used: one as the positive terminal and the other as the negative terminal. The solar cell tester originally had a current and voltage resolution of 4.9 mA and 0.6 mV respectively. As the current resolution of the solar cell tester was in the mA range, the shunt resistor used when testing cells had to be changed from 2 Ω to 2 kΩ, in order to measure currents in the μA range.

5.1.1 Measurement Procedure

The printed PV modules were first cut out from the A4 paper substrate, using a clean pair of scissors, to an 8×8 cm^2 sized sheet. The PV module was then placed in the measurement box of the semiconductor characterization system, and the electrodes were connected to the terminals of the device as illustrated in figure 5.3. The silver base contact was connected to SMU1 while the TCO front contact was connected to GNDU. The contacts were then tested with a digital multimeter to ensure that there was electrical contact between the printed devices and the electrodes. Once this was done, the fluorescent lamp was held in place above the sample at a distance of 8.5 cm from the substrate. The experimental electrical characterization procedure was then carried out as described below.

For characterisation using the Spi-Cell Tester, each device to be characterized was placed in position on the test plate, and the vacuum system was activated to hold it in place. The electrodes were then lowered into contact with the device, and the xenon lamp switched on, with its shutter closed before a measurement cycle was begun.

Photoresponse Measurements

In order to carry out current photoresponse measurements, the Keithley SCS was programmed to operate in sampling mode, with a hold time of 1 s, to record the current response of the device as time elapsed. For current response measurements, the SMU was configured to maintain a zero potential difference across the device, and measure the current through the device, in steps of 1 s. The aim of this experiment was to test the response of the printed PV device to light, and determine if that response was consistent with the expected electrical behaviour of PV devices. Once the measurement cycle commenced, the current response of the device was recorded as the fluorescent lamp was switched on and off. The light source was initially switched off for 300 s with the current through the printed device measured over this duration. The light source was then switched on for 300 s and the current through the printed device also measured. After this, the light source was switched off for a duration of 600 s, and then switched on for a further 600 s, with the current response of the printed device measured throughout the cycle. The total measurement time for each device characterized was about 1800 s, and 100 devices were tested. As the current response of the devices being tested could be monitored in real time, the on and off measurement cycle was longer than described above for some devices, depending on their performance.

A similar procedure was carried out for the voltage photoresponse measurements, in which case, the voltage response of the devices as time elapsed was measured. For voltage response measurements, the SMU was configured to maintain zero current through, and measure the voltage across the device, in steps of 1 s. The results obtained from this characterization procedure are presented in section 5.2. For both current and voltage response tests, the measurements were carried out at room temperature, with SMU1 connected to the silver base contact and the GNDU probe connected to the top TCO layer. Although the devices to be tested were placed in the sample box, and shielded from direct external light sources, diffuse light was able to reach the device from the general lighting in the laboratory. This was due to the experimental setup, in which the top cover of the sample box had to be left open in order to carry out "light on" tests, maintaining the same measurement conditions with respect to electrical noise. The effect of the diffuse light was minimized by ensuring most of the device was shielded by the fluorescent lamp when carrying out "light off" measurements.

Current-Voltage (I-V) Response Measurements

For devices with fast response times, I-V characterization was also carried out with the Keithley SCS. This instrument was used in carrying out I-V response characterization due to its capability of measuring currents as low as 1 pA. The I-V response measurements were first carried out in the dark, and then under illumination. The SCS was programmed to sweep the voltage across the devices from -8.0 to +8.0 V in steps of 0.01 V. A hold time of 600 s and sweep delay of 1 s were set to allow for current settling. The devices were connected to the probes in the same manner as during the photoresponse measurements. When carrying out dark I-V response measurements, the sample box was closed to ensure no light was allowed to reach the printed device. During each voltage sweep, the SCS recorded the corresponding current response and the data was plotted in the form of I-V response curves. After completing the dark I-V characterization, the printed device was then exposed to light from the fluorescent lamp and the measurement cycle repeated.

I-V characterisation was also carried out using the Spi-Cell tester. The Spi-Cell tester was equipped with a bipolar operational power supply, used as the electronic load when testing solar cells, and was controlled by the computer test programme. Once the measurement cycle was activated via the computer controls, the shutter of the xenon lamp opened, exposing the printed device to the high intensity light. The bipolar power supply varied the resistance load across the device, simultaneously measuring and recording the current and voltage, and the data plotted in the form of I-V curves and saved. Each measurement cycle lasted for approximately 10 s. The temperature control unit was used to regulate the temperature of the printed devices while measurements were taken. Due to the limitation in its current resolution, the Spi-Cell tester could only test devices with currents in the μA range.

5.2 Electrical Performance

The results obtained from the electrical characterization tests using the Keithley characterisation system, and Spi-Cell Solar Tester are presented in this section.

Single Layers

Using the Keithley measurement system, characteristic curves of the current and voltage responses of the devices were obtained.

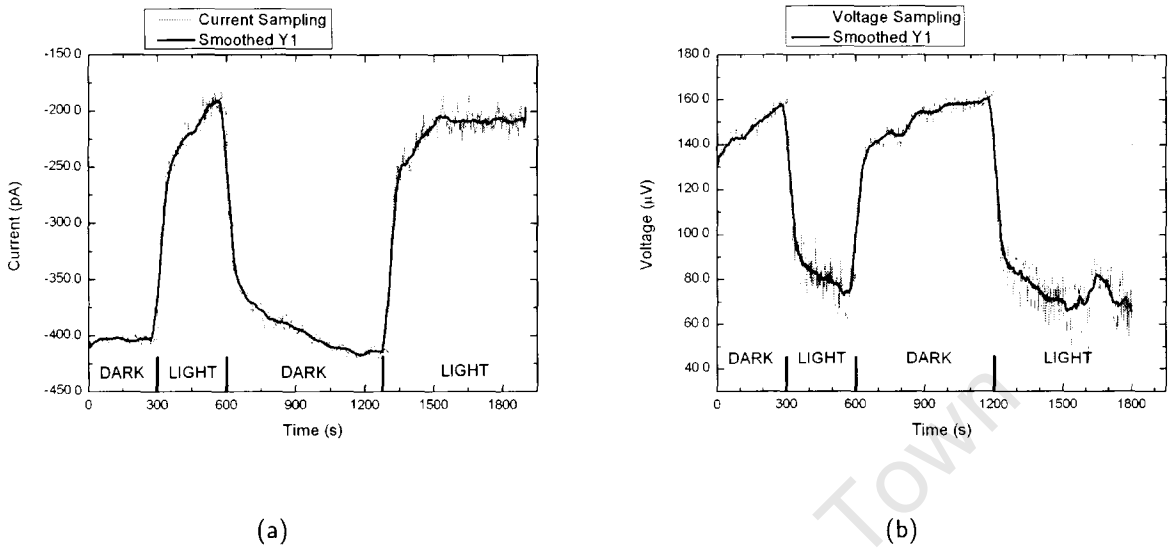


Figure 5.5: Typical (a) current and (b) voltage photoresponse curves of characterised devices. The thick lines are the smoothed function.

Figure 5.5, shows the current and voltage response of a device with intrinsic silicon as the active semiconducting layer. Also plotted is a smoothed curve of the data. The curves obtained from the measurement appeared very noisy. This was most likely as a result of interference from the fluorescent lamp as the intensity of the noisy output increased during the "light on" measurement cycle. As figure 5.5(a) shows the output current appears fairly constant with time. The base level is not zero, probably as a result of the biasing effect of the Keithley SCS when it carries out measurements. When the light is switched on, the photoresponse curves show a sharp response to illumination, with a very steep gradient. The steepness of this gradient begins to reduce after approximately 90 s. This steep response is most likely as a result of the time required for the fluorescent lamp to reach its full intensity. As the lamp settled the effect of the sudden charge reduced, shown by the very slow increase of current with time. Once the light was switched off, the sharp response is again observed but this lasts for a longer period than when switching on, as the fluorescent lamp has a slower discharge than charge time. Again, the rate of current change reduces, and the device begins to stabilize at a level slightly lower than the initial base level. During the second cycle, the device repeats the same behaviour. The device then reached a peak value of about 200 pA after about 300s, before stabilizing.

The voltage response of the device, as shown in figure 5.5(b), was similar to the current response. However, unlike in the current response, where the output current was more positive when the

device was illuminated, the voltage across the device was more negative. The voltage across the device under dark conditions was non-zero and was increasing. This non-zero voltage measured across the device is most likely as a result of the built-in potential between the different layers of the device [16]. As the light was switched on, the potential across the device dropped very quickly, and the rate began to slow down after about 90 s. The measured voltage was also noisy. The intensity of the noisy signal increased when the lamp was on, indicating that it was the most likely source of interference during measurements. After the lamp was switched off, the potential increased rapidly, and began approaching a stable value after about 600 s. The fast response was also brief, with a slower rate of change in the potential across the device after about 90 s.

Current and voltage response curves were obtained for 51 devices, consisting of different types of single silicon layers. The maximum and minimum current ($\Delta I_{max}, \Delta I_{min}$), and voltage range values ($\Delta V_{max}, \Delta V_{min}$) were determined, as well as the maximum and minimum characteristic response times, τ_{min} and τ_{max}. $\Delta I_{max}, \Delta I_{min}, \Delta V_{max}, \Delta V_{min}$ for each device were determined by averaging out the data over 10 points, and the standard deviation associated with each value was determined and these results are presented in table 5.2.

Device	ΔI_{max} (nA)	ΔI_{min} (nA)	ΔV_{max} (mV)	ΔV_{min} (mV)	τ_{max}	τ_{min} (s)
SMO	3.823±0.034	0.674±0.008	0.165±0.002	0.065±0.001	119.94	21.23
SPO	5.236±0.065	1.680±0.013	0.154±0.004	0.057±0.001	156.01	19.04
SIO	0.472±0.007	0.044±0.002	0.166±0.003	0.047±0.002	32.72	9.02
SNO	1.500±0.016	0.840±0.021	0.119±0.003	0.092±0.002	205.40	41.89

Table 5.2: Characteristic results obtained from current and voltage photoresponse characterization of the printed nanoparticulate PV devices.

Not every printed device tested provided a discernable photoresponse curve, which was likely due to a short circuit within the device, or poor electrical contact between the different layers. From the p- and metallurgical type silicon devices, roughly 80% of the devices provided discernable photoresponse curves, while n-type and intrinsic silicon printed devices had a yield of approximately 67 and 58% respectively. These results serve as an indication regarding the quality of the inks, and the printing process.

For devices with fast response times, I-V response curves were obtained. The characteristic curve obtained for single layers, as shown in figure 5.6, had similar characteristics to that of an Ohmic resistor, when tested under dark conditions, which is in agreement with the behaviour expected of a metal-semiconductor contact [16]. When illuminated however, the overall response was non-

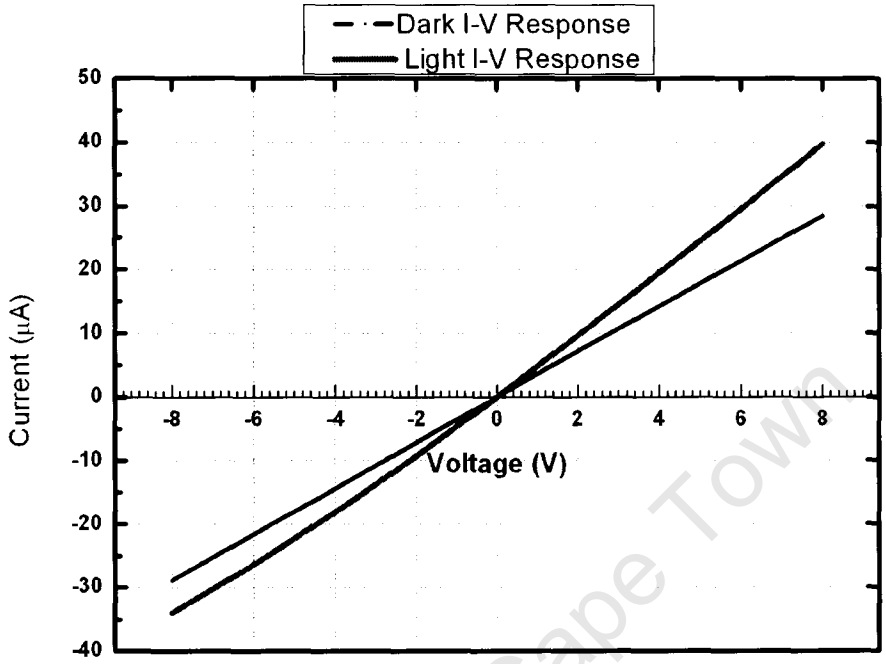


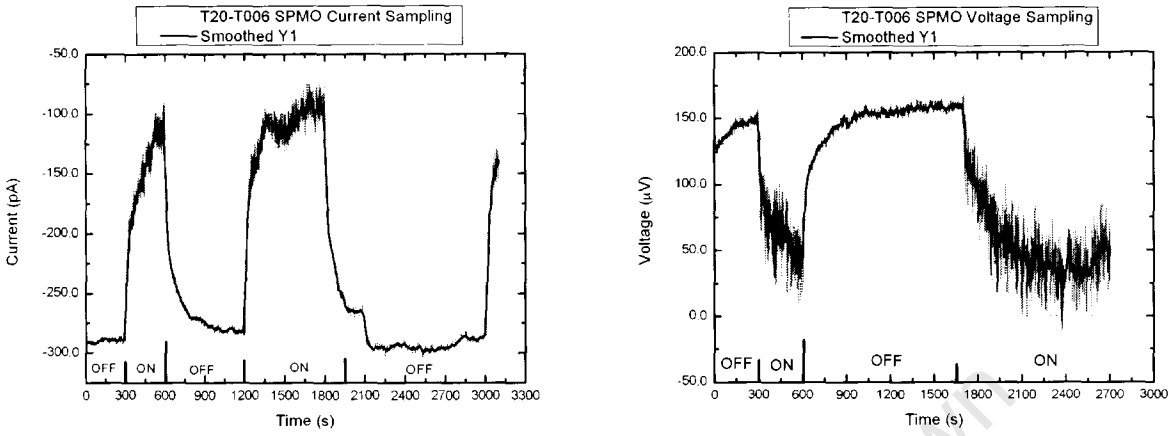
Figure 5.6: Typical I-V response curves obtained for single layer printed devices.

linear, with two distinct linear regions. The first linear region occurred when the bias voltage was positive, while the second linear region occurred when a negative bias voltage was applied across the device.

Heterojunctions

Photoresponse tests were also carried out on the printed devices with double layers consisting of a layer of p-type silicon printed on a metallurgical or n-type silicon layer. From the devices tested, the parameters deduced from the photoresponse curves are presented in table 5.3. The photoresponse behaviours observed were similar to those obtained from devices consisting of a single silicon layer, as shown in the curves for a device with metallurgical silicon bottom layer in figure 5.7.

A similar behaviour was observed with a device consisting of a layer of p-type silicon printed on an n-type silicon layer. Two of each type of heterojunction devices were characterised, using the Keithley SCS, for I-V and photoresponse tests, and ΔI, which represents the difference between



(a) (b)

Figure 5.7: Plots of the (a) current and (b) voltage photoresponse of a heterojunction device.

the light and dark currents, and ΔV, the difference between the light and dark voltages, were determined and are presented in table 5.3. τ is the response time of the device, calculated as the average time taken for the device to reach $(1 - 1/e)$ of the maximum value. The yield of the devices characterised was approximately 50% from both sets of devices.

Device	ΔI (nA)	ΔV (mV)	τ (s)
SPMO	0.230±0.002	0.178±0.004	27.61
SPNO	3.477±0.030	1.401±0.011	27.49

Table 5.3: Results obtained from current and voltage photoresponse characterization of the printed nanoparticulate PV devices.

Using the Keithley SCS, I-V response tests were carried out for devices with printed P and N layers. The interface between these two layers formed the P-N junction of the PV cell. The I-V curves obtained for a P-N junction printed device are presented in figures 5.8 and 5.9.

The profile of the device, when characterised in the dark, was similar to that of a P-N junction diode [36]. Under positive voltage bias, the current increased exponentially with increasing voltage as figure 5.8 shows. Under illumination, the same behaviour is observed, with a higher output current. This indicated that the completed PV structure was indeed exhibiting electronic characteristics typical of solar cells [16]. The general shape of the curve is correct, but the illuminated curve should shift down below the dark I-V curve in the fourth quadrant [19]. Under

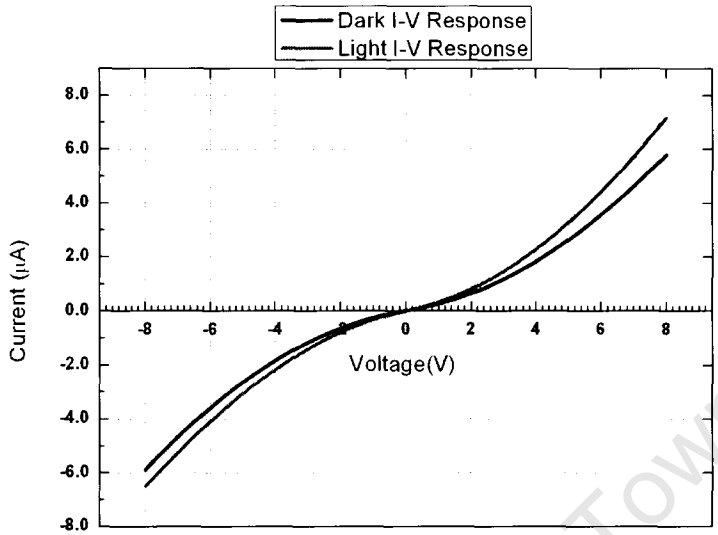


Figure 5.8: Measured I-V response curve of a printed silicon PV device with a p-n heterojunction structure.

negative bias, the behaviour was also exponential but, as can be seen from the curves, the overall response of the devices was not symmetrical about the current axis. The values of I_{sc} and V_{oc} for this device were determined using figure 5.9.

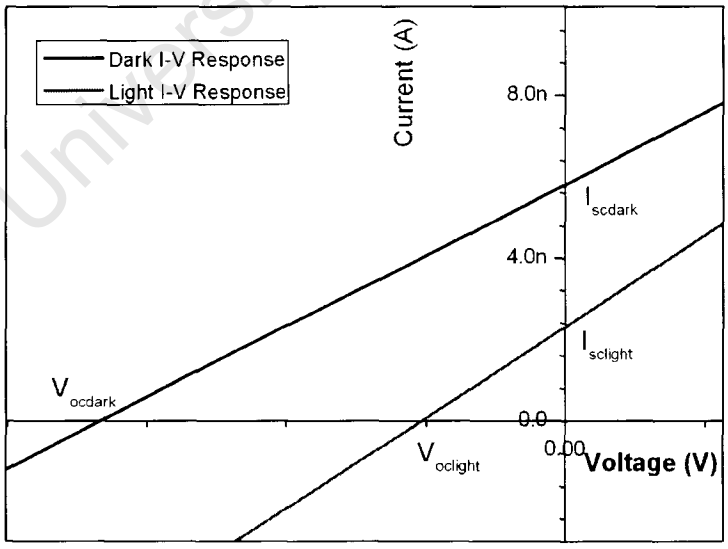


Figure 5.9: Measured I-V response curve of a printed silicon PV device using a p-n heterojunction structure showing I_{sc} and V_{oc} in the dark and when illuminated.

The values of I_{sc} and V_{oc} for the devices tested, deduced from their I-V response curves, were 2.30 nA and 0.80 mV respectively.

Spi-Cell Tester Measurements

For measurements carried out with the Spi-Cell system, only devices with an SPNO configuration could be characterized, as the outputs from other device configurations were too low to be measured. Figure 5.10 shows a typical current-voltage response curve for a PV module. Plotted on the same graph, is the power curve for the device showing the maximum power point, P_{max}.

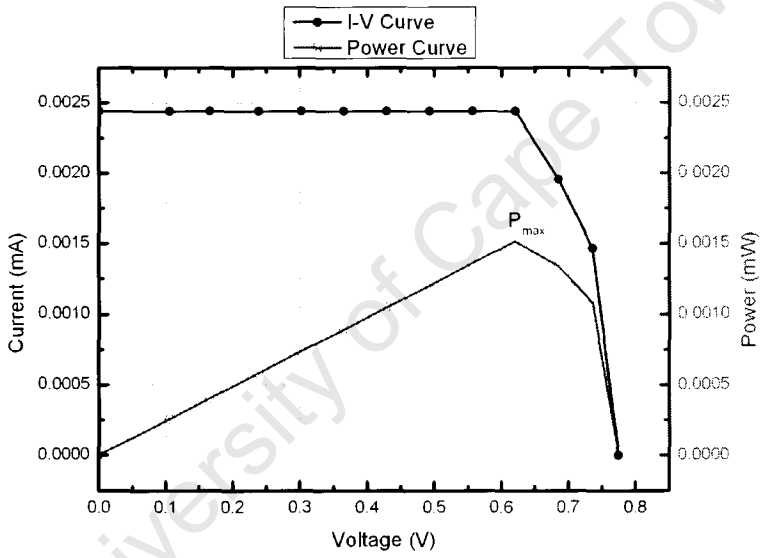


Figure 5.10: I-V response and power output curves for a P-N junction PV cell obtained using the Spi-Cell Tester.

The current-voltage response curve obtained is characteristic of the expected behaviour of a functional solar cell [20, 23]. The intensity of the lamp used in characterizing the devices was 1000 W.m^{-2} and the active area of the PV module was 0.001 m^2. From the I-V curves plotted, and using equations (2.59) and (2.60), the electrical characteristics were determined for the PV devices. These characteristics are presented in table 5.4.

Characteristic	Value
Short Circuit Current, I_{sc} (mA)	0.00245
Open Circuit Voltage, V_{oc} (V)	0.77462
Peak Current, I_{pm} (mA)	0.00244
Peak Voltage, V_{pm} (V)	0.61984
Maximum Power Point, P_{max} (mW)	0.00151
Fill Factor, FF	0.79692
Efficiency, η %	1.512 μ

Table 5.4: Table showing the electrical characteristics of a printed solar cell.

6. Discussion

The basic concept behind the experimental procedure followed in the fabrication of the PV devices described in chapter 5, involved a novel approach towards producing PV cells. This approach, as described in this thesis, focuses on the use of screen printing of nanoparticulate silicon inks as a fabrication technique for producing silicon PV cells on paper substrates. In order to use the technique of screen printing, the active semiconductor had to be prepared in the form of an ink. Ink making is a complex process, in which several variables need to be taken into account in order to produce an ink with the right balance between printability and functionality [67]. In order for this to be achieved, the silicon material had to be prepared in the form of a nanopowder, which could then be mixed with other components to produce an ink. This required the use of a synthesizing technique for producing nanoparticles. The technique employed in this thesis was milling and the experimental approach was discussed in chapter 3. This chapter proceeds to discuss the results obtained at the various stages of the fabrication and characterisation process.

6.1 PV Device Fabrication and Performance

As discussed earlier in chapter 2, a solar cell is a two terminal device, consisting of a light absorbing material which generates charge carriers under illumination and behaves like a diode in the dark [8]. The charges generated within the solar cell are driven to either of its terminals by a built in asymmetry in the device, achieved by means of a p-n junction [8]. In order for a device to function as a solar cell, the following requirements must be met [8, 16, 98]:

- light should reach the p-n junction,
- it must consist of a photovoltaic material of energy band gap E_g, which absorbs incident light of energy $E > E_g$ allowing charge carriers to be generated,
- the photogenerated carriers should not recombine, implying that it must have a mechanism that allows for charge separation, and
- it must also have a mechanism for the collection of the charges to an external circuit or load.

The PV devices were described in the previous chapter as consisting of a printed layer of TCO which served as a window layer, allowing light to penetrate into the device, the silicon structure

and the silver base layer. The mechanism for charge separation was achieved by the printed p-n heterojunction described in chapter 4. Photogenerated charges were collected by means of the silver base layer as well as the top TCO layer. Thus, the major requirements for a fully functional solar cell were met by means of the fabrication procedure.

In powder form, silicon nanoparticles could be brought together to form a layer that would have properties akin to a continuous material. However, without a mechanism whereby the particles could be held together in a stable structure, it would be extremely difficult to maintain a conduction path for the transport of charges within the bulk structure. The particles were, therefore, used in preparing an ink which could then be screen printed and, after drying, form a stable network. As presented in section 4.4, at a particle loading of 80% by weight, scanning electron micrographs of the printed layers show that they consisted of tightly packed particles, which would allow for charge transport when an external field is applied. The micrographs show that, when printed, the silicon nanoparticles tended to agglomerate into large clusters. In order to create the junction required for charge separation and hence, the photovoltaic effect, it was necessary that the printed layers formed a single network with the different layers adhering together. As shown in the scanning electron micrographs of the cross sectional view of the layers, this was achieved. The printed silicon layers made good contact with each other as well as the top and bottom contacts of the device.

6.1.1 Analysis of PV Device Performance

In order for the printed layers to function properly as PV devices, there had to be good electrical contact between them. Both optical and scanning electron microscopy showed that the screen printed layers appeared continuous.The graphs of the photoresponse characteristics of single layer devices, presented in 5.6, show that, in the dark the layers had an ohmic response to an applied voltage, consistent with results obtained for a metal-semiconductor contact [16, 99]. Therefore, the printed layers were indeed continuous and electrically conducting. In the I-V characteristics of the single layers under illumination, it was observed that the response was not uniform across the entire voltage range tested. A linear response was observed only when a positive voltage was applied across the layer. From the I-V curves, as shown in figure 5.6, the resistance for the different configurations of single layer devices were determined to be 0.28, 0.078, and 0.39 MΩ for the intrinsic, metallurgical, and p-type silicon layer devices respectively. These observations imply that devices produced using the commercially sourced intrinsic nanopowders could be used in producing electrically functional devices. Similarly, particles produced using high energy milling

were not electrically passivated. Furthermore, using these particles to prepare a semiconducting ink and printing them, semiconductor devices were produced that were electrically responsive, and had structural integrity.

Figure 5.8, shows that the dark I-V characteristics of the printed P-N junction device were similar to that of a p-n junction diode [8, 16]. This is consistent with existing theory, which describes the behaviour of the solar cell as similar to a photodiode i.e. it behaves like a p-n junction diode in the dark with a different response under illumination [16, 23]. When illuminated, the devices showed a visible current-voltage response as shown in figure 5.8. This response was more pronounced when a positive voltage bias was applied across the device, as observed from the graph. Hence, using the nanoparticulate inks produced, and depositing each semiconducting layer sequentially on each other, a device was fabricated which had I-V characteristics consistent with those obtained from p-n junction diodes, and had a definite response to illumination.

From the I-V characterisation carried out using the Spi-Cell tester, the responses of the p-n junction devices were consistent with the behaviour of PV cells [20, 22]. The values of I_{sc}, I_{pm} and P_{max}, deduced from the I-V characteristic curves, are quite low for high power applications and the efficiency of the cells is very low. However, the values obtained for the V_{oc}, V_{pm} and FF of the printed PV cells are good and comparable to what is currently obtained from PV cells made from organic solar cells which have V_{oc} between 0.5 - 0.8 V, and fill factors ranging from 0.4261 - 0.6660 [100, 5]. The fill factor obtained is also comparable with amorphous silicon cells, used in low power devices which have FF in the order of 0.766 for tandem cells [101]. As the current produced by the solar cell is dependent on the transport of charges within the system [8], it would seem that the device structure does not allow for the free movement of charges. Due to the complex nature of the different layers containing organic binders and nanoparticles, a further study to understand the charge transport through these media is required but is outside the scope of this thesis.

The behaviour of a solar cell can be described using equation (2.56). However, due to the presence of parasitic resistances in a cell, equation (2.62) is generally used in modelling the behaviour of a solar cell under actual operating conditions [19, 98] and the equivalent circuit diagram is shown in figure 2.12. Equation (2.62) can be rewritten as [27, 98]

$$I = I_0 \left\{ \exp\left[\frac{q}{m k_B T} (V - I R_s) \right] - 1 \right\} + \left(\frac{V - I R_s}{R_{sh}} \right) - I_L \quad , \tag{6.1}$$

where I_0 is the reverse saturation current, q is the electronic charge, m the ideality factor, k_B Boltzmann's constant, V the output voltage, I_L the photogenerated current, R_s, R_{sh} the series

and shunt resistances, and T the temperature. For dark I-V characterisation, $I_L = 0$, and if R_{sh} is large, $\frac{V}{R_{sh}} \rightarrow 0$, then equation (6.1) can be rewritten as

$$V = IR_s + \frac{mk_BT}{q} \ln \left[\frac{I}{I_0} \left(1 + \frac{R_s}{R_{sh}} \right) + 1 \right] \quad . \tag{6.2}$$

Using the data obtained from the dark I-V characterisation carried out with the Keithley SCS, a V-I curve of the data was plotted and is shown in figure 6.1. Equation (6.2) was used as a fitting equation to the experimental data, as shown in figure 6.1.

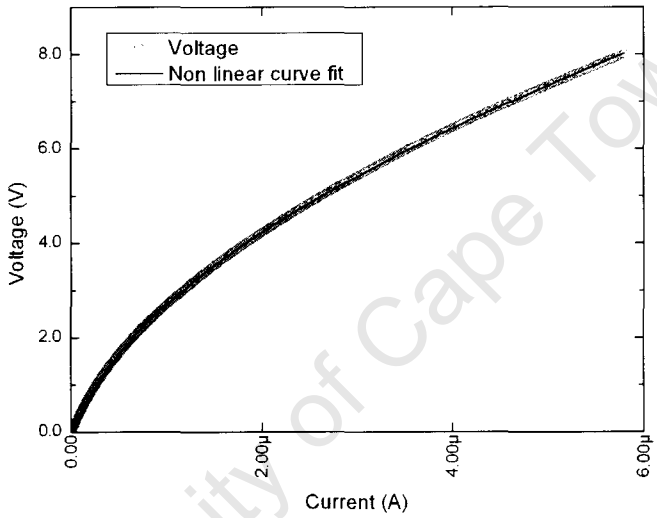


Figure 6.1: V-I curve of the p-n junction solar cell in the dark. The non-linear curve fit is shown in dark lines.

A good fit was obtained, and I_0 was determined to be 0.4924±0.0019 μA. The ideality factor m, was deduced to be 76.23±0.22. This value of the ideality factor is very high compared to what is usually obtained for crystalline silicon solar cells, where m usually lies between 1 and 3 [20, 23, 26]. This high value of m is reflected in the very low values of current obtained, and gives a measure of how much the solar cell behaviour deviates from ideal conditions [24], and could be as a result of the quality of the p-n junction formed. The value of R_{sh} was determined to be 930 MΩ while the series resistance R_s, was 0.52±0.003 MΩ. From equation (6.1), it can be seen that the joint effect of R_{sh} and R_s is to reduce the overall efficiency of the cell. The shunt resistance, R_{sh} is a result of leakage current through the cell [8], and is required to be as large as possible in order to eliminate the $\frac{V-IR_s}{R_{sh}}$ term [8]. The value of R_{sh} determined was relatively high, indicating that the leakage current was in the order of 0.8 nA, which is small compared to I_{sc} and agrees with theoretical expectations. The series resistance term, R_s, which arises due to

the resistance of the cell material to current flow, as well as between the contacts of the cell, is required to be as small as possible for high efficiency cells [8]. The high value of R_S obtained could also explain the low efficiency of 1.512 μ% obtained from the experimental data. This also suggests a high contact resistance between the printed p- and n-type silicon layers, as well as between the semiconductor layers and the top and bottom contacts.

The analysis of the device characteristics described above are consistent with a fully functional solar cell. The low output current and power from the cell could be as a result of low photogeneration of carriers, due to insufficient penetration of light into the silicon layers. The transparent conducting oxide used as the top window layer had a very low transmissivity in the order of 0.1 and thus, the amount of light penetrating into the active layers would not be optimum. Due to the complex ink and binder matrix, it is highly probable that the photogenerated charges would not move freely, increasing the probability of recombination before they could be collected, leading to reduced device performance. However, the open circuit voltage of 0.77462 V obtained when testing the device under standard AM 1.5 conditions, is very good, and consistent with what is obtainable from silicon solar cells [17]. The fill factor of approximately 80% is also very good.

6.1.2 Device Performance and Print Quality

The results obtained for the different devices were analysed in their print order to determine the relationship between the print quality and device performance. Figure 6.2 shows the plots of current and voltage as a function of print number obtained for the p-type silicon devices. The correlation between the voltage and current ranges for each device configuration was also examined and a representative plot is shown in figure 6.3.

As can be observed from figure 6.3, there is a positive correlation between the current and voltage responses for each device. From figure 6.2, it is observed that the first few devices have low current and voltage ranges, which begin to stabilise as more devices were printed. The maximum values for the current and voltage ranges occur at about the median device and then their performance begins to decrease until minimum values are reached in the last few prints. Similar trends were observed for the single layer devices consisting of metallurgical, intrinsic, n- or p-type silicon as the active semiconductor. This behaviour is related to the behaviour of the ink during printing. As mentioned in section 4.2, a thixotropic ink exhibits shear thinning behaviour, but regains its initial properties once the applied pressure is removed. In the case of the silicon inks prepared for the printing of the layers, as discussed in section 4.3.1, the inks exhibited shear thinning behaviour

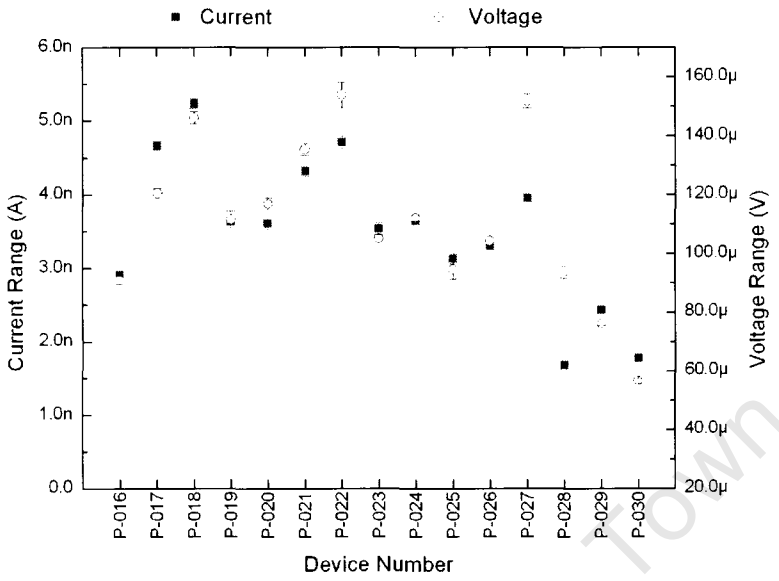


Figure 6.2: Plot showing the current and voltage range of measured SPO devices in their print order.

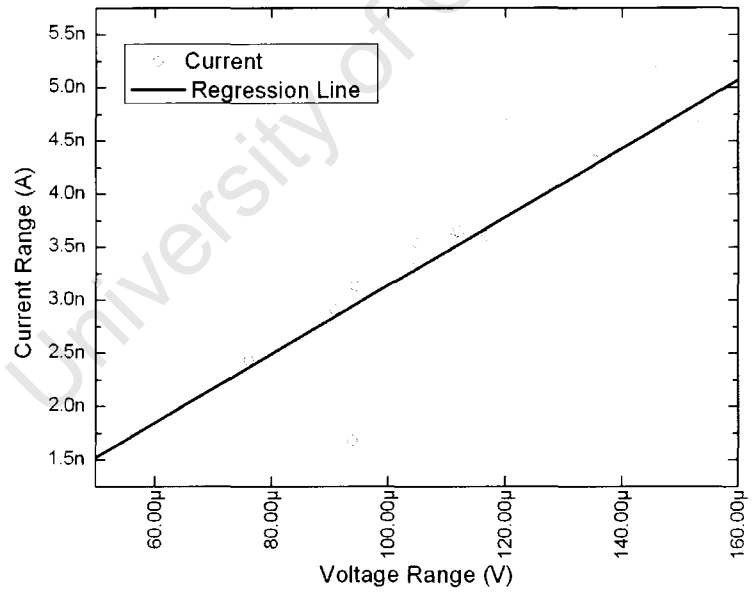


Figure 6.3: Correlation between the voltage and current ranges for printed SPO devices

only. As the preparation process was not optimal, it appears that the first few print strokes had the effect of mixing the inks further, resulting in better print quality with time. However, as the ink did not regain its initial viscous properties, the quality of the ink deteriorated, requiring more print strokes to obtain good layers. The electrical performance of the devices as shown in figure

6.2, indicates that the later prints performed badly due to the ink quality. The poorer electrical performance was not as a result of the printing process as the same settings and conditions were applied during the printing of the devices. By means of this analysis, it is possible to optimise the printing process to obtain reproducibility between different batches.

7. Conclusion

This thesis has focused on the production of PV devices by means of screen printing. Apart from the cost advantages, the approach employs silicon nanoparticles in producing the semiconductor inks used in producing the devices. Thus, by means of mechanical milling, silicon nanoparticles were produced and used as the active material in making an ink. Without the complicated processes generally employed in PV device fabrication, these nanoparticulate semiconducting inks were then used in producing junctions between differing silicon materials in the form of printed layers which then formed an electrically functional device. The printed devices exhibit electrical properties characteristic of silicon PV devices and microscopy revealed that the nanoparticles had indeed formed clusters that were capable of transporting charge through the device. Thus, the experimental process followed resulted in the successful production of a functional silicon solar cell.

This process is currently being optimised. The capacitive effects observed, as well as the low power output from the devices require improvement. This requires a better understanding of the ink preparation process as well as optimizing the particle loading of the inks. The printing process is also being optimized in order to allow for deposition of thicker layers which properly adhere to each other when heterojunctions are fabricated, and maintain their structural integrity during, and after the printing process. Work is also being carried out on the material used as the top metal contact. The aim is to be able to get a material that will allow more light to penetrate into the device, which should result in higher photogeneration of charges. Device testing conditions are also being improved in order to have a better understanding of the fabricated devices.

In spite of these challenges, the initial results presented in this thesis are encouraging, and hint at the possibility of screen printing on paper substrates becoming an effective means of producing silicon based PV devices for low power devices such as cell phones, calculators and other portable devices.

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