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DIRECT DIGITAL CONTROL
OF A
D. C. MACHINE

by

H. F. Wechuizen

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S U M M A R Y

The object of this Thesis is to build an interface between a computer and a three phase thyristor bridge rectifier, enabling the computer to control its D.C. output voltage. By writing a suitable computer program, this system was extended to provide closed loop computer control of the speed of a D.C. machine.

The first interface and computer program were so designed that the computer provided the required analogue triggering delay for voltage control of the D.C. output.

This setup did not allow for infinite variation of the voltage and occupied a large portion of the computer time. Thus it was decided to modify the interface, letting it provide its own delay, thus freeing the computer of the delay routine and giving it more time to do other tasks. Control of the bridge rectifier was also improved.

When closed loop control was implemented, the system was found to be unstable. It was thus simulated and stabilized on the analogue computer. A new digital computer program was written incorporating those characteristics which were found necessary in the simulation to make the system stable.

The modified form of compensation was found to give a satisfactory performance for both step and ramp inputs to the system as well as load transients on the D.C. motor.

Various types of tachogenerator were tested to find which was the most suitable for operation with the computer. All the types tested gave satisfactory performances. The major factor affecting performance was the quality of the tachogenerator.

CHAPTER I

INTRODUCTION

The purpose of this thesis is to investigate the feasibility of using a small digital computer to directly control electrical equipment.

At present the small computer is used in industry to control the entire operation of rolling mills¹³ in numerical machine control⁵ etc.. In these cases the various units that comprise the plant are separate closed-loop control systems which require analogue input control signals. As the computer processes digital signals, expensive digital-to-analogue convertors are required to interface the computer to the control systems. Any analogue information fed to the computer from the system also requires an analogue-to-digital convertor which is also costly.

In this thesis it is proposed to include the computer in the control loops of the various units and to do away with the digital-to-analogue convertors. This means that some of the control gear can be eliminated, their functions being simulated by the computer, and that the remaining control units must accept and understand digital signals. This is illustrated in Figure I.

A device which accepts digital signals is the thyristor - a voltage pulse placed on its gate will turn a thyristor on if the anode circuit conditions are suitable. Developing equipment to allow a computer to control a bank of thyristors might appear at first sight to have limited application but virtually any type of electrical apparatus may be controlled by this means. D.C. machines may be controlled by A.C. phase control of a single or three phase bridge or by chopper modulation of a D.C. supply. A.C. machines may be controlled by means of a form of modulation now being developed at this University, and resistive heating can also be very successfully controlled by means of thyristors.

The system chosen for development in this case was that of speed control, the power being supplied by a D.C. motor which was armature controlled by means of a three phase thyristor bridge.

For the test set up, speed feedback was, by means of an analogue-to-digital convertor. The development of a digital tachometer is a subject of a later thesis.

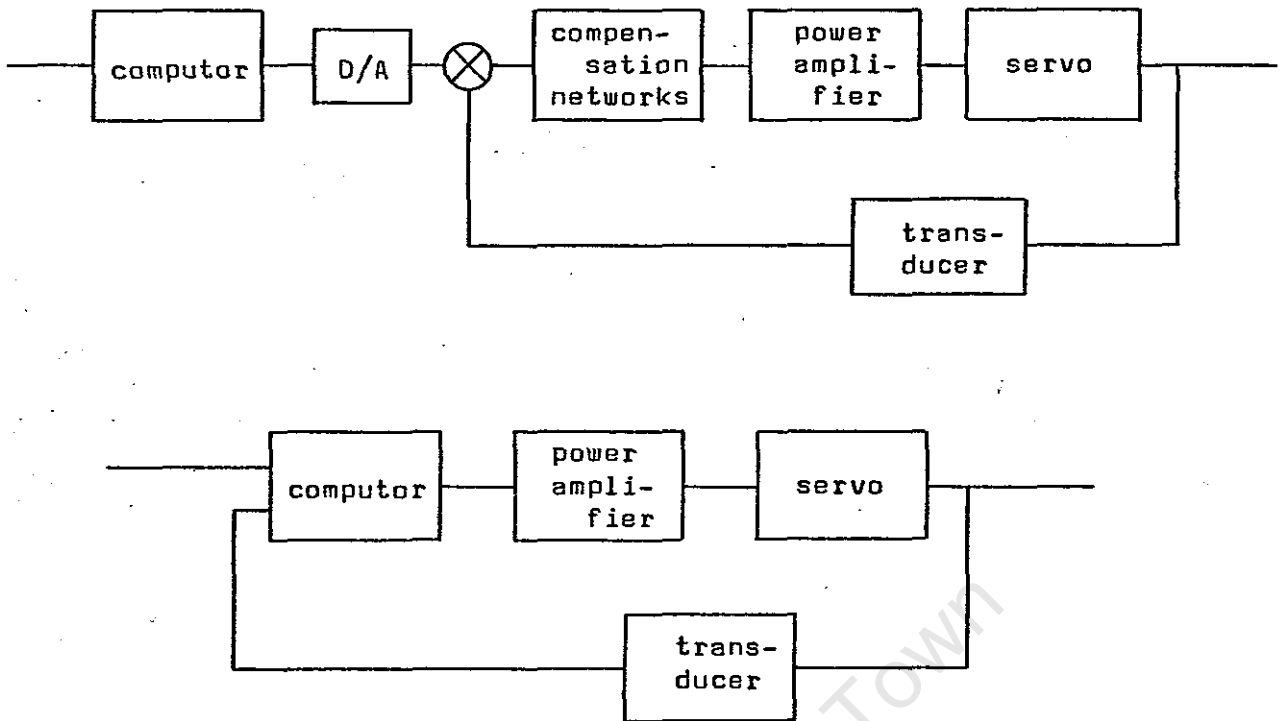


FIGURE I

The upper diagram shows how one of several servo control systems would be controlled by a computer in systems currently in use. The lower diagram shows the system which is to be developed.

The research can thus be divided into three broad groups:-

- (a) Development of a digital interface between the computer and thyristor bridge (hardware).
- (b) Development of a computer programme suitable for the control of the machine.
- (c) To look at different tachometers to find which type is most suitable for use with a computer.

A D.C. speed control system was chosen because the thyristor control of a D.C. machine is already fairly common and the design techniques and behaviour of thyristor controlled D.C. machines is fairly well known. A dynamic load was chosen because this would bring to light any further problems that might be encountered with this method of control.

A block diagram of the system used is shown in Figure 2.

The computer used is one designed for this sort of duty and has eight kilowords of random access memory with an instruction execution time of 1,8 microseconds. This controls through the interface to be designed and built, a three phase thyristor bridge. The bridge thus

supplies D.C. power of variable voltage to a separately excited shunt wound D.C. motor, the speed of which is fed back to the computer via a tacho-generator. The tacho signal and the control set point are fed into the computer via an analogue to digital convertor.

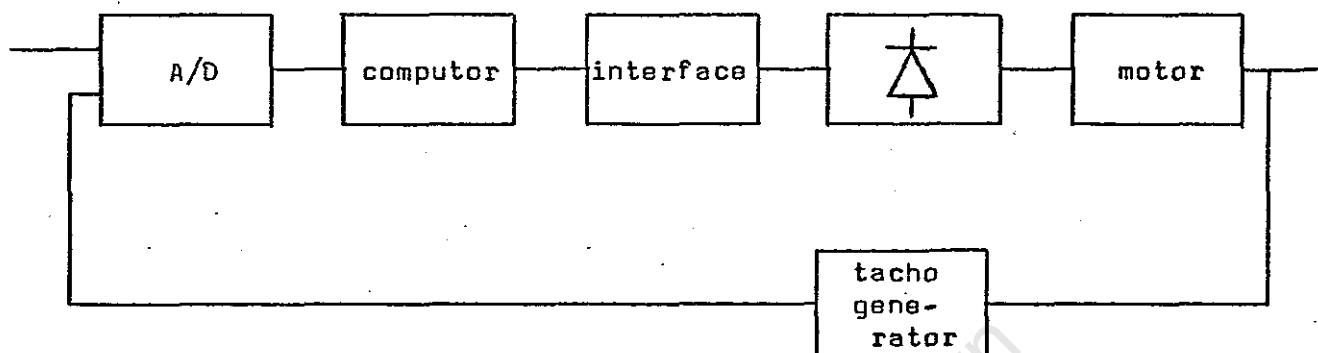


FIGURE 2

Detailed block diagram of system to be developed.

C H A P T E R I IDESIGN OF THE FIRST INTERFACE

Use of a computer to control thyristor banks has been investigated before, notably by Fallside & Farmer³ and also by Rodd¹⁶ but in both cases the computer was fed detailed information about the three phase supply and then the computer had to decide which thyristor to fire. This involved fairly complicated interfacing and a lengthy computer program, keeping the computer occupied for a fair time. This resulted in a very expensive, though highly accurate, setup with limited application. For this thesis, it was decided to do all the thyristor addressing external to the computer thus simplifying both the hardware and the software which now only had to calculate and provide the firing delay. Thus the function of the interface is to detect when it is possible to fire the next thyristor, inform the computer of this fact and remember which thyristor is to be fired. When it receives the command from the computer to fire a thyristor, it must enable the appropriate trigger circuit.

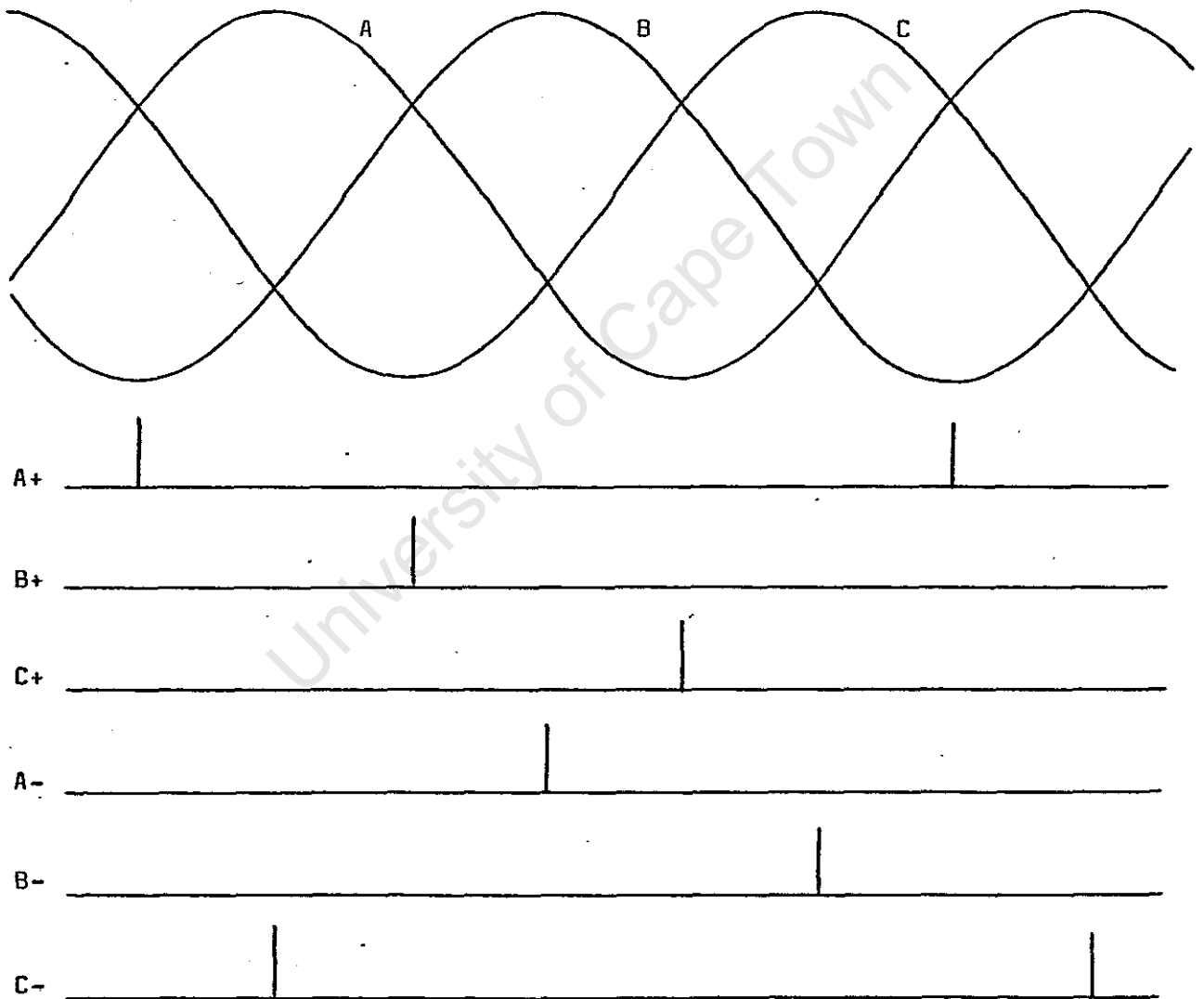
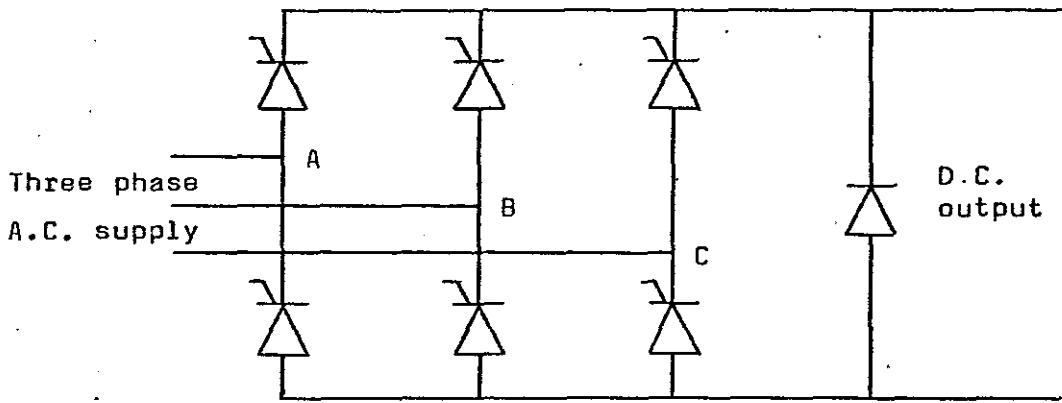
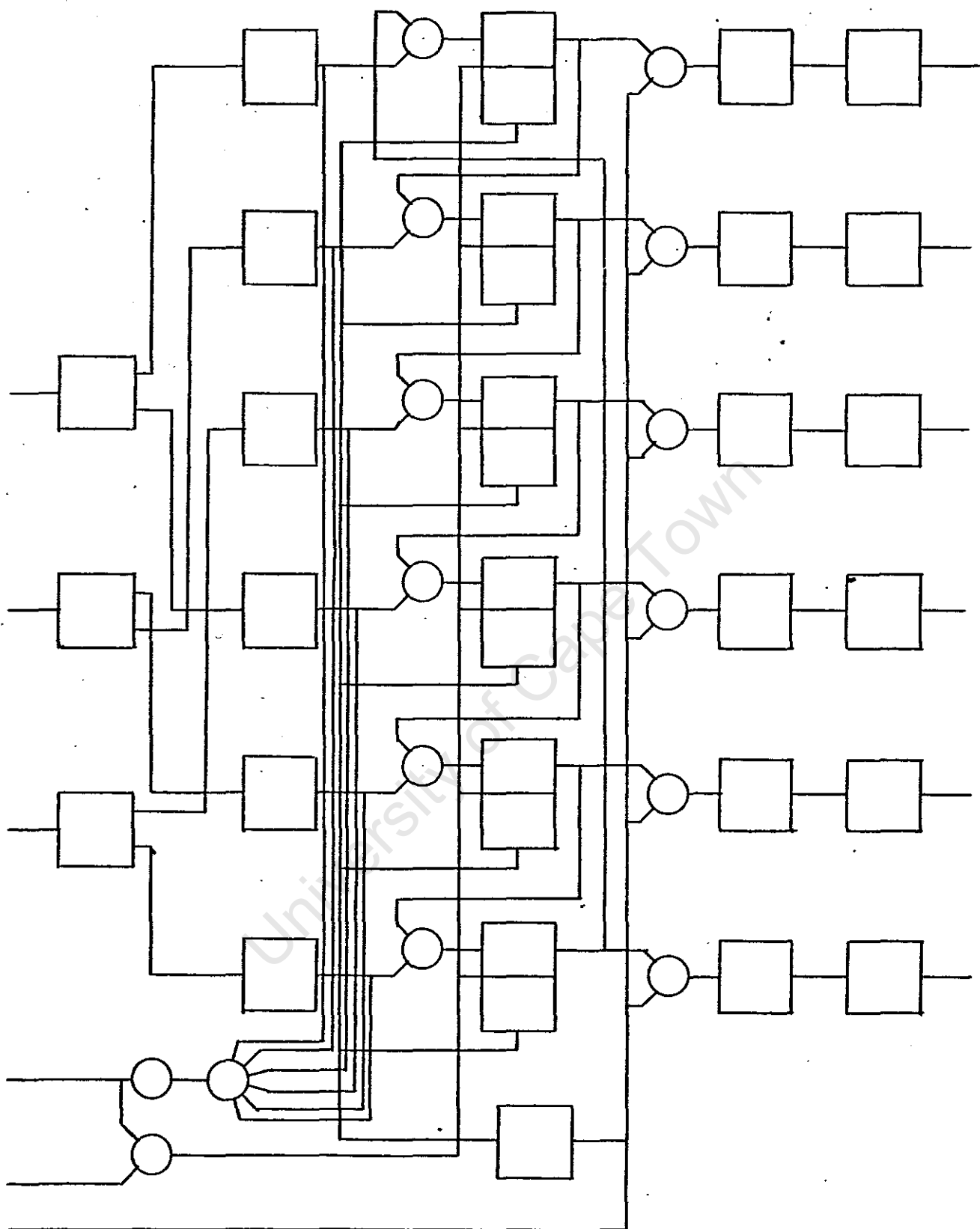


FIGURE 3

- (a) The thyristor bridge used.
- (b) Waveforms of three phase supply.
- (c) Pulses generated by crossover detectors.

Consider the waveform in Figure 3 (b). Assuming the maximum D.C. voltage is required, every time a positive and rising phase voltage exceeds that of a positive and falling phase voltage, a thyristor connected to the positive D.C. rail must be fired. A similar set of conditions applies to a thyristor connected to the negative D.C. rail. Pulses indicating these crossover points supplied by the interface to the computer are shown in Figure 3 (c). If less than the maximum voltage is required, these pulses must still be supplied to the computer telling it when to start the delay count-down for delayed firing of the thyristor. This works very well up to a maximum firing delay of $\frac{\pi}{3}$ radians (60°) at which point another crossover occurs. However, to produce minimum voltage a firing delay of $\frac{2\pi}{3}$ radians is required. Thus for delays greater than $\frac{\pi}{3}$ radians, two addresses would be set resulting in incorrect firing of the thyristors. This difficulty can be overcome by address shifting. Since one address must be set and one firing pulse given every $\frac{\pi}{3}$ radians, the address set by the interface must be shifted one place for the longer delay. This is also done under the control of the computer.

The design for the first interface thus consisted of six crossover detectors, each having associated with it a monostable multivibrator. These provide pulses at the crossover points of the three phase supply for the respective thyristors. The pulses from the detectors are fed to a six input OR gate, the output of which is fed to the computer informing it of every crossover point. The individual pulses are also fed to a local memory in the interface which retains the address until the firing pulse is received from the computer. The output of each element is connected to an input of an AND gate while the other input receives the trigger pulse from the computer, thus enabling the correct thyristor to be fired. A block diagram of the interface is shown in Figure 4.



Crossover
detectors

Crossover
monostable
multivibrators

Local
memory

Trigger
control
monostable
multivibrators

Trigger
circuits

FIGURE 4

BLOCK DIAGRAM OF INTERFACE

The various parts of the interface are now considered in detail.

CROSSOVER DETECTORS:

Voltage comparators could have been used for this purpose, but at the time the interface was built these were extremely costly and exhibited a sharp change of state for one direction of voltage change only. For this reason, it was decided to attempt to build a discrete component crossover detector. This could be done only at a cost comparable to the integrated circuit voltage comparator. The main difficulty encountered was to obtain a high common mode rejection ratio for the differential input. Looking again at the voltage waveforms in Figure 3 (b), it can be seen that there is a voltage zero crossing point displaced by an angle of $\frac{\pi}{12}$ radians from every voltage crossover point. It is possible to utilize this point if a phase shift of $\frac{\pi}{12}$ radians is introduced in the reference supply to the comparators. This can be done by utilizing a star-delta transformer, enabling the use of a simple zero crossing detector for this purpose. The sine wave of the mains can readily be approximately squared by the circuit shown in Figure 5 (a), the waveform being shown in Figure 5 (b). The final squaring of the wave can be done by a Schmitt trigger changing state on the positive going voltage at +0,IV and -0,IV on the negative going part of the waveform. The final circuit used is shown in Figure 5 (c).

This circuit gives equally fast changes of state for positive and negative going input voltages. The transition time of the detector was measured to be approximately 60 nanoseconds.

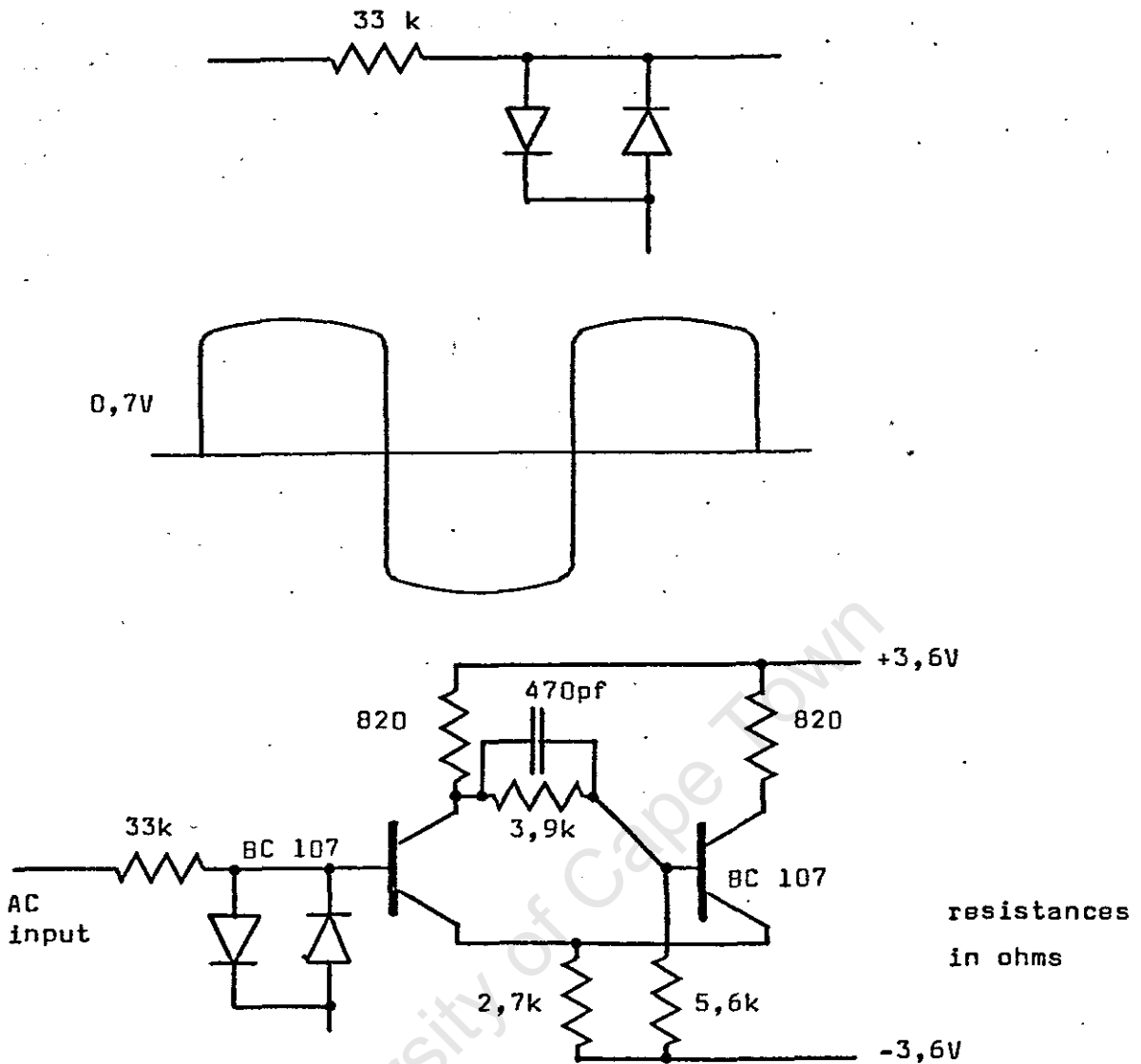


FIGURE 5

- (a) Circuit of voltage squarer.
 (b) Output waveform of squarer.
 (c) Complete circuit of zero crossing detector.

THE MONOSTABLE MULTIVIBRATORS.

These are arranged so that they set the individual memory flip-flops and signal the computer that a voltage crossover has taken place. At the experimental stage, the more conventional collector coupled multivibrator was tried first, but it was found that the shortest switching time obtainable was much longer than the hundred nano-seconds recommended by the manufacturers of the flip-flop used in the local memory¹². Consequently the emitter coupled multivibrator was tried and was found to give much better switching times, comparable to those of the Schmitt trigger used in the zero crossing detector. The disadvantage of having to provide both positive and

negative supplies in order to achieve a near zero output in the stable state is of no consequence in this case because these supplies are already required for the zero crossing detectors. The circuit of the monostable multivibrator is shown in Figure 6.

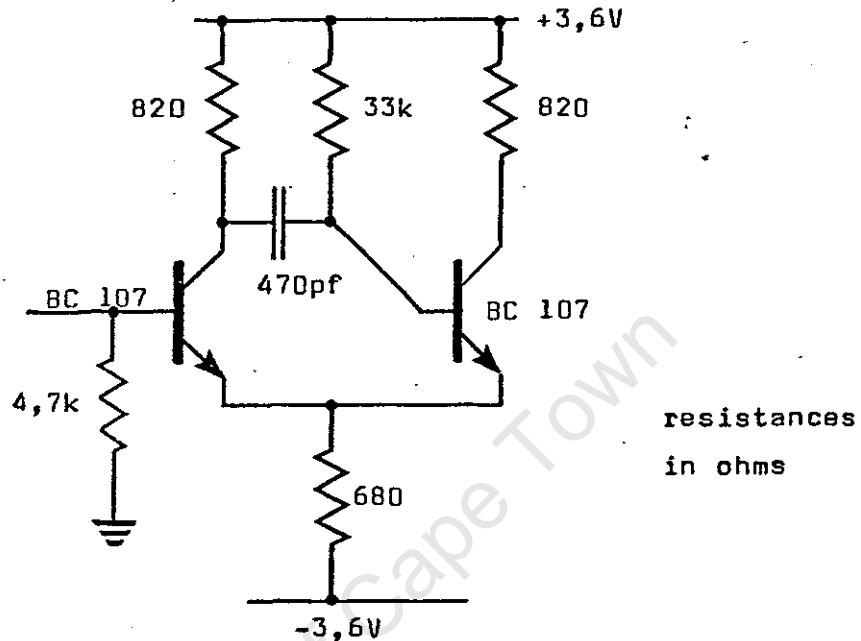


FIGURE 6

Circuit of monostable multivibrator used in conjunction with zero crossing detectors.

LOCAL MEMORY.

The purpose of the memory is to retain the location of the thyristor to be fired while the computer calculates and provides the firing delay. It consists of a set of six J-K flip-flops which are controlled both by the zero crossing monostables and by the computer. When a pulse is received from a crossover detector, the respective flip-flop is set. After the firing pulse from the computer is received it is reset. The memory is wired in the form of a ring counter so that if an address shift is required, it can be done under computer control. The circuit diagram of the local memory is shown in Figure 7, together with the control logic and resetting monostable.

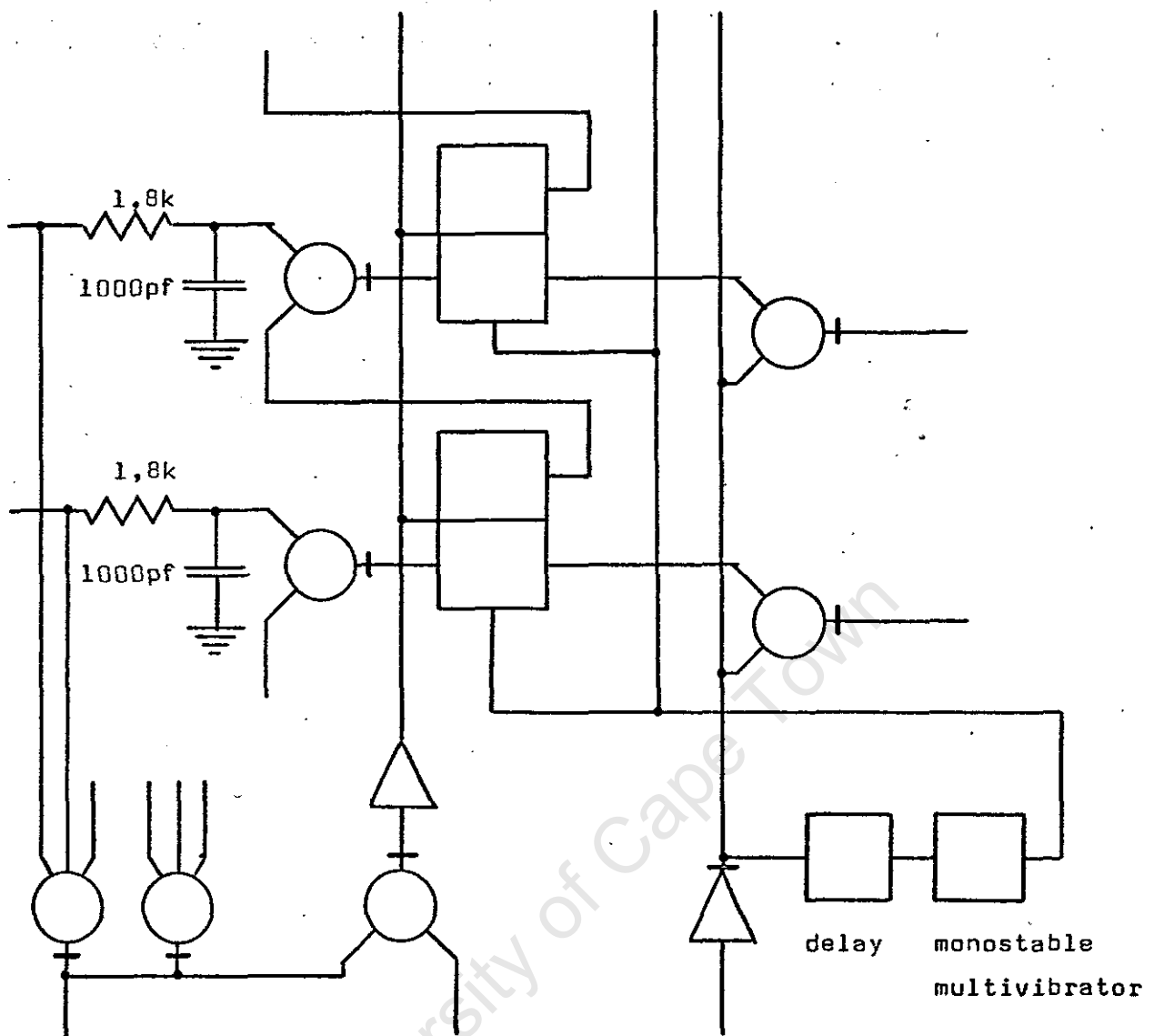


FIGURE 7

Circuit of part of local memory
and its control logic.

TRIGGER CONTROL MONOSTABLE MULTIVIBRATOR.

These monostable multivibrators control the thyristor trigger circuits, being triggered from the AND gates which receive their inputs from the local memory and the line carrying the firing pulses from the computer.

GATE WIDTH OF MONOSTABLE MULTIVIBRATOR.

Although there are six thyristors in the three phase bridge, each one conducts for $\frac{2\pi}{3}$ radians because at least two thyristors conduct at any one time. Since a commutation occurs once every $\frac{\pi}{3}$ radians, there must be a commutation in the middle of conduction period of another thyristor. This may cause the extinction of the thyristor producing discontinuous current flow. To overcome this, the thyristors

may either be given two pulses, one at the beginning of its conduction period and again when the other thyristors commutate, or one pulse long enough to maintain the thyristor in the conducting state over the commutation period. In this case the easier method was to produce a long gate pulse of about 4 ms., sufficiently long to maintain the thyristor in its conducting state through the commutation period starting after 3,3 ms..

The emitter coupled monostable multivibrator was again used because of its superior speed, eliminating any uncertainty due to slow transition times. The circuit diagram is shown in Figure 8.

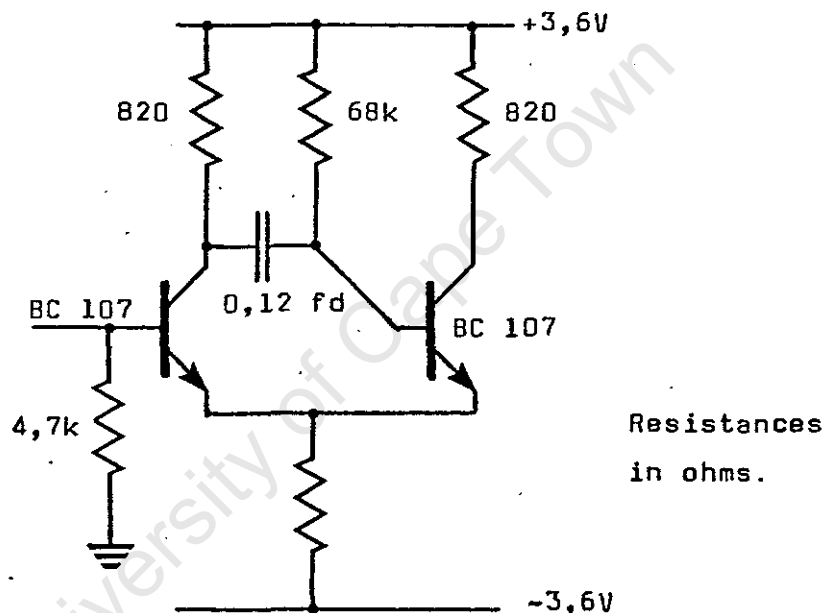


FIGURE 8

Circuit of monostable multivibrator for controlling trigger circuit.

THYRISTOR TRIGGER CIRCUITS.

Thyristors can be triggered in one of two ways ^{8,15}. The first is to apply a D.C. pulse for the duration of the conduction period with the input power kept within the power handling capability of the thyristor gate. The second is to apply a large short duration pulse with the instantaneous power many times that of average power handling capability of the gate.

The first method has the advantage that, if the current in the power circuit of the thyristor is likely to be discontinuous it will

be maintained in its conduction state whereas with the second method of triggering, the thyristor has no gate signal to keep it in the on state if the main current momentarily falls to zero.

When the thyristor is given a short high power pulse, turn on is more reliable and the latching current is reduced. Thus a compromise can be made by inputting to the gate a series of high power pulses for the duration of conduction period of the thyristor. This may cause trouble in A.C. circuits which have inductance, because at the beginning of the conduction period when the current is small, it may not be sufficient to hold the thyristor in the conducting state, thus the thyristor may switch on and off as it receives the gate pulse, causing relatively large current surges in the power circuit. In the case of the bridge rectifier circuit where the output is D.C., current flow is continuous and much larger than the latching current of the thyristor, resulting in immediate turn on at the first trigger pulse.

Of the various types of pulse generator in use, the unijunction oscillator is about the simplest, requiring only one transistor with no power amplification. It has a rather low upper frequency limit for this particular application resulting in a finite delay between the unclamping of the oscillator and the production of the first pulse. Fortunately, this delay is very predictable for any one oscillator.

The circuit of the oscillators used is shown in Figure 9, there being one oscillator per thyristor. The first transistor Q, acts as a switch to start and stop the oscillator and is controlled by the trigger control monostable. The pulse transformer has a ratio of 1:1.

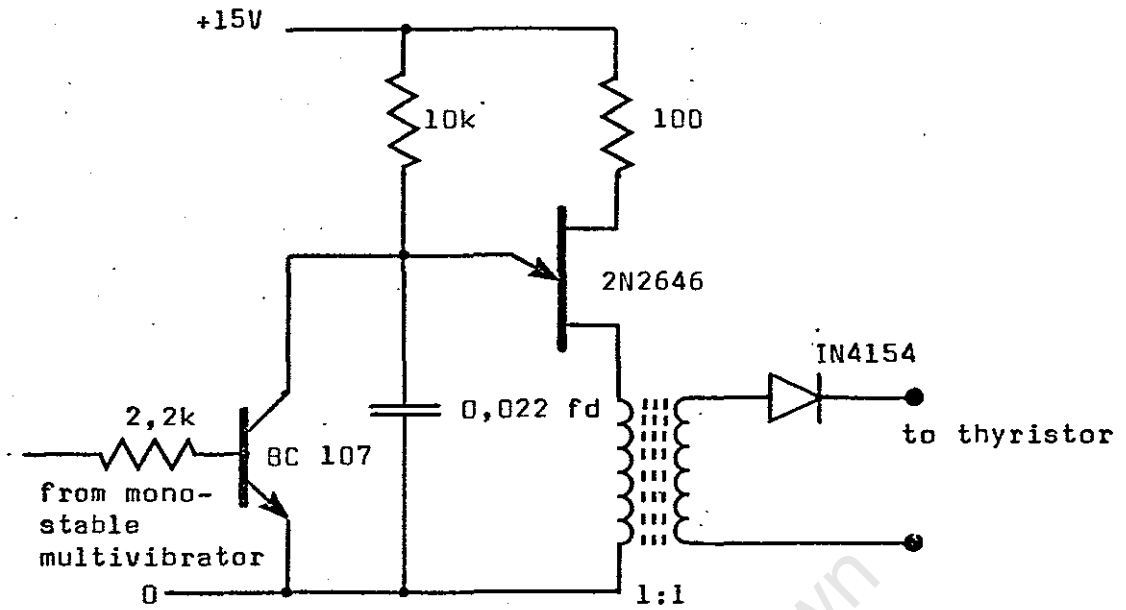


FIGURE 9

Trigger circuit for controlling thyristors

CONTROL LOGIC.

There remains just the monostable multivibrators which provide the delay and resetting pulse for the flip-flop once the firing pulse has been received. The delay is introduced so that a definite pulse of about 2 sec., is given to the trigger control monostables. The circuit diagram is shown in Figure 10. The timing pulses for the interface are shown in Figure 11.

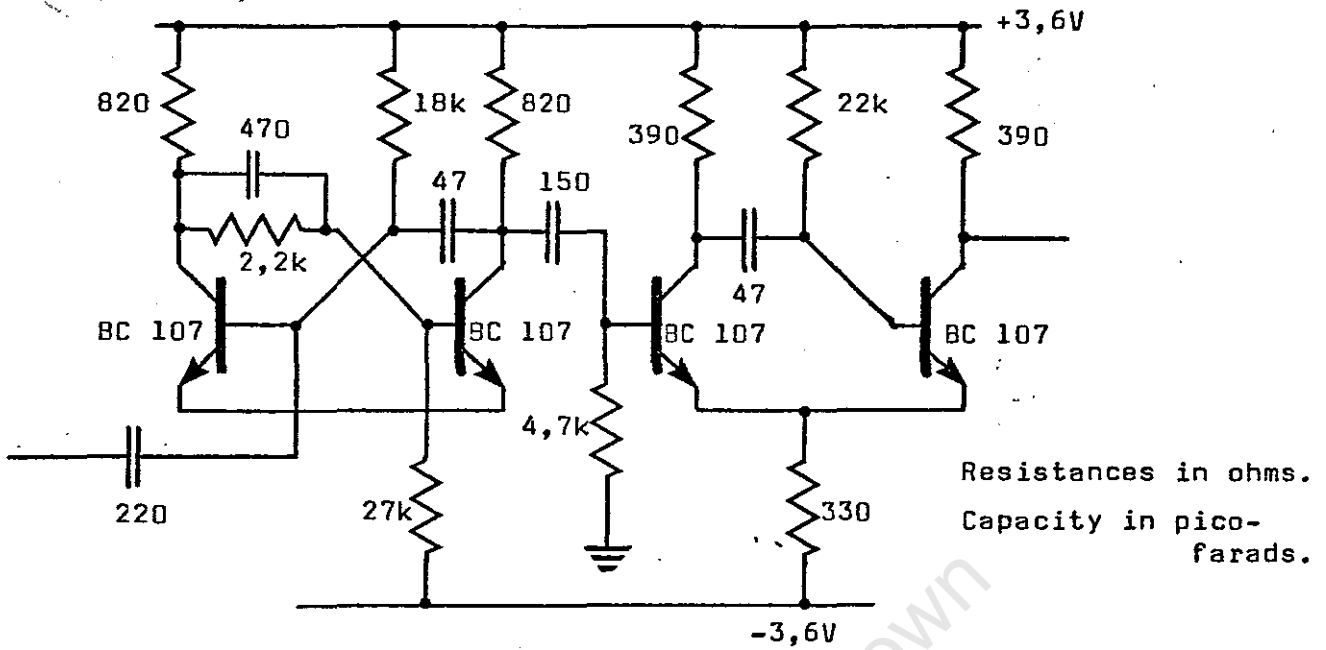


FIGURE 10

Circuit used for resetting local memory after occurrence of firing pulse.

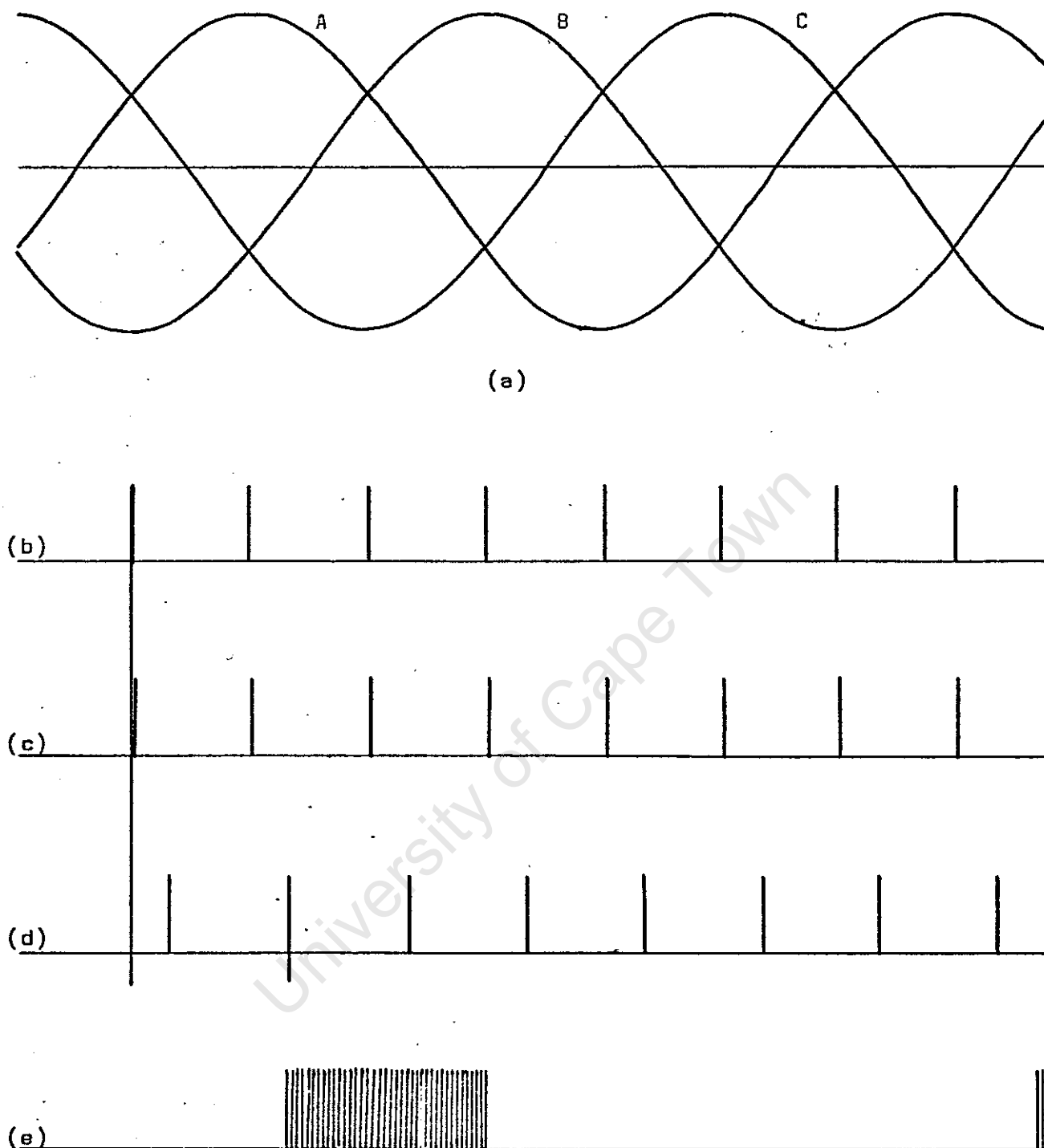


FIGURE 11

Timing pulses for interface

- (a) Voltage waveform of three phase supply.
- (b) Pulses supplied to computer from crossover detectors.
- (c) Shift pulses generated by computer if address shift is required.
- (d) Trigger pulses generated by computer after appropriate time delay.
- (e) Trigger pulses for thyristor connected between phase A and positive D.C. rail.

CHAPTER IIITHE COMPUTER:
CONNECTING IT TO THE SYSTEM

This chapter will briefly describe the operation of the computer and methods of inputting and outputting information.

THEORY OF OPERATION:

Information on the general principles of operation of a digital computer is readily available^{1,6,9} and will not be dealt with here. This section will describe how the computer is connected to its peripherals and how information is transferred between them.

All information inputted to and outputted from the computer goes via a bus consisting of eighteen lines called the E bus. Since the computer used has an eighteen bit word length, there is one line available per bit. Each peripheral device connected to the computer has a digital circuit associated with it usually mounted on one computer card. This circuit is connected to the E bus and to several of seven further control lines. All these circuits are controlled directly by the computer under program control, with the peripheral devices responding when interrogated by the computer. There is one exception to this where data transfer can be initiated by the peripheral device and thereafter control is transferred to the computer. This is the Direct Memory Access facility, but since this facility is not used in the present application, it will not be discussed any further.

If the peripheral device can perform a number of operations, the first instruction communicated to it before a data transfer is usually an External Control instruction (EXC) which sets up the logic for the device to perform a specific function. The next is a Sense instruction (SEN) which causes the computer to interrogate the peripheral device ascertaining its state of readiness for a data transfer. When the device is ready the computer can execute an instruction which causes data to be transferred between it and the peripheral device. Each device has a number by which it can be addressed. Thus, if the high speed paper tape reader has to be started, the instruction EXC 537 must be executed. The last two digits of the instruction form the address while the "five" commands the reader to start when the instruction is given.

Another means of communicating with the computer is via the interrupt facility. This is not really a method of data transfer but if the computer receives a signal from the interrupt controller, it interrupts the program currently being executed and branches to another program which services the interrupt.

FUNCTION OF THE COMPUTER IN THE SYSTEM.

The function of the computer is simply, upon receiving an indication that a voltage crossover of the three phase supply has occurred, to calculate the firing delay of the thyristor bridge required to give an output determined by parameters fed to the computer from external equipment.

In the case of D.C. machine speed control, the parameters are the desired speed of the machine and the actual speed determined by means of a tachogenerator.

INDICATING THE OCCURENCE OF A CROSSOVER.

The crossover points of the three phase supply are detected by the interface and are indicated by voltage pulses.

These signals can be detected by the computer in one of three ways:-

- (i) By means of the analogue-to-digital convertor.
- (ii) By means of the sense lines.
- (iii) By means of the interrupt facility.

If the analogue-to-digital convertor was used, a crossover detector would not be required as a low voltage replica of the main supply could be fed direct to the convertor. This system is of little use in this case owing to long conversion time of the order of 50 sec. of the convertor. This will introduce a random error of at least 50 sec. into the detection of the crossover point. Another disadvantage of this system is that the computer will spend a large amount of its time waiting for the convertor while it could be doing more useful things.

In the second method, the accuracy is greatly improved. Here a crossover detector would be required. The sense line in this case is essentially the same as the sense facility used when the computer interrogates a peripheral device, but in this case the line is brought out of the computer and there is no actual data transfer. The line can be interrogated approximately once every 10 sec. which is a great improvement, although the computer still has to waste a large amount of time interrogating the sense line. What is needed is a facility whereby the computer can be busy with one task up to the point in time

where a crossover occurs, then it can perform the required operations to fire the next thyristor and return to its previous task. Such a facility is offered by the interrupt module, the computer taking action within 1,8 sec. of detecting the interrupt, this interval being the cycle time of the computer. Because of its obvious advantages, it was decided to use this method of indicating the voltage crossover points.

SET POINT AND TACHOGENERATOR INPUTS.

As only analogue tachogenerators were available in the department, it was decided to make use of these, leaving the development of a digital tachogenerator to a later thesis. Thus, this signal being analogue in nature, it was necessary to use an analogue-to-digital convertor to transfer this information into the computer.

Since a convertor had associated with it a ten channel multiplexer, it was decided, for convenience, to input the speed set point via the convertor thus using an analogue voltage reference signal.

OUTPUT SIGNALS.

The output from the computer is in the form of trigger pulses to the interface. These pulses can be derived from the computer by using the External Control instruction available on the E bus. A computer interface card has been constructed where eighteen flip-flops, which can be connected to external equipment, can be set in either the high or the low state under program control by the use of the External Control instructions. Thus a pulse can be generated by setting the required flip-flop high and then low under program control.

C H A P T E R I V

THE C O M P U T O R : ITS P R O G R A M

This chapter will briefly describe the program used for checking the interface and for the first experimental runs. Two forms of compensation are also considered.

For the initial runs the program was kept simple and was divided into two sub-programs, the decision as to which program was to be used being taken by a third supervisory sub-program.

The first sub-program was basically an open loop program which was used when a change in set point was detected. Its purpose was to calculate a suitable delay from a given set point and to store this memory such that it was accessible to other parts of the program.

If the set point remained fixed for a certain time, control would transfer to the second sub-program which offered closed loop control. The behaviour of this program was analogous to that of an integrator. It would alter the firing delay according to the difference between the tachogenerator voltage and that of the set point.

The supervisory program also had to decide whether to provide the delay and firing pulse and then calculate the new delay, or vice versa. The reason for this was that the computer took about a millisecond to execute the above program which is approximately a third of the time between interrupts (3,3 milliseconds) thus the dynamic range of the firing pulse would be restricted to two thirds of the time between synchronization pulses, if the computation and firing sequences were not switched. It may be argued that as the change in effective D.C. voltage is small in the first millisecond of delay, the delay calculation may be done first and then a shortened delay countdown initiated after this; but as the full range of the delay is 6,6 ms., there would be a period between 3,3 ms. and approximately 4,3 ms. where the computer would be unable to deliver a trigger pulse as it would be executing the control program, which it is called upon to do every 3,3 ms. by the crossover detectors. This would occur where the rate of change of output D.C. voltage of the controlled bridge rectifier with respect to the triggering delay of the thyristors, is a maximum, resulting in a step of approximately 17% of the maximum rated voltage. This is unacceptable as it would cause large current surges to flow in the load circuit if this is, for instance, a D.C. shunt motor. A certain speed range would

also be unavailable to the motor.

Thus the supervisory program would decide on one of four sequences of operation by taking the previous delay value and calculating between which of five values it lay. The four operation sequences are shown in Figure 12, together with the delay figures between which they operate.

The last part of the program was the delay countdown routine which accessed the memory location containing the latest delay, placed the value in one of the registers and then decremented the contents of the register every computer cycle until it reached zero; whereupon it called the routine which gave the firing pulse to the local memory.

The entire program described above was executed every time the computer received an interrupt following a voltage crossover detection.

Another form of compensation which was considered initially was a form of differentiating feedback. When the set point was held constant, the computer would observe any change in the tachometer reading and from the rate of change of speed, alter the firing delay of the thyristors to try to minimise any speed deviation of the motor. It was hoped that the computer controlled system would be less prone to the influence of noise in the signal than its analogue equivalent, but this is not the case.

As shown in appendix (3), the noise in the tachogenerator readings is three to four times the maximum rate of change of the true speed readings when full load is placed on an unloaded machine, so this form of compensation was abandoned.

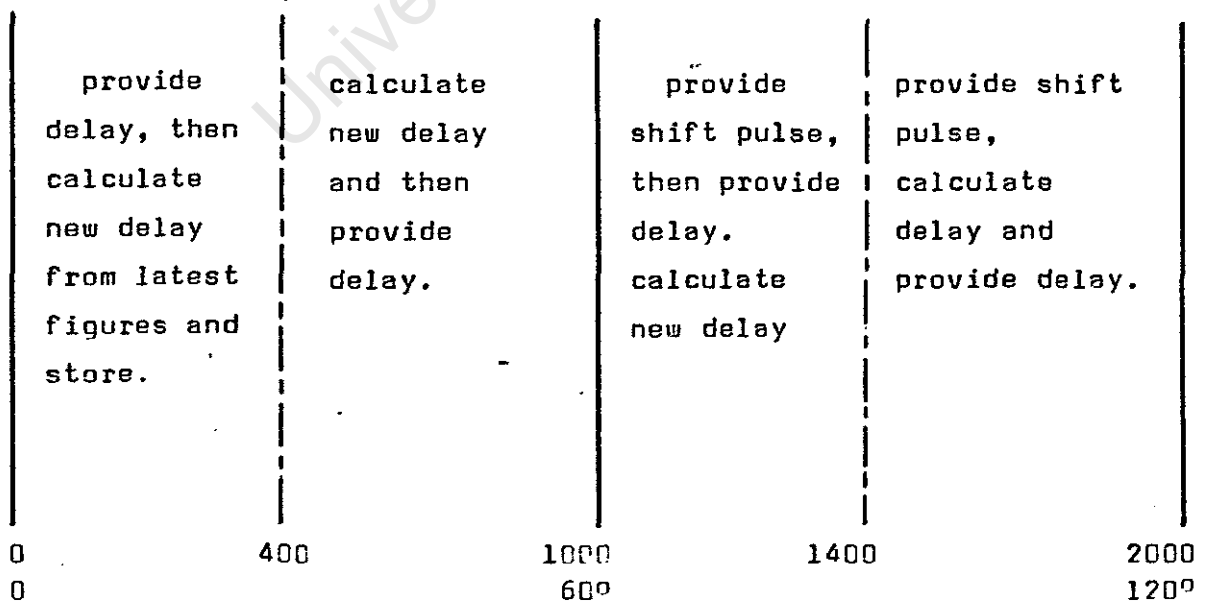


FIGURE 12

The four possible operation sequences which can be performed by the computer

C H A P T E R V

THE ANALOGUE TO DIGITAL CONVERTOR AND TACHOMETERS

The analogue to digital convertor used was of conventional design. It was a twelve bit convertor with a bi-polar input of $\pm 10\text{v}$, giving a bit resolution of $4,8\text{mv}$. Although this gives an accuracy far greater than that required, it was hoped that rate of change of speed could be observed, allowing differential feedback compensation. However, tests showed that this was not possible owing to noise problems. (See Appendix (3)).

To enable the convertor to digitize waveform with maximum accuracy, a sample and hold device is used in front of the convertor. This is necessary because the convertor takes a finite time to perform its conversion and if the waveform being observed has high frequency components, its magnitude could have changed appreciably by the time the conversion is complete, giving an erroneous reading of the voltage. Thus when a digital reading of an analogue voltage is required, the sample and hold samples the signal and then maintains that voltage while the convertor executes its conversion. This configuration, unfortunately, is now very susceptible to noise, because the sample and hold may take its sample at the instant a stray voltage spike due to noise occurs thus causing an erroneous reading.

TACHOMETERS.

The tachogenerators tested can be divided into two groups: A.C. types and D.C. types.

Two types of A.C. tachos were tried. The permanent magnet rotor type and the induction generator. The permanent magnet type generator was found to give a good clean waveform. The A.C. signal was rectified and smoothed before being applied to the analogue to digital convertor. In order to have a filter time constant sufficiently short (one tenth motor time constant) so as not to introduce a lag in the tacho voltage reading, the number of poles in the generator had to be large in order to obtain a fairly high output frequency. A 32 pole generator giving 400 Hz at 1500 rpm proved to give very satisfactory results.

A point to note with this type of tachogenerator is that the output ripple of filter is independent of the motor speed as the ripple factor of the output voltage is inversely proportional to frequency while the voltage is proportional. i.e. if f is above the breakpoint

of the filter: $F = \frac{k}{\omega}$

where F = ripple factor

k = proportionality constant

ω = frequency, rad/sec, and is directly related to the speed of the tachogenerator.

and $V = k\omega$

where V = output voltage of tachogenerator

k = proportionality constant

ω = as before

now $R = VF$

where R = ripple voltage

$\therefore R = k\omega \times \frac{k}{\omega} = k k = \text{constant}$

The A.C. induction generator has a drag cup rotor with two windings in the stator electrically at right angles to each other. One winding is excited from a 400 Hz A.C. supply. The second output winding gives a certain fraction of this input voltage, proportional to the speed of the generator. Thus:

where $E_o = KE\omega$

E_o = output voltage

K = proportionality constant

E = input voltage

ω = speed of rotation of generator.

This tacho, which is a highly accurate instrument, has the complication of requiring a separate stable 400 Hz supply upon which the accuracy of the instrument is dependant.

With rated input reference voltage, the generator gave an output of about 3v per 1000 rpm into a load of 10 k . This required at least two operational amplifiers to provide a satisfactory signal for the convertor. The first provides the load for the tachogenerator and also acts as a buffer driver for the rectifier immediately following it. To obtain as low an output impedance as possible, this was used as a unity gain amplifier. The second operational amplifier provided the gain required to supply 10 volts to the analogue to digital convertor when the machine was running at 1500 rpm.

The type of D.C. tachogenerator tried can be divided into three

groups:-

- (i) the conventional D.C. tacho with permanent magnet field and wound armature,
- (ii) homo-polar and
- (iii) printed circuit types.

The conventional D.C. tachos gave a fairly high output voltage of from 3V to 60V per 1000 rpm.. The output signal of this type contains a large amount of commutator noise. Tacho's which have a large number of commutator segments give a cleaner output signal than those with fewer segments but noise amplitude is still of the order of two volts at all speeds.

Two types of homo-polar tachos were tried; one with a rotating permanent magnet field¹⁴ and the other with an energised stationary field. The version with the rotating field magnet had the advantage that no spurious voltages could be introduced into the output signal owing to the shaft vibrating in its mountings as the field would move with the shaft. The main drawback of this tacho was the extremely low output voltage being of the order of a millivolt because of the low flux density of the field magnet and lack of an iron circuit. The brush noise in this instance was a few orders of magnitude larger than the D.C. signal.

The stationary field homo-polar tacho produced a fairly clean signal of about 0,07V per 1000 rpm. but this again, has the complication of requiring an external supply to energise the field. The output signals of both types also need further amplification before being fed to the analogue to digital convertor.

A small printed circuit motor was tried as a tachometer. In this machine the armature consists of a disc of insulating material with the windings formed on it in a radial pattern as shown in Figure 13.

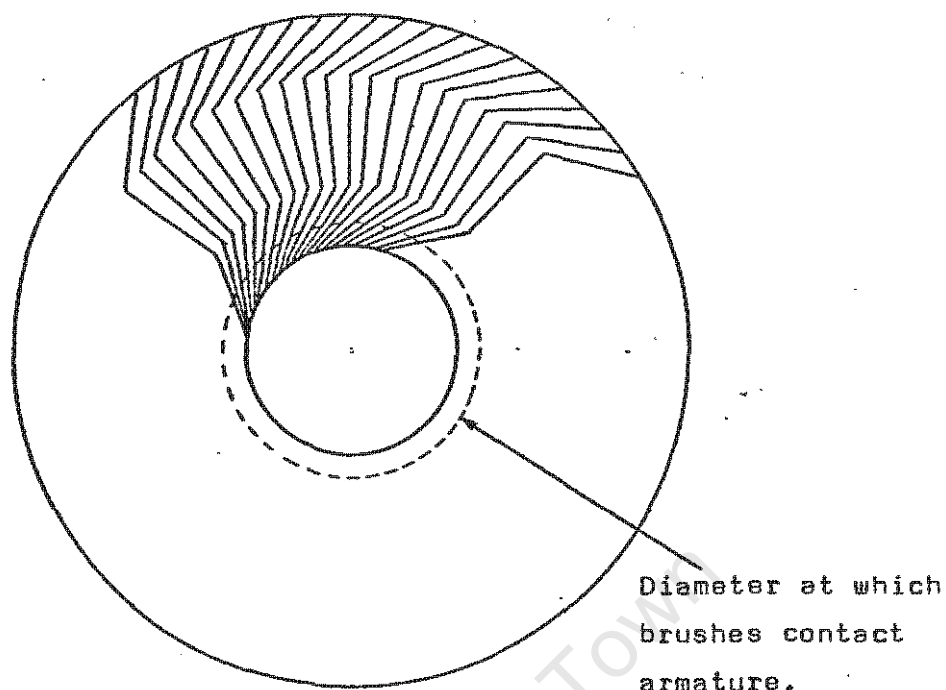


FIGURE 13

Schematic of armature of printed circuit motor

The brushes run on the side of the disc directly on the windings, thus giving a large number of "commutator segments".

It was hoped that this would reduce the commutator noise but when this motor was run as a tacho, it was found that the output voltage varied with the angular position of the armature. Thus a fluctuation in the voltage of about 5% occurred when the tacho was driven at constant speed.

From the above it can be seen that of the A.C. tachos, the permanent magnet rotor type gives the most easily utilized signal, while of the D.C. tachos, those of good quality and conventional design, are the most practical. Both of these types were used in the actual system, giving equally satisfactory results.

In connection with the mounting of the tachogenerator, it was found almost impossible with the equipment available to eliminate a modulation in the output signal caused by slight eccentricities in the coupling between tacho and the motor whose speed was to be measured. The rate of change of voltage introduced by this is comparable to that encountered due to speed variations in the motor caused by load fluctuations. Therefore, it would be very difficult to observe

instantaneous speed changes of the motor with an analogue system. If a digital system were used it would be possible to feedback the position of the motor shaft in addition, and the computer, knowing the inaccuracies of the digital tacho, would be able to calculate the exact speed of the motor.

University of Cape Town

C H A P T E R VI

THE FIRST EXPERIMENTAL RUNS

When the testing stage was reached, as many of the functions of the interface as possible were tested before being connected to the computer. The next stage was to run the computer and interface together to fully check out the interface and to debug the computer program. The interface performed satisfactorily, but trouble was experienced with the firing delay calculation program. The relation between the D.C. voltage and firing delay angle of the thyristors is trigonometrical and in order to avoid a complex calculation, each time the computer interrupt was serviced, a piecewise linear approximation of five segments was used. Because the slopes of these segments could only be matched approximately, a voltage jump occurred each time a new formula was used for the different section of the curve. This was much greater than expected, so the five segment approximation was dropped in favour of a three segment one which was much more easily implemented in the computer.

Owing to inaccuracies in the delay time calculation program and to variations in the supply frequency, it was found necessary to put limits on the delay in each half of the firing delay range as shown in Figure 14.

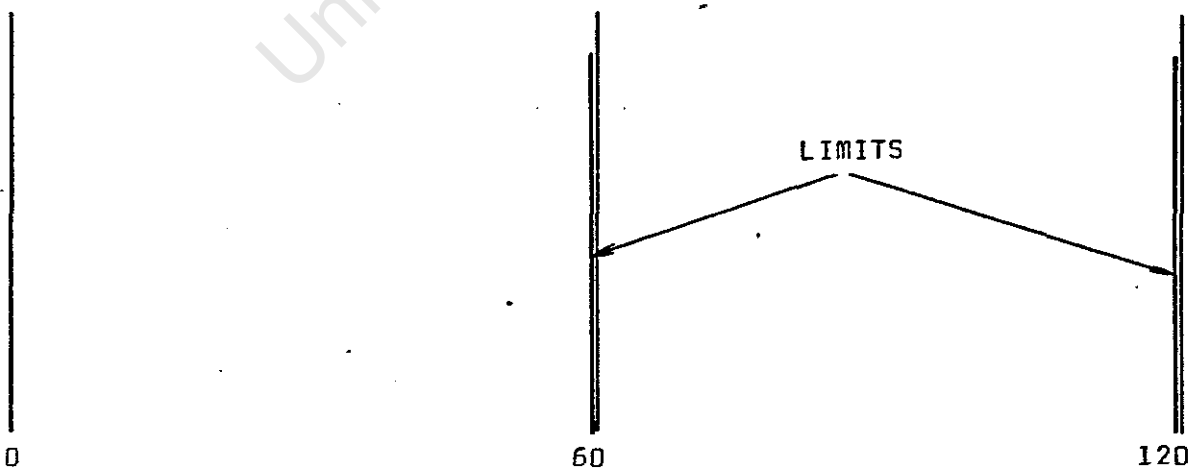


FIGURE 14

The limits placed on the triggering delay to avoid
the loss of detection of an interrupt.

In order not to miss an interrupt, the computer had to be ready to receive it slightly before the end of each half delay period, thus it was required to have finished its delay countdown and given the firing pulse to the interface before the next interrupt was received. This makes it impossible for certain delay times to be realised, causing a voltage jump in the output of the bridge rectifier as the set point is linearly increased. It will be shown later these limits proved to be the downfall of the system as it was then operating.

When the thyristors were connected to a light load and voltage applied to them, it was found that they were firing very erratically. Thinking that the current was perhaps too small for the thyristors to latch into the on state, the load was increased but this brought about no improvement.

Consider for a moment the operation of a three phase thyristor bridge. As can be seen in Figure 15, two thyristors are in the conducting state at any one time.

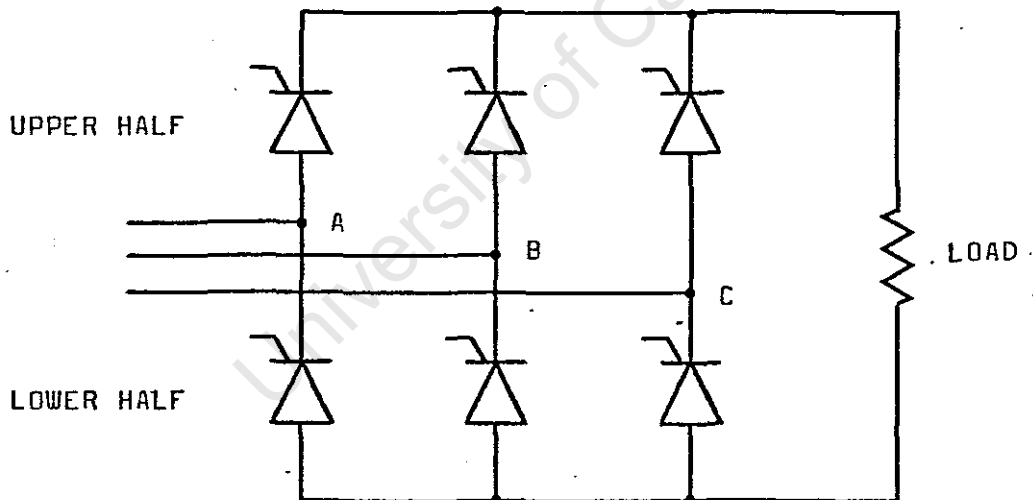


FIGURE 15

The three phase thyristor bridge. When current flows in the load one thyristor in each of the upper and lower halves of the bridge must be in the conducting state.

At approximately the mid-point of the conduction period of one thyristor, two others will commutate which may cause current discontinuities resulting in the first thyristor reverting to its blocking state.

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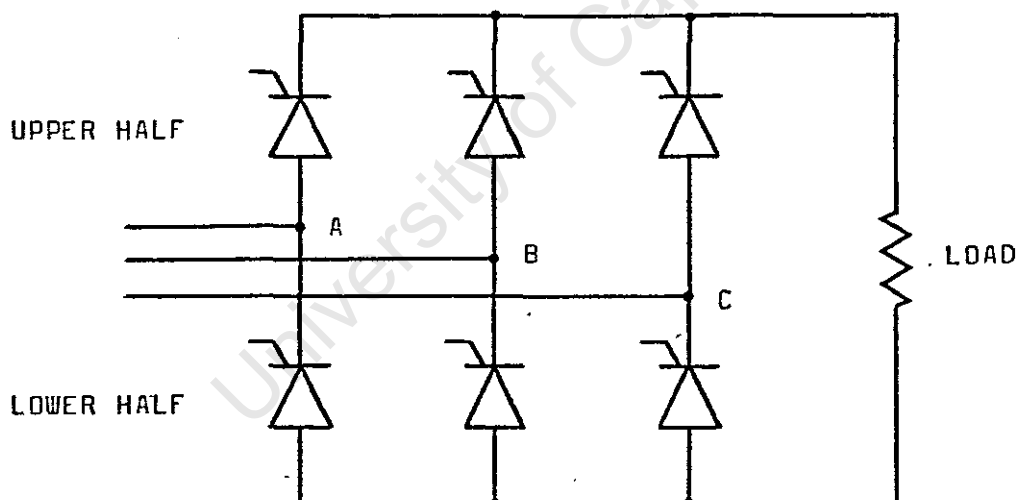


FIGURE 15

The three phase thyristor bridge. When current flows in the load one thyristor in each of the upper and lower halves of the bridge must be in the conducting state.

At approximately the mid-point of the conduction period of one thyristor, two others will commutate which may cause current discontinuities resulting in the first thyristor reverting to its blocking state. To avoid this, trigger pulses are maintained on the gates of

the thyristors until this commutation period has ceased, but because of the low duty cycle of the pulse generators (approx. 1 in 10) the pulses from the different generators may not be present at the gates of their respective thyristors at the same instants in time. This results in open circuit conditions existing in the power circuit and the thyristors fail to turn on. Thus the trigger circuits can either be replaced with a type that is capable of giving synchronous pulses or, as was done in this case, a centre tapped bleeder resistance was placed across the output of the thyristor bridge with the centre tap connected to the star point of the step down isolation transformer. This gave the thyristors a definite load into which to fire independent of any other thyristor.

After this modification had been added, the performance of the system on resistive load was greatly improved, although at two specific values of delay, firing was erratic. The reason for this was that the crossover detectors were changing state several times in the region of the true crossover point as a result of noise being generated by the commutation of the thyristors in the bridge rectifier circuit. The interaction between the detectors and thyristors was reduced by inserting R.C. networks in the supply leads to the zero crossing detectors. However to eliminate the trouble, it was found necessary to supply the interface from a separate three phase transformer.

The next step was to connect the thyristor bridge to a D.C. motor. This was done and the motor was successfully controlled on open loop.

The computer program was written in such a manner that, if the set point remained fixed, the system would automatically change to closed loop control after a delay of about one second. This was done to allow the motor to settle down before closed loop control commenced. When closing the loop was attempted, it was found that it could not be done as there was a large amount of R.F. digital noise present on the input line carrying the set point voltage to the analogue to digital convertor. When the potentiometer controlling the setpoint voltage was heavily screened and an R.C. filter placed across its output, the noise was greatly reduced and it was possible to run under closed loop control.

When the system ran under closed loop control, it was found that the speed would oscillate violently about the setpoint. After limits were imposed on the rate of change of firing delay limiting the rate of change of D.C. voltage to 160V/sec., it was found that the motor would oscillate by about fifty rpm. either side of the setpoint with a period of about 1,3 sec.. At certain values of setpoint voltage, it

was noted that as the output voltage of the thyristor bridge varied, voltage jumps occurred. The cause of this was traced to incorrect limits being placed on the firing delay in the first half of the firing delay range. If this limit was set so that the computer was ready for the next zero crossing interrupt a few microseconds before it came, the system would behave satisfactorily until the mains frequency changed slightly. If it decreased, the voltage step would occur while if it increased, the computer would miss an interrupt thus causing spurious misfiring of the thyristor bridge. To ensure that the misfiring never occurred, it was necessary to adjust the limit such that the computer would always be ready for the interrupt for the highest mains frequency likely to be encountered. As this frequency was encountered only occasionally, it was impossible to avoid a voltage step between the two halves of the delay range. To overcome this difficulty, the computer must know the instantaneous frequency of the mains at all times or it must remain in the countdown delay and at the same time be ready for an interrupt from the interface. The first arrangement would be very difficult to achieve as it is servicing the interface at six times the mains frequency while the second solution is impossible for the computer to achieve as it is basically a serial device, i.e. it can perform only one operation at a time.

A solution to this problem would be to perform the delay countdown external to the computer and have additional logic that can make a decision as to when to give the shift and trigger pulses allowing for the slight uncertainty in the arrival of the zero crossing pulse.

Having the counter external to the computer would allow it to perform the full delay countdown, thus no approximations would have to be made of the interval between zero-crossing to find the reduced firing delay. Some further advantages of bringing the counter outside the computer are that the computer is freed of the countdown routine, reducing the total time it has to service the interface, and freeing it for other jobs, and that the computer is no longer obliged to service the interface at a rate of 300 times a second. If the interface is provided with a buffer memory, the frequency of updating the delay may be greatly reduced and the interface and computer may now run asynchronously.

C H A P T E R V I I

THE NEW INTERFACE AND MODIFICATIONS
TO THE PROGRAM.

It is apparent from the foregoing chapter that an extension to the older interface or a new interface is required. This is to embody the characteristics of the old one, but in addition it must include a delay countdown circuit and logic to control the address shifting of the thyristors for long delays. For this circuit to have a better performance than the countdown loop formed in the computer program, it must execute the full delay, thus eliminating any approximations to be made of the interval between voltage cross-overs. This necessitates the use of two counters because the full delay is equal to twice the interval between voltage crossovers. The operation of the two counters is shown in Figure 16.

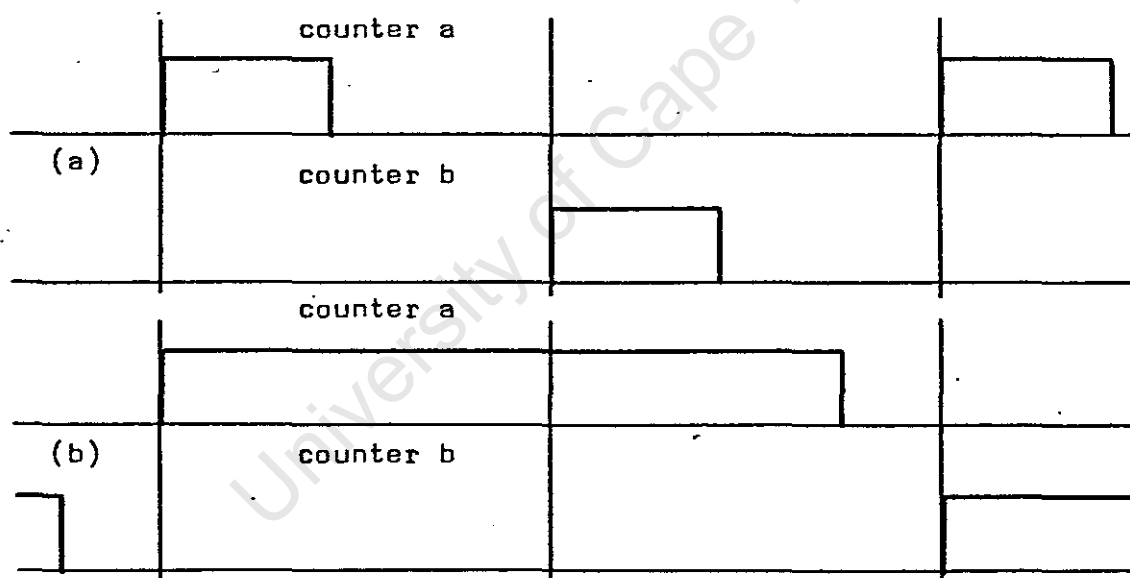


FIGURE 16

Diagram showing sequence of operation of the two counters
for (a) short delays and (b) long delays.

It can also be seen from the diagram that the counter currently in use is still active when the following voltage crossover occurs. If a signal indicating the status of this counter is connected to one input of an AND gate while the other input receives the signals from the crossover detectors, the output of this gate can be used to generate the shift pulse.

Thus no restrictions are placed on the trigger pulse until the instant at which a voltage crossover occurs. If the counter completes its count while the crossover or shift pulses are present, it would be necessary to hold back the signal until these two are completed.

If a completely new interface were built, a more elegant solution would be to have three binary counters each controlling two thyristors. Associated with each counter would be a crossover detector of the type described in Chapter 2. The counter would be triggered every time the detector's output changed state while its absolute state would determine which thyristor would be triggered. This configuration eliminates the necessity of having a local memory and the address shifting facility associated with it. The block diagram for one counter is shown in Figure 17.

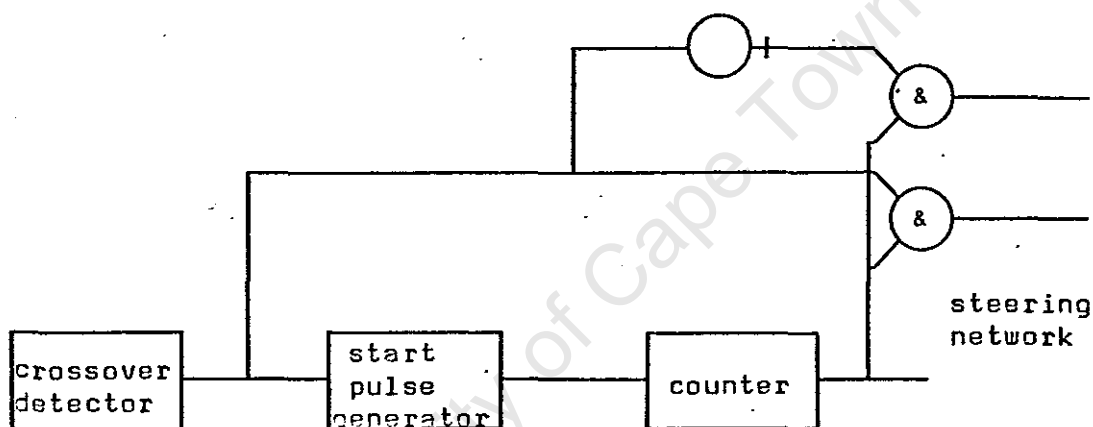


FIGURE 17

Block diagram showing part of the circuit
for interface using three counters

In view of the fact that the first interface already existed, it was decided to build the two counter system, this being added as extra hardware to the first interface. This would give the flexibility of being able to perform the countdown under software control if necessary or of being able to use the external counter.

A diagram of the extension to the interface is shown in Figure 18.

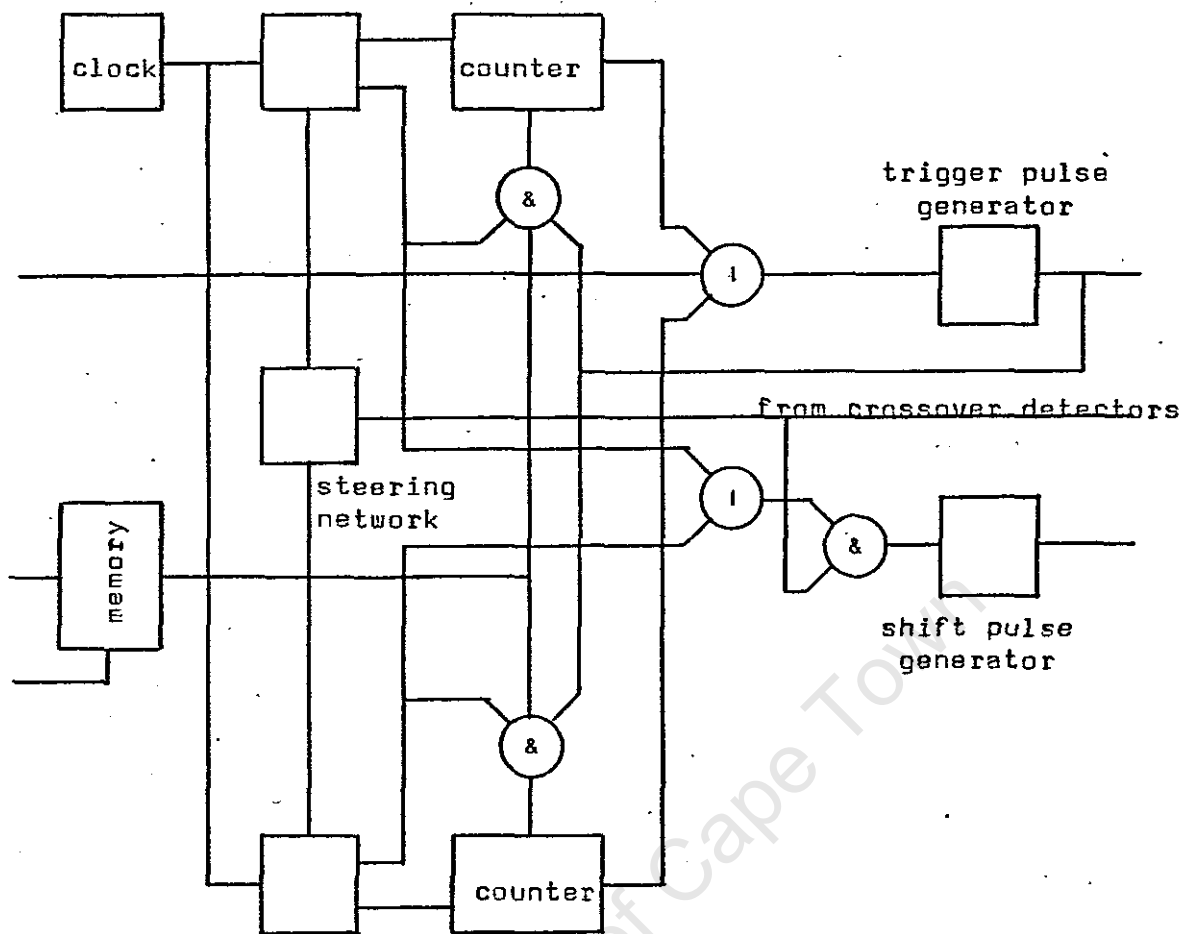


FIGURE 18

Block diagram of extension to the interface

It consists chiefly of two binary counters, a memory buffer and a clock plus control logic. The clock runs continuously, the counters being started and stopped by switches. The counters are started alternately by means of a steering device which changes state at the end of each interrupt pulse. When the counter reaches zero, the switch controlling the clock pulses is automatically opened and, provided there is no shift pulse present, a trigger pulse is generated which is supplied to the interface and also opens the gates between the memory buffer and the counter allowing the latter to be reset. A 'true' signal must also be present from the computer before the trigger pulse can be supplied to the interface.

If a crossover pulse occurs while one of the counters is on, the shift pulse generator delivers a pulse to the interface at the same time inhibiting any trigger pulses which might occur while the address is

being shifted. The memory buffer receives its information from and is controlled by the computer. Its output is available to the counters so that they may be reset to a value determined by the computer.

The binary counters mentioned above have eight bits, this value being chosen as it gave 256 discrete states corresponding to a maximum speed change of 6 rpm. for a machine nominally rated at 1500rpm.. This corresponds to a change of 0,4% which would be just detectable with the instruments available.

THE PROGRAM:

The basic open and closed loop control programs were retained while the supervisory program was changed. Initiation of the execution of the program was transferred from the interrupt facility to the real time clock. The mechanism of operation is very similar to that of the interrupt. In the computer is a variable frequency square wave oscillator, which, under program control, can be caused to generate an interrupt after a predetermined number of integral cycles. In this application it was programmed to give an interrupt every 40 ms., corresponding to a frequency of 25 Hz since the computer was no longer in direct control of the interface, it was decided to bring a digital control signal from the computer to the interface thus returning absolute control to the computer. This line was controlled from the computer console but could also be under program control. For example, if a current level detector was incorporated in the system, the computer could cause a system shutdown using this facility, if current consumption became excessive.

At the time that these experiments were started, there was no hardware available on the computer by which digital data could be transferred to external equipment in parallel form, i.e. no hardware by means of which 'n' bits of data could be transferred simultaneously on 'n' data lines. Thus the External Control (EXC) lines were used. The state of eight lines was sequentially set according to a binary number corresponding to the delay calculated by the computer. A ninth line was used to clock this data into the local memory of the interface, after which the lines were reset under program control. (See Appendix 6).

C H A P T E R VIII

ANALOGUE SIMULATION OF THE SYSTEM

When the system was set up and tried out in the laboratory with the extension to the interface, it was found that there was smooth control of the voltage, the jump at the half delay having been eliminated.

When the system was changed to closed loop control, it was found that the limit cycle mentioned previously still occurred with the new system. At this stage it was decided to try and simulate the operation of the motor and computer. As the computer operated in a discrete time manner, it was thought that analysis would be facilitated by the use of the Z-transform. However, in developing the theory of this transform in the book by Gupta⁷, the frequency content of the pre-sampled and post-sampled control signals of a discrete time system is examined. It is shown that, if the frequency spectrum of the pre-sampled signal can be represented by $U(j\omega)$, then the frequency spectrum of the post-sampled signal can be represented by

$$U^*(j\omega) = \frac{1}{T} \sum_{k=0}^{k=\infty} U(j\omega + j\omega_s k)$$

where ω_s = sampling frequency

The spectrum of the pre-sampled control signal $U(j)$ is shown in Figure 19a.

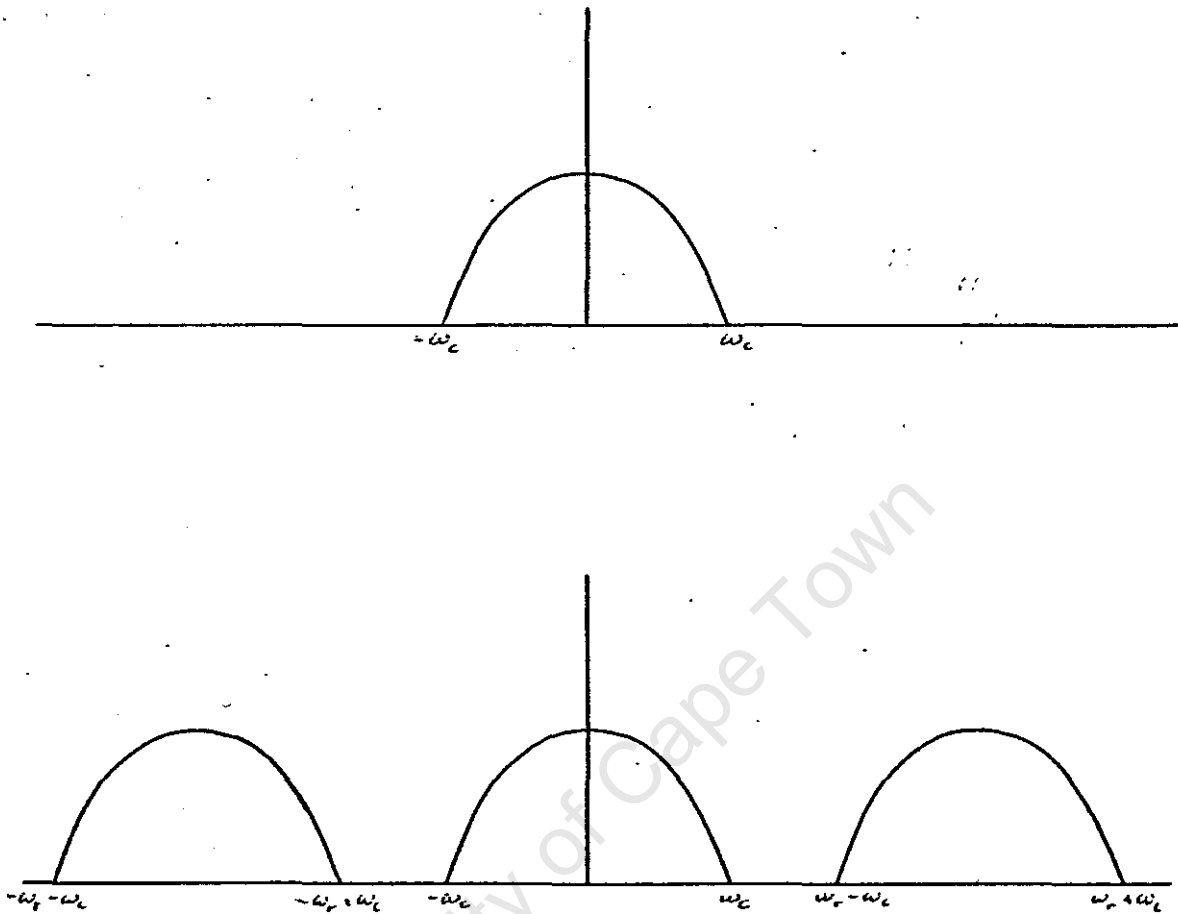


FIGURE 19

The spectrum of the pre-sampled signal is shown in (a) while that of the post-sampled signal is shown in Figure 19(b)

From this it can be seen that the new spectrum contains that of the original plus an infinite number of side components the lowest of which is equal to $\omega_r - \omega_c$ where ω_c is the highest frequency component of the original control signal. In the computer control system just described it would be safe to assume ω_c would not be greater than 10 rad/sec while the sampling frequency ω_r used was approximately 160 rad/sec. Thus the lowest frequency side component likely to be introduced into the system would be about 150 rad/sec. From Appendix 4 it can be seen that the response of the motor would be approximately 60 dB down from the flat response in this frequency region. In view of this it was decided to try and examine the system on the analogue computer simulating the sampler as a pure gain and to use continuous time system compensation techniques.

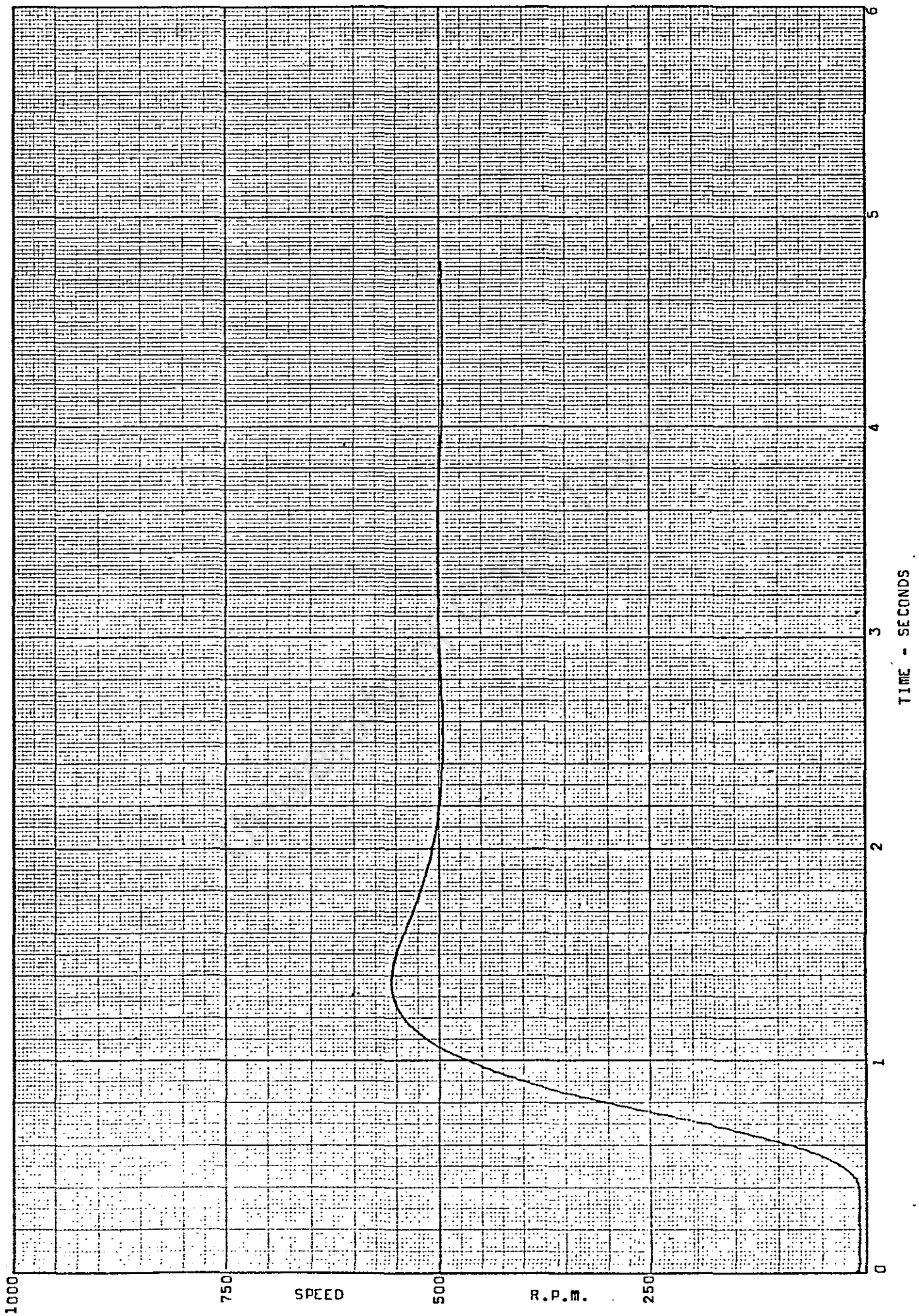


FIGURE 20

To obtain the transfer function of the motor, a transient test was performed by causing an abrupt change in the firing delay of the thyristor bridge. This caused a voltage step to be applied to the armature circuit of the DC motor. The response is shown in Figure 20. Using the curves and equations given in Clark², the transfer function of the motor and series inductance was found to be:-

$$G(s) = \frac{1}{[s+(1,5+j5,05)] [s+(1,5-j5,05)]}$$

When this was simulated on the analogue computer, these values had to be adjusted slightly to give

$$G(s) = \frac{1}{[s+(1,7+j3,62)] [s+(1,7-j3,62)]}$$

as the simulated response was too fast with the damping being less than that of the actual system.

The next stage was to simulate the complete system, i.e. to find the analogue computer equivalent circuit of the digital computer and to simulate the non linearity introduced by the voltage control of the thyristor bridge.

The digital computer program was written such that it noted the control set point, compared it with the actual speed of the machine and modified the firing delay to bring about a reduction in the error between actual and desired speeds. Thus if a constant speed error existed, the firing delay time would change at a linear rate. Thus the computer program could be represented by the block diagram shown in Figure 21.

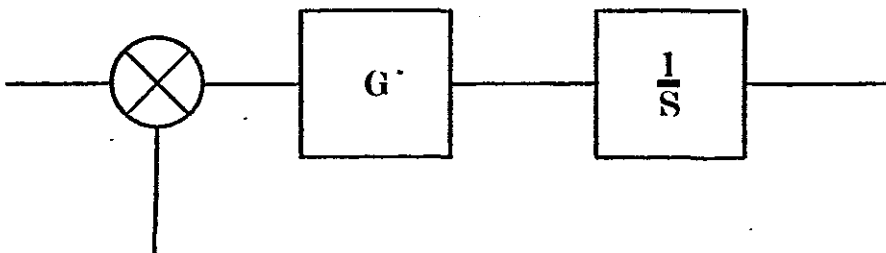


FIGURE 21

Block diagram of the equivalent of the digital computer program

This can be easily simulated on the analogue computer.

For a fixed A.C. voltage the relationship between D.C. output voltage and firing delay angle of the thyristor bridge is not linear but can be represented by the following equations:-

$$\text{For } 0 < \alpha < \frac{\pi}{3},$$

$$E_{dc} = \frac{3\sqrt{3}}{\pi} E \cos \alpha$$

$$\text{and for } \frac{\pi}{3} < \alpha < \frac{2\pi}{3},$$

$$E_{dc} = \frac{3\sqrt{3}E}{\pi} \left(1 + \frac{\cos \alpha}{2} - \frac{\sqrt{3}}{2} \sin \alpha \right)$$

where E_{dc} = average DC output voltage

E = peak AC voltage.

This can be easily represented on the analogue computer with the aid of the variable diode function generator. Thus the complete block diagram of the system is shown in Figure 22a, while the analogue computer setup derived from it is shown in Figure 22b.

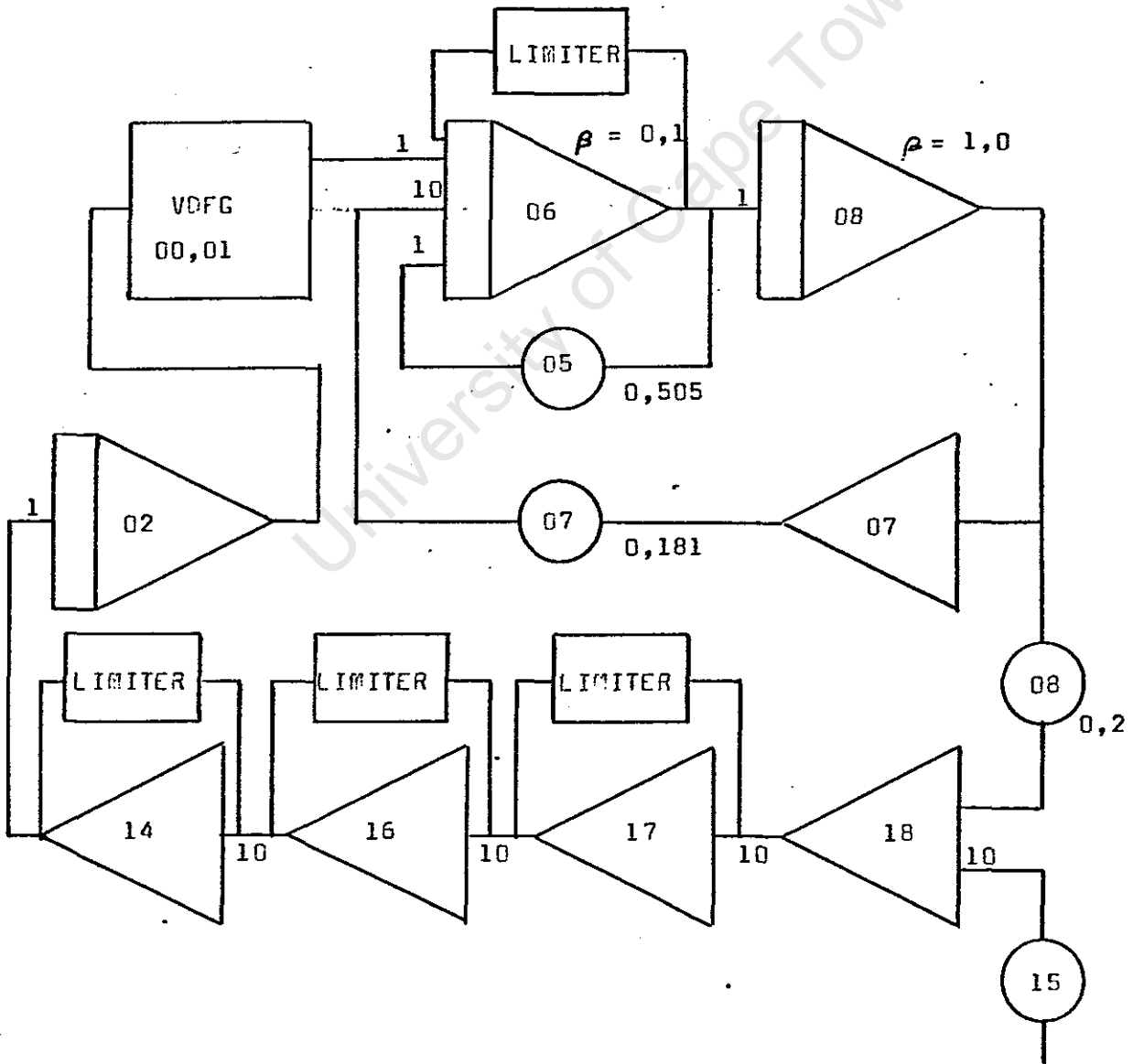
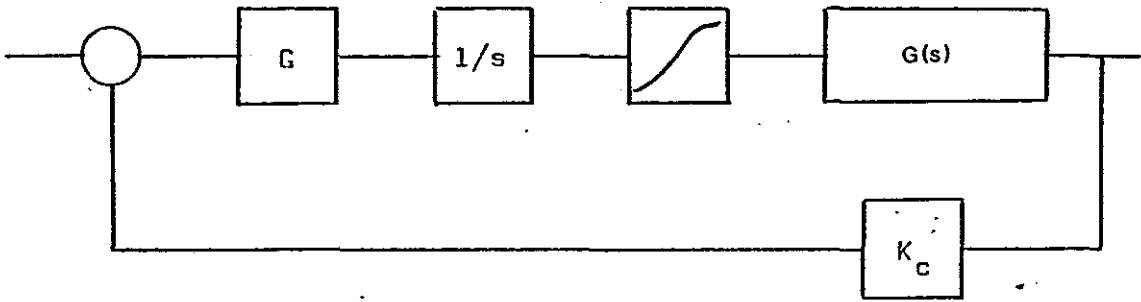


FIGURE 22

The block diagram of the system is shown in (a) while equivalent analogue computer setup is shown in (b)

Values can be calculated for the block diagram equivalent of the computer program as follows. In the program, the maximum rate of change of the trigger delay number is 12 digits per sampling instant in the range between 0 and 256 corresponding to the D.C. voltage varying between 220V and 0V. This modification of the delay number is derived directly from the error between the control setpoint and tachogenerator voltage. Thus an error of 12 digits or more between these two readings results in the maximum rate of change of D.C. voltage which is

$$\frac{nV}{NT}$$

where n = max. change of delay number/sample
 N = max. value of delay number
 V = max. D.C. voltage in volts
 T = sampling interval in seconds

Now $n = 12$, $N = 256$, $V = 220V$ and $T = 40ms$.

Therefore the maximum rate of change is

$$\frac{12 \times 220}{256 \times 40 \times 10^{-3}} = 196 \text{ V/sec.}$$

An error of 12 digits corresponds to an error voltage of $12 \times 9,8mV = 117 \text{ mV}$, where the $9,8mV$ is the resolution of the analogue to digital convertor. Thus, assuming the integrator of the equivalent block diagram has a gain of one, there is a total gain of $\frac{196}{117} \times 10^3 = 1700$ approximately in the forward loop of the control system.

This gain is not constant because, if the error increases beyond twelve, the rate of change of the delay number is unaltered. Thus the program is simulating the effect of saturation in an analogue system, giving the full gain for small errors but exhibiting a variable gain once the maximum rate of change of the delay number supplied to the interface is reached. This is illustrated in Figure 23.

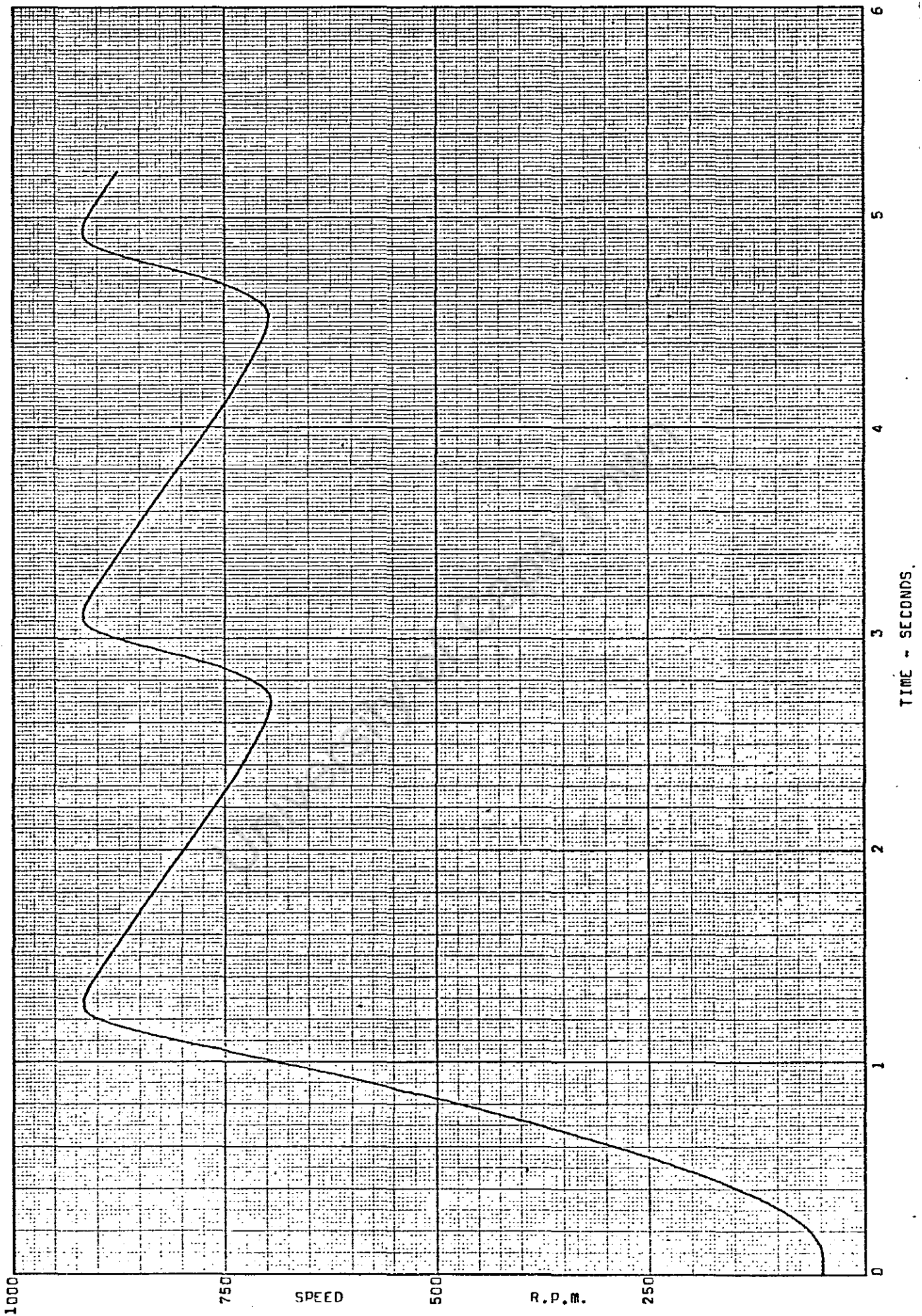


FIGURE 24

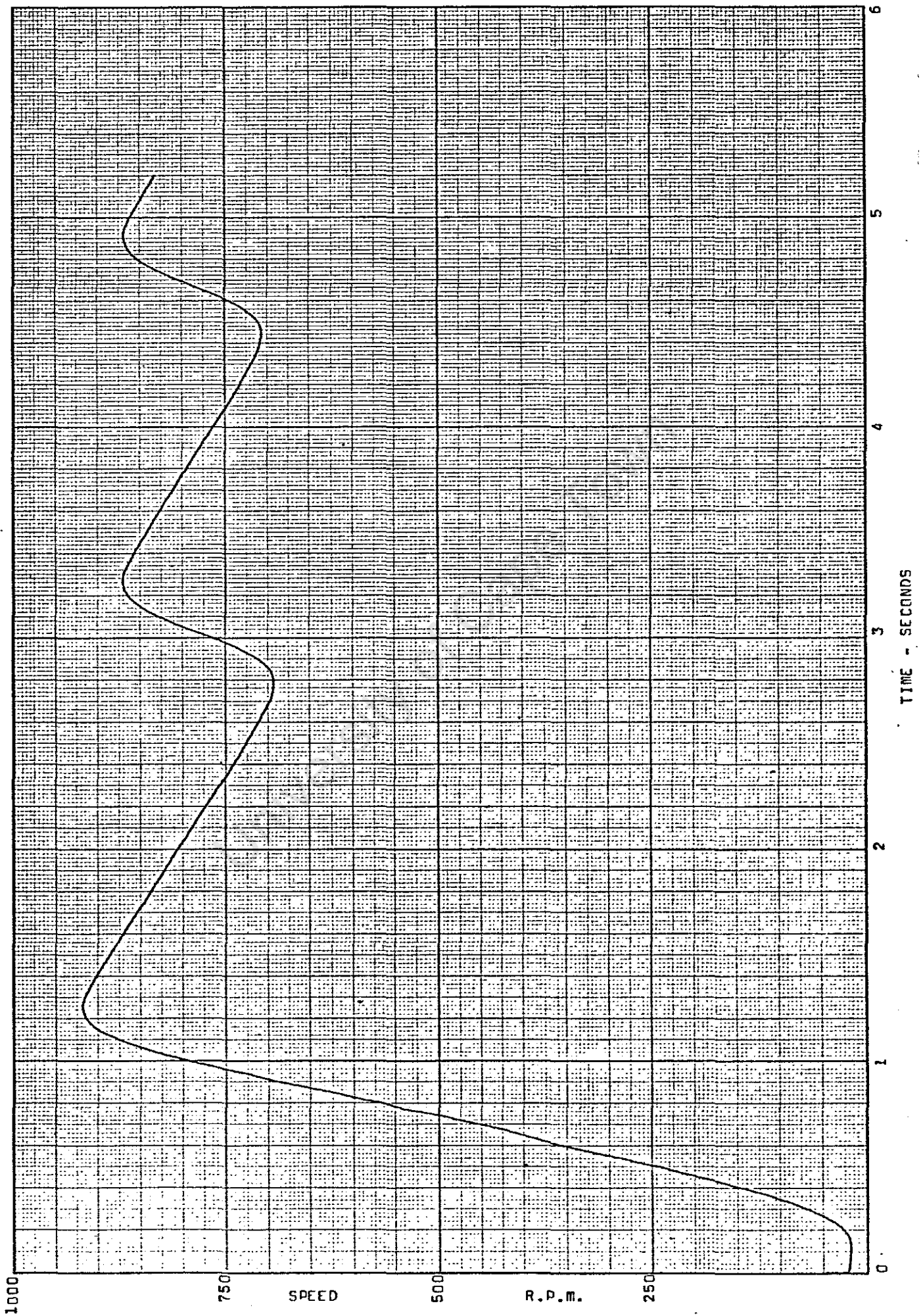


FIGURE 25

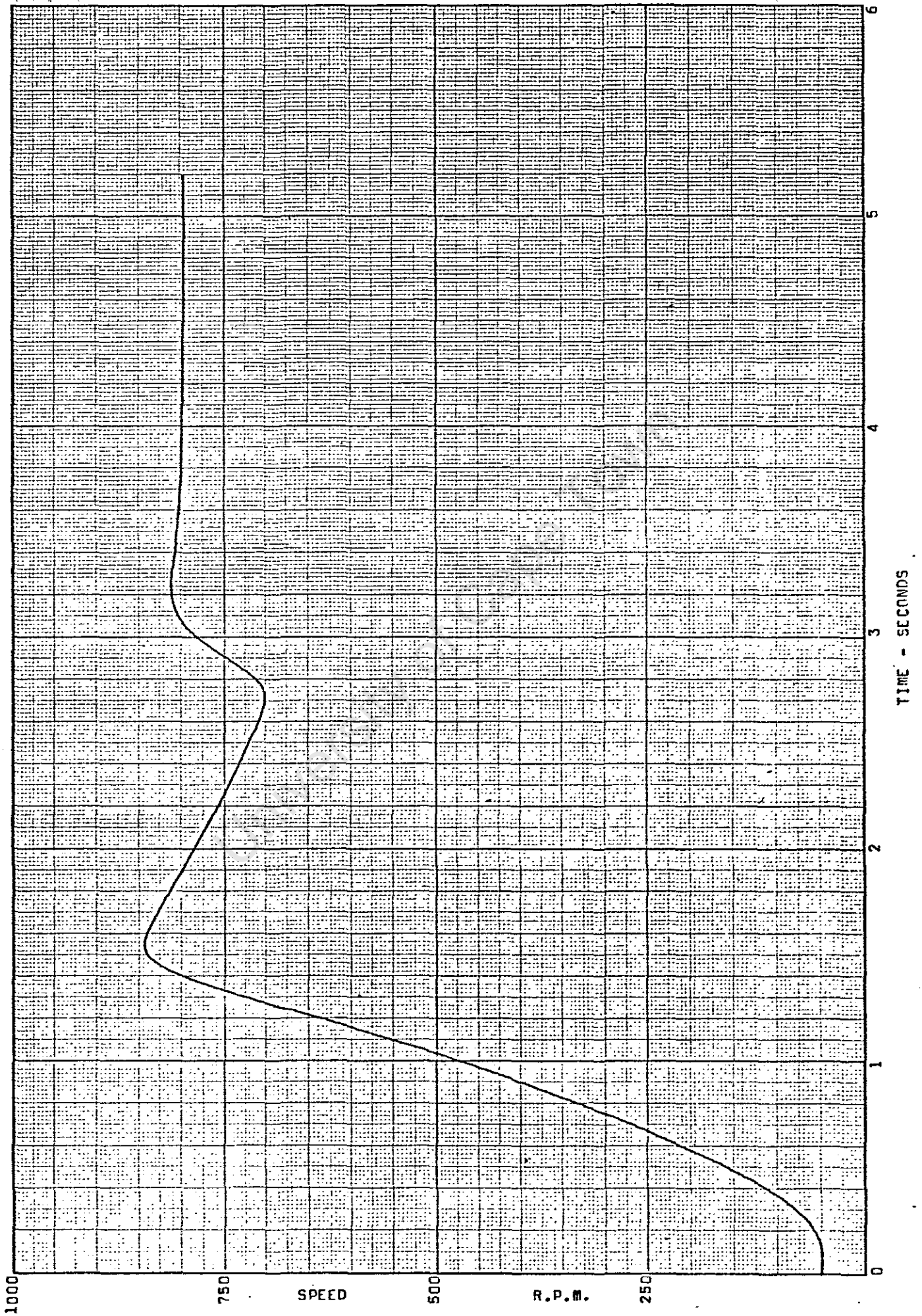


FIGURE 26

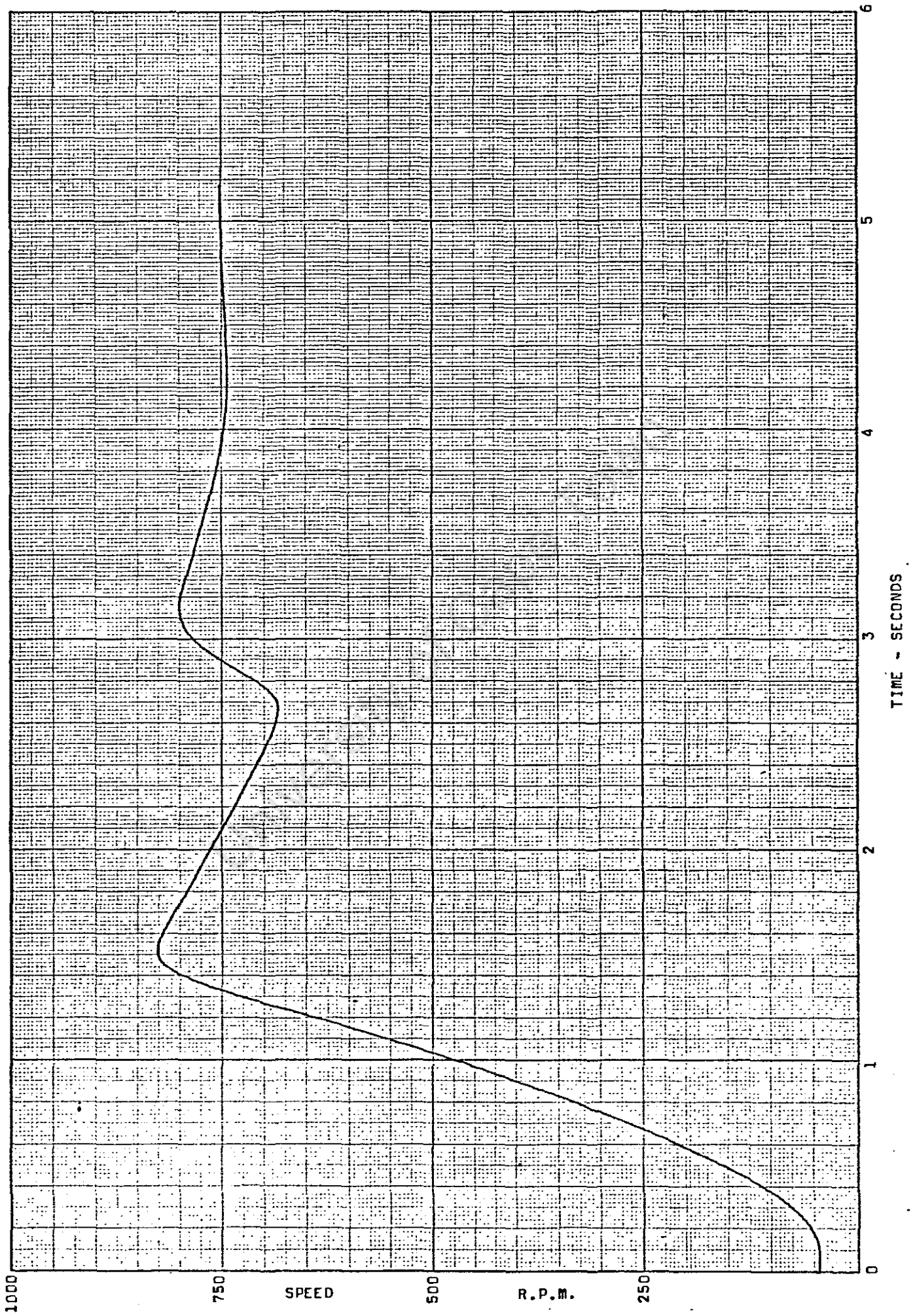


FIGURE 27

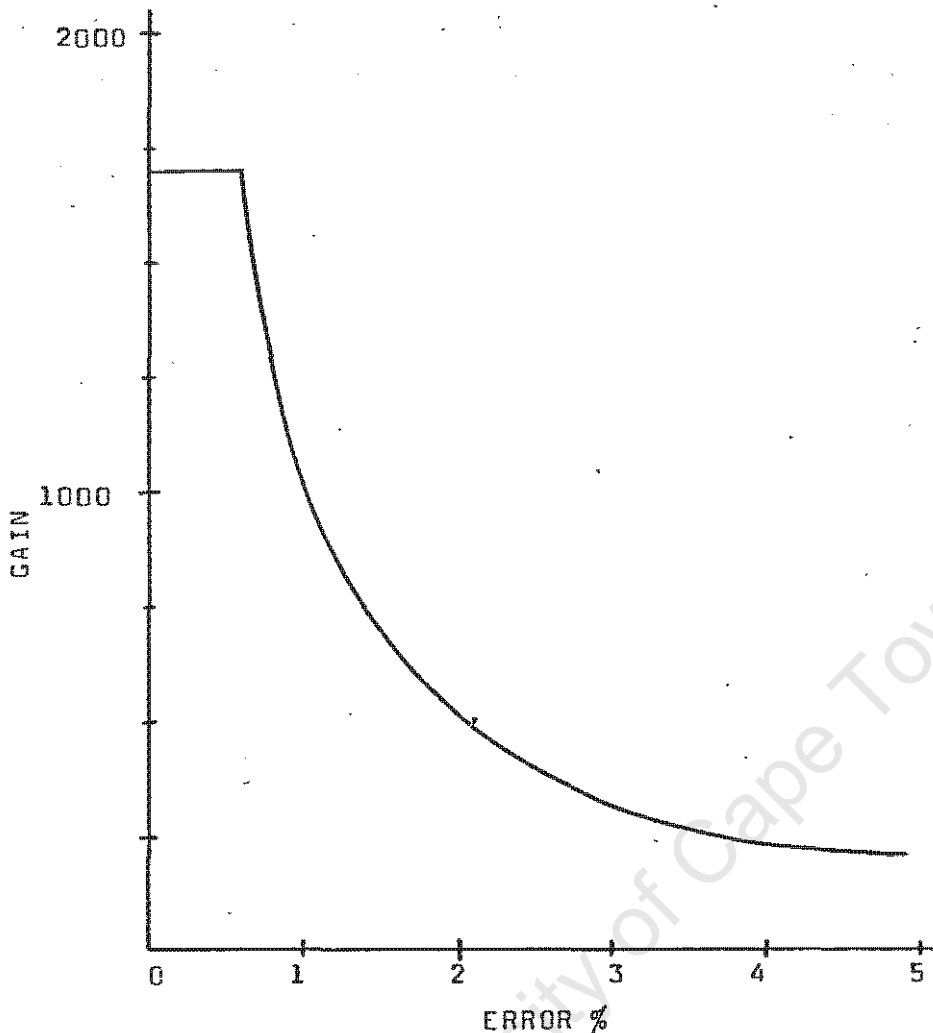


FIGURE 23

Variable gain characteristic of computer program

When the problem had been set up on the analogue computer, the gain was adjusted to give the correct maximum rate of change of the output of the integrator simulating the digital computer program, for the same percentage error at the summer.

This simulation was tried and produced a response as shown in Figure 24., which closely resembles the behaviour of the actual system shown in Figure 25. The analogue system could be very easily stabilized by reducing the gain constant of the equivalent computer program to 1. This could only be done in the actual system by reducing the sampling frequency by a factor of 300 giving a sampling interval of 12 seconds which is highly impractical.

The circuit was then restored to the original gain and a dead band was introduced to see if this would suppress the oscillations around the set point. A large dead band of $\pm 6\%$ stabilized the system.

As this obviously introduces a large steady state error, it was decided to replace this dead band zone with a zone of reduced gain. This produced the desired effect as can be seen in Figure 27. Figure 26 shows the response with the 6% dead zone, while Figure 28 shows how the dead zone and reduced gain zone were effected on the analogue computer.

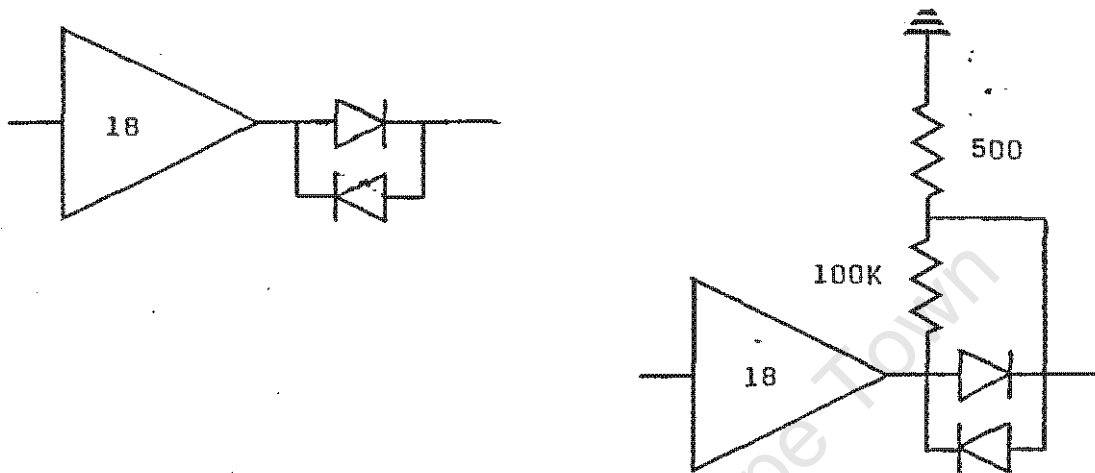


FIGURE 28

Patching on analogue computer to achieve the dead zone and reduced gain characteristics

This reduced gain zone could be implemented in the digital computer program by allowing the firing delay number to be modified approximately every tenth sampling instant and limiting the amount by which it may be modified to about a quarter of that in the high gain zone.

CHAPTER IX

THE FINAL EXPERIMENTAL RUNS

A new digital computer program was written for the control of the D.C. machine embodying the principles outlined at the end of the last chapter. A dead band of $\pm \frac{1}{2}\%$ was also introduced. Limits on the maximum rate of change of the delay number were again imposed for the following reason:

The D.C. motor used for the test runs has a rating of 53A. As the maximum current the bridge rectifier can handle was 33A, it was necessary to impose a limit in the program on the maximum rate of change of firing delay of the thyristor bridge in order to control the maximum current flowing in the power circuit.

The program was written in such a manner that the constants controlling the behaviour of the system could be readily adjusted to obtain any desired performance. This was loaded into the computer and test runs were taken, the results being described in the following paragraphs.

Figures 29 - 52 show response curves of the system to step input, the motor running initially at 100 rpm and finally settling at 750 rpm.

Except as stated the parameters for these curves are as follows:-

Max. rate of change of delay per sample: 5 bits per sampling instant.

Absolute dead band: $\frac{1}{2}\%$

Sampling rate in reduced gain region: every 10th sampling interval.

The first five figures show responses under no load conditions for reduced gain zones as follows:-

Figure No.	29	30	31	32	33
Reduced gain zone width, % of full delay range	53,5	47,6	37,5	30,0	25,0
percent overshoot	00	00	5%	10	15

Figures 34 - 38 show response for the motor driving a generator with a 1kW load at 750 rpm. The reduced gain zone widths are as follows:-

Figure No.	34	35	36	37	38
Reduced gain zone width, % of full delay range	40,0	37,5	23,8	15,7	9,4
percent overshoot	00	00	5	10	15

Figures 54 and 55 show plots of overshoot against reduced gain zone width for no load and a kW load on the generator. The no load curve is hyperbolic in nature and obeys the equation.

$$(1 + 0,65)W = 47,6$$

where S = overshoot, %

W = reduced gain zone width, %

The 1kW load curve also appears to be hyperbolic in nature, the load causing the reduced gain width to decrease, but the spread in the readings is too great to find a meaningful equation.

After the previous trials, the machine was run with no load and the program constants adjusted to give critical damping. The number of sampling instants between which corrective action was taken in the reduced gain region, was then varied. The effects can be compared in Figures 30, 39 and 40, the variable being tabulated as follows:-

Figure No.	30	39	40
Reduced sampling rate	every 10th sample	every 20th sample	every 5th sample

From these it can be seen that the reduced sampling rate is fairly critical. Too fast a sampling rate tends to make the system oscillatory while too slow a rate tends to produce a result similar to that of an overdamped sampled data system.

Figures 41 - 44 show the effects of varying the sampling rate. In each case the sampling time was doubled, as was the maximum change of delay number per sample, while the number of samples between which the delay was modified in the reduced gain region was halved, to maintain the same rate of change per unit time. The reduced gain zone width was adjusted to give a critically damped response in each case excepting the last. Considering that the reduced gain zone widths are within 3% of each other, it can be deduced that the system is independent of the sampling frequency above 6,25 Hz (T = 160 m sec). The system is still controllable with longer periods but the response is different.

The data for the curves are:-

Figure No.	41	42	43	44
sampling interval m.sec.	40	80	160	320
Max. change of delay per sample	5	10	20	40
No. of samples between modification of delay in reduced gain zone	10	5	2	1
Reduced gain zone width percent	37,5	40,2	37,5	37,5

The generator had a 500 w load at 750 rpm.

Figures 45 - 48 show response to a step load of 1 kW applied to the generator for different sampling intervals, the parameters for each sampling interval being the same as in the previous set of curves. It can be seen that the difference between the curve is negligible, and shows that the response is adequate for load holding.

Figures 49 - 51 show the response of the system to a triangular input voltage of peak to peak amplitude 2,4V. Figure 49 shows the response to a wave of period 100 sec. The error is always within the reduced gain zone so it is smooth and linear. When the period is reduced to 0,20 sec., the error alternates between the low and high gain zones giving a response as shown in Figure 50. Figure 51 shows the response to triangular wave of period 2 sec. Here the change between the two gain zones is so frequent that it cannot be noticed.

This last set of figures was obtained with the program parameters adjusted to give a critically damped response with the generator supplying 500 W to a resistive load. Armature current flow of the motor was continuous when these curves were taken. Although not perfect, the response is adequate.

Response of the motor to a downward step of from 750 rpm to 375 rpm was satisfactory as can be seen in Figure.52.

If the supply is disconnected from a D.C. shunt motor, a voltage due to the back E.M.F. of the motor will be maintained in the motor circuit, gradually falling as the motor speed drops. With a thyristor drive it is desirable that the voltage at the output of the controlled bridge rectifier should closely follow this back E.M.F. voltage, if a smooth response is to be expected from the system on a downward step of the setpoint voltage. Unless special precautions are taken the rectifier voltage will decrease much more rapidly than that due to the back E.M.F. of the motor and probably fall to zero as a result of negative feedback. When the motor has slowed to near the final value, the rectifier voltage will have to first increase from zero and then speed up the motor which, of course, has continued to slow down.

It can be seen that this form of compensation gives a readily controllable system. Any degree of damping can be obtained for a step input to the system. When a ramp voltage is applied to the input, there are no signs of instability although for certain rates of rise of input voltage, the system response is erratic.

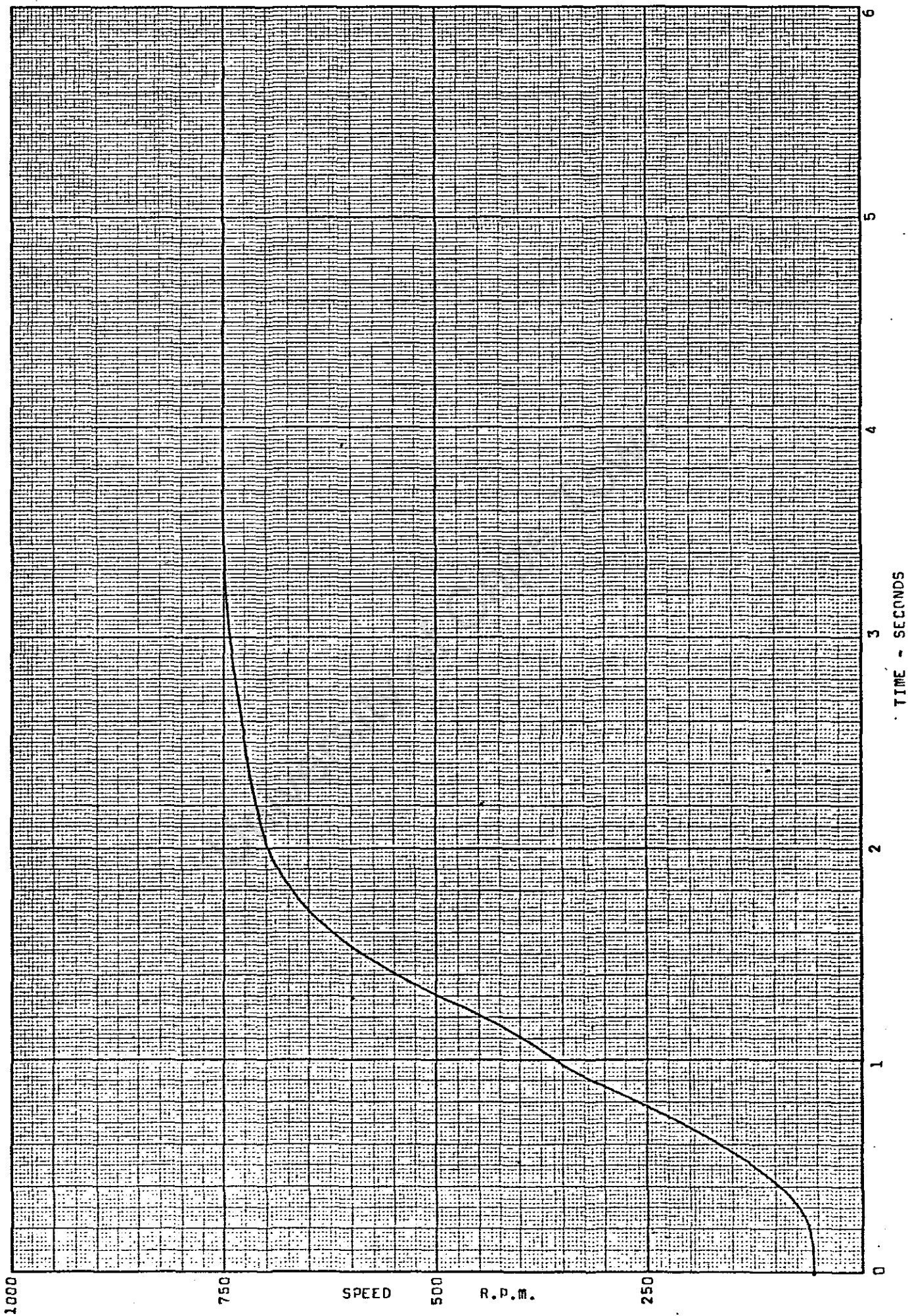


FIGURE 29

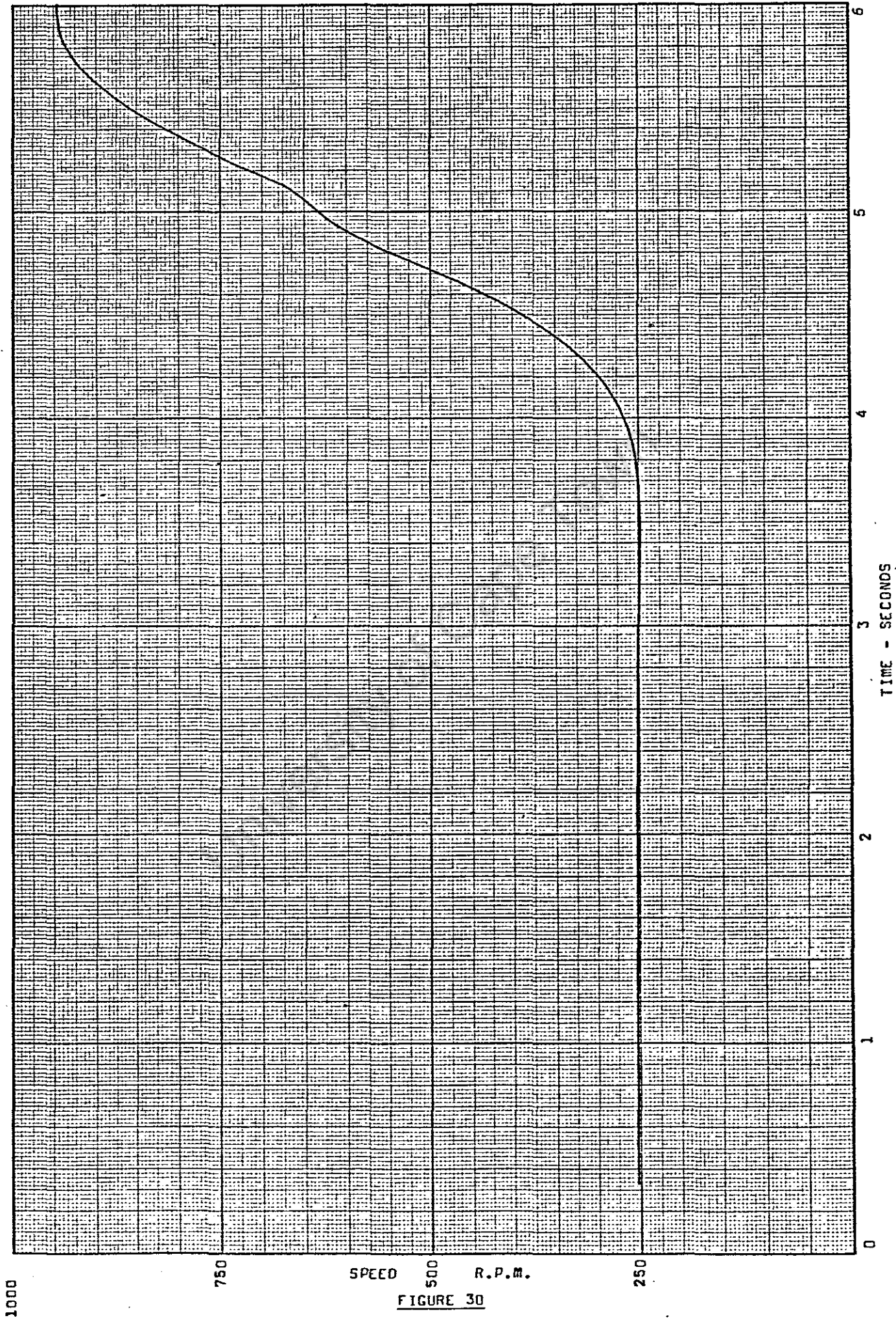


FIGURE 30

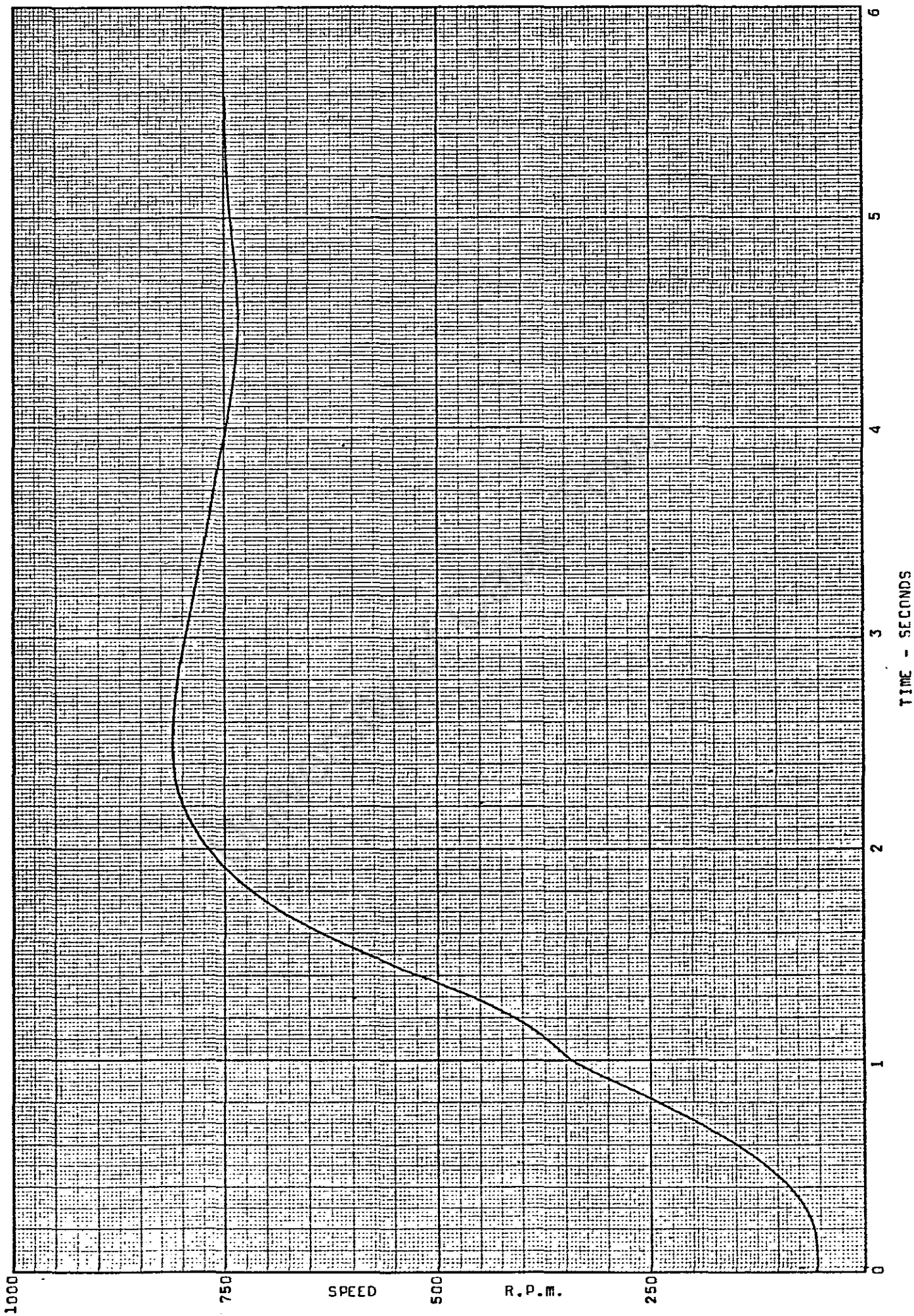


FIGURE 31

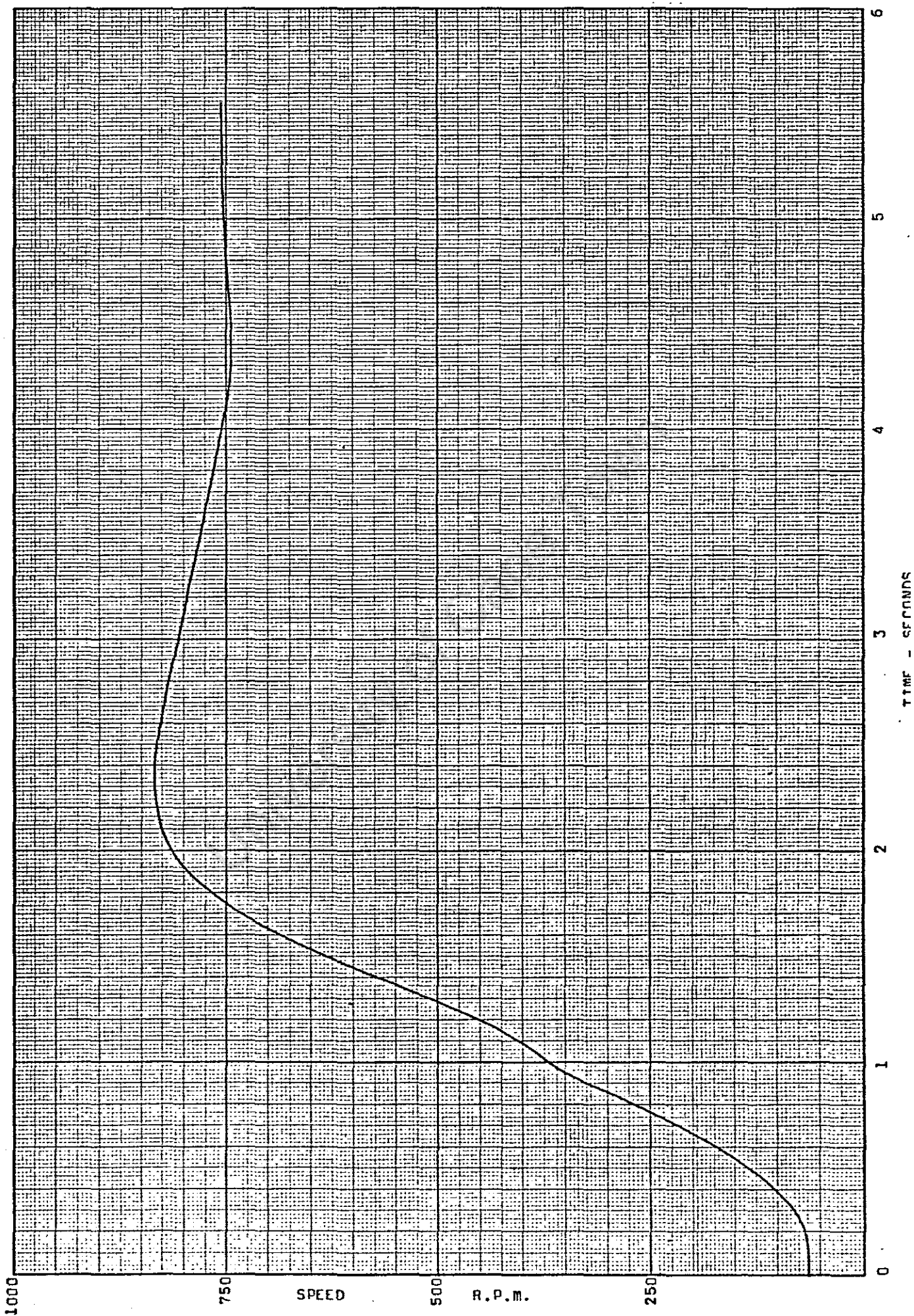


FIGURE 32

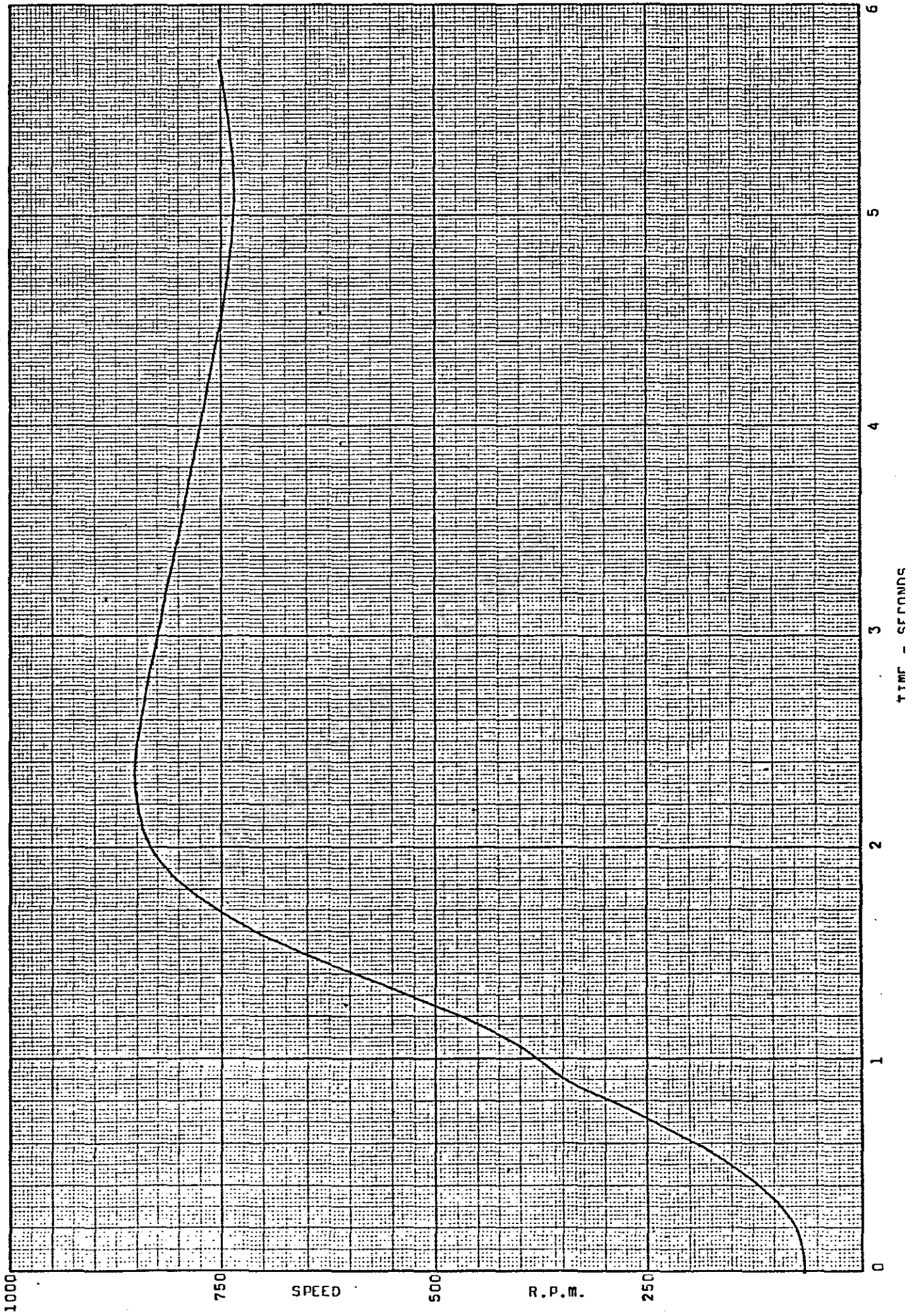


FIGURE 33

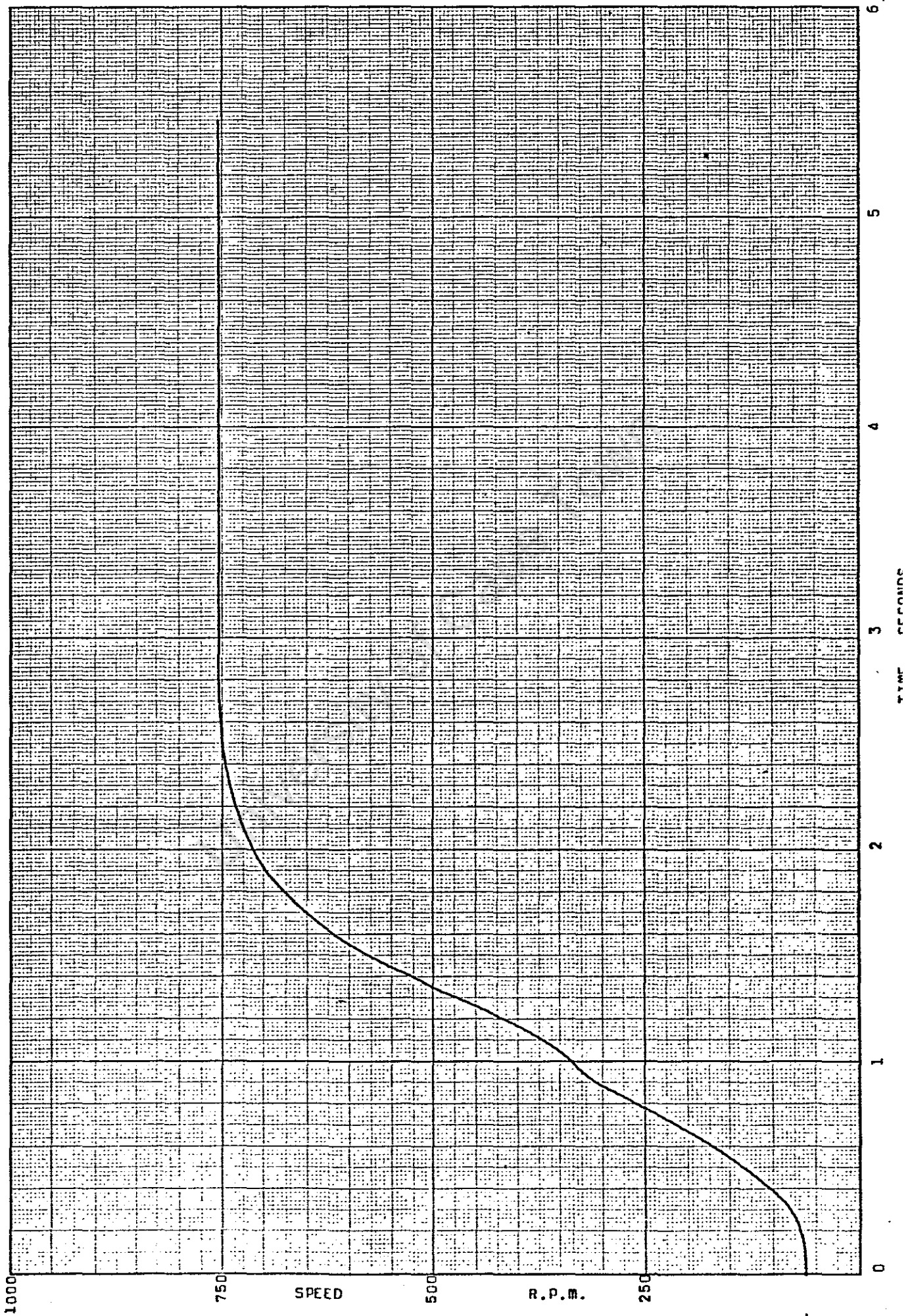


FIGURE 34

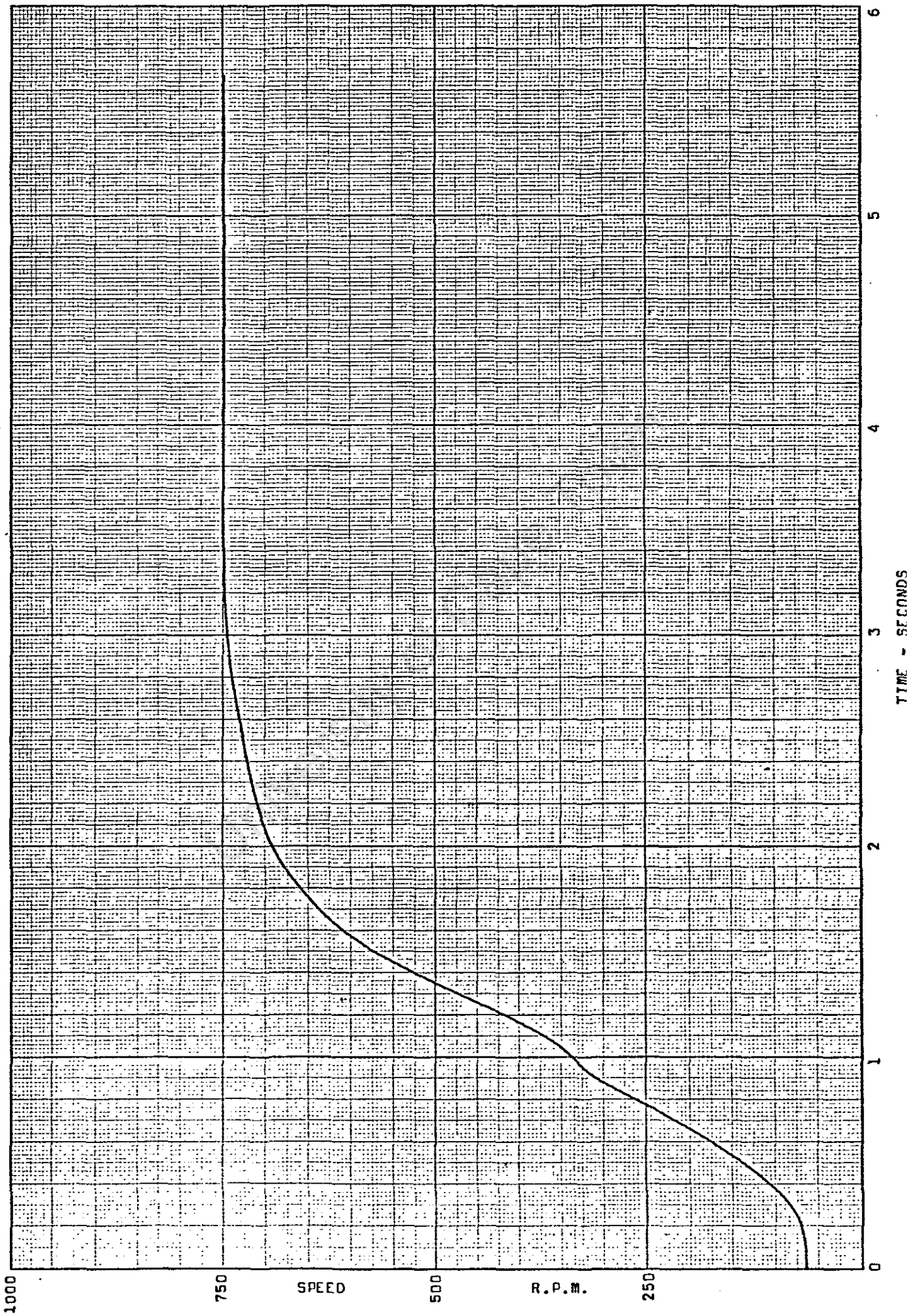


FIGURE 35

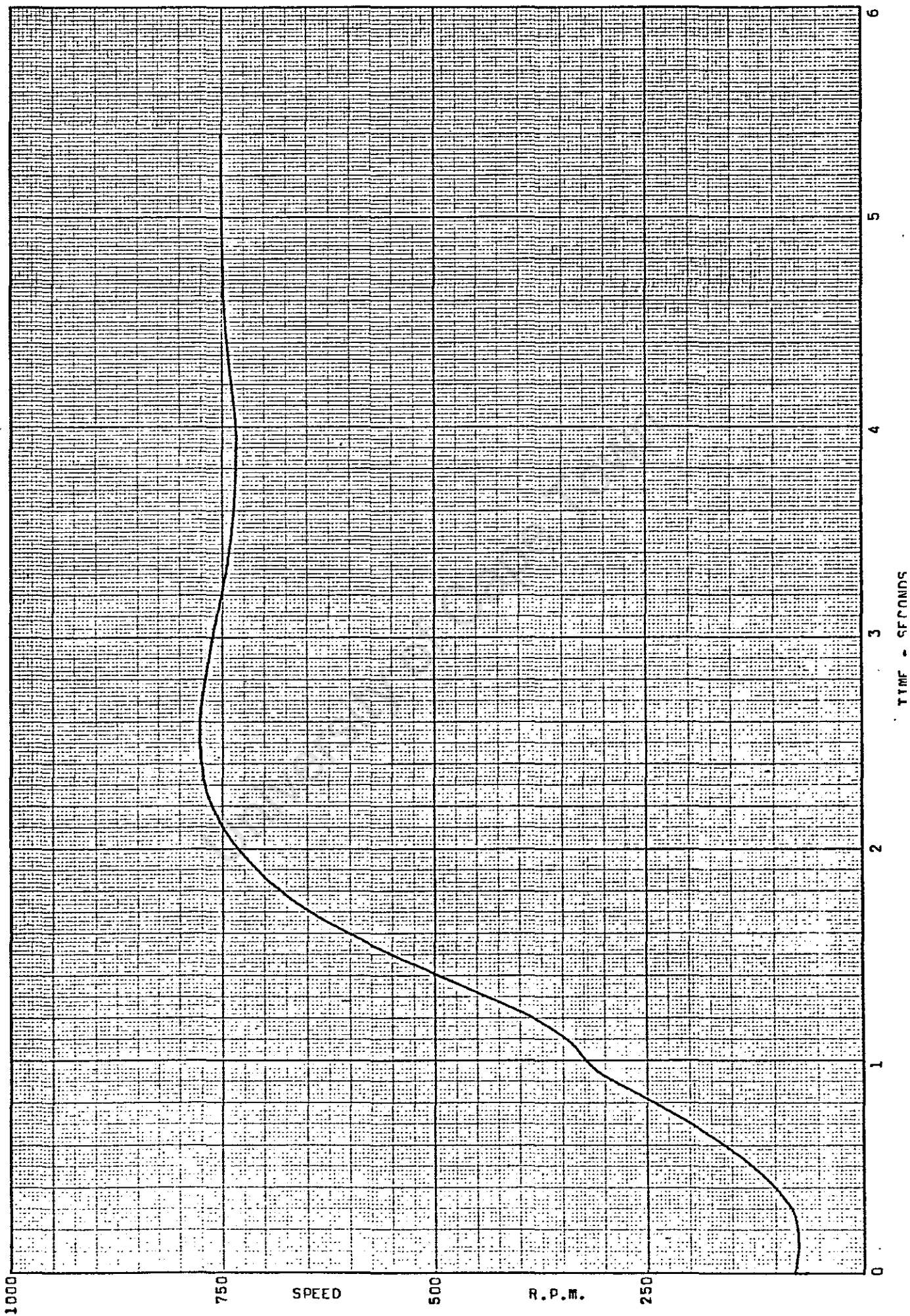


FIGURE 36

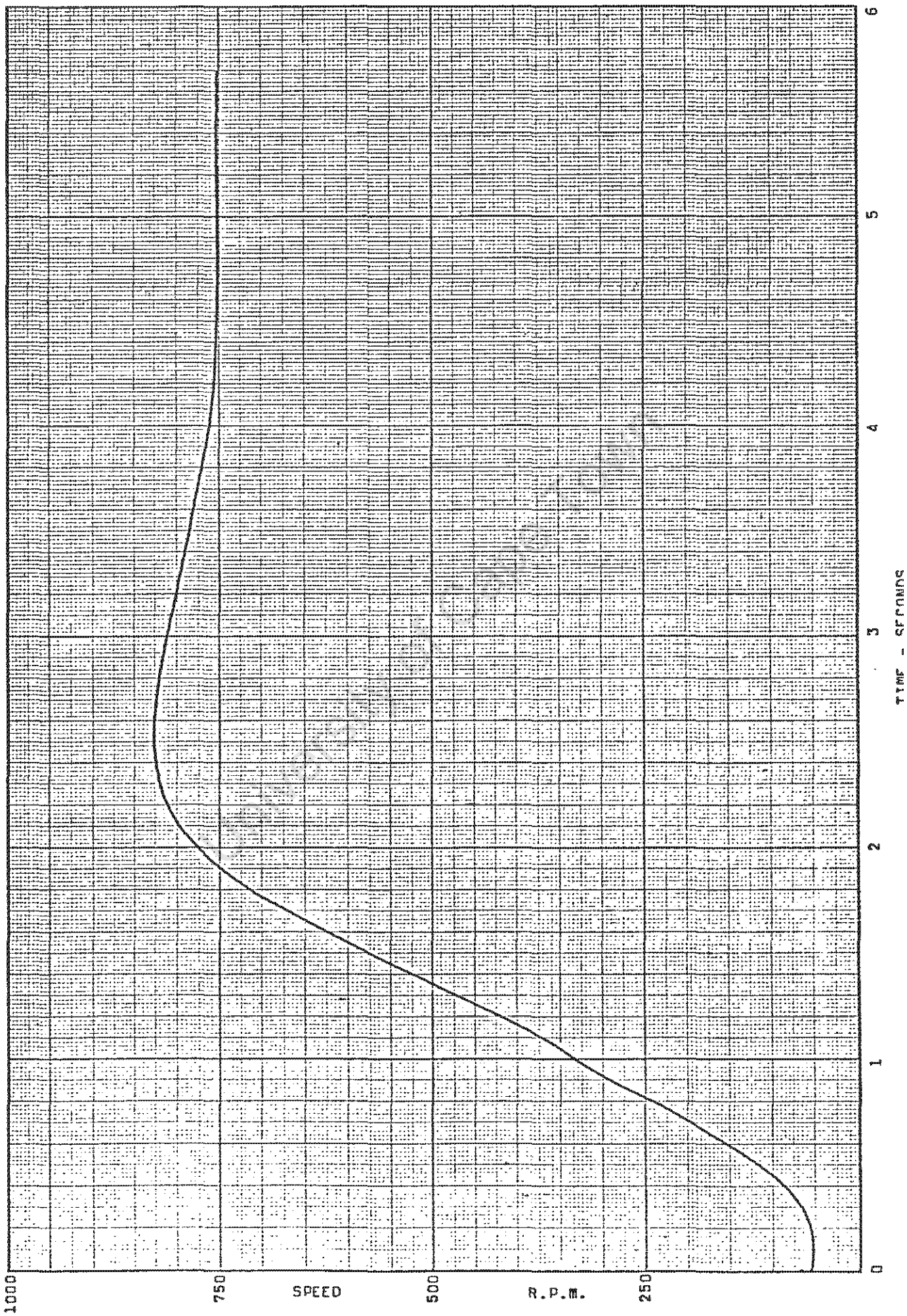


FIGURE 37

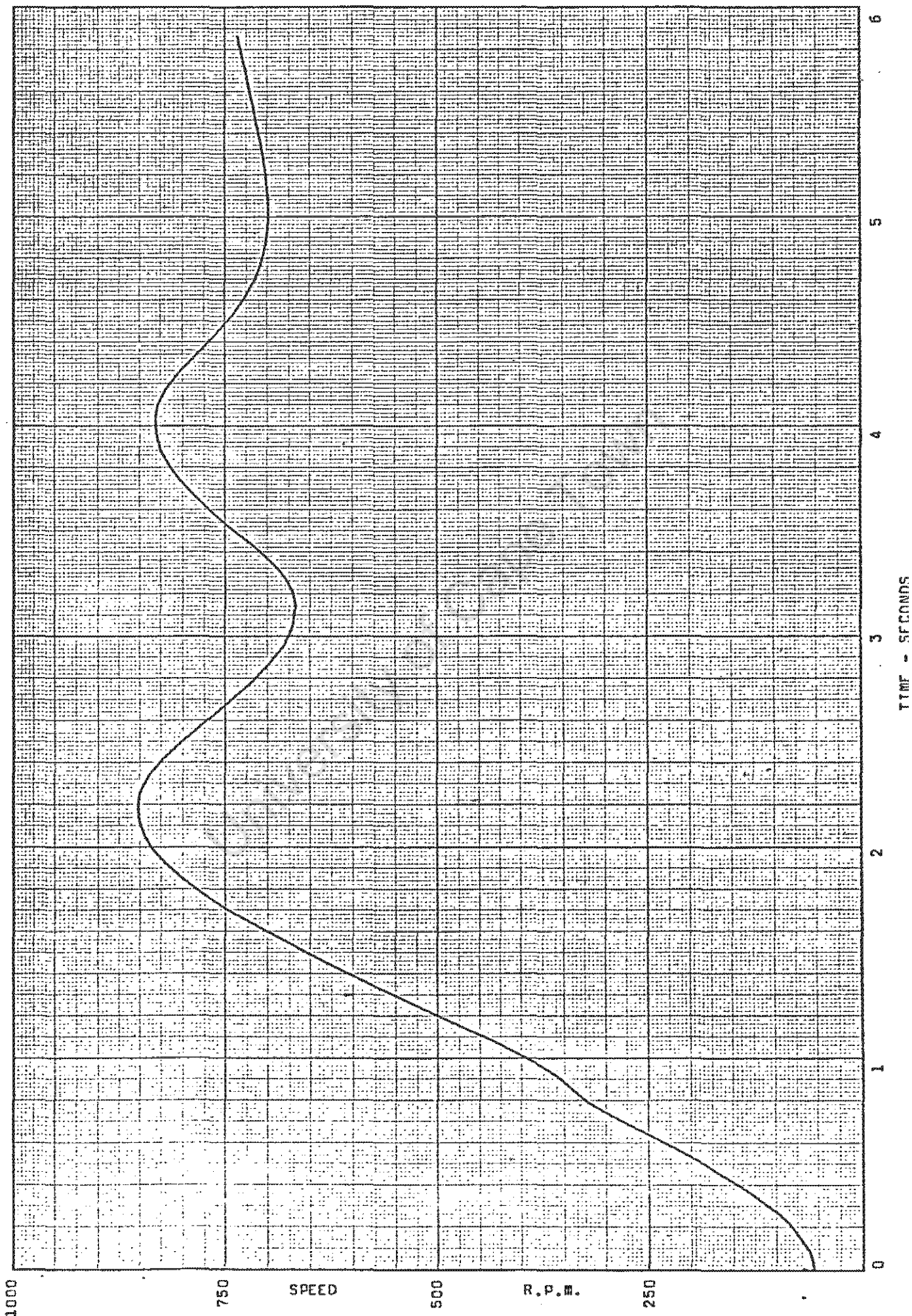


FIGURE 38

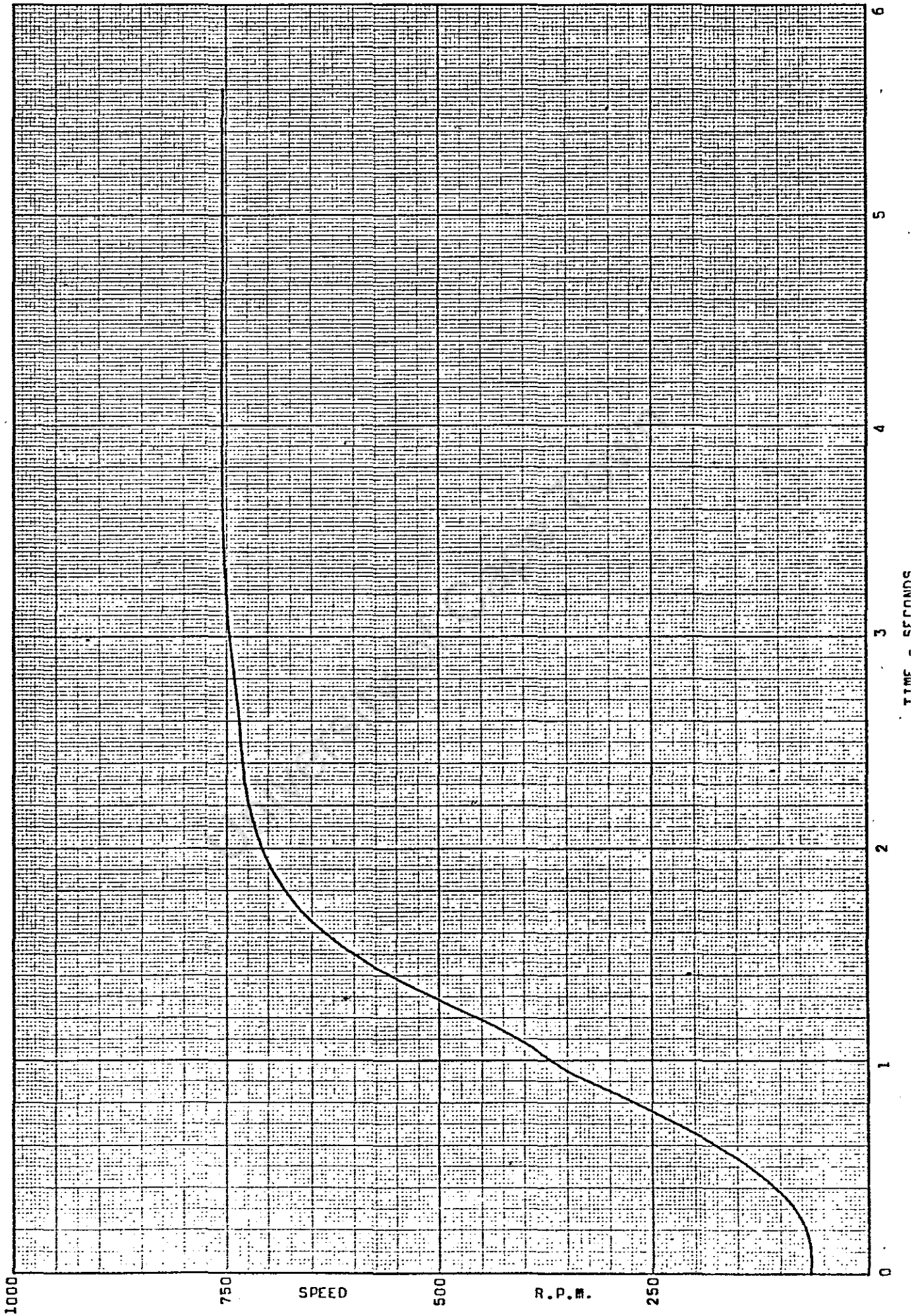


FIGURE 39

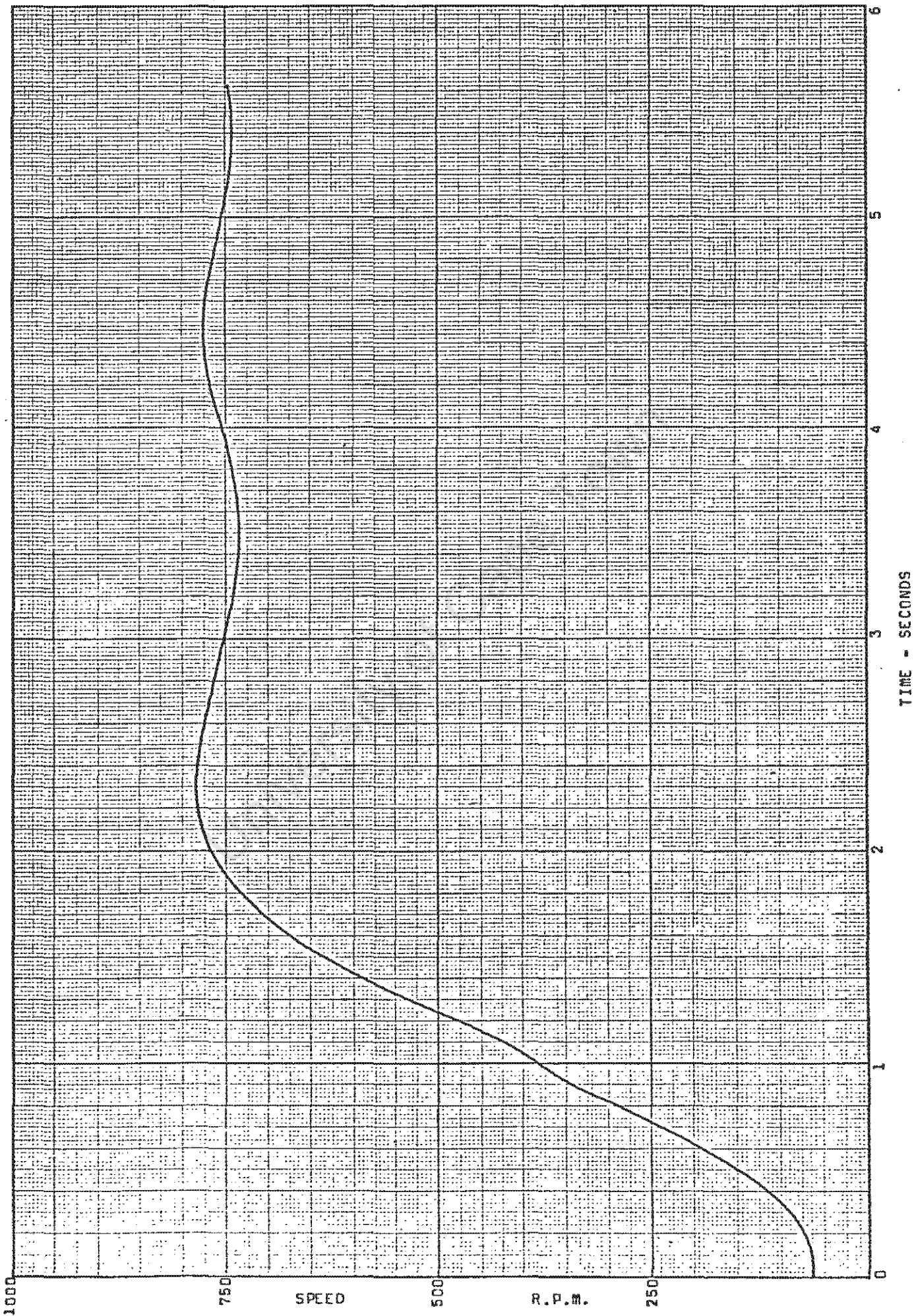


FIGURE 40

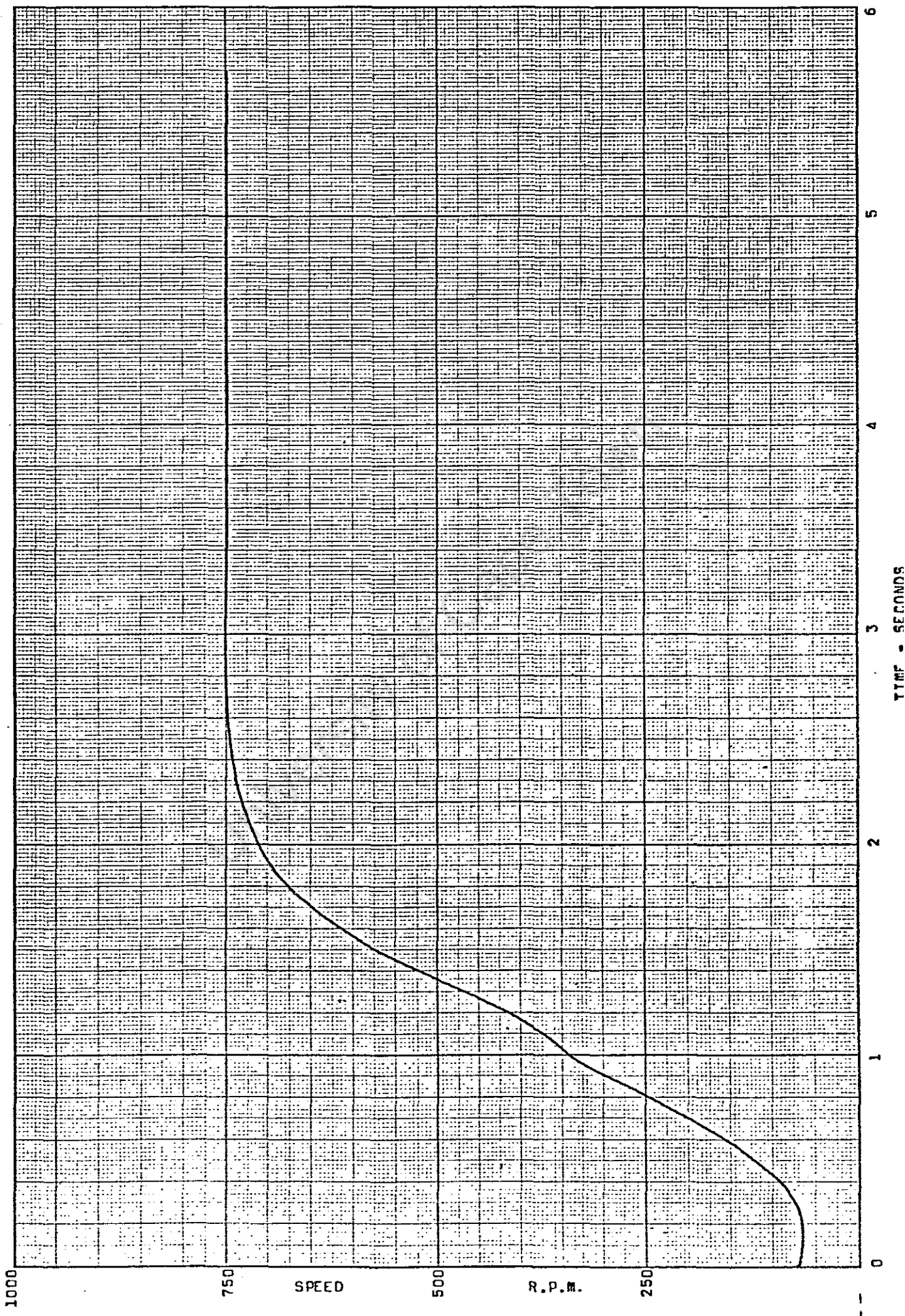


FIGURE 41

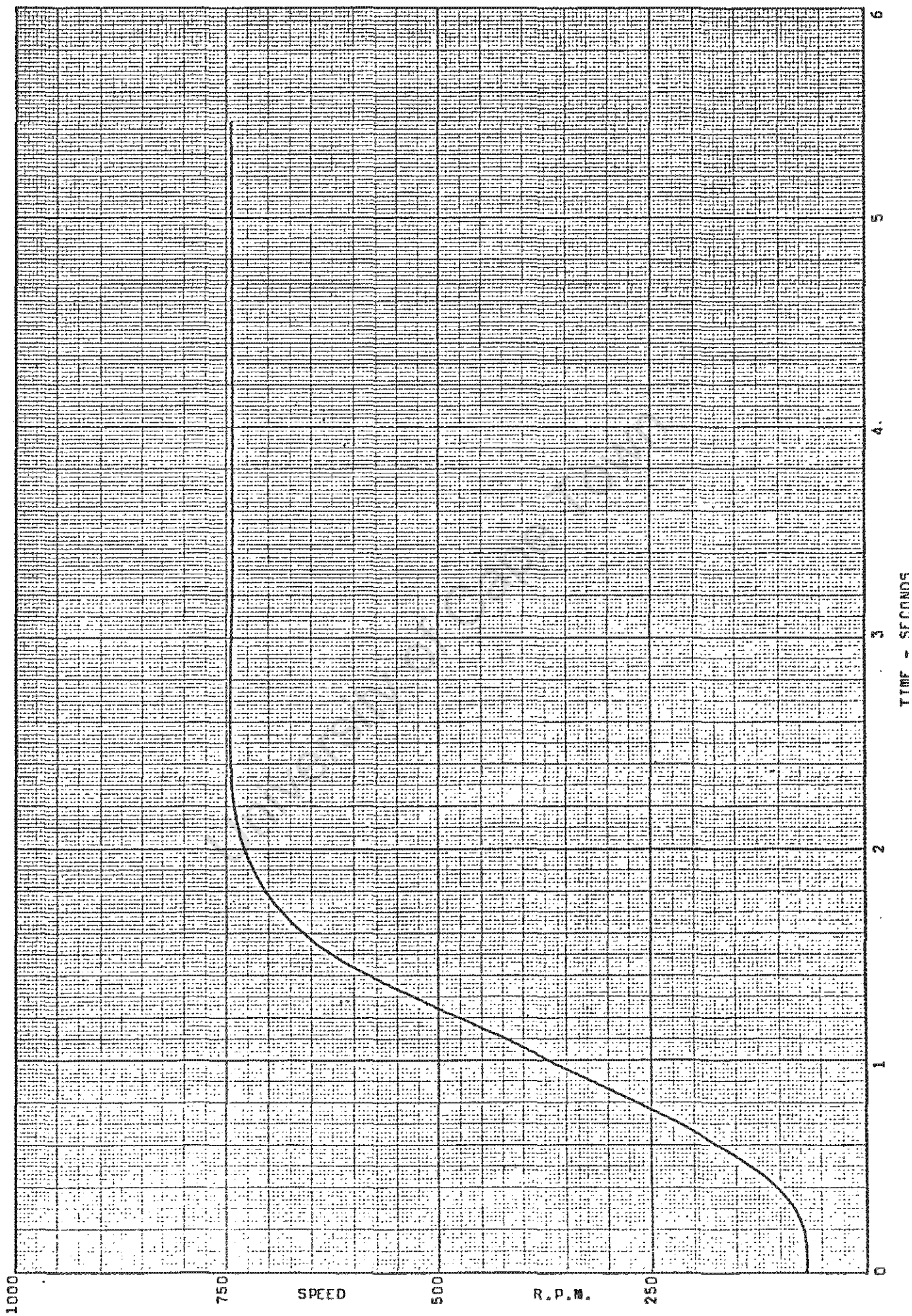


FIGURE 42

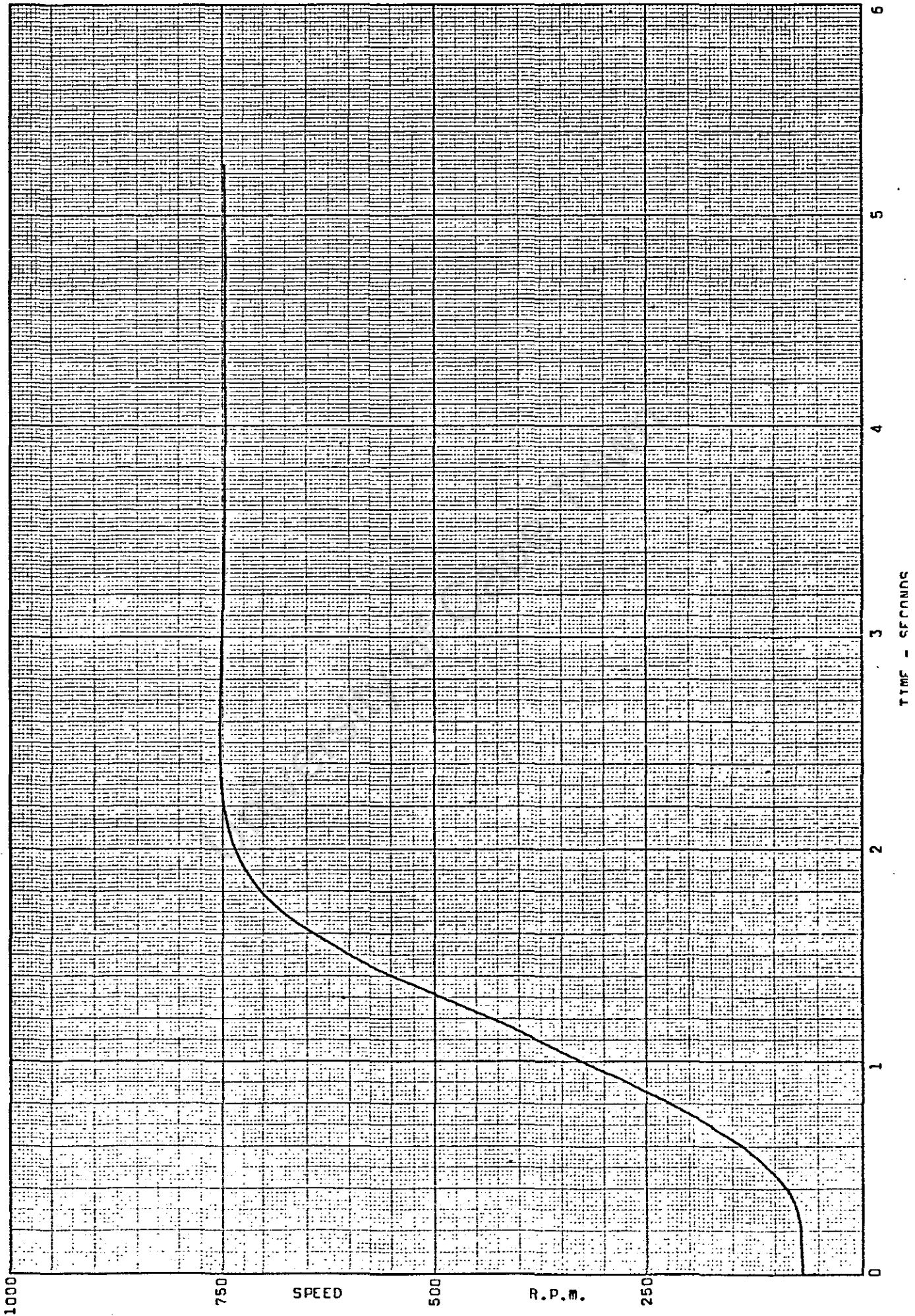


FIGURE 43

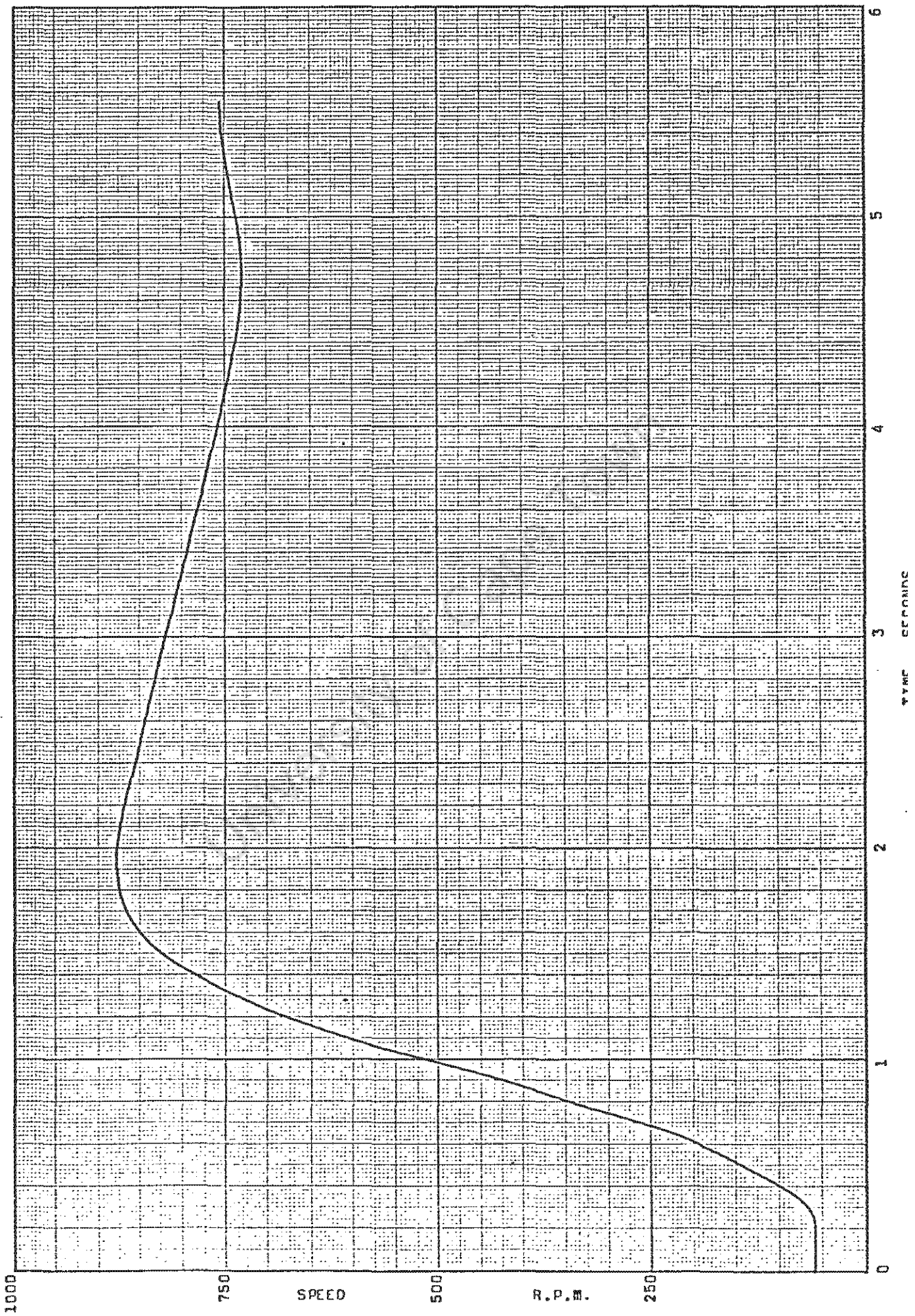


FIGURE 44

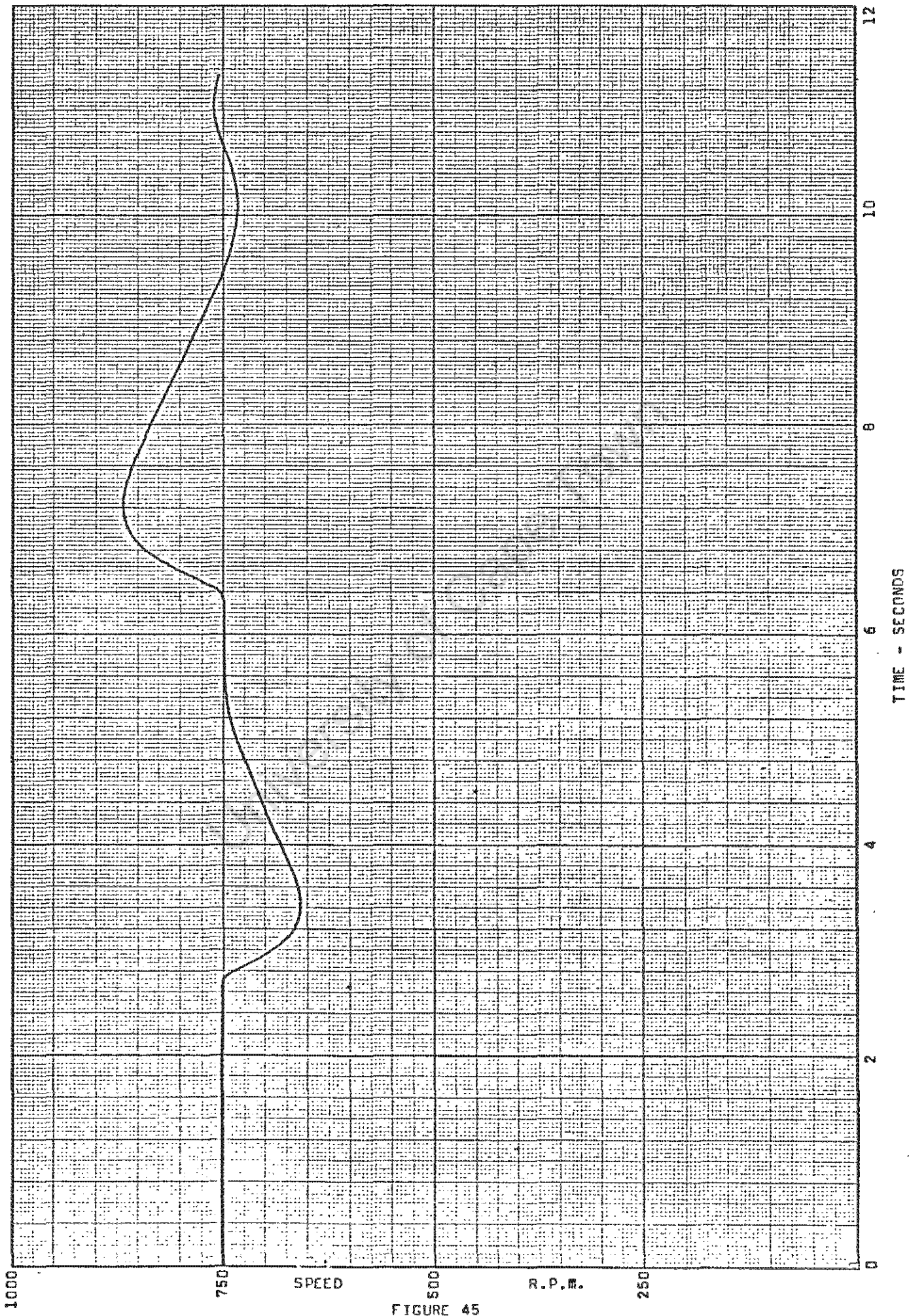


FIGURE 45

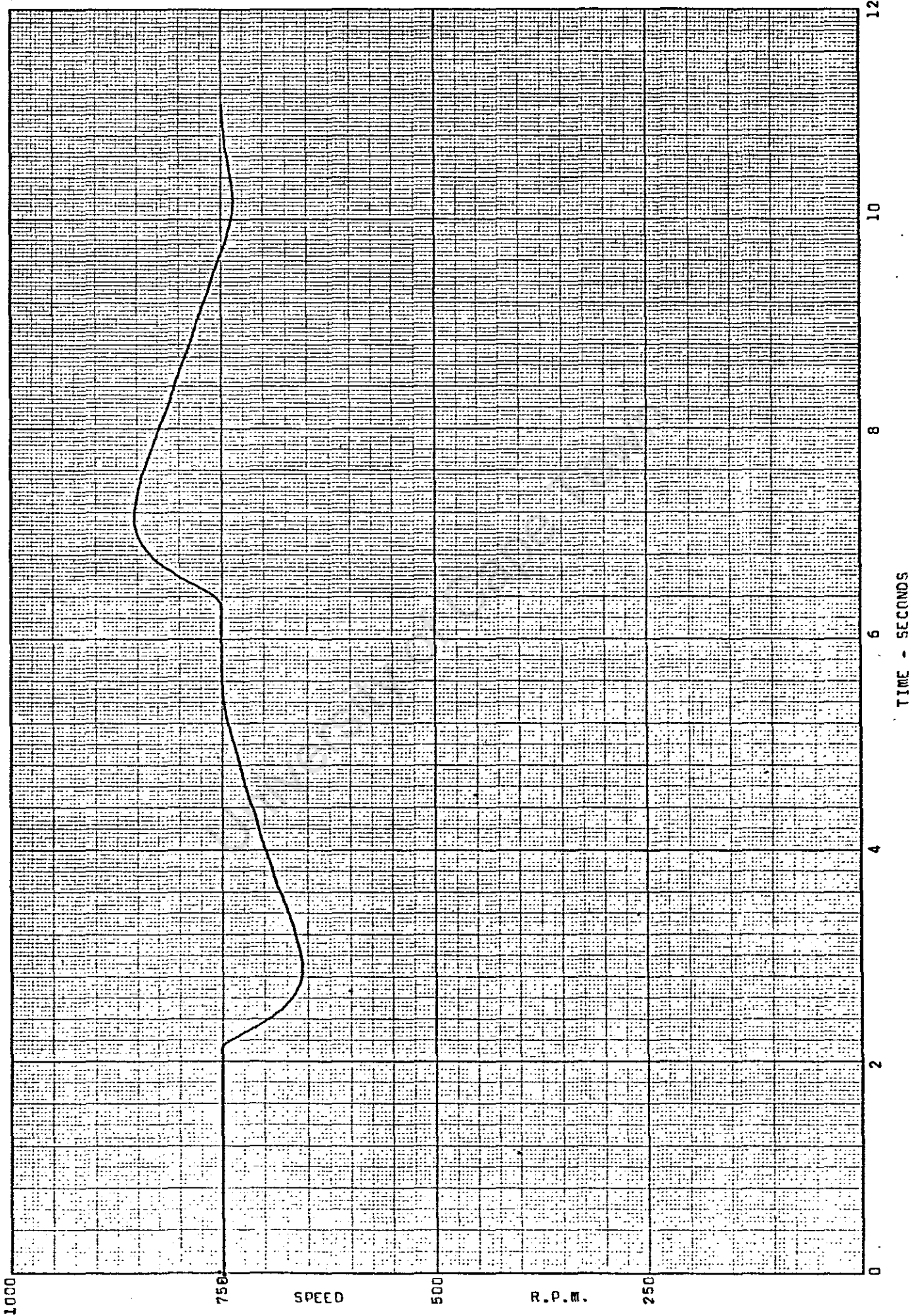


FIGURE 46

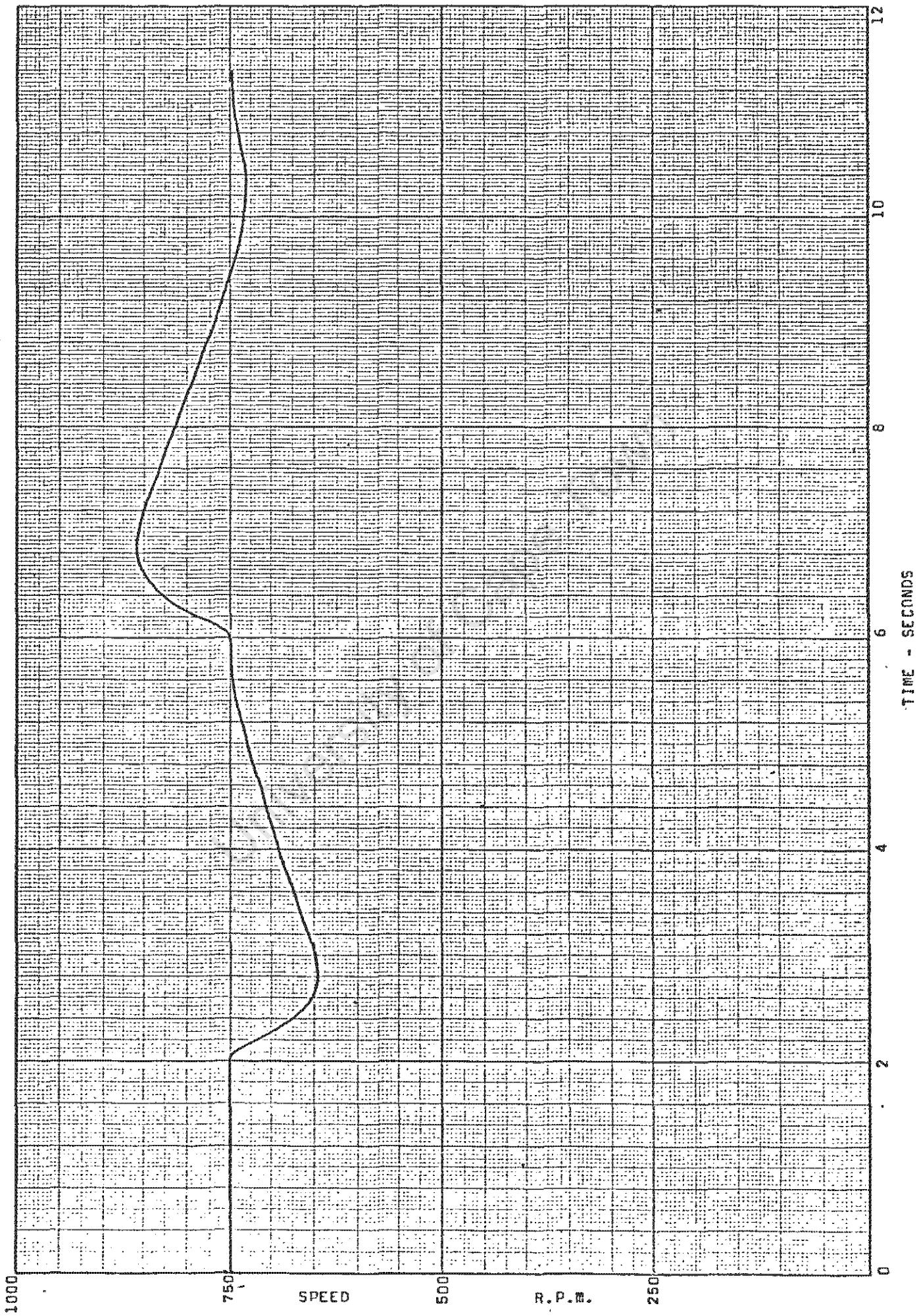


FIGURE 47

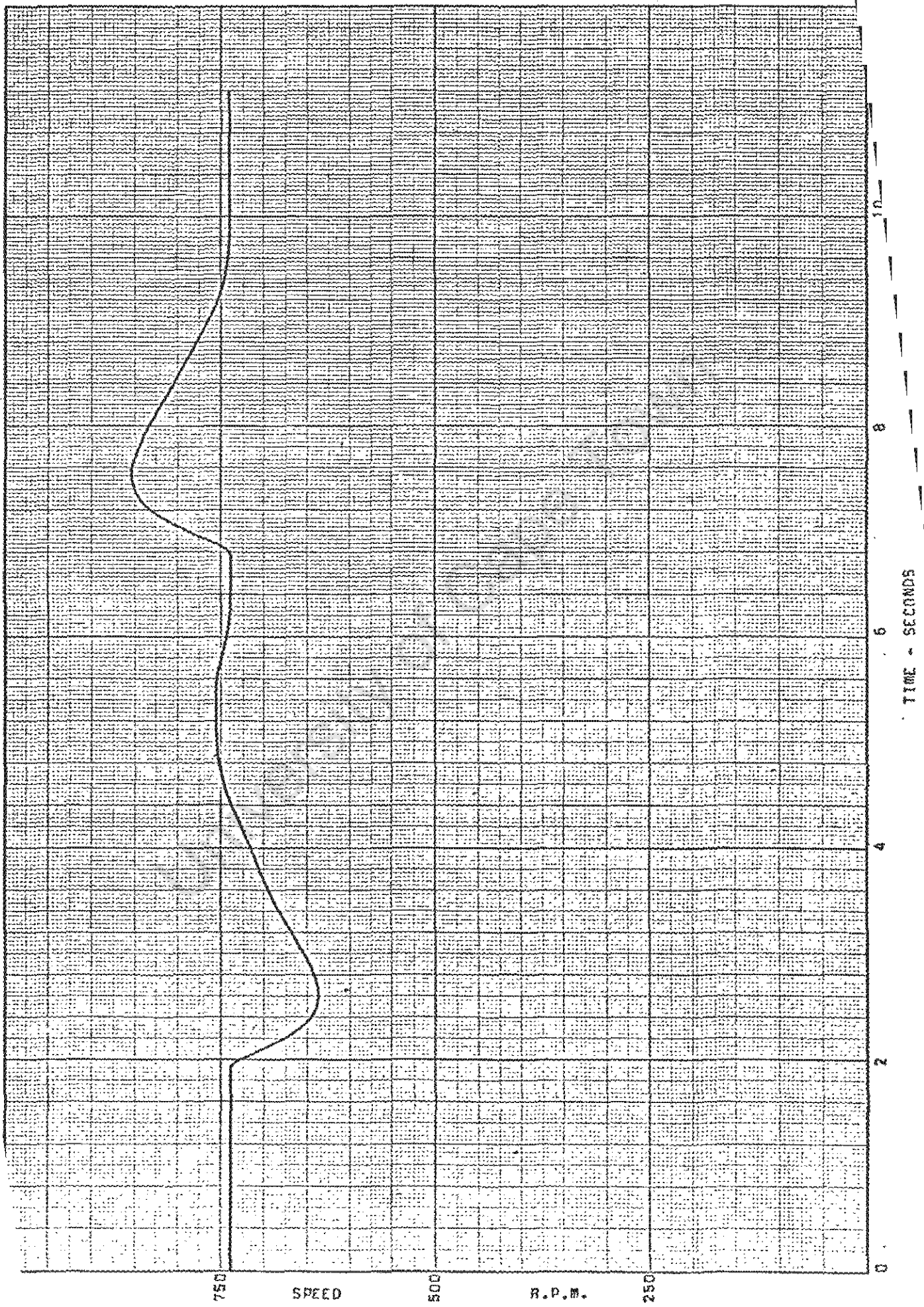


FIGURE 4B

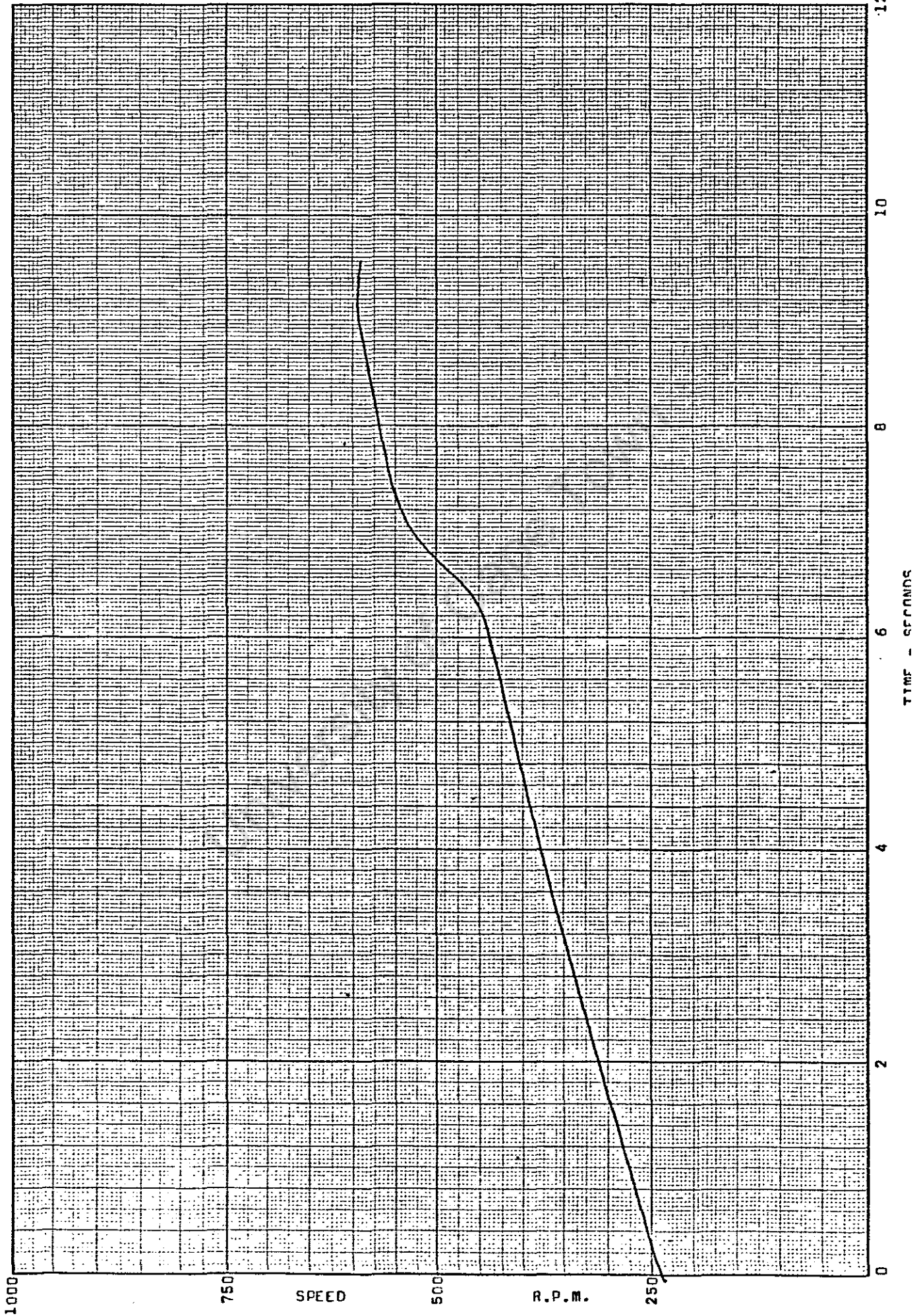


FIGURE 49

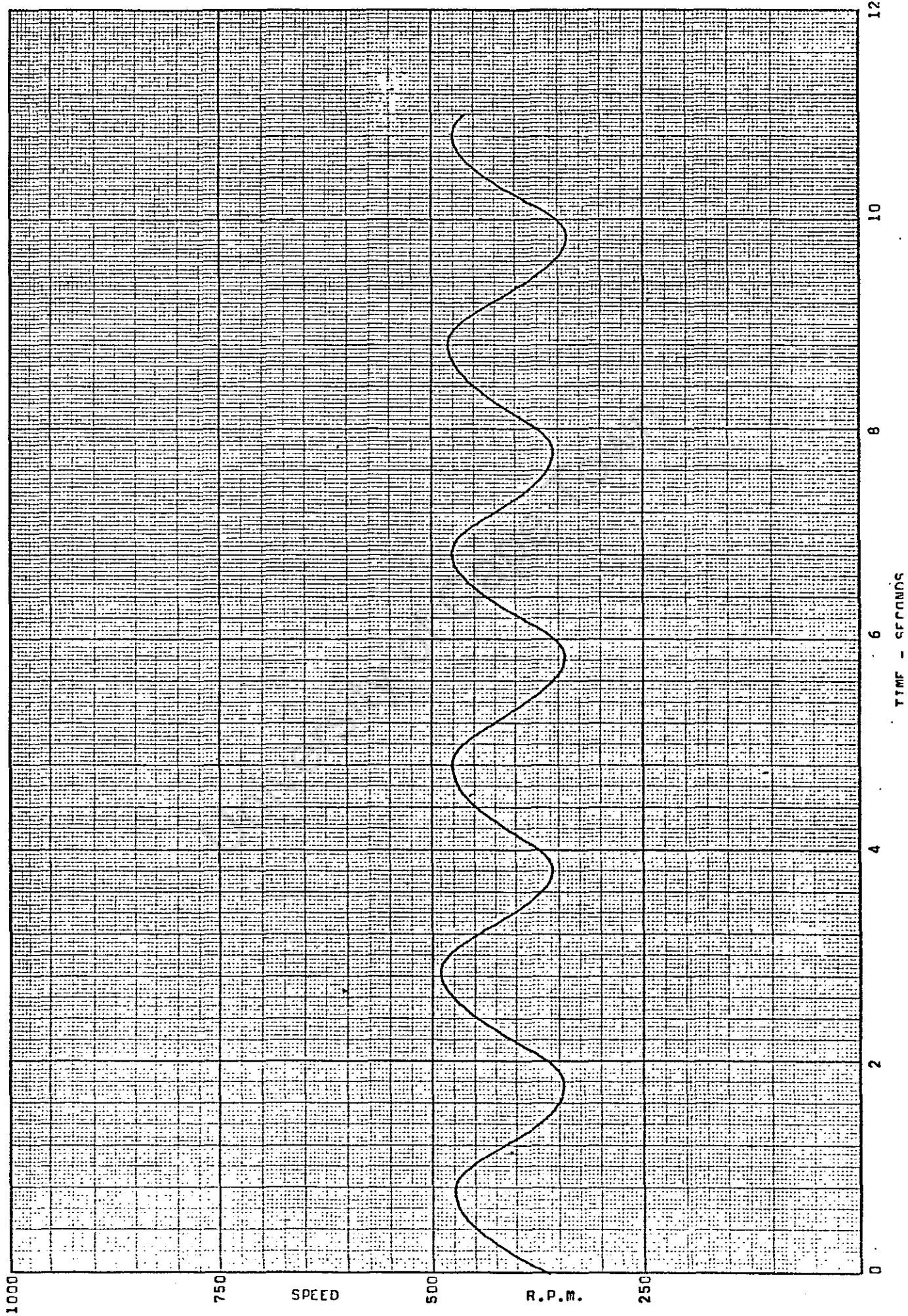


FIGURE 50

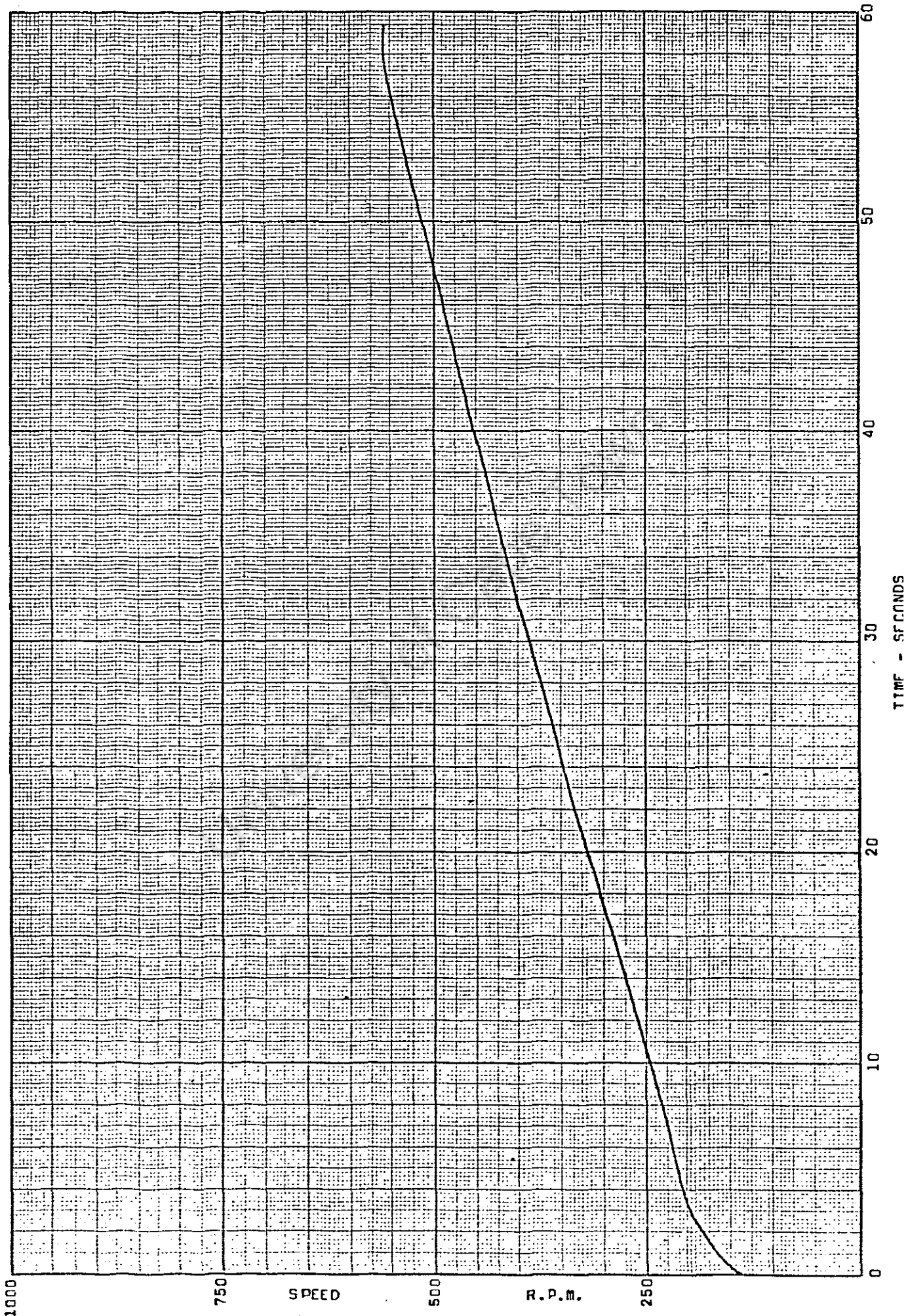


FIGURE 51

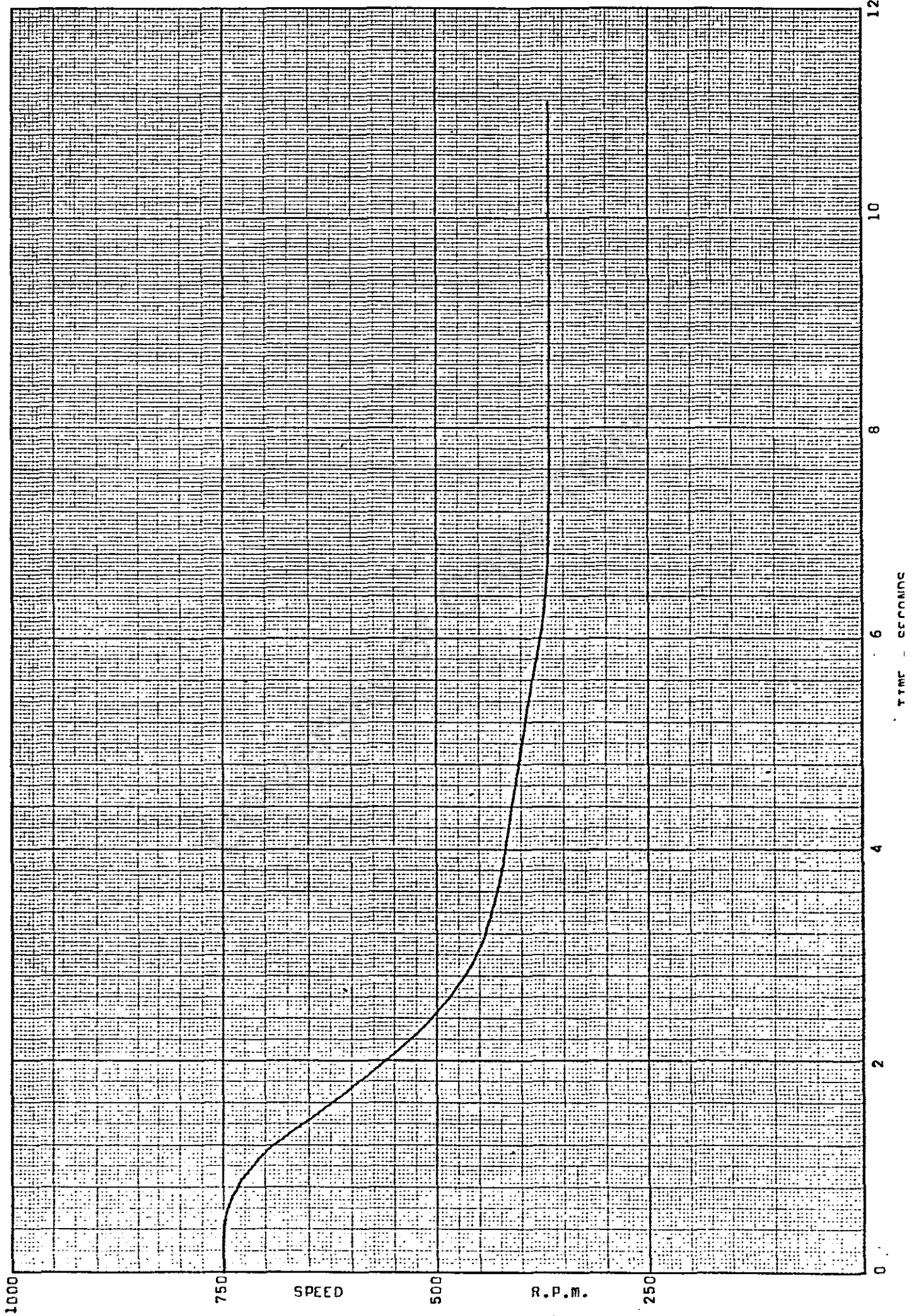


FIGURE 52

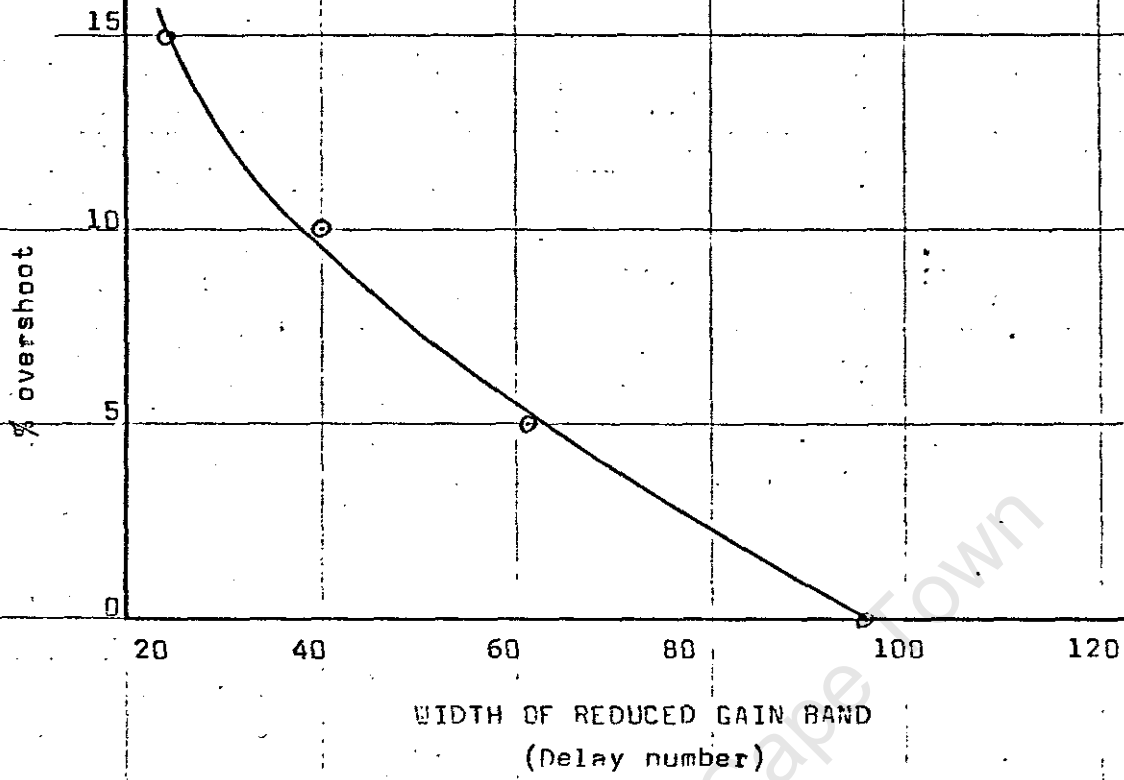


FIGURE 54

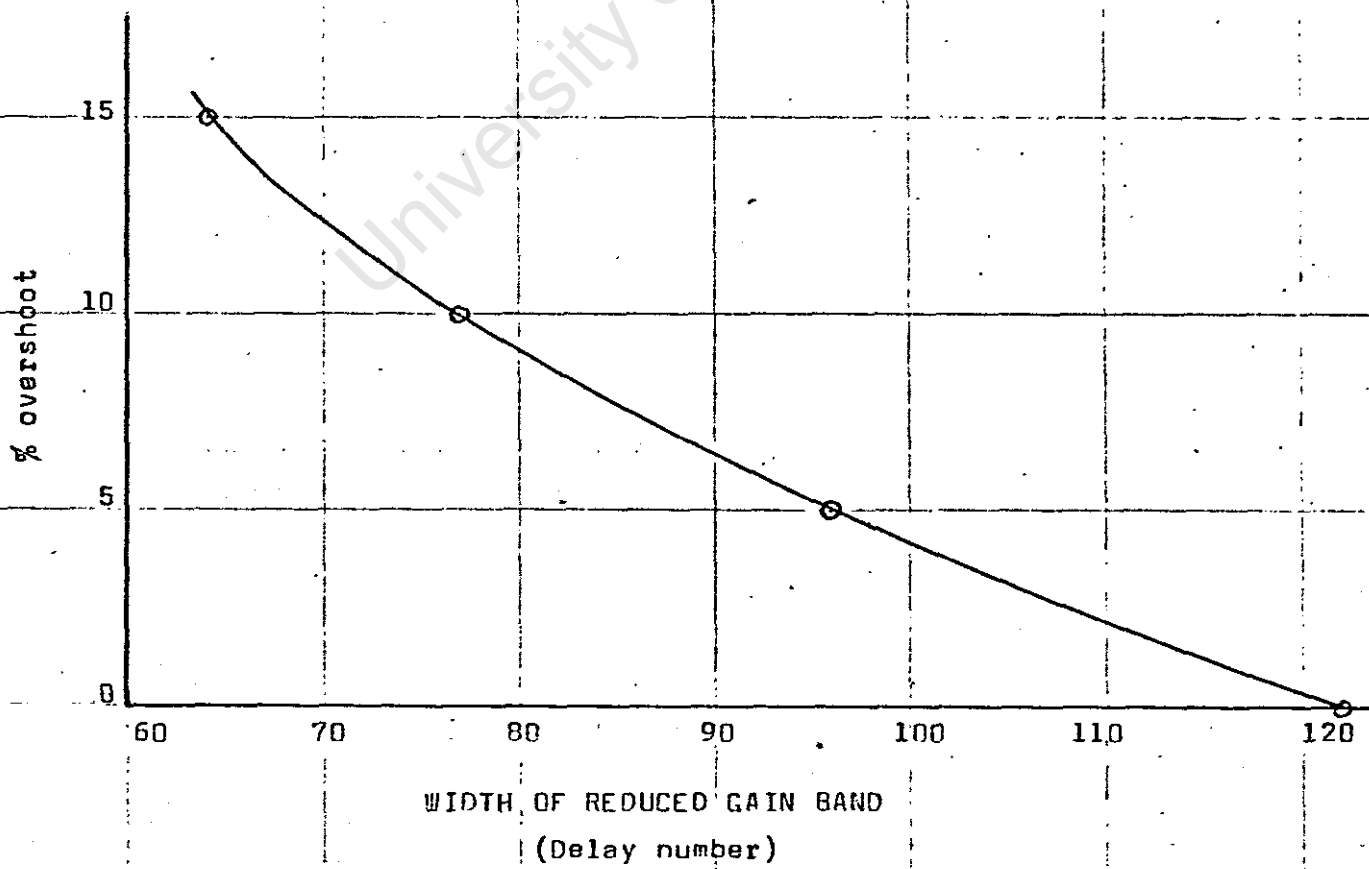


FIGURE 53

CHAPTER XCONCLUSIONS

The objects of this thesis as set out in the introduction are (i) to design and build an interface between a computer and a thyristor bridge rectifier, (ii) to write a suitable program, enabling the computer to provide closed loop speed control of a D.C. machine and (iii) to investigate the compatibility of various types of tachogenerators with the analogue to digital convertor of the computer.

The final modified interface provided what was at first thought to be complete control of the rectifier but as can be seen on most of the curves from Figures 29 - 52, a slight discontinuity reveals itself at about 300 rpm. This is caused by a loss of the trigger pulse when it immediately follows the shift pulse for the longer delays. Its behaviour is very erratic and its exact cause was never traced. Thus an interface using three binary counters offers a much neater solution to the problem, avoiding the method of address shifting used in the present interface.

When the original interface was used, the analogue delay for the thyristor was provided by the computer, necessitating it servicing the interface 300 times a second. Depending on the length of delay, it could spend up to 95% of its time in a count-down loop providing this delay. The modified interface allowed the computer to run asynchronously with it, taking less than 2% of the computer time. This frees the computer to do other tasks, such as controlling more machinery for entire system control, data logging and general calculations. It is even possible to use this interface for sampled data control, the longest sampling interval being limited only by the system being controlled.

The compensation routines developed for the computer, while perhaps not giving optimal performance for any one type of input control voltage, do produce a system which is stable at all times and provides a satisfactory response to load transients. It is unlikely that the general performance of the system can be improved but response to any particular set of circumstances can be improved at the expense of the response to other input wave-forms.

The speed of response of the system is slow but can be

improved if a thyristor bridge of greater current handling capability were used.

Digital systems are generally less affected by noise than their analogue counterparts, however, the digital computer is a tremendously complicated piece of equipment and it appears from its behaviour in the test runs on the machines to be more susceptible to noise than a simpler analogue controller. When it is affected by noise it usually means that the program is partially destroyed resulting in the computer completely losing control of the machine which usually either stops or runs up to maximum speed. This is probably the most serious drawback of the system though it should not be insurmountable. Industrially, minicomputer control, although not as closely linked with the machines as here, seems to be enjoying increasing popularity.

Failure of the computer as used in the system developed in this thesis would mean manual, open loop control of the motor by hand setting of the delay number for the thyristor bridge. This is tedious but it can be done in a case of emergency. The computer used for the experimental setup has never had a failure of the type that would render computer control of the system impossible.

A digital computer has to digitize all analogue error in processes which will always result in a quantization error in both input and output. If this quantization noise is not to affect the system, the analogue to digital, and digital to analogue conversion must always be performed with greater accuracy than that required. This was found to be so with the tachogenerator voltage that was fed back to the computer. The ripple in this signal was always sufficient to cause the analogue to digital convertor output to vary by at least one bit, but the situation frequently arose where the tacho voltage was such that the same amount of ripple caused the convertor output to vary by two bits, resulting in the D.C. motor hunting. This was eliminated by increasing the width of the dead band.

Economically, computer control of one machine is not justified. This system was mainly developed to simplify those systems where a computer would normally be used. This system eliminates the need for digital to analogue convertors of the conventional type and eliminates the need for the expensive analogue control gear normally used. If this system were used with a digital tachogenerator, the

cost of interfacing the computer would be less than R100.

Various types of tachogenerators were tested. There was no great difference between these and it was possible to use any of the various types provided that they were of reasonably high quality. If extremely high accuracy is required, the permanent magnet motor A.C. tachometer of greater than 32 poles would probably give the most satisfactory signal.

University of Cape Town

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A P P E N D I X ITHE COMPUTER

The Computer used for this Thesis is a Varian 622/1 which has 8 kilo-words of memory, each word consisting of 18 bits. Software input and output is by means of teleprinter keyboard and page printer as well as a high speed paper tape reader and punch.

This computer has a very simple input-output system where all the peripherals are controlled and accessed through a single input-output bus, which consists of eighteen parallel data lines and seven control lines. This works on the party line system where all the peripherals are connected in parallel.

Each device has an address number associated with it by means of which it may be interrogated. Logic which is physically located in the computer on what is called a peripheral device control card, performs this address decoding, as well as the decoding of instructions and generation of the responses to the computer. Normally all communications are initiated by the computer, except in the case of the Interrupt and Direct Memory Access Facilities.

The input-output instructions in which all information transfer is performed by the computer, can be divided into three groups.

- (a) Control Instructions. These are called External Control Commands by the computer manufacturer and are usually used to start or stop the peripheral device or to set the device in readiness for a particular operation. In this thesis, the instruction was used in conjunction with a special control card which allows a set of eighteen flip-flops to be controlled by means of these instructions. This was used to generate the trigger and shift pulses for the first interface and for the data transfer in the modified interface.

(b) Device Status Sense Instructions. These instructions are used to enable the computer to ascertain the status of a peripheral device preparatory to the interchange of information.

Most peripheral devices incorporate some mechanical process in their operation with the result that they are usually much slower than the computer in operation. Thus, if the computer is transferring information continuously to a peripheral device, it must first use the sense instruction to ascertain if the device is ready to transfer information.

On the special control card mentioned earlier, there are also eighteen sense lines which are available for external connection. Thus the status of external devices can be ascertained using these lines. For example, if one of these lines could monitor a current level detector, slight overloads could be detected by the computer allowing it to take corrective action before severe overloads or failure of components could occur.

(c) Data Transfer Instructions. These instructions cause the actual transfer of data between the computer and a peripheral device. These instructions usually follow a sense instruction, ensuring that valid data is about to be transferred. It is possible to transfer data directly between the peripheral device and memory or the accumulator.

There are two more facilities available which are connected to the input-output bus. There are the Interrupt and Direct Memory Access (D.M.A.) facilities.

The Interrupt Module offers a facility whereby it is possible to interrupt the computer in the program that it is executing and cause it to jump to another program to service that interrupt.

The interrupt can be generated in the computer by placing a logical nought on one of eight lines connected to the interrupt causing the computer to jump to a specific location in memory where it will find the program that services that interrupt. The module is so designed that line 0 will have highest priority, while line 1 will

generate an interrupt provided line 0 is not generating an interrupt, etc..

The D.M.A. is a facility such that it is possible to enter information directly into the memory of the computer without the program currently being executed taking any part in the process. The data transfer is initiated and controlled by the external device.

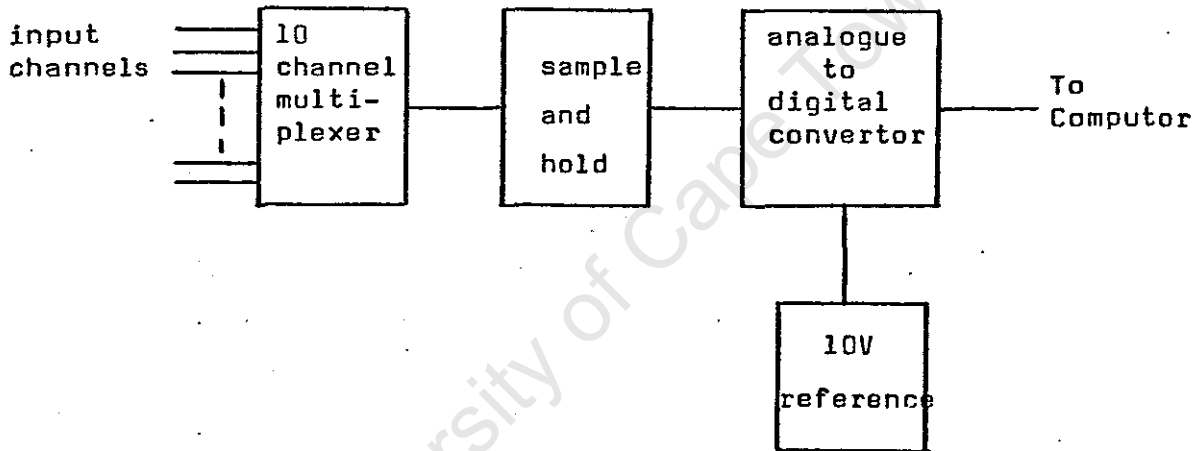
When it is required that data be transferred, the peripheral device signals the computer which then completes the execution of its current instruction, transfers one word of data between memory and peripheral device and then continues with its program until it receives another signal from the peripheral device.

The interrupt and D.M.A. facilities are the only two whereby it is possible for external devices to control the operation sequence of the computer, greatly enhancing the flexibility of this machine. It is possible to influence the computer by means of the sense lines, either directly or indirectly by causing it to wait for a certain status of an external device, but it has to wait in a program loop continually testing the line until the response is true.

In the case of these last two facilities, the computer is left free to perform other functions until the external equipment is ready to communicate with the computer. Computer response is also faster as it can take action immediately an instruction cycle is completed. In the case where the sense lines are used, it can only check once every time it goes through the program loop which will involve three or four instructions.

APPENDIX 2THE ANALOGUE TO DIGITAL CONVERTORS

The first analogue to digital convertor used was manufactured by Redcor Modules. The complete convertor system consisted of the analogue to digital convertor, a sample and hold, a 10 channel multiplexer and a 10v ref. source, all supplied with plus and minus 22,5V D.C. as shown in Figure A1.

FIGURE A1

Block diagram of analogue-to-digital convertor

The convertor has a bipolar input of 10V. It is a 12 bit convertor giving a resolution of 4,8 mV per bit and works on the principle of successive approximation giving an average conversion time of 44 sec.

The frequency bandwidth of this convertor is severely limited if its full accuracy is to be realized since the input voltage must not change by more than half a least significant bit in its conversion time. Assuming a sine wave of 10v amplitude the maximum frequency can be calculated as follows:-

Maximum rate of change of voltage is:-

$$\frac{\frac{1}{2} \text{ LSB}}{\text{conversion time}} = \frac{4,8 \times 10^{-3}}{2 \times 44 \times 10^{-6}} = 54,5 \text{ V/sec.}$$

Rate of change of voltage of a sine wave =

$$V \omega \cos \omega t$$

where V = amplitude of wave

ω = angular frequency

t = time

$$\therefore \text{Maximum rate of change} = V \omega = 10 = 54,5 \text{ V/sec.}$$

$$\therefore \omega = 5,45 \text{ rad/sec.}$$

$$\therefore f = 0,87 \text{ HZ}$$

However, the frequency response can be greatly enhanced by the addition of a sample and hold module. This is connected between the incoming signal and the analogue to digital convertor. When this device is in the sample mode, its output follows the input, but in the hold mode the output is fixed at a value corresponding to the input at approximately that time when the sample mode signal is removed. There is a delay, typically 50ns between the time when the signal is removed and when the device actually clamps its output. There is also a certain amount of uncertainty or jitter in this device. In the sample and hold used this jitter is 5ns which gives an uncertainty of 1mV in sampling a signal whose slew rate is 0,2V/s. Assuming the signal is sinusoidal and has an amplitude of 10V, the maximum frequency the device can handle is

$$\frac{0,2 \times 10^6}{2\pi \times 10} = 31,8 \text{ kHz}$$

A ten channel multiplexer is added in front of the sample and hold to increase the usefulness of the convertor. With this it is possible to have up to ten analogue devices connected to the convertor, the computer selecting the channel that is to be sampled before initiating the conversion.

The ten volt reference source is used by the analogue to digital convertor against which it compares the input signal for purposes of conversion.

During the course of this thesis, the convertor failed as a result of faulty operation of its power supply. Consequently, another analogue to digital convertor was used. This was manufactured by Analogue Devices limited and is a 10 bit convertor with a bipolar input of $\pm 5\text{v}$ giving a resolution of approximately 9,8 mV. Its conversion time is approximately 25 sec.

It can be seen from the foregoing that this type of convertor, having a fairly high frequency capability, is rather susceptible to noise. Thus the leads to the convertor from the tachogenerator, and the setpoint control had to be screened and low pass filters included in the circuit reasonably near to the convertor.

As noise from the tachogenerators, which is mainly brush noise or ripple from the AC tacho, and ripple caused by shaft eccentricities could not be reduced below about 15mV, jitter was always present in the tachogenerator readings. Thus a small deadband region always had to be incorporated in the computer program to allow for this.

A P P E N D I X 3TACHOGENERATORS

This appendix briefly lists the specifications of the tachometers used and some of the output obtained from them.

A.C. TACHOMETERS:

The first tachometer tried was a 32 pole permanent magnet rotor type with nameplate specifications as follows:-

Type - Mawdsley T.G. 210

Output voltage/1000 r.p.m. 20,1 RMS

Maximum Current 0,35a

The output voltage waveform is shown in Figure A5.

This signal was rectified and smoothed by the circuit shown in Figure A2,

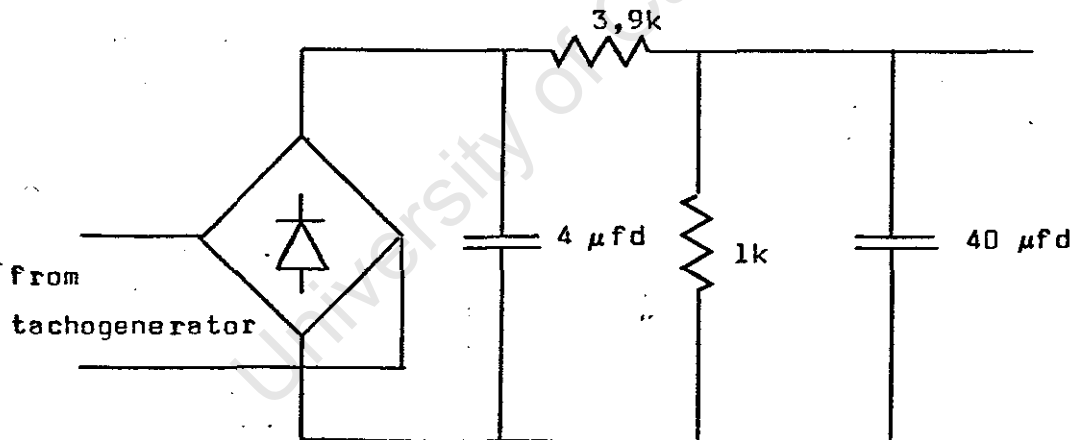


FIGURE A2

Circuit of rectifier and smoothing circuit used for Mawdsley tachogenerator

the output waveform being shown in Figure A6.

The effect of rotor misalignment can be clearly seen in this figure.

The second A.C. tachometer tried was a magslips with the following specifications:-

Type - Muirhead, Magslip - 2" Induction Generator No.1 Mk I

Input: 50Va 50 Hz - Power Consumption: 7w

Output: 7v/1000 r.p.m. in 10 K load

Source impedance 315.

To obtain a D.C. signal from this tacho with an acceptable ripple voltage, the filter time constant would be much greater than one tenth of the 400 ms time constant of the motor first used for the test runs, so it was decided to supply the tacho from a 400 Hz supply. This gave an output voltage of 3v/1000 rpm into a 10 k load. This signal required amplification, rectification and smoothing before being applied to the analogue to digital convertor.

An operational amplifier being basically an instrument amplifier has insufficient current drive to supply a capacitive input filter. When a low pass RC filter is used, the output is significantly less than the 10v maximum that the operational amplifier is capable of supplying. Thus it was necessary to use two operational amplifiers as shown in Figure A3.

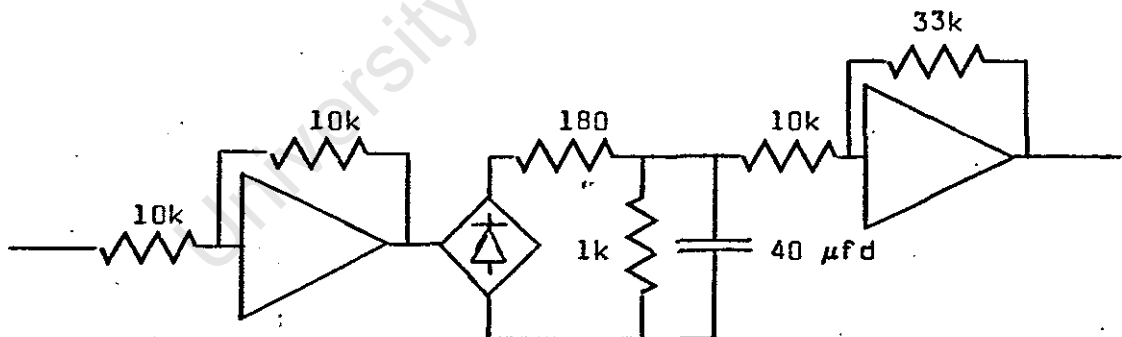


FIGURE A3

Circuit used to smooth and amplify the signal from the magslip

D.C. TACHOGENERATORS:

The first type of D.C. tachogenerator tried was the conventional type with permanent magnet field and wound armature. The generator was of the cheaper type normally

used for indication purposes. It was found this type suffered from a large amount commutation noise, making the signal totally unsuitable for the analogue to digital convertor of the computer. After the other types of tachogenerator mentioned in this appendix were tested, a high quality tachogenerator of the type just described was purchased and tested. This was found to give satisfactory results as shown in Figures A7, A8, A9.

The divider and filter circuit is shown in Figure A4.

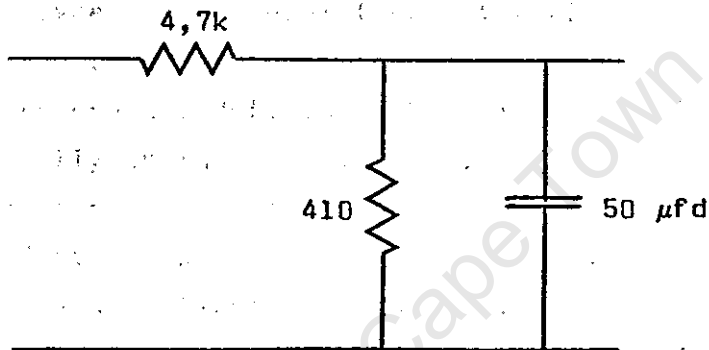


FIGURE A4

Divider and smoothing circuit used for
Hubner D.C. tachogenerator

The specifications for the tachogenerator are as follows:-

Type: Hubner TDP 0,2 - 4

Output voltage 60v/1000 r.p.m.

Maximum current 67 mA

Another type of D.C. tacho tried was the homopolar tacho. These types have small output voltages and current collecting brushes but no commutators. It was hoped that the output signal would be relatively noise free.

Two variations of this type of tachogenerator were tried.

The first one tried was one similar to that suggested by Ramshaw¹⁴. This consisted of a disc permanent magnet magnetised axially with single polarities at the faces. A brass disc was fixed in contact with this and the two rotated as one unit.

The field from the magnet could be regarded as stationary, with the disc acting as one continuous conductor rotating in the field. The advantages of this system are that no iron circuit is required and that any vibrations in the shaft do not cause spurious voltages to be introduced into the output signal because the field and conductor move as one, resulting in no relative movement between these two. The big drawback is that the output voltage is extremely small - about $1\text{mV}/1000$ r.p.m., so that the noise introduced by low noise brushes is still a few order of magnitudes bigger than the signal itself.

The second type of homopolar tachometer also has a brass disc and brushes at the centre and periphery but it has a stationary energised field with an iron circuit. With the field fully energised this produced about $0.07\text{v}/1000$ rpm, the percentage noise voltage being less than that encountered from the other tachogenerators. This signal would require amplification before being applied to the analogue to digital convertor. The output waveform is shown in Figure A10.

From the above it can be seen that the permanent magnet rotor A.C. tacho and permanent magnet field, wound armature D.C. tacho provide the simplest means for obtaining an analogue speed indication which will provide a signal capable of being read to an accuracy of better than $\pm 0.02\%$.

For greater precision the magclip or a higher quality homopolar tachometer than the type tested would provide cleaner and more accurate signals which could be processed with greater facility by the computer. These tacho-generators would, however, require stable power supplies.

RATE OF CHANGE OF TACHOGENERATOR VOLTAGE
UPON APPLICATION OF FULL LOAD TO AN
UNLOADED MACHINE.

The average unloaded D.C. shunt motor will show approximately a 5% reduction in speed as it is loaded to full load. If this is applied suddenly, the rate of change of speed will be less than that of an exponential.

The first machine used had a calculated motor time constant of 379 m sec. This being a 1500 rpm motor, the loaded machine would run at approximately 1425 rpm. Thus a step

load placed on the machine would result in a response slower than indicated by the following equation:

$$s = 1500 - 750 (1 - e^{-0,379t})$$

where s = motor speed, rpm.

t = time, seconds.

The sampling interval of the original system was 3,3 ms, thus the initial change of tachogenerator voltage in this time is as follows:-

$$V = 10 - \frac{10}{1500} \times 1500 - 750 (1 - e^{-0,379 \times 3,3 \times 10^{-3}})$$

$$= 4,3 \text{ mV}$$

where V - change in tachogenerator voltage

This is comparable with the noise present in the tachogenerator signal and so it would be impossible to detect the true rate of change of voltage which would always be less than this.

The method of operation of the analogue to digital convertor generally makes the computer more susceptible to noise in its analogue input because the sample and hold module is commanded to hold its output at any arbitrary instant relative to the input waveform. This may occur at the instant a noise spike is present on the input signal resulting in the digitisation of a voltage that is considerably in error of the true input signal.

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The method of operation of the analogue to digital convertor generally makes the computer more susceptible to noise in its analogue input because the sample and hold module is commanded to hold its output at any arbitrary instant relative to the input waveform. This may occur at the instant a noise spike is present on the input signal resulting in the digitisation of a voltage that is considerably in error of the true input signal.

FIGURE A5

Waveform of A.C.
permanent magnet rotor
tachogenerator.

Scale: $x = 1\text{ms/div}$
 $Y = 10\text{V/div}$

FIGURE A6

Waveform of output of
smoothing circuit from
A.C. tachogenerator

Scale: $x = 5\text{ms/div}$
 $Y = 10\text{mV/div}$

FIGURE A7

Waveform of output of
Hubner D.C. tachogenerator.
bottom line of graticule
is 0V.

Scale: $x = 10\text{ms/div}$
 $Y = 10\text{V/div}$

FIGURE A8

Noise of output of
Hubner D.C. tachogenerator.

Scale: $x = 10\text{ms/div}$
 $Y = 0,5\text{V/div}$

FIGURE A9

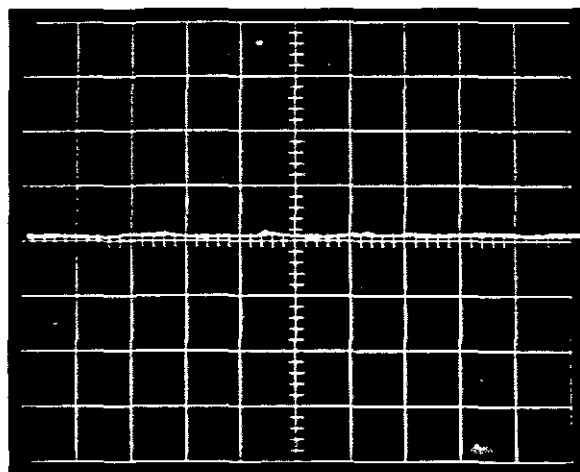
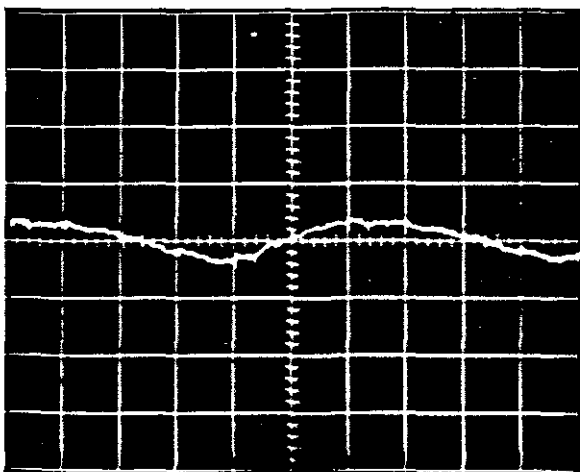
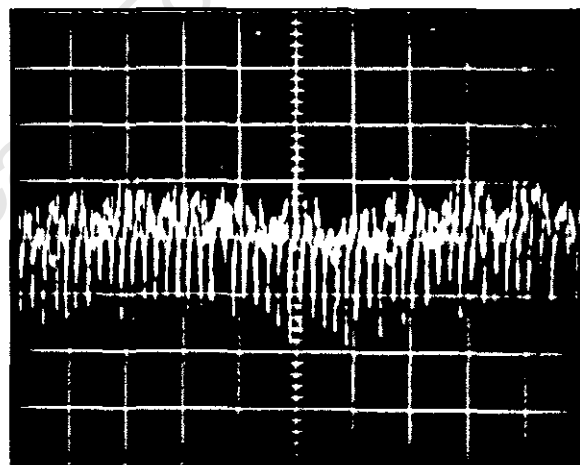
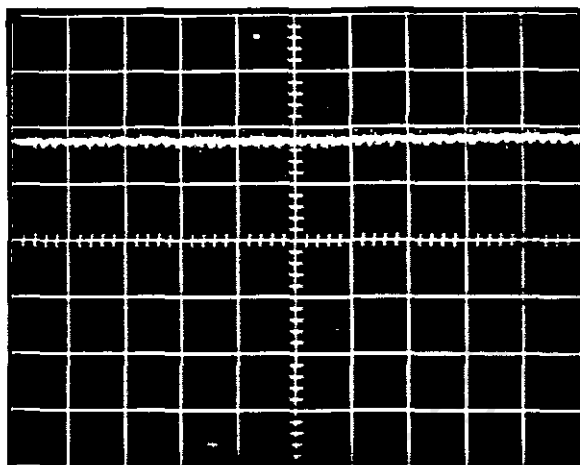
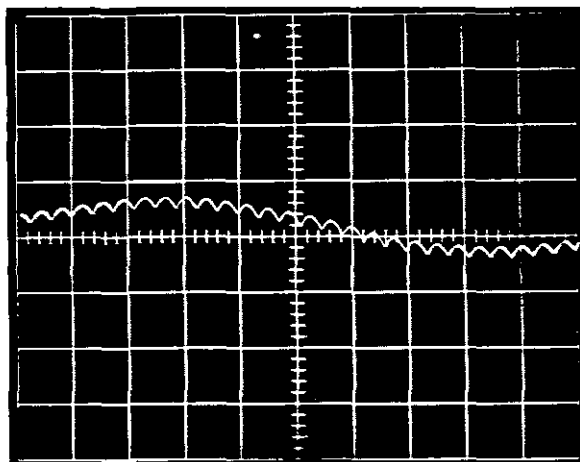
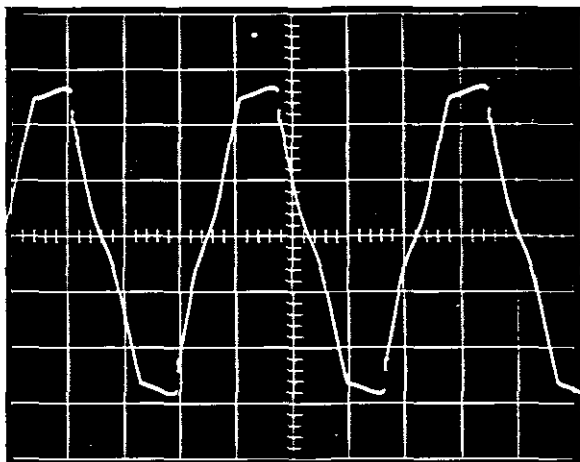
Output of smoothing circuit
connected to Hubner D.C.
tachogenerator.

Scale: $x = 10\text{ms/div}$
 $Y = 10\text{mV/div}$

FIGURE A10

Output signal of energised
field homopolar tachogenerator.
bottom line of graticule
is 0V.

Scale: $x = 10\text{ms/div}$
 $Y = 10\text{mV/div}$



A P P E N D I X 4THE POWER CIRCUIT AND MOTOR
CHARACTERISTICS

The power circuit is shown in detail in Figure A10.

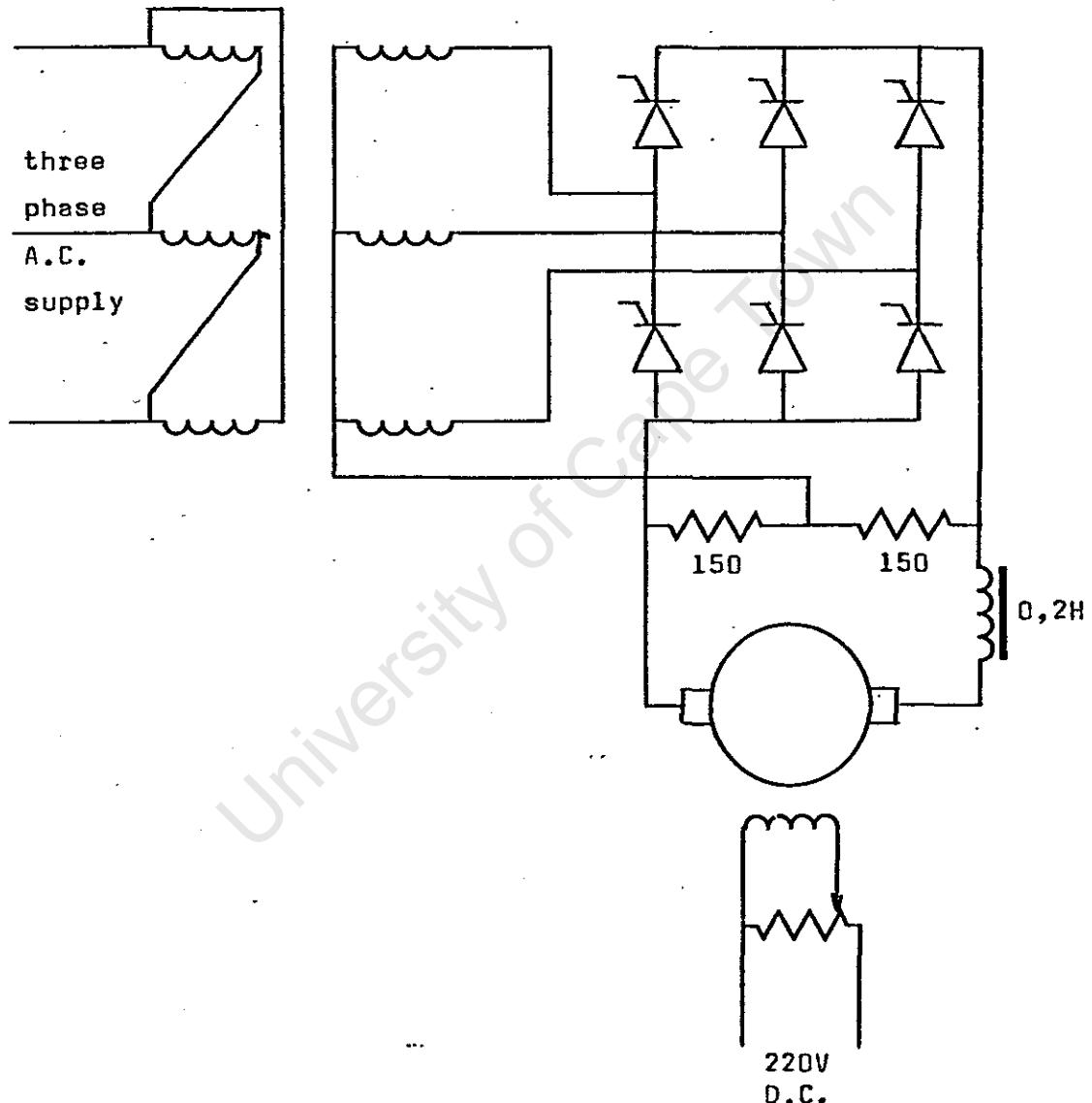


FIGURE A10

Diagram showing circuit associated with D.C. machine

Power comes from the three phase A.C. supply through a 2:1 stepdown delta-star isolation transformer which also provides the commutation reactance for the three phase fully controlled thyristor switch. The bridge consists of six R.C.A. 2N3899 thyristors which gives it a maximum

continuous current capability of 33A. Spike suppression for the thyristors is provided by a small three phase diode bridge driving on R.C. network which has an extremely low dynamic impedance. This gives protection mainly against spikes originating elsewhere in the mains supply and gives only limited protection against voltage spikes generated in the bridge itself. This is no serious drawback as voltage spikes which could be damaging to the thyristors are not normally generated in this sort of circuit.

Immediately after the bridge rectifier is the centre tapped bleeder resistor necessary for reliable operation of the thyristors. The circuit is then completed by the series inductor and the armature circuit of the D.C. shunt motor.

The series inductor allows continuous current flow in the motor armature circuit and reduces the ripple voltage present in the armature circuit. The value of the inductor was chosen using the formulae and curves given in a paper by Singleyla, taking $p' = 6$, $\cos x = 0$, $I_d = 3a$.

The frequency response is shown in the lower curve of Figure A11. This was obtained indirectly by taking the frequency response of the motor and an S.C.R. control unit (upper curve, figure A11). The frequency response of the controller was then obtained and the motor response deduced from these two.

The transient response of the motor was also taken using the computer and bridge rectifier built for this thesis. The response is shown in figure 20.

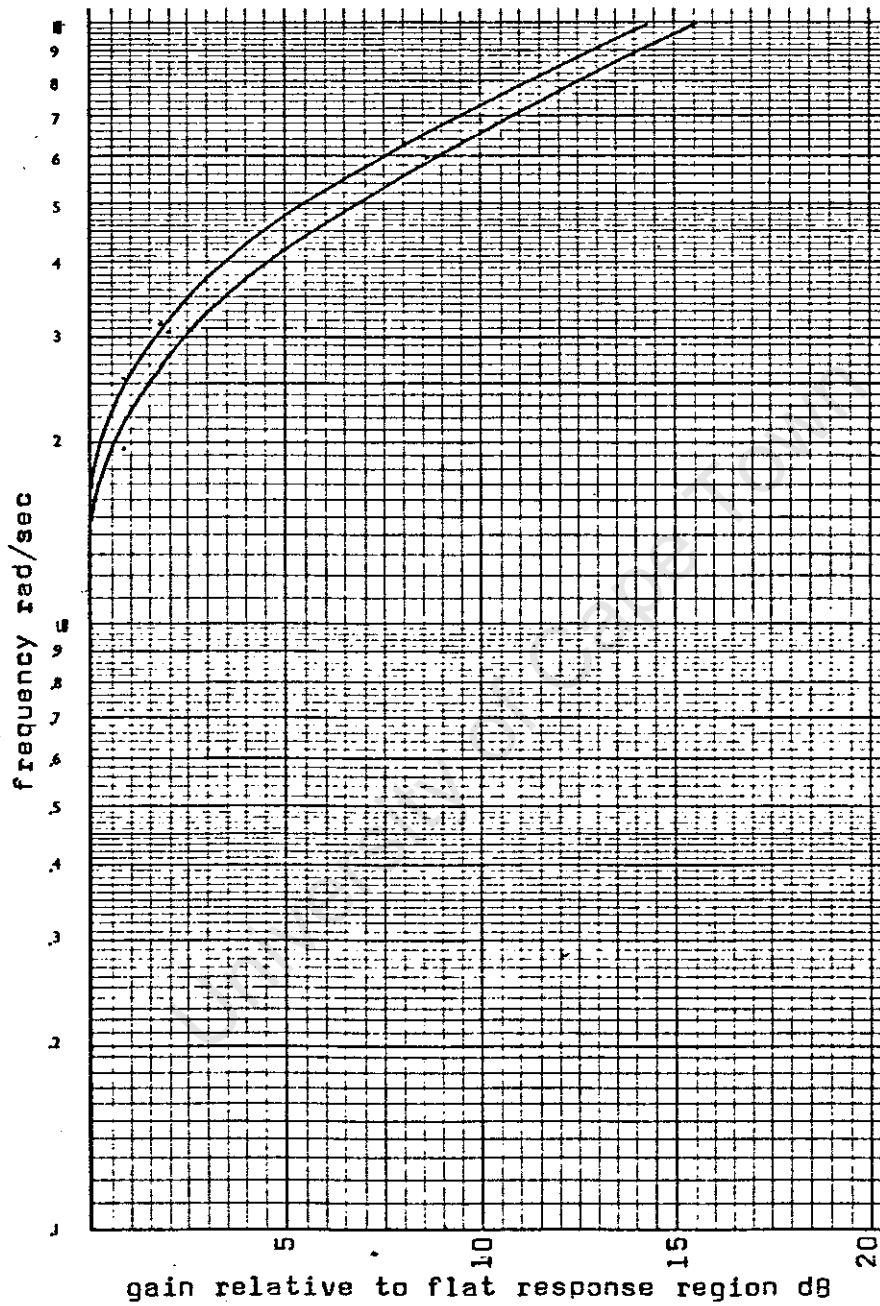


FIGURE A11

A P P E N D I X 5THE INTERFACE

The original interface is described in detail in the main text and will not be described further here. A list of semiconductors and integrated circuits is, however, given below in Table 1 and a detailed circuit diagram is given in Figure A12.

TABLE 1

List of semiconductors used in original interface.

<u>SECTION</u>	<u>DEVICE</u>	<u>TYPE</u>	<u>QUANTITY</u>
crossover detectors	diode	1N4154	6
	transistor	BC107C	6

crossover monostable multivibrator	transistor	BC107C	12

Local memory and control logic	J-K flip flop	MC 790P	3
	quad-2 input gate	MC 724P	4
	triple-3 input gate	MC 792P	1
	dual-4 input buffer gate	MC 788P	1
	dual buffer	MC 799P	1

trigger control monostable multivibrator	transistor	BC 107C	12

trigger circuit	transistor	BC 107C	6
	injunction transistor	2N2646	6

A brief description of the operation of the extension to the interface is given in the main text with a block diagram. A few further details are given here with a circuit diagram in Figure A13, and a list of integrated circuits in Table 2.

The binary counters consist of D-flip flops. These are different from the J-K flip flops in that they have only one data input and that the output changes state on the

positive going edge of the clock pulse. In the configuration in which they are wired in Figure A8 and assuming positive logic, the flip flops form a down counter, this being what is required. Unfortunately, to set these flip flops before the count starts, the present inputs would have to be used.

If the state of one flip flop is to remain unchanged while the one preceding is to be reset, the first flip flop would change state when the output of the previous one went from 0 to 1, resulting in a chain reaction with the following counters being set to 1.

This difficulty would be avoided if the clear inputs were used. Output would be taken from the complemented outputs with the counter now behaving as an up-counter. This will provide satisfactory operation if the complemented outputs of the buffer memory are fed to the counters.

The output of the gate which detects the zero state of the counter is clocked with the main oscillator in order to avoid ambiguous transitional states of the ripple counter giving false zero indications.

There are two interlocks on the trigger pulse generator. The first is in conjunction with the crossover detectors from the original interface. As soon as a crossover pulse arrives, the trigger pulse from the generator is inhibited, allowing the interface to store the address of the next thyristor to be triggered. The trigger pulse is sufficiently long for a pulse to be delivered to the interface after the crossover pulse has occurred. The second interlock derives from the shift pulse generator. This inhibits the trigger pulse generator while a shift pulse is being delivered. If the binary counter reaches zero while this pulse is present, the counter maintains this state until it is possible for the trigger pulse to be delivered.

TABLE 2

<u>SECTION</u>	<u>DEVICE</u>	<u>TYPE</u>	<u>QUANTITY</u>
memory buffer	quad latch	SN7475	2
counters and control logic	D flip flop	SN7474	10
	triple 3 input gate	SN7410	6
	quad 2 input gate	SN7400	3
	buffer driver	SN7440	1
Shift pulse generator	monostable multivibrator	SN74121	1
	quad 2 input gate	SN7400	2
Trigger pulse generator	monostable multivibrator	SN7412	1
	quad 2 input gate	SN7400	2

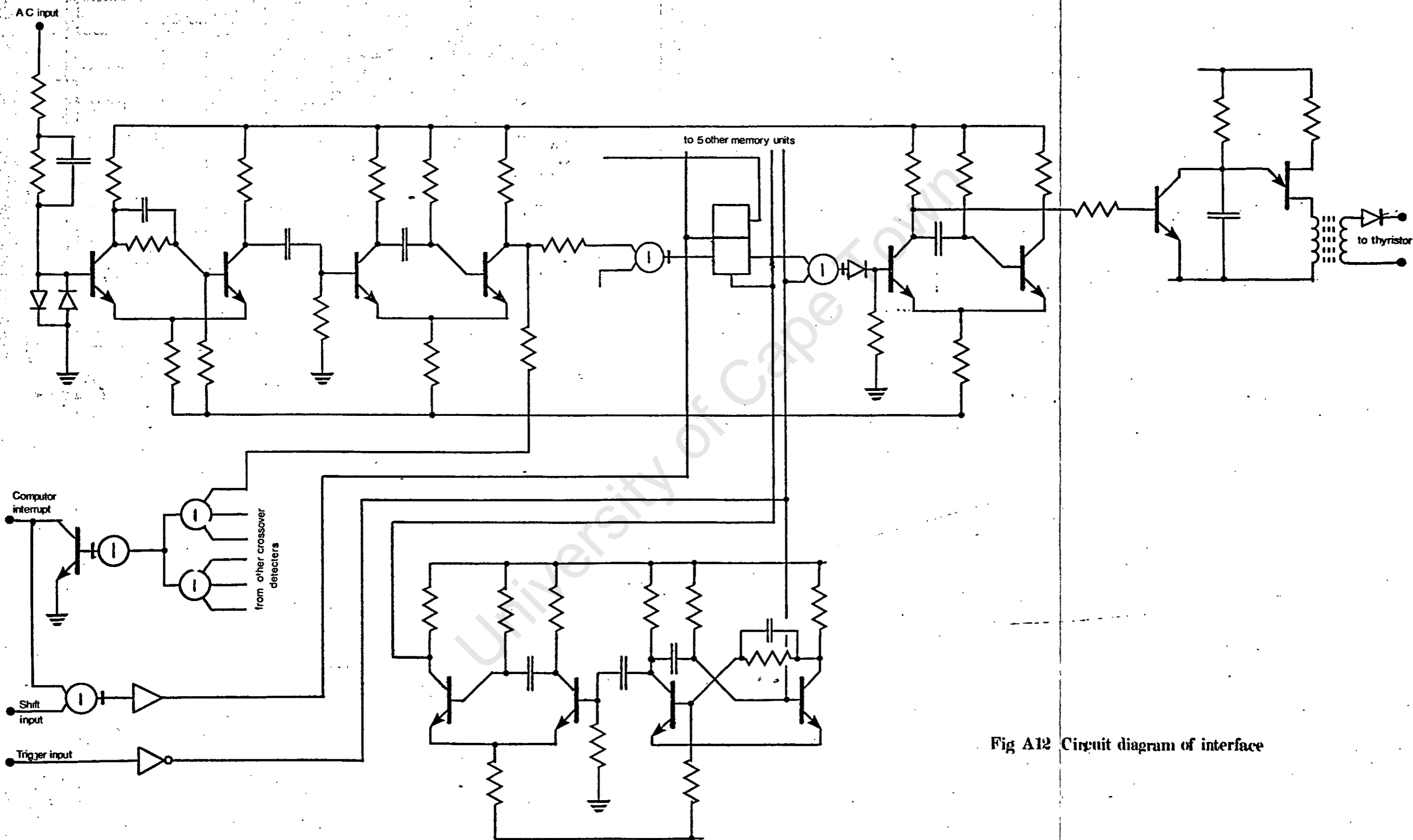


Fig A12 Circuit diagram of interface

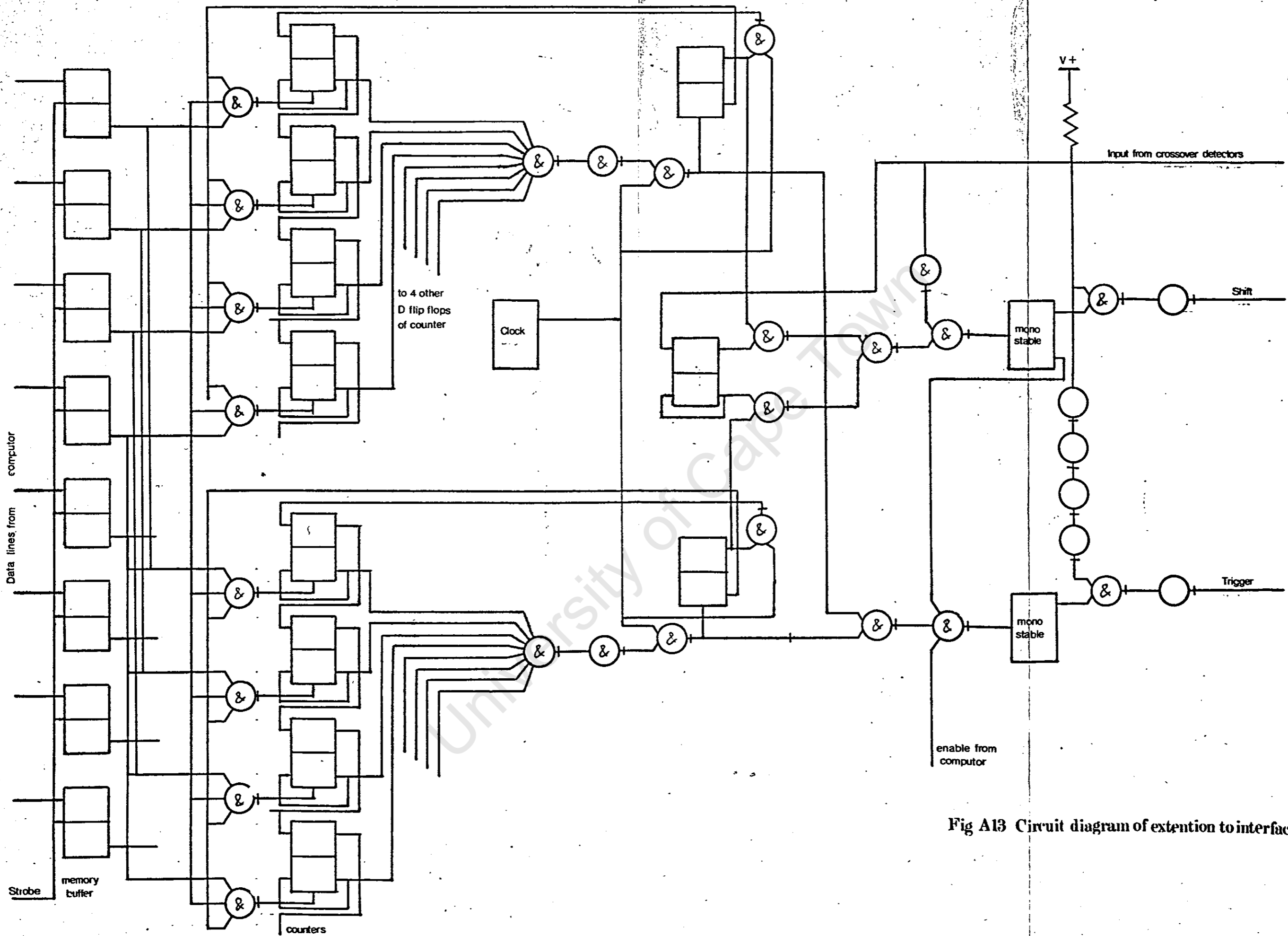
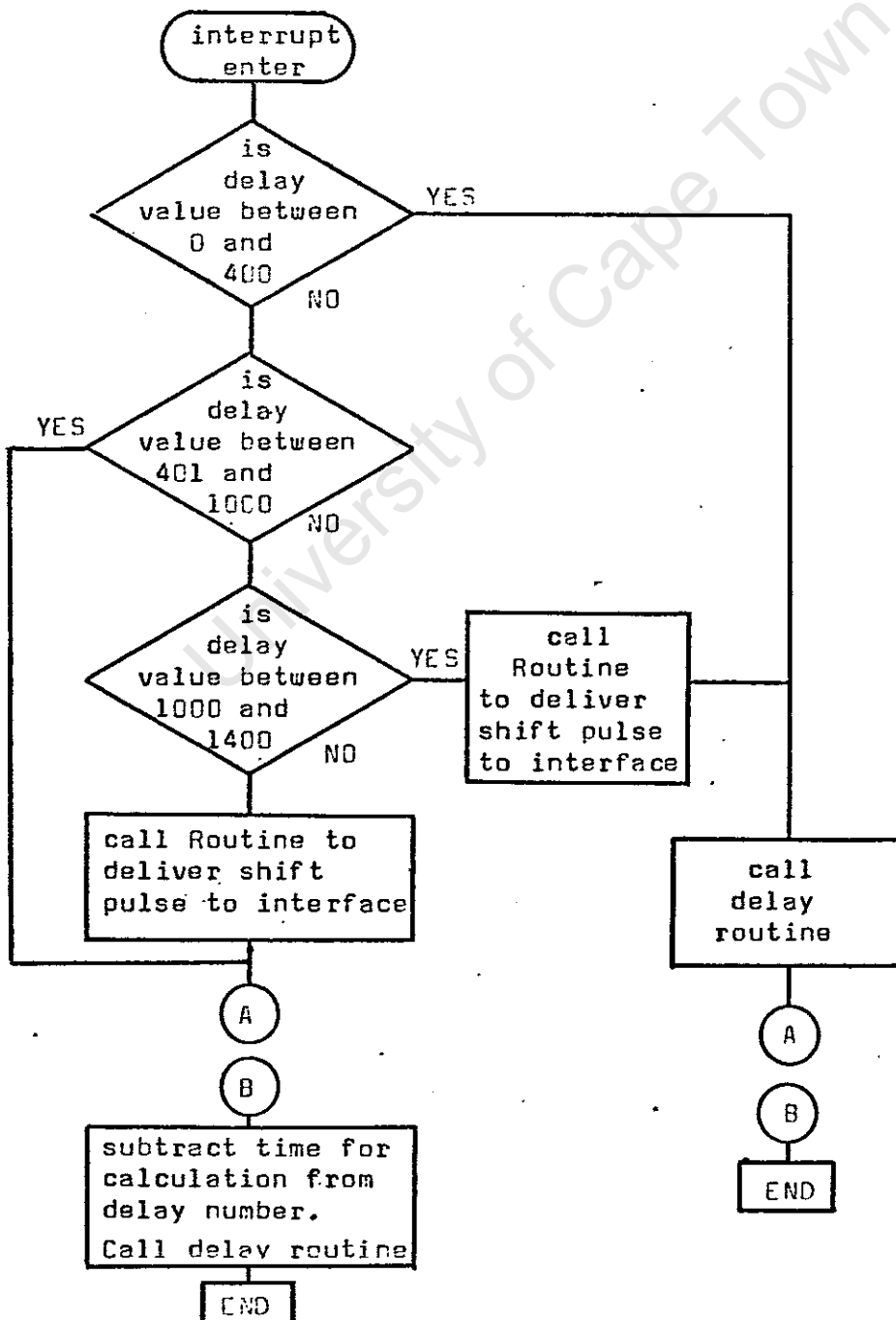
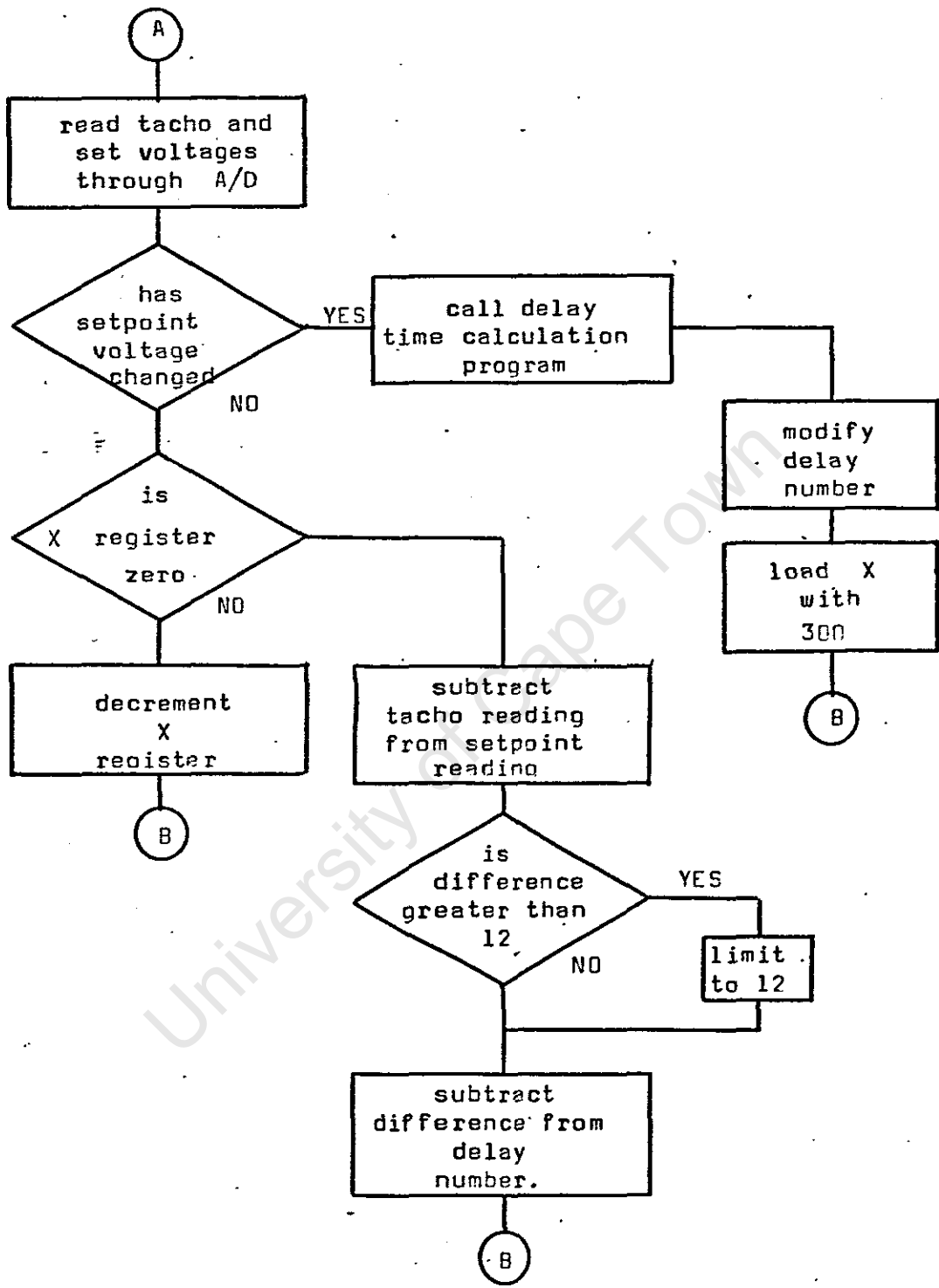


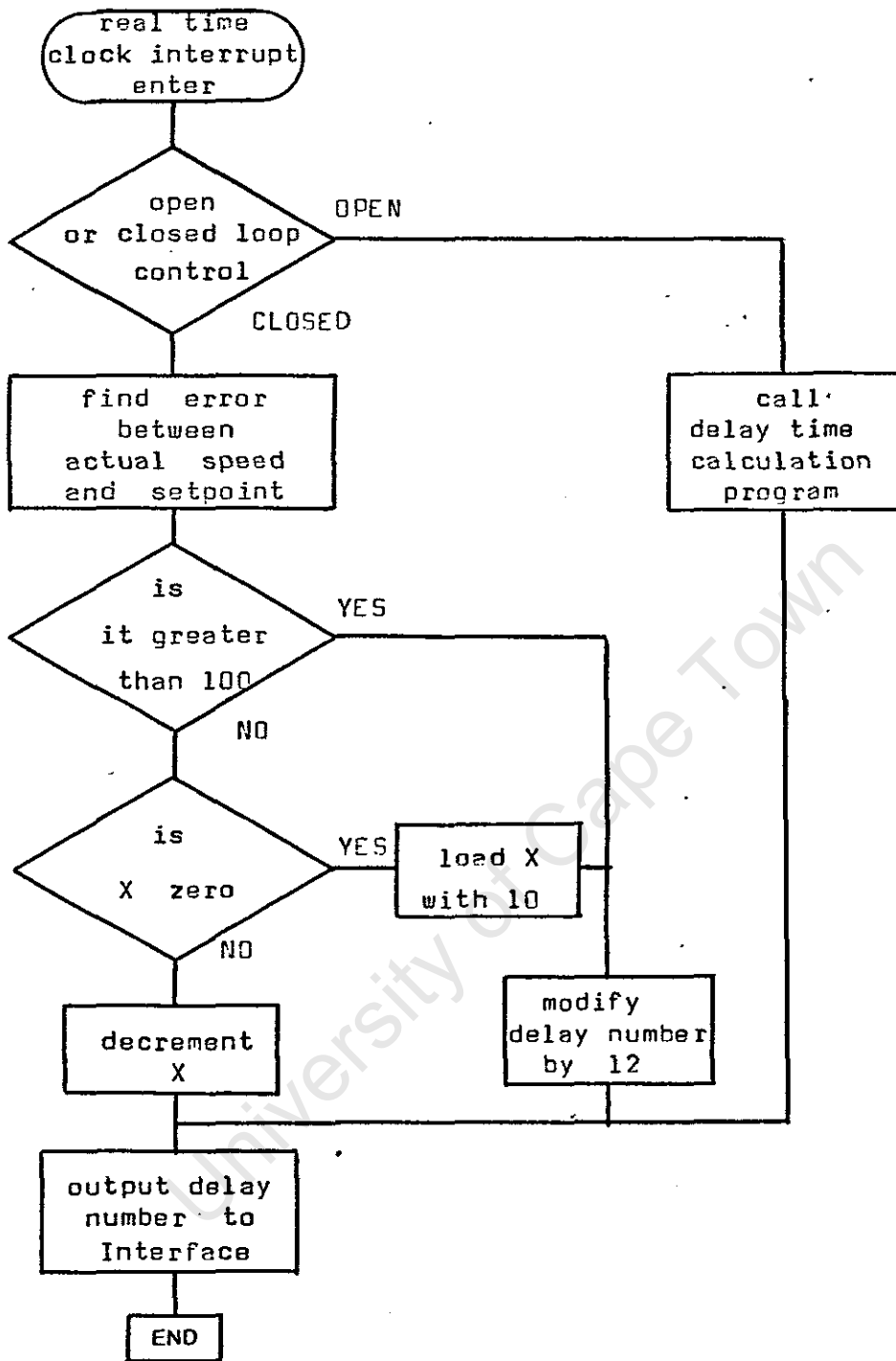
Fig A13 Circuit diagram of extension to interface

A P P E N D I X 6THE COMPUTER PROGRAMS

This appendix contains the flow diagrams and programs used for the original interface. A program used for data logging the firing delay number is also included although no chart is given as this is used in conjunction with the second control program.







SYMBOLS

0 000747 R REGI
0 000723 R FIRE
0 000715 R MAX
0 000714 R HOLD
0 000713 R SKAL
0 000670 R ALT
0 000644 R CORR
0 000636 R MU
0 000635 R LMDA
0 000607 R ERR
0 000606 R NUM
0 000562 R SPED
0 000531 R SPOD
0 000512 R EXC
0 000504 R UPDA
0 000475 R TEMP
0 000461 R TWO
0 000445 R ONE
0 000421 R DLY
0 000412 R DES
0 000411 R GAMA
0 000410 R BETA
0 000407 R ALFA
0 000377 R SHIF
0 000357 R MOD
0 000305 R PELT
0 000277 R CARB
0 000276 R ACC
0 000260 R UNUS
0 000232 R DUO
0 000212 R TRES
0 000140 R CALC
0 000122 R ORGN

 *PROGRAM FOR ON LINE SPEED CONTROL OF 1 DC *
 *MACHINE BY DETERMINING FIRING ANGLE OF *
 *THYRISTORS *
 * H.F.W. 4/12/70 *

000100			,ORG	,0100	
000100	002000		,CALL	,CALC	
000101	000140	R			
000102			,BSS	,16	
000122	006010	ORGN	,LDAI	,0	
000123	000000				
000124	103140		,OAR	,040	SET INTERRUPT
000125	100340		,EXC	,0340	
000126	005000		,NOP	,	
000127	005000		,NOP	,	
000130	005000		,NOP	,	
000131	001000		,JMP	,*-3	
000132	000126	R			
000133			,BSS	,5	
000140	000000	CALC	,ENTR	,	
000141	010276		,LDA	,ACC	
000142	006140		,SUBI	,500	
000143	000764				
000144	001004		,JAN	,UNUS	
000145	000260	R			
000146	006140		,SUBI	,01100	
000147	001100				
000150	001004		,JAN	,DUO	
000151	000232	R			
000152	006140		,SUBI	,266	
000153	000412				
000154	001004		,JAN	,TRES	
000155	000212	R			
000156	002000		,CALL	,PELT	
000157	000305	R			
000160	002000		,CALL	,REGI	
000161	000747	R			
000162	010276		,LDA	,ACC	
000163	006140		,SUBI	,02300	
000164	002300				
000165	001004		,JAN	,**+14	
000166	000203	R			
000167	050277		,STA	,CARB	
000170	006140		,SUBI	,01600	
000171	001600				
000172	001002		,JAP	,**+5	
000173	000177	R			
000174	010277		,LDA	,CARB	
000175	001000		,JMP	,**+7	
000176	000204	R			
000177	006010		,LDAI	,01600	
000200	001600				
000201	001000		,JMP	,**+4	

000202	000205	R			
000203	005001			,TZA	,
000204	005000			,NOP	,
000205	002000			,CALL	,FIRE
000206	000723	R			
000207	100240			,EXC	,0240
000210	001000			,JMP*	,CALC
000211	100140	R			
000212	010276		TRES	,LDA	,ACC
000213	002000			,CALL	,REGI
000214	000747	R			
000215	006140			,SUBI	,02300 18 34+22?
000216	002300				
000217	001002			,JAP	,**4
000220	000223	R			
000221	006010			,LDAI	,0
000222	000000				
000223	002000			,CALL	,FIRE
000224	000723	R			
000225	002000			,CALL	,PELT
000226	000305	R			
000227	100240			,EXC	,0240
000230	001000			,JMP*	,CALC
000231	100140	R			
000232	002000		DUO	,CALL	,PELT
000233	000305	R			
000234	010276			,LDA	,ACC
000235	006140			,SUBI	,193
000236	000301				
000237	001002			,JAP	,**4
000240	000243	R			
000241	050277			,STA	,CARB
000242	006140			,SUBI	,02000
000243	002000				
000244	001002			,JAP	,**5
000245	000251	R			
000246	010277			,LDA	,CARB
000247	001000			,JMP	,**4
000250	000253	R			
000251	006010			,LDAI	,1184
000252	002240				
000253	002000			,CALL	,FIRE
000254	000723	R			
000255	100240			,EXC	,0240
000256	001000			,JMP*	,CALC
000257	100140	R			
000260	010276		UNUS	,LDA	,ACC
000261	006140			,SUBI	,22
000262	000026				
000263	001002			,JAP	,**4
000264	000267	R			
000265	006010			,LDAI	,0
000266	000000				
000267	002000			,CALL	,FIRE

000270 000723 R
 000271 002000
 000272 000305 R
 000273 100240
 000274 001000
 000275 100140 R
 000276
 000277

ACC ,BSS ,1
 CARB ,BSS ,6

 *DELAY TIME CALC PROGRAM ALLOWING FOR LOAD *
 *AND SPEED VARIATIONS *

000305 000000
 000306 002000
 000307 000504 R
 000310 140415
 000311 050411
 000312 140410
 000313 001004
 000314 000322 R
 000315 010410
 000316 120413
 000317 050412
 000320 001000
 000321 000350 R
 000322 010411
 000323 001010
 000324 000357 R
 000325 020407
 000326 005311
 000327 001010
 000330 000357 R
 000331 001020
 000332 000336 R
 000333 005322
 000334 001000
 000335 000326 R
 000336 120407
 000337 020407
 000340 005111
 000341 001010
 000342 000357 R
 000343 001020
 000344 000350 R
 000345 005322
 000346 001000
 000347 000340 R
 000350 002000
 000351 000421 R
 000352 050276
 000353 006030
 000354 000454
 000355 001000
 000356 000377 R

PELT ,ENTR ,
 ,CALL ,UPDA DESIRED SPEED
 ,SUB ,DES+3
 ,STA ,GAMA
 ,SUB ,BETA
 ,JAN ,**7
 ,LDA ,BETA
 ,ADD ,DES+1
 ,STA ,DES
 ,JMP ,**24
 ,LDA ,GAMA
 ,JAZ ,MOD
 ,LDB ,ALFA
 ,DAR ,
 ,JAZ ,MOD
 ,JEZ ,**5
 ,DBR ,
 ,JMP ,*-6
 ,ADD ,ALFA
 ,LDB ,ALFA
 ,IAR ,
 ,JAZ ,MOD
 ,JEZ ,**5
 ,DBR ,
 ,JMP ,*-6
 ,CALL ,DLY
 ,STA ,ACC
 ,LDXI ,300
 ,JMP ,SHIF

```

000357 001040 MOD ,JXZ ,**7
000360 000366 R
000361 005344 ,DXR , DES SPEED UNCHANGED:MONI TERS
000362 002000 ,CALL ,SPOD ACTUAL SPEED
000363 000531 R
000364 001000 ,JMP ,SHIF
000365 000377 R
000366 002000 ,CALL ,SPOD
000367 000531 R
000370 002100 ,JS1M ,ERR
000371 000607 R
000372 002200 ,JS2M ,DIFF
*SY
000373 000000
000374 002400 ,JS3M ,INT
*SY
000375 000000
000376 050276 ,STA ,ACC
000377 020414 SHIF ,LDB ,DES+2
000400 060415 ,STB ,DES+3
000401 020413 ,LDB ,DES+1
000402 060414 ,STB ,DES+2
000403 020412 ,LDB ,DES
000404 060413 ,STB ,DES+1
000405 001000 ,JMP* ,PELT
000406 100305 R
000407 000002 ALFA ,DATA ,2
000410 000240 BETA ,DATA ,160
000411 GAMA ,BSS ,1
000412 DES ,BSS ,7
*****
*CALCULATION OF DELAY FOR SPECIFIED SPEED UNDER *
*NO LOAD. *
*****
000421 000000 DLY ,ENTR ,
000422 010412 ,LDA ,DES
000423 006140 ,SUBI ,227
000424 000343
000425 001004 ,JAN ,ONE
000426 000445 R
000427 006140 ,SUBI ,1593
000430 003071
000431 001004 ,JAN ,TWO
000432 000461 R
000433 006010 ,LDAI ,2047
000434 003777
000435 140412 ,SUB ,DES
000436 005012 ,TAB ,
000437 005001 ,TZA ,
000440 006160 ,MULI ,2
000441 000002
000442 005021 ,TBA ,
000443 001000 ,JMP* ,DLY
000444 100421 R

```

```

000445 006010 ONE ,LDAI ,227
000446 000343
000447 140412 ,SUB ,DES
000450 005012 ,TAB ,
000451 005001 ,TZA ,
000452 006160 ,MULI ,2
000453 000002
000454 005021 ,TBA ,
000455 006120 ,ADDI ,1846
000456 003466
000457 001000 ,JMP* ,DLY
000460 100421 R TWO
000461 006010 ,LDAI ,1820
000462 003434
000463 140412 ,SUB ,DES
000464 050475 ,STA ,TEMP
000465 004343 ,LSRA ,3 SUB 0.125 FROM VALUE
000466 050476 ,STA ,TEMP+1 TO ALTER SLOPE
000467 010475 ,LDA ,TEMP
000470 140476 ,SUB ,TEMP+1
000471 006120 ,ADDI ,454
000472 000706
000473 001000 ,JMP* ,DLY
000474 100421 R
000475 TEMP ,BSS ,7

```

READING IN OF DESIRED SPEED FROM ADC CHANNEL 0

```

000504 000000 UPDA ,ENTR ,
000505 006010 ,LDAI ,01
000506 000001
000507 103155 ,OAR ,055
000510 005000 ,NOP ,
000511 005000 ,NOP ,
000512 100155 EXC ,EXC ,0155
000513 101155 ,SEN ,0155,**5
000514 000520 R
000515 005000 ,NOP ,
000516 001000 ,JMP ,*-3
000517 000513 R
000520 102555 ,CIA ,055
000521 050412 ,STA ,DES
000522 001000 ,JMP* ,UPDA
000523 100504 R
000524 ,BSS ,5

```

* READING IN OF ACTUAL SPEED FROM ADC CHANNEL 1 *


```

000531 000000 SPOD ,ENTR ,
000532 006010 ,LDAI ,02
000533 000002
000534 103155 ,OAR ,055
000535 005000 ,NOP ,

```

```

000536 005000 ,NOP ,
000537 100155 ,EXC ,0155
000540 020606 ,LDB ,NUM
000541 016562 ,LDA ,SPED,2
000542 005122 ,IBR ,
000543 056562 ,STA ,SPED,2
000544 005322 ,DBR ,
000545 001020 ,JBZ ,**5
000546 000552 R
000547 005322 ,DBR ,
000550 001000 ,JMP ,*-7
000551 000541 R
000552 101155 ,SEN ,0155,**4
000553 000556 R
000554 001000 ,JMP ,*-3
000555 000551 R
000556 102055 ,IME ,055,SPED
000557 000562 R
000560 001000 ,JMP* ,SPOD
000561 100531 R
000562 SPED ,BSS ,20
000606 000011 NUM ,DATA ,9

```

* SIMPLE ERROR COMPENSATION

```

000607 000000 ERR ,ENTR ,
000610 020606 ,LDB ,NUM
000611 005122 ,IBR ,
000612 060635 ,STB ,LMDA
000613 005322 ,DBR ,
000614 016562 ,LDA ,SPED,2
000615 005322 ,DBR ,
000616 126562 ,ADD ,SPED,2
000617 001020 ,JBZ ,**4
000620 000623 R
000621 001000 ,JMP ,*-4
000622 000615 R
000623 005012 ,TAB ,
000624 005001 ,TZA ,
000625 170635 ,DIV ,LMDA
000626 060636 ,STB ,MU
000627 010412 ,LDA ,DES
000630 140636 ,SUB ,MU
000631 002000 ,CALL ,CORR
000632 000644 R
000633 001000 ,JMP* ,ERR
000634 100607 R
000635 LMDA ,BSS ,1
000636 MU ,BSS ,6

```

* SUBROUTINE CORR FOR COMPENSATION ROUTINES *

```

000644 000000 CORR ,ENTR ,
000645 001002 ,JAP ,ALT

```

000646	000670	R			
000647	005211		,CPA	,	
000650	005012		,TAB	,	
000651	005001		,TZA	,	
000652	160713		,MUL	,SKAL	
000653	060714		,STB	,HOLD	
000654	005021		,TBA	,	
000655	140715		,SUB	,MAX	MAX ERROR VALUE
000656	001002		,JAP	,**4	
000657	000662	R			
000660	001000		,JMP	,**4	
000661	000664	R			
000662	010715		,LDA	,MAX	
000663	050714		,STA	,HOLD	
000664	010276		,LDA	,ACC	
000665	120714		,ADD	,HOLD	
000666	001000		,JMP*	,CORR	
000667	100644	R			
000670	005012	ALT	,TAB	,	
000671	005001		,TZA	,	
000672	160713		,MUL	,SKAL	
000673	060714		,STB	,HOLD	
000674	005021		,TBA	,	
000675	140715		,SUB	,MAX	
000676	001002		,JAP	,**4	
000677	000702	R			
000700	001000		,JMP	,**4	
000701	000704	R			
000702	010715		,LDA	,MAX	
000703	050714		,STA	,HOLD	
000704	010276		,LDA	,ACC	
000705	140714		,SUB	,HOLD	
000706	001002		,JAP*	,CORR	
000707	100644	R			
000710	010276		,LDA	,ACC	
000711	001000		,JMP*	,CORR	
000712	100644	R			
000713	000001		SKAL	,DATA	,1
000714			HOLD	,BSS	,1
000715	000005		MAX	,DATA	,5
000716				,BSS	,5

 *TO FIRE SCR, PULSE PLACED ON LINE 054 *

000723	000000		FIRE	,ENTR	,
000724	005012			,TAB	,
000725	005001			,TZA	,
000726	006170			,DIVI	,3
000727	000003				
000730	001020		,JEZ	,**5	
000731	000735	R			
000732	005322		,DBR	,	
000733	001000		,JMP	,*-3	
000734	000730	R			

```

000735 104054 ,EXC2 ,054
000736 005000 ,NOP ,
000737 100054 ,EXC ,054
000740 001000 ,JMP* ,FIRE
000741 100723 R
000742 ,BSS ,5

```

```

*****
*TO SHIFT ADDRESS OF SCR TO BE FIRED : PULSE *
* PLACED ON LINE 0154 *
*****

```

```

000747 000000 REGI ,ENTR ,
000750 104154 ,EXC2 ,0154
000751 100154 ,EXC ,0154
000752 001000 ,JMP* ,REGI
000753 100747 R
000000 ,END ,

```

LITERALS

POINTERS

SYMBOLS

- 1 000747 R REGI
- 1 000723 R FIRE
- 1 000715 R MAX
- 1 000714 R HOLD
- 1 000713 R SKAL
- 1 000670 R ALT
- 1 000644 R CORR
- 1 000636 R MU
- 1 000635 R LMDA
- 1 000607 R ERR
- 1 000606 R NUM
- 1 000562 R SPED
- 1 000531 R SP0D
- 1 000512 R EXC
- 1 000504 R UPDA
- 1 000475 R TEMP
- 1 000461 R TWO
- 1 000445 R ONE
- 1 000421 R DLY
- 1 000412 R DES
- 1 000411 R GAMA
- 1 000410 R BETA
- 1 000407 R ALFA
- 1 000377 R SHIF
- 1 000357 R MOD
- 1 000305 R PELT
- 1 000277 R CARB
- 1 000276 R ACC
- 1 000260 R UNUS
- 1 000232 R DU0

PAGE 000011

1 000212 R TRES
1 000140 R CALC
1 000122 R ORGN

University of Cape Town

SYMBOLS

0	002457		AIS
0	002147		ACS
0	000712	R	LOG
0	000702	R	SAVA
0	000664	R	STRT
0	000657	R	PFR
0	000656	R	CON
0	000655	R	DUG
0	000654	R	COM
0	000653	R	MASK
0	000652	R	UNUS
0	000647	R	EXC
0	000621	R	LOW
0	000546	R	ADDR
0	000541	R	INTE
0	000507	R	DZN2
0	000502	R	ATTN
0	000471	R	LID
0	000465	R	DOD
0	000454	R	DZN1
0	000450	R	MOD
0	000436	R	DED
0	000430	R	ERR
0	000427	R	NUM
0	000403	R	SPED
0	000364	R	SPOD
0	000337	R	UPDA
0	000332	R	DES
0	000323	R	TEMP
0	000307	R	TWO
0	000277	R	ONE
0	000257	R	DLY
0	000252	R	LIM2
0	000246	R	OUT
0	000240	R	LIMP
0	000222	R	LIM1
0	000214	R	LIMT
0	000167	R	PELT
0	000162	R	ACC
0	000154	R	FLAG
0	000150	R	SAVE
0	000116	R	CALC
0	000045	R	PRST

```

*****
* PROGRAM FOR ON LINE CONTROL OF 1 D.C. M/C *
* SUITABLE FOR USE WITH BOTH INTERFACES IN TANDEM *
* INTERRUPT BY RTC *
* SS1 ENABLES MACHINE START UP *
* SS2 PROVIDES CLOSED LOOP CONTROL *
* SS3 PROVIDES DATA LOG OF TRIGGER DELAY NUMBER *
*****

```

```

000040          ,ORG ,040
000040 002000   ,CALL ,PFR
000041 000657 R
000042 001000   ,JMP ,STRT
000043 000664 R
000044 040045   ,INR ,**+1          RTC INSTR.
000045 037730 PRST ,DATA ,16344
000046 002000   ,CALL ,CALC
000047 000116 R

000100          ,ORG ,0100
000100 006010   ,LDAI ,0377
000101 000377
000102 050162   ,STA ,ACC          MAIN CONTROL PROG.
000103 050163   ,STA ,ACC+1
000104 006030   ,LDXI ,49
000105 000061
000106 100147   ,EXC ,0147
000107 010154   ,LDA ,FLAG
000110 002002   ,JAPM ,LOG
000111 000712 R
000112 005000   ,NOP ,
000113 005000   ,NOP ,
000114 001000   ,JMP ,**-5
000115 000107 R
000116 000000   CALC ,ENTR ,
000117 050150   ,STA ,SAVE
000120 060151   ,STB ,SAVE+1
000121 070152   ,STX ,SAVE+2
000122 006010   ,LDAI ,16344
000123 037730
000124 050045   ,STA ,PRST
000125 001100   ,JSS1 ,**+5
000126 000132 R
000127 100050   ,EXC ,050
000130 001000   ,JMP ,**+7
000131 000137 R
000132 104050   ,EXC2 ,050          ENABLE INTERFACE
000133 002000   ,CALL ,PELT
000134 000167 R
000135 002000   ,CALL ,LIMT
000136 000214 R
000137 002000   ,CALL ,ADDR
000140 000546 R
000141 005101   ,INCR ,1

```

```

000142 050154      ,STA  ,FLAG
000143 010150      ,LDA  ,SAVE
000144 020151      ,LDB  ,SAVE+1
000145 030152      ,LDX  ,SAVE+2
000146 001000      ,JMP* ,CALC

```

```

000147 100116 R
000150      SAVE ,BSS ,4
000154 000000      FLAG ,DATA ,0
000155      ,BSS ,5
000162      ACC  ,BSS ,5

```

```

*****
* SPEED CONTROL PROGRAM
*****

```

```

000167 000000      PELT ,ENTR ,
000170 002000      ,CALL ,UPDA
000171 000337 R
000172 002000      ,CALL ,SP0D
000173 000364 R
000174 001200      ,JSS2 ,**7
000175 000203 R
000176 002000      ,CALL ,DLY
000177 000257 R
000200 050162      ,STA  ,ACC
000201 001000      ,JMP* ,PELT
000202 100167 R
000203 002000      ,CALL ,ERR
000204 000430 R
000205 001000      ,JMP* ,PELT
000206 100167 R
000207      ,BSS ,5

```

```

*****
* SUBROUTINE TO LIMIT MAX RATE OF CHANRE OF DLY *
*****

```

```

000214 000000      LIMT ,ENTR ,
000215 010162      ,LDA  ,ACC          LATEST DELAY
000216 140163      ,SUB  ,ACC+1        PREVIOUS DELAY
000217 001004      ,JAN  ,**8
000220 000227 R
000221 006140      ,SUBI ,12
000222 000014
000222      LIM1 ,BES ,0
000223 001004      ,JAN  ,OUT
000224 000246 R
000225 001000      ,JMP  ,LIMP
000226 000240 R
000227 120252      ,ADD  ,LIM2
000230 001002      ,JAP  ,OUT
000231 000246 R
000232 010163      ,LDA  ,ACC+1
000233 140252      ,SUB  ,LIM2
000234 050163      ,STA  ,ACC+1
000235 050162      ,STA  ,ACC

```

```

000236 001000      ,JMP* ,LIMT
000237 100214 R
000240 010163      LIMP ,LDA ,ACC+1
000241 120222      ,ADD ,LIM1
000242 050163      ,STA ,ACC+1
000243 050162      ,STA ,ACC
000244 001000      ,JMP* ,LIMT
000245 100214 R
000246 010162      OUT  ,LDA ,ACC
000247 050163      ,STA ,ACC+1
000250 001000      ,JMP* ,LIMT
000251 100214 R
000252

```

LIM2 ,BSS ,5

*CALCULATION OF DELAY FOR SPECIFIED SPEED UNDER *
* NO LOAD *

```

000257 000000      DLY  ,ENTR ,
000260 010332      ,LDA ,DES
000261 006140      ,SUBI ,57
000262 000071
000263 001004      ,JAN ,ONE
000264 000277 R
000265 006140      ,SUBI ,397
000266 000615
000267 001004      ,JAN ,TWO
000270 000307 R
000271 006010      ,LDAI ,511
000272 000777
000273 140332      ,SUB ,DES
000274 004301      ,ASRA ,1
000275 001000      ,JMP* ,DLY
000276 100257 R
000277 006010      ONE ,LDAI ,57
000300 000071
000301 140332      ,SUB ,DES
000302 004301      ,ASRA ,1
000303 006120      ,ADDI ,462
000304 000716
000305 001000      ,JMP* ,DLY
000306 100257 R
000307 006010      TWO ,LDAI ,455
000310 000707
000311 140332      ,SUB ,DES
000312 050323      ,STA ,TEMP
000313 004343      ,LSRA ,3
000314 050324      ,STA ,TEMP+1
000315 010323      ,LDA ,TEMP
000316 140324      ,SUB ,TEMP+1
000317 006120      ,ADDI ,115
000320 000163
000321 001000      ,JMP* ,DLY
000322 100257 R
000323          TEMP ,BSS ,7

```

SUB 0.125 FROM VALUE
TO ALTER SLOPE

```

000332      DES ,BSS ,5
*****
*READING IN OF DESIRED SPEED FROM ADC CHANNEL 0 *
*****
000337 000000      UPDA ,ENTR ,
000340 006010          ,LDAI ,0
000341 000000
000342 103155          ,OAR ,055
000343 005000          ,NOP ,
000344 005000          ,NOP ,
000345 100155          ,EXC ,0155
000346 101155          ,SEN ,0155,**5
000347 000353 R
000350 005000          ,NOP ,
000351 001000          ,JMP ,*-3
000352 000346 R
000353 102055          ,IME ,055,DES
000354 000332 R
000355 001000          ,JMP* ,UPDA
000356 100337 R
000357          ,BSS ,5
*****
* READING IN OF ACTUAL SPEED FROM ADC CHANNEL 1 *
*****
000364 000000      SPOD ,ENTR ,
000365 006010          ,LDAI ,01
000366 000001
000367 103155          ,OAR ,055
000370 005000          ,NOP ,
000371 005000          ,NOP ,
000372 100155          ,EXC ,0155
000373 101155          ,SEN ,0155,**4
000374 000377 R
000375 001000          ,JMP ,*-3
000376 000372 R
000377 102055          ,IME ,055,SPED
000400 000403 R
000401 001000          ,JMP* ,SPOD
000402 100364 R
000403          SPED ,BSS ,20
000427 000011      NUM ,DATA ,9
*****
*          COMPENSATION ROUTINE          *
*****

000430 000000      ERR ,ENTR ,
000431 010403          ,LDA ,SPED
000432 140332          ,SUB ,DES
000433 001004          ,JAN ,**9
000434 000444 R
000435 006140          ,SUBI ,28
000436 000034
000436          DED ,BES ,0
000437 001004          ,JAN ,DZN1

```

000440	000454	R		
000441	120436		,ADD	,DED
000442	001000		,JMP	,**6
000443	000450	R		
000444	120436		,ADD	,DED
000445	001002		,JAP	,DZN2
000446	000507	R		
000447	140436		,SUB	,DED
000450	120162		MOD	,ADD ,ACC
000451	050162		,STA	,ACC
000452	001000		,JMP*	,ERR
000453	100430	R		
000454	070541		DZN1	,STX ,INTE
000455	030542		,LDX	,INTE+1
000456	001040		,JXZ	,**5
000457	000463	R		
000460	040542		,INR	,INTE+1
000461	001000		,JMP*	,ERR
000462	100430	R		
000463	120436		,ADD	,DED
000464	006140		,SUBI	,2
000465	000002			
000465			DOD	,BES ,0
000466	001004		,JAN*	,ERR
000467	100430	R		
000470	006140		,SUBI	,5
000471	000005			
000471			LID	,BES ,0
000472	001002		,JAP	,**5
000473	000477	R		
000474	120471		,ADD	,LID
000475	001000		,JMP	,**3
000476	000500	R		
000477	010471		,LDA	,LID
000500	005000		,NOP	,
000501	006020		,LDBI	, -10
000502	777766			
000502			ATTN	,BES ,0
000503	060542		,STB	,INTE+1
000504	030541		,LDX	,INTE
000505	001000		,JMP	,MOD
000506	000450	R		
000507	070541		DZN2	,STX ,INTE
000510	030542		,LDX	,INTE+1
000511	001040		,JXZ	,**4
000512	000515	R		
000513	040542		,INR	,INTE+1
000514	001000		,JMP*	,ERR
000515	100430	R		
000516	140436		,SUB	,DED
000517	120465		,ADD	,DOD
000520	001002		,JAP*	,ERR
000521	100430	R		
000522	120471		,ADD	,LID

```

000523 001004      ,JAN ,**5
000524 000530 R
000525 140471      ,SUB ,LID
000526 001000      ,JMP ,**5
000527 000533 R
000530 010471      ,LDA ,LID
000531 005211      ,CPA ,
000532 005111      ,IAR ,
000533 005000      ,NOP ,
000534 020502      ,LDB ,ATTN
000535 060542      ,STB ,INTE+1
000536 030541      ,LDX ,INTE
000537 001000      ,JMP ,MOD
000540 000450 R
000541
INTE ,BSS ,5
*****
* SCALING AND ADDRESS DECODING OF DLY *
*****

000546 000000      ADDR ,ENTR ,
000547 070655      ,STX ,DUO
000550 006030      ,LDXI ,-7
000551 777771
000552 010162      ,LDA ,ACC
000553 001004      ,JAN ,**9
000554 000564 R
000555 050654      ,STA ,COM
000556 006140      ,SUBI ,0400
000557 000400
000560 001002      ,JAP ,**7
000561 000567 R
000562 001000      ,JMP ,**6
000563 000570 R
000564 005001      ,TZA ,
000565 001000      ,JMP ,**3
000566 000570 R
000567 010656      ,LDA ,CON
000570 050652      ,STA ,UNUS
000571 005002      ,TZB ,
000572 005101      ,INCR ,1
000573 004541      ,LLSR ,1
000574 004441      ,LLRL ,1
000575 050653      ,STA ,MASK
000576 150652      ,ANA ,UNUS
000577 001010      ,JAZ ,**4
000600 000603 R
000601 002000      ,CALL ,EXC-1
000602 000646 R
000603 010647      ,LDA ,EXC
000604 006120      ,ADDI ,0100
000605 000100
000606 050647      ,STA ,EXC
000607 001040      ,JXZ ,**6
000610 000615 R

```

```

000611 005144      ,IXR      ,
000612 010653      ,LDA      ,MASK
000613 001000      ,JMP      ,*-15
000614 000574 R
000615 104150      ,EXC2     ,0150
000616 100150      ,EXC      ,0150
000617 010647      ,LDA      ,EXC
000620 006140      ,SUBI     ,04000
000621 004000
000621          LOW ,BES      ,0
000622 050647      ,STA      ,EXC
000623 006030      ,LDXI     , -7
000624 777771
000625 010647      ,LDA      ,EXC
000626 006140      ,SUBI     ,0100
000627 000100
000630 050647      ,STA      ,EXC
000631 002000      ,CALL     ,EXC-1
000632 000646 R
000633 001040      ,JXZ      ,**+5
000634 000640 R
000635 005144      ,IXR      ,
000636 001000      ,JMP      ,*-8
000637 000626 R
000640 010647      ,LDA      ,EXC
000641 120621      ,ADD      ,LOW
000642 050647      ,STA      ,EXC
000643 030655      ,LDX      ,DUO
000644 001000      ,JMP*     ,ADDR
000645 100546 R
000646 000000      ,ENTR     ,
000647 104051 EXC   ,DATA     ,0104051
000650 001000      ,JMP*     ,EXC-1
000651 100646 R
000652          UNUS ,BSS      ,1
000653          MASK ,BSS      ,1
000654          COM  ,BSS      ,1
000655          DUO  ,BSS      ,1
000656 000377          CON  ,DATA     ,0377

```

* PF/R SERVICE ROUTINE *

```

000657 000000          PFR ,ENTR     ,
000660 050702          ,STA      ,SAVA
000661 060703          ,STB      ,SAVA+1
000662 070704          ,STX      ,SAVA+2
000663 000000          ,HLT      ,
000664 010657          STRT ,LDA      ,PFR
000665 141000          ,SUB      ,01000
000666 001004          ,JAN      ,0102
000667 000102
000670 006010          ,LDAI     ,0377

```

```

000671 000377
000672 050162      , STA , ACC
000673 050163      , STA , ACC+1
000674 100147      , EXC , 0147
000675 010702      , LDA , SAVA
000676 020703      , LDB , SAVA+1
000677 030704      , LDX , SAVA+2
000700 001000      , JMP* , PFR
000701 100657 R
000702 000000      SAVA , DATA , 0, 0, 0
000703 000000
000704 000000
000705              , BSS , 5

```

* PROGRAM TO STORE FIRING DELAY READGS *

```

000712 000000      LOG , ENTR ,
000713 005001      , TZA ,
000714 050154      , STA , FLAG
000715 001400      , JSS3 , ++4
000716 000721 R
000717 001000      , JMP* , LOG
000720 100712 R
000721 001040      , JXZ* , LOG
000722 100712 R
000723 010162      , LDA , ACC
000724 006055      , STAE , ACS, 1
000725 002147
000726 010163      , LDA , ACC+1
000727 006055      , STAE , AIS, 1
000730 002457
000731 005344      , DXR ,
000732 001000      , JMP* , LOG
000733 100712 R
          002147      ACS , EQU , 02147
          002457      AIS , EQU , 02457
          000100      , END , 0100

```

LITERALS

POINTERS

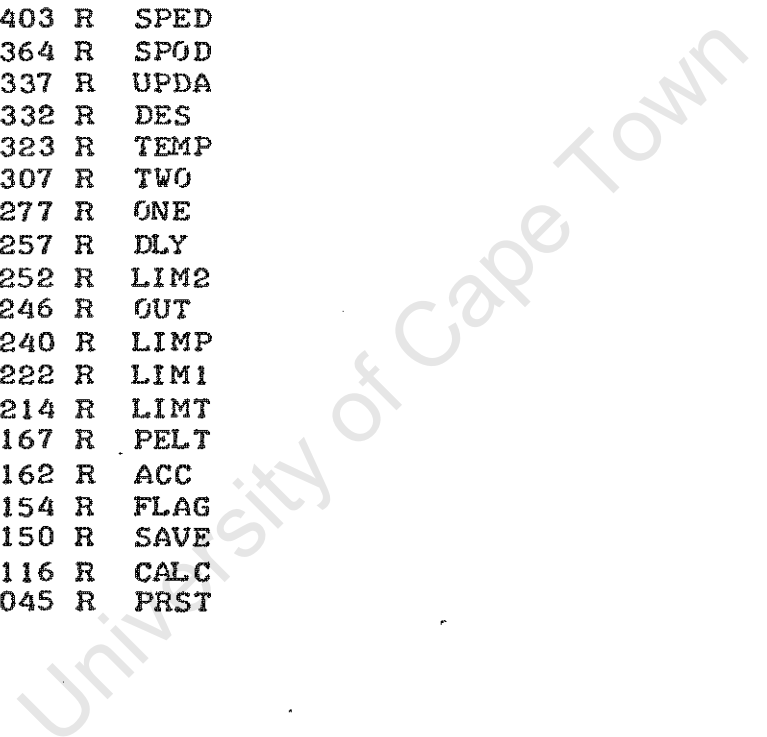
SYMBOLS

```

1 002457 AIS
1 002147 ACS
1 000712 R LOG
1 000702 R SAVA
1 000664 R STRT
1 000657 R PFR
1 000656 R CON
1 000655 R DUO

```

1 000654 R COM
1 000653 R MASK
1 000652 R UNUS
1 000647 R EXC
1 000621 R LOW
1 000546 R ADDR
1 000541 R INTE
1 000507 R DZN2
1 000502 R ATTN
1 000471 R LID
1 000465 R DOD
1 000454 R DZN1
1 000450 R MOD
1 000436 R DED
1 000430 R ERR
1 000427 R NUM
1 000403 R SPED
1 000364 R SPOD
1 000337 R UPDA
1 000332 R DES
1 000323 R TEMP
1 000307 R TWO
1 000277 R ONE
1 000257 R DLY
1 000252 R LIM2
1 000246 R OUT
1 000240 R LIMP
1 000222 R LIM1
1 000214 R LIMT
1 000167 R PELT
1 000162 R ACC
1 000154 R FLAG
1 000150 R SAVE
1 000116 R CALC
1 000045 R PRST



 * LOG OF FIRING DELAY READINGS IN CONJUNCTION *
 * WITH TAPE FOR CONTROL OFM/C WITH D. B. *
 * TAPE DATED 29/3/72 *

002000			,ORG ,02000
002000	002000		,CALL ,CRLF
002001	002116	R	
002002	006030		,LDXI ,50
002003	000062		
002004	002000		,CALL ,BDC,ACS
002005	002022	R	
002006	002147	R	
002007	002000		,CALL ,BDC,AI S
002010	002022	R	
002011	002457	R	
002012	012141		,LDA ,MARK
002013	002002		,JAPM ,CRLF
002014	002116	R	
002015	001040		,JXZ ,0100
002016	000100		
002017	005344		,DXR ,
002020	001000		,JMP ,*-10
002021	002006	R	
002022	000000		BDC ,ENTR ,
002023	072142		,STX ,INTR
002024	032022		,LDK ,BDC
002025	025000		,LDB ,0,1
002026	062032		,STB ,**4
002027	042022		,INR ,BDC
002030	032142		,LDX ,INTR
002031	006025		,LDBE ,0,1
002032	000000		
002033	006030		,LDXI ,2
002034	000002		
002035	005001		,TZA ,
002036	006170		,DIVI ,10
002037	000012		
002040	006055		,STAE ,STOR,1
002041	002143	R	
002042	001040		,JXZ ,**5
002043	002047	R	
002044	005344		,DXR ,
002045	001000		,JMP ,*-7
002046	002036	R	
002047	006030		,LDXI ,-2
002050	777776		
002051	006015		,LDAE ,STOR+2,1
002052	002145	R	
002053	006120		,ADDI ,0260
002054	000260		
002055	002000		,CALL ,PUN
002056	002100	R	

002057	001040		,JXZ	,**+5
002060	002064	R		
002061	005144		,IXR	,
002062	001000		,JMP	,*-8
002063	002052	R		
002064	006010		,LDAI	,0240
002065	000240			
002066	002000		,CALL	,PUN
002067	002100	R		
002070	032142		,LDX	,INTR
002071	001000		,JMP*	,BDC
002072	102022	R		
002073			,BSS	,5
002100	000000	PUN	,ENTR	,
002101	101537		,SEN	,0537,**+4
002102	002105	R		
002103	001000		,JMP	,*-2
002104	002101	R		
002105	103137		,GAR	,037
002106	042141		,INR	,MARK
002107	001000		,JMP*	,PUN
002110	102100	R		
002111			,BSS	,5
002116	000000	CRLF	,ENTR	,
002117	006010		,LDAI	,0215
002120	000215			
002121	002000		,CALL	,PUN
002122	002100	R		
002123	006010		,LDAI	,0212
002124	000212			
002125	002000		,CALL	,PUN
002126	002100	R		
002127	006010		,LDAI	,-71
002130	777671			
002131	052141		,STA	,MARK
002132	001000		,JMP*	,CRLF
002133	102116	R		
002134			,BSS	,5
002141		MARK	,BSS	,1
002142		INTR	,BSS	,1
002143		STOR	,BSS	,4
002147		ACS	,BSS	,200
002457		AI S	,BSS	,200
	002000		,END	,02000

LITERALS

POINTERS

SYMBOLS

1 002457 R AIS
 1 002147 R ACS