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Doctoral Thesis

Electrical performance and use in logic of printed current switching transistors employing nanostructured silicon

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Declaration of Authorship

I, Serges ZAMBOU, declare that this thesis titled, 'Electrical performance and use in logic of printed current switching transistors employing nanostructured silicon' and the work presented in it are my own. I confirm that:

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- Where I have consulted the published work of others, this is always clearly attributed.
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" Education is the most powerful weapon which you can use to change the world."

Nelson Mandela

Abstract

Printed electronics seek to replace a full range of conventional electronic components and circuits with their printed counterparts, and offer an extraordinary range of advantages in producing flexible, low-cost, large area coverage, stretchable, wearable devices and circuits. We already witness the incredible advantages and extraordinary contribution of printed electronics in our daily lives, as well as in the cutting-edge printed electronics innovations and research available today. At an in-depth level, and as an important contribution to printed devices, this work presents the design, production, and characterization of a novel fully printed current-driven switch, referred to here as a Current Switching Transistor (CST). The CST possesses the unique ability to operate as a two-way switch for both direct (DC) and alternating current (AC). In this thesis, CSTs were successfully used for the fabrication of flexible fundamental "AND" and "OR" logic gates.

At the fundamental level, this work sets out to illustrate that, a printed nanostructured silicon layer could be used as the active material for current switching transistors and other electronic devices. Also investigated was the temperature dependence of the transfer characteristics, in an extended range of temperature from 340 to 10 K, as well as their reliability when subjected to a constant current bias stress. Significantly in this work, the switching behavior observed and the electrical properties of the CSTs produced using nanostructured silicon remained excellent at temperatures as low as 10 K. Such transistor performance demonstrates the transistor's high potential as the candidate for cryogenic applications. The transistor's mechanism of operation was shown to be based on the activated percolation of charge carriers through the network of particles in the active silicon layer. Additionally, this work shows that the ON/OFF ratio of the transistors was temperature dependent, yielding the highest value of 10^3 achieved at cryogenic temperatures below 150 K. A reliability test achieved through bias stressing the base terminal, with a constant voltage of 52 V or a current of 75 μA for up to 6 hours at room temperature proved the devices to be highly stable. Except for the reversible shift in the switching voltage, which could be attributed to self-heating, no alteration of the device characteristics was observed.

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Contents

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Chapter 1

Introduction

In recent years, printed electronics have received a great deal of attention largely to their high potential in a range of applications, including amongst others, sensory skins [1–3], smart packaging [4, 5], flexible [6–9], wearable [10–13] and stretchable electronics [14–16]. Also referred to as macroelectronics [17, 18], printed electronics mainly seek to create fully functional devices and circuits, using a particular printing technique, unlike conventional electronics where the progress is driven by the overall size reduction of electronics component or devices per unit area [6]. For applications where performance and speed are not the first requirements, printed electronics offer greater advantages over conventional electronics [19, 20]. Printed electronics is cost-effective, allow large area printing, and the possibility of producing devices with complex innovative designs such as: flexible displays [21, 22], smart clothing [23], printed thermistors [24], flexible photovoltaics [25, 26]. Alongside these advantages offered by printed electronics, one of the challenges is to produce adequate electronic inks [27–31] for the printing of passive, active, capacitive and reactive devices capable of operating like their conventional counterparts. A further challenge is to deposit the inks in the form of thin or thick film in appropriate sequences, in such a way that it creates functional devices and circuits.

During the recent surge in printed electronics research, much of the attention has been given to organic [32–34] and molecular electronics [35, 36], which mostly rely, on the use of polymers, organic or molecular inks in device production. On the other hand, organic materials used in printed electronics are still limited by their stability and mobility compared to inorganic material [34, 35]. However, due to the fact that, inorganic materials show better electric mobility, scalability, and control of properties, increased attention is being given to the use of inorganic materials in printing electronics. It is noticed, therefore, that several inorganic inks have been reported for the fabrication

of printed devices, including silicon [30, 37, 38], transparent oxides, chalcogenides, and other compound semiconductor inks [6].

Transistors are widely used as switches in computing, gate logic, display driving, integrated circuits (IC), and radio-frequency identification tags (RFIDs) [35, 39–42]. For increased competitiveness, printed transistors should be able to perform similar tasks as their conventional counterparts. Due to differences in production processes, however, it is not always possible to produce printed analogs of existing devices. For instance, to date, there is no account of printed bipolar junction transistor (BJT), due to the difficulty in printing pnp or npn interfaces. The transistor presented in this thesis, which adds to the family of printed devices, is a novel type of transistor referred to as the Current Switching Transistor (CST). The CSTs are produced on flexible substrates, using nanostructured silicon material as an active layer, with a unique mode of operation. Unlike conventional transistors that operate by field modulation of charge carriers, the CSTs conduction mechanism relies on an activated transport of charge carriers within a percolation network of silicon particles.

Although transistors have traditionally been used for direct current (DC) switching, in recent years there have been an increasing number of reports on the use of transistors and diodes in AC signal processing [43–46]. Alternating current (AC) is widely used in machine drivers, control equipment and electronics [43, 47]. In most circuits, the AC signal is first converted into DC due to the inability of some electronics devices or components to operate in AC. Transistors were originally built for their amplification, but nowadays, they are largely used as switches in circuits [48, 49]. Switching both AC and DC current/voltage is essential for many applications and circuits in computing industries [50, 51]. It is standard to switch a DC signal with a transistor, although there are reports on transistors and diodes operating directly with small AC signals [37, 43, 52]. However, it is worth noting that there have not been to date, reports of single transistor capable of switching an AC signal. In general, to switch AC signal, a circuit made of solid state devices such as reversely switched dynistor(RSD) [53–55], silicon-controlled rectifier (SCR)[56–58], TRIACs [58, 59] are often used. The CST present in this thesis thus attempts to close this gap. It introduces a transistor that is capable of switching both DC and AC signals. The AC switching is made possible both by the conduction mechanism of the printed nanostructured silicon [24, 60] and the operation mechanism of the CST which switches the preferred carrier path between pairs of terminals once the carriers have enough energy to cross internal barriers in the material.

As device performance being critical feature in electronics [61], usually involving electrical, mechanical and thermal performance, this thesis largely focuses on the design, production, and characterization of silicon-based fully printed transistors, working both

in direct and alternating current. The CSTs are produced on flexible substrates at room temperature by screen printing without any other additive process. Furthermore, transistors are characterized in DC and AC to demonstrate their switching performance and establish their operation mechanism. Various performance studies are carried out on the devices including : (1) variable temperature measurement over a wide range of temperature in order to establish the thermal behavior and devices' stability; (2) a dimensional study to establish the overall change in the device performance when their characteristic dimensions change; (3) bias stress tests which demonstrate the device reliability and correlate the thermal behavior as the device heats up under bias. Finally, attention was also given to the use of CSTs as building blocks for fundamental logic gates.

Chapter 2 introduces relevant background literature on silicon, doping and the invention and operation mechanism of conventional transistors. This chapter also covers switches and highlights the use of transistors as switches. The chapter ends with an overview of transistors production, and the use of paper as substrates in printed electronics. Chapter 3 presents the various design and architecture of CSTs used for this work and describes the main apparatus and experimental setup used for electrical characterization. The basic mode of the CST operation is discussed along with the presentation of preliminary results based on a model of CSTs. Chapter 4 focuses on the building of fundamental logic gates using the CSTs as building blocks. Chapter 5 discusses the performance and operation of the transistors. Different models of CSTs will be characterized under ambient conditions, and at variable temperatures. Testing of reliability of the CSTs to current stress is also investigated in this chapter. In chapter 6, we characterize and discuss the operation of the CST in AC-AC signal. The operation mechanisms of switching AC signal using a single CST is discussed as well. The conclusion of this work is presented in chapter 7.

Chapter 2

General Background

The work presented in this chapter focuses chiefly on the development of a transistor that functions as a current-driven switch that is capable of switching both AC and DC signals, as well as its application in gate logic. In this regard, the first section sets out the adequate context that will provide a suitable background to the work, and provide the necessary theoretical knowledge to fully grasp the findings of this work.

The properties of silicon will be discussed in 2.1 as silicon was used as the principal active material of transistors developed in this work. A general knowledge of transistors, their mode of operation, and fabrication will be provided in section 2.2.

Nowadays, transistors are mainly used as electronic switches in gate logic and displays [62–65], section 2.3, provides a background to switches in general, with a particular emphasis on electronic switches. Another section 2.4 will be base on the methods used to produce the transistors. Lastly section 2.5 will provide a general knowledge on the use of paper as substrates in printed electronics , followed by the chapter's conclusion.

2.1 Silicon

Since the electronics revolution in the 1950s, and due to its electronic and mechanical properties silicon has been the most widely used material in electronics [66–69]. At room temperature, silicon is a solid and naturally crystallizes in a diamond structure with a face-centered cubic lattice. Its basic structure is made of two identical atoms at the positions $\{(0,0,0),(\frac{1}{4},\frac{1}{4},\frac{1}{4})\}$ in the unit cell with a lattice parameter of 5. 431 nm as shown in figure 2.1a.

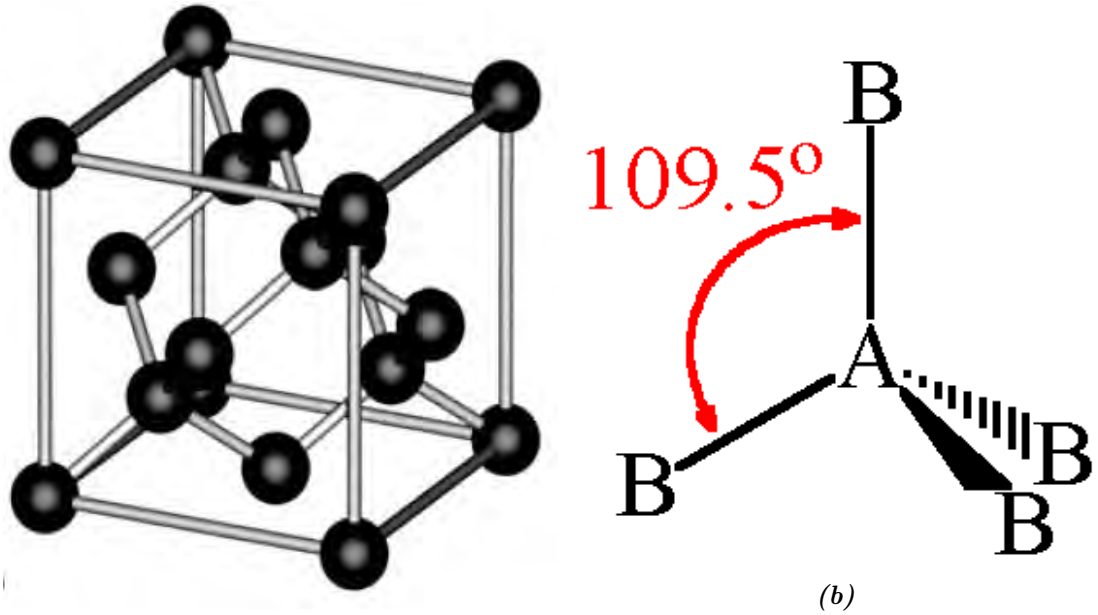


Figure 2.1: *(a) Crystal structure of silicon showing the tetrahedral bond arrangement [70, 71]. (b) Present the tetrahedral structure with its approximated angle of 109.5° between the covalent bond of A and B. Adapted from [70, 71]*

In this regard, the microstructure of silicon falls into in three main categories: single crystalline, polycrystalline, and amorphous. Single crystalline silicon is a three dimension material which is periodic, and highly ordered within its microstructure over a long range. Polycrystalline silicon is made of many small silicon crystals, with a random orientation located as domains, and separated by grain boundaries [72, 73]. Unlike the other two forms of silicon, amorphous silicon is principally made of an atomic arrangement of silicon which only has short range order [74, 75].

Various grades of silicon are used in electronics, these include: metallurgical silicon with a level of purity by atoms of 98% [73, 76]; polycrystalline silicon with a purity level of 99.99999999% [73]; and silicon single crystal, in ingot or wafer forms, with an atomic concentration of impurity atoms less than 10^{-12}.

2.1.1 Silicon doping

At 300 K in intrinsic or pure silicon, the carrier concentration is approximately $1.0 \times 10^{10}\text{cm}^{-3}$ [77]. With a carrier concentration as low as the one above-mentioned, most electronic devices such as transistors, diodes, integrated circuits will not properly operate. For instance, the operation of thin film transistor on AMOLED displays required an electron concentrations of approximately 10^{21}cm^{-3} or 10^{16}cm^{-3} when made of a

transparent conductive oxide (TCO) or an amorphous oxide semiconductor (AOS) respectively [78]. For most electronic application such as transistors, and logic gates [37], the carrier concentration needs to be higher, therefore the intrinsic semiconductor, can be doped. Doping is described as the intentional addition of electrically active impurities to a semiconductor [77].

A doped semiconductor is obtained by adding either donors or acceptors to an intrinsic semiconductor. Donors are impurities that contribute electrons to the conduction band, while acceptors are impurities that accept electrons from the valence band and create holes.

Generally, for Si and Germanium (Ge) belonging to the group IV of the periodic table, the typical donors are from the group V(P, As, Sb), and the acceptors from the group III (B, Al, Ga, In). Silicon is an indirect band gap semiconductor, so the maximum of its valence band and the minimum of the conduction band are at different positions in the Brillouin zone, with a bandgap of 1.17 eV and 1.124 eV respectively at 0 K and 300 K. During doping, the donors or acceptors are ionized, either giving away or accepting an electron. Therefore the electrical conductivity of the semiconductor is modified, and a new ground state of energy is created. The energy necessary to free an electron from a donor atom, taking it into a conduction band, is called the donor ionisation energy and (E_d), the energy necessary to take an electron from the valence band is called the acceptor ionisation energy (E_a).

Acceptor type	B	Al	Ga	In
E_a (meV)	45	57	65	16
Donor type	P	AS	Sb	
E_d (meV)	45	49	39	

Table 2.1: *Acceptor and donor ionisation energies in Si, from various elements of group III and IV [79].*

Table 2.1 gives some common value of ionization energies while doping silicon with elements respectively from groups III and V. After the doping, the semiconductor is referred to as n-type when its conductivity is determined by electrons, and p-type when it is determined by holes.

Figure 2.2 describes the density of states, the Fermi distribution, and the carrier concentration for n-doped, intrinsic and p-doped semiconductors. In the left column, the bold line marks the energy level for the donors or acceptors in the band gap [76, 77, 79].

In n-doped semiconductors, the donor ionization energy level is close to the conduction band. This explains how an electron could be easily given to the conduction band when

the necessary temperature is reached. For the p-doped type of semiconductor, the acceptor energy level is located close to the valence band. The difference of energy between the conduction and the valence band is called the band gap (E_g=E_c-E_v) representing for an intrinsic semiconductor the amount of energy that should be applied to the semiconductor to move an electron from the valence band to the conduction band. For an intrinsic semiconductor, the intrinsic Fermi level is given by $E_F \approx (E_c + E_v)/2$ and is located near the middle of the bandgap. For the n-type or p-type, the Fermi level is shifted toward the conduction band or the valence band respectively [79].

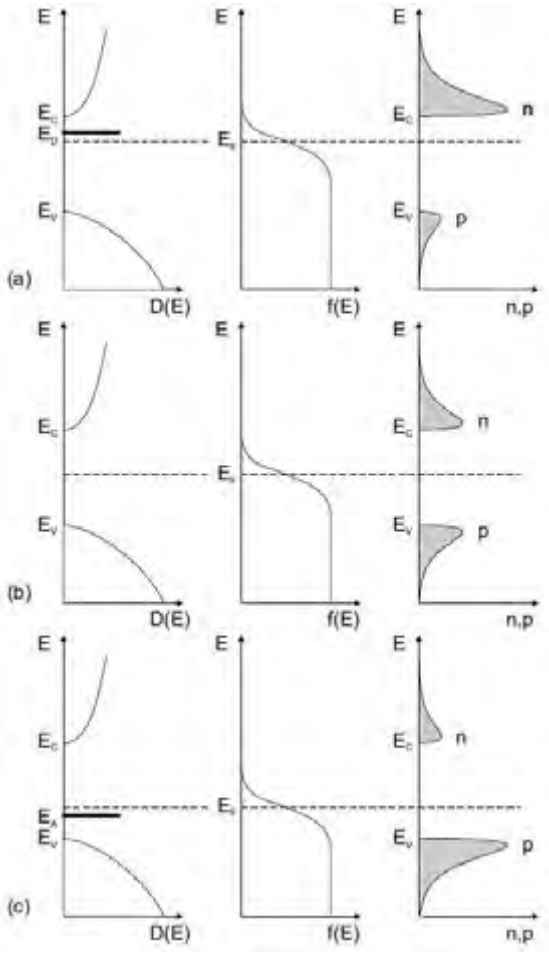


Figure 2.2: *Left column: Density of states D(E); Middle column: Fermi distribution f(E); Right column: Carrier concentration (n,p). (a) n-type semiconductor, (b) intrinsic semiconductor, (c) p-type semiconductor. n and p are the concentrations of electrons and holes in the conduction and valence bands. E_C: Conduction energy level, E_V: Valence energy level, E_F: Fermi energy level, E_D: Energy of donor ionization, E_A: Energy of acceptor ionization[77, 79] .*

Although doping modulates the conductivity of a semiconductor, there is no infinite doping. In this instance, doping is limited by the number of available sites that can host impurity atoms and the proportion of impurities that can be added to a semiconductor before a transition occurs. The transition happens when the electrical conductivity of the semiconductor is in the domain of metal such as 1.0×10^{-8} Ωm, or when the forbidden

gap of figure 2.2 no longer applies. Therefore, a transition occurs when a semiconductor is so highly doped that it ceases to act as a semiconductor, but more like a metal.

2.2 Transistors

In 1925, Lilienfeld filed the first patent application for a field effect transistor[80] in Canada and a year later in the USA. Although this patent was granted in 1930 [80], transistors were first popularized in the 1950s following the works of Bardeen, Brattain and Shockley at Bell Labs in 1948 [81, 82]. Bardeen *et al* introduced a transistor which was initially described to work as an amplifier, and as a replacement for vacuum tubes [83]. Thus transistors quickly became the main components used as electronic switches in the 1960s [84]. Nowadays, billions of transistors are packed into chips, where they largely function as switches in logic gates. From the initial idea of transistors to date, transistors have witnessed tremendous development, prompting significant research attention. However, despite the change in size and method of producing transistors from the 1950s, their mode of operation and architecture has remained largely unchanged. This section provides an outline of various types of transistors, their basic modes of operation, and their methods of fabrication.

2.2.1 Types of transistors

Transistors are generally three or four terminal devices, exhibiting a trans-conductance or trans-resistance. A transistor's major mode of operation is to modulate the current between a pair of electrodes, by applying a current or potential at the third electrode. Transistors are commonly divided into two main classes: junction transistors and field effect transistors.

The point-contact transistor

The year 1948 will always be remembered as the birth year of solid state devices, being the year in which the first working transistor was built at Bell laboratories. In the 1940s, the increased demand of vacuum tubes and triodes for amplification forced scientists and engineers to invest much effort in finding electronics' replacement for vacuum tubes. Using the knowledge of that era's semiconductors, and the prediction of a field effect transistor (FET) by Lilienfeld in 1925 [80], Bardeen, and Brattain ironically discovered the first transistor (point-contact transistor), while mastering their understanding of the potential screen effect at the surface of a semiconductor during their attempts to

produce a working field effect transistor. Their transistor model, architecture, and understanding was improved two months later by William Shockley, to produce the first junction transistor that is widely used as an amplifier today.

Figure 2.3 below, illustrates the schematic of the contact point transistor as presented by Bardeen *et al*; used in this instance to amplify a small AC signal.

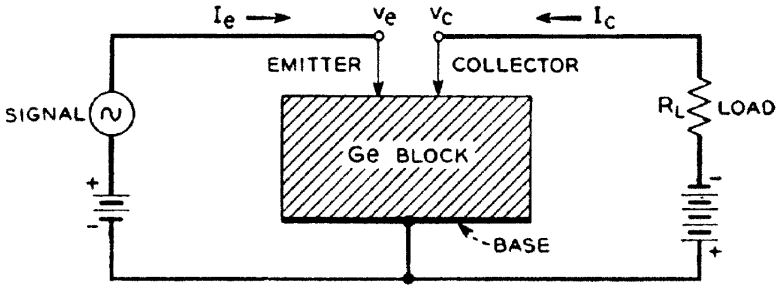


Figure 2.3: *Schematic of the first working transistor (the point contact transitor) [85]. I_E, V_E,I_C,V_C are by convention respectively the emitter current,voltage and collector current and voltage.*

The first point-contact transistor was made of a block of n-type germanium which was known to present a rectifying contact with metal [86, 87], connected to three contacts.

In this experiment, the surfaces of the germanium were cleaned and polished to avoid oxidation. The bottom was connected to a low-resistance conductor and labelled the "Base" (B). Two metallic contact-point electrodes were mounted on the top side of the germanium block, and referred to as the "Emitter" and the "Collector". The distance between the two electrodes was between approximately (0.005-0.025) cm [85]. A transistor is said to be in forward bias when its p or n side are connected to the positive or negative side of a DC current/voltage generator. In reverse bias, the configuration is the opposite of that in forward bias. For the point-contact transistor operation, the emitter is forward-biased and the collector reversed-biased. Bardeen et al demonstrated, the variation of a current/voltage in one terminal, may induce a non-proportional flow of current in other terminals [85–87].

The point-contact transistor was the first solid state device operating on minority carriers; however, it is a noted fact that the charge transport is made by holes flowing from the emitter electrode towards the collector electrode, that is, through the electrode contact point. The rectifying nature of the germanium surface ensures that the hole can freely flow into the n-doped germanium block by the emitter, and is able to flow out through the collector contact point. In contrast, electrons cannot flow or enter the germanium block via the collector point.

The Bipolar junction transistor

If the first irony of the transistor invention was Bardeen and Brattain's discovery of first point-contact transistor years after Lilienfelds' first invention, then one could suggest that a second irony is the fact that William Shockley, the instigator and head of the transistor research group at Bell labs in the late 1940s, was not directly part of the field effect transistor development or the point contact transistor invention [88, 89]. William Shockley was not named as an inventor on either of the first two transistor patents. However, two months later, William Shockley filed a patent application [82] on the theory and operation mechanism of a new type of transistor, subsequently referred to as the bipolar junction transistor (BJT) [90, 91]. Attributing its name to the fact that it operates with both n and p-type materials. The BJT is made up of three layers of alternatively doped materials, so it can also be seen as two n-p or p-n junction arranged back to back. There are two types of BJT: pnp where a very thin layer of n-type material is sandwiched between two layers of p-type material; and npn in which a very thin layer of p-type material is sandwiched between two layers of n-type material. In the pnp transistor, the collector and emitter are p-type and the n-doped material forms the base, whereas in the npn device, the p-type material forms the base. Here it is important to note that, theories governing the operation mechanisms of both pnp and npn are similar, leading to an explanation of one of the transistors as sufficient for both types.

In practice, the BJT is made up of three layers of semiconductors, with alternating types of doping, as shown in the pnp model in figure 2.4. The BJT terminals are labelled as 'Emitter' (E), "Base" (B) and "Collector" (C), as shown in figure 2.4. In the pnp model, the emitter is made of a highly p-doped region, the middle region or base is made of a thin layer of low doped n-material, and the collector is made of a low-doped p- type semiconductor. The base doping level of the emitter is, in general, less than 10:1 [92]. The low doping of the base decreases its conductivity, and therefore increases the resistivity. A contrast of color in figure 2.4 is used to illustrate the level of doping in the P regions. In practice, the thickness of the base layer should not exceed 30 μm.

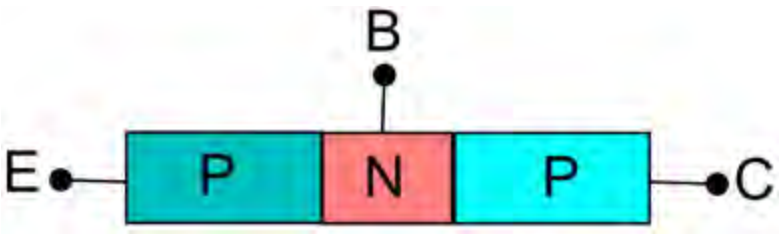


Figure 2.4: *Bipolar Junction Transistor illustration (pnp type) with the electrodes shown as E(Emitter), C(Collector), B (Base).*

Figure 2.5 shows a pnp BJT in equilibrium, with zero-biasing currents on all the terminals. Here it is worth noting that whenever a p-n junction is made, there is a movement of holes and electrons across the junction, as shown in figure 2.5, for both the p-n and n-p junctions. There is a movement of holes from the p-doped semiconductor to the n-doped semiconductor, meanwhile, electrons will diffuse from the n-region to the p-region. The movement continues until the diffusion current is equal to the drift current, thus creating a depletion region. The depletion region, as its name suggests, is depleted of holes and electrons at the two sides of the junction, thus forming a region depleted of free charge carriers. This process creates charged ions in the vicinity of the junction, generating an electric field oriented from the n-region toward the p-region. Once the electric field in the depletion region is established, it is associated with a potential, and will prevent any attempt of diffusion between the two regions. However, the size of the barrier created in the depletion region can be controlled via an external voltage, so that it can be raised up or down.

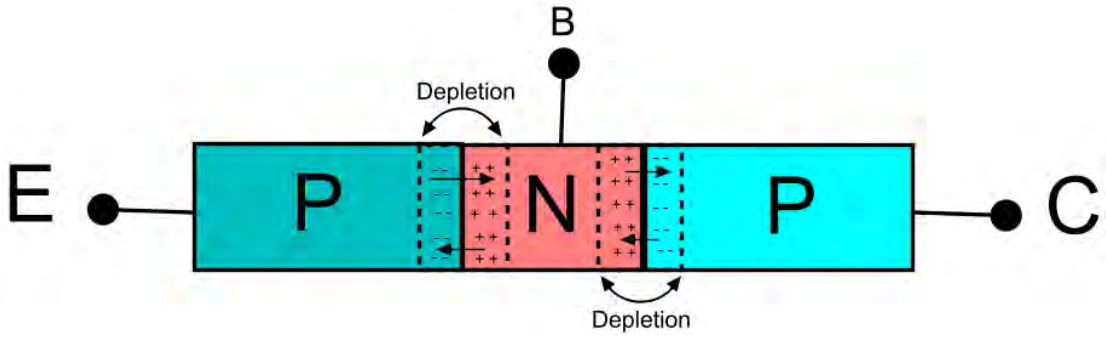


Figure 2.5: *Diffusion of holes and electrons at the vicinity of the interface between N and P regions in and pnp transistor.*

Figure 2.6 shows the BJT in one of its operation configurations. There are four possible ways to connect a BJT. The emitter and collector can be both forward-biased when the battery's positive side is connected to the p-region (pnp) or the negative side is connected to the n-region of the transistor (npn). The emitter and collector can also be both reversed-biased. Furthermore, (E) can be forward and (C) reversed or vice-versa. Precisely for this purpose, the configuration in figure 2.6 is used as a starting point to explain the basic operational mode of the BJT.

When the emitter of a pnp BJT is forward biased, holes are injected into the emitter as seen at the left side of figure 2.6 and in figure 2.7a. Thus the application of a forward voltage creates a potential that shrinks the width of the emitter-base depletion region. When a sufficient voltage is applied to the emitter, holes will diffuse across the p-n junction in large numbers. The electron concentration in the n-region is low, partially from having holes from the creation of the depleted region. Here it is worth noting that all the holes cannot recombine. A few holes will leave the n-region via the base

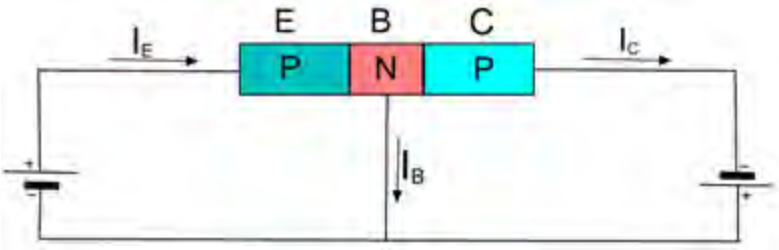


Figure 2.6: *Bipolar Junction Transistor connected to two batteries, the emitter in forward and the collector in reversed bias.*

electrode and return to the other side of the battery. This is in essence, based on the fact that the base region is thin and a high-resistance material, owing to its low level of doping [93]. A significantly large number of holes will diffuse throughout the n-region, but it is important however to observe that, should the emitter be reversed-biased, the barrier height at the emitter-base depleted region would have increased, and thus no holes would have been allowed to diffuse into the base region.

Hypothetically framed, if we were to look at the right side of figure 2.6 as shown in figure 2.7b, the junction between B-C will be reverse-biased, and there will be no current. However it becomes important to note when the emitter is forward-biased, and the collector reversed-biased, that the potential established between the emitter and collector allows the holes from the emitter region to diffuse throughout the base, and ultimately reaching the collector. In this process, small quantities of holes will indeed travel via the base electrode. Let us also note that a small change in the base current is also followed by a significant change in the collector current, giving an amplification process.

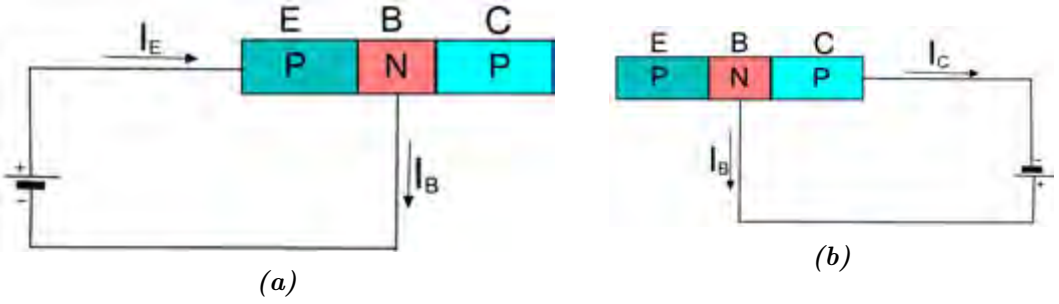


Figure 2.7: *Current flow in a BJT (a) Battery connected between the emitter-base in forward bias (b) battery connected between the base-collector terminals in reversed bias.*

With this illustration, we can summarize the flow of carriers in the BJT with the pnp transistor of figure 2.8, where the direction of red arrows represent the carrier path and their relative thickness represent the quantity. The dark bands show the depletion regions whilst in operation. From the diagram of figure 2.8, one could argue that from this assertion it is evident from the Kirchhoff's law of I_E=I_C+I_B. Here, we can observe that the collector current is made of minority and majority carriers. The minority

current at the collector is called the "leakage current", representing the current that will flow in the collector when the emitter is open.

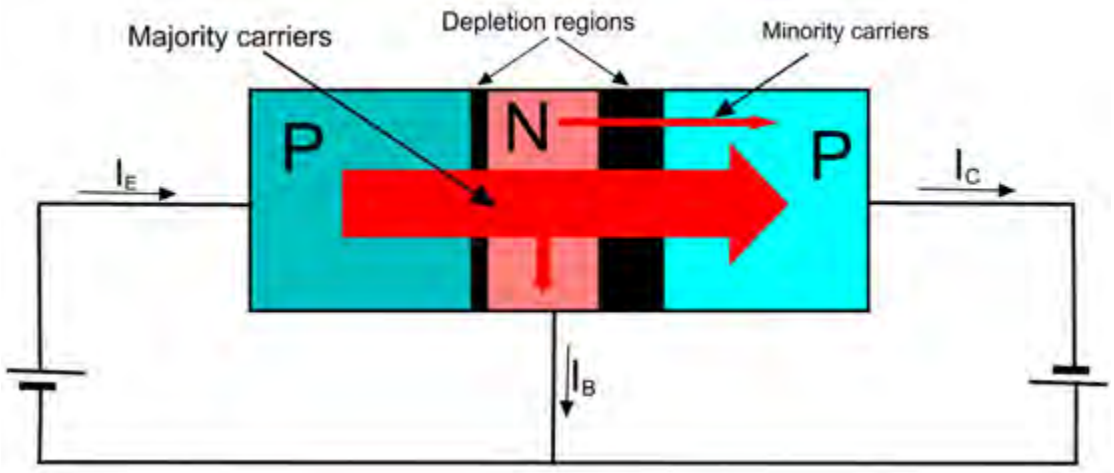


Figure 2.8: *Carriers path in a pnp BJT (after [92]).*

The Field effect transistor (FET)

Since the beginning of intensive research on transistors, there was scientific evidence that the field effect transistor (FET) could be manufactured. However, it took half a century between Lilienfeld's invention [80] and the mass production of FET devices. It thus becomes worth noting that, although the BJT presented earlier and the FET do indeed perform similar functions, each presents a certain advantage for particular applications. Their fundamental difference is the fact that the BJT is current-controlled and the FET is voltage-controlled [94]. The FET is a unipolar device, meaning that the conduction mechanism is based on only one type of carrier (hole or electron). However similarly to pnp and npn BJTs, we can have n-channel FET and p-channel FETs in which electrons and holes are the charge carriers respectively. The first unipolar device was made by Dacey *et al* in 1952 [95], and further research on oxides led to the production of the first FET by Duane Kahng in 1955 [96]. Although not highly reliable at the time, FETs underwent significant improvements in the materials used for their fabrication and their architecture, ultimately being widely used by the 1970's [88]. With the FET having three-terminal device features, where the current flows between a pair of terminals, the FET can be controlled by applying a voltage on the third terminal.

Modern FETs can be classified into various types, including: the junction field effect transistor (JFET)[97, 98], the metal-oxide-semiconductor FET (MOSFET) [99, 100] and the Organic FET (OFET)[101, 102]. FETs and BJTs share several properties and hence carry out similar roles in various applications. However, the fundamental difference between the FET and the BJT is that the BJT is a current driven device, where the

current between two terminals is controlled by the current on the third terminal - unlike the FET, which is voltage-controlled. Although playing the same role in circuits, FETs do not all share the same operating mechanism. Therefore the conduction mechanisms of two of the most common FETs: the JFET and the MOSFET will be presented.

The conduction mechanisms for an n-channel FET is similar to that in the p-channel FET. Therefore, without loss of generality, only one channel type will be presented in the following discussion.

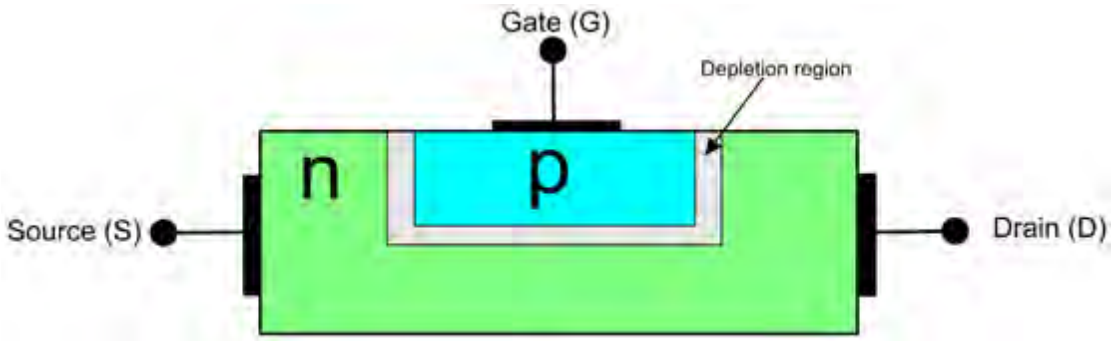


Figure 2.9: *Schematic of an n-channel Junction Field Effect Transistor (JFET) with the three electrodes labelled as Gate (G), Source (S), Drain (D).*

Figure 2.9 shows an n-channel JFET made of a wide channel of low doped n-type material and a heavily doped p-type material. One could observe that at zero bias voltage there is a depletion layer (shaded in grey), created in the vicinity of the junction of the p-region and the n-region. Due to the high level of p-doping, the depletion layer is formed almost completely on the side of the n-material [103]. The two sides of the channel, are denoted as 'Source' (S), and 'Drain' (D) respectively. The third electrode connected to the p-region is, in this case, called 'the Gate' (G); with the name possibly suggesting the gate electrode that will serve to control the flow of charge between the drain and the source [104, 105]. One can observe that the JFET operation mechanism is based on the control of majority carriers between the source and the drain in a channel modulated by an electrostatic field created by the potential at the adjacent terminal.

In figure 2.10, the gate potential is at zero and a potential difference V_1 is established between the source (S) and the drain (D). The potential V_1 generates a flow of majority carriers (electrons), from the source to the drain, with the electron path shown in the figure by the arrows.

Due to the distribution of the potential in the channel with higher voltages toward the drain terminal, the electric field created in the depletion region is not uniform. Therefore, the depletion region (shaded in grey) is wider toward the drain electrode.

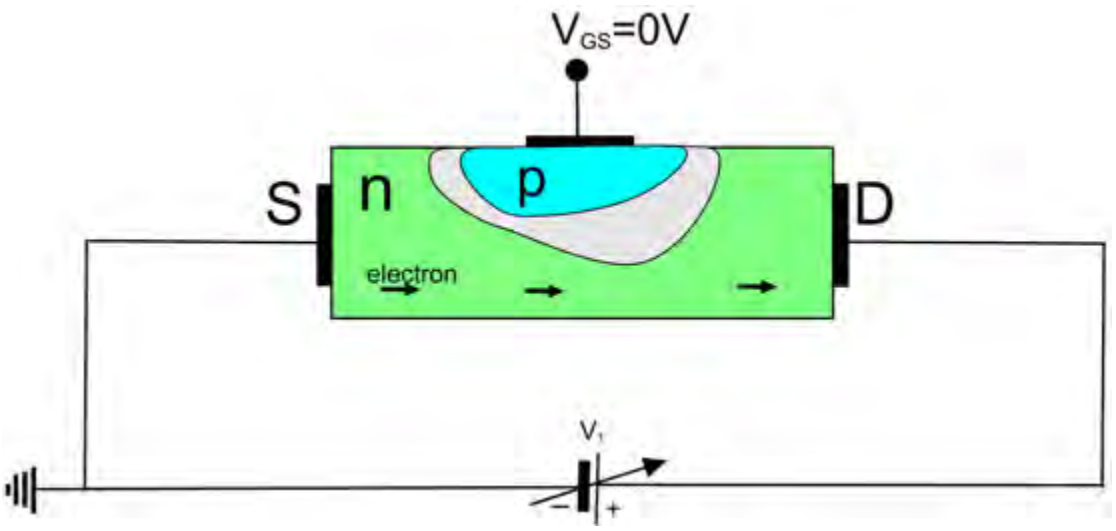


Figure 2.10: *Carrier path in a pnp BJT, when a voltage V_1 is established between the Source and the Drain.*

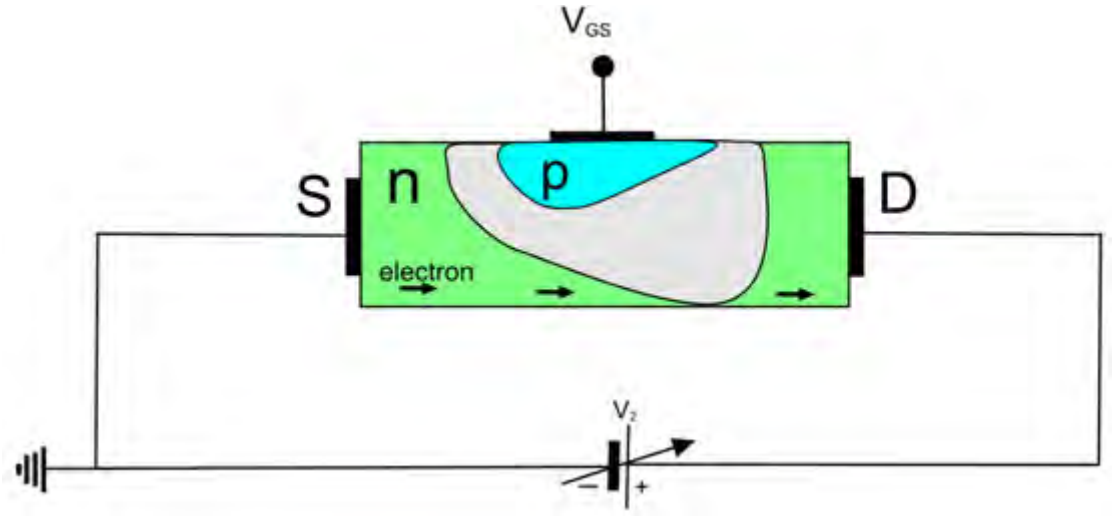


Figure 2.11: *Carrier path in a pnp BJT.*

If the gate voltage is kept at zero, $V_G = 0\ V$, and the source-drain voltage V_{DS} is increased to a potential $V_2 > V_1$, (figure 2.11) the form of the depletion layer will change further. From small voltages, the inflation of the depletion region does not change noticeably, either the channel width nor the resistivity. For higher values of V_2 the depletion region is much wider, reducing considerably the channel width as shown in figure 2.11. One should note that, when the source voltage is considerably high, the resistivity of the channel increases rapidly until it reaches a constant value when the depletion region extends across the whole width of the channel. This culminates in a constant drain current. This condition is referred to as the 'pinch-off' or a saturation region [104].

To illustrate this concept in figure 2.11, while keeping V_{DS}, we applied voltage to the

gate, where holes will leave the highly doped p-region. Here, the size of the depletion region will increase more quickly, and the saturation region will be reached sooner, compared to the case when there is no bias-voltage. In other words, should the gate voltage continuously decrease, we will ultimately arrive at a state where the drain saturation current is zero, with no current flowing into the drain. The device is in the off state.

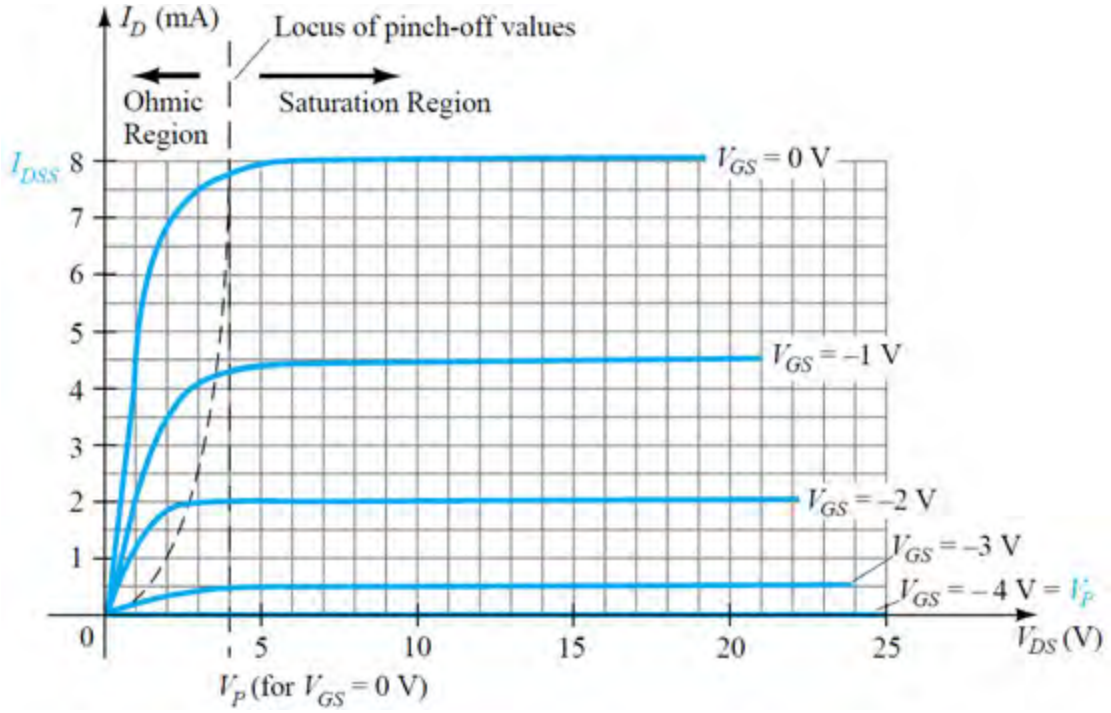


Figure 2.12: *Current-Voltage transfer characteristics of an n-channel JFET (after[92]).*

Exploring this concept even further, using a set of current-voltage characteristics, as shown in figure 2.12, one observes voltages corresponding to the same n-channel JFET representing the drain dependent current, given as a function of V_{DS} for various gate bias voltages ranging from 0 to -4 V. In this figure, one sees that the saturation current value of the n-channel JFET decreases, as the magnitude of the negative bias current applied to the gate increases. Here the pinch-off voltage (V_P) when the saturation current is 0, as shown in the graph by the curve at $V_{GS} = -4V$ is referred to as the "turn off voltage".

The other main category of FET is the MOSFET, differing from the JFETs generally by the fact that control of the flow of electron in the channel is made by the gate, which is insulated from the rest of the structure by an oxide or dielectric layer.

There are two main types of MOSFET: firstly, depletion-type when there is a channel between the drain and the gate terminal, as shown in figure 2.13; and secondly, enhancement-types indicating that there is no channel between the source and the drain. Figure 2.13 shows a depletion-type n-channel MOSFET, which is a transistor made up

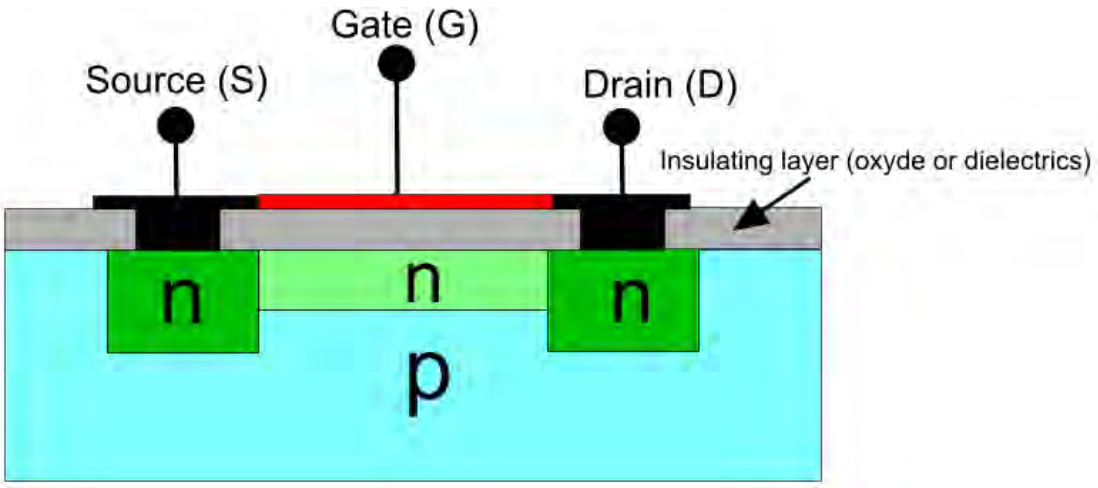
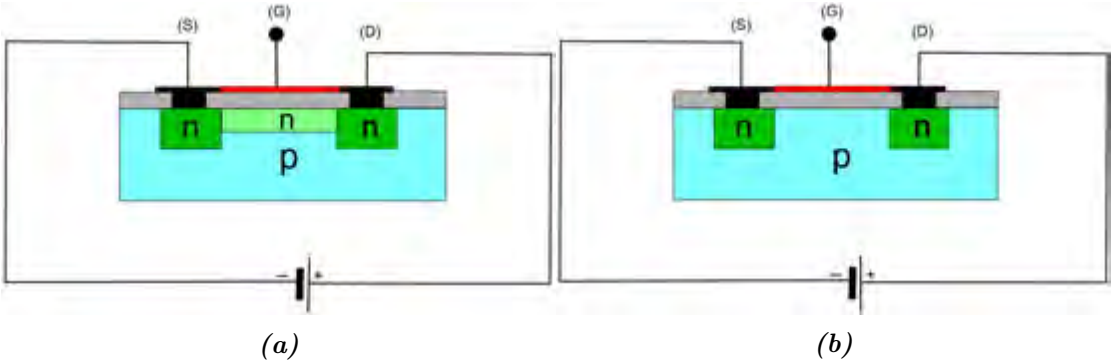


Figure 2.13: *Depletion-type n-channel metal-oxide-semiconductor field effect transistor (MOSFET).*

of a p-substrate material, a low doped n-channel connected to two heavily doped drain and source regions. An insulator isolates the gate electrode from the n-channel.



(a) ***(b)***

Figure 2.14: *MOSFETs connected to external voltages. (a) Depletion-type n-channel MOSFET (b)Enhancement-type n-channel MOSFET.*

When a voltage is established between the drain and the source of a depletion-type n-channel MOSFET, as shown in figure 2.14a, at zero gate voltage, electrons will flow from the source to the drain. Therefore, one can observe that $I_S = I_D$. However, if the voltage applied to the gate is negative, the electrons in the channel are repelled to the p-region where they recombine, thus causing a reduction in conductivity in the channel. Similarly, if the negative voltage is made more negative, a certain value of V_G, we will reach the pinch-off region current saturation as described earlier.

The enhancement-type n-channel MOSFET in figure 2.14b operates in a slightly different manner from the depletion-type. The main difference between the two transistors is that the enhancement-type does not have a channel, therefore when a voltage is established between the source and the drain at zero gate voltage, there is no current between the drain and the source. When a positive voltage is established on the gate in figure 2.14b,

holes are repelled under the insulating layer. If the gate voltage is increasingly positive, more holes will be repelled near the insulator, with electrons accumulating near the insulating layer. As the number of electrons increases at the vicinity of the insulator for a high enough voltage referred to as"threshold voltage". The n-channel will be formed, and current will start flowing between the source and the drain.

2.3 Electronic switches

Switching is one of the most common operations in engineering and science. A switch is generally defined as a device that is able to turn a signal ON and OFF and connect or disconnect two or many elements of a circuit or a system. Switches can be classified as momentary or maintained. In general, there are two categories of switches: mechanical and electronic switches. Mechanical switches are made of moving parts and can be turned ON/OFF manually. Electronic switches, in contrast, are made of non-moving parts and are generally solid-state devices or assemblies of solid-state devices. Switches are also classified into momentary and maintained switches, with the maintained being a switch that remains in a particular state when actuated. Maintained switches are mainly used for low-speed switching, mechanical and non-automated switching, whereas the momentary switches, act as switching when actuated by an input signal or a preset condition, these includes diode, transistor, relay, actuators and most solid state switching devices.

Mechanical and electro-mechanical switches are no longer appropriate for high speed and remote switching. Therefore, they are not used in fast-switching electronics and computers, due to their low-switching speed as well as the difficulty of integrating them into a complex network [105]. Nowadays, there are countless numbers of switches, so only a few basic and most popular switches are presented in the following discussion.

Diodes

A diode is the simplest electronic component used for switching. It is generally made of a $p-n$ semiconducting junction or a metal-semiconductor Schottky junction [106–108]. The mechanical equivalent of a diode is a single pole single throw switch, as it switches in only one direction and can only be ON or OFF.

To pass the current in one direction, a diode uses the existence of a depletion layer at the $p-n$ junction. Figure 2.15 illustrates how the current-voltage transfers characteristics of an ideal diode, as well as showing its mode of operation as a switch. For an applied

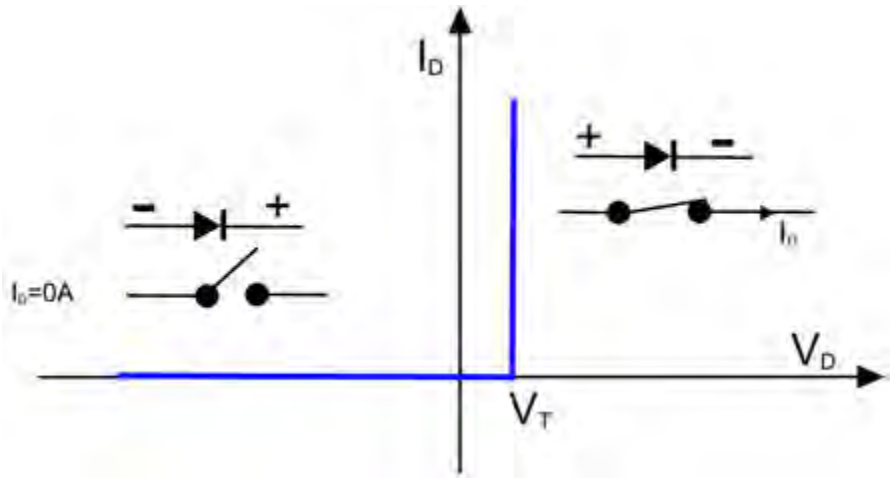


Figure 2.15: *Ideal diode working as a switch.*

voltage V_D, when the diode is connected in reverse bias like in the left side of figure 2.15, the depletion layer at the junction of the $p-n$ diode will increase in size, therefore increasing the resistance of the diode to (ideally) infinite. Due to the high resistance, no current will flow through the diode ($I_D = 0\ V$), and the diode behaves like an open switch. When the diode voltage V_D is connected in forward bias (right side of figure 2.15), as soon as the voltage applied to the diode is greater than the threshold voltage V_T, the diode resistance goes to zero, thus a current flows through the diode and the only limitation will be the external circuit.

Transistors

The uses of transistors in switching circuits are constantly increasing with their main fields of application nowadays in computers, telecommunications, television, displays, RFIDs, instrumentation, power electronics, control and automation systems [109–111]. Each set of applications requires a different type of transistor. The most widely used transistors in switching circuits are the MOSFETs and the bipolar transistor presented earlier. In general, MOSFETs are used in low voltage and high-frequency applications, because of their unipolarity and their fast-switching response. For high voltage applications, where speed is not a priority, bipolar transistors are preferred due to the small conduction losses as the voltage increases.

The current-voltage characteristics shown in figure 2.16 illustrated the dependence of the drain current on the drain voltage, for a given gate voltage, in a depletion mode MOSFET. While working in a switching circuit, transistors are used in the saturation region - where the current is constant and can be controlled by the gate/base. In the above figure, the current between the drain at the source is (5 mA) at zero gate voltage,

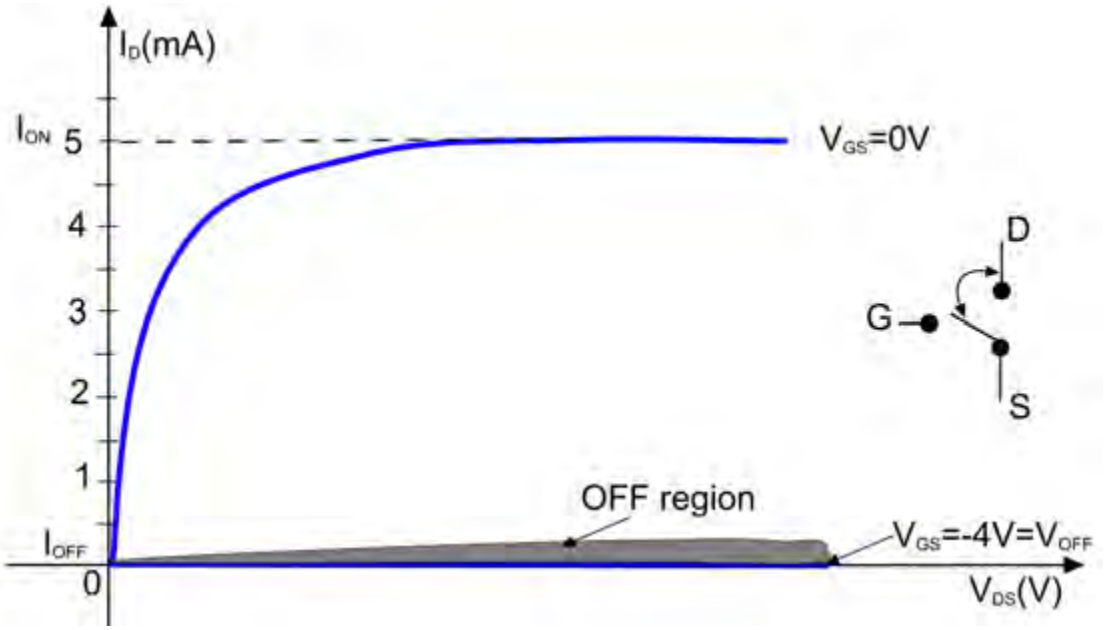


Figure 2.16: *Current-voltage transfer characteristic of a MOSFET working as a switch.*

corresponding to an ON state, where the current will be refered to as I_{ON}. When an appropriate voltage is applied to the gate, with the transistor channel resistance high enough for the current not to flow, the transistor is referred to as being OFF, the current between the source-drain is zero or a small leakage current. A switching transistor is often represented by a switch controlled by a gate/base terminal [103]. The right side of figure 2.16, shows an illustration of such switches.

The parameters of a switch are given by its I_{ON}/I_{OFF} ratio and its switching time. I_{ON}/I_{OFF} is the ratio of the highest current in the device, to the smallest current in the device. This ratio is effective as an indicator for the potential applications where the device can be used. In general, nano-applications are only able to handle very small current, and require high I_{ON}/I_{OFF} [112].

The switching time of a device is evaluated by studying the output waveform of a square wave input signal. Figure 2.17 illustrates the typical output current waveform at the collector of a BJT, mounted in common emitter configuration, and with the base connected to a square signal. We can observe from the top figure that, when a voltage V_2 is connected to the transistor, the device is 'OFF' as shown in the bottom part of figure 2.17, and $I_B \approx I_C \approx 0$. At t_1 the input voltage quickly rises to V_1, and the transistor is now forward bias, however, we can see that the output current will progressively rise to saturation. Traditionally, the device is considered to be completely 'OFF' when the collector current is less than 10% of the collector saturation current I_{Cs}, the time taken by the device to rise from zero to $0.1I_{Cs}$ will be the delay time t_d as shown in the figure.

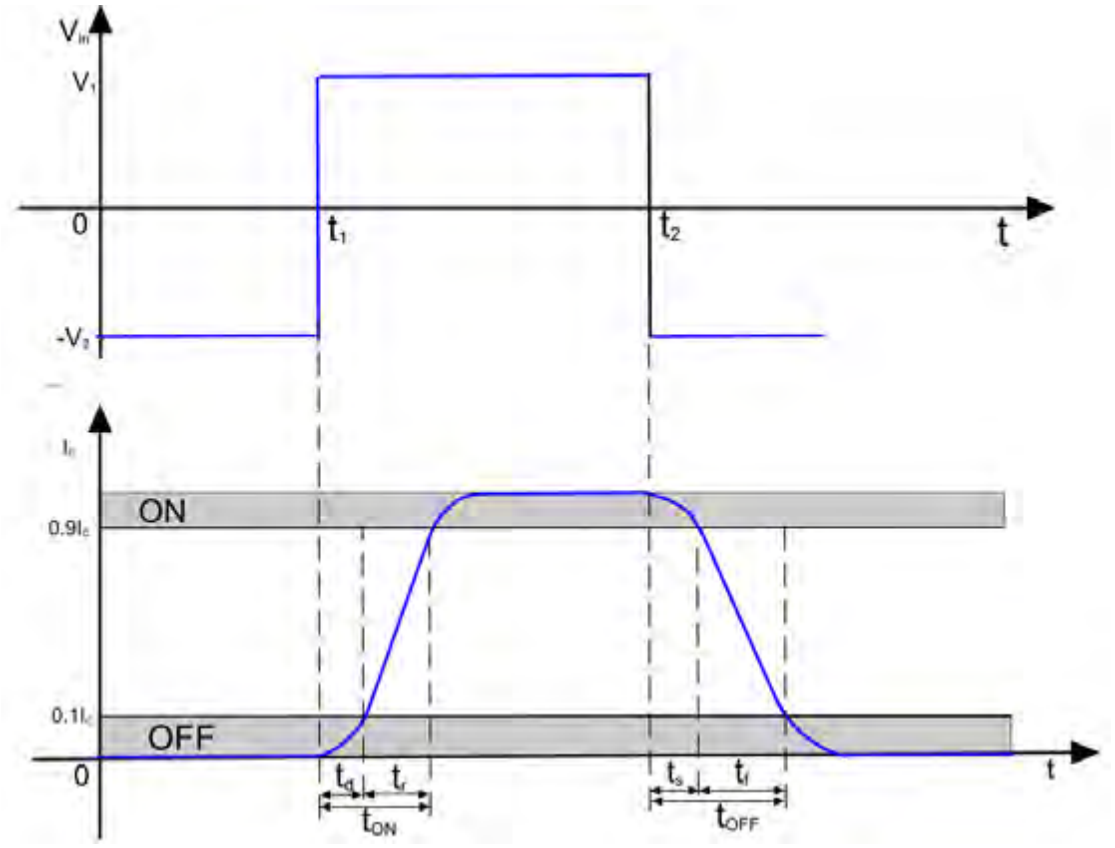


Figure 2.17: *Input (top) and output (bottom) waveforms of a current respectively at the base and the collector of a BJT.*

From the delay time, the current will rise faster to reach 90% of their saturation value. This time is called the "rise time" t_r. Once the saturation current is attained for the applied input voltage, the current will remain constant and the device is "ON".

When the voltage is reverse biased again at time t_2, due to the charge stored in the device, the current does not instantly decrease. The time lapsed for the collector saturation current to drop to 90% is called the 'storage time' t_s, and the time lapsed when current falls from $0.9\mathrm{I}_{Cs}$ to $0.1\mathrm{I}_{Cs}$ is referred to as the 'fall time' t_f. The ON and OFF times are respectively defined as $t_{ON} = t_d + t_r$ and $t_{OFF} = t_s + t_f$. The total switching time, defined as $t_{total} = t_{ON} + t_{OFF}$, is a pivotal switching parameter as it defines the maximum number of switching operations that can be performed with the device during a specific time. To achieve theoretical success at switching at any given frequency, the total switching time should be less than half of the period $t_{total} < Period/2$, where the period is defined as the time lapse between two consecutive wave crests to pass the same fix point. In other words, the shorter the total time, the higher the frequency that can be used on the device. Several other types of switches are used in electronics, but they generally originate from a diode or transistor, through the addition of more layers in

their structure or tuning the doping to the desired application. Other electronic switches include triacs, dynistors, thyristors, and silicon controlled rectifiers.

2.4 Transistor production

The number of electronic switches and applications integrating switching devices have been increasing since they were first introduced [113]. The fast improvement and the diversification of methods to produce transistors are driven by the deep understanding of transistor theory. Obviously, the advancement of transistor fabrication has always been related to that of the semiconductor production, doping control, novel materials, and novel methods of semiconductor fabrication.

The first transistor [83, 86] was built manually in 1947, from n-doped germanium, connected to two electrodes [83, 86]. The following year, the BJT was produced by chemical diffusion of different types and levels of dopant, in the same piece of intrinsic semiconductor [89–91] chemical diffusion was the standard of transistor production until the early 1960s, when Jean Hoerni introduced the planar process [114, 115].

The planar process is still the standard in semiconductor industry today, using a simple process of masking some part of a wafer or substrate, where a device or circuit is going to be built and using various lithographic processes to produce several devices or circuits at once. The planar process is used in the production of a wide range of circuits, including Integrated Circuit (IC), microprocessors, RAM, and SRAM. The planar process has become quite dominant in the industry, owing to its high reproducibility rate, reliability and the ease of producing identical circuits. The following section succinctly describes the main methods of device fabrication.

Lithography

Lithography is the most widely used method of producing transistors and ICs. The production of silicon transistors by this method commences with oxidizing a silicon wafer surface at high temperature ($600° - 1500°C$), thereby protecting the silicon from contamination [116, 117]. Then, the oxide layer is covered by a thin layer of ultraviolet (UV) light sensitive material, and spun at high speed in order to obtain a uniformly thin layer called a photoresist [118]. The next step is the selective removal of certain areas of the photoresist in a process called photolithography. In practice, the photomask blocks UV on its opaque areas and exposes other areas. Depending on the nature of the photoresist, a negative or positive photoresist can be created using UV-photolithography,

wet photolithography or electron lithography [103]. After these steps, the patterns obtained from lithography are transferred to a film by either dry or wet etching [119–121]. The final fabrication steps usually involve selectively doping certain areas of the device by ion implantation, gas-source doping or solid-source diffusion [103]. Lithography is a highly reliable process, which has contributed significantly to transistor size reduction as well as the development of mass production.

Nowadays up to four billion transistors can be found in a single chip. Although very reliable, lithography is quite an expensive process and is usually more complex than described above. At any given time more than ten lithographic steps are performed with different masks to produce a single device. Hence there is a constant need to search for alternatives or complementary methods to lithography.

Flexible electronics

Flexible electronics is the production of devices or circuits on flexible substrates such as paper, plastic or metal foil [122, 123]. Since the 1980s, there has been a significant increase in interest regarding flexible technology driven by the sheer size of possibilities that flexible technology offers [124, 125]. In addition, any thin material possesses a high tendency to bend. In the recent decade, tremendous progress has been made on flexible electronics, particularly on the fabrication of wearable technology and flexible displays.

The development of flexible technology obviously drives the development of flexible transistors and switches. The trend in conventional electronics is to reduce the number of transistor per mm^2 and produce much more complex and miniaturized devices. Whereas, in flexible technology, the trend is to be able to produce large-size devices such as extremely large displays. Hence the production mechanism of a transistor includes the methods cited above, thin film deposition, printing, and other chemical processes. In printing electronics, transistors are produced by successive deposition of electronics inks (conductors, semiconductors, dielectrics) in a defined pattern to produce the desired transistors. The size of the devices to be patterned using printing technique are limited upward only by the size of the printer to be used, in fact, it is possible to print a device of very big size should the printer be available for such design. It is understood that with printing technique the size and the dimension of any known substrate used in printing media can be used to produced electronic devices. However, in the other size of the scale the smaller size of the devices that can be printed is very limited compared to devices produced by planar processes. In screen printing, for instance, the smaller size of the devices is defined amongst other parameters by the smallest gap that can be printed

between two conducting line without getting a short circuit, the smallest reliable gap between two conducting line during this work was 200 μm.

2.5 Paper substrate

In electronics, the substrate use for the production of a device is as much important as the active material used and the architecture of the device itself . The performance of electronic devices is strongly related to the type of substrate used for their production. With the planar process, devices such as transistors, diodes, ICs, microchips are built in doped substrates, and their substrate is entirely integrated into their design.

During the past 3 decades, there has been a surge in flexible electronics research [37, 126–129] . For instance, in recent years the development and production of various devices on flexible substrates have been reported These include transistors [48, 129], logic circuits [37, 130], diodes [29, 38], solar panel [131, 132] , MEMS [133, 134], sensors [135, 136] , batteries [137], RFID [138] . The development of flexible electronics is linked to the development of flexible substrate . Several types of flexible substrates are being used for the production of electronic and bio-medical devices. The much widely use category of flexible substrates are Poyethylene terapthalate (PET), plastics, rubber, and paper [37, 139]. Each substrate provides advantages and disadvantages, but the structure of much flexible substrate can be modified to meet specified electrical, mechanical or chemical characteristics favorable to produce electronic devices. Amongst the above-mentioned substrate, paper is the cheapest and the environmental friendly substrate.

Paper has been around for more than thousand years and has primarily been used for writing and mass media production. In the last 20 years, the need for flexible, low-cost, light weight coupled with the development of semiconducting, polymeric, and composite inks prompted a new interest in the use of paper as electronic substrate.

For this work, the paper was principally used as substrates. A paper made of cellulose fiber principally obtained from wood was used in this work. Common characteristics to define the type of a paper is their mass per unit area, which is referred to as grammage. Light paper or tissues are in the range between 10- 70 g/m^2, whereas the paper commonly used in office ranged from 70-120 g/m^2, beyond this value paper, are referred to as thick paper or cardboard. Paper is often coated or tuned to modify their parameters such as conductivity, permeability, porosity and flexibility [140–142]. These techniques are important for certain types of applications However, it also increases the price/grammage of the paper. In this thesis, the paper used did not undergo any treatment. The plain papers 80 g/m^2 and 170 g/m^2 were used, whereas, the devices produced on each

paper did not present any significant difference since the surface of these substrates are supposed to be electrically and chemically inactive. Figure 2.18 , shows the transversal view of 80 g/m^2 plain paper

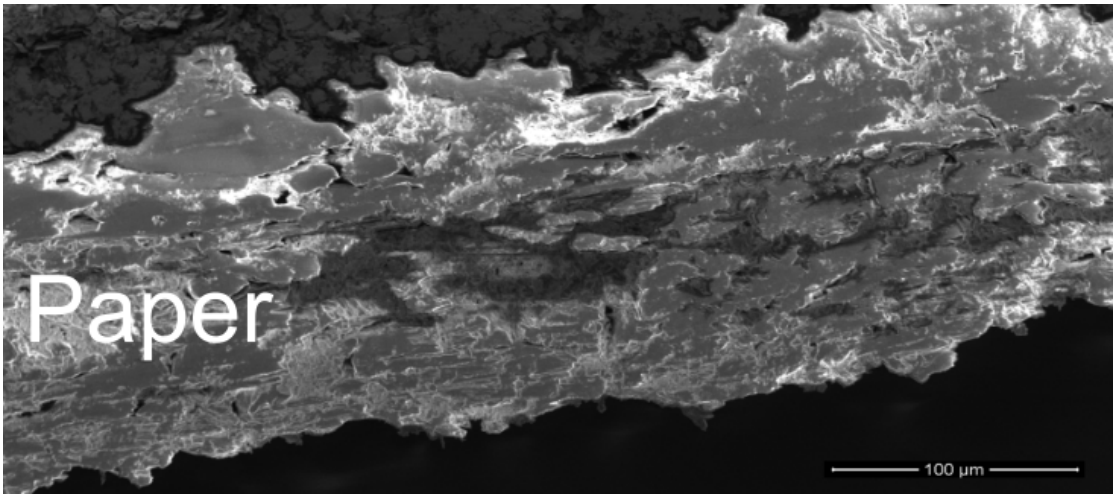


Figure 2.18: *Transversal view of a paper with grammage 80 g/m^2 made of wooden fibre observed under SEM.*

The electrical properties of cellulose-based paper substrates is a laborious field of study and is not yet fully understood due to factor such as the influence of relative humidity (RH) of the paper [139]. Simula *et al* reported a volume and surface resistivity for the paper substrates at the RH 20-40% to typically be $10^1$0-10^{14} Ωcm and 10^{11}-10^{15} Ωsq^{-1} [143]. At room temperature with a RH of (50±5)% we measured the resistance of a 250 μm segment made of printed silver, p-doped printed silicon and cellulose paper. We recorded values of approximately 3 Ω for silver, 2 MΩ for printed silver, No reading was recorded on the paper using a Uni-T digital multimeter which has the capability to read up to 10^{10} Ω This shows that the substrate used for the study is highly insulating and would likely not contribute to the overall conductivity of the devices. Furthermore, a study of the magneto-conductivity of these substrates at low temperature showed that the substrate does not contribute to the overall conductivity of the devices produced on paper at low-temperature [**?**]. Hence, it will be considered for this study that the substrate does not contribute to the electrical performance of the devices.

Chapter 3

Devices architecture, design and production

This chapter introduces a novel type of a printed transistor which presents a unique property of two-way switching, focusing on the architecture, production and operation of the current switching transistor (CST) as follows: 3.1 will address the properties of the CST in relation to other transistors, subsequently presenting all the CST used during this study. Section 3.2 will discuss the CST's key parameters. Section 3.3 will detail the current switching transistor architecture. Section 3.4 describes the experimental set up and characterization used for the device's production and characterization. Sections 3.6 and 3.7 will describe the general techniques and equipment used for the electrical characterization of this thesis at room and variable temperature. The chapter's last section focuses on and discusses the results obtained with an interdigitated CST when the channel width is varied.

3.1 Background of current switching transistor (CST)

We introduce here a current-driven switch with an operation mechanism based on activated charge transport. In preliminary results, the current switching transistor (CST)[48, 144], was presented as a transistor with the ability to switch current between terminals. Conventional transistors in switching mode rely either on modulation of current flowing through the emitter by the carriers injected into the base in the case of bipolar transistors or on the control of charge going between the drain and the source using an electric field generated from the voltage applied onto the gate terminal for FETs. Similarly, to these conventional transistors, the current between each pair of CST terminals can be controlled by a voltage applied to the third terminal. But unlike

most conventional transistors, the CST relies on activated charged transport, which is the dominant transport mechanisms of a network of silicon particles [24, 30, 31].

Nowadays in circuits and applications, the main role of transistors is to switch. Figures 3.1a and 3.1b, represent a BJT and FET respectively. These transistors, although different in their architecture, mode of operation, and switching mechanism, share in common the fact that they can switch in only one way since the doping level is modulated in their structure. The BJT relies both on minority and majority carriers to operate, and its switching mechanism is based on the diffusion of electrons from the n to the p-region and holes from the P to the N-region for a pnp transistor. Hence the variation of current/voltage in the base (B) allows the regulation of the current between the emitter (E) and the collector (C). In the FET, while in operation the current is from the source (S) to the Drain (D), the current can be modulated by the field created by a voltage applied to the gate (G). Thus during the switching with a FET, the current between the source and the drain is controlled. For both the BJT and the FET the current can be switched ON or OFF between two terminals, and a mechanical analogue representing both their switching mechanism is presented in figure 3.1c. The blue arrows in 3.1c shows that the base or gate can be used to regulate the current between the emitter-collector or drain-source terminals.

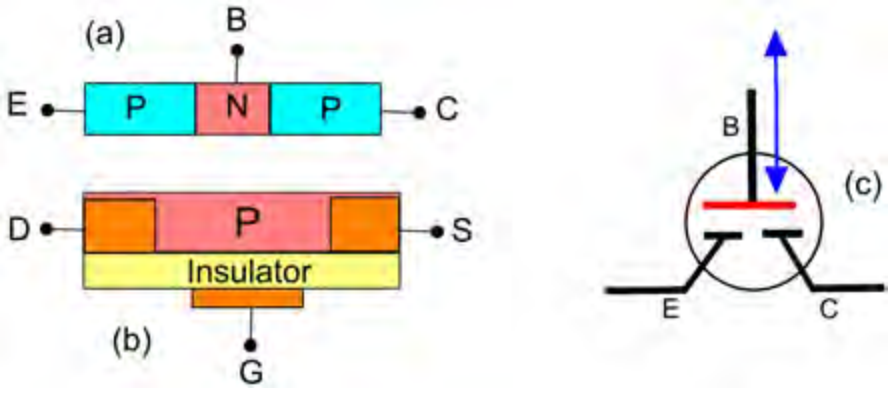


Figure 3.1: *(a) Illustration of a PNP type bipolar junction transistor (BJT), with its terminals represented by Emitter (E) Collector (C), Base (B). (b) Schematic of a field effect transistor (FET), with its terminals represented by the gate (G), source (S), drain (D). (c) mechanical analogue of BJT and FET switch, where the blue arrow shows the possibility of using the Base/Gate to modify the current flow between the other pair of terminals.*

We previously showed that the CST could be modeled by an equivalent circuit made of three varistors [48, 49] as shown in figure 3.2a. Figure 3.2a, shows a triangle with each side occupied by a varistor, in this case, the varistors of type SIOV-S14K75 manufactured by TDK EPCOS, were used. The triangle of varistors operates in such a way that the current between one terminal and any one of two other terminals is routed in such a manner that: when a positive current is present at the first terminal, there is a negligible

current through a second terminal at which a positive potential is applied and a positive current out of the third terminal which is held at a negative potential with respect to the second terminal; and when there is a negative current, outwards of the first terminal, there is a positive current into the second terminal and negligible current through the third terminal[37, 48, 144].

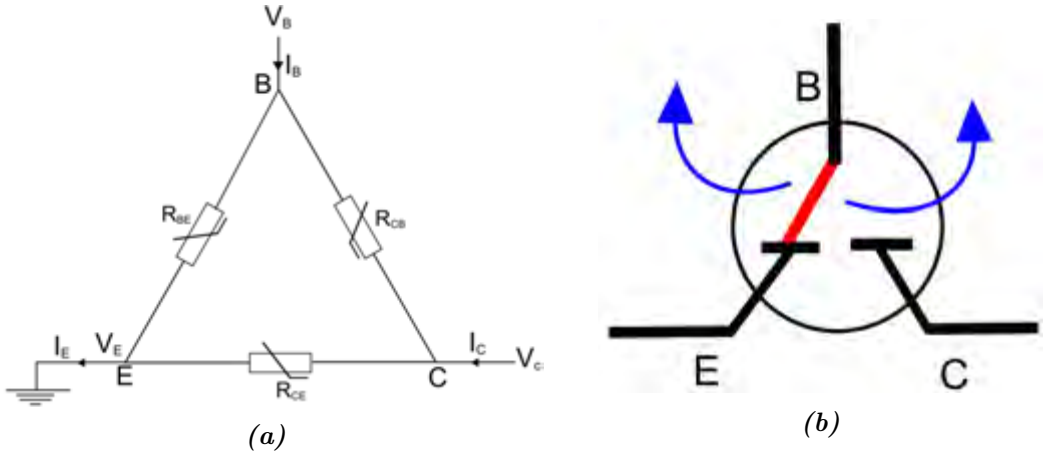


Figure 3.2: *(a) Schematic representation of the CST model using a triangle of varistors, the emitter voltage is grounded. (b) Mechanical analogue of the CST. The arrows show that the CST switching mechanism can be operated in both way unlike the conventional transistor that can only be switched in one way*

Unlike most conventional transistors, the current path in the CST depends only on the sign and magnitude of the voltage at its terminals. For instance, when the collector voltage is positive, and the emitter connected to the ground, the current will be between the base and the collector for a positive potential on the base. When the collector voltage is negative, the current will flow between the base and the emitter instead. Therefore there is no current in the collector, meaning that the device off. The schematic in figure 3.2b shows the mechanical analogue model of the CST. It acts like a single-pole double throw switch, where the two arrows in figure 3.2b represent the fact that the current path can be changed between terminals.

The transfer characteristics of the triangle of varistors model are shown in figure 3.3. These transfer characteristics were recorded in current sweep mode with a semiconductor parameter analyzer (Keithley 4200 SCS), with the collector biased, and the emitter terminal grounded. Figure 3.3, shows the dependence of collector current on the base voltage and current for various collector bias voltages under ambient conditions. Figure 3.3a shows near perfect switching behavior since the collector current is completely zero as soon as the base current becomes positive. The IV transfer characteristics in figure 3.3b show the evolution of switching voltage as the bias voltage on a terminal, here the collector, increases. This shows that the switching persists as long as the bias voltage is greater than the switching threshold.

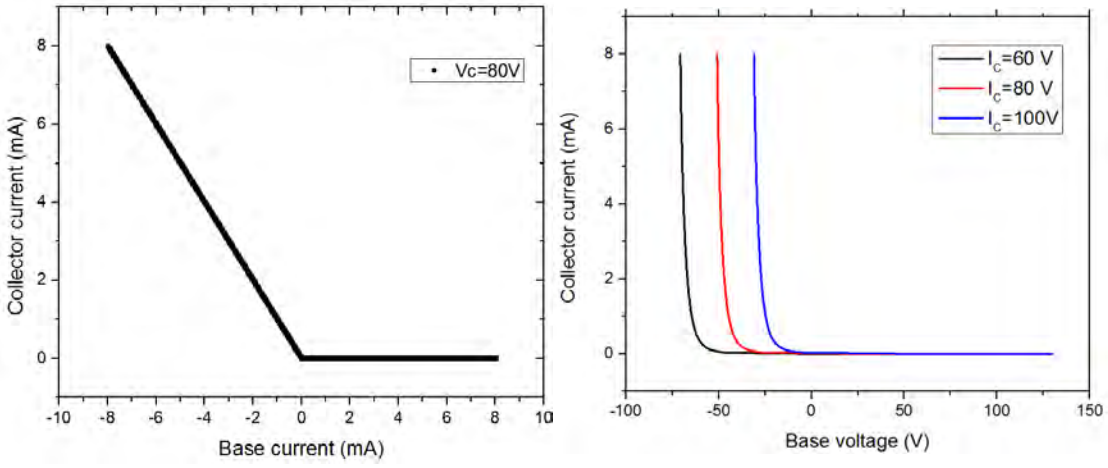


Figure 3.3: *Transfer characteristics of a triangle of varistors (SIOV-S14K75). (a) Current-current transfer characteristics, the collector voltage was biased at 80 V. (b) Current-voltage transfer characteristics for the collector biased at 60 V, 80 V, 100 V.*

We have also shown in previous work that one important aspect of the CSTs was the fact that it can be fabricated using various approaches. In fact, the CST could be broadly made by building a three terminal device, using any combination of materials displaying a varistor-like behavior between each pair of terminals. The varistor characteristics could arise from the rectifying junctions between the semiconductor material and the contacts or from the interfaces at the junction of a particulate or grained material. Thus, besides the schematic of 3.2a, built with discrete varistors, several architectures of CSTs were produced with the active material being nanostructured silicon presenting varistor-like behaviors [24, 29–31, 48, 49], as will be presented later.

3.2 Transistor key parameters

The characteristics of CSTs studied in this work were influenced by differences in architecture. The parameters presented here are those that were important to the design or investigated during our study.

- **The diode ideality factor η:** Is a factor intrinsic to a semiconductor junction, describing how close the junction is to the perfect junction with a step function potential barrier. At the junction, the current density consisting of thermionic emission and tunneling is given by : $J = J_0[\exp(qV/\eta k_B T) - 1]$ [145], where J_0 is the saturation current density representing the current density of the majority carriers moving in reverse direction at zero voltage [146], and the Boltzmann factor $\exp(qV/\eta k_B T)$ is a probabilistic term representing the proportion of charges with

sufficient energy to cross the energy barrier, also known as activation energy[147, 148]. For an ideal diode $\eta = 1$ [149], this number can be higher than 2, depending on the type of material or junction used [150] In material made at a microscopic level of grains or domains this number can reach many hundred [48, 151] . The ideality factor can also be seen as an average number of successive barriers over which the potential V is applied in a complex system, such that the potential difference over each barrier is greater that the Boltzmann factor.

- **The transistor channel Length (L):** The length of the conducting path in the semiconductor between each pair of consecutive electrodes. Generally, for the CST, there are three independent channel lengths which may or not be equal corresponding to the varistors R_{BE}, R_{CB}, R_{CE} in figure 3.2a.
- **The transistor channel Width (W):** The width of the conducting path in the transistor.
- **The collector bias voltage V_C:** This is the constant voltage applied to the collector terminal during the characterization. The collector voltage is very important in this study, as the switching of the CST is influenced by the value of V_C.

3.3 Current Switching Transistor architecture

In device physics and printed electronics, device architectures are very important as their variation directly influences the device response to quantities such as electric current, light, and temperature [152–155]. Thus concept, design, and architecture were of extreme importance in the present work. Architectures of CST used in this study are presented here, as they differ by the configuration of their electrodes and the channel of the active layer. The devices could be divided into two main categories: symmetric and asymmetric. Each model will be presented with characteristic dimensions.

Figure 3.4, is the architecture of the CST presented earlier [48, 49]. It is an asymmetric transistor named for the study as type "J". The left-hand side of the figure shows an overview of the transistor with the electrodes labelled the Base (B), collector (C), emitter (E) in analogy to the conventional notation for a bipolar or point contact transistor. The base is in the form of two sharp points connected by a common conductor. The electrodes are in the same plane, with the collector electrode being the mirror image of the emitter from a central axis through the two tips of the base. The right-hand side of 3.4, shows the magnification of the area under the active layer of semiconductor. Transistors with various architectures and different electrode shapes were developed.

However, the behavior of a transistor was only defined by the size of the silicon connecting electrodes. Thus the dimension of the silicon is the main CST characteristics that will be mentioned for all the CSTs presented throughout this work. For the CST presented in figure 3.4 the dimension of the active silicon is given by the letters f, g with $2g$=0.4 mm, these dimensions correspond to channel lengths of $L_{CE} \approx 0.4$ mm and $L_{CB} = L_{BE} \approx 0.2$ mm. We should note that the smallest reliable gap between two electrodes printed during this work was 0.2 mm.

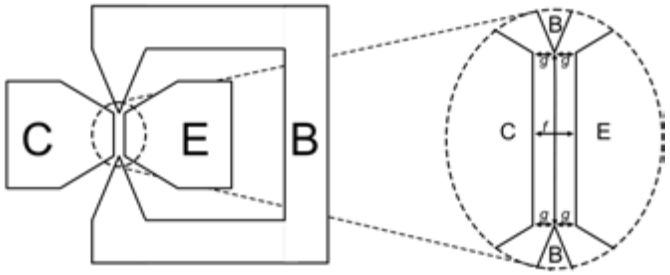


Figure 3.4: *(left) An asymmetric CST architecture, electrodes are labelled as Emitter (E), Collector (C)and Base (B), the dotted ellipsoid shape represents the area covered by silicon. (Right) is the magnified view of the area of the electrodes below the active layer of silicon. e,f,g indicate the characteristic dimensions of these CST adapted from [49].*

Figure 3.5 is the design of a symmetric model of CST referred to as type JT. The left-hand side shows the design of the device, made of three identical base (B), collector (C), emitter (E) electrodes. These electrodes are lines of width l, with minimum separation m. The central axes of the electrodes are separated from each other by an angle of 120° and are all located in the same plane. The active layer of silicon in this structure is represented by the triangle at the centre of the structure delimited by the dotted line. The right-hand side of figure 3.5 is a magnification of the central area cover by the silicon. For this model, four types of transistors with different patterns were made. Besides the shape presented here, another model was obtained by rotating the triangular shape here by 180°, and two more were obtained by replacing the triangle by circles of radius respectively 3.0 mm and 4.5 mm. Figure 3.6, shows the illustration of the characteristic dimensions for the CST JT device. In this architecture, the channel length and width are equal and given by $L = W = \frac{l}{2} + m$, for this study the channel length and width were taken to be 0.8 mm.

Figure 3.7 is another symmetric design of CST investigated in this study. The left side of the figure shows the completed transistor formed by its electrodes and the silicon layer. The Emitter (E), Collector (C) and Base (B) electrodes are arranged as interdigitated arcs of concentric circles, each spanning 240°. The right-hand side of the figure shows a magnified view of the area of the electrode below the semiconducting silicon. The aim of using interdigitated fingers was to reduce the electrical resistance of the silicon track, by

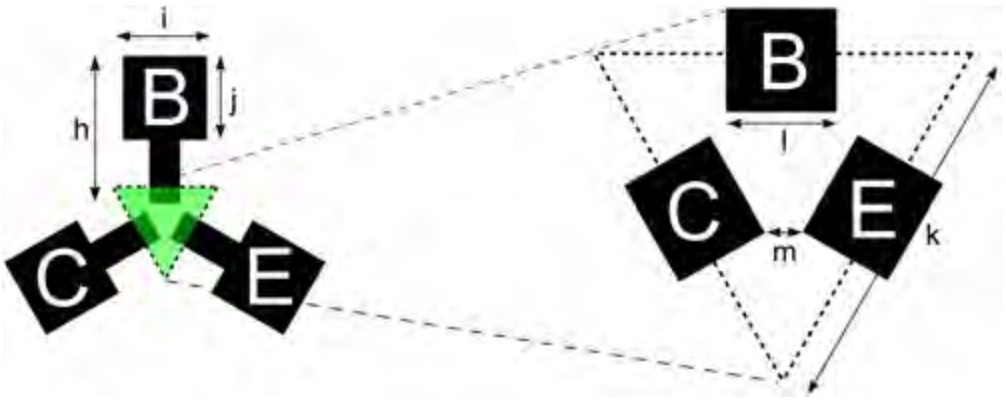


Figure 3.5: *(left) A symmetric model of CST (CST JT), electrodes are labelled as Emitter (E), Collector (C)and Base (B), the green triangle with the dotted contour is the shape and the coverage of the active layer of silicon. (Right) Is the magnified view of the area of the electrodes right below the active layer of silicon. l,m are characteristic dimensions of the silicon track inside the transistor.*

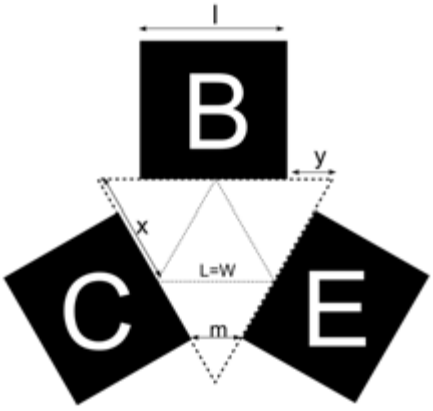


Figure 3.6: *Schematic diagram illustrating the CST JT width and length. From simple geometric calculation we derive that for this CST architecture the channel length (L) and width (W) are equal and can be written as $L = W = \frac{l}{2} + m$ where l is the line width and m the contact pad. In the case of this study the dimensions were taken to be l =1.2 mm and m =0.2 mm therefore $L = W$ =0.8 mm.*

increasing the width of the channel while maintaining a short length. The outer dotted circle is the size of the silicon layer. The structure was named CST W for this study, indicating that the silicon channel width of this model was varied during the study.

The total width (W) of the active layer was calculated as:

$$
\begin{aligned}
W_1 &\approx 2\pi r_{min} \\
W_2 &\approx 2\pi(r_{min} + 2L) \\
W_3 &\approx 2\pi(r_{min} + 4L) \\
W_4 &\approx 2\pi(r_{min} + 6L) \\
&\vdots \approx \vdots \\
W_n &\approx 2\pi(r_{min} + 2(n-1)L) \\
W = \sum_{n=1}^{n-1} W_n &\approx 2\pi n\Big[r_{min} + (n-1)L\Big], \qquad (3.1)
\end{aligned}
$$

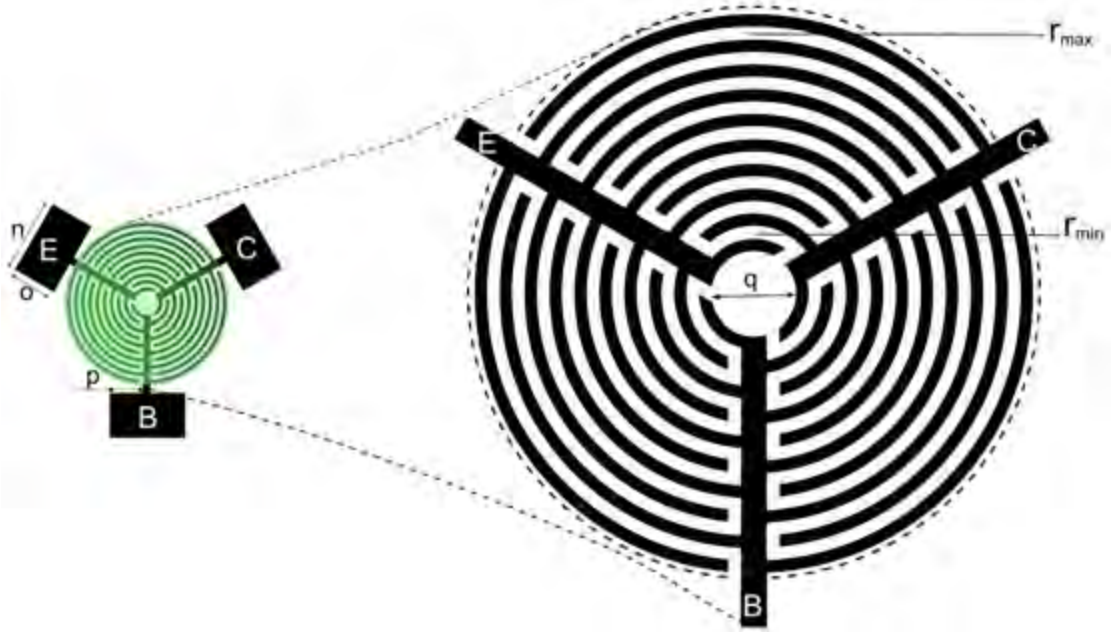


Figure 3.7: *(left) A symmetric model of CST (CST W), electrodes are labelled as Emitter (E), Collector (C)and Base (B), the green circle with the dotted contour is the shape and the coverage of the active layer of silicon. (Right) Is the magnified view of the interdigitated electrodes under the silicon layer. The letter q indicates the diameter of the inner silicon disk.*

with r_{min} taken to be the radius of the smallest arc of silicon, n the number of circular silicon track of the same length to the centre of the transistor. For this study, the transistor lengths were L =0.5 mm This length was approximately the smallest gap that could be printed with a circular design without getting the arcs short-circuited. Smaller, gap was tried but the success rate of the devices produced with such gap was very low. r_{min} =4 mm, this value was chosen both from the smallest gap that could be printed with this design and the necessity to have distinct silicon track. q =3.2 mm and the number of circular silicon tracks n were respectively 9;14 and 19. This translate into channel widths of: $W_1 \approx$ 452.16 mm, $W_2 \approx$ 923.16 mm and $W_3 \approx$ 1551.16 mm. We started with the device W_1, the idea was to increase the width of the silicon track by a similar factor, so we chose the width of W_2 to be the double of W_1 and the width of W_3 to be three times the width of W_1.

Figure 3.8 is also an asymmetric model of CST. The left side of the figure shows the complete transistor, where one sees the dimensions of silicon track on the right. For this study, the channel length of this transistor was taken as $L_{CE} = L_{BC} = L_{BE}$ =0.3 mm. The smallest dimension between two conducting electrodes that could be printed with CST architecture made of rectangles or triangles was around 0.2 mm, the dimensions of this design were chosen to be close to that value.

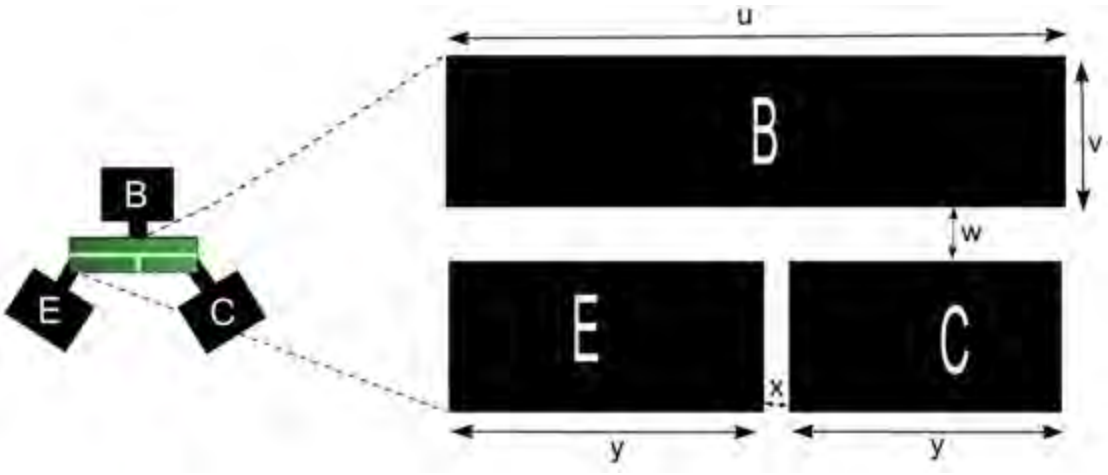


Figure 3.8: *(left) a model of asymmetric CST (CST JE), Emitter (E), Collector (C)and Base (B) electrode can be seen. the green coverage is the shape and position of the active layer of silicon. (Right) is the magnified view of the electrodes under the silicon layer. The letter u,v,w,x, and y indicate the dimensions characteristics of the CST.*

3.4 Experimental method and preliminary results

3.4.1 Silicon powder production and ink formulation

The main approaches for nanoparticle production are classified as top-down and bottom-up methods. The most commonly used bottom-up methods include solid-phase deposition (SPC), chemical vapor deposition (CVD), aerosol synthesis, liquid phase method, self-assembly and positional method [31, 156] which allow the formation of nanosized structures including nanoparticles by assembly atoms and molecules. It is interesting to mention that bottom-up methods produce very defined, regular and fine particles or clusters, but the cost of production is often too high for industrial scales. Top-down approaches consist of size reduction of bulk material into nano-sized structures, which can be achieved by mechanical, chemical reaction, and lithographic techniques, or just occur naturally [156]. In contrast to bottom-up methods, milling particularly provides an easily scalable production process for nanoparticles with a more irregular shape. For this work, the top-down approach was used to produce nanostructured material by high-energy milling, a method of mechanical attrition used to produce nanoparticles [156, 157].

High energy milling

High energy milling results in the mechanical breakdown of a solid into smaller particles without changing its state or composition [158]. It uses a mixture of grained material

as a feedstock to produce nanostructured material by continued impact and shear force. For this research, nanostructured silicon aggregates composed of nanoparticles were produced by high energy mechanical milling using a vibratory disc mill. The mill used consists of four sets of 52100 chrome steel pestles and mortars, with each mortar having a lid fitted with rubber O-rings to ensure its airtightness. The four vessels are mounted on a base that vibrates in two axes to cause a lateral and rotational movement of the pestles as illustrated in figure 3.9. By means of this combined movement, the material in the mortar is ground by impact and friction, and homogenized at the same time [157, 159]. This leads to a progressive reduction in the size of the particles. By the size of the particles, we will refer to the approximate diameter of a particle along their longest axe.

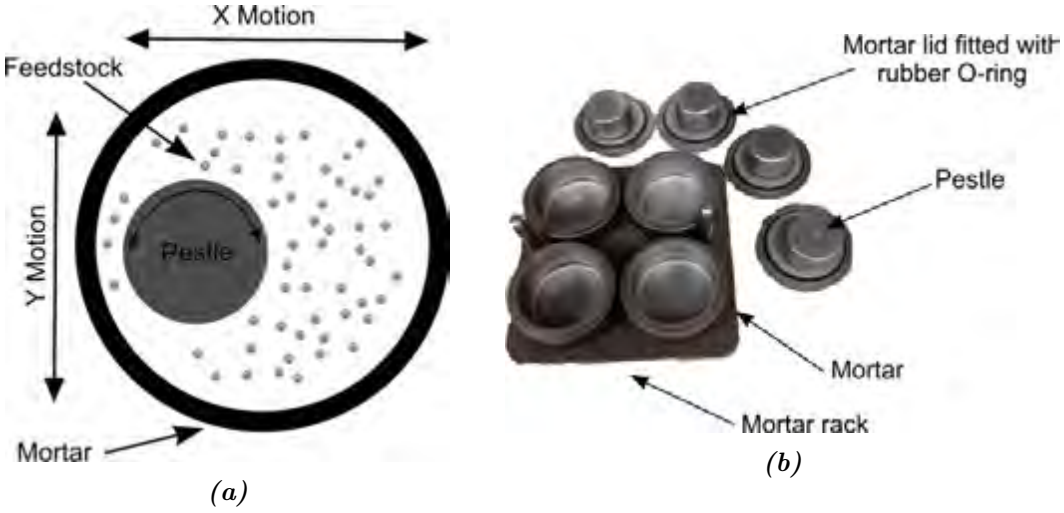


Figure 3.9: *(a) Mechanism illustrating the movement of the pestle inside the mortar during the milling operation. The double headed arrows indicate the different movements of the pestle (Adapted from [157, 160]). (b)Aset of four pots with their pestle and lid fitted with rubber O-ring.*

The milling set of figure 3.9b is made of four pots, and each pot is an open cylinder with an inner diameter of 8 cm and a depth of 3.7 cm. The pestle is a cylinder of 5.5 cm diameter, 3.3 cm height, and 0.6 kg in mass. Prior to milling, pots and pestles were cleaned using quartz, by milling it successively twice for periods of 10 minutes to prevent cross-contamination, as recommended by the Centre for Minerals Processing, and then cleaned with compressed air and then wet-cleaned with acetone and ethanol. After cleaning, the feedstock of 27 g of silicon was loaded in each pot. The feedstock load represented to the pot volume a ratio of approximately of 1:10. The volume ratio is critical, as the pestle mobility during milling depends on this ratio. The pestles and the pots always move in opposite directions for a maximum impact and produce nanoparticles by comminution, or consecutive reduction under severe plastic deformation [157, 158, 161]. During milling, the particle size cannot decrease indefinitely, and the

smallest average particle sizes with silicon were achieved at five hours effective milling time. Beyond this time, particles started clustering and the average size of the aggregates increased. So, the regime of 5 hours of effective milling time was used during this work.

For this study, different types of bulk silicon were used as feedstock. Firstly p-type and n-type single crystalline prime grade doped silicon wafers from (Siegert Wafer GmbH, Aachen, Germany) were used. The silicon wafers were doped with boron and arsenic respectively and had an initial resistivity of $\rho < 0.005\ \Omega$ m . Similarly, doped p and n-type ingots from the same vendor were also used. The p-type silicon ingot doped with boron had a nominal resistivity of $\rho < 0.001\ \Omega$m , whereas the n-type silicon doped with phosphorous, has a nominal resistivity of $\rho = 0.001 - 0.00102\ \Omega$ m . A 99.9 % pure 2503 metallurgical grade silicon purchased from Silicon Smelters, Polokwane, South Africa was also used.

3.4.2 Ink rheology and stability

The inks used throughout this study were water-based, as previous work showed that such ink retains their main functionality such as conductivity, capacitance, after being printed and cured [162]. A thinner was used to meet the ink printability ink viscosity requirements of screen printing which are 0.5- 505 Pa.s [163]. Table 3.1 illustrates the general ink viscosity requirements associated with various printing methods.

Printing method	**Ink viscosity (Pa.s)**
Screen printing	$0.5 - 505$
Gravure method	$0.01 - 0.2$
Flexography	$0.05 - 0.5$
Offset lithography	$5 - 100$
Inkjet printing	$0.001 - 0.04$

Table 3.1: *Printing method with corresponding ink viscosity requirement. Adapted from [164]*

The rheology was further checked by determining the contact angle, which is the angle between a horizontal surface and the tangent to the surface of the droplets. The surface energy of the ink can be calculated exactly if the surface energy of the surface is known. The general mesh count of the screen used for this study required the contact angle of the composite ink to be around $(50 \pm 5)^\circ$ for proper printability, this was in agreement with previous studies made by Batsirai[24]. For lower values of the contact angle, the ink was too fluid and yield a poor edge definition of the printed structure and a non-uniform printed surface. For higher value, the inks were too thick and would not flow through

the screen. Thus, the typical contact angles from the left and right side of the ink drop of semiconductor were in the range $(50 \pm 5)^\circ$ on a glass surface.

The inks were produced by mixing a chosen type of silicon powder (p-type, n-type, metallurgical grade) with a water-based acrylic binder from Marchem, Cape Town, South Africa. Prior to the production of the ink, glassware and instruments were cleaned twice with acetone and ethanol and properly dried to avoid any residue or contaminant. Then, the silicon powder and the binder were mixed in a ratio of 80:20 by weight. The binder was kept in a glass bowl, and silicon powder was added successively in small quantities and steadily mixed manually. Propylene glycol (propan-1,2-diol) from Sigma Aldrich, Germany, was added later to act as a thinner. The thinner allows the rheological printing requirements to be met. Previous studies have shown that after curing the thinner completely evaporates and the binder is reduced to less than 10% of its initial mass concentration [24].

3.4.3 Morphology and internal structure of Silicon

A small amount of the milled powder produced from 2503 grade silicon feedstock was used to check the microstructure of the powder using Transmission Electron Microscopy (TEM). Prior to the measurement, the silicon powder was put in methanol then sonicated for 10 seconds to break up large agglomerates. Immediately after sonication a small amount of methanol powder mixture was pipetted onto a holey carbon grid. A JEOL-Jem 2100 transmission electron microscope was used at 200 kV. The micrographs of nanostructured silicon shown in figure 3.10, showed similar features to other TEM studies on similar material [165], where a detailed discussion of the silicon powder is given summarizing the results at low magnification. Figure 3.10a and 3.10b showed the the two regions on the grid of the nanostructured systems at the same magnification. We can see that the two figures (3.10a, 3.10b)show nanostructured silicon aggregates. These structures were consistently observed at different positions in the grid, and thus we could say that the silicon used in this study was made of clusters of various sizes that also formed clusters of clusters. The structures are clusters of silicon particles, and can be seen in micrographs figures 3.10d and 3.10c. Figure 3.10d is the area enclosed by a red square on figure 3.10c. This area is made of clusters, and the area enclosed by the red ellipse is a typical region where clusters overlap. Overlapping regions and contact between the particles are very important because they enable charge transport in the nanoparticulate network. The majorities of crystallographic planes were oriented along $< 111 >$ and $< 100 >$ [30, 38] direction [166].

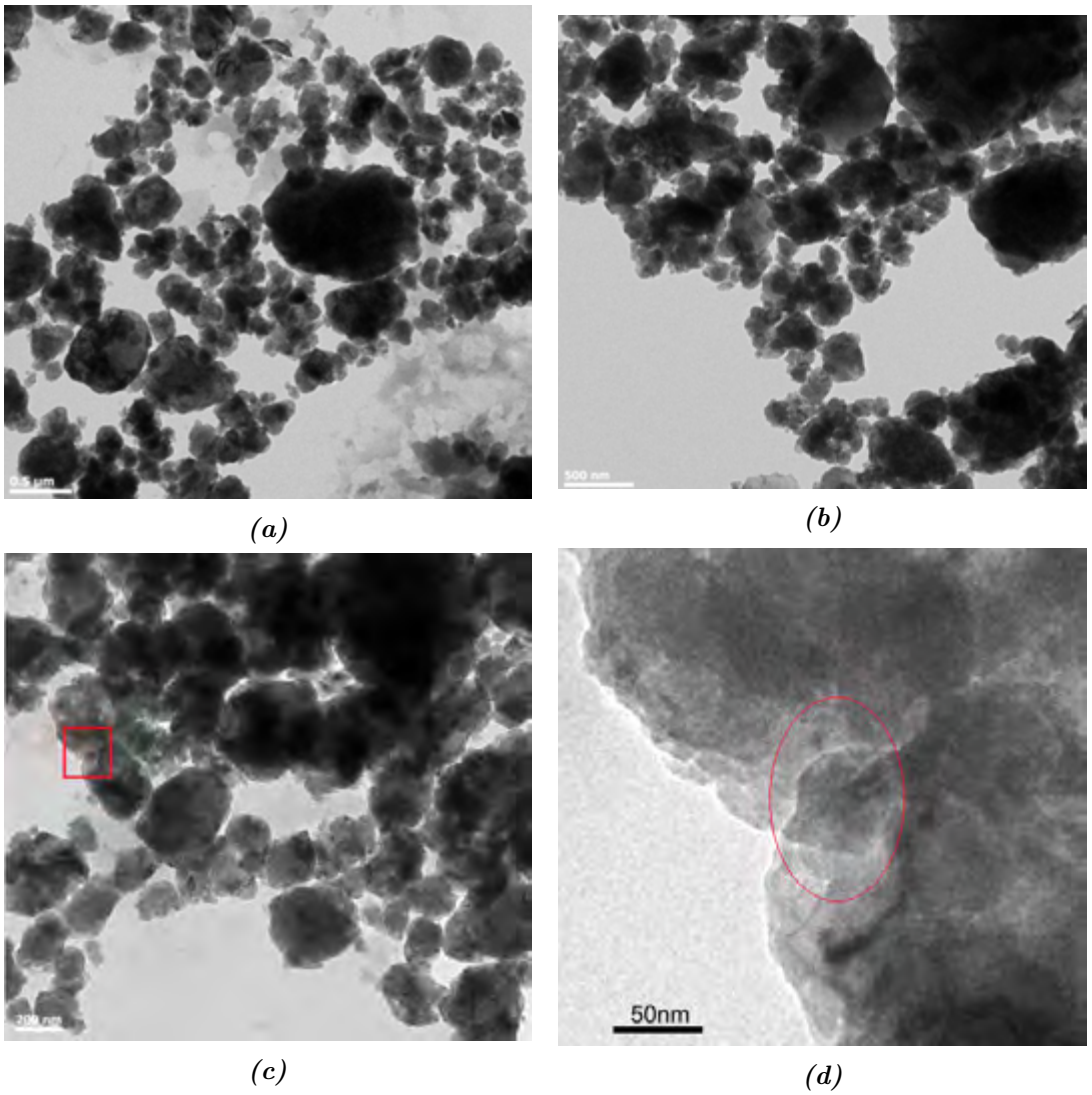


Figure 3.10: *TEM images of 5 hours milled metallurgic silicon grade 2503 at different magnification. From low magnification (a) to high magnification (d). The red ellipse show the region were two clusters overlapped.*

3.4.4 Screen printing deposition

Screen printing is one of the oldest printing methods which allows the deposition of ink in a precise manner on a substrate. The most important parts of a screen printing equipment are: screen with the design, the ink to be deposited, a movable squeegee that is used to force the ink through the screen, and the substrate onto which the design will be patterned [167]. For this study, an ATMA-60PD digital electric flat bed screen printer was used for printing, including both the printing of silicon layers forming the semiconducting part of the devices and the silver layer forming the contacts. The printer used for this work is presented in figure 3.11.

The screen printer is a semi-automatic printer equipped with a high precision pneumatic

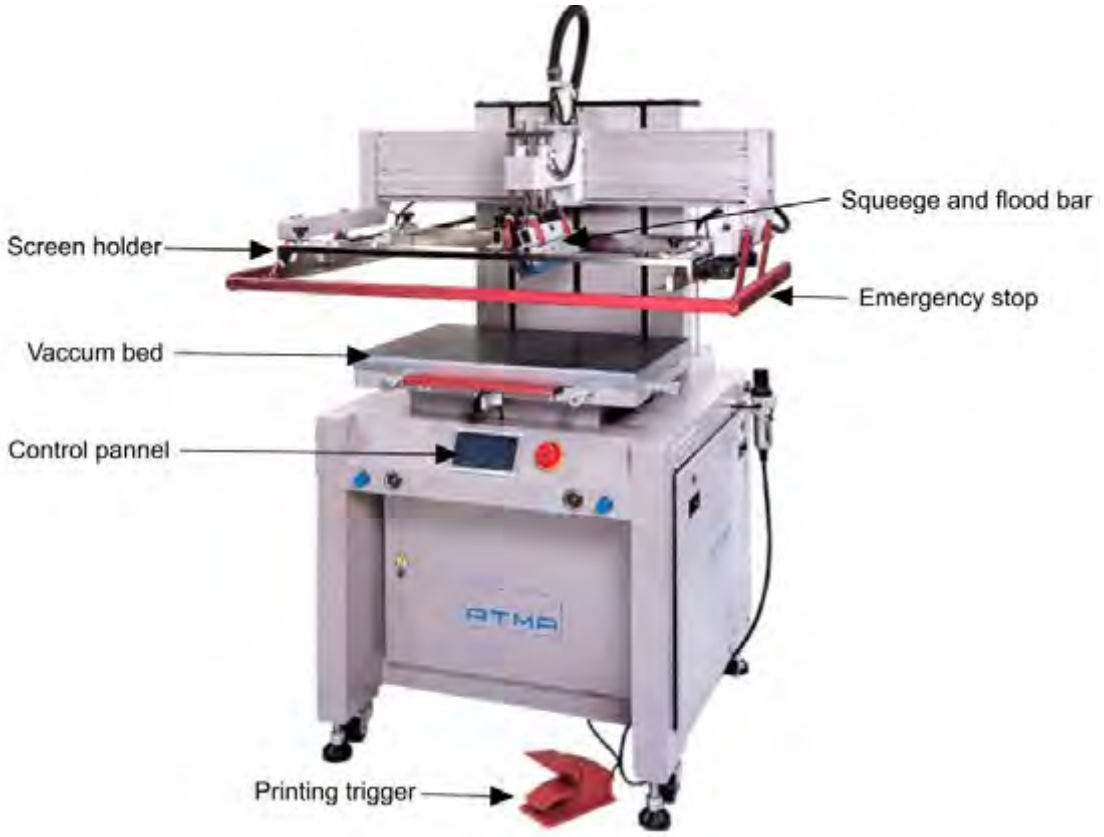


Figure 3.11: *ATMA-60PD Digital Electric Flat Screen printer.*

system. This system serves to keep the substrate on the vacuum bed during registration and printing. It also controls the motion of the squeegee, flood bar, and screen during the operation.

More than 30 screens were used during this study, all made of woven Sefar monofilament polyester fiber. To commence, a sheet of fiber was stretched and fixed onto a rectangular aluminum frame of dimensions 70 $\times$ 30 cm^2, then covered on both sides by a photoresist. To ensure a better edge definition of the print, the front side was covered twice by the photoresist. The design is then transferred into the screen as a stencil via photolithography. The characteristics of the screens used were related to the type of ink to be printed. For silver, screens with a mesh of 150 lines per cm and a thread filament of 31 μ m of diameter were used, this screen offer smaller opening due to the smaller size of the particle in the silver ink. To print silicon, screens with a mesh count of 100 lines per cm and a diameter thread of 40 μm were used. The diameter of the silicon particles and clusters in the ink was bigger than the one of the silver, therefore the screens using wider opening were used. It is understood that the density of a screen can influence on the quality of the devices produced with that screen. In this study, the thread filament dimensions, and the printing speed were monitored not to change significantly since our goal was to produce electrically consistent ans stable devices. The

printing speed and screen filaments density of this work were chosen carefully based of previous work done on the printability of silicon done by [24, 29, 49, 60]. The screen tension is a good indicator of the quality of the screen; as a good screen must be able to peel away from the substrate after printing, and be stretched enough to not make a blurred line at the edge of the design. The average screen tension was around (24 ± 2) N/cm at room temperature, before the first use. Screen tension decreases with use, so the tension was regularly checked with a SEFAR TENSOCHECK 100 tensiometer before each print. Screens were discarded when their tension fell below 21 N/cm.

As mentioned above, the squeegee in screen printing is used to force the ink through the screen by applying a shear force to the ink. The squeegees used in this study were of parallelepiped rectangular shape, made of polyurethane with a hardness of 70 on the shore A scale. Throughout printing, the squeegee was positioned in such a way that one of its edges was in direct contact with the screen during the printing process. The angle between the squeegee and the substrate plane was 70°.

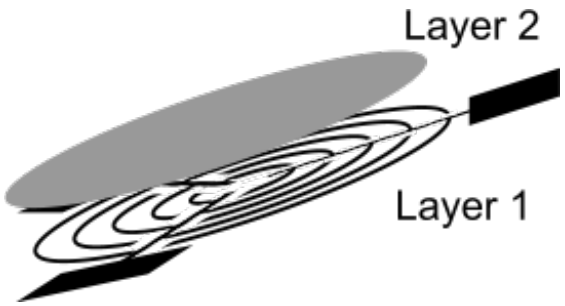


Figure 3.12: *Illustration of printing deposition steps, the first layer is the design of an interdigitated silver layer and the second layer is a plain disk of silicon to be deposit on top of the silver.*

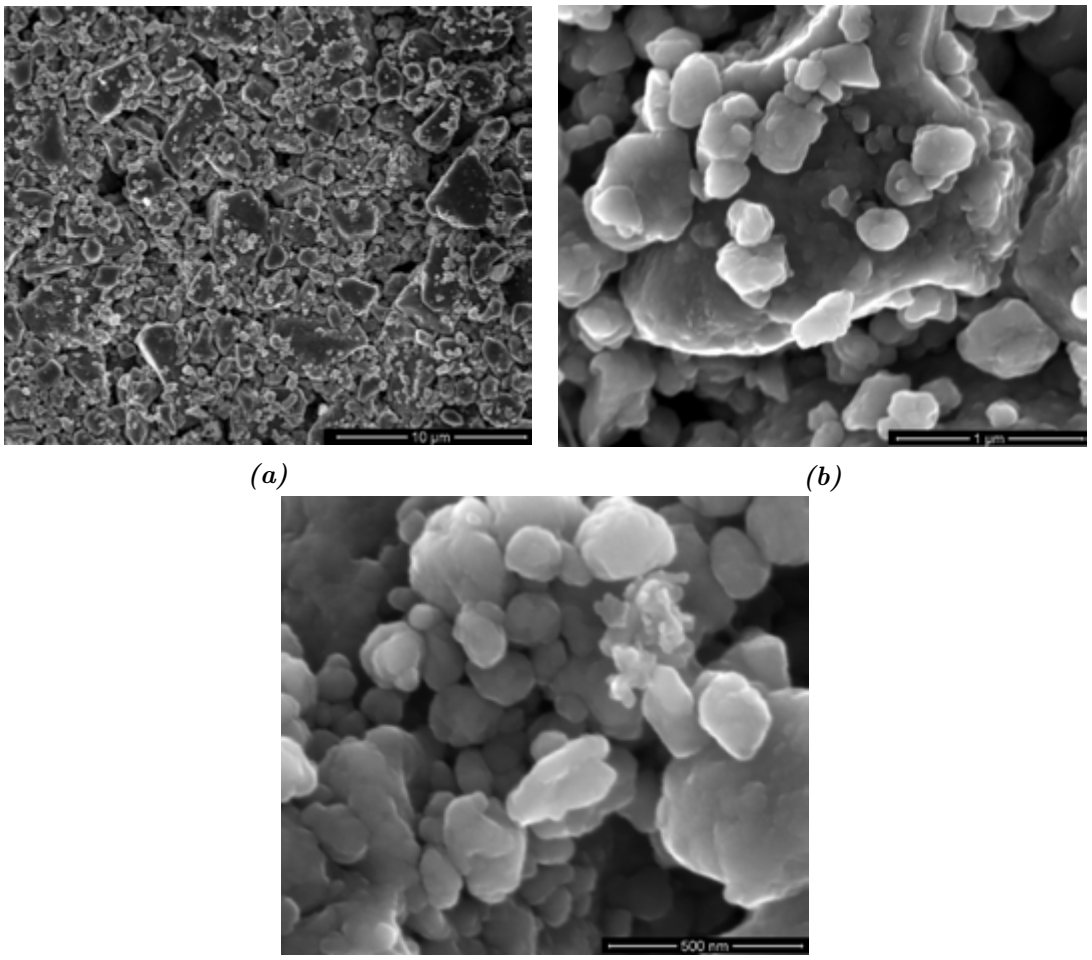
In printed electronics, the speed of the squeegee can influence the thickness of the layer, hence the resistivity of a printed layer [168]. The silver ink was printed at squeegee speed of 250 mm/s, this speed was shown to print a very smooth layer of silver devoid of pinhole with a very constant layer thickness. The silicon ink was thicker therefore needed more shear force applied by the squeegee to go through the screen, so silicon was printed at a speed of 200 mm/s. It was found in previous work that silicon printed at this speed was stable, with a regular thickness and devoid of pinhole [24, 37, 48, 49] . Figure 3.12 is an illustration of the printing sequence of a device. It shows the first layer that is deposited on the substrate, left to dry and then the second layer deposited at a later stage, to form the final device. The devices presented in this work were mostly printed on plain paper, and a few were printed on polyethylene terephthalate (PET). For each set of prints, a registration accuracy of the two layers was made to approximately 200 μm precision. In order to avoid pinholes or poor coverage of a layer, each layer was

printed twice. Between printing the layers, the first layer was left to cure for at least 18 hours at room temperature $(22 \pm 2)^{\circ}$C and relative humidity of $(50 \pm 5\%)$.

3.4.5 Structure of a printed layer of silicon

Printed silicon layers were investigated by scanning electron microscopy using a Nova Nano SEM 230 operated at a beam energy of 5 keV. Typical secondary electron images of the surface of the printed layers are presented in figure 3.13. A low magnification micrograph (figure 3.13a) shows a highly irregular arrangement of differently sized structures, but it also indicates that a continuous network of irregularly shaped structures of silicon is formed. The printed silicon layer surface (figures 3.13b and 3.13c) shows the same printed silicon layer surface at different magnifications, indicating that the layer structures are made of smaller clusters reflecting the structure of the primary clusters found in the silicon powder. The higher magnification micrograph 3.13c also revealed that the printed layer, even at the micro level, is highly porous. A combined study using both the TEM images of figure 3.10 to estimate the primary size of the particle, the line scan of the image in figure 3.13c along the diagonal and the horizontal using the imaging software ImageJ and the greyscale was used to estimate the average size distribution of the particles. An average size distribution of (126.7 ± 3.4) nm along the long axis and (78.4 ± 1.2) nm along the short axis were respectively found [169, 170].

The transistor electrodes in this work were printed using conducting silver ink (Dupont 5000). A cross section of the silver ink was observed under SEM. Prior to the microscopy, silver was printed on plain paper and allowed to dry for 24 hours under ambient conditions. The printed layer was cut through using a very thin steel scalpel, and the cross-sectional view was observed using the Nano SEM 230, operated under similar conditions as described above. Figure 3.14 shows the cross-section of a layer of printed silver at low magnification. In the figure, the top part presents the printed silver and the bottom part the plain paper used throughout this work. Observed under various conditions, such as back scattered, it was clear that the grey area on top of the paper was silver and the dark area below the paper was the dark space inside the SEM. Therefore, a clear delineation between the paper and the silver can be observed in this figure. Similar delineation was observed between printed silicon and paper as well as between the printed silver and silicon. This means there is no mixture of material or structure during the printing.



(a) ***(b)***

(c)

Figure 3.13: *SEM images of printed silicon layer on paper at increasing magnification from (a) to (c).*

3.5 Devices produced

The active layers in the CSTs represented by "S" on the printed transistors in figures 3.15, 3.16 and 3.17 were printed using various types of silicon ink made from p-type and n-type single crystalline prime grade doped silicon wafers or ingots. The silicon wafers were doped with boron and arsenic respectively with an initial resistivity $\rho <$ 0.005 Ωm. The p-type silicon ingot doped with boron has a nominal resistivity of $\rho < 0.001$ Ωm, and the n-type silicon doped with phosphorous has a nominal resistivity of $\rho = 0.001 - 0.00102$ Ωm. The main substrate used for this work was plain paper.

Throughout this thesis, several thousand devices were produced. Devices were printed with various combinations of architecture electrode and active material. Various types of characterization were performed on these devices and will be presented throughout this thesis. It should also be noted that for a set of identical devices produced, in view of the number of devices produced, sample devices representative of the set were

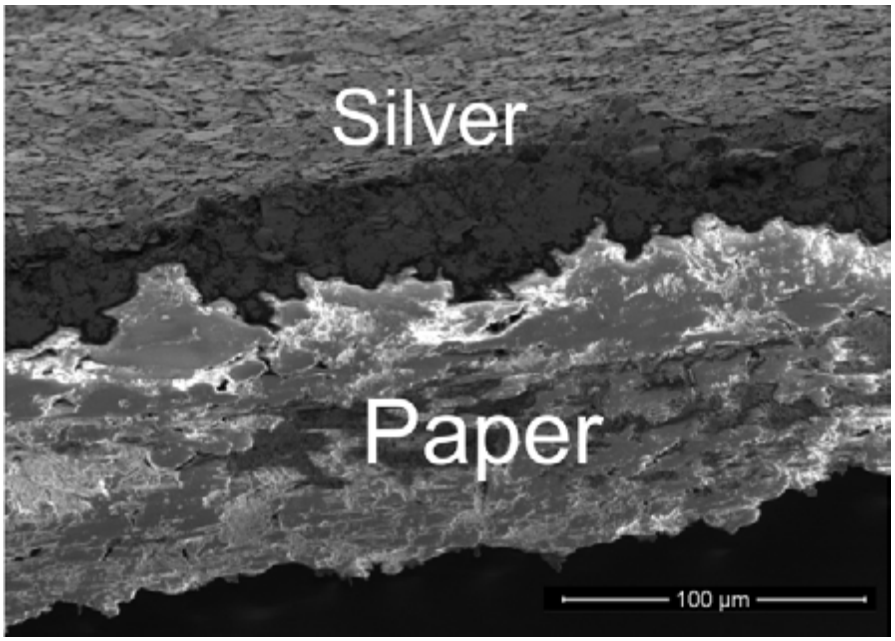


Figure 3.14: *SEM image of a cross sectional view of a printed layer of silver on plain paper at low magnification.*

(a) ***(b)***

Figure 3.15: *Photographs of printed asymmetric CSTs. Electrodes are printed with silver. The dark area labelled S for semiconductor, is the active layer of silicon. Electrodes are represented by B, C, and E.*

(a) ***(b)***

Figure 3.16: *Photographs of two symmetric fully printed transistors with the same type of electrodes. E,B,C represented the electrodes and S is the layer of silicon semiconductor. The active layer of semiconductor in the left side is triangular and the one in the right side is circular.*

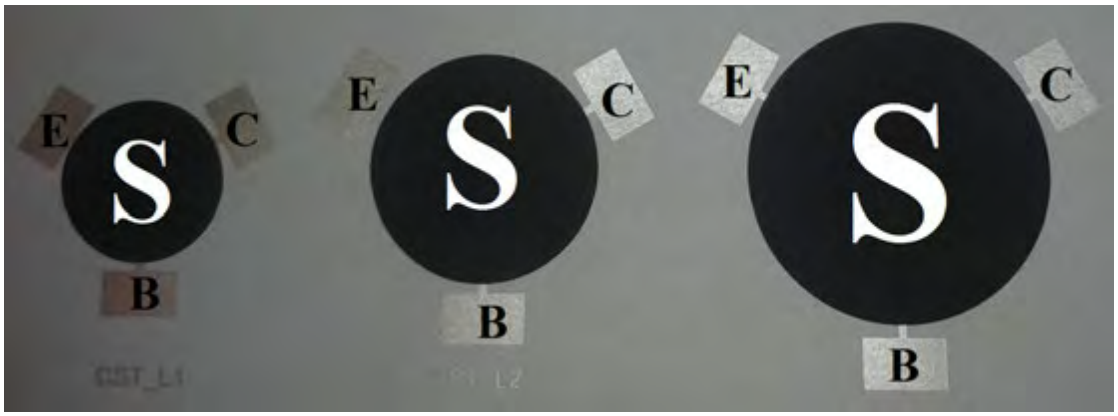


Figure 3.17: *Photographs of three symmetric CST. The diameter of the silicon layer increase from the left to the right. E,B,C represented the electrodes and S is the layer of silicon semiconductor. The electrode was printed with Dupont 5000 silver and the active layer with p or n typed silicon.*

characterized randomly. Table 3.2 describes the devices produced in this work and the type of characterization performed on the devices. For the sake of conciseness, representative samples of the devices will be presented in this thesis.

	asymmetric devices	**Interdigitated devices**	**symmetric**
Produced	≈ 2000	600	≈ 2500
DC characterization with 4200SCS	≈ 500	195	≈ 500
cryogenic study with the HMS		None	30
perfromance in AC/AC	15		20
transient performance		40	
reliability under constant bias current stress			20

Table 3.2: *List of devices produced with the various type of characterization performed on them.*

Besides these devices, in table 3.2 some devices were also produced with the same active material using a Transparent Conducting Oxide (TCO) for the electrodes. This was mainly to confirm that the general behavior of the devices observed in our study was not a result of the type of electrode use but effectively a property of the active layer.

3.6 Electrical characterization of devices

Electrical characterization is of fundamental importance to understand electronic devices, and predict their behavior. The electrical characterization of the devices developed during this work forms a considerable part of this thesis, and the measurement set

up presented in this section were used, to characterize the cup and bold structure and various CST architectures. These characterizations set up were used in DC for room and variable temperature electrical characterization, including the effect of collector voltage bias, the time response of the devices, the temperature dependence of the devices, as well as their reliability under constant current stress. Electrical characterization under AC current/voltage were also performed but will be developed in another chapter.

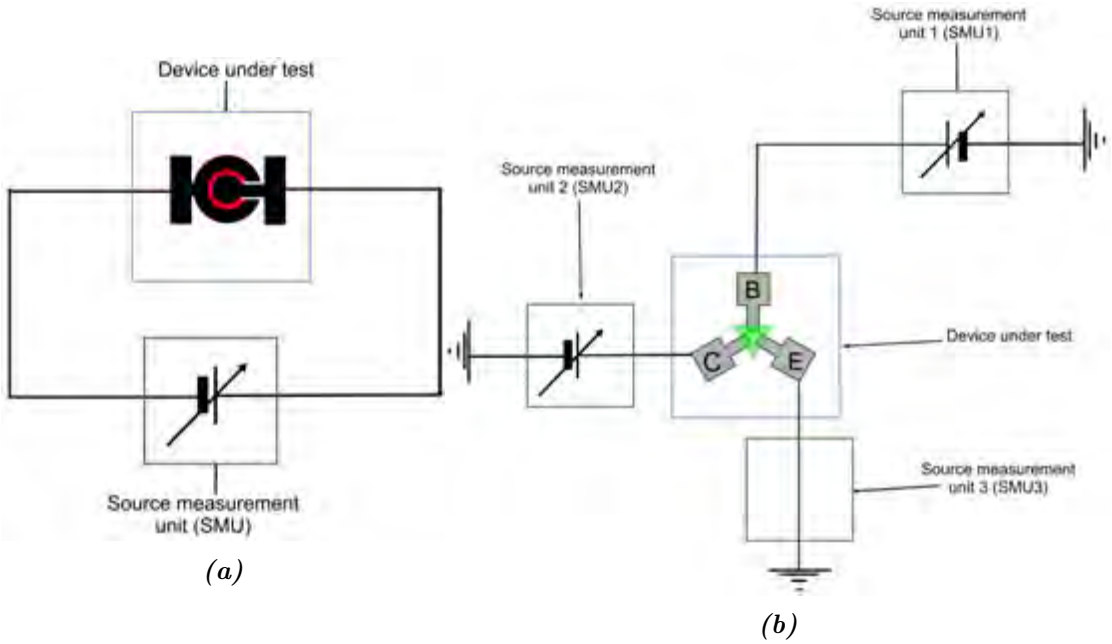


Figure 3.18: *Circuit diagram used during the characterization. (a) circuit used for two terminal measurement, the circuit feature the device under test and a source measurement unit (SMU). (b) Typical circuit used for three terminal electrical characterization, the circuit is made of three source measurements unit all connected to the device under test.*

Figure 3.18 shows the typical DC characterization set up used for this work. Figure 3.18a was used for two terminal characterization of the cup and ball structure, which provides electrical behavior of the active material. Equipment used for characterization in this work were all state of the art equipment, recognized as standard electrical characterization tools, with high precision and reliability for electrical testing. The source measurement units found in figure 3.18, are independent sources of measurement that can source voltage measure current, source current measure voltage, bias current or voltage or simply be grounded. These SMUs are integrated into the characterization tools, the main tools used for this study were the semiconductor parameter analyzer (Keithley 4200 SCS) and the Lakeshore 75014 CCRSM Hall Measurement System. Figure 3.18b, show the CST under measurement, the devices are connected to three source measurement unit. During this study, the emitter connected to the source measurement unit 3, were always grounded and taken as reference. The SMUs used were either automated

while using the Keithley 4200 SCS or made by a combination of equipment while using a testing station.

3.6.1 Characterization using a customized testing station

A custom testing station, shown in figure 3.19 was built using various measurement and testing equipment. The element numbered 5 is the testing board which is presented in detail in figure 3.20. This testing board includes four flexible gooseneck cables, selected for their flexibility fitted with gold-plated spring loaded pogo pins with flat tips, presenting an excellent electrical contact. The test probe springs were used to keep the device under test from moving. During testing, the devices were mounted on a thick sheet of plexiglass. The testing board features a breadboard shown at the right of figure 3.20 that is used to add additional discrete components to the circuit of the device under test. The board contains five banana sockets, four of which are connected to each of the test probes, while the fifth is grounded to prevent hazard. The ISO-TECH IPS601A power supply **(1)** and the Topward 6303 DS Dual Tracking DC Power Supply **(2)**, in figure 3.19 which are able to produce independently up to 60 V DC each was used. Current and voltage were monitored, and recorded using a Keithley 2000 Digital Multimeter **(3)** or/and a Fluke 111 digital multimeter. An Agilent 33220A Arbitrary waveform generator **(4)** was used to generate transient signals.**(6)** Variacs were used to generated AC signal while studying the behavior of CST under AC conditions.

Figure 3.19: *Testing station: this station contains a large part of the equipment used during the electrical characterization. (1) ISO-Tech IPS601A DC power supply; (2) Topward 6303 DS Dual Tracking DC Power Supply; (3) Keithley 2000 Digital Multimeter; (4) Agilent 33220A Arbitrary waveform generator; (5) Probe set and a breadboard; (6) Variacs.*

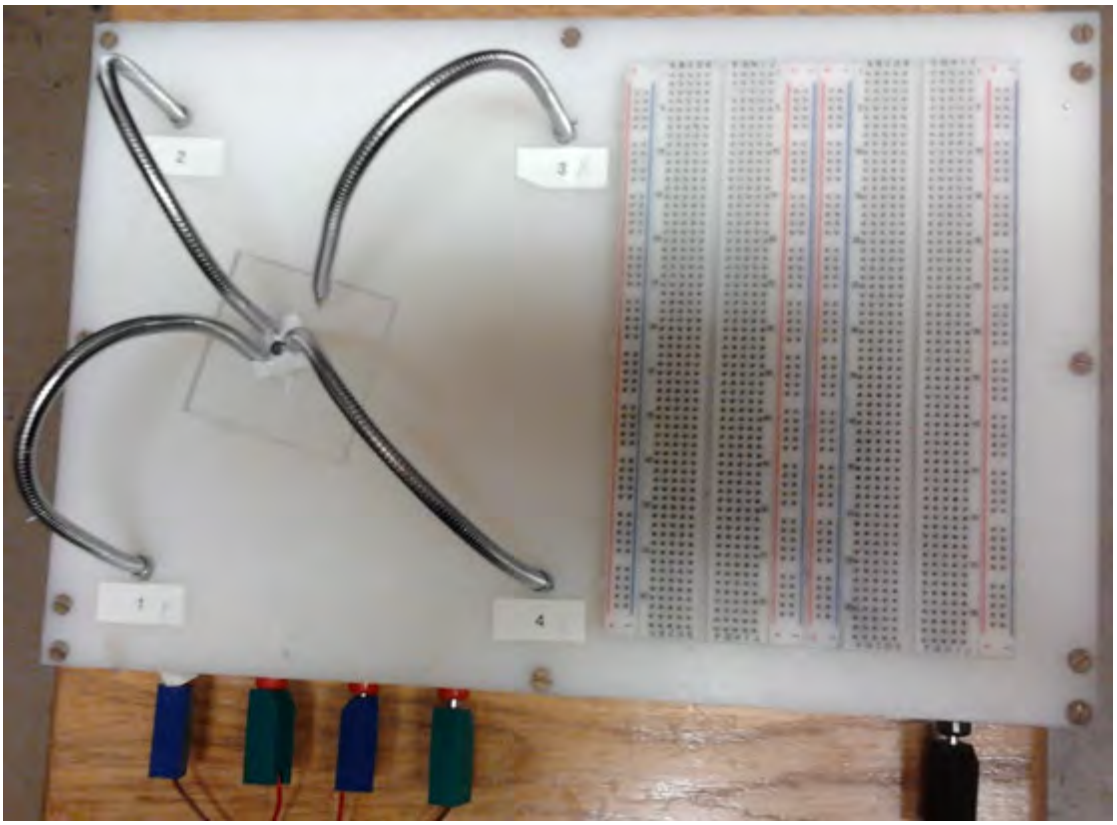


Figure 3.20: *Top view of the testing board (element 5 of 3.19) is made of four goosenecks fitted with spring-loaded pogo pins with a flat head. The figure also shows a transistor under measurement, sitting on the Plexiglas under three goosenecks. The right side of the figure features a breadboard used whenever additional components are needed to be used during the characterization.*

3.6.2 DC characterization using the Keithley 4200 SCS

The semiconductor parameter analyzer (Keithley 4200 SCS) shown in figure 3.21, which has a current and voltage resolution of 1 pA and 1 μV [171], was used for the DC electrical characterization. The Keithley 4200 SCS used in this study has four built-in SMUs, but only three were used. The SMUs source voltage and/or current and simultaneously measure and record them. The Keithley 4200 SCS measurement units operate either as a high voltage source $[-200; 200] \pm 10$ V with a low current source $[-100; 100] \pm 5$ mA or as a low voltage source $[-20; 20] \pm 1$ V and a high current source $[-10; 10] \pm 5$ A. The sample station for the Keithley 4200 SCS is contained in a double-walled Faraday cage (see element (2) of figure 3.21). During this work, the data measurement were several order of magnitude above the resolution of the instrument therefore are consider to be actual measurement and not artifact or noise. The devices are connected with three probes to the SMUs via low resistance triaxial cable. The cage is made of two independent aluminum walls separated by a thick layer of expanded polystyrene. The devices under measurement were mounted on a slice of plexiglas on the metal station

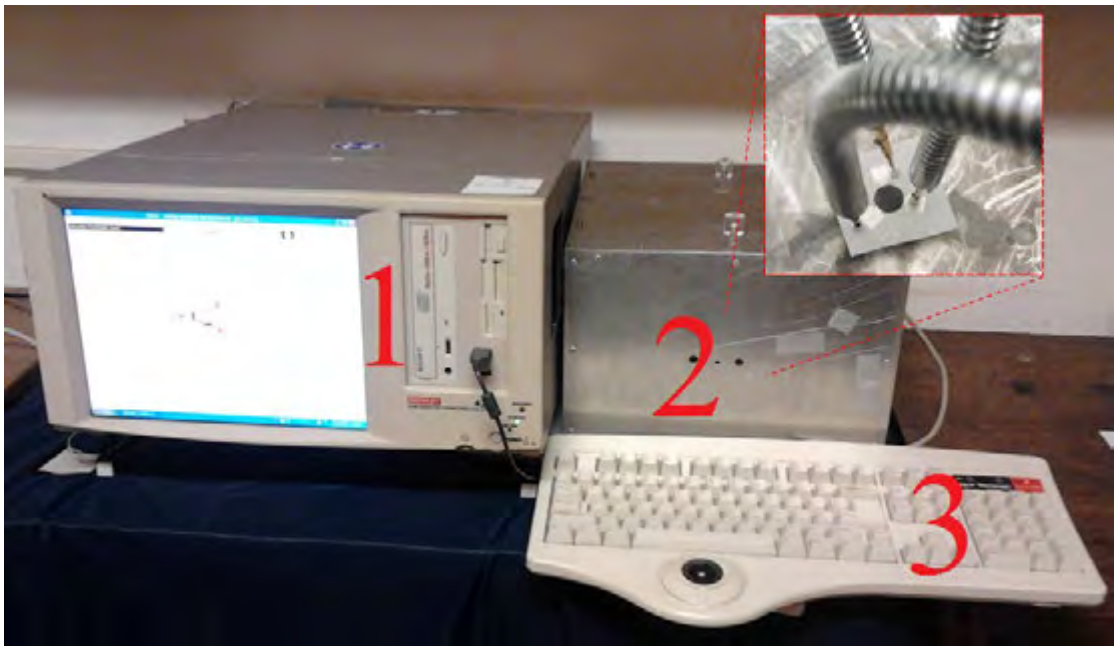


Figure 3.21: *Electrical characterization set up: 1- Keithley 4200 SCS; 2- Double walled box Faraday Cage; 3- Control Keyboard. the insert image in the top-right is an overview of the devices being characterized inside the double walled Faraday box.*

in the inner box. The Faraday cage provides various advantages, including procuring a stable environment during testing, shielding against eventual nearby electromagnetic noise [31], and against any source of light.

3.6.3 CST time response

The switching time response of the transistors produced in this thesis was investigated as an indicator of the quality of their switching and interpreted in terms of the structure of the nanoparticulate material. The time response of any device is broadly seen as the time needed by the device to respond to an input signal [172, 173]. This time response limits the switching speed, and therefore the type of application or circuit where the device can be used, for instance, low-speed devices, will not be adequate for high-frequency applications. The switching speed of the transistor was determined using a transient signal with a rectangular pulse shape of variable width and period. The devices were mounted on the testing board shown in figure 3.20, with the base terminal connected to an Agilent 33220A Arbitrary waveform generator. The generator was set to produce a square signal of 20 V peak to peak magnitude. The square signal from the generator was offset using one of the DC supplies shown in figure 3.19. The collector terminal of the CST was connected to a voltage source which was stepped from 60 to 100 V while the emitter terminal was grounded through a resistor.

3.7 Temperature dependence measurement

The number of electronic devices and their range of application has increased exponentially during the past few decades [174–176], and more applications require devices to operate under cryogenic conditions [177–179]. Very little work has been done on the ability of different types of transistors to operate at cryogenic temperatures below 150 K; this is partly due to the difficulty in characterizing devices at low temperature. Intrinsically, the properties of semiconducting materials are temperature dependent, therefore the behavior of a semiconductor device can change drastically at extremely cold temperature [180]. Therefore, producing electronics devices which can retain their function at cryogenic temperature, is a significant step toward their application at very low temperature.

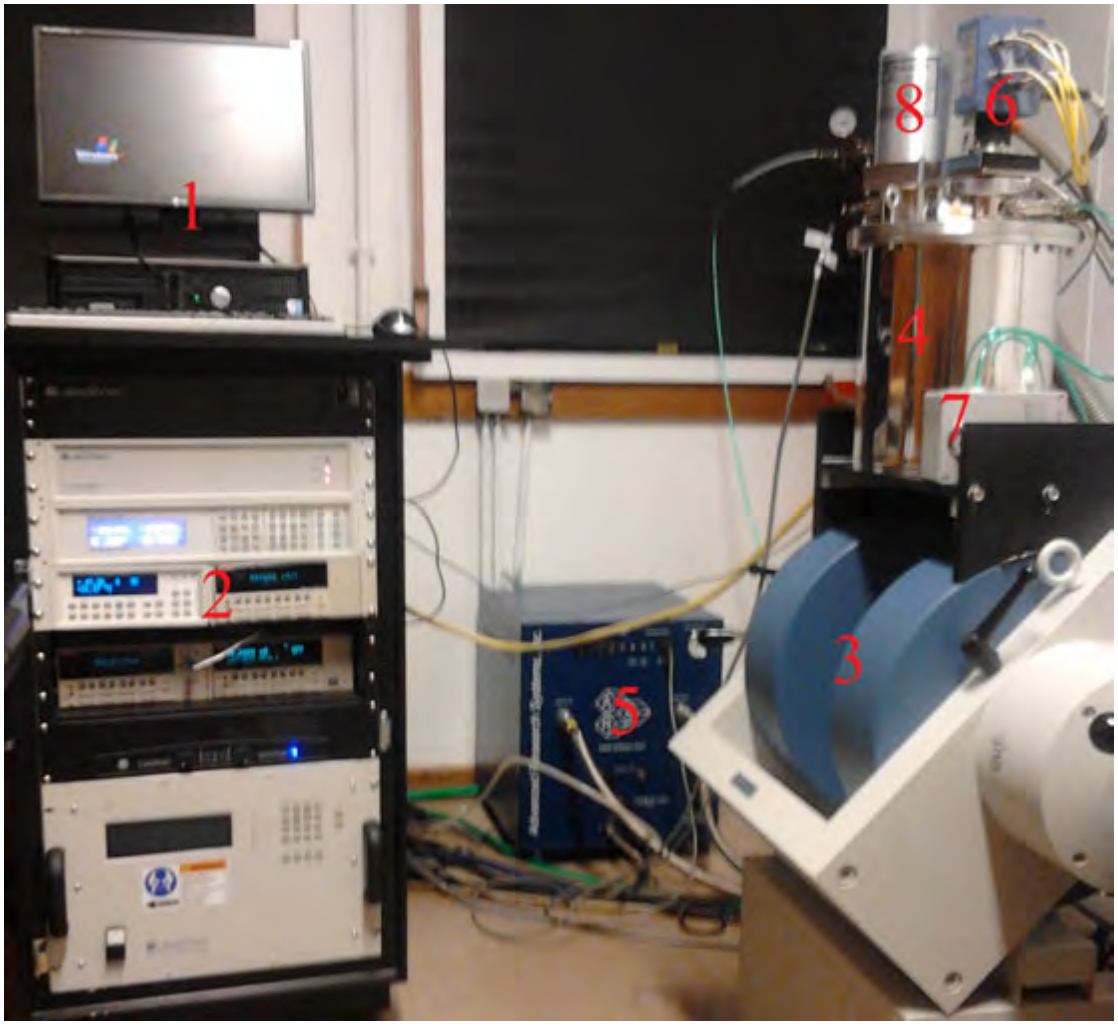


Figure 3.22: *The Lakeshore 75014 CCRSM Hall Measurement System: (1) PC for control (2)Cluster of electronic measurement equipment made of volmeter, ammeter, current source and electromagnet power supply (3) Electromagnet (4) Cryostat (5) Compressor (6)Sample holder junction box (7) Flush fill unit (8) Expander*

The measurements were performed using a Lakeshore 7500 CCRSM Hall Measurement System (HMS) figure 3.22, which is a fully automated electrical characterization system. The principal function of the HMS is to perform IV characterization at variable temperatures and magnetic fields with high precision. The instrument is actually a cluster of state of the art hardware and software integrated to run automated measurements. The main components of the HMS include: a high precision voltmeter (Keithley 2184A Nanovoltmeter), a constant current source (Keithley 6620 Precision current source), a high precision ammeter (Keithley 6485 Picoammeter), a Lakeshore 642 Electromagnet Power Supply unit with electromagnet, Lakeshore 475 DSP gaussmeter, HMS Matrix amplifier, Lakeshore 340 temperature controller and a cryostat with heating and cooling system [24, 181, 182]. Specific information on the HMS can be found in reference [182] .

The HMS in this work was used only for temperature dependent IV characterization under zero magnetic field. The HMS 75014, comes with tails of approximately 1.5 m each. A sample holder is located at the bottom of the tail, the sample holder is made of 6 connectors that could be wired to the device under measurement. The upper end of the tail is made of 6 terminals all connected to the sample holder and offer the possibility to be connected to various sources of measurement. The sample to be measured was mounted on an appropriate sample holder, the device electrodes (two or three) were soldered to very thin low resistance silver wires and connected to the terminals on the sample card. The contact resistance of the solder junctions was confirmed to be negligible, compared to the sample resistance. The sample holder was then inserted in the cryostat until the sample was in position at the bottom of the cryostat tail. The sample holder was then hermetically sealed with an O-ring, and the residual air was flushed out of the sample chamber with helium, which also served as the heat exchange gas. A model 75014 closed cycle refrigerator sample module (CCRSM) and a two stage helium compressor technology capable of achieving cooling, were used to provide variable temperature environment of temperature between 5 to 345 K. The Lakeshore model 340 temperature controller, fitted with two internal heaters and sensors was used to provides stable temperature during the characterization. The first sensor monitors the temperature at the head of the tail, while the other sensor is situated next to the sample and used to specifically measured the temperature of the sample. The two heaters of the system take a considerable time to settle at a given temperature, as the machine uses two independent PID algorithms for the two heaters to attain the set sample temperature. For the variable temperature characterization of this work, a dwell time of 2 seconds was used, the temperature was ramped at 1.5 K/min and the settling time of 45 min minimum allowed at each temperature. The long settling time was chosen in such a way that the first 4 decimal digits of the temperature do not longer fluctuate. Thus the time taken to collect the data for each sample for the temperature from 340 to 10 K were

approximately 24 hours. For the two terminal devices, which were used mainly to study the behavior of the network of nanoparticles, various IV characteristics were obtained over a temperature range from 345 to 10 K. The HMS was used in its automated mode by sweeping the current and measuring the voltage for a given temperature.

A different set-up was necessary to study the transfer characteristics of the three terminal device. Although very reliable and versatile, the HMS software is unable to hold the voltage or current constant in one of its SMU and sweep current/voltage between other terminals, therefore making it system not appropriate to record IVs of a transistor. To tackle this issue, for variable temperatures measurement on transistors, low resistance cables were used to connect the connectors from the sample holder tail to the Keithley 4200 SCS SMUs. Thus for a three terminal device, the CCRMS was used to cool down the sample, with the PC only controlling and monitoring the parameters of the cryostat chamber, while the Keithley 4200 SCS was used to measure and record the transfer characteristics.

3.8 Results

3.8.1 Electrical behavior of printed silicon

In order to understand properly the electrical behavior of the CSTs produced in this thesis, we first studied the p and n doped silicon used throughout the study. The semiconducting material was studied by performing Current-Voltage (I-V) characterization on p and n-doped silicon in the temperature range from 340 to 10 K.

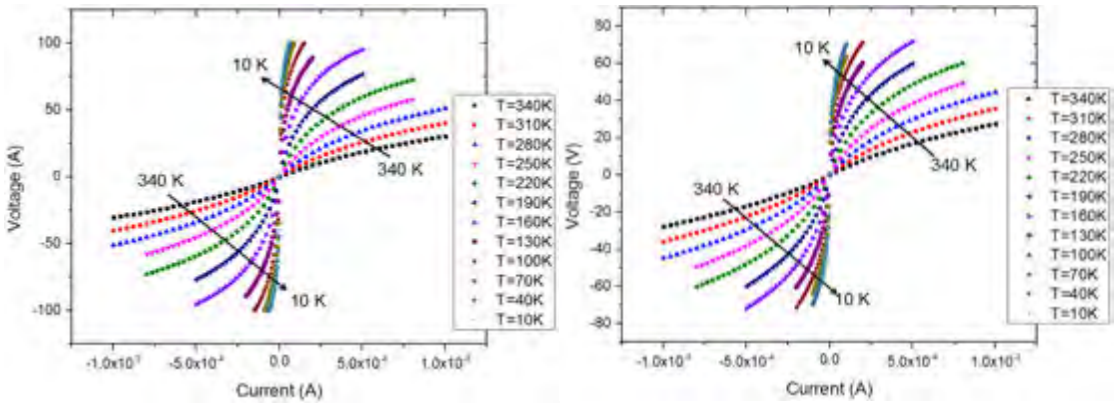
Figure 3.23: *The cup and ball structure use to study material behavior.*

The electrical properties of the silicon used were first studied using the test structure shown in figure 3.23, referred to as cup and ball. This is made of two electrodes, the left in a cup shape and the right in a ball shape with a gap of 200 μm. The structure is bridged by a layer of active material as shown in the right side of figure 3.23. In this work, the electrodes of the test structure were printed with silver and the active layers (shaded in red) with p, n-doped or metallurgical silicon. Using a Wyko NT9100

optical Profiler from Veeco in Vertical Step Interferometry (VSI) mode, we analyzed the thickness and the average roughness on each printed layer. The average layer of the printed silver was around 4.7 μm, the analysis of the highest peak point to the lowest in the same printed sample yielded to a surface roughness of 1.05 μm. Similar analysis made on the printed layer of silicon yielded a thickness of 18 μm and a surface roughness of 5 μm [37]. Additionally, the cross-section of the printed layers observed under a SEM corroborated the results obtained from the profilometry [37].

Figures 3.24a and 3.24b are typical current-voltage characteristics of n and p doped silicon used for this study, the IV characteristics of more devices have been added to the appendix, to show the consistency of the cup and ball test structure. The curves of figure 3.24 were measured in a temperature range between 340-10 K. These IV curves were measured using the Lakeshore 7500 CCRSM, in its automated measurement mode. During the operation, when a given temperature was settled, the IV was measured by sweeping the current and recording the voltage. The experimental data of the various current-voltage were extracted from the software and re-plotted using Origin 9 for more clarity and further investigation. The typical IV characteristics of the material, as shown in figures 3.24a and 3.24b, were consistent with previous studies [24, 49] on silicon produced by the same method. The IV curves have a symmetric shape passing through the zero voltage, zero current which suggests the behavior of diode in back to back configuration, varistor-like components or materials made of grains and boundary at microscopic level. The IV curves also show a non-linear behavior with a differential conductance (G=dI/dV) increasing with voltage for a given temperature. The plain paper used as the substrate for this study was the office A4 paper made from wood. At room temperature the substrate was an insulator, for instance using a uni-T digital multimeter capable of reading resistance of up to 10^8 Ω. We were not able to read the resistance of a segment of approximate length 250 μm, whereas on the same distance an approximate value of 2-3 MΩ, and 1-3 Ω were read for the printed silicon and silver respectively. Viewing the delineation between the paper and the printed inks observed from microscopy, we assumed that the contribution of the substrate on the overall electrical behaviour of the devices was minor. Thus, the IV characteristics show that for a given voltage, the differential conductance decreases with the temperature, from which it can be inferred that thermal activation is an important mechanism of charge transport in the structure.

Due to the relative high times required to perform a complete set of variable temperature measurement on a cup and ball structure, 20 devices were measured in these conditions and few more of them will be reported in the appendix section. All the measurements were performed under DC regime, and they were no relaxation between measurement, once the data for a given temperature were recorded, the system was ramped down to



(a) *(b)*

Figure 3.24: *Typical current-voltage (IV) curves characteristics for cup and ball printed on plain paper and characterized for temperature between 340 to 10 K.* ***(a)*** *active layer is n-doped silicon;* ***(b)*** *active layer is p-doped silicon.*

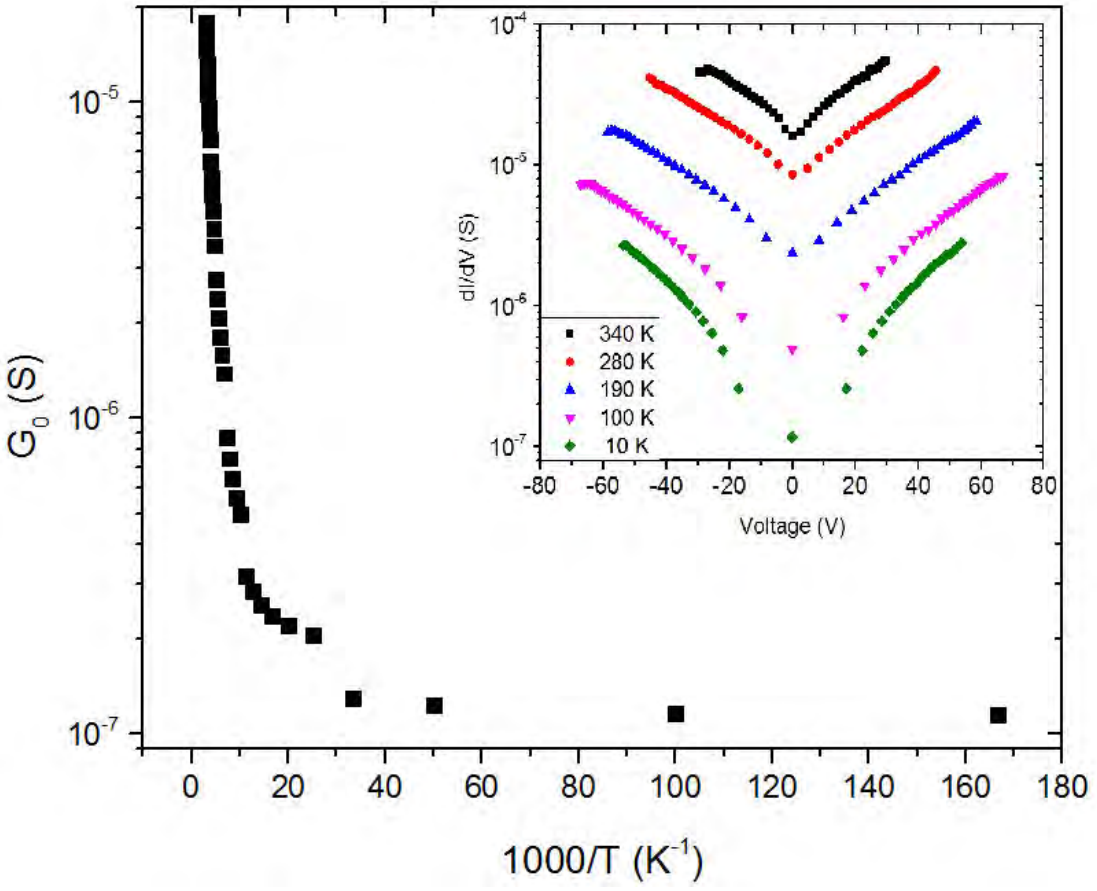


Figure 3.25: *Temperature dependence of a minimum conductance of a printed p-doped silicon layer produced by milling. The insert shows the differential conductance (G=dI/dV) as a function of the voltage at several temperatures in the range from 340 to 10 K.*

a lower temperature. The transfer characteristics obtained with these test structures were very similar, hence their reproducibility, thermal cycling was not performed on the device, this means that a device was not cool, then heat up and cool again.

The inset in figure 3.25 shows the differential conductance (G=dI/dV) as a function of applied voltage for a typically printed layer of the p-typed silicon employed in this work at various temperatures. From the inset, the minimum differential conductance was extracted near zero voltage for each temperature, and the result is presented in a form of an Arrhenius plot for $G_0(T)$ in figure 3.25, were $G_0(T)$ represent the minimal differential conductance for a given temperature. The graph of $G_0(T)$ has two main regions, one at low and the other at high temperature. At temperatures greater than approximately 200 K, $\log G_0(T)$ is proportional to T^{-1}, meaning that the electrical transport is simply activated. At very low temperature, below approximately 90 K, we observed that $G_0(T)$ decreases much more slowly. This is consistent with variable range hopping transport in which the conductance is $G \approx \exp(-(T_0/T)^{\gamma})$ where γ and T_0 are constants related to the material [183]. This overall behavior was typical of material with thermally activated charge transport.

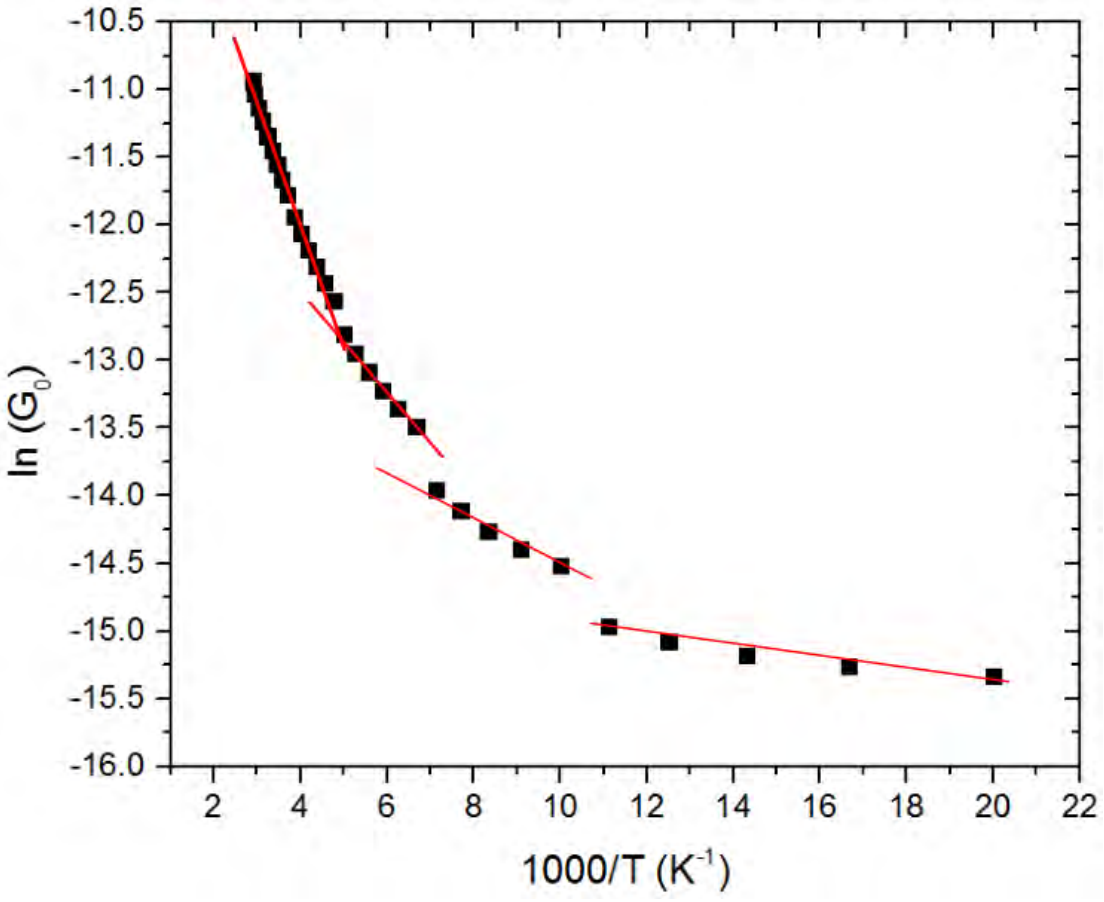


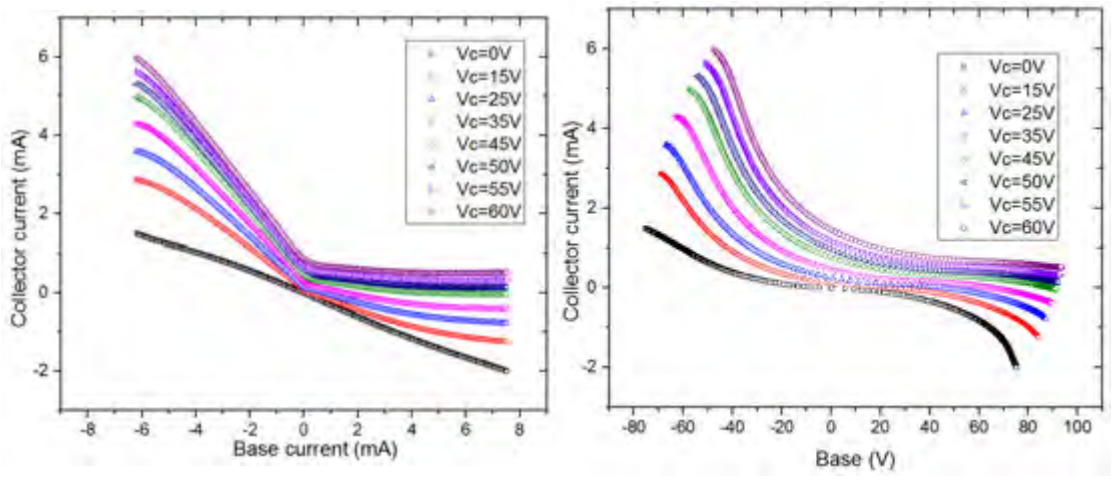
Figure 3.26: *Arrhenius plot of the logarithmic minimal conductance against the temperature of a printed p-doped silicon layer produced by milling. The red solid segments, represent the unweighted line of best fit of the data for each data section.*

The graph of figure 3.26, is a logarithmic plot of the minimal conductance of a printed p-doped silicon layer produced by milling, represent against the temperature. From figure 3.26, we denoted four regions with each governed by its own activation energy. A linear fitting was made in each of the four sections, then the slopes of the linear fit were extracted and used to determine the activation energy governing each region. The values of the activation energy were obtained to be (3.38±0.51)meV, (16.80±1.43)meV, (35.24±1.78)meV, and (75.05±2.19)meV for temperature below 90 K, between 90-140 K, 140-200 K and above 200 K respectively. These values of the activation energy suggested that the carriers transport mechanism are not identical at low and high temperature, so besides the thermally activated charge transport other forms of carriers transport may be involved.

3.8.2 DC characteristics of a printed CST W transistor

The main focus of this thesis is the development and characterization of the novel current-driven switching transistor. This section presents the electrical characterization, namely the current-voltage, as well as the current-current characterization of a current switching transistor. The model presented here is the type W interdigitated model described in figures 3.7 and 3.17. Three hundreds devices labelled CST W with an outer diameter of silicon of 22.9 mm were produced. Fifty percents were chosen randomly and characterized, of which more than 80% showed consistent behavior. Most of the non-functional devices were due to poor sample registration during the printing or, other factors that could be attributed to the screen printing. Additionally, 150 more CST W were produced, in three sets of 50 devices, each with silicon outer diameters of 22.9 mm, 32.5 mm and 42.6 mm respectively. A third of each category were characterized. The transfer characteristics presented here were obtained using the Keithley 4200 SCS, by stepping several voltages on the collector terminal while sweeping the current and the base with the Emitter grounded at room temperature.

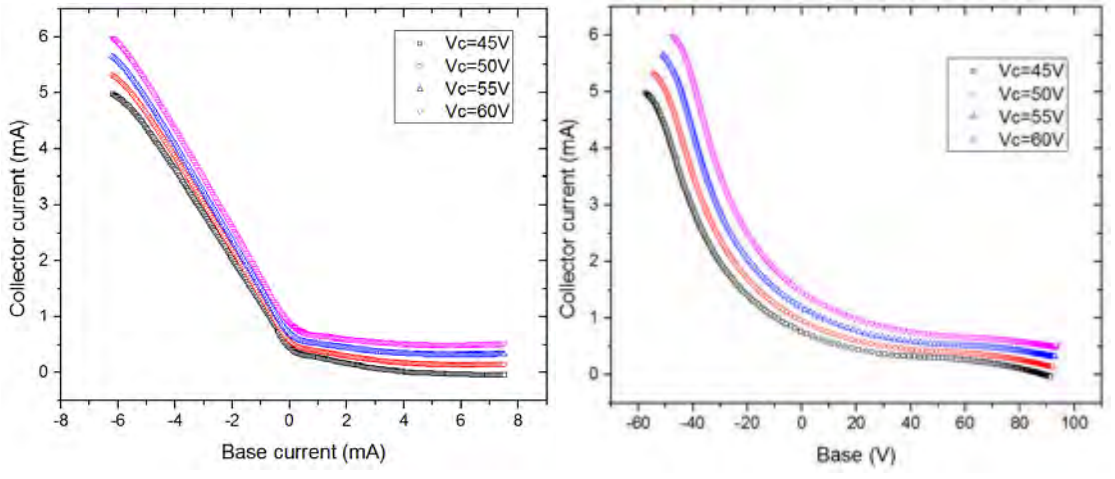
Figure 3.27a shows current-current characteristics of a CST W at collector bias voltages of 0,15,25,35,45,50,55 and 60 V respectively. These curves present two parts, which show that the response of the collector electrode depends on the magnitude of current in the base, specifically the differential $\mathrm{d}I_c/\mathrm{d}I_b$ depends on the direction of I_b . When the current injected in the base is negative, there is a positive current in the collector. Both graphs of 3.27 show that for a given negative value of current or voltage, the positive current in the collector increases with the value of the voltage bias, reaching a ratio of approximately $I_c/I_b \approx$-1 around $V_c = 60$ V. However, when we apply a positive current in the base, the resulting collector current is negative for low collector bias voltage. This results in a negative slope that can be observed. For higher collector



(a) *(b)*

Figure 3.27: *Transfer characteristics of CST W printed on paper with silver electrodes and highly p-doped type silicon. Device label CSTW:P-2-1(a)current-current transfer characteristics for 8 collector bias voltage. (b) current-voltage transfer characteristic for 8 collector voltages.*

voltages around 30 V, the slope of I_c/I_b tends to zero, therefore the current stops in the collector. The property of controlling current in an electrode or switching current is the main reason why these devices were named current switching transistors. Similar behavior was previously reported in insulated gate field effect transistors (IGFET)using active silicon produced by similar method [31].



(a) *(b)*

Figure 3.28: *Transfer characteristics of CST W printed on paper with silver electrodes and highly p-doped type silicon. This is an extract of the 4 highest collector voltages of 3.27.(a)current-current transfer characteristics (b) current-voltage transfer characteristic.*

The graphs in figure 3.28 are extracts from figure 3.27, with a view of having a closer look at the region where the transistor is switching. Similar transfer characteristics are shown in figure 3.29, for device CST W: P-5-4. The curves of figure 3.29 , clearly show

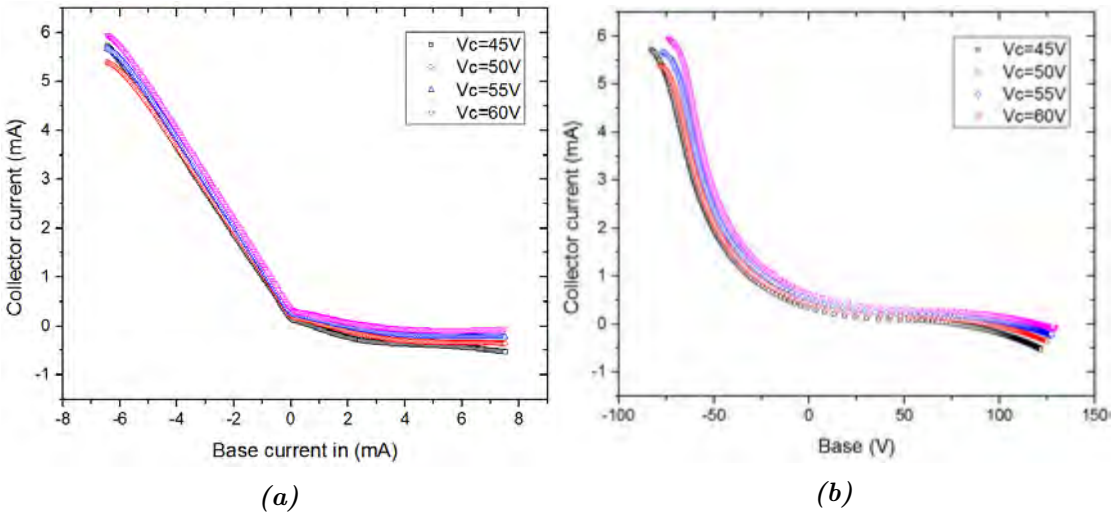


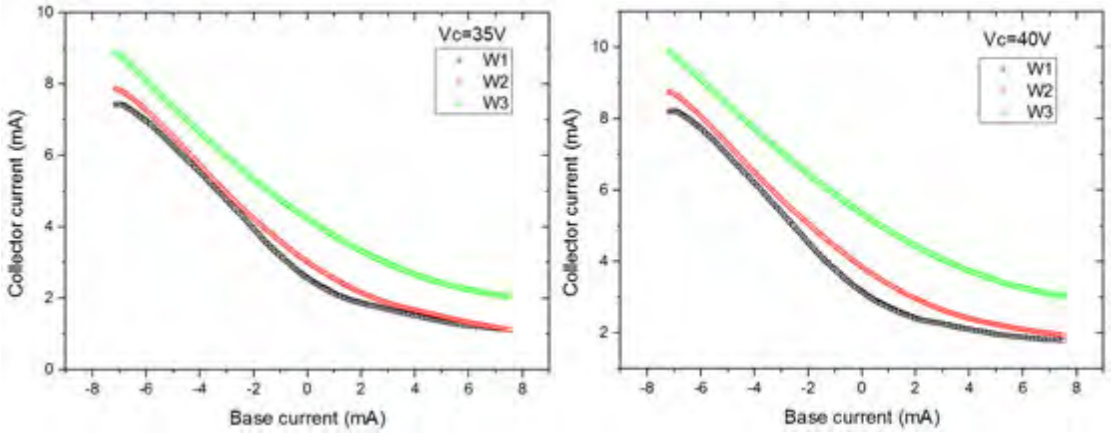
Figure 3.29: *Transfer characteristics of CST W printed on paper with silver electrodes and highly P-doped type silicon. Device label CSTW:P-5-4(a)current-current transfer characteristics for 4 collector collector voltage. (b) current-voltage transfer characteristic for 4 collector voltage.*

that the current in the collector could be turned off by applying current or voltage to the base. This state will be referred to as the "off state". We can also realize from the current-current transfer characteristics, that the "off current phase" starts when the base current becomes positive. While looking at current-voltage characteristic, we note that, for this model of transistor at a very high base voltage, the collector terminal may slowly start conducting again. One of the main objectives of this thesis was to improve the design of the devices in order to have a permanent off state from when the devices turn off, and another was to perform this current switching at low bias voltage without changing the fundamental structure of the transistor. The latter concern will be presented in the next subsection.

3.8.3 Influence of silicon channel width in the CST

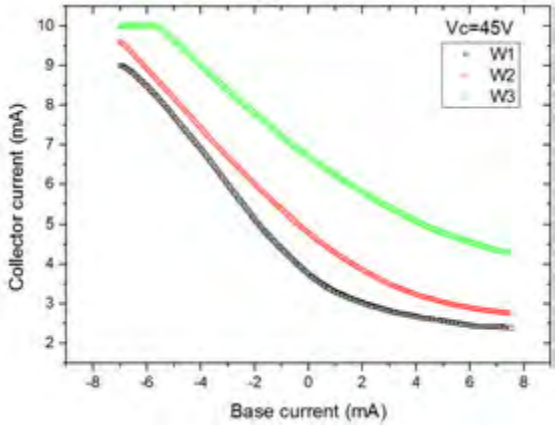
Figure 3.27a showed us that the current could be switched in the collector terminal, at high base voltage, and particularly when the collector bias is above 35 V for the CST W. Below this bias switching threshold, the devices conduct independently of the base voltage. We also note that the switching behavior is more defined with increasing collector voltage. For instance, the switching region of the transfer characteristics of figure 3.27a tend to the horizontal as the collector bias voltage increases. Further investigation was carried on by varying the transistor width in the interdigitated design while keeping the channel length constant. The transistor channel length could not have been reduced any further due to printing constraints. The total width of the transistor CST W was derived to be: $W = 2\pi n\Big[r_{min} + (n-1)L\Big]$ with with the transistor length L=0.5 mm

and the minimal track radius r_{min}=4 mm. The with W represents the total width of the silicon track, and n the number of gaps between the silver fingers. The values of n are 9, 14 and 19 respectively, thus W_1 =452.16 mm, W_2 =923.16 mm, and W_3 =1551.16 mm.



(a) ***(b)***

Figure 3.30: *Current-current transfer characteristics of 3 different CST W printed on paper with silver electrodes and highly P-doped type silicon. (a) Current-current transfer characteristics at V_c =35 V. (b) Current-current transfer at V_c =40 V. W_1, W_2, W_3 are the respective channel widths of the transistor.*



(a)

Figure 3.31: *Current-current transfer characteristics of 3 different CST W at biased $V_C = 45V$.*

Figures 3.30 and 3.31 are the current-current transfer characteristics of 3 CST W, produced simultaneously and on the same substrate. During the characterization, the collector electrodes were held at was 35, 40 and 45 V respectively for each of the devices. We observed that although the trans-resistance remains negative, the switching is weakened at low collector voltage. Additionally, when the channel width is increased there is a higher current in the collector channel as observed in the curves. The graphs of figures 3.30 and 3.31, show that at a given voltage, the transistor with narrower channel

displays better-switching behavior, but has a lower current compared to its counterpart with wider channels. It is important to note that, the plateau observed in the first region of the transistor of length W_3 on figure 3.31, is due to the limitation in compliance current on the Keithley 4200 SCS input.

3.9 Discussion

3.9.1 Printed layer modeling

From the IV characteristics presented in the previous section (3.8.1), we derive a mathematical model to describe the electrical response of the material. The symmetric shape observed in figures 3.24b and 3.24a suggest the behavior of a diode. Therefore, the doped material was modeled with an equivalent electric circuit made of two diodes mounted in an anti-parallel configuration as shown in figure 3.32. Another description of the material was made with the model in figure 3.33, where the resistance R is a series resistance attributable to the leads and a constant resistance at the silicon-silver interface. Whenever a voltage is applied between the points A and B, one of the diodes will be forward biased and the other will be reversed biased. Therefore, each diode will reproduce one branch of the symmetric IV curve. The equivalent circuit justifies the symmetry observed on the material IV curve to always be passing the current.

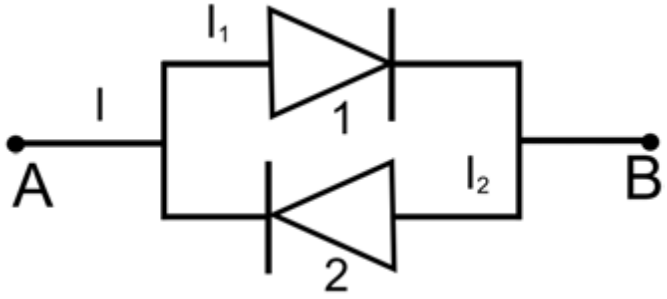


Figure 3.32: *Equivalent circuit describing the printed doped-silicon. This circuit is made of two diodes 1 and 2 in an anti-parallel configuration. I, I_1 and I_2 are the currents in the circuit.*

In figure 3.32, I, I_1 and I_2 are the total and partial current in the circuit when a voltage is applied between A and B. When a DC voltage is applied between A and B with the positive electrode connected to A, diode 1 will be in forward bias and diode 2 in reverse. If the voltage is reversed, we will have the opposite effect with the second diode now being forward biased. In general, the current I will be the sum of the current I_1 and I_2 flowing in each diode. The current flowing in a diode is given by :

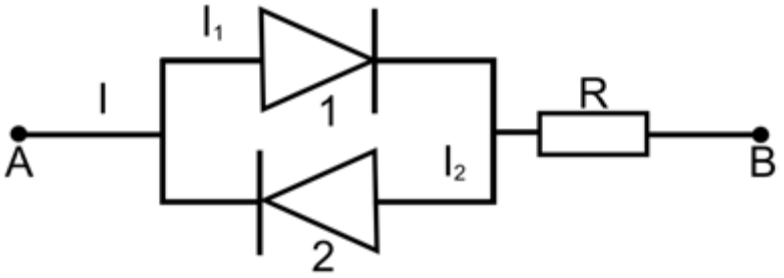


Figure 3.33: *Equivalent circuit describing the printed doped-silicon. This circuit is made of two diodes 1 and 2 in anti-parallel arrangement with a resistor in series. I, I_1 and I_2 are the currents in the circuit.*

$$I = I_s\Big[\exp(\frac{eV}{\eta k_B T}) - 1\Big], \tag{3.2}$$

where e, η, k_B and T are the electronic charge, the diode ideality factor, the Boltzmann constant and the absolute temperature respectively. V is the voltage applied across the diodes and I_s is the diode reverse saturation current. The diodes 1 and 2 in the modeling are made of the same material, therefore η, and I_s are the same. The current flowing in the diode 1 can be written as:

$$I_1 = I_s\Big[\exp(\frac{eV}{\eta k_B T}) - 1\Big], \tag{3.3}$$

The second diode being in opposition to the first one, the expression of the current in that diode is given by:

$$I_2 = -I_s\Big[\exp(\frac{-eV}{\eta k_B T}) - 1\Big]. \tag{3.4}$$

Thus the current I flowing through the combined diodes as a function of the voltage applied is:

$$\begin{aligned} I &= I_1 + I_2 \\ &= I_s\Big[\exp(\frac{eV}{\eta k_B T}) - 1\Big] - I_s\Big[\exp(\frac{-eV}{\eta k_B T}) - 1\Big] \\ I &= I_s\left[\exp(\frac{eV}{\eta k_B T}) - \exp(\frac{-eV}{\eta k_B T})\right]. \end{aligned} \tag{3.5}$$

Equation 3.5 describes a non-linear relationship between the current in the anti-parallel system and the voltage applied. This was used to describe both the material and later to describe the transistors produced in this work.

By taking into consideration the resistor, as in figure 3.33, the effective voltage flowing into the diode will be :

$$\begin{aligned} V_D &= V_A - V_B - RI \\ &= V - RI. \end{aligned} \tag{3.6}$$

Therefore, the current I flowing in the branch will be given by :

$$I = I_s \left[\exp\left(\frac{e(V-RI)}{\eta k_B T}\right) - \exp\left(\frac{-e(V-RI)}{\eta k_B T}\right) \right]. \tag{3.7}$$

Equations 3.5 and 3.7 were respectively used to fit the IV characteristics. We fitted the experimental data of the IV curves using an unweighted least-square model using equation 3.7, for temperatures between 7 to 345 K. The series resistance values ranged from(150 ± 10 %) kΩ to (12 ± 5 %) kΩ. This was in agreement with previous experimental results [24, 38] of measurements performed at 300 K. So we can conclude that the model presented here correctly describes doped milled silicon nanostructured systems produced by milling within the range of temperatures study in this thesis.

The current-voltage electrical characteristic of figure 3.34 shows the electrical behavior of the active material in operation at 300 K, with a solid fitted line of the experimental data. The experimental data of figure 3.24 were fitted with the analytic equation 3.7. By nonlinear implicit fitting of the data, the best-fit line of the experimental data was plotted as the solid line (red) in figure 3.34. As observed in figure 3.34, the theoretical model fitted the experimental data with extraordinary agreement at all temperatures.

We fitted the experimental data of the IV curves using an unweighted least-square model using equation 3.7, for temperatures between 340 to 10 K. The series resistance values ranged from(150 ± 10 %) kΩ to (12 ± 5 %) kΩ. This was in agreement with previous experimental results [24, 38] of measurements performed at 300 K, so the model presented here correctly describes milled doped silicon nanostructured systems produced by milling within the range of temperatures study in this thesis.

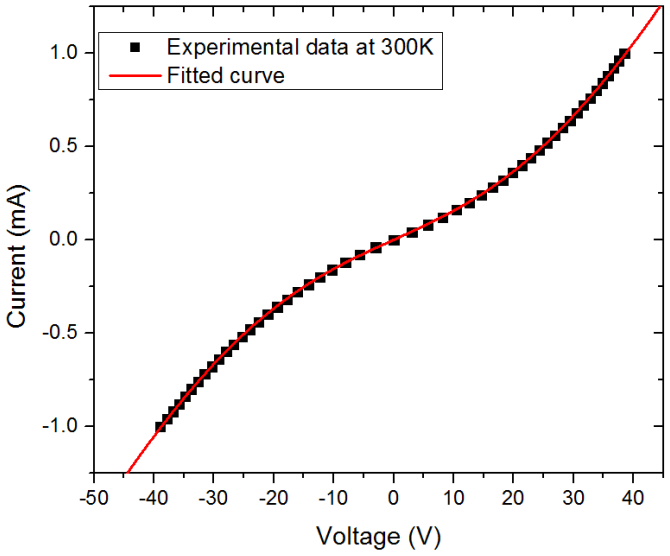


Figure 3.34: *Current-voltage transfer characteristics of the active material, obtained from the cup and ball structure. The black square represents the experimental data of the transfer characteristic at 300 K, whereas the solid red line is the best fit of the data using the equation 3.7.*

3.9.2 CST W modeling and parameter fitting

In the previous section, we were able to model the printed silicon with high accuracy as a two terminal device made of anti-parallel diodes. Viewing the current switching transistor as a three terminal device, we were also able to model it as well using the branch of anti-parallel diodes as a basic unit. Figure 3.35 shows the analogue of the current switching transistor using discrete components. Each pair of terminals is modelled with two anti-parallel diodes as discussed earlier. For the modeling of the figure 3.35, B, C, and E are base, collector and emitter terminals respectively. I_B,I_C and I_E are the base, collector and emitter currents flowing into or out of the electrodes respectively. I_{CE},I_{CB} and I_{EB} are the internal currents between the collector-emitter, collector-base, and emitter-base respectively. V_E, V_C and V_B are the emitter, collector, and base voltage at respective terminals. During the electrical characterization, the emitter was grounded and also used as a current sink, while the collector was kept at a constant voltage as the current was swept at the base.

Using the equation of the current flowing in a system of two anti-parallel diodes described by equation 3.5, and the Kirchoff's junction rule with the arbitrary directions of current chosen above, we can write:

$$I_{CE} = I_{CEs}\left[\exp\left(\frac{eV_{CE}}{\eta k_B T}\right) - \exp\left(\frac{-eV_{CE}}{\eta k_B T}\right)\right], \tag{3.8}$$

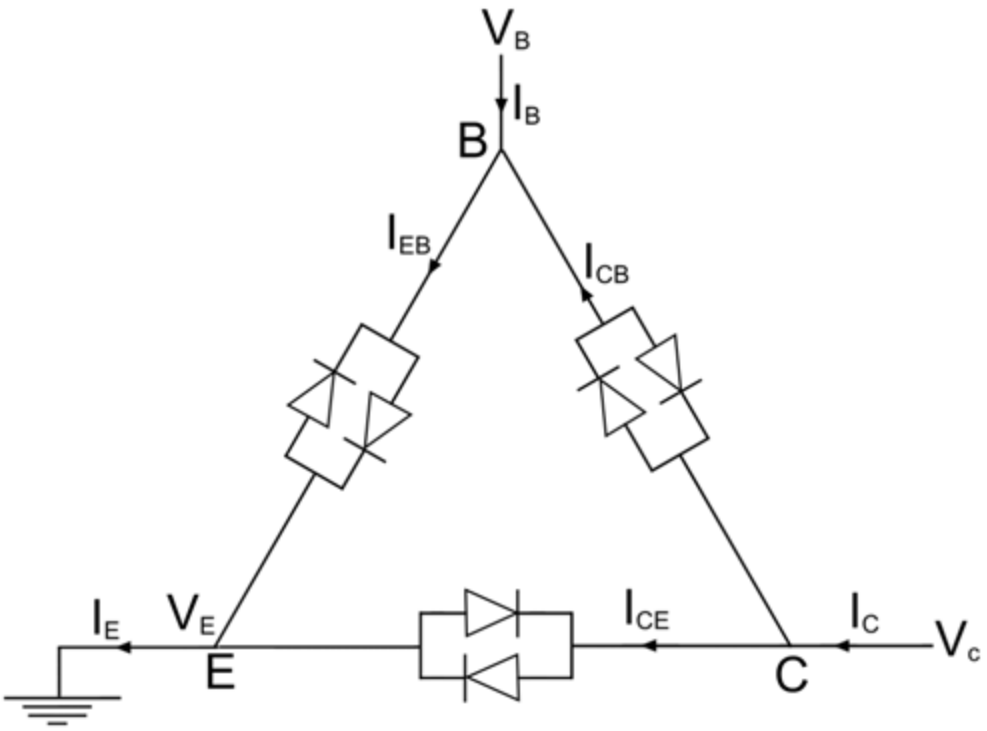


Figure 3.35: *Equivalent circuit model of the CST. The circuit is made of three branches of diode in anti-parallel configuration mounted in a triangular arrangement. C, E, and B are the Collector, Emitter, and Base. The arrows in the branches are the arbitrary direction of current in the branches. I_E, I_C, I_B, I_{CE},I_{CB},I_{EB} are current respectively flowing at the emitter, collector, base, between the Collector-emitter, collector-base, and emitter-base. V_E, V_C and V_B are the voltage respectively at the emitter, collector, and base.*

and

$$I_{CB} = I_{CBs}\left[\exp\left(\frac{eV_{CB}}{\eta k_B T}\right) - \exp\left(\frac{-eV_{CB}}{\eta k_B T}\right)\right]. \tag{3.9}$$

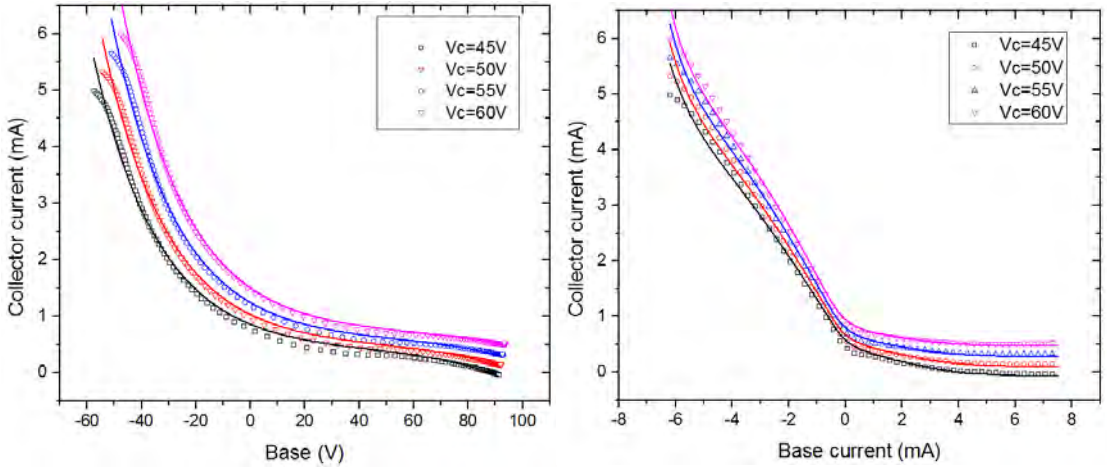
Therefore

$$\begin{aligned} I_C &= I_{CE} + I_{CB} \\ &= I_{CEs}\left[\exp\left(\frac{eV_{CE}}{\eta k_B T}\right) - \exp\left(\frac{-eV_{CE}}{\eta k_B T}\right)\right] + I_{CBs}\left[\exp\left(\frac{eV_{CB}}{\eta k_B T}\right) - \exp\left(\frac{-eV_{CB}}{\eta k_B T}\right)\right] \\ &= I_{CEs}\left[\exp\left(\frac{e(V_C - V_E)}{\eta k_B T}\right) - \exp\left(\frac{-e(V_C - V_E)}{\eta k_B T}\right)\right] \\ &+ I_{CBs}\left[\exp\left(\frac{e(V_C - V_B)}{\eta k_B T}\right) - \exp\left(\frac{-e(V_C - V_B)}{\eta k_B T}\right)\right]. \end{aligned} \tag{3.10}$$

Equation 3.10 describes the current into the collector. I_{CEs} and I_{CBs} are the saturation current of the collector-emitter and the collector-base channels. The transfer characteristic data obtained from the Keithley 4200 SCS gave us a relationship between I_C, I_B,

V_B, V_C at a given temperature, so equation 3.10 could be used to fit the data.

At room temperature, the average resistance between each pair of electrodes measured with a Fluke digital multimeter 15B was 2 MΩ. The series resistance associated to an anti-parallel diode being (12±5%) kΩ can be neglected compared to the resistance between the electrodes. Thus equation 3.10 was used to fit the data and extract key parameters. Around 30 devices were chosen in this case and fitted, as seen in figure 3.36 the fitted model described accurately the experimental data, the device presented here is a sample representative and more plots will be enclosed in the appendix. Figure 3.36b shows only a third of the data points for clarity once the data were fitted. The fitted data obtained from fitting the experimental data of figure 3.36a were used to model the current-current transfer characteristics of figure 3.36b. the value obtained for the collector current was re-used to model the current-current transfer characteristics.



(a) *(b)*

Figure 3.36: *Experimental data and fitted II, IV curves using equation 3.10 for a CST W device at 45, 50,55 and 60 V respectively. (a) current-voltage transfer characteristics with the corresponding fitted plots (solid line). Current-current transfer characteristics with the corresponding fitted plots (solid line).*

V_C (V)	I_{CBs} (μA)	I_{CEs} (μA)	η	Adj. r-quare
45	105± 2	162± 2	779±4	0.99803
50	107 ±3	170± 3	834 ± 6	0.99728
55	108± 3	172± 3	933±7	0.99732
60	118±3	171±3	924± 7	0.99728

Table 3.3: *Results and extracted parameters for fitted current-voltage data of the CST W device presented in figure 3.36 . V_C, I_{CBs}, I_{CEs},η, Adj. r-Squared, are the collector voltage, saturation currents, ideality factor and adjusted r-Squared.*

Table 3.3 shows the extracted parameters for the device fitted in figure 3.36. The adjusted r-square (Adj. r-square) in statistic described how best a theoretical model fit or predict the experimental data. The adj. r-square can take on any value less than

1 with 1 indicating a better fit. The adj. r-squared values in table 3.3 shows a very good fit of the data. Table 3.3 suggest that the saturation currents of a CST W device varies slightly with increasing collector bias voltage in the range 45-60 V. The influence of the transistor channel width on the electrical performance of the transistors were done by printing three CST W of same channel length but different channel width. The channel length of 0.5 mm was chosen as it was the smallest gap that could be reasonably printed without short-circuiting the electrodes. The channel width of o W_1 =452.16 mm, W_2 =923.16 mm,and W_3 =1551.16 mm were used. The width W_1 was initially chosen, the value of W_2 was choose in such a way that it approximately double the width of W_1. W_3 was subsequently chosen to approximately triple the width of W_1. The ideality factors in table 3.4 overlap within uncertainties, for this model at room temperature. This suggests that the increase in CST width at room temperature does not affect the electrical conduction mechanism in the devices. This is further supported by the single value of the activation energy obtained earlier for temperature greater than 200 K.

	V_C (V)	I_{CBs} (nA)	I_{CEs} (nA)	η	Adj. r-square
W_1	35	483 ± 13	485 ± 10	936 ± 11	0.99337
	40	513 ± 15	503 ± 12	971 ± 13	0.99175
	45	496 ± 13	462 ± 10	956 ± 11	0.99425
W_2	35	813 ± 21	372 ± 8	859 ± 11	0.99411
	40	956 ± 27	434 ± 10	935 ± 14	0.99363
	45	1090 ± 29	465 ± 11	981 ± 14	0.99525
W_3	35	1270 ± 29	440 ± 8	861 ± 11	0.99659
	40	1610 ± 39	541 ± 11	981 ± 14	0.99711
	45	1049 ± 23	498 ± 7	913 ± 8	0.99929

Table 3.4: *Results and extracted parameters for fitted current-voltage data of three CST W devices W_1, W_2,W_3 . V_C, I_{CBs}, I_{CEs},η, Adj. r-Square, are the collector voltage, saturation currents, ideality factor and adj R-Square.*

The results show in table 3.4, were characterized at collector biased of 35, 40 and 45 V respectively. This is significantly lower than other value of biased current applied during this work for other type of CST architecture. But this was justified with the fact that, as the channel length increases, the resistivity of the silicon track decreases, and the biasing voltage to obtained the switch was found to decrease as well. It was found that the increases in channel width do decrease the value of the collector voltage needed to switch the devices, but the switching is less pronounced compared to that of the CST J devices to be described in chapter 5. Ideally, for a device with collector-base and collector-emitter of the same dimension, the internal saturation current of these channels should have been the same. However, we observed in table 3.4 that, this is

applicable in the transistor with width W_1 only. The relative changed observed in the saturation currents of the channel for the devices with width W_2 and W_3 were attributed to printing registration [37, 129]. It is known that a slight shift on the registration can induce a change in the electrical parameter of a printed devices[184–188]. The results of table 3.4 show that the saturation current at the electrodes of the CST increases with the increase of the channel's width. For instance, at 45 V, the saturation current I_{CBs} increases from (496±13) to (1049± 23) nA as the channel width changed from 452.16 to 1551.16 mm. The increase of saturation current was in the same direction as the increase of OFF current or leakage current, thus as the channel width increases at ambient temperature, we will experience a higher leakage.

The results suggested that for a wider channel, there are more possibilities for carriers to find lower barriers, thus the ideality factor remained in the same range. The devices with wider channels, such as W_3 were able to carry currents in the order of milliamperes, which is 3 to 4 times higher than the ON current in W_1. One of the conclusions from this architecture is that in order to have a better switching device with low OFF current and smaller leakage, the channel width has to be reduced. However, one of the limitations of printing electronics is the smaller gap that could be printed with this design. To improve the switching, other transistors architecture with shorter channels were investigated and will be presented in the upcoming chapter.

Chapter 4

Gate logic with the CST

Whilst the electronics revolution in the 1950s brought about the vast improvements in the field of computing such as the increase in computing power, improved ability to use ICs, and developments in microprocessor systems, equipment and appliances, it is worth noting that such tremendous progress owes its success to developments made in transistors and switches in general. Transistors are an essential building block for gate logic [189], and therefore play a key role in the computing industries. However, the physical limitations of conventional materials used for the fabrication of transistors are being reached [39, 40]. This key research on transistors is no longer focused only on the size reduction of an individual transistor, but also on novel approaches to transistor fabrication. For the past 20 years, an increasing number of researchers have been trying to redefine or produce logic gates for various types of applications, including flexible electronics [190–192], molecular electronics [193–195], organic electronics [196–199] and stretchable electronics [200].

Within this realm of rigorous gate-logic innovation, this chapter focuses on the actual logic gate fabrication using the CST, starting with a discussion on the fundamentals of logic gate, and the method of constructing logic gate. This is followed by the presentation of logic gates built using CSTs. Finally, the chapter will present the principal results and their operation mechanisms.

4.1 The logic gate

4.1.1 Fundamental of logic gates

Logic gates form the basic fundamental blocks of a computing device, with the ability to perform logic operations using one or more variables as input and return one output

variable. In principle, logic gates can be built from mechanical, hydraulic, chemical, magnetic and electronic systems. However, electronics are the most widely used logic gate, performing Boolean logic using basic switching elements [201]. In binary logic, values are represented by either "0"/"LOW"/"OFF" or "1"/"HIGH"/"ON". The two states are defined in electronic logic by the voltage or current level. In a current level, for instance, the state "1" corresponds to when the current is flowing through a terminal and "0" otherwise for positive logic. In negative logic, the high states correspond to "0" and the low state corresponds to "1". The fundamental gates "NOT", "AND" and "OR" can be used to build more complex logic operations [42].

The NOT gate, as shown in figure 4.1 performs a Boolean operation, such that the output signal in figure 4.1a is always opposite to the input signal. Figures 4.1b and 4.1c show the truth table of a NOT gate and the waveform of a square signal throughout the gate.

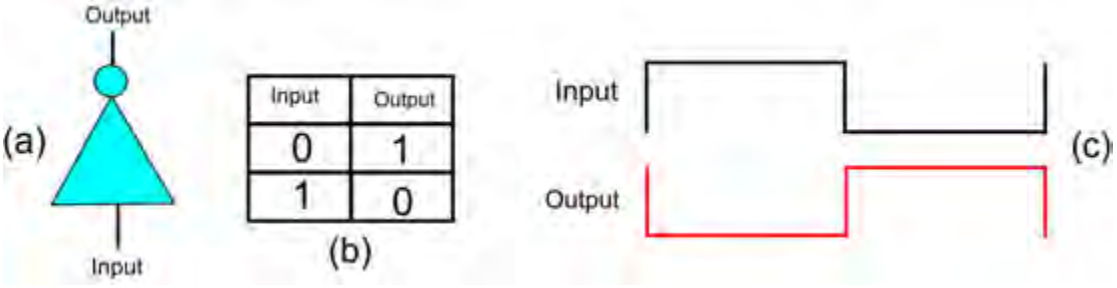


Figure 4.1: *Illustration of NOT logic, (a): Input and output signal (b): Truth table of a NOT gate (c) Waveform signal throughout a NOT gate.*

The AND gate has 2 inputs and a single output as shown in figure 4.2. For a two-input signal, the voltage level of an AND gate is shown by its truth table in figure 4.2b. For the two input waveforms in figure 4.2c, the output waveform is presented. As a rule, the AND produces a high output signal when the two input signals are high, otherwise, it produces a low signal.

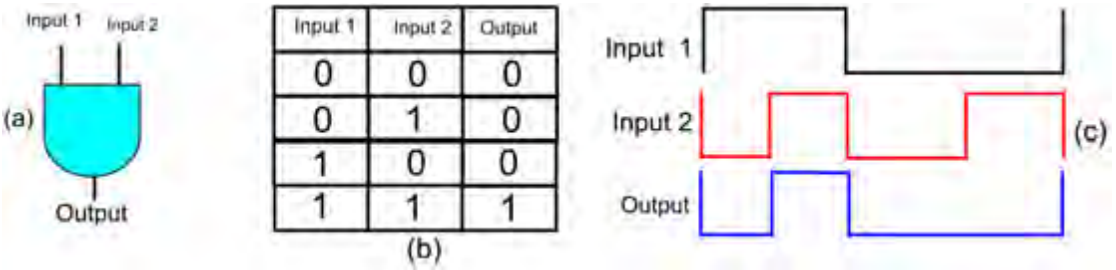


Figure 4.2: *Illustration of AND logic, (a): AND block with two inputs and one output (b): Truth table of AND gate, (c) inputs and ouput waveform for the AND gate.*

Another fundamental gate logic OR is shown in figure 4.3. The OR gate, like the AND, has two inputs and a single output. However, the output signal of the OR gate is low

when the two inputs are low, and high if one or both of the inputs is high. The truth table summarizing the operation of OR gate is presented in figure 4.3 (b), and the behavior of a square signal waveform through the OR gate is also presented in figure 4.3 (c).

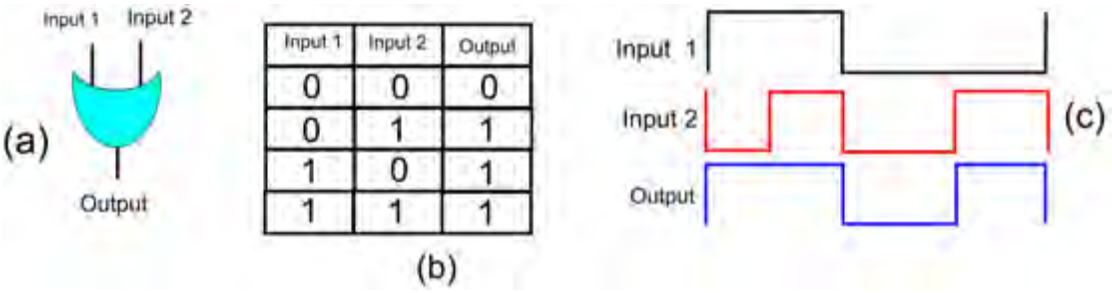


Figure 4.3: *Illustration of OR logic, (a): OR block with two inputs and one output (b): Truth table of a OR gate, (c)input and ouput waveforms signal in an OR gate.*

4.1.2 Logic families

A logic family is a group of logic gates that use similar types of switches as their building blocks. The first category of gate introduced in the 1930s is diode logic (DL) also known as the resistor-diode-logic (RDL), built by a combination of diodes and resistors [202, 203]. RDL cannot perform an inversion, therefore the number of logic gates which can be built from this class is very limited, and thus pure RDL has not found much application in digital electronics. Resistor-transistor logic (RTL), is another family of logic gates that was used in earlier computing. RTL gates are built from a combination of BJTs and resistors. The RTL gates allowed the construction of an inverter in the 1950s, offering a wider range of gate construction compared to RTL.

Diode-Transistor Logic (DTL) is a family of gates that emerged by using both diodes and transistors in the same gate logic. Transistor-Transistor Logic (TTL), quickly superseded the DTL and RTL families from the 1960s. A TTL gate is built from BJTs and resistors [204, 205], it is used in various domains within the computing industry, and equipment drives. The TTL are limited in high-frequency applications, due to minority carrier operation of BJTs.

The most widely used family of gate logic is the CMOS family, in which complementary FETs (NMOS, PMOS) are arranged to build logic gates [42, 206]. The CMOS family presents several advantages over previous families, including their size [207, 208], the low power consumption, the possibility to be powered at different voltages [209, 210], and the ease of mass manufacturing [211]. Nevertheless, besides the conventional families of gates cited above, researchers are constantly introducing novel families of gate base on new device configurations and novel materials. These novel families include

resonant-tunneling-diode (RTD) [212, 213], differential current switch logic (DCSL)[214], carbon nanotube (CNTFETs) logic [215, 216], high-performance fast feedthrough logic (FTL)[217], and current injection logic (CIL) [218]

4.1.3 Logic gate fabrication

As mentioned earlier, logic gates are principally built from switches and resistors. The methods and processes used to produce transistors are therefore also used for the production of logic gates. The method used to produce logic gates is related to the type of application in which the device is going to be used. In the case of flexible and stretchable technology, printing methods can be used, but for conventional application in the computer industry, photolithographic methods are generally used.

4.2 Experimental method

4.2.1 Production of printed logic gate

The CSTs presented in this thesis were used as building blocks for logic gates using their switching capability. In earlier results, we established that the n-type and p-type CST transistors present similar electrical characteristics [37, 48], and therefore electrical properties could be fully predicted from architecture. For this study, we used the symmetric CST model, shown in figure 4.4 as the building block. Its channel width and length are equal to $L \approx W \approx 0.8$ mm.

Figure 4.4: *CST architecture used as switching block for the logic gate fabrication.*

The transistors used here were produced using the standard printing process described in chapter 3. The conducting electrodes were printed from Dupont LuxPrint 5000 Silver

ink, and the active layers were printed with semiconducting inks made from highly doped p-type silicon with a nominal resistivity of $\rho < 0.0001$ Ωm at room temperature. All the transistors used as building blocks for the logic gate were printed on plain 80 g/m^2 white paper. The gate properties were obtained by characterizing individual transistors or many transistors connected with highly conductive low resistance copper wire. The wire resistance was negligible compared to the resistance of the transistors OFF circuit, therefore, not contributing to the properties of the logic gate.

4.2.2 The electrical characterization of CST based logic gates

During this study, several types of logic gates were built from CST transistors and more than a hundred of them were characterized. The logic gate characterization was carried out at various steps. From the batch of transistors produced, individual transistors were chosen at random and characterized with a semiconductor parameter analyzer Keithley 4200 SCS. This operation was repeated several times with various collector bias voltages, to ensure there are no signs of failure in the chosen transistors. One of the biggest inconveniences of printing electronics is that there is a significant variation in electrical characteristics of the devices produced [184–188]. Therefore, for logic gate fabrication, transistors whose electrical performance was in a very tight electrical range were selected. For instance, the resistance of the channels for the devices used in this experiment was not different by 10% of their value.

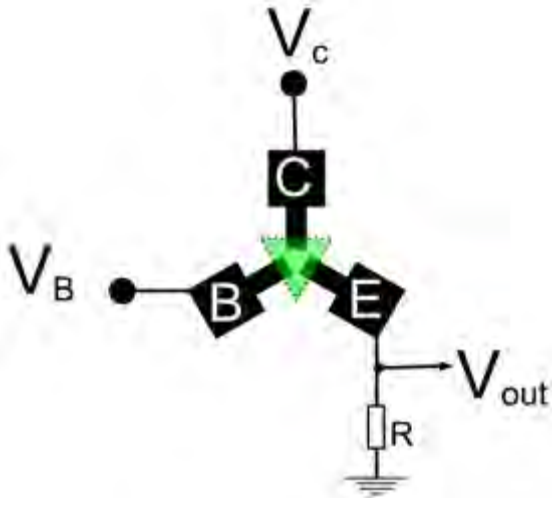


Figure 4.5: *Shematic of a CST characterization for logic gate application, R is a resistor.*

The logic gate electrical characterization was performed using the circuit diagram presented in figure 4.6 and 4.7. This was carried out with a testing station featuring various electrical current/voltage sources and measurement systems, introduced in chapter 3. For this characterization, the operation voltage +V was always kept on, the voltages

in the bases were attributed various values and the output voltage was monitored for their output using a Fluke 111 digital multimeter. The characterization was performed at ambient temperature under DC current/voltage. Figure 4.5 shows a schematic of a single CST under test, different voltage levels are sourced to V_C and V_B and the output is used to check the working operation and condition of the device prior to their use in the logic block. As the devices used are symmetric devices, the electrodes can be interchanged for any desired application [37]. Currents and voltages were supplied to the circuit by 4 independent ISO-TECH IPS601A power supplies and a Topward 6303 DS Dual Tracking DC power supply. The current and voltage were monitored using a Keithley 2000 digital multimeter with operating range between 0.1 μ to 1000 V and 10 nA to 3A for voltage and current respectively in DC operation. A FLUKE 111 digital multimeter and a Tektronix TDS2000 digital oscilloscope were also used to measure the current and voltage.

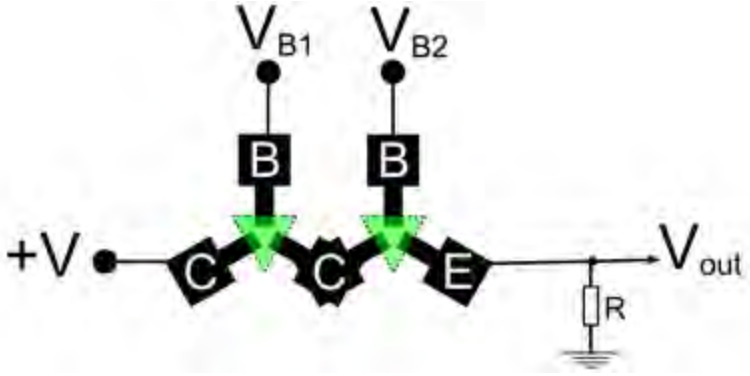


Figure 4.6: *Schematic of a CST based logic gate , with two transistors connected by their collector and emitter. A load resistance R is connected between the ground and the output signal.*

The transistors were mounted in several configurations, but only two are presented here, shown in figures 4.6 and 4.7. Figure 4.6 shows the CSTs in a series configuration, the operation voltage $+V$ is at the collector of the first transistor and the system is grounded by the second emitter through a resistor R. In this configuration, one collector and emitter are joined together; the input voltages (V_{B1},V_{B2}) are connected to the two base terminals and the output voltage is probe from the second emitter. The set up shown in figure 4.7, is the parallel configuration of CSTs, with one emitter-collector joined and connected to the operation voltage $+V$. The other emitter, collector are connected in common and grounded through the resistor R, the voltages are still sources on V_{B1} and V_{B2}. The applied voltages are sourced on their base terminal. The voltage $+V$ is set to be above the switching threshold voltage of an individual transistor. The output voltages V_{out} were monitored and recorded for further analysis of the characterization.

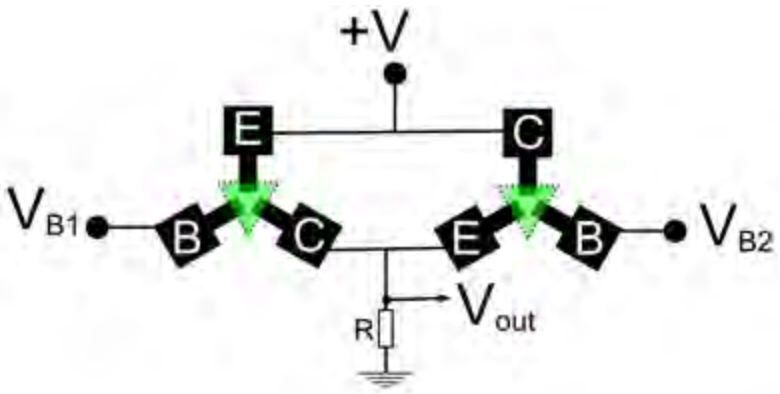


Figure 4.7: *Schematic of a logic gate based CST, with two transistors connected by their emitter-collector terminals and load resistance R.*

4.3 Results and discussion

The following subsections will discuss the results and the performance of the logic gate built during this work; the table of input and output voltages using the configuration of figures 4.6, and 4.7, truth tables of OR and AND boolean logic operation using the CSTs will also be discussed. For statistical purposes, it is important to note that the few sample results presented here are representative of the results obtained.

4.3.1 Single transistor in a logic block

The first step toward the building of a logic gate is to have a good switch, and one of the most important features in complex circuits, is to be able to characterize a single component or circuit parts individually in order to make default and failure characterization easier [219–223]. The transistor electrodes could be changed without changes in the transfer characteristics; this provides a significant advantage over other transistors which can be wired only in a dedicated way.

The transfer characteristics in figure 4.8 illustrates the collector current dependence on the base voltage at given biased collector voltages, for a transistor characterized individually in a block of two transistors connected in series. The few scattered data points observed at the starting of the plots, seen during the characterization were attributed to an artifact of the measurement when the Keithley 4200 SCS start its operation. This assumption was supported by the fact that, similarly scattered data were observed for the same devices even when the range of the current applied during the characterization changed.

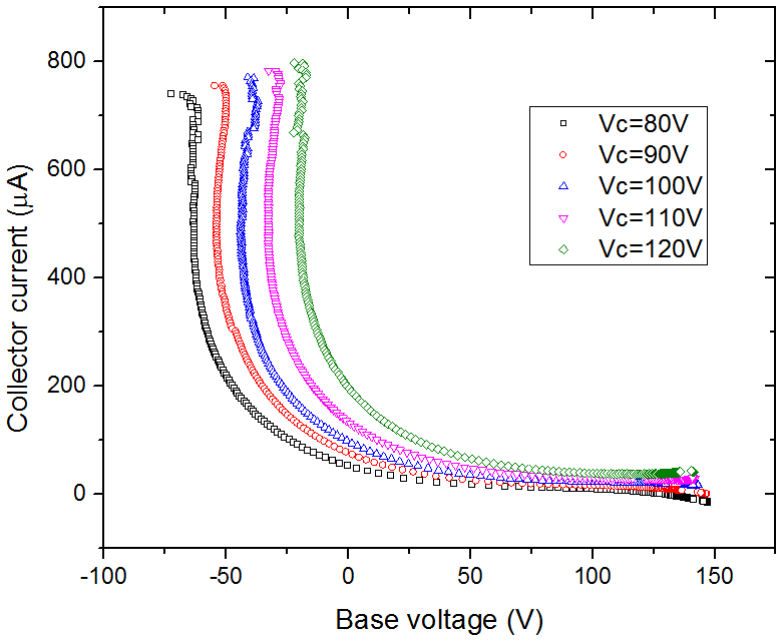


Figure 4.8: *Current-voltage transfer characteristics of a CST JT device characterized at biased collector voltage of 80, 90, 100, 110 and 120 V.*

4.3.2 Combination of CSTs as an AND gate

The possibility of using electronic switches in everyday applications such as ICs, chips, RFIDs, depends largely on their ability to build logic gates and perform logic operations [224–227]. The logic gates were characterized using voltage level as a reference for the devices being ON or OFF. Positive voltage logic was used, meaning that the high voltage was attributed to the logic "1" and the low voltage to the logic "0". Several works on logic gates explicitly demonstrate that there is no single standard method to determine the "OFF" and"ON" state of a device [224, 225, 228–230]. Therefore, for any given study, the high and low state of a device first needs to be defined.

Earlier, we demonstrated that the region where the CST starts presenting very good switching behavior were for base-collector voltage beyond 60 V for the CST JT architecture model. So we will consider the output voltage to the"OFF" or "0" when its value is less than half of the input signal and below 65 V. The output voltage will be "ON" or "1" otherwise.

The layout shown in the schematic diagram of figure 4.6, was used for the results presented here, a driving voltage greater than 100 V was connected to $+V$ through a load resistance of 1.5 MΩ for safety reasons. The output voltage V_{out} was recorded with the multimeter Keithley 2000 in their operation as voltmeter. During the characterization both the voltage and the current at each terminal were recorded. A sample representative of the results obtained is presented in figure 4.9.

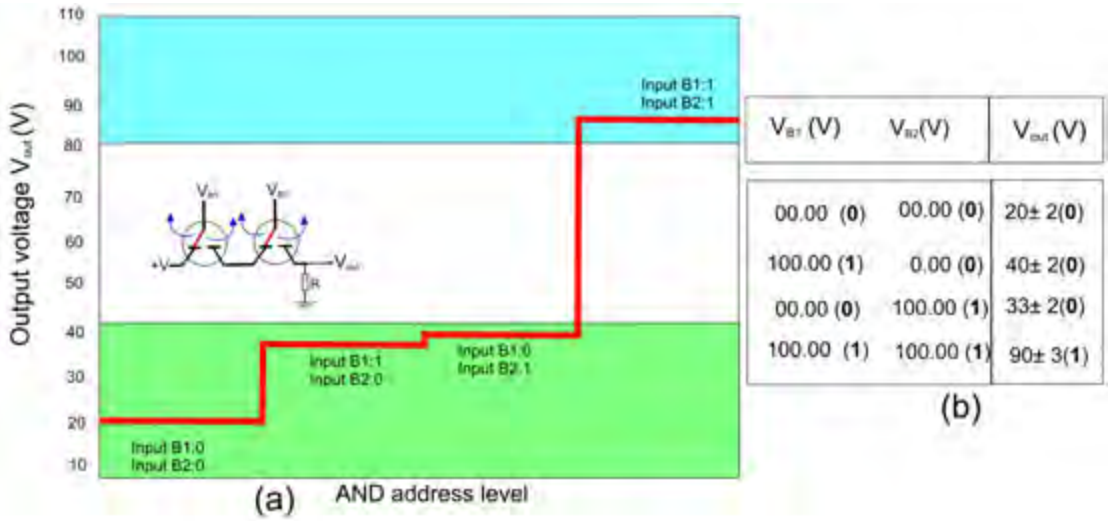


Figure 4.9: *Demonstration of "AND" gate logic circuit base on CST transistors. This gate is formed by combining two transistors in series (left insert). (a) The address level is plotted against the output voltage for the combination (0;0), (0;1),(1;0),(1;1).(b) shows the truth table for the various combination (0;0), (0;1),(1;0),(1;1) expressing a AND gate logic.*

One of the significant results of this work was being able to combine the printed transistors to achieve a boolean logic. Figure 4.9 shows the AND address level with corresponding output voltage level, and the transistors in the setup (inset figure 4.9) could be operated independently. This is a requisite for applications in integrated circuits [230], as it provides the possibility to quickly identify a faulty transistor when the number of transistors increases in the circuit. While keeping the operation voltage $(+V)$ at 100 V we made different combinations of 0.00 V and 100.00 V in the inputs signal, read their output voltage and plotted their different level in the layout schematic in figure 4.9a.

The table of figure 4.9b shows the output voltages for the AND address level, clearly depicting the output voltage higher when the two inputs are high. The green and blue shaded areas represent the logic "0" and logic "1" regions respectively. The mechanism behind the operation of this gate could be explained by the operation mechanism of an individual transistor itself. When the first base input voltage V_{B1} is low or eventually negative, the preferred path for carriers will be between the input B1 and the electrode connected to the operation voltage. When the first input is high enough for instance 100.00 V, the current path will be between the first base and the first emitter. From that stage, the output voltage level will be defined by the second transistor.

The second transistor, while performing a similar operation to the first one, will yield a high output when both inputs are high. The difficulty encountered with this logic gate was the high leakage current. The low output voltage should be as low as 0.00 V, however, in this case, lowest voltages were approximately 20.00 V when the inputs voltages were 0.00 V for AND logic. The relatively high output voltage observed when

the two inputs were low, is linked to the current leakage of individuals transistors. In fact, this demonstrates that the transistor commences conduction as soon as the operation voltage is connected. To reduce the leakage observed in the CST, various approaches were experienced, for instance, silver ink purchased from Creative material was used as electrodes but did not show a significant improvement on the leakage. Devices were also produced on plain thick paper (170 g/m^2), with no significant improvement on the current leakage. Further devices were printed using Thin Conductive Oxide (TCO) as electrodes without noticeable change in the leakage current. However, lowly doped active silicon provided lower leakage current, but does no longer provide cryogenic environment operation below 150 K. The CSTs were successfully operated at cryogenic temperature, although we could not perform variable temperature measurement on the logic gate, due to the narrow space (13 $\times$13 cm^2)inside the cryogenic chamber, it is reasonable to think that these logic gates will also operate at cryogenic temperature [37]. The type of connection between the active layer and the metallic electrode may also be a reasonable way to reduce the leakage and improve on the logic gate electrical performance.

4.3.3 Combination of CSTs for OR logic gate

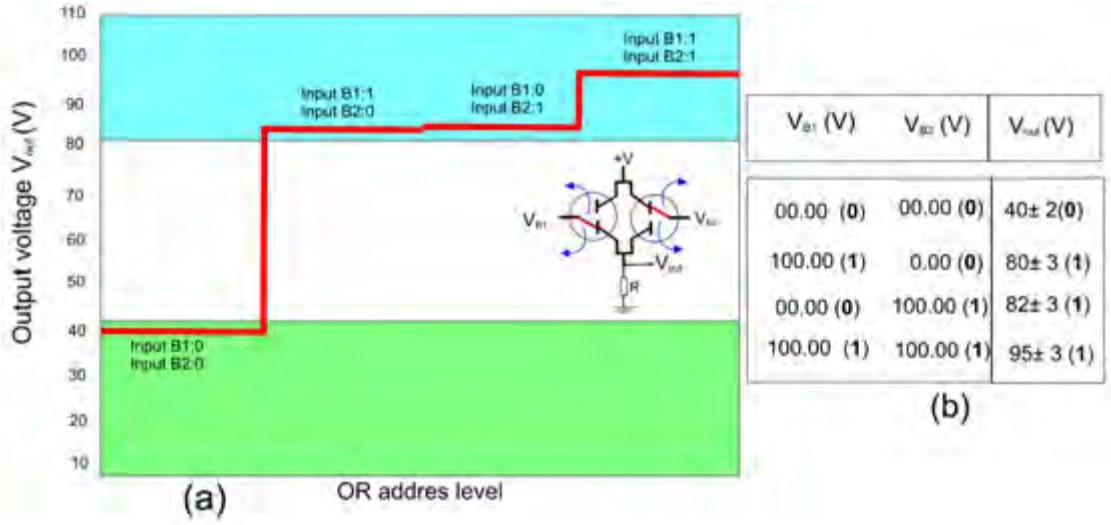


Figure 4.10: *Demonstration of "OR" gate logic circuit base on CST. This gate is formed by combining two transistors in parallel (right insert). (a) The address level is plotted against the output voltage V_{out} for the combination (0;0), (0;1),(1;0),(1;1).(b) shows the truth table for the various combination (0;0), (0;1),(1;0),(1;1) expressing a OR gate logic.*

Using the combination of two transistors in parallel, we successfully built a gate capable of performing OR in positive boolean logic. The inset in figure 4.10b shows the OR gate logic configuration. The equipment used for the OR-gate characterization was similar to the one used for the AND-gate. Figure 4.10a shows the OR address level against the gate output voltage; clearly showing the high output value whenever one of the

outputs is high. This was predicted by the transfer characteristics of a single transistor, as it possesses the ability to change the current path from one terminal to another when the appropriate voltage is applied to the third terminal. Figure 4.10b shows the corresponding truth table. As mentioned before, the leakage current is still high, hence the significant output voltage when the inputs are both low. The ability to build logic gates with screen printing method on paper is the first step toward large area production. The reduction of leakage current, as well as the construction of a much more complex gate logic, will be possible work to cover in the future. It has been demonstrated in this thesis that a single CST could be modeled, using a triangle of varistors that could be further modeled by a triangle of diodes in an anti-parallel configuration. From that point of view, the logic gates built here could be classified as resistor-diode logic gate. Due to the fact that p and n-typed printed CSTs transistors showed similar operation mechanisms and electrical behavior, our attempt to build an inverter has so far not been successful. During this work, the CST was established to be operating properly from above room temperature down to 10 K, individual devices present lower leakage at low temperature, therefore in the hypothesis where the logic gate could operate at cryogenic temperature, the logic gates may present lower leakage at that temperature.

The current chapter successfully demonstrated the CST to build a logic gate. To extend this result to its potential operation in logic at cryogenic temperature the following chapter will discuss the results of individual devices in operation at variable temperature. In the following chapter, the reliability of the CSTs will also be investigated during an extensive current bias.

Chapter 5

Transistor performance

In the electronics industry, devices are usually classified in terms of their electrical characteristics [231, 232]. Base on the device's performance, one could determine the device's mode and range of application. According to the IEEE Standard Test Methods for transistors characterization [233], the performance of a transistor can be evaluated from the information such as the transistor dimensions ON/OFF ratio, saturation current, and temperature dependence.

We previously introduced a model of the current switching transistor (CST) working as a two-way current switch [37, 48]. The main parameters that enable us to understand the CST and its mode of operation were presented and the parameters extracted using a least-squares fitting of the data.

In this chapter, the performance of symmetric and asymmetric CSTs is presented, when the switching behaviour is investigated, including a study of the CST's switching speed. Additionally, an analysis of the CST's behaviour as the temperature varies from 340 to 10 K is also presented and the subsequent impact of low temperature on the devices. The electrical reliability of the CST subjected to a constant current/voltage bias will also be investigated. The experimental set up described in chapter 3 will be used in this chapter to characterized the devices, but when needed specific information on the set up as well as measurement condition will be recalled from chapter 3.

5.1 Bias stress stability of the CST

The electrical behaviour of an electronic device usually deteriorates under application of a constant voltage/current at one of its terminals for a long period of time. In many cases for transistors, current stress can cause the saturation of a terminal or ionization

[234–236], resulting in the permanent damage to the transistor. A good transistor should be stable under constant bias stress. Hence, for this work the stability of the transistors under a constant bias stress was studied. The transistors used for this study were printed on plain paper, with a symmetric architecture (design JT). The electrodes were printed with silver, and the active layer was made of p-doped silicon. The current bias stability tests were performed using the Keithley 4200 SCS. The transistor under test was first connected as a three terminal device, and characterized with a bias collector voltage of 100 V, with the emitter grounded while sweeping a current from -750 to 750 μA at a step of 5 μA in the base. Then, the collector voltage was disconnected from the circuit, and a constant current of 75 μA corresponding approximately to 52 V, is applied from the source measurement unit to the base terminal for a period ranging from few minutes to 6 hours. In between biasing, current-current and current-voltage characteristics were measured at different time intervals.

5.2 Results

The following subsections present the CST performance related results: namely the II and IV transfer characteristics; the switching speed; the response to a constant current bias stress; and the temperature dependence.

5.2.1 Current-voltage characterization

Figure 5.1 shows three current-current transfer characteristics of the asymmetric CST design J (figure 3.4). The electrodes of the devices in figures 5.1a and 5.1b were printed with Dupont 5000 silver ink, while the active layers were made of p and n-silicon ink respectively. The device in figure 5.1c, has the same structure as the others, however, the electrodes here were printed with Dupont 7162 translucent conductive oxide (TCO). The transfer characteristics were obtained using the Keithley 4200 SCS. During the characterization, the emitter electrodes were grounded, while the collector voltage was stepped by 10 V from 80 to 120 V. For a constant collector voltage, the base current was swept from -100 μ to 100 μA in steps of 1 μA. When a negative voltage or current is applied to the base terminal, the current on the collector decreases progressively, with a slope of approximately -1 for all the current-current characteristics presented. When the current applied to the base voltage become positive, the characteristic dramatically changes the slope and the current in the collector stop decreasing. Thus the second region of the graph tends to a low constant collector current, which is an indication of a very good switching behavior, particularly when compared to the interdigitated design CST W transistors presented in chapter 3, which show higher OFF currents.

The analysis of the switching behavior of both the CST W and the CST J suggested that the overall low resistivity of the CST W track compared to the latter, decreased the collector biased current required to switch the devices, but also increased the leakage current. Further confirmation of this assumption was made since the devices produced with lowly doped milled silicon has lower leakage current compared to their highly doped counterpart. The increased in conductivity in the active layer also induced an increase of leakage current.

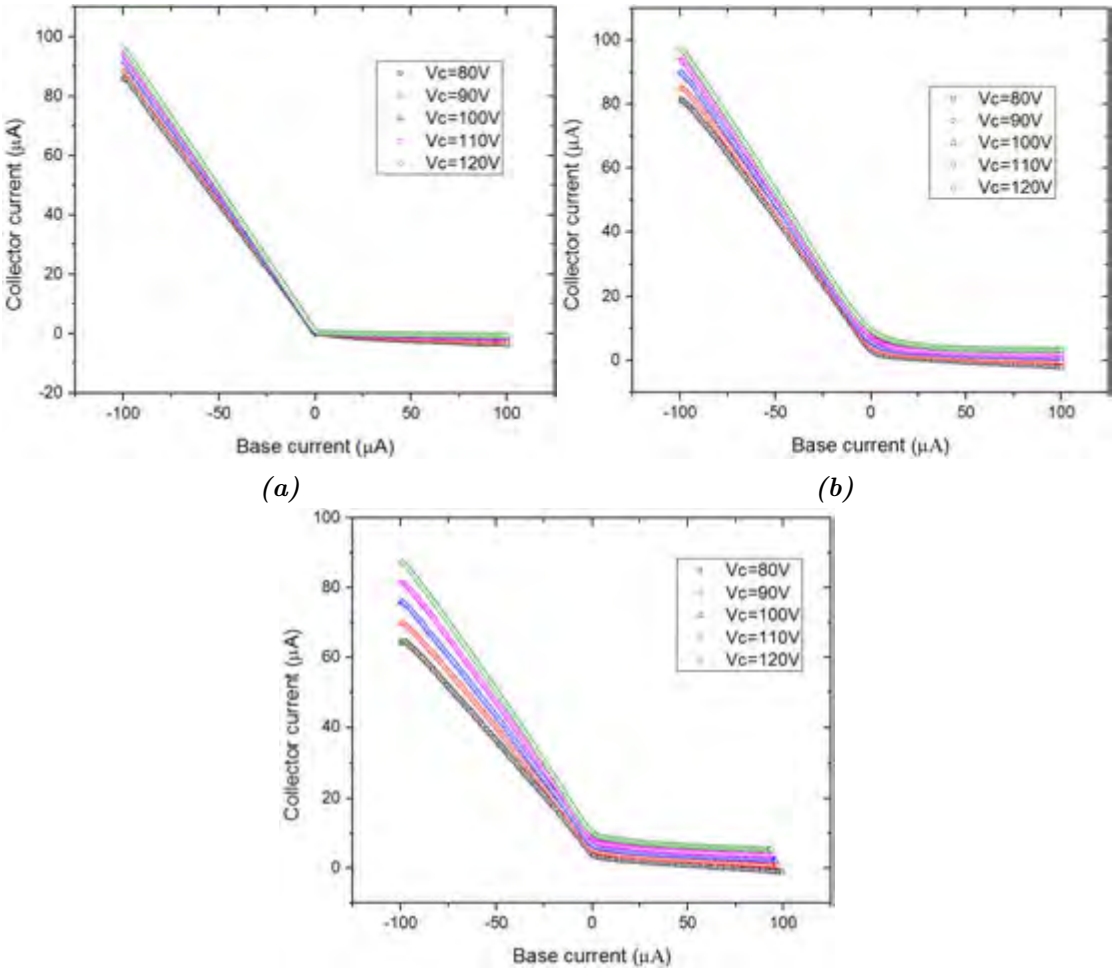
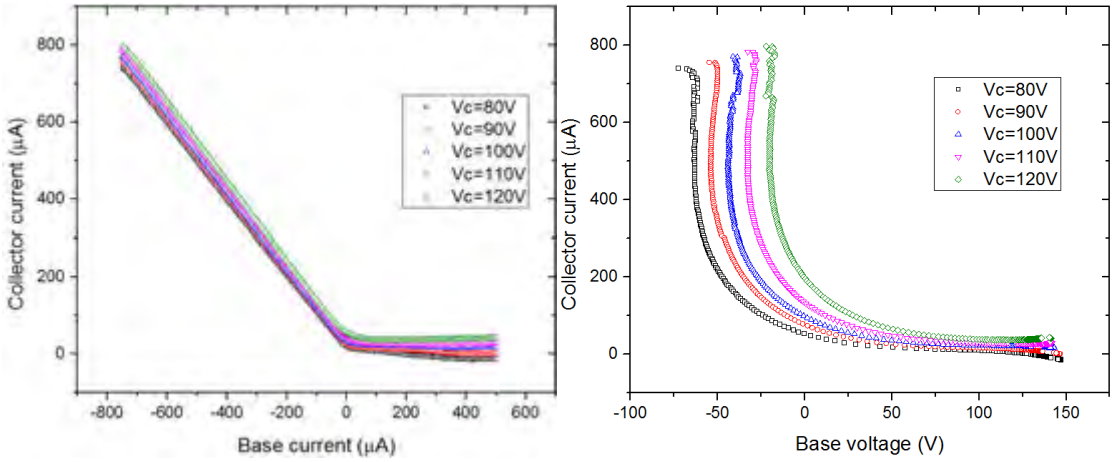


Figure 5.1: *Current-current transfer characteristic for 3 asymmetric CST J devices. The curves were all at 80,90,100, 110 and 120 V respectively. (a) is made of an active layer of n-silicon printed on silver electrodes (b) is made of an active layer of p-Si printed on silver electrodes. (c) Is made of active p-Si printed on Thin Conductive Oxide (TCO) electrodes.*

The transfer characteristics in figures 5.1a and 5.1b, describe the dependence of collector current as a function of base voltage, for the same type of transistor employing n-silicon and p-silicon as their active layers respectively. The devices are characterized for the same range of collector voltage and under the same ambient conditions. We realized that the two devices are sweeping a similar type of current, and their device electrical

characteristics are very similar. In fact, for all the identical devices produced just with differently doped silicon, the results were similar, suggesting that the CST switching operation was not dependent on the type of doping or charge carriers. Based on this observation, it was decided to report for the p-Si only. Figure 5.1a and 5.1c also describe the electrical response of the same architecture of CST J, with the only difference being that the latter was printed with transparent conducting oxide (TCO) electrode instead of silver. By doing so, we emphasize that the switching and general electrical behavior of the devices are not due to the type of electrode, but solely to the active silicon.



(a) *(b)*

Figure 5.2: *II and IV transfer characteristics of a CST JT device JTb1-P09-34C at respective collector biased voltage of 80,90, 100, 110 and 120 V.*

In figure 5.2, current-current and current-voltage characteristics of the symmetric JT design are presented, and these curves were characterized under the same conditions as the one in figure 5.1. All the transfer characteristics of the CST at high voltage present a non-linear behavior with a steep increase of collector current for decreasing negative current or voltage, but without current saturation. This behavior is associated with transistors with non-ohmic contacts at the collector terminal [237]. Although presenting similar switching behavior, the symmetric JT transistors swept a current 8 times higher than the asymmetric J transistors, this is due their difference of channel width. As predicted earlier, devices with wider channels allowed more current to flow. From the IV curves in figure 5.2b, when the base voltage switches from negative to positive, the gradient of the IV curves remains negative, but this gradient tends to zero above a threshold voltage of approximately 30 V. Therefore our transistors perform better as switches when the collector is biased above this voltage.

5.2.2 Device time response

The time response is one of the major factors limiting transistor performance. Here, time response for the type W CST (figure 3.7) model was investigated using the circuit shown in figure 5.3. The base of the device under test was connected to a signal generator providing a square pulse with a V_{PP} =20 V at 5 kHz. The signal was offset with a DC voltage of -50 V. The idea of the offset was to place the transient voltage in the region where the device will change state between ON and OFF. The collector voltage was biased with a positive operating voltage of 50 V, while the emitter was grounded through a resistor load of 1 MΩ. The output resistance value was chosen as to allow suitable reading of the output voltage in the oscilloscope without overshooting, spike or noise. The transient signal was monitored with an oscilloscope through the channel 1 and 2 (see figure 5.3).

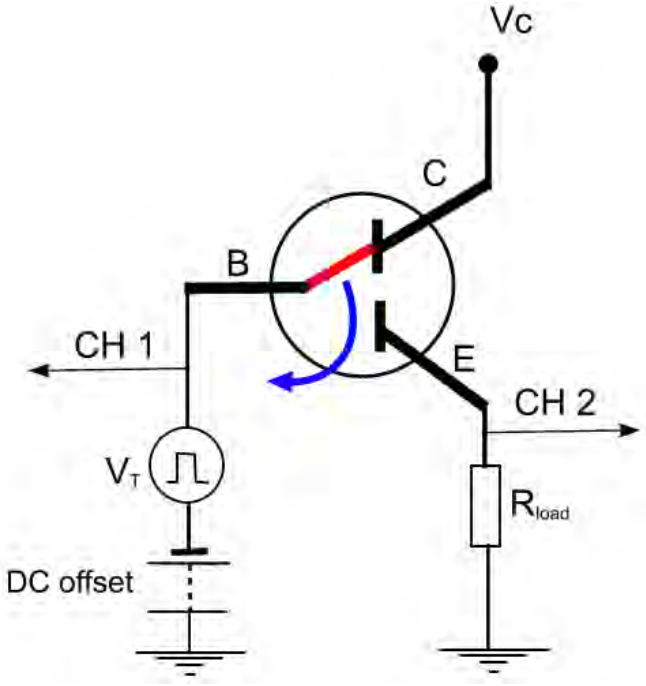


Figure 5.3: *Circuit diagram for time response study. V_T is the transient voltage, R_{load} is the resistance load, CH 1 and 2 are the oscilloscope channels,DC offset is the voltage offsetting the transient signal.*

Figure 5.4 shows the input and output signal for a square signal going through the CST. The diagram of figure 5.4 and the definition of the ON time, OFF time , and switching time described in chapter 2 were used to approximate those values. We obtained approximately 19 μs and 28 μs for the ON and OFF time respectively. Therefore the switching time of the devices obtained was approximately 47 μs. The switching time of the CST was significantly lower compared to the one reported on fully printed organic transistors [238, 239]. The CST lower switching time can be justified by the absence of

dielectric or insulator in their structure that could have lead to significant storage and delay times.

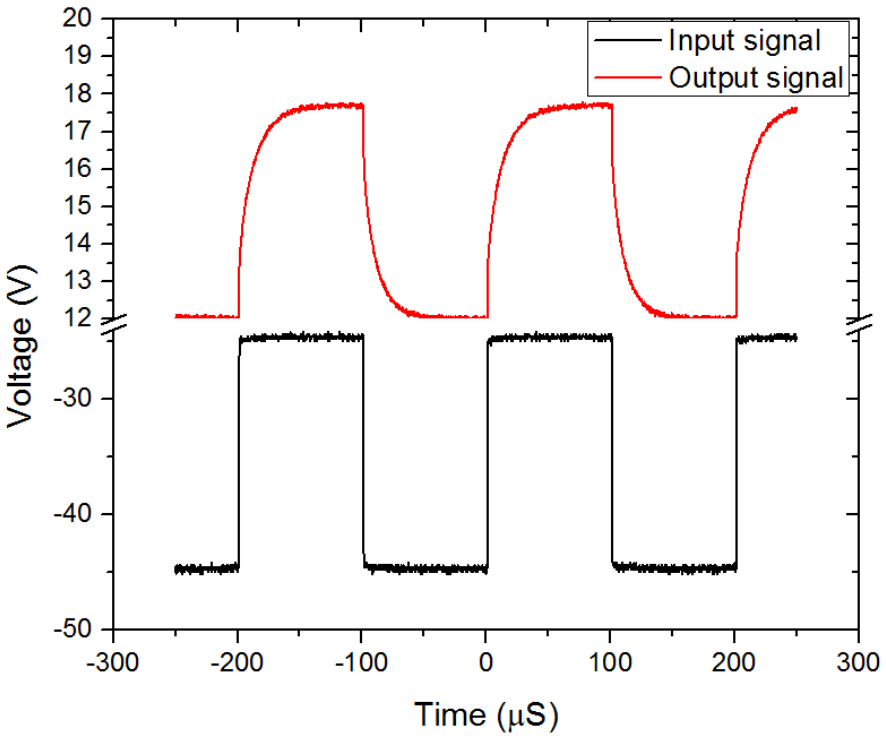
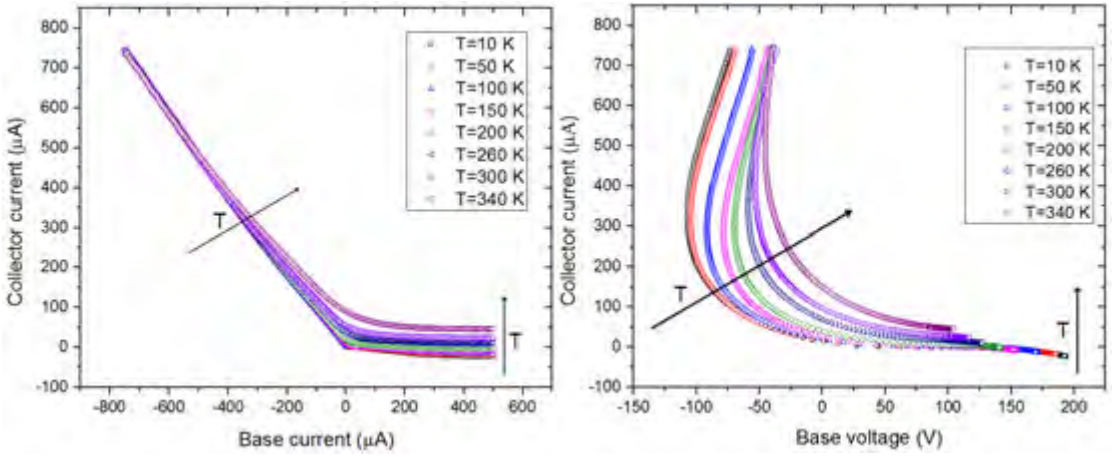


Figure 5.4: *Input and output signals of a 5 kHz square voltage through the CST device. This was characterized using the circuit diagram of figure 5.3*

5.2.3 Effect of temperature on CST characteristics

The temperature dependence of electronic materials is one of the major factors influencing the behaviour of devices and components for applications in which temperature needs to change. The electrical conductance usually decreases when temperature decreases in transistors, leading to an alteration of switching mechanisms at very low temperature [240]. In chapter 3, we showed that for printed layers of both n and p-doped the differential conductance increases with the temperature. This is a property that leads to the uses of this material as temperature sensors [24, 38]. However, it is unclear how this affects the performance of a printed transistor at different temperatures. In this work, we present experimental data for CSTs operating from 340 to 10 K. For practical reasons, especially the limited space in the sample chamber, only the small JT design CST (figure 3.5) was investigated. The devices used here were printed on plain paper with silver electrodes and highly doped p-Silicon active layers. After the production, the devices were stored at room temperature for at least 24 hours prior to temperature dependent characterization.

The CST JT devices were characterized at variable temperatures between 340 to 10 K, and biased at voltages between 60 to 90 V. For the sake of clarity, the transfer characteristics obtained with the collector bias of 90 V will be presented. However, for more clarity and visibility, transfer characteristics for fewer voltages than measured are presented. The decision to report only at a collector bias of 90 V, was not for particular reason because the transfer characteristics for other biased voltage were consistent with the one of 90 V. The transfer characteristics for voltage between 60-80 V characterized at variable temperature could also be found in the appendix.



(a) *(b)*

Figure 5.5: *Electrical transfer characteristics of a CST JT device characterized for the temperature from 340 to 10 K. (a) current-current transfer measured at a collector biased voltage of 90 V. (b) current-voltage characteristics measured at a biased voltage of 90 V. The temperature increases in the direction indicated by the arrows.*

Figure 5.5 shows the current-current and current-voltage characteristics of a printed CST JT model characterized at a collector biased voltage of 90 V and temperature ranging from 340 to 10 K. Figure 5.5a shows that for a given collector bias voltage 90 V in this case, for negative base currents the gradient of I_C versus I_B increases when the temperature decreases. However, for positive base currents, the value of the OFF current decreases when the temperature decreases and even changes sign at very low temperatures (below 50 K). This change of sign indicates that under these conditions, all current is out of the emitter and is sourced from both the base and collector. In figure 5.5b, it is observed, for the given collector voltage, the switching threshold voltage decreases with the temperature.

5.2.4 Transistor under constant bias stress

Figure 5.6 shows the II and IV transfer characteristics of the CST JT over a certain period of time under stress, and characterized at collector voltage bias of 100 V. The

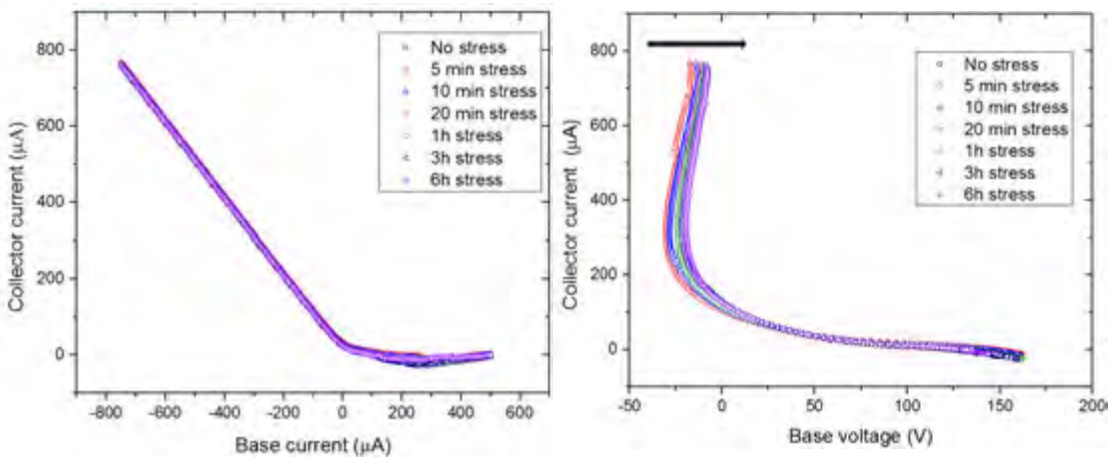


Figure 5.6: *Transfer characteristics of a printed symmetric CST JT device JTa3-3. (a) current-current (b) current-voltage. The device was characterized at room temperature, the curves here represent the characteristics of the same device after a permanent stress of 50 μ A at the base terminal for the respective period of 5 min, 10 min, 20 min, 1 h, 3 h and 6 h. The collector voltage was set at 100 V for all the curves, the II and IV curve without stress is also given for reference. The arrow indicates the direction of transfer characteristics shift.*

results for the collector bias voltage of 100 V presented here was consistent with the one characterized at 90 V. The electrical transfer characteristics for the collector bias voltage of 90 V can be found in the appendix. A constant bias voltage of 52 V was applied to the base for an extended period of times. We recorded that the devices retained their switching capability since their electrical transfer characteristics do not show significant change throughout the stressing period. The current-current transfer characteristic in figure 5.6a shows a set of transfer characteristics for the devices stresses over a six-hour period. It is observed that the current-current characteristics vary little within the period of stress, suggesting a good reliability of the devices stressed for a period of 6 hours. It is observed that for negative current at the base, the collector current response remains almost unchanged during the stressed period. When the transistor operated at its OFF region, minor variation in the OFF-current was observed without systematic change from the non-stressed devices to the 6 hours stressed. We previously reported that the electrical transport mechanism in doped silicon produced by milling was mainly due to the activation of charge transport [24, 38, 48]. The current-voltage transfer characteristics of figure 5.6b shows a shift to the right on the transfer characteristics, this shift was in the same direction as one of the transfer characteristics which was similar to the shift observed in the variable temperature measurement. Therefore, the displacement of the transfer characteristics to the right could be attributed to the self-heating of the devices during a continuous bias. This assumption was confirmed by comparing figures 5.6b and 5.5b, as we observed that the shift occurs in the same direction for instance at

collector biased voltage of 90 V. So we can infer that the current bias for the period of 6 hours does not cause any degradation of the transistors.

5.3 Discussion

In this section, are discuss the results presented in the previous section, and in evaluating the impact of bias stress and temperature on the behavior of transistor a mathematical model based on the equivalent circuit of a triangle of diode pairs, mounted in an anti-parallel construction will be used. The electrical characteristics and switching behavior of the transistors will be described in terms of the physical processes.

5.3.1 CST modeling and switching mechanism.

The CST were produced using different architecture as described in chapter 3. Although different in size and shape the CST showed similar electrical behavior, but only differs in the magnitudes of their electrical parameters [129].

The transistors studied could be modeled using the same approach as described in chapter 3. So far, the CST has been modeled with a triangle containing a pair of diodes, mounted in an anti-parallel configuration [48, 129]. Although that model successfully fitted the experimental data with an excellent agreement, the silicon material was better described with the anti-parallel diode pair connected in series to a resistor (R), the resistor being the sum of the series resistance, equipment resistance, and various metal-semiconductor junctions. For characterization at low temperatures, the model shows in figure 5.7, was used to describe the CST and extract parameters from data fitting. The resistor (R) in the model is the same for all three branches, because the system is made of the same material, and therefore each branch is similar. At higher temperature the effect of this resistance was negligible.

The current in a pair of anti-parallel diodes connected in series to a resistor was given by:

$$I = I_s \left[\exp\left(\frac{e(V - RI)}{\eta k_B T}\right) - \exp\left(\frac{-e(V - RI)}{\eta k_B T}\right) \right]. \tag{5.1}$$

By simple rearrangement of the equation 5.1 an explicit expression of the voltage in term of the current can be given by:

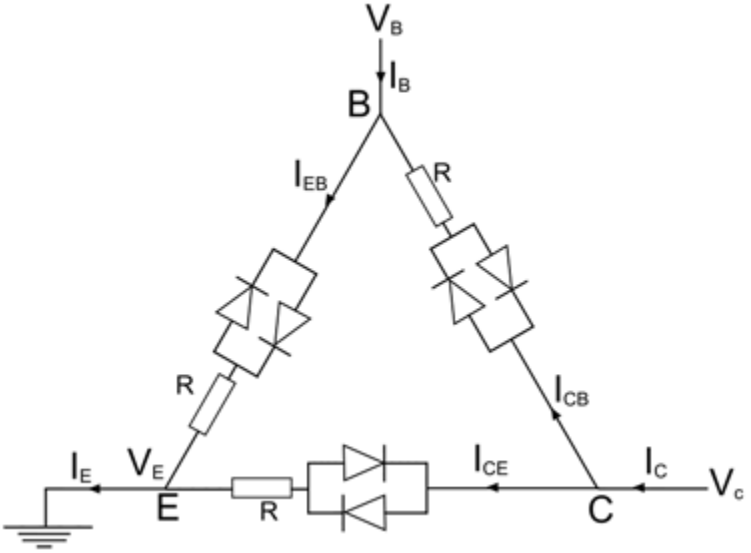


Figure 5.7: *Equivalent circuit modeling of the CST. C, E and B are the collector, emitter and Base. The arrows in the branches are arbitrary direction of current in the branches. I_E, I_C, I_B, I_{CE},I_{CB},I_{EB} are current respectively flowing at the emitter, collector, base, and internal currents. V_E, V_C and V_B are the voltage respectively at the emitter, collector and base. R is a series resistance in each branch.*

$$V = \frac{\eta k_B T}{e} \ln \left| \frac{I}{2I_s} + \sqrt{\left(|\frac{I}{2I_s}|\right)^2 + 1} \right| + IR. \tag{5.2}$$

Therefore by applying equation 5.2 to the model in figure 5.7 we can write :

$$\begin{aligned} V_B &= V_C - V_{CB} \\ V_B &= V_C - \frac{\eta k_B T}{e} \ln \left| \frac{I_{CB}}{2I_{CBs}} + \sqrt{\left(\frac{I_{CB}}{2I_{CBs}}\right)^2 + 1} \right| + I_{CB}R \\ V_B &= V_C - \frac{\eta k_B T}{e} \ln \left| \frac{I_C - I_{CEs}}{2I_{CBs}} + \sqrt{\left(\frac{I_C - I_{CEs}}{2I_{CBs}}\right)^2 + 1} \right| + (I_C - I_{CEs})R, \end{aligned} \tag{5.3}$$

where I_C, I_{CEs}, I_{CBs} are the collector current and internal saturation currents, and V_C and V_B are the collector and base voltages. I_{CB}, I_{EB} are the emitter-base and emitter-collector internal currents respectively. η, k_B, T and e are the ideality factor, the Boltzmann constant, the transistor temperature and the electric charge respectively.

Figure 5.8b shows typical transfer characteristics of a symmetric CST JT used. In the case of this figure, all the data were collected at 295 K, and the experimental data were fitted using the model of equation 5.3. During the fitting, the temperature and collector voltage were kept constant and did not vary. I_{CBs} and I_{CEs} were independent

parameters and allowed to vary. The ideality factor η was an independent variable as well and was allowed to vary during the fitting. The series resistance R associated to the branch was also and independent parameter allowed to vary. The adjusted r-squared values provided in table 5.1 provide information on the quality of the fit for a given collector bias voltage. The solid (red line), represent the best-fitted curves of the experimental data. The extracted parameters from these fits are shown in table 5.1. This model fitted the data with good agreement, and therefore will be used for subsequent fitting at variable temperature.

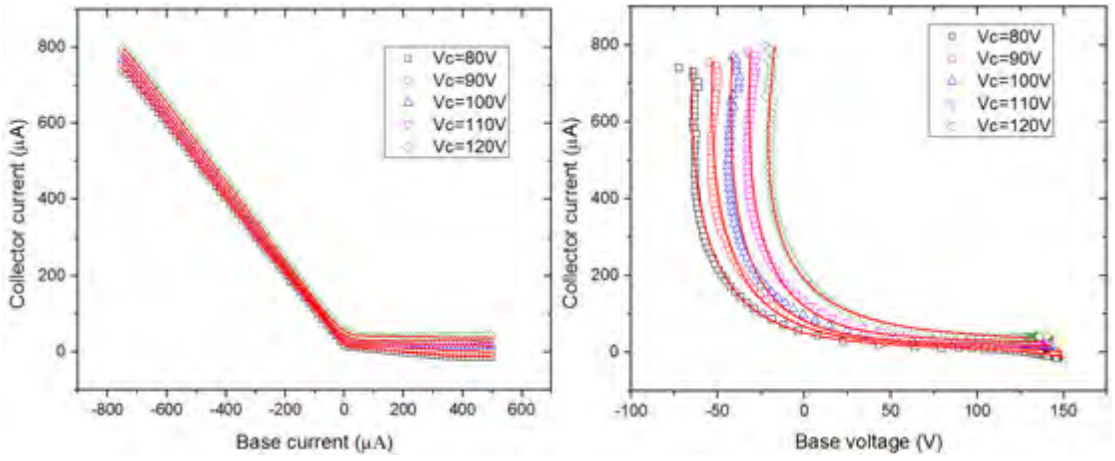


Figure 5.8: *Typical transfer characteristics of a printed symmetric CST JT. (a) current-current (b) current-voltage. The collector voltage was stepped from 80-120 V, the Emitter were grounded and current were swept in the base. The red solid plots are the fitted curved using the model of equation 5.3.*

V_C (V)	I_{CBs} (μ A)	I_{CEs} (μ A)	η	R(kΩ)	Adj. r-squared
80	3.3 ± 0.1	13.8 ± 0.1	1319 ± 15	50 ± 2	0.99912
90	2.7 ± 0.1	18 ± 1	1254 ± 13	48 ± 2	0.99892
100	1.8 ± 0.1	23 ± 1	1161 ± 13	48 ± 2	0.99821
110	1.9 ± 0.2	31.0 ± 0.1	1173 ± 38	49 ± 6	0.98573
120	5.8 ± 0.9	40.2 ± 0.4	1596 ± 96	80 ± 10	0.96648

Table 5.1: *Extracted parameters from fitting transfer characteristics curves of figure 5.8 with the equation 5.3. V_C is the collector voltage, I_{CBs} and I_{CEs} are the collector-base and collector-emitter internal current saturation, η is the ideality factor, R the series resistance and Adj. r-squared the adjusted r-squared.*

From the data analysis the switching mechanisms of the CST was proposed using the model of figure 5.9. In the model of figure 5.9, the CST is represented by a triangle of pairs of anti-parallel diodes. The emitter current is grounded and the collector is placed at a positive voltage. The base voltage can be either positive or negative. When the base voltage is negative, the potential difference between the collector and the base is considerably higher than the potential between the emitter-base, and the preferred path

of the carrier in the path between the base-collector, therefore we observed a current in the collector. This path is shown in red figure 5.9. The equivalent mechanical switch model on the right-hand side of the figure shows the current flowing from the base to the collector. During this process, the devices are ON and passing current.

When the base voltage becomes positive, the preferred path is now between the emitter and base. Therefore there is no current through the collector, and thus the collector electrode is OFF. That path is shown in blue in figure 5.9, and the mechanical switch model on the left-hand side of the figure represent the OFF state of the transistor. Ideally, the current in the collector electrode should be zero. However, in reality, this current is never zero. We realized that the OFF current slightly increases as the collector bias voltage increases, and decreases as the temperature decreases for a given voltage.

Due to the fact that the CST terminals are similar and can play the same role, the CST works as a two-way (double throw) switch, because the current can be switched between two electrodes just by putting the electrodes at different voltages.

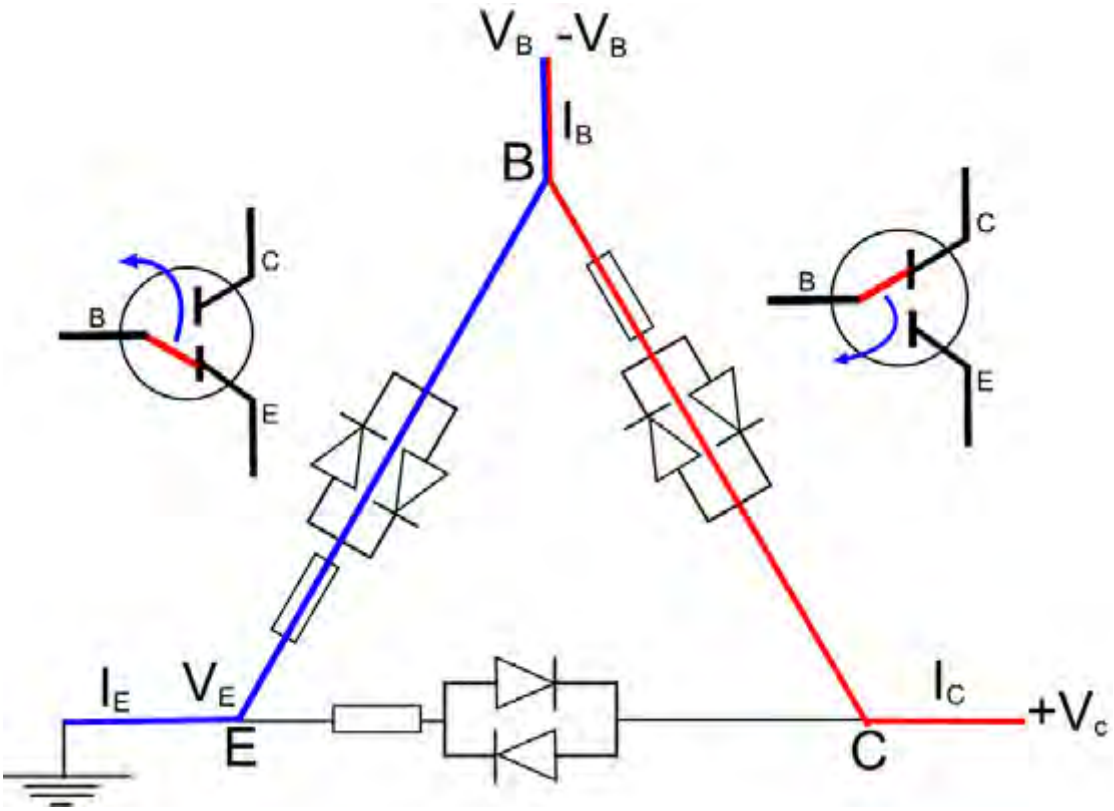
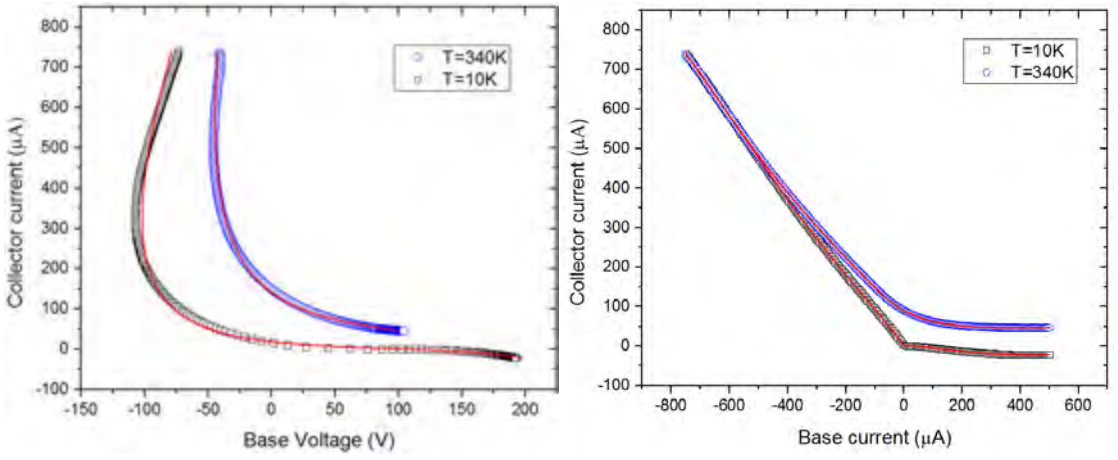


Figure 5.9: *CST switching operation mechanism. The left and right-hand side of the figure shows the mechanical equivalent switch of the transistor as it is OFF (left) and ON (right). The central image shows the path use by carriers when the voltage in the base terminal change from positive to negative. The collector is held at a positive voltage, the emitter grounded, the base can be either positive or negative.*

We would have expected the ideality factor to decreases as the collector bias voltages increase because the carriers have more energy to cross barriers. The saturation current was also expected to increase with increasing collector bias voltages. The values of table 5.1 shows an inconsistent changed on these expectations from 110 V. We believe that this could be caused by the slightly lower value of the adjusted r-squared which suggested that the analytic model does not fit the experimental data at 110, 120 V as well as it does in lower voltages. The series resistance obtained for the biased current from 80-110 V agree within their uncertainty, showing consistent and similar electrical transport mechanism as the bias voltage increases.

5.3.2 Temperature dependence of CST parameters

The transfer characteristics obtained from the characterization of the CST at variable temperature were further investigated in order to provide more explanation on the switching mechanism of the CST. The active layer of this device was p-silicon and printed on plain paper with Dupont 5000 silver electrodes. As seen in figure 5.5, the transistor's electrical characteristics are temperature-dependent, but maintained their overall switching behavior. Hence the experimental data could be fitted with equation 5.3.



(a) *(b)*

Figure 5.10: *Transfer characteristics of a printed symmetric CST JT device JTa3-3, fitted with the analytic model of equation5.3 . (a) Dependence of collector current with the base voltage plotted along with the line of best fit (red solid line)(b) Current-current characteristics plotted with the analytic model. The device was characterized for a range of temperature from 340 to 10 K but only the first and the last plot are shown here.*

Figure 5.10, shows the typical current-current and current-voltage characteristics for the CST JT. The red solid line of figure 5.10a is the line of best fit for the experimental data obtained by non-linear curve fitting. The fitted data of the collector obtained from the plot of 5.10a is plotted along the experimental data of the base current to

obtain the solid red line of figure 5.10b. The analytic model fitted the data well, as the temperature decreases, the lowest adjusted r-squared obtained was 0.99753. The Characteristics presented here, were at a collector bias of 90 V, with the emitter grounded and current swept in the base electrode. For clarity, figure 5.10 only depicts the curves for temperatures 10 and 340 K. Other fitted transfer characteristics are located between these plots as showed in figure 5.5. The fitted curves for the intermediate plot were monotonous and similar to the one presented. The parameters such as the ideality factor, the series resistance, and the internal saturation current were extracted from these fitting and will be further discussed in a form of plots. The transistor was considered to be in OFF state when the current flowing through the collector was lowest. Similarly, the ON state corresponds to the region where the transistor was still conducting, and we chose the ON current to be the highest current sweep by the terminal before the saturation. It was observed that the OFF current decreases with temperature, while the ON current does not change with temperature. The ON/OFF ratio is an important parameter used to define electronic devices. The current ON/OFF ratio define the ratio of the highest to the lowest current that can pass through the device without alteration on its behavior. For this work, at a given temperature, the ON current was considered to be the higher value of the current when the device in ON, and the OFF-current the lowest value of the CST in their OFF state. Analysis of the transfer characteristics at variable temperatures showed that the ON/OFF ratio of the printed switches increases with temperature. The ON/OFF ratio of 10^3 was achieved at temperatures below 150 K, whereas above 300 K the ON/OFF ratio was 10; between 150 and 300 K, the typical ON/OFF ratio was 10^2. The ON/OFF ratio of 10^3 is in the same order of magnitude with fully printed organic transistors in similar substrate [241–244]. Although smaller as compared to the ON/OFF ratio of 10^5 reported on printed transistor using carbon nanotubes as active material [245, 246]. This is actually an acceptable result for non-lithographic fabrication processes [37, 129]. A graphic of figure 5.11 recapitulates these results.

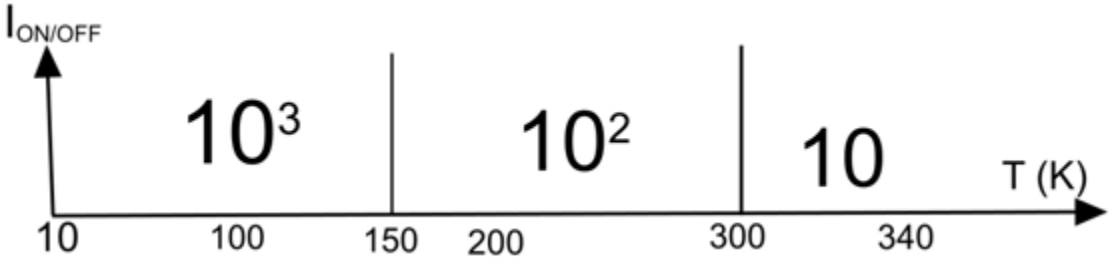


Figure 5.11: *Typical ON/OFF current ratio of printed CST, the results in this figure were obtained with the symmetric transistor CST JT. The schematic shows that the ON/OFF current ratio varies with temperature.*

By fitting the transfer characteristics for all the temperatures and extracting parameters such as the internal reverse saturation current; the ideality factor; the series resistance

associated to a branch and their transconductance, we were able to establish the relationship between those parameters and the temperature. Their subsequent analysis supported the transistor behavior as observed in figures 5.5 and 5.10.

Results from chapter 3 suggested that the active silicon used for this study was thermally activated, presenting principally four activation energy at various range of temperature. We concluded from the analysis of the experimental data and the fitting of parameters that thermionic emission and precisely charged based on the activation of charged carriers was the dominant transport mechanism. The CST was characterized at variable temperatures and the parameters extracted from fitting the experimental data were compared to that of the active material. Namely, the ideality factor of the transistors varies in the same manner as the ideality factor of the active material. This strongly suggests that the CST electrical transport mechanism is similar to the electrical transport observed in the active material, hence the dominant transport mechanism in the CST is based on the activation of charged carriers. The dominant transport mechanism observed here was corroborated by previous studies done on the electrical transport mechanism in a network of percolated nanostructured active silicon [24, 31, 48, 160].

A nanostructured network of particles can be illustrated by the drawing of figure 5.12, where the circle represents a particle or a cluster of particles. A nanostructured network of particles is usually made of interconnected particles and islands which can be connected to the network or completely isolated. A previous study by Jonah *et al* [30, 170] demonstrated that a system of printed nanostructured silicon with a ratio by mass of silicon particle loading greater than 70 % was highly interconnected and could be fairly represented by a system of particles highly interconnected as presented in the schematic of figure 5.12. In the network, any carrier can move from A to B using various trajectories. We will assume that a carrier effectively moves from A to B using the path presented in the schematic of figure 5.12.

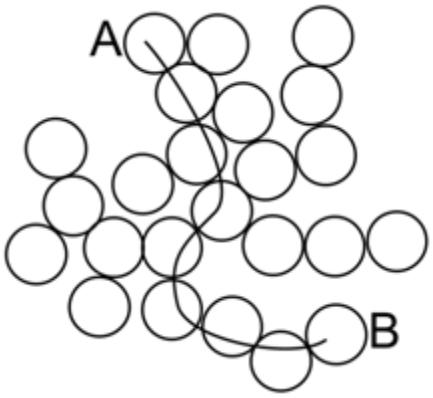


Figure 5.12: *Illustration of a network of nanoparticulate silicon. A and B are two randomly chosen particles. The black line is a random path that a carrier can use to go from A to B.*

When a potential is applied between points A and B in figure 5.12, the carrier will choose an optimal path between the two points. In fact, the charges carriers tend to minimize the energy used in their path to move from an electrode to another. So, while going through the percolated network, the interface at particles or metal semiconductor will act like barriers [247]. The energy required for a carrier to cross those barriers at intersection strongly depends on the barrier height.

Figure 5.13: *Illustration of a random path into a complex network of particles. Barriers are randomly made of different height, width, and shapes. The barrier height is represented by* Φ

Figure 5.13 illustrates random types of barriers representing the complexity of the path that can be followed by a carrier in the active layer of the transistor moving from one electrode to another. For a carrier to cross an interface or barrier of height Φ, it should possess an energy at least equal to that of the barrier, in thermionic emission dominated transport in the hypothesis that tunneling is not a significant mode of transport in the system. The energy drop across an ideal junction is proportional to the Boltzmann factor $\exp(eV/k_BT)$. For multiple barriers, this factor is affected by the ideality factor η. Thus, the probability for a carrier to cross multiple barriers in a percolated network can be written as $\exp(eV/\eta k_BT)$, where η is the ideality factor, seen as the average number of barriers crossed by the carrier during its path in the network.

Figure 5.14 shows the dependence of the ideality factor and the internal series conductance between a pair of electrodes with temperature. The ideality factor plotted on figure 5.14a were extracted parameter from the best fit of the experimental data of the CST JT device presented in figure 5.5. The inverse of the series resistance extracted from that fit was plotted in figure 5.14b

Figure 5.14 clearly shows that the ideality factor, like the conductance or the series resistance, has a non-linear progression with temperature. For instance, the plot of figure 5.14a were fitted with an exponential function in the form of $A\exp(B/T)$, the fit agrees with the data and shows and adjusted r-squared of 0.998. This result suggest that the ideality factor increases in an exponential form with decreasing temperature. The ideality factor increases by a factor of approximately 35 between 340 to 10 K. It was demonstrated in earlier chapter that, the values of the activation energy were (3.38 ± 0.51) meV, (16.80± 1.43) meV, (35.24 ±1.78) meV, and (75.05 ± 2.19) meV for

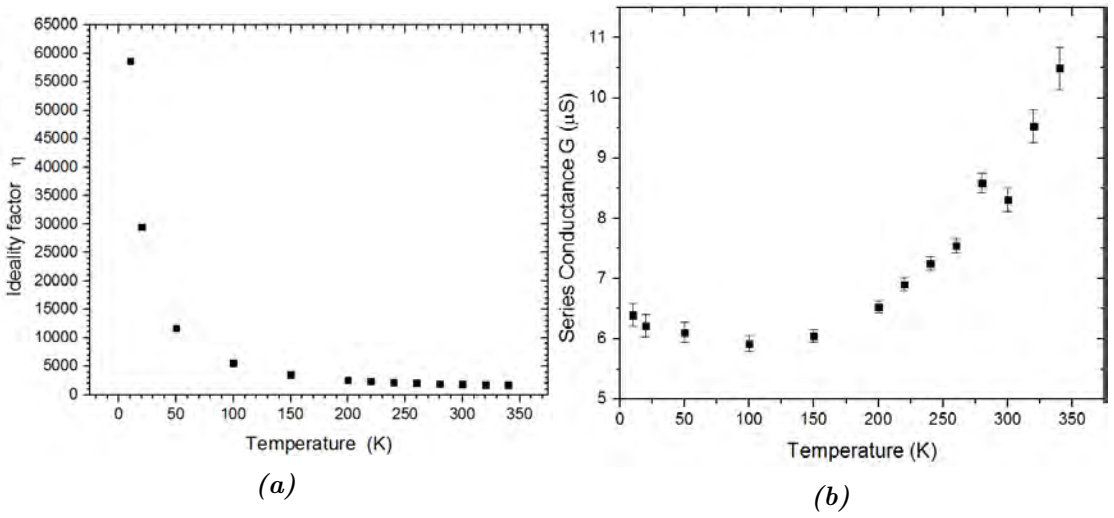


Figure 5.14: *(a) Dependence of ideality factor (η) with temperature(T). (b) Dependence of series conductance ($G = 1/R$) of a pair of electrodes with temperature (T) . The ideality factor and the internal resistance were obtained from fitting data in the extended temperature range of 340-10 K, for the collector voltage of V_C =90 V. The internal series conductance is plotted with the error bars on their value.*

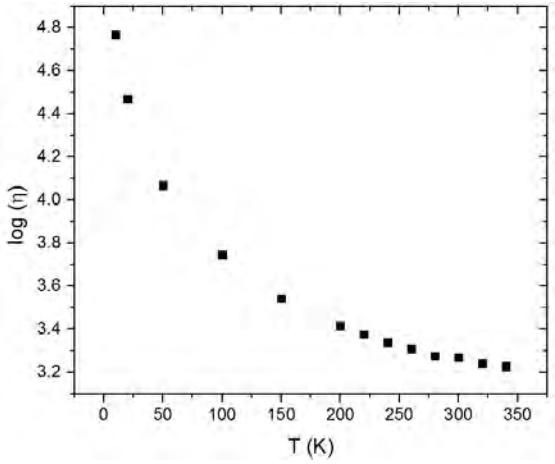


Figure 5.15: *Dependence of the logarithm of the ideality factor with the temperature.*

temperature below 90 K, between 90-140 K, 140-200 K and above 200 K respectively. The plot of the logarithm of the ideality factor against the temperatures presented in figure 5.15 shows two regions, namely for the temperature above 200 K, the logarithm is located between the value 3.2 to 3.4, whereas below 200 K there is a wider spread of the data. It can be said that, at temperatures above 200 K, the ideality factor is weakly dependent on temperature. The ideality factor increases rapidly as the temperature decreases. Combining the ideality factor results with the values of the activation energy, we can reasonably say that, at low temperature the carriers have just enough energy to cross small barriers, therefore will likely use much winding path between electrodes. Since the ideality factor is symbolized by an ideal junction, it can be expected that with a windier trajectory of the carriers the ideality factor will increase. However,

other types of transport mechanism are very likely involved in the two regimes, such as the hopping transport well-know in polymeric blend films with metallic electrodes [240]. The data analysis infers that the electrical transport mechanism in a CST is temperature dependent. It also shows that, for a device made of an active material with grains, domains, or clusters the activation energy is lower at low temperature, the low carriers energy may results in carriers using windier and longer paths to travel between a pair of electrodes, therefore crossing more junctions, hence decreasing in conductance. However, they are several paths through the material which may have similar lengths with different energy, it is still unclear how the preferred path may be chosen in this case by carriers, and how this behavior may affect the overall dependence of the ideality factor as the temperatures change.

The inverse of the extracted series resistance from fitting the experimental data of figure 5.10 was plotted against the temperature (figure 5.14b). The internal series conductance increases with the temperature. The conductance shows an exponential increase at high temperature, especially above 150 K. Whereas between 50 and 150 K the series conductance overlap within their error bars. The decreases of the series conductance were also correlated with the increases of ideality factor. At low temperature, carriers have low thermal energy and can only cross barriers with small height. By this process, the carriers path becomes longer and yield increases in the resistance. Additionally, the increasing conductivity could also be attributed to the intrinsic increases of charged carriers in a doped semiconductor material as the temperature increases.

The graph of figure 5.16, shows that as well as the ideality factor, and the series conductivities, the internal saturation current also decreases when the temperature decreases. The experimental data showed that the ON current value does not change with temperature, therefore the reduction in OFF-current with temperature, yield an increase of ON/OFF current ratio. Namely the ON/OFF current ratio increase by a hundred order of magnitude from 340 to 10 K. The ON/OFF ratio of 10^3 obtained at 10 K, shows that the device can be operated at cryogenics temperature, this will add to the family of switching devices, a device capable of switching at very low temperature.

The saturation current for both the collector-emitter I_{CEs} (black squares) and the collector-based I_{CBs} (red circles) are non-linear and exhibit an exponential increase when the temperature increases. The saturation current ranged from (2.1 $\pm$ 0.2) μA and (2.7$\pm$ 0.1) μA at 10 K to (50.1$\pm$ 0.2) μA and (12.6$\pm$ 0.4) μA at 340 K for the collector-emitter and the collector-base current respectively. It should have been expected that symmetric devices with the collector-emitter and collector-base channel of same dimensions to have similar internal saturation current. However, it is observed that this only applies at cryogenic temperatures below 150 K. It is extremely difficult to

make a near perfect print in printed electronics, so a small mismatch during the registrations of each layer during the device production can possibly lead to such unexpected phenomenon. However, since the saturation current is similar at low temperature, this could as well be due to a reason not elucidated by this work and may need future investigations on the phenomenon.

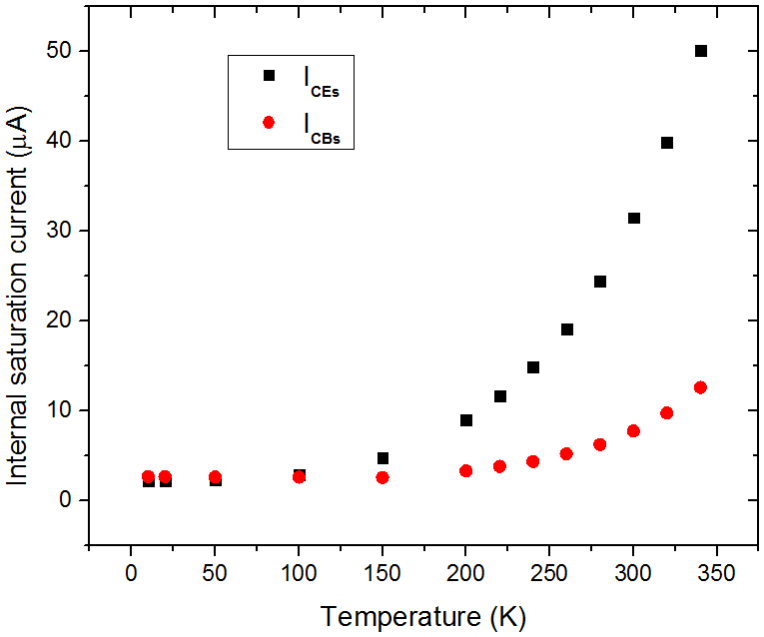


Figure 5.16: *Internal saturation currents in function of the temperature for a p-type symmetric JT transistor model. In black squares collector-emitter current and collector-base in red squares.*

Taking into consideration the variable temperature results applied to the switching mechanism described in figure 5.9, the collector voltage at positive potential with the emitter grounded, at a given base voltage, illustrated by the charge carriers will travel along the path with a higher potential difference between the collector-base and the emitter-base terminals. When the base-collector is positive, the transistor switched OFF the collector terminal. In theory, the OFF current should tend to zero, but we observed an OFF current of 45.7 μA at 340 K due to leakage. This reduces by many tenth order of magnitude at 10 K, yielding a reduction of leakage current by many tenth order of magnitude. These results are supported by previous studies which showed that devices electrical performance are often improved in cryogenic environment [248–250].

5.3.3 Consequence of constant bias stressing on the CST

The experimental data presented in figure 5.6 for the devices stressed for a period of 6 hours were further analyzed. The analytic model described by equation 5.3 were used to fit the experimental data of the bias stressed experiment. The substrate used for this

study was the plain paper made of fiber cellulose from wood. The biggest inconvenient of this substrate is their fragility to heat, fire, wettability, and their porosity. To prevent the wettability and thermal fragility of this substrate method such as including fire retardant or encapsulating the substrate with thin films of polymer are often used, however, these techniques significantly increase the substrate price per grammage. The office paper used as substrates for this study was neither coated or pre-treated against the heat. So, the current bias stress study here was limited by the fragility of the substrate. In fact, the 6 hours stress-time was imposed by the fragility of the substrate. Beyond six hours of stress time, we observed brown spot on the substrate similar to burning, so the devices were damage.

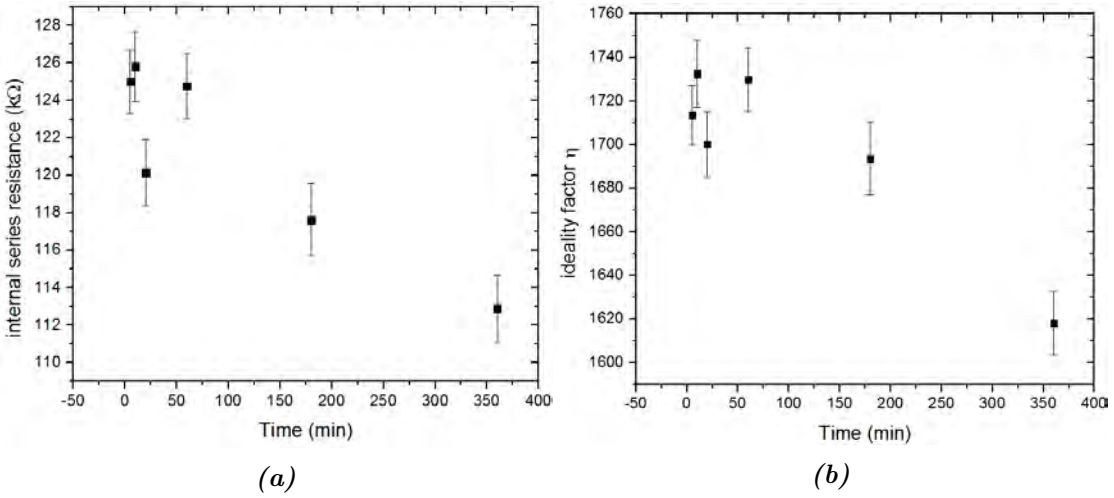


Figure 5.17: *(a) Dependence of series internal resistance (R) with time. (b) Dependence of ideality factor (η) with time. The base voltage of the symmetric CST JT model was biased with a constant current for an extended period of 6 hours. The device displayed here is the JTb300B characterized each time at collector bias of 100 V. The data are plotted with error bars representing the uncertainty on the data from fitting.*

Figures 5.17, shows the dependence of the series resistance and ideality factor with temperature. It can be argued that, for a transistor stressed over a short period of time, approximately below an hour, the parameters overlap within their error bars. As the bias stress time increased, the ideality factor starts decreasing. The decreasing in ideality factor during the stress yielded an increase of leakage current at the collector terminal. Being aware that the CST operates by charge activation, this result was predictable, as the extended stress heats the active layer and therefore provides more thermal energy to carriers to cross the barriers. It is observed from the graph of figure 5.6 that the transfer characteristics progressively shift to the right from the initial unstressed device as the biasing time increase. s This result corroborated the shift observed in the transfer characteristics as the temperature changed, so we suggested the shift observed in the transfer characteristics was due the device self-heating.

Chapter 6

Alternating Current (AC) Switching with the CST

For all of their existence, transistors have been under intensive investigation due to their multifunctionality and applications including amplification, switching, light emission, modulation, logic gates, integrated circuits (IC) [47, 251–254]. Despite the attention given to transistor research, the majority of investigations have been made on operation with direct-current (DC) voltage/current [52, 255–258]. However, various works on transistors operated with AC signals demonstrate the importance of electronic devices directly driven by AC [43–46]. In previous chapters, we introduced a fully-printed current switching transistor and their operation which relies on activated charge transport through the complex network of nanostructured silicon. Due to the fact that the CSTs switching operation does not depend on the charge carrier type, but mainly on the activation energy for charge transport, we demonstrated that alternating current could be switched using CSTs. In this chapter, the switching mechanism of the CST is studied under AC voltage/current. As for the case of DC switching, the main parameters are extracted from least-squares fitting of the data and used to explain the operation mechanism.

6.1 Alternating current

Over the past decade, several studies have been made on the use of AC with electronic devices and components. For instance, in junction diodes and light emitting diodes [259–263] significant progress is being made. However, the operation mechanism of conventional BJTs and FET made them unsuitable for AC operation. Nothing to our knowledge has been done for the exclusive use of AC in transistor operation. In an

AC signal, the electric current changes direction periodically. Therefore unlike the DC, possessing constant voltage, the AC voltage changes from positive to negative. For this study, we used a voltage/current signal which is a sine wave defined by $v(t) = V_m \sin(\omega t)$, where $v(t)$ is the instantaneous voltage, V_m the maximum voltage, and ω the angular frequency. The main parameters of an AC signal are its frequency, which is the number of time that the voltage/current changes direction within a second; the maximum voltage, being the highest value of the instantaneous voltage and the root mean square voltage (V_{rms}) being the DC equivalent of the voltage that would lead to the same power dissipation.

6.2 Switching under AC

The necessity of being able to switch every type of signal is critical in electronics. However, some forms of signal like AC, present a higher difficulty to be switched compared to the DC. For very low-speed applications, AC signals can be switched using a mechanical switch. However, for high speed and automated switching, mechanical switches can no longer be used. Due to the importance of alternating and pulsed signal switching in machine drive, computers, electronics, instrumentation applications [53, 54], and various solutions have been introduced to switch AC signals. The reversely switched dynistor (RSD) is one of the devices used for AC switching [53–55]. The RSD is a two-electrode solid-state device made of a monolithic integrated thyristor, transistor, capacitor and diode units [53, 264–266]. RSDs' switch AC and surge signals ON and OFF by acting on a load mounted on the devices [54], RSDs' are used to switch very high voltage and current, such as 25 kV, and 10 kA [267]. Although an efficient AC switch, the RSDs switching time still needs to be improved. Thyristors, or Silicon Controlled Rectifier (SCRs) and triacs are devices used most widely for AC switching [56–58]. Triacs are three terminal devices made up of pre-amplifiers and thyristors, mounted in an anti-parallel arrangement. The triac is a solid-state switch used with loads that are driven with alternating voltages [58]. Triacs can turn an AC signal ON or OFF when triggered [59]. Although good AC switches, triacs, and SCRs are very limited when it comes to switching high frequency and high amplitude pulse signals [55]. Viewing the increased need of devices and components working directly with AC, and the importance of AC switching in modern electronics and appliances, all efforts are being made to improve the existing AC switches and more importantly investigate new approaches of AC switching. Here it was shown that direct current could be switched with CSTs [48, 144]. The switching operation mechanisms were dependent on the arrangement of electrode configuration and based on charge transport. In this chapter, we demonstrate that an AC signal can be switched with a CST without additional electronic components [37]. This

represents a significant improvement compared to the current commercial AC switches mentioned earlier.

6.3 Experimental method

Besides the characterization under DC voltage/current presented in previous chapters, the transistors were characterized under AC conditions. This section presents the architecture of the transistors used in AC, as well as the apparatus, equipment and set up used during the AC characterization.

6.3.1 Transistor fabrication and design

In earlier works [37, 48, 49, 144] and previous chapters, we presented various architecture of CSTs and concluded that their switching operation was governed by the same mechanism. For instance, the CST switching mechanism was not dependent on the type of carriers but only on the non-linear varistor behavior of its active layer. Therefore a study performed on a p-typed CSTs could be generalized to the n-type and vice versa. The two models of CSTs shown in figure 6.1 were used for AC studies.

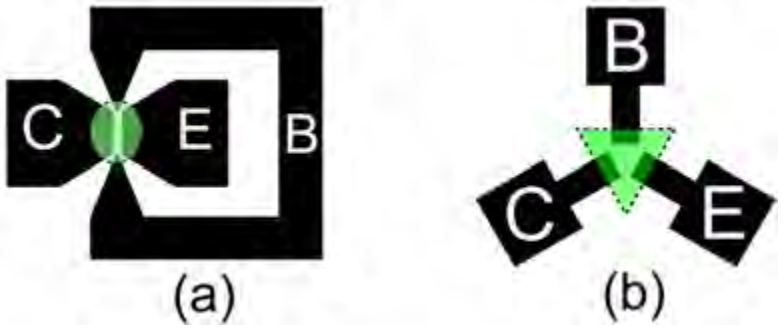


Figure 6.1: *CSTs architecture use for the AC measurements. (a) Printed asymmetric CST structure with terminals labelled and active material shown(green). (b) Printed symmetric CST structure with terminals label and active material shown(green).*

Figure 6.1 consists of an asymmetric CST (figure 6.1a) with transistor channel lengths L_{CE} ≈0.4 mm and $L_{CB} = L_{BE}$ ≈0.2 mm and the symmetric CST (figure 6.1b) with channel length and width equal $L = W \approx 0.8$ mm. The devices were produced by screen printing onto 80 g/m^2 flexible plain paper substrates at room temperature without post-processing steps. The ATMA AT-60PD semi-automatic flatbed screen printer was used to produce the devices. The metal contacts (dark in figure 6.1) were printed with DuPont LuxPrint 5000 silver conductor ink, using a 150 lines/cm monofilament polyester mesh with a fibre diameter of 31 microns. The metal contacts were cured for 24 hours at ambient conditions, and their average thickness was found to be 18 μm [37] measured

with a Wyko NT1100 optical profiler. The semiconducting layers were printed using a water-based acrylic silicon ink [24, 29–31, 37, 48, 49] (in green in figure 6.1). The inks contained nanostructured particles of silicon produced from highly doped p-type silicon wafers (Siegert Wafer GmbH, Germany) with an initial resistivity $\rho < 0.002$ Ωm by high energy milling for 5 hours. The semiconducting ink was cured for approximately 18 hours at ambient condition prior to the devices characterization. Similarly to the devices used in DC study, the nanostructured silicon had a log-normal size distribution, with mean of (78.4±1.2) nm along their short axis and (126.7 ± 3.4) nm along their long axis [268]. There was no significant presence of other elements or an oxide shell on the particles. HRTEM studies of a section produced by FIB-SEM cutting of printed layers [29, 38, 165] have shown that they were no significant oxide barrier at the interface between the silicon nanoparticles after printing the devices.

6.3.2 CST characterization under alternating current (AC)

The CSTs were characterized in a similar manner in both AC and DC. However, the AC characterization was carried out in two steps. The transistors used for the AC characterization were first characterized in DC using the semiconductor parameter analyzer to ensure that the devices were operating without fault. Afterward, the AC characterization was performed on those devices.

A custom made testing station was built with various equipment, to be able to characterize the device in AC-AC. The electrical characterization of the CST was subsequently performed in AC-AC using the circuit diagram of figure 6.2.

Two variacs directly connected to the main supply were used as current/voltage sources, labeled in the circuit diagram as source 1: (S_1) and source 2: (S_2), at a frequency of 50 Hz. Variacs were chosen for their capacity to produce higher sinusoidal voltage compared to the Agilent 33220A Arbitrary waveform generator which could only produce a maximum of 20 V peak to peak, that is unable to drive the CSTs. A digital oscilloscope TDS2024C (Tektronix) was connected to the base (B) and collector (C) terminals to monitor the current flowing from the two variacs as shown in figure 6.2 by the channel 1 and 2. Since they were not significant capacitive and inductive effect inside the CST, the two signals from the variacs were in phase. A series resistance load of 100 kΩ was connected directly between the variacs and the transistor under measurement for safety reason and to limit the current in case of failure. The resistor value was chosen as not to create a significant drop in the voltage at collector and base terminal.

During the characterization, the collector (C) was biased with an AC voltage from the current source (S_1) which was stepped progressively for new voltages bias. The second

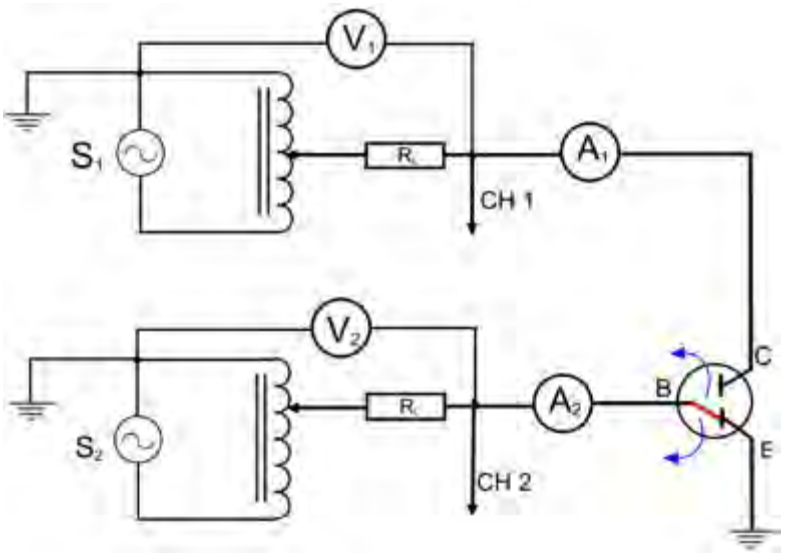


Figure 6.2: *Circuit diagram used to study the AC behavior of the CSTs. The sources 1 and 2 (S_1; S_2) are two independent variac. During the measurement, a variac is used to bias the collector terminal at a constant V_{rms} voltage, meanwhile the other variac is used to sweep the voltage across the base from 0-120 V. Variacs are connected to the transistor through a resistance load (R_L). Ammeters are connected between the variacs the collector and the base to measure the current flowing through those terminals. Voltmeters V_1 and V_2 measure the voltage at the electrodes. The voltage at the collector and base were always monitored by an oscilloscope.*

AC current source (S_2) delivered a voltage between 0-120 V that was used to sweep the current in the base, while the emitter (E) was grounded for all the measurements. The voltages at the terminals, as well as the current flowing into terminals were measured using either a Keithley 2000 digital multimeter or Mastech MS8217 digital multimeters.

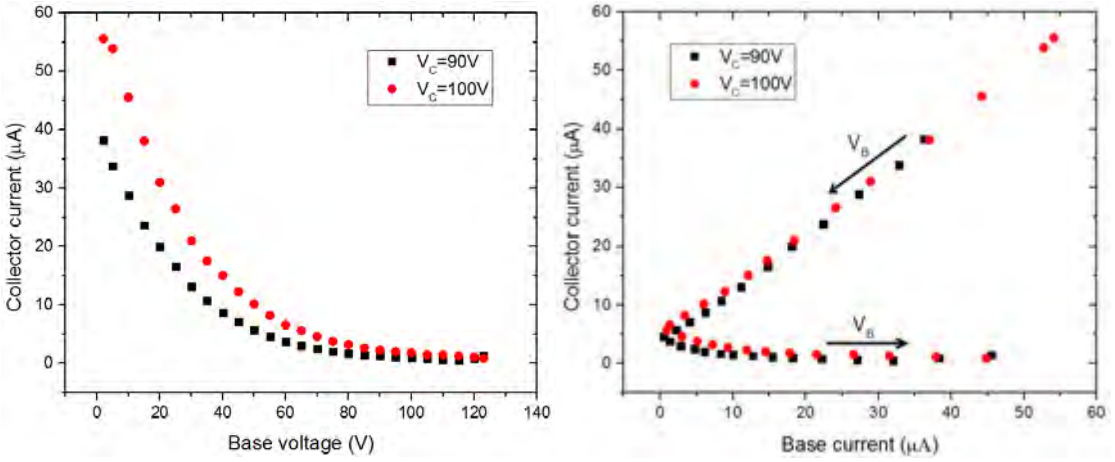
For this experiment approximately 40 CSTs devices were characterized. The data obtained from this characterization were processed and plotted using Origin Pro 9 and will be presented in the following section.

6.4 Results

As observed during the CST characterization under DC, the devices under AC presented similar electrical behavior, however, a wider spread was observed in the data. A plausible reason for the spread was the fully manual collection of the data on a bench test compared to the data collected with advanced characterization tools in DC. The results to be presented in this section are representative of the average electrical behavior of the devices.

During the AC-AC characterization, the emitter remained grounded, and the collector voltage was biased with voltage in an extended range from 20-110 V. This range was

chosen to correspond to the range study for the DC characterization as they will provide more ground to analyze the results and compare it to the one observed in DC. For low emitter voltages, as observed in DC operation a switching pattern could not be observed. The emitter terminal was grounded for the whole duration of the measurement. A voltage from 0 to 120 V was manually swept at the base terminal at approximately 5 V/step. The voltage limit of 120 V was imposed by the limit of operation of the variacs. However, this range was acceptable since the switching in the collector electrode was observed well before this value. The resistor load depicted in figure 6.2 was taken to be R_L =100 kΩ for the results presented here.

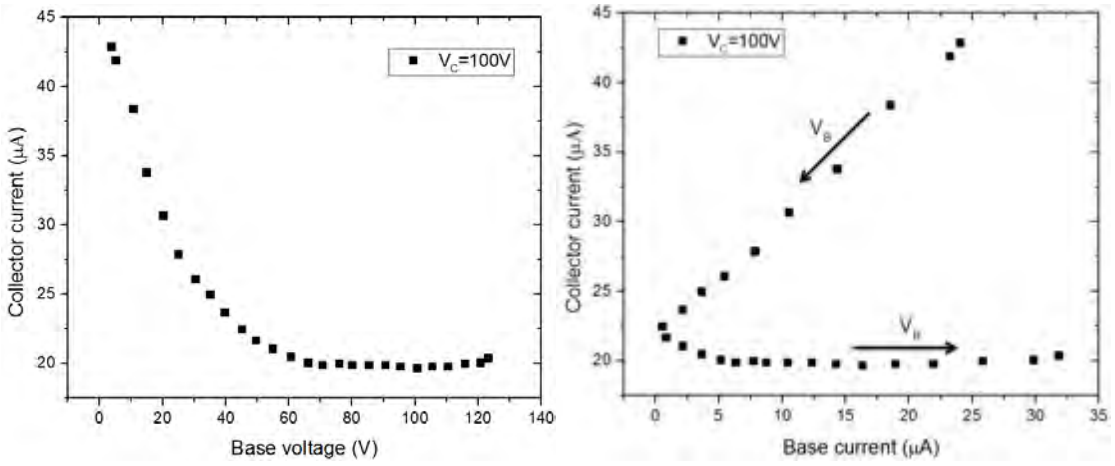


(a) *(b)*

Figure 6.3: *Transfer characteristics of the asymmetric CST J transistor under AC-AC operation measured at room temperature at a collector bias of 90 and 100 V(a) current-voltage at 100 V (Red circles) and 90 V (black squares), the arrow represents the direction of the base voltage increase. (b) current-current transfer characteristics at 100 V (Red circles) and 90 V (black squares).*

Figure 6.3 presents the IV and II transfer characteristics for the asymmetric CST J device measured for collector biases of 90 and 100 V. Figure 6.3a shows results similar to those observed with the operation in direct current [37, 48, 144]. Here, it can be clearly observed from the IV curves that, for 90 and 100 V collector bias, the differential conductance has a negative gradient and decreases almost exponentially until the switching threshold voltage, where the gradient became approximately zero. For a gate voltage greater or equal to 65 V considered as the threshold switching voltages at the bias of 90 and 100 V the base, current was approximately 2.8 μA and 0.9 μA respectively for those voltages. This lower value of the current is the OFF current . Figure 6.3b shows the II characteristics in AC for an asymmetric CST. For a low base voltage, there is a large current in the collector, the collector current decreases in a near $\frac{I_C}{I_B} \approx 1$ gradient to the lowest collector current value of approximately 1 μA. The arrows (black) represent the direction of base potential increases, it shows that starting from the base voltage of 0, the collector current decreases progressively until it reaches the OFF value

when the base voltage is approximately greater or equal to 65 V. The current leakage observed in DC mode of operation is also observed in this case, but the leakage here is higher that those in DC mode of operation. Besides the reason mentioned for leakage in DC operation, the manual operation of the set up should be a factor that increases the leakage.



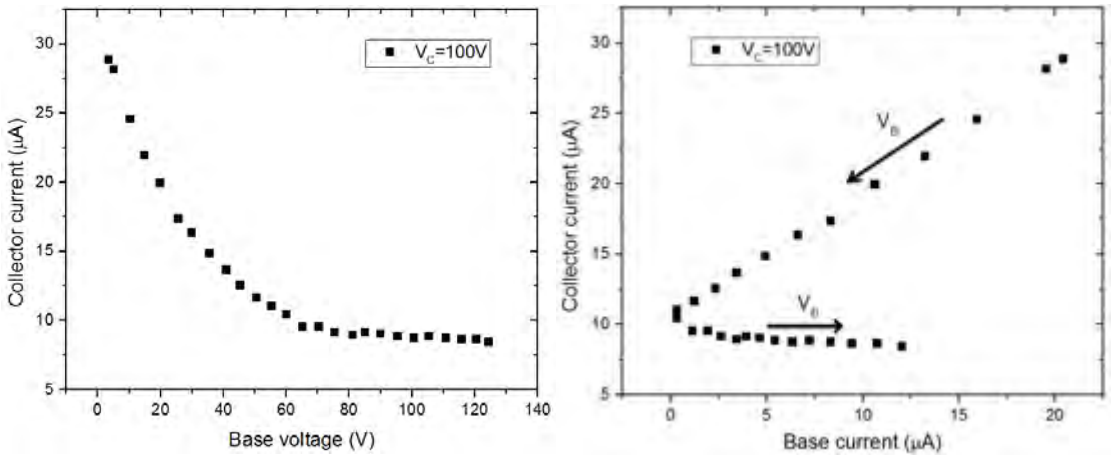
(a) *(b)*

Figure 6.4: *Transfer characteristics of the symmetric CST JTa transistor (device : CST JTa3P11)measured at room temperature (a) current-voltage transfer characteristics in ac operation mode of a CST with a collector voltage at 100 V. (b) current-current transfer characteristics in ac operation mode of a CST with a collector voltage at* 100 *V. The arrow designates the direction of increasing potential applied to the base.*

Figure 6.4 shows the transfer characteristics of the symmetric CST JT device in AC mode of operation. The transistors were characterized under the same conditions as the asymmetric device shown above at the collector bias of 100 V. The OFF current for this device was reached when the base voltage was approximately $V_B \gtrsim$65 V as observed in the asymmetric model, the OFF current was observed to be I_C =19.8 μA. So the leakage in the symmetric transistor was in general higher than in its asymmetric counterpart. The high leakage current observed in the symmetric configuration could be attributed to the greater channel length and width. The OFF current in AC was an order of magnitude higher than the OFF current obtained in DC characterization, which can be attributed to the high leakage current in AC, with the variacs connected by a common ground.

Figure 6.5 is presented to illustrate the consistency of the CSTs switching in AC operation. The switching behavior of the nearly 40 devices characterized in AC with the collectors biased in an extended voltage range 20-120 V, showed that proper switching is obtained only for collector voltages greater than 70 V. Below this value the switching region is very poorly defined and the collector remained conductor even for high value of the base voltage. The whole experiment data collected from this experiment will be

supply to the university of Cape Town library as part of the supplementary material of this work. The OFF current is observed to be I_C =8.8 μA for a CST JT device. It should be mentioned that the variation in OFF current was wider in AC operation than the one in DC. Although we attributed the wider spread in the OFF-current in AC operation to the manual collection of the data, the possibility of other type of factor affecting the OFF current can not be excluded.



(a) *(b)*

Figure 6.5: *Transfer characteristics of a symmetric CST JTa transistor (device : CST JTa4P11)measured at room temperature (a) current-voltage transfer characteristics in AC operation mode of a CST with a collector voltage at 100 V. (b) current-current transfer characteristics in AC operation mode of a CST with a collector voltage at 100 V. The arrow designates the direction of increasing potential applied to the base.*

6.5 Discussion

This section closely investigates the results collected from the CSTs characterization in AC operation, the CST switching mechanism under AC, as well as the similarity between AC and DC mode of operation. The varistor model will also be used to model the CSTs under AC and extract key parameters.

6.5.1 CST switching mechanisms under alternating current (AC)

In previous works, the CSTs were described using a model of a triangle of varistors, which was motivated by early studies on nanostructured silicon [24, 29–31, 37, 48, 49, 60] used as the active material in electronic devices. Varistor-like materials made of blocks and domains can be described using diodes, so the non-linearity of a varistor can be modeled using identical diodes mounted in an anti-parallel configuration. The triangle

of varistors, modeled as a triangle of anti-parallel diodes used for DC is used in this section to describe the CST operation mode.

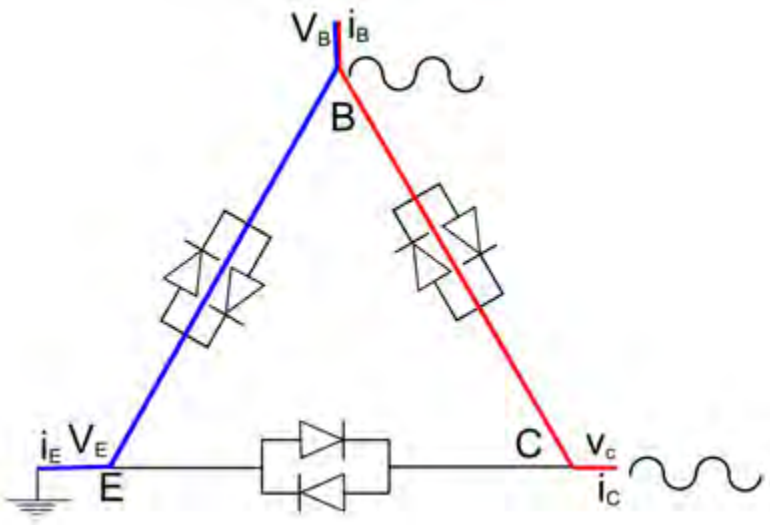


Figure 6.6: *CST alternating current switching mechanism. The collector and the base are source by AC current in phase. For base voltage greater than the threshold of $V_{rms} = 65V$, the preferred conducting path is the path between E-B (in blue)and the current between B-C is very low and almost constant. For voltages below the threshold the preferred conducting path is between the B-C (red), therefore the current is flowing in the collector.*

The schematic of figure 6.6 shows a triangle with sides made of anti-parallel diodes, where the emitter is grounded. In this model, the arrangement of anti-parallel diodes allows the current to always be able to flow between two terminals. When the collector terminal is biased with voltages lower than 60 V, the voltage increases in the base do not allow the collector current to completely be switched OFF. When the collector is biased at high AC voltages (90 or 100 V), and both the collector and base current are in phase, the increase of base voltage allows the current into the collector terminal to be fully controlled. When the collector voltage is biased with high AC voltages, and with the emitter grounded the preferred current path is between the base and collector for base electrode voltages below the threshold of 65 V. Therefore, the current flows into the collector electrode. For a base voltage greater than 65 V, the preferred path of the current is between the base and emitter and therefore there is almost no current between either the base or emitter and the collector. Thus the collector current is fully inhibited and the only current in the collector is the leakage. As indicated earlier, charge transport in the nanostructured aggregate silicon is based on activated charge transport [24]. In AC operation, unlike DC there is no permanent negative current or voltage, and therefore the preferred percolation path used by carriers from an electrode to another is based on the potential difference between the base-emitter and the collector-base. Thus for low base voltages, the base-collector path is the one with the higher potential difference, therefore the charge carriers will travel through that path. For base voltage

greater than the threshold voltage, the path with more energy became the base-emitter, and the current is switched OFF at the collector.

6.5.2 Modeling of CST in AC mode and parameter extraction

In chapters 3 and 5, the CSTs were modeled using a triangle of varistors. The triangle current in a set of varistors could be described by:

$$I_C = I_{CEs}\left[\exp\left(\frac{e(V_C - V_E)}{\eta k_B T}\right) - \exp\left(\frac{-e(V_C - V_E)}{\eta k_B T}\right)\right] + I_{CBs}\left[\exp\left(\frac{e(V_C - V_B)}{\eta k_B T}\right) - \exp\left(\frac{-e(V_C - V_B)}{\eta k_B T}\right)\right]. \quad (6.1)$$

where I_C describes the current flowing into the collector terminal. I_{CEs} and I_{CBs} are the reverse saturation current of the collector-emitter and the collector-base channels. η, k_B and T are the ideality factor, the Boltzmann constant, and the layer temperature during the measurement. V_B, V_C,V_E are the base, collector and emitter voltages respectively. The transfer characteristics data obtained from the testing station in AC were fitted using equation 6.1 and are shown in figure 6.7.

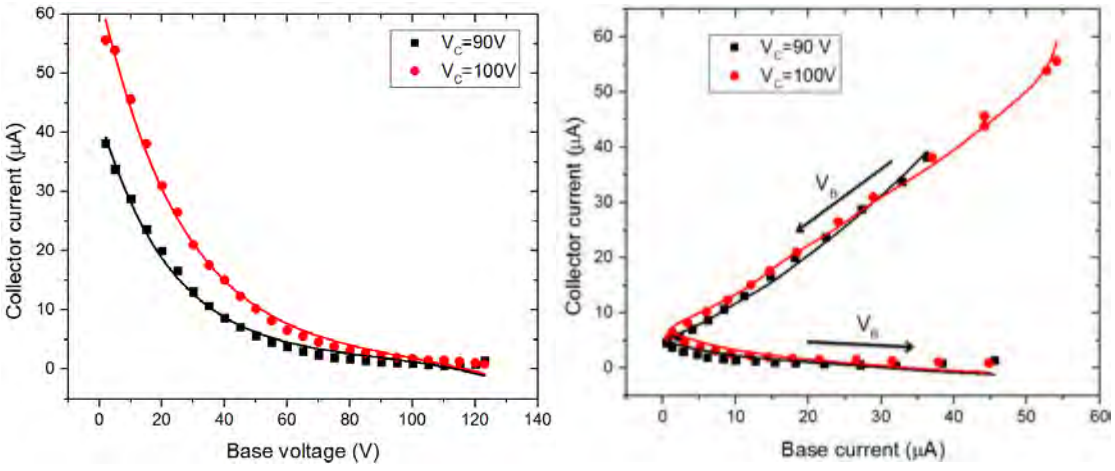


Figure 6.7: *Fitted transfer characteristics of the asymmetric CST J transistor J19 measured at room temperature.(a) current-voltage transfer characteristics in ac operation mode of a CST with a collector voltage at 90 and 100 V, fitted with equation 6.1 . (b) current-current transfer characteristics in ac operation mode of a CST with a collector voltage at 90 and 100 V fitted with equation 6.1 . The circles, squares represent the experimental data and the continuous (red) line represent the fitted data line.*

Figure 6.7 shows the fitted experimental data using the model of equation 6.1 on the asymmetric J19 transistor. The data of figure 6.7a, were fitted with the analytic equation 6.1, during the fitting the internal saturation currents, and the ideality factor were

allowed to vary while the temperature and the collector voltage were kept constant. The emitter current was zero, as that electrode was grounded during the whole measurement. The temperature was taken to be 295 K, this temperature was the approximate temperature of the environment where the measurement was done. The red solid line of figure 6.1 are the lines of best fit obtained after the converged fitting operation. The fitting model illustrated good description of the experimental data trend as the adjusted r-squared value of the devices fitted was around 0.9. The fitted data of the collector current were plotted against the experimental base current data and are plotted as the solid lines of figure 6.7b. Key parameters were extracted using the least squares fit of the data for the biased collector voltages of 90 and 100 V at 295 K and a frequency of 50 Hz.

	V_C (V)	I_{CBs} (μA)	I_{CEs} (μA)	η	Adj. r-squared
J19	90	0.74 ± 0.1	0.035± 0.005	883±30	0.99213
	100	1.29± 0.1	0.038± 0.006	1017± 31	0.9949

Table 6.1: *Results and extracted parameters for fitted current-voltage data of a "J" CST transistor in AC operation. V_C, I_{CBs}, I_{CEs},η, $Adj.r - Squared$, are respectively the collector voltage, saturation currents, ideality factor and adj. r-squared.*

Table 6.1 depicts the extracted saturation current for the collector-base voltage were higher by many ten order of magnitude than the collector-emitter saturation current. The ideality factor was found to be (883± 30) and (1017±31) at 90 and 100 V respectively which are comparable to the ideality factor obtained in DC operation.

More devices characterized in AC were also fitted using the same equation. Figure 6.8 is another sample representative of the fitting, which shows the fitted experimental data for the symmetric JTa transistors, characterized with the collector voltage bias with V_C =100 V. The fitting procedure was the same as the one used to obtain the table of figure 6.1. From the fit a general trend of the key parameters is presented in table 6.2

Table 6.2 shows the extracted parameters from fitting the experimental data of 4 symmetric CST devices. The devices presented here were randomly chosen for characterization. The results of table 6.2, shows a significantly higher collector-emitter reverse saturation current, as compared to the asymmetric design presented in table 6.1. This higher current was attributed to a much higher leakage current, due to the larger transistor channel length and width in the CST with symmetric architecture. We observed in table 6.1 and 6.2 that, for a given device the ideality factor tends to increase as the collector biasing voltage increases. This is the opposite to what was observed in DC operation, suggesting that other forms of electrical transport may be acting while the devices operate in AC.

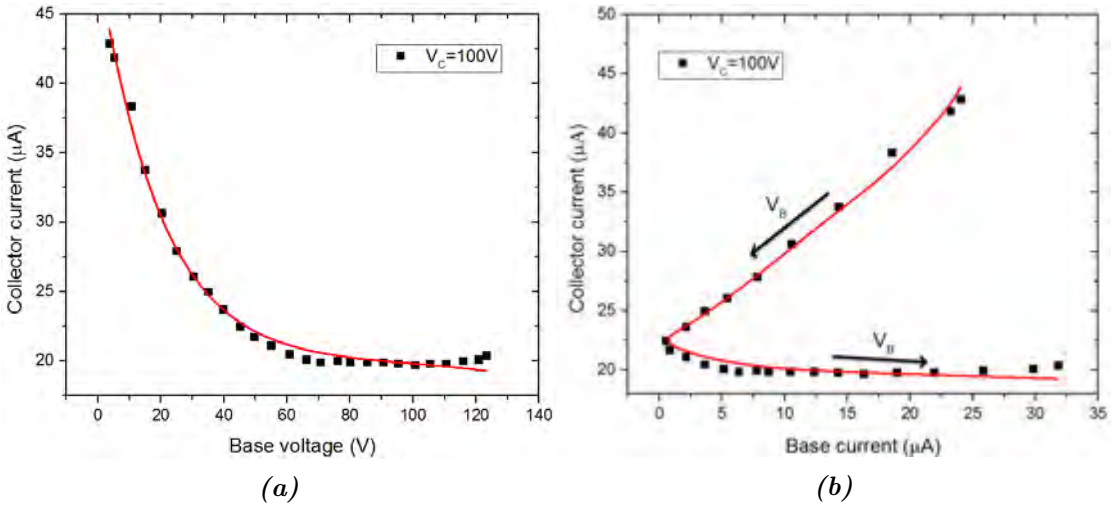


Figure 6.8: *Transfer characteristics of the symmetric CST JTa transistor (device CST JTa4P11)measured at approximately 295 K (a) current-voltage transfer characteristics in AC operation mode of a CST with a collector voltage at 100 V. (b) current-current transfer characteristics in AC operation mode of a CST with a collector voltage at 100 V. The arrow designated show the direction of increase base voltage.*

	V_C (V)	I_{CBs} (nA)	I_{CEs} (nA)	η	Adj r-squared
$JTa2P12$	90	157 ± 21	161 ± 23	752 ± 24	0.99287
	100	362 ± 74	33 ± 72	917 ± 48	0.9838
$JTa1P7$	90	199 ± 13	161 ± 12	869 ± 17	0.99705
	90	209 ± 12	157 ± 10	892 ± 15	0.99819
$JTa4P11$	90	249 ± 29	99 ± 12	851 ± 26	0.99384
	100	411 ± 44	155 ± 17	972 ± 28	0.9954
$JTa3P11$	90	144 ± 21	107 ± 16	861 ± 11	0.99344
	100	182 ± 31	124 ± 22	981 ± 14	0.99295

Table 6.2: *Extracted parameters from fitting the experimental data of the transfer characteristics of 4 symmetric CST, namely the devices labeled JTa2P12, JTa1P7, JTa4P11, JTa3P11 in AC operation. V_C, I_{CBs}, I_{CEs}, η, Adj r-squared, are respectively the collector voltage, saturation currents, ideality factor and adjusted R-Square.*

The CSTs principal mode of charge transport was shown to be based on thermal activation of their carriers. Thus, it is understood that the transport mechanism for nano-structured materials working on thermionic activation, principally on activated charged transport mostly depends on the energy given to the carriers [269, 270]. Therefore with either the DC or AC the switching could still be achieved with the CSTs without alteration of the devices. Various devices were alternatively used in AC and in DC without a noticeable change in their transfer characteristics. To fully support that the devices use the same mode of operation in both AC and DC, an analogy was drawn from their current-current transfer characteristics. For instance in figure 6.9, the

current-current transfer characteristics of the asymmetric J19 and symmetric JTaP11 are presented again. Unlike the presentation in figures 6.7b and 6.8b, the collector current for the region where the differential resistance is still decreasing was multiplied by a factor of -1, resulting in current-current transfer characteristics similar to those in the DC mode of operation.

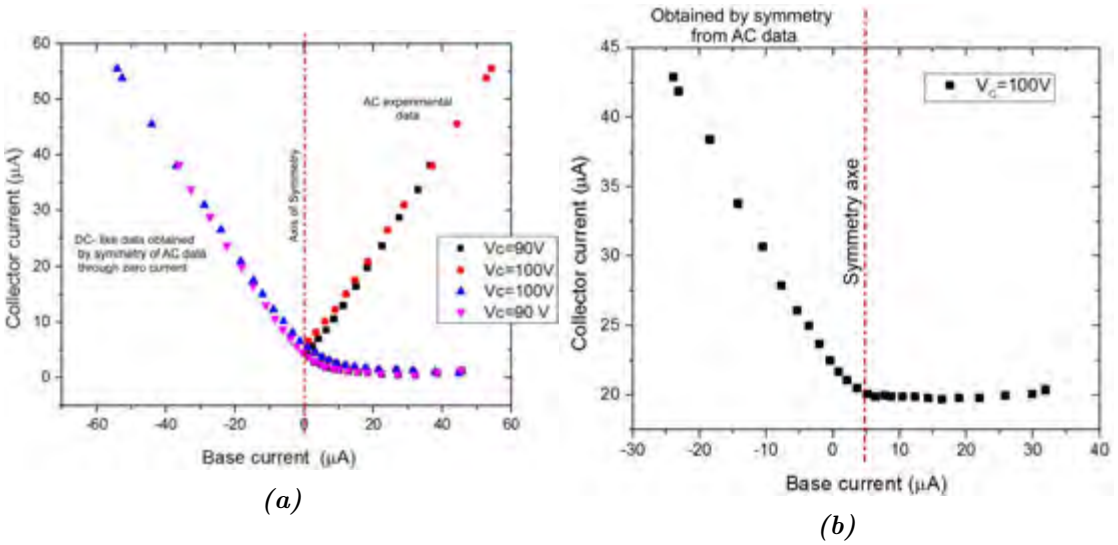


Figure 6.9: *Current-current transfer characteristics of asymmetric and symmetric CST, obtained by symmetry to approximately 0 V collector voltage from the experimental data of 6.7b and 6.8b at 90 and 100 V . (a) experimental data from device JTa19. (b) Experimental data from device JTa4P11.*

Transistors being widely used as switches nowadays [271], the novel current driven switch, presented here adds to the existing technology a new way of switching large AC signals. The devices also present a serious advantage over their counterparts such as the dynistors or triacs, due to their cost, flexibility, light-weight, environment-friendly. It is believed that the CST could also be used in AC in cryogenic environment, so possible further work will be to investigate the CSTs at variable temperature with transient signals.

Chapter 7

Conclusion

The work presented here employed nanostructured silicon, produced by milling, as the active material in a flexible transistor produced on paper by means of screen printing. The transistor reported in this thesis and referred to as Current Switching Transistors (CST), is operated as a two-way or double-throw in which the current switches between two terminals, by injection of current or applied voltage at the third terminal. These transistors printed with a matrix of silicon nanostructured material fixed in an acrylic binder, and silver electrodes, illustrate the particular ability to switch both DC and AC. The CST characterization both in DC and AC operation revealed that, when the collector and emitter terminals were held at a fixed voltage, the electrical conduction paths could be modulated by the voltage applied to the base terminal, therefore leading to the current being switched in the collector terminal. We also demonstrated that the current could be switched between each pair of terminals, and the CSTs terminals could be interchanged for various applications or connections.

The transfer characteristics of CSTs from above room temperature to very low temperature were studied, demonstrating that printed CSTs continue to work as switches at ultra-low temperature such at 10 K. The CSTs show lower OFF-current and higher ON/OFF ratio at this temperature, so making them an excellent candidate for cryogenics application. Further, variable temperature studies also showed that the current ON/OFF ratio is higher at low temperature, making the devices a better switch at lower temperatures.

In the OFF state, the devices had a significant leakage current, which is most likely due to the devices architecture or the type of semiconductor-metal junctions formed between the active material and the electrodes or the doping level of the active layer. As a result of the decrease in the conductance of the active layer, the magnitude of the leakage current was found to be related to the architecture, and significantly decreased with

decreasing temperature. It was also shown that the devices operated independently of the type of doping, their ideality factors were found to be significantly higher, by about 3 order of magnitude, than the ideal junction. The high ideality factor was a consequence of the structure of the silicon, suggesting that, at a microscopic level, the conducting path covers numerous clusters and junctions. Furthermore, the ideality factor increases in a non-linear manner as the temperature decreases, attributed to the diminution of thermal energy available to the carriers as the temperature decreases. Bias stressing the base terminal, with a constant voltage of 52 V, for up to 6 hours, demonstrated that the devices characteristics were not altered by the continued stressing within this time period, which indicates an acceptable reliability. However, from unstressed electrical transfer characteristics, a shift to the right of the subsequent transfer characteristics was obtained from current stressing on the base terminal. The shift of the transfer characteristics could be attributed to the device self-heating from long biasing. This was corroborated by the results obtained from variable temperature measurement.

Furthermore, we attempted to demonstrate that the CSTs electrical properties can be modified through variation of the characteristic dimensions of the active layer. Here, the increase in the channel width of the active layer, while keeping its length constant, resulted in a significant increase of the ON current, thus indicating the CSTs high capacity for being customized for desired applications without the need of changing the fabrication process.

The experimental data produced in this thesis was satisfactorily modeled using a triangle of varistors. Similarly, the varistors were represented by a pair of anti-parallel diodes. Modeling the transistors provided us with information on their internal structure and operation mechanism. Therefore the modeling may help to predict and produce better devices in future work.

Finally, the CSTs were further used as building blocks for fundamental logic gates (OR; AND). Here, two categories of gates were constructed with the transistors either in series or parallel and characterized at room temperature. The gate leakage was more significant compared to the leakage observed on a single transistor. The source of large leakage, not completely understood yet, was attributed to the type of metal-metal contact established between the transistors, the doping level of the active material and the manual collection of the data. Being aware that the CSTs still operate at low temperature, we predict that the logic gate will also work at low temperature. This work, therefore, suggests that the transistors presented in this thesis, do indeed add to the family of flexible devices, a desirable light weight transistor that is fully flexible, with a unique ability to switch AC and DC. With all its reliability and functionality, we believe that these transistors will most suitably find applications in the computing industries and machine drives that rely

heavily on logic circuits; therefore, with the major advantage of having the ability to work optimally in low-temperature applications. Furthermore, this work demonstrates that the transistor's flexibility and its production process at room temperature further allow high suitability for applications such as flexible displays, radio frequency identification (RFID), wearable electronics and smart packaging. Based on such satisfactory results, we envision to continue furthering this research by: (1) employing silicon produced by different mechanisms such as CVD, to produce these devices, (2) expanding the choice of substrate in a much wider range of flexible substrate and stretchable substrate, (3) studying the switching reliability of the CSTs over a long cycling period (4) attempting to print fully integrated circuits using our transistors and, finally attempting to use various active materials presenting varistor-like characteristics.

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Appendix A

Appendices

During this work, several hundreds devices and test characterization structures were produced. In this part of the thesis, we will add more results in the forms of graphs to support the result, presented in other thesis chapter. Throughout this work, the devices produced were given unique label in order to be able to identify each devices. For instance, a device could be presented here as J-P80-07-3: where J is the device design, p is the doping type of the active layer, 80 is the ratio in term of mass of the particle loading to the binder in the composite ink, 07 is the position of the devices in the sheet and 3 is the print number of the shit. The date where the electrodes of a devices were printed was also used as an element to codified the devices, so in some instance two device could have similar code, but will be different since they were printed on different date, hence files in different binder.

A.1 IV characteristics of p and n doped silicon

A.2 Extracted parameter from fitting

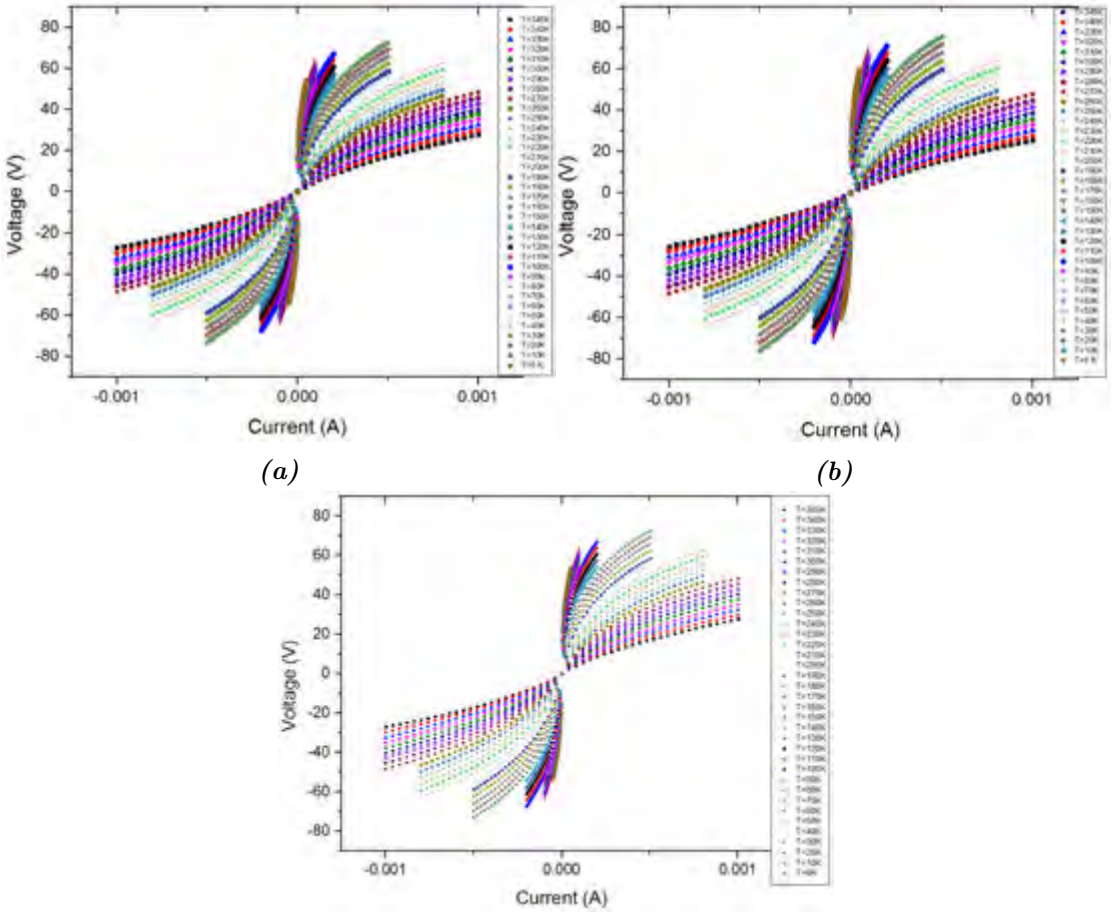
The parameters of table A.1 are the extracted parameters from some fitted CST W model devices. the dimension of the devices fitted here were the one of CST W_1 described in chapter 3.

A.3 variable temperature measurement

In this section we will present more graphs obtained with the CST JT at variable temperature measurement.

	V_C (V)	I_{CBs} (μA)	I_{CEs} (μA)	η	Adj. r-square
P80-11-8	45	99±2	117 ± 1	770 ± 4	0.99693
	50	102±2	137 ± 2	834 ± 6	0.99461
	55	104± 3	142 ± 3	877 ± 7	0.99234
	60	111± 3	148 ± 3	925 ± 8	0.98921
P80-10-12	45	194±4	185± 3	725± 5	0.99862
	50	197±6	185± 5	758± 7	0.9976
	55	213± 7	196±6	818± 9	0.99696
	60	248± 10	220±8	895± 12	0.99613
P80-10-8	45	137±3	137± 2	708± 4	0.99866
	50	147±3	149± 2	787± 5	0.99809
	55	156± 4	159±3	852± 6	0.99759
	60	156± 5	158±4	890± 8	0.99637
P80-10-1	45	140±5	164± 4	914± 10	0.99227
	50	122±4	160± 4	898± 8	0.99546
	55	139± 5	178±5	954± 10	0.99293
	60	126± 4	163±4	942± 8	0.99512
P80-2-4	45	52±1	42± 1	858± 5	0.99807
	50	48±2	46± 2	870± 7	0.99557
	55	35± 1	36±1	820± 4	0.9989
	60	32± 1	34±1	814± 3	0.99931
P80-2-3	45	44±9	29± 9	904±4	0.99871
	50	51±2	34± 1	972± 7	0.9965
	55	40± 6	25±5	936± 3	0.99938
	60	34± 4	21±3	910± 2	0.99965
P80-4-1	45	36±7	27± 8	900±4	0.99887
	50	41±1	32± 1	965± 6	0.99745
	55	30± 1	22±4	910± 3	0.99949
	60	26± 1	19±3	905± 3	0.99946
P80-5-4	45	32±1	30± 1	929±4	0.9986
	50	31±1	33± 1	954± 7	0.99646
	55	21± 1	23±1	892± 3	0.99923
	60	18± 1	20±1	874± 3	0.99942

Table A.1: *Results and extracted parameters for several CST W devices. The dimension of the devices presented here are similar to the one of W_1, shows in chapter 3. V_C, I_{CBs}, I_{CEs},η, Adj. r-Square, are the collector voltage, saturation currents, ideality factor and adj R-Square.*



(a) *(b)*

(c)

Figure A.1: *Current-voltage transfer characteristics for a cup and ball structure made of p-doped active silicon, printed on plain paper and characterized between 345 to 6 K. The first graph plotted with black square seen as the top in the first quadrant and as the bottom in the second quadrant is the graph at 345 K, the last graph is the one of 6 K in between those plot, the other one are from 340 to 10 K by step of 10 K. (a) transfer characteristics for the device P80-14-C1. (b) transfer characteristics for the device P80-12-C1. (c) transfer characteristics for the device P80-8-C2.*

A.4 Biased stress transfer characteristics at 90 V

The results present if figure A.5 are the one of a bias stressed CST JT devices for a total periods of 6 hours.

A.5 Transfer characteristics of the CST J, with TCO electrodes

The transfer characteristics presented in figure A.6, are the one of CST models J printed with TCO electrodes. More of these transfer characteristics would be supply as supplementary documents to the UCT library.

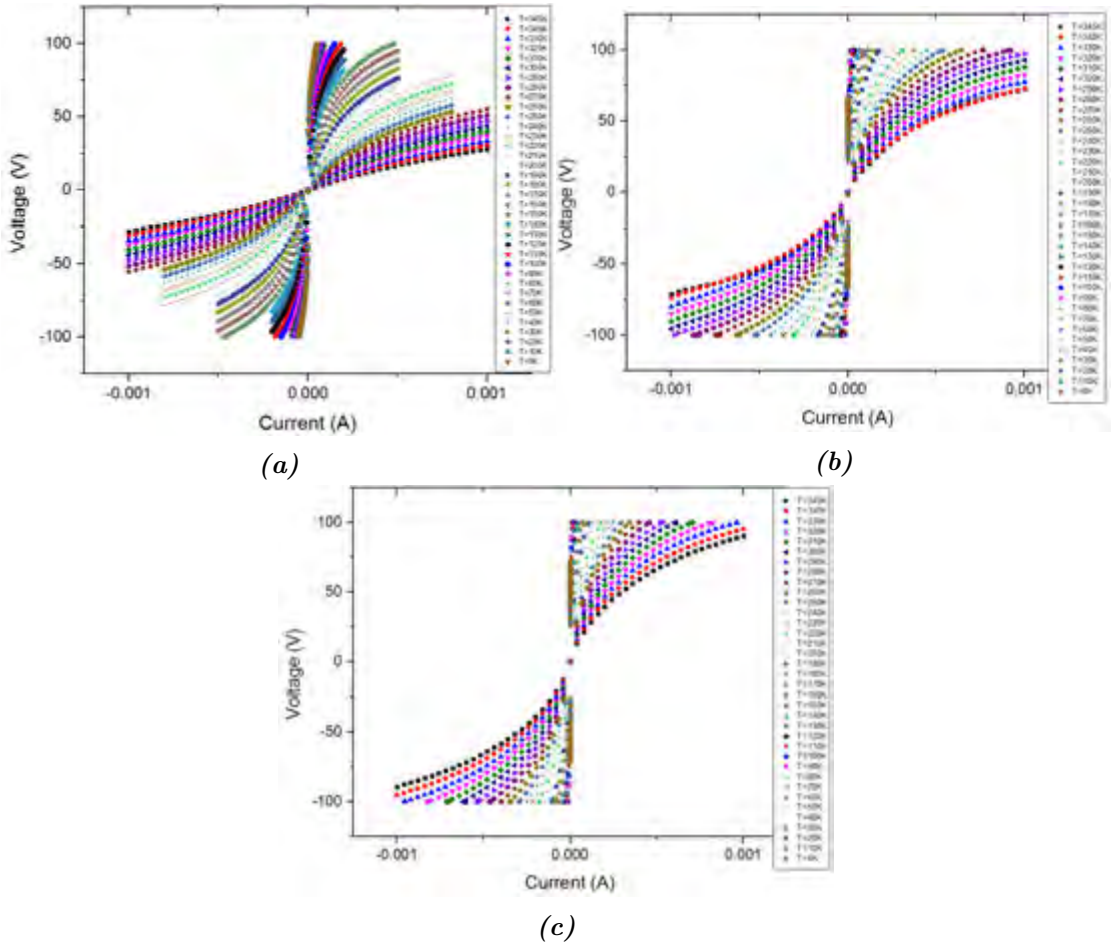


Figure A.2: *Current-voltage transfer characteristics for a cup and ball structure made from n-doped silicon printed on plain paper and characterized between 345 to 6 K. The first graph plotted with black square seen as the top in the first quadrant and as the bottom in the second quadrant is the graph at 345 K, the last graph is the one of 6 K in between those plot, the other one are from 340 to 10 K by step of 10 K. (a) transfer characteristics for the device N80-10-C1. (b) transfer characteristics for the device N80-5-C2. (c) transfer characteristics for the device N80-13-C2.*

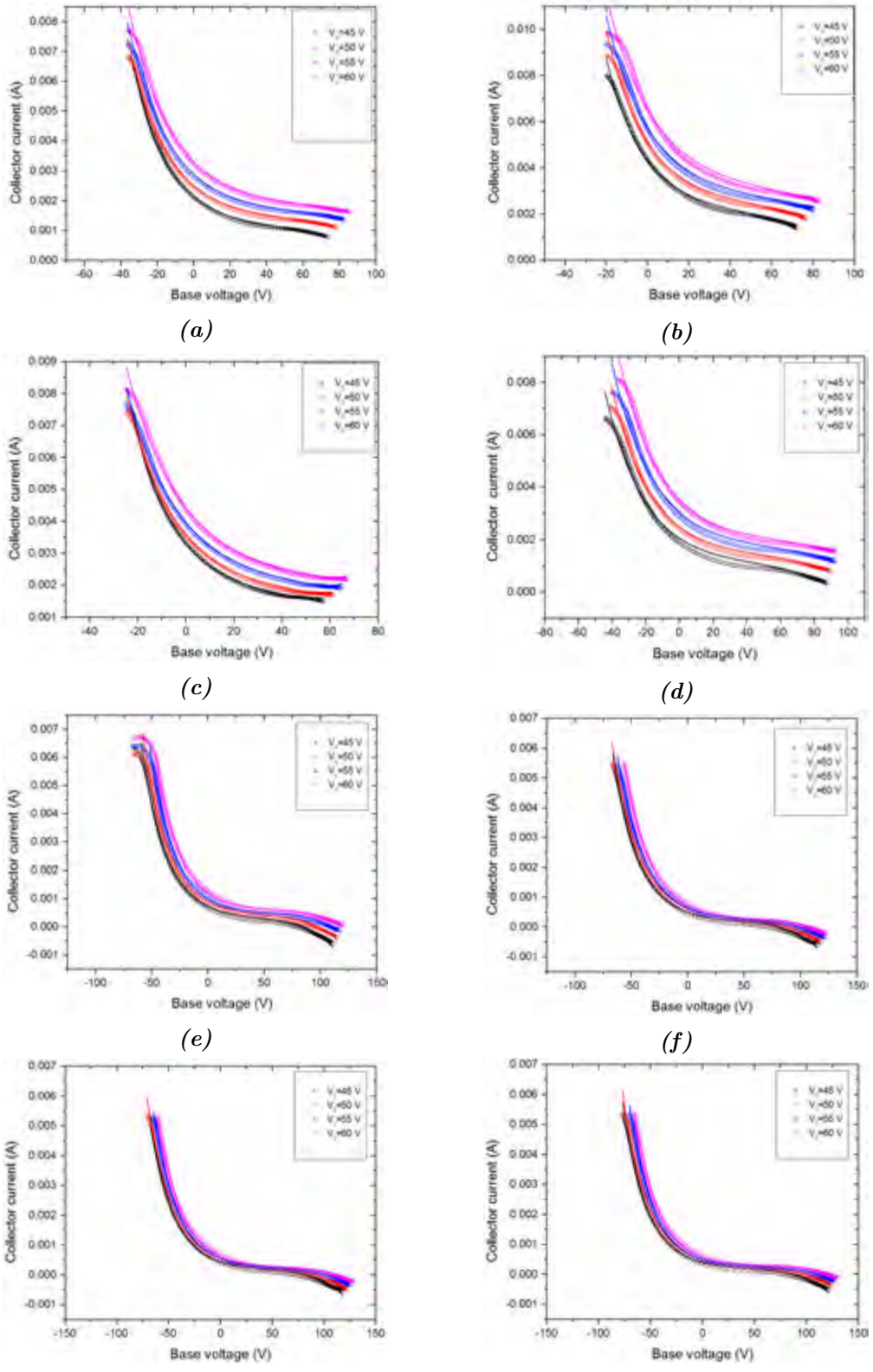


Figure A.3: *Current-voltage transfer characteristics for selected CST W devices. The devices are the one presented in table A.1. The graph are in the same order as classified in the table. The solid line represent the line of best fit of the experimental data.*

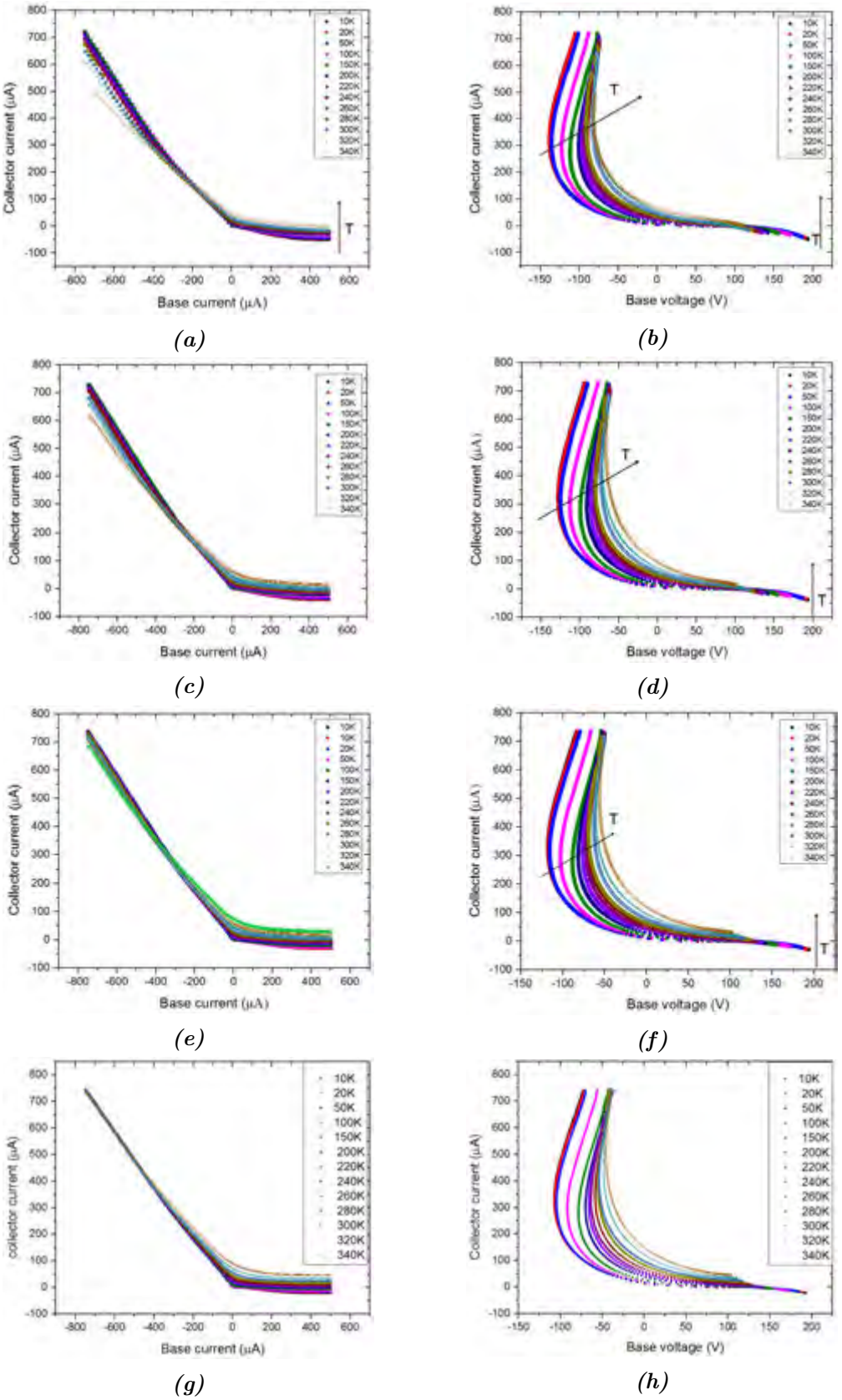


Figure A.4: *Current-current and current-voltage transfer characteristics for a CST at variable temperature operation at biased collector voltage of 60, 70, 80 and 90 V respectively.*

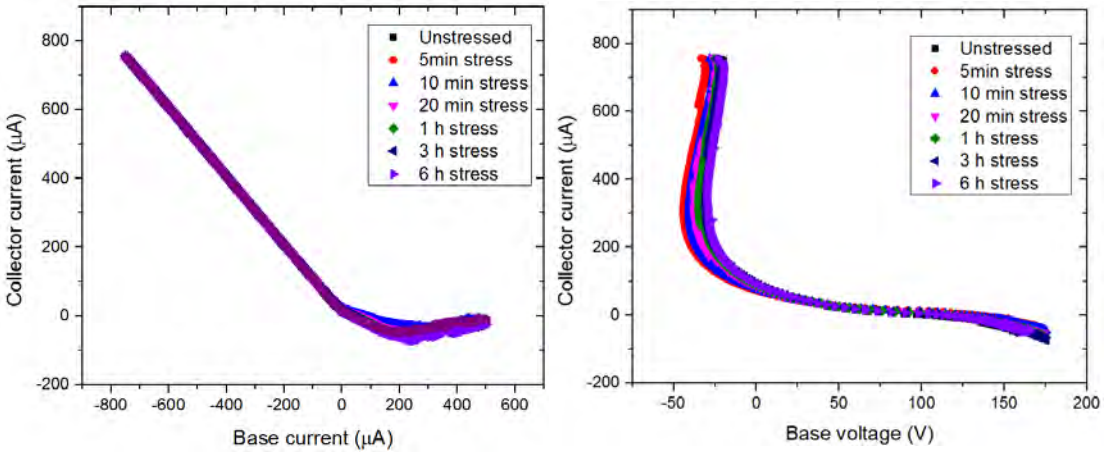
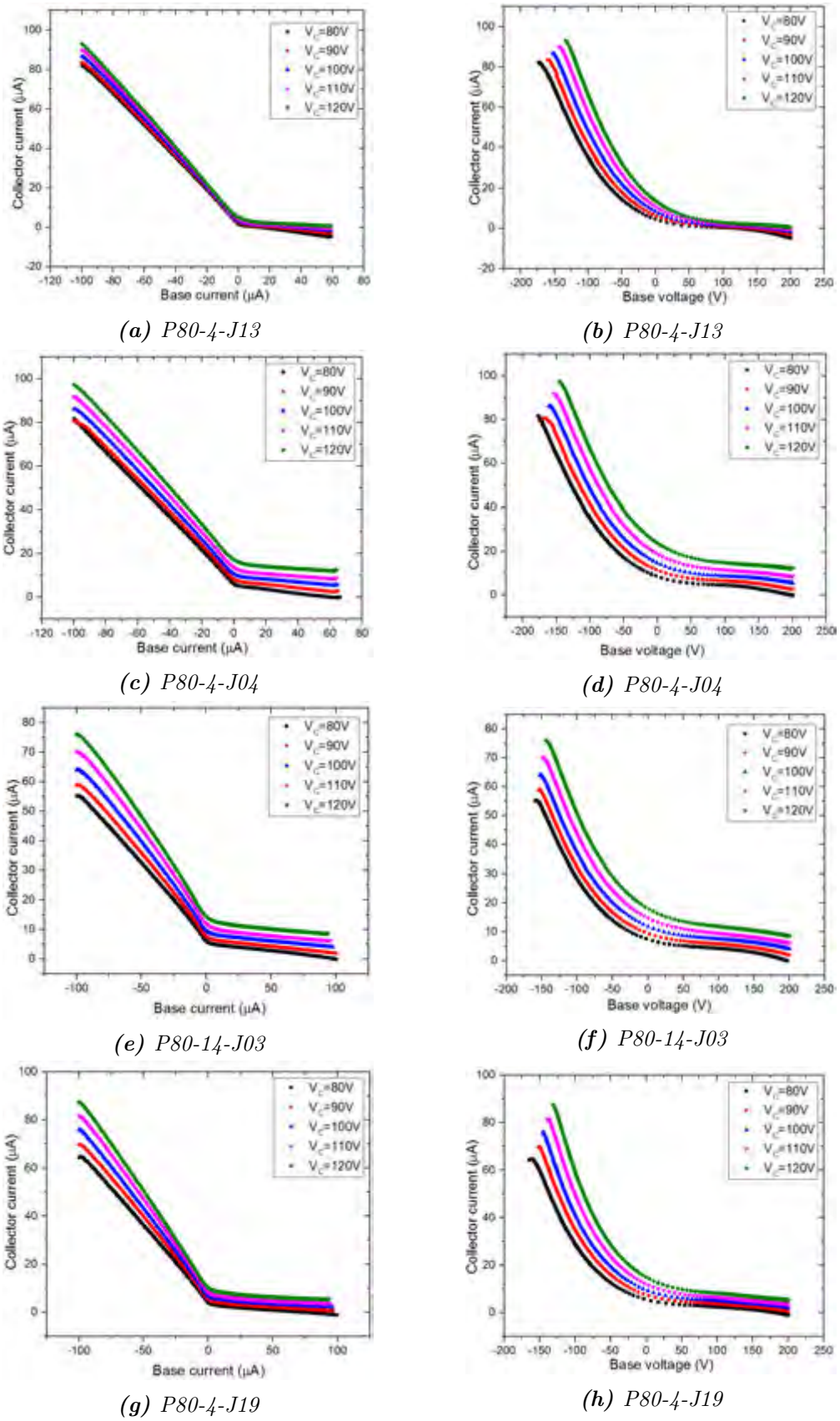


Figure A.5: *Transfer characteristics of a stressed CST JT device. The device presented here were stress over a period of 6 hours at a collector biased voltage of 90 V.*



(a) *P80-4-J13*

(b) *P80-4-J13*

(c) *P80-4-J04*

(d) *P80-4-J04*

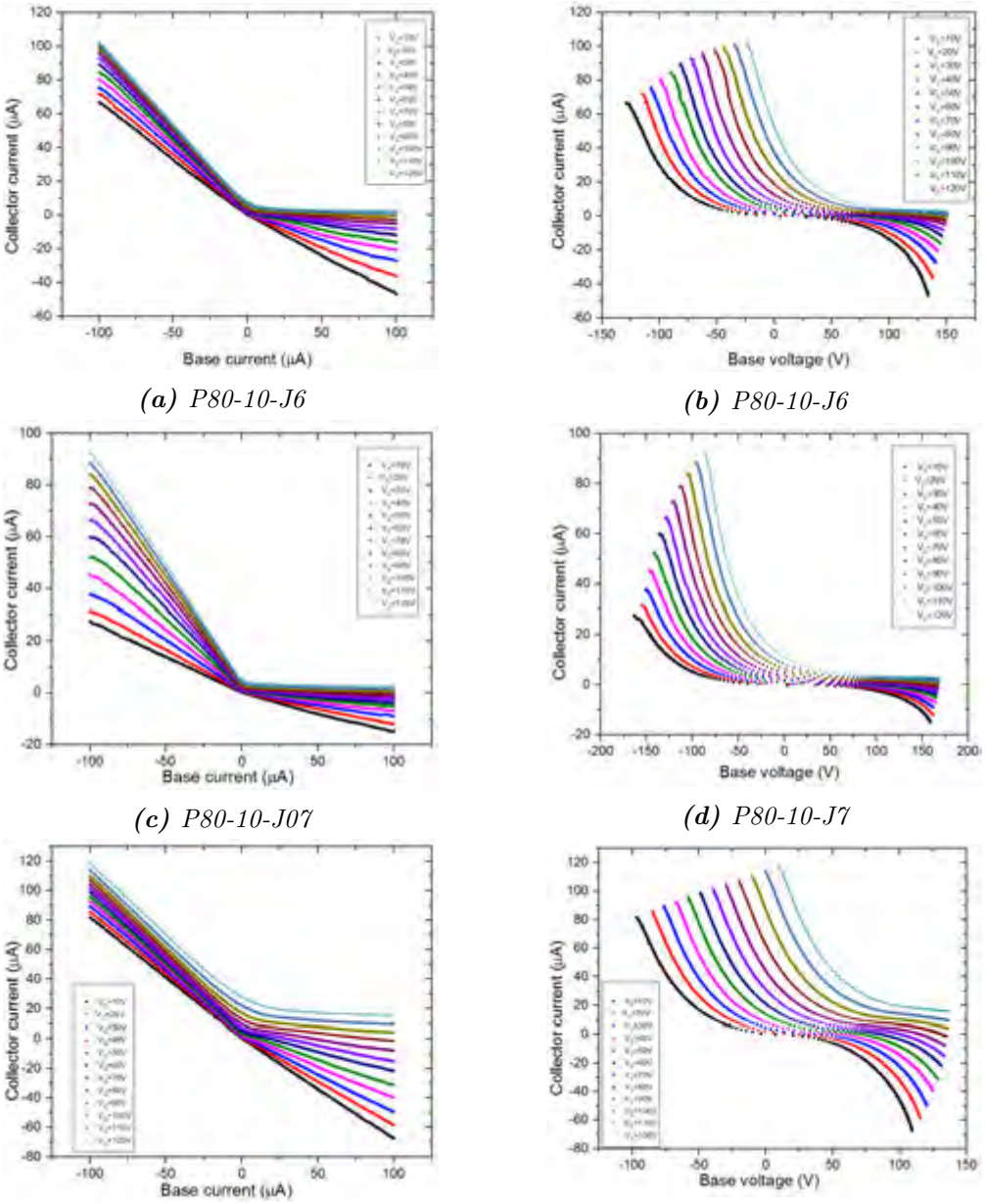
(e) *P80-14-J03*

(f) *P80-14-J03*

(g) *P80-4-J19*

(h) *P80-4-J19*

Figure A.6: *Current-current and current-voltage transfer characteristics for 4 CST devices with J design. The electrodes of the devices presented here were printed with thin condcutive oxide (TCO)*



(a) *P80-10-J6*

(b) *P80-10-J6*

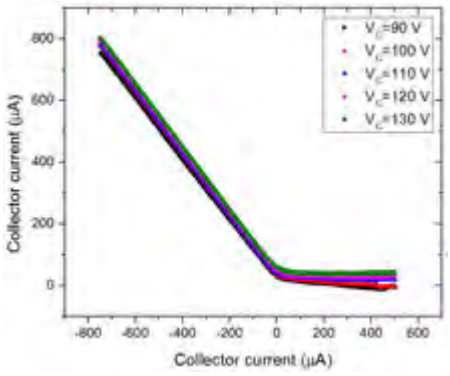
(c) *P80-10-J07*

(d) *P80-10-J7*

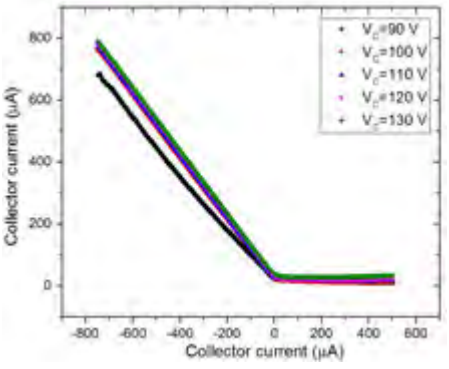
(e) *P80-9-J16*

(f) *P80-9-J16*

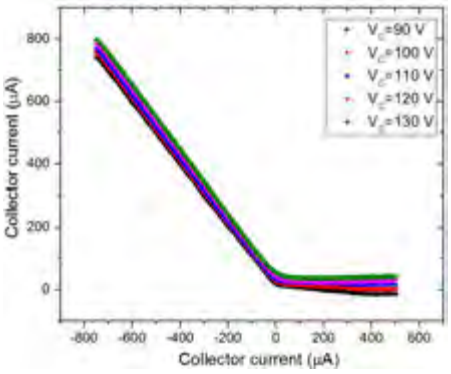
Figure A.7: *Current-current and current-voltage transfer characteristics for 3 CST devices with J design. The devices presented here were characterized with a bias voltage from 10 to 120 V by step of 10 V. The lowest plot is the one biased at 10 V and the upper plot is bias at 120 V.*



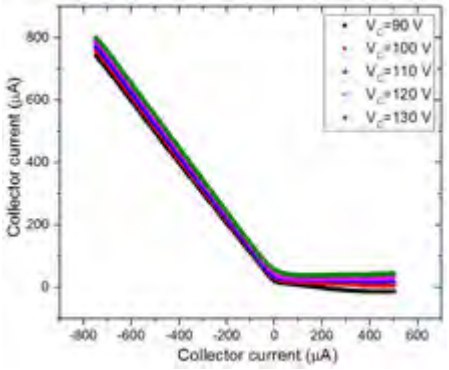
(a) *P80-JTa1-02*



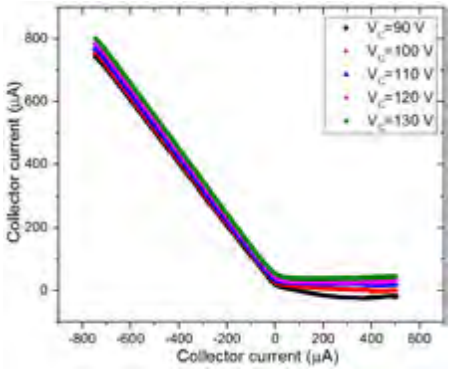
(b) *P80-JTa3-02*



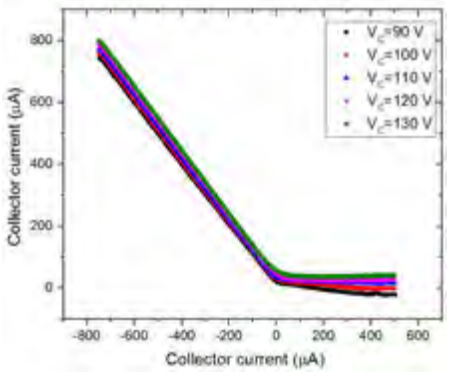
(c) *P80-JTa3-09-48*



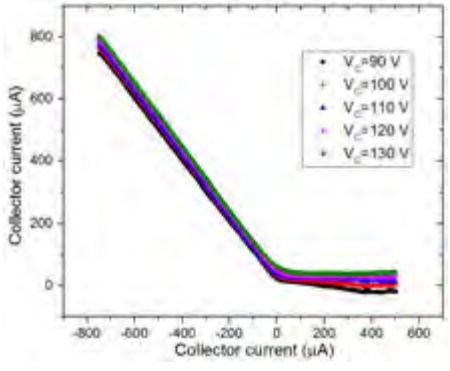
(d) *P80-JTa3-09-34*



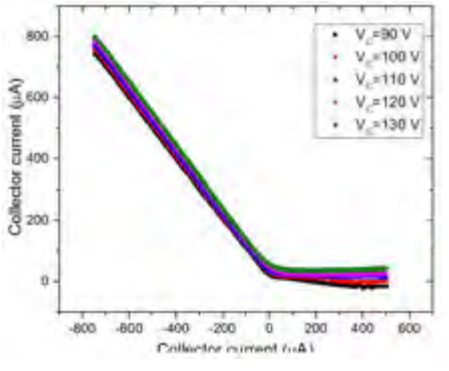
(e) *P80-JTa3-09-21*



(f) *P80-JTa3-09-59*



(g) *P80-JTa3-09-87*



(h) *P80-JTa3-09-71*

Figure A.8: *Current-current and current-voltage transfer characteristics for various CST devices with JT design. The devices presented here were characterized with a bias voltage from 90 to 130 V by step of 10 V. The lowest plot is the one biased at 90 V and the upper plot is bias at 130 V.*