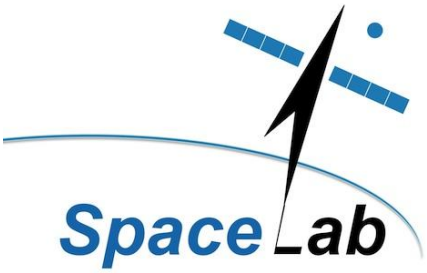
Thermal Design and Analysis of the SKA SA MeerKAT Digitiser

by

Vaughan Moss

A dissertation submitted in partial fulfilment of the requirements for the degree of
Master of Philosophy
in
Space Studies



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Thermal Design and Analysis of the SKA SA MeerKAT Digitiser

Keeping sealed radio-electronics cool in the Karoo Desert

by **Vaughan Moss**

Abstract

The Square Kilometre Array Project is a multi-national venture attempting to build the world's largest radio telescope. Australia and South Africa (together with other African countries), will be host to the SKA site. Both countries are building precursor radio telescopes to demonstrate their ability to successfully host the project. Square Kilometre Array South Africa (SKA SA) is currently constructing the MeerKAT Radio Telescope in the Karoo Desert.

Radio telescopes are conventionally designed to have the signal Digitiser located in the pedestal of the radio telescope antenna structure to shield the incoming radio signal from being contaminated by the electromagnetic interference (EMI)/radio frequency interference (RFI) noise created by the Digitiser electronics. However, if a Digitiser could be placed near the antenna feed, this would decrease the length of the signal path between the receiver and the Digitiser, which would decrease noise on the signal.

The aim of this thesis is to present a viable thermal design for an externally, near-feed mounted, passively cooled Digitiser on the MeerKAT Radio Telescope. This has never been done before.

Through calculation, simulation and design iteration this aim was achieved, resulting in an operational Digitiser system which is being used on the MeerKAT Radio Telescope and could potentially also be used in SKA Phase 1.

Dedication and Acknowledgements

This dissertation is dedicated to my wife. It would not have been completed without her constant support and encouragement. *Consummatum est.*

Thank you to Sias Malan, Francois Kapp, Alec Rust, Dr Marc Welz and Carla Sharpe for all their help and Square Kilometre Array South Africa who provided financial support for my degree.

Finally, thank you to my academic supervisor, Prof Peter Martinez, for his guidance, patience, encouragement and the endless hours he spent reading and suggesting edits for this dissertation.

Declaration

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09/11/2017

Contents

Acronyms

AC alternating current. 18

ADC analog-to-digital converter. 10, 17, 20, 49, 57–60, 64, 67, 93, 97

ADM Advanced Demonstration Model. 16

CAD computer aided design. 29

CFD computational fluid dynamics. 29

COTS commercial-off-the-shelf. 14, 20–26, 28–32, 34–37, 94

CSIRO Commonwealth Scientific and Industrial Research Organisation. 2

DC direct current. 18

EMI electromagnetic interference. i, 11, 12, 14, 20, 29, 46, 47, 93, 94, 96, 97

FPGA field programmable gate array. 54–56, 96

HartRAO Hartebeeshoek Radio Astronomy Observatory. 7

IP ingress protection. 14, 52

ISPO International SKA Project Office. 1, 2

ISSC International Square Kilometre Array Steering Committee. 1, 2

KAPB Karoo Array Processor Building. 10–12

KAT Karoo Array Telescope. 7

KAT 20 Karoo Array Telescope 20. 7

KAT 7 Karoo Array Telescope 7. 7

LNA low-noise amplifier. 10, 12, 15, 16

MeerKAT "meer" (more) Karoo Array Telescope. i, 6–11, 13, 15–17, 21, 94

MPO Multi-fiber Push On. 54

MTBF mean time between failure. 29

NRF National Research Foundation. 2, 7

OMT orthomode transducer. 9, 10

PCB printed circuit board. 47, 48, 54–57, 59, 60, 94–96

prepSKA preparation for Square Kilometre Array. 4

PSU Power Supply Unit. 17, 27, 31, 46, 47, 52, 64–66, 94

RF Radio Frequency. 17

RFCU Radio Frequency Conditioning Unit. 17, 20, 47, 49, 64, 67

RFI radio frequency interference. i, 6, 11, 12, 20, 29, 94–97

SAAO South African Astronomical Observatory. 6

SALT Southern African Large Telescope. 6

SAST South African Standard Time. 21

SCG Sample Clock Generator. 17, 49, 61, 63, 67

SFP+ small form-factor pluggable. 54

SKA Square Kilometre Array. i, 1–7, 95

SKA SA Square Kilometre Array South Africa. i, 5, 7, 10, 20, 93

SSEC SKA Science and Engineering Committee. 2

TDP total dissipated power. 21

TIM thermal interface material. 93, 96, 97

UK United Kingdom. 2

URSI International Union of Radio Science. 1

US United States. 2

USA United States of America. 1

VLBI Very Long Baseline Interferometry. 2

XDM Experimental Development Model. 7

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Chapter 1

Introduction

1.1 SKA and the SKA Organisation

The Square Kilometre Array (SKA) is a global project focused on building the world's most sensitive radio telescope. This telescope is being built to answer the fundamental questions about the Universe, namely its origin and evolution. It is one of the most ambitious science projects in history and requires collaboration among policy-makers, engineers and scientists from around the globe if it is to succeed. It is envisioned that the SKA will eventually consist of thousands of dishes and near a million antennae that would collectively create over a square kilometre of collecting area. This would allow the instrument to observe and survey the sky faster and in finer detail than is currently possible with existing radio telescopes anywhere else in the world [1].

1.1.1 SKA Organisation

The idea to build the SKA was first conceptualised in 1991, with the International Union of Radio Science (URSI) establishing the Large Telescope Working Group in September 1993. Its aim was to initiate an international drive to develop scientific goals and technical specifications for a cutting-edge radio observatory. The meetings held by this working group provided a forum for debating the technical research needed for organising the multi-national scientific community to work jointly toward achieving this common goal. By 1997 eight institutions from six countries (Australia, Canada, China, India, the Netherlands, and the USA) signed a Memorandum of Agreement to collaborate on a technology study programme culminating in a very large radio telescope.

The International Square Kilometre Array Steering Committee (ISSC) was created on 10 August 2000 in a Memorandum of Understanding signed at the International Astronomical Union meeting in Manchester, United Kingdom. This was signed by delegates from eleven countries, namely Australia, Canada, China, Germany, India, Italy, the Netherlands, Poland, Sweden, the United Kingdom, and the United States.

The above agreement was superseded by the Memorandum of Agreement to Collaborate in the Development of the Square Kilometre Array on the 1st of January 2005, allowing the ISSC to grow to 21 members (7 each from Europe, USA and the rest of the World) and establishing the International SKA Project Office (ISPO).

In anticipation of the growth of the ISPO, the ISSC called for site proposals to host the Project Office in 2007. A Memorandum of Agreement was signed in October 2007 between the ISSC and the University of Manchester allowing the Project Office to move to the new Alan Turing building in Manchester. The building also housed the Jodrell Bank Centre for Astrophysics.

Figure 1.1: The Alan Turing Building at the University of Manchester[2].

Drawn up in 2007 and coming into effect on 1 January 2008, a new International Collaboration Agreement for the SKA Programme was signed by the European, US, and Canadian SKA consortia, the Australian SKA Coordination Committee, the National Research Foundation in South Africa, the National Astronomical Observatories in China, and the National Centre for Radio Astrophysics in India. It ratified the role of the SKA Science and Engineering Committee (SSEC), which would replace the ISSC. The SSEC serves as the primary medium for debate and decision making on all scientific and technical topics for the SKA amongst the signatories of the International Collaboration Agreement.

A second agreement to establish the SKA Program Development Office was also drafted in 2007 and became effective on 1 January 2008. It afforded a structure to globalise the technology development and design effort of the SKA. This agreement was signed by the Commonwealth Scientific and Industrial Research Organisation (CSIRO) Australia Telescope National Facility, University of Calgary, Cornell University, the Joint Institute for Very Long Baseline Interferometry (VLBI) in Europe, and the National Research Foundation (NRF) in South Africa. This office would be funded by all signatories to the agreement, with a common fund allowing it to finance its activities.

Currently the "SKA Organisation" is legally a non-profit company that manages the SKA Project. It was founded in December 2011 to solidify the exchanges between international parties and to centralise leadership of the project. The company is a private UK company limited by guarantee. This means that the company does not have share capital or shareholders, but has members who are guarantors (with limited liability) instead of shareholders. The guarantors give an undertaking to

contribute a nominal amount should the company close down. Directors of the Board are appointed by the members.

In November 2012, due to a rapid increase in the number of employees, the offices relocated from the Alan Turing Building at the University of Manchester to a newly constructed building at the Jodrell Bank Observatory in Cheshire, England [3].

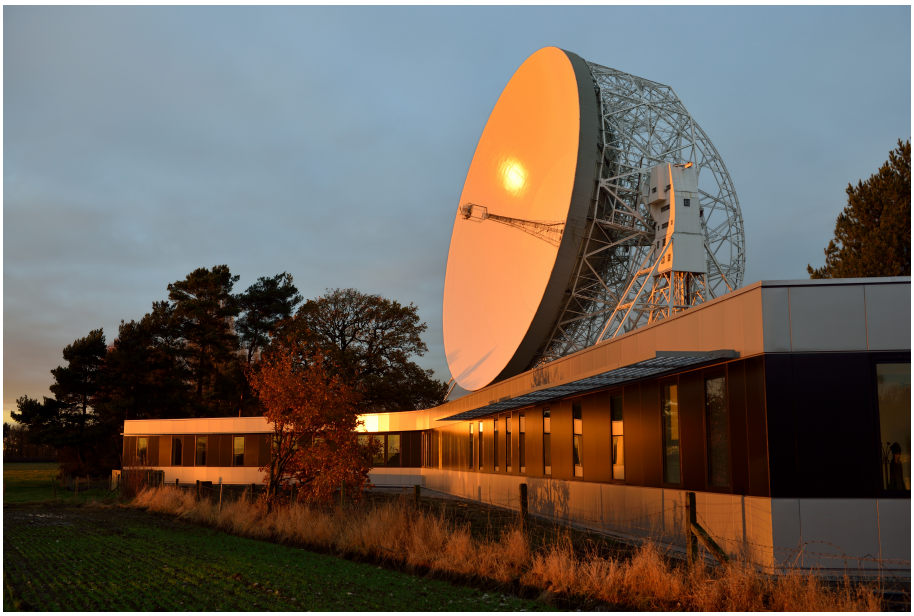


Figure 1.2: SKA Organisation Headquarters, at Jodrell Bank Observatory near Manchester, England. The Lovell Telescope is seen in the background [4].

The SKA collaboration currently consists of 10 member nations (formerly 11), namely:

- Australia: Department of Industry and Science
- Canada: National Research Council
- China: National Astronomical Observatories of the Chinese Academy of Sciences
- Germany: Federal Ministry of Education and Research (withdrew in June 2015)
- India: National Centre for Radio Astrophysics
- Italy: National Institute for Astrophysics
- New Zealand: Ministry of Economic Development
- South Africa: National Research Foundation
- Sweden: Onsala Space Observatory
- The Netherlands: Netherlands Organisation for Scientific Research
- United Kingdom: Science and Technology Facilities Council

There are currently 10 partner countries and roughly 100 organisations within them involved in the design and development of the project [5]. Germany was previously a member but withdrew from the project at the end of June 2015.

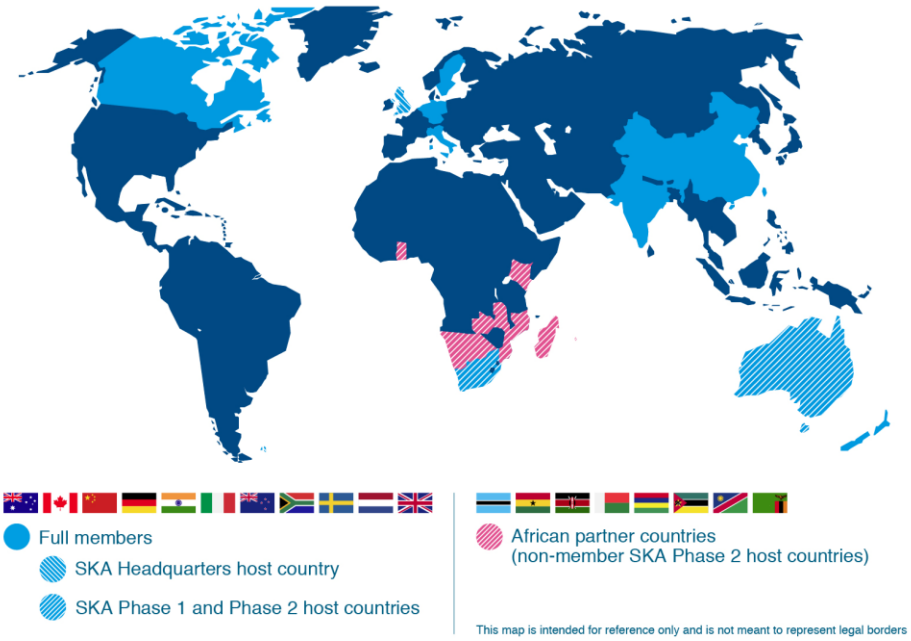


Figure 1.3: SKA Member and Partner Countries [6].

1.1.2 SKA Time-line

The SKA was first conceptualised in 1991 and an international working group was created in 1993. This group spearheaded the signing of the first Memorandum of Agreement in 2000. The next few years to 2006 saw a substantial amount of development work to identify a list of potential sites. prepSKA was formed in 2008; its goal was to make the SKA Organisation a legal entity, which it achieved in 2011. The site bid and selection process ran through 2011 and 2012, when two sites in Australia and South Africa were chosen. Research proposal requests were called for, received and evaluated in 2013. At the same time the cost ceiling of the project was established.

SKA Phase 1 Construction is scheduled to occur from 2018 to 2023. Scientific observations in this phase are envisaged to commence in 2020. Phase 1 will establish an operational array of telescopes of roughly 10% of the capacity of the completed array allowing useful observations to be made by the science community.

SKA Phase 2 Construction is scheduled to take place from 2023 to 2030 [7] and will consist of antennae with a combined collection area of one square kilometre. The SKA project timeline is illustrated schematically in Figure 1.4.

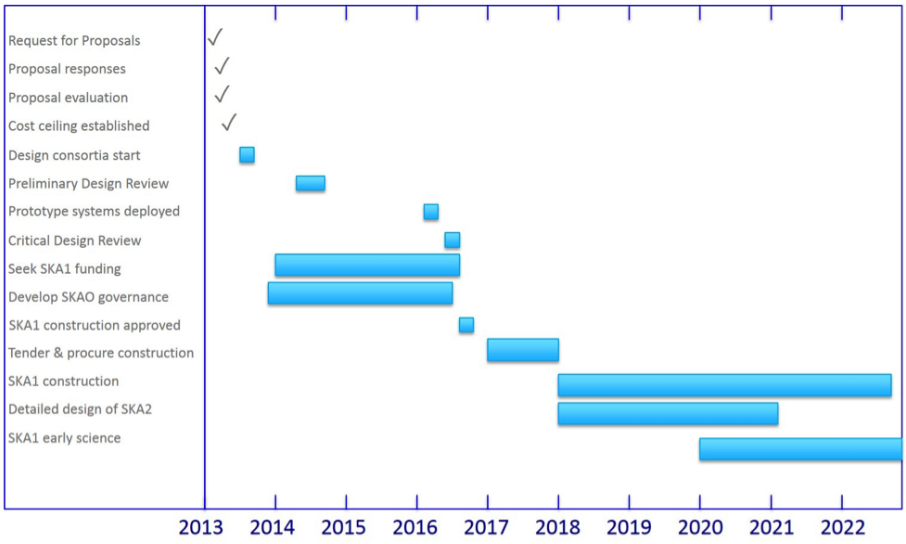


Figure 1.4: SKA Project timeline [8].

1.2 Square Kilometre Array South Africa (SKA SA)

The decision to make astronomy a prime focus area in South Africa's science and technology landscape can be attributed to the white paper on Science and Technology prepared in 1996 by the South African Government, as well as the 2002 National Research and Development Strategy prepared by the Department of Science and Technology. The 1996 white paper contained a statement of intent to have fundamental scientific research as a focus; astronomy is specifically referenced in the document:

> *"Scientific endeavour is not purely utilitarian in its objectives and has important associated cultural and social values. It is also important to maintain a basic competence in flagship sciences such as physics and astronomy for cultural reasons. Not to offer them would be to take a negative view of our future - the view that we are a second class nation, chained forever to the treadmill of feeding and clothing ourselves."* [9]

Building on this an excerpt from the 2002 national R&D strategy sums up the reason for the focus on astronomy:

> *"One way to achieve national excellence is to focus our basic science on areas where we are most likely to succeed because of important natural or knowledge advantages. In South Africa, such areas include astronomy, palaeontology and indigenous knowledge."* [9]

The South African Department of Science and Technology's Strategic Plan (2011–2016), and its ten-year plan (2008–2018), with specific goals being set for astronomy put the above strategy into effect:

> *"In growing its knowledge base, South Africa also needs to build on its niche strengths, especially those in which it has a geographic or natural*

advantage, such as astronomy, biodiversity, Antarctic research, minerals processing and palaeontology... ...become the preferred destination for major astronomy projects and associated international investment in construction and operations... construct a powerful radio astronomy telescope and use it for world-class projects... " [9]

The following strategy was devised [9]:

1. Identify, and protect, an ideal location for the core of the SKA - a site that has the combined attributes of a low radio frequency interference (RFI) environment, ready access to infrastructure, and a benign climate.

2. Demonstrate the suitability of the site for radio astronomy by constructing South Africa's precursor telescopes on the site, and making the site available to other radio astronomy experiments.

3. Demonstrate South Africa's ability to design, construct, operate and maintain a radio astronomy facility, and the associated infrastructure.

4. Employ a risk-reducing, system engineering approach to ensure that the MeerKAT, once fully constructed and operating, delivers the best science results possible.

5. Align the MeerKAT design with SKA technologies, for easy integration with the SKA.

6. Align the MeerKAT science objectives with the SKA, and listen to what the local and international radio astronomers need from the MeerKAT.

7. Design infrastructure to be scalable for the SKA.

8. Pave the way for radio astronomy science and engineering capacity development and infrastructure, in Africa, through the construction of a network of radio telescopes on the continent.

9. Use the excitement of the SKA and MeerKAT to attract young people into science and engineering studies.

10. Create large and dynamic radio astronomy research groups in African universities.

11. Showcase Africa's talent, and ability to deliver, to attract internationally recognised scientists to work with, and in Africa.

12. Employ the best and brightest to work in the South African SKA Project.

13. Retain support by delivering MeerKAT and the associated infrastructure within schedule and budget, and to specification.

During a conference held at the South African Astronomical Observatory (SAAO) in the early 2000's the idea to participate in SKA was formulated; initially only to offer the site and infrastructure to the project. At this time the Southern African Large Telescope (SALT) was being completed and it was decided that South Africa should expand into radio astronomy. No longer would it just provide the site and

infrastructure, but actual working telescopes were to be designed and built locally. The initial concept was a 20-antenna array of $15m$ dishes to be called the Karoo Array Telescope 20 (KAT 20). A team of scientists and engineers started work on this at the Hartebeeshoek Radio Astronomy Observatory (HartRAO) from 2006/2007. An experimental development model called XDM, consisting of a single $15m$ dish was designed and constructed by the end of 2007 to test the dish design and manufacturing procedures for the Karoo Array Telescope (KAT).

The Square Kilometre Array South Africa (SKA SA) business unit was formed as a subsidiary of the National Research Foundation (NRF) in early 2008 and the Karoo Array Telescope 7 (KAT 7) design was finalised. This precursor was to be an engineering test bed to demonstrate South Africa's technical capability to the world.

The first two antennae were completed and tested just before Christmas 2009 (called Fringe Finder). The remaining five dishes were completed by December the following year and have worked so well that KAT 7 has been used for actual science ever since it was commissioned. The first two papers published using KAT 7 were "A return to strong radio flaring by Circinus X-1 observed with the Karoo Array Telescope test array KAT-7"[10] and "KAT-7 science verification: Using HI observations of NGC3109 to understand its kinematics and mass distribution"[11]

MeerKAT (a play on words from a small carnivoran belonging to the mongoose family and the Afrikaans word "meer" which means "more", i.e. "more KAT") was conceptualised in late 2010/early 2011 as a precursor array which could be integrated into the mid-frequency component of SKA Phase 1. It would consist of sixty-four, $13.5m$ offset Gregorian, interlinked receivers/dishes when completed. The first antenna was installed in March 2014 and qualified by July 2014. Since then, more antennae have been completed.

On the 25th of May 2012 the decision on which country would host the SKA was announced by the International SKA Organisation. It was decided that the SKA would make use of the infrastructure of both South Africa and Australia. In Phase 1 the sixty-four dish MeerKAT precursor array would be integrated into SKA and an additional 190 mid-frequency dish-shaped antennae, each about $15m$ in size, will be built to supplement them. In Phase 2 a further three thousand mid-frequency dishes will be constructed. The majority of these will be located in the Northern Cape, South Africa. Other African countries, namely Namibia, Botswana, Zambia, Mozambique, Kenya, Ghana, Madagascar and Mauritius will host the rest of the dishes. In addition, a large number of flat mid-frequency antennae, each about $60m$ in diameter will be constructed in the Northern Cape.

1.3 Radio Telescopes

Radio telescopes are utilised to analyse and study naturally occurring radio waves from astronomical bodies, including stars and galaxies. Radio telescopes are useful to observe objects which can't be seen in the visible spectrum (Figure 1.6). However, the radio waves from these objects are extremely weak when they reach the Earth as they have travelled extremely long distances before reaching us.

A radio telescope looks like a large satellite dish and consists of several main elements, namely: a dish and antenna, a receiver, a detector, and an analyser (see Figure 1.7).

Figure 1.5: MeerKAT antennae. [12]

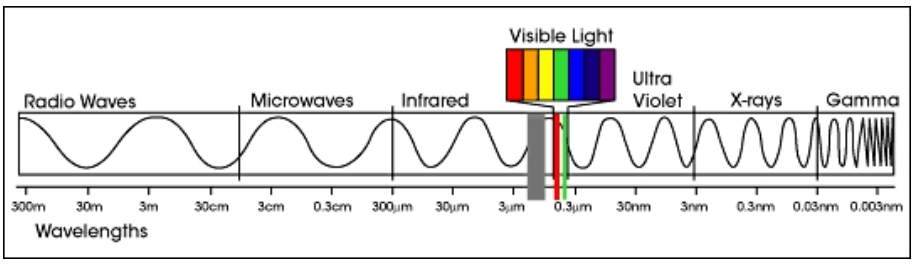


Figure 1.6: The electro-magnetic spectrum. [13]

Dish (Reflector) and Antenna (Sub-reflector) - The dish reflects and focuses the radio waves towards the antenna. The larger the dish, the more it reflects and hence focuses a stronger signal on the antenna. It is therefore desirable to build the largest dish possible. At $500m$ in diameter, the Aperture Spherical Telescope (FAST) in China is the largest single-dish telescope in the world. Unfortunately the cost of the dish increases exponentially with increase in size. A larger dish would require a larger and stronger mount to support its increased size, weight and the wind load it would experience. Larger motors would be required to drive it. These motors would require more power to operate and hence would consume more electricity. Finally there are technological limitations in mechanical structure size with today's material and engineering abilities - evidence of this was seen in the collapse of the 300 foot ($90m$) Green Bank Telescope at 9:43 p.m. EST on Tuesday the 15th of November 1988 (see Figure 1.8). The main support for the antenna, a large gusset plate in the box girder assembly, suddenly failed and the entire telescope collapsed. If the dish is not required to be steerable, it can be made larger than steerable dishes.

To address the limitations in dish size astronomers combine data from many smaller dishes and antennae together to form a single image. This is called aperture synthesis.

Receiver - The receiver converts the radio waves received by the antenna into electrical signals. To do this it has to be very sensitive; that is, it must have very low noise levels. This is achieved by cooling the receiver to very low temperatures ($< 123K(150°C)$). At cryogenic temperatures the atomic vibration of matter in the receiver, which is responsible for most of the noise, is decreased significantly.

Detector - Once converted to an electrical signal by the receiver, the strength

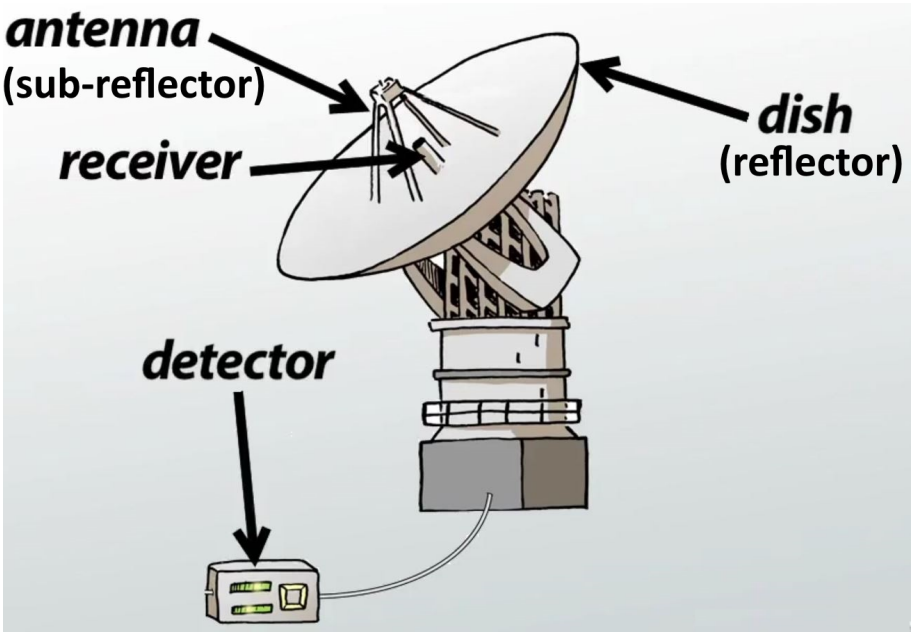
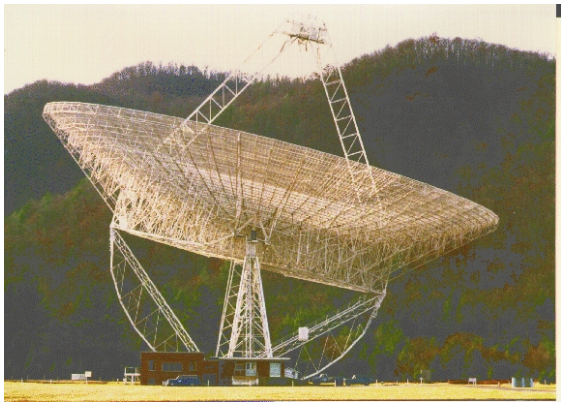


Figure 1.7: Parts of a radio telescope. [14]



(a) Green Bank 300 Foot Telescope before. [15]

(b) Green Bank 300 Foot Telescope after.[15]

Figure 1.8: Collapse of the Green Bank 300 Foot Telescope.

of the signal or power density is measured by the detector for imaging. The stronger the signal the brighter a particular point in the image will be.

Analyser - The Analyser creates an image through the process of aperture synthesis from the visibilities measured by interferometric baseline pairs. This operation is usually performed by a computer. [14]

1.4 General design of the dish

The MeerKAT radio telescope consists of sixty-four dishes in an offset Gregorian configuration. The advantage of this configuration is that the receiver and sub-reflector do not hang over the main reflector surface itself which would block some of the radio waves.

The signal path for MeerKAT is as follows: Reflector, sub-reflector, horn, or-

thomode transducer (OMT), low-noise amplifier (LNA), digitiser, switch, fibre, correlator, science data processor. The electromagnetic/radio wave strikes the main reflector/dish and is redirected to the sub-reflector. This in turn reflects the wave onto the receiver.

On MeerKAT the receiver consists of the horn, OMT, LNA and Digitiser (conventionally, the Digitiser is not considered part of the receiver). The horn collects and focuses the radio waves into a waveguide for receiving the signal. The OMT converts the electromagnetic wave into a radio frequency voltage signal and separates it into the horizontal and vertical polarisations. The radio frequency voltage signal is then amplified by the cryogenically cooled LNA, which adds very little noise to the signal. Finally the Digitiser converts the analog radio frequency voltage signal to a digital signal. This conversion is performed by an analog-to-digital converter (ADC) located within the Digitiser itself. Each receptor will have four different receivers for different, useable portions of frequency ranges, namely L-Band ($900MHz - 1670GHz$), UHF Band ($580MHz - 1015GHz$), S-Band ($1670GHz - 3.2GHz$) and X-Band ($8GHz - 14.5GHz$).

Figure 1.9: SKA SA MeerKAT Offset Gregorian Reflector. [16]

Once converted to a digital signal, the data is sent by the Digitiser to the correlator via buried fibre optic cables. This is located several kilometres away inside the Karoo Array Processor Building (KAPB) at the Losberg Site Complex.

Once at the KAPB, the signal is digitally processed through various stages. Two examples of this are correlation, which is where the signals from various receptors are combined together to form an image of an area of sky at which the receptors are pointing, and beam forming; this coherently adds signals from various receptors to

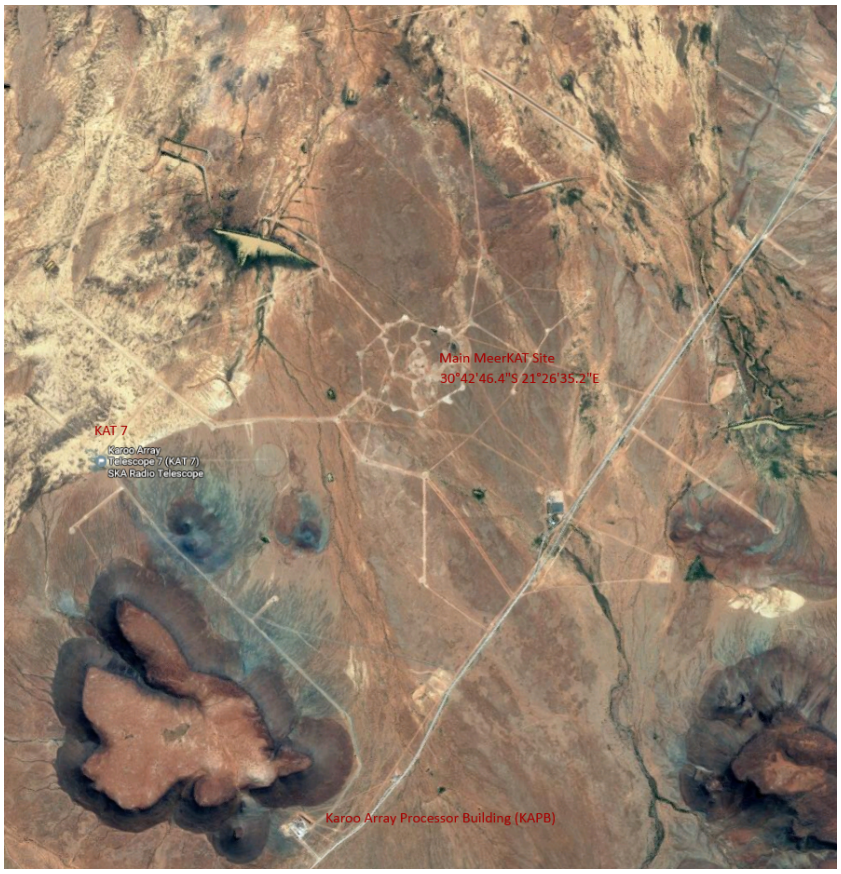


Figure 1.10: The MeerKAT site at $30°42'46.4"S$ $21°26'35.2"E$. The elements of the array are on the light brown circles. [17]

form a number of narrow, high sensitivity beams used in pulsar science. The KAPB is also a storage archive for some of the science data generated by MeerKAT.

1.5 Challenge with present placement of the Digitiser in the MeerKAT telescopes

The Digitiser system is traditionally housed in the pedestal of the radio telescope antenna structure. This is done to minimise the risk of contamination of the radio frequency signal by the electronics within the Digitiser itself. The pedestal is well shielded and significantly attenuates any escaping electromagnetic interference (EMI)/radio frequency interference (RFI) signal generated from within as well as protecting equipment inside from electromagnetic noise from outside. When there is flow of current in an electrical circuit an electromagnetic field or wave is generated (Faraday's Law of Induction). If the flow of current ceases or reverses polarity the electromagnetic wave collapses. Alternating current and digital electronics switching on and off create these magnetic waves. The growth and decay of the magnetic field generates electromagnetic waves which propagate into space. When these electromagnetic waves pass through a metal object, a secondary current is induced within that object. If that object were to be the receiver, or on the signal path of the radio telescope, it would receive signal noise which would degrade the quality of the signal of interest.

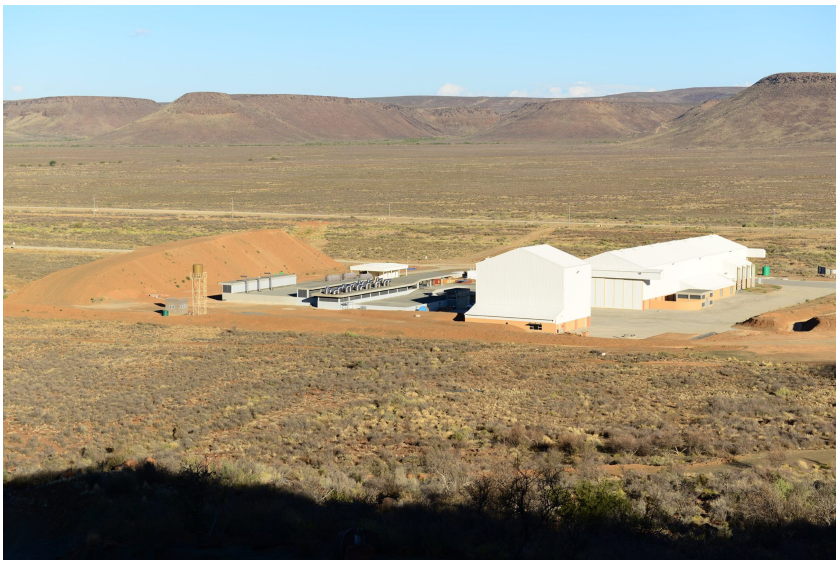


Figure 1.11: The Karoo Array Processor Building (KAPB) (to the left of the white integration buildings) at the Losberg Site Complex. [17]

Digital electronics have largely replaced their analog counterparts - they are cheaper to produce and easier to design with as there are fewer components utilised. They do however rely on the switching on and off of signals to function. This switching generates electromagnetic waves (albeit small) as explained above. The radio waves of interest to astronomers lie in the frequency range $3kHz$ to $300GHz$. If the electronics in the Digitiser operate within the frequency range of the signal to be digitised itself the signal could be contaminated by the electronics. The signals observed by radio astronomers are incredibly weak (as an example a cell phone signal is a billion billion times stronger than the signal received by a radio telescope) and as a result are completely lost in the noise generated by the electronics.

The downside to placing the Digitiser in the pedestal is that phase instability (inductive and capacitive properties of copper wire), as well as gain slope (different gains at different frequencies) and copper losses (resistance of the copper wire) would be present as a result of the long copper co-axial cable run from the LNA at the feed to the Digitiser in the pedestal.

Placing the Digitiser near the feed would address the above problem as there would be a digital signal path from near-feed to the correlator. A digital signal is effectively a string of on and off or one and zero pulses at a known frequency which is interpreted as a binary number by the receiving "system". Part of the binary message also contains information to let the receiver know if the signal is contaminated. Usually, unless the electromagnetic interference (EMI)/radio frequency interference (RFI) noise coupling on the signal path is constant and large, the digital signal would be immune to the noise as the receiver only needs to know if the signal is on or off. The fibre cable would decrease the likelihood of the losses even further as it is immune to electromagnetic interference (EMI)/radio frequency interference (RFI) noise as it is not made of an electrically conductive material. The downside to this is the potential of radio wave signal contamination from the Digitiser electronics as explained above. With the Digitiser so close to the feed utmost care must be taken to ensure that this does not occur.

1.6 The importance of good thermal design

The only way to EMI/RFI shield the Digitiser electronics effectively is to place it in a completely sealed conductive box. This has been shown to effectively dampen electromagnetic interference from escaping. In practise this is difficult to implement for several reasons, namely:

1. Power and signal cables still need to enter and leave the enclosure, creating apertures for electromagnetic waves to escape.

2. The electronics need to be inserted into the enclosure and hence require an opening or lid which would create further avenues for electromagnetic interference to escape (there is still a gap between a lid and base through which electromagnetic waves can escape).

3. Corrosion of the metallic enclosure decreases its conductivity, especially on mating surfaces.

4. Electronics generate heat which needs to be dissipated to the surrounding atmosphere. Forced convection(fans) require apertures in the enclosure for convecting air to enter and leave and themselves generate electromagnetic noise (from brushes and slip rings in DC motors and alternating current in induction motors).

5. Thermal loading by the sun on the enclosure surface adds to the heat load, which creates further problems.

The first three issues can be overcome by treating all surfaces with electrically conductive and corrosion resistant coatings as well as special gasketing between mating surfaces, which effectively creates contiguous surfaces. Treating the heat dissipation problem is more tricky as one is reduced to using conduction and natural convection (and a small amount of radiation) alone for heat dissipation. Special care is required to effectively conduct heat through the Digitiser chassis to the surface and then naturally convect that heat away. Furthermore solar shielding is required to mitigate solar loading which could heat the chassis up and decrease its effectiveness in dissipating the heat generated by the electronics.

A passively cooled, near feed Digitiser has not been successfully built in the past.

1.7 Thesis objectives

The aim of this dissertation is too present the thermal design of an externally, near feed mounted, passively cooled Digitiser for the MeerKAT Radio Telescope. The Digitiser design should meet the following thermal and mechanical requirements:

1. The Digitiser should be able operate between a minimum and maximum ambient air temperature of $-10°C$ and $40°C$ respectively.

2. The case temperature of critical electrical components is to remain below $85°C$ to ensure safe operation.

3. The Digitiser should provide $100dB$ of electromagnetic interference (EMI) shielding.

4. The Digitiser should fit the geometrical envelope of $600mm$ x $400mm$ x $350mm$.

5. The Digitiser should weigh less than $40kg$ and should be easily handled by one person. [18]

At the start of this project no Digitiser had been built which, when placed near feed, would not contaminate the incoming radio signal.

1.8 Layout of this dissertation

This dissertation is structured as follows. Chapter 2 details the problem overview, reviews the Digitiser subsystem and Digitiser design requirements. A simple geometrical model of a commercial-off-the-shelf (COTS) enclosure is introduced, first-order thermal estimates are calculated and a thermal simulation of the model is run. When the model fails to meet the thermal requirements, a custom designed enclosure is investigated. Once again first-order thermal estimates are calculated and thermal simulations are run. Following this heat-sinks and a solar shield are incorporated into the conceptual design.

Chapter 3 documents the actual mechanical design of the conceptual Digitiser enclosure, including the placement of major components, the overall dimensions, enclosure weight, solar shield design, ingress protection (IP), sealing for EMI prevention, mounting interfaces, major component mechanical design and a thermal simulation of the full system.

In Chapter 4 an overview of the Digitiser being tested in a thermal chamber is described with the test results graphed. On-site temperature logs are also graphed and these values are compared to the thermal simulations to validate them.

In Chapter 5 a brief summary of the design process is presented and recommendations are given for future work and for practitioners working in this field.

Chapter 2

Conceptual thermal design of the MeerKAT Digitiser

2.1 Problem overview

The MeerKAT Digitiser is a critical part of the MeerKAT radio telescope array. The primary function of the Digitiser is to convert the pre-conditioned wide-band radio analog feed signal (both vertical and horizontal polarisations), independently, from a cryogenically cooled low-noise amplifier (LNA) which is co-located on a rotating feed indexer platform, to a digital signal. An illustration of a MeerKAT antenna is shown in Figure 2.1.

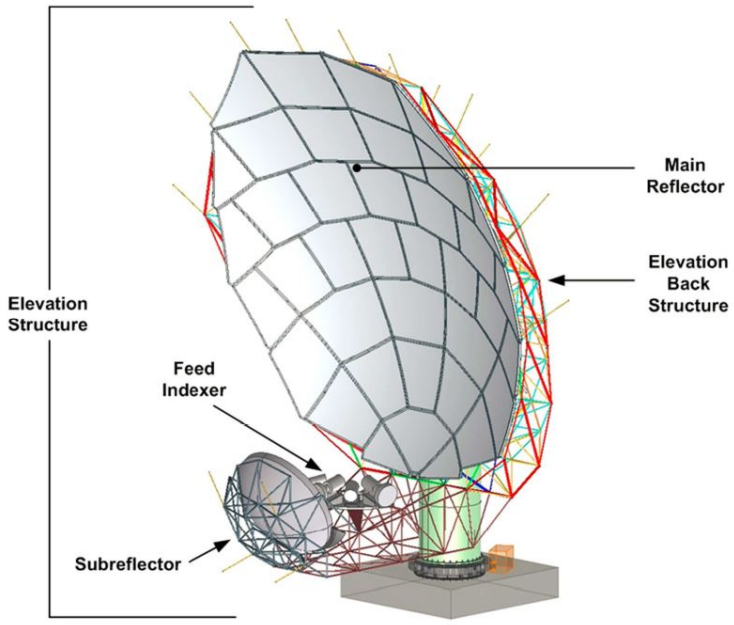


Figure 2.1: Illustration of a MeerKAT antenna, showing the feed indexer platform's location. [18]

The feed indexer platform is shown in more detail Figure 2.2. The MeerKAT digitiser will require operation in hostile environmental conditions, with direct exposure to extremes of temperature, solar radiation, dust and occasional rain. As the site is remotely located with the antennae being situated far apart and 256 Digitisers

in operation, maintenance requirements for these units over their service life (which may exceed 30 years) should be minimised. [18]

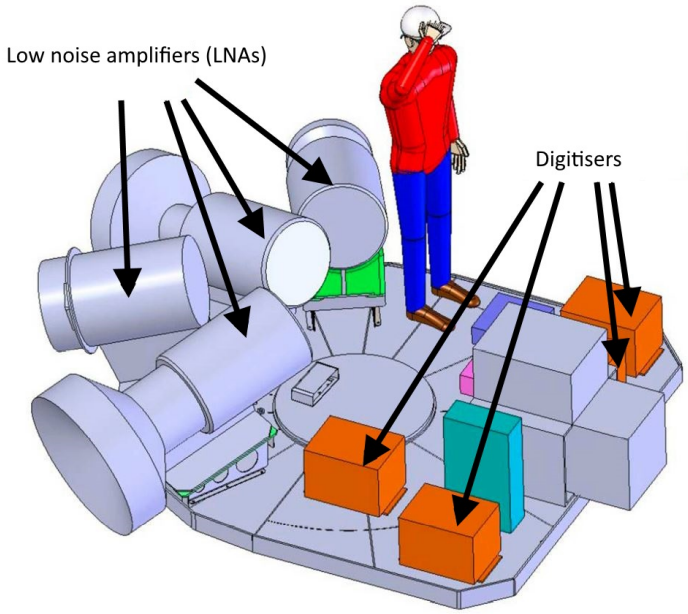


Figure 2.2: Feed indexer platform, showing the positions of the LNAs and Digitisers on the platform. [18]

The digital outputs from the four Digitisers are sent over four 10 Gb fibre-optic ethernet links. Four different frequency bands have been chosen to be observed by the MeerKAT array and hence four separate Digitisers will be required, one for each band. These are:

- UHF band: $580 - 1015MHz$
- L-band : $900 - 1670MHz$
- S-band: $1.67 - 3.2GHz$
- X-band: $8 - 14.5GHz$

The MeerKAT antennae are located near Carnarvon in the Karoo (see Figure 2.3). The location of the Digitiser on the feed indexer platform carries a high risk of radio frequency interference emerging from the Digitiser enclosure and contaminating the receiver signal. The minimum level of EMI/RFI shielding required by the enclosure has been determined experimentally from the Digitiser Advanced Demonstration Model (ADM) to be 90 dB.

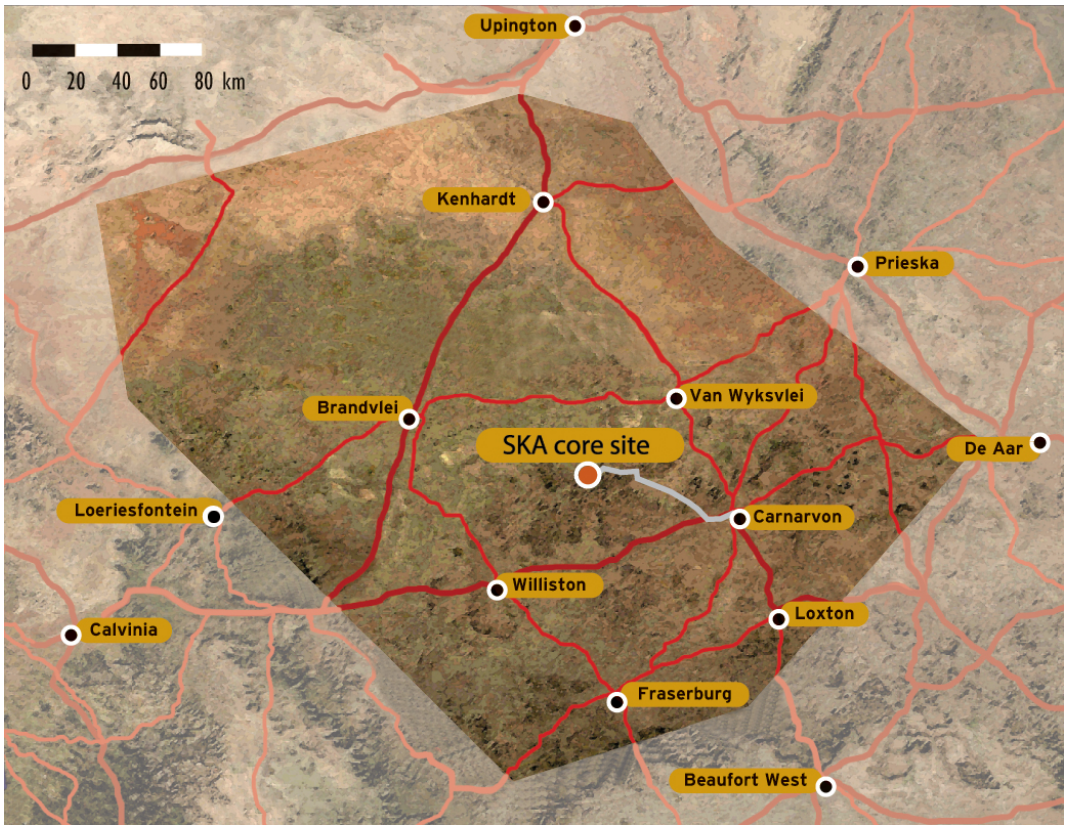


Figure 2.3: MeerKAT telescope array location near Carnarvon. [19]

2.2 Digitiser sub-system overview

A block diagram of the Digitiser system is shown in Figure 2.4. The horizontally and vertically polarised antenna feeds entering the Digitiser pass through interfaces IF1 and IF2, respectively, to two Radio Frequency Conditioning Unit (RFCU) modules. These serve to pre-condition the Radio Frequency (RF) signals by allowing the selection of band-specific frequencies and by adding programmable gain. The Radio Frequency Conditioning Units pass the conditioned Radio Frequency signals to the analog-to-digital converter modules through interfaces 3 (IF3) and 4 (IF4). The analog-to-digital converter modules convert the conditioned Radio Frequency signals from analog to digital signals using sampling clocks provided by the Sample Clock Generator (SCG) on interfaces 22 (IF22) and 23 (IF23). The digitised signals undergo electrical-to-optical conversion before being passed optically via interfaces 5 (IF5) and 6 (IF6) to the so called "D-Engine". The D-Engine converts the optical analog-to-digital converter outputs back to an electrical signal, performs necessary pre-processing, and packetizes the sampled spectrum along with meta-data. The D-Engine accepts a 1 pulse-per-second optical input over interface 10 (IF10), and provides an optical noise diode control output to allow for external receiver calibration on interface (IF9). Control and monitoring of the Radio Frequency Conditioning Unit and analog-to-digital converter modules by the D-Engine is implemented through optical interfaces IF18, IF19, IF20 and IF21. The D-Engine provides this data as an output of the Digitiser over multiple fibre-optic $10Gb$ Ethernet links (IF7). The Sample Clock Generator accepts a reference clock over a fibre-optic interface (IF8) that is used to drive the sampling clocks. The Power Supply Unit module ac-

cepts universal AC input power from the Digitiser's external interface and supplies conditioned DC power to the other modules. [18] [20]

2.3 Design requirements

The operational design requirements for the Digitiser system with respect to thermal performance are as follows:

- Temperature extremes - The Digitiser housing shall survive without the degradation of environmental or RFI seals when exposed to temperatures of $-5°C$ and $+50°C$ respectively for a maximum continuous period of 16 hours at each temperature.
- Operational Temperatures - The Digitiser housing shall provide thermal relief to the internal components allowing them to function correctly up to $40°C$ ambient temperature.
- Solar irradiation - The Digitiser housing shall sustain no deformation of material, deformation of the surface finish or change in colour while being exposed to the UV portion of the sunlight spectrum as defined in the ETSI EN 300019-2-4 V2.2.2 standard.
- Digitiser mass - The Digitiser mass shall not exceed 40 kg. [18]

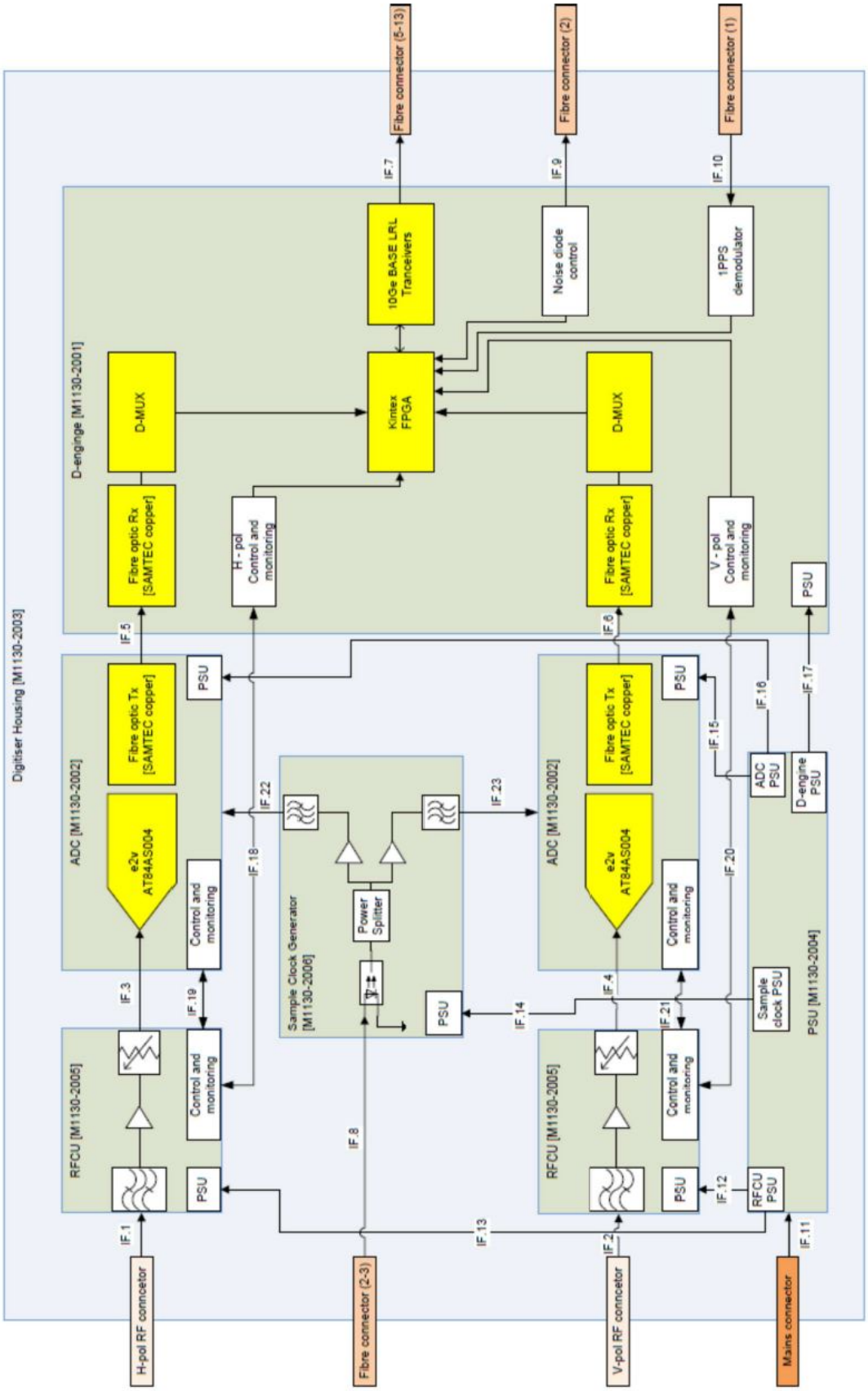
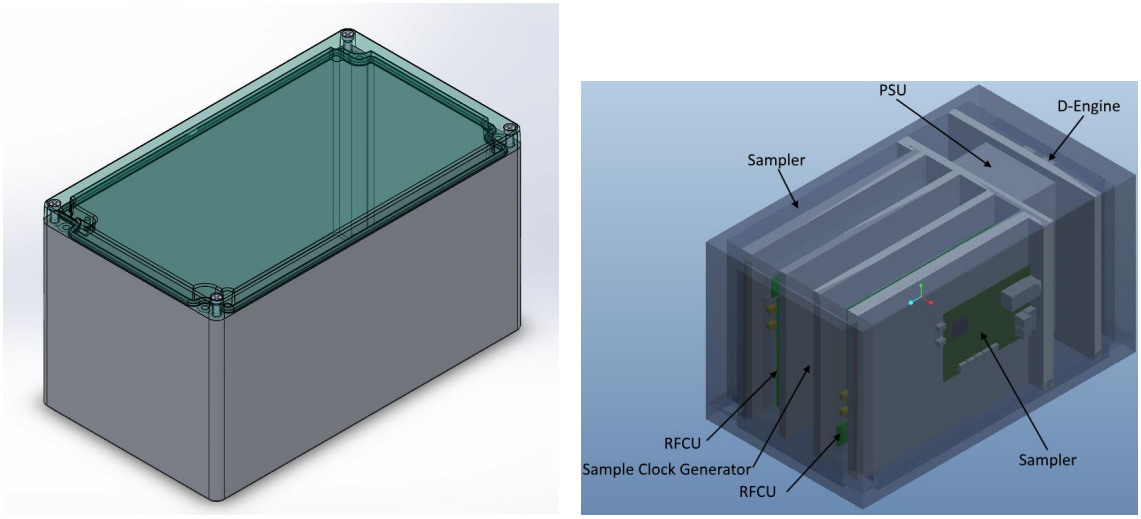


Figure 2.4: Block diagram of Digitiser. [18]

2.4 Thermal analysis of a simple geometrical model Digitiser enclosure ("COTS enclosure concept")

Design work had already been performed on a prototype RFCU module when the design for the mechanical enclosure commenced. SKA SA had already developed similar technology for both the D-Engine and ADC/sampler module. These pre-existing electronic designs were incorporated into an initial concept design for the Digitiser. In the hope of minimising development cost and time a commercial-off-the-shelf enclosure which would meet RFI requirements (100 dB of attenuation) and fit all the components was investigated as a possible solution for the Digitiser enclosure - if the components housed within could be maintained at a safe temperature during operation.

The commercially available 01.23 40 23 aluminium industrial enclosure manufactured by ROSE Systemtechnik GmbH (see Figure 2.5a) was found to be a good starting point. This is an aluminium die cast enclosure with pre-cut grooves in it. This allowed electromagnetic interference/radio frequency interference gasketing with $100dB$ of attenuation to be fitted.



(a) ROSE Systemtechnik GmbH 01.23 40 23 RFI enclosure.

(b) Early Digitiser concept in a ROSE Systemtechnik GmbH 01.23 40 23 enclosure.

Figure 2.5: Preliminary Digitiser enclosure concept based on the available COTS Rose enclosure.

The enclosure was sub-divided into seven compartments with aluminium walls with similar existing electronic modules placed within them as shown in Figure 2.5b. The hottest modules, namely the D-Engine and ADC/sampler modules, were placed nearest a surface as shown in Figure 2.5. The layout was also made symmetrical to ensure that the duplicate modules, RFCUs and ADC/samplers for the horizontal and vertical polarisations would have the same heat distribution across them.

2.5 First-order thermal estimate calculation for the COTS enclosure concept

To establish whether utilising a commercially available Rose enclosure would be feasible, thermal calculations and simulations were performed on a simplified geometric model of the Rose enclosure. The model would need to maintain a steady-state temperature within safe component operating limits at $40°C$ ambient temperature, with solar radiation, using natural convection, while dissipating between 95 and $125W$ (as determined by an electrical engineer responsible for hardware design). Forced convection was undesirable as it could potentially introduce electromagnetic interference from fan motors.

To calculate the first-order thermal estimate, the following parameters were used. The physical dimensions of the conceptual enclosure were taken to be:

$$Length_{Enclosure} = 400mm,$$

$$Width_{Enclosure} = 230mm,$$

$$Height_{Enclosure} = 225mm.$$

The expected total dissipated power (TDP) for the Digitiser is estimated to be:

$$95W \leq TDP \leq 125W$$

The MeerKAT's maximum ambient operating temperature from the requirements is specified to be:

$$T_{ambient} = 40°C.$$

2.5.1 Heating as a result of solar radiation

As the Digitiser is located outdoors, it will be further heated by solar radiation.

Solar insolation

The MeerKAT site location is $30.721°S$, $21.411°E$. Solar radiation would be a maximum during the southern hemisphere summer solstice on 21 December at local solar noon, which would be approximately 13h00 SAST for the Northern Cape. For our purpose we can take an interval one hour before and one hour after local solar noon as the period of maximum intensity of the solar radiation (Figure 2.7). This period is likely to exceed the settling time to reach thermal steady-state for the Digitiser and hence the solar radiation value will be considered a constant.
For the first-order estimate, solar radiation, I, will be taken as the average solar radiation for a 2-hour period centered on local solar noon. This value is calculated to be:

$$I = 1.053\text{kWm}^{-2}$$

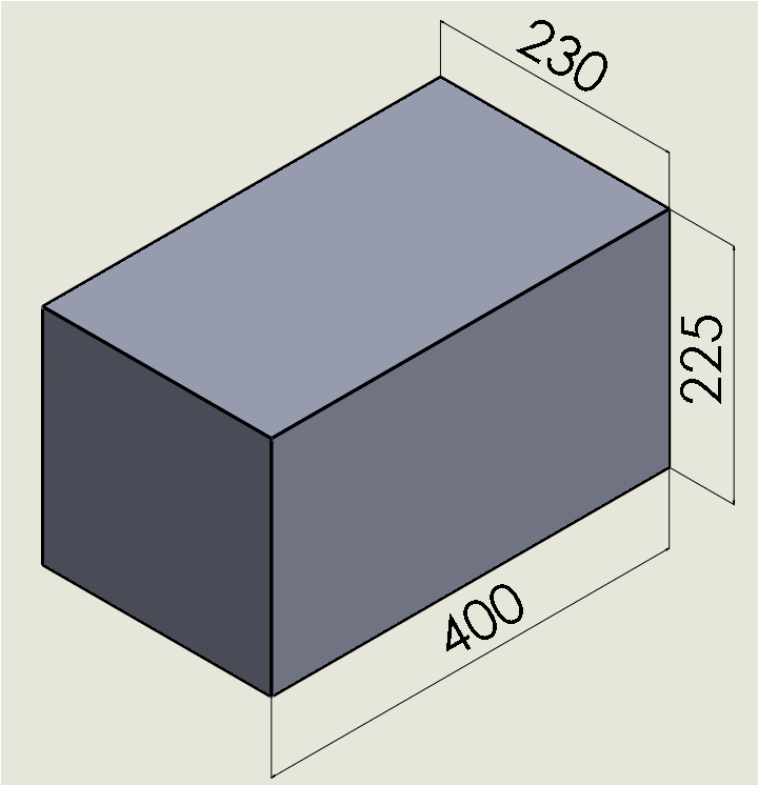


Figure 2.6: Simplified geometrical representation of the COTS Rose enclosure (the dimensions are in mm).

Surface treatment	Absorptivity α_s	Emissivity ε	Ratio α_s/ε
Aluminium film	0.09	0.03	3
Black anodised aluminium	0.78	0.86	0.91
Black paint on metal [22]	0.97	0.97	1
White paint on metal [22]	0.21	0.96	0.22

Table 2.1: Emissivity and absorptivity of various metal surface treatments. [22]

Emissivity and absorbtivity

The surface treatment of the Digitiser would need to maximise emissivity and minimise absorptivity. Table 2.1 shows the possible surface treatments and their effect on absorptivity and emissivity.
Incident radiation on the exposed Digitiser surface will result in a heating effect, known as solar loading. This solar loading value can be calculated as:

$$Q = \alpha A I$$

where Q refers solar loading (W), α refers to surface absorptivity, A refers to the surface area exposed to radiation (also known as the view factor)(m^2) and I refers to the solar radiation (W/m^2).

View factor

The view factor is defined as the projected surface area of an object perpendicular to incident radiation from the sun (where the sun's rays are simplified to a parallel

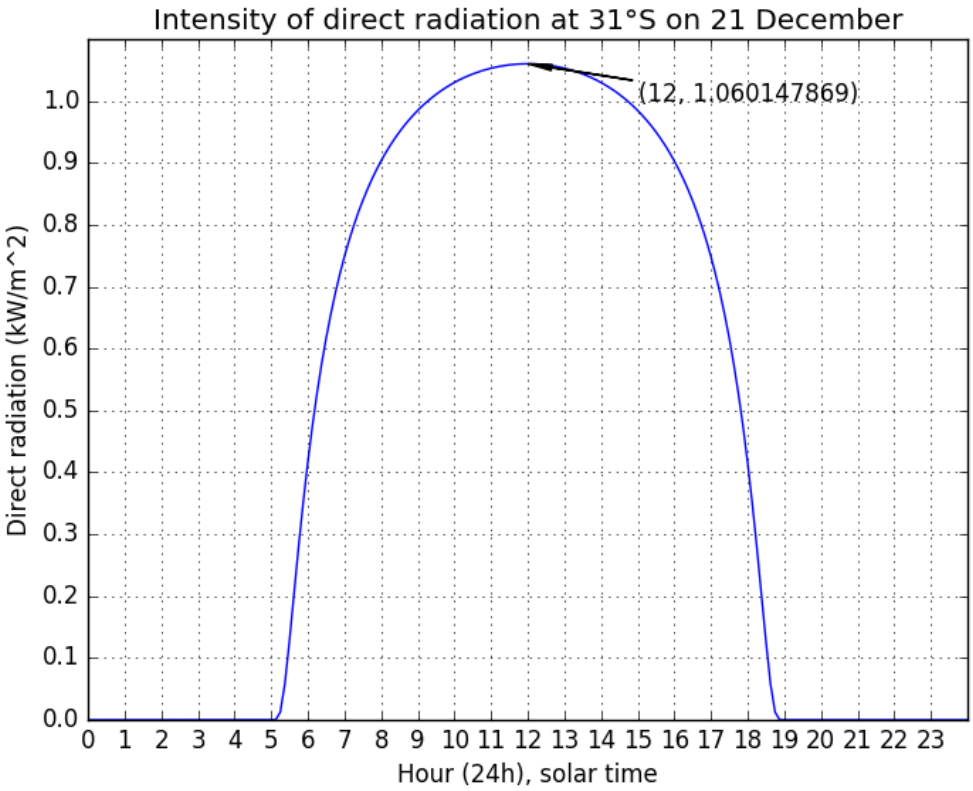


Figure 2.7: Solar Insolation: estimated solar radiation at $-31°$ latitude on 21 December at a given local solar time.[21]

beam). The maximum exposed surface area of the enclosure is calculated by first calculating which elevation angle θ would result in a maximum surface area for the side and lid, followed by calculating an azimuth angle ϕ which would result in a maximum surface area for the side, lid and front/back. The surface area for two sides is calculated as seen in Figure 2.8:

$$\begin{aligned} SA_{2-sides} &= l \cdot (h \cdot \sin\theta + w \cdot \cos\theta) \qquad , 0 \leq \theta \leq \frac{\pi}{4} \\ SA_{2-sides} &= 0.4 \cdot (0.23 \cdot \sin\theta + 0.225 \cdot \cos\theta) \qquad , 0 \leq \theta \leq \frac{\pi}{4} \end{aligned} \tag{2.1}$$

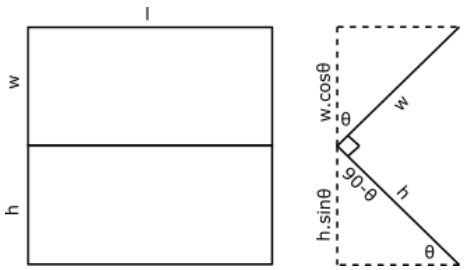


Figure 2.8: Calculating the surface area for two sides of the COTS enclosure.

To find the maximum projected surface area, the gradient is calculated, set to zero

and the corresponding θ is found:

$$\begin{aligned} \frac{dSA_{2-sides}}{d\theta} &= l \cdot h \cdot \cos\theta - l \cdot w \cdot \sin\theta \\ \theta &= \tan^{-1}(\frac{h}{w}) \\ &= \tan^{-1}(\frac{0.225}{0.23}) \\ &= 0.774\,\text{rad} \end{aligned} \tag{2.2}$$

Substituting θ back into equation 2.1, the maximum projected surface area for two sides is now calculated:

$$\begin{aligned} SA_{2-sides} &= 0.4 \cdot (0.23 \cdot \sin\theta + 0.225 \cdot \cos\theta) \\ &= 0.1287\,\text{m}^2 \end{aligned}$$

This can be confirmed by iterating equation 2.1 through θ, where $0 \leq \theta \leq \frac{\pi}{4}$.

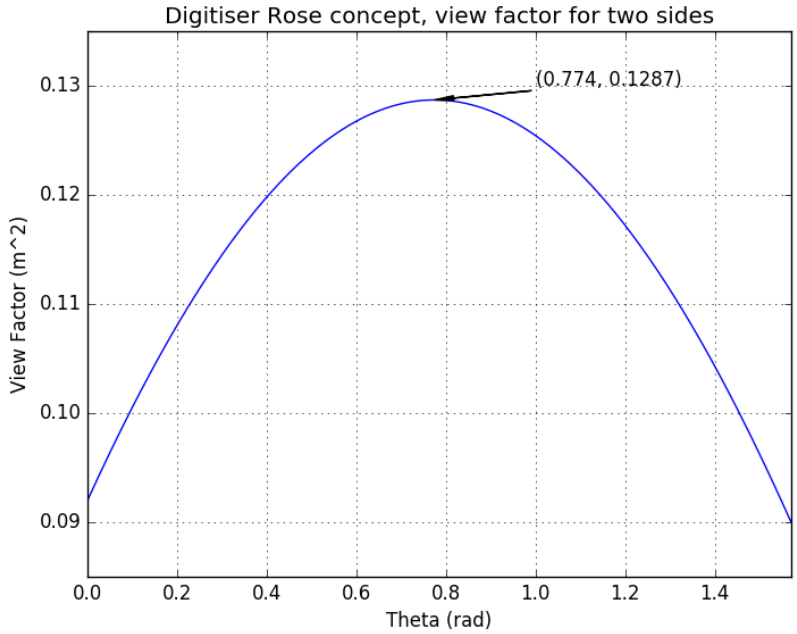


Figure 2.9: Projected surface area of two sides of the COTS enclosure as a function of solar elevation angle θ.

As seen in Figure 2.10, the projected surface area of the two sides rotating through the azimuth angle ϕ is:

$$SA_{2-sides} = l \cdot (h \cdot \sin\theta + w \cdot \cos\theta) \cdot \cos\phi \quad , 0 \leq \phi \leq \frac{\pi}{4} \tag{2.3}$$

The projected surface area for three sides adds the projected surface area of the front/rear to equation 2.3, as seen in Figure 2.11:

$$SA_{3-sides} = l \cdot (h \cdot \sin\theta + w \cdot \cos\theta) \cdot \cos\phi + (h^2 + w^2) \cdot \cos\theta \sin\theta \sin\phi \quad , 0 \leq \phi \leq \frac{\pi}{4} \tag{2.4}$$

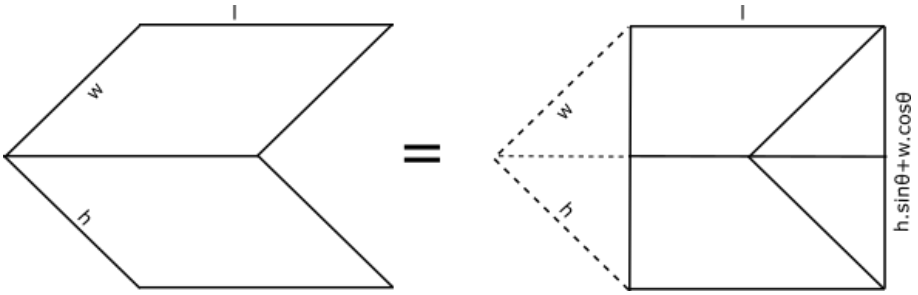


Figure 2.10: Equivalent projected surface area of two sides of the COTS enclosure rotating through the azimuth angle ϕ.

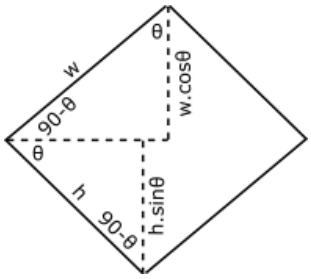


Figure 2.11: Projected surface area of three sides of the COTS enclosure rotating through the azimuth angle ϕ.

Once again, the maximum projected surface area is found by calculating the gradient of the surface area,

$$\frac{dSA_{3-sides}}{d\phi} = -l \cdot (h \cdot \sin\theta + w \cdot \cos\theta) \cdot \sin\phi + (h^2 + w^2) \cdot \cos\theta \sin\theta \cos\phi, \quad (2.5)$$

setting it to 0, and solving for ϕ:

$$\begin{aligned}
\phi &= \tan^{-1}\left(\frac{(h^2 + w^2) \cdot \cos\theta \sin\theta}{l \cdot (h \cdot \sin\theta + w \cdot \cos\theta)}\right) \\
&= \tan^{-1}\left(\frac{(0.225^2 + 0.23^2) \cdot \cos 0.774 \sin 0.774}{0.4 \cdot (0.225 \cdot \sin 0.774 + 0.23 \cdot \cos 0.774)}\right) \\
&= 0.382\,\text{rad}
\end{aligned}$$

Substituting ϕ back into equation 2.5, the maximum projected surface area for three sides is calculated:

$$\begin{aligned}
SA_{3-sides} &= 0.4 \cdot (0.225 \cdot \sin 0.774 + 0.23 \cdot \cos 0.774) \cdot \cos 0.382 + \\
&\quad (0.225^2 + 0.23^2) \cdot \cos 0.382 \cdot \sin 0.382 \cdot \sin 0.382 \\
&= 0.1387\,\text{m}^2
\end{aligned}$$

This can be confirmed by iterating equation 2.5 through ϕ, where $0 \leq \phi \leq \frac{\pi}{4}$ as seen in Figure 2.12.

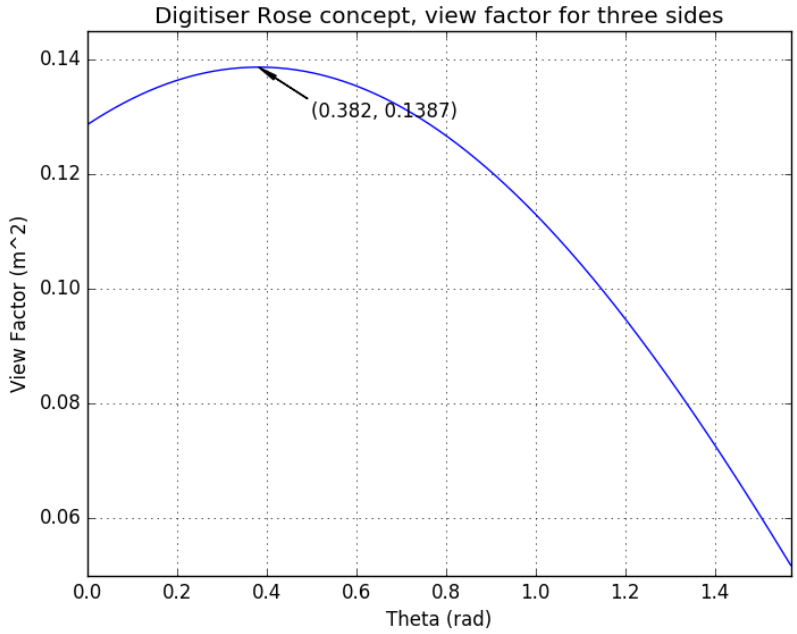


Figure 2.12: Projected surface area of three sides of the COTS enclosure as a function of solar elevation angle.

Solar loading

The total solar load through direct solar radiation for white painted aluminium as seen in Table 2.1 is then:

$$Q = 0.21 \cdot 0.1387 \cdot 1000 = 29.13W$$

For black painted aluminium:

$$Q = 0.97 \cdot 0.1387 \cdot 1000 = 134.55W$$

The above values suggest that it would be wise to place a solar shield over the enclosure to reduce the effect of solar loading. Given the earlier estimate of the total dissipated power from the Digitiser being around 95 to $125W$, $30W$ adds an additional $25 - 30\%$ of solar loading to the system.

2.5.2 Heat flux calculation

An estimate of the surface temperature of a solid can be calculated using the heat transfer co-efficient:

$$k = \frac{q}{\triangle T}$$

where k is the heat flux co-efficient ($^{W}/_{m^2K}$), q is the heat flux ($^{W}/_{m^2}$) and ΔT is the increase in temperature relative to the environment or above ambient temperature, in degrees Kelvin (or Celsius).

This equation is then rearranged to calculate ΔT. Expressing q as the ratio of internally dissipated power Q (Watts) and total surface area A (m^2).

$$\triangle T = \frac{Q}{kA} \tag{2.6}$$

Accepted values of k for air are shown in Table 2.2. The results of ΔT are shown in Table 2.3. For these calculations the total surface area of the conceptual Digitiser is:

$$A = 2 \cdot l \cdot h + 2 \cdot l \cdot w + 2 \cdot w \cdot h = 0.4675m^2$$

As an example, the Power Supply Unit at 80% efficiency is specified to be:

$$Q \approx 95W$$

Then using this to calculate $\triangle T$ for $k = 5\mathrm{Wm}^{-2}\mathrm{K}^{-1}$:

$$\triangle T = \frac{95}{5 \cdot 0.4675} = 40.6°C$$

Similarly, the Power Supply Unit at 60% efficiency is specified to be:

$$Q \approx 125W$$

Again using this to calculate $\triangle T$ for $k = 5\mathrm{Wm}^{-2}\mathrm{K}^{-1}$:

$$\triangle T = \frac{125}{5 \cdot 0.4675} = 53.5°C$$

The estimation assumes that the surface temperature and radiation are uniform across the body (which is true if the internal enclosure is well designed and the external environment is controlled).

Description	$k(\mathrm{W/m^2K})$
Air, free convection	0.5-10
Air, forced convection	10-200

Table 2.2: Convective co-efficient k-values for natural and free convection of air. [23]

PSU Efficiency	Solar Radiation	Finish	$Q(W)$	$k(\mathrm{W/m^2K})$		
				1	5	10
				$\triangle T$		
80%	No		95.0	203.2	40.6	20.3
60%	No		125.0	267.4	53.5	26.7
80%	Yes	White	124.1	265.5	53.1	26.6
60%	Yes	White	154.1	329.7	65.9	33.0
80%	Yes	Black	229.6	491.0	98.2	48.1
60%	Yes	Black	259.6	555.2	111.0	55.5

Table 2.3: $\triangle T$ values for a range of Digitiser enclosure surface finishes and PSU efficiencies.

2.5.3 Component temperatures

Electronic components are classified into "Commercial" and "Industrial" temperature grades within the electronics industry, of which the standard operating temperature ranges are shown in Table 2.4. One should be aware that the classification is not an industry standard and hence represents a general guideline only. Most complex electronic components and devices provide documentation on their safe operating temperature ranges, and should be evaluated individually. For the sake of establishing whether the COTS Enclosure concept is feasible the values in Table 2.4 will be used as the maximum allowable component temperatures.

Description	Temperature
Commercial grade	$0 \rightarrow 70°C$
Industrial grade	$-40 \rightarrow 85°C$

Table 2.4: Temperature range values for commercial and industrial grades of electronic components. [24]

From previous experience and consultation with sub-contractors, it has been found that mechanical design with careful consideration of conduction cooling will result in component junction temperatures within $10 - 15°C$ of enclosure wall temperatures (for components with power dissipation $\leq 15W$) [20]. A general junction temperature for components can then be calculated as follows:

$$T_j = T_a + T_{ae} + T_{ej}$$

where T_j refers to the junction temperature of a component, T_a to ambient temperature, T_{ae} to the temperature delta from ambient to an enclosure wall and T_{ej} to the temperature delta from enclosure wall to component junction. Table 2.5 shows the junction temperature calculated using this equation for four possible combinations of PSU efficiency and surface finish.

PSU Efficiency	Finish	$Q(W)$	$\triangle T$ $(°C)$	T_j $(°C)$
80%	White	124.1	29.5	84.5
60%	White	154.1	36.6	91.6
80%	Black	229.6	54.6	109.6
60%	Black	259.6	61.7	116.7

Table 2.5: T_j values for $k = 9$, ambient temperature $= 40°C$.

In Table 2.5, k is assumed to be 9. From previous experience, this value has matched similar systems in a laboratory setting. The results above suggest that it is unlikely that the COTS enclosure conceptual design will operate below $85°C$. It should be noted that the above also assumes perfect design, i.e. an optimal surface finish and perfect conduction. "Commercial grade" components will certainly not be suitable, and even "industrial grade" components may run above the recommended limits. Table 2.6 shows that if a value of $k = 25$, which is in the realm of convection cooling, were to be selected, then the COTS enclosure concept could be viable. Even at this low k-value, forced convection cooling level, commercial grade components

PSU Efficiency	Finish	$Q(W)$	$\triangle T$ ($^\circ C$)	T_j ($^\circ C$)
80%	White	124.1	10.6	65.6
60%	White	154.1	13.2	68.2
80%	Black	229.6	19.6	74.7
60%	Black	259.6	22.2	77.2

Table 2.6: T_j values for $k = 25$, ambient temperature = $40^\circ C$.

are a viable option if a white painted surface is used. However, there are two caveats to using forced convection cooling. Fan motors can produce electromagnetic interference (EMI)/ radio frequency interference (RFI) and pose the potential risk of contaminating the incoming signal to be digitised. Secondly, moving mechanical components (typically fans) associated with forced-air cooling typically have the lowest mean time between failure (MTBF). This would have a negative impact on combined sub-system MTBF figures and increase maintenance costs.

2.5.4 Validation of the preceding simple analysis

As the convection co-efficient was an unknown in the preceding analysis, we did not really know what the maximum operating temperature was likely to be. In order to have a better idea of this, we ran a simple simulation of the geometry of the COTS enclosure with the envisaged power-dissipation levels. To run the simulation, a solid cuboid with the outer dimensions of the enclosure concept was modelled using computer aided design (CAD). This was centred on a Cartesian coordinate system where X is width, Y is length, and Z is height. A boundary domain (also a cuboid) was then added to enclose the solid. Best CFD practice suggests the domain should be 5 times the width and length in X and Y and 8 times the length of the model in the Z direction [25]. It is centred on both the X and Y axes, while the Z axis is offset by $\frac{1}{8}$ [25]. This test volume is shown in Figure 2.13.

For the thermal simulation, gravity is in the negative Z direction. The solid is assigned aluminium material properties, while the boundary domain is set as air. The ambient temperature of the boundary domain at its inlet is set to $40^\circ C$. A $125W$ heat load is assigned to the cuboid. The simulation is solved for steady state conditions and terminates when the maximum temperature of the solid converges. The final iteration Z-plane temperature plot is shown in Figure 2.14. The COTS concept enclosure temperature is in the region of around $100^\circ C$ (and hence the components inside would be at an even higher temperature), which is well above the maximum component temperature limit of $85^\circ C$.

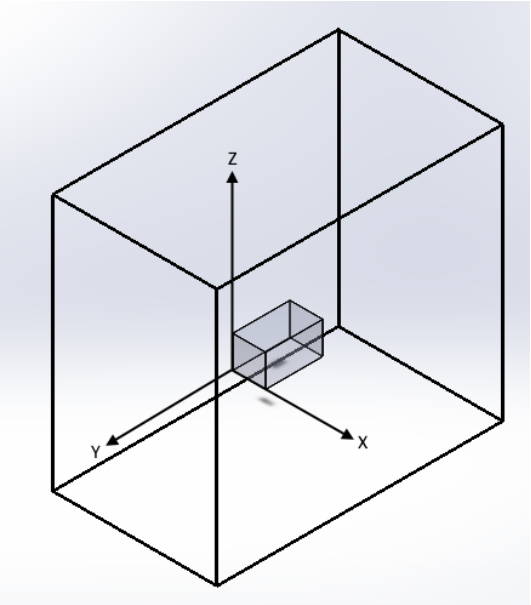


Figure 2.13: Thermal simulation for the Digitiser enclosure based on the COTS enclosure geometry.

2.6 Estimating the natural convection heat transfer coefficient k

Thermal simulations can produce incorrect values if the user makes incorrect assumptions, meshes incorrectly or inputs incorrect starting and boundary conditions. Another way to estimate the surface temperature T_s or convection co-efficient k of the enclosure was required to confirm the simulation. Two methods were selected to do this. One way was to estimate the surface temperature T_s, solve for k and then resolve for T_s [26]. One would then use the new T_s value and iterate until the k and T_s values converge. The second method would be to use a simplified formula for heat transfer by convection of air [27].

2.6.1 Simplified formula for heat transfer by convection of air

This method has two unknowns and calculates the heat transfer coefficient for natural convection of air over a flat plate (see Equation 2.7), but combined with the Newton rate equation (see Equation 2.8) one can either solve for the previous unknowns (see Equation 2.10 and Equation 2.9). [28]

$$k = C \cdot (\frac{\triangle T}{L})^n = C \cdot (\frac{T_s - T_a}{L})^n, \tag{2.7}$$

where k is the convection co-efficient ($Wm^{-2}K^{-1}$), C is a dimensionless constant (see Table 2.7), L is the length perpendicular to natural convection (m), T_s is surface temperature ($^\circ C$), T_a is ambient temperature ($^\circ C$) and n is a dimensionless exponential constant (see Table 2.7).

$$Q = k \cdot A \cdot \triangle T, \tag{2.8}$$

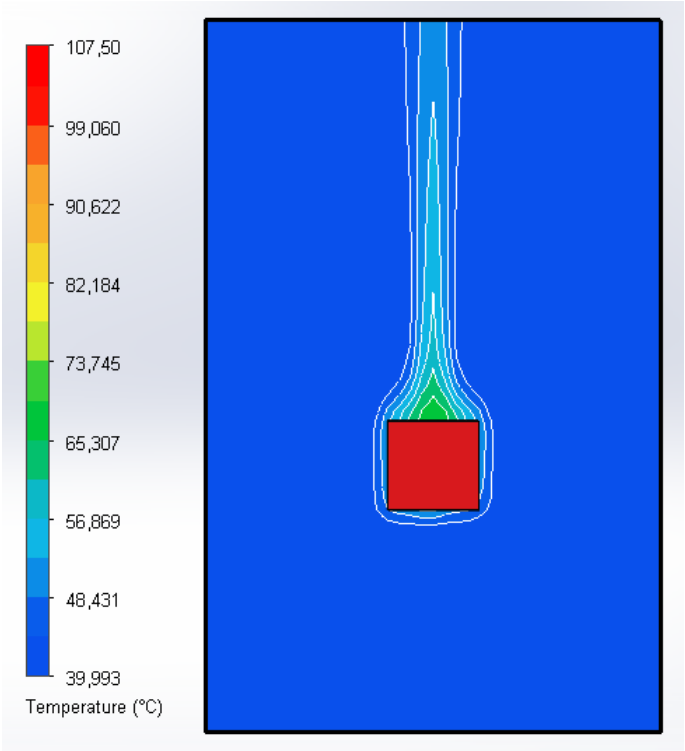


Figure 2.14: Thermal simulation for the Digitiser enclosure concept based on the Rose enclosure (XZ-plane).

Plate orientation	C constant	n exponent
Vertical	1.42	0.25
Horizontal (Up)	1.32	0.25
Horizontal (Down)	0.59	0.25

Table 2.7: Values of constant C and exponent n for various plate orientations.

where Q is the dissipated power in (W), k is the convection co-efficient, A is the surface area (m^2) and δT is the change in temperature between the surface and ambient $(°C)$.

$$T_s = T_a + (\frac{Q}{C \cdot A \cdot L^{-n}})^{\frac{1}{n+1}} \tag{2.9}$$

$$k = \frac{Q}{A \cdot \triangle T} \tag{2.10}$$

As an example, if the COTS concept is horizontally orientated and the Power Supply Unit is 80% efficient, calculating $\triangle T$:

$$\triangle T = (\frac{Q}{2 \cdot C_{vrt} \cdot A_{sd}l \cdot l^{-n} + 2 \cdot C_{vrt} \cdot A_{fb} \cdot w^{-n} + C_{hu} \cdot A_{tb} \cdot l^{-n} + C_{hd} \cdot A_{tb} \cdot l^{-n}})^{\frac{1}{n+1}}$$

Evaluating the individual terms,

$$\begin{aligned} 2 \cdot C_{vrt} \cdot A_{sd}l \cdot l^{-n} &= 2 \cdot 1.42 \cdot 0.4 \cdot 0.225 \cdot 0.4^{-0.25} = 0.321... \\ 2 \cdot C_{vrt} \cdot A_{fb} \cdot w^{-n} &= 2 \cdot 1.42 \cdot 0.23 \cdot 0.225 \cdot 0.23^{-0.25} = 0.212... \\ C_{hu} \cdot A_{tb} \cdot l^{-n} &= 1.32 \cdot 0.23 \cdot 0.4 \cdot 0.4^{-0.25} = 0.152... \\ C_{hd} \cdot A_{tb} \cdot l^{-n} &= 0.59 \cdot 0.23 \cdot 0.4 \cdot 0.4^{-0.25} = 0.068... \end{aligned}$$

Substituting this back into the original equation,

$$\begin{aligned}\triangle T =&(\frac{125}{0.321+0.212+0.153+0.068})^{\frac{1}{1.25}}\\ \triangle T =&59.6^{\circ}\mathrm{C}\end{aligned}$$

and k,

$$\begin{aligned}k =&\frac{125}{2\cdot(0.09+0.05175+0.092)\cdot\triangle T}\\ k =&4.485\,{}^{\mathrm{W}}/_{\mathrm{m}^{\circ}\mathrm{K}}\end{aligned}$$

$\triangle T$ can now be substituted back in to solve for T_s in the simplified formula for air:

$$\begin{aligned}T_s =&T_a+\triangle T\\ =&40+59.616\\ =&99.6^{\circ}\mathrm{C}\end{aligned}$$

This value agrees closely with the simulation value and suggests that it was done correctly. The k and T_s values for the COTS concept enclosure in a horizontal and vertical orientation are shown in Table 2.8 and 2.9.

PSU Efficiency	Finish	$Q(W)$	T_s ($^{\circ}C$)	k (${}^{\mathrm{W}}/_{\mathrm{m}^{\circ}\mathrm{K}}$)
80%	White	124.1	99.274	4.479
60%	White	154.1	110.482	4.677
80%	Black	229.6	136.965	5.065
60%	Black	259.6	146.974	5.191

Table 2.8: Estimated T_s and k values of the COTS enclosure in a horizontal orientation, ambient temperature = $40^{\circ}C$.

PSU Efficiency	Finish	$Q(W)$	T_s ($^{\circ}C$)	k (${}^{\mathrm{W}}/_{\mathrm{m}^{\circ}\mathrm{K}}$)
80%	White	124.1	94.478	4.873
60%	White	154.1	104.781	5.088
80%	Black	229.6	129.121	5.511
60%	Black	259.6	138.321	5.648

Table 2.9: Estimated T_s and k values of the COTS enclosure in a vertical orientation, ambient temperature = $40^{\circ}C$.

2.6.2 Iterative method to solve for k

The equation for convective heat transfer used previously was:

$$Q = k\cdot A\cdot(T_s - T_a) \tag{2.11}$$

An alternative way to solve for the convection co-efficient k is by using the Nusselt number. The Nusselt number is defined as the ratio between convective and conductive heat transfer:

$$\begin{aligned} Nu &= \frac{Convective\ heat\ transfer}{Conductive\ heat\ transfer} \\ &= \frac{k \cdot L}{\lambda}, \end{aligned} \tag{2.12}$$

where $Nu =$ Nusselt number (dimensionless), $k =$ convection co-efficient ($W/m^{-2}K^{-1}$), $\lambda =$ thermal conductivity ($W/m^{-1}K^{-1}$) and $L =$ characteristic length (m). Rearranging the equation the heat transfer co-efficient will be:

$$k = \frac{Nu \cdot \lambda}{L} \tag{2.13}$$

The Nusselt number for flat isothermal plates is used to solve for Equation 2.13 and is defined as:

$$Nu = C \cdot Ra^n, \tag{2.14}$$

the values for the constant C and the exponential constant n are shown in Table 2.10, where Ra is the Rayleigh number - defined for a fluid as a dimensionless number associated with buoyancy-driven flow. The Rayleigh number is:

$$Ra = Gr \cdot Pr, \tag{2.15}$$

where Gr is the Grashof number and Pr is the Prandtl number - the ratio of momentum diffusivity to thermal diffusivity. If $Ra < 10^9$ heat flow is laminar but if $Ra \geq 10^9$ then heat flow is turbulent.

The Grashof number is then defined as:

$$Gr = \frac{g_c \cdot L^3 \cdot \beta \cdot (T_s - T_a)}{\eta^2}, \tag{2.16}$$

where g_c is the gravitational constant ($^{m}/_{s^2}$), L is the the characteristic length perpendicular to the fluid flow (m), and β is the thermal expansion co-efficient of air. For gases, β is the reciprocal of temperature in Kelvin ($\frac{1}{^\circ K}$) - $\beta = \frac{1}{T_a}$, T_s is the surface temperature ($^\circ C$) (and is guessed for the first iteration to solve for k as explained below), T_a is the ambient temperature ($^\circ C$) and η is the kinematic viscosity of air ($^{m^2}/_{s}$).

Flow	Vertical plate		Flow	Horizontal plate	
	C	n		C	n
Laminar flow	0.59	0.25	Laminar flow (up)	0.54	0.25
Turbulent flow	0.14	0.33	Laminar flow (down)	0.27	0.25
			Turbulent flow	0.14	0.33

Table 2.10: Nusselt number for flat isothermal plates.

The Prandtl number Pr from Equation 2.15 is defined as:

$$Pr = \frac{\mu \cdot c_p}{\lambda}, \tag{2.17}$$

where μ is the dynamic viscosity of air ($^{kg}/_{m \cdot s}$), c_p is the specific heat of air ($^{J}/_{kg \circ K}$) and λ is the thermal conductivity of air ($^{W}/_{m \circ K}$). Once the value for k is found it is substituted Equation 2.11 to determine the surface temperature:

$$T_s = T_a + \frac{Q}{k \cdot A}$$

This new value for the surface temperature is substituted into the Grashof Equation 2.16 and a new value of k is determined. This process is repeated until the value for T_s and k converge. To illustrate the iterative method, one iteration will be shown to evaluate the COTS concept in a horizontal orientation at $Q = 125W$. An initial guess of $T_s = 100°C$ is used:

$$\begin{aligned} Gr_{side/lid} &= \frac{g_c \cdot l^3 \cdot \beta \cdot (T_s - T_a)}{\eta^2} \\ &= \frac{9.81 \cdot 0.4^3 \cdot \frac{1}{273.15+40} \cdot (100 - 40)}{(1.694 \cdot 10^{-5})^2} \\ &= 4.192 \cdot 10^8 \end{aligned}$$

$$\begin{aligned} Gr_{front/back} &= \frac{g_c \cdot w^3 \cdot \beta \cdot (T_s - T_a)}{\eta^2} \\ &= \frac{9.81 \cdot 0.23 \cdot \frac{1}{273.15+40} \cdot (100 - 40)}{(1.694 \cdot 10^{-5})^2} \\ &= 7.969 \cdot 10^7 \end{aligned}$$

$$\begin{aligned} Pr &= \frac{\mu \cdot c_p}{\lambda} \\ &= \frac{1.907 \cdot 10^{-5} \cdot 1005}{2.725 \cdot 10^{-2}} \\ &= 0.703 \end{aligned}$$

$$\begin{aligned} Ra_{side/lid} &= Gr_{side/lid} \cdot Pr \\ &= 4.192 \cdot 10^8 \cdot 0.703 \\ &= 2.948 \cdot 10^8 \end{aligned}$$

$$\begin{aligned} Ra_{front/back} &= Gr_{front/back} \cdot Pr \\ &= 7.969 \cdot 10^7 \cdot 0.703 \\ &= 5.605 \cdot 10^7 \end{aligned}$$

Both these numbers are $< 1 \cdot 10^9$; therefore the flow is laminar.

$$\begin{aligned} Nu_{side} &= C_v \cdot Ra_{side/lid}^{n_v} \\ &= 0.59 \cdot (2.948 \cdot 10^8)^{0.25} \\ &= 77.31 \end{aligned}$$

$$\begin{aligned} Nu_{front/back} &= C_v \cdot Ra_{front/back}^{n_v} \\ &= 0.59 \cdot (5.605 \cdot 10^7)^{0.25} \\ &= 51.05 \end{aligned}$$

$$
\begin{aligned}
Nu_{lid} &= C_{hu} \cdot Ra_{side/lid}^{n_{hu}} \\
&= 0.54 \cdot (2.948 \cdot 10^8)^{0.25} \\
&= 70.76
\end{aligned}
$$

$$
\begin{aligned}
Nu_{base} &= C_{hd} \cdot Ra_{side/lid}^{n_{hd}} \\
&= 0.27 \cdot (2.948 \cdot 10^8)^{0.25} \\
&= 35.38
\end{aligned}
$$

$$
\begin{aligned}
k_{side} &= \frac{Nu_{side} \cdot \lambda}{l} \\
&= \frac{77.31 \cdot 2.725 \cdot 10^{-2}}{0.4} \\
&= 5.267 \text{W/m}^2\text{K}
\end{aligned}
$$

$$
\begin{aligned}
k_{front/back} &= \frac{Nu_{front/back} \cdot \lambda}{w} \\
&= \frac{51.05 \cdot 2.725 \cdot 10^{-2}}{0.23} \\
&= 6.048 \text{W/m}^2\text{K}
\end{aligned}
$$

$$
\begin{aligned}
k_{lid} &= \frac{Nu_{lid} \cdot \lambda}{l} \\
&= \frac{70.76 \cdot 2.725 \cdot 10^{-2}}{0.4} \\
&= 4.82 \text{W/m}^2\text{K}
\end{aligned}
$$

$$
\begin{aligned}
k_{base} &= \frac{Nu_{base} \cdot \lambda}{l} \\
&= \frac{35.38 \cdot 2.725 \cdot 10^{-2}}{0.4} \\
&= 2.41 \text{W/m}^2\text{K}
\end{aligned}
$$

$$
\begin{aligned}
T_s &= T_a + \frac{Q}{2 \cdot k_{side} \cdot A_{side} + 2 \cdot k_{front/back} \cdot A_{front/back} + k_{lid} \cdot A_{base/lid} + k_{base} \cdot A_{base/lid}} \\
&= 40 + \frac{125}{2 \cdot 5.267 \cdot 0.09 + 2 \cdot 6.048 \cdot 0.05175 + 4.82 \cdot 0.092 + 2.41 \cdot 0.092} \\
&= 95.8^\circ\text{C}
\end{aligned}
$$

Further iterations converge on a surface temperature $T_s = 96.6°C$, which is within $4°C$ of the previous estimate and thermal simulation. At this point it seems more than likely that the COTS concept enclosure will be unsuitable for passive cooling as the chassis temperature (and hence the component T_j temperatures) will be far above the $85°C$ limit. A custom enclosure will need to be considered.

2.7 Thermal analysis of a simple geometrical model Digitiser enclosure ("Custom concept")

As seen in the previous section the commercial-off-the-shelf (COTS) Rose enclosure would not be able to keep component temperatures below $85°C$ as specified in the requirements in Section 2.3. A custom designed enclosure would need to be considered. A good starting point was thought to be maximising the enclosure size to the full keep-out zone placed in the requirements. The keep-out zone dimensional constraints for the Digitiser enclosure are:

$$\begin{aligned} Length_{max} &= 600mm \\ Width_{max} &= 400mm \\ Height_{max} &= 350mm \end{aligned}$$

Using these maximum values and the previous estimation method the temperature at the surface of the enclosure (T_s) is calculated as before:

$$\begin{aligned} \triangle T =& (\frac{125}{0.678 + 0.500 + 0.360 + 0.161})^{\frac{1}{1.25}} \\ \triangle T =& 31.2°\text{C}, \\ T_s =& 40 + 31.2 \\ =& 71.2°\text{C} \end{aligned}$$

T_s is now added to T_{ej} (the temperature delta from enclosure wall to component junction), from Section 2.5.3, to find the estimated component junction temperature T_j:

$$\begin{aligned} T_j &= T_a + T_{ae} + T_{ej} \\ &= T_s + T_{ej} \\ &= 71.2°C + 15°C \\ &= 86.2°C \end{aligned}$$

This is still over $85°C$ (albeit slightly) and would in any case not allow any space for natural convection to occur as such a large enclosure would likely be right up against other Digitisers and components mounted on the pedestal. The surface area for natural convection would need to be increased, i.e. heat-sinking to allow adequate natural convection. Furthermore, solar radiation would increase temperatures - a solar shield should be used. To verify the wall temperature calculation T_s, a simulation was run with the same geometry and dimensions as seen in Figure 2.15. The maximum wall temperature correlates with that calculated ($T_s \approx 71°C$).

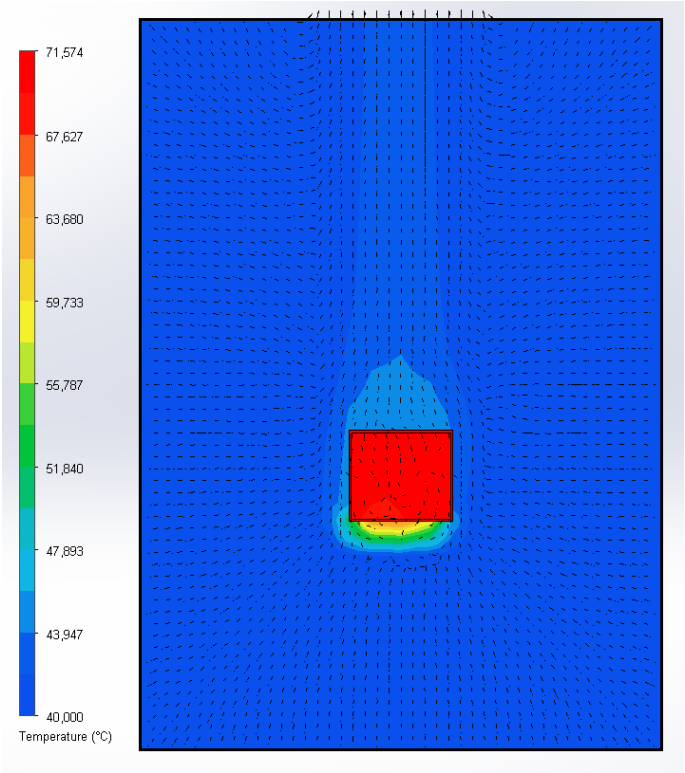
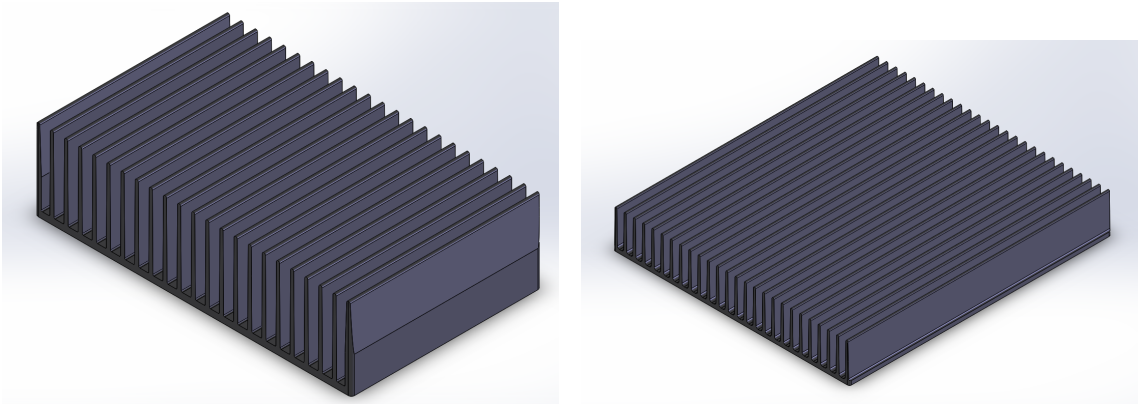


Figure 2.15: Thermal simulation for a "Maximum dimensioned" Digitiser (XZ-plane).

2.7.1 Adding heat-sinks to the enclosure to increase surface area

Suitable commercial-off-the-shelf (COTS) heat-sinks for natural convection were chosen (detailed in Chapter 3.1) for the side walls and rear of the enclosure. Fischer SK 157 (see Figure 2.16a)and Fischer SK 190 (see Figure 2.16b) for the side walls and rear, respectively. No heat-sink would be placed on the front face as the signal interfaces would be located there.



(a) Fischer SK157. **(b)** Fischer SK190.

Figure 2.16: Heat-sinks selected for the custom enclosure.

The geometric dimensions for the Fischer SK157 are:

$$\begin{aligned} Length_{SK157} &= 300mm \\ Width_{SK157} &= 180mm \\ Height_{SK157} &= 77.5mm \\ Height_{fins} &= 71.5mm \\ Width_{fins} &= 4mm \\ Gap_{fins} &= 9.4mm \\ N_{fins} &= 23 \end{aligned}$$

The geometric dimensions for the Fischer SK190 are:

$$\begin{aligned} Length_{SK190} &= 230mm \\ Width_{SK190} &= 255mm \\ Height_{SK190} &= 37.5mm \\ Height_{fins} &= 34mm \\ Width_{fins} &= 3mm \\ Gap_{fins} &= 6mm \\ N_{fins} &= 26 \end{aligned}$$

Adding these to the the custom enclosure design and leaving enough space for a solar shield results in an enclosure with the following dimensions:

$$\begin{aligned} Length_{custom} &= 449mm \\ Width_{custom} &= 215mm \\ Height_{custom} &= 255mm \end{aligned}$$

Using these dimensions, the estimate for the wall temperature T_s is once again calculated:

$$\begin{aligned} \triangle T =& (\frac{125}{0.397 + 0.229 + 0.156 + 0.070})^{\frac{1}{1.25}} \\ =& 54.1°\text{C}, \\ T_s =& 40 + 54.1 \\ =& 94.1°\text{C}. \end{aligned}$$

For completeness a thermal simulation of the geometry was run as seen in Figure 2.17.

Adding the heat-sinks (Figure 2.18), the estimate for the wall temperature T_s is re-calculated:

$$\begin{aligned} \triangle T =& (\frac{125}{2.451 + 0.114 + 0.074 + 0.166 + 0.074})^{\frac{1}{1.25}} \\ =& 20.4°\text{C}, \\ T_s =& 40 + 20.4 \\ =& 60.4°\text{C}, \end{aligned}$$

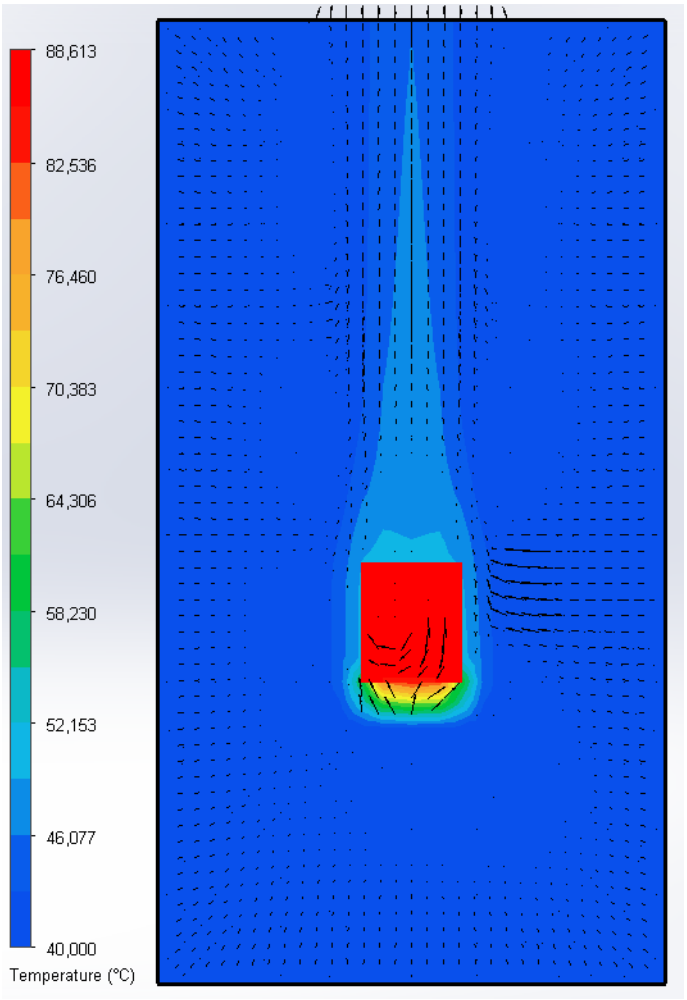


Figure 2.17: Thermal simulation for the Custom Digitiser concept with no heat-sinks(XZ-plane).

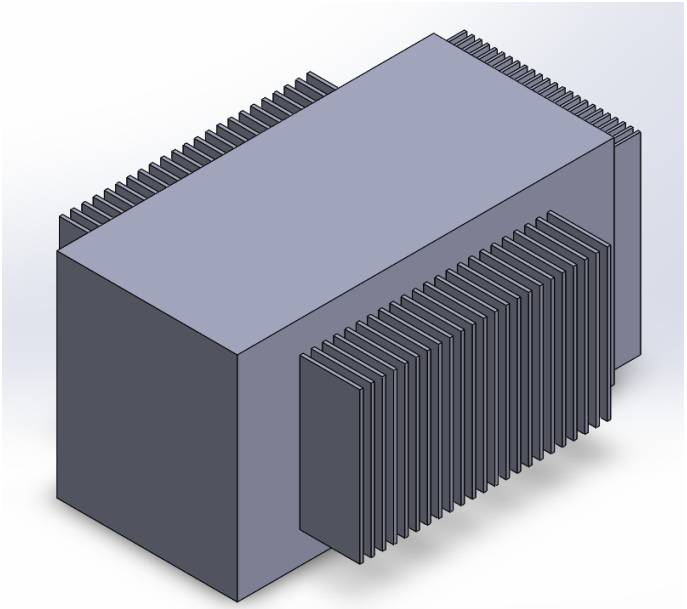


Figure 2.18: Simple geometrical model of the Custom Digitiser concept with heat-sinks.

as well at the final iteration of the iterative method used to calculate T_s as used in Section 2.6.2:

$$\begin{aligned}
Gr_{side/lid} &= \frac{g_c \cdot l^3 \cdot \beta \cdot (T_s - T_a)}{\eta^2} \\
&= \frac{9.81 \cdot 0.449^3 \cdot \frac{1}{273.15+40} \cdot (59.24 - 40)}{(1.694 \cdot 10^{-5})^2} \\
&= 1.901 \cdot 10^8 \\
Gr_{front/back} &= \frac{g_c \cdot w^3 \cdot \beta \cdot (T_s - T_a)}{\eta^2} \\
&= \frac{9.81 \cdot 0.215 \cdot \frac{1}{273.15+40} \cdot (59.24 - 40)}{1.694 \cdot 10^{-5})^2} \\
&= 2.087 \cdot 10^7 \\
Pr &= \frac{\mu \cdot c_p}{\lambda} \\
&= \frac{1.907 \cdot 10^{-5} \cdot 1005}{2.725 \cdot 10^{-2}} \\
&= 0.703
\end{aligned}$$

$$\begin{aligned}
Ra_{side/lid} &= Gr_{side/lid} \cdot Pr \\
&= 1.901 \cdot 10^8 \cdot 0.703 \\
&= 1.337 \cdot 10^8 \\
Ra_{front/back} &= Gr_{front/back} \cdot Pr \\
&= 2.087 \cdot 10^7 \cdot 0.703 \\
&= 1.468 \cdot 10^7 \\
Nu_{side} &= C_v \cdot Ra_{side/lid}^{n_v} \\
&= 0.59 \cdot (1.337 \cdot 10^8)^{0.25} \\
&= 63.444 \\
Nu_{front/back} &= C_v \cdot Ra_{front/back}^{n_v} \\
&= 0.59 \cdot (1.468 \cdot 10^7)^{0.25} \\
&= 36.521 \\
Nu_{lid} &= C_{hu} \cdot Ra_{side/lid}^{n_{hu}} \\
&= 0.54 \cdot (1.337 \cdot 10^8)^{0.25} \\
&= 58.068 \\
Nu_{base} &= C_{hd} \cdot Ra_{side/lid}^{n_{hd}} \\
&= 0.27 \cdot (1.337 \cdot 10^8)^{0.25} \\
&= 29.034
\end{aligned}$$

$$
\begin{aligned}
k_{side} &= \frac{Nu_{side} \cdot \lambda}{l} \\
&= \frac{63.444 \cdot 2.725 \cdot 10^{-2}}{0.449} \\
&= 3.851 \text{W/m}^2\text{K} \\
k_{front/back} &= \frac{Nu_{front/back} \cdot \lambda}{w} \\
&= \frac{36.521 \cdot 2.725 \cdot 10^{-2}}{0.215} \\
&= 4.629 \text{W/m}^2\text{K} \\
k_{lid} &= \frac{Nu_{lid} \cdot \lambda}{l} \\
&= \frac{58.068 \cdot 2.725 \cdot 10^{-2}}{0.449} \\
&= 3.524 \text{W/m}^2\text{K} \\
k_{base} &= \frac{Nu_{base} \cdot \lambda}{l} \\
&= \frac{29.033 \cdot 2.725 \cdot 10^{-2}}{0.449} \\
&= 1.762 \text{W/m}^2\text{K}
\end{aligned}
$$

$$
\begin{aligned}
T_s &= T_a + \frac{Q}{2 \cdot k_{side} \cdot A_{side} + k_{front/back} \cdot A_{front} + k_{front/back} \cdot A_{back} + k_{lid} \cdot A_{base/lid} + k_{base} \cdot A_{base/lid}} \\
&= 40 + \frac{125}{2 \cdot 3.851 \cdot 0.707 + 4.629 \cdot 0.055 + 4.629 \cdot 0.055 + 3.524 \cdot 0.103 + 1.762 \cdot 0.103} \\
&= 59.3^\circ\text{C}
\end{aligned}
$$

These values are compared to a thermal simulation of the Custom enclosure geometry with heat-sinks added (see Figure 2.19) and fall within $4^\circ C$ of each other. Finally the generalised "junction temperature" T_j value is once again calculated:

$$
\begin{aligned}
T_j &= T_a + T_{ae} + T_{ej} \\
&= T_s + T_{ej} \\
&= 59.245^\circ C + 15^\circ C \\
&= 74.3^\circ C
\end{aligned}
$$

This value is just over $10^\circ C$ below the $85^\circ C$ limit and suggests that this may be a viable solution. The additional heat load from solar radiation still needed to be considered to assess whether the custom enclosure design would work.

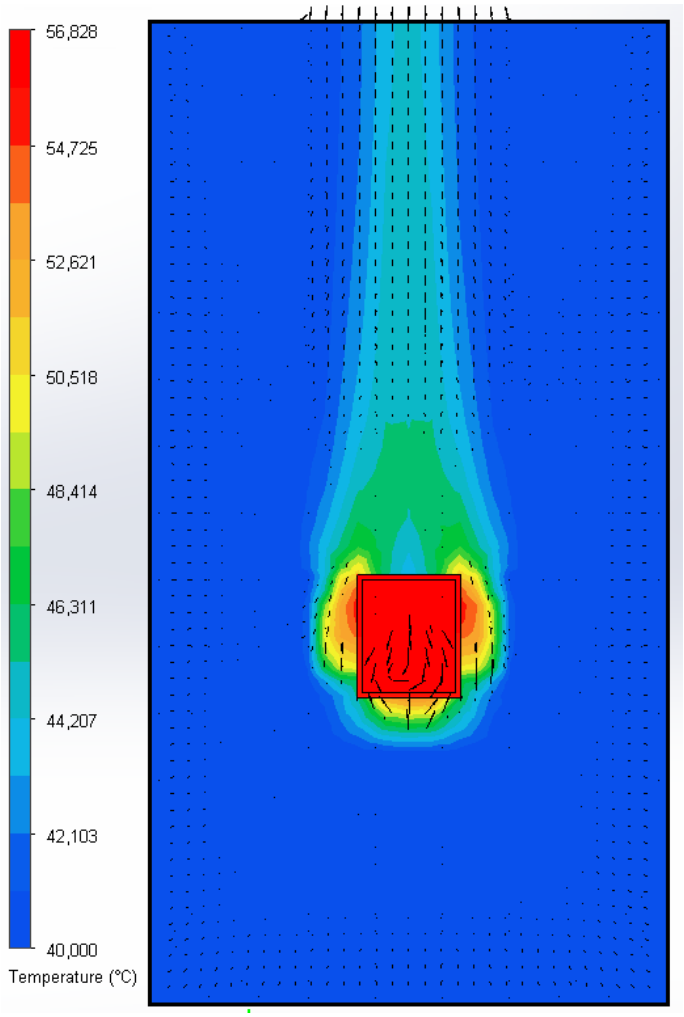


Figure 2.19: Thermal simulation for the custom Digitiser concept with heat-sinks(XZ-plane) (plane between fins).

2.7.2 Solar radiation

To calculate the incident solar radiation, the maximum projected surface area values need to be calculated for the custom concept enclosure. For the sake of simplicity the projected surface area of the heat sink fins is ignored because they comprise a small addition to the projected surface area of the enclosure. Equation 2.2 and Equation 2.5 are used to calculate the angles at which this maximum projected surface area would occur:

$$\begin{aligned}
\theta &= \tan^{-1}(\frac{h}{w}) \\
&= \tan^{-1}(\frac{0.255}{0.215}) \\
&= 0.87\,\text{rad} \\
\phi &= \tan^{-1}(\frac{(h^2+w^2)\cdot\cos\theta\sin\theta}{l\cdot(h\cdot\sin\theta+w\cdot\cos\theta)}) \\
&= \tan^{-1}(\frac{(0.255^2+0.215^2)\cdot\cos 0.87\cdot\sin 0.87}{0.449\cdot(0.255\cdot\sin 0.87+0.215\cdot\cos 0.87)}) \\
&= 0.351\,\text{rad}
\end{aligned}$$

These values are substituted back into the maximum projected surface equation:

$$\begin{aligned}
SA_{3-sides} &= l\cdot(h\cdot\sin\theta+w\cdot\cos\theta)\cdot\cos\phi+(h^2+w^2)\cdot\cos\theta\sin\theta\sin\phi \\
&= 0.449\cdot(0.255\cdot\sin 0.87+0.215\cdot\cos 0.87)\cdot\cos 0.351+ \\
&(0.255^2+0.215^2)\cdot\cos 0.87\cdot\sin 0.87\cdot\sin 0.351 \\
&= 0.1595\,\text{m}^2
\end{aligned}$$

This maximum surface area is used to calculate the heat load from solar radiation:

$$\begin{aligned}
Q_{solar} &= \alpha AI \\
&= 0.21\cdot 0.1595\cdot 1053 \\
&= 35.27\text{W}
\end{aligned}$$

An additional $35W$ of power seems to be quite significant. The surface temperature estimate is calculated to see its effect:

$$\begin{aligned}
\triangle T =& (\frac{125+35.27}{2.451+0.114+0.074+0.166+0.074})^{\frac{1}{1.25}} \\
=& 24.9^\circ\text{C}, \\
T_s =& 40+24.9 \\
=& 64.9^\circ\text{C}
\end{aligned}$$

To ensure that the estimate value was correct the iterative method is also used to calculate the surface temperature value:

$$\begin{aligned}
T_s &= T_a+\frac{Q+Q_{solar}}{2\cdot k_{side}\cdot A_{side}+k_{front/back}\cdot A_{front}+k_{front/back}\cdot A_{back}+k_{lid}\cdot A_{base/lid}+k_{base}\cdot A_{base/lid}} \\
&= 40+\frac{125+35.27}{2\cdot 3.851\cdot 0.707+4.629\cdot 0.055+4.629\cdot 0.055+3.524\cdot 0.103+1.762\cdot 0.103} \\
&= 64.7^\circ\text{C}
\end{aligned}$$

This is again added to the estimated T_{ej} value to check the junction temperature.

$$\begin{aligned} T_j &= T_a + T_{ae} + T_{ej} \\ &= T_s + T_{ej} \\ &= 64.7°C + 15°C \\ &= 79.7°C \end{aligned}$$

This value is $5.3°C$ below the $85°C$ maximum but does not leave a large margin for error. A solar shield should be added to increase the margin.

2.7.3 Adding a solar shield and its effect on radiation

The solar shield dimensions are:

$$\begin{aligned} Length_{shield} &= 600mm \\ Width_{shield} &= 403mm \\ Height_{shield} &= 300mm \end{aligned}$$

Following the procedure as in the previous section Equation 2.2 and Equation 2.5 are again used to calculate the angles at which the maximum projected surface area would occur:

$$\begin{aligned} \theta &= \tan^{-1}(\frac{h}{w}) \\ &= \tan^{-1}(\frac{0.3}{0.403}) \\ &= 0.64\,\text{rad} \\ \phi &= \tan^{-1}(\frac{(h^2+w^2)\cdot\cos\theta\sin\theta}{l\cdot(h\cdot\sin\theta + w\cdot\cos\theta)}) \\ &= \tan^{-1}(\frac{(0.3^2+0.403^2)\cdot\cos 0.64\cdot\sin 0.64}{0.6\cdot(0.3\cdot\sin 0.64 + 0.403\cdot\cos 0.64)}) \\ &= 0.381\,\text{rad} \end{aligned}$$

These values are substituted into the projected surface area equation to obtain the maximum:

$$\begin{aligned} SA_{3-sides} &= l\cdot(h\cdot\sin\theta + w\cdot\cos\theta)\cdot\cos\phi + (h^2+w^2)\cdot\cos\theta\sin\theta\sin\phi \\ &= 0.6\cdot(0.3\cdot\sin 0.64 + 0.403\cdot\cos 0.64)\cdot\cos 0.381 + \\ &(0.3^2+0.403^2)\cdot\cos 0.64\cdot\sin 0.64\cdot\sin 0.381 \\ &= 0.3248\,\text{m}^2 \end{aligned}$$

The heat load from solar radiation into the solar shield is calculated from this:

$$\begin{aligned} Q_{solar} &= \alpha_{whitepaint}\cdot SA_{3-sides}\cdot I \\ &= 0.21\cdot 0.3248\cdot 1053 \\ &= 71.823\text{W} \end{aligned}$$

This value is then used to calculate the surface temperature on the solar shield:

$$\begin{aligned}\triangle T =& (\frac{71.823}{0.581+0.431+0.363+0.162})^{\frac{1}{1.25}}\\ =& 21.7°\text{C},\\ T_s =& 40+21.7\\ =& 61.7°\text{C}\end{aligned}$$

Next the radiated heat transferred to the Digitiser by the solar shield is calculated [29]:

$$\begin{aligned}T_{shield} &= 334.815\,\text{K}\\ T_{digitiser} &= 332.395\,\text{K}\\ \varepsilon_{whitepaint} &= 0.96\\ SA_{shield} &= 0.8436\text{m}^2\\ SA_{digitiser} &= 0.4325\text{m}^2\\ F_v &= \frac{SA_{digitiser}}{SA_{shield}}\\ &= 0.5159\end{aligned}$$

where the Digitiser temperature and shield temperature are converted to Kelvin, ε is the emissivity value for white paint, SA_{shield} and $SA_{digitiser}$ are the surface areas of the solar shield and Digitiser, respectively and F_v is a ratio of the surface area of the solar shield seen by the Digitiser.

$$\begin{aligned}Q_{shield\rightarrow digitiser} &= \frac{SA_{shield}\cdot\sigma\cdot(T^4_{shield}-T^4_{digitiser})}{(\frac{1-\varepsilon_{whitepaint}}{\varepsilon_{whitepaint}})+(\frac{SA_{shield}+SA_{digitiser}\cdot SA_{shield}\cdot F_v}{SA_{digitiser}-SA_{shield}\cdot F_v^2})+(\frac{1-\varepsilon_{whitepaint}}{\varepsilon_{whitepaint}})\cdot\frac{SA_{shield}}{SA_{digitiser}}}\\ &= \frac{0.8436\cdot 5.67\cdot 10^{-8}\cdot(334.815^4-332.395^4)}{(\frac{1-0.96}{0.96})+(\frac{0.8436+0.4325\cdot 0.8436\cdot 0.5159}{0.4325-0.8436\cdot 0.5159^2})+(\frac{1-0.96}{0.96})\cdot\frac{0.8436}{0.4325}}\\ &= 3.3812\,\text{W}\end{aligned}$$

This is less than a quarter of the value calculated with no solar shield. It is then added to the Digitiser dissipated power to obtain the surface temperature:

$$\begin{aligned}\triangle T =& (\frac{125+3.3812}{2.451+0.114+0.074+0.166+0.074})^{\frac{1}{1.25}}\\ =& 20.9°\text{C},\\ T_s =& 40+20.9\\ =& 60.9°\text{C}\end{aligned}$$

The junction temperature is again calculated:

$$\begin{aligned}T_j &= T_a + T_{ae} + T_{ej}\\ &= T_s + T_{ej}\\ &= 60.9°C + 15°C\\ &= 75.9°C\end{aligned}$$

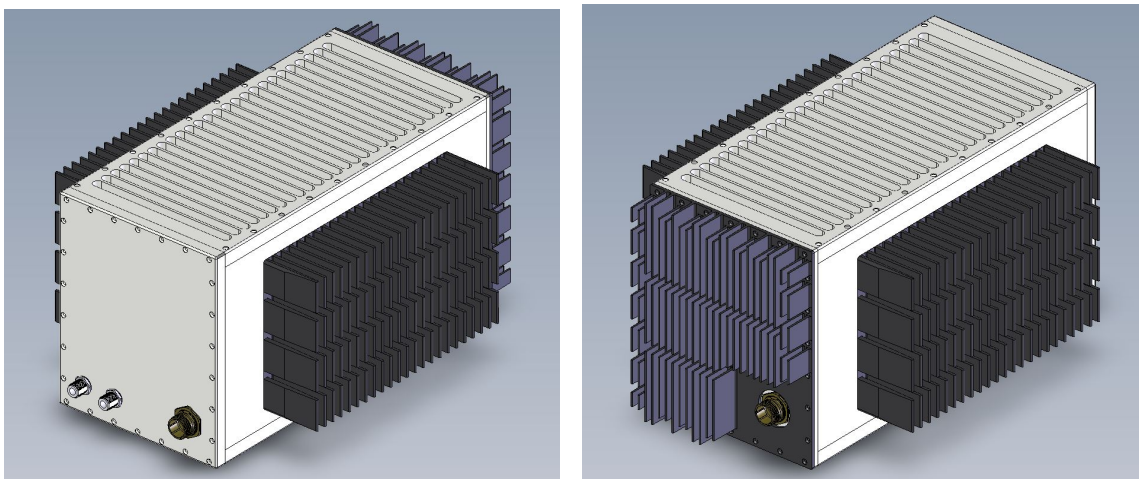
This final value is $9.1°C$, below the $85°C$ limit. It does not leave a lot of room for error but should be adequate to allow the Digitiser components to be cooled using natural convection.

Chapter 3

Detailed Design and Thermal Simulations

3.1 Conceptual Digitiser enclosure model

The proposed Digitiser design, based on conduction and natural convection, can be seen in Figure 3.1a and 3.1b. Natural convection is the proposed cooling method to minimise the possibility of electromagnetic interference (EMI), which could result if active cooling methods, e.g. fans, are used.



(a) Front projected view of conceptual Digitiser.

(b) Rear projected view of conceptual Digitiser.

Figure 3.1: Conceptual Digitiser enclosure.

3.1.1 Overview of conceptual Digitiser enclosure design

To best illustrate the conceptual Digitiser enclosure design an exploded view is provided in Figure 3.2. The outer enclosure is made up of 2 mirrored side walls, a bottom and top lid (which are exactly the same design), and a front panel. The Power Supply Unit (PSU) enclosure also acts as the rear wall of the outer main enclosure. All of these parts are machined out of aluminium. Finally, heat sinks are placed on both side walls and the rear of the enclosure. They are included to increase heat transfer to the surrounding environment using both natural convection

and radiation. A modular design was chosen for all the internal components to allow for easier maintenance and repair. Each of the major components is housed within its own separate aluminium housing. The housings act as a large conductive heat sink as well as increasing the amount of EMI protection. These enclosures have uniform outer dimensions, barring the PSU (which, as mentioned, acts as the rear wall of the Digitiser enclosure). The major component enclosures are designed to maximise the heat flow to the side walls of the outer enclosure and to the rear wall in the case of the PSU. The finned heat sinks are placed on the sides and rear wall for this reason. Connector interfaces between all the major components are located on their respective front panels, barring the PSU connections on the rear of each module (and front face of the PSU). The vertical and horizontal polarisation input and digital fibre output interfaces are located on the outer enclosure front panel, while the external power inlet is located on the outer enclosure PSU/rear wall. A space for the interconnecting harnesses is left between the major component module front faces and the outer enclosure front panel.

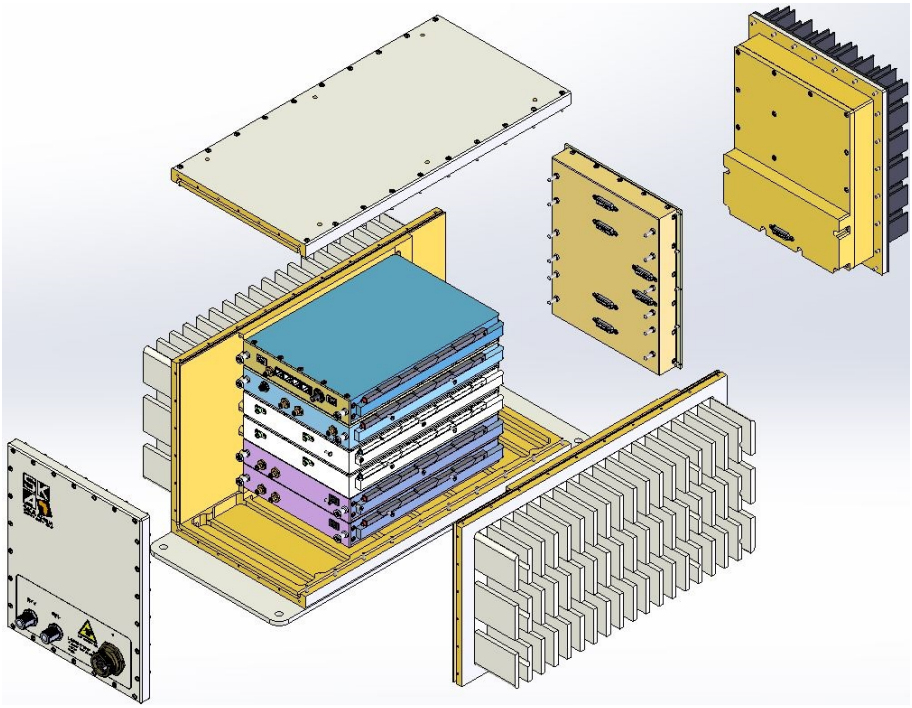


Figure 3.2: Exploded view of the Digitiser enclosure concept design.

Module construction

Each of the major component enclosures consists of a main lid (heat sink), base, and front face (see Figure 3.3). The exception to this is the PSU, explained above, and the Radio Frequency Conditioning Unit (RFCU), which only consists of a lid and base (as decided by Tellumat - the manufacturer of that unit). The parts are machined out of aluminium and given a conductive surface finish to increase the EMI shielding effectiveness on all mating edges. These parts fully encapsulate the printed circuit board (PCB), and form a Faraday cage around the PCB, when fully assembled. Furthermore, mating surfaces are given stepped joins to increase EMI protection and fastening screws are closely spaced to decrease aperture widths and increase the metal to metal bonding.

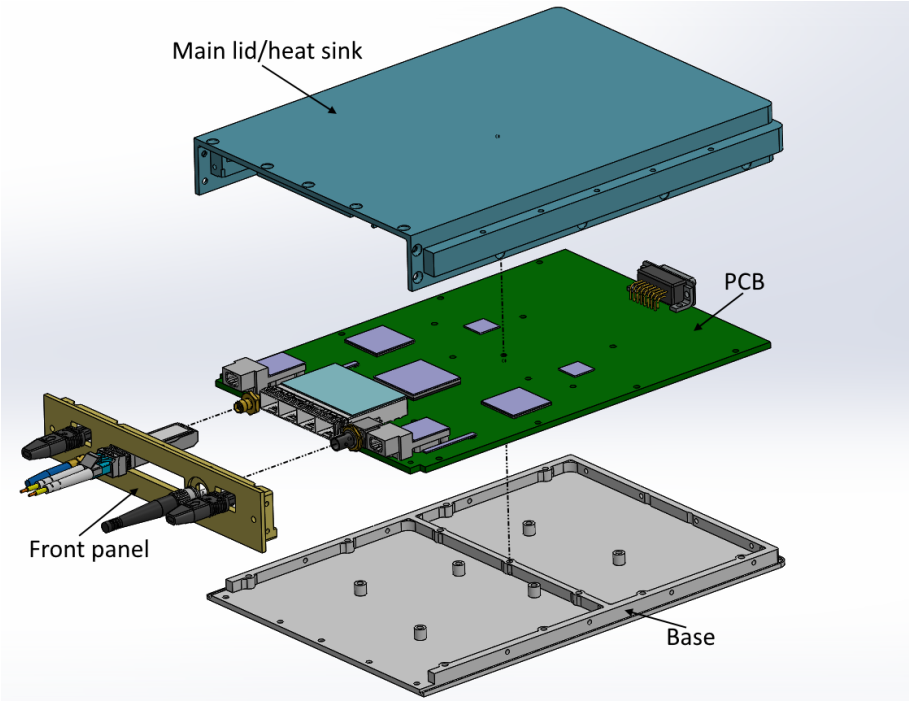


Figure 3.3: Exploded view of a Digitiser module.

A thermally conductive path or thermal interface to the side walls of the outer enclosure is provided through extrusions on the main lid which touch down on high-powered components on the PCB and the PCB itself, as illustrated in Figure 3.4. To account for mechanical manufacturing tolerances, a thermal gap filler is placed between the chip and extrusion to ensure there is an unbroken thermal path (i.e. no air gap) between the PCB and the cover/main heat sink. The thermal interface between the major component enclosure and the side wall of the outer enclosure is provided by compressed metal-to-metal contact from guide rails and grooves on the major component enclosure and outer enclosure, respectively. The force to create compression is provided by wedge-locks which expand in the guide grooves. Compression decreases the thermal resistance between interfaces.

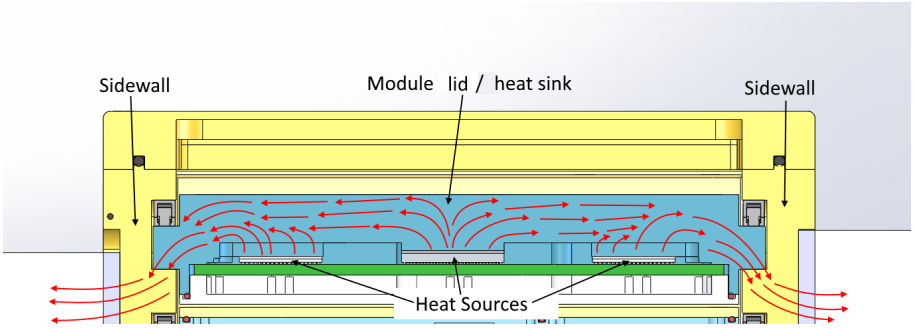


Figure 3.4: Thermal path to side walls through lid/heat-sink.

Good thermal conduction from the PCB is achieved by using exposed copper surfaces where the lid extrusions touch down, large copper planes and numerous thermal relief vias.

3.1.2 Placement of major components

The overall concept of component placement is to keep high-powered components away from each other, avoiding concentrated heated regions and placing them in regions where the thermally conductive and radiative surface area would be greatest.

The D-Engine, with an estimated power consumption of around $40W$, is placed at the top of the enclosure cavity. Being the highest power component, this position allows an extra thermal path through the lid if the path through the side walls provides insufficient cooling. The $4W$ Sample Clock Generator (SCG) and two RFCUs are placed below this and finally the two $20W$ analog-to-digital converter (ADC) converter modules occupy the bottom two levels of the Digitiser module stack.

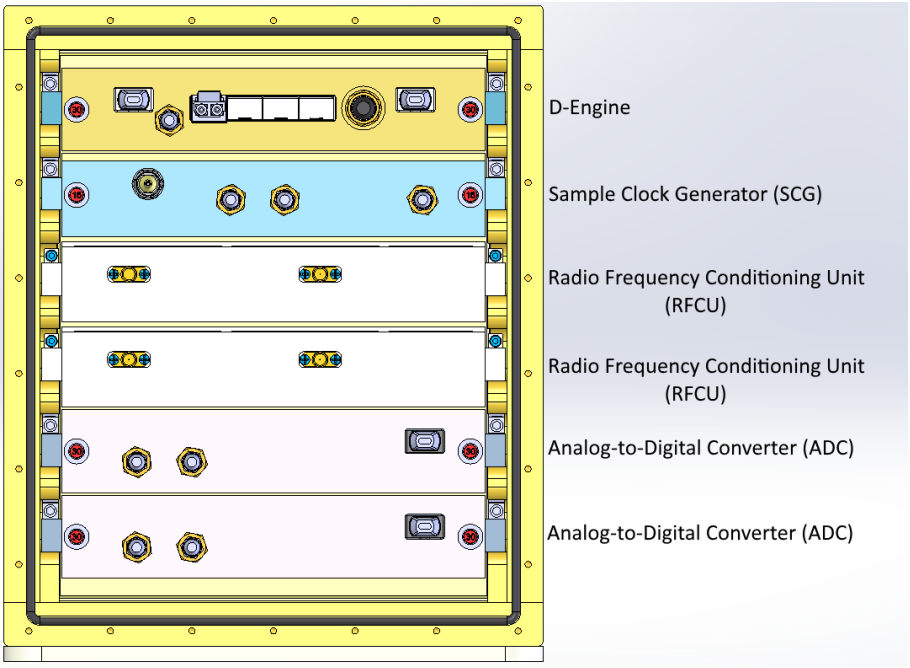


Figure 3.5: Digitiser module stack-up.

3.1.3 Conceptual Digitiser enclosure dimensions

The Digitiser enclosure dimensions are shown in Figure 3.6.

$$Length_{Enclosure} = 449mm,$$

$$Width_{Enclosure} = 215mm,$$

$$Height_{Enclosure} = 255mm.$$

These dimensions are still within the allocated space on the indexer platform, as can be seen in Figure 3.7.

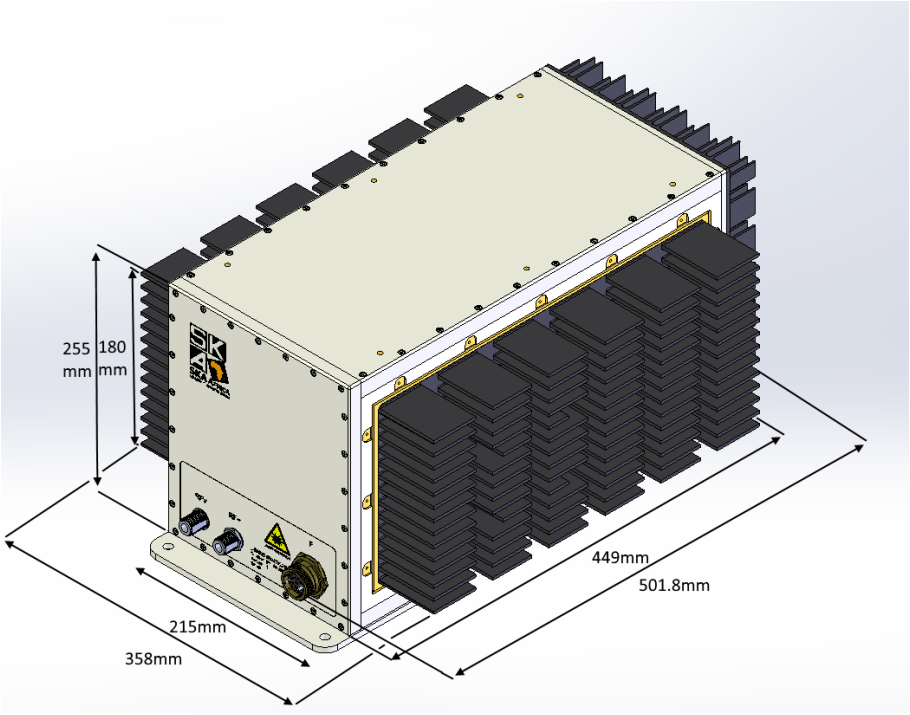


Figure 3.6: Digitiser enclosure dimensions.

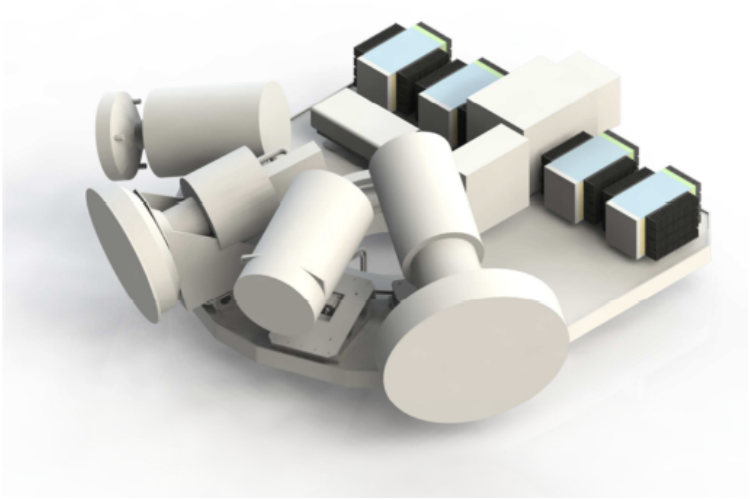


Figure 3.7: Placement of Digitiser enclosures on the indexer-platform. [20]

3.1.4 Enclosure weight

The masses of the components of the outer Digitiser enclosure as well as the masses of the internal modules can be seen in Table 3.1. The total mass of 31.397 kg is well below the 40 kg limit provided in the requirements.

Item	Weight (kg)	Qty.	Total weight (kg)
Side wall	3.238	2	6.476
Lid	2.010	2	4.020
Side heat sink	3.283	2	6.566
Rear heat sink	1.494	1	1.494
Front panel	0.783	1	0.783
PSU a	0.559	1	0.559
PSU b	1.772	1	1.772
PSU c	0.283	1	0.283
			21.953
Component lid	1.155	6	6.930
Component base	0.411	6	2.466
Component face	0.068	6	0.408
			9.804
		Total	**31.397**

Table 3.1: Conceptual Digitiser enclosure weight estimate. [20]

3.1.5 Solar radiation shield

The conceptual design for the Digitiser solar radiation shield is shown in Figure 3.8. Its purpose is to diminish the amount of solar radiation absorbed by the Digitiser enclosure itself - while being sufficiently far enough away from the enclosure to not obstruct the flow of rising hot air (natural convection) over the enclosure. It is constructed of aluminium and painted white. An air gap is left below the solar shield to allow an inlet for cool air and cutouts are employed to allow air to escape. Furthermore the side walls create a chimney effect on the sidewall heat-sinks forcing rising air to pass between the heat-sink fins.

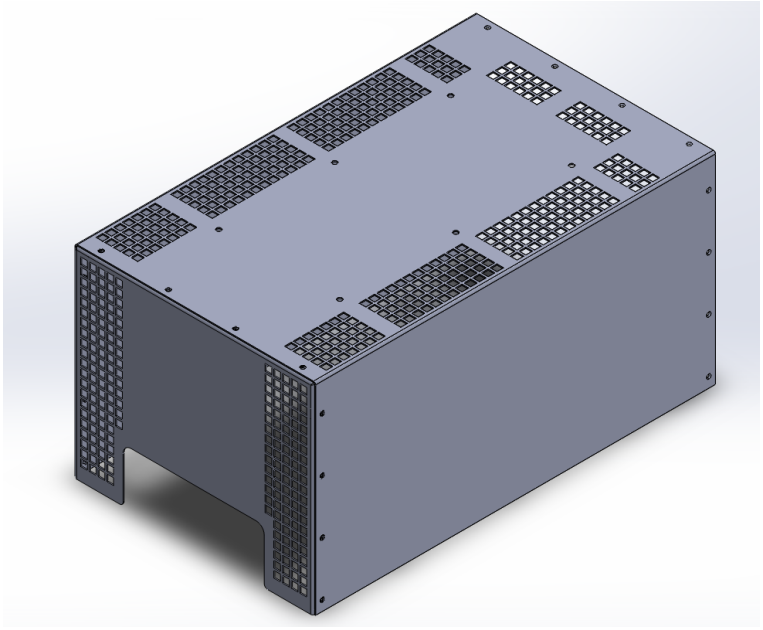


Figure 3.8: Digitiser solar shield.

3.1.6 IP Sealing

One of the requirements on the Digitiser is an IP-67 (ingress protection) rating. This was addressed by creating tongue-and-groove joints in the outer housing lids, front face, side walls and PSU and placing an electrically conductive metal-impregnated silicone elastomer gasket in it. See Figure 3.9.

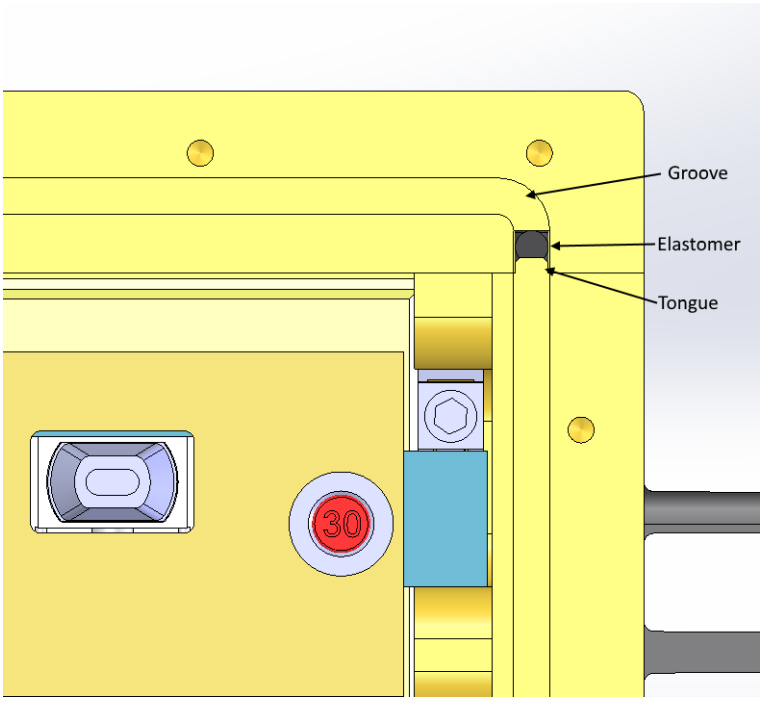


Figure 3.9: IP Sealing grooves and elastomer.

3.1.7 Digitiser mounting

The Digitiser mounting interface can be seen in Figure 3.10. The Digitiser is attached to a mounting base plate using six M8 x 10mm screws from below. Four M8 x 40mm hexagonal spacers screw into both the mounting base plate and the indexer platform. The spacers ensure that there is a large enough air gap below the Digitiser to not impede the rising hot air. The air gap also thermally isolates the Digitiser from the indexer platform in the event that any heat should be present there, i.e. from other high-powered units sinking heat into the platform or from solar radiation loading.

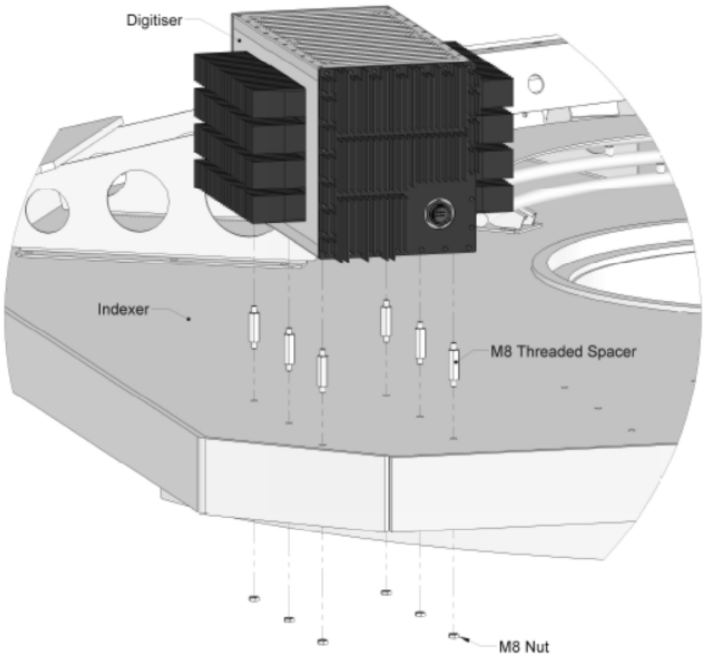


Figure 3.10: Mounting the Digitiser on the indexer platform. [20]

3.1.8 D-Engine module conceptual design

A conceptual PCB layout for the D-Engine module can be seen in Figure 3.11.

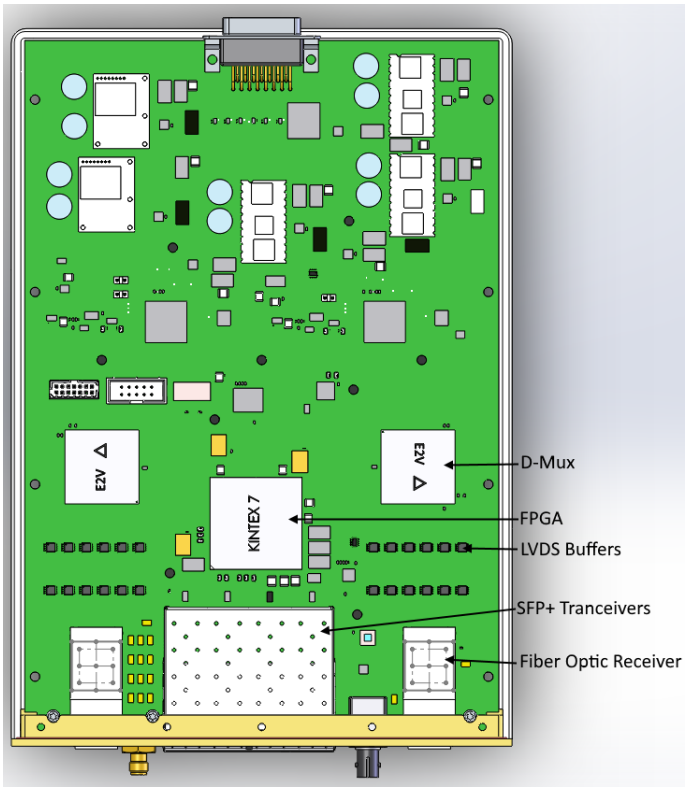


Figure 3.11: Symmetrical layout of the D-Engine PCB design.

The PCB is encased in a component enclosure that touches down on the high-powered components as shown previously in 3.1.1. Ideally, from a thermal perspective, high-powered components should be placed as near to the sides of the PCB as possible to ensure the shortest thermal path to the side walls of the enclosure (see Figure 3.12). These high-powered components include the FPGA, de-multiplexers, small form-factor pluggable (SFP+) and Multi-fiber Push On (MPO) fibre optical receivers. Suggested maximum power values for these components are shown in Table 3.2.

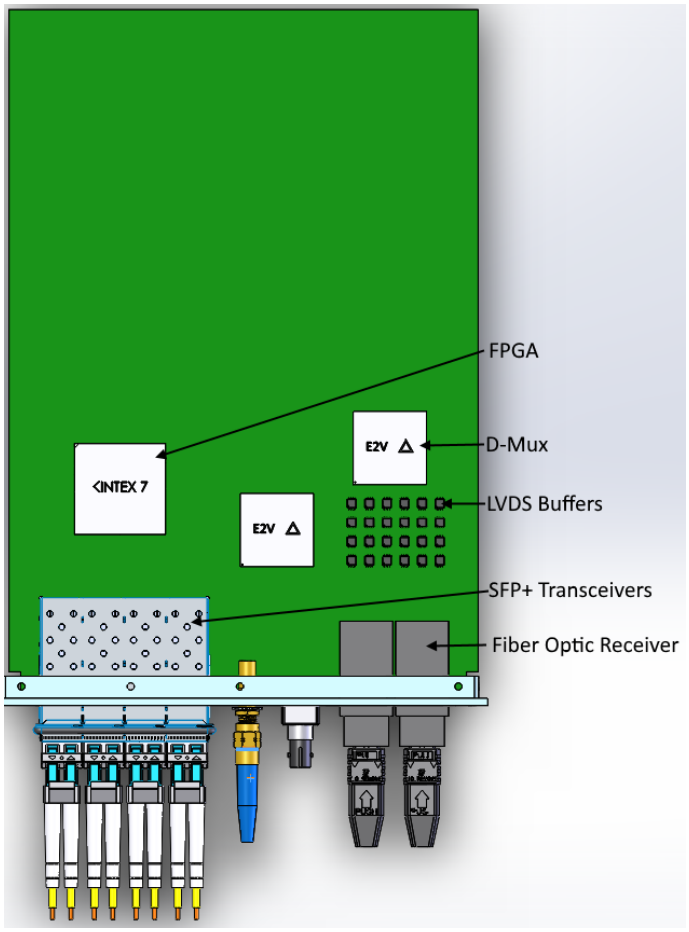


Figure 3.12: Asymmetrical layout of the D-Engine PCB design.

A layout where the FPGA is located in the centre of the board (Figure 3.14) has the advantage of decreasing the complexity of trace routing compared to the asymmetrical layout (Figure 3.11). All the high-powered components are mated to the enclosure lid using a thermal compound to eliminate any air gaps (and to compensate for mechanical tolerances) which are highly thermally insulating.

Component	Power (W)	Qty.	Total power (W)
FPGA	14.5	1	14.5
De-Mux	2.7	2	5.4
SFP+ Tranceivers	1.0	4	4.0
Fibre Optic Receiver	1.55	2	3.1
LVDS Buffers	0.1	24	2.4
Other	9.37	1	9.37
		Total	**36.37**

Table 3.2: Estimated maximum power budget for the D-Engine high-powered components.

The two layouts are compared by running thermal simulations using the previously calculated surface temperature of $61.5°C$ as the boundary condition on the bottom surface of the two guide rails on the D-Engine enclosure lid. Convection (and radiation) are ignored in the simulation as there is little to no air flow within and around the modules. All thermal simulations were run using Autodesk Simulation CFD.

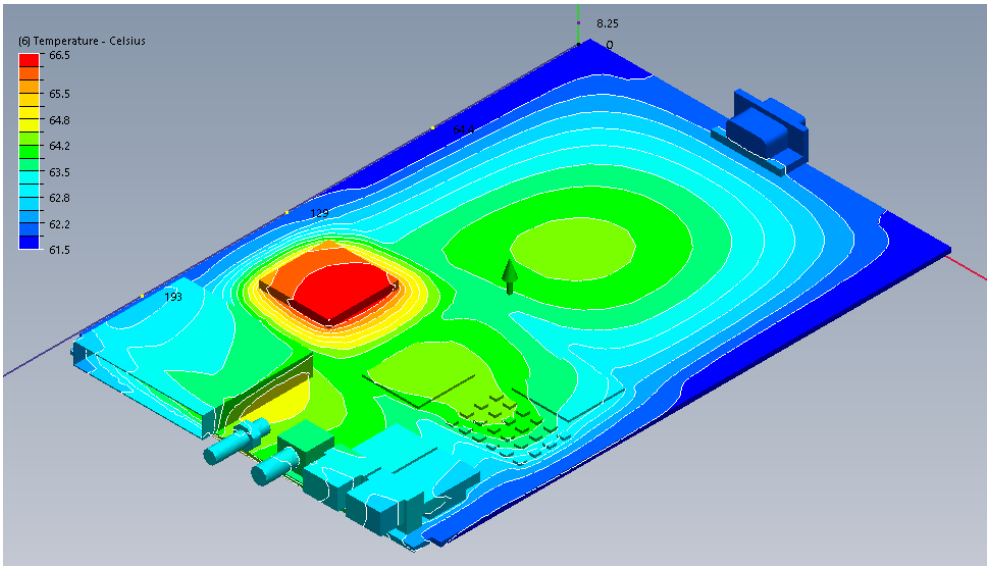


Figure 3.13: Asymmetrical thermal plot of the D-Engine PCB.

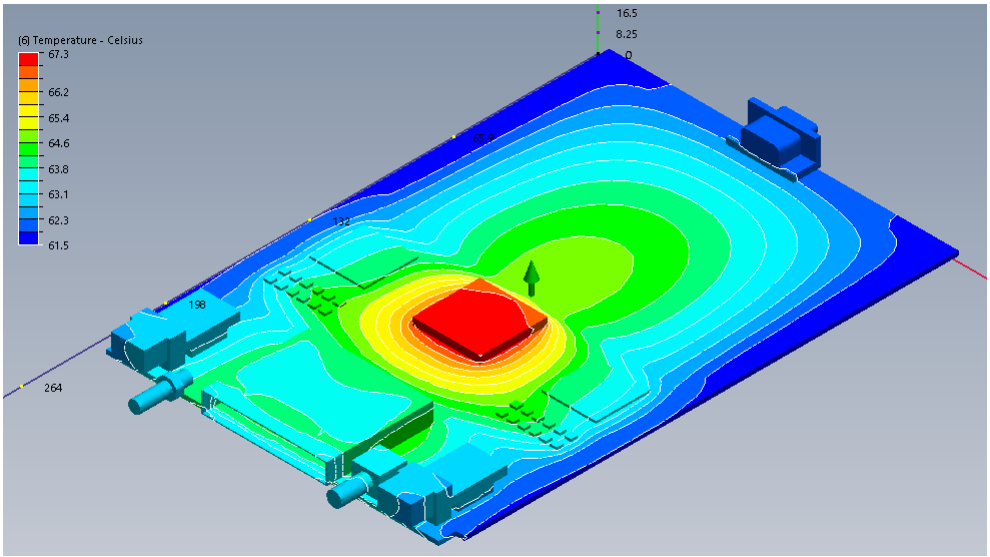


Figure 3.14: Symmetrical thermal plot of the D-Engine PCB.

The first thing to note is that the simulations suggest that $T_{ej} = 67.3°C - 61.5°C = 5.8°C$, not $15°C$ as conservatively estimated in the previous calculations (for the FPGA). The junction temperature T_j for the FPGA is now $65.5°C$ or $67.3°C$, respectively. If the two simulations are compared it can be seen that the FPGA has a maximum temperature $0.8°C$ lower in the asymmetrical layout. This is not a significant difference and the symmetrical layout also has the advantage

of keeping the mirrored components at a similar temperature which could result in them operating more consistently with respect to each other. The engineers responsible for the layout of the PCB felt that the small temperature drop gained from the asymmetrical layout was not worth the increased complexity of the PCB trace layout; hence the symmetrical layout was selected.

3.1.9 Sampler/ADC module conceptual design

A conceptual layout for the Sampler/ADC module can be seen in Figure 3.15.

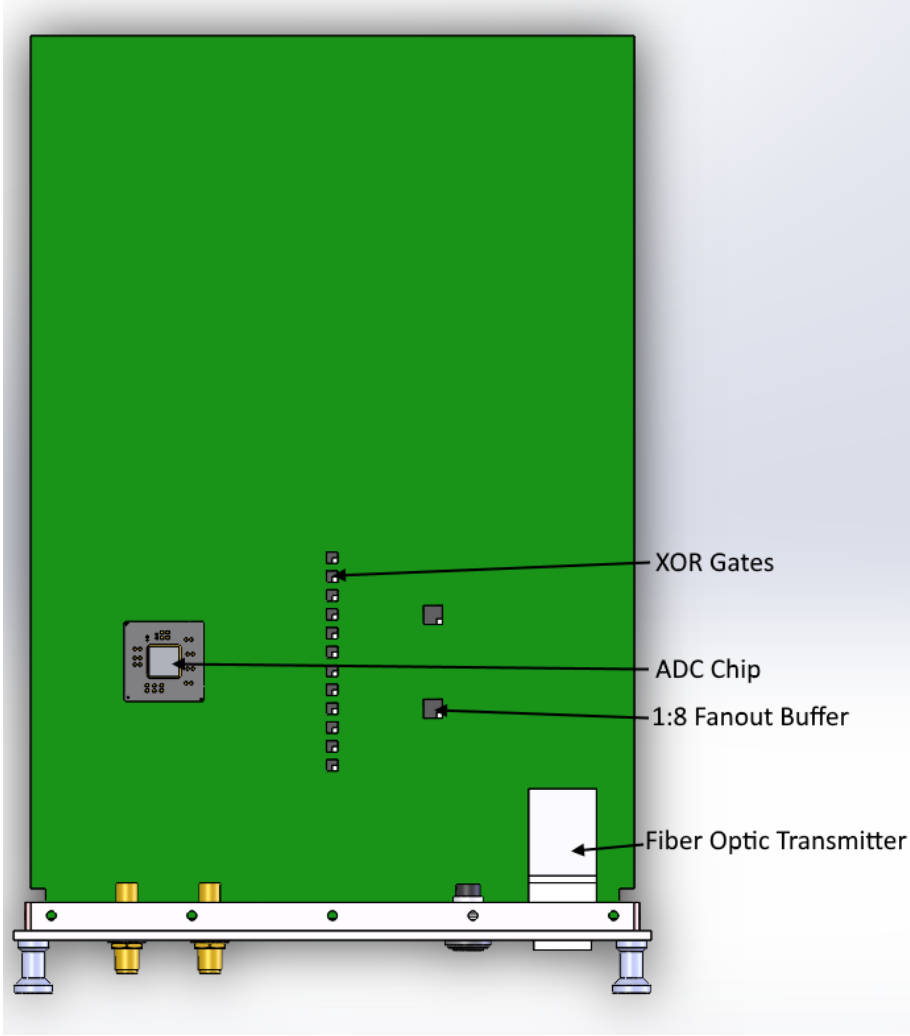


Figure 3.15: Layout of the Sampler/ADC PCB design.

The hot components are deliberately placed as close as possible to the side walls to minimise the resistance of the thermal path. Figure 3.16 is an isometric view of the Sampler/ADC showing how the lid touches down on hot components.

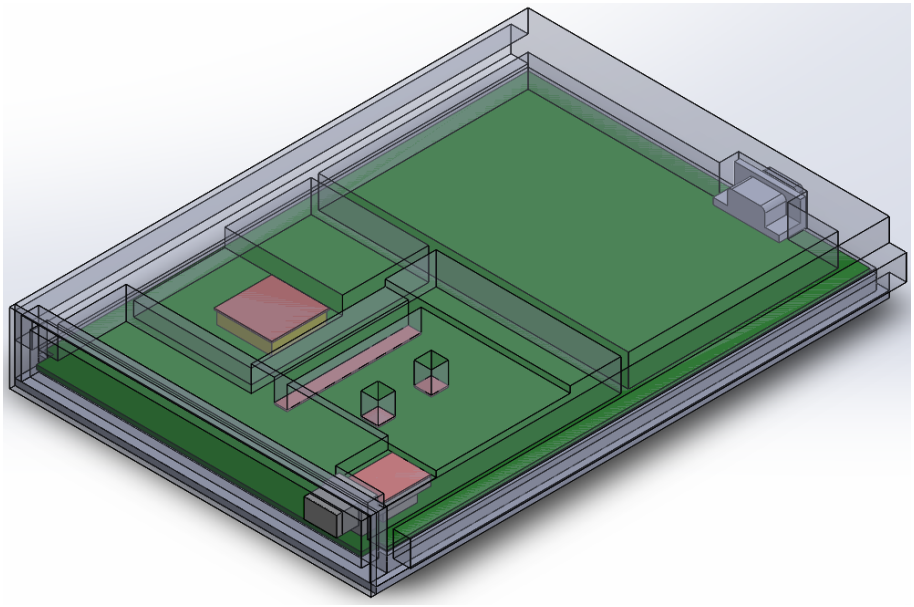


Figure 3.16: Isometric view of the Sampler/ADC module showing the lid (transparent) touching down on hot components.

A sectional view of the ADC chip thermal interface to the module lid is shown in Figure 3.17. The small conductive surface area of the ADC chip is mated to a copper heat spreader with a thermal interface material to ensure there are no air gaps (which would act as a thermal insulator). This heat spreader is then mated to the Sampler/ADC module lid (also with a thermal interface material). This is done as copper has a thermal conductivity of 395 $^{\mathrm{W}}/_{\mathrm{mK}}$, two to three times that of aluminium (121 $\rightarrow$ 208 $^{\mathrm{W}}/_{\mathrm{mK}}$). This spreads the heat to a larger surface area allowing the aluminium lid to dissipate the heat more effectively. A completely copper lid was not considered as it was deemed too costly and was not required to achieve the necessary cooling for this module.

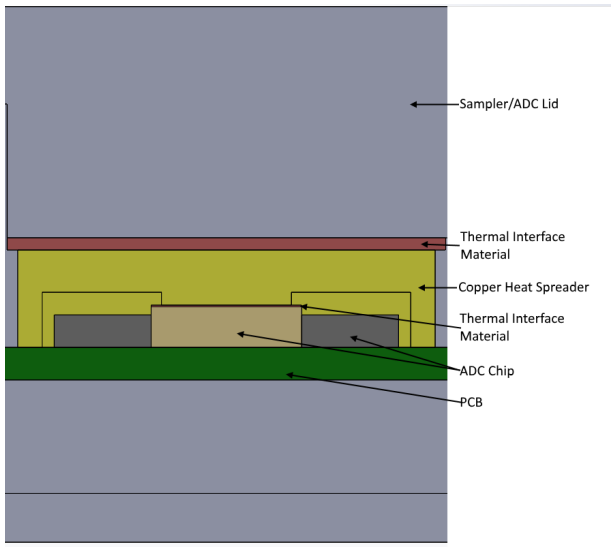


Figure 3.17: Cross-section of the ADC thermal interface to module lid.

Table 3.3 shows the maximum estimated power dissipation of the main components in the Sampler/ADC module.

Component	Power (W)	Qty.	Total power (W)
ADC	5.00	1	5.00
Fiber Optic Transmitter	1.45	1	1.45
XOR Gates	0.21	12	2.52
1:8 Fanout Buffer	1.77	2	3.54
Other	8.33	1	8.33
		Total	**20.84**

Table 3.3: Estimated maximum power/thermal budget for the Sampler/ADC high-power components.

Two thermal simulations were run. In the first, an aluminium heat spreader (see Figure 3.18) was used and in the second, a copper one (see Figure 3.19). The previously calculated surface temperature of $61.5°C$ was used as the boundary condition on the bottom surface of the two guide rails on the Sampler/ADC enclosure lid. Convection (and radiation) were ignored in the simulation as there is little to no air flow within and around the modules.

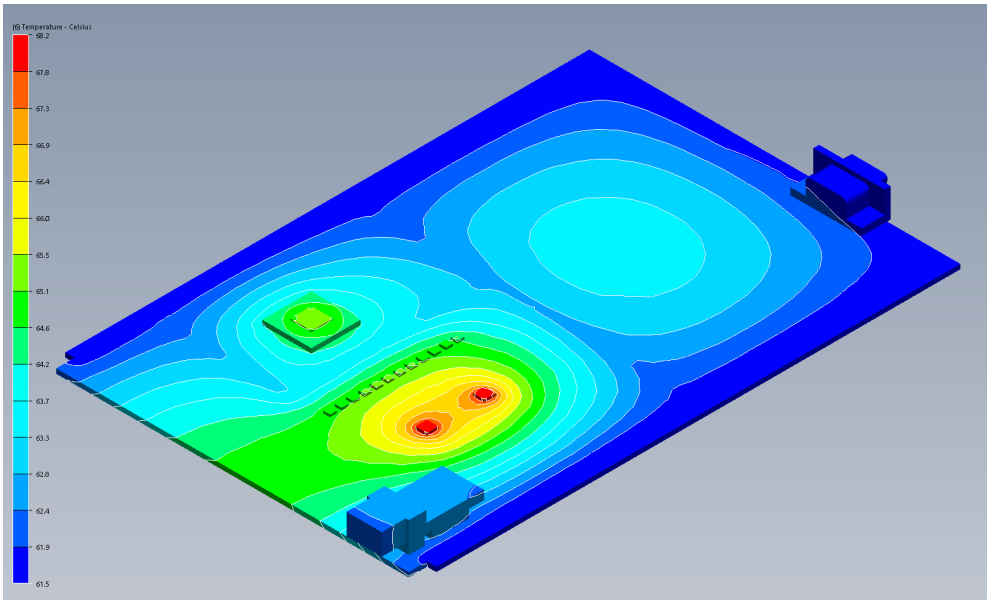


Figure 3.18: Thermal plot of the Sampler/ADC PCB with an aluminium heat spreader.

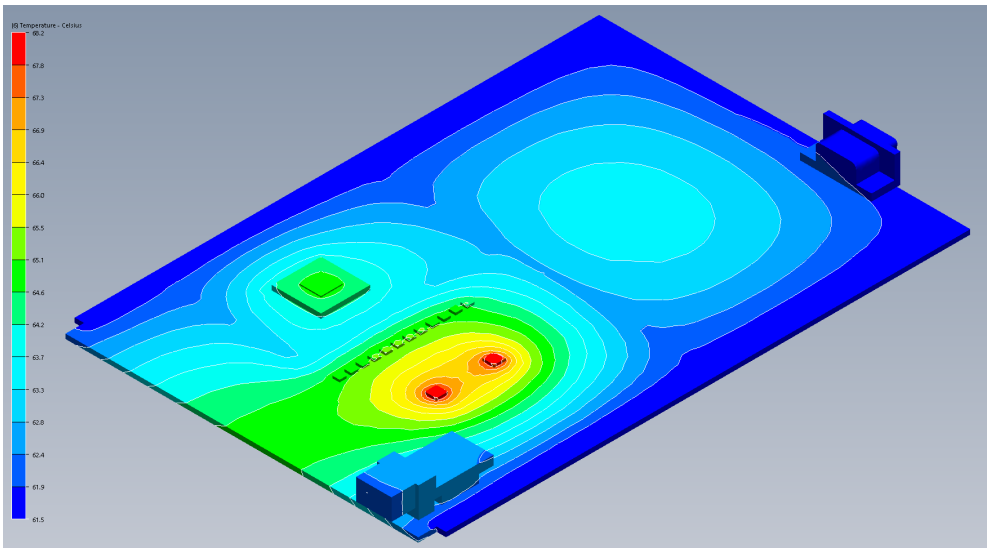


Figure 3.19: Thermal plot of the Sampler/ADC PCB with a copper heat spreader.

The first thing to note is that the simulations suggest that $T_{ej} = 68.3°C - 61.5°C = 6.8°C$, not $15°C$ as conservatively estimated in the previous calculations. The junction temperature T_j for the ADC is now $65.5°C$ with an aluminium heat spreader or $65.1°C$ with a copper heat spreader. If the two simulations are compared it can be seen that the ADC has a maximum temperature $0.4°C$ less with a copper heat spreader. This is not a significant difference. Nevertheless, our head engineer still felt we should use the copper heat spreader as the ADC chip had been found to run at quite a high temperature on prototypes previously investigated. The electrical team was not as concerned about the 1:8 fanout buffer which was shown to run at $68.2°C$ - the hottest component - and felt that it would be unlikely that it would dissipate full power. Even at this temperature it was still operating $16.8°C$ below its $85°C$ maximum operating temperature.

3.1.10 Sample Clock Generator module conceptual design

A conceptual layout for the Sample Clock Generator (SCG) module can be seen in Figure 3.20.

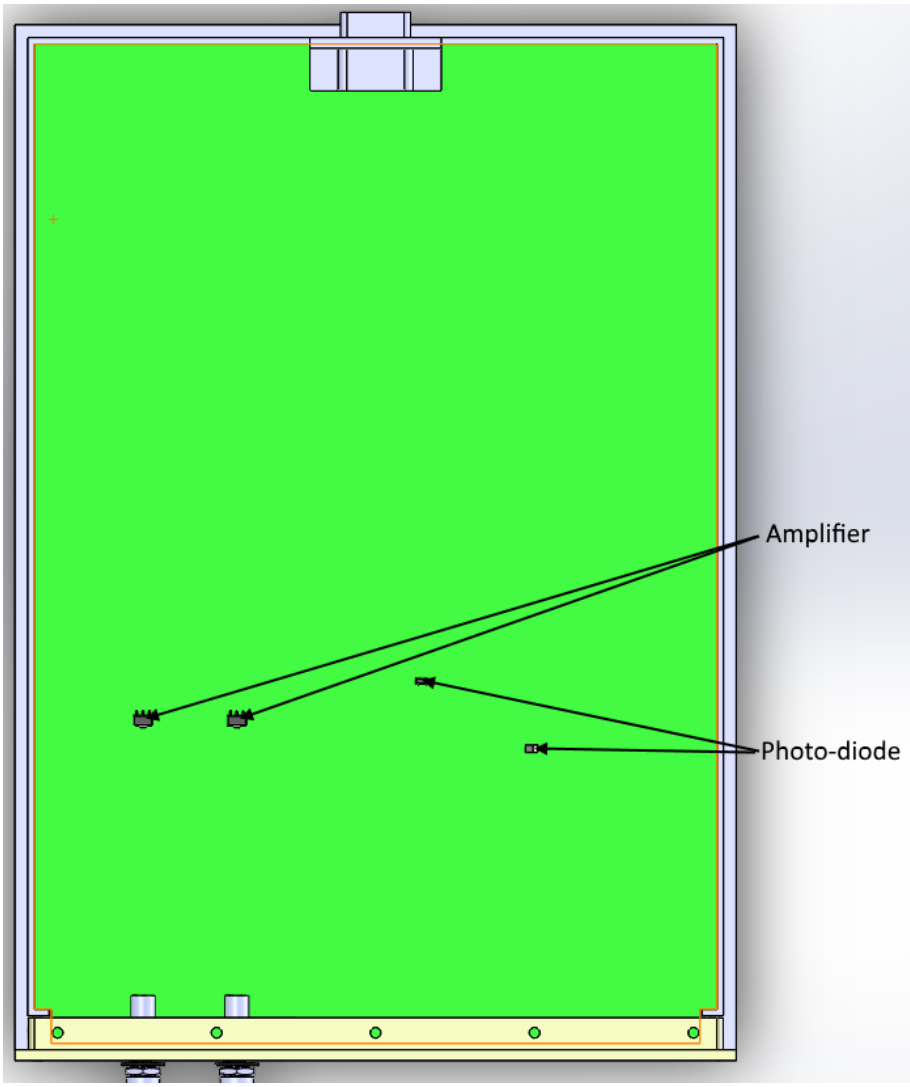


Figure 3.20: Layout of the Sample Clock Generator PCB design.

This module had very few components and they did not dissipate much power. This being said they all had a small surface area which could result in high temperatures if heat was not dissipated efficiently. The module lid touches down on all "hot" components to allow heat to conduct up through the lid to its sides, where it escapes to the side walls of the main housing.

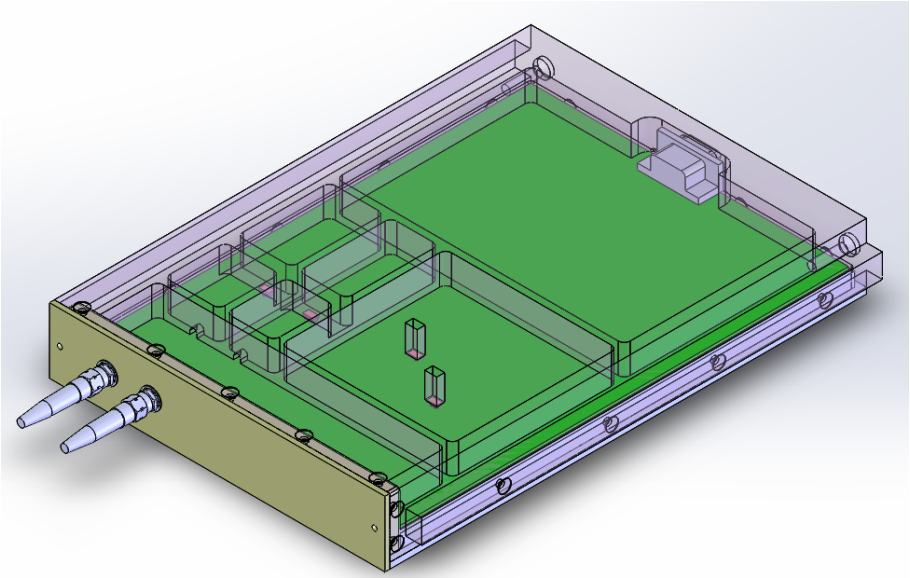


Figure 3.21: Isometric view of the Sample Clock Generator module showing the lid (transparent) touching down on hot components.

Table 3.4 shows the maximum estimated power dissipation of the main components in the Sample Clock Generator module.

Component	Power (W)	Qty.	Total power (W)
Amplifiers	1.6	2	3.2
Photo-diode 1	0.16	1	0.16
Photo-diode 2	1.2	1	1.2
		Total	**4.56**

Table 3.4: Estimated maximum dissipated power/thermal budget for the Sample Clock Generator high-power components.

A thermal simulation of the Sample Clock Generator was run. The previously calculated surface temperature of $61.5°C$ was used as the boundary condition on the bottom surface of the two guide rails on the Sample Clock Generator enclosure lid. Convection (and radiation) were ignored in the simulation as there is little to no air flow within and around the module.

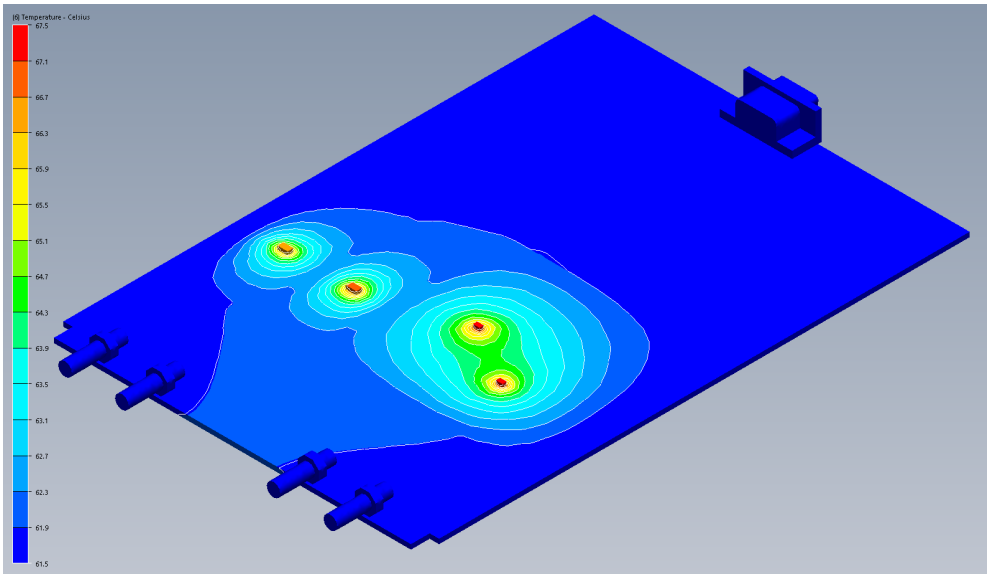


Figure 3.22: Thermal plot of the Sample Clock Generator PCB.

The maximum junction temperature is seen in the photo-diodes, $T_{ej} = 67.5°C - 61.5°C = 6.0°C$, not $15°C$ as conservatively estimated in the previous calculations. The junction temperatures T_j for the amplifiers are now $67.1°C$ and $66.7°C$. These values were deemed acceptable as they were $17.5°C$ to $18.3°C$ below their maximum allowable operating temperature of $85°C$.

3.1.11 Power Supply Unit module conceptual design

A conceptual layout for the Power Supply Unit (PSU) module can be seen in Figure 3.23. This module does not share the same basic chassis design as the D-Engine, Sampler/ADC, Sample Clock Generator and Radio Frequency Conditioning Unit (RFCU). It forms part of the rear wall of the Digitiser main enclosure to ensure that the heat dissipated by the PSU as a result of its inefficiency escapes directly through the rear wall.

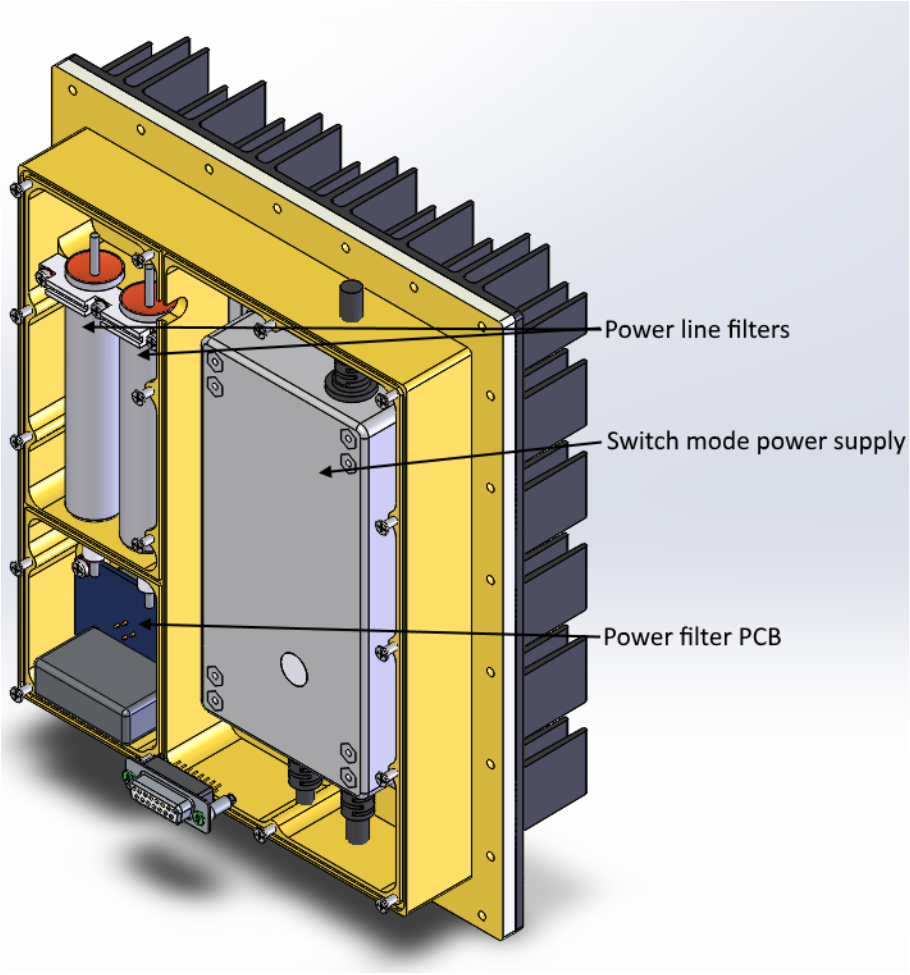


Figure 3.23: Layout of the Power Supply Unit design.

The only component in this module which dissipates heat is the switch mode power supply (see Figure 3.23). It was mated to the outer surface of the PSU module with a thermal interface material to allow the heat to dissipate directly to the back wall of the Digitiser main enclosure.

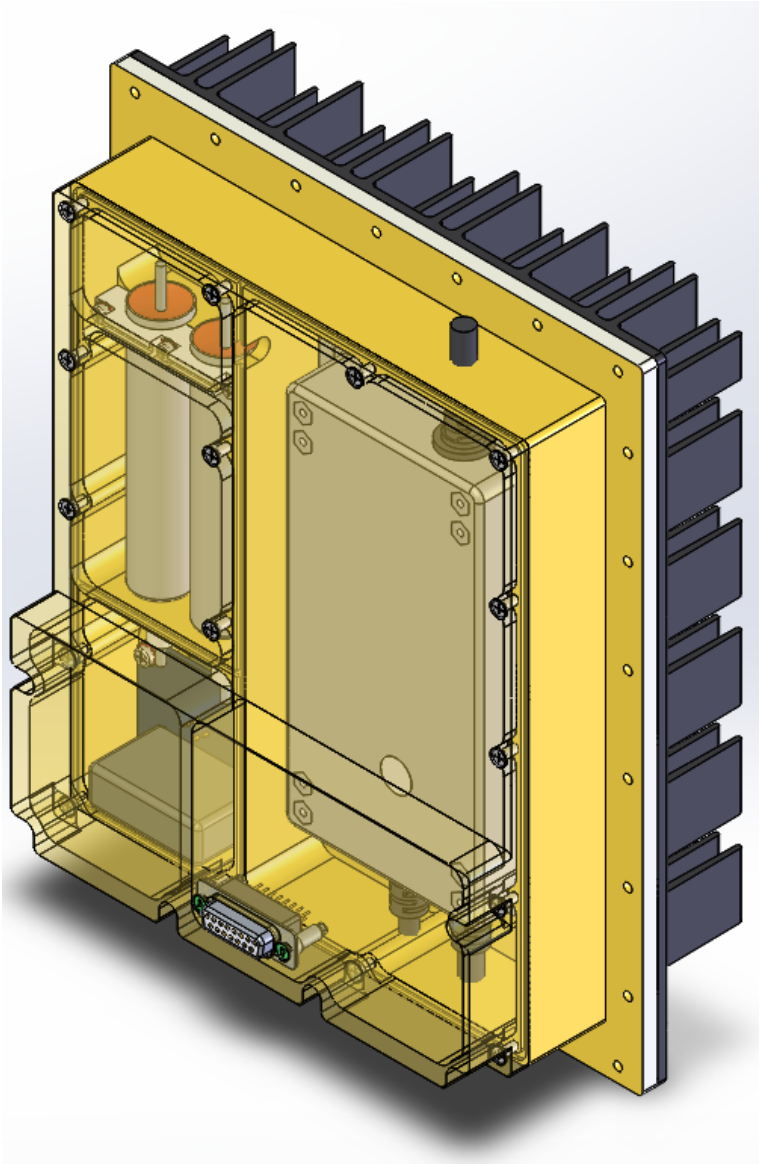


Figure 3.24: Isometric view of the PSU module showing the lid (transparent).

Table 3.4 shows the maximum estimated power dissipation of the switch-mode power supply unit within the PSU module.

Component	Power (W)	Qty.	Total power (W)
Switch-mode power supply	14.2	1	14.2
		Total	**14.2**

Table 3.5: Estimated maximum dissipated power/thermal budget for the PSU.

A thermal simulation of the PSU module was run. The previously calculated surface temperature of $61.5°C$ was used as the boundary condition on the back surface of the PSU enclosure lid. Convection (and radiation) were ignored in the simulation as there was little to no air flow within and around the module (excluding the back wall's previously calculated value).

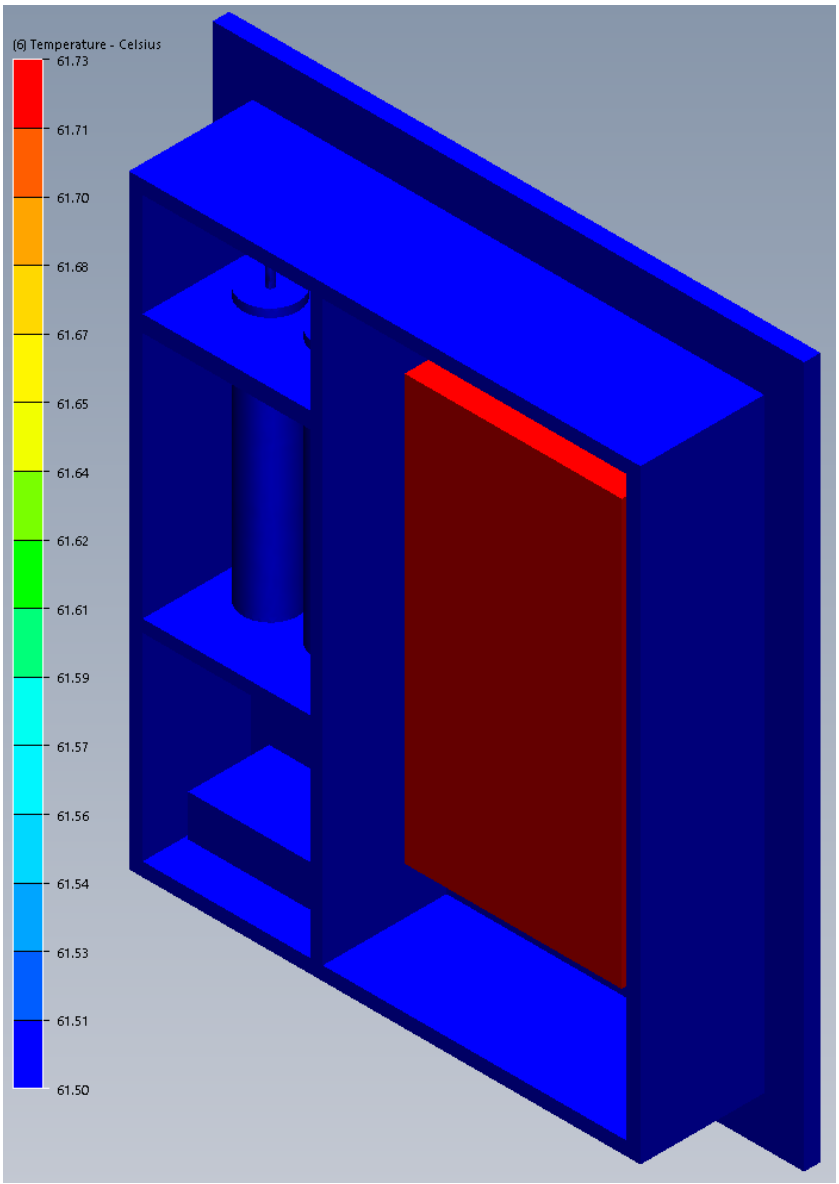


Figure 3.25: Thermal plot of the PSU module.

As a result of the large surface area of the switch-mode power supply in comparison to its power dissipation and the fact that the thermal path to the outer enclosure is very short, its surface temperature is $T_{ej} = 61.7°C - 61.5°C = 0.2°C$. This value was far below the $85°C$ maximum allowable operating temperature; hence the thermal design for the PSU module was accepted.

3.1.12 Radio Frequency Conditioning Unit (RFCU) and Backplane module design

The Radio Frequency Conditioning Unit (RFCU) module was designed by a 3rd party and hence the mechanical design was managed by them using our module design concept. The chassis had the same outer dimensions as the D-Engine, Sampler/ADC and SCG (see Figure 3.26).

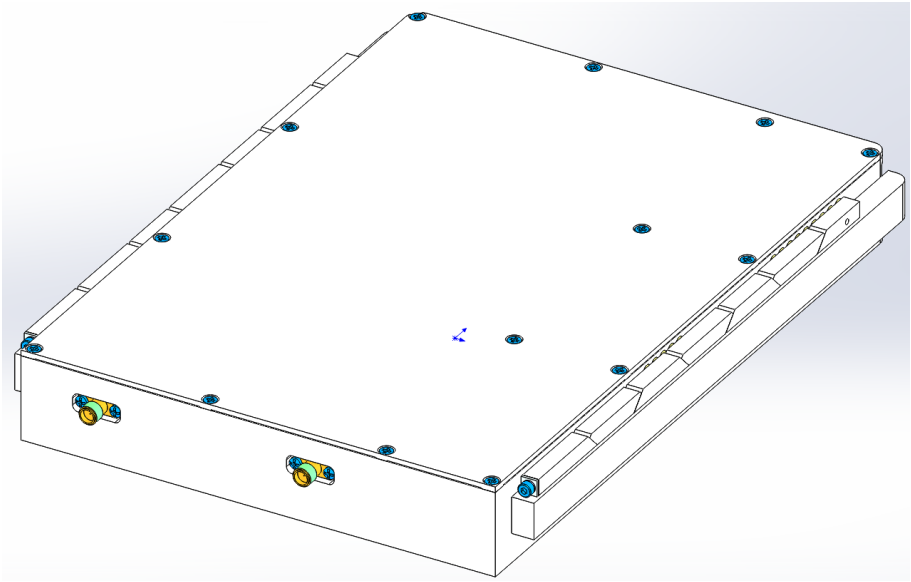


Figure 3.26: RFCU module.

Table 3.6 shows the maximum estimated power dissipation of the main components in the RFCU module.

Component	Power (W)	Qty.	Total power (W)
Positive supply	4	1	4
Negative supply	0.08	1	0.08
		Total	**4.08**

Table 3.6: Estimated maximum dissipated power/thermal budget for the RFCU high-power components.

The Backplane module layout can be seen in Figure 3.27. Its function is to split and distribute output from the power supply to the various modules. It contains no components which dissipate any power and hence no thermal simulation of it was necessary.

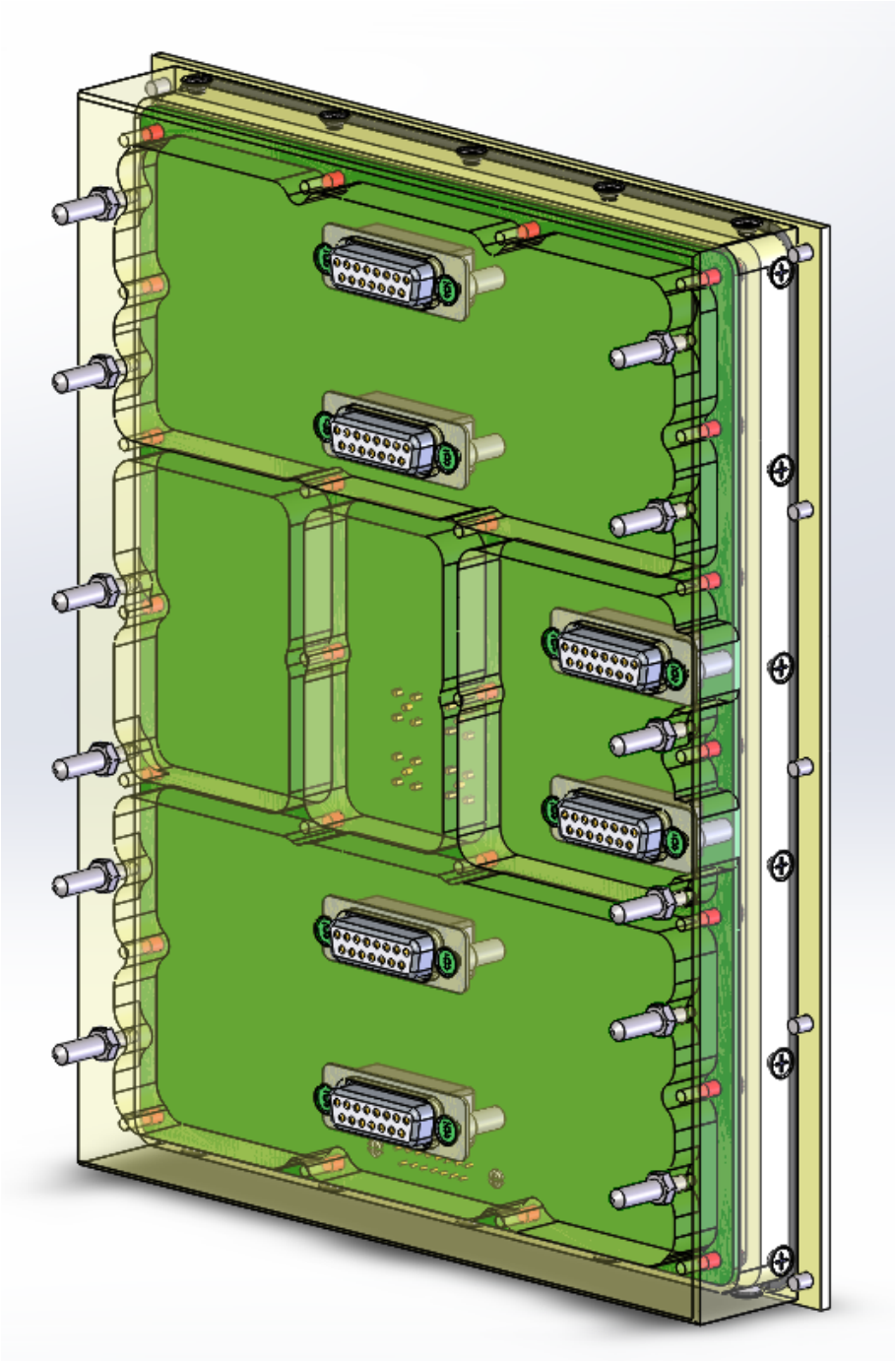


Figure 3.27: Layout of the Backplane.

3.1.13 Thermal simulation for the whole system

All the modules were then combined into the overall system as seen in Figure 3.28 and thermal simulations run - firstly without and then with solar radiation.

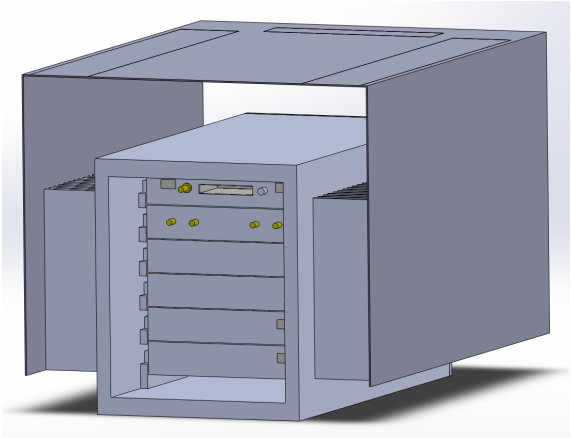


Figure 3.28: Front sectioned view of the thermal model showing the modules in the outer enclosure with a solar shield.

The components within the modules of the Digitiser were assigned power values as per the power/thermal budget seen in Table 3.7. The thermal model is enclosed in a boundary volume as seen in Figure 3.29. These values are determined by calculating five times the width and length of the enclosure and eight times the height of the enclosure. The enclosure is also offset by $382.5mm$ in the vertical direction so that it is $\frac{3}{8}$ of the total height from the floor of the boundary volume. This is to allow sufficient space above and to the sides of the model to prevent the natural convection simulation from being influenced by the boundaries. Furthermore the pressure is 0 Pa gauge on all surfaces of the boundary volume and the ambient air temperature is $40°C$.

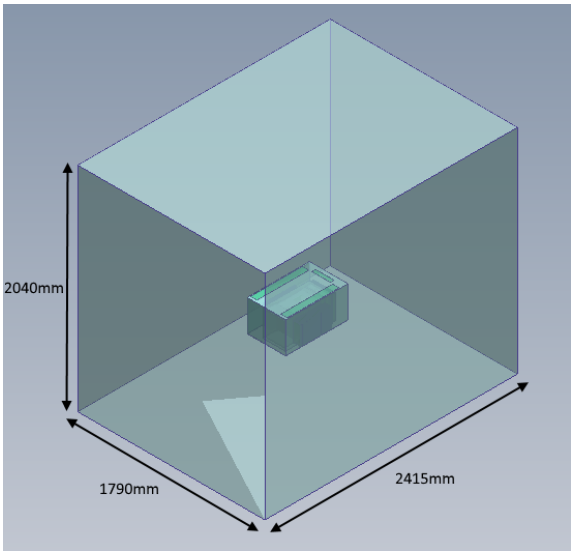


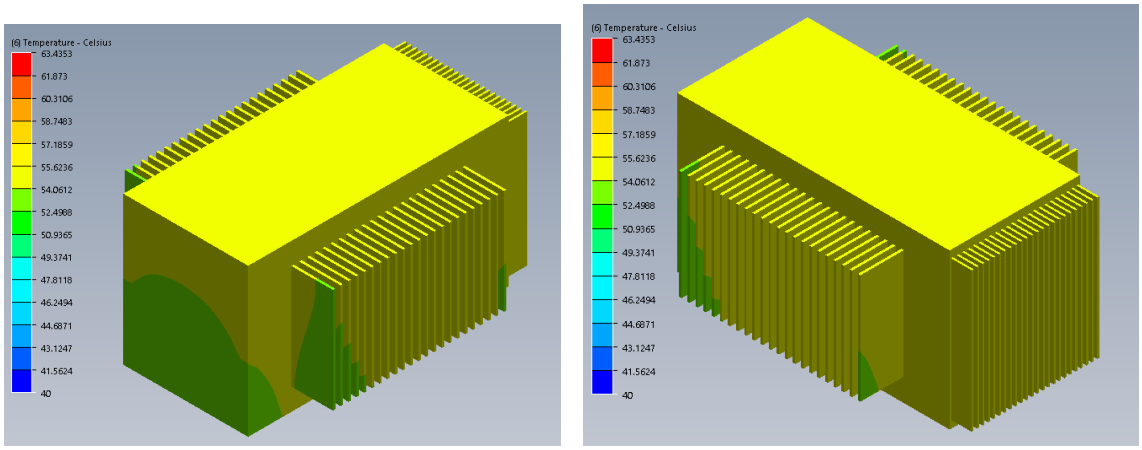
Figure 3.29: Calculated boundary volume for the overall Digitiser thermal simulation.

Component	Power (W)	Qty.	Total power (W)
FPGA	14.5	1	14.5
De-Mux	2.7	2	5.4
SFP+ Tranceivers	1.0	4	4.0
Fibre Optic Receiver	1.55	2	3.1
LVDS Buffers	0.1	24	2.4
Other	9.37	1	9.37
		D-Engine Sub-total	**38.77**
ADC	5	1	5
Fiber Optic Transmitter	1.45	1	1.45
XOR Gates	0.21	12	2.52
1:8 Fanout Buffer	1.77	2	3.54
Other	8.33	1	8.33
		Sampler Sub-total	**20.84**
		x2	**41.68**
Amplifiers	1.6	2	3.2
Photo-diode 1	0.16	1	0.16
Photo-diode 2	1.2	1	1.2
		SCG Sub-total	**4.56**
Switch-mode power supply	14.2	1	14.2
		PSU Sub-total	**14.2**
Positive supply	4	1	4
Negative supply	0.08	1	0.08
		RFCU Sub-total	**4.08**
		x2	**8.16**
		Total	**107.37**
		Solar radiation	**71.82**

Table 3.7: Estimated maximum power/thermal budget for the Digitiser high-power components.

Thermal simulation with no solar radiation

As mentioned before the first thermal simulation did not take into account the solar radiation load (and radiation as a whole) on the Digitiser. This was done to allow a comparison to laboratory testing of the Digitiser as detailed in the following chapter.



(a) Front isometric view of Digitiser thermal model.

(b) Rear isometric view of Digitiser thermal model.

Figure 3.30: Digitiser thermal model.

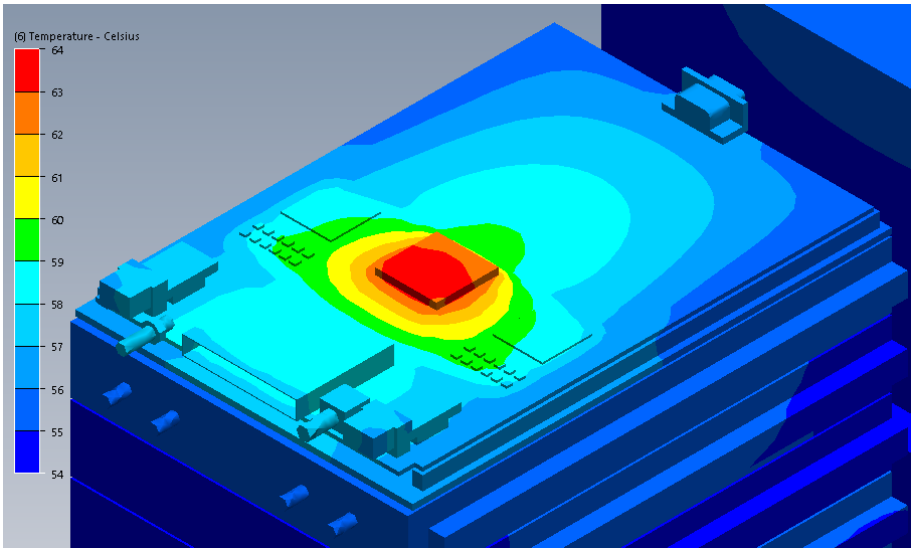


Figure 3.31: Thermal plot of the D-engine.

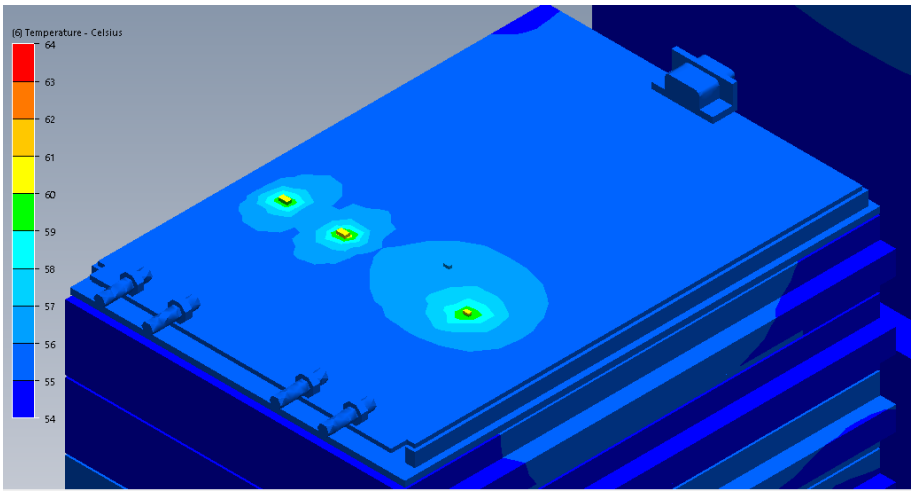


Figure 3.32: Thermal plot of the SCG.

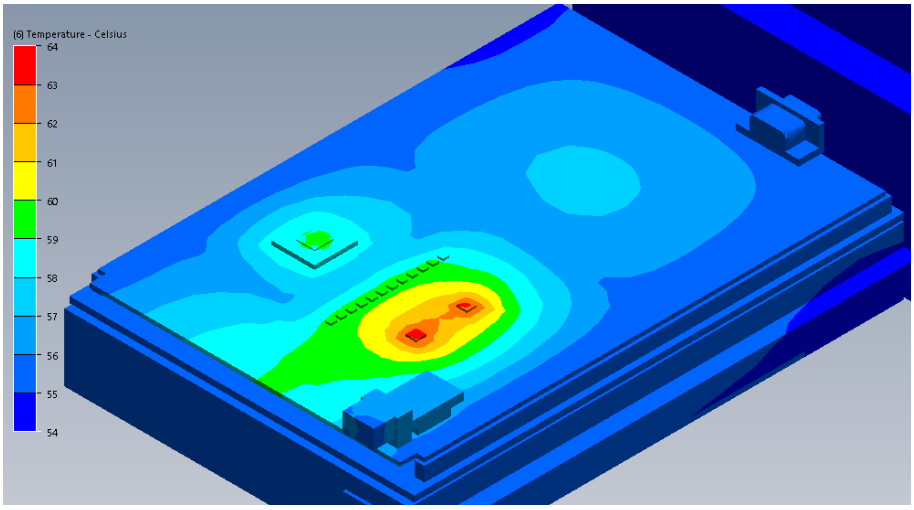


Figure 3.33: Thermal plot of the horizontal polarisation sampler.

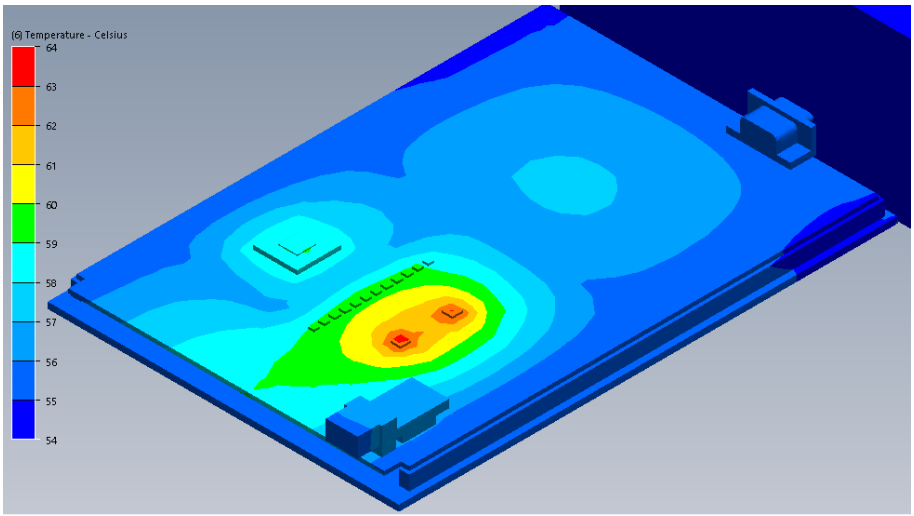


Figure 3.34: Thermal plot of the vertical polarisation sampler.

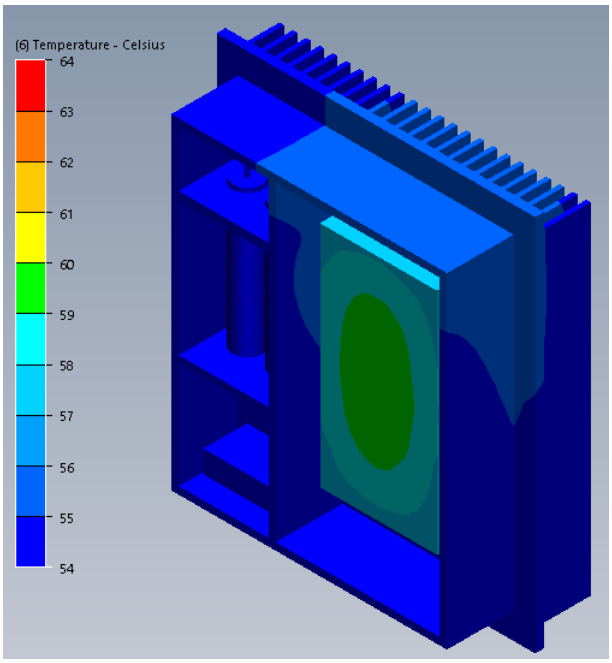


Figure 3.35: Thermal plot of the PSU.

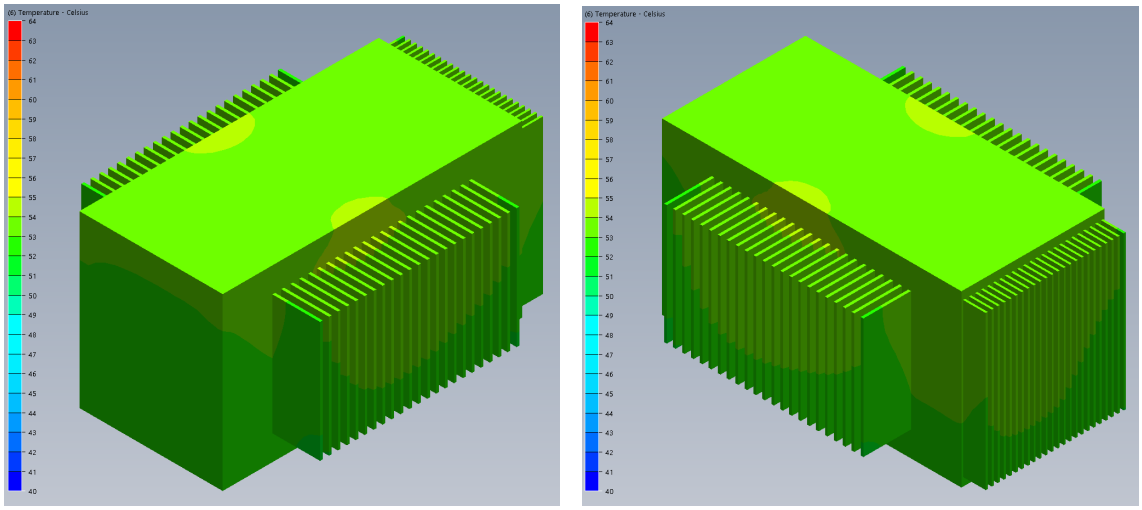
Component Description	Temp. ($°C$) in stack	Temp. ($°C$) individual modules
D-Engine FPGA Die	63	67
D-Engine FPGA Ambient	60	65
D-Engine ADC Optical	58	63.8
D-Engine ADC PSU	58	63.8
Sampler Horizontal Die	59	68.3
Sampler Horizontal PCB	58	63.7
Sampler Vertical Die	58	68.3
Sampler Vertical PCB	58	63.7
PSU	59	61.7

Table 3.8: Digitiser temperatures (no solar radiation) compared to previously calculated values for the individual modules in isolation.

Table 3.8 indicates that the average temperature calculated in the thermal simulations is typically 4 to 6 $°C$ lower than the previously calculated values for the individual modules. This further suggests that this solution is feasible as the maximum operating temperature of the components moves further below the maximum allowable value of $85°C$.

Thermal simulation with solar radiation

The second simulation included thermal radiation and the additional $71.82W$ of solar radiation on the solar shield calculated in the previous chapter. The boundary volume, pressure and ambient temperature remained unchanged for this simulation.



(a) Front isometric view of Digitiser thermal model.

(b) Rear isometric view of Digitiser thermal model.

Figure 3.36: Digitiser thermal model with solar radiation.

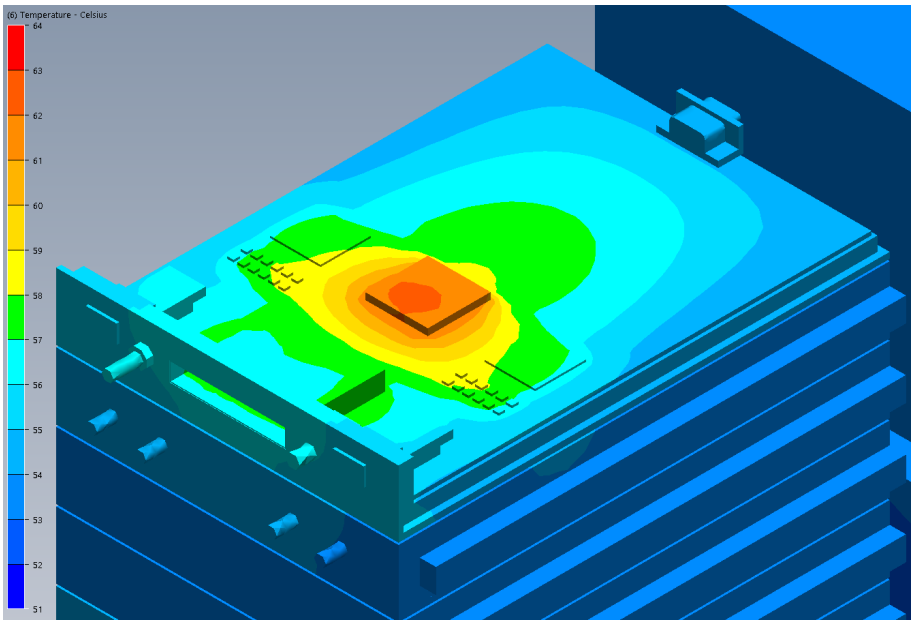


Figure 3.37: Thermal plot of the D-engine with solar thermal loading.

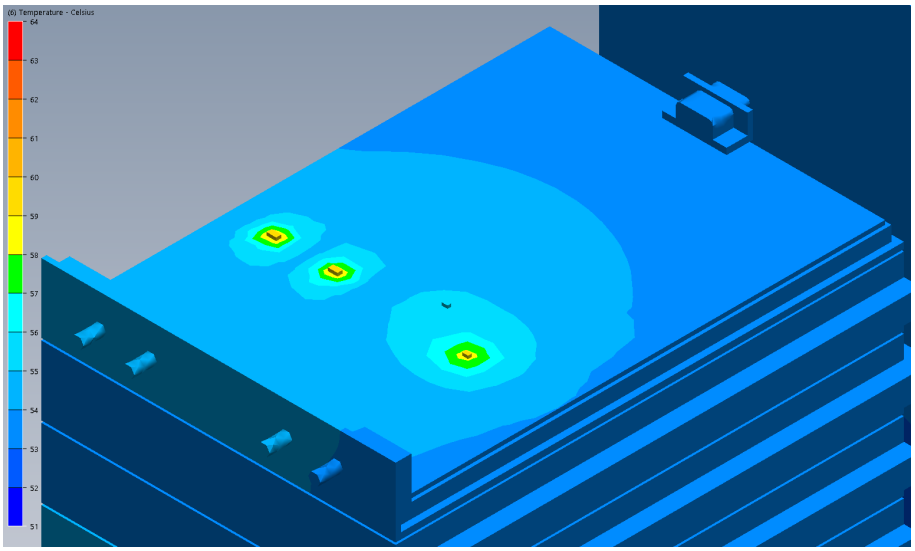


Figure 3.38: Thermal plot of the SCG with solar thermal loading.

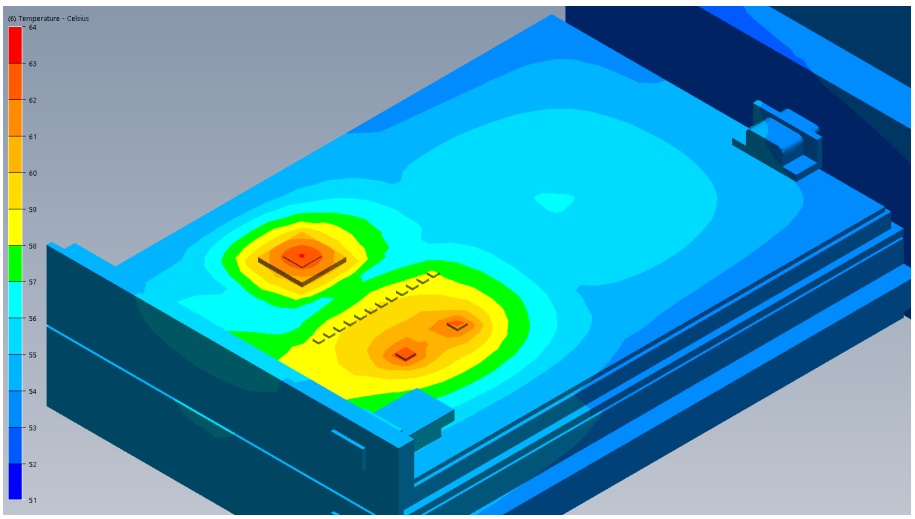


Figure 3.39: Thermal plot of the horizontal polarisation sampler with solar thermal loading.

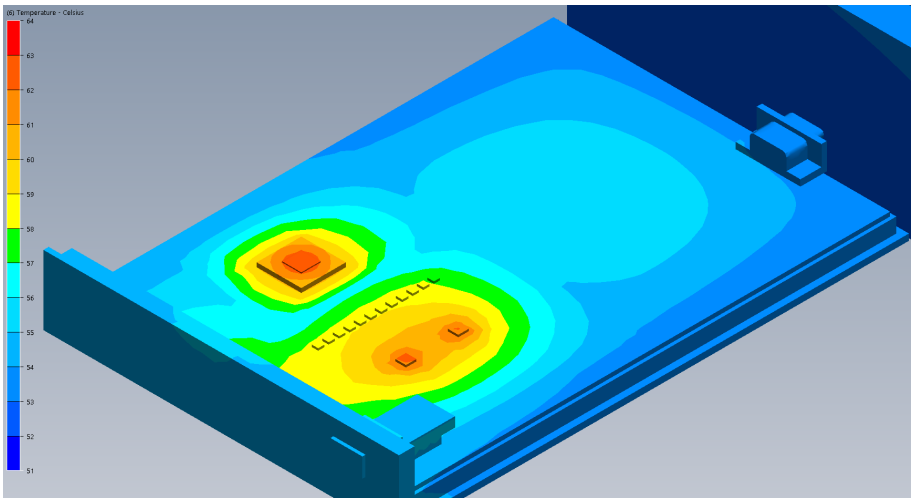


Figure 3.40: Thermal plot of the vertical polarisation sampler with solar thermal loading.

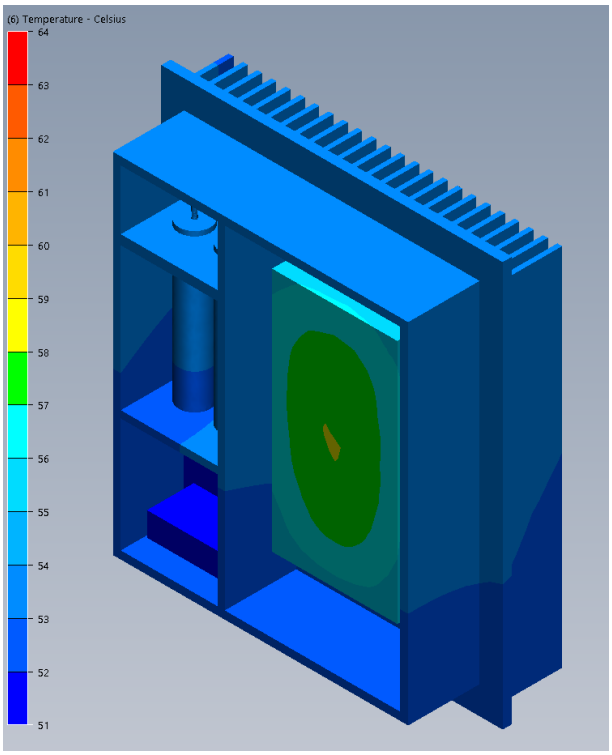


Figure 3.41: Thermal plot of the PSU with solar thermal loading.

Component Description	Temp. ($^{\circ}C$) in stack	Temp. ($^{\circ}C$) individual modules
D-Engine FPGA Die	61	67
D-Engine FPGA Ambient	57	65
D-Engine ADC Optical	56	63.8
D-Engine ADC PSU	56	63.8
Sampler Horizontal Die	56	68.3
Sampler Horizontal PCB	55	63.7
Sampler Vertical Die	56	68.3
Sampler Vertical PCB	55	63.7
PSU	57	61.7

Table 3.9: Digitiser temperatures (with solar radiation) compared to previous individually calculated values with no solar loading.

Table 3.9 indicates that the average temperature of the modules in the stacked thermal model is some 6 to 8 $^{\circ}C$ lower than the individually calculated values. These values are also in fact roughly $2^{\circ}C$ lower than the non-solar radiation loading values. This is probably due to the extra heat dissipation offered by thermal radiation and also possibly the chimney effect created by the solar shield.

Chapter 4

Results and Experimental Validation

In order to validate the design presented in Chapter 2 and to verify the results of the numerical simulations presented in Chapter 3, we performed a series of experiments in a thermal chamber and collected in-situ measurements from the prototype Digitisers installed on telescope pedestals in the Karoo site of MeerKAT.

4.1 Thermal chamber testing

Digitiser thermal test configuration

This test configuration was used to perform the majority of environmental testing for the Digitiser. The diagram in Figure 4.1 shows the layout of the configuration. The required signal levels stated in this procedure assumed that all cable and component losses were compensated for such that the levels stated were applied to the input of the Digitiser. The following settings were used on the equipment for the test configuration:

1. Signal generator 1
    - Frequency = 1712MHz
    - Power level = -9 dBm
    - Reference oscillator = “internal”
2. Signal generator 2
    - Frequency = Set as per applicable test procedure
    - Power level = Set as per applicable test procedure
    - Reference oscillator = “external”
3. Noise source
    - Attenuation level = Set as per applicable test procedure
4. Spectrum analyzer
    - Set as per applicable test procedure

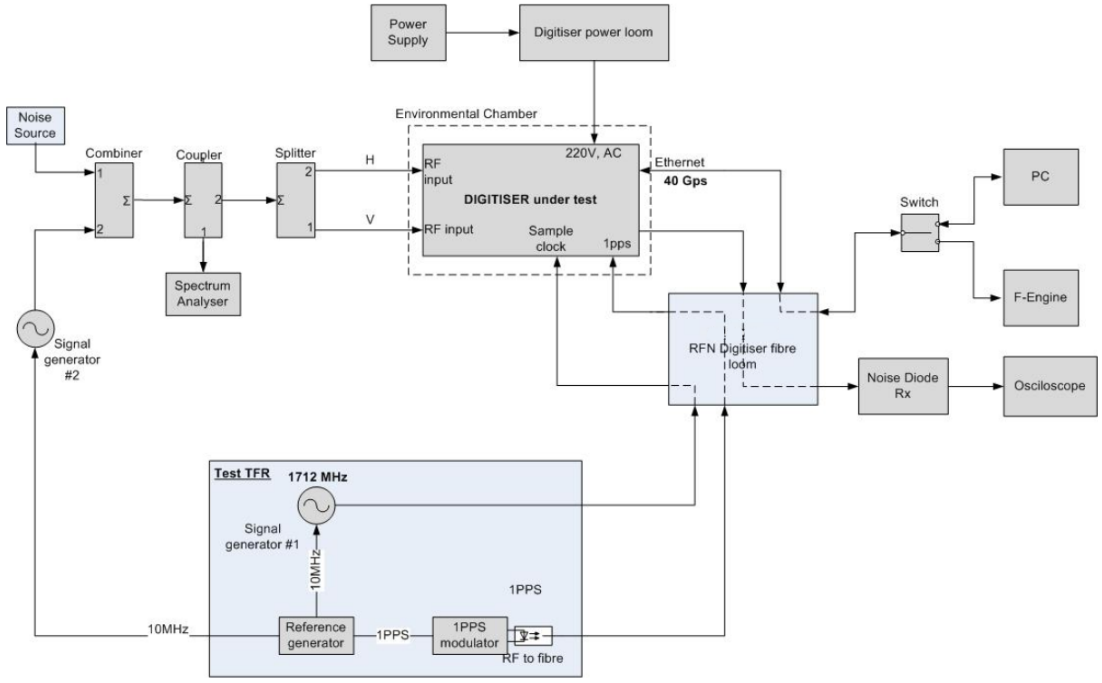


Figure 4.1: Digitiser configuration for laboratory-based environmental testing. [30]

5. DMC simulator
    - Python scripts were used to control and monitor the Digitiser
6. F-engine simulator
    - Not used for environmental tests
7. Environmental chamber
    - Environmental chamber configured according to the temperature profile given in Figure 4.2 [30]

Temperature profile

A temperature profile was designed to test the Digitiser at its minimum and maximum operating temperatures of $-5°C$ and $40°C$, respectively. The profile would need to maintain these minimum and maximum temperatures for a long enough period to check the stability of the thermal performance. A period of 180 minutes or 3 hours was agreed upon for each case. The Digitiser requirements also stated that it should be able to operate stably with a change of temperature of $2°C$ per 10 minutes and this was incorporated into the temperature profile. The temperature profile would be cycled as many times as possible within the test window afforded by the test facility so that we could be sure that the results were repeatable and that the Digitiser would be stable over a long period of operation. The thermal test profile can be seen in Figure 4.2 [30].

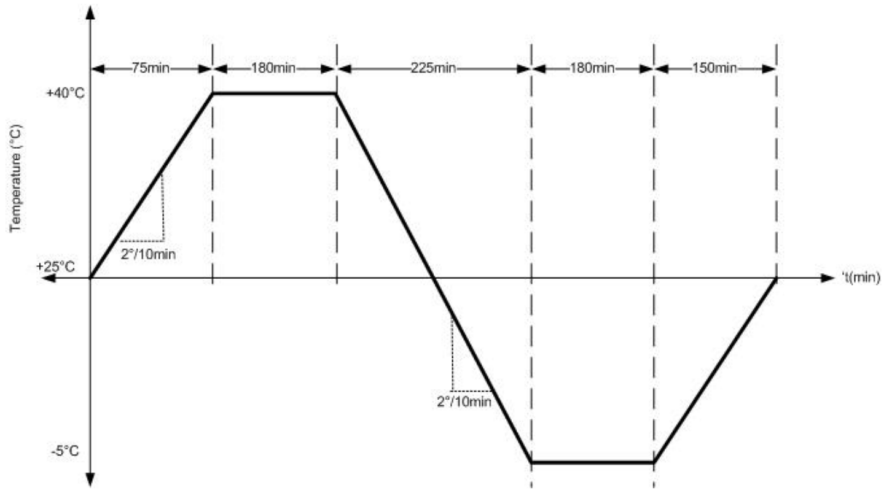


Figure 4.2: Temperature profile (based on MIL-STD 810) used for tests conducted in the thermal chamber. [18]

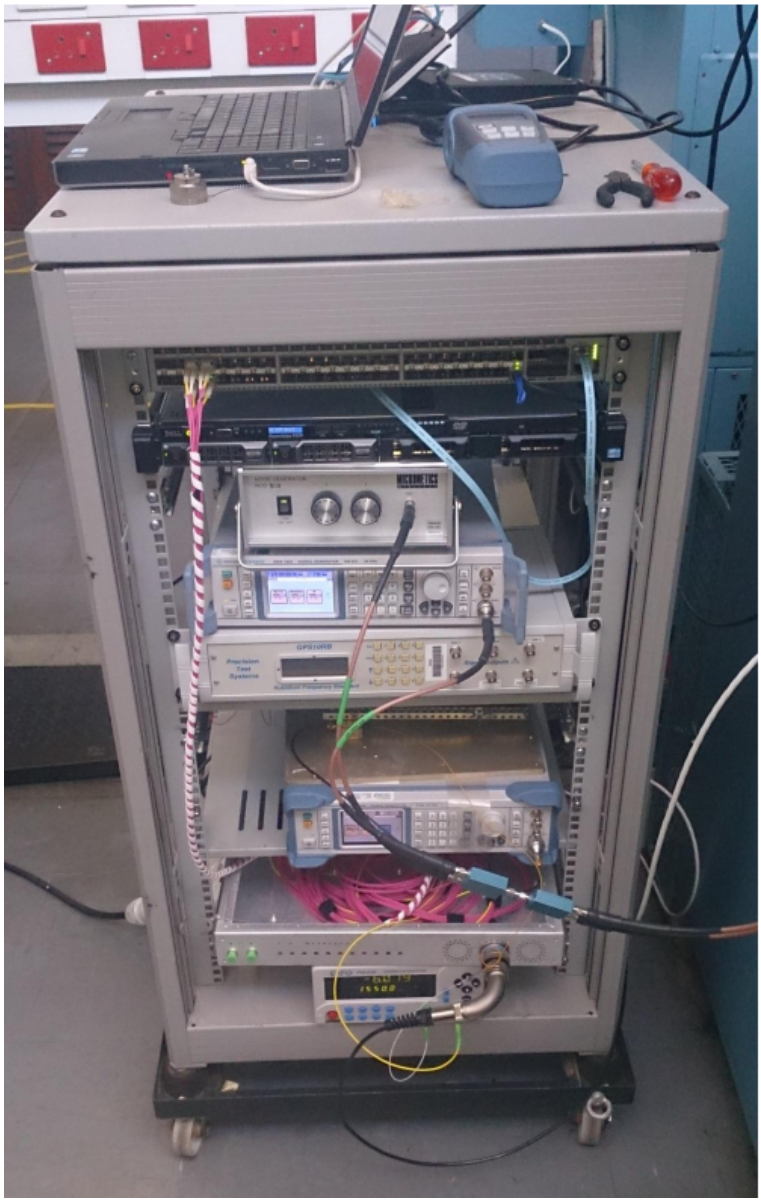


Figure 4.3: Environmental test equipment. [30]

Figure 4.4: Environmental test noise source. [30]

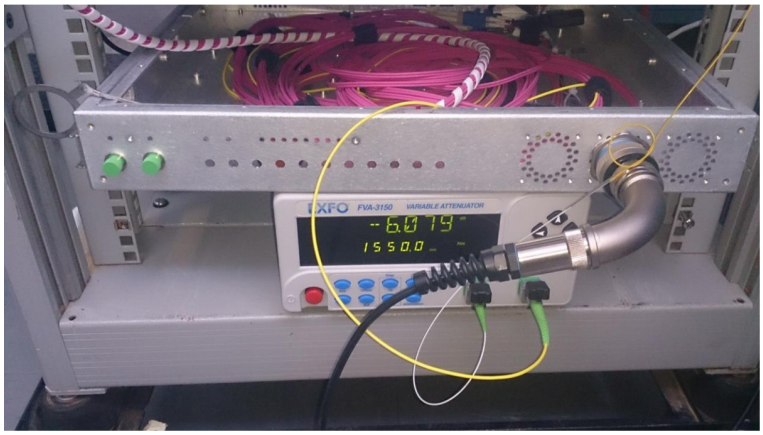


Figure 4.5: Environmental test optical attenuator. [30]

Figure 4.6: Environmental test clock source. [30]

Testing operational temperature limit with air temperature changes

The Digitiser was tested to ensure that all modules and components remained below their safe operating temperature limit of 85°C. The air temperature changes were bounded by the following requirements:

- Range: -5 to +40 °C
- Rate of change: 2 °C in 10 minutes (worst case)

The modules were all driven at their full capacity to simulate the worst case heat dissipation. A portion of the test data logs is provided in Figures 4.7, 4.8 and 4.9.

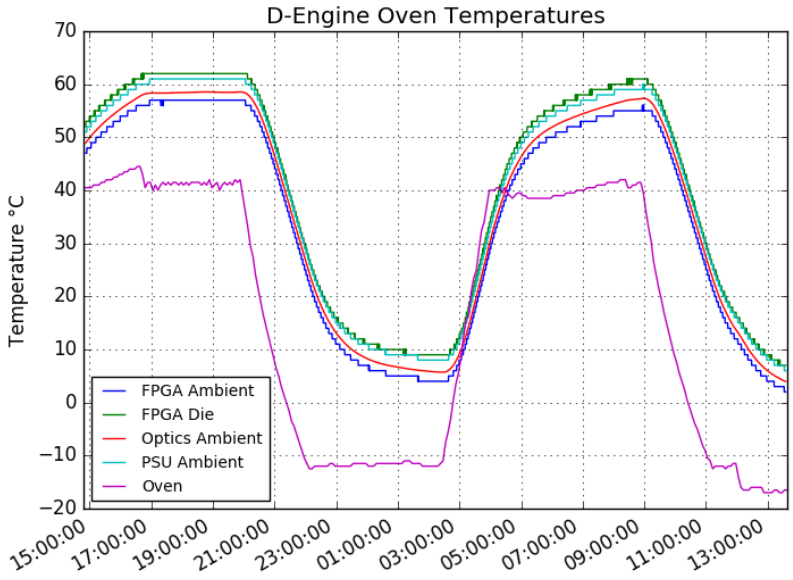


Figure 4.7: D-Engine temperatures recorded in the thermal chamber following cycles of the temperature profile in Figure 4.2.

The Digitisers continued to produce a coherent output throughout the test and all modules remained within their safe operating limit as can be seen in Figures 4.7, 4.8 and 4.9.

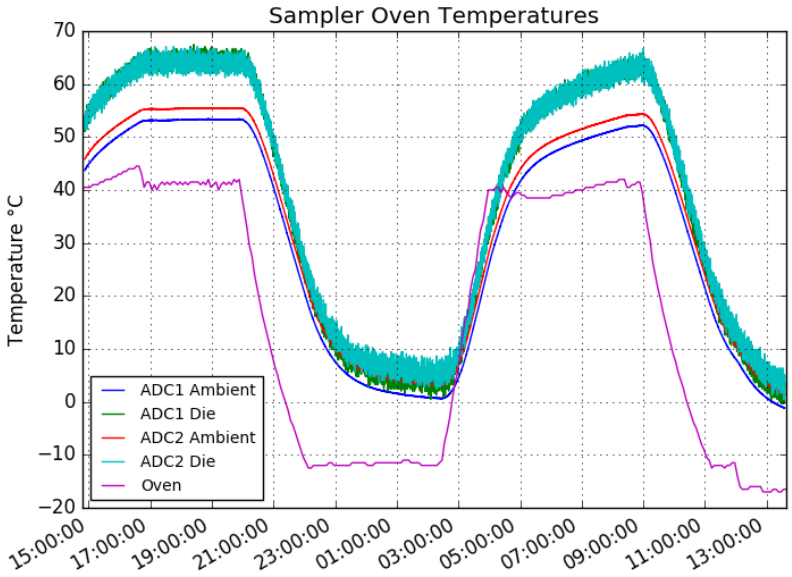


Figure 4.8: Sampler temperatures recorded in the thermal chamber following cycles of the temperature profile in Figure 4.2.

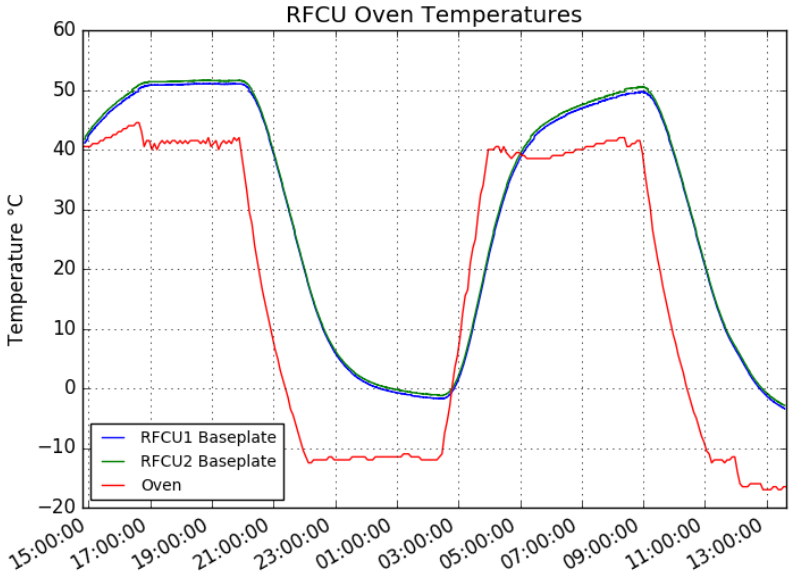


Figure 4.9: RFCU temperatures recorded in the thermal chamber following cycles of the temperature profile in Figure 4.2.

4.2 On-site temperature logs for the prototype Digitisers

Prototype Digitisers were placed on site on the completed telescope pedestals and tested for functionality. Sensor data was logged over a period of a few months to monitor temperature, amongst other things. Temperature logs are shown for Digitiser 003 (Figure 4.10, 4.11 and 4.12), Digitiser 004 (Figure 4.13, 4.14 and 4.15), Digitiser 005 (Figure 4.16, 4.17 and 4.18) and Digitiser 006 (Figure 4.19, 4.20 and 4.21). It can be seen from the graphs that there were offline periods where sensor data was not logged.

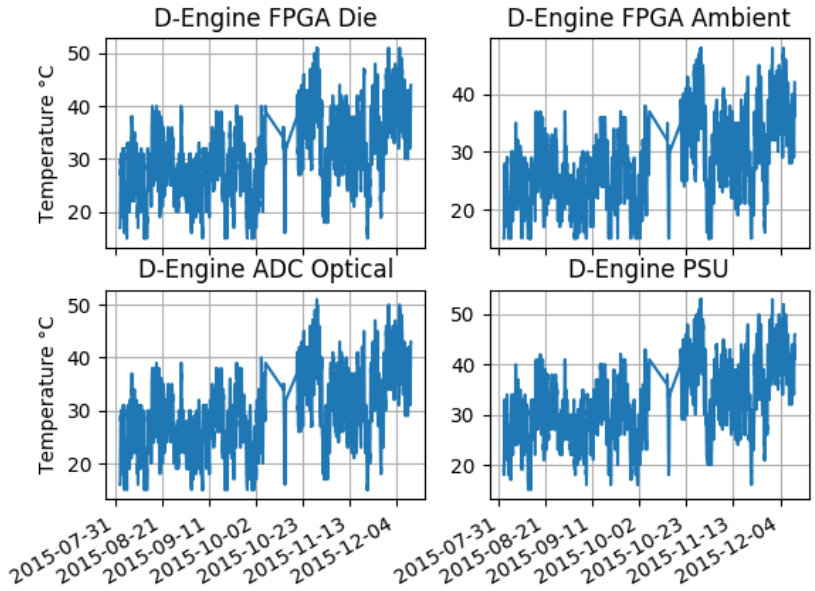


Figure 4.10: D-Engine temperature sensor values for Digitiser 003.

Component Description	Date time	Temp. ($°C$)
D-Engine FPGA Die	2015-10-29 09:33:52	51
D-Engine FPGA Ambient	2015-10-29 09:27:11	48
D-Engine ADC Optical	2015-10-29 09:39:27	51
D-Engine ADC PSU	2015-10-29 09:39:59	53
Sampler Horizontal Die	2015-10-29 15:13:39	70
Sampler Horizontal PCB	2015-10-29 09:40:29	48
Sampler Vertical Die	2015-10-29 15:06:19	69
Sampler Vertical PCB	2015-10-29 09:41:29	48
RFCU Horizontal Baseplate	2015-10-29 09:29:10	45
RFCU Vertical Baseplate	2015-10-29 09:29:10	45

Table 4.1: Digitiser 003 maximum temperatures logged from Aug 01 2015 to Dec 31 2015.

The maximum air temperatures recorded near Carnarvon were 37 and 38 $°C$ on the 28th and 29th of October 2015, respectively. These values are 3 and 2 $°C$ shy

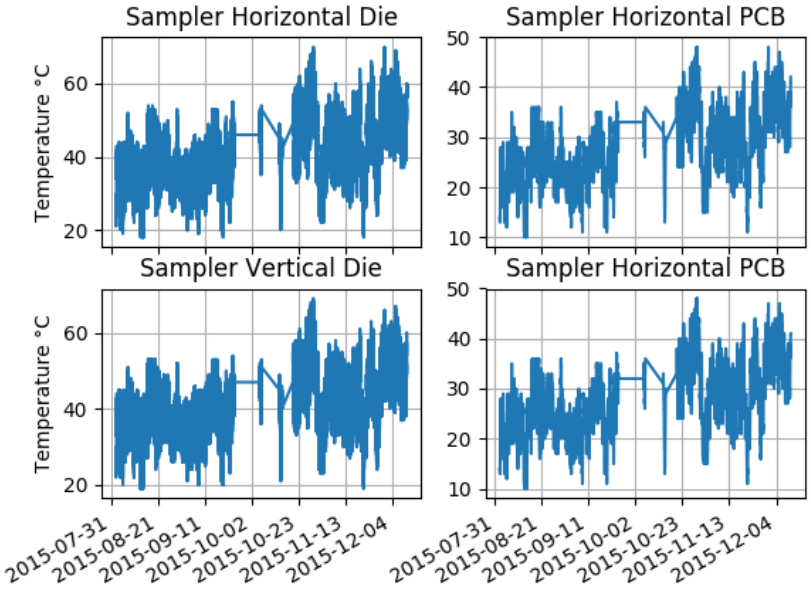


Figure 4.11: Sampler temperature sensor values for Digitiser 003.

Component Description	Date time	T($°C$)
D-Engine FPGA Die	2015-10-29 12:51:25	53
D-Engine FPGA Ambient	2015-10-29 14:39:13	50
D-Engine ADC Optical	2015-10-29 12:48:38	51
D-Engine ADC PSU	2015-10-29 14:49:56	55
Sampler Horizontal Die	2015-10-29 14:35:24	73
Sampler Horizontal PCB	2015-10-29 13:29:37	49
Sampler Vertical Die	2015-10-29 14:54:01	69
Sampler Vertical PCB	2015-10-29 14:41:11	50
RFCU Horizontal Baseplate	2015-10-29 14:46:40	47
RFCU Vertical Baseplate	2015-10-29 14:49:40	47

Table 4.2: Digitiser 004 maximum temperatures logged from Aug 01 2015 to Mar 31 2016.

of the maximum operating temperature for the Digitiser. It can be seen from Table 4.1 and 4.2 that the module temperatures fall below their maximum allowed value of 85 $°C$, with the highest temperature being 73 $°C$ (Sampler Horizontal Die).

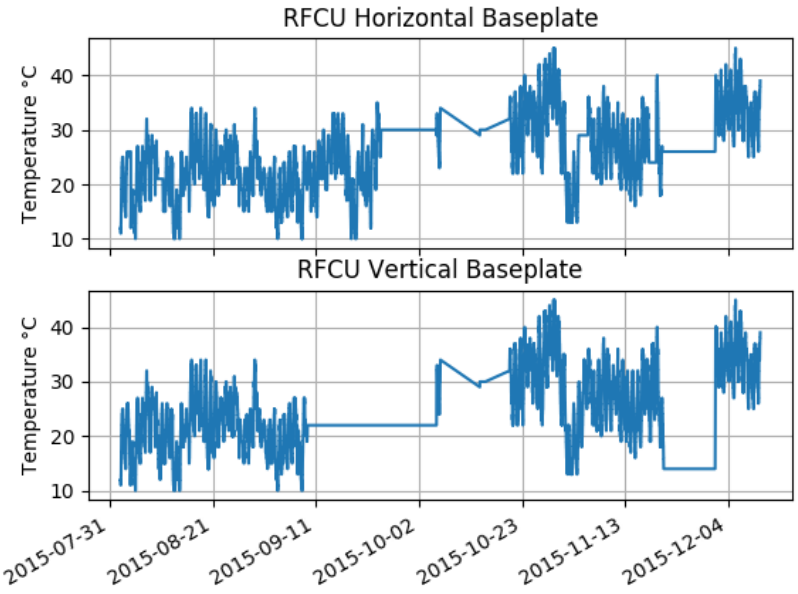


Figure 4.12: RFCU temperature sensor values for Digitiser 003.

Component Description	Date time	T($°C$)
D-Engine FPGA Die	2015-10-29 12:51:25	54
D-Engine FPGA Ambient	2015-10-29 14:39:13	50
D-Engine ADC Optical	2015-10-29 12:48:38	52
D-Engine ADC PSU	2015-10-29 14:49:56	55
Sampler Horizontal Die	2015-10-29 14:35:24	64
Sampler Horizontal PCB	2015-10-29 13:29:37	49
Sampler Vertical Die	2015-10-29 14:54:01	69
Sampler Vertical PCB	2015-10-29 14:41:11	49
RFCU Horizontal Baseplate	2015-10-29 14:46:40	48
RFCU Vertical Baseplate	2015-10-29 14:49:40	49

Table 4.3: Digitiser 005 maximum temperatures logged from Aug 01 2015 to Apr 15 2016.

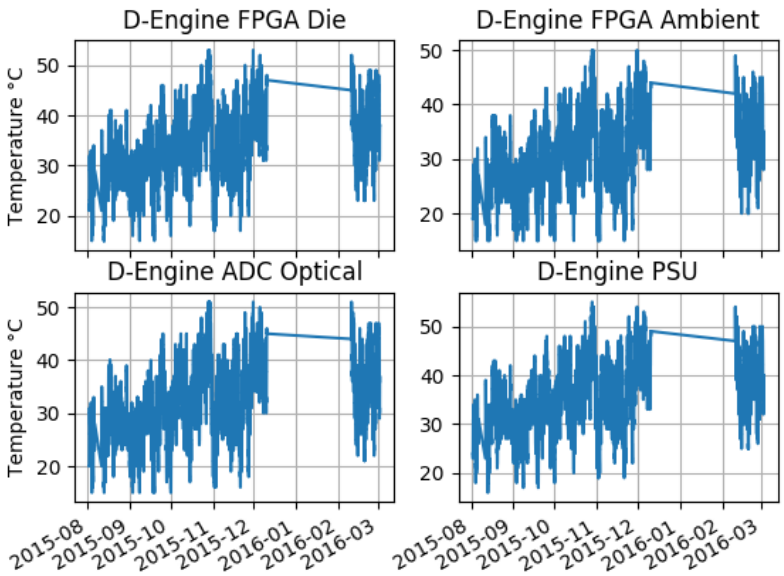


Figure 4.13: D-Engine temperature sensor values for Digitiser 004.

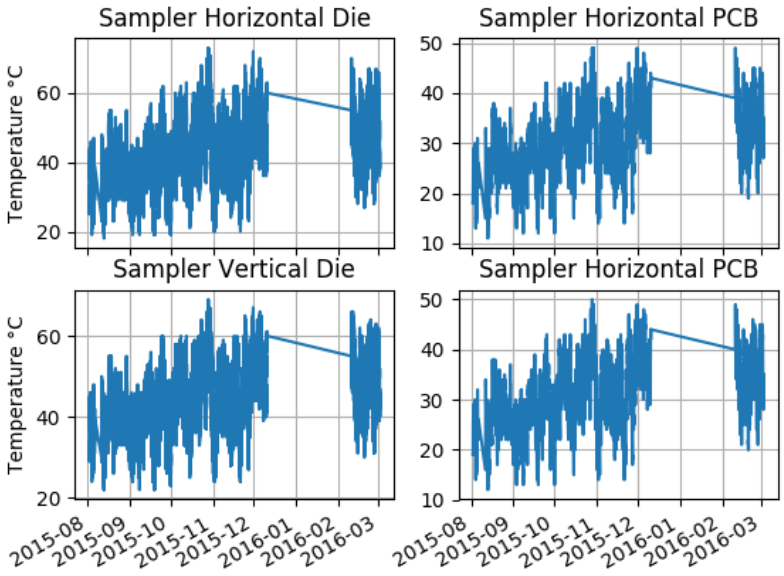


Figure 4.14: Sampler temperature sensor values for Digitiser 004.

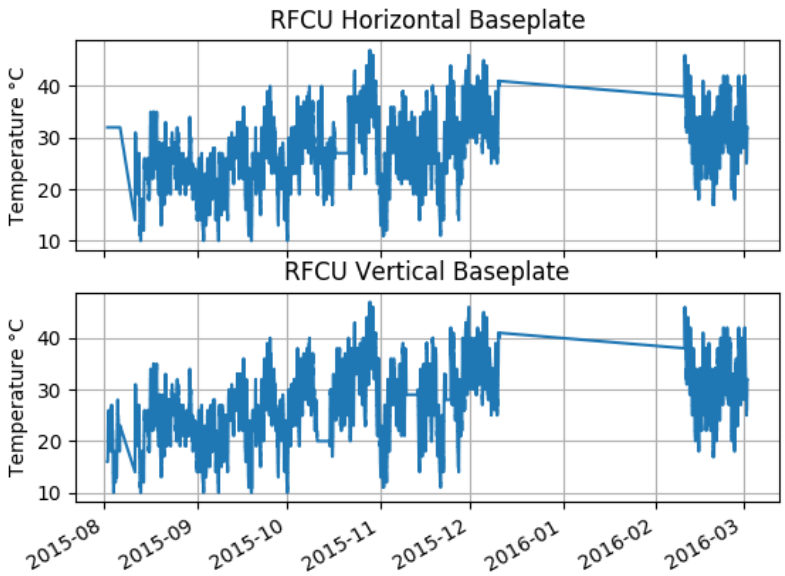


Figure 4.15: RFCU temperature sensor values for Digitiser 004.

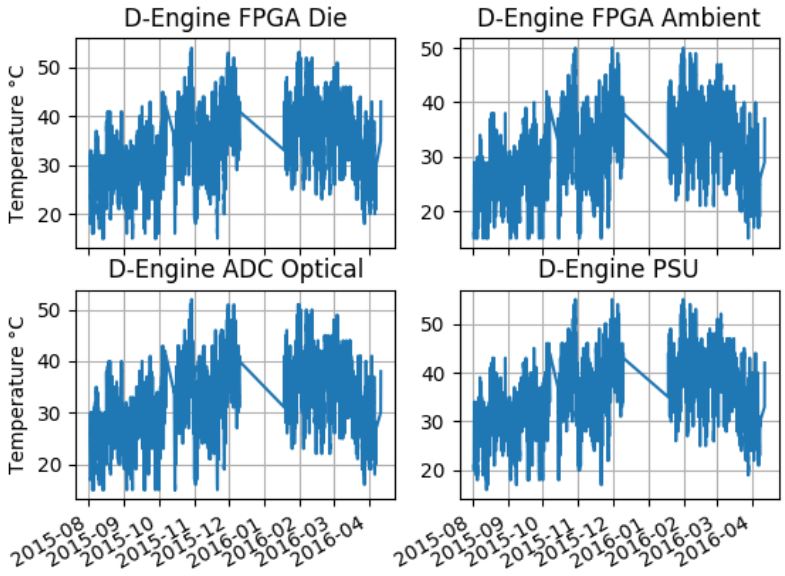


Figure 4.16: D-Engine temperature sensor values for Digitiser 005.

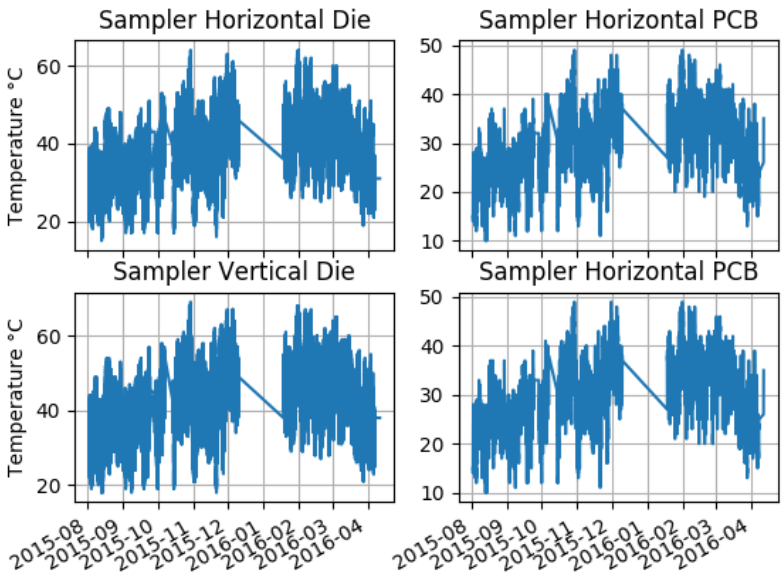


Figure 4.17: Sampler temperature sensor values for Digitiser 005.

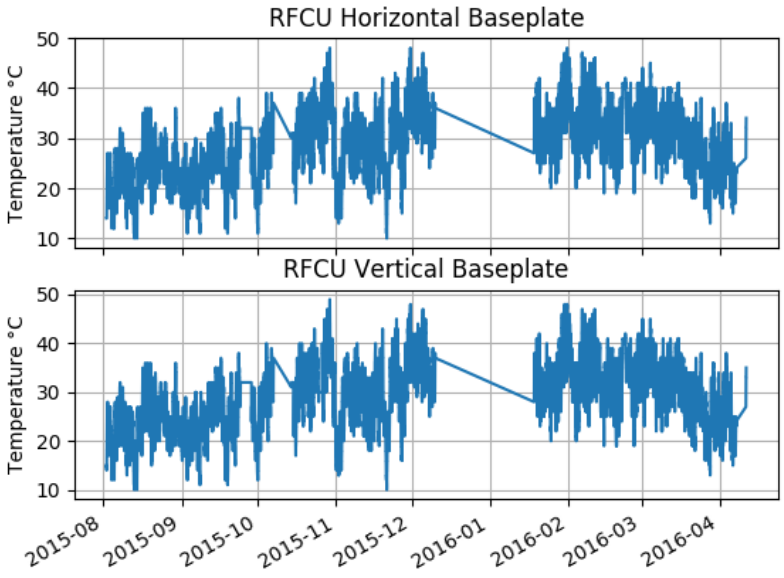


Figure 4.18: RFCU temperature sensor values for Digitiser 005.

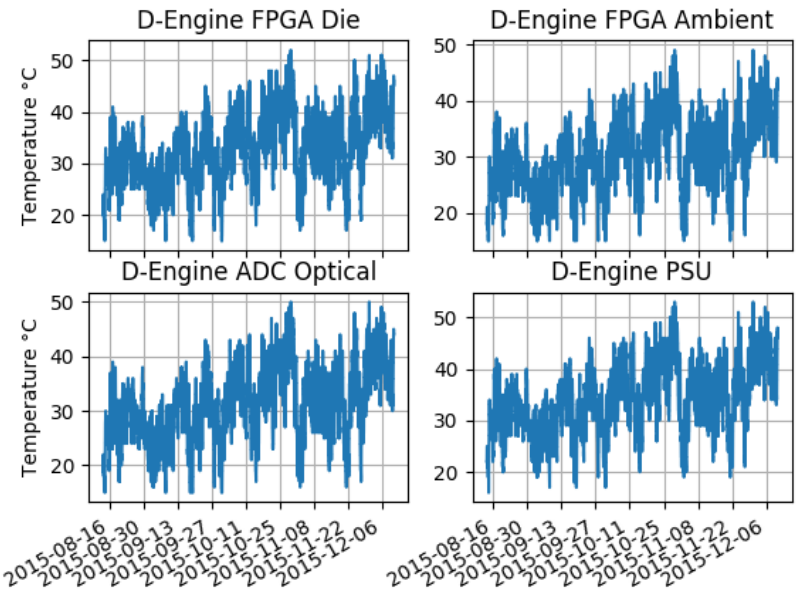


Figure 4.19: D-Engine temperature sensor values for Digitiser 006.

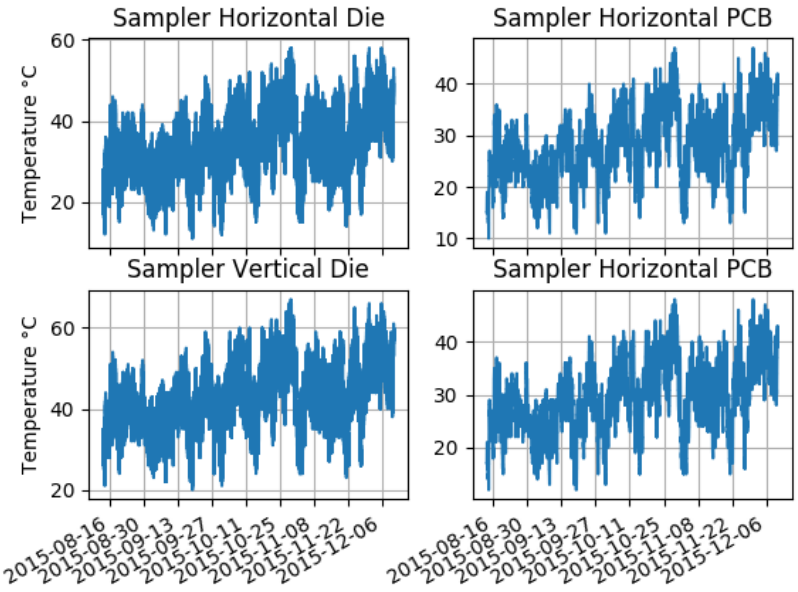


Figure 4.20: Sampler temperature sensor values for Digitiser 006.

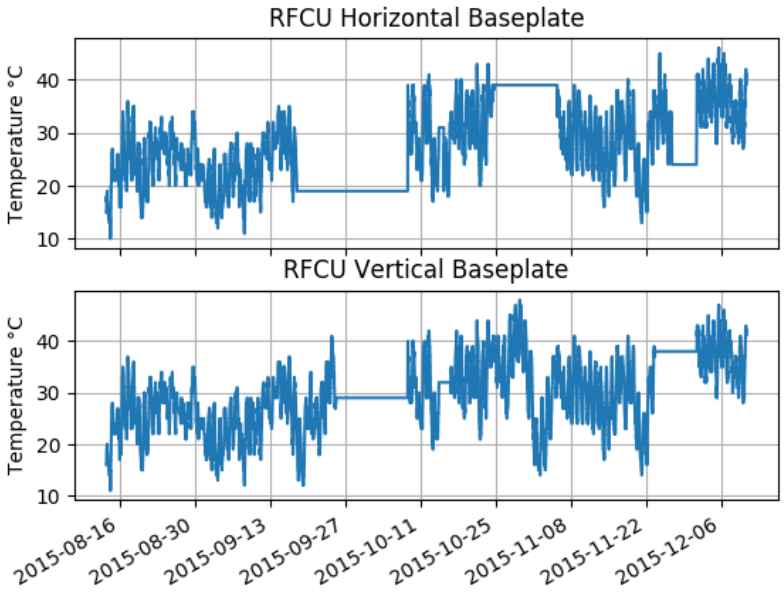


Figure 4.21: RFCU temperature sensor values for Digitiser 006.

Component Description	Date time	T($°C$)
D-Engine FPGA Die	2015-10-29 12:51:25	52
D-Engine FPGA Ambient	2015-10-29 14:39:13	49
D-Engine ADC Optical	2015-10-29 12:48:38	50
D-Engine ADC PSU	2015-10-29 14:49:56	53
Sampler Horizontal Die	2015-10-29 14:35:24	58
Sampler Horizontal PCB	2015-10-29 13:29:37	47
Sampler Vertical Die	2015-10-29 14:54:01	67
Sampler Vertical PCB	2015-10-29 14:41:11	48
RFCU Horizontal Baseplate	2015-10-29 14:46:40	46
RFCU Vertical Baseplate	2015-10-29 14:49:40	48

Table 4.4: Digitiser 006 maximum temperatures logged from Aug 01 2015 to Dec 31 2016.

4.3 Comparison/Validation of results

The temperature values recorded for the Digitiser in the oven test and the data gathered from the prototype on-site Digitisers were compared to those in the simulation value from the previous chapter in Table 4.5. It was noted here that the ADC die temperatures were $9°C$ and $17°C$ higher in the oven and on-site logs, respectively, than the simulation values. Although this was still $20°C$ and $12°C$ below the $85°C$ requirement we wanted to know why there was such a discrepancy in the values. We discovered that the case on the ADC chip was not in contact with the extrude (including the thermal interface material (TIM)) touching down on it due to the tolerances of the chip and extrude height. A thicker TIM was used to solve this problem but since the original design still had met specification, another round of formal oven testing was not performed.

Component Description	On-Site ($°C$)	Oven ($°C$)	Simulation ($°C$)
D-Engine FPGA Die	53	62	62
D-Engine FPGA Ambient	50	56	57
D-Engine ADC Optical	51	58	56
D-Engine ADC PSU	55	61	56
Sampler Horizontal Die	73	65	56
Sampler Horizontal PCB	49	55	56
Sampler Vertical Die	69	65	56
Sampler Vertical PCB	50	53	55
PSU	51	57	57

Table 4.5: Digitiser thermal oven temperatures compared to simulated temperatures including solar radiation from Table 3.9.

4.4 Achievement of goals

The Square Kilometre Array South Africa Digitiser met all of the five objectives specified under test and in the field, namely:

1. The Digitiser was able to operate between a minimum and maximum ambient air temperature of $-10°C$ and $40°C$.

2. The case temperatures of critical electrical components remained below $85°C$ which ensured safe operation of the Digitiser.

3. The Digitiser chassis provided $100dB$ of electromagnetic interference (EMI) shielding.

4. The Digitiser fitted the geometrical envelope of $600mm$ x $400mm$ x $350mm$.

5. The Digitiser weighed less than $40kg$ and was able to be handled by one person.

Chapter 5

Conclusion and Further Work

5.1 A brief summary

In this dissertation we have presented the design of an externally, near-feed mounted, passively cooled Digitiser for the MeerKAT Radio Telescope. This has never been done before. Radio telescopes are conventionally designed to have the signal Digitiser located in the pedestal of the radio telescope antenna structure to shield the incoming radio signal from being contaminated by the electromagnetic interference (EMI)/radio frequency interference (RFI) noise created by the Digitiser electronics. However, if a Digitiser could be placed near the antenna feed, this would decrease the length of the signal path between the receiver and the Digitiser, which would decrease noise on the signal.

We first considered a low-cost commercial-off-the-shelf (COTS) solution to the problem by investigating a ROSE industrial enclosure with an EMI/RFI seal. This enclosure was chosen based on it fitting the geometric dimensional constraints of the Digitiser, its EMI/RFI capabilities and the suitability of this enclosure for outdoor applications. Through calculation and simulation we found that this enclosure would be unsuitable as it did not have a large enough surface area to allow natural convection required to keep the Digitiser electronics within their recommended operating temperatures. It was apparent that a COTS solution would not be feasible and therefore a custom designed enclosure would be needed.

We then considered an enclosure design with the maximum allowable geometric dimensions. Thermal calculations and simulations showed again that, even with these maximum dimensions, the surface area of the enclosure would not be large enough to allow natural convection to keep the Digitiser electronics within recommended operating temperatures. To address this problem, heat-sinks were added to the enclosure - two for the sides for the thermal path of the modules and one on the back for the possible inefficiency of the Power Supply Unit (PSU). This enclosure was evaluated through calculation and simulation and was found to be adequate.

As an externally mounted Digitiser would be exposed to solar radiation, we investigated the need for thermal protection against solar heating. Simple calculations suggested that there would be a significant amount of heat added to the system by solar radiation. A suitable solar shield was designed to create a chimney effect over the side heat-sinks, thereby improving convective cooling.

The internal modules were then designed by creating a generic a clam-shell module and PCB designs through which protrusions from the lids touching down on hot

components would allow heat to flow to the sides of the module and into the sidewalls of the outer enclosure to the heat-sink. Components were placed near the sides of the PCBs to minimise the thermal path and extra copper ground planes were added to PCBs to maximise heat flow through the PCB itself. Once laid out, each individual module was thermally simulated to ensure component temperatures remained below the acceptable maximum of 85°C.

Finally, the entire housing with all its component modules was simulated to ensure all modules behaved correctly by dissipating their heat into the outer enclosure sidewalls. The solar radiation was accounted for by applying its heat load to the solar shield in the simulation. The results from these simulations suggested that the Digitiser design would meet the temperature requirements.

Prototypes were then built and tested in a laboratory thermal chamber. The thermal test profile cycled through a range of temperatures from the minimum to the maximum allowable operating temperatures to observe the behaviour of the Digitiser. Data values were logged and assessed to confirm that the operational component temperatures remained below the maximum allowable limits. The measured temperatures were also compared to the simulated results. The prototypes passed laboratory thermal and RFI tests.

Finally the prototype Digitisers were installed on site as construction work finished on the first pedestals. Temperature data was continuously logged and observed at a number of points in each Digitiser. This data revealed that the Digitiser component temperatures remained below the allowed acceptable maximum of 85°C even on days where the ambient temperature peaked at 40°C.

The goal of this dissertation was to design and successfully build a passively cooled, near feed, externally mounted Digitiser.Through calculation, simulation and iteration this goal was achieved resulting in an operational Digitiser system which is being used on the MeerKAT Radio Telescope and potentially also in SKA Phase 1.

Having successfully designed and built a near feed externally mounted Digitiser it is now possible for other designers to use this existing design as a basis for their work on future radio telescopes. Prior to this work no radio telescope designs have been able to successfully create a near-feed externally mounted Digitiser. The success of the design means that lower signal-to-noise ratio designs should be possible in the future.

5.2 Recommendations for future work

5.2.1 Digitiser mounting interface as a heat path

The idea to use the antenna indexer platform as a large heat sink for the Digitisers mounted to it was discussed early on in the design process. Due to time constraints on a final solution for the interface requirements between the Digitiser and the platform the design team decided to use a blank plate with set dimensions which would be mated to the platform using M8 Bolts and standoffs (allowing an air gap, for heat-sinks relying on natural convection) between the Digitiser base and indexer platform. This solution allowed the team to change the outer dimensions and mating interface of the Digitiser without costly design changes on the indexer platform. If the base of the Digitiser could be mated to the indexer platform it would act as a

heat spreader and heat-sink. This would drive component temperatures down and increase the temperature margin further below the acceptable 85°C maximum. It could also allow the FPGA to use more of its processing power (and hence generate more heat).

5.2.2 Thermal interface materials

The thermal interface material (TIM) used in the Digitiser proved to be one of the most critical elements in effectively dissipating heat. There were many cases of poor compression on the material and mating surfaces which resulted in components operating at very high temperatures. Three kinds of TIM were researched while developing the Digitiser. A liquid type, a putty, and a sponge. We had the best results with the putty as it was both compressible and able to spread into small gaps between mating surfaces without warping of the PCB and components. Its one drawback was the difficulty in cutting it to size and getting it to stay in place while mating all the surfaces together. The liquid variant did not provide enough compression and hence performed poorly even though it had the lowest thermal resistance of the three kinds. Previous experience in other projects suggested that the sponge variant was difficult to get hold of in thin enough sheets which would provide a low enough thermal resistance to be effective. The sponge was also prone to over-compression which warped the PCB and components and resulted in erratic behaviour in the electronics. Further investigation on other types and makes of thermal interface material which could further reduce the thermal resistance between mating surfaces of the module components and heat spreading module lids is recommended.

5.3 Recommendations for practitioners

5.3.1 Geometric dimensioning & tolerancing during manufacture

A recurring problem encountered during the prototyping (and manufacturing) phase of the Digitiser mechanical housing was both the geometric tolerancing provided on drawings and the manufacturers' ability to meet them consistently. Geometric drawings are usually provided with an overall tolerance which manufacturers are required to meet to ensure that all the parts fit together correctly. The Digitiser mechanical design followed the International Organization for Standardization (ISO) tolerancing standard, which should have been sufficient to result in housings that would correctly fit together. During the fabrication of our initial two prototypes the manufacturing company took care with the milling of the various parts and we had favourable results which met thermal and EMI/RFI requirements. Unfortunately the following eight pre-production housings all failed the requirements. I discovered that the manufacturers were not ensuring all dimensions were within the required tolerances - they only measured a few overall dimensions which were often not important. This was also coupled with them often delivering parts which had too much material taken off (see 5.3.2). To combat this I had to comb over all drawings and highlight dimensions of critical importance to ensure the correct fitting together of parts. These dimensions were also given even higher tolerances to be certain that the manufacturer would not take any short cuts. I also went on to inspect and correct

all measuring programs used by the metrology department of the manufacturer to ensure they checked these "critical dimensions".

5.3.2 Chromate conversion coatings and powder coatings

All metal parts were given a chromate conversion coating for two reasons. Firstly it made the aluminium parts more electrically conductive, which meant a more effective "Faraday Cage" around the electronics resulting in fewer EMI/RFI emissions. Secondly it offered more protection against oxidation of the aluminium parts, which would decrease their electrical conductivity. Powder-coating was also applied to the outer enclosure to provide a hardy protective layer for corrosion and rough handling of the Digitiser in operation. I discovered however that, if the application of the chromate conversion coating or powder-coating was not satisfactorily applied by the manufacturer, the parts were dipped in acid to remove the coatings before reapplying them. The acid however also took off enough aluminium to result in part dimensions no longer meeting the required tolerances. These parts were also not re-measured after chromate conversion and powder-coating and hence if they were out of specification the manufacturers would not pick it up.

5.3.3 Thermal interface materials

Thermal interface materials (TIMs) are fairly poor conductors of heat in comparison to metals. They are however far better conductors than air. Our initial focus was to find the TIM with the lowest thermal resistance. The product most recommended was Arctic Silver, a liquid type TIM which was very expensive. Given its high cost we initially used it on the ADC chip as its thermal interface surface was very small and we needed to dissipate a comparatively large amount of heat through this surface. I could never get satisfactory results with it and eventually tried the thermal putty, which was far cheaper and had a far lower thermal conductivity, and was used on other parts of the Digitiser. The temperature of the ADC chip dropped significantly and I realised that compression between mating surfaces was far more important than the thermal conductivity of the TIM.

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