

**ANALYSIS OF
SYMMETRICAL COMPONENTS
OF HARMONICS
FOR THREE PHASE
POWER SYSTEMS**

by **KWAN LEUNG SHUM**

**This thesis presented to the University of Cape Town in
partial fulfillment of the Master of Science Degree
in Electrical and Electronic Engineering**

September 1986

The University of Cape Town has been given
the right to reproduce this thesis in whole
or in part. Copyright is held by the author.

The copyright of this thesis vests in the author. No quotation from it or information derived from it is to be published without full acknowledgement of the source. The thesis is to be used for private study or non-commercial research purposes only.

Published by the University of Cape Town (UCT) in terms of the non-exclusive license granted to UCT by the author.

I dedicate this thesis to
my parents and Teresa
for their Love, Encouragement
and Inspiration.

Kwan L. Shum

C O N T E N T S

	PAGE
Acknowledgement	1
Abstract	2
List of Illustrations	3
List of Tables	5
List of Symbols	6
List of Abbreviations	7
 Chapter One. Introduction.	 8
1-1. An introduction to harmonic distortion.	9
1-2. Causes of harmonics.	9
1-3. Harmonic currents and their effects on system voltages.	10
1-4. The disadvantages of harmonic distortion.	11
1-5. Harmonic elimination.	12
1-6. Measurement of harmonic distortion.	14
1-7. Aim of this thesis.	14
 Chapter Two. Mathematical model of harmonics.	 16
2-1. Symmetrical components analysis.	17
2-2. Symmetrical components of various harmonics.	21
2-2-1. Positive-sequence system.	23
2-2-2. Negative-sequence system.	24
2-2-3. Zero-sequence system.	25
2-3. Relationship between line and phase voltages and currents with harmonics.	26
 Chapter Three. Harmonic monitoring.	 28
3-1. Character of current transformer.	29
3-2. Signal processing techniques.	32
3-2-1. Filtering.	33
3-2-2. Fourier transform.	33
3-2-3. Signal modulation ____ "+1 and -1" technique.	34
3-2-4. Aspects of the different methods.	41
3-3. Interpretation of results.	45

Chapter Four.	Instrumentation.	46
4-1.	Introduction.	47
4-2.	Basic design philosophy.	47
4-2-1.	Part 1 Scaling.	47
4-2-2.	Part 2 Reference clock generator.	51
4-2-3.	Part 3 Sign-bit modulator.	55
4-2-4.	Part 4 Modulating clock generators.	58
4-2-5.	Dual-edge triggered flip-flop (DET FF).	64
4-2-6.	Part 5 Sample-and-hold and analogue-to-digital convertor (ADC).	67
4-2-7.	Part 6 Microprocessor unit.	76
4-2-8.	Part 7 Instrumentation interface.	82
4-2-9.	Part 8 Microcomputer.	88
4-2-10.	Overall operation.	88
4-2-11.	SH-64 bus.	90
4-2-12.	Layout of circuitry.	90
Chapter Five.	Software.	92
5-1.	The procedure of developing an operating system for the instrument.	93
5-2.	The operating system.	94
5-2-1.	Initialization.	97
5-2-2.	The operation of the software.	97
5-3.	Software of the microcomputer.	105
Chapter Six.	Results.	108
6-1.	Testing apparatus.	109
6-2.	Preparation of testing apparatus.	110
6-3.	Procedure of operating the harmonic analyser.	111
6-4.	Results of the tests.	113
6-5.	Conclusion of the tests.	114
Chapter Seven.	Conclusions and recommendations.	117
Bibliography		121
Appendices :		124
A.	Assignment of SH-64 Bus.	A1
B.	Individual circuit diagrams of Card A, B and C.	B1
C.	Program Listing of the Operating System.	C1
D.	Program Listing of the Software of Microcomputer.	D1
E.	The Results of the Tests.	E1

A C K N O W L E D G E M E N T

I express my sincere gratitude to the large number of individuals without whose help this project could not have been accomplished. I am indebted to them for their constructive contribution and verbatim review of the contents of the thesis and in particular to my supervisors, Professor N. Enslin and Mr. K. P. Hoffman for their continued supervision during the course of this work.

Mr. Watson, come here, I want you.

Alexander Graham Bell

A B S T R A C T

Harmonic distortion of three phase power systems is caused by large amounts of electric power consumers using power electronic installations (e.g. drives and rectifiers). It has a number of undesirable consequences and has become an increasingly important problem with the rapid growth and ready availability of the power electronic devices and installations.

A famous mathematical technique called "symmetrical components" was used to model the fundamental components of three phase systems. This method was extended to various harmonics.

The aim of this thesis is to measure both the magnitudes and phase angles of various harmonics which exist in three phase power systems, and to express them in symmetrical components.

A digital electronics and microprocessor-based instrument was designed and constructed using the novel signal modulation technique called "+1 and -1" which was developed by the author of this thesis. This instrument was employed to achieve the above objectives.

LIST OF ILLUSTRATIONS

PAGE

Chapter Two :

2.1	Definition of phase voltage and current in 3-phase circuit.	18
2.2	Real system and corresponding symmetrical components.	19

Chapter Three :

3.1	Simplified equivalent circuit of CT.	31
3.2	Magnetization curve of CT.	31
3.3	Typical frequency response of CT.	31
3.4	Relationship between X_k , Y_k and θ_k .	42
3.5	X_k - Y_k - θ_k curves of fundamental and 3rd harmonic.	43

Chapter Four :

4.1	Basic layout of the overall system.	48
4.2	Voltage scaling circuit.	50
4.3	Current scaling circuit.	50
4.4	Multiplexer.	52
4.5	Phase-shift compensator and low-pass filter.	54
4.6	Reference clock generator.	55
4.7	Sign-bit modulator.	57
4.8	Equivalent circuit of sign-bit modulator.	57
4.9	Actual sign-bit modulator circuit.	59
4.10	Controlling circuit and timing diagram of counter 1 of 8254, programmable interval timer.	62
4.11	Digital phase shifter (set to 90 deg.) .	63
4.12	Modulating clock generator.	65
4.13	Dual-edge triggered flip-flop (DET-FF).	66
4.14	Analogue-to digital convertor system.	69
4.15	Timing diagram of ADC.	70
4.16	Controlling circuit of sample-and-hold device and its timing diagram.	72
4.17	Circuit diagram of signal \overline{ADCL} , \overline{ADCH} , \overline{S} and their timing diagram.	74
4.18	Rectifier circuit.	75
4.19	New chip select (\overline{NCS}) circuit of non-memory peripherals and its timing diagram.	78
4.20	New chip select circuit of EPROM and its timing diagram.	80
4.21	New chip select circuit of RAM and its timing diagram.	81
4.22	Circuit secures New chip select signals.	83
4.23	E signal circuit.	85
4.24	R/\overline{W} signal circuit.	85

4.25	Circuitry of triple wait-state generator.	86
4.26	timing and state diagrams of triple wait-state generator.	87

Chapter Five :

5.1	Flowchart of the operating system.	95
5.2	Order of execution of procedures of operating system.	96
5.3	Flowchart of Program "H7" .	106

Chapter Six :

6.1	Interface between the analyser and the supply.	112
-----	--	-----

L I S T O F T A B L E S

	PAGE
Chapter Two :	
2-1. Sequence of harmonics in three-phase systems.	26
Chapter Four :	
4-1. Address of each <u>new chip select</u> .	79

L I S T O F S Y M B O L S

This list does not include all symbols used, since all symbols were already clearly defined in the thesis. Instead this list displays the symbols which may create confusion.

$\bar{U}_0, \bar{U}_+, \bar{U}_-$	Zero, positive and negative sequence components
$\bar{V}_0, \bar{V}_+, \bar{V}_-$	Sequence components of Voltages
$\bar{I}_0, \bar{I}_+, \bar{I}_-$	Sequence components of Currents
$U_{a0}(t), U_{b0}(t), U_{c0}(t)$	Instantaneous zero sequence components
$U_{a1}(t), U_{b1}(t), U_{c1}(t)$	Instantaneous positive sequence components
$U_{a2}(t), U_{b2}(t), U_{c2}(t)$	Instantaneous negative sequence components
\hat{U}_k	Peak amplitude
\bar{U}_k	Mean level of output
${}_0\bar{U}_k$	Mean level of output modulated at 0 deg. phase shift clock
${}_{90}\bar{U}_k$	Mean level of output modulated at 90 deg. phase shift clock
k	Order of harmonic
$\theta, \varnothing, \alpha, \beta$	Angles
H_n	Rms value of amplitude of nth harmonic

L I S T O F A B B R E V I A T I O N

ADC	Analogue-to-digital Convertor
CT	Current Transformer
DET	Dual Edge Triggered
FF	Flip Flop
FFT	Fast Fourier Transform
IIR	Impulse Response Filter
PLL	Phase Lock Loop
ZC	Fundamental Filtered Zero-crossing

CHAPTER ONE

" Where shall I begin, please your Majesty ? " he asked. Begin at the beginning, the King said, gravely, " and go on till you come to the end: then stop. "

Alice's Adventures in Wonderland,

Lewis Carroll

The last thing one knows in constructing a work is what to put first.

Blaise Pascal

1 Introduction

1-1. An introduction to harmonic distortion .

The aim of an electric power system is to provide a supply of electricity to large numbers of consumers. Ideally this electricity is supplied as a perfectly sinusoidal voltage of constant amplitude and frequency. In practice the operation of the supply system and the use made of the supply by the consumers causes various deviations from the ideal. One form of deviation is distortion of the waveform. This problem has become increasingly important with the ready availability of power electronic devices.

1-2. Causes of harmonics.

If a power system is to supply a good sinusoidal voltage the generators themselves must generate a sinusoidal waveform. Starting at the generator terminals the first components to affect the waveform are the transformers. Partial saturation of the iron causes the magnetising current to differ significantly from a sine wave, which is to say that it contains harmonic components [1]. The contribution of harmonics of the magnetising current to the distortion of the supply voltage depends on the source impedance of the supply and the magnitude of the harmonic currents.

Larger amounts of harmonic distortion are more usually caused by various types of rectifying load. For a rectifier of a given size, the harmonic currents are affected by the pulse number and the possible application of phase angle control [2]. Loads containing saturated iron cores also draw distorted current. Significant amounts of harmonic distortion may arise, not only from large installations, but also from the combined effect of a large number of small installations. The manufacturers of household appliances should adopt power supply circuits that do not cause large switch-on transients, for examples as in TV receivers, heaters and boilers [3]. These transients are equivalent to injecting a substantial amount of harmonic currents into the supply as well as in some cases direct currents.

1-3. Harmonic currents and their effects on system voltages.

The harmonic voltage distortion can be found as the product of the harmonic current and the impedance at that frequency of the component or components through which it flows. The harmonic voltage distortion is liable to reach unusually high values when the harmonic current encounters a parallel or series resonant circuit [4]. Since a parallel combination of inductance and capacitance presents a high impedance to current, the harmonic voltage distortion will be increased. A series resonant circuit provides a low impedance path for currents which will in turn cause increased voltage distortion across the inductive and capacitive branches. An electricity distribution network

contains inductive components, usually in the form of the leakage reactance of transformers. Capacitors are often connected for power factor correction and in cable networks, the cable capacitance can also form part of a tuned circuit.

The maximum voltage distortion on a power system does not necessarily occur at the point of connection of the distorting load. Magnification may very well be caused at relatively remote points on the network and this must always be kept in mind when connecting distorting loads.

1-4. The disadvantages of harmonic distortion.

Harmonic distortion has a number of undesirable consequences. Harmonic distortion increases the current carried by capacitors connected to the system, particularly when they unexpectedly form part of a resonant circuit. Such current may operate a protective device causing the capacitor to be disconnected, or may, over a period, reduce the life of the capacitor [4].

The most serious effect upon a.c. machines of system harmonics is an increase in machine losses [5, 6, 7]. The major component of extra loss occurs in the rotor. Harmonic voltage distortion has little effect upon the torque or power developed by a machine but can give rise to torque pulsations which could be significant [6, 7].

Some electronic equipment uses the supply voltage waveform directly to control the switching instant of thyristors and similar components. Distortion of the voltage wave can adversely affect

the performance of such devices, particularly when the distortion is severe, and the voltage may cross the zero line or some other level more than twice per cycle [2]. Since the ear is most sensitive to sounds having frequencies around 1 KHz, the introduction of voltages of this frequency into a telephone system will lead to a disturbing hum [2]. Such disturbances can occur when telephone lines run parallel with power lines carrying distorted currents with appreciable high frequency components [2]. Distorted currents will also increase the losses in the supply system both because a given power supply requires a larger r.m.s. current and as a result of additional skin effect losses [2].

1-5. Harmonic elimination.

Most of the information on harmonic control relates to the three-phase a.c.- d.c. or a.c.- a.c. power convertor. There are in general two accepted ways in which the harmonics developed by the convertor can be controlled. The first method is to increase the pulse number of the convertor and the second is to install harmonic filters [2]. In the first case the orders of the characteristic harmonic for a waveform with pulse number p are $pq \pm 1$, where q is an integer. Therefore, the higher the pulse number, the higher the frequency of the lowest order harmonic produced. Moreover as the harmonic order increases, its amplitude decreases. On the other hand, harmonic filters connected to a.c. system generally have two functions, i.e. to

reduce harmonic voltage and current below the permitted levels and also the to provide of some of the reactive power absorption. There have been several attempts to achieve harmonic control by other means. Three of these are:

1. Magnetic flux compensation for power transformers.

A current transformer is use to detect the harmonic components coming from the non-linear load and these are fed through an an amplifier into the tertiary winding of a transformer in such a manner as to cause cancellation of the harmonic current concerned [8].

2. Harmonic re-injection for low pulse-number convertors to emulate the qualities of higher pulse-number convertors.

The d.c. ripple output of 6-pulse convertor and the output of its feedback convertor can be combine together to produce a 12-pulse waveform on the d.c. side [9] .

3. Multi-layer cables are composed of different materials with higher values of resistance on the outside layers.

This is to eliminate the higher harmonics which propagate along the outside layers due to the skin-effect for d.c. transmission lines. This method was utilized in the d.c. transmission lines between coal enriched Siberia and the industrially dense European part of USSR [10] .

All the methods mentioned above are generally complicated and expensive, to implement practically.

1-6. Measurement of Harmonic Distortion.

For many years the standard method of measuring harmonic distortion was to select the appropriate frequency component from the distorted wave by means of a tuned circuit. Another approach is to use the sampling circuits to store the instantaneous values of the waveform at successive instants during the cycle and to compute a Fourier analysis on-line. Signal modulation technique is also one of the alternative way, which separates the various frequencies components of the signal by means of modulating them with a special modulating waveform.

1-7. Aim of this thesis.

The principle objective of this project is to design and construct an instrument capable of measuring both magnitude and phase of harmonic power flow. The method adapted in this thesis is the signal modulation technique.

There are six main areas which need close examination with reference to harmonic monitoring techniques of this project. Primarily, the electronic components used in building the instrument must be highly precise, e.g. the input scaling circuits must employ very low offset type operational amplifiers and the analogue-to-digital convertor must be stable and should have high resolution quality. Secondly, the meters connected to the harmonic generators, which are used to calibrate the readings of the instrument, must be very accurate. It will be perfect for testing accuracy if electronic programm-

able harmonic generators are employed instead of the traditional synchronous rotating generators. The electronic generators consist of high resolution and precise digital-to-analog convertors. The shapes, amplitudes and angles of their output waveforms can also be programmed. Since the output waveforms, amplitudes and angles are known and are highly stable, it is not necessary to rely on analogue meters and oscilloscopes, etc. Analogue meters often generate inaccurate readings. Thirdly, the frequency response and accuracy of the current transformers is important. Large input current signals will have to be stepped down, so that their amplitudes are compatible with the electronic equipment. Fourthly, the type of analytic technique must be considered to give maximum accuracy and potential of real-time speed of measurement. Fifthly, the instrument must be designed to have the capability of communication with other instruments or controllers. Finally, the results must be interpreted correctly by the equipment and presented in a meaningful manner.

CHAPTER TWO

For every problem there is one solution which is simple, neat and wrong.

H. L. Mencken.

2 Mathematical Model of Harmonics

2-1. Symmetrical Components Analysis.

The electrical power system normally operates in a balanced 3 - phase sinusoidal steady state mode. However, there are certain situations which can cause unbalanced operation. The most severe of these is a short circuit or fault. Less severe conditions are the presence of large amount of single phase loads and their unequal distribution. A long untransposed transmission lines inherently also causes unbalance [11, 12].

Arbitrarily unbalanced three phase voltages or currents can be transformed into 3 sets of balanced 3-phase components or symmetrical components [13]. We can transform an arbitrarily unbalanced condition into symmetrical components, compute the system response by straight- forward circuit analysis on simple circuit models, and transform the results back into the original phase variables.

In a general 3-phase circuit, we must deal with a minimum of three voltages and three currents. The specific definitions are shown in Fig. 2.1 . Each voltage and current is considered as being a sinusoidal steady state waveform and therefore may be expressed using phasor notation as shown in Fig. 2.2 [14].

Modern technique in the calculation of system unbalanced conditions demands a knowledge of the theory of symmetrical components and the phase sequence characteristics of the individual parts of the system.

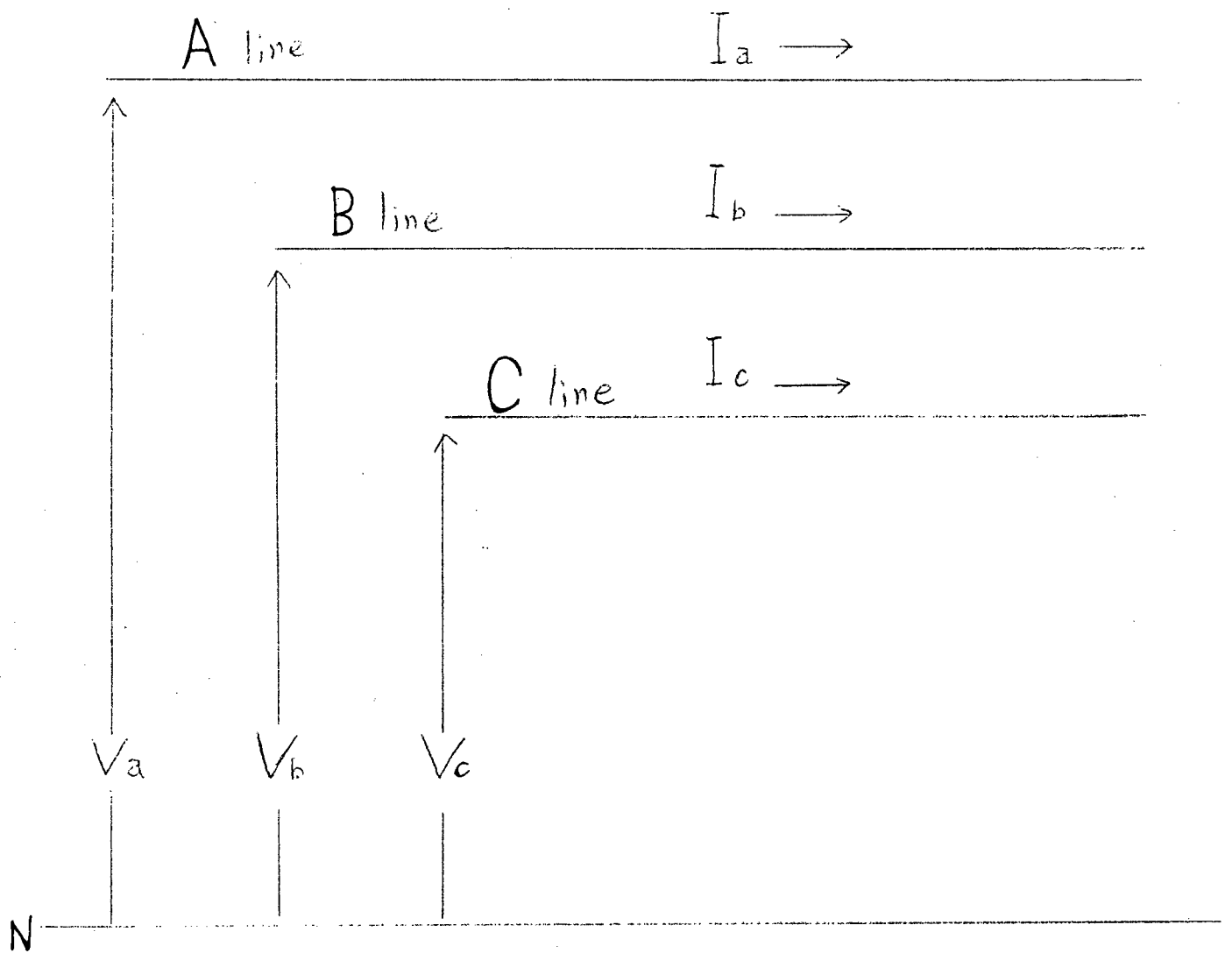
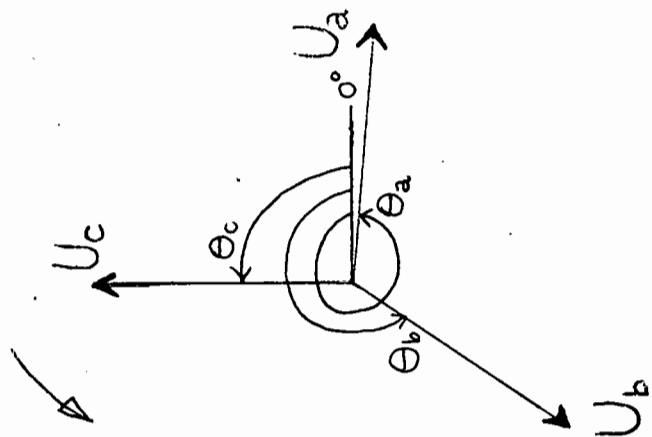
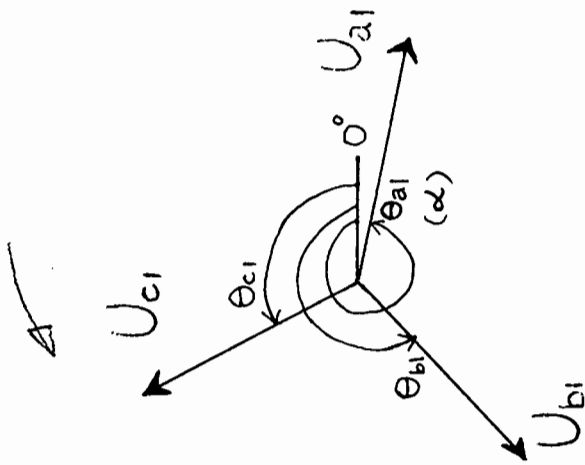


Fig. 2.1 Definition of phase voltage and currents in 3-phase circuit.



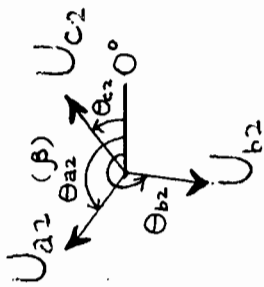
Real system

(a)



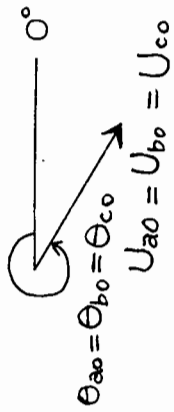
+ve seq.

(b)



-ve seq.

(c)



zero seq.

(d)

Fig. 2.2 Real system and corresponding symmetrical components.

It is possible to analyse any given system of three-phase unbalanced phasors into three other balanced phasor systems which are called positive, negative and zero phase sequence phasors respectively.

The positive phase sequence system is that in which the phase (or line) voltages and or currents reach their maxima in the same order as do those of the normal supply.

It is conventionally assumed that all phasors rotate in a counter-clockwise direction, and the positive phase sequence system is that in which the phase maxima occur in the order ABC [15].

Conversely, the negative phase sequence system is that in which the phasors, while rotating in the same direction as the positive phase sequence phasors, namely, counter-clockwise, reach their maxima in the order ACB [15].

The zero phase sequence system is a single-phase phasor, and it represents the residual voltage or current which is present in three-phase circuit under fault conditions when a fourth wire is present either as a direct metallic connection or as a double earth on the system [15].

The positive phase sequence systems of voltages and currents are those which correspond to the normal load conditions [16].

The negative phase sequence systems of voltages and currents are those which set up in the circuit by the fault, and their magnitudes are a direct measure of the superposed fault conditions between phases. The individual voltages and currents of this system are confined to the three lines [16].

The zero phase sequence systems of voltages and currents are set up in the circuit by the fault, and their magnitudes are a direct measure of the superposed fault conditions to earth . The voltages and currents of this system embrace the fourth wire (or ground) in addition to the three line wires [16]. The fundamental frequency positive- and negative- sequence impedance of machines rotating close to synchronous speed differ considerably. This is due to the fact that the stator developed rotating flux field set up by the positive-sequence voltages component is largely magnetizing, only small currents are induced in the rotor. However, negative-sequence currents of double frequency are induced in the rotor and the impedance is determined largely by the leakage fluxes of the stator and rotor [17].

As has been stated above, the method is applicable for quantities which may be represented by sinusoidal voltages and currents. For problems in which higher harmonics play an important part the method is also applicable.

2-2. Symmetrical components of various harmonics.

A distorted current or voltage waveform can be represented by the well-known Fourier series which is the sum of a fundamental and a series of harmonic components. For this to be valid, the distorted waveform has to have the same wave shape for an indefinite number of cycles or persist for a reasonable length of time.

Distorted waves of a periodic nature can be resolved into a Fourier series consisting of a fundamental and higher harmonics.

The result can be expressed in the general form

$$u(t) = \sqrt{2} [H_1 \cos (wt + \phi_1) + H_2 \cos 2(wt + \phi_2) + H_3 \cos 3(wt + \phi_3) + \dots] \quad (2.1)$$

in which H_1, H_2, \dots , represent the r.m.s. values of amplitude and $\phi_1, \phi_2, \phi_3, \dots$ represent the phase angle of the respective harmonics. This relation can also be expressed in exponential terms as :

$$\begin{aligned} u(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(wt + \phi_n) = \\ &= \operatorname{Re} \sqrt{2} [H_1 \exp j (wt + \phi_1) + H_2 \exp j2(wt + \phi_2) + H_3 \exp j3(wt + \phi_3) + \dots] \end{aligned} \quad (2.2)$$

The phase relationship between the fundamental and the harmonic components is always important. When several different sources combine together, the phase angle of the harmonic components may differ considerably and the resulting distortion may be emphasised or reduced.

The advantage of this method of representing a distorted wave as being made up of a fundamental and a series of harmonics is that, in a linear system each harmonic component may be considered separately, and the final distortion may be found by superposition of the various components.

2-2-1. Positive- sequence System .

Considering first the symmetrical system of three- phase currents or voltages U_{a1} , U_{b1} and U_{c1} in Fig. 2.2 . Being balanced, U_{a1} , U_{b1} and U_{c1} have equal amplitudes , are displaced 120 deg. relative to each other other , and

$$\begin{aligned} U_{a1}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \alpha_n) \exp jn(0) \\ &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \alpha_1) + H_2 \exp j2(\omega t + \alpha_2) \\ &\quad + H_3 \exp j3(\omega t + \alpha_3) + \dots] \quad (2.3.a) \end{aligned}$$

$$\begin{aligned} U_{b1}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \alpha_n) \exp jn(4\pi/3) \\ &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \alpha_1 + 4\pi/3) + H_2 \exp j2(\omega t + \alpha_2 + 4\pi/3) \\ &\quad + H_3 \exp j3(\omega t + \alpha_3 + 4\pi/3) + \dots] \quad (2.3.b) \end{aligned}$$

$$\begin{aligned} U_{c1}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \alpha_n) \exp jn(2\pi/3) \\ &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \alpha_1 + 2\pi/3) + H_2 \exp j2(\omega t + \alpha_2 + 2\pi/3) \\ &\quad + H_3 \exp j3(\omega t + \alpha_3 + 2\pi/3) + \dots] \quad (2.3.c) \end{aligned}$$

or, by substituting $a = \exp j(2\pi/3)$ and $a^2 = \exp j(4\pi/3)$

$$\begin{aligned} U_{a1}(t) &= \operatorname{Re} \sqrt{2} [\\ &\quad H_1 \exp j(\omega t + \alpha_1) + H_2 \exp j2(\omega t + \alpha_2) + H_3 \exp j3(\omega t + \alpha_3) \\ &\quad + \dots] \quad (2.4.a) \end{aligned}$$

$$\begin{aligned} U_{b1}(t) &= \operatorname{Re} \sqrt{2} [\\ &\quad a^2 H_1 \exp j(\omega t + \alpha_1) + a H_2 \exp j2(\omega t + \alpha_2) + H_3 \exp j3(\omega t + \alpha_3) \\ &\quad + \dots] \quad (2.4.b) \end{aligned}$$

$$\begin{aligned} U_{c1}(t) &= \operatorname{Re} \sqrt{2} [\\ &\quad a H_1 \exp j(\omega t + \alpha_1) + a^2 H_2 \exp j2(\omega t + \alpha_2) + H_3 \exp j3(\omega t + \alpha_3) \\ &\quad + \dots] \quad (2.4.c) \end{aligned}$$

Thus it will be seen that the fundamental terms (H1) possess a positive-sequence (as do the fourth and seventh, etc. harmonics), the second harmonic terms (H2) possess a negative-sequence (also fifth and eleventh, etc.) and the third harmonic terms (H3) possess a zero-sequence (also all multiples of three). These results are summarized in Table 2-1.

2-2-2. Negative-sequence System.

Likewise, consider system of three phase currents or voltages U_{a2} , U_{b2} and U_{c2} in Fig. 2.2 .

$$\begin{aligned}
 U_{a2}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \beta_n) \exp jn(0) \\
 &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \beta_1) + H_2 \exp j2(\omega t + \beta_2) \\
 &\quad + H_3 \exp j3(\omega t + \beta_3) + \dots] \quad (2.5.a)
 \end{aligned}$$

$$\begin{aligned}
 U_{b2}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \beta_n) \exp j(2\pi/3) \\
 &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \beta_1 + 2\pi/3) + H_2 \exp j2(\omega t + \beta_2 + 2\pi/3) \\
 &\quad + H_3 \exp j3(\omega t + \beta_3 + 2\pi/3) + \dots] \quad (2.5.b)
 \end{aligned}$$

$$\begin{aligned}
 U_{c2}(t) &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} H_n \exp jn(\omega t + \beta_n) \exp j(4\pi/3) \\
 &= \operatorname{Re} \sqrt{2} [H_1 \exp j(\omega t + \beta_1 + 4\pi/3) + H_2 \exp j2(\omega t + \beta_2 + 4\pi/3) \\
 &\quad + H_3 \exp j3(\omega t + \beta_3 + 4\pi/3) + \dots] \quad (2.5.c)
 \end{aligned}$$

or, again by substituting $a = \exp j(2\pi/3)$ and $a^2 = \exp j(4\pi/3)$

$$U_{a2}(t) = \operatorname{Re} \sqrt{2} [$$

$$H_1 \exp j(\omega t + \beta_1) + H_2 \exp j2(\omega t + \beta_2) + H_3 \exp j3(\omega t + \beta_3) + \dots] \quad (2.6.a)$$

$$U_{b2}(t) = \operatorname{Re} \sqrt{2} [$$

$$a H_1 \exp j(\omega t + \beta_1) + a^2 H_2 \exp j2(\omega t + \beta_2) + H_3 \exp j3(\omega t + \beta_3) + \dots] \quad (2.6.b)$$

$$U_{c2}(t) = \operatorname{Re} \sqrt{2} [$$

$$a^2 H_1 \exp j(\omega t + \beta_1) + a H_2 \exp j2(\omega t + \beta_2) + H_3 \exp j3(\omega t + \beta_3) + \dots] \quad (2.6.c)$$

The fundamental terms (H_1) have a negative-sequence (as do the fourth and seventh, etc. harmonics), the second harmonic terms (H_2) have a positive-sequence (also fifth and eighth, etc.) and the third harmonic terms (H_3) have a zero-sequence (also all multiples of three). These results are also summarized in Table 2-1.

2-2-3. Zero-sequence System.

If a purely zero-sequence system is considered with phasor diagram as shown in Fig. 2.2.d. $U_{a0}(t)$, $U_{b0}(t)$ and $U_{c0}(t)$ are equal in magnitude and in phase so that the fundamental and all the harmonic terms (H_n) are of zero-sequence.

Harmonic [Hn]	Sequence		
	Positive [Ua1,Ub1,Uc1]	Negative [Ua2,Ub2,Uc2]	Zero [Ua0,Ub0,Uc0]
H1	+ve	-ve	0
H2	-ve	+ve	0
H3	0	0	0
H4	+ve	-ve	0
H5	-ve	+ve	0
H6	0	0	0
H7	+ve	-ve	0
H8	-ve	+ve	0
H9	0	0	0
**			
**			
**			
**			
**			
**			
**			
**			
**			

TABLE 2-1. SEQUENCE OF HARMONICS IN THREE-PHASE SYSTEMS

2-3. Relationship between line and phase voltages and currents with harmonics.

When substantial harmonics are present the $\sqrt{3}$ relation between line and phase quantities (i.e. $V_{line} = \sqrt{3} V_{phase}$) of the star-connection of a 3-phase system no longer holds. Harmonic voltages in successive phases are $\pm 2\pi n/3$ out of phase with each other and the resulting line voltage becomes

$$V_{ab}(t) = V_a(t) - V_b(t)$$

$$\begin{aligned}
 &= \operatorname{Re} \sqrt{2} \sum_{n=1}^{\infty} V_n [\exp jn(\omega t + \phi_n) - \exp jn(\omega t + \phi_n + 4\pi/3)] \\
 &= \sqrt{2} \sum_{n=1}^{\infty} V_n [\cos n(\omega t + \phi_n) - \cos n(\omega t + \phi_n + 4\pi/3)] \\
 &= -\sqrt{2} \sum_{n=1}^{\infty} V_n [2 \sin n(\omega t + \phi_n + 2\pi/3) \sin n(2\pi/3)]
 \end{aligned}$$

When $n = 3, 6, 9$, etc. V_{ab} becomes zero, i.e. no triple harmonics exist in the line voltages. Similarly, for the delta-connected three phase system, a complete path for the triple harmonic currents is formed. These currents flow in phase around the loop and the relation of $I_{\text{line}} = \sqrt{3} I_{\text{phase}}$ also no longer holds.

When analysing the penetration of harmonics into a power network it is usual to assume that the effective inductive reactance for the n th harmonic is n times the fundamental value ($Z_L = j n \omega_f L$) and the capacitive reactance is $1/n$ times ($Z_C = 1/j n \omega_f C$) [14].

CHAPTER THREE

There is a Turkish proverb to the effect that 'the world belongs to the dissatisfied.'

I believed in this saying absolutely.

For me the one great underlying principle of all human progress is that 'divine discontent' makes men strive for better conditions and improved methods.

Charles P. Steinmetz

3 HARMONIC MONITORING

There are three areas which need close examination with reference to harmonic monitoring. These are the current transformer, signal processing equipment and interpretation of results.

3-1. Character of Current Transformer.

The simplified equivalent circuit of current transformer is shown in Fig. 3.1. [18].

Defining

L_2 = Leakage reactance referred to secondary

L_e = Magnetising reactance referred to secondary

L_l = Terminating reactance of secondary

C_w = Reactance due to wire capacitance referred to secondary .

For low frequencies, the effect of wire capacitance (C_w) can be neglected and therefore

$$I_2' = (N1/N2) I_1 \quad (3.1)$$

$$I_e = E_2 / \omega L_e \quad (3.2)$$

$$I_2 = I_2' - I_e \quad (3.3)$$

$$E_2 = \omega I_2 (L_2 + L_l) \quad (3.4)$$

Substituting equations (3.1) and (3.3) into equation (3.4) :

$$E_2 = \omega (L_2 + L_l) [(N1/N2) I_1 - I_e] \quad (3.5)$$

To predict I_2 for a given I_1 with known termination (L_l),

equation (3.5) has two unknowns (E_2 and I_e) . The

second relation between E_2 and I_e is the magnetization curve

(E_2 versus I_e : Fig. 3.2) . If equation (3.5) is plotted

on the same coordinates as the magnetization curve (Fig.3.2), the intersection of the two plots will represent a solution for E_2 and I_e . Knowing I_e , now I_2 can be solved. The

error of CT is the deviation of I_2 from I_2' as expressed as a percentage of I_2' .

$$\text{CT error} = (I_2' - I_2) / I_2' = I_e / I_2'$$

CT error increases with increasing CT current and is further increased by high terminating impedance. The optimum termination of CT would be a perfect short circuit. Even at short circuit the CT error is not zero, due to the internal leakage reactance of the CT.

The typical frequency response of a CT is plot of the magnitude of the current ratio, that is, $| \text{Output current} | / | \text{Input current} | = |G(j\omega_e)|$, as a function of radian frequency ω_e , that is, as the frequency of forcing function ω_e change for a fixed load.

[19]. The magnitude of the force function is maintained constant during the process of taking data for the $|G(j\omega_e)|$ versus ω_e plot (Fig. 3.3).

When a current transformer operating at 50 or 60 Hz carries very low current, the absolute error increases because the magnetising current becomes more significant. The better the CT quality, the smaller is the effect. As frequency increases, magnetising reactance increases and magnetising current decreases (see equation 3.2), so that for small current a CT produces a higher output of current at high frequencies than at low frequencies. Errors due to core losses and secondary leakage inductance and winding capacitance are only significant at frequencies

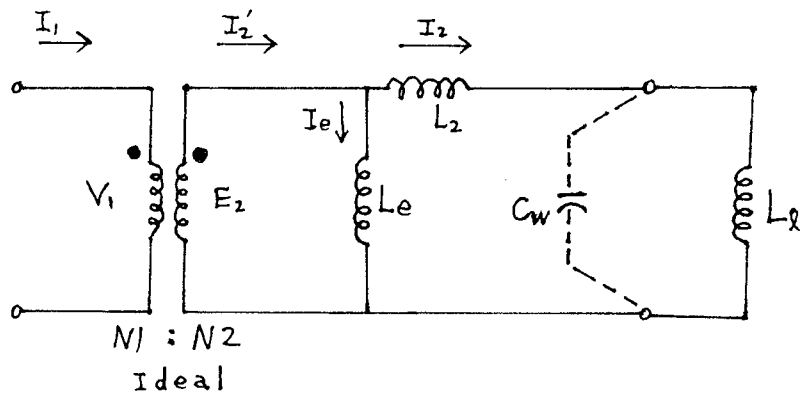


Fig. 3.1 Simplified Equivalent Circuit of CT.

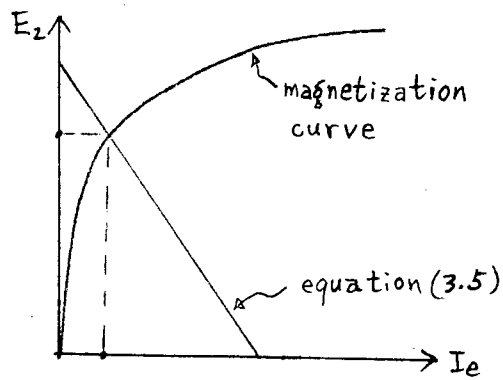


Fig. 3.2 Magnetization Curve of CT

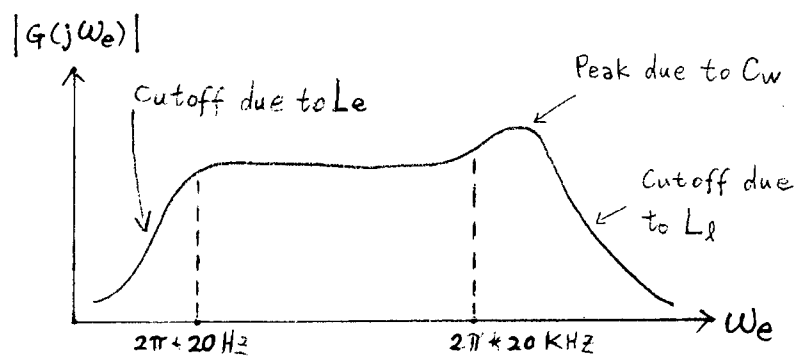


Fig. 3.3 Typical Frequency Response of CT

of above 20 KHz generally. Below 20 KHz commercially available CTs are reported [20] to be adequate for harmonics monitoring . However, the following precautions should be taken :

- 1) The CT burden should be very low impedance , to reduce the required CT voltage and , consequently , the magnetising current .
- 2) It is recommended that twisted- pair or coaxial leads from the CT to the test equipment as short as possible to minimize unwanted pickup .
- 3) If the CT is a multi- winding type, use the highest ratios of secondary/primary . Higher ratios require lower magnetising current and tend to be more accurate .

3-2. Signal processing techniques.

There are, basically, three different approaches to analysis of harmonic distortion. They are

- (i) Filtering
- (ii) Fourier transform
- (iii) Modulation

Each of the above can be implemented by analogue or digital techniques. The digital approach supersedes the analogue one in new designs as a result of digital devices are relatively much cheaper and can be programmable.

3-2-1. Filtering.

With the filtering technique both random transient and steady state harmonics can be measured if the relative phase relationships of the harmonics are of no concern. Phase shifts at different frequencies can be compensated by use of tunable all pass filter, which unfortunately also have different amplitude responses to different signals carrying different frequencies. A filter bank is required to deal with different frequencies. A six-pole Butterworth bandpass filter is a suitable choice because of its monotonically flat amplitude response. Even if the frequency of the input signal shifts slightly from the centre frequency of the filter, there is no need to re-calibrate [21]. In its digital implementation, it is referred to as an Infinite Impulse Response filter. The design of IIR filters has traditionally been based upon the transformation of an analogue filter approximation to a digital filter [21].

3-2-2. Fourier Transform.

The Fourier Transform can be approximated by the discrete Fourier transform which can be speeded up by using Fast-Fourier-transform algorithms. Although the Fast-Fourier-transform algorithm was developed for use on general-purpose computers, some dedicated digital signal processors with FFT-based spectrum analyzers like TI's TMS 320, TRW's TDC 102B and IIT's UDPI 01, on a single PC board, have recently become available on the market. The FFT operates on whole blocks of data at a time in order to

transform the signals from the time domain to the frequency domain. It is essential that analogue signals be bandlimited before sampling. Even if the signal is naturally bandlimited, since additive noise may have a much broader spectrum than the signal, analogue lowpass filtering is almost always necessary prior to sampling. The phase information obtained after the transform of a filtered signal have some degree of phase shift comparing with the original signals. The analogue signals pass through an antialiasing filter, sampler and A/D converter. The next step is windowing, which involves multiplying each sample point in the frame by a weighting coefficient. A discrete window, called a Dolph-Chebyshev window, is a suitable choice. This particular window has a very narrow main lobe. Windowing is required to account for the finite length of sample, since the FFT should operate on an infinitely continuous signal. After weighting, the data passes through the FFT algorithm, which involves squaring and summing of each spectral point [22].

3-2-3. Signal Modulation " +1 and -1 " Technique.

There are various types of modulation methods. The following method, developed by K. L. Shum from an idea in a paper by Dr. M. L. Meade [23], represents a new attempt at measuring components (amplitude and phase) of harmonics in a waveform.

Let a signal be $\sum_{k=h}^{\infty} \hat{U}_k \sin (KW_s t + \theta_k/K)$, where \hat{U}_k is the peak amplitude, θ_k is the angle, K is the order of harmonics referred to W_s (the fundamental angular frequency of the signal) and h can be any positive integer.

Let the gain be switched from +1 to -1 at a reference frequency, so that the gain = +1 ; $0 < t < \pi/W_r$

$$-1 ; \pi/W_r < t < 2\pi/W_r$$

where W_r is the angular reference frequency .

Let the mean level of output over one reference period be U_k

$$U_k = \sum_{k=h}^{\infty} U_k W_r \left[\int_0^{\pi/W_r} \sin(KW_s t + \theta_k/K) dt - \int_{\pi/W_r}^{2\pi/W_r} \sin(KW_s t + \theta_k/K) dt \right] / 2\pi$$

$$= \frac{\sum_{k=h}^{\infty} U_k W_r \left\{ [-\cos(KW_s t + \theta_k/K)]_0^{\pi/W_r} - [-\cos(KW_s t + \theta_k/K)]_{\pi/W_r}^{2\pi/W_r} \right\}}{2\pi KW_s}$$

$$= \sum_{k=h}^{\infty} U_k W_r \left\{ [-\cos(\pi KW_s/W_r + \theta_k/K) + \cos(\theta_k/K)] - [-\cos(2\pi KW_s/W_r + \theta_k/K) + \cos(\pi KW_s/W_r + \theta_k/K)] \right\} / 2\pi KW_s$$

Let $N = KW_s / W_r = Kf_s / f_r$, then

$$U_k = \sum_{k=h}^{\infty} U_k [\cos(\theta_k/K) + \cos(2\pi N + \theta_k/K) - 2\cos(\pi N + \theta_k/K)] / 2\pi N$$

When N is an even number , $U_k = 0$.

When N is an odd number , $\cos(\theta_k/K) = -\cos(\pi N + \theta_k/K)$, then

$$U_k = \sum_{k=h}^{\infty} 2 U_k \cos(\theta_k/K) / \pi N = \sum_{k=h}^{\infty} (2 U_k / \pi) (f_r / Kf_s) \cos(\theta_k/K)$$

$$= \sum_{k=h}^{\infty} A_k (f_r / Kf_s) \cos(\theta_k/K) ; \quad \text{where } A_k = 2 U_k / \pi N \quad (3.6.1)$$

$$\text{When } f_r = Kf_s , U_k = \sum_{k=h}^{\infty} A_k \cos(\theta_k/K) = \sum_{k=h}^{\infty} X_k \quad (3.6.2)$$

Shifting the reference frequency to 90 degrees lag, causes the mean level of output over one reference period to equal

$$U_k = \sum_{k=h}^{\infty} A_k \cos(\theta_k/k - \pi/2) = \sum_{k=h}^{\infty} A_k \sin(\theta_k/k) = \sum_{k=h}^{\infty} Y_k \quad (3.6.3)$$

When N is a fraction, the situation becomes more complicated.

Consider a distorted waveform which has a fundamental and harmonic frequencies.

The radian frequency (ω_r) of the reference clock is given by

$$\omega_r = L \omega_s \quad \text{for } L > 1.$$

The frequency of Mth harmonic is M times the frequency of fundamental.

Let the mean level of output over one fundamental period be U_M .

For $L > M$ and $M = 1, 2, 3, \dots, \infty$,

$$\begin{aligned} U_M &= \sum_{M=1}^{\infty} \hat{U}_M \sum_{Q=1}^L \left\{ \int_{(2Q-2)*2\pi/2L}^{(2Q-1)*2\pi/2L} \sin(M\omega t + \theta_M/M) d(\omega t) \right. \\ &\quad \left. - \int_{(2Q-1)*2\pi/2L}^{2Q*2\pi/2L} \sin(M\omega t + \theta_M/M) d(\omega t) \right\} / 2\pi \\ &= \sum_{M=1}^{\infty} \hat{U}_M \sum_{Q=1}^L \left\{ \left[-\cos(M\omega t + \theta_M/M) \right]_{(2Q-2)\pi/L}^{(2Q-1)\pi/L} \right. \\ &\quad \left. - \left[-\cos(M\omega t + \theta_M/M) \right]_{(2Q-1)\pi/L}^{2L\pi/L} \right\} / 2\pi M \\ &= \sum_{M=1}^{\infty} \sum_{Q=1}^L \left\{ \left\langle -\cos \left[(2Q-1)\pi M/L + \theta_M/M \right] + \cos \left[(2Q-2)\pi M/L + \theta_M/M \right] \right\rangle \right. \\ &\quad \left. - \left\langle -\cos \left[2Q\pi M/L + \theta_M/M \right] + \cos \left[(2Q-1)\pi M/L + \theta_M/M \right] \right\rangle \right\} \\ &\quad \hat{U}_M / 2\pi M \end{aligned}$$

$$= \sum_{M=1}^{\infty} \hat{U}_M \sum_{Q=1}^L \left\{ -2 \cos \left[(2Q-1) \pi M/L + \theta_M/M \right] + \cos \left[(2Q-2) \pi M/L + \theta_M/M \right] + \cos \left[2Q \pi M/L + \theta_M/M \right] \right\} / 2 \pi M$$

Let $P = Q-1$, then

$$\underline{U}_M = \sum_{M=1}^{\infty} \hat{U}_M \sum_{P=0}^{L-1} \left\{ -2 \cos \left[(2P+1) \pi M/L + \theta_M/M \right] + \cos \left[2P \pi M/L + \theta_M/M \right] + \cos \left[(2P+2) \pi M/L + \theta_M/M \right] \right\} / 2 \pi M$$

Let $\phi = \pi M/L + \theta_M/M$, then

$$\begin{aligned} \underline{U}_M &= \sum_{M=1}^{\infty} \hat{U}_M \sum_{P=0}^{L-1} \left\{ -2 \cos (2 \pi M P/L + \phi) + \cos (2 \pi M P/L + \phi - \pi M/L) + \cos (2 \pi M P/L + \phi + \pi M/L) \right\} / 2 \pi M \\ &= \sum_{M=1}^{\infty} \hat{U}_M \sum_{P=0}^{L-1} \left\{ -2 \cos (2 \pi M P/L + \phi) + 2 \cos (2 \pi M P/L + \phi) \cos (\pi M/L) \right\} / 2 \pi M \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\cos (\pi M/L) - 1] \left[\sum_{P=0}^{L-1} \cos (2 \pi M P/L + \phi) \right] / 2 \pi M \right\} \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\cos (\pi M/L) - 1] \operatorname{Re} \left[\sum_{P=0}^{L-1} e^{j(2 \pi M P/L + \phi)} \right] / 2 \pi M \right\} \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\cos (\pi M/L) - 1] \operatorname{Re} \left[e^{j\phi} \sum_{P=0}^{L-1} e^{j2 \pi M P/L} \right] / 2 \pi M \right\} \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\cos (\pi M/L) - 1] \operatorname{Re} \left[e^{j\phi} \sum_{P=0}^{L-1} (e^{j2 \pi M/L})^P \right] / 2 \pi M \right\} \end{aligned}$$

If $\exp j \pi M/L \neq 1$ (which implies $L \neq M$), then

$$\begin{aligned} \underline{U}_M &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\cos (\pi M/L) - 1] \left[1/2 \pi M \right] * \operatorname{Re} \left\langle \left[e^{j\phi} \right] \left[1 - (e^{j2 \pi M/L})^L \right] / \left[1 - e^{j2 \pi M/L} \right] \right\rangle \right\} \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\dots] [\dots] \operatorname{Re} \left\langle [\dots] \left[1 - e^{j2 \pi M} \right] / [\dots] \right\rangle \right\} \\ &= \sum_{M=1}^{\infty} \left\{ 2 \hat{U}_M [\dots] [\dots] \operatorname{Re} \left\langle [\dots] \left[1 - 1 \right] / [\dots] \right\rangle \right\} \\ &= 0 \end{aligned}$$

Modulating the signal for one fundamental period, with a clock frequency ranging from the fundamental to its n th harmonic (where n can be infinity), gives us a mean level of output.

This mean level of output can be represented by the equation (3.6.1) with different f_r/Kf_s ratios, which must be an odd number.

Unfortunately this modulation technique does not allow the direct measurement of the magnitude of individual harmonics, since the presence of higher harmonics also contributes to the mean d.c. output (see equation 3.6.1) . These higher harmonics result in smaller d.c. components as the order of the harmonics increases.

If the d.c. components arising from harmonics higher than the 25th are neglected, then a set of equations (3.7) can be obtained from equations (3.6.2) and (3.6.3) .

Referring to equations set (3.7) ,

- \hat{U}_k is the peak amplitude of the signal.
- θ_k is the angle of signal with respect to the reference (usually taken as the zero crossing point of the fundamental) .
- U_k is the mean level of output modulated at the reference frequency.
- ${}_{90}U_k$ is the mean level of output modulated at the frequency with 90 deg. phase shifted.
- k is the order of the harmonics.

$$\begin{aligned}
{}_0U_1 &= \frac{2}{\pi} \hat{U}_1 \cos \theta_1 + \frac{2}{3\pi} \hat{U}_3 \cos \theta_3 + \frac{2}{5\pi} \hat{U}_5 \cos \theta_5 + \\
&\quad \text{--- --- ---} + \frac{2}{23\pi} \hat{U}_{23} \cos \theta_{23} + \frac{2}{25\pi} \hat{U}_{25} \cos \theta_{25} \\
{}_{90}U_1 &= \frac{2}{\pi} \hat{U}_1 \sin \theta_1 + \frac{2}{3\pi} \hat{U}_3 \sin \theta_3 + \frac{2}{5\pi} \hat{U}_5 \sin \theta_5 + \\
&\quad \text{--- --- ---} + \frac{2}{23\pi} \hat{U}_{23} \sin \theta_{23} + \frac{2}{25\pi} \hat{U}_{25} \sin \theta_{25} \quad (3.7.1)
\end{aligned}$$

$$\begin{aligned}
{}_0U_2 &= \frac{2}{\pi} \hat{U}_2 \cos \theta_2 + \frac{2}{3\pi} \hat{U}_6 \cos \theta_6 + \frac{2}{5\pi} \hat{U}_{10} \cos \theta_{10} + \\
&\quad \text{--- --- ---} + \frac{2}{9\pi} \hat{U}_{18} \cos \theta_{18} + \frac{2}{11\pi} \hat{U}_{22} \cos \theta_{22} \\
{}_{90}U_2 &= \frac{2}{\pi} \hat{U}_2 \sin \theta_2 + \frac{2}{3\pi} \hat{U}_6 \sin \theta_6 + \frac{2}{5\pi} \hat{U}_{10} \sin \theta_{10} + \\
&\quad \text{--- --- ---} + \frac{2}{9\pi} \hat{U}_{18} \sin \theta_{18} + \frac{2}{11\pi} \hat{U}_{22} \sin \theta_{22} \quad (3.7.2)
\end{aligned}$$

$$\begin{aligned}
{}_0U_3 &= \frac{2}{\pi} \hat{U}_3 \cos \theta_3 + \frac{2}{3\pi} \hat{U}_9 \cos \theta_9 + \frac{2}{5\pi} \hat{U}_{15} \cos \theta_{15} \\
&\quad \frac{2}{7\pi} \hat{U}_{21} \cos \theta_{21} \\
{}_{90}U_3 &= \frac{2}{\pi} \hat{U}_3 \sin \theta_3 + \frac{2}{3\pi} \hat{U}_9 \sin \theta_9 + \frac{2}{5\pi} \hat{U}_{15} \sin \theta_{15} \\
&\quad \frac{2}{7\pi} \hat{U}_{21} \sin \theta_{21} \quad (3.7.3)
\end{aligned}$$

$$\begin{aligned}
{}_0U_4 &= \frac{2}{\pi} \hat{U}_4 \cos \theta_4 + \frac{2}{3\pi} \hat{U}_{12} \cos \theta_{12} + \frac{2}{5\pi} \hat{U}_{20} \cos \theta_{20} \\
{}_{90}U_4 &= \frac{2}{\pi} \hat{U}_4 \sin \theta_4 + \frac{2}{3\pi} \hat{U}_{12} \sin \theta_{12} + \frac{2}{5\pi} \hat{U}_{20} \sin \theta_{20} \quad (3.7.4)
\end{aligned}$$

$$\begin{aligned}
{}_0U_5 &= \frac{2}{\pi} \hat{U}_5 \cos \theta_5 + \frac{2}{3\pi} \hat{U}_{15} \cos \theta_{15} + \frac{2}{5\pi} \hat{U}_{25} \cos \theta_{25} \\
{}_{90}U_5 &= \frac{2}{\pi} \hat{U}_5 \sin \theta_5 + \frac{2}{3\pi} \hat{U}_{15} \sin \theta_{15} + \frac{2}{5\pi} \hat{U}_{25} \sin \theta_{25} \quad (3.7.5)
\end{aligned}$$

$$\begin{aligned}
 {}_0U_6 &= \frac{2}{\pi} \hat{U}_6 \cos \theta_6 + \frac{2}{3\pi} \hat{U}_{18} \cos \theta_{18} \\
 {}_{90}U_6 &= \frac{2}{\pi} \hat{U}_6 \sin \theta_6 + \frac{2}{3\pi} \hat{U}_{18} \sin \theta_{18}
 \end{aligned} \tag{3.7.6}$$

$$\begin{aligned}
 {}_0U_7 &= \frac{2}{\pi} \hat{U}_7 \cos \theta_7 + \frac{2}{3\pi} \hat{U}_{21} \cos \theta_{21} \\
 {}_{90}U_7 &= \frac{2}{\pi} \hat{U}_7 \sin \theta_7 + \frac{2}{3\pi} \hat{U}_{21} \sin \theta_{21}
 \end{aligned} \tag{3.7.7}$$

$$\begin{aligned}
 {}_0U_8 &= \frac{2}{\pi} \hat{U}_8 \cos \theta_8 + \frac{2}{3\pi} \hat{U}_{24} \cos \theta_{24} \\
 {}_{90}U_8 &= \frac{2}{\pi} \hat{U}_8 \sin \theta_8 + \frac{2}{3\pi} \hat{U}_{24} \sin \theta_{24}
 \end{aligned} \tag{3.7.8}$$

$$\begin{aligned}
 {}_0U_9 &= \frac{2}{\pi} \hat{U}_9 \cos \theta_9 \\
 {}_{90}U_9 &= \frac{2}{\pi} \hat{U}_9 \sin \theta_9
 \end{aligned} \tag{3.7.9}$$

$$\begin{aligned}
 {}_0U_{10} &= \frac{2}{\pi} \hat{U}_{10} \cos \theta_{10} \\
 {}_{90}U_{10} &= \frac{2}{\pi} \hat{U}_{10} \sin \theta_{10}
 \end{aligned} \tag{3.7.10}$$

$$\text{---} \tag{3.7.11}$$

$$\text{---} \tag{3.7.23}$$

$$\begin{aligned}
 {}_0U_{24} &= \frac{2}{\pi} \hat{U}_{24} \cos \theta_{24} \\
 {}_{90}U_{24} &= \frac{2}{\pi} \hat{U}_{24} \sin \theta_{24}
 \end{aligned} \tag{3.7.24}$$

$$\begin{aligned}
 {}_0U_{25} &= \frac{2}{\pi} \hat{U}_{25} \cos \theta_{25} \\
 {}_{90}U_{25} &= \frac{2}{\pi} \hat{U}_{25} \sin \theta_{25}
 \end{aligned} \tag{3.7.25}$$

For $h = 9, \dots, 25$, equations (3.7.9) to (3.7.25) can be solved simultaneously for the absolute values of A_k and θ_k to give:

$$A_k = \sqrt{X_k^2 + Y_k^2} \quad (3.8.1)$$

$$\theta_k = K \arccos (X_k / A_k) \quad (3.8.2)$$

Equations (3.7.6) to (3.7.8) each have two d.c. terms. The second terms arising from higher harmonics could be eliminated by dividing equations (3.7.18), (3.7.21) and (3.7.24) by a factor of 3 and then subtracting the results from equations (3.7.6) to (3.7.8) respectively. Equations (3.8.1) and (3.8.2) can now be applied to find $A_6, \theta_6, A_7, \theta_7, A_8$ and θ_8 .

Based on the same procedure, the d.c. terms existing in equations (3.7.1) to (3.7.5) can be eliminated and A_1 to A_5 and θ_1 to θ_5 can also be obtained.

The values of each θ_k from the equation (3.8.2) are the absolute values and the quadrants to which they belong is determined according to Fig. (3.4). Fig. 3.4 shows the relationship between X_k, Y_k and θ_k for each individual harmonic. Fig. (3.5) shows the X_k, Y_k, θ_k curves for the fundamental and the third harmonic.

3-2-4. Aspects of the different methods.

Both digital filtering and discrete Fourier Transform algorithms have been developed for use on minicomputers. There are large amounts of software for implementing a digital filter in many digital filters and signal processing books. Most of the programs are written in Fortran-77. In one book [24],

X_k - Y_k - θ_k Relationship

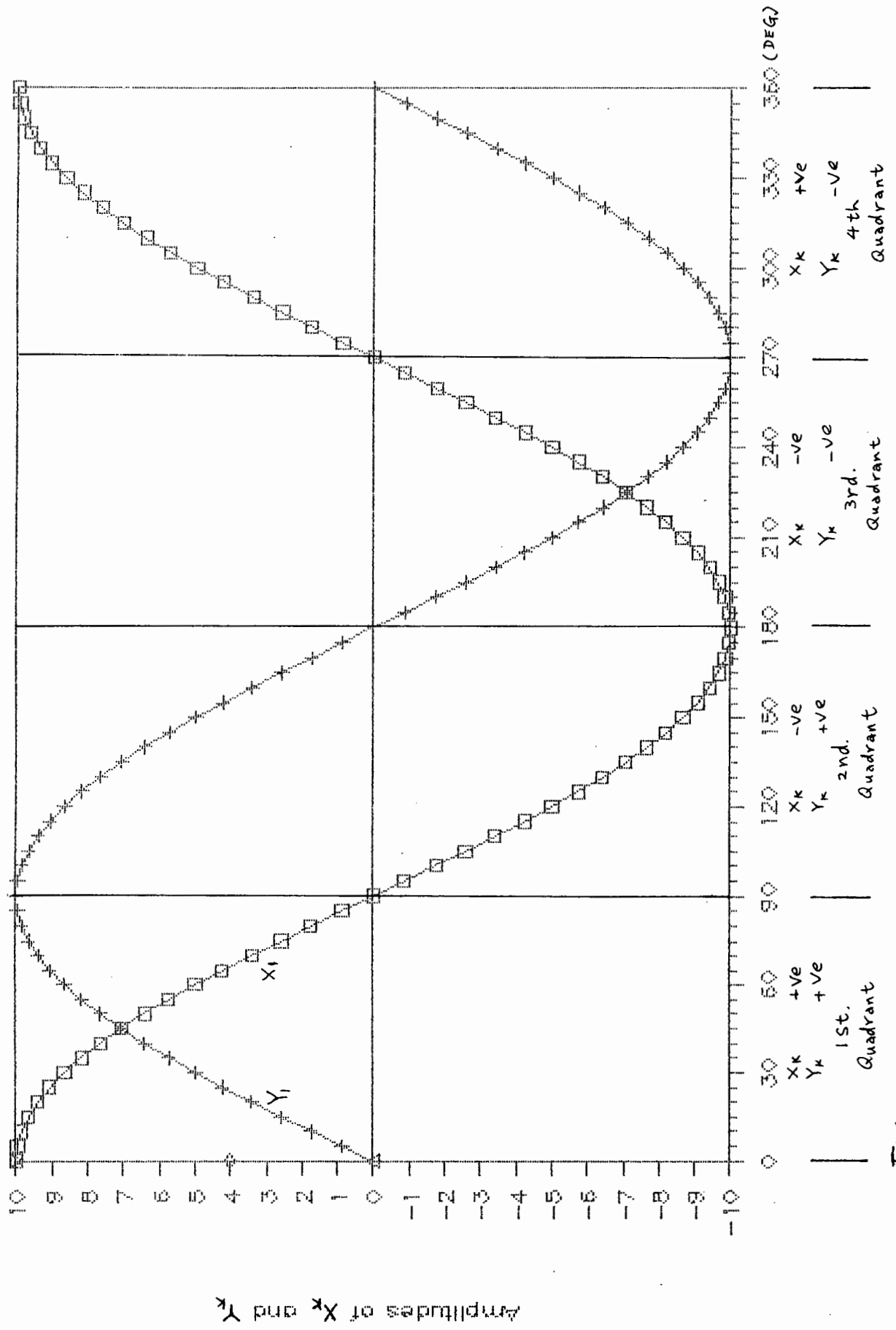


Fig. 3.4 Relationship between X_k , Y_k and θ_k

$X_k - Y_k - \theta_k$ Relationship

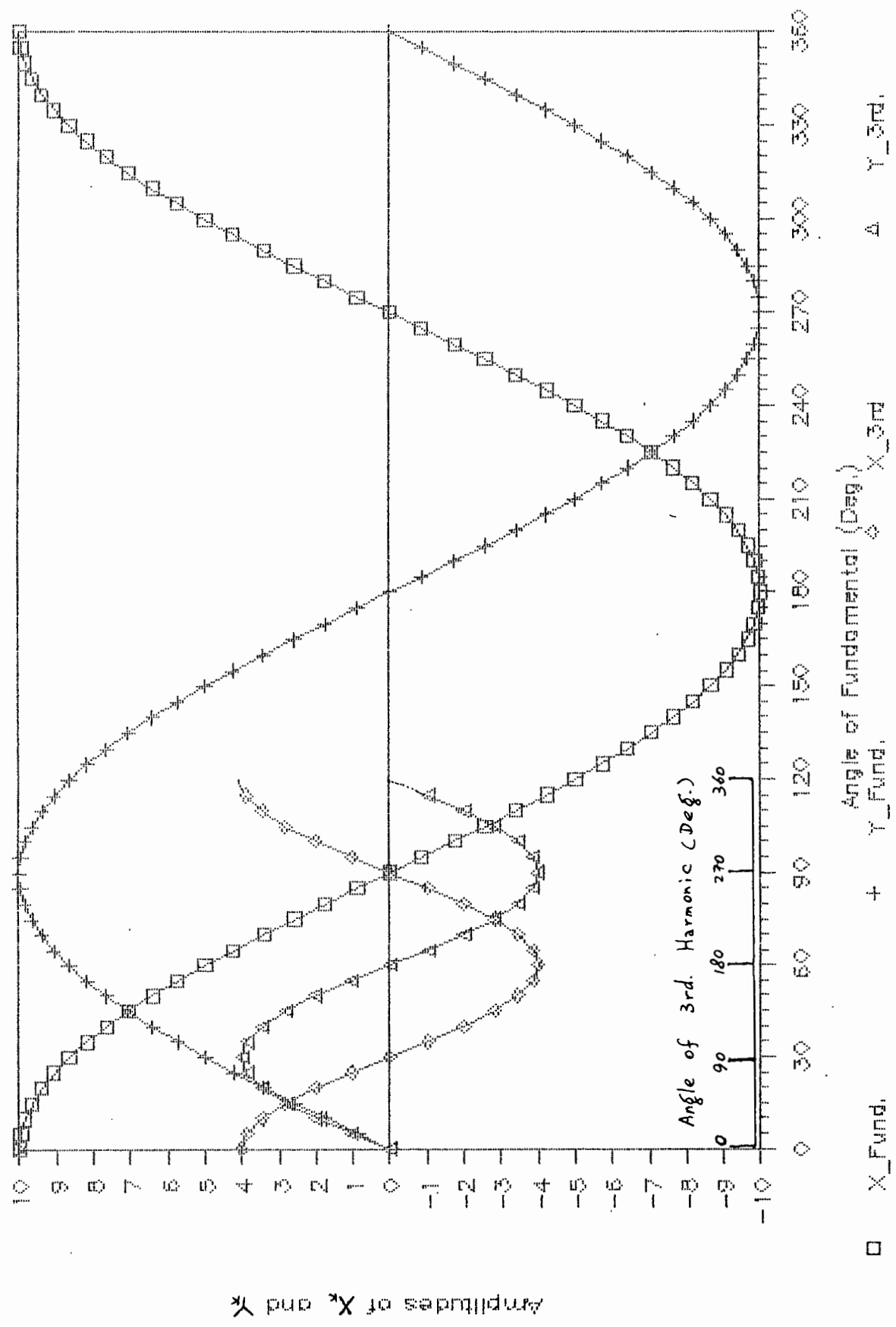


Fig. 3.5 $X_k - Y_k - \theta_k$ Curves of Fundamental and 3rd. Harmonic.

the authors collected several special programs written in assembly languages of several of the most common 16-bit microprocessors, i.e. 8086, MC68000, Z8000, TMS9995, and 9445 respectively for the implementation of real-time software filters in digital form. A similar situation exists for the handling of DFT's. GEÇKİNLİ and YAVUZ, in their book [22], published a special program for measuring the harmonics on the mains.

It is difficult to translate this software into the Basic language and run it on microcomputers because most of microcomputers using the Basic language are slow, especially on input routine. Unfortunately, in measurement of harmonics, a high sample rate is demanded.

One of the principle objective of this project was to design and construct an instrument capable of measuring the magnitude and phase of the harmonic components of both voltage and current accurately and quickly. The signal modulation method described above is the most attractive choice. This method is better than the filtering and Fourier transform methods because it preserves both magnitude and phase information of all harmonics involved. It also has the advantage that any shapes of waveform can be analyzed as in the filtering and Fourier transform methods. This is a more generalized method than the one developed recently by the Russian born Israeli engineer M. A. Slonim and his colleagues P. P. Biringer and I. Rapoport [25, 26] which can handle only a limited number of known waveforms. Another advantage is that it can be easily implemented by digital

circuitry and software, as described in the rest of this thesis.

3-3. Interpretation of results.

Harmonic measurements of a substantial mains power which has multiple frequencies, resonances, fluctuating amplitudes and multiple sources nature, are complicated.

Strange phenomena can be present if overheating or instability occurs in the system during measurement. In this case, measurements of harmonics alone are inadequate and may be misleading.

A non-linear load supplied by a noisy source can cause the net power flow to be away from or towards the load depending on the relative magnitude of the harmonic source in the load and the supply. The magnitude is usually too small to be of concern, otherwise measurements can be postponed until the supply gets quieter.

CHAPTER FOUR

The fancy is indeed no other than a mode of memory emancipated from the order of time and space.

Samuel Taylor Coleridge

4 INSTRUMENTATION

4-1. Introduction

One of the aims of this thesis is to design an instrument based on the " +1 and -1 " signal modulation technique to measure both magnitude and phase of voltage and current, which forms a major part of the work involved in this project.

This instrument should run fast and preferably have the capacity to run in real time. The new trend in electronic system design is to minimize the use of analogue circuitry, especially analogue filters, and instead maximize the use of digital circuits and software. Unfortunately, due to limited funds, a low-cost design is the only choice.

The basic design principle, the actual hardware development, the practical problems encountered and their solutions will be explained in the following paragraphs.

4-2. Basic design philosophy.

Fig. 4.1 shows the basic layout of the instrument. It is convenient to divide it into eight major functional blocks.

4-2-1. Part 1 Scaling.

The maximum inputs to the instrument are defined as :

V - 240 V a.c.

I - 1 A a.c.

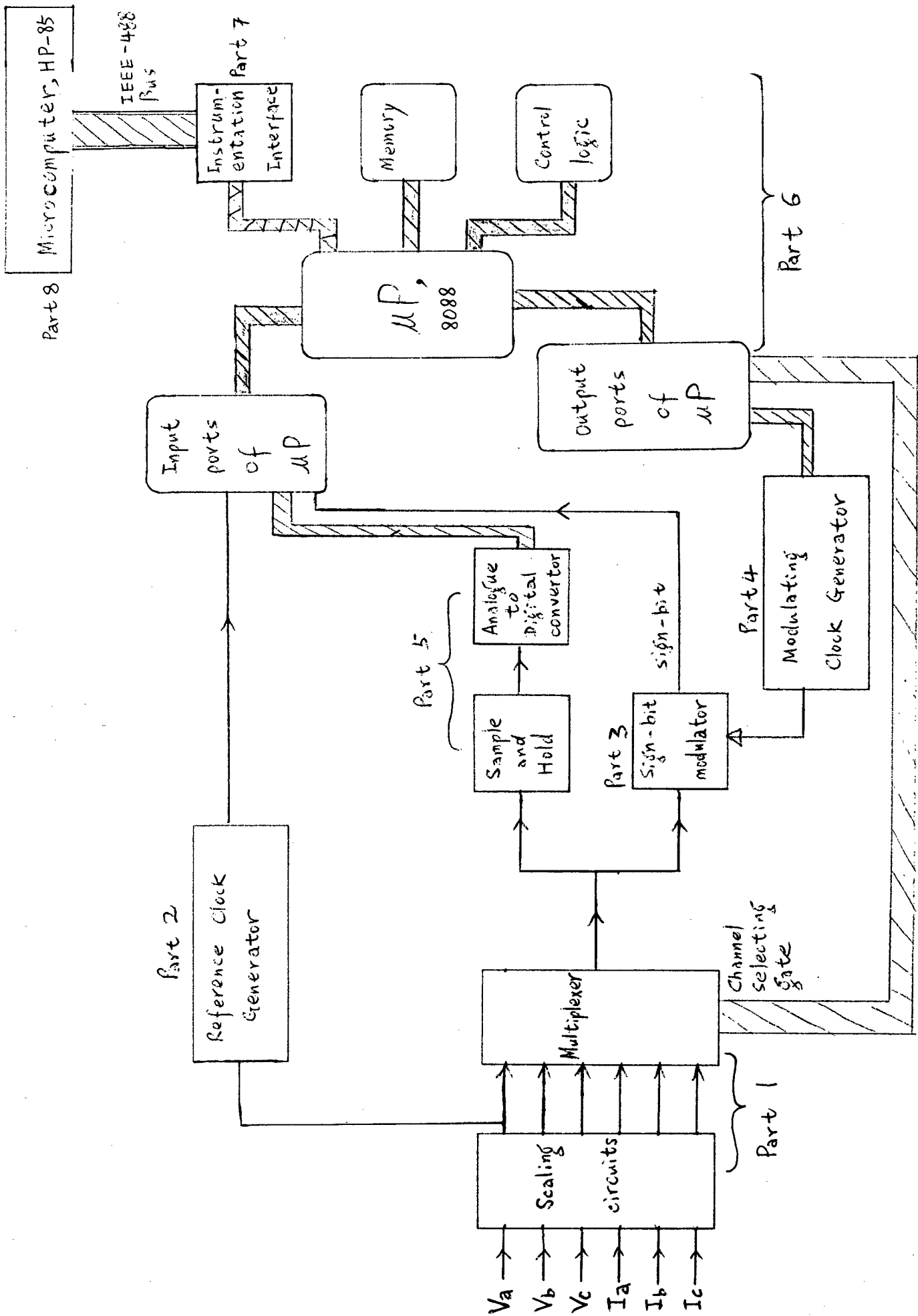


Fig. 4.1 Basic layout of the overall system.

A LED indicator on the front panel of the instrument will light up if any input signal exceeds these values. The signals pass through a scaling circuit made up of high wattage resistors, restricting the amplitude of the signals to within -5 V and +5 V. Scaling down 240V a.c. maximum input voltage to 5V a.c. requires the circuit shown in Fig. 4.2 .

The resistors used are at least half-watt each and 1% accurate.

The total gain of this passive circuit is :

$$V_{out}/V_{in} = 5/(330 + 10) = 1/68$$

If the input voltage signals are larger than 240 Va.c., the values of resistors of voltage scaling circuit should be recalculated to suit the new specification. It is not recommended that potential transformers be used for scaling purposes because their frequency response characteristics depend on such factors as stray inductance, capacitance of the windings and the frequency dependent core losses.

Input current signals must be converted to voltages. The circuit in Fig. 4.3 is employed.

The resistors here are 10-watt each and 1% accurate.

The total gain of this passive circuit is:

$$V_{out}/I_{in} = (4.7 + 2.2) \text{ V/A} = 6.9 \text{ V/A}$$

Over-range current signals can be stepped down using current transformers with 0.1% rated accuracy.

Thereafter the signals are fed to an analogue multiplexer which is controlled by the microprocessor. The multiplexer chooses one of six channels ($V_a, V_b, V_c, I_a, I_b, I_c$) and feeds this to the

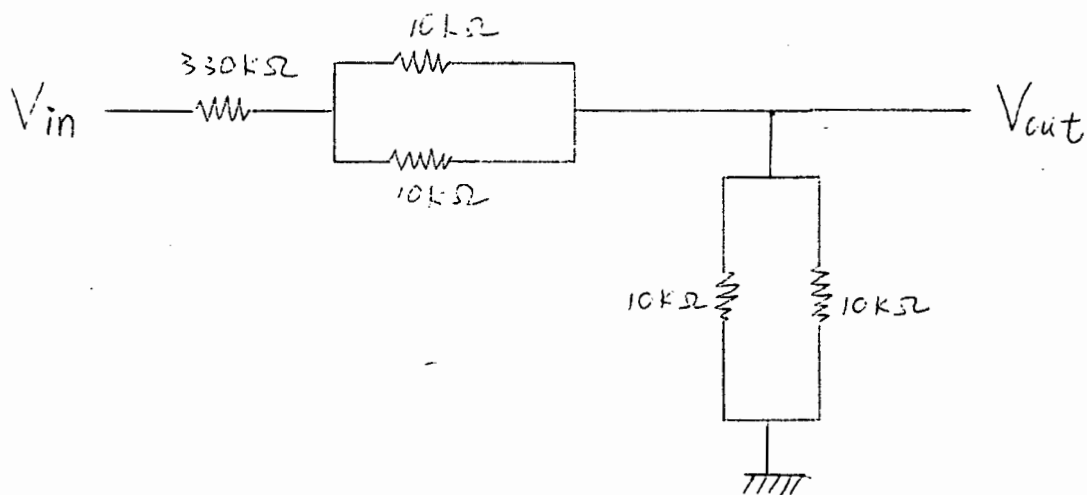


Fig. 4.2 Voltage Scaling Circuit

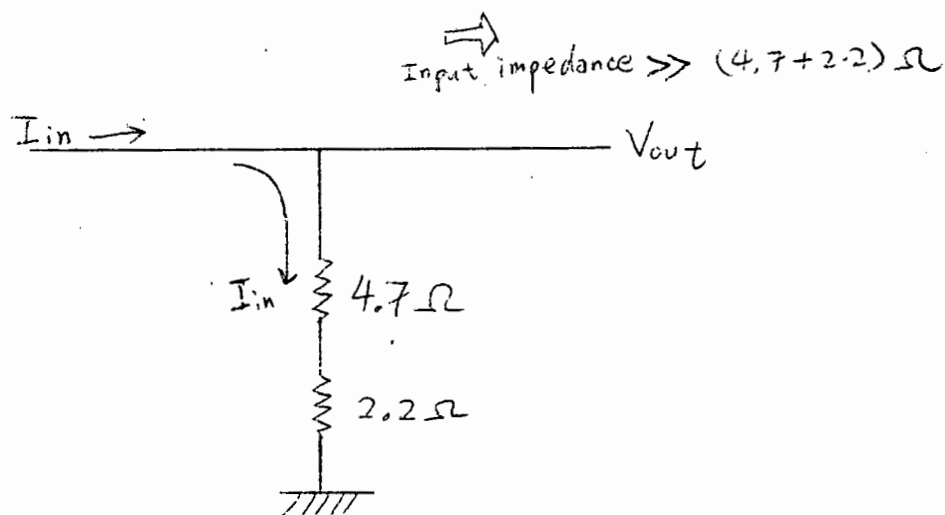


Fig. 4.3 Current Scaling Circuit

high input impedance buffer and then to the inputs of the sign-bit modulator and the sample and hold.

The analogue multiplexer is implemented with cmos analogue gates and a digital decoder. The cmos analogue gates used were IH 5052 which have 150 ohms on-resistance and 60 dB cross coupling rejection. The latter parameter is small enough to be neglected and the former can be compensated. The IH5052 is directly controlled by TTL logic levels. Unfortunately, IH5052 is not a device designed for precision applications. It has voltage and current offsets and on-off switching noise which may degrade the accuracy of the measurement. A better device should be used to replace the IH5052 if funds become available. The decoder causes the multiplexer to route one of the input channels to the buffer. It is controlled by the microprocessor. Fig. 4.4 shows the circuit diagram of the multiplexer.

4-2-2. Part 2 Reference clock generator.

The fundamental of V_a is chosen as the reference clock of the whole system. The signal from channel V_a is noisy and contaminated by harmonics because it comes from the mains. There are two methods of recovering the fundamental from the input signal, namely :

1. Low pass active filter.
2. Phase-locked loop with exclusive-or gate input to eliminate noise.

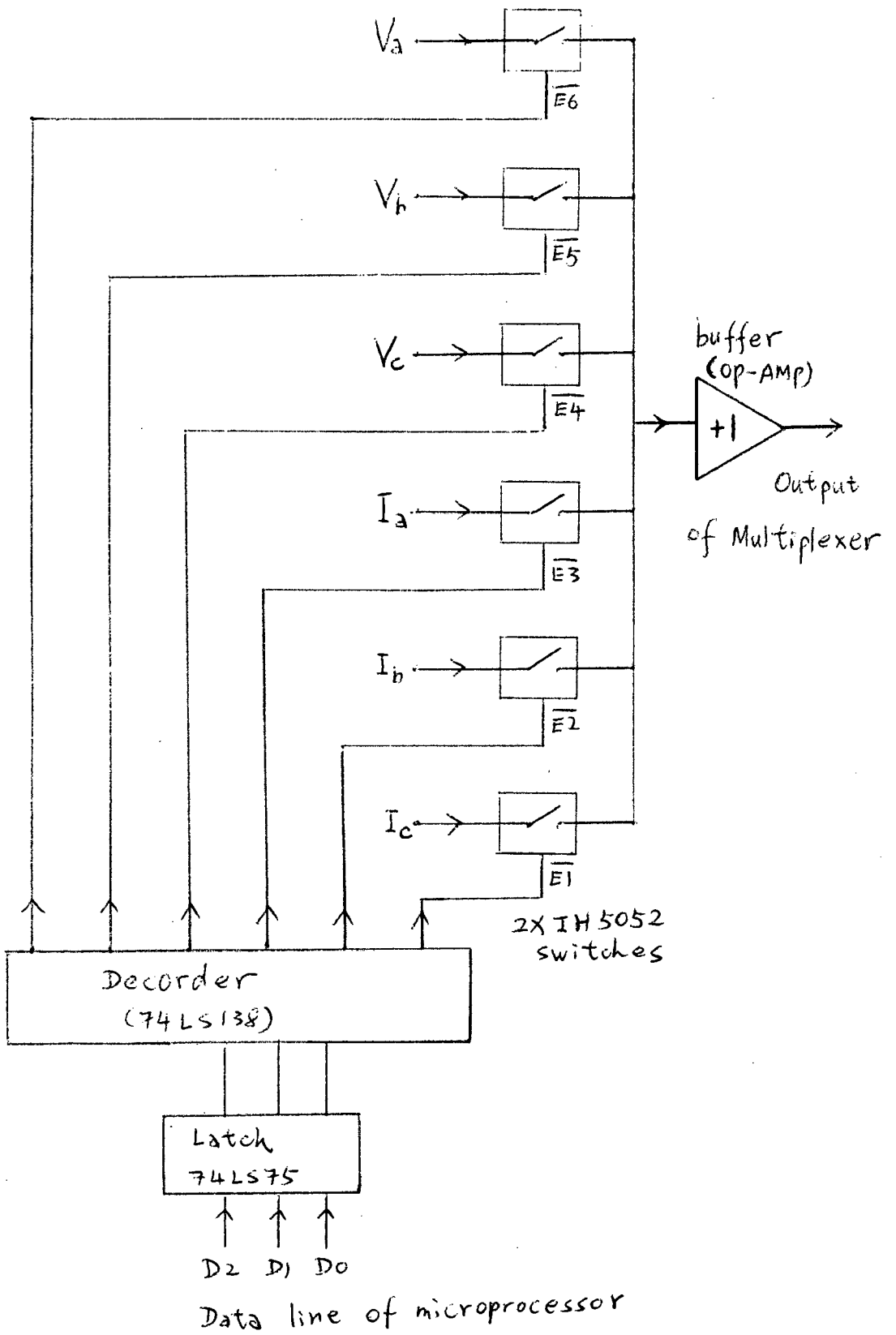
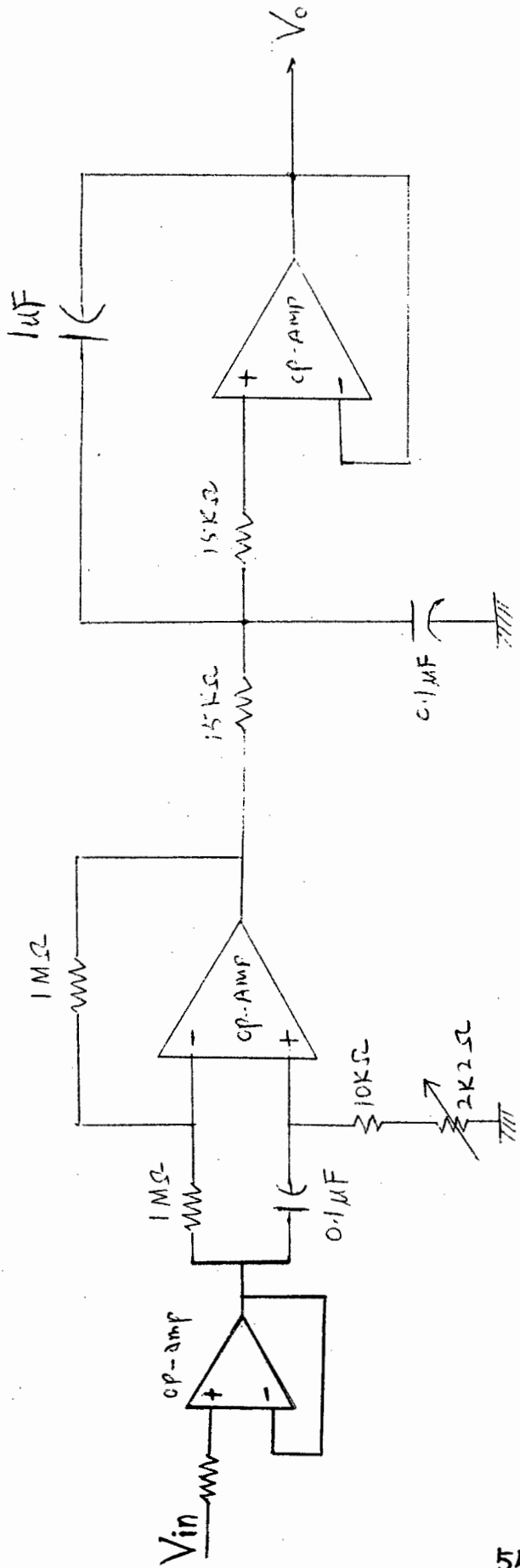


Fig. 4.4

Multiplexer

Both methods generate phase shift which could be compensated for by an analogue phase-shifter. The input impedance of such a phase-shifter must be very high to avoid loading which will have an effect on the accuracy of the signal V_a . One of the disadvantages of a PLL is that it can also lock onto an harmonic of the signal [27]. The filter is thus left as the only option. Unfortunately, neither the low-pass filter nor the phase compensation circuit have a high value of input impedance, so the V_a input signal first has to be buffered using a voltage follower circuit which has an input impedance of several mega-ohms. The low-pass filter is a second order active Tschebyshev type. The 2nd harmonic has 20 dB attenuation relative to the fundamental frequency. Fig. 4.5 shows the circuit [21]. The 2K2-ohm trim pot in Fig. 4.5 has to be adjusted with the help of an oscilloscope until the input signal (50 Hz) of the phase-shift compensator is in phase with the output of low-pass filter. The signal passes through the lowpass filter and is fed to a zero-crossing detector. A zero-crossing detector, implemented by analog comparator LM319, would detect the fundamental filtered signal as it crosses the zero value. Noise will cause multiple zero crossings. Thus another detector must be used in conjunction with the zero-crossing detector to detect the first rising edge. A non-retriggerable one-shot 74LS221 is suitable for this application. Once triggered, its output is independent of further transitions of the input and it will be reset after a preset time. The output of the one-shot will be a clean and well defined reference



buffer phase-shift compensator

low-pass filter

Phase-shift compensator and low-pass filter

Fig. 4.5

clock. This reference clock need not have a 50% duty cycle, because only the period of the reference clock is of importance. The reference clock generator circuit diagram is shown in Fig. 4.6 .

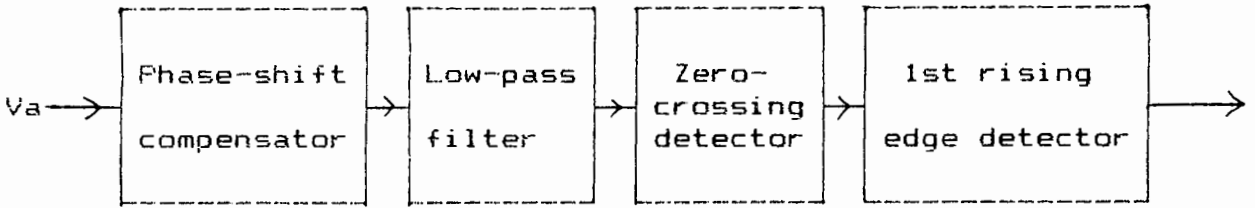


Fig. 4.6 Reference Clock Generator.

4-2-3. Part 3 Sign-bit modulator

The function of the sign-bit modulator is to multiply the amplitude of the input signal by +1 or -1 within a specified period . This operation is controlled by the modulating clock. This procedure has first been implemented by software on a computer. The computer gets the samples directly from the ADC and then multiplies them by +1 or -1 according to the reference clock which is also simulated by software. This method of implementation was attempted, but is impractical, because it uses too much processing time, i.e. it delays the measurement time. Some additional hardware is required to speed up the operation. The output of the modulator feeds a sign detector LM311 to generate a reference clock. The clock will be in a high state if the amplitude of the signal from the modulator is negative and the clock will be in a low state if the signal is positive. The output of the sign detector is assigned to the sign-bit of

the ADC and the ADC therefore only measures the absolute amplitude of the signal and not its sign.

Care must be taken in the design of a sign-bit modulator. The multiplier function of the modulator needs to be symmetrical about the zero voltage reference to generate output values with a positive and negative gain of one during a specified period.

It can only allow small errors due to the offset of the ground reference voltage and the switching noise at the time the signal switches from +1 to -1 or vice versa.

The circuit diagram (Fig. 4.7) and procedure to design a sign-bit modulator is as follows :

The modulating clock is derived from a modulating clock generator, its frequency being controlled by the microprocessor. When the switch 1 is on, the output voltage will be equal to the inverse of the value of the input. When the switch 1 is off, the output will be equal to the input voltage.

Switch 2 is always on and is built in the same IC package as switch 1. The on-resistance of switch 1 and that of switch 2 is therefore always the same even if the temperature changes.

The next step is to look for optimal values of resistances R_1 , R_2 , and R_f in Fig. 4.7 .

Let the on-resistance of switch 1 and 2 be r ohms and its off-resistance be infinite.

According to Fig. 4.8 ,

$$\begin{aligned} e_1 &= (V_o - V_{in})R_1 / (R_1 + R_f + r) + V_{in} \\ &= V_o R_1 / (R_1 + R_f + r) + V_{in} [1 - R_1 / (R_1 + R_f + r)] \end{aligned}$$

$$e_2 = V_{in} R_3 / (R_2 + R_3)$$

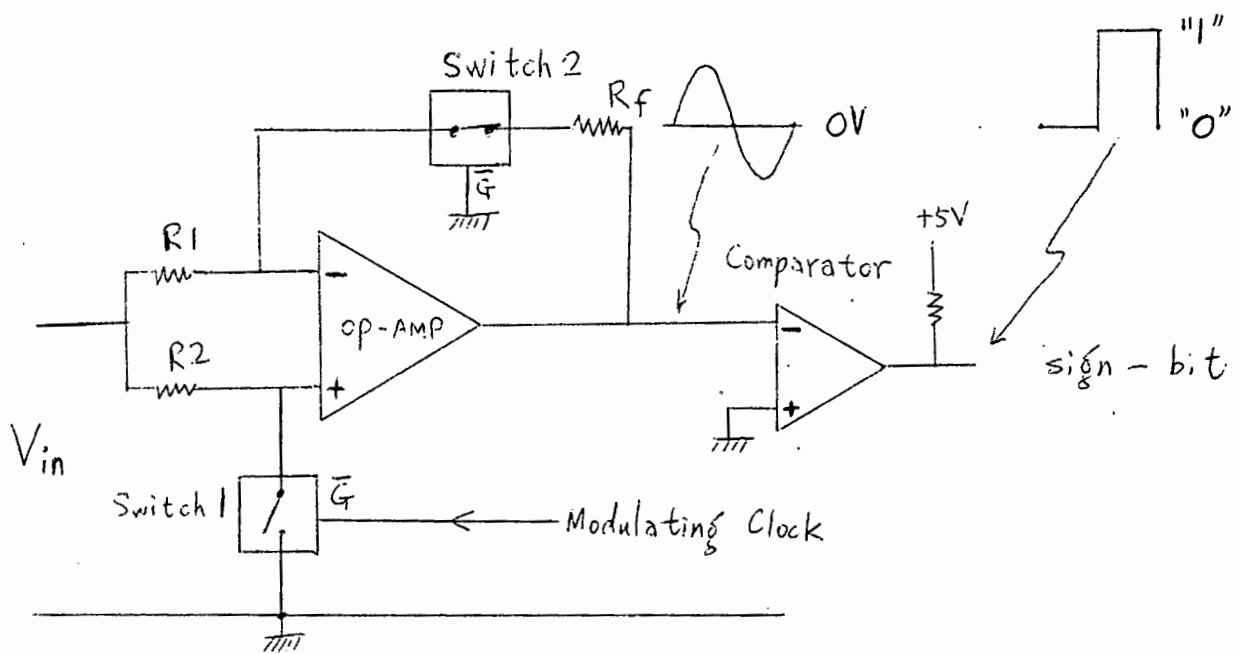


Fig. 4.7 Sign-bit modulator

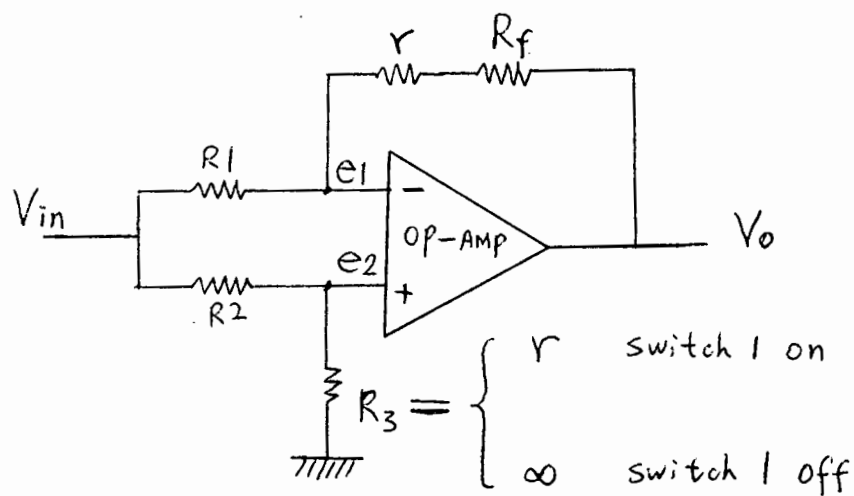


Fig. 4.8. Equivalent circuit of Sign-bit modulator

When the open loop gain is very large, $e_1 = e_2$, therefore

$$V_o R_1 / (R_1 + R_f + r) = V_{in} [R_3 / (R_2 + R_3) + R_1 / (R_1 + R_f + r) - 1]$$

$$V_o / V_{in} = [R_3 / (R_2 + R_3) - (R_f + r) / (R_1 + R_f + r)] (R_1 + R_f + r) / R_1$$

(4.1)

When switch 1 is off, R_3 is equal to infinity.

Equation (4.1) becomes

$$V_o / V_{in} = (R_1 + R_f + r) [1 - (R_f + r) / (R_1 + R_f + r)] / R_1$$

$$= (R_1 + R_f + r) [(R_1 + R_f + r - R_f - r) / (R_1 + R_f + r)] / R_1$$

$$= 1$$

When switch 1 is on, R_3 is equal to r ohms and V_o / V_{in} is expected to be -1 .

Equation (4.1) becomes

$$(R_1 + R_f + r) [r / (R_2 + r) - (R_f + r) / (R_1 + R_f + r)] / R_1 = -1$$

$$r (R_1 + R_f + r) / [R_1 (R_2 + r)] - R_f / R_1 - r / R_1 = -1$$

$$r [(R_1 + R_f + r) / (R_2 + r) - 1] / R_1 - R_f / R_1 = -1$$

$$r [(R_1 + R_f - R_2) / (R_2 + r)] - R_f / R_1 = -1$$

Taking $R_1 + R_f - R_2 = 0$, the expression becomes $R_f = R_1$ and then $R_2 = 2 R_1 = 2 R_f$. The modulator is implemented by a precision operational amplifier (OP-27) [28], a cmos analogue switch IH5052 and metal film precision resistors. Choosing $R_1 = 100k$ ohms the other values can be derived as, $R_2 = 200k$ ohms and $R_f = 100k$ ohms. The circuit in Fig. 4.9 is the actual modulator.

4-2-4. Part 4 Modulating clock generators.

The modulating clock generator is a programmable square wave generator. It must be possible for the microprocessor to set

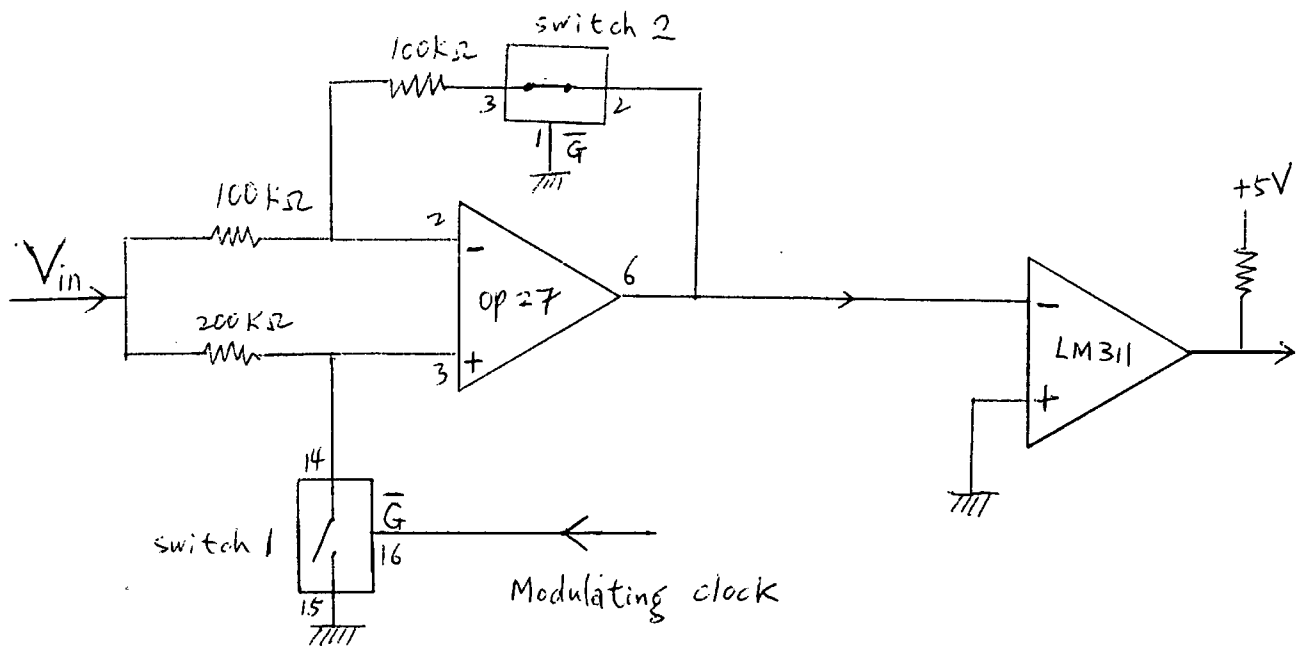


Fig. 4.9 Actual Sign-bit Modulator circuit

its output frequency to the fundamental or any of the harmonics of the reference clock from the zero-crossing detector. One important point is that it must have the capability to synchronize with the input reference clock with very little phase shift error, ideally zero-phase shift. Another clock generator operating at the same frequency, but with a 90 degree phase shift is required to run in parallel with the zero-phase-shift one. This could be implemented in software, but the use of a digital phase shifter is preferable in order to save computing time in the microprocessor. The Intel chip 8254 [29] is chosen as the in-phase clock generator. Its operating clock frequency is 2.5 MHz. The 8254 has three programmable interval count-down counters. When counter 0 operates in mode 3, it behaves as a square wave generator. When counter 1 operates in mode 2, it behaves as an automatic reloaded counter. To calculate the frequency of the Nth order harmonic of the input signal counter 1 must count the duration between two successive rising edges of the fundamental filtered zero-crossing (ZC) signal, i.e. the duration of one cycle of the fundamental component of the input signal. The microprocessor will then read the value of the count from counter 1 and divide it by N. After dividing the value of the count by N, the microprocessor sends this value to counter 0 to generate a modulating square wave clock which is of the same period as the Nth harmonic of input signal. In order to obtain the value of the count from counter 1, the clock input of counter 1 must be inhibited by using the GATE1 input of this

counter. Otherwise, the count may be in the process of changing when it is read, giving an undefined result. Counter 0 also has a GATE0 input which is used to synchronize it with the rising edge of the ZC signal. Fig. 4.10 shows the controlling circuit and timing diagram of counter 1. An innovative device, called the dual edge triggered flip-flop (DET FF) is used to allow counter 1 to operate in counting mode between two assigned successive rising edges of the ZC signal. Unfortunately, in order to prevent counter 1 from operating repeatedly, the first rising edge of the ZC signal cannot be directly applied to the DET flip-flop. Instead, the microprocessor has to poll the ZC signal until it detects a change state low to state high. It then issues a GATE0 signal which in turn activates the GATE1 input line of counter 1. This will become inactive again after the second successive rising edge of the ZC signal. Whenever the GATE1 input line is inactive, the final value of the count is latched and the microprocessor can read it from counter 1. Another modulating clock has a 90 degree phase-lag in relation to the first one. This clock generator is implemented using a phase-lock loop (PLL) technique. The chip chosen was a cmos 4046 [30]. The PLL was designed to lock to the input clock signal with a frequency range from 35 Hz to 1.5 KHz. This circuit is programmed to have a fixed 90 degree phase-shift between the input and output clock signals by setting the B inputs of a cascaded 8-bit BCD magnitude comparator chip 74C85 to 89. Fig. 4.11 shows the circuit of the digital phase

$$U(\theta - \frac{\pi}{2})$$

output ↑

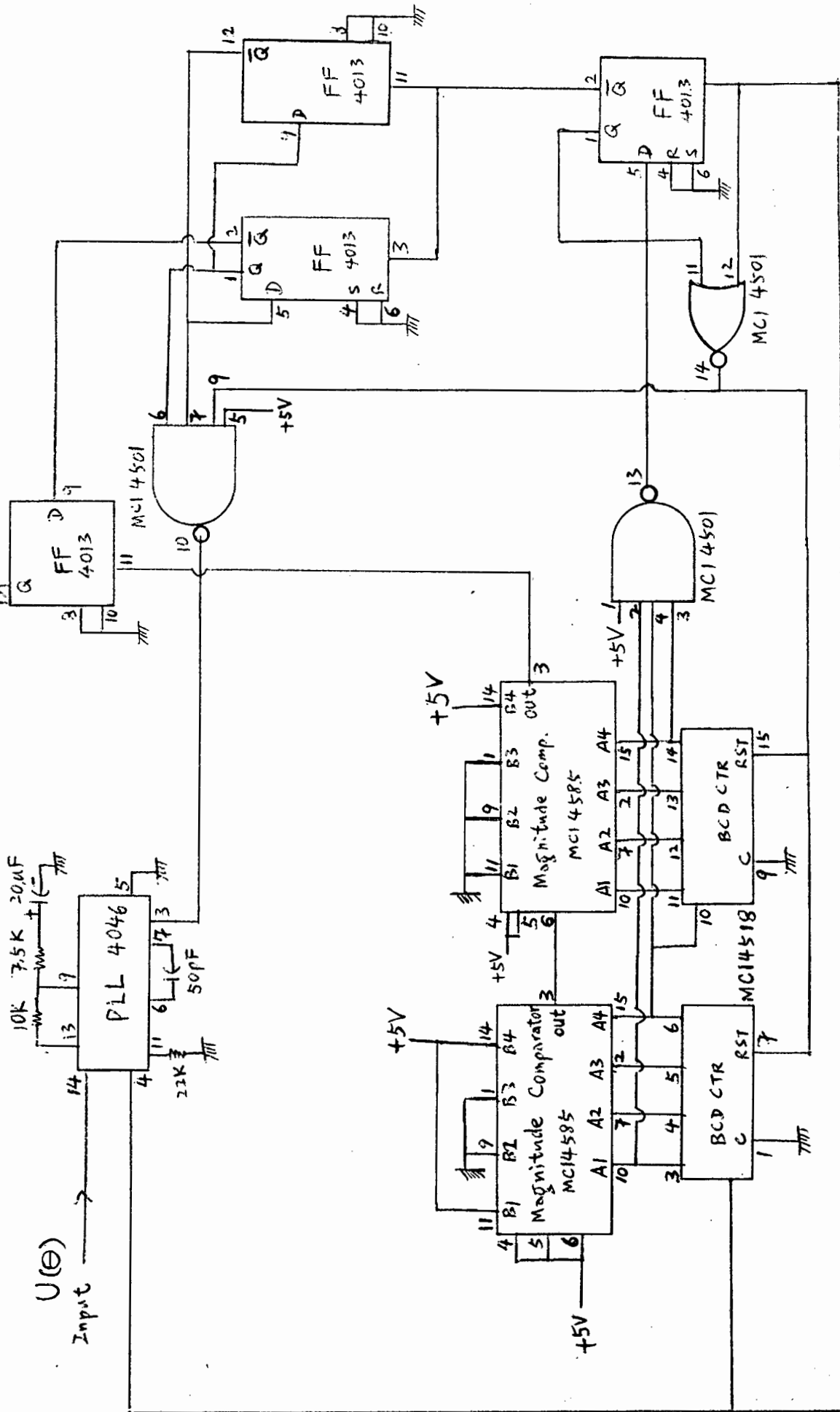


Fig. 4.11 Digital phase shifter (set to 90°)

shifter. Both clocks feed an analogue multiplexer (cmos 4051) and one of them is selected by the microprocessor as a modulating clock. Fig. 4.12 shows a modulating clock generator.

4-2-5. Dual-edge triggered flip-flop (DET FF) .

Before further discussion of other circuits, a commercially unavailable device, called a dual-edge triggered flip-flop has to be mentioned, because it will appear frequently later on. There are occasions when the design of discrete logic circuits can be simplified if DET FFs are utilised. The DET FF is developed with the use of a controlled glitch and its circuit and timing diagram are shown in Fig.4.13.

Referring to Fig.4.13 , the output goes to the 1 state on every positive transition of the input A line and the output goes to the 0 state on every positive transition of the input B line. The output of the flip-flop is capable of being reset by another A line transition immediately after being cleared, regardless of the level of B line. A controlled glitch occurs whenever the B line makes a positive transition. The circuit's operation is as follows :

1. Qa is set by every positive transition of line A.
2. If Qa is set, FFB is enabled and set on a positive transition of line B;
3. this causes FFA to clear, which now clears FFB via its clear input.
4. Thus FFB is only set for the time it takes itself to set,

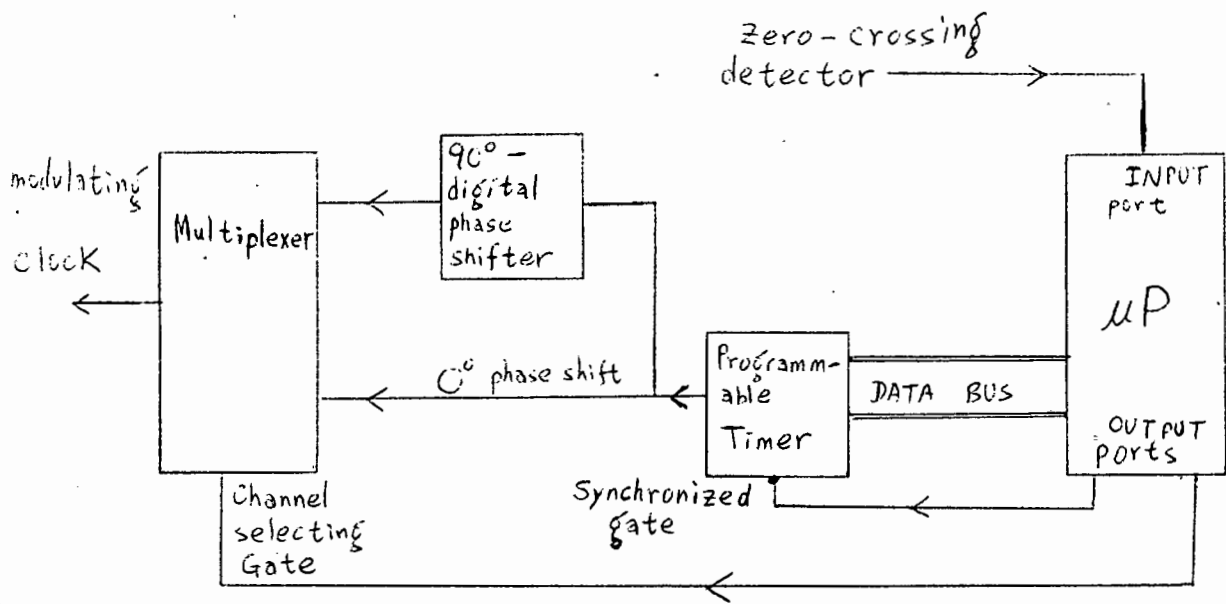


Fig 4.12 Modulating Clock Generator

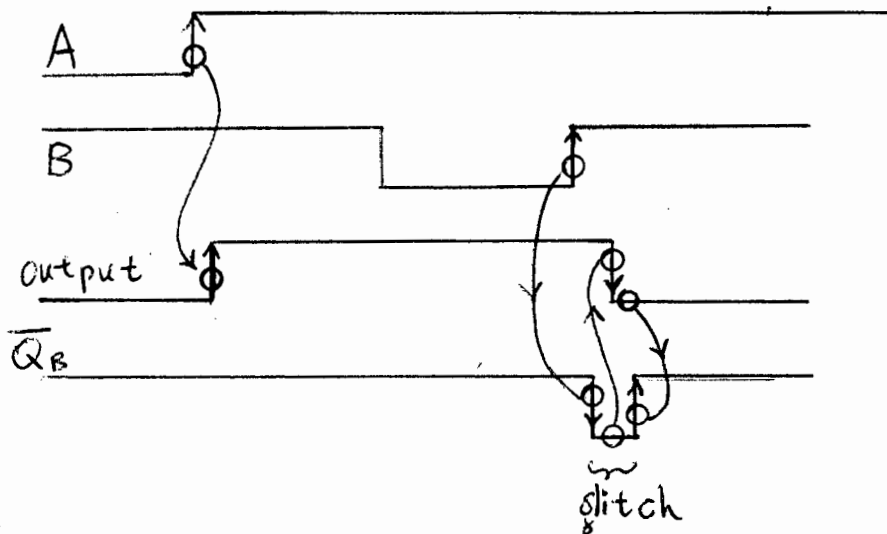
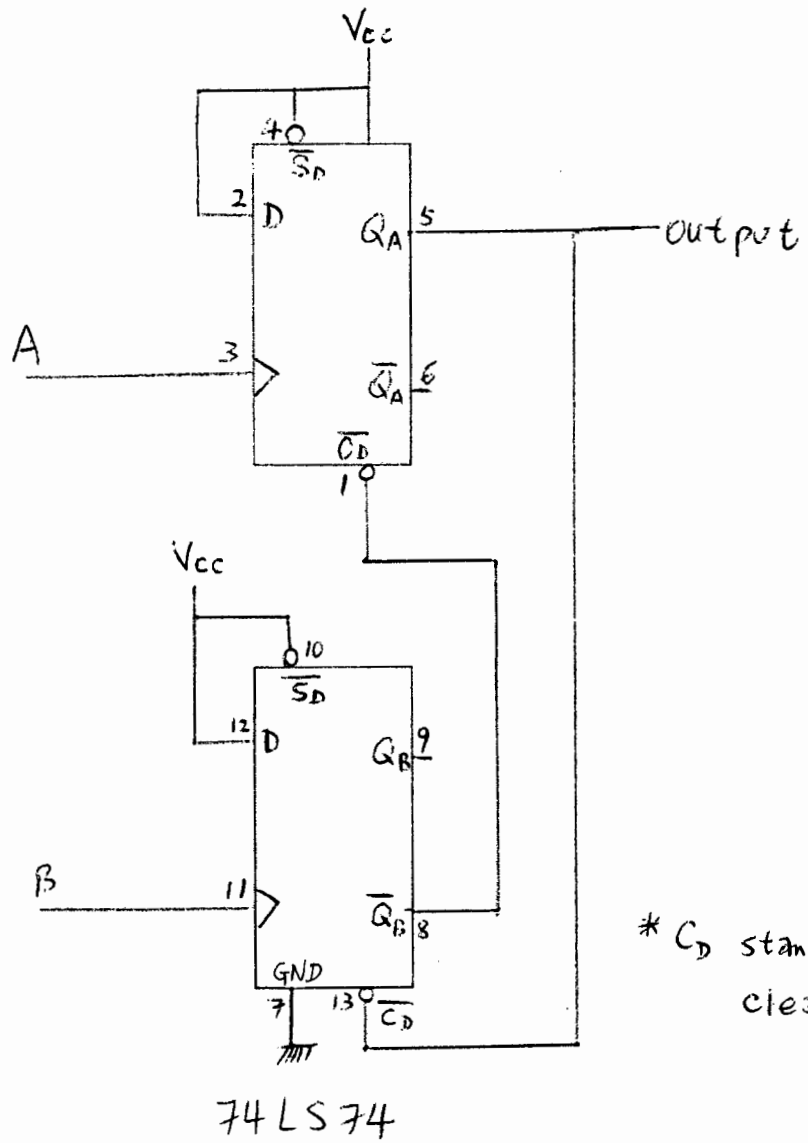


Fig. 4.13 Dual-edge triggered Flip-Flop (DET FF)

plus the time it takes for FFA to clear. Since this is about two propagation delay times, FFB creates a glitch of perhaps 40 ns maximum.

5. The positive transition of the line B causes the glitch, which is the setting of FFB.
6. When FFB is set, it causes the clearing of FFA, and when FFA clears, it clears FFB terminating the glitch.
7. In summary, the positive edge of the B line causes the output to rise, and the positive edge of the B line causes the glitch, which causes the output to fall.

4-2-6. Part 5 Sample- and- Hold and Analogue- to- Digital Convertor (ADC).

It is necessary to locate a sample and hold device LF398 in front of an analogue to digital convertor, even if the ADC has a very fast conversion speed. Its function is to hold the input signal constant for the duration of the sampling of the ADC. It has a storage capacitor to store the input signal value and also to smooth very short spikes which are fatal to the accuracy of an ADC. A small value of storage capacitor is preferable for high sample rate applications and the capacitor used should have a very low loss. Polyethylene type capacitors are employed. The sample and hold device has a FET type input with a very high input impedance to prevent the leakage of charge from the storage capacitor. It should also have a fast slew rate to follow the change of input signal during sampling. Access times also need

to be short for high speed applications.

The ADC was based on a 12-bit successive approximation register 74C905, a fast analogue comparator LM361 and a R-2R resistor ladder. A homemade ADC system was used instead of a commercially available one, because high speed 12-bit ADCs are expensive and the cheap ones are too slow [31]. If there are enough funds, a commercially available fast ADC should be employed to ensure the accuracy of the measurement.

The principle of the successive approximation type ADC will not be discussed further here. There is extensive literature concerning data conversion and acquisition which explains in detail how such ADC 's work.

In order to drive the 12-bit 50K/100K resistor ladder network and achieve + or - 1/2 LSB resolution, two cmos 74HC244 chips [30] are used as buffers. The power supply of the 74HC244 is regulated. Fig. 4.14 and Fig. 4.15 show the ADC system and its timing diagram respectively.

The successive approximation register has such inputs as a clock line, a start line (\bar{S}) and a data line (D) . The outputs are data lines D0 to D11 and a conversion complete line (\bar{CC}) .

The operation clock frequency, derived from the 15 MHz of the clock generator of the microprocessor, is 1.25 MHz, ($15/12 = 1.25$) .

The sampling rate is 13.2 μ S. In 20 ms, the ADC can take 1470 samples. According to Sharon's Theorem the minimum sampling frequency should be $2*25*50$ Hz = 2.5 KHz. By increasing the sampling frequency a more accurate result of measurement is

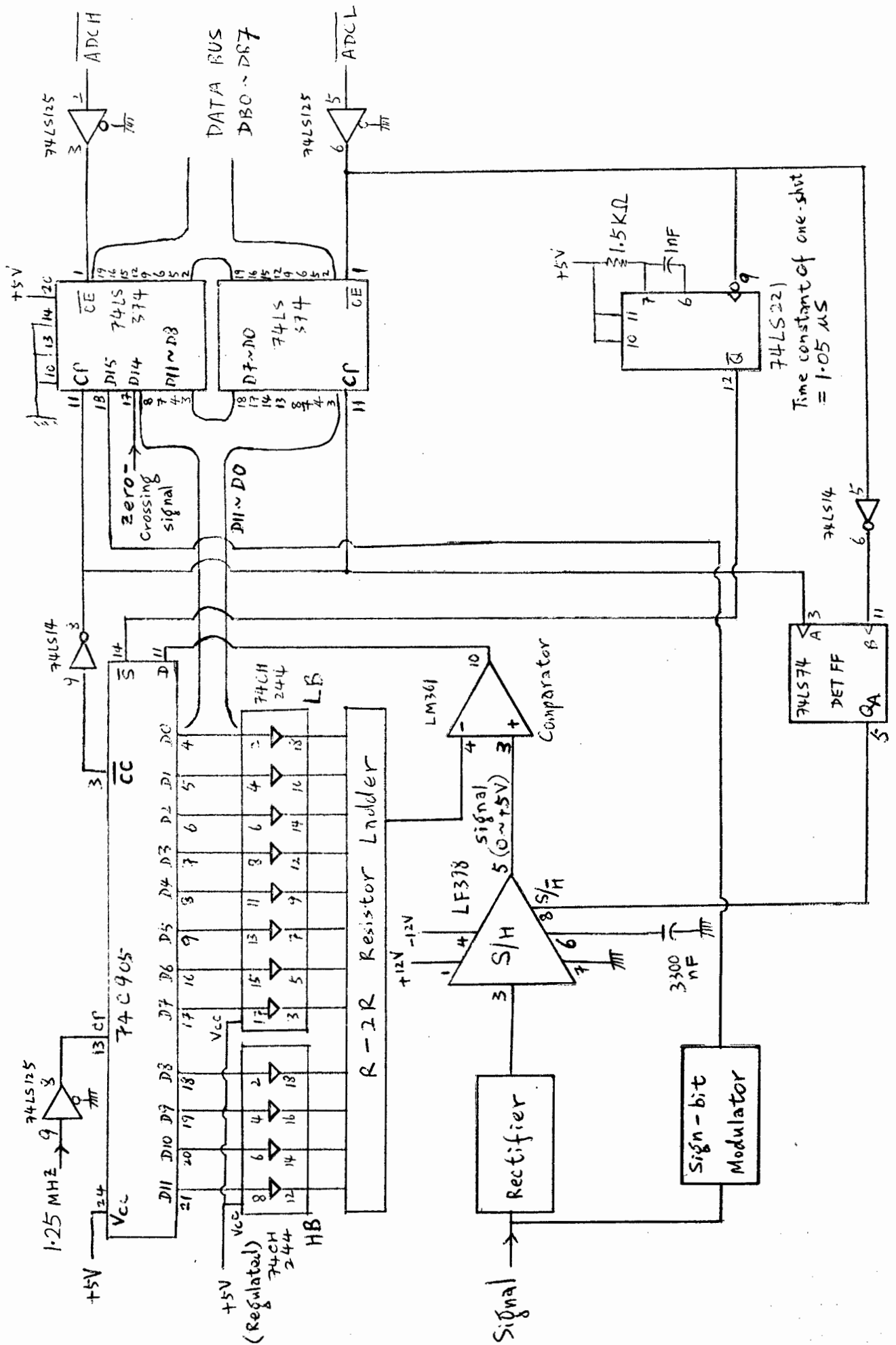


Fig. 4.14 Analogue-to-Digital Converter system

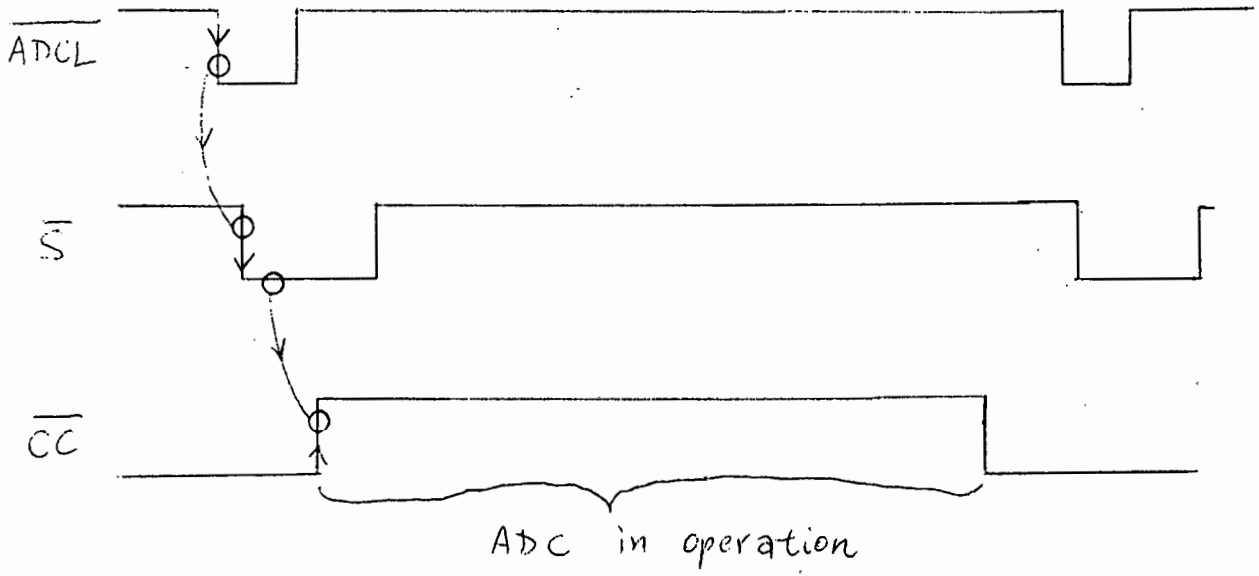


Fig. 4.15 Timing diagram of ADC.

obtained. It should be realized that the settling time of the ADC must be less than the sampling time between two successive samples.

The $\overline{\text{ADCL}}$ line feeds the one-shot circuit to create the $\overline{\text{S}}$ signal of the ADC which starts at the rising edge of $\overline{\text{ADCL}}$ and ends after one operational clock period of the ADC.

Both the CC and ADCL signals feed a DET FF to set up the control logic input (S/H) of the sample-and-hold device. Fig. 4.16 shows the circuit and timing diagram.

During the period between the rising edges of control signals "ADCL" and "CC", the sample-and-hold device operates in hold mode and the rest time in sample mode.

$\overline{\text{S}}$ is derived from a monostable with a period of 1.05 μs , which ensures that $\overline{\text{S}}$ is held in the 0 state for at least one operational clock period of the ADC, this being necessary to initiate a conversion. The monostable is triggered when the low byte of the ADC is read, and the sample-and-hold device is switched to hold mode, ready for the next conversion. The data input (D) comes from the output of the comparator. The conversion complete output ($\overline{\text{CC}}$) goes high whenever the conversion begins and remains at the 1 state during a conversion.

After a maximum of 13 cycles it goes to the 0 state and the conversion is complete. This latches the data outputs into two eight-bit latches to be read by the microprocessor. It also switches the sample-and-hold device back to sample mode. When the microprocessor reads the 16-bit port ADCP, the chip select line for the ADC (from decoder 74LS138) goes low. This,

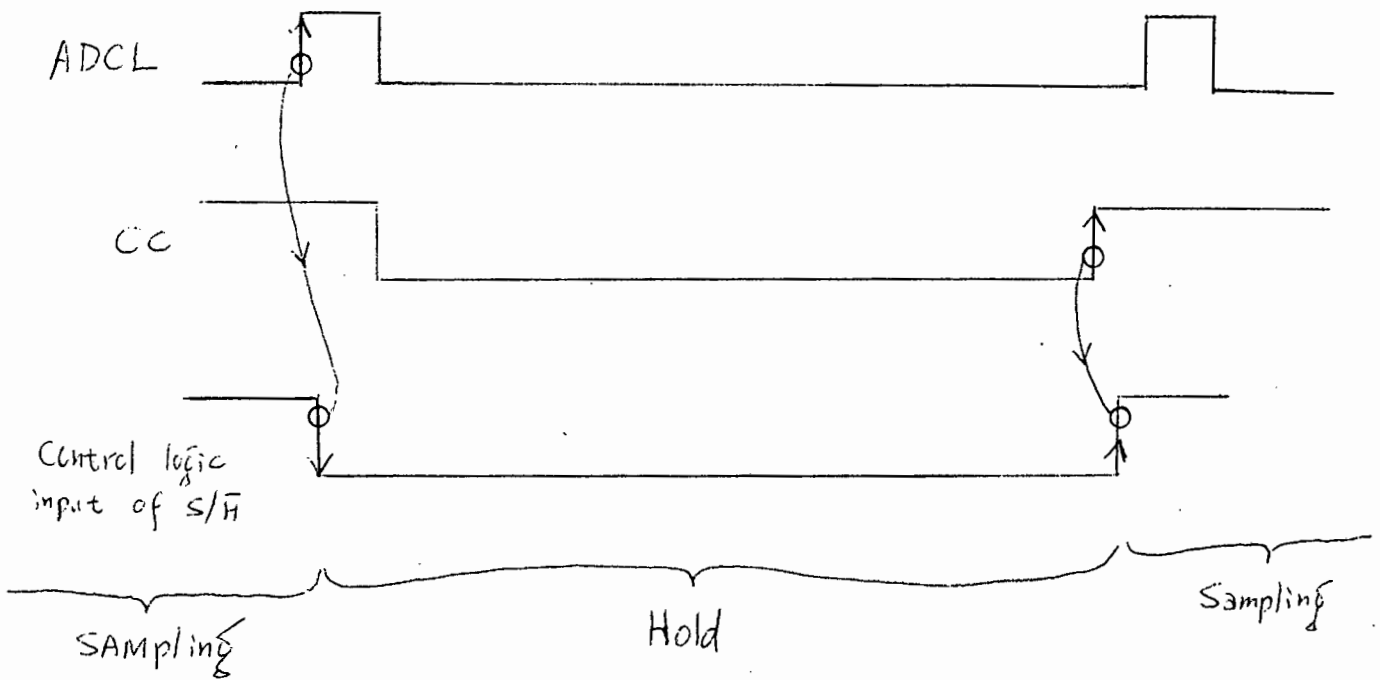
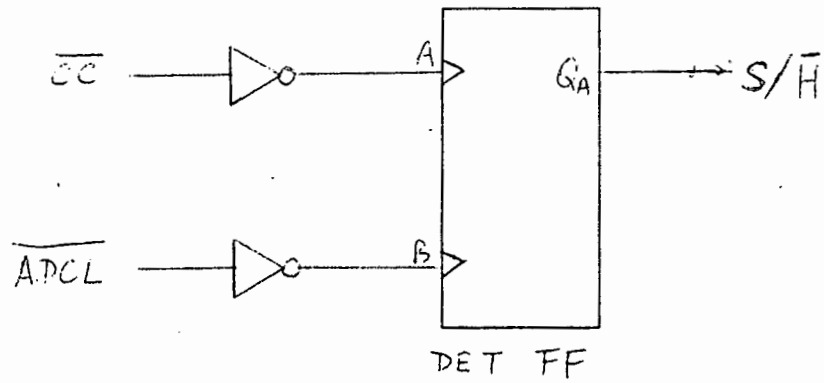


Fig. 4.16 Controlling circuit of S/H device and its timing diagram.

together with the read strobe and A0 being low, generates $\overline{\text{ADCL}}$, which enables the low byte from the latch onto the data bus. The microprocessor then issues a second read with A0 high to read the second byte. This ensures $\overline{\text{ADCH}}$ to go low, allowing the second latch to put the high byte onto the data bus.

Fig. 4.17 shows its circuit and timing diagram.

Only 5 bits of the MSB are used to represent the input signal in digital form, i.e. D8 to D11 and D15. D12 to D13 are permanently tied to ground and D14 is tied to the zero-crossing detector's output. In other words D14 is used as a semaphore to show when the zero crossing occurs.

D15 is the sign bit of the data which is generated from the sign-bit modulator. If it is low, the data is positive; if high, the data is negative.

The input signal of the ADC cannot go beyond the range of 0 to 5 volts, because the ADC operates only within these limits.

A.C. input signals have to be rectified before they can be fed to the ADC. The rectifying circuit is exactly the same as the one used as the modulating clock generator. Fig. 4.18 shows the circuit. Referring to Fig. 4.18, whenever the input signal is positive, the output of comparator LM319 goes high. This switches off the switch IH5052, so the output signal follows the input signal. Whenever the input signal is negative, the output of LM319 goes low to turn on the switch, so that the circuit has a gain of -1, rectifying the signal.

Data expressed in this form is better than in 2's complement form because it gains one more bit, i.e. 13-bit accuracy.

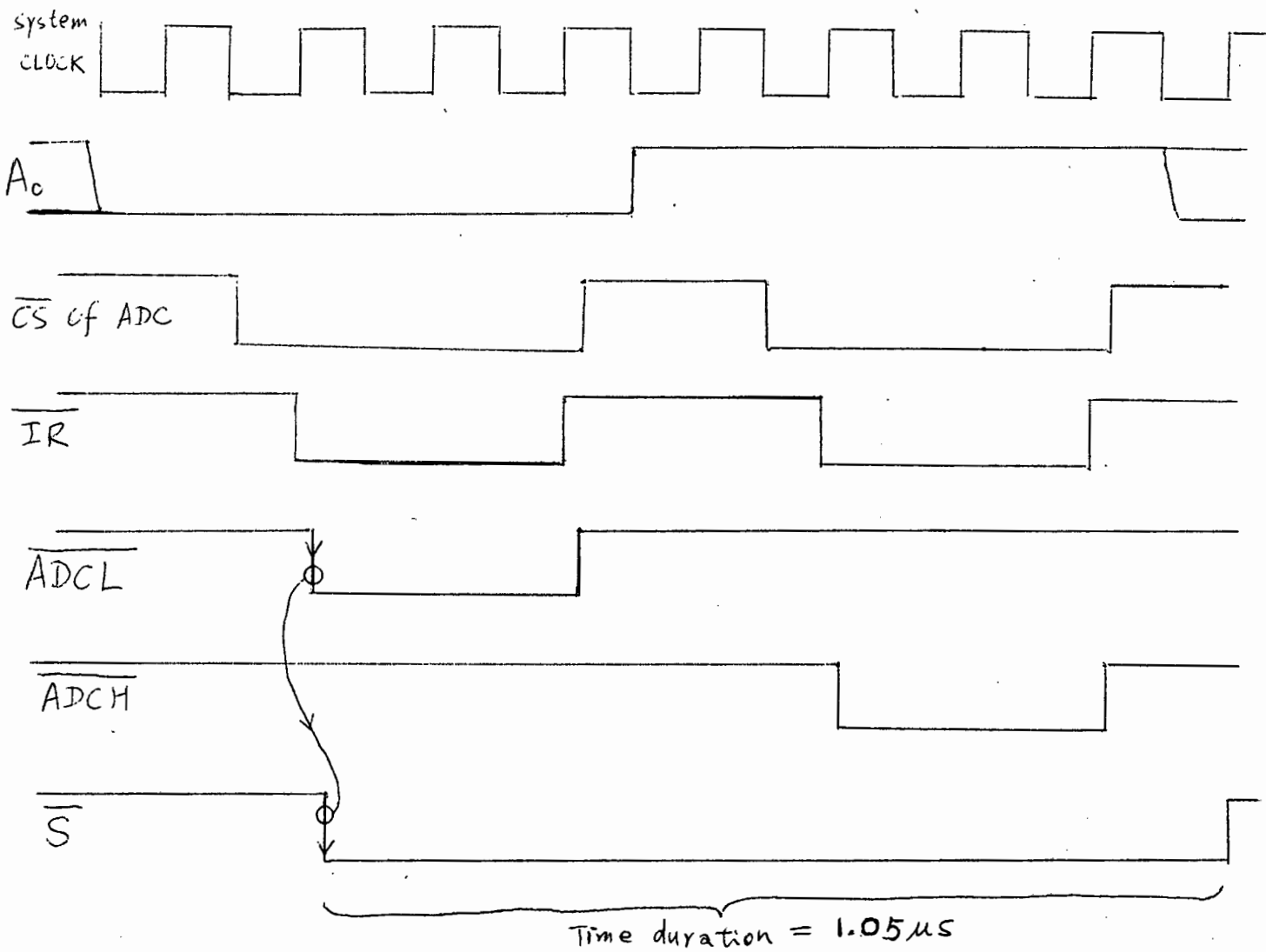
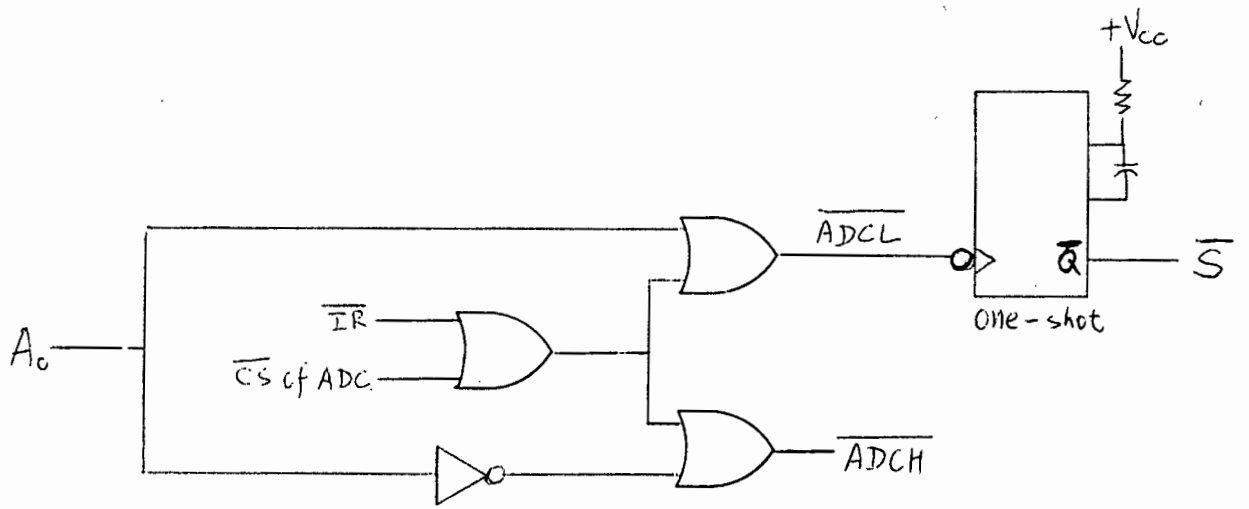


Fig. 4.17

Circuit diagram of signals \overline{ADCL} , \overline{ADCH} , \overline{S} and their timing diagram.

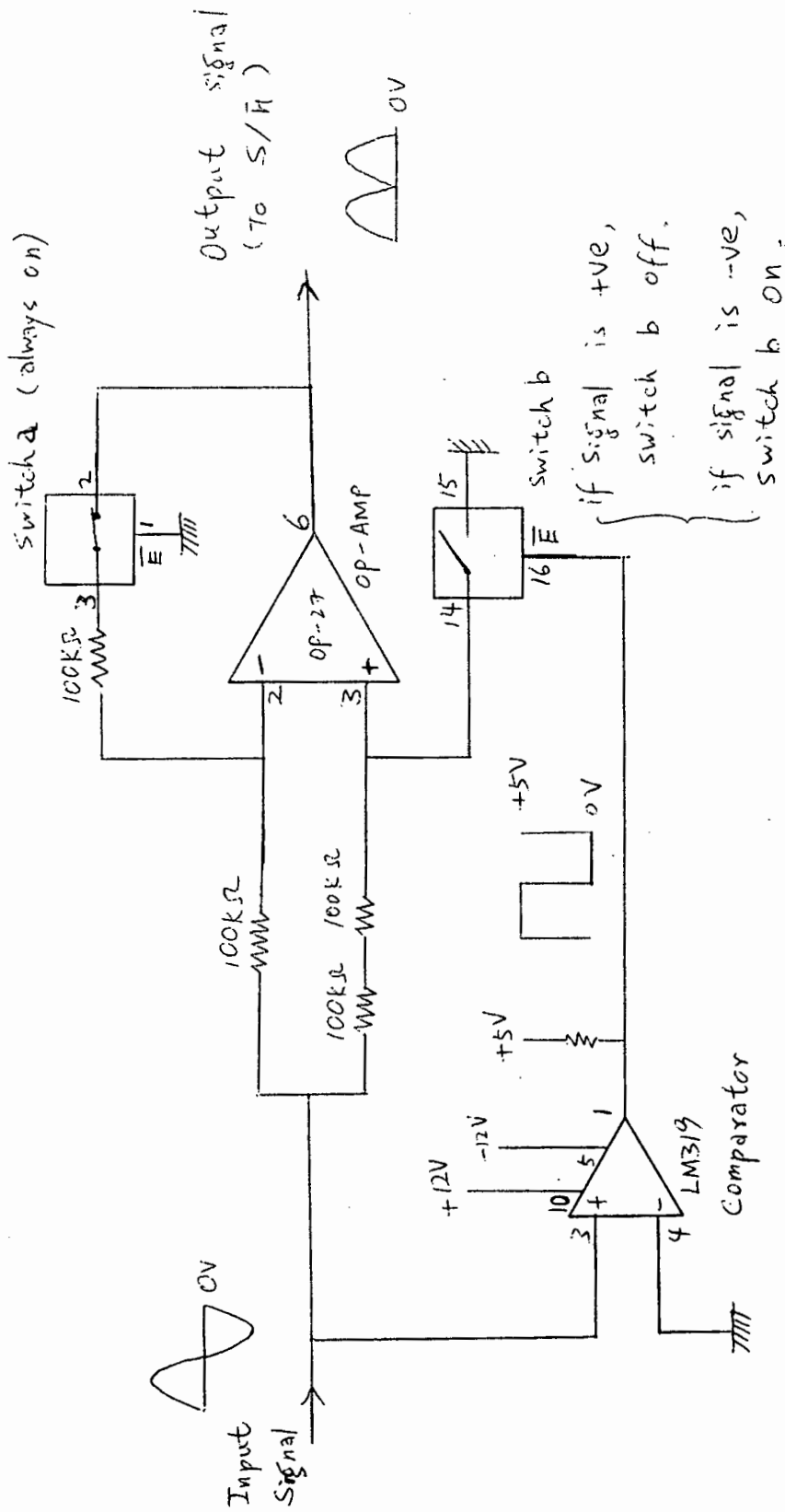


Fig. 4.18 Rectifier circuit

Thus, depending on the sign-bit, the input signal is modulated in software, which is faster than the traditional hardware modulator.

4-2-7. Part 6 Microprocessor unit.

The microprocessor is the central unit of the system. It links all other units of the system through its data, address and control lines. The microprocessor unit includes input-output ports, memory and control logic.

In order to facilitate the arithmetic processing, eliminate the requirements for writing long software routines and accelerate the measuring time, a hardware numerical processor is desirable. Owing to the economic factor, some algorithms for arithmetic processing has to be developed instead.

The Intel chip 8088 was used as the microprocessor unit of the system because of the microprocessor development facilities for the Intel 8088 available. The Intel MDS III computer, the IBM PC with Microsoft Assembler and the PDP-11 with an 8086 Cross Assembler are good examples.

The Intel functions of the 8088 processor are quite different from its predecessor, the 8085, and circuits designed for the 8085 would not be compatible to the 8088 system. The 8088 has an instruction stream queuing mechanism which is lacking in the 8085. This queuing mechanism allows the 8088 efficient use of bus bandwidth. Whenever there is space for at least 2 bytes in the queue, the bus interface unit of the processor will

attempt a word fetch memory cycle. This greatly reduces dead time on the memory bus. The queue acts as a first-in-first-out buffer, from which the execution unit executes instruction bytes as required. Because of the presence of the queuing mechanism, the address lines of the microprocessor are always busy. This is the most important key point for designing the peripheral interfacing circuits of the 8088.

The $\overline{\text{cs}}$ lines of the memory and peripherals, including the timer, the ADC and the instrumentation interface controller, come from the address bus. $\overline{\text{cs}}$ lines can stay active until very late in the bus cycle, resulting in bus contention elsewhere in the system. A new chip-select ($\overline{\text{NCS}}$) signal needs to be generated, starting at the falling edge of the address latch enable (ALE) control signal of the processor and terminating when either the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ control signal goes high. This could easily be implemented with one DET FF.

When the input or output instruction of I/O port is executed by the microprocessor, signal $\overline{\text{S2}}$ becomes active. The inverted $\overline{\text{S2}}$ together with the falling edge of the ALE causes the DET FF to generate the falling edge of $\overline{\text{NCS}}$ of peripherals.

Fig. 4.19 shows the new chip select circuit of peripherals and its timing.

Referring to Fig. 4.19, whenever the $\overline{\text{S2}}$ signal is activated, the present cycle accesses an input or output port. The new chip select ($\overline{\text{NCS}}$) signal determines the active period of the decoder 74LS138. Address lines A5, A6 and A7 decide which

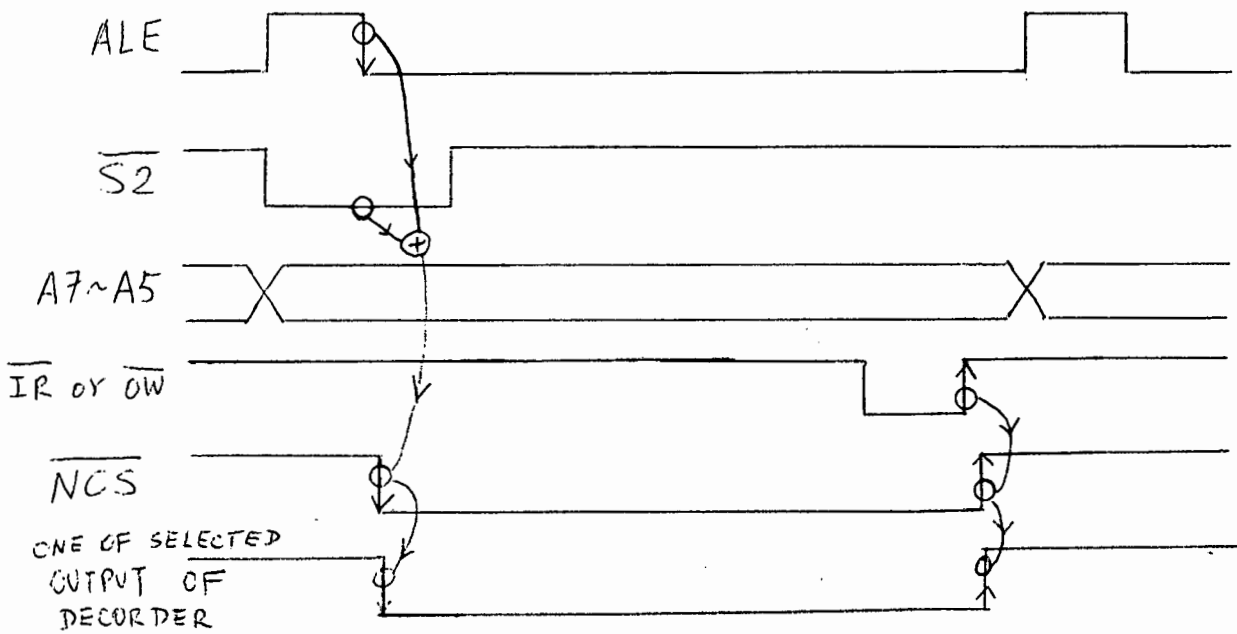
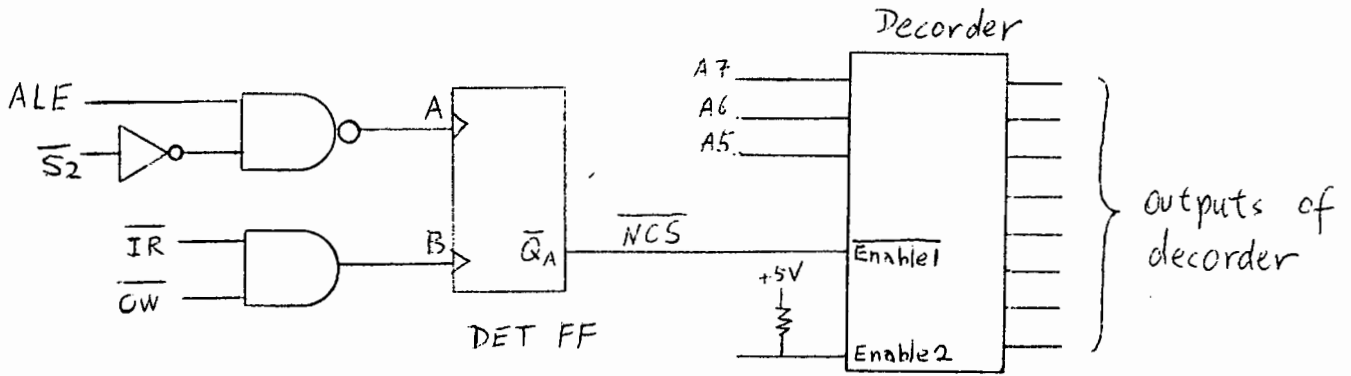


Fig. 4.19

New chip select (\overline{NCS}) circuit of non-memory peripherals and its timing diagram.

one of the eight output lines of the decoder which has same duration as $\overline{\text{NCS}}$, is to be active. Table 4.1 shows the address of each new chip select line and which chip is activated by the $\overline{\text{NCS}}$ line.

Fig. 4.20 shows the new chip select of the erasable programmable read only memory (EPROM) and the timing diagram. The EPROM can be addressed from 0FC000H up to 0FFFFFFH, 16K bytes altogether.

Address	new chip select
0E0H to 0FFH	HPIB talker and listener
0C0H to 0DFH	LED and Multiplexer
0A0H to 0BFH	ADC
80H to 9FH	1. Manual switches 1 to 5 decide the maximum order of harmonic to be measured (maximum up to 25th) . 2: Zero-crossing signal
60H to 7FH	Programmable interval timer.
40H to 5FH	Modulating clocks selector.
20H to 3FH	Synchronizing signal for modulating clock.

Table 4.1 Address of each new chip select.

Fig. 4.21 shows the new chip select circuit of random access memory (RAM) and its timing diagram. The RAM can be addressed from 0000H up to 1FFFH; 8K bytes space altogether.

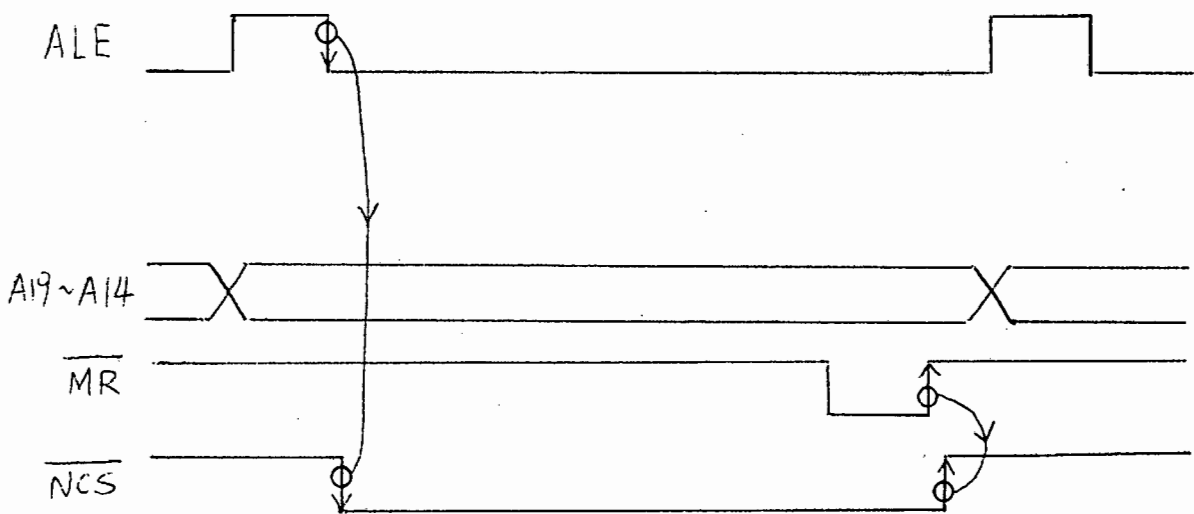
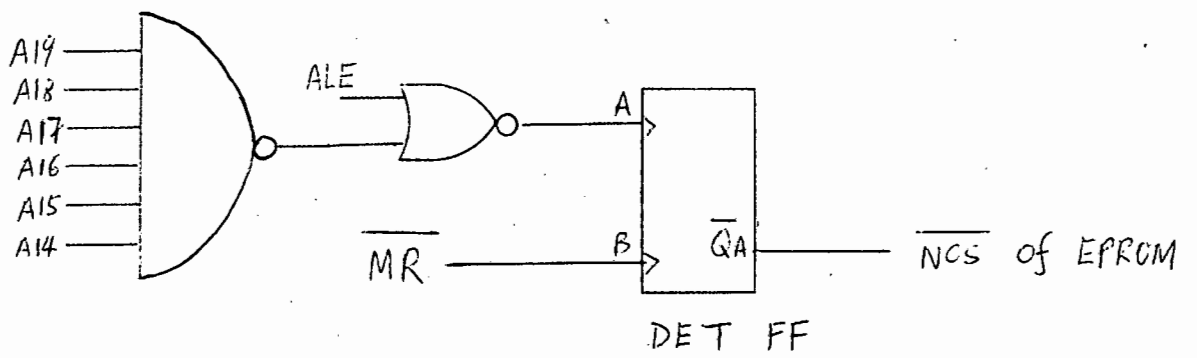


Fig 4.20 New chip select circuit of EPROM and its timing diagram

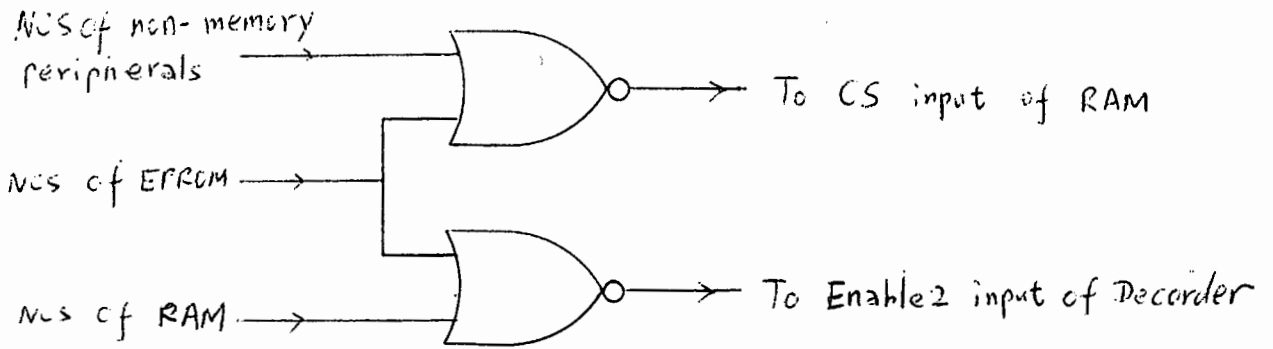


Fig. 4.22 Circuit secures New chip select signals

This signal can be generated with the circuit of Fig. 4.23 .
MC68488 also has R/\bar{W} signal line. This signal can be implemented with the circuit of Fig. 4.24 .
According to the specification of the 8088, \bar{IR} and \bar{OW} only last minimumly for 325 ns. On the other hand, the E signal must have a minimum duration of 450 ns. Therefore a wait state generator for the 8088 is needed in order to lengthen the E signal to more than 450 ns duration. Since one wait state can only generate 100 ns extra time, which does not match the specification of the MC68488, a triple wait state generator is employed. Fig. 4.25 and Fig. 4.26 show the triple wait state generator and its timing and state diagrams respectively.
Referring to Fig. 4.26, the system's $\bar{\text{WAIT}}$ line is driven low whenever a device requiring three wait states is selected. The flip-flops are cleared when either $\bar{\text{ALE}}$ or the $\bar{\text{CS}}$ of the GPIA is high, forcing system $\bar{\text{wait}}$ line high, which is connected to the RDY1 line of the system clock generator 8284.
If no wait state is required, the flip-flops do not change. If a wait state is required, the CLR pins of the flip-flops are released and the output of the generator toggles on the falling edge of the system clock at the beginning of T2 to force three wait states according to the state diagram of outputs Q1 and Q2 of FF1 and FF2 (Fig. 4.26) . After 3 wait states, the $\bar{\text{WAIT}}$ signal is removed, indicating readiness and allowing the completion of the bus cycle. Further changes in the state of the flip flop will not affect the bus cycle. The circuit allows approximately 600 ns for the chip to select, decode and

from 8088 to MC 68488

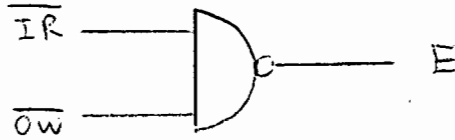


Fig 4.23 E signal circuit

from 8088 to MC 68488

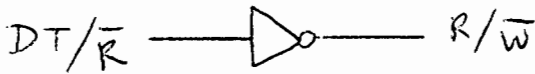


Fig. 4.24 R/\overline{W} signal circuit

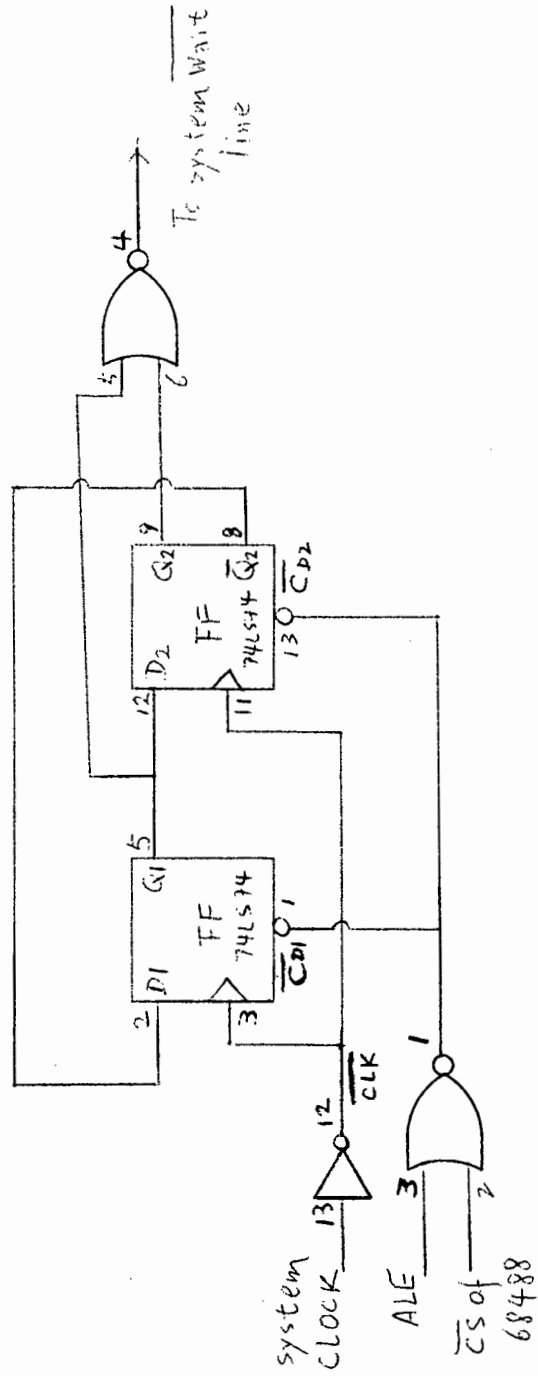
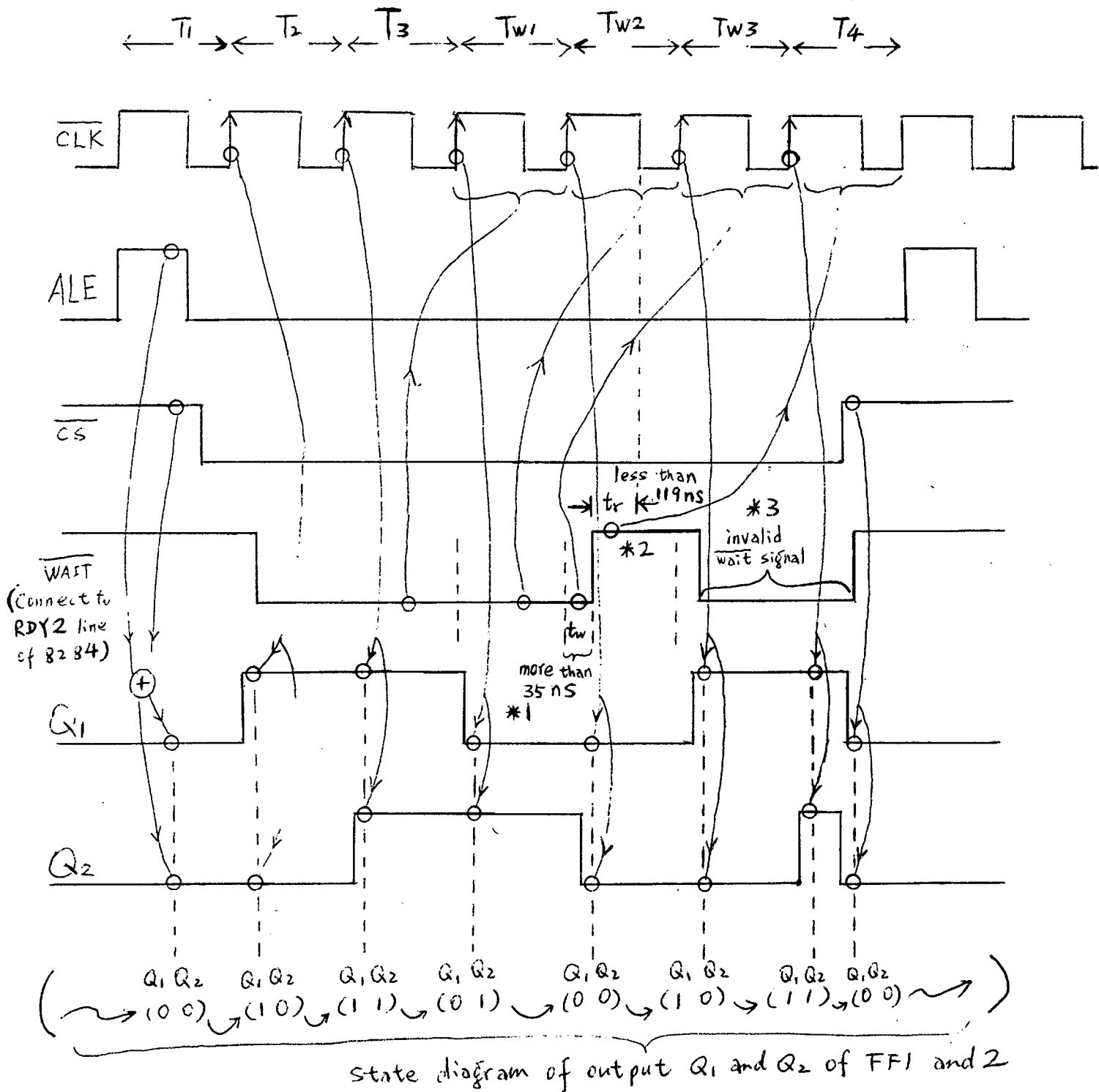


Fig. 4.25 Circuitry of Triple Wait - state Generator



According to the Specification of 8284 :

- *1. One wait state T_{w3} sets up because $t_w > 35 \text{ ns}$.
- *2. T_4 cannot be issued after T_{w2} because of $t_w > 35 \text{ ns}$ and $t_r < 119 \text{ ns}$, instead T_4 is issued after T_{w3} .
- *3. This wait signal is invalid and ignored by 8284 because it is not issued by the end of T_2 or start of T_3 .

Fig. 4.26

Timing and state diagrams of

Triple Wait - State Generator

condition the system's ready signal.

4-2-9. Part B Microcomputer.

The purpose of using a microcomputer (HF 85) is mostly for scaling the raw results and expressing them in *symmetrical components*, then to utilize its screen and printer to display the results. It is also used as a controller to control other potential instruments running in parallel with the system by means of its instrumentation interface.

4-2-10. Overall operation.

Finally, consider the overall action of the system. After passing through the scaling circuit, the input signal from V_a goes into the reference clock generator. The reference clock generator recovers the fundamental of the input signal in the form of a clean and well defined rectangular wave. This signal is then fed to the input port of the microprocessor. The microprocessor always polls the input-port to see whether the input rectangular wave changes from a low state to a high state. If this happens, the microprocessor immediately sends out a signal from its output port to the modulating clock generators in order to synchronize the reference clock. There will be a phase shift between the reference clock and modulating clock, caused by the time gap between the time when the microprocessor catches the change of state of reference clock and when the

microprocessor issues a synchronizing signal. This phase shift will be negligible if the polling frequency of the microprocessor is very much higher than the frequency of the reference clock. The modulating clock signal feeds the sign-bit modulator and modulates one of the six input channels of the analogue multiplexer which is selected by the microprocessor cyclically, in order to generate the sign-bit for the ADC. The output of the buffered multiplexer is fed to the sample and hold device and then the ADC. The sample and hold samples the input analogue signal at a specified time and then holds this value until it takes the next sample point. The ADC converts the analogue values held in the sample and hold into digital code and then feeds it to the input port of the microprocessor. The microprocessor fetches the data from the ADC and then processes it according to the program stored in the memory. The microprocessor deals with each input channel for one cycle of ~~fundamental period~~ time and then switches to the next channel until all six channels have been served. After serving all six input channels, the microprocessor continues to calculate all the required data and then passes it to the instrumentation interface. The microcomputer picks up the data from the instrumentation interface and then multiplies it by the scaling factors and expresses it in *symmetrical components*. It then transfers the data to its display unit or uses it for other purposes.

4-2-11. SH-64 Bus.

Because many electronics components are incorporated in the system, it was impossible to fit all the components on one card. The SH-64 bus was utilized to help the distribution of the components onto several cards. The assignment of the function of every line is shown in Appendix [A]. One of the most fatal disadvantages of the SH-64 bus is its backplane which has undershoot and ringing transients. All the wires in the backplane behave as transmission lines, in which unwanted transients exist.

Several attempts were made to eliminate these transients and the following conclusions obtained.

1. All the input and output lines of each card have to be secured by the drivers or buffers.
2. The 74ALS or 74F series of TTL drivers and buffers are highly recommended, because the 74ALS and 74F series IC's outputs include clamping diodes to limit undershoot and control ringing on long signal lines. As with the input diode clamps, these diodes are intended for transient suppression [35] .
3. Deploy active terminators at both ends of the backplane.

4-2-12. Layout of circuitry.

The system has been constructed using a modular approach. Each module resides on a standard Eurocard, 100 mm by 220 mm. These

cards then plug into an SH-64 backplane using a rack mounting system . There are three cards in the system: Card A, Card B and Card C.

Card A contains all analogue circuits and the ADC .

Card B contains the microprocessor, memory, counter and control circuits.

Card C contains the IEEE-488 interface and digital phase shifter circuits.

These individual circuit diagrams are appended in Appendix B.

CHAPTER FIVE

It is important to note that probably no large operating system using current design technology can withstand a determined and well-coordinated attack, and that most such documented penetrations have been remarkably easy.

B. Hebbard et al.

It is necessary to point out that there is almost no writings composed in non-parent language of the author which is not subject to criticism if any defect therein is purposively sought.

Kwan Leung Shum

5 SOFTWARE

5-1. The procedure of developing an operating system for the instrument .

The operating system of the instrument was developed using the editing, assembling and in-circuit emulation facilities of Intel's Microprocessor Development Series III System (MDS-III) . This system allows easy and rapid development and debugging of assembly language (ASM 86) programs, the language used for writing the operating system of the instrument . Each routine is created as a file using the editor called "Alter" of the MDS-III . The editor creates what is known as a source code, which must then be assembled by ASSEMBLER_86 to form the microprocessor compatible machine code of 8088. The MDS_III linker program called "LINK 86" is then use to link all the routines together without assigning absolute addresses. All the routines are now specified at relocatable addresses and are ready to be debugged using the in-circuit- emulator (ICE_86) facilities. These are particularly powerful facilities which allow users to trace the execution of a program, thus allowing programming errors to be located and corrected. Perhaps more important is that this can be done using combination of the MDS-III hardware features and/or the hardware of the instrument being developed. Thus the software can be initially tested using MDS-III hardware only. As more of the system hardware is developed, so it is incorporated into the test

procedure, thereby ensuring that all testing and debugging is carried out on a unit as close to the final product as possible. After the debugging procedure, a system program of the MDS-III called "LOC 86" is employed to locate the software at absolute addresses. Another system program of MDS_III called "OH 86" is used to convert the binary absolute object module into Intel's standard hexadecimal format. This hexadecimal file is then transferred to the host computer (PDP-11/23). Unfortunately, the Intel's standard hexadecimal format is not used by the EPROM programmer, which is connected to the PDP-11/23. Therefore, a system program on the PDP-11/23 called "CON" is used to convert it into compatible form. The final step is to down-load the compatible hexadecimal code developed in PDP-11/23 to the EPROM programmer and program the code into the EPROM.

5-2. The operating system.

The operating system controls all the functions of the harmonic analyser. There are two diagrams of concern. The first is Fig. 5.1 which is the flowchart outlining the operating system. Fig. 5.2 shows the priority of the various procedures and nesting procedures and where they fit into the overall operating system and the sequence in which they are called.

The program listing of the operating system in the Appendix C includes comments for the purpose of demonstrating the function of each section of the code.

It must be stressed that the software currently used was composed

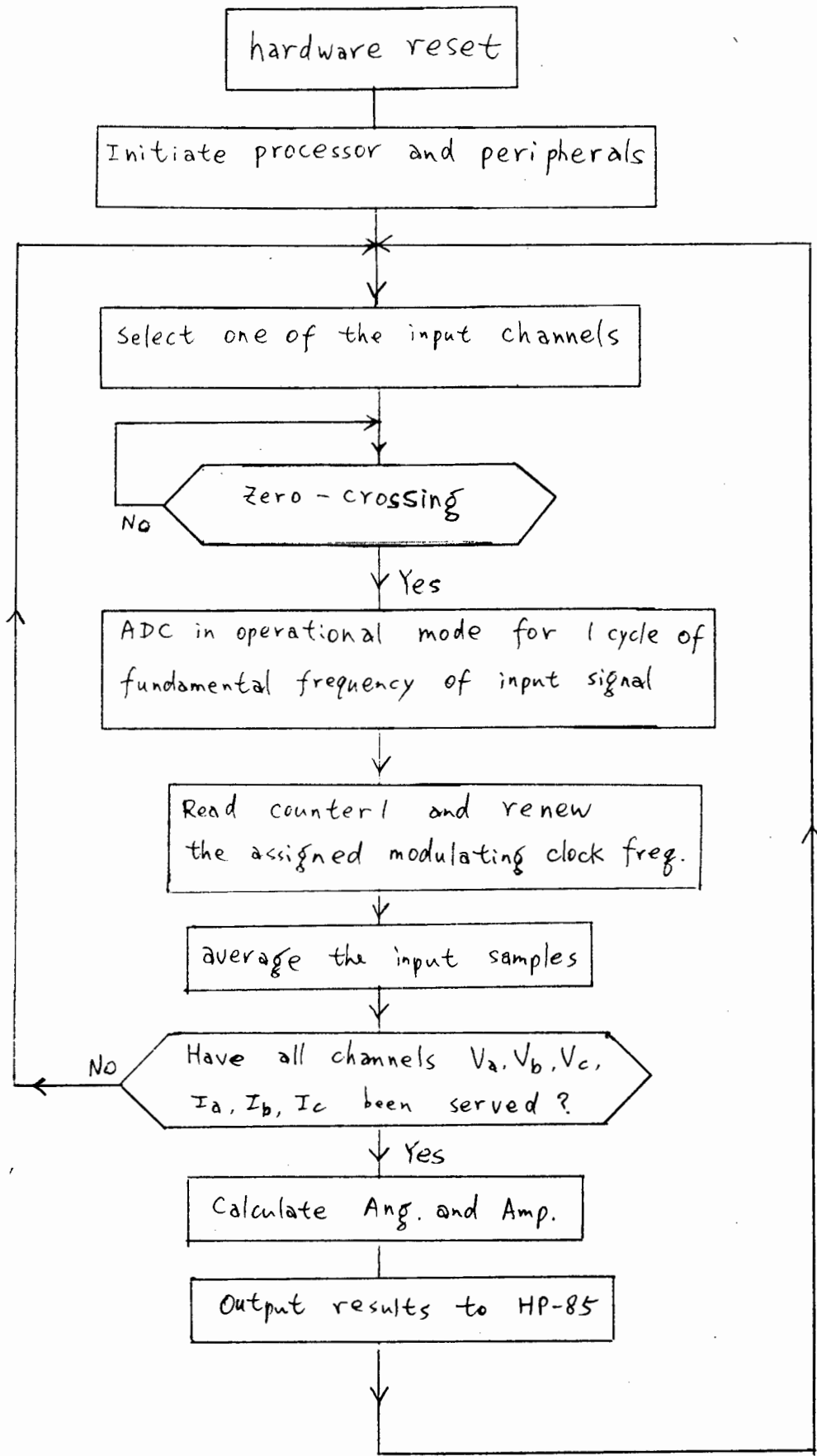


Fig 5.1 Flowchart of the operating system.

BEGIN	MOD_CLK_SYN MOD_CLK_UPDATE DUMMY_READ	ZC_ADC MOD_CLK_UPDATE_1
	ZC_ADC MOD_CLK_UPDATE_1 AVERAGING	LED
	ZC_ADC MOD_CLK_UPDATE_1 AVERAGING MOD_CLK_UPDATE_1 THREE_7_8	
	THREE_7_7	DEHA
	THREE_7_6	DEHA
	THREE_7_5	DEHA
	THREE_7_4	DEHA
	THREE_7_3	DEHA
	THREE_7_2	DEHA
	THREE_7_1	DEHA
	DIV_32 SROOT	QUE QUE
	DIV_32 FANG GPIB GPIB GPIB1	

Fig. 5.2 Order of Execution of the Procedure of Operating System.
(Read from the left and down).

with the objective of achieving maximum speed because real-time signal processing speed is required.

5-2-1. Initialization.

The operating system was divided into 8 parts, Part 0 to Part 7. Part 0 consists of the "SAMP" segment, "ATCS" segment and "STACK_SEG" segment.

The "SAMP" segment sets up the storage area for the temporary data and scratch pad registers.

The "ATCS" segment stores the whole arc_cosine look_up table.

The "STACK_SEG" segment preserves the memory space for the system stack.

5-2-2. The operation of the software.

Following a hardware reset program, which is inside the "RES" segment located at the end of the program, execution is transferred to the "BEGIN" procedure. The "BEGIN" is the main procedure which is divided into seven parts, parts 1 to 7.

<1> Part 1 starts the code segment and defines the addresses of all the I/O ports, and initialises all the segment registers and stacks.

<2> In Part 2 the microprocessor turns off the overflow LED and selects channel 6 which accesses Va as the first channel to be processed. Counter 0 and counter 1 are then initialised. It selects the 0_deg. phase modulating clock to modulate the input signal. The microprocessor then reads the external switch port

"SWF" , which must be set manually before the program commences in order to determine the maximum order of harmonics (from 1 to 25) to be measured. Counter 0 of the chip 8254 provides the modulating clock to the sign-bit modulator. This is initially set to 50 Hz. Once the measuring process starts the counter assigned frequency is updated to a new harmonic frequency before the microprocessor commences to process the new channel during the measurement.

Procedure "MOD_CLK_SYN" is then called. This procedure polls the ZC port until the fundamental filtered zero_crossing (ZC) signal is detected. When this is completed it synchronizes the modulating clock by resetting counter 0.

Procedure "MOD_CLK_UPDATE" is now called and polls the ZC port until the ZC signal is again detected (i.e. one fundamental cycle later) .

The value of counter 1 is read. This value is decremented until one fundamental cycle has passed. This value is used to update counter 0, which generates the modulating clock.

Procedure "DUMMY_READ" is now executed; this is a pilot procedure which leads the ADC into the normal operation. The channel pointer (R6) is initialised with channel 6 which accesses Va.

The microprocessor now calls procedure "ZC_ADC" with a zero degree phase shift modulating clock. This procedure lets the CPU first poll the ZC port until the rising edge of ZC signal is detected after which the analogue-to-digital convertor (ADC) starts converting the analogue signal into the digital form. The microprocessor stores the samples in the memory for one

period of the zero_crossing signal, and then checks each sample to determine whether its value is out of the 0 to 5V range. If it is, the CPU lights the LED to show the overflow status of the input signal. While checking overflow operation, the CPU also modulates each sample according to its sign_bit, D15, which comes from the sign_bit modulator. If the D15 contains "0", the CPU will not change the sample, which means the sample is multiplied by one. If the D15 contains "1", the CPU will convert the sample into 2's complement form, which means the sample is multiplied by negative one. After modulating all samples, the CPU sums them up and then averages them by dividing the summation value with the total number of samples involved in the summation. After averaging, the mean level values of output ${}_0U_k$ and ${}_{90}U_k$ are obtained. The ${}_0U_k$ and ${}_{90}U_k$ are obtained by modulating at 0_ and 90_ degree phase shift reference clock respectively. The ${}_0U_k$ and ${}_{90}U_k$ are then stored at address XY in memory.

The ADC does have offset error which must be eliminated by the following procedure :

Let P_i be the absolute value of sample with +ve sign-bit .

Let Q_j be the absolute value of sample with -ve sign-bit .

Let R_i and R_j be the absolute values of offset error of the ADC,

$$i = 1, 2, \dots, M$$

$$j = 1, 2, \dots, N$$

$$k = i + j$$

where k is the total number of input samples in one fundamental period.

Take approximation, R_i or $R_j = R$ which will be equal to the minimum absolute value of samples, i.e., $R = \text{Min} (P_i \text{ or } Q_j)$.

$$\begin{aligned} \text{Sum of samples} &= \text{Summation } [(+P_i + R_i)] + \text{Summation } [(-Q_j - R_j)] \\ &= \text{Summation } [P_i] - \text{Summation } [Q_j] + (M-N)*R \end{aligned}$$

Therefore,

$$\text{Summation } [P_i] + \text{Summation } [Q_j] = \text{Sum of samples} - (M-N)*R$$

where $(M-N)$ is the difference of the number of samples with +ve and -ve sign bit.

Procedure "MOD_CLK_UPDATE_1" is called and counter 0 generates modulating clock with its assigned harmonic frequency. This assigned frequency is stored in register R14. The microprocessor chooses the 90_deg. phase shift modulating clock before modulating the input signal so that the modulating clock can have longer time to stabilise.

Procedure "AVERAGING" is called and checks for overflow of input signal and modulates samples with gain +1 or -1 according to sign-bit. It also eliminates the offset error according to the method described above in the "ZC_ADC" .

Procedures "ZC_ADC" and "MOD_CLK_UPDATE_1" are again called but at a 90_deg. phase shift modulating clock. The next channel (i.e. channel 5) is then selected.

Procedure "AVERAGING" is again called to process those samples derived at the 90_deg. phase modulating clock.

The whole cycle is then repeated. This cycle is repeated for each channel (channel 6 down to channel 1, each with two sets of data, one at 0_degree and the other 90_degree phase shift

modulating clock) .

After all six channels have been accessed the contents of register R14 is decreased by one. It is then checked to see if it is zero. If not, the cycle is repeated using the new harmonic frequency. If it is zero then Part 3 is started.

<3> Part 3 processes equation set (3.7) and is programmed to calculate D.C. terms of $2U_k \cos \theta_k / k(p+1)\pi$ and $2U_k \sin \theta_k / k(p+1)\pi$ in equation (3.7) based on the method described in the section (3-2-3) . Equation (3-7-6) to (3-7-8) each have two D.C. terms. The 2nd term arising from the higher harmonics can be eliminated by dividing equation equations (3.7.18), (3.7.21) and (3.7.24) by a factor of 3 and then subtracting them from equations (3.7.6) to (3.7.8) respectively. By repeating the same procedure, those D.C. terms which exist in equation (3.7.1) to (3.7.5) can be eliminated.

The D.C. terms are stored in memory in the following order :

($0V_{ak}$ $90V_{ak}$
 $0V_{bk}$ $90V_{bk}$
 $0V_{ck}$ $90V_{ck}$
 $0I_{ak}$ $90I_{ak}$
 $0I_{bk}$ $90I_{bk}$
 $0I_{ck}$ $90I_{ck}$)

where subscript k is the order of the harmonic.

The values of D.C. terms are stored in memory, starting with those related to the fundamental and going up to those related to the highest harmonic.

According to the above data structure, each set of values related

to a particular harmonic occupies 12 words (or 24 bytes). This means that the starting address offset of each set of data related to a particular harmonic is a multiple of 24.

Part 3 processes 8 procedures, namely procedure "THREE_7_8" down to "THREE_7_1".

Procedure "THREE_7_8" begins by initializing the starting environment for calculating equation (3.7.8). The microprocessor first reads the switch port (SWP) to determine the maximum order of harmonic that needs to be measured.

If the order of the harmonic is less than or equal to 23, the procedure terminates and returns to the main routine. If it is greater than 23, a factor 3 is stored in register R6. Thereafter the routine DEHA is called and executes the following procedure:

It retrieves the set $(U_{24} \quad U_{24})$ and divides it by the content of R6, which is 3. It then subtracts the result from set $(U_8 \quad U_8)$. The new set of results is $2U_8 \cos \theta_8 / \pi$ and $2U_8 \sin \theta_8 / \pi$. This set is stored back in $(U_8 \quad U_8)$. All the results are expressed in the two's complement form.

Procedures "THREE_7_7" down to "THREE_7_1" operate on the same basis, each using a different set of data, a different dividing factor stored in R6 and a different address pointer according to equation set (3.7).

<4> Part 4 calculates the average input fundamental frequency of 6 channels based on the first 12 input values from counter 1, which are stored in the memory location "ZCC" using the following equation:

FREQ * 10 = 10*12*2.5E6 / SUM [ZCC] ,

where 2.5 is the operational frequency of counter 1 in MHz , 10 a scaling factor and SUM [ZCC] the summation of the first 12 input values.

<5> Part 5 calculates $A_k = \sqrt{X_k^2 + Y_k^2}$ and
 $\theta_k = \text{ARC_COS} (X_k/A_k)$.

It also calculates the quadrant of θ_k according to Fig. 3.4 .

It uses procedure "DIV_32" , which is a 32_bit by 32_bit division procedure, using the subtract_and_test method.

Another procedure involved is "SROOT" which has a nesting procedure called "QUE" . "SROOT" calculates the square root of a 32_bit binary number involved in the calculation of

$\sqrt{X_k^2 + Y_k^2}$. The algorithm of calculating square roots is from an old Chinese formula which is expressed in verse form for decimal numbers modified for binary numbers.

It first divides the 32_bit number into two groups of 16_bit each. The procedure called "QUE" calculates both the most and the least significant words of the data. The result of a square root of a 32_bit number is 16_bit .

After "SROOT" is completed, "DIV_32" is called to work out X_k/A_k . Procedure "FANG" is called to determine the absolute value of θ_k in binary form. The arc_cosine value (or θ_k) is contained in the DI register. The angle determined is only in the range 0 to 90 degree with scaling factor 10, that is, 0 to 900. Its quadrant has to be established by other procedures. This procedure uses fast searching method to determine the angle from the looking_up table defined in the "ATCS" segment. The

accuracy (resolution) of this look_up table is 0.2 degree. The speed of this procedure using a look_up table in conjunction with a searching technique is much faster than numerical processors.

The quadrant of θ_k is determined from the sign of X_k and Y_k according to Fig. (3.4). θ_k is based on the fundamental scale. On the harmonic scale, $\theta_k = K * \theta_k$. It is important to note that θ_k is always checked and adjusted to an angle between 0 and 360 degree.

<6> Part 6 chooses the angle of the fundamental component of V_a as the reference. All angles of the harmonic components, which are sets of data, refer to it. If any angle is larger than 360 degree the microprocessor adjusts the angle to the range of 0 to 360 degree.

<7> Part 7 transfers amplitudes and angles of V_k and I_k from the fundamental up to the assigned harmonic order (maximum 25), to the GPIB bus. The interface address of this instrument is arbitrarily assigned as 9. Procedures "GPIB" and "GPIB1" are called three times in total to transfer three types and sets of data: (1) total number of data that needs to be transferred, (2) fundamental frequency and (3) amplitudes and angles, to the GPIB interface. The GPIB is one of the most complex interface systems. To describe its operation is beyond the scope of this thesis. To understand this routine one needs to consult the data sheet of MC68488 and IEEE_488 bus specification. The whole program will be repeated after the data has been transferred to the interface.

5-3. Software of the microcomputer.

A program called "H7" written in the Basic language runs on an HP85 microcomputer for scaling the raw data of harmonic components from the HPIB, expressing them in symmetrical components and calculating the rms values of output voltage and current of the 3 phases. Fig. 5.3 shows the flowchart of the program. The program listing is appended in Appendix D.

The program first polls the HPIB until it is ready for transferring data. The raw data is then received from the HPIB. The microcomputer then scales the data to obtain the resultant harmonic components of amplitude and angle. After scaling, the resultant components will be printed. Thereafter, the resultant components are relocated in the memory to create the initial circumstances for calculation of symmetrical components (\bar{U}_0 , \bar{U}_+ and \bar{U}_-) of each harmonic voltage and current. According to Fortesque's theory [13], \bar{U}_0 , \bar{U}_+ and \bar{U}_- can be calculated as follows :

$$\bar{U}_0 = (\bar{U}_a + \bar{U}_b + \bar{U}_c) / 3$$

$$\bar{U}_+ = (\bar{U}_a + a \bar{U}_b + a^2 \bar{U}_c) / 3$$

$$\bar{U}_- = (\bar{U}_a + a^2 \bar{U}_b + a \bar{U}_c) / 3$$

or,

$$\bar{U}_0 = ([U_a \cos \theta_a + U_b \cos (\theta_b) + U_c \cos (\theta_c)] + j [U_a \sin \theta_a + U_b \sin (\theta_b) + U_c \sin (\theta_c)]) / 3$$

$$\bar{U}_+ = ([U_a \cos \theta_a + U_b \cos (120+\theta_b) + U_c \cos (240+\theta_c)] + j [U_a \sin \theta_a + U_b \sin (120+\theta_b) + U_c \sin (240+\theta_c)]) / 3$$

$$\bar{U}_- = ([U_a \cos \theta_a + U_b \cos (240+\theta_b) + U_c \cos (120+\theta_c)] + j [U_a \sin \theta_a + U_b \sin (240+\theta_b) + U_c \sin (120+\theta_c)]) / 3$$

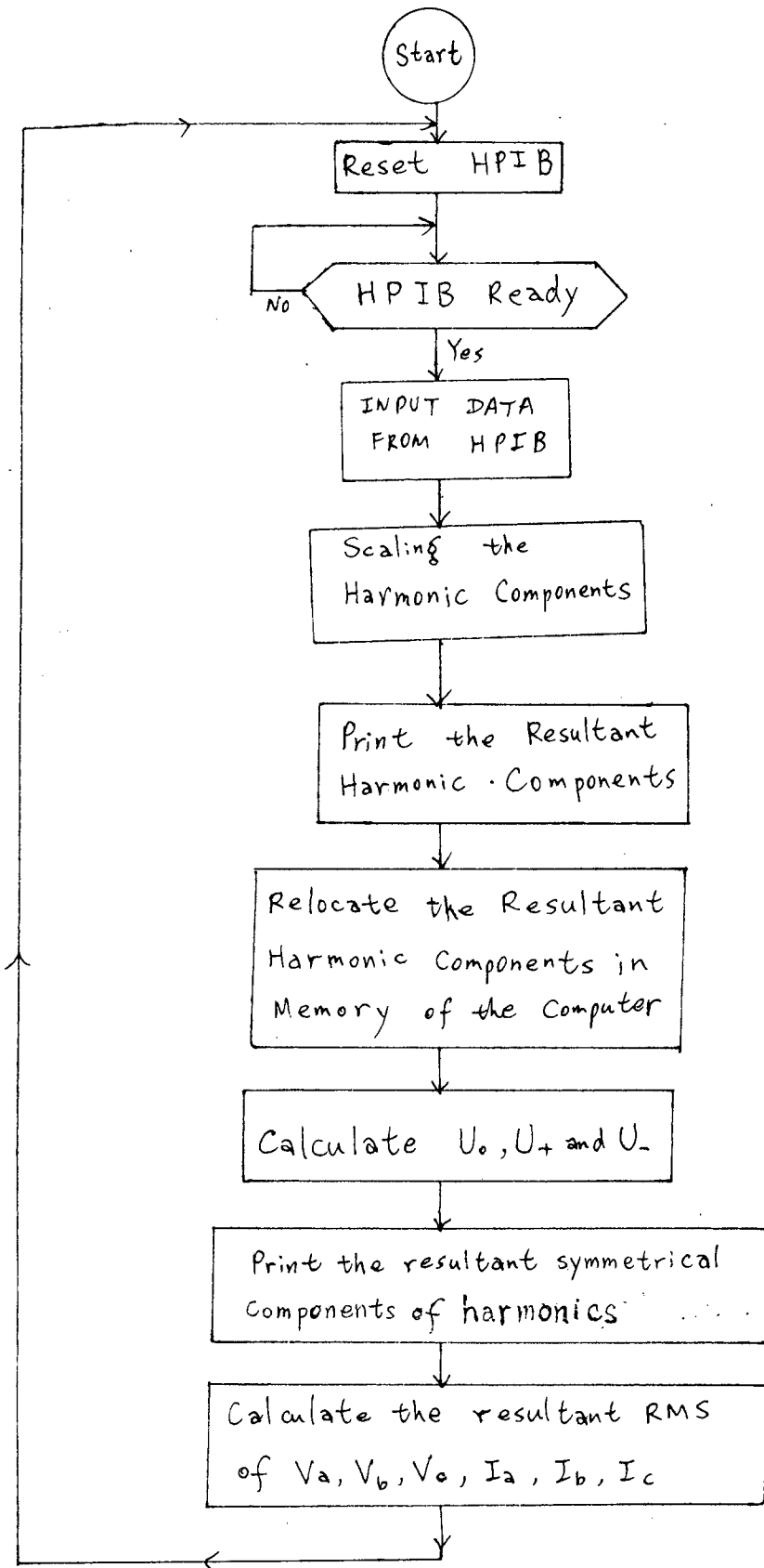


Fig. 5.3 Flowchart of Program "H7".

Referring to the above formula, \bar{U}_a , \bar{U}_b and \bar{U}_c are to be considered as sinusoidal steady state and are expressed in notation of the phase voltage or current of three phase systems. Define $\bar{U}_i = U_i \angle \theta_i$, where i can be a , b or c . \bar{U}_0 , \bar{U}_+ and \bar{U}_- are zero, positive and negative sequence components respectively. The last step of the program is to calculate and print the resultant rms values of V_a , V_b , V_c , I_a , I_b and I_c in order to compare them to readings from the analogue meters.

CHAPTER SIX

Nothing ever becomes real till it is experienced _____ even a
proverb is no proverb to you till your life has illustrated it.

John Keats

6 RESULTS

The success of a new instrument depends on its ability to measure a given value more accurately, more simply, more cheaply and with more versatility than is allowed by existing equipments. Thus the testing and evaluation is as important as the design and construction of a new instrument.

6-1. Testing Apparatus.

The apparatus employed to evaluate the performance of the harmonic analyser are as follows :

- (1) A set-up of three phase synchronous rotating harmonic generators manufactured by the Mawdsley's Ltd., England.
- (2) Three sets of CTs (JIS C1731, Type 2243, Rated Accuracy 0.1%) manufactured by the Yokogawa Electric Works Ltd., Japan.
- (3) Three sets of Voltmeters and Ammeters (Type 2013, Class 0.5) manufactured by the same company as the CTs.
- (4) One Digital Storage Oscilloscope.
- (5) One X-Y Plotter.
- (6) Three sets of adjustable Resistive Loads.
- (7) One Current Probe.

Further details about the characteristics of the above apparatus can be obtained by consulting the specification sheets of their manufacturers.

6-2. Preparation of Testing Apparatus.

The following matters have to prepare for the testing :

(1) Firstly all the meters used in test were calibrated and a range on them has been selected to give a ~~maximum~~ deflection in order to obtain a more accurate and reliable reference for measurement.

(2) The connecting leads between the analyser and the CT were made as short as possible so as to avoid excessive unwanted pickup.

(3) One of the input channels of a digital storage oscilloscope was utilized to monitor the output voltage waveform of phase A.

(4) A current probe was connected to the other channel of the oscilloscope to show the current waveform of phase A.

(5) The stored voltage and current waveforms were then plotted using an X-Y plotter.

(6) The readings from the analogue meters were the root mean square values of the tested waveforms. Each reading represents the summation of all the measured harmonics of each phase. This can be illustrated in the following equation :

$$U_{rms} = \sqrt{\frac{1}{T} \int_0^T [\sum H_k(t)]^2 dt}$$

where U_{rms} is the resultant root mean square (RMS) value of the voltage or current.

A software approach was adopted to calculate the resultant RMS values of V_a , V_b , V_c , I_a , I_b and I_c of all the harmonics from the memory of the microcomputer. These resultant values are used to compare the readings obtained from the analogue meters.

(7) The expression given by $[\sum \hat{U}_k \sin (KW_s t + \theta_k / K)]$ represents the tested waveform. Substituting the peak amplitudes (\hat{U}_k) and phase angles (θ_k) of harmonic components obtained from the analyser to the expression, the waveform could be reconstructed. This was accomplished using a programming technique to take the summation of the most significant harmonics of phase A, i.e. the fundamental, 3rd, 5th and 7th. The reconstructed individual and resultant waveforms of phase A were then utilized to compare the one recorded by the X-Y plotter.

6-3. Procedure of operating the harmonic analyser.

Procedure of operating the harmonic analyser is as follows :

- (1) Connect the voltages and currents inputs properly as in Fig. 6.1. Resistive loads A, B and C must be adjusted to match each other precisely to minimize unbalance amongst phases.
- (2) Using the manual switch inside the analyser to assign the maximum order (from 1 to 25) of the harmonic needed to be measured (in this measurement the switch is set to 7) and then turn on the analyser.
- (3) Switch on the HP85 and load the "H7" program from the tape.
- (4) Press the reset button on the front panel of the analyser.
- (5) Wait for 1 minute time and then press the RUN button on the keyboard of HP85.
- (6) The results will be shown in the screen or printer of HP85 automatically and continuously.
- (7) The operation can be stopped by pressing the reset key of HP85 together with the reset button of the analyser.

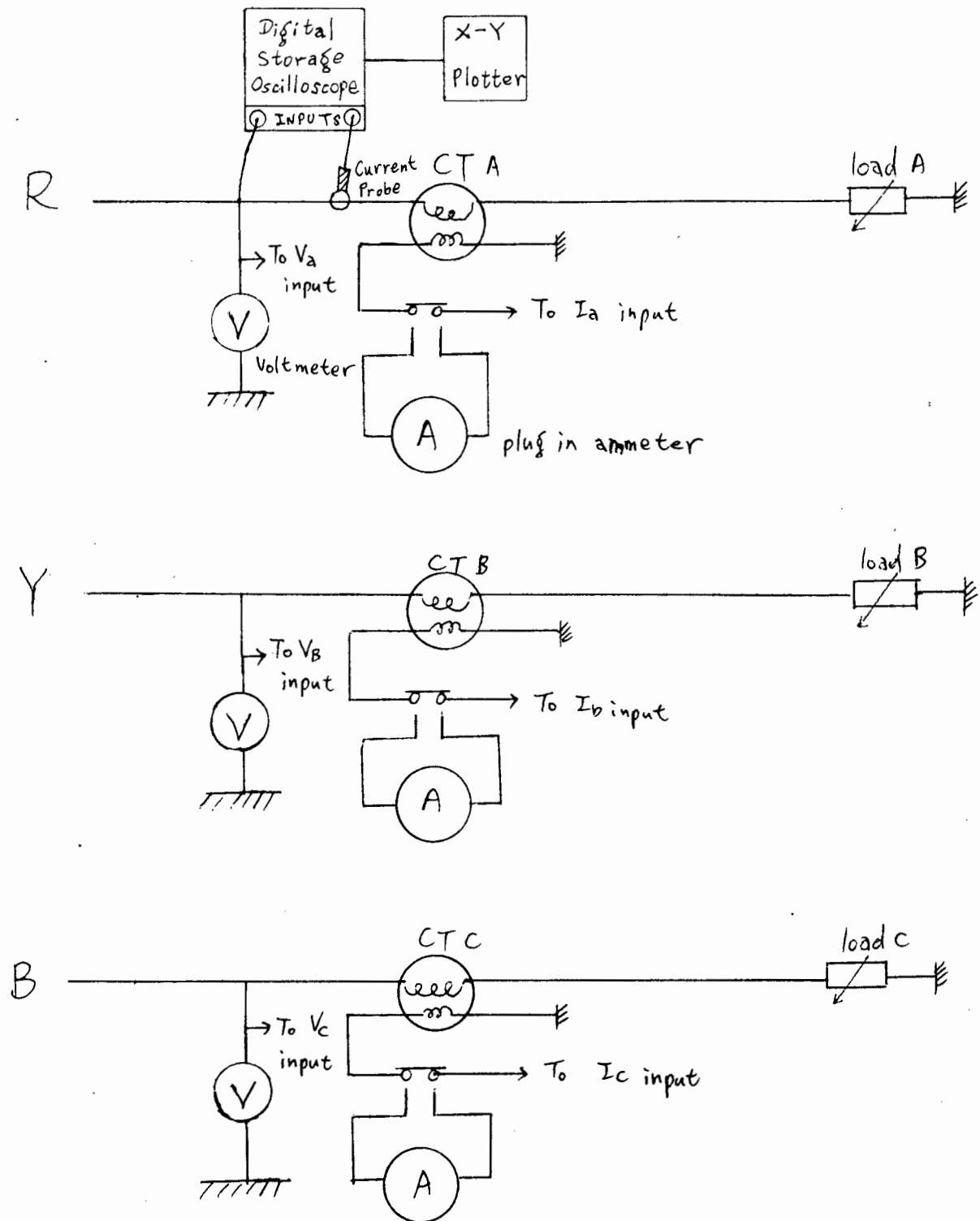


Fig. 6.1 Interface between the analyser and the supply.

6-4. Results of the tests.

Two sets of results each were recorded at different electrical angles for the following combinations of harmonics, which were generated by the harmonic generators.

- (1) 1st and 3rd (Test 1 and 2).
- (2) 1st and 5th (Test 3 and 4).
- (3) 1st and 7th (Test 5 and 6).
- (4) 1st, 3rd, 5th and 7th (Test 7 and 8).

An additional test (Test 9) was done to examine non-distorted waveforms with fundamental frequency in an unbalanced three phase power supply by decreasing the resistances of Load A, B and C in turn.

The results of the tests are appended in Appendix E to demonstrate the capability of the analyser.

6-5. Conclusion of the tests.

The various tests performed on the analyser show that the analyser does measure harmonic components in amplitude and angle correctly for voltage and current. Unfortunately the goals of high degree of precision and real time speed were not consummately achieved with this model, but some alterations could be made to enhance both accuracy and speed considerably.

Firstly with regard to the real time speed, this can be improved by adding more hardware into the measuring system. One analyser per channel would be ideal if the economic factor is not of concern.

Secondly with regard to accuracy, an attempt to explain the difference of readings between the analyser and the analogue meters has to be considered first :

(1) The readings taken from the reference meters are at a time later or earlier than that obtained from the analyser. This is because of the unavailability of the sophisticated controlling excitation circuitry to stabilize the generators. Hence, there must be some difference between the two readings.

(2) The analogue multiplexer in the input circuit of the analyser generates noise. This is caused by channel switching. It also has an inherent voltage and current offset error.

(3) The readings were taken by the analyser on each channel at least one fundamental period after the previous one, instead of taken simultaneously. This also causes error owing to frequency fluctuations of the signal from the generators at various measuring times.

(4) The performance of ADC is not as reliable as a commercial equivalent. The former device is more probably susceptible to error.

(5) The analogue meters and current transformers have nonlinear characteristics such as stray inductance, capacitance of windings and the frequency dependent core loss, which way also cause error.

(6) The harmonic generators have no scale to show the change of the electrical angle. This makes the measurement very inconvenient.

The way to eliminate the experimental errors is as follows :

{a} The errors owing to the instability of the rotating harmonic generators and the nonlinearity of analogue meters as in (1), (5) and (6) above can be eliminated by the employment of the electronic harmonic generators instead of the one used in the measurement as explained in section 1-7. The construction and design the electronic generators is beyond the scope of this thesis.

{b} The error owing to the switching noise, voltage and current offset of the multiplexer and the time interval between the measurements of successive channels as in (2) and (3) above can be overcome by using 12 ADCs, two for each channel at 0 and 90 deg. phase shift modulating clock, instead of employment of the noisy analogue multiplexer.

{c} The error owing to the performance of ADC in (4) above can be overcome by replacement of the homemade ADC with a more reliable commercial equivalent.

{d} A more careful layout of the circuit on a printed circuit board would also reduce the noise, i.e. reduce the degree of error.

CHAPTER SEVEN

To make an end is to make a beginning.

The end is where we start from.

T. S. Eliot

If a jade travels thousand miles, it is only through
perseverance.

K. L. Shum

7 CONCLUSIONS AND RECOMMENDATIONS

This thesis has covered the subject of harmonics existing in a three phase power system and the measurement thereof. It is hoped that its application will be of some use in solving some of the problems caused by harmonics in three phase systems.

In view of the contents of this thesis the following conclusions can be drawn.

(1) The main contribution of this project was the development of a general purpose instrument for measuring amplitudes and phase angles of harmonics of the three phase power systems and express them in symmetrical components.

(2) The final configuration of the instrument is relatively unimportant. Important is the measurement technique employed by the instrument.

(3) The project showed that an innovative "+1 and -1" modulation technique can be successfully applied to measure the amplitudes and phase angles of harmonics.

(4) The various tests performed on the instrument show that it functions properly, but the goals of high degree of precision and real time speed were not consummately achieved with this first model.

(5) The overall impression of the thesis is that the expressing of the amplitudes and phase angles of harmonic components in symmetrical components seems irrelevant. The reason of expressing the testing results in symmetrical components will be explained in Recommendation (3).

In the view of the author of this thesis the following recommendations are proposed.

<1> A thorough analysis and software simulation tests to evaluate the performance of the "+1 and -1" technique should be internationally disclosed by the author of this thesis in order to raise a challenge to the current signal processing methods. These jobs are obviously beyond the scope of this thesis.

<2> Both measuring speed and accuracy will be considerably improved if some alterations are made according to the suggestions in section 6-5.

<3> "Symmetrical components" is the elementary vehicle of unbalance and load flow analyses for three phase power systems. With a little additional software, this instrument can be extended to analyse unbalance and load flow, etc. i.e. increasing the versatility of the instrument.

<4> An instrument like this is useful for harmonic, unbalance, load flow analyses, etc. in areas with dense electrical distribution networks, for example the USA, Europe and North-east Asia.

<5> The merits and advantages of this instrument over that of the mini- and/or mainframe computer include the following :
Inexpensive and easy installation, maintenance and supervision of performance in terms of

- (a) harmonic analysis,
- (b) unbalance analysis,
- (c) load flow analysis,
- (d) the ability of communication with host computer and/or

parallel operation with other instruments such as controllers, etc.

is ensured if an entire distribution network is served by this instrument.

<6> The deployment of hundreds of this instrument in a whole distribution network will prove more effective than a few mini- and/or mainframe computers.

<7> The versatility of the instrument makes it extremely powerful and it is hoped that circumstances will permit the further development and application of the instrument.

B I B L I O G R A P H Y

- [1] Fitzgerald, Electric Machinery 4/E, 1984
International Student Edition
- [2] Kimbark, E. W. Direct Current Transmission
Vol. 1, Wiley, New York, 1971
- [3] RCA Silicon Power Circuits Manual, 1969.
- [4] Reeve, J. and Krishnayya, P. L. S.,
Unusual current harmonics arising from high voltage
d.c. transmission, IEEE PAS - 87, No. 3, pp 883-893,
March 1968
- [5] Klingshirn, E. A. and Jordon, H. E.,
Polyphase induction motor performance and losses on
non-sinusoidal voltage sources, IEEE Trans, Pas-87,(3),
pp. 624-631, 1968.
- [6] Chalmers, B. J. and Sarkar, B. R.
Induction motor losses due to non-sinusoidal waveforms.
Proc IEE, 115,(12), pp 1777-1782, 1968
- [7] BEDŘICH HELLER and VÁCLAN HAMATA,
Harmonic field effects in induction machines,
Elsevier Scientific, 1977
- [8] Sasaki, H and Machida, T., " A new method to a.c.
harmonic currents by magnetic flux compensation.
Considerations on basic design. "
Trans IEEE, Pas 71, pp. 2009 - 2019, 1952
- [9] Baird, J. F., and Arrillage, J., " Harmonic reduction
in dc-ripple reinjection. "
Proc. IEEE 127 , Pt. C., No 5 (Sept. 1980)
- [10] D.C. Transmission, Zhejiang Power Research Institute.
(in Chinese),1981.
- [11] Gross, E. T. B. and Hesse, M. H.,
Electromagnetic Unbalance of Untransposed Transmission
Lines.,
AIEE Trans., Vol. 72, Dec 1953, pp 1323-1336
- [12] Gross, E. T. B. and Nelson, S. W.,
Electromagnetic Unbalance of Untransposed Transmission
Lines II - Single Lines with Horizontal Conductors.
AIEE Trans., Vol. 74, Oct. 1975, pp 887-896.
- [13] Foresque, C. L. , Method of Symmetrical Coordinates
applied to the solution of Polyphase Networks,
Trans. AIEE 37 : pp 1027- 1140, 1918

- [14] Weedy , B. M. Electric Power Systems, 3rd Ed., 1979
- [15] Ander, F. M., Analysis of Faulted Power System,
Iowa State Press , Ames, Iowa, 1973
- [16] Franklin and Franklin
JSP Transformers Book 11/E, Butterworth & Co. Ltd. 1983
- [17] Wagner and Evans, Symmetrical Components,
McGraw_ Hill Book Co. , 1933
- [18] Gross, Charles A., Power System Analysis,
Auburn University, 1979
- [19] Van E Marblekos,
Electric Machine Theory for Power Engineers
Univ. of Washington, 1980
- [20] Douglass, D. A., Current Transformer accuracy with
asymmetric and high frequency fault currents,
TRANS IEEE, paper 805M 634-6, Summer Meeting,
Minneapolis, 1980
- [21] Lam, H. Y- F, Analog and Digital Filter, Design and
Realization. Prentice_ Hall , 1979
- [22] Geçkinli and Yavuz , Discrete Fourier Transform
and its applications to power spectra estimation.
Amsterdam, Elsevier Scientific, 1983
- [23] Meade, M. L. Advances in lock- in amplifiers.
J. Phys. E: Sci. Instrum., Vol. 15 1982
- [24] Phillips and Nagle , Digital Control System Analysis
and Design . Prentice Hall, 1984
- [25] M. A. Slonim, I. Rappoport and F. P. Biringer,
Calculation of Fourier Coefficients of Experimentally
obtained waveform.
IEEE Trans. on Industrial and Control Instrumentation
Nov. 1981, vol IECI-28 No. 4
- [26] M. A. Slonim, Theory of Static Converter Systems,
Elsevier Science Publishers B. C., 1984
- [27] Gardner, F. M., Phaselock Techniques,
J. Wiley and Son Inc., 1979
- [28] PMI, Catalogue , 1982
- [29] Intel, Microprocessor and Peripheral Handbook, 1983
- [30] National Semi. , Cmos Data Book , 1984

- [31] National Semi. , Data Acquisition Data Book, 1984
- [32] Motorola Semi. , 8_ bit Microprocessor Handbook
- [33] Hewlett Packard, Tutorial Description of the HP-IB
Nov. 1980
- [34] IEEE Standard Digital Interface for Programmable
Instrumentation, IEEE Standard 488-1975
- [35] Motorola Semiconductor, Schottky TTL Data Book, 1984/85
- [36] Richards, R. K., Arithmetic Operations in Digital
Computers, Van Nostrand 1955
- [37] Titus, Rony, Larson and Titus,
8080/8085 Software Design, Howard W. Sam & Co., 1979

APPENDICES

The world is surely large enough for you and me.

Toby

Appendix A.

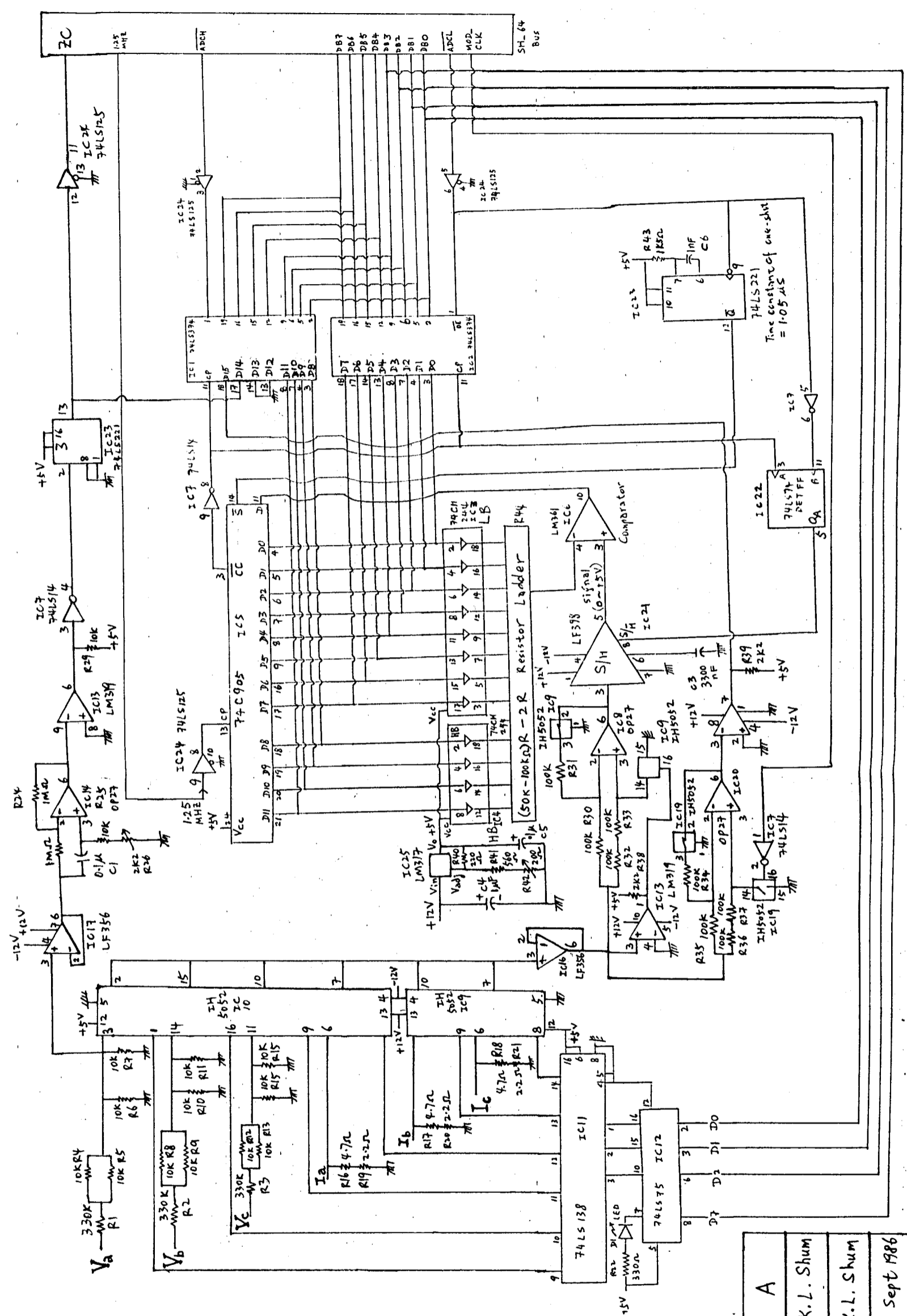
Assignment of SH-64 Bus

(C)	(Pin)	(A)
+ 5 V	1	+ 5 V
DB1	2	DB0
DB3	3	DB2
DB5	4	DB4
DB7	5	DB6
ZC	6	1.25 MHz
R/ \bar{W}	7	E
LEDP	8	
$\overline{\text{ADCH}}$	9	$\overline{\text{ADCL}}$
AB1	10	AB0
	11	AB2
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	$\overline{\text{RESET}}$
	22	
	23	
	24	
	25	
	26	
OUT 0	27	$\overline{\text{CS}}$ OF 68488
	28	
	29	
	30	MOD_CLK
- 12 V	31	PHASE PORT
+ 12 V	32	GND

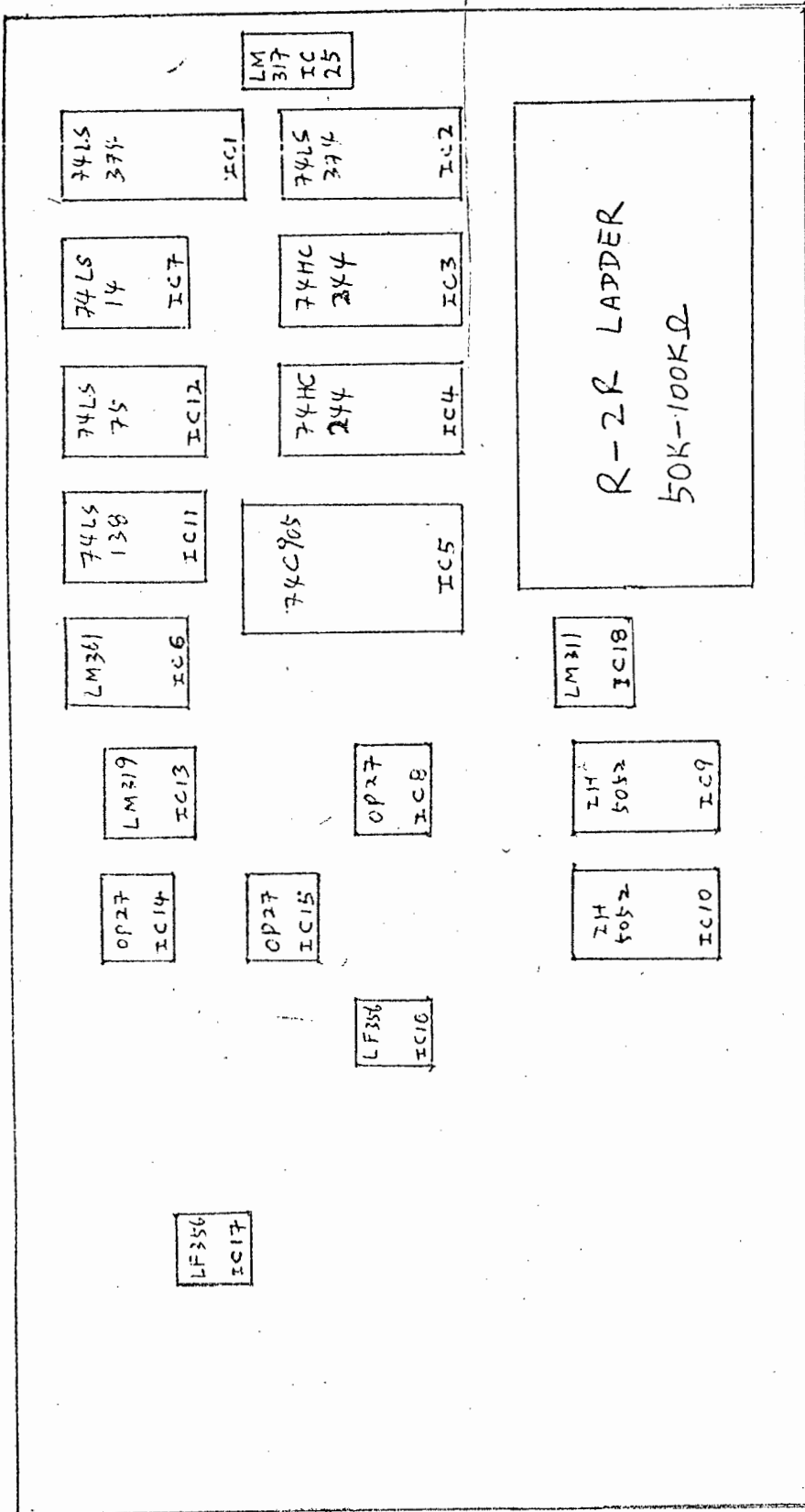
Notice : DB and AB stand for Data and Address Bus respectively.

A P P E N D I X B

Individual Circuit Diagrams of Card A, B and C.

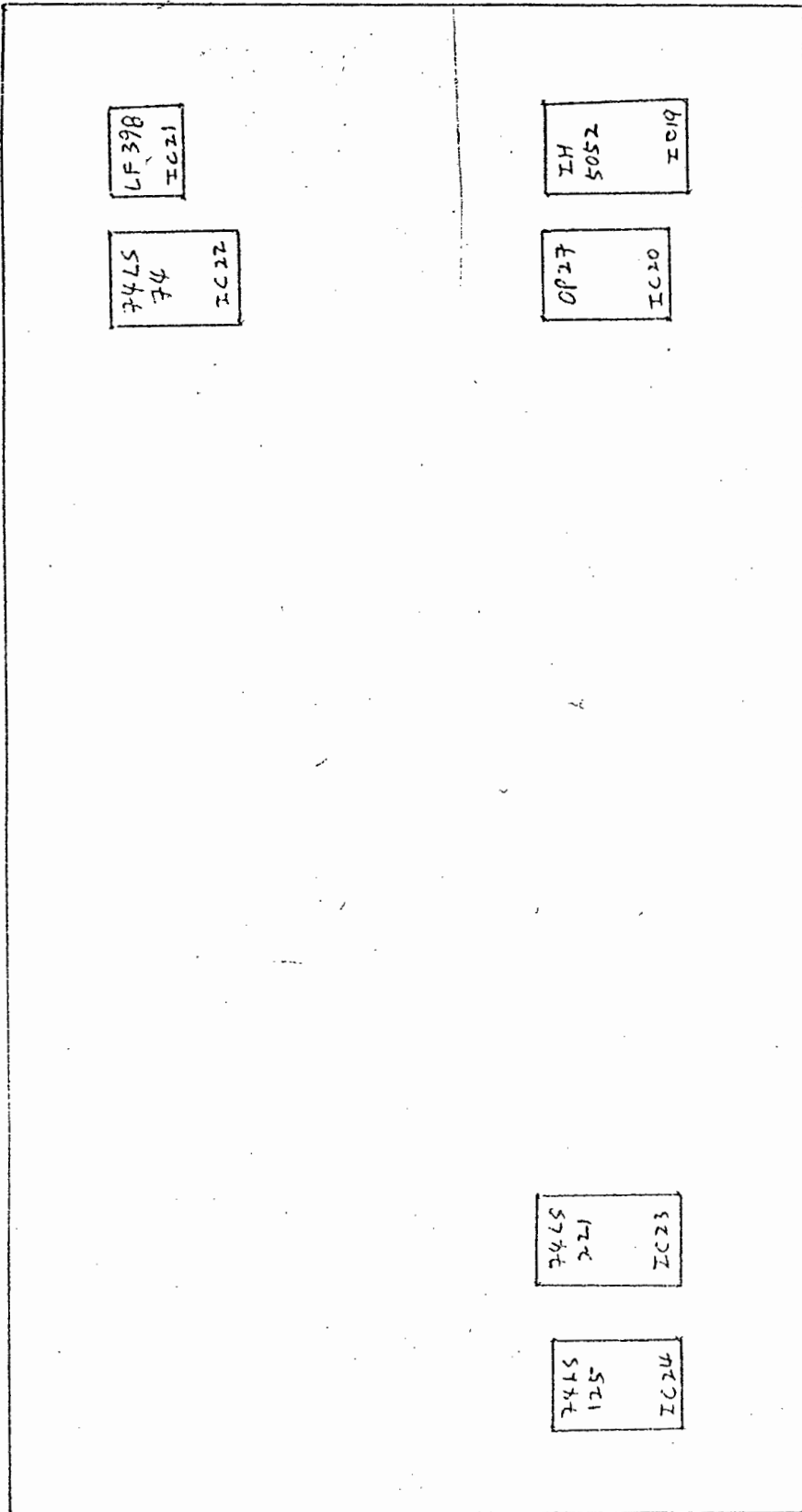


CARD A
 DESIGN K.L. Shum
 DRAWN K.L. Shum
 DATE 3 Sept 1986



(Top View)

Layout of CARD A (Top View)



(Bottom View)

Layout of CAPD A (Bottom View)

IC Listing of CARD A :

- | | | | |
|-----|---------|-----|----------|
| 1) | 74LS374 | 16) | LF356 |
| 2) | 74LS374 | 17) | LF356 |
| 3) | 74HC244 | 18) | LM311 |
| 4) | 74HC244 | 19) | IH5052 |
| 5) | 74C905 | 20) | OP27 |
| 6) | LM361 | 21) | LF398 |
| 7) | 74LS14 | 22) | 74LS74 |
| 8) | OP27 | 23) | 74LS221 |
| 9) | IH5052 | 24) | 74LS125A |
| 10) | IH5052 | 25) | LM317 |
| 11) | 74LS138 | | |
| 12) | 74LS75 | | |
| 13) | LM319 | | |
| 14) | OP27 | | |
| 15) | OP27 | | |

Components Listing of Card A :

Capacitor

C1,C2 -----0.1 μ

C3 -----3300n polyethylene

C4 -----1 μ tant

C5 ----- 0.1 μ tant

C6 ----- 1n

C7 ----- 1 μ

Others

D1 -----LED

Resistor :

R1,R2,R3 330K ohm 1/2W

R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R15 10K ohm 1/2W

R16,R17,R18 4.7 ohm 10W

R19,R20,R21 2.2 ohm 10W

R22 330 ohm 1/2W

R23,R24 1Mohm 1%

R25 10K ohm

R26 2K2 trimmed pot

R27,R28 15K ohm 1%

R30,R31,R32,R33,R34,R35,R36,R37 100K ohm 1%

R38,R39 2K2 ohm

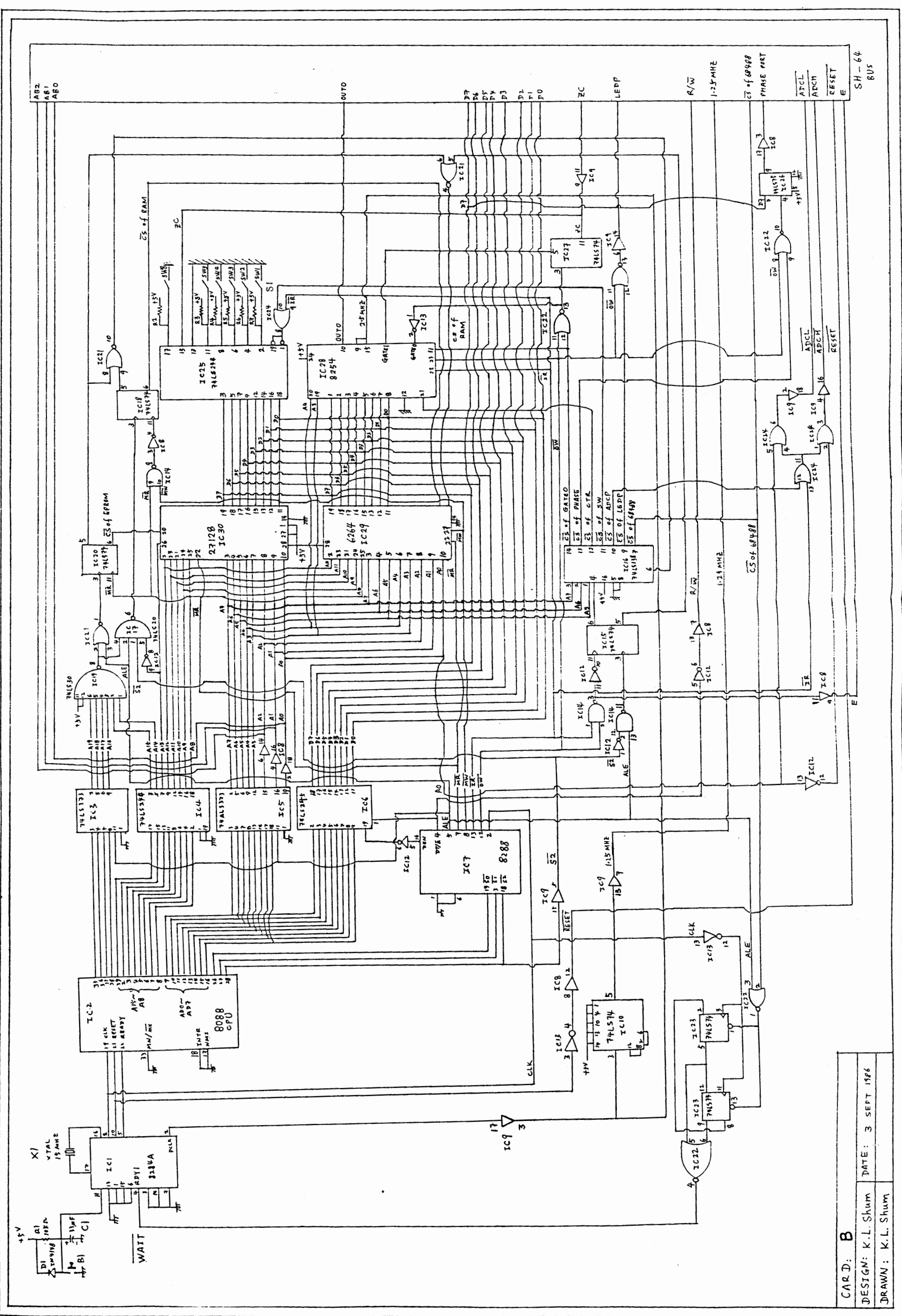
R40 220 ohm

R41 560 ohm

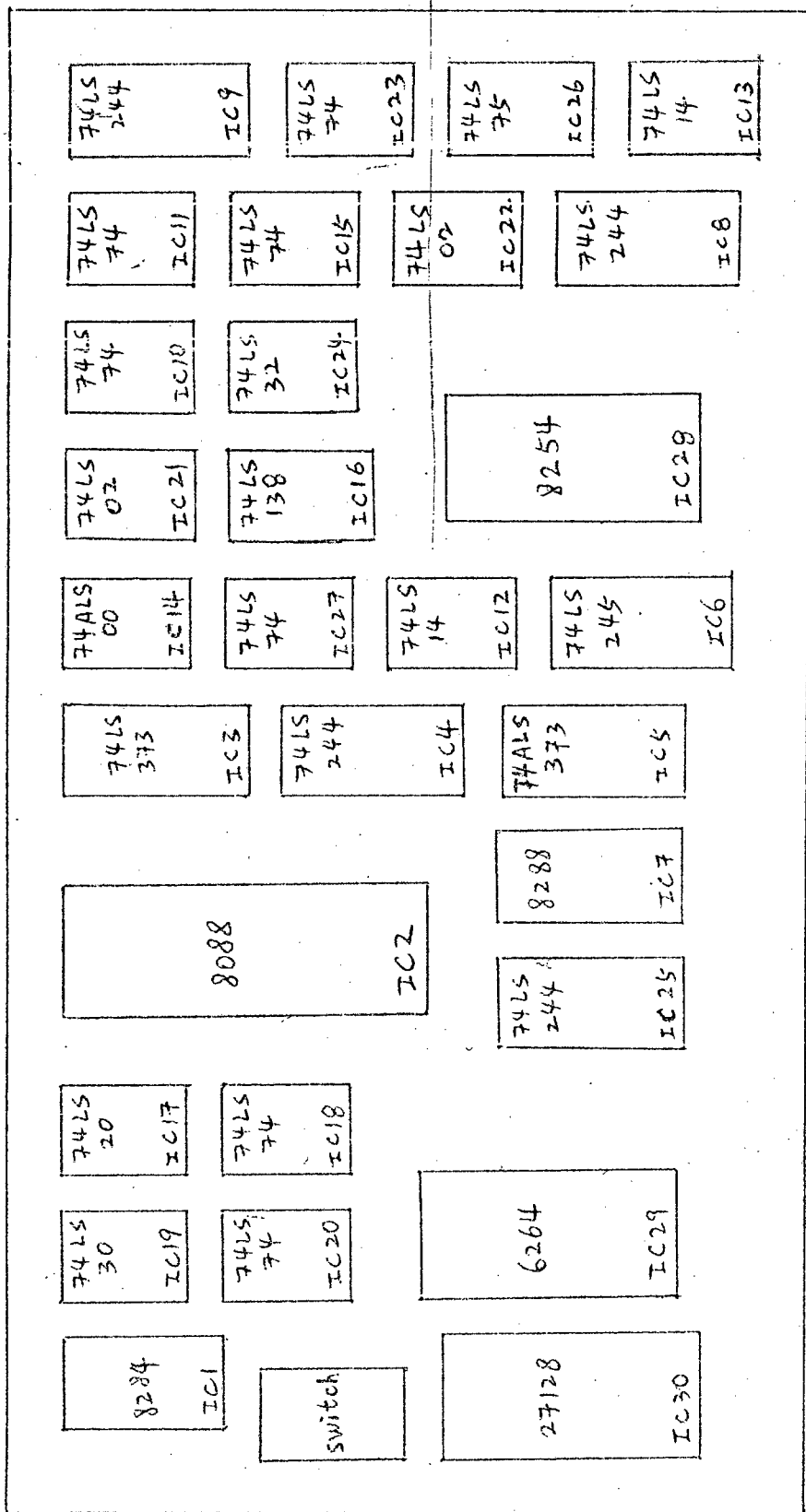
R42 200 ohm trimmed pot

R43 1K5 ohm

R44 50K-100K ohm (12-bit) Resistor Ladder



CARD: B
 DESIGN: K.L. SHUM DATE: 3 SEPT 1986
 DRAWN: K.L. SHUM



(Top View)

Lay out of CAP.D.B

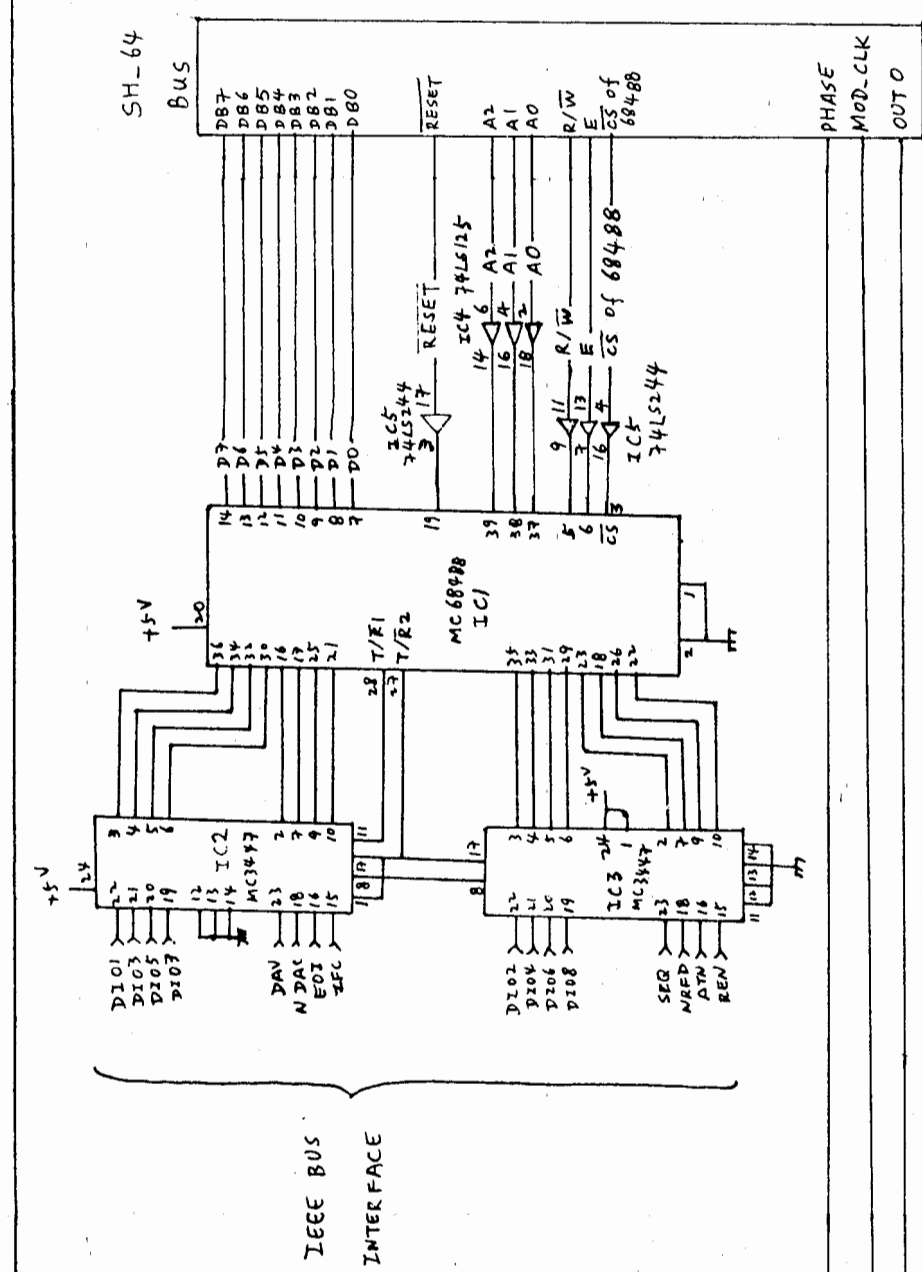
IC Listing of CARD B :

1)	8284	16)	74LS138
2)	8088	17)	74LS20
3)	74LS373	18)	74LS74
4)	74LS244	19)	74LS30
5)	74ALS373	20)	74LS74
6)	74LS245	21)	74LS02
7)	8288	22)	74LS02
8)	74LS244	23)	74LS74
9)	74LS244	24)	74LS32
10)	74LS74	25)	74LS244
11)	xxxxxx	26)	74LS75
12)	74LS14	27)	74LS74
13)	74LS14	28)	8254
14)	74ALS00	29)	6264
15)	74LS74	30)	27128

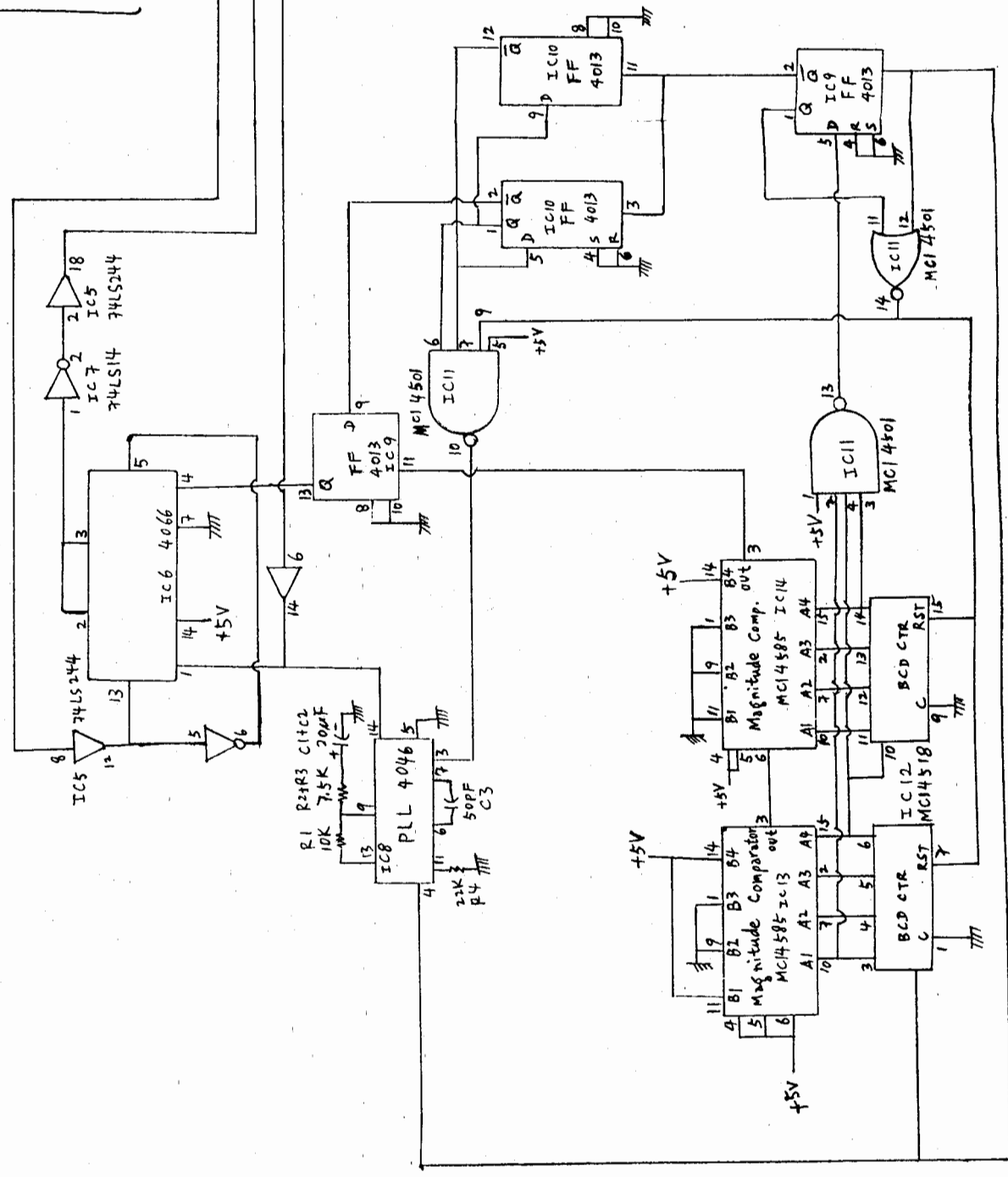
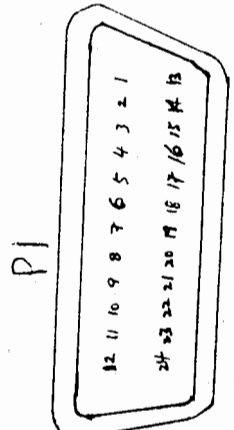
Component Listing of Card B :

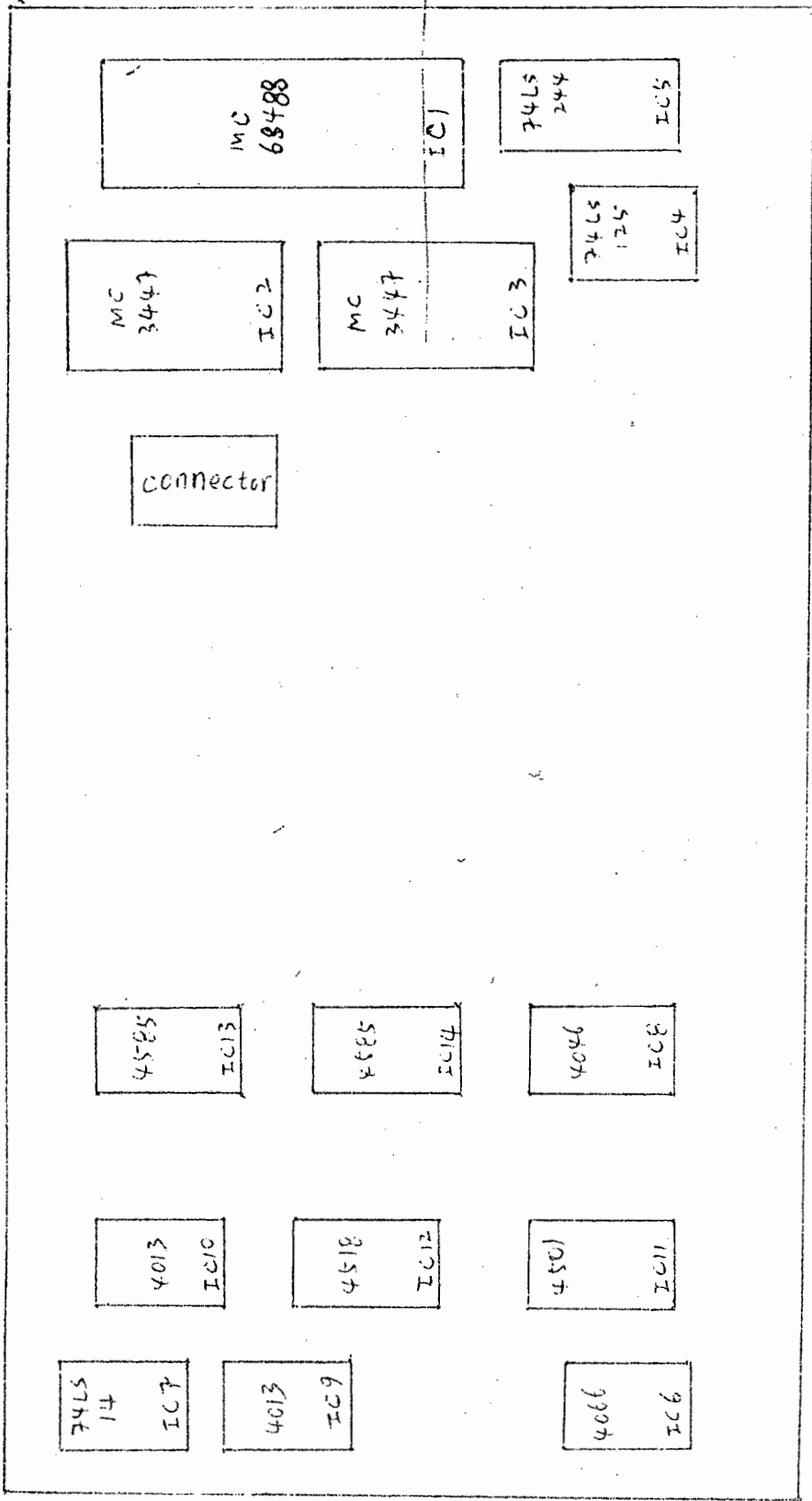
X1 ----- 15MHZ Crystal
D1 ----- IN4148 Diode
B1 ----- Press-button switch
C1 ----- 33 μ F tant
R1 ----- 10K ohm
R2,R3,R4,R5,R6,R7 ----- 2K2 ohm
S1 ----- 8 position switch

CARD: C
 DESIGN: K.L. Shum
 DRAWN: K.L. Shum
 DATE: 3 SEPT 1986



(Contact)	(Signal line)	(Contact)	(Signal line)
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	E01	17	REN
6	DAV	18	} GND
7	NRFD	19	
8	NDAC	20	
9	IFC	21	
10	SRQ	22	
11	ATN	23	
12	SHIELD	24	





(Top View)

Layout of CAPDC

IC Listing of Card C :

- 1) MC68488
- 2) MC3447
- 3) MC3447
- 4) 74LS125A
- 5) 74LS244
- 6) 4066
- 7) 74LS14
- 8) 4046
- 9) 4013
- 10) 4013
- 11) 4051
- 12) 4518
- 13) 4585
- 14) 4585

Component Listing of Card C :

- P1 IEEE/ANSI Connector
C1,C2 10 u ohm tant
C3 50pF
R1 10 K ohm
R2,R3 15 K ohm
R4 22K ohm

A P P E N D I X C

Program Listing of Operating System.

ES-III 8086/87/88/186 MACRO ASSEMBLER V2.0 ASSEMBLY OF MODULE SHUM
ST MODULE PLACED IN :F3:A2:OBJ
ASSEMBLER INVOKED BY: ASMB6.86 :F3:A2.SRC SYMBOLS

LINE	SOURCE
1	ALL PRAISE BE TO GOD
2	THE LORD OF THE WORLDS
3	MOST BENEFICIENT AND MOST MERCIFUL
4	THE MASTER OF THE DAY OF JUDGEMENT
5	TO THEE ALONE DO WE WORSHIP
6	THINE AID WE SEEK
7	SHOW US THE STRAIGHT PATH
8	THE PATH OF THOSE ON WHOM THOU HAST BESTOWED THY GRACE
9	NOT OF THOSE WHOSE FORTION IS WRATH NOR OF THOSE WHO GO ASTRAY
10	AMEN

NAME SHUM

#####

ABBREVIATION :

ABS.	STANDS FOR ABSOLUTE VALUE
ADC	STANDS FOR ANALOGUE TO DIGITAL CONVERTOR
AMP.	STANDS FOR AMPLITUDE
ANG.	STANDS FOR ANGLE
CLK	STANDS FOR CLOCK
MAX.	STANDS FOR MAXIMUM
MIN.	STANDS FOR MINIMUM
XY	STANDS FOR D.C. TERM
ZC.	STANDS FOR FUNDAMENTAL FILTERED ZERO_CROSSING

OBJ

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

OBJ

LINE

SOURCE

51 #####

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

#####

PROCEDURES ORDER :

- (1) BEGIN
- (2) ZC_ADC
- (3) AVERAGING
- (4) MOD_CLK_UPDATE_1
- (5) MOD_CLK_UPDATE
- (6) MOD_CLK_SYN
- (7) DEHA
- (8) DIV_32
- (9) SROOT
- (10) QUE
- (11) LFANG
- (12) GPIB
- (13) GPIB1
- (14) DUMMY_READ
- (15) THREE_7_8
- (16) THREE_7_7
- (17) THREE_7_6
- (18) THREE_7_5
- (19) THREE_7_4
- (20) THREE_7_3
- (21) THREE_7_2
- (22) THREE_7_1
- (23)

#####

PART : 0

SET UP STORAGE AREA AND LOOK_UP TABLE FOR ARC_COS .

#####

SAMP SEGMENT WORD AT 45H

SAM DW 2000D DUP(?) ;NO. OF SAM FROM ADC

AMP DW 150D DUP(?) ;6*25_ NO. OF V AND I

(2000
???)
)
(150
???)
)

```

DBJ
(150
???)
(300
???)
???)
(3
???)
???)
???)
???)
(12
???)

```

```

LINE SOURCE
102 ANG DW 150D DUP(?) ;6*25_ NO. OF ANG OF V AND I
103 XY DW 300D DUP(?) ;12*25_ NO. OF X OR Y PER CHANNEL
104 PAF DW ?
105 PA DW 3 DUP(?)
106 ASH DW ?
107 ASL DW ?
108 FREQ DW ?
109 ZCCP DW ?
110 ZCC DW 12D DUP(?)

```

```

; AVERAGE FREQUENCY OF INPUT SIGNAL
; ZCC POINTER
; ZCC STORES 1ST 12 VALUE OF COUNTER 1

```

```

R0 TO R16 ARE SCRATCH PADS TO STORE TEMPORARY DATA :

```

```

111 R0 DW ?
112 R1 DW ?
113 R2 DW ?
114 R3 DW ?
115 R4 DW ?
116 R5 DW ?
117 R6 DW ?
118 R7 DW ?
119 R8 DW ?
120 R9 DW ?
121 R10 DW ?
122 R11 DW ?
123 R12 DW ?
124 R13 DB ?
125 R14 DB ?
126 R15 DB ?
127 R16 DB ?

```

```

SAMP ENDS

```

```

ATCS SEGMENT WORD AT 0FC00H

```

```

FFFF
DFFF
BFFF
SFFF
OFFF
SFFF
)FFF
SI=0
SI=2
SI=4

```

OBJ SOURCE

149	D7FF	DW	0FFD7H	
150	CEFF	DW	0FFCEH	
151	C5FF	DW	0FFC5H	
152	B8FF	DW	0FFB8H	
153	B0FF	DW	0FFB0H	
154	A5FF	DW	0FFA5H	
155	98FF	DW	0FF98H	
156	88FF	DW	0FF88H	
157	70FF	DW	0FF70H	
158	6EFF	DW	0FF6EH	
159	5FFF	DW	0FF5FH	
160	4FFF	DW	0FF4FH	
161	3DFF	DW	0FF3DH	
162	28FF	DW	0FF28H	
163	19FF	DW	0FF19H	
164	05FF	DW	0FF05H	
165	F1FE	DW	0FFEF1H	
166	DCFE	DW	0FFEDCH	
167	C6FE	DW	0FFEC6H	
168	AFFE	DW	0FFEAFH	
169	97FE	DW	0FE97FH	
170	7FFE	DW	0FE7FH	
171	66FE	DW	0FE66H	
172	4CFE	DW	0FE4CH	
173	31FE	DW	0FE31H	
174	16FE	DW	0FE16H	
175	FAFD	DW	0FDFAH	
176	DDFD	DW	0FDDDH	
177	BFED	DW	0FDBFH	
178	A0FD	DW	0FDA0H	
179	81FD	DW	0FD81H	
180	60FD	DW	0FD60H	
181	3FFD	DW	0FD3FH	
182	1EFD	DW	0FD1EH	
183	FBFC	DW	0FCFBH	
184	D8FC	DW	0FC8H	
185	B3FC	DW	0FCB3H	
186	8FFC	DW	0FC8FH	
187	69FC	DW	0FC69H	
188	42FC	DW	0FC42H	
189	1BFC	DW	0FC1BH	
190	F3FB	DW	0FBF3H	
191	CAPB	DW	0FBCAH	
192	A0FB	DW	0FBA0H	
193	76FB	DW	0FB76H	
194	4AFB	DW	0FB4AH	
195	1EFB	DW	0FB1EH	
196	F2FA	DW	0FAF2H	
197	C4FA	DW	0FA4H	
198	96FA	DW	0FA96H	
199	66FA	DW	0FA66H	
200	36FA	DW	0FA36H	
201	06FA	DW	0FA06H	
202	D4F9	DW	0F9D4H	
203	A2F9	DW	0F9A2H	

;SI=20 (10)

;SI=40 (20)

;SI=60 (120)

;SI=72 (#36)

;SI=80 (40)

;SI=100 (50)

;SI=120 (60)

OBJ LINE SOURCE

```

6FF9 DW
3BF9 DW
06F9 DW
D1F8 DW
9BF8 DW
64F8 DW
2CF8 DW
F4F7 DW
BAF7 DW
80F7 DW
45F7 DW
0AF7 DW
C0F6 DW
90F6 DW
52F6 DW
14F6 DW
D4F5 DW
94F5 DW
53F5 DW
11F5 DW
C0F4 DW
8CF4 DW
48F4 DW
03F4 DW
BDF3 DW
77F3 DW
30F3 DW
E8F2 DW
A0F2 DW
56F2 DW
00F2 DW
C1F1 DW
76F1 DW
29F1 DW
DCF0 DW
8EF0 DW
40F0 DW
F0EF DW
A0EF DW
4FEF DW
FEEEE DW
ABEEE DW
58EEE DW
04EEE DW
B0ED DW
5AED DW
04ED DW
AEEC DW
56EC DW
FEEB DW
A5EB DW
F1EA DW
95EA DW
39EA DW
0F96FH DW
0F93BH DW
0F906H DW
0F8D1H DW
0F89BH DW
0F864H DW
0F82CH DW
0F7F4H DW
0F7BAH DW
0F780H DW
0F745H DW
0F70AH DW
0F6CDH DW
0F690H DW
0F652H DW
0F614H DW
0F5D4H DW
0F594H DW
0F553H DW
0F511H DW
0F4CFH DW
0F48CH DW
0F448H DW
0F403H DW
0F3BDH DW
0F377H DW
0F330H DW
0F2E8H DW
0F2A0H DW
0F256H DW
0F20CH DW
0F1C1H DW
0F176H DW
0F129H DW
0F0DCH DW
0F08EH DW
0F040H DW
0EFF0H DW
0EFA0H DW
0EF4FH DW
0EEFEH DW
0EEABH DW
0EE58H DW
0EE04H DW
0EDB0H DW
0ED5AH DW
0ED04H DW
0ECAEH DW
0EC56H DW
0EBFEH DW
0EB45H DW
0EB0BH DW
0EAF1H DW
0EA95H DW
0EA39H DW

```

:SI=140 (70)
:SI=144 (#72)

:SI=160 (80)

:SI=180 (90)

:SI=200 (100)
:SI=204 (#102)

:SI=220 (110)

OBJ LINE SOURCE

```

DDE9 259 DW 0E9DDH
7FE9 260 DW 0E97FH
21E9 261 DW 0E921H
C2E8 262 DW 0E8C2H
63E8 263 DW 0E863H
02E8 264 DW 0E802H
A1E7 265 DW 0E7A1H
40E7 266 DW 0E740H
DDE6 267 DW 0E6DDH
7AE6 268 DW 0E67AH
16E5 269 DW 0E616H
B1E5 270 DW 0E5B1H
4CE5 271 DW 0E54CH
E6E4 272 DW 0E4E6H
7FE4 273 DW 0E47FH
18E4 274 DW 0E418H
AFE3 275 DW 0E3AFH
46E3 276 DW 0E346H
DDE2 277 DW 0E2DDH
73E2 278 DW 0E273H
07E2 279 DW 0E207H
9CE1 280 DW 0E19CH
2FE1 281 DW 0E12FH
C4E0 282 DW 0E0C2H
E6DF 283 DW 0E05AH
76DF 284 DW 0DFE6H
06DF 285 DW 0DF76H
96DE 286 DW 0DF06H
25DE 287 DW 0DE96H
B2DD 288 DW 0DE25H
40DD 289 DW 0DD82H
58DD 290 DW 0DD40H
E3DB 291 DW 0DDCCH
F8DA 292 DW 0DD58H
81DA 293 DW 0DBE3H
09DA 294 DW 0DB6EH
18D9 295 DW 0DAF8H
9ED8 296 DW 0DA81H
25D8 297 DW 0DA09H
9AD7 298 DW 0D991H
2ED7 299 DW 0D918H
B2D6 300 DW 0D89FH
5DD6 301 DW 0D825H
87D5 302 DW 0D7AEH
39D5 303 DW 0D72EH
BAD4 304 DW 0D6B2H
3AD4 305 DW 0D635H
B8D3 306 DW 0D5B7H
26D2 307 DW 0D539H
7FE2 308 DW 0D4BAH
C2E1 309 DW 0D43AH
63E1 310 DW 0D3BAH
02E1 311 DW 0D339H
A1E0 312 DW 0D2BBH
40E0 313 DW 0D236H

```

```

:SI=240 (120)
:SI=246 (#123)
:SI=260 (130)
:SI=280 (140)
:SI=290 (#145)
:SI=300 (150)
:SI=320 (160)
:SI=322 (#161)
:SI=340 (170)

```

OBJ SOURCE

```

B3D1 0D1B3H
2FD1 0D12FH
ABD0 0D0ABH
26D0 0D026H
A1CF 0CF1AH
1ACF 0CE94H
9ACE 0CE0CH
84CD 0CD84H
FBCC 0CCFBH
72CC 0CC72H
E8CB 0CBEBH
D2CA 0CAD2H
46CA 0CA46H
BAC9 0C9BAH
2DC9 0C92DH
9FC8 0CB9FH
10C8 0CB10H
81C7 0C781H
F2C6 0C661H
61C6 0C5D1H
3FC5 0C53FH
ADC4 0C4ADH
1AC4 0C41AH
87C3 0C387H
53C2 0C2F3H
09C1 0C1C9H
33C1 0C133H
9DC0 0C09DH
06C0 0C006H
6E8E 0BF6EH
D68E 0BED6H
3DBE 0BE3DH
A4BD 0BDA4H
0ABD 0BD0AH
70BC 0BC70H
D4BB 0BBD4H
39BB 0BB39H
9CBA 0BA9CH
00BA 0BA00H
62B9 0B962H
C4B8 0B8C4H
25B8 0B825H
86B7 0B786H
E6B6 0B6E6H
46B6 0B646H
A5B5 0B5A5H
04B5 0B504H
62B4 0B462H
FFB3 0B3BFH
1CB3 0B31CH
78B2 0B278H

```

;SI=358 (#179)
;SI=360 (180)

;SI=380 (190)

;SI=400 (200)

;SI=416 (#208)
;SI=420 (210)

;SI=440 (220)

OBJ LINE SOURCE

D4B1	369	DW	0B1D4H	
2FB1	370	DW	0B12FH	:SI=460 (230)
8AB0	371	DW	0B0BAH	
E4AF	372	DW	0AFE4H	:SI=466 (#233)
3DAF	373	DW	0AF3DH	
96AE	374	DW	0AE96H	
EFAD	375	DW	0ADEFH	
47AD	376	DW	0AD47H	
9EAC	377	DW	0AC9EH	
F5AB	378	DW	0ABF5H	
4BAB	379	DW	0AB4BH	
A1AA	380	DW	0AAA1H	:SI=480 (240)
F6A9	381	DW	0A9F6H	
4BA9	382	DW	0A94BH	
9FAB	383	DW	0A89FH	
F2A7	384	DW	0A7F2H	
45A7	385	DW	0A745H	
98A6	386	DW	0A698H	
EAA5	387	DW	0A5EAH	
3CA5	388	DW	0A53CH	
8DA4	389	DW	0A48DH	
DDA3	390	DW	0A3DDH	:SI=500 (250)
2DA3	391	DW	0A32DH	
7DA2	392	DW	0A27DH	
CCA1	393	DW	0A1CCH	
1AA1	394	DW	0A11AH	
68A0	395	DW	0A068H	:SI=514 (#257)
B59F	396	DW	09FB5H	
029F	397	DW	09F02H	
4E9E	398	DW	09E4FH	
9B9D	399	DW	09D9BH	:SI=520 (260)
E69C	400	DW	09CE6H	
319C	401	DW	09C31H	
7C9B	402	DW	09B7CH	
C69A	403	DW	09AC6H	
5999	404	DW	09A0FH	
A198	405	DW	09959H	
E997	406	DW	098A1H	
3197	407	DW	097E9H	
7896	408	DW	09731H	
BE95	409	DW	09678H	:SI=540 (270)
0595	410	DW	095BFH	
4B94	411	DW	09505H	
9093	412	DW	0944BH	
D592	413	DW	09390H	
1992	414	DW	092D5H	
5D91	415	DW	09219H	
A190	416	DW	0915DH	
E48F	417	DW	090A1H	
268F	418	DW	08FE4H	:SI=558 (#279)
688E	419	DW	08E26H	:SI=560 (280)
AABD	420	DW	08E68H	
EB8C	421	DW	08DAAH	
2C8C	422	DW	08CEBH	
	423	DW	08C2CH	

OBJ LINE SOURCE

```

6C8B 424 08B6CH
AC8A 425 08AACH
EC89 426 089ECH
2889 427 0892BH
6A88 428 0886AH
A887 429 087ABH
E686 430 086E6H
2386 431 08623H
6085 432 08560H
9C84 433 0849CH
D983 434 083D9H
1483 435 08314H
5082 436 08250H
8A81 437 0818AH
C580 438 080C5H
FF7F 439 07FFFH
397F 440 07F39H
727E 441 07E72H
AB7D 442 07DABH
E37C 443 07CE3H
1B7C 444 07C1BH
537B 445 07B53H
8B7A 446 07ABBH
C279 447 079C2H
F878 448 078F8H
2E78 449 0782EH
6477 450 07764H
9A76 451 0769AH
CF75 452 075CFH
0375 453 07503H
3874 454 07438H
9F72 455 0736CH
D371 456 0729FH
3870 457 071D3H
6A6F 458 07106H
9C6E 459 06F6AH
CE6D 460 06E9CH
306C 461 06DCEH
606B 462 06C30H
906A 463 06B60H
C069 464 06A90H
F068 465 069C0H
1E68 466 068F0H
4E67 467 0681FH
7C66 468 0674EH
AB65 469 0667CH
D864 470 0661FH
0664 471 065ABH
3363 472 064D8H
6062 473 06406H
8D61 474 06333H
E960 475 06260H
      476 0618DH
      477 060B9H
      478

```

:SI=580 (290)

:SI=600 (#300)

:SI=620 (310)

:SI=640 (320)
:SI=642 (#321)

:SI=660 (330)

OBJ LINE SOURCE

```

E55F 479 DW 05FE5H
115E 480 DW 05FF11H
3D5E 481 DW 05E3DH
685D 482 DW 05D68H
935C 483 DW 05C93H
BD5B 484 DW 05BBDH
E75A 485 DW 05AE7H
115A 486 DW 05A11H
3B59 487 DW 0593BH
6558 488 DW 05865H
8E57 489 DW 0578EH
B756 490 DW 05687H
DF55 491 DW 055DFH
0855 492 DW 05508H
3054 493 DW 05430H
5853 494 DW 05358H
7F52 495 DW 0527FH
A651 496 DW 051A6H
CE50 497 DW 050CEH
F44F 498 DW 04FF4H
1B4F 499 DW 04F1BH
414E 500 DW 04E41H
674D 501 DW 04D67H
8D4C 502 DW 04C8DH
B34B 503 DW 04BB3H
DB4A 504 DW 04AD8H
FD49 505 DW 049FDH
2249 506 DW 04922H
4748 507 DW 04847H
6B47 508 DW 0476BH
8F46 509 DW 0468FH
B345 510 DW 045B3H
D744 511 DW 044D7H
FB43 512 DW 043FBH
1E43 513 DW 0431EH
4142 514 DW 04241H
6441 515 DW 04164H
8740 516 DW 04087H
A93F 517 DW 03FA9H
CC3E 518 DW 03ECC
EE3D 519 DW 03DEEH
103D 520 DW 03D10H
323C 521 DW 03C32H
523B 522 DW 03B53H
743A 523 DW 03A74H
9639 524 DW 03996H
B738 525 DW 038B7H
D837 526 DW 037D8H
F836 527 DW 036F8H
1936 528 DW 03619H
3935 529 DW 03539H
5934 530 DW 03459H
7933 531 DW 03379H
9932 532 DW 03299H
B931 533 DW 031B9H

```

; SI=680 (#340)

; SI=700 (350)

; SI=718 (#359)
; SI=720 (360)

; SI=740 (370)

; SI=756 (#378)

; SI=760 (380)

; SI=780 (390)

OBJ	LINE	SOURCE	
D830	34	DW	030D8H
F82E	35	DW	02FF8H
172F	36	DW	02F17H
362E	37	DW	02E36H
522D	38	DW	02D55H
742C	39	DW	02C74H
922B	40	DW	02B92H
B12A	41	DW	02AB1H
CF29	42	DW	029CFH
ED28	43	DW	028EDH
0B27	44	DW	0280BH
2926	45	DW	02729H
4725	46	DW	02647H
6524	47	DW	02565H
8323	48	DW	02483H
A022	49	DW	023A0H
B821	50	DW	022BEH
DE20	51	DW	021DBH
1520	52	DW	020F8H
3420	53	DW	02015H
5520	54	DW	01F32H
7C20	55	DW	01E4FH
9920	56	DW	01D6CH
B820	57	DW	01C89H
DE20	58	DW	01BA5H
1520	59	DW	01AC2H
3420	60	DW	019DEH
5520	61	DW	018FBH
7C20	62	DW	01817H
9920	63	DW	01733H
B820	64	DW	0164FH
DE20	65	DW	0156BH
1520	66	DW	01487H
3420	67	DW	013A3H
5520	68	DW	012BFH
7C20	69	DW	011DBH
9920	70	DW	010F7H
B820	71	DW	01012H
DE20	72	DW	00F2EH
1520	73	DW	00E4AH
3420	74	DW	00D65H
5520	75	DW	00C81H
7C20	76	DW	00B9CH
9920	77	DW	00AB8H
B820	78	DW	009D3H
DE20	79	DW	008EFH
1520	80	DW	0080AH
3420	81	DW	00725H
5520	82	DW	00641H
7C20	83	DW	0055CH
9920	84	DW	00477H
B820	85	DW	00393H
DE20	86	DW	002AEH
1520	87	DW	001C9H
3420	88	DW	000E4H

```

;SI=792 (#396)
;SI=800 (400)

;SI=820 (410)

;SI=830 (#415)

;SI=840 (420)

;SI=860 (430)
;SI=866 (#433)

;SI=880 (440)

```

OBJ 0000
(25
???)
)

```

LINE SOURCE
589 DW 00000H ;SI=900 (450)
590
591 ENDS
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641

STACK_SEG DW SEGMENT WORD AT 40H
           DUP(?)

STACK_TOP LABEL WORD
STACK_SEG ENDS

;#####
;PART : 1
;STARTS THE CODE SEGMENT AND INITIALIZES ALL THE SEGMENT REGISTERS
;AND STACKS, AND DEFINES ADDRESSES OF ALL THE I/O PORTS.
;#####

CODE_SEG SEGMENT WORD AT 0FC50H
ASSUME CS:CODE_SEG,DS:SAMP,SS:STACK_SEG,ES:ATCS

;-----
;LEDP EQU 0C0H ;LEDP CONTAINS 8 BIT D0 TO D7,
;D7 IS FOR LED.
;-----
;LED_ON EQU 80H
;LED_OFF EQU 00H
;CHAN_Va EQU 06H
;-----
;ADCP EQU 0A0H ;INPUT AND STARTING PORT OF ADC,
;D15 IS SIGN_BIT AND D14 IS ZC SIGNAL,
;D0 TO D11 IS SAMPLE FROM 12_BIT_ADC.
;-----
;ZC_MASK_OF_ADC EQU 40H
;SIGN_BIT_MASK EQU 8000H
;SAMPLE_MASK EQU 0FFFH
;-----
;SWP EQU 80H ;SWP CONTAINS 8 BIT D0 TO D7,
;FORM_MASK EQU 80H ;D6 IS ZERO-CROSSING SIGNAL.
;ZC_MASK_OF_SWP EQU 40H ;D5 AND D7 ARE UNUSED, D0 TO D4 ARE
;FOR MANUAL SET SWITCHES TO DECIDE
;THE MAX ORDER OF HARMONICS THAT NEEDS
;TO BE MEASURED.
;-----
;HA_ORDER_MASK EQU 1FH

```

```

OBJ          LINE          SOURCE
-----
18          642          ;CENTRAL WORD OF COUNTER.
16          643          ;INITIALIZES COUNTER0 AS SQUARE WAVE,
14          644          EQU 78H          36H
10          645          ;BINARY, MODE 3.
10          646          ;INITIALIZES COUNTER1 AS RATE GENERATOR,
10          647          EQU 74H          ;BINARY, MODE 2.
10          648
10          649
10          650          ;-----
10          651          ;COUNTER1 PORT.
10          652          EQU 68H          ;COUNTER0 PORT.
10          653          EQU 60H
10          654
10          655          ;-----
10          656          ;0 OR 90 DEG MODULATING CLK SELECT PORT,
10          657          ;ONLY D7 IS EMPLOYED IN THE PORT.
10          658          EQU 40H          ;
10          659          EQU 80H          MOD_CLK_0
10          660          EQU 00H          MOD_CLK_90
10          661
10          662          ;-----
10          663          ;MODULATING CLK SYNCHRONIZED PORT.
10          664          EQU 20H          ;
10          665
10          666          ;-----
10          667          ;
10          668          BEGIN          PROC          FAR
10          669
10          670
10          671
10          672          ;DISABLE INTERRUPT.
10          673          CLI          AX,SAMP
10          674          MOV          DS,AX
10          675          MOV          AX,STACK_SEG
10          676          MOV          SS,AX
10          677          MOV          AX,ATCS
10          678          MOV          ES,AX
10          679          MOV          SP,OFFSET STACK_TOP
10          680
10          681          ;-----
10          682          ;PART : 2
10          683          ;THIS ROUTINE INITIALIZES MOST I/O PORTS AND TEMPORARY REGISTERS.
10          684          ;IT ALSO MODULATES SIX CHANNELS CYCLICALLY AT EITHER 0 DEG.
10          685          ;OR 90 DEG. PHASE SHIFT MODULATING CLK. THIS MODULATING CLOCK CAN
10          686          ;HAVE DIFFERENT HARMONIC FREQUENCIES WHICH WOULD BE ASSIGNED BY THE
10          687          ;EXTERNAL SWITCH. IT ALSO DIRECTS ADC TO OPERATE IN SYNCHRONIZATION
10          688          ;WITH THE FUNDAMENTAL FILTERED ZERO CROSSING SIGNAL. THE MODULATED
10          689
10          690
10          691
10          692
10          693
10          694
10          695
10          696
10          697
10          698
10          699
10          700
10          701
10          702
10          703
10          704
10          705
10          706
10          707
10          708
10          709
10          710
10          711
10          712
10          713
10          714
10          715
10          716
10          717
10          718
10          719
10          720
10          721
10          722
10          723
10          724
10          725
10          726
10          727
10          728
10          729
10          730
10          731
10          732
10          733
10          734
10          735
10          736
10          737
10          738
10          739
10          740
10          741
10          742
10          743
10          744
10          745
10          746
10          747
10          748
10          749
10          750
10          751
10          752
10          753
10          754
10          755
10          756
10          757
10          758
10          759
10          760
10          761
10          762
10          763
10          764
10          765
10          766
10          767
10          768
10          769
10          770
10          771
10          772
10          773
10          774
10          775
10          776
10          777
10          778
10          779
10          780
10          781
10          782
10          783
10          784
10          785
10          786
10          787
10          788
10          789
10          790
10          791
10          792
10          793
10          794
10          795
10          796
10          797
10          798
10          799
10          800
10          801
10          802
10          803
10          804
10          805
10          806
10          807
10          808
10          809
10          810
10          811
10          812
10          813
10          814
10          815
10          816
10          817
10          818
10          819
10          820
10          821
10          822
10          823
10          824
10          825
10          826
10          827
10          828
10          829
10          830
10          831
10          832
10          833
10          834
10          835
10          836
10          837
10          838
10          839
10          840
10          841
10          842
10          843
10          844
10          845
10          846
10          847
10          848
10          849
10          850
10          851
10          852
10          853
10          854
10          855
10          856
10          857
10          858
10          859
10          860
10          861
10          862
10          863
10          864
10          865
10          866
10          867
10          868
10          869
10          870
10          871
10          872
10          873
10          874
10          875
10          876
10          877
10          878
10          879
10          880
10          881
10          882
10          883
10          884
10          885
10          886
10          887
10          888
10          889
10          890
10          891
10          892
10          893
10          894
10          895
10          896
10          897
10          898
10          899
10          900
10          901
10          902
10          903
10          904
10          905
10          906
10          907
10          908
10          909
10          910
10          911
10          912
10          913
10          914
10          915
10          916
10          917
10          918
10          919
10          920
10          921
10          922
10          923
10          924
10          925
10          926
10          927
10          928
10          929
10          930
10          931
10          932
10          933
10          934
10          935
10          936
10          937
10          938
10          939
10          940
10          941
10          942
10          943
10          944
10          945
10          946
10          947
10          948
10          949
10          950
10          951
10          952
10          953
10          954
10          955
10          956
10          957
10          958
10          959
10          960
10          961
10          962
10          963
10          964
10          965
10          966
10          967
10          968
10          969
10          970
10          971
10          972
10          973
10          974
10          975
10          976
10          977
10          978
10          979
10          980
10          981
10          982
10          983
10          984
10          985
10          986
10          987
10          988
10          989
10          990
10          991
10          992
10          993
10          994
10          995
10          996
10          997
10          998
10          999
10          1000

```

OBJ

```

LINE SOURCE
697 ;SAMPLES HAVE TO BE SUMMED UP AND AVERAGED TO GET THE RESULTANT D.C.
698 ;TERMS AS EXPRESSED IN EQUATION SET (3.7) .
699 ;THE INPUT FUNDAMENTAL FREQUENCY OF THE SIGNAL MUST NOT BE LESS THAN
700 ;45 HZ AND NOT GREATER THAN 65 HZ.
701 ;THE CPU CLK FREQUENCY IS 5 MHZ, THE OPERATIONAL CLOCK FREQUENCY OF
702 ;COUNTER0 AND COUNTER1 IS 2.5 MHZ AND THE ADC CLK FREQUENCY IS 1.25 MHZ.
703 ;THE DATA SAMPLING TIME IS 13.2 MICRO SEC.
704
705 PROCEDURES INVOLVED :
706 MOD_CLK_SYN
707 MOD_CLK_UPDATE
708 DUMMY_READ(ZC_ADC,MOD_CLK_UPDATE_1),
709 ZC_ADC
710 MOD_UPDATE_1
711 AVERAGING(CED),
712 ZC_ADC
713 MOD_UPDATE_1
714 AVERAGING(CED),
715 MOD_CLK_UPDATE_1.
716
717 SCATCH FAD REGISTERS :
718 CHANNEL POINTER.
719 R6-- NUMBER OF NET +VE OR -VE SAMPLES.
720 R7-- RESULTANT VALUE OF THE COUNT_DOWN COUNTER, COUNTER1.
721 R8-- XYP (Xk OR Yk POINTER)
722 R11-- HARMONIC ORDER THAT IS GOING TO BE EXECUTED.
723 R14-- MAX. ORDER OF HARMONIC THAT NEEDS TO BE MEASURED,
724 R15-- SELECTED BY EXTERNAL SWITCH.
725 ZCC THE VALUE OF COUNTER1.
726 ZCCP_ POINTER OF ZCC.
727
728 #####
729
730 L_BEGIN: MOV AL,LED OFF
731 OUT LEDP,AL
732 MOV AL,CHAN_va
733 OUT LEDP,AL
734
735 ;TURN OFF LED.
736
737 ;AT THE BEGINNING OF MEASUREMENT CPU SELECTS
738 ;CHANNEL 6 WHICH ACCESSES Va AS THE FIRST
739 ;CHANNEL TO BE PROCESSED.
740
741
742
743
744
745
746
747
748
749
750
751 MOV CX,9
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000

```

B90900

```

OBJ          LINE      SOURCE
50           752          LA217:  PUSH AX
58           753          POP AX
E2FC        754          LOOP LA217
B036        755          MOV AL,CTR0_CNTL_WORD
E678        756          OUT CTCR,AL
B074        757          MOV AL,CTR1_CNTL_WORD
E678        758          OUT CTCR,AL
B8FFFF     759          MOV AX,0FFFFH
E768        760          OUT CTR1,AX
B080        761          MOV AL,MOD_CLK_0
E640        762          OUT PHASE,AL
E480        763          IN AL,SWP
241F        764          AND AL,HA_ORDER_MASK
BB9414     765          MOV BX,OFFSET R15
8807        766          MOV [BX],AL
B850C3     767          MOV AX,50000D
E760        768          OUT CTR0,AX
E81F04     769          CALL MOD_CLK_SYN
EBF703     770          CALL MOD_CLK_UPDATE
EBE206     771          CALL DUMMY_READ
33F6       772          XOR SI,SI
BB8E14     773          MOV BX,OFFSET R11
8937       774          MOV [BX],SI
BB5E14     775          MOV BX,OFFSET ZCCP
8937       776          MOV [BX],SI
B001       777          MOV AL,1
BB9314     778          MOV BX,OFFSET R14
8807       779          MOV [BX],AL
B90600     780          MOV CX,6
BB8414     781          MOV BX,OFFSET R6

```

; DOWN.

; INITIALIZES COUNTER0 AS SQUARE WAVE, BINARY, MODE 3.

; INITIALIZES COUNTER1 AS RATE GENERATOR, BINARY, MODE 2.

; INITIALIZES COUNTER1 WITH 0FFFFH.

; CHOOSE PHASE 0 DEG MODULATING CLK AT THE BEGINNING, TO MODULATE THE INPUT SIGNAL.

; INPUT FROM EXTERNAL SWITCH PORT TO SEE MAX. ORDER OF HARMONIC THAT NEEDS TO BE MEASURED.

; INITIALIZES THE MODULATING CLK IMPLEMENTED BY COUNTER0 OF 8254 AS 50 HZ WHICH IS EQUIVALENT TO 2.5 MHZ/50 HZ=50 000.

; SYNCHRONIZE MODULATING CLK.

; UPDATE MODULATING CLK.

; GUIDE THE ADC INTO NORMAL OPERATION.

; NULL SI.

; INITIALIZES XYP.

; INITIALIZES ZCCP.

; R14 INITIALIZED WITH FUNDAMENTAL.

; CX, 6 CHANNELS.

; INITIALIZES CHANNEL POINTER WITH CHANNEL

LAC:

```

OBJ          LINE          SOURCE
807          807          ;Va AT THE BEGINNING.
808          808          ;CHANNEL STARTS FROM 6 DOWN TO 1 .
809          809          ;POLL ZC PORT AND OPERATE ADC AT
810          810          ;ZERO PHASE SHIFT MOD_ CLK .
EB6002      811          MOV [BX],CX
812          812          CALL ZC_ADC
813          813          CALL MOD_CLK_UPDATE_1
EB8803      814          MOV AL,MOD_CLK_90
815          815          OUT PHASE,AL
816          816          CALL AVERAGING
817          817          CALL ZC_ADC
818          818          CALL MOD_CLK_UPDATE_1
819          819          CALL ZC_ADC
820          820          CALL MOD_CLK_UPDATE_1
821          821          MOV BX,OFFSET R6
822          822          MOV AX,[BX]
823          823          DEC AX
824          824          CMP AX,0
825          825          JNE L3211
826          826          MOV AL,CHAN_Va
827          827          OUT LEDF,AL
828          828          MOV AL,MOD_CLK_0
829          829          OUT PHASE,AL
830          830          CALL AVERAGING
831          831          MOV BX,OFFSET R6
832          832          MOV CX,[BX]
833          833          LOOP L3211
834          834          MOV BX,OFFSET R15
835          835          MOV DL,[BX]
836          836          MOV BX,OFFSET R14
837          837          MOV AL,[BX]
838          838          CMP AL,DL
839          839          JZ LK21
840          840          INC AL
841          841          MOV [BX],AL
842          842          CALL MOD_CLK_UPDATE_1
843          843          JMP LAC
844          844          ;DL MAX ORDER OF HARMONIC THAT NEEDS TO BE
845          845          ;MEASURED.
846          846          ;AL ORDER OF HARMONIC THAT JUST EXECUTED.
847          847          ;CHECK WHETHER EXECUTED ASSIGNED ORDERS ?
848          848          ; IF FINISH JUMP TO PART 3.
849          849          ;NO
850          850          ;NEXT ORDER OF HARMONIC THAT NEEDS TO BE
851          851          ;MEASURED.
852          852          CALL MOD_CLK_UPDATE_1
853          853          JMP LAC
854          854          ;REPEAT EXECUTE INPUT ROUTINE.
855          855          ;
856          856          ;
857          857          ;
858          858          ;
859          859          ;
860          860          ;
861          861          ;

```

OBJ

LINE SOURCE

```

862 #####
863 #####
864 #####
865 #####
866 #####
867 #####
868 #####
869 #####
870 #####
871 #####
872 #####
873 #####
874 #####
875 #####
876 #####
877 #####
878 #####
879 #####
880 #####
881 #####
882 #####
883 #####
884 #####
885 #####
886 #####
887 #####
888 #####
889 #####
890 #####
891 #####
892 #####
893 #####
894 #####
895 #####
896 #####
897 #####
898 #####
899 #####
900 #####
901 #####
902 #####
903 #####
904 #####
905 #####
906 #####
907 #####
908 #####
909 #####
910 #####
911 #####
912 #####
913 #####
914 #####
915 #####
916 #####
#####
PART : 3
THIS ROUTINE PROCESSES EQUATION SET (3.7) AND IS PROGRAMMED TO CALCULATE
D.C. TERMS OF  $2U_k(\cos \theta_k)/\pi^{(p+1)k}$  AND  $2U_k(\sin \theta_k)/\pi^{(p+1)k}$  IN THE
EQUATION SET (3.7) BASED ON THE METHOD DESCRIBED IN THE SECTION (3_2_3).
EQUATIONS (3.7.6) TO (3.7.8) EACH HAVE TWO D.C. TERMS. THE 2ND TERM
ARISING FROM THE HIGHER HARMONICS COULD BE ELIMINATED BY DIVIDING EQUATIONS
(3.7.18), (3.7.21) AND (3.7.24) BY A FACTOR OF 3 AND THEN SUBTRACTING THEM
FROM EQUATIONS (3.7.6) TO (3.7.8) RESPECTIVELY. BY REPEATING THE SAME
PROCEDURE, THOSE D.C. TERMS WHICH EXIST IN EQUATIONS (3.7.1) TO (3.7.5)
CAN BE ELIMINATED.
THE D.C. TERMS ARE STORED IN MEMORY IN THE FOLLOWING ORDER :
      C 0Vak 90Vak 0Vbk 90Vbk 0Vck 90Vck
          0Iak 90Iak 0Ibk 90Ibk 0Ick 90Ick J
WHERE SUBSCRIPT K IS THE ORDER OF THE HARMONIC.
ACCORDING TO THE ABOVE DATA STRUCTURE, EACH SET OF THE VALUES RELATED
TO A PARTICULAR HARMONIC OCCUPIES 2*2*6 BYTES OF MEMORY IN ADDRESS XY.
THIS MEANS THAT THE STARTING ADDRESS OFFSET OF EACH SET OF DATA
RELATED TO A PARTICULAR HARMONIC IS A MULTIPLE OF 24. ALL DATA ARE
EXPRESSED IN 2'S COMPLEMENT FORM.
EIGHT PROCEDURES ARE NEEDED TO BE PROCESSED IN THIS PART, NAMELY
PROCEDURE "THREE_7_8" DOWN TO "THREE_7_1" .

PROCEDURES INVOLVED :
THREE_7_8(DEHA),
THREE_7_7(DEHA),
THREE_7_6(DEHA),
THREE_7_5(DEHA),
THREE_7_4(DEHA),

```

OBJ

SOURCE

LINE

THREE_7_3(DEHA);
THREE_7_2(DEHA);
THREE_7_1(DEHA);

917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971

SCATCH PAD REGISTERS :

R0_ POINTER FOR CHANNEL.
R1_ LAST D.C. TERM ADDRESS POINTER.
R2_ DIVISOR.
R3_ NEXT D.C. TERM ADDRESS OFFSET.
R5_ POINTER FOR 0 AND 90 DEG.
R6_ GREATEST DIVISOR.

#####

LK21: CALL THREE_7_8
CALL THREE_7_7
CALL THREE_7_6
CALL THREE_7_5
CALL THREE_7_4
CALL THREE_7_3
CALL THREE_7_2
CALL THREE_7_1

E89706
E8D406
E81107
E84E07
E89807
E8E207
E83908
E8AA08

#####

PART : 4

CALCULATE THE AVERAGE INPUT FUNDAMENTAL FREQUENCY OF 6 CHANNELS
BASED ON THE FIRST 12 INPUT VALUES FROM COUNTER1 USING THE FOLLOWING
FREQ*10 = (10*12*2.5E6) / (SUMC ZCC J) ,
WHERE OPERATING FREQUENCY OF COUNTER1 IS 2.5 MHZ, 10 IS A SCALING
FACTOR AND SUMCZCCJ IS THE SUMMATION OF THE 12 INPUT VALUES.

PROCEDURES INVOLVED :

DIV_32 .

#####

L09: MOV BX,OFFSET ZCC
XOR SI,SI
MOV CX,12D

BB6014
33F6
B90C00

;NULL SI.
;CX...NUMBER OF EXECUTING TIMES OF LOOP.

```

LINE SOURCE
1027 ;RB_ NUMBER OF Xk AND Yk THAT NEEDS TO BE MANAGED.
1028 ;
1029 ;#####
1030 ;#####
1031 ;#####
1032 ;#####
1033 ;#####
1034 ;#####
1035 ;#####
1036 ;#####
1037 ;#####
1038 ;#####
1039 ;#####
1040 ;#####
1041 ;#####
1042 ;#####
1043 ;#####
1044 ;#####
1045 ;#####
1046 ;#####
1047 ;#####
1048 ;#####
1049 ;#####
1050 ;#####
1051 ;#####
1052 ;#####
1053 ;#####
1054 ;#####
1055 ;#####
1056 ;#####
1057 ;#####
1058 ;#####
1059 ;#####
1060 ;#####
1061 ;#####
1062 ;#####
1063 ;#####
1064 ;#####
1065 ;#####
1066 ;#####
1067 ;#####
1068 ;#####
1069 ;#####
1070 ;#####
1071 ;#####
1072 ;#####
1073 ;#####
1074 ;#####
1075 ;#####
1076 ;#####
1077 ;#####
1078 ;#####
1079 ;#####
1080 ;#####
1081 ;#####

XOR SI,SI
MOV BX,OFFSET R5
MOV [BX],SI
; NULL SI.
; INITIALIZES AMP AND ANG ADDRESS POINTER.
MOV BX,OFFSET R0
MOV [BX],SI
; INITIALIZES XY ADDRESS POINTER.
XOR AX,AX
; NULL AX.
IN AL,SWP
AND AL,HA_ORDER_MASK
MOV DX,6
MUL DX
; INPUT FROM SWITCH FORT TO SEE THE MAX ORDER
; OF HARMONIC THAT NEEDS TO BE MEASURED.
MOV BX,OFFSET RB
; 6 CHANNELS.
; NUMBER OF Xk & Yk THAT NEEDS TO BE MANAGED.
MOV [BX],AX
; RB NUMBER OF EXECUTING TIMES OF THE LOOP
; WHICH IS EQUAL TO THE PRODUCT OF NUMBER OF
; CHANNELS AND MAX ORDER OF HARMONIC THAT
; NEEDS TO BE MEASURED.
MOV BX,OFFSET R0
MOV SI,[BX]
; SI_ POINTER OF ADDRESS XY.
MOV BX,OFFSET XY
MOV AX,[BX+SI]
; AX_ Xk .
MOV BX,OFFSET R1
MOV [BX],AX
; DI_ Yk .
MOV BX,OFFSET XY
ADD SI,2
MOV DI,[BX+SI]
; CHECK SIGN BIT OF Xk FOR PREPARATION OF
; MULTIPLICATION.
MOV DX,AX
TEST DH,80H
JZ LM11
NEG AX
; Xk ^2 .
MOV DX,AX
MUL DX
; MSW _ Xk ^2 .
MOV BX,OFFSET R3
MOV [BX],DX
; LSW _ Xk ^2 .
MOV BX,OFFSET R4
MOV [BX],DX

```

OBJ

33F6
BB8214
8937

BB7814
8937

33C0

E480

241F

BA0600
F7E2

BB8B14

8907

BB7814
8B37

BBFB11
8E00

BB7A14
8907

BBFB11
83C602
8B38

8ED0

F6C680
7402

F7D8

8ED0
F7E2

BB7E14
8917

BB8014

```

OBJ          LINE          SOURCE
8907        1082        MOV [BX],AX
8BD7        1083        MOV DX,DI
F6C680     1084        TEST DH,80H
7402       1085        JZ LM12
1086       1086        NEG DX
1088       1087        MOV AX,DX
1089       1088        MUL DX
LM12:      1089        MOV DI,[BX]
1090       1090        MOV BX,OFFSET R3
1091       1091        MOV BP,[BX]
1092       1092        ADD AX,DI
1093       1093        ADC DX,BP
1094       1094        CALL SROOT
1095       1095        MOV BX,OFFSET R5
1096       1096        MOV SI,[BX]
1097       1097        MOV BX,OFFSET AMP
1098       1098        MOV [BX+SI],CX
1099       1099        MOV BX,OFFSET R1
1100       1100        MOV AX,AX
1101       1101        AND DX,8000H
1102       1102        JZ LQ91
1103       1103        NEG AX
1104       1104        MOV BP,0
1105       1105        MOV DX,0FFFFH
1106       1106        MUL DX
1107       1107        MOV DI,AX
1108       1108        CALL DIV_32
1109       1109        CALL FANG
1110       1110        ;B* IS BASED ON THE FUNDAMENTAL SCALE. ON HARMONIC SCALE, B*=K*B.
1111       1111        ;B* IS CHECKED AND ADJECED TO THE RANGE OF 0 AND 360 DEG.
1112       1112        XOR AX,AX
1113       1113        IN AL,SWP
1114       1114        AND AL,HA ORDER_MASK
1115       1115        XCHG DI,AX
1116       1116        MUL DI
1117       1117        CMP AX,3600E
1118       1118
1119       1119
1120       1120
1121       1121
1122       1122
1123       1123
1124       1124
1125       1125
1126       1126
1127       1127
1128       1128
1129       1129
1130       1130
1131       1131
1132       1132
1133       1133
1134       1134
1135       1135
1136       1136

```

```

;CHECK SIGN BIT OF YK FOR PREPARATION OF
;MULTIPLICATION.

```

```

;YK ^2 .

```

```

;DI_ Xk ^2 _ LSBY .

```

```

;BP_ Xk ^2 _ MSBY .

```

```

;Xk ^2 + Yk ^2 .

```

```

;SRQ ( Xk ^2 + Yk ^2 ) .

```

```

;STORE ROOT .

```

```

;AX_ Xk WITH SIGN_ BIT .

```

```

;TEST SIGN .

```

```

;+VE Xk .

```

```

;-VE Xk NEEDS TO BE CHANGED TO +VE VALUE .

```

```

;BP_ MSW OF DIVISOR.

```

```

;0FFFFH IS SCALING FACTOR OF DIVIDEND .

```

```

;SCALING .

```

```

;Xk/Ak .

```

```

;FIND ADS[ANG] .

```

```

;B* IS BASED ON THE FUNDAMENTAL SCALE. ON HARMONIC SCALE, B*=K*B.
;B* IS CHECKED AND ADJECED TO THE RANGE OF 0 AND 360 DEG.

```

```

XOR AX,AX
IN AL,SWP
AND AL,HA ORDER_MASK
XCHG DI,AX
MUL DI
CMP AX,3600E

```

```

OBJ          LINE          SOURCE
7303        1137          JNB LQ95
2D100E     1138          SUB AX,3600D
8BF8       1139          MOV DI,AX
BB7814     1140          MOV BX,OFFSET R0
8B37       1141          MOV SI,CBXJ
BBF811     1142          MOV BX,OFFSET XY
BB00       1143          MOV AX,CBX+SIJ
250080     1144          AND AX,8000H
83C602     1145          ADD SI,2
BB10       1146          MOV DX,CBX+SIJ
81E20080  1147          AND DX,8000H
83C602     1148          ADD SI,2
BB7814     1149          MOV BX,OFFSET R0
8937       1150          MOV CBXJ,SI
D1C0       1151          ; SI_ XY ADDRESS INDEX .
D1C0       1152          ; Xk SIGN.
250200     1153          ; MASK OFF OTHER BITS EXCEPT SIGN_ BIT.
D1C2       1154          ; Yk SIGN.
81E20100  1155          ; MASK OFF OTHER BITS EXCEPT SIGN_ BIT.
23D0       1156          ; SI_ NEXT XY POINTER.
33FA00     1157          ; DETERMINE ONE OF FOUR QUADRANTS THE ANGLE BELONGS ACCORDING TO
7503       1158          ; FIG.(3.4)
8B2390     1159          ROL AX,1
33FA00     1160          ROL AX,1
7503       1161          AND AX,2
33FA00     1162          ROL DX,1
7503       1163          AND DX,1
8B2390     1164          ADD DX,AX
33FA00     1165          CMP DX,0
7503       1166          JNE LQ2K
8B2390     1167          JMP LQ0K
33FA00     1168          CMP DX,2
7503       1169          JNE LQ3K
8D0807     1170          MOV BP,1800D
37FD       1171          XCHG DI,BP
2BFD       1172          SUB DI,BP
8B1490     1173          JMP LQ0K
33FA00     1174          CMP DX,3
7503       1175          JNE LQ4K
3D0807     1176          MOV BP,1800D
37FD       1177          XCHG DI,BP
2BFD       1178          SUB DI,BP
8B1490     1179          JMP LQ0K
33FA00     1180          CMP DX,4
7503       1181          JNE LQ4K
1C70807   1182          ADD DI,1800D
B0890     1183          JMP LQ0K
D100E     1184          MOV BP,3600D
77EF      1185          XCHG BP,DI
BFD       1186          SUB DI,BP
B8214    1187          MOV BX,OFFSET R5
B37      1188          MOV SI,CBXJ
1191     1189          ; INDEX OF ANG ADDRESS.
1191     1190
1191     1191

```

```

LINE          SOURCE
1192          MOV BX,OFFSET ANG
1193          MOV [BX+SI],DI
1194          ADD SI,2
1195          MOV BX,OFFSET RS
1196          MOV [BX],SI
1197          MOV BX,OFFSET RB
1198          MOV AX,[BX]
1199          DEC AX
1200          JZ LQR
1201          JMP LQR
1202          MOV BX,OFFSET RB
1203          MOV AX,[BX]
1204          DEC AX
1205          JZ LQR
1206          JMP LQR
1207          MOV BX,OFFSET RS
1208          MOV [BX],SI
1209          DEC AX
1210          JZ LQR
1211          JMP LQR
1212          MOV BX,OFFSET RB
1213          MOV AX,[BX]
1214          DEC AX
1215          JZ LQR
1216          JMP LQR
1217          MOV BX,OFFSET RB
1218          MOV AX,[BX]
1219          DEC AX
1220          JZ LQR
1221          JMP LQR
1222          MOV BX,OFFSET RS
1223          MOV [BX],SI
1224          DEC AX
1225          JZ LQR
1226          JMP LQR
1227          MOV BX,OFFSET RB
1228          MOV AX,[BX]
1229          DEC AX
1230          JZ LQR
1231          JMP LQR
1232          MOV BX,OFFSET RS
1233          MOV [BX],SI
1234          DEC AX
1235          JZ LQR
1236          JMP LQR
1237          MOV BX,OFFSET RB
1238          MOV AX,[BX]
1239          DEC AX
1240          JZ LQR
1241          JMP LQR
1242          MOV BX,OFFSET RS
1243          MOV [BX],SI
1244          DEC AX
1245          JZ LQR
1246          JMP LQR

```

```

OBJ          DBJ
3 BBCC10
3 8938
3 83C602
3 BB8214
3 8937
3 BB8B14
3 8B07
3 48
3 7403
3 E905FF

```

```

#####
PART : 6
CHOOSE THE ANGLE OF THE FUNDAMENTAL COMPONENT OF Va AS THE REFERENCE.
ALL ANGLES OF HARMONIC COMPONENTS REFER TO IT. IF ANY ANGLE IS
LARGE THAN 360 DEGREE, THE CPU ADJUSTS THE ANGLE TO THE RANGE OF
0 TO 360 DEG.
#####
LQR: XOR AX,AX
IN AL,SWP
AND AL,HA_ORDER_MASK
SHL AX,1
MOV BP,AX
MOV DX,3
MUL DX
XOR SI,SI
MOV BX,OFFSET ANG
MOV DX,[BX+SI]
NEG DX
MOV CX,AX
MOV AX,[BX+SI]
ADD AX,DX
MOV [BX+SI],AX
ADD SI,2
LOOP LT31
#####
; NULL AX .
; INPUT FROM SWITCH PORT TO SEE THE MAX ORDER
; OF HARMONIC THAT NEEDS TO BE MEASURED.
; 2*AX
; BP_ 2*AX .
; DX_ 3*AX .
; NULL SI .
; GET ANG. OF Va OF FUNDAMENTAL .
; NEGATIVE IT .
; CX 2*3*AX .
; GET ANG(I) .
; ANG(I) - REFERENCE ANG .
; STORE NEW VALUE OF ANG(I) .
; NEXT ANG ADDRESS INDEX .
; TEST EXECUTING TIMES OF THE LOOP.

```

OBJ	LINE	SOURCE
8 8BCD	1247	MOV CX,BF
A BE0000	1248	MOV SI,0
0 8B00	1250	
F 50	1251	MOV AX,[BX+SI]
0 056009	1252	PUSH AX
3 3D100E	1253	ADD AX,2400D
5 720B	1254	
8 2D100E	1255	CMP AX,3600D
8 3D100E	1256	JB LTB5
E 7203	1257	
0 2D100E	1258	SUB AX,3600D
3 83C602	1259	CMP AX,3600D
5 8900	1260	JB LTB5
3 58	1261	
2 05B004	1262	SUB AX,3600D
0 3D100E	1263	ADD SI,2
7 720B	1264	MOV [BX+SI],AX
1 2D100E	1265	
4 3D100E	1266	POP AX
7 7203	1267	ADD AX,1200D
2 2D100E	1268	CMP AX,3600D
2 83C602	1269	JB LTB6
1 2D100E	1270	
4 3D100E	1271	SUB AX,3600D
7 7203	1272	CMP AX,3600D
2 2D100E	1273	JB LTB6
2 83C602	1274	
2 8900	1275	SUB AX,3600D
1 83C602	1276	ADD SI,2
4 E2C7	1277	MOV [BX+SI],AX
	1278	ADD SI,2
	1279	
	1280	LOOP LTB4
	1281	
	1282	
	1283	
	1284	
	1285	
	1286	
	1287	
	1288	
	1289	
	1290	
	1291	
	1292	
	1293	
	1294	
	1295	
	1296	
	1297	
	1298	
	1299	
	1300	
	1301	

#####

PART : 7

TRANSFER : (1) THE TOTAL NUMBER OF DATA THAT NEEDS TO BE TRANSFERRED,
 [2] AMPLITUDES AND ANGLES OF V & I FROM FUNDAMENTAL TO THE ASSIGNED
 HARMONICS ORDER [MAX 25] AND (3) THE AVERAGE INPUT FREQUENCY TO GPIB
 BUS. THE WHOLE PROGRAM WILL BE REPEATED AFTER THE DATA HAS BEEN
 TRANSFERRED TO THE INTERFACE.

PROCEDURES INVOLVED :

OBJ

SOURCE

LINE

1302 GPBIB,
1303 GPIG,
1304 GPIG1.
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356

SCATCH PAD REGISTERS :

R4_ THE TOTAL NUMBER OF AMPLITUDES OR ANGLES THAT NEEDS TO BE TRANSFERRED
TO GPIB.
INITIALLY THE CONTENT OF R4 =
6*(MAX ORDER OF HARMONIC THAT NEEDS TO BE MEASURED)
AND WILL EVENTUALLY DECREASE TO ZERO.

R5_ THE TOTAL NUMBER OF DATA THAT NEEDS TO BE TRANSFERRED TO GPIB.
INITIALLY THE CONTENT OF R5 =
6*2*(MAX ORDER OF HARMONIC THAT NEEDS TO BE MEASURED) + 1
AND WILL EVENTUALLY DECREASE TO ZERO.

NOTES :

TO UNDERSTAND THIS ROUTINE ONE NEEDS TO CONSULT THE DATA SHEET OF
MC68488 AND IEEE_ 488 BUS SPECIFICATION.

#####

6	33C0	XOR AX,AX	; NULL AX .
3	E480	IN AL,SWP	
3	A 241F	AND AL,HA_ORDER_MASK	;AL_MAX ORDER OF HARMONIC THAT NEEDS ;TO BE MEASURED.
0E	BA0600	MOV DX,6	;6*AX .
	F7E2	MUL DX	
1	BB8014	MOV BX,OFFSET R4	
4	8907	MOV [BX],AX	
5	D1E0	SHL AX,1	;2*6*AX ;+1 .
3	40	INC AX	;2*6*AX ;+1 .
7	BB8214	MOV BX,OFFSET R5	
3	8907	MOV [BX],AX	
5	B009	MOV AL,9	
0	E6E4	OUT 0E4H,AL	; INITIALIZES INTERFACE ADDRESS AS 9 .
2	B080	MOV AL,80H	; RESET GPIB .

OBJ	LINE	SOURCE	
4 E6E3	1357	OUT 0E3H,AL	
3 32C0	1358	XOR AL,AL	
3 E6E3	1359	OUT 0E3H,AL	
1 E6E0	1360	OUT 0E0H,AL	; CLEAR RESET.
3 E6E2	1361	OUT 0E2H,AL	; NO INTERRUPTS .
3 B041	1362	MOV AL,41H	; NO OPTION .
3 E6E5	1363	OUT 0E5H,AL	; SERIAL POLL AND SQR .
3 E4E1	1364	IN AL,0E1H	; SPE OCCURED ?
1 2404	1365	AND AL,4	; NO .
3 74FA	1366	JZ LHT	; YES .
3 E4E1	1367	IN AL,0E1H	; SERIAL POLL END ?
3 2404	1368	AND AL,4	; NO .
3 75FA	1369	JNZ LJT	; YES .
3 32C0	1370	XOR AL,AL	; CLEAR RSV .
3 E6E5	1371	OUT 0E5H,AL	
	1372		
	1373		
	1374		
	1375		
	1376		
	1377		
	1378		
	1379		
	1380		
	1381		
	1382		
	1383		
	1384		
	1385		
	1386		
BB8214	1387	MOV BX,OFFSET R5	
B90100	1388	MOV CX,1	
BE0000	1389	MOV SI,0	
E8E903	1390	CALL GP1B	
	1391		
	1392		
	1393		
	1394		
	1395		
	1396		
BB5C14	1397	MOV BX,OFFSET FREQ	
B90100	1398	MOV CX,1	
BE0000	1399	MOV SI,0	
E8DD03	1400	CALL GP1B	
	1401		
	1402		
	1403		
	1404		
	1405		
	1406		
BB8014	1407	MOV BX,OFFSET R4	
BB0F	1408	MOV CX,1	
BE0000	1409	MOV SI,0	
E80404	1410	CALL GP1B1	
	1411		

; TRANSFER TOTAL NUMBER OF DATA THAT NEEDS TO BE TRANSFERRED :

; TRANSFER FUNDAMENTAL FREQUENCY :

; TRANSFER AMP. AND ANG. :

OBJ

5 E94BFD

SOURCE

JMP LBEGIN ;GO BACK TO THE BEGINNING.

BEGIN ENDP

~~~~~

ZC\_ADC PROC NEAR

#####

THIS PROCEDURE LETS THE CPU FIRST POLL THE ZC PORT UNTIL ZC SWITCHES FROM THE "0" TO THE "1" STATE, THEN THE ADC STARTS OPERATING .

ADC GETS THE SAMPLES FOR ONE PERIOD OF ZC SIGNAL, AND THEN CHECKS EACH SAMPLE TO SEE WHETHER ITS VALUE IS OUT OF THE 0 TO 5 V RANGE. IF IT IS, CPU LIGHTS THE LED TO SHOW OVERFLOW STATUS OF INPUT SIGNAL.

WHILE CHECKING OVERFLOW OPERATION, CPU ALSO MODULATES EACH SAMPLE BY GAIN +1 OR -1 ACCORDING TO ITS SIGN-BIT, D15, WHICH COMES FROM THE SIGN-BIT MODULATOR. IF THE D15 CONTAINS "1", THE CPU WILL CONVERT THE SAMPLE INTO 2'S COMPLEMENT FORM, WHICH MEANS THE SAMPLE IS MULTIPLIED BY NEGATIVE ONE. IF THE D15 CONTAINS "0", THE CPU WILL NOT CHANGE THE SAMPLE, WHICH MEANS THE SAMPLE IS MULTIPLIED BY ONE. AFTER MODULATING THE SAMPLES, CPU SUMS THEM UP AND THEN AVERAGES THEM BY DIVIDING THE SUMMATION VALUE WITH THE TOTAL NUMBER OF SAMPLES INVOLVED IN SUMMATION. AFTER AVERAGING, THE MEAN LEVEL VALUES OF OUTPUT, 00K AND 90UK, ARE OBTAINED. 00K COMES FROM MODULATION AT 0\_DEG. PHASE SHIFT REFERENCE CLOCK AND 90UK COMES FROM MODULATION AT 90\_DEG. CLOCK 00K AND 90UK ARE THEN STORED AT XY ADDRESS OF MEMORY.

THE ADC DOES HAVE OFFSET ERROR WHICH MUST BE ELIMINATED BY SOFTWARE

LINE

- 1412
- 1413
- 1414
- 1415
- 1416
- 1417
- 1418
- 1419
- 1420
- 1421
- 1422
- 1423
- 1424
- 1425
- 1426
- 1427
- 1428
- 1429
- 1430
- 1431
- 1432
- 1433
- 1434
- 1435
- 1436
- 1437
- 1438
- 1439
- 1440
- 1441
- 1442
- 1443
- 1444
- 1445
- 1446
- 1447
- 1448
- 1449
- 1450
- 1451
- 1452
- 1453
- 1454
- 1455
- 1456
- 1457
- 1458
- 1459
- 1460
- 1461
- 1462
- 1463
- 1464
- 1465
- 1466

OBJ

SOURCE

LINE

```

1467  APPROACH.      THE PROCEDURE OF ELIMINATING OFFSET ERROR IS AS FOLLOWS :
1468
1469  LET P1 BE THE ABSOLUTE VALUE OF SAMPLE WITH +VE SIGN_ BIT
1470
1471  LET QJ BE THE ABSOLUTE VALUE OF SAMPLE WITH -VE SIGN_ BIT
1472
1473  LET R1 AND RJ BE THE ABSOLUTE VALUES OF OFFSET ERROR OF ADC ,
1474
1475  WHERE I = 1,2,.....,M
1476
1477  J = 1,2,.....,N
1478
1479  K = I + J
1480
1481  WHERE K IS THE TOTAL NUMBER OF INPUT SAMPLES IN ONE FUNDAMENTAL PERIOD.
1482
1483  TAKE APPROXIMATION, R1 OR RJ = R WHICH WILL BE EQUAL TO THE MIN. ABS.
1484
1485  VALUE OF SAMPLES, THAT IS, R = MIN ( P1 OR QJ ) .
1486
1487  SUM OF SAMPLES = SUMMATION [(+P1 + Ri)] + SUMMATION [(-QJ - Rj)]
1488
1489  = SUMMATION [Pi] - SUMMATION [Qj] + (M-N)*R
1490
1491  THEREFORE,
1492
1493  SUMMATION [Pi] + SUMMATION [Qj] = SUM OF SAMPLES - (M-N)*R
1494
1495  WHERE (M-N) IS THE DIFFERENCE OF THE NUMBER OF SAMPLES WITH +VE SIGN BIT
1496
1497  AND -VE SIGN BIT.
1498
1499  IN SUMMARY, THE TRUE VALUE OF THE SUM OF THE SAMPLES IS EQUAL TO THE SUM
1500
1501  OF THE SAMPLES MINUS THE PRODUCT OF THE DIFFERENCE OF THE NUMBER OF SAMPLES
1502
1503  WITH +VE SIGN BIT & -VE SIGN BIT AND THE SAMPLE WITH MINIMUM ABSOLUTE VALUE.
1504
1505  #####
1506
1507  #####
1508
1509  #####
1510
1511  LA10:  MOV DI,32768D      ;DI THE DIFFERENCE OF THE NUMBER OF SAMPLES
1512
1513
1514
1515  MOV BX,OFFSET R7        ;WITH +VE SIGN_BIT AND -VE SIGN_ BIT STARTING
1516
1517  MOV [BX],DI             ;WITH OFFSET 32768 .
1518
1519
1520
1521  XOR SI,SI               ;NULL SI
1522
1523  MOV BX,OFFSET SAM       ;SAMPLE ADDRESS.
1524
1525  MOV BP,2                ;INCREMENT OF ADDRESS AND +VE SIGN INDEXES.
1526
1527  MOV CL,ZC_MASK_OF_SWP   ;DX ZC ADDRESS .
1528
1529  MOV DX,SWP

```

BF0080  
BB8614  
893F  
33F6  
BB0000  
BD0200  
E140  
BAB000

| OBJ      | LINE | SOURCE                |                                                 |
|----------|------|-----------------------|-------------------------------------------------|
| D EC     | 1522 | IN AL,DX              | : POLL ZC .                                     |
| E 22C1   | 1523 | AND AL,CL             |                                                 |
| 0 75FB   | 1524 | JNZ LA1               | : ZC_ HIGH .                                    |
| 2 B80900 | 1525 | MOV AX,9              |                                                 |
| 5 50     | 1526 | PUSH AX               | : WAIT 10 MICRO SEC FOR ZC SETTLE DOWN.         |
| 6 58     | 1527 | POP AX                |                                                 |
| 7 48     | 1528 | DEC AX                |                                                 |
| 8 75FB   | 1529 | JNZ LA3               |                                                 |
| A EC     | 1530 | IN AL,DX              |                                                 |
| B 22C1   | 1531 | AND AL,CL             |                                                 |
| D 74FB   | 1532 | JZ LA2                | : ZC_ LOW .                                     |
| F E620   | 1533 | OUT GATE,AL           | : ZC_ HIGH                                      |
|          | 1534 |                       | : SYNCHRONIZE MODULATING CLK AND START COUNTER1 |
|          | 1535 |                       | : COUNTING.                                     |
|          | 1536 |                       | : WHEN ZC SWITCHES FROM "0" TO "1" STATE,       |
| 1 BAA000 | 1537 | MOV DX,ADCF           | : ADC STARTS ITS OPERATION.                     |
| 4 ED     | 1538 | IN AX,DX              | : DX_ ADC ADDRESS                               |
| 5 8900   | 1539 | MOV [BX+SI],AX        | : INITIALIZES ADC OPERATION.                    |
|          | 1540 |                       | : FIRST SAMPLE IS INVALID.                      |
| 7 B10A   | 1541 | MOV CL,10D            |                                                 |
| 9 FEC9   | 1542 | DEC CL                | : CL_ NUMBER OF EXECUTING TIMES OF THIS LOOP.   |
|          | 1543 |                       | : ADC TAKES 9 SAMPLES WITHOUT POLL ZC IN ORDER  |
| B 7501   | 1544 | JNZ L3H               | : TO GIVE ZC 120 MICRO SEC TO SETTLE DOWN.      |
| D 90     | 1545 | NOP                   |                                                 |
| E 8900   | 1546 | IN AX,DX              |                                                 |
| 1 03F5   | 1547 | MOV [BX+SI],AX        |                                                 |
| 3 75F7   | 1548 | ADD SI,BP             |                                                 |
| 5 90     | 1549 | DEC CL                |                                                 |
| 7 90     | 1550 | JNZ L3H               |                                                 |
| 8 B140   | 1551 | NOP                   |                                                 |
|          | 1552 | MOV CL,ZC_MASK_OF_ADC |                                                 |
| B 8900   | 1553 | IN AX,DX              |                                                 |
| 0 03F5   | 1554 | MOV [BX+SI],AX        |                                                 |
| 2 84E1   | 1555 | ADD SI,BP             |                                                 |
| 4 90     | 1556 | TEST AH,CL            |                                                 |
| 5 90     | 1557 | JNZ L3A               | : TEST ZC .                                     |
|          | 1558 | NOP                   | : ZC_ HIGH .                                    |
| B 8900   | 1559 | NOP                   | : ZC_ LOW .                                     |
| 0 03F5   | 1560 | MOV CL,9              |                                                 |
| 2 84E1   | 1561 | IN AX,DX              |                                                 |
| 4 90     | 1562 | MOV [BX+SI],AX        |                                                 |
| 5 90     | 1563 | ADD SI,BP             |                                                 |
| 6 B109   | 1564 | TEST AH,CL            |                                                 |
|          | 1565 | JNZ L3A               |                                                 |
|          | 1566 | NOP                   |                                                 |
|          | 1567 | NOP                   |                                                 |
|          | 1568 | NOP                   |                                                 |
|          | 1569 | MOV CL,9              |                                                 |
| 8 ED     | 1570 | IN AX,DX              | : CL_ NUMBER OF EXECUTING TIMES OF THIS LOOP.   |
| 9 8900   | 1571 | MOV [BX+SI],AX        | : ADC TAKES 9 SAMPLES WITHOUT POLL ZC IN ORDER  |
| B 03F5   | 1572 | ADD SI,BP             | : TO GIVE ZC 120 MICRO SEC TO SETTLE DOWN.      |
| D FEC9   | 1573 | DEC CL                |                                                 |
|          | 1574 |                       |                                                 |
|          | 1575 |                       |                                                 |
|          | 1576 |                       |                                                 |

| OBJ        | LINE | SOURCE                |
|------------|------|-----------------------|
| F 1 75F7   | 1577 | JNZ L3F               |
| F 1 90     | 1578 | NOP                   |
| F 2 3 B140 | 1579 | NOP                   |
| S 5 ED     | 1580 | MOV CL,ZC_MASK_OF_ADC |
| S 8 03F5   | 1581 | IN AX,DX              |
| A 4 84E1   | 1582 | MOV [BX+SI],AX        |
| A 4 74F7   | 1583 | ADD SI,BP             |
|            | 1584 | TEST AH,CL            |
|            | 1585 | JZ L3C                |
|            | 1586 |                       |
|            | 1587 |                       |
|            | 1588 |                       |
| E 0 D1EE   | 1589 | IN AX,CTR1            |
|            | 1590 | SHR SI,1              |
| 2 BBA406   | 1591 | MOV BX,1700D          |
| 3 3BF3     | 1592 | CMF SI,BX             |
| 7 7202     | 1593 | JB L395               |
| 7 EB8D     | 1594 | JMP LA10              |
|            | 1595 |                       |
|            | 1596 |                       |
|            | 1597 |                       |
|            | 1598 |                       |
|            | 1599 |                       |
|            | 1600 |                       |
|            | 1601 |                       |
|            | 1602 |                       |
|            | 1603 |                       |
|            | 1604 |                       |
| 3 BB4C04   | 1605 | MOV BX,1100D          |
| 3 3BF2     | 1606 | CMF SI,BX             |
| 3 7702     | 1607 | JA L395               |
| 3 EB84     | 1608 | JMP LA10              |
|            | 1609 |                       |
|            | 1610 |                       |
|            | 1611 |                       |
|            | 1612 |                       |
|            | 1613 |                       |
|            | 1614 |                       |
|            | 1615 |                       |
|            | 1616 |                       |
|            | 1617 |                       |
|            | 1618 |                       |
| 1 8B00     | 1619 | MOV DX,AX             |
| 3 8BFFF    | 1620 | MOV AX,0FFFFH         |
| 3 2BC2     | 1621 | SUB AX,DX             |
| 3 8B8814   | 1622 | MOV BX,OFFSET RB      |
| 3 8907     | 1623 | MOV [BX],AX           |
|            | 1624 |                       |
|            | 1625 |                       |
| 1 56       | 1626 | PUSH SI               |
|            | 1627 |                       |
| 1 8B5E14   | 1628 | MOV BX,OFFSET ZCCP    |
| 1 8B37     | 1629 | MOV SI,[BX]           |
| 3 83FE18   | 1630 | CMF SI,24D            |
| 3 740D     | 1631 | JE L321               |

```

;TEST ZC:
;ZC_ LOW:

```

```

;ZC_ HIGH. LASTEST VALUE FROM COUNTER1.
;GETS THE LASTEST VALUE FROM COUNTER1.
;SI=SI/2, SI_ TOTAL NUMBER OF SAMPLES:

```

```

;CHECK TO SEE WHETHER THE FREQUENCY OF ZC
;SIGNAL, THAT IS, THE FREQUENCY OF FUNDAMENTAL
;IS ABOVE 45 HZ WHICH IS EQUIVALENT TO THE
;NUMBER OF INPUT SAMPLES, 1700 (5 MHZ/66*45 HZ),
;IN WHICH 66 IS THE NUMBER OF CPU CYCLES NEEDED
;TO EXECUTE THE INPUT ROUTINE OF ADC.
;FREQUENCY OF ZC IS BELOW 45 HZ, REPEAT THE
;OPERATION UNTIL IT MATCHES THE REQUIREMENT .

```

```

;CHECK TO SEE WHETHER THE FREQUENCY OF ZC
;SIGNAL, THAT IS, THE FREQUENCY OF FUNDAMENTAL
;IS BELOW 65 HZ WHICH IS EQUIVALENT TO THE
;NUMBER OF INPUT SAMPLES, 1100 (5 MHZ/66*65 HZ),
;IN WHICH 66 IS THE NUMBER OF CPU CYCLES NEEDED
;TO EXECUTE THE INPUT ROUTINE OF ADC.
;FREQUENCY OF ZC IS ABOVE 65 HZ, REPEAT THE
;OPERATION UNTIL IT MATCHES THE REQUIREMENT .

```

```

;START VALUE OF COUNTER1 = 0FFFFH .
;AX_ RESULTANT VALUE OF COUNTER1.

```

```

;RB_ RESULTANT VALUE OF COUNTER1.

```

```

;STORE FIRST 12 COUNTS OR COUNTER1.

```

```

OBJ          BB6014
             89000
             83C602
             BB5E14
             8937
             5E
             C3

LINE         SOURCE
1632         MOV BX,OFFSET ZCC
1633         MOV [BX+SI],AX
1634         ADD SI,2
1635
1636         MOV BX,OFFSET ZCCP
1637         MOV [BX],SI
1638
1639         POP SI
1640
1641         RET
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686

             ; NEXT ADDRESS POINTER.

L321:
ZC_ADC      ENDF

=====
#####
THIS PROCEDURE CHECKS FOR OVERFLOW OF THE INPUT SIGNAL AND MODULATES
SAMPLES WITH GAIN +1 AND -1 ACCORDING TO SIGN-BIT.      IT ALSO
ELIMINATES THE OFFSET ERROR ACCORDING TO THE METHOD USED IN "ZC_ADC" .
#####

AVERAGING   PROC    NEAR

MOV DI,0FFFFH
             ; DI MINIMUM OFFSET ERROR, THE 1ST SEED IS
             ; 0FFFFH .
MOV AX,SI
PUSH AX
             ; THE CONTENT OF SI IS FROM ZC_ADC PROC .
             ; SAVE TOTAL NUMBER OF SAMPLES IN STACK.
XOR CX,CX
             ; CX NULL LSBY OF SUM OF SUMMATION OF ALL
             ; MODULATED SAMPLES.
XOR BP,BP
             ; BP NULL MSBY OF SUM OF SUMMATION OF ALL
             ; MODULATED SAMPLES.
MOV BX,OFFSET SAM
XOR SI,SI
JMP L4C
             ; NULL SI.
LLED:       CALL LED
             ; OVERFLOW.
L4C:        PUSH AX
             ; SAVE NUMBER OF EXECUTING TIMES OF THIS LOOP.
MOV AX,[EX+SI]
             ; AX ORIGINAL SAMPLE.

```

```

OBJ          LINE          SOURCE
83C602      1687      ADD SI,2
88DB       1688      MOV BX,AX
81E3FF0F   1689      AND BX,SAMPLE_MASK
56         1690      PUSH SI
8BF3       1691      MOV SI,BX
81FBFF0F   1692      CMP BX,SAMPLE_MASK
74EB       1693      JE LLED
1694
3BDE       1695      CMP BX,DI
7302       1696      JNB L4A
87DF       1697      XCHG BX,DI
1699
96         1700      XCHG AX,SI
57         1701      PUSH DI
1702
8B8614     1703      MOV BX,OFFSET R7
8B3F       1704      MOV DI,[BX]
1705
81E60080   1706      AND SI,SIGN_BIT_MASK
1707
7409      1708      JZ L4B
4F         1709      DEC DI
1710
BAFFFF     1711      MOV DX,0FFFFH
E7D8      1712      NEG AX
EB0490    1713      JMP L4BB
47         1714      INC DI
33D2      1715      XOR DX,DX
893F      1716      MOV [BX],DI
5F         1717      POP DI
03CB      1718      ADD CX,AX
13EA      1719      ADC BP,DX
5E         1720      POP SI
BB0000    1721      MOV BX,OFFSET SAM
58         1722      POP AX
48         1723      DEC AX
75BD      1724      JNZ L4C
BB8614    1725      MOV BX,OFFSET R7
8B07      1726      MOV AX,[BX]
1740
1741
; NEXT ADDRESS INDEX OF SAMPLES.
; BX_ ABS [SAM]
; SAVE ADDRESS INDEX OF SAMPLES IN STACK.
; SI_ ABS [SAM ]
; CHECK OVERFLOW.
; OVERFLOW.
; LOOK FOR MIN. ABS [SAM] AS OFFSET ERROR.
; DI_ MINIMUM OFFSET ERROR.
; SI_ ORIGINAL SAMPLES, AX_ ABS [SAM] .
; DI_ NUMBER OF NET +VE OR -VE SAMPLES WITH
; OFFSET 32768 .
; MODULATE SAMPLES WITH GAIN +1 OR -1 ACCORDING
; TO SIGN_ BIT .
; +VE SIGN_ BIT, D15_ ZERO .
; -VE SAMPLE, DI-1 .
; -VE SIGN_ BIT, D15_ ZERO, NEGATE THE SAMPLE
; INTO 2'S COMP. FORM.
; +VE SAMPLE, DI+1 .
; MSBY OF +VE MODULATED SAMPLE.
; SAVE NUMBER OF NET +VE OR -VE SAMPLES WITH
; OFFSET 32768 IN R7.
; DI_ MINIMUM OFFSET ERROR.
; SUM THE SAMPLES_ LSBY :
; SUM THE SAMPLES_ MSBY :
; SI_ ADDRESS INDEX OF SAMPLES.
; AX_ NUMBER OF EXECUTING TIMES OF THIS LOOP.
; DECREASE LOOP TIMES.
; AX_ NUMBER OF NET +VE OR -VE SAMPLES WITH

```

| OBJ      | LINE | SOURCE                                                                |
|----------|------|-----------------------------------------------------------------------|
|          | 1742 | ; OFFSET 32768 .                                                      |
| BA0080   | 1743 | MOV DX, 32768D                                                        |
| 3BC2     | 1744 | CMP AX, DX                                                            |
| 7211     | 1745 | JB L4                                                                 |
|          | 1746 |                                                                       |
|          | 1747 |                                                                       |
|          | 1748 | ; 32768 < AX .                                                        |
| 2BC2     | 1749 | SUB AX, DX                                                            |
|          | 1750 |                                                                       |
| F7E7     | 1751 | MUL DI                                                                |
|          | 1752 |                                                                       |
| F7D0     | 1753 | NOT AX                                                                |
| F7D2     | 1754 | NOT DX                                                                |
| 050100   | 1755 | ADD AX, 1                                                             |
| 83D200   | 1756 | ADC DX, 0                                                             |
|          | 1757 |                                                                       |
|          | 1758 |                                                                       |
|          | 1759 |                                                                       |
| EB0690   | 1760 | JMP L5                                                                |
|          | 1761 |                                                                       |
| 92       | 1762 | XCHG DX, AX                                                           |
| 2BC2     | 1763 | SUB AX, DX                                                            |
| F7E7     | 1764 | MUL DI                                                                |
|          | 1765 |                                                                       |
|          | 1766 |                                                                       |
|          | 1767 |                                                                       |
| 03C8     | 1768 | ; SUM OF SAMPLES + (MINIMUM OFFSET ERROR)*(NUMBER OF NET -VE SAMPLES) |
| 13EA     | 1769 | ADD CX, AX                                                            |
|          | 1770 | ADC BF, DX                                                            |
|          | 1771 |                                                                       |
| 8BD5     | 1772 | MOV DX, BF                                                            |
| 8BF9     | 1773 | MOV DI, CX                                                            |
| 8BC2     | 1774 | MOV AX, DX                                                            |
| 250080   | 1775 | AND AX, 8000H                                                         |
| 740E     | 1776 | JZ L41                                                                |
|          | 1777 |                                                                       |
|          | 1778 |                                                                       |
|          | 1779 |                                                                       |
| 83EF01   | 1780 | SUB DI, 1                                                             |
| 83D400   | 1781 | SBB DX, 0                                                             |
| F7D7     | 1782 | NOT DI                                                                |
| F7D2     | 1783 | NOT DX                                                                |
| 81C20080 | 1784 | ADD DX, 8000H                                                         |
|          | 1785 |                                                                       |
|          | 1786 |                                                                       |
|          | 1787 |                                                                       |
| 59       | 1788 | POP CX                                                                |
| BD0000   | 1789 | MOV BF, 0                                                             |
|          | 1790 |                                                                       |
| EBD300   | 1791 | CALL DIV_32                                                           |
|          | 1792 |                                                                       |
| 81E20080 | 1793 | AND DX, 8000H                                                         |
| 7402     | 1794 | JZ L42                                                                |
|          | 1795 |                                                                       |
| F7DF     | 1796 | NEG DI                                                                |

```

OBJ          LINE          SOURCE
BB8E14      1797      MOV BX,OFFSET R11
8B37        1798      MOV SI,[BX]
           1799
BBF811      1800      MOV BX,OFFSET XY
8938        1801      MOV [BX+SI],DI
83C602      1802      ADD SI,2
BB8E14      1803
8937        1804      MOV BX,OFFSET R11
           1805      MOV [BX],SI
           1806      RET
C3          1807
           1808
           1809
           1810
           1811
           1812
           1813
           1814
           1815
           1816
           1817
           1818
           1819
           1820
           1821
           1822
           1823
           1824
           1825
           1826
           1827
           1828
           1829
           1830
           1831
           1832
           1833
           1834
           1835
           1836
           1837
           1838
           1839
           1840
           1841
           1842
           1843
           1844
           1845
           1846
           1847
           1848
           1849
           1850
           1851

BB8E14      1797      MOV BX,OFFSET R11
8B37        1798      MOV SI,[BX]
           1799
BBF811      1800      MOV BX,OFFSET XY
8938        1801      MOV [BX+SI],DI
83C602      1802      ADD SI,2
BB8E14      1803
8937        1804      MOV BX,OFFSET R11
           1805      MOV [BX],SI
           1806      RET
C3          1807
           1808
           1809
           1810
           1811
           1812
           1813
           1814
           1815
           1816
           1817
           1818
           1819
           1820
           1821
           1822
           1823
           1824
           1825
           1826
           1827
           1828
           1829
           1830
           1831
           1832
           1833
           1834
           1835
           1836
           1837
           1838
           1839
           1840
           1841
           1842
           1843
           1844
           1845
           1846
           1847
           1848
           1849
           1850
           1851

           AVERAGING      ENDP
           ;
           =====
MOD_CLK_UPDATE_1      PROC      NEAR
;#####
;THIS PROCEDURE NOTIFIES COUNTER 0 TO GENERATE A MODULATING CLK WITH
;ASSIGNED HARMONIC FREQUENCY.
;#####
;#####
PUSH AX
PUSH BX
PUSH CX
PUSH DX
MOV BX,OFFSET R8
MOV AX,[BX]
XOR CX,CX
MOV BX,OFFSET R14
MOV CL,[BX]
XOR DX,DX
DIV CX
OUT CTR0,AX
POP DX
POP CX
POP BX
;CX... ORDER OF HARMONIC.
;GENERATE MODULATING CLK.

```

OBJ

58

C3

LINE

1852  
1853  
1854  
1855  
1856  
1857  
1858  
1859  
1860  
1861  
1862  
1863  
1864  
1865  
1866  
1867  
1868  
1869  
1870  
1871  
1872  
1873  
1874  
1875  
1876  
1877  
1878  
1879  
1880  
1881  
1882  
1883  
1884  
1885  
1886  
1887  
1888  
1889  
1890  
1891  
1892  
1893  
1894  
1895  
1896  
1897  
1898  
1899  
1900  
1901  
1902  
1903  
1904  
1905  
1906

SOURCE

POP AX

RET

MOD\_CLK\_UPDATE\_1            ENDP

=====

#####

THIS PROCEDURE POLLS THE ZC PORT UNTIL ZC SIGNAL SWITCHES FROM THE LOW STATE TO THE HIGH STATE.        THEN IT SYNCHRONIZES THE MODULATING CLOCK IMMEDIATELY AND UPDATES THE VALUE OF COUNTER0.

#####

MOD\_CLK\_UPDATE    PROC        NEAR

B0FFFF

B140  
BA8000

EC  
22C1  
75FB

B80900

50  
58  
48  
75FB

EC  
22C1  
74FB

E568  
2BE8  
8BC5

E760

MOV BP,0FFFFH            ;COUNTER1 IS COUNT\_DOWN COUNTER, START AT  
MOV CL,ZC\_MASK\_OF\_SWP    ;0FFFFH  
MOV DX,SWP                ;DX\_ ZC PORT.  
  
LA215:    IN AL,DX            ; POLL ZC .  
          AND AL,CL            ; ZC\_ HIGH .  
          JNZ LA215  
  
          MOV AX,9             ; ZC\_ LOW.  
          PUSH AX             ; WAIT 10 MICRO SEC FOR ZC SETTLE DOWN.  
          POP AX  
          DEC AX  
          JNZ LA216  
  
LA216:    IN AL,DX            ; POLL ZC .  
          AND AL,CL            ; ZC\_ LOW.  
          JZ LA214  
  
          IN AX,CTR1          ; ZC\_ HIGH.  
          SUB BP,AX            ; INPUT VALUE FROM COUNTER1.  
          MOV AX,BP            ; WORK OUT THE VALUE.  
  
          OUT CTR0,AX         ; UPDATE COUNTER0 .

```

1907 LINE SOURCE
1908 OUT GATE,AL ;SYNCHRONIZE THE MODULATING CLK .
1909 RET
1910
1911 MOD_CLK_UPDATE ENDP
1912
1913 =====
1914
1915 #####
1916 ;THIS PROCEDURE FOLLS THE ZC PORT UNTIL ZC SIGNAL SWITCHES FROM THE LOW TO
1917 ;THE HIGH STATE. THEN IT SYNCHRONIZES THE MODULATING CLK IMMEDIATELY.
1918 ;#####
1919
1920 MOD_CLK_SYN PROC NEAR
1921 MOV CL,ZC_MASK_OF__SWF ;DX_ ZC PORT.
1922 MOV DX,SWF ;POLL ZC .
1923 LA17: IN AL,DX ;ZC_ HIGH.
1924 AND AL,CL ;ZC_ LOW.
1925 JNZ LA17 ;WAIT 10 MICRO SEC FOR ZC SETTLE DOWN.
1926
1927 MOV AX,9 ;POLL ZC .
1928 PUSH AX ;ZC_ LOW.
1929 POP AX ;WAIT 10 MICRO SEC FOR ZC SETTLE DOWN.
1930 DEC AX
1931 JNZ LA171
1932
1933 LA27: IN AL,DX ;POLL ZC .
1934 AND AL,CL ;ZC_ LOW.
1935 JZ LA27
1936 OUT GATE,AL ;ZC_ HIGH , SYNCHRONIZE MODULATING CLK.
1937 RET
1938
1939 MOD_CLK_SYN ENDP
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961

```

OBJ

E620

C3

B140  
BAB000

EC  
22C1  
75FB

B80900  
50  
58  
48  
75FB

EC  
22C1  
74FB

E620

C3

```

OBJ          LINE          SOURCE
=====
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016

BB8414      MOV BX,OFFSET R6
BB807       MOV AX,[BX]
           ; AX_ DIVISOR.
BB7C14      MOV BX,OFFSET R2
BB707       MOV [BX],AX
           ; R2_ DIVISOR.
33FF       XOR DI,DI
           ; DI_ SUM, INITIALIZED WITH ZERO.
BBF811      MOV BX,OFFSET XY
BB800       MOV AX,[BX+SI]
           ; AX_ X<OR Y<.
BB7E14      MOV BX,OFFSET R3
BB17        MOV DX,[BX]
2BF2       SUB SI,DX
           ; DX_ NEXT ADDRESS OFFSET.
           ; SI_ NEXT ADDRESS INDEX.
BB7C14      MOV BX,OFFSET R2
BB0F        MOV CX,[BX]
8BD1       MOV DX,CX
83EA02     SUB DX,2
8917       MOV [BX],DX
           ; CX_ DIVISOR LSBY .
           ; DX_ DIVISOR.
           ; DX_ NEXT DIVIDER.
8BD0       MOV DX,AX
80E680     AND DH,80H
7402      JZ LAGM
           ; CHECK SIGN BIT OF X<OR Y< FOR PREPARATION
           ; OF DIVISION.
F7D8       NEG AX
52         PUSH DX
33D2       XOR DX,DX
F7F1       DIV CX
59         POP CX
F6C680     TEST DH,80H
7402      JZ LAGM
           ; OF DIVISION.
F7D8       NEG AX

```

```

#####
; THIS PROCEDURE ELIMINATES D.C. TERMS DERIVED FROM THE HIGH HARMONICS
; WHICH EXISTS IN THE MEAN LEVEL OUTPUT GENERATED BY MODULATING THE LOW
; HARMONICS SIGNAL.
#####

```

```

DEHA      PROC NEAR
MOV BX,OFFSET R6
MOV AX,[BX]
           ; AX_ DIVISOR.
MOV BX,OFFSET R2
MOV [BX],AX
           ; R2_ DIVISOR.
XOR DI,DI
           ; DI_ SUM, INITIALIZED WITH ZERO.
MOV BX,OFFSET XY
MOV AX,[BX+SI]
           ; AX_ X<OR Y<.
MOV BX,OFFSET R3
MOV DX,[BX]
SUB SI,DX
           ; DX_ NEXT ADDRESS OFFSET.
           ; SI_ NEXT ADDRESS INDEX.
MOV BX,OFFSET R2
MOV CX,[BX]
MOV DX,CX
SUB DX,2
MOV [BX],DX
           ; CX_ DIVISOR LSBY .
           ; DX_ DIVISOR.
           ; DX_ NEXT DIVIDER.
MOV DX,AX
AND DH,80H
JZ LAGM
           ; CHECK SIGN BIT OF X<OR Y< FOR PREPARATION
           ; OF DIVISION.
NEG AX
PUSH DX
XOR DX,DX
DIV CX
POP CX
TEST DH,80H
JZ LAGM
           ; OF DIVISION.
NEG AX

```

```

LAGM:
MOV DX,AX
AND DH,80H
JZ LAGM
NEG AX
PUSH DX
XOR DX,DX
DIV CX
POP CX
TEST DH,80H
JZ LAGM
NEG AX

```



```

OBJ          SOURCE
03F8        LACN:  ADD DI,AX           ;DI_ SUM.
8B07        MOV AX,[BX]           ;CHECK TO SEE WHETHER THE 1ST D.C. OF
          CMP AX,1                ;EQUATION ARISES?
          JNE LQA                 ;NO.
F7DF        NEG DI               ;YES, NEGATIVE THE SUM IN 2'S COMP. FORM.
          MOV BX,OFFSET XY
          MOV AX,[BX+SI]
          ADD AX,DI
          MOV [BX+SI],AX
          MOV BX,OFFSET R1
          MOV SI,[BX]
          ADD SI,2
          MOV [BX],SI
          MOV BX,OFFSET R5
          MOV CX,[BX]
          RET
          DEHA  ENDF

          ;=====
          ;#####
          ;32_ BIT BY 32_ BIT DIVISION PROCEDURE USING THE SUBTRACT_ AND_ TEST
          ;METHOD.
          ;THIS PROCEDURE DIVIDES THE 32_BIT QUANTITY IN REGISTER PAIR DX AND DI BY
          ;THE 32_BIT QUANTITY IN REGISTER PAIR BP AND CX .    THE RESULT WILL BE
          ;STORED IN REGISTER PAIR DX AND DI AND THE REMAINDER IN REGISTER PAIR
          ;BP AND CX WHEN THE 8088 RETURNS FROM THE PROCEDURE.
          ;THE SUBTRACT_ AND_ TEST METHOD WAS DESCRIBED IN TWO BOOKS, [ 36,37 ] .
          ;SUBTRACT_ AND_ TEST METHOD :

```

```

LINE
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071

```

```

03F8
8B07
$D0100
75C9
F7DF
8BF811
8B00
03C7
8900
8B7A14
8B37
83C602
8937
8B8214
8B0F
C3

```

OBJ

SOURCE

IN BINARY DIVISION, THE DIVISOR WAS SUBTRACTED FROM THE FIRST BIT OF  
 THE DIVIDEND. IF A BORROW OCCURRED AS A RESULT OF THE SUBTRACTION,  
 WHICH IT DID, A "0" IS ENTER IN THE QUOTIENT, AND THE DIVISOR IS ADDED TO  
 THE RESULT OF THE SUBTRACTION SO THAT THE ORIGINAL VALUE OF THE DIVIDEND  
 IS RESTORED. IF NO BORROW OCCURS DURING THE SUBTRACTION, A "1" IS  
 ENTERED INTO THE QUOTIENT, AND THE RESULT OF THE SUBTRACTION IS USED FOR  
 THE NEXT SUBTRACT\_AND\_TEST PROCESS.  
 FOR EXAMPLE, DIVIDES 1101 0010 BY 101 :

```

00 1101 0010 DIVIDEND
-10 1000 0000 DIVISOR
-----
10 0101 0010 BORROW OCCURS; QUOTIENT BIT = 0 ,
+10 1000 0000 SO ADD DIVISOR TO RESULT.
-----
00 1101 0010
- 1 0100 0000 SHIFT DIVISOR , TRY AGAIN.
-----
11 1001 0010 BORROW OCCURS; QUOTIENT BIT = 0 ,
+ 1 0100 0000 SO ADD DIVISOR TO RESULT.
-----
00 1101 0010
- 1010 0000 SHIFT DIVISOR , TRY AGAIN.
-----
00 0011 0010 NO BORROW , QUOTIENT BIT = 1.
- 101 0000 NO ADDITION , SHIFT DIVISOR ;TRY AGAIN .
-----
11 1110 0010 BORROW OCCURS; QUOTIENT BIT = 0 ,
+ 101 0000 SO ADD DIVISOR TO RESULT.
-----
00 0011 0010
- 10 1000 SHIFT DIVISOR , TRY AGAIN.
-----
00 0000 1010 NO BORROW , QUOTIENT BIT = 1.
- 1 0100 NO ADDITION , SHIFT DIVISOR ;TRY AGAIN .
-----
11 1111 0110 BORROW OCCURS; QUOTIENT BIT = 0 ,
+ 1 0100 SO ADD DIVISOR TO RESULT.
-----
00 0000 1010
- 1010 SHIFT DIVISOR , TRY AGAIN.
-----
00 0000 0000 NO BORROW , QUOTIENT BIT = 1.
- 101 NO ADDITION , SHIFT DIVISOR ;TRY AGAIN .
-----
11 1111 1011 BORROW OCCURS; QUOTIENT BIT = 0 ,
+ 101 SO ADD DIVISOR TO RESULT.
  
```

LINE 2072  
 2073  
 2074  
 2075  
 2076  
 2077  
 2078  
 2079  
 2080  
 2081  
 2082  
 2083  
 2084  
 2085  
 2086  
 2087  
 2088  
 2089  
 2090  
 2091  
 2092  
 2093  
 2094  
 2095  
 2096  
 2097  
 2098  
 2099  
 2100  
 2101  
 2102  
 2103  
 2104  
 2105  
 2106  
 2107  
 2108  
 2109  
 2110  
 2111  
 2112  
 2113  
 2114  
 2115  
 2116  
 2117  
 2118  
 2119  
 2120  
 2121  
 2122  
 2123  
 2124  
 2125  
 2126

```

LINE      OBJ      SOURCE
1277      -----
1278      00 0000 0000
1279      EIGHT SHIFTS AND SUBTRACTIONS HAVE BEEN PERFORM, SO THE DIVIDEND
1280      HAS BEEN DIVIDED BY THE QUOTIENT.      THE RESULT IS (0010 1010) .
1281      #####
1282      DIV_32  PROC      NEAR
1283
1284      PUSH SI
1285      MOV AX,8000H
1286      AND AX,DX
1287      PUSH AX
1288      PUSH BX
1289      MOV SI,CX
1290      MOV AX,BF
1291      MOV BX,33D
1292      XOR BF,BF
1293
1294      XOR CX,CX
1295      AND DX,7FFFH
1296
1297      NXTBIT:  RCL DI,1
1298              RCL DX,1
1299
1300      DEC BX
1301      JZ L112
1302
1303      RCL CX,1
1304
1305      RCL BF,1
1306      SUB CX,SI
1307
1308      SBB BF,AX
1309
1310      JNC NOADD
1311
1312      ADD CX,SI
1313      ADC BF,AX
1314
1315      NOADD:  CMC
1316
1317      ; MASK OF SIGN_ BIT.
1318      ; SAVE SIGN_ BIT
1319      ; SI_ MSBY OF THE DIVISOR.
1320      ; AX_ MSBY OF THE DIVISOR.
1321      ; BX_ DIVISOR'S BIT VALUE, START VALUE,33.
1322      ; NUCL PAIR BF AND CX THEY WILL USED TO STORE
1323      ; THE PARTIAL DIVIDEND.
1324
1325      ; ROTATE THE LSB OF DIVIDEND INTO THE CARRY.
1326      ; ROTATE THE MSB OF DIVIDEND INTO THE CARRY.
1327      ; BX_ DECREMENT THE BIT COUNT.
1328      ; RETURN IF VALUE IS 0 .
1329
1330      ; OTHERWISE , ROTATE THE MSB OF THE DIVISOR
1331      ; INTO THE PARTIAL DIVISOR STORED IN REGISTERS
1332      ; BF AND CX .
1333
1334      ; SUBTRACT THE LSB OF DIVISOR FROM LSBY OF
1335      ; PARTIAL DIVIDEND.
1336
1337      ; SUBTRACT WITH BORROW THE DIVISOR FROM MSBY
1338      ; OF PARTIAL DIVIDEND.
1339
1340      ; IF THE CARRY IS 0, DO NOT ADD THE DIVISOR TO.
1341
1342      ; THE RESULT OF THE PREVIOUS SUBTRACTION THE
1343      ; DIVISOR MUST BE ADDED TO THE RESULT OF THE
1344      ; SUBTRACTION SO THAT THE PREVIOUS VALUE OF
1345      ; PARTIAL DIVIDEND IS RE-ESTABLISHED .
1346
1347      ; COMPLEMENT THE CARRY.

```

DBJ  
 BEB  
 DB  
 13D0  
 JE  
 13

```

LINE SOURCE
2182 JMP NXTBIT ; THEN TEST ANOTHER BIT IN THE DIVISOR.
2183
2184 POP BX ; AX SIGN BIT.
2185 POP AX ; RECOVER SIGN_BIT OF DIVIDEND.
2186 ADD DX,AX
2187 POP SI
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228
2229
2230
2231
2232
2233
2234
2235
2236
    
```

DIV\_32 ENDF

-----

WHEN PROCEDURE DIV\_32 IS CALLED, THE DIVIDEND MUST BE CONTAINED IN THE REGISTER PAIR DX AND DI AND THE DIVISOR MUST BE IN REGISTER PAIR BP AND CX. THE BIT COUNT IS 33 BECAUSE THERE ARE 32 BITS IN THE DIVIDEND, AND THE ROTATE LOOP WITHIN THE PROCEDURE MUST BE EXECUTED AN ADDITIONAL TIME SO THAT THE LAST BIT OF THE QUOTIENT IS SAVED IN THE APPROPRIATE REGISTER PAIR. REGISTER BP AND CX IS THEN CLEARED BECAUSE THIS IS THE REGISTER PAIR THAT IS USED TO HOLD THE PARTIAL DIVIDEND. THE 32 BIT DIVIDEND CONTAINED IN REGISTER PAIR DX AND DI IS THEN ROTATED ONCE TO THE LEFT. THE CARRY IS EITHER A LOGIC 1 OR A LOGIC 0 AS A RESULT OF THIS ROTATION. THIS SEQUENCE OF TWO INSTRUCTIONS NOT ONLY ROTATES THE MSB OF THE DIVIDEND INTO THE CARRY, BUT IT ALSO CAUSES THE CARRY TO BE ROTATED INTO THE LSB OF REGISTER PAIR DX AND DI. THIS TECHNIQUE IS USED TO ROTATE THE QUOTIENT, BIT-BY-BIT, INTO REGISTER PAIR DX AND DI. AFTER THE DIVIDEND HAS BEEN ROTATED, THE BIT COUNT STORED IS DECREMENTED. WHEN THE COUNT REACHES ZERO, THE PROCEDURE IS COMPLETED. IF THE COUNT IS NONZERO AFTER THE DEC BX INSTRUCTION IS EXECUTED, THE JZ INSTRUCTION IS NOT EXECUTED. THE MSB OF THE DIVIDEND, WHICH IS NOW IN THE CARRY, IS ROTATED INTO THE LSB OF THE PARTIAL DIVIDEND THAT IS STORED IN REGISTER PAIR BP AND CX, ONCE THE PARTIAL DIVIDEND IS FORMED, THE DIVISOR HAS TO BE

OBJ

SOURCE

LINE

2237 SUBTRACTED FROM IT. THE CONTENT OF SI IS SUBTRACTED FROM THE CONTENT OF  
2238 THE CX REGISTER (THE LSBY OF THE PARTIAL DIVIDEND), SUB CX,SI. THE  
2239 RESULT OF THE SUBTRACTION IS SAVED IN THE CX REGISTER. THE MSBY OF THE  
2240 PARTIAL DIVIDEND, STORED IN THE BP REGISTER AND THE CONTENT OF AX IS  
2241 SUBTRACTED-WITH-BORROW FROM BP (SBB BP,AX). THE SBB INSTRUCTION IS  
2242 USED BECAUSE THERE MAY HAVE BEEN A BORROW GENERATED WHEN THE LSBY OF THE  
2243 DIVISOR WAS SUBTRACTED FROM THE LSBY OF THE PARTIAL DIVIDEND. THE SBB  
2244 INSTRUCTION NOT ONLY SUBTRACTS THE CONTENT OF MEMORY FROM THE BP REGISTER.  
2245 OF COURSE, THE CARRY CONTAINS ANY BORROW. IF NO BORROW OCCURS FROM THIS  
2246 ENTIRE 32\_BIT SUBTRACTION, THEN THE PARTIAL DIVIDEND IS EQUAL TO OR LARGER  
2247 THAN THE DIVISOR. IF THERE IS A BORROW AS A RESULT OF THE 32\_BIT  
2248 SUBTRACTION, THEN THE PARTIAL DIVIDEND IS SMALLER THAN THE DIVISOR MUST BE  
2249 ADDED TO THE RESULT OF THE 32\_BIT SUBTRACTION TO RESTORE THE PARTIAL  
2250 DIVIDEND TO ITS ORIGINAL VALUE. TO DO THIS, BOTH ADD AND ADC  
2251 INSTRUCTIONS ARE EXECUTED. IF THERE IS NO BORROW AS A RESULT OF THE  
2252 32\_BIT SUBTRACTION, THE 8088 JUMPS TO NOADD. AT NOADD, THE CARRY IS  
2253 COMPLEMENTED TO REFLECT WHETHER OR NOT A BORROW OCCURED AS A RESULT OF THE  
2254 32\_BIT SUBTRACTION. THIS CARRY BIT IS THEN ROTATED INTO THE LSB OF  
2255 REGISTER PAIR DX AND DI AT THE TIME THAT THE NEXT MSB OF THE DIVIDEND  
2256 CONTAINED IN REGISTER PAIR DX AND DI IS ROTATED LEFT INTO THE CARRY.  
2257 THE QUOTIENT IS STORED IN REGISTER PAIR DX AND DI. THE 32\_BIT  
2258 REMAINDER IS SAVED IN THE REGISTER PAIR BP AND CX.

-----

=====

#####

32- BIT SQUARE ROOT PROCEDURE :

2291

IBJ

SOURCE

LINE

2292 THIS PROCEDURE CALCULATES THE SQUARE ROOT OF DATA STORED IN REGISTER  
2293 FAIR DX AND AX (32\_BIT) WHERE DX CONTAINS MSW, AX CONTAINS LSW, THE  
2294 RESULT WILL BE STORED IN CX REGISTER (16\_BIT). THE ALGORITHM OF  
2295 CALCULATING SQUARE ROOTS FOR BINARY NUMBERS IS MODIFIED FROM AN OLD  
2296 CHINESE RHYMED PITHY FORMULA FOR DECIMAL NUMBERS. THE PROCEDURE  
2297 IS AS FOLLOWS :

(1) SEPARATE THE BITS OF THE RADICAND INTO GROUPS OF TWO BITS  
EACH , STARTING FROM THE MSB.

(2) BEGIN THE ACTUAL EXTRACTION OPERATION AT THE FIRST GROUP OF BITS  
FROM THE LEFT THAT DOES NOT CONTAIN TWO ZEROES. ALIGN A 1 WITH  
THE RIGHT-HAND BIT OF THIS GROUP AND SUBTRACT. THE REMAINDER WILL  
BE NONNEGATIVE AND A 1 IS ENTERED IN THE ROOT FOR THIS GROUP. FOR  
EACH DOUBLE 0 GROUP TO THE LEFT OF THIS GROUP, A 0 IS ENTERED IN THE  
ROOT .

(3) FOR ALL SUCCEEDING GROUPS, THE TRIAL FACTOR TO BE SUBTRACTED FROM THE  
REMAINDER IS THE EXPRESSION [  $4*2^{N+1}$  ], THE RIGHT HAND DIGIT OF THE  
TRIAL DIVISOR IS ALIGNED WITH THE RIGHT HAND DIGIT OF THE GROUP FOR  
WHICH IT IS USED, AND SUBTRACTED. IF THE REMAINDER IS NONNEGATIVE,  
A 1 IS ENTERED AS THE ROOT FOR THAT GROUP. IF THE REMAINDER IS  
NEGATIVE, THE ROOT IS 0 AND THE SUBTRACTION IS RESTORED. SEE THE  
FOLLOWING EXAMPLES IN WHICH THE SQUARE ROOT OF (01 01 00 01) IS  
EXTRACTED .

```

1 0 0 1  ROOT
-----
01 01 00 01
 01
-----
0 01
 1 01      (4*1)+1
-----
RESTORE
 01 00

```

OBJ

SOURCE

LINE

```

2347 10 01 (4*2)+1
2348 -----
2349 RESTORE
2350 1 00 01
2351 1 00 01 (4*4)+1
2352 -----
2353 0 00 REMAINDER
2354 #####
2355 #####
2356 #####
2357 #####
2358 #####
2359 #####
2360 #####
2361 #####
2362 #####
2363 #####
2364 #####
2365 #####
2366 #####
2367 #####
2368 #####
2369 #####
2370 #####
2371 #####
2372 #####
2373 #####
2374 #####
2375 #####
2376 #####
2377 #####
2378 #####
2379 #####
2380 #####
2381 #####
2382 #####
2383 #####
2384 #####
2385 #####
2386 #####
2387 #####
2388 #####
2389 #####
2390 #####
2391 #####
2392 #####
2393 #####
2394 #####
2395 #####
2396 #####
2397 #####
2398 #####
2399 #####
2400 #####
2401 #####

MOV BX,OFFSET ASH ; STORE MS WORD OF DATA.
MOV [BX],DX
MOV BX,OFFSET ASL ; STORE LS WORD OF DATA.
MOV [BX],AX
MOV BP,0 ; INITIALIZES ROOT.
MOV CX,DX ; CX_ MS WORD OF DATA.
ROL DX,1 ; SHIFT BIT 15 AND 14 TO BIT 9 AND 8 POSITION.
ROL DX,1 ; STORE IT.
MOV BX,OFFSET R6 ; MASK OFF ALL BITS EXCEPT BIT 15 AND 14.
MOV [BX],DX ; SHIFT THESE TWO BITS TO RIGHT END POSITION.
CALL QUE ; FIRST WORK OUT THE MS WORD OF DATA.
MOV BX,OFFSET ASL ; AX_ LS WORD OF DATA.
MOV AX,[BX] ; DX_ LS WORD OF DATA.
ROL DX,1 ; SHIFT BIT 7 AND 6 TO BIT 21 AND 0 POSITION.
ROL DX,1 ; STORE IT.
MOV BX,OFFSET R6 ; SHIFT THESE TWO BITS TO RIGHT END POSITION.
MOV [BX],DX
AND AX,0C000H ; MASK OFF LAST 2 BITS OF MS WORD OF LAST
ROL AX,1 ; REMAINDER.
ROL AX,1 ; CX- NEW DIVIDEND.
AND CX,0FFFCH
OR CX,AX

```

BE5814  
8917

BE5A14  
8907

BD0000

BECA

D1C2  
D1C2

BE8414  
8917

81E100C0  
D1C1  
D1C1

E82300

BE5A14  
8E07  
8E07  
D1C2  
D1C2

BE8414  
8917

2500C0  
D1C0  
D1C0

81E1FCFF  
0BC8

```

OBJ          3E0300          2402  LINE  SOURCE
EB0300          2403          CALL QUC          ;WORK OUT THE LS WORD OF DATA.
BBCD          2404          MOV CX,BP          ;CX_ STORE THE RESULT.
CS          2405          RET
          2406
          2407
          2408
          2409          SKOOT   ENDP
          2410
          2411
          2412
          2413
          2414
          2415
          2416
          2417
          2418
          2419
          2420
          2421
          2422
          2423
          2424
          2425
          2426
          2427
          2428
          2429
          2430          QUC     PROC NEAR
          2431          MOV DI,8
          2432          LSR3:  MOV AX,DX
          2433          ADD AX,AX
          2434          ADD AX,AX
          2435          INC AX
          2436
          2437          MOV DX,CX
          2438          SUB CX,AX
          2439          JNB LSR1
          2440
          2441          MOV CX,DX
          2442          MOV AX,0
          2443          JMP LSR2
          2444
          2445          LSR1:  MOV AX,1
          2446
          2447          LSR2:  ROL BP,1
          2448          OR BP,AX
          2449
          2450          MOV BX,OFFSET R6
          2451
          2452          MOV DX,[BX]
          2453          MOV AX,DX
          2454          ROL AX,1
          2455          ROL AX,1
          2456
          3F0800
          3BC5
          3C00
          3C00
          40
          3BD1
          2BC8
          730B
          3BCA
          3B0000
          3B0490
          3B0100
          31C5
          2BE8
          3BE414
          3B17
          3BC2
          31C0
          31C0

```

;;WORK OUT THE LS WORD OF DATA.

;;CX\_ STORE THE RESULT.

RET

SKOOT ENDP

=====

;;THIS PROCEDURE CALCULATES BOTH THE MOST OR THE LEAST SIGNIFICANT

;;(MS OR LS) WORD OF THE SQUARE ROOT.

;;(MS OR LS) WORD OF THE SQUARE ROOT.

;;FOLLOWING LOOP, TOTAL IS 8 FOR 8 BITS.

PROC NEAR

DI NUMBER OF EXECUTING TIMES DOES THE

FOLLOWING LOOP, TOTAL IS 8 FOR 8 BITS.

4\*2^N+1

DX PSEUDO REMAINDER.

CX\_ REMAINDER

IF REMAINDER > TRIAL FACTOR.

ASSIGN ROOT FOR THAT TWO BITS IS 0.

ASSIGN ROOT FOR THAT TWO BITS IS 1.

BP\_ ROOT.

PREPARE NEXT TWO BITS WHICH ARE TO BE

DEALT WITH.

```

OBJ          LINE  SOURCE
BB8414      2457  MOV BX,OFFSET R6
8907        2458  MOV [BX],AX
            2459
31E200C0    2460  AND DX,0C000H
01C2        2461  ROL DX,1
01C2        2462  ROL DX,1
            2463  ;REMAINDER LS WORD.
01C1        2464  ROL CX,1
01C1        2465  ROL CX,1
            2466  ;REMAINDER MS WORD.
2BCA        2467  OR CX,DX
            2468  ;CX_ NEW DIVIDEND.
4F          2469  DEC DI
75C3        2470  JNZ LSR3
C3          2471  RET
            2472
            2473
            2474
            2475
            2476
            2477
            2478
            2479
            2480
            2481
            2482
            2483
            2484
            2485
            2486
            2487
            2488
            2489
            2490
            2491
            2492
            2493
            2494
            2495
            2496
            2497
            2498
            2499
2500        2500  LED   PROC   NEAR
2501        2501  MOV AL,LED ON
2502        2502  OUT LEDP,AL
2503        2503  HLT
2504        2504  ;HALT THE CPU.
2505
2506
2507
2508
2509
2510
2511
            ENDP
            ENDP
=====
-----
FUNCTION OF THIS PROCEDURE IS :
LIGHT THE LED TO SHOW OVERFLOW STATUS OF ADC AND HALT THE CPU.
THE SYSTEM CAN ONLY RESTART AGAIN BY PRESSING THE RESET BUTTON
ON THE FRONT_ PANEL .
-----
LED   PROC   NEAR
MOV AL,LED ON
OUT LEDP,AL
HLT
;HALT THE CPU.
LED   ENDP
    
```

DBJ

SOURCE

LINE

2512  
2513  
2514  
2515  
2516  
2517  
2518  
2519  
2520  
2521  
2522  
2523  
2524  
2525  
2526  
2527  
2528  
2529  
2530  
2531  
2532  
2533  
2534  
2535  
2536  
2537  
2538  
2539  
2540  
2541  
2542  
2543  
2544  
2545  
2546  
2547  
2548  
2549  
2550  
2551  
2552  
2553  
2554  
2555  
2556  
2557  
2558  
2559  
2560  
2561  
2562  
2563  
2564  
2565  
2566

```
=====
```

```
FANG      PROC      NEAR
```

```
-----
```

THIS PROCEDURE CAN CALCULATE ARC\_ COSINE IN BINARY FORM THE ARC\_ COSINE VALUE IS CONTAINED IN THE DI REGISTER. THE ANGLE FOUND IS ONLY IN THE RANGE 0 TO 90 DEG WITH SCALING FACTOR 10, THAT IS, 0 TO 900. ITS QUADRANT HAS TO BE DETERMINED BY OTHER PROCEDURES.

THIS PROCEDURE USES FAST SEARCHING METHOD TO FIND OUT THE ANGLE FROM THE LOOK\_UP TABLE DEFINED IN THE "ATCS" SEGMENT OF THE PROGRAM.

FOR EXAMPLES :

WHEN THE ARC\_ COS VALUE IS 0FFFFH CORRESPONDING TO INDEX SI= 0 MEANS 0 DEG.

WHEN THE ARC\_ COS VALUE IS 0FFD7H CORRESPONDING TO INDEX SI= 20 MEANS 0.2 DEG.

WHEN THE ARC\_ COS VALUE IS 9FB5H CORRESPONDING TO INDEX SI= 514 MEANS 51.4 DEG.

WHEN THE ARC\_ COS VALUE IS 0000H CORRESPONDING TO INDEX SI= 900 MEANS 90.0 DEG.

THE ACCURACY OF THIS LOOK\_UP TABLE IS 0.2 DEG RESOLUTION.

EVERY ITEM IN ACOS TABLE HAS 4 DIGITS EXPRESSED IN HEX FORM.

PROCEDURE "FANG" FIRST CHECKS THE MOST SIGNIFICANT DIGIT TO SEE WHICH ONE (FROM 0 TO F) IT IS. IT THEN JUMPS TO THE STARTING ADDRESS OF

ONE OF THOSE ITEMS WITH SAME MOST SIGNIFICANT DIGIT, SO THAT IT STARTS SEARCHING THERE UNTIL THE RIGHT ANGLE IS FOUND, INSTEAD OF SEARCHING

VERY SLOWLY FROM THE BEGINNING ( SI = 0 ) TO THE END ( SI = 900 ) OF THE TABLE. FOR EXAMPLE 0FXXH STARTS AT SI = 0, 0EXXH START AT

SI= 204 AND 7XXH STARTS AT SI = 600. BECAUSE THOSE ITEMS UNDER

THE HEADING OF F, E AND D ARE TOO MANY, THE SECOND MOST SIGNIFICANT

JB

SOURCE

2567 DIGIT OF THEM ALSO NEEDS TO BE CHECKED IN ORDER TO SPEED UP THE SEARCH  
 2568 PROCEDURE .  
 2569  
 2570 SIMILARLY, THE ANGLE OF ARC\_ SINE CAN ALSO BE FOUND OUT BY REVERSING  
 2571 THE ORDER OF THE SI INDEX IN THE INVERTED ARC\_ COS TABLE, THAT IS,  
 2572 SI = 900 MEANS 0 DEG AND SI = 0 MEANS 90 DEG.  
 2573 THE SPEED OF THIS PROCEDURE USING A LOOK\_UP TABLE INCOOPERATED WITH A  
 2574 SEARCHING TECHNIQUE IS MUCH FASTER THAN NUMERICAL PROCESSORS.  
 2575  
 2576  
 2577  
 2578  
 2579  
 2580  
 2581  
 2582  
 2583  
 2584  
 2585  
 2586  
 2587  
 2588  
 2589  
 2590  
 2591  
 2592  
 2593  
 2594  
 2595  
 2596  
 2597  
 2598  
 2599  
 2600  
 2601  
 2602  
 2603  
 2604  
 2605  
 2606  
 2607  
 2608  
 2609  
 2610  
 2611  
 2612  
 2613  
 2614  
 2615  
 2616  
 2617  
 2618  
 2619  
 2620  
 2621

3BC7

3BD0

)1C0

)1C0

)1C0

)1C0

3BF8

)1C7

)1C7

)1C7

1E70F00

50F00

8C0

412

8

412

8

412

8

412

8

412

8

412

B1390

MOV AX,DI  
MOV DX,AX

ROL AX,1

ROL AX,1

ROL AX,1

ROL AX,1

MOV DI,AX

ROL DI,1

ROL DI,1

ROL DI,1

ROL DI,1

AND DI,000FH

AND AX,000FH

OR AX,AX

JZ LT09

DEC AX

JZ LT19

DEC AX

JZ LT29

DEC AX

JZ LT39

DEC AX

JZ LT49

DEC AX

JZ LT59

JMP LCN9

;AX\_ MDST SIGNIFICANT DIGIT (HEX).  
;DI\_ 2ND MOST SIGNIFICANT DIGIT (HEX).

| OBJ    | LINE | SOURCE |              |
|--------|------|--------|--------------|
|        | 2622 | LT09:  | JMP LT0      |
| E9B000 | 2623 |        |              |
| E9A700 | 2624 | LT19:  | JMP LT1      |
| E99E00 | 2625 |        |              |
| E99500 | 2626 | LT29:  | JMP LT2      |
| E98C00 | 2627 |        |              |
| E98300 | 2628 | LT39:  | JMP LT3      |
|        | 2629 |        |              |
|        | 2630 | LT49:  | JMP LT4      |
|        | 2631 |        |              |
|        | 2632 | LT59:  | JMP LT5      |
|        | 2633 |        |              |
|        | 2634 | LCN9:  | DEC AX       |
|        | 2635 |        | JZ LT6       |
|        | 2636 |        |              |
|        | 2637 |        |              |
|        | 2638 |        | DEC AX       |
|        | 2639 |        | JZ LT7       |
|        | 2640 |        |              |
|        | 2641 |        | DEC AX       |
|        | 2642 |        | JZ LT8       |
|        | 2643 |        |              |
|        | 2644 |        | DEC AX       |
|        | 2645 |        | JZ LT9       |
|        | 2646 |        |              |
|        | 2647 |        | DEC AX       |
|        | 2648 |        | JZ LT10      |
|        | 2649 |        |              |
|        | 2650 |        | DEC AX       |
|        | 2651 |        | JZ LT11      |
|        | 2652 |        |              |
|        | 2653 |        | DEC AX       |
|        | 2654 |        | JZ LT12      |
|        | 2655 |        |              |
|        | 2656 |        | DEC AX       |
|        | 2657 |        | JZ LT13      |
|        | 2658 |        |              |
|        | 2659 |        | DEC AX       |
|        | 2660 |        | JZ LT14      |
|        | 2661 |        |              |
|        | 2662 |        | CMP DI,000EH |
|        | 2663 |        | JB LT151     |
|        | 2664 |        |              |
|        | 2665 |        | MOV SI,0     |
|        | 2666 |        | JMP LTE      |
|        | 2667 |        |              |
|        | 2668 | LT151: | CMP DI,0007H |
|        | 2669 |        | JNA LT152    |
|        | 2670 |        | MOV SI,36D   |
|        | 2671 |        | JMP LTE      |
|        | 2672 |        |              |
|        | 2673 | LT152: | MOV SI,72D   |
|        | 2674 |        | JMP LTE      |
|        | 2675 |        |              |
|        | 2676 | LT14:  | CMP DI,0008H |
|        | 2677 |        |              |

| OBJ    | LINE | SOURCE              |
|--------|------|---------------------|
| 7206   | 2677 | JB LT141            |
| 3E6600 | 2678 | MOV SI, 102D        |
| 3B6390 | 2679 | JMP LJE             |
| 3E7B00 | 2680 |                     |
| 3B5D90 | 2681 | LT141: MOV SI, 123D |
| 33FF09 | 2682 | JMP LJE             |
| 7206   | 2683 | LT13: CMF DI, 0009D |
| 3E9100 | 2684 | JB LT131            |
| 3B5290 | 2685 |                     |
| 3EA100 | 2686 | MOV SI, 145D        |
| 3B4C90 | 2687 | JMP LJE             |
| 3EB300 | 2688 |                     |
| 3B4690 | 2689 | LT131: MOV SI, 161D |
| 3ED000 | 2690 | JMP LJE             |
| 3B4090 | 2691 |                     |
| 3EE900 | 2692 | LT12: MOV SI, 179D  |
| 3B3A90 | 2693 | JMP LJE             |
| 3E0101 | 2694 |                     |
| 3B3490 | 2695 | LT11: MOV SI, 208D  |
| 3E1701 | 2696 | JMP LJE             |
| 3B2E90 | 2697 |                     |
| 3E2C01 | 2698 | LT10: MOV SI, 233D  |
| 3B2890 | 2699 | JMP LJE             |
| 3E4101 | 2700 |                     |
| 3B2290 | 2701 | LT9: MOV SI, 257D   |
| 3E5401 | 2702 | JMP LJE             |
| 3B1C90 | 2703 |                     |
| 3E6701 | 2704 | LT8: MOV SI, 279D   |
| 3B1690 | 2705 | JMP LJE             |
| 3E7A01 | 2706 |                     |
| 3B1090 | 2707 | LT7: MOV SI, 300D   |
| 3E8C01 | 2708 | JMP LJE             |
| 3B0A90 | 2709 |                     |
| 3E9F01 | 2710 | LT6: MOV SI, 321D   |
| 3B0490 | 2711 | JMP LJE             |
| 3EB101 | 2712 |                     |
|        | 2713 | LT5: MOV SI, 340D   |
|        | 2714 | JMP LJE             |
|        | 2715 |                     |
|        | 2716 | LT4: MOV SI, 359D   |
|        | 2717 | JMP LJE             |
|        | 2718 |                     |
|        | 2719 | LT3: MOV SI, 378D   |
|        | 2720 | JMP LJE             |
|        | 2721 |                     |
|        | 2722 | LT2: MOV SI, 396D   |
|        | 2723 | JMP LJE             |
|        | 2724 |                     |
|        | 2725 | LT1: MOV SI, 415D   |
|        | 2726 | JMP LJE             |
|        | 2727 |                     |
|        | 2728 | LT0: MOV SI, 433D   |
|        | 2729 |                     |
|        | 2730 |                     |
|        | 2731 |                     |

```

LINE          SOURCE
2732          LBL:      ADD SI,SI          ;WORK OUT THE TRUE ADDRESS INDEX.
2733          23F6
2734          3B00000 MOV BX,OFFSET ACOS
2735          263B10 CMP DX,ES:[BX+SI]
2736          7305 JNB LT20
2737          33C602 ADD SI,2
2738          2739 JMP LTEL1
2739          2741 MOV DI,SI
2740          2742
2741          2743
2742          2744
2743          2745
2744          2746
2745          2747
2746          2748
2747          2749
2748          2750
2749          2751
2750          2752
2751          2753
2752          2754
2753          2755
2754          2756
2755          2757
2756          2758
2757          2759
2758          2760
2759          2761
2760          2762
2761          2763
2762          2764
2763          2765
2764          2766
2765          2767
2766          2768
2767          2769
2768          2770
2769          2771
2770          2772
2771          2773
2772          2774
2773          2775
2774          2776
2775          2777
2776          2778
2777          2779
2778          2780
2779          2781
2780          2782
2781          2783
2782          2784
2783          2785
2784          2786
2785          2787
2786          2788

SOURCE
LTEL1:
LTEL2:
LT20:
FANG
GPIB
LBL:
LBL1:
LBL3:
LBLA:

;SEARCH UNTIL THE INPUT VALUE IN DI MATCHES
;WITH THE ONE IN LOOK_UP TABLE.
;DI_ ANG .
;DX_ DATA TO SEND.
;PRIMARY TKR OK TO GO OCCURED ?
;NO .
;YES
;B0 SET ?
;NO .
;YES, LOAD DATA TO SEND (MSBY) .
;PRIMARY TKR OK TO GO OCCURED ?

#####
;THIS PROCEDURE POLLS THE READINESS OF GPIB AND TRANSFERS THE DATA
;OF TOTAL NUMBER OF DATA NEEDS TO BE TRANSFERRED AND THE FUNDAMENTAL
;FREQUENCY TO THE GPIB.
#####
PROC NEAR
MOV DX,[BX+SI] ;DX_ DATA TO SEND.
IN AL,0E2H ;PRIMARY TKR OK TO GO OCCURED ?
AND AL,88H
CMP AL,88H
JNZ LBL1 ;NO .
IN AL,0E0H ;YES
TEST AL,40H ;B0 SET ?
JZ LBL3 ;NO .
MOV AL,DH ;YES, LOAD DATA TO SEND (MSBY) .
OUT 0E7H,AL
IN AL,0E2H ;PRIMARY TKR OK TO GO OCCURED ?

```

```

LINE SOURCE
2787 AND AL,88H
2788 CMF AL,88H
2789 JNZ LBLA
2790
2791 LBLC: IN AL,0E0H
2792
2793 TEST AL,40H
2794 JZ LBLC
2795
2796 MOV AL,DL
2797 OUT 0E7H,AL
2798
2799 ADD SI,2
2800 LOOP LBL
2801
2802 LBL4: IN AL,0E0H
2803 TEST AL,40H
2804 JZ LBL4
2805
2806 RET
2807
2808
2809
2810 GPIB ENDP
2811
2812
2813
2814
2815
2816
2817
2818
2819
2820
2821
2822
2823
2824
2825
2826
2827
2828
2829
2830
2831
2832
2833
2834
2835
2836
2837
2838
2839
2840
2841

; NO .
; YES
; B0 SET ?
; NO .
; YES, LOAD DATA TO SEND (LSBY).
; INCREASE ADDRESS POINTER.
; B0 SET ?
; NO .
; YES .

=====
;
;
;
; THIS PROCEDURE FOLLS THE READINESS OF GPIB AND TRANSFERS THE DATA
; OF AMP. AND ANG. TO THE GPIB.
;
=====
GPIB1 PROC NEAR
TLBT: MOV BX,OFFSET AMP
MOV DX,[BX+SI]
TLBT1: IN AL,0E2H
AND AL,88H
CMP AL,88H
JNZ TLBT1
TLBT3: IN AL,0E0H
TEST AL,40H
JZ TLBT3
; BA00F
; B10
4E2
488
C88
5F8
4E0
840
4FA
; DX_ DATA TO SEND
; PRIMARY TKR OK TO GO OCCURED ?
; NO .
; YES
; B0 SET ?
; NO .

```

| OBJ   | LINE | SOURCE             |                                  |
|-------|------|--------------------|----------------------------------|
|       | 2842 | MOV AL, DH         |                                  |
|       | 2843 | OUT 0E7H, AL       | ; YES, LOAD DATA TO SEND (MSBY). |
| 3AC6  | 2844 |                    |                                  |
| 36E7  | 2845 |                    |                                  |
|       | 2846 | IN AL, 0E2H        |                                  |
| 4AE2  | 2847 | AND AL, 88H        | ; PRIMARY TKR OK TO GO OCCURED ? |
| 4888  | 2848 | CMP AL, 88H        |                                  |
| 75F8  | 2849 | JNZ TLBTA          | ; NO .                           |
|       | 2850 |                    |                                  |
| 4E0   | 2851 | IN AL, 0E0H        |                                  |
| 840   | 2852 | TEST AL, 40H       | ; YES                            |
| 74FA  | 2853 | JZ TLBTC           | ; B0 SET ?                       |
|       | 2854 |                    | ; NO .                           |
| 3AC2  | 2855 | MOV AL, DL         |                                  |
| 36E7  | 2856 | OUT 0E7H, AL       | ; YES, LOAD DATA TO SEND (LSBY). |
|       | 2857 |                    |                                  |
| 3BC10 | 2858 | MOV BX, OFFSET ANG |                                  |
| 3B10  | 2859 | MOV DX, CBX+SIJ    | ; DX... DATA TO SEND..           |
|       | 2860 |                    |                                  |
|       | 2861 |                    |                                  |
| 4E2   | 2862 | IN AL, 0E2H        |                                  |
| 488   | 2863 | AND AL, 88H        | ; PRIMARY TKR OK TO GO OCCURED ? |
| 3C88  | 2864 | CMP AL, 88H        |                                  |
| 75F8  | 2865 | JNZ FLBL1          | ; NO .                           |
|       | 2866 |                    |                                  |
| 4E0   | 2867 | IN AL, 0E0H        |                                  |
| 840   | 2868 | TEST AL, 40H       | ; YES                            |
| 74FA  | 2869 | JZ FLBL3           | ; B0 SET ?                       |
|       | 2870 |                    | ; NO .                           |
| 3AC6  | 2871 | MOV AL, DH         |                                  |
| 36E7  | 2872 | OUT 0E7H, AL       | ; YES, LOAD DATA TO SEND (MSBY). |
|       | 2873 |                    |                                  |
| 4E2   | 2874 | IN AL, 0E2H        |                                  |
| 488   | 2875 | AND AL, 88H        | ; PRIMARY TKR OK TO GO OCCURED ? |
| 3C88  | 2876 | CMP AL, 88H        |                                  |
| 75F8  | 2877 | JNZ FLBLA          | ; NO .                           |
|       | 2878 |                    |                                  |
| 4E0   | 2879 | IN AL, 0E0H        |                                  |
| 840   | 2880 | TEST AL, 40H       | ; YES                            |
| 4FA   | 2881 | JZ FLBLC           | ; B0 SET ?                       |
|       | 2882 |                    | ; NO .                           |
| AC2   | 2883 | MOV AL, DL         |                                  |
| 6E7   | 2884 | OUT 0E7H, AL       | ; YES, LOAD DATA TO SEND (LSBY). |
|       | 2885 |                    |                                  |
| 3C602 | 2886 | ADD SI, 2          |                                  |
| 203   | 2887 | LOOP TLBX          | ; INCREASE ADDRESS POINTER.      |
| B0390 | 2888 |                    |                                  |
|       | 2889 | JMP TLBL4          |                                  |
| BA4   | 2890 |                    |                                  |
|       | 2891 | JMP TLBT           |                                  |
|       | 2892 |                    |                                  |
| 4E0   | 2893 | IN AL, 0E0H        |                                  |
| 840   | 2894 | TEST AL, 40H       | ; B0 SET ?                       |
| 4FA   | 2895 | JZ TLBL4           | ; NO .                           |
|       | 2896 |                    |                                  |

```

LINE          SOURCE          RET          ;YES .
2897          RET
2898
2899
2900
2901          GFI B1          ENDP
2902
2903
2904
2905
2906
2907
2908
2909
2910
2911
2912
2913
2914
2915
2916
2917
2918
2919
2920
2921
2922
2923
2924
2925
2926
2927
2928
2929
2930
2931
2932
2933
2934
2935
2936
2937
2938
2939
2940
2941
2942
2943
2944
2945
2946
2947
2948
2949
2950
2951

=====
DUMMY_READ   PROC          NEAR
MOV AL,1
MOV BX,OFFSET R14
MOV [BX],AL
XOR SI,SI          ;NULL SI .
MOV BX,OFFSET R11
MOV [BX],SI          ;INITIALIZES XYP .
MOV BX,OFFSET ZCCP
MOV [BX],SI          ;INITIALIZES ZCCP.
CALL ZC_ADC
CALL MOD_CLK_UPDATE_1
RET
DUMMY_READ   ENDP
=====
THREE_7_8    PROC          NEAR
;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION (3.7.8).
IN AL,SWP
AND AL,HA_ORDER_MASK
CMP AL,23D
JA LQ9H
JMP LQ98L
LQ9H:        MOV SI,552D
MOV BX,OFFSET R6
MOV AX,3
ORDER:      > 23 .
ORDER:     =< 23 .
            ;(24-1)*2*2*6 .

```

OBJ

C3

B001  
BB9314  
BB07  
33F6

BBE14  
8937

BB5E14  
8937

E886FB

E8DEFC

C3

E480

241F  
3C17

7703  
EB3590

BE2802

BB8414  
EB0300

```

OBJ          LINE          SOURCE
8907         2952         MOV [BX],AX
            2953
            2954
            2955
            2956
            2957
            2958         MOV BX,OFFSET R3
            2959         MOV AX,384D
            2960
            2961
            2962
            2963         MOV [BX],AX
            2964
            2965         MOV BX,OFFSET R1
            2966         MOV [BX],SI
            2967
            2968         MOV CX,6
            2969         MOV BX,OFFSET R0
            2970         MOV [BX],CX
            2971
            2972         MOV CX,2
            2973         MOV BX,OFFSET R5
            2974         MOV [BX],CX
            2975
            2976         CALL DEHA
            2977
            2978         LOOP L08
            2979
            2980         MOV BX,OFFSET R0
            2981         MOV CX,[BX]
            2982
            2983         LOOP L08B
            2984
            2985         L098L:  RET
            2986
            2987
            2988         THREE_7__8  ENDF
            2989
            2990
            2991
            2992
            2993
            2994         THREE_7__7  PROC    NEAR
            2995
            2996         ;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.7).
            2997         IN AL,SWP
            2998         AND AL,HA ORDER_MASK
            2999         CMP AL,20D
            3000
            3001
            3002
            3003         JA L09G
            3004         JMP L097L
            3005
            3006
            ;ORDER : > 20 .
            ;ORDER : =< 20 .

```

```

;2*2*6*(16), WHERE THE CONTENT INSIDE THE
;( ) IS THE DIFFERENCE OF ORDER BETWEEN
;TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN THE
;EQUATION .

```

```

;SI_ LAST D.C. TERM ADDRESS POINTER.

```

```

;CX_ POINTER FOR CHANNEL.

```

```

;CX_ POINTER FOR 0 AND 90 DEG.

```

```

;ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.

```

```

;CX_ POINTER FOR CHANNEL.

```

```

;=====

```

```

THREE_7__7  PROC    NEAR

```

```

;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.7).

```

```

IN AL,SWP

```

```

;INPUT FROM SWITCH PORT TO SEE MAX. ORDER
;OF HARMONIC THAT NEEDS TO BE MEASURED.

```

```

AND AL,HA ORDER_MASK
CMP AL,20D

```

```

JA L09G
JMP L097L

```

```

7703
EB3590

```

```

OBJ          LINE          SOURCE
: FOR INSTRUCTIONS BELOW :
: SI_ LAST D.C. TERM ADDRESS POINTER.
: AX_ GREATEST DIVISOR.
L096:      MOV SI,480D      ; (21-1)*2*2*6 .
BB8414     MOV BX,OFFSET R6
BB8300     MOV AX,3
BB907      MOV [BX],AX

: CALCULATE EQUATION (3.7.7) :
MOV BX,OFFSET R3
MOV AX,336D

MOV [BX],AX
MOV BX,OFFSET R1
MOV [BX],SI
MOV CX,6
MOV BX,OFFSET R0
MOV [BX],CX
MOV CX,2
MOV BX,OFFSET R5
MOV [BX],CX
CALL DEHA
LOOP L07
MOV BX,OFFSET R0
MOV CX,[BX]
LOOP L077
L097L:    RET
THREE_7_7      ENDP
:=====
THREE_7_6      PROC      NEAR

```

```

:2*2*6*(14), WHERE THE CONTENT INSIDE THE
:( ) IS THE DIFFERENCE OF ORDER BETWEEN
:TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN THE
:EQUATION .
:SI_ LAST D.C. TERM ADDRESS POINTER.
: CX_ POINTER FOR CHANNEL.
: CX_ POINTER FOR 0 AND 90 DEG.
:ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.
: CX_ POINTER FOR CHANNEL.

```

```

OBJ          LINE          SOURCE
E480        3062          ;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.6).
241F        3063          IN AL,SWP
3C11        3064          ;INPUT FROM SWITCH PORT TO SEE MAX. ORDER
              3065          ;OF HARMONIC THAT NEEDS TO BE MEASURED.
7703        3066          AND AL,HA ORDER_MASK
EB3590      3067          CMP AL,17D
              3068          JA LQ9F
              3069          JMP LQ96L
              3070          ;ORDER : > 17 .
              3071          ;ORDER : =< 17 .
              3072
              3073
              3074
              3075
              3076
              3077
              3078
              3079          LQ9F:   MOV SI,40BD
              3080          ;INSTRUCTIONS BELOW :
              3081          ;SI_ LAST D.C. TERM ADDRESS POINTER.
              3082          ;AX_ GREATEST DIVISOR.
              3083          MOV BX,OFFSET R6
              3084          MOV AX,3
              3085          MOV [BX],AX
              3086
              3087
              3088
              3089          ;CALCULATE EQUATION (2.4.6) :
              3090          MOV BX,OFFSET R3
              3091          MOV AX,228D
              3092
              3093          ;2*2*6*(12), WHERE THE CONTENT INSIDE THE
              3094          ;( ) IS THE DIFFERENCE OF ORDER BETWEEN
              3095          ;TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN THE
              3096          ;EQUATION .
              3097          MOV [BX],AX
              3098
              3099          ;SI_ LAST D.C. TERM ADDRESS POINTER.
              3100          MOV BX,OFFSET R1
              3101          MOV [BX],SI
              3102
              3103          ;CX_ POINTER FOR CHANNEL.
              3104          MOV CX,6
              3105          MOV BX,OFFSET R0
              3106          MOV [BX],CX
              3107
              3108          ;CX_ POINTER FOR 0 AND 90 DEG.
              3109          MOV CX,2
              3110          MOV BX,OFFSET R5
              3111          MOV [BX],CX
              3112
              3113          ;ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.
              3114          CALL DEHA
              3115          LOOP LQ6
              3116          MOV BX,OFFSET R0
              3117          MOV CX,[BX]
              3118          LOOP LQ66
              3119          ;CX_ POINTER FOR CHANNEL.
              3120          LQ66:
              3121          LQ6:
              3122          LQ96L:  RET

```

```

LINE SOURCE
1117 THREE_7_6 ENDP
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
OBJ E480 E480
    241F 3C0E
    7703 EB4290
    3C19 7209
    BE4002 EB0500 EB0790
    BE5001 EB0300
    BB8414 B907
    BB7E14 BBF000
    B907
    BB7A14 B937
    B90600

=====
THREE_7_5 PROC NEAR
;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.5).
    IN AL,SWP
    AND AL,HA ORDER_MASK
    CMP AL,14D
    JA LQ9E
    JMP LQ95L
    ORDER : > 14 :
    ORDER : =< 14 :

;FOR INSTRUCTIONS BELOW :
;SI LAST D.C. TERM ADDRESS POINTER.
;AX GREATEST DIVISOR.
LQ9E:  CMP AL,25D
      JB Q551
      MOV SI,576D
      MOV AX,5
      JMP Q559
Q551:  MOV SI,336D
      MOV AX,3
Q559:  MOV BX,OFFSET R6
      MOV [BX],AX
;CALCULATE EQUATION (3.7.5) :
      MOV BX,OFFSET R3
      MOV AX,240D
      MOV [BX],AX
      MOV BX,OFFSET R1
      MOV [BX],SI
      MOV CX,6
      ;2*2*6*(10), WHERE THE CONTENT INSIDE THE
      ; ( ) IS THE DIFFERENCE OF ORDER BETWEEN
      ; TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN
      ; THE EQUATION .
      ;SI LAST D.C. TERM ADDRESS POINTER.

```

```

OBJ          LINE          SOURCE
: BB7814     3172     MOV BX,OFFSET R0
: 890F       3173     MOV [BX],CX
:           3174
: 890200     3175     MOV CX,2
: BB8214     3176     MOV BX,OFFSET R5
: 890F       3177     MOV [BX],CX
:           3178
: E834FC     3179     CALL DEHA
:           3180
: E2F9       3181     LOOP L05
:           3182
: BB7814     3183     MOV BX,OFFSET R0
: 8B0F       3184     MOV CX,[BX]
:           3185
: E2EA       3186     LOOP L055
:           3187
: C3         3188     RET
:           3189
:           3190
:           3191
:           3192
:           3193
:           3194
:           3195
:           3196
:           3197
:           3198
: E480       3199     THREE_7_5     ENDF
:           3200
:           3201
:           3202
: 241F       3203     ;
: 3C08       3204     ;
:           3205
: 7703       3206     ;
: EB4290     3207     ;
:           3208
:           3209
:           3210
:           3211
:           3212
:           3213
:           3214
:           3215
: 3C14       3216     ;
: 7209       3217     ;
:           3218
: BEC801     3219     ;
: B80500     3220     ;
: EB0790     3221     ;
:           3222
: BE0801     3223     ;
: B80300     3224     ;
:           3225
: BB8414     3226     ;

```

;CX\_ POINTER FOR 0 AND 90 DEG.

;ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.

;CX\_ POINTER FOR CHANNEL.

THREE\_7\_5 ENDF

THREE\_7\_4 PROC

;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.4).  
 IN AL,SWP  
 AND AL,HA ORDER\_MASK  
 CMP AL,11D  
 JA L09D  
 JMP L094L

;ORDER : > 11 :  
 ;ORDER : =< 11 :

;FOR INSTRUCTIONS BELOW ;  
 ;SI LAST D.C. TERM ADDRESS POINTER.  
 ;AX\_ GREATEST DIVISOR.

L09D: CMP AL,20D  
 JB Q441  
 MOV SI,456D  
 MOV AX,5  
 JMP Q449

Q441: MOV SI,264D  
 MOV AX,3

Q449: MOV BX,OFFSET R6

```

OBJ
8907      MOV [BX],AX

BB7E14
BB8000
8907      MOV [BX],AX

BB7A14
8937      MOV BX,OFFSET R1
          MOV [BX],SI

B90600
BB7B14
890F      MOV CX,6
          MOV BX,OFFSET R0
          MOV [BX],CX

LQ44:
B90200
BB8214
890F      MOV CX,2
          MOV BX,OFFSET R5
          MOV [BX],CX

E8E7FB
E2F9      CALL DEHA
          LOOP LQ4

BB7B14
8B0F      MOV BX,OFFSET R0
          MOV CX,[BX]

E2EA
C3        LOOP LQ44

LQ94L:    RET

THREE_7_4      ENDP

;=====
THREE_7_3      PROC    NEAR
;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.3).
IN AL,SWP
AND AL,HA_ORDER_MASK
CMP AL,8
JA LQ9C
JMP LQ93L

;ORDER : > 8 :
;ORDER : =< 8 :

```

```

;2*2*6*(8), WHERE THE CONTENT INSIDE THE
;( ) IS THE DIFFERENCE OF ORDER BETWEEN
;TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN
;THE EQUATION.

```

```

;SI_ LAST D.C. TERM ADDRESS POINTER.

```

```

;CX_ POINTER FOR 0 AND 90 DEG.

```

```

;ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.

```

```

;CX_ POINTER FOR CHANNEL.

```

```

;INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.3).

```

```

;INPUT FROM SWITCH PORT TO SEE MAX. ORDER
;OF HARMONIC THAT NEEDS TO BE MEASURED.

```

```

;ORDER : > 8 :
;ORDER : =< 8 :

```

```

DBJ
LINE SOURCE
3282 ; FOR INSTRUCTIONS BELOW ;
3283 ; SI_ LAST D.C. TERM ADDRESS POINTER.
3284 ; AX_ GREATEST DIVISOR.
3285
3286 L09C: CMP AL,21D
3287 JB Q331 ; ORDER < 21 .
3288
3289 MOV SI,480D
3290 MOV AX,7
3291 JMP Q339 ; ORDER >= 21 .
3292 ; (21-1)*2*2*6 .
3293
3294 Q331: CMP AL,15D
3295 JB Q332 ; ORDER < 15.
3296
3297 MOV SI,336D
3298 MOV AX,5
3299 JMP Q339 ; ORDER >= 15 .
3300 ; (15-1)*2*2*6 .
3301
3302 MOV SI,192D
3303 MOV AX,3
3304
3305 MOV BX,OFFSET R6
3306 MOV [BX],AX
3307
3308 Q332:
3309
3310 ; CALCULATE EQUATION (3.7.3) :
3311 MOV BX,OFFSET R3
3312 MOV AX,144D
3313
3314 MOV [BX],AX
3315
3316 MOV BX,OFFSET R1
3317 MOV [BX],SI
3318
3319 MOV CX,6
3320 MOV BX,OFFSET R0
3321 MOV [BX],CX
3322
3323 MOV CX,2
3324 MOV BX,OFFSET R5
3325 MOV [BX],CX
3326
3327 Q333:
3328
3329 CALL DEHA
3330 LOOP L03
3331
3332 MOV BX,OFFSET R0
3333 MOV CX,[BX]
3334
3335
3336
387E14 ; 2*2*6*(6), WHERE THE CONTENT INSIDE THE
389000 ; ( ) IS THE DIFFERENCE OF ORDER BETWEEN
; TWO SUCCESSIVE NEIGHBOUR D.C. TERMS IN THE
; EQUATION.
3907 ; SI_ LAST D.C. TERM ADDRESS POINTER.
387A14
3937
390600
387814
390F
390200
388214
390F
; ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.
; 2F9
; 87814
; 80F

```

```

DBJ
E2EA
33
337
338 LOOP LQ33
339
340 LQ3L: RET
341
342
343 THREE_7_3 ENDF
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
E480
E41F
E305
7703
E86990
E316
7209
3EF801
380B00
E82E90
E312
7209
E9801
380900
E82190
E30E
7209
E3801
80700
E81490
E30A

```

```

SOURCE
LOOP LQ33
LQ3L: RET
THREE_7_3 ENDF
=====
THREE_7_2 PROC NEAR
; INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.2) .
IN AL,SWF
AND AL,HA_ORDER_MASK
CMP AL,5
JA LQ9B
JMP LQ92L
; ORDER : > 5 :
; ORDER : =< 5 :
LQ9B: CMP AL,22D
JB Q221
; ORDER < 22 .
MOV SI,504D
MOV AX,11D
JMP Q229
; ORDER >= 22 .
; (22-1)*2*2*6 .
Q221: CMP AL,18D
JB Q222
; ORDER < 18 .
MOV SI,408D
MOV AX,9
JMP Q229
; ORDER >= 18 .
; (18-1)*2*2*6 .
Q222: CMP AL,14D
JB Q223
; ORDER < 14 .
MOV SI,312D
MOV AX,7
JMP Q229
; ORDER >= 14 .
; (14-1)*2*2*6 .
Q223: CMP AL,10D

```

```

; FOR THE INSTRUCTIONS BELOW
; SI LAST D.C. TERM ADDRESS POINTER.
; AX GREATEST DIVISOR.

```



```

LINE
3447
3448
3449
3450
3451
3452
3453
3454
3455
3456
3457
3458
3459
3460
3461
3462
3463
3464
3465
3466
3467
3468
3469
3470
3471
3472
3473
3474
3475
3476
3477
3478
3479
3480
3481
3482
3483
3484
3485
3486
3487
3488
3489
3490
3491
3492
3493
3494
3495
3496
3497
3498
3499
3500
3501

OBJ
3480
341F
3C02
703
B4190

; INITIALIZES THE STARTING ENVIRONMENT FOR CALCULATING EQUATION(3.7.1) .
IN AL,SWP
AND AL,HA_ORDER_MASK
CMP AL,2
JA LQ9A
JMP LQ91L
; CHECK 2ND ORDER.
; ORDER : > 2 :
; ORDER : =< 2 :

; CALCULATE EQUATION (3.7.1) :
LQ9A: MOV BX,OFFSET R3
MOV DX,48D
MOV [BX],DX
MOV AH,AL
RCR AH,1
JC LQ1E
DEC AL
LQ1E: XOR AH,AH
MOV BX,OFFSET R6
MOV [BX],AX
DEC AX
MOV DX,24D
MUL DX
MOV BX,OFFSET R1
MOV [BX],AX
MOV SI,AX
MOV CX,6
MOV BX,OFFSET R0
MOV [BX],CX
MOV CX,2
MOV BX,OFFSET R5
MOV [BX],CX
LQ11:
LQ1: CALL DEHA
LOOP LQ1

; 2*2*6*(2) , WHERE THE CONTENT INSIDE THE
; ( ) IS THE DIFFERENCE OF ORDER BETWEEN TWO
; SUCCESSIVE NEIGHBOUR D.C. TERMS IN THE
; EQUATION .
; AH MAX ORDER OF HARMONIC THAT NEEDS TO BE
; MANAGED.
; USE CARRY BIT TO TEST ODD OR EVEN NUMBER ?
; ODD NUMBER.
; EVEN NUMBER, MAKE IT ODD.
; NULL AH.
; 2*2*6 . .
; SI LAST D.C. TERM ADDRESS POINTER.
; CX POINTER FOR CHANNEL.
; CX POINTER FOR 0 AND 90 DEG.
; ELIMINATE D.C. TERMS DUE TO HIGHER HARMONICS.

```

OBJ  
3B7814  
3B0F  
E2EA  
33

```

LINE SOURCE
3502 MOV BX,OFFSET R0 ;CX_ POINTER FOR CHANNEL.
3503 MOV CX,[BX]
3504 LOOP LQ11
3505 LQ11: RET
3506
3507
3508 THREE_7_1 ENDF
3509
3510
3511
3512
3513
3514
3515
3516
3517
3518
3519
3520
3521
3522
3523
3524
3525
3526
3527
3528
3529
3530
3531
3532
3533
3534
3535
3536
3537
CODE_SEG ENDS
; ~~~~~
RES SEGMENT AT 0FFFFH
JMP BEGIN
RES ENDS
; =====
END BEGIN

```

A000050FC

SYMBOL TABLE LISTING

| NAME           | TYPE    | VALUE | ATTRIBUTES             |
|----------------|---------|-------|------------------------|
| ??SEG          | SEGMENT | 0000H | SIZE=0000H FARA PUBLIC |
| ADCF           | V WORD  | 00A0H | ATCS                   |
| AMP            | NUMBER  | 0FA0H | (150) SAMP             |
| ANG            | V WORD  | 10CCH | (150) SAMP             |
| ASH            | V WORD  | 1458H | SAMP                   |
| ASL            | V WORD  | 145AH | SAMP                   |
| ATCS           | SEGMENT | 036AH | SIZE=0386H WORD ABS    |
| AVERAGING      | F NEAR  | 0000H | SIZE=0089H CODE SEG    |
| BEGIN VA       | F FAR   | 0000H | SIZE=02C8H CODE SEG    |
| CHAN VA        | NUMBER  | 0006H | SIZE=09BAH WORD ABS    |
| CODE_SEG       | SEGMENT | 0060H |                        |
| CTR0           | NUMBER  | 0036H |                        |
| CTR0_CNTL_WORD | NUMBER  | 0068H |                        |
| CTR1           | NUMBER  | 0074H |                        |
| CTR1_CNTL_WORD | NUMBER  | 0078H |                        |
| CTRC           | NUMBER  | 047DH |                        |
| DEHA           | F NEAR  | 04DBH | SIZE=005EH CODE SEG    |
| DIV 32         | F NEAR  | 072CH | SIZE=0035H CODE SEG    |
| DUMMY_READ     | F NEAR  | 072CH | SIZE=001AH CODE SEG    |
| FANG           | F NEAR  | 059CH | SIZE=00FBH CODE SEG    |
| FORM_MASK      | NUMBER  | 0080H |                        |
| FREQ           | V WORD  | 145CH | SAMP                   |
| GATE           | NUMBER  | 0020H |                        |
| GPFB           | F NEAR  | 0697H | SIZE=0032H CODE SEG    |
| GPFB1          | F NEAR  | 06C9H | SIZE=0063H CODE SEG    |
| HA ORDER_MASK  | NUMBER  | 001FH |                        |
| L12            | L NEAR  | 050AH | CODE SEG               |
| L321           | L NEAR  | 0368H | CODE SEG               |
| L3211          | L NEAR  | 0085H | CODE SEG               |
| L395           | L NEAR  | 033BH | CODE SEG               |
| L396           | L NEAR  | 0344H | CODE SEG               |
| L3A            | L NEAR  | 030BH | CODE SEG               |
| L3C            | L NEAR  | 0325H | CODE SEG               |
| L3F            | L NEAR  | 02FEH | CODE SEG               |
| L3H            | L NEAR  | 03DFH | CODE SEG               |
| L4             | L NEAR  | 0401H | CODE SEG               |
| L41            | L NEAR  | 0410H | CODE SEG               |
| L42            | L NEAR  | 039AH | CODE SEG               |
| L4A            | L NEAR  | 0380H | CODE SEG               |
| L4B            | L NEAR  | 0380H | CODE SEG               |
| L4BB           | L NEAR  | 0383H | CODE SEG               |
| L4C            | L NEAR  | 037FH | CODE SEG               |
| L5             | L NEAR  | 03E4H | CODE SEG               |
| L999           | L NEAR  | 00D0H | CODE SEG               |
| LA1            | L NEAR  | 02DDH | CODE SEG               |
| LA10           | L NEAR  | 02C8H | CODE SEG               |
| LA11           | L NEAR  | 0063H | CODE SEG               |
| LA17           | L NEAR  | 0468H | CODE SEG               |
| LA171          | L NEAR  | 0470H | CODE SEG               |
| LA2            | L NEAR  | 02EAH | CODE SEG               |

| NAME    | TYPE   | VALUE  | ATTRIBUTES          |
|---------|--------|--------|---------------------|
| LA214   | NEAR   | 0453H  | CODE SEG            |
| LA215   | NEAR   | 04446H | CODE SEG            |
| LA216   | NEAR   | 0444EH | CODE SEG            |
| LA217   | NEAR   | 0011EH | CODE SEG            |
| LA27    | NEAR   | 0475H  | CODE SEG            |
| LAC     | NEAR   | 02E5H  | CODE SEG            |
| LACM    | NEAR   | 005DH  | CODE SEG            |
| LAGM    | NEAR   | 04AAH  | CODE SEG            |
| LAGN    | NEAR   | 04B7H  | CODE SEG            |
| LBEGIN  | NEAR   | 0013H  | CODE SEG            |
| LBL     | NEAR   | 0697H  | CODE SEG            |
| LBL1    | NEAR   | 0699H  | CODE SEG            |
| LBL3    | NEAR   | 06A1H  | CODE SEG            |
| LBL4    | NEAR   | 06C2H  | CODE SEG            |
| LBLA    | NEAR   | 06ABH  | CODE SEG            |
| LBLC    | NEAR   | 06B3H  | CODE SEG            |
| LBN9    | NEAR   | 05E1H  | CODE SEG            |
| LED OFF | NUMBER | 0597H  | SIZE=0005H CODE_SEG |
| LED ON  | NUMBER | 0000H  |                     |
| LEDP    | NUMBER | 0080H  |                     |
| LHT     | NEAR   | 00C0H  | CODE SEG            |
| LJT     | NEAR   | 0292H  | CODE SEG            |
| LK21    | NEAR   | 0298H  | CODE SEG            |
| LLED    | NEAR   | 00ACH  | CODE SEG            |
| LM11    | NEAR   | 037CH  | CODE SEG            |
| LM12    | NEAR   | 012AH  | CODE SEG            |
| LM0K    | NEAR   | 0141H  | CODE SEG            |
| LO1     | NEAR   | 01E6H  | CODE SEG            |
| LO11    | NEAR   | 09ABH  | CODE SEG            |
| LO1E    | NEAR   | 09A3H  | CODE SEG            |
| LO2     | NEAR   | 0989H  | CODE SEG            |
| LO22    | NEAR   | 095FH  | CODE SEG            |
| LO2K    | NEAR   | 0957H  | CODE SEG            |
| LO25    | NEAR   | 01C4H  | CODE SEG            |
| LO2K    | NEAR   | 08EBH  | CODE SEG            |
| LO25    | NEAR   | 08E3H  | CODE SEG            |
| LO2K    | NEAR   | 01D3H  | CODE SEG            |
| LO4     | NEAR   | 0891H  | CODE SEG            |
| LO44    | NEAR   | 0889H  | CODE SEG            |
| LO4K    | NEAR   | 01DFH  | CODE SEG            |
| LO5     | NEAR   | 0844H  | CODE SEG            |
| LO55    | NEAR   | 083CH  | CODE SEG            |
| LO6     | NEAR   | 07F7H  | CODE SEG            |
| LO66    | NEAR   | 07EFH  | CODE SEG            |
| LO7     | NEAR   | 07E7H  | CODE SEG            |
| LO77    | NEAR   | 07AFH  | CODE SEG            |
| LO8     | NEAR   | 0777H  | CODE SEG            |
| LO88    | NEAR   | 076FH  | CODE SEG            |
| LO9     | NEAR   | 00C4H  | CODE SEG            |
| LO91    | NEAR   | 016CH  | CODE SEG            |
| LO91L   | NEAR   | 09E9H  | CODE SEG            |
| LO92L   | NEAR   | 096DH  | CODE SEG            |
| LO93L   | NEAR   | 08F9H  | CODE SEG            |
| LO94L   | NEAR   | 089FH  | CODE SEG            |
| LO95    | NEAR   | 018DH  | CODE SEG            |

| NAME              | TYPE   | VALUE | ATTRIBUTES |
|-------------------|--------|-------|------------|
| L095L             | L      | 0852H | CODE SEG   |
| L096L             | L      | 0805H | CODE SEG   |
| L097L             | L      | 07C5H | CODE SEG   |
| L098L             | L      | 0785H | CODE SEG   |
| L09A:             | L      | 0979H | CODE SEG   |
| L09B:             | L      | 0905H | CODE SEG   |
| L09C:             | L      | 08ABH | CODE SEG   |
| L09D:             | L      | 085EH | CODE SEG   |
| L09E:             | L      | 0811H | CODE SEG   |
| L09F:             | L      | 07D1H | CODE SEG   |
| L09G:             | L      | 0791H | CODE SEG   |
| L09H:             | L      | 0751H | CODE SEG   |
| L0A:              | L      | 0489H | CODE SEG   |
| L0B:              | L      | 0108H | CODE SEG   |
| L0R:              | L      | 0203H | CODE SEG   |
| LSR1:             | L      | 056EH | CODE SEG   |
| LSR2:             | L      | 0571H | CODE SEG   |
| LSR3:             | L      | 0559H | CODE SEG   |
| LT0:              | L      | 0682H | CODE SEG   |
| LT09:             | L      | 05CFH | CODE SEG   |
| LT1:              | L      | 067CH | CODE SEG   |
| LT10:             | L      | 0646H | CODE SEG   |
| LT11:             | L      | 0640H | CODE SEG   |
| LT12:             | L      | 063AH | CODE SEG   |
| LT13:             | L      | 0629H | CODE SEG   |
| LT131:            | L      | 0634H | CODE SEG   |
| LT14:             | L      | 0618H | CODE SEG   |
| LT141:            | L      | 0623H | CODE SEG   |
| LT151:            | L      | 0607H | CODE SEG   |
| LT152:            | L      | 0612H | CODE SEG   |
| LT19:             | L      | 05D2H | CODE SEG   |
| LT20:             | L      | 0676H | CODE SEG   |
| LT29:             | L      | 0694H | CODE SEG   |
| LT3:              | L      | 05D5H | CODE SEG   |
| LT31:             | L      | 0670H | CODE SEG   |
| LT39:             | L      | 021DH | CODE SEG   |
| LT4:              | L      | 05D8H | CODE SEG   |
| LT49:             | L      | 066AH | CODE SEG   |
| LT5:              | L      | 05DBH | CODE SEG   |
| LT59:             | L      | 0664H | CODE SEG   |
| LT6:              | L      | 05DEH | CODE SEG   |
| LT7:              | L      | 065EH | CODE SEG   |
| LT8:              | L      | 065BH | CODE SEG   |
| LT9:              | L      | 0652H | CODE SEG   |
| LTB4:             | L      | 064CH | CODE SEG   |
| LTB5:             | L      | 022DH | CODE SEG   |
| LTB6:             | L      | 0243H | CODE SEG   |
| LTE:              | L      | 025CH | CODE SEG   |
| LTE1:             | L      | 0685H | CODE SEG   |
| MOD_CLK_0:        | NUMBER | 008AH | CODE SEG   |
| MOD_CLK_90:       | NUMBER | 0000H | CODE SEG   |
| MOD_CLK_SYN:      | NUMBER | 0463H | CODE SEG   |
| MOD_CLK_UPDATE:   | NUMBER | 043EH | CODE SEG   |
| MOD_CLK_UPDATE_1: | NUMBER | 0423H | CODE SEG   |

SIZE=001AH CODE SEG  
 SIZE=0025H CODE SEG  
 SIZE=001BH CODE SEG

| NAME           | TYPE    | VALUE | ATTRIBUTES          |
|----------------|---------|-------|---------------------|
| NOADD          | .       | 0507H | CODE_SEG            |
| NXTBIT:        | L       | 04F2H | CODE_SEG            |
| PA:            | L       | 1452H | CODE_SEG            |
| PAP:           | Y       | 1450H | (3) SAMP            |
| PHASE          | NUMBER  | 0040H | SAMP                |
| PLBL:          | L       | 06F2H | CODE_SEG            |
| PLBL1          | L       | 06F7H | CODE_SEG            |
| PLBL3          | L       | 06FFH | CODE_SEG            |
| PLBLA          | L       | 0709H | CODE_SEG            |
| PLBLC          | L       | 0711H | CODE_SEG            |
| 0221:          | L       | 0912H | CODE_SEG            |
| 0222:          | L       | 091FH | CODE_SEG            |
| 0223:          | L       | 092CH | CODE_SEG            |
| 0224:          | L       | 0939H | CODE_SEG            |
| 0229:          | L       | 093FH | CODE_SEG            |
| 0331:          | L       | 08B8H | CODE_SEG            |
| 0332:          | L       | 08C5H | CODE_SEG            |
| 0339:          | L       | 08CBH | CODE_SEG            |
| 0441:          | L       | 086BH | CODE_SEG            |
| 0449:          | L       | 0871H | CODE_SEG            |
| 0551:          | L       | 081EH | CODE_SEG            |
| 0559:          | L       | 0824H | CODE_SEG            |
| QUE            | L       | 0556H | SIZE=0041H CODE_SEG |
| R0:            | Y       | 1478H | SAMP                |
| R1:            | Y       | 147AH | SAMP                |
| R10:           | Y       | 148CH | SAMP                |
| R11:           | Y       | 148EH | SAMP                |
| R12:           | Y       | 1490H | SAMP                |
| R13:           | Y       | 1492H | SAMP                |
| R14:           | Y       | 1493H | SAMP                |
| R15:           | Y       | 1494H | SAMP                |
| R16:           | Y       | 1495H | SAMP                |
| R2:            | Y       | 147CH | SAMP                |
| R3:            | Y       | 147EH | SAMP                |
| R4:            | Y       | 1480H | SAMP                |
| R5:            | Y       | 1482H | SAMP                |
| R6:            | Y       | 1484H | SAMP                |
| R7:            | Y       | 1486H | SAMP                |
| R8:            | Y       | 1488H | SAMP                |
| R9:            | Y       | 148AH | SAMP                |
| RES            | SEGMENT | 0000H | SIZE=0005H PARA ABS |
| SAMP:          | Y       | 0000H | (2000) SAMP         |
| SAMPLE_MASK:   | SEGMENT | 0FFFH | SIZE=1496H WORD ABS |
| SIGN_BIT_MASK: | SEGMENT | 8000H |                     |
| SROOT:         | NUMBER  | 0510H |                     |
| STACK_SEG:     | P       | 0032H | SIZE=0046H CODE_SEG |
| STACK_TOP:     | Y       | 0080H | SIZE=0032H WORD_ABS |
| SWP:           | NUMBER  | 0080H | STACK_SEG           |
| THREE_7_1:     | P       | 096EH | SIZE=004CH CODE_SEG |
| THREE_7_2:     | P       | 08FAH | SIZE=0074H CODE_SEG |
| THREE_7_3:     | P       | 08FAH | SIZE=005AH CODE_SEG |
| THREE_7_4:     | P       | 0853H | SIZE=004DH CODE_SEG |
| THREE_7_5:     | P       | 0806H | SIZE=004DH CODE_SEG |
| THREE_7_6:     | P       | 07C6H | SIZE=0040H CODE_SEG |

| NAME           | VALUE | ATTRIBUTES          |
|----------------|-------|---------------------|
| THREE_7_7      | 0786H | SIZE=0040H CODE_SEG |
| THREE_7_8      | 0746H | SIZE=0040H CODE_SEG |
| TLBL4          | 0725H | CODE_SEG            |
| TLBT1          | 06C9H | CODE_SEG            |
| TLBT3          | 06CEH | CODE_SEG            |
| TLBTA          | 06D6H | CODE_SEG            |
| TLBTC          | 06E0H | CODE_SEG            |
| TLBX           | 0723H | CODE_SEG            |
| XY             | 11F8H | (300) SAMP          |
| ZC_ADC         | 02C8H | SIZE=00A2H CODE_SEG |
| ZC_MASK_OF_ADC | 0040H |                     |
| ZC_MASK_OF_SWP | 0040H |                     |
| ZCC            | 1460H | (12) SAMP           |
| ZCCF           | 145EH | SAMP                |

END OF SYMBOL TABLE LISTING

ASSEMBLY COMPLETE, NO ERRORS FOUND

INPUT FILE: :F3:A2.LNK

OUTPUT FILE: :F3:A2

CONTROLS SPECIFIED IN INVOCATION COMMAND:

DATE: 14/07/86 TIME:  
WARNING 63: SS AND SP REGISTERS NOT INITIALIZED  
WARNING 64: DS REGISTER NOT INITIALIZED

MEMORY MAP OF MODULE SHUM

MODULE START ADDRESS PARAGRAPH = FC50H OFFSET = 0000H  
SEGMENT MAP

| START  | STOP   | LENGTH | ALIGN | NAME      | CLASS | OVERLAY |
|--------|--------|--------|-------|-----------|-------|---------|
| 00200H | 00200H | 0000H  | G     | ??SEG     |       |         |
| 00400H | 00431H | 0032H  | A     | STACK_SEG |       |         |
| 00450H | 018E5H | 1496H  | A     | SAMP      |       |         |
| FC000H | FC385H | 0386H  | A     | ATCS      |       |         |
| FC500H | FC8B9H | 09BAH  | A     | CODE_SEG  |       |         |
| FFFF0H | FFFF4H | 0005H  | A     | RES       |       |         |

A P P E N D I X D

Program Listing of the Software of Microcomputer.

```

10 REM PROG H7
20 DIM A(20) ! Va
30 DIM B(20) ! ANG Va
40 DIM C(20) ! Vb
50 DIM D(20) ! ANG Vb
60 DIM E(20) ! Vc
70 DIM F(20) ! ANG Vc
80 DIM Z(500) ! RAW DATA
90 DEG
100 RESET 7 ! RESET HPIB
110 ! #####
120 ! POLL FOR HPIB READINESS
130 ! #####
140 S=SPOLL(709) ! SERIAL POLL
150 DISP S ! STATUS OF HPIB
160 IF NOT BIT(S,6) THEN 140
170 DISP "SQR OK ?"
180 REM SERVICE REQUEST
190 DISP "S = ";S
200 IF NOT BIT(S,0) THEN 140
210 REM TEST READINESS OF HPIB
220 DISP "BIT 0 SET OK"
230 ENTER 709 USING "#,W" ; B
240 REM B IS TOTAL NUMBER OF
250 REM INPUT SAMPLES AND EACH
260 REM CONSISTS OF ONE WORD IN
270 REM MEMORY.
280 DISP " B=";B
290 ! #####
300 ! INPUT DATA FROM HPIB
310 ! #####
320 FOR I=0 TO B-1
330 ENTER 709 USING "#,W" ; Z(I)
340 REM Z(I) IS AMP. OR ANG.
350 NEXT I
360 ! #####
370 ! SCALE HARMONIC COMPONENTS
380 ! #####
390 F=Z(0)/10
400 REM RECOVER THE FUND. FREQ.
410 PRINT "FUND. FREQ.=";F;" HZ"
420 PRINT
430 C=B-1
440 REM C IS TOTAL NUMBER OF RAW
DATA OF AMP. AND ANG.
450 M=C DIV 12
460 REM M IS ORDER OF HARMONICS
NEEDED TO BE HANDLED.
470 J=1
480 REM J=1 IS INDEX TO ADDRESS
THE FIRST DATA, Va, IN MEMORY.

490 L=7
500 REM L=7 IS INDEX TO ADDRESS
THE FIRST CURRENT AMPLITUDE,
Ia.
510 FOR K=1 TO M
520 FOR I=J TO J+5 STEP 2
530 Z(I)=.0922*Z(I)
540 REM .0922 IS SCALING FACTOR
OF VOLTAGE = (340/5)(5/2^12)
*(PI/2)(1/SQR 2)

550 REM (340/5) FROM INPUT
SCALING CIRCUIT.
560 REM (5/2^12) FROM ADC.
570 REM (PI/2) FROM COEF. OF
EQN SET (3),(1/SQR 2) IS RMS

580 NEXT I
590 J=J+12
600 NEXT K
610 FOR K=1 TO M
620 FOR I=L TO L+5 STEP 2
630 Z(I)=.001965*Z(I)
640 REM .001965 IS INPUT CURRENT
SCALING FACTOR = (1/SQR 2)*
(1/6.9)(5/2^12)(PI/2)

650 REM (1/6.9) SCALING FACTOR.
660 NEXT I
670 L=L+12
680 NEXT K
690 FOR I=2 TO C STEP 2
700 Z(I)=Z(I)/10
710 REM SCALING FACTOR OF ANG.
720 NEXT I
730 ! #####
740 ! PRINT RESULTANT
750 ! HARMONIC COMPONENTS
760 ! #####
770 H=1 ! H IS HARMONIC ORDER
780 FOR I=1 TO C STEP 12
790 PRINT "HA. ORDER=";H
800 PRINT
810 PRINT "VA=";Z(I)
820 PRINT "ANG VA=";Z(I+1)
830 PRINT "VB=";Z(I+2)
840 PRINT "ANG VB=";Z(I+3)
850 PRINT "VC=";Z(I+4)
860 PRINT "ANG VC=";Z(I+5)
870 PRINT
880 PRINT "IA=";Z(I+6)
890 PRINT "ANG IA=";Z(I+7)
900 PRINT "IB=";Z(I+8)
910 PRINT "ANG IB=";Z(I+9)
920 PRINT "IC=";Z(I+10)
930 PRINT "ANG IC=";Z(I+11)
940 PRINT
950 PRINT
960 H=H+1
970 NEXT I
980 H=H-1
990 ! #####
1000 ! RELOCATE RESULTANT
1010 ! HARMONIC COMPONENTS
1020 ! IN MEMORY
1030 ! #####
1040 REM STORE Va, Ia
1050 T=0
1060 J=0
1070 FOR I=T TO 12*6+6+T STEP 6
1080 A(J)=Z(I)

```

```

1090 J=J+1
1100 NEXT I
1110 REM STORE ANG OF Va AND Ia
1120 T=T+1
1130 J=0
1140 FOR I=T TO 12*6+6+T STEP 6
1150 B(J)=Z(I)
1160 J=J+1
1170 NEXT I
1180 REM STORE Vb, Ib
1190 T=T+1
1200 J=0
1210 FOR I=T TO 12*6+6+T STEP 6
1220 C(J)=Z(I)
1230 J=J+1
1240 NEXT I
1250 REM STORE ANG OF Vb AND Ib
1260 T=T+1
1270 J=0
1280 FOR I=T TO 12*6+6+T STEP 6
1290 D(J)=Z(I)
1300 J=J+1
1310 NEXT I
1320 REM STORE Vc, Ic
1330 T=T+1
1340 J=0
1350 FOR I=T TO 12*6+6+T STEP 6
1360 E(J)=Z(I)
1370 J=J+1
1380 NEXT I
1390 REM STORE ANG OF Vc AND Ic
1400 T=T+1
1410 J=0
1420 FOR I=T TO 12*6+6+T STEP 6
1430 F(J)=Z(I)
1440 J=J+1
1450 NEXT I
1460 ! #####
1470 ! CALCULATE U0, U+ AND U-
1480 ! #####
1490 N=0
1500 FOR I=1 TO H
1510 Q=0
1520 FOR P=1 TO 2
1530 G=A(N)*COS(B(N))
1540 W=A(N)*SIN(B(N))
1550 X=G+C(N)*COS(D(N))+E(N)*COS
(F(N))
1560 Y=W+C(N)*SIN(D(N))+E(N)*SIN
(F(N))
1570 K=SQR(X^2+Y^2)/3
1580 L=ATN2(Y,X)
1590 X=G+C(N)*COS(120+D(N))+E(N)
*COS(240+F(N))
1600 Y=W+C(N)*SIN(120+D(N))+E(N)
*SIN(240+F(N))
1610 M=SQR(X^2+Y^2)/3
1620 R=ATN2(Y,X)
1630 X=G+C(N)*COS(240+D(N))+E(N)
*COS(120+F(N))

```

```

1640 Y=W+C(N)*SIN(240+D(N))+E(N)
*SIN(120+F(N))
1650 U=SQR(X^2+Y^2)/3
1660 V=ATN2(Y,X)
1670 N=N+1
1680 IF Q=1 THEN GOTO 1850
1690 ! #####
1700 ! PRINT RESULTANT
1710 ! SYMMETRICAL COMPONENTS
1720 ! OF HARMONICS.
1730 ! #####
1740 PRINT "HA. ORDER= ";I
1750 PRINT
1760 PRINT "V0= ";K
1770 PRINT "ANG V0= ";L
1780 PRINT "V+= ";M
1790 PRINT "ANG V+= ";R
1800 PRINT "V-= ";U
1810 PRINT "ANG V-= ";V
1820 PRINT
1830 Q=1
1840 GOTO 1940
1850 PRINT "I0= ";K
1860 PRINT "ANG I0= ";L
1870 PRINT "I+= ";M
1880 PRINT "ANG I+= ";R
1890 PRINT "I-= ";U
1900 PRINT "ANG I-= ";V
1910 PRINT
1920 PRINT
1930 Q=0
1940 NEXT P
1950 NEXT I
1960 ! #####
1970 ! CALCULATE RESULTANT
1980 ! PHASE VOLTAGES
1990 ! AND CURRENTS.
2000 ! #####
2010 K=SQR(2)
2020 L=0
2030 M=0
2040 N=0
2050 Q=0
2060 R=0
2070 Z=0
2080 FOR P=0 TO 360
2090 U=0
2100 V=0
2110 W=0
2120 X=0
2130 Y=0
2140 O=0
2150 FOR G=1 TO H
2160 T=2*(G-1)
2170 U=U+A(T)*SIN(G*(P-B(T)/G))*
K
2180 V=V+C(T)*SIN(G*(P-D(T)/G))*
K
2190 W=W+E(T)*SIN(G*(P-F(T)/G))*
K

```

```

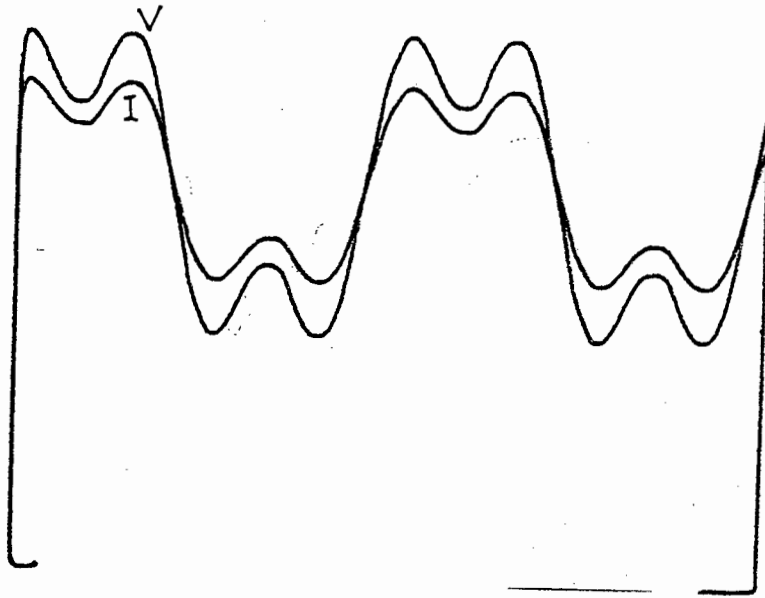
2200 S=T+1
2210 X=X+A(S)*SIN(G*(P-B(S)/G))*
      K
2220 Y=Y+C(S)*SIN(G*(P-D(S)/G))*
      K
2230 O=O+E(S)*SIN(G*(P-F(S)/G))*
      K
2240 NEXT G
2250 L=L+U^2
2260 M=M+V^2
2270 N=N+W^2
2280 Q=Q+X^2
2290 R=R+Y^2
2300 Z=Z+O^2
2310 NEXT P
2320 A=L/360
2330 B=SQR(A)
2340 C=M/360
2350 D=SQR(C)
2360 E=N/360
2370 F=SQR(E)
2380 G=Q/360
2390 H=SQR(G)
2400 I=R/360
2410 J=SQR(I)
2420 K=Z/360
2430 L=SQR(K)
2440 ! #####
2450 ! PRINT RESULTANT RMS
2460 ! OF Va,Vb,Vc, Ia, Ib, Ic.
2470 ! #####
2480 PRINT
2490 PRINT
2500 PRINT "VA= ";B
2510 PRINT "VB= ";D
2520 PRINT "VC= ";F
2530 PRINT "IA= ";H
2540 PRINT "IB= ";J
2550 PRINT "IC= ";L
2560 END

```

A P P E N D I X E

Note : The units of voltage and current used in this appendix are  
V and A respectively.

T E S T 1



Resultant Waveform of Harmonics : 1st + 3rd

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

|     |               |      |       |
|-----|---------------|------|-------|
| VA= | 67.0529388831 | 68.8 | -2.61 |
| VB= | 67.8032042389 | 68.8 | -1.48 |
| VC= | 69.6338462756 | 68.7 | +1.34 |
| IA= | 4.55966540441 | 4.48 | +1.75 |
| IB= | 4.32040754068 | 4.51 | -4.40 |
| IC= | 4.48314959128 | 4.50 | -0.45 |

FUND. FREQ = 50 HZ

HA. ORDER= 1

VA= 60.8876  
ANG VA= 0  
VB= 61.7244  
ANG VB= 240  
VC= 63.6252  
ANG VC= 120

IA= 4.22432  
ANG IA= 4.6  
IB= 3.953365  
ANG IB= 244.6  
IC= 4.148115  
ANG IC= 124.6

HA. ORDER= 2

VA= .3688  
ANG VA= 79.7  
VB= .3603  
ANG VB= 319.7  
VC= .3466  
ANG VC= 199.7

IA= .013755  
ANG IA= 87.5  
IB= .01179  
ANG IB= 327.5  
IC= .01179  
ANG IC= 207.5

HA. ORDER= 3

VA= 28.0054  
ANG VA= 26.9  
VB= 27.3522  
ANG VB= 266.9  
VC= 27.7146  
ANG VC= 146.9

IA= 1.711515  
ANG IA= 48.3  
IB= 1.69776  
ANG IB= 288.3  
IC= 1.676145  
ANG IC= 168.3

HA. ORDER= 4

VA= .0922  
ANG VA= 87.9  
VB= .0921  
ANG VB= 327.9  
VC= .0896  
ANG VC= 207.9

IA= .00986  
ANG IA= 77.9  
IB= .009257  
ANG IB= 317.9  
IC= .008579  
ANG IC= 197.9

HA. ORDER= 5

VA= 1.5362  
ANG VA= 270.5  
VB= 1.46596  
ANG VB= 150.5  
VC= 1.61064  
ANG VC= 30.5

IA= .036055  
ANG IA= 267.9  
IB= .038545  
ANG IB= 147.9  
IC= .03169  
ANG IC= 27.9

HA. ORDER= 6

VA= .0922  
ANG VA= 347.9  
VB= .0936  
ANG VB= 227.9  
VC= .09657  
ANG VC= 107.9

IA= .02075  
ANG IA= -2.1  
IB= .02358  
ANG IB= 237.9  
IC= .021615  
ANG IC= 117.9

HA. ORDER= 7

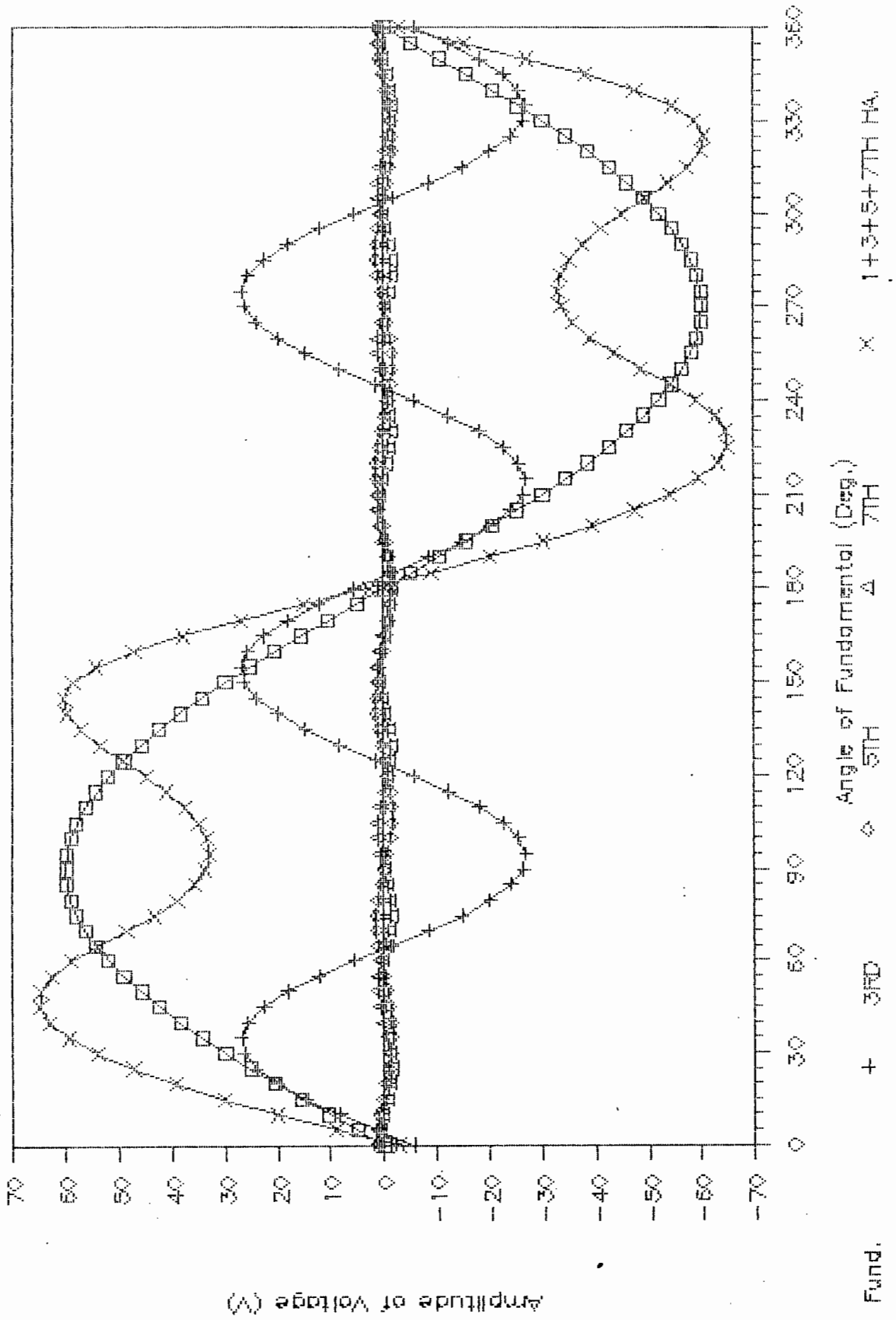
VA= 1.1752  
ANG VA= 268.9  
VB= 1.2576  
ANG VB= 147.9  
VC= 1.1986  
ANG VC= 27.9

IA= .021615  
ANG IA= 277.9  
IB= .01972  
ANG IB= 157.9  
IC= .024545  
ANG IC= 37.9

Amplitudes and phase angles of harmonic components.

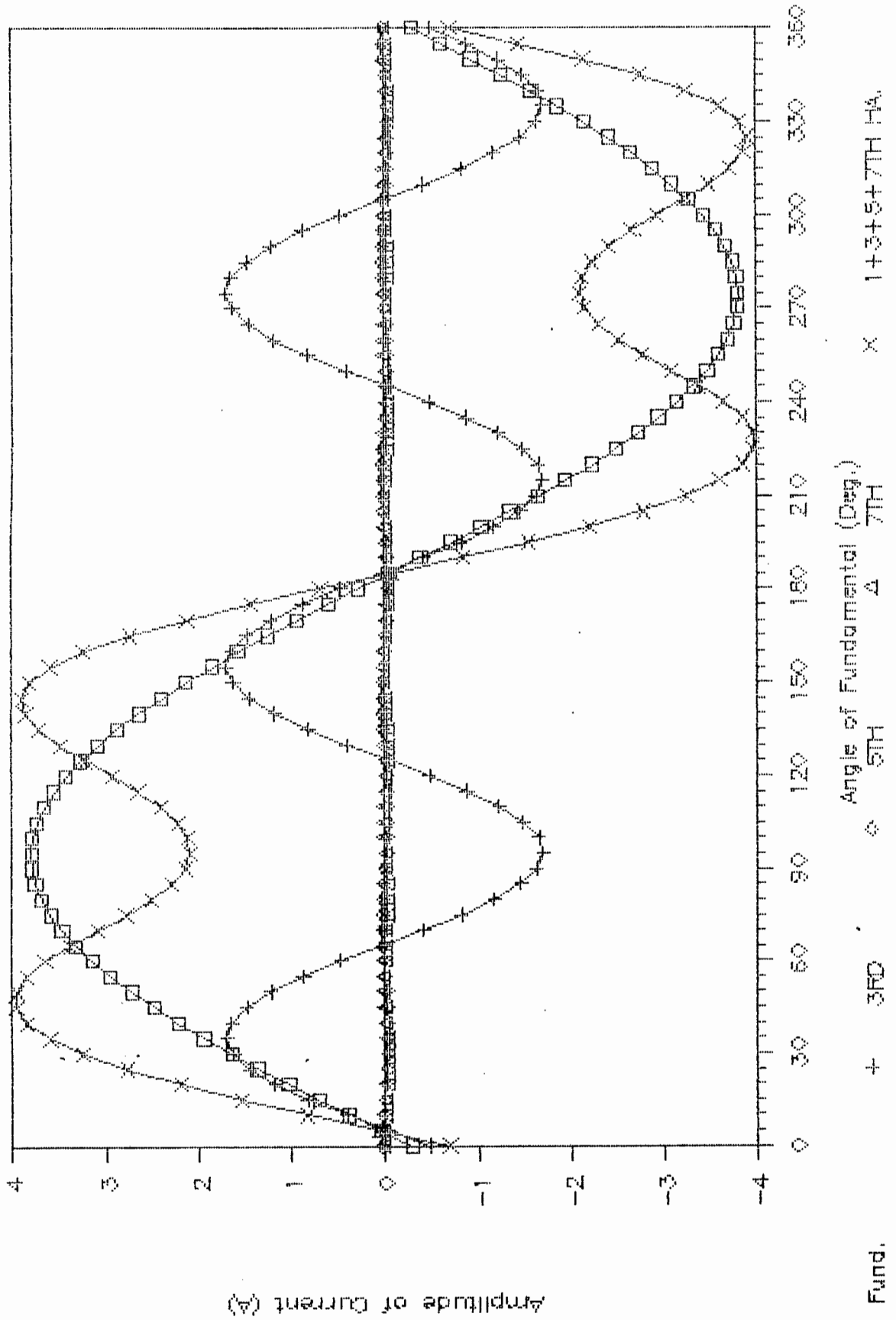
Reconstructed waveforms

# TEST\_1

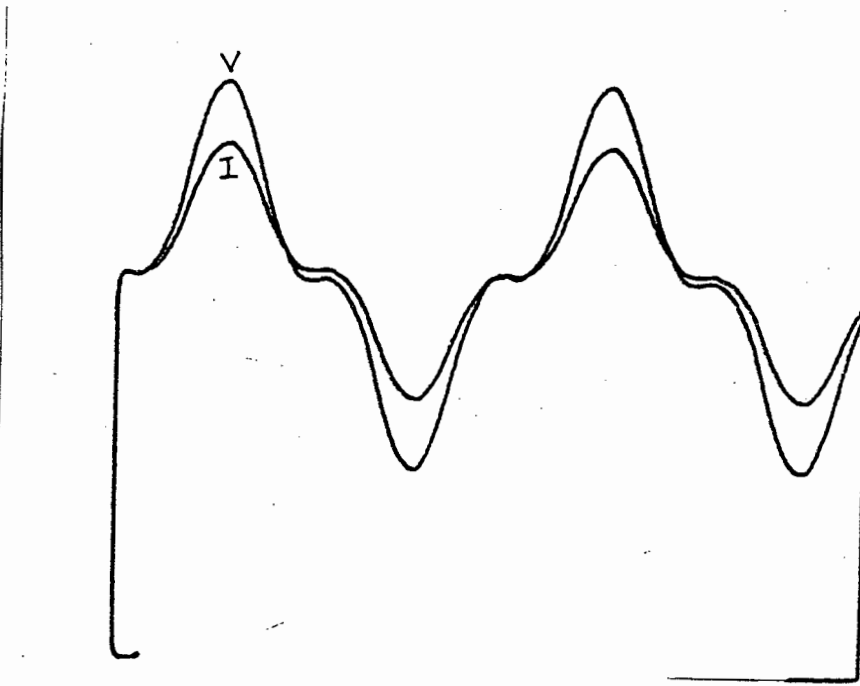


Reconstructed waveforms

TEST 1



T E S T 2



Resultant Waveform of Harmonics : 1st + 3rd

| Resultant RMS Values<br>of 3 phase components | Analogue Meters readings<br>of 3 phase power supply | DEVIATION<br>( % ) |
|-----------------------------------------------|-----------------------------------------------------|--------------------|
|-----------------------------------------------|-----------------------------------------------------|--------------------|

|                   |      |       |
|-------------------|------|-------|
| VA= 63.5193948132 | 66.5 | -0.82 |
| VB= 64.3324605928 | 66.4 | -2.06 |
| VC= 64.4957617223 | 66.6 | -4.35 |
| IA= 3.28211639887 | 3.35 | -2.13 |
| IB= 3.2624909387  | 3.31 | -1.53 |
| IC= 3.38656677526 | 3.36 | +0.88 |

FUND. FREQ = 50.1 HZ

HA. ORDER= 1

VA= 61.544  
ANG VA= 0  
VB= 62.2706  
ANG VB= 240  
VC= 62.5828  
ANG VC= 120

IA= 3.110595  
ANG IA= 6  
IB= 3.08505  
ANG IB= 240.6  
IC= 3.232425  
ANG IC= 120.6

HA. ORDER= 2

VA= .1944  
ANG VA= 95.8  
VB= .23572  
ANG VB= 335.8  
VC= .2272  
ANG VC= 215.8

IA= .053055  
ANG IA= 110.3  
IB= .053051  
ANG IB= 350.3  
IC= .055548  
ANG IC= 230.3

HA. ORDER= 3

VA= 15.674  
ANG VA= 186.6  
VB= 15.8584  
ANG VB= 66.6  
VC= 15.235  
ANG VC= 306.6

IA= 1.043415  
ANG IA= 190.4  
IB= 1.051275  
ANG IB= 70.4  
IC= .99499  
ANG IC= 310.4

HA. ORDER= 4

VA= .2844  
ANG VA= 253.2  
VB= .2305  
ANG VB= 133.2  
VC= .2858  
ANG VC= 13.2

IA= .01104  
ANG IA= 270.6  
IB= .01198  
ANG IB= 150.6  
IC= .010021  
ANG IC= 30.6

HA. ORDER= 5

VA= .6192  
ANG VA= 234.4  
VB= .6305  
ANG VB= 114.4  
VC= .5956  
ANG VC= 354.4

IA= .06681  
ANG IA= 247.2  
IB= .067705  
ANG IB= 127.2  
IC= .068775  
ANG IC= 367.2

HA. ORDER= 6

VA= .5532  
ANG VA= 73.2  
VB= .5206  
ANG VB= 313.2  
VC= .5298  
ANG VC= 193.2

IA= .010025  
ANG IA= 87.6  
IB= .01061  
ANG IB= 327.6  
IC= .01139  
ANG IC= 207.6

HA. ORDER= 7

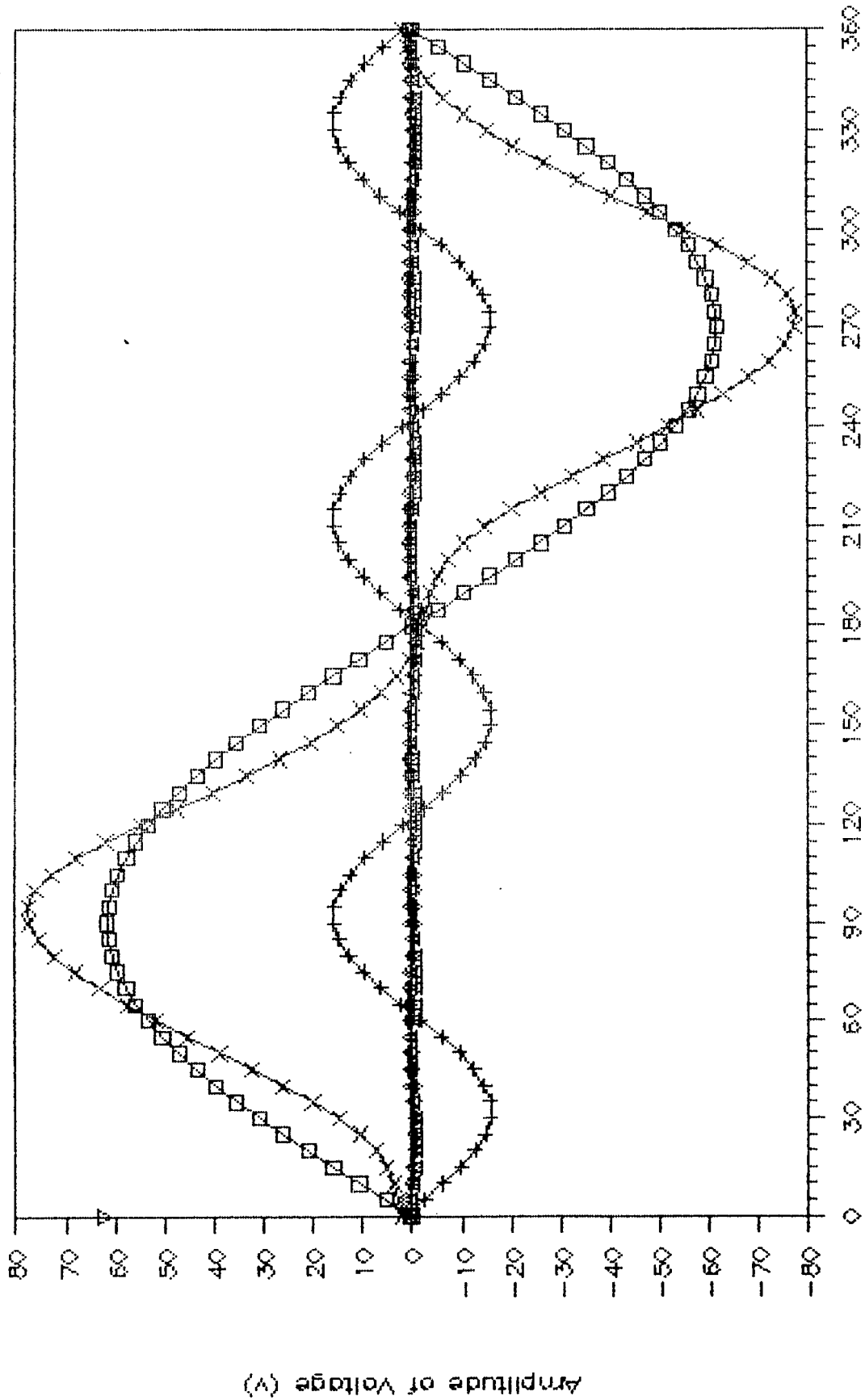
VA= .7298  
ANG VA= 241.4  
VB= .7397  
ANG VB= 121.4  
VC= .7376  
ANG VC= 1.4

IA= .010565  
ANG IA= 248.8  
IB= .00978  
ANG IB= 128.8  
IC= .012755  
ANG IC= 8.8

Amplitudes and phase angles of harmonic components.

Reconstructed waveforms

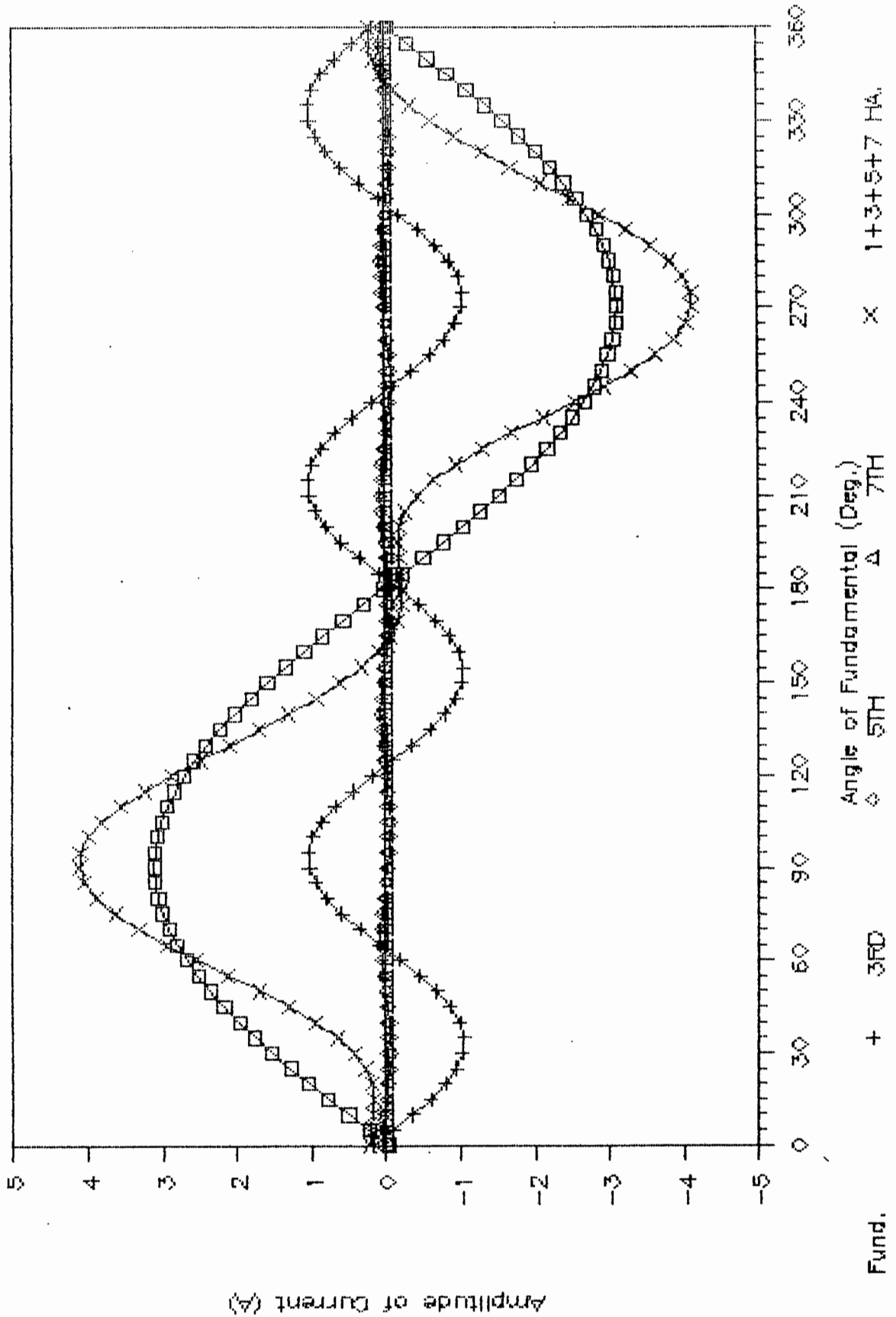
TEST\_2



□ Fund.    + 3RD    Δ 5TH    × 1+3+5+7 HA.

Reconstructed waveforms

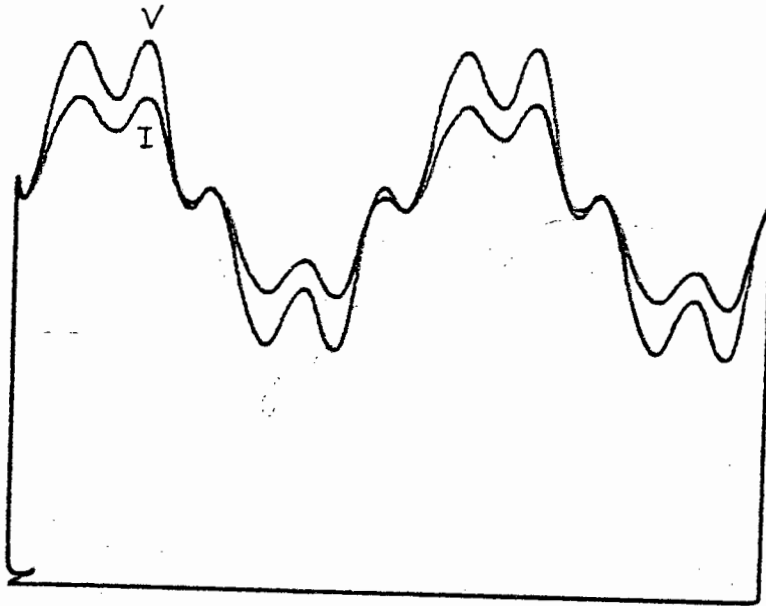
TEST\_2



|                        |                        |
|------------------------|------------------------|
| HA. ORDER= 1           | HA. ORDER= 4           |
| V0= .307726595819      | V0= 1.82044866262E-2   |
| ANG V0= 162.970047695  | ANG V0= -45.5279116091 |
| V+= 62.1324666667      | V+= .2669              |
| ANG V+= 0              | ANG V+= -106.8         |
| V-= .307726595819      | V-= 1.82044866267E-2   |
| ANG V-= -162.970047695 | ANG V-= -168.072088392 |
| I0= 4.54694565057E-2   | I0= 5.65667845223E-4   |
| ANG I0= 111.266584568  | ANG I0= -178.066244557 |
| I+= 3.14269            | I+= 1.10136666667E-2   |
| ANG I+= .599999999997  | ANG I+= -89.4          |
| I-= 4.54694565073E-2   | I-= 5.656678452E-4     |
| ANG I-= -110.066584566 | ANG I-= -.733755442334 |
| HA. ORDER= 2           | HA. ORDER= 5           |
| V0= 1.25957947128E-2   | V0= 1.02812126394E-2   |
| ANG V0= -72.9398219061 | ANG V0= 155.901455161  |
| V+= .219106666666      | V+= .6151              |
| ANG V+= 95.8           | ANG V+= -125.6         |
| V-= 1.25957947128E-2   | V-= 1.02812126392E-2   |
| ANG V-= -95.4601780928 | ANG V-= -47.1014551595 |
| I0= 6.45706363433E-3   | I0= 6.0453434789E-4    |
| ANG I0= 176.699152836  | ANG I0= 36.4733590374  |
| I+= 4.78846666667E-2   | I+= 6.77203333333E-2   |
| ANG I+= 110.3          | ANG I+= -112.8         |
| I-= 6.4570636343E-3    | I-= 6.04534347847E-4   |
| ANG I-= 43.9008471639  | ANG I-= 97.9266409574  |
| HA. ORDER= 3           | HA. ORDER= 6           |
| V0= .184895153474      | V0= 9.70383658393E-3   |
| ANG V0= 109.867603214  | ANG V0= 89.0837667315  |
| V+= 15.5891333333      | V+= .534533333333      |
| ANG V+= -173.4         | ANG V+= 73.2           |
| V-= .184895153472      | V-= 9.70383658353E-3   |
| ANG V-= -96.6676032156 | ANG V-= 57.3162332697  |
| I0= 1.75985502087E-2   | I0= 3.95379564473E-4   |
| ANG I0= 122.992216517  | ANG I0= -127.115003951 |
| I+= 1.02989333333      | I+= .010675            |
| ANG I+= -169.6         | ANG I+= 87.6           |
| I-= 1.75985502088E-2   | I-= 3.9537956448E-4    |
| ANG I-= -102.192216517 | ANG I-= -57.684996047  |
| HA. ORDER= 7           | HA. ORDER= 7           |
| V0= 3.0116440691E-3    | V0= 3.0116440691E-3    |
| ANG V0= 73.0124815438  | ANG V0= 73.0124815438  |
| V+= .7357              | V+= .7357              |
| ANG V+= -118.6         | ANG V+= -118.6         |
| V-= 3.01164406931E-3   | V-= 3.01164406931E-3   |
| ANG V-= 49.7875184668  | ANG V-= 49.7875184668  |
| I0= 8.90160722083E-4   | I0= 8.90160722083E-4   |
| ANG I0= -5.94822465143 | ANG I0= -5.94822465143 |
| I+= 1.10333333333E-2   | I+= 1.10333333333E-2   |
| ANG I+= -111.2         | ANG I+= -111.2         |
| I-= 8.90160722063E-4   | I-= 8.90160722063E-4   |
| ANG I-= 143.548224652  | ANG I-= 143.548224652  |

Symmetrical components of harmonics.

T E S T 3



Resultant Waveform of Harmonics : 1st + 5th

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

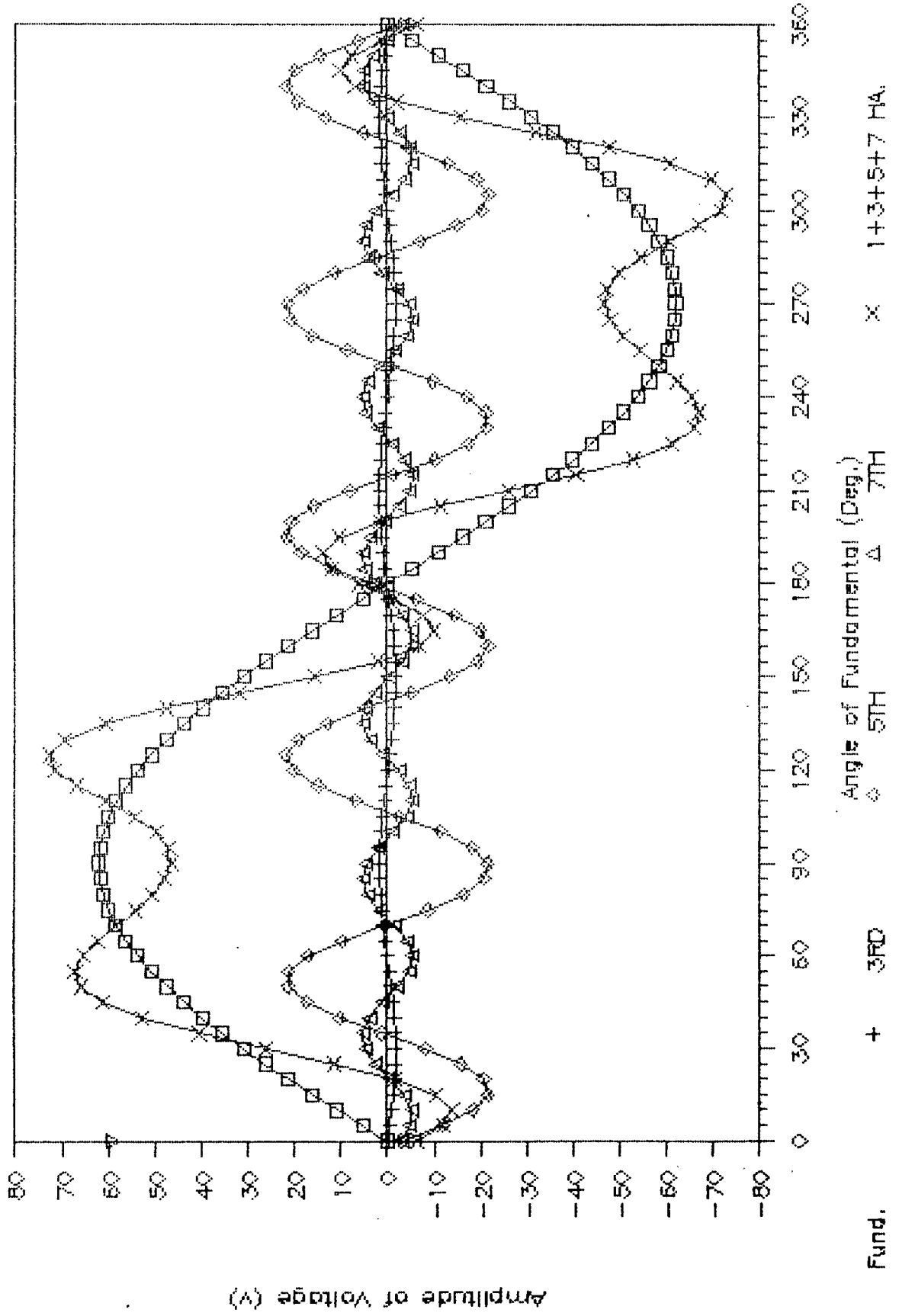
|     |               |      |       |
|-----|---------------|------|-------|
| VA= | 65.9948721091 | 65.6 | +0.59 |
| VB= | 64.3132509633 | 65.2 | -1.38 |
| VC= | 68.5060398004 | 65.8 | +4.0  |
| IA= | 3.59300894235 | 3.60 | -0.29 |
| IB= | 3.53322204009 | 3.61 | -2.27 |
| IC= | 3.71060885465 | 3.58 | +3.50 |

|                       |               |
|-----------------------|---------------|
|                       | HA. ORDER= 4  |
|                       | VA= .0505     |
|                       | ANG VA= 273.7 |
|                       | VB= .04752    |
|                       | ANG VB= 153.7 |
|                       | VC= .05674    |
|                       | ANG VC= 33.7  |
|                       | IA= .008405   |
|                       | ANG IA= 264.5 |
|                       | IB= .00786    |
|                       | ANG IB= 144.5 |
|                       | IC= .008825   |
|                       | ANG IC= 24.5  |
| FUND. FREQ. = 49.9 HZ |               |
| HA. ORDER= 1          |               |
| VA= 62.0506           |               |
| ANG VA= 0             |               |
| VB= 60.086            |               |
| ANG VB= 240           |               |
| VC= 64.54             |               |
| ANG VC= 120           |               |
| IA= 3.267795          |               |
| ANG IA= 5.1           |               |
| IB= 3.20295           |               |
| ANG IB= 245.1         |               |
| IC= 3.42696           |               |
| ANG IC= 125.1         |               |
| HA. ORDER= 2          |               |
| VA= .35178            |               |
| ANG VA= 268.1         |               |
| VB= .34894            |               |
| ANG VB= 148.1         |               |
| VC= .33192            |               |
| ANG VC= 28.1          |               |
| IA= .03144            |               |
| ANG IA= 270.7         |               |
| IB= .033406           |               |
| ANG IB= 150.7         |               |
| IC= .031965           |               |
| ANG IC= 30.7          |               |
| HA. ORDER= 3          |               |
| VA= 1.6596            |               |
| ANG VA= 177.1         |               |
| VB= 1.5674            |               |
| ANG VB= 57.1          |               |
| VC= 1.844             |               |
| ANG VC= 297.1         |               |
| IA= .03537            |               |
| ANG IA= 180.9         |               |
| IB= .03375            |               |
| ANG IB= 60.9          |               |
| IC= .039651           |               |
| ANG IC= 300.9         |               |
|                       | HA. ORDER= 5  |
|                       | VA= 21.7592   |
|                       | ANG VA= 175.7 |
|                       | VB= 22.3124   |
|                       | ANG VB= 55.7  |
|                       | VC= 22.3124   |
|                       | ANG VC= 295.7 |
|                       | IA= 1.440345  |
|                       | ANG IA= 180.1 |
|                       | IB= 1.44624   |
|                       | ANG IB= 60.1  |
|                       | IC= 1.36764   |
|                       | ANG IC= 300.1 |
|                       | HA. ORDER= 6  |
|                       | VA= .0553     |
|                       | ANG VA= 87.1  |
|                       | VB= .0614     |
|                       | ANG VB= 327.1 |
|                       | VC= .0698     |
|                       | ANG VC= 207.1 |
|                       | IA= .080565   |
|                       | ANG IA= 79.7  |
|                       | IB= .060915   |
|                       | ANG IB= 319.7 |
|                       | IC= .07323    |
|                       | ANG IC= 199.7 |
|                       | HA. ORDER= 7  |
|                       | VA= 5.3476    |
|                       | ANG VA= 146.7 |
|                       | VB= 4.5178    |
|                       | ANG VB= 26.7  |
|                       | VC= 4.627     |
|                       | ANG VC= 266.7 |
|                       | IA= .382785   |
|                       | ANG IA= 155.5 |
|                       | IB= .339945   |
|                       | ANG IB= 35.5  |
|                       | IC= .371385   |
|                       | ANG IC= 275.5 |

Amplitudes and phase angles of harmonic components.

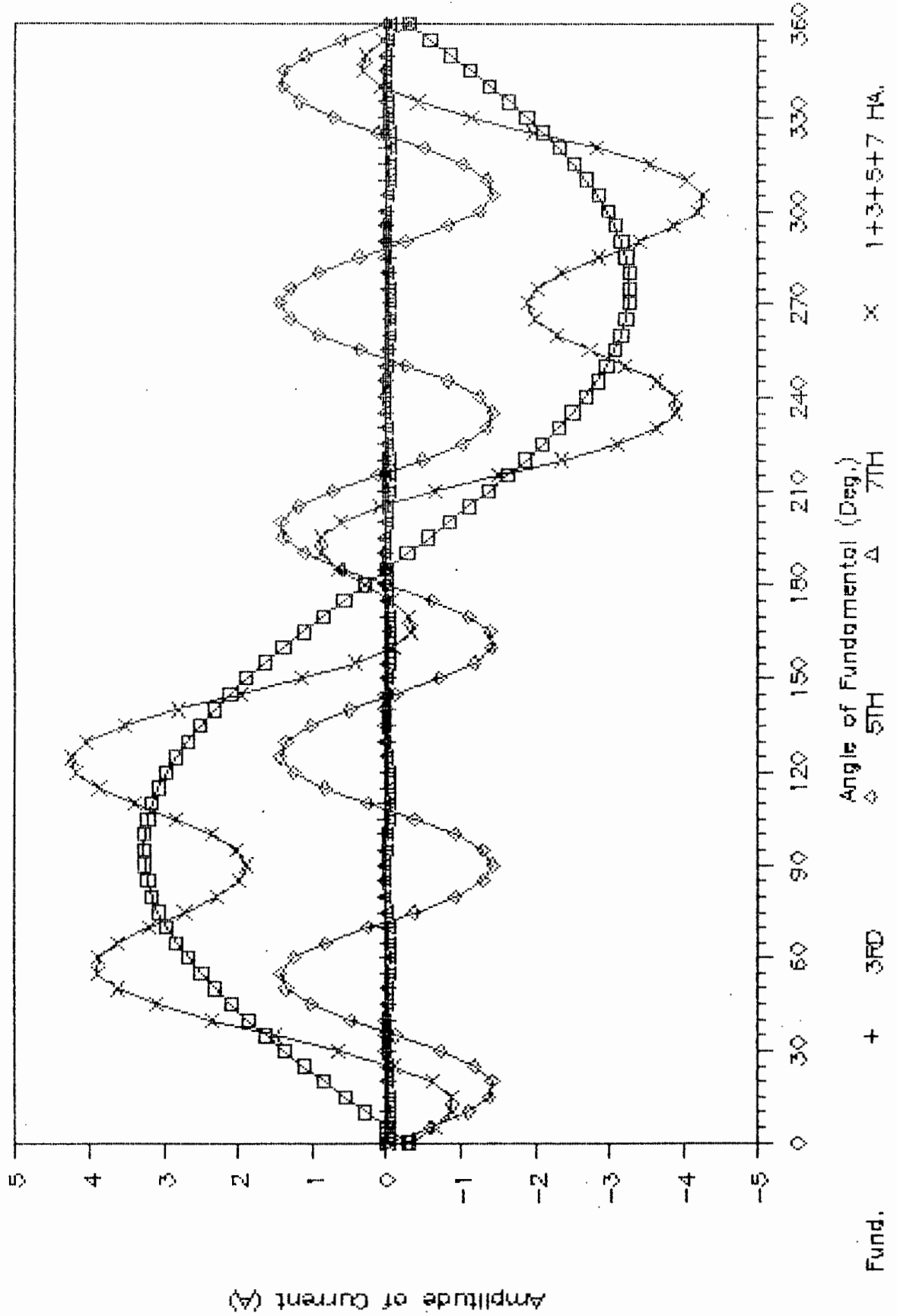
Reconstructed waveforms

# TEST\_3



Reconstructed waveforms

# TEST\_3



Symmetrical components of harmonics.

HR. ORDER = 2

U0 = .260315731372  
 RNG U0 = 153.655389084  
 U+ = 4.8308  
 RNG U+ = 146.7  
 U- = .260315731374  
 RNG U- = 139.744610915

I0 = 1.28099336455E-2  
 RNG I0 = -159.386312056  
 I+ = .364705  
 RNG I+ = 155.5  
 I- = 1.28099336455E-2  
 RNG I- = 110.386312058

HR. ORDER = 6

U0 = 4.2033055775E-3  
 RNG U0 = -128.132534604  
 U+ = 6.21666666663E-2  
 RNG U+ = 87.1  
 U- = 4.20330557753E-3  
 RNG U- = -57.6674653958

I0 = 5.73286795593E-3  
 RNG I0 = 118.024492995  
 I+ = .07157  
 RNG I+ = 79.7  
 I- = 5.73286795593E-3  
 RNG I- = 41.3755070053

HR. ORDER = 5

U0 = 184399999996  
 RNG U0 = -4.29999999175  
 U+ = 22.128  
 RNG U+ = 175.7  
 U- = 184400000009  
 RNG U- = -4.29999999144

I0 = 2.52748536077E-2  
 RNG I0 = 116.23939078  
 I+ = 1.418075  
 RNG I+ = -179.9  
 I- = 2.52748536143E-2  
 RNG I- = -116.039390773

HR. ORDER = 4

U0 = 2.71647647599E-3  
 RNG U0 = 15.237778769  
 U+ = 5.15866666667E-2  
 RNG U+ = -86.3  
 U- = 2.71647647595E-3  
 RNG U- = 172.162222123

I0 = 2.79349442656E-4  
 RNG I0 = -9.72697775913  
 I+ = 8.36333333333E-3  
 RNG I+ = -95.5  
 I- = 2.79349442652E-4  
 RNG I- = 178.776977759

HR. ORDER = 3

U0 = .08131275696  
 RNG U0 = -82.00660535  
 U+ = 1.69033333333  
 RNG U+ = 177.1  
 U- = 8.13127569587E-2  
 RNG U- = 76.2066053494

I0 = 1.76025821972E-3  
 RNG I0 = -74.5069678687  
 I+ = .036257  
 RNG I+ = -179.1  
 I- = 1.7602582197E-3  
 RNG I- = 76.2069678683

HR. ORDER = 2

U0 = 6.2011002608E-3  
 RNG U0 = -144.302775502  
 U+ = .344213333333  
 RNG U+ = -91.9  
 U- = 6.2011002608E-3  
 RNG U- = -39.4972244955

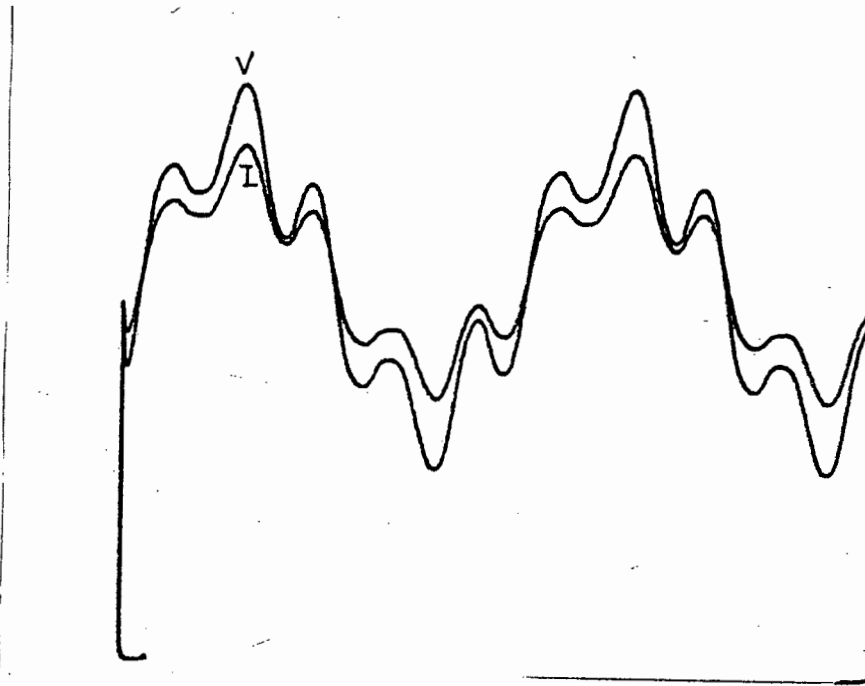
I0 = 5.87710340607E-4  
 RNG I0 = 135.756127626  
 I+ = 3.22703333333E-2  
 RNG I+ = -89.3  
 I- = 5.8771034064E-4  
 RNG I- = 45.6438723732

HR. ORDER = 1

U0 = 1.28873067437  
 RNG U0 = 93.8916791623  
 U+ = 0  
 RNG U+ = 0  
 U- = 1.28873067437  
 RNG U- = -93.8916791623

I0 = 6.65494182947E-2  
 RNG I0 = 108.763279517  
 I+ = 3.299235  
 RNG I+ = 5.1  
 I- = 6.65494182887E-2  
 RNG I- = -98.5632795202

T E S T 4



Resultant Waveform of Harmonics : 1st + 5th

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

|     |               |      |       |
|-----|---------------|------|-------|
| VA= | 69.7298610701 | 68.7 | +1.48 |
| VB= | 70.4163674201 | 68.8 | +2.3  |
| VC= | 68.8809356176 | 68.9 | -0.03 |
| IA= | 3.63730758947 | 3.59 | +1.29 |
| IB= | 3.65189706206 | 3.60 | +1.42 |
| IC= | 3.78473008016 | 3.60 | -5.14 |

FUND. FREQ. = 50.1 HZ

HA. ORDER= 1

VA= 67.49004  
ANG VA= 0  
VB= 68.0202  
ANG VB= 240  
VC= 66.0932  
ANG VC= 120

IA= 3.456435  
ANG IA= 6  
IB= 3.46626  
ANG IB= 240.6  
IC= 3.60708  
ANG IC= 120.6

HA. ORDER= 2

VA= .3688  
ANG VA= 87.8  
VB= .3688  
ANG VB= 327.8  
VC= .3844  
ANG VC= 207.8

IA= .00393  
ANG IA= 95.7  
IB= .003405  
ANG IB= 335.7  
IC= .005895  
ANG IC= 215.7

HA. ORDER= 3

VA= .461  
ANG VA= 338.8  
VB= .4688  
ANG VB= 218.8  
VC= .4532  
ANG VC= 98.8

IA= .112005  
ANG IA= 342.6  
IB= .12327  
ANG IB= 222.6  
IC= .113755  
ANG IC= 102.6

HA. ORDER= 4

VA= .0922  
ANG VA= 81.8  
VB= .0844  
ANG VB= 321.8  
VC= .0795  
ANG VC= 201.8

IA= .00786  
ANG IA= 94.5  
IB= .006895  
ANG IB= 334.5  
IC= .00786  
ANG IC= 214.5

HA. ORDER= 5

VA= 16.8726  
ANG VA= 32.6  
VB= 16.7024  
ANG VB= 272.6  
VC= 18.2414  
ANG VC= 152.6

IA= 1.098435  
ANG IA= 40  
IB= 1.07289  
ANG IB= 280  
IC= 1.081625  
ANG IC= 160

HA. ORDER= 6

VA= .0922  
ANG VA= -2.2  
VB= .1044  
ANG VB= 237.8  
VC= .0811  
ANG VC= 117.8

IA= .00786  
ANG IA= 10.4  
IB= .00786  
ANG IB= 250.4  
IC= .005895  
ANG IC= 130.4

HA. ORDER= 7

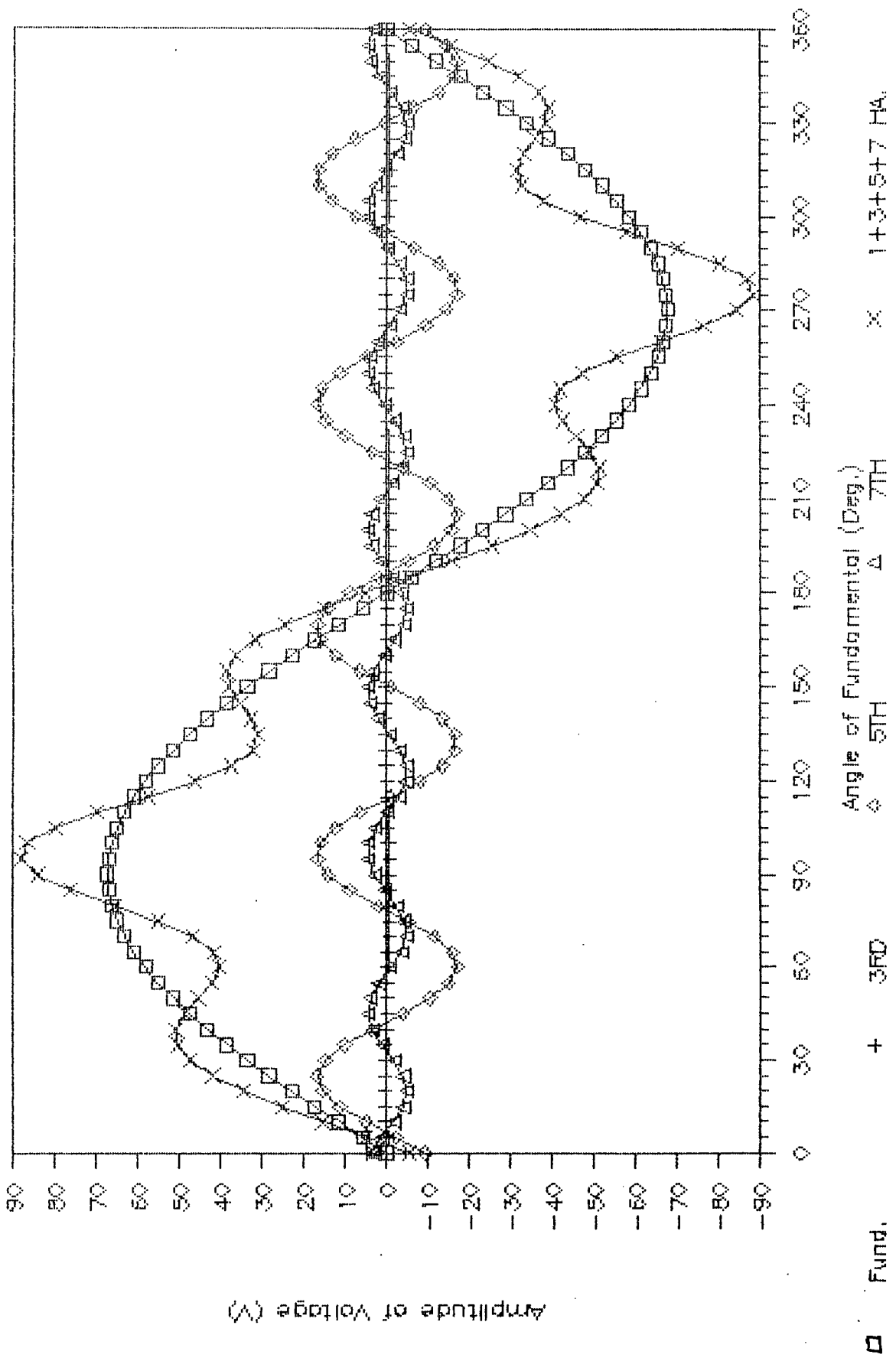
VA= 4.7022  
ANG VA= 229.5  
VB= 4.8866  
ANG VB= 109.5  
VC= 4.4256  
ANG VC= 349.5

IA= .249555  
ANG IA= 231.4  
IB= .26331  
ANG IB= 111.4  
IC= .245625  
ANG IC= 351.4

Amplitudes and phase angles of harmonic components.

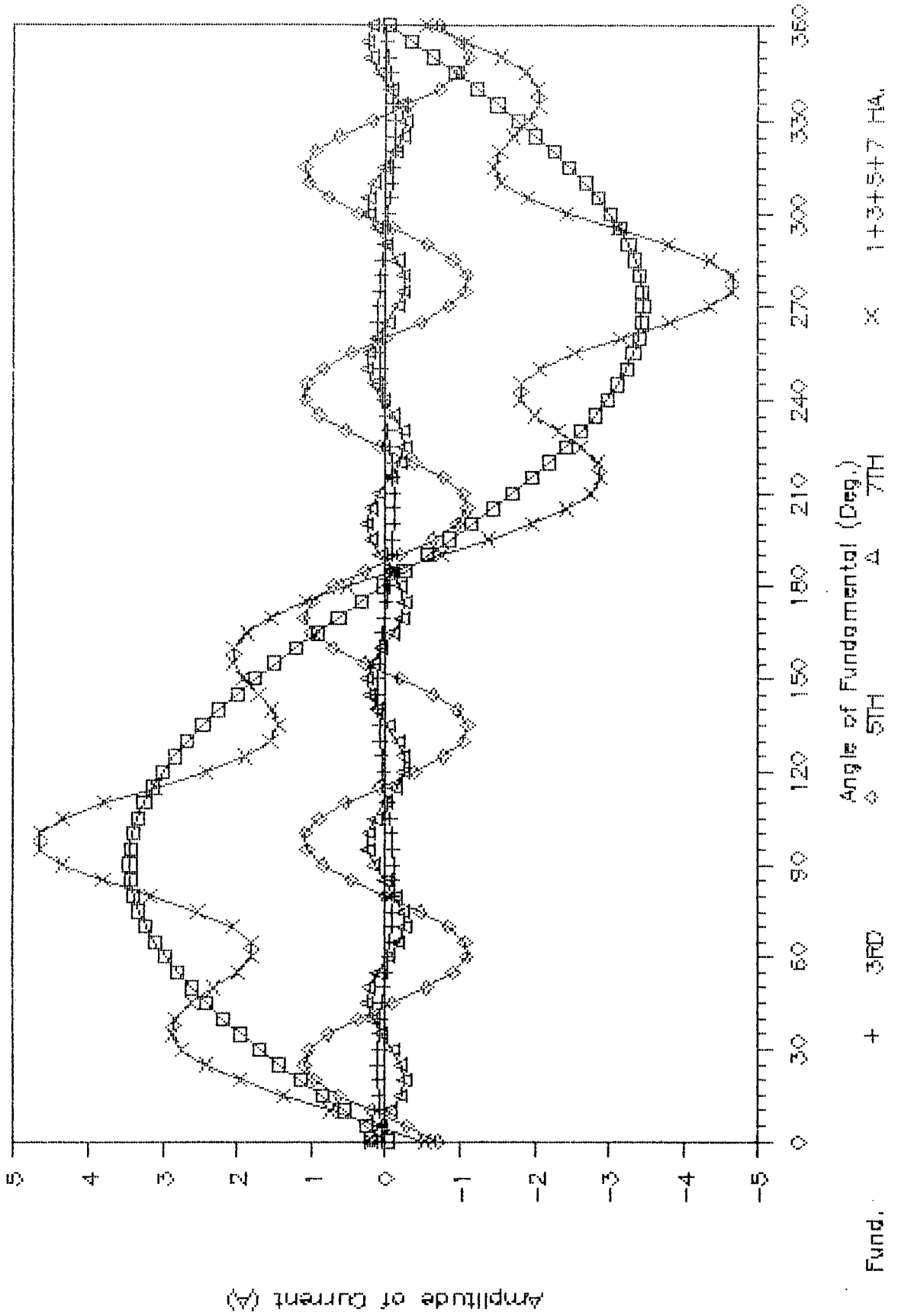
Reconstructed waveforms

TEST\_4



Reconstructed waveforms

TEST\_4



HA. ORDER= 1  
 V0= .57472508458  
 ANG V0= -75.4436671604  
 V+= 67.2011466667  
 ANG V+= 0  
 V-= .57472508458  
 ANG V-= 75.4436671604  
 I0= .048660227343  
 ANG I0= 123.941462927  
 I+= 3.509925  
 ANG I+= .5999999999994  
 I-= 4.86602273413E-2  
 ANG I-= -122.741462929

HA. ORDER= 2  
 V0= .0052  
 ANG V0= -152.199999997  
 V+= .374  
 ANG V+= 87.8  
 V-= 5.20000000017E-3  
 ANG V-= -32.2000000001  
 I0= 7.57809342777E-4  
 ANG I0= -155.836386237  
 I+= .00441  
 ANG I+= 95.7  
 I-= 7.57809342773E-4  
 ANG I-= -12.7636137631

HA. ORDER= 3  
 V0= 4.50333209933E-3  
 ANG V0= -111.199999999  
 V+= .461  
 ANG V+= -21.2  
 V-= 4.50333209977E-3  
 ANG V-= 68.7999999979  
 I0= 3.49998373027E-3  
 ANG I0= -145.69895992  
 I+= .116343333333  
 ANG I+= -17.4  
 I-= 3.49998373013E-3  
 ANG I-= 110.898959921

HA. ORDER= 4  
 V0= 3.69789730043E-3  
 ANG V0= 59.3103282475  
 V+= 8.53666666667E-2  
 ANG V+= 81.8  
 V-= 3.6978973004E-3  
 ANG V-= 104.289671752  
 I0= 3.21666666667E-4  
 ANG I0= 154.5  
 I+= 7.53833333333E-3  
 ANG I+= 94.5  
 I-= 3.21666666666E-4  
 ANG I-= 34.4999999999

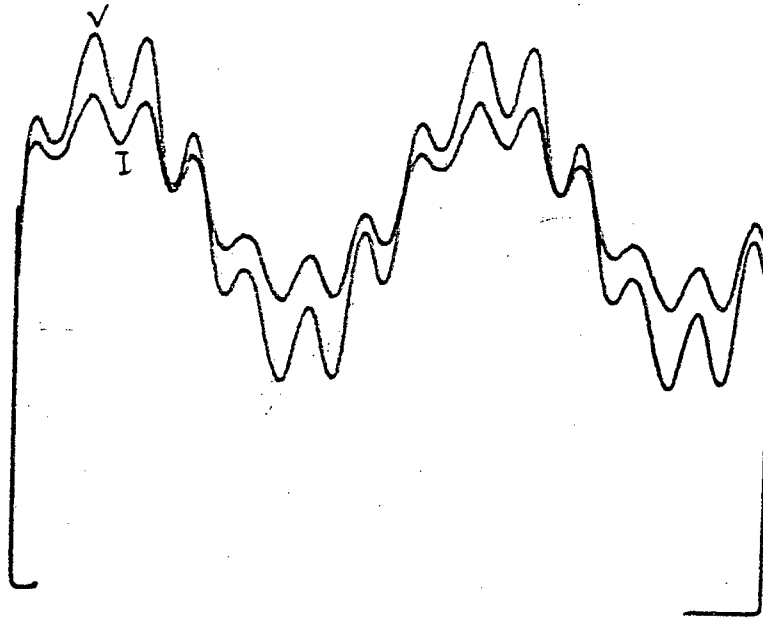
HA. ORDER= 5  
 V0= .48711751264  
 ANG V0= 146.81108775  
 V+= 17.2721333333  
 ANG V+= 32.6  
 V-= .487117512627  
 ANG V-= -81.6110877495  
 I0= 7.4960113458E-3  
 ANG I0= 59.6570369813  
 I+= 1.08431666667  
 ANG I+= 39.9999999999  
 I-= 7.49601134547E-3  
 ANG I-= 20.3429630469

HA. ORDER= 6  
 V0= 6.72862871953E-3  
 ANG V0= -93.7613175901  
 V+= 9.25666666667E-2  
 ANG V+= -2.2  
 V-= 6.72862871943E-3  
 ANG V-= 89.3613175902  
 I0= 6.54999999997E-4  
 ANG I0= -49.6000000002  
 I+= .007205  
 ANG I+= 10.4  
 I-= .000655  
 ANG I-= 70.4000000003

HA. ORDER= 7  
 V0= .133963494198  
 ANG V0= 146.086775553  
 V+= 4.67146666667  
 ANG V+= -130.5  
 V-= .133963494194  
 ANG V-= -47.0867755539  
 I0= 5.36140606547E-3  
 ANG I0= 123.61634884  
 I+= .25283  
 ANG I+= -128.6  
 I-= 5.3614060654E-3  
 ANG I-= -20.8163488426

Symmetrical components of harmonics.

T E S T 5



Resultant Waveform of Harmonics : 1st + 7th

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

|     |               |      |        |
|-----|---------------|------|--------|
| VA= | 68.4758053145 | 68.3 | + 0.26 |
| VB= | 66.2619574706 | 68.3 | - 3.08 |
| VC= | 69.0493238655 | 68.2 | + 1.23 |
| IA= | 3.86254413218 | 3.79 | + 1.81 |
| IB= | 3.88116442695 | 3.81 | + 1.80 |
| IC= | 3.89538410965 | 3.80 | + 2.30 |

FUND. FREQ. = 49.9 HZ

HA. ORDER= 1

VA= 65.923  
ANG VA= 0  
VB= 63.5116  
ANG VB= 240  
VC= 66.4266  
ANG VC= 120

IA= 3.680445  
ANG IA= 357.8  
IB= 3.680305  
ANG IB= 233.8  
IC= 3.696165  
ANG IC= 117.8

HA. ORDER= 2

VA= .0016  
ANG VA= -2.2  
VB= .0025  
ANG VB= 237.8  
VC= .0022  
ANG VC= 117.8

IA= .02716  
ANG IA= 12.2  
IB= .029125  
ANG IB= 252.2  
IC= .027335  
ANG IC= 132.2

HA. ORDER= 3

VA= 1.6596  
ANG VA= 195.6  
VB= 1.4114  
ANG VB= 75.6  
VC= 1.5674  
ANG VC= 315.6

IA= .09253  
ANG IA= 187.8  
IB= .09432  
ANG IB= 67.8  
IC= .103795  
ANG IC= 307.8

HA. ORDER= 4

VA= .1844  
ANG VA= 297.8  
VB= .1844  
ANG VB= 177.8  
VC= .1992  
ANG VC= 57.8

IA= .013755  
ANG IA= 320.8  
IB= .01965  
ANG IB= 200.8  
IC= .01358  
ANG IC= 80.8

HA. ORDER= 5

VA= .2331  
ANG VA= 267.8  
VB= .2662  
ANG VB= 147.8  
VC= .1948  
ANG VC= 27.8

IA= .03716  
ANG IA= 270  
IB= .03405  
ANG IB= 150  
IC= .0393  
ANG IC= 30

HA. ORDER= 6

VA= .1688  
ANG VA= 267.8  
VB= .1844  
ANG VB= 147.8  
VC= .1922  
ANG VC= 27.8

IA= .013755  
ANG IA= 257.8  
IB= .015895  
ANG IB= 137.8  
IC= .019125  
ANG IC= 17.8

HA. ORDER= 7

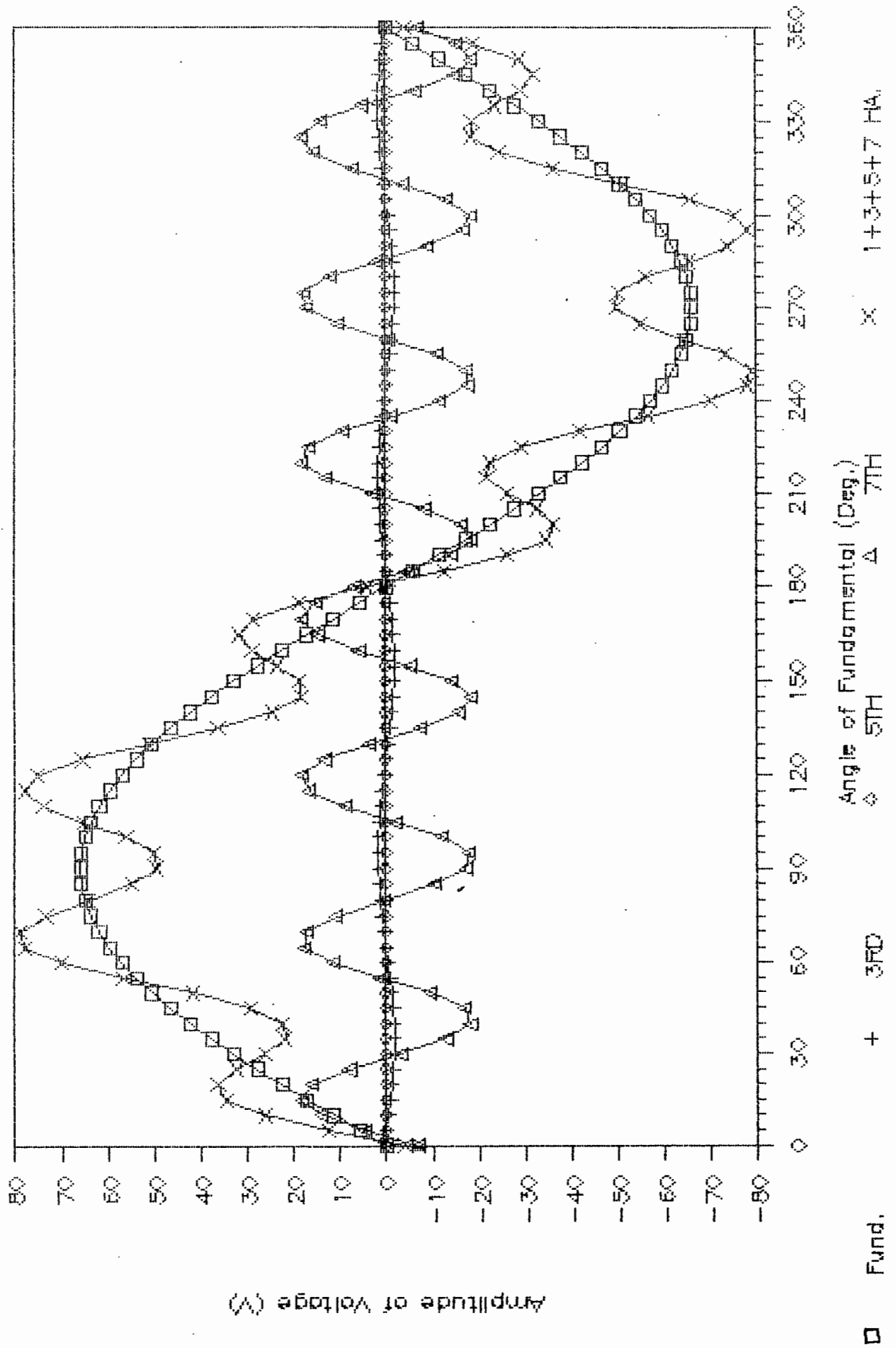
VA= 18.44  
ANG VA= 21.8  
VB= 18.0712  
ANG VB= 261.8  
VC= 18.0854  
ANG VC= 141.8

IA= 1.16721  
ANG IA= 18.1  
IB= 1.165245  
ANG IB= 258.1  
IC= 1.18686  
ANG IC= 138.1

Amplitudes and phase angles of harmonic components.

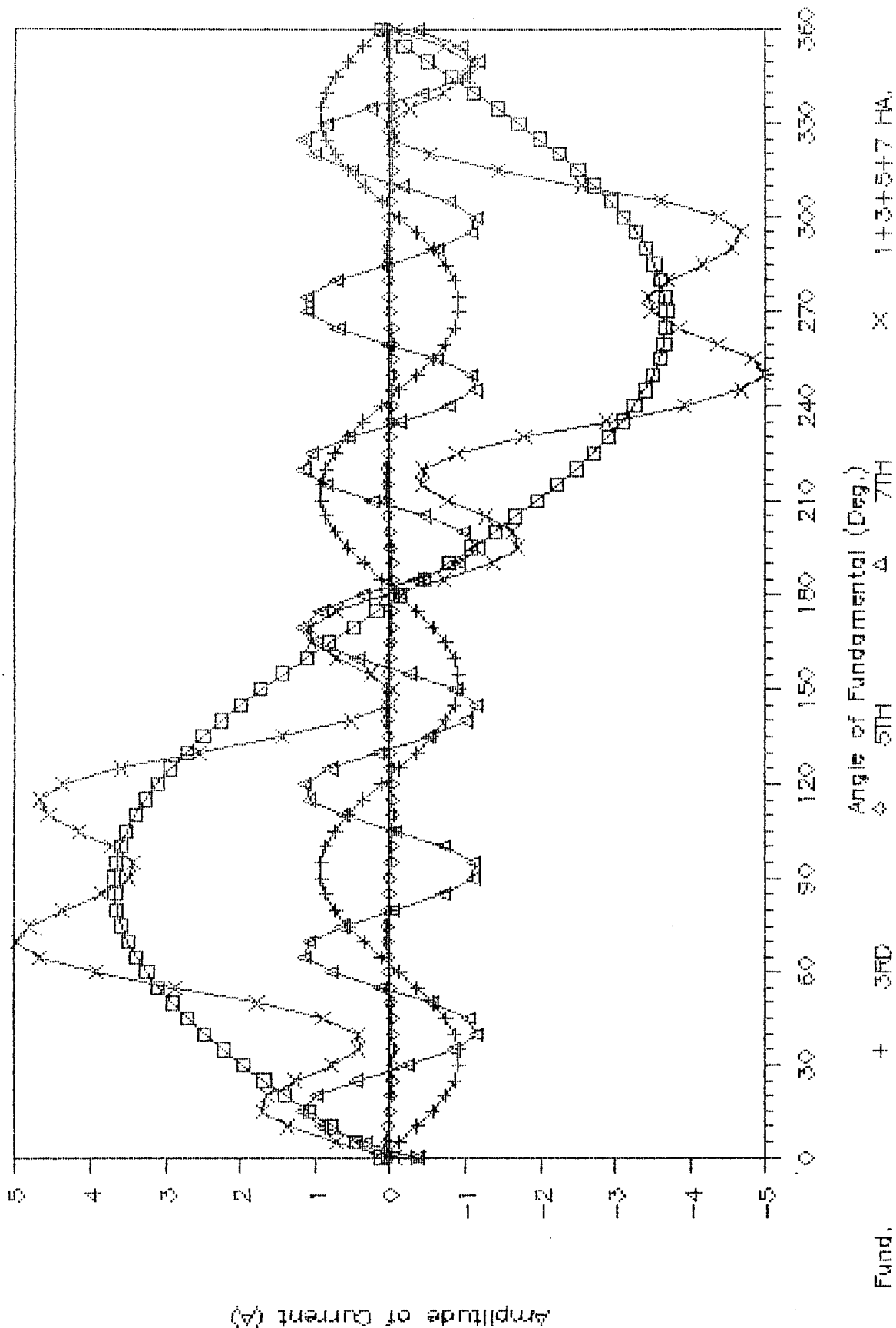
Reconstructed waveforms

TEST\_5



Reconstructed waveforms

TEST\_5



HA. ORDER= 1  
 V0= .89955816067  
 ANG V0= 69.3003073284  
 V+= 65.2870666667  
 ANG V+= 0  
 V-= .89955816067  
 ANG V-= -69.3003073284  
 I0= 9.03486729683E-2  
 ANG I0= 145.900434323  
 I+= 3.68630789807  
 ANG I+= -3.53309255017  
 I-= 8.12782710507E-2  
 ANG I-= 25.688357504

HA. ORDER= 2  
 V0= 2.64575131108E-4  
 ANG V0= -163.093394649  
 V+= .0021  
 ANG V+= -2.2  
 V-= 2.64575131108E-4  
 ANG V-= 158.693394649  
 I0= 6.27868970753E-4  
 ANG I0= -112.414989741  
 I+= 2.78733333333E-2  
 ANG I+= 12.2  
 I-= 6.2786897076E-4  
 ANG I-= 136.814989742

HA. ORDER= 3  
 V0= 7.24339085723E-2  
 ANG V0= -125.958444441  
 V+= 1.54613333333  
 ANG V+= -164.4  
 V-= 7.24339085747E-2  
 ANG V-= 157.15844444  
 I0= 3.49507550387E-3  
 ANG I0= -43.697953952  
 I+= 9.68816666667E-2  
 ANG I+= -172.2  
 I-= 3.4950755039E-3  
 ANG I-= 59.297953952

HA. ORDER= 4  
 V0= 4.9333333334E-3  
 ANG V0= 57.8000000011  
 V+= .189333333334  
 ANG V+= -62.2  
 V-= 4.9333333337E-3  
 ANG V-= 177.800000001  
 I0= 4.9699527674E-3  
 ANG I0= -67.3773691619  
 I+= 1.32069436776E-2  
 ANG I+= -58.3036964963  
 I-= 7.3568006987E-3  
 ANG I-= 75.7695297575

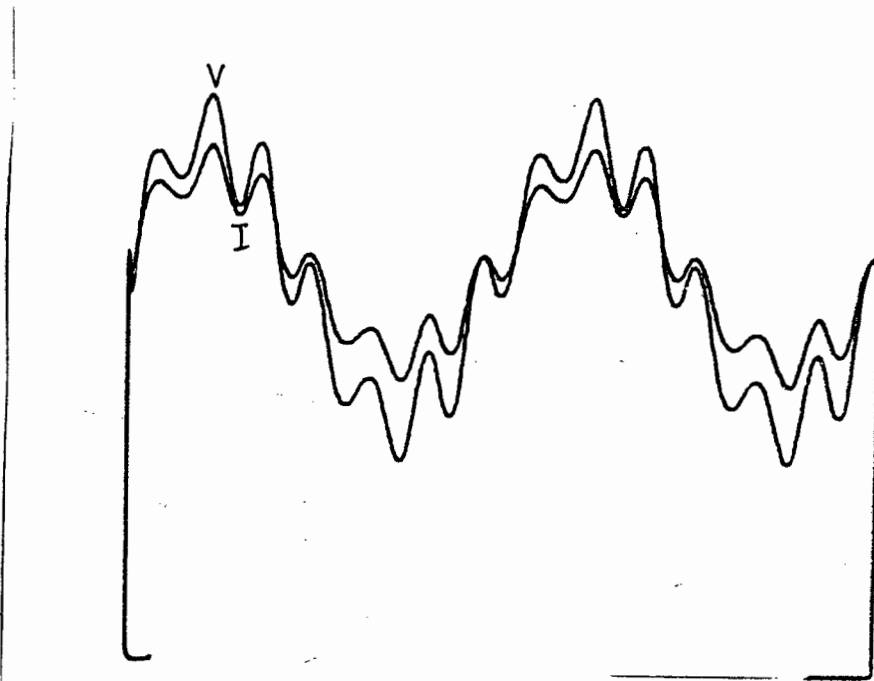
HA. ORDER= 5  
 V0= 2.06296173281E-2  
 ANG V0= -179.792250039  
 V+= .231366666667  
 ANG V+= -92.2  
 V-= 2.06296173281E-2  
 ANG V-= -4.60774996041  
 I0= 1.52414274631E-3  
 ANG I0= -6.08884929744  
 I+= 3.68366666667E-2  
 ANG I+= -90  
 I-= 1.52414274631E-3  
 ANG I-= -173.911150703

HA. ORDER= 6  
 V0= 6.87895340877E-3  
 ANG V0= 68.6933946504  
 V+= .1818  
 ANG V+= -92.2  
 V-= 6.87895340887E-3  
 ANG V-= 106.906605351  
 I0= 1.56079395751E-3  
 ANG I0= 41.1159788746  
 I+= 1.62583333333E-2  
 ANG I+= -102.2  
 I-= 1.56079395751E-3  
 ANG I-= 114.484021125

HA. ORDER= 7  
 V0= .120636331362  
 ANG V0= 23.7472685036  
 V+= 18.1988666667  
 ANG V+= 21.8  
 V-= .120636331371  
 ANG V-= 19.8527314714  
 I0= 6.90085320787E-3  
 ANG I0= 133.384996063  
 I+= 1.173105  
 ANG I+= 18.1000000001  
 I-= 6.90085320867E-3  
 ANG I-= -97.1849960547

Symmetrical components of harmonics.

T E S T 6



Resultant Waveform of Harmonics : 1st + 7th

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

|     |               |      |        |
|-----|---------------|------|--------|
| VA= | 67.9139168173 | 67.5 | + 0.60 |
| VB= | 68.3451306581 | 67.6 | + 1.11 |
| VC= | 70.3145667161 | 67.5 | + 4.00 |
| IA= | 4.07056726523 | 3.86 | + 5.16 |
| IB= | 3.90141061957 | 3.88 | + 0.51 |
| IC= | 4.06407707808 | 3.87 | + 4.77 |

FUND. FREQ. = 50.1 HZ

HA. ORDER= 1

VA= 65.7102  
ANG VA= 0  
VB= 66.1144  
ANG VB= 240  
VC= 68.0436  
ANG VC= 120

IA= 3.90292  
ANG IA= 3.8  
IB= 3.723675  
ANG IB= 243.8  
IC= 3.896595  
ANG IC= 123.8

HA. ORDER= 2

VA= .2766  
ANG VA= 87.8  
VB= .261  
ANG VB= 327.8  
VC= .2922  
ANG VC= 207.8

IA= .02751  
ANG IA= 95.6  
IB= .02358  
ANG IB= 335.6  
IC= .02786  
ANG IC= 215.6

HA. ORDER= 3

VA= 3.3972  
ANG VA= 80.1  
VB= 3.5816  
ANG VB= 320.1  
VC= 3.4894  
ANG VC= 200.1

IA= .09422  
ANG IA= 76.3  
IB= .09482  
ANG IB= 316.3  
IC= .084495  
ANG IC= 196.3

HA. ORDER= 4

VA= .4688  
ANG VA= 237.7  
VB= .5376  
ANG VB= 117.7  
VC= .4454  
ANG VC= 357.7

IA= .020545  
ANG IA= 263.2  
IB= .025545  
ANG IB= 143.2  
IC= .02393  
ANG IC= 23.2

HA. ORDER= 5

VA= 1.2  
ANG VA= 269.6  
VB= 1.1986  
ANG VB= 149.6  
VC= 1.2376  
ANG VC= 29.6

IA= .019475  
ANG IA= 254.2  
IB= .019825  
ANG IB= 134.2  
IC= .01786  
ANG IC= 14.2

HA. ORDER= 6

VA= .0922  
ANG VA= 177.8  
VB= .0832  
ANG VB= 57.8  
VC= .0844  
ANG VC= 297.8

IA= .005895  
ANG IA= 188.4  
IB= .00537  
ANG IB= 68.4  
IC= .00786  
ANG IC= 308.4

HA. ORDER= 7

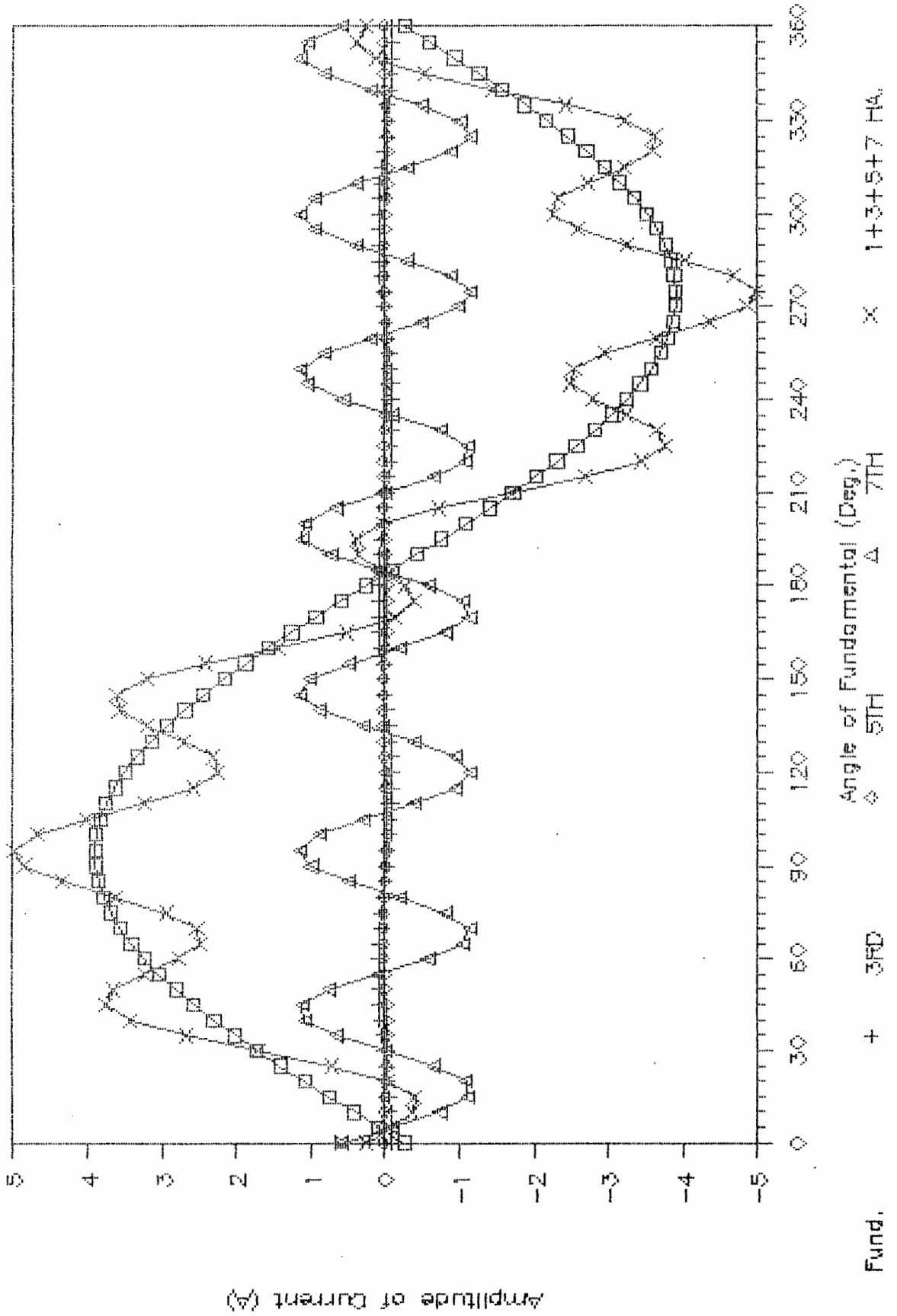
VA= 16.7662  
ANG VA= 200.2  
VB= 16.596  
ANG VB= 80.2  
VC= 16.9648  
ANG VC= 320.2

IA= 1.15149  
ANG IA= 210.4  
IB= 1.14756  
ANG IB= 90.4  
IC= 1.133805  
ANG IC= 330.4

Amplitudes and phase angles of harmonic components.

Reconstructed waveforms

TEST\_6



HA. ORDER= 4

HA. ORDER= 1  
V0= .719951612577  
ANG V0= 129.327061372  
V+= 66.6227333333  
ANG V+= 0  
V-= .719951612577  
ANG V-= -129.327061372

V0= 2.76705218198E-2  
ANG V0= 131.829984681  
V+= .483933333333  
ANG V+= -122.3  
V-= 2.76705218195E-2  
ANG V-= -16.4299846807

I0= 5.87225595713E-2  
ANG I0= 62.0182057005  
I+= 3.84106333333  
ANG I+= 3.8  
I-= 5.87225595737E-2  
ANG I-= -54.4182057011

I0= 1.4732136075E-3  
ANG I0= 101.648858913  
I+= .02334  
ANG I+= -96.8  
I-= 1.47321360749E-3  
ANG I-= 64.7511410874

HA. ORDER= 5

HA. ORDER= 2  
V0= 9.00666419937E-3  
ANG V0= 177.800000001  
V+= .2766  
ANG V+= 87.8  
V-= 9.0066641997E-3  
ANG V-= -2.2000000118

V0= 1.27730619321E-2  
ANG V0= 27.7868341984  
V+= 1.21206666667  
ANG V+= -90.4  
V-= .012773061933  
ANG V-= 151.413165802

I0= 1.37205846977E-3  
ANG I0= 159.822996488  
I+= 2.63166666667E-2  
ANG I+= 95.6  
I-= 1.37205846977E-3  
ANG I-= 31.3770035133

I0= 6.05160676557E-4  
ANG I0= -175.410986162  
I+= 1.90533333333E-2  
ANG I+= -105.8  
I-= 6.0516067658E-4  
ANG I-= -36.189013841

HA. ORDER= 6

HA. ORDER= 3  
V0= 5.32316948213E-2  
ANG V0= -69.9000000015  
V+= 3.4894  
ANG V+= 80.100000001  
V-= 5.32316948213E-2  
ANG V-= -129.899999999

V0= 2.82134719594E-3  
ANG V0= -175.147322973  
V+= 8.660000000003E-2  
ANG V+= 177.8  
V-= 2.82134719593E-3  
ANG V-= 170.747322972

I0= 3.34615243397E-3  
ANG I0= 13.3329035276  
I+= .091178333333  
ANG I+= 76.3  
I-= 3.3461524339E-3  
ANG I-= 139.267096472

I0= 7.57809342777E-4  
ANG I0= -63.1363862369  
I+= .006375  
ANG I+= -171.6  
I-= 7.57809342777E-4  
ANG I-= 79.9363862373

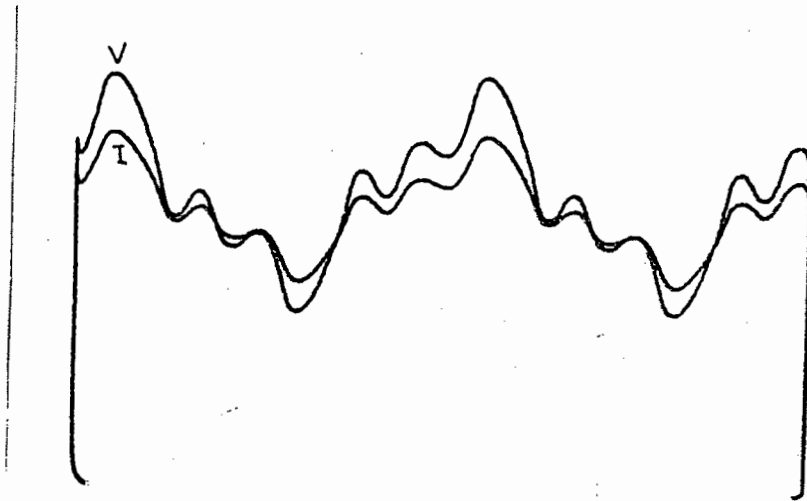
HA. ORDER= 7

V0= .106568559077  
ANG V0= -67.2543216625  
V+= 16.7756666667  
ANG V+= -159.8  
V-= .106568559017  
ANG V-= 107.65432167

I0= 5.36140606463E-3  
ANG I0= 162.616348844  
I+= 1.144285  
ANG I+= -149.6  
I-= 5.36140606773E-3  
ANG I-= -101.816348833

Symmetrical components of harmonics.

T E S T 7



Resultant Waveform of Harmonics : 1st + 3rd + 5th + 7th

Resultant RMS Values  
of 3 phase components

Analogue Meters readings  
of 3 phase power supply

DEVIATION  
( % )

|     |               |      |       |
|-----|---------------|------|-------|
| VA= | 44.3830492041 | 45.1 | -1.62 |
| VB= | 44.3373683613 | 45.1 | -1.71 |
| VC= | 44.9042010583 | 45.2 | -0.67 |
| IA= | 2.67576605228 | 2.70 | -0.75 |
| IB= | 2.64710039713 | 2.72 | -2.64 |
| IC= | 2.65348301378 | 2.73 | -2.90 |

HA. ORDER= 4

VA= .09126  
ANG VA= -5.6  
VB= .07652  
ANG VB= 244.4  
VC= .09864  
ANG VC= 124.4

IA= .01872  
ANG IA= -1.3  
IB= .01537  
ANG IB= 238.7  
IC= .01924  
ANG IC= 118.7

HA. ORDER= 5

VA= 13.1262  
ANG VA= 124.9  
VB= 12.80188  
ANG VB= 4.9  
VC= 12.5637  
ANG VC= 244.9

IA= .836127  
ANG IA= 127.5  
IB= .870212  
ANG IB= 7.5  
IC= .85429  
ANG IC= 247.5

HA. ORDER= 6

VA= .2041  
ANG VA= 281.2  
VB= .2171  
ANG VB= 161.2  
VC= .1976  
ANG VC= 41.2

IA= .018054  
ANG IA= 272.5  
IB= .021106  
ANG IB= 152.5  
IC= .017452  
ANG IC= 32.5

HA. ORDER= 7

VA= 10.7013  
ANG VA= 199.2  
VB= 11.1017  
ANG VB= 79.2  
VC= 11.5102  
ANG VC= 319.2

IA= .6945  
ANG IA= 201.1  
IB= .6758  
ANG IB= 81.1  
IC= .7012  
ANG IC= 321.1

FUND. FREQ. = 50.1 HZ

HA. ORDER= 1

VA= 38.695  
ANG VA= 0  
VB= 38.452  
ANG VB= 240  
VC= 39.132  
ANG VC= 120

IA= 2.240235  
ANG IA= 3.1  
IB= 2.19678  
ANG IB= 243.1  
IC= 2.20874  
ANG IC= 123.1

HA. ORDER= 2

VA= .1742  
ANG VA= 289.5  
VB= .1764  
ANG VB= 169.5  
VC= .1821  
ANG VC= 49.5

IA= .044126  
ANG IA= 296.3  
IB= .042216  
ANG IB= 176.3  
IC= .040112  
ANG IC= 56.3

HA. ORDER= 3

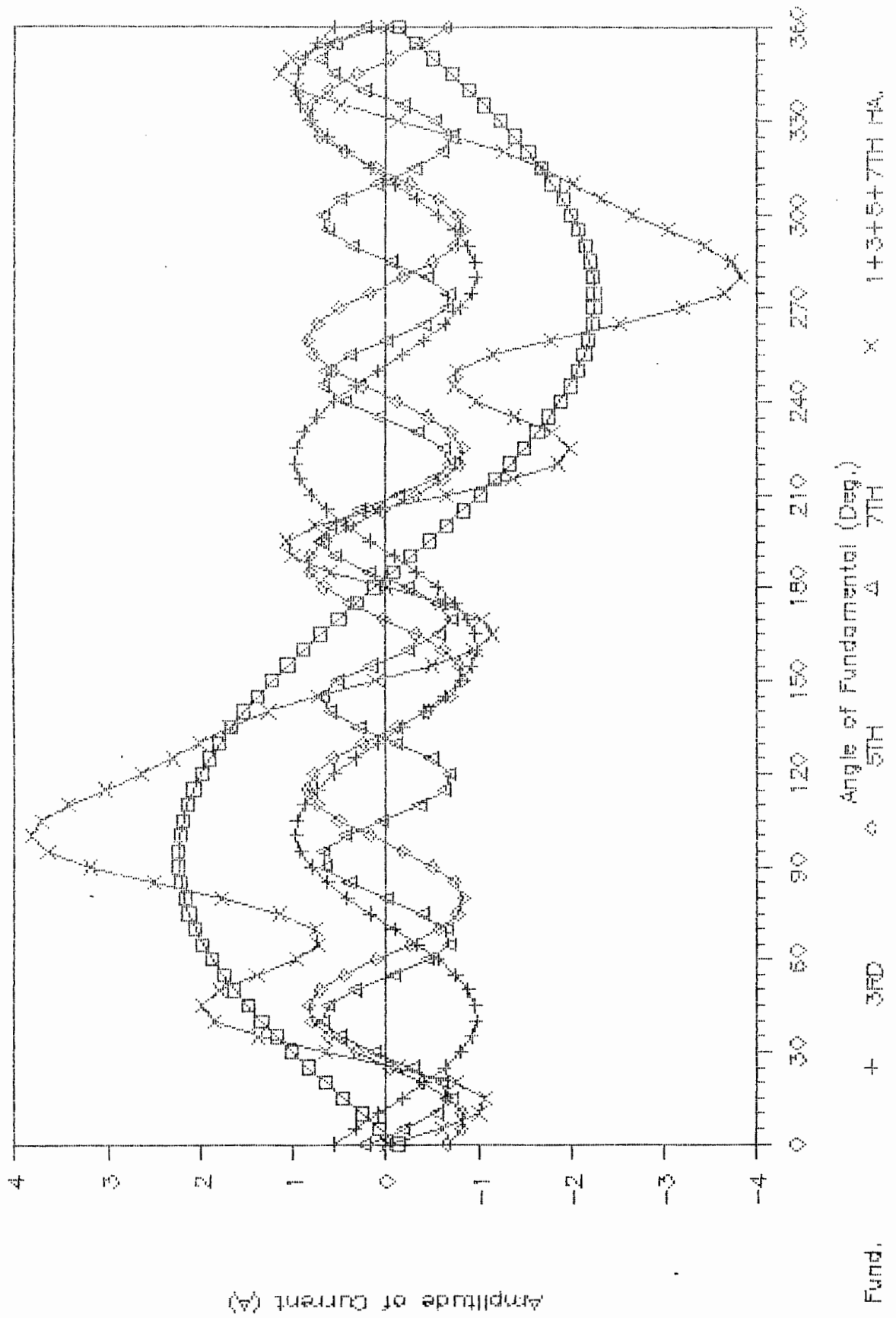
VA= 13.6245  
ANG VA= 222.4  
VB= 14.1321  
ANG VB= 102.4  
VC= 13.9279  
ANG VC= 342.4

IA= .97825  
ANG IA= 214.7  
IB= .98216  
ANG IB= 94.7  
IC= .96862  
ANG IC= 334.7

Amplitudes and phase angles of harmonic components.

Reconstructed waveforms

TEST 7



HA. ORDER= 1  
 V0= .198944157444  
 ANG V0= 99.3534675283  
 V+= 38.7596666667  
 ANG V+= 0  
 V-= .198944157444  
 ANG V-= -99.3534675283  
 I0= 1.29591733926E-2  
 ANG I0= 18.564458455  
 I+= 2.215255  
 ANG I+= 3.1  
 I-= 1.29591733912E-2  
 ANG I-= -12.3644584646

HA. ORDER= 2  
 V0= 2.35395648062E-3  
 ANG V0= 65.1520586001  
 V+= .177566666667  
 ANG V+= -70.4999999999  
 V-= 2.35395648022E-3  
 ANG V-= 153.847941392  
 I0= 1.15919301432E-3  
 ANG I0= -95.298356633  
 I+= 4.2151333333E-2  
 ANG I+= -53.7000000001  
 I-= 1.15919301432E-3  
 ANG I-= -32.1016433684

HA. ORDER= 3  
 V0= .147442693172  
 ANG V0= 66.0268292783  
 V+= 13.8946666667  
 ANG V+= -137.6  
 V-= .147442693183  
 ANG V-= 18.773170739  
 I0= 4.02324219727E-3  
 ANG I0= 138.406979038  
 I+= .976343333333  
 ANG I+= -145.3  
 I-= 4.02324219693E-3  
 ANG I-= -69.0069790391

HA. ORDER= 4  
 V0= 1.34214543809E-3  
 ANG V0= 59.6759761878  
 V+= 8.85023020273E-2  
 ANG V+= .978191492941  
 V-= 1.16928916388E-2  
 ANG V-= -81.8511450922  
 I0= 1.21266006963E-3  
 ANG I0= 65.8106890118  
 I+= 1.77766666667E-2  
 ANG I+= -1.3  
 I-= 1.21266006962E-3  
 ANG I-= -68.4106890117

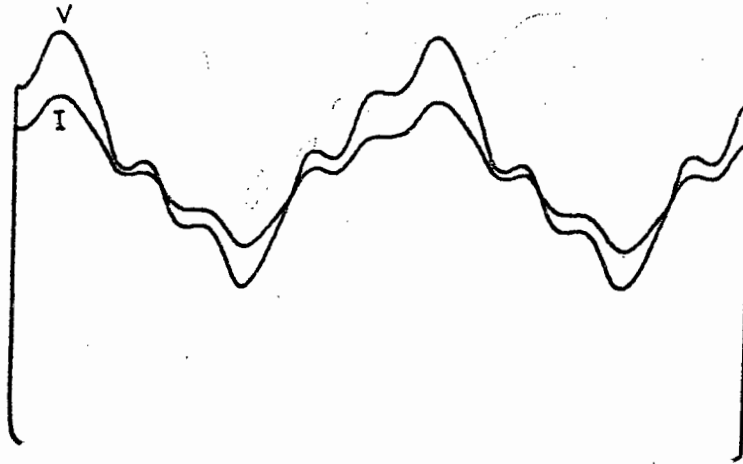
HA. ORDER= 5  
 V0= .163013193899  
 ANG V0= 99.952618703  
 V+= 12.8305933333  
 ANG V+= 124.9  
 V-= .163013193868  
 ANG V-= 149.847381296  
 I0= .009846578306  
 ANG I0= -24.6738626511  
 I+= .853543  
 ANG I+= 127.5  
 I-= 9.84657830573E-3  
 ANG I-= -80.3261373501

HA. ORDER= 6  
 V0= 5.73246117387E-3  
 ANG V0= -179.693394652  
 V+= .206266666667  
 ANG V+= -78.8  
 V-= 5.73246117387E-3  
 ANG V-= 22.0933946498  
 I0= 1.13109641992E-3  
 ANG I0= 161.337969067  
 I+= 1.88706666666E-2  
 ANG I+= -87.5  
 I-= 1.13109641991E-3  
 ANG I-= 23.6620309336

HA. ORDER= 7  
 V0= .233513218767  
 ANG V0= -11.1312434901  
 V+= 11.1044  
 ANG V+= -160.8  
 V-= .233513218742  
 ANG V-= 49.5312434828  
 I0= 7.6002192947E-3  
 ANG I0= -84.1570723442  
 I+= .6905  
 ANG I+= -158.9  
 I-= 7.60021929513E-3  
 ANG I-= 126.357072343

Symmetrical components of harmonics.

T E S T 8



Resultant Waveform of Harmonics : 1st + 3rd + 5th + 7th

| Resultant RMS Values<br>of 3 phase components | Analogue Meters readings<br>of 3 phase power supply | DEVIATION<br>( % ) |
|-----------------------------------------------|-----------------------------------------------------|--------------------|
| VA= 57.7644336395                             | 55.2                                                | +4.45              |
| VB= 54.7388799311                             | 55.3                                                | -1.02              |
| VC= 56.9422137505                             | 55.4                                                | +2.70              |
| IA= 3.16394054622                             | 3.00                                                | +5.18              |
| IB= 3.26697949845                             | 3.05                                                | +6.64              |
| IC= 3.17080819827                             | 2.95                                                | +6.97              |

FUND. FREQ. = 49.9 HZ

HA. ORDER= 1

VA= 55.712  
ANG VA= 0  
VB= 52.4588  
ANG VB= 240  
VC= 54.8245  
ANG VC= 120

IA= 3.00124  
ANG IA= 1.1  
IB= 3.10876  
ANG IB= 241.1  
IC= 3.00674  
ANG IC= 121.1

HA. ORDER= 2

VA= .08342  
ANG VA= 113.1  
VB= .08267  
ANG VB= 353.1  
VC= .08198  
ANG VC= 233.1

IA= .01988  
ANG IA= 120.3  
IB= .02076  
ANG IB= 3  
IC= .02104  
ANG IC= 240.3

HA. ORDER= 3

VA= 10.2138  
ANG VA= 216.9  
VB= 10.3426  
ANG VB= 96.9  
VC= 10.0987  
ANG VC= 336.9

IA= .691035  
ANG IA= 220.1  
IB= .686752  
ANG IB= 100.1  
IC= .693421  
ANG IC= 340.1

HA. ORDER= 4

VA= .1085  
ANG VA= 307.2  
VB= .0982  
ANG VB= 187.2  
VC= .1124  
ANG VC= 67.2

IA= .01685  
ANG IA= 322.7  
IB= .01724  
ANG IB= 202.7  
IC= .01421  
ANG IC= 82.7

HA. ORDER= 5

VA= 8.6517  
ANG VA= 147.1  
VB= 8.8431  
ANG VB= 27.1  
VC= 8.5462  
ANG VC= 267.1

IA= .59223  
ANG IA= 140.5  
IB= .57374  
ANG IB= 20.5  
IC= .58247  
ANG IC= 260.5

HA. ORDER= 6

VA= .0847  
ANG VA= 291.6  
VB= .0768  
ANG VB= 171.6  
VC= .0882  
ANG VC= 51.6

IA= .02434  
ANG IA= 280.1  
IB= .02248  
ANG IB= 160.1  
IC= .027625  
ANG IC= 40.1

HA. ORDER= 7

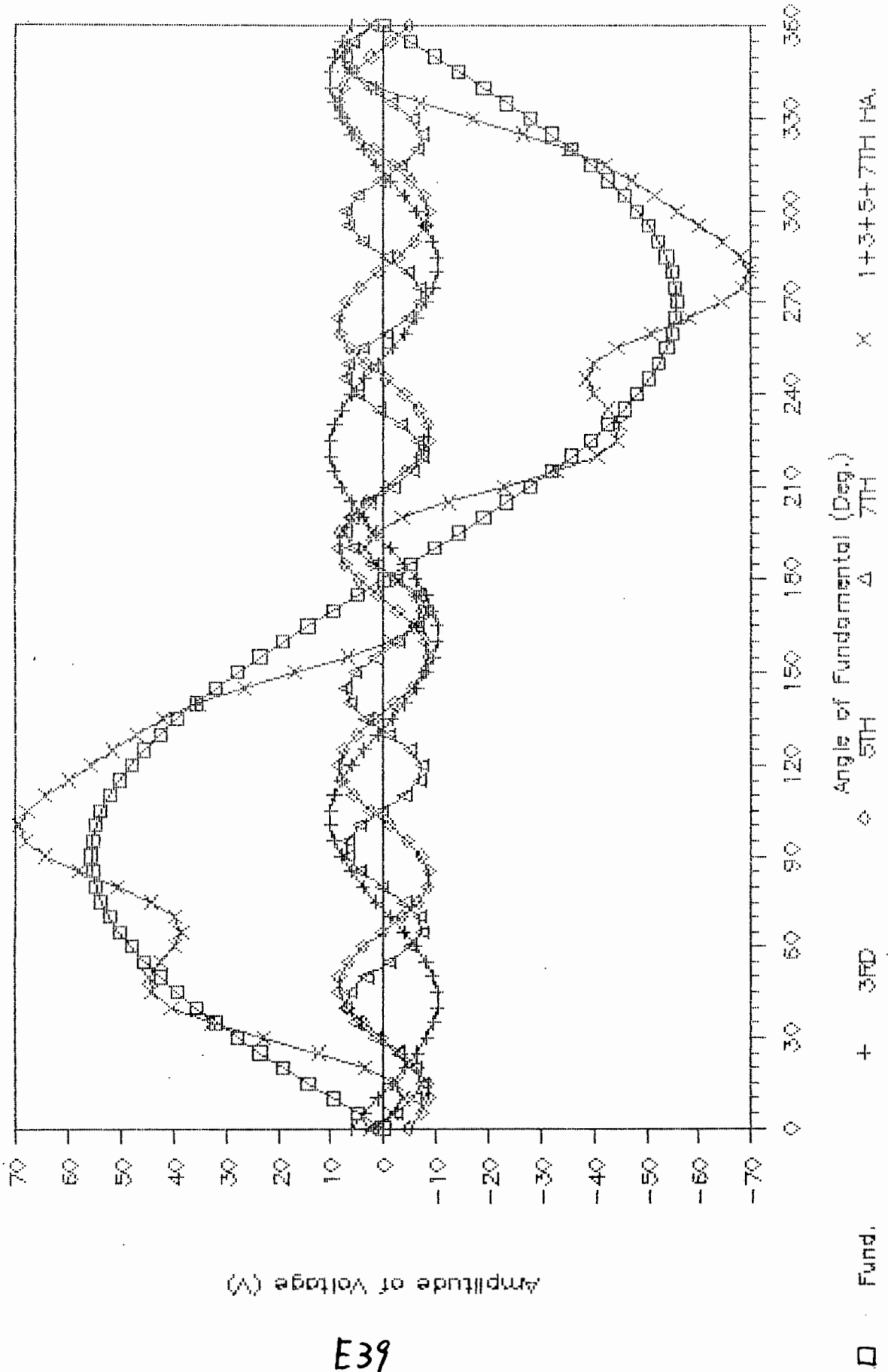
VA= 7.3231  
ANG VA= 197.2  
VB= 7.4879  
ANG VB= 77.2  
VC= 7.5266  
ANG VC= 317.2

IA= .416367  
ANG IA= 201.4  
IB= .44243  
ANG IB= 81.4  
IC= .42344  
ANG IC= 321.4

Amplitudes and phase angles of harmonic components.

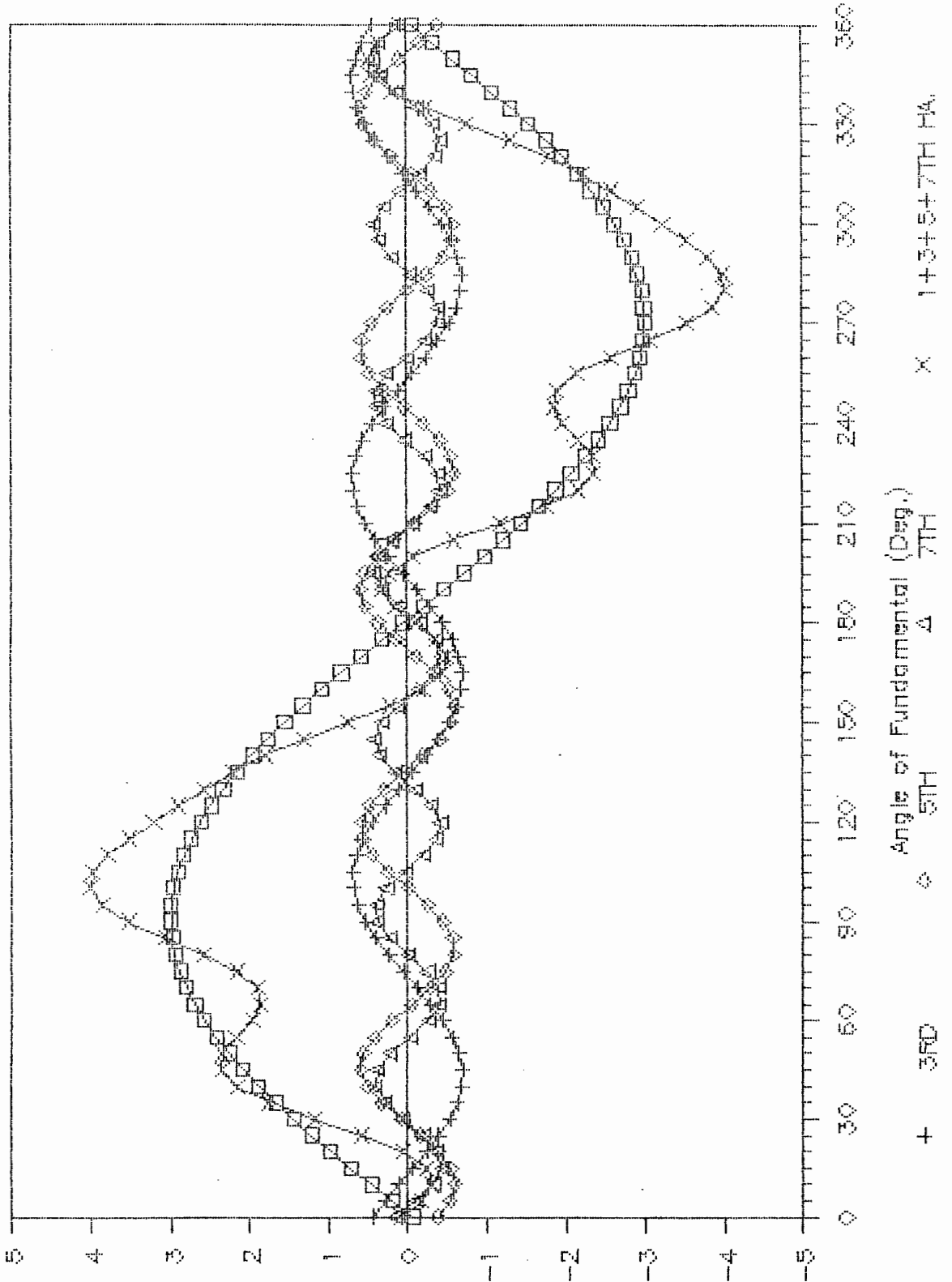
Reconstructed waveforms

TEST 8



Reconstructed waveforms

TEST\_8



```

HA. ORDER= 1
V0= .970896006003
ANG V0= 44.699639539
V+= 54.3317666667
ANG V+= 0
V-= .970896006003
ANG V-= -44.699639539

I0= 3.49594056663E-2
ANG I0= -121.50303536
I+= 3.03891333334
ANG I+= 1.1
I-= .034959405666
ANG I-= 123.70303536

```

```

HA. ORDER= 4
V0= 4.23569487943E-3
ANG V0= 22.6142884408
V+= .106366666667
ANG V+= -52.8
V-= 4.23569487943E-3
ANG V-= -128.21428844

I0= 9.51682720257E-4
ANG I0= -104.093954611
I+= .0161
ANG I+= -37.3000000001
I-= 9.51682720237E-4
ANG I-= 29.4939546121

```

```

HA. ORDER= 2
V0= 4.1581245771E-4
ANG V0= 84.4780564516
V+= .08269
ANG V+= 113.1
V-= 4.1581245776E-4
ANG V-= 141.721943552

I0= 3.4947579793E-4
ANG I0= -73.0728258083
I+= .02056
ANG I+= 120.3
I-= 3.4947579793E-4
ANG I-= -46.3271741846

```

```

HA. ORDER= 5
V0= 8.68951539393E-2
ANG V0= 47.616826923
V+= 8.68033333337
ANG V+= 147.1
V-= 8.68951539337E-2
ANG V-= -113.416826923

I0= 5.3403630758E-3
ANG I0= 168.657902368
I+= .582813333333
ANG I+= 140.5
I-= 5.34036307553E-3
ANG I-= 112.342097636

```

```

HA. ORDER= 3
V0= 7.04448799357E-2
ANG V0= 125.042543765
V+= 10.2183666667
ANG V+= -143.1
V-= 7.04448799573E-2
ANG V-= -51.2425437651

I0= 1.95096338009E-3
ANG I0= -59.2262940338
I+= .69040266667
ANG I+= -139.9
I-= 1.95096338015E-3
ANG I-= 139.426294035

```

```

HA. ORDER= 6
V0= 3.37161352733E-3
ANG V0= 9.03763304827
V+= 8.32333333333E-2
ANG V+= -68.4
V-= 3.37161352733E-3
ANG V-= -145.837633047

I0= 1.50410272256E-3
ANG I0= 19.185109776
I+= .024815
ANG I+= -79.9
I-= 1.50410272257E-3
ANG I-= -178.985109776

```

```

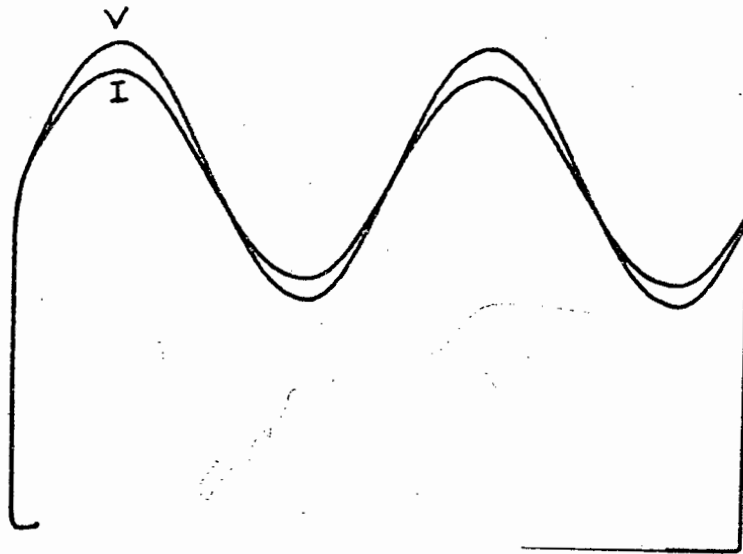
HA. ORDER= 7
V0= .062391675013
ANG V0= 6.885104994
V+= 7.44586666667
ANG V+= -162.8
V-= .062391675013
ANG V-= 27.5148950065

I0= 7.78148585543E-3
ANG I0= 66.1879606987
I+= .427412333333
ANG I+= -158.6
I-= 7.78148585487E-3
ANG I-= -23.3879606963

```

Symmetrical components of harmonics.

T E S T 9



Waveform of Fundamental

|       | RMS Values of 3<br>phase components | Analogue Meters Readings<br>of 3 phase power supply | DEVIATION<br>( % ) |
|-------|-------------------------------------|-----------------------------------------------------|--------------------|
| [ A ] |                                     |                                                     |                    |
| Va=   | 60.4282                             | 59.9                                                | +0.87              |
| Vb=   | 61.766                              | 61.5                                                | +0.43              |
| Vc=   | 62.4724                             | 61.5                                                | +1.56              |
| Ia=   | 4.680723                            | 4.70                                                | -0.41              |
| Ib=   | 3.643274                            | 3.60                                                | +1.19              |
| Ic=   | 3.574456                            | 3.61                                                | -1.0               |
| [ B ] |                                     |                                                     |                    |
| Va=   | 61.6544                             | 61.8                                                | -0.24              |
| Vb=   | 60.483                              | 61.0                                                | -0.85              |
| Vc=   | 62.3241                             | 61.7                                                | +1.0               |
| Ia=   | 3.54338                             | 3.56                                                | -0.47              |
| Ib=   | 4.728361                            | 4.74                                                | -0.47              |
| Ic=   | 3.4848                              | 3.55                                                | -1.87              |
| [ C ] |                                     |                                                     |                    |
| Va=   | 61.5734                             | 61.9                                                | -0.53              |
| Vb=   | 62.3348                             | 61.8                                                | +0.86              |
| Vc=   | 59.0723                             | 60.2                                                | -1.91              |
| Ia=   | 3.6762                              | 3.58                                                | +2.62              |
| Ib=   | 3.5437                              | 3.58                                                | -1.02              |
| Ic=   | 4.773264                            | 4.75                                                | +0.49              |

(A)

FUND. FREQ. = 50.1 HZ

HA. ORDER= 1

VA= 60.4282  
 ANG VA= 0  
 VB= 61.766  
 ANG VB= 240  
 VC= 62.4724  
 ANG VC= 120  
  
 IA= 4.680723  
 ANG IA= 3.8  
 IB= 3.643274  
 ANG IB= 243.8  
 IC= 3.574456  
 ANG IC= 123.8

HA. ORDER= 1

V0= .599482013453  
 ANG V0= 160.113345716  
 V+= 61.5554666667  
 ANG V+= 0  
 V-= .599482013453  
 ANG V-= -160.113345716  
  
 I0= .357836749417  
 ANG I0= .617840670755  
 I+= 3.96615  
 ANG I+= 3.8  
 I-= .357836749417  
 ANG I-= 6.98215932943

(B)

FUND. FREQ. = 49.9 HZ

HA. ORDER= 1

VA= 61.6544  
 ANG VA= 0  
 VB= 60.483  
 ANG VB= 240  
 VC= 62.3241  
 ANG VC= 120  
  
 IA= 3.54338  
 ANG IA= 5.4  
 IB= 4.728361  
 ANG IB= 245.4  
 IC= 3.4848  
 ANG IC= 125.4

HA. ORDER= 1

V0= .5379965004  
 ANG V0= 81.0730836803  
 V+= 61.4870333333  
 ANG V+= 0  
 V-= .5379965004  
 ANG V-= -81.0730836803  
  
 I0= .42351108377  
 ANG I0= -112.311599324  
 I+= 3.93726333333  
 ANG I+= 5.39999999998  
 I-= .423511083773  
 ANG I-= 123.111599324

(C)

FUND. FREQ. = 49.9 HZ

HA. ORDER= 1

VA= 61.5734  
 ANG VA= 0  
 VB= 62.3348  
 ANG VB= 240  
 VC= 59.0723  
 ANG VC= 120  
  
 IA= 3.6762  
 ANG IA= 8.3  
 IB= 3.5437  
 ANG IB= 248.3  
 IC= 4.773264  
 ANG IC= 128.3

HA. ORDER= 1

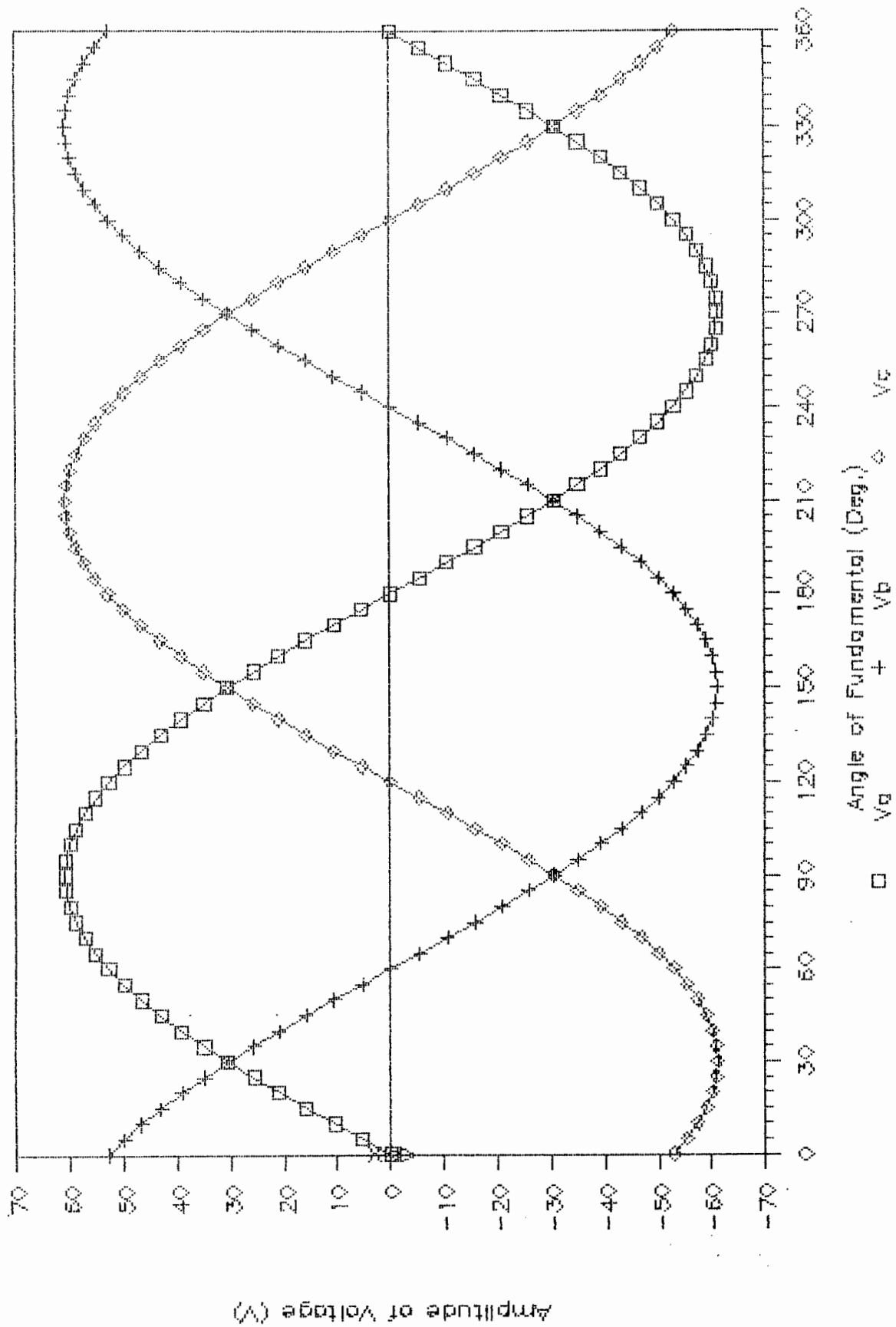
V0= .985431540573  
 ANG V0= -72.8983743999  
 V+= 60.9934333333  
 ANG V+= 0  
 V-= .985431540573  
 ANG V-= 72.8983743999  
  
 I0= .389665156827  
 ANG I0= 122.666786378  
 I+= 3.99773333333  
 ANG I+= 8.3  
 I-= .389665156823  
 ANG I-= -106.066786378

Amplitudes and Angles of Fundamental

Symmetrical Components of Fundamental

Reconstructed waveforms

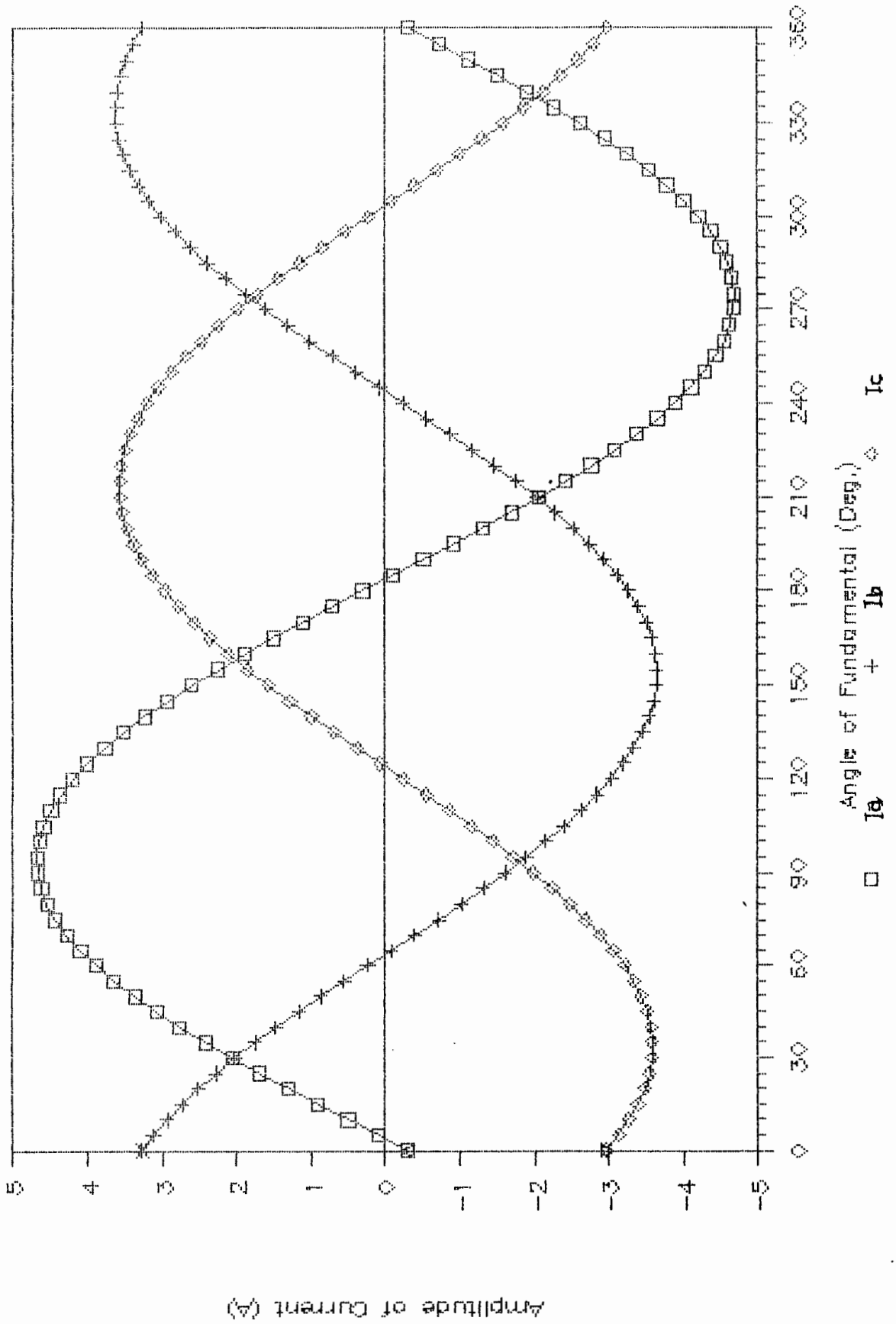
TEST 9



Reconstructed waveforms

TEST\_9

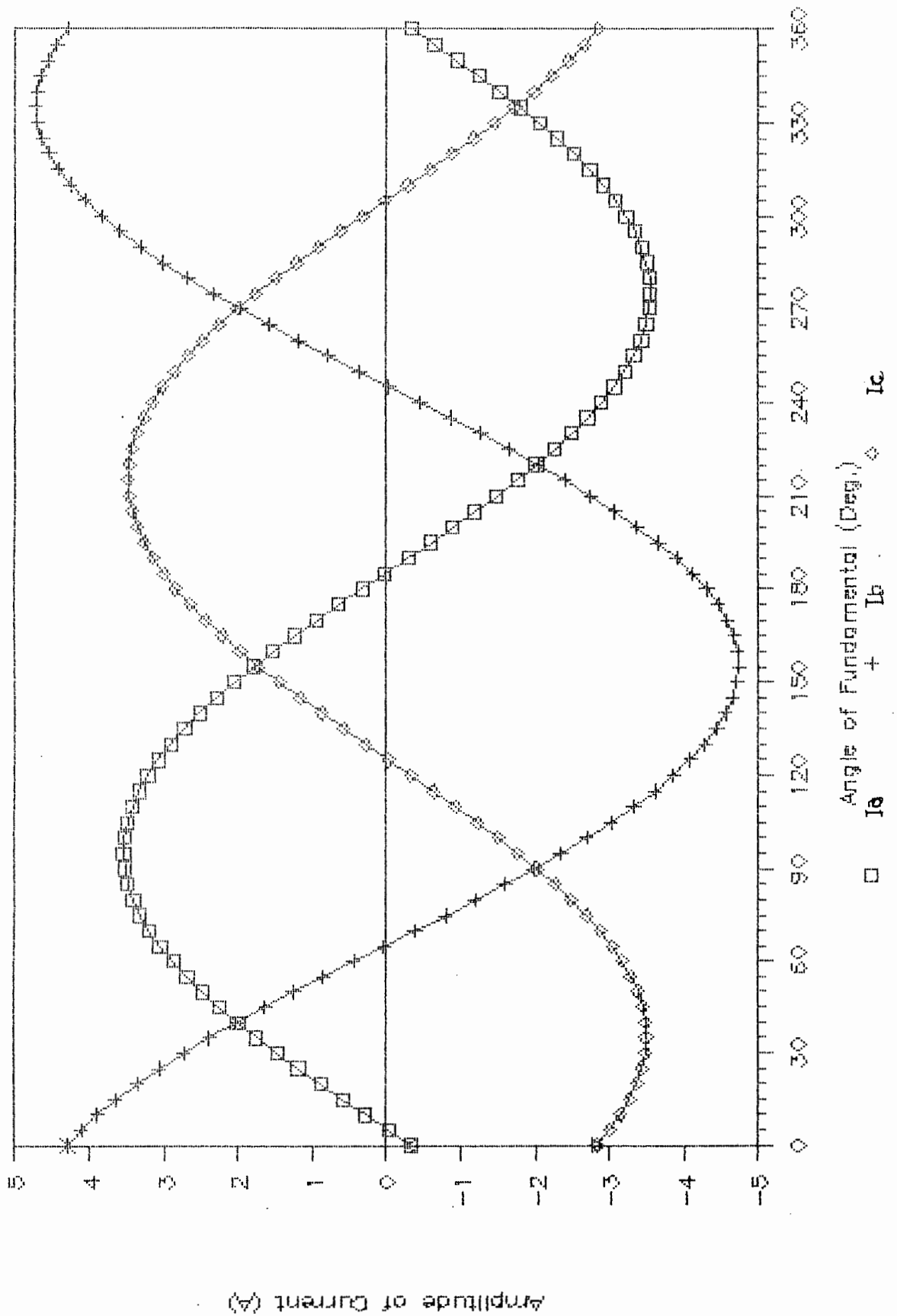
A Phase



Reconstructed waveforms

TEST 9

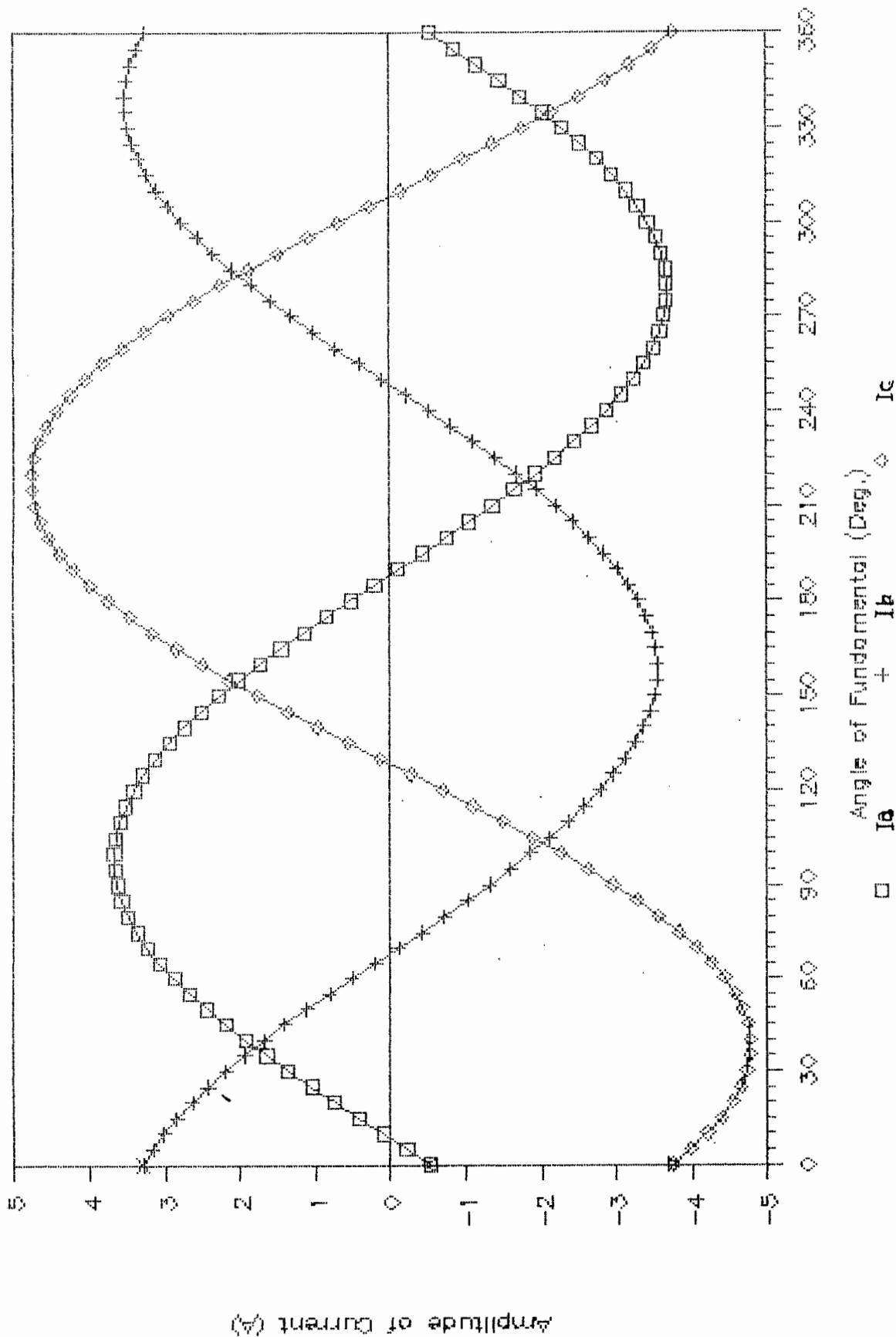
B Phase



Reconstructed waveforms

TEST\_9

C Phase



E47