A HIGH SPEED DATA LINK

Thesis submitted for the Degree of
Master of Science (Engineering)

by

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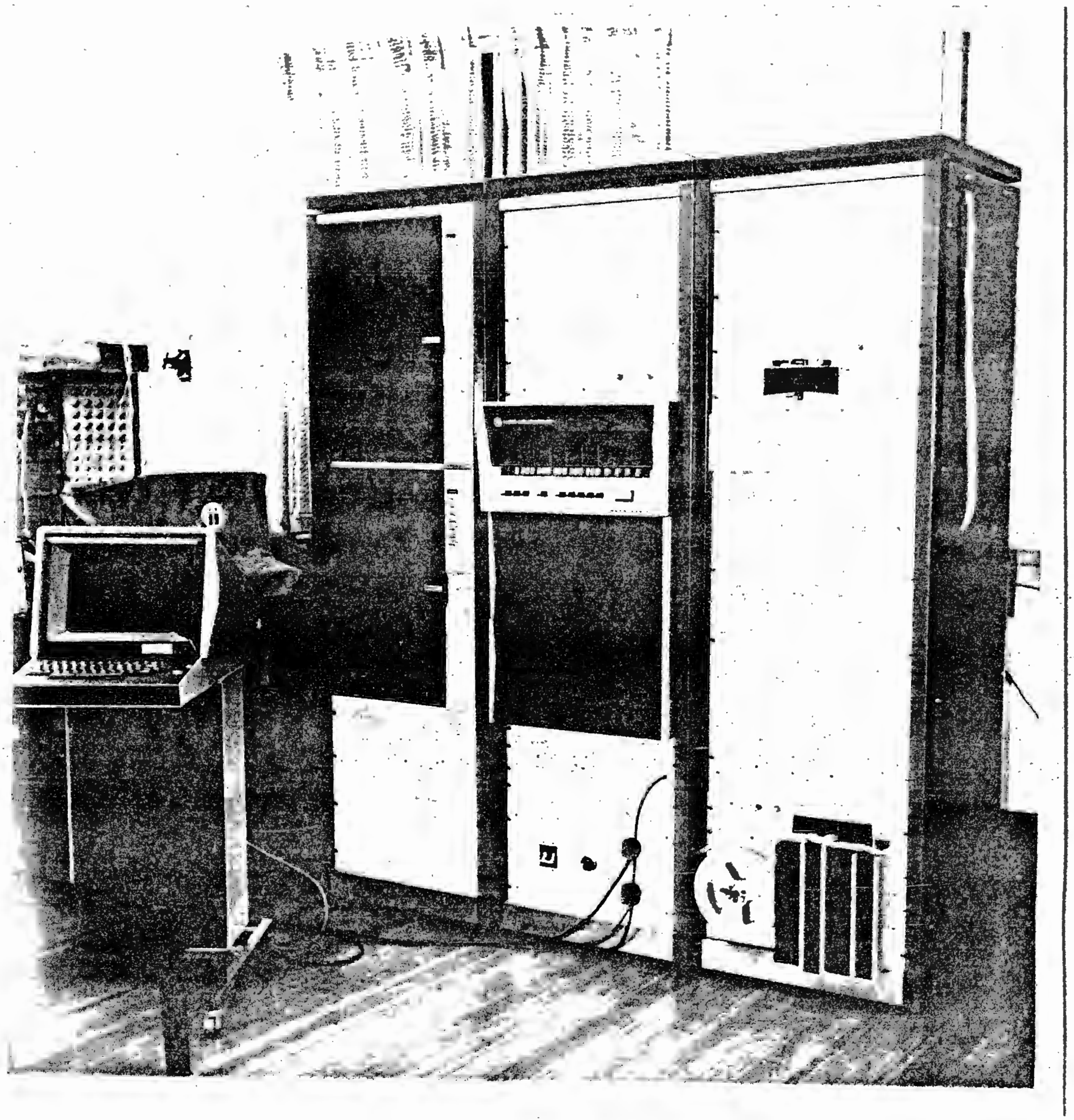
UCT/1979

THE VARIAN 620I MINICOMPUTER.



ACKNOWLEDGEMENTS

I would like to acknowledge my debt to Mr M. G. Rodd, my internal supervisor, who provided assistance and constructive criticism during the past two years.

The Council for Scientific and Industrial Research and the National Institute for Metallurgy are to be thanked for assistance with finance and equipment.

GERALD THORNING

1974

"A High Speed Data Terminal" was presented to the SAIEE on the 8th August,1974 at the Athenaeum,Newlands, Cape Town.

"A New Approach to High Speed Data Terminals" has been submitted as a paper for publication in the SAIEE Proc.

CONTENTS

CHAPTER ONE

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1.1. HISTORY

Work done on a Varian 620I computer in the field of automation and control showed the need for high-speed data terminals that would extend the use of the Varian to remote processes. The need and requirements of such a terminal are very much functions of the past history of work done on the Varian in this field. An outline of this work will therefore not be amiss.

The minicomputer arrived on the market around 1967 mainly as a rather crude device for OEM purposes. The software backup was poor and the accent was on not allowing the mini to gain respectability as a freestanding computer. The mini does, however, fulfil a natural role as a control device in process control applications and it was not long before the machine was used both as a medium-powered freestanding computer and as a dedicated computer in the field of control. The relatively low initial capital outlay in a basic computer consisting of. say, a CPU, 4k of 16-bit memory, a teletype and an input/output port, makes it feasible and even desirable to completely dedicate the mini to one or more tasks. This dedication allowed a new concept in real time control as the machine can be physically placed near the process and direct interfacing between the two is possible. Difficulties do however arise in research establishments and in certain industrial spheres. As the mini gained respectability, manufacturers, taking advantage of an extremely lucrative market, produced better machines with improved software backup, and, paradoxically, a downward trend in the cost of CPU, memory, peripheral devices, and software, with the result that the mini looks less like a mini as it approaches the big machines in capability.

As a result, research establishments in particular, have sophisticated minicomputers at the disposal of a user for part of the time, while doing normal processing for the remainder. While a user has the machine under his control, the machine is to all intents dedicated. In certain industrial applications where the computer controls the process, if the process is slow enough, time sharing can be employed, the free time being spent on general computing.

In the instances mentioned the mini has moved away from the traditional bare minimum and will typically be surrounded by bulk storage devices such as discs and magnetic tapes, and a range of input/output peripherals. The peripheral devices, because of their mechanics, require a controlled environment which in general will be removed from the processes under control. This is particularly true of the industrial environment.

A direct interface is now no longer possible and a link between computer and process for the transfer of data and control instructions is needed. To illustrate the magnitude and type of problem involved, the work that initiated the development of a terminal is described.

1.1.1. RESEARCH USING A VARIAN 620I COMPUTER

With the advent of the mini, research into the digital control of DC machines was started. This initial research used a very basic, portable, Varian 620I, consisting of CPU, 8k of 16-bit memory and a teletype. The computer was used on site. Research evolved a closed loop control system where the speed was sampled and the firing angle of thyristors controlled to maintain the correct speed.

Other work involving the machine was reasearch into the field patterns of a model of an arc furnace. The computer scanned two-dimensional slices of the arc furnace field and produced field plots on a graphic display unit.

As the complexity of this research increased, the computer was increased in memory capability and bulk storage devices such as a disc were added, requiring the computer to be housed in an air-conditioned environment which was 200 metres removed from the area where the research was being conducted.

Anticipating this state of affairs, it became necessary to develop specifications for a link as dictated by the research in progress and to investigate means of implementing this link. Systems developed or being developed were to be assessed, and if unsuitable, the possibility of developing a system was to be investigated.

1.2. THE SYSTEM REQUIREMENTS

Before any assessment of the equipment that is available can be made, the system desired must be clearly specified. In the previous section it was shown that the necessity for some form of link arose when research requiring this link was already well advanced with several man-years spent in the areas of research mentioned. It is these areas that will dictate the requirements of the link and it is according to these requirements that the system specifications were drawn up. In addition to the usual requirements of a design of this nature, several other factors were taken into account.

[1] Considerable time and effort had gone into the development of specialised hardware for the control of plant. In general this hardware was in the form of a direct interface which connected, via control circuitry, the computer's input/output structure to some aspect of the plant.

[2] Because the reasearch in these fields was still in its infancy, all the software was custom designed for the

project, and was intimately related to the nature of the hardware mentioned above.

[3] The researchers involved had generated considerable know-how and familiarity with the equipment as it stood. Any reallignment of thinking in an area which was secondary to the main body of research was not an advantage.

The three factors indicate that any link should be implemented such that hardware and software that had been developed while the computer was on site should be compatible with the remote or terminal end, and that the researcher be presented with a system which bears a resemblance to the system he is familiar with. This suggests a transparent link and terminal. The computer does not address the link and is unaware of its existence. Any hardware at the remote point is accessed in a similar manner to that when the computer was on site.

1.2.1. SYSTEM SPECIFICATIONS

Section 1.2. dealt with the system requirements. These requirements introduce the first basic specification of a high-speed terminal.

First Specification The terminal must present to the user a system which is similar to the computer's input/output structure in terms of both physical dimensions and electrical quantities. This is equivalent to extending the input/output structure to the remote point. Appendix I gives a detailed description of the hardware and software format of the Varian 620I input/output structure.

Although this approach was primarily dictated by user needs, it does enjoy other advantages. Economically, the compatibility with existing hardware and software is an added attraction. It also permits the use of standard Varian hardware, such as input/output port chassis and power supplies at the remote side.

The second bounding factor that is to be applied is that of economics. The machine is to be suitable for use in industrial applications as an extension of a computer. With a complete computing system only costing several thousands of Rands, for a terminal to be of use, it must have distinct advantages over replacing it with a dedicated computer. The total capital cost of cabling and hardware should therefore be as low as possible. This economic comparison between a basic computer set-up and the terminal is not altogether valid, as the purpose of the terminal is to place the controllability of a fairly large computing system at the disposal of a user woring in a remote industrial enviroment.

Economics does, however, become a factor in the choice of elements for implementing the link. The cost of the system is a complex one which must take factors such as space occupied, power consumed, voltage rails required and simplicity of design into account. As it is described in Appendix I, the input/output structure consists of a number of slot positions wired in parallel so that all the input/output signals appear at each position. Any card inserted into a slot will have access to the entire input/output bus. Each of these slot positions represents a sizeable capital investment and interface designs are limited to as few of these positions as possible.

The Varian board for insertion into the slots is designed to contain fourteen pin- and sixteen pin wirewrap sockets with no provision made for discrete components. All discrete components are mounted on component headers and inserted into the wirewrap sockets. Limiting a design to the use of this board only as the interface between the computer and the transmission medium is restrictive in the choice of components and modes of transmission available. A careful assessment of economic attractiveness, compactness, power supply requirements and design flexibility is necessary and is discsuused in a further chapter. Reflection on these points does, however, reveal a second broad specification.

Second Specification

(i) Restrict the design of the interface between the computer input/output and the transmission link to as few input/output slot positions as possible, and, as a corollary, restrict components to fourteen- and sixteen pin DIL circuits requiring ± 5 or ± 12 volts.

While adding to the simplicity of the design, the specification above is restrictive to design approach and is more a desirable feature than specification.

(ii) The voltage requirements of components must be a factor in their selection. The disadvantages of having supplies other than the standard computer supplies are obvious.

(iii) Component availablity and reliability. Recent years have seen a proliferation of components, particularly in the data transmission field, without a corresponding increase in information and application. This, together with high prices and the apparent hesitancy of manufacturers to second source certain of the more exotic components, makes the choice of components a compromise between what is suitable and what can be obtained.

Third Specification The feasibility of implementing a high-speed link was to be assessed as quickly as possible. On the strength of this the direction of research involving the possible use of a terminal was to be decided.

* * *

CHAPTER TWO / THE STRUCTURE OF THE TERMINAL

2

2.1. INTRODUCTION

A terminal that is a replica of the computer input/output structure in terms of physical dimensions and electrical quantities is one of the specifications of the system. Since these quantities form the basis around which a design will proceed, they are discussed in this chapter.

2.2. PHYSICAL ASPECTS OF THE TERMINAL

The input/output port of the Varian 620I consists of a number of similar slot positions with the backplanes of the slots wired in parallel. A card inserted into a slot has access to all of the data and control lines as well as the Varian power supply. A number of these slot positions are housed in a frame measuring 22 x 19,5 x 11 inches to give an input/output chassis. Cards controlling interface device controllers are inserted in the slot positions. These cards can take two forms.

[1] A printed circuit board. Because of the complex layout problem involved in producing a PC board for a digital design, the use of the PC board is generally limited to the commercially available mass-produced product. The economics involved places it beyond consideration in a "one of" design and in any event must be limited to a final design. Printed circuit techniques do not lend themselves to the modification of boards.

[2] The Varian interface board. This board contains a number of positions that will accept fourteen- and sixteen pin DIL wirewrap sockets with $\pm$ 5 and 12 volt supply rails

extended to various points on the board. It is on this board with its layout flexibility that development interfaces are produced. The use of this board does restrict the choice of components in terms of shape and power supply requirements, but it does introduce some interesting features.

(i) The proposed system configuration has all the signals present on the computer input/output reproduced at the terminal end in a chassis containing a number of the input/output slots. Figure 2.1.a. is a block diagram of the proposed system. It consists of an interface at the computer containing control logic, a bi-directional transmission system for the shifting of data and control information between the computer and the terminal, an interface at the terminal connecting the transmission system to the terminal input/output slot, and finally the terminal structure itself.

By restricting the choice of components to those compatible with the Varian interface board, the system is reduced to that illustrated in Figure 2.1.b. The entire terminal system now consists of circuitry on one or more of these boards at each end of the link, the transmission link, and the terminal chassis supply. In this configuration a simple compact and flexible system exists, a particularly attractive approach for industrial application.

It remains to show the practicability of implementing this system. A suitable transmission technique and elements for applying this technique will be discussed in further chapters.

(ii) Time, cost and difficulty of manufacture make the manufacture of a custom designed board for insertion

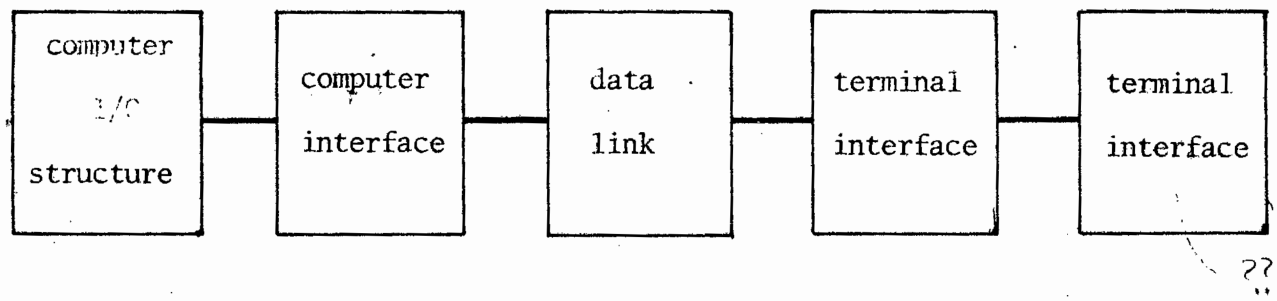
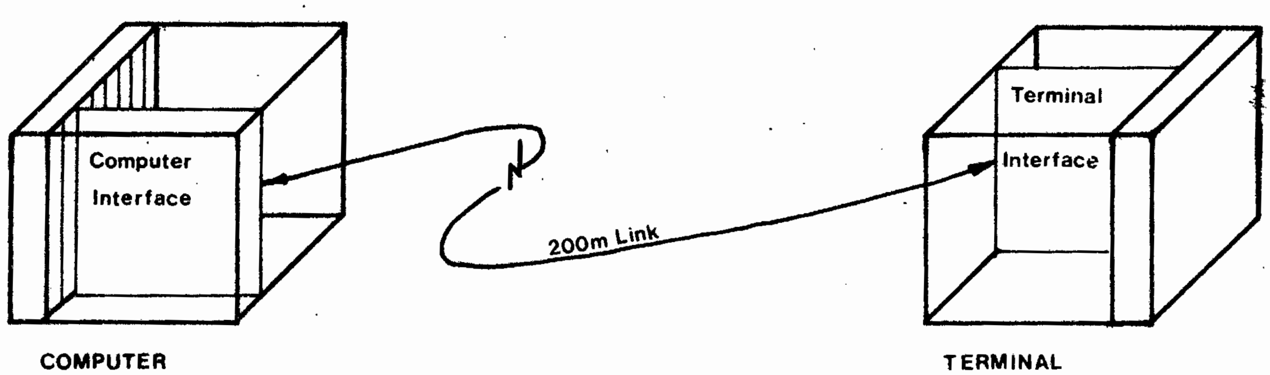


FIGURE 2.1.a

FIGURE 2.1.b



into a slot position and capable of mounting components other than sixteen- or fourteen pin wirewrap sockets prohibitive. As with PC boards this would be limited to a final design in any event. One means of overcoming this restriction of components is to have an intermediate board that connects the Varian board to the transmission system. Location of the board and additional connecting cables are problems which do not encourage this approach.

(iii) Components requiring voltages other than those available from the standard Varian computer supply will necessitate an external supply. Again this detracts from the ideal of producing a viable industrial product, the success of which will be related to its simplicity.

Possible earth problems could arise and modifications to theexisting supplies would be necessary to include the external supply in the switching of these supplies.

2.3. ELECTRICAL CHARACTERISTICS OF THE INPUT/OUTPUT STRUCTURE
The input/output system, a party line, time-shared input/output bus has three elements that need to be reproduced at the terminal.

[1] The set of sixteen bi-directional lines called the E-bus. (EB00 through EB15)

[2] A set of ten individual control lines.

[3] A set of eight interrupt lines.

All these lines follow the negative logic convention with logical true at 0 volts DC and logical false at 3 volts DC.

2.3.1. TIMING OF THE INPUT/OUTPUT MODES OF OPERATION

The timing of the signals on the different control and data lines during programmed input/output operations, interrupt initiated input/output operations and cycle stealing input/output operations are described and patterns in the sequence of operations are discussed.

[1] Programmed input/output operations

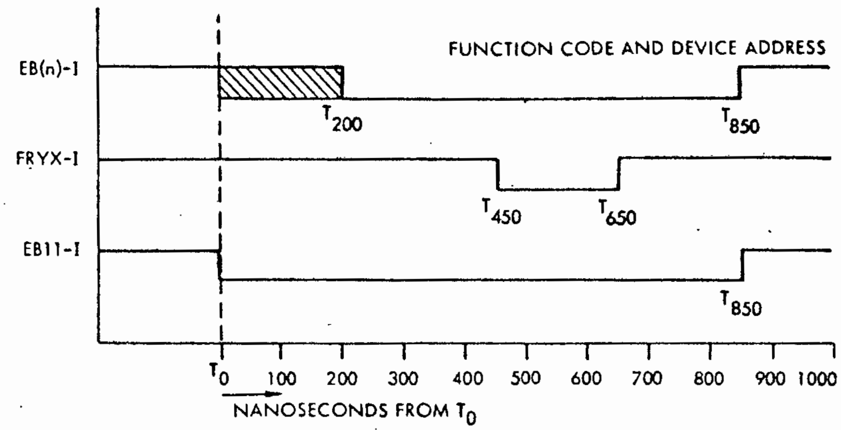
(i) External Control is used to initiate a specific mode of operation in a peripheral device. Figure 2.2. shows the timing of this ~~two~~ one phase operation. For the duration of the pulse on the control line FRYX-I, the device address, the function code and EB11 high are present on the E-bus.

(ii) Programme Sense: The status of a peripheral device controller is sensed by the computer. It is a single phase operation with a device address, the function code and EB12 high for the duration of the pulse on the FRYX-I control line. The peripheral controller has to respond with a true of false condition on the control line SERX-I before the end of the FRYX-I phase. Figure 2.3. illustrates the timing.

(iii) 16-bit word input transfer. The execution of an input transfer instruction is a two phase operation. The first phase selects the peripheral device controller that will participate in the second phase data transfer. The transfer timing is shown in Figure 2.4. The first phase is initiated by the computer which places the device address on EB00 through EB05 with EB13 held true to indicate an input transfer. Again, it is a pulse on the FRYX-I control line that identifies this first phase. During the second phase, a pulse on control line DRYX-I enters whatever has been placed on the E-bus.

FIGURE 2.2.

EXTERNAL CONTROL TIMING



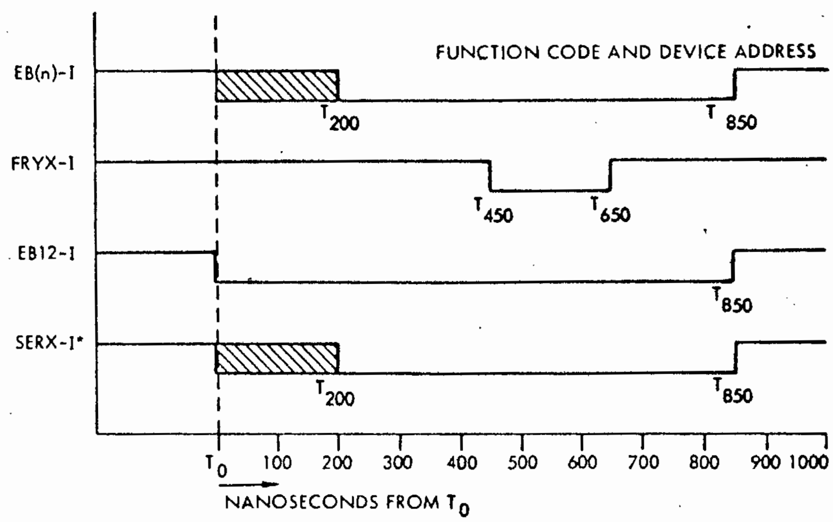
T_0 is the start of the execute phase of the external control instruction.

Logic levels: true = 0 VDC
false = +3 VDC

= time when signal is settling.

FIGURE 2.3.

PROGRAM SENSE TIMING



T_0 is the start of the execute phase of the sense instruction.

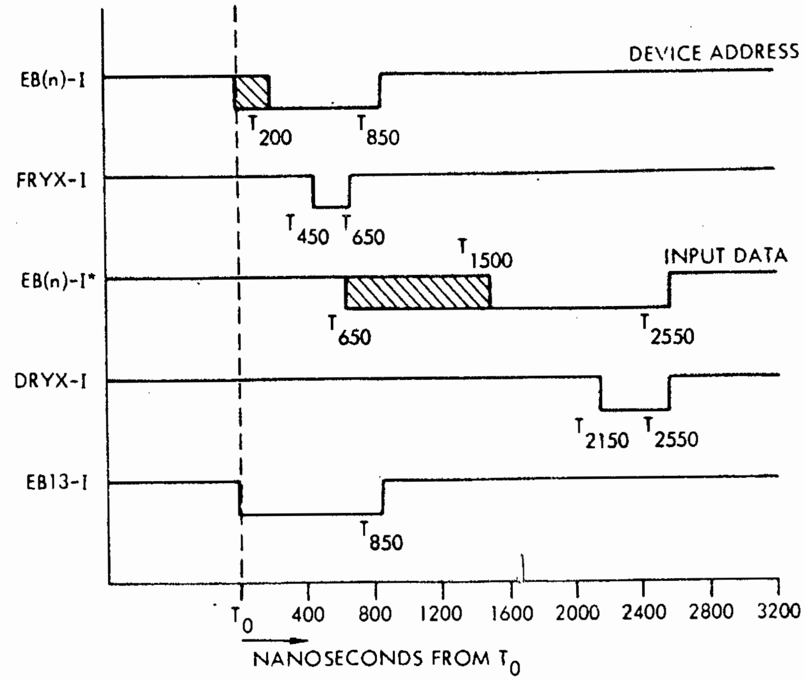
Logic levels: true = 0 vdc,
false = +3 vdc.

= time when signal is settling.

* SERX-I is normally on at T_{200}; it must be on by T_{650}.

FIGURE 2.4.

DATA-IN TIMING



T_0 is the start of the execute phase of the data transfer in instruction.

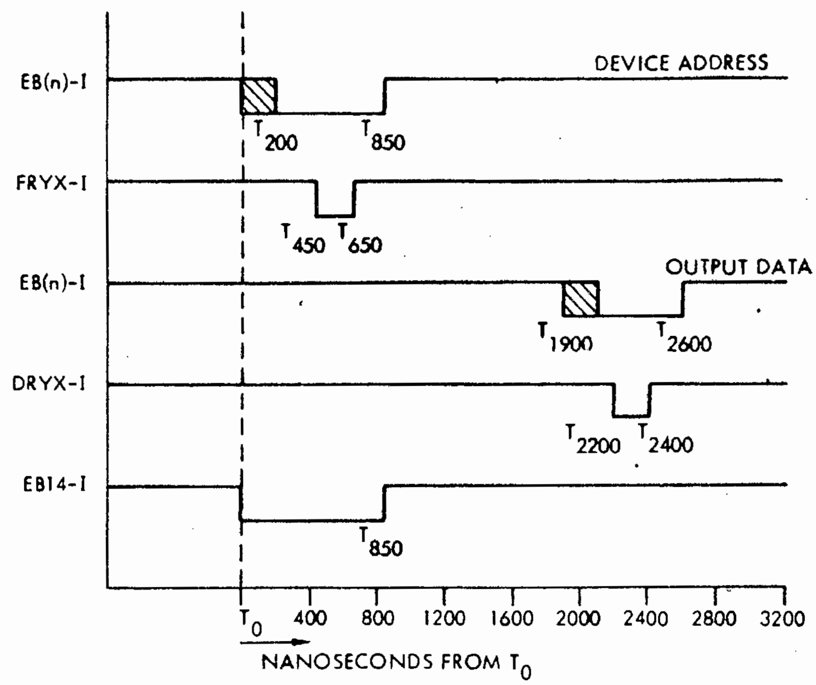
Logic levels: true = 0 vdc,
false = +3 vdc.

[hatched box] = time when signal is settling.

* EB(n)-I (input data) must be off by T_{2700}.

FIGURE 2.5.

DATA-OUT TIMING



T_0 is the start of the execute phase of the data transfer out instruction.

Logic levels: true = 0 vdc,
false = +3 vdc.

[hatched box] = time when signal is settling.

(iv) 16-bit word output transfer. The execution of an output transfer instruction is similar to an input transfer in the sequence of operations except that during the FRYX-I phase, it is EB14 that identifies it as a data transfer out, and it is the computer which places the 16-bit word on the E-bus during the second or DRYX-I phase. Figure 2.5. shows the timing.

[2] Interrupt input/output operations

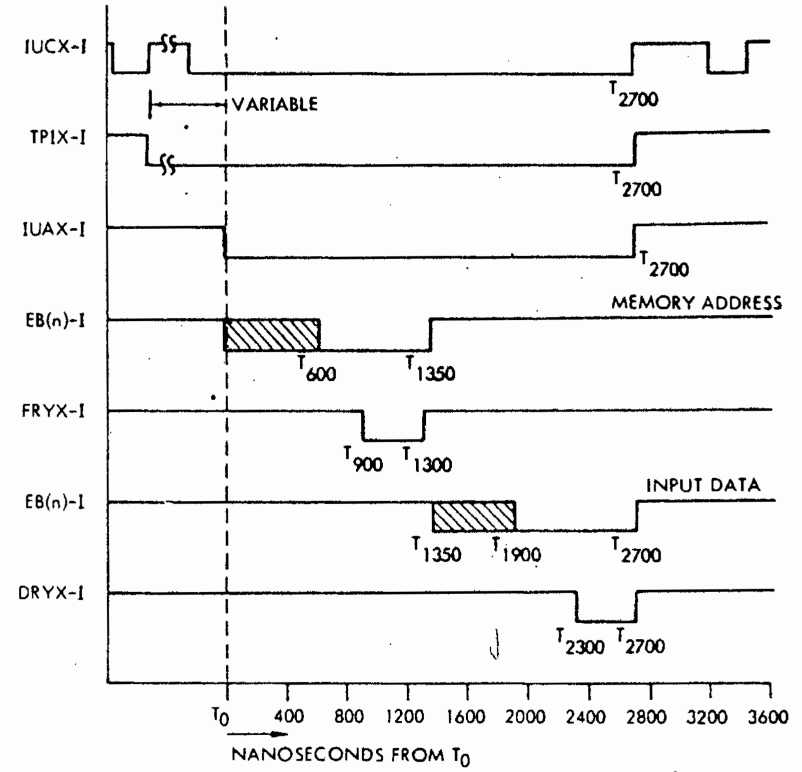
Three of the control lines on the input/output bus allow peripheral devices to interrupt the programme being processed. IURX-I (Interrupt Request) alters the programme flow, TPIX-I (Trap-in Request) stops programme flow and enters a 16-bit word off the E-bus into memory and returns to the programme, and TPOX-I (Trap-out Request) stops programme flow, places a 16-bit word from memory onto the E-bus and returns to the programme.

(i) Interrupt Request. Peripheral devices do not in general generate the entire sequence of addresses, control pulses and so on necessary for an interrupt. Instead this is done by the Priority Interrupt Module (PIM) and the peripheral device controller has access to a set of eight interrupt lines which are arranged in a priority chain. When a peripheral initiates an interrupt request by pulling one of the eight lines down, the PIM generates the necessary address location.

(ii) Trap - in Request. Figure 2.6. shows the timing. The peripheral device requests a Direct Memory Access (DMA) transfer by placing TPIX-I high. The computer acknowledges the request on IUAX-I and inhibits the IUCX-I clock line for the duration of the operation. A two phase operation follows. During the FRYX-I phase, the peripheral device places the memory address

FIGURE 2.6.

TRAP-IN TIMING



T_0 is the start of the input sequence.

Logic levels: true = 0 vdc,
false = +3 vdc.

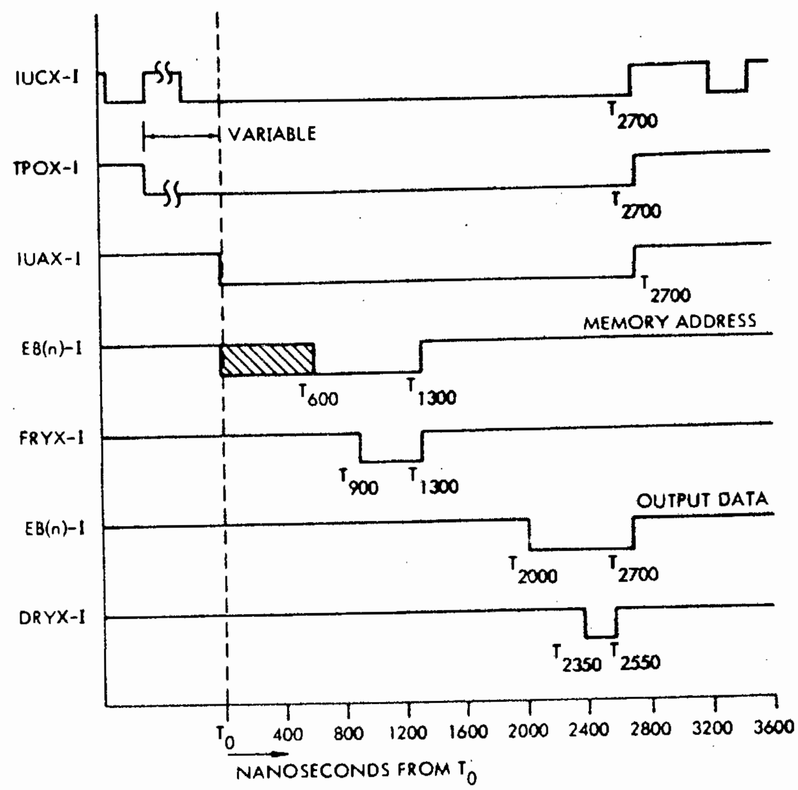
TPIX-I is normally off at T_{2700}; it must be off by T_{2900}.

EB(n)-I (memory address) is normally on at T_0; it must be on by T_{600}. It is normally off at T_{1300}; it must be off by T_{1600}.

EB(n)-I (input data) is normally on at T_{1350}; it must be on by T_{1900}. It is normally off at T_{2700}; it must be off by T_{2900}.

FIGURE 2.7.

TRAP-OUT TIMING



T_0 is the start of the output sequence.

Logic levels: true = 0 vdc,
false = +3 vdc.

= time when signal is settling.

TPOX-I is normally off at T_{2700}; it must be off by T_{2900}.

EB(n)-I (memory address) is normally on at T_0; it must be on by T_{600}. It is normally off at T_{1300}; it must be off by T_{1500}.

at which the word is to be stored on the E-bus. During the second, or DRYX-I phase, a pulse on the DRYX-I control line enters the 16 bits of data that the peripheral device controller has placed on the E-bus.

(iii) Trap-out Request. As shown in Figure 2.7. the timing is similar to that for an input transfer, except during the second phase where it is the computer that places the word on the E-bus.

2.4. PATTERNS IN THE INPUT/OUTPUT TIMING

When the input/output operations are regarded from a transmission point of view, certain similarities between the timing of some of these operations are evident.

[1] The Execute and the 16-bit output transfer instructions. Although the former is a single phase operation and the latter a two phase operation, both have information flow purely away from the computer. Peripheral device controllers do not participate in the operation, but merely accept the information. The peripheral should have been placed in a position to receive this information by prior sense of execute instructions if necessary.

[2] Both the Trap-out Request and the Trap-in Request share a common property in that the peripheral device making the request must supply the memory location address involved in the transfer before the FRYX-I phase.

[3] The sense instruction is rather unique in that the information flow on the E-bus is away from the computer with the status of the peripheral supplied to the computer on line SERX-I before the end of the FRYX-I cycle.

[4] The data transfer in and the trap-in instructions are both two phase operations with data being supplied to the computer by a peripheral during the second or DRYX-I phase.

Two points emerge from this discussion. Firstly, under certain circumstances the direction of information flow on the E-bus is reversed. A choice of transmission system must obviously include this facility.

Secondly, bearing in mind that the objective of the development work is to produce a replica of the computer input/output timing at the terminal, the transmission delay over a link of an appreciable distance is going to have some effect when the computer requires a peripheral to place information at the input/output structure within a specified time after initiating an input/output operation. This problem and its solution is discussed in Chapter 3.

* * *

CHAPTER THREE / TRANSMISSION DELAY 3

The previous chapter described the timing of the different input-output software instructions. What emerged from this was that there could be data flow both in and out of the computer during either the FRYX-I or the DRYX-I phases, this depending on the particular instruction being executed.

The specifications of the system include the point that the link be transparent and that no limits be placed on the user when developing hardware of software. In other words, the terminal amounts to an extension of the computer input-output structure to a remote point.

The requirements of and problems associated with the choice of a transmission system capable of satisfying this become apparent when the timing of operations requiring information to be supplied by a peripheral situated at the terminal is considered . It is intended to provide a terminal which will be some hundreds of metres removed from the computer. Even the most idealised mode of transmission cannot propagate information faster than the speed of light, and assuming an optimistic velocity factor of 0,7, the delay between introducing information into one end of a 200-metre link and receiving the information at the other end will be of the order of one microsecond. In the instance of the Execute and data Transfer-out instructions, data flow is from the computer only, as mentioned. Hence, no switching of information flow is involved and any delay due to the link will merely result in the information arriving at the terminal belatedly. Since the sequence is asynchronous to the peripheral situated at the terminal, the peripheral is unaware of the delay.

However, during the sense instruction, for example, the addressed peripheral must indicate its status on the control line SERX-I within 200 nanoseconds after the computer has initiated the sequence. It will take the information one microsecond to reach the terminal at which point the peripheral must be allowed 200 nanoseconds to respond to the information. Then an additional one microsecond for this response to arrive back at the computer. The total delay between the computer starting the sequence and the response arriving at the computer is 2,2 microseconds. The permitted delay is 200 nanoseconds. Clearly the information has arrived at the computer 2 microseconds, or the round trip delay time along the link, too late. A similar problem exists for all instructions where a response is expected from an addressed peripheral situated at the remote point. It should also be remembered that no delay due to the particular mode of transmission has been allowed for. This will in fact aggravate the problem.

It is necessary at this stage to determine whether the specifications as laid down in Chapter One are at all reasonable. If it is not feasible to implement these specifications, what avenues are open by way of a compromise? It is perhaps at this point that any alternative approach to providing some form of link be investigated.

3.1. ALTERNATIVE APPROACHES TO PROVIDING A TERMINAL

Initially it was laid down that:

[1] the terminal is transparent, resulting in:

[2] existing software for the control of peripherals being compatible with the terminal, and:

[3] existing hardware such as peripheral controllers being compatible with the terminal end.

This led to specifying that the terminal should consist of an extension of the computer input-output structure. Assuming that it is not practicable to overcome the delay problem, a compromise on one of more of the points mentioned above will be necessary.

Point [1]. Points [2] and [3] rely on the fact that the terminal is in fact transparent, with the computer addressing a peripheral situated at the terminal directly, and so a compromise on this point will amount to a compromise on the other two. It must be borne in mind that one of the reasons for adopting this approach is the thousands of Rands that have been invested in existing hardware and software. A deviation from this ideal then opens a whole new area with commercial systems becoming a viable proposition.

For instance, commercially available input-output systems that can connect remote points using the CAMAC concept provide an extremely flexible product, but at a price. Basically the system consists of a highway onto which channels of input-output information can be multiplexed. Appendix IV gives a description of the system.

While being an attractive system that is typical of the commercial product, the system is expensive. A controller interfacing the CAMAC input-output crate and associated control logic to the computer's input-output structure is necessary. A local controller crate as well as a remote crate with the associated supplies are required, and in addition, and perhaps one of the strongest points against this approach, is the replacement of all existing hardware interfaces by those compatible with the CAMAC crate. Software changes in the manner of addressing the peripheral devices will also be necessary since the remote crate is not transparent when connected to a Varian 620I.

For economic reasons alone then, even ignoring the researcher disorientation which would result from the installation of a new and totally unfamiliar system, a system using the CAMAC approach and obtained commercially, is not viable.

The stipulation that the link amounts to an extension of the computer input-output remains and the terminal must either be implemented employing software changes or the delay problem must be overcome. Point [3] then must remain. A compromise on point [2] would be the only alternative possible, and this is discussed in the next section.

3.1.1. SOFTWARE CHANGES TO OVERCOME DELAY

The Varian software includes:

EXECUTE
DATA-IN
DATE-OUT
SENSE
DMA
INTERRUPT

Thes constitute input-output instructions and, as previously discussed, a problem exists when a peripheral at the terminal has to supply the computer with information during an instruction cycle.

A possible solution would be to place constraints on the manner in which input-output routines that involve the terminal are written. If, for instance, a user was constrained to duplicating all instructions when addressing the terminal, then during the first instruction the information is conveyed to the terminal. When the response arrives back at the computer, it is stored in control logic at the computer end of the terminal. The second duplicate instruction then enters the information into the computer.

Sample programme:

Label field	Mnemonic	Variable Field
J0	SEN	0102,J1
J1	SEN	0102,J10
	JMP	J0
J10	CIA	02
	CIA	02

Assuming device with address 02 is situated at the terminal, the first sense instruction senses the condition of function 01 on device 02 and whether this status us true or false continues to the next sense instruction. The second sense instruction is the true instruction and will enter the status of the device which has been stored in the control logic at the computer. If this status had been true, the computer would try to enter a 16-bit word from device 02 into the A register, again by duplication. In this manner, a rather cumbersome but feasible means of implementing the terminal exists.

The factors which detract from the attractiveness of this approach are:

[1] It places rather crude restraints on the user.
[2] Existing software would not be compatible.
[3] The terminal is no longer transparent in that the peripheral situated at the terminal is not addressed in the same manner as the same peripheral were it situated at the computer.

In conclusion, then, it can be stated that this method approaches the requirements of a link as a compromise, and it remains to show whether it is at all feasible to overcome the delay problem with hardware.

3.2. A SOLUTION TO THE DELAY PROBLEM

The problem arises because of the conflict between two fundamental processes, the input-output timing and the delay along the link. The question arises, is it possible to alter either of these two? Previously it was mentioned that the delay is inevitable. The alternative therefore is to investigate whether it is possible to alter the input-output timing of the computer.

The following points must be borne in mind:

[1] If the timing is to be altered, it must be done so that the time content of the information is not lost as the object of this approach is to produce a replica of the normal timing at the terminal. In other words, the information present at the computer must always be sufficient to reproduce exactly the input-output timing at the terminal.

[2] Any addition or modification to the CPU should be minimal. Complex alterations to the CPU detract from the simple flexible system and will result in scepticism on the user's part. These alterations must be regarded with caution as particularly in the case of the Varian, the generation of timing pulses by the control logic is complex and includes a tremendous amount of redundancy. Modifications to this circuitry could have side effects which are difficult to assess but which affect the ultimate reliability of the computer. This suggests that any timing control be done at an early stage in the generation of the timing pulses.

[3] By controlling the timing of an input-output sequence, software will not draw a distinction between a peripheral situated at the terminal and the same peripheral situated at the computer. It will however be necessary for the logic involved in altering the computer's input-output timing to know whether the peripheral is at the computer or at the terminal. If this distinction is not drawn then whenever a peripheral has to provide the computer with some information during the execution of an instruction, the timing will be interfered with, even if the peripheral is situated at the computer.

3.2.1. TIMING AND CONTROL OF THE VARIAN 620I

Basic timing signals are derived from a master clock circuit located on processor card DM112. The master clock is generated by a crystal-controlled oscillator operating at a frequency of 8.8MHz which is counted down and passed through a pulse-width adjustable one shot to produce a continuous train of pulses typically 56 nanoseconds wide, spaced 450 nanoseconds apart. This output is used to generate the various clock signals shown in figure 3.1. These pulses are only the start of a very long train of pulses.

The Varian 620I has a basic machine cycle of 1,8 microseconds. All operations performed by the computer are accomplished in some multiple of the master clock timing cycle. The basic clocks generated from the master clock are used to time three operating

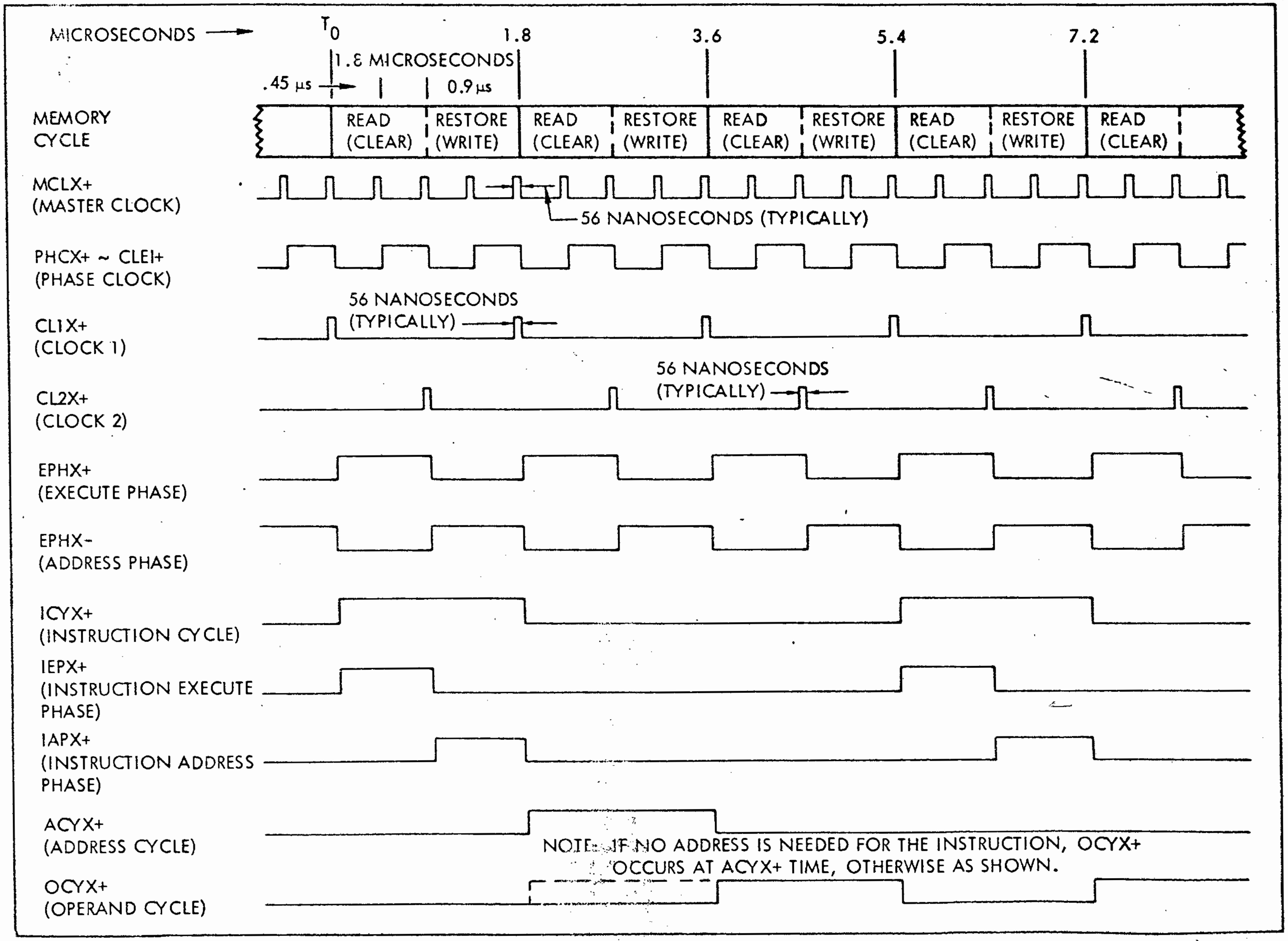


FIGURE 3.1. CLOCK AND PHASE TIMING

sequences: Instruction cycle (ICYX+), Address cycle (ACYX+), and Operand cycle (OCYX+).

Figure 3.2 shows the master clock. Notice how the timing immediately begins to split into various timing sequences. Referencing the section on the Processor Control #4 which contains the clock generation circuitry, in the Varian Data 620I Maintenance Manual Volume Two, shows the rapid manner in which the basic clock signal is divided up into the various pulses. Any modification to this circuitry must be done as early in this generation sequence as possible.

3.2.2. HALTING THE COMPUTER CLOCK TO OVERCOME THE DELAY

Earlier on in this chapter, it was stated that since the timing is to be reproduced at the terminal, alteration of timing must be accomplished such that sufficient information is always present on the input-output structure for the reconstruction of the normal timing at the terminal. A feature of the Varian's approach to the input-output sequencing is that all the information necessary to identify the instruction that is to be executed and the peripheral that is being addressed is on the input-output structure for the duration of the first or FRYX-I phase.

Coupled to this is the fact that the sense instruction needs a reply from the peripheral before the end of the FRYX-I phase. Two conclusions can be drawn from this:

[1] To satisfy the sense instruction requirements, it is neccesary to implement any timing changes immediately the FRYX-I phase commences.

[2] All the information required for the reproducing of the input-output timing is present immediately the FRYX-I phase commences.

Since these two points do not contradict each other this approach was further investigated.

As mentioned earlier, the increasing complexity of pulse generation

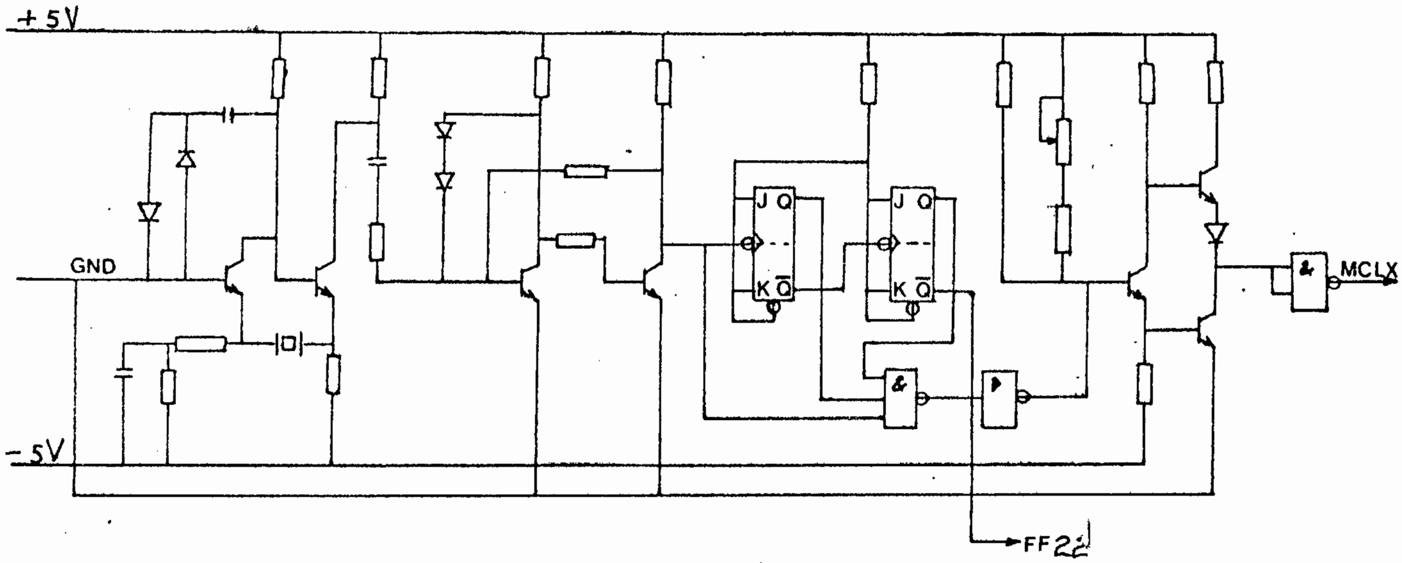
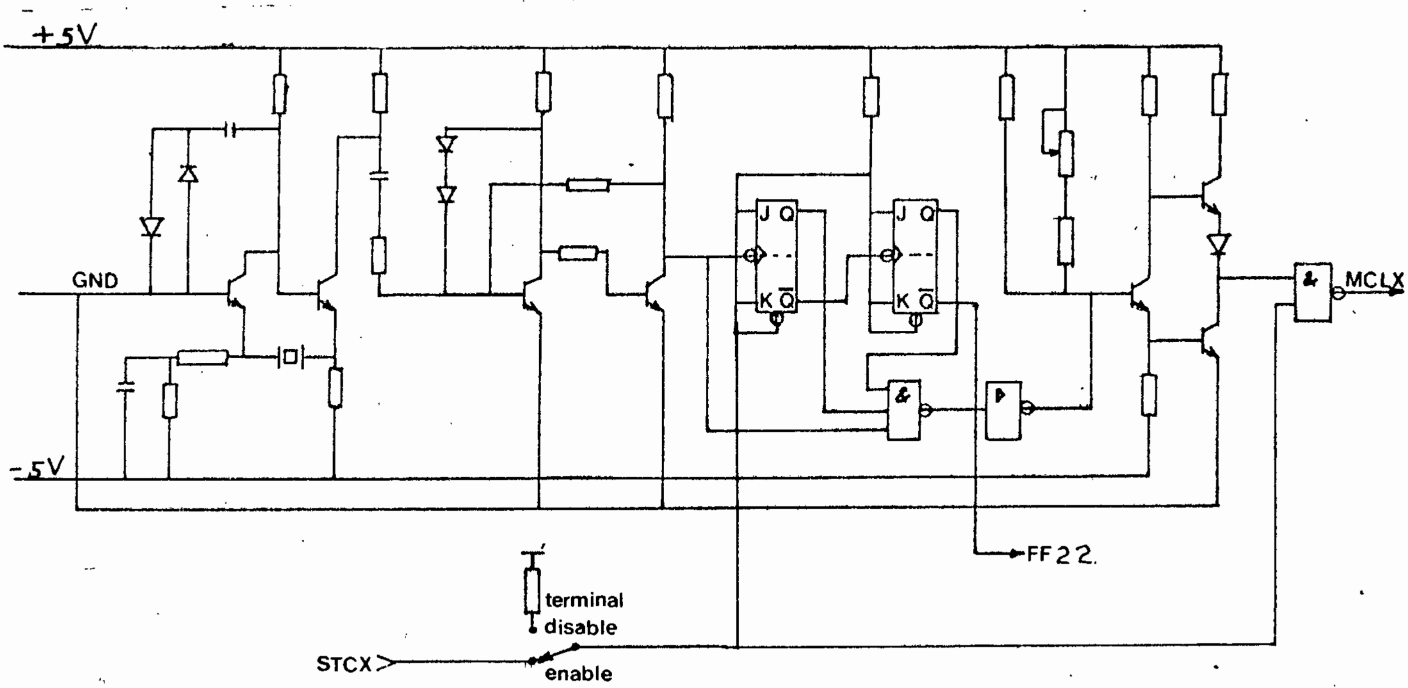


FIGURE 3.2. MASTER CLOCK

FIGURE 3.3. MODIFICATIONS TO INHIBIT MASTER CLOCK



as one moves from the master clock generator suggests that any modification be done right at the master clock itself. Referring to Figure 3.2, investigation showed that if after the FRYX-I phase has started the clock output was frozen by inhibiting the JK flip flops in the divider chain and by inhibiting the output of the MCLX+ line, the entire computer was held in a state of suspension. For as long as the clock is inhibited, the information present on the input-output bus at the start of the FRYX-I phase is held there. When the clock is restarted, the computer continues with the normal timing of the input-output sequence.

A situation now arises where the computer is stopped whenever the data is required from a peripheral. This allows the information to reach the terminal. The terminal then reconstructs the input-output timing, extracts the information from the peripheral, and sends this information to the computer. The computer must be halted for a period that allows the information to arrive back at the computer at the instant when it is required. The delay required is that of twice the delay along the link. Figure 3.3 shows the modified clock generator with the facility to inhibit its output.

Extensive testing of this approach was done to assess the effects on the computer and the timing of the input-output using a dual beam oscilloscope. The period for which the computer was halted was varied randomly and its effect noted. In all instances the computer timing which is edge triggered was not affected. The input-output timing was correct, except that the FRYX-I pulse width varied by up to 10 nanoseconds, depending on the period for which the computer was inhibited. Since the normal pulse width is a minimum of 200 nanoseconds, this variation was ignored.

Using this approach the terminal will most closely approach that specified in Chapter One. A problem does arise however since the link is no longer entirely transparent. It is necessary to distinguish whether a peripheral is situated at the terminal or at the computer. If this is not done, the computer will be halted whenever it requires a peripheral to supply data, even if that peripheral is sutuated at the computer. The next section deals with this problem.

3.2.3. IDENTIFYING THE LOCATION OF A PERIPHERAL

All software developed for the control of peripherals and these peripherals themselves must operate equally well at the computer or at the terminal. It is therefore the terminal control logic situated at the computer which must distinguish whether the peripheral being addressed is at the computer or at the terminal. If the device is at the terminal, the computer is to be halted.

This suggests a system where all the addresses of peripheral devices situated at the terminal are stored at the computer end of the link. When the computer addresses a peripheral device whose address is held in the store, and it is an instruction that requires data from the peripheral, then the computer clock must be inhibited. Obviously the peripheral devices that are inserted at the terminal are purely a function of what a particular user needs and so the contents of this store must be alterable. This identifying circuit must then at least contain:

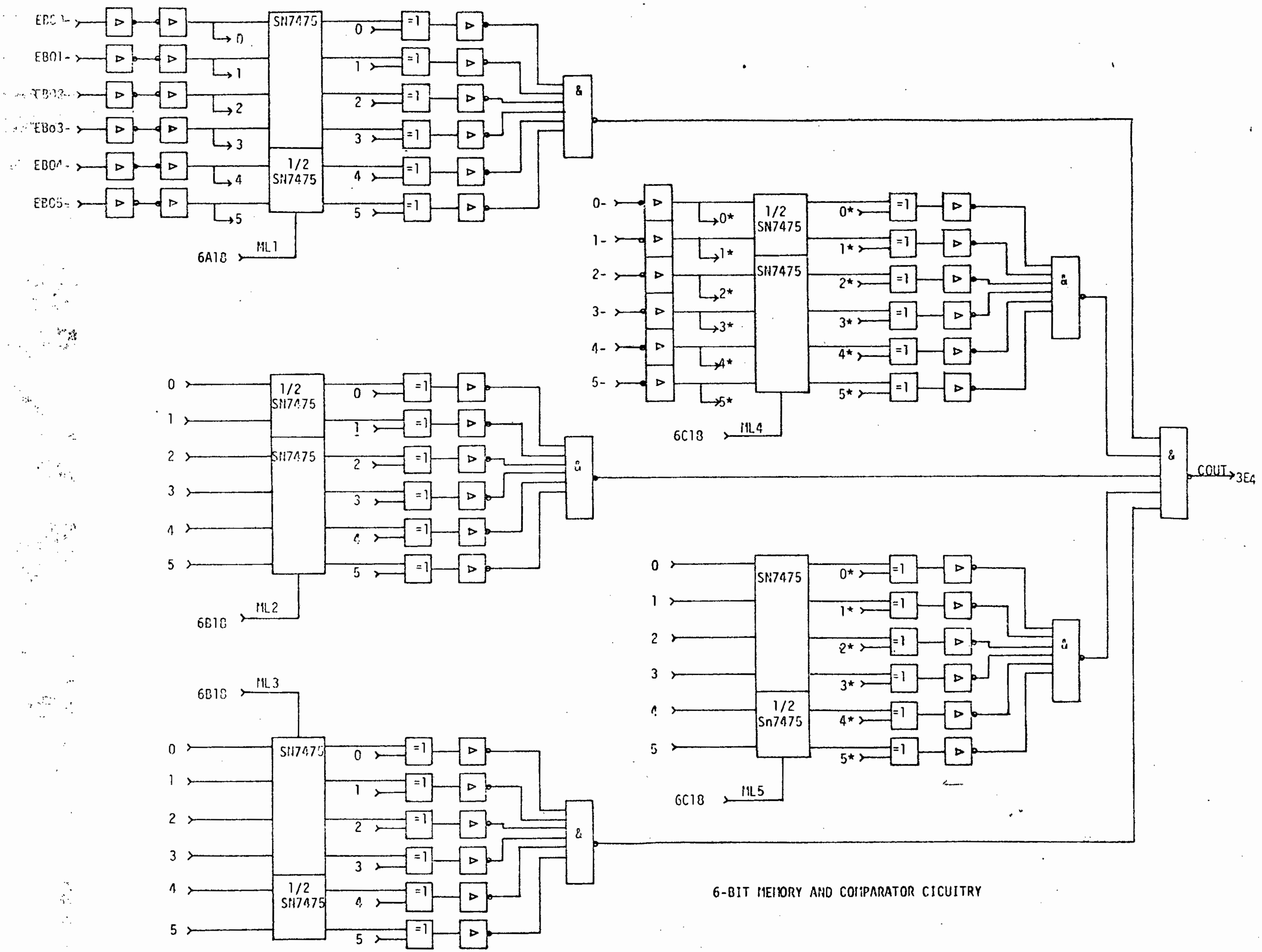
[1] A store capable of holding several 6-bit words which correspond to the peripheral addresses.
[2] The contents of the store must be alterable. Since the contents of the store must be dictated by the user, the approach used was to have the store loaded by software

The contents of the store must be compared with the first 6 bits of the E-bus. If the address on the E-bus corresponds with any of those held in the store and it is during a cycle requiring the peripheral to supply a response to the computer, then the computer must be inhibited. Figure 3.4 shows the implementation of this using conventional TTL logic.

The store consists of five sets of 6-bit data latches. To load addresses into the 6-bit latches, the circuit is situated at device address 76.

The instruction: EXECUTE 0176 will select the first 6-bit set of

FIGURE 3.4.a MEMORY AND COMPARATOR



6-BIT MEMORY AND COMPARATOR CICUITRY

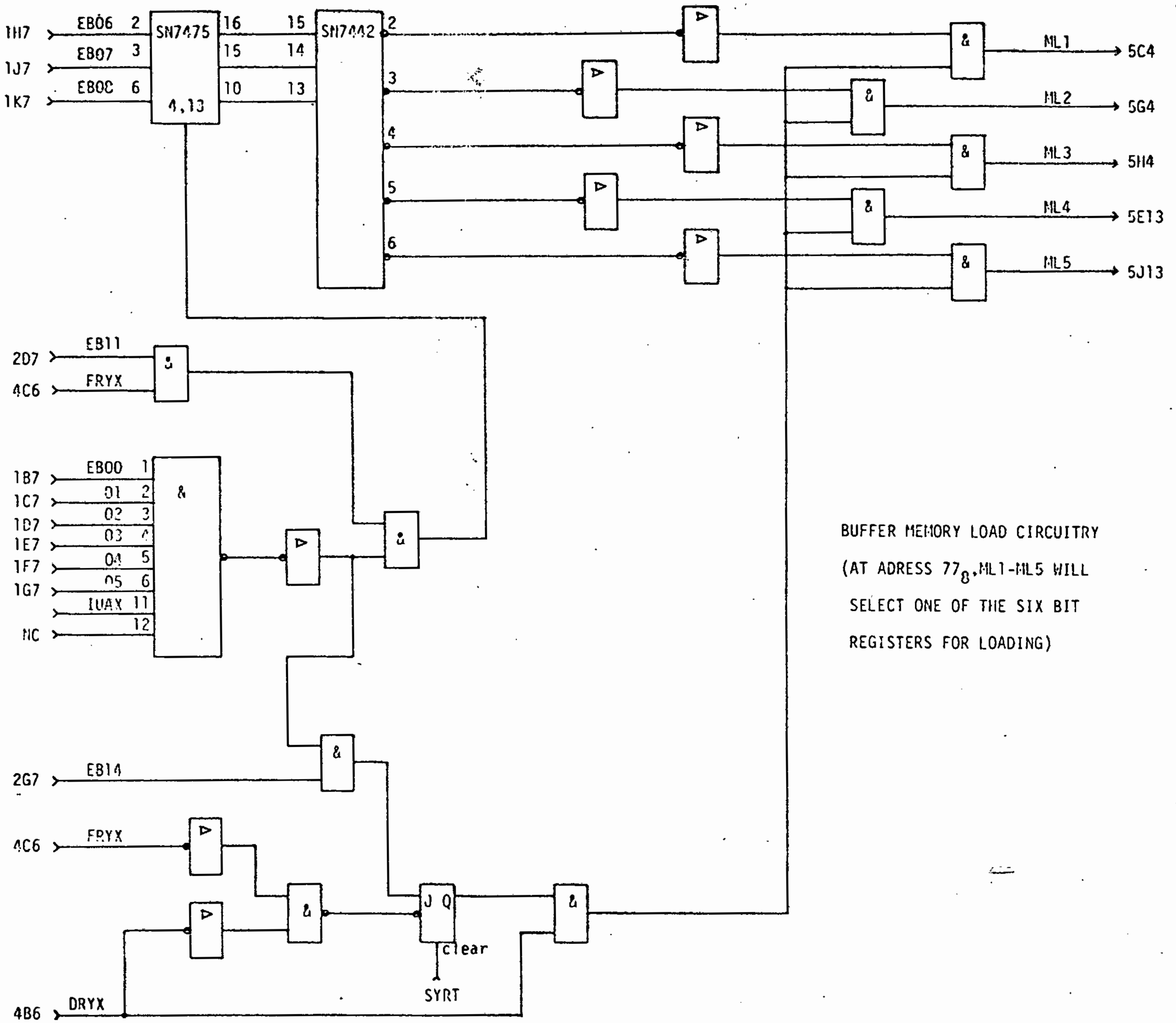


FIGURE 3.4.b MEMORY LOAD CIRCUITRY

latches, and then EXECUTE 0276 will select the second set, and so on. After a particular set has been chosen and output instruction to address 76 will load that register.

Sample Programme:

Label Field	Mnemonic	Variable Field
	START	
	LDAI	01
	EXC	0176
	OAR	76
	LDAI	05
	EXC	0276
	OAR	76
	HALT	

The first store is selected and 01 is stored in it. After that the second 6-bit store is selected and 05 is stored in it. (NOTE: All figures are in octal).

Once the latches have been loaded any further address that appears on the E-bus during the FRYX-I phase is compared with those in store. If any of the addresses in store correspond to that on the E-bus, and it is a data-in instruction, the computer is inhibited.

Using this approach where the terminal is to reproduce the computer input-output structure and any delay due to the link delay as well as delay due to the particular mode of transmission used is overcome by inhibiting the computer clock output, it becomes necessary to provide a transmission link that will implement this. Chapter 4 deals with this problem.

* * *

CHAPTER FOUR / THE DATA LINK

4

4.1. INTRODUCTION

The data link provides the path along which data transfers between the computer and the terminal must take place. The method adopted for implementing the link must be adequate to handle the volume of data in the time allocated, and in addition, must account for the environmental and economic factors.

The information is present in a parallel format on the input-output structure at both the terminal and the computer. The link must be capable of transferring the data in a suitable format and exactly reproducing information at the opposite end. Information which must be conveyed by the link can be divided into several categories.

[1] The information on the E-bus. The E-bus is bi-directional with the sixteen bits of information going either in or out of the computer. At any given instant the information flow is in one direction only. This allows some scope in the choice of link as for transmission of the E-bus one bi-directional channel or two separate channels could be used.

[2] Control lines which convey control pulses out of the computer. Among these are the FRYX, the DRYX, the SYRT, the IUCX and the IUAX control lines. The FRYX and DRYX phases are associated wth information on the E-bus. SYRT, the system reset, can occur outside any input-output instruction cycle, while IUCX is a continuous clock pulse at 1,1 MHz and IUAX is associated with the interrupt system.

[3] The control lines and eight interrup lines which convey in-

formation to the computer.

[4] Ancillary information such as computer status indication.

Whether parallel or serial or more sophisticated techniques are used for data transmission it is the data described above which will affect the choice.

4.2. SPEED REQUIREMENTS

In addition to being suitable for transmission of the data as it is described in the previous section, the technique and components used must be capable of processing and conveying the data at a sufficiently high speed. Essentailly it is the use to which the computer will be put that dicates the desired speed of operation and, consequently, the form of transmission line used.

The work already done in the areas of process control and data capture had a Varian computer facility for use on site with direct access to the computer input-output structure. All hardware and software was developed using this speed of operation, even if the plant controlled did not require this. Coupled to this is the fact that projected forecasts of future research predict that the research will move into the area of multiple process control. A derating of the speed at which the terminal can process input-output operations will amount to a derating of the machine's performance as a whole, narrowing the area of application of the terminal.

Before any time for information processing is allowed for, there already exists the time interval required to allow information to propagate along the link. The question that arises is to what extent can time be allocated for information processing at either end beyond the inevitable link delay? The answer to this can only be qualitative. Any additional delay should be as small as possible. The choice of transmission line should therefore be the fastest allowed by criteria such as economics, environment and simplicity.

4.3. SERIAL TRANSMISSION

Transmitting data in a serial form can have distinct economic advantages over parallel transmission. The number of components, cable connectors and cable size are all reduced and a more elegant solution is achieved.

4.3.1. THE THEORY OF SERIAL TRANSMISSION [10, 11]

In modern high speed data transmission, synchronous transmission, where the entire message is transmitted sequentially with equal time-slot widths assigned to each symbol, is used. A block diagram of the transmission system is shown in Figure 4.1.

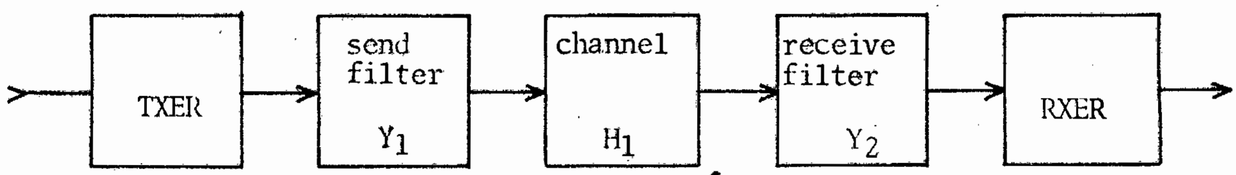


FIGURE 4.1. TRANSMISSION SYSTEM

An input shaping filter with transmittance function $Y_1(f)$ is inserted between the transmitter and tha channel input. The channel is assumed to have transmittance function H(f). There is an output shaping network or receiving filter with transmittance function $Y_2(f)$ between the channel output and the decision making part of the receiver. The resolution of the signal into sinusoidal components can be simply performed at any point in the system in terms of the Fourier transform of the original signal:

$$S(f) = \int_{-\infty}^{\infty} S(t) e^{-j2\ ft} dt \qquad 4\ [1]$$

$$= \sum_{n=-N}^{N} G(f) e^{-j2\ nfT} \qquad 4\ [2]$$

Where a message consisting of 2N + 1 symbols produces a wave form:

$$s(t) = \sum_{n=-N}^{N} b_n g(t-nT) \qquad 4\ [3]$$

with $T = \frac{1}{f_s}$, the sampling period

b_n = a distinct symbol

g(t) is a standard pulse emitted by the transmitter.

The output of the receiving filter is:

$$Q(f) = Y_2(f)\ H(f)\ Y_1(f)\ G(f). \qquad 4\ [4]$$

and the signal from the receiving filter is given by:

$$r(t) = \int_{-\infty}^{\infty} Y_2(f)\ H(f)\ Y_1(f)\ S(f) e^{j2\ \ ft}\, df \qquad 4\ [5]$$

$$= \sum_{m=-N}^{N} b_n \int_{-\infty}^{\infty} Q(f) e^{j2\ \ f(t-nT)}\, df \qquad 4\ [6]$$

$$= \sum_{m=-N}^{N} b_n\ q(t-nT) \qquad 4\ [7]$$

The four different functions $Y_2(f)$, $Y_1(f)$, H(f) and G(f) are combined as a product to form one function Q(f) which completely determines the wave from which the message is to be read. The channel function H(f) is typically an initial condition. The Fourier transform G(f) of the standard signal pulse g(t) is associated with the switching process at the transmitter. The two filter functions $Y_1(f)$ and $Y_2(f)$ are then adjusted to give the desired Q(f).

The object of serial transmission is to deliver the sequence of values b_n at the receiver. The transmission problem thus reduces to establishing means of recognising the individual B_n's in the received signal wave of equation 4 [7]. One obstacle to be overcome is the intersymbol interference resulting from the overlapping of the functions q(t-nT) along the time scale. Basic methods for suppressing intersymbol interference in a band limited system were proposed by Nyquest. His first method, known as Nyquest 1, requires that q(0) is a non-zero contant A and that q(mT) vanishes when m is any positive or negative integer. In this manner each pulse is sampled when contributions from all other pulses pass through zero. In mathematical terms this requires that:

$$q(mT) = A\ \delta_{m0} \qquad 4\ [8]$$

where δ_{mn} is the Kronecker delta defined as unity when m = n and zero otherwise. This yields

$$q(mT) = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} e^{j2\pi m\frac{f}{fs}} \sum_{n=-\infty}^{\infty} Q(f+nfs)df \qquad 4\ [9]$$

Equation 4 [8] is satisfied if

$$\sum_{n=-\infty}^{\infty} Q(f+nfs) = \frac{A}{fs} \qquad 4\ [10]$$

Band limited functions which satisfy the Niquest 1 criterion can be constructed from 4 [10].

The narrowest band is given by:

$$q(t) = A\,\frac{\sin \pi ft}{\pi ft} \qquad 4\ [11]$$

There is no intersymbol interference when the signalling rate is f_s at the samples are taken at multiples of $\frac{1}{fs}$. The band required is exactly the range from $\frac{-fs}{2}$ to $\frac{fs}{2}$ which means that no frequencies of absolute values exceeding half the signalling rate are needed.

The bad feature of this approach is the slow rate of decay of $\frac{\sin \pi ft}{\pi ft}$. One effect is that there is no margin for error in sampling times. The intersymbol interference denoted by I will tend to infinity as the number of symbols, N, tends to infinity when a finite error, ε, exists in the sampling time of a train of pulses which are all one's.

It could be argued that the sequence which produces catastrophic interference is very unlikely, and that therefore there need be only a small error rate in the receiving rate when the amount of synchronising error is small. In fact, the worst case may enjoy a higher probability of occurrence because of its particular pattern.

The minimum bandwidth solution can be made more practicable by extending the bandwidth to between $\frac{fs}{2}$ and fs. This eliminates the very slow roll off of q(t) and provides an allowable margin of error in smapling time.

Niquests's first method of overcoming the effects of intersymbol interference depends on sampling a received signal wave at the mid point of the signalling intervals. The is particularly suitable for accurate recognition of the symbols. When precision synchronisation is not possible, the transition between unlike symbols in the received wave are used. Accurate timing information is not necessary since the number of like symbols in sequence is given by the nearest whole number of symbol intervals in the time between adjacent transitions, giving the Niquest 2 method.

Ideally the transition should occur at the edges of the symbol intervals. Again, the minimum bandwidth solution is $\frac{-fs}{2}$ to $\frac{fs}{2}$ and the corresponding pulse is:

$$q(t) = \frac{2A \cos \pi fst}{\pi(1-4fs^2t^2)} \qquad 4\ [12]$$

This case has the peculiarity that any alternating train of pulses produces no output. Hence the lack of output can be interpreted as a train of reversals. Again the Niquest 2 is more easily realised by extending the bandwidth beyond $\frac{fs}{2}$. At twice the minimum bandwidth the correct timing and transition can be achieved using a 100% cosine roll off function.

4.3.2. EFFECTS OF NOISE ON SERIAL TRANSMISSION

The effects of intersymbol interference can be controlled to prevent confusion of successive symbols in a noise-free environment. The bi-polar digital signal with independent, equally likely choices between +A and -A in each signal interval is optimum among binary systems with respect to minimum probability of error in transmission. Amongst these systems is the alternate mark inversion (AMI). Considerations such as simplicity of terminal apparatus may lead to a choice of system which is sub-optimum from the standpoint of error rate. An example is simple on-off transmission which suffers a 3dB penalty in signal to noise ratio when the noise is white.

The reliability of the serial approach then suffers because of intersymbol interference and noise. The former can be controlled by suitable filters in the send and receive paths which do however add to the time response of the system, the more idealised the circuit, the longer the filter delay, otherwise the output response woould have to anticipate the input. Assuming the channel can be made error free from intersymbol interference, the channel is still susceptible to symbol interference due to extraneous electrical disturbances. and to thermal noise, the latter placing the ultimate limitations on the channel performance and the former can in theory be avoided by suitable shielding and isolation.

4.3.3. SERIALISATION APPLIED TO THE TERMINAL

Section 4.1. deals with the requirements of the data link in terms of the amount of data that has to be transmitted. The bi-directional requirement would require two or more serial lines. In the forward direction from the computer to the terminal the E-bus, six control lines and allowing eight additional lines for ancillary purposes, requires the transmission of thrity bits of information. In the return direction the E-bus return, four control lines, the eight interrupt lines and several lines for ancillary purposes are needed, requiring more than thirty bits of information to be transmitted.

The information to be transmitted in either direction is in blocks such as the E-bus. Because of the length of a thirty-bit string of data, synchronisation using the Niquest 1 criterion of correct sampling at the centre of each symbol introduces a high probability of intersymbol error. Niquest 2 provides a practical solution by placing a start-stop pulse at each end of the different blocks of data transmitted. In this manner parity chacking on each block in the serial string is possible, and the number of bits of data for transmission of all the data at either the computer or the terminal reaching forty.

The limitation placed on serial systems is the time required to convert from parallel to serial and then back to parallel. The rate at which this can be achieved is limited by the components available.

Bearing in mind that the logic at the input-output structure is TTL or compatible logic, a forty-bit register capable of parallel loading and serial shift at the sending end, and a forty-bit register capable of serial loading and parallel output at the receiving end would be necessary. Section 4.2 stated that any delay beyond that of the transmission delay was undesirable. The fastest means of implementing theconversion using TTL logic would be the use of Schottky TTL with J-K flip flops as elements in the shift registers. A clock speed of 70 MHz could be achieved with this approach, requiring more than 0,5 microseconds for encoding and the same period for decoding. The use of ECL could further increase this speed by a factor of 1,5. TTL to ECL 10 000 series converters could be employed to convert the logic to that compatible with a forty-bit ECL register which is clocked onto line. The high speed application is limited however by the components available for transmitting and receiving. Isolation is limited to systems operating at speeds at less than 20 MHz. The use of such a system results in a prohibitively large delay. The high speed application requires direct coupled transmission which is discussed in a further section.

A method of improving system performance is to have more than one serial line transmitting in one direction. Blocks of data are then divided amongst the lines. The rate of data transfer is proportional to the number of lines used. In such a system the number of lines would be a compromise between operating speed and economic considerations.

4.4. PARALLEL TRANSMISSION

In the case of the serial transmission system, a major problem is synchronising the encoding and decoding of the data. Special filter techniques are necessary to optimise the system so that any error in the sampling frequency at the receiver would not result in erroneous data. Data in the format of the input-output structure does not lend itself to serial transmission, particularly as data transfers in both directions is necessary. The serial to parallel and parallel to serial conversion required time and resulted in a derating of system speed. A solution to this problem is to have several of these lines in parallel reducing both the time required for encoding and decoding, and the length of the date word sent on each line, reducing the probability of error due to sampling frequency error.

A logical extension of the multiple serial line is parallel transmission. No conversion is involved and assuming all the channels in the parallel system to have similar charactersitics, time skewing between lines is avoided and the approach does not suffer from any inherent flaws. At the speed at which data transfers take place in the input-output structure, data transmission line components employing isolation or direct coupling are readily available in high density integrated circuit form.
A particularly attractive asset of the parallel system applied to the terminal is that it conveys the real time information content of the data. Serialisation loses this, requiring circuits at each end of the line for reconstruction of the timing sequences. The effect on this of the interrupt lines, for example, with their priority chain structure, is difficult to guage.

The parallel system does require a large cable with many driving and receiving elements, but the less stringent specifications placed on these components can offset any economic disadvantages. Using the specification described earlier for a simple economical system, a terminal was investigated using the parallel approach.

4.5. CROSSTALK

When currents or voltages are impressed on a line in a system, static and magnitic fields interact to affect adjacent lines. This cross-coupling effect is known as crosstalk.

Signal lines are grouped into three categories, coaxial lines, twisted pair lines, and straightwire lines. Because of the low impedance and shielding characteristics of coaxial cable, crosstalk on this form of line is minimal with normal levels of transmission, and does not present a problem. Figure 4.2 is a simplified but adequate description of practical types of transmission lines. The mutual reactances L_m and C_m form the noise coupling paths and the L_s and C_s determine the characteristic impedance of the line.

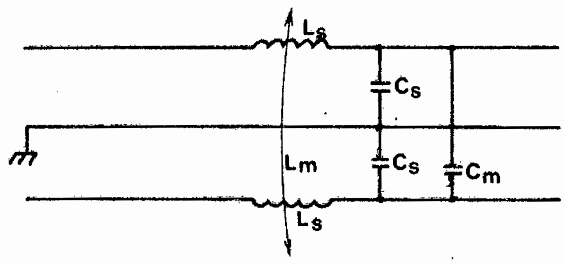


FIGURE 4.2.

Crosstalk is a function of the ratio of the mutual impedance to the characteristic impedance of the line [12]. The analysis of coupling in most practical systems is complex and the results doubtful because of the boundary conditions of the problem. Over long distance transmission, techniques such as coaxial cable and balanced lines which avoid crosstalk are used. Crosstalk is investigated using measuring apparatus on site.

4.6. GROUNDING [1, 7]

Grounding is generally concerned with providing a low impedance reference path to which signal and power voltages may be established. The objective is to prevent any electromagnetic interference generated at one point of a system from being transmitted through a common ground impedance to other units. In serial transmission in high frequency circuitry, if one of the conductors is connected to ground directly, or through an impedance, and if both circuits connected by the signal path are connected to their DC power supply grounds, a ground loop is formed into which low frequency current can be induced by electromagnetic flux linkages from external sources. This is particularly true of the working environment where most electrical apparatus results in considerable flux leakage from the mains supply. Even if this does not affect the high frequency circuitry, the loop can transfer this interference energy to another susceptible circuit. If this loop is unavoidable, in practice the area enclosed by the loop is kept to a minimum to reduce coupling. Several techniques exist for overcoming earth problems. Basically, these either remove the loop or break the elctrical continuity of the loop or ignore the effects of the loop.

[1] Inductive coupling. Transformers are used to inductively couple the line to the circuitry at either end. Section 4.7.1. deals with the transformer coupling.

[2] Optical coupling. Optical coupled elements are usually placed at an end of a cable, eliminating the loop. Techniques are described in section 4.7.2.

[3] A third technique uses layout methods. For several pieces of apparatus that are connected together, a common earth point is used removing any common ground impedance. Applied to the transmission problem this amounts to extending the point to be grounded of one end of the line to the opposite end and grounding it there. This removes any common ground impedance but earth loops are formed, and special cabling techniques will be necessary to avoid the effects of this. Further points detracting from this approach are the stray capacitance at the "floating" end could couple that end to the local ground and there is no guarantee that the user will not ground the floating side through a piece of equipment connected to the terminal system.

The techniques described above either eliminate the ground loop or try to overcome common ground impedance problems. A transmission technique that effectively ignores the effect of ground problems is to use a balanced line transmission. An unbalanced system is defined as one in which two conductors present different impedances with respect to ground (usually one of the conductors is at ground potential). The capacitance with respect to ground of the individual conductors is then different and consequently the current in the two conductors may be different. In contrast, a balanced system is one in which the two conductors present the same impedance to ground and in general the two conductors are equally above and below ground potential. Figure 4.3 illustrates this approach. Current flowing in the loop formed by the signal cable and the ground will induce voltage across the balanced pair. If these conductors are perfectly balanced, the common mode voltages thus induced on the leads will separately produce equal and opposite effects in the receiver, hence they cancel. Section 4.8. deals with this in detail.

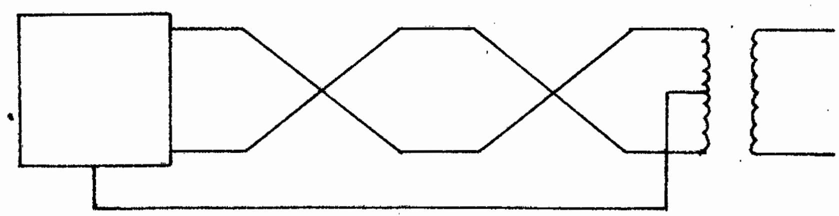


FIGURE 4.3. BALANCED LINE TRANSMISSION

4.7. ISOLATION

There are three forms of isolation, electromagnetic (with a transformer), electromagnetic (with a RF link) and optical isolation. A radio frequency link, while avoiding the use of cabling, is an over-elaboration of the problem and violates the ideal of simplicity and is not considered.

4.7.1. ISOLATION USING PULSE TRANSFORMERS [1,2,3,4,8,9]

In general there are two types of transformers, namely, ordinary transformers according to Faraday's laws or induced voltage, and the transmission line type of transformer. For very high frequency applications, the ordinary transformer fails for several reasons. In the first place, materials which are suitable for high frequencies, that is ferrites, have permeabilities which generally fall off rapidly above several MHz, resulting in a loss of coupling between primary and secondary windings. In addition, stray capacitance and leakage inductance of the windings create several problems which cannot easily be circumvented. This unwanted capacitance and inductance will have resonant points which drastically affect the frequency response of the device. The transmission line type of transformer absorbs the unavoidable stray inductance and capacitance into the characteristic impedance of the line, avoiding resonance and providing a broad band device.

In the transmission line type device the aim is to provide a broad band device, capable of impedance transformation, and is not intended as an isolation device. [1] Used as a coupling device in a long transmission line, it will result in a loop susceptible to mains flux. The normal type of transformer, then, is the only means of electromagnetic coupling with its relatively low frequency response.

The transformer eliminates the DC component and special coding of the transmitted signal is required. One means of overcoming this is to use alternate mark inversion. Figure 4.4. shows the implementation of a bi-directional transmission line using a ferrite H10 core (Philips) and capable of transmitting data at a rate of 20 MHz. The alternate mark inversion represents logic one's by current flow in either direction, and each successive one is indicated by reversal of current. One advantage of this sort of transmission is that it facilitates transmission error detection. A centre tap on the transformer offers a convenient method of implementing the bipolar format with the single transformer coupling both send and receive circuits to the transmission line. Both send and receive circuits use transistors in an emitted couple configuration, preventing saturation. A monolithic transistor array package such as CA3045 is used in the receive circuitry to minimise the number of components.

When the signal at the base of Q1 or Q2 is below threshold, a current through Q3 results, placing a logic 0 at the input to the TTL inverter. When a logic one is received, the base of Q1 or Q2 (depending on polarity) goes more positive than the threshold voltage set at Q3.

In the send circuitry the current through R2 flows through Q6 to ground in the non transmitting stage. To transmit pulses, input lines feeding Q4 and Q5 alternatively go negative. Thus current through R2 is diverted through Q4 and Q5 and into alternate sides of the transformer. The circuit shown in figure 4.5. can be used to achieve AMI.

Because of the large number of discrete components needed, the use

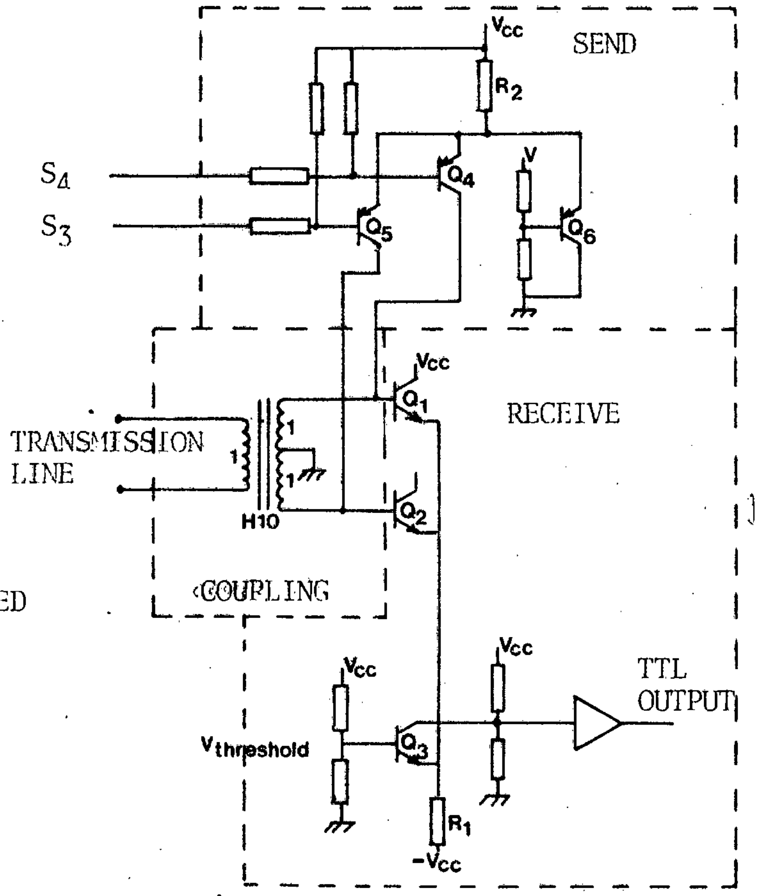


FIGURE 4.4.

TRANAFORMER COUPLED
TRANSMISSION LINE

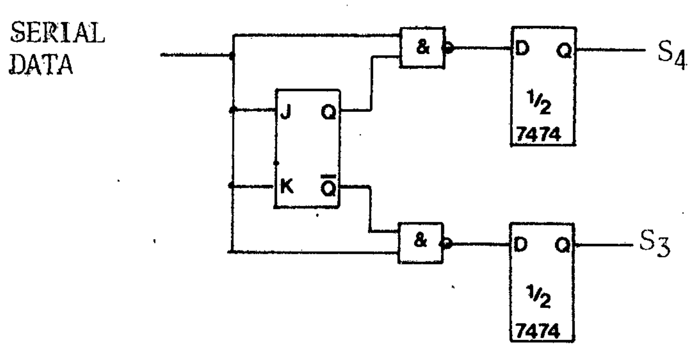


FIGURE 4.5.

BIPOLAR CODING.

of this line in the link would be restricted to a serial system. The number of components on the send side could be reduced by using elements such as the HD 245 transmitters shown in Figure 4.6. This element contains three transmitters in one 14-pin package. If the receive circuitry is to maintain high speed, the use of discrete elements is still necessary.

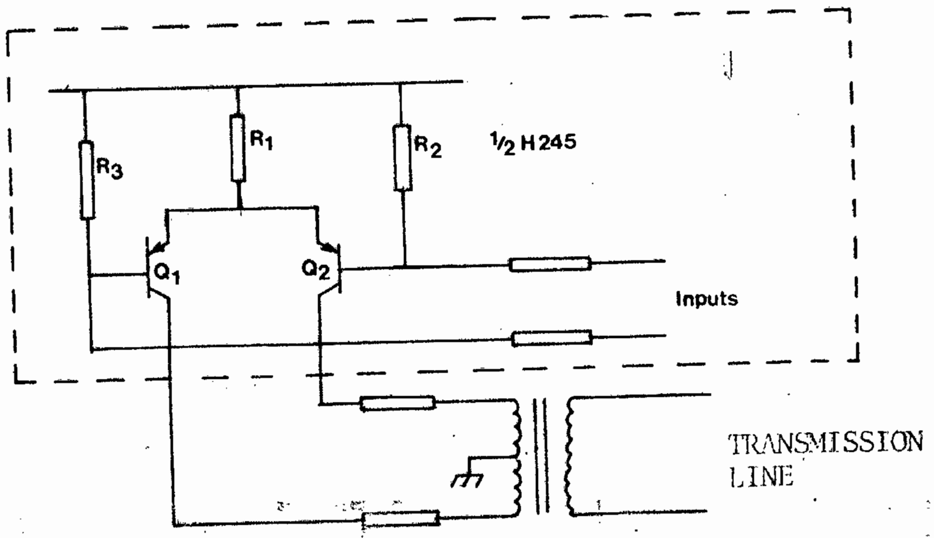


FIGURE 4.6.

A further problem is that of transient response if the signal is to be transmitted or received without pulse distortion. A digital signal consisting of pulses has an infinite Fourier spectrum with the amplitude of the spectrum decreasing for high frequencies. Since the signal has an irregular duty cycle, in order to transmit the signal without deteriorating the frequency envelope, the response of the system must be that of a second-order system with critical damping. [4]

To achieve this the capacitors and resistors shown in figure 4.7. are necessary, the capacitor acting as a fast energy transfer medium.

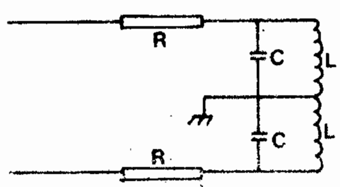


FIGURE 4.7.

The Kirchoffs closed loop equation becomes

$$E_0 = iR_1 + \frac{Ldi}{dt} + \frac{1}{c}\int idt \qquad [4.13]$$

where E_0 is the applied voltage, and L is the equivalent inductance of the transformer. Differentiating with respect to time:

$$0 = \frac{Ld^2i}{dt^2} + R\frac{di}{dt} + \frac{i}{C} \qquad [4.14]$$

The solution is of the form:

$$i(t) = A_1e^{P_1t} + A_2e^{P_2t} \qquad [4.15]$$

where A_1 and A_2 are arbitrary constants, and P_1 and P_2 are roots of the equation:

$$LP^2 + R_1P + \frac{1}{C} = 0 \qquad [4.16]$$

yielding:

$$P_1 = -\frac{R_1}{2L} + \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}} \qquad [4.17]$$

and

$$P_2 = -\frac{R_1}{2L} - \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}} \qquad [4.18]$$

and is of the form

$$P_1 = -a + \sqrt{a^2 - w_o^2} \qquad [4.19]$$

$$P_2 = -a - \sqrt{a^2 - w_o^2} \qquad [4.20]$$

This results in the three solutions:

[1] The overdamped case $a^2 > w^2$, then P_1 and P_2 are real and negative.
[2] The underdamped case $a^2 < w^2$, then P_1 and P_2 are complex.
[3] The critically damped case $a^2 = w^2$, and $P_1 = P_2 = -a$.

Thus w_o and a determine the damping factor and these two elements are determined by R, L and C. Since L is fixed by the transformer, the variables are R and C.

To summarise, the use of transformer coupling provides a practical means of overcoming earthing problems but is limited in frequency response to tens of MHz, and is wasteful of components. As a serial transmission element, this form of transmission is ideal but the limited frequency response would place serious limitations on the terminal system. A compromise in this area would be the serial transmission of data along several lines, the number of lines required being a trade off between operating speed and system complexity. Using several lines will also serve to reduce the length of the blocks of data to be transferred, decreasing the probability of sampling errors.

4.7.2. OPTICAL COUPLING [4,5]

Optical coupled isolation consists of transferring the electrical signals from one circuit to another via a stream of photons. In figure 4.8. it is seen that the input side of the isolator consists merely of a forward biased gallium arsenide diode which emits infra red light with an intensity which is controlled by the forward biased current.

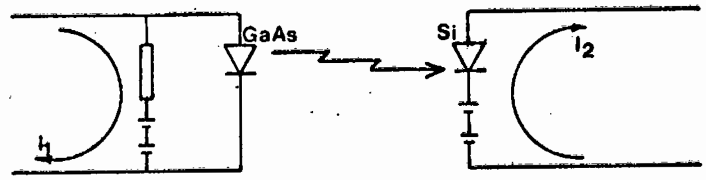


FIGURE 4.8.

The output side consisting of a silicon PIN photodiode which responds efficiently to this infra red wavelength. While the forward current in the gallium arsenide diode produces radiation which the silicon photodiode can detect, the reverse cannot happen, and therefore, the signal transfer is in one direction only.

The photodiode coupled pair will have a top frequency of approximately 10 MHz with a rise and fall time of 5 nanoseconds. The phototransistor coupled pair will have a bandwidth of less than 1 MHz with a rise and fall time measured in microseconds, and is only suitable for use in low frequency applications.

The circuit shown in Figure 4.9.a. was developed by Hewlett-Packard and is one of the faster optical coupled circuits available. The bandwidth is in the region of 10 MHz and Figure 4.9.b. shows the response to a pulse. This limitation on bandwidth makes optical coupling unsuitable even for parallel transmission in the terminal system and is applicable only in a severe industrial environment when the degree of isolation offered by these devices is required.

4.8. DIRECT COUPLED BALANCED LINE TRANSMISSION [13,14,15,16]

In data transmission applications there are several digital communication systems available. Low and moderate speed digital systems are defined by the EIA standard, RS 232. This type of system is intended for local (less than 100 feet) communications with peripheral devices. For very high speed data applications, coaxial and microwave systems are used for long distance transmission. Another general class of digital communications is high speed transmission over distances of up to several thousand feet, and it is the direct coupled balanced line that comes into its own here. This is because, although data rates up to 10 MHz using the standard TTL can be achieved, the transmission distance must be very short. For example, a fifty foot low capacitance cable will have a capacitance of approximately 750 pf which requires a current of greater than 50 mA to drive 5 volts into this cable. Therefore voltage mode transmitters are undesirable for long transmission lines at high data rates due to the large current required to charge the transmission line capacitance. An

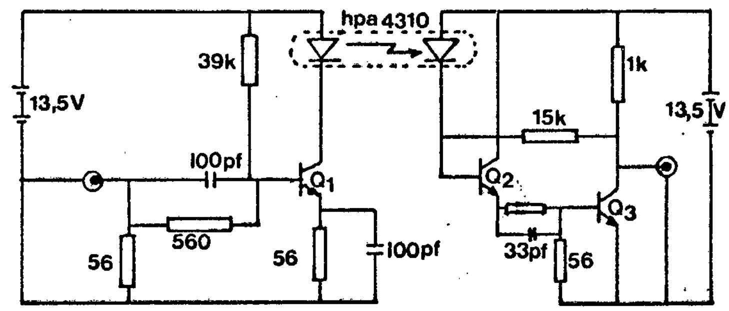
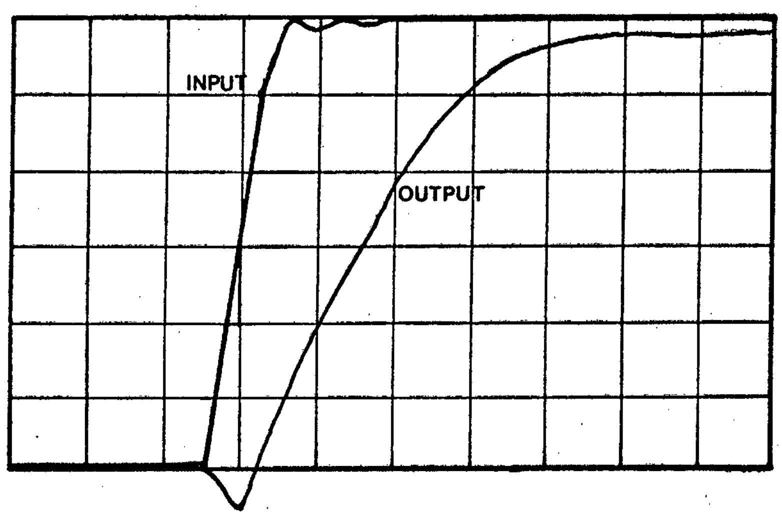


FIGURE 4.9.a

FIGURE 4.9.b



20nS/DIV

RISE TIME 60 NANOSECONDS

alternative method for driving high data rates down long transmission lines is to use a current mode transmitter on a balanced line. Current mode logic changes the current in a transmission line and requires very little change in voltage. For example, a 2 mA change in current will result in a 100 mV change across a 50 ohm terminating impedance, independent of the line characteristics.

4.8.1. ECL AS A TRANSMITTER DEVICE [14]

The complementary output of the emitter coupled logic family provides a natural twisted pair line driver. Any of the MC 10 000 series gates would provide a suitable transmitter with up to four transmitters available on a single chip. The MC 10115 or 10116 are special quad and triple line receivers respectively requiring little input current and suitable for use on lines with low capacitance up to several hundreds of metres in length. Figures 4.10.a. and 4.10.b. show different configurations.

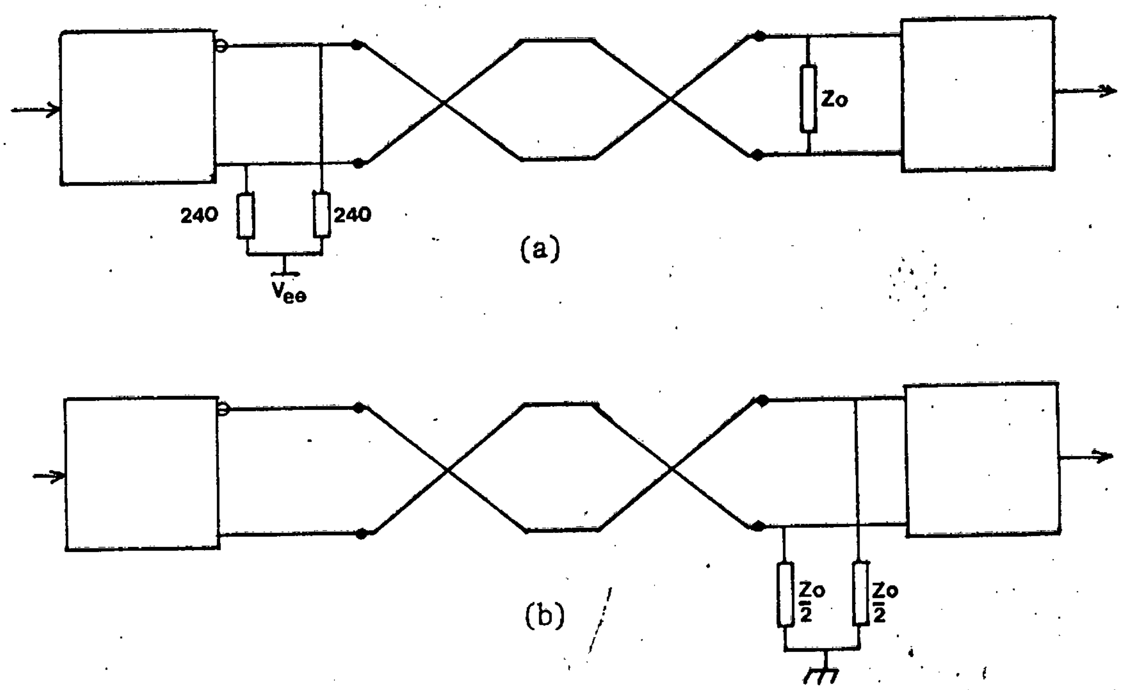


FIGURE 4.10.

Because of the high component density, ECL is particularly suitable for parallel transmission but several factors detract from this.

[1] The high edge speeds (typical rise time is 4 nanosecs). Special layout techniques are required for the component board, and the individual cable pairs require screening which is economically unattractive.

[2] The voltage requirements are v_{ee} = - 5,2 and v_{cc} = 2,2 and are not available from the Varian supply.

[3] The non saturating ECL logic requires a relatively large and constant supply current.

While providing a very high speed link, ECL, in the face of similar compatible TTL logic, is not the optimum choice for the terminal.

4.8.2. TTL BALANCED LINE DRIVING AND RECEIVING [14.15]

There are several compatible TTL line drivers and receivers such as the Harris HT 245/545 and HD 248/548, the SN 75 100L dual receiver and then the SN 75 107/8 dual line receiver and SN 75 109/10 dual lone driver. Using voltage supply requirements, receiver sensitivity and transmitter flexibility as criteria, the driver/receiver pair were chosen.

SN 75 109/10 line drivers. These integrated circuits are dual line drivers with independent channels and common voltage and ground terminals. The driver circuits feature a constant current output that is switched to either of the two output terminals by the appropriate logic levels at the input terminals. The output current can be inhibited by appropriate logic levels at the inhibit inputs. The output constant current is 6 mA for the SN 75 109 and 12 mA for the SN 75 110. The driver outputs have a common mode voltage range of -3 volts to +10 volts, allowing common mode voltage on the line without affecting driver performance. Appendix 3 contains data extracted from [15].

SN 75 107/8 line receivers. The dual line receivers have two independent channels per chip with common voltage supplies.

The SN 75 107 has a totem pole output and the SN 75 108 has an open collector output for dot ORing. The receiver circuits are able to detect signals of 25 mV or greater across the input terminals and converts the polarity of the signal into appropriate TTL compatible output logic levels. The input receiver common mode voltage range is ± 3 volts.

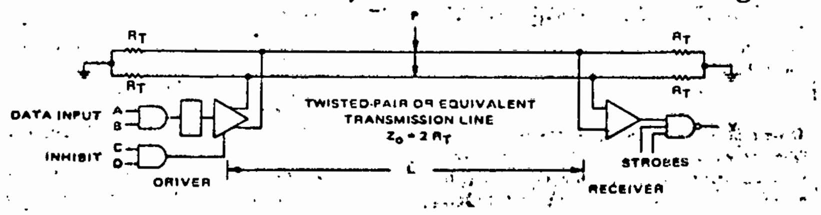
4.8.3. APPLICATION

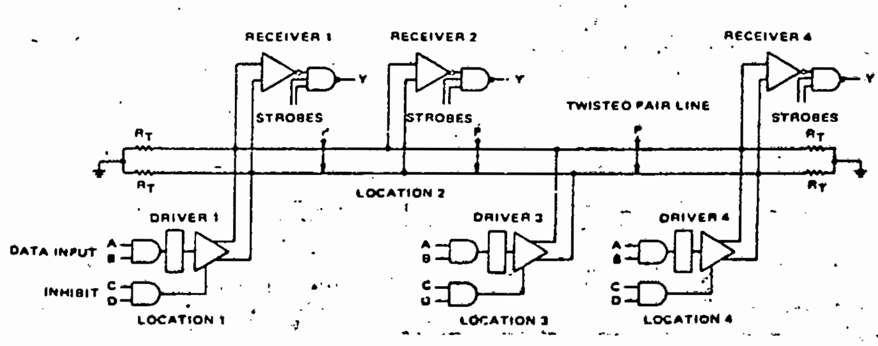
Firgure 4.11.a. is a typical application of the driver/receiver elements. The transmitter alternately applies the current to each of the two conductors in the twisted pair line such that the total current is constant and always in the same direction. This current flows through either of the terminating impedances and returns to the transmitter as a steady state DC current via the earth. The differential signal amplitude at the receiver is given by:

$$V_{diff} = I.R_T \qquad [4.21]$$

Using conventional twisted pair wire with a typical characteristic impedance of 120 ohms, hence R_T is 60 ohms, then the SN 75 110 produces a V_{diff} of approximately 360 mV. The receiver requires 25 mV differentailly to determine the output state. Thus a noise margin of better than 300 mV exists to account for any differential noise entering on to the paired line due to slight imbalance.

The high input impedance, requiring less than 75 microamps allows the data bus system as shown in Figure 4.11.b.





4.9. TRIAL TRANSMISSION SYSTEM

To asses the driving and receiving elements and to evaluate the cable used, a trial system was constructed.

4.9.1. CHOICE OF CABLE

The only cable commercially available was post office cross-connection wire which has approximately one twist per centimetre. The DC resistance over a distance of 100 metres is 10 ohms. To assess the characteristic impedance, the measuring circuit in Figure 4.12. was used. Using the fact that:

$$Z_o = \frac{Zoc}{Zsc}$$

where Zoc is the open circuit impedance and Zsc is the short circuit impedance, the sweep generator feeds a constant current drive through the tracking generator. Since the line is fed with a constant current drive, the voltage across it is a direct reading of the impedance looking into the line. The tracking generator sweeps the X-axis of the oscilloscope and applies the voltage to the Y amplifier. In this way a trace of Zoc and Zsc were obtained. From measured points, the characteristic impedance as a function of frequency was calculated and is shown in Figure 4.13.

Wile the results indicated varying characteristic impedance, a short circuit and open circuit are hard to define at 30 MHz and the geometric mean of 120 ohms is generally taken as the characteristic impedance.

Tests were performed on the custom built lines to assess the effects of varying twists per centimetre and also the effect of the gauge of the line. Figure 4.14. shows the effects of twists per cm. on the characteristic impedance. This effect is small. To assess the effect of the different gauges, using the same apparatus, the different lines were terminated in a 120-ohm resistor and the voltage attenuation at 10 MHz noted. The two lines tested were 30-gauge wirewrap wire and the conventional 24-gauge Post Office cross-connection wire. The attenuation is listed in Table 4.1.

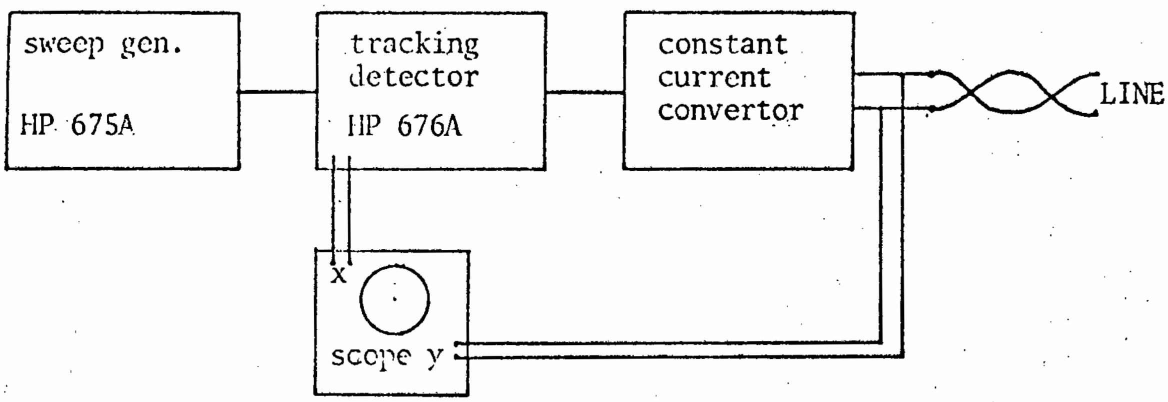


FIGURE 4.12.

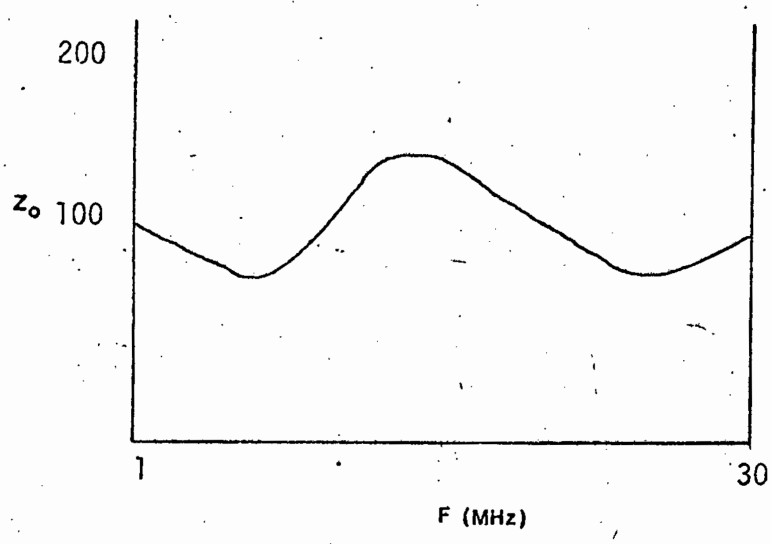


FIGURE 4.13.

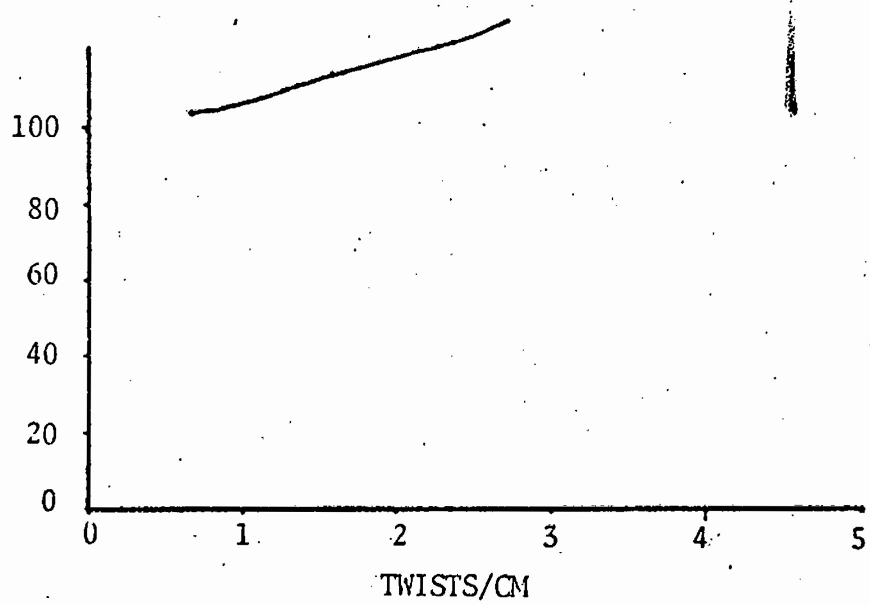


FIGURE 4.14.

	PO CABLE	30# CABLE
ATTENUATION	1dB	12dB

TABLE 4.1.

The results show that while twists per cm. do not affect the characteristic impedance to any extent, the increasing resistance with increasing gauge drastically affects the attenuation. Assuming each of the lines to be attenuated in 60 ohms to ground and using the SN 75 110 as the driver element, as shown in Figure 4.11.a., the amount of attenuation noted is 24 dB. Electrically the Post Office cross-connection wire is seen to be more than adequate and is the cheapest and most readily available cable. A 40-pair 200 metre cable was made up for the terminal after the results obtained on the trial line.

4.9.2. THE TRIAL LINE

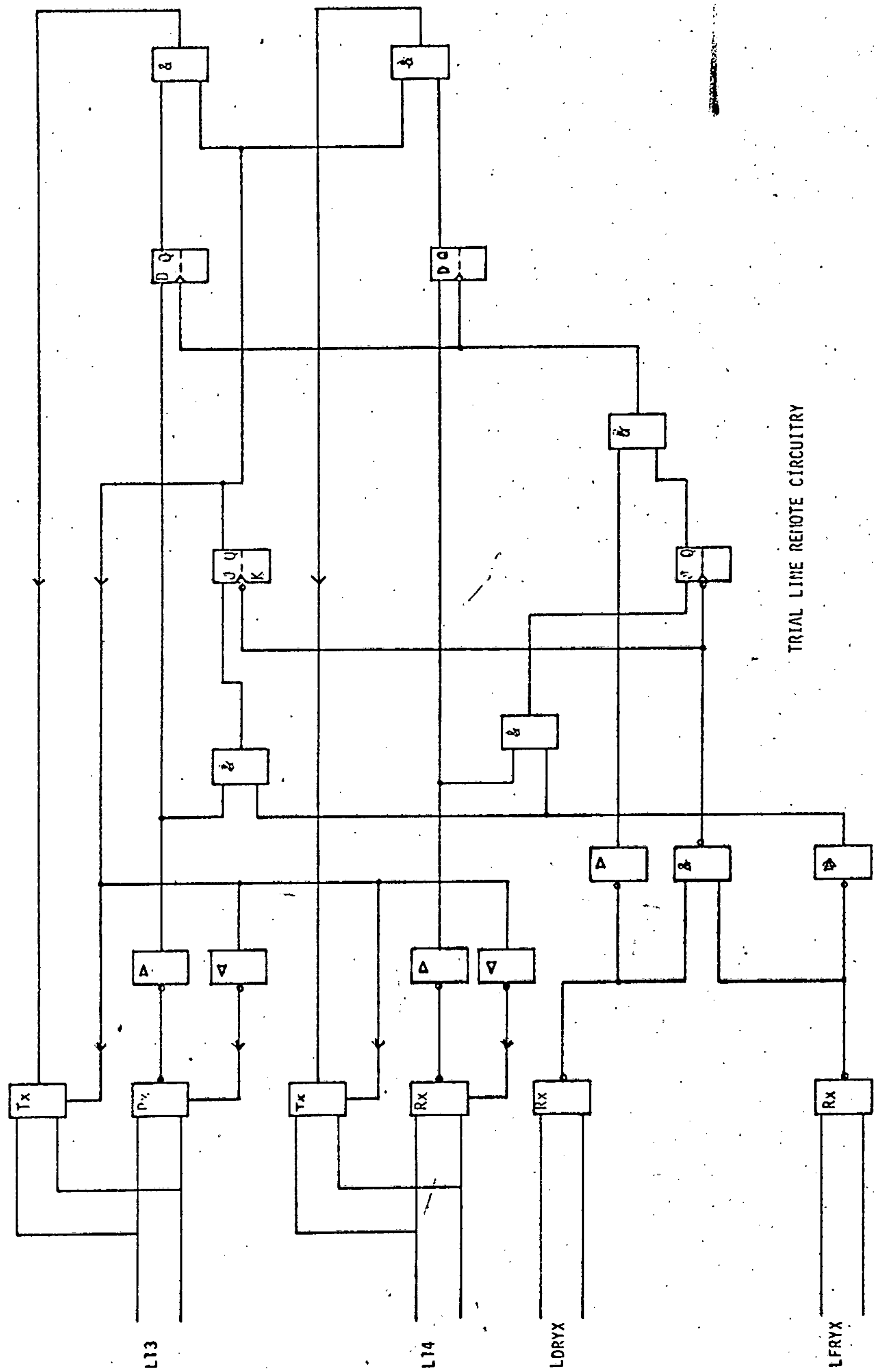
The trial line achieved three purposes. To select either 56 ohms or 62 ohms as the terminating impedance to ground, to test the application of the transmission system to the terminal problem and finally to generate know-how.

The trial system consisted of four pair of 200 metre cable with two of the pairs operating as bi-directional transmission lines and the other two pairs unidirectional transmission lines. Connected to the computer input-output structure, the system was able to transmit two bits of data from EB 13 and EB 14 and store these bits at the remote point under the control of the data-out instruction. A data-in instruction then returned these two bits of information to the computer. Figures 4.15. and 4.16. show the circuitry involved. The programme associated with information transfer was:

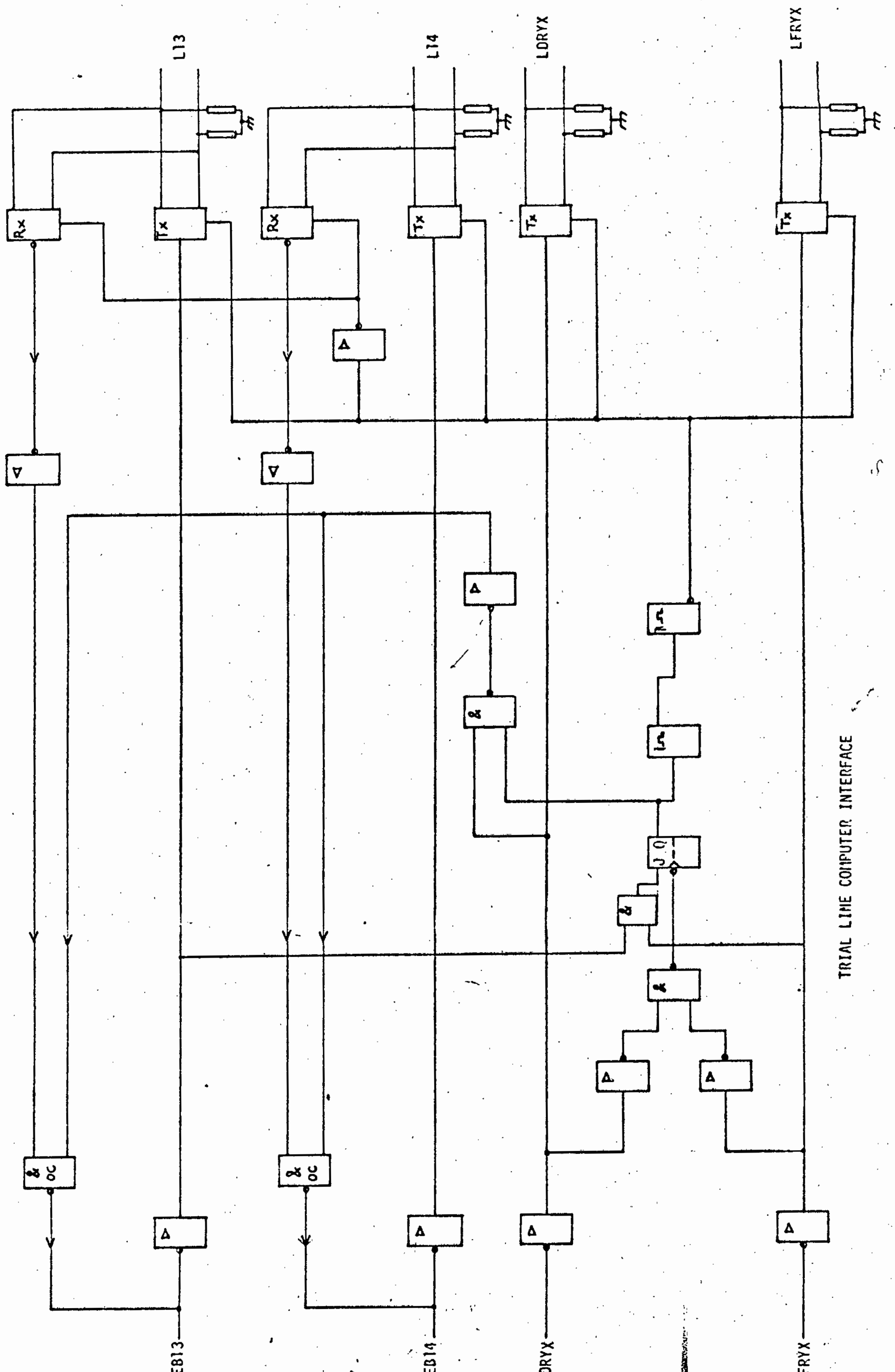
LABEL FIELD	MNEMONIC	VARIABLE FIELD
J1	OAR	00
	NOP	
	NOP	
	CIA	00
	JMP	J1

Bits 13 and 14 of the A register were circulated between the remote end of the line while the different lines were tested with an oscilloscope. With the 56 ohm terminating impedance, a negative reflection resulted, indicating that the terminating

FIGURE 4.15



TRIAL LINE REMOTE CIRCUITRY



TRIAL LINE COMPUTER INTERFACE

impedance is too low, as shown in Figure 4.17.

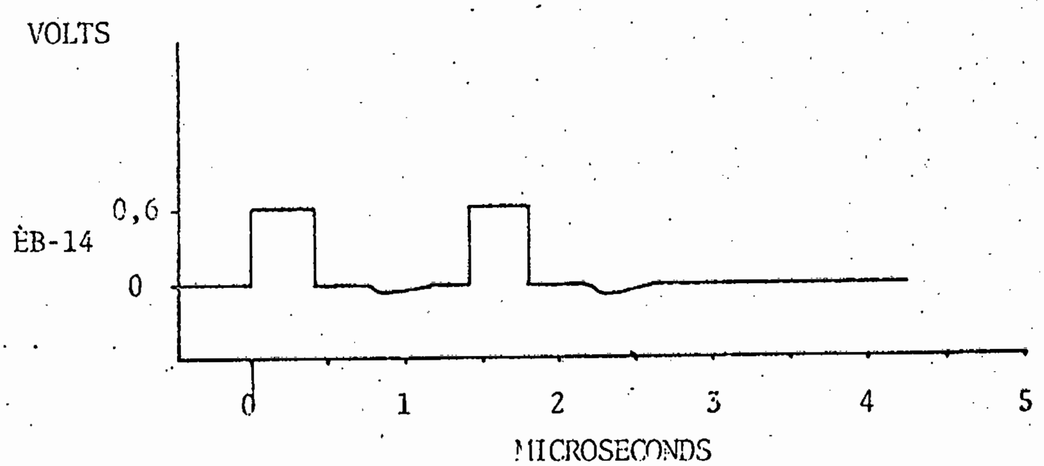


FIGURE 4.17 DIFFERENTIAL OUTPUT

4.9.3 RESULTS

[1] The terminating impedance is to be 62 ohms.

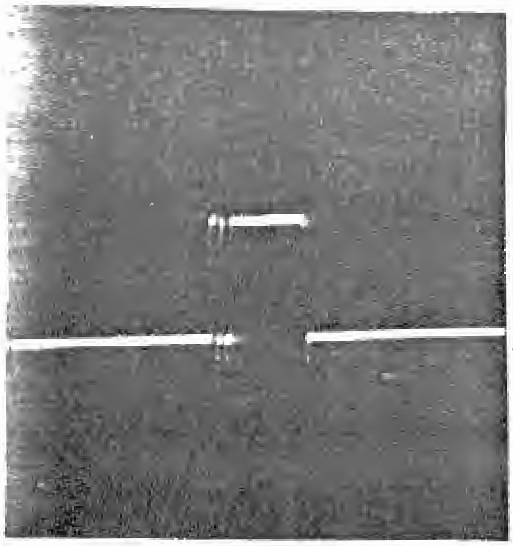
[2] An earth cable running with the signal cable reduced the loop size and the noise induced on the cable. Ideally, this earth would be a screen around the cable, but economics prevented this.

[3] Crosstalk from one pair to the other was negnigible. This is to be expected as the constant current switching between the two conductors of a pair results in the nett current flowing down the cable being constant with no reulting electromagnetic coupling to adjacent cables.

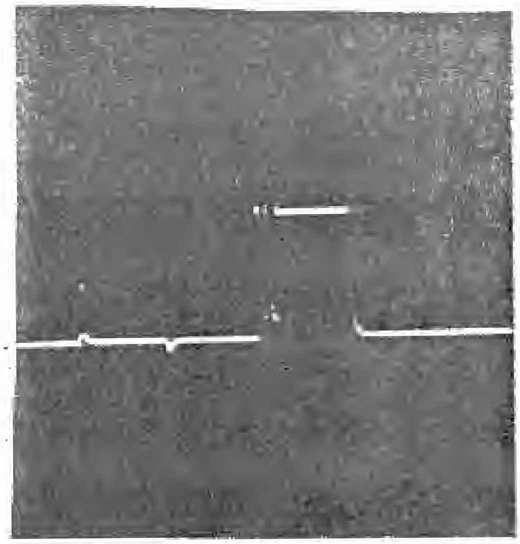
[4] A noisy environment was simulated by laying the cable around thyristor drives, induction motors and along electrical supply cables. This resulted in a negligible amount of differential voltage (quantitative measurement was beyond the sensitivity of the instruments available), and the common mode voltage noise was of the order of hundreds of mV, well within the 3V maximum common mode voltage of the receivers. This could result in component failure should large earth transience occur in an industrial environment. A massive transient on the earth at one end could result in a surge current propogating to the opposite end and resulting in excessive common mode voltage. Two techniques can be adopted

2V/DIV

0,5uS/DIV



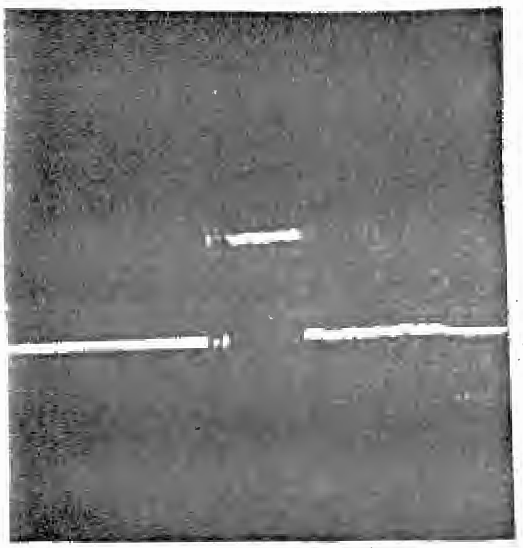
input to SN75110



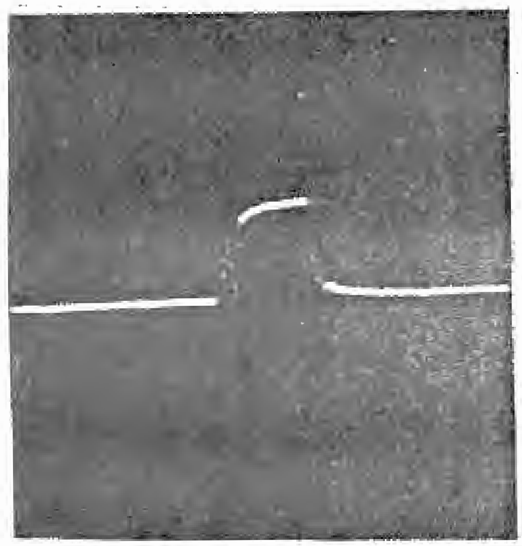
output of SN75107

0,2V/DIV

0,5uS/DIV



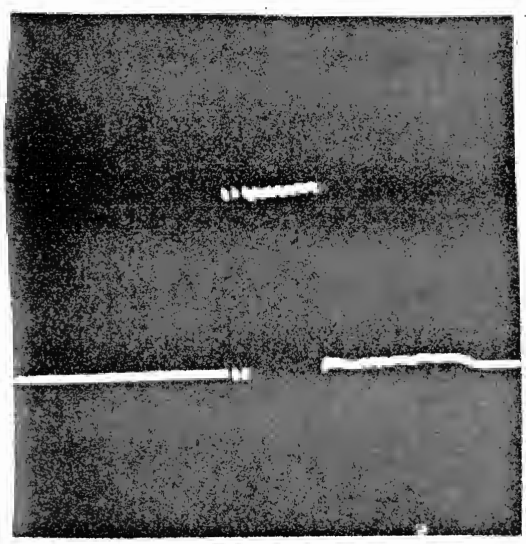
common mode output of
SN75110 driver



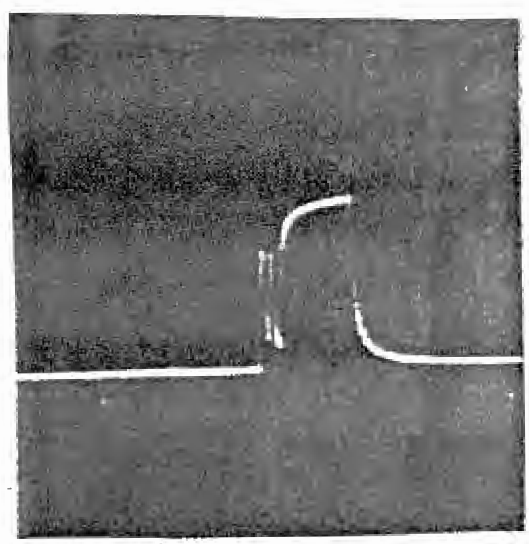
common mode input to
SN75107 receiver

0,2V/DIV

0,5uS/DIV



differential output of
SN75110 driver



differential input to
SN75107 receiver

FIGURE 4.18. TRANSMISSION LINE VOLTAGE WAVEFORMS.

to overcome this in an extreme environment.

(i) Clamping diodes can be employed to ensure that the voltage on the line at either end does not exceed the supply rails of ± 5 V.

(ii) A portion of each transmission line and the earth is wound araound a magnetic core to form a Balum transformer. Flux produced by the signal currents and the earth return cancel each ohher and the signal is not affected by the transformer. Ground currents produce a flux in the core and the current is reduced by the inductance and by the core losses.

Both these solutions are unwieldy and are dictated by a severe environment. The environment in which a terminal is to operate will normally be a moderate one. Should it become necessary to implement either (i) or (ii) then a look at transformer coupling, with its higher cost and complexity, would be justified.

[5] Standing waves created on lines that are open-circuited at one end can result in receiver destruction at the opposite end. This is a practical consideration which dictates tha manner in which the cable termination must be approached.

The method adopted was to provide a cable correctly terminated at each end with a heavy copper conductor linking the opposite earth points. The computer was hard-wired onto the one end of the cable while theterminal had access via a short cable to several points along the length of the cable.

Figure 4.18. shows the voltage wave forms at the input to the transmitter, the common mode voltage on the line and the differential voltage on the line at the transmitter, and at the receiving end and the output of the receiver. This series of traces was taken over a weekend when the ambient environment was free from electrical interference

* * *

CHAPTER 5 / THE TERMINAL

5

5.1. INTRODUCTION

Chapter 4 deals with the choice of transmission medium. The approach that would best meet the specifications was the parallel transmission of the input-output information with no attempt at encoding. The components to implement this were balanced line drivers and receivers, providing a bi-directional link with very good noise immunity. Chapter 5 deals with control circuitry required at the computer and at the terminal to control the transmission of data and the timing of operations needed to overcome the delay problem that was discussed in Chapter 3.

5.2. CONTROL CIRCUITRY AT THE COMPUTER

Chapter 3 dealt with the problem where a delay existed between placing information on a cable and receiving it at the output. This problem was overcome by inhibiting the computer clock. One function of the control circuitry at the computer is to control the inhibiting. Figure 5.1 is an algorithm of information processing necessary to allow for the transmission line delay.

5.2.1. SWITCHING OF THE E-BUS LINES

In all normal input-output operations, a peripheral device address and instruction identification information is placed on the E-bus during the first phase. In the terminal system, therefore, the E-bus line drivers and receivers are held so that information transfer is away from the computer, with the information appearing on the E-bus transmitted to the terminal end. Figures 5.2 and 5.3 show the circuitry involved with the transmitting and receiving of information on the E-bus. A logical low on line INBT disables the drivers, and a logical high on line ENLE enables the receivers. The open collector power drivers on the E-bus will simultaneously be enabled at the end of the first phase when it is a data-in

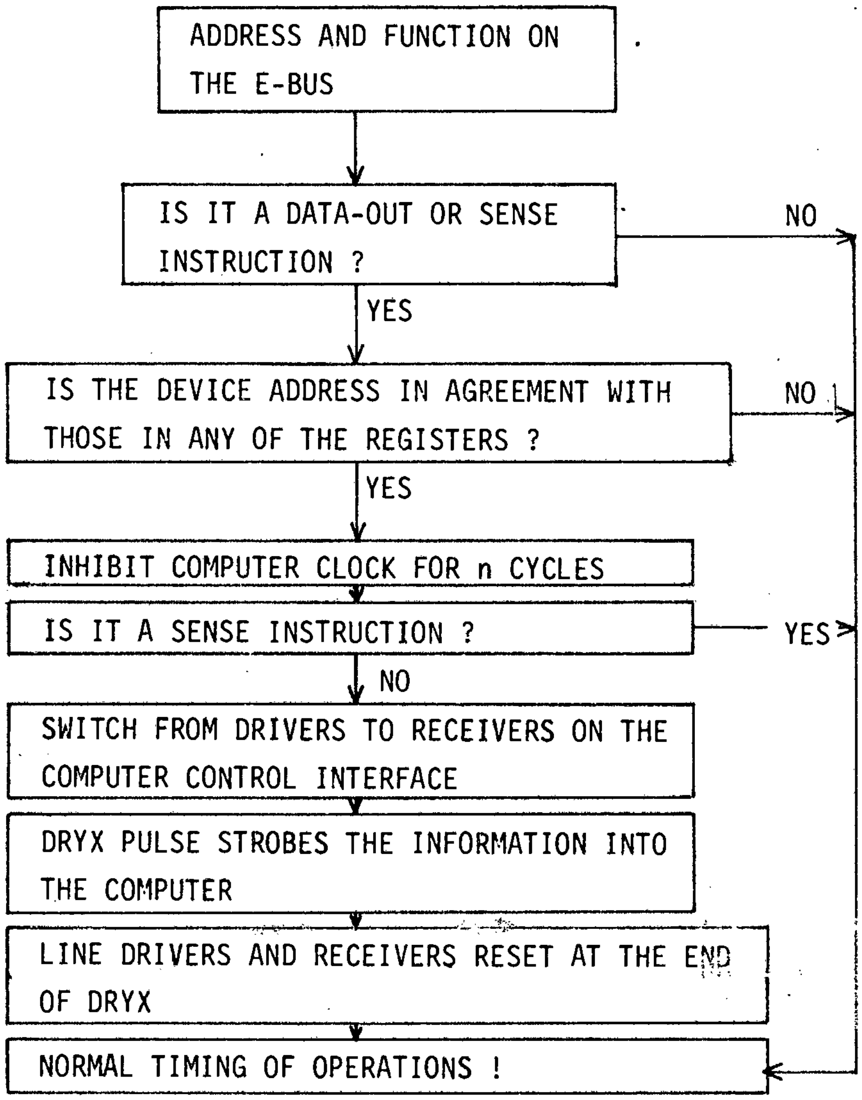
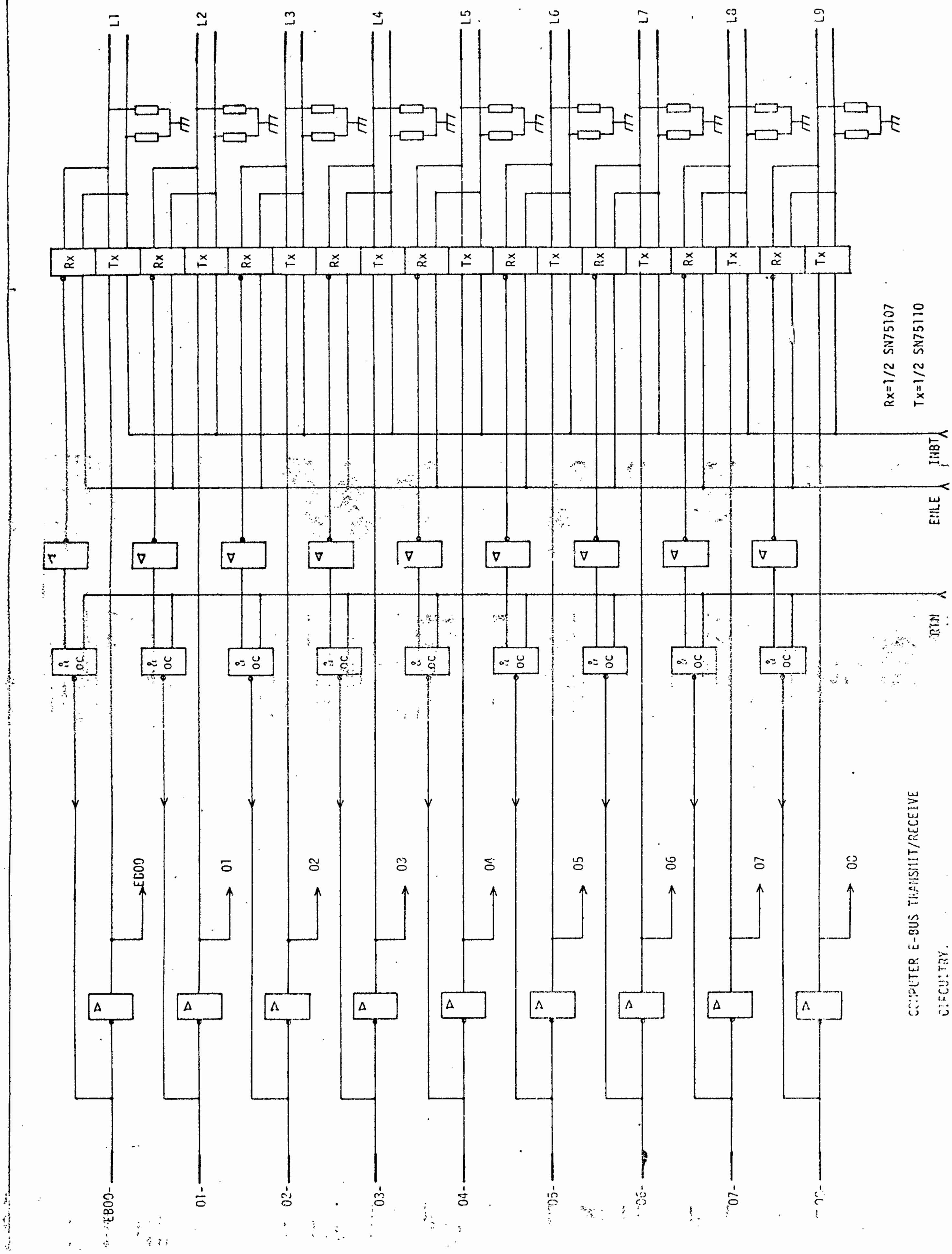


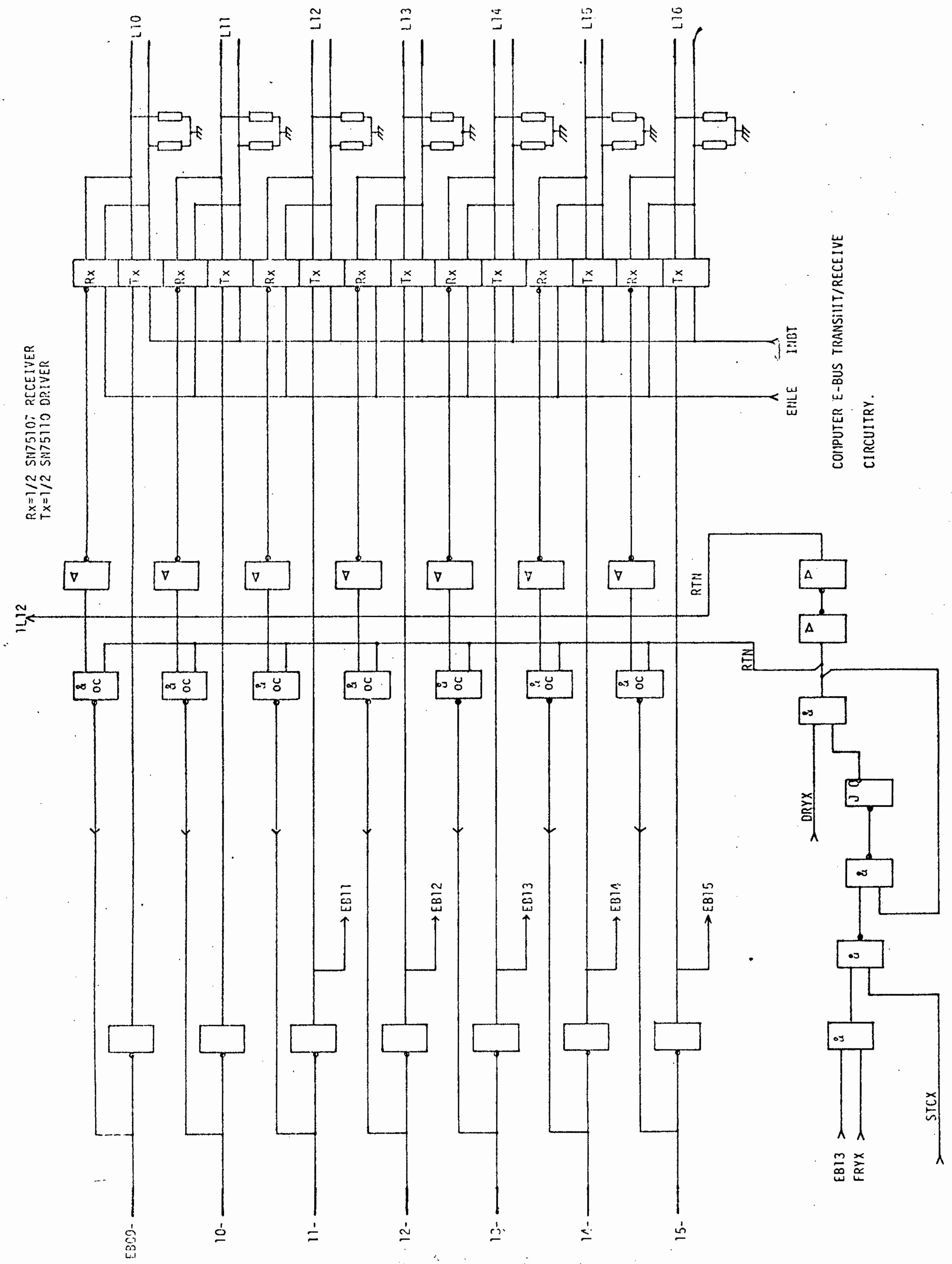
FIGURE 5.1. ALGORITHM OF INFORMATION FLOW

FIGURE 5.2.



COMPUTER E-BUS TRANSMIT/RECEIVE CIRCUITRY.

FIGURE 5.3.



COMPUTER E-BUS TRANSMIT/RECEIVE CIRCUITRY.

instruction. A pulse on the DRYX line will strobe the data that has been placed on the E-bus into the computer during the second phase. At the end of the second phase the drivers and receivers are returned to the normal mode.

5.2.2. TIMING THE DELAY

It is necessary to inhibit the computer at the start of the FRYX phase for a period equal to the round trip delay along the cable. A timing element such as a monostable multivibrator would be sufficient if this delay was constant, thus implying a fixed length of cable. The intention is to provide several outlets along the cable, allowing the terminal to have access to the cable from any one of several laboratories. The distance between the computer and the terminal is then a function of the terminal position and the cable delay is not constant. A more direct form of delay measurement is necessary. To do this, when it is necessary to inhibit the computer, a pulse is transmitted to the terminal which returns it along a second line. The return of this pulse at the computer then re-enables the machine. Figure 5.4a shows the generation of the STCX pulse which inhibits the computer and is transmitted to the terminal. The terminal returns the STCX pulse as the STCR pulse. The STCX pulse is also used for control purposes at the terminal end. This is discussed in Section 5.3. Figure 5.4b shows the circuitry for receiving the STCR pulse at the computer. The STCR pulse is then used to restart the computer and if it is a data-in instruction inhibits the drivers by placing a low on line INBT and enables the receivers by placing a logical high on line ENLE. The E-bus is now in a receive mode and data arriving from the terminal will be entered during the second phase.

5.2.3. IDENTIFYING THE PERIPHERAL LOCATION

Chapter 3 dealt with the problem of identifying whether a peripheral deviceis at the computer or at the terminal end. To do this a memory was used. Figure 5.5 shows the memory circuitry which contains up to five peripheral device addresses. The comparator circuits compare the addresses contained in the memory with any address appearing on the E-bus. Figure 5.2 shows the circuitry needed to load these memories using software. Situated at device address 77_8, the

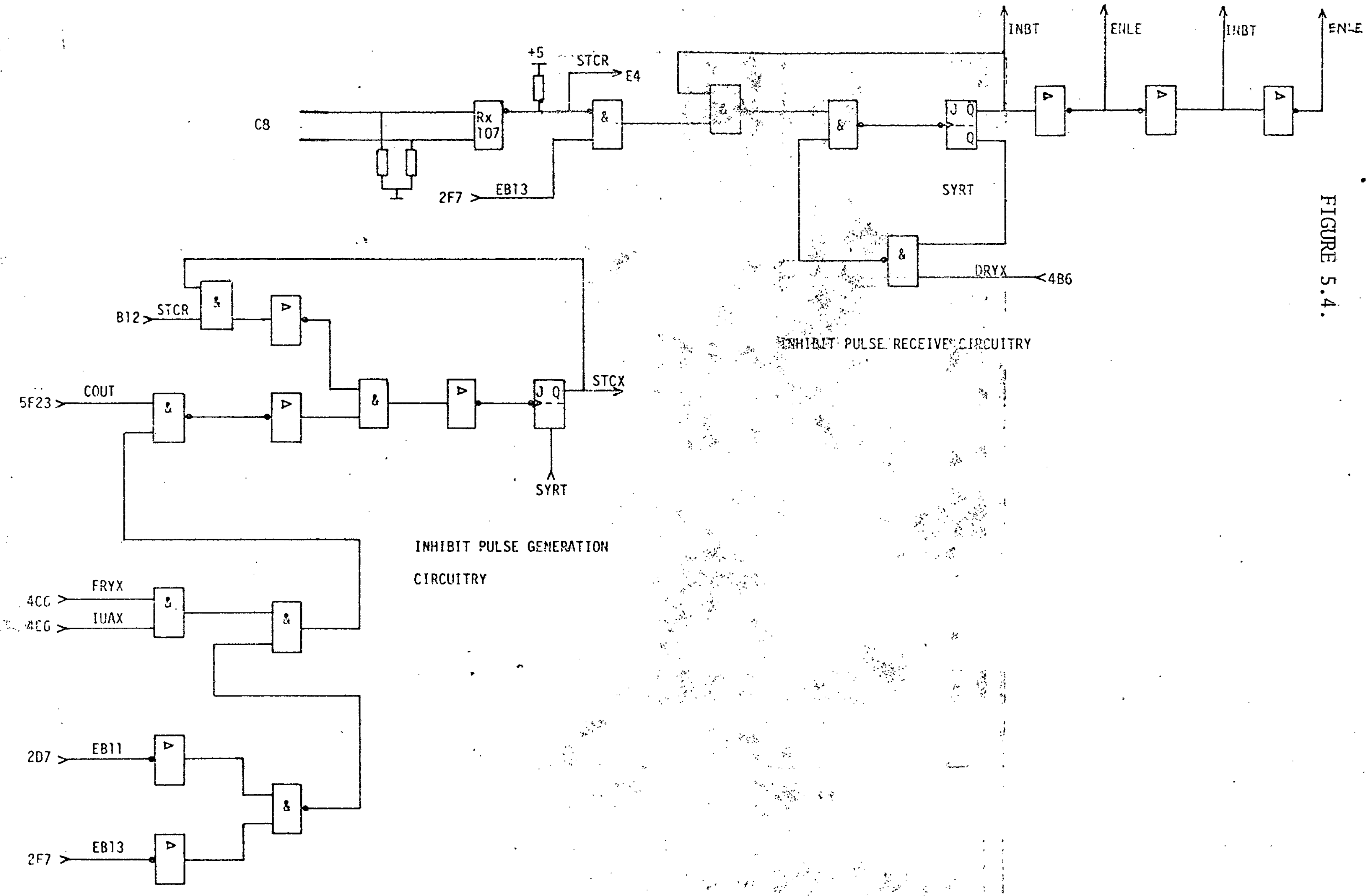
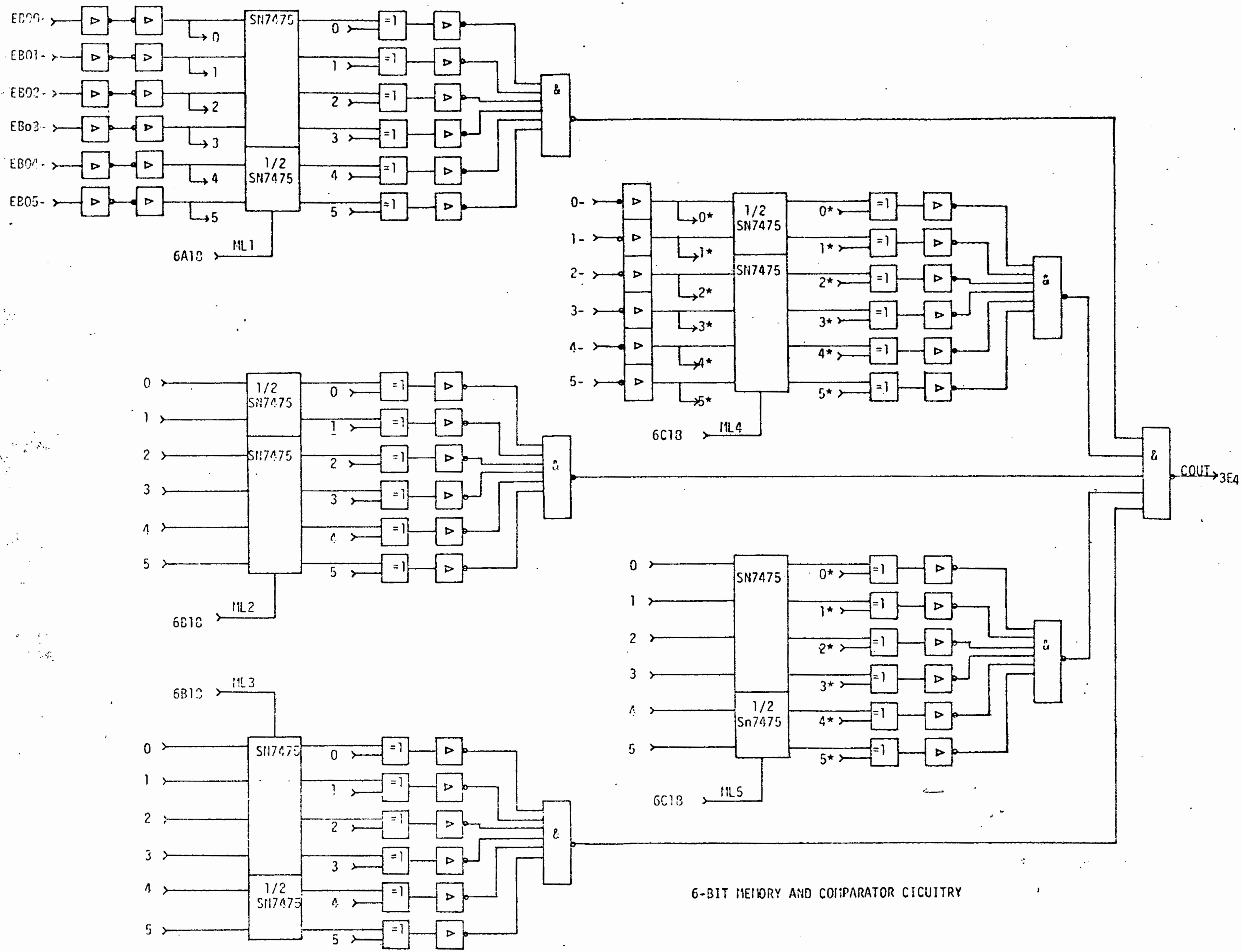

INBT
ENLE
INBT
ENLE
+5
STCR
E4
C8
Rx
107
&
J Q
Q
SYRT
2F7
EB13
DRYX
4B6
INHIBIT PULSE RECEIVE CIRCUITRY
B12
STCR
5F23
COUT
STCX
SYRT
INHIBIT PULSE GENERATION
CIRCUITRY
4CG
FRYX
4CC
IUAX
2D7
EB11
2F7
EB13

FIGURE 5.4.



6-BIT MEMORY AND COMPARATOR CICUITRY

FIGURE 5.5.

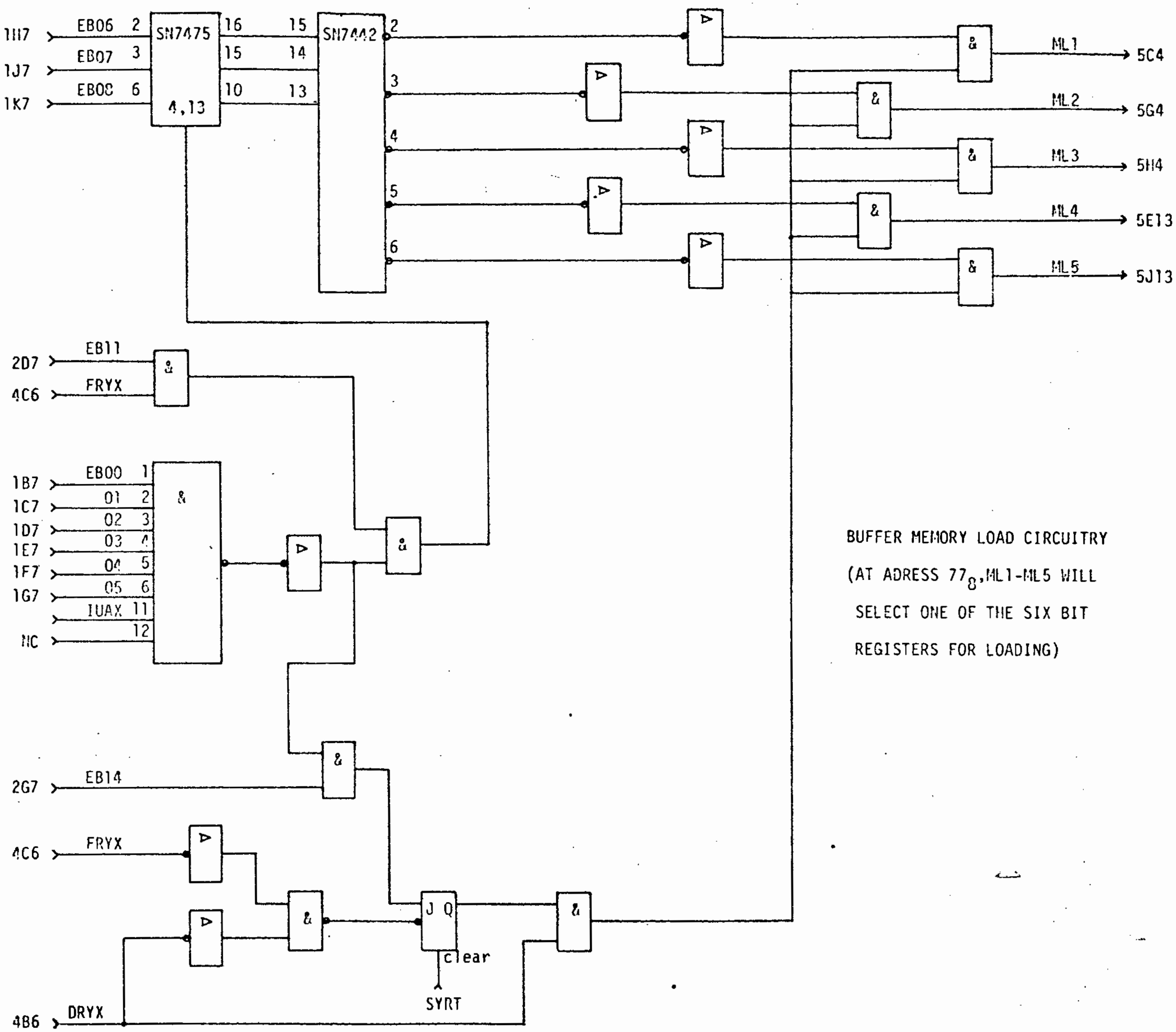


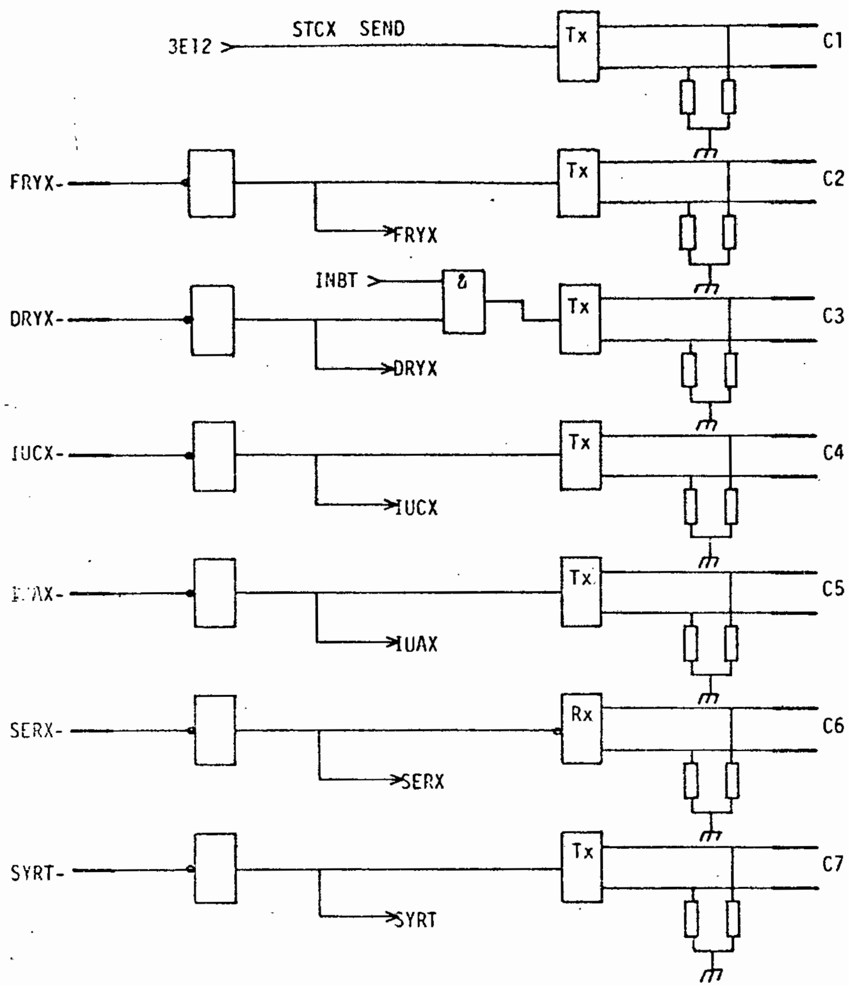
FIGURE 5.6.

BUFFER MEMORY LOAD CIRCUITRY

(AT ADRESS 77_8,ML1-ML5 WILL

SELECT ONE OF THE SIX BIT

REGISTERS FOR LOADING)



CONTROL LINE TRANSMIT CIRCUITRY

FIGURE 5.7.

load circuitry has an execute instruction to select one of the five memories. An output instruction from the A-register will then enter the contents of the A-register into the selected memory. During normal input-output operations if an address on the E-bus agrees with any of those held in the store, a pulse COUT is generated and is used to generate STCX.

5.2.4. CONTROL PULSES

The circuitry for transmitting and receiving the various control pulses is shown in figure 5.7. The control lines differ from the E-bus lines in that they are unidirectional.

5.3. THE TERMINAL CONTROL CIRCUITRY

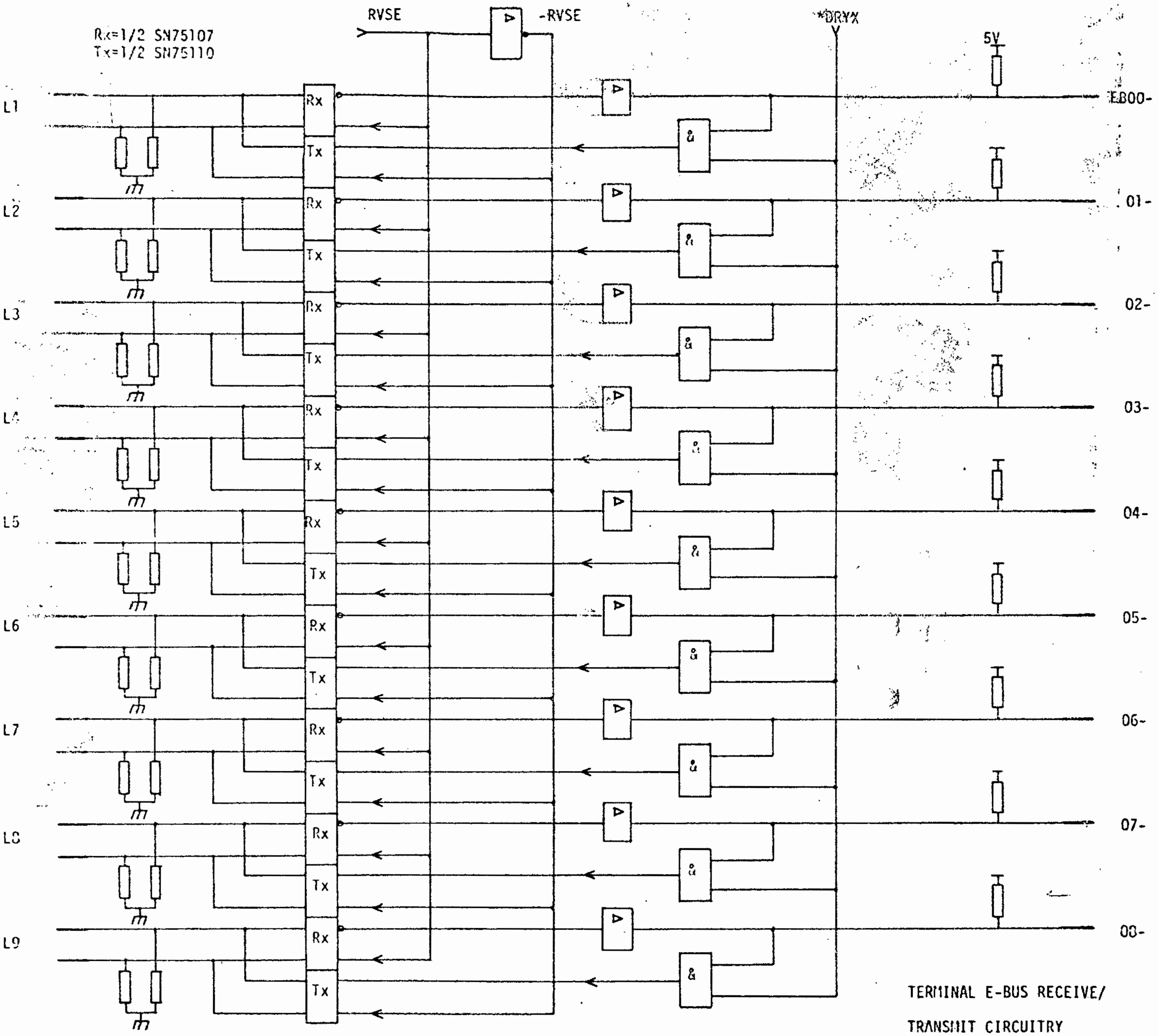
When the computer requires data from a peripheral situated at the terminal it is necessary to inhibit the computer during the FRYX phase. All the information on the control lines and the E-bus is held for the duration of this "freeze". This data is transmitted to the terminal. One of the tasks of the terminal control circuitry is to use this information to generate the normal timing sequence, extract the data from the addressed peripheral and return this data to the computer in time to be entered after the computer has been re-enabled.

5.3.1. THE E-BUS CIRCUITRY

Figures 5.8 and 5.9 show the E-bus circuitry. The sixteen lines are normally in the receive mode and all data received is displayed on the terminal equivalent of the E-bus. When it is necessary to supply the computer with data that has been placed on the equivalent E-bus by a peripheral device, the control circuitry switches the lines to the transmit mode and the equivalent DRYX or second phase generated by the control circuitry enters whatever has been placed onto the E-bus onto the transmission lines.

5.3.2. CONTROL CIRCUITRY

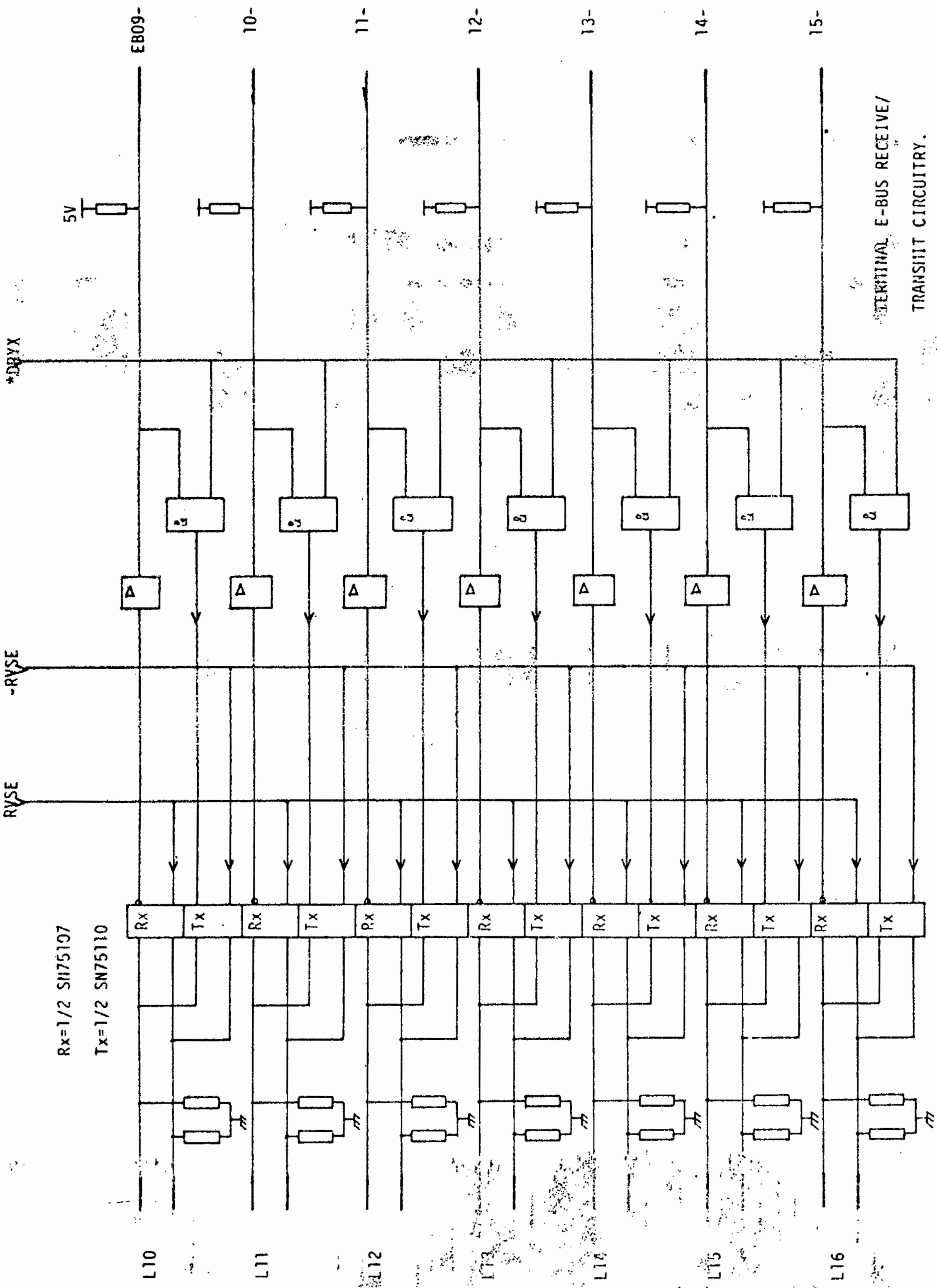
The arrival of the STCX pulse at the terminal indicates that the computer is frozen and the terminal must generate its own timing sequence. This is accomplished by terminating the FRYX phase at



TERMINAL E-BUS RECEIVE/
TRANSMIT CIRCUITRY

FIGURE 5.8.

FIGURE 5.9.



TERMINAL E-BUS RECEIVE/
TRANSMIT CIRCUITRY.

the appropriate time and switching the E-bus lines to the transmit mode and then generating a DRYX phase. In the case of the sense instruction the sequence is the same except that the DRYX phase is not generated. The E-bus circuitry is returned to the normal receive mode at the end of the simulated instruction cycle.

To generate the sequence of timing, the monostable multivibrator was investigated but was found to have appreciable random pulse width variations in the short term and a systematic changing of the pulse width over extended periods. The specifications for the control pulses that are given in the Varian data manuals do not allow for the pulse width or the time between pulses to vary to any extent and a more predictable system of pulse generation was required.

The circuit used to generate the timing sequence was a variable frequency 10 MHz pulse generator driving a 4-bit synchronous counter. The 4-bit output of the counter was then decoded to give the end of the FRYX phase, the beginning of the DRYX phase and the end of the DRYX phase. Timing was adjusted by either altering the clock frequency or changing the point at which decoding took place. Figure 5.10 shows this circuit and associated circuitry necessary to initiate and terminate the timing.

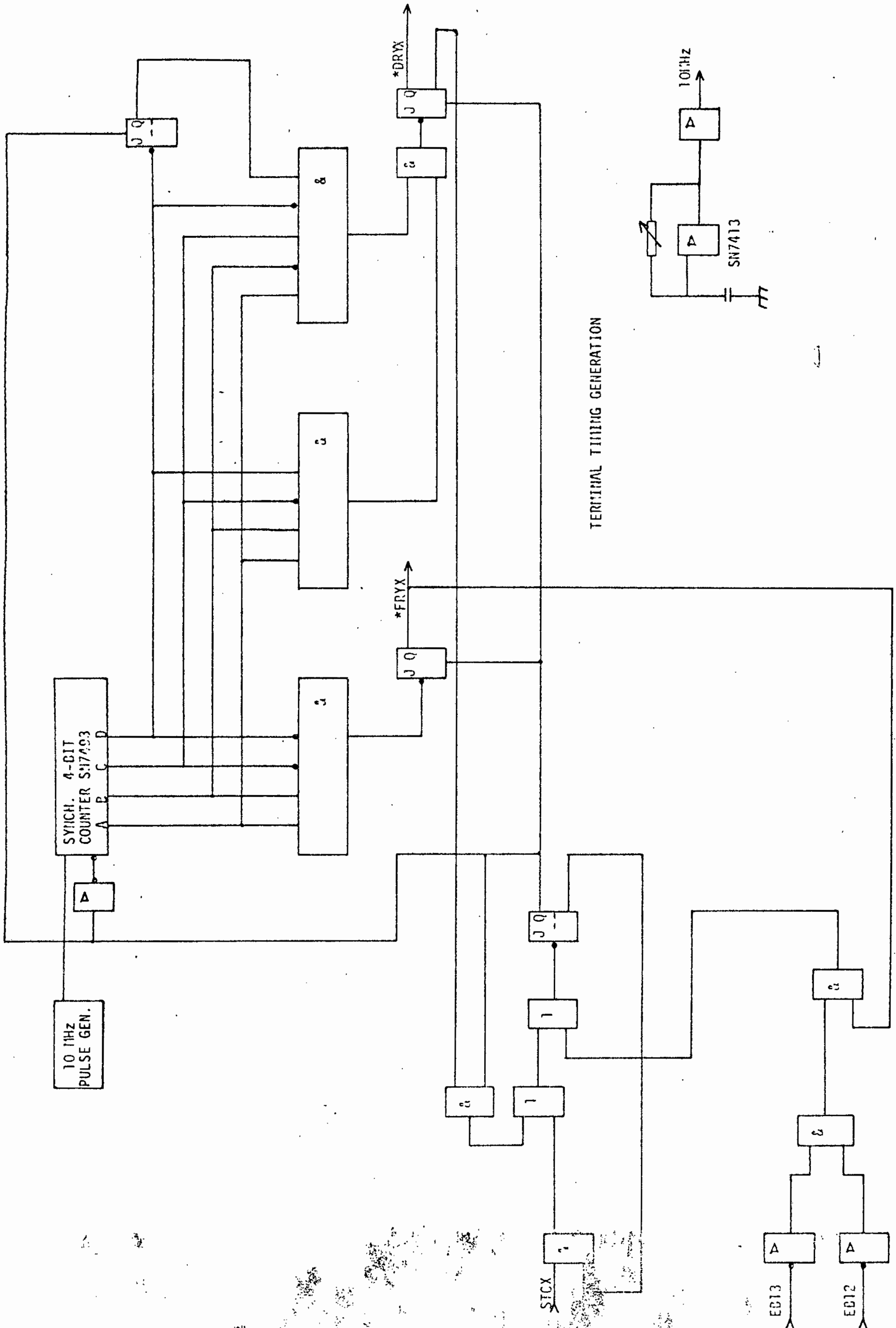
5.3.3. CONTROL PULSES

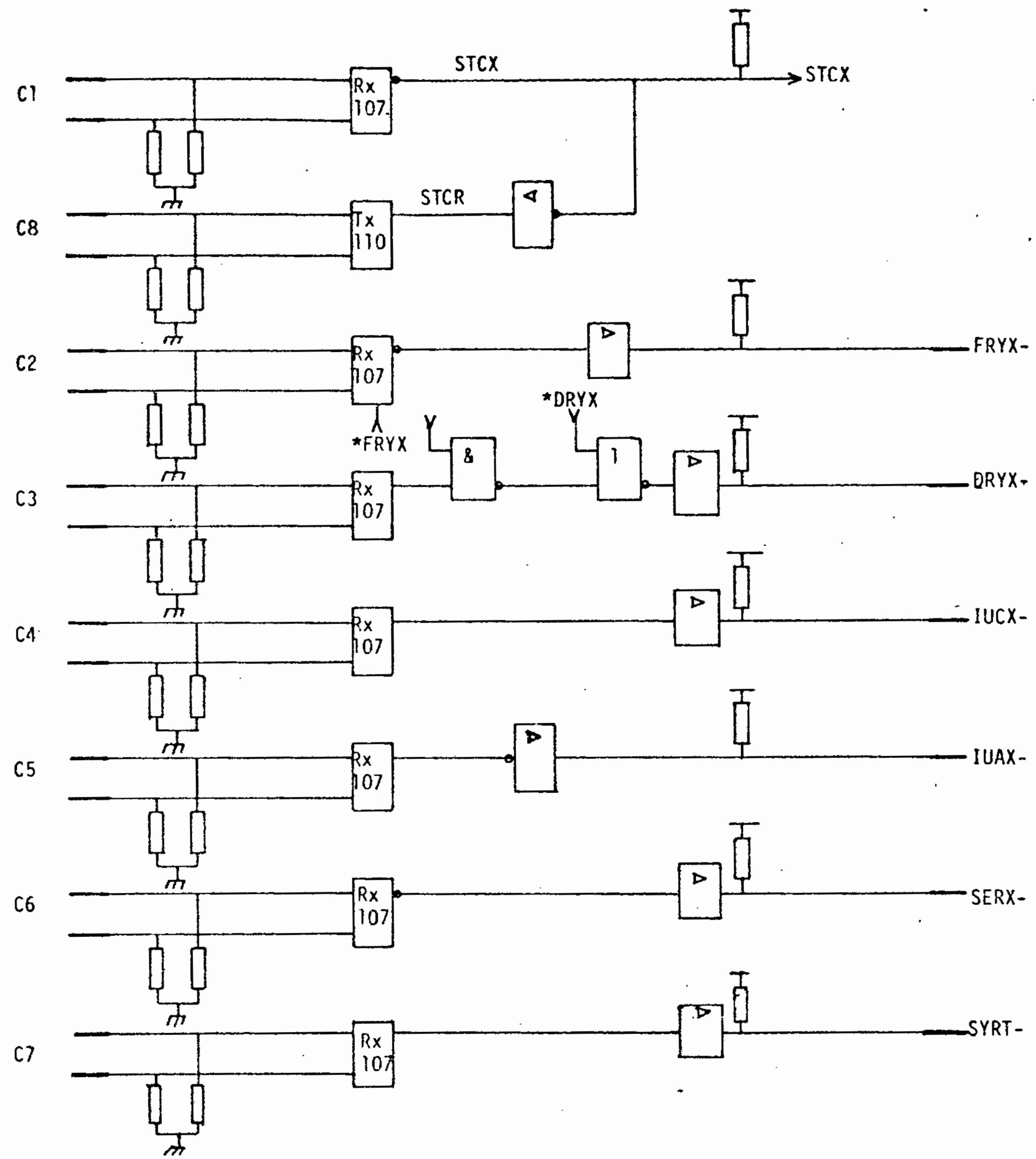
The different control lines are received and transmitted on uni-directional lines. In order to terminate the FRYX phase, the control circuitry inhibits the FRYX line receiver. When it is necessary to generate a DRYX phase for a data return to the computer, the DRYX line receiver is disabled and the control circuitry introduces its own DRYX. This circuitry is shown in Figure 5.11.

5.4. THE INTERRUPT SYSTEM

The computer interrupt structure consists of eight interrupt lines into the Priority Interrupt Module which arranges the interrupts into a priority chain. These eight interrupt lines were extended to the terminal as shown in Figure 5.12. As it is shown, each

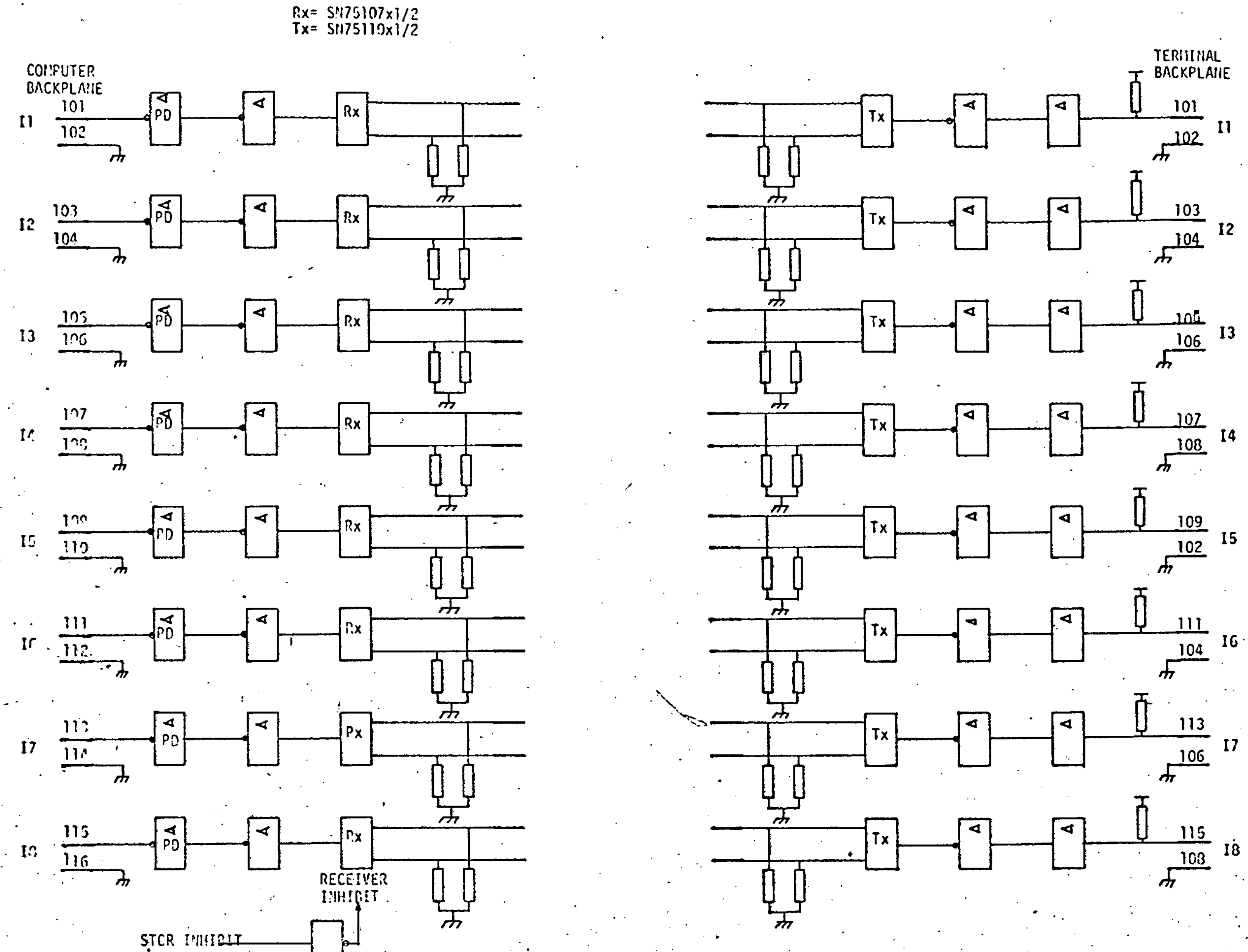
FIGURE 5.10.


TERMINAL TIMING GENERATION
*DRYX
*FRYX
10MHz
SN7413
SYNCH. 4-BIT
COUNTER SN7493
A B C D
10 MHz
PULSE GEN.
STCX
EB13
EB12



TERMINAL CONTROL LINE CIRCUITRY

FIGURE 5.11.



INTERUPT LINES I1 - I8 ARE WIPED ONTO BACKPLANE OF I/O SLOT POSITION FROM BACKPLANE OF THE PIM MODULE IN THE COMPUTER MAINFRAME.THE STCR INHIBIT LINE INHIBITS THE RECEIVERS WHEN LOGICALLY LOW.

INTERUPT LINES WIRED FROM THE FRONT PANEL OF THE TERMINAL ONTO THE BACKPLANE OF THE TERMINAL I/O CONTROLLER SLOT POSITION AND EXTENDED THROUGH TO THE COMPUTER.

FIGURE 5.12

interrupt uses a full transmission line. The possibility of multiplexing the eight interrupts onto one line using parallel to serial conversion was investigated. In applications where cable optimisation is necessary this approach would be valid, but serialisation results in each interrupt being scanned at a rate of less than 1 MHz when the components available are used. Careful assessment would be required of the effect of this restraint on equipment developed by users. As a 40-pair cable was available, parallel transmission was used, retaining the real time aspect of the information transmitted. An additional problem to serialisation is the problem of incorrect sampling when converting from serial to parallel, as descibed in Chapter 4. In control applications, an error on interrupt structure could produce interesting results!

5.5. THE TERMINAL STRUCTURE

The terminal system in the basic form described above consists of three parts.

[1] The computer control circuitry. It is situated as an interface between the Varian computer's input-output chassis and the transmission medium, and all circuityr is contained on one Varian board. The only feature distinguishing this board from the other standard interfaces is that it must have access to the Varian clock through the backplane of the slot in which the board is located. Figure 5.13 is a photograph of this board.

[2] The transmission medium consisting of 40 pairs of post office twisted cross-connection wire.

[3] The terminal control citcuitry. Again, this is located on one board interfacing the cable to the terminal input-output chassis. Figure 5.14 is a photograph of this board.

In this form an economical, compact and flexible system exists, the terminal hardware itself merely consisting of an input-output chassis and standard Varian supply with the terminal control interface occupying one slot position.

5.6. MULTIPLEXING

Several outlets along the link enabling the terminal to be connected into the link at any of these points is a requirement of the

FIGURE 5.13
Standard Varian interface board. Occupying one slot in the computer expanson chassis,it contains the circuitryfor the control of the terminal.

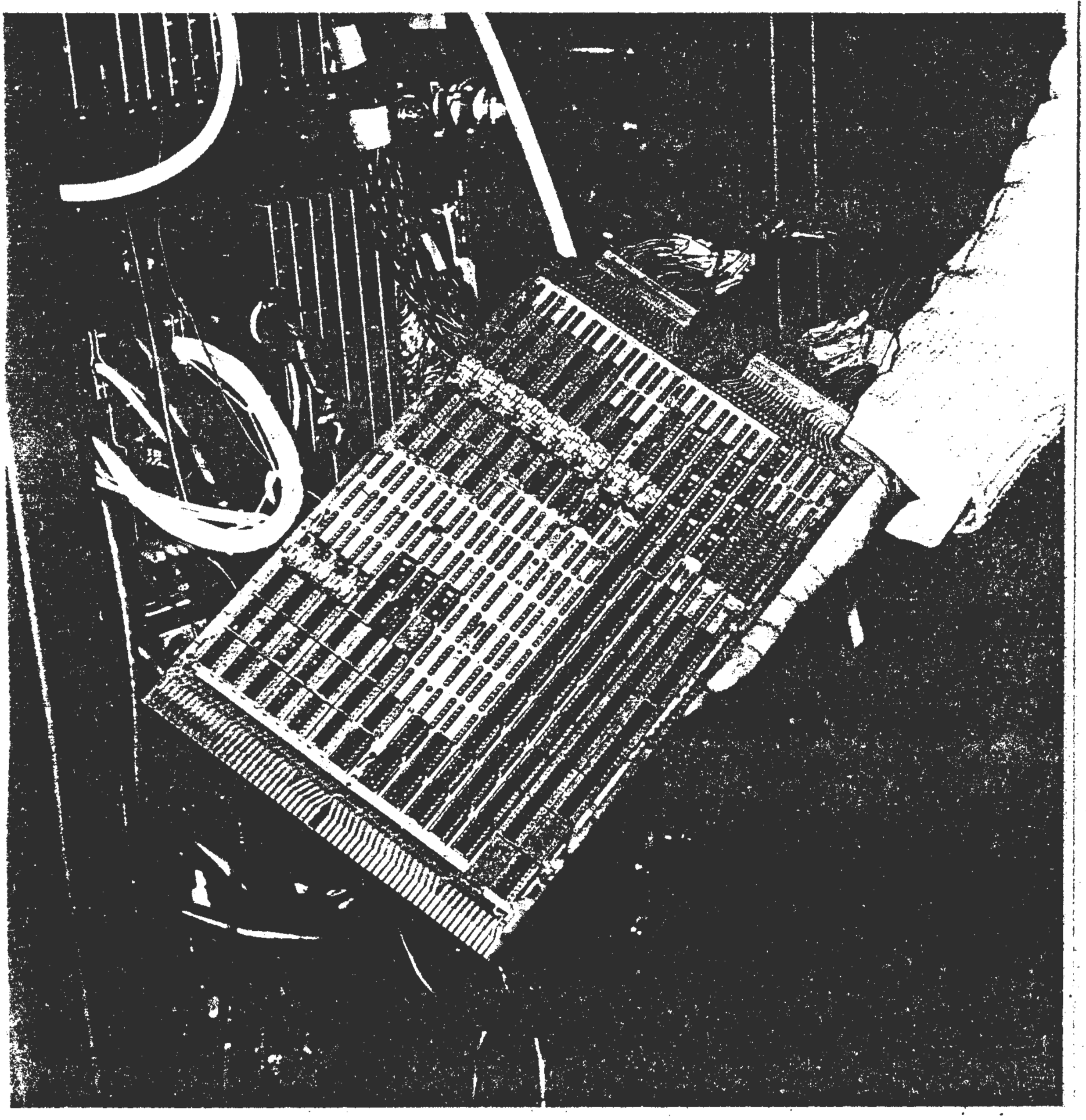
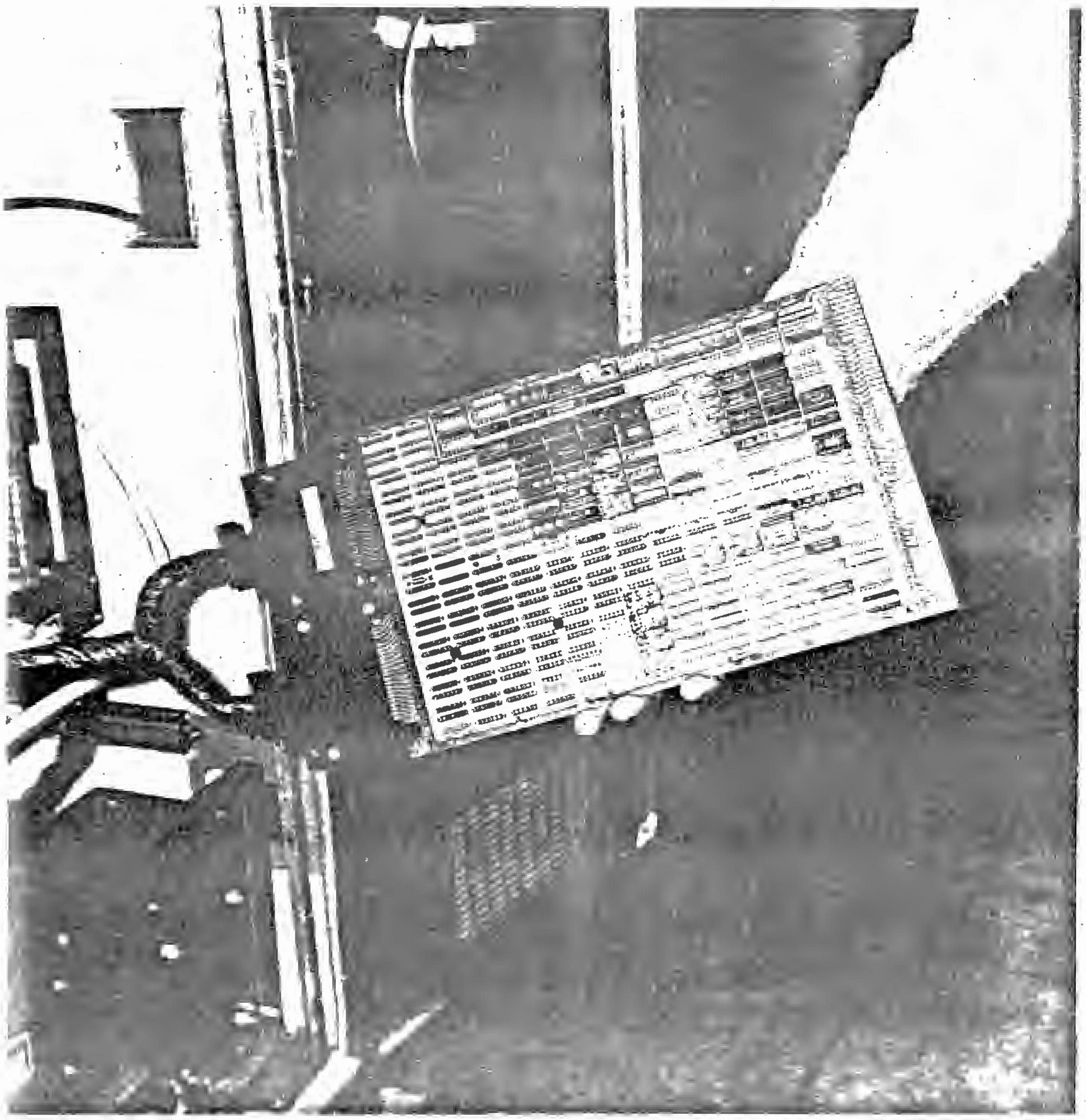


FIGURE 5 .14
Contains the terminal control circuitry.The terminal accesses the board through edge connector P1 on the right.The cable comes in on J1 and J2 on the left.



system. An advantage of the balanced line driving and receiving system used is that provided the cable is correctly terminated at both ends, driving and receiving can be done at any point along the line. An interesting situation now exists where it is possible to have more than one terminal system along the length of the line. The timing of the cable delay is now dependent on which of the terminals is being addressed. There are several ways in which the delay can be assessed.

[1] The control circuitry at the computer has a set of peripheral address memories for each terminal. Any address of a peripheral device situated at a terminal has the address stored in the memory associated with that terminal. Using a loop to time the delay to the terminal and back it would be necessary to provide a separate return path for each terminal. However, since each terminal is now in a fixed location, a timing element such as a monostable situated at the computer could account for the delay.

[2] A more flexible approach is to leave the control circuitry at the computer as it is and include a memory at each of the terminals. The terminal memories contain the addresses of the devices situated at that terminal. The computer then addresses the line without being aware of the location of the addressed peripheral. When the instruction being executed requires the delay to be taken into account, the terminal with the peripheral being addressed uses the contents of its memory to identify that a response is required, and returns the delay timing pulse along and commmon return line.

The terminal is again independent of its location and can be inserted at any point along the line. Obviously, the same device address cannot be used for similar devices situated at different points along the line.

5.7. OPTIMISING THE NUMBER OF LINES

Each line consisting of a driver and receiver element and a twisted pair cable represents capital expenditure and the reduction of the number of pairs required is an advantage.

The use of serialisation techniques can be used for sets of data lines such as the eight interrupt lines. Serialisation in that particular instance applied unacceptable constraints upon the user.

The E-bus has sixteen bits of data in parallel on it. This parallel data dictated parallel transmission, and considering the random nature of the data on any one of the lines, a reduction in the number of lines to transmit the E-bus information must result in a loss of information.

The control lines have little room for minimising the number of lines. The control lines in general contain time information on the sequence in which events must occur. The serialisation will reduce this information content. The DRYX line, though, is redundant since in a two phase operation the DRYX phase is identified by information contained in the first phase. The DRYX line can therefore be eliminated altogether and the DRYX phase reconstructed at the terminal end, or a more attractive approach would be to use the same line transmitting the FRYX phase and the DRYX phase with the appropriate switching between the two.

The SERX sense line and the SYRT, or system reset line, can never contain information simultaneously. The SERX line is used during the execution of a sense instruction while the SYRT line is used to reset peripheral devices only when and input-output instruction is not being executed. The line can therefore be used to convey SYRT normally, and at the start of the sense instruction cycle, the direction of this line can be reversed to convey the SERX signal.

Refinements such as these would lead to a minimum cable size. In the prototype, a 40 twisted pair cable was available and minimisation was not applied.

* * *

CHAPTER SIX / ANCILLARY FEATURES AT THE TERMINAL

6

6.1. INTRODUCTION

The ultimate usefulness of the terminal system will be determined by the user's response to it. The basic system described in the previous chapter, while providing a terminal structure, requires additional features such as the indication of the computer status before it becomes attractive to the user.

6.2. COMPUTER STATUS INDICATION

Originally the user had the computer on site, giving access to the entire front panel of the computer. It needs to be asked to what extent these facilities need to be extended to the terminal.

[1] The sense switches. The three sense switches allow for the manual alteration of the programme flow. To provide a set of sense switches at the terminal, the output of the debounce circuits of the switches at the computer would require modification to allow parallel operation with the switch at the terminal. Investigation showed that certain integrated circuits on the computer motherboard would need to be changed for their open collector equivalents, the printed circuit track would have to be cut in places and clumsy wiring between the console motherboard and the expansion chassis would be necessary. The terminal is destined for control and data capture purposes and as such, all software used on it should be tried and tested. It was decided that on this basis a software equivalent of the sense switch could be implemented according to the user's needs. Three methods exist whereby this can be implementd:

(i) Using the interrupt. Three of the eight available interrupt lines could be used for the sense switch application. If any of the three interrupt lines are set, the software simulates a sense switch.

(ii) Continuously sense an input device such as the graphic display or the teletype for one of three characters, each character representing a sense switch.

(iii) The terminal has an interface device that provides the user with 24 sense lines (described in 6.6.). A continuous scan of three of these sense lines could simulate the sense switches.

[2] Control switches, register access, and indication. The magnitude of the modifications to the computer motherboard and the cabling necessary to extend access to, and indication of, even one of the computer registers, precludes consideration. --> The question is are the run and step switches to be extended? Having access to the run switch assumes that the user is able to dictate the point at which the programme must start. This requires the register access facility which has already been discounted, and so extending the run/step facility is unnecessary. Chapter 7 deals with hardware and software which prevents the computer going into step while executing a program.

[3] Computer status indication. The three status indications extended to the computer were run/step, indicating whether the computer is in the run or step mode, and the OVFL indication, indicating whether the overflow has been set.

(i) Run/Step. The run/step indications are complementary, the computer either being in run or in step. The indication was derived from the line HLTX-1 on pin 70 of the back plane wiring of the Processor 1 card in the computer mainframe, and wired onto the backplane of the terminal control card in the expansion chassis of the computer.

(ii) The OVFL indication is dictated by the line OVXX+ on pin 13 of the backplane wiring of cards DM 102-8 of the computer mainframe and was extended to the backplane of the terminal control card.

Both the run/step and OVFL indications do not have noise or speed problems associated with the data transmission.

Essentially, three conditions exist. Either run is on (Step being complementary), OVFL is on, or run and OVFL are on. Various techniques of impressing this information on a single pair of lines were looked at. This consisted of a crude serial system with a start pulse and two bits to contain the information, and using the balanced line transmission system, since this was available. A second approach was to use three level transmission on a single line, but this required too many discrete components. As there were spare cables available, cable optimisation was not performed and the indications were carried over on two pairs as shown in Figure 6.1.

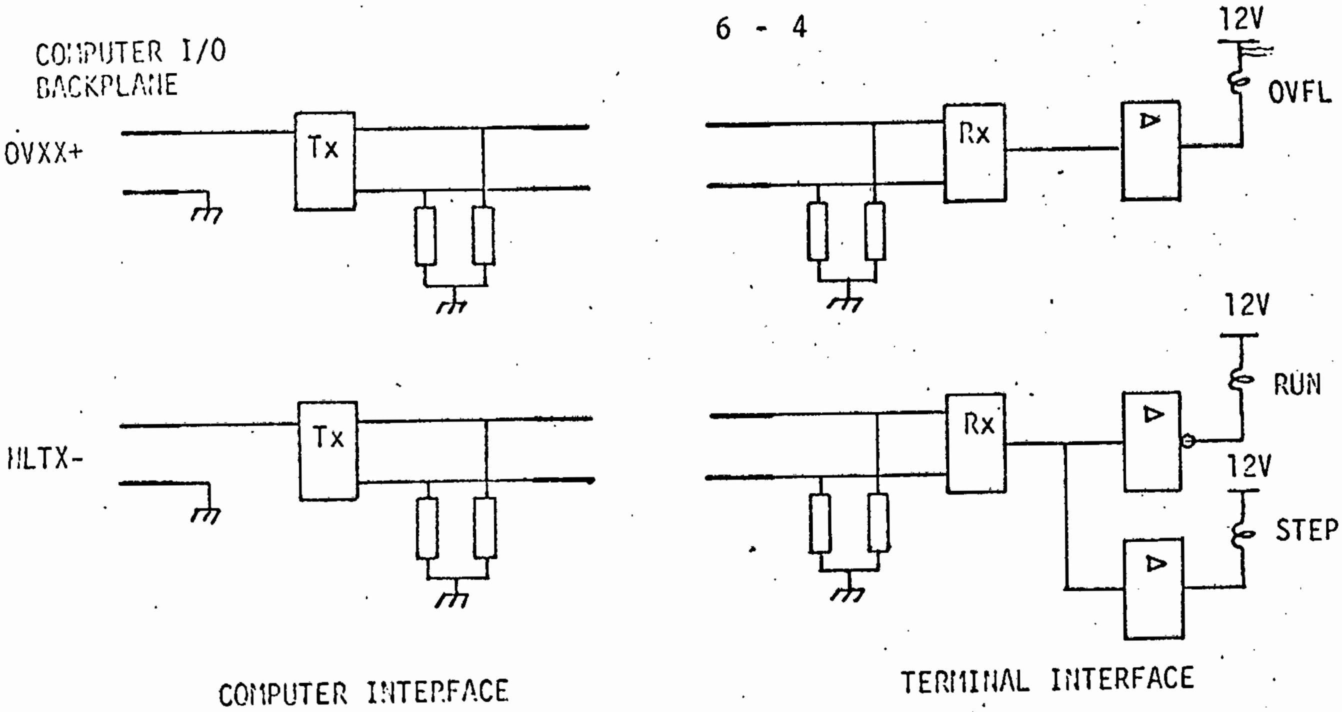
6.3. VOICE COMMUNICATION

Initial usage of the basic terminal structure showed the need for a voice channel between the terminal and the computer. This was implemented using the master/slave technique. In the normal position, the loudspeaker situated at the terminal operates as a microphone, and feeds an amplifier which drives down the line to a speaker at the computer. For speech from the computer to the terminal, the operator at the terminal presses a button reversing the amplifier and the roles of both the loudspeakers. Figure 6.2. shows the circuit. The limitations of the speaker and amplifier confine the frequency response to a range between 200 Hz and 4 kHz, sufficient for comprehension.

6.4. TERMINAL ENABLE/DISABLE

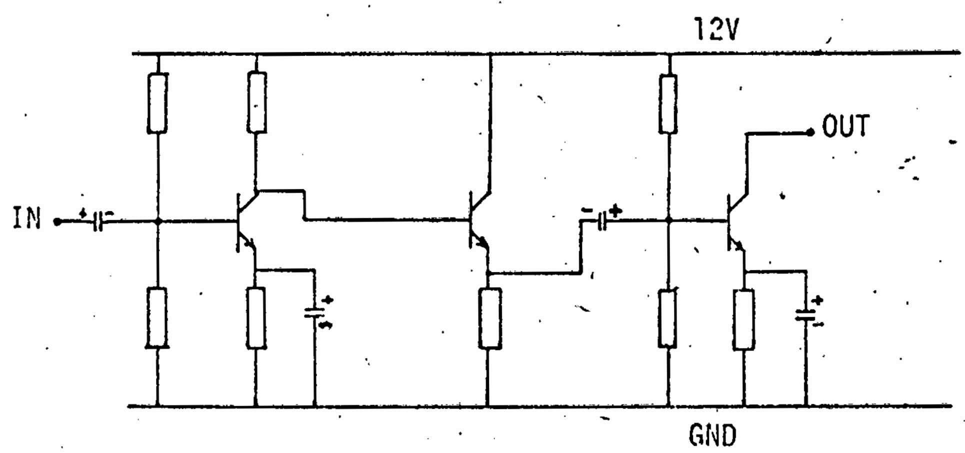
When power is removed from the terminal, the transmission loop for timing the delay and the eight interrupt line receivers at the computer are not held in one or two states by the terminal line drivers and the receivers supply erroneous information to the computer. To prevent this, two facilities were included at the computer:

[1] Manual enable/disable. This consisted of a toggle switch at the computer which in the disable position prevented the terminal control circuitry from having access to the computer clock and disabled all the receiver outputs at the computer. This switch is only enabled after power has been placed on the

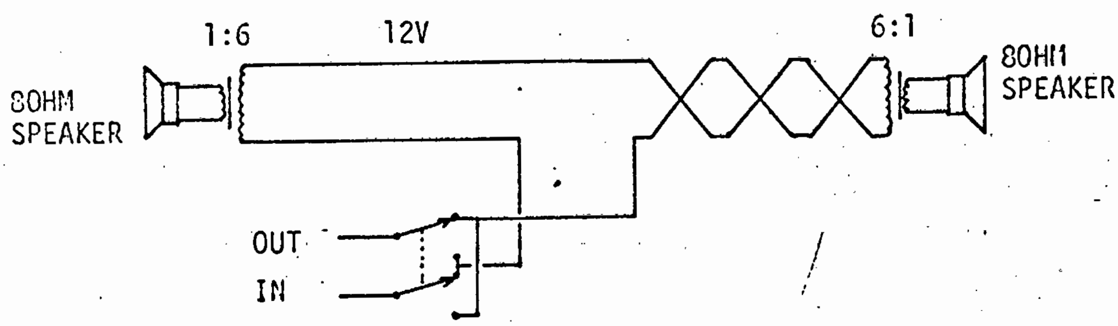


COMPUTER STATUS INDICATION

FIGURE 6.1



(a) INTERCOM AMPLIFIER



SWITCHING DIRECTION OF INTERCOM AT TERMINAL

(b)

FIGURE 6.2

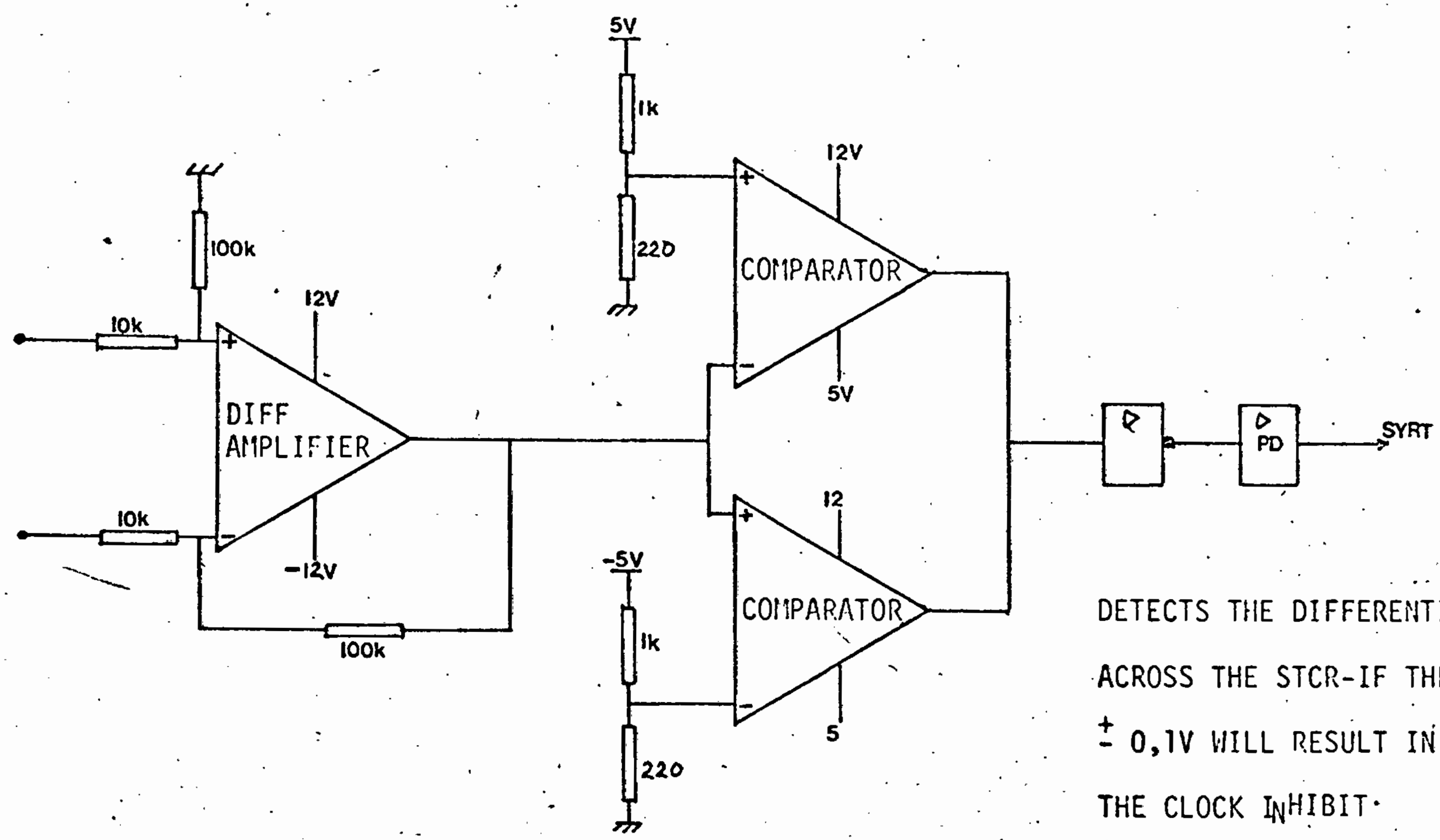


FIGURE 6.3

DETECTS THE DIFFERENTIALVOLTAGE ACROSS THE STCR-IF THE VOLTAGE WITHIN ± 0,1V WILL RESULT IN A SYRT AND DISABLES THE CLOCK INHIBIT.

terminal.

[2] Automatic terminal disable. This consists of a circuit which monitors the STCR line with a comparator circuit. When power is on at the terminal, the differential voltage across this line is always $\pm 0,2$V approximately. Should the power be removed from the terminal, the line is approximately at zero V. The comparator detects if the voltage is within the range $\pm$ 0,1 V. If the voltage is in this range, the circuit duplicates the action of the manual switch. The circuit is shown in Figure 6.3.

6.5. COMPUTER POWER FAIL

If the computer power should go down, the E-bus line receivers at the terminal will output erroneous information, resulting in possible damage to peripheral devices. A current loop was included in the system to prevent power existing at the terminal without there being power at the computer first as shown in Figure 6.4.

6.6. FRONT PANEL OF THE TERMINAL

Besides the indication lamps already mentioned, several additional facilities were included as shown in Figure 6.5.

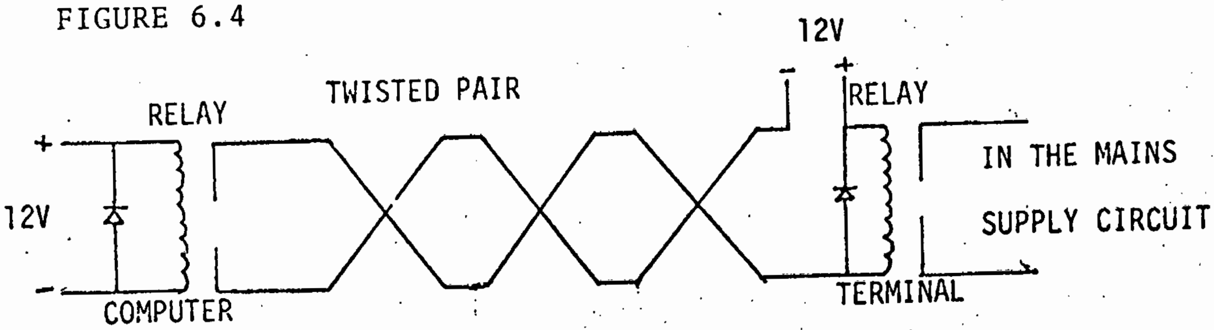
[1] Interrupt button. [20] A system had been developed which allowed the manual interrupting of the Varian 620I computer programme to the AID debug programme. This facility was extended to the terminal, as shown in Figure 6.6, providing a useful method of jumping out of an endless loop programme.

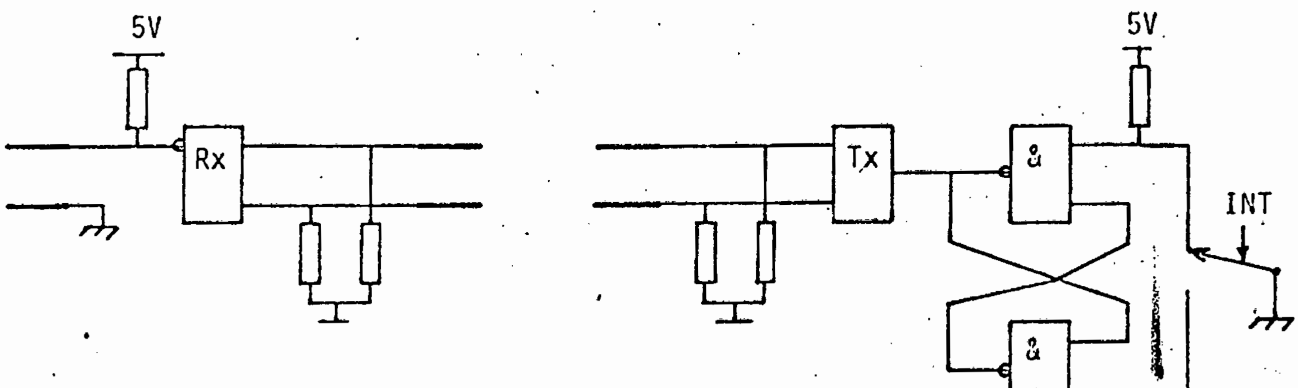
[2] Sense lines. An interface controller, situated at the terminal, allows a user to sense any one of twenty four lines via the front panel.

[3] Execute lines. Included in the sense interface is a facility which allows the user to initiate any one of 24 devices, again through the front panel.

[4] Interrupt lines. Described in Chapter 5, these lines are wired

FIGURE 6.4

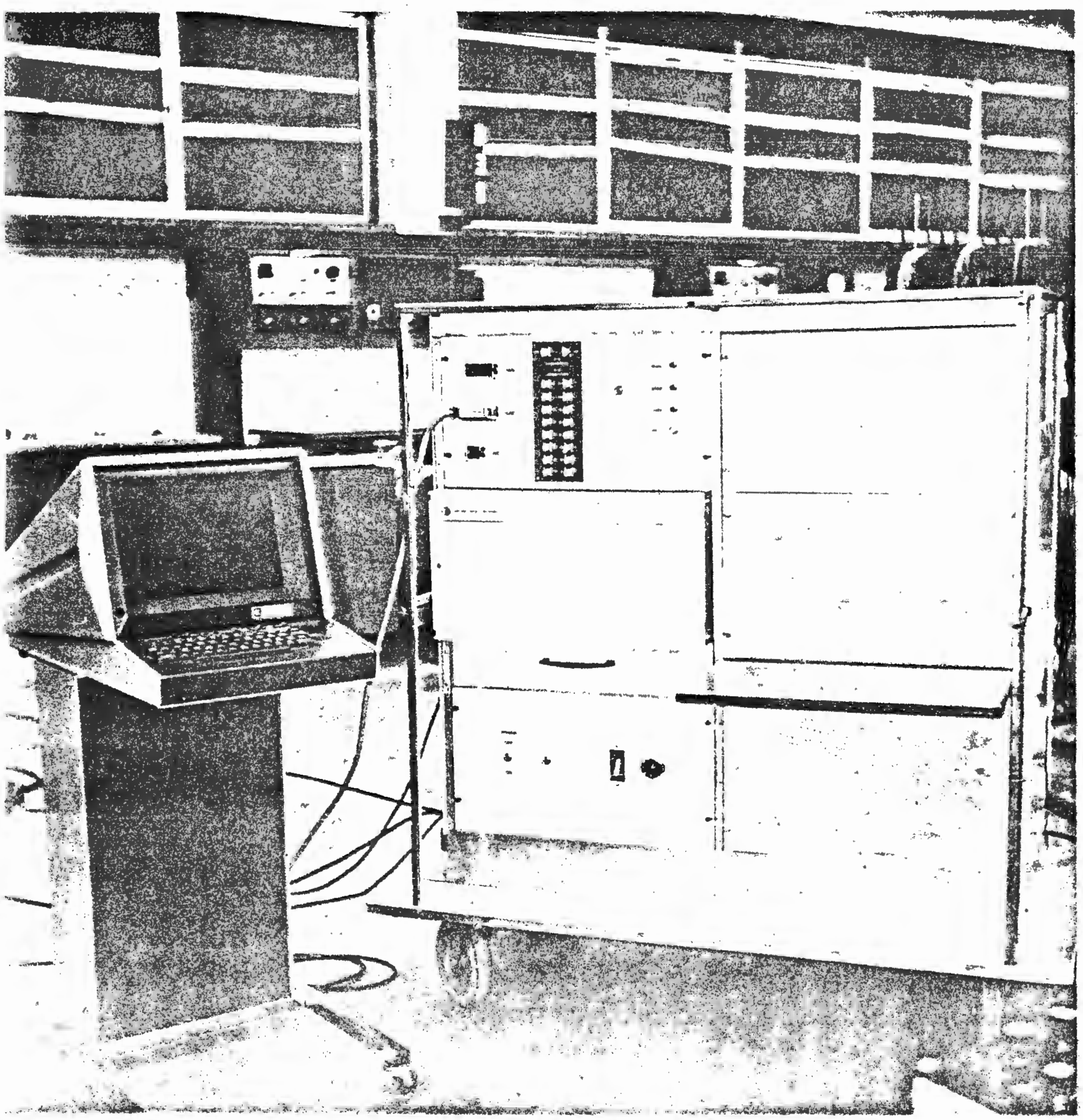




DEBOUNCED INTERUPT TRANSMITTED TO COMPUTER
AND orED WITH LOCAL INTERUPT BUTTON ANDINITIATES
AN INTERUPT TO THE CONTROL PROGRAM, AID.

FIGURE 6.6

FIGURE 6.4
THE TERMINAL.



to the front panel to give the user access to the eight interrupt lines.

[5] Analog/Digital and Digital/Analog outlets are provided in the front panel, sixteen of the former, and two of the latter. These outlets connect to their respective cards situated in the expansion chassis.

* * *

CHAPTER SEVEN / EVALUATION OF THE TERMINAL SYSTEM

7

7.1. RELIABILITY

The information, as it is presented on the input-output bus of the computer, has built-in redundancy to ensure reliability. For example, the data transfer out timing allows 300nS on the leading edge and 200 nS on the trailing edge of the bits of information on the E-bus during which settling down and phase shift errors occur. The information is only sampled for the 200 nS interval at the centre of this information. This advantage is retained in the parallel form of transmission. Any difference in phase delay along the different lines will be small because of the lines having similar characteristics. This phase shift is absorbed by the redundancy.

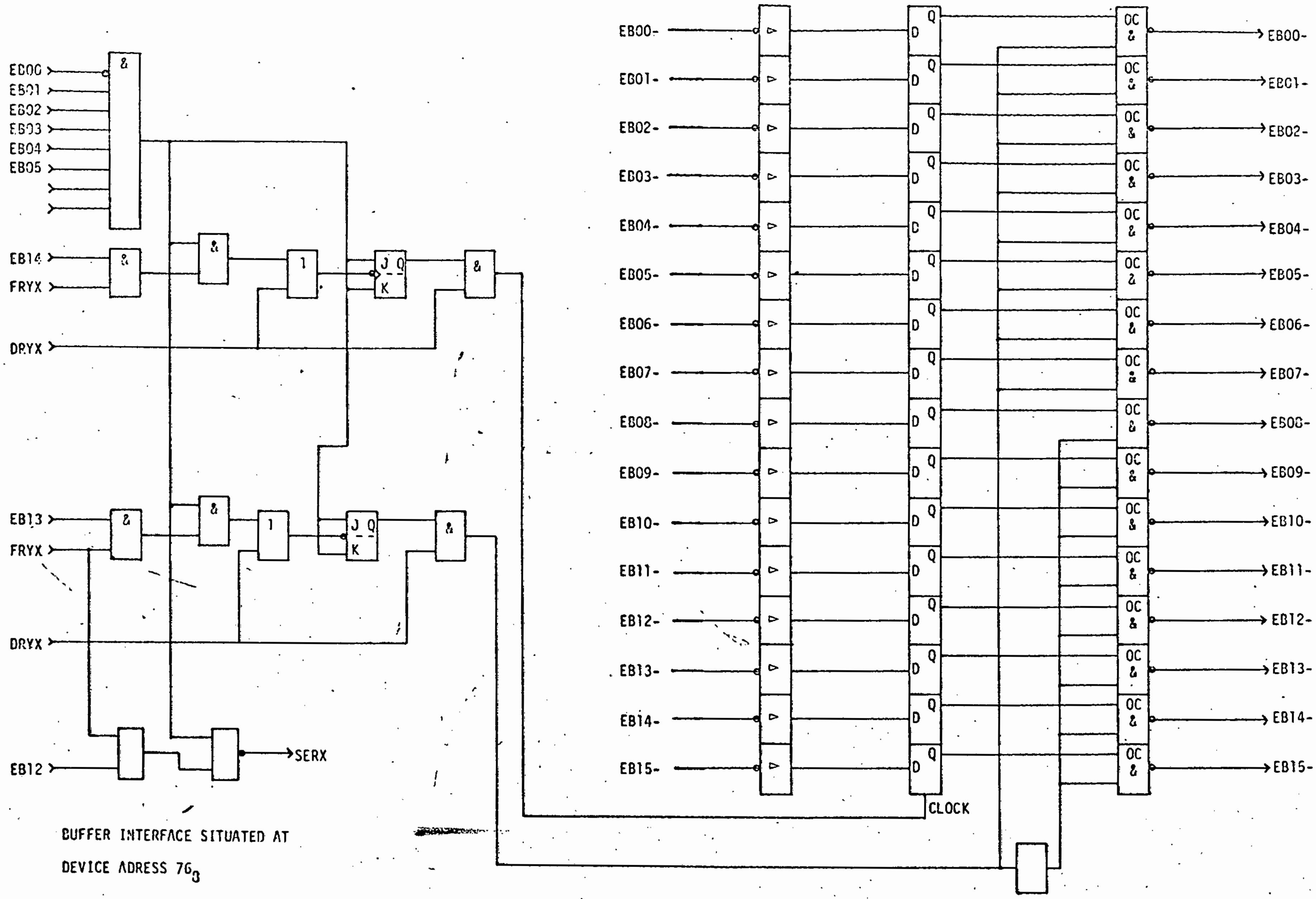
Tests were performed in an attempt to assess the reliability of the system in a noisy environment.

7.2. TEST HARDWARE

Testing the terminal served two objectives. Initial testing using a dual beam oscilloscope served to test the soundness of the philosophy behind the logic design approach, and to generate know-how in the machine. The secondary testing consisted of checking error rates on the system.

The hardware for performing these tests consisted of an interface situated at the terminal and operating as a device at address 76_8. The device is capable of accepting and storing a 16-bit word using a data-out instruction from the computer. A date-in instruction will return the contents of the 16-bit store to the computer. Figure 7.1. shows the logic implementation.

The interface proved to be a useful maintenance tool and includes



BUFFER INTERFACE SITUATED AT

DEVICE ADRESS 76_8

FIGURE 7.1

a facility for checking the sense line.

7.3. TEST SOFTWARE

The object of the test software was to gauge the effect of cross-talk and a noisy environment using the hardware desribed in the previous section. Essentailly the routines continuously outputted and inputted a sixteen-bit word to the store. The reply from the store was entered into an array in memory.

Programme 1:

LABEL FIELD	MNEMONIC	VARIABLE FIELD
START	LDXI	010000
J1	LDA	CODE
	OAR	076
	CIA	076
	STA	010000,1
	JXZ	036000
	DXR	
	JMP	J1
CODE	BSS	1

Figure 7.2. shows the 16-bit word consisting of all ones received from the store and entered into memory. Figure 7.3. shows the received data for a word consisting of all zeros.

Programme 2:

LABEL FIELD	MNEMONIC	VARIABLE FIELD
START	LDXI	010000
J1	LDA	COD 1
	IAR	076
	CIA	076
	STA	010000,1
	LDA	COD 2
	OAR	076
	CIA	076
	DXR	
	STA	010000,1
	JXZ	036000
	JMP	J1
COD 1	BSS	1

FIGURE 7.2

ALL ONE;S RECEIVED FROM THE TERMINAL

010420	177777	177777	177777	177777	177777	177777	177777	177777
010430	177777	177777	177777	177777	177777	177777	177777	177777
010440	177777	177777	177777	177777	177777	177777	177777	177777
010450	177777	177777	177777	177777	177777	177777	177777	177777
010460	177777	177777	177777	177777	177777	177777	177777	177777
010470	177777	177777	177777	177777	177777	177777	177777	177777
010500	177777	177777	177777	177777	177777	177777	177777	177777
010510	177777	177777	177777	177777	177777	177777	177777	177777
010520	177777	177777	177777	177777	177777	177777	177777	177777
010530	177777	177777	177777	177777	177777	177777	177777	177777
010540	177777	177777	177777	177777	177777	177777	177777	177777
010550	177777	177777	177777	177777	177777	177777	177777	177777
010560	177777	177777	177777	177777	177777	177777	177777	177777
010570	177777	177777	177777	177777	177777	177777	177777	177777
010600	177777	177777	177777	177777	177777	177777	177777	177777
010610	177777	177777	177777	177777	177777	177777	177777	177777
010620	177777	177777	177777	177777	177777	177777	177777	177777
010630	177777	177777	177777	177777	177777	177777	177777	177777
010640	177777	177777	177777	177777	177777	177777	177777	177777
010650	177777	177777	177777	177777	177777	177777	177777	177777
010660	177777	177777	177777	177777	177777	177777	177777	177777
010670	177777	177777	177777	177777	177777	177777	177777	177777
010700	177777	177777	177777	177777	177777	177777	177777	177777
010710	177777	177777	177777	177777	177777	177777	177777	177777
010720	177777	177777	177777	177777	177777	177777	177777	177777
010730	177777	177777	177777	177777	177777	177777	177777	177777
010740	177777	177777	177777	177777	177777	177777	177777	177777
010750	177777	177777	177777	177777	177777	177777	177777	177777
010760	177777	177777	177777	177777	177777	177777	177777	177777
010770	177777	177777	177777	177777	177777	177777	177777	177777
011000	177777	177777	177777	177777	177777	177777	177777	177777
011010	177777	177777	177777	177777	177777	177777	177777	177777
011020	177777	177777	177777	177777	177777	177777	177777	177777
011030	177777	177777	177777	177777	177777	177777	177777	177777
011040	177777	177777	177777	177777	177777	177777	177777	177777

FIGURE 7.3

ALL ZERO'S RECEIVED FROM THE TERMINAL

010410	000000	000000	000000	000000	000000	000000	000000	000000
010420	000000	000000	000000	000000	000000	000000	000000	000000
010430	000000	000000	000000	000000	000000	000000	000000	000000
010440	000000	000000	000000	000000	000000	000000	000000	000000
010450	000000	000000	000000	000000	000000	000000	000000	000000
010460	000000	000000	000000	000000	000000	000000	000000	000000
010470	000000	000000	000000	000000	000000	000000	000000	000000
010500	000000	000000	000000	000000	000000	000000	000000	000000
010510	000000	000000	000000	000000	000000	000000	000000	000000
010520	000000	000000	000000	000000	000000	000000	000000	000000
010530	000000	000000	000000	000000	000000	000000	000000	000000
010540	000000	000000	000000	000000	000000	000000	000000	000000
010550	000000	000000	000000	000000	000000	000000	000000	000000
010560	000000	000000	000000	000000	000000	000000	000000	000000
010570	000000	000000	000000	000000	000000	000000	000000	000000
010600	000000	000000	000000	000000	000000	000000	000000	000000
010610	000000	000000	000000	000000	000000	000000	000000	000000
010620	000000	000000	000000	000000	000000	000000	000000	000000
010630	000000	000000	000000	000000	000000	000000	000000	000000
010640	000000	000000	000000	000000	000000	000000	000000	000000
010650	000000	000000	000000	000000	000000	000000	000000	000000
010660	000000	000000	000000	000000	000000	000000	000000	000000
010670	000000	000000	000000	000000	000000	000000	000000	000000
010700	000000	000000	000000	000000	000000	000000	000000	000000
010710	000000	000000	000000	000000	000000	000000	000000	000000
010720	000000	000000	000000	000000	000000	000000	000000	000000
010730	000000	000000	000000	000000	000000	000000	000000	000000
010740	000000	000000	000000	000000	000000	000000	000000	000000
010750	000000	000000	000000	000000	000000	000000	000000	000000
010760	000000	000000	000000	000000	000000	000000	000000	000000
010770	000000	000000	000000	000000	000000	000000	000000	000000
011000	000000	000000	000000	000000	000000	000000	000000	000000
011010	000000	000000	000000	000000	000000	000000	000000	000000
011020	000000	000000	000000	000000	000000	000000	000000	000000
011030	000000	000000	000000	000000	000000	000000	000000	000000

FIGURE 7.4

testing the prior history

[illegible]	[illegible]	[illegible]	[illegible]	052525	125252	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	052525	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	052525	[illegible]	[illegible]
[illegible]	125252	[illegible]	125252	052525	125252	052525	125252	052525
[illegible]	125252	[illegible]	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	125252	052525	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	125252	[illegible]	125252	052525	125252	052525	125252	052525
[illegible]	125252	[illegible]	125252	052525	125252	052525	125252	052525
[illegible]	125252	[illegible]	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	125252	052525	125252	052525	125252	052525	125252	[illegible]
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525
[illegible]	125252	052525	125252	052525	125252	052525	[illegible]	052525
[illegible]	[illegible]	[illegible]	125252	052525	125252	052525	[illegible]	[illegible]
[illegible]	125252	052525	125252	052525	125252	052525	125252	052525

Programme 2 (Continued)

COD 2	BSS	1

This programme is typical of the programme used to test the past history of the terminal. Two words are alternately sent to the terminal, stored, and then returned. Figure 7.4. shows the return data fro two words alternately seen from the terminal.

7.4. CONTROL HARDWARE AND SOFTWARE

With a distance of some 200 yards between the computer and the terminal, the computer going into step while executing a programme has obvious disadvantages for the user. Hardware and software that would avoid this were briefly investigated.

7.4.1. CONTROL HARDWARE

The large computers have a protect facility which generates an interrupt instead of going into step when the computer attempts to execute an illegal instruction. Investigation showed that this could be applied to the Varian Computer. Logic can be made to inhibit the pulse on the step line and to generate an interrupt back to AID.

7.4.2. CONTROL SOFTWARE

Varian Data recently produced a new version of their AID debug programme, AIDF. This control programme has a facility for testing the valididty of each instruction before execution. This allows the initial debugging of a programme on site without fear of stepping the computer.

7.5. GRAPHIC DISPLAY UNIT

The computer has a graphic display unit situated at device address 01_8 and controlled by a synchronous control interface which accesses the C-bus directly. A graphic display unit was provided at the terminal. Because direct access to the C-bus was not available, an asynchronous controller operating off the E-bus controlled the unit. The device address was 05_8.

* * *

APPENDIX 1

THE PHYSICAL AND ELECTRICAL ASPECTS OF THE VARIAN 620I INPUT/OUTPUT STRUCTURE [17, 18]

The Varian 620I input-output structure provides an interface between the computer and peripheral devices that are connected to for the purposes of data transfers into and out of the computer. It is a party line time sharing system with two structural elements accessed by external controllers.

[1] A set of 16 bi-directional lines (EB00 through EB15) called the E-bus. These 16 lines are essentially the date lines and are used for:

(a) transfer of operands
(b) peripheral device addresses
(c) memory location addresses
(d) peripheral control codes
(e) peripheral sense codes

[2] A set of ten individual control lines that:

(a) indicate the type of information present on E-bus lines
(b) provide timing and synchronisation of data transfers between the central processor unit and peripheral controllers
(c) initiate a specific action or sequence on the part of the CPU or controllers

The E-bus lines are bi-directional; the control lines are uni-directional, directing signals either to or from the CPU. All the outputs of the lines follow the negative logic convention with TTL open collector drivers on the line, allowing a party system.

INPUT/OUTPUT MODES OF OPERATION

There are three basic modes of operation for the input-output system.

[1] Programmed input-output operations as a result of instructions written into the computer programme. Four types of input-output operation can be performed under programme control.

(a) External control. An external control code is transmitted under programme control from the computer to a peripheral.

(b) Programme sense. The status of a selected peripheral sense line is interrogated by the computer.

(c) Single word input transfer. A 16-bit word is transferred from a peripheral to the A or B registers or directly to memory.

(d) Single word output transfer. A 16-bit word is transferred to a peripheral from either the A or B registers or directly from memory.

[2] Interrupt initiated input-output operations are equivalent to programmed input-output operations except that they are initiated by a request generated by a peripheral. An interrupt branches the programme to a memory address location that generally contains a jump and mark instruction. This directs the programme to an input-output routine.

[3] Cycle stealing input-output. Trap requests for direct memory access are generated by a peripheral and are equivalent to the interrupt requests except that they inhibit the progress of the main programme for only 2,7 microseconds required to transfer a word of data directly between memory and the peripheral device. A peripheral signalling on the TPIX line is requesting a DMA of one word into the computer. A signal on the TPOX line indicates a DMA out of the computer.

PROGRAMMED INPUT/OUTPUT IN DETAIL

External control This is used to initiate a specific mode of operation in a peripheral device. The EXC input-output timing is shown in Figure 2.2. Signal lines EB00 through EB05 contain the device address. EB06 through EB08 indicate the function code. EB11 and FRYX identify it as an EXC instruction.

Programme sense (SEN) The programme sense instruction is used to test the status of a specific device condition. The SEN instruction has EB00 through EB05 contain the device address, EB06 through EB08 the function code to be sensed. EB12 and FRYX identify the instruction as a sense. The peripheral indicates the status of the function being sensed via control line SERX. Figure 2.3. illustrates the sense timing.

Single word input transfer The execution of an input transfer instruction is a two phased operation. The first phase selects the peripheral device controller that is to participate in the second phase data transfer. During the first phase, the computer places the device address on lines EB00 through EB05. EB13 and FRYX are used to identify the instruction and to indicate the first phase. The selected peripheral places the data on the E-bus lines and it is entered by a pulse on the DRYX line during the second phase of the operation. Figure 2.4. shows the timing.

Single word output transfer The execution of an output command is a two phased operation similar to that of the input instruction, except that during the first phase it is is EB14 and FRYX that identify the instruction being executed, and during the second phase it is the computer that places data on the E-bus. Figure 2.4. shows the timing.

INTERRUPT STRUCTURE IN DETAIL

Three of the control lines are capable of interrupting or inhibiting the programme being processed by the CPU. The three lines are: IURX (interrupt request), TPIX (trap-in request) and TPOX (trap-out request). The three are similar in that

[1] The computer responds to all three by an IUAX (interrupt acknowledge) signal.
[2] In each case, a memory location address must be placed on the E-bus for the computer to process the request.

The IURX request branches the programme to the interrupt address. The TPIX and TPOX trap requests direct the computer to transfer data to or from the memory.

The IURX interrupt can in theory be generated by any controller or peripheral connected to the E-bus, but in practice, interrupting on IURX to alter a programme flow is done through the priority interrupt module (PIM).

The PIM provides eight interrupt lines for access by peripheral devices, with each line having an assigned priority. Any peripheral can now initiate an interrupt by setting one of these lines low. The PIM then generates the IURX interrupt request and the memory address. The peripheral does not have any part to play in this beyond initiating the interrupt.

For a direct memory access transfer of data in or out of the computer, the peripheral controller initiates a TPIX or TPOX trap request on the trailing edge of the interrupt clock IUCV. When the interrupt acknowledge (IUAX) has been received from the computer, the peripheral places the memory address on the E-bus. This completes the first phase of the cycle stealing input-output transfer.

The second phase is the transfer of date directly to or from memory on the E-bus. The memory location accessed during the operation is that of the memory address placed on the E-bus during the first phase. The timing is shown in Figures 2.6 and 2.7.

To summarise, the structure of the input-output system consists of:

[1] 16 lines, EB00 through EB15 for data transfers
[2] Control lines:
   (a) FRYX indicates the address phase
   (b) DRYX indicates the data phase
   (c) SERX monitors controller's response to a sense instruction
   (d) SYRT is used to initialise peripherals
   (e) IUCX is a 1,1 MHz clock
   (f) IURX is an interrupt request
   (g) IUAX acknowledges the receipt of an interrupt request, trap-out or trap-in
   (h) TPIX trap-in request
   (i) TPOX trap-out request
[3] 8 interrupt lines

THE INPUT/OUTPUT CHASSIS

The input-output expansion chassis has a number of parallel slot positions with their backplanes wired such that a card inserted into any one of the slots has access to the full set of input-output data and control lines. Any external device gains access to this structure through cards inserted into these slot positions. Typically these cards will be printed circuit boards with control logic for the more standard peripheral devices. A second form of card is the Varian interface board. This board contains a number of positions for either fourteen or sixteen pin wirewrap sockets and has ± 5 V and ± 12 V extended around the board. It is on this board, with its layout flexibility, that design interfaces are done.

* * *

APPENDIX 2

DATA ON THE SN75 110 DUAL LINE DRIVER AND THE SN75 107 DUAL LINE RECEIVER.

Extracted from the Texas Instruments Integrated Circuits catalogue,1971.

logic

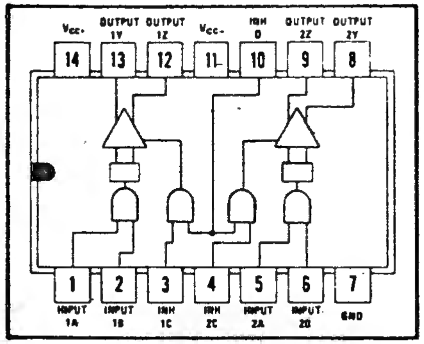
TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state

SN55109, SN55110 J DUAL-IN-LINE PACKAGE
SN75109, SN75110 J OR N DUAL-IN-LINE PACKAGE



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (See Note 1) . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . −7 V
Logic and inhibitor input voltages (See Note 1) . . . . 5.5 V
Common-mode output voltage (See Note 1) . . . . −5 to 12 V
Operating free-air temperature range, Series 55 . . . . −55°C to 125°C
Series 75 . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . −65°C to 150°C

recommended operating conditions (see note 2)

	SN55109, SN55110			SN75109, SN75110			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
[redacted]mon-mode output voltage (See Note 1)	0		10	0		10	V
Negative common-mode output voltage (See Note 1)	0		−3	0		−3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to the network ground terminal.
2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

definition of input logic levels†

		TEST FIGURE	MIN	MAX	UNIT
V_{IH}	High-level input voltage at any input	16, 17	2	5.5	V
V_{IL}	Low-level input voltage at any input	16, 17	0	0.8	V

†The algebraic convention where the most-positive (least negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

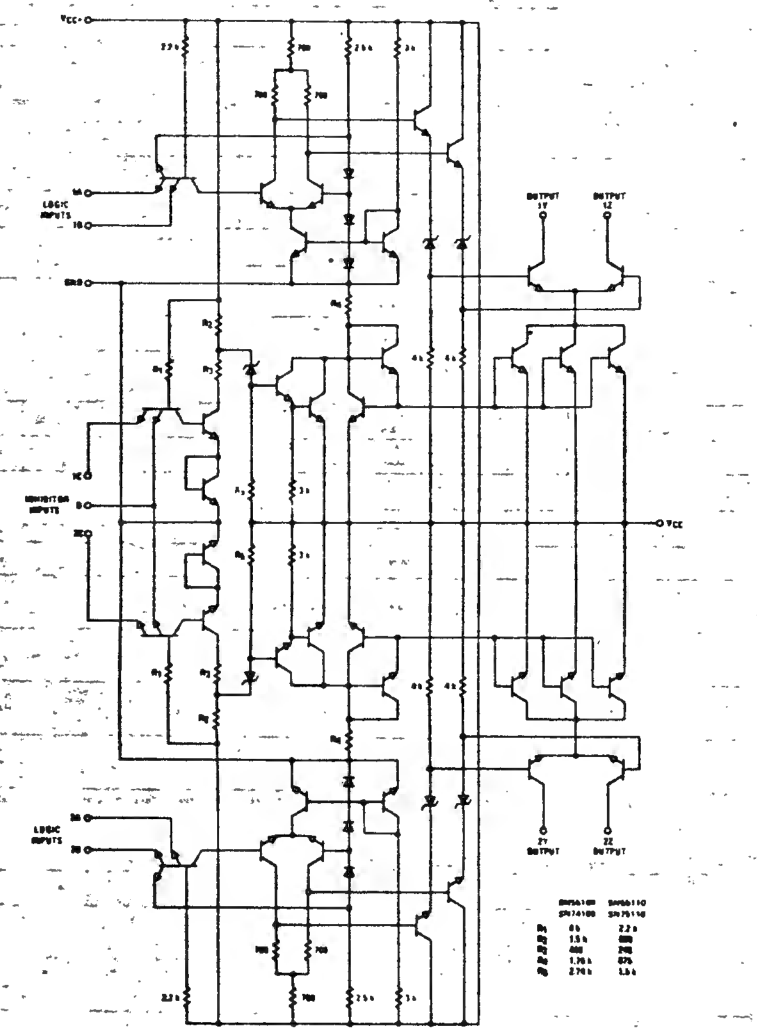
PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55109, SN75109			SN55110, SN75110			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
$I_{IH(L)}$	High-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IH(L)}$ = 2.4 V	V_{CC-} = MAX,			40			40	µA
			V_{CC+} = MAX, $V_{IH(L)}$ = MAX V_{CC+}	V_{CC-} = MAX			1			1	mA
$I_{IL(L)}$	Low-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IL(L)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			40			40	µA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
$I_{IL(I)}$	Low-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into D	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			80			80	µA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
$I_{IL(I)}$	Low-level input current into D	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−6			−6	mA
$I_{O(on)}$	On-state output current	18	V_{CC+} = MAX,	V_{CC-} = MAX			7			15	mA
			V_{CC+} = MIN	V_{CC-} = MAX	3.5			6.5			mA
$I_{O(off)}$	Off-state output current	18	V_{CC+} = MIN	V_{CC-} = MIN			100			100	µA
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		18	30		23	35	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		−18	−30		−34	−50	mA
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		18			21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		−10			−17		mA

‡For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation delay time, low-to-high level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation delay time, high-to-low level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		13	25	ns

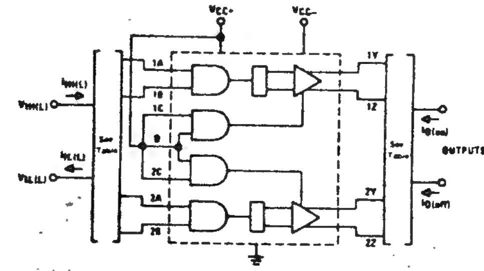
schematic



NOTES: 1. Component values shown are nominal.
2. Resistance values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

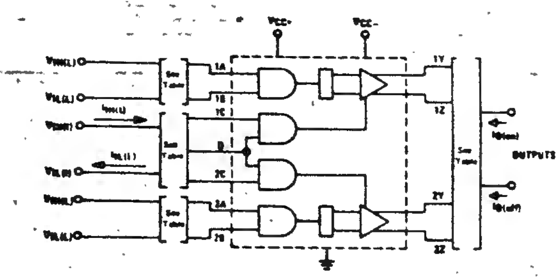


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(L)}$	Open	$V_{IH(I)}$	H (See Note 1)	L (See Note 1)
$V_{IL(L)}$	V_{CC+}	$V_{IH(I)}$	L (See Note 1)	H (See Note 1)
$I_{IH(L)}$	Gnd	$V_{IH(I)}$	Gnd	Gnd
$I_{IL(L)}$	4.5 V	$V_{IH(I)}$	Gnd	Gnd

NOTES: 1. Low output represents the on state, high output represents the off state.
2. Each input is tested separately.

FIGURE 16 – $V_{IH(L)}$, $V_{IL(L)}$, $I_{IH(L)}$, and $I_{IL(L)}$



TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
$V_{IH(I)}$	$V_{IH(L)}$	Open	H (See Note 1)	L (See Note 1)
	$V_{IL(L)}$	Open	L (See Note 1)	H (See Note 1)
$V_{IL(I)}$	$V_{IH(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
	$V_{IL(L)}$	V_{CC+}	H (See Note 1)	H (See Note 1)
$I_{IH(I)}$	Gnd	Gnd	Gnd	Gnd
$I_{IL(I)}$	Gnd	4.5 V	Gnd	Gnd

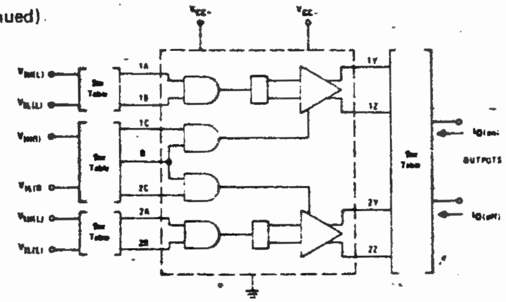
NOTES. 1. Low output represents the on state, high output represents the off state
2. Each input is tested separately.

FIGURE 17 – $V_{IH(I)}$, $V_{IL(I)}$, $I_{IH(I)}$, $I_{IL(I)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

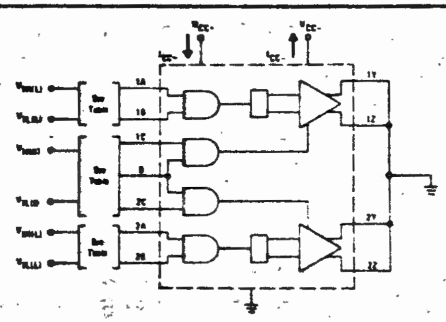
d-c test circuits† (continued)



TEST TABLE

TEST		LOGIC INPUTS 1A or 2A	LOGIC INPUTS 1B or 2B	INHIBITOR INPUTS 1C or 2C	INHIBITOR INPUTS D
$I_{O(on)}$	at output 1Y or 2Y	[illegible] / [illegible] / [illegible]	[illegible] / [illegible] / [illegible]	[illegible]	[illegible]
$I_{O(on)}$	at output 1Z or 2Z	[illegible]	[illegible]	[illegible]	[illegible]
$I_{O(off)}$	at output 1Y or 2Y	[illegible]	[illegible]	[illegible]	[illegible]
$I_{O(off)}$	at output 1Z or 2Z	[illegible] / [illegible] / [illegible]	[illegible] / [illegible] / [illegible]	[illegible]	[illegible]
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	[illegible] / [illegible] / [illegible]	[illegible] / [illegible] / [illegible]

FIGURE 18 – $I_{O(on)}$ and $I_{O(off)}$



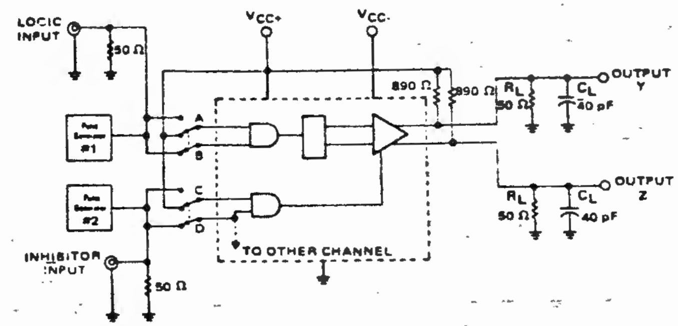
TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC+(on)}$	Driver enabled	[illegible]	[illegible]
$I_{CC-(on)}$	Driver enabled	[illegible]	[illegible]
$I_{CC+(off)}$	Driver inhibited	[illegible]	[illegible]
$I_{CC-(off)}$	Driver inhibited	[illegible]	[illegible]

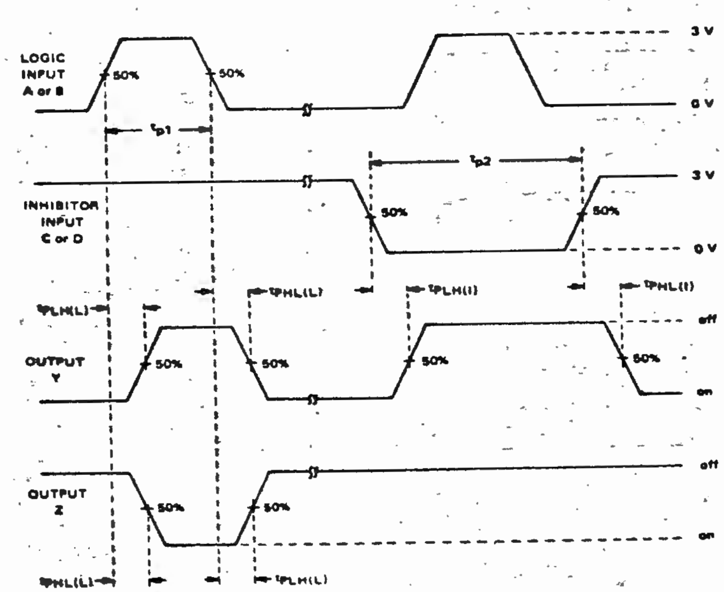
FIGURE 19 – I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: $Z_{out} = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 20–PROPAGATION DELAY TIMES

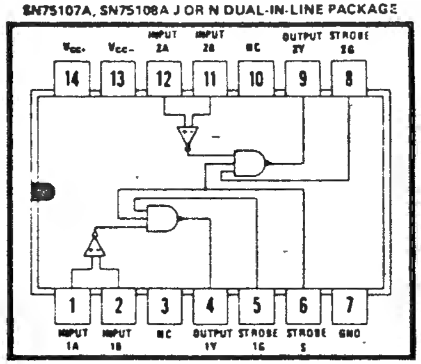
A2 - 4

logic

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

SN55107A, SN55108A J DUAL-IN-LINE PACKAGE
SN75107A, SN75108A J OR N DUAL-IN-LINE PACKAGE



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

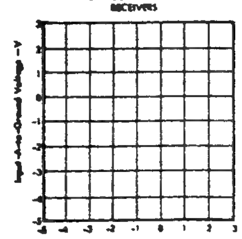
Supply voltage V_{CC+} (See Note 1) .... 7 V
Supply voltage V_{CC-} (See Note 1) .... −7 V
Differential input voltage (See Note 2) .... ±6 V
Common-mode input voltage (See Note 1) .... ±5 V
Strobe input voltage (See Note 1) .... 5.5 V
Operating free-air temperature range, Series 55 .... −55°C to 125°C
Series 75 .... 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package .... −65°C to 150°C
plastic dual-in-line (N) package .... −65°C to 150°C

recommended operating conditions (see note 3)

	SN55107A, SN55108A MIN	NOM	MAX	SN75107A, SN75108A MIN	NOM	MAX	UNIT
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Output sink current			−16			−16	mA
Differential input voltage (See Notes 2 and 4)	−5†		5	−5†		5	V
Common-mode input voltage (See Notes 1 and 4)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (See Note 4)	−5†		3	−5†		3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. When using only one channel of the line receiver, the inputs of the other channel should be grounded.
4. The recommended combinations of input voltages fall within the shaded area of the figure at the right.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS



†The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

definition of input logic levels†

	TEST FIGURE	MIN	MAX	UNIT
V_{IDH} High level input voltage between differential inputs	1	0.025	5	V
V_{IDL} Low level input voltage between differential inputs	1	5	−0.025	V
$V_{IH(S)}$ High level input voltage at strobe inputs	3	2	5.5	V
$V_{IL(S)}$ Low-level input voltage at strobe inputs	3	0	0.8	V

†The algebraic convention where the most positive (least-negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

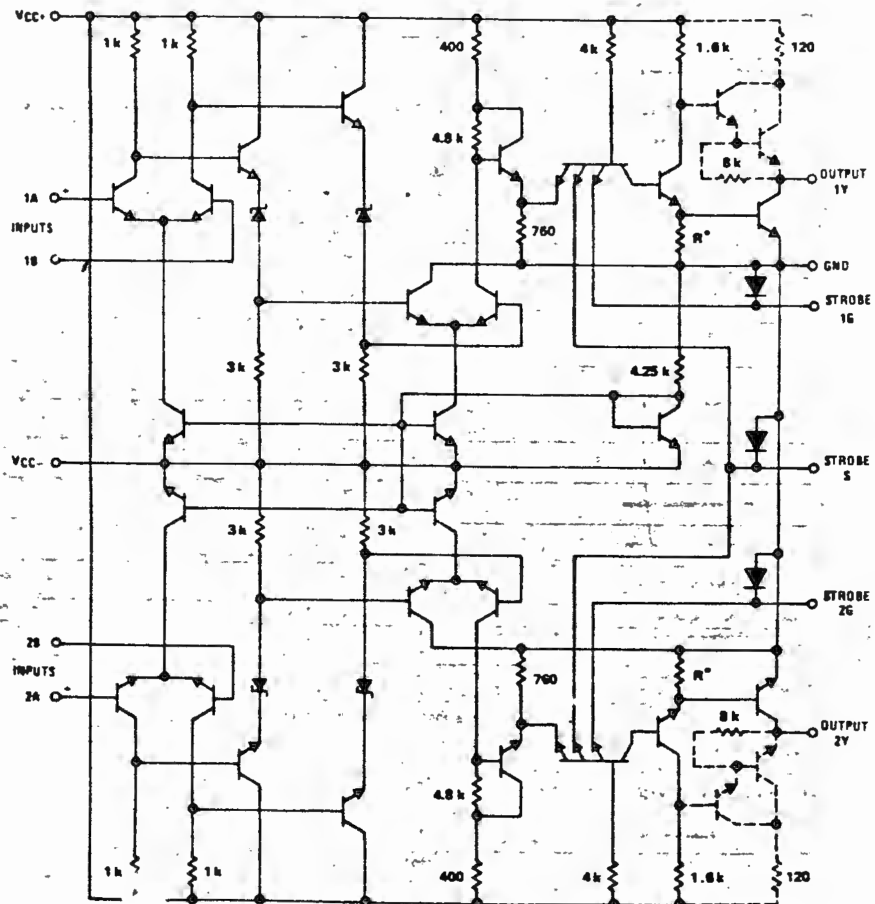
PARAMETER		TEST FIGURE	TEST CONDITIONS‡		SN55107A, SN75107A MIN	TYP§	MAX	SN55108A, SN75108A MIN	TYP§	MAX	UNIT
I_{IH}	High-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = 0.5 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V		30	75		30	75	µA
I_{IL}	Low-level input current into 1A or 2A	2	V_{CC+} = MAX, V_{ID} = −2 V,	V_{CC-} = MAX, V_{IC} = −3 V to 3 V			−10			−10	µA
I_{IH}	High-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			40			40	µA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
I_{IL}	Low-level input current into 1G or 2G	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−1.6			−1.6	mA
I_{IH}	High-level input current into S	4	V_{CC+} = MAX, $V_{IH(S)}$ = 2.4 V	V_{CC-} = MAX,			80			80	µA
			V_{CC+} = MAX, $V_{IH(S)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
I_{IL}	Low-level input current into S	4	V_{CC+} = MAX, $V_{IL(S)}$ = 0.4 V	V_{CC-} = MAX,			−3.2			−3.2	mA
V_{OH}	High-level output voltage	3	V_{CC+} = MIN, I_{load} = −400 µA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage	3	V_{CC+} = MIN, I_{sink} = 16 mA,	V_{CC-} = MIN, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current	3	V_{CC+} = MIN, V_{OH} = MAX V_{CC+}	V_{CC-} = MIN,						250	µA
I_{OS}	Short-circuit output current¶	5	V_{CC+} = MAX,	V_{CC-} = MAX	−18		−70				mA
I_{CCH+}	High logic level supply current from V_{CC+}	6	V_{CC+} = MAX, V_{ID} = 25 mV,	V_{CC-} = MAX, T_A = 25°C		18	30		18	30	mA
I_{CCH-}	High-logic-level supply current from V_{CC-}	6	V_{CC+} = MAX, V_{ID} = 25 mV	V_{CC-} = MAX, T_A = 25°C		−8.4	−15		−8.4	−15	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN55107A, SN75107A MIN	TYP	MAX	SN55108A, SN75108A MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low level, from differential inputs A and B to output	7	R_L = 390 Ω,	C_L = 50 pF		17	25				ns
			R_L = 390 Ω,	C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		10	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low level, from strobe input G or S to output	7	R_L = 390 Ω,	C_L = 50 pF		8	15				ns
			R_L = 390 Ω,	C_L = 15 pF					13	20	

schematic

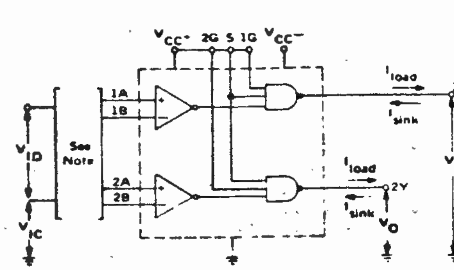


R^* = 1 kΩ for SN5510 . SN75107A, 750 Ω for SN55108A and SN75108A.

NOTES
1. Components .alues shown are nominal.
2. Resistance values are in ohms.
3. Components shown with dashed lines are applicable to the SN55107A and SN75107A only.

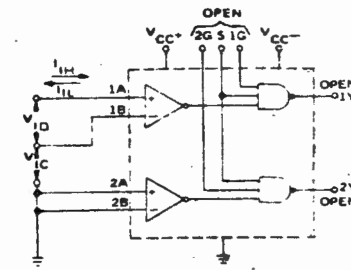
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



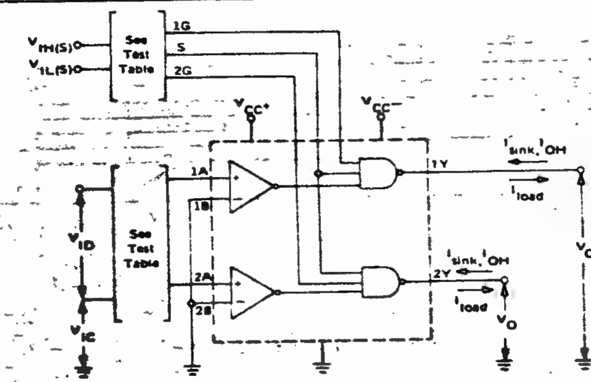
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 1 – V_{IOH} and V_{IDL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 2 – I_{IH} and I_{IL}



TEST TABLE

SN55107A SN75107A	SN55108A SN75108A	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{OH}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	+25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	[illegible]	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

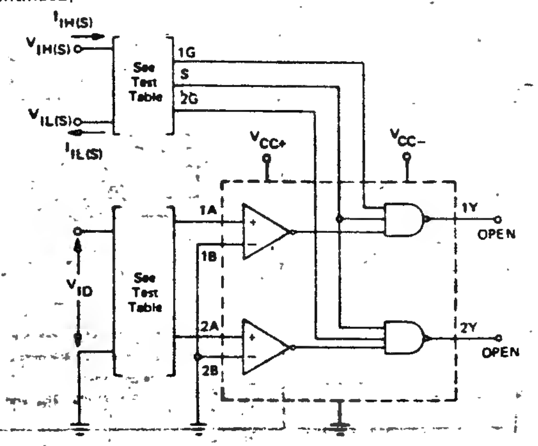
NOTES:
1. V_{IC} = -3 V to 3 V.
2. When testing one channel, the inputs of the other channel should be grounded.

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}

† Arrows indicate actual direction of current flow

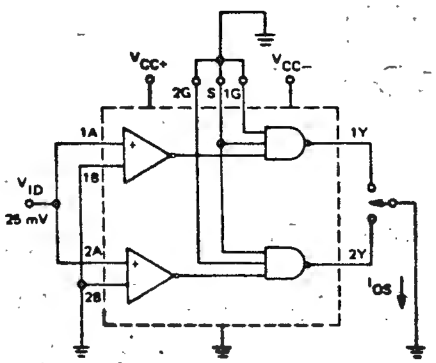
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	- 25 mV	25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be grounded at a time.

FIGURE 5—I_{OS}

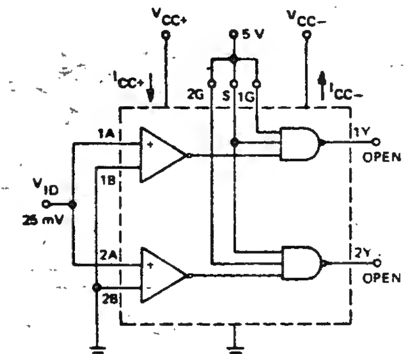
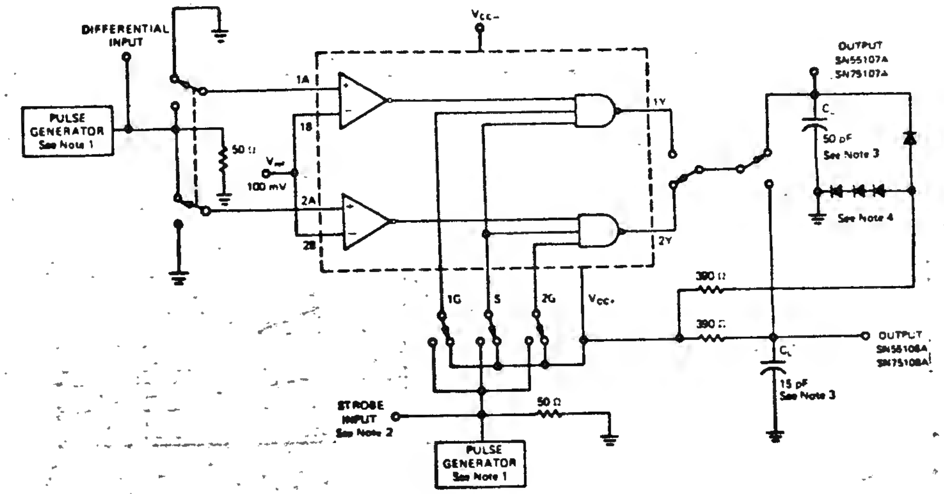


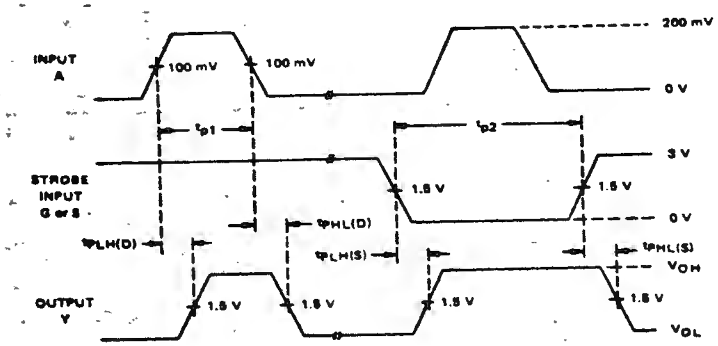
FIGURE 6—I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: $Z_{out} = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A 2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

FIGURE 7—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

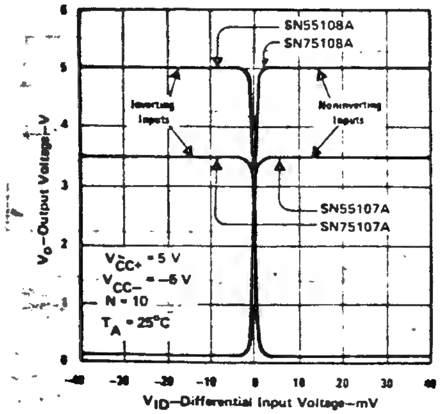


FIGURE 8

HIGH-LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

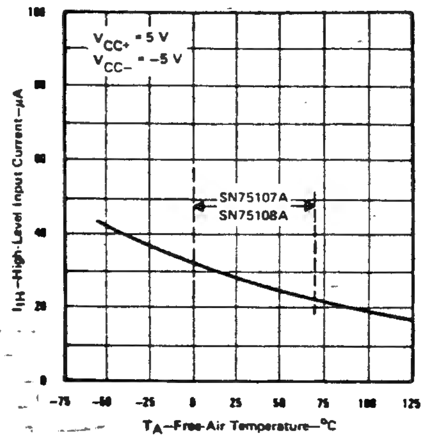


FIGURE 9

HIGH-LOGIC-LEVEL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

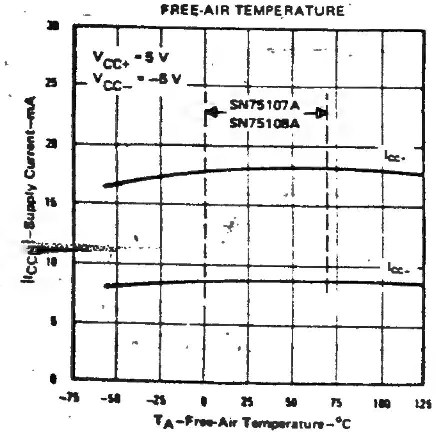


FIGURE 10

SN55107A, SN75107A
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

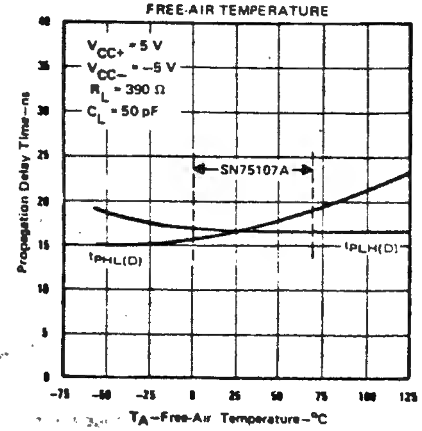


FIGURE 11

TYPICAL CHARACTERISTICS

SN55108A, SN75108A
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

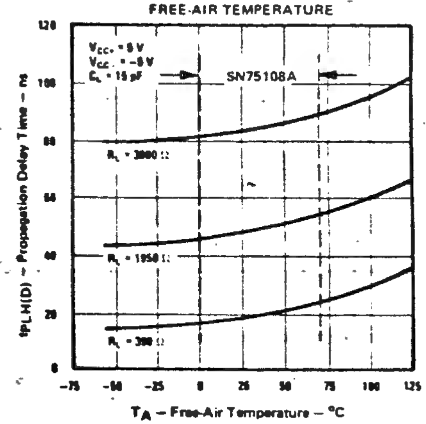


FIGURE 12

SN55108A, SN75108A
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

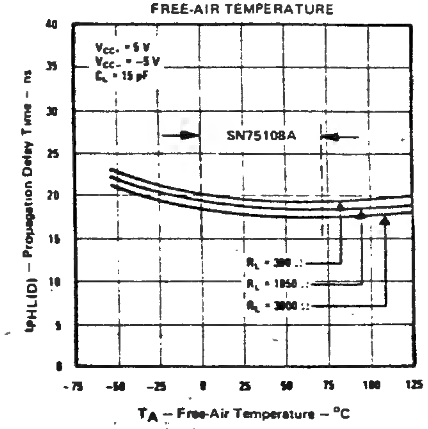


FIGURE 13

SN55107A, SN75107A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

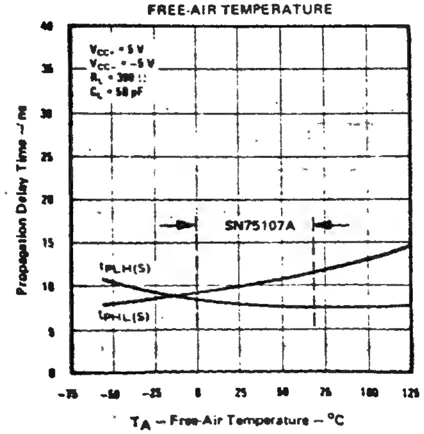


FIGURE 14

SN55108A, SN75108A
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

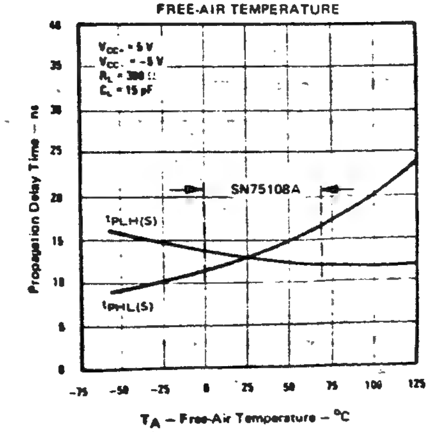


FIGURE 15

TYPICAL CHARACTERISTICS

SN55109, SN75109
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

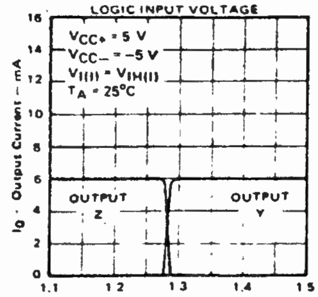


FIGURE 21

SN55110, SN75110
OUTPUT CURRENT
vs
LOGIC INPUT VOLTAGE

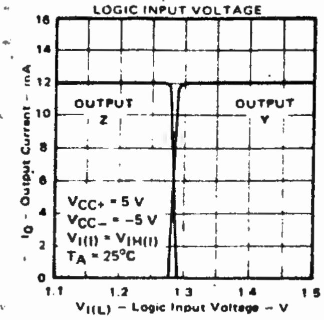


FIGURE 22

SN55109, SN75109
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

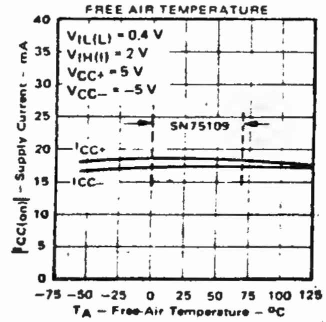


FIGURE 23

SN55110, SN75110
SUPPLY CURRENT WITH DRIVER ENABLED
vs
FREE-AIR TEMPERATURE

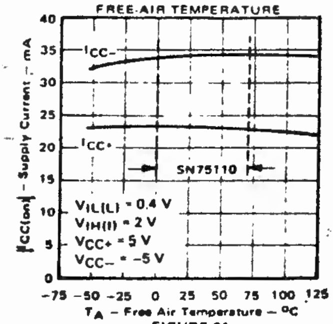


FIGURE 24

PROPAGATION DELAY TIME
(LOGIC INPUTS)
vs
FREE-AIR TEMPERATURE

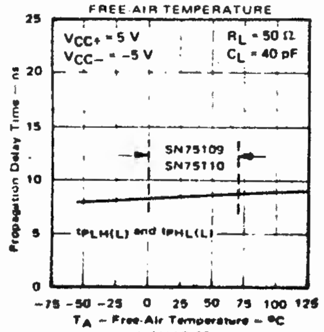


FIGURE 25

PROPAGATION DELAY TIME
(INHIBITOR INPUTS)
vs
FREE-AIR TEMPERATURE

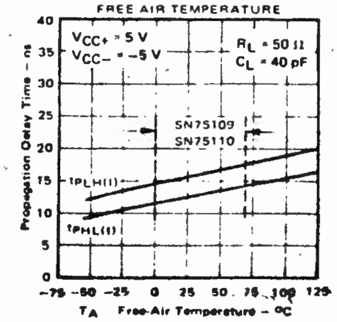


FIGURE 26

APPENDIX 3

CAMAC

"Computer aided measurement and control" is an attempt to standardise data handling equipment. CAMAC is a specification for modular data handling equipment based on standard interfaces to a highway. It was developed by laboratory organisations whose prime interest was in the use of electronics for nuclear research and development and so, while providing one of the fastest commercial systems available, it is restricted to laboratory environments and is an expensive system.

Figure A3.1. shows the schematic of the CAMAC principle. The crate provides a common highway similar in principle to the Varian input-output structure where any peripheral controller can access the data-way information.

<u>The CAMAC system</u> The CAMAC concept allows many channels of inout-output information to be multiplexed in a party line or highway configuration. The CAMAC highway has a 24-bit parallel data path in the read (input to the computer) and write (output from the computer) directions. Each crate can contain up to twenty three peripheral controllers, each accessing the data-way through an 86-way slot position. Each crate has two special slot positions, one of the slots being a data-way, the other being a control path, for the crate controller. The crate controller generally interfaces the local data-ways to the computer and connects together the crate controllers, in each of up to seven crates on a branch highway so that they, too, are multiplexed to the computer. The data transfer operation between a peripheral controller and the crate controller is a fixed time-sequence of events in a manner similar to that of the Varian input-output timing. On the branch highway, similar events adapt themselves to the length of the highway used in each particular operation on the handshake

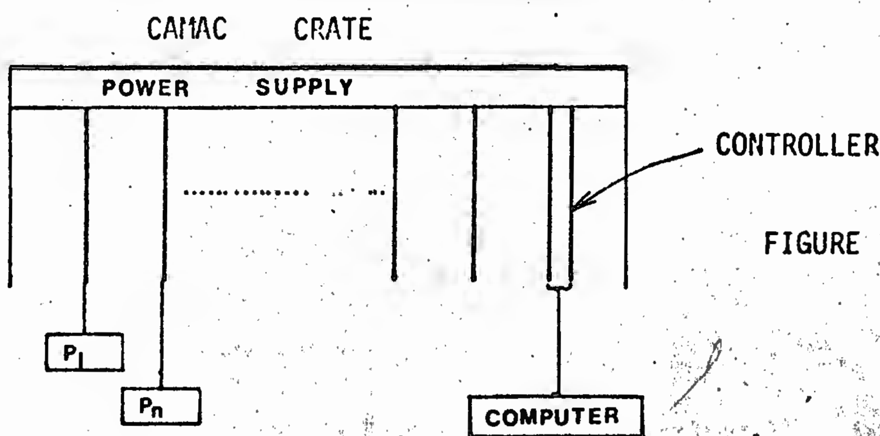


FIGURE A3.1

principle. For branch lines of a couple of metres, twisted pair cables with one side grounded and termination at both ends are used. For branch lines of up to several km, balanced line transmission on a 66 twisted pair cable is being investigated by the South African Atomic Energy Board. A transmission technique similar to the one used in the implementation of this thesis is being investigated, although at the time of writing no results had been published.

Any peripheral controller can have up to sixteen sub-addresses, each of which can be instructed to perform any one of up to 32 functions, or can demand attention by a look-at-me signal (L) from a crate controller. If the controller is in a branch, facilities are provided for grading the L signals into a 24-bit word on the branch highway.

A variant of the normal configuration is to have the computer interfaced as a peripheral device controller rather than through te crate controller. The crate controller now makes double transfers, for example, fetching data from a peripheral into a register in the crate controller and then sending the data out again on the data-way to the computer via the computer interface module. The crate controller is now a more general purpose device not related to the features of the computer used. It is possible for the coupler between the computer and CAMAC to interface the branch highway directly rather than through the CAMAC crate which then has its controller linked to the branch highway. It is in this configuration that a system approaching that desired for research using the Varian 620I is achieved with the computer accessing the CAMAC system via a coupler to the branch highway. For execution of the same operations under computer control typically, information about the required operation is put into the accumulator of the computer and transferred to the controller. The controller executes the operation, say, reads data from the module, and the data is entered into the computer. One direct way of implementing the coupling is to take the input-output bus of the computer to the crate controller. The computer can then organise any CAMAC transfer under programme control. Programme transfers of [illegible] are relatively slow this kind are relatively slow, because the employ instructions to the CPU of the computer.

For greater speed, the controller transfers data between CAMAC and the computer using cycle stealing DMA.

A coupler for the Varian 620 range of computers and a CAMAC crate data-way is available from Borer Products. It allows DMA transfers between any peripheral controller on the branch highway and the computer. The software routines for the data transfers are complex; the computer, accessing the CAMAC crate via the data-way, needs to request priority for each data transfer.

<u>CAMAC and the terminal compared</u> CAMAC's original claim to fame was that for C types of computers and N types of peripherals C x N peripheral device controllers were necessary before CAMAC was introduced. If all computers and peripherals were to be equipped with the same standard input-output interface, then the number of types of interface units would be reduced to N + C. In instances where the choice of computer type is limited, or where a single computer is involved, then C = 1. The computer now has a fixed configuration and the number of controllers required for N peripherals is N. This is the situation with the Varian 620I involved in the research where it was necessary to extend the data capture and controllability of a sophisticated computer system to a point some 200 metres away. Only one computer was involved and perhaps more important, the peripheral device controllers for the standard peripherals as well as device controllers for specialised equipment such as transducers existed before the implementation of the terminal system. In addition, the existing hardware and software for coupling CAMAC to the Varian 620 computer is orientated towards a multiprocessor, multicrate environment with software developed for higher level language use. The economics involved and time spend on reorientation of the researchers' thinking precluded consideration of the CAMAC system.

* * *

APPENDIX 4

WORKING DIAGRAMS

All circuitry at the computer is located on one standard Varian board in slot 5 of the expansion chassis. The board accesses the remainder of the computer through the backplane. The 40-pair cable is connected directly to J1 and J2 on the board.

All circuitry at the terminal is also loacted on one board. Again the cable accesses the board through plugs J1 and J2 while the terminal accesses the board through the backplane.

RUN/STEP AND OVFL INDICATIONS
Run/step is indicated by line HLTX- on pin 070 on the backplane of the Processor 1 card in the computer mainframe. OVFL is derived from the pulse OVXX+ on pin 13 of the card DM 102-8.

MANUAL INTERRUPT
The manual interrupt extended to the terminal is backplane wired from the interface containing the interrupt circuitry to the terminal control card.

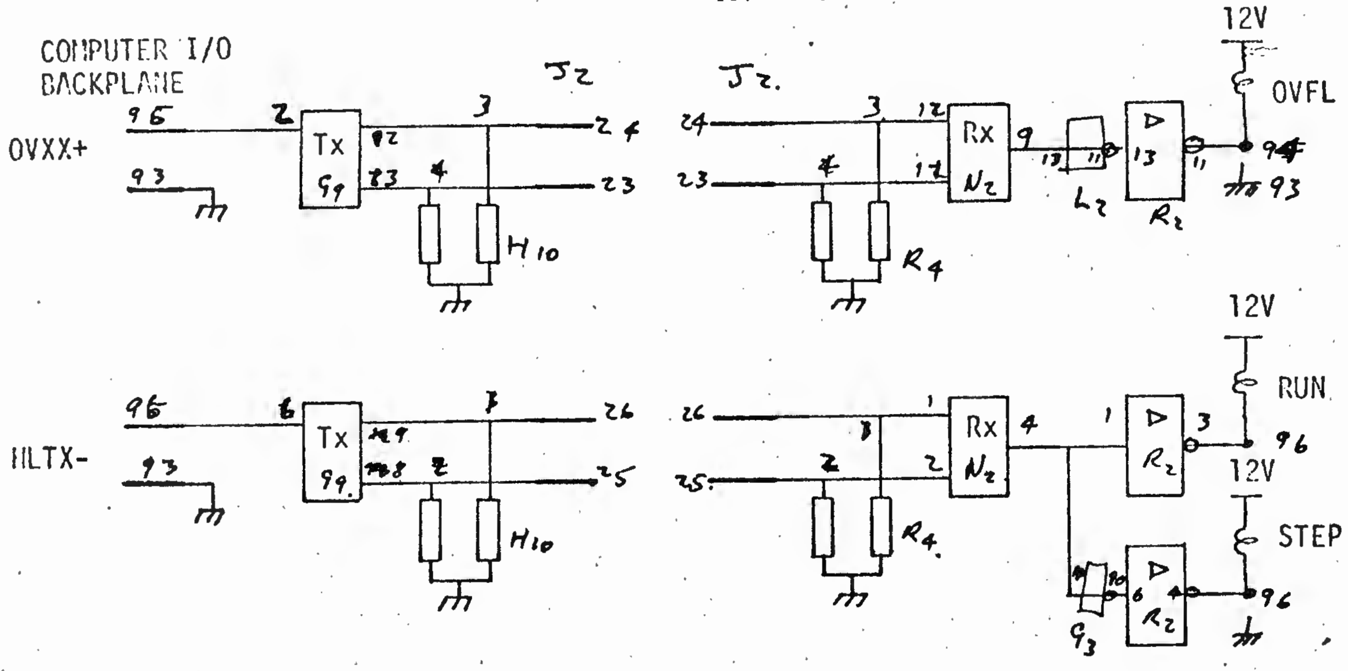
THE CLOCK INHIBIT
The Processor 4 card was modified so that if pin 121 on its backplane is grounded to pin 119, the clock is stopped.

WIRELIST OF THE BACKPLANE OF EACH SLOT POSITION IN THE INPUT/OUTPUT CHASSIS.

1	GRD
2	EB00 -
3	GRD
4	EB01 -
5	GRD
6	EB02 -
7	GRD
8	EB03 -
9	GRD
10	EB04 -
11	EB05 -
12	EB06 -
13	EB07 -
14	EB08 -
15	EB09 -
16	EB10 -
17	EB11 -
18	EB12 -
19	EB13 -
20	EB14 -
21	EB15 -
22	GRD
23	~~EB16 -~~
24	GRD
25	EB17 -
26	GRD
27	FRYX -
28	~~DRYX -~~
29	DRYX -
30	GRD
31	SERX -
32	GRD

33	TPIX-1
34	TPIX-1 (R)
35	TPOX-1XX
36	TPOX-1 (R)
37	
38	GRD
39	
40	GRD
41	
42	
43	SYRT -
44	IUAX -
45	IUCX-
46	
47	
48	
49	TRQX -
50	TROX -
51	GND
52	
53	GRD
54	CDCX -
55	GRD
56	DCEX -
57	GRD
58	TAKX -
59	GRD
60	DESX -
61	
62	

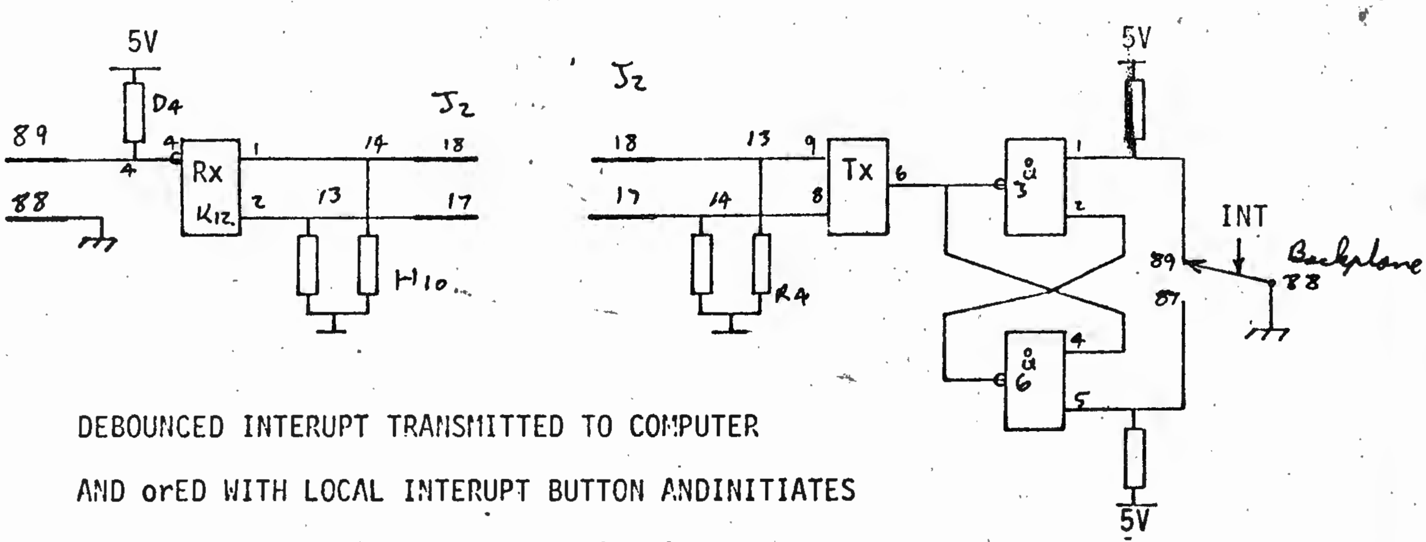
115	nc
116	nc
117	-5V
118	+5V
119	-12V
120	+12V
121	+5V
122	= 100
123	-5V
124	-5V
125	+5V
126	+5V
127	-12V
128	-12V
129	+12V
130	nc



COMPUTER INTERFACE

TERMINAL INTERFACE

COMPUTER STATUS INDICATION

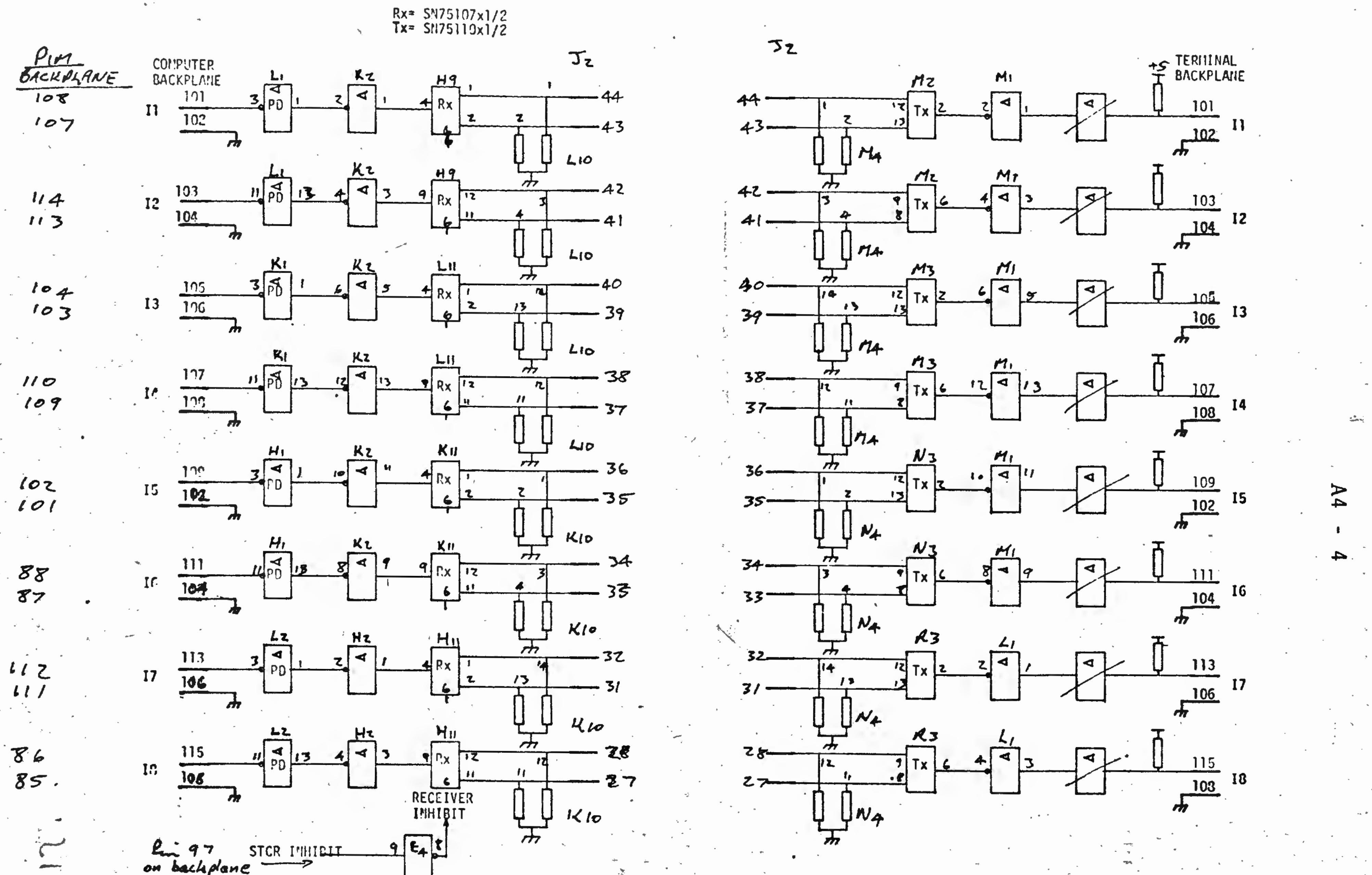


DEBOUNCED INTERUPT TRANSMITTED TO COMPUTER

AND orED WITH LOCAL INTERUPT BUTTON ANDINITIATES

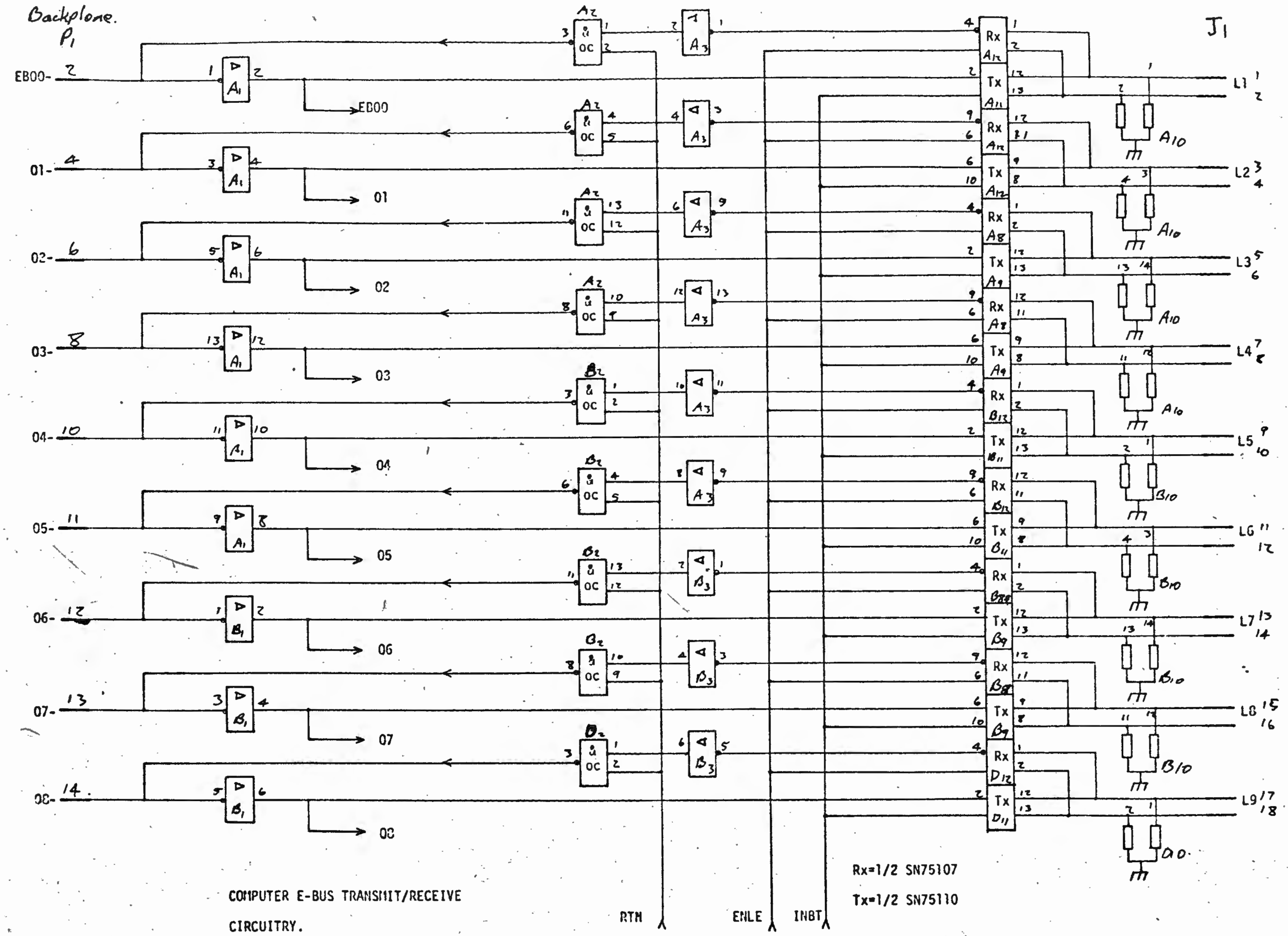
AN INTERUPT TO THE CONTROL PROGRAM, AID.

INTERUPT LINE TO JUMP TO AID EXTENDED TO THE
interrupt line
TERMINAL.

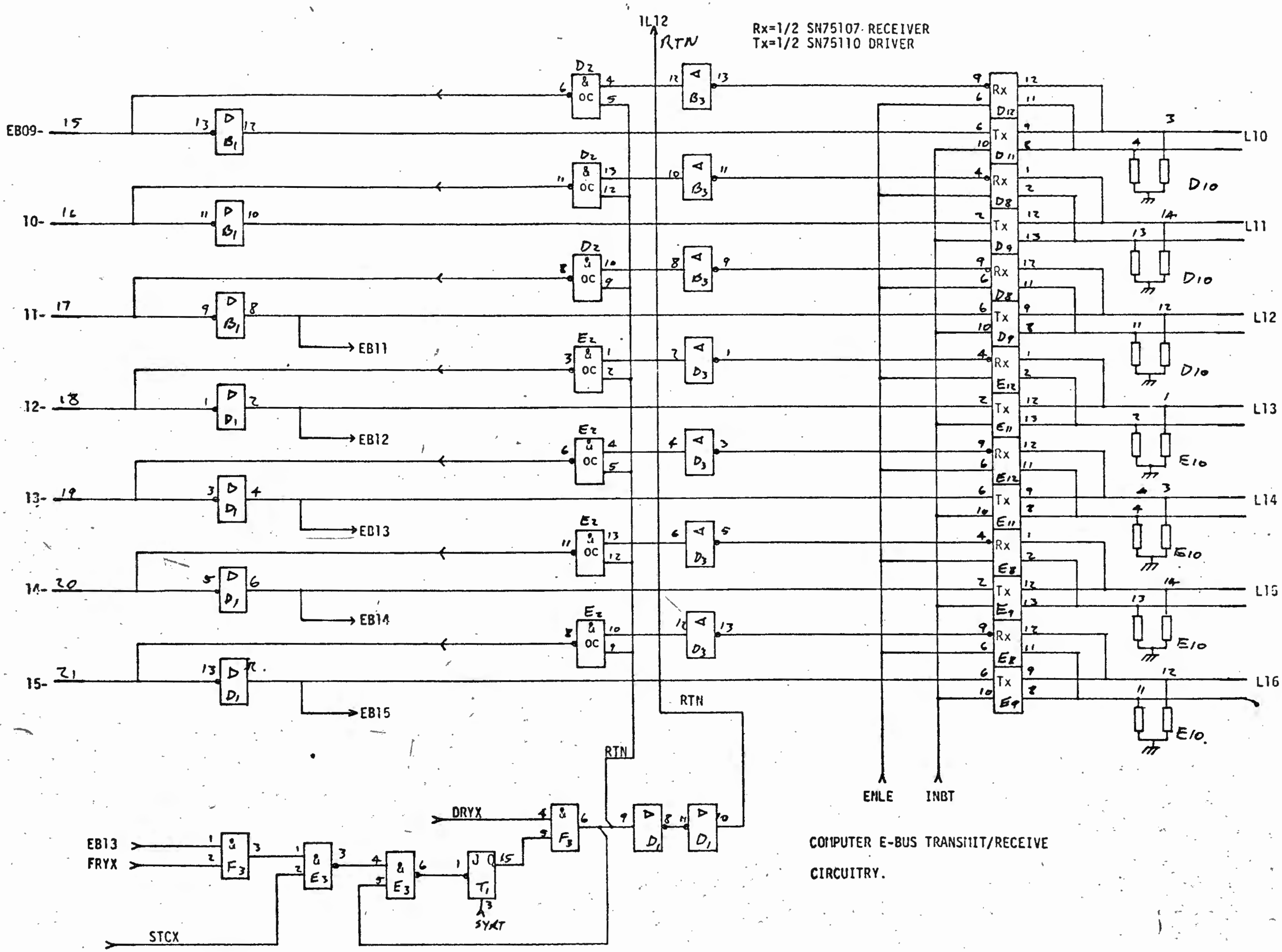


INTERUPT LINES I1 - I8 ARE WIRED ONTO BACKPLANE OF I/O SLOT POSITION FROM BACKPLANE OF THE PIM MODULE IN THE COMPUTER MAINFRAME.THE STCR INHIBIT LINE INHIBITS THE RECEIVERS WHEN LOGICALLY LOW.

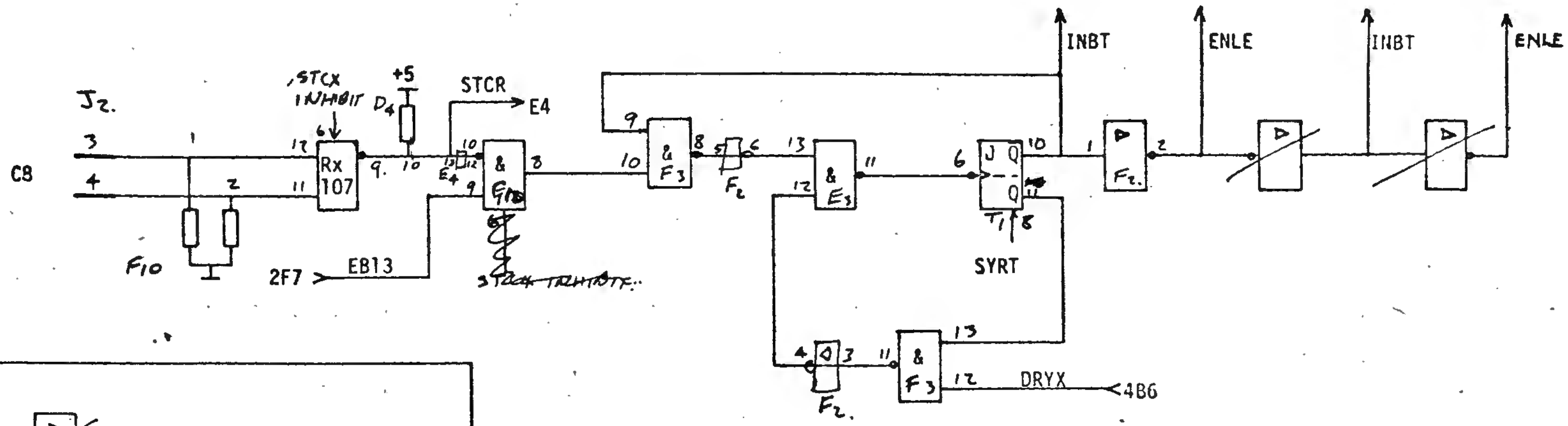
INTERUPT LINES WIRED FROM THE FRONT PANEL OF THE TERMINAL ONTO THE BACKPLANE OF THE TERMINAL I/O CONTROLLER SLOT POSITION AND EXTENDED THROUGH TO THE COMPUTER.



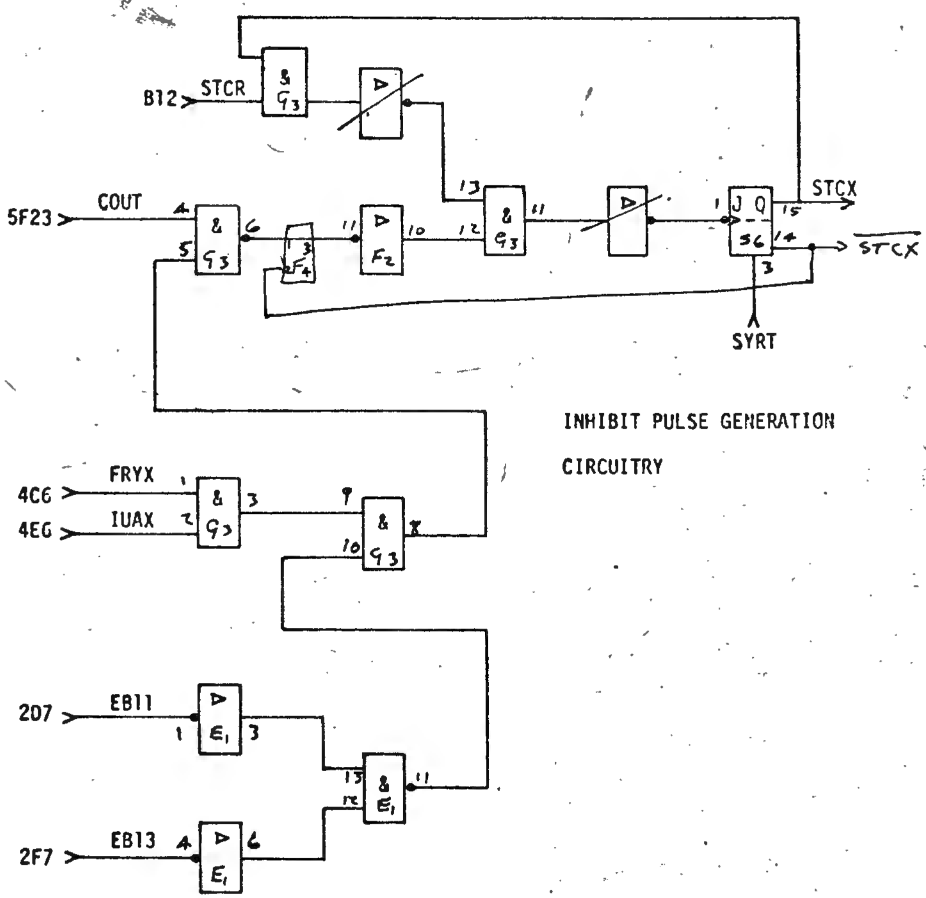
COMPUTER E-BUS TRANSMIT/RECEIVE CIRCUITRY.



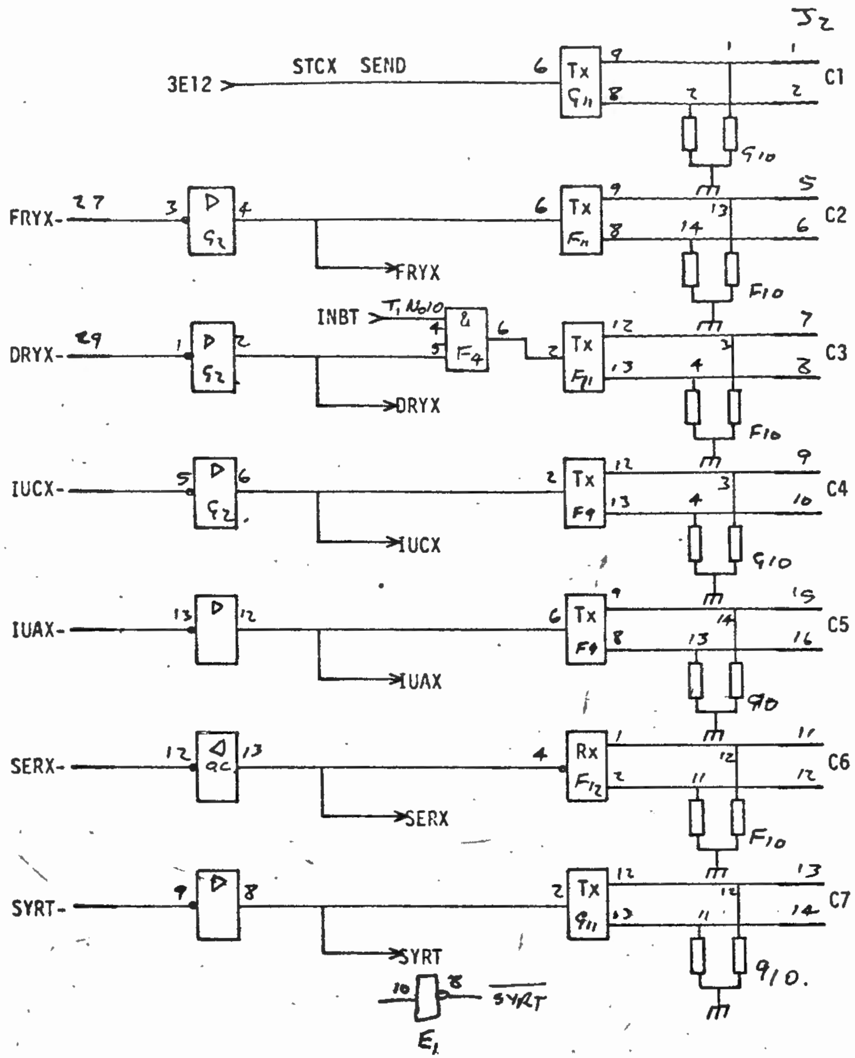
COMPUTER E-BUS TRANSMIT/RECEIVE CIRCUITRY.



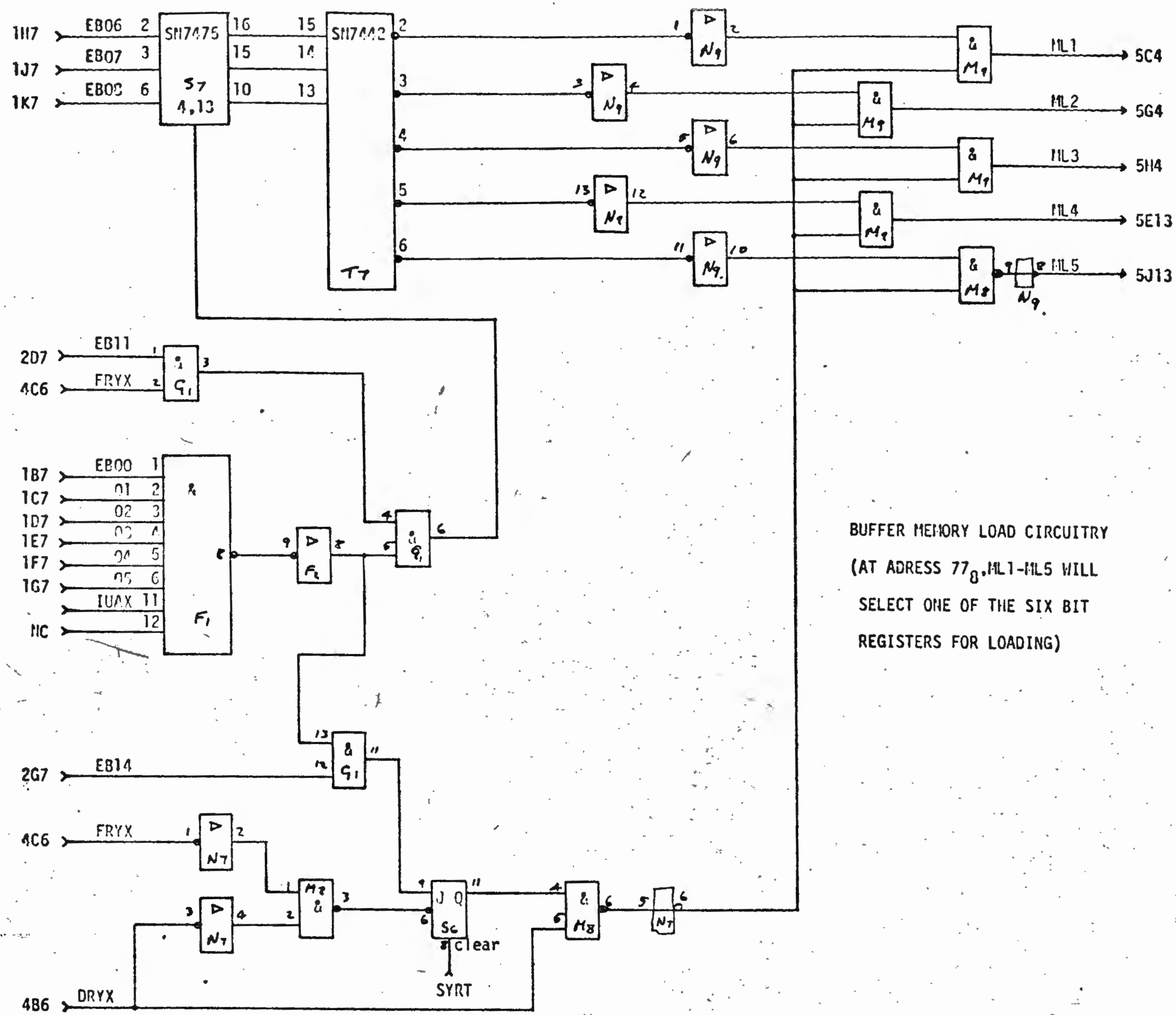
INHIBIT PULSE RECEIVE CIRCUITRY



INHIBIT PULSE GENERATION CIRCUITRY

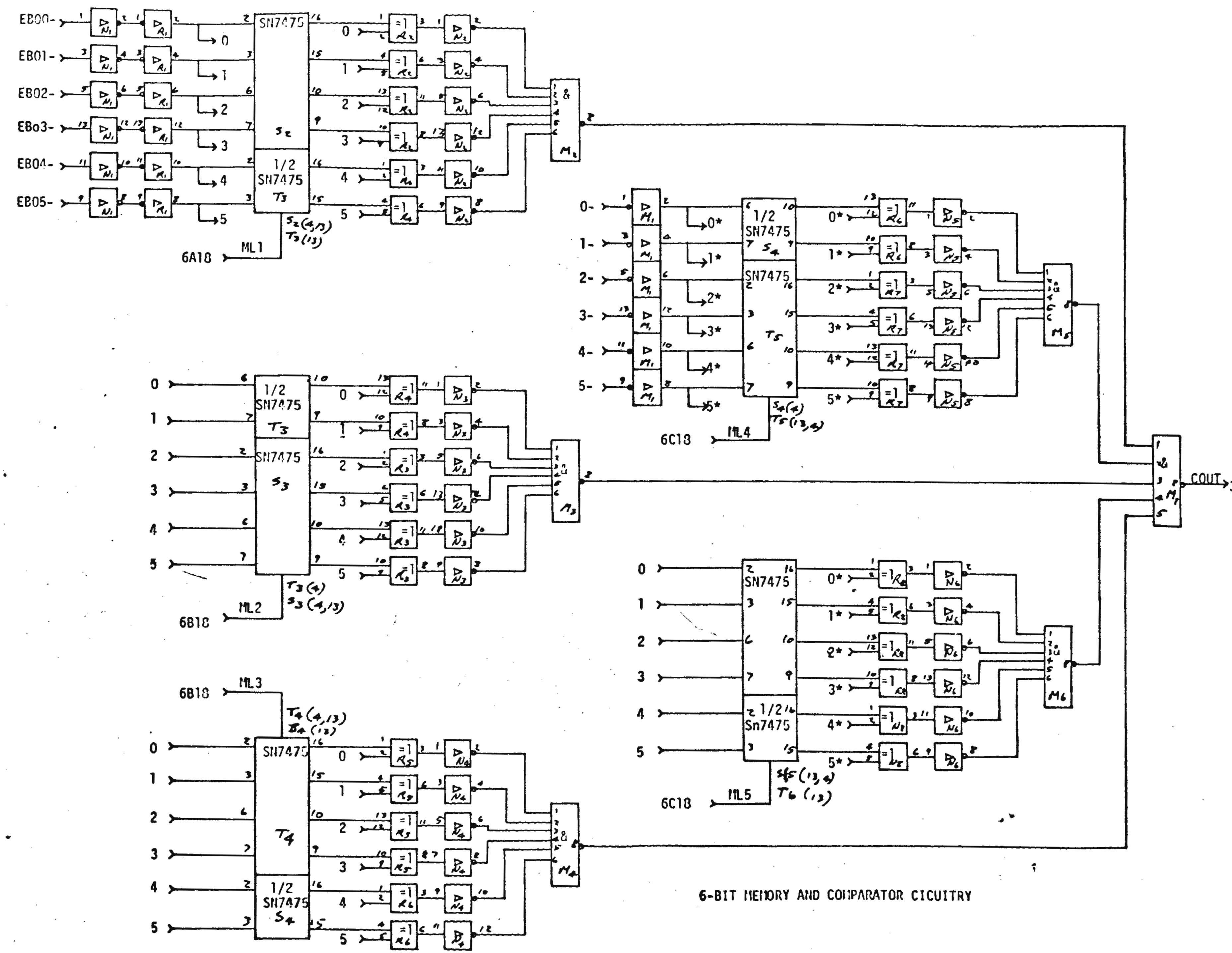


CONTROL LINE TRANSMIT CIRCUITRY

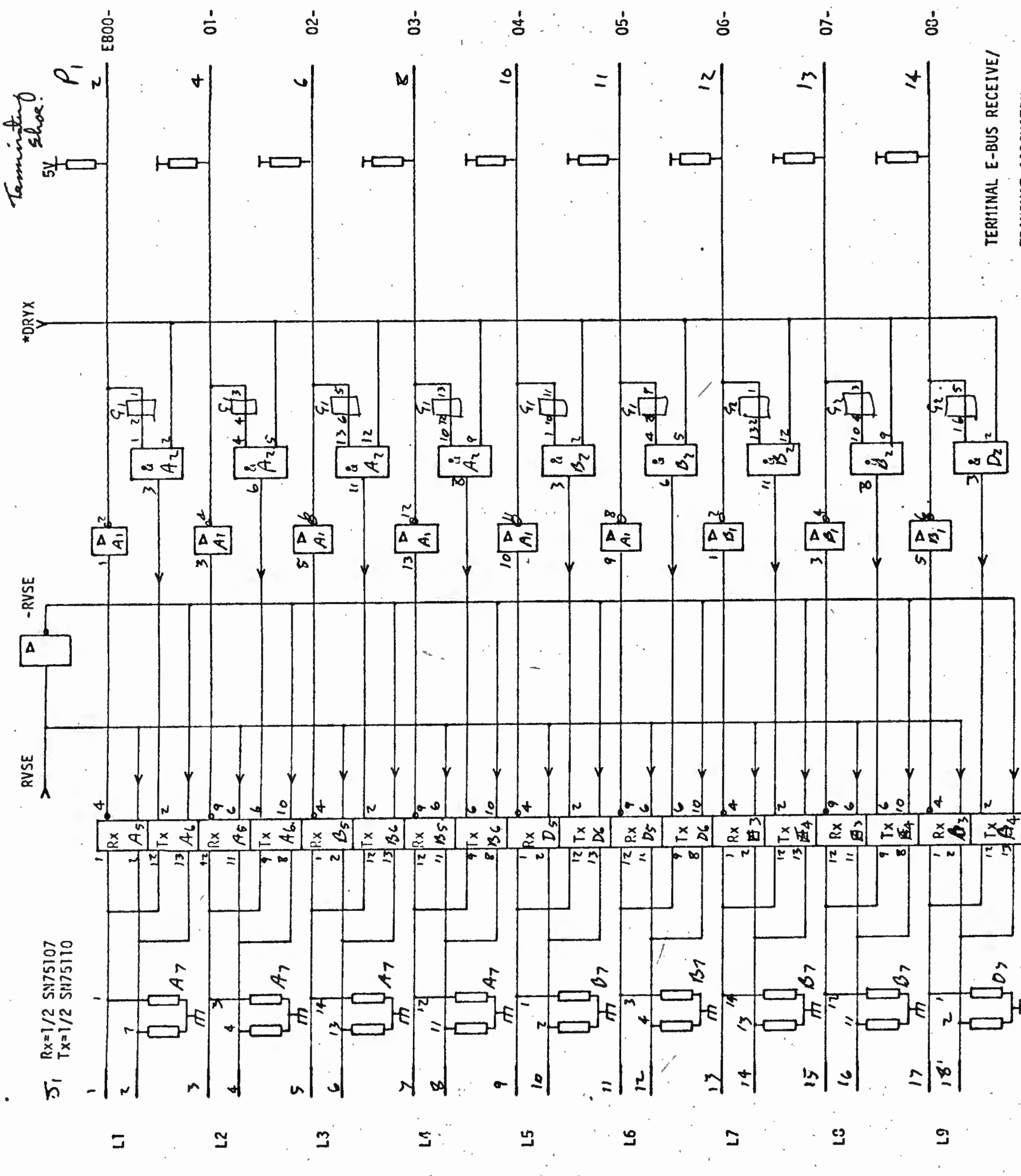


BUFFER MEMORY LOAD CIRCUITRY

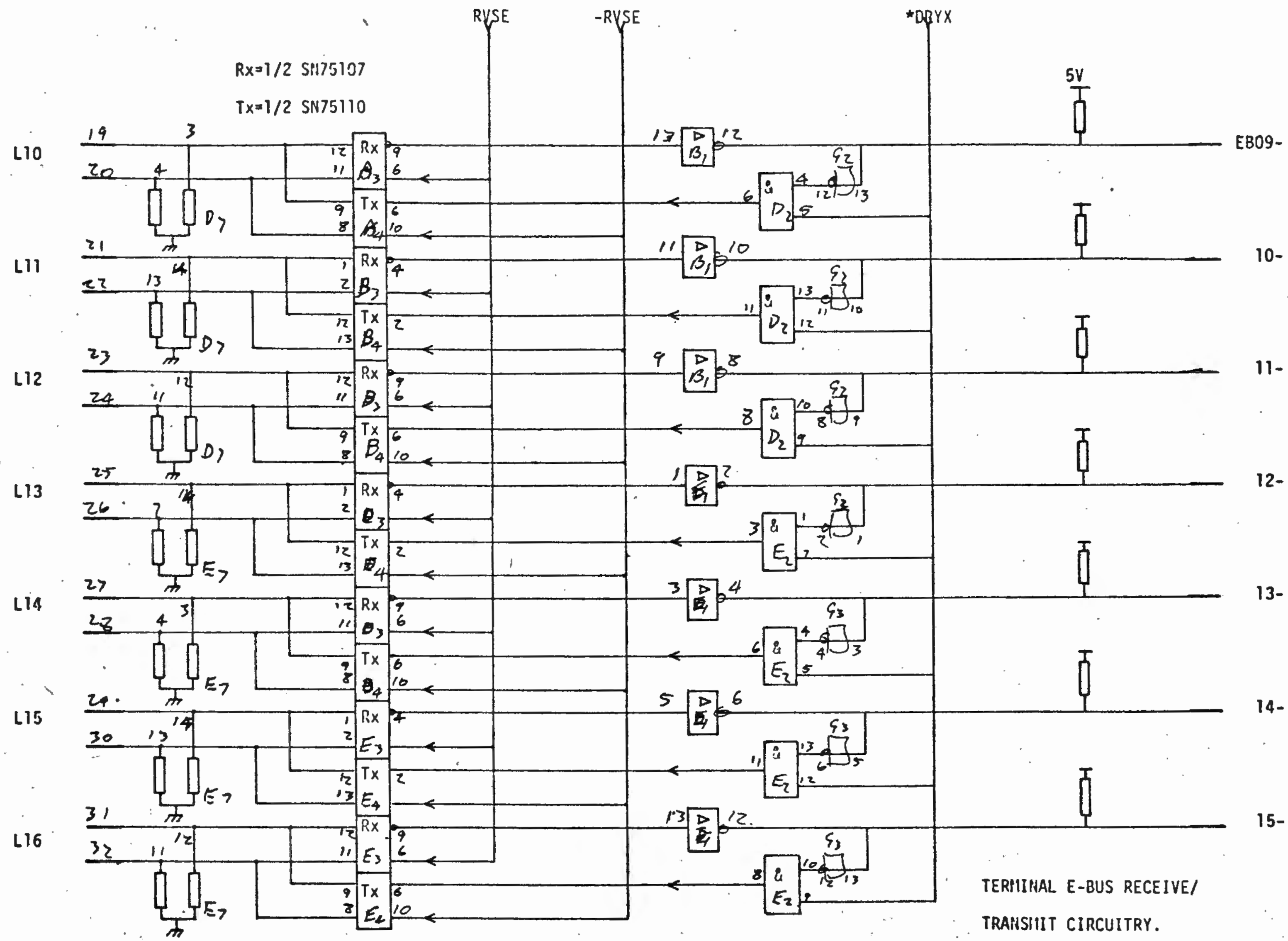
(AT ADRESS 77_8, ML1-ML5 WILL SELECT ONE OF THE SIX BIT REGISTERS FOR LOADING)



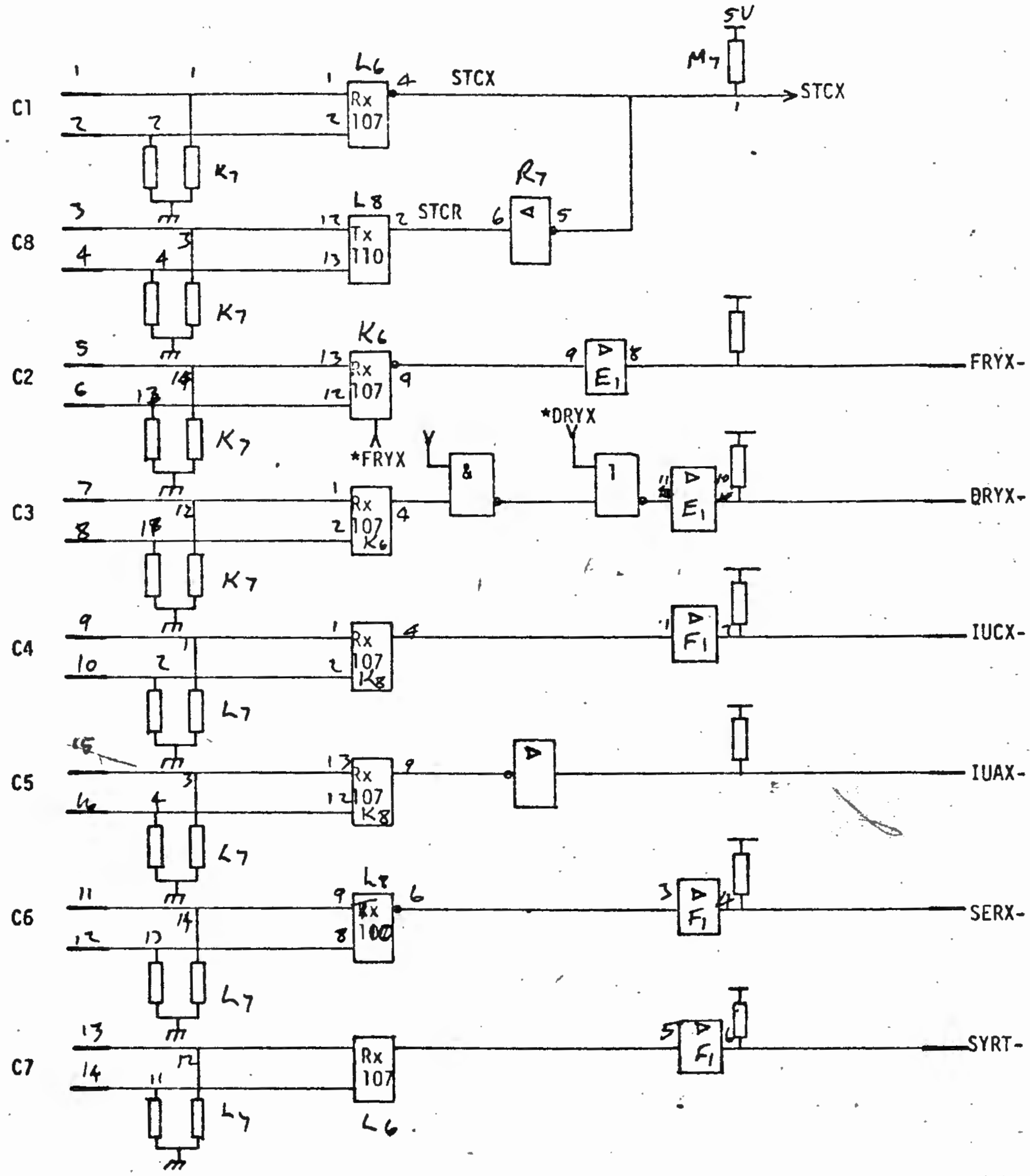
6-BIT MEMORY AND COMPARATOR CICUITRY



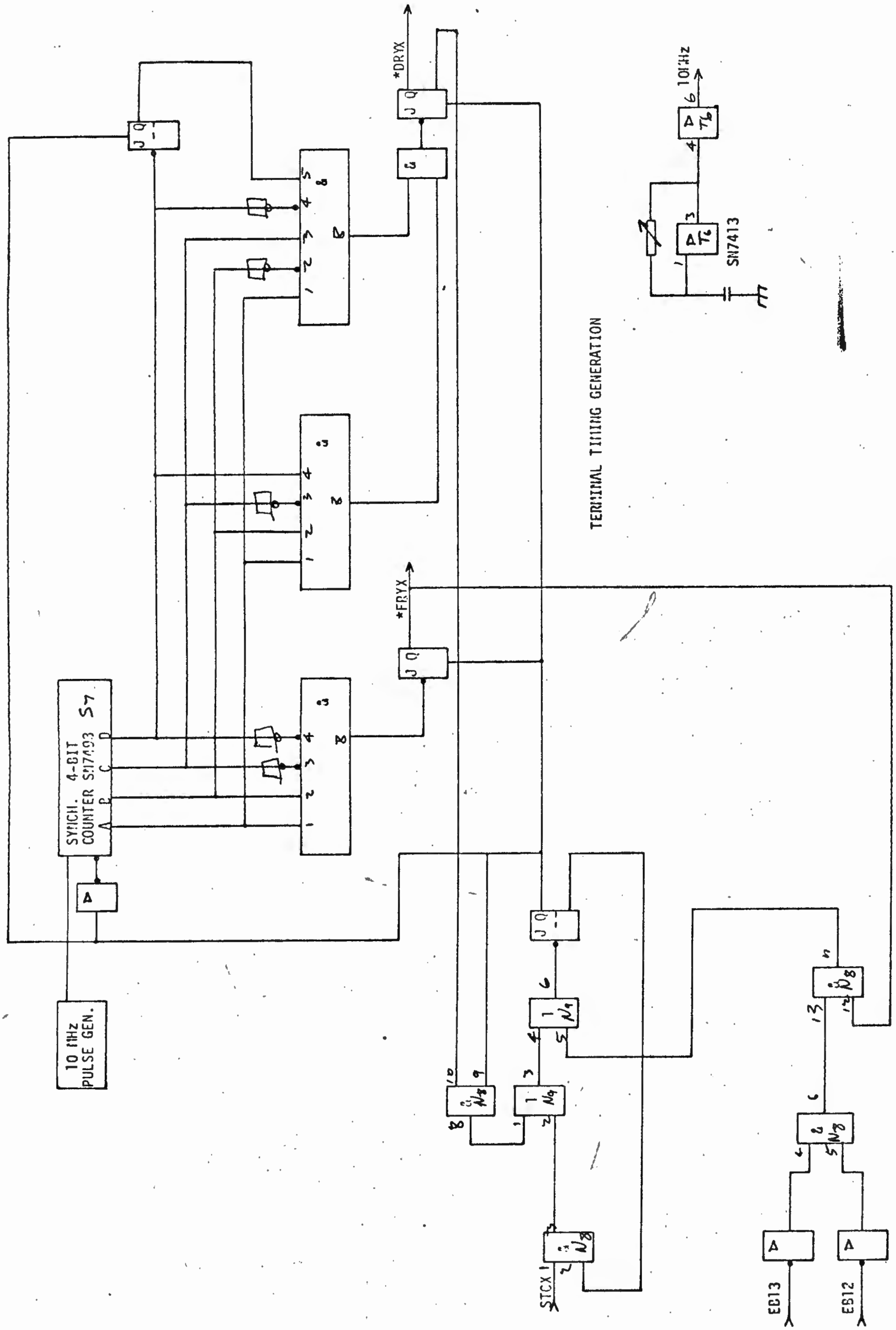
TERMINAL E-BUS RECEIVE/
TRANSMIT CIRCUITRY



TERMINAL E-BUS RECEIVE/
TRANSMIT CIRCUITRY.

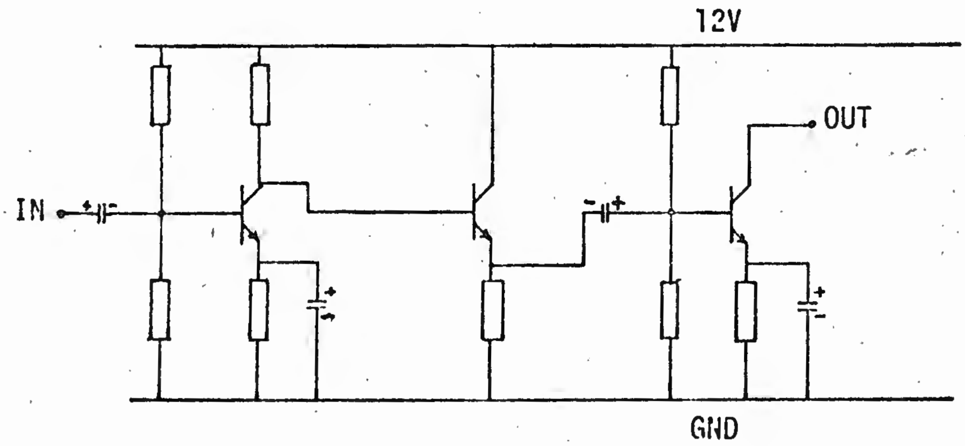


TERMINAL CONTROL LINE CIRCUITRY

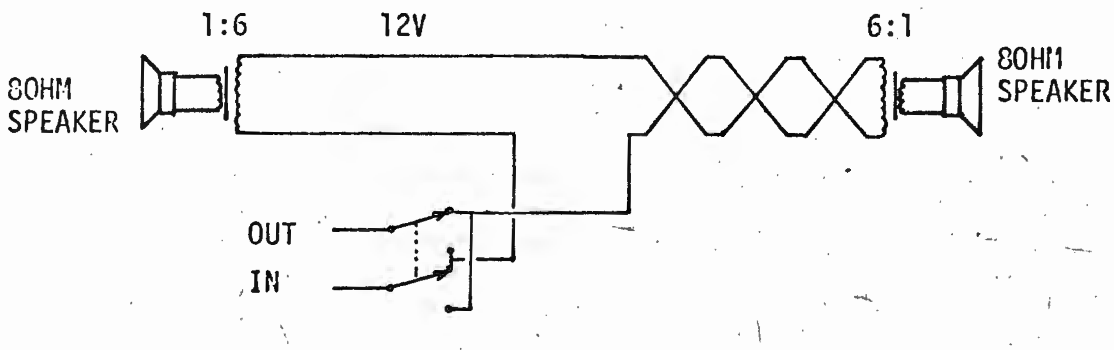


TERMINAL TIMING GENERATION

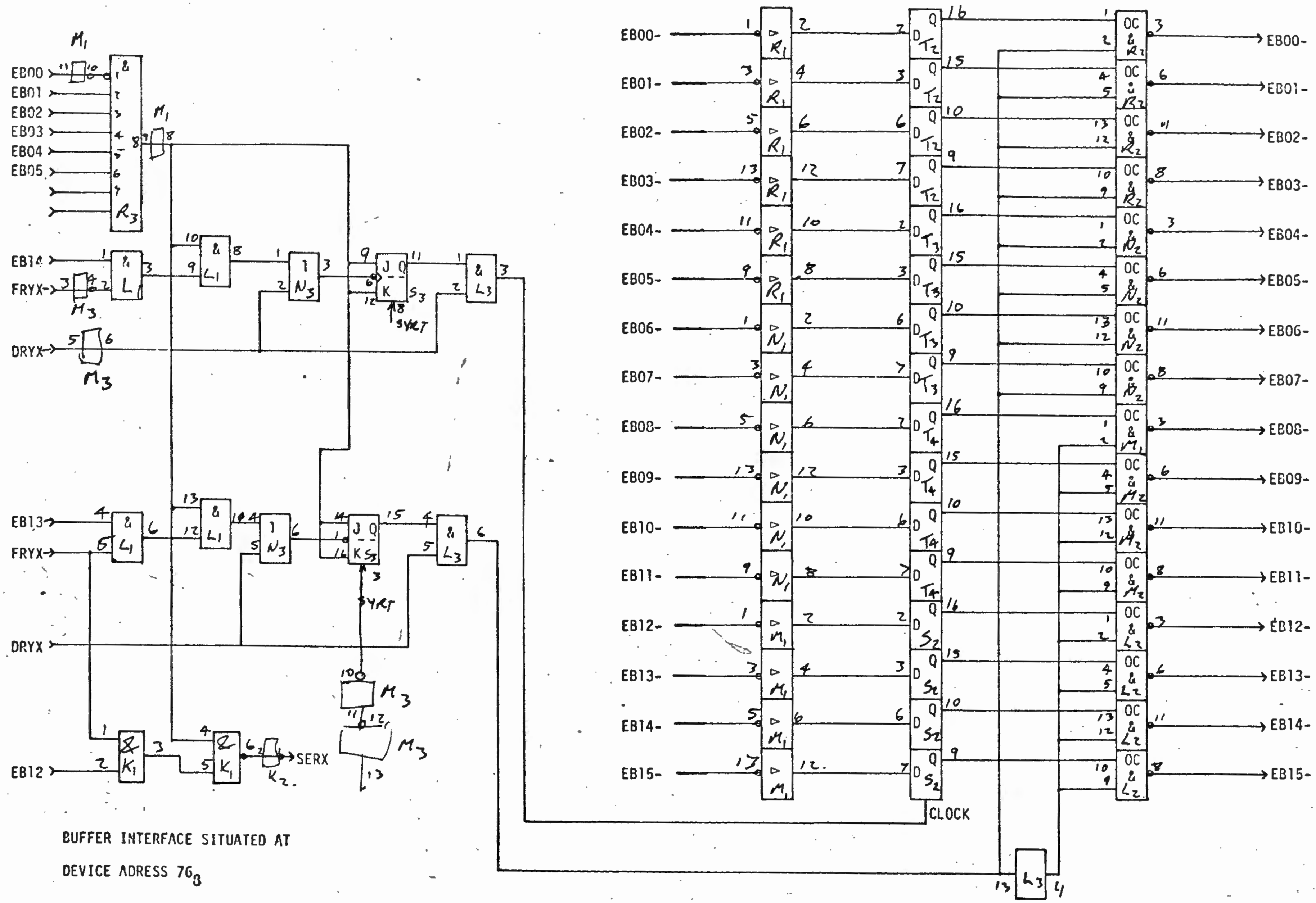
mounted on veroboard at the terminal



INTERCOM AMPLIFIER



SWITCHING DIRECTION OF INTERCOM AT TERMINAL



BUFFER INTERFACE SITUATED AT

DEVICE ADRESS 76_8

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