UNIVERSITY OF CAPE TOWN

DEPARTMENT OF ELECTRICAL ENGINEERING

EVALUATION AND MITIGATION OF THE UNDESIRED EFFECT OF DC BIAS ON INVERTER POWER TRANSFORMER

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MASTERS

IN ELECTRICAL ENGINEERING

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DECLARATION

I declare that this thesis "***Evaluation and Mitigation of the Undesired Effect of DC bias on Inverter Power Transformer***" has not been submitted before at any university. I hereby confirm that it is based on my own work. Each significant contribution to this dissertation from works of other people has been referenced.

Signature_____ Date: 5th October 2009

ISUMBINGABO Emma Francoise

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This project was undertaken with assistance from a number of people and for this reason I wish to express my gratitude to them for their contributions.

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TERMS OF REFERENCE

This project was proposed by Dr Michel Malengret, a Senior Lecturer at the University of Cape Town on the 30th January 2008. The research is aimed at the investigation of the effects that DC bias has on a single phase 6 kVA power transformer so as to design a control system that could mitigate those effects.

Dr Michel Malengret was the Supervisor of the Project. The requirements for this Thesis project were specifically set as follows:

1. Review the existing literature pertaining to (a) the effects that DC bias has on the operating characteristics of a power transformer (b) the operating principle of single phase inverter which has a power transformer connected to its output.

2. Investigate the likely occurrence of a DC bias in single phase inverter transformer and possible ways of mitigating its adverse effects.

3. Validate the above theory by (a) Laboratory experiment of DC bias in power transformer and (b) Measuring the DC bias in single phase inverter system.

4. Indirectly determine the degree of DC bias by measuring harmonics on the primary side of an inverter power transformer.
5. Develop a control algorithm to mitigate the DC bias,

6. Run simulations using MATLAB to test the usefulness of the algorithm.

7. Implement the control system algorithm in the laboratory using a digital signal processor (TMS320LF2407).

SYNOPSIS

Inverters have traditionally been used mostly in standalone systems (non-grid connected), Uninterruptible Power Supplies (UPS) and, more recently, in distributed generated systems (DGs). DG systems are based on grid connected inverters and are increasingly being connected to utility grids to convert renewable energy sources to the utility grids. Such sources are likely to have a significant impact in the future in meeting the electricity demands of industry and domestic consumption. Common DGs utilize DC power sources such as fuel cells, batteries, photovoltaic (solar) power, and wind power.

Most of power supplies in domestic and industries are AC power consumers and, for this reason, the DC power has to be converted to meet the requirement.

Two main causes of DC current in inverter power transformer are:

1) Non-linearity and asymmetry in its switching mechanism which may result in undesired DC current at its input. This DC current introduced into an inverter transformer results in the transformer's magnetic flux distortion and in some cases magnetic saturation. This, in turn, results in asymmetrical primary currents in the transformer (inverter side). This is due to the non linear characteristics of the transformer magnetic flux.

2) The same effects can be produced by the connection of asymmetrical loads (e.g. asymmetrical rectifier) to the inverter output.

The result in both cases is an asymmetrical magnetic flux in the transformer. This is manifested as even and odd current harmonics as well as an increase in the reactive power requirement from the inverter.

To remedy this situation, it is, therefore, necessary to incorporate into the inverter's control system a mechanism of cancelling the DC magnetic motive force (mmf) that causes the magnetic flux distortion.

This Thesis presents a method of introducing a DC voltage component in the inverter's voltage output so as to inject the necessary DC current into the primary side of the inverter's transformer so as to cancel the total DC mmf that the transformer is subjected to (supply and load side).

This project consists of three main parts namely: Modeling, Simulation and Laboratory Experiment. Activities undertaken under Modeling and Simulation were as follows:

- Determining the effects of DC current on a power transformer.
- Investigating the likely occurrence of saturation of the power transformer incorporated in inverter systems.
- Mitigating the effects that can be caused by the presence of a DC component in the windings of a power transformer.
- After understanding the literature on the subject of interest, MATLAB SIMULINK and MATLAB m-files were used to simulate the behavior of the power transformer under three situations :
- The transformer under linear load.
- The transformer subjected to asymmetrical loading.
- The inverter system that has a power transformer on its output

were designed in MATLAB and used to simulate the situation for each case.

To validate the theory and simulation results, experimental work was carried out as follows:

- Investigation of the effects that DC (current) injection can have on a 6 kVA power transformer.
- Investigation of the performance of a 6 kVA power transformer under linear loading.
- Investigation of the performance of a 6 kVA power transformer under non-linear loads.
- Investigation of the likely occurrence of DC offset in inverter system.
- Mitigation of the effect of DC bias on power transformer using extra windings.
- Mitigation of the effects of DC offset in power inverter transformer by using the second harmonic content of the primary current as a feedback signal.

Results obtained showed a successful implementation of the proposed method. However limitations of the controller performances were experienced and will require future work.

It was concluded that a total removal of the undesired effects of DC bias is achievable and that total removal of DC offset in power inverter transformer is possible if the limitations of the controller are overcome.

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LIST OF ABREVIATION

GP Timer : General purpose timer.

TxPR : Timer x, period register.

TxCMPR: Timer x compare register.

TxCNT: Timer x, counter.

TxCON: Timer x control register.

TxPWM : Timer x, PWM pin.

MAXCONV: Maximum conversion.

CHSELSEQ1: Channel sequencer.

ADCTRLx: ADC control register.

GPTCONx: General purpose control register.

DC: Direct Current.

AC: Alternating C

Chapter 1

INTRODUCTION

Direct Current (DC) effect on power transformers has recently received significant attention. DC current could be caused by, power electronics equipment operating under normal conditions, and under abnormal conditions, or could be due to geomagnetically induced current (GIC) in transmission systems.

Depending on the level and duration of the presence of DC current, undesirable effects such as:

- Transformer half cycle saturation
- Transformer magnetizing current distortion
- Transformer overheating
- Increase in reactive power absorption
- Corrosion of grounding equipment
- Metering errors and malfunction of protective equipment may result.

This thesis focuses on methods of mitigation of the magnetizing current distortion resulting from such DC current. These DC currents can manifest themselves in the primary supply, and the secondary load side of a single phase inverter transformer or both. The objective of this Thesis is to find an effective method so as to restore the magnetizing characteristics of the power transformer by injecting a compensating DC current. The thesis focuses on the application of DC effect mitigation in inverters in particular. This is achieved by controlling

the switching intervals so as to cause a DC voltage component which will result in a DC current flowing on the primary side which would improve the magnetic flux so as to improve symmetry between the positive and negative cycle. The goal is to neutralize the DC offset resulting from both the inverter (in the case of symmetrical load) and asymmetrical loads currents.

In order to achieve the control of the DC current offset into the inverter system, a real time digital signal processor (DSP) was used, which was sufficiently fast (40 Million Instructions Per Second) so as to detect the magnetic flux distortion and do the necessary real time calculation and control of the pulse width of the PWM signals to remedy the problem.

1.1 Justification of a Pulse Width Modulation (PWM) Control Inverter Capable of Injecting a Direct Current

Inverters have traditionally been used mostly in standalone systems (non-grid connected), uninterruptible power supplies (UPS) and more recently in distributed generated systems (DGs). DG systems are based on grid connected inverters and are increasingly being connected to utility grids to connect renewable energy sources to the utility grids. Such sources increase substantially and have a significant impact in the future in meeting the electricity demands of industry and domestic consumption. Common DGs utilize DC power sources such as fuel cells, batteries, photovoltaic (solar) power, and wind power.

Two main causes of DC current in inverter power transformer are:

1) Non linearity and asymmetry in the inverter switching mechanism may result in undesired DC current to flow. This DC current is introduced into an inverter transformer which can result in the transformer's half cycle magnetic saturation. This, in turn, results in asymmetrical currents in the transformer's primary (inverter side).

2) The same effects can be produced by the connection of asymmetrical loads (e.g. asymmetrical rectifier) to the inverter output.

The result in both cases is an asymmetrical current in the primary side of the transformer. This is manifested as even and odd current harmonics, as well as an increase in the reactive power requirement from the inverter.

To remedy this situation, it is, therefore, necessary to incorporate into the inverter control system a mechanism of cancelling the DC magnetic motive force (mmf) that causes the magnetic flux distortion. The method used in this thesis is to introduce a DC voltage component in the inverter's voltage output so as to inject the necessary DC current into the primary side of the inverter transformer so as to cancel the total DC mmf that the transformer is subjected to (supply and load side).

1.2 Objectives of the Study

1.2.1 Main Objective

The main objective of the study is to first analyze the effect of DC current on a power transformer and propose a method of mitigating its effect by injecting the necessary DC current that would counteract the undesired DC currents that may exist on the supply or load side. In order to do so, a method of determining the magnetic asymmetry is required. It will be shown in this thesis that this can be achieved by measuring the level of even harmonic of the primary current.

1.2.2 Specific objectives

- To validate the theory with respect to the effect of DC current in inverter systems.
- To find practical methods of restoring flux symmetry by the inverter injecting DC current component into the primary side of the inverter transformer.
- To investigate the extent of correlation of results obtained by simulation and laboratory work.

1.3 Structure of the Thesis

This thesis consists of six chapters with the following outline:

Chapter 1 gives the need for the research as well as the objectives.

Chapter 2 focuses on the review of the literature on the operating principles of (a) single phase power inverter (b) voltage control methods and (c) the distortion that can be detected on its output as well as the state of the art in the mitigation of such effects.

Chapter 3 gives the overall approach to the research. The chapter presents the methodology used to carry out simulations in MATLAB 7.2 of the performance of a single phase 6 kVA power transformer under (i) linear load (ii) non-linear (asymmetrical) load and (iii) voltage controlled voltage source inverter. The chapter also presents the methodology used for the investigations on the inverter power transformer.

Chapter 4 is devoted to systems design focusing mainly on the hardware and software systems. The hardware system includes the following: driver modules for the MOSFET switches used in the inverter bridge; the power supply used to power the devices that require external power source; sensors used to measure the current on the primary side of the power

transformer and the DSP Controller and its interface card. The software system design comprises the program structure; the main program flow chart; main code written in C; the interrupt service routine and the compiler.

In chapter 5, laboratory work is presented. First, the investigation of the performance of power transformer under various DC current injections is presented as well as the approach used to carry out the experiment is outlined. Results obtained are presented and discussed. Secondly, the inverter system laboratory set-up as well as the experimental work conducted is described. Results obtained are presented and discussed.

The last section of chapter 5 deals with the mitigation of the undesirable effects of DC offset on single phase 6 kVA power transformer. A method of mitigating harmonics using extra windings is also presented together with a control system that eliminates DC mmf in the inverter power transformer by introducing a DC current in a third windings . The level of magnetic distortion is assessed by observing the second harmonic of the primary current. Chapter 6 presents the conclusions and recommendations based on the results obtained in the research project.

Chapter 2

LITERATURE REVIEW

2.1 Introduction

This Chapter presents a review of research publications related to single phase inverter systems and sources of DC current in inverter systems, effects on the power inverter transformer as well as the mitigation of the resulting effects. The aim of the chapter is to investigate the sources of DC current in transformer-based inverter systems, study their effects on the power transformer and finally cover the literature about the ways of mitigating the DC offset in inverter power transformers.

The literature on inverter systems covers control systems, unipolar and bipolar switching schemes, and current and voltage inverter systems and examines the advantages and disadvantages of these control systems.

2.2 Operating Principles of a Single Phase Inverter

An inverter is essential for the interfacing of a distributed generator power source with the AC network/AC loads [1]. There are many possible inverter topologies and inverter switching schemes and each one will have its own relative advantages and disadvantages. The choice of an inverter topology is mostly based on the ability to obtain high power conversion efficiency and lower output current distortion.

Single phase inverters may be unipolar switched or bipolar switched. They can be current controlled or voltage controlled [2], even though current controlled inverter systems [3,4,5 and 6] offer many advantages over voltage controlled inverter systems with regard to minimization of current distortion. The present work focuses on voltage controlled inverter systems because of their simplicity.

2.2.1 Voltage Controlled Voltage Source Inverter Control Methods

In a pulse width modulated (PWM) inverter system the prevention of the possible occurrence of unstable phenomena can be achieved by controlling the voltage output level, its frequency and its phase angle [7]. Normally a control device is used to sense the level of the output voltage, its frequency and phase, and to store the voltage error after comparing with the desired level. This information is then used to compensate for a voltage instruction value or a PWM instruction signal, in order to correct a voltage error.

2.2.2 Current Distortion at the Inverter Output

Numerous problems prevent the inverter circuits from obtaining a low harmonic content sine wave at the output. Typical of these problems are those that arise from load and source characteristics as well as from switching transients in the inverter [8 and 9].

The presence of finite variable switching time in addition to the non linearity of the switches and the load further contribute to the imperfections present in the inverter sine wave output. Inverter related distortion can be divided into low order harmonics regions of the frequency spectrum and high order harmonics distortion which is primarily associated with the switching frequency harmonics.

With regard to high order harmonics, passive filters are designed to overcome their presence in the inverter's output signals. Connecting the inverter to an isolating transformer will also reduce some of the harmonics through the use of its leakage inductance and winding capacitance. Low order harmonics, on the other hand, are not attenuated by the filtering effect of combined transformer and filter inductance and capacitance and therefore require much more sophisticated and costly devices to remove them, when the filter is employed. It is thus common to rely on the inverter current control loop to reduce low order harmonics to an acceptable level [10]. For obtaining the proper sine wave of the inverter outputs, accurate control strategies should be used to mitigate the contributors to the low harmonic distortion. Some of the contributors to the current distortion are listed below [11and 12]:

- Non -linear effects due to dead time device voltage drop, current limit and filter choke saturation,
- Limited PWM resolution,
- Finite loop time,
- Finite loop gain,
- Measurement inaccuracies,
- Lack of stiffness in the DC link resulting in excessive current ripple,
- Non linear loads connected to inverter systems.

2.3 DC Offset Current from the Inverter Operation

The sources that are likely to contribute to the presence of DC offset current at the output of inverters include [1]:

- The impedance of the two arms of the inverter bridge not being perfectly equal.
- DC offset present in the reference current,
- DC offset introduced by feedback current sensors,
- Non- linear loads (asymmetrical loads).

In an inverter system where a transformer is connected at the output for output voltage stepping up, there is a danger that the transformer that normally operates near saturation will go into saturation.

2.3.1 Effects of DC (Current) on Power Transformers

Power inverters connected to the AC network via transformers do not inject DC offset current into the power supply system [13]. However, the presence of DC current at the output of the inverter, connected on the primary of the transformer, can lead to several adverse effects on the transformer. These effects depend on the transformer's construction and are well documented [14]. Some of the undesired effects due to the presence of DC offset include:

- Saturation of the power transformer core leading to generation of harmonics,
- Increase in magnetizing current (inductive current) and increase in reactive power absorption,
- Overheating of the transformer due to the current harmonics and skin effects,
- Increase in acoustic noise emission,
- Acceleration of corrosive effects,
- Increase in transformer losses.

2.3.1.1 Effect of Half Cycle Saturation on the Performance of a Power Transformer

A DC component resulting from an imbalance between the volt-second of alternate half cycles in the operation of the output power transformer of an inverter can result in an eventual "firing" of the magnetic core of the power transformer on one end of its asymmetrical hysteresis loop. The intensity of the exciting current under saturated core conditions can exceed the highest instantaneous load current on the inverter several times over. One of the major causes of DC component arises because of inadvertent switching-time error [15] in an inverter system. When this DC current flows in the transformer windings, it shifts the AC operating point on the BH curve [16] and this may cause severe transformer half cycle saturation [17]. A transformer with half cycle saturation becomes a rich source of even and odd harmonics and draws significant inductive MVAR from the power source, and generates more heat which results in more losses, decreasing the system's efficiency [18,19 and 20].

According to Jayasinghe, the consequence of transformer half cycle saturation can be classified as follows [21]:

(i) Generation of both even and odd harmonics in the transformers,

(ii) An increase in reactive power drawn by transformers,

(iii) A possible drastic leakage flux effect in the transformer with resulting excessive localized heating which could result in increase in losses, and degradation of the transformer insulation.

2.4 Inverter Systems and Non Linear Loads

In inverter systems design, the goal is to maintain the desired output voltage waveform over all loading conditions and transients. This ensures continuous power flow to critical loads in event of disturbance surges and AC line failure [9,10,11and 12]. This establishes conditions for the inverter system to rely on its control system to produce the shape of the waveform and regulated output voltage magnitude.

Several researchers [9,10,11 and 12] have proposed advanced control systems based on closed loop controllers which overcome the distortion in the inverter output voltage, thus leading to a faster response and improved total harmonic distortion (THD) content, regardless of the loads connected at the output of the inverter.

Michael, William and Robert [9] explored two feedback topologies based on:

- Filter inductor current and load current sensing.
- Filter capacitor current sensing.

In a case where an inductor current feedback is used, two methods of load current decoupling were considered and the capacitor current method was also considered in lieu of current sensing.

Mihalache [10] also proposed a simple, reliable and easily implemented fully digital control strategy that provides an excellent disturbance and feed forward decoupling method that takes into account the effect of discretization by employing voltage and current controllers that adapt their structure to different types of loads.

Ying-Yu and Shih-Liang [11] have also presented a multi-loop controller which consists of a current controller, a voltage controller and a feed forward controller to achieve a minimal possible total harmonic distortion in the output voltage to meet the stringent requirements of modern high performance AC conditioning systems.

The reviewed control system strategies were in agreement with regard to the advantages of using fully digital controllers to achieve fast current control of the PWM inverters with low total harmonic distortion. However, they omitted to investigate the case where the disturbance is caused by a non-linear load consisting of a half-bridge rectifier. An aspect of this thesis will, therefore, be to investigate the inverter's current waveform distortion caused by the connection of non-linear loads which are half-wave rectifier in nature.

2.4.1 DC Offset Current from Asymmetrical Loads (Half-wave rectifier)

Non-linear loads, connected on a secondary side of a power transformer, introduce higher levels of harmonics, as documented by many researchers [9,10,11,12 and 22]. These non-linear loads are defined as the loads that draw current which is not sinusoidal and they include such equipment as arc furnaces, gas discharge lighting, solid state motor drives, battery chargers, UPS systems, and increasingly common electronic power supplies.

Non-linear loads generate harmonics currents which flow from the load toward the power source, following paths of least impedances. This thesis looks at the behavior of non linear loads which are half-wave rectifier based. When an inverter load consists of a half wave rectifier, a DC current is generated on the secondary of the system step-up transformer. This DC current is superimposed on the AC current which represents the rectifier ripple. The DC

current is injected into the transformer from its secondary and the transformer draws even harmonics from the side of the transformer supplied by the voltage source [23].

It takes only a small amount of DC current injection to cause the transformer to exceed the institute of electrical and electronic engineering (IEEE) Standard which imposes limits on the magnitude of harmonic currents and DC currents that may be injected into the utility by distributed generators or from a utility customer's premises. Recently, IEEE enacted IEEE STANDARDS 929-2000 [24] and its limits of allowed even harmonic and DC injection in a system by distributed generators are much stricter than the previous limits. These standards state that the amount of DC current injected into a system by distributed generators should not exceed 0.5 percent of the distributed generators' output current ratings. Further, the new standards for injected even harmonics require that the second harmonic current be maintained at less than 1 percent of the output current rating of a distributed generator or AC power source [23].

It is clear that these standards require a distributed generator to function as a substantially sinusoidal AC current source with a low harmonic content.

In a transformer isolated distributed generator, DC injected into the transformer from the power inverter side is blocked by the transformer from passing through the utility side of the transformer. This demonstrates that the transformer can be used to protect the utility and its equipment from DC injection. However, the transformer by itself does not solve the problem of large even harmonic amplitudes which will/could result [23].

Additionally, another more subtle problem with the use of transformers to isolate distributed generators and connected power converters is that a power converter, such as an inverter, can appear to be a source of even harmonics when DC current is injected into the transformer

from the utility side (load side), even if the power converter itself is not a source of DC offset.

It is thus very important to design a control system that monitors and controls current flow between an alternating current power source which is mostly interfaced to an inverter when DG are used and the AC load side which can be a source of distortion for the overall system. This control system should control the amount and magnitude of DC current and even harmonics currents injected by the load into the system step up transformer.

2.5 DC Offset Current Elimination

Results of research carried out to investigate the effects of DC current on power transformer's performance [23,27,28,29,30,31 and 32] show that the presence of DC currents on either side of a power transformer are sources of current and voltage harmonics, especially, even harmonics. In any AC network, the presence of harmonics is not desired, because these may be a source of problems for the consumers of the utility grids. Therefore, even if transformers are used to isolate the inverter systems from the grid, it should be an advantage to minimize these harmonics.

2.5.1 Existing Direct Current Injection and Even Harmonics Control Systems

Research has been carried out by distributed power generation industries to find a solution to the problem of DC injection and even harmonics in their systems but only limited success has been achieved [23 and 24]. Many of the solutions found could only solve the problem of DC injection, but even harmonics were shown to be more difficult to control.

Some of the approaches to the problem are given below:

1. Manufacturers in the industry have been using the method of including a voltage transformer in the output circuit of their power generator downstream of the power inverter [23].As stated before; this approach has only been successful in addressing the DC current problem. The transformer could only block the DC current from flowing through and reaching the other side. Unfortunately, the Transformer continued to draw even harmonics on the other side, its supplied side, making the approach ineffective with regard to adherence to IEEE standards.

2. Another approach used in these industries has been to embed a magnetic field sensor into the transformer to measure DC flux and adjust the power inverter by equating the DC flux to zero [26 and 27]. The system has two disadvantages. The first disadvantage is the high cost of the component used and the second drawback is the temperature drift of the sensor which develops with time.

3. A resistor shunt was then used to measure the amount and level of DC injection so that the power inverter could be adjusted accordingly to output the desired current output [28]. This also has had limited success since the DC current has to be reduced to less than 0.5 percent of the AC current output from the generator to meet the new IEEE standards and it is difficult to filter the relatively small DC current from the relatively large AC current signal.

4. Another approach has been to place large capacitors in series between the power inverter connected to the generator and the transformer. The capacitors are effective in blocking DC current from getting into the transformer and preventing the transformer from drawing even harmonics. The limitation of this approach is the high cost of the capacitors [29].

5. The manufacturers have also adopted the use of expensive components and new microprocessors, but still this prevented the DC injection but the problem of even harmonics remained and the distributed generator designers could not keep these harmonics to the desired limits [30,31,32 and 33].

   A control system which prevents transformer's saturation, controls DC current injection, and minimizes even harmonic current is, therefore, needed.

2.6 Control Systems [34]

Control systems are necessary components of modern industrial processes and our daily lives. Control mechanisms have evolved from mechanical, pneumatic and electromechanical systems to electronic control systems.

Electronic control systems have been implemented with analog components like resistors, capacitors and op-amps (operational amplifiers). However, the development of microprocessors has created new opportunities for control systems. This is due to the powerful processing capabilities of microprocessors, but also the need for a new body of knowledge that utilizes some of these processing capabilities.

2.6.1 Analog Control Systems [34]

Control systems have traditionally been implemented using analog components which implement filter-like structures that modify the frequency response of the system. Even if more powerful analog processing elements like multipliers are available, they are generally not used because of their high cost. In spite of their simpler processing elements, analog controllers can be used to implement high performance systems.

2.6.2 Digital Control Systems [34]

Since the appearance of microprocessors and microcontrollers digital controllers are taking over many applications from analog controllers. In a digital control system, the controller is implemented with a microprocessor or a microcontroller, which handles the signal processing. The input signal, being most of the time analog in nature, a conversion is needed at the input of the digital system and, for the real world interpretation of the result; another converter is needed at the output of the system. Figure 2.1 below illustrates the working principles of a digital control system.

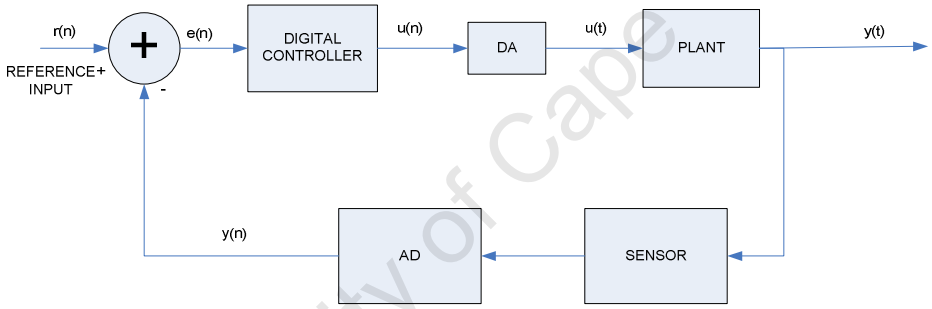


Figure 2.1: A Digital control system

2.6.3 Analog versus Digital Control Systems [34]

Selecting a controller to be used in a system should be done very carefully, considering the advantages and limitations of each type. For example, analog controllers will offer the advantage of continuous processing of the signal and can be used for very high bandwidth. They also provide infinite resolution of the signal that they are measuring, thus providing precise control. They are very easy to design due to their long-standing availability. The

design of a system using analog controllers can be cost-effective since they can be implemented using cheaper components.

On the other hand, analog controllers are built using components which are vulnerable to temperature and ageing factors, which affect the reliability and stability of the system in which they are used. Analog controllers are limited to the design of simple algorithms because of the delay in signal processing and they are, therefore, mostly used to develop PID control and compensation techniques.

Digital controllers function by sampling the received signal at discrete time intervals, which limits the bandwidth that can be handled by these controllers. The processing of the signal takes a finite amount of time, adding to phase delay in the system. In addition, the resolution of the signal is limited by the resolution or wordlength of the processor. Digital controllers also require additional components like analog to digital converters and digital to analog converters and newer processors may have these components on the same chip. Digital controllers have only recently been developed, which makes them difficult to design since their behavior is not yet understood by many designers.

On the other hand, the advantages presented by digital controllers include their stable performance: they are not affected by component ageing or temperature drift. When the design is made in the Z-domain the behavior of digital controllers can be precisely controlled. They can be used to implement sophisticated techniques like state control, optimal control and adaptive control. Digital controllers are programmable which makes them easy to upgrade. When digital controllers are properly designed their advantages outweigh their disadvantages.

2.6.4 Choice of Digital Controller Processor

It can be very difficult to decide on the type of processor to use, since the performance and behavior of the digital controller can be critical. Four of the possible choices are listed below:

- Microcontrollers,
- General purpose microprocessors,
- Digital signal processors (DSP),
- Bit-slice processors (which are not often used because of their high cost).

Digital controllers monitor signals at discrete time intervals or finite sampling rates. If the signal is not sampled fast enough, some of the information may be lost. The processing of the signal takes a finite amount of time. The processing has to be completed before the arrival of the next sample. Too much delay in the output can cause loss of information or excessive phase delay in the system, leading to system instability. These are some conditions which lead to minimum performance requirements on the processor. Digital controllers use discrete steps to represent a signal, which is limited to the wordlength of the processor. Coefficients or gain constants have also to be represented in the limited wordlength and this discretization or loss of resolution is known as quantization error. In addition, results of mathematical operations have to fit into a limited wordlength which can result in the loss of part of the operation result. This is referred to as truncation error. Both of these errors cause oscillations or limit the cycles and can lead to instability [33]. Another problem that occurs in digital controllers is the overflow of the registers. Successive mathematical operations in a digital controller can cause the registers to overflow. Registers in most processors wrap around,

causing the result of the calculation to go from the most positive to the least negative, in turn causing the output to reverse directions. Most of these problems occur in microprocessors and microcontrollers because their architectures are not designed to do signal processing. However, most of the problems discussed above can be eliminated with the use of digital signal processors as controllers.

2.7 Digital Signal Processors (DSP) as Controllers [34]

Digital signal processors architecture has been designed for signal processing systems. They don't only solve numerical problems in the signal processing, but are also able to meet the bandwidth requirements of high performance systems using sophisticated techniques. In digital signal processing most algorithms, including control algorithm can be represented as difference equations consisting of multiple accumulates.

2.7.1 DSP-based Inverter Systems

The reliability of an inverter system depends on its control system. Traditional analog control strategies for PWM inverters contain many crucial components, whose temperature drift and ageing parts will negatively affect the systems long time stability.

DSP offers flexibility in designing control loops through its programmability. Advanced algorithms are possible using DSPs, and the systems in which DSPs are used are reliable [33]. The use of DSPs to implement the digital control of inverter systems allows low total harmonic distortion, a sinusoidal output voltage and power factor correction of a system under large non-linear loads. The DSP based control of a single phase inverter system

consists of a single chip DSP Controller and dedicated interface hardware and software designed for the interface and control of the inverter system [10].

The advantages presented by the use of DSP Controllers for inverter systems include the use of advanced technologies through replacing analog control with DSP based digital control, this is done by replacing hardware with flexible software. The use of a DSP in an inverter control system also leads to cost reduction due to software replacement of hardware components, standardization of design procedures across an entire product line, reutilization of software intellectual properties, and increased performance [34, 35 and 36].

With DSPs, closed loop control systems can be easily implemented to minimize the total harmonic in the inverter output voltage, and eliminate the undesired harmonics in the output current. The DSP controls the inverter switches so that the output voltage can track the sinusoidal reference at each sampling instant. In most DSP feedback control systems, the inductor current and the output voltage are sensed as feedback variables, and the control algorithm computes the required pulse width for the inverter [9].

2.7.1.1 Overview of the Theory pertaining to DC current in Digitally Controlled Inverter Systems [33]

In digitally controlled inverter systems truncation error caused by numerical arithmetic can arouse continuous collection of flux imbalance and lead to inverter transformer saturation. In most inverter control schemes, a feedback voltage is compared to a reference to form a voltage error. The obtained error passes through a voltage regulator output which is compared with a carrier triangular signal to generate the required PWM signal to control the switches. The process guarantees that the shape, amplitude and phase of the output voltage is close to the given reference voltage. If the output signal of the voltage regulator has a DC component

and power switches are ideal it is certain that there will be flux imbalance in the output transformer.

2.7.1.1.1 Infection of truncation error [33]

Using a fixed-point digital signal processor like the TMS320LF2407 DSP to deal with floating numbers calculated during controller design may require number notation, which means using fixed point numbers of decimal points. In the PI controller mostly used in inverter systems and meant to be used in this project, the mathematical model shown in equation 2.1 below is to be implemented

$$u(n) = K_p\left[e(n) + \frac{T}{T_i}\sum_{j=0}^{n} e(j)\right] \tag{2.1}$$

where K_p is the proportional gain and $K_i = K_p\frac{T}{T_i}$ is the proportional gain, T is the sample time. T_i is the integrating time of the controller. $u(n)$ Is the output of the regulator and $e(n)$ is the nth error between the feedback and the reference signal.

General PI has two expressing patterns: one is full-quantity mode and the other is incremental mode. The mode shown in equation 2.1 is dispersed full quantity PI arithmetic. Shown below in equation 2.2 is the dispersed increment PI arithmetic

$$u(n) = u(n-1) + K_p[e(n) - e(n-1)] + K_i e(n) \tag{2.2}$$

Increment PI arithmetic is so simply and conveniently realized by software that it is applied widely in digitally controlled DC systems. However, in AC systems, the collection of truncation error may lead to saturation of the system because the arithmetic depends on

historical track. In implementing PI arithmetic as shown in (2.2) proportional gain K_p and integral gain K_i are all floating point numbers. Since (2.2) can be expressed as (2.3) below:

$$u(n) = u(n-1) + \Delta u(n) \tag{2.3}$$

where

$$\Delta u(n) = K_p * [e(n) - e(n-1)] + K_i e(n) \tag{2.4}$$

It is clear that K_p and K_i are Q-notated floating-point numbers in the digital process, and the middle variable $\Delta u(n)$ is also a Q-notated floating-point number. However, the ultimate results of PI arithmetic should be fixed-point numbers, so a process during which floating-point numbers are changed into fixed-point numbers is needed. That is, the decimal fractional is removed and only the integer is left. However, truncation error will result from this process. If the error comes from $\Delta u(n)$ it will be coupled into $u(n)$. Substituting truncation error with $\Delta u(n)$ produces

$$\Delta u(n) = \Delta u(n)\_d + \Delta u(n)\_f \tag{2.5}$$

where $\Delta u(n)\_d$ and $\Delta u(n)\_f$ are the integer part and decimal fraction of $\Delta u(n)$ respectively. $\Delta u(n)\_f$ is the truncation error of $\Delta u(n)$. So increment PI arithmetic can be expressed as shown below:

$$\begin{aligned} u(n) &= u(n-1) + \Delta u(n)\_d \\ u(n) &= u(n-1) + \Delta u(n - \Delta u(n)\_f) \end{aligned} \tag{2.6}$$

According to these (2.7) is deduced.

$$u(n) = u(0) + \sum_{j=0}^{n} \Delta u(j) - \sum_{j=0}^{n} \Delta u(j)\_f \quad (2.7)$$

where $\sum_{j=0}^{n} \Delta u(j)\_f$ is the total truncation error.

If the above process is adopted, truncation error will accumulate ceaselessly. The DC component of the PWM modulating signal and that of the output voltage and primary current of the power transformer will increase till the transformer saturates.

2.7.1.1.2 Solution of the truncation error [33]

To avoid the accumulation of truncation error, the computing procedure of PI arithmetic must be amended. Taking into account the origin of the error, $\Delta u(n)$ is expected to be precise. The whole variable in the deducing process will be precise if there is no truncation error $\Delta u(n)$.
It is only when the PI regulator has the current result (there is output voltage at every integral time in this project) that the changing process during which floating-point numbers are changed into fixed-point numbers happens. In fixed-point DSP truncation error cannot be avoided and a proper control method must be established to limit its effects. If the DC component can be checked out promptly and be reduced or eliminated through a proper control method, flux imbalance in the transformer can be avoided.

2.7.1.1.2 Infection of the sampling circuit [33]

During the digital control process, the error caused by the sampling circuit and modulating circuit together with the error in the reference of ADC may result in a total error E of a whole sine period unequal to zero. Figure 2.2 depicts the process of sampling the inverter output

signal using the attenuator circuit which steps down the amount of output voltage V_0 and modulates it before sending it to the DSP's ADC.

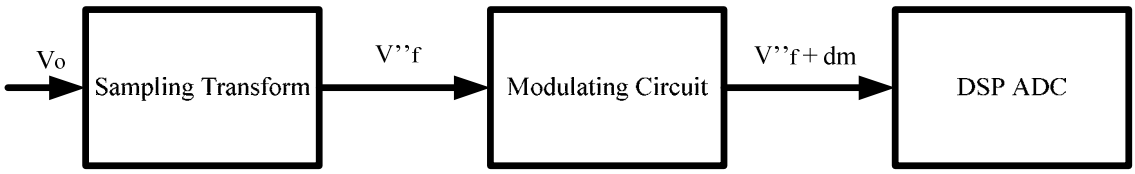


Figure 2.2: Sampling diagram of output voltage

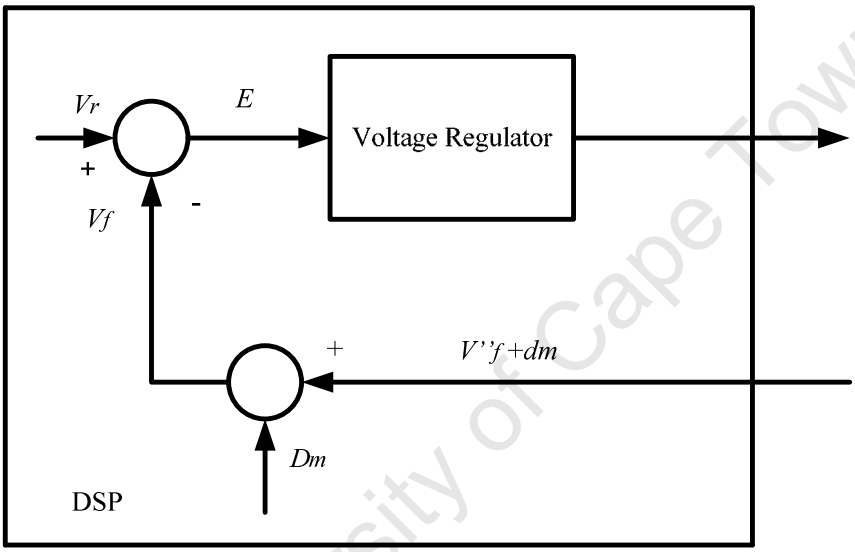


Figure 2.3: The diagram of voltage regulation

Figure 2.3 above [33] depicts the control frame of digital voltage regulation, where $V''_f + dm$ is the feedback voltage which is delivered to the ADC channel after modulating the circuit. dm is the factual DC component superimposed on the feedback voltage V''_f, and Dm is the ideal DC component which should be superimposed on the feedback voltage. From figure 2.3 the following equations can be seen.

$$V_f = (V'''_f + dm) - Dm = V''_f + (dm - Dm) \tag{2.8}$$

If the factual DC component dm is unequal to the ideal DC component Dm, a bias will be superposed on feedback voltage V''_f and there will be DC component existing in V_f, resulting in the asymmetry of driving signals, producing flux imbalance in the inverter output power transformer.

2.7.1.1.3 Solution to the infection of the sampling circuit [33]

This problem can be solved by providing a variable Dm that could be used to regulate the reference to ensure symmetry in the inverter output voltage. To guarantee the total error E of the whole sine period equal to zero, the following equation is needed.

$$dm - Dm = 0 \tag{2.9}$$

If the DSP can obtain the current reference dm of the modulating circuit instantaneously and deal with the sampling result of the ADC with the obtained reference dm, instead of using the ideal reference Dm, nothing can influence feedback voltage V_f even though the current reference dm exists.

Capturing reference by software instantaneously can therefore be selected to avoid the infection of reference drifting to the flux balance of the power transformer. This thesis used taking the on-line calculated average value of the feedback voltage as the ideal reference Dm of the modulating circuit, but some DC component still existed. This was investigated by measuring the second harmonic of the primary current of the inverter output power transformer.

2.8 PI Controller

Proportional integral controller (PI Controller) is a generic control loop feedback mechanism controller used for electromechanical motion control [37and 38]. In a system where a PI is used for control purposes, the proportional controller will have the effect of reducing the rise time and will reduce but never eliminate the steady state error, but may make the transient response worse [33 and 39]. The combination of both controllers may result in an optimal controller for some systems [37].

2.9 Summary

Although there is limited literature on the subject, the Author has provided what literature is available on the key aspects of designing and implementing the digital voltage regulation with a flux balance control for single phase inverter systems. In chapter 4, a detailed simulation study is presented where a transformer is used in an AC voltage system to step up/down the AC voltage, to supply a non linear load. The study has been carried out prior to designing the control system in order to understand perfectly the effects that DC current can have on the performance of a power transformer, how to mitigate those effects and the level of mitigation which can be reached.

Chapter 3

METHODOLOGY

3.1 Introduction

This chapter of the thesis presents the methodology used to carry out the research on the effects that DC current can have on power transformer incorporated into power inverter system. The Author spent about a year researching by conducting experiements for a better understanding of the principles of power transformer and inverter systems. The success of the project relied mainly on the better understanding of the behaviour of the power transformer under any kind of loading. The methodology adopted comprised both the simulation of a 6 kVA power transformer model using MATLAB/SIMULINK and laboratory experiments undertaken to achieve both the main and specific objectives. First, the methodology used to conduct simulation on a 6 kVA power transformer is outlined in the following sections. Simulation provided a better understanding of the theory pertaining to the principles underlying the performance of a power transformer. This will be followed by the methodology adopted in performing a number of experiments in the laboratory aimed not only at the validation of the theory with effect the effects of DC injection on a 6 kVA power transformer under various loads but also finding measures necessary for the mitigation of its undesired effects.

3.2 Simulation in Matlab

3.2.1 Introduction

In this section of the chapter, simulations done with MATLAB/SIMULINK to investigate the effects of DC current on power transformer are detailed. The investigation was done in two phases: one phase where the DC current is injected from the secondary side of the power transformer, and another phase where the DC current results from the inverter switching process. For comparison purpose, a linear load that consists of a pure resistor was first used to assess the performance of a power transformer. Then non-linear loads were connected to the secondary windings of the power transformer. The non-linear loads were represented by single diode rectifier. The next section presents simulation of a system where a linear load, consisting of a pure resistor, is connected on the secondary winding of a power transfomrer. Voltage and current waveforms are analysed to investigate the occurence of distortion in the transformer's primary current due to linear load.

3.2.2 Power Transfomer

3.2.2.1 Simulation of the performance of a 6 kVA power transformer under linear load

3.2.2.1.1 Introduction

In fundamentals of AC [40] a linear load is defined as the one in which both current and voltage have the same waveform and reach their peak simultaneously; also referred to as in phase. Linear loads are necessary to achieve maximum efficiency. The aim of this simulation work is to investigate the behavior of a 6 kVA power transformer under linear load. The expected outcome should be the linearity between the voltage and current in both windings.

Since it is stated above that a linear load helps to achieve maximum efficiency, the waveforms should be free from any harmonics, and consisting of the fundamental which is used to transmit the power to the receiving end.

3.2.2.1.2 Simulation setup in MATLAB/SIMULINK

Figure 3.1 depicts the circuit diagram used to investigate the effects of a linear load on a 6 kVA power transformer used in inverter design. The linear load is represented by a pure resistor connected to the secondary windings of a power transformer. This resistor is variable in order to achieve variation of the load current and observe the effects that variation could have on the power transformer's magnetising characteristics. The connection of a pure resistance to the secondary side of the power transformer results in the AC current circulating in the transformer windings, both primary side and secondary side. Since the power transformer was not perfectly modelled , the results obtained show an approximate view of what should be expected. Future work will detail the imperfections in the power transformer and proper simulation packages will be used in order to achieve the real representation of the power transformer and investigate its magnetising characteristics under different loading situations.

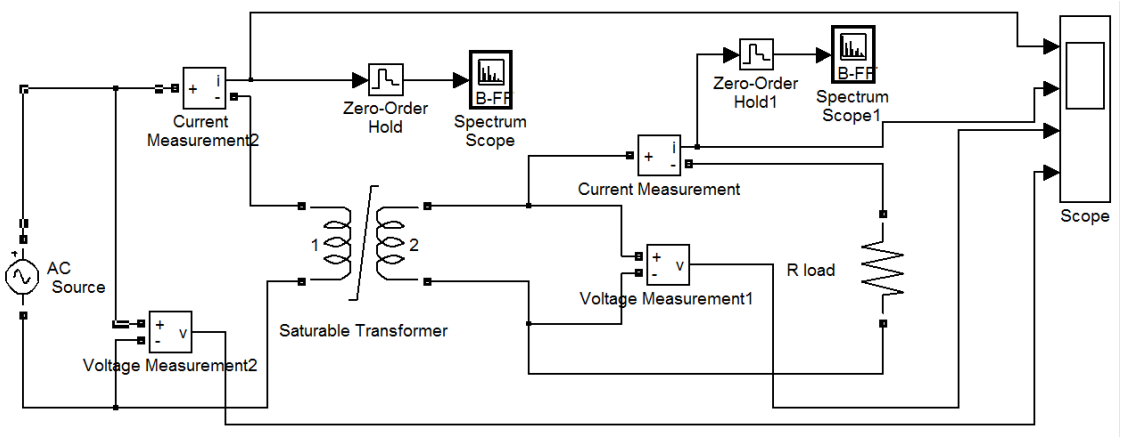


Figure 3.1: Simulink model of a 6 kVA power transformer with a linear load

3.2.2.2 Simulation of the Performance of a Power Transformer under Non-linear Loads [41, 42 and 43]

3.2.2.2.1 Introduction

Some loads, such as household appliances, cause a DC current to flow when connected to the secondary windings of a power transformer. Most of the time, this DC offset is transient. It appears for a short time when the appliance is being used then disappears. This DC offset can push the transformer that normally operates near saturation into half cycle saturation . When a toroidal transformer is used, as is the case in this research, a noise will be heard from the power transformer's windings which shows the abnormal operation of the power transformer. The same DC offset could result from inverter systems whose power switches don't have the same characteristics which leads to the abnormal operation of the inverter whose output would have a DC component, hence causing DC mmf. If the system has a power transformer at its ouput for isolating purpose or stepping up the voltage, this power transformer could experience a half-cycle saturation which could result in various power quality problems. In

this section simulation work is presented to discuss the effects of these non-linear loads on the performance of a 6 kVA inverter toroid power transformer available .

The aim of the thesis is investigation of the performance of a power transformer under various levels of DC bias and the mitigation of the resulting effects. The work focuses on the behaviour of the power transformer's magnetising characteristics under DC offset. This includes the variation of the magnetising current under DC bias, the variation of magnetising branch elements values due to DC bias, and the variation of the power tranformer's reactive power which determines the variation of the displacement power factor of the power transformer. Since the full modelling of the power transformer was not included in this research, only experimental results of the investigation of the magnetising characteristics of a power transformer are presented, leaving the power transformer modelling and simulation to be dealt with in future research work.

In the next section, the theory of the behaviour of the non-linear load which is a half-wave rectifier in nature is presented. In the section, the results presented show the scenario when a DC current circulates superimposed on the AC load current.

3.2.2.2.2 Half Bridge Rectifier Load

a. Introduction

Any appliance which has a one way for half power can introduce a DC component in the transformer to which it is connected. This type of load is equivalent to a diode connected in series with the load circuit so as to reduce the voltage and hence the power by half. However, by half-wave rectifying the transformer secondary voltage in this manner, there is inevitable

interaction with the power transformer impedance. More explanations on the behaviour of a single phase rectification process, the resulting current and voltage waveform and the numerical calculations used in half wave rectifiers are provided in [appendix A] .

For the simulation purpose, a non-linear load drawing asymmetrical currents was connected to the secondary windings of the power transformer. This consisted of a diode connected at the output of the transformer in series with the transformer rated load. The purpose of the connected diode was to inject some DC current. The diode current was varied using a pure variable resistor. The resultant waveform is a sinewave with a certain level of distortion depending on the amount of current supplied by the diode through the variable resistor. Figure 3.2 shows the arrangement of electrical elements used in this simulation and the area in the circuit where measurements were to be focused.

b. Simulation setup in MATLAB/SIMULINK

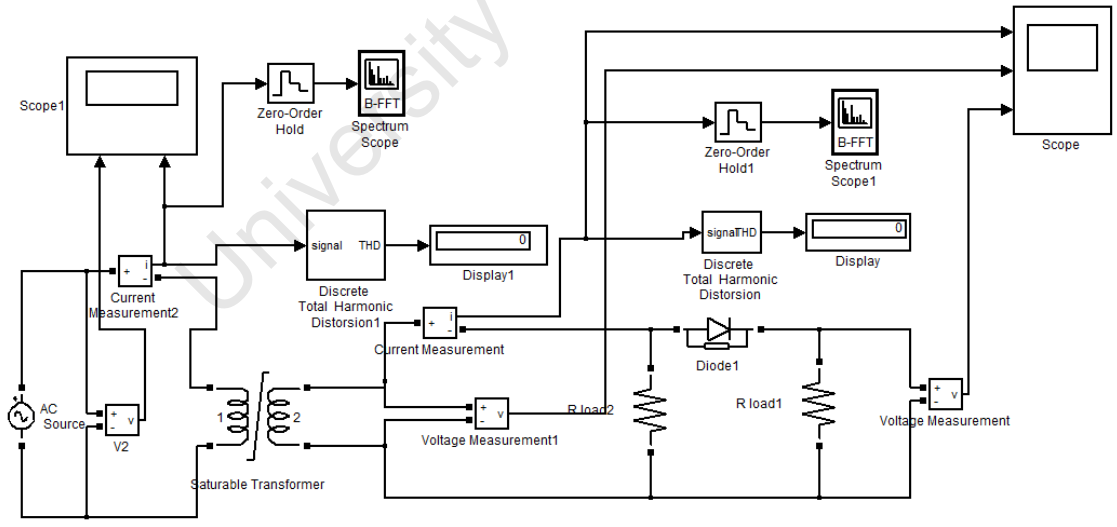


Figure 3.2: Simulink model of a 6 kVA power transformer with asymmetrical load (half-wave rectifier)

As depicted in figure 3.2 above, the investigation made to evaluate the performance of the 6 kVA power transformer operating under non-linear loads which are half-bridge rectifier is

nature was first done using MATLAB/SIMULINK simulator. All the components used to build the model were available in the SIMULINK library. An AC source was connected to the transformer primary current and a non-linear load which is a diode was connected as a load to the secondary windings. A variable resistor was connected in parallel with the non-linear load to allow variation of the connected non-linear load. Measurement were done on both the primary and secondary sides current and voltage by the use of voltmeter and ammeter. Total harmonic distortion of both voltage and current waveforms were investigated. Expected outcomes are :

- Distortion in the primary current due to asymmetrical currents drawn by the load
- Less distortion in the transformer primary voltage when compared to that of the current.

Component specification

- AC voltage source (25.9V)
- 6 kVA saturable model of transformer with 25.9/230V
- A single diode with an internal resistor of 0.01
- 2 variable resistors

Measuring devices

- Simulink scope
- Simulink voltmeters
- Simulink ammeter

- Harmonic spectrum
- THD blockset

3.2.2.2.3 Full Bridge Rectifier Loads

a. Introduction

A full bridge rectifier provides full wave rectification from a two wire AC power source input. The bridge rectifier makes use of four diodes in a bridge arrangement to achieve full wave rectification. This diode rectifier, when connected as a load on the secondary windings of a power transformer, produces a non-linear current which circulates in the secondary windings producing harmonics which then are transmitted to the primary side. This section of the thesis is aimed at investigating the rise of harmonics in a 6 kVA power transformer when a full bridge rectifier load is connected on its secondary windings. The first step in this investigation involved connecting a full bridge rectifier load to the transformer secondary windings The measured transformer voltage and current waveforms were then compared to the waveforms obtained when a linear load was investigated. The harmonics generated by the rectifier were then assessed and compared to those obtained when a linear load is connected to the secondary windings.

b. Simulation setup in MATLAB/SIMULINK

Figure 3.3 below depicts the schematic diagram used for this investigation. The diagram was designed using MATLAB/SIMULINK package, all the components used in the designed were available in the SIMULINK library.

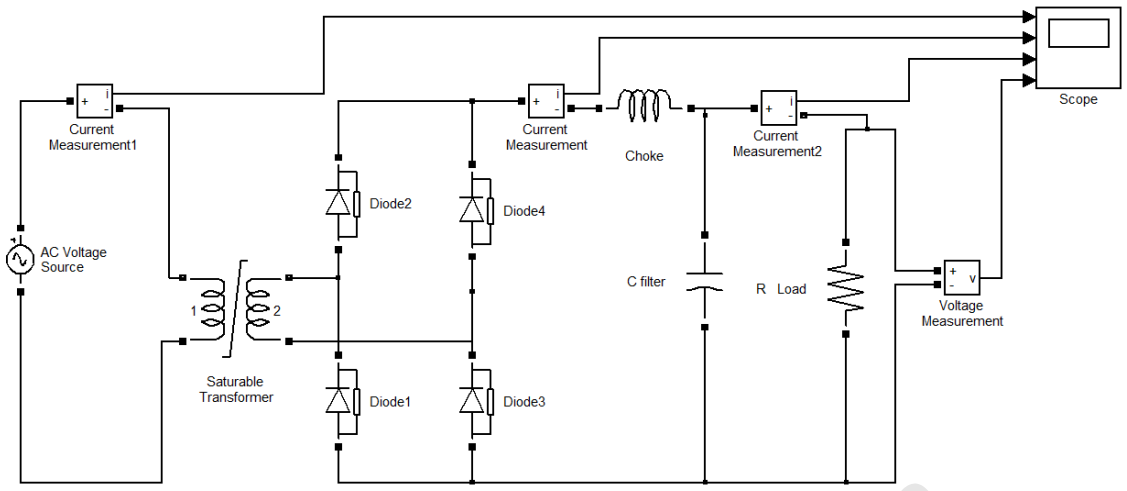


Figure 3.3 : Simulink model of a power transformer with a full-wave rectifier load

Figure 3.3 bove depicts the simulink model of a non-linear load connected to the secondary windings of a power transformer. An AC source of 25.9V was used to power the transformer this make the transformerv primary be 25.9V, the secondary was 230 V. A non-linear load represented by a full brigde rectifier was then connected to secondary of the power transformer. This load constisted of four identical diodes connected to form a bridge. An inductor-capacitor LC filter was connected to the output of the bridge to smooth the ripples superimposed on the DC current . A pure resistor was used to vary the load current. Waveforms of the current and voltage were captured by the use of simulink scopes.

3.2.3 Simulation of a single phase voltage controlled voltage Source inverter (VCVSIs)

3.2.3.1 Introduction

VCVSIs are widely used in power supplies and power quality controllers, as well as in renewable energy, marine and military applications.

Their role in the circuit is to convert a DC current power source into an AC current power source. They require, therefore, a very robust design and high efficiency, especially, when

they are used in DGs or renewable energy applications, where their failure can be costly and irremediable.

The design of inverters has improved since the availability of software and simulation packages such as MATLAB/SIMULINK and PSpice, as well as the development of programmable devices such as DSPs. These allow enhancements to inverter performance at the analysis and design stage rather than time-consuming improvements during implementation.

This chapter of the thesis presents a simulation of a 6 kVA single phase full bridge inverter using MATLAB/SIMULINK. The choice of MATLAB/SIMULINK for modeling and simulations of the inverter's dynamics in this work was influenced by its simplicity in analyzing linear and non-linear systems in continuous time, sampled time or a combination of both.

Mathematical modeling and simulations are used to design the controller of the inverter system which is a non-linear system. The process of generation of inverter output voltage is explained in appendix B.

3.2.3.2 Simulation Using an M-File Code

This section of the chapter gives details about the procedure undertaken to carry out the simulation of the voltage source voltage controlled inverter. First a code which simulates the inverter was designed for use in Matlab. This code was an m-file which was first designed in 2004 by Yasin A.Shiboul [45]. The code was modified to adapt the requirements set out for a case where a 48V DC is used for the inverter's input. The m-file, which gives the simulation results of a single phase voltage source voltage controlled inverter system, is presented in the appendix C, the results of the investigation made to determine the level of distortion of the

inverter's output voltage will be presented in the results section . For simplicity a pure resistor was used as the inverter's load.

3.2.3.3 Simulation with Matlab/Simulink

3.2.3.3.1 Introduction

In this section, simulation procedure of a power inverter in MATLAB/SIMULINK is detailed. The inverter switching process was first investigated; the switching frequency was set to 10 kHz. The inverter was switched in unipolar mode, and the output of the inverter was a PWM waveform. Second, an inductor was added to the output of the inverter for filtering purpose. A 6 kVA power transformer, object of our investigation was then connected to isolate the sources and step up the output voltage. A filter capacitor was connected to the output of the power transformer in parallel with a pure resistor considered as a load. The results obtained using a Simulink model will be compared with those obtained using a Matlab m-file.

3.2.3.3.2 Simulation set-up

a. Simulation without an AC Filter Output

In Figure 3.4 below, a unipolar switching scheme is used to achieve the switching operation of the MOSFETs, the schematic diagram of the inverter used to simulate the inverter's system in Matlab simulink is shown. The system consists of a DC voltage source, 4 power switches to make a bridge, PWM signals for the control of the switches, and a display unit in order to capture the output voltage waveform for discussion.

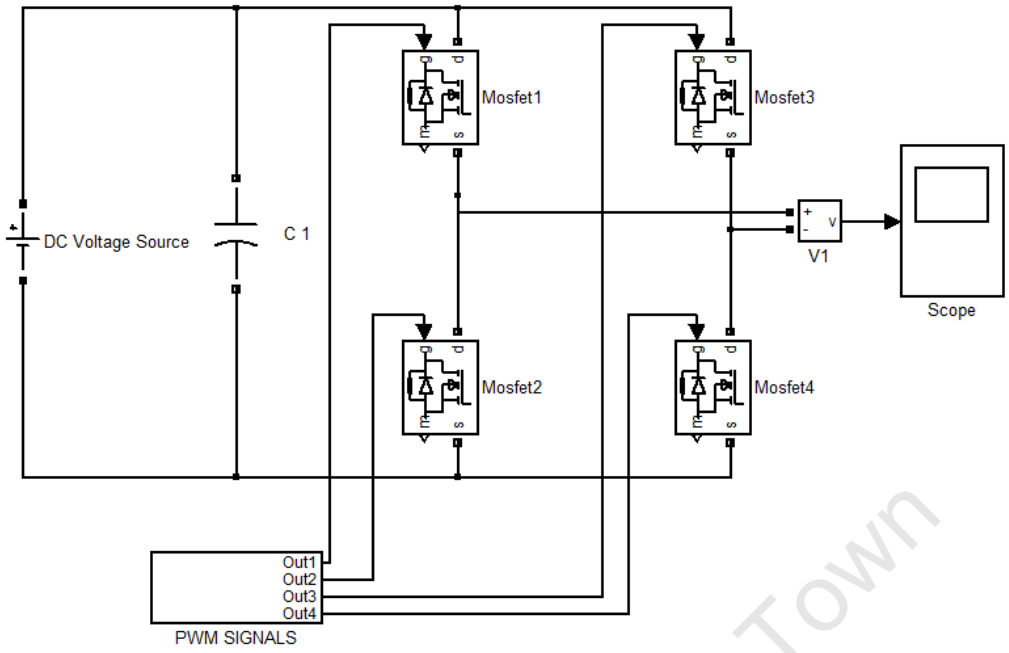


Figure 3.4: MATLAB/SIMULINK Model of a single phase unipolar inverter without filter out

b. Simulation with an AC Filter Output

In this section, simulation of an inverter system with an AC filter is presented. The filter is made of a high frequency inductor, a power transformer whose purpose is to provide isolation and to step up/down the resulting voltage to meet the standard levels of voltage, and a capacitor connected to the output of the power transformer. The simulation was performed using Simulink in Matlab. The value of the high frequency inductor filter was 47µH and the transformer's ratings were 6 kVA at 25.9/230V, the output capacitor value was 33µF and a pure resistor was used as load. In Figure 3.5 below, the Simulink model of the system is presented. This shows a detailed schematic diagram used to investigate the level of distortion in the inverter's output when an AC filter is used to filter out high frequencies resulting from the inverter's switching operation.

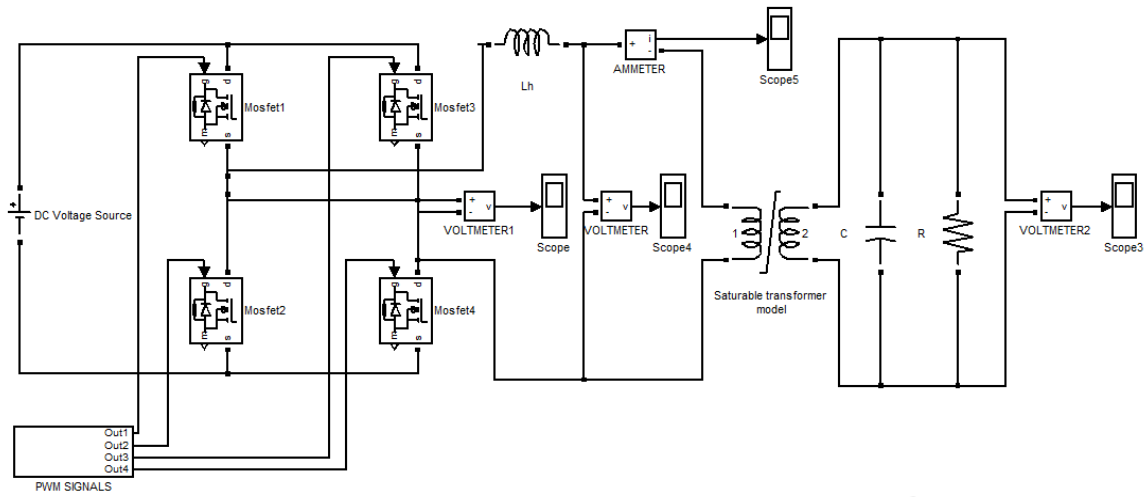


Figure 3.5: Simulink model of the inverter's system with an AC filter

3.3 Laboratory work

The following experiments were performed in the laboratory:

3.3.1 6 kVA Power Transformer

- Determination of the effects that DC bias has in the secondary windings of the 6 kVA power transformer,
- 6 kVA power transformer magnetizing characteristics:
  - a) Under 0 DC injection
  - b) Under DC injection
    - i) At zero AC load
    - ii) When an AC circulates with DC in the secondary windings,
- Prediction of the magnetizing current's distortion resulting from DC offset,
- Shift in the operating point of the core steel characteristics (B-H),

- Harmonics contents in the magnetizing current of a power transformer under different DC injections,
- Harmonics cancellation using extra windings.

The description as well as the experimental set-up for each of these, is described in the following sections.

3.3.1.1 Determination of the Effects that a DC Bias has in the Secondary Windings of a Power Transformer

To determine the effects that a DC bias has in the secondary windings of a power transformer, tests were conducted on a 6 kVA single phase transformer operating under zero AC loading. To achieve this zero AC loading, a voltage cancelling was made with the help of another power transformer of the same characteristics connected in parallel. A diode was incorporated in series to prevent current reversion.

A variable resistor was used to vary the value of the DC bias.

3.3.1.2 Measurements of Power Transformer's Magnetizing Characteristics

This section aims at validating the theory on the operational characteristics of a power transformer under a DC bias.

3.3.1.2.1 Measurement of Power Transformer Magnetizing Characteristics under Alternating Current

To determine the design parameters under non-ideal situation of a 6 kVA power transformer equivalent circuit, two tests were performed; those are open circuit test and short circuit test.

3.3.1.2.2. Measurement of Power Transformer's Magnetizing Characteristics under DC Injection

a) At zero AC

The main objective of this experiment was to determine the magnetizing characteristics of the power transformer when exposed to DC injection and compare the results obtained with the zero DC bias transformer's magnetizing characteristics. The difference in the results obtained will be attributed to the presence of DC within the secondary windings**.**

Description of the Experiment and Set-up

The test set-up consists of two identical 6 kVA single phase power transformers connected in such a way that their secondary voltages oppose each other and, as such, cancel out.

The DC injected in the secondary winding was made through a 12V battery in series with a variable resistor to help in varying the amount of DC current injected.

A diode, D, is connected in series in the secondary circuit to rectify any small amount of current present due to the mis-match of the transformer's secondary voltages.

First, a DC of 125mA was injected into the power transformer.

Thereafter, DC of 270mA, 525mA, and 780mA, were injected one after the other through the use of a variable resistor.

Readings of current, total harmonic distortion THD, crest factor, minimum/maximum values of Current and power were taken by the use of power quality analyser (Chauvin Arnoux). The experimental set-up is shown in figure 3.6.

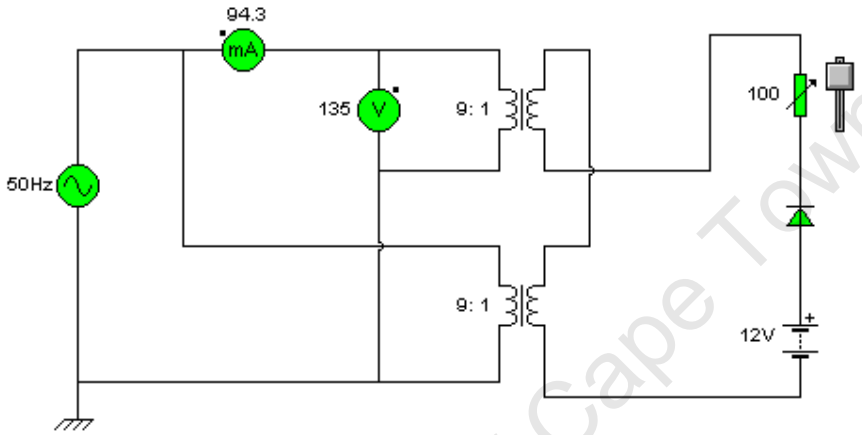


Figure 3.6: Circuit diagram of transformer with a DC injection at zero AC

In the above circuit diagram, an ammeter was used to measure the primary current while a voltmeter, connected in parallel with the supply, was used to measure the primary voltage. The power in the primary was measured by the use of a power quality analyser. Additional readings, namely, the power factor, reactive power, apparent power, total harmonic distortion (THD) etc. were taken with the help of the power quality analyser.

b) When AC Circulates with DC in the Secondary Windings

In this test, an AC load was connected at the secondary terminals of the power transformer. A 12V battery was also inserted in the circuit. The DC was varied with the help of a variable

resistor. In this situation, the AC current and DC current are superimposed in the secondary windings.

Description of the Experiment and Set-Up

Figure 3.7 shows the set up arrangement for this experiment.

A Power Quality Analyser was set in such a manner that readings of AC and Voltage as well as Power could be taken. Additional information was obtained for both the primary and secondary sides by the use of a Power Quality Analyser. A DC Ammeter was connected on the primary side as well as the secondary to enable injected DC readings to be taken.

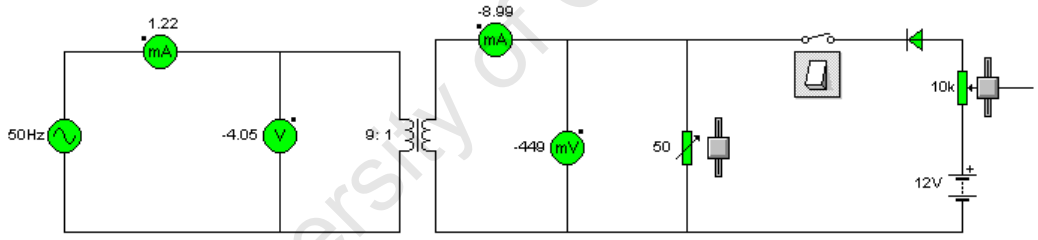


Figure 3.7: Circuit diagram for a transformer with AC load and DC injection

In this test an AC load was connected on the secondary terminals of the power transformer. A 12V battery was inserted in the secondary circuit to introduce a DC component through a variable resistor.

3.3.1.3 Prediction of the Magnetizing Current Distortion Resulting from DC Offset

3.3.1.3.1 Description of the Experiment and Set Up

For this test, the secondary terminals of the power transformer were first connected in such a way that the voltage output was cancelled, the magnetizing current was measured on the primary side by means of a Agilent Technologies DS06012A, a Transcend USB was used to capture the magnetizing current waveform in different scenarios where a DC is injected through the secondary windings. The same magnetizing current waveforms were captured with the scenario when an AC is superimposed to the DC in the secondary windings of the power transformer .The next step was to analyze the results obtained from these tests.

3.3.1.4 Shift in the Operation Point on the Core Steel Characteristic (B-H) Curve

The nonlinear magnetic characteristics of a power transformer core are needed to predict distortion of its primary current due to DC injection. Transformer magnetization curves can also be obtained by measurements. Here the focus is on the measurements of hysteresis to prove that DC introduces a shift in operating point of the magnetizing characteristics.

3.3.1.4.1 Measurements of Practical Hysteresis

A transformer's hysteresis curve provides a graphical representation of the magnetization characteristics of the unit.

This section describes hysteresis tests undertaken on a 6 kVA single phase power transformer. The hysteresis loops were measured with a 50 Hz sinusoidal excitation on a grain orientated silicon steel toroidal core at room temperature. The test core has the following dimensions: outer diameter =240mm, inner diameter =120mm, height =80mm, mean path length =180mm and cross sectional area of 516mm², the primary winding has 178 turns wound on the toroidal core and the secondary windings has 20 turns also wound on the

toroidal core . The methodology employed as well as the validity of the results will be detailed in the following sections.

a. Experimental Set Up and Circuit Diagram

The circuit diagram used to conduct the hysteresis test relies on the fact that the flux is the integral of the voltage.

By assuming the series parameters of the transformer electrical equivalent circuit negligible, the flux values were obtained by integrating the supply voltage by the use of a RC circuit as shown in the figure below:

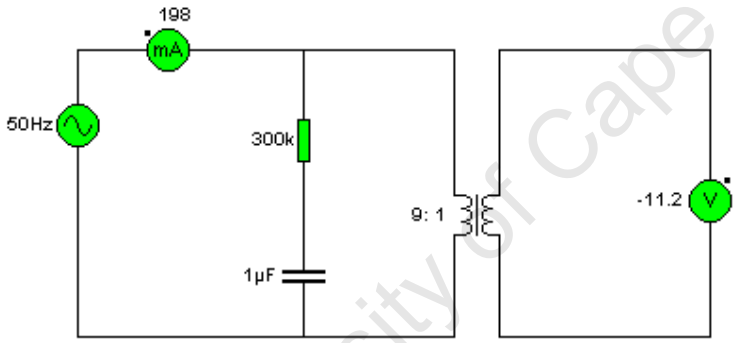


Figure 3.8: Diagram of a voltage integrator

The series RC circuit was arranged so that the capacitive reactance at 50Hz is significantly less than the series resistor value and as such a reasonably accurate integration would be obtained. The measurement of the hysteresis loop was obtained using an Agilent Technologies DS06012A oscilloscope whose channel 2 has been placed across the capacitor, using high voltage probe interface.

The Agilent Technologies DS06012A was set to the x-y plot mode, channel 1 was connected to a current transformer whose role was to measure the magnetizing current of the

transformer, channel 2 will be the “y” axis and channel 1 will be the “x” axis. All the connections to the channels were made via high voltage probes interfaces.

The supply voltage was varied for values of -17.4%, -8.6%, +8.6% and +17.4% of its nominal value , readings were taken, and hysteresis loop captured by a digital camera.

The next experiment was the measurements of the hysteresis loops when the power transformer is subjected to an increasing value of DC injection.

Once again, it was assumed that the transformer’s series parameters are negligible and by connected another transformer in anti-parallel on the same source dual voltage cancellation was obtained which allowed a pure DC to be injected from the transformer secondary windings. The arrangement of the set up is show in the figure 3.9 below:

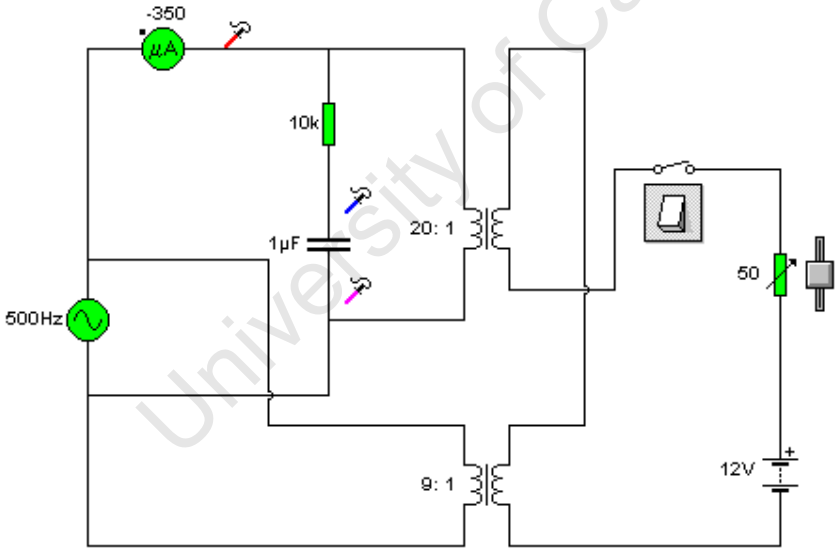


Figure 3.9: Diagram used for hysteresis measurements

3.3.1.5 Harmonic Contents in the Magnetizing Current of a Transformer under Different DC Injection

3.3.1.5.1. Transformer Magnetizing Current Harmonic Contents at Zero AC Load

The main objective of this experiment was to determine the magnetizing current harmonics contents in the power transformer when exposed to DC current injection.

a. Description of the Experiment and Set-Up

The test set-up consists of two identical 6 kVA single phase power transformers connected in such a way that their secondary voltage oppose each other and, as such, cancel out.

The DC current injected in the secondary winding is made from a DC-DC converter in series with a variable resistor to help in varying the amount of DC current injected.

The supply voltage was varied, from 21.5V (under voltage operation), to 25.8V which is the transformer nominal voltage.

The DC current injection was then varied for all those different values of voltage. Readings of total magnetizing current, harmonic contents, reactive power, total harmonic distortion THD were taken. The figure below depicts the experimental set-up:

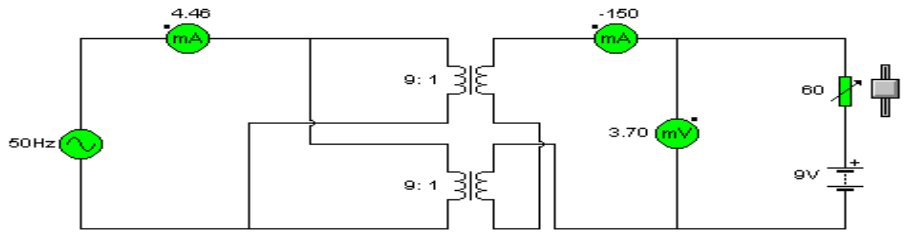


Figure 3.10: Circuit diagram of transformer magnetizing current measurements when a DC current is injected

3.3.1.5.2 Transformer's Primary Current Harmonic Contents when DC is superimposed to AC in the Power Transformer's Secondary Windings.

a. Description of the Experiment and Set-up

In this test, an AC non-linear load was connected at the secondary terminals of the power transformer. The non-linear load consisted of a half-wave rectifier. Due to this, a DC current was superimposed on the AC current in the secondary windings. The DC current injected was varied using a variable resistor. The figure below shows the experimental set-up and arrangement of the measuring devices. A power quality analyzer was set in such a manner that readings of AC voltage and current on the primary side as well as on the secondary side could be taken. An oscilloscope was used to take readings of different harmonics. An ammeter was connected in series on the secondary side as well on the primary side to measure the injected DC current.

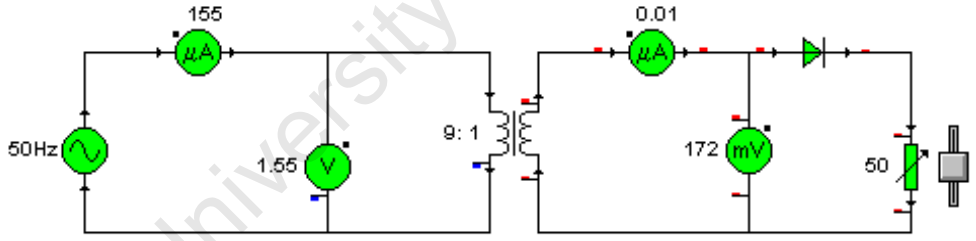


Figure 3.11: Circuit diagram for a transformer with AC load and DC current injection

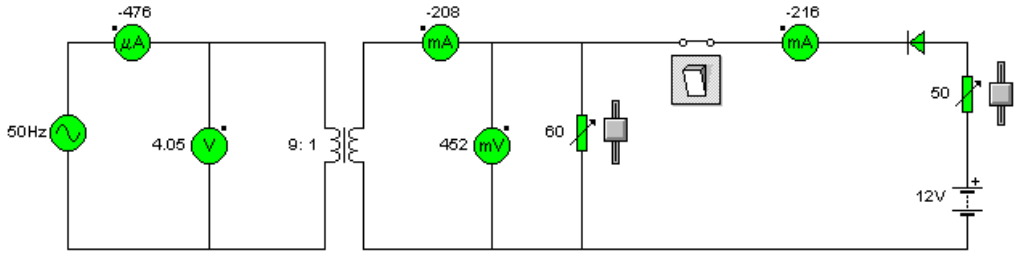


Figure 3.12: Circuit diagram for a transformer with AC load and DC current injection

3.3.2 Prototype of the inverter

The prototype of the inverter system was designed and built over a 6 month period at the power laboratory of the University of Cape Town with components provided by MLT Drives CC (see appendix D). The prototype was designed not only for the validation of the theory but also for obtaining simulation results in the actual situation in order to mitigate adverse effects arising from DC current under various loads.

The following equipment was used to build the DSP-based single phase inverter system:

- A DC battery bank to provide DC voltage input to the inverter at 48 VDC,
- Four power MOSFETs mounted on heatshink,
- A DC Capacitor link, rated at 33000 μF, 62 V,
- A High frequency inductor rated at 42 μH,
- A 6 kVA power transformer,
- An AC capacitor rated at 30μF, at 400 V,
- Linear load,
- Non-linear load, rectifier in nature,
- Asymmetrical loads,
- A DSP Controller, TMS320LF2407.

The following experiments were performed in the laboratory on the prototype inverter:

- Measurements without inverter's output filter;
- Measurements with inverter's output filter;
- Harmonics cancellation using extra windings;
- Transformer's primary current second harmonic extraction;
- Mitigation of the transformer's primary current second harmonic content.

3.4 Mitigation of the Undesired Effects of DC Offset

3.4.1 Introduction.

The undesired effects of DC current on power transformer have been discussed in chapter 2. In this section of the chapter, an approach to remove the DC mmf offset before it becomes a threat to the power transformer is investigated and implemented. The mitigating methodology requires operating properly for both situations when the DC offset is caused by an injection from the primary side or from a bias in the secondary side. The methodology first consists of assessing the level of magnetic flux asymmetry by observing the second current harmonics on the primary side (inverter side). This indicator is then used as a feedback signal to the inverter DSP controller to introduce the necessary DC voltage bias that will introduce a mitigating DC current for the purpose of counteracting the undesired DC mmf, so that the sums of all DC mmf is zero.

This chapter also deals with the cancellation of magnetic flux distortion by using a transformer extra windings (third winding) so as to show that the undesired DC mmf can also be counteracted by introducing a DC current into a third winding of the transformer under investigation.

3.4.2 Harmonics cancellation using extra windings

The main objective of this experiment was to determine the level of cancellation that could be achieved by first proving the principle of DC mmf cancellation by using extra windings subjected to DC current.

3.4.2.1 Experiment set up

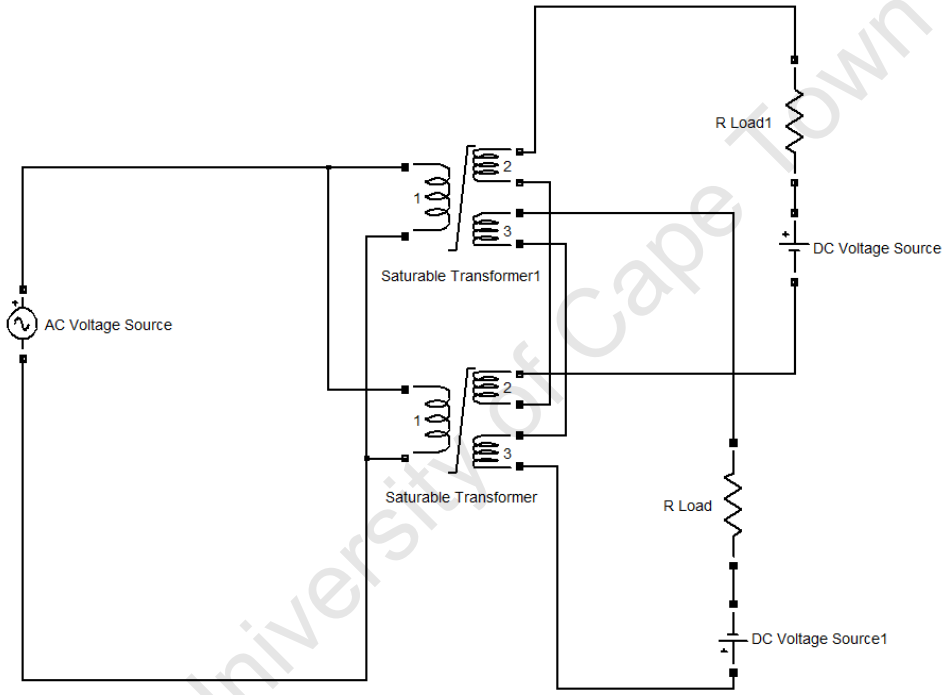


Figure 3.13: Harmonic cancellation using extra windings

Figure 3.13 depicts the set-up of the experiment conducted to investigate the level of mitigation of harmonics that can be achieved by introducing DC current into a third winding.

For this purpose, two similar 6 kVA power transformers (The top is the one under investigation) and the second transformer B to facilitate the introduction of DC current [Appendix D] were connected in parallel on the primary side and into anti-series on the

secondary and third winding so as to cancel the total AC voltage seen by the DC power supply which introduces a DC current bias on the secondary of transformer A. The same principle was applied to the third windings so as to facilitate the injection of the mitigating DC ampere turns into the third winding of transformer A. The DC current into the third winding was also introduced with the aid of a battery and variable resistance.

3.4.3 DC elimination in single phase inverter system

3.4.3.1 Introduction

As presented in the previous chapters, to satisfy the requirement of higher reliability of inverter systems, an isolation transformer is usually incorporated between the PWM inverter systems and the load or transmission system in case of grid connected inverter systems.

The reason as previously stated is the existence of a DC component which can result either from the primary side or the secondary side of a transformer. This DC current can originate from the given sinusoidal modulating wave or the carrier, due to the non-uniform storage time of power switches and the dead zone of driving signals, and the use of asymmetrical loads on the secondary side of the power transformer. This DC current may seriously arouse saturation of the core and lead to overload and output distortion, which seriously affects the proper function of the inverter. In this chapter, a valid solution is proposed. The flux balance is achieved by mitigation of some of the effects that the DC current can have on the power transformer. The solution involves the sampling of the instantaneous transformer primary current and extract the second harmonic current component so to use as a feedback indicator to shift or delay the switching time according to the sensed DC offset. Design guidelines are provided and experimental results are presented.

3.4.3.2 Proposed topology for DC offset and Even Harmonics Control System in a Power Inverter

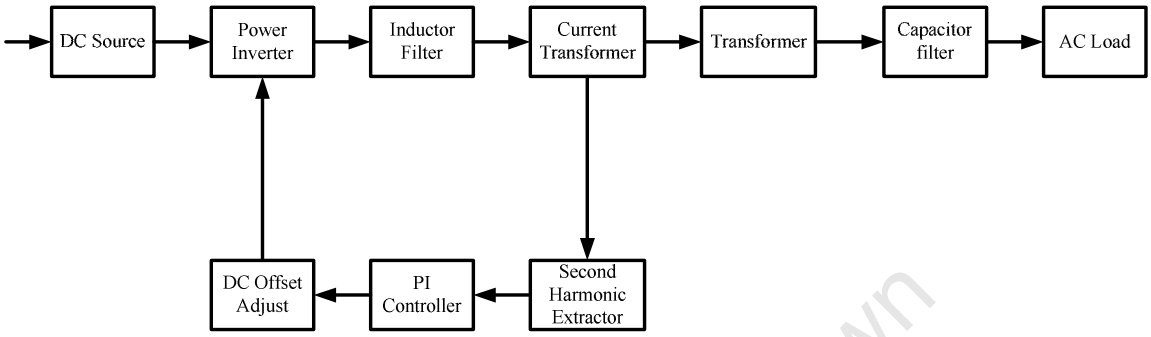


Figure 3.14: Block diagram of the proposed topology

The control system proposed above is inserted between a DC power source and a utility to control the injection of DC current and even harmonics into the utility. The control system can be used in grid tied inverter systems or in standalone inverter systems. The system includes a power inverter that provides the function of converting the power from a DC source to AC energy with a desired shape.

An LC filter is then connected to the output of the inverter to eliminate high frequency components of the current signal and pass only low frequency components of the output current signal. A voltage transformer is then connected to block DC current and isolate the power source from the utility or utility grid. A feedback control loop is included in the control system, measuring, with a pair of current transformers, DC current and even harmonics in the current flowing into and out of the power transformer. A signal combiner is used to combine the outputs of the two current transformers such that its output to a second harmonic extractor represents both the inductor current and the load current of the voltage transformer. The second harmonic extractor determines the magnitude of the second

harmonic which is used in the feedback control loop through the feedback controller. The controller creates a control signal that is used to create a DC control signal in proportion to the second current harmonic.

A reference signal is then used to control the operation and output the power converter to force the total DC mmf to be zero. This is manifested by the suppression of the second current harmonic in particular.

In the following section the experimental stages undergone to extract and then mitigate the second harmonic content in the power transformer's primary current are explained.

3.4.3.3 Transformer's Primary Current Second Harmonic Content.

The extraction of the second primary side current (PWM inverter side) harmonic was achieved by using a second harmonic band pass filter which was designed and implemented by the Author**.** To be able to extract the second harmonic from the power transformer primary current, some conditions needed to be met to ensure sufficient accuracy of the extracted information. These were:

- The circuit designed to extract the second harmonic must not introduce any additional offset current. This could lead to over- or under-correction of the DC offset error, resulting in a worse situation.
- The measurement process should be able to extract the totality of the second harmonic so that total mitigation could be achieved. Failure to do so would prevent total removal of DC mmf bias in the inverter transformer core.

3.4.3.4 Band Pass Filter

For the purpose of extracting a second harmonic from the inverter output power transformer current, a filter which had to extract a frequency of 100 Hz from the transformer's primary current was designed**.** The filter was built in the laboratory and tested. Using the available resistor and capacitor values to build the filter introduced an error through their values' tolerance. To overcome this problem, 3 similar filters were connected in series so that the band pass was narrowed. In figure 3.15 below, the schematic diagram used to implement the band pass filter is presented.

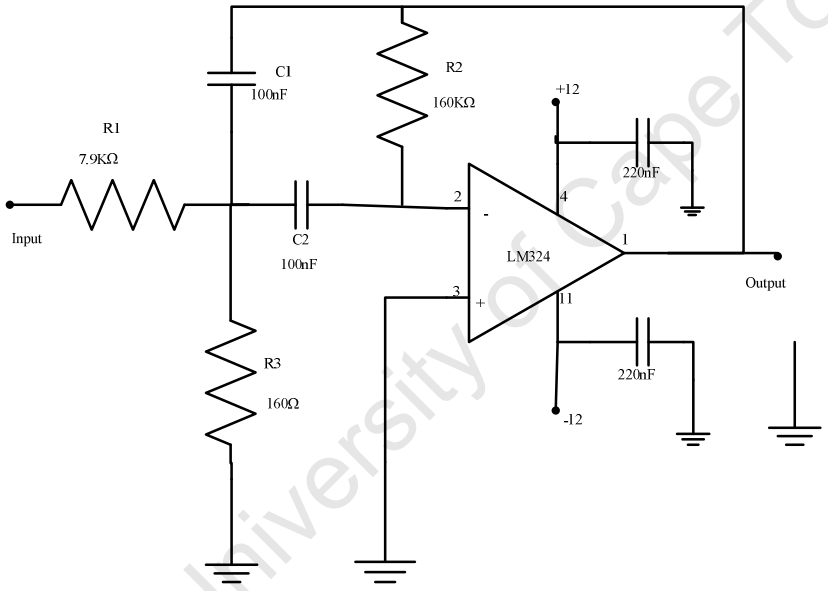


Figure 3.15: Band pass filter (Second harmonics extractor)

Chapter 4

SYSTEM DESIGN

4.1 Introduction

The single phase inverter system consists of two main parts, namely:

- The power circuit
- The control circuit

The power circuit is mostly composed of high current and high voltage components and the control circuit is mostly made up of electronic components such as DSP which do not require high level signals of voltage to operate. In this chapter, the design and implementation of the inverter parts will be discussed.

4.2 System Hardware

4.2.1 Power Circuit

The power circuit is composed of four parts, namely a full bridge inverter circuit, a DC power source which consists of batteries, a LC passive filter with a power transformer, and the load. The battery used in this project was rated at a voltage of 12VDC and since the inverter's input voltage is set at 48VDC. Four batteries were connected in series to give the required

48VDC. The rating of these batteries is of 100AH. Power switches were then connected in a bridge mode to make a full bridge inverter.

PWM inverters use semiconductor devices as switches and this is always a source of harmonics in the system. The switching frequency harmonics and their multiples are mostly removed by an LC filter. The resultant output is a sinewave which is the fundamental.

The isolation between the two types of power source, that is, AC and DC, is provided by a power transformer which also provides the step up to the output voltage of the inverter. The load varies according to the application of the inverter. Figure 4.1 below depicts the power circuit of an inverter system.

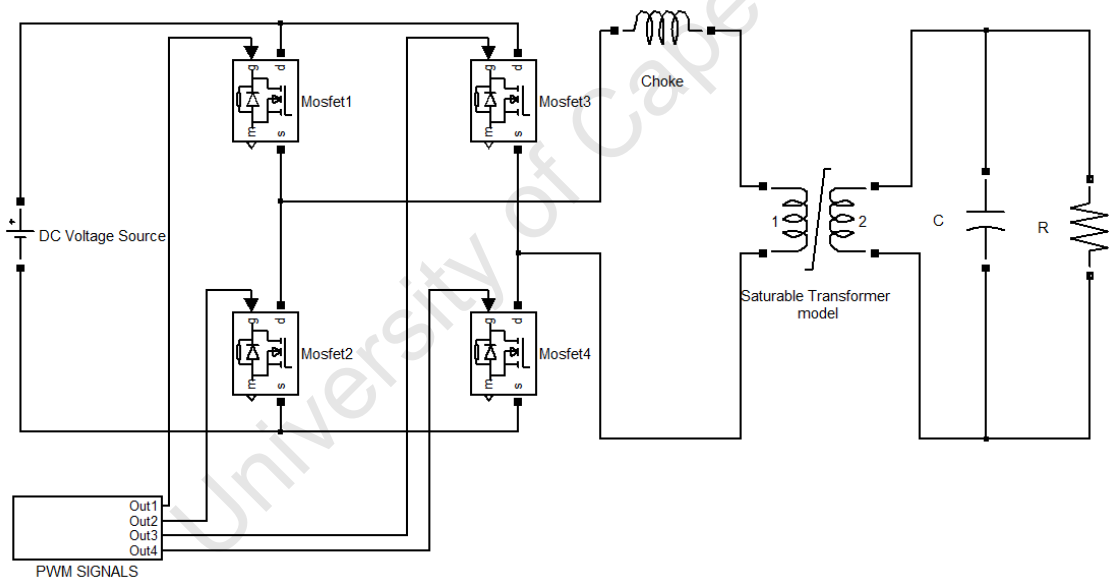


Figure 4.1: Power circuit of an inverter system

4.2.1.1 DC Link Capacitors and Output Capacitor

The purpose of inserting the capacitors in parallel with the DC power source at the input of a power inverter is to decrease the impedance of the source, hence minimizing the impact of

the high ripple currents on high density storage devices like battery packs and to ameliorate the impact of switching voltage transients on the power semiconductor devices, referred to as MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in this case. The link capacitor used in this design has a capacitance value of 3300μF, and the capacitor used at the output of the power transformer has a capacitance value of 30 μF rated at 440V and 50 Hz.

4.2.1.2 Power Switches

The inverter power circuit consists of switching devices which, in this case, are power MOSFET. These switching devices are current controlled devices. A block of paralleled FETs manufactured by called MLT Drives are used in this project. The advantages of using MOSFET for power switching are listed in the appendix E. The block of paralleled FETs is shown in Figure 4.2 below:

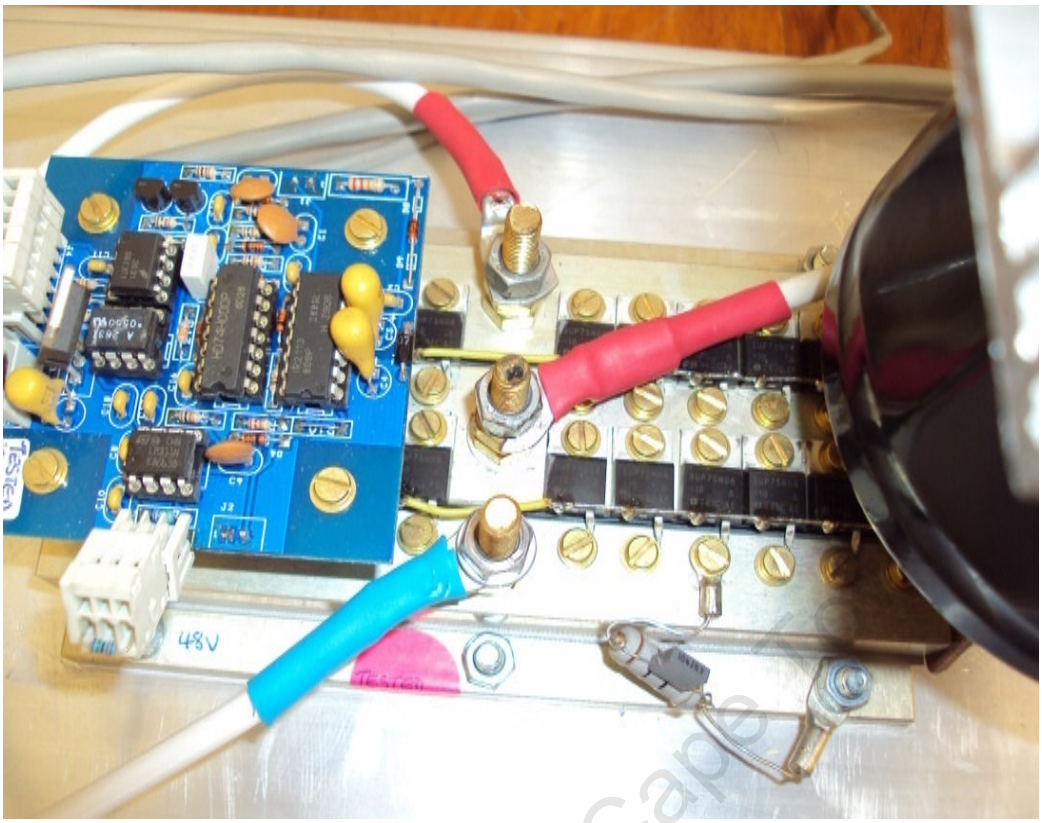


Figure 4.2: Paralleled FET switches

4.2.1.3 FET Driver [Appendix F]

The FET driver used in this project was designed by Engineers at MLT Drives (MLT Drives, 2004). The PWM signals created by the DSP are 0 to 5 volts at a very small current. In view of the fact that the output pins of the DSP do not provide the correct voltage and current to drive the MOSFETs, an MLT driver board was, therefore, used to produce the signals that drive the power MOSFETs by amplifying the DSP output signals to the required level for triggering the MOSFETs.

The driver board is powered by an isolated 15 volt supply from the special power supply provided by MLT Drives. A dead time is implemented on the driver board to avoid shoot through faults. The driver also protects the MOSFET by switching off an over current. The

driver board uses an opto-isolator to isolate the DSP signal from the MOSFET. Not AND (NAND) gates amplify the DSP current to supply other chips which require high levels of current to operate. The output of the amplifier is connected to an opto-isolator which changes the signal path from electrical to optical, then back to an electrical signal. The optical transmission provides necessary galvanic insulation between the power side of the inverter and the DSP. This isolation is necessary because the DSP is a very sensitive device, while the inverter is a major source of interference. The operation amplifier feeds the input or luminescent diode of the opto-isolator. The output of the opto-isolator feeds into the DSP analog input. A variable collector resistor was used to set the offset voltage of the DC input. Figure 4.3 below depicts the FET driver card used in this project.

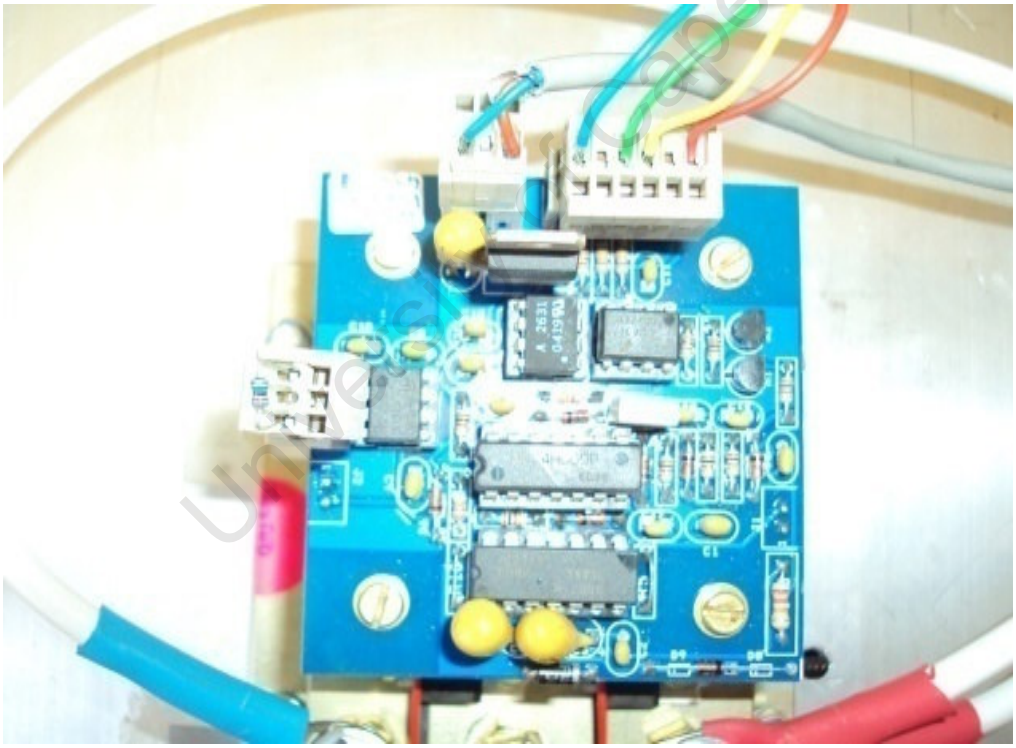


Figure 4.3: FET driver board

4.2.1.4 Inductor Design

A 47μH high frequency inductor was used at the output of the inverter to filter out all high frequency resulting from the inverter switching. This was provided by MLT Drives.

4.2.1.5 6 kVA Power Transformer

A single phase two windings power transformer was connected at the output of the inductor filter. This power transformer was the object of the investigation in this project to see how the effects of a DC offset injection into the power transformer could be mitigated. The work carried out to determine the characteristics of the power transformer is described in Appendix G, where the magnetizing characteristics as well as the transformer's efficiencies at different levels of loading are detailed. A 6 kVA power transformer that was under the study was provided by MLT Drives which were used for isolation and stepping up the voltage in the manufacture of MLT 6 kVA power inverter. Figures 4.4 a,b show the magnetic core of the transformer under investigation.

Figure 4.4 a: 6 kVA power transformer core without windings

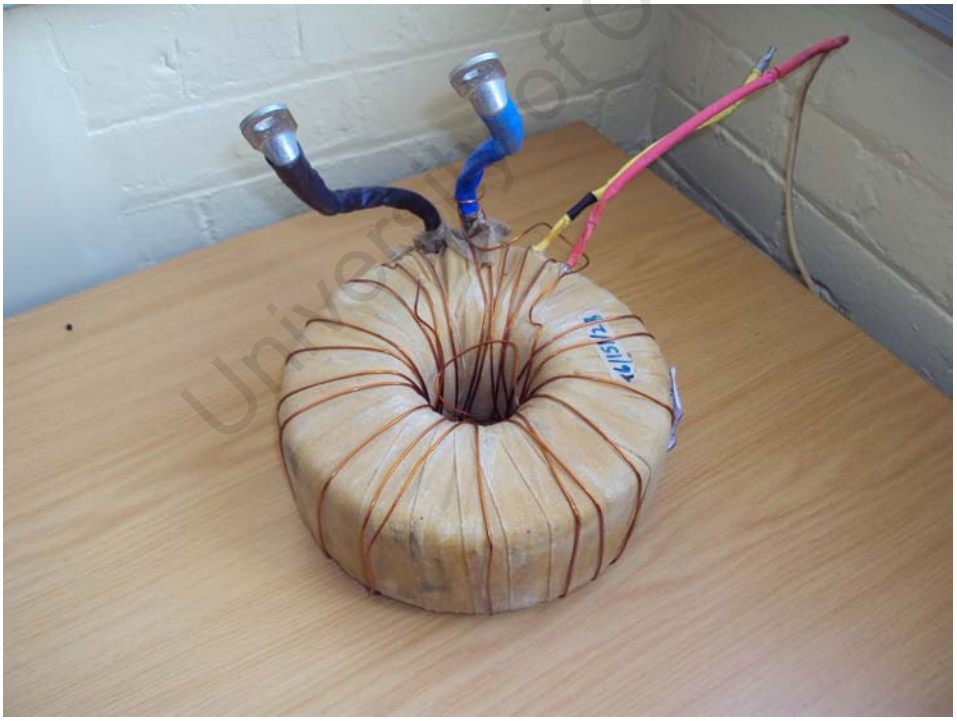


Figure 4.4 b: 6 kVA Power transformers with the 3rd windings added for the purpose of investigation

4.2.2 Control Circuit

The controller topologies are discussed in the section below. The voltage regulation was achieved by using a P controller whilst the second harmonic suppression was achieved by using a PI controller. Both controllers use a closed loop system where the output voltage and the inductor current second harmonic are fed back to the DSP. The Section deals only with the voltage regulator since the second harmonic extraction and control will be presented in further chapters. To control the regulation of the inverter voltage with DSP, two digital outputs and one analog input are required from the DSP. Figure 4.5 below shows a conceptual connection diagram between the DSP and the inverter. The DSP will output a PWM switching waveform to the inverter.

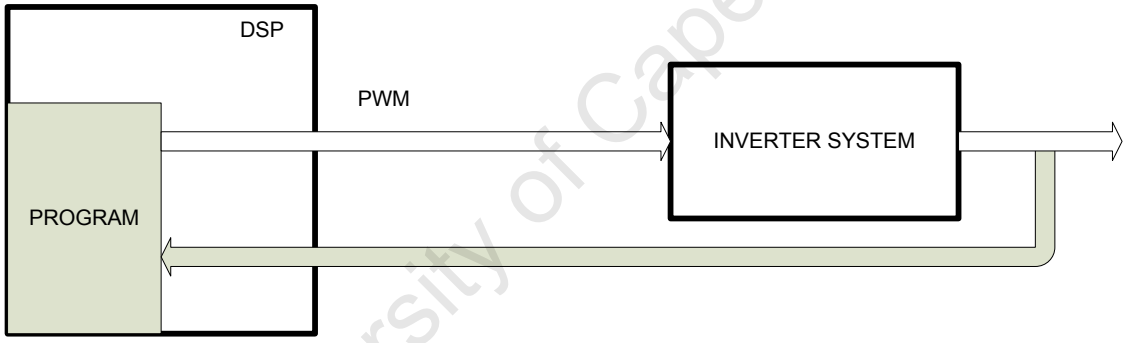


Figure 4.5: Physical implementation of inverter voltage controller

4.2.2.1 Power Supply Design

In an inverter system the controller should be powered from the DC bus or from any other separate power source. The power supply provides power to the DSP, MOSFETs and other devices that need power to operate. The design of the power supply used in this project was based on the Viper50/SP chip. This chip has the ability to power itself up and regulate its output over a wide range of input voltage. The power supply was manufactured and tested at

MLT Drives (MLT Drives, 2004). It was also adapted to the inverter system presented in this thesis. Below is the figure that depicts the above defined power supply:

Figure 4.6: Power supply

The power supply takes its power from either the DC bus of the inverter or from an AC source. In this project, an AC source was used as an input to the power supply, thereby creating the need to use a single phase rectifier on the power supply layout for the AC rectification purpose. The specifications of the wide range power supply are:

- Input Voltage Range : 35VDC to 400VDC
- Output 1: + 5V DC / 500 mA
- Output 2: + 15V DC / 100 mA
- Output 3: - 15 V DC / 100 mA
- Output 4 : + 15V DC /100 mA

Outputs 1, 2 and 3 have the same reference of 0 volts, and are used to power the DSP, the interface board and the measurement devices. Output 4 is an isolated supply which means that its reference is different from the one used for outputs 1, 2 or 3. Output 4 powers the driver board used to operate the MOSFETs.

4.2.2.2 Current and Voltage Sensors

4.2.2.2.1 Current Sensor

This section will not discuss the current sensor since in this project only a voltage signal is used to provide the regulation of the inverter output voltage. The analog to digital conversion of the voltage was done at 10 KHz. After digitalizing, the output voltage was compared to a set point voltage which is set through the DSP Code. The error was then used as the input to the digitally implemented P controller. The output of the P controller is the duty cycle used to control the switching of the MOSFET. By controlling the duty cycle, the output voltage of the inverter system is controlled to force the system to track the desired voltage waveform at the output of the inverter.

The next section details the controller used to implement the 6 kVA inverter system. Its features are provided as well as information regarding the interface card used to condition the signals so that they can be processed by the controller.

4.3 DSP Controller and Interface Card

4.3.1 Introduction to the TMS320 LF 2407 DSP Controller

The Texas Instruments TMS320 LF 2407 DSP Controller is a programmable digital controller with a C2xx DSP central processing unit (CPU) as the core processor. The LF2407 contains the DSP core processor and useful peripheral integrated onto a single piece of

silicon. The LF 2407 combines a powerful CPU with on-chip memory and peripherals integrated into a single chip. This minimizes circuit board space thus reducing circuit board and system overall costs.

The LF 2407 DSP controller offers 40 million instructions per second (MIPS) performance. The fast processing speed of the C2xx CPU allows users to compute parameters in real time rather than having to look up approximations from tables stored in memory. This fast performance is well suited to processing control parameters in applications such as notch filters and sensor less motor control algorithms where a large amount of calculations must be computed quickly. Figure 4.7 depicts the TMS320 LF 2407 DSP and technical data and information sheets pertaining to this type of Controller are provided in Appendix H.

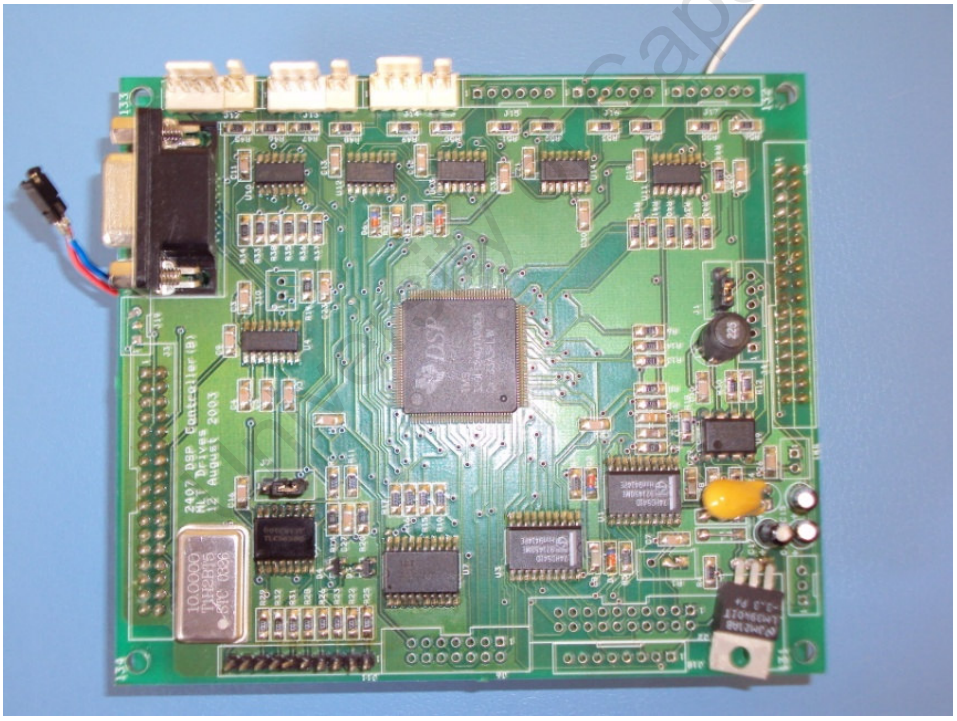


Figure 4.7: TMS320LF2407 DSP board

4.3.2 Interface Card

The operating voltages and currents of a DSP are limited to certain values which do not necessarily correspond to the real world values which need to be processed by the DSP. Thus there is a need to condition the signal prior to its insertion into the DSP for processing. This makes it necessary to use an interface card as a means of conditioning the signal being measured from the system in order to sample it and process it digitally. After it is sampled the signal is used to implement the desired algorithm by using the DSP. Figure 4.8 below depicts the interface card used in this project.

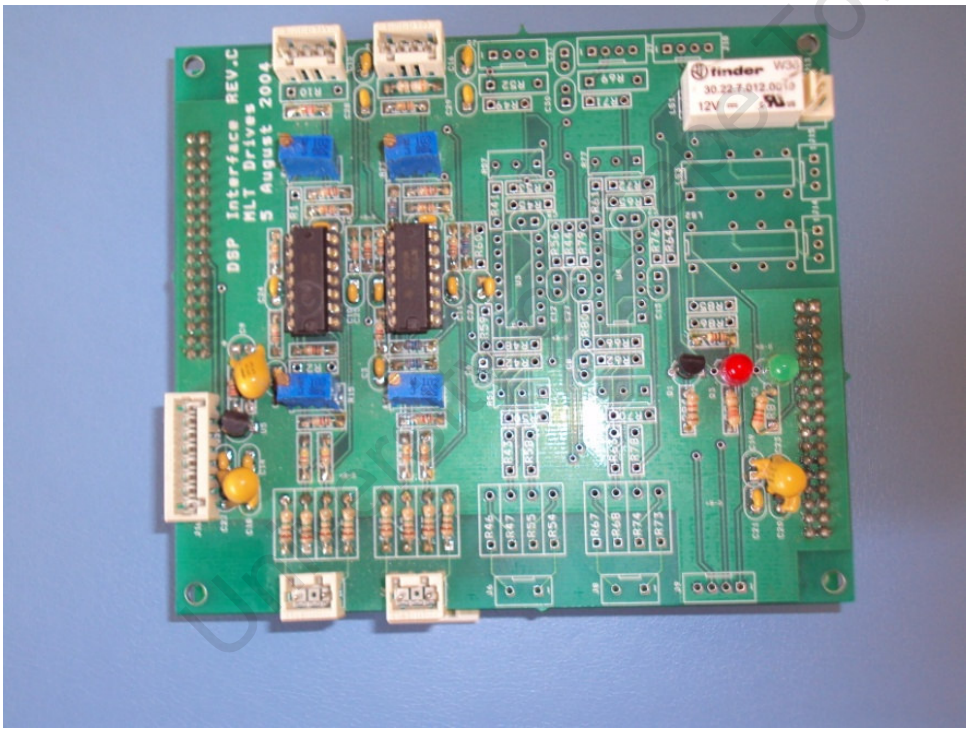


Figure 4.8: TMS320LF2407 DSP interface card

The interface card contains a resistive network and op-amps used to condition the signal being measured from the system. Voltage and current signal conditioning circuits are provided on the interface board since the voltage signal is usually greater than the allowed

input value of the DSP. The voltage signal needs to be attenuated to prevent any damage to the DSP.

The current is usually processed through an amplifier which increases it value prior to processing.

In this project, two signals were captured from the output of the inverter system and fed back to the DSP, these are:

- The output voltage
- The power transformer primary current second harmonic component

The input of the analog to digital converter ranges from 0 to 3.3 volts. The peak output voltage is 325 volts and this voltage should correspond to 3.3 V after conditioning. Figure 4.9 below illustrates the conditioning circuit used to measure the output voltage. The voltage is taken directly from the output capacitor filter and plugged into the interface card which has on its board resistors op-amp for signal condition purposes. Figure 4.9 below depicts the circuit used for voltage signal conditioning.

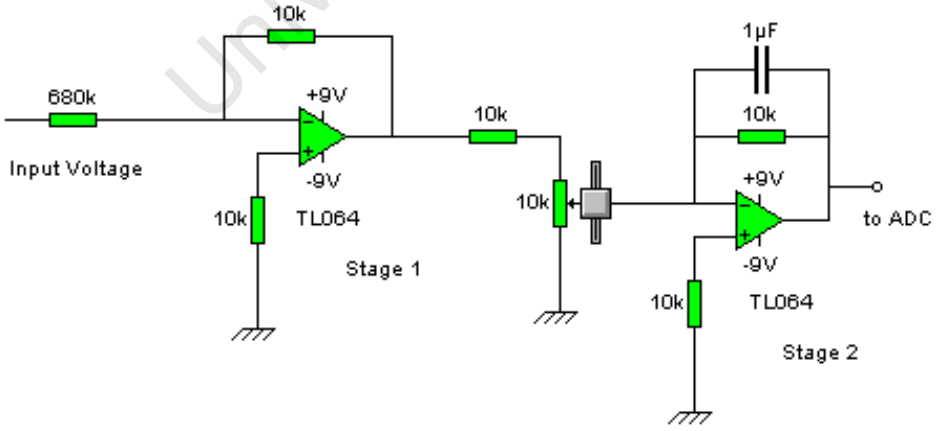


Figure 4.9: Voltage signal conditioning circuit

The op-amp at stage1 buffers the voltage input to the DSP and a potentiometer is used to calibrate the signal being measured to compensate for the inaccuracies introduced in the measurements by the tolerance of the resistors and capacitors used. At stage 2, the measurement signals are filtered to remove any noise pickup from the system and measurement cables. A schematic of the interface card used for the 6 kVA inverter system is provided in Appendix I.

4.3.2.1 Real and Digital Values

The analog to digital converter included in the TMS320 LF 2407 DSP provides the function of converting the analog signal captured at the output of the Inverter system into a corresponding digital value. The input voltage range of the ADC is from 0 to 3.3 volts. In order to use the measured voltage and current, these must be converted from digital values into volts and amperes.

In the following section, an algorithm designed to implement a digitally controlled inverter system will be explained. Details will be provided concerning how software enables the DSP to do specific tasks.

4.4 Software Design

4.4.1 Introduction

This chapter describes the program that implements a closed loop control system for a single phase unipolar switch mode inverter using the TMS320LF2407 DSP. The programming process of the DSP was carried out in C. During the process the inverter output's voltage used for the closed loop feedback is instantly sensed and fed to the DSP by the use of one of

the channels of the ADC. The sections given below provide a detailed overview of how the software for this project was designed and implemented.

4.4.2 Program Structure

This project involved the development of software that provides the digital control algorithm of a single phase inverter.

1) PWM pattern was achieved using a TMS320 LF 2407 DSP. The details of how the PWM signals were generated are provided below and the code generated in the DSP is provided in Appendix J. The PWM generated were used to investigate the switching process of the inverter, to find out if the hardware was responding correctly to the DSP implemented code.
2) A regulation code was designed for the case where the inverter's output was filtered to extract the desired voltage waveform and eliminate all the unwanted frequencies. The code incorporating the regulation process can be found in Appendix J.

4.4.2.1 Generation of Single Phase PWM Patterns

This section of the chapter presents the process undertaken to generate the PWM patterns used to switch the inverter power circuit. The generation of PWM patterns comprised the following steps as depicted in the Figure 4.10 below:

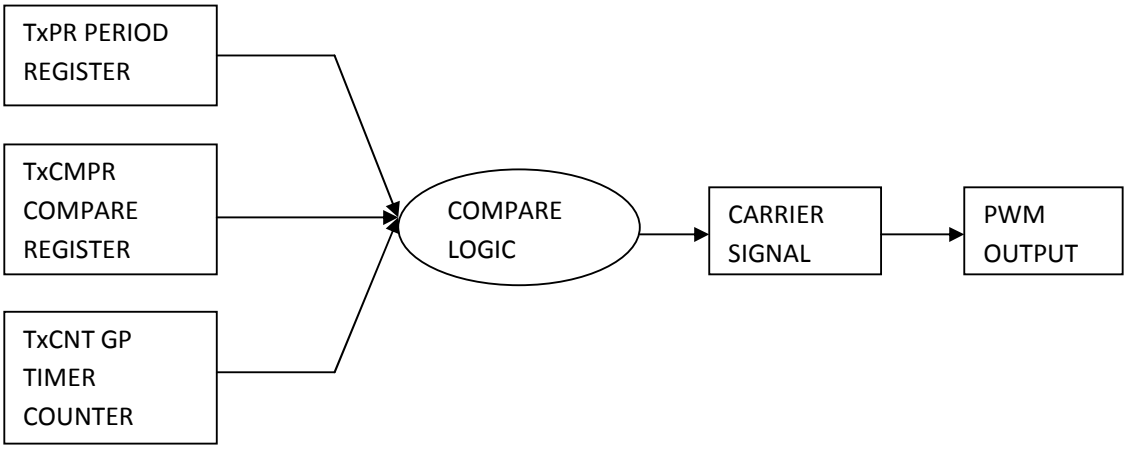


Figure 4.10: Generation of single phase PWM patterns

- Counting Mode (Continuous Up, Continuous Up/Down)

To obtain the carrier signal for a PWM algorithm, continuous up or continuous up/down counting mode must be selected by using TxCON register value. The continuous up mode results in an asymmetric carrier signal and continuous up/down mode results in a symmetric carrier signal

- General Purpose GP Timer Compare Operation

Every GP timer has compare register TxCMPR and an output pin TxPWM. The value of the compare register is compared with the value of GP Timer counter (Carrier Signal). The PWM changes its state (from 0 to 1 or from 1 to 0) when the comparison is a match. Figure 4.11 below illustrates the generation of PWM signals with a symmetric carrier signal. The timer is in continuous count up/down mode. During each timer period, the carrier signal was compared with the value stored in the compare register TxCMPR, and the + sign in the Figure 4.11 represents the compare matches. Before the first match PWM x+1 is zero and PWM x is logic 1 and the value of the compare register is greater than the value of the carrier signal.

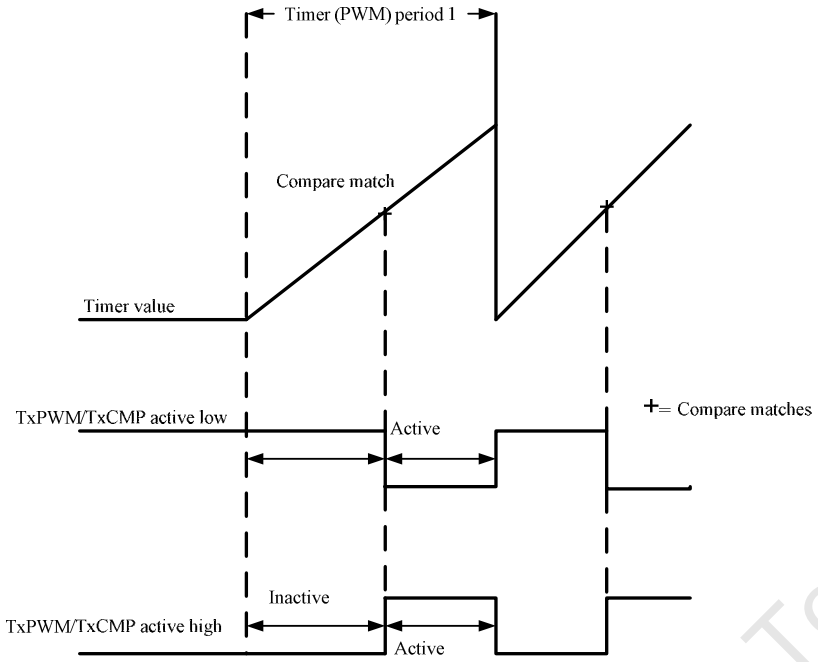


Figure 4.11: Timer compare match and associated change on TxPWM Pin

- ❖ Code Source to Machine Code [46]

The code generation process was done using C and compiled to translate the source code to the machine readable code (the binary code). The following file systems were provided within the compiler development environment to help in performing the Compile-Link-Program (CLP) Routine.

- ✓ *Compiler.Bat File*

Compiler .bat is the command to start compiling the program code. The compiler links the run.c code with the included header files (with suffix .h). Compiling generates the following files with the following suffixes and links the entire executable files to produce a run.out file:

- *.asm: is the assembler code generated
- *.lst is the assembler code with print layout and line numbers
- *.err is the error information if compilation was successful

- Run.obj file is the compiler user code that is generated as a result of successful compilation
- *.map is the memory allocation configuration and all global variables
- *.cmd is the file that contains all the *.obj files that are not generated by the compiler but are needed to run the project
- *.inf is the information about the section size and memory allocation
- Run. out is the executable file generated by linking the executable files with Run.obj

✓ *Con_Prg.bat file*

Con_Prg.bat is the command that starts the hex converter and the serial programmer using the Run.out file to program DSP flash RAM.

❖ **Compiler-Link-Program Routine Common Errors**

- A Folder path problem can occur when CLP runs the run.c code in the same folder as the Compiler.bat file. For this reason to run a new code it is necessary to replace the old run.c code in the correct folder with the new one. If the new code is saved in a different folder the CLP will run the old code.
- When using interrupts one has to replace branch.obj with ints.obj in cmd file. Branch.obj is invoked by the linker to perform a simple jump to the start address of the running program, whereas an interrupt is a jump to a specific address in the program memory.

4.4.2.2 Reading Voltage Sensors

A feedback control loop was created through software by using ADC and a sampling technique. The details about the process undertaken to create the code that enables the control loop are provided in the Sections below.

4.4.3 Main Program Flow Chart

Figure 4.12 illustrates the main program flow chart of the software created in this project. First, a software initialization of all variables was undertaken. Then desirable registers and interrupts were enabled. Unused interrupts were masked, and then both Timers, i.e. Timer 1 and Timer 2 were configured. The program loops in the background routine performing all nontime critical functions. The background routine is the main program loop that ensures that the program has defined bounds. The program code is shown in Appendix J.

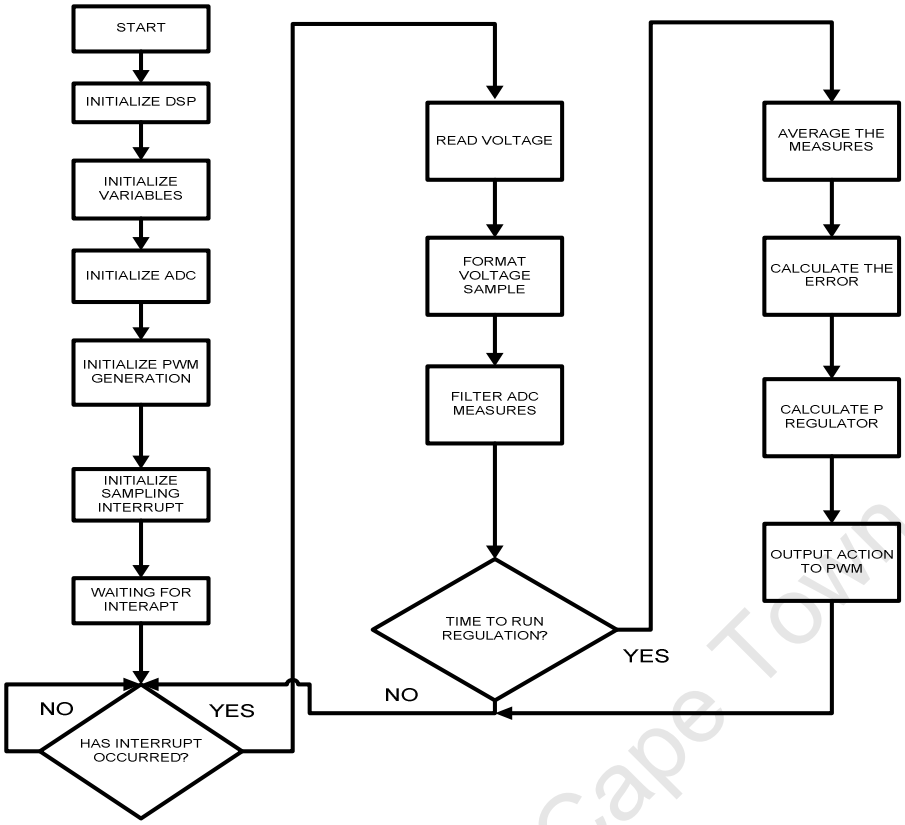


Figure 4.12: General program flow chart

The flow chart above depicts the startup procedure of the main routine which is a very important step as the main components for the running of the software are set during this process. The procedure consisted of assigning values to registers that would dictate the behavior of the pointer assigned to the register. First, the PWM output was assigned to particular output pins and these have to be set to zero. This avoids the sending of random signals to the MOSFET before the interrupt service routine is called upon for the first time. These arbitrary signals could switch the MOSFET on or off without any proper control and may cause damage to the system.

4.4.4 Main C Code Description

4.4.4.1 Variable Initialization

In this block of code, variables used in this software were initialized by assigning constants to them. Variables that were initialized included:

- Voltage Probe Offset
- Current Probe Offset
- Voltage Sample
- Current Sample
- Voltage Sum
- Current Sum
- Voltage Averaged
- Current Averaged
- Voltage Reference
- Action Output by the Regulator
- Error of the Voltage Regulator
- Regulation Integrator
- Regulation Proportional
- Interrupt Counter

4.4.4.2 Initialization of the ADC

This block of the code initializes the analog to digital converter hardware of the TMS320 LF 2407 that performs the analog voltage sensing and converts it to the digital signal with a

sampling technique. During the process of initializing the ADC, the first step was to reset the ADC, then the ADCTRL1 was initialized in such a way that bit 6 was equal to zero to allow for a start-stop mode of the ADC. The MAXCONV was then initialized to determine the number of conversions which were to be performed by the ADC. The CHSELSEQ1 set the conversion on channels used. By initializing the ADCTRL2 the ADC sequencer was set and the ADC was enabled to be started by an event.

4.4.4.3 Initialization of GP Timer for PWM Generation

In this block of the code, parameters of the PWM waveforms were set. The period of the carrier was 20 KHz and the modulating signal was 50Hz. The first step was to set the General Purpose input output pin registers for primary functions, and then the General Purpose timer control register GPTCONA was set. In the following line of the code, the Timer 1 counter was reset as well as the Timer1 period which was set to generate the carrier signal frequency.

4.4.4.4 Sampling Period Interrupt Initialization

In this code, Timer 2 was used to set the modulating signal frequency. First the Timer 2 counter was cleared and the Timer 1 period loaded. Bits 10 and 9 of GPTCONA were set to 10 to start ADC upon Timer 2 period occurrence. Bit 6 = 1 enables Timer 1 compare output for PWM generation, bit 2, 1=10 sets output pin polarity high. T1CON was initialized so that it set the Timer 1 control register for bit 12,11 = 01 which corresponded to continuous up down count mode Bit 6 = 1 enables the Timer and bit 1=1 enables the compare operation. The Timer 2 control register was initialized for bits 12, 11=01 continuous up/down count mode and bit 6=1 which enables the timer. Next the interrupt upon Timer 2 period occurrence

was enabled. The interrupts flags were reset and appropriate interrupts enabled. The program was designed to run in an endless loop while waiting for an interrupt.

4.4.5 Interrupt Service Routing (ISR)

The algorithm was set to perform several tasks once an interrupt occurs. After the sensor voltage values are obtained the algorithm either returns to the main wait loop or branches to the regulation code. The interrupt used for this code was GPT1_underflow, which occurs at a rate of 10 kHz, which allows time for the Timer to reach its period of 1024. The timing of the ISR is done by a counter that counts up and down according to the switching frequency required. The timing of the counter is done by setting pre-scaler values that determine what the DSP's clock period is going to be multiplied by to achieve the required timing of the interrupt. First, a counter was set to count up to a set value and count back down to zero. The clock used by the DSP being 30 MHz crystal, the clock period was 25nS. The counter was set to count up to 1024 and down 1024 which effectively means that it has counted 1024 twice. Therefore, (1024 x 2x 25 nS) = 51µS which corresponds approximately to 20 KHz.

4.4.5.1 Reading Voltage Sensor

The first requirement when reading the sensors is to ensure that there is protection against negative values that may occur because of physical sensor drift. A negative value needs to be eliminated. The probe offset is determined manually when physically connecting the DSP to the converter. In this section a block of the code was designed to take ADC registers readings, to which offset were subtracted, so that the results are positive or zero. The results are then stored in the ADC which is 10 bits. This requires the results to be shifted to remove

the least significant bits. The voltage samples stored into the ADC were then formatted by multiplying them with a certain gain to accommodate the use of DSP.

4.4.5.2 Filtering the ADC Readings

This block of code was designed to accumulate the voltage samples from every interrupt in order to calculate their average once every PWM cycle.

4.4.5.3 The Regulation Code Sequences

The Inverter's output voltage readings are taken and stored once every period of the GPT1_underflow interrupt. If enough readings have been taken, the sum of all voltage samples is provided which is averaged and stored as an average load voltage, then an offset is deduced and the result filtered. This average load voltage is then compared to the reference voltage to produce an error. The error is sent and processed by a digital proportional controller which provides a control action signal. The signal must be transformed into a corresponding duty cycle. The transformation is done through the code. The process of obtaining this duty cycle is explained in the next section.

- **Output Action to PWM**

The action signal from P Controller ensures its dynamic performance through the process speed of the DSP. The actual relationship between the duty cycle and the voltage gain is dependent upon the load and converter characteristics and would, therefore, have to be identified for each specific application. The duty cycle effectively output by the PWM hardware as it is programmed is the following function:

$$d = \frac{TxPR - TxCMPR}{TxPR} \tag{4.1}$$

The code must adapt the action signal from P regulator (Action) into a value to be stored in the T1CMPR register. The equation used is:

$$\frac{Action}{TxPR} = \frac{TxPR - TxCMPR}{TxPR} \tag{4.2}$$

which yields the simple transformation implemented in the code sequence provided in Appendix J.

$$TxCMPR = TxPR - Action \tag{4.3}$$

The equation 4.3 above shows that the action signal was subtracted from the P Regulator. This resulted in a new value in the PWM Timer compare to be used by the PWM hardware for the next PWM cycle.

The next chapter presents the results obtained when investigating the effects of a DC current on 6 kVA power transformer; the prototype was built and tested in the laboratory. Readings of all measurement made on the prototype are provided.

Chapter 5

PRESENTATION AND DISCUSSION OF RESULTS

5.1 Simulations Results

5.1.1 Linear load connection

Figure 5.1 below, depicts the results of waveforms of current and voltage obtained when a pure resistor is connected to a 6 kVA power transformer and a pure AC current circulates in the secondary windings.

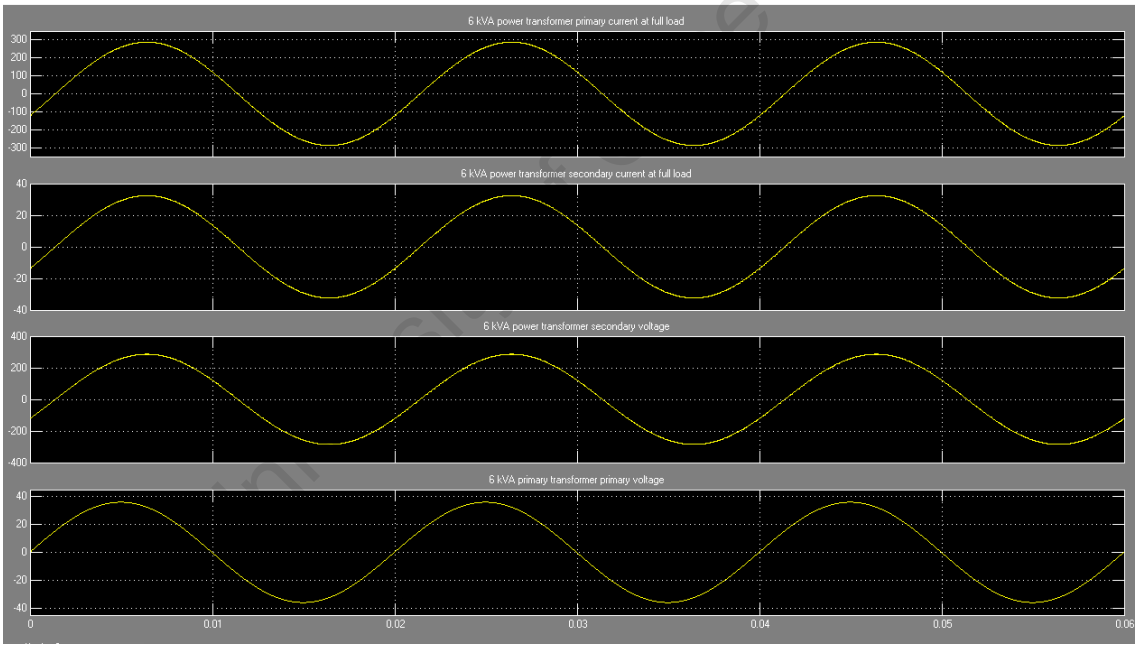


Figure 5.1: Simulated transformer's voltage and current waveforms when a linear load is connected

The waveforms in figure 5.1 show the results obtained in the scenario presented in figure 3.1. The top waveform depicts the transformer primary current (100A/division); the second waveform depicts the transformer's secondary current (20A/division); the third waveform

depicts the transformer's secondary voltage (200V/division) and the bottom waveform shows the transformer primary voltage (20V/division) when the transformer operates at full load (6 kVA).

It can be seen that the waveforms are purely symmetrical, which ensures that there is no DC offset resulting from the connected load. Figures 5.2 and 5.3 show the harmonic content in the secondary voltage and current waveforms. The waveforms are composed of the fundamental components only; this is due to the linearity in the connected loads. Figures 5.4 and 5.5 show the harmonic content of the primary voltage and current waveforms The results show that the waveforms are only composed of the fundamental at 50 Hz. The percentage total voltage and current harmonic distortion THD measured using the Matlab/Simulink THD block shows that there is no distortion.

Table 5.1 : Harmonic contents in the power transformer's secondary voltage under linear loads

Secondary voltage and current harmonic contents										
% rated load	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}	6^{th}	7^{th}	8^{th}	9^{th}	10^{th}
25%	100	0	0	0	0	0	0	0	0	0
50%	100	0	0	0	0	0	0	0	0	0
25%	100	0	0	0	0	0	0	0	0	0
100%	100	0	0	0	0	0	0	0	0	0

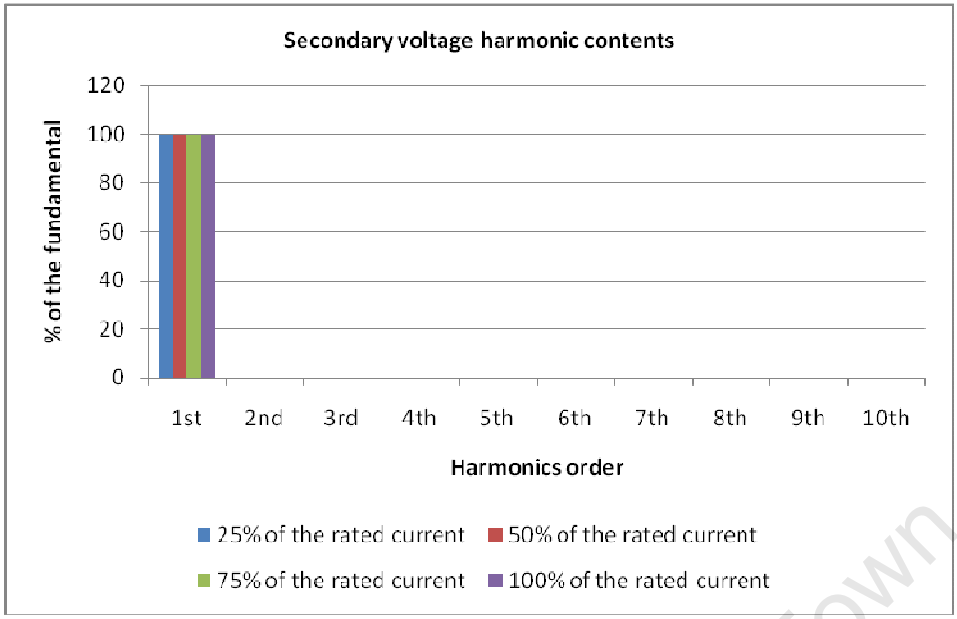


Figure 5.2: Transformer's secondary voltage harmonic contents

Table 5.2 : Harmonic Contents in the Power Transformer's Secondary Current under Linear Loads

Secondary current harmonic contents										
% rated load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
25%	100	0	0	0	0	0	0	0	0	0
50%	100	0	0	0	0	0	0	0	0	0
25%	100	0	0	0	0	0	0	0	0	0
100%	100	0	0	0	0	0	0	0	0	0

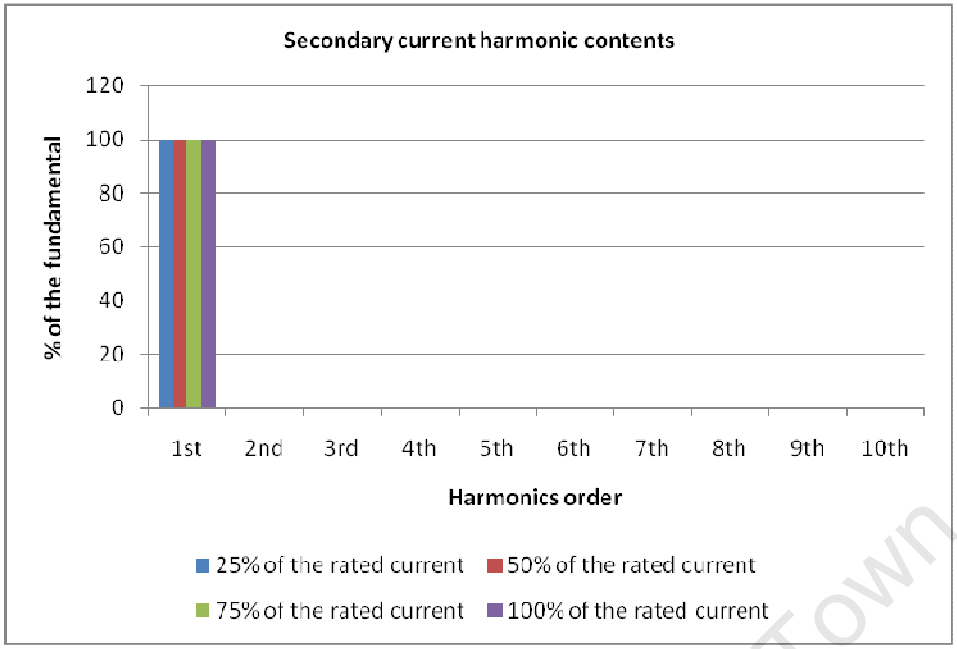


Figure 5.3: Load current harmonic contents

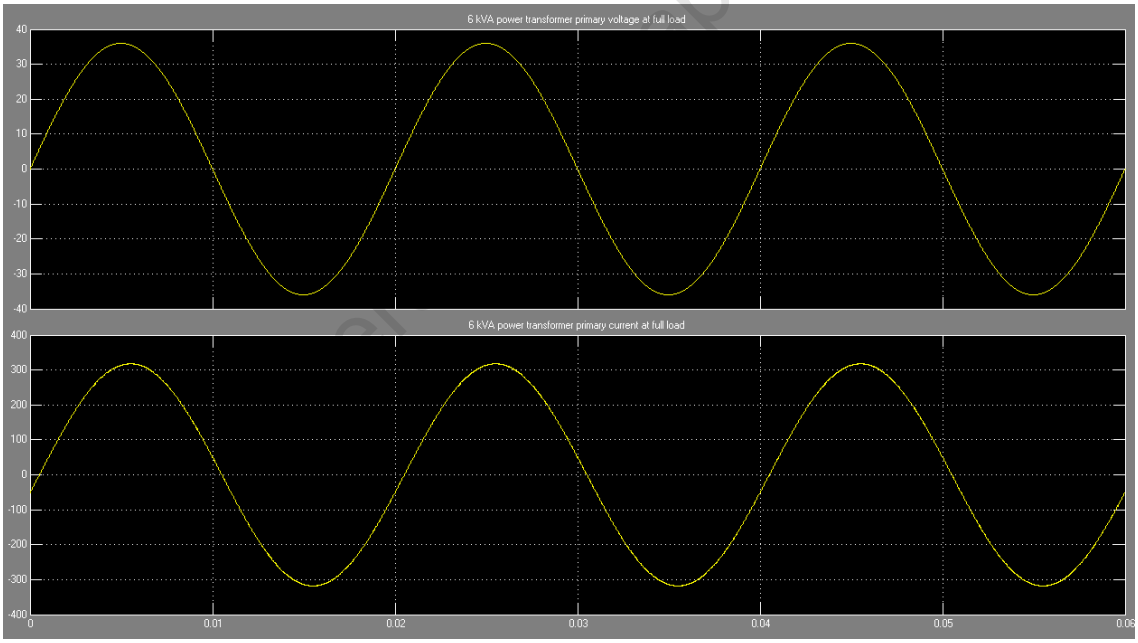


Figure 5.4: Simulated 6 kVA power transformer's primary side voltage and current waveforms under linear load

Figure 5.4 above depicts the source voltage (top) and current (bottom) waveforms. They are pure sinewave and this was proved by their low %THD and their crest factor which was in

the range defined for pure sinewave. The measurements were performed by using the Matlab THD blockset.

Table 5.3 : Harmonic contents in the power transformer's primary voltage under linear loads

Primary voltage harmonic contents										
% rated load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
25%	100	0	0	0	0	0	0	0	0	0
50%	100	0	0	0	0	0	0	0	0	0
25%	100	0	0	0	0	0	0	0	0	0
100%	100	0	0	0	0	0	0	0	0	0

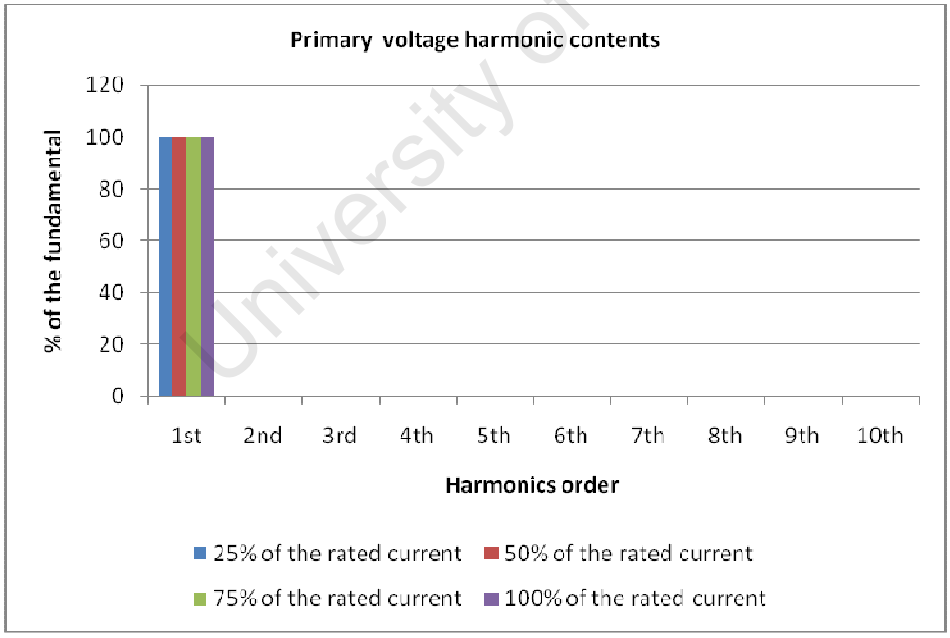


Figure 5.5: 6 kVA power transformer's primary voltage harmonic contents under linear loading

Table 5.4 : Harmonic contents in the power transformer's primary current under linear loads

Primary current harmonic contents										
% rated load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
25%	100	0	0	0	0	0	0	0	0	0
50%	100	0	0	0	0	0	0	0	0	0
25%	100	0	0	0	0	0	0	0	0	0
100%	100	0	0	0	0	0	0	0	0	0

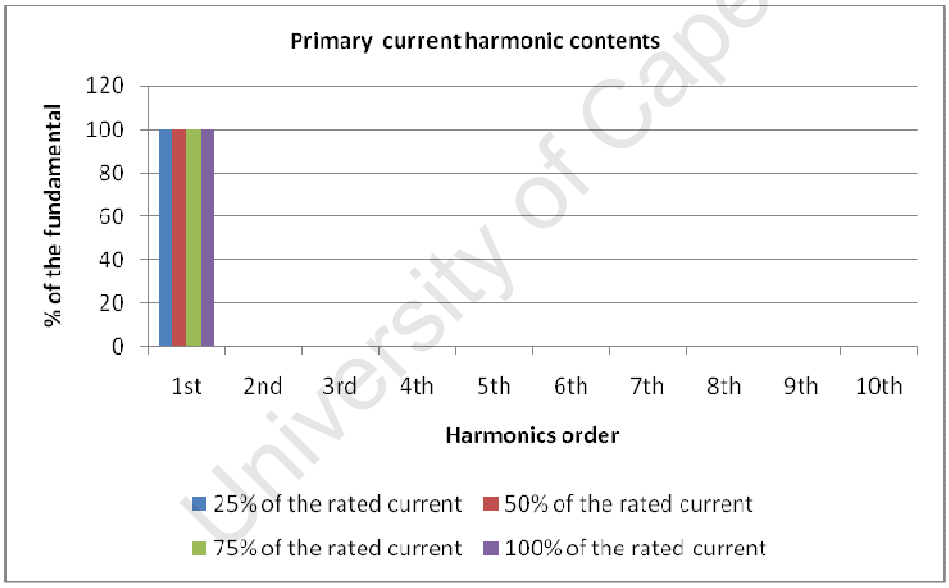


Figure 5.6: 6 kVA power transformer's primary current harmonic contents under linear loading

5.1.2 Non-linear Load Connection

In this section, the simulation results obtained during the investigation of the performance of a power transformer subjected to DC currents resulting from nonlinear load currents are

presented. The first step is to present the results obtained when using a half-wave rectifier load and thereafter a full wave rectifier having an inductor-capacitor filter and a resistor load is discussed. Simulation waveforms of the transformer's voltage and current are presented together with their harmonic contents.

5.1.2.1 Simulation Results with Nonlinear Loads (Asymmetrical Loads)

For the simulation where a non-linear load drawing asymmetrical currents is connected to the secondary windings of the power transformer , resulting waveforms are shown in figure 5.7 below. Figure 5.8 depicts the individual harmonics that compose the power transformer's primary current. Figure 5.9 shows the secondary voltage and current waveforms measured at different points of the secondary windings, while Figure 5.10 shows the secondary current harmonic contents. More details are discussed in the following section.

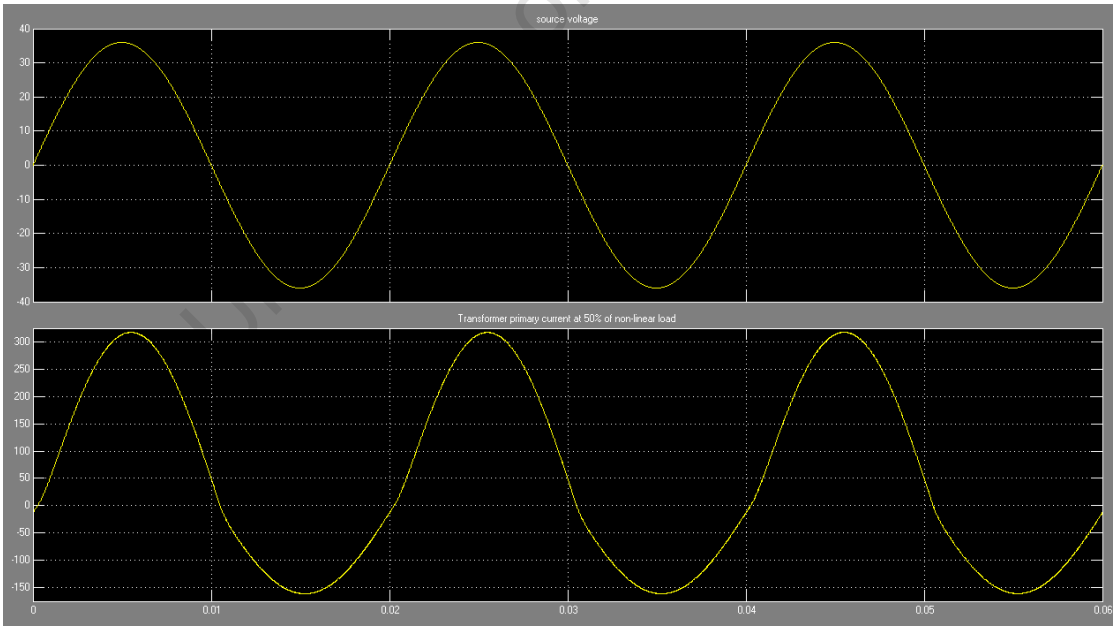


Figure 5.7: Simulated transformer's primary voltage and current waveform when combining a 50% linear load with a 50% non linear load

The results depicting the effects of DC current on the primary current and voltage are shown in figure 5.7 above. The top waveform represents the transformer's primary voltage and the bottom waveform represents the current in the primary windings. The first step carried out in this investigation was to connect an asymmetrical load whose rating current was at 50% of the power transformer's rated current. As expected, the measured value of the DC component of the primary current remained zero irrespective of the DC current circulating in the transformer's secondary windings. As shown in figure 5.4, when the DC current in the secondary windings is zero, the duration of the positive and negative half cycles are both ten milliseconds (50Hz) . However, when a diode supplies a rectified current in the secondary windings, the duration of the negative half cycle is reduced and the peak of the negative half wave increases. Since no DC current is transferred to the primary, the area encompassed by the positive and negative half cycle of the magnetising current waveform must be equal. Hence, the negative cycle peak increases to compensate for the reduction in the duration of the negative cycle.

Table 5.5: Results obtained during the assessment of transformer's primary current harmonic contents under asymmetrical load

Transformer primary current harmonic contents under asymmetrical loading										
% of asymmetrical load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
0%	100	0	0	0	0	0	0	0	0	0
25%	100	62.3	0	34.4	0	23	0	13.11	0	13.1
50%	100	21.6	8	46.6	6	31	5	21.6	3	13
25%	100	81	12.2	53.4	13.8	39.6	12	25.8	10.3	13.2
100%	100	86.2	15.8	59.6	15.8	45.6	14	31.6	12.2	12.5

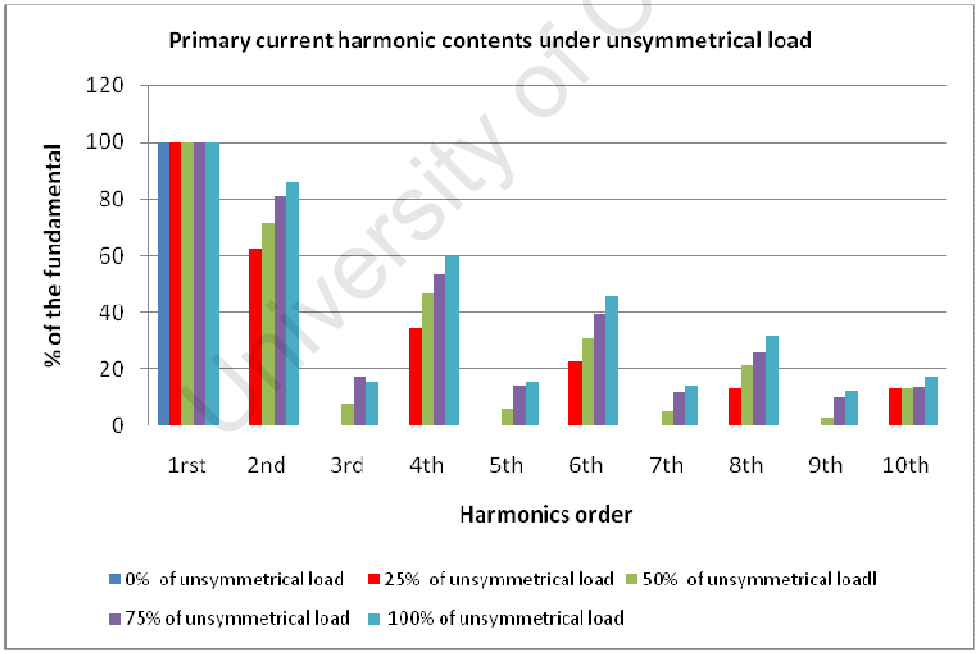


Figure 5.8: Harmonic contents in the power transformer's primary current when an asymmetrical load is connected to its secondary windings

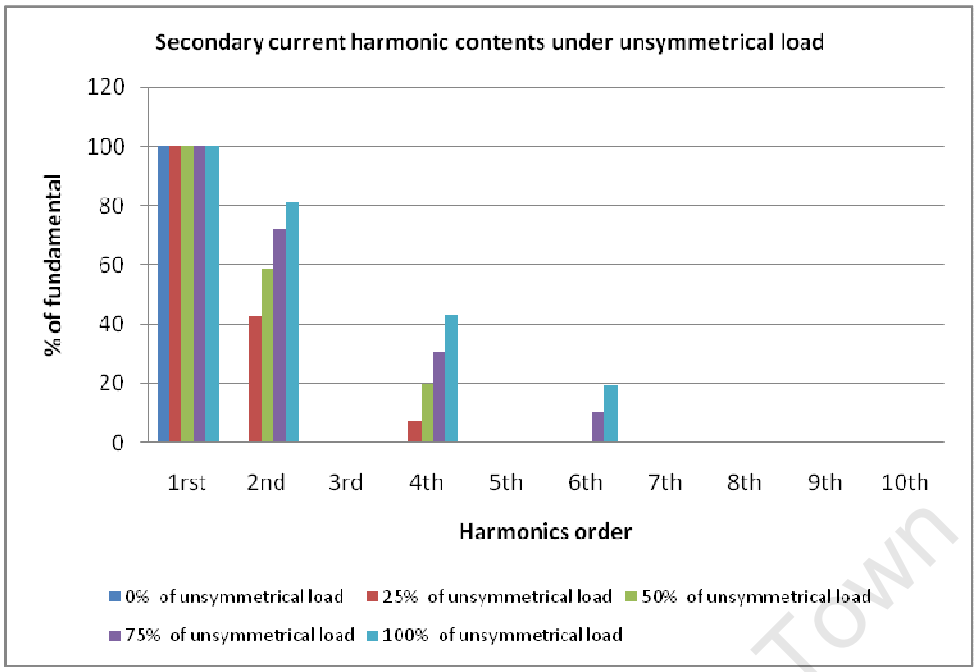


Figure 5.9: Harmonic contents in the power transformer's secondary current when an asymmetrical load is connected to its secondary windings

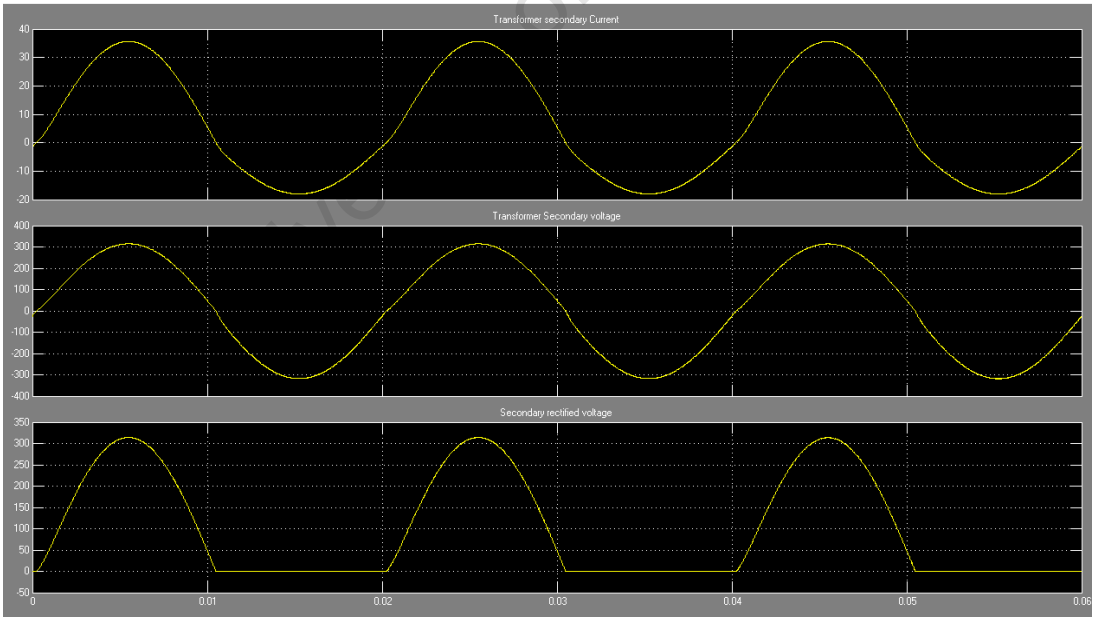


Figure 5.10: Simulated transformer's secondary voltages and current waveform when combining a 50% linear load with a 50% non-linear load

When an asymmetrical load, represented by a half-wave rectifier, is connected on the transformer's secondary windings, the secondary voltage and current are rectified resulting in a signal which consists of both DC current and AC current superimposed. In the case where the rectifier load contributes a 100% to the rated load current, the resulting signals are half-wave rectified as shown in figure 5.11 below. This proves that the load is drawing asymmetrical currents from the power source. On the other hand, when the asymmetrical load represents only a percentage of the rated current together with a linear load which draws pure AC from the power source, the secondary voltage and current waveforms represented in figure 5.11 show some DC offset which results in harmonics. This distortion is transferred to the primary side by the secondary component.

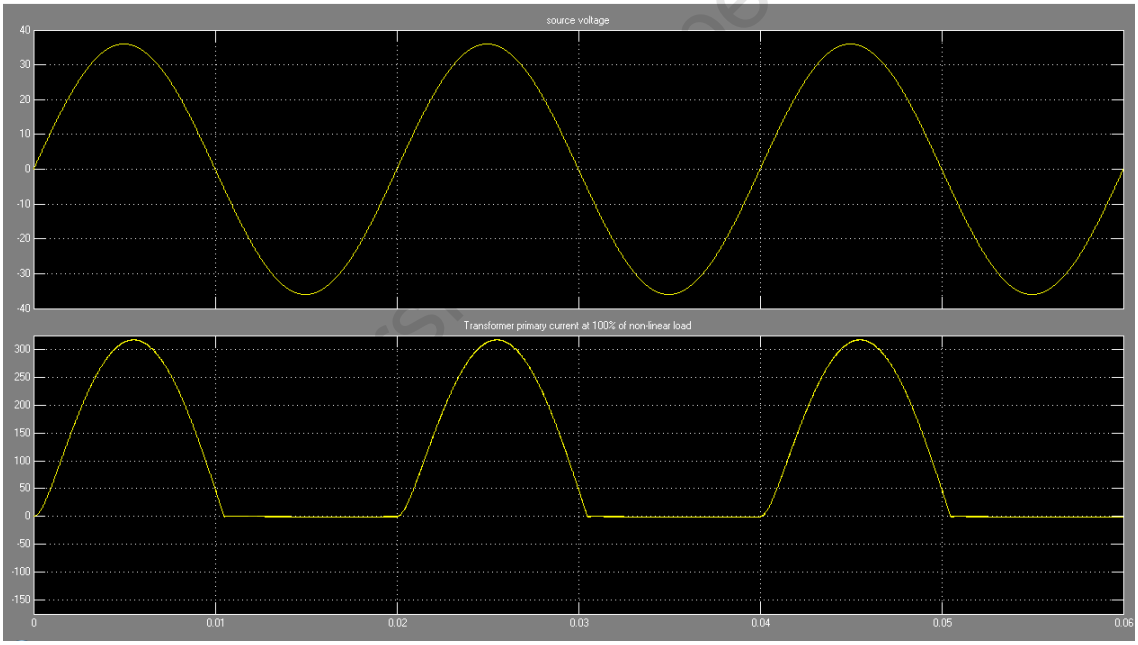


Figure 5.11: Simulated transformer's primary voltage and current waveform when combining a 0% linear load with a 100% non linear load

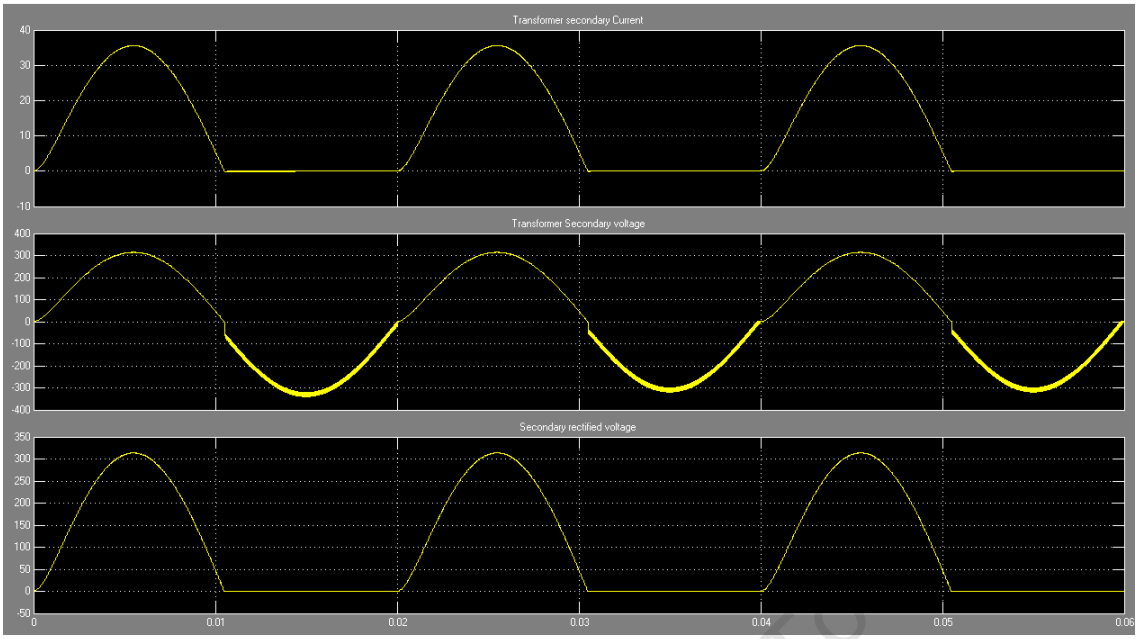


Figure 5.12: Simulated transformer's secondary voltage and current waveforms a 100% non-linear (asymmetrical) load is connected to the secondary windings

After the investigation of the effects of the asymmetrical loads on a 6 kVA power transformer, simulation results have been presented to show that asymmetrical loads introduce a high level of distortion in the power transformer's currents. The transformer being the most expensive element in any power system, poor power quality of the devices being fed can damage the power transformer due to the distorted current drawn by the appliance which consequently leads to costly operation of the system. It is, therefore, advisable to control the quality of the currents drawn by inserting filters or compensators which prevent the injection of distorted power back into the power network, or more specifically which prevent DC current from being injected into the power transformers. In the next section, non-linear loads represented by a full-bridge rectifier connected on the secondary windings of a power transformer fed from the AC supply voltage are investigated. The resulting currents waveforms will be investigated and the level of distortion discussed.

5.1.2.2 Simulation Results when Non-Linear Loads (Full Wave Rectifier) are Connected to the Transformer

Voltage and current waveforms obtained during the simulation of the performanvce of a 6 kVA power transformer when a full brigde rectifier is connected to its secondary windings are presented in the figure 5.13 below:

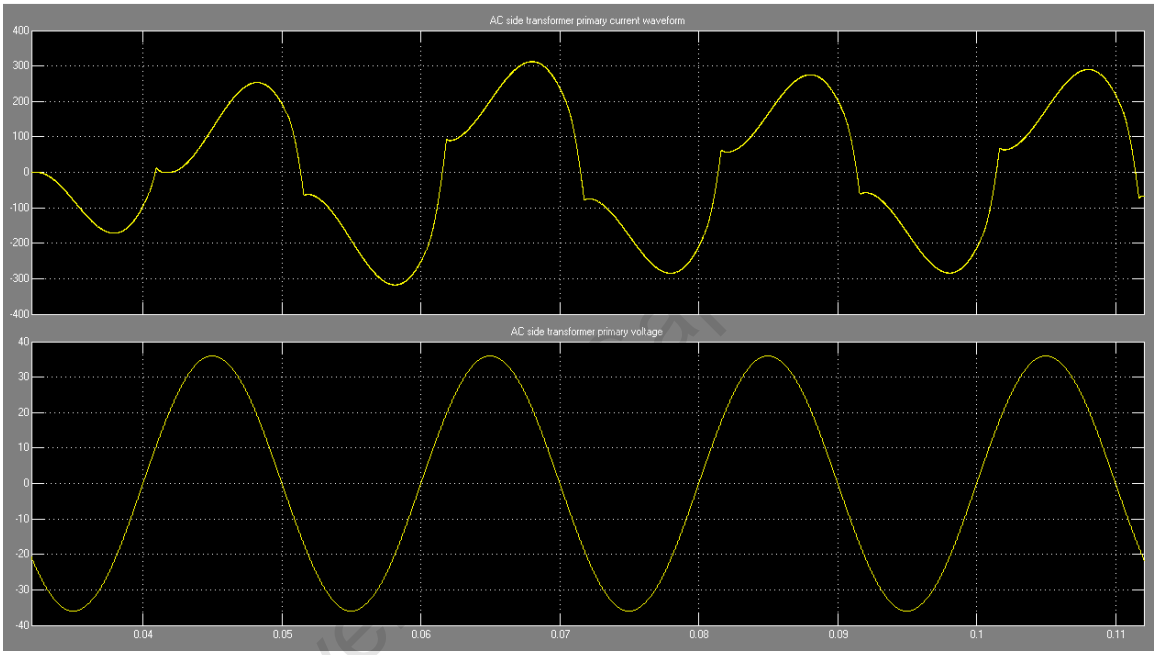


Figure 5.13: Simulated power transformer's primary voltage and current waveforms when the load consists of non-linear load (full bridge rectifier)

Figure 5.13 above depicts the power transformer's primary current when a full bridge rectifier is connected on its secondary windings. The waveform looks distorted despite the fact that it is showing symmetry. This result is typical of current drawn by the full brigde rectifier having an inductor, a capacitor filter and a resistor load connected to its output [44]. A linear load was further connected to the power transformer's secondary winding in parallel with the full bridge. This linear load represents the case where the non-linear load is only

drawing a certain percentage of the transformer rated current. Investigation of the level of distortion in the transformer's primary current was carried out.

Table 5.6: Results obtained during the assessment of transformer primary current harmonic contents under non-linear symmetrical load

Transformer's primary current harmonic contents under non-linear symmetrical loading										
% of non linear load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
0%	100	0	0	0	0	0	0	0	0	0
25%	100	0	62.2	0	48.3	0	35.5	0	30.6	0
50%	100	0	62.2	0	54.8	0	42	0	22.6	0
25%	100	0	22.1	0	59	0	49	0	44.2	0
100%	100	0	25.4	0	64	0	55.2	0	49.2	0

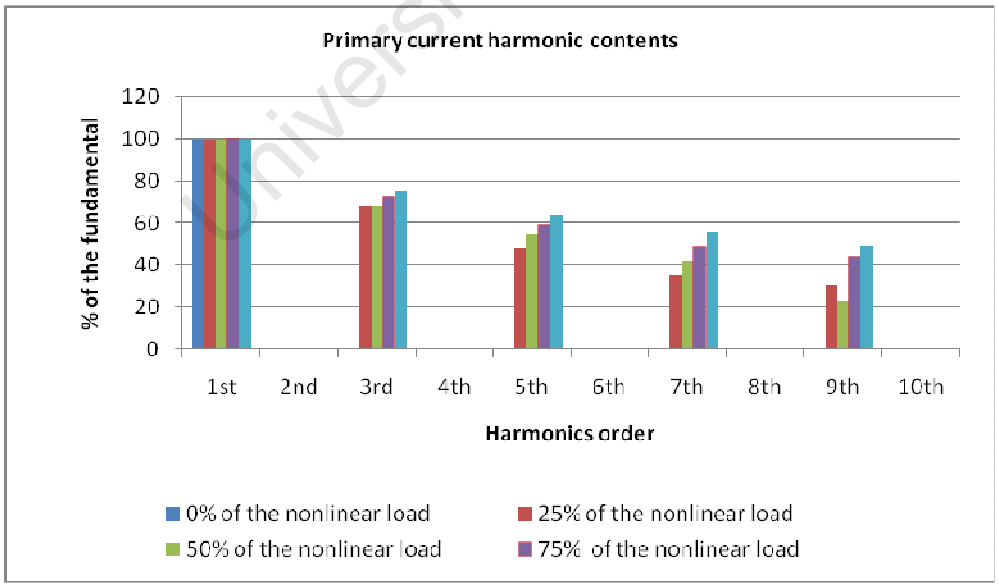


Figure 5.14: Power transformer's primary current harmonic contents under non-linear load

Table 5.7: Results obtained during the assessment of transformer's secondary current harmonic contents under non-linear symmetrical load

Transformer's secondary current harmonic contents under non-linear symmetrical loading										
% of non linear load	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
0%	100	0	0	0	0	0	0	0	0	0
25%	100	0	55.8	0	22.9	0	9	0	0	0
50%	100	0	58	0	34.8	0	18.6	0	0	0
25%	100	0	61.9	0	40.5	0	28.6	0	16.6	0
100%	100	0	64.3	0	42.6	0	35.2	0	28.6	0

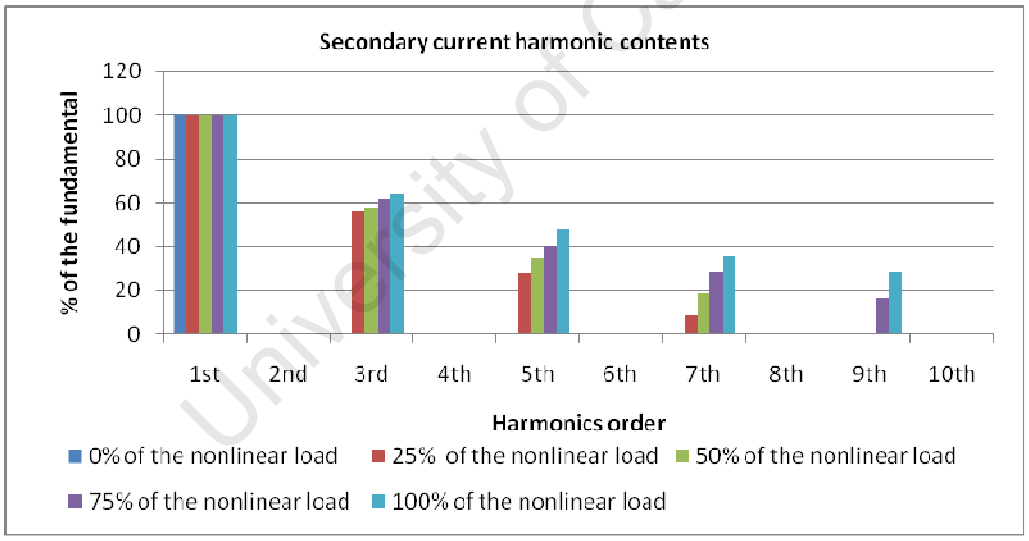


Figure 5.15:Power transformer's secondary current harmonic contents under non-linear load

Figure 5.14 depicts the power transformer's primary current harmonic contents. The result shows that the waveform consists of odd orders of harmonics only. When the non-linear load is at a percentage of zero, the primary current waveform consists of only the fundamental.

Other odd orders of harmonic arise with the increase in the percentage of non-linear load. Figure 5.15 shows that the secondary current waveform also has odd order of harmonics when a non-linear load is connected to the transformer secondary windings. The secondary also shows no harmonics except the fundamental when the percentage of non-linear current drawn from the source is zero, then it starts showing some distortion once the level of non-linear load connected is increased. The harmonics generated by non-linear loads are very high in magnitude when compared to the fundamental and this could result in low transformer efficiency since the power transferred from the primary to the secondary is only dependent on the fundamental component of the voltage and the current.

Later in the thesis, an experimental work carried out to determine the effects that a DC current can have on a 6 kVA inverter power transformer is presented; the analysis of the power transformer's voltage and current waveforms is also provided. Finally, a study carried out to investigate methods of mitigation of a DC current effect on power transformer is presented.

5.1.3 Simulation of a Single Phase Voltage Controlled Voltage Source Inverter (VCVSIs)

This section of the chapter presents the results obtained during the simulation in MATLAB of a single phase inverter system. First, the results obtained using an m-files as well as those when the inverter is simulated using SIMULINK are presented**.**

5.1.3.1 Results when Using M-files

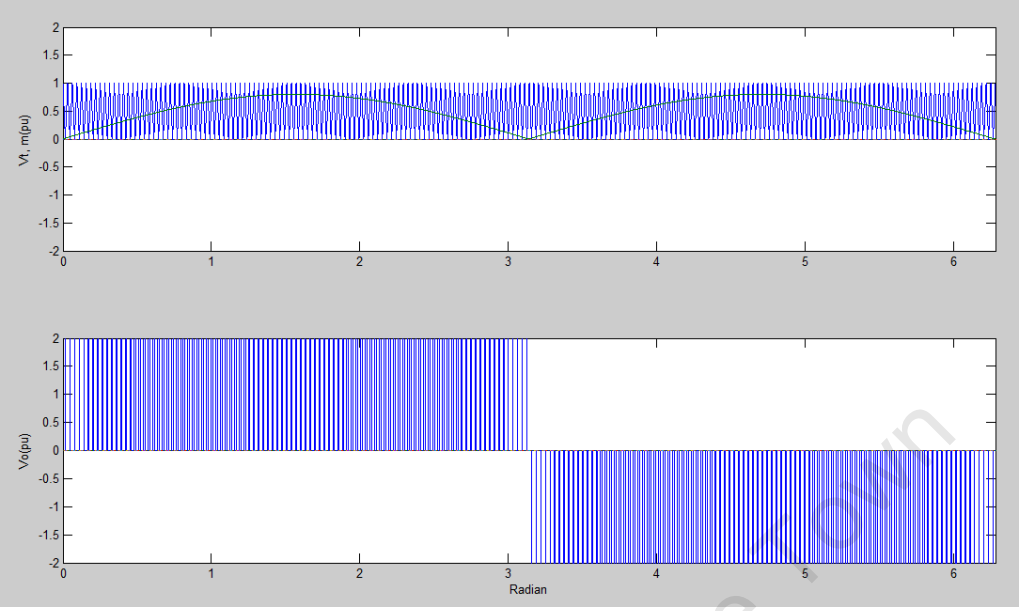


Figure 5.16: Simulated inverter switching pattern (top) inverter output voltage (bottom)

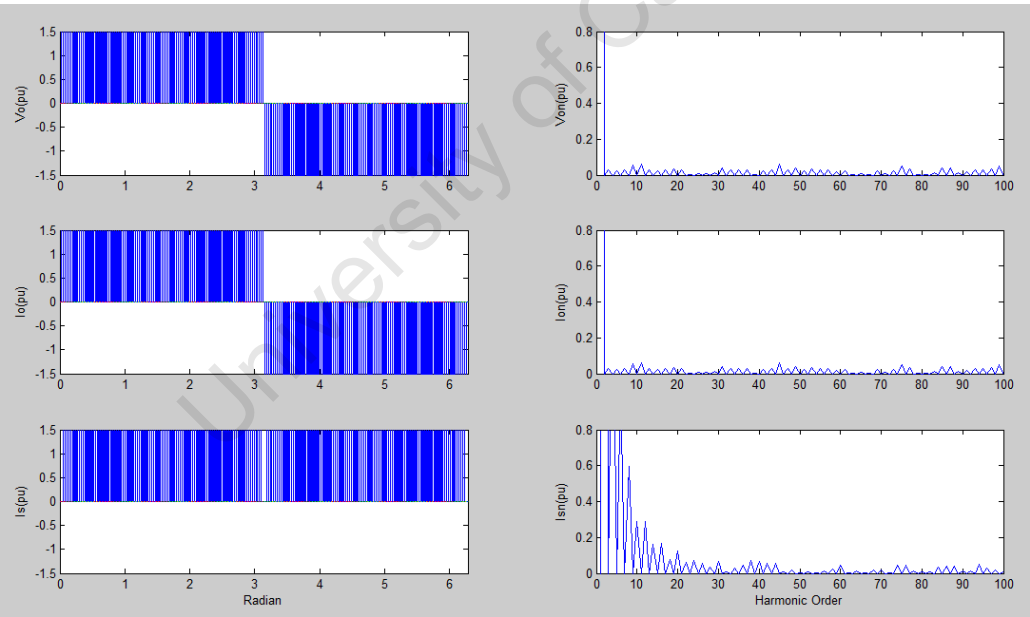


Figure 5.17: Inverter's output voltage, output current, input current, as well as the harmonic contents

Figure 5.16 (top) depicts the triangular waveform which is compared to a sinusoidal modulating signal. The patterns produced are used to switch the inverter's switching devices on and off and the output is shown in Figure 5.17 (bottom) above. The output is called PWM output. The output is not yet a sinusoidal signal and it has to pass through a filter in order to obtain a desired signal that will look like the reference signal. Figure 5.17 depicts the inverter's output voltage and current waveforms. The voltage waveform was discussed above and the current varies linearly with the voltage since the load connected is a simple resistor. With the results obtained above, the total harmonic distortion (THD) of the inverter's output voltage can be calculated using the formula shown below:

$$THD_V = \frac{V_{rms} - V_1}{V_1} \tag{5.1}$$

where V_{rms} is the rms value of the inverter output voltage and V_1 is the rms value of the Inverter's output voltage fundamental component. The calculated %THD is 77%.

This shows that the inverter's output waveform is not sinusoidal and contains harmonic components. These components may be reduced using different switching techniques and their effects diminished by a filter. Any non sinusoidal alternating waveform can be shown as an infinite number of sinusoidal functions with related harmonics using Fourier series. It is, therefore, clear that the main component has the fundamental and the frequencies of the remaining harmonic components are multiple of the fundamental frequency. The period of the resultant waveform is always equal to the period of the base waveform. The voltage waveform of the real inverter is non sinusoidal and, having the orders and amplitudes of its harmonic components, can be very helpful in the design and selection of proper switching techniques. The elimination of the switching frequencies is discussed in Section 5.1.3.3 below.

5.1.3.2 Results when Using SIMULINK

Figure 5.18 below depicts the results obtained when an inverter system is simulated in MATLAB/SIMULINK using the diagram showed in figure 3.4. The resulting waveform was captured at the inverter output by the use of SIMULINK scope.

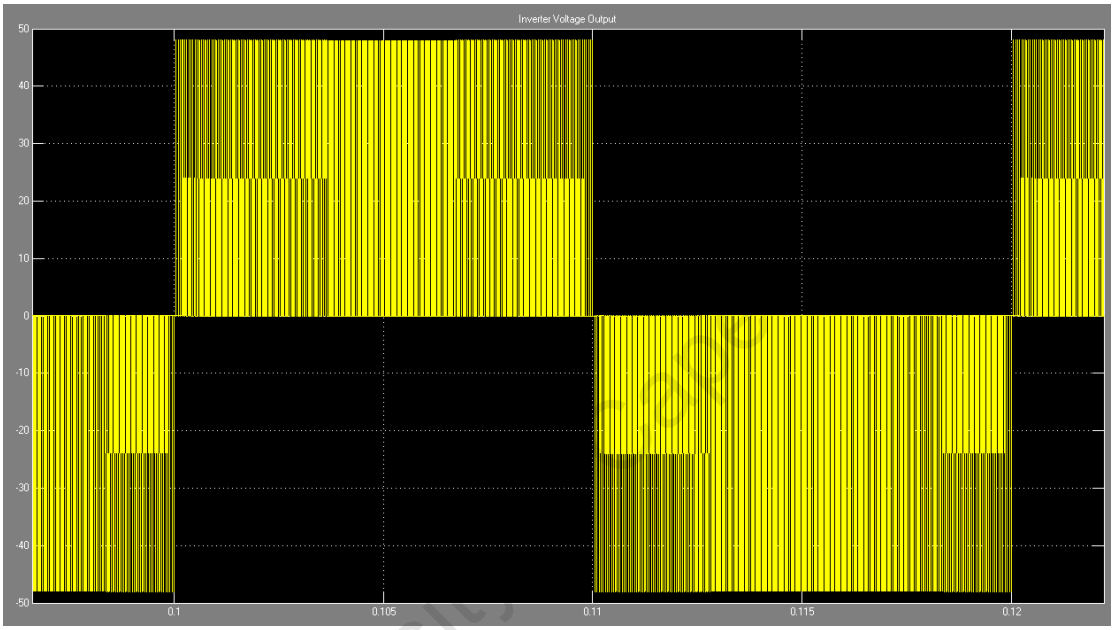


Figure 5.18: Simulated inverter's output voltage without filter (simulation results using Simulink/Matlab)

Comparing results in Figures 5.17 and 5.18, it can be concluded that the Matlab m-file and Matlab/Simulink model have given the same results.

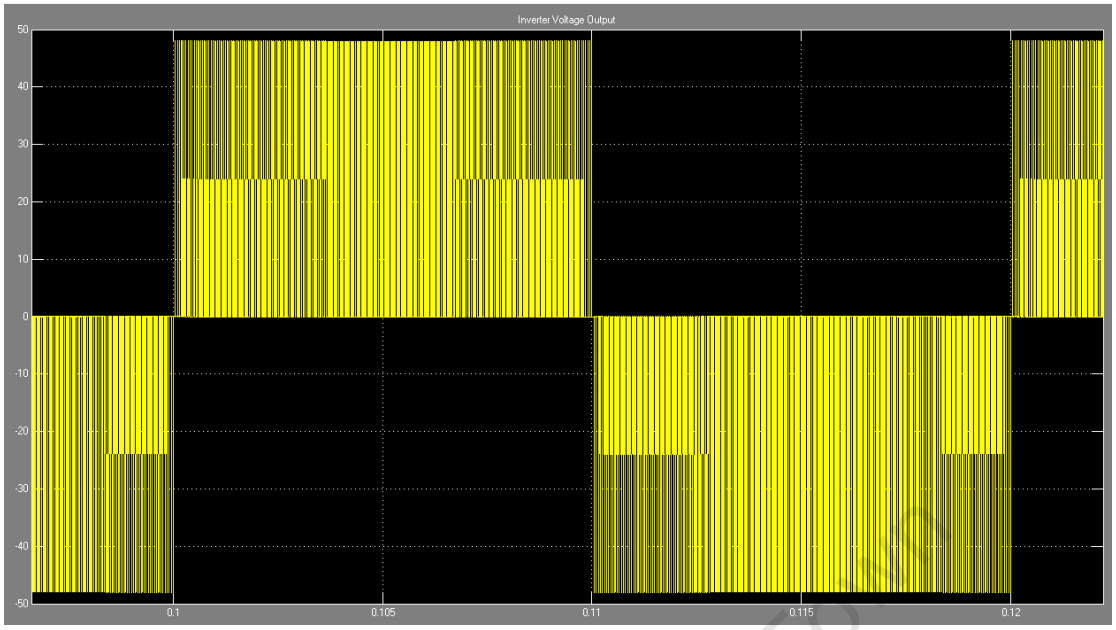
5.1.3.3 Elimination of Switching Frequencies

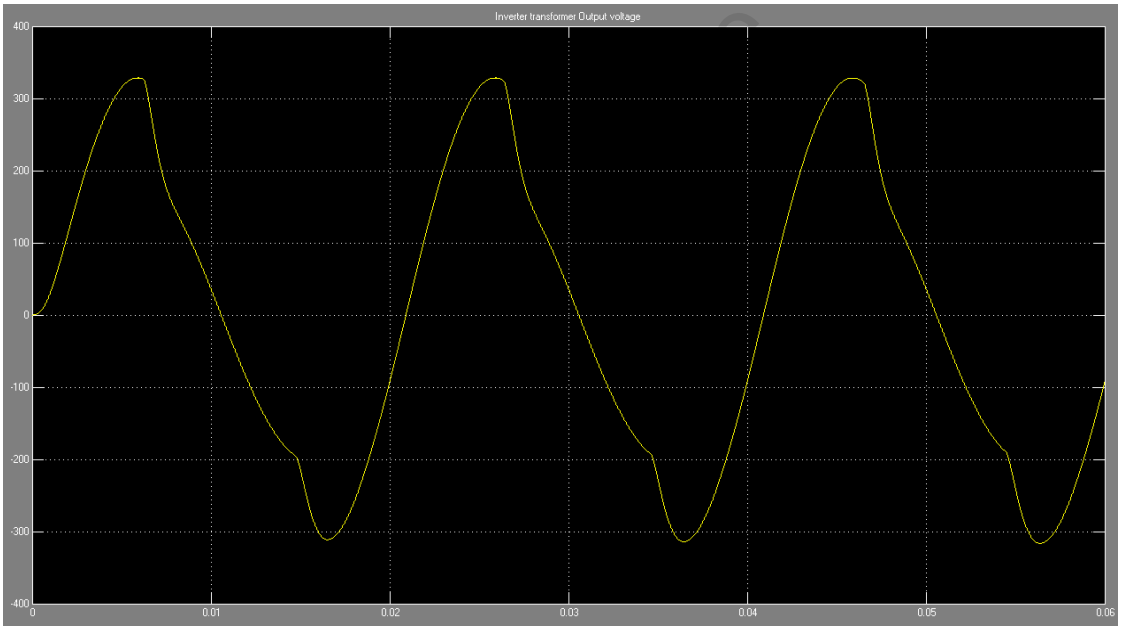
In the inverter's systems there are three groups of frequencies with amplitude large enough to be of concern to manufacturers and users of the distributed generators. These groups include

low frequency harmonics which are the multiples of the fundamental frequency (50Hz), switching frequency harmonics and high frequency harmonics.

By properly designing a control system feedback for the inverter, low frequency voltage harmonics can be mitigated. The presence of stray capacitance and stray inductance in the current control circuits gives rise to high frequency current harmonics (in the hundred of KHz to MHz). This will not be of concern since a sine PWM control scheme was used to produce patterns which operated the inverter switches. But in the systems where these frequencies are of concern they can be reduced by using a radio frequency interference (RFI) filter.

Harmonics also exist around the switching frequencies of the inverter. These are in the kHz range as has been noticed during the simulation. This gives rise to potential waveform distortion and the risk of harmonic resonance that could lead to the destruction of some of the system elements. Because of the danger presented by these harmonics, there is a need to filter them out in order to have a properly operating inverter system. In this section, an AC filter is presented which eliminates all the high frequency components in the inverter output voltage, leaving the signal only with a component at 50 Hz.


Inverter Voltage Output
50
40
30
20
10
0
-10
-20
-30
-40
-50
0.1
0.105
0.11
0.115
0.12


Inverter transformer Output voltage
400
300
200
100
0
-100
-200
-300
-400
0
0.01
0.02
0.03
0.04
0.05
0.06

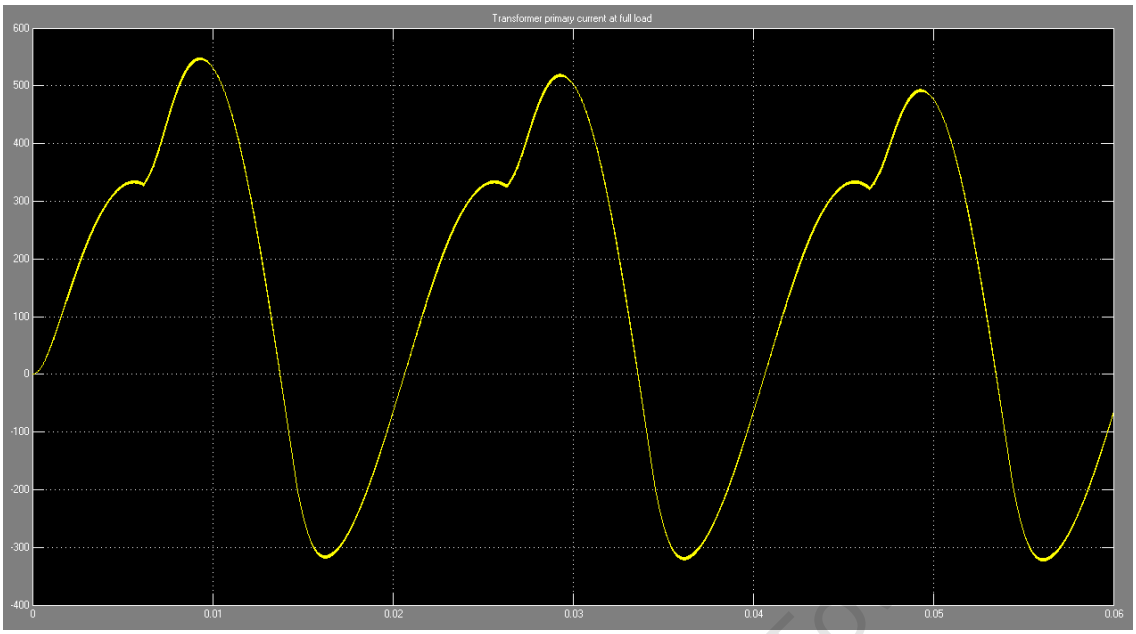


Figure 5.19: Simulated inverter output voltage and current waveforms with AC filter and resistor load (first is the PWM output, second is the transformer's voltage, and third is the transformer's primary current)

The purpose of this simulation exercise was to determine the effectiveness of the AC filter. This process was also necessary to establish the level of distortion after an AC filter was added. Figure 5.19 depicts the transformer's output voltage and current waveforms when a filter was added. The waveforms show a small distortion although the amplitude and the period of the waveform are correct. The investigation, using fast Fourier transform (FFT) to determine the harmonic contents of the waveform, has shown that the waveform consists of the fundamental, the second, third, fourth, fifth and sixth harmonics. The transformer's primary current shown in Figure 5.19 also shows the same FFT bar. The investigations concentrated on the elimination of the lower order of harmonics since the high order of harmonics were filtered by the inductor. As a result, the output of the inverter was different from the desired output. The difference between the output voltage and the desired reference signal is called an error and a voltage regulation must take place to reduce or eliminate that

difference (error) between the two signals. Section 5.1.3.4 below explains, in detail, the process of regulating the output voltage so that the difference between the output voltage and the desired reference can be reduced or eliminated. Further results obtained during simulation of inverter system with a voltage regulator will also be presented.

5.1.3.4 Inverter's Voltage Regulator

In this section, a simulation conducted to investigate the response of an inverter's system when a regulator is used to correct the error between its voltage output and the desired voltage output is presented. The system consists of a closed loop control system made by interconnecting components of the inverter system in a configuration that provides a desired system response. In this control system, the output voltage of the inverter system is compared with a desired voltage output. The error is then fed to the controller which varies the control signal according to the error signal so that the difference between the actual system output value and the desired output system value is minimized. In this work, only the results showing the level of distortion in the inverter's output voltage is detailed. Figure 5.20 below depicts the inverter's output voltage when a proportional P controller is used for regulation.

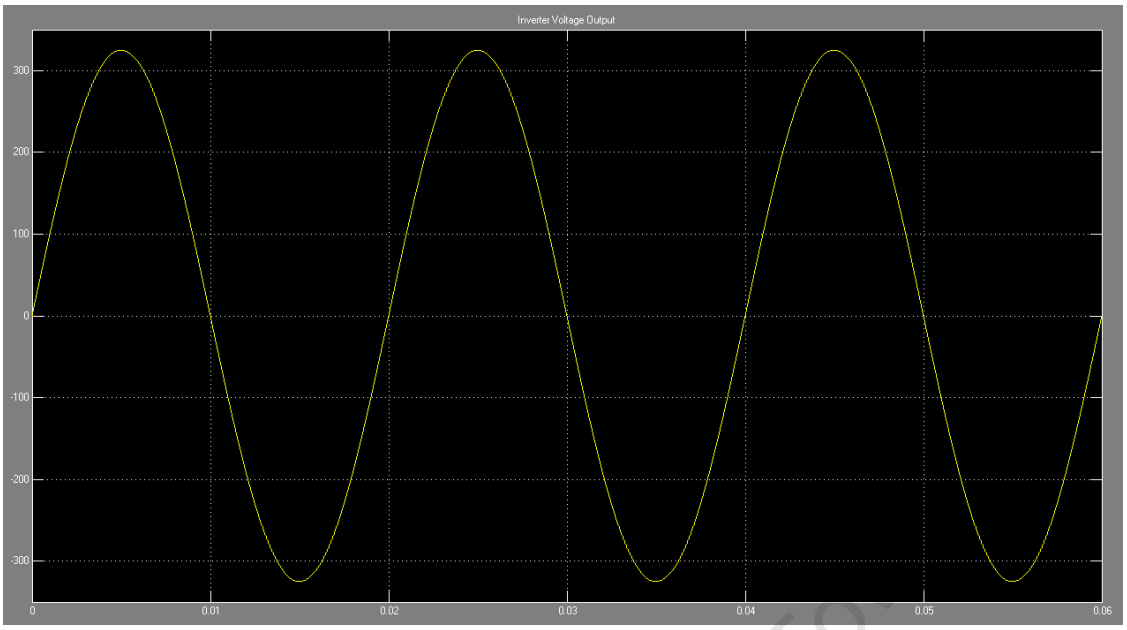


Figure 5.20: Simulated inverter's output voltage waveform when a P controller for voltage regulation is used

In Figure 5.20 above, the inverter's regulated output voltage looks like the desired perfect sine wave. Its percentage THD is very low, in the order of some units per cent, and its crest factor is 1.41. This is a proof that a proper voltage regulation was achieved. The measurements of the percentage THD and the crest factor CF were calculated using a Matlab/Simulink block set. The crest factor was measured indirectly as a ratio between the peak values of the inverter's output voltage waveform over the rms value of the same waveform.

5.1.3.5 Remarks

In the section above, the results of a simulation using a single phase inverter system which has a LC filter and a power transformer at the output and a proportional P voltage regulator were presented. The simulation's results will be validated by experimental results which will

be presented later in this chapter. The inverter's voltage regulator did not show all the controller specification which include:

- The steady state error settling time which was not in the scope of this work.
- Percentage overshoot: obviously using a P controller, some percentage overshoot should occur but since this did not destabilize the system it was not of much concern in the simulation.
- Oscillation frequency
- Percentage ripple

All these specifications were out of the scope of this work. Still the system worked sufficiently well.

5.2 Laboratory Work

5.2.1 Investigation of the Performance of the Power Transformer under Various DC Current Injections

5.2.1.1 Magnetizing Characteristics under Sinusoidal Supply Voltage and Effects of DC Current Injection on Magnetizing Characteristics

The results were obtained on the 6 kVA power transformer under AC current magnetization as well as by imposing a varying amount of DC current into the secondary of the power transformer are presented in the figures below:

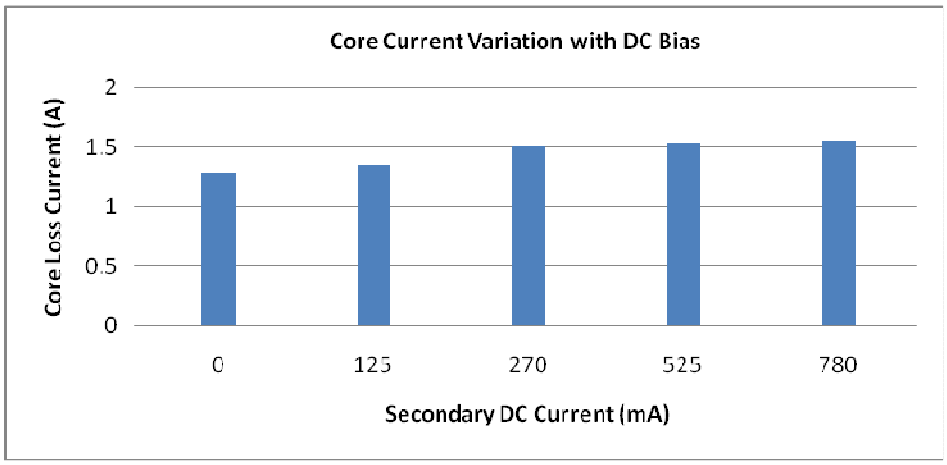


Figure 5.21: Core current variation with DC bias

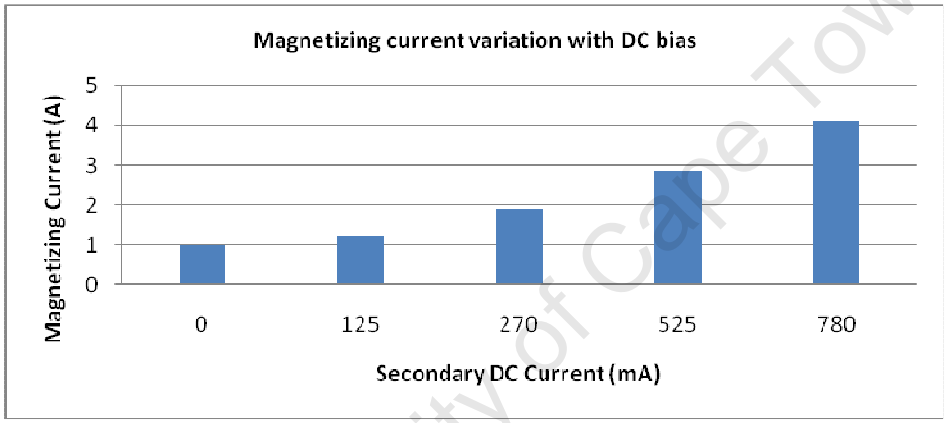


Figure 5.22: Magnetizing current variation with DC bias

Figure 5.21 illustrates the effect that DC bias has on the core current of a power transformer. Since the core current in a power transformer is frequency dependent, it is evident that the core current will not vary much since the frequency was kept constant during the tests.

By observing the graph shown in Figures 5.22, it is evident that the magnetizing current increased considerably with the increase in the DC current injected. This explains the basic theory which states that the transformer enters half cycle saturation due to DC bias since the excess flux in the secondary winding is not cancelled by any corresponding component in the

primary winding. Thus, the transformer has to increase its own magnetizing current to keep the flux stable.

The variation in the magnetizing current causes an increase in the power transformer's reactive power, since it is directly dependent. The increase in the reactive power results in an increase in the apparent power drawn from the primary source.

The real (active) power depends on the core material. The current in the core being constant, the real power does not vary to a large degree. Figures 5.23, 5.24 and 5.25 show the variation in apparent power and reactive power with DC bias.

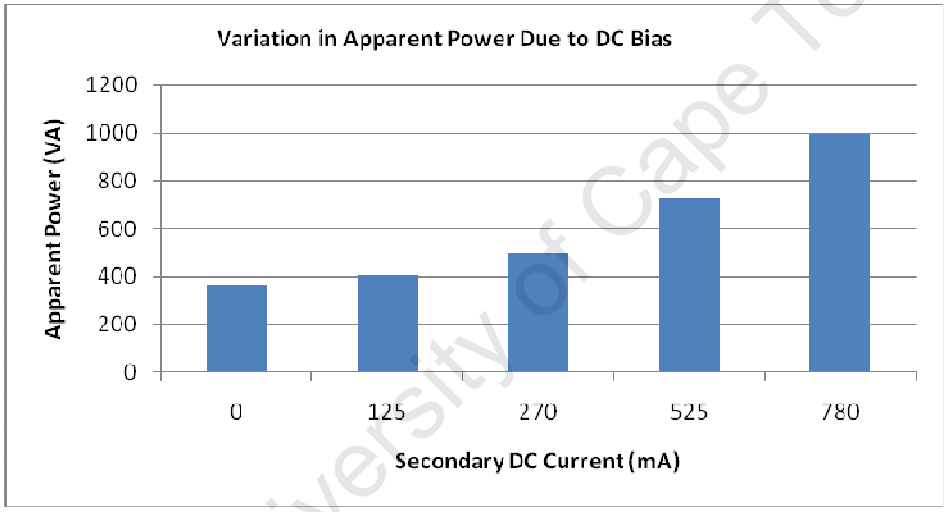


Figure 5.23: Variation in apparent power of a transformer due to DC bias

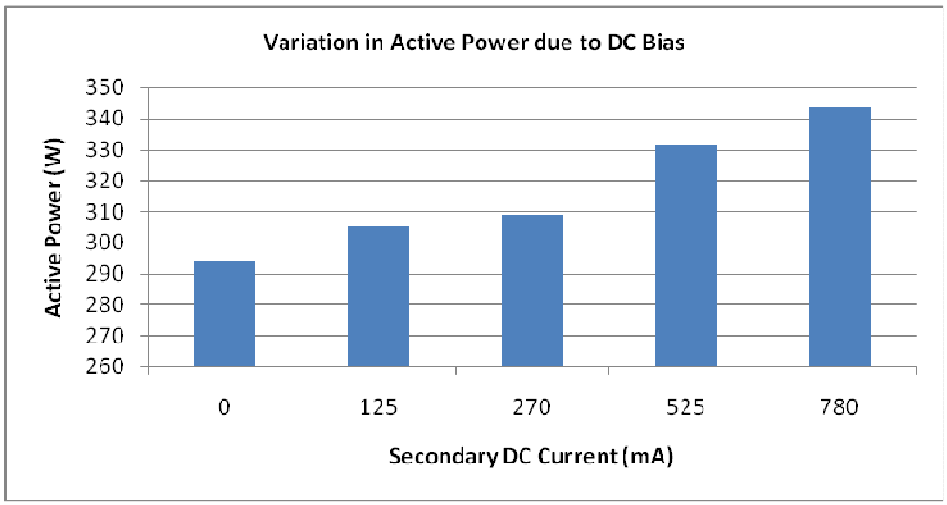


Figure 5.24: Variation in active power in a transformer due to DC bias

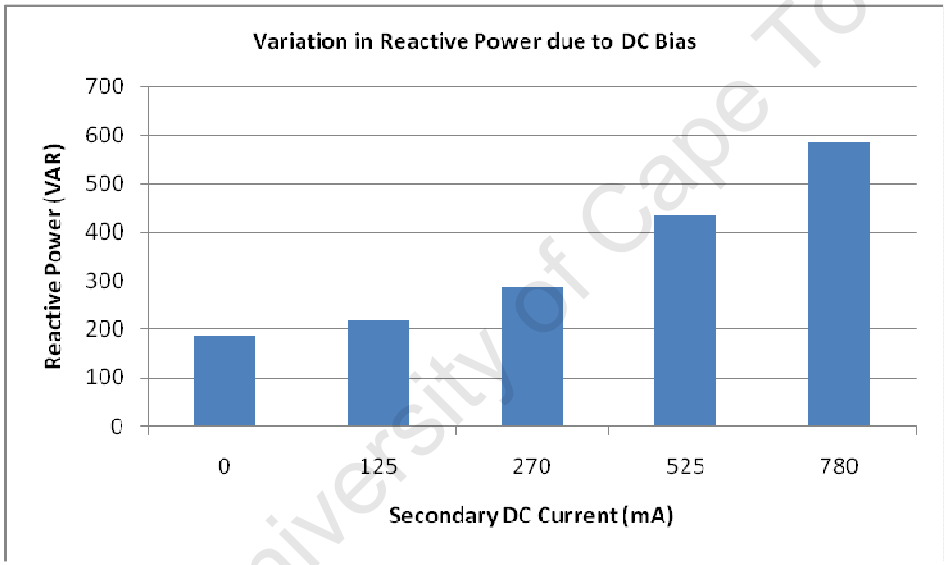


Figure 5.25: Variation in reactive power due to DC bias

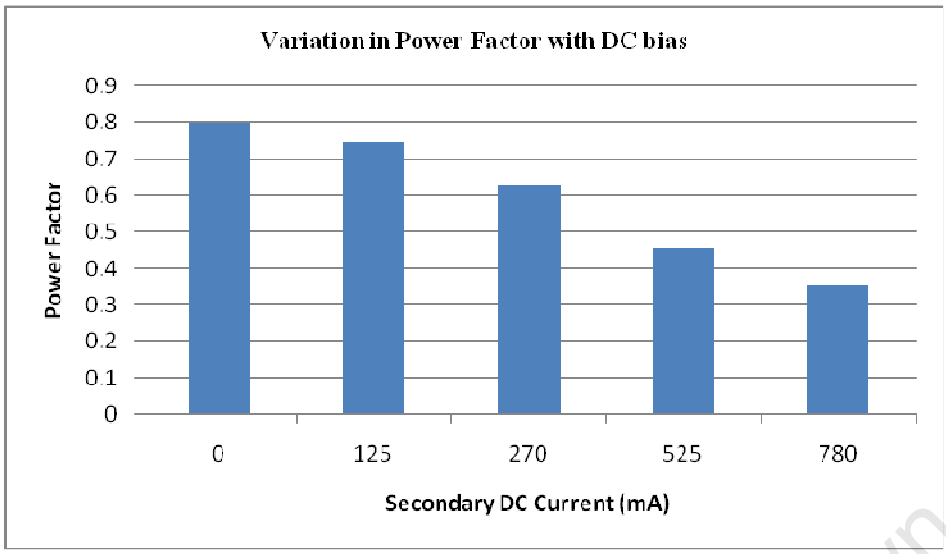


Figure 5.26: Power factor variation with DC bias.

Figure 5.26 shows the relationship between the power factor and the increase in injected DC current. The power factor decrease can be accounted for by the increase in distortion and asymmetry of the primary current.

5.2.1.2 Evaluation of the Magnetizing Current Distortion Resulting from DC offset

Asymmetry and distortion in the power transformer magnetizing current

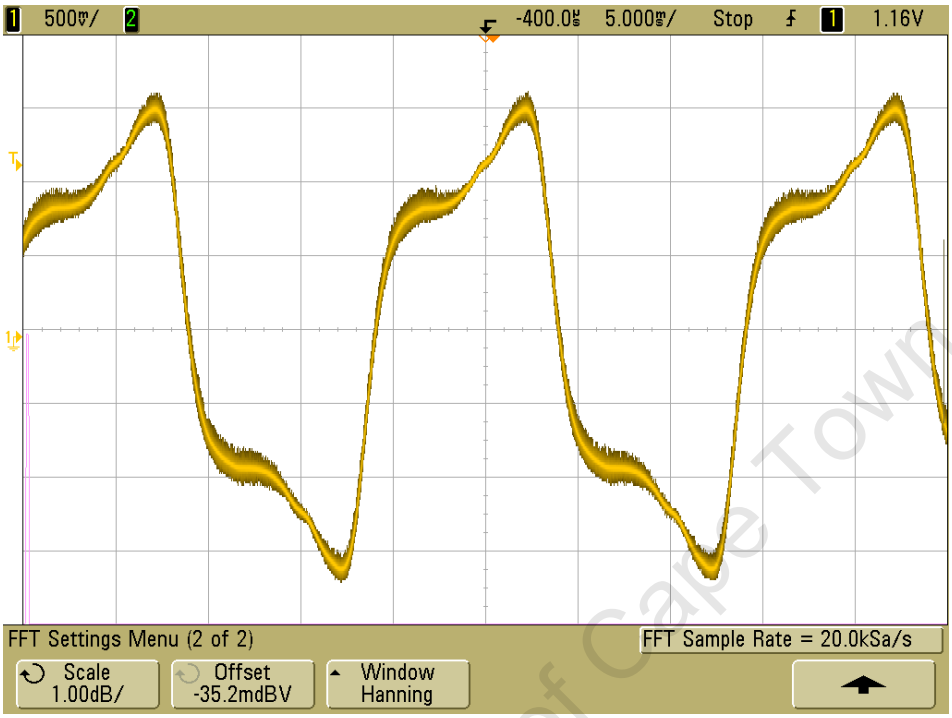


Figure 5.27: Measured magnetizing current of a 6 kVA power transformer on no load and with no DC current injection

It can be seen that the magnetizing current is symmetrical around the x-axis, which means that the mean value of the current is zero, that is, no DC current component.

That situation changes once a DC current is injected into the secondary windings. The waveform, which is not sinusoidal but symmetrical, becomes increasingly distorted and has an increasing average value (figure 5.28), as the DC current injected increases.

Figures below show different waveforms according to different DC current injected values for two main situations:

- When only a DC current circulates in the transformer's secondary windings.

- When DC current and AC current are superimposed on the transformer's secondary windings.

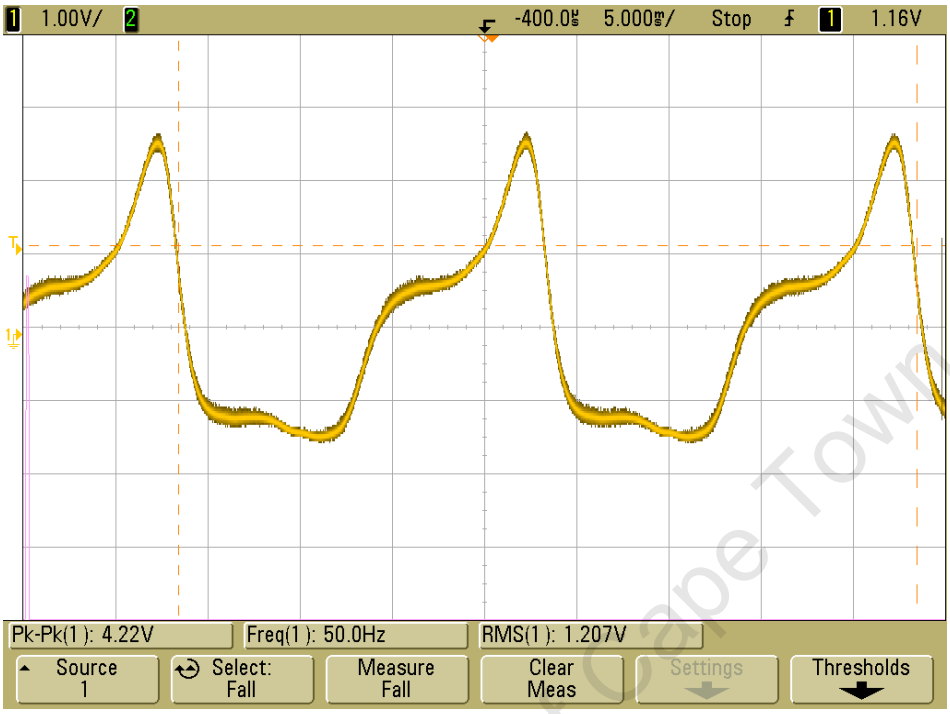


Figure 5.28: Measured magnetizing current waveform with 100mA DC injection

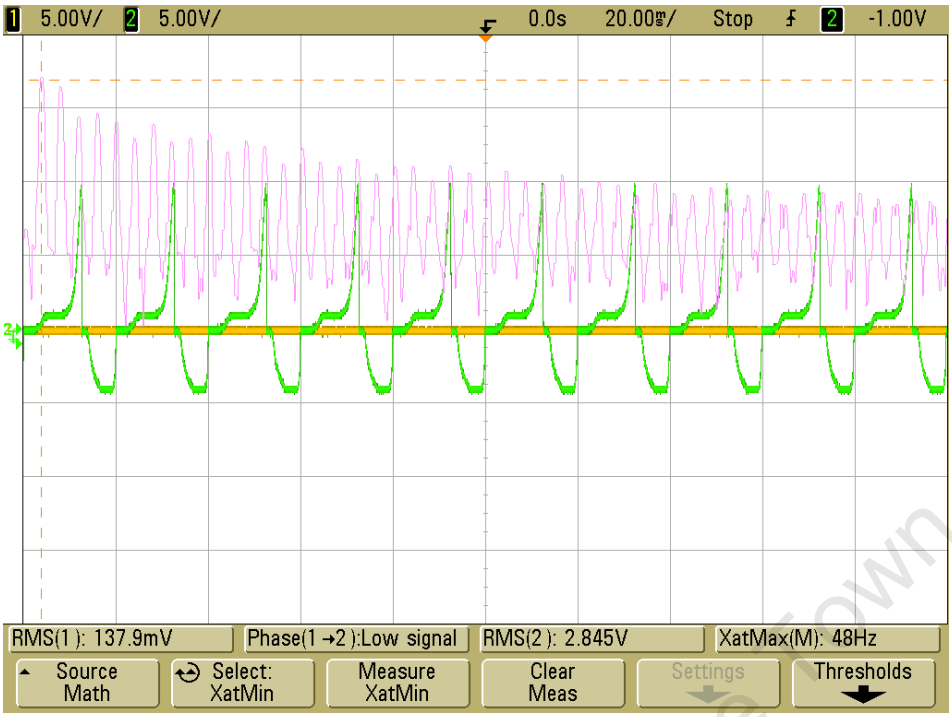


Figure 5.29: Measured magnetizing current waveform when a rectifier is connected to the secondary windings.

5.2.1.3 SHIFT in the Operating Point on the Core Steel Characteristic (B-H) Curve, of the 6 kVA power transformer

While the hysteresis models are usually in terms of field variables, such as magnetic flux density (B) and magnetic field intensity (H), experimental data are usually in terms of circuit variables, such as voltages (v) and currents (i). In this experiment, circuit variables were measured from a sample toroidal core.

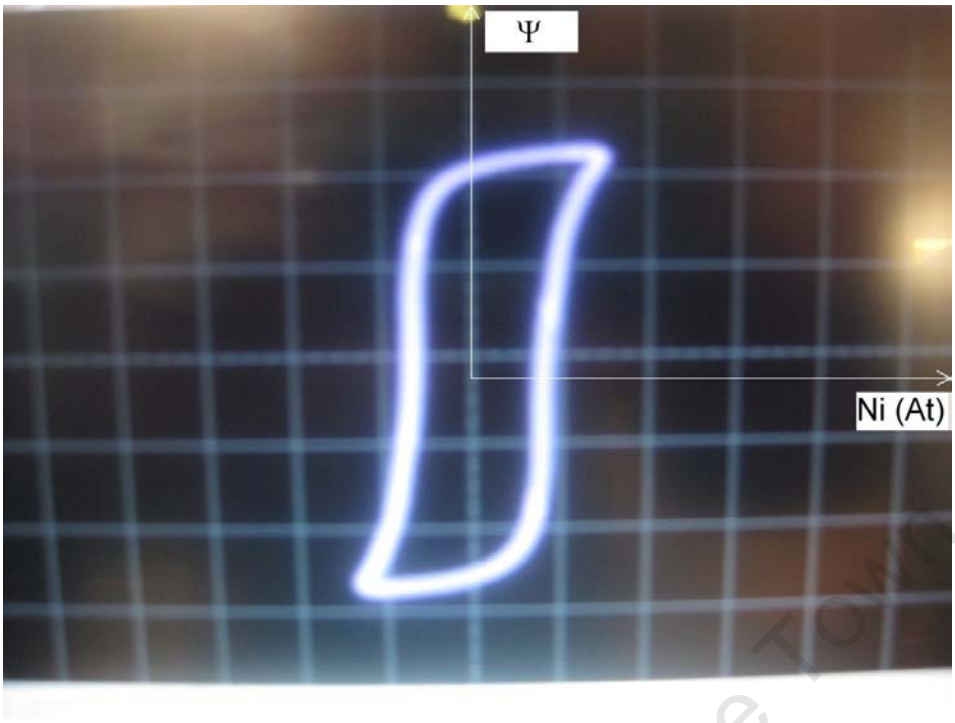


Figure 5.30: Hysteresis loop of a 6kVA (230/25) V power transformer operating at nominal voltage

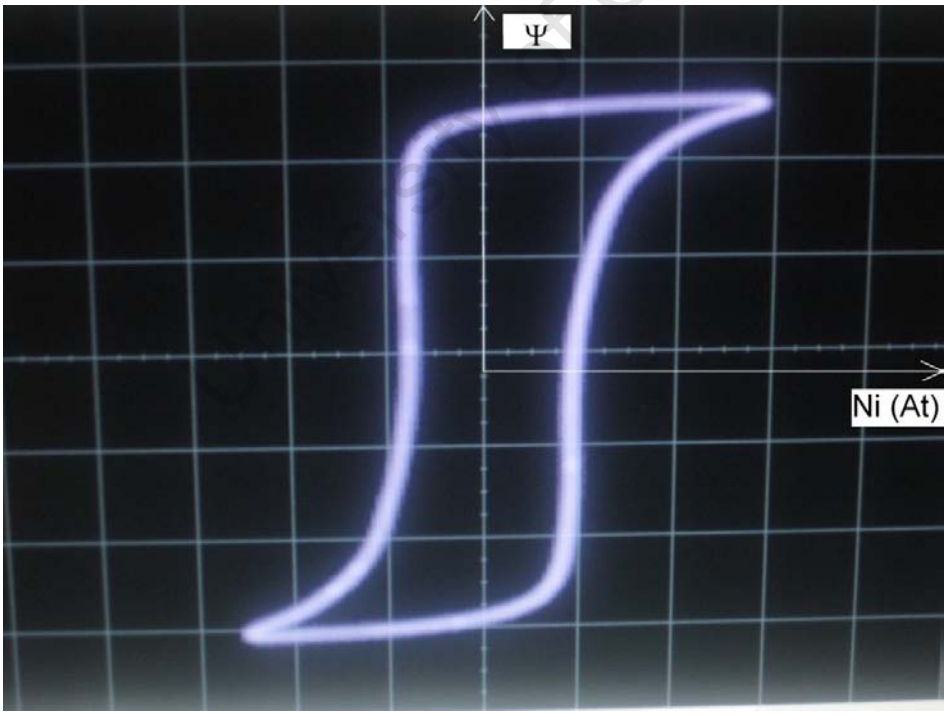


Figure 5.31: Hysteresis loop of a 6 kVA, (230/25) V power transformer operating at 17.4% overvoltage

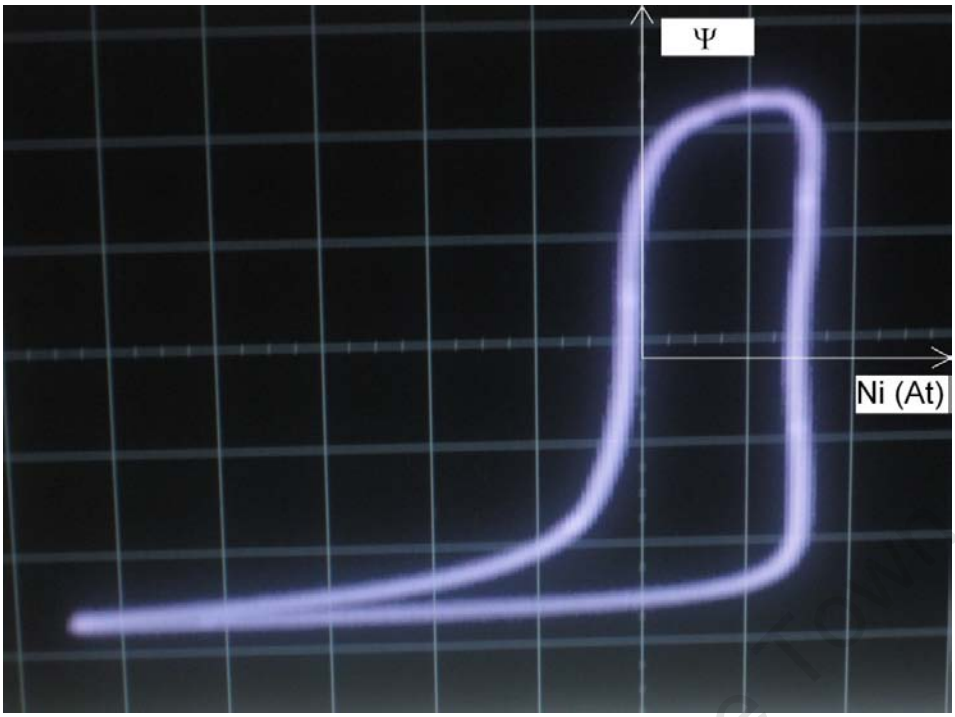


Figure 5.32: Hysteresis loop of a 6 kVA power transformer operating at nominal voltage and subjected to a 540mA positive DC current Injection

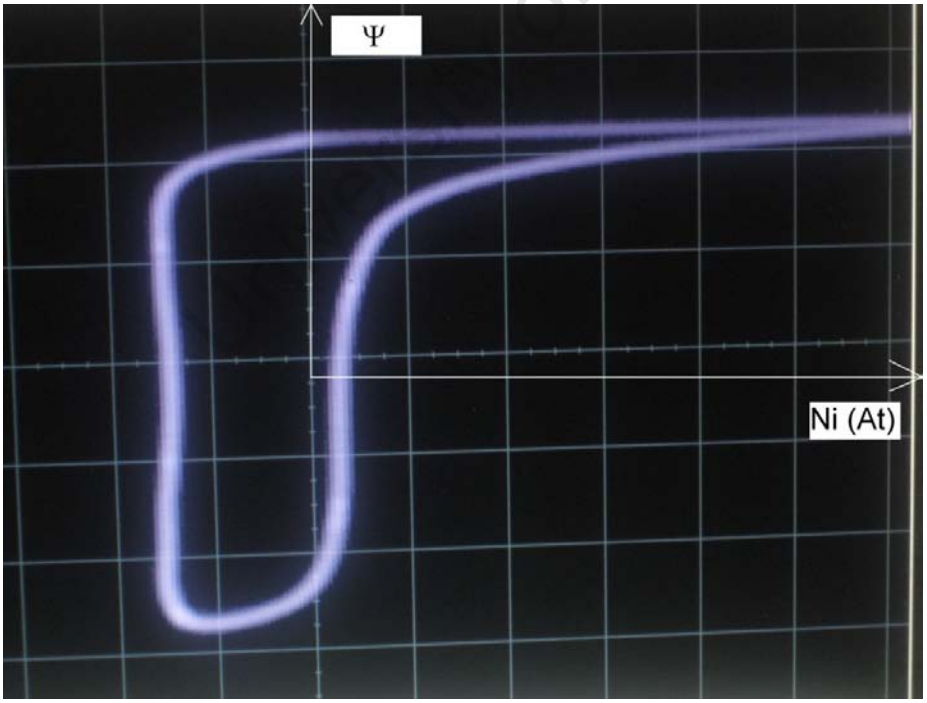


Figure 5.33: Hysteresis loop of a 6kVA power transformer with a negative DC current injection

With the voltage fixed at its nominal value (230V primary), a varying constant DC voltage supply resulted in a DC current in the secondary windings through a variable resistor. Plots of the resulting hysteresis loops were then captured (see figures above).

The hysteresis at nominal voltage was necessary to provide an indication of the transformer's performance when operating under normal conditions compared with the situation where a DC is injected which results in the core flux being biased.

It has to be noted, however, that these plots are not a complete representation of hysteresis characteristic exhibited by the core when DC current is injected in the secondary.

The integrator works out the flux by means of measurements of the integral of the supply voltage. The integral measures only the AC flux and is unable to provide the DC flux.

The interesting findings from these measurements of hysteresis are that:

Although the integrator of induced voltage from an open circuit third winding is unable to provide the true representation of biased flux, the resulting flux shown in figure 5.22 displays a large increase in the peak value for the negative half cycle of the magnetizing current.

5.2.1.4 Harmonic Contents in the Magnetizing Current of a Transformer under Different DC Current Injection

The aim of this section is to analyze the level of primary current harmonics distortion created in a single phase transformer when exposed to a DC current. The level of distortion will be compared to relevant standards. The harmonic spectrum will be investigated to determine which harmonic orders dominate and why. The results obtained during the tests performed to

determine the harmonic contents on the primary side current of a 6 kVA power transformer are presented below:

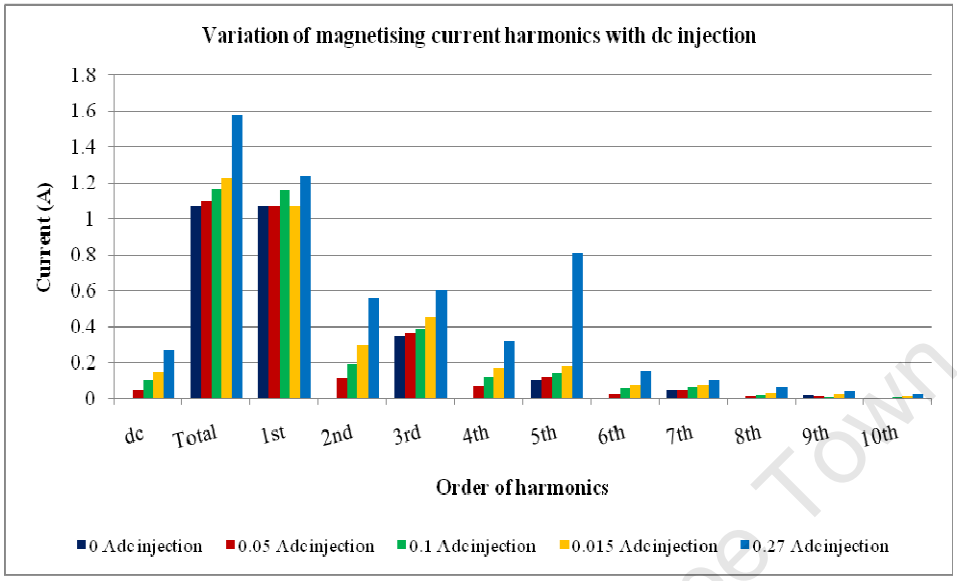


Figure 5.34: Measured primary current harmonic contents in the 6 kVA power transformer in nominal voltage operation, when only DC current circulates in the secondary windings

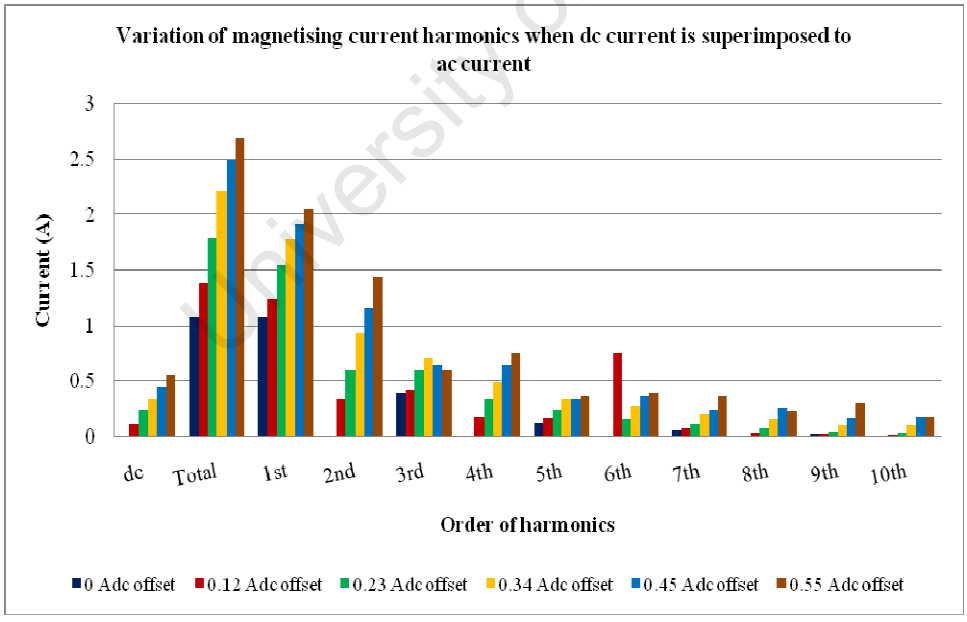


Figure 5.35: Measured primary current harmonic contents in the 6 kVA power transformer in nominal voltage operation, when an AC current circulates with DC current in the secondary windings

Harmonic contents in the primary current are presented as figures 5.34 and 5.35. In recording the results, it was decided to present up to the 10th harmonic since further orders of harmonics were less significant to the work. The results confirm the generation of even harmonics in the supply voltage side current and, as the graphs depict, the harmonics of 2nd, 4th and 6th order increase considerably when a varying DC current is injected whereas the harmonics of order 7th, 9th, show little variation with respect to the DC current injected.

The asymmetry in the secondary current due to DC bias has caused a significant increase in the 2nd and 4th even harmonics. The 3rd and the 5th harmonics have also experienced a significant increase. The increase in the 7th and 9th is mostly due to the existing distortion of the power laboratory supply voltage waveform and also largely due to the no-load asymmetrical magnetizing current distortion. By Fourier even harmonics only exist if the first and second halves of a waveform are not symmetrical (mirror image). Note that non sinusoidal waveforms that are symmetrical will not contain even harmonics. Hence the presence of even harmonics is a good indicator of the asymmetry of the magnetic flux caused by DC mmf.

5.2.1.5 Conclusion

The study of the performance of a power transformer under varying DC current injection and the mitigation of undesired effects has revealed positive results which validate the theory of this study. The main conclusions that can be drawn from the laboratory tests performed are:

- A DC current component in the secondary windings is not transferred on the primary windings.

- A DC component in the secondary windings of a power transformer causes increased distortion, asymmetry and displacement factor in the transformer non load primary current.

- On the evaluation of the transformer's magnetizing current:

(i) There is a change in the time duration of the negative cycle or positive cycle depending on the direction of the offset

(ii) The duration of the positive half cycle is reduced from 10mS of zero dc current injection to 8mS as a result of the positive duration of the current waveform.

(iii) The peak amplitude of the positive half cycle waveform is larger than the negative one.

- A test on the shift in the magnetizing curve (B-H) through the measurements of the hysteresis indicates that:

(i) Although the RC integrator is unable to provide the true representation of a biased flux, the resulting flux suggests a large increase in the peak value of the positive cycle of the magnetizing current.

(ii) When a positive bias is applied to the core, the large peak value of the negative magnetizing current is necessary to maintain symmetry of the primary current.

- With reference to the mitigation measures, it was observed that the complete restoration of the magnetizing current to its original no DC current bias was possible as the cancellation current was increased. The other observation was that DC current injection can be cancelled by similar DC current injection with opposing polarities through the use of extra windings.

- Harmonics analysis revealed that harmonics of orders greater than 10 were of less significance with respect to the research work. The analysis also showed that harmonics of the 2nd, 4th and 6th orders vary considerably with the injection of varying DC current. On the other hand, harmonics of the 7th and 9th orders show little variation with respect to the DC current injection.

- Mitigation of undesired effects of a power transformer under varying DC current injection is achievable.

- For tests on the shift in the magnetizing curve (B-H), further investigations are necessary to provide more details on the shift of the transformer operating point.

- Software which controls the DC current injection and even harmonics is necessary for the cancellation of the DC current injection effects in power transformers.

The next chapter presents the design, modeling and simulation of the single phase inverter system with an output power transformer. Since power transformer flux balance control is the aim of this thesis, and the simulation package used is unable to model some of the power transformer characteristics, namely the flux and the magnetizing field properly, only the effects of the power transformer flux imbalance on the performance of a power transformer will be presented in this thesis. This leaves the Author with the duty of presenting a detailed modeling and simulation of the power transformer in future work.

5.2.2 Investigation using Inverter System

As mentioned in the section above, the experiment was conducted in phases, namely:

- Measurements without inverter's output filter
- Measurements with an inverter's output filter.

5.2.2.1 Measurements without Inverter's Output Filter.

a) Results and Discussion

After the switches were triggered and the dc bus connected, the inverter started running and the output was a PWM signal amplified at the input voltage level, as shown in figure 6.20 below:

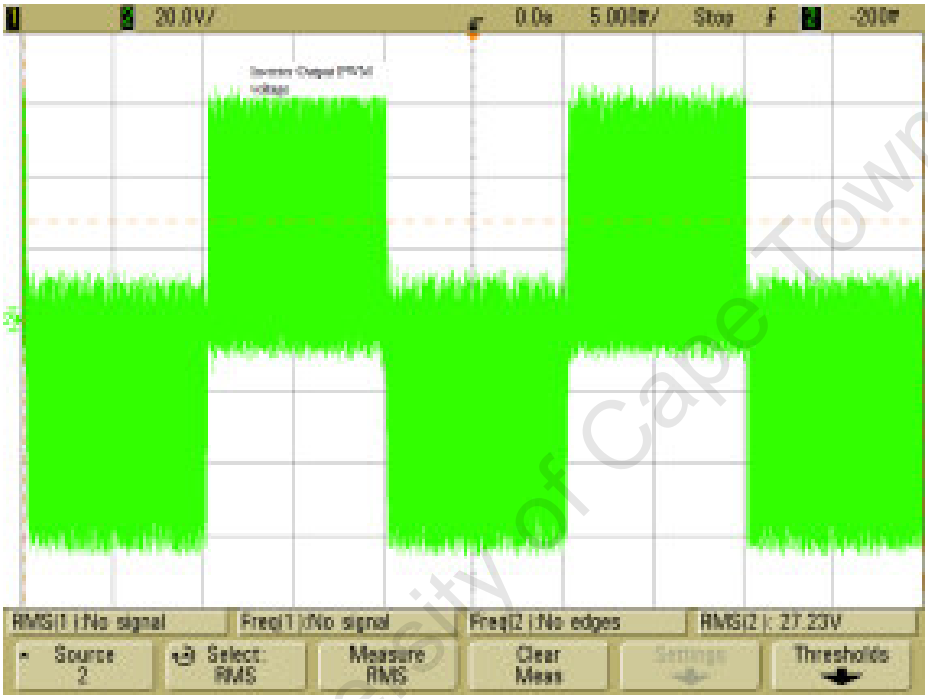


Figure 5.36: Inverter output PWM voltage

The waveform given in the Figure 5.36 above depicts the output voltage of an inverter when there is no filter at its output. The waveform consists of a 50 Hz fundamental and high order harmonics. The harmonics need to be filtered out.

The fundamental voltage V_o is:

$$V_0 = 0.707 * ma * V_{dc} \qquad (6.1)$$

where V_0 represents the rms value of the Inverter's output voltage , ma is the modulation index which corresponds to a value of 0.8 in the design, and V_{dc} is the Inverter's input voltage.

5.2.2.2 Measurements with Inverter's Output Filter

In this experiment, an output filter was added which consisted of a high frequency inductor connected directly to the output of the inverter. The high frequency inductor presents high impedance to components having a high frequency, as explained in the formula below:

$$X_L = Lw \tag{5.1}$$

where X_L is the reactance of the inductor, L is the inductance, and w is the angular frequency which is directly dependant on the frequency of the signal as shown in the formula below:

$$w = 2 * pi * f \tag{5.2}$$

where f is the frequency of the signal.

Next, a 6 kVA power transformer was connected to the output of the inductor. The power transformer has two purposes: to isolate the DC power source to prevent this getting to the load side of the inverter and to step up the inverter's output voltage so that it could reach the standard 230 volts AC required.

a) Results and Discussion

This section of the chapter presents the results obtained when measurements were made on the inverter system with a filter output. The DSP Controller code was also updated to include

a voltage regulation. The regulation utilizes the inverter's output voltage is used for the feedback closed loop control. Results obtained were closer to the desired output waveform. Figure 5.37 below depicts the inverter's output voltage measured at the capacitor filter output terminals:

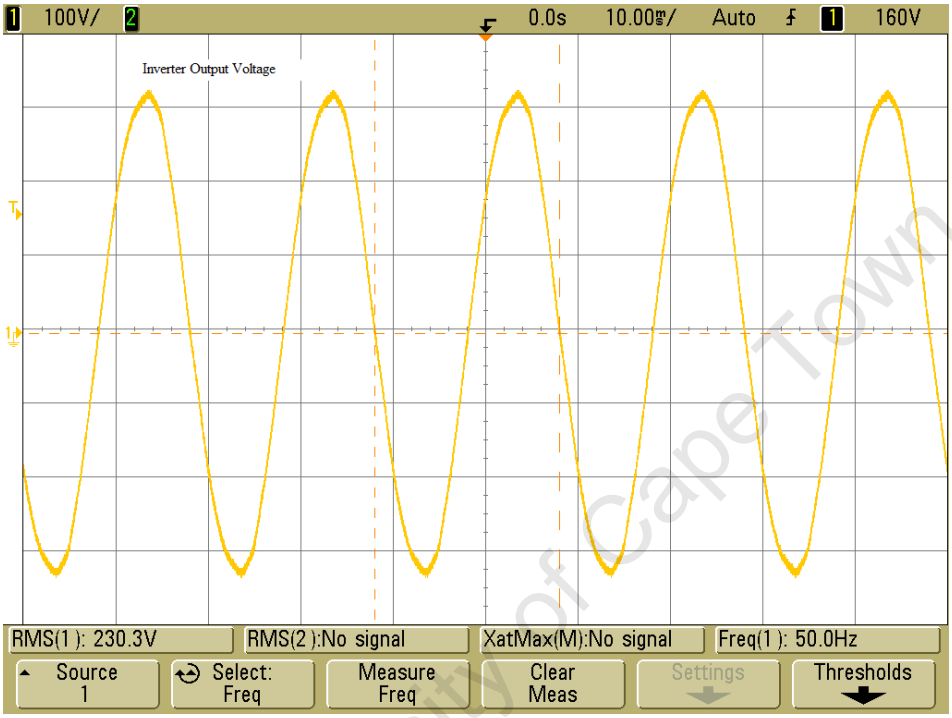


Figure 5.37: Inverter's output voltage measured at the capacitor's filter terminals

Figure 5.37 above shows that the voltage is a good sine wave. The investigation was mostly focused on the power transformer's primary current. The transformer, being the most expensive component in the power system, it was very important to determine the elements that limit its performance. The DC current injection is one of the factors that can harm a power transformer. This Section discusses the results of an investigation of DC bias in the power transformer. First, the power transformer's magnetizing current is presented in Figure 5.38 below:

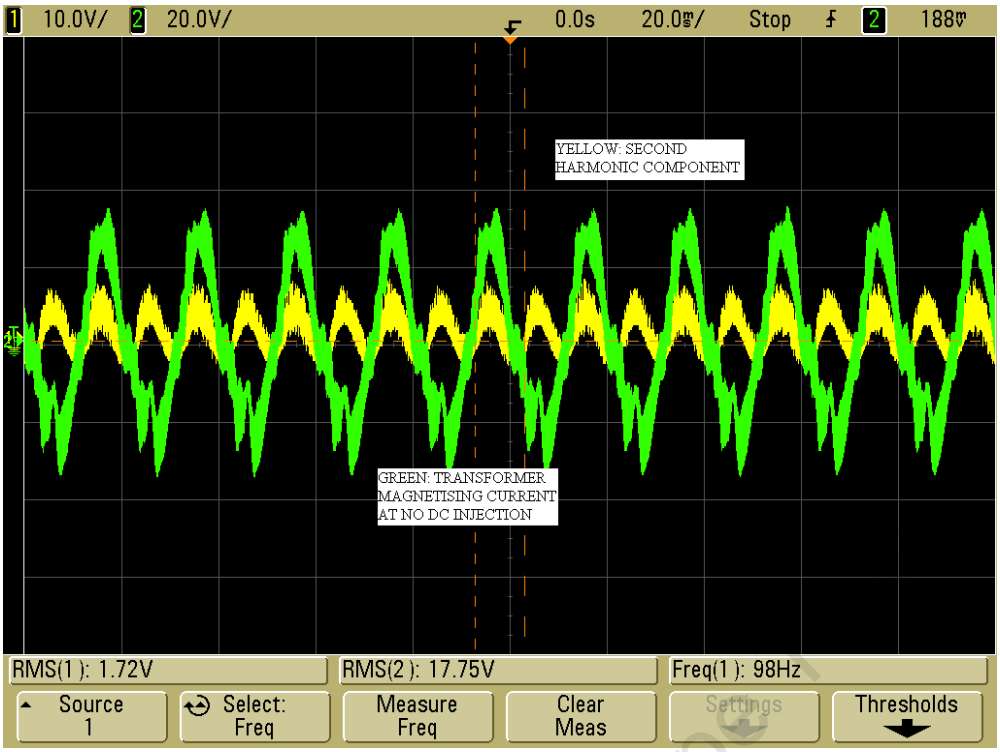


Figure 5.38: Transformer's magnetizing current (Green) and its second harmonic component with no DC bias

Since one of the aims of this project is to restore the symmetry of the magnetic flux caused by DC currents in the primary and secondary side of a 6 kVA power transformer, one needs to (i) extract and measure accurately the magnitude of the second harmonic (ii) minimize its effects on the power transformer.

In this project, the measurement and extraction of a second harmonic (which is a proof of DC injection in the power transformer) was undertaken. Figures 5.39 and 5.41 below depict the amount of the second harmonic in the power transformer's magnetizing current. First, measurements were taken when only the DC current originated from the primary side of the power transformer, that is, the inverter's side. The level of second harmonic in the magnetizing current was measured. This was shown to be at 25% of the fundamental. The % THD was also high, at 17%. This is unacceptable for a case where an inverter is to be

connected to a grid since it would inject DC currents into the grid. Next, an asymmetrical load which is a rectifier in nature was connected to the secondary side of the inverter transformer, as shown in Figure 5.39 below:

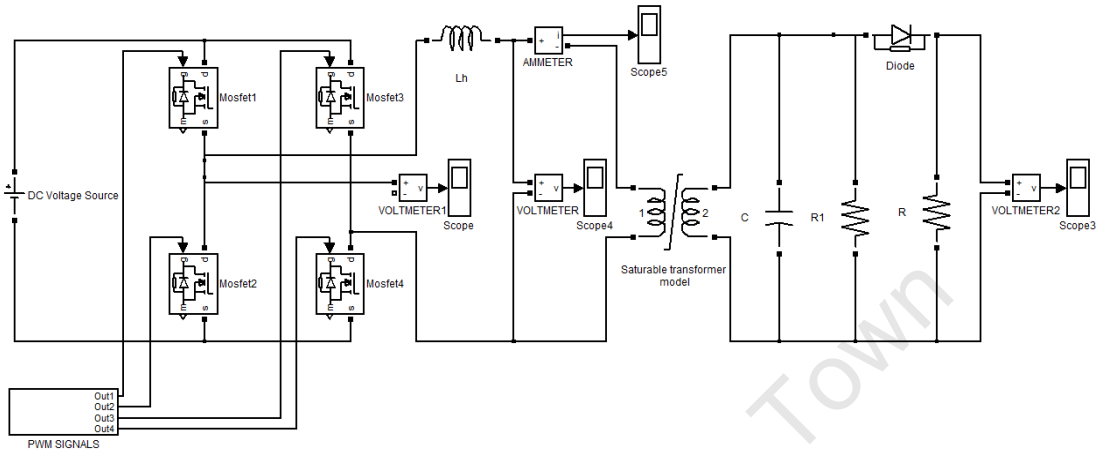


Figure 5.40: Schematic diagram used for asymmetrical current loads investigation

The results obtained are presented in Figure 5.40 and Figure 5.41 below. These highlight the second harmonic component of the transformer's primary current. The second harmonic increased to reach 85% of the fundamental, as shown in Figure 5.41 below. Even order of harmonic increased at a significant rate. Also, odd order of harmonics increased.

Figure 5.40: Transformer's magnetizing current and its second harmonic at no DC injection

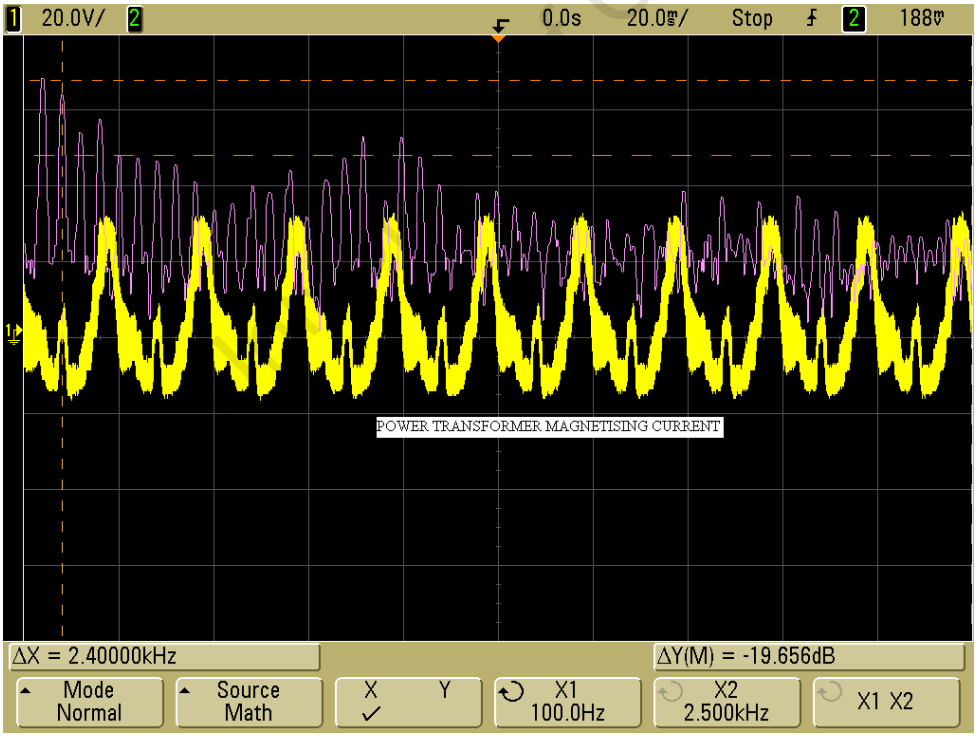


Figure 5.41: Transformer's magnetizing current (yellow) and its harmonic contents when a DC current is injected

From the figures above, magnitudes of DC current offset in the transformer can be evaluated by evaluating the second harmonic component of the transformer's magnetizing current. The level of the second harmonic measured at the primary side of the power transformer was found to vary between 25% and 85% when the load drew from 0 to 12A of asymmetrical current. This is not acceptable since the percentage THD allowed is 5%. The THD of the inverter presented here is 17% at no load. This increase in the percentage of THD is due to the inverter's asymmetrical switching. To achieve one of the aims of this project, the problem of DC injection and even harmonics rising in the inverter system had to be solved. To correct this problem, the main sources that contributed toward the presence of DC offset current in the inverter's power transformer's magnetizing current needed to be identified.

5.2.2.3 Remarks

The digital voltage regulation loop and its proportional controller operated satisfactory. Experimental values of the transformer's primary current second harmonic show that there is a saturation of the transformer's core when an asymmetrical load is connected. The power transformer does not allow a direct current to pass through but the effects of this DC current are sensed on the other side of the transformer.

In the next section of the chapter, sources of DC offset in the inverter's system are described and the removal of DC offset current by second harmonic extraction and suppression is presented.

5.2.3 Mitigation of Undesired effect of DC Current on Power Transformer

5.2.2.2 Using Extra Windings

The results obtained during the tests performed to investigate the level of cancellation of harmonics in the power transformer are presented in the figures 5.42 and 5.43 below:

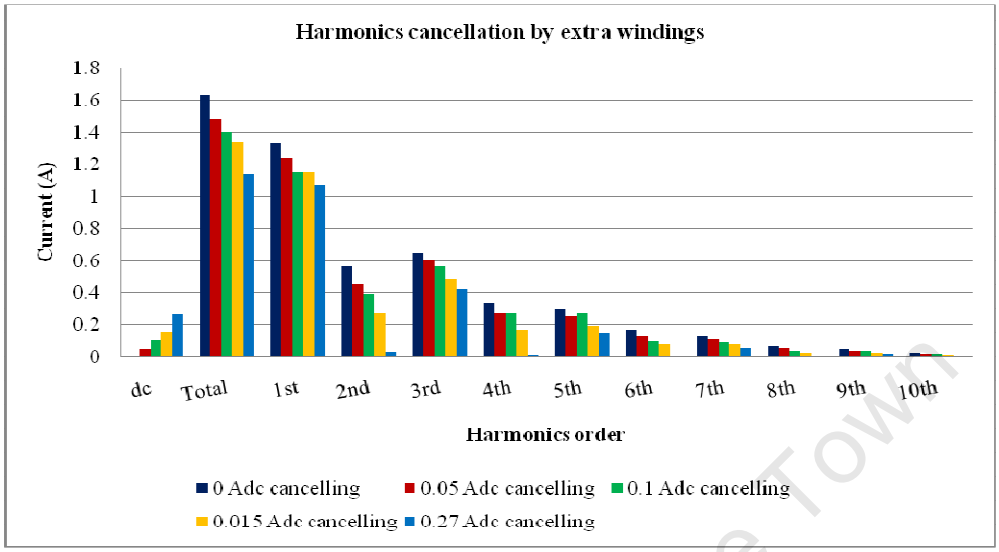


Figure 5.42: Cancellation of magnetizing current harmonic contents using extra windings

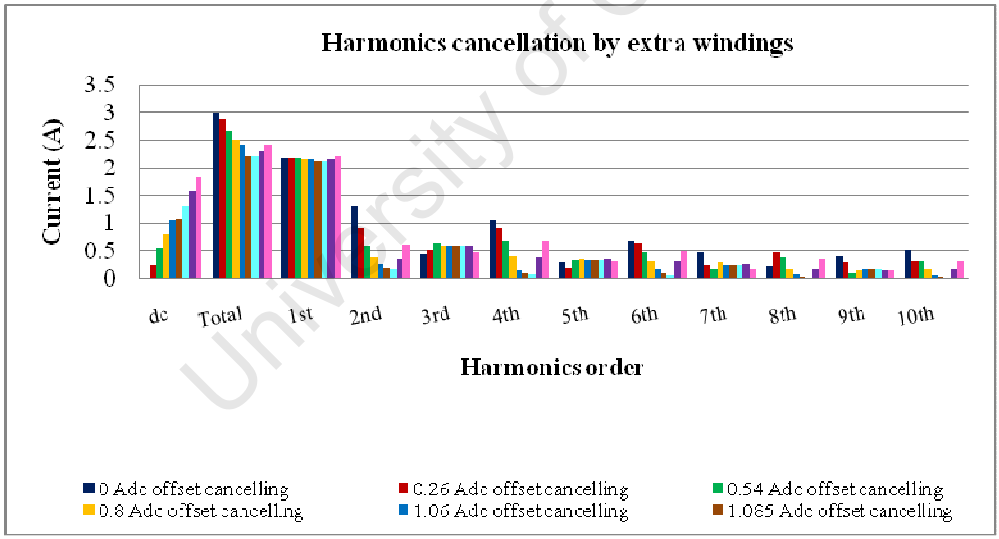


Figure 5.43: Harmonics cancellation using extra windings. The figure shows also the over cancelling which results in harmonics re-generation

The results show that, by applying the same DC current injection on extra windings wound on the same core of a power transformer subjected to a DC bias, the generated harmonics can be cancelled out.

The results show that by applying the same DC current injection into an extra extra winding (third), one can effectively cancel out the undesired DC flux and its effect manifested in harmonic current components and in particular even harmonics (due to flux asymmetry)

5.2.3.1 DC Elimination in Single Phase Inverter System

5.2.3.1.1 Second Harmonic Extraction

Figure 5.44 below shows the results obtained when the filter was used to extract the second harmonic from the transformer's primary current.

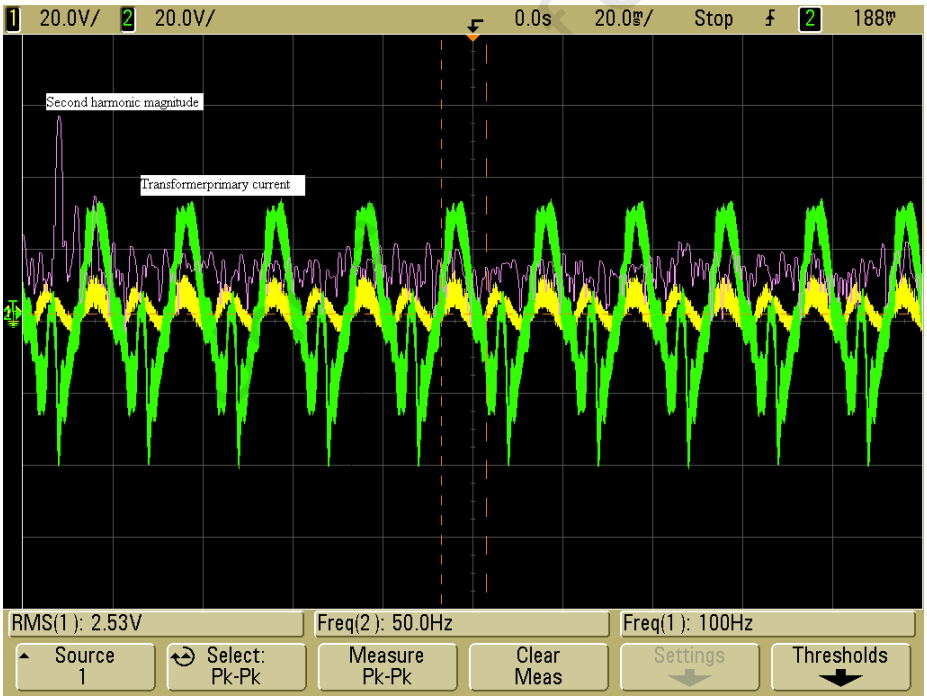


Figure 5.44: Measured transformer's primary current (green) with its second harmonic component when the load is linear

Figure 5.45: Measured transformer's primary current and second harmonic content

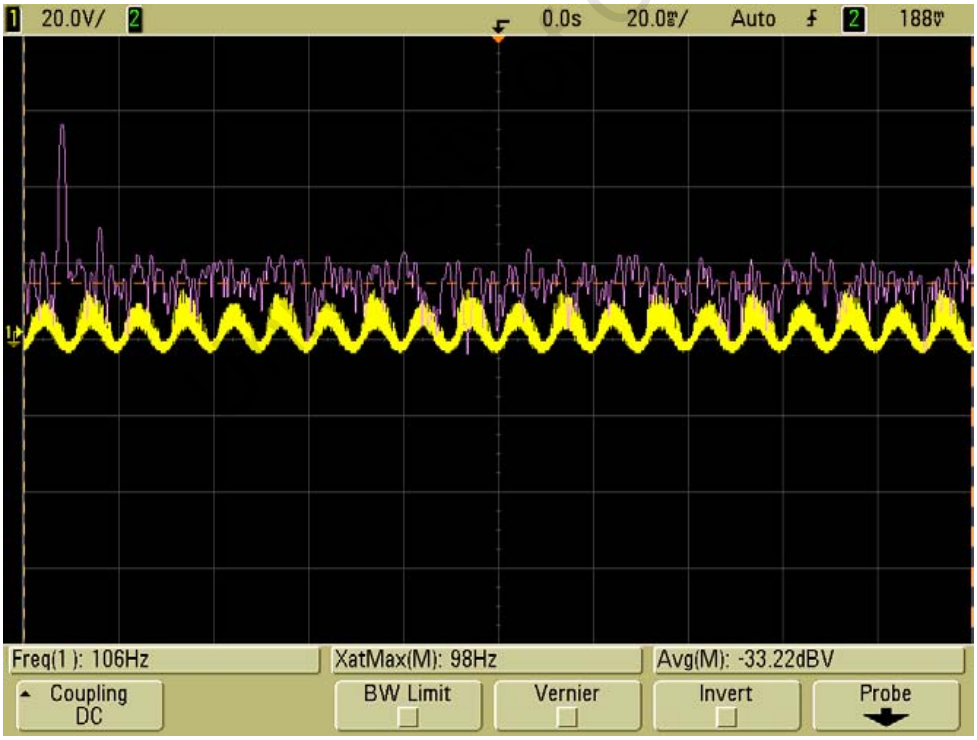


Figure 5.46: Extracted second harmonic

From figure 5.45 presented above, the transformer's primary current is distorted. This is due to the layout of the experimental setup. The filter capacitor is placed at the output of the power transformer and this causes the primary current of the power transformer to be filtered only by the use of the high frequency inductor. The second harmonic component of the primary current already exists even though a linear load is used. The phenomenon has been explained above in section 2.7.1.1. The control system design in this section is aimed at removing the total second harmonic whether a system is loaded by linear or asymmetrical loads. Figure 5.47 below depicts the scenario where an asymmetrical load is connected to the output of the power transformer. The figure shows the magnitude of the second harmonic resulting from such a situation. It also shows that the distortion in the primary current due to the transformer saturation resulting from the DC current introduced by the load connected.

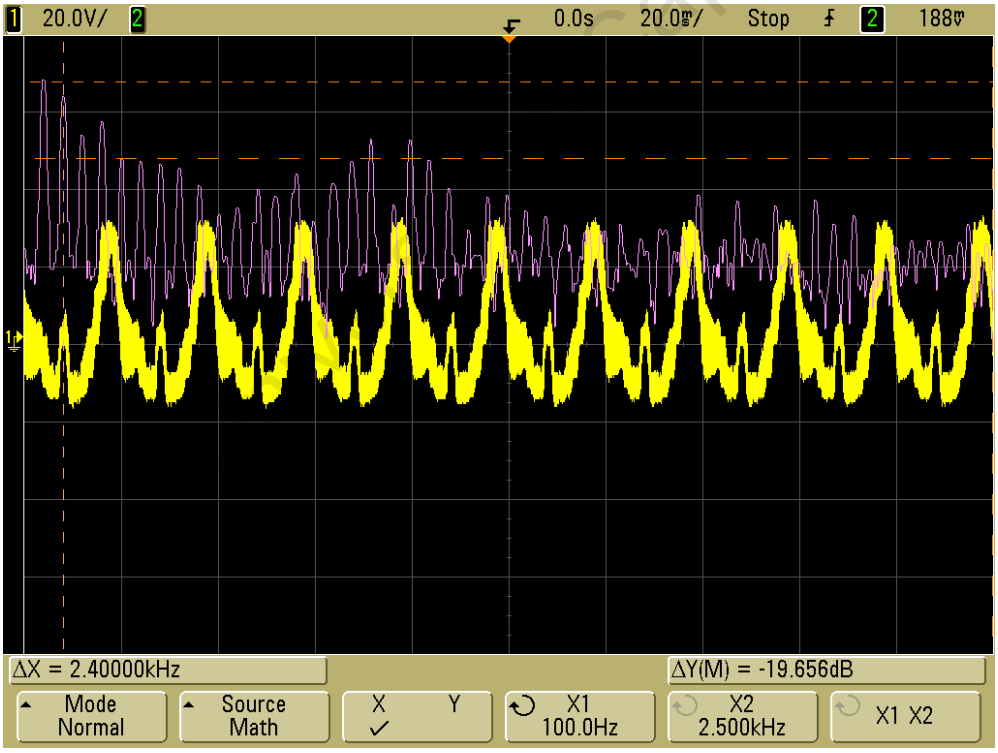


Figure 5.47: Power transformer's primary current and its harmonic contents when an asymmetrical load is connected

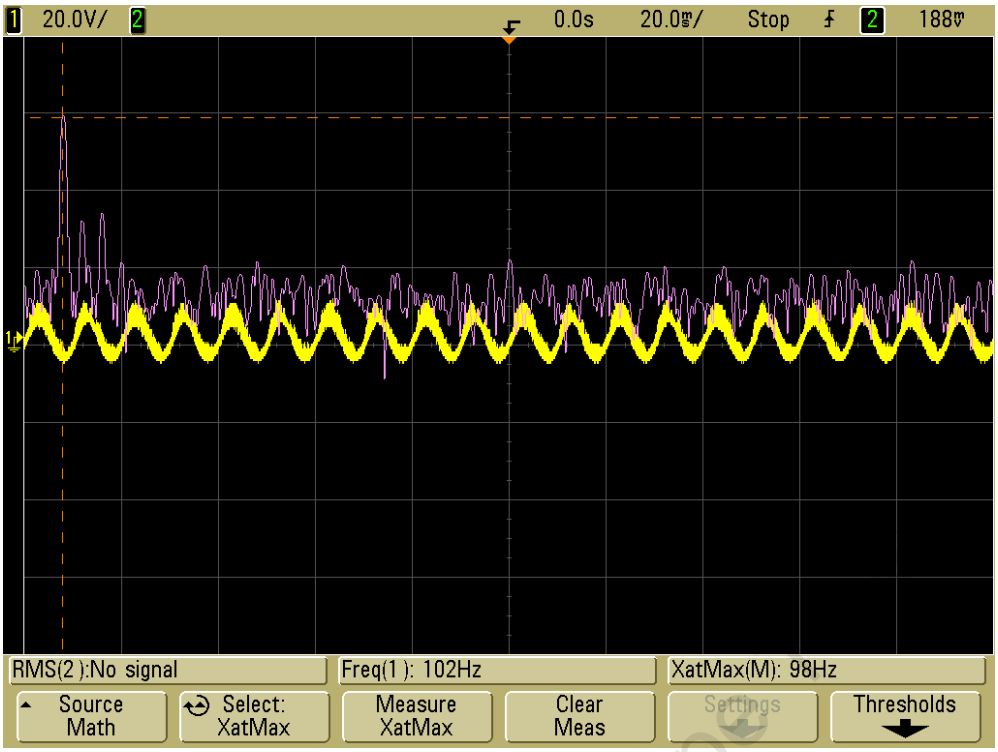


Figure 5.48: Extracted second harmonic under asymmetrical loads

From figure 5.47 shown above, it can be seen that (i) all order of harmonics rise with the connection of an asymmetrical load to the output of the power transformer (ii) the second harmonic could reach the percentage of 85% of the fundamental and (iii) other orders of harmonic also present high percentages when compared to the fundamental. This causes the system to have a high percentage of distortion in the transformer B-H characteristic (trace obtained from integrating the voltage), the flux density presents a high peak in the positive half cycle, and the time duration of the positive half cycle is reduced. This is the evidence that the power transformer has reached saturation; experiencing an increase in reactive power and a rise in even harmonics. Details regarding the transformer's behavior under saturation were given earlier in this chapter. The total second harmonic (most prominent) was extracted in order to mitigate it, and its magnitude is shown in figure 5.48 above.

5.2.3.1.2 DC magnetic flux Suppression

In this project, a digital PI controller was designed and used to mitigate the second harmonic content of the transformer's primary current. This was accomplished by embedding the digital PI controller code into the code designed to implement DC/AC conversion using DSP. The control algorithm was designed to provide the removal of the DC flux.

The block of code for the implementation of a digital PI controller is provided in appendix J, together with the overall code.

The complete DSP-based inverter's system with DC offset and even harmonic control system was designed and built. The DSP ran the inverter by providing the PWM signals for inverter MOSFET switches. A DC voltage offset in the correct direction was introduced into the PWM comparison signal. This signal is proportional to the value of the error signal that represents the level of the amplitude of the second current harmonic.

Figure 5.49 below depicts the results obtained from the mitigation process. The figure shows that mitigation was successfully achieved to some extent only and needed more refinement in the measurement of the second current harmonic. Nevertheless, the results were encouraging as it showed that the principle of measuring the second harmonic of the primary side current can be used for the purpose of an error signal in the PI control loop.

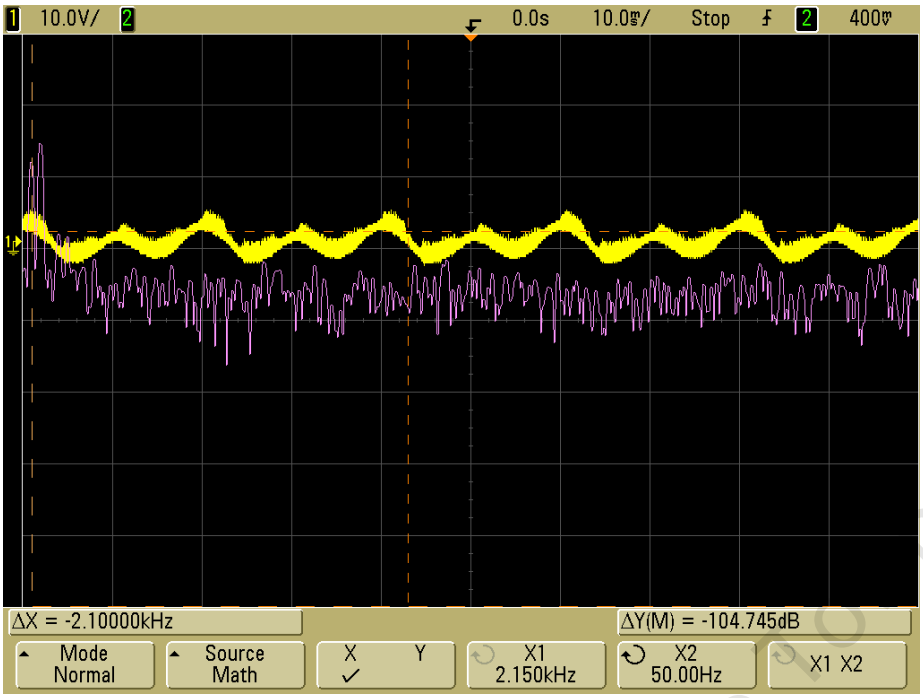


Figure 5.49: First harmonic content in the extracted second harmonic

The design of the second harmonic extractor was then revised to narrow again the band. Three identical extractor circuits were placed in cascade to achieve better results. As shown in figure 5.50, only the remaining second harmonic is represented in the results obtained after mitigation.

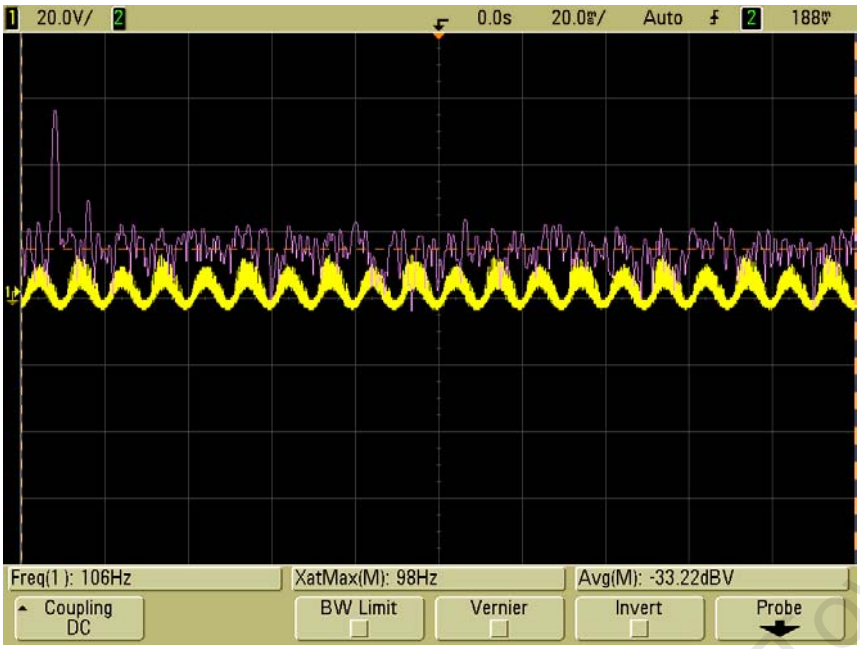


Figure 5.50: Extracted second harmonic after mitigation

As can be seen from Figure 5.50 above, the mitigation of the second harmonic was improved to some degree. Further improvements will be the subject of future work.

The next chapter presents conclusions and recommendations resulting from the research undertaken to investigate the effects of DC current on power transformers, especially, when these are connected to the output of inverter systems.

Chapter 6

CONCLUSION AND RECOMMENDATIONS

6.1 Conclusion

The results obtained and presented in chapter 5 of this thesis show that the objectives outlined in chapter 1 have been achieved. Based on the experimental results of this research, the following conclusions can be drawn:

a) Although there is limited literature on the subject, the author has provided what is available in the literature on the state of the art of the key aspects of designing and implementing the digital voltage regulation with a flux balance control for single phase inverter systems.

b) When a pure resistor is connected to a 6 kVA power transformer and a pure alternating current circulates in the secondary windings, it can be seen that the waveforms are purely symmetrical which ensures that there is no DC offset resulting from the load connected.

   The waveforms are composed of the fundamental components only. This is due to the linearity in the loads connected.

c) After the investigation of the effects of the asymmetrical loads on a 6 kVA power transformer, simulation results presented show that asymmetrical loads introduce a high level of distortion in the power transformer currents which is manifested in even harmonics.

d) The harmonics generated by non-linear loads are very high in magnitude when compared to the fundamental and this could result in low transformer efficiency since the power transferred from the primary to the secondary is only dependent on the fundamental component of the voltage and the current.

e) The results of a simulation using a single phase inverter system which has a LC filter and a power transformer at the output and a proportional P voltage regulator show that the simulation was a success.

The study of the performance of a power transformer under varying DC current injection and the mitigation of adverse effects has revealed some positive results which validate the theory. The main conclusions that can be drawn from the laboratory experiments performed are:

- A DC current component in the secondary windings is not transferred on the primary windings but causes asymmetry in the BH characteristics of the transformer core.
- The above causes primary magnetizing current distortion.
- The degree of asymmetry can be assessed by observing the 2^{nd} current harmonic in particular.
- A signal representing the magnitude of the second harmonic can be used in a PI feedback control loop which is to introduce a PWM generated DC current component that will in turn restore the symmetry of the primary side harmonic. This is manifested by the suppression of the 2nd current harmonic on the inverter output.
- With reference to the mitigation measures, it was observed that the complete restoration of the magnetizing current to its original no DC bias was possible as the cancellation current was adjusted so that the total DC mmf which the transformer is subjected to

amounted to zero. Another observation was that DC injection could also be cancelled by similar DC injection with opposing polarities through the use of extra windings.

- Harmonics analysis revealed that harmonics of orders greater than 10 were of less significance with respect to the research work. The analysis also showed that harmonics of the 2nd, 4th and 6th orders vary considerably with the injection of varying DC current. On the other hand, harmonics of the 7th and 9th orders show little variation with respect to the DC injection.

- For tests on the shift in the magnetizing curve (B-H), further investigations are necessary to provide more details on the shift of the transformer operating point.

- Software which controls the DC injection by the inverter by observing and extracting the most prominent even current harmonics (2nd) in the primary side was designed and tested successfully for the cancellation of the DC injection effects in power transformers.

6.2 Recommendations

Based on the experimental results and conclusions of this report, mitigation of the undesired effects of DC offset by using the inverter itself in inverter connected power transformer can be an effective solution without resorting to extra windings.

The results obtained in canceling the DC bias was only met partially when an attempt was made to introduce DC current into the primary side by adjusting the DC voltage offset of the PWM waveform. However, the Author is of the opinion that, with further work and more refined measurement of the second current harmonics on the primary side (inverter side) and better control algorithm of the DSP which generated the PWM signals, total cancelling is achievable.

It is, therefore, recommended that the control system can be designed and implemented in industrial stand alone and grid connected inverters so as to mitigate any DC component that the inverter transformer may be subjected to (primary and/or secondary side).

The following suggestions are made by the Author:

- Replacement of the TMS320LF2407 DSP provided in section 2.7.1.1 of chapter 2 with a more powerful DSP so as to achieve better mitigation of the DC flux must be considered.
- Improvement of the PI control of the PWM DC voltage offset so as to get better response in correcting the DC flux.

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APPENDIX A

THEORETICAL MODEL OF A SINGLE PHASE HALF WAVE RECTIFIER

A.1 Theoretical Model

Any used appliance which has a switch for half power can introduce a DC current component in the transformer to which it is connected. In this type of load, a diode is connected in series in the load circuit to reduce the voltage,, and hence the power by half. However by half-wave rectifying the transformer secondary voltage in this manner, there is inevitable interaction with the power transformer impedance.

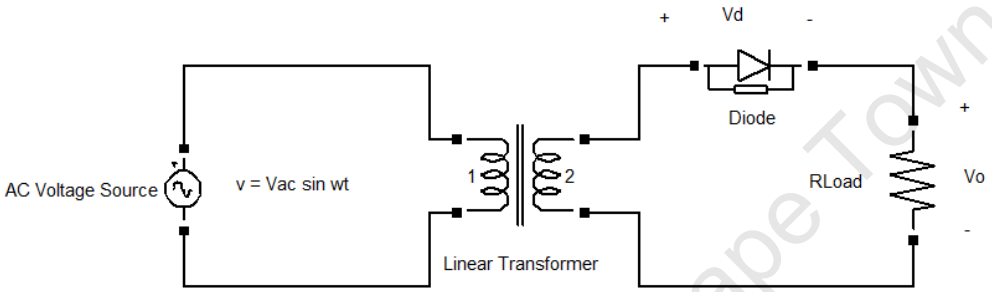


Figure A.1: Single phase half-wave rectifier

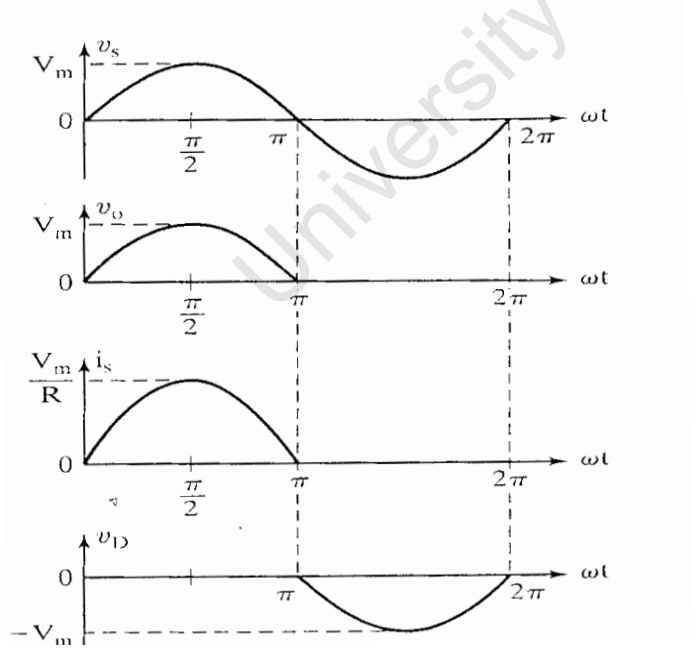


Figure A.2: Single phase half-wave rectifier voltages and current waveforms

The performance parameters of the single phase half-wave rectifier shown in figure A.1 above are:

- Average value of the output voltage, V_{dc}
- Average value of the output current, I_{dc}
- Output DC power, P_{dc}

  where $P_{dc} = V_{dc} I_{dc}$
- rms value of the output voltage, V_{rms}
- Output ac power, P_{ac}

  where $P_{ac} = V_{rms} I_{rms}$
- Efficiency, η

  where $\eta = P_{dc} / P_{ac}$
- Effective (rms) value of the ac component of the output voltage, V_{ac}

  where $V_{ac} = \sqrt{V_{rms}{}^2 - V_{dc}{}^2}$
- Form factor, FF

  $FF = V_{rms} / V_{dc}$
- Ripple factor, RF

$$RF = V_{ac} / V_{dc}$$

- Alternate form for ripple factor

$$RF = \sqrt{V_{rms} / V_{dc}}^{2} - 1 = \sqrt{FF^{2} - 1}$$

- Transformer utilization factor, TUF

$TUF = P_{dc} / V_s I_s$ where $V_s I_s$ are the rms voltage and current of the power transformer secondary.

- Displacement angle, ϕ

- Displacement factor, DF

where $DF = \cos\phi$

- Harmonic factor, HF

$$HF = \left(\frac{I_S^{2} - I_{s1}^{2}}{I_{S1}^{2}} \right)^{\frac{1}{2}} = \left[\left(\frac{I_s}{I_{s1}} \right)^{2} - 1 \right]^{\frac{1}{2}}$$

- Power factor, PF

$$PF = \frac{V_S I_{S1}}{V_S I_S} \cos\phi = \frac{I_{S1}}{I_S} \cos\phi$$

- Crest factor, CF

$$CF = \frac{I_{S(peak)}}{I_S}$$

A.2 Numerical Calculations

Table A.1 below shows the results obtained by numerically calculating the parameters of a single phase half wave rectifier.

Table A.1: Results obtained by numerical calculation of the half-wave rectifier parameters.

Parameters	**Values**
Average voltage, V_{dc}	$0.318V_m$
Average current, I_{dc}	$0.318V_m / R$
rms voltage, V_{rms}	$0.5V_m$
rms current, I_{rms}	$0.5V_m / R$
Output dc power, P_{dc}	$\frac{(0.318V_m)^2}{R}$
Output ac power, P_{ac}	$\frac{(0.5V_m)^2}{R}$
Efficiency, η	40.5%
Transformer form factor, FF	157%
Ripple factor, RF	121%

Transformer utilization factor, *TUF*	0.286
Crest factor, *CF*	2
Power factor, *PF*	0.707

APPENDIX B

MATHEMATICAL ANALYSIS AND SIMULATION OF A SINGLE PHASE VOLTAGE CONTROLLED VOLTAGE SOURCE INVERTER (VCVSIs)

B.1 Introduction

VCVSs are widely used in power supplies and power quality controllers, as well as in renewable energy, marine and military applications.

Their role in the circuit is to convert a direct current (DC) power source into an alternating current (AC) power source. They require, therefore, a very robust design and high efficiency, especially when they are used in distributed generators (DG) or renewable energy applications, where their failure can be costly and irremediable.

The design of Inverters has improved since the availability of software and simulation packages such as MATLAB/SIMULINK and PSpice, as well as the development of programmable devices used in motion control such as Digital Signal Processors (DSPs). These allow enhancements to inverter performance at the analysis and design stage rather than time-consuming improvements during implementation.

This Chapter of the Thesis presents a simulation of a 6 KVA single phase full bridge Inverter using MATLAB/SIMULINK. The choice of MATLAB/SIMULINK for modeling and simulations of the Inverter's dynamics in this work was influenced by its simplicity in analyzing linear and non-linear systems in continuous time, sampled time or a combination of both.

Mathematical modeling and simulations are used to design the controller of the inverter system which is a non linear system. The Inverter showed in Figure B.1 below outputs a square wave voltage.

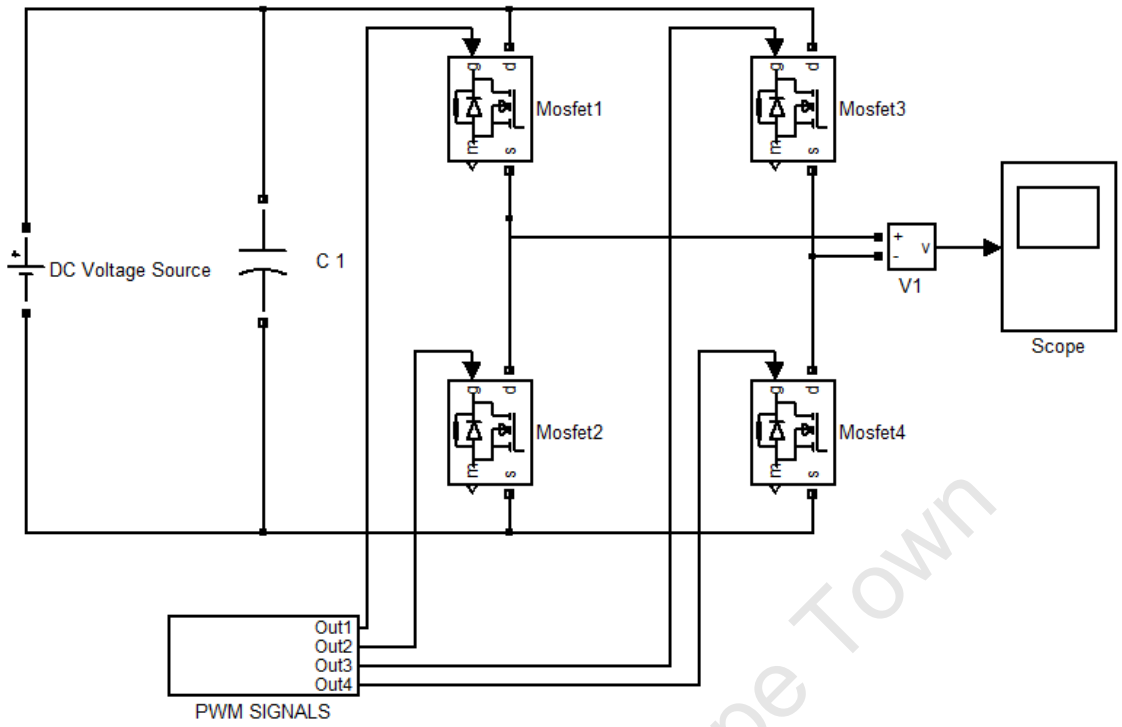


Figure B.1: Inverter System without Filter and Transformer's Output

The Inverter's equivalent circuit is also presented in order to easily analyze mathematically the output voltage depending on the combinations of switches both for bipolar and unipolar switching techniques.

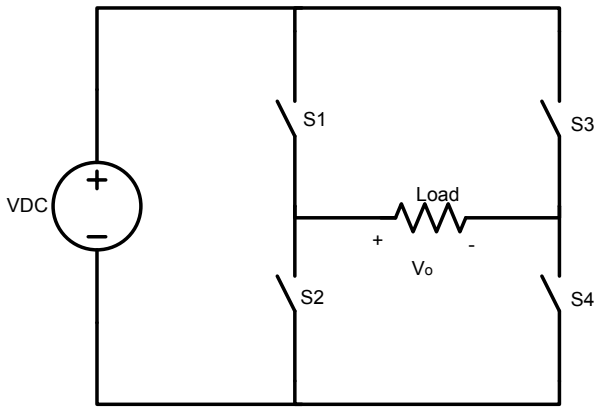


Figure B.2: Equivalent Circuit of Inverter System

To illustrate the concept of the AC waveform generation the following circuit diagrams are provided, where V_{dc} represents the Inverter's input DC voltage and V_0 is the Inverter's output voltage, S1, S2,S3, and S4 are the Inverter's power switches and the load is a simple Resistor.

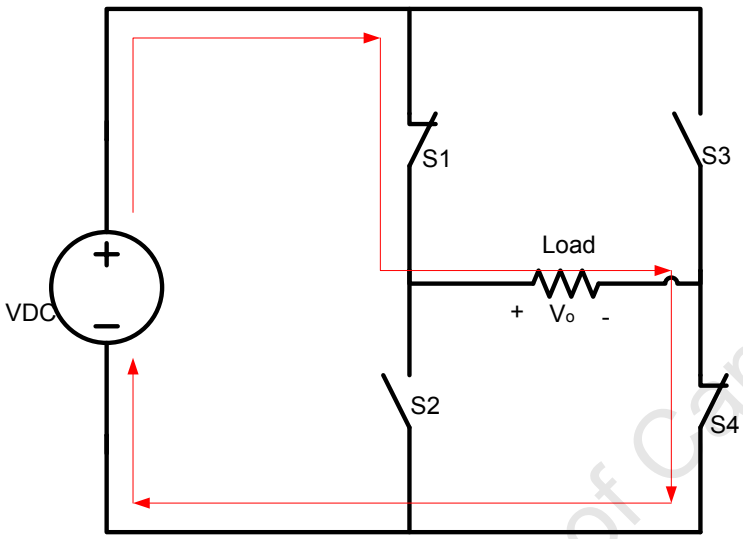


Figure B.3: Inverter's Half Cycle Output

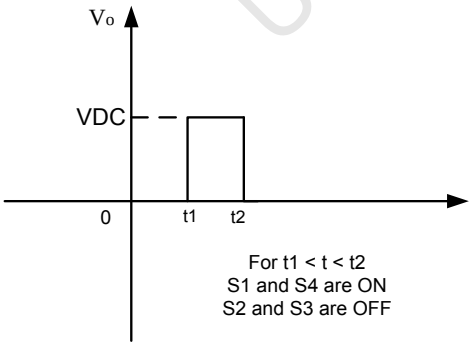


Figure B.4: Inverter's Output Waveform for the Positive Half Cycle

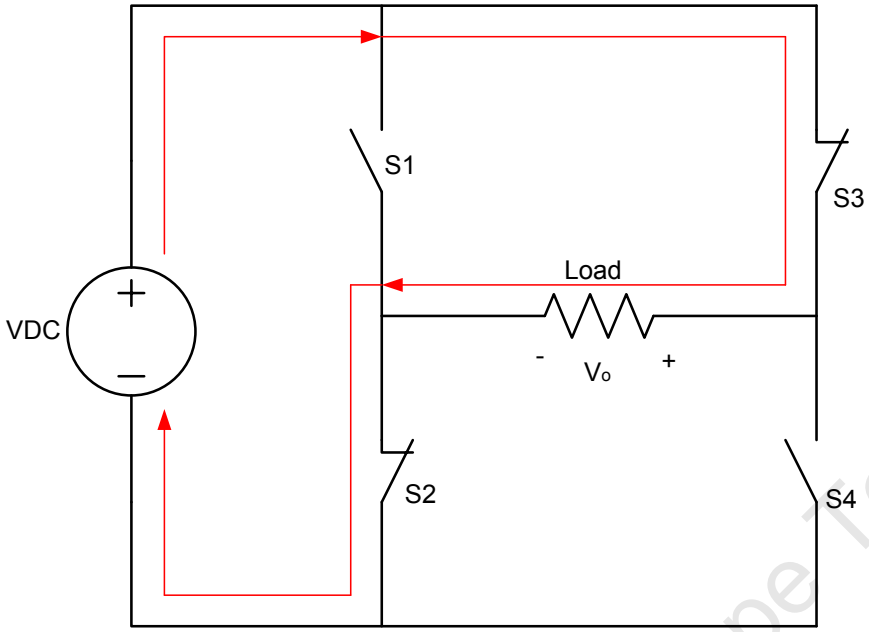


Figure B.5: Inverter's Negative Half Cycle Operation

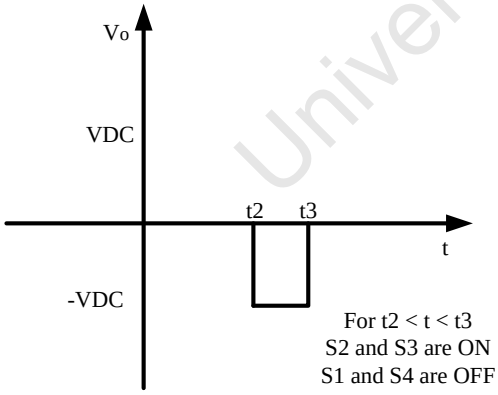


Figure B.6: Inverter's Negative Half Cycle Voltage Waveform

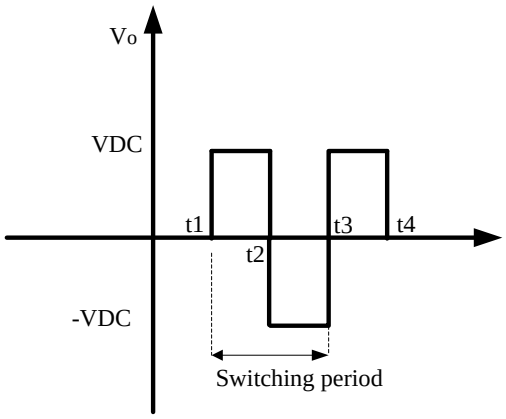


Figure B.7: Inverter's Full Cycle Output Voltage Waveform

B.2 Mathematical Modeling of a Pulse Width Modulation Power Inverter

To produce a sinusoidal output voltage waveform of variable frequency and amplitude, a sinusoidal reference signal (Vref) is compared with the triangular waveform (Vtri). The amplitude modulation index (m), which controls the rms value of the output voltage, is defined as equation (B.1) the ratio of the peak value of the reference signal and the peak value of the carrier signal, which is a triangular waveform in this case.

$$m = \frac{Vref}{Vtri} \qquad \text{(B.1)}$$

Leg A and B of the full-bridge inverter shown in figure B.2 are controlled separately by comparing Vtri with Vref and Vtri with -Vref. The resulting waveforms are used to control the switches as follows:

In leg A:

Vref > Vtri : S1 on and

Vref <Vtri: S4on

And

In leg B:

-*Vref > Vtri: S3 on* and

-*Vref< Vtri: S2 on*

The PWM signals obtained are applied to leg A and B of the full bridge Inverter.

Note that S4 and S2 will automatically be created as the inversion of S1 and S3 respectively (Figure B.2). In the section below a simulation process is presented where the above mathematical model is used to design a code using Matlab.

APPENDIX C

% a Program for Analysis of a Voltage-source inverter with Sinusoidal-Pulse-Width Modulated output.

% a Program for Analysis of a Voltage-source inverter with Sinusoidal-Pulse-Width Modulated output.

```
% PART I (Preparation)
% In this part, the screen is cleared. Any other functions, figures and
% variables are also cleared. The name of the program is displayed.
clc
clear all
disp('Voltage-Source Inverter with Sinusoidal-Pulse Width Modulated Output')
disp('')
%
% PART II
% In this part, the already known variables are entered. The User is
% asked to enter the other variables.
% Vrin is the DC input voltage.
Vdc=48V;
% f is the frequency of the output voltage waveform.
f=input('The frequency of the output voltage, f = ');
% Z is the load impedance in per unit.
Z=1;
% ma is the modulation index
ma=input('the modulation index,ma, (0<ma<1), ma = ');
% phi is load-phase-angle
phi=input('the phase angle of the load in degrees = ');
% fc is frequency of the carrier signal.
fc=input('The frequency of the carrier signal= ');
%
% PART III
% Calculating load parameters.
%
phi=phi*pi/180;
% R and L are the load resistance and inductance respectively.
```

```
R=Z*cos(phi);
L=(Z*sin(phi))/(2*pi*f);
%
% PART IV
% calculating the frequency modulation which defines the number of pulses per period, N
N=fc/f;
%
%PART V
% Building the Sawtooth signal,Vt, the output voltage waveform, Vout,
% and finding the beginning (alpha) and the end (beta)for each of the output pulses.
%
% In each period of the sawtooth, there is one increasing and decreasing part of
% the sawtooth, thus the period of the output voltage waveform is divided into
% 2N sub-periods, k is used as a counter of these sub-periods.
% For calculation purposes each of these sub-periods is divided into 50 points, i.e., the
% output voltage waveform period is divided into 100N points.
% j is a counter inside the sub-period
% i is the generalized time counter

for k=1:2*N
  for j=1:50
    % Finding the generalized time counter
    i=j+(k-1)*50;
    % Finding the time step
    wt(i)=i*pi/(N*50);
    % Finding the half period of the output voltage.
    if(sin(wt(i)))>0
       hpf=1;
    else
       hpf=-1;
    end
```

```
  % Calculating the modulating signal.
   ma1(i)=ma*abs(sin(wt(i)));
  % Calculating the sawtooth waveform
  if rem(k,2)==0
     Vt(i)=0.02*j;
     if abs(Vt(i)-ma*abs(sin(wt(i))))<=0.011
        m=j;
        beta(fix(k/2)+1)=3.6*((k-1)*50+m)/N;
     else
        j=j;
     end

  else
     Vt(i)=1-0.02*j;
    if abs(Vt(i)-ma*abs(sin(wt(i))))<0.011
        l=j;
        alpha(fix(k/2)+1)=3.6*((k-1)*50+l)/N;
     else
        j=j;
     end

  end
  % calculating the output voltage waveform

  if Vt(i)>ma*abs(sin(wt(i)))
     Vout(i)=0;
  else
     Vout(i)=hpf*Vdc;
  end

end
```

```
end
beta(1)=[];
% PART VI
% Displaying the beginning (alpha), the end (beta) and the width
% of each of the output voltage pulses.

disp('  ')
disp('.....................................................................')
disp('alpha    beta    width')
[alpha'  beta'  (beta-alpha)']

% PART VII
% Plotting the, the triangular carrier signal, Vt,
% the modulating signal and the output voltage waveform, Vout.

a=0;
subplot(2,1,1)
plot(wt,Vt,wt,ma1,wt,a)
axis([0,2*pi,-2,2])
ylabel('Vt, m(pu)');

subplot(2,1,2)
plot(wt,Vout,wt,a)
axis([0,2*pi,-2,2])
ylabel('Vo(pu)');
xlabel('Radian');

% PART VIII
% Analyzing the output voltage waveform

% Finding the rms value of the output voltage
```

```
Vo =sqrt(1/(length(Vout))*sum(Vout.^2));
disp('The rms Value of the output Voltage = ')
Vo
%  Finding the harmonic contents of the output voltage waveform
y=fft(Vout);
y(1)=[];
x=abs(y);
x=(sqrt(2)/(length(Vout)))*x;
disp('The rms Value of the output voltage fundamental component = ')
x(1)
%
% Finding the THD of the output voltage
THDVo = sqrt(Vo^2 -x(1)^2)/x(1);
%
% PART IX
% Calculating the output current waveform
m=R/(2*pi*f*L);
DT=pi/(N*50);
C(1)=-10;
%
i=100*N+1:2000*N;
Vout(i)=Vout(i-100*N*fix(i/(100*N))+1);
%
for i=2:2000*N;
C(i)=C(i-1)*exp(-m*DT)+Vout(i-1)/R*(1-exp(-m*DT));
end
%
%
% PART X
% Analyzing the output current waveform
% F inding the harmonic contents of the output current waveform
```

```
for j4=1:100*N
   CO(j4)=C(j4+1900*N);
 CO2= fft(CO);
 CO2(1)=[];
 COX=abs(CO2);
COX=(sqrt(2)/(100*N))*COX;
end

% Finding the RMS value of the output current.
 CORMS = sqrt(sum(CO.^2)/(length(CO)));
 disp(' The RMS value of the load current =')
 CORMS

%Finding the THD for the output current
 THDIo = sqrt(CORMS^2-COX(1)^2)/COX(1);

% PART XI
% Finding the supply current waveform
%
for j2=1900*N+1:2000*N
    if Vout(j2)~=0
      CS(j2)=abs(C(j2));
     else
     CS(j2)=0;
   end
end
% PART XII
% Analyzing the supply current waveform
%
% Supply current waveform and its average value
for j3=1:100*N
```

```
    CS1(j3)=abs(CS(j3+1900*N));
end
CSRMS= sqrt(sum(CS1.^2)/(length(CS1)));
disp('The RMS value of the supply current is')
CSRMS

CSAV= (sum(CS1)/(length(CS1)));
disp('The Average value of the supply current is')
CSAV

% Finding the Fourier analysis of the supply current waveform
%
 CS2= fft(CS1);
 CS2(1)=[];
 CSX=abs(CS2);
 CSX=(sqrt(2)/(100*N))*CSX;

% PART XIII
% Displaying the calculated parameters.
 disp(' Performance parameters are')
 THDVo
 THDIo
  a=0;
%
%PART XIV
% Opening a new figure window for plotting of
% the output voltage, output current, supply current and the harmonic
% contents of these values
%
Figure (2)
%
```

```
 subplot(3,2,1)
 plot(wt,Vout(1:100*N),wt,a);
 title('');
 axis([0,2*pi,-1.5,1.5]);
 ylabel('Vo(pu)');
%
%
 subplot(3,2,2)
 plot(x(1:100))
 title('');
 axis([0,100,0,0.8]);
%%
%%
 ylabel('Von(pu)');
%
 subplot(3,2,3)
 plot(wt,C(1900*N+1:2000*N),wt,a);
 title('');
 axis([0,2*pi,-1.5,1.5]);
 ylabel('Io(pu)');
%
 subplot(3,2,4)
 plot(COX(1:100))
 title('');
 axis([0,100,0,0.8]);
 ylabel('Ion(pu)');
%
 subplot(3,2,5)
 plot(wt,CS(1900*N+1:2000*N),wt,a);
 axis([0,2*pi,-1.5,1.5]);
 ylabel('Is(pu)');
```

```
 xlabel('Radian');
%
 subplot(3,2,6)
 plot(CSX(1:100))
 hold
 plot(CSAV,'*')
 text(5,CSAV,'Average valu')
 title('');
 axis([0,100,0,0.8]);
 ylabel('Isn(pu)');
 xlabel('Harmonic Order');
```

APPENDIX D

EXPERIMENTAL SET UP

Figure D.1: Laboratory set up for hysteresis and harmonics measurements

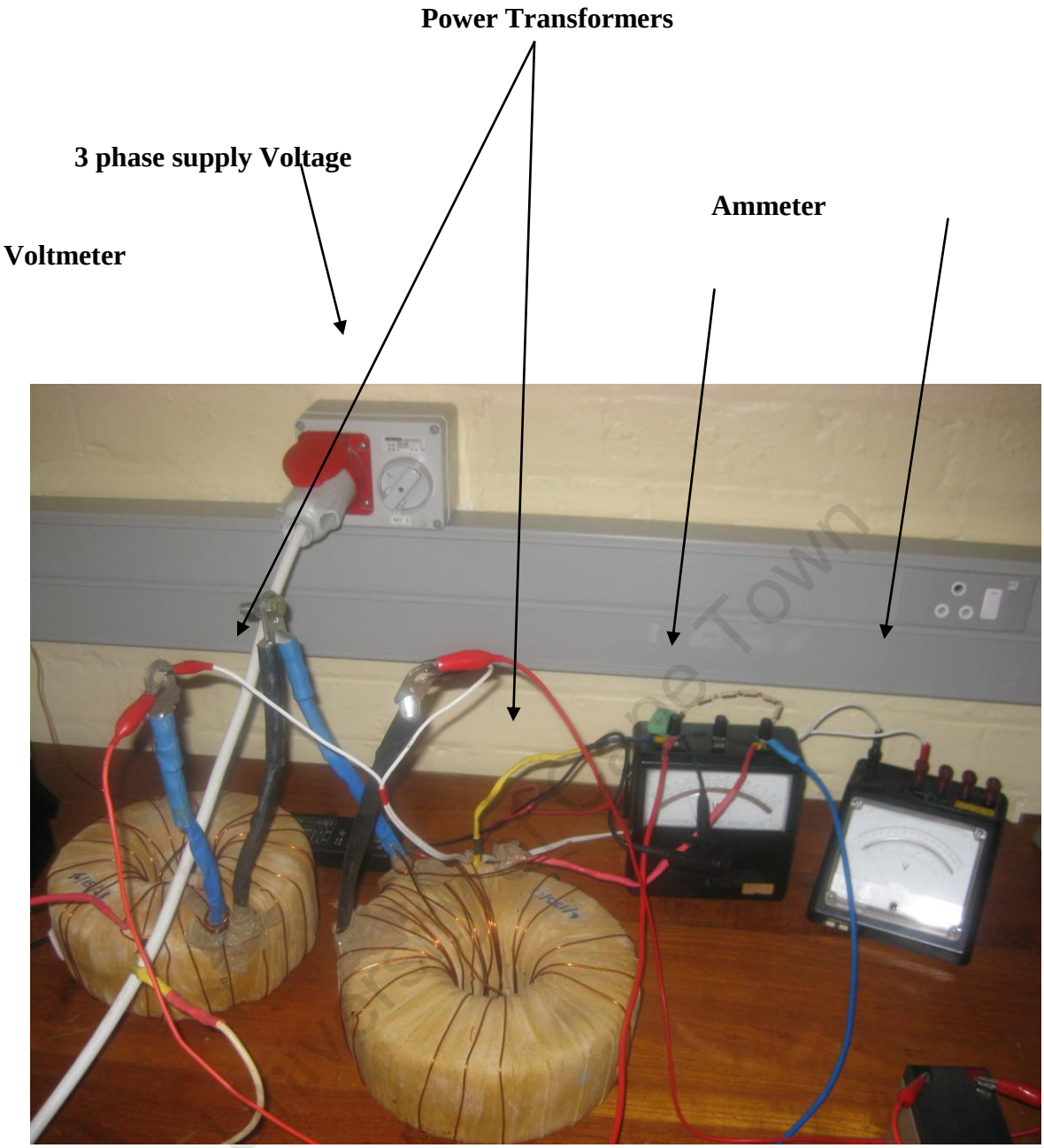


Figure D.2: Power transformers used in anti-parallel mode to inject/cancel the secondary voltage

Figure D.1: Laboratory setup schematic of inverter system

International
IOR Rectifier

Power MOSFET Basics

By Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

Power MOSFET Basics

Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

Discrete power MOSFETs employ semiconductor processing techniques that are similar to those of today's VLSI circuits, although the device geometry, voltage and current levels are significantly different from the design used in VLSI devices. The metal oxide semiconductor field effect transistor (MOSFET) is based on the original field-effect transistor introduced in the 70s. Figure 1 shows the device schematic, transfer characteristics and device symbol for a MOSFET. The invention of the power MOSFET was partly driven by the limitations of bipolar power junction transistors (BJTs) which, until recently, was the device of choice in power electronics applications.

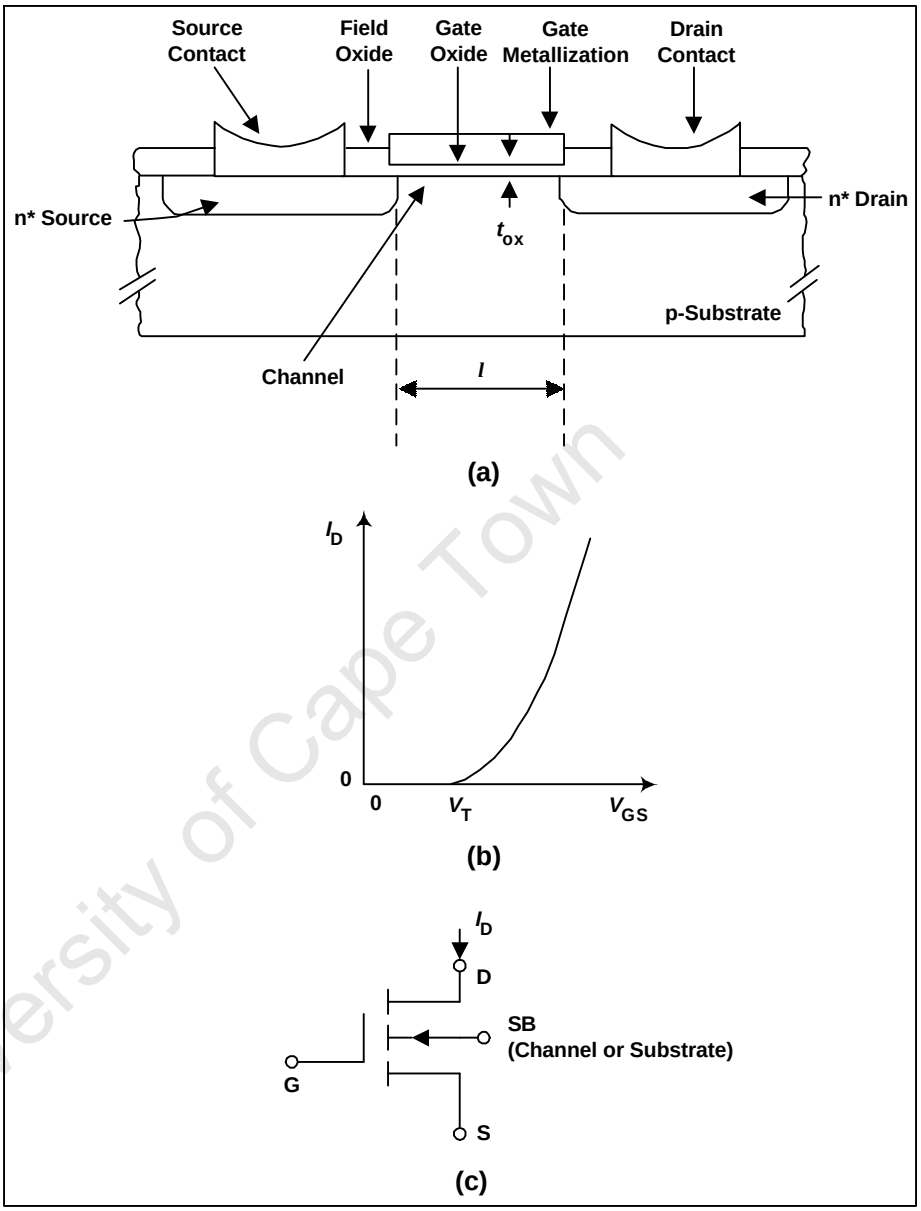


Figure 1. Power MOSFET (a) Schematic, (b) Transfer Characteristics, (c) Device Symbol.

Although it is not possible to define absolutely the operating boundaries of a power device, we will loosely refer to the power device as any device that can switch at least 1A. The bipolar power transistor is a current controlled device. A large base drive current as high as one-fifth of the collector current is required to keep the device in the ON state.

Also, higher reverse base drive currents are required to obtain fast turn-off. Despite the very advanced state of manufacturability and lower costs of BJTs, these limitations have made the base drive circuit design more complicated and hence more expensive than the power MOSFET.

Another BJT limitation is that both electrons and holes contribute to conduction. Presence of holes with their higher carrier lifetime causes the switching speed to be several orders of magnitude slower than for a power MOSFET of similar size and voltage rating. Also, BJTs suffer from thermal runaway. Their forward voltage drop decreases with increasing temperature causing diversion of current to a single device when several devices are paralleled. Power MOSFETs, on the other hand, are majority carrier devices with no minority carrier injection. They are superior to the BJTs in high frequency applications where switching power losses are important. Plus, they can withstand simultaneous application of high current and voltage without undergoing destructive failure due to second breakdown. Power MOSFETs can also be paralleled easily because the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all components.

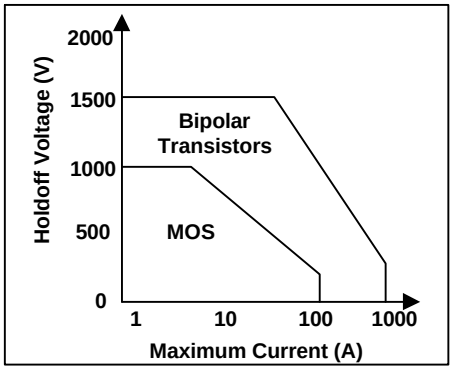


Figure 2. Current-Voltage Limitations of MOSFETs and BJTs.

However, at high breakdown voltages (>200V) the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with similar voltage rating. This makes it more attractive to use the bipolar power transistor at the expense of worse high frequency performance. Figure 2 shows the present current-voltage limitations of power MOSFETs and BJTs. Over time, new materials, structures and processing techniques are expected to raise these limits.

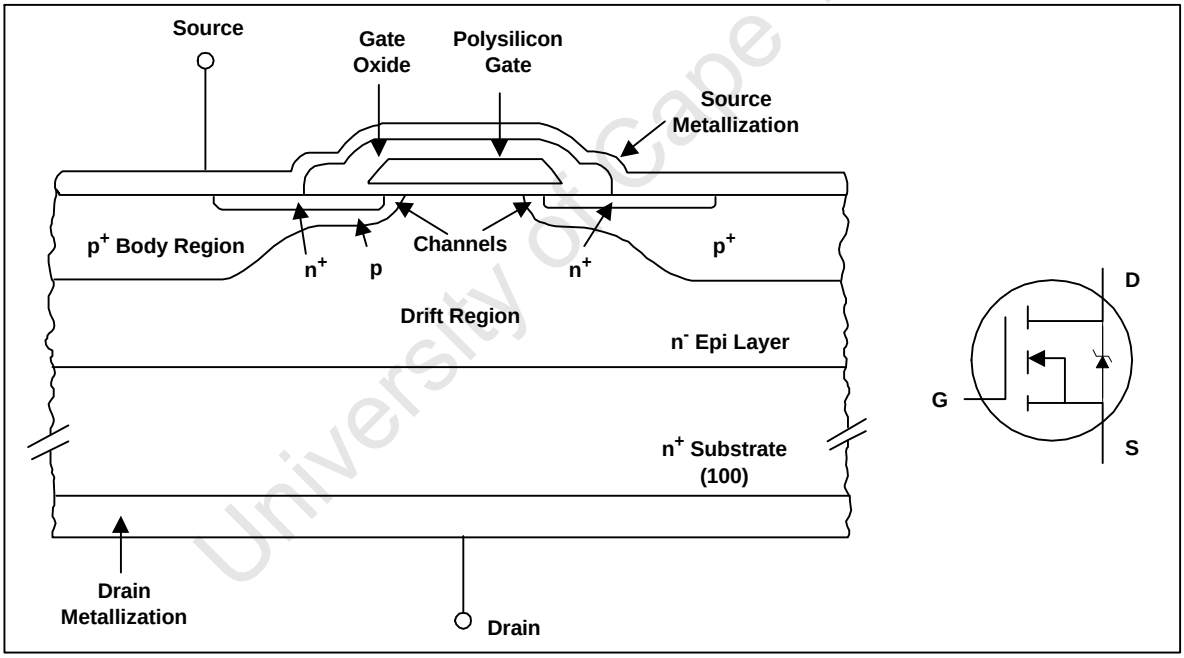


Figure 3. Schematic Diagram for an n-Channel Power MOSFET and the Device.

Figure 3 shows schematic diagram and Figure 4 shows the physical origin of the parasitic components in an n-channel power MOSFET. The parasitic JFET appearing between the two body implants restricts current flow when the depletion widths of the two adjacent body diodes extend into the drift region with increasing drain voltage. The parasitic BJT can make the device susceptible to unwanted device turn-on and premature breakdown. The base resistance RB must be minimized through careful design of the doping and distance under the source region. There are several parasitic capacitances associated with the power MOSFET as shown in Figure 3.

C_{GS} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is independent of applied voltage. C_{GD} consists of two parts, the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. C_{GD} is a nonlinear function of voltage. Finally, C_{DS}, the capacitance associated with the body-drift diode, varies inversely with the square root of the drain-source bias. There are currently two designs of power MOSFETs, usually referred to as the planar and the trench designs. The planar design has already been introduced in the schematic of Figure 3. Two variations of the trench power MOSFET are shown Figure 5. The trench technology has the advantage of higher cell density but is more difficult to manufacture than the planar device.

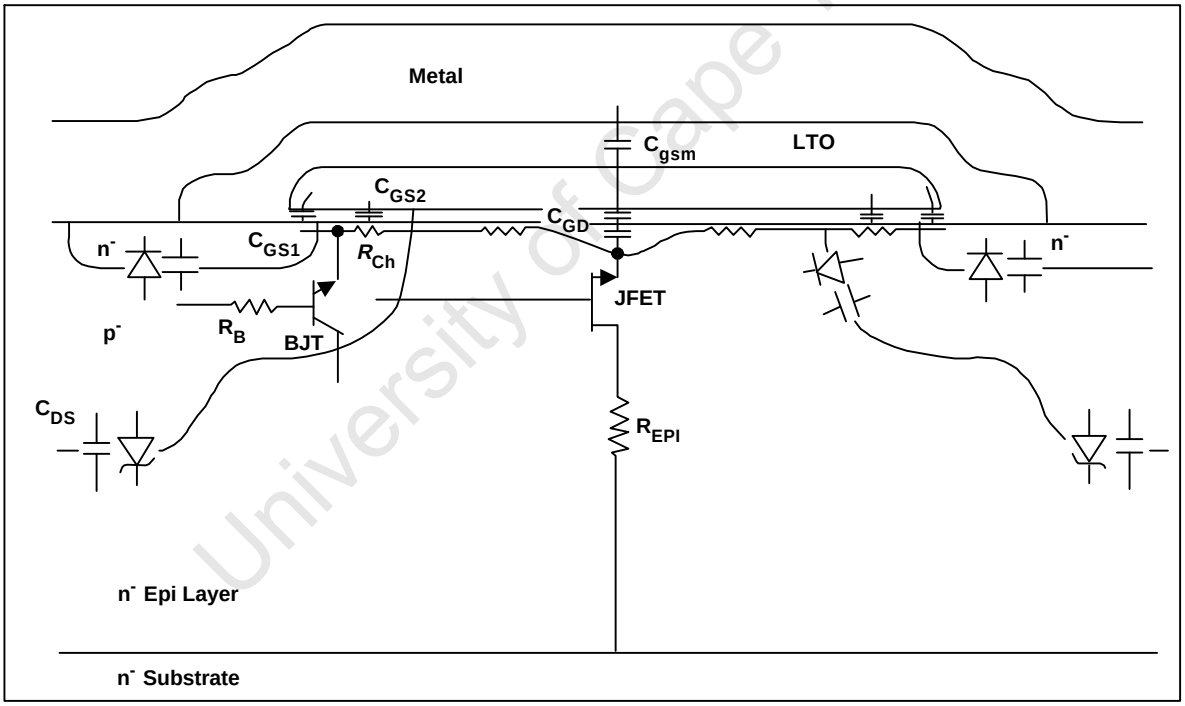


Figure 4. Power MOSFET Parasitic Components.

BREAKDOWN VOLTAGE

Breakdown voltage, BV_{DSS}, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. Current-voltage characteristics of a power MOSFET are shown in Figure 6. BVDSS is normally measured at 250μA drain current. For drain voltages below BV_{DSS} and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift p-n junction. Two related phenomena can occur in poorly designed and processed devices: punch-through and reach-through. Punch-through is observed when the depletion region on the source side of the body-drift p-n junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristics as shown in Figure 7. The leakage current flowing between source and drain is denoted by I_{DSS}. There are tradeoffs to be made between $R_{DS(on)}$ that requires shorter channel lengths and punch-through avoidance that requires longer channel lengths.

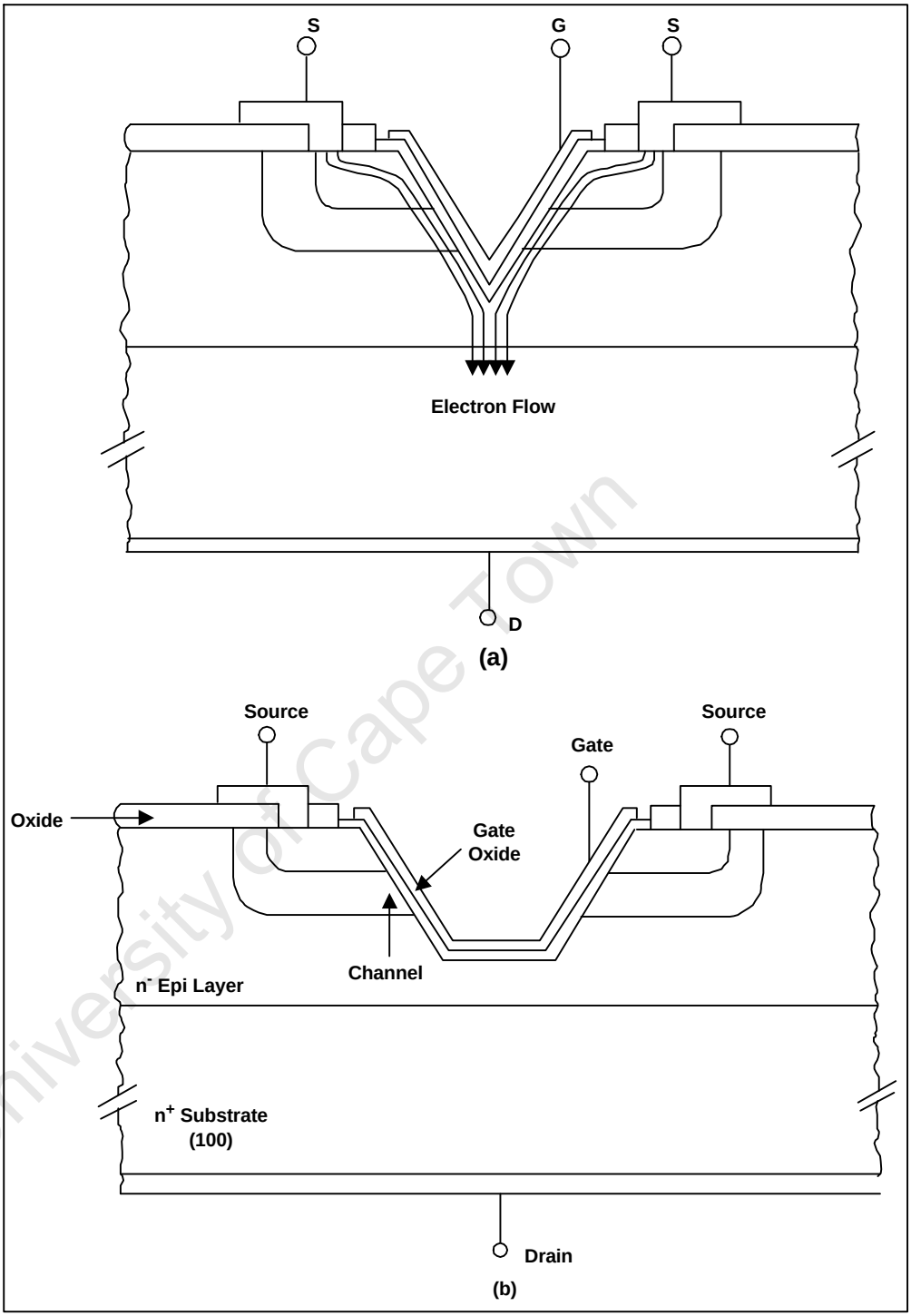


Figure 5. Trench MOSFET (a) Current Crowding in V-Groove Trench MOSFET, (b) Truncated V-Groove MOSFET

The reach-through phenomenon occurs when the depletion region on the drift side of the body-drift p-n junction reaches the epilayer-substrate interface before avalanching takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of $2x10^5$ V/cm where avalanching begins.

ON-RESISTANCE

The on-state resistance of a power MOSFET is made up of several components as shown in Figure 8:

$$R_{DS(on)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml} \quad (1)$$

where:

R_{source} = Source diffusion resistance
R_{ch} = Channel resistance
R_A = Accumulation resistance
R_J = "JFET" component-resistance of the region between the two body regions
R_D = Drift region resistance
R_{sub} = Substrate resistance

Wafers with substrate resistivities of up to 20mΩ-cm are used for high voltage devices and less than 5mΩ-cm for low voltage devices.

R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain Metallization and the silicon, metallization and Leadframe contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices.

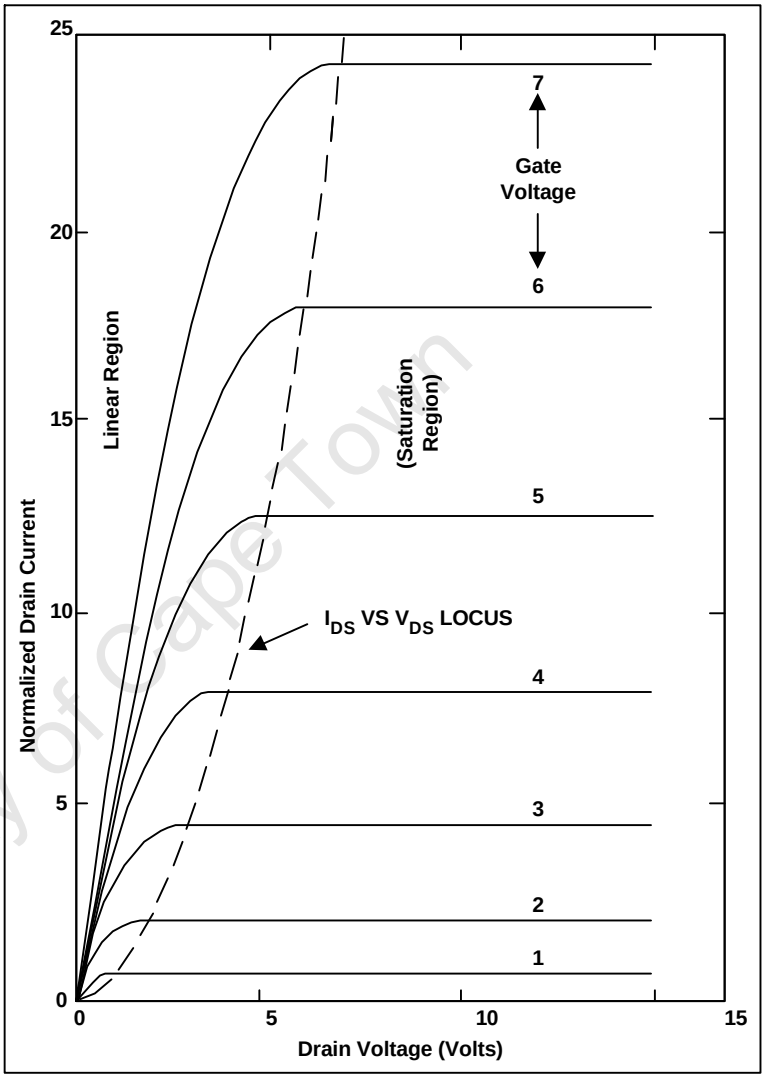


Figure 6. Current-Voltage Characteristics of Power MOSFET

Figure 9 shows the relative importance of each of the components to $R_{DS(on)}$ over the voltage spectrum. As can be seen, at high voltages the $R_{DS(on)}$ is dominated by epi resistance and JFET component. This component is higher in high voltage devices due to the higher resistivity or lower background carrier concentration in the epi. At lower voltages, the $R_{DS(on)}$ is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires and leadframe. The substrate contribution becomes more significant for lower breakdown voltage devices.

TRANSCONDUCTANCE

Transconductance, gfs, is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a V_{gs} that gives a drain current equal to about one half of the maximum current rating value and for a VDS that ensures operation in the constant current region. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases. Cell density has increased over the years from around half a million per square inch in 1980 to around eight million for planar MOSFETs and around 12 million for the trench technology. The limiting factor for even higher cell densities is the photolithography process control and resolution that allows contacts to be made to the source metallization in the center of the cells.

Channel length also affects transconductance. Reduced channel length is beneficial to both gfs and on-resistance, with punch-through as a tradeoff. The lower limit of this length is set by the ability to control the double-diffusion process and is around 1-2mm today. Finally the lower the gate oxide thickness the higher gfs.

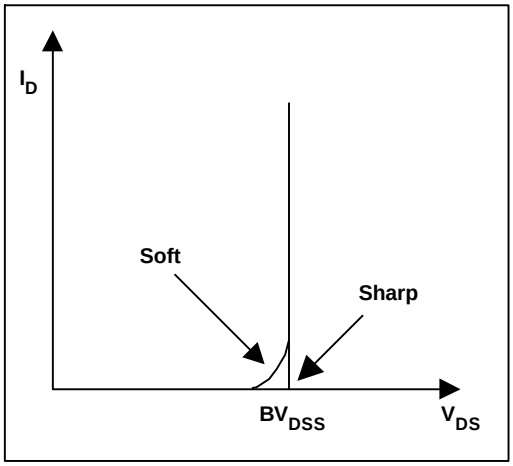


Figure 7. Power MOSFET Breakdown Characteristics

THRESHOLD VOLTAGE

Threshold voltage, V_{th}, is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. V_{th} is usually measured at a drain-source current of 250μA. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic-compatible devices with thinner gate oxides. With power MOSFETs finding increasing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of RDS(on) and Vth.

DIODE FORWARD VOLTAGE

The diode forward voltage, VF, is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. Figure 10 shows a typical I-V characteristics for this diode at two temperatures. P-channel devices have a higher VF due to the higher contact resistance between metal and p-silicon compared with n-type silicon. Maximum values of 1.6V for high voltage devices (>100V) and 1.0V for low voltage devices (<100V) are common.

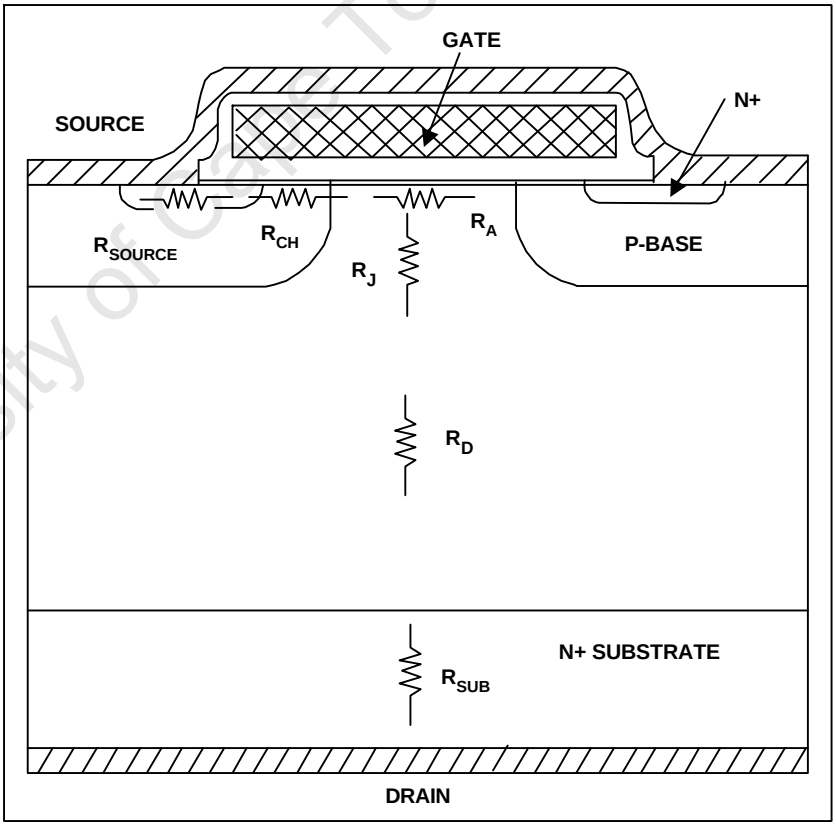


Figure 8. Origin of Internal Resistance in a Power MOSFET.

POWER DISSIPATION

The maximum allowable power dissipation that will raise the die temperature to the maximum allowable when the case temperature is held at 25^{0}C is important. It is give by Pd where:

$$P_d = \frac{T_{jmax-25}}{R_{thJC}} \qquad (2)$$

T_{jmax} = Maximum allowable temperature of the p-n junction in the device (normally 150^{0}C or 175^{0}C) R_{thJC} = Junction-to-case thermal impedance of the device.

DYNAMIC CHARACTERISTICS

When the MOSFET is used as a switch, its basic function is to control the drain current by the gate voltage. Figure 11(a) shows the transfer characteristics and Figure 11(b) is an equivalent circuit model often used for the analysis of MOSFET switching performance.

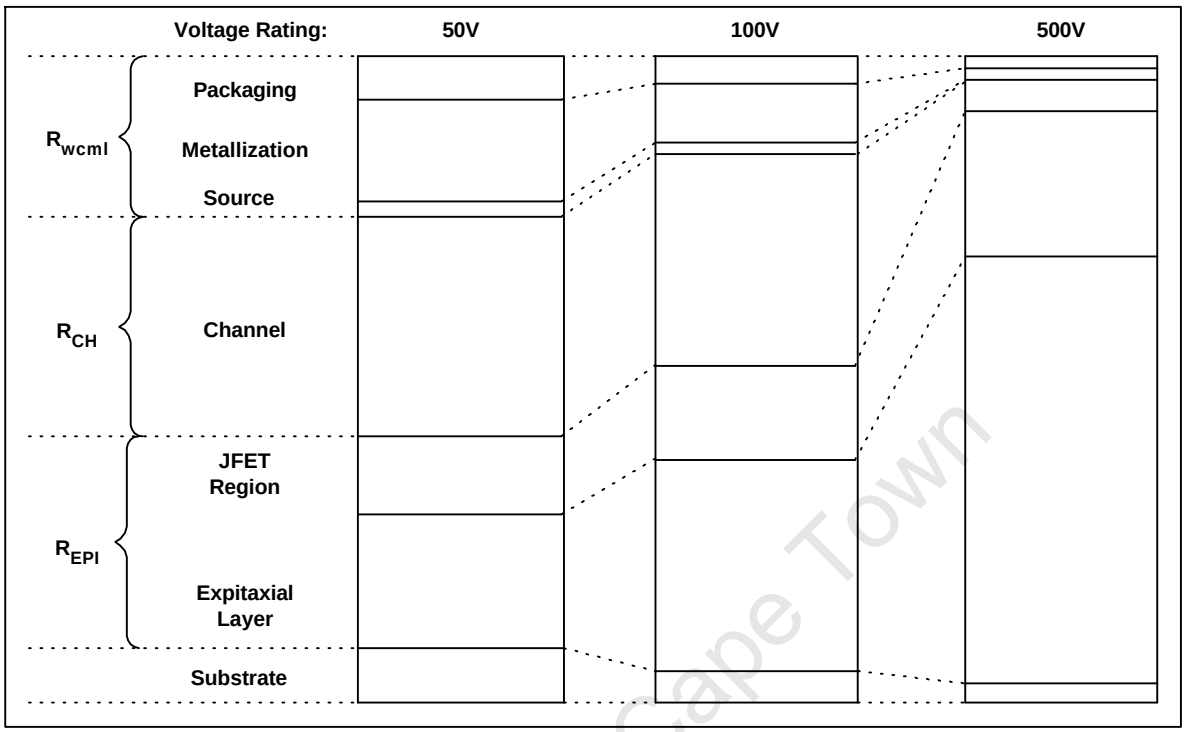


Figure 9. Relative Contributions to $R_{DS(on)}$ With Different Voltage Ratings.

The switching performance of a device is determined by the time required to establish voltage changes across capacitances. R_G is the distributed resistance of the gate and is approximately inversely proportional to active area. L_S and L_D are source and drain lead inductances and are around a few tens of nH. Typical values of input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances given in the data sheets are used by circuit designers as a starting point in determining circuit component values. The data sheet capacitances are defined in terms of the equivalent circuit capacitances as:

$C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted

$C_{rss} = C_{GD}$

$C_{oss} = C_{DS} + C_{GD}$

Gate-to-drain capacitance, C_{GD}, is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. C_{GD} is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances.

Figure 12 shows a typical switching time test circuit. Also shown are the components of the rise and fall times with reference to the V_{GS} and V_{DS} waveforms.

Turn-on delay, $t_{d(on)}$, is the time taken to charge the input capacitance of the device before drain current conduction can start. Similarly, turn-off delay, $t_{d(off)}$, is the time taken to discharge the capacitance after the after is switched off.

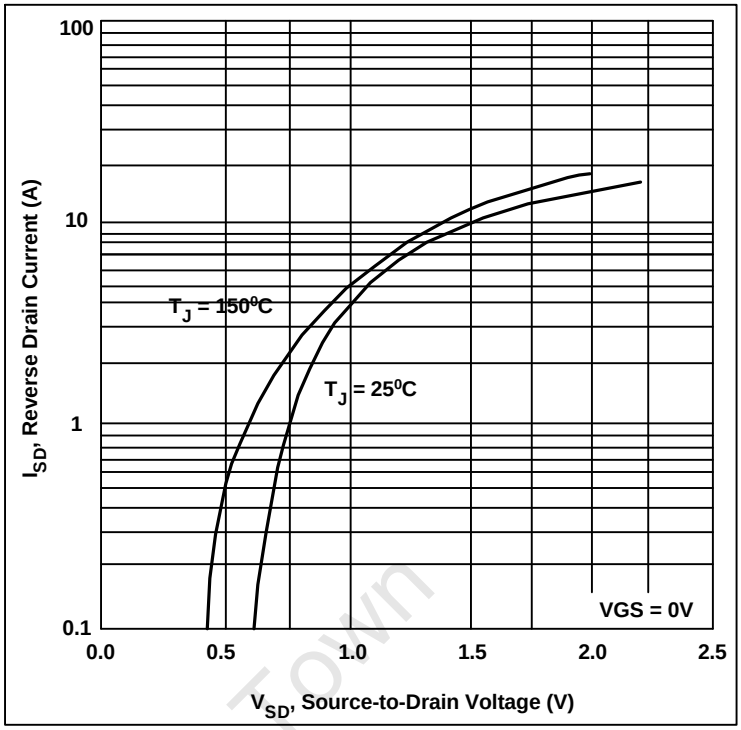


Figure 10. Typical Source-Drain (Body) Diode Forward Voltage Characteristics.

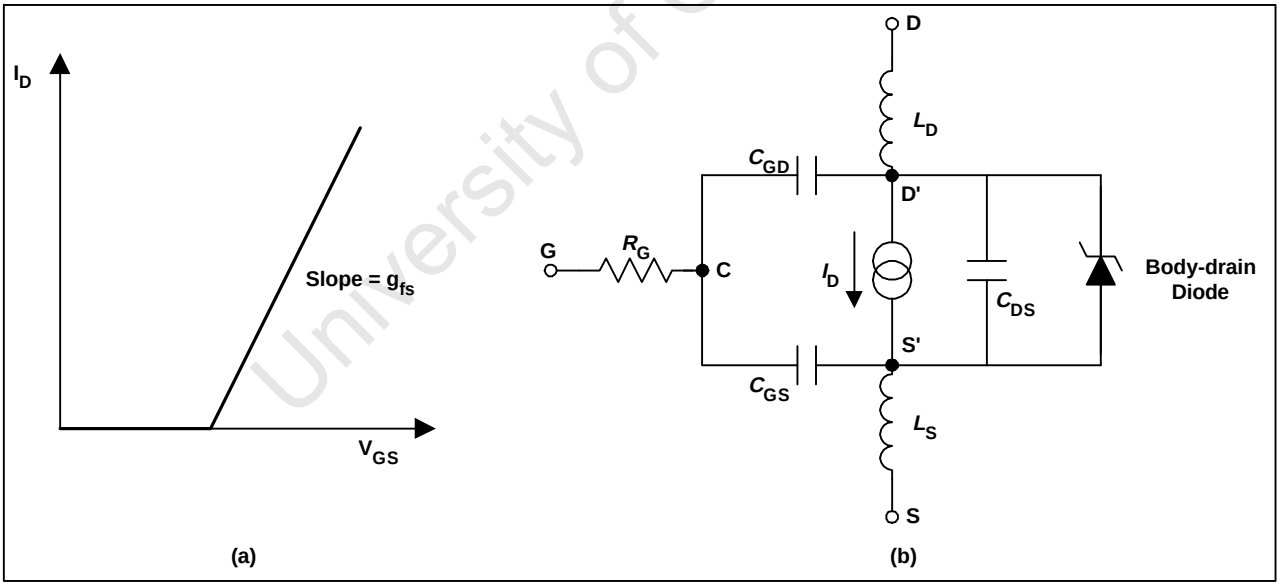


Figure 11. Power MOSFET (a) Transfer characteristics, (b) Equivalent Circuit Showing Components That Have Greatest Effect on Switching

GATE CHARGE

Although input capacitance values are useful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and transconductance make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Most manufacturers include both parameters on their data sheets. Figure 13 shows a typical gate charge waveform and the test circuit. When the gate is connected to the supply voltage, V_{GS} starts to increase until it reaches V_{th}, at which point the drain current starts to flow and the C_{GS} starts to charge. During the period t_1 to t_2, C_{GS} continues to charge, the gate voltage continues to rise and drain current rises proportionally. At time t_2, C_{GS} is completely charged and the drain current reaches the predetermined current I_D and stays constant while the drain voltage starts to fall. With reference to the equivalent circuit model of the MOSFET shown in Figure 13, it can be seen that with C_{GS} fully charged at t_2, V_{GS} becomes constant and the drive current starts to charge the Miller capacitance, C_{DG}. This continues until time t_3.

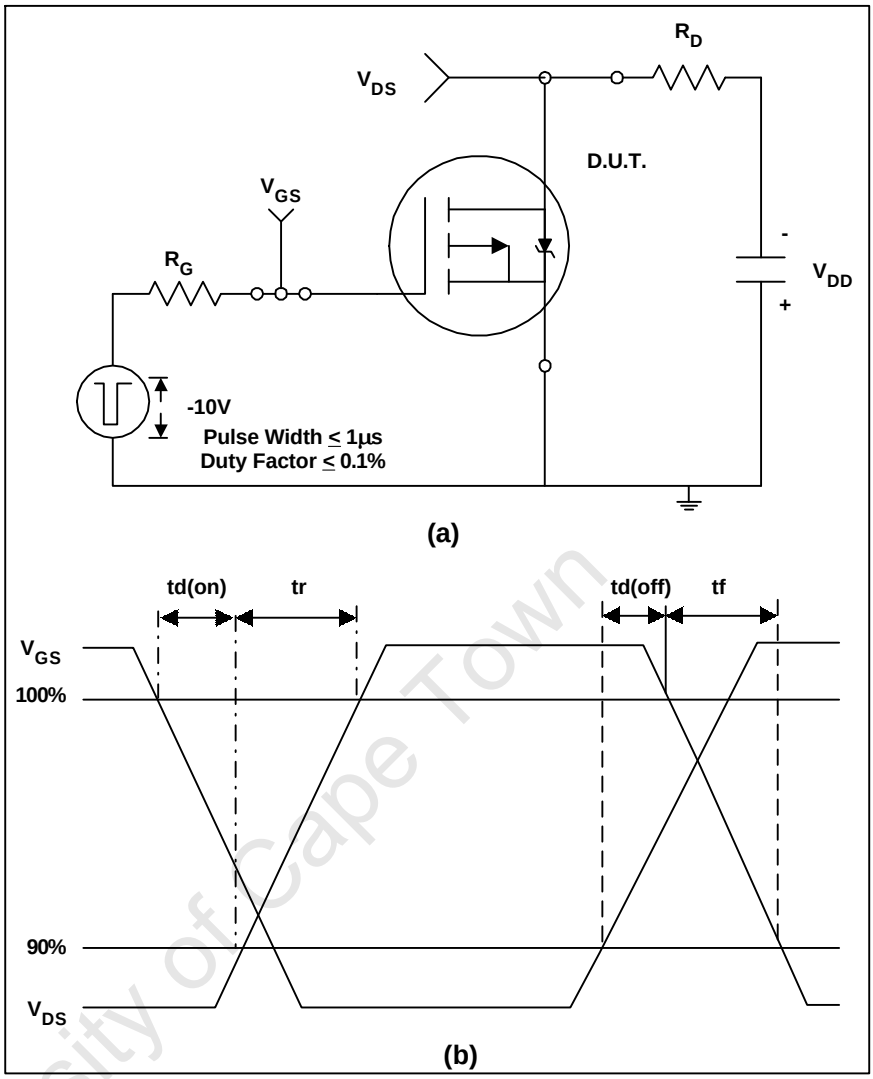


Figure 12. Switching Time Test (a) Circuit, (b) VGS and VDS Waveforms

Charge time for the Miller capacitance is larger than that for the gate to source capacitance C_{GS} due to the rapidly changing drain voltage between t_2 and t_3 (current = C dv/dt). Once both of the capacitances C_{GS} and C_{GD} are fully charged, gate voltage (V_{GS}) starts increasing again until it reaches the supply voltage at time t_4. The gate charge (Q_{GS} + Q_{GD}) corresponding to time t_3 is the bare minimum charge required to switch the device on. Good circuit design practice dictates the use of a higher gate voltage than the bare minimum required for switching and therefore the gate charge used in the calculations is Q_G corresponding to t_4.

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because Q = CV and I = C dv/dt, the Q = Time x current. For example, a device with a gate charge of 20nC can be turned on in 20µsec if 1ma is supplied to the gate or it can turn on in 20nsec if the gate current is increased to 1A. These simple calculations would not have been possible with input capacitance values.

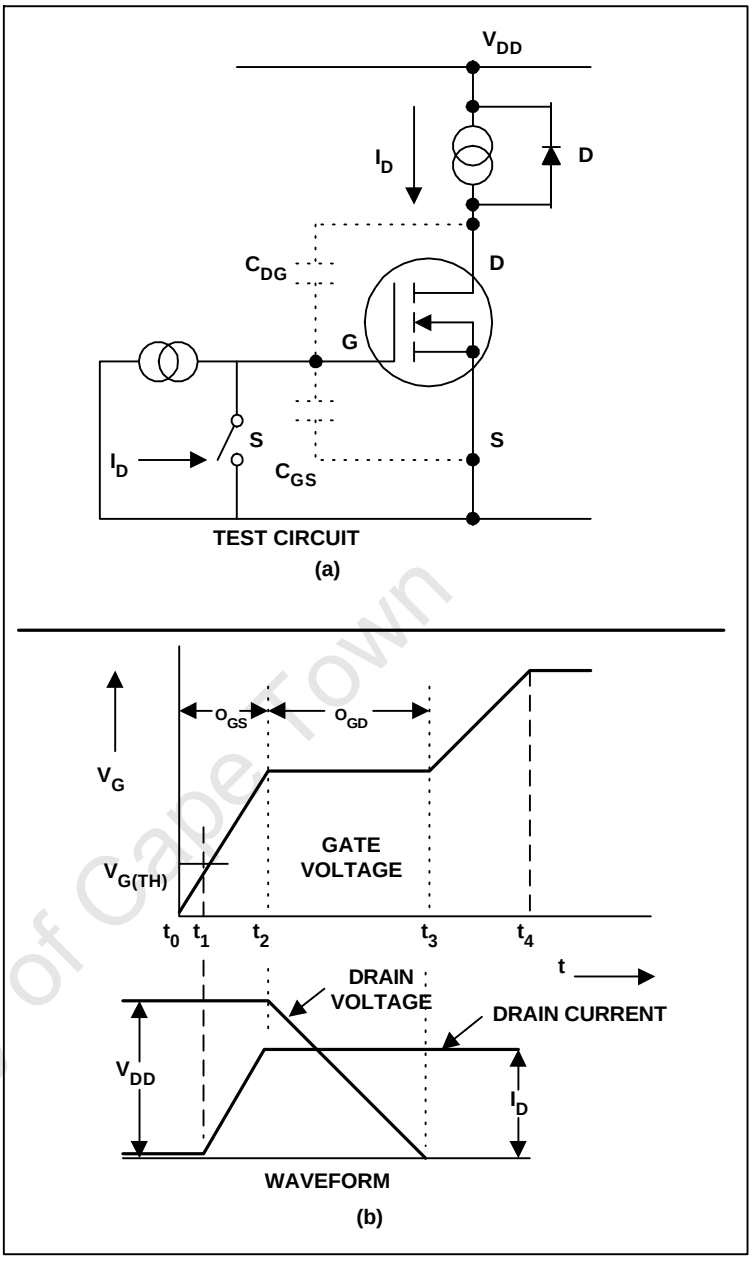


Figure 13. Gate Charge Test (a) Circuit, (b) Resulting Gate and Drain Waveforms.

dv/dt CAPABILITY

Peak diode recovery is defined as the maximum rate of rise of drain-source voltage allowed, i.e., dv/dt capability. If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into current conduction mode, and under certain conditions a catastrophic failure may occur. There are two possible mechanisms by which a dv/dt induced turn-on may take place. Figure 14 shows the equivalent circuit model of a power MOSFET, including the parasitic BJT. The first mechanism of dv/dt induced turn-on becomes active through the feedback action of the gate-drain capacitance, CGD. When a voltage ramp appears across the drain and source terminal of the device a current I_1 flows through the gate resistance, R_G, by means of the gate-drain capacitance, C_{GD}. R_G is the total gate resistance in the circuit and the voltage drop across it is given by:

$$V_{GS} = I_1 R_G = R_G C_{GD} \frac{dv}{dt} \qquad (3)$$

When the gate voltage V_{GS} exceeds the threshold voltage of the device V_{th}, the device is forced into conduction. The dv/dt capability for this mechanism is thus set by:

$$\frac{dv}{dt} = \frac{V_{th}}{R_G C_{GD}} \qquad (4)$$

It is clear that low V_{th} devices are more prone to dv/dt turn-on. The negative temperature coefficient of V_{th} is of special importance in applications where high temperature environments are present. Also gate circuit impedance has to be chooses carefully to avoid this effect.

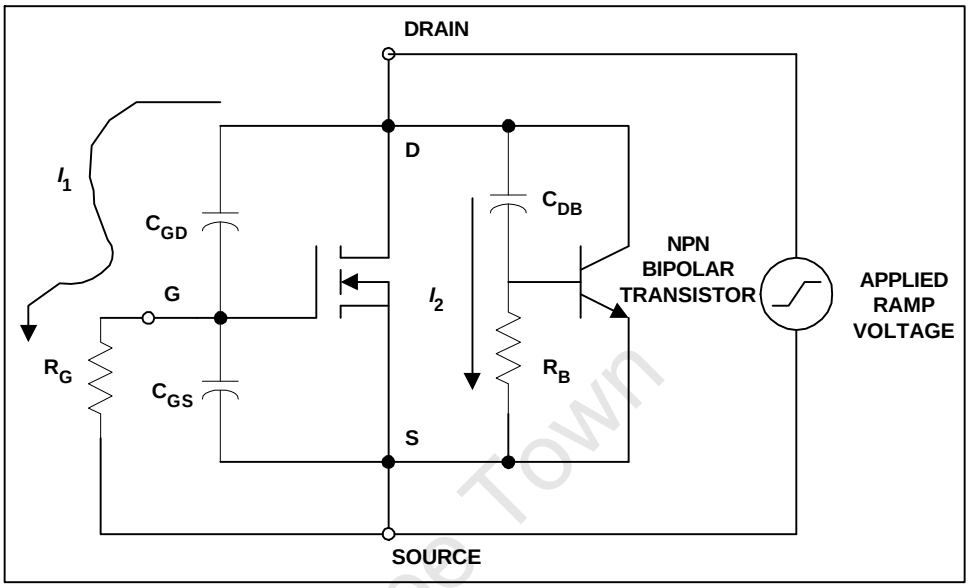


Figure 14. Equivalent Circuit of Power MOSFET Showing Two Possible Mechanisms for dv/dt Induced Turn-on.

The second mechanism for the dv/dt turn-on in MOSFETs is through the parasitic BJT as shown in Figure 15. The capacitance associated with the depletion region of the body diode extending into the drift region is denoted as C_{DB} and appears between the base of the BJT and the drain of the MOSFET. This capacitance gives rise to a current I_2 to flow through the base resistance R_B when a voltage ramp appears across the drain-source terminals. With analogy to the first mechanism, the dv/dt capability of this mechanism is:

$$\frac{dv}{dt} = \frac{V_{BE}}{R_B C_{DB}} \qquad (5)$$

If the voltage that develops across R_B is greater than about 0.7V, then the base-emitter junction is forward-biased and the parasitic BJT is turned on. Under the conditions of high (dv/dt) and large values of R_B, the breakdown voltage of the MOSFET will be limited to that of the open-base breakdown voltage of the BJT. If the applied drain voltage is greater than the open-base breakdown voltage, then the MOSFET will enter avalanche and may be destroyed if the current is not limited externally.

Increasing (dv/dt) capability therefore requires reducing the base resistance R_B by increasing the body region doping and reducing the distance current I_2 has to flow laterally before it is collected by the source metallization. As in the first mode, the BJT related dv/dt capability becomes worse at higher temperatures because R_B increases and V_{BE} decreases with increasing temperature.

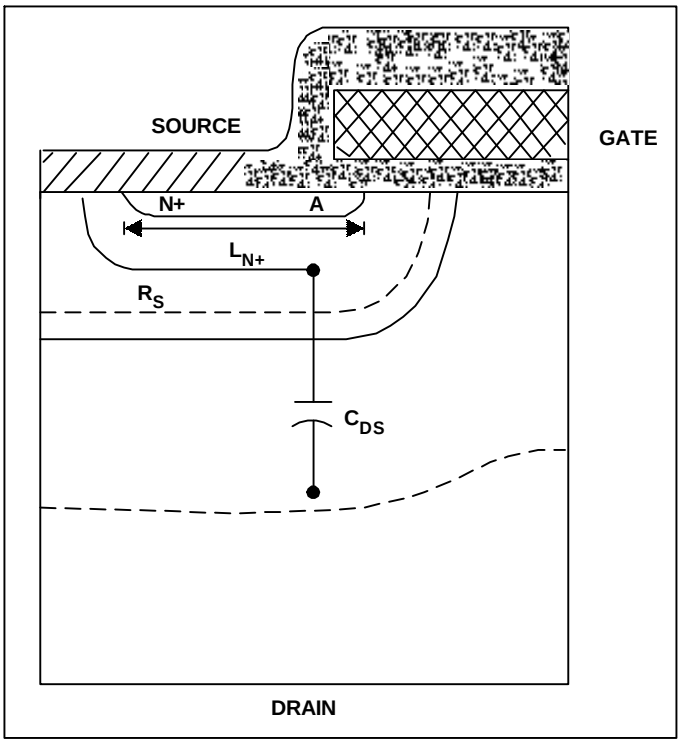
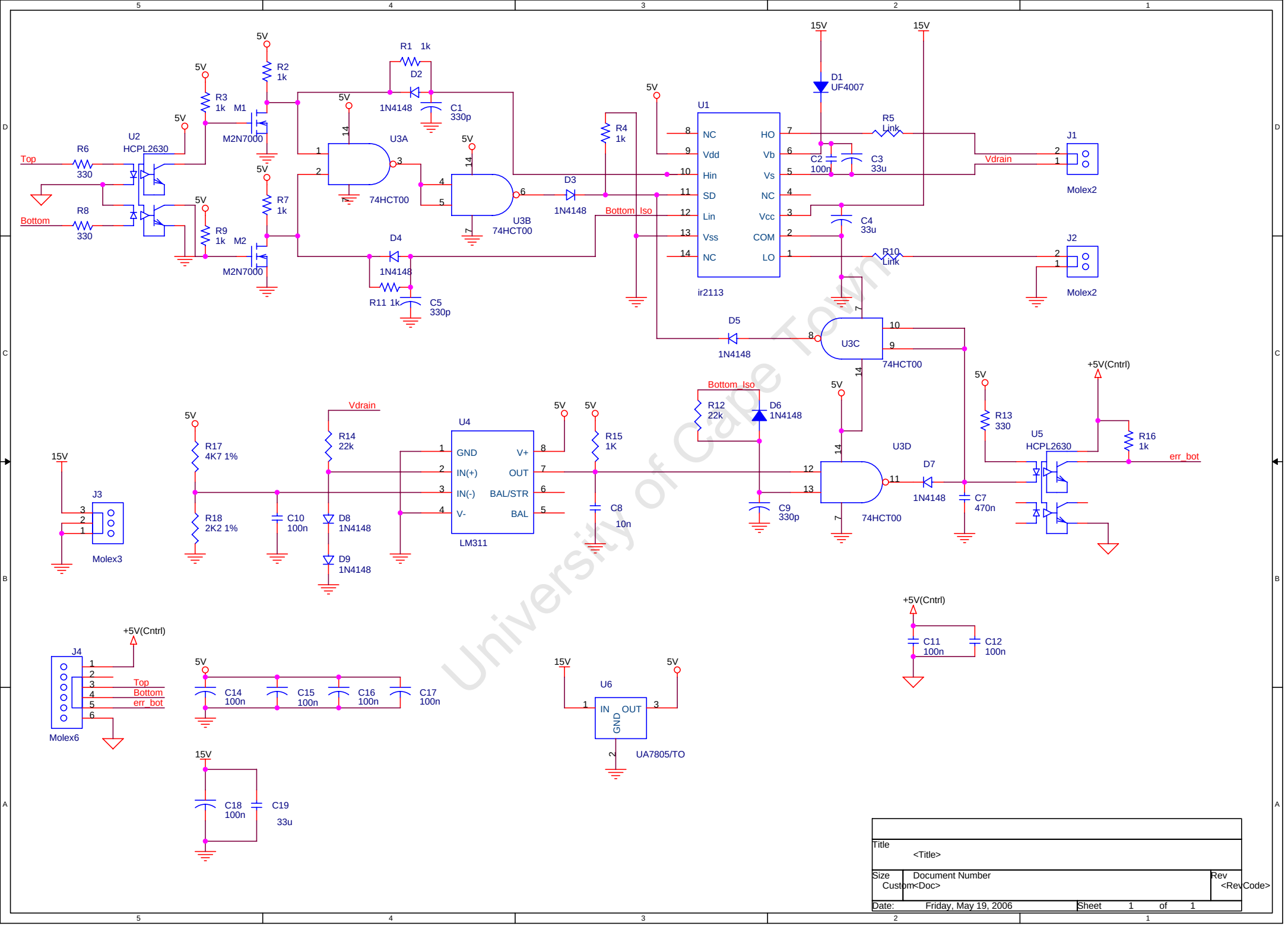


Figure 15. Physical Origin of the Parasitic BJT Components That May Cause dv/dt Induced Turn-on

References:

"HEXFET Power MOSFET Designer's Manual - Application Notes and Reliability Data," International Rectifier
"Modern Power Devices," B. Jayant Baliga
"Physics of Semiconductor Devices," S. M. Sze
"Power FETs and Their Applications," Edwin S. Oxner
"Power MOSFETs - Theory and Applications," Duncan A. Grant and John Gower



UNIVERSITY OF CAPE TOWN

DEPARTMENT OF ELECTRICAL ENGINEERING

Technical report on:

POWER TRANSFORMER MAGNETIC MEASUREMENT UNDER ALTERNATING CURRENT

By Emma-Françoise Isumbingabo

January, 2008

1. Introduction.

In Power Transformer Design, ideal model may be well suited for rough approximations; however, the non-ideal parameters are needed for careful Power Transformer circuit designs. Knowing the non-ideal parameters allows the engineer to optimize a design using equations.

If all dimensions and material properties of a transformer are known, the non-ideal parameters can be directly calculated. However, this is usually not the case, and a simple technique for obtaining the parameters can be used. In this technical report, method for determining the parameters of the equivalent circuit model using two simple transformer tests (the open circuit and short circuit tests) is described. Expressions for calculating the parameters are derived in terms of laboratory measurements. The procedure is performed in the laboratory for 6KVA Power Transformer. The results obtained by experimental tests are compared to those obtained by simulation using SimPower Systems Block-set within the MATLAB Software.

Objectives of the section

The objectives of this laboratory work are as follows:

- To determine the Non- Ideal parameters of a 6KVA Power Transformer Equivalent Circuit using two Transformer Tests Methods which are the No-Load Test and the Short-Circuit Test.
- To compare the obtained results with those obtained by Simulation using SimPower Systems software within MATLAB

2. Background of Power Transformer

2.1 Basic principles of Power Transformer

The Transformer is based on two principles:

- An electric current produces a magnetic field (electromagnetism)

- A changing magnetic field within a coil of wire induces a voltage across the ends of the coil (electromagnetic induction). By changing the current in the primary coil, one changes the strength of its magnetic field; since the

secondary coil is wrapped around the same magnetic field, a voltage is induced across the secondary coils.

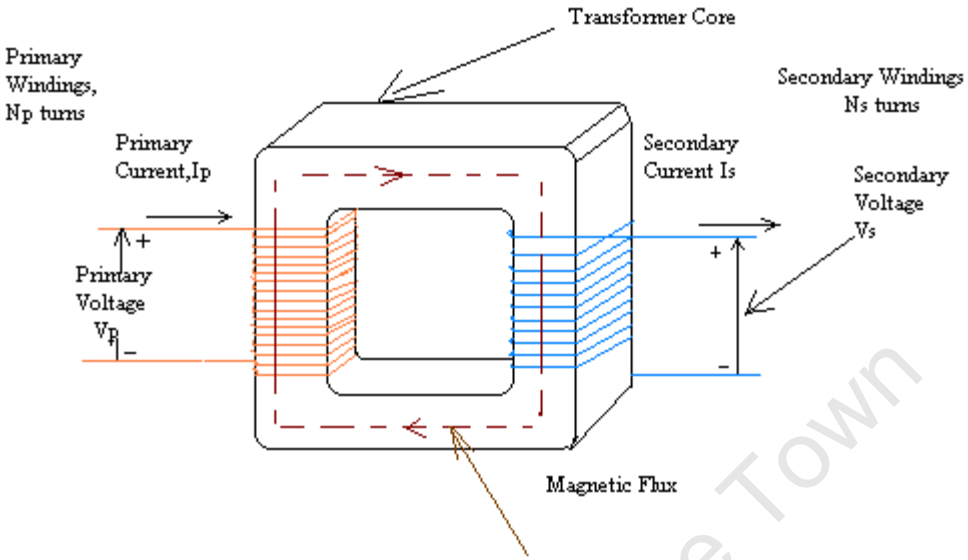


Figure 2.1: An Ideal Step-Down Transformer Showing Magnetic Flux in the Core

A current passing through the primary coil creates a magnetic field. The primary and secondary coils are wrapped around a core of very high magnetic permeability, such as iron; this ensures that most of the magnetic field lines produced by the primary current are within the iron and pass through the secondary coil as well as the primary coil.

2.2 Induction law

The voltage induced across the secondary coil may be calculated from Faraday's law of induction, which states that

$$V_s = N_s \frac{d\Phi}{dt} \qquad (1)$$

where V_s is the instantaneous voltage, N_s is the number of turns in the secondary coil and Φ equals the total magnetic flux through one turn of the coil. If the turns of the coil are oriented perpendicular to the magnetic field lines, the flux is the product of the magnetic field strength *B* and the area *A* through which it cuts. The area is constant, being equal to the cross-sectional area of the transformer core, whereas the magnetic field varies with time according to the excitation of the primary.

Since the same magnetic flux passes through both the primary and secondary coils in an ideal transformer, the instantaneous voltage across the primary winding equals

$$V_p = N_p \frac{d\Phi}{dt} \qquad (2)$$

Taking the ratio of the two equations for V_s and V_p gives the basic equation for stepping up or stepping down the voltage

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} \qquad (3)$$

2.4 Transformer Equivalent Circuit.

The quantities to be modelled in a transformer are:

(i) The transformation ratio of the transformer
(ii) The copper losses in the windings.
(iii) Useful and leakage fluxes.
(iv) Iron losses in the core.

2.4.1 The Ideal transformer

Models of an ideal Transformer typically assume a core of negligible reluctance with two windings of zero resistance. When a voltage is applied to the primary winding, a small current flows, driving flux around the magnetic circuit of the core. The current required to create the flux is termed the *magnetizing current*; since the ideal core has been assumed to have near-zero reluctance, the magnetizing current is negligible, although a presence is still required to create the magnetic field.

The changing magnetic field induces an electromotive force (EMF) across each winding. Since the ideal windings have no impedance, they have no associated voltage drop, and so the voltages V_P and V_S measured at the terminals of the Transformer, are equal to the corresponding EMFs. The primary EMF, acting as it does in opposition to the primary voltage, is sometimes termed the "back EMF". This is due to Lenz's law which states that the induction of EMF would always be such that it will oppose development of any such change in magnetic field.

2.4.2 Copper Losses

Copper Loss is the term often given to heat produced by electrical currents in the conductors of Transformer windings, or other electrical devices. Copper losses are an undesirable transfer of energy, which result from induced currents in adjacent components. The term is applied regardless of whether the windings are made of copper or another conductor, such as aluminium. Hence the term winding loss is often preferred. A related term, load loss closely related but not identical, since an unloaded Transformer will have some winding loss.

Copper losses result from Joule heating and so are also referred to as "I squared R losses", in deference to Joule's First Law. This states that the energy or power lost each second increases as the square of the current through the windings and is proportional to the electrical resistance of the conductors.

$$Copper Losses = I^2.R \qquad (4)$$

where I is the current flowing in the conductor and R the resistance of the conductor. With I in amperes and R in ohms, the calculated power loss is given in watts.

These winding resistances can be represented in the equivalent circuit by resistances included in series with the ideal Transformer.

2.4.3 Useful or Main Flux

In a transformer the flux which links both primary and secondary windings is called useful or main flux. For sinusoidal operation of the transformer, instantaneous values are considered and the main flux may be written as follows

$$\phi = \Phi \sin wt \qquad (5)$$

Then the induced e.m.f is,

$$e_1 = N_1 \frac{d\phi}{dt} = wN_1\Phi \cos wt \qquad (6)$$

Thus the flux is proportional to the e.m.f. and lags it by 90^0.

As written above, the current producing this Useful Flux is called Magnetizing Current, and it can be designed by I_m Current. This magnetizing current being in phase with the flux, it lags the induced e.m.f by 90^0

The effect of this magnetizing current can be included in the equivalent circuit by connecting an inductance, called the magnetizing inductance in parallel with the primary coil of the ideal Transformer. The use of an inductance is due to the fact that the voltage across an inductor is 90^0 leading the current through it. And it is connected in parallel because it is directly proportional to the e.m.f.

2.4.4 Leakage flux

The Ideal Transformer model assumes that all flux generated by the primary windings links all the turns of every windings, including itself. In practice, some flux traverses paths that take it outside the windings. Such flux is termed *leakage flux*, and manifests itself as self-inductance in series with the mutually coupled transformer windings. Leakage results in energy being alternately stored in and discharged from the magnetic fields with each cycle of the power supply. It is not itself directly a source of power loss, but results in poorer voltage regulation, causing the secondary voltage to fail to be directly proportional to the primary, particularly under heavy load.

The effect of the leakage flux can be included in the equivalent circuit by including an inductance in series with each coil of the Ideal Transformer.

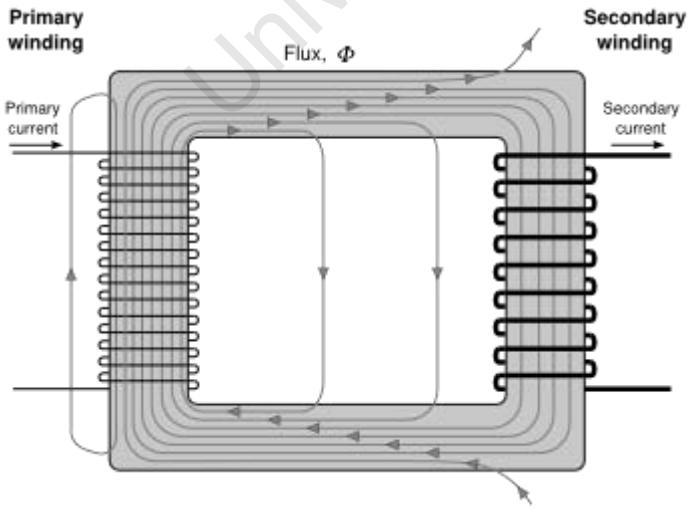


Figure 2.2: Flux Leakage in a Two-Winding Transformer

2.4.5 Iron Losses

Core Loss (or iron loss) is a form of energy loss that occurs in Electrical Transformers and other inductors. The loss is due to a variety of mechanisms related to the fluctuating magnetic field, such as eddy currents and hysteresis. Most of the energy is released as heat, although some may appear as sound. For a particular transformer iron losses are constant for a fixed value of voltage; therefore they can be represented in the equivalent circuit by a resistance connected in parallel with the primary coil of the ideal transformer.

The equivalent circuit of a practical Transformer is obtained by combining the effects above, and is show in the figure below

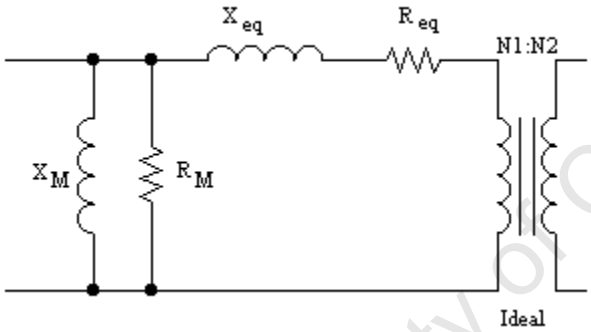


Figure 2.3: Transformer Equivalent Circuit

2.5 Referred values

In order to simplify the Transformer equivalent circuit, the Ideal Transformer is eliminated from it by referring the secondary parameters on the primary side.

The secondary current I_2 is replaced by the referred current I'_2 flowing in the primary side of the equivalent circuit, where

$$I'_2 = \frac{N_2}{N_1} I_2 \qquad (7)$$

The secondary voltage V_2 is replaced by the referred voltage V_2''

Where

$$V'_2 = \frac{N_1}{N_2} V_2 \qquad (8)$$

The secondary winding resistance R_2 is replaced by the referred secondary resistance R'_2 connected in the primary side of the equivalent circuit. The value of R'_2 is such that the power dissipated in R''_2 when the referred current I'_2 flows through it is equal to the power dissipated in R_2 when the current I_2 Flows through it

$$\text{(illegible)}_2 R'_2 = I_2^2 R_2 \quad (9)$$

$$R'_2 = \left[\frac{N_1}{N_2}\right]^2 R_2 \quad (10)$$

$$X'_{l2} = \left[\frac{N_1}{N_2}\right] X_{l2} \quad (11)$$

The equation (11) shows the referred value X'_{l2} which replace the secondary leakage inductance X_{l2}.

The resulting equivalent circuit is shown below:

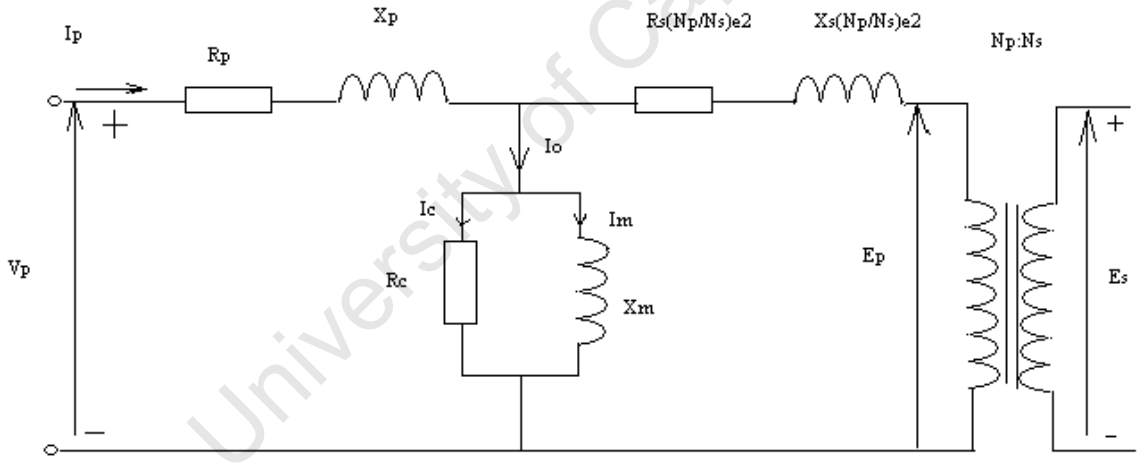


Figure 2.4: Transformer Equivalent Circuit

3. Power transformer tests.

3.1 Open circuit test.

For this test the secondary winding of the transformer is open, and the primary winding is fed by the full rated voltage, the measurements apparatus are such that the reading of primary voltage, current and power are taken.

Let these readings be $V_0, I_0, and \ P_0$ respectively.
Assume that the secondary current $I_2 = 0$ and also that in a practical transformer, the core resistance R_c and the magnetizing inductance X_m are very much greater than the primary series resistance R_1 and the primary series inductance X_{l1}. R_C and X_m are given by

$$R_c = \frac{V_0}{I_c} \tag{12}$$

and

$$X_m = \frac{V_0}{I_m} \tag{13}$$

Where $I_c = I_0 \cos\theta$ and $I_m = I_0 \sin\theta$; θ is the open circuit power factor angle at the primary rated voltage.
Consider

$$\cos\theta = \frac{P_0}{V_0 I_0} \tag{14}$$

hence current $I_c = \frac{P_0}{V_0}$ (15)

Therefore $R_c = \frac{{V_0}^2}{P_0}$ (16)

and $X_m = \frac{{V_0}^2}{Q_0}$ (17)

Where $Q_0 = P_0 \tan\theta$ (18)

3.1.1. Sample calculations

3.1.1.1. Description of the experiment and setup

A 6 KVA, 9:1 Transformer was tested in the laboratory to determine its equivalent circuit parameters. The test was conducted under an assumed sinusoidal main supply (voltage source); the figure below shows the supply voltage waveform, and its total harmonic distortion (THD)

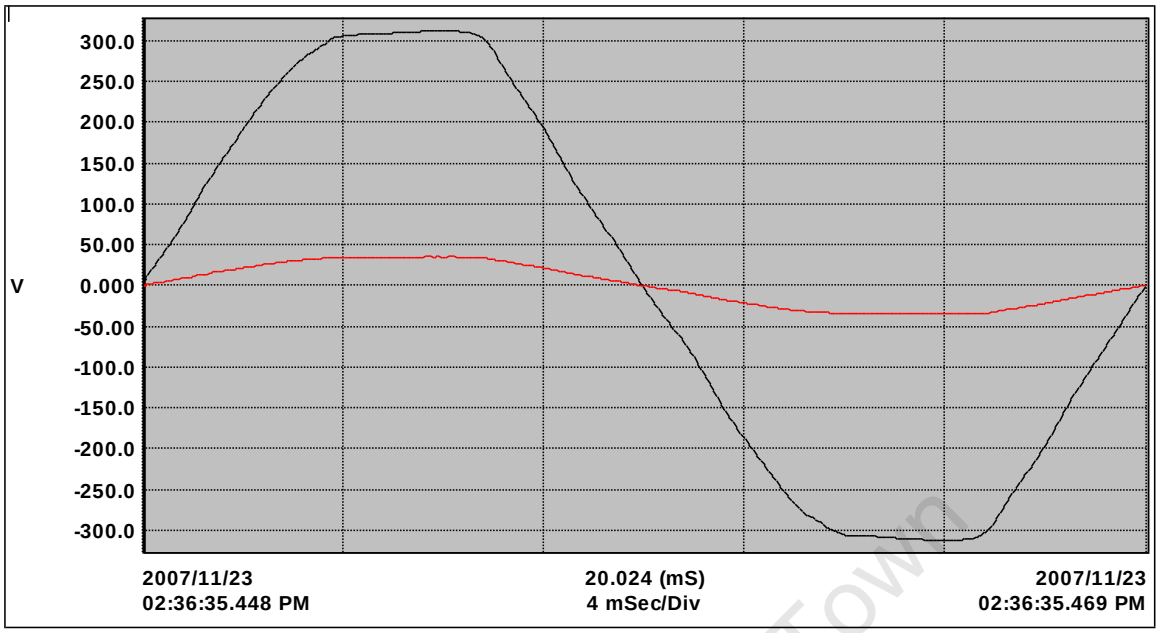


Figure 3.1: Supply Voltage Waveform

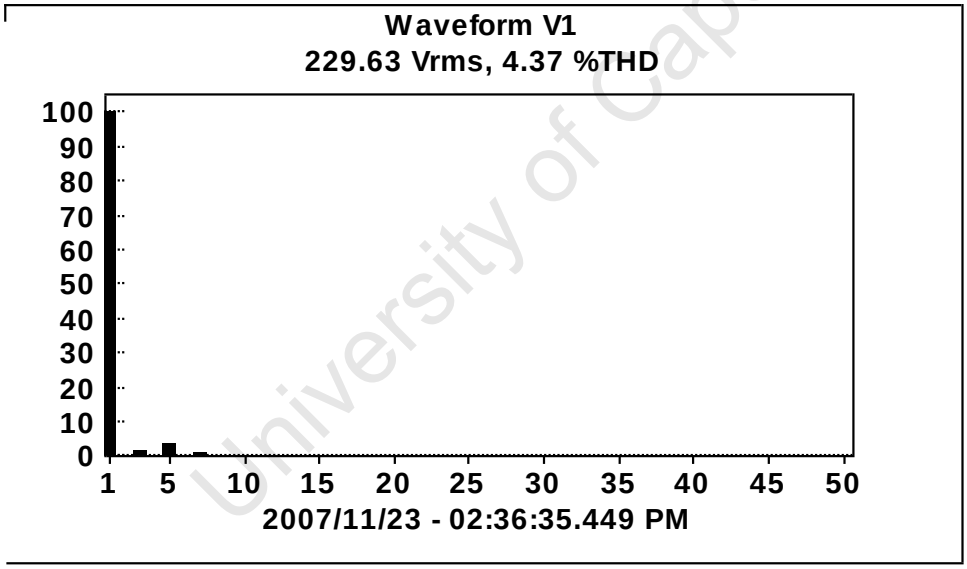


Figure 3.2: Input Voltage Total Harmonics Distortion THD

The crest factor being 1.39, the voltage is assumed to be sinusoidal. For making the open circuit test the wiring diagram was as follows

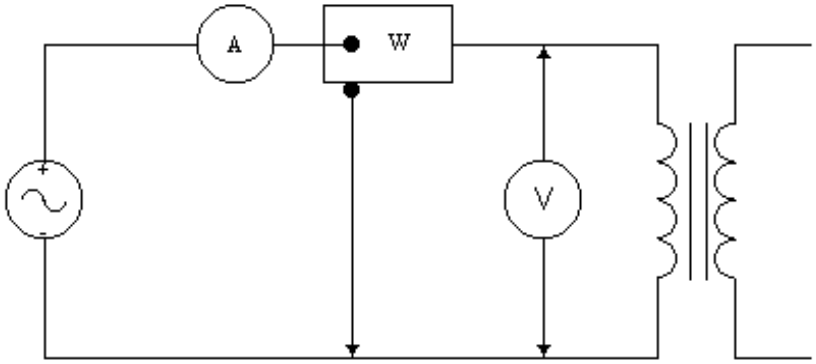


Figure 3.3: Open Circuit test Wiring Diagram

With the Transformer secondary open, the primary voltage was increased slowly from zero to the nominal value.
A digital multimeter was used to measure the open circuit current, a power analyzer was used to capture the primary current and voltage waveforms, the power analyzer was used as well as a wattmeter to measure the open circuit power. The power measured was the power dissipated in the magnetizing resistance R_m ,and it is defined as the core losses.

The figure below shows the magnetizing current under open circuit test.

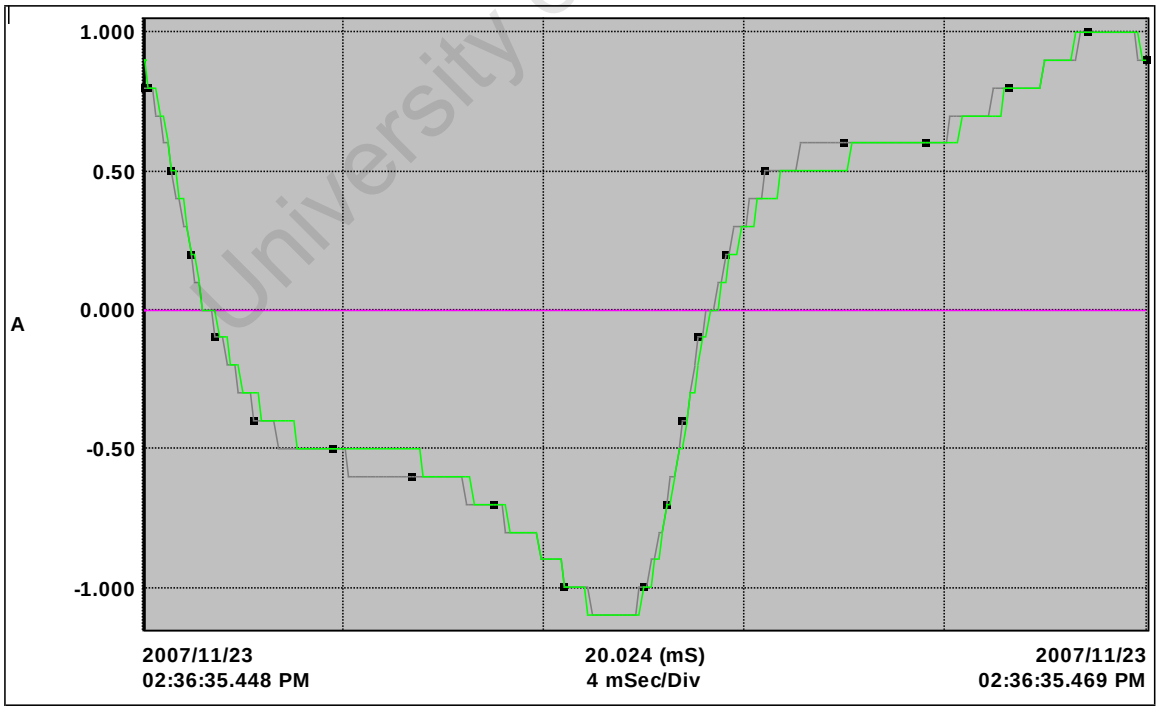


Figure 3.4: 6KVA Power Transformer Magnetizing Current.

The magnetizing current is much distorted; hence its THD is very high as shows in the figure below

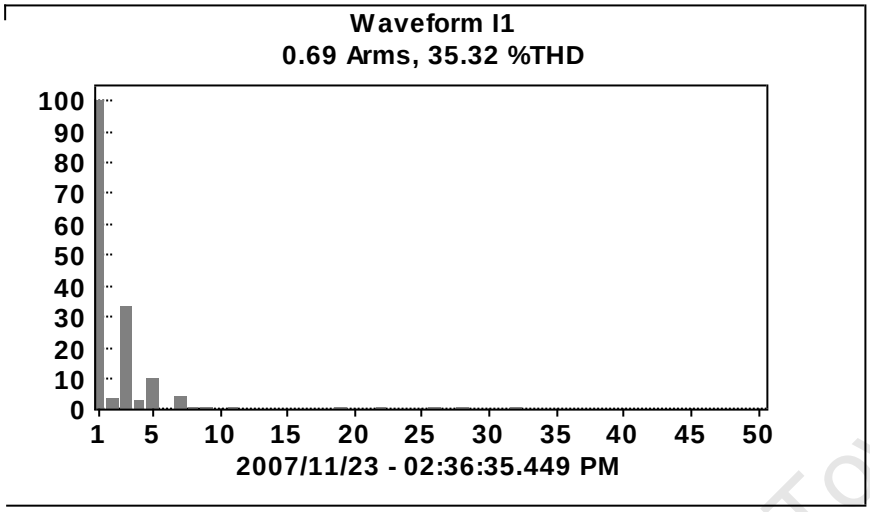


Figure 3.5: 6KVA Power Transformer Magnetizing Current THD

3.1.1.2 Presentation of Results

For open circuit measurements The no-load measurements are $V_1 = 25.9VAC$, $I_1 = 0.7A$, $P_1 = 15.203W$, $Q_1 = 9.87VAR$.

The parallel parameters of the transformer are calculated using Equations (19) and (20)

$$Rm = \frac{25.9^2}{15.203} \tag{19}$$

$$Rm = 44\Omega$$

$$Xm = \frac{25.9^2}{9.87} \tag{20}$$

$$Xm = 68\Omega$$

3.2 Short circuit test.

For this test the secondary winding of the transformer is short circuited, the primary winding is supplied from a variable voltage source, and measurements are taken for current, voltage, and power in the primary circuit.

The primary voltage is slowly increased until the rated (full load) current flows in the windings. Let voltage reading be $V_{sc,}$ current reading be I_{sc} and

power reading be P_{sc}, according to the equivalent circuit shown in figure (3), when the secondary is short circuited,

$$Z_e = \frac{V_{sc}}{I_{sc}}, R_e = \frac{P_{sc}}{I^2{}_{sc}} \tag{21}$$

$$X_e = \sqrt{Z^2{}_e} - R^2{}_e \tag{22}$$

3.2.1 Sample calculations

3.2.1.1. Description of the experiment and setup

The short circuit wiring diagram is shown in the figure (10). With the secondary terminals shorted, the primary voltage was increased from zero until the rated current was reached in the primary. Then primary current, primary voltage, primary power and the secondary current were measured. At this point the primary voltage is much less than the rated value.
Figure (10) shows the short circuit wiring diagram.

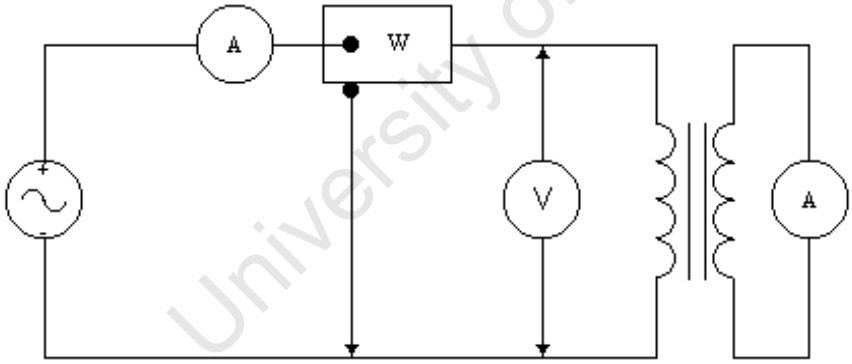


Figure 3.6: Transformer Short-Circuit test Wiring Diagram

3.2.1.2 Presentation of results

The short circuit measurements results in $V_1cc = 10.1V$,
$P_1cc = 259.7W$, $I_1cc = 26.5A$, $\tan\theta_{cc} = 0.249$, $\cos\theta_{cc} = 0.97$
The series parameters of the 6KVA transformer equivalent circuit are calculated using Equations (23) and (24)

$$\mathrm{Re}\,q = \frac{259.7}{26.5^2} \tag{23}$$
$$\mathrm{Re}\,q = 0.37\Omega$$
$$Zeq = \frac{V_1cc}{I_1cc}$$
$$Zeq = \frac{10.1}{26.5}$$
$$Zeq = 0.38\Omega \tag{24}$$
$$Xeq = \sqrt{Zeq^2} - \mathrm{Re}\,q$$
$$Xeq = 0.09\Omega$$

4. Voltage Regulation

It has been observed during the laboratory experiment that the terminal voltage of the transformer drops with respect to the increase in current drawn from it.
The voltage at load is different from that measured at no-load.
It is that difference which is known as REGULATION, expressed in % and defined as:

$$\%\,\mathrm{Re}\,gulation = \frac{V_{NOLOAD} - V_{load}}{V_{noload}} * 100 \tag{25}$$

5. Transformer Efficiency

The general definition of efficiency is the ratio of the power output to the power input; the difference is termed power loss.
In the case of a transformer, loss consists of two components:

- Copper loss
- Iron loss

Therefore the efficiency of the transformer is given by:

$$\eta = \frac{output}{input} = \frac{output}{output + copperlosses + F_e losses} \tag{26}$$

$$\eta = \frac{V_2 I_2 \cos\theta_2}{V_2 I_2 \cos\theta_2 + I_2{}^2 R_E + F_E} \tag{27}$$

Where F_e represent the constant iron losses

Assume the power factor to be constant,

let divide both the numerator and denominator by I_2

$$\eta = \frac{V_2 \cos\theta_2}{V_2 \cos\theta_2 + I_2 R_e + \frac{F_e}{I_2}} \tag{28}$$

Differentiating the denominator with respect to I_2, and equating to zero gives,

$$\frac{d(den)}{dI_2} = R_e - \frac{F_e}{I_2{}^2} = 0 \tag{29}$$

$$I_2{}^2 R_e = F_e \tag{30}$$

Equation 30 shows the condition for maximum efficiency of the transformer. Where $I_2{}^2 R_e$ represents the copper losses and F_e represents the constant iron losses.

5.1. Sample Calculations of Efficiency

For this test, a variable resistance was connected on the output terminals of the secondary winding.

At any variation of the resistance, readings of primary active power and secondary active power were taken.

Efficiency was calculated. Results are presented in the table below:

Table 1: Transformer efficiency

Test No	$I_2(A)$	*Power input* $P_1(W)$	*Power output* $P_2(W)$	*Efficiency* $\eta(\%)$
1	0.3	74.646	68.94	92
2	8.8	2,005	1,936	96.56
3	13.1	2,982.14	2,867.59	96.1
4	16.5	3,655.818	3,499.65	95.72
5	20.6	4,576.017	4,346.6	94.98
6	23.5	5,071.58	4,801.05	94.66
7	27.6	5,983.382	5,630.4	94.1

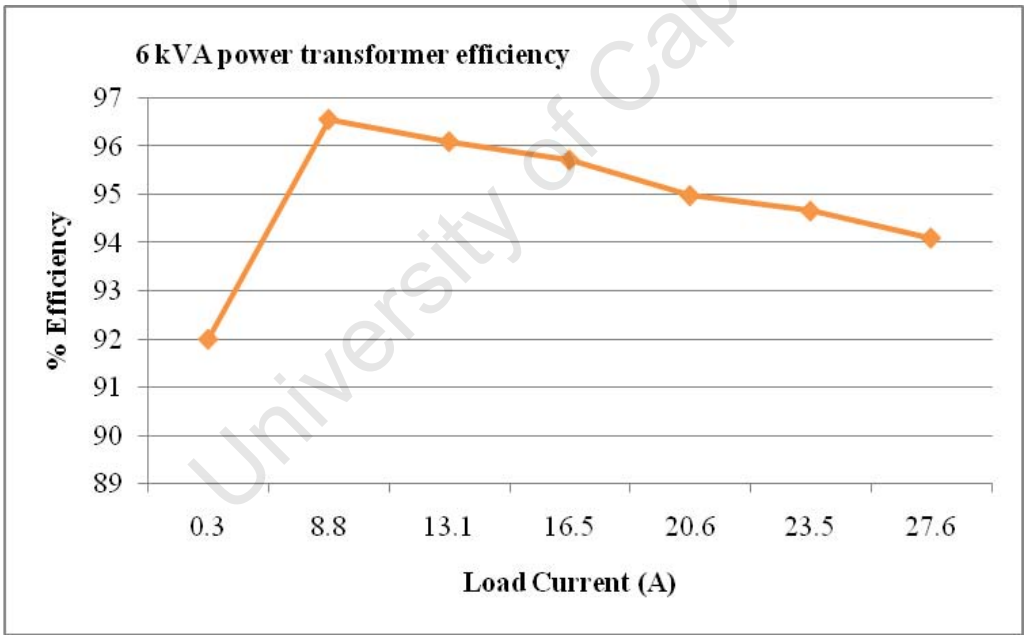
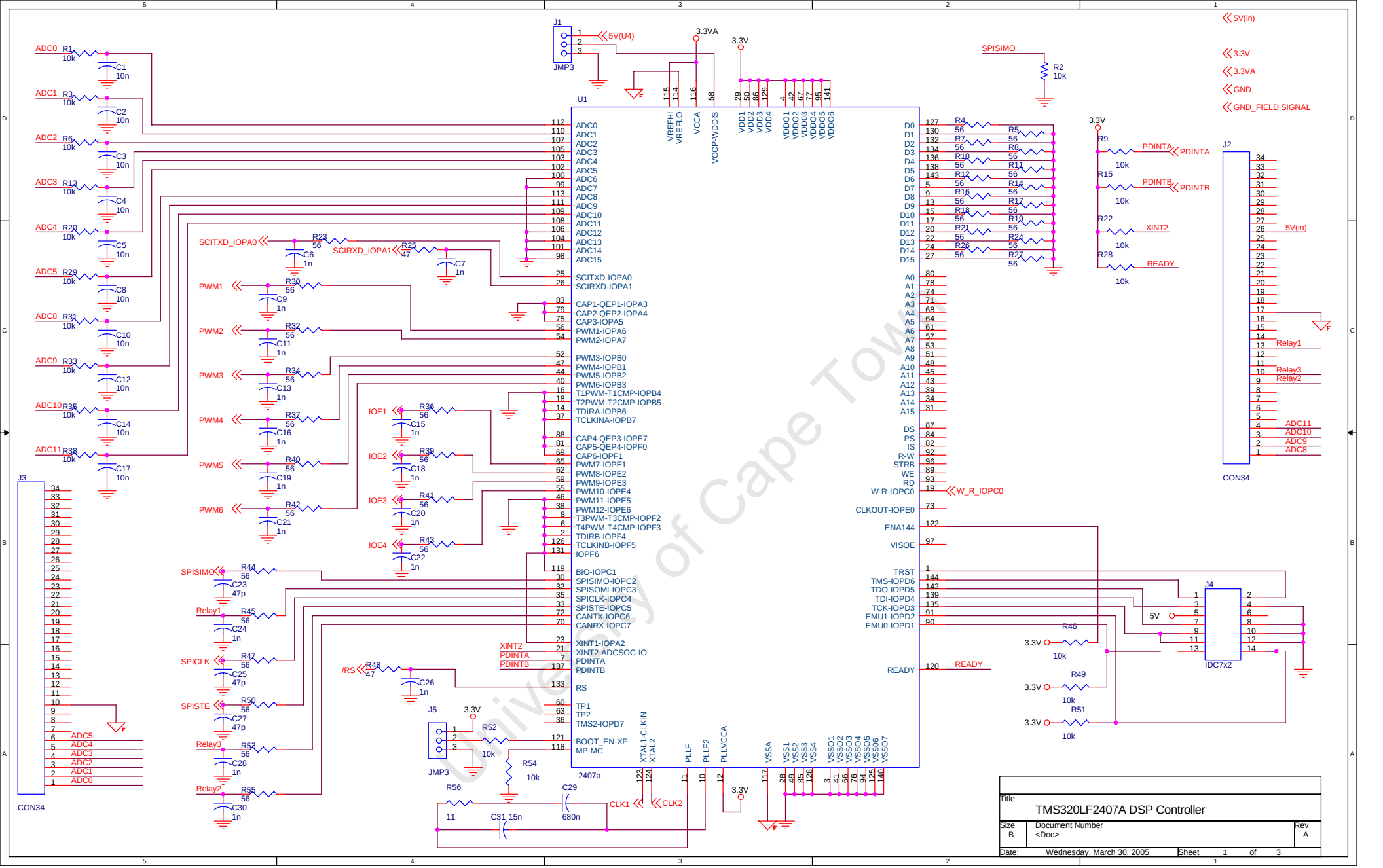
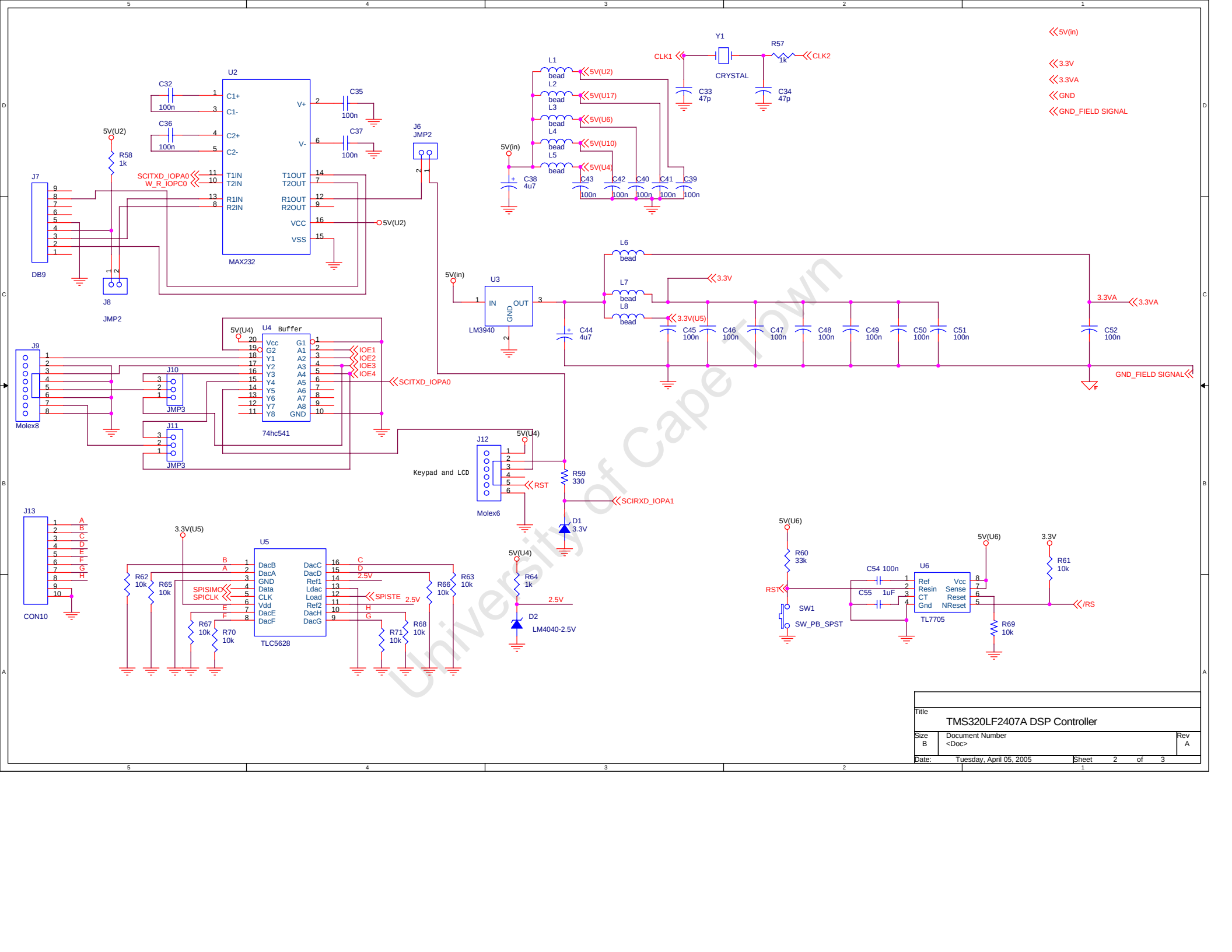


Figure 5.1: $\eta = f(I_2)$ **curve**





Title	TMS320LF2407A DSP Controller	
Size B	Document Number <Doc>	Rev A
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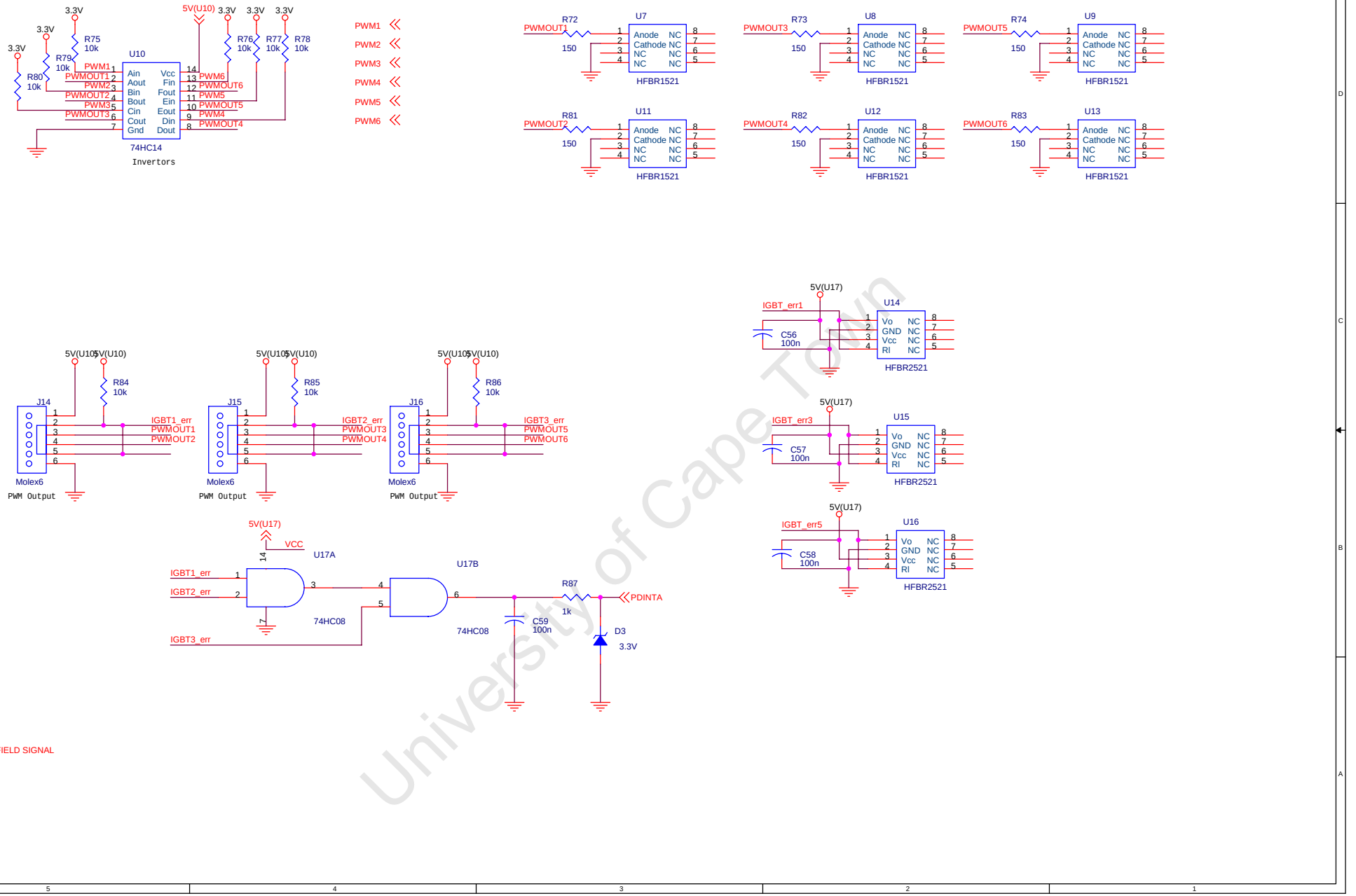

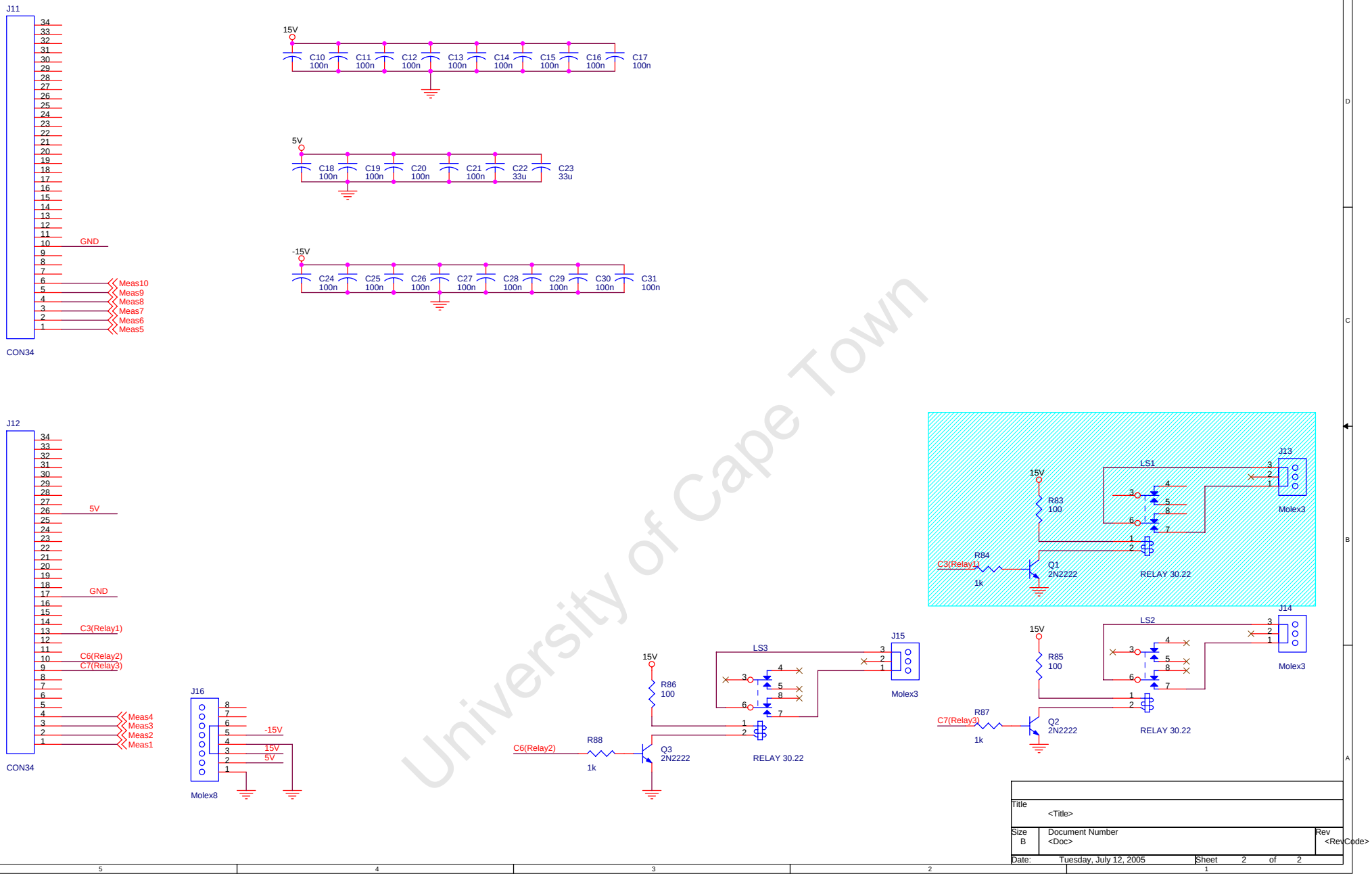
J11
CON34
GND
Meas10
Meas9
Meas8
Meas7
Meas6
Meas5
15V
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
5V
C18 100n
C19 100n
C20 100n
C21 100n
C22 33u
C23 33u
-15V
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
C29 100n
C30 100n
C31 100n
J12
CON34
5V
GND
C3(Relay1)
C6(Relay2)
C7(Relay3)
Meas4
Meas3
Meas2
Meas1
J16
Molex8
-15V
15V
5V
R86 100
R88 1k
Q3 2N2222
LS3
RELAY 30.22
J15
Molex3
R83 100
R84 1k
Q1 2N2222
LS1
RELAY 30.22
J13
Molex3
R85 100
R87 1k
Q2 2N2222
LS2
RELAY 30.22
J14
Molex3
University of Cape Town
Title
<Title>
Size B
Document Number
<Doc>
Rev
<RevCode>
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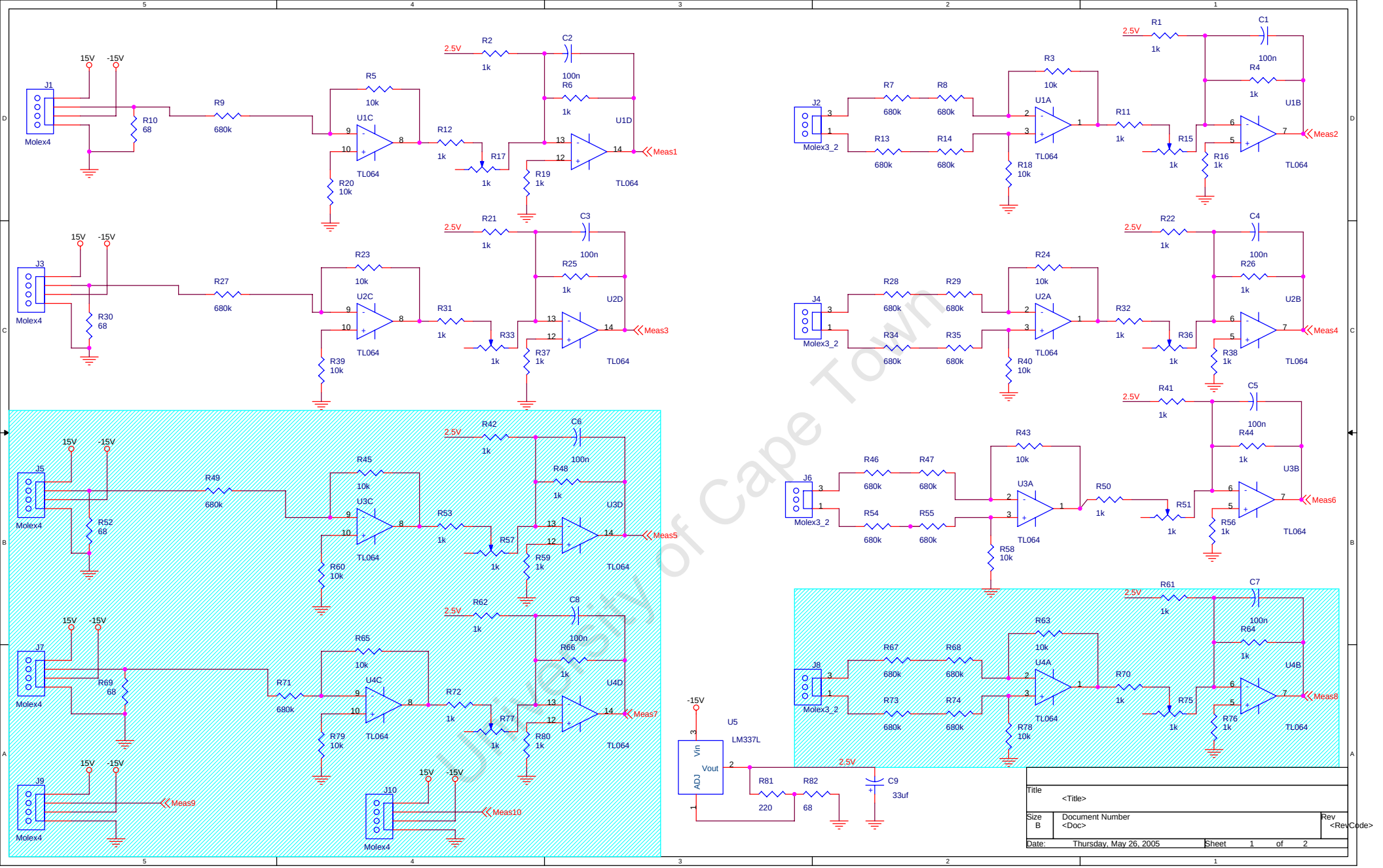

APPENDIX J

C CODE

```
/*
StandAlone Inverter 6kva 1 Phase
    */

#include "LF2407.h"

/* DAC,Display,ADC variables */
long int m;
int i,j,DAC1,DAC2,DAC3,DAC4,DAC5,DAC6,DAC7,DAC8,adc0val,adc1val,adc2val,adc3val;
int adc4val,adc5val,adc6val,adc7val;
int programfinish;
/* Inverter Variables */
int Vdc,Iout,Vout,Vout_old,Temp,Vdc_int,Vout_int,Iout_int,Temp_int,Vref;
long int Vdc_int_tot,Iout_int_tot,Temp_int_tot,Vout_int_tot;
int angle,angle_A,angle_B,angle_C;
int A,B,C,sector,t0,swfr;
long int t1temp,t2temp,t3temp,t1,t2,Aref,Bref,Cref,amplitude;
int Varef,Vbref,Vcref,Varefp,Varefm;
```

```
int count,V1count;

long int power,power_int,power_int_tot,LS_time,LS_count,Off_count=0;

int Vcutoff,Vrecon,Vbathigh;

int Padd,Pcount,Profile_count,LS_pwr,ramp_count;

char off,on=0;

int Voff,Ioff,test,Vout_old,Vout_tmp,out_err;

int Vpeak;

unsigned long int UVCnt = 0;

int PDA,OC,OV,UV,OT,PV;

int errtest=0,errcnt=0;

int oc_trip_counter = 0;

long int fault_reset_counter;

/* variables for 2nd harmonic of current */

int I_2nd_harmonic, I_2nd_harmonic_output, I_term, K_term;

long int I_2nd_harmonic_tot;

int I_2nd_harmonic_offset;

#define I_GAIN 1

#define K_GAIN 1
```

```
extern int sine();

/**

 * Function to reset watchdog

 */

void Reset_WD()

{

        *WDKEY = 0x0055;

        *WDKEY = 0x00AA;

}



 /* General purpose timer 1 interrupt

 * Occurs at rate of 10kHz (whenever timer reaches its period of 1024)

 */

interrupt void GPT1_underflow(void)

{

        /**PFDATDIR |= 0x0008;

        /* ADC measurement */
```

```
/*RESULT0 = ADC9, RESULT1 = ADC9, RESULT2 = ADC11, RESULT3 = ADC11

RESULT4 = ADC0, RESULT5 = ADC0, RESULT6 = ADC10, RESULT7 = ADC10

ADCIN0: CURRENT 2ND HARMONIC

ADCIN8: TEMP

ADCIN9: VDC

ADCIN10: IOUT

ADCIN11: VAC */

*CHSELSEQ1 = 0xBB99;

*CHSELSEQ2 = 0xAA00;

*ADCTRL2 |= 0x2000;

while(ADCTRL2 && 0x0200 == 0x0000) {};

*ADCTRL2 |= 0x0200;

adc0val = *RESULT0;

adc0val = adc0val>>6;

adc0val &= 0x03FF;

adc1val = *RESULT1;

adc1val = adc1val>>6;

adc1val &= 0x03FF;
```

```
adc2val = *RESULT2;

adc2val = adc2val>>6;

adc2val &= 0x03FF;

adc3val = *RESULT3;

adc3val = adc3val>>6;

adc3val &= 0x03FF;

adc4val = *RESULT4;

adc4val = adc4val>>6;

adc4val &= 0x03FF;

adc5val = *RESULT5;

adc5val = adc5val>>6;

adc5val &= 0x03FF;

adc6val = *RESULT6;

adc6val = adc6val>>6;

adc6val &= 0x03FF;

/* harmonic filter */

adc7val = *RESULT7;

adc7val = adc7val>>6;
```

```
adc7val &= 0x03FF;

Vout_old = Vout;

Vdc = (adc0val + adc1val)/2;

Vout_old = Vout;

Vout_tmp = (adc2val + adc3val)/2 - Voff;

Vout = Vout_old * 0x07;

Vout += Vout_tmp;

Vout = Vout >> 3; /* Output voltage filtering */

/* Vout = (Vout_old*7 + ((adc2val + adc3val)/2 - Voff))/8 */

Temp = 300;    /* No temperature reading: ADC result used for I_2nd_harm */

Iout = (adc6val + adc7val)/2 - Ioff;

/* Current 2nd Harmonic filter */

I_2nd_harmonic = (adc4val + adc5val)>>1 - I_2nd_harmonic_offset;

I_2nd_harmonic_tot = I_2nd_harmonic_tot + I_2nd_harmonic;

I_term = I_GAIN * I_2nd_harmonic_tot;

K_term = K_GAIN * I_2nd_harmonic;

I_2nd_harmonic_output = K_term + I_term;
```

```
    count++;
    if (Vout > 0 ) Vout_int_tot = Vout_int_tot + Vout;
    if (Vout < 0 ) Vout_int_tot = Vout_int_tot - Vout;
    if (Iout > 0 ) Iout_int_tot = Iout_int_tot + Iout;
    if (Iout < 0 ) Iout_int_tot = Iout_int_tot - Iout;
    Vdc_int_tot = Vdc_int_tot + Vdc;
    Temp_int_tot = Temp_int_tot + Temp;
    power = Vout*Iout;
    power = 166*power/1024;
    power_int_tot = power_int_tot + power;
    V1count++;
    /*If enough readings have been taken, update the *_int variables*/
    if (((V1count>300)&(Vout>-10)&(Vout<10))|(V1count>1919))
    {
Vout_int = Vout_int_tot/V1count;
Iout_int = Iout_int_tot/V1count;
Vdc_int = Vdc_int_tot/V1count;
Temp_int = Temp_int_tot/V1count;
```

```
        power_int = power_int_tot/V1count;
        Vout_int_tot = 0;
        Iout_int_tot = 0;
        Vdc_int_tot = 0;
        Temp_int_tot = 0;
        power_int_tot = 0;
        V1count = 0;
        out_err = Vref - Vout_int;
        if(out_err > 10) out_err = 10;
        if(out_err < -10) out_err = -10;
        amplitude += out_err;
            }
 /* Protection and switch on and off */
/*
       ramp_count++;
            if ((Vout_int<200)&(ramp_count>15)) {amplitude++;    ramp_count = 0;}
            if (ramp_count>100) ramp_count = 100;
  */
```

```
/*Protection for over/under current, voltage and temperature*/

        if (Vdc_int>Vrecon) UV = 0;

        if (Vdc_int>Vcutoff) UVCnt = 0;

        /* Simon: Allow no load if (Vdc_int<Vcutoff) UVCnt++; */

        if (UVCnt > 100000) UV = 1;

        if (Vdc_int>Vbathigh) OV = 1;

        if (Vdc_int<Vbathigh) OV = 0;

        if (Temp_int>800) OT = 1;                /* O Temp = 80 */

        if (Temp_int<650) OT = 0;

        if (power_int>6400)

        {

                Padd = power_int/128 - 50;

                Pcount++;

                if (Pcount>5000)

                {

                        Profile_count = Profile_count + Padd;

                        Pcount = 0;

                }
```

```
}
else
{
        Profile_count = 0;
}


if (Profile_count>800)
{
        Profile_count = 801;
        PV = 1;
}


LS_count++;


/* Note: Allow no load */
/* if ((on==1)&(power_int<LS_pwr)) Off_count++; */
if (Off_count>100000) Off_count = 100000;
```

```
if (power_int>LS_pwr)
{
        on = 1;
        Off_count = 0;
}

if (LS_count>LS_time)
{
        off = 0;
        LS_count = 0;
}

/* Note: Allow no load
if ((Vout_int>220)&(power_int<LS_pwr)&(LS_time>0)&((on==0)|(Off_count==100000)))
{
        off = 1;
        on = 0;
}
```

```
*/

/* end protection */

/*T2CNT is Timer 2 counter register (50Hz)

  By using the timer, we know the position in the waveform

  We therefore know the angle of the voltage phasor*/

t1temp = *T2CNT;

t1temp = 671*t1temp/4096;

angle = (int)t1temp;

if (amplitude>588) amplitude = 588;

if (amplitude<0) amplitude = 0;

/*Check flags*/

if ((OC==0)&(UV==0)&(OV==0)&(OT==0)&(PV==0)&(off==0))

{

        /*COMCONA is Compare Control Register for EVA

          Code sets FCOMPOE to 1, i.e. Enables PWM pins*/

        *COMCONA |= 0x0200;

}
```

```
    /* STRAT - added  for current limiting and retry on short function
       Evaluates true if !PDPINTA pin is 1*/
    if(((*COMCONA & 0x0100) == 0x0100) && (oc_trip_counter < 3) && (OC == 1))
    {
            if(errtest < 20000)
            {
                    errtest++;
            }
else        /*never runs*/
            {
                    oc_trip_counter++;
                    errcnt = 0;
                    fault_reset_counter = 0;
                    *COMCONA |= 0x0200;
                    OC = 0;
            }
    }
```

```
/*If less than 3 short circuits within 10 minutes then reset fault counter*/

if(oc_trip_counter < 4)

{

        fault_reset_counter++;

        if(fault_reset_counter > 6000000)

        {

                oc_trip_counter = 0;

                fault_reset_counter = 0;

        }

}

/* END - added by  for current limiting and retry on short function */




/*If any fault occurred, switch output off*/

if ((OC==1)|(UV==1)|(OV==1)|(OT==1)|(PV==1)|(off==1))

{

        amplitude = 0;
```

```
                *COMCONA &= 0xFDFF;        /*Clears FCOMPOE , i.e. disables PWM pins*/
        }
        /*PWM output voltage regulation*/


        /*Vpeak is peak output value, calculated from Vref */
        if (Vout>Vpeak+5) amplitude-=2;
/*Angle calculated earlier from T2CNT; amplitude is new desired amplitude*/
        t1temp = 1*(sine(angle));
        Varefp = (amplitude*t1temp)/1024 - I_2nd_harmonic_output;
        if (Varefp>512) Varefp = 512;    /*PWM timer counts from 0 to 1023 */
        if (Varefp<-512) Varefp = -512;
        Varefm = -Varefp;
      /*Update compare registers: when GPT1 reaches value in CMPR1 or CMPR2,
          pins PWM1,2 or PWM3,4 are updated*/
        *CMPR1 = Varefp + 512;
        *CMPR2 = Varefm + 512;
        programfinish = 1;
```

```
        Reset_WD();
        /* Added by MB for current limiting
          Evaluates true if !PDPINTA pin is 0*/
        if(!(*COMCONA & 0x0100))
        {
                errcnt++;
                errtest = 0;
    if(errcnt > 450)
    {
                        errcnt = 451;
                        OC = 1;
    }
        }

        /*Clear interrupt flag */
        *EVAIFRA |= 0x0200;
}
```

```
interrupt void Test3(void)

{

}




interrupt void Test4(void)

{

}




interrupt void Test5(void)

{

}




/**

 * ADC Interrupt
```

```
 * Does nothing
 */
interrupt void XINT2(void)
{
        *XINT1CR |= 0x8000;
}



/**
 * Main function
 */
void main(void)
{
        /* Delay */
        for (m=0; m<100000; m++) {}


        /* Enable peripheral clocks for EVA, EVB, SCI, SPI, ADC */
        *SCSR1 = 0x00EC;
```

```
/**SCSR2 |= 0x0020;    /* Disable WD */

/**WDCR |= 0x0020;    /* Disable WD */



/* Declare Unused IO pins as inputs */

*MCRA &= 0x0000;

*MCRB &= 0x0000;

*MCRC &= 0x0000;

*PADATDIR &= 0x0000;

*PBDATDIR &= 0x0000;

*PCDATDIR &= 0x0000;

*PDDATDIR &= 0x0000;

*PEDATDIR &= 0x0000;

*PFDATDIR &= 0x0000;



/* MCRA is MUX control reg A: code enables the PWM pins */

*MCRA |= 0x0FC0;



/* Interrupt setup */
```

```
*IMR = 0x0023;

*IFR = 0xFFFF;

*EVAIMRA = 0x0201;

asm("    clrc INTM");



/* SPI port setup for DAC coms */

*SPICCR &= 0x0FF7F;            /*SPI config control reg */

*MCRB |= 0x001C;

*SPICCR |= 0x000B;

*SPICTL = 0x0006;              /*SPI operation control reg */

*SPIBRR |= 0x0003;             /*SPI bit rate reg */

*SPICCR |= 0x0080;



*PCDATDIR |= 0x2020;



/* registers for E1 as code-timer */

*PEDATDIR |= 0x0202;           /* E1 is output and high */
```

```
/* Registers for ADC */


/* ACQ PS = 1111, CPS=1, CONT RUN=0, High Prior Interrupt, SEQ CASC=1
   Therefore, acquisition time window is 64/CLK */
*ADCTRL1 = 0x0F90;


/*Does nothing*/
*ADCTRL2 = 0x0000;


/* Sets 8 conversions to occur in a single sequence */
*MAXCONV = 0x000F;


/*  SCI (UART) port setup  */
*MCRA |= 0x0003;       /* IOPA0 = SCITXD and IOPA1 = SCIRXD */
*SCICCR = 0x0007;      /* 1 stop bit, no parity, 8 bit char length, loopback enabled */
*SCICTL1 = 0x0003;
*SCIHBAUD = 0x0001;            /* Baud rate set to 9600 */
*SCILBAUD = 0x00FF;
```

```
*SCICTL2 = 0x0002;    /* Enable RXRDY interrupt */

*SCICTL1 = 0x0023;  /* Relinquish from reset */



/* Registers for PWM generation */



/*  CMP1ACT=01,  CMP2ACT=10,  CMP3ACT=01,  CMP4ACT=10,  CMP5ACT=01,
CMP6ACT=10

   01 is active low on compare, 10 is active high on compare */

*ACTRA = 0x0999;



/* Sets 1 us deadtime */

*DBTCONA = 0x0AE8;



/* Reset compare registers */

*CMPR1 = 0;

*CMPR2 = 0;



/* Disable, then enable, compare operation (toggle bit CENABLE) */

*COMCONA = 0x0107;
```

```
*COMCONA = 0x8107;



/* Read Parameter Table from EEPROM: 48V battery, 6kVA system*/

Vcutoff = 12*420/10;

Vrecon = 12*480/10;

Vbathigh = 12*600/10;

LS_time = 0;

LS_pwr = 5;

Vref = 230;



LS_time = 19532*LS_time;



/* Calculate Vpeak from Vref */

t1temp = Vref;

t1temp = (230*t1temp)/128;

Vpeak = (int)t1temp;



/* Calculate current offset Ioff */
```

```
/* All results are from ADC10 (AC Current) */

*CHSELSEQ1 = 0xAAAA;

*CHSELSEQ2 = 0xAAAA;



/* Start sequencer and wait for result */

*ADCTRL2 |= 0x2000;

test = *ADCTRL2;

test &= 0x1000;

test = test>>12;

while(test==1) {test = *ADCTRL2;
                test &= 0x1000;
                test = test>>12;};

*ADCTRL2 |= 0x0200;



adc0val = *RESULT0;

adc0val = adc0val>>6;

adc0val &= 0x03FF;
```

```
adc1val = *RESULT1;

adc1val = adc1val>>6;

adc1val &= 0x03FF;



adc2val = *RESULT2;

adc2val = adc2val>>6;

adc2val &= 0x03FF;



adc3val = *RESULT3;

adc3val = adc3val>>6;

adc3val &= 0x03FF;



adc4val = *RESULT4;

adc4val = adc4val>>6;

adc4val &= 0x03FF;



adc5val = *RESULT5;
```

```
adc5val = adc5val>>6;

adc5val &= 0x03FF;



adc6val = *RESULT6;

adc6val = adc6val>>6;

adc6val &= 0x03FF;



adc7val = *RESULT7;

adc7val = adc7val>>6;

adc7val &= 0x03FF;



/* Offset is average of all readings */

Ioff = (adc0val + adc1val + adc2val + adc3val + adc4val + adc5val + adc6val + adc7val)/8;



/* Calculate voltage offset Voff */



/* All results are from ADC11 (AC Voltage) */

*CHSELSEQ1 = 0xBBBB;
```

```
*CHSELSEQ2 = 0xBBBB;



/* Start sequencer and wait for result */

*ADCTRL2 |= 0x2000;

test = *ADCTRL2;

test &= 0x1000;

test = test>>12;

while(test==1) {test = *ADCTRL2;

                                test &= 0x1000;

                                test = test>>12;};

*ADCTRL2 |= 0x0200;



adc0val = *RESULT0;

adc0val = adc0val>>6;

adc0val &= 0x03FF;



adc1val = *RESULT1;

adc1val = adc1val>>6;
```

```
adc1val &= 0x03FF;


adc2val = *RESULT2;
adc2val = adc2val>>6;
adc2val &= 0x03FF;


adc3val = *RESULT3;
adc3val = adc3val>>6;
adc3val &= 0x03FF;


adc4val = *RESULT4;
adc4val = adc4val>>6;
adc4val &= 0x03FF;


adc5val = *RESULT5;
adc5val = adc5val>>6;
adc5val &= 0x03FF;
```

```
adc6val = *RESULT6;

adc6val = adc6val>>6;

adc6val &= 0x03FF;



adc7val = *RESULT7;

adc7val = adc7val>>6;

adc7val &= 0x03FF;



/* Offset is average of all readings */

Voff = (adc0val + adc1val + adc2val + adc3val + adc4val + adc5val + adc6val + adc7val)/8;



/* Calculate offset for 2nd harmonic of current, I_2nd_harmonic_offset */



/* All results are from ADC0 (I_2nd_harmonic) */

*CHSELSEQ1 = 0x0000;

*CHSELSEQ2 = 0x0000;



/* Start sequencer and wait for result */
```

```
*ADCTRL2 |= 0x2000;

test = *ADCTRL2;

test &= 0x1000;

test = test>>12;

while(test==1) {test = *ADCTRL2;

                test &= 0x1000;

                test = test>>12;};

*ADCTRL2 |= 0x0200;



adc0val = *RESULT0;

adc0val = adc0val>>6;

adc0val &= 0x03FF;



adc1val = *RESULT1;

adc1val = adc1val>>6;

adc1val &= 0x03FF;



adc2val = *RESULT2;
```

```
adc2val = adc2val>>6;

adc2val &= 0x03FF;



adc3val = *RESULT3;

adc3val = adc3val>>6;

adc3val &= 0x03FF;



adc4val = *RESULT4;

adc4val = adc4val>>6;

adc4val &= 0x03FF;



adc5val = *RESULT5;

adc5val = adc5val>>6;

adc5val &= 0x03FF;



adc6val = *RESULT6;

adc6val = adc6val>>6;

adc6val &= 0x03FF;
```

```
adc7val = *RESULT7;

adc7val = adc7val>>6;

adc7val &= 0x03FF;



/* Offset is average of all readings */

I_2nd_harmonic_offset = (adc0val + adc1val + adc2val + adc3val + adc4val + adc5val + adc6val
+ adc7val)/8;




/* Setup timers */

swfr = 1024;

*T1PR = swfr;          /* Period = 2048*25nsec*2 = 100usec : freq approx 10kHz */

*T1CNT = 0x0;

*T1CON = 0xA802;      /* Up/down continuous mode, prescaler=1 (i.e. freq=CPUCLK)

                                                    timer disable, internal clock, Timer compare
enable */



*T2PR = 6250;              /* Period = 6142*25nsec*128 approx = 20msec or 50Hz */
```

```
*T2CNT = 0x0;

*T2CON = 0x9702;       /* Continuous up count, prescaler=111 (i.e. freq=CPUCLK/128)
                                                    timer disable, internal clock, Timer compare
enable */


*T1CON = 0xA842;       /* start the clock */

*T2CON = 0x9742;       /* start the clock */


/* Enable WD */

*WDCR = 0x00A8;

Reset_WD();


programfinish = 0;


/* Reset global variables */

count = 0;

V1count = 0;

Vdc_int_tot = 0;

Vdc_int = 0;
```

```
        Temp_int_tot = 0;
        Temp_int = 0;
        Vout_int_tot = 0;
        Vout_int = 0;
        Iout_int_tot = 0;
        Iout_int = 0;
        power_int = 0;
        power_int_tot = 0;
        I_2nd_harmonic_tot = 0;
amplitude = 0;
        Padd = 0;
        Pcount = 0;
        Profile_count = 0;
        OC = 0;
        OV = 0;
        UV = 0;
        OT = 0;
        PV = 0;
```

```
PDA = 0;

off = 1;

LS_count = 0;

Send_error = 0;

ramp_count = 0;

fault_reset_counter = 0;



/* Main loop */

for (;;)

{

        if (OT==1) Send_error = 20;

        if (OV==1) Send_error = 21;

        if (PV==1) Send_error = 22;

        if (UV==1) Send_error = 23;

        if (OC==1) Send_error = 24;

        if ((OT==0)&(OV==0)&(PV==0)&(UV==0)&(OC==0)) Send_error = 25;



        if (Send_flag==1)
```

```
        {
            Hbyte = Send>>8;
            Lbyte = (char)Send;
            *SCITXBUF = Hbyte;while((*SCICTL2 & 0x0080) == 0x0000) {};
            *SCITXBUF = Lbyte;while((*SCICTL2 & 0x0080) == 0x0000) {};
            Send_flag = 0;
        }

        while (programfinish == 0);

        programfinish = 0;
}
```