Design and Implementation of a Secondary Surveillance Radar/Identification Friend or Foe Transceiver Card

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DECLARATION

I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own.

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Abstract

The performance of SSR/IFF equipment, i.e. the transponder or the interrogator, can be tested by means of an SSR/IFF test set, which is usually extremely expensive, hard to transport and requires end-user certificates.

This dissertation thus focuses on the design and implementation of a short-range real-time SSR/IFF Transceiver Card (ITRC), which can be used as an experimental platform for SSR/IFF test applications. User requirements are provided and analysed, resulting in a system breakdown structure, where for each subsystem a summary of related concepts is presented in order to produce the technical requirements for the system.

The hardware was designed to be smaller, lighter, less expensive and easy to repair than conventional SSR/IFF test sets. When it has been integrated with an existing SSR/IFF reply emulator, it is capable of generating and analysing RF SSR/IFF signals for modes 1, 2, 3/A, C and secure mode 4 at a frequency of 1030 MHz and 1090 MHz in order to test the functionality of the interrogator and transponder.

Verification for the design was accomplished by testing the transceiver hardware and then integrating the system with SSR/IFF transponder and interrogator. The results achieved were found to be compliant with the user requirements.

Acknowledgements

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Nomenclature

ADC	Analogue to Digital Converter
ACP	Azimuth Change Pulse
ARP	Azimuth Reference Pulse
ATC	Air Traffic Control
ATCRBS	Air Traffic Control Radar Beacon System
BIT	Built-In Test
BPF	Band Pass Filter
CW	Continuous Wave
DAC	Digital to Analogue Converter
DSP	Digital Signal Processor
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
IFF	Identification Friend or Foe
IIR	Infinite Impulse Response
ITRC	IFF transceiver card
INT	Interrogator
ISLS	Interrogation Side-Lobe Suppression
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
LO	Local Oscillator
Mode S	Civilian Surveillance mode
NATO	North Atlantic Treaty Organization
PAM	Pulse Amplitude Modulation
PPI	Plan Position Indicator
RF	Radio Frequency
SIF	Selectivity Identification Feature
SLS	Side-Lobe Suppression

SPDT	Single Pole Double Throw
SPI	Special Pulse Indicator
SSR	Secondary Surveillance Radar
STANAG	Standardisation Agreement
TTL	Transistor-Transistor Logic
TxP	Transponder
UCT	University of Cape Town
UUT	Unit Under Test
VCO	Voltage Control Oscillator
VHDL	VHSIC Hardware Description Language
VSWR	Voltage Standing Wave Ratio

1 Introduction

This dissertation describes the specifications, design, implementation and test procedure of a real time, Secondary Surveillance Radar/Identification Friend or Foe (SSR/IFF) transceiver for SSR/IFF test applications. This system represents part of a planned SSR/IFF test simulation system that is shown in Figure 2.

The IFF Transceiver Card (ITRC), which is the focus of this dissertation, is designed to detect and transmit SSR/IFF Radio Frequency (RF) signals compatible with the North Atlantic Treaty Organisation's (NATO) Standardization Agreement known as STANAG-4193, in modes 1, 2, 3/A, C and mode 4. It is intended to be able to test the functionality of interrogators and transponders.

1.1 Introduction to SSR and IFF

Secondary Surveillance Radar (SSR) is a radar system used in Air Traffic Control (ATC) for monitoring purposes. It is based on the Identification Friend or Foe (IFF) system, which was developed by the military during the Second World War, and the two systems are still in use today [3].

Both military and civilian systems are used to identify the identity, position and altitude of a platform (in other words, an aircraft, a ship, etc.). IFF is also used to recognize friendly platforms by sending encrypted interrogations, which means that only platforms carrying the correct decipher key are recognized as friends.

The SSR/IFF system, as illustrated in Figure 1, mainly comprises an interrogator and a transponder (transmitter-responder). The interrogator continuously transmits interrogation pulses via the directional beam of the antenna (this could be either a ground station rotation antenna or an airborne directional antenna) at 1030 MHz. When the transponder passes through the main beam of the interrogator antenna, it detects the interrogation signal, demodulates it and replies at 1090 MHz to the interrogator, which decodes the reply and determines the identity of the aircraft. The aircraft is then displayed as a tagged icon on the air traffic controller's radar screen at the calculated

bearing and range. The interrogation can happen between a ground station and a platform or between two platforms [1], [3].

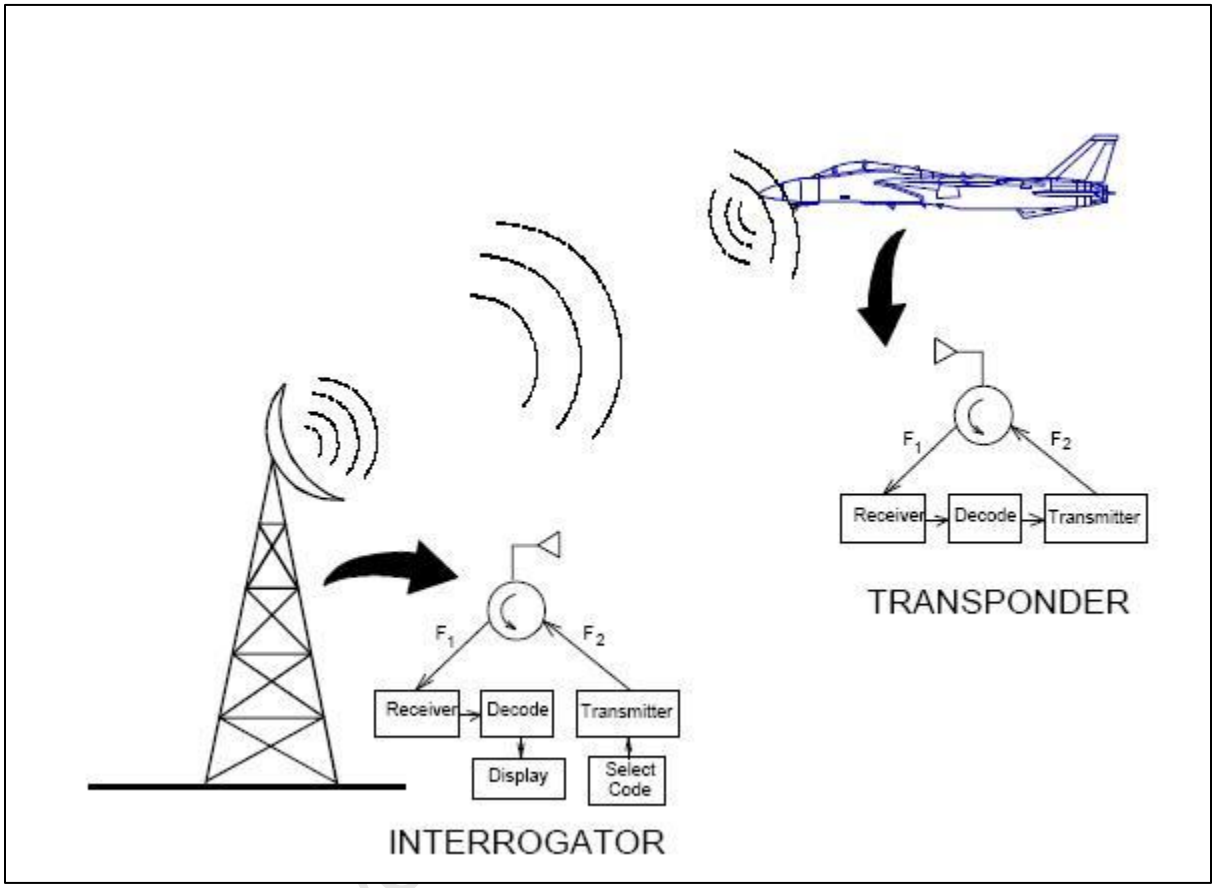


Figure 1: Typical SSR/IFF system components. The ground station's interrogator sends interrogations in one of the SSR/IFF modes and the target's transponder receives and decodes the interrogations. It then replies to the interrogator, which decodes the replies and shows the target's identity and range on a radar monitor. Adapted from [2].

The transponder's replies are generated depending on the mode in which it was interrogated. There are various interrogation modes for SSR/IFF (see Section 3.2.1.1). Military platforms use modes 1, 2, 3 and 4, whereas civilian platforms use modes A, C and S. Modes 1, 2 and 3 are known as Selectivity Identification Feature (SIF) modes. Mode 1 is used for military tactical operations; mode 2 is used to identify military aircraft

missions; modes 3 and A (called also mode 3/A due to their similarity) request an identity that is used for air traffic control purposes; mode C is used to request an aircraft's altitude; and mode 4 is classified for exclusive use by NATO countries. Mode S is replacing SIF modes; it is able to deal with ATCRBS (Air Traffic Control Radar Beacon Systems) and uses discrete addressing to interrogate targets one by one [1].

1.2 Introduction to the ITRC

The performance of the SSR/IFF equipment, i.e. the transponder or the interrogator, can be tested by means of an SSR/IFF test set, which can be connected directly to the unit being tested or to an antenna that is transmitting and receiving at a short distance. The short-range is preferred to avoid the phase difference issue, which is described in Section 1.6. In this study, the functional operation of the equipment is tested by generating SSR/IFF interrogation and reply pulses.

The IFF Transceiver Card (ITRC) is designed and implemented as an experimental platform for SSR/IFF test applications. It is designed to test the functionality of the interrogator and transponder by analysing incoming SSR/IFF signals and generating valid interrogations and replies with specific characteristics for different applications. An IFF reply emulator [5], which is a project that has been developed by another Masters student in the Radar Remote Sensing Group (RRSG) at the University of Cape Town (UCT), and which represents a part of the IFF test simulation system illustrated in Figure 2, has been modified and used to analyse received Transistor-Transistor Logic (TTL) signals and to generate valid interrogations and replies.

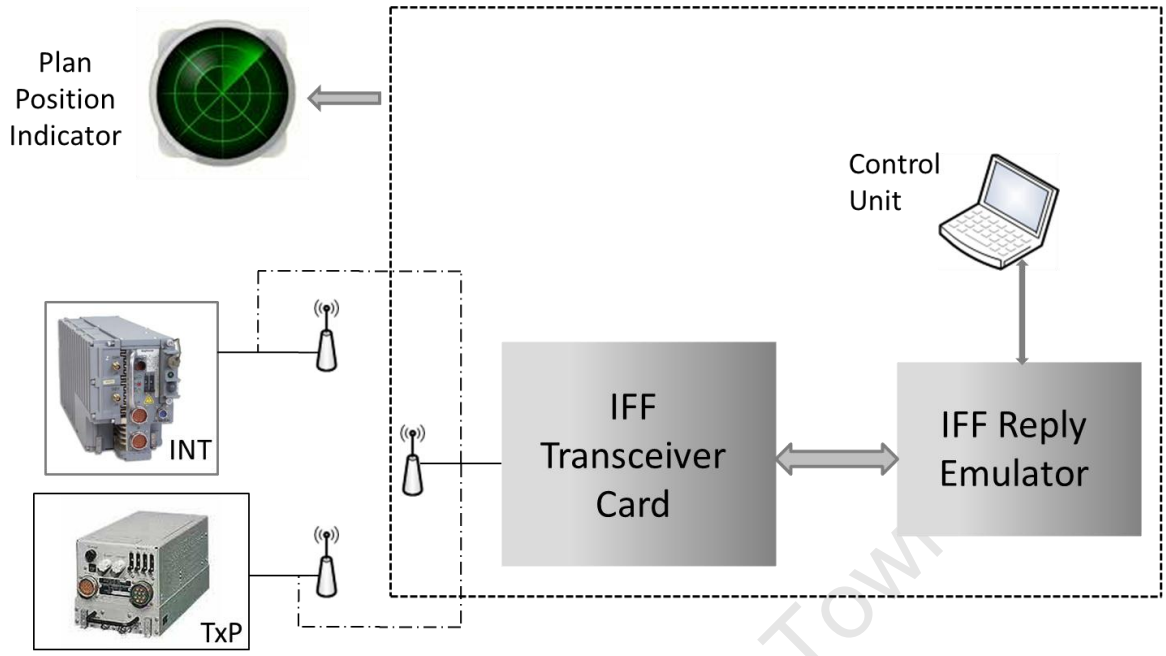


Figure 2: SSR/IFF Test Simulation System. The box surrounded by the dashed line represents the SSR/IFF test system that is used to test the functionality of an existing transponder and an interrogator under development. The dash-dot line shows that the test set can be connected directly to IFF equipment or to an antenna for short range testing. The plan position indicator represents the position and identity of targets.

1.3 Scope of the project

The project scope is to create a suitable platform that is able to generate and send SSR/IFF signals as well as to detect and analyse SSR/IFF signals coming from short ranges.

The project structure, as summarised in the high level block diagram (Figure 3), encompasses three sections:

1. An analogue section, which is responsible for capturing and transmitting analogue signals.
2. A digital section, which is responsible for analysing the data coming from the analogue section, generating the data going to the analogue section and identifying the input/output signals values to control the components of the analogue section.

3. A PC workstation, which is responsible for programming and debugging the digital section as well as reporting the test results.

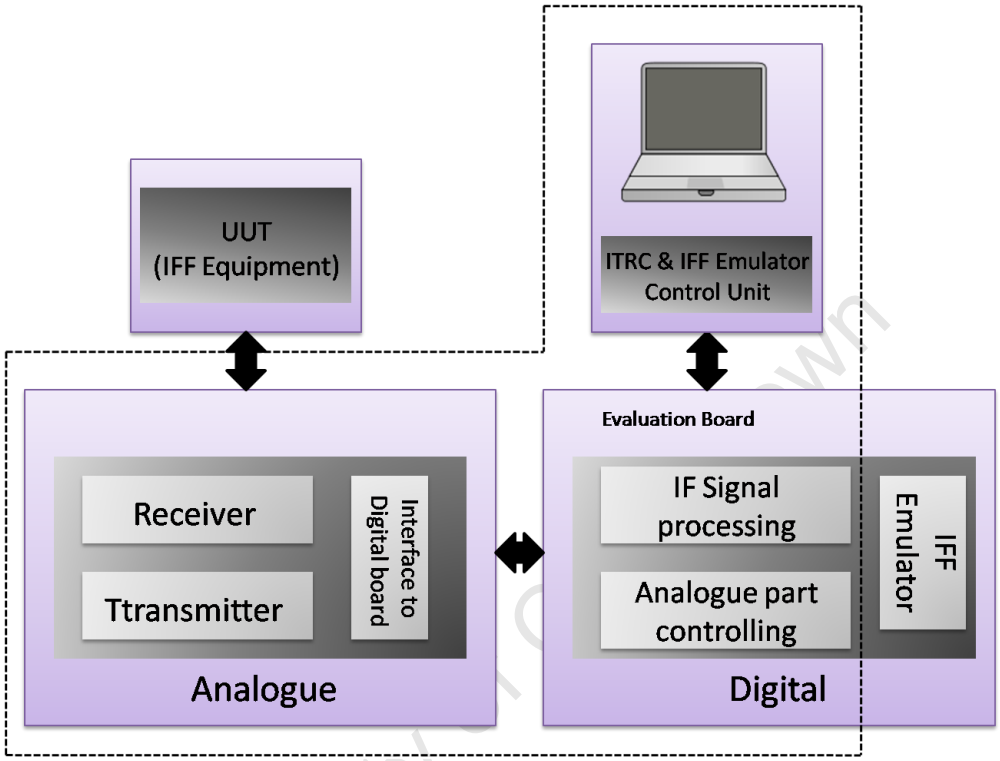


Figure 3: The dashed section of the diagram represents the ITRC High Level Block Diagram. The ITRC analogue section consists of a receiver, a transmitter and an interface board. The receiver down-converts the SSR/IFF RF signals received from the IFF Unit Under Test (UUT) to IF signals and passes them through the interface board to the digital evaluation board for processing. The transmitted RF interrogations and replies are managed by TTL signals coming from the digital board, which determine the mode of operation and the peak power of the pulses. The digital part of the ITRC is responsible for analysing the IF signals that come from the receiver as well as determining the control signals value based on the test applied. The control unit is used to select the SSR/IFF mode of operation and the test type.

1.4 Project objectives

The objectives of the project are:

- To analyse the requirements of testing the SSR/IFF equipment in order to establish specifications for the ITRC.
- To simulate, design and implement the hardware that is necessary to achieve the requirements of the analogue section.
- To understand the capabilities of the IFF reply emulator, which represents a part of the IFF simulation system, and to modify the firmware in order to meet the user requirements.
- To control the input /output signals of the ITRC using the Quixote board.
- To analyse and test the system performance.

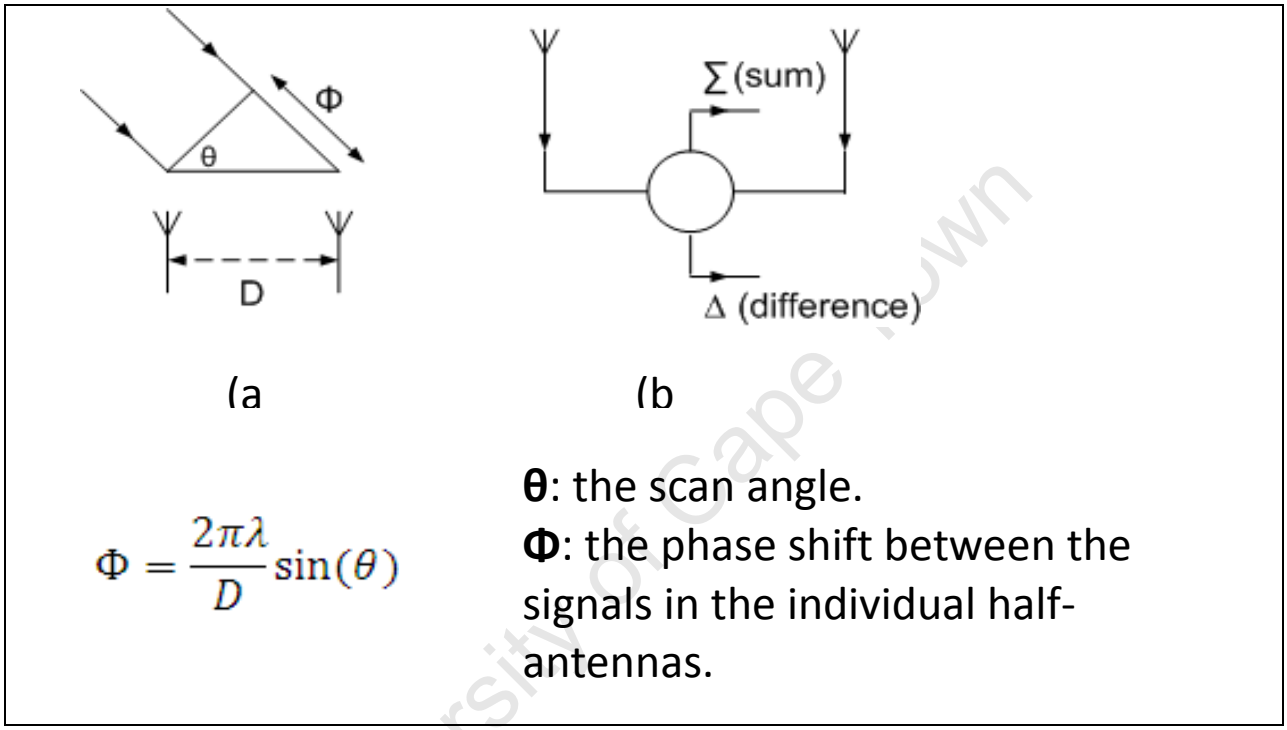
1.5 Background

The ITRC is designed to test an existing transponder as well as an interrogator under development. The test requirements of the interrogator and the transponder were used to determine the ITRC specifications. Normally during testing and qualifying the transponders and interrogators, many problems may arise due to SSR/IFF test sets not generally being available or not working properly. Cost and time needed to repair such equipment, its lack of transportability and the need for end-user certificates may be serious obstacles. The ITRC, as a prototype, does not replace SSR/IFF test sets, i.e. it does not provide their entire range of functions; however, it does provide some of the main test functions (see Section 3.3). Firmware written by another student in the RRSG has been modified and used for the digital generation of SSR/IFF interrogations and replies (see Section 3.1).

1.6 Limitations of the project

A transponder has two RF channels connected respectively to the upper and lower antennas of the airborne platform. The antenna that receives the stronger signal is used to transmit the reply. In the interrogator, there are also two RF channels, namely, the sum and delta channels. The antenna connected to the interrogator consists of two parts, as illustrated in Figure 4-a. Signals arriving at the two parts from any angle

normally have the same strength but with a phase difference due to the extra distance to be travelled to the other part of the antenna. The two received signals are processed: the result of their addition is the sum signal, whereas the difference between them represents the delta signal, as shown in Figure 4-b.



$$\Phi = \frac{2\pi\lambda}{D}\sin(\theta)$$

Figure 4: Adapted from [1]. (a) Relative phase delay of the signal at the antenna, (b) Production of sum and delta beams.

The ITRC as test equipment did not take into account the above mentioned issues because it is only used for short-range testing. It tests the transponder, as an airborne target, located in the main lobe (the effective beam) of the transmitter by using one channel and terminating the other channel. In the case of testing an interrogator, the ITRC tests the interrogator as a target located between the two parts of the antenna, i.e. it analyses the signals coming through the sum channel only. The delta channel is always terminated because the phase difference between the two received signals in these conditions is almost zero.

The ITRC is designed to be able to respond to ATCRBS interrogation in modes 1, 2, 3/A and C. The system is also capable of responding to mode 4 with fixed challenges. Mode S capabilities were not considered in the ITRC design, but could be expanded on in future testing.

The ITRC as test equipment does not test more than one unit at a time. It can either receive interrogations from one interrogator or it can receive replies from one transponder.

1.7 Plan of development

The subsections below describe briefly the following chapters of the dissertation.

Chapter 2: User Requirements

This chapter presents the functional, performance and hardware requirements of the ITRC project. These requirements have been derived from the specifications and test requirements of existing IFF equipment, transponders and interrogators. The objective of this project is to generate valid RF interrogations and replies using the IFF Emulator firmware and to analyse signals coming from transponders or interrogators using the capabilities of the Quixote evaluation board [9].

Chapter 3: Functional analysis, system specifications and acceptance test procedure

This chapter describes the ITRC architecture and looks at how the system is intended to work. All the cases that the ITRC will cover as a transponder and as an interrogator are introduced in this chapter.

This chapter also includes the functional analysis of the system, which leads to the specifications of the ITRC. Chapter 3 analyses the system by doing some theoretical calculations in order to define the main parameters of the transceiver performance, such as receiver dynamic range and transmitter output power.

Chapter 4: System design

This chapter simulates the system using the knowledge gained from Chapter 3. It thus looks at critical areas and at how the maximum performance levels can be achieved. The difficulty of solving critical area problems and the time constraints of the project have led to certain tradeoffs, such as using off-the-shelf modules or modules from other projects. After completing the system simulations using *Agilent Genesys* software, this chapter documents the components that have been selected and the reason why these components were chosen. The system schematic and layout have been generated using the *Altium Designer* software.

The digital evaluation board specifications and the interface to the analogue board are also contained in this chapter. It furthermore presents the IFF emulator abilities and the functions that have been added to the system to meet all user requirements. The Digital Signal Processor (DSP) and FPGA codes have been modified to manage the input/output signals, which determine the functions applied to the analogue board.

Chapter 5: System testing

This chapter evaluates the performance of the ITRC by testing the analogue and digital parts of the system. It includes the RF and IF test results of the transmitter and the receiver. All results must meet the user requirements detailed in Chapter 2. Digital testing is covered too, to ensure that the FPGA and the DSP have been programmed successfully and correctly, and that it is able to communicate with the analogue board. A built-in test of the card is a part of the system test procedure, which includes other tests, such as load return loss and loopback tests. The chapter further discusses all the problems and obstacles that occurred during the test phase, as well as the methodologies used to solve them. There are no environmental tests required for this card, as it operates at normal environmental conditions.

This chapter discusses the testing of the IFF equipment's functionality, the transponder and the interrogator, using the ITRC. The IFF equipment needed to test the ITRC will be borrowed from Tellumat [14], a South African company, during the test phase.

Chapter 6: Conclusion and future work

This chapter presents a conclusion of the designed system and its compliance with the user requirements. It also documents the problems that occurred during the study and makes recommendations for ensuring better performance. Future work and suggestions to improve the system are also included at the end of this chapter.

1.8 Summary

The first chapter of this dissertation introduced the ITRC project as well as the objectives and limitations of the research. It also gave a brief overview of the SSR/IFF and the system's main components. This chapter ended with an overview of the contents of the following chapters. The next chapter describes in detail the functional, performance and hardware requirements of the ITRC project.

2 ITRC User Requirements

The ITRC represents part of an IFF simulation system, which has the ability to test existing transponders and interrogators under development. Thus, most of the ITRC design requirements have been derived from these equipment test requirements.

The ITRC is a system required to generate and analyse SSR/IFF RF signals, depending on the applied test application (see Section 4.5.3.5). This chapter presents the functional, performance and hardware user requirements of the ITRC.

2.1 Functional Requirements

The following are the functional requirements that the ITRC must satisfy as real-time SSR/IFF test equipment.

2.1.1 Transponder simulation

When the ITRC acts as a transponder, it must be able to generate valid SSR/IFF RF replies, depending on the mode of operation described in Section 2.1.3. The generated SSR/IFF signals must be compliant with the international IFF standard STANAG 4193.

As a transponder, the ITRC must be able to receive SSR/IFF interrogations from an interrogator and then to decide whether to reply or not. When used for laboratory testing, the interrogator must be able to see the ITRC as a transponder located in the main lobe (the effective beam) of the transmitter.

2.1.2 Interrogator simulation

When the ITRC acts as an interrogator, it must be able to generate valid SSR/IFF RF interrogations, depending on the required mode of operation described in Section 2.1.3. As with the transponder, the generated SSR/IFF signals must be compliant with the international IFF standard STANAG 4193.

The ITRC as an interrogator must be able to generate interrogations as signals from the main-lobe or the side-lobes of the antenna, as well as to receive replies from a transponder and to analyse them to determine the target's identity and range. When used for laboratory testing, the transponder must reply to the ITRC from one channel only.

2.1.3 IFF modes of operation

The ITRC must be able to generate and respond to modes 1, 2, 3/A, C and mode 4 challenges and replies.

2.1.4 Number of targets

As an interrogator, the ITRC must be able to respond to one transponder at a time, i.e. it does not need to de-garble overlapped replies or de-correlate False Replies Unsynchronized in Time (FRUIT).

When replying, the ITRC must be able to generate normal replies from up to 1500 targets. Garbled and FRUIT replies must be generated from up to four targets to test the interrogator's ability to de-garble and identify false replies.

2.1.5 Real-time operation

The ITRC, when used as a transponder, must be able to receive interrogations and reply to them within the time limits defined in the IFF standard STANAG 4193.

In both cases, i.e. interrogating and replying, the ITRC must be able to control the switching time between the transmitting and the receiving sections.

2.1.6 Range

The ITRC must be able to communicate with targets located at any distance between 10 metres and one kilometre.

2.2 Performance Requirements

The ITRC performance must be tested to make sure that the card works properly. The performance of the ITRC is defined by its ability to identify and generate SSR/IFF STANAG-4193 compliant signals. The following are the performance requirements that need to be part of the ITRC design plan.

2.2.1 ITRC self-test (loopback test)

The ITRC must have the facility to conduct loopback self-testing. It must be able to transmit modulated SSR/IFF signals and route them back to the receiver to be analysed

and verified. The isolation between the transmitting and receiving stages should not be affected by the loopback path and should be at least 70 dB.

2.2.2 Load Return Loss Measurement

The ITRC must provide simultaneous measurements of the transmitted power and the reflected power of the connected antenna or IFF equipment.

2.3 Hardware Requirements

2.3.1 Digital Board

The Innovative Integration Quixote board [9], which has been used to run the IFF reply emulator, must be used as the digital section of the project (see Section 4.5.1).

2.3.2 IFF reply emulator Firmware reuse

The firmware of the IFF reply emulator must be modified to meet the ITRC requirements.

2.3.3 ITRC-Quixote interface

The ITRC receiver must provide the Quixote board with signals at an IF frequency of 70 MHz. The Quixote board must provide the ITRC with the information required to generate IFF RF pulses to be transmitted within certain times. The input/output signals must be made available from/to the ITRC via the input/output pins of the Quixote board.

2.4 Summary

This chapter presented the user requirements of the ITRC, which have been divided into functional requirements, performance requirements and hardware requirements. The following chapter explains the system architecture and analyses the user requirements to derive the ITRC technical specifications and the procedure to test the system performance.

3 Concept Study and Requirements Analysis

This chapter starts with a brief description of the SSR/IFF target emulator, which has been developed by another Masters student in the RRSG at UCT. The user requirements in the previous chapter have been analysed to create a system breakdown for the ITRC project.

The ITRC subsystems' concept studies are summarized in this chapter to discuss the aspects that are relevant to the project. These concept studies are the result of studying the NATO document (STANAG-4193) [7], which describes the SSR/IFF timing and power level standards. The ITRC requirements have been derived either from the subsystem concept study or directly from the user requirements.

3.1 SSR/IFF Reply Emulator Background

The SSR/IFF target emulator [5] is a real-time system designed to test an SSR/IFF interrogator digital signal processor. It is able to generate digital TTL SSR/IFF replies that are compatible in time with relevant aspects of STANAG-4193 [7]. The emulator is capable of generating simultaneous replies from up to 1500 simulated targets in each antenna sweep. The emulated target may move within 360^{o} at ranges from 0 to 600km and at mode C altitude from -1000 to 121000 feet. These targets are equipped with SSR/IFF transponders and cryptographic computers, which can be programmed by the user to reply in mode 1, 2, 3/A, C and secure mode 4 as well as to give emergency and Special Position Indicator (SPI) replies. The emulator is able to create both garbled and FRUIT SSR/IFF reply scenarios. The target emulator tests the ability of the interrogator's signal processor to identify the emulated targets correctly.

3.2 User Requirements Analysis

The user requirements in Chapter 2 have been analysed to conceptualise the ITRC structure. Figure 5 summarizes the identified subsystems of the ITRC and the functions of each subsystem. Thereafter, the operational concepts of each subsystem were studied to derive the specifications of the ITRC.

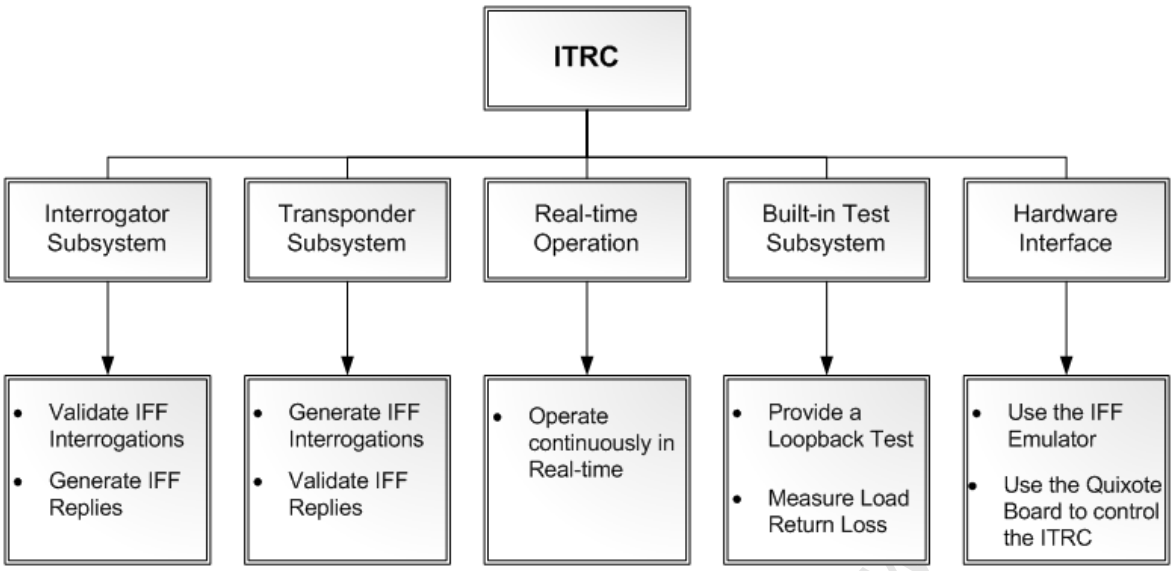


Figure 5: ITRC System Breakdown, indicating the ITRC subsystems and the main functions of each subsystem.

3.2.1 Interrogator Subsystem

The interrogator is a challenge system meant to identify the platform's identity, position and altitude. The interrogator sends a challenge at a frequency of 1030MHz, consisting of coded interrogations, depending on the mode of operation, as described in Section 3.2.1.1 below, and then receives and processes coded replies from the airborne transponder at a frequency of 1090MHz, whereafter it decides whether the reply is valid or not [1].

The aspects of the user requirements that are relevant to the interrogator are analysed in this section, leading to the specifications for the ITRC interrogator subsystem.

3.2.1.1 Interrogator Modes of Operation

The civilian and military modes of operation were defined in the introduction of Chapter 1. Military platforms conventionally use modes 1, 2, 3 and 4, whereas civilian platforms conventionally use modes A, C and S.

The challenges (interrogations) generated by the interrogator, except for those of mode 4, consist of three pulses: two identical mode pulses called P1 and P3 and a side-lobe

suppression (SLS) pulse called P2. The characteristics of these pulses are summarised in Table 1. The period between P1 and P3 determines the mode of operation, as seen in Figure 6, and the difference in amplitude between (P1, P3) and P2 describes whether the target is in the main lobe or the side-lobe of the main beam of the interrogator antenna. The side-lobe pulse is explained further in the following section.

Table 1: Modes 1, 2, 3/A, C and mode 4 interrogation pulse characteristics

Duration	For modes 1, 2, 3/A and C: P1 and P3: 0.8 ± 0.1 µs. P2: 0.8, +0.05, -0.1 µs.	For mode 4: All pulses: 0.5 ± 0.1 µs.
Rise Time	Between 0.05 and 0.1 µs.	
Decay Time	Between 0.05 and 0.2 µs.	
Pulse Top Ripple	1 dB peak to peak (maximum)	

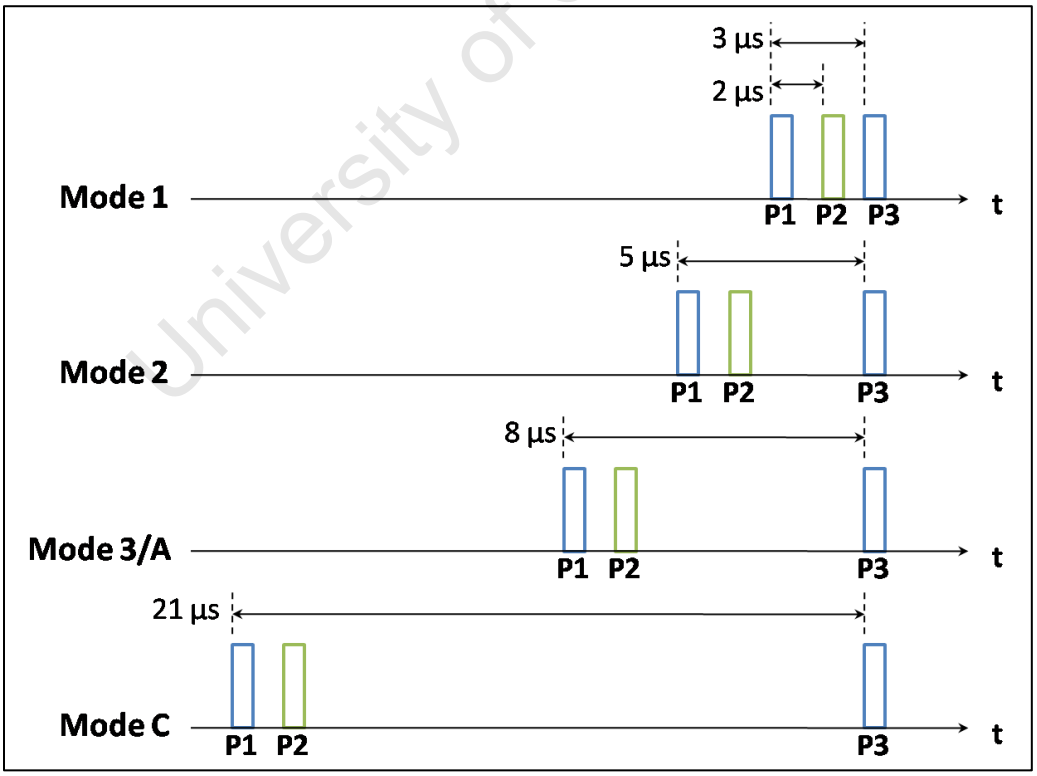


Figure 6: Modes 1, 2, 3/A and C interrogation timing characteristics. The pulse interval between P1 and P3 determines the interrogation mode.

A mode 4 interrogation consists of thirty-seven pulses, as shown in Figure 7. The first four pulses, which are collectively known as the Sync Pulse Group, allow the transponder to detect the interrogation in mode 4. The fifth pulse is the side-lobe suppression pulse, which is similar to P2 in modes 1, 2, 3/A and C. The last 32 pulses consist of an encrypted message containing a delay value, which determines when the transponder must reply. This message is generated by a cryptographic computer connected to the interrogator.

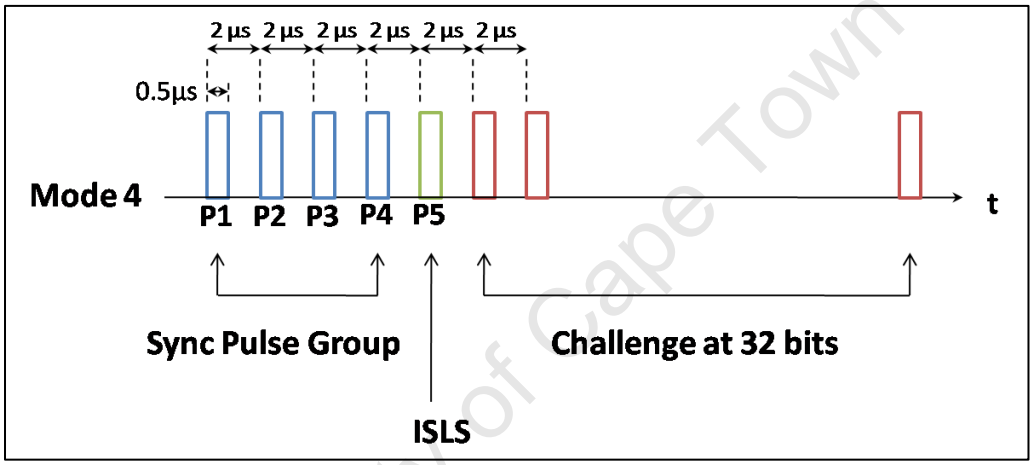


Figure 7: IFF Secure Mode 4 interrogation timing characteristics. A mode 4 interrogation consists of a group of 4 pulses (collectively called the Sync Pulse Group) spaced at 0, 2, 4, and 6 µs respectively, and an ISLS pulse at 8 µs. These signals are followed by up to 32 pulses, which specify the time that a transponder must wait before generating a reply.

3.2.1.2 Interrogation Side-Lobe Suppression

The interrogator system generates two beams via two different antennas, as seen in Figure 8 below. The first beam, called the interrogate beam or the main beam, is a narrow beam with side-lobes and a much lower gain. The second one, called the side-lobe suppression (SLS) beam, is generated from an omnidirectional antenna to cover all directions except that of the main beam. The side-lobe suppression is meant to prevent short-range aircrafts from replying to signals from the interrogator beam side-lobes, which could lead to false measurement of the real target direction [1]. To reply, the

transponder just needs to compare the level of P1, P3 with the level of P2 to know whether the interrogation is transmitted from the main lobe or from a side-lobe.

P1 and P3 are transmitted via the interrogate beam, whereas P2 is transmitted via the side-lobe suppression beam [1]. The PIN switch module, which represents a part of the interrogator system, is responsible for switching between P1, P2 and P3 within a certain time depending on what mode of operation is applied.

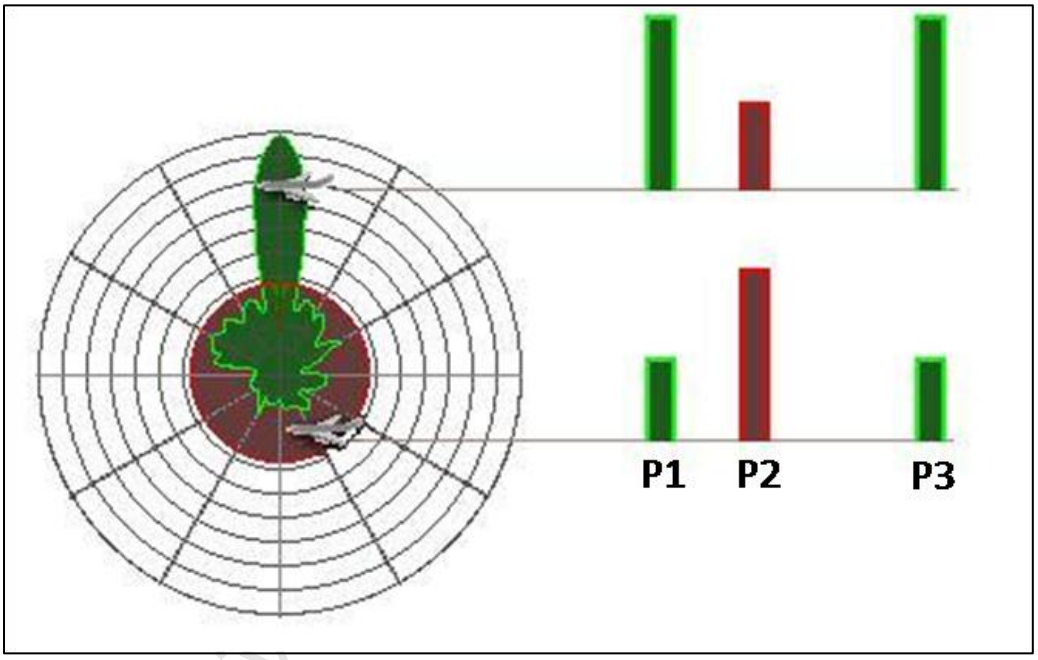


Figure 8: Interrogation Side-lobe Suppression (ISLS). The gain of the directive antenna is greater than the gain of the omnidirectional antenna. Therefore, the amplitude of P2 (or P5 in the case of mode 4 interrogations) is lower than P1 and P3 when the target is in the main interrogation beam [10].

3.2.1.3 Reply Signals

In general, the interrogator can receive one of the following types of replies:

1) Normal replies, in which case the interrogator receives a reply from one target at a time.

2) Garbled replies, which are defined as an overlap in time between two or more replies from two or more aircrafts. Such an overlap happens when the number of targets in the same area increases, so that they become closely spaced in range and azimuth[1], [4].
3) FRUIT replies, which are defined as replies received by an interrogator when it was not expecting replies at that specific time. This happens when one or more targets are located in the main beam of two or more interrogators[1], [4].

3.2.2 Transponder Subsystem

The transponder is an SSR/IFF airborne equipment that receives interrogations at a frequency of 1030MHz and, depending on the detected mode of operation, as described in Section 3.2.1.1, the transponder modulates and transmits the appropriate reply to the interrogator at a frequency of 1090MHz [1].

The aspects of the user requirements that are relevant to the transponder are analysed in this section, leading to the ITRC transponder subsystem specifications.

3.2.2.1 Transponder Modes of Operation

The transponder reply in all modes described in Section 3.2.1.1, except for mode 4, consists of F1 and F2, which are called framing pulses. As shown in Figure 11 below, the 13 data pulses between F1 and F2, except for pulse X, which is not currently used, constitute 4096 different reply codes. These reply codes are used, depending on the interrogation mode, as shown in Table 2, and the interrogated transponder code that has been set by the operator. The special position indicator (SPI) pulse at the end is an optional pulse controlled by the pilot and switched on only on the request of the ground ATC for additional identification purposes [1]. The characteristics of the reply pulses are given in Table 3.

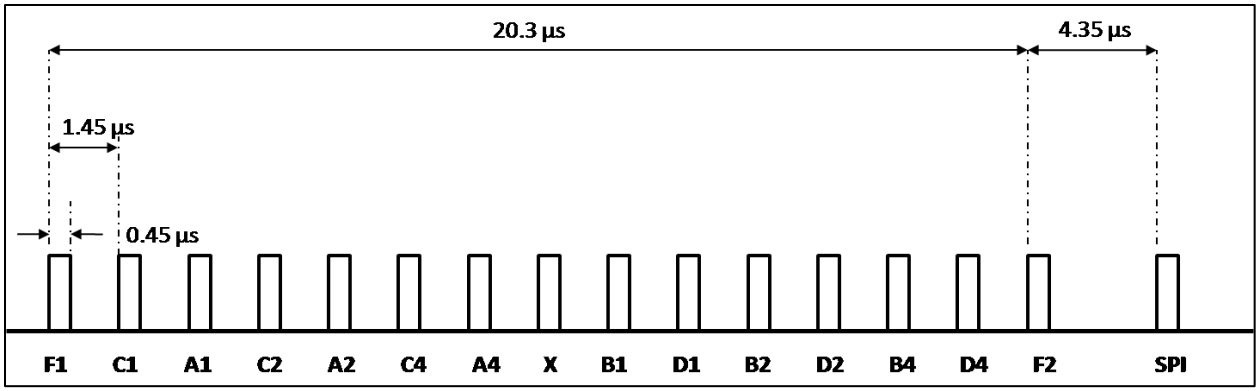


Figure 11: Modes 1, 2, 3/A and C reply timing characteristics. The reply consists of two framing pulses (F1 and F2), on either side of 13 data pulses. By using 12 of these pulses, the transponder is able to generate 4096 different reply codes.

Table 2: Reply codes for modes 1, 2, 3/A and C

Mode	No. of codes	Description
1	32	All A, B1 and B2 pulses
2	4096	All pulses
3/A	4096	All pulses
C	2048	D1 pulse not used

Table 3: Modes 1, 2, 3/A, C and mode 4 reply pulse characteristics

Duration	All pulses: 0.45 ± 0.1 µs.
Rise Time	Between 0.05 and 0.1 µs.
Decay Time	Between 0.05 and 0.2 µs.
Pulse Top Ripple	1 dB peak to peak (maximum)

The mode 4 reply signal consists of three pulses, which are transmitted with a coded delay. For the interrogator to mark the target as a friend, the reply delay value must correspond to the value in the interrogation. A 202µs fixed delay is added to the reply

delay, which gives the transponder enough time to pass the encrypted message to the cryptographic computer attached to it. Figure 12 summarizes the timing characteristics of mode 4 replies.

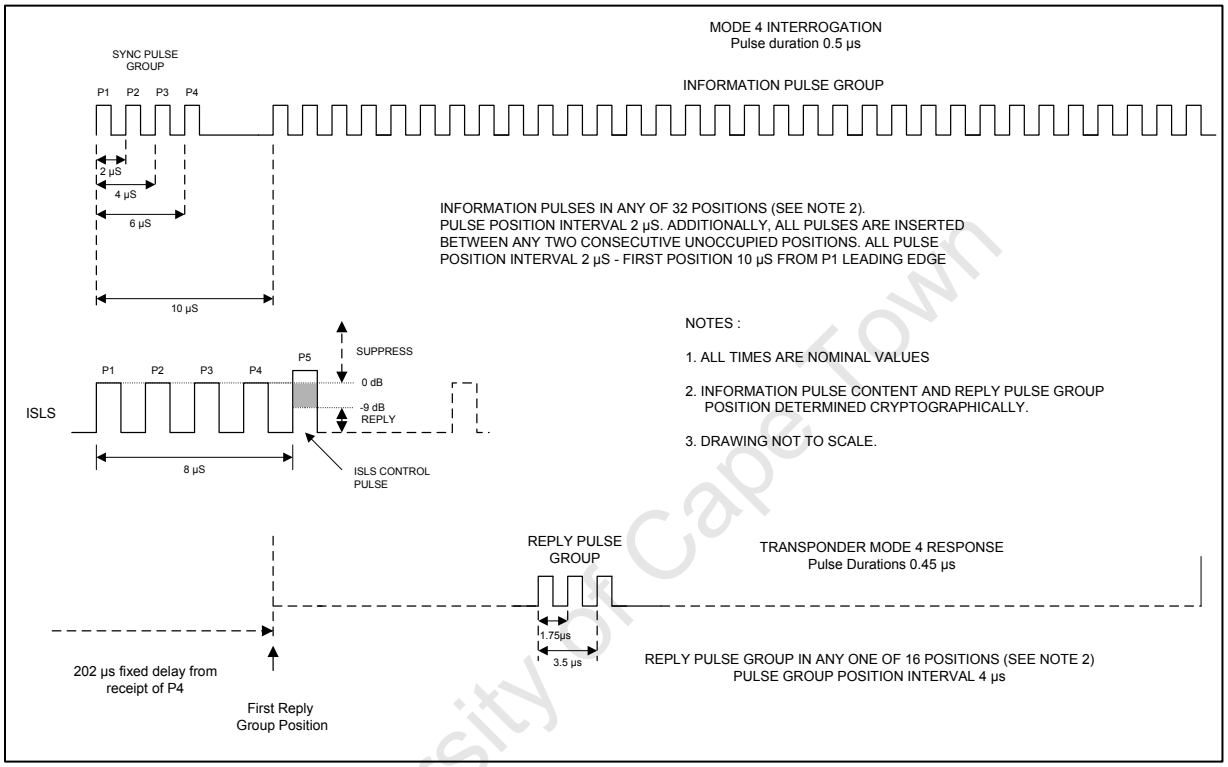


Figure 12: Mode 4 interrogation and reply timing characteristics [7].

3.2.3 Real-time Operation

The SSR/IFF system operates in real-time mode. When a transponder receives an interrogation, it has to reply to that interrogation within a certain time. According to STANAG-4193 [7], the time between receiving interrogation pulse P3 and generating the first framing pulse F1 of a transponder reply in mode 1, 2, 3/A and C should be 3 ± 0.5 µs. For mode 4, the interval between receiving the P4 interrogation pulse and generating the first pulse of the first reply group position should be 202 ± 1.25 µs.

3.2.4 Built-in Test Subsystem (BIT)

The performance of the ITRC is defined by its ability to identify and generate SSR/IFF STANAG-4193 compliant signals. The ITRC should be able to transmit predefined simulated SSR/IFF interrogations or replies and to route them back to the receiver to be analysed and verified. The isolation between the transmitter and receiver should not be affected by the loopback path. The Built-In Test (BIT) subsystem should enable the measurement of Forward Power and Reverse Power to and from the load connected to the ITRC.

3.2.5 Hardware Interface

According to Section 2.3 of the user requirements, the Innovative Integration Quixote board [9] must be used in the design and implementation of the digital section of the project.

The ITRC should be able to down-convert received IFF RF signals to IF signals at 70MHz before passing them on to the Quixote's Analogue-to-Digital Converter (ADC). The Quixote board must provide the ITRC with the TTL signals required to generate IFF RF pulses, which must be transmitted within certain time limits. The input/output signals must be made available from/to the ITRC via the input/output pins of the Quixote board.

3.3 ITRC Requirements

The following are the ITRC transmitter and receiver requirements, which have been derived from analysing the ITRC user requirements and the ITRC subsystems.

3.3.1 ITRC Transmitter Requirements

3.3.1.1 Transmitted Interrogation and Reply Signals

The ITRC is required to generate SSR/IFF interrogation pulses compatible with STANAG-4193 [7] in modes 1, 2, 3/A, C and mode 4. The timing characteristics of these pulses should comply with the timing requirements set out in Table 1, and the pulse

interval value should correspond to the values in Figure 6 and Figure 7, depending on the mode of operation.

The ITRC is also required to generate SSR/IFF reply pulses that are compatible with STANAG-4193 [7] in modes 1, 2, 3/A, C and mode 4. The timing characteristics of these pulses should comply with the timing requirements set out in Table 3, and the pulse interval value should correspond to the values in Figure 11 and Figure 12, depending on the mode of operation.

According to Section 2.1.6, the ITRC is required to transmit SSR/IFF interrogations and replies to targets located at any distance between 10 metres and one kilometre targets. Due to the short distance testing requirement, the ITRC does not need to generate P1, P2 and P3 of interrogation from two different antennas, which is described in Section 3.2.1.2. The ITRC as an interrogator must be able to generate a signal encompassing all the three pulses with P2 having a variable amplitude. Depending on the generated value of P2, the transponder under test will receive interrogations, whether as a target in the interrogate beam or as a target in a side-lobe. The fast switching time between the three pulses should be considered during the design phase.

3.3.1.2 Targets Generation

The ITRC must be able to generate normal replies from up to 1500 targets per antenna rotation. Garbled and FRUIT replies must be generated from up to four targets to test the interrogator's ability to de-garble and identify false replies.

In order to generate SSR/IFF interrogation and reply pulses, the ITRC should use the Pulse Amplitude Modulation (PAM) format with an on/off keying ratio of not less than 40 dB. The RF switching between the pulses must be fast enough to achieve the allowed time interval between the pulses.

Pulse amplitude modulation is a pulse modulation technique in which the amplitude of the pulse carrier is varied according to the input signal amplitude.

3.3.1.3 Transmitted Signal Centre Frequency

In compliance with STANAG-4193 [7], the ITRC should be able to transmit the generated interrogations at a frequency of 1030 ± 0.2 MHz and the generated replies at a frequency of 1090 ± 0.5 MHz.

3.3.1.4 Transmitter Output Power

According to the user requirements in Chapter 2, the ITRC is required to transmit SSR/IFF interrogations and replies to targets located at any distance between 10 metres and one kilometre. In order to satisfy these requirements, the output power measured at the ITRC output should not be more than +25 dBm (the maximum input power to a transponder or an interrogator located at 10 meters from the ITRC) and not less than +7 dBm (the minimum input power to a transponder or an interrogator located at 1000 meters from the ITRC). These values have been estimated by using the following equation [2]:

$$\boldsymbol{Pt} = \frac{\boldsymbol{Pr}}{\boldsymbol{Gt} \,.\, \boldsymbol{Gr} \,.\, [\boldsymbol{\lambda}/(\boldsymbol{4\pi R})]^{\boldsymbol{2}}}$$

Where:

$\boldsymbol{Pt}$ is the power level in watts at the transmitting antenna input.

$\boldsymbol{Pr}$ is the power level in watts at the receiving antenna input. For a transponder or an interrogator to be able to process received replies and interrogations, the received signal level should be within the range -22 dBm to -80 dBm. This is in compliance with STANAG-4193 [7].

$\boldsymbol{Gr}$ and $\boldsymbol{Gt}$ are the antenna gain of the transmitting and receiving antennas, respectively. It is assumed that the gain of both transmitting and receiving antennas equals +3 dB.

$\boldsymbol{\lambda}$ is the wavelength in meters (0.283m), which can be calculated by the following equation:

$$\lambda = c/f$$

Where c is the constant value for the speed of light ($3\ x\ 10^8$ m/s), and f is the frequency in Hz, which is assumed to be the average of the two SSR/IFF frequencies (1060 MHz).

R is the distance between the two antennas in meter. The minimum range is 10 meters and the maximum is 1000 meters.

3.3.1.5 Real-time Operation

As described in Section 3.2.3, the ITRC is required to respond to received interrogations within a certain time limit. Thus, the switching between the ITRC transmitter and receiver should be fast enough to meet this requirement.

3.3.2 ITRC Receiver Requirements

3.3.2.1 Received Interrogation and Reply Signals

When the ITRC is acting as an interrogator, it should accept replies in mode 1, 2, 3/A and C only if the pulse duration and the pulse interval with respect to the first framing pulse are within ±0.15 μs of the nominal values. For mode 4 replies to be accepted, the pulse intervals with respect to the first reply pulse should be within ±0.1 μs of the nominal values. This is in compliance with STANAG-4193 [7].

When the ITRC is acting as a transponder, it should accept interrogations in mode 1, 2, 3/A and C only if the pulse duration of P1 and P3 and the pulse interval between them are within ± 0.1 μs of the nominal values. For mode 4 interrogations to be accepted, the nominal pulse intervals of the sync pulse group should be multiples of 2 μs with respect to P1, and the pulse interval tolerance should be ±0.05μs. These specifications are in compliance with STANAG-4193 [7].

3.3.2.2 Received Signal Analysis

As test equipment, the ITRC tests only one transponder at a time, and is not required to analyse garbled or FRUIT replies. As an interrogator, the ITRC should respond only to normal replies and ignore any other kind of replies.

3.3.2.3 Received Signal Centre Frequency

The ITRC should be able to detect and analyse SSR/IFF interrogations and replies at a frequency of 1090 ± 0.5 MHz and 1030 ± 0.5 MHz, respectively. This is in compliance with STANAG-4193 [7].

3.3.2.4 Receiver Sensitivity

Sensitivity in a receiver is defined as the minimum input signal the receiver can process to provide usable information at the output. Normally, the receiver must be sufficiently highly sensitive to detect and process weak signals coming from long-range targets. However, as the ITRC will be designed to operate as short-distance test equipment, it is only required to be capable of processing signals received from targets located at a maximum distance of one kilometre.

3.3.2.5 Receiver Dynamic Range

The dynamic range of a receiver is defined as a measure of the ratio between the strongest and weakest input signal that the receiver can handle. The dynamic range of the ITRC receiver should be within the range 40 ± 2dB. This value has been derived from the following equation [2]:

$$\boldsymbol{Pr} = \boldsymbol{Pt} \,.\, \boldsymbol{Gt} \,.\, \boldsymbol{Gr} \,.\, [\boldsymbol{\lambda}/(\boldsymbol{4\pi R})]^{\boldsymbol{2}}$$

Where:

$\boldsymbol{Pr}$ is the power received at the antenna connected to the ITRC.

$\boldsymbol{Pt}$ is the power transmitted by the antenna connected to the IFF equipment under test. According to STANAG-4193, the average output power of the SSR/IFF transponder is around 500W, while the output power of the SSR/IFF interrogator is 0 to 2kW. A common 500W has been used in this calculation.

$\boldsymbol{Gr}$ and $\boldsymbol{Gt}$ are the antenna gain of the transmitting and receiving antennas, respectively. It is assumed that the gain of both transmitting and receiving antennas equals +3 dB.

$\boldsymbol{\lambda}$ is the wavelength in meters (0.283m), as calculated in Section 3.3.1.4

$\boldsymbol{R}$ is the distance between the two antennas in meters. The minimum range is 10 meters and the maximum is 1000 meters.

The minimum and maximum signal powers the ITRC can handle are -30 dBm and +10 dBm, respectively. Therefore, the dynamic range of the receiver is the difference between the minimum and maximum values.

3.3.2.6 Receiver Bandwidth

The receiver bandwidth is a measure of how well it passes in-band signals. The receiver bandwidth should be limited to passing replies and interrogations pulses and to rejecting out-of-band noise. Filters should be used in both RF and IF parts of the receiver to block signals at the image frequency.

3.4 Summary

This chapter presented a breakdown of the ITRC system, based on analysing the user requirements described in Chapter 2. The capabilities of the SSR/IFF target emulator, which will be used to provide the ITRC with TTL SSR/IFF replies, were summarised in this chapter. It also included a concept study for each of the ITRC subsystems, which led to the ITRC requirements. Based on the information presented herein, the following chapter describes the design of the ITRC, and it covers the changes made to the SSR/IFF emulator in order to meet the ITRC requirements.

4 ITRC System Design

The overall goal of this project is to create a transceiver that is capable of generating and processing SSR/IFF signals at 1030MHz and 1090MHz. The system specifications are derived from the requirements discussed in Chapter 3. The description of the ITRC system design in this chapter consists of two main parts, viz. the analogue design and the digital design.

The first part defines and describes the subsections that make up the ITRC architecture of the analogue part, summarising the purposes of each subsection and presenting the relevant design parameters. The ITRC transceiver, as illustrated in Figure 9, consists of front-end circuitry (Section 4.1), a transmitter (Section 4.2), a receiver (Section 4.3) and an interface to the power supply and to the digital board (Section 4.4).

These subsections are simulated using Agilent *Genesys* software [11], in order to gauge the minimum output power of the system stages and to ensure that the power levels are compatible with the user requirements. At the end of each subsection, a table summarizes the main components used. Schematics created for the ITRC analogue part, using *Altium Designer* software [12], are illustrated in Appendix A.

The second part of this chapter (Section 4.5) introduces the *Quixote* digital board, which has been used to run the IFF Reply Emulator as well as the digital section of the ITRC. A brief overview of the emulator design concept is given too. The design of the ITRC IFF emulator interface and other digital related issues are described in detail.

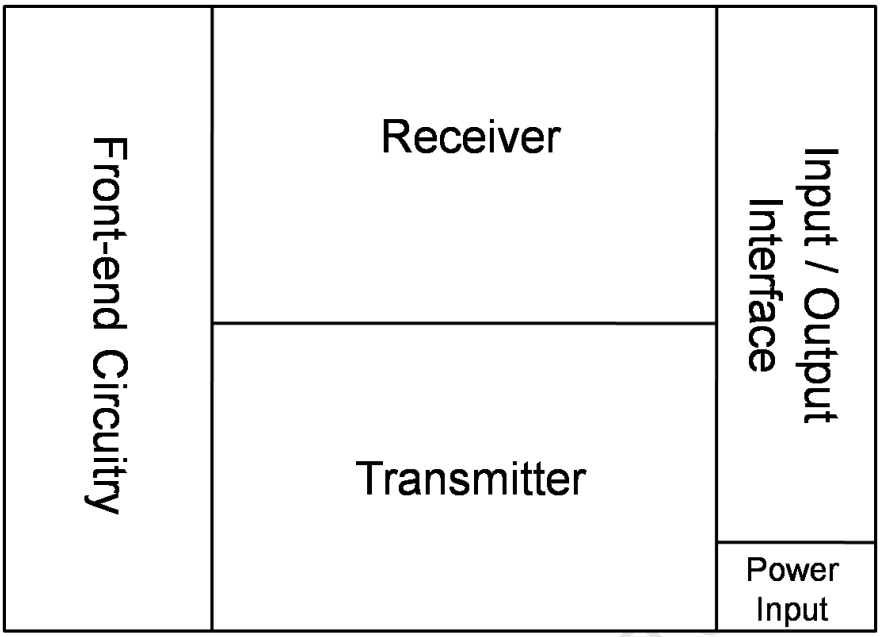


Figure 9: ITRC System Architecture.

4.1 ITRC Front-end Design

Based on the ITRC requirements, which were discussed in the preceding chapter, the front-end circuitry was designed to perform the following functions:

- Attenuate out-of-band signals and harmonics of transmitted and received signals.
- Enable the ITRC to switch between the receiver and the transmitter and provide high isolation between them.
- Facilitate the implementation of system level built-in test functions, such as transmitted power measurement, Voltage Standing Wave Ratio (VSWR) measurement and transmitted signal loopback testing.

4.1.1 ITRC Front-end Structure

Figure 10 below shows the ITRC front-end block diagram. Sections (4.1.1.1) to (4.1.1.4) discuss the design parameters of the ITRC front-end.

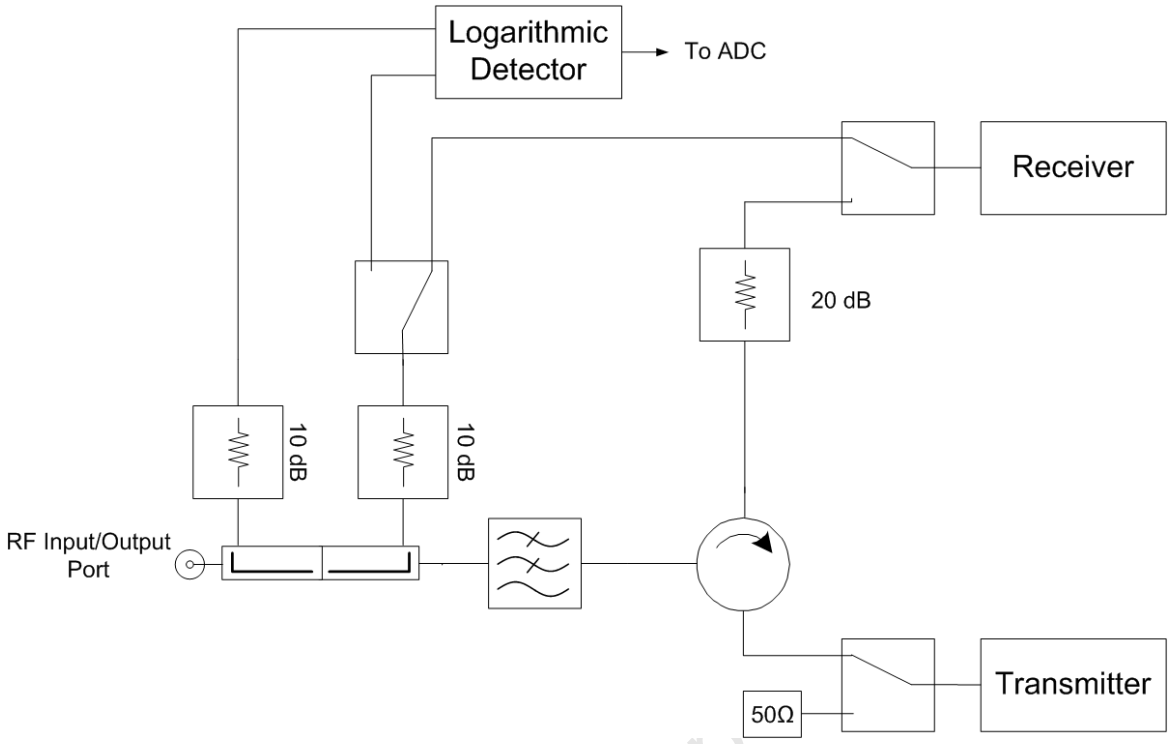


Figure 10: ITRC Front-end Block Diagram

Genesys was used to simulate the ITRC front-end, as illustrated in Figure 11, based on the specifications of the real components that were chosen to build the ITRC front-end. Figure 12 shows the maximum power level the receiver is able to process.

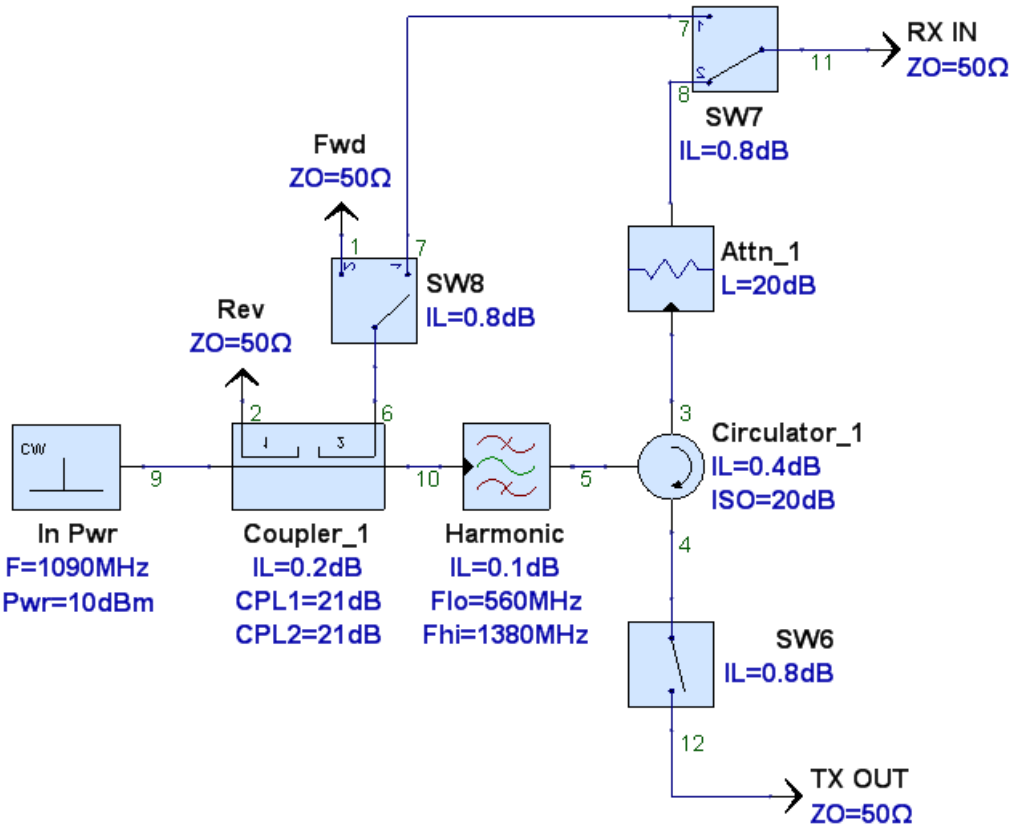


Figure 11: Simulation of the real components of the ITRC front-end using Genesys.

4.1.1.1 RF Switch

As seen in Figure 10, the ITRC front-end section uses three Single Pole Double Throw (SPDT) switches, which need to be switched simultaneously. The input signal applied at the RFC port, the common port, can be routed through RF1 or RF2. The switch can also be set in the "all off" state, which isolates RF1 and RF2 from RFC by connecting them to embedded 50 ohm resistors.

The switch was selected due to its fast switching, low insertion loss, high isolation (about 70 dB), and high P1dB compression point (+32 dBm). The switching states are controlled via two TTL signals (*Vctl* and *EN*) coming from the digital side of the ITRC. The switch states, which have been adapted from the component datasheet, are listed in Table 4 below.

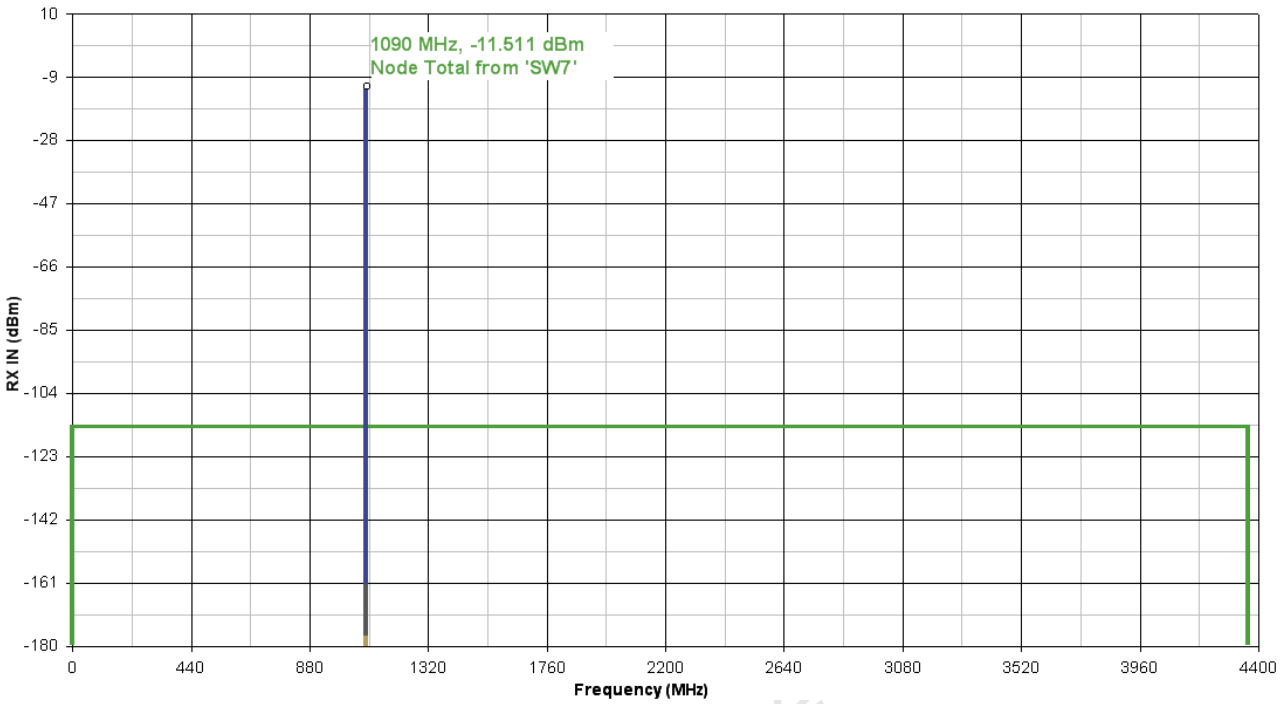


Figure 12: ITRC receiver input power at 1090 MHz. The plot shows that the maximum power at the receiver input is about -11.5 dBm.

Table 4: SPDT Switch Truth Table.

Control Input		Signal Path State	
Vctl	EN	RFC – RF1	RFC – RF2
Low	Low	OFF	ON
High	Low	ON	OFF
Low	High	OFF	OFF
High	High	OFF	OFF

The switches are used to switch between transmitting and receiving functions as well as to provide high isolation between the transmitter and the receiver channels, as described in Section 4.1.1.4.

4.1.1.2 Harmonic Filter

A 7th order Chebyshev filter is incorporated into the front-end of the ITRC to suppress unwanted harmonic frequencies from the transmitter, and in turn to attenuate high frequency spurious signals before they reach the receiver input.

Harmonic filter rejection criteria, summarised in Table 5 below, are derived from one of the user's documents.

Table 5: Harmonic filter pass-band and stop-band specifications.

Pass-band	Insertion loss over 1.03 to 1.09GHz band	≤ 0.4dB
	Lower 3dB point	560±10MHz
	Upper 3dB point	≥ 1380±10MHz
	Ripple over 3dB Band	≤ 0.2dB
Stop-band	Rejection @ 400MHz	≥ 20dB
	Rejection of higher order 1030MHz Harmonics	≥ 60dB

The following equation is used to calculate the centre frequency [13]:

$$f_o = \sqrt{f_a \cdot f_b (MHz)}$$

Where:

f_o is the centre frequency.

f_a and f_b are any two frequencies (one above and one below the passband) having equal attenuation.

Therefore, using the 3-dB lower and upper frequencies from Table 5, the centre frequency equals 879 MHz. The previous equation can be used again to calculate the lower frequency (f_1) at 60 dB of attenuation.

$$879\ MHz = \sqrt{2060\ x\ f_1 (MHz)} \quad \rightarrow \quad f_1 = 375\ MHz$$

Now the ratio of the bandwidth of interest to the 3-dB bandwidth can be calculated using the following equation:

$$\frac{BW_{40dB}}{BW_{3dB}} = \frac{2060 - 375}{1380 - 560} = 2.05$$

Figure 13 shows that a 7th order filter can be designed to satisfy the filter requirements.

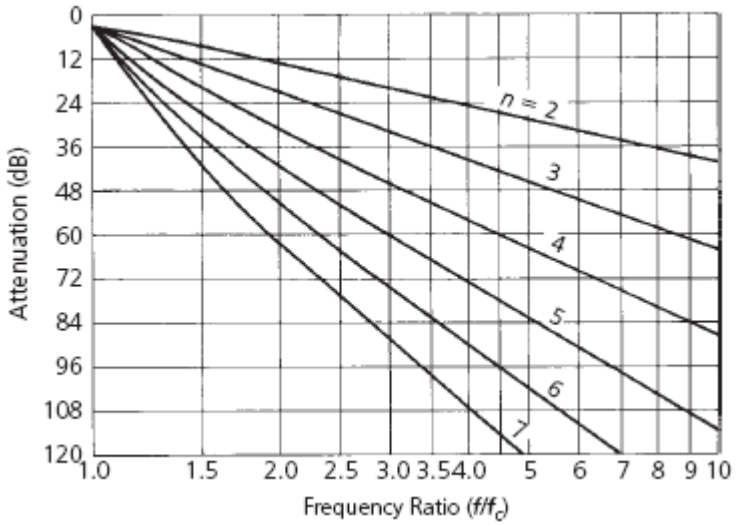


Figure 13: Attenuation characteristics for a Chebyshev filter with 0.1 dB ripple [13].

The simulation of the filter and its response are shown in Figures 14 and 15, respectively.

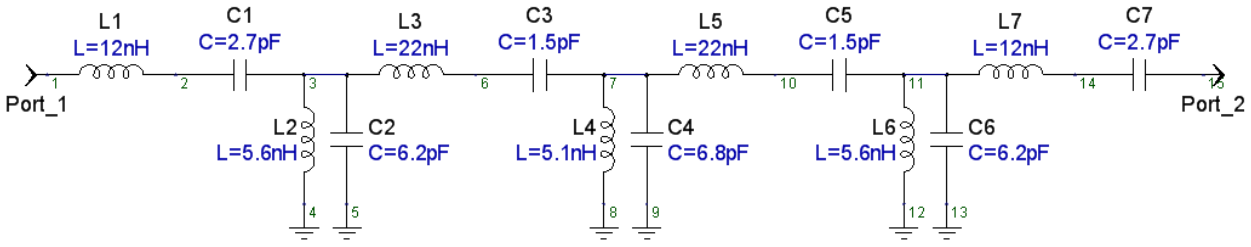


Figure 14: 7th order Chebyshev filter schematic.

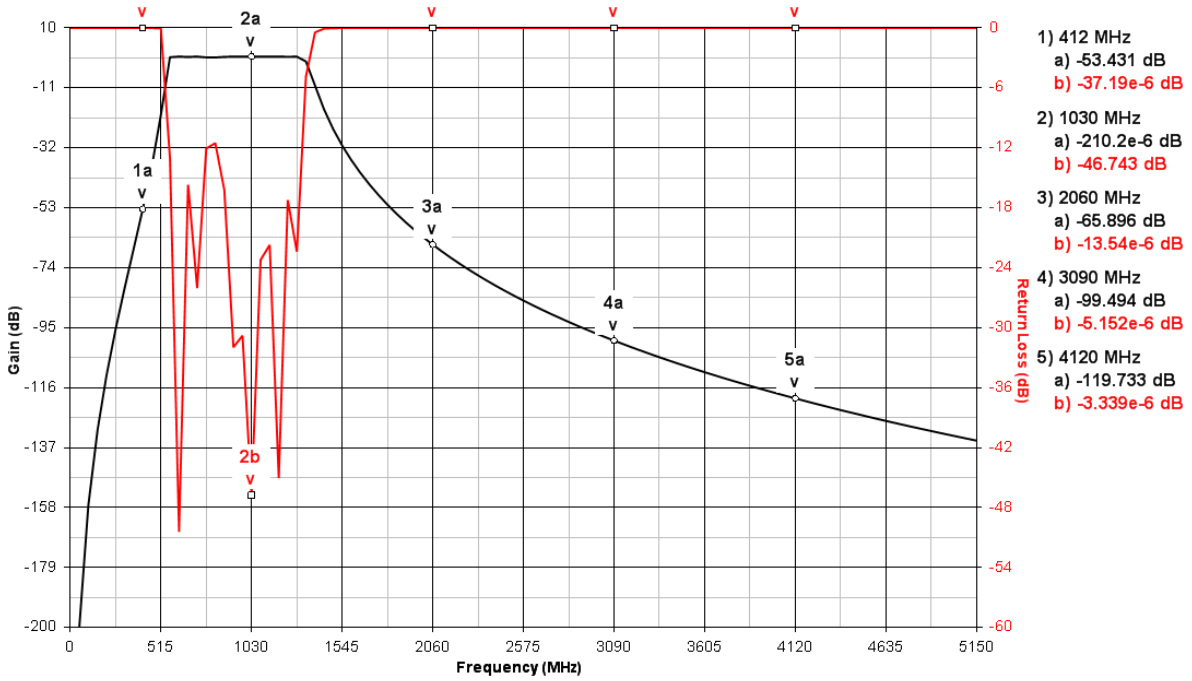


Figure 15: The response of the 7th order Chebyshev filter.

4.1.1.3 VSWR Measurement

The VSWR in a transmission line is the ratio of the maximum to minimum voltage. It can be calculated using the following equation:

$$VSWR = \frac{|1+\rho|}{|1-\rho|}$$

Where ρ is the reflection coefficient, which is the magnitude of the reflected power relative to the incident power.

The VSWR measurement is an indicator of the quality of the matching between the ITRC and the load connected to it. The smaller the VSWR is, the better the load is matched to the ITRC and the more power is delivered to the load.

As seen in Figure 10, a dual directional coupler is used to measure the transmitted and reflected power levels. A high dynamic range dual logarithmic detector is used to receive the two signals and provide a direct reading of the return loss. Two 10 dB attenuators are used at the input of the detector, as recommended by the manufacturer.

4.1.1.4 Transmitter/Receiver Isolation

Since the ITRC transmitter and receiver are using the same frequencies, high isolation is required to avoid power leakage from the transmitter to the receiver or vice versa. When the ITRC is transmitting, the receiver is protected by more than 80 dB of isolation, which is provided by the circulator, the 20 dB attenuator and the switch at the input of the receiver (see Figure 16). Similarly, when the ITRC is receiving, the transmitter is also protected by more than 80 dB of isolation, which is in this case provided by the circulator and the switch connected to the transmitter output (see Figure 17).

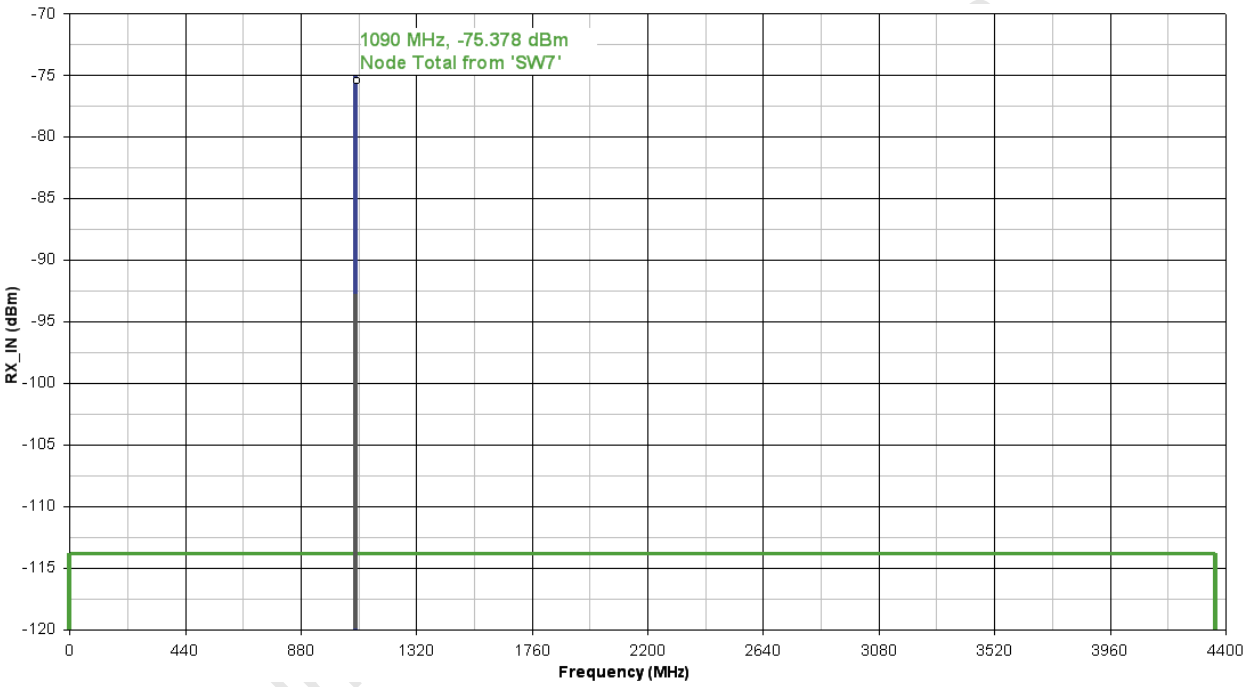


Figure 16: The signal power level at the receiver input. When the ITRC transmits at 10 dBm, the power level of the signal leaked to the receiver is attenuated by more than 80 dB.

4.1.2 Front-end Components

Table 6 summaries the front-end components of the ITRC.

Table 6: Components of the ITRC Front-end.

Component Type	Manufacturer	Part Number
SPDT RF Switch	Hittite	HMC349MS8G

Circulator	Nanjing Guangshun	TH101-S1
Dual Directional Coupler	Mini-Circuits	ZX30-20-20BD+
Dual Logarithmic Detector	Analog Devices	ADL5519
20 dB attenuator	Telegartner	J01156A0041
Harmonic Filter	Designed by the author	

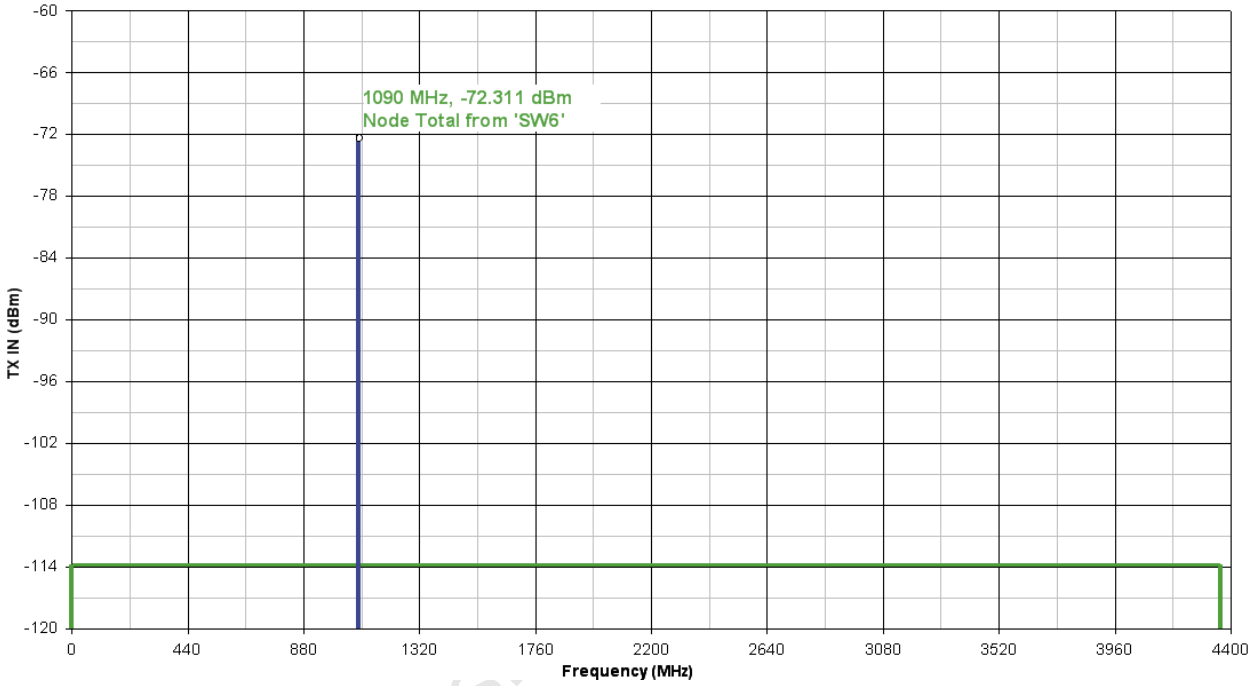


Figure 17: The signal power level at the transmitter output. When the ITRC receives signals at 10 dBm, the power level of the signal leaked to the transmitter is attenuated by more than 80 dB.

4.2 ITRC Transmitter Design

The ITRC transmitter requirements were discussed in the previous chapter. The transmitter was designed to achieve the following functions:

- Generate SSR/IFF interrogations and replies at 1030 MHz and 1090 MHz, respectively, in modes 1, 2, 3/A, C and mode 4.
- Generate normal, garbled and FRUIT replies in all the previous modes.

- Transmit signals at different power levels up to +18 dBm. There is no need to test the maximum input power (+25 dBm) of an IFF equipment, which was discussed in Section 3.3.1.4. Thus, a lower value (+18 dBm) has been chosen to be the maximum output power.

4.2.1 Transmitter Structure

Figure 18 shows the ITRC transmitter block diagram. The transmitter is made up of a synthesizer, switches, filters, an amplifier and a variable attenuator. The synthesizer can be programmed to generate an RF signal at 1030MHz or 1090 MHz, depending on the required function. The synthesizer output is connected to a SPDT switch, which changes between ON and OFF states, based on TTL signals coming from the digital board. The variable attenuator is then used to reduce the amplitude of the generated pulses. The previous three components together perform the required pulse amplitude modulation. The generated signal passes to the front-end circuitry through a process of RF filtering and amplification.

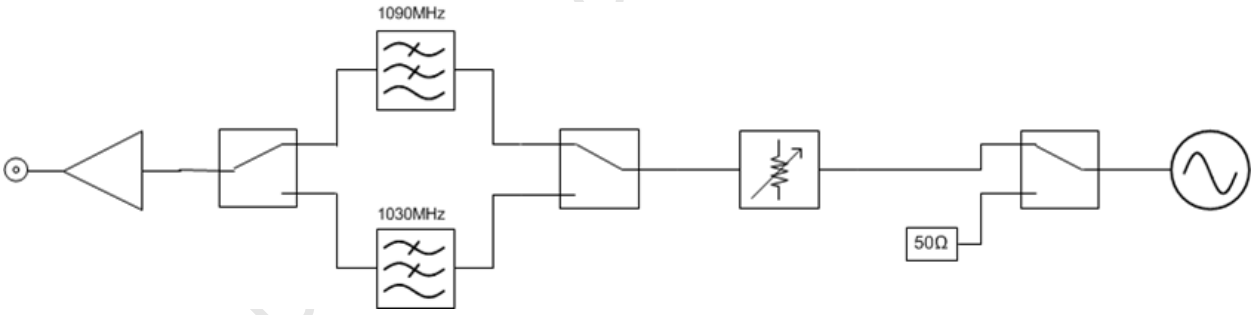


Figure 18: ITRC Transmitter Block Diagram.

Genesys was used to simulate the ITRC transmitter, as illustrated in Figure 19, based on the specifications of the real components that were chosen to build the ITRC transmitter. A summary of these components is given in Table 7.

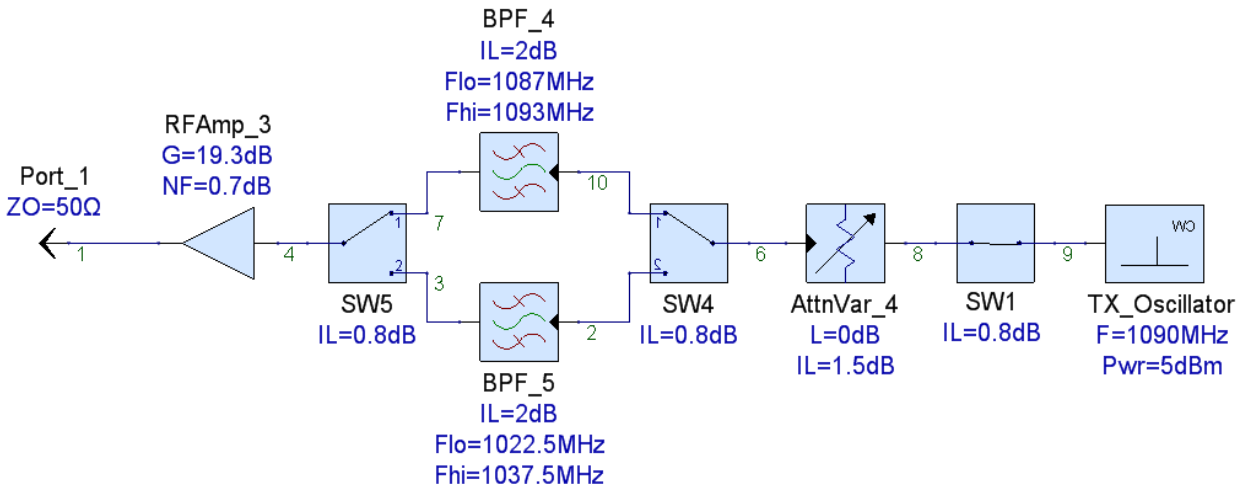


Figure 19: Simulation of the real components of the ITRC transmitter using Genesys.

The Continuous Wave (CW) source in this simulation represents the synthesizer, which generates +5 dBm signals at 1090 MHz. The variable attenuator loss value is set to zero to simulate the transmitter maximum output power. As seen in Figure 20, the maximum output power of the simulated transmitter at 1090 MHz is +17.5 dBm.

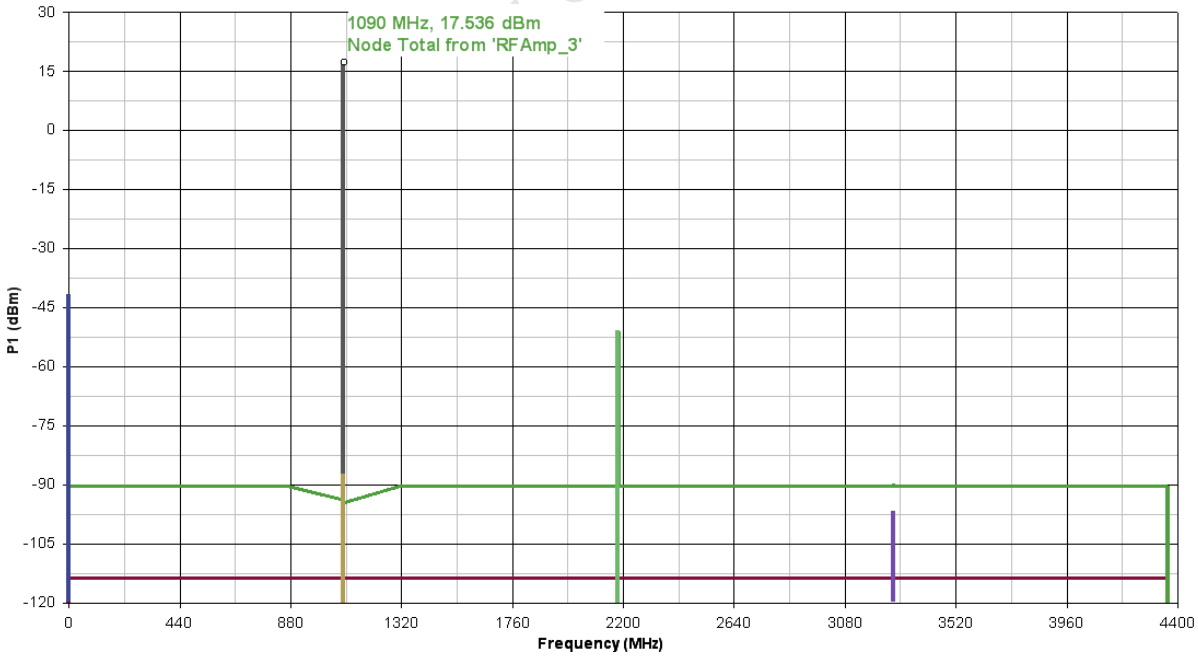


Figure 20: ITRC transmitter output power at 1090 MHz. The plot shows that the maximum power at the transmitter output is about +17.5 dBm.

4.2.1.1 Synthesizer

The component used to generate the 1030 MHz and 1090 MHz frequencies is an integer-N synthesizer and Voltage Control Oscillator (VCO) that operates in a wide-band frequency range. A 3-wire serial interface is used to write to the device. A 40 MHz crystal oscillator with a high degree of frequency stability drives the reference input of the synthesizer.

As per the synthesizer datasheet, the centre frequency is set by two external inductors. The value of these inductors can be calculated using the following equation:

$$f_o = \frac{1}{2\pi\sqrt{6.2\ pF\ (0.9\ nH + L_{ext})}}$$

Where:

f_o is the centre frequency.

L_{ext} is the external inductance.

A balun filter is used to combine the synthesizer to outputs and to increase the output power. A loop filter is also used to keep the synthesizer stable and to filter the unwanted spurs.

4.2.1.2 Variable Attenuator

A 6-bit digital attenuator covering a 31.5 dB attenuation range in 0.5 dB steps was used to control the ITRC transmitter output power level. The attenuator was chosen due to its fast switching speed, high attenuation accuracy, low insertion loss and the high power output at the 1 dB compression point.

4.2.1.3 Filters

The purpose of the RF filter is to reject unwanted out-of-band signals. Two ceramic band pass filters (BPF) with very narrow bandwidth are used in the transmitter channel to attenuate the signals outside the passband and to reduce the noise level at the RF amplifier input. The transmitter switches between the two filters based on the

transmitting frequency, i.e. whether it is 1030 MHz or 1090 MHz. Figure 21 below shows the RF filter performance.

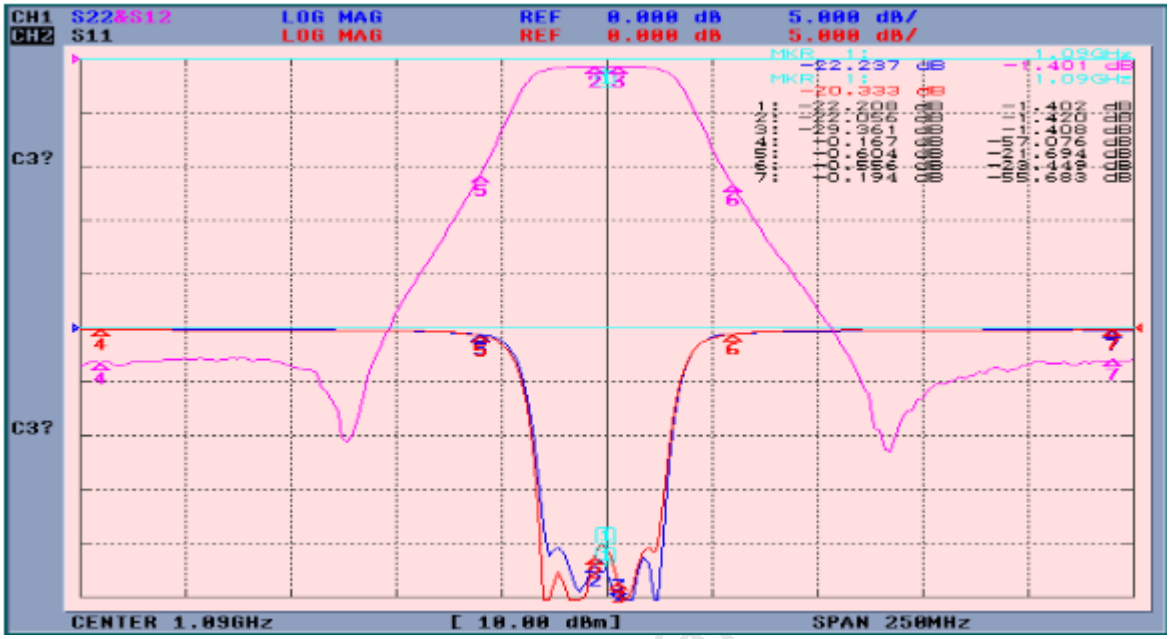


Figure 21: RF filter performance graph at centre frequency of 1090 MHz [adapted from the component datasheet].

4.2.1.4 Low Noise Amplifier

An RF Low Noise Amplifier (LNA) is used at the end of the transmitter channel to amplify the filtered RF signal. The chosen amplifier offers high linearity, high gain and a low noise figure. The high gain ensures that the transmitter is able to generate the required maximum power, whereas the high linearity keeps the amplifier output signal in direct proportion to the input signal.

4.2.2 Transmitter Power Levels

Figure 22 below shows the minimum and maximum power at each stage of the ITRC transmitter. It can be seen that the transmitter is capable of generating signals between -13 dBm and +17.5 dBm.

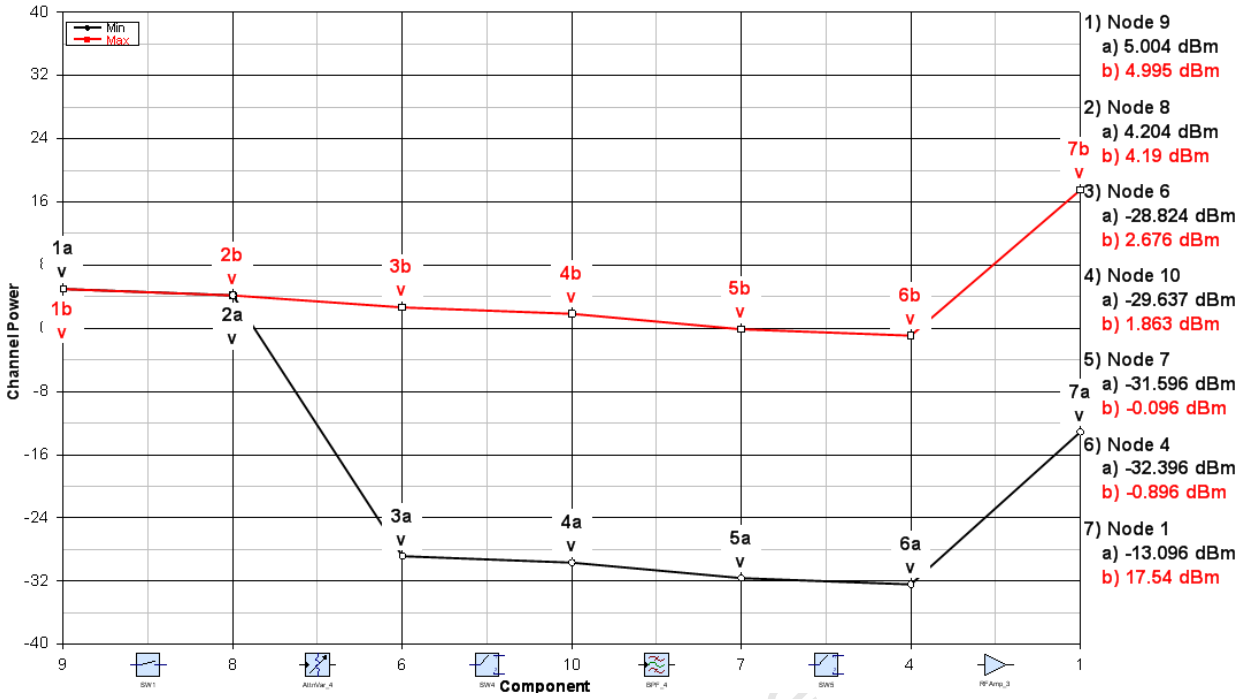


Figure 22: Minimum and maximum power levels at each stage of the ITRC transmitter.

4.2.3 Transmitter Components

Table 7 summaries the components used to build the transmitter section of the ITRC.

Table 7: Summary of ITRC Transmitter Components.

Component Type	Manufacturer	Part Number
SPDT RF Switch	Hittite	HMC349MS8G
1030 MHz RF Filter	ECHO Microwave	EMA8F1030P6D20A
1090 MHz RF Filter	ECHO Microwave	EMA8F1090P6D20A
Variable Attenuator	Hittite	HMC472LP4
Synthesizer	Analog Devices	ADF4360-7
Crystal Oscillator	Cardinal	LF-TVXO009920
RF Amplifier	Avago Technologies	MGA-62563

4.3 ITRC Receiver Design

Based on the ITRC requirements analysis, which was completed in Chapter 3, the receiver was designed to achieve the following functions:

- Detect and analyse SSR/IFF interrogations and replies at 1030MHz and 1090 MHz, respectively, in modes 1, 2, 3/A, C and mode 4.
- Process signals coming from targets at a maximum distance of one kilometre.

4.3.1 Receiver Structure

The ITRC receiver block diagram is shown in Figure 23. The receiver channel consists of switches, filters, amplifiers, a synthesizer and a mixer. The switches and filters circuitry is similar to that of the transmitter channel, and it is responsible of filtering the received signal based on the applied test function. The RF amplifier amplifies the received signal and passes it to the frequency mixer. The mixer down-converts the received RF signal to 70 MHz by combining it with another signal generated by the synthesizer. The down-converted signal passes to the digital board through a process of IF filtering and amplification.

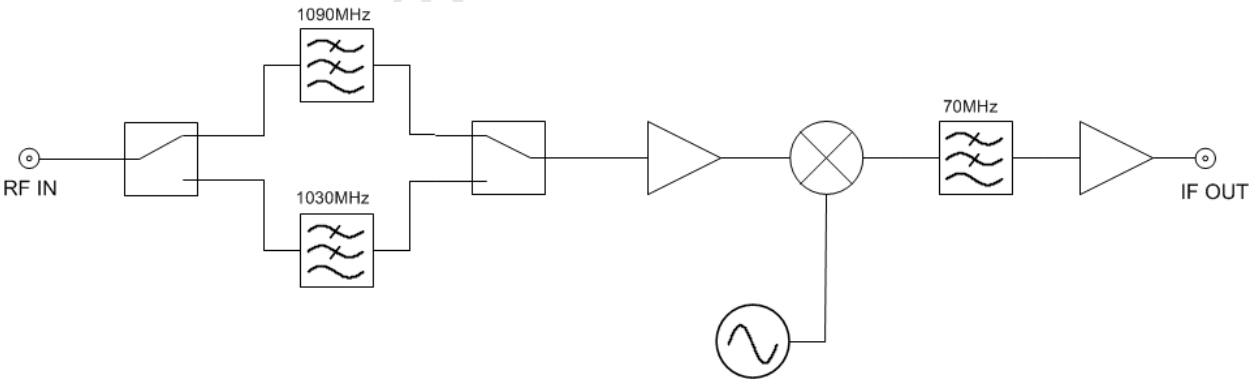


Figure 23: ITRC Receiver Block Diagram.

Genesys was used to simulate the ITRC receiver, as illustrated in Figure 24, based on the specifications of the real components that were chosen to build the ITRC receiver. A summary of these components is given in Table 8.

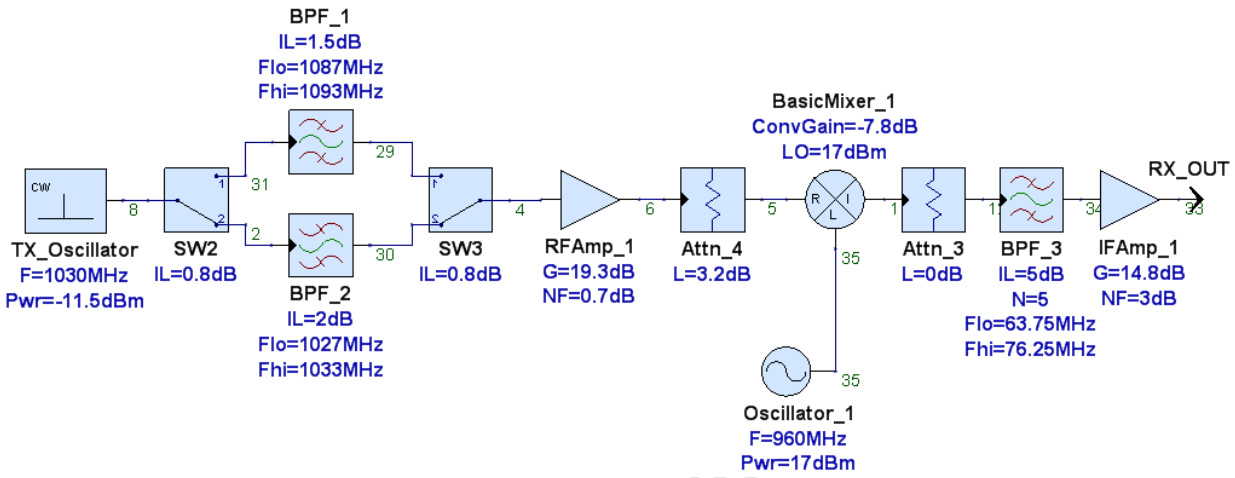


Figure 24: Simulation of the real components of the ITRC receiver using Genesys.

The Continuous Wave (CW) source in this simulation, which generates -11.5 dBm signals at 1030 MHz, represents the maximum input signal. The variable attenuator loss value is set to zero to simulate the transmitter maximum output power. As seen in Figure 25, the maximum power of the IF output signal at 1030 MHz is +1 dBm.

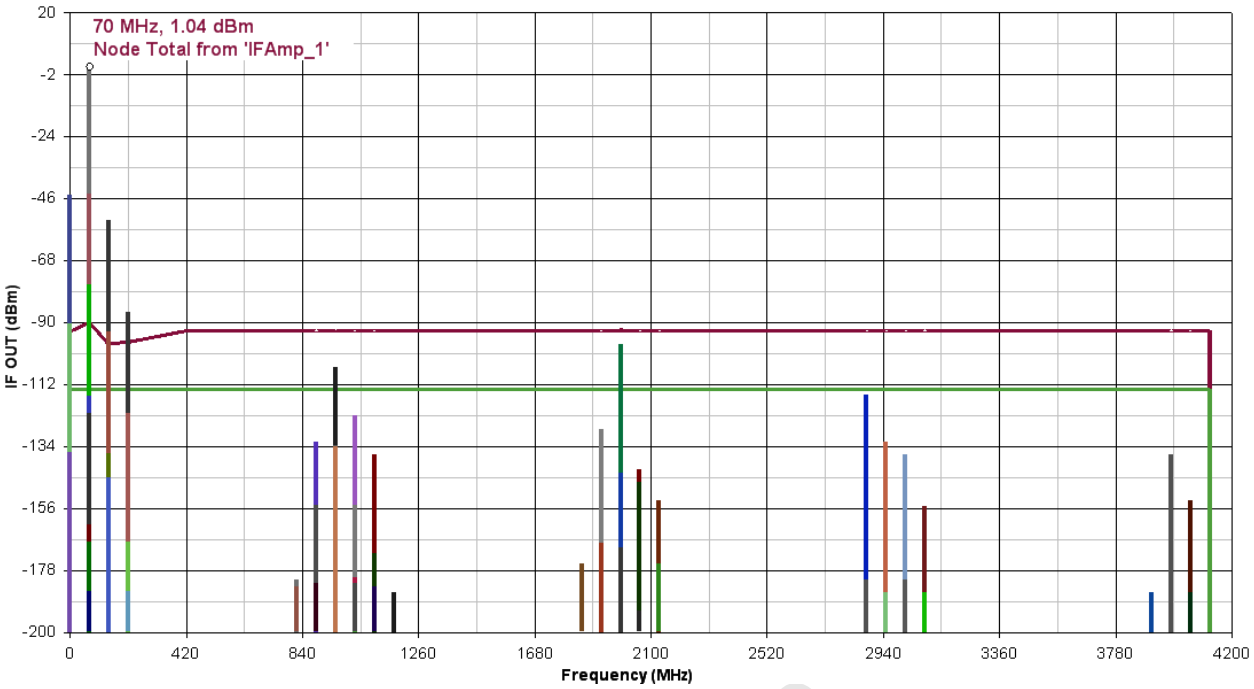


Figure 25: ITRC receiver output power at 70 MHz. The plot shows that maximum power at the receiver output is about +1 dBm.

4.3.1.1 Filters

The same ceramic RF filters used in the transmitter are used at the input of the receiver to limit the band of the incoming signal and minimize the input noise. The receiver switches between the two filters, depending on the receiving frequency of 1030 MHz or 1090 MHz. The output of the mixer is filtered by an IF band pass filter with a narrow bandwidth. Figure 26 below shows the performance of the IF filter.

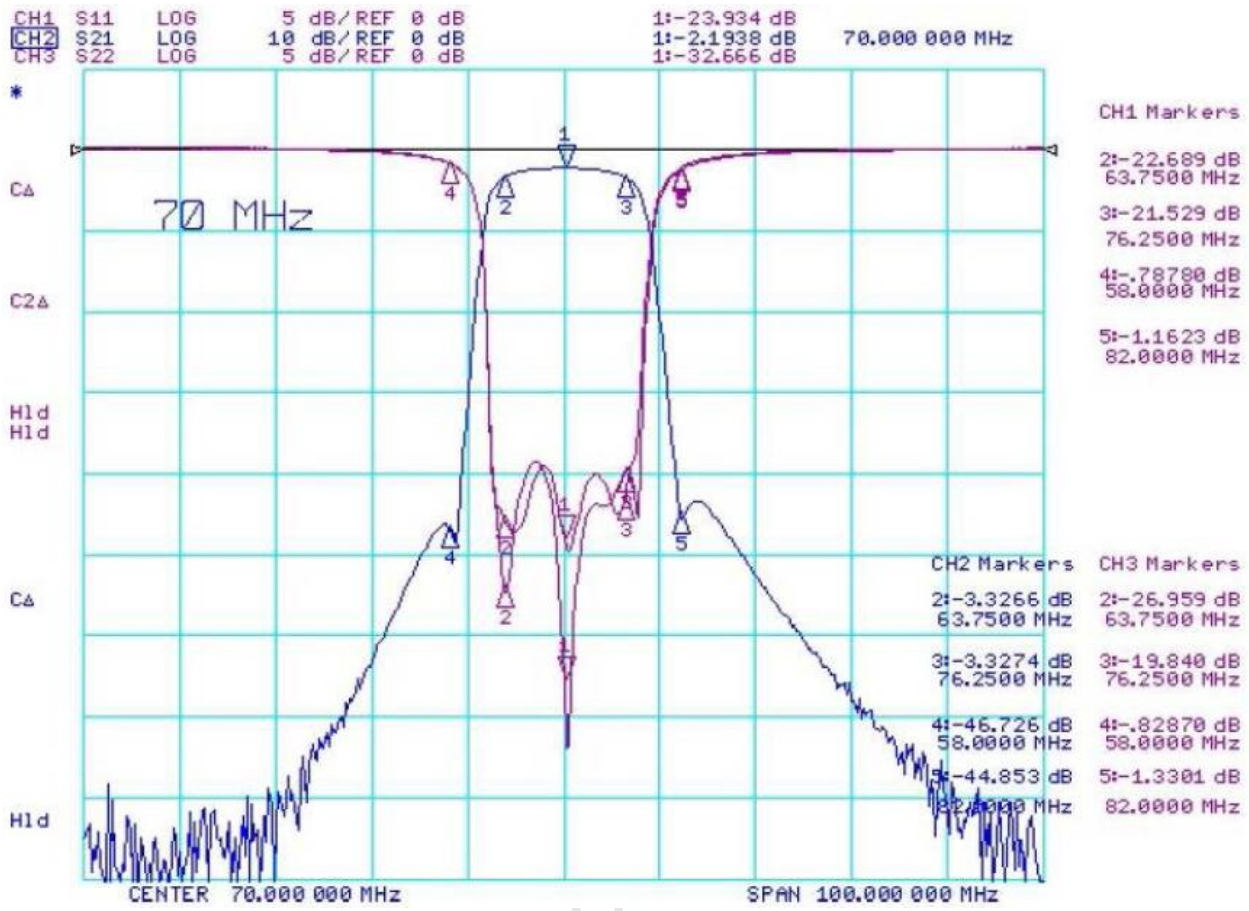


Figure 26: IF filter performance graph at centre frequency of 70 MHz [adapted from the component datasheet].

4.3.1.2 Synthesizer

The ITRC receiver is designed with a synthesizer similar to the one used in the transmitter channel. The receiver synthesizer can be programmed to generate 960 MHz and 1160 MHz to keep the IF output at 70 MHz.

4.3.1.3 Mixer

In a receiver, a frequency mixer is used to convert an RF frequency to a lower IF frequency by combining the frequency of the received signal with another frequency generated by a local oscillator connected to the mixer.

The mixer always generates the sum and the difference of the mixed frequencies. The local oscillator and its harmonics are mixed with each input signal to produce both sum and difference frequencies. The IF filter is used to reject image signals and unwanted harmonics. The receiver mixer has been chosen due to its low conversion loss, its high third order intercept point and the high isolation between the mixer ports. Figure 27 shows that the local oscillator generates different frequencies, depending on the received signal frequency, to keep the IF frequency constant.

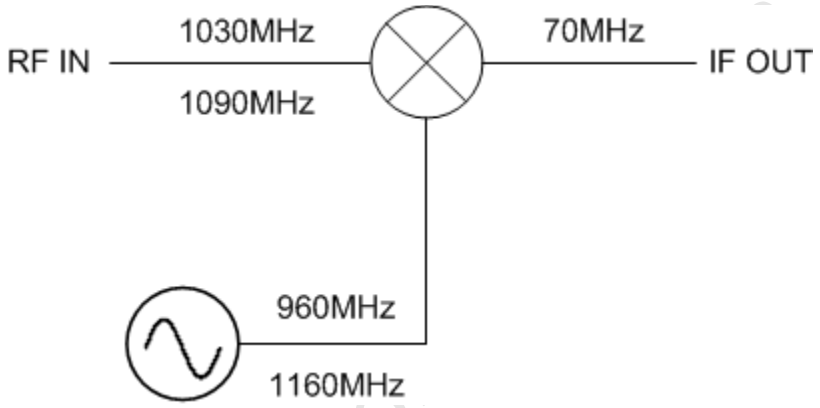


Figure 27: Mixer Down-conversion. The local oscillator output frequency is generated depending on the received signal frequency to keep the IF frequency constant.

4.3.1.4 Low Noise Amplifiers

The RF LNA used in the receiver is similar to the one in the transmitter channel; it is used to amplify the received low power signal. Another LNA with a high linearity, high gain and low noise figure is used to provide power gain in the IF stage of the receiver.

4.3.2 Receiver Parameters

The performance of the receiver could be affected by parameters such as gain, noise and sensitivity. This section discusses all of these parameters, concluding with a budget analysis of the receiver.

4.3.2.1 Gain

The gain is the ratio in decibels between the input and the output power levels of the receiver. The receiver should be capable of providing the gain needed to deliver a signal with the desired output power level. Figure 28 shows the minimum and maximum power at each stage of the ITRC receiver. Over the dynamic range of the receiver, the amplitude relation between the IF output signals and the corresponding RF input signals is linear.

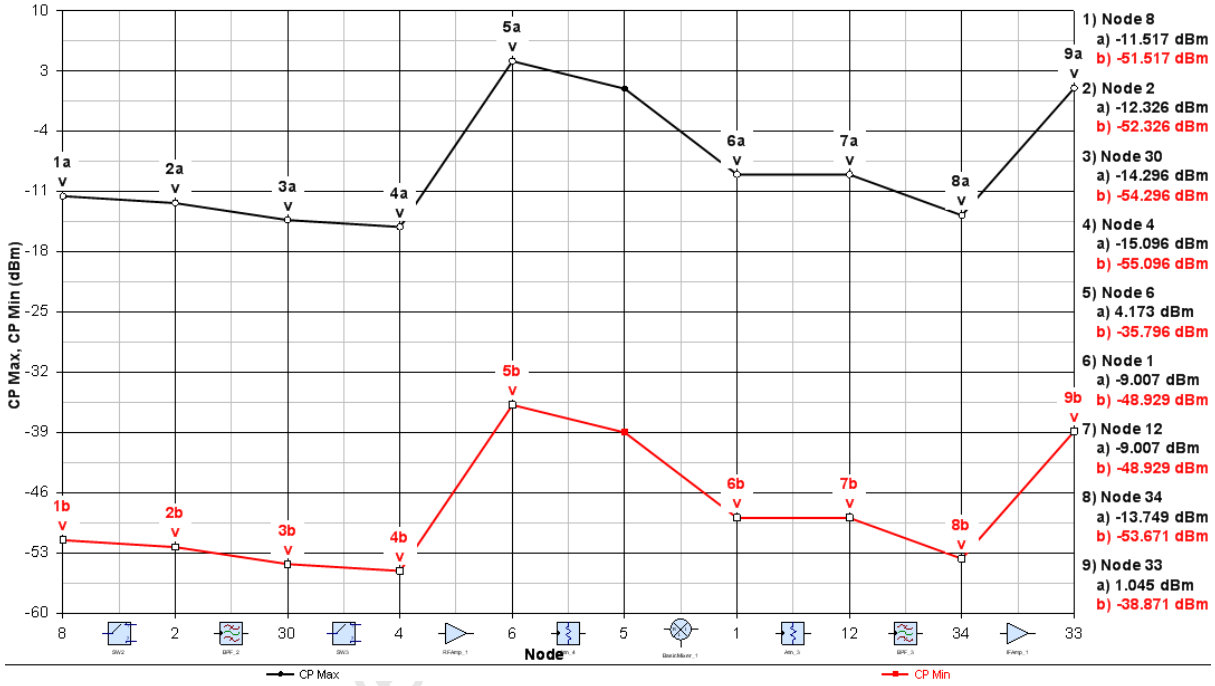


Figure 28: Minimum and maximum power levels at each stage of the ITRC receiver.

4.3.2.2 Noise

There are two types of noise in the receiver. The first type is noise received by the antenna and the second type is noise generated by the receiver itself. The noise received by the antenna can be calculated using the following equation [2]:

$$N = k\,T_o\,B$$

Where:

$\boldsymbol{k}$ is Boltzmann's Constant (1.38 x 10^{-23} Joule/^{o}K)

$\boldsymbol{T_o}$ is the temperature of the receiver input, which equals 290^{o}K

$\boldsymbol{B}$ is the receiver bandwidth in Hz.

The input noise power level at the input of the receiver is -99.2 dBm.

The second type of noise, the receiver noise, is the noise generated by the components in the receiver channel. It can be obtained by calculating the overall noise figure (F) of the receiver. The noise figure is defined as the ratio of input signal-to-noise ratio (S/N_i) to output signal- to-noise ratio (S/N_o). The overall noise figure of the receiver can be calculated using the following equation [2]:

$$\boldsymbol{F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}}$$

Where $\boldsymbol{F}$ and $\boldsymbol{G}$ are the component's noise figure and gain, respectively. The cumulative noise figure of the receiver is described in the budget analysis system.

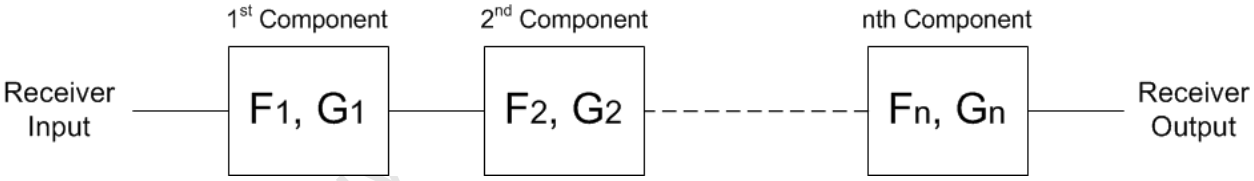


Figure 29: Cascaded block diagram example. The cumulative noise figure values in Table 8 are calculated for the receiver in Figure 24 based on the equation above. For example, for the first two components: Cum. NF equals $\boldsymbol{10\,Log\left[10^{0.8/10} + \frac{10^{2/10}-1}{10^{-0.8/10}}\right] = 2.8\,dB}$

4.3.2.3 Sensitivity

Sensitivity in a receiver is defined as the minimum input signal the receiver can process to provide usable information at the output. The receiver sensitivity can be calculated using the following equation [2]:

$$\boldsymbol{S_{min} = (S/N)_{min}\, k\, T_o\, B\, F}$$

Where: S_{min} is the receiver sensitivity.

$(S/N)_{min}$ is the minimum signal-to-noise ratio needed to process a received signal. The minimum signal-to-noise ratio is about 24.4 dB, according to Section 4.3.2.4.

k is Boltzmann's Constant (1.38 x 10^{-23} Joule/^{o}K).

T_o is the temperature of the receiver input (290^{o}K).

B is the receiver IF bandwidth (33 MHz).

F is the receiver noise figure, which is about 6.43 dB according to Section 4.3.2.4.

Based on these calculations, the ITRC receiver sensitivity equals -68 dBm, which covers the minimum input signal requirement.

4.3.2.4 Receiver Budget Analysis

Tracking the signal and noise levels along the receiver stages is important to ensure linear operation and to keep the signal-to-noise ratio at the output of the receiver above the minimum requirement. Table 8 shows the result of analysing the cascaded components of the receiver shown in Figure 24.

Table 8: ITRC Receiver Budget Analysis.

Components	Input	SW	FLT	SW	AMP	ATT	MIX	ATT	FLT	AMP
BW (MHz)		4000	40	4000	2900		1600		33	2960
Cum. Gain (dB)		-0.8	-2.8	-3.6	+15.7	+12.7	+4.9	+4.9	-0.1	+14.7
Noise Figure (dB)		0.8	2	0.8	0.7	3	0.7	0	5	2.9
Cum. Noise Figure (dB)		0.8	2.8	3.6	4.3	4.34	4.36	4.36	5.35	6.43
Noise (dBm)	-99.2	-85.5	-87.4	-83.8	-62.7	-65.7	-73.5	-73.5	-78.5	-61.2
1dB Comp. Point (dBm)		+32		+32	-0.3		+14			+8.2
Maximum Signal		-11.5	-12.3	-14.3	-15.1	+4.2	+1.2	-6.6	-6.6	-11.6

4.3.3 Receiver Components

The components used to build the ITRC receiver section are summarized in Table 9 below:

Table 9: ITRC receiver components summary.

Component Type	Manufacturer	Part Number
SPDT RF Switch	Hittite	HMC349MS8G
1030 MHz RF Filter	ECHO Microwave	EMA8F1030P6D20A
1090 MHz RF Filter	ECHO Microwave	EMA8F1090P6D20A
70 MHz IF Filter	C. TECH	CLBA70P13K40G
Mixer	Mini-Circuits	ADE-17H
Synthesizer	Analog Devices	ADF4360-7
Crystal Oscillator	Cardinal	LF-TVXO009920
RF Amplifier	Avago Technologies	MGA-62563
IF Amplifier	Avago Technologies	MGA-30689

4.4 ITRC Interface

The purpose of the interface section is to filter and distribute the input power, which comes from an external power supply, between the ITRC subsystems. It also converts the input 5 volt to the 3.3 volt required for the transmitter and receiver synthesizers. The interface thus communicates between the analogue section and the digital board. Table 10 summarizes the ITRC power consumption with full loads applied.

Table 10: ITRC system maximum current and total power consumption.

Subsystem	Component	Voltage (V)	Max. Current (mA)	QTY	Total Current (mA)	Power Consumption (W)
Front-end	HMC349MS8G	5	5	3	15	0.075
Receiver	HMC349MS8G	5	5	2	10	0.05
	MGA-62563	5	90	2	180	0.9
	MGA-30689	5	110	1	110	0.55

	ADG619	5	0.001	1	0.001	0.000005
	ADL5519	5	60	1	60	0.3
	TCVCXO	3.3	3	1	3	0.0099
	ADF4360-7	3.3	14	1	14	0.0462
Transmitter	HMC349MS8G	5	5	3	15	0.075
	MGA-62563	5	90	2	180	0.9
	HMC472LP4	5	5	1	5	0.025
	TCVCXO	3.3	3	1	3	0.0099
	ADF4360-7	3.3	14	1	14	0.0462
Interface	MC5255-3.3YM5	5	55	1	55	0.275
	ADG619	5	0.001	1	0.001	0.000005
	SN74LVC2G04	5	0.01	4	0.04	0.0002
Total					**664.042**	**3.26241**

4.5 ITRC Digital Design

This section introduces the Quixote board, which has been used to run the IFF Reply Emulator and the digital side of the ITRC. A brief overview of the emulator design concept is given too. The design of the ITRC IFF emulator interface is described in detail in this section.

4.5.1 Hardware Overview

The Quixote board [9] contains a Texas Instruments TMS320C6416 DSP and a Xilinx XC2V6000 Virtex-II FPGA. It also comprises two 14-bit Analog Devices AD6645 analogue-to-digital converters (ADC) and two 14-bit AD9746 digital-to-analogue converters (DAC). The board has a 32 MB SDRAM as well as an 8 MB ZBT SBSRAM. A 32-bit port is available for general purpose digital input/output.

4.5.2 IFF Reply Emulator

The IFF reply emulator [5] uses eight transponder-cryptographic computer pairs, which exist in the FPGA, to emulate up to 1500 targets. The eight pairs are divided into two groups, used to receive interrogations in a ping-pong method, switched by ACP pulses.

The Azimuth Change Pulse (ACP) is a train of 4096 pulses per 360^{o} with a fixed pulse interval that provides the azimuth of an SSR/IFF antenna. An Azimuth Reference Pulse (ARP) is used to reset the ACP counter and it is generated only once per antenna rotation [5].

When an ACP/ARP pulse is detected, the DSP updates the personalities of the transponder-cryptographic computer pairs based on interrupts from the FPGA. The target personality can be updated from a look-up table located in the SDRAM and managed by the DSP. The table contains information such as reply code and target range. Moreover, this look-up table is mirrored, so that the DSP can switch between the two tables to update one of them with the calculated changes in the positions and ranges of targets for the following antenna rotation, while the other table is being used to update the FPGA.

4.5.3 ITRC to IFF Reply Emulator Interface Design

The IFF Reply Emulator was designed to generate TTL replies from internal transponder-cryptographic computer pairs with different personalities, in terms of reply code and range, based on the detected TTL interrogations. The emulator also comprises internal interrogator-cryptographic computer pairs that are responsible for generating FRUIT replies.

In order to satisfy all of the ITRC transmitting and receiving requirements, new VHDL modules were added to interface to the existing IFF Target Emulator modules. The dashed boxes in Figure 30 represent the new VHDL modules.

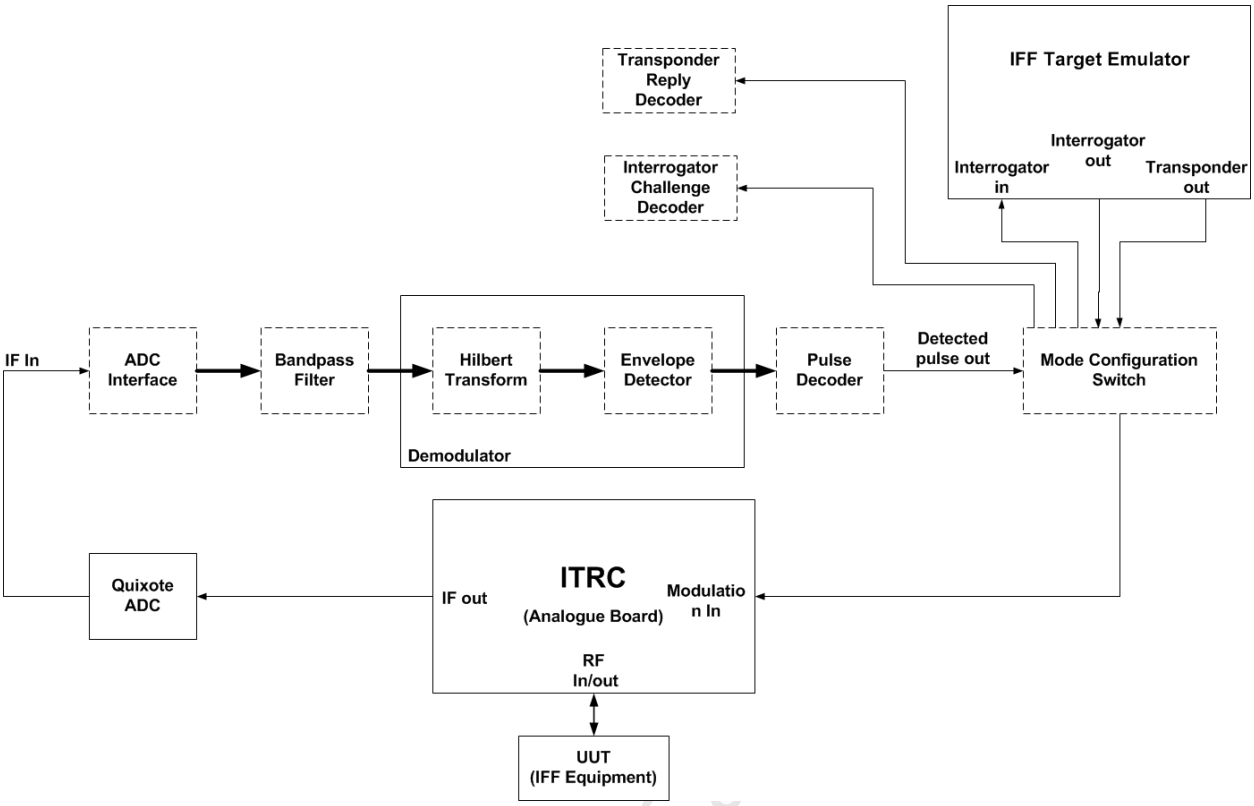


Figure 30: ITRC IFF Emulator Interface Context Diagram.

4.5.3.1 ADC Interface

The ADC Interface is a modified version of the ADC hardware component of the existing Quixote board. The new ADC interface has been modified to operate in streaming mode, in contrast to the buffered mode of the original Quixote model, shown in Figure 31.

In buffered mode, data would be captured until the buffer reached a preset threshold. The data would then have to be transferred from the buffer at a higher speed than capturing the data. The aim of this high speed transfer is to prevent buffer overflow, which would mean a loss of data. The ADC interface operates in streaming mode because the ITRC samples the IF output of the receiver at 100 MHz and the Quixote FPGA clock is also running at 100 MHz.

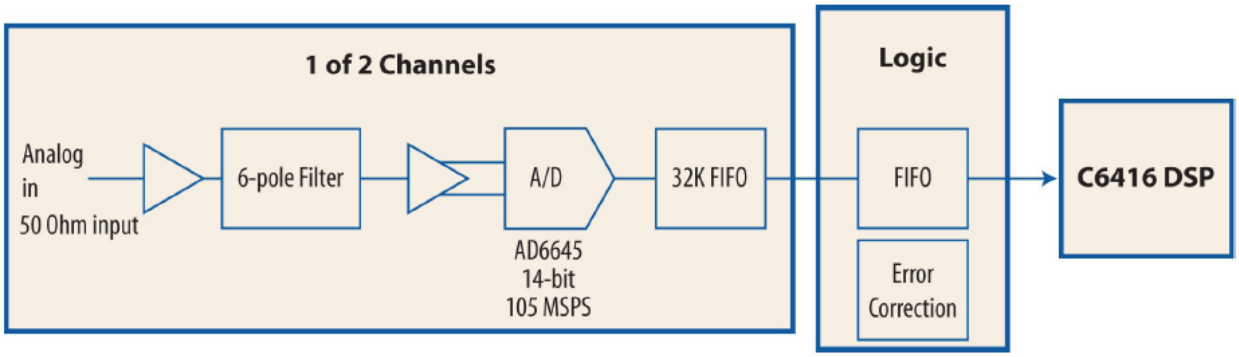


Figure 31: Adapted from [9]. Interconnections of the Quixote analogue input sub-system.

The Quixote ADC (AD6645) is configured to sample the IF output of the ITRC at 100 MHz; this gives an IF in the digital domain of 30 MHz, as seen in Figure 32. The ITRC analogue part was used to send an SSR IF signal in mode 1 to the ADC input. The time domain plot and the Fast Fourier Transform (FFT) plot of the ADC data capture for Mode 1 are shown in Figure 33 and Figure 34, respectively.

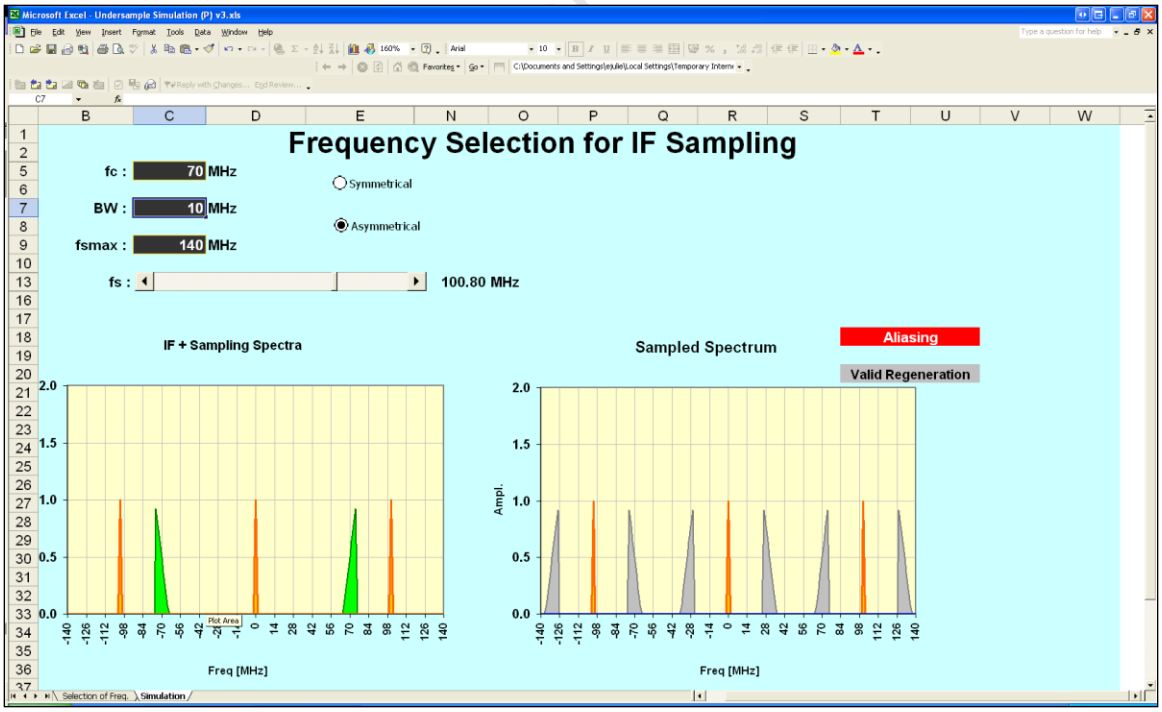


Figure 32 : Sampling frequency selection

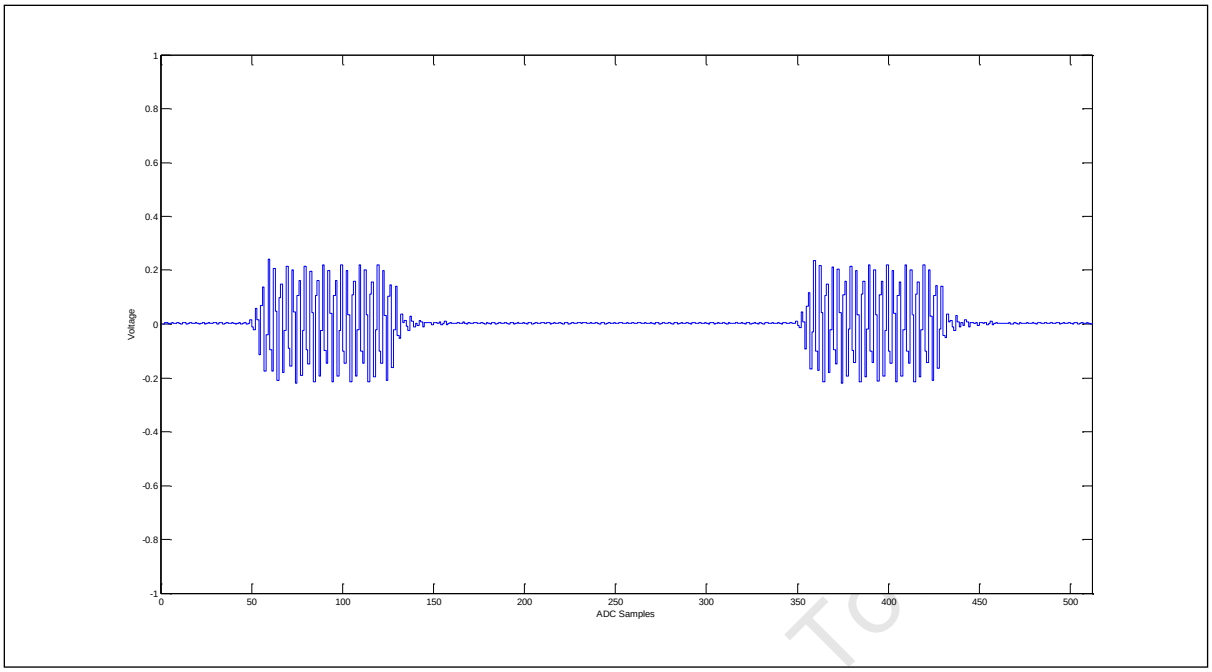


Figure 33 : Time Domain Plot of ADC data capture for Mode 1

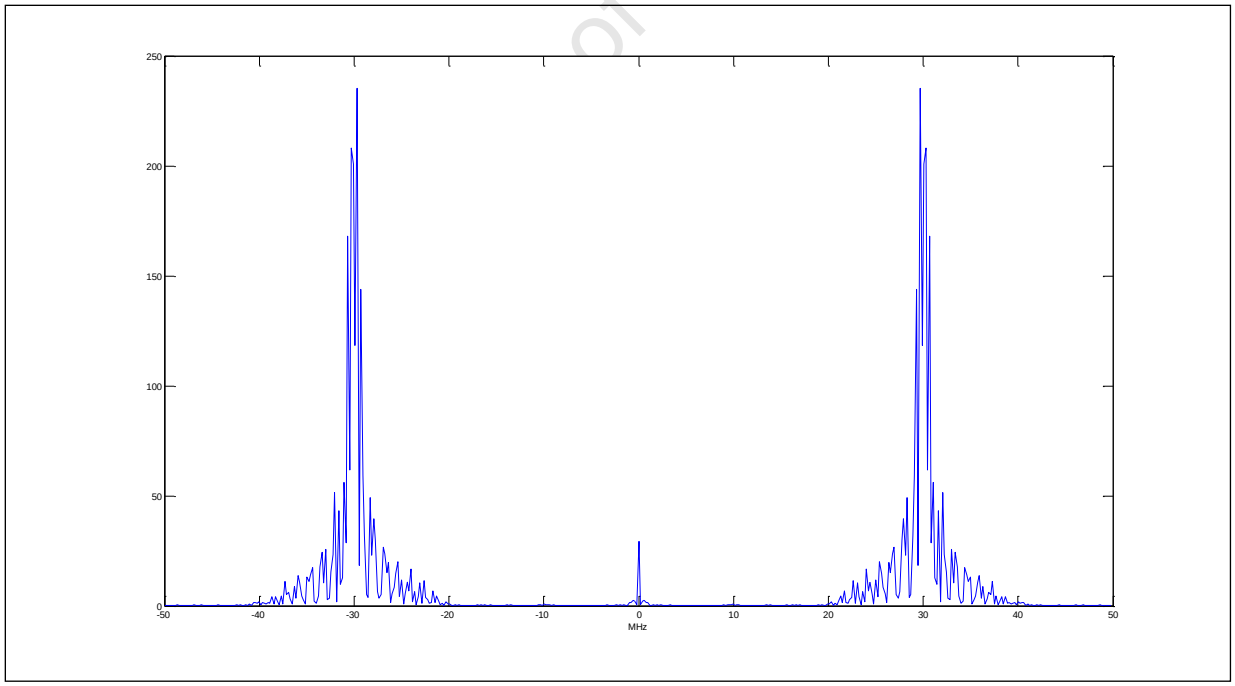


Figure 34: FFT Plot of ADC data capture for Mode 1

4.5.3.2 Digital Band-pass Filter

The band-pass filter was added to the design because problems were initially experienced with the Quixote hardware interfacing. The initial FFT plots of the ADC data that were captured showed unexpected frequency spurs in the band of interest. At that stage, it was not known whether this might be caused by the hardware not being optimised to work at a 70 MHz intermediate frequency.

The band-pass filter is implemented with the Filter Design and Analysis Tool from *MathWork* [8] using the following specifications:

- Filter order = 8
- Fs = 100 MHz
- Fstop1 = 15 MHz
- Fpass1 = 25 MHz
- Fpass2 = 35 MHz
- Fstop2 = 45 MHz

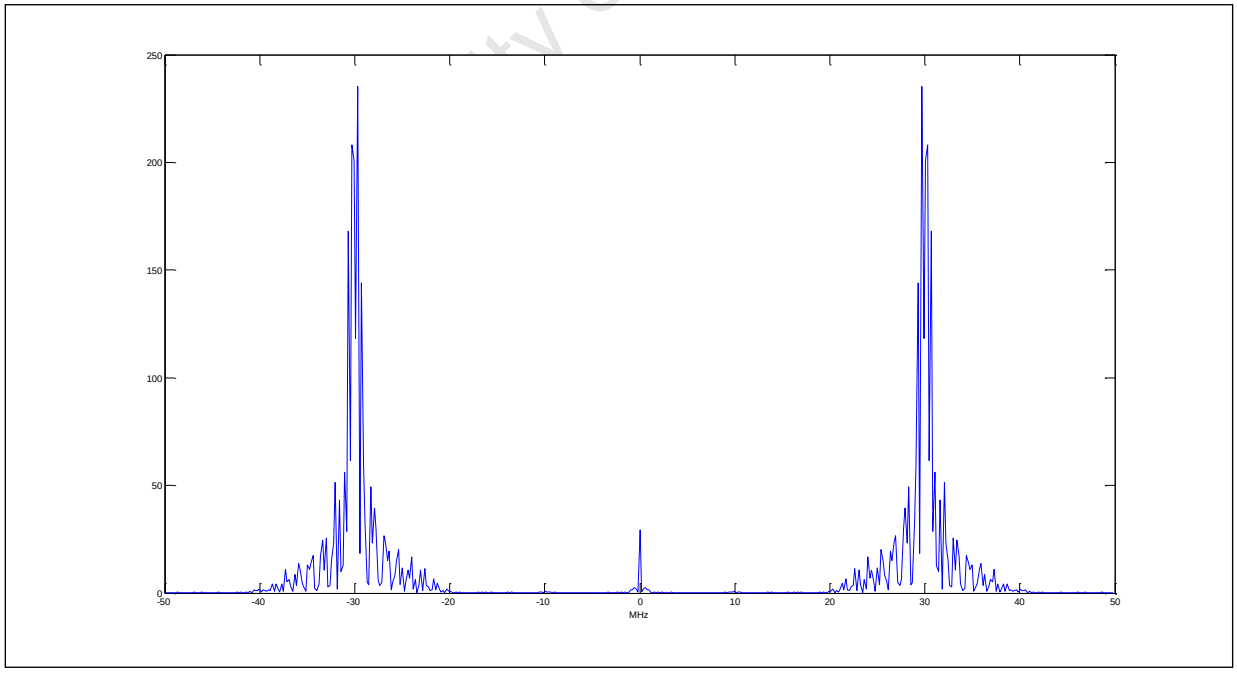


Figure 35 : FFT Plot of Band-pass Filter output for Mode 1 interrogation

From the FFT plots in Figure 34 and Figure 35, it can be seen that the band-pass filter has a minimal impact. Thus, the filter could be removed from the design, and the only impact this would have is to reduce the system delay.

4.5.3.3 Demodulator

The demodulator consists of the Hilbert transformer and the Envelope detector. The output of the demodulator is the envelope detected pulses of the incoming PAM signals. The envelope detection scheme used in the design [6] takes the sum of the absolute values of a complex signal's real and imaginary parts, and applies that sum to a simple first-order low pass Infinite Impulse Response (IIR) filter to obtain an envelope signal E(n), as shown in Figure 36 [6].

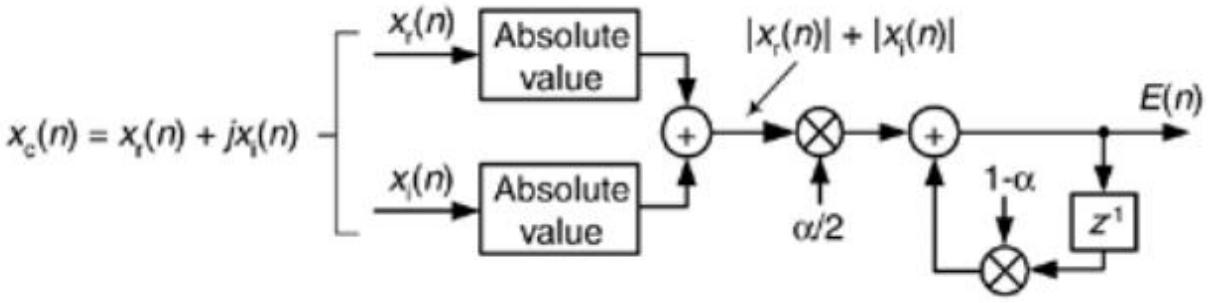


Figure 36: Adapted from [6]. Envelope detection Block diagram.

The Hilbert transformer is implemented with the Filter Design and Analysis Tool from *MathWorks* using the following specifications:

- Filter order = 8
- Fs = 100 MHz
- Frequency vector = [15 45] (MHz)

The first order low pass IIR filter of the original design was removed from the design, as this was causing unacceptable stretching of the decoded pulse width. This was done before the ADC hardware interface issues experienced above were resolved. The initial

design of the Hilbert transform was also using the full bit width output. The output of the Hilbert transform in the current design was truncated to 14 bits.

A low pass Finite Impulse Response (FIR) filter can be used to replace the IIR filter used in the envelope detection scheme mentioned above. This should reduce the pulse top oscillations and the oscillations at the start and end of the pulse, as seen in Figure 37. The oscillations at the start and end of the pulse are the cause of the narrow pulses out of the threshold detector shown in Figure 43.

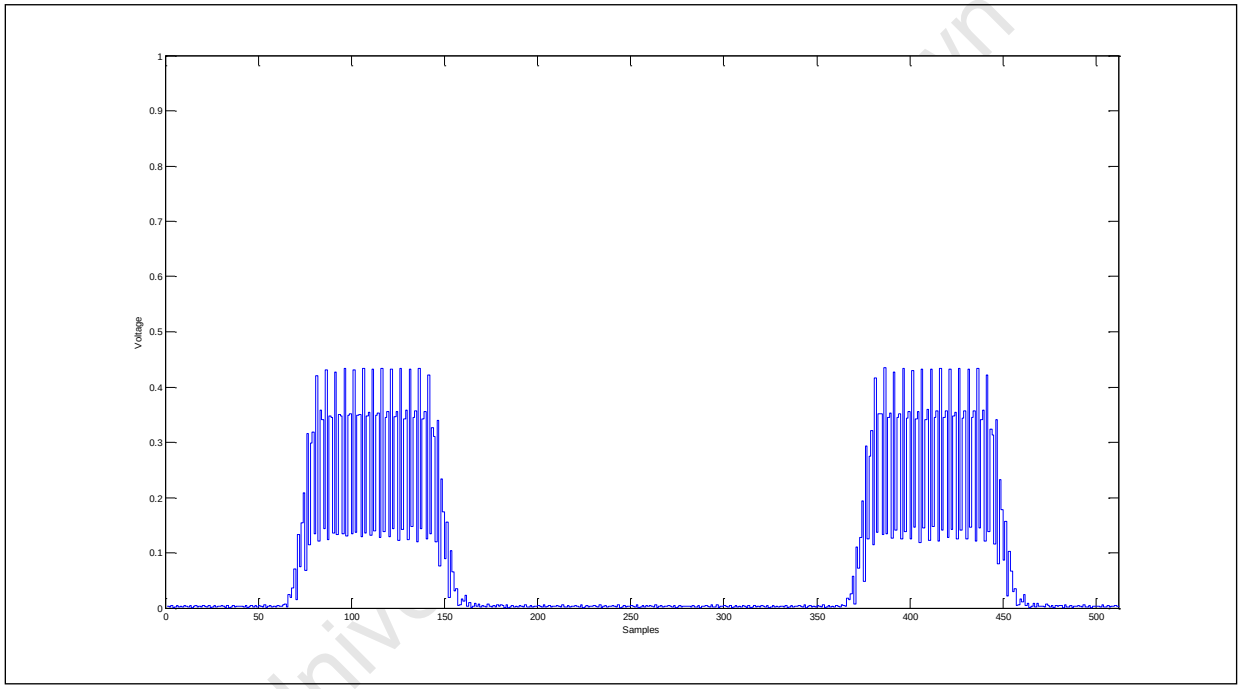


Figure 37 : Time Domain plot of Demodulator output for a Mode 1 interrogation

Figure 38 and Figure 39 are the results of a *Modelsim* simulation using the actual captured data of a Mode 1 interrogation. The signals *Envout_s* and *pulse_out* are for the current demodulator and threshold detector output respectively. The signal *lpf_out_s* is the demodulator output filtered with a FIR low pass filter. The signal *pulse_out2* is the output of the threshold detector with signal *lpf_out_s* as the input. From the simulation, we can observe that the pulse width of *pulse_out2* is 990 ns. This is 190 ns longer than

the expected pulse width of 800 ns and it furthermore falls outside of the specification, which is 800±50 ns. One possible way to improve the accuracy of the detected pulse width is to modify the threshold detector from having a fixed detection level to an adjustable one. The adjustable detection level should be adjusted so that it is always 50% lower than the pulse top. This implies that a peak detector must be implemented to find the pulse top.

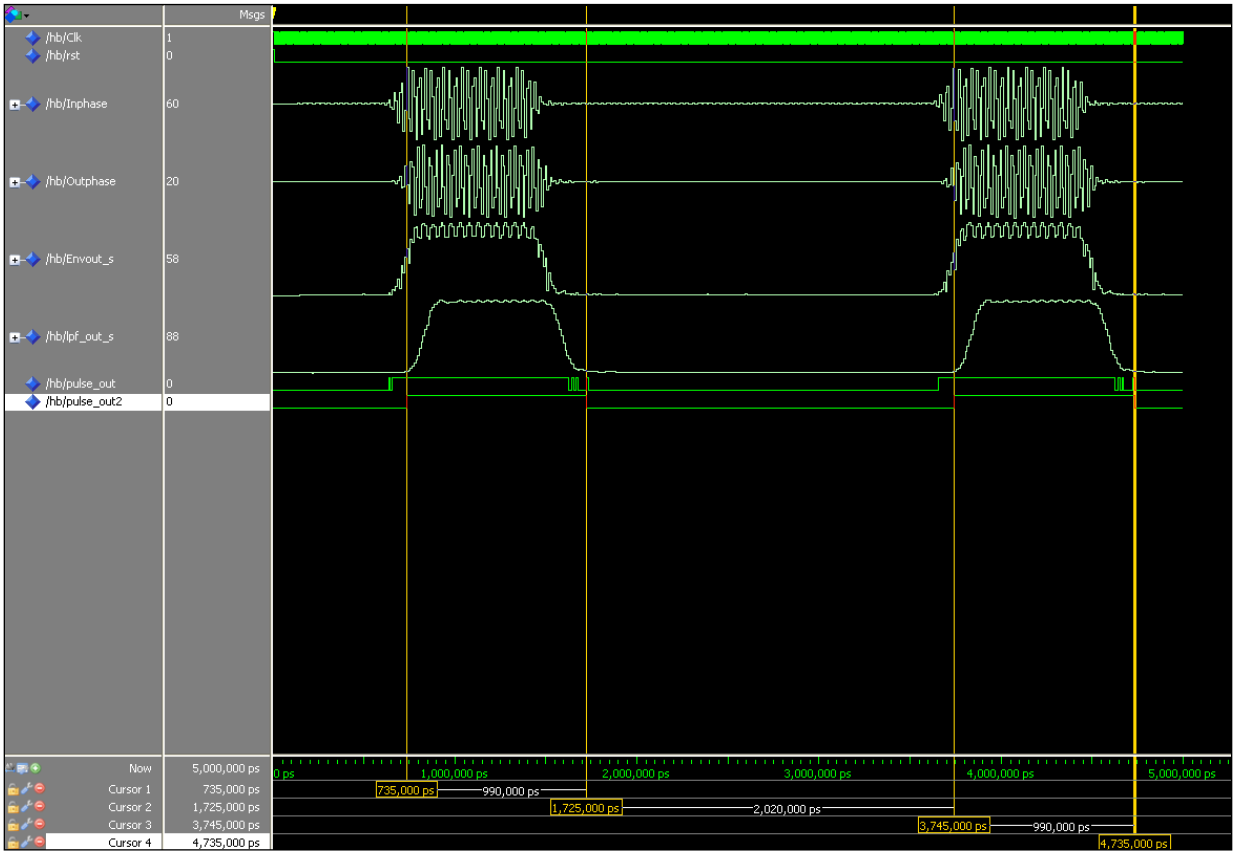


Figure 38 : *Modelsim* Simulation of Mode 1 interrogation.

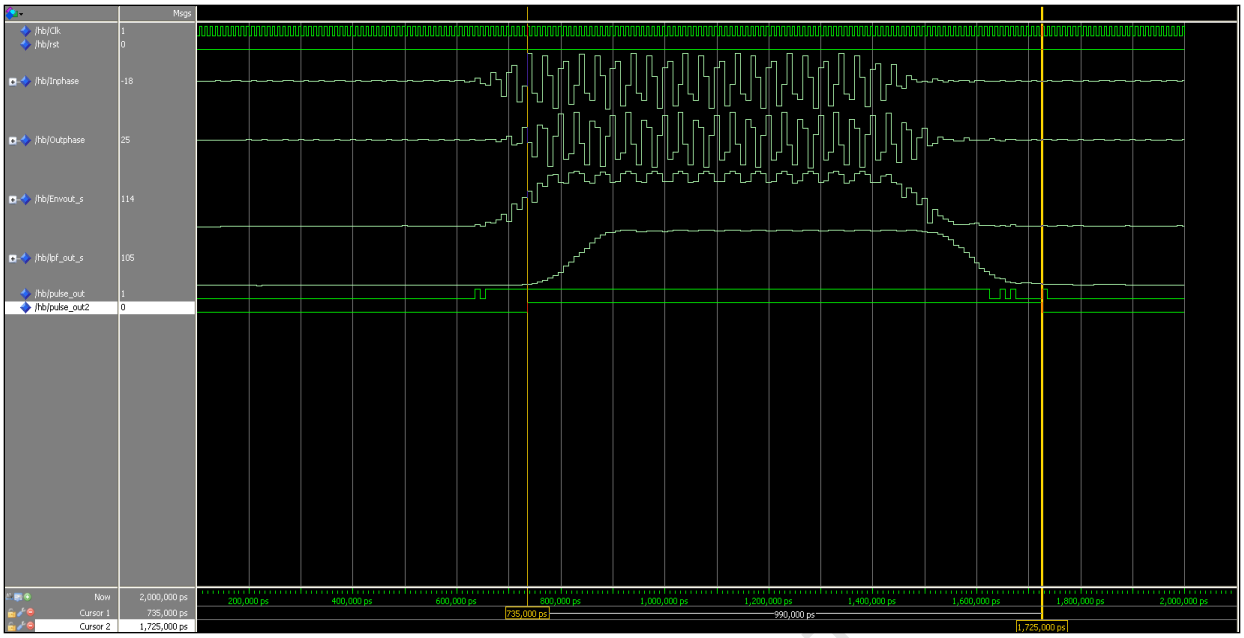


Figure 39 : *Modelsim* Simulation of Mode 1 interrogation (Zoomed in).

Figure 40 below is a Simulink model used for simulating the demodulator. The model implements the current demodulator design but also compares the current output with a demodulator output low pass filtered with FIR and IIR filters. The IIR filter is implemented, as in Figure 36. The FIR filter has a cut-off frequency of 10 MHz.

Figure 41 is the simulation result for the demodulator model. The top waveform is the input to the Zero-Order Hold block (this represents the ADC). The yellow signal in the bottom window is the FIR filtered signal, the magenta signal is the demodulator output, and the cyan signal is the IIR filtered signal. From the comparison, it can be observed that the FIR filtered signal performs the best with respect to the pulse top ripple.

In Figure 42, the value of Alpha (α) has been reduced to reduce the pulse top ripple. The downside to this adjustment is that it negatively affects the rise and fall time of the detected pulse, which in turn affects the pulse width of the detected signal. This FIR filter with a threshold detector and an adjustable detection level seems to be the best option for more accurate detection of pulse width. This in turn would mean that the pulse decoder would not have to regenerate the detected pulse.

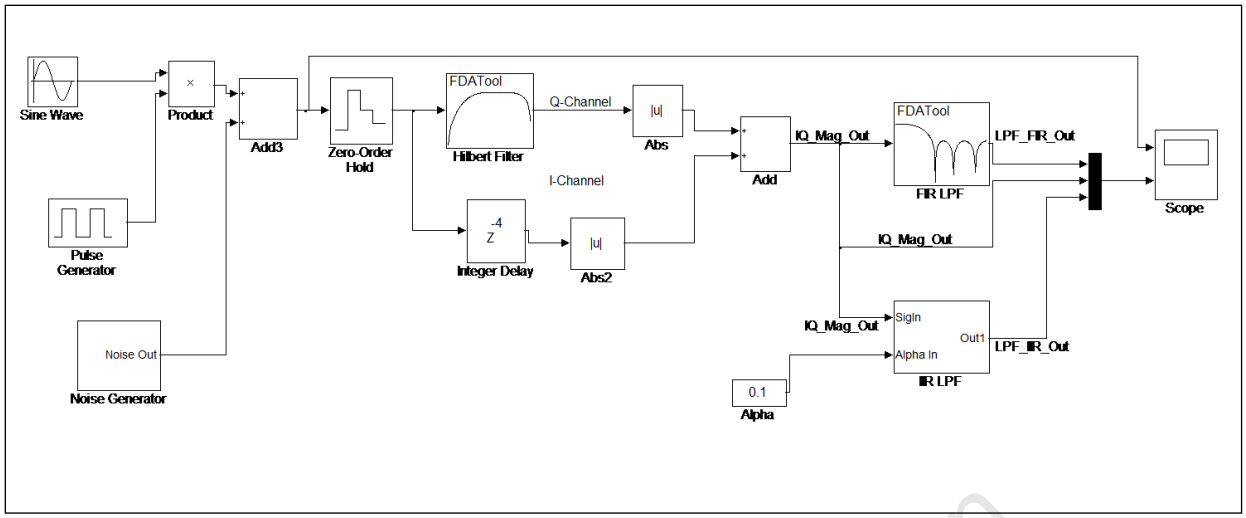


Figure 40 : Simulink model for Demodulator

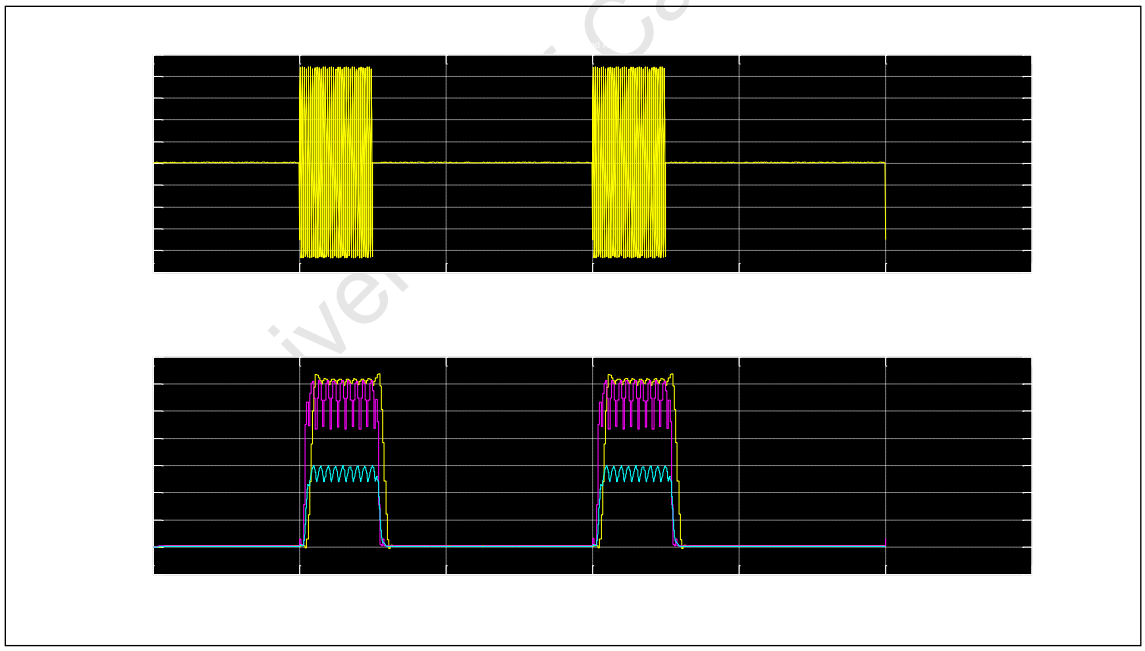


Figure 41 : Mode 1 interrogation simulation (Alpha = 0.1)

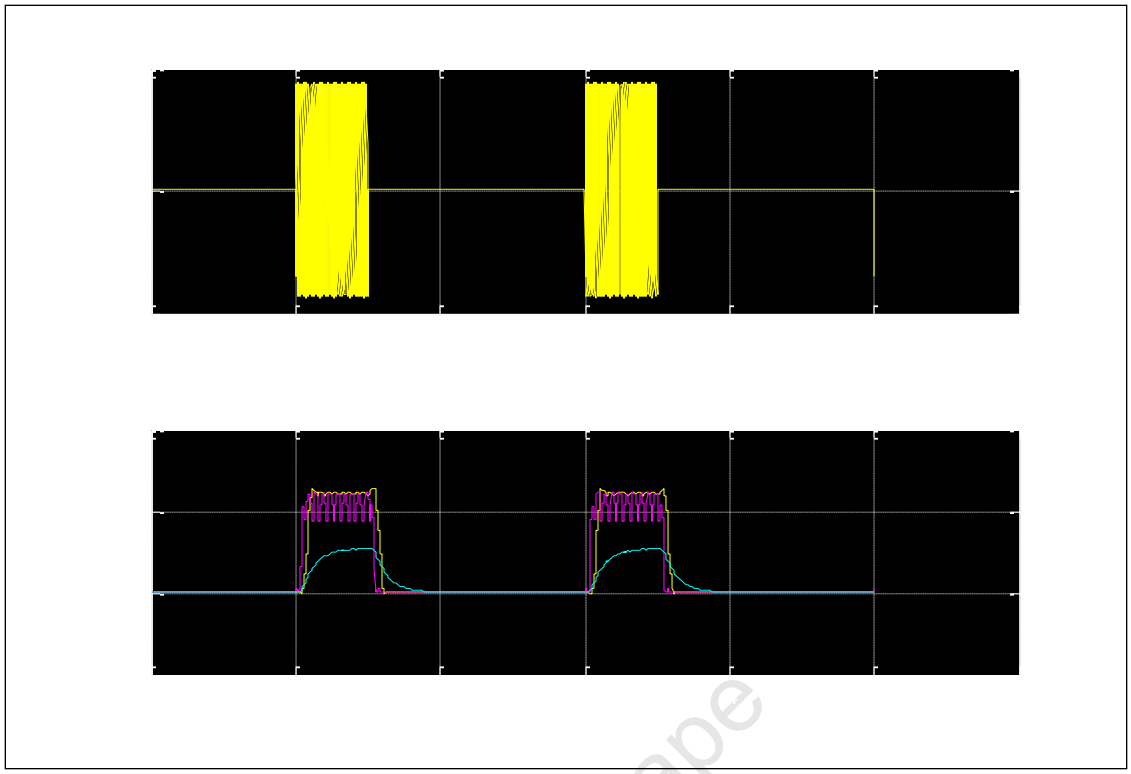


Figure 42 : Mode 1 interrogation simulation (Alpha = 0.01)

4.5.3.4 Pulse Decoder

The pulse decoder implements a fixed-level threshold detector, with the output being a digital logic '1' or '0', pulse filter and a pulse processor. The ideal output of the threshold detector should be the digital representation of the demodulated PAM signal. The pulse filter is used to filter out the 1 or 2 samples that are low during the active period of the detected pulse. The pulse processor detects pulses that are high for at least 350 ns and then regenerate pulses of 450 ns or 800 ns, depending on whether the incoming signal was from a transponder or interrogator.

Figure 43 below is a screen capture of the *Xilinx Chipscope* application while monitoring the output of the threshold detector, pulse filter and pulse processor for a mode 1 interrogation. From the screen capture, it can be observed that the output of the threshold detector (*threshold_detected pulse*) has some narrow pulses at the start and

end of the two pulses. From the output of the pulse filter (*thr_pulse_filt*), it can be observed that the narrow pulses have been filtered out.

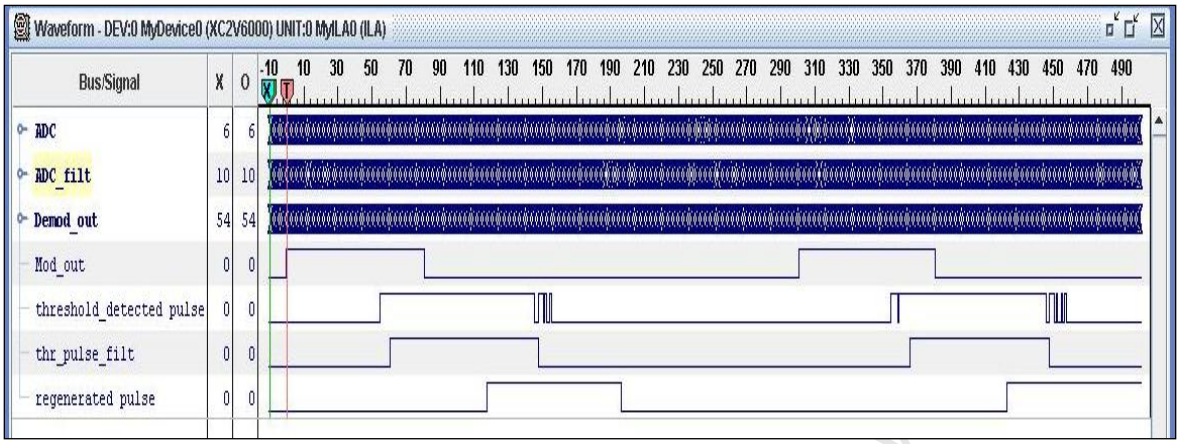


Figure 43 : Screen Capture of Xilinx Chipscope for Mode 1 interrogation

4.5.3.5 Mode Configuration Switch

The mode configuration switch implements a switch matrix for inter-connecting signals from the different modules, described in Table 11, depending on the mode of operation. See table below.

Table 11: Modes of operation and their signal interconnections.

Mode of operation	Signal interconnections
Interrogator Loopback mode	Interrogator out -> Modulation in Detected pulse out -> Interrogator Challenge decoder
Transponder Loopback mode	Transponder out -> Modulation in Detected pulse out -> Transponder Reply decoder
Interrogator Test	Detected pulse out -> Interrogator in Transponder out -> Modulation in
Transponder Test	Interrogator out -> Modulation in Detected pulse out -> Transponder Reply decoder

4.5.3.6 Transponder Reply Decoder

The transponder reply decoder extracts the reply data from the demodulated reply and furthermore measures the delay from when an interrogation was generated until a reply has been received. The reply data and reply delay is written to memory-mapped registers, which can be read via the software running on the DSP.

Table 12: FPGA registers and their addresses.

Name	Address
Reply Data Register	0x804A0000
Reply Delay Register	0x804C0000

The reported reply delay is the number of elapsed clock cycles from the interrogation P1 pulse to the transponder F2 reply pulse. The clock period equals 10 ns. The measured value for the reply delay consists of the following additional delays:

1. Interrogation P1-P3 delay (Dependent on the mode of interrogation, 3 μs for Mode 1, 21μs for Mode C, etc.)
2. Reply delay (Fixed at 3 μs : 300 clock cycles)
3. F1-F2 reply spacing (20.3 μs : 2030 clock cycles)
4. System delay (ADC buffer, filters, etc. : 140 clock cycles)

4.5.3.7 Interrogator Challenge Decoder

The interrogator challenge decoder extracts the mode of interrogation by measuring the delay between P1-P3 of the interrogation. A number representing the mode of interrogation is written to a memory-mapped register at address 0x804E0000. Table 13 below lists all modes of interrogation and their mode register values.

Table 13: Mapping of Interrogation mode register value and Mode of interrogation.

Interrogation mode register value	Mode of interrogation
1	1
2	2
3	3/A
4	4
5	C

4.6 Summary

This chapter has described the design of the analogue and digital parts of the ITRC system. The description of each analogue subsection began with a block diagram defining the relevant stages of that subsection. This block diagram was simulated using *Genesys* software, which furthermore guided the choice of components to suit the design. The main parameters of each subsection to achieve the maximum performance level were discussed in detail.

The chapter also presented the VHDL models, which have been added to the IFF reply emulator in order to satisfy the user requirements. All obstacles encountered during the digital design phase, especially with regard to the digital hardware interface, and the ways in which such problems were resolved, were discussed too.

The following chapter documents the analogue and digital tests that were done on the ITRC system.

5 ITRC System Testing

This chapter presents the practical tests that were done on the ITRC system. The first part looks at the analogue tests that were conducted to evaluate the performance of the ITRC transmitter and receiver and to ensure that the test results satisfy the user requirements. The second part of this chapter details the ITRC functional testing, which has been performed by integrating the ITRC with the SSR/IFF interrogator and transponder. This part describes the loopback, interrogator and transponder test procedures and presents the test results. The interrogator was also tested for FRUIT and garbled replies. At the time these tests were performed, a cryptographic-computer was unavailable, however, and thus it was not possible to perform the mode 4 tests.

5.1 ITRC Test Procedure and Results

The following acceptance tests were used to evaluate the performance of the various analogue subsections of the ITRC; the results of those tests are described in this section. The insertion loss of the cables used during the testing was taken into account to ensure accurate measurements.

5.1.1 Test Equipment

Table 14 below lists all the test equipment used for all the tests:

Table 14: List of equipment used to test the ITRC.

Equipment	Model Information
Multi-meter	Yokogawa 7532
Power Supply	N/A
Signal Generator	HP 8642B
Spectrum Analyser with DC block	HP 8593E
Oscilloscope	TDS 1012
Male SMA - Male SMA Cables	N/A
50Ω Male SMA 2 Watt Terminations	N/A
PC installed with Windows XP (SP3)	N/A
Digital Board	Quixote Board Revision E
JTAG Emulator	Xilinx

5.1.2 Power Consumption

In order to perform this test, all SMA ports have been terminated in 50Ω to measure the quiescent +5V current consumption. A multi-meter with appropriate settings selected was used to measure the current. According to Section 4.4, the ITRC maximum current consumption with full loads applied is 664 mA.

5.1.2.1 Summary of Results

Table 15: Power consumption test result.

Power Consumption	Unit	Low Limit	Test Result	High Limit	Pass/Fail
Maximum Quiescent +5V Current Consumption	mA	-	610	664	Pass

5.1.3 Return Loss Measurement

The purpose of the return loss measurement is to determine the fraction of the power reflected from the load connected to the ITRC with respect to the incident power. The values have been measured while the ITRC is connected to an IFF equipment. The return loss value is about -21 dB, which is derived from the VSWR values in Table 16 below using the following equation:

$$\boldsymbol{Return\ Loss} = \boldsymbol{-20\ Log}\left(\frac{\boldsymbol{VSWR-1}}{\boldsymbol{VSWR+1}}\right) \quad [\boldsymbol{dB}]$$

The table shows that the VSWR has been measured twice, viz. manually and using dual logarithmic detector: the results are almost the same.

5.1.3.1 Summary of Results

Table 16: VSWR measurements.

VSWR	Unit	Low Limit	Test Result	High Limit	Pass/Fail
VSWR at 1030MHz (manual measurement)	:1	1	1.2	2	Pass
VSWR at 1030MHz using the logarithmic detector output	:1	1	1.18	2	Pass

VSWR at 1090MHz (manual measurement)	:1	1	1.2	2	Pass
VSWR at 1090MHz using the logarithmic detector output	:1	1	1.17	2	Pass

5.1.4 Transmitter Output Frequency

This test was performed to check the output frequency of the transmitter's programmable synthesizer, which was measured at the transmitter output port using a spectrum analyser, in order to insure that the synthesizer is able to generate the required frequency based on the test applied. Figure 44 and Figure 45 illustrate the LO's output power at 1030 MHz and 1090 MHz, respectively.

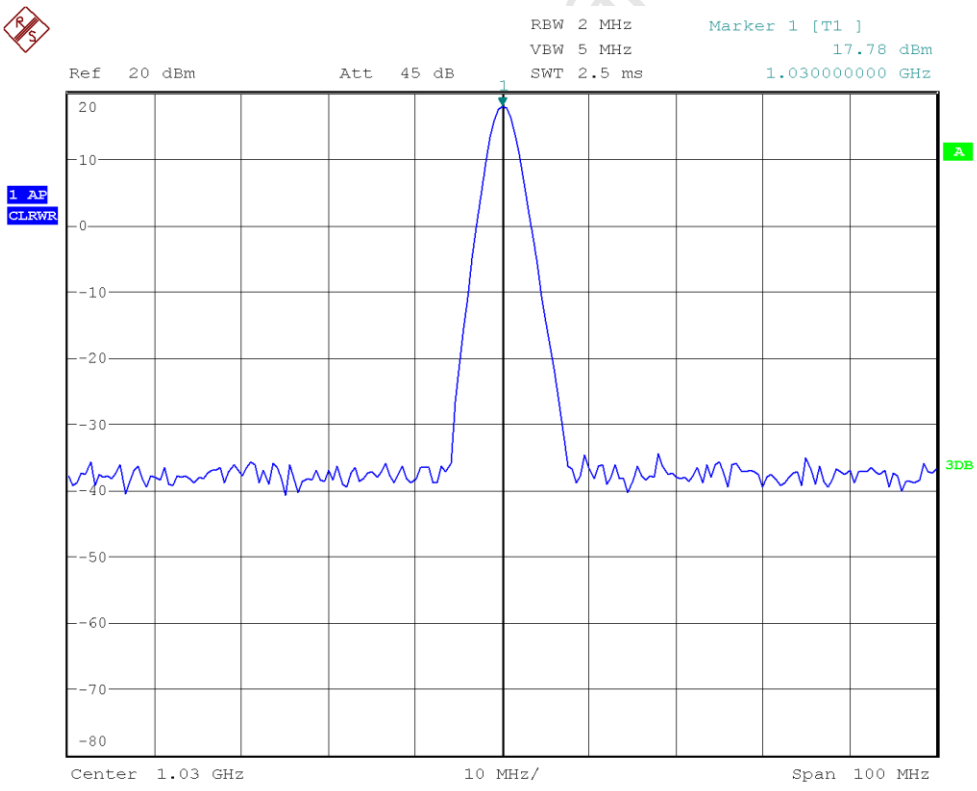


Figure 44: Output signal of the transmitter's local oscillator at 1030 MHz.

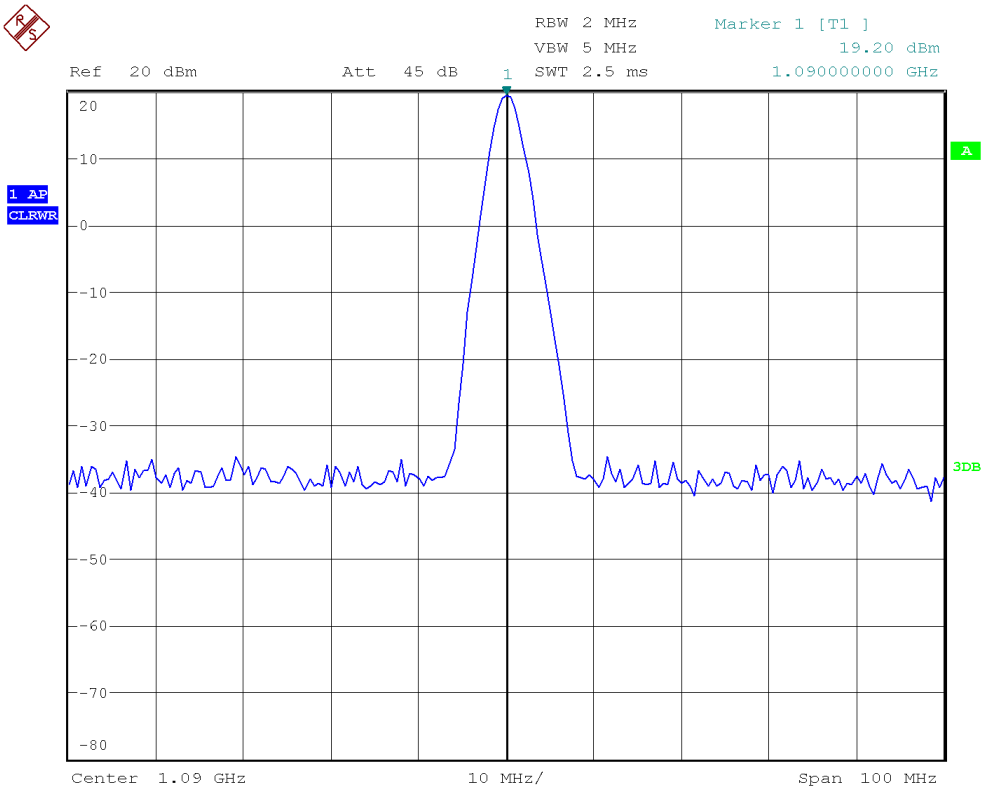


Figure 45: Output signal of the transmitter's local oscillator at 1090 MHz.

5.1.5 Transmitter Output Power Levels

This test is used as a measure of the transmitter's linearity. The RF signal power generated by the local oscillator of the transmitter is decreased in steps of 1 dB using the variable attenuator. Figure 47 shows the linear relationship between the attenuation value and the output power. It also shows that the maximum output power is +18 dBm (see Section 4.2 for parameters).

5.1.5.1 Test Setup

The transmitter output power levels were measured at the transmitter output port using the spectrum analyser, as shown in Figure 46. All the other SMA ports were terminated in 50Ω.

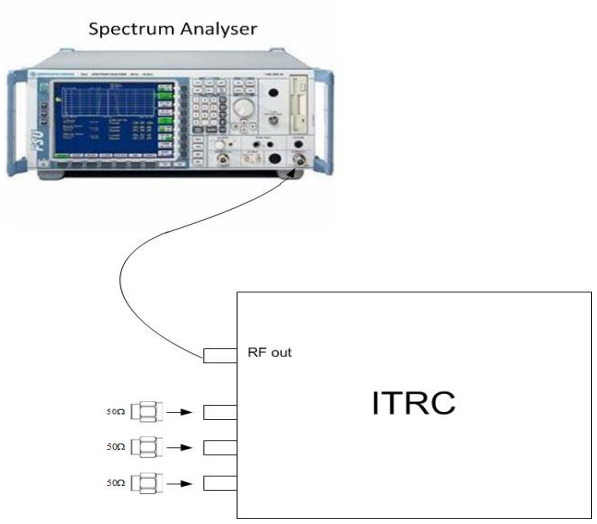


Figure 46: Transmitter output power measurement setup.

5.1.5.2 Summary of Results

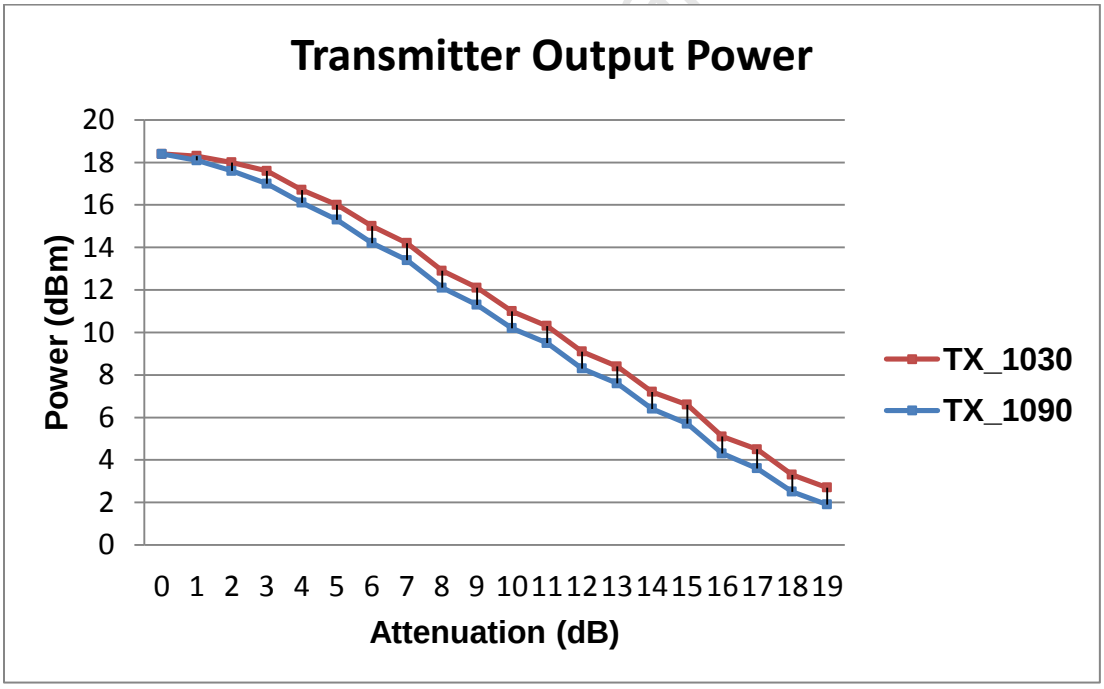


Figure 47: Transmitter output power vs. attenuation values.

5.1.6 Transmitter / Receiver Isolation

The goal of this test is to measure the power leakage from the transmitter to the receiver input during transmission. The transmitter was set to transmit the maximum power, which is +18 dBm. The spectrum analyser was used to measure the power level at the receiver input and compare it with the transmitter output power. The result is shown in Table 17 below (see the user requirements set out in Section 2.2.1).

5.1.6.1 Summary of Results

Table 17: Isolation between the transmitter output and the receiver input.

Isolation	Unit	Low Limit	Test Result	High Limit	Pass/Fail
Receiver input (transmitter RF out = +18 dBm, 1030MHz)	dB	70	75.6	-	Pass
Receiver input (transmitter RF out = +18 dBm, 1090MHz)	dB	70	75	-	Pass

5.1.7 Receiver Output Power Levels

This test is used as a measure of the receiver's linearity. The signal generator was used to transmit RF signals at 1030 MHz and 1090 MHz to the receiver input. The power level of the input signal increased in 1 dB steps to cover the power range specified in Section 3.3.2.5. Figure 49 shows the linear relationship between the input and output power levels.

5.1.7.1 Test Setup

The IF output power was measured using the spectrum analyser, as illustrated in Figure 48. All the other SMA ports were terminated in 50Ω.

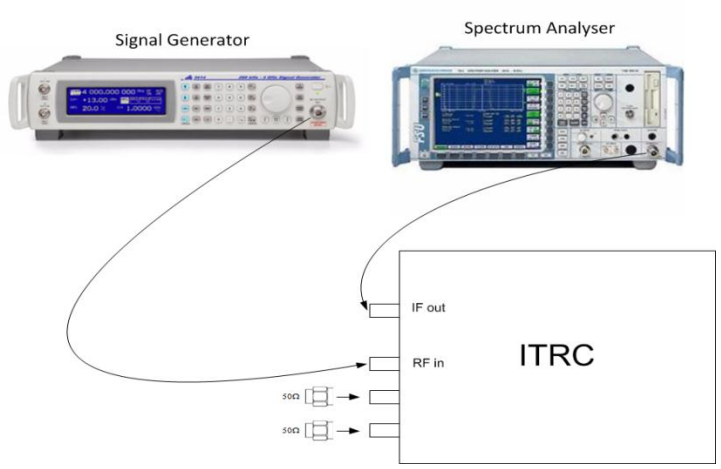


Figure 48: Receiver output power measurement setup.

5.1.7.2 Summary of Results

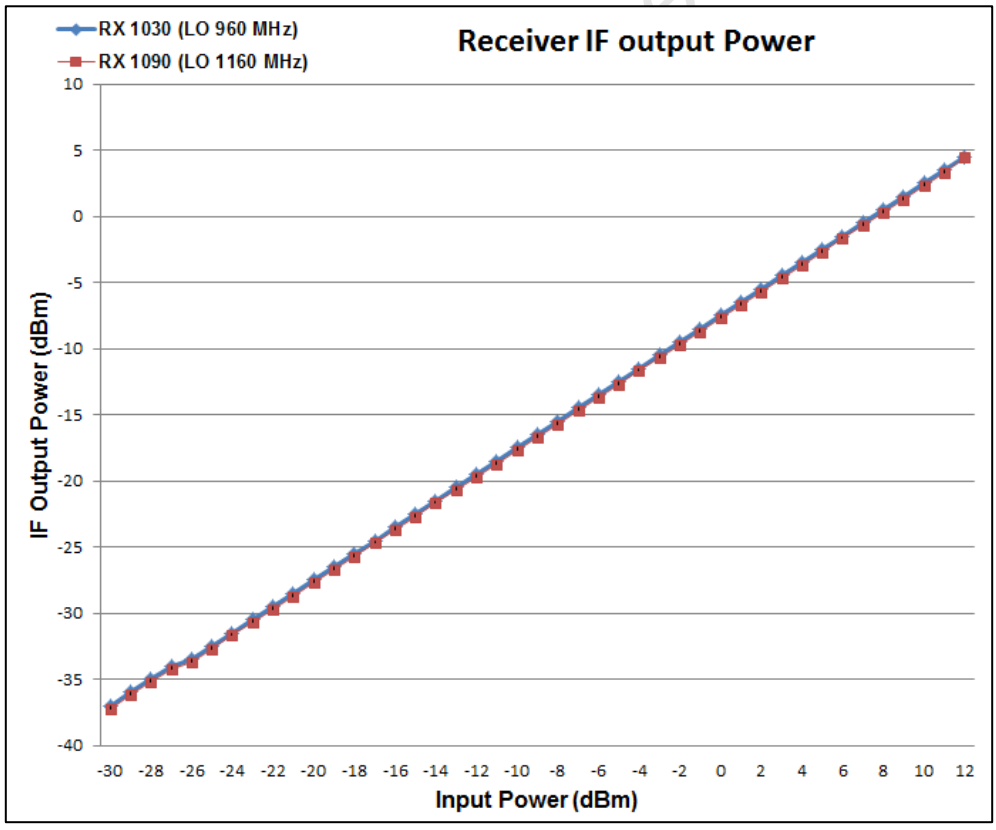


Figure 49: Receiver output power vs. input power.

5.1.8 Loopback Path Test

The purpose of the loopback test is to test the transmit and receive channels. The output of the transmitter is routed back to the input of the receiver via the front-end circuitry. This test involved transmitting +18 dBm from the transmitter channel and measuring the IF output power, which was +0.2 dBm, as expected. The functional test of the loopback path will be described in Sections 5.2.1 and 5.2.2 below.

5.2 ITRC functionality testing

This section describes the ITRC functional test procedure and presents the results of the performance tests. The ITRC was integrated with a transponder and an interrogator in order to complete these required tests.

5.2.1 Interrogator Loopback Test

5.2.1.1 Test Procedure

An internal interrogator of the IFF Target Emulator was enabled with the different interrogation modes. The ITRC was configured to operate in “interrogator loopback” mode (recall Table 11). The interrogation mode value was read from the Interrogation mode register to confirm the mode of interrogation, as illustrated in Table 18 below.

5.2.1.2 Test Results

Table 18: Interrogation modes and their register values.

Mode of Interrogation	Interrogation mode register value
1	1
2	2
3/A	3
C	5

5.2.2 Transponder Loopback test

5.2.2.1 Test Procedure

An internal interrogator and transponder of the IFF Target Emulator were enabled. The interrogator challenge output was internally connected to the transponder challenge input. The ITRC was configured to operate in “Transponder Loopback” mode. The interrogator was configured for different modes of interrogation, whereas the transponder was configured to reply with different reply codes as well as different reply delay values. The reply data register and reply delay register were read, as in Table 19 below, to confirm the preset reply code and reply delay.

5.2.2.2 Test Results

Table 19: Reply data register and reply delay register values.

Reply Code	Reply Delay (Clock Cycle)	Detected Reply Code	Detected Reply Delay (Clock Cycle)
Mode 1			
0x0000	0	0x0000	2767±2
0x0100	0	0x0100	2768±2
0x0200	0	0x0200	2766±2
0x1000	0	0x1000	2766±2
0x2000	0	0x2000	2766±2
0x4000	0	0x4000	2765±2
0x7300	0	0x7300	2765±2
0x7300	100	0x7300	2870±2
	500		3270±2
	1000		3770±2
Mode 2			
0x0000	0	0x0000	2967±2
0x0001	0	0x0001	2968±2
0x0010	0	0x0010	2966±2
0x0100	0	0x0100	2966±2
0x1000	0	0x1000	2966±2

0x1111	0	0x1111	2966±2
0x0002	0	0x0002	2965±2
0x0020	0	0x0020	2965±2
0x0200	0	0x0200	2967±2
0x2000	0	0x2000	2968±2
0x2222	0	0x2222	2965±2
0x0004	0	0x0004	2966±2
0x0040	0	0x0040	2966±2
0x0400	0	0x0400	2966±2
0x4000	0	0x4000	2965±2
0x4444	0	0x4444	2966±2
0x7777	0	0x7777	2965±2
	100		3070±2
	500		3470±2
	1000		3970±2
Mode 3			
0x0000	0	0x0000	3266±2
0x0001	0	0x0001	3266±2
0x0010	0	0x0010	3266±2
0x0100	0	0x0100	3266±2
0x1000	0	0x1000	3266±2
0x1111	0	0x1111	3266±2
0x0002	0	0x0002	3266±2
0x0020	0	0x0020	3266±2
0x0200	0	0x0200	3266±2
0x2000	0	0x2000	3266±2
0x2222	0	0x2222	3266±2
0x0004	0	0x0004	3266±2
0x0040	0	0x0040	3266±2
0x0400	0	0x0400	3266±2

0x4000	0	0x4000	3266±2
0x4444	0	0x4444	3266±2
0x7777	0	0x7777	3266±2
	100		3370±2
	500		3770±2
	1000		4270±2
Mode C			
0x0000	0	0x0000	4566±2
0x0001	0	0x0001	4566±2
0x0010	0	0x0010	4566±2
0x0100	0	0x0100	4566±2
0x1000	0	0x1000	4566±2
0x1110	0	0x1110	4566±2
0x0002	0	0x0002	4566±2
0x0020	0	0x0020	4566±2
0x0200	0	0x0200	4566±2
0x2000	0	0x2000	4566±2
0x2222	0	0x2222	4566±2
0x0004	0	0x0004	4566±2
0x0040	0	0x0040	4566±2
0x0400	0	0x0400	4566±2
0x4000	0	0x4000	4566±2
0x4444	0	0x4444	4566±2
0x7776	0	0x7776	4566±2
	100		4670±2
	500		5070±2
	1000		5570±2
	150000		154570±2

The detected reply was found to be as stated in the specifications for the Transponder Reply Decoder. Taking Mode C with a transponder reply delay of 150000 clock cycles as example:

Actual delay (clock cycles) = $D_{measured} – (D_{P1-P2} + D_{reply} + D_{F1-F2} + D_{system})$

$= 154570 – (2100 + 300 + 2030 + 140) = 150000$

5.2.3 Interrogator test (Normal Operation)

5.2.3.1 Interrogator Plot Software Overview

The *Interrogator Plot* Software is a program developed by Tellumat, and it is used to display targets on a map, based on the information received from the interrogator connected to the system. The software mainly comprises two windows, namely, a Log window and a Display window. The Log window of the Plan Position Indicator (PPI) Map Display Graphic User Interface (GUI), shown in Appendix B, allows the user to view the target reports received from the interrogator. The target report contains the following information, which can be saved by the user for playback at a later stage:

- Distance of target
- Angle of target
- Reply code of target (Reported height of target in case of Mode C)
- Number of hits (replies vs. interrogations)

The Display window of the PPI Map Display GUI, as shown in Figure 51, plots a target on a map from the target reports received from the interrogator. The target is displayed on the map with the associated reply mode and reply data. For Mode C, the altitude is displayed with the target.

5.2.3.2 Test Procedure

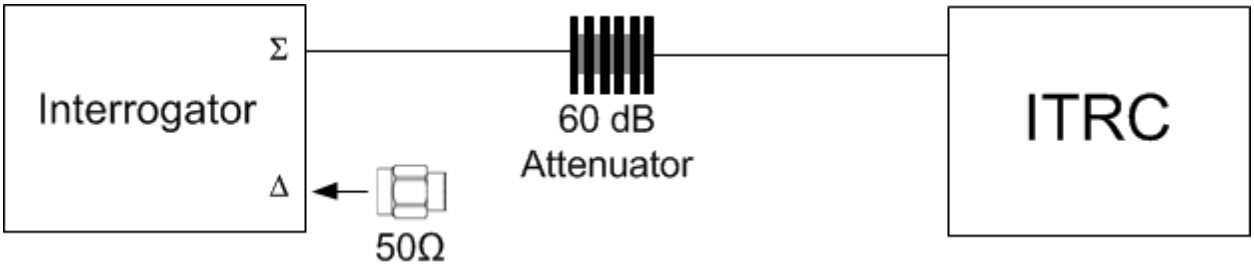


Figure 50: Interrogator Test Setup. A high power 60 dB attenuator is connected between the ITRC board and the interrogator to protect the ITRC receiver from the interrogator output power, which is about +63 dBm. The interrogator's delta channel is terminated with 50Ω.

An SSR/IFF interrogator was connected to the ITRC based on the setup shown in Figure 50. An internal transponder of the IFF Target Emulator was enabled. The Detected Pulse output (recall Figure 30) was internally connected to the transponder challenge input. The ITRC was configured to operate in "Interrogator Test" mode at different output power levels. The interrogator was configured for different modes of interrogation. The internal transponder was configured to reply with different reply delay values equating to an actual distance value. Figure 51 shows a plot report from targets located at 300 km from the interrogator and replying on all modes except Mode 4. Each mode has been tested individually at 50 km and 300 km, using different power levels. The plot reports are contained on a CD accompanying this dissertation.

5.2.3.3 Test Results

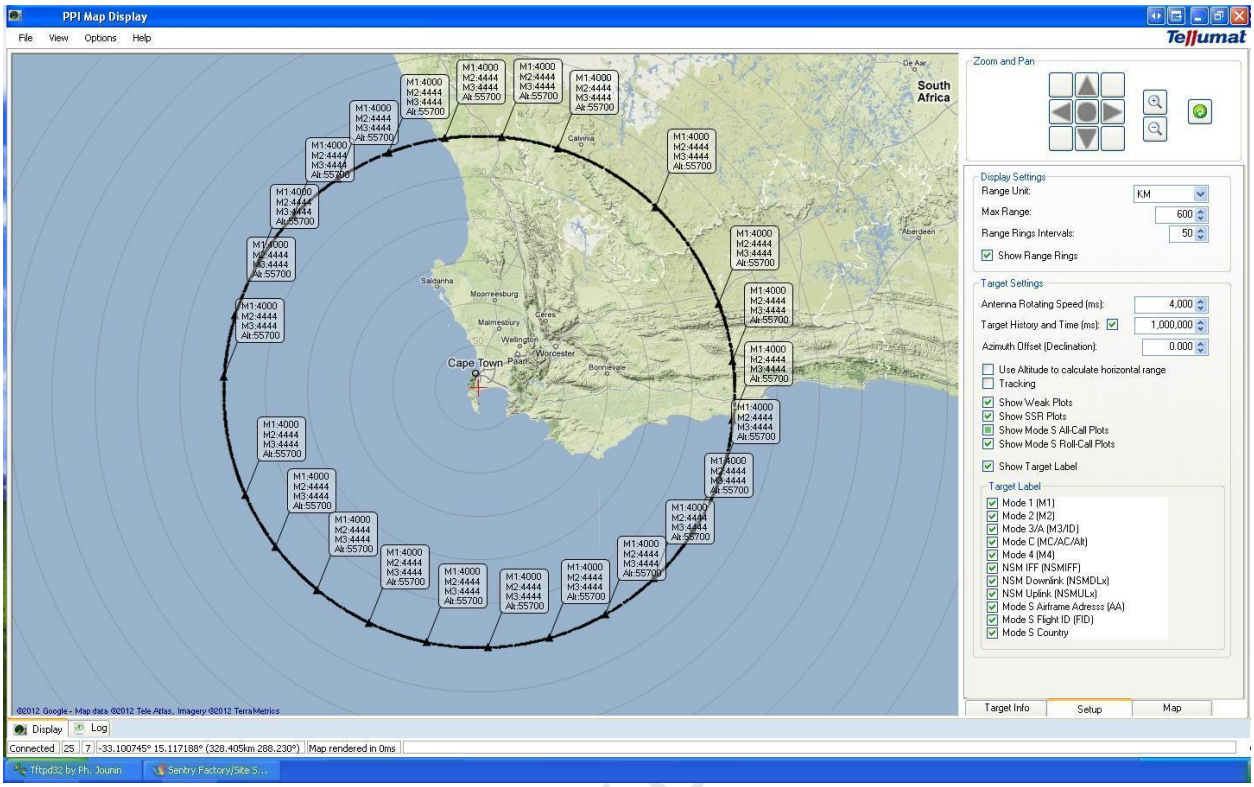


Figure 51: A plot shows targets replying in modes 1, 2, 3/A and mode C, which are located at 300 km from the interrogator.

5.2.4 Interrogator Test (FRUIT Reply)

5.2.4.1 Test Procedure

Two internal transponders and two internal interrogators of the IFF Target Emulator were enabled. The detected pulse output, the received interrogation, and the two internal interrogator challenge outputs were internally connected to the transponder challenge input. The two internal interrogators were configured to operate with a different interrogation mode to that of the actual interrogator.

The ITRC was configured to operate in “Interrogator Test” mode at different output power levels. The interrogator was configured for different modes of interrogation. The internal transponder was configured to reply with different reply delay values equating to an actual distance value. Figure 52 below shows the captured interrogator plot report.

5.2.4.2 Test Results

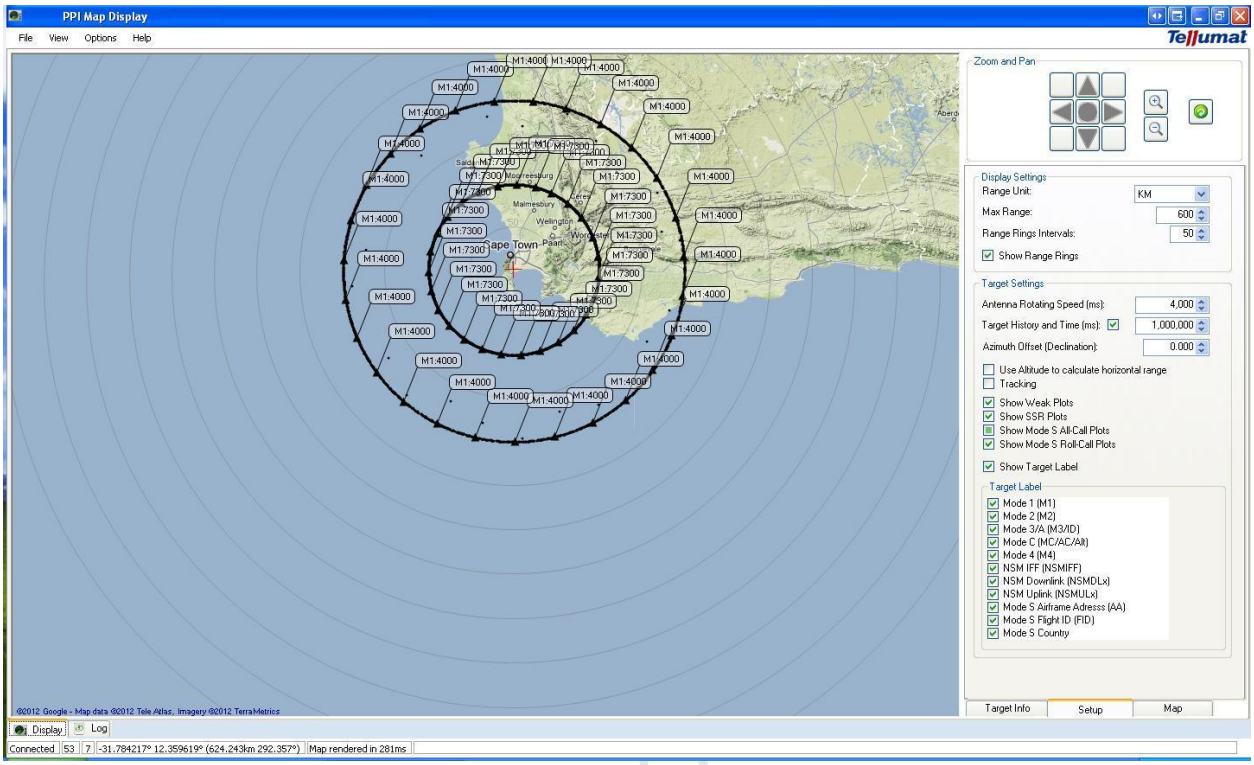


Figure 52: FRUIT reply scenario. When the ITRC received an interrogation in Mode 1, replies in Mode 1 were generated from two internal transponders configured to reply with different reply delay values. The interrogator report included normal (expected) replies from targets located at 100 km and unexpected replies from targets located at 200 km from the interrogator.

5.2.5 Interrogator Test (Garbled Reply)

5.2.5.1 Test Procedure

The ITRC was configured to operate in “Interrogator Test” mode. Two internal transponders of the IFF Target Emulator were enabled.

The first transponder was fixed in position at a distance of 200 km and set to reply between 100 and 164 ACP counts (8.8 and 14.4 degrees). The reply code for this transponder was set to 4000.

The second transponder was configured to move in a circle at a distance of 200 km, starting at 4 and 64 ACP counts (0.35 and 5.6 degrees). The reply code for this

transponder was set to 7300. The interrogator plot reports were captured to confirm operation.

5.2.5.2 Test Results

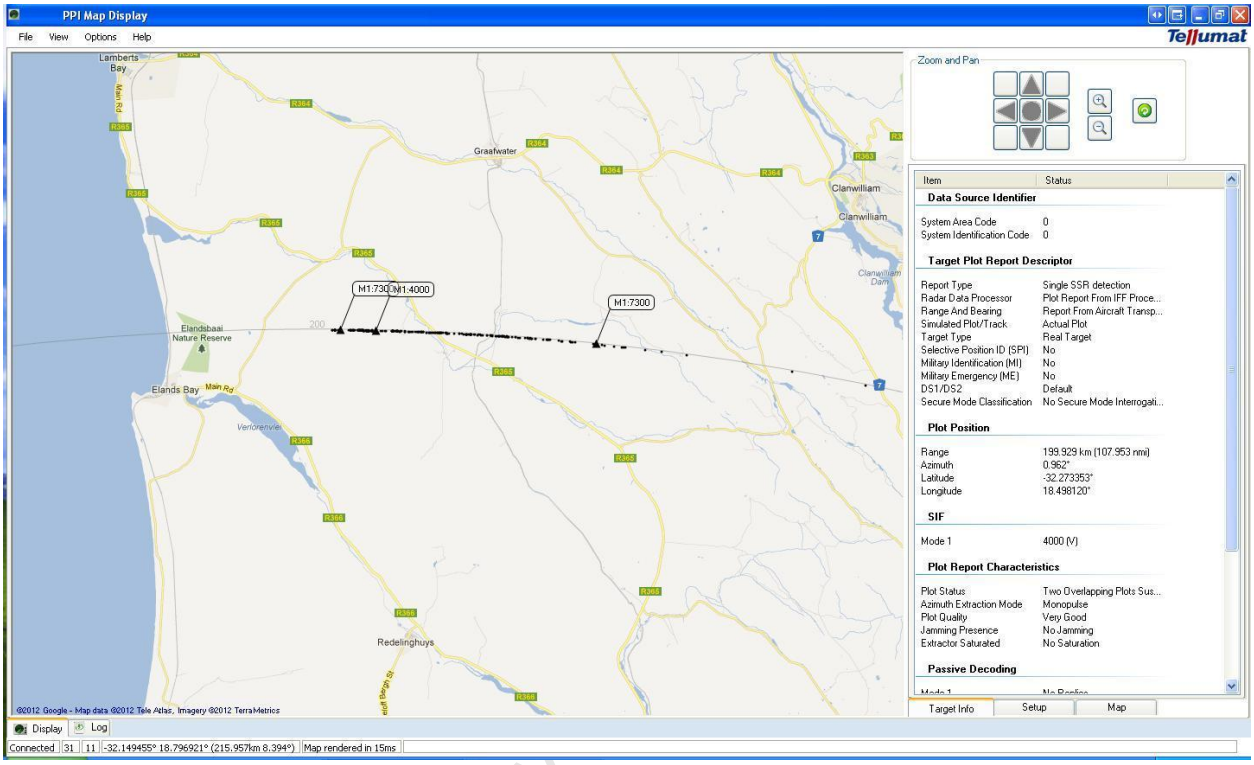


Figure 53: Garbled reply scenario. The interrogator could not distinguish the fixed target from the moving target due to the overlapping between the replies coming from them.

As this test involves a moving target, which eventually overlaps with a fixed target, not much information could be obtained from the screen capture of the targets overlaid on the map in Figure 53. From the file “DecodedPlotReports.txt”, which can be found on the CD accompanying this dissertation, it can be seen that both target transponders are decoded from time 20:02:47 to 20:21:18.

From time 20:21:18 to time 20:24:33, however, only the moving target is decoded. This implies that the interrogator could not discriminate between the fixed target and the moving target, when their replies were overlapping with one another. The moving target

could be decoded, however, as part of the replies were not overlapping with those of the fixed target.

From time 20:24:33 to time 20:46:23, it can be seen that the interrogator was again able to start decoding both targets. This indicates where the moving target has moved past the fixed target.

5.2.6 Transponder Test

5.2.6.1 Test Procedure

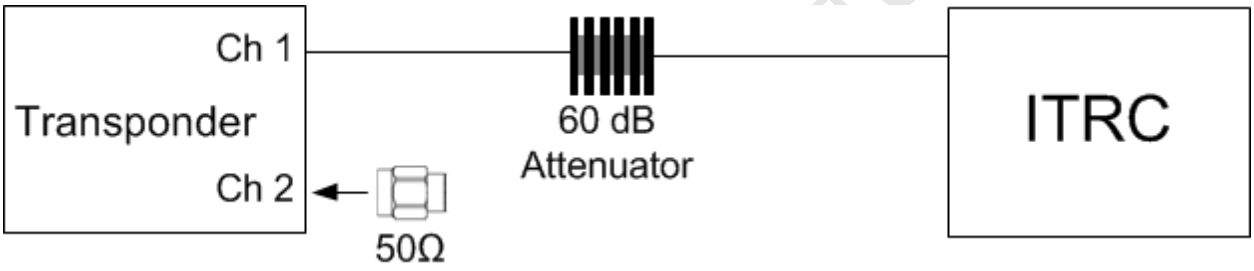


Figure 54: Transponder Test Setup. A high power 60 dB attenuator is connected between the ITRC board and the transponder to protect the ITRC receiver from the transponder output power, which is about +55 dBm. One of the transponder's channels is terminated with 50Ω.

The ITRC was connected to an SSR/IFF transponder based on the setup shown in Figure 54. An internal interrogator of the IFF Target Emulator was enabled. The ITRC was configured to operate in "Transponder Test" mode at different output power levels. The internal interrogator was configured for different modes of interrogation. The transponder was configured with preset reply codes. The Reply data register and Reply delay register was read to confirm the preset reply code and reply delay, as illustrated in Table 20 below.

5.2.6.2 Test Results

Table 20: Reply data register and reply delay register values.

Interrogation Mode	Transponder Code	Detected Reply Code	Detected Reply Delay (Clock Cycle)
Maximum Power			
1	1100	0x1100	2790±2
2	2250	0x2250	2991±2
3/A	3333	0x3333	3309±2
C	5440	0x5440	4613±2
Minimum Power			
1	1200	0x1200	2790±2
2	2250	0x2250	2991±2
3/A	3333	0x3333	3309±2
C	5440	0x5440	4613±2

5.3 Summary

This chapter described the procedure used to test and verify the ITRC system. It began with testing the various ITRC analogue sections and presenting the results; it was found that these results satisfied the user requirements. Functional test procedures were then performed, by connecting the ITRC to a transponder and an interrogator, to test the ability of the ITRC system to communicate with SSR/IFF equipment. The results showed that the ITRC was indeed able to achieve all the required functional tests except Mode 4 tests, which could not be performed due to the unavailability of a cryptographic-computer during the test phase. Due to the large size of the test results, these have been copied onto a CD accompanying this dissertation. The next chapter will conclude the project and suggest areas for future improvements.

6 Conclusions and Future Work

This chapter documents the conclusions of the project based on the results and performance achieved with the designed system and presents the recommendations to improve the receiver's performance.

6.1 Project conclusions

The overall goal of this project was to create a transceiver that, when integrated with the SSR/IFF reply emulator, would be capable of generating and processing SSR/IFF RF interrogations and replies.

In Chapter 2, the user requirements related to the SSR/IFF Transceiver Card (ITRC) project were presented. These requirements were analyzed in Chapter 3, which led to the breakdown structure of the ITRC. The ITRC requirements were derived from studying each of the ITRC subsystems. Chapter 3 also summarized the capabilities of the SSR/IFF reply emulator. The design of the analogue and digital parts of the ITRC has been described in Chapter 4. The descriptions of each analogue subsection began with a block diagram defining the relevant stages of the subsection. The block diagram was then simulated, which guided the choice of the components used in the design. Chapter 4 also presented the VHDL modules, which have been added to the SSR/IFF reply emulator in order to satisfy the user requirements. The procedure used to test and verify the ITRC system was described in Chapter 5.

Base on the test results, the ITRC is found to be compliant with the user requirements in Chapter 2 except that one of these, namely, the transmit interrogations with P2, have a variable amplitude. This requirement could not be satisfied due to the big change that would need to be made in the DSP and FPGA codes of the SSR/IFF emulator. Unfortunately, at the time these tests were performed, a cryptographic-computer was unavailable, however, and thus it was not possible to perform the mode 4 tests.

6.2 Recommendations

The following are some recommendations for possible future improvements to the ITRC system.

- In order to allow the ITRC system to communicate with targets at ranges beyond one kilometer, the ITRC transmit channel gain has to be improved to generate more than +18 dBm and the receive channel have to be developed to be sufficiently highly sensitive.
- Currently the amplitude of the generated RF pulses is not adjusted dynamically. In order to do this, the software of the SSR/IFF reply emulator will have to be changed to accommodate passing on the value of the programmable attenuator to each internal transponder. This will also affect the FPGA code, as each generated transponder will have to send the attenuator setting on a pulse by pulse base to some arbitrator. The function of the arbitrator will be to set the attenuator to the appropriate value. This will be very important in the case where pulses overlap.
- In the current system, to generate targets and configure the operating modes of the ITRC, the DSP software has to be changed and recompiled. The DSP software could be updated and software for the front-end could be developed to be able to do this without requiring recompilation.
- The *Quixote* board, as an expensive board, could be replaced with a less expensive digital board that already has a DSP and FPGA compatible with the digital design requirements.

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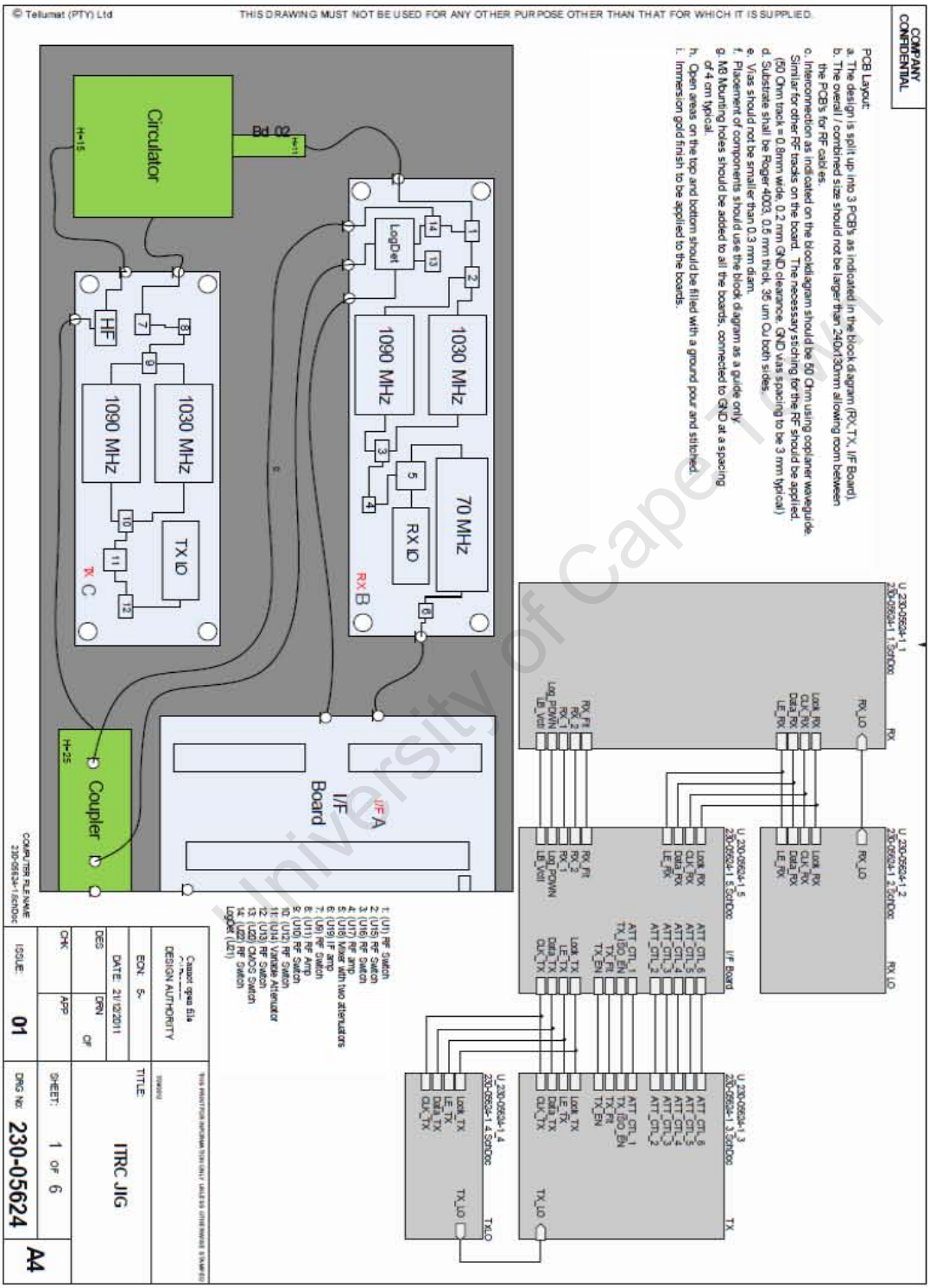
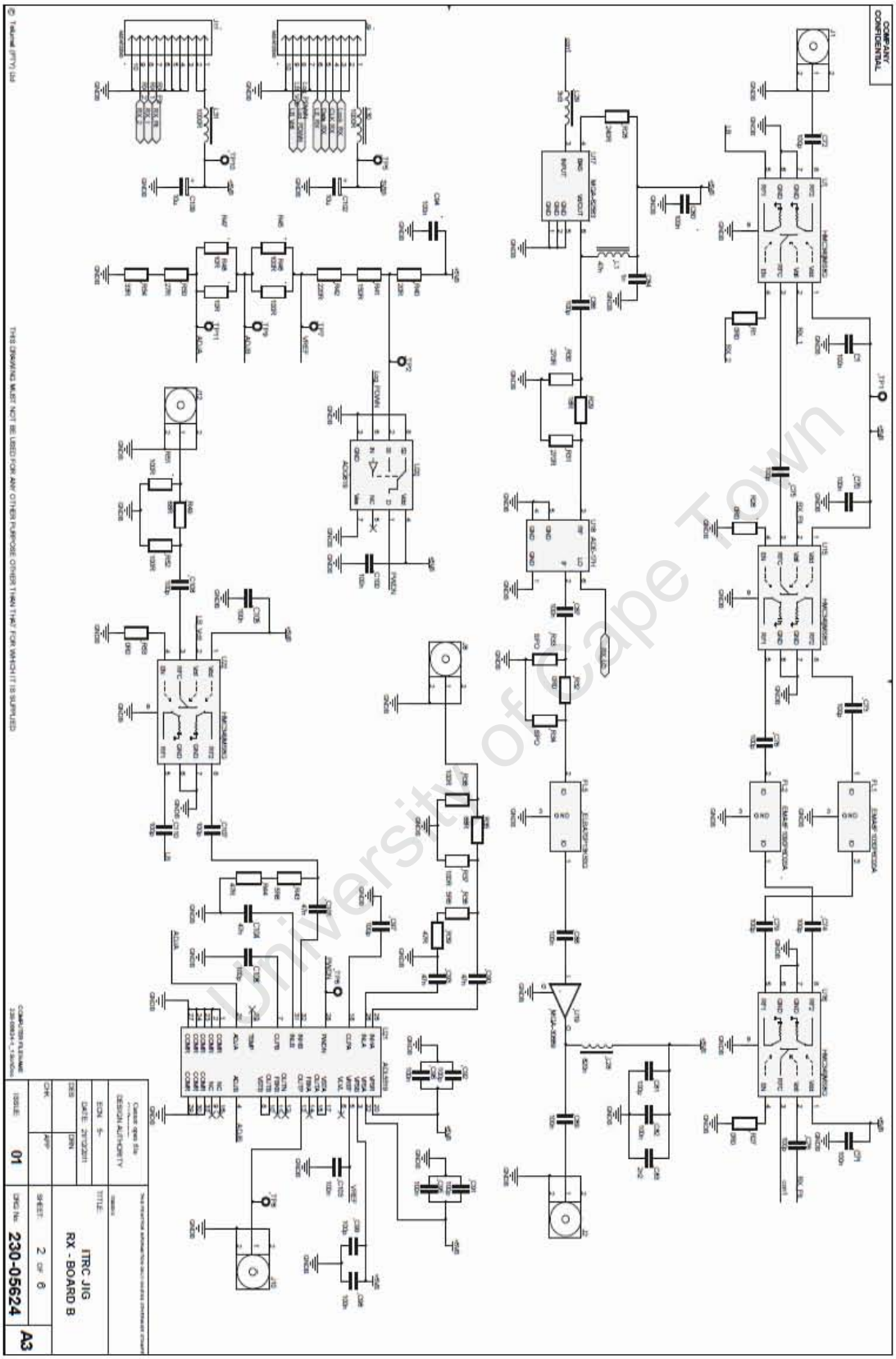
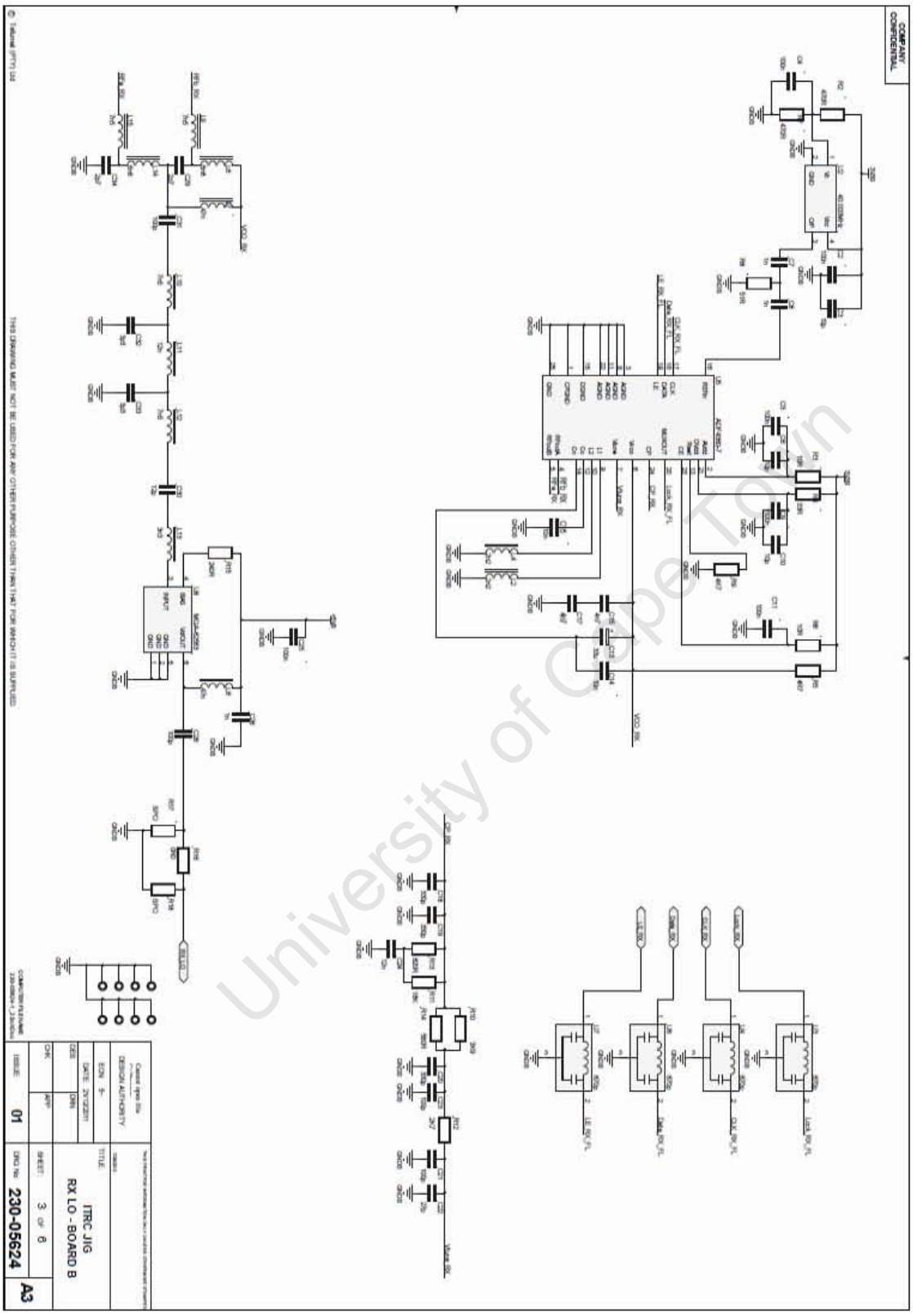
Appendix A: ITRC Schematic Using Altium Designer Software



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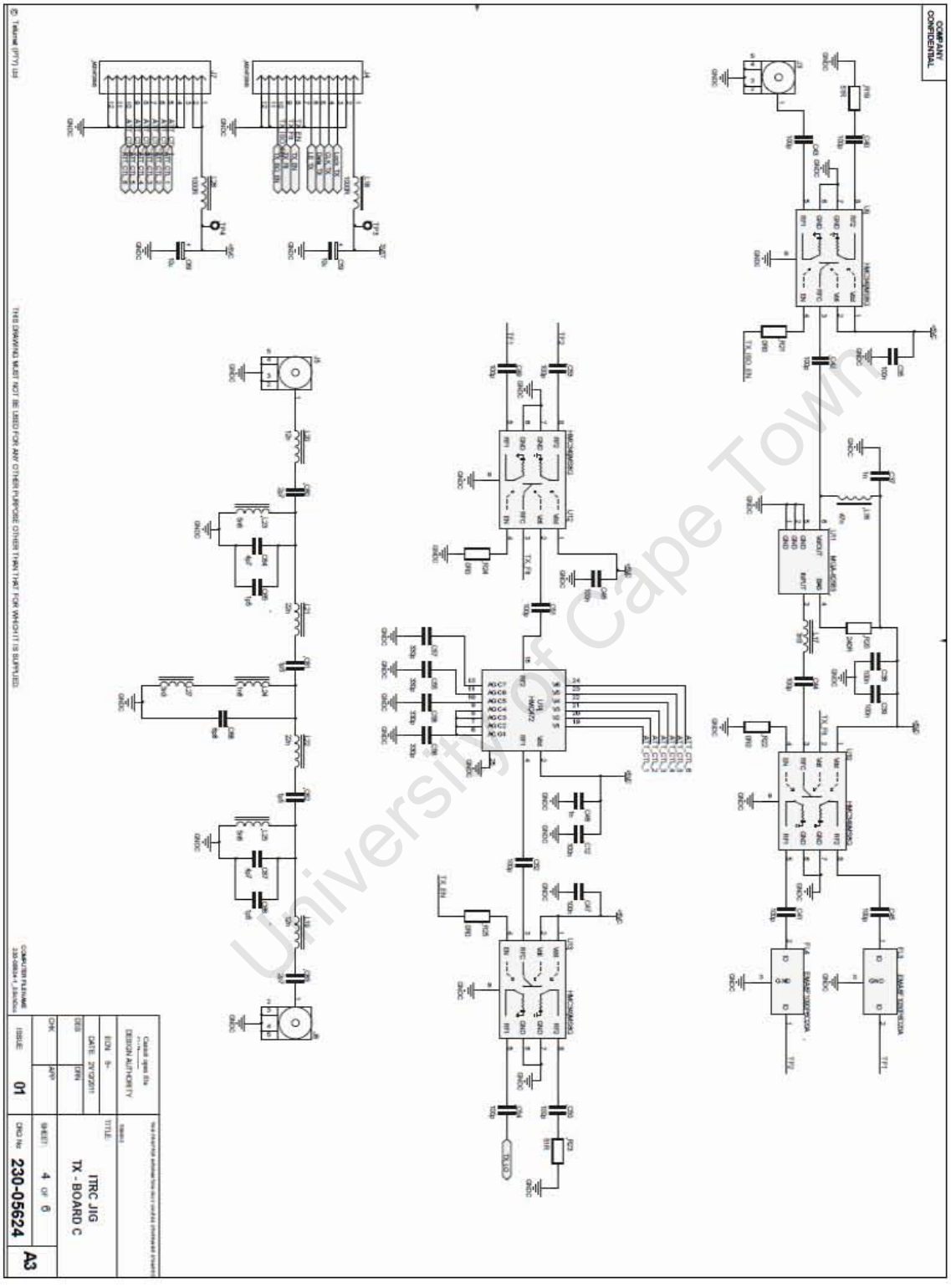

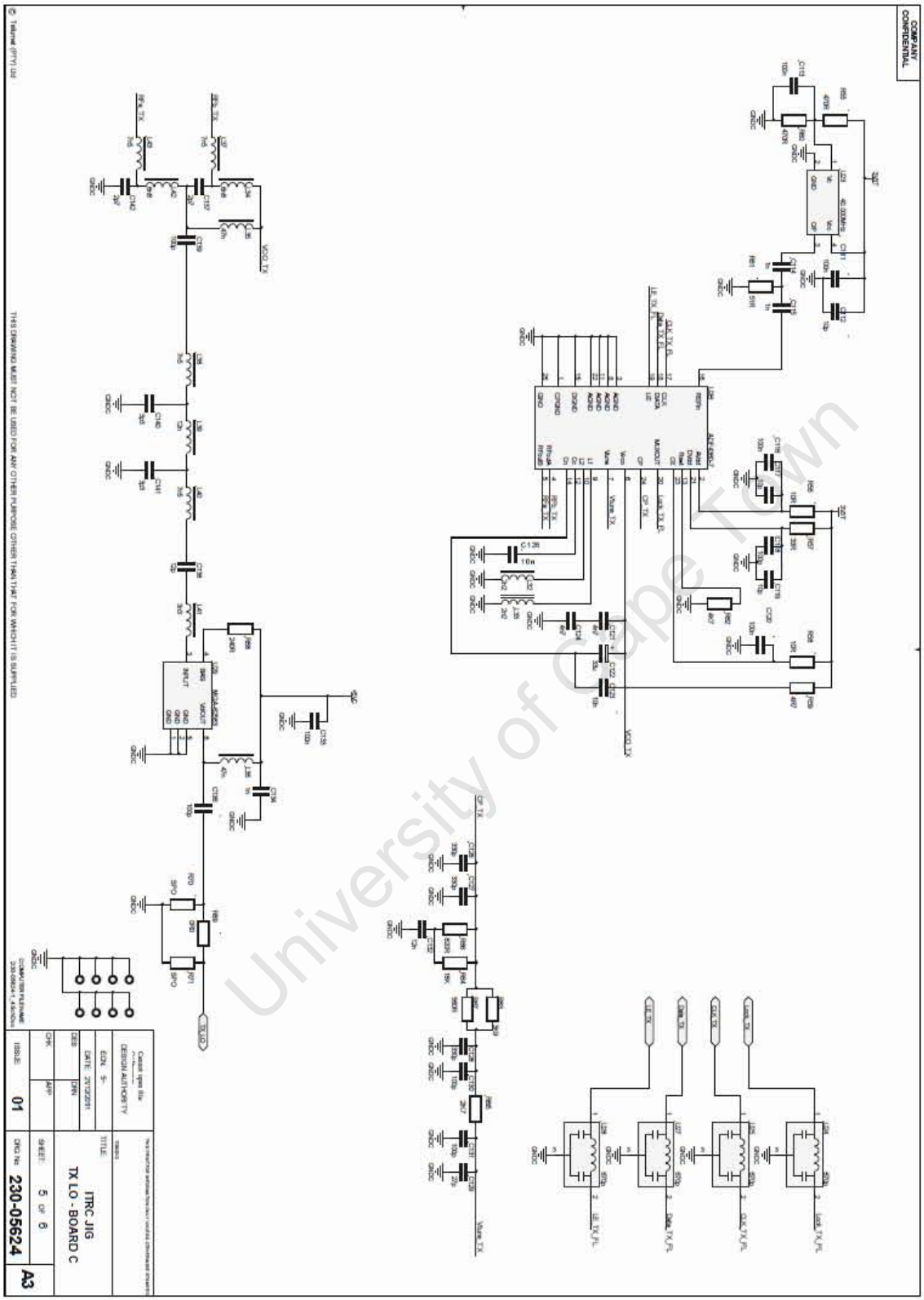
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DATE 27/07/2011
THIS DRAWING MUST NOT BE USED FOR ANY OTHER PURPOSE OTHER THAN THAT FOR WHICH IT IS SUPPLIED
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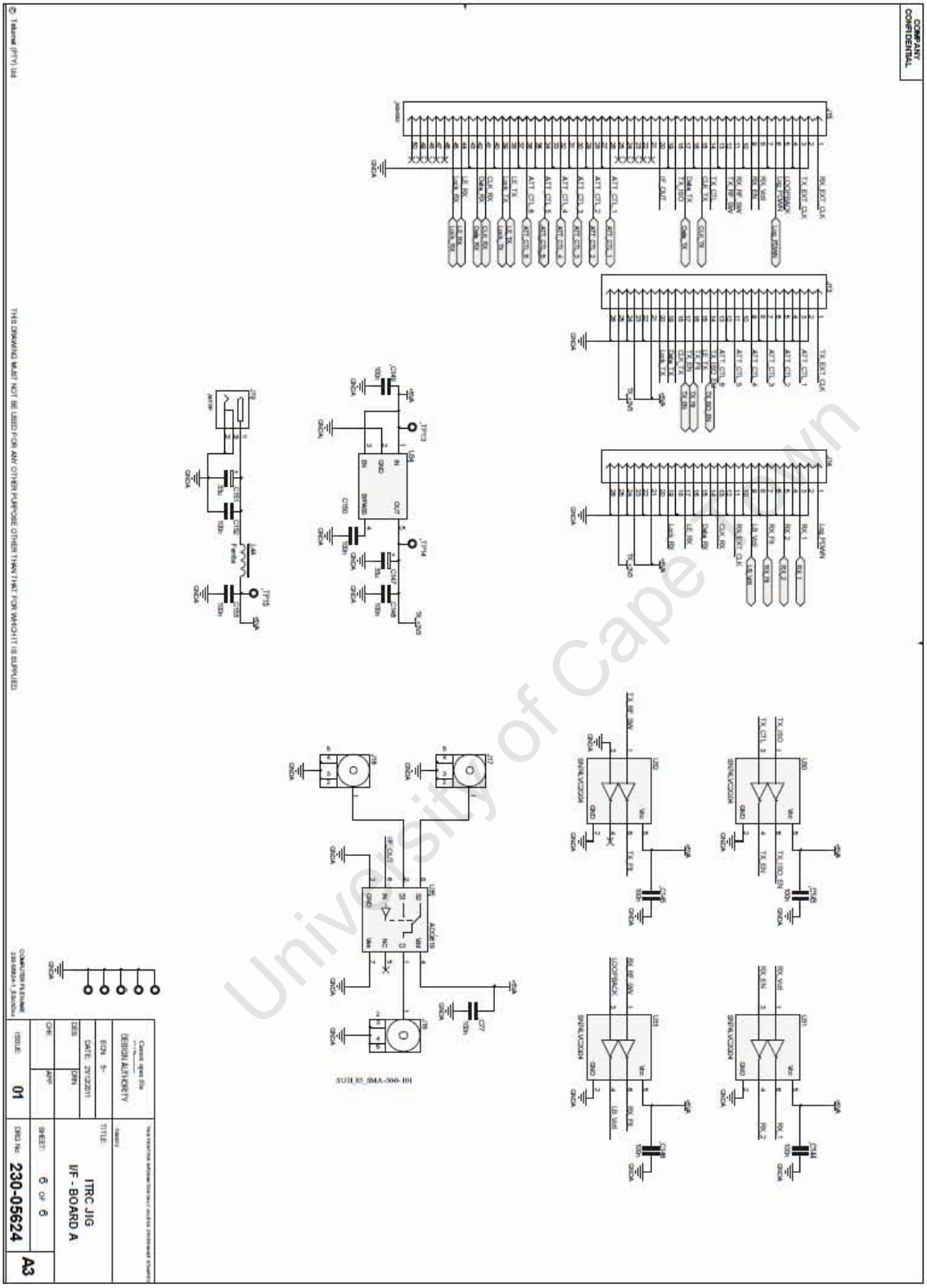
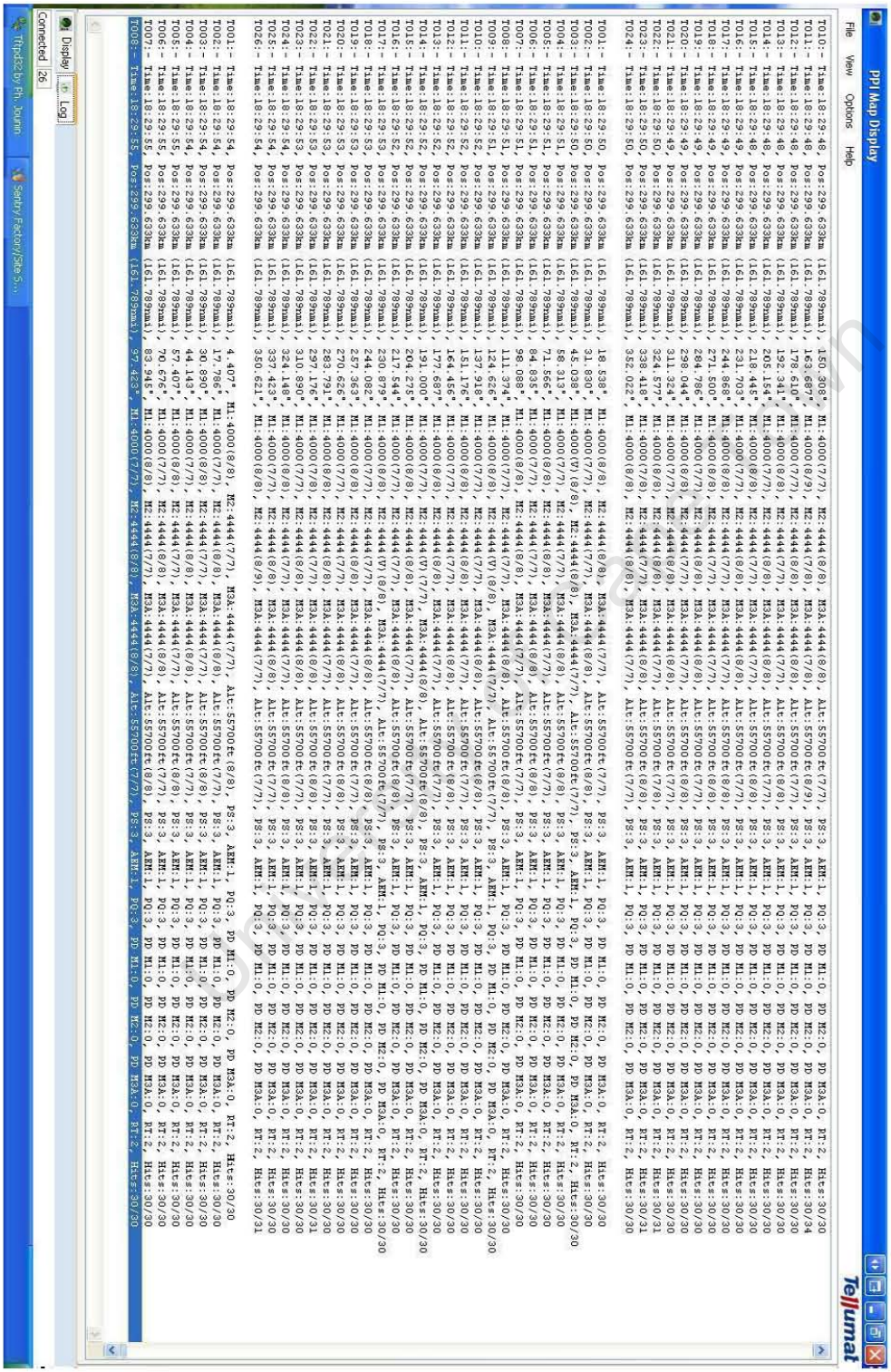


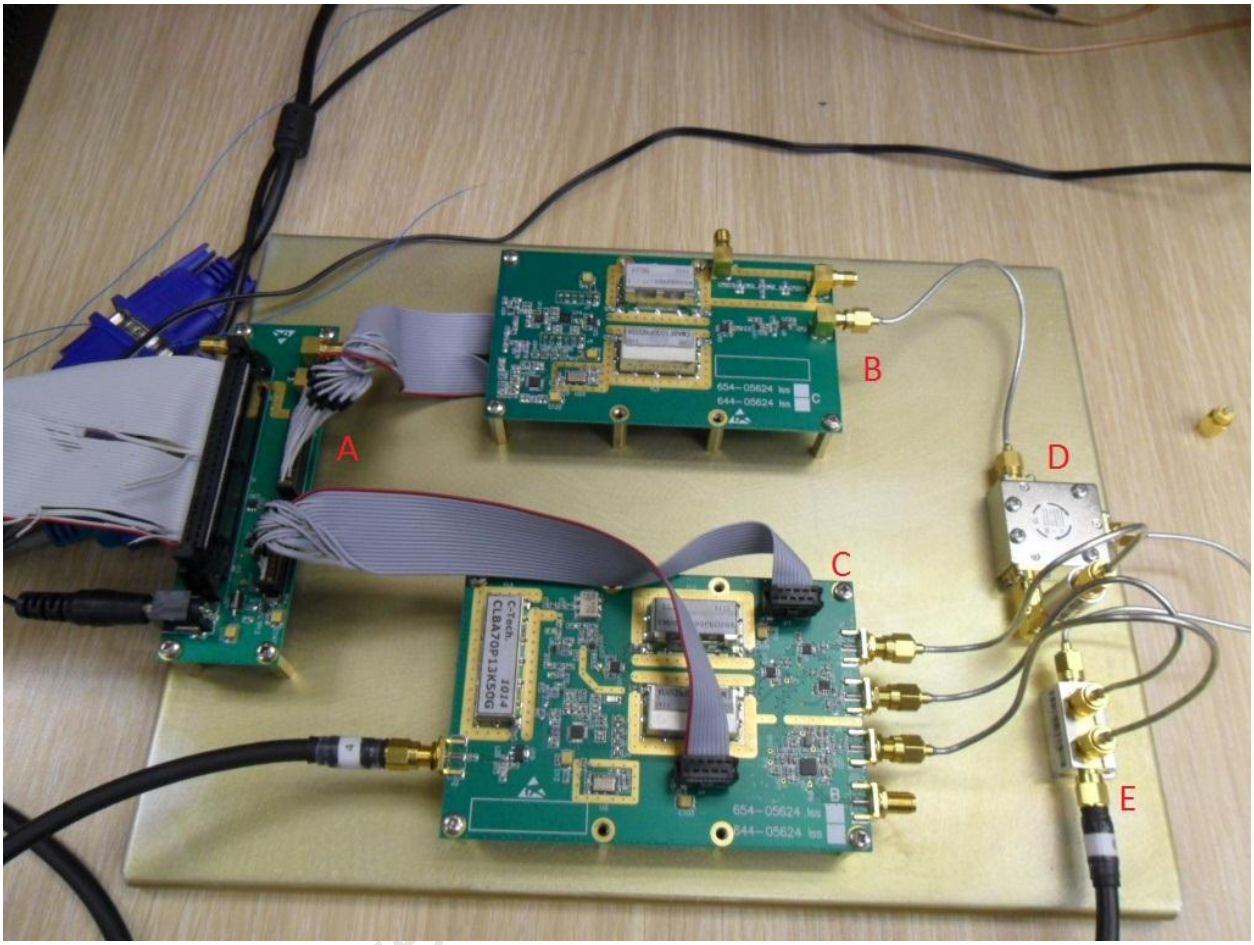
Appendix B: Log window of the PPI Map Display GUI



Appendix C: CD Contents

- Copy of the dissertation.
- Interrogator test results (Normal reply, garbled reply and FRUIT reply).
- ITRC Demodulator Simulink model.
- FPGA VHDL code.
- DSP C code.

Appendix D: ITRC Boards



A: Interface board to the Quixote digital board.

B: Transmitter board.

C: Receiver board.

D: RF circulator.

E: Dual directional coupler