AN INVESTIGATION INTO GAIN AND GROUP DELAY MEASUREMENT FOR DIGITAL MICROWAVE RADIO

by
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Submitted to the University of Cape Town in partial
fulfillment of the requirements for the degree of
Master of Science in Engineering.

DECLARATION

I declare that this thesis is my own unaided work and is being submitted to the University of Cape Town in partial fulfillment of the requirements for the degree of Master of Science in Engineering. It has not been submitted before to any other university for any degree or examination.

Signed by candidate

D.B.GAMMON 28 April 1990

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ABSTRACT

Digital Microwave Radio is increasingly replacing analogue systems on line-of-sight microwave links. These systems are particularly susceptible to channel linearity and group delay distortion caused by multipath fading. A simple, inexpensive method of measuring gain and group delay over a link is called for. This is required to have sufficient dynamic range and speed to cover the fast, deep frequency selective fades associated with multipath fading. A brief overview of multipath fading and its measurement is given.

The design and construction of a simple, prototype PC-based gain and group delay measurement system for a loop-back arrangement is described. This system is based at the IF frequency. It consists of hardware/software interfaces, an IF frequency synthesizer/generator, gain measurement, group delay measurement, and control and processing software. The IF frequency is swept over the frequency band, either in a synthesized manner, or in a fast, non-synthesized manner and measurements taken during the sweep. These are displayed by the software. Gain measurement is performed by comparison of amplitudes of the IF signal and group delay measurement by phase comparison of a modulation of the IF signal. A method is given to extend the system to an end-to-end measurement.

The existing system is capable of measuring gain and group delay in a loop-back system at the required speed and with the required amplitude range. Some problems exist in the accuracy, range and resolution of the group delay measurements and in the matching for gain measurements. Recommendations are made to correct these in an end-to-end measurement system.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figures Page

Tables

NOMENCLATURE

DMR : Digital Microwave Radio. Microwave radio networks employing digital coding and modulation schemes.

IC : Integrated Circuit.

IF : Intermediate Frequency.

LOS : Line-of-Sight. A microwave path in which the receiver is in sight of the transmitter.

MLA : Microwave Link Analyzer. A device used in analyzing the propagation characteristics of a microwave path.

PC : Personal Computer.

RF : Radio Frequency.

f : Frequency of a signal.

f_m : Frequency of modulating signal.

ϕ : Phase difference of a signal.

ϕ_m : Phase difference of modulating signal.

ϕ_a : Phase difference of IF signal.

τ : Group delay of a signal.

τ_m : Group delay of modulating signal.

τ_a : Group delay of IF signal.

CHAPTER ONE

INTRODUCTION

Line of sight (LOS) microwave radio relay links are at present the backbone of telecommunication networks. Despite the introduction of optic fibre, its expense indicates that LOS links are likely to continue to be important for a long time in the future [1.1].

The trend in the 1980's has been for digital microwave (DMR) radio systems to replace analogue systems. The digital system is often overlaid, as much as possible, on the existing analogue network. In order to obtain high signaling efficiency, high speed digital transmission systems make use of complex modulation and coding schemes (for example PSK, QAM, QPRS). These phase/amplitude modulation techniques are far more sensitive to channel linearity and group delay distortion than analogue FDM systems. This is particularly so when the digital system uses the same relatively long hops of the analogue network.

Of the various types of fading that can occur on a microwave link, causing distortion of the received signal, digitally modulated signals are particularly susceptible to distortion caused by multipath fading. Tests have indicated that they are 10 to 12 times more sensitive than analogue systems [1.2] and this is a fundamental limitation to increased bit rates [1.3].

In order to observe and predict distortions that may occur on existing and proposed links, especially for the introduction of DMR onto a link, a cost effective method of measuring distortion parameters over a lengthy period of time is called for. This will help the link engineer to design systems with optimized transmit power, antenna size and position, hop length and equalization. This should result in improved bit error rates and a lower system outage time.

1.1 MULTIPATH FADING

When the level of the signal at the receiver end of a LOS link decreases, the signal is said to be faded. This fading may be flat, affecting all frequencies similarly, or selective, affecting only certain frequencies. Fading caused by hydrometers such as rain, mist, hail and snow affect frequencies above 10GHz and is non-selective [1.4]. Selective fading, caused by the signal travelling from transmitter to receiver via more than one path, is known as multipath fading. As the paths differ in length, the combined signal at the receiver is distorted in amplitude and phase, depending on the wavelength [1.5].

A number of factors may cause multipath conditions to occur. The most common causes are additional paths to the direct path from transmitter to receiver, as a result of reflection or refraction. Reflection may arise from elevated layers of discontinuity in temperature or humidity, or from ground or water reflections. Flat, arid plains and even ploughed fields can exhibit reflection coefficients of up to 0.9. Sheets of water, particularly close to the midpoint of a link are notorious sources of reflection. It is thus important to avoid such conditions in choosing the sight of repeater stations.

In some literature (for example [1.6]), the term multipath is reserved for the situation where the multiple paths are caused by refraction alone. These conditions occur because of the varying refractive index of the air, which is altitude dependent and also time variant. These conditions can be either stable or turbulent. Multipath fading due to refraction is most severe in stable conditions on quiet, windless, misty nights when temperature inversions occur. This forms ground based or elevated stratified layers and the signal is refracted (and partially reflected) [1.7, 1.8].

The various types of fading, with the typical form of amplitude distortion they cause are shown in Figure 1.1.

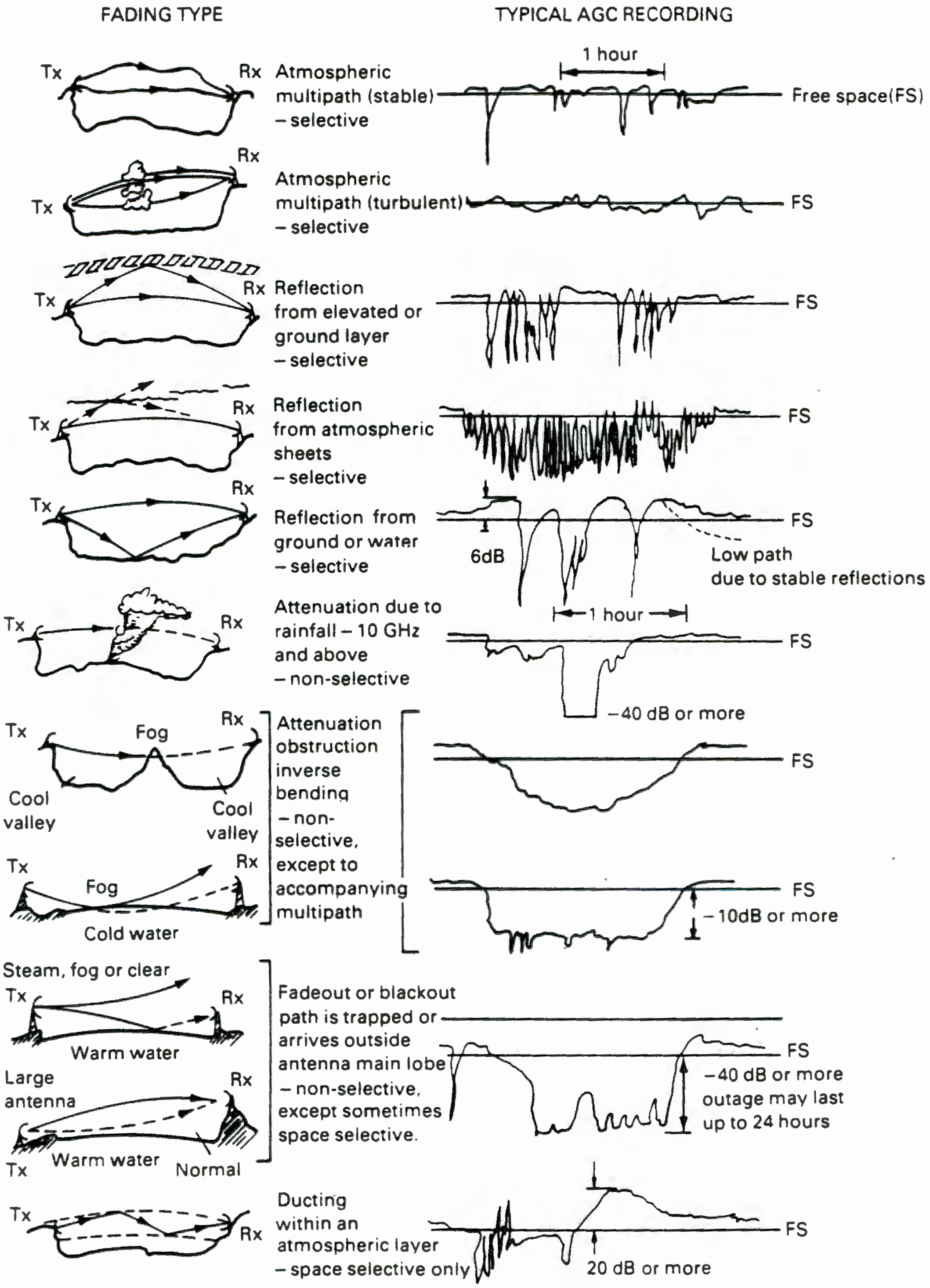


Figure 1.1 Categories of Fading Events [1.9]

selective fadings in contrast to the flat fadings caused by precipitation. This is most pronounced during conditions of stable refractive multipath. The deep selective fadings occur because the number of propagation paths is small (being from two to five), no one path has a dominating signal and the lengths of the individual paths differ by at least a few tenths of a metre, corresponding to relative delays of a few nanoseconds or more [1.10]. The fades are also time dependent.

The primary manifestation of multipath fading is amplitude and group delay distortion across the channel bandwidth. In the case of DMR, this can cause severe intersymbol interference at the receiver, resulting in a high bit error rate [1.11]. The fades can be very deep, up to 60dB in amplitude and these notches can travel across the frequency band very rapidly. Frequency shifts of up to 100MHz/sec in the IF band can be expected [1.12].

Multipath fading was tolerated on analogue microwave paths for many years because of the resistance of FM systems to the linear amplitude distortion component that predominates in this type of fading [1.13]. The first investigations of multipath fading on LOS links were done in the 1950's, notably by Bell Laboratories [1.14, 1.15], but only since the introduction of high capacity DMR in the 1970's has there been a growth of interest in multipath fading. There is extensive literature on many aspects of the subject. These include statistical observations of multipath behavior on links over an extended period of time [1.16 - 1.20], measurement of multipath parameters [1.21 - 1.24], mathematical models and simulations for multipath behavior and their conformance to observed conditions [1.25 - 1.29] and affects on digital radio [1.30]. A large proportion of the later references relate specifically to multipath in digital radio systems. Most of these experiments are performed on existing links.

1.2 MEASUREMENT OF DISTORTION CAUSED BY MULTIPATH FADING

1.2.1 Multipath Models

A number of mathematical models have been proposed to simulate multipath propagation in order to characterize fading channels statistically. The most widely accepted and used is the three-path model proposed by Rummler [1.31]. This has a better correlation with measured data than the initial two-ray model.

With such a model a so-called signature can be determined for a link, giving a locus of fade notch depths and frequencies, to predict radio system outage. These models will not be discussed here and the reader is referred to [1.32, 1.33] for a description.

1.2.2 Multipath Parameters

The criteria for distortionless transmission fall in two parts. Firstly the amplitude (magnitude) response should be flat over the bandwidth of interest, meaning that all frequencies within the bandwidth should be attenuated identically. Secondly the phase response must be linear over the bandwidth [1.34]. This is because the phase change of a signal over a link is proportional to its frequency, being given by

$$\phi(f) = 360.\frac{f.l}{c} \quad \text{[degrees]} \quad \ldots\ldots\ldots\ldots \quad (1.1)$$

for an airlink, with l = length, f = frequency and c = speed of light.

A more useful technique to determine phase distortion is group delay. This is defined as the derivative of the phase response with respect to frequency:

$$\tau(f) = \frac{-1}{360}.\frac{d\phi}{df} \quad \text{[Seconds]} \;.......... \;(1.2)$$

with ϕ the phase in degrees.

From (1.1): $$\tau(f) = \frac{-1}{c} \quad \text{[Seconds]} \;.......... \;(1.3)$$

Thus, distortionless transmission should give rise to constant group delay over the desired bandwidth.

The distortion resulting from multipath (and other) fading effects causes linear distortion, as opposed to non-linear distortion caused by non-linearities in the circuitry (such as intermodulation). Linear distortion is a deviation from constant amplitude and/or deviation from linear phase or constant group delay, over the bandwidth.

Variations in amplitude are caused by the multiple signals adding at the receiver in different phase relationships. Variations in group delay are caused by the effective action of different frequencies in the signal travelling at different speeds during multipath conditions. Depending on the lengths of the multiple paths, the different signals take varying times to reach the transmitter. This results in the group delay of the total signal being increased from its direct, single path value by a few nano-seconds to a few tens of nanoseconds, depending on the path lengths.

Two other parameters are also sometimes measured. These are differential phase and differential gain, defined as the difference in phase and gain respectively encountered by a low level, high frequency sinusoid of a superimposed low frequency signal [1.35]. Refer to Figure 1.2 for a comparison between differential phase and group delay. However the most important parameters are gain and group delay.

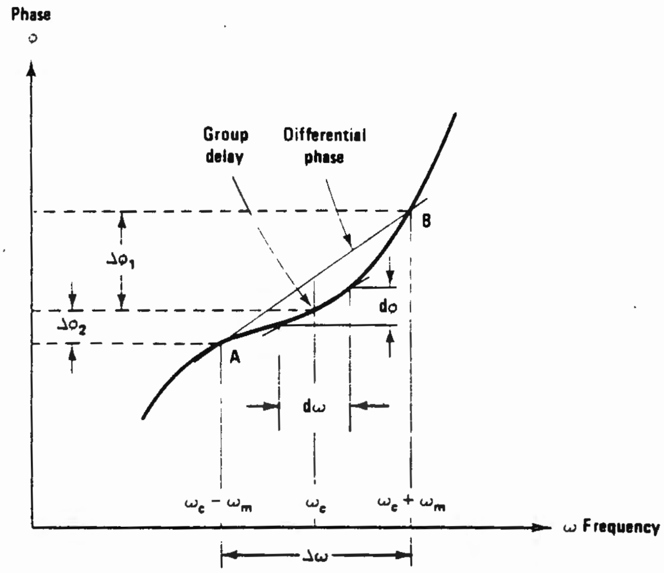


Figure 1.2 Group Delay and Differential Phase [1.36]

Measurements may be performed by sweeping the frequency and measuring distortion parameters at RF or IF, but existing microwave link analyzers invariably perform measurements at IF, as this is available at all stations on a link and is easier to work with. This provides IF gain and group delay characteristics. However, many measurements and extraction of multipath parameters on links have been performed by sweeping the RF (for example [1.37]). Details of multipath parameter measurement techniques for experiments reported in the literature are rare, although most use a frequency sweep and sampling mechanism, or a commercial microwave link analyzer. An alternative to this, for group delay measurement, is the use of short transmitted pulses [1.38, 1.39]. A common form of gain measurement is to record the automatic gain control setting of the receiver. A typical measurement plot from an experiment is given in Figure 1.3.

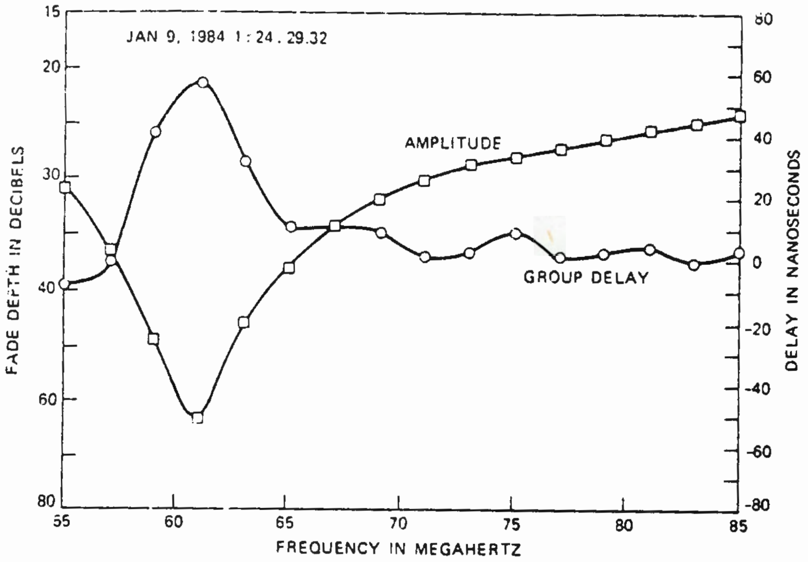


Figure 1.3 Typical Gain and Group Delay Plot of a Fading Event [1.40]

These measurements may be analyzed to trace sources of distortion on a link. The details are beyond the scope of this discussion and may be found in [1.41, 1.42]. It has been estimated that to gain a true representation of the rapidly moving fades characteristic in multipath fading, the IF frequency has to be swept at a rate of the order of 10 sweeps per second [1.43].

1.2.3 The Microwave Link Analyzer (MLA)

The MLA is a sophisticated piece of equipment used for measuring distortion parameters on microwave links. Gain, group delay, differential gain and differential phase can be measured. It is extensively used by the Post Office.

The MLA is inserted in the IF stage of a link and uses a 70MHz sinusoid to sweep the IF bandwidth. The IF can be set to either 35, 70 or 140 MHz centre. A high frequency measuring voltage is superimposed on the swept IF frequency using FM. This results in the swept voltage shifting the working point of the measuring voltage along the transfer characteristic, allowing the measuring voltage to "explore" the characteristic. This is seen in the frequency domain as a line triplet exploring the bandwidth at 70 Hz. This is illustrated in Figure 1.4 for an IF of 140MHz and a sweep deviation of ±18MHz.

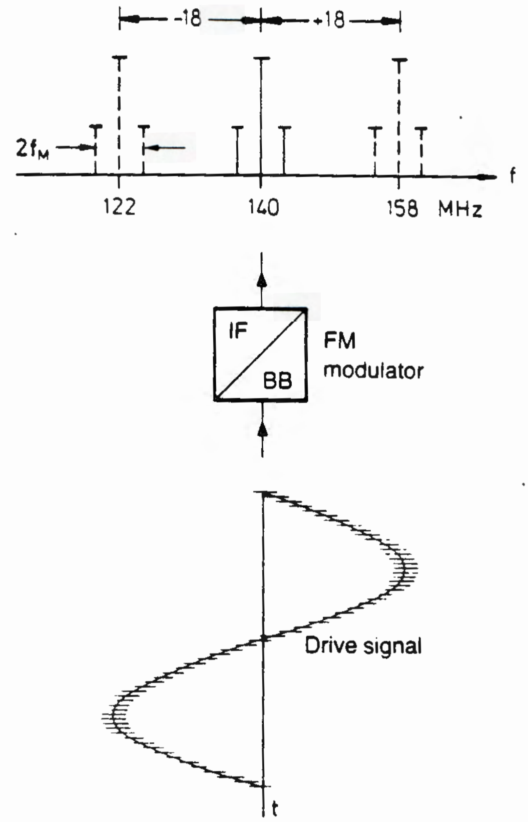


Figure 1.4 Spectral Representation of Frequency Modulated Measuring Signal of MLA [1.44]

Differential phase and differential gain are measured with a measurement voltage of 1MHz or more, while gain and group delay use a measuring voltage of less than 1MHz (usually 500kHz). The demodulated signal at the receiver is displayed using the 70MHz sweep voltage. The different distortion parameters can be displayed and non-linearities seen in the slope of the display. This is known as the intermodulation method. It is illustrated in Figure 1.5 and described in detail in the MLA manual [1.45]. The MLA can cover the required dynamic range of 60dB and can operate at the required sweep speed when outputing the results in an analogue form [1.46].

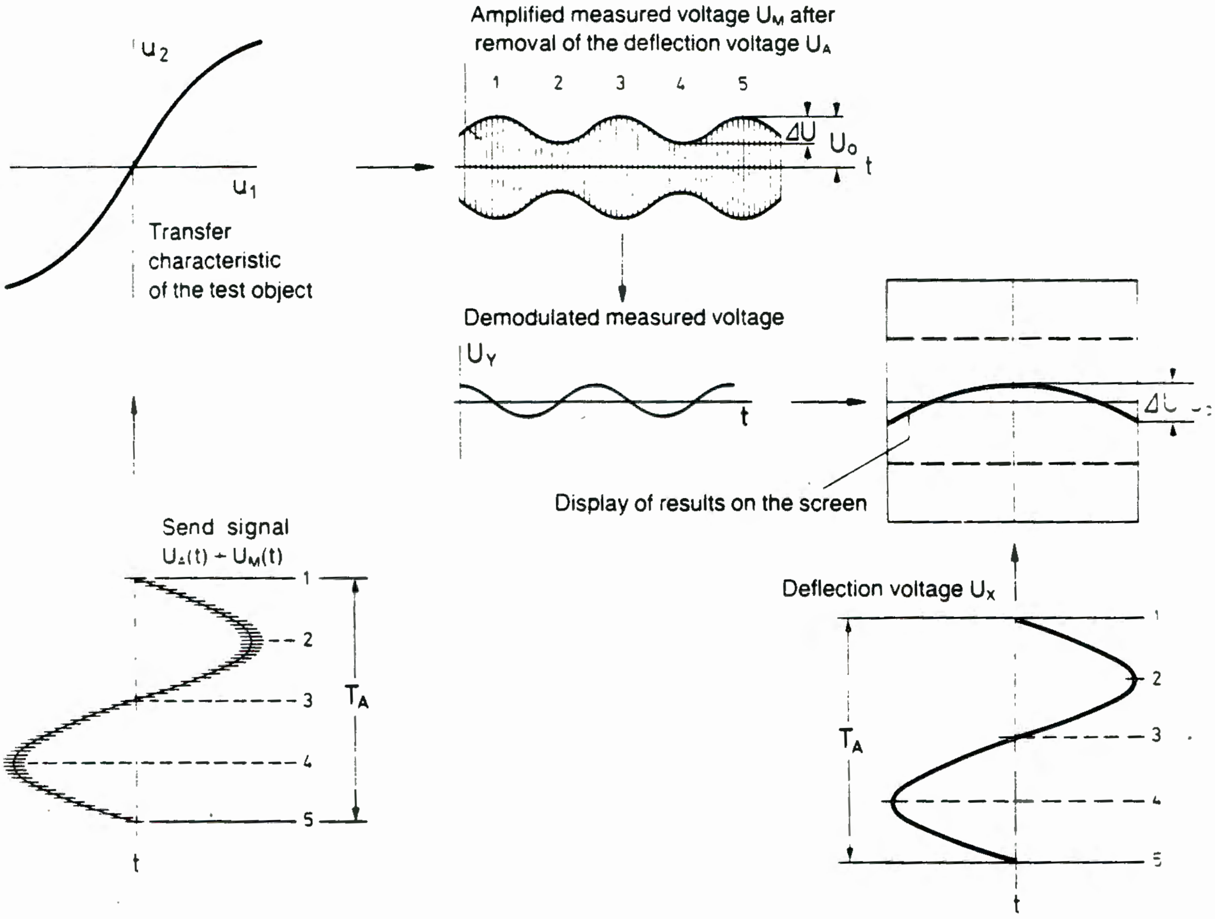
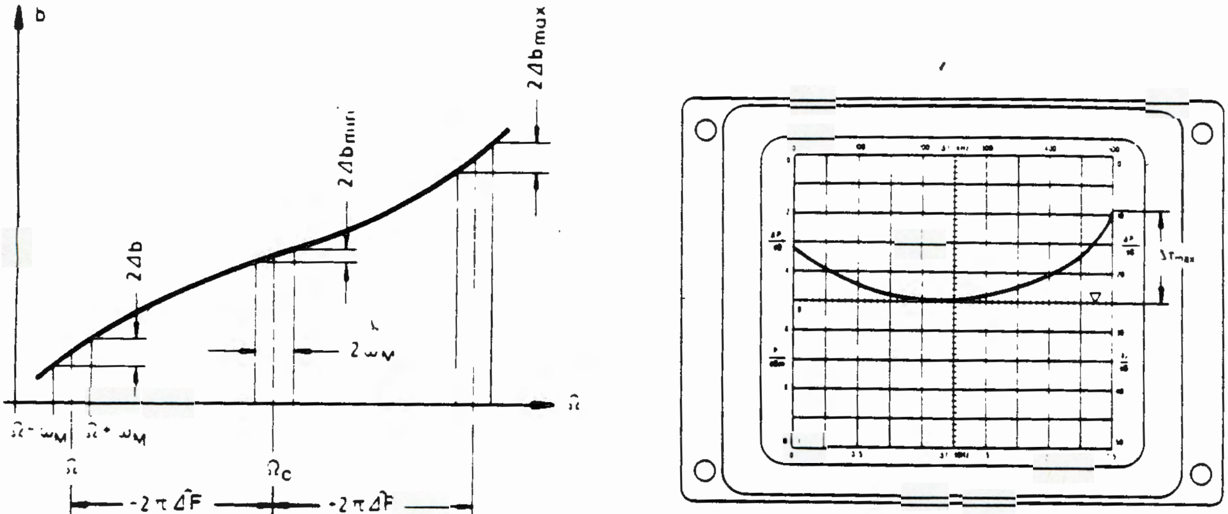


Figure 1.5 Measurement of non-linearity using the Intermodulation Method [1.47]



Sweep width

Curve of the group delay distortion

Figure 1.6 MLA Plot of Group Delay
from Phase Sweep [1.48]

A system for measuring amplitude and group delay conditions on a microwave link using an RME-5 MLA and an intelligent interface to a computer for processing has been described by Donnevert and Greil [1.49]. Forty samples with 1MHz spacing are taken across the IF band. This system allows high speed digitization, processing and recording of measured data on a long term basis.

1.3 PC - BASED MEASUREMENT

Although the MLA provides the link engineer with sufficient information, it is an expensive piece of equipment and it is unrealistic to install instruments on a number of links over a long period of time. The need for cumulative propagation characteristics on microwave links, especially with a view to installing digital systems, within the Department of Posts and Telecommunications in South Africa, resulted in the desirability of a simple, inexpensive path analyzer to be developed. A PC based system provides a convenient means of achieving this, because of the relative moderate cost of the PC.

The subject of the remaining part of this dissertation is therefore the design and construction of a prototype PC-based device, capable of giving an indication of gain and group delay characteristics of a LOS microwave link, over the IF frequency band. It must be stressed that the aim of the project is to develop a simple, inexpensive method of providing basic information on gain and group delay over a link and not to match the sophistication of existing equipment.

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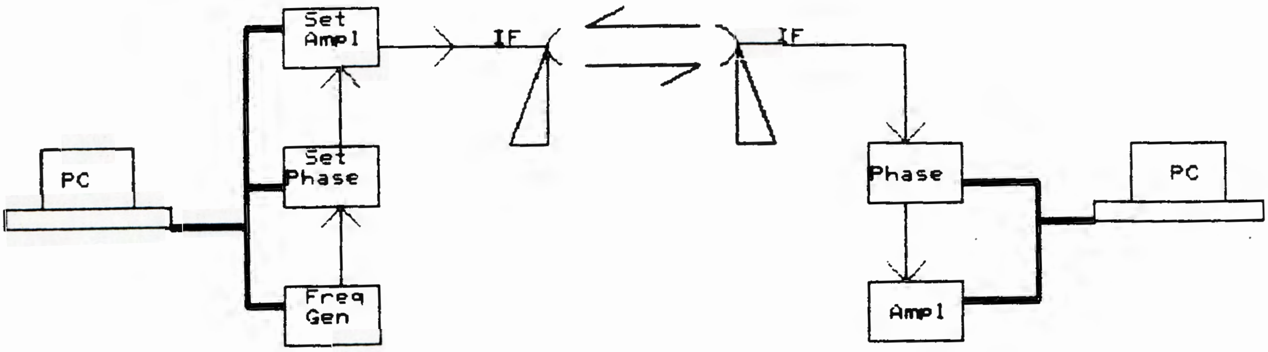
CHAPTER TWO

OVERVIEW OF THE PROPOSED SYSTEM

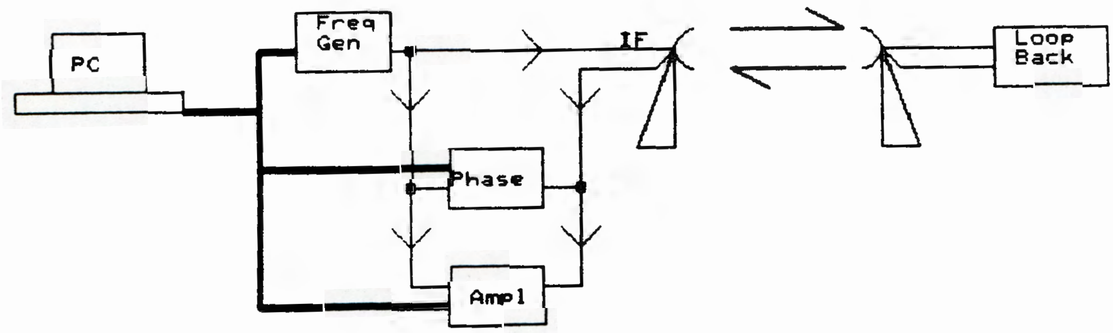
A microwave route consists of a number of hops, each with a transmitter and receiver. At each regenerator station, the signal is mixed down to IF after reception and then mixed back up to RF before re-transmission. The proposed instrument for measuring distortion on the link is inserted at the IF stage and all measurements based at IF.

2.1 END-TO END AND LOOP-BACK MEASUREMENTS

The final product will need to make comparisons between measurements of phase and amplitude at both ends of a hop in a so called end-to-end measurement, in order to obtain the path characteristics. However, for development, a loop-back arrangement is used, where the signal is in effect simply returned from receiver to transmitter. This allows measurements and control at only one end of the link to be performed and only one set of apparatus to be used. This will however not give a true indication of the one way path characteristics, as an effective measurement of the combined forward and return paths is being made. The two systems are shown in Fig 2.1.



End-to-end Measurement



Loop-back Measurement

Figure 2.1 End-to-end and Loop-back Measurement.

The measuring equipment developed for a loop-back arrangement can be used, with some additions, in an end-to-end measurement system.

2.2 PRINCIPLES OF OPERATION

The basic concept of the system is for a PC controlled system to sweep across the IF frequency band in a number of steps.

At each frequency point, measurements between the transmitted and returned signals provides gain and group delay values.

2.2.1 Frequency Sweeping

The most widely used IF frequency band for digital radio is 70MHz ± 20MHz, although 140MHz ± 20MHz is also common for higher data rates. This system was developed for an IF frequency centred at 70MHz with bandwidth from 50MHz to 90MHz.

A possible extension of the project would be time domain analysis of the data obtained. With this in mind, it was decided to take 256 samples across the frequency band, to allow for operations such as a Fast Fourier Transform to be performed on the data. Taking a greater factor of two samples would be redundant, as the graphics screen on which the data is plotted cannot support the resolution.

It was envisaged that phase measurements to determine IF group delay would be performed at the IF frequency. This requires a highly stable, synthesized frequency source to ensure phase coherency for phase comparison. However, if each of the 256 frequencies in the frequency range were to be synthesized, the sweep times would not be fast enough to follow the fast moving fading events occurring in multipath fading. As mentioned before, sweep rates of the order of 10 per second are required.

In order to solve this problem, a means was proposed whereby frequencies may either be synthesized, or swept by a learnt sequence from the synthesized sweep; the latter being much faster. The initial sweep would be synthesized providing a learn sequence for subsequent sweeps. Gain measurements would be performed during fast sweeps and periodic synthesized sweeps performed for phase measurement. As matters transpired, a method of low frequency phase measurement was the synthesized sweep was only necessary to initialize the system and for subsequent recalibration. A simpler non-synthesized IF frequency set-up thus could have been used. However, the frequency synthesizer set-up was retained as it had already been developed and provided a convenient means of generating the IF frequencies.

2.2.2 Modules of the System

The proposed system to measure gain and group delay over a microwave link consists of the following modules:

- IF frequency synthesizer/generator
- Amplitude detector
- Phase comparator
- Software/hardware interface
- Software

These will be linked as illustrated in the block diagram for the loop-back system as shown in Fig. 2.2. The description of the implementation of each section will be described in detail in the next chapter.

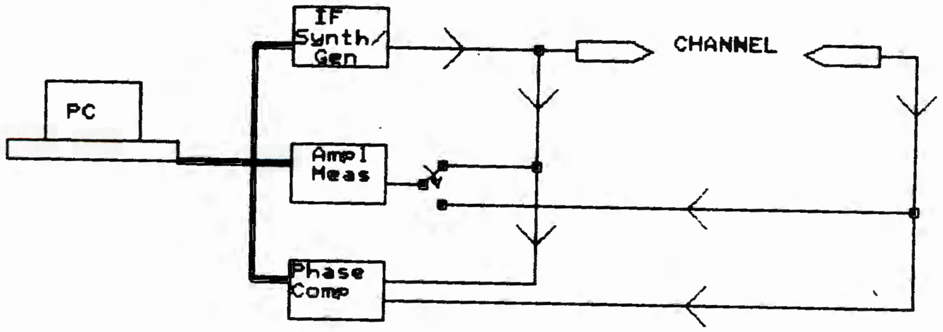


Figure 2.2 Block Diagram for Proposed Loop-back Measurement

CHAPTER THREE

IMPLEMENTATION OF THE SYSTEM

3.1 INTRODUCTION

The modules of the system were constructed individually and modifications made as time progressed to link them to one another. The IF sections of the hardware were constructed on RF prototype board, which allows minimum lead length and the use of a ground plane. Other low frequency sections were designed on bread-board and subsequently transferred to printed circuit board. CMOS integrated circuitry is used in most cases, due to its low power consumption and wide supply voltage limits. In high speed applications (above 1MHz) TTL or high speed CMOS is used.

A power supply, capable of delivering one amp, was constructed to supply the circuitry. Regulated ±12 volts and ±5 volts are provided. The power supplies are carefully decoupled at regular points where they feed circuitry against high and low frequency noise.

Each section of the loop-back system will be described in detail with reference to their interaction with other sections. The proposed method to extend this to an end-to-end measurement system is given at the end of the chapter.

3.2 HARDWARE/SOFTWARE INTERFACES

The interfacing between the PC and the hardware takes two forms. Those for digital signals to and from digital hardware make use of 8255 parallel input/output ports and those for reading data from analogue circuitry make use of a plug-in PC-26 A/D acquisition card.

3.2.1 The 8255 Ports

An 8255 plug-in card, developed at UCT, was used. This contains two 8255 chips, each with three 8 bit ports, which may be separately addressed and configured as inputs or outputs by a control word in the software. Digital data can then be respectively read or written. In this case digital connections are made with an A/D, a D/A and a frequency loading interface. Each chip has a 26 pin output which is connected to the hardware via strip cable.

3.2.2 The PC-26 A/D Acquisition Card

The PC-26 plug-in analogue to digital acquisition card has a resolution of 12 bits and has 16 multiplexed input channels. The sampling frequency may be set by software or by the onboard timer, the latter allowing faster, more accurate sampling. The total conversion time is 40µs, placing an upper limit of 25kHz on the sampling frequency. Various monopolar and bipolar voltage ranges may be selected via jumpers on the card [3.1].

The card has its own addressable 8255 ports. Port A reads the eight least significant bits of the 12 bit digital conversion and the first four bits of port B read the four most significant bits. Port C is used for channel selection and the type of sampling control. A sequence for an A/D conversion, with software timing, consists of raising bit C0, waiting at least 40µs until the end of conversion and then reading the A/D value from ports A and B. The resultant digital value, in the range 0 - 4095, is found by adding port A to the masked and shifted first four bits of port`B.

In this case, as the exact sampling frequency is not critical, the sampling frequency is set by a delay in the software of close to the 40µs limit. The monopolar 0 - 10 volt range is used. The card had to be calibrated for zero and full scale by trimming the relative potentiometers. Two of the channels are used - one for amplitude measurement and one for phase measurement.

3.2.3 Anti-Aliasing Filter

It was initially considered necessary to limit the maximum frequency of the signal to half the sampling frequency of the A/D card according to Nyquist's criterion, to avoid aliasing. For this purpose a sixth order elliptical low pass filter was constructed using two MF10 switched capacitor filters. The filter has a steep 60dB roll off between pass and stop bands.

Subsequently, however, it was discovered that such a filter is not necessary in the present case. Experience in another project indicated that the filter caused unwanted ringing on rapidly changing signals and that without it, due to the non-periodicity of the signals, there were no notable effects of aliasing. Therefore the filter was discarded and a simple RC filter used instead, with 3dB point set at half the sampling frequency. For completeness the design of the sixth order filter is given in Appendix A.

3.3 IF FREQUENCY GENERATION

A voltage controlled oscillator (VCO) is used to generate the IF frequencies. This can be controlled by a frequency synthesizer. As described in section 2.2.1, a system whereby the frequencies in a sweep may either be synthesized or swept by a learnt sequence is required. To achieve this, an initial synthesized sweep is made and the voltage required on the VCO for each frequency is read via an A/D and stored in a look-up table. On subsequent sweeps, these voltages are applied directly to the VCO via a D/A, in sequence, allowing a much faster sweep. Further synyhesized sweeps may be performed in order to recalibrate the system.

The initial design for the IF frequency generation was drawn up by Dr. R.M.Braun (project supervisor). The design consists of the frequency synthesizer, the frequency loading interface, the VCO and the A/D - D/A interface. The frequency synthesizer and VCO were developed with assistance from Mr. D.Gale, co-worker for the initial portion of the project.

3.3.1 The Frequency Synthesizer

A Philips SAA1057 frequency synthesizer chip was used because of its availability, inexpense and relative simplicity. This is linked to an external VCO and synthesizes frequencies from a stable crystal source in a phase locked loop method (Figure 3.3.1).

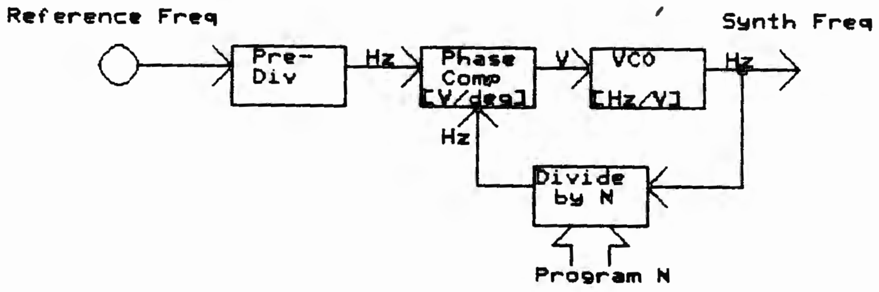


Figure 3.3.1 Phase Locked Loop Frequency Synthesis

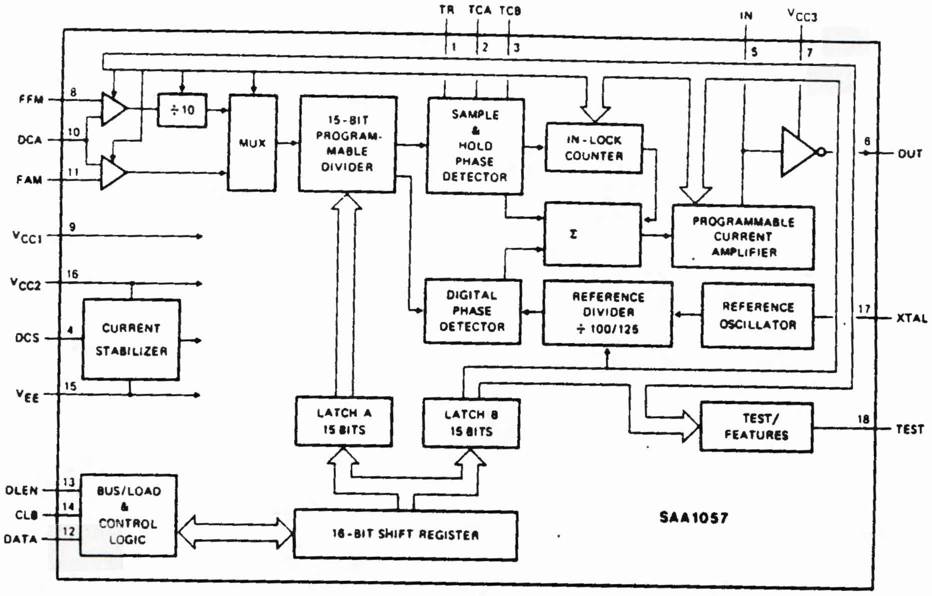


Figure 3.3.2 Block Diagram of SAA1057 Frequency Synthesizer [3.2]

Referring to the block diagram of the SAA1057 in Figure 3.3.2, the VCO is connected between pin 6(out) and the FM input to the synthesizer - pin 8(FFM). The frequency generated by the VCO is divided by a programmable divider and compared to the reference frequency of the crystal (connected to pin 17(xtal)), using a digital phase detector. The output of the phase detector is summed with a sampled and held measure of the phase of the divided signal. This is used to drive a current amplifier, the output of which is filtered and fed as the control voltage to the external VCO. The purpose of the sample and hold detector is to allow the synthesizer to lock onto the programmed frequency with improved spectral purity. An attenuated version of the control voltage is applied to the feedback pin 5.

The chip requires data in a serial form. This is received and timed by the inputs pin 12(data), pin 13(data length) and pin

14 (clock). The input from the VCO is received via pin 8, the FM input, as the subsequent division by ten allows the IF frequency range of 50 - 90MHz to be synthesized. Two power supplies are required - 5 volts for VCC1 and VCC2 and 12 volts for VCC3. The RC values for the external portion of the sample and hold circuit were taken from the application notes [3.3, 3.4].

The reference frequency is supplied by a 5MHz temperature controlled crystal oscillator (TCXO) with square wave output, the accuracy of which can be guaranteed to be ±1 ppm for a supply voltage of 9 - 12 volts. Tests revealed that the TCXO could be trimmed to 5 000 000 Hz ± 0.2Hz. The spectrum of the clock signal is given in Figure 3.3.3.

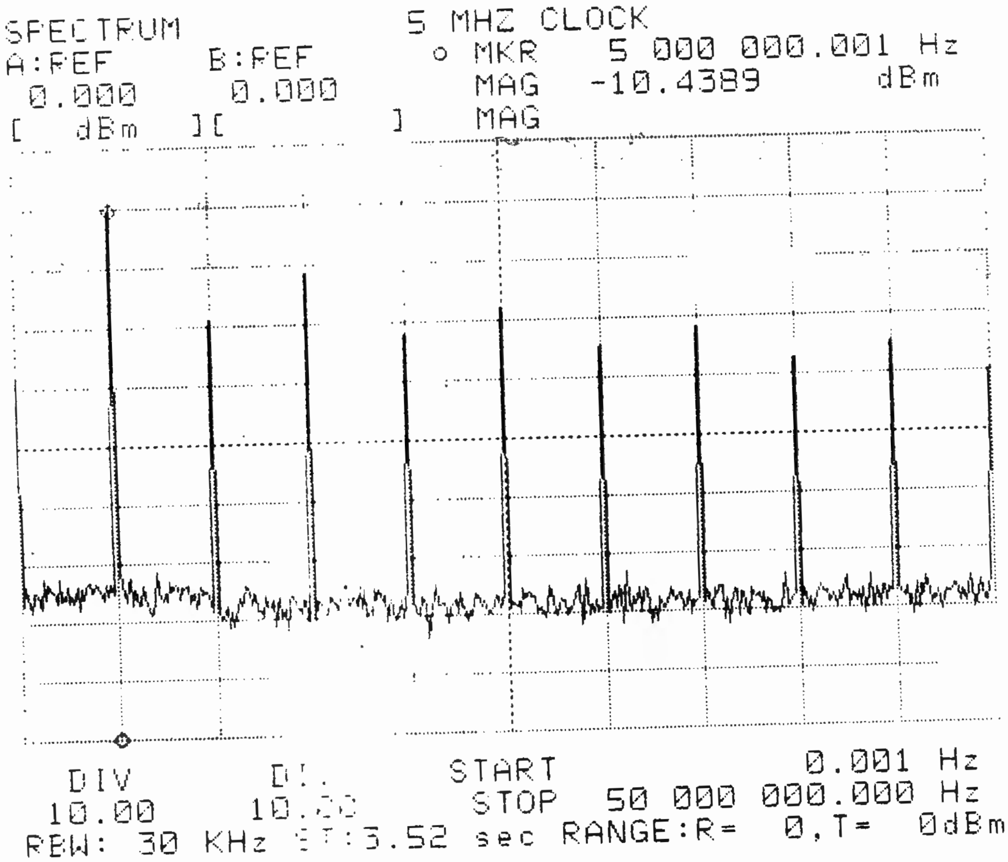


Figure 3.3.3 Spectrum of 5MHz Clock

The frequency synthesizer and TCXO circuitry is included in Figure 3.3.4 along with the VCO circuitry.

3.3.2 The Voltage Controlled Oscillator (VCO)

It was initially intended to develop a varactor tuned, discrete element, transistor oscillator with frequency doublers to step up the frequency from 35MHz to 70MHz and then 140MHz ranges (the two IF frequencies for DMR). This idea was abandoned in favour of a Plessey SP1648 varactor tuned VCO IC. This proved to be simple and reliable in the 50 - 90 MHz range.

The SP1648 is tuned by an external LC tank circuit. Details are given in the data sheet in Appendix F. The inductor is a wire wound toroidal RF ferrite core with an approximate value of 0.1µH. Some trial and error was used in obtaining the number of turns for the correct frequency range. The variable capacitance is realised with a MV1404 varactor diode whose capacitance changes with voltage applied. The MV1404 has a capacitor ratio of 10, enabling it to cover the 50 - 90 MHz frequency range. A radio frequency choke and capacitor isolate the rest of the circuitry connected to the varactor from the high frequencies generated by the VCO. The circuit is included in Figure 3.3.4. Table 3.3.1 shows the generated frequency against voltage applied to the varactor from tests conducted.

Table 3.1 Varactor Voltage vs Generated Frequency [3.5]

Varactor Voltage [volts]	Generated Frequency [MHz]
0.0	0.0
4.3	43.1
4.7	45.0
5.5	50.0
6.1	55.0
6.6	60.0
7.0	65.0
7.3	70.0
7.6	75.0
8.0	80.0
8.4	85.0
8.8	90.0
9.6	100.0
10.5	115.0

As can be seen from the table, the lowest frequency that can be generated is approximately 43MHz, which requires a voltage of 4.3 volts. Below this voltage no signal is produced. In order for the SAA1057 to have a signal at its VCO input to begin the synthesis operation, some form of "start up" circuitry is required. The output of the SAA1057 is thus fed into an inverting summer operational amplifier (IC U4A of Figure 3.3.4) and summed with a voltage that can be set by a trim potentiometer. The summed voltage is re-inverted before driving the varactor of the SP1648. The voltage from the trimpot is chosen such that, at power up, with zero voltage from the SAA1057, a frequency of a few megahertz below 50MHz is generated by the VCO. A voltage of 5 volts, giving a frequency of 47MHz was found to be adequate.

The circuitry of the VCO is included in Figure 3.3.4. The spectrum of a 70MHz synthesized signal from the VCO is shown in Figure 3.3.5. This shows a typical synthesized characteristic.

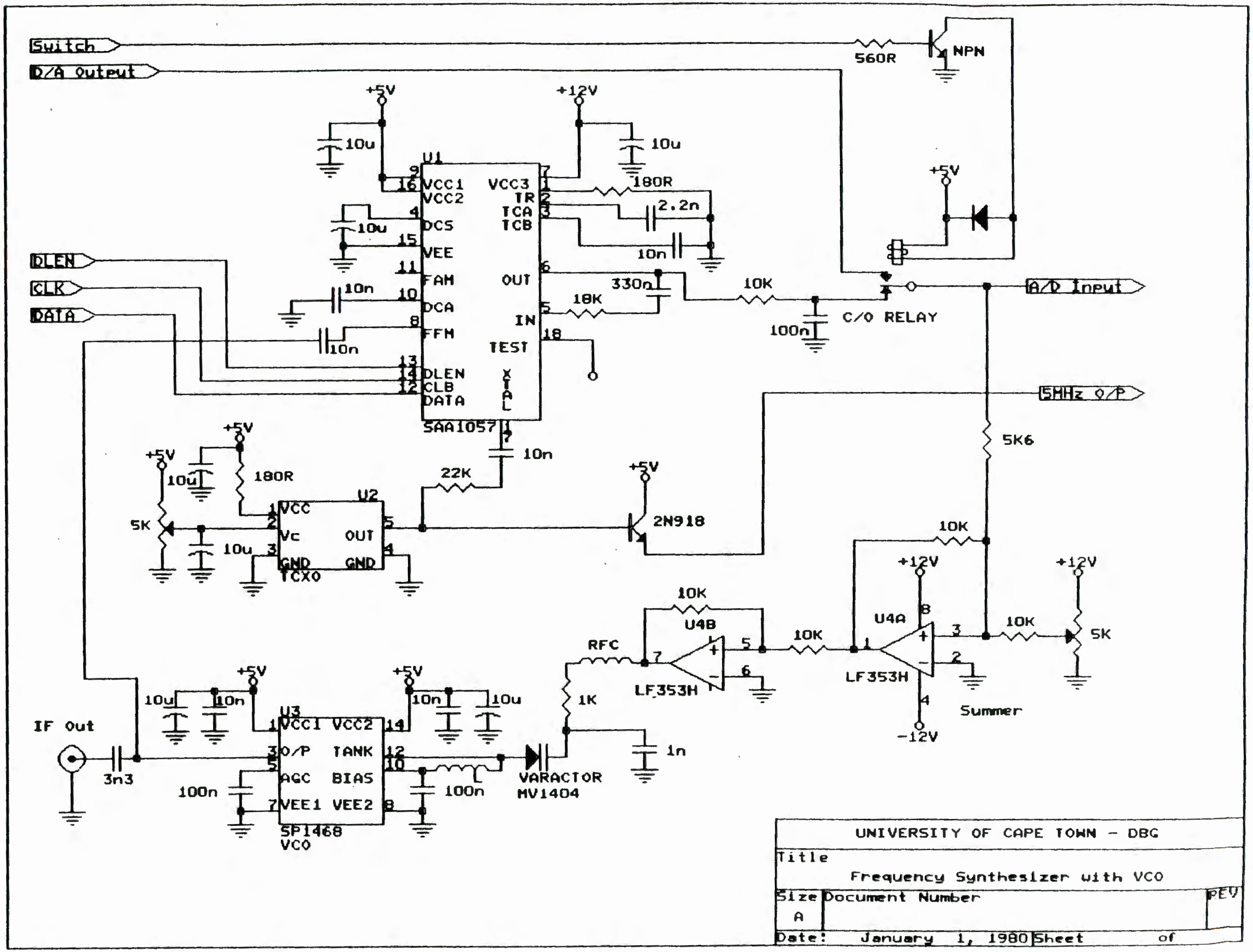
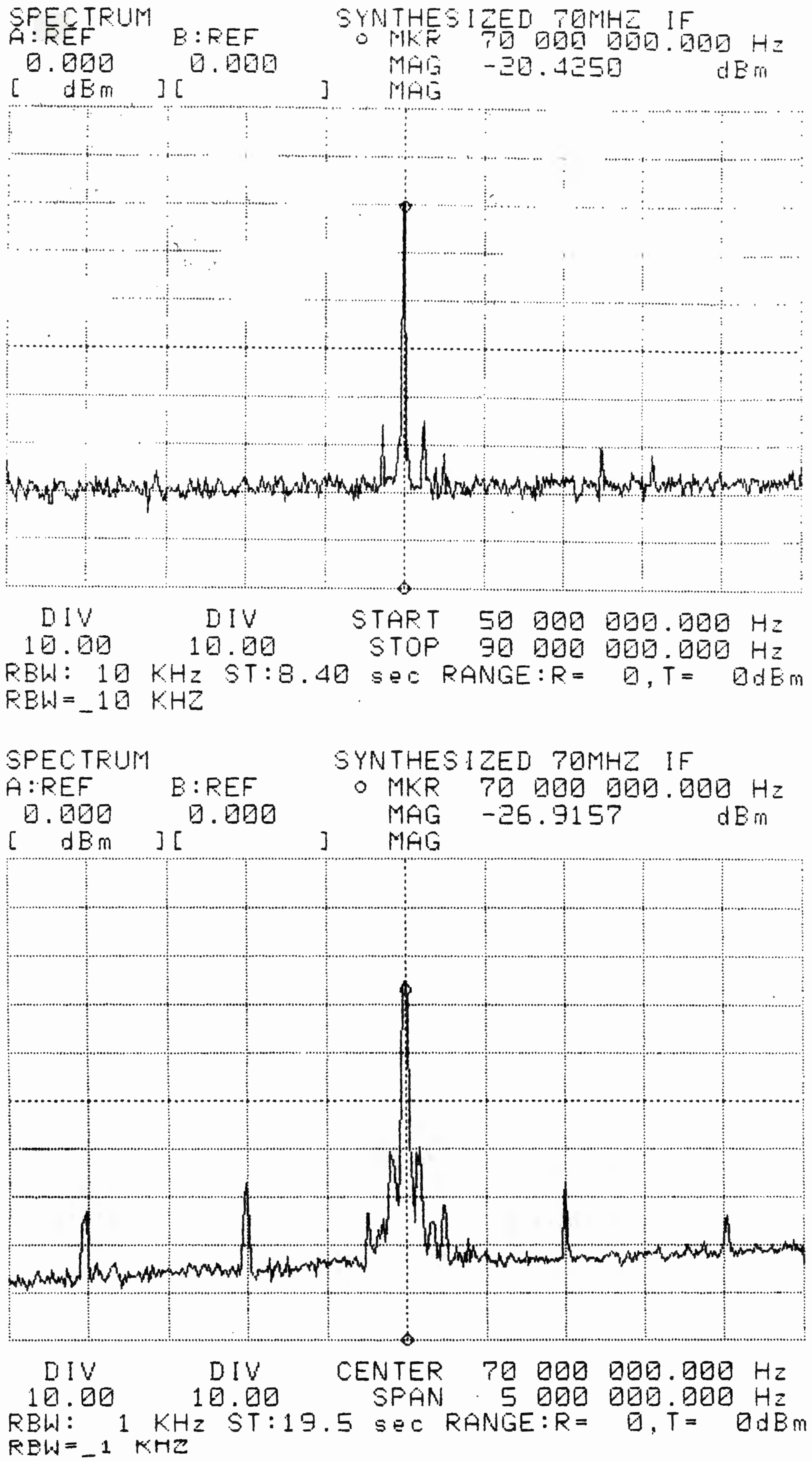


Figure 3.3.4 The Frequency Synthesizer and VCO



SPECTRUM SYNTHESIZED 70MHZ IF
A:REF B:REF ○ MKR 70 000 000.000 Hz
0.000 0.000 MAG -20.4250 dBm
[dBm][ ] MAG

DIV DIV START 50 000 000.000 Hz
10.00 10.00 STOP 90 000 000.000 Hz
RBW: 10 KHz ST:8.40 sec RANGE:R= 0,T= 0dBm
RBW=_10 KHZ

SPECTRUM SYNTHESIZED 70MHZ IF
A:REF B:REF ○ MKR 70 000 000.000 Hz
0.000 0.000 MAG -26.9157 dBm
[dBm][ ] MAG

DIV DIV CENTER 70 000 000.000 Hz
10.00 10.00 SPAN 5 000 000.000 Hz
RBW: 1 KHz ST:19.5 sec RANGE:R= 0,T= 0dBm
RBW=_1 KHZ

Figure 3.3.5 Spectra of Synthesized 70MHz Signal

3.3.3 Frequency Loading Interface

The SAA1057 requires data in a serial form, with acompanying clock signal and length of data signal. The frequency loading interface converts the two 8 bit words from the PC into a 16 bit serial form (DATA), generates the clock (CLB) to synchronize the data transfer, and the data length signal (DLEN). A strict timing relationship between the clock signal, the data and the positioning of the DLEN signal has to be adhered to. This is explained more fully in the data sheets in Appendix F. The operation is explained referring to the circuit diagram in Figure 3.3.6 and the timing diagram shown in Figure 3.3.7.

Ports A and B of the first 8255 chip provide the two 8 bit digital words to the 74HC165 shift registers, which clock them out in a 16 bit serial fashion. The 5 least significant bits of port C are used to co-ordinate the transfer of the data. Bit C0 resets the central D-type flip-flop ensuring that the DLEN line (connected to the Q output) is initially low. Bit C1, active low, (shown as PULS1 on the timing diagram) resets the 555 timer which generates the clock signal. The frequency of the 555 clock is set to provide a period of close to the minimum of that required by the SAA1057 of 10μs. The clock must be reset as no transient is permitted during the setup time (see timing diagram in Appendix F).

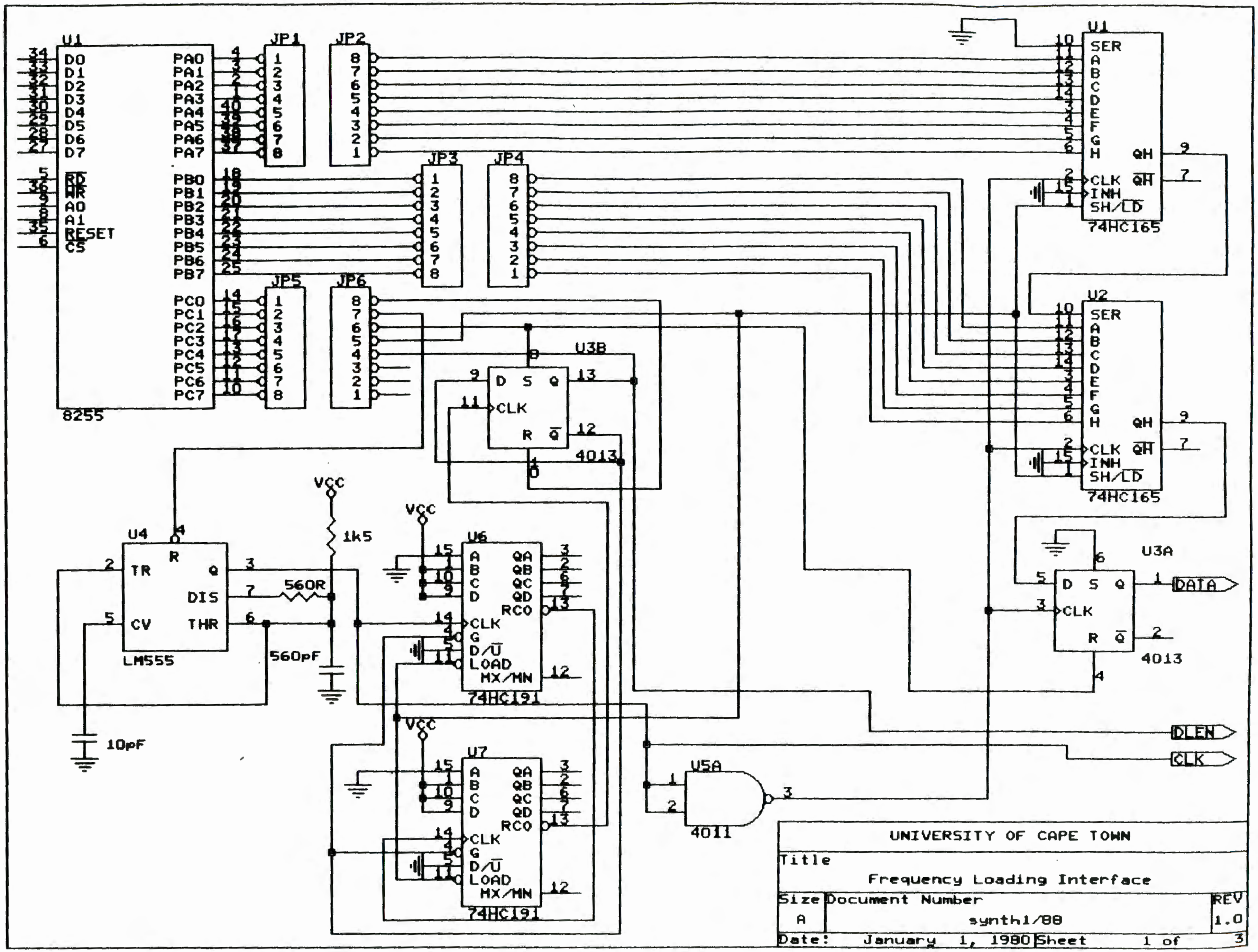
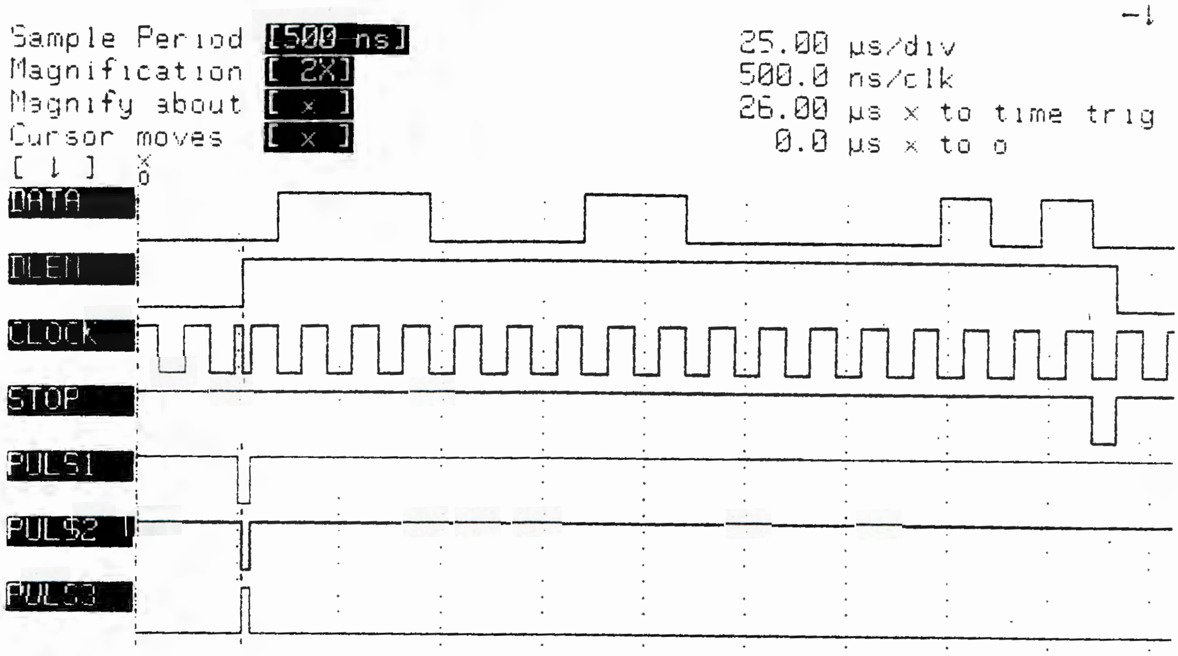


Figure 3.3.6 Frequency Loading Interface



Sample Period [500 ns]
Magnification [2X]
Magnify about [x]
Cursor moves [x]
[↓] $\overset{x}{o}$

25.00 µs/div
500.0 ns/clk
26.00 µs x to time trig
0.0 µs x to o

Figure 3.3.7 Timing Diagram for Data Transfer to SAA1057

Bit C2 (PULS 3 on the timing diagram) is active high and sets the central D-type flip-flop and resets the data output flip-flop. This raises the DLEN line indicating that data is about to be transferred. Bit C3, active low, (PULS 2 on the timing diagram) causes the shift registers to load data from ports A and B. On the next clock edge this data begins to be shifted through the registers. Bit C3 also causes the 74HC191 up/down counters to be loaded with the value of 15. On each subsequent clock, counter one counts up from 15. An overflow occurs at 17, which clocks the second counter to count up one from 15. The first counter resets to 0 and counts up to 17 again, clocking the second counter once more. This causes the second counter to overflow, which clocks the central D-type flip-flop, causing its output to toggle, thus lowering DLEN. This overflow clock signal is shown as STOP on the timing diagram. In this manner the overflow from the second counter occurs after 17 clock cycles and DLEN remains high for just over 17 clock cycles, encompassing the 16 bits of serial data and allowing a leading zero before the data, which is required by the SAA1057. The leading zero is produced automatically by virtue of the serial input of the first shift register being connected to ground. Note that DLEN is raised before the first leading edge of the clock.

Bit C4 is used as an input to monitor the DLEN line in order to determine when a 16 bit serial word has been passed. The clock signal is inverted to clock the shift registers to maintain synchronisity.

The software that runs the synthesizer thus sends the following data on lower port C:

Hex	Binary	Action
0B	1011	Reset f/f 1
08	1000	Reset 555
04	0100	Reset 555, set f/f 1, reset f/f 2, load counters, load shift registers
0A	1010	No action

3.3.4 SAA1057 Programming

The action of the SAA1057 is determined by the data passed to it from the PC in the form of 16 bit serial words. The word can be of two types: control or data. Both have a leading zero before the 16 bits. A control word is identified by a "1" following the leading zero. The control word is only used once to initiate the device, thereafter the frequency may be changed with the data word alone. The format of the data word and control word are given in Figure 3.3.8. The control word informs the SAA1057 as to the inputs being used, the reference division, the current amplifier gain, the phase detector and the test pin output. Amongst others, the test pin output can be programmed to indicate a lock condition.

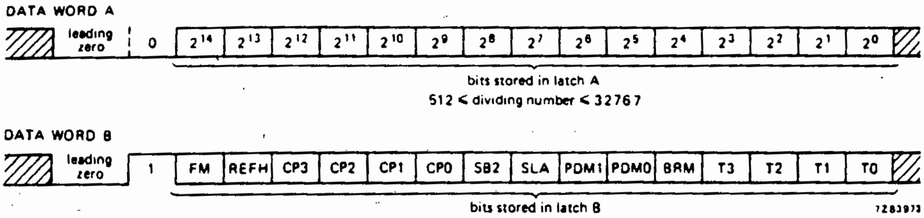


Figure 3.3.8 Control and Data Word Formats for SAA1057

The data word, to synthesize a specific frequency, is determined by:

for FM input

$$\text{step size} = \frac{\text{clock reference freq} * 10}{\text{reference division} * 32}$$

$$\text{data word} = \frac{\text{desired frequency}}{\text{step size}}$$

The reference division is the amount that the clock reference frequency is divided by. This can be set (in the control word) to either 100 or 125. In this case a reference division of 100 is used as it provides the simpler means to derive the required frequencies in the 256 steps between 50 and 90 MHz. More detail is provided in the data sheet of the SAA1057 in Appendix F.

The 8 most significant bits of the words are placed on port A and the 8 least significant bits on port B of the first 8255, which feeds the frequency loading interface. Thus, to synthesize 70MHz:

$$\text{step size} = \frac{5.10^6 * 10}{100 * 32}$$

$$= 15625$$

$$\text{data word} = \frac{70.10^6}{15625}$$

$$= 4480$$

$$= 1180 \text{ in Hexadecimal}$$

Thus 11 Hexadecimal is placed on port A and 80 Hexadecimal on port B.

3.3.5 The A/D and D/A

For the method of increasing the sweep rate, an A/D is used to monitor the voltages on the varactor of the VCO. These are stored in a look-up table and then used to drive the varactor of the VCO directly, via a D/A.

A 10 bit ADC1001 and 10 bit DAC1008 are used in order to obtain accurate voltage measurements. The circuits are shown in Figure 3.3.9. The D/A is operated in the voltage switching mode, in which the pin "Iout1" acts as a voltage reference while the pin "Vref" is the input. The voltage reference, which is required to be about 10 volts less than the supply voltage of 12 volts, is maintained constant at 2.2 volts by a green light emitting diode from the 5 volt supply. The 10 bit digital data is provided from port A and two bits of port C of the second 8255. The output is connected to a non-inverting amplifier (U3A), with variable gain supplied by a multi-turn potentiometer, to accurately amplify the output to the correct analogue level. The chip select input is controlled by a bit from port C, which is lowered to perform a D/A conversion, while the write and transfer pins are held low.

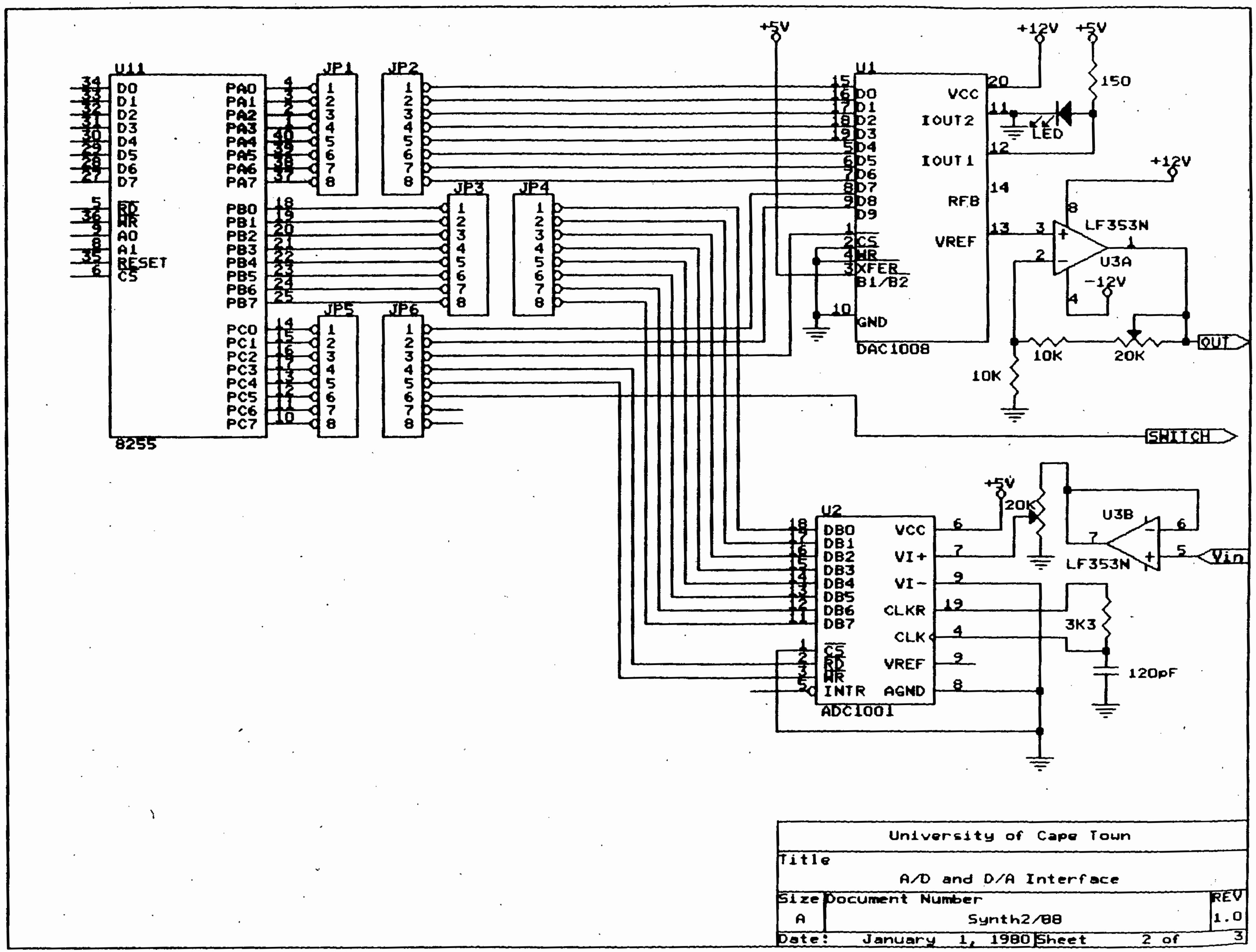


Figure 3.3.9 A/D and D/A Circuitry

The input to the ADC1001, VI+, is supplied from a variable voltage divider and buffered with a follower (U3B) to avoid loading the VCO. The voltage divider, consisting of a multi-turn potentiometer, can be adjusted to provide the correct input level - the maximum level being that of the reference voltage of 5 volts. The 10 bit data is read in two separate bytes - first the first 8 bits and then the last 2 bits - onto port B of the 8255. The read and write inputs are controlled by two bits of port C, while the chip select input is held low. The read and write inputs are lowered to initiate a conversion and the write input lowered in between the reading of the two bytes. The RC values for the clock control of the chip are chosen for the recommended clock frequency of 410kHz.

A test program to perform an A/D conversion on an analogue voltage, read the result and then output the digital result to the D/A and compare the voltages, was written and tested for a range of voltage levels. This was used to calibrate the A/D and D/A and check that the system was working correctly.

3.3.6 Switching of Voltage Source for VCO

The switching of the varactor of the VCO to receive its voltage level from the frequency synthesizer or the D/A is performed with a change-over reed relay, controlled by a bit of port C of the second 8255. A transistor follower arrangement is used to supply the current drive required for switching as shown in Figure 3.3.10.

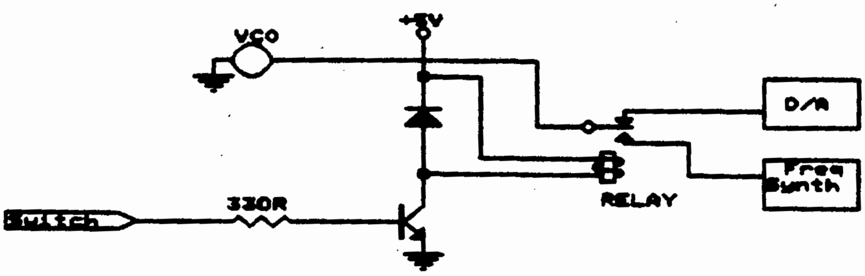


Figure 3.3.10 VCO Voltage Source Switching Mechanism

3.4 GROUP DELAY MEASUREMENT

3.4.1 Introduction

As group delay is defined as the derivative of phase difference across the channel with respect to frequency, the measurement involved is that of phase difference between transmitted and received signal, over the IF frequency band. These measurements can then be processed to provide a display of group delay.

It was initially envisaged that the phase measurements would be done directly at the IF frequency. A number of methods of doing this were proposed by Mr. D.Gale [3.6], using various modulation and mixing techniques. The most suitable was found to be the so called "nFr" scheme for an end-to-end measurement, where IF frequencies are synthesized and mixed at either end of a link. Owing to time constraints, none of these were implemented, but a simple amplitude modulation and mixing technique, proposed by Dr. R.Braun, was used, where phase measurements are done at low frequency.

In this technique, the swept IF frequency is amplitude modulated with a stable 1MHz signal. The return signal is demodulated and compared in phase, for each IF frequency, with the reference modulating signal. In order to simplify phase comparison, both the modulating and demodulated signals are mixed down to a low 24kHz signal. The phase comparator is required to measure 0 - 360 degrees unambiguously. The block diagram of the system is shown in Figure 3.4.1.

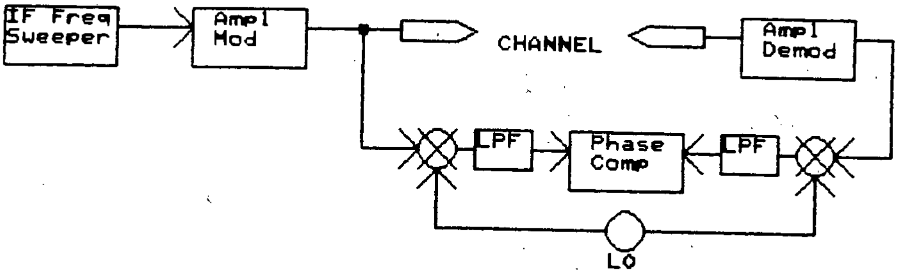


Figure 3.4.1 Phase Measurement System

Amplitude modulation was chosen instead of frequency modulation because of its relatively simple modulation and demodulation. Its disadvantage is in changing the amplitude of the signal that is being measured. To minimize this effect, as low as possible depth of modulation must be used.

3.4.2 Derivation of IF Group Delay from Phase Measurements

The measured phase difference, $\varnothing_m$, is for the 1MHz modulation. The actual phase difference of the IF signal, $\varnothing_a$, at each frequency, f, is given by:

$$\varnothing_a = \frac{\varnothing_m * f}{f_m} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.4.1)$$

where f_m is the modulating frequency (1MHz in this case). The group delay of the IF signal, τ_a, is defined as the differential of phase with respect to frequency:

$$\tau_a = \frac{d\varnothing_a}{df} \quad \text{[seconds]} \quad \ldots\ldots\ldots\ldots \quad (3.4.2)$$

$\varnothing_a$ in [fractions of a cycle]

From 3.4.1:

$$\tau_a = \frac{\varnothing_m}{f_m} \quad \text{[seconds]} \quad \ldots\ldots\ldots\ldots \quad (3.4.3)$$

$\varnothing_m$ in [fractions of a cycle]
f_m in [hertz]

Thus, THE IF GROUP DELAY IS DIRECTLY PROPORTIONAL TO THE MEASURED PHASE DIFFERENCE, being the phase difference, expressed in fractions of a cycle, divided by the modulating frequency in hertz.

3.4.3 Trade-off in Phase Measurement Techniques

The method of determining the group delay by measuring the phase difference of the modulation of the IF frequency has the advantage of the phase measured being a direct measurement of the group delay, as described above. However, there are various trade-offs to be considered.

The 1MHz modulation was chosen as a compromise between resolution of phase measurement, size compared to the IF bandwidth and ease of measurement. Greater resolution of IF phase measurement is obtained as the frequency of modulation increases, with maximum resolution when the measurement is actually done at IF. However, frequencies above 1MHz become increasingly difficult to work with. The lower the modulation frequency, the less resolution one can obtain in the measurement of phase difference for the swept IF signal. Conversely, the modulation frequency must be small compared to the IF bandwidth of 40MHz in order to obtain realistic results as the modulation frequency "scans" the bandwidth. With a 1MHz modulation, the "scan" width within the 40MHz bandwidth is 2MHz, which is acceptable.

The sweep time is found to be approximately 0.07 seconds (see section 4.1), thus there are approximately 70 000 cycles of 1MHz in each sweep. It is required to measure phase difference at 256 points across the frequency band, so this number of cycles is sufficient to produce accurate results.

From (3.4.3), with f_m = 1MHz, the maximum unambiguous group delay that can be measured is 1µs. A higher modulation frequency would lower this, but increase resolution, while reducing the scanning accuracy.

3.4.4 Amplitude Modulation

The 1MHz modulating signal is derived from the 5MHz TCXO used in the frequency synthesis. The output of the TCXO is current amplified with a transistor follower to increase its fanout. The 5MHz signal is divided by five with a 74LS90 IC to provide a stable 1MHz signal and then smoothed from its square form with an RC low pass stage.

A number of methods for amplitude modulating the IF signal with the relatively high 1MHz signal were proposed. This was complicated by the fact that a constantly varying IF signal has to be modulated. One such method involved modulation by the action of diodes on the signal as in Figure 3.4.2.

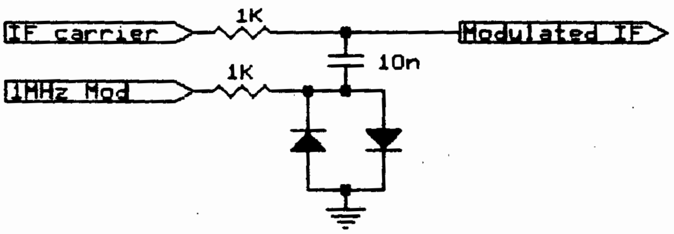


Figure 3.4.2 Amplitude Modulation with Diodes

In this simple method, the modulating signal turns the diodes on and off to varying degrees, resulting in a form of amplitude modulation of the carrier. This system was found to be unsuitable as it varied the DC level of the signal without producing true amplitude modulation. A method of modulation by varying the power supply on an MAR amplifier was also found to be unsuitable for the same reason.

The method finally employed involved the modulating signal varying the tail current of a differentially connected transistor pair. The circuit was constructed using a CA3086 general purpose transistor array IC. This chip has five general purpose silicon n-p-n transistors on a common monolithic substrate, including two internally connected to form a differentially connected pair. The circuit employed is shown in Figure 3.4.3.

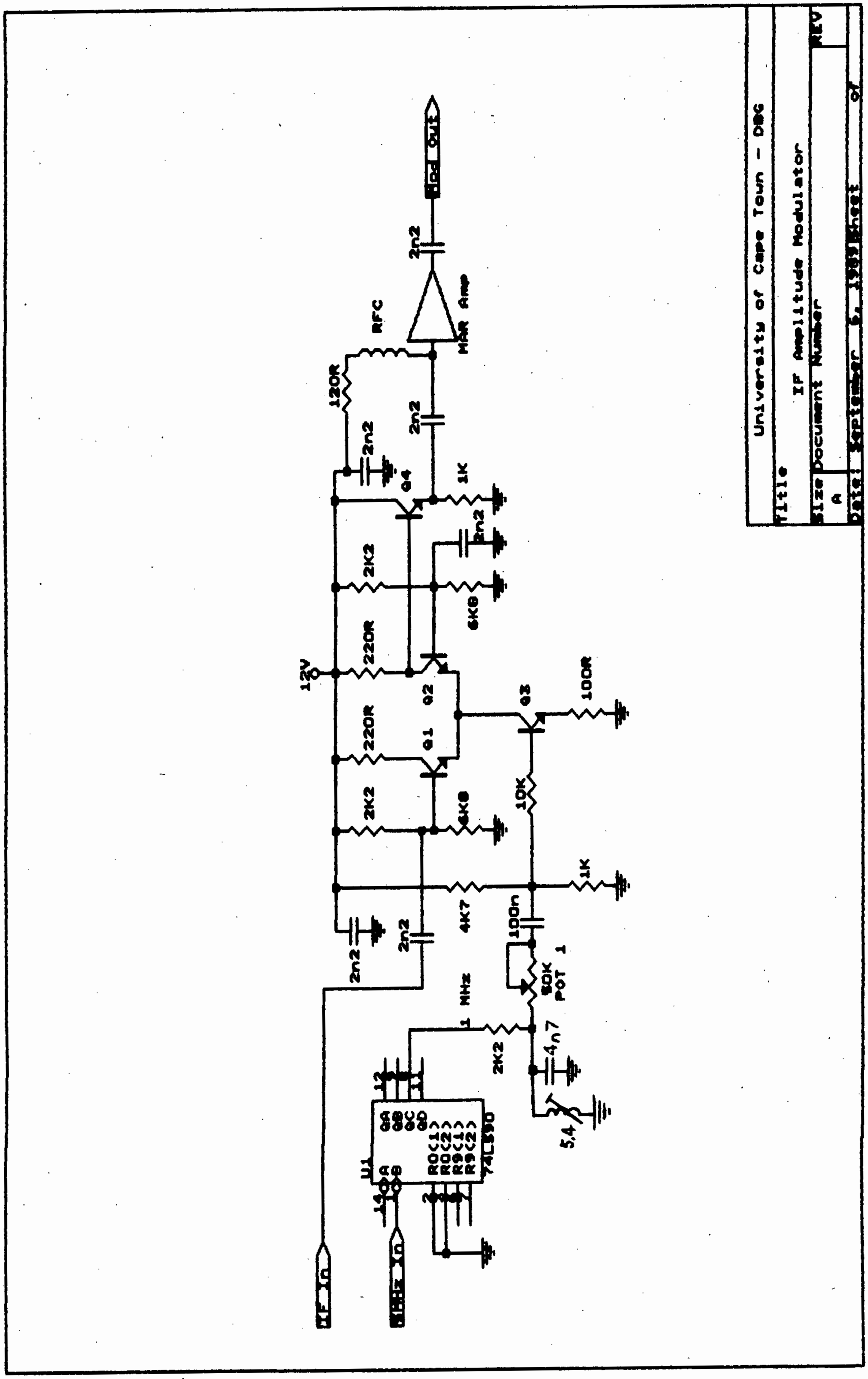


Figure 3.4.3 Amplitude Modulation using a Differentially Connected Pair

The bases of the differential transistors, Q1 and Q2, are biased at approximately 3 volts. The tail current is modulated by the modulating signal applied to the base of transistor Q3. Varying DC levels were applied to the base of Q3 and the resulting modulation observed, to determine the correct biasing for linear modulation. It was found that the transistor needed to be biased at approximately 2 volts. The input is AC coupled and all DC sections are decoupled.

The 1MHz square wave is applied to a high Q tuned circuit to convert it to a sinusoidal wave and this is used as the modulating waveform on the biased base of Q3, via a potentiometer to adjust the depth of modulation. The tuned circuit is used to prevent modulation with unwanted harmonics, specifically second harmonics, which introduce phase offsets after the subsequent demodulation. The modulated output is buffered with an MAR amplifier.

Figure 3.4.4 The 1MHZ Amplitude Modulated IF Signal
(Maximum Modulation)

3.4.5 Amplitude Demodulation

The amplitude measuring circuitry used for gain measurement (see section 3.5.1) cannot follow the relatively fast 1MHz modulation and is thus unsuitable for amplitude demodulation. Instead a simple diode envelope detector is used as shown in Figure 3.4.5.

This is preceded by an MAR amplifier and transistor cascode stage, to provide amplification to bring the signal above the diode voltage drop for as wide a dynamic range as possible. Schottky diodes with voltage drops of about 0.4 volts are used. The cascode arrangement cancels the Miller effect capacitance. A radio frequency choke is used as collector load to provide high impedance to the IF frequencies, resulting in high gain. Diodes D1 and D2 act as diode detectors, D2 providing a path for the negative signal. Diode D1 charges up the capacitor for the positive part of the signal and the RC time constant is set to allow following of the 1MHz modulation.

The output of the demodulator is filtered with an RC filter, with 3dB point set at 1MHz. This signal is then amplified and squared by means of the cascaded CMOS inverters. The first inverters, having negative feedback, operate in the linear condition and each stage amplifies by a factor of ten. The last two inverters are configured in a positive feedback arrangement and act as a Schmitt trigger. The resultant output is the demodulated 1MHz square wave.

3.4.6 The Mixing Process

The modulating and demodulated 1MHz square waves are mixed down to 24kHz for simple phase comparison. This is achieved by mixing with a 1.024 MHz local oscillator (LO) and filtering out the difference component. The use of a common local oscillator maintains the phase relationship of the two signals.

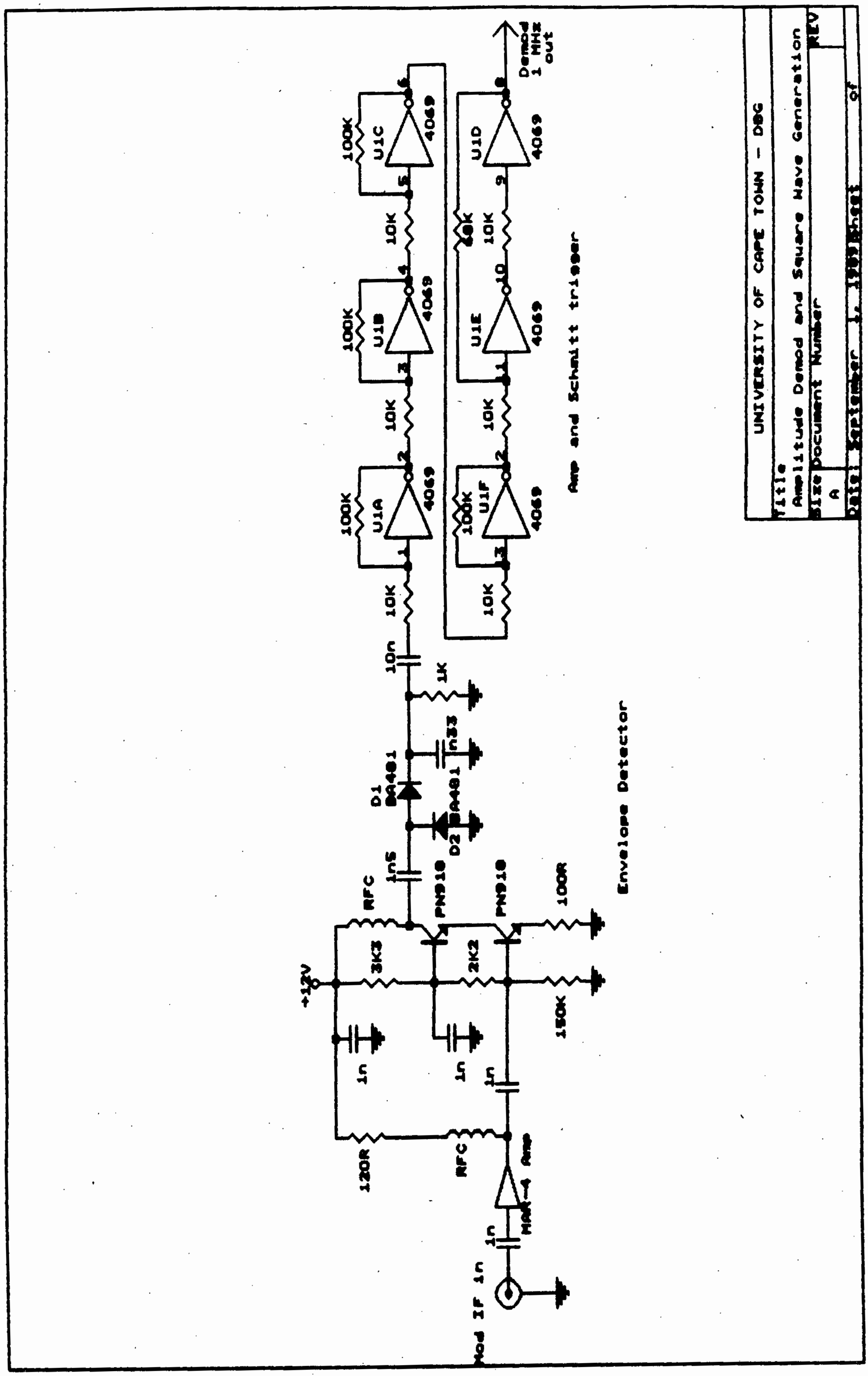


Figure 3.4.5 Amplitude Demodulation and Squaring

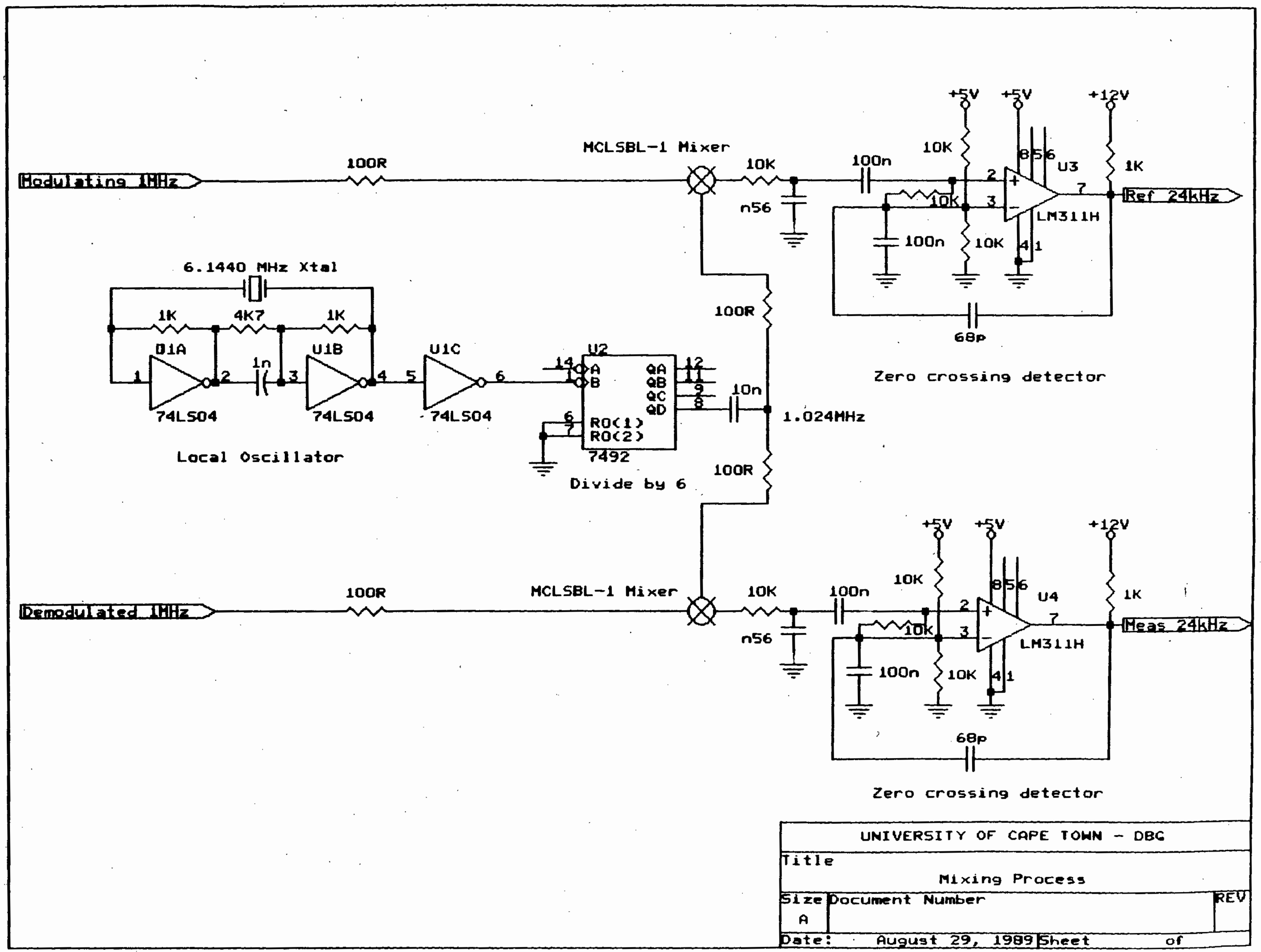


Figure 3.4.6 Mixing Circuitry

The 1.024 MHz LO is derived from a readily available 6.1440 MHz crystal oscillator divided by six. The 6.1440 MHz oscillator was constructed with a crystal with feedback around two TTL inverters as shown in Figure 3.4.6. This is divided by six with a 7492 IC.

For the mixing of the two 1MHz signals with the 1.024 MHz LO, two MCLSBL-1 double balanced mixers are used. These mixers require the so called RF and LO inputs to be no greater than 1dBm and 7dBm respectively. This is achieved by supplying these signals via 100Ω resistors. The 1Mhz square wave signals are taken via high Q tuned circuits to ensure that the RF inputs to the mixers are driven with a pure sinusoidal wave with no additional harmonics, which would cause excess mixing products. The resultant mixing process consists of the sum and difference frequencies at 2.024 MHz and 24 kHz respectively. In order to obtain only the desired difference component, an RC low pass filter, with 3dB point set at approximately 40kHz is used on each output. This is sufficient because of the wide range between sum and difference components.

The 24kHz output signals from the mixers are sinusoidal, approximately 100 millivolts peak to peak and with a 50 millivolt DC offset. These are squared with a form of zero crossing detector comparator as shown in Figure 3.4.6. The zero crossing detector consists of an LM311 comparator run off a single supply, with the inverting input biased at half supply. The input is AC coupled and applied to the non-inverting input as well as to the inverting input via a resistor and capacitor to ground. This results in the reference voltage of the comparator always being at the DC level of the signal as the AC portion at the inverting input is shorted to ground. Hysteresis is provided by positive feedback via a small (68pF) capacitor, which was found to eliminate multiple transitions and stabilize the system. It is imperative that the output of the comparator is clean, without multiple transitions, otherwise problems arise in the subsequent digital circuitry. The output pull-up resistor of the comparators is connected to the 12 volt supply to provide the correct level for the subsequent CMOS phase comparison circuitry.

3.4.7 Phase Comparison

An unambiguous 0 - 360 degrees phase comparison is required. Methods using an exclusive-or gate only provide 0 - 180 degrees phase comparison. The concept used in this circuit, proposed by Dr. R.Braun, is for the rising edge of the modulating or reference signal to set a flip-flop and the rising edge of the demodulated return or measured signal to reset the flip-flop. While set, the output of the flip-flop allows an integrator to charge up from a constant current source. The value reached is directly proportional to the phase difference. The charge can then be transferred and the integrator reset.

The circuit is shown in Figure 3.4.7 and the timing diagram in Figure 3.4.8. Both the measured signal and the reference signal are divided by two (M/2 and R/2) to provide signals with transitions at only the positive edge of the original signal. The reference signal is further divided by two to provide a divided by four version of the original (R/4). This is achieved with a 4520 dual binary counter. The positive going edge of R/4 clocks a D-type flip-flop, with D input connected high, thus setting it. In this manner a phase measurement is initiated for every four cycles of the reference signal. The M/2 signal is exclusively OR-ed with a delayed version of itself, to produce a spike for each positive transition of the original measured signal. The delay is achieved by feeding the M/2 signal through two EXOR gates with one input of each connected high, resulting in an inversion and re-inversion. This produces sufficient propagation delay to produce a spike that will reset the flip-flop. Thus the positive edge of the signal resets the flip-flop.

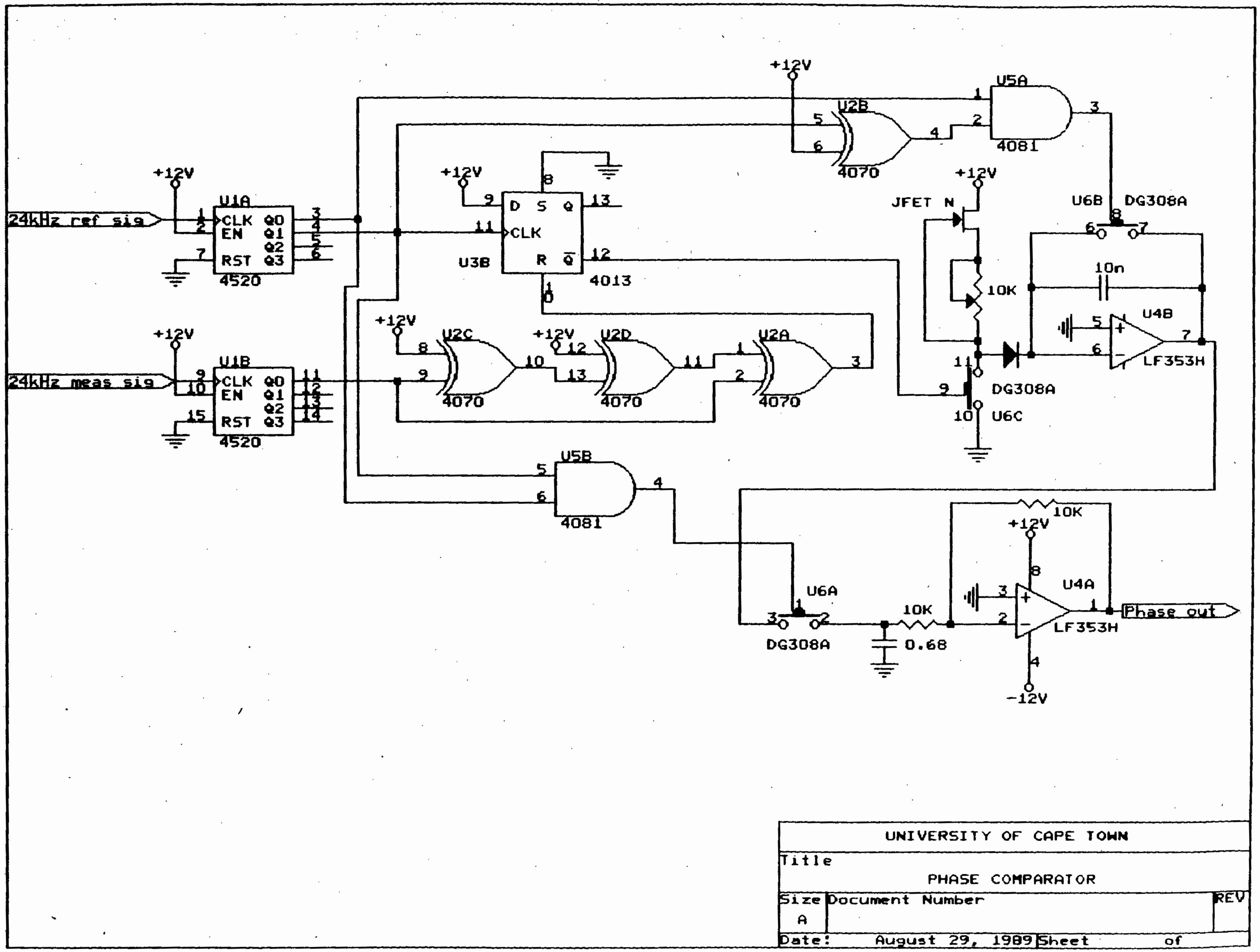
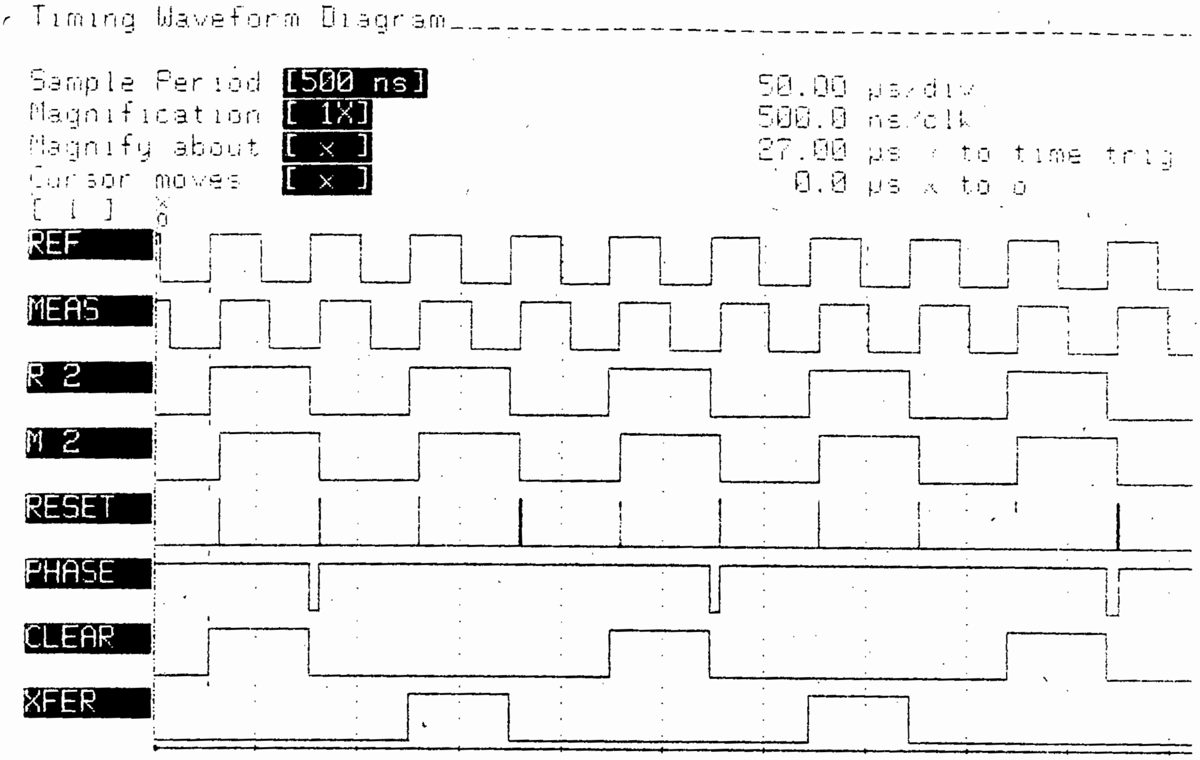


Figure 3.4.7 Phase Measurement Circuitry



Timing Waveform Diagram

Sample Period [500 ns]
Magnification [1X]
Magnify about [x]
Cursor moves [x]

50.00 µs/div
500.0 ns/clk
27.00 µs o to time trig
0.0 µs x to o

Figure 3.4.8 Phase Measurement Timing Diagram

While set, the flip-flop charges up an operational amplifier integrator (U4B) via a junction FET configured as a constant current source. The $\overline{Q}$ output of the flip-flop is used to control a DG308A normally closed analogue switch (U6C), so that when set, the switch is open, allowing the current source to charge up the integrator. When the flip-flop is reset, the switch is closed, so that current is shorted to earth, while the diode prevents the integrator from discharging. The potentiometer on the current source and the value of the integrating capacitor (10nF), are set for the integrator to charge to the correct maximum level (10 volts in this case for the A/D card).

After one cycle, corresponding to the maximum phase difference of 360 degrees, the charge of the integrator is transferred to a capacitor and then the integrator reset. This is achieved by closing analogue switches U6A and U6B respectively. The control of these operations is performed by

AND-ing R/2 and R/4 or its inverse as shown in the timing diagram of Figure 3.4.9.

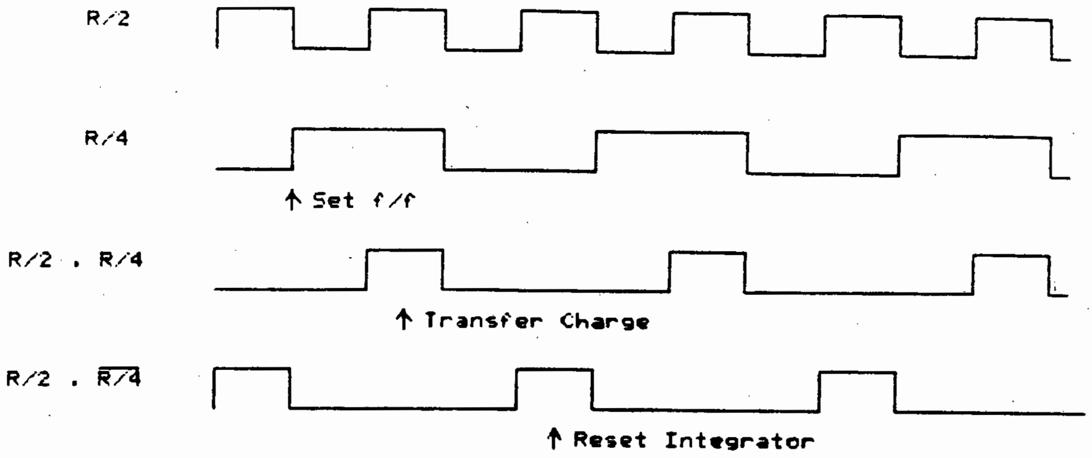


Figure 3.4.9 Timing of Charge Transfer and Integrator Reset Controls

The value of the capacitor to which charge is transferred was chosen such that the RC time constant formed by it and the analogue switch (on resistance ≈ 100Ω) is approximately a third of the time between samples (found to be 260μs). A 0.68μF capacitor is used. This RC arrangement also has the effect of acting as an anti-aliasing filter for the A/D acquisition card as described in section 3.2.3.

As the integrator integrates negatively, the transferred voltage is re-inverted and buffered with a unity gain inverting amplifier (U4A). The output is read by the second channel of the PC-26 A/D card. The inputs to the circuit may be reversed in order to obtain the correct lag/lead phase relationship between the reference and measured signals, as phase reversal can occur through the mixing process.

A variable 0 - 360 degree phase shifter was constructed to test the circuitry. The details of this circuit are given in Appendix B.

3.4.8 Anti-coincidence Circuitry

If the measured and reference signals are nearly in phase with one another, the phase reading shifts between 0 and 360 degrees, giving false, rapid transitions. Signals within 15% phase of each other are found to be problematic [3.12]. In order to avoid this, "anti-coincidence" circuitry is added prior to the phase measurement circuitry [3.13]. This is shown in Figure 3.4.10.

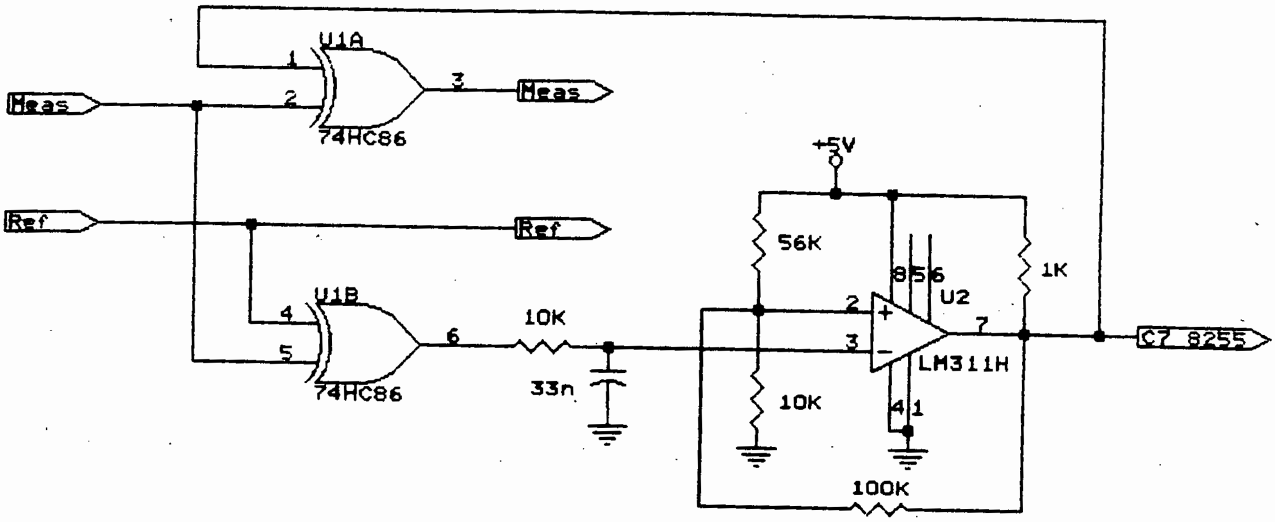


Figure 3.4.10 Anti-coincidence Circuitry

The reference and measured signals are applied to an EX-OR gate (IC 1B), which produces an ouput waveform with maximum mark-space ratio for 180 degrees phase difference and minimum for 0 and 360 degrees phase difference. The mark-space ratio is converted to a proportional DC voltage by an RC stage. This is fed to a comparator (IC 2) such that, if the signals are within 15% of one another in phase the comparator is set (high). The output of the comparator is fed back to EX-OR gate, IC 1A, which acts as a programmable inverter, shifting the phase of the measured signal by 180 degrees if the comparator is set. This ensures that no spurious phase measurements can occur. In this condition the phase measurement is 180 degrees out from the true value. The comparator output is used, via a bit of the first 8255 port to indicate the condition and the opposite correction made in the software.

3.5 GAIN MEASUREMENT

The principle of gain measurement is to compare the amplitudes of the outgoing signal to the return signal, over the IF frequency band. To achieve this, the amplitude measuring circuitry is connected to the outgoing signal during the initial synthesized sweep. The amplitude, for each of the 256 frequencies, is stored in a look-up table. On subsequent, unsynthesized sweeps, the amplitude measuring circuitry is connected to the return signal and the gain determined by comparison, in software, of the measured amplitudes with those in the look-up table. The amplitude measuring circuitry has to be capable of covering a wide dynamic range of greater than 60dB to follow the deep fades expected during multipath fading.

3.5.1 Amplitude Measuring Circuitry

A method of measuring amplitude with a simple diode envelope detector preceded by a transistor cascode amplifier stage identical to that used for amplitude demodulation in the phase measurement process (section 3.4.3) was tested. This worked well for signal levels above -30dBm, but signals below this were not detected as they were not sufficiently amplified to exceed the diode voltage drop (despite the use of Schottky diodes). Signals above 0dBm saturated, so a dynamic range of only 30dB could be covered, making the system unsuitable. A graph of voltage out against input level for the envelope detector is given in Figure 3.5.1.

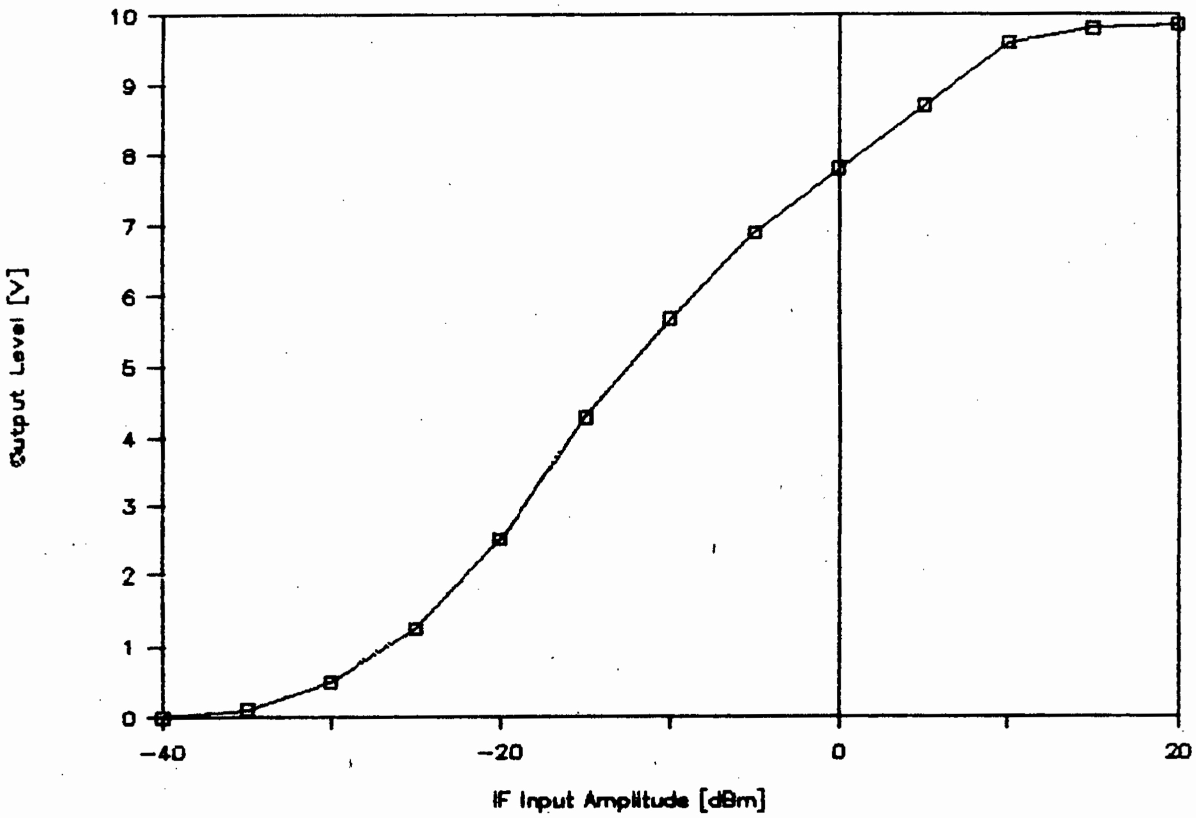


Figure 3.5.1 Envelope Detector Amplitude Response

The method implemented to cover the wide dynamic range, is to make use of logarithmic amplifiers in a successive detection system. Each logarithmic amplifier consists of a limiting amplifier with RF input and output and a detector with a so called video output, as illustrated in Figure 3.5.2.

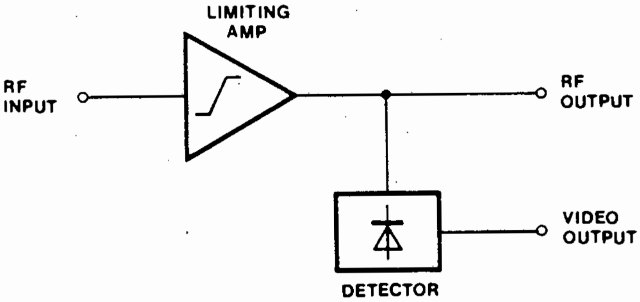


Figure 3.5.2 Basic Log State of a Logarithmic Amplifier [3.7]

A series of identical limiting amplifiers with logarithmic detectors are cascaded. The parallel sum of the detected outputs produce a composite logarithmic straight line function, thus covering a wide dynamic range. For a strip constructed by cascading individual logarithmic amplifiers, as in Figure 3.5.3, the first stage gives a video output identical to the single device (a logarithmic law over a limited input voltage range). The second stage receives the input signal, increased by the gain of the first stage. Over the range of the detector, this gain is constant, so when a logarithmic scale is used for the RF input, the second stage video output will be identical to that of the first stage, just displaced to the left by the stage gain. This is shown in Figure 3.5.3 for a three stage strip.

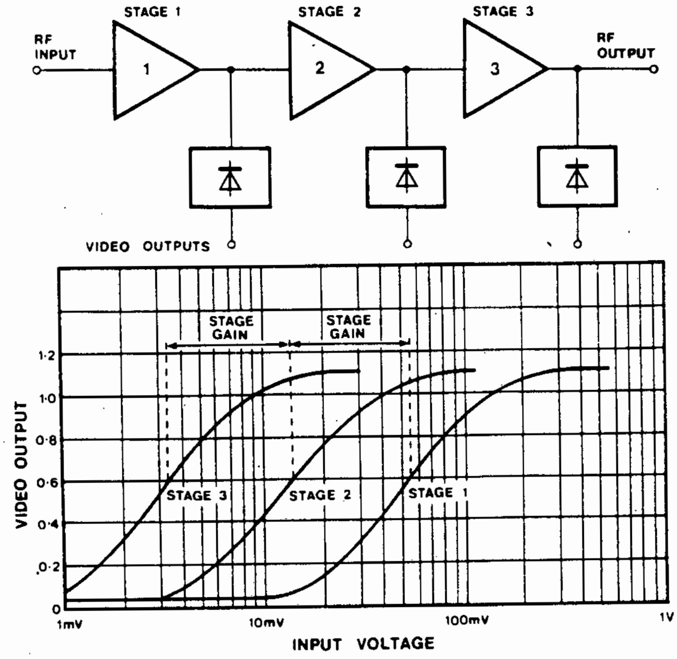


Figure 3.5.3 Video Outputs from 3 Stage Strip [3.8]

The video (detector) outputs from each stage are summed, producing a logarithmic response, as shown in Figure 3.5.4. For each increase in input level corresponding to the stage gain, a contribution equal to the maximum video output from a single stage is added to the summed video output. In this way a very accurate logarithmic law can be obtained.

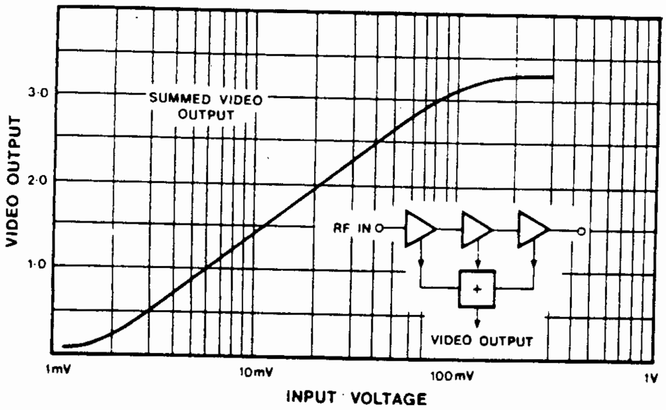


Figure 3.5.4 Output from Strip [3.9]

The dynamic range is extended by increasing the number of stages. The limit is reached when the last stage in the cascade reaches full video output solely on the noise produced from the first stage . The dynamic range can be further increased by attenuating the input signal and applying it to another short strip in parallel with the main strip. This so called lift stage continues to give an output change when the main strip has saturated. [3.10].

In this case, six logarithmic amplifiers are cascaded in the main strip using three Plessey SL523 dual logarithmic amplifier chips. A lift stage with two logarithmic amplifiers (one SL523) fed from a variable attenuator is used. The circuit is given in Figure 3.5.5. The video outputs are summed with a common base summing transistor and a 1kΩ resistor placed in series with each video output to avoid oscillations due to feedback on the video line [3.11]. The summed video output is fed into an inverting operational amplifier (U1) with potentiometers to set the gain and the DC level. This is necessary as the summed video output has a large negative DC offset and an inverted response and the output has to be set to the range 0 - 10 volts for the A/D acquisition card. The signal is buffered with a follower (U2) and read by the first channel of the A/D card. An RC low pass filter after the gain stage acts as the anti-aliasing filter for the A/D card as described in section 3.2.3.

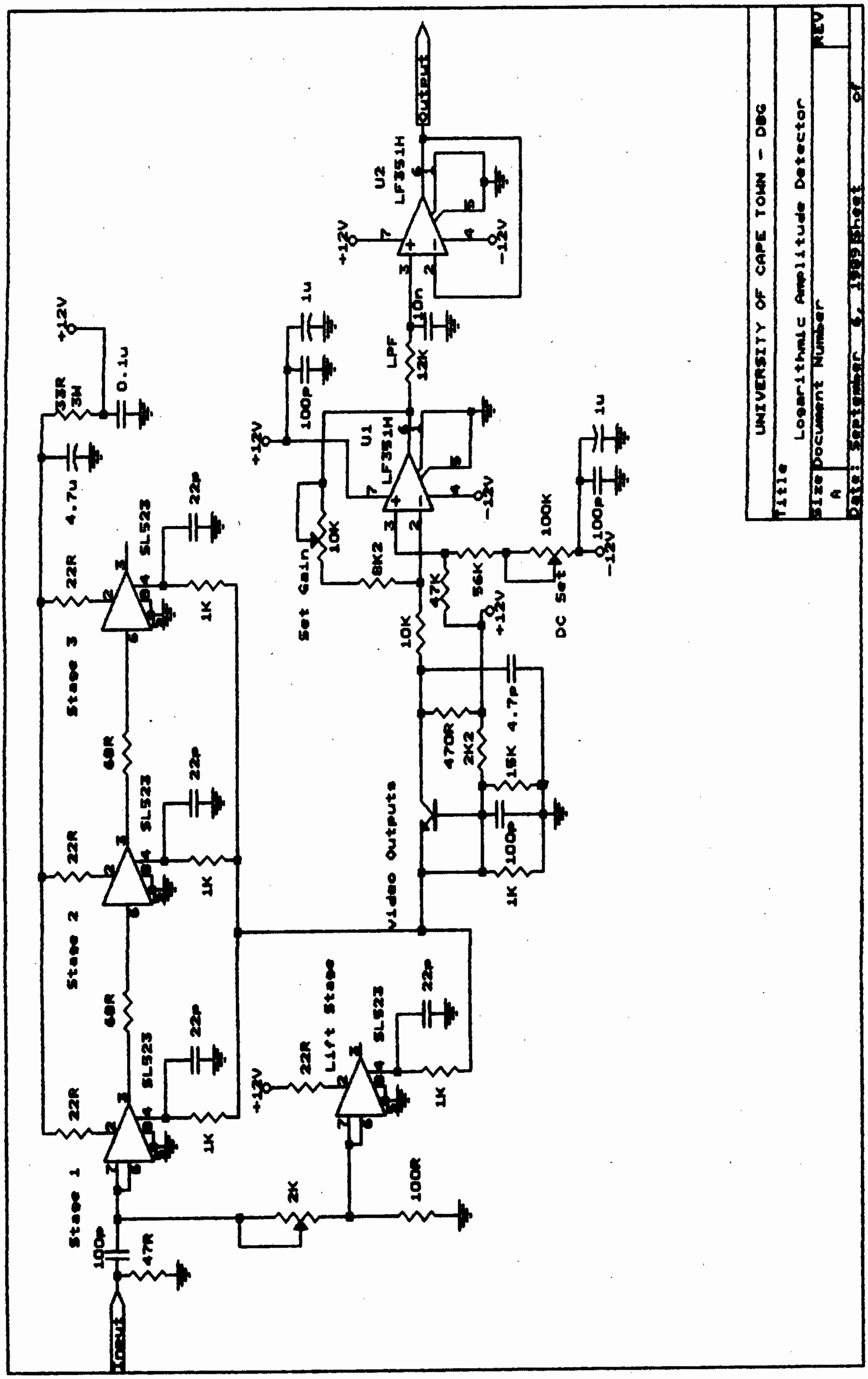


Figure 3.5.5 Logarithmic Amplitude Detector

The linear range of the logarithmic law detection response was found to be for signals of amplitude -5dBm to -70dBm, giving a dynamic range of 65dB.

3.5.2 Switching and Matching

The switching of the amplitude measuring circuitry between the outgoing and return signals is performed with a change-over reed relay, under control of a bit of port C of the second 8255, in the same manner as that described in section 3.3.6. A complication is the aspect of matching. The transmitter, with output impedance of 50Ω should see 50Ω terminations, whether the amplitude measuring circuitry is connected to the outgoing or return section. Improper matching causes standing waves to be formed over the channel, which affects the amplitude measurements. Differing matching, depending on the position of the amplitude measurement, will cause differing standing wave patterns, affecting gain measurement.

In order to obtain correct matching, a dummy 50Ω load is switched onto the end of the channel with a second relay, when the amplitude measurement is taking place on the outgoing signal. The output impedance of the modulated, swept IF signal is set to 50Ω. Its level also has to be decreased from that set by the MAR amplifier at the output of the modulator, to the correct level for the amplitude measuring circuitry of -5dBm (the top of the linear measurement range). This is done with a pi section resistor attenuation network, having 50Ω input and output impedance. The details of this design are given in Appendix C. The input impedance of the amplitude measuring circuitry is 50Ω. This switching and matching scheme is shown in Figure 3.5.6. The input impedance of the demodulator for the phase measurement process is also 50Ω in order to obtain a correct match.

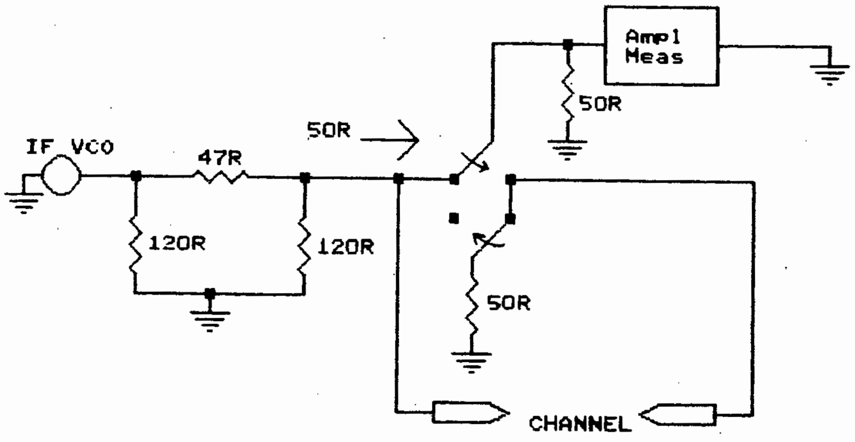


Figure 3.5.6 Matching and Switching Section for Amplitude Measurement

3.6 SOFTWARE

An IBM compatible AT PC with a 10MHz clock is used. This is sufficiently fast to produce the necessary sweep speeds and to display data in near real time. The software was written in Turbo Pascal version 4.0. This is a powerful, fast, user friendly language ideally suited to the task. Control of hardware can be performed by simple commands to input/output port addresses. Another major attraction of Turbo Pascall is the powerful graphics package that it supports. This is used as a versatile means of displaying data. The software may easily be adapted and/or extended to allow display and storage of data by other means. At present the data is always plotted, which is time consuming and an alternative would be to store the data or write it to a file. This is a simple process, but plotting the data is more instructive for development.

The separate areas of the software are the menus, the frequency synthesis, the A/D and D/A conversion, the reading of analogue data and the processing and display of data. A listing of the program is given in Appendix D and the flow-chart in Figure 3.6.1.

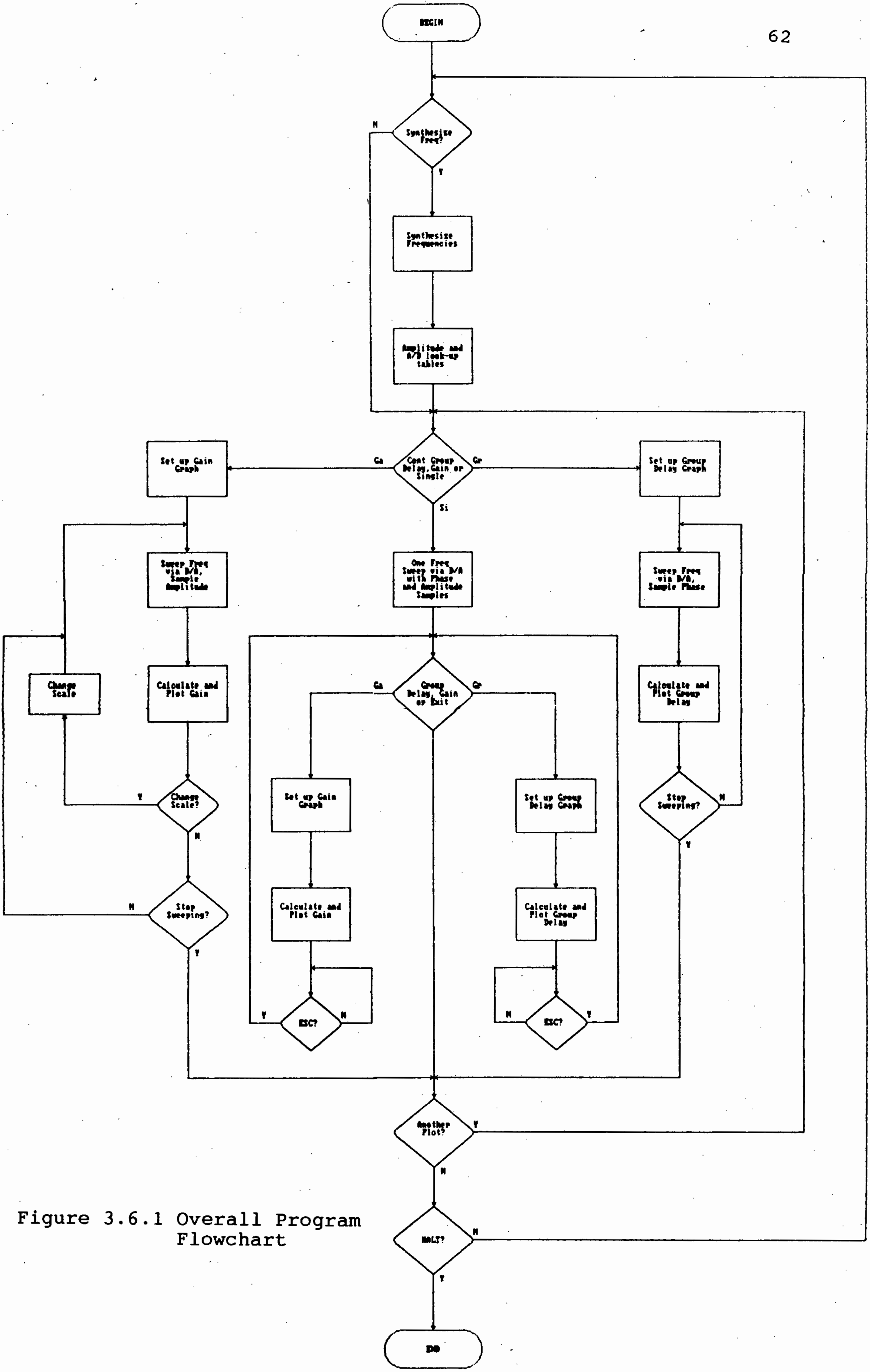


Figure 3.6.1 Overall Program Flowchart

3.6.1 Menus

The program is menu driven. On starting, the main program provides the user with the choice of initializing the system with a synthesized frequency sweep or entering unsynthesized sweeps directly. If initialization is chosen, procedure "freq_synth" is called. Once a synthesized sweep has been performed, procedure "menu" gives the user the choice of continuous group delay measurement, continuous gain measurement or a single sweep. If continuous gain is chosen, procedures "gain_parameters", "gain_graph" and "draw_gain" are called to display gain measurements continuously. The corresponding phase procedures are called if continuous group delay is chosen.

For the case of a single sweep option, procedure "single_sweep" performs a single sweep and measurement. Procedure "single_menu" then provides the user with the choice of plotting the gain or group delay information from the same single sweep. Depending on the option, procedures "single_gain" or "single_phase" are called.

Each menu and display may be exited with the escape key, returning the user to the previous menu and finally exiting the program. The user also has the choice of re-initializing the system with a synthesized frequency sweep.

3.6.2 Frequency Synthesis

Procedure "freq_synth" first calls procedure "initialize". This writes the control word for the SAA1057 frequency synthesizer chip to the frequency loading circuitry via ports A and B of the first 8255 chip. Bits of port C are used to control the timing of the circuitry, as described in section 3.3.3. The DLEN line is monitored by a bit of port C to determine when the control word has been sent.

Procedure "freq_synth" then sets the data word for the synthesizer to synthesize a frequency of 50MHz (the beginning of the IF frequency band). This is outputed on ports A and B, with the necessary control on bits of port C. The DLEN line is again monitored to determine when the data word has been sent. 256 frequencies, from 50 - 90 MHz, are thus generated in a loop, with a value corresponding to 1/256 of the 40MHz range being added to the data word each time. For each synthesis, an analogue to digital sample is taken of the amplitude of the outgoing signal via channel one of the PC-26 A/D card and stored in a look up table. This is performed in the same manner as that described in section 3.6.4. In addition, procedure "adc" is called each time to perform an A/D conversion to store the voltage on the varactor of the VCO. Finally, once 256 frequencies have been synthesized in the sweep, the two bits of port C of the second 8255 are set to switch the reed relays so that subsequent amplitude measurements are taken on the return signal, the voltage on the VCO varactor will come from the D/A converter and the dummy 50Ω load is switched out.

3.6.3 A/D and D/A Conversion

Procedure "adc" is called during frequency synthesis to perform an A/D conversion at each frequency. This is done by toggling the read and write inputs of the ADC1001 chip via two bits of port C of the second 8255. The 10 bit digital conversion is then read on port B in two stages: first the upper eight bits and then the lower two bits, with the read line lowered in between. The 8 bit and 2 bit results are shifted, masked and added to give an 8 bit lower byte and 2 bit upper byte and stored in look-up arrays "low_bits" and "high_bits" respectively.

Procedure "dac" is called during fast frequency sweeping to perform a D/A conversion of voltage to the VCO. The procedure is called with the frequency sample number as its argument and a D/A conversion performed of the corresponding bytes in the look-up tables "low_bits" and "high_bits". The lower byte is sent through port A and the upper 2 bit byte through the lower 2 bits of port C of the second 8255. A bit of upper port C toggles the chip select input of the DAC1008 to perform a conversion.

3.6.4 Reading of Analogue Data

Procedure "AD_sample" is called to obtain 256 samples of data via the PC-26 A/D card on either channel one (for amplitude) or channel two (for phase). for each pass through the loop, procedure "dac" is called to set the frequency. In this manner the frequency range is swept and measurements taken at each frequency point. The procedure is called with channel number as its argument in order to select the correct channel for amplitude or phase measurements. The channel is selected and the software clock cleared via port C of the card. To initiate a conversion the software clock bit is raised. The software then performs a delay loop for at least 40µs to allow time for the conversion. The delay time sets the sampling frequency, which in this case is set to be 60µs (determined by monitoring the end of conversion pin of the A/D with a logic analyzer).

The 12 bit result of the conversion is then read from ports A and B, giving a lower 8 bit byte and upper 4 bit byte. Subsequently, in the plotting procedures, the upper 4 bits are shifted, masked and added to the lower byte to provide a single value result.

In the case of the option for a single sweep, procedure "single_sample" is used. This performs a sweep and takes a sample from both channels consecutively for each frequency point, so that gain and group delay data may be plotted from the same sweep.

3.6.5 Processing and Display of Data

Separate procedures are used for the processing and display of gain and group delay data. Procedures "gain_parameters" and "phase_parameters" initialize the graphics mode and set the respective graph position, axes co-ordination and calculate the scale. Procedures "gain_graph" and "phase_graph" draw the respective outlines, graph axes and labels. They also save the drawn screen to a position in memory for subsequent refreshments of the screen.

Procedures "draw_gain" and "draw_phase" perform the display of gain and group delay data on a continuous basis. Procedure "AD_sample" is called to perform a sweep and provide data. The 12 bit sampled values have a value in the range 0 - 4095. The gain is calculated by subtracting from the measured amplitude value, the value of the outgoing amplitude stored in the look-up table, for each frequency. This multiplied by a factor gives the gain in dB's, as the amplitude is measured in a logarithmic fashion. The multiplication factor is chosen to provide the correct scaling for plotting, as described below.

If the true amplitude of the signal is x, then the amplitude measured in a logarithmic fashion, y, is

$$y = A\log_{10}x \quad \ldots\ldots\ldots\ldots\ldots \quad (3.6.1)$$

where A is a constant to be determined. The gain is to be measured in dB's as

$$G = 20\log_{10}\frac{x_1}{x_2} \quad \ldots\ldots\ldots\ldots\ldots \quad (3.6.2)$$

From 3.6.1, $x = 10^{y/A}$

Thus, $G = 20\log_{10}10^{y_1/A} - 20\log_{10}10^{y_2/A}$

$$= 20/A(y_1 - y_2) \quad \ldots\ldots\ldots\ldots \quad (3.6.3)$$

This has a maximum value of 4095. Thus, for a 65dB range

$$20/A * 4095 = 65$$

Thus, the factor $20/A = 0.0159$.

The default scale is 10dB per division, which may be changed.

As derived in section 3.4.2, the group delay in seconds is the measured phase difference divided by the modulating frequency of 1000 Hz. If the result is plotted in microseconds, then the group delay is the same as the measured phase difference in fractions of a cycle. The sampled value is divided by 4095 - its maximum value, which corresponds to 1μs of group delay, to obtain a value between 1 and 0. It was discovered that the circuitry caused a constant 0.2μs offset in the measurement of group delay and a negative response. To counteract this, the measured value is subtracted from 0.2 before plotting. Compensation is also provided for the measured value "looping around" in the range 0 - 1 μs, as well as detecting and compensating for inversions introduced by the ant-coincidence circuitry.

The first sweep is plotted, using lines to each calculated point, and thereafter subsequent sweeps plotted while erasing the line produced from the previous sweep. This is done by setting the colour to blank, redrawing the old line segment, resetting the colour on and drawing the new line segment from the previous point to the new point, for each sample in the sweep. The data is continuously plotted, with the program checking for key presses at the end of each sweep. After every 10 sweeps the background is refreshed from that stored in memory. An escape key will exit the plotting and, in the case of gain display, a space key will allow the user to change the scale. This causes procedure "gain_scale" to be called in which the scale in dB per division may be entered. By using a compiler directive to switch off the error checking, only the correct format of entry is accepted. The procedure changes the scaling factors to reset the new scale.

For the option of a single sweep, procedures "single_gain" and "single_phase" are used to plot the respective data once in a similar manner to the continuous case. The procedures then wait for an escape key before exiting. The scale may be changed for the single gain case in the same manner as the continuous case.

3.7 SUMMARY OF THE LOOP-BACK SYSTEM

The entire loop-back system, with the connection of the various parts described, is best illustrated by a block diagram as given in Figure 3.7.1. Photographs of the laboratory set-up and the circuitry are given in Figures 3.7.2 and 3.7.3.

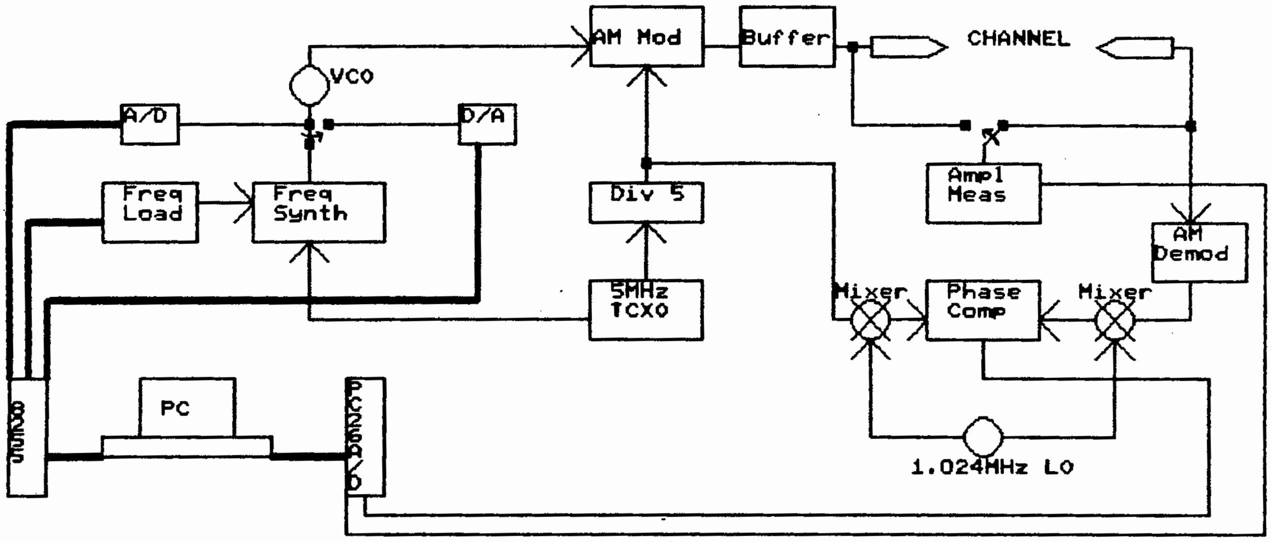


Figure 3.7.1 Block Diagram of Loop-back Measurement System

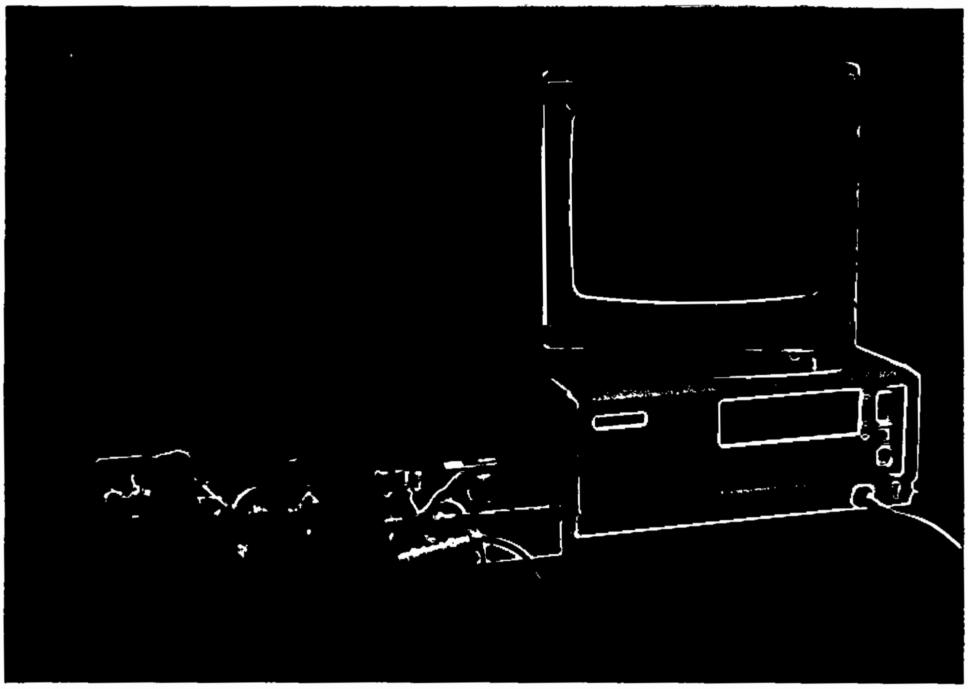


Figure 3.7.2 The Laboratory Test Set-up

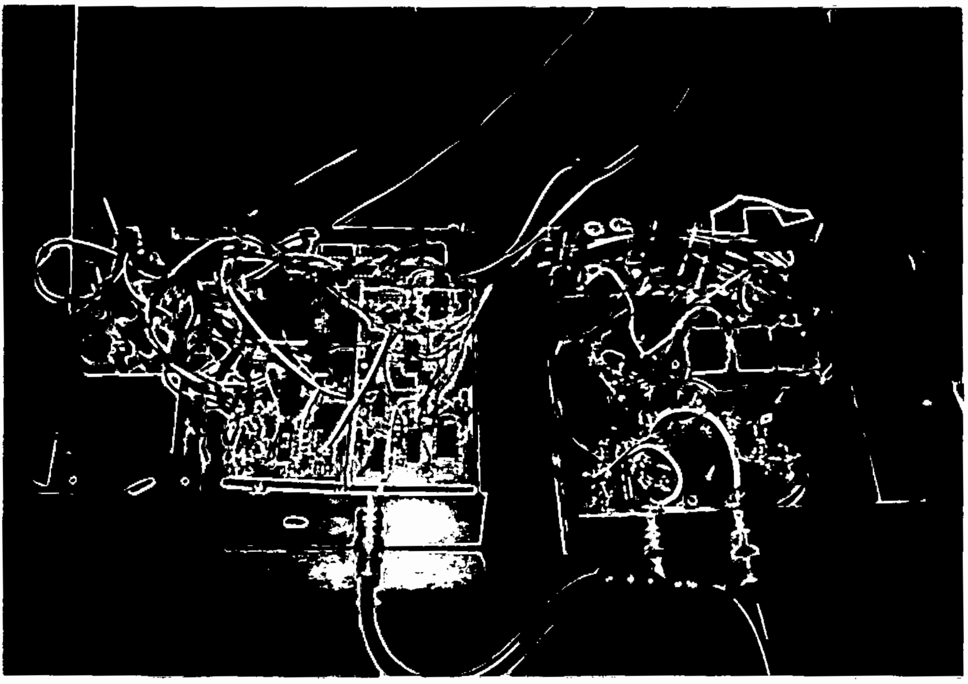
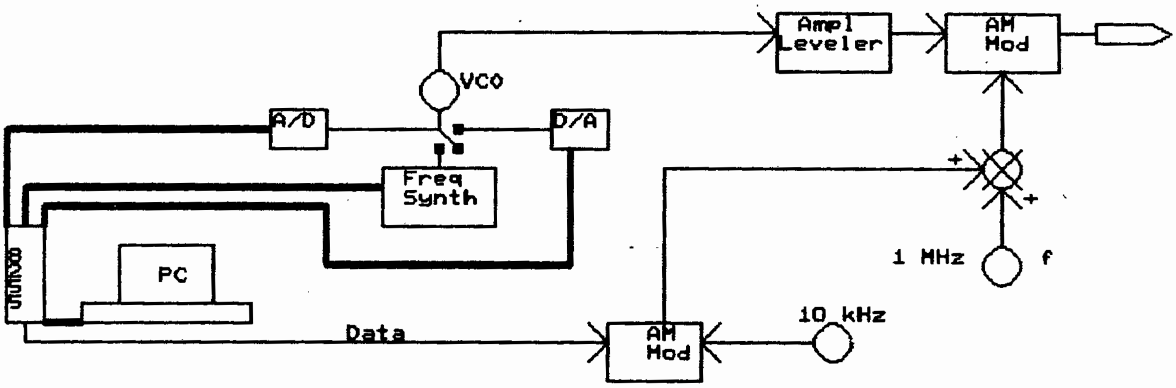


Figure 3.7.3 The Circuitry

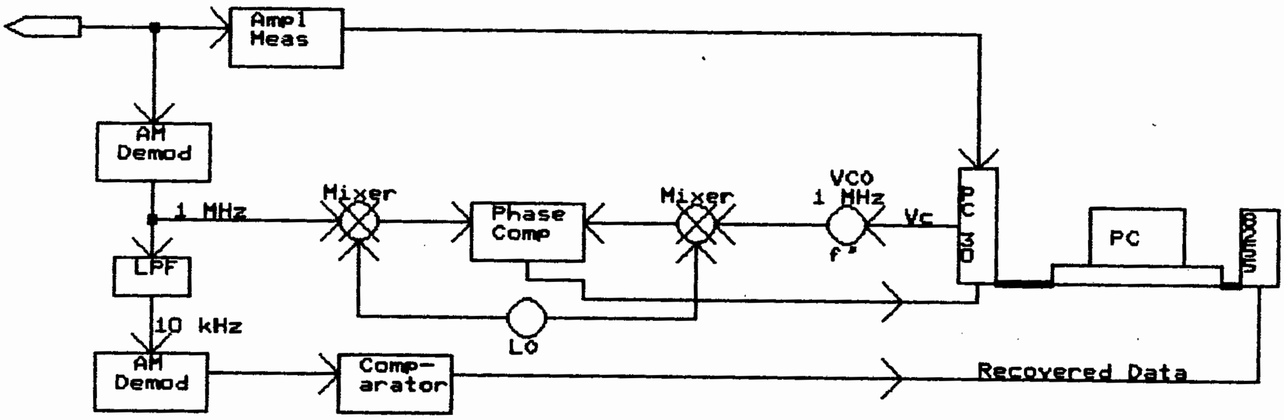
The left hand enclosure contains the power supply, VCO, frequency synthesizer, frequency loading interface, A/D and D/A interface, modulation circuitry and mixing circuitry. The right hand enclosure contains the amplitude measuring circuitry, the phase comparison circuitry and the demodulation circuitry. The co-axial cable, simulating a channel, extends off the bottom right of the photograph.

3.8 EXTENSION TO AN END-TO-END SYSTEM

The method proposed to extend the existing loop-back system to an end-to-end measuring system is shown in block diagram form in Figure 3.8.1. This involves computer control at both ends of a link.



TRANSMITTER



RECEIVER

Figure 3.8.1 Block Diagram of End-to-end Measurement System

The receiver will have a PC-30 plug-in card, which has both A/D and D/A channels, enabling acquisition of phase and amplitude data as well as analogue control. Data, informing the receiver of the status of the system and synchronizing the receiver and transmitter will be transmitted by amplitude modulating a low frequency (10kHz) carrier with data from a bit of an 8255 port and adding this to the 1MHz modulation. The receiver will demodulate this back to bit form with an amplitude demodulator followed by a comparator.

The phase and amplitude measuring systems will remain the same. The outgoing signal will be amplitude levelled to provide a constant reference for gain measurement so that the amplitude measurement need only be performed at the receiver, with the existing circuitry. Phase measurement will be achieved by locking the receiver 1MHz VCO, f', to the transmitter 1MHz modulating oscillator, f, in a set-up phase. This will be done by adjusting the control voltage to the VCO, Vc, via a D/A channel of the PC-30 until zero phase difference is detected in the set-up phase. Otherwise the same technique and phase measuring circuitry as that developed may be used.

3.9 References

3.1) Eagle Electric, PC-26 Analogue to Digital Converter Board, Application notes, 1984.

3.2) Philips, Bipolar ICs for Radio and Audio Equipment, Data Handbook, 1984, pp.32.

3.3) Philips, pp.31-40.

3.4) J.Matull and J.van Straaten, "**Single-chip Synthesizer for Radio Tuning**", Electronic Components and Applications, vol.4, no.3, May 1982, pp.150-156.

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3.6) D.J.Gale, pp.75-82.

3.7) Plessey Semiconductors, "**Broadband Amplifiers Applications**", 1982, p.26.

3.8) Plessey Semiconductors, p.24.

3.9) Plessey Semiconductors, p.26.

3.10) Plessey Semiconductors, p.26,27.

3.11) Plessey Semiconductors, p.27.

3.12) S.Schrire, Unpublished notes on Tellurometer Phase Measurement.

3.13) Plessey S.A., MRD1 Manual, 1981, p.6-10-14.

CHAPTER FOUR

PERFORMANCE OF THE SYSTEM

The circuit draws a total of 730mA, 540mA from the +12 volt supply, 30mA from the -12 volt supply and 160mA from the +5 volt supply. The performance in respect of frequency generation and speed of measurements, group delay measurement and gain measurement will be described. Unfortunately, there was no microwave link available to perform tests on, consequently all tests had to be performed under laboratory conditions, with co-axial cable acting as the channel.

4.1 FREQUENCY GENERATION AND SPEED OF MEASUREMENT

As predicted, the synthesized sweep is slow, taking 160ms to lock onto the first frequency and 10ms for each subsequent frequency; a total of 2.72s for the whole sweep. To ensure locking on all frequencies, the delays in the software are set such that the total synthesized sweep time is approximately 5 seconds. This includes the time taken for amplitude and D/A measurements.

The unsynthesized sweeps are much faster, with a total time between samples of 260µs (this includes the compulsory delay of 40µs to await the end of conversion and the time for data capture). This gives a total sweep time of 66ms, for 256 samples, which allows sweep rates in excess of 10 per second, as required to follow the fast moving fades associated with multipath fading. When the system is configured to plot each sweep, as it is at present, the time taken for processing and plotting reduces the sweep time to 0.62 seconds. This is slower than desirable, but the software may easily be adapted to store data, without direct plotting, to allow faster sweep rates. The sweep times are summarized in Table 4.1.1.

Table 4.1.1 Sweep Times

Operation	Sweep Time [ms]
Synthesized Sweep	5000
Fast Sweep	66
Fast Sweep and Plot	620

The frequencies generated in the fast sweep are accurate to within ±40kHz of the original synthesized frequencies. This is due to the limitations in resolution and accuracy of the A/D and D/A voltage measurement system. This is acceptable for the 256 steps in the range 50 - 90 MHz.

4.2 GROUP DELAY MEASUREMENTS

4.2.1 Phase Measurement Circuitry

The performance of the phase measuring circuitry was tested with a 24kHz square wave reference and a variable 0 - 360 degree phase shifted version of the reference, measured on an accurate phase meter. This was produced with a phase shifter described in Appendix B. The acceptable linearity of voltage out against phase difference, as measured on a phase meter, is illustrated in Figure 4.2.1. The resolution, is in the order of 1:1000, but this is difficult to determine with any accuracy with the analogue measurements.

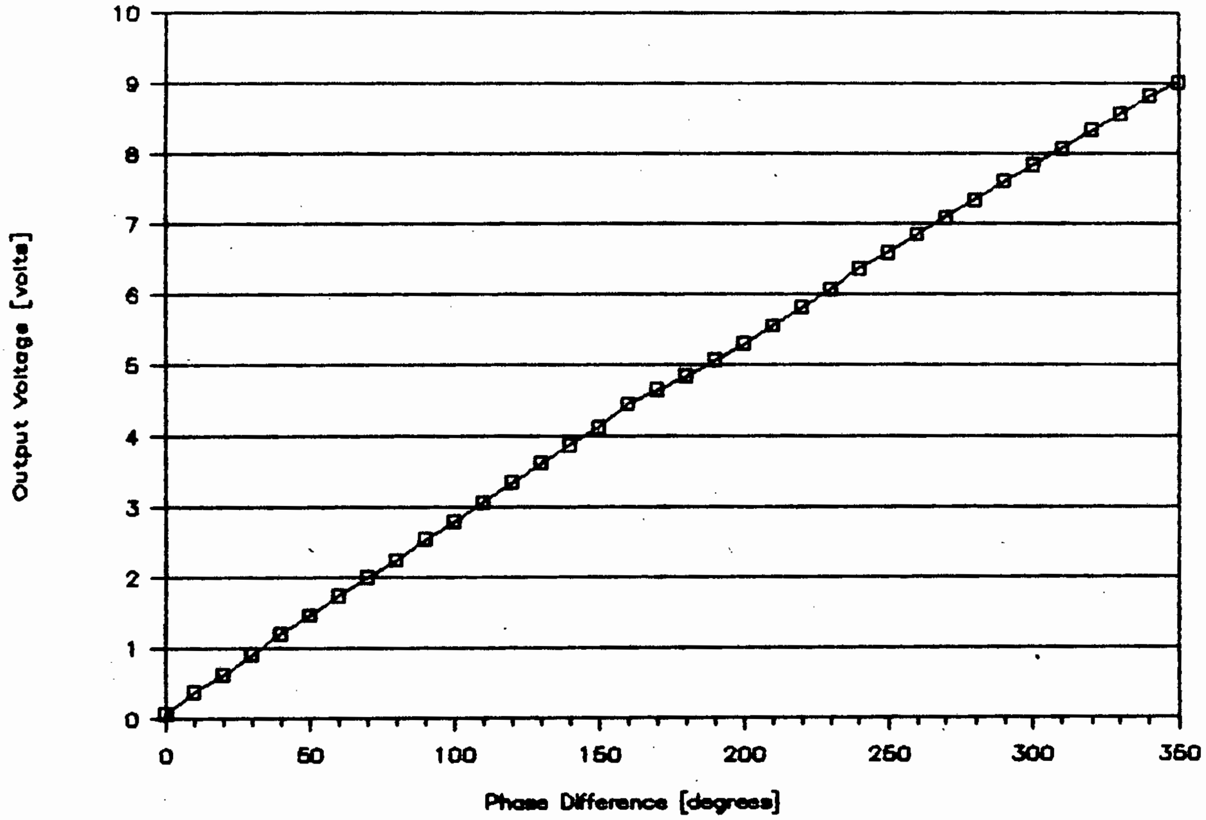

Figure 4.2.1 Linear Phase Comparator Response

4.2.2 Dynamic Range Limitations

A limitation of the phase measuring technique is in the demodulation of the signal to provide the 1MHz comparison signal. Tests performed, with varying amplitude modulated IF signal levels from an HP8656B signal generator, indicated that the envelope detector can only demodulate effectively down to a signal level of -25dBm. Below this, the signal is not amplified above the voltage diode drop and phase comparison cannot take place. A depth of modulation of 20% is required to maintain demodulation to this level. This is unfortunate as phase information will be lost during fades of greater than 25dB. The logarithmic amplitude measuring circuitry with wide dynamic range, as described in section 3.5.1, is unsuitable for this task, as it cannot follow the fast 1MHz modulation.

4.2.3 Group Delay Linearity and Accuracy

The performance of the overall group delay measurement technique was tested by inserting various lengths of co-axial cable in the channel and comparing the group delay result over the IF frequency sweep, with that given by theory. For a length of co-axial cable, l, the phase change, ϕ_a, and the group delay, τ_a, are given by

$$\phi_a = 360.\frac{f*l}{c'} \quad \text{[degrees]} \quad \ldots\ldots\ldots \quad (4.2.1)$$

$$\tau_a = \frac{1}{360}.\frac{d\phi_a}{df} \quad \text{[seconds]} \quad \ldots\ldots\ldots \quad (4.2.2)$$

Thus, $$\tau_a = \frac{l}{c'} \quad \text{[seconds]}$$

where c' is the speed of propagation in co-axial cable, which is $2*10^8$ m/s. The result should be constant over the frequency band.

Despite the use of a smooth, fundamental modulation described in section 3.4.4, the modulation/demodulation process is still noisy and imperfect. Because of this, a small, constant offset in the phase relationship from that expected is introduced which is reflected in the group delay result, being consistently 0.06μs (± 0.01μs) greater than predicted. The offset is far more severe when modulation with a square wave with many harmonics is used.

The offset is compensated for in software. The result is consistent with theory as shown in Table 4.2.1 and Figure 4.2.3. A brief procedure was added to the software to calculate the average group delay measured over the frequency range.

Table 4.2.1 Predicted and Measured Group Delay for Various Channel Lengths

Length of Cable [m]	Predicted Group Delay [μs] (1/c′)	Average Measured Group Delay [μs]
0	0.000	0.001
15	0.075	0.073
18	0.090	0.091
25	0.125	0.126
33	0.165	0.168
37	0.185	0.184
40	0.200	0.200
58	0.290	0.295
70	0.350	0.340
85	0.425	0.429

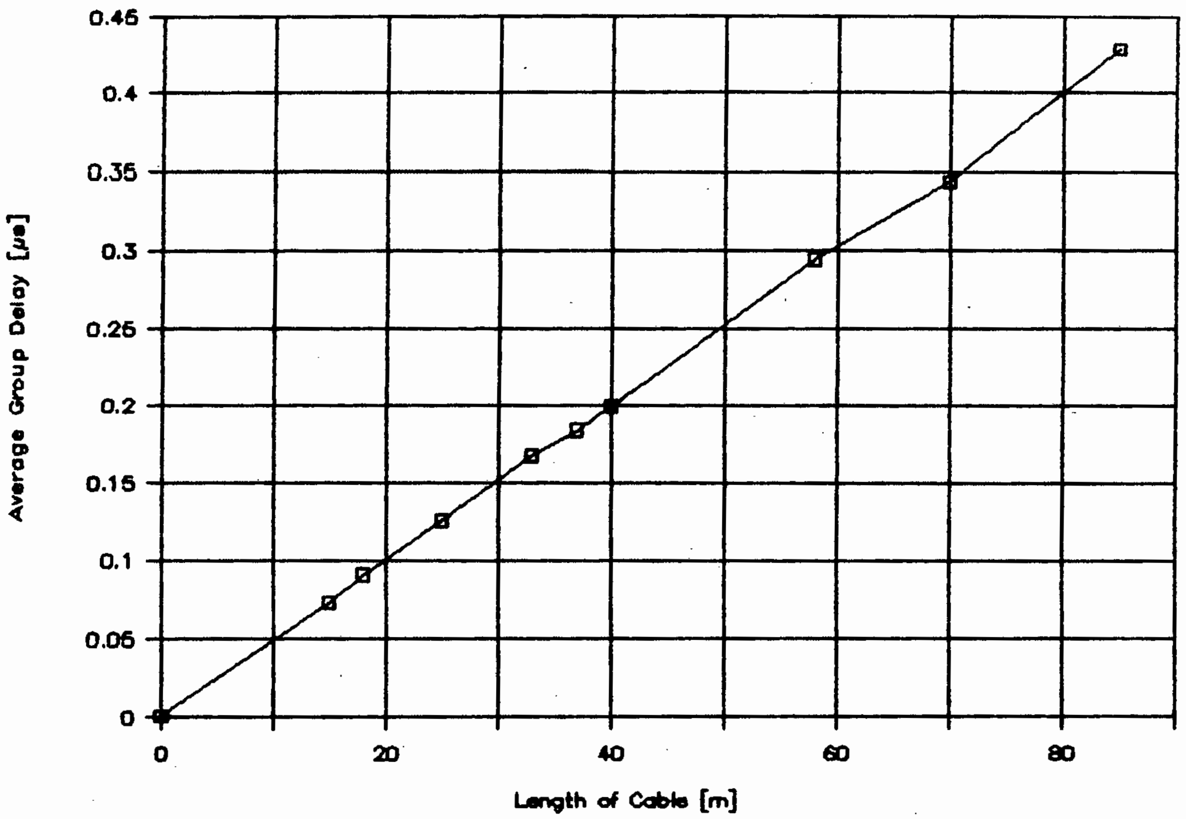

Figure 4.2.3 Corrected Group Delay against Channel Length

Without the ant-coincidence circuitry described in section 3.4.8, when the measured phase difference is very close to 0 degrees, corresponding to ±0.1μs of group delay, rapid transitions occur between 0 and 360 degrees of measured phase difference, which shows up as sharp deviations from 0.1μs displayed group delay. This is corrected with the anti-coincidence circuitry and corresponding software.

There is some deviation from the constant group delay expected over the frequency band, with a maximum deviation of 0.02μs from the average value. This is mainly due to the imperfect modulation and demodulation involved in the phase measurement process. An example plot of constant group delay response is given in Figure 4.2.4.

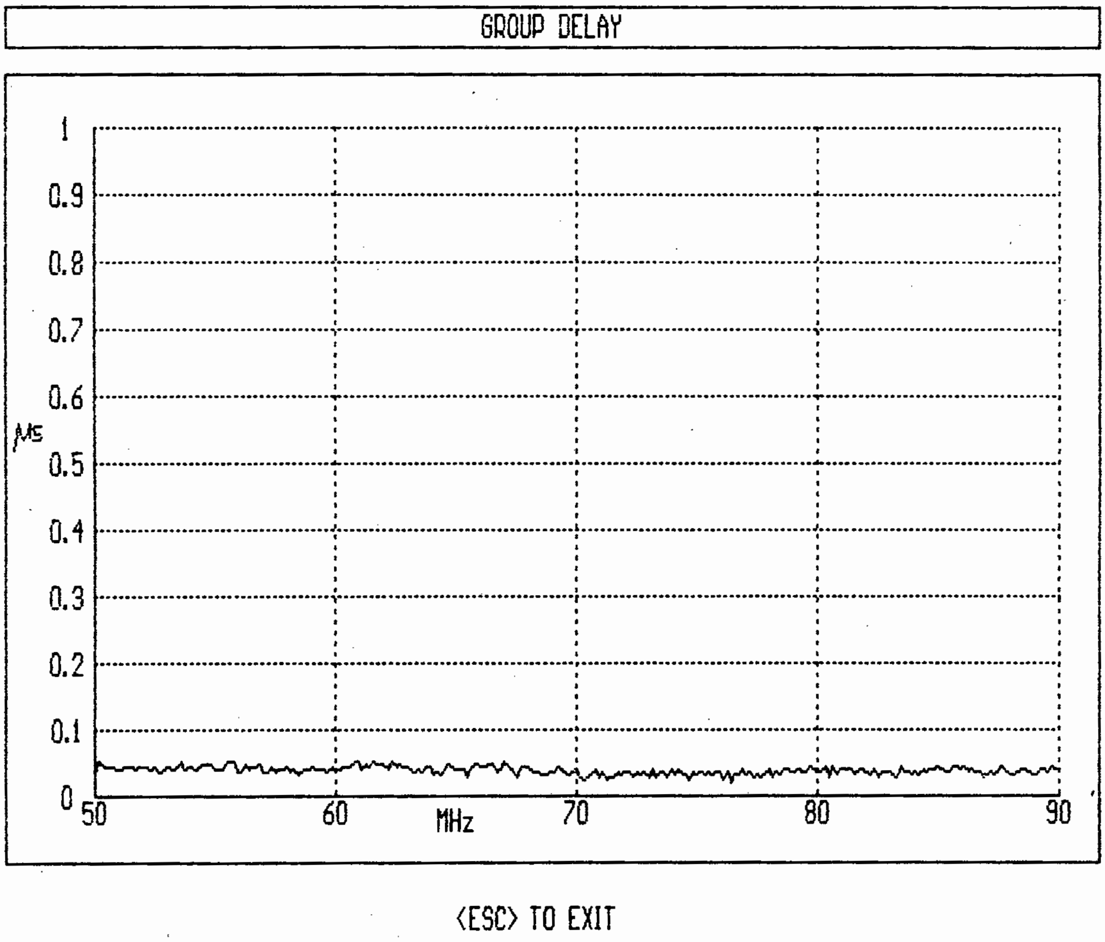

Figure 4.2.4 Group Delay Plot for 15m Channel Length

The degree of accuracy is not sufficient when relative differences in delay of multipath signals of a few nano-seconds are expected. The greatest difference in group delay that can be determined is approximately 20ns. The total group delay over a link will be greater than the maximum 1μs, but the value measured will "loop around" to give the fractional part in micro-seconds. The absolute value is not important, but rather the relative difference from the single path value, caused by relative delays of multipath. A better system would be to have greater resolution in phase measurement and less range. This would allow more accurate measurement of relative group delays caused by multipath.

A primary cause for the lack of accuracy is that the present system does not have ideal modulation and demodulation methods. The modulation is noisy and the demodulation lacks dynamic range.

4.3 GAIN MEASUREMENT

4.3.1 Amplitude Measuring Circuitry

Varying amplitudes of IF signal in the range 50 - 90 MHz were delivered to the amplitude measuring circuitry from an HP8656B frequency generator and the output level monitored. The graph of Figure 4.3.1 indicates the accurate logarithmic response for the input amplitude range of -5dBm to -70dBm - a dynamic range of 65dB. The varying responses for the different frequencies is not important because a ratio of amplitude measurements, at each frequency, is used for gain calculation and not an absolute value. The linearity of the logarithmic law for each frequency is the important point.

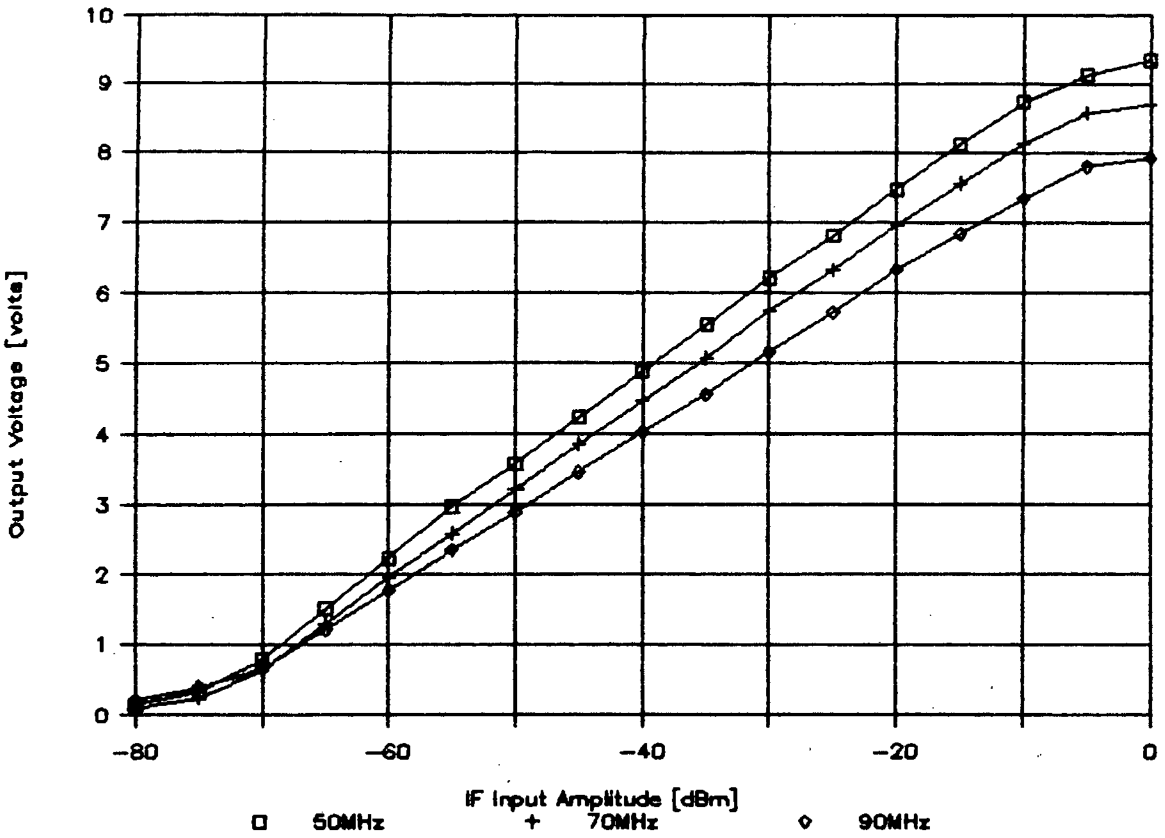

Figure 4.3.1 Logarithmic Response of Amplitude Detector

4.3.2 Gain Linearity and Accuracy

In order to determine the accuracy of the gain measurement, the frequency generating section of the circuitry was replaced with an HP8656B frequency generator and a constant -5dBm 70MHz supplied for the initial sweep. The signal level was then lowered and the resultant gain displayed was determined. The results are given in Table 4.3.1.

Table 4.3.1 Gain Display for Reducing Signal Levels

Input Level [dBm]	True Attenuation [dB]	Gain Displayed [dB]
-5	0	0.0
-10	5	-4.2
-15	10	-9.5
-20	15	-14.2
-25	20	-19.5
-30	25	-25.4
-33	30	-29.8
-40	35	-34.8
-45	40	-39.5
-50	45	-44.5
-55	50	-49.5
-60	55	-54.5
-65	60	-58.0

As a further test of the effect of attenuation in the channel, the complete system was set up and varying amounts of attenuation introduced into the channel using high accuracy co-axial attenuators. The average measured gain over the frequency band was determined. The results are given in Table 4.3.2.

Table 4.3.2 Gain Measured against Channel Attenuation

Attenuation [dB]	Average Gain Measured [dB]
0	0.0
6	-6.0
10	-10.5
16	-15.5
20	-20.5
23	-23.0
26	-25.0
30	-28.0
39	-35.0

There is a certain amount of ripple on the display from the constant gain expected over the frequency band. This deviation is a maximum of ±2dB from the average value for attenuations less than 35dB. For larger attenuations, the effect becomes more severe, with larger ±5dB variations and a lower than expected average level. The primary reason for this is mismatching between the transmitter and receiver circuitry. Different standing waves are introduced on the channel depending on whether amplitude measurement is taken on the outgoing or return signals; the transmitter seeing different loads depending where the amplitude measurement takes place. The amplitude variations caused are most marked when the return signal is low. This is despite the attempts described in section 3.5.2 to correct this problem. The problem may be eliminated by a system whereby amplitude measurements are only performed at one point, with constant matching. Such a method would be used in the proposed end-to-end measurement system, where the signal is leveled at the transmitter, as an amplitude reference.

A second factor causing a non-flat display, is the variations in amplitude caused by the 1MHz amplitude modulation. The amplitude measuring circuitry tries to follow this, causing some rippling. However, the circuitry is not fast enough to follow the 1MHz modulation and the effect is smoothed. An example gain plot is given in Figure 4.3.2.

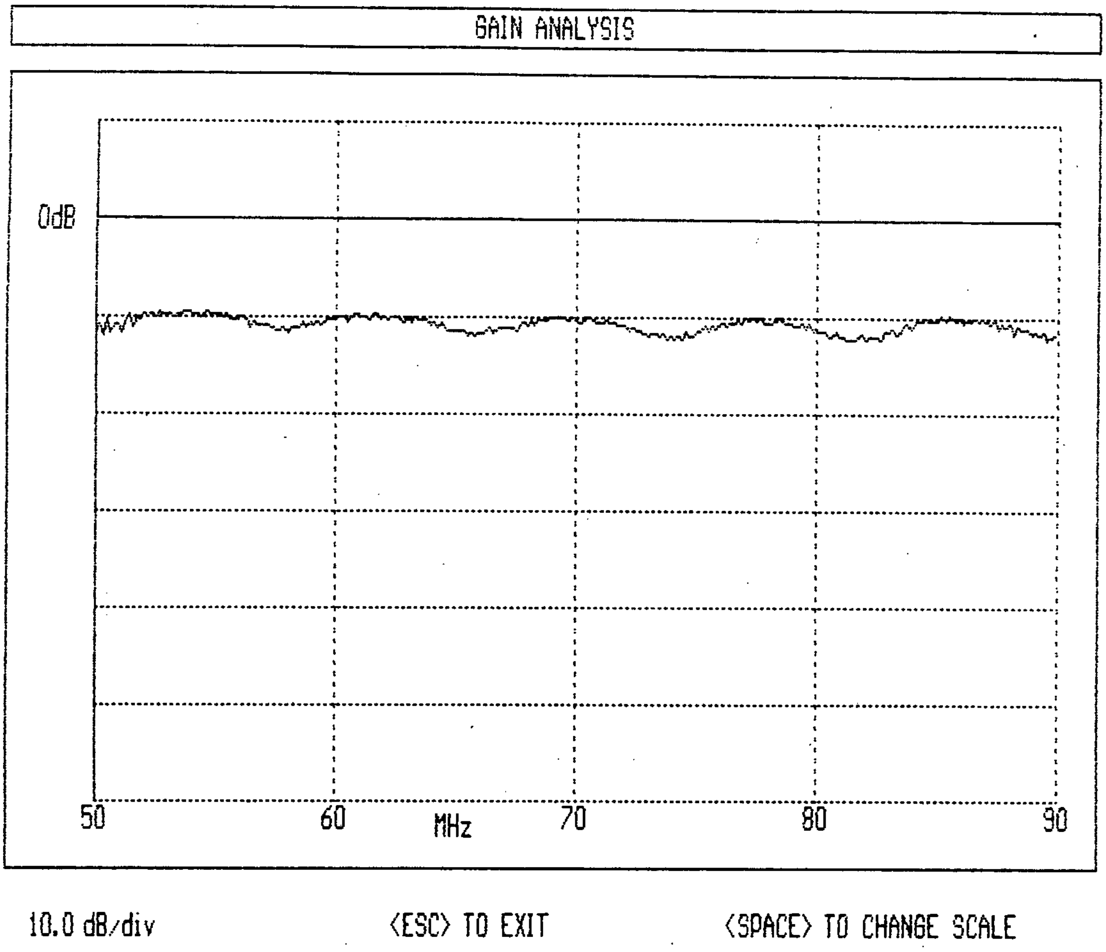

Figure 4.3.2 Gain Plot for 10dB Attenuation

4.4 PERFORMANCE UNDER MULTIPATH CONDITIONS

Owing to the lack of availability of a link, the system could not be tested under typical field conditions, including multipath conditions. However, a two channel multipath situation was simulated by splitting the signal between two pieces of similar length co-axial cable, the shorter one simulating the direct path and the longer one a reflected or refracted path. The plots of gain and group delay are given in Figures 4.4.1 and 4.4.2 for different two-path conditions. The plots exhibit classic sharp, deep frequency selective fades, indicated by the 30dB attenuations and increase in group delay.

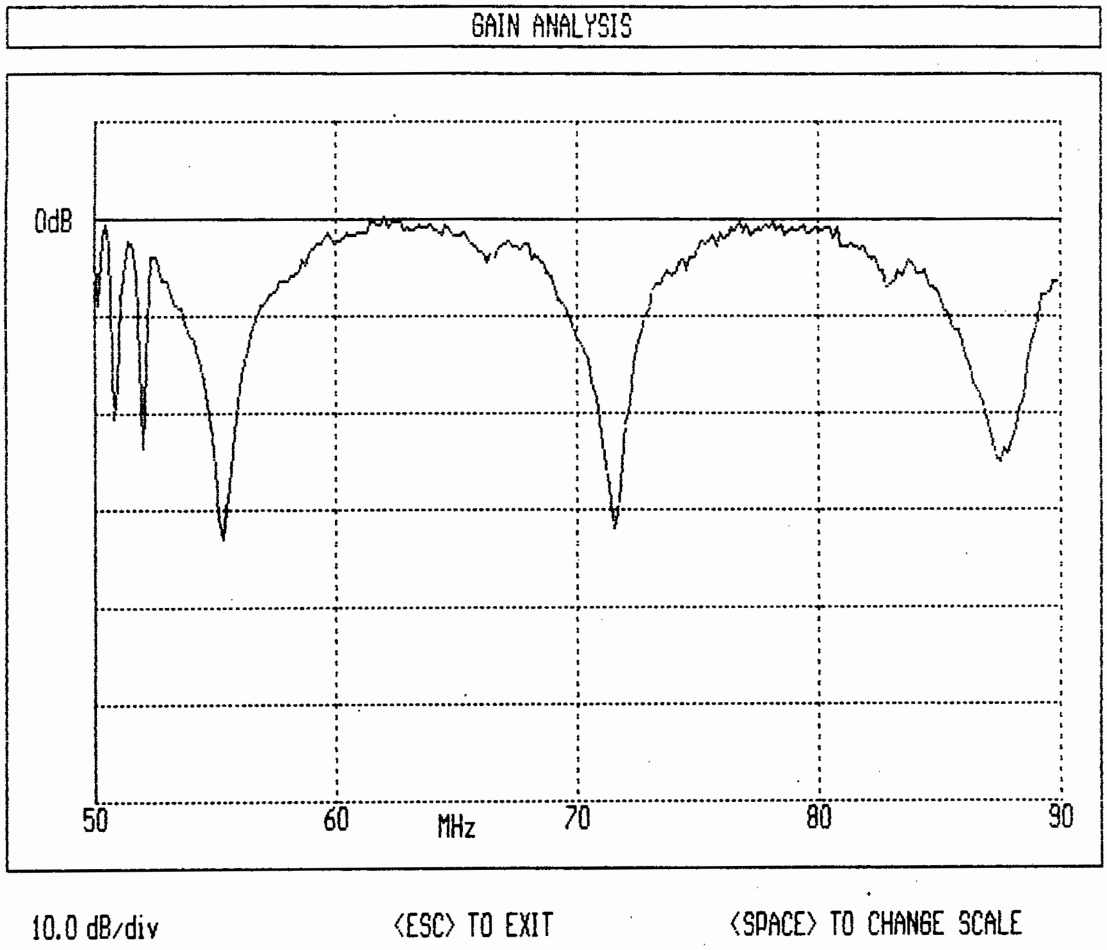

Figure 4.4.1 Gain Plot for Multipath Conditions

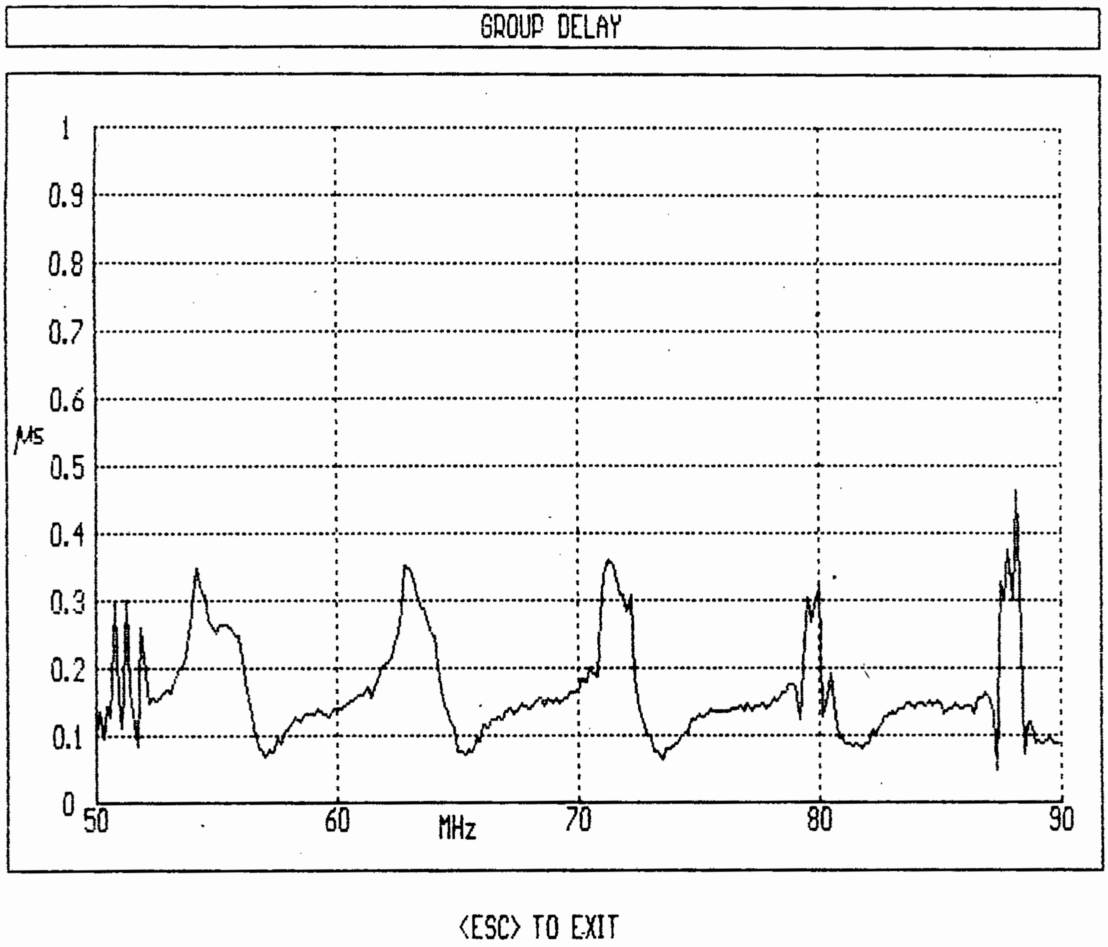

Figure 4.4.2 Group Delay Plot for Multipath Conditions

No further quantitative tests to determine the validity of multipath measurements could be performed, because of the lack of availability of a fading simulator or similar piece of equipment.

SUMMARY

The following units have been linked together in a simple loop-back, IF gain and group delay measurement system:

Data Interfaces

Phase and amplitude analogue data is read by the PC via a PC-26 A/D acquisition card. Digital data is read from and written to the hardware via two 8255 input/output ports.

PC-26: 2 of 16 channels used
12 bit resolution
Maximum 25kHz rate of conversion
Three 8 bit 8255 ports included
8255s: Six 8 bit programmable input or output ports
1MHz rate of data transfer

IF Frequency Generation

50 to 90 MHz frequency sweeps are performed using a Plessey SP1648 VCO controlled by a Philips SAA1057 frequency synthesizer, for synthesized sweeps, or by a D/A - A/D interface for fast, non-synthesized sweeps. Data is transferred from the PC to the synthesizer by a parallel to serial frequency loading interface.

50 - 90 MHz IF bandwidth
-5dBm output level
Synthesized ±1Hz stability
2.72s synthesized sweep time
66ms fast sweep time

Group Delay Measurement

Group delay measurement involves amplitude modulating the swept IF signal with a stable signal and comparing the phase of the demodulated return signal with the original reference modulating signal. A mixing process is used to enable low frequency phase comparisons.

Phase Comparator: 1:1000 resolution
Accurate linear response
30dB dynamic range
Anti-coincidence circuitry
Group Delay: 0 - 1μs range
±0.02μs accuracy

Gain Measurement

Gain measurement involves comparison of the amplitudes of the outgoing and return swept IF signal.

Amplitude Measurement: 65dB dynamic range
Accurate logarithmic response
Gain Measurement: ±2dB accuracy

Software

The software is written in Turbo Pascall 4.0 and presents the gain and group delay results in graphical form. Different procedures control the frequency synthesis and subsequent frequency sweeping and acquisition, processing and display of gain and group delay data. The software may easily be modified for storage of data and/or display in other forms.

Total sweep time with plotting: 0.62 seconds

CONCLUSIONS AND RECOMMENDATIONS

A simple, prototype, PC based system exists for measuring gain and group delay on a microwave link for the 70MHz IF frequency band, in a loop-back system. This is of sufficient speed and range to follow fading events associated with multipath conditions.

- The hardware/software interfaces of the 8255 and PC-26 cards have proved adequate for data capture and control.

- The frequency synthesizer/generator system allowing slow, synthesized sweeps or fast unsynthesized sweeps functions as required.

- The gain measurement system has the required dynamic range and adequate accuracy. However, matching problems cause spurious rippling in the measured gain, especially for higher attenuations. It is recommended that this be improved by a system whereby amplitude need only be measured at one point, so that non-constant matching does not arise. It is envisaged that in an end- to-end measurement system this will be less of a problem, as amplitude measurement will be taken at one end only, with constant matching.

- The group delay measurement system works adequately for signal levels above -25dBm. The present system is attractive because of the direct group delay result from the phase measurement. The resolution and accuracy is insufficient to provide an accurate representation of group delay differences caused by multipath conditions of relative delays less than approximately 20 nano-seconds. It is recommended that a more sophisticated means of amplitude modulation and demodulation be employed to increase the dynamic range and increase the accuracy and resolution. This will also correct the further problem of constant phase offset. Alternatively, a method of phase measurement directly at the IF frequency should be used, such as the "nFr" scheme outlined by Mr. D.Gale and mentioned in section 3.4.1. The synthesizer for such a system has already been developed.

Transitions between 0 and 360 degrees for phase measurements close to 0 degrees are corrected by anti-coincidence circuitry.

The software controls the hardware and processes and displays data as required. It may be adapted and extended in numerous ways to display and/or store the data as may be required for specific cases. One such extension recommended is a facility whereby data is only recorded or plotted when the gain or group delay exceed certain limits. This will save time and reduce memory requirements. A periodic automatic recalibration involving a synthesized sweep should be added by simple addition to the software, as opposed to the present manual option.

This system needs to be extended to an end-to-end measurement system. It is recommended that this be done in the method proposed. This makes use of the methods developed for the loop-back system, with some adaptions and the same circuitry already developed, with some additions.

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APPENDIX A

SIXTH ORDER ELLIPTIC LOW PASS FILTER DESIGN

The sixth order elliptic low pass filter was designed as an anti-aliasing and buffering filter for the PC-26 A/D acquisition card. It was subsequently found to be unnecessary and not used.

Two MF10 dual switched capacitor filters, employing three cascaded stages were used in the design to implement a sixth order elliptic low pass filter, as described in [A.1]. Referring to the low pass filter tolerance limits as illustrated in Figure A.1, the sampling frequency, fs, of the A/D card was thought to be approximately 5kHz. This was set at the beginning of the stop band, with the pass band extending to fc = 2kHz, to give fs/fc = 2.5, which exceeds Nyquist's criterion to avoid aliasing. The design was for a minimum attenuation, Amin, between pass and stop band of 74dB and maximum ripple, Amax, in the pass band of 0.1dB.

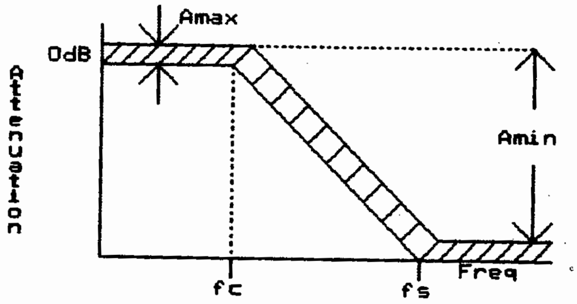


Figure A.1 Low Pass Filter Tolerance Limits

The circuit is given in Figure A.2. The external clock, implemented with a comparator U4, sets the cut-off frequency, which may be adjusted, being 10 times the cut-off frequency. The values of the resistors connecting the high pass, low pass and inverting inputs of the internal operational amplifiers of the three switched capacitor filters, sets the other limits. The equations for calculating these values may be found in [A.2]. The nearest available resistor values to those calculated are given below:

R1A = 22K   R2A = 12K   R3A = 10K
R4A = 22K   RLA = 22K   RHA = 150K
R2B = 22K   R3B = 22K   R4B = 22K
RLB = 22K   RHB = 270K
R2C = 27K   R3C = 100K   R4C = 22K
RLC = 22K   RHC = 1M8
RG1 = 22K   RG2 = 100K
R1 = R2 = R3 = 1K
C1 = C2 = C3 = C4 = 10nF   C5 = 820nF

The unavailability of exact resistor values degrades the performance of the original design.

The input is buffered and low pass filtered and a variable DC voltage supplied to correct the internal DC offset of the circuitry. The output is amplified to the correct level and low pass filtered to remove the ten times clock frequency component. The transfer function of the filter is given in the spectrum of Figure A.3, indicating the steep, 70dB roll off between pass and stop bands.

References

A.1) National Semiconductor, Switched Capacitor Filter Handbook, 1984.

A.2) National Semiconductor.

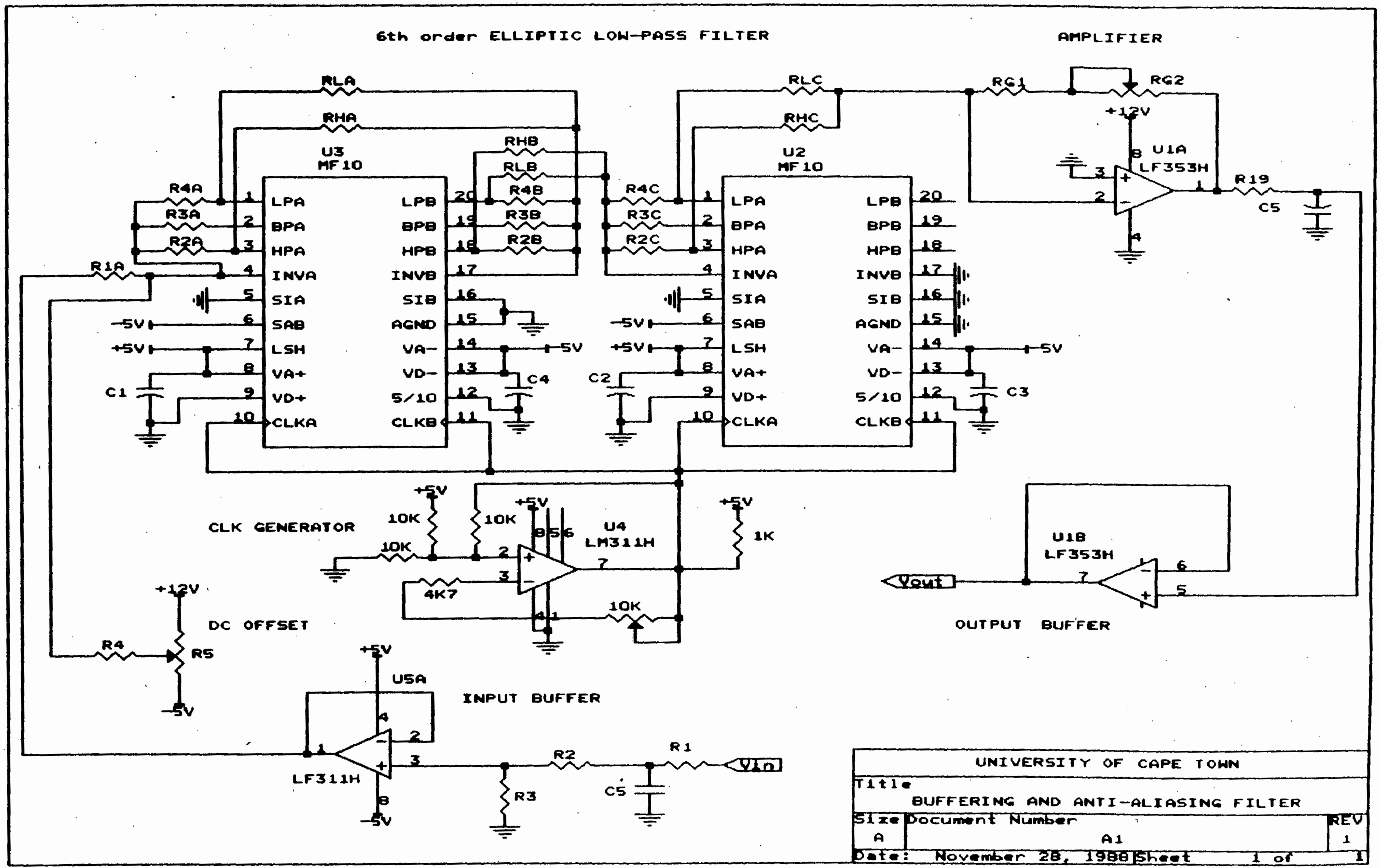


Figure A.2 Sixth Order Elliptic Low Pass Filter

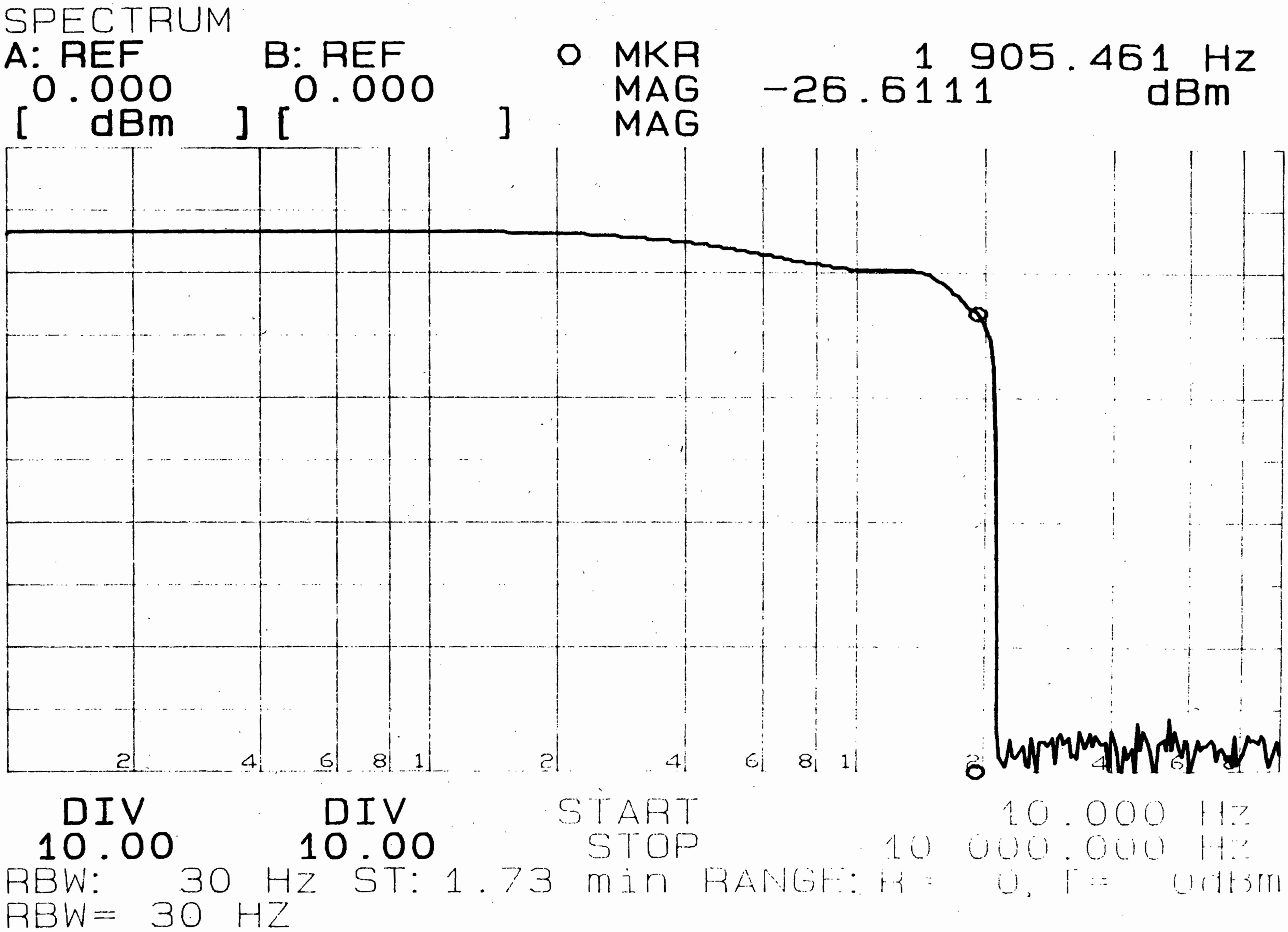


Figure A.3 Transfer Function of the Filter

APPENDIX B

PHASE SHIFTER CIRCUITRY

The phase shifter was used to test the phase measuring circuitry. A unity gain phase splitter, employing an emitter degenerated amplifier with unity gain, followed by a variable RC shifting stage was used [B.1] as shown in Figure B.1.

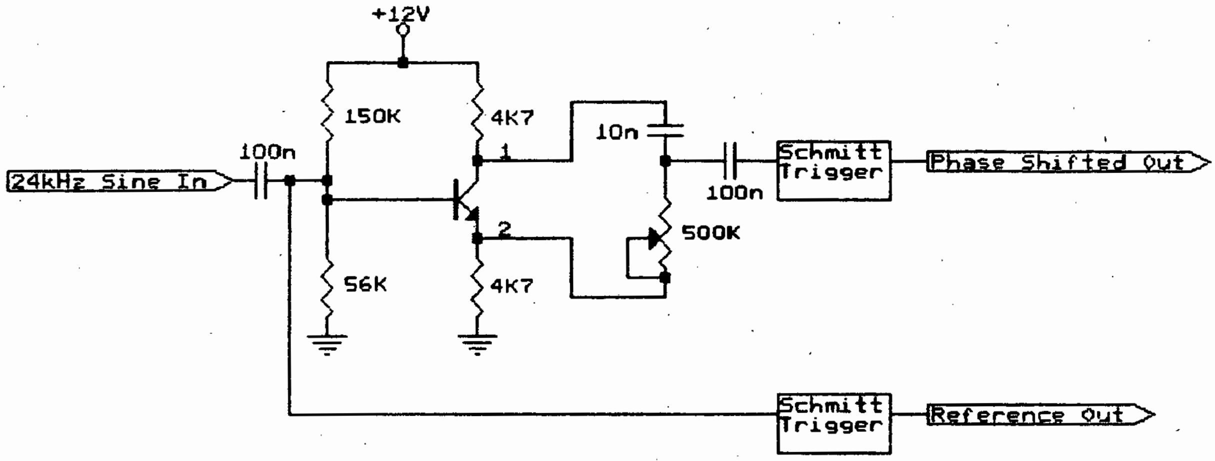


Figure B.1 Phase Shifter

For a sinusoidal input, the phase splitter generates the signal at point 2 and its inverse at point 1. The variable RC stage produces an output sine wave of adjustable phase of nearly 0 - 180 degrees, with constant amplitude. The RC values need to be chosen to present an impedance that is high compared to the emitter and collector resistors, so that the phase splitter can drive the RC phase shifter. When R is low there is insufficient drive and so the full 0 - 180 degree range cannot be reached. The input and the phase shifted output are squared with Schmitt triggers with adjustable reference points, to be used as test signals on the reference and measured inputs of the phase measuring circuitry. To achieve the required full 0 - 360 degree phase shift range, the two inputs to the reference and measured inputs are reversed after the first 180 degrees, to achieve an effective

180 - 360 degree phase shift. Phase shifts close to 180 degrees could not be produced in this manner. To test the circuitry for a 180 degree phase shift, a simple inverter was used. The phase shift was accurately measured with a phase meter.

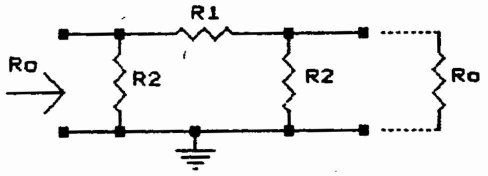
Reference

B.1) P.Horowitz and W.Hill, "**The Art of Electronics**", Cambridge University Press, New York, 1980, pp.63,64.

APPENDIX C

ATTENUATION AND MATCHING NETWORK

In order to attenuate the IF signal from the output MAR amplifier stage to the correct level for amplitude measurement and to maintain a 50Ω output impedance, a pi resistor section attenuator network was used as shown in Figure C.1, having input and output impedance of 50Ω.



Ro = 50Ω

Figure C.1 Pi section Matching Network

In this case, the signal needs to be attenuated from a level of 280mV RMS to 120mV RMS (-5dBm), giving a factor of

$$N = 280/120 = 2.33$$

The values of R1 and R2 are given by [C.1]:

$$R1 = Ro * \frac{N^2 - 1}{2N} = 50 * \frac{4.43}{4.66} = 47.5\Omega$$

$$R2 = Ro * \frac{N + 1}{N - 1} = 50 * \frac{3.33}{1.33} = 125\Omega$$

The values used are: R1 = 47Ω
R2 = 120Ω

Reference

C.1) W.Fraser, "**Telecommunications**", Macdonald and co., London, 1967.

APPENDIX D

SOFTWARE

The listing of the program, written in Turbo Pascal 4.0 which performs control, processing and display, is given in this Appendix.

```
program PLA;

{---------------------------------------------------------------------------}
{ Program to synthesize frequencies from 50 to 90 MHz and to calculate and  }
{ display the gain and group delay over this range. The program performs    }
{ control on the hardware via two 8255 I/O chips and obtains analogue data  }
{ via a PC-26 A/D card.                                                     }
{---------------------------------------------------------------------------}

uses
    graph, crt, dos;

const
 max = 256;
 delay_loop = 10;
 factor = 59;

var
 voltage, xmax, xmin, ymax, ymin, scalex, scaley, dB_div, zeropoint, group_delay
: real;
 done, x, xleft, yleft, xorig, yorig, width, height, grdriver, grmode: integer;
 screen: word;
 dataa, datab: byte;
 outline: pointer;
 ymsb, ylsb, output, gain, phase, invert: array[0..256] of integer;
 low_bits, high_bits: array[0..256] of byte;
 opt: char;

{---------------------------------------------------------------------------}

Procedure BEEP;
 begin
  sound(500); delay(500); nosound;
 end;

{---------------------------------------------------------------------------}


procedure dac(y: integer);

{Procedure to perform 1 D/A conversion of data from A/D lookup table}

var
 i: integer;
begin
 port[$264] := low_bits[y];          {Port A, lower byte}
 port[$266] := $D8 + high_bits[y];   {Chip select low and upper byte}
 port[$266] := $DC + high_bits[y];   {Chip select high and upper byte}
end;

{---------------------------------------------------------------------------}

 procedure adc;

 {Procedure to perform an A/D conversion}

 var
  i, temp: integer;
 begin
  port[$266] := $2C;                                      {Write low}
  port[$266] := $3C;                                      {Read and write high}
  for i := 1 to 50 do begin end;                          {delay}
  port[$266] := $34;                                      {Read low for 1st byte}
```

X

```
   dataa := port[$265];                                {1st byte}
   port[$266] := $3C;                                  {Both high}
   port[$266] := $34;                                  {Read low for 2nd byte}
   for i := 1 to 50 do begin end;                      {delay}
   datab := port[$265];                                {2nd byte}
   port[$266] := $3C;                                  {Both high}
   low_bits[x] := (datab shr 6) + ((dataa shl 2) and $FC); {Convert to byte form}
   high_bits[x] :=((dataa and $C0) shr 6);               {          for A/D  }
  end;

{-----------------------------------------------------------------------------}

procedure initialize;

{Procedure to initialise frequency synthesizer}

var
 i: integer;
 begin
  port[$263] := $88;                      {control word for 8255: 10001000}
  port[$262] := $0B;                      {port C: 00001011 reset flip-flop}
  port[$260] := $05;                      {word B, port A: (tests: 5 = lock?)}
  port[$261] := $E3;                 {word B, port B:E1, E3, E5, ED, FD(gains)}
  port[$262] := $08;                      {1st pulse low}
  port[$262] := $04;                      {2nd pulse high/low}
  port[$262] := $0A;                      {return}
  repeat
   done := port[$262] or $EF;             {Wait for DLEN to go low}
  until done = $EF;
  for i := 1 to 1000 do begin end;
 end;


{-----------------------------------------------------------------------------}

procedure freq_synth;
{-----------------------------------------------------------------------------}
{ Procedure to synthesize 256 frequencies from 50 - 90 MHz. For each frequency }
{ the outgoing amplitude is measured by an A/D conversion and stored in a look }
{ up table and the procedure ADC is called to measure the voltage on the       }
{  varactor.                                                                   }
{-----------------------------------------------------------------------------}

 var
  i, j: integer;
  data: word;
 begin
  initialize;
  port[$267] := $82;                    {Control word for 2nd 8255: 10000010}
  port[$266] := $20;                    {Set switches on to measure outgoing}
  clrscr;
  gotoxy(25, 13);
  write('Synthesizing frequencies...');
  data := $0C80;
  port[$260] := $80;                        {port A for 50 MHz}
  port[$261] := $0C;                        {port B for 50 MHz}
  delay(100);
  x := 0;
  for j := 0 to max do                      {256 times}
   begin
    port[$262] := $A0;                      {1st pulse low}
    port[$262] := $04;                      {2nd pulse high/low}
    port[$262] := $0A;                      {return}

    {AD sample: amplitude measurement}
    port[$702] := $12;                    {Channel 1 and clear software clock}
```

```
    port[$702] := $13;                          {Channel 1 and set software clock}
    for i := 0 to delay_loop do                 {delay sets sample frequency}
     begin
     end;
    ymsb[j] := port[$701];                      {most significant byte}
    ylsb[j] := port[$700];                      {least significant byte}
    output[j] := (ymsb[j] and $0F)*256 + ylsb[j];  {Mask low bits of msb + lsb}
    if output[j] = 0 then output[j] := 1;       {Avoid divisions by zero later}
    adc;                                        {A/D conversion from varactor}

    data := data + $A;                          {Add 156.25kHz}
    port[$260] := data and $00FF;               {New port A}
    port[$261] := (data and $FF00) shr 8;       {New port B}
    x := x + 1;
    for i := 1 to 3000 do begin end;            {Wait to lock}
   end;  {for}
   port[$266] := $DC;     {Switches off: future amplitude measurements on return}
 end;

{-----------------------------------------------------------------------------}

procedure AD_sample(channel: integer);
{-----------------------------------------------------------------------------}
{ Procedure to sample channel 1 or 2 of AD card max times. Each time procedure }
{ DAC is called to set each of the frequencies between 50 and 90 MHz.          }
{-----------------------------------------------------------------------------}

var
 i, j: integer;
begin
 for i := 0 to max do                           {max number of samples}
  begin
   dac(i)                                       {Voltage to varactor to set freq};
   if (i >= 0) and (i <= 5) then delay(1);      {Delay for first 5 to catch}
   if channel = 2 then delay(1);                {Delay for phase measurements}
   port[$702] := (channel SHL 4) + 2;     {Channel select and clear software clock}
   port[$702] := (channel SHL 4) + 3;     {Channel select and set software clock}
   for j := 0 to delay_loop do                  {delay sets sample frequency}
    begin
    end;
   ymsb[i] := port[$701];                       {most significant byte}
   ylsb[i] := port[$700];                       {least significant byte}
   invert[i] := port[$266] AND $80;             {Check for inversion}
  end;
end;

{-----------------------------------------------------------------------------}

procedure single_sample;
{-----------------------------------------------------------------------------}
{ Procedure to sample channel 1 and 2 of AD card max times for phase and      }
{ gain measurements off the same sweep. Each time procedure DAC               }
{ is called to set each of the frequencies between 50 and 90 MHz.             }
{-----------------------------------------------------------------------------}

var
 i, j: integer;
 gain_msb, gain_lsb, phase_msb, phase_lsb: array[0..256] of integer;

begin
 for i := 0 to max do                           {max number of samples}
  begin
   dac(i)                                       {Voltage to varactor to set freq};
   delay(2);
{gain}
   port[$702] := $12;                          {Channel 1 and clear software clock}
```

```
   delay(1);
   port[$702] := $13;                          {Channel 1 and set software clock}
   for j := 0 to delay_loop do                 {delay sets sample frequency}
    begin
    end;
   gain_msb[i] := port[$701];                   {most significant byte}
   gain_lsb[i] := port[$700];                   {least significant byte}
   gain[i] :=  ((gain_msb[i] and $0F)*256) + gain_lsb[i];   {Calc gain value}
{phase}
   port[$702] := $22;                          {Channel 2 and clear software clock}
   delay(1);
   port[$702] := $23;                          {Channel 2 and set software clock}
   for j := 0 to delay_loop do                 {delay sets sample frequency}
    begin
    end;
   phase_msb[i] := port[$701];                  {most significant byte}
   phase_lsb[i] := port[$700];                  {least significant byte}
   invert[i] := port[$266] AND $80;             {Check for inversion}
   phase[i] := ((phase_msb[i] and $0F)*256) + phase_lsb[i];   {Calc phase value}
  end;
end;

{---------------------------------------------------------------------------}


procedure  gain_parameters;
{Procedure to set up graph size and position}

begin

 grdriver := detect;
 InitGraph(grdriver, grmode, '');               {Initialize graphics}
 xmax := max;
 xmin := 0;
 xorig := 0;
 ymax := 10;                                    {Axes co-ordination}
 ymin := -60;
 yorig := 0;
 xleft := 75;
 yleft := 295;                                  {Graph position}
 width := 600;
 height := 252;
 scalex := width/(xmax - xmin);                 {Scaling factors}
 scaley := height/(ymin - ymax);
 dB_div := 10;                                  {Scale}
 zeropoint := yleft - (height*6/7);             {Reference point for plotting}
end;

{---------------------------------------------------------------------------}

procedure gain_graph;
var
 i, j: integer;
 dB_div_string: string;

 begin
  {draw box}
  rectangle(20, 0, 700, 15);
  rectangle(20, 25, 700, 320);

  {draw axes and grids}
  line(xleft, yleft, xleft, yleft - height);

  for j := 0 to 7 do
    begin
     setlinestyle(1, 0, 1);                     {Dotted lines}
```

```
      if j = 6 then setlinestyle(0, 0, 1);      {Solid 0 line}
      line(xleft, yleft - j*(height div 7), xleft + width, yleft - j*(height div
7));
     end;
     for j := 1 to 4 do
      begin
        line(xleft + j*(width div 4), yleft, xleft + j*(width div 4), yleft - hei
ght);
      end;
     setlinestyle(0, 0, 1);                         {Reset to solid lines}

     {Text}
     SetTextStyle(2, 0, 5);
     SetTextJustify(1, 1);
     OutTextXY(360, 6, 'GAIN ANALYSIS');
     OuttextXY(50, 78, '0dB');
     OuttextXY(75, 300, '50');
     OuttextXY(225, 300, '60');
     OuttextXY(375, 300, '70');
     OuttextXY(525, 300, '80');
     OuttextXY(675, 300, '90');
     OuttextXY(300, 303, 'MHz');
     OutTextXY(310, 340, '<ESC> TO EXIT');
     OutTextXY(560, 340, '<SPACE> TO CHANGE SCALE');
     Str(dB_div:4:1, dB_div_string);
     OutTextXY(50, 340, dB_div_string);
     OutTextXY(80, 340, '    dB/div');

     screen := ImageSize(0, 0, 719, 347);           {Save screen}
     GetMem(outline, screen);
     GetImage(0,0,719,347,outline^);                {to memory}
  end;

{---------------------------------------------------------------------------}

procedure gain_scale;

{Procedure to change scale of gain graph}

begin
 closegraph;
 freemem(outline, screen);                        {Free memory}
 {$I-}                                            {Switch off error checking}
repeat
  writeln('Enter dB/div');
  readln(dB_div);
  if dB_div = 0 then dB_div := 0.1;
  clrscr;
until IOresult  = 0;                              {Until correct format entered}
 {$I+}
 ymin := -dB_div * 6;
 ymax := dB_div;
 scaley := height/(ymin - ymax);                  {Calc new scale}
 InitGraph(grdriver, grmode, '');                 {re-initialize graphics}
 gain_graph;                                      {re-draw graph}
end;

{---------------------------------------------------------------------------}

procedure draw_gain;
{Procedure which calls sampling procedure and continuously plots gain points}

 var
  x, y: array[0..999] of integer;
  refresh, i, nx, ytemp, input: integer;
  ratio, ypoint: real;
```

```
  answer: char;

begin
 for i := 0 to max do
  begin
   x[i] := 0;
   y[i] := 0;                                     {Initialize array of points to 0}
  end;

   {Plot first set}
   AD_sample(1);                                      {Sample 256 Points}
   input := ((ymsb[0] and $0F)*256) + ylsb[0];        {Calc value from A/D sample}
   ypoint := 1/factor * (input - output[0]);         {Calc ratio from stored value
   x[0] := xleft;                                     {Calc 1st x and}
   y[0] := round(zeropoint + ypoint * scaley);        {      y positions}
   moveto(x[0], y[0]);                                {Move there}
   nx := 1;
   repeat
     input := ((ymsb[nx] and $0F)*256) + ylsb[nx];     {calc input value}
     ypoint := 1/factor *  (input - output[nx]);       {Ratio}
     x[nx] := round(nx * scalex + xleft);              {Calc subsequent x }
     y[nx] := round(zeropoint + ypoint * scaley);      {          and y positions}
     lineto(x[nx], y[nx]);                             {Draw line to them}
     nx := nx + 1;
   until nx = max;                                     {Until 256 points plotted}
   answer := #3;
   if keypressed then
    begin                                              {Check for ESC}
     answer := readkey;
     if answer = #27 then
      begin
       closegraph;
       freemem(outline, screen);                      {Free memory}
       exit;
      end;
      if answer = #32 then gain_scale;             {Change scale if space pressed
    end;

 {Plot subsequent sets}
  refresh := 0;
  repeat
  if refresh = 10 then                                {Refresh every 10 sweeps}
   begin
    PutImage(0,0,outline^, Orput);                    {Refresh screen}
    refresh := 0;
   end; {if}
   AD_sample(1);                                      {Get 256 gain samples}
   input := ((ymsb[0] and $0F)*256) + ylsb[0];        {Calc samlpe value}
   ypoint := 1/factor * (input - output[0]);          {Ratio}
   ytemp := y[0];                                     {Save orig y position}
   x[0] :=  xleft;                                    {Calc 1st x and }
   y[0] := round(zeropoint + ypoint * scaley);        {           y positions}
   nx := 1;
   repeat
     setcolor(0);                                     {ie. blank}
     moveto(x[nx-1], ytemp);                          {Move to old x,y position}
     lineto(x[nx], y[nx]);                            {Delete previous line}
     moveto(x[nx-1], y[nx-1]);                        {Move back to new position}
     ytemp := y[nx];                                  {Save old y position}
     input := ((ymsb[nx] and $0F)*256) + ylsb[nx];    {Calc sample value}
     ypoint := 1/factor * (input - output[nx]);
     x[nx] := round(nx * scalex + xleft);             {Calc next x and }
     y[nx] := round(zeropoint + ypoint * scaley);     {           y positions}
     setcolor(15);                                    {Colour back on}
     lineto(x[nx], y[nx]);                            {Draw line to new position}
     nx := nx + 1;
```

```
    {text}
    SetTextStyle(2, 0, 5);
    SetTextJustify(1, 1);
    OutTextXY(360, 6, 'GROUP DELAY');
    OuttextXY(58, 44, '1');
    OuttextXY(58, 69, '0.9');
    OuttextXY(58, 94, '0.8');
    OuttextXY(58, 119, '0.7');
    OuttextXY(58, 144, '0.6');
    OuttextXY(58, 169, '0.5');
    OuttextXY(58, 194, '0.4');
    OuttextXY(58, 219, '0.3');
    OuttextXY(58, 244, '0.2');
    OuttextXY(58, 269, '0.1');
    OuttextXY(58, 294, '0');
    Setviewport(25, 155, 35, 165, false);
    moveto(0, 10);
    lineto(3, 0);
    lineto(4, 4);
    lineto(6, 6);                                      {Draw a "µ" sign!}
    lineto(8, 4);
    lineto(10, 0);
    lineto(10, 5);
    setviewport(0, 0, 719, 347, false);
    OuttextXY(40, 156, 's');
    OuttextXY(75, 300, '50');
    OuttextXY(225, 300, '60');
    OuttextXY(375, 300, '70');
    OuttextXY(525, 300, '80');
    OuttextXY(675, 300, '90');
    OuttextXY(300, 303, 'MHz');
    OutTextXY(350, 340, '<ESC> TO EXIT');
    screen := ImageSize(0, 0, 719, 347);                   {Save screen}
    GetMem(outline, screen);
    GetImage(0,0,719,347,outline^);                        {to memory}
  end;

{----------------------------------------------------------------------------}

 procedure draw_phase;

 const
  factor = 52;

 var
  x, y: array[0..999] of integer;
  refresh, i, nx, ytemp, input: integer;
  ratio, ypoint: real;
  answer: char;
 begin
  for i := 0 to max do
   begin
    x[i] := 0;                              {Initialize array of points to 0}
    y[i] := 0;
   end;

    {Plot first set}
    AD_sample(2);
    phase[0] := ((ymsb[0] and $0F)*256) + ylsb[0]; {1st phase from A/D sample}
    x[0] := xleft;
    ypoint := 0.2 - phase[0]/4095;                 {Calc 1st group delay point}
    if ypoint < -0.02 then ypoint := 0.97 + ypoint;
    if invert[0] = 1 then ypoint := frac(ypoint + 0.5); {Correct for inversion}
    y[0] := round(zeropoint + ypoint * scaley);

    moveto(x[0], y[0]);
```

```
  nx := 1;
  repeat
    phase[nx] := ((ymsb[nx] and $0F)*256) + ylsb[nx];  {Get measured phase}
    if abs(phase[nx] - phase[nx - 1]) > 100 then phase[nx] := phase[nx-1];
                                                   {Disallow rapid transitions}
    ypoint := 0.2 - phase[nx]/4095;         {Calc group delay point correcting}
    if ypoint < -0.02 then ypoint := 0.97 + ypoint;    {for non-linearity}
    if invert[nx] = 1 then ypoint := frac(ypoint + 0.5); {Corr for inversion}
    x[nx] := round(nx * scalex + xleft);
    y[nx] := round(zeropoint + ypoint * scaley);
    setcolor(15);
    lineto(x[nx], y[nx]);
    nx := nx + 1;
  until nx = max;                                  {Until 256 points plotted}
  answer := #3;
  if keypressed then
   begin                                           {Check for ESC}
    answer := readkey;
    if answer = #27 then
     begin
      closegraph;
      freemem(outline, screen);
      exit;                                        {Free memory on exiting}
     end;
   end;

{Plot subsequent sets}
 refresh := 0;
 repeat
 if refresh = 10 then
  begin
   PutImage(0,0,outline^, Orput);                        {Refresh screen}
   refresh := 0;
  end; {if}
  AD_sample(2);                                        {Get 256 phase samples}
  phase[0] := ((ymsb[0] and $0F)*256) + ylsb[0];       {Calc 1st phase value}
  ypoint := 0.2 - phase[0]/4095;                       {Calc group delay point}
  if ypoint < -0.02 then ypoint := 0.97 + ypoint;
  if invert[0] = 1 then ypoint := frac(ypoint + 0.5); {Corr for inversion}
  ytemp := y[0];
  x[0] :=  xleft;
  y[0] := round(zeropoint + ypoint * scaley);
  moveto(x[0], y[0]);
  nx := 1;
  repeat
    phase[nx] := ((ymsb[nx] and $0F)*256) + ylsb[nx];   {Get measured phase}
    setcolor(0);                                    {ie. blank}
    moveto(x[nx-1], ytemp);                         {Move to old x,y position}
    lineto(x[nx], y[nx]);                           {Delete previous line}
    moveto(x[nx-1], y[nx-1]);                       {Move back to new position}
    ytemp := y[nx];
    ypoint := 0.2 - phase[nx]/4095;         {Calc group delay point correcting}
    if ypoint < -0.02 then ypoint := 0.97 + ypoint;          {non-linearities}
    if invert[nx] = 1 then ypoint := frac(ypoint + 0.5); {Corr for inversion}
    x[nx] := round(nx * scalex + xleft);                      {Calc next x and }
    y[nx] := round(zeropoint + ypoint * scaley);              {     y positions}
    setcolor(15);                                               {Colour back on}
    lineto(x[nx], y[nx]);                           {Draw line to new position}
    nx := nx + 1;
   until nx = max;                                   {Until 256 points plotted}
   refresh := refresh + 1;
   if keypressed then
    begin
     answer := readkey;
    end;
```

```
  until answer = #27;                                    {Until ESC pushed}
  closegraph;
  freemem(outline, screen);
 end;

{----------------------------------------------------------------------------

Procedure single_gain;
{Procedure to plot single sweep of gain measurements}

var
  x, y: array[0..999] of integer;
  i, nx: integer;
  ratio, ypoint: real;
  answer: char;

 begin
  for i := 0 to max do
   begin
    x[i] := 0;                                   {Initialize array of points to 0}
    y[i] := 0;
   end;

   repeat
    ypoint := 1/factor * (gain[0] - output[0]);           {Calc ratio}
    x[0] := xleft;                                        {Calc 1st x and}
    y[0] := round(zeropoint + ypoint * scaley);           {     y positions}
    moveto(x[0], y[0]);                                   {Move there}
    nx := 1;
    repeat
      ypoint := 1/factor *  (gain[nx] - output[nx]);
      x[nx] := round(nx * scalex + xleft);                {Calc subsequent x }
      y[nx] := round(zeropoint + ypoint * scaley);        {    and y positions}
      lineto(x[nx], y[nx]);                               {Draw line to them}
      nx := nx + 1;
    until nx = max;                                      {Until 256 points plotted}
    answer := readkey;
    if answer = #27 then
       begin
        closegraph;
        freemem(outline, screen);
        exit;
       end;
       if answer = #32 then gain_scale;
   until answer <> #32;                                   {Change scale if required}
 end;

{---------------------------------------------------------------------------}

Procedure single_phase;
{Procedure to plot single sweep of phase measurements}

var
  x, y: array[0..999] of integer;
  i, nx: integer;
  ratio, ypoint: real;
  answer: char;
 begin
  for i := 0 to max do
   begin
    x[i] := 0;
    y[i] := 0;
   end;

    ypoint := 0.2 - phase[0]/4095;                      {Calc 1st group delay point}
    if ypoint < -0.02 then ypoint := 0.97 + ypoint;
```

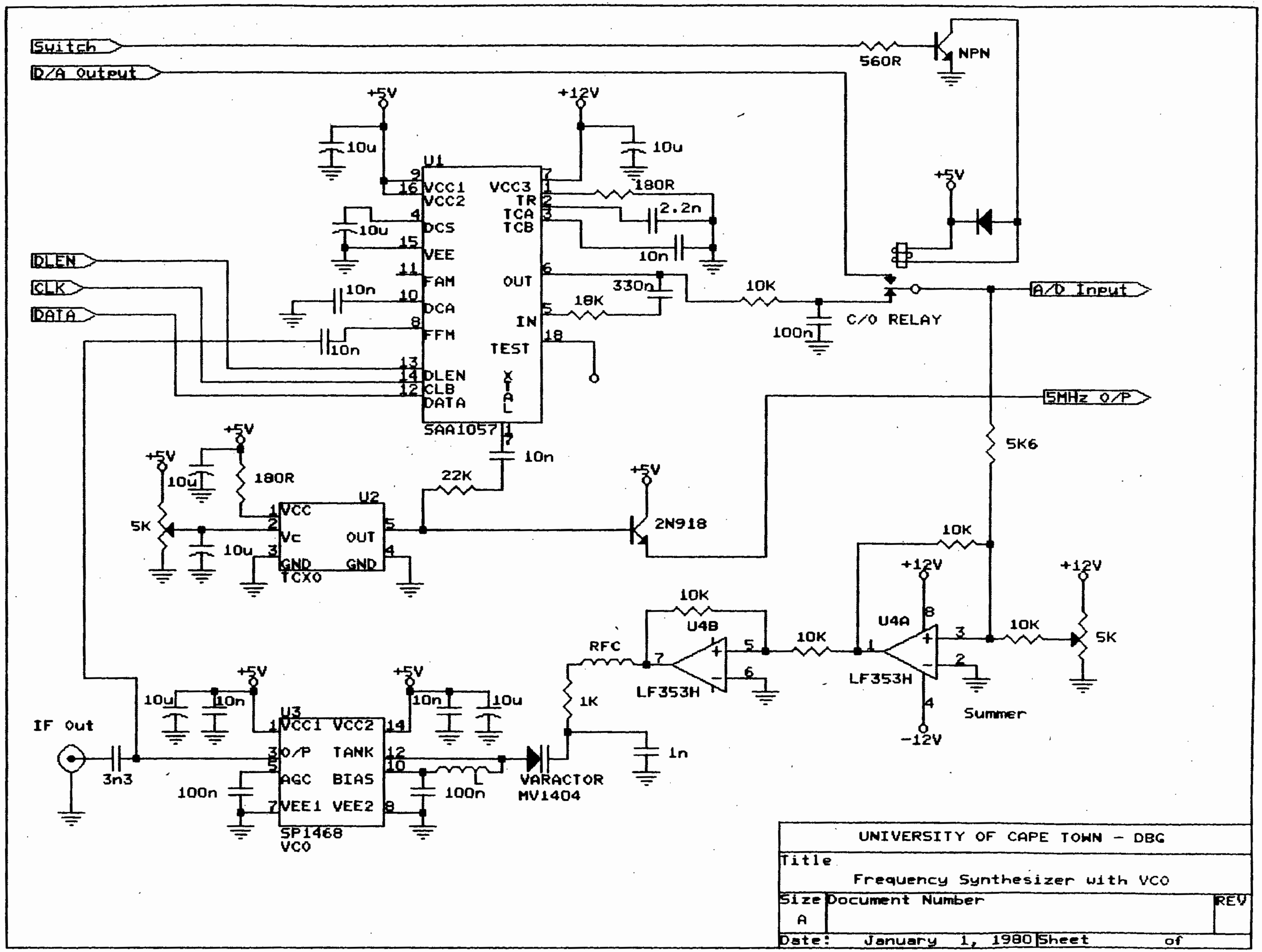
```
   .if invert[0] = 1 then ypoint := frac(ypoint + 0.5); {Corr for inversion}
    x[0] := xleft;                                     {Calc 1st x and}
    y[0] := round(zeropoint + ypoint * scaley);        {      y positions}
    moveto(x[0], y[0]);                                      {Move there}
    nx := 1;
    repeat
      ypoint := 0.2 - phase[nx]/4095;                          {Calc group delay point
      if ypoint < -0.02 then ypoint := 0.97 + ypoint;   {and correct}
      if invert[nx] = 1 then ypoint := frac(ypoint + 0.5); {Corr for inversion}
      x[nx] := round(nx * scalex + xleft);                     {Calc subsequent x }
      y[nx] := round(zeropoint + ypoint * scaley)  ;           {        and y positions
      lineto(x[nx], y[nx]);                                    {Draw line to them}
      nx := nx + 1;
    until nx = max;                                          {Until 256 points plotted
    repeat until readkey = #27;
    closegraph;
    freemem(outline, screen);                                {Free memory on exiting}
 end;

{-------------------------------------------------------------------------------}

Procedure Single_menu;

{Menu for single sweep: plot group delay or gain}

 var
  i: integer;
  choice: char;
  outf:text;

 begin
  repeat
   clrscr;
   gotoxy(24, 13);
   write('<P> for group delay measurement');
   gotoxy(24, 15);
   write('<G> for gain measurement');
   gotoxy(33, 23);
   writeln('<ESC> to exit');
   gotoxy(80, 25);
   choice := readkey;
   case choice of
    #71, #103: begin
                gain_parameters;
                gain_graph;
                single_gain;
               end;
    #80, #112:begin
               phase_parameters;
               phase_graph;
               single_phase;
              end;
   end;  {Case}
 until choice = #27;         {Escape}
end;

{-------------------------------------------------------------------------------}

Procedure Menu;

{Main menu: continuous group delay or gain or single sweep}

 var
  choice: char;
 begin
  repeat
```

```
   clrscr;
   gotoxy(23, 13);
   write('<P> for continuous group delay measurement');
   gotoxy(23, 15);
   write('<G> for continuous gain measurement');
   gotoxy(23, 17);
   write('<S> for single sweep');
   gotoxy(33, 23);
   writeln('<ESC> to exit');
   gotoxy(80, 25);
   choice := readkey;
   case choice of
    #71, #103: begin
                gain_parameters;
                gain_graph;
                draw_gain;
               end;
    #80, #112:begin
               phase_parameters;
               phase_graph;
               draw_phase;
              end;
    #83, #115:begin
               clrscr;
               write('Sampling...');
               single_sample;
               single_menu;
              end;
   end;  {Case}
 until choice = #27;                  {Escape}
end;
{-----------------------------------------------------------------------------}

{*** MAIN PROGRAM ***}

begin
 port[$703] := $92;                     {Initialize A/D ports}
 repeat
  clrscr;
  gotoxy(24, 2);
  highvideo;
  writeln('┌───────────────────────────┐'); gotoxy(24, 3);
  writeln('│ P A T H   A N A L Y Z E R │'); gotoxy(24, 4);
  writeln('└───────────────────────────┘');
  normvideo;
  gotoxy(24, 13);
  write('<I> to initialize system');
  gotoxy(24, 15);
  write('<P> for previous initialization');
  gotoxy(33, 23);
  write('<ESC> to exit');
  gotoxy(80, 25);
  opt := readkey;
  case opt of
     #73, #105: begin
                 freq_synth;
                 menu;
                end;
     #80, #112: menu;
    end;    {case}
 until opt = #27;               {Exit}
 clrscr;
end.
```

APPENDIX E

CIRCUIT DIAGRAMS

The circuit diagrams of all the circuitry developed for the Path Analyzer are given in this Appendix.



UNIVERSITY OF CAPE TOWN – DBG

Title

Frequency Synthesizer with VCO

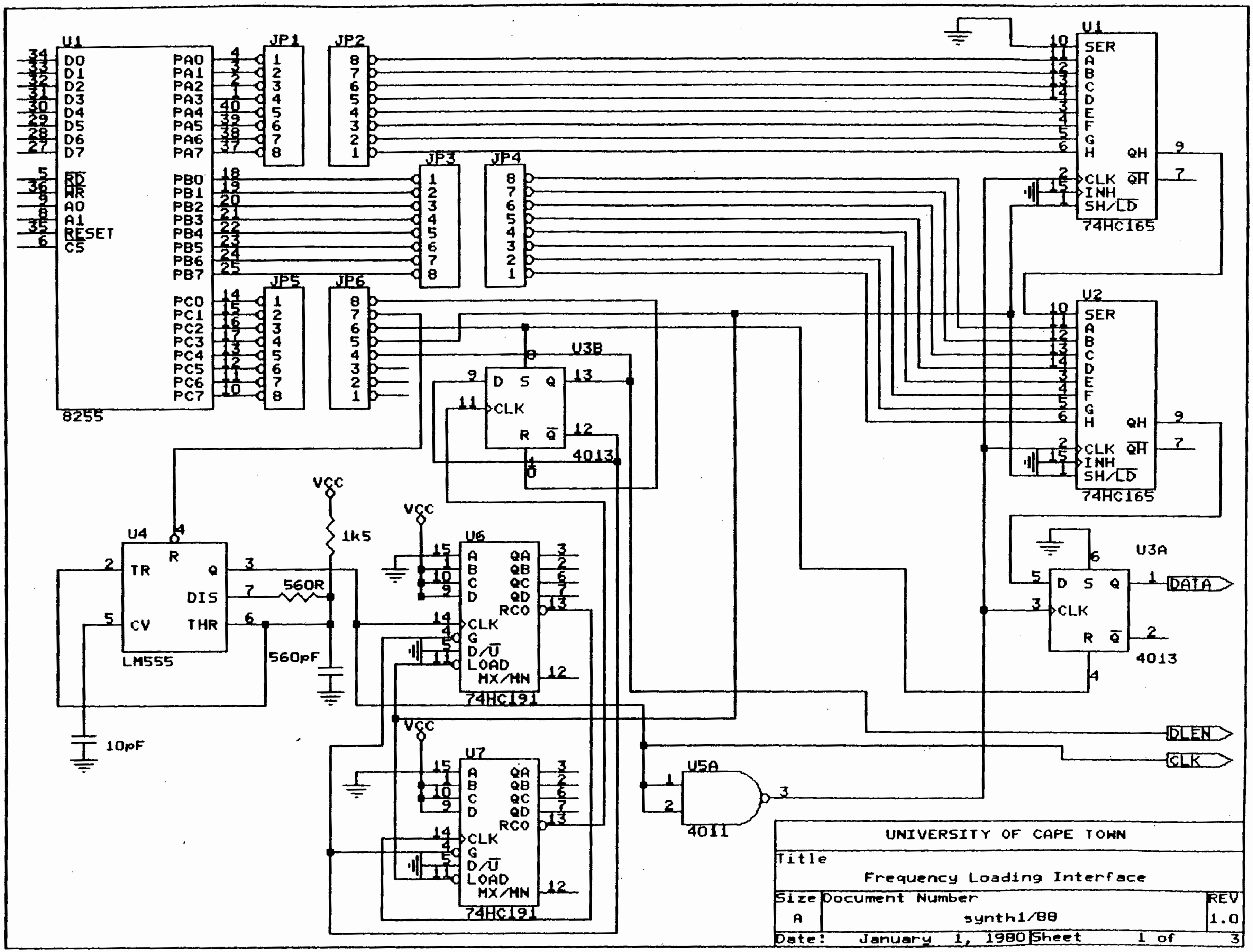
Size A

Document Number

REV

Date: January 1, 1980

Sheet of



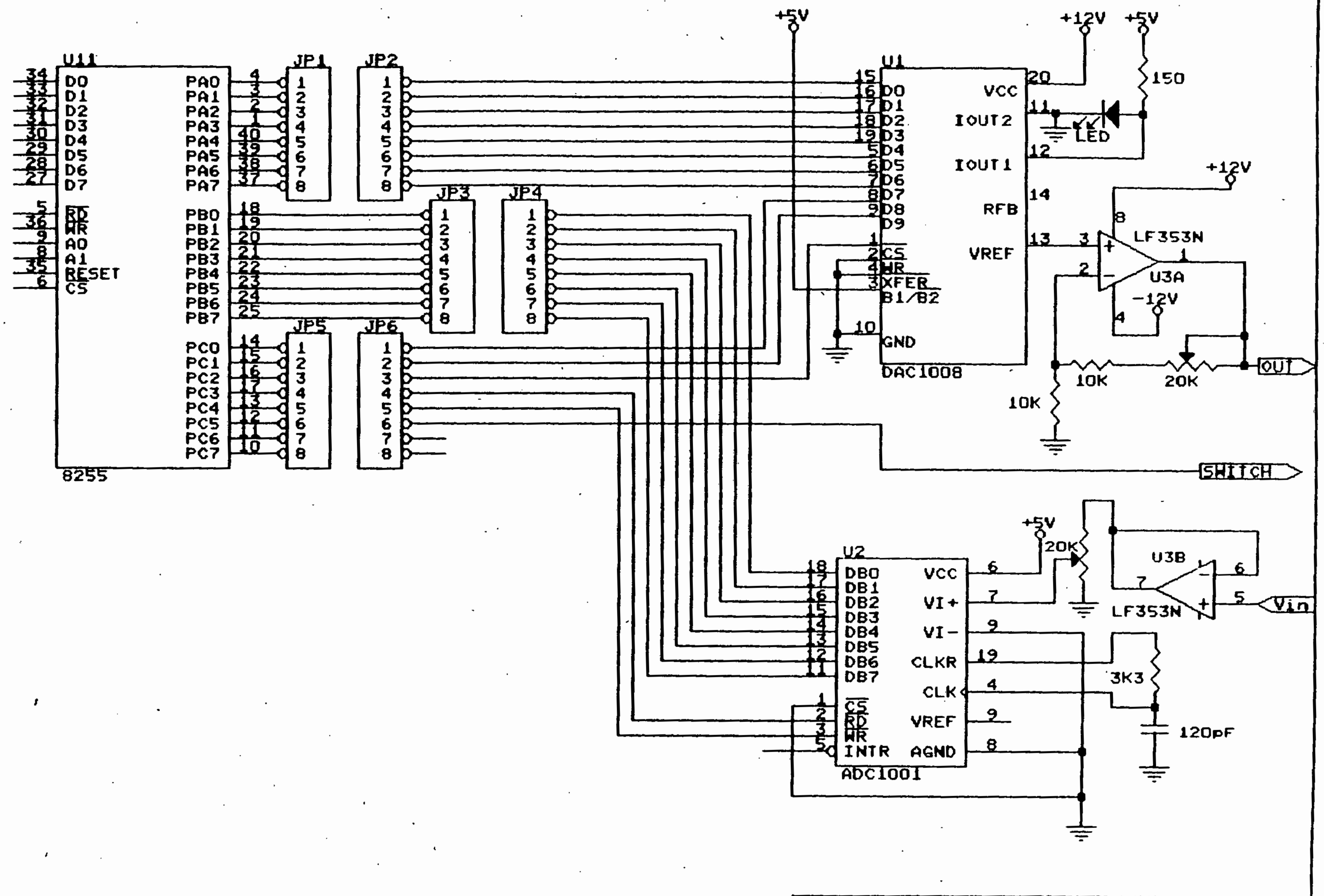
UNIVERSITY OF CAPE TOWN

Title

Frequency Loading Interface

Size	Document Number	REV
A	synth1/88	1.0

Date: January 1, 1980 Sheet 1 of 3



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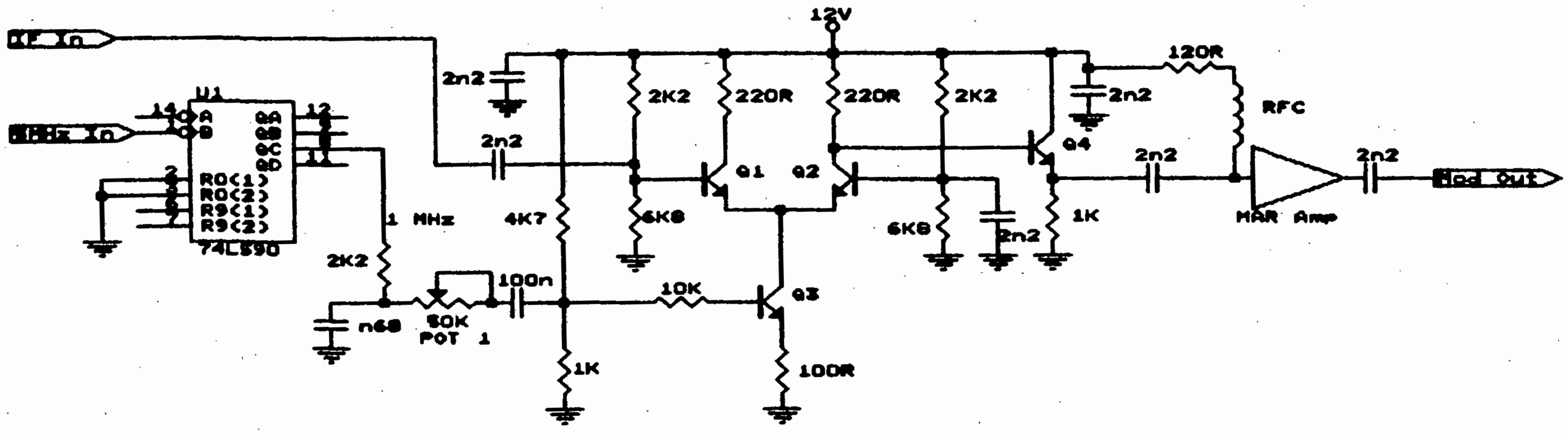
Title

A/D and D/A Interface

Size	Document Number	REV
A	Synth2/88	1.0

Date: January 1, 1980 Sheet 2 of 3



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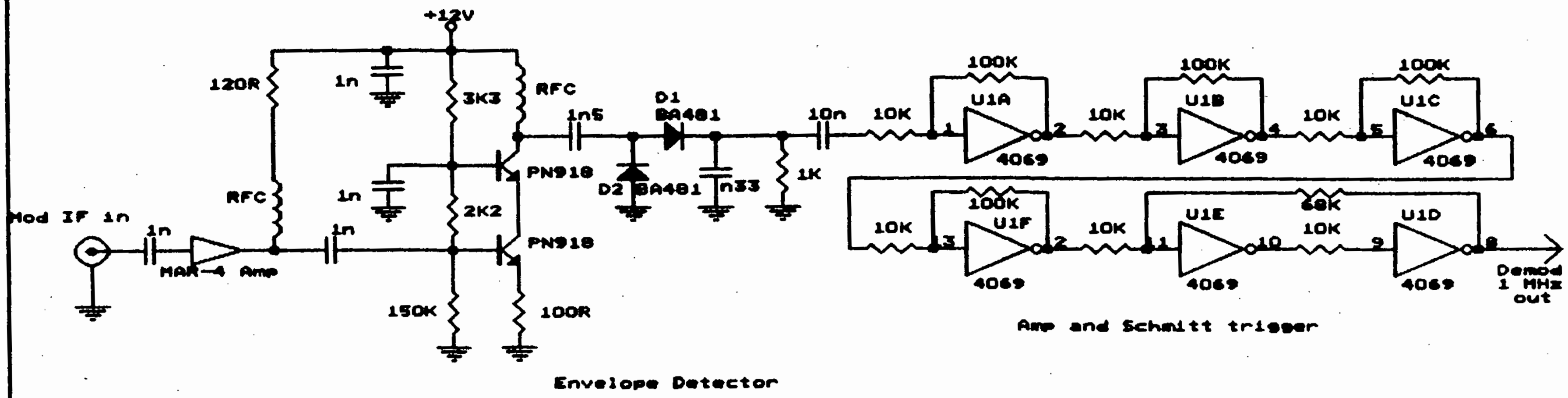

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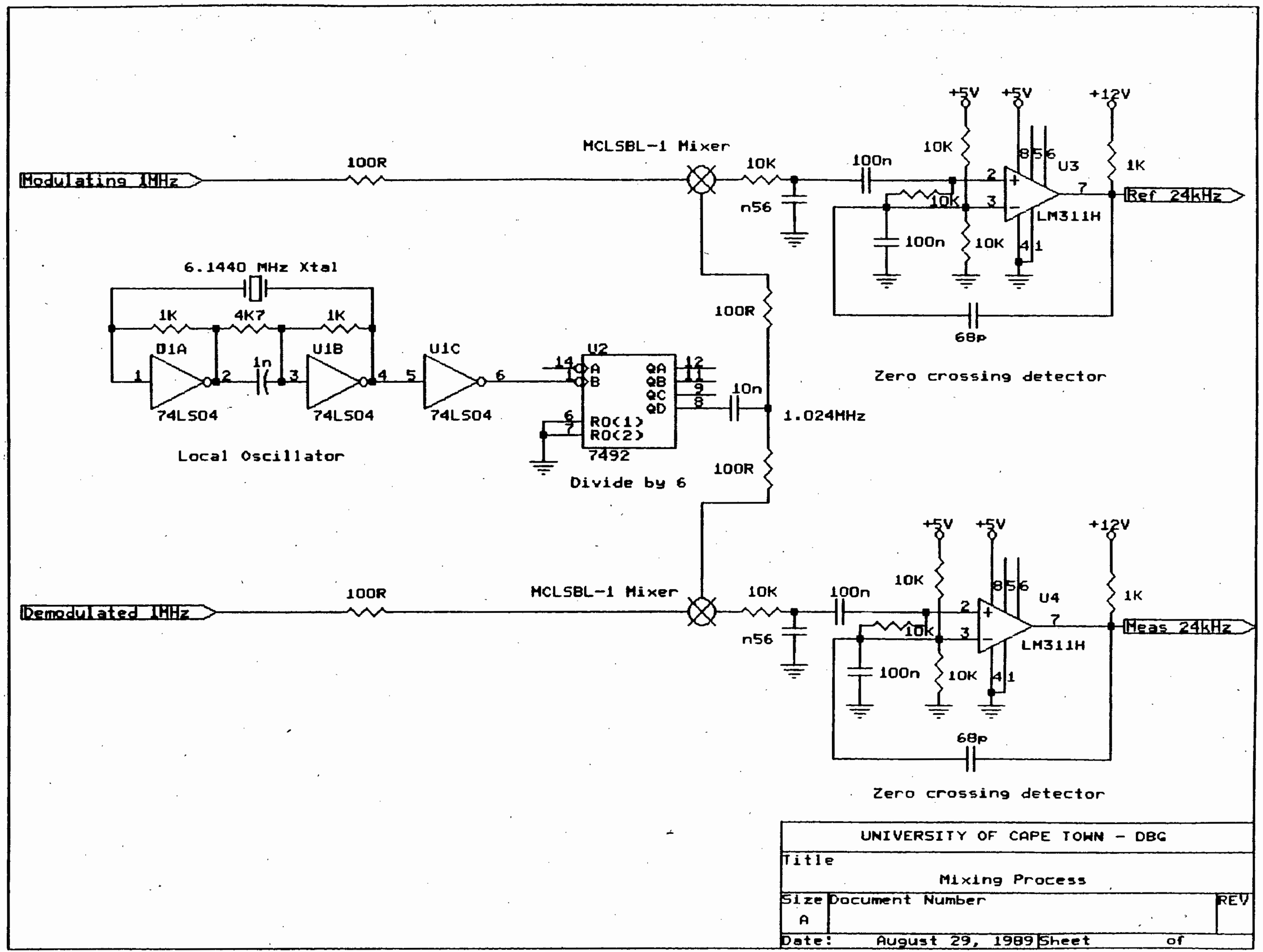

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Mixing Process

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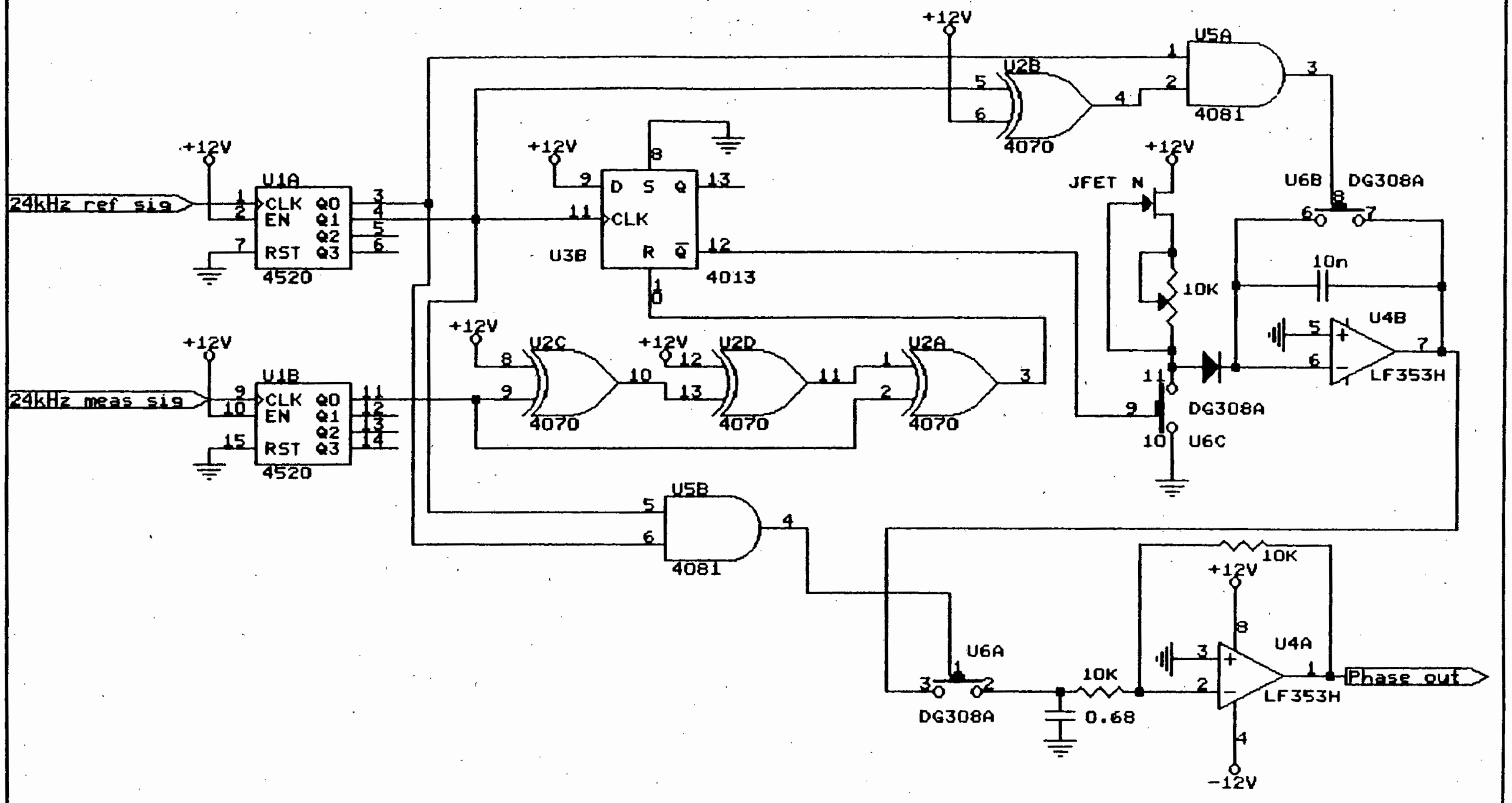

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Title

PHASE COMPARATOR

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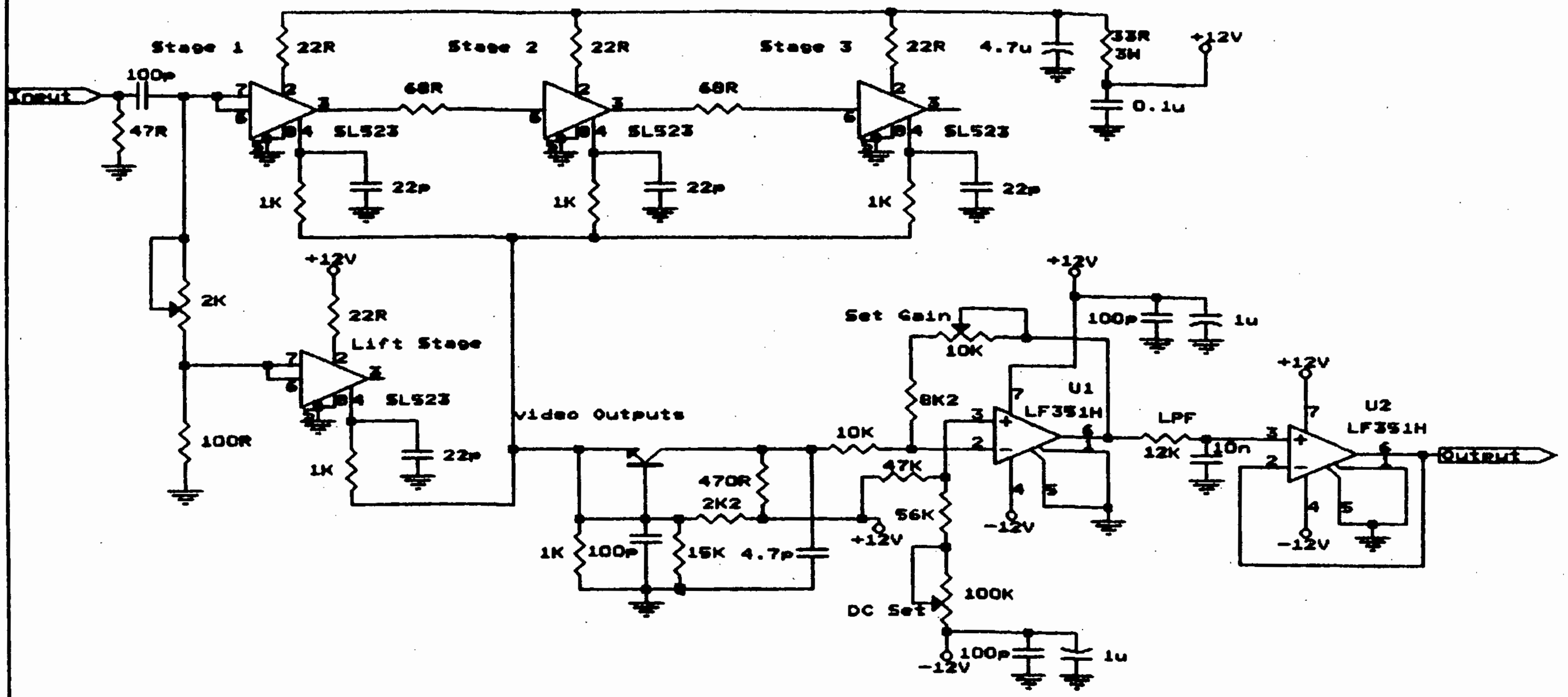

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Title

Logarithmic Amplitude Detector

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APPENDIX F

DATA SHEETS

The data sheets for the following devices are included in this Appendix:

SAA1057	Frequency Synthesizer
SP1648	Voltage Controlled Oscillator

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}		3,6 to 12	V
	V_{CC2}		3,6 to 12	V
	V_{CC3}		V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ.	18	mA
	I_{CC3}	typ.	0,8	mA
Input frequency ranges				
at pin FAM	f_{FAM}		512 kHz to 32	MHz
at pin FFM	f_{FFM}		70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	>	4	MHz
Operating ambient temperature range	T_{amb}		−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

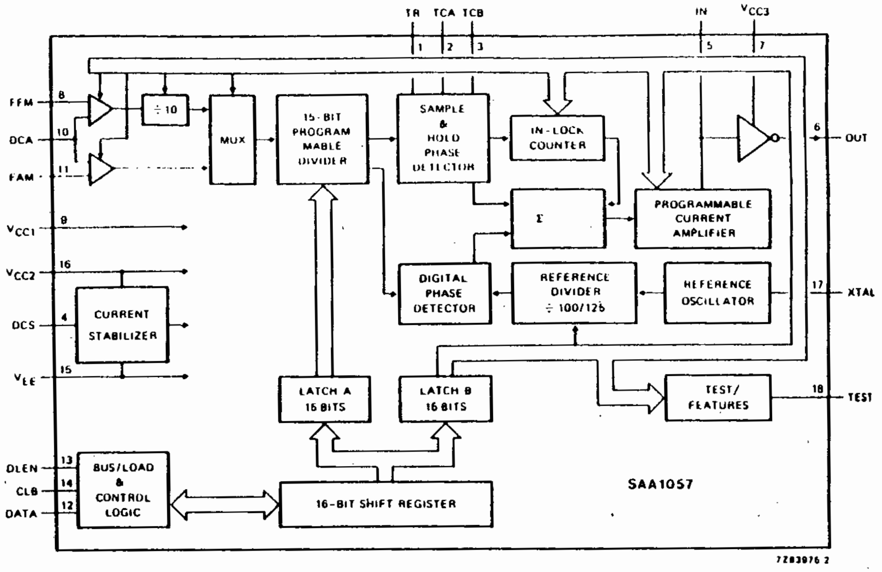


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divid (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM	FM/AM selection; '1' = FM, '0' = AM
REFH	reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)
CP3 CP2 CP1 CP0	control bits for the programmable current amplifier (see section Characteristics)
SB2	enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically
SLA	load mode of latch A; '1' = synchronous, '0' = asynchronous
PDM1 PDM0	phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM	bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on
T3	test bit; must be programmed always '0'
T2	test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin
T1	test bit; must be programmed always '0'
T0	test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

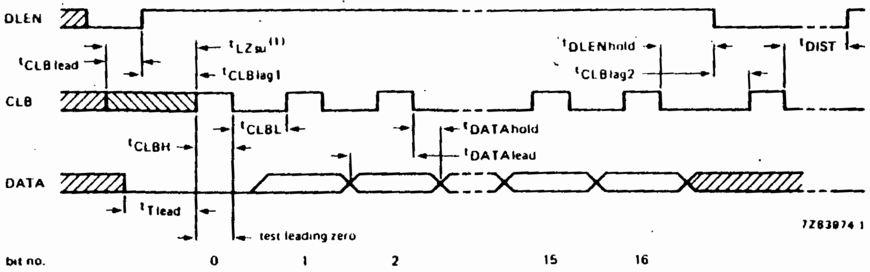


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines.

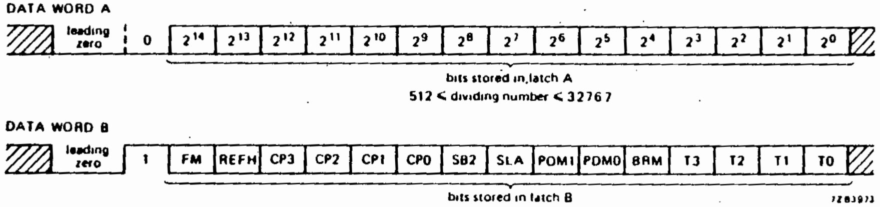


Fig. 3 Bit organization of data words A and B.

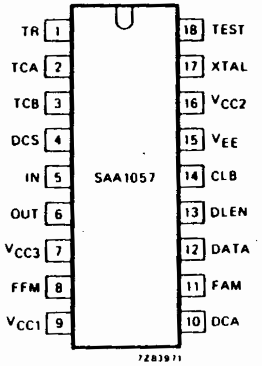


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	I_{tot} = I_{CC1} + I_{CC2} in-lock: BRM = '1'; PDM = '0' I_{OUT} = 0
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	
Operating ambient temperature	T_{amb}	−25	–	+ 80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\,(rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\,(rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	µA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	µA	V_{IH} = 2,4 V

---

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.	conditions
BUS inputs timing (DLEN, CLB, DATA)					see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	– μs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	– μs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	– μs	
CLB pulse width HIGH	t_{CLBH}	5	–	– μs	
CLB pulse width LOW	t_{CLBL}	5	–	– μs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	– μs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	– μs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	– μs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	– μs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	– μs	next transmission after word ‘B’ to other device or
Busy time					
asynchronous mode	t_{DIST}	0,3	–	– ms	next transmission to SAA1057 after word ‘A’ (see also note 5)
synchronous mode	t_{DIST}	1,3	–	– ms	
Sample and hold circuit (TR, TCA, TCB)					see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	– V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7 V	
Capacitance at TCA (external)	C_{TCA} C_{TCA}	– –	– –	2,2 nF 2,7 nF	REFH = ‘1’ REFH = ‘0’
Discharge time at TCA	t_{dis} t_{dis}	– –	– –	5 μs 6,25 μs	REFH = ‘1’ REFH = ‘0’
Resistance at TR	R_{TR}	100	–	– Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	– V	
Capacitance at TCB	C_{TCB}	–	–	10 nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10 nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.	conditions
Programmable current amplifier (PCA)					
Output current of the dig. phase detector	± I_{dig}	–	0,4	– mA	
Current gain of PCA					
CP3 CP2 CP1 CP0					
P1 0 0 0 0	G_{P1}	–	0,023	–	V_{CC2} ⩾ 5 V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–	
P3 0 0 1 0	G_{P3}	–	0,23	–	
P4 0 1 1 0	G_{P4}	–	0,7	–	
P5 1 1 1 0	G_{P5}	–	2,3	–	
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	– μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1 V	in-lock
Output amplifier (IN,OUT)					
Input voltage	V_{IN}	–	1,3	– V	in-lock; equal to internal reference voltage
Output voltages					
minimum	V_{OUT}	–	–	0,5 V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	– V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	– V	I_{OUT} = 0,1 mA
Maximum output current	± I_{OUT}	5	–	– mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*					
Output voltage LOW	V_{TL}	–	–	0,5 V	
Output voltage HIGH	V_{TH}	–	–	12 V	
Output current OFF	I_{Toff}	–	–	10 μA	V_{TH}
Output current ON	I_{Ton}	150	–	– μA	V_{TL}
Ripple rejection**					
at f_{ripple} = 100 Hz					
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	– dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	– dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	– dB	V_{OUT} ⩽ V_{CC3}–3 V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

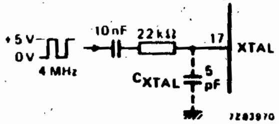


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

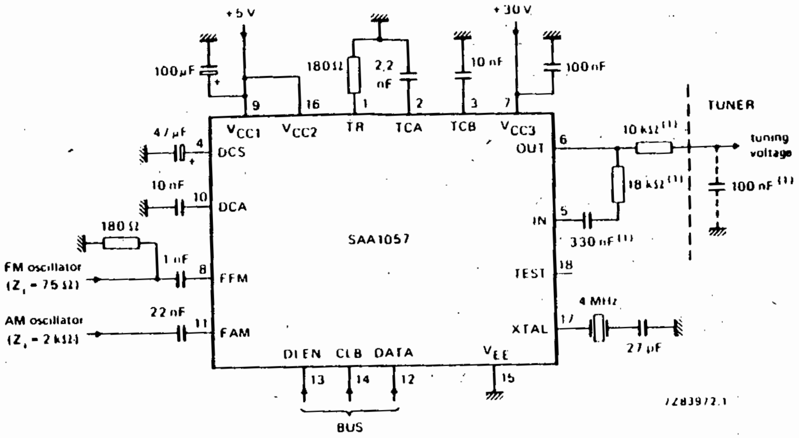
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

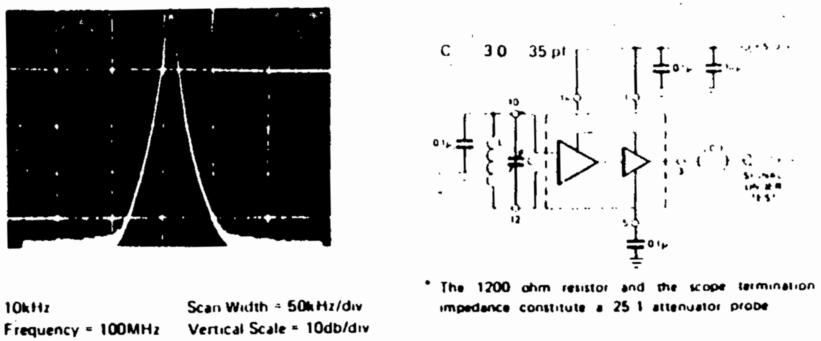
Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning ◄— voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

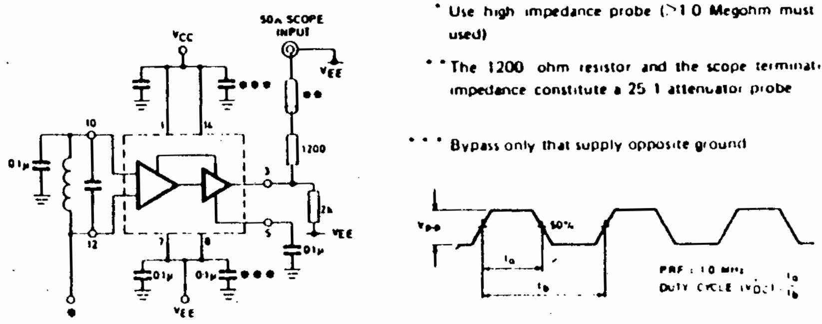


B.W. = 10kHz
Center Frequency = 100MHz

Scan Width = 50kHz/div
Vertical Scale = 10db/div

* The 1200 ohm resistor and the scope termination impedance constitute a 25 1 attenuator probe

Fig 3 Spectral purity of signal at output



* Use high impedance probe (>1.0 Megohm must be used)

** The 1200 ohm resistor and the scope termination impedance constitute a 25 1 attenuator probe

*** Bypass only that supply opposite ground

Fig 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648 The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8 An automatic gain control (AGC) is incorporated to limit the current through the emitter coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3 TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer Figure 3 indicates the high spectral purity of the oscillator output (pin 3)

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} (≈ 1.4 V for positive supply operation)

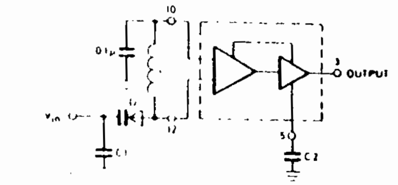
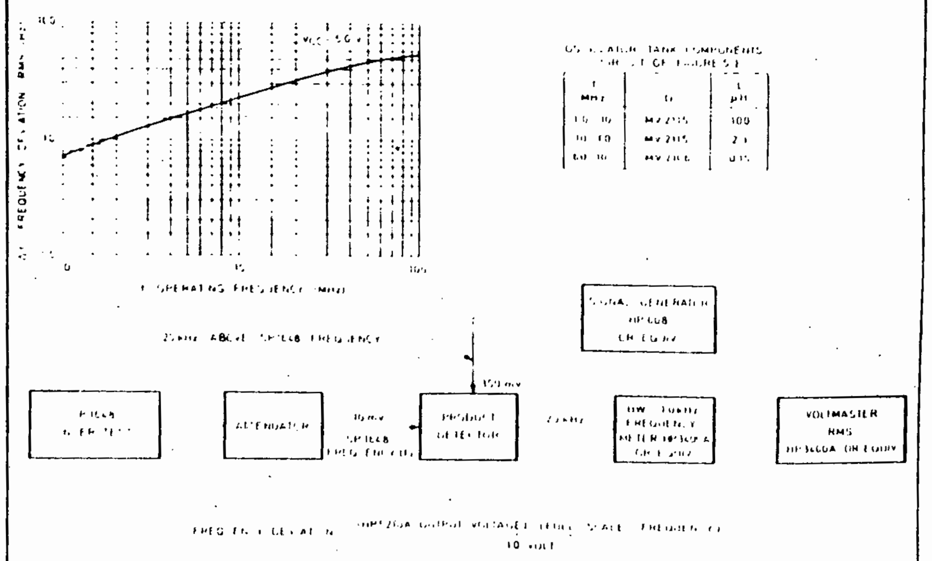


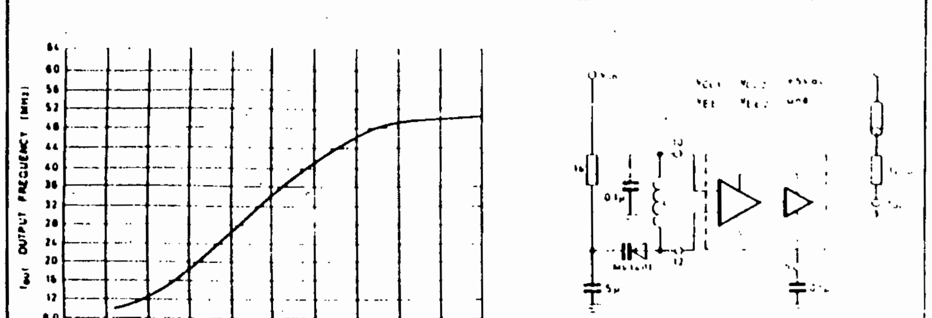
Fig 5 The SP1648 operating in the voltage controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise This variation is plotted versus operating frequency in Figure 6



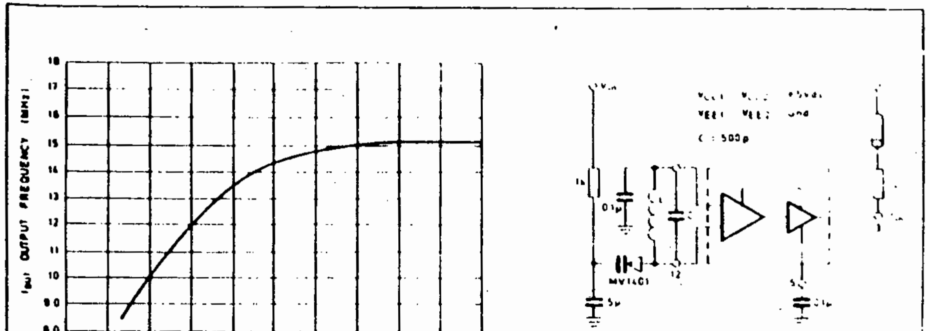
Note Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing

Fig 6 Frequency deviation test circuit



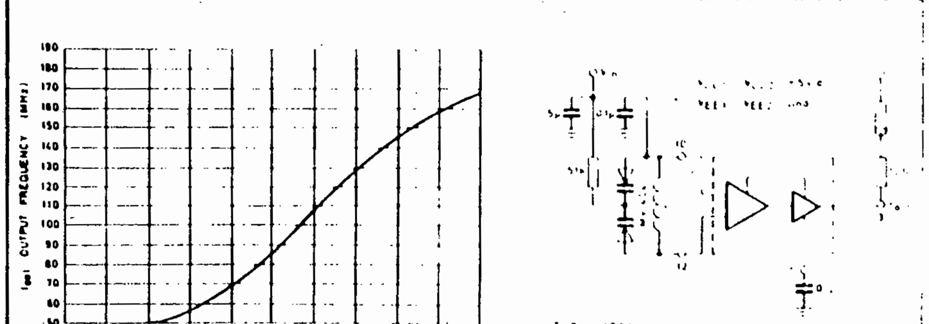
* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe

Fig. 7



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe

Fig. 8



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

$$\text{where } f_{min} = \frac{1}{2^{\pi}\sqrt{L}\,(C_D(max) + C_S)}$$

C_S = shunt capacitance (input plus external capacitance)

C_D = varactor capacitance as a function of bias voltage

Good RF and low frequency by passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1µF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used, at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak to peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used).