

University Of Cape Town.

Department of Electrical Engineering

DIRECT DIGITAL CONTROL OF THYRISTOR NETWORKS

"An Investigation Into the On-Line Control of Thyristor Networks

By Means of a Small Digital Computer."

A Thesis submitted in fulfilment of the requirements
for the degree of Master of Science (Engineering),
at the University of Cape Town.

by

Michael G.Rodd, B.Sc.(Eng)(Cape Town).

30th September, 1970.

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Finally, he wishes to thank his wife for the many hours which she has spent on the preparation of this thesis.

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Introduction.

This thesis is an investigation into the applications of a digital computer ^{to} in the on-line control of thyristor networks. This will involve producing hardware and software to determine firing sequences, firing delays, etc., and to execute the firing instructions. These are to be determined by the computer from the initial instructions and information fed back from the system, correlated with information in the memory. The ultimate aim is geared towards the control of induction motors, based on research work at present being carried out under Professor N.C. Enslin, at the University of Cape Town, on the speed control of induction motors by thyristor networks.

The steps involved are:-

(i) The design and construction of an interface with up to 36 output lines, each of which is independently addressable through a single computer word. On execution of the selected instruction word, the line (normally held logically false) determined by the address held in that particular instruction word, will become true, and will remain true for a period determined by the computer. X

(ii) The development of a suitable firing circuit, which will (a) fire the thyristor when the line from the computer is set true, and (b) isolate the computer from the power circuitry being driven.

(iii) The design and construction of a simple controller to set up initial conditions.

(iv) The development of suitable software to run various configurations of thyristors, and to be under the control of the initial instructions, as well as responding to information being obtained from the system it is driving, i.e. to be truly on-line. X

The approach adopted is to develop a simple, single-phase system which will embody most of the principles involved in the multi-thyristor networks. After this, a three-phase system is constructed, to consist of a bridge-connected rectifier whose output is voltage regulated. This system is used to drive a separately-excited D.C. machine. The computer is used as a feedback speed-controller.

The next stage is to lay the groundwork for the computer control of a 36-thyristor network used to control the speed of an induction motor. The development of this system is being carried out in the Department of Electrical Engineering. The principle behind applying the computer to the network is so that various modes of operation may be explored. This thesis outlines the basic software required, and some of the initial results are given.

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CHAPTER I

THE INTERFACE BETWEEN THE COMPUTER AND THE SYSTEM.

The most important development required in order to implement direct digital control of thyristors, using an on-line computer, is obviously the design and construction of an interface (i.e., a network permitting communication between two seemingly incompatible systems) in order that the computer's hardware may be used to provide the necessary pulses to fire the thyristors. One solution is the use of a Digital-to-Analogue Converter, but on two counts this is not feasible. (a) Speed - the conversion rate is not particularly fast, in the order of 6 microseconds for the converter available, and (b) eventually up to 36 channels will be required. This implies either 36 Digital-to-Analogue units, or one Digital-to-Analogue unit plus a 36-channel multiplexer, both of which are extremely costly.

The answer appears to lie in the utilization of a facility available on most small computers - the "external control system". This system decodes a special machine-code instruction and places part of the instruction word on to the output bus (E-Bus) of the computer. The section placed on the output bus may be of any specific code, which may then be decoded to form varying addresses. Thus, on the execution of one instruction, one pulse may be produced which may then be transferred to an external device. Thus, every 1.8 microseconds (the cycle-time of the computer used) such a pulse is produced on any unique line. This is obviously an economical and fast method to employ.

The Varian Data 620/i has such a facility. This makes available a pulse on the E-Bus when the 'EXC' (or 'SEL') instruction is executed. (These ^{are} ~~or~~ the mnemonic formats which form part of the assembler system for the Varian computer - see Appendix I) The format of the instruction is 1OKXY, and is a single-word instruction. There are two EXC instructions available, EXC and EXCB. These are distinguished by K=0 for EXC and K=4 for EXCB. The YY is the basic address of the device into which the EXC is feeding, and the X may be further decoded to make a one-in-eight channel selection. One can thus design an interface which will produce one-in-sixteen possible lines for each address group. The choice of address is limited to 0 - 77, and must not clash with any of the standard peripherals, each of which has its own address.

1.1 Pulse Production and Timing. See Fig No 1(e)

The EXC command causes the function code (Bits 6-8) and the device address (Bits 0-5) to be placed on the E-Bus. The EXC interface decodes the code, and when the FRYX line goes from true-to-false, the decoded signal is fed to the required device. In this case, it sets a flip-flop which is connected to the firing circuit of a thyristor, i.e. one instruction can fire one thyristor.

1.2 Address Decoding. See Fig No 1(a)

The device addresses used were 54, 56 and 57. All lines of the E-Bus must be supplied with a line-receiver in order to lower the drain on the E-Bus, and the lines on the E-Bus are in complement form (i.e. -0, -2, -3....etc.), so it is convenient to use normal integratedcircuit inverters as line receivers through-

out. The three addresses 54, 56 and 57 are decoded using NAND gates as shown. In each case the "5" is common, and this is combined with the decoded bits 0, 1 and 2 as shown, remembering that the bits are numbered from right to left. As DTL logic is being used, the "wired-AND" feature of this logic-family can be used to reduce the number of integrated circuits. Note that the decoded addresses are 54^+ , 56^+ , and 57^+ , i.e. not negated.

1.3 Gating Between EXC and EXCB. See Fig No 1 (b)

In order to produce twice the number of addresses available, the addresses 54, 56 and 57 are gated with $EB11^-$ (which is true for EXC) and $EB15^-$ (which is true for EXCB). These are also gated with $FRYX^-$, as this pulse is generated by the computer to indicate that there is an address and control code on the E-Bus. Again, NAND gates are employed to do the decoding, as shown.

1.4 Decoding Of Bits 6, 7 and 8. See Fig No 1(c)

For each EXC, 8 further channels can be selected via bits 6 - 8. So a one-in-eight decoder must be designed. This is then repeated four times and in each case gated with 54, 54B, 56, 56B, 57 or 57B to produce 36 channels. The decoder is the normal NAND-type decoder. Four-input NAND gates are deliberately used, so as to include the gating with 54, 56 and 57, etc. Note that on the present design, only 56 and 57 are fully decoded, these yielding 32 lines, so 54 only needs to yield four lines in order that 36 lines may be obtained.

1.5 Flip-Flops. See Fig No 1(d)

There are thus thirty-six channels available. These signals are used to set and reset a series of flip-flops. Using D-type, edge-triggered flip-flops, the EXC pulse is used in each case to set a flip-flop, and the corresponding B-pulse to reset it. Since these pulses can never be produced simultaneously, this method reduces the number of flip-flops needed. Note that all the clock inputs to the flip-flops are tied together, and fed with the system reset pulse from the computer to initialize all flip-flops. To ensure this condition, the inputs are tied to ground throughout. Note: To reset all flip-flops, a buffer NAND gate, which has the necessary fan-out, is used and fed by the system's reset pulse, SYRT⁻, which is controlled by a switch on the console of the computer.

1.6 Choice of Integrated Circuits and Design

Implementation. See Fig No 1(f).

As this is a relatively simple and straightforward design, the techniques used are fairly rule-of-thumb, and a bit of juggling is required to reduce the number of packages needed, with a view to keeping the cost down. So if, for example, only three of the four available gates on a three-input quad NAND package are needed, the fourth gate is used as, say, a line receiver, the inputs being joined together. This technique can be clearly seen by reference to the wiring diagrams.

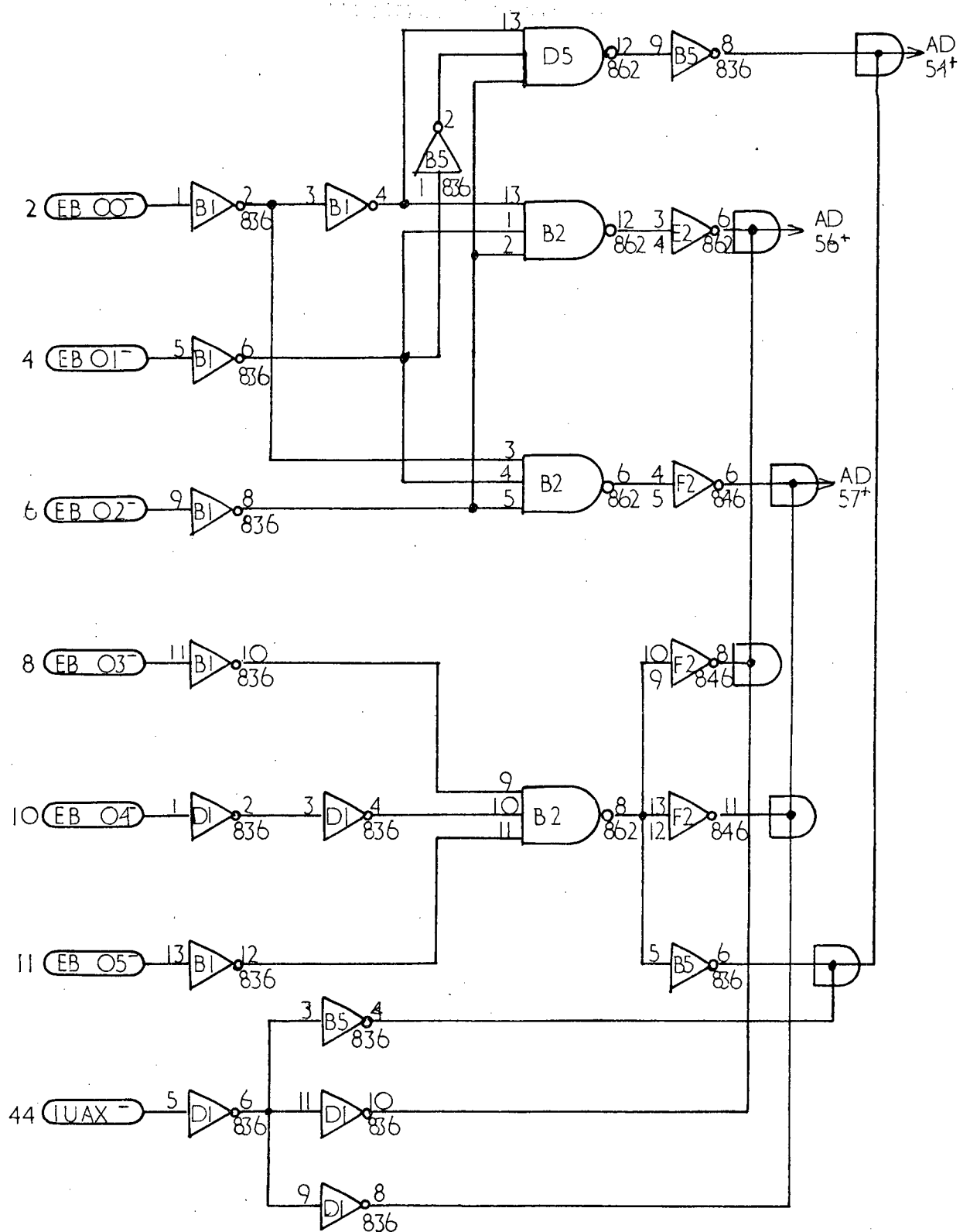
The specifications of the integrated circuits used are contained in Reference No 14.

The interface is mounted on a special plug-in board provided by the manufacturers of the computer. The board plugs in to the E-Bus on the expansion chassis of the computer, and is connected to the thyristor network by twisted pairs of cables, connected via an edge connector to the interface board. The integrated circuits are mounted on integrated circuit bases, and the interconnections are made using wire-wrapping techniques. No power supply connections are shown in the drawing, as these are immediately connected when the bases are soldered to the board, one side of the board being +5 volts, and the other 0 volts.

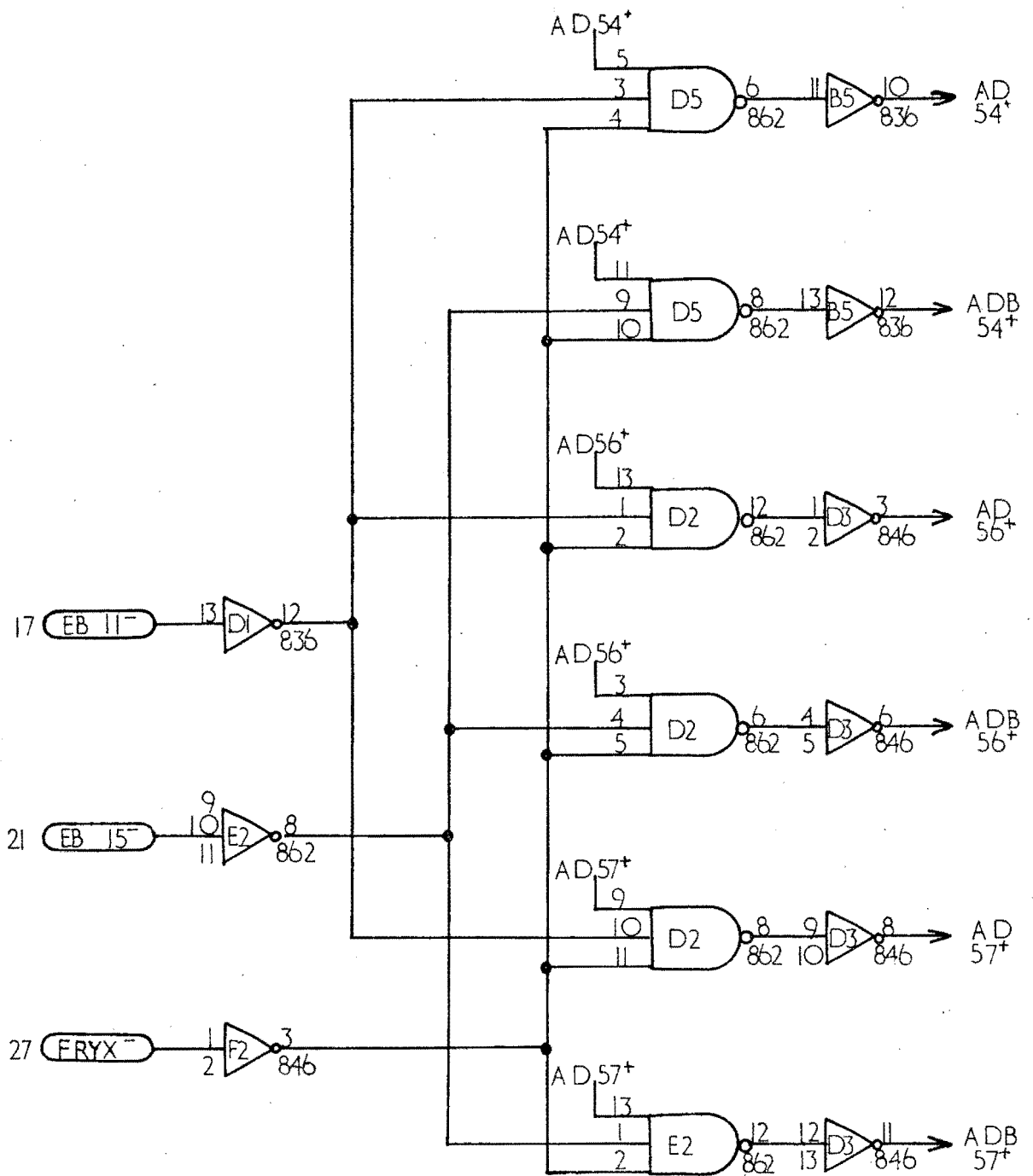
1.7 Comment

For the initial stages, this design can give 18 lines with a variable pulse-length available on any given line (i.e. any line can be set and reset under program control). When the work is extended to the full control of a 36-thyristor network, obviously the interface must be extended, and it might become advisable to review the idea of having a variable pulse-length, and, for obvious economic reasons, use each setting, or resetting, of the flip-flops to trigger a monostable to produce a pulse of suitable constant width. Using this idea, 36 separate lines may be available, but careful programming will be required. For the last part of the thesis it will be seen that 18 lines are required, half of the 36 thyristors being fired under a master-slave system. One advantage of the present arrangement is that either the normal or the complemented output may be used, depending on the firing circuitry employed

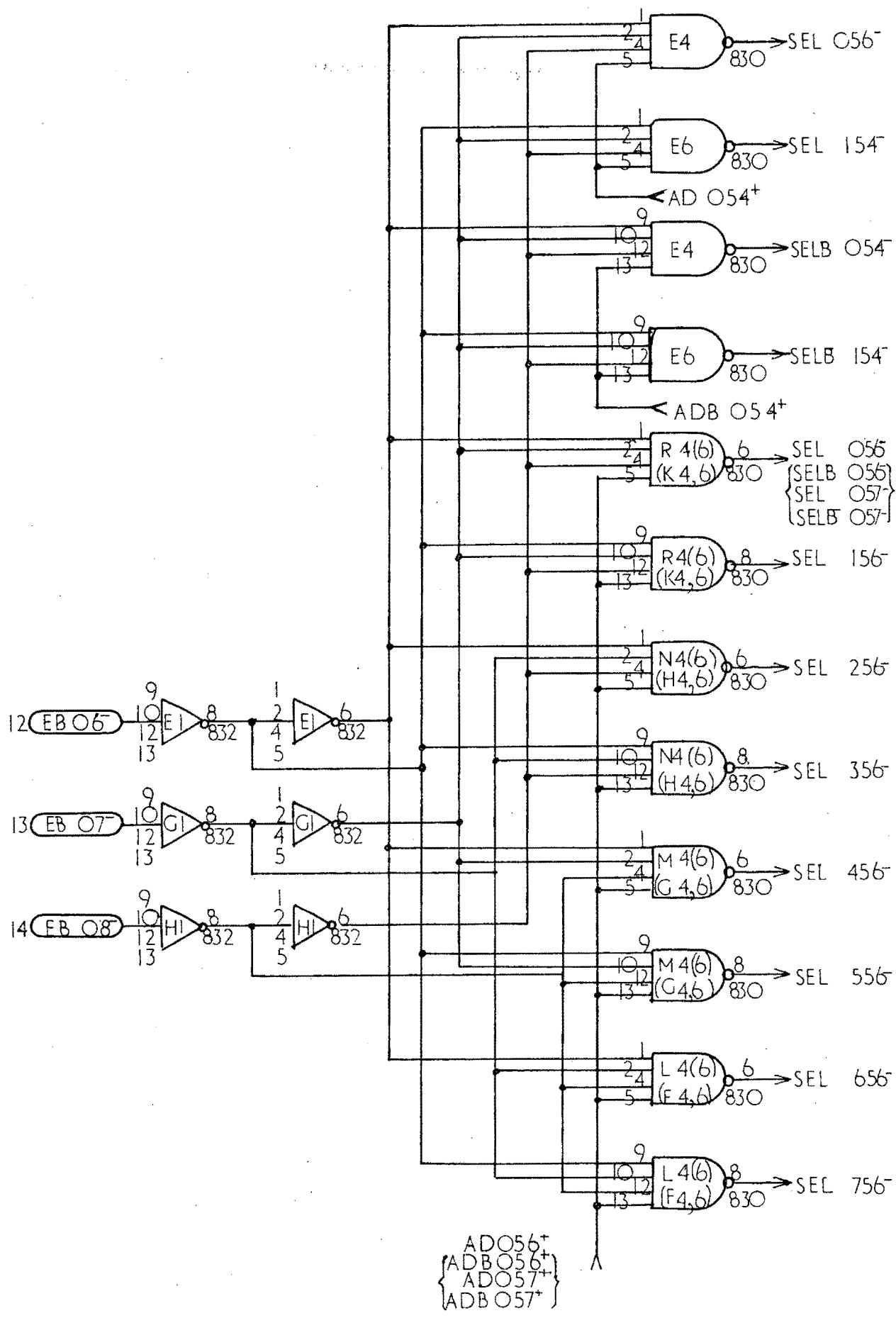
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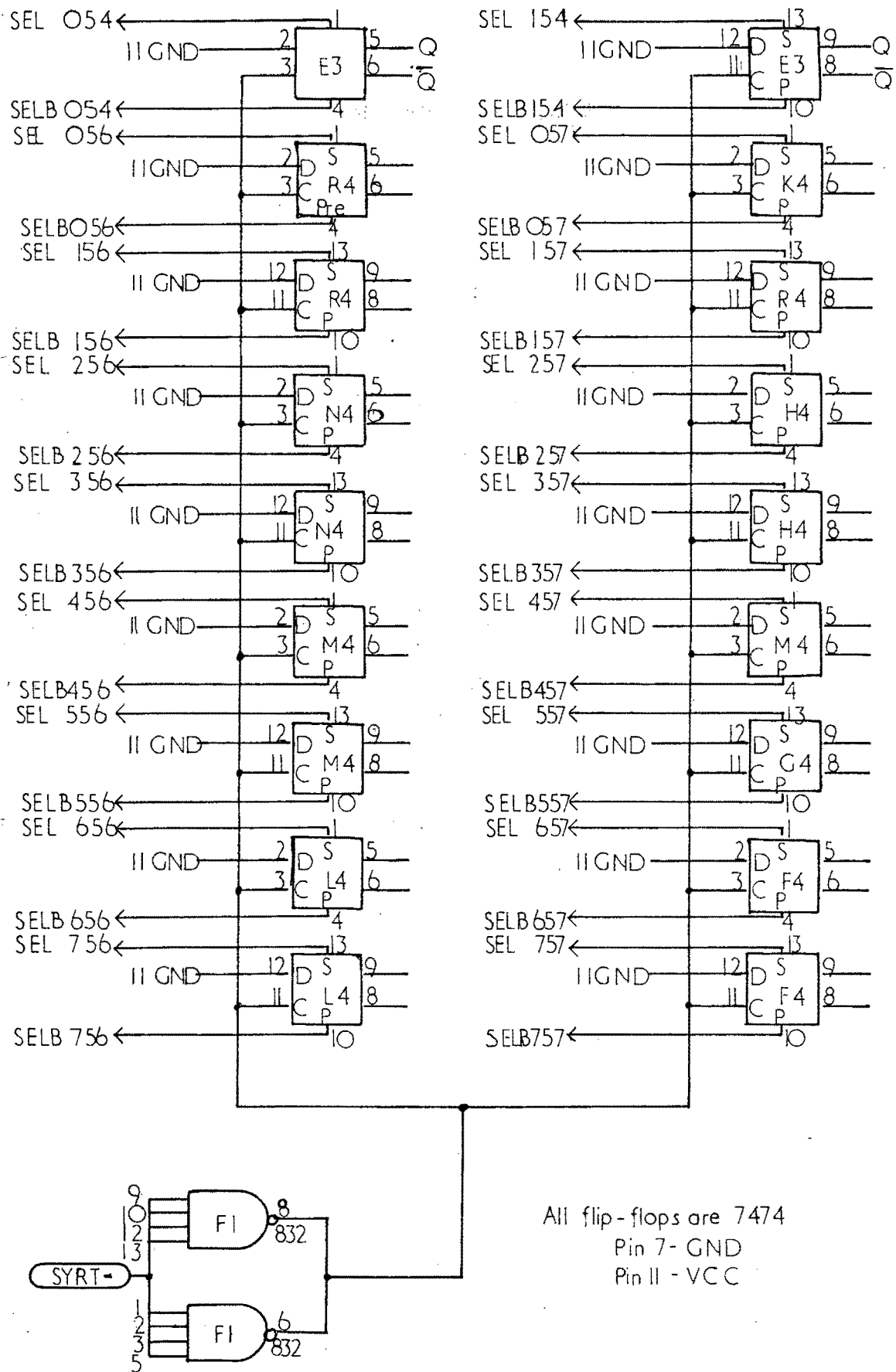
— FIG N°1(a): EXC INTERFACE —



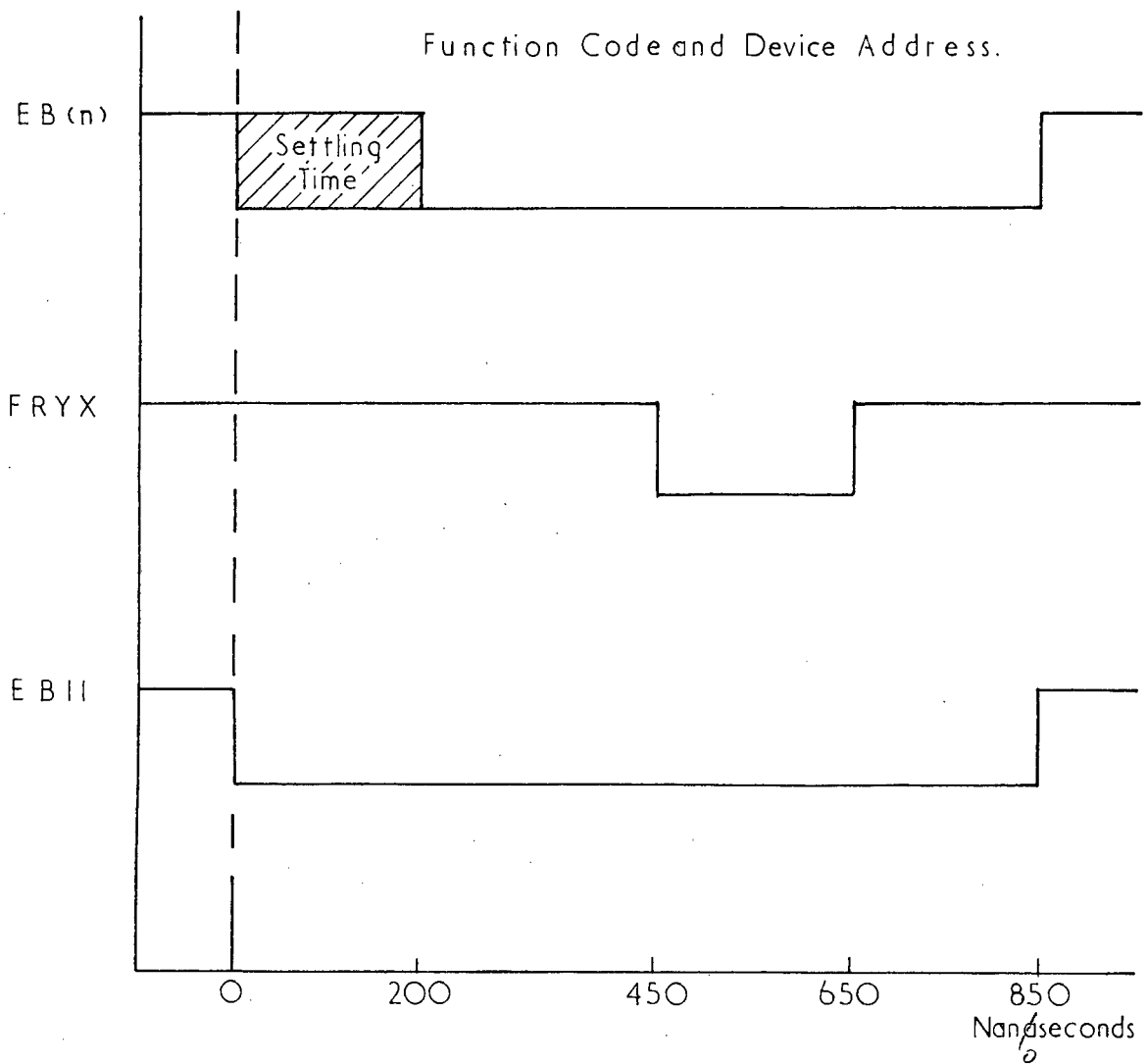
— FIG N° 1(b): EXC INTERFACING —



— FIG N° 1(c): EXC INTERFACE —

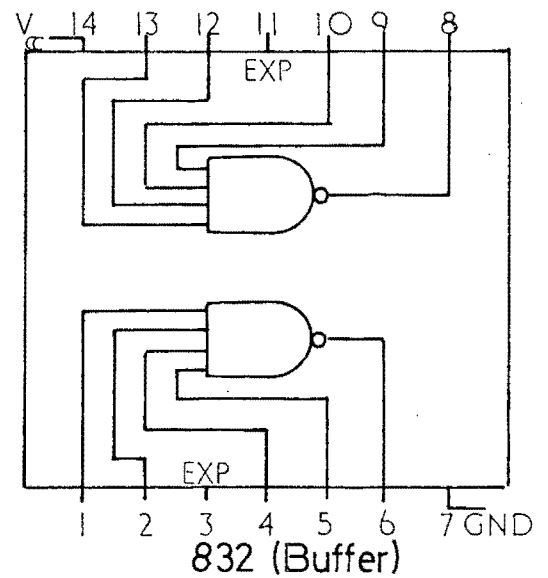
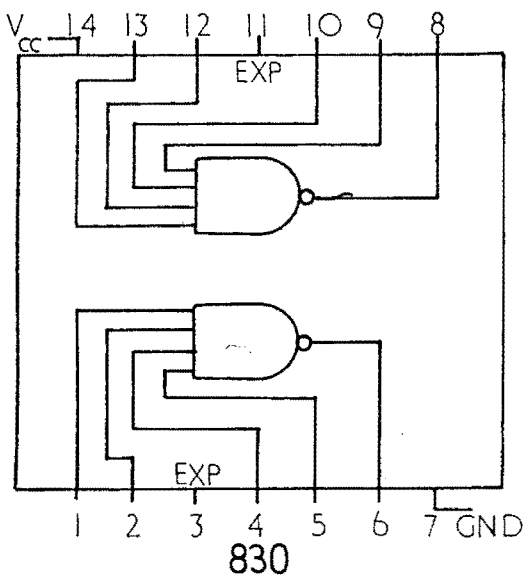
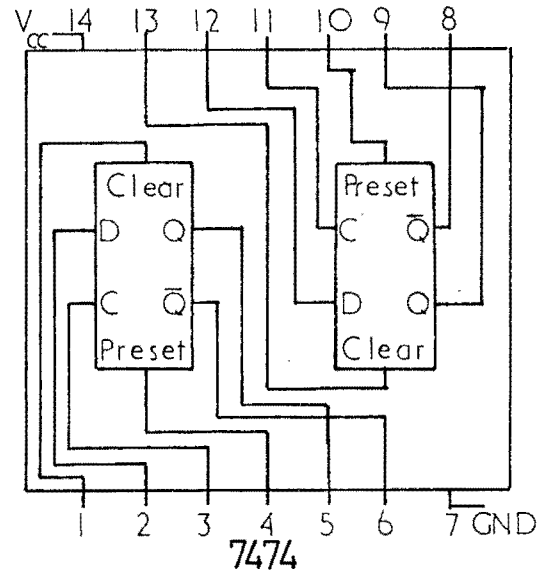
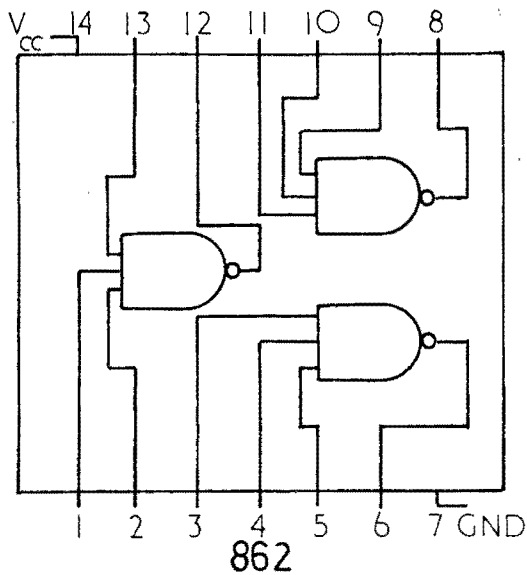
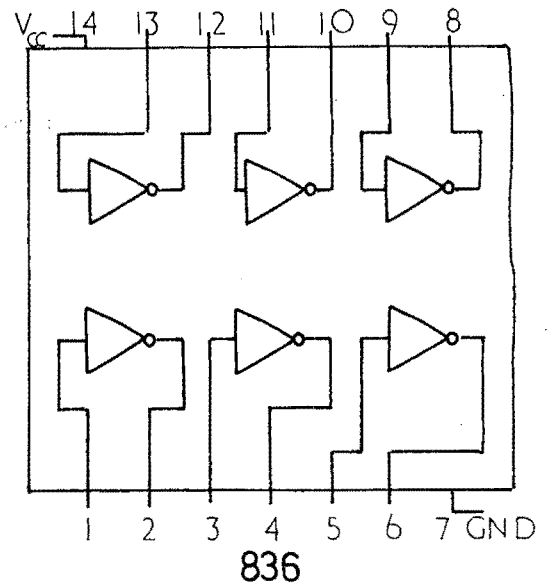
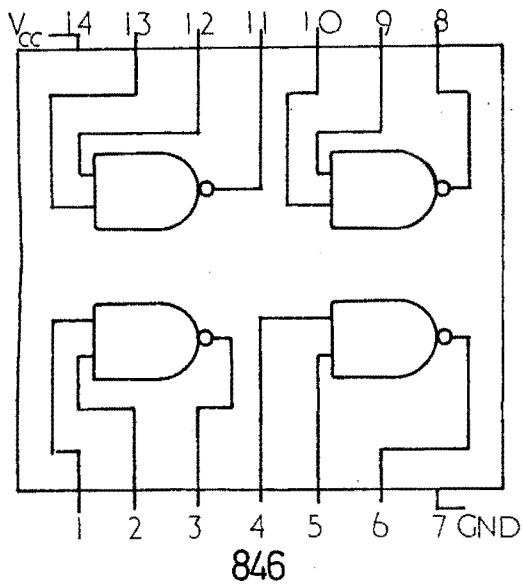


— FIG N° 1(d): EXC INTERFACE —



0 is taken as the start
of the execution phase of the instruction

— FIG N°(e) : THE EXC INTERFAC E—TIMING —



— FIG N°1(f): EXC INTERFACE —
 — INTEGRATED CIRCUITS —

CHAPTER II

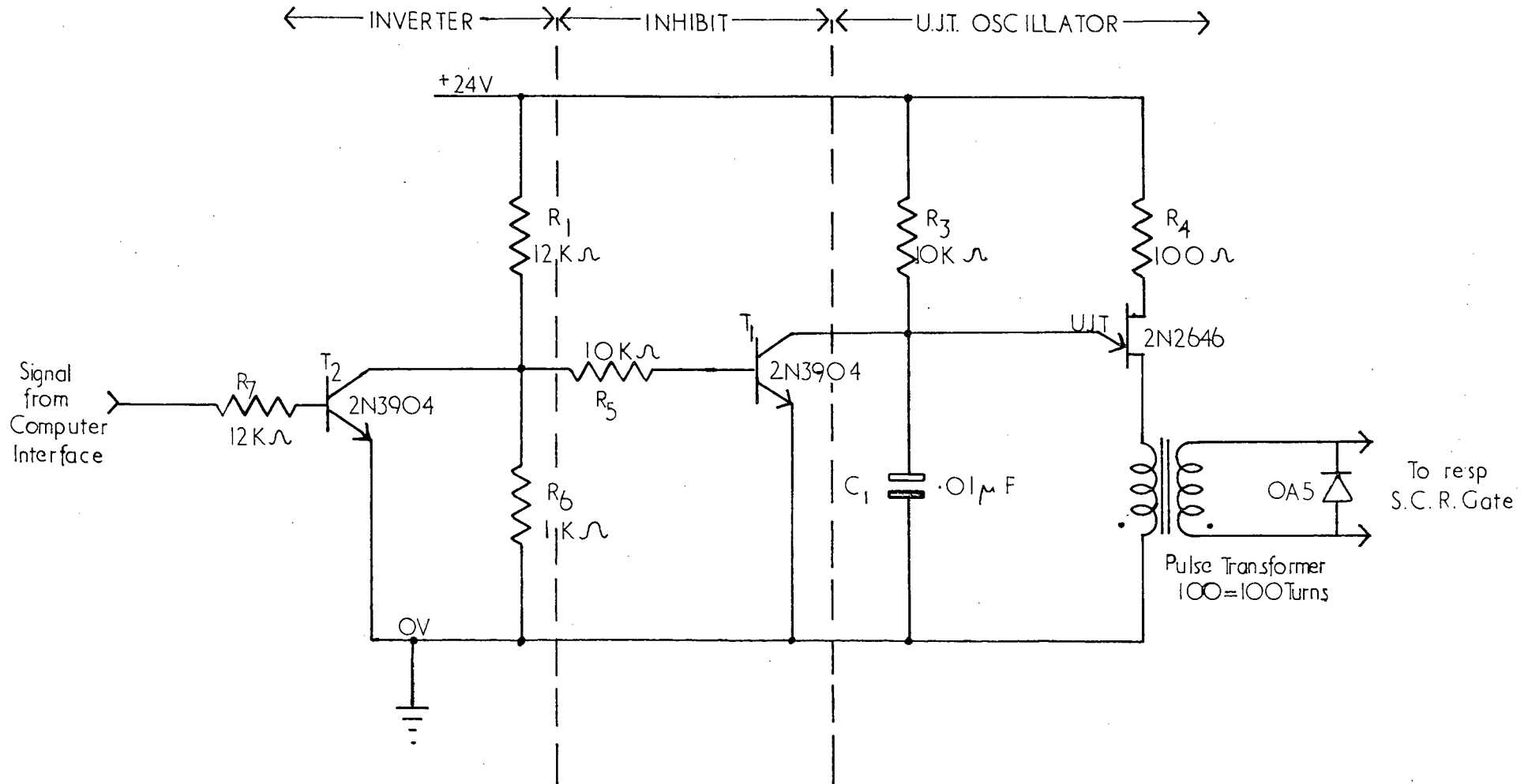
HARDWARE FOR THE FIRING OF SINGLE- AND THREE-PHASE THYRISTOR SYSTEMS.

For the first two systems to be developed, i.e. the control of a single thyristor, and the control of a three-phase thyristor network, there were three development requirements: firstly, a suitable firing circuit had to be designed and constructed, and secondly, a means of zero-crossing detection had to be devised. Thirdly, a means of setting the initial conditions had to be decided upon.

2.1 The Firing Circuit.

In order to ensure complete isolation of the power circuitry from the computer, the firing circuit chosen was a Uni- junction (UJT) oscillator, fed into the gate of the thyristor concerned via a pulse transformer. (Reference No 6)

The actual unijunction circuit is designed according to the manufacturer's data. For a 2N2646 unijunction (See Fig No 2), suitable supply voltage is +24 volts, and the period of oscillation is approximately $T = R_3 C_1$. R_3 is chosen from manufacturer's curves to be 10K Ω , and so for a frequency of 10KHz, the capacitance (C_1) required is $\sim 0.1 \mu\text{F}$. A simple means of switching the unijunction on was achieved by placing an NPN transistor (T_1) across the capacitor. When the transistor is on, the capacitance is shorted out, and hence the oscillator is inhibited. It was decided to use positive logic, so an inverter was required between the interface and the inhibiting transistor. The inhibiting transistor (T_1) was biased by R_1 and R_6 .



— FIG N° 2 : TRIGGER CIRCUIT FOR THYRISTORS —

So when the interface flip-flop is set to a 1 (= ±2volts) the inhibit is released from the unijunction oscillator, which then sends a train of pulses into the thyristor gate and fires the thyristor. Note that a train is more desirable than a single spike, because it ensures successful firing. In practice, a pulse of height +8 to +11volts should ensure firing.

The pulse-transformers used were made up from small transformers salvaged from an ICT computer, of a typical pot-core design with a fairly high μ_R (≈ 100). A satisfactory turns ratio was 1:1, 100 turns on both primary and secondary.

Power supply was from a regulated laboratory power-pack.

Choice of frequency was governed by two factors,

- (a) Maximum practical frequency of a unijunction oscillator, and
- (b) Quickest possible formation of the pulse after the release is given by the execution of the computer instruction. As stated before the frequency chosen was 10KHz, but this could be increased to 100 KHz if it is found desirable. However, the higher the frequency used, the shorter is the charging time of the capacitance, hence the smaller the energy fed into the pulse-transformer. This implies that a larger voltage must be applied to the unijunction; this being undesirable, the frequency of 10KHz was convenient.

2.2 Synchronization with the A.C. Supply to the Network

It was important at this stage to develop a suitable

method of synchronizing the computer to the mains. Two methods are available. The first is expensive in terms of both cost and time, but extremely fast in operation. This system was constructed on the EXC interface board, and is useful if only one initial synchronization is required. The second method uses the Analogue-to-Digital converter and is slower, but as it is immediately available and has multi-channels, it is more practical for systems when, say, three signals have to be individually synchronized.

2.2.1 Method 1. This method uses the "SEN" instruction (double word) in the 620/i instruction set. When this instruction is executed, it places an address (specified in the first word) on the E-Bus, and if it receives a "true" response from the device it is sensing, it jumps to the address held in the second word. In order to achieve this, the EXC interface can be used to obtain the necessary address decoding, and this signal can be gated with a pulse from a suitable zero-crossing detector. (See Fig No 3).

The zero-crossing detector ⁹ consists of an SN 72710N (Texas) differential-comparator which requires a power-supply of +14, 0, and -7 volts, and gives an output of approximately +2 volts when the incoming signal is positive, and 0 when the incoming signal is negative. (See Ref. 14 for details of the 72710N integrated circuit) The response time is approximately 40nsec. The output of this is used to trigger a monostable made up of four NAND gates and a capacitance. X

Thus the decoded address (in this case 056+, obtained

from the EXC interface) is gated with $EB12^{\overline{}}$ (which is true when the "SEN" instruction is executed), and the output from the zero-crossing detector. The output of the gate is fed back on to the $SERX^{\overline{}}$ line, which is thus set true, and the jump is made to the specified address.

The programming of this is extremely simple and quick as regards the number of instructions required, e.g.

```
ZERC, SEN, 056, NEXT
      , JMP, -2
NEXT, ...,
```

Obviously this system is highly accurate. The monostable is designed to give a pulse which must have a minimum width of $4x \text{ cycle-time} = 7.2 \text{ microseconds}$, to ensure that a zero-crossing is detected. Note: The power supplies for the comparator were obtained from those available on the E-Bus, i.e. -5 and +12 volts. Although these are not exactly as specified by the manufacturer, they do in fact operate the circuit without any loss in efficiency.

Note: From this idea another means of obtaining a zero-crossing point was evident. This uses the interrupt facility of the computer. This is an optional piece of hardware with 10 outgoing lines, which are normally set to approximately 5 volts. The interrupt system is automatically scanned every 900nanoseconds and the interrupt, in the form of one or more of the lines going to ground, is recognised before the fetch cycle of the next instruction to be executed. If signals exist on one or more of the interrupt lines, a system of priority determines the order in which they are to be

operated upon. When a signal is acknowledged, the instruction at a special interrupt address is executed. This can be used in the following way:

An external zero-crossing detection puts a signal on to an interrupt line. This then causes the computer to come out of a calculation, or a waiting routine, and to execute its firing sequence. In this way the computer can carry out many other functions and only be used to control firing when it receives an interrupt. (A similar scheme has been adopted in Ref 1) This suggests the possibility of the computer's controlling more than one network. This thesis will not be concerned with this idea, however, but in fact this principle will be employed by another research student working in conjunction with the author at the University of Cape Town.

2.2.2 Method II. The second method is more straightforward. It employs the Analogue-to-Digital interface, and consists simply of sampling the mains. An L.T. transformer was placed across the incoming A.C. supply, and a voltage of about 6 volts_{p-p} was connected to one or more of the Analogue-to-Digital input sockets. 6.3-volt zener diodes were placed across this feed, in order to protect the interface from any surges, etc.

To synchronize the computer with the supply, we simply have to take a sample and calculate whether it is, in fact, a zero-crossing point. Obviously, one will not necessarily find the exact point, because of the finite cycle times between calculations. A convenient method is to determine the maximum time between repe-

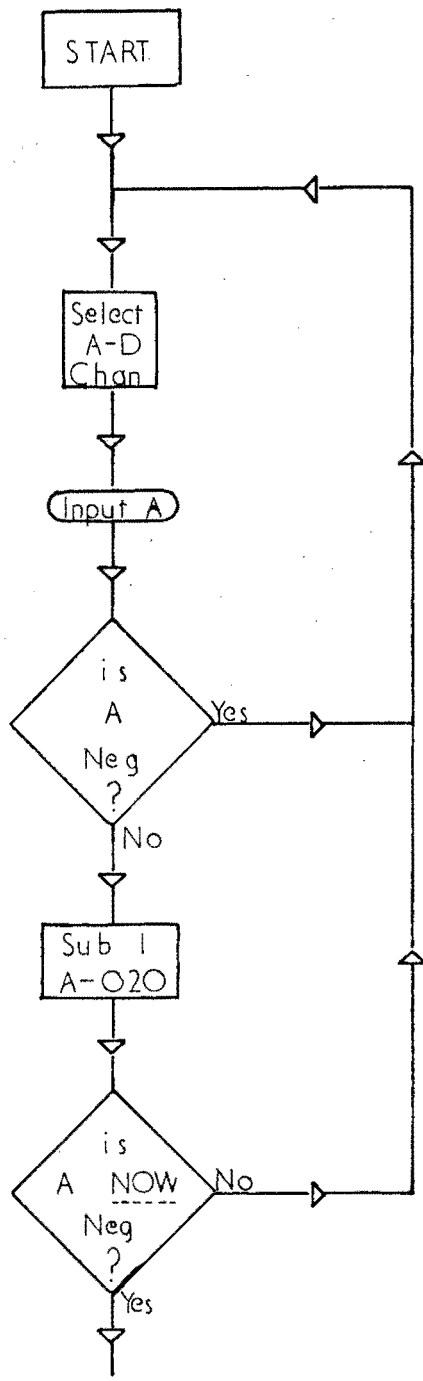
titive samples, say 20 microseconds, and subtract a suitably-scaled number from the sampled input. This is clearly shown by the following algorithm (See Fig No 4).

Note that this gives zero-crossing points of both positive and negative going crossings, but for the earlier tests this does not matter, as we can only fire the particular SCR after a positive going zero-crossing anyway! However, as will be shown later, a means can be devised to determine whether the zero-crossing detected is positive or negative going.

The immediate disadvantage of this scheme is, of course, speed - we must go through the Analogue-to-Digital algorithm and the zero-crossing calculations each time - but we have to balance this slight loss of accuracy against ~~convenience~~ and the simplicity of having a readily-available interface.

The Analogue-to-Digital algorithm is relatively simple, and involves the selection of the required channel, holding of the analogue sample via a sample-and-hold control, and the starting of the Analogue-to-Digital conversion. The module must then be sensed for conversion completed, and the digital value read into the computer's register. See Appendix I for details of the Analogue-to-Digital converter. The programming of this routine is as follows:
(Using the DAS assembler language form, see Appendix I)

, LDA , CHAN	Load A register with channel No.
, OAR , 055	Output channel No to multiplexer



— FIG N° 4: ALGORITHM TO DETERMINE ZERO-CROSSING —

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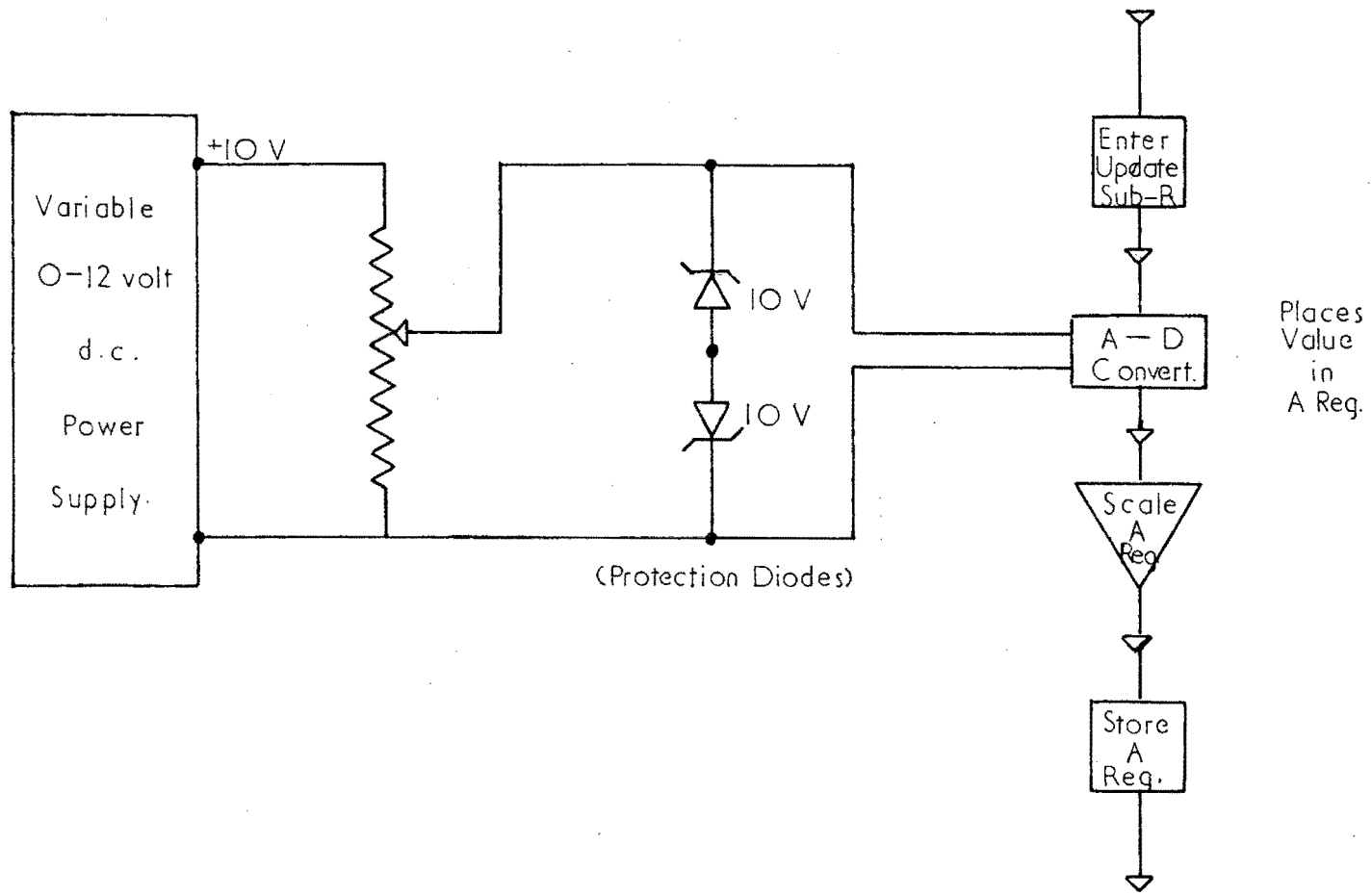
, NOP , (Delay cycle to allow for switching
, NOP , (in the multiplexer.
, EXC , 0155 Start Analogue-to-Digital Conversion
BACK , SEN , 0155 , INP (Sense if conversion complete.
, NOP , (If it is, jump to INP
, NOP , Wait
, JMP , BACK Try again
INP , CIA , 055 (Clear A Register and Input the
(digital value

```

2.2.3 Notes on the Choice of Method. In the work described here, both methods were tried and found acceptable for a single-phase system, but on a multi-phase system requiring more than one synchronization point, the second method was chosen for economic reasons. This would be true in most applications, because usually an Analogue-to-Digital converter is required to feed-back information to the system, so it would, in fact, make more use of the essential equipment.

2.3 Setting Initial Conditions.

A simple controller is required in order that the operator may set the initial conditions for the firing of the thyristor i.e. determine the phase angle or voltage required. A simple controller was devised, whereby a potentiometer was used to select a voltage (< +10 volts) which was fed into the computer via the Analogue-to-Digital converter, and the voltage read was suitably scaled to determine the firing-angle. The combined algorithm and circuit diagram is shown in Fig No 5 . This means that the operator can select the firing-angle of the thyristor, i.e. the execution



— FIG N°5 : UPDATING OF THE FIRING ANGLE —

of the firing instruction at a selected interval after synchronization via the detection of a zero-crossing point.

The scaling is based on the number of computer cycles per delay loop (see program later); the value of the angle being held in terms of the number of countdown loops which must be gone through to achieve the current firing delay after synchronization.

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CHAPTER III

THE CONTROL OF THE FIRING ANGLE OF A SINGLE THYRISTOR

This was chosen as the logical first step in the development of a computer-controlled thyristor system, as it would involve many of the features required in the ultimate system, i.e. a simple algorithm, a suitable firing circuit, synchronization with the incoming A.C. line, and some form of simple control to determine the required firing angle. The electronics have been dealt with, and this chapter will deal with the development of the algorithm and its implementation.

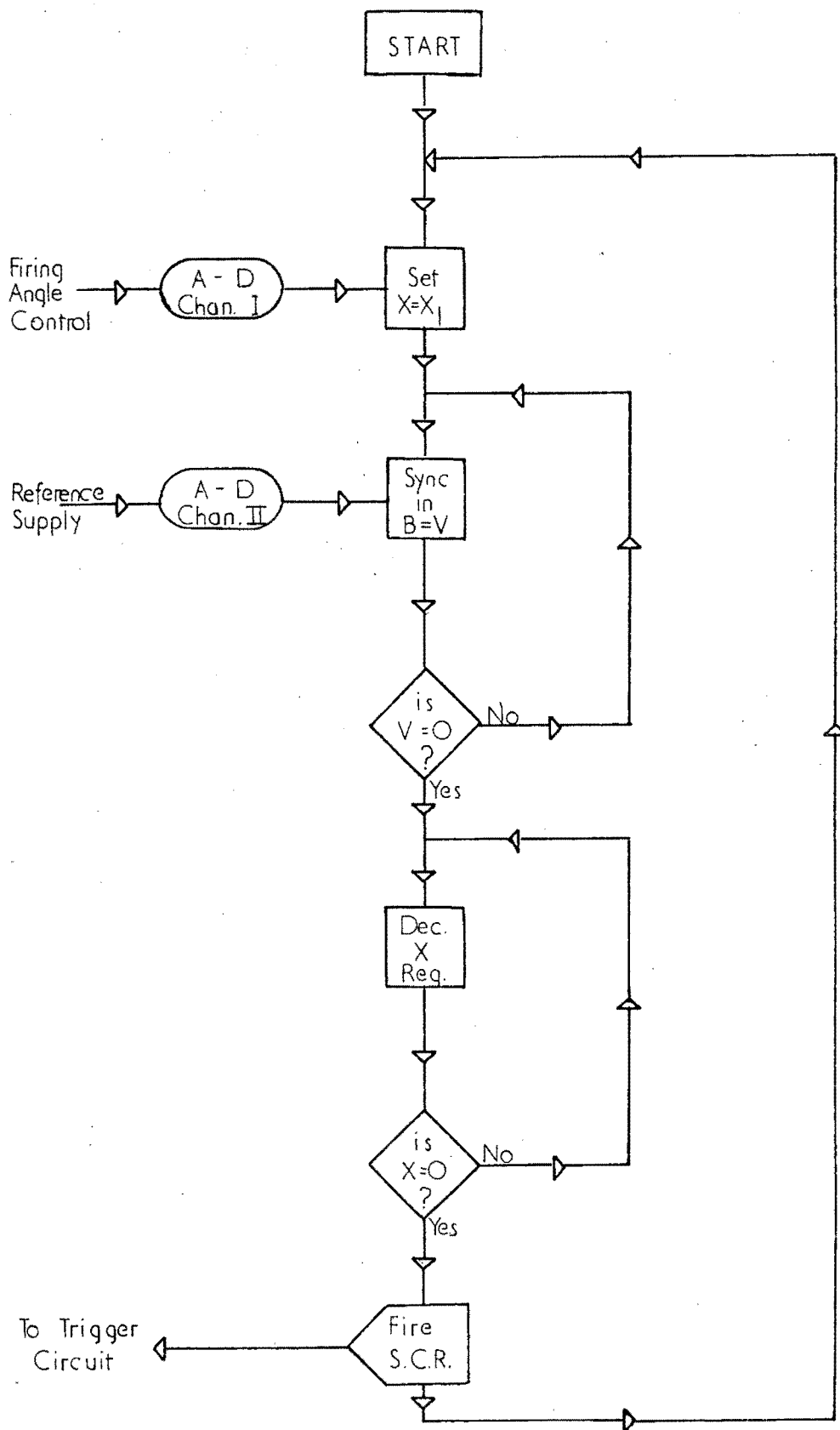
3.1. The Firing Algorithm.

The algorithm for the single-phase firing is very simple but does involve the basic principles for any firing system, i.e.:

- a) Update desired firing angle.
- b) Synchronize.
- c) Go into a countdown loop to achieve delay.
- d) Fire the thyristor.
- e) Reset the firing flip-flop after a set delay - this delay being chosen with a view to ensuring that the thyristor does, in fact, fire even if it does not fire on the first pulse released by the unijunction trigger circuit. It must, naturally, be reset in time to be able to find the next zero-crossing point. The algorithm is shown in Fig No 6, and the program follows simply from it.

3.2 Experimental Arrangement.

The single thyristor was connected up initially to a



— FIG N° 6 : SIMPLE ALGORITHM —
 — FOR PHASE-CONTROL OF ONE THYRISTOR. —

purely resistive load, the voltage being set by a variac, and the firing angle varied over its whole range. The second test was to feed the output voltage into a small D.C. machine, with a series .2H choke, to obtain a degree of smoothing, and so to test the system working on an inductive load. A summary of results is given in the next section. Note that it is rather difficult to calculate the duration of the firing angle delay routine, and in practice this had to be carried out on the experimental apparatus.

3.3 Conclusions on the Control of the Firing Angle of a Single-Phase System.

Extensive tests were carried out on this simple system, and these proved to be most successful. The firing angle could be varied over a full range from about 3 degrees to 180 degrees. The only limitation is that there is a delay of ± 20 microseconds, due to the finite delay between the computer's detecting the zero-crossing, and the actual production of the firing pulse. Note: This delay is, of course, dependant on which synchronizing system is used. At the present time the delay is so very small as to be negligible, but it will have to be considered in future systems where overall efficiency is considered.

The accuracy is exceptionally good, e.g. a delay of 180 degrees was proportional to a setting of the X-Register of 3500 (octal), so the selection of the angle is accurate to about 1 in 1800. Obviously the accuracy is a function of the controller for setting the X-Register, viz. the potentiometer arrangement feeding into the Analogue-to-Digital converter.

As stated before, this system was used to drive a thyristor into both resistive and inductive loads, at voltages and currents within the rating of the thyristor, and the overall result was proof that the system is feasible.

A particularly interesting calculation is the determination of the time the computer needs to perform the essential functions - for the above algorithm it shows that $\pm 99.6\%$ of the computer's time is taken in waiting for a synchronization pulse or in a countdown loop. Obviously, this is time that can be used for performing many other error calculations, firing other thyristors, updating, etc. This is, of course, of interest in the time-sharing of the computer, i.e. to make more use of the computer's time by means of controlling more than one machine, data-logging, etc.

3.4 Comment.

An extremely accurate, and extremely expensive, method of controlling the firing angle of a thyristor! But this did prove that the system is feasible, and provided a check on the software, the interface, and the firing system.

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CHAPTER IV

TO CONTROL THE SPEED OF A D.C. MACHINE

USING A THREE-PHASE, HALF-WAVE RECTIFIER

This was the second step in the development of the system, involving the production of suitable software to control a three-phase, half-wave thyristor network, bearing in mind the initial conditions and the response of the system. The general idea of this section was to control the speed of the machine via armature voltage control, i.e. to set up the voltage required to run the machine at a certain speed without any load. As the load increases, the applied voltage must be stepped up to maintain a constant speed, and vice-versa, the field of the machine being separately excited.

4.1 Firing Circuits.

The firing circuits for the half-wave bridge are identical to those previously employed on the single-phase control, except, of course, that three are required.

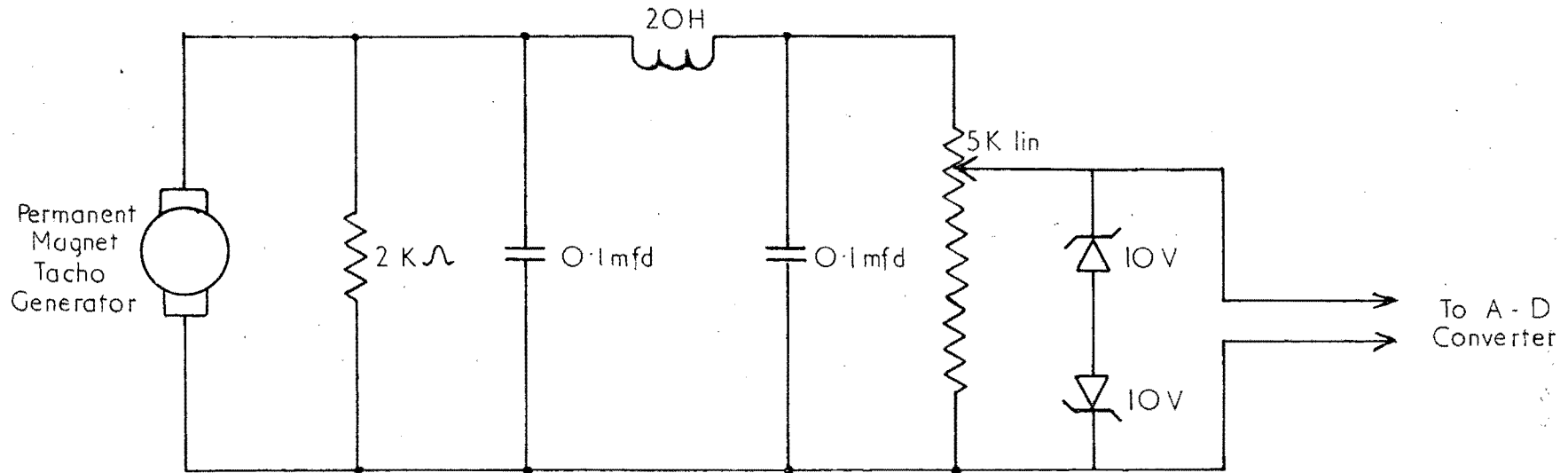
4.2 Feedback Circuitry.

In order to read the speed of the machine, the use of a tachogenerator was required, positioned on the shaft of the machine. The tachogenerator used for the purposes of this experiment was an ex-aircraft D.C. tachogenerator with rather unsatisfactory characteristics : having relatively few commutator segments, the D.C. output contained about 50% ripple, and this necessitated a filter to achieve a smooth, ripple-free output.

But, in addition, the time-constant of the feedback had to be considered. Ideally, the tachogenerator should react immediately to any change in the speed of the machine, but with the filter the time-constant of the feedback system was greater than that of the machine. So a fairly unstable system could be predicted, and, considering the speed of the computer, a fair amount of "hunting" was expected. This would arise because the machine would speed up, but the speed fed back would lag and cause the required position to be overshoot, and, of course, when slowing down, the reverse would occur.

One technique that can be used is to sample the tachogenerator output, say every 50 cycles, and to make a change in firing angle only after that period. Also, to achieve a certain amount of smoothing from the computer, one can average out the readings made every cycle and take an average at the end of the sampling period. This averaging process requires a careful mathematical analysis in order to determine the optimum number of samples and the validity of the result. This process will not be dealt with in this thesis, but in practice 24 samples are most suitable. (Further details on this sampling technique may be found in Ref Nos. 16 and 17)

See Fig No 7 for the filter circuit. The design of the filter will not be dealt with in detail here, but it was carried out using conventional methods (See Appendix III). The design yields a filter which reduces the ripple to approximately 2%, but unfortunately has a rather long time-constant.



— FIG N° 7: TACHOGENERATOR FILTER CIRCUIT —

Note: The ripple is, of course, a function of the machine's speed, so the ripple output of the filter is not the same over all ranges of speed.

4.3 The Firing Algorithm.

The algorithm for firing this system is purely an extension of that used for the single-thyristor control, with only two important changes:-

- a) Dealing with a three-phase system implies that, if the firing angle is greater than 120° , provision must be made to synchronize with the next phase, whilst still counting down the first phase. This amounts to having facilities available to have two countdown registers available at any one time. This does suggest the possibility of only synchronizing on one phase and using that point as a reference for the other two phases, but in order to make the system as flexible as possible, this approach was not adopted. Also, it could be necessary in such a system to determine both negative- and positive-going zero-crossing points.
- b) In the updating routine, the set speed must always be read as before; but, in addition, the actual speed, as detected by the tachogenerator, must be sampled, suitable averaged as previously discussed, and then compared with the required speed, after which appropriate action can be taken. Also, because of the slowness of the tachogenerator, a facility must be available to restrict the firing angle to within realistic limits, i.e. to prevent the machine's hunting from one extreme to the other.

Fig No 8 shows the algorithm for one phase and the in-

terconnections to the next. A brief outline of how this algorithm works follows below:

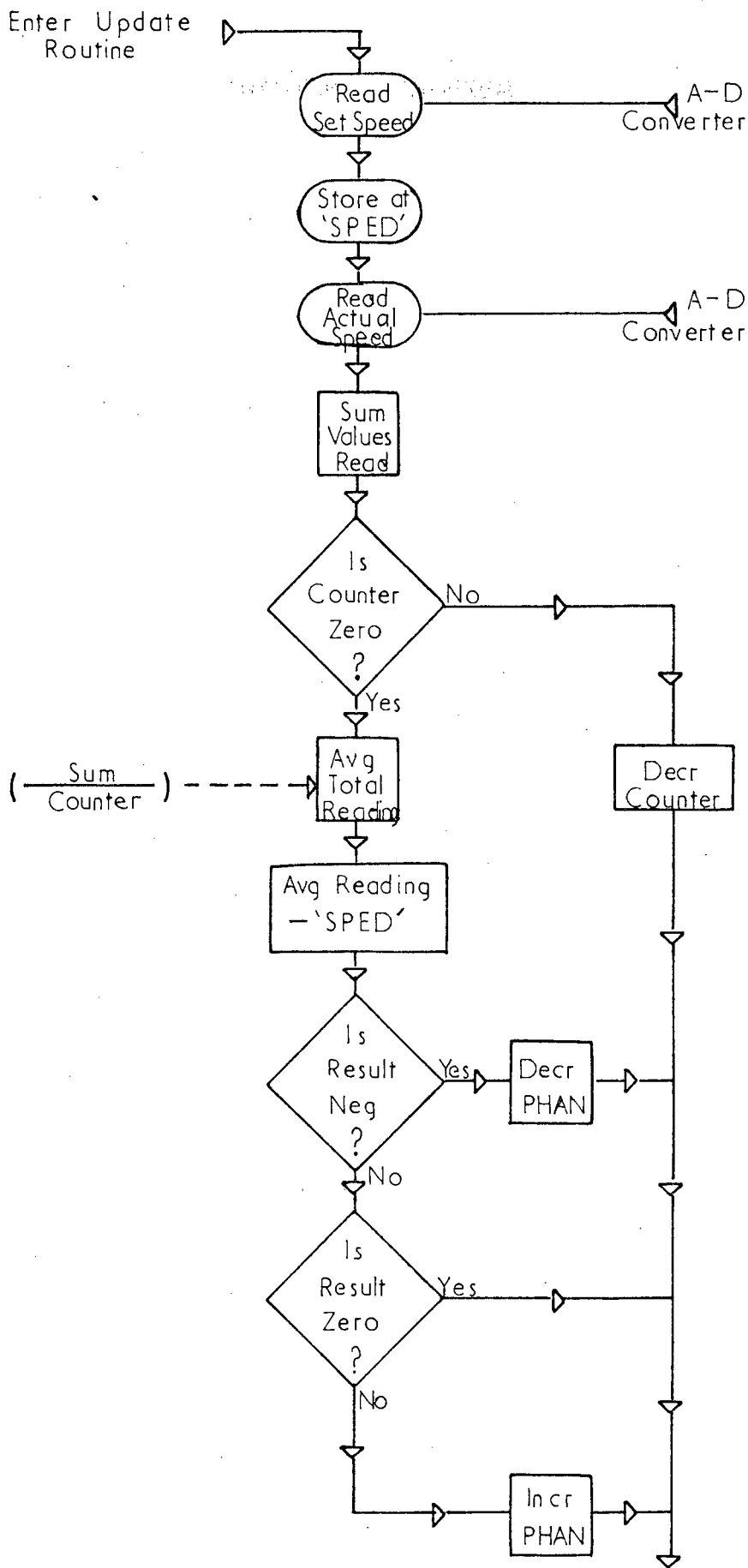
When the program commences, the machine is set to run at a set speed until the first tachogenerator reading is obtained. The firing section starts by setting the B-Register to the set firing angle, suitably scaled, called "PHAN". The synchronization point for the A-phase is found, and the countdown for the A-phase is started. In the countdown loop, a search is made for the zero-crossing point for the next phase, say the B-phase. If this point is found before the countdown for the A-phase is completed, the X-Register is immediately set to "PHAN", having previously been set to zero. Once the X-Register is set, this is used as a "flag" to indicate that in fact the B-phase has been synchronized, so that if the X-Register is not zero, the search for B-phase synchronization has been completed. So in the same loop both the B-Register and the X-Register are decremented

Once the A-phase countdown is completed, the firing-pulse for the thyristor in this phase is produced, and the phase is fired. A check is made to see if the next phase, the B-phase, has been synchronized. If it has, the contents of the X-Register, which has already started the countdown for the B-phase, are shifted into the B-Register and the whole procedure is repeated. If the flag has not been set, indicating that the B-phase has not been synchronized, the B-Register is loaded with "PHAN" and a search is made for the synchronization point, and then the procedure is repeated as before.

(See Fig No 9) In each case, just after the synchronization point has been found, the updating routine is entered. In this the set value is read and stored at "SPED" (the initial set speed being held in "PHAN", both "SPED" and "PHAN" being labels of specified locations in the memory). The actual value of the speed is then read and stored at a specified location and successive readings are added to this, until the correct number of samples has been made. When this point is reached, the total is divided by the number of samples made, and an "average" is placed in the A-Register. The value of "SPED" is subtracted from this value. If the result is negative, indicating that the machine is running too slowly, the current value of the firing-angle ("PHAN") is decremented. If the result is positive, "PHAN" is incremented, and if it is zero, indicating that the speed is correct, no change is made to "PHAN". In this manner the comparator compensates for any variations in speed.

One immediate disadvantage of this method is that the countdown loops are not always of the same length, because of the necessary calculations made after a predetermined number of cycles, but the overall effect is so small that it does not affect the speed of the machine. In fact, every 24th firing cycle is slightly different, but this slight change in voltage is absorbed by the inductance of the circuit, and the machine being driven does not react to the variation.

A short routine is used after the correction of "PHAN" has been carried out. In this routine the value of "PHAN" is examined and never allowed to exceed suitable upper and lower limits. That is, if the machine is running up to full speed, until that speed is reached



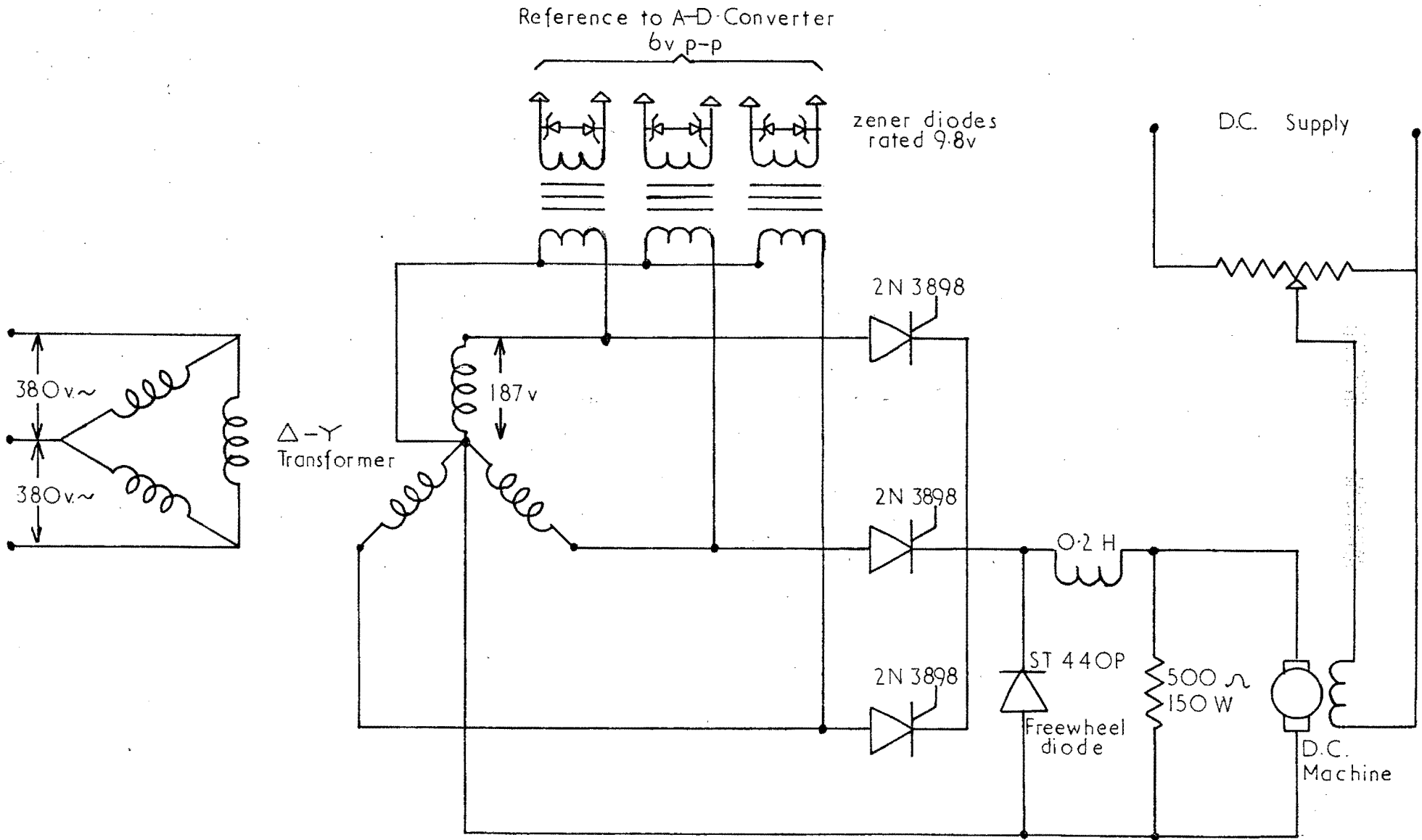
— FIG N° 9: UPDATING ALGORITHM —

the tachogenerator will always indicate that the speed is too low, and the firing angle will continually be decremented - so the routine will hold to its lowest limit, and prevent "PHAN" from becoming negative.

4.4 Power Circuitry.

See Fig No 10 for the power circuits. The machine driven was a 4 h.p. machine, rated at 220 volts and 16.7 amps at 1500 r.p.m. The field was separately excited and held at constant excitation throughout. The thyristors available were RCA 2N3898, with a rating of 22 amp D.C. average, and a peak surge current rating of 350 amperes, this being suitable for maximum loading of the machine. (See Appendix II for specifications) The supplies were taken from a three-phase transformer giving 187 volts on its secondary, so the maximum rating of the machine was, in fact, obtainable.

In order to give the thyristor a small current to fire on (being an inductive load, of course, the current will lag behind the voltage), a resistance of $500\ \Omega$, 150W was placed in parallel with the load. A choke was necessary to smooth the waveform of the resultant voltage, this being rated at 16 amps, 0.2 H. An avalanche diode was connected across the armature of the machine to maintain current through the inductive load when the thyristors are switched off. Using this, commutation was aided by bypassing the holding current which the inductive nature of the circuit causes to flow - this would prevent the thyristors from turning off, even though the applied voltage was zero. This diode would also, being of an avalanche type, protect the system from high-voltage transients caused by load switching.



— FIG N° 10: POWER CIRCUITRY —

4.5 The Speed Controller.

The same controller to set the desired speed as was used for the single-phase control, was employed here.

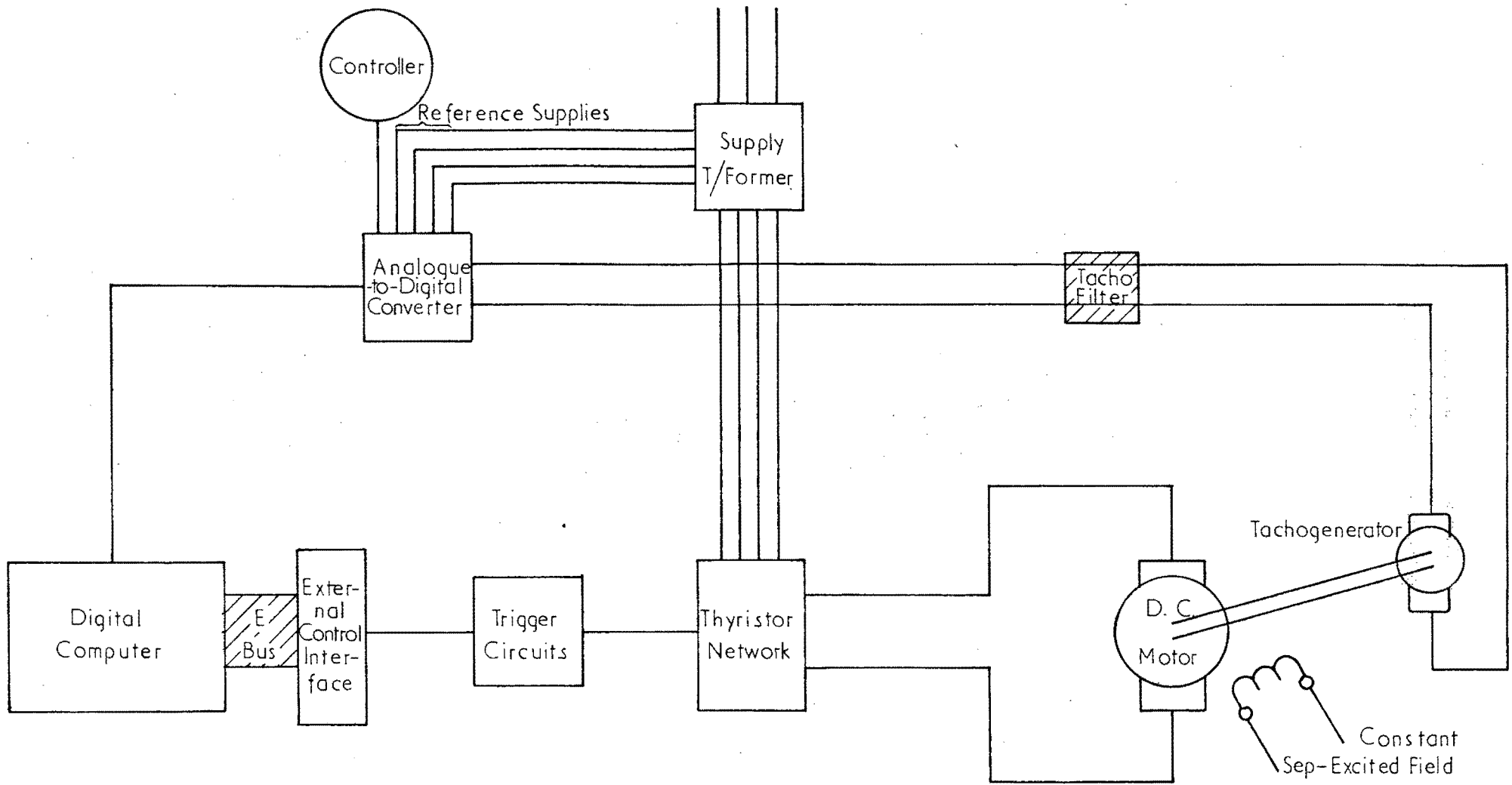
4.6 Zero-Crossing Synchronization.

This was achieved in the same manner as for the single-phase control, except that three transformers were used, connected as shown in Fig No 10. Again, zener diodes were connected back-to-back to protect the Analogue-to-Digital converter from over-voltage on its inputs. It is obviously important to ensure that the phase relation between the low voltage applied to the Analogue-to-Digital converter inputs and the normal voltage applied to the thyristors, is correct, i.e. that they are exactly in phase.

4.7 Performance of the Control System.

The overall system (See Fig No 11) functioned rather as expected, and produced a rather effective speed controller within the limits of the equipment. As stated above, the tachogenerator with its necessary filtering equipment is the defect, and applies a severe restriction on the stability of the system. Scaling of both speed inputs, via controller and tachogenerator, is relatively simple and is best carried out by an initial estimate and final adjustments made on-line.

The machine was loaded up to full load by means of a dynamometer (i.e. a free-swinging D.C. machine) and with the speed set to various values, the speed-versus-load curves were taken. A typical characteristic is shown in Fig No 12. It was found that suc-



— FIG N° 11 : BLOCK DIAGRAM OF SYSTEM —

cessful control was achieved between about 25% of rated speed and about 80% of rated speed. In the lower regions the tachogenerator becomes increasingly unreliable, and in the upper regions the limitations of the 187-volt supply do not permit a high enough D.C. voltage to be produced. Between the speeds stated, the speed regulation is as good as 3% (i.e., a variation of 3% between speed at no load and at full load).

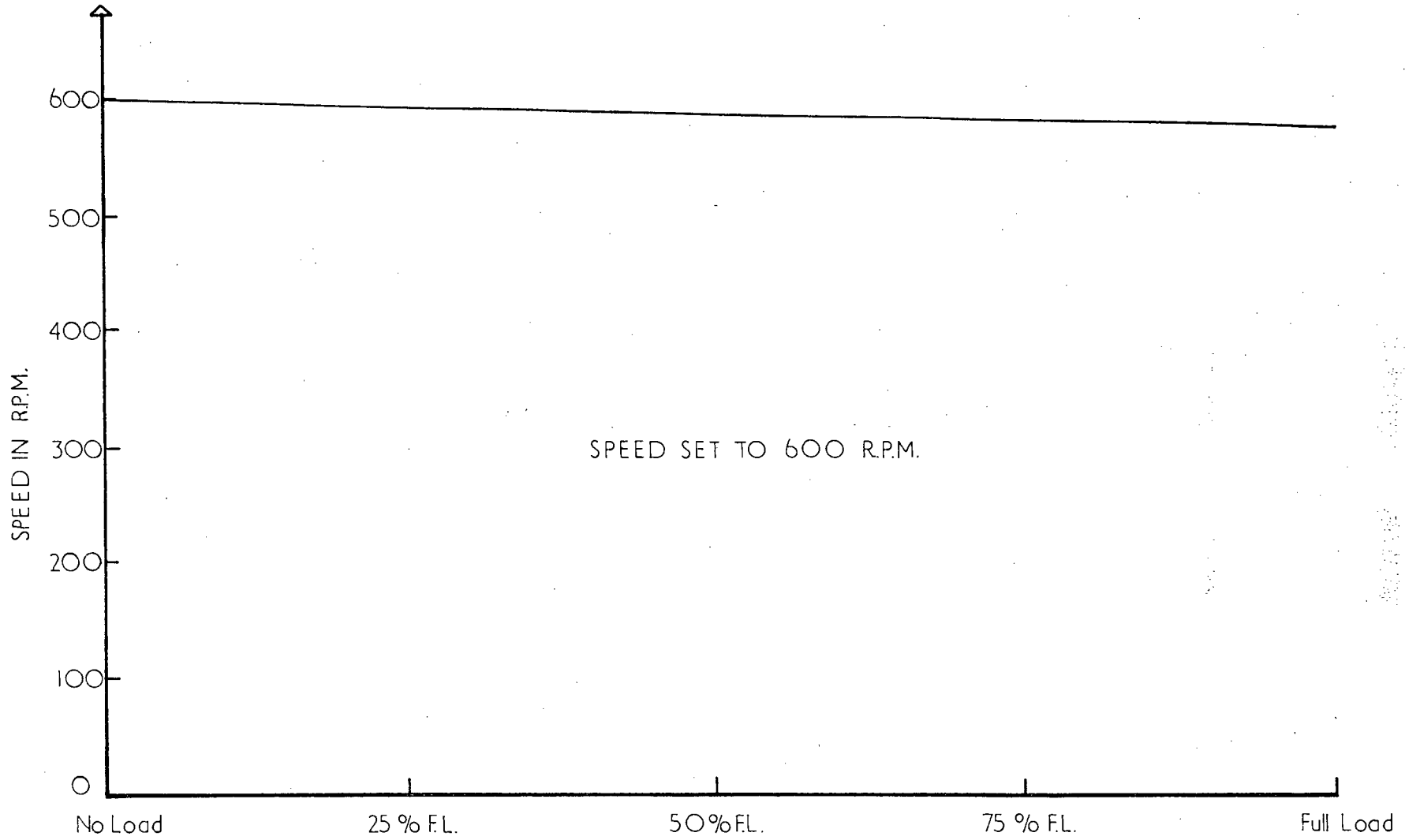
Obviously, as a precise speed controller this is not very impressive, but extremely good control can be achieved with a more accurate, ripple-free, faster tachogenerator. It was felt that as this was only a step towards the control of the A.C. machine, it would not be profitable to go more deeply into this form of control, but obviously much work can be done to improve the system. The answer to the feedback problem can be found in one of two possible ways, i.e.

- (i) An improved tachogenerator, the output of which may be analysed by the computer using digital filtering techniques to produce an accurate and relatively fast indication of the speed, and
- (ii) Use of a speed indicator ^{giving} ~~given~~ a digital output, e.g. a shaft encoder. This, of course, would again have to be subjected to digital filtering techniques, but is obviously quicker than (i).

In practice, of course, other criteria would have to be examined to determine speed; for example, maximum allowed acceleration, maximum current, etc.

4.8 Conclusions on the Speed Control of a D.C. Machine Using a Half-Wave, Three-Speed Rectifier.

Why put heading here?



— FIG N°12: SPEED CHARACTERISTIC —

In principle, a very accurate speed control can be achieved, and in a highly efficient manner. In practice, the system is realisable, and results achieved are most encouraging. As a system in itself, this method is most useful, especially as it could be applied to the control of several machines by one central computer. This may be carried out on a time-sharing basis, and a suitable system has been worked out using local memories located on each machine, with use made of the interrupt facility on the computer. However, this is another project on its own.

As a step towards the A.C. machine control, this system is most valuable, and shows that the control algorithms are fairly straightforward and that error calculation is feasible. The limitations are from the speed detection hardware. An important fact which also ^{emerges} (comes to the surface) is that the computer can control extremely large pieces of equipment and, with the systems employed, receive no interference from that equipment.

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CHAPTER V

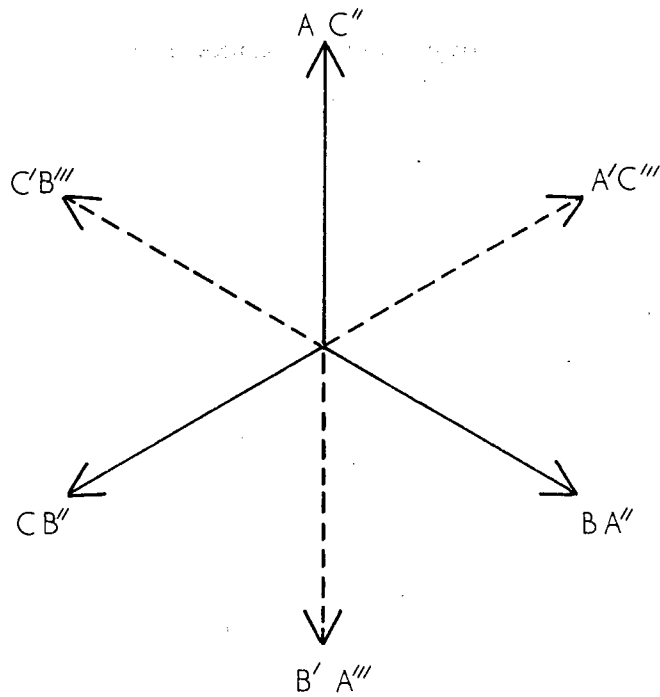
INTRODUCTION TO THE PRINCIPLE OF TIME MODULATION.

Although this thesis is primarily concerned with the digital control of the thyristor network required to implement time modulation of a three-phase system, it is necessary to get a clear picture of the principles involved in this unique form of modulation. The theory was developed at the University of Cape Town by Professor N.C.Enslin, and is forming the basis of Mr M.Case's work at present. The application of the principle to the control of induction motors has been patented by Professor Enslin.

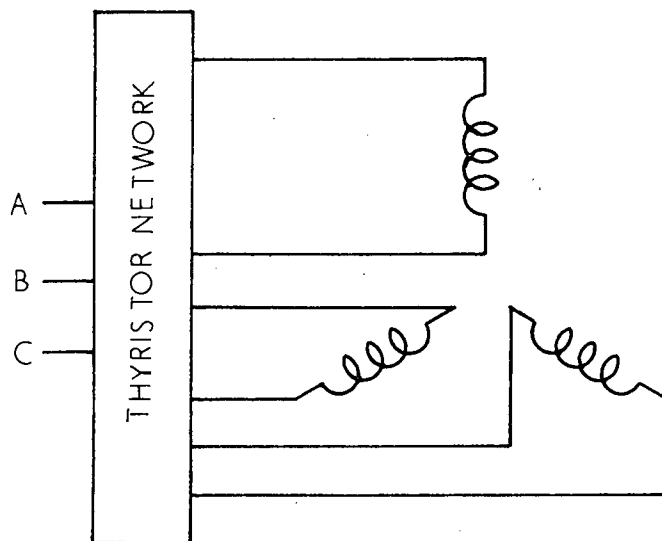
The principle is best illustrated when applied to the speed control of an A.C. machine, but, as will be shown later, the practical implementation of this presents many difficulties, so that this thesis will only demonstrate that control is feasible, and show that the software developed is successful, by applying the computer plus thyristor network to the control of a purely resistive load.

5.1 Simple Explanation of the Effect of Time Modulation.

If we consider a star-connected motor, as in Fig No 13, it is obvious that to run the machine at synchronous speed we would have to connect the machine to ABC on the phasor diagram. If we now reconnect the machine to A'B'C' it can be seen that the step would produce a 60° retardation. If, of course, the step was in the opposite direction, it would cause a 60° incrementation. So then if the machine is sequentially connected in the sequence ABC - A'B'C' - A''B''C'', etc, it would undergo successive retardation steps which



a) Phasor Diagram



b) Machine Stator Windings

— FIG N° 13: A STAR-CONNECTED MACHINE FOR —
 — A TIME-MODULATED SYSTEM —

would in effect produce a new applied frequency. The actual equivalent frequency would be a function of the speed at which we apply the successive re-connections - this is referred to as the "stepping-speed". The system will produce an output frequency which is given by the equation

$$f_{\text{out}} = f_{\text{supply}} \pm \frac{f_c}{2m}$$

when f_{out} is the effective output frequency, f_{supply} the frequency of the three-phase supply, and f_c the stepping speed (i.e. the speed at which we apply the sequential re-connections). m is the number of phases. Thus for a three-phase system we have a continuously variable output frequency which is purely a function of the input frequency and the stepping (or control) frequency. The direction in which we step determines whether the resultant frequency is above or below the basic frequency.

5.2 Application to the Control of an Induction Motor.

An induction motor is essentially a fixed speed machine whose speed is a direct function of the applied frequency, i.e. $N_s = \frac{f_o}{p}$, where N_s is the synchronous speed, f_o is the applied frequency, and p is the number of pole pairs. For many decades means of controlling the speed of induction motors have been devised (Ref any of the thousands of A.C. Machine textbooks and publications!). These have all been some means of controlling and varying the applied frequency, but most solutions are costly and bulky, and men have striven to achieve a relatively simple and economical solution. The development of the thyristor has led to the extension of inverters, etc, but the theory of time modulation offers a seemingly simple, economical

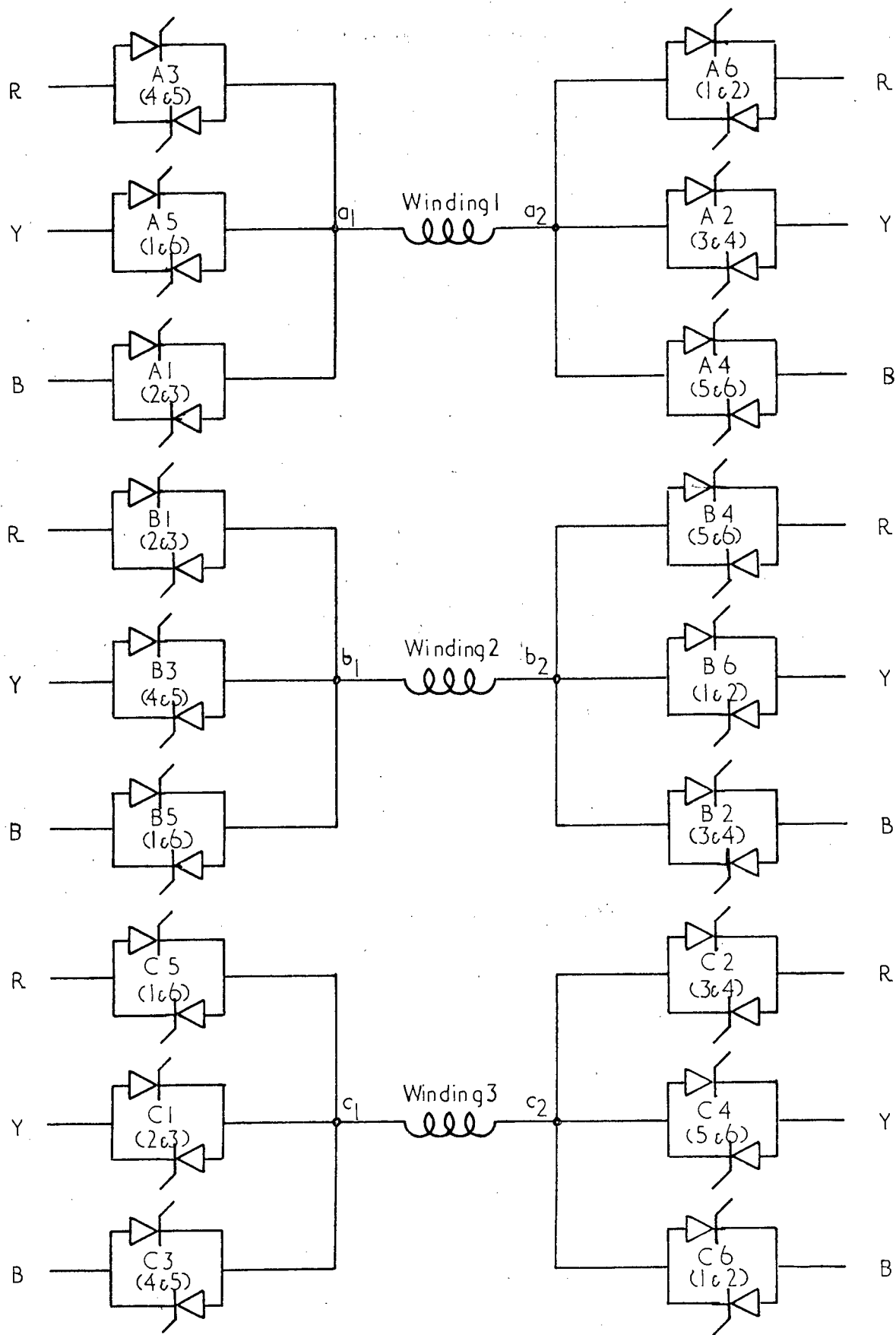
and less bulky answer. As thyristors are being developed with very large ratings and their costs are being reduced, a network of thyristors with a fairly simple control is becoming very feasible. The ability of the computer, as this thesis sets out to show, to control such a network, makes the idea very attractive, as the computer could control a multitude of machines in a complete system.

So, in general then, the synchronous speed of the machine would be given by $N_s = \frac{1}{p} (f_s \pm \frac{f_c}{6})$, where symbols have their same meanings. The important thing to note is that this is a continuously variable system, which in principle is dependant on the stepping frequency, f_c , the speed being variable over a range from just above standstill to twice synchronous speed.

5.3 Practical Implementation of Time Modulation.

Fig No 14 shows a thyristor network which will be capable of performing the necessary sequential switching required to carry out time modulation. This can be simply demonstrated if we follow through the following sequence for a delta-connected machine.

- (i) Connect winding 1 between yellow and red by turning on the two thyristors in set A5 and in set A6. The thyristors are connected in anti-parallel, and are fired alternatively.
- (ii) The first stepping pulse turns off set A5 at a suitable moment, i.e. a voltage zero-crossing of yellow phase, and then set A1 is fired. The winding is now connected between blue and red.
- (iii) The next pulse will turn off set A6 and turn on A2. The winding is now connected between blue and yellow, etc.



- FIG N° 14 : THYRISTOR NETWORK FOR TIME MODULATION -

The sequential switching order can easily be seen from the following table: (N.B. In this table the A's, B's and C's refer to the ends of each winding as per Fig No 14).

<u>OUTPUT FREQUENCY</u>	<u>RED PHASE</u>	<u>YELLOW PHASE</u>	<u>BLUE PHASE.</u>
$f_s - \frac{f_c}{6}$	c ₁ a ₂	a ₁ b ₂	b ₁ c ₂
(Direction of Stepping)	a ₂ b ₁	b ₂ c ₁	c ₂ a ₁
↓	b ₁ c ₂	c ₁ a ₂	a ₁ b ₂
Phase Sequence RYB	c ₂ a ₁	a ₂ b ₁	b ₂ c ₁
↑	a ₁ b ₂	b ₁ c ₂	c ₁ a ₂
(Direction of Stepping)	b ₂ c ₁	c ₂ a ₁	a ₂ b ₁
↑	c ₁ a ₂	a ₁ b ₂	b ₁ c ₂
$f_s - \frac{f_c}{6}$	a ₂ b ₁	b ₂ c ₁	c ₂ a ₁
	b ₁ c ₂	c ₁ a ₂	a ₁ b ₂
	etc	etc	etc

TABLE 5(i) : DETAILS OF SWITCHING SEQUENCE.

Note that in Fig No 14, each set of thyristors has been given two numbers - 2 and 3, 4 and 5, etc. These refer for convenience to the sequence of switching, i.e., to decrease frequency step 1 has A5 and A6 on, step 2 has A1 and A6 on, etc.

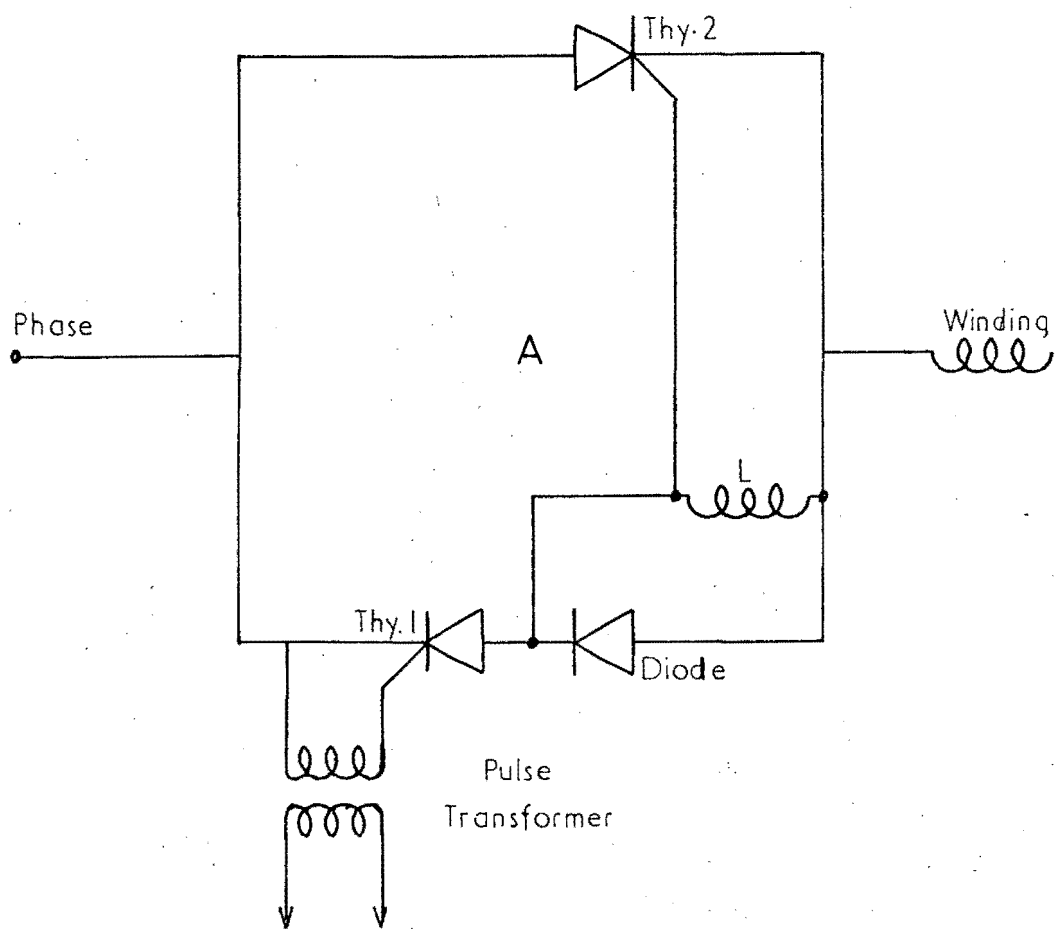
5.4 Determination of Switching Times and Negative Slaving

It is at once obvious that not only the order in which the thyristors are fired is important, but also when they are switched. As stated above, the two anti-parallel thyristors in each set are fired alternatively to allow conduction in both directions.

This could be done by providing alternate trigger pulses to the two gates, but in order to reduce the amount of controlling required, and hence reduce the overall cost, a system of "negative slaving" was developed. In this, a series diode in one arm (Ref Fig No 15) is used to provide the potential when its corresponding thyristor is conducting, which will provide energy to be stored in inductance L. When that thyristor ceases to conduct, the stored energy is fed into the gate of the second thyristor and causes it to fire. Practical problems met with in this system will be dealt with later, but in principle it does reduce overall control, but also reduces overall cost.

The solution to the problem of when to step to the new connection is not very clear, and, as will be shown later, there do seem many possibilities. At present, the system used is to detect zero-crossing of the phase to be switched off, and to base the stepping on this. The major problem is obvious - line-to-line faults - and this presents one of the major problems in the system. With a resistive load all is fine as current follows voltage, so voltage zeros are the same as current zeros, but with inductive loads, as presented by a machine, this is not the case. So it cannot be assumed that a voltage-zero is in fact the correct switching interval, as there might still be a current present which could cause the thyristor to conduct at the wrong time, and cause line-to-line faults.

For the purposes of this thesis, running on resistive loads, zero-crossings were acceptable and were found to produce successful results. But it does appear that switching decisions must not be based on voltage conditions only, but also on current conditions.



— FIG N° 15: NEGATIVE SLAVING —

5.5. Summary.

The intention of this chapter has been to present a brief and simplified introduction to the theories and some of the problems of time modulation. To get a physical picture of the effect visualize that you have a three-phase supply in front of you. To time-modulate you simply pick out a phase, then drop it, and pick up another phase, etc. The result is a wave which is composed of the bits of the sine waves you have selected. With the powerful tool of a thyristor available, plus the associated electronics, such a system is feasible for very large amounts of power.

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CHAPTER VI

DEVELOPMENT OF SOFTWARE FOR CONTROL OF TIME MODULATION

THYRISTOR NETWORK.

The ^{previous} last chapter dealt with the principles involved in time modulation, and from this emerged some of the problems which are encountered when programming a digital computer to control the sequential thyristor firing. The three main sections which have to be covered in the software development are:-

- (i) Zero-crossing detection
- (ii) The sequential switching.
- (iii) Delays and Updating.

The relevant flow-diagrams are contained in Figs No 16 (a), (b), (c), (d).

6.1 Overall Requirements of the Program.

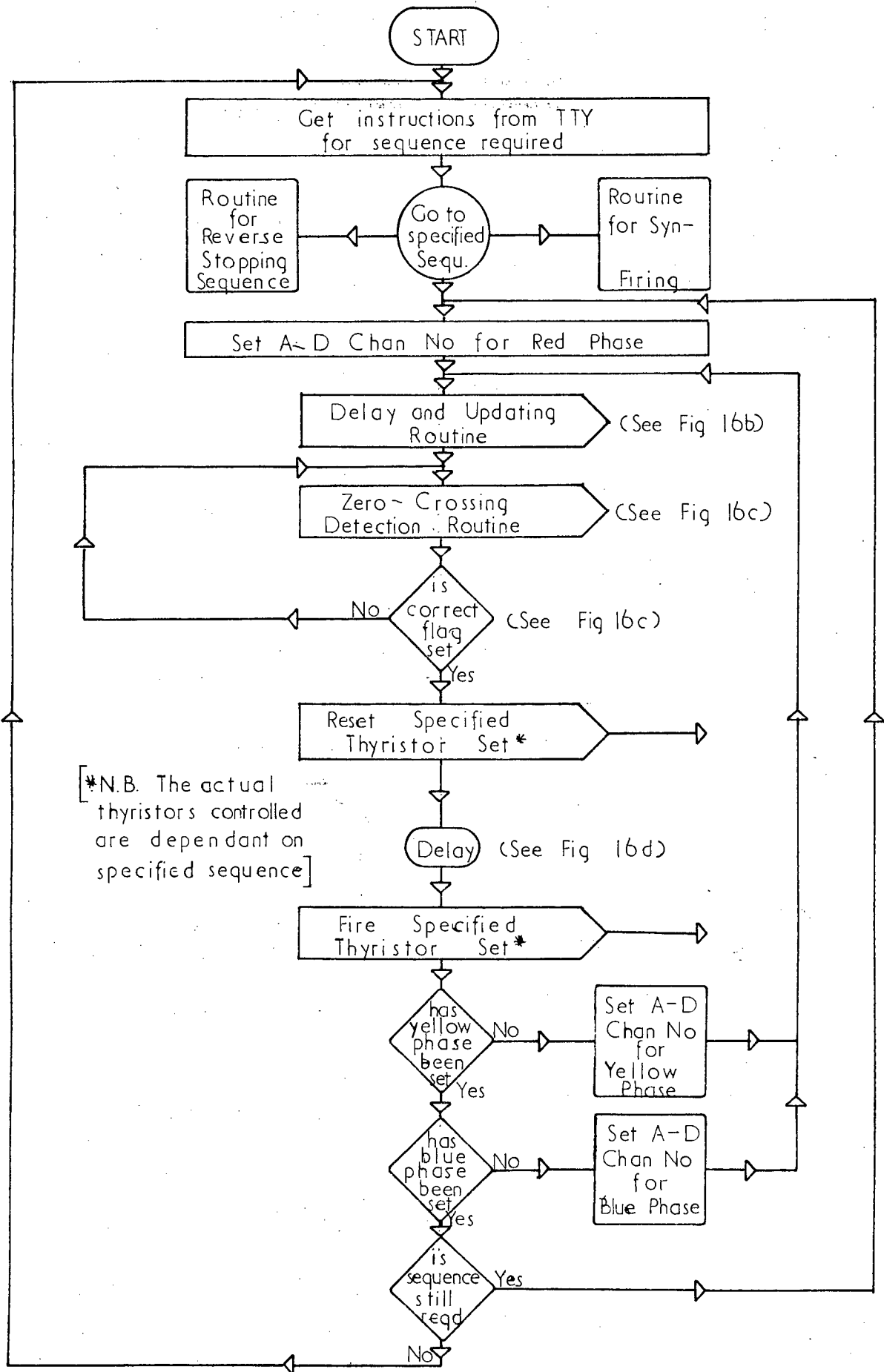
The program has to be able to reset and fire the thyristors in a pre-determined sequence with due regard to synchronization points and required stepping speed. The synchronization, as stated previously, can be taken as the zero-crossing point of the phase feeding the thyristor which is to be reset. However, there is one problem that does emerge. When we step from Red-Yellow and from Yellow-Blue, it can reset the thyristor set on the negative-going crossing-point, fire the next set, and no back-fire (i.e. line-to-line fault) should occur. This can be seen from Fig No: 14 by examination of the directions of the thyristors. But, when the step is made from Blue back to Red, an extra half-cycle must be allowed to go by before we can fire the next set. This implies that we must act on the positive-going zero-crossing point. From this it can be seen that the

zero-crossing routine used in the previous chapters must be changed. (See 6.2).

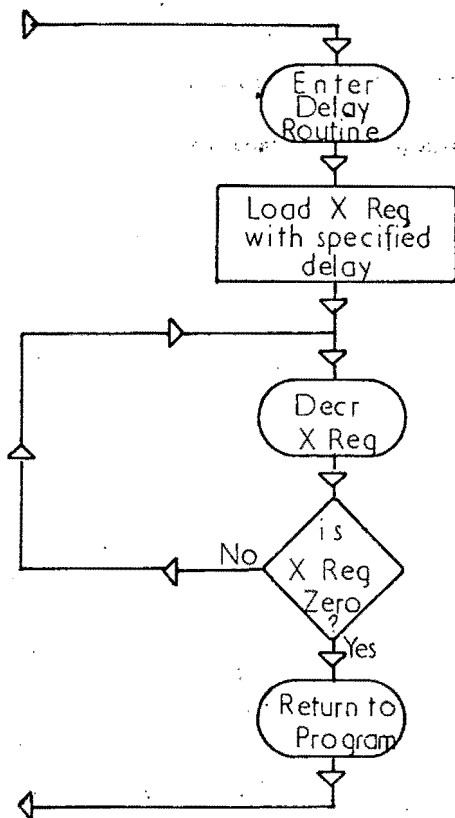
Besides this one complication, the rest of the program requires careful programming to achieve the correct sequential switching, and provision must be made so that the stepping speed and the direction of stepping may be simply and speedily altered. The following sections deal in detail with each block in the overall program.

6.2 Zero-Crossing Routine.

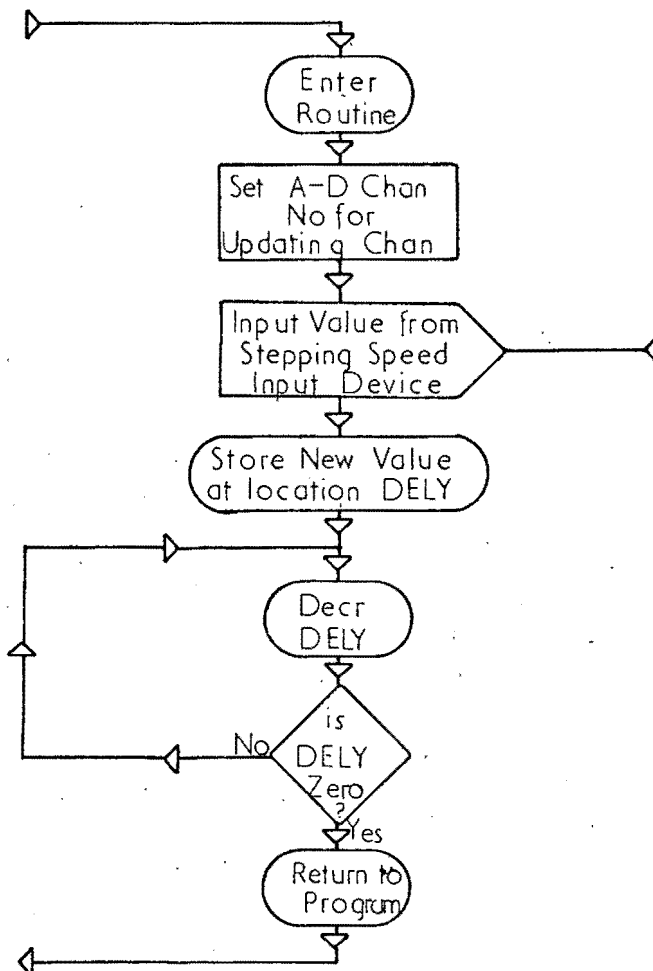
The routine is shown in algorithmic form in Fig No 16(d), and involves a short routine to determine direction of the zero-crossing, which itself is obtained using the routines developed in Chapter II. The direction is determined by first seeing if the value read is positive or negative. The maximum or minimum value is found by comparison of the sampled value with a value that is expected to be the limiting value. After this point has been found, the input is examined to find a zero-crossing point. Thus, by knowing whether the zero-crossing has been found after a positive or negative maximum, the direction of the zero-crossing may be found, and a suitable "flag" set accordingly. In the program this flag may be examined to determine the correct zero-crossing point. The reason for finding the maximum value is that it ensures that the direction is determined correctly, since, as can be seen from the original routine in Chapter II, the zero-crossing is only approximately found because of slowness of sampling, so we could get a case when the first sample is just positive, i.e. +0001, and the next sample, when examined for a zero-cross, could just fall inside the region allowed for a



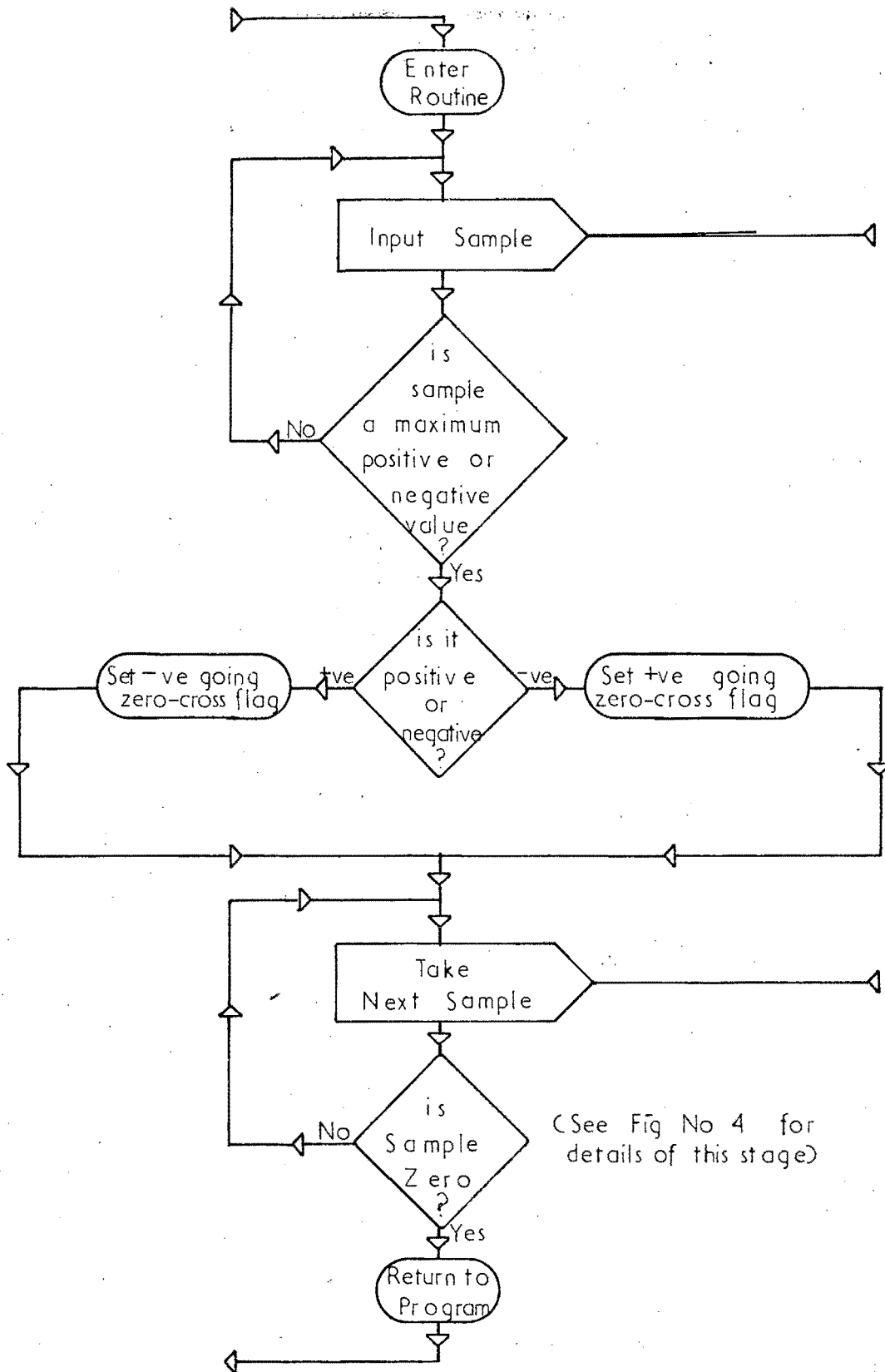
— FIG N° 16 (a): ALGORITHM FOR CONTROL —
 — OF MULTI-THYRISTOR NETWORKS —



- FIG N° 16(b): DELAY ROUTINE BETWEEN RESETING AND -
- FIRING THYRISTORS -



— FIG N° 16(c): DELAY AND UPDATING ROUTINE —



— FIG N° 16(d): ZERO CROSSING DETECTION ROUTINE —

zero-crossing reading. This would then give a false result, i.e. set the incorrect flag.

6.3 The Sequential Switching.

Fig 16(a) gives an overall picture of the sequence required. The order of switching is always the same, and runs in the following steps:-

- (i) Select sequence required.
- (ii) Get correct zero-crossing for Red phase.
- (iii) Reset and fire required thyristor sets.
- (iv) Get correct zero-crossing for Yellow phase.
- (v) Reset and fire required thyristor sets.
- (vi) Get correct zero-crossing for Blue phase.
- (vii) Reset and fire required thyristor sets.
- (viii) Examine required stepping speed and set delay accordingly.
When delay completed, go back to step (ii) for next set of thyristors.
- (ix) At end of six steps check if same sequence required. If no change, continue at (ii). If change order, return to (i).

The selection of sequences is made via a special teletype message which sets the program to run through the switching operations required for that sequence. In the actual program developed, four modes were available: (a) To increase frequency.

(b) To decrease frequency.

(c) To run at synchronous frequency.

(d) To allow the operator to fire any re-

quired thyristors to facilitate testing

In addition, it was found necessary always to start any sequence with the thyristors set to fire at synchronous frequency.

6.4 Delays and Updating Routine.

Basically, two delay routines are required. The first forms part of the updating routine. The required stepping speed is indicated by means of a potentiometer fed into the Analogue-to-Digital converter, as used before to indicate initial conditions in the previous systems. This value is suitably scaled and this scaled value is used to determine the stepping speed by means of a delay. In this, the value stored is counted down in a simple delay routine which holds up the computer before it continues on to the next set of switching instructions, i.e., between each step applied there is a delay set by means of a simple analogue controller. By this means a continuously variable stepping speed may be obtained.

The second delay is one which is not obvious from the outset and is one that in practice it was found essential to include. This delay, of fixed duration, is inserted between each resetting and firing instruction, and covers any backfire which might occur because of the slight inaccuracies which occur when determining the zero-crossing point, since the exact zero-crossing point is not able to be determined by the method of sampling. The necessary duration of this delay was found to be of the order of 800 microseconds.

6.5 Drawbacks and Shortcomings of the Program Developed.

In the program developed there are numerous shortcomings which place immediate restrictions on the control, and it is

a useful exercise to analyse these with an eye to further development. It must always be borne in mind that the system must be a realistic one, and one that can have a practical application. The experimental program falls short of this mainly with regard to time consumption. The routines which involve the use of the Analogue-to-Digital conversions are time-consuming - the continual sampling is wasteful - and such time can be more valuably used in control of other machines, calculations or data-logging. As with the two previous systems, the interrupt system could be used to give synchronization and eliminate the costly sampling periods. Likewise, the stepping-speed indicator should be digital, as will the feed-back.

The second major defect is that no reference is made to the currents flowing - as stated, this is not important in a resistive load, but in a practical situation is of vital interest. A very sensitive form of current detection is required here to tell the computer exactly which thyristor is on or off. This information could be fed to the computer and the program run with reference to these conditions.

The third problem is the fact that the program is purely sequential, and so very high stepping speeds cannot be achieved since the zero-cross of one phase must always be obtained before the next phase can be examined. This is not a serious problem, but is a result arising from the method of zero-crossing detection used. Use of the interrupt system, with the priority interrupt principle being employed, will eliminate this restriction.

To summarise then, the program developed is quite adequate to prove that the system is feasible and practical, provided it is realised that the restrictions were made in its development. To achieve the really flexible situation will require much development in the fields of small current detection, and the improvement of digital feedback techniques.

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CHAPTER VII

PRACTICAL IMPLEMENTATION OF THE DIGITAL CONTROL

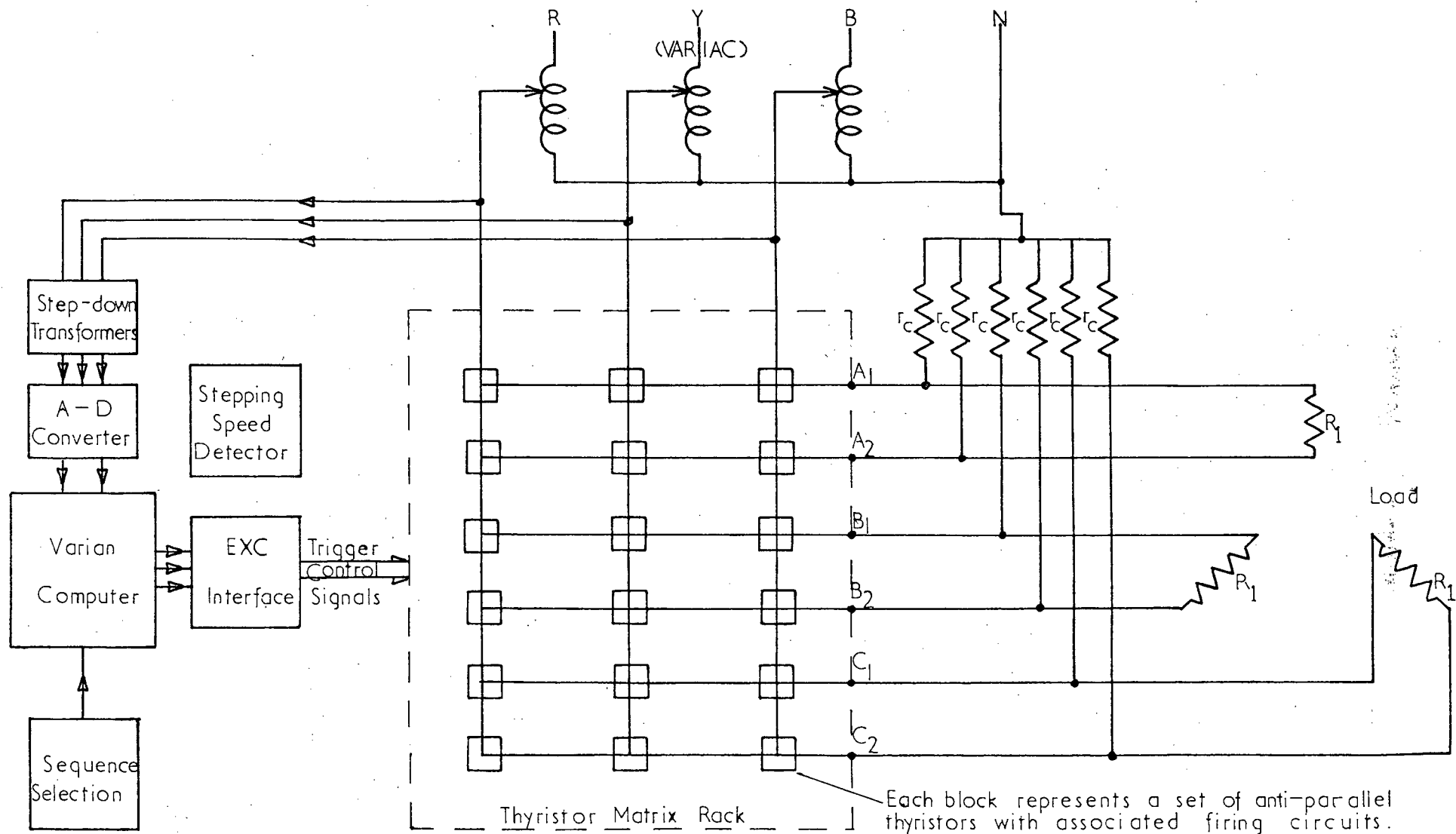
REQUIRED TO PRODUCE TIME MODULATION

This chapter is concerned with the physical layout and construction of the thyristor network, plus the interfacing to the computer, and all associated electronics. It must be noted here that the actual rack was designed by Mr M. Case (See Acknowledgements), and constructed by the Department's workshops. The wiring of the control lines and the final debugging and testing was carried out by the author.

7.1 Brief Description of the Thyristor Rack.

The rack was designed in order that it might be as versatile as possible. The thyristors were the same as those specified in Appendix II, and in order to dissipate the heat generated when running the system at its maximum rating, a large area of heat-sink was required. The solution was found to be the use of sets of cast cooling fins recovered from the power supplies of a scrapped computer. These were then mounted on a frame and connected in the form shown in Fig No 17. With this form of mounting, the unit could be used in any mode, and be used to run machines with current demands of up to 25 Amps per thyristor. Each thyristor set was individually fused, allowing for easy testing, etc.

Between the heatsinks-mounted thyristor in each set was mounted a small length of tag-board, on to which the trigger circuits plus negative slaving coils can be mounted. Again, this was deliberately made very flexible in order that design changes could easily be



— FIG N° 17 : OVERALL THYRISTOR NETWORK CONTROL SYSTEM —

implemented. The control wires for each firing unit were taken out via twisted pairs of P.O. cable to a 32-pin socket. From this outlet twisted pairs ran to the EXC interface.

Finally, the supply was taken off a three-phase variac, and the synchronizing signals fed via step-down transformers (as describer in Chapter III) to the Analogue-to-Digital converter. The loading will be described in detail later.

7.2 Triggering of the Thyristors.

The individual trigger circuits were similar to that shown in Fig No 2, with two changes. Firstly, resistance R_4 may be dispensed with, and secondly the inverter stage is not used. The reason for this is that in order to make the system compatible with the electronic controller being used on the off-line control work, this system had to work off the same logic, i.e. the firing pulses are released when 0 volts are applied to the inhibit, and turned off by +2 volts being applied. This also meant that a slight change had to be made at the EXC interface board, and the output from the flip-flops (See Fig No 1(d)) had to be taken from the \bar{Q} output rather than the Q , i.e. to get the different logic form. This system is, however, undesirable, as it does make the whole system non-fail-safe in the sense that all thyristors will be fired if the controller does not hold their control lines to +2 volts. So the program must ensure that this situation cannot occur, but obviously if the computer is switched off before the power to the thyristors is, or if a control line goes open-circuit, incorrect firing will occur. The system was adopted purely to suit other aspects of the

work using this network - ideally the circuitry used previously, where an inverting stage (Fig 2) is included in the firing control, should be used as this is completely fail-safe.

The EXC interface was dealt with in Chapter I, and besides the one change mentioned above, was found to perform satisfactorily.

7.3 Negative Slaving.

The principle of negative slaving has been dealt with in Chapter VI. However, it was found in practice to present some difficulty. The problem arises through a wide spread in the gate characteristics of the thyristors used. Generally, a coil of inductance .4 H and a Q-factor of 20 is found to provide enough energy with a steep enough voltage front to trigger the slaved thyristor. But in certain cases this is not the case, and it appears that for some thyristors more energy with a faster and higher voltage front is required. One answer is to use coils of a higher Q-factor, with a step-up ratio, i.e. in the form of an auto-transformer, so that a higher voltage is pumped into the slaved thyristor.

The problem with this solution was that it would require a re-design of the coils and this would consume valuable time. So a compromise was reached, simply raising the voltage applied to the coil by inserting a second diode in series with the present one. Obviously, this is uneconomical, but it was merely a compromise in order to get this thesis advanced as quickly as possible - it being the principles and not the practical details which are the subject

concerned here.

7.4 Loading of the Network.

In order to provide an overall check of the system from the point of view of hardware and software development, the rack was run on to a purely resistive load. The applied voltage was about 70 volts (phase) and the loads determined from this. Firstly the main load, which replaces the normal machine winding connections, was set to 500 ohms, with a suitable dissipation rating (this is R_1 in Fig No 17). Secondly, and this applies more so in the case of inductive loads, it is essential to provide each thyristor with a small current to fire on when it is turned on, as there may not be enough current flowing through the thyristor to latch it (since the thyristor requires a minimum current to fire on, called the "latching current", See Ref 6). This current may be provided by a suitable resistance (r_c in Fig No 17) connected from each output A_1 , A_2 , B_1 , etc, to neutral. The latching current of the thyristors used is of the order of 40 mA, so r_c may be set to 1000 ohms.

7.5 Protection of the Thyristors and Computer.

The firing circuits ensure that the computer is isolated from any large power elements, and provided the insulation on the pulse transformers is adequate, there is virtually no chance of high voltage A.C. getting on to the EXC interface, and hence into the computer. The synchronizing signals are protected from overvoltage being applied to the Analogue-to-Digital converter by zener diodes, as is the input from the stepping speed indicator.

The thyristors are naturally an expensive item, and must be fully protected. As stated before, each set is fully fused, and in the early test stages these fuses were set so that they would blow at any current above the expected one. With the loading outlined above, the maximum current should be just about .9 Amps, so fuse wire with a rating of 1.1 Amps was used, the principle being that any line-to-line fault would cause this small fuse to blow, and protect the thyristors. In practice, this scheme works fairly well and is useful for initial testing. Once the program had been verified, the fuse rating was increased so that variations in loading, etc, could be made to test the system fully.

One point which was not catered for, was the reduction of transients which occur when the thyristors are turned on and off (See Ref 18), for example, the reverse recovery charge. Such effects are likely to cause spurious firing, etc, in other thyristor sets, especially when operating on inductive loads, but on the present system caused no ill-effects. These may, however, be reduced by an RC network connected across each thyristor.

The question of pick-up and interference from the power side on to the control lines was investigated, and the answer lies in keeping the control wires well away from the power sections, and in the use of twisted pairs. In this way, there was no noticeable interference. The actual control lines were brought out of the front of the rack and simply strung together in self-supporting trees.

One final problem that will always occur is that any

switching transients which can occur on the computer's supply when associated equipment is switched on or off, say a large machine at the other end of the laboratory, can get into the computer and feed rubbish into its memory. In practice this proved to be rather a nuisance, but could only be eliminated if the computer was run off a completely separated and isolated supply. However, at present this remains an inherent potential danger.

7.6 General Instrumentation.

As this was an experimental system, instrumentation was not of vital importance, the most important instrument being a storage-oscilloscope. As the waveform produced is not repetitive, this presents triggering difficulties in the oscilloscope, so that the storage facility is vital. Current waveforms are easily observed by means of series connected shunts. Ammeters were connected in the incoming lines to provide a monitor of the currents being drawn. In order to produce meaningful waveforms, an ultra-violet recorder was used, and this aspect will be dealt with more fully in the next chapter.

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CHAPTER VIII

RESULTS AND CONCLUSIONS ON THE CONTROL OF THE THYRISTOR NETWORK.

In the preceding chapters the development of the hardware and software necessary to control the thyristor network to perform time modulation, has been fully described. It remains now to give an account of the results obtained on tests run with this system, and then to analyse these results, remembering that the system must have some practical feasibility.

8.1 Practical Difficulties and Initial Impressions.

One of the greatest problems when running the system for the first time is the setting-up of delay routines, scaling factors, etc, and the fact that the rack is not fail-safe - any wrong step will normally end with a series of blown fuses. (Preferable to blown thyristors, though!) So the first two objects were to ensure that both sides of the system were independently functioning correctly. The program may be checked and (debugged) quite simply, as the EXC interface can be isolated from the trigger circuits, and the Analogue-to-Digital converter can be fed directly off the three-phase supply. Using a multi-trace oscilloscope, the various pulses produced by the EXC interface may be examined with reference to the A.C. supply, and the program checked completely in this manner. Scaling factors relative to stepping speed settings may be set at this stage, as well as lengths of some of the delay routines. The delay routine between resetting and firing pulses is best estimated, and the optimum determined, at a later stage.

The operation of the thyristors and their associated firing circuits may easily be checked out, this being one rather dubious advantage of the control system, since when the interface is disconnected, all trigger circuits are enabled. So to check each set, its corresponding fuse just needs to be inserted! In fact, this debugging process proved to be a major time-consuming aspect, due mainly to the variations in gate characteristics. (See Chapter VII for comments on negative slaving problems)

Once these two sections had been verified, the system as a whole could be run, starting with the control set to step at a very slow stepping speed. Generally, from this stage onwards little difficulty was experienced with the system, and long tests could be carried out with the computer in complete control. As expected, with a resistive load, little trouble was experienced with back-fires. The next sections deal with the gathering and analysis of results.

8.2 Processes involved in the System Verification.

The first question that must be asked is, "what will prove that the system is successful?", i.e., "what are the important criteria for system verification?". Two criteria seem vital.

- (i) Does the system carry out its designed functions?
- (ii) Is the computer able to control the system continually over a long period? i.e. Is the system stable?

The second of these can only be of importance, of course, if the first criterion is true. So the system must be run up and the output examined, and then the system must be run continuously for a lengthy period, after which the output must be examined,

and compared to the first output viewed.

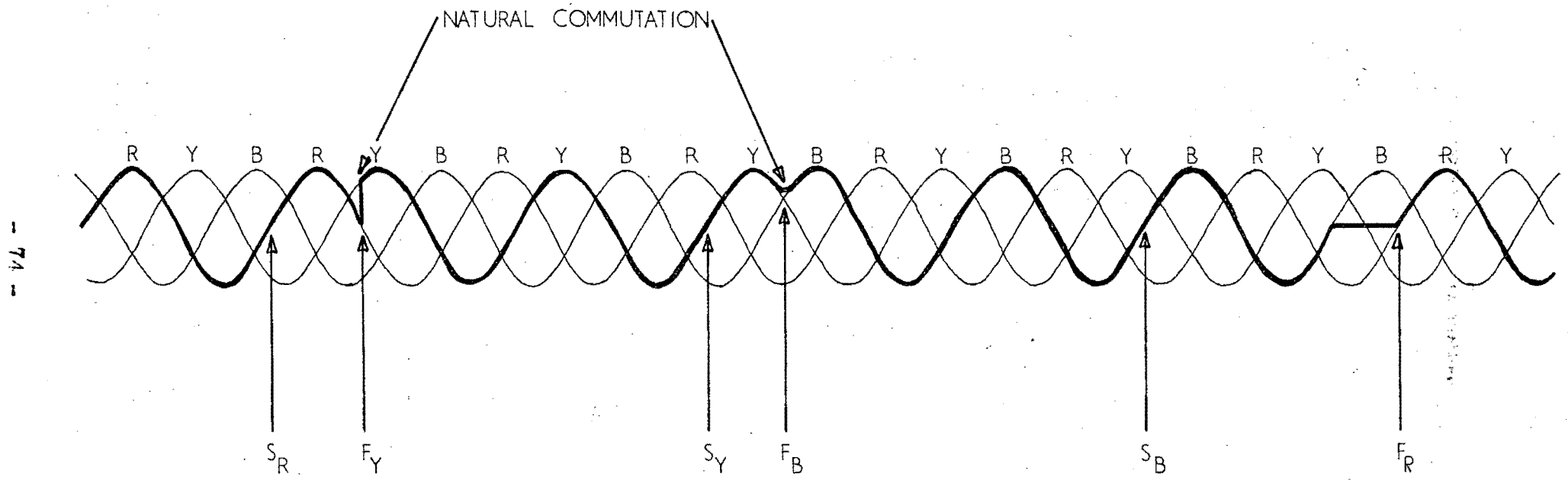
In order to view the output, a storage oscilloscope is adequate, but for a permanent record the ultra-violet pen recorder is needed, plus, of course, being multi-channel. The connection of this to the system is fairly simple using series shunts for current observations and potential-divider networks for voltage waveforms.

Once it was verified that all three loads were performing in exactly the same way, attention was devoted to one load, and three aspects were recorded and compared, i.e. phase voltage, voltage across load, and load current. It was found that the system was reliable and variable from a maximum stepping speed of 48 steps per second up, and down to a stepping speed of one step per minute. This would give rise to a frequency variation of 42 Hz to 58 Hz. In an application to an induction motor with four poles, the speed variation would amount in theory to a speed variation of approximately 1260 to 1740 r.p.m. . This is not a very great range, but it must be realised that this has two significant facts:-

(i) Continuous variability.

(ii) Range is restricted only by software. This can definitely be improved by elimination of the present Analogue-to-Digital means of synchronization.

Also, it has been found in practice that in fact this range is easily obtained by the method of time-modulation, and any greater variation produces many other complications.



— FIG N° 18: PREDICTED WAVEFORM AT ONE END OF LOAD WITH REFERENCE TO NEUTRAL —

8.3 Analysis of Traces for Verification of the System.

(See Figs 19 (a), (b) and (c).)

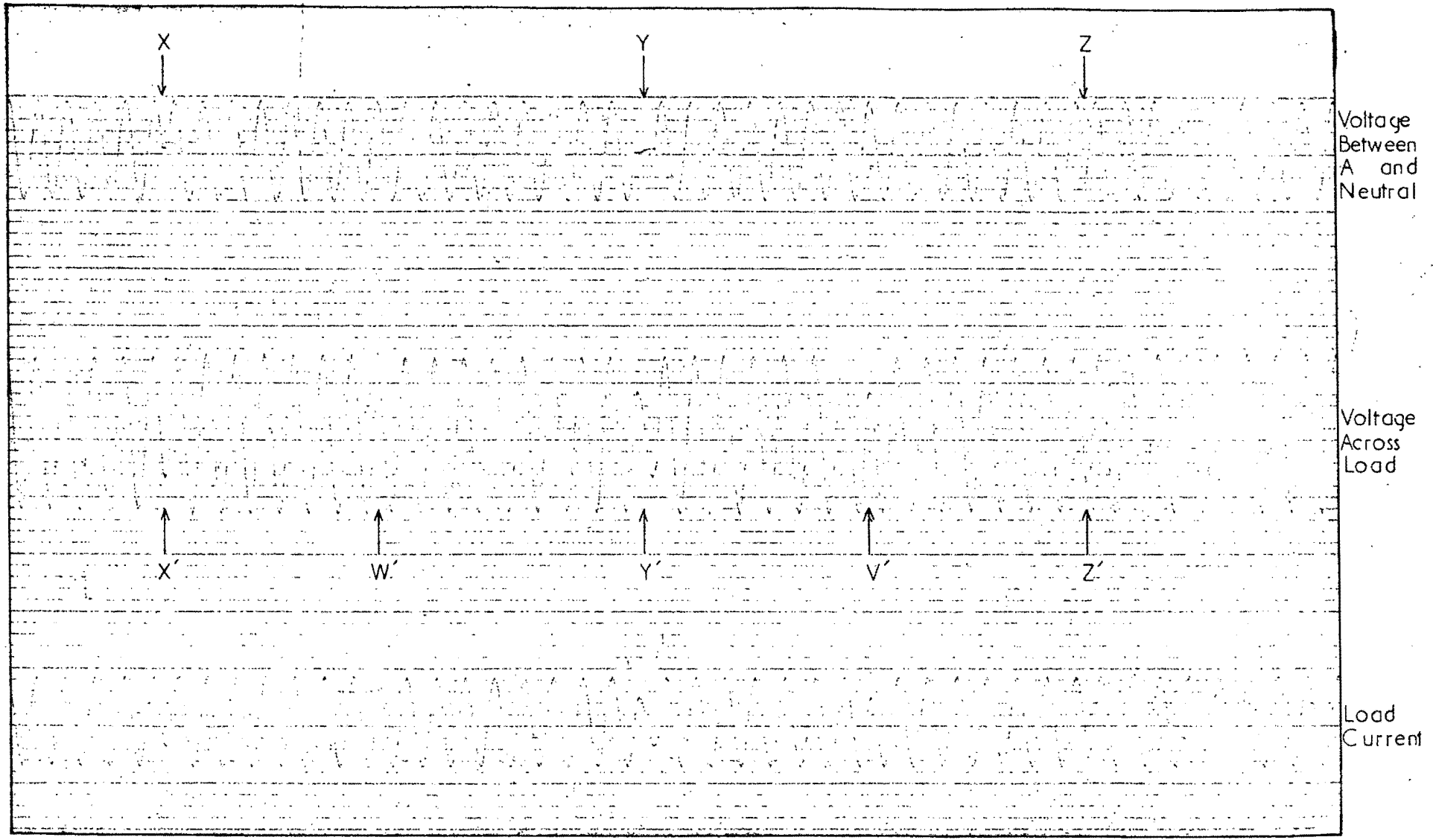
At first sight the traces obtained from the ultra-violet recorder appear to be rather strange, and in order to make some sense of them, it must be determined what sort of trace is, in fact, expected. An examination of Fig No 18 will supply the answer to this.

In this figure two important points must be kept in mind

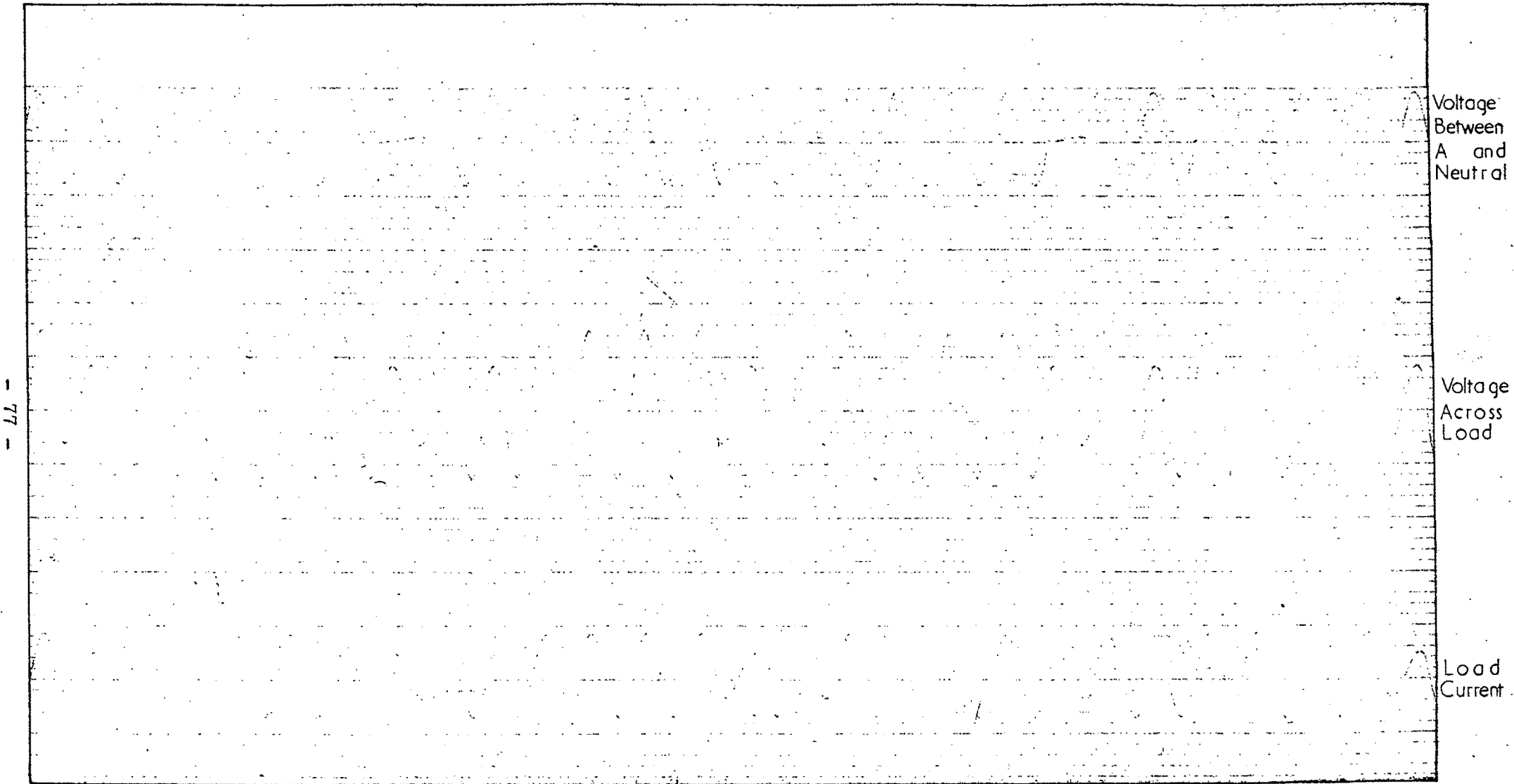
- (i) Natural commutation may occur between Red and Yellow, and between Yellow and Blue.
- (ii) When a transition is made back from Blue to Red, an extra waiting period must be allowed because of the direction of the thyristors (See Fig No 14).

So now, referring to Fig No 18, the following sequence occurs:-

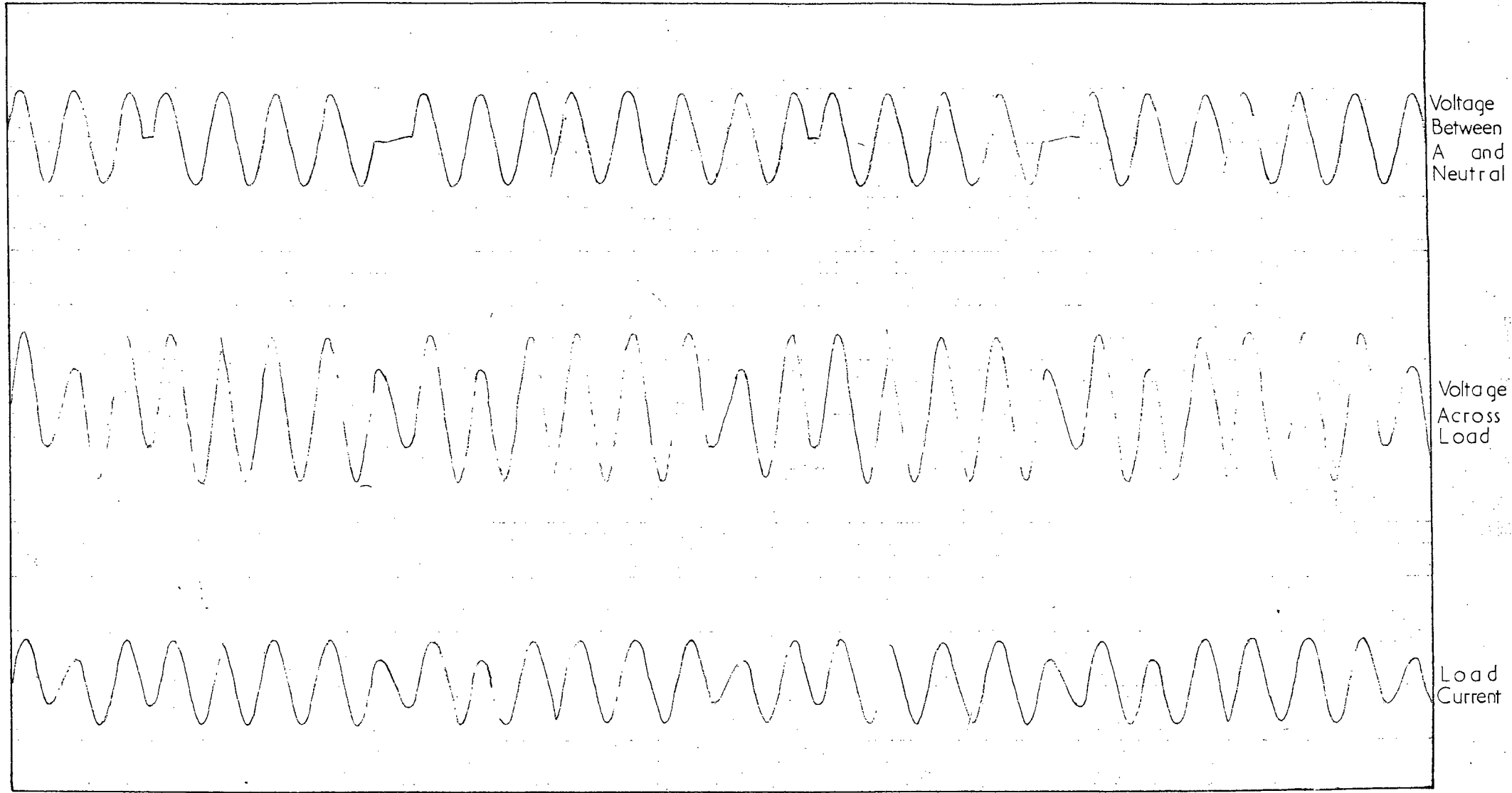
- (i) Synchronize with Red phase at point S_R , reset Red phase thyristor and fire Yellow phase set. Natural commutation occurs as demonstrated. Exact point of firing of Yellow, F_Y , depends on delays allowed, etc.
- (ii) Synchronize with Yellow phase at point S_Y , reset Yellow phase thyristor, and fire Blue phase set. Natural commutation occurs.
- (iii) Synchronize with Blue phase at point S_B , reset Blue phase thyristor, but wait for negative half cycle to complete its conduction period before firing Red phase. Hence the period of zero voltage will occur.



— FIG N° 19(a): WAVEFORMS FOR SLOW STEPPING SPEED : $f_{out} = 45 \text{ Hz}$ —

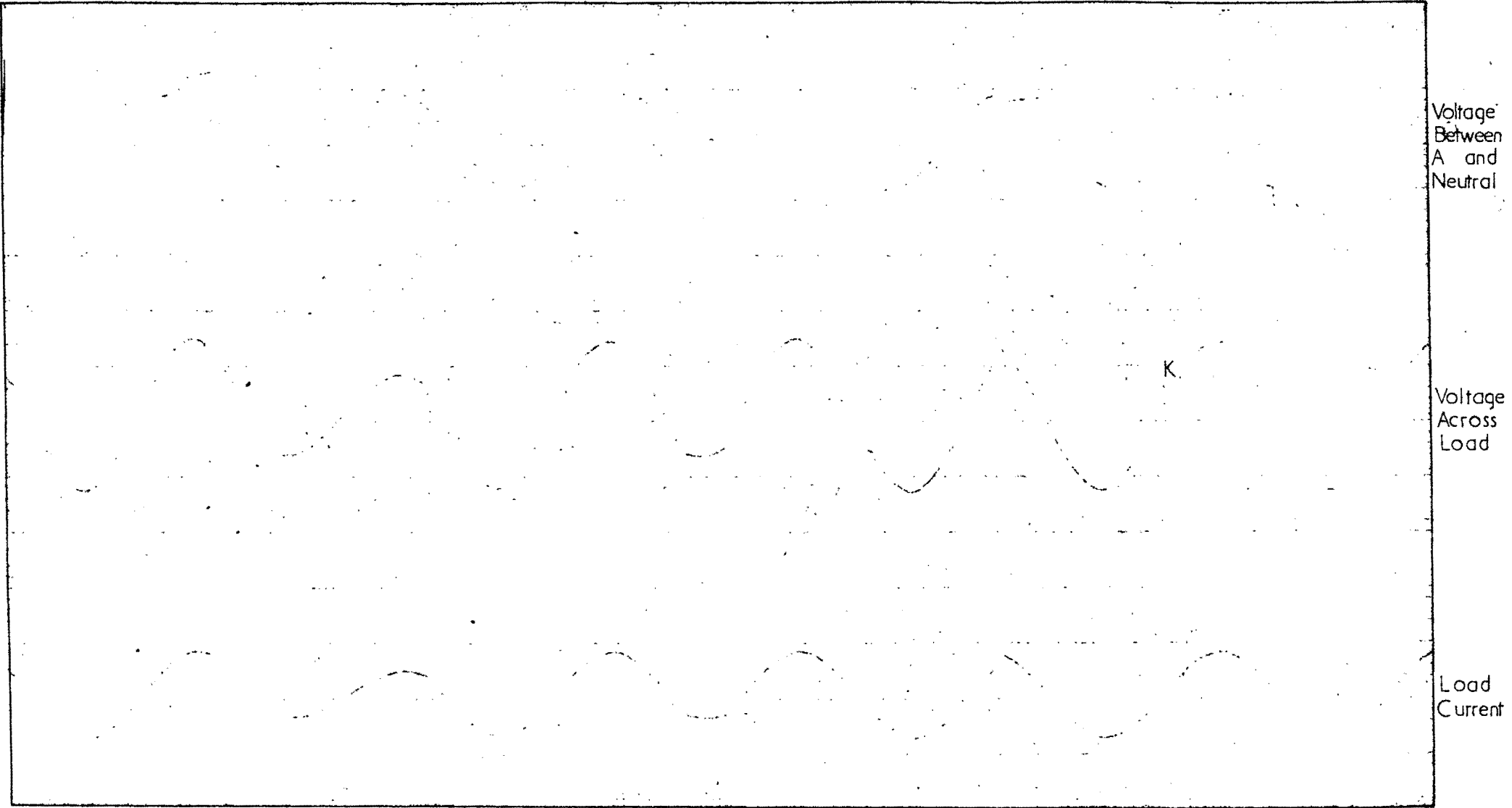


— FIG N° 19(b): WAVEFORM FOR FAST STEPPING SPEED : $f_{out} \approx 45 \text{ Hz}$ —



(TOUCHED UP FOR CLARITY)

— FIG N° 19(b): WAVEFORM FOR FAST STEPPING SPEED : $f_{out} \approx 45 \text{ Hz}$ —



— FIG N° 19 (c); EXPANDED WAVEFORM FOR FAST STEPPING SPEED —

So careful observation and understanding of the sketched three phase diagram will present the typical waveform that is expected at one end of the load when referred to the neutral.

Now the next step is to analyse the actual waveforms obtained. It must be clearly understood that in observing the waveform across the load, the effect of the above sequence is now applied to both ends of the load, and the load voltage is the overall effect, considering that each end is switched in sequence as described.

Fig No 19(a) shows the waveforms obtained for a relatively slow stepping rate. This trace clearly illustrates the effect on one side of the winding relative to neutral. In the upper curve, points X, Y and Z are equivalent to points F_B , F_R and F_Y in the sketch on Fig No 18. The similarity proves that the output is as predicted. The centre trace is the voltage appearing across the load - this reflects the effects of the stepping and produces an output frequency of approximately 49 Hz. The current trace, of course, just follows the voltage because of the resistive load.

Fig No 19(b) shows similar traces obtained for a higher stepping speed - the approximate output frequency is 45 Hz, i.e., stepping at 30 Hz. The characteristics are the same as expected. One point to demonstrate is that there are regions when the voltage swing across the load is greatly reduced. It is due to the difficult transition between Blue and Red, where one side of the load has zero volts applied to it, with, of course, a resistive load to neutral.

Fig No 19(c) shows the same settings as in Fig No 19(b) except that the trace has been greatly expanded by increasing the paper speed of the recorder. The various transitions are clearly shown here. Slight irregularities in the traces at points such as K are caused by the slight delay between firing pulses being applied, and the thyristor actually firing.

8.4 Conclusions on the Control of the Time Modulation

Thyristor Network.

It is not intended to give a critical appreciation of the practicalities of time modulation. There are obviously many points to be investigated, and its usefulness as a method to control an A.C. machine has still to be fully examined. It has been the intention of the author to present a unique method to control the electronics needed to produce time-modulation, and the results must be examined in this light.

It has been positively demonstrated that such a control scheme ^{can} (is able to) be implemented, and the hardware and software have been shown to be satisfactory. This is clearly demonstrated by the traces taken - the predicted results have in fact been confirmed under test conditions. There appear now to be two uses of this scheme. Firstly, it can be used for the absolute control of machines. Secondly, it may be used as a tool in the future research into the applications of time-modulation, since sequencing, timing, etc, may easily be altered without the necessity of producing new electronic hardware. The whole field may now be fully investigated, and possibly many defects or advantages may come to light.

As for the work done so far, there seem to be many avenues for improvement. Firstly, the synchronization times must be queried. Observations made of the traces produced suggest that there are far more favourable switching points which, if used, could produce a waveform which is far smoother, and free from discontinuities. In this way, many harmonics which are obviously present in the waveforms obtained, may be reduced or completely limited. This means ^{? eliminated} that the zero-crossing synchronization is therefore not desirable. Thus, if the computer were fed with more information from the actual thyristor bank, it could select the most suitable switching points.

The question of line-to-line faults must also be carefully considered. One view is that there is a statistical probability of these occurring, and the thyristors must be selected to cope with them. But it does seem possible that if synchronization firing points could be more carefully selected, these effects could be reduced to a minimum. Incidentally, if the computer were to carry out the sequence selection and not run under such strict program control, it would make the computer more suitable to be able to control more than one machine, as is desirable in a practical system.

The rate of stepping has been purely under the control of the operator. In a practical situation this would be based on information fed-back from the system, i.e. would completely close the loop. The situation that could arise is that the system might need to be run so slowly that time modulation control would cease to be capable of producing such a low frequency signal. This would require the computer now to fire the thyristors to produce a cycloconverter sys-

tem. Memory capabilities would allow this, but very complex programming would obviously arise.

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CHAPTER IX

OVERALL REVIEW OF DIRECT DIGITAL CONTROL OF THYRISTOR NETWORKS.

The objects of this thesis were outlined in the introduction, and the step-by-step development has been set out in the preceding chapters. In this chapter a broad view of the whole concept is taken, with special regard to the feasibility and practical application of such a form of control, as indicated by the results obtained.

Generally, the aim of this thesis has been achieved in that hardware and software have been developed to control, by means of an on-line digital computer, various configurations of thyristor networks. In most cases, only one possible configuration was controlled, but, especially in the case of the large time modulation network, many other configurations are possible. It may easily be seen that such a network may be fed off D.C. to perform the function of an inverter, or off A.C. to become a cyclo-converter or a straight three-phase bridge rectifier. For all these configurations, the basic hardware is the same as has been constructed, and the problem remains purely one of software. It is important to remember that to allow full control of the network as laid out, the idea of negative slaving must be dropped and control, by the computer, must be obtained for all 36 thyristors. This would require either another set of flip-flops and additional decoding, or the two outputs Q and \bar{Q} must be utilised and used to set separate flip-flops which are reset by some overall instruction. This might be of some advantage as it would ensure complete resetting before the next firing group is operated, and will

lead to a slightly more safe and back-fire-free system.

It is very significant that there is relatively little published work on these topics (See Reference List). One important reason for this is that it is obviously not economical to use an extremely costly computer to control one network and hence one machine. The future obviously lies in the integration of the computer into the control of a multi-thyristor system, where the computer controls numerous machines which react with each other, and also performs other menial tasks such as data-logging, etc. In case of an alarm, the computer could undertake any protective action required.

Similar such schemes have been employed in industry, but at present most of them involve a large percentage of Analogue-to-Digital and Digital-to-Analogue conversions, and are not strictly digital controllers in the sense used in this thesis.

In general, the control of D.C. machines appears to be, as indicated by results obtained, relatively straightforward, and very feasible as so little of the computer's time is taken in actually performing the control functions. As stated previously, as an offshoot of this thesis, work has progressed on the control of more than one machine by one central computer. To make such a system useful practically, much of the wasted computer time must be eliminated. Several ways of achieving this are apparent. Firstly, all forms of Analogue-to-Digital conversions using conversion hardware must be eliminated. These may be replaced by the use of a digital tachometer, use of the interrupt facility of the computer, and reducing the num-

ber of synchronization points by means of a hardware Real-time clock. Secondly, any large amount of data-handling must be carried out using direct memory access. And all alarms would, as is presently being carried out, use the priority interrupt inputs. These methods would also largely reduce the number of costly peripherals, which, as most computer users have found to their dismay, amount to a large percentage of the total cost of the system.

The latter section of this thesis has dealt with the application of the digital computer to the control of thyristor networks to perform time-modulation. This really throws the field of speed control of induction motors into the hands of the digital computer system. From the comments in the last chapter it will be realised that there is a lot of work still needed in this field, but the progress via experiments carried out has shown that the principle of computer control of large A.C. machines is feasible without having to go through the usual step of conversion to D.C. and then the use of an inverter. One point worthy of note is that, for very large machines, the cost of the computer controlled system could be considerably less than the present systems being used.

As mentioned previously, it would be of great economic interest to eliminate the Analogue-to-Digital converters, and to go directly into the computer in digital form. Conventional digital shaft encoders tend to be limited in their resolution at high speed, and the work on time modulation has indicated that it would be greatly advantageous if the computer knew the exact state of each thyristor and the exact position of the rotor. So this would require accu-

rate current detections (or, in fact, any means of determining what the state of a thyristor is), plus an extremely accurate means of digital feedback. From these parameters, the computer could decide its optimum switching sequence in relation to the overall system.

With the state of the art as it is at the present, then, it can be clearly stated that direct digital control of thyristor networks is a successful means of control, but from an economic point of view, the computer must be the heart of a complex of networks controlling a complete system. Once this point is reached, then direct digital control becomes an economic prospect.

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APPENDIX I

THE VARIAN DIGITAL COMPUTER.

A full description of the computer system used may be found in Reference No 4. However, in order to provide the reader with a brief outline of this system, the following section has been included. The computer used for the purposes of this thesis was a Varian Data 620/i Digital Computer, which is a small, modern, system-oriented machine, and which can be employed for special digital and hybrid applications as well as for general computational use. The model used had the following notable features:-

- (a) 8,192, 18-bit words of memory.
- (b) 1.8 microsecond cycle time, i.e., the time to bring an instruction from memory, act upon it, and replace it.
- (c) Fast reader and punch facilities - the computer working on a paper-tape system.
- (d) Analogue-to-Digital Interface provided (See later note).

I.1 Organization.

The organization of the Varian is typical of a modern small computer, and basically provides 9 registers, three of which are directly accessible for data handling (These are referred to as the A, B and X registers), plus a fairly unique Bus structure by which information is routed via parallel communication paths. The "E-Bus" is particularly important as this is the bus which is externally accessible and on to which interfacing equipment such as the Analogue-to-Digital converter, and the special EXC interface, is con-

ected. The E-Bus is a parallel bus which carries each bit in a selected word, which may be placed on it via an input/output instruction or an External Control Instruction, as well as various control pulses and voltage rails (See Appendix Table No 1 of E-Bus connections).

In addition, the Varian has a Direct Memory Access Facility and a multilevel priority interrupt system.

I.2 Interfacing.

As mentioned previously, interfacing equipment is connected directly on to the E-Bus. Two important interfaces were used for the work in this thesis. The first is the Analogue-to-Digital interface, which was supplied with the computer and constructed locally. This consists of a 10-channel multiplexer module, a sample-and-hold module, an Analogue-to-Digital converter, and various decoding networks and buffers. The programming of the Analogue-to-Digital Converter is simple:-

- (a) The channel is selected by placing a suitable selection "mask" on the E-Bus.
- (b) This opens the selected channel, which is then connected to the sample-and-hold module.
- (c) After a suitable settling time, the sample-and-hold is frozen by an external control pulse, suitably addressed. This also starts the Analogue-to-Digital module converting.
- (d) The Analogue-to-Digital module is sensed for a signal which indicates that the conversion is completed. When this signal is received, the digital value is transferred into the selected register or memory location.

The Analogue-to-Digital converter has a range of +10 volts to -10 volts, and gives an 11-bit-plus-sign-bit digital equivalent, i.e. 3777_{octal} is equivalent to 10 volts. The accuracy is 4 millivolts.

The second interface is the EXC interface, which was designed and constructed for the specific needs of this thesis. See Chapter I for details.

I.3 Control of the Computer.

As with all digital computers, the Varian 620/i has its own machine-code, with the following specific features:-

(a) Addressing.

- (i) Direct addressing of 2,048 words in memory.
- (ii) Relative addressing (Relative to program counter, X or B Register)
- (iii) Multi-level indirect addressing, i.e. finding a new address at the address specified.
- (iv) Immediate and Extended addressing.

(b) Instructions.

There are both single and double instruction words used, with over 100 standard commands and many other macroinstructions. The instructions are as follows ; Load, Store, Arithmetic, Logical, Jump, Jump and Mark, Execute, Immediate, Input/Output, Register Change, Logical and Arithmetic Shift, Control and Extended Addressing.

(c) Programming (See Ref No 4)

The computer has available a compiler (or assembler) software

package, referred to as "DAS". This is a relatively simple autocode language, and the general format may be seen in the programs referred to in Appendix IV. It is basically a language in which all machine code instructions, addresses, constants, etc, are given a simple and meaningful mnemonic format. Source programs are written in this language, and the compiler program is used to "compile" the object program, which is finally placed by the paper-punch on to paper tape. In the process of compilation, a full listing is obtained. (See App 4)

Note: (i) The widely-used autocode "FORTRAN" may be used on this computer, but, for on-line purposes, it is far easier to use the "DAS" coding which is so similar to the actual machine code of the computer.

(ii) In the listings given by "DAS", the first column of figures contains the location in memory where the machine-code instruction, listed in the second column, is stored when the program is loaded into memory. The rest of each line contains the source program data.

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<u>Line:Function</u>	<u>Line:Function</u>	<u>Line:Function</u>	<u>Line:Function</u>
1 GRD	22 GRD	43 SYRT -	
2 EBOO -	23 EB16 -	44 IUAX -	
3 GRD	24 GRD	45	115
4 EBO1 -	25 EB17 -	46	116
5 GRD	26 GRD	47	117 -5V
6 EBO2 -	27 FRYX -	48	118 +5V
7 GRD	28	49 TROX -	119 -12V
8 EBO3 -	29 DRYX -	50 TROX -	120 +12V
9 GRD	30 GRD	51	121 +5V
10 EBO4 -	31 SERX -	52	122 =100
11 EBO5 -	32 GRD	53 GRD	123 -5V
12 EBO6 -	33	54 CDCX -	124 -5V
13 EBO7 -	34	55 GRD	125 +5V
14 EBO8 -	35	56 DCEX -	126 +5V
15 EBO9 -	36	57 GRD	127 -12V
16 EB10 -	37	58 TAKX -	128 -12V
17 EB11 -	38 GRD	59 GRD	129 +12V
18 EB12 -	39	60 DESX -	130
19 EB13 -	40 GRD	61	
20 EB14 -	41	62	
21 EB15 -	42		

APPENDIX TABLE NO 1: E-BUS CONNECTIONS.

APPENDIX II
NOTES ON THE THYRISTORS USED
IN THE SINGLE-PHASE AND THREE-PHASE SYSTEMS

It must be noted that the thyristors used in the last application described, i.e. the speed control of the induction motor, were part of an existing arrangement designed and constructed as part of Mr M.Case's Ph.D. thesis (See Ref. 8), and no design details are dealt with in this thesis. For the earlier applications the principal details of the thyristors used are as follows (For full details see Ref. 7):-

Thyristor Specification

Type	:	R.C.A. 2N3899
Peak Reverse Voltage (Repetitive)	:	600 volts
Peak Forward Blocking Voltage (Repetitive)	:	700 volts
Forward Current: Avg D.C. at conduction angle of 180°	:	22 Amperes
RMS Value	:	35 Amperes
Peak Surge Current (for one cycle max.)	:	350 Amperes
Rate of Change of Forward Current, $\frac{di}{dt}$:	200 Amperes/Microsec.
Gate Power: Peak for 10 microsec duration	:	40 Watts
Average	:	0.5 Watts

Triggering Considerations.As stated before, triggering by means of unijunction transistor oscillators was chosen. Pulse triggering of this form is very convenient and, as can be seen, lends itself to automatic control via the computer. Pulse triggering can also accommodate the wide tolerances in the triggering considerations, as the trigger can overdrive the gate without any harm.

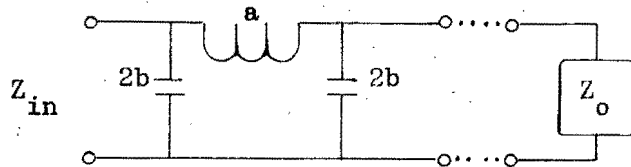
As mentioned, provided the frequency of the pulses is not too high, the power level is relatively small, as the condenser charges up relatively slowly and discharges very rapidly. This leads to the large, high-current thyristors' being controlled by very low-powered and simple devices. Design criteria may be found in Ref. 6, pp 73 - 79.

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APPENDIX III

See Ref. No 15. Referring to Fig No 7, if we assume that the filter is correctly terminated, the input impedance, Z_{in} , is equal to the characteristic impedance, Z_o . Obviously, if Z_o is real, the filter will absorb real power, and if Z_o is imaginary, it may not pass real power. So all the power supplied to the filter is passed if Z_o is real, and rejected if Z_o is imaginary. The cut-off frequency occurs when Z_o changes from real to imaginary.

Considering the Π network used, if we use the following symbols, the expression for Z_o may easily be deduced, viz :



So $Z_{in} = \frac{a}{2} + \frac{b(\frac{a}{2} + Z_o)}{b + Z_o + \frac{a}{2}}$ - Derived by considering the network as parallel and series impedances.

Now, by definition, $Z_{in} = Z_o$.

Therefore $Z_o = \sqrt{ab} \sqrt{1 + \frac{a}{4b}}$

Now, replacing a by $j\omega L$ and $2b$ by $\frac{1}{j\omega c}$,

We get $Z_o = \sqrt{\frac{L}{2c}} \sqrt{1 - \frac{\omega^2 Lc}{2}}$

From this it is clear that the expression is real when $\frac{\omega^2 Lc}{2} < 1$ and that the cut-off frequency occurs when $\frac{\omega^2 Lc}{2} = 1$.

So if we choose $L = 20 \text{ H}$ (at a designed current of 25mA), and let the cut-off occur at about 5 Hz (very low since we are interested only in the D.C. level, and from measurements made, this frequency appears to be of the order of the lowest ripple frequency - this frequency being dependant on the speed of the machine),

if $f = 5 \text{ Hz}$, therefore $\omega = 10\pi$.

$$\text{therefore } c = \frac{2}{L\omega^2} = \frac{2}{100\pi^2 \times 20}$$

$$= .1 \text{ mfd.}$$

Thus, choosing these values will give a filter which will have a very low cut-off, as required, but unfortunately, as can be seen, a high time-constant. The latter is undesirable, but is a necessary evil because of the very bad waveform given by the tachogenerator.

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APPENDIX IV
COMPUTER PROGRAMS.

In order to make this thesis more readable, it was decided not to include any of the actual programs developed. The flow charts give the general outline, and these may be applied using whatever computer language is available. As stated in appendix I, the programs were written in "DAS", the assembler language of the Varian computer. The actual programs are kept in the program library of the Department of Electrical Engineering at the University of Cape Town, and are available for inspection. These programs give a full listing of each control configuration, plus the machine-code equivalents.

The programs housed are as follows:-

- (a) Program to ~~control the~~ firing angle of a single phase, one thyristor system, with reference to initial conditions only.
- (b) Program to implement voltage control of a three phase, half-wave thyristor network, with reference to initial conditions only.
- (c) Program to implement speed control of a D.C. machine, separately excited, working in a closed loop, with speed set by external controller and voltage applied to armature controlled to minimise error between set speed and speed as indicated by tachogenerator feedback.
- (d) Program to control a multi-thyristor network to produce an output frequency of one of three forms, i.e.
 - (i) At input frequency.
 - (ii) At frequencies greater than input frequency.
 - (iii) At frequencies less than input frequency.

(Both (ii) and (iii) are continuously variable, the fre-

quency being determined by an external controller.)

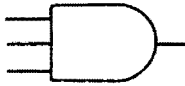
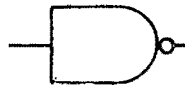



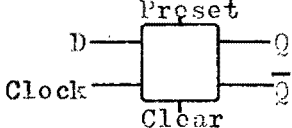

- (e) A special debugging routine applicable to the multi-thyristor network, in which any sequence of thyristors may be selected, delays set, and positive and negative zero-crossing points specified. These instructions are entered in simple mnemonic forms via the teletype. This program is referred to as the "Thyristor Aid Program", and is used to run experimental systems and to perform debugging routines.
- (f) All sub-routines used throughout this thesis are also available for general usage.

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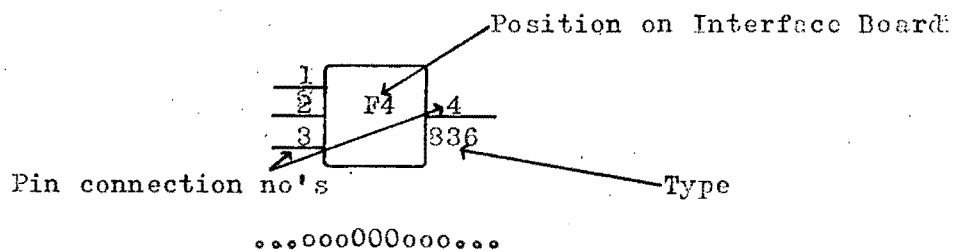
APPENDIX V

LOGIC SYMBOLS USED THROUGHOUT THIS THESIS.

In the various logic diagrams contained in this thesis the following set of symbols has been adopted:-

<u>FUNCTION</u>	<u>SYMBOL</u>
AND	
NAND	
BUFFER AMPLIFIER	
NOT	
WIRED AND (FEATURE OF DTL LOGIC)	
FLIP-FLOP D-TYPE, EDGE-TRIGGERED	
INPUT/OUTPUT FROM EDGE-CONNECTOR	

In addition, the following system of notation is used:-



APPENDIX VI.

SELECTION OF EXC CONTROL LINES.

The following table lists the lines which are available on the EXC interface, referred to the edge-connector and the designation to individual sets of thyristors on the network rack.

<u>EDGE CONNECTOR PIN No</u>	<u>THYRISTOR GROUP</u>	<u>ADDRESS</u>
1	A ₁	056
3	A ₂	156
5	A ₃	256
7	A ₄	356
9	A ₅	456
11	A ₆	556
13	C ₁	656
15	C ₂	756
17	B ₁	057
19	B ₂	157
21	B ₃	257
23	B ₄	357
25	B ₅	457
27	B ₆	557
29	C ₃	657
31	C ₄	757
33	C ₅	054
35	C ₆	154