DESIGN OF THE ELECTRONICS SUBSYSTEM FOR A HIGH-RESOLUTION ELECTRO-OPTICAL PAYLOAD USING SYSTEMS ENGINEERING APPROACH

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Dissertation submitted in partial fulfilment of the requirements for the degree of Master of Philosophy in Space Studies

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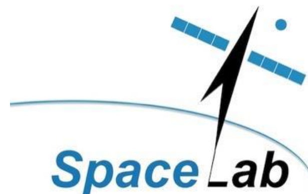

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ABSTRACT

Satellite imagers, in contrast to commercial imagers, demand exceptional performance and operate under harsh conditions. The camera is an essential part of an Earth Observation Electro-Optical (EO) payload that is designed in response to needs such as military demands, changes in world politics, inception of new technologies, operational requirements and experiments. As one of the key subsystems, the Imager Electronics Subsystem of a high-resolution EO payload plays very important role in the accomplishment of mission objectives and payload goals. Hence, these Electronics Subsystems require a special design approach optimised for their needs and meticulous characterizations of high-resolution space applications.

This dissertation puts forward the argument that the system being studied is a subsystem of a larger system and that systems engineering principles can be applied to the subsystem design process also. The aim of this dissertation is to design the Imager Electronics Subsystem of a high-resolution Electro Optical Payload using a systems engineering approach to represent a logical integration and test flow using the space industry guidelines.

The Imager Electronics Subsystem consists of group of elements forming the functional chain from the Image Sensors on the Focal Plane down to electrical interface to the Data Handling Unit and power interface of the satellite. This subsystem is responsible for collecting light in different spectral bands, converting this light to data of different spectral bands from image sensors for high-resolution imaging, performing operations for aligning, tagging and multiplexing along with incorporating internal and external interfaces.

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LIST OF ACRONYMS

ADC	Analog-to-Digital Converter
AIT	Assembly, Integration and Test
AIV	Assembly, Integration and Verification
AOCS	Attitude and Orbital Control System
AR	Anti-reflective
CAD	Computer Aided Design
CAN	Controller Area Network
CCD	Charge Coupled Device
CE	Conductive Emission
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
CS	Conductive Susceptibility
DC	Direct Current
DPU	Data Processing Unit
DTU	Detector Unit
ECSS	European Cooperation for Space Standardization
EGSE	Electrical Ground Support Equipment (EGSE)
EM	Electromagnetic
EM	Engineering Model
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EO	Electro Optical
ESA	European Space Agency
ESD	Electrostatic Discharge
FE	Finite Element
FM	Flight Model
FPA	Focal Plane Assembly
FPGA	Field Programmable Grid Array
FMS	Focal Plane Assembly - Mechanical Structure
FPU	Front Plane Unit
FS	Fully System
GigE	Gigabit Ethernet
GSD	Ground Sampling Distance
GSE	Ground Support Equipment

I/O	Input/ Output
IC	Integrated Circuit
IES	Imager Electronics Subsystem
INCOSE	International Council on Systems Engineering
ITAR	International Traffic in Arms Regulations
LEO	Low Earth Orbit
LVDS	Low Voltage Differential Signaling
MCU	Management Controller Unit
MOE	Measure of Effectiveness
MOP	Measure of Performance
MS	Multispectral
MTF	Modulation Transfer Function
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NGO	Needs Goals and Objectives
NUC	Nonuniformity Correction
OBC	Onboard Computer
OC	Out of Context
OPS	Optical Subsystem
PBS	Product Breakdown Structure
PC	Personal Computer
PCB	Printed Circuit Board
PCBA	PCB Assembly
PEA	Payload Electronics Assembly
PLS	Payload Electronics Subsystem
PHY	Physical Layer
PI	Power Integrity
PPS	Pulse Per Second
PS	Partially System
QM	Qualification Model
QPL	Qualified Part List
RE	Radiative Emission
RS	Radiative Susceptibility
SE	Systems Engineering
SEE	Single Event Effect
SEP	Systems Engineering Process

SI	Signal Integrity
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
TBC	To Be Confirmed
TBD	To Be Determined
TFU	Thermal and Focus Controller Unit
TID	Total Ionization Dose
TMTC	Telemetry and Telecommand
TRL	Technology Readiness Level
WBS	Work Breakdown Structure

1 INTRODUCTION

1.1 Motivation

During the last two decades, the worldwide demand for mid-to-high resolution Earth images taken from LEO satellites has constantly increased for a widespread range of applications from the defense and security, to environmental, agricultural, and geophysics applications to more recent general public demand [1]. Starting with the launch of the IKONOS satellite in 1999, space-based imaging systems have achieved sub-meter ground resolution for commercial applications and the quality and amount of information provided by these optical payloads is continually increasing. High-Resolution (HR) Electro-optical satellite imagery offers sub-meter resolution that is regarded as the highest quality images currently available from commercial remote sensing. These satellites are generally characterized by large dimensions, heavy weight and typically high cost. This implies that considerable effort is required for the design of the payload for these high-resolution satellites to make the mission successful.

As one of the key subsystems, the Electronics Subsystem of a high-resolution payload plays very important role in the accomplishment of mission objectives and payload goals. Hence, these electronics subsystems require a special design approach optimised for their needs and the meticulous characterizations of high-resolution space applications. The design of cameras for satellites is different from normal terrestrial commercial cameras, where the former demand exceptional performance, operate under harsh conditions and are designed in response to needs such as experimentation, inception of new technologies, operational requirements, and military demands and changes in world politics also.

Although the term 'System Engineering' dates back to 1940's in the Bell Telephone Laboratories, the major application of the subject gained the eminence during the Second World War. [2] Systems Engineering started to evolve as a branch of engineering during the late 1950's, when the race to get into space and to develop nuclear warhead missiles was considered absolutely essential for national security and reputation, and extreme political pressures were placed on the military services and their civilian contractors to develop, test, and place in operation nuclear missiles and the Earth orbiting satellites. During that tense period of time and

the competitive situation, the military services and their contractors sought the techniques and tools that would help them stand out at system performance (mission success), and project management (technical performance, delivery schedule, and cost control). During that time period and after that, many lessons were learned from difficulties and failures that revolutionised the practices for the development of high technology products, including all disciplines of engineering, manufacturing, procurement, testing, and quality control with the motivation of accomplishment of high system reliability. Today, systems engineering is regarded as an all-embracing discipline, providing the trade-offs and integration between system elements to achieve the best overall product. [3]

For space missions, systems engineering provides the required method and approach to design and develop space missions. Methods, processes and techniques in space systems engineering are designed to ensure that the end result of the space missions conforms to what was expected in the initial conception. The systems engineering principles, with defined scope, are also applicable at system and subsystem levels.

This dissertation puts forward the argument that the system being studied is always a subsystem of a larger system and the systems engineering principles can be applied, with the defined scope, to the subsystem design process as well. The aim of this dissertation is to apply a systems engineering approach for the design of an electronics subsystem of a High-Resolution Electro-Optical payload and to represent a logical integration and test flow using the system engineering guidelines. There are comprehensive resources available which provide insight and practical knowledge of using systems engineering approach and these are readily followed in this dissertation. [4]

The most influential phase of the systems engineering process is the definition of requirements, and entire fields of study have arisen addressing requirements, with their own conferences, journals and methods. This is all to ensure that there is agreement between the designers, those responsible for its construction and eventual deployment, and those paying for it. [5]

It is important that every requirement for a subsystem harmonises with the overall system and it is a function of systems engineering that these requirements are fulfilled. For this, each subsystem has its own set of requirements, derived from the system requirements, and based on these requirements different sets of configuration to be evaluated using the design methodology to develop satisfactory conceptual designs. Through comprehensive and iterative problem-solving process [6], a baseline solution is developed. In order to successfully satisfy all the desired requirements and specifications of a physically realisable subsystem, it is necessary to identify interfaces and develop an adequate, assembly and verification plan during the design

process. The process completes with verification that the need is met, including interfaces, form, fit, and completeness. The application of systems engineering to a project is tailored to the project's needs. [7]

1.2 Objectives

This dissertation is centred on the 'high level' design of an Imager Electronics Subsystem. During this design phase, there are general stakeholders' needs (e.g., operational requirements) [6] of the subsystem. While this design stage has many different feasible design solutions, it is important that the designer delve into all the issues that could potentially drive the overall complexities of the subsystem.

The main objective of this work is to propose a systems engineering approach to assist the designer of the subsystem understand the stakeholders' needs, evaluate various design alternatives, and eventually reach a realisable design solution.

The mission objective and goals are given as a reference mission. The insights gained from this study would be used in real mission for high resolution imaging mission in future.

1.3 Scope of This Dissertation

The intent of this work is to advance the knowledge and the understanding of the subsystem design according to the systems engineering practices and the solution of design issues in the acquisition of advanced systems. This dissertation does not focus the systems engineering discipline itself as it is not just about the systems engineering principles, rather it is more focused on the application of systems engineering principles and processes that would be used in the designing of a subsystem for a payload.

The 'Imager Electronics Subsystem' is regarded as a subsystem of the 'High-Resolution EO Payload' system. The Imager subsystem consists of group of elements forming the functional chain from the image sensors on the Focal Plane down to the electrical interface, to the Data Handling Unit, Telemetry and Telecommand (TMTC) and power interface of the satellite. This subsystem is responsible for capturing light from telescope, producing image data with the help of image sensors in different spectral bands, performing operations for sending this data to Satellite after aligning, tagging and multiplexing. Architecture and design of the telescope and compression, packetization and mass memory modules are not included in the scope of this dissertation.

The scope of the work includes studying and analysing the payload's scientific needs and requirements to define the Imager Electronics subsystem requirements and to create the functional architecture for the subsystem. The functional architecture is mapped to the physical architecture. Physical decomposition is performed, and the subsystem is broken down (e.g. units and modules). This decomposition leads to development of alternative conceptual designs (i.e. architectures). Based on a trade-off of the concepts, along with determining the interfaces with other subsystems, a preferred architecture is presented as a recommended baseline solution. The Assembly Integration and Verification (AIV) activity is performed to provide an assembly and integration flow and a verification plan with the selected verification and test philosophy. In the establishment of the AIV plan no software is adopted.

It is understood that generally there is a distinction between the mission designers (engineers) and those who have commissioned the mission and desire its end results (client). Construction of a satellite or its subsystems, launch and operations are to be performed by different entities, and therefore documentation and commonly understood processes are critical to successful alignment and outcomes of the various mission phases. [5] But these documents are not in the scope of this dissertation work.

1.4 Organisation of Dissertation

This dissertation is structured as follows:

Chapter 2 addresses the needs identification and gives an introduction to the systems engineering process in the light of guidelines from different sources and standards of systems engineering and a system engineering approach that will be followed in this dissertation for the design.

Chapter 3 addresses the requirements definition, functional analysis, allocation and functional architecture of the Imager Electronics Subsystem.

Chapter 4 presents the search for alternatives. This chapter addresses the iterative process carried out and the thought through approach taken into account for viable alternatives that could perform the required functions and fulfil the requirements.

Chapter 5 introduces the baseline design. Preferred alternatives resulting from the selection process becomes the technical baseline for the design project. Once the design baseline has been selected, it becomes the basis for control of the 'iterative refinement' processes, which adds details to the design and eventually yields the end product that has been verified to perform the functions and meet the requirements. This includes identifying system interfaces, both the

internal and the external interface, at the beginning of the design and continually managed throughout the life of the task to reduce unnecessary redesign resulting from incompatible system designs.

Chapter 6 introduces the Assembly, Integration and Verification (AIV) plan. The AIV plan is a plan of activities that are logical and interrelated sequence of events. The main objective is to achieve a high degree of confidence that the subsystem complies with its specified performance parameters. In order to achieve the objective, it emphasises having not only a very good test infrastructure (i.e. facilities) and an adequate AIV plan but also a qualified and efficient test team. This process is devised to provide confidence that the subsystem will achieve its operational objectives, survive in the launch environment, and perform its functions adequately during the designed lifetime. [8]

Chapter 7 presents the conclusion of the overall design and recommendations for future work.

2 SYSTEMS ENGINEERING APPROACH IN DESIGN

2.1 Introduction

Design of the Imager Electronics Subsystem (IES) is completed following the systems engineering guidelines. In a broad perspective, systems engineering is about viewing the system holistically to consider every aspect of a program or product in its entirety over the lifecycle encompassing the concept, design synthesis, verification and validation, operation, and disposal at the end-of-life. It ensures the implementation of processes that assure that the needs, goals and objectives of a product are met throughout the lifecycle. To achieve this, many standards have evolved over time that are followed by organisations for their projects. One important aspect in this is that no standard is cast in stone in practicing the systems engineering approach. Although the systems engineering standards of NASA, ESA, INCOSE and others provide a comprehensive set of guidelines, these standards are most often customized to match the organisations' needs in their operations, for their products and services, as well as to fulfil the agreements in a contract [6].

The whole process of systems engineering can be considered to based on two sister processes, i.e. a technical process that is focused on technical efforts to produce the system with required capability and performance, and a management process that is focused on organized technical management efforts to monitor the progress, risk, and effectiveness as well as to manage complexity [9]. The Systems Engineering Process (SEP) presented in this chapter is a customised SEP that describes the technical process of the systems engineering for the achievement of the design of the IES subsystem in fulfilling the objective and goals.
The systems engineering approach, in essence, is a hierarchy of steps that begins with defining a need, advances to a technical baseline and ends with verification that the need has been met. The principles of this hierarchy are presented in Table **2-1**:

Table 2-1: Principles of systems engineering approach.

Need	**Why and what the system is required for?**
Functions	What functions the system is required to perform?
Requirements	What are the set of requirements (functional requirements, performance requirements, derived requirements, interface requirements) the system is required to fulfil and under what conditions and constraints?
Alternatives	What different design solutions are available to meet the requirements and to perform the functions?
Criteria	What should be the criteria for selection amongst the alternatives?
Technical Baseline	What is the best suitable or the preferred alternative?
Verification	The proof that the preferred alternative performs the functions and meets the requirements

2.2 Systems Engineering Process

The primary goal of the systems engineering process is to lead the designer(s) to transform the requirements into system architecture, performance parameters, and design details. The Systems Engineering Process (SEP) presented in Figure 2-1 is applied in this dissertation for the design process of the Imager Electronics Subsystem for a high resolution EO payload of a satellite to provide a desirable and satisfactory outcome. The SEP is an iterative process that provides comprehensive problem solving by defining the problem, determining the effective needs, and then developing a solution though an iterative problem-solving approach [6].

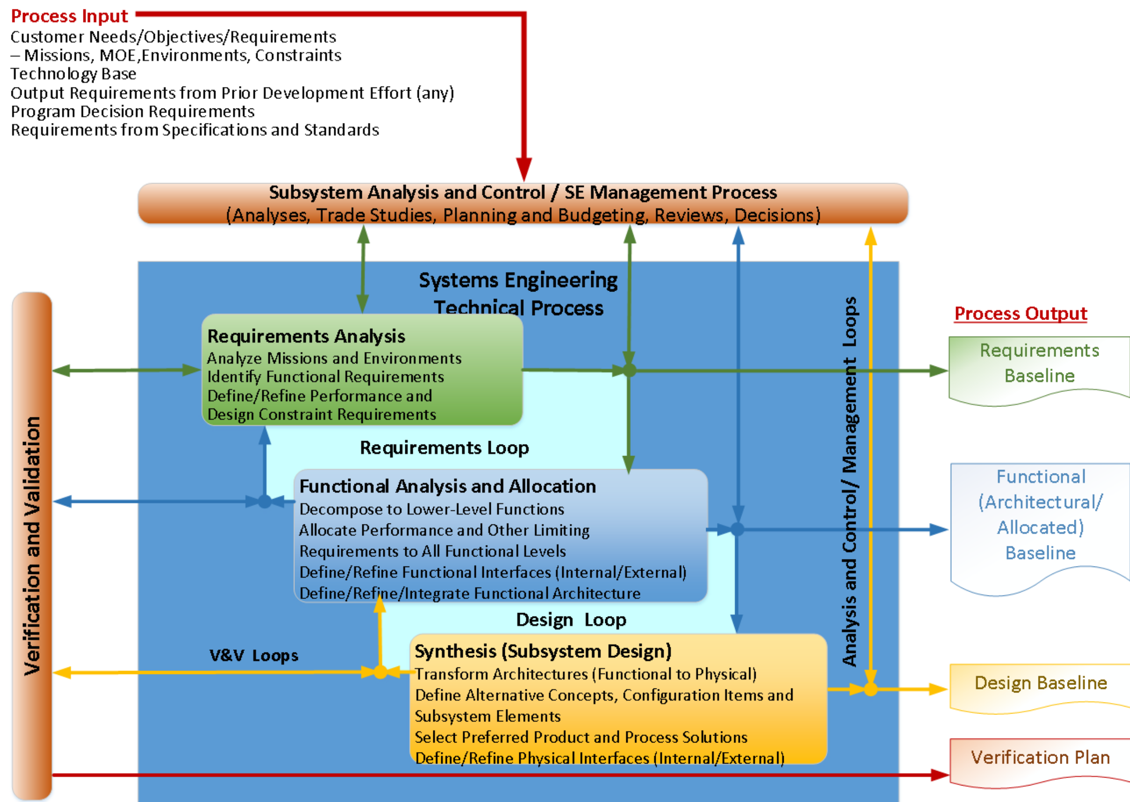

Figure 2-1: Systems Engineering Process [9].

It is the responsibility of management (program and project managers) to implement the SEP when planning a project that in general, takes into account the following factors:

- Project team's mix of experience and skills
- Documentation of the selected engineering methodology (and tools)
- Access to a technical expert about the end product
- Determine action of how the selected methodology is approved [7]

However, the system engineer is responsible for the execution of the SE process.

2.3 Problem Statement

A good system engineering approach requires a clear understanding of all the stakeholders of the problem and the boundaries of the system. [6]The client identifies and determines the problem, and all the stakeholders need to discuss and agree on the understanding of the problem and the solution. The system dynamics, such as the scope, constraints, assumptions and, the interactions with stakeholders are first studied and logically reasoned to provide the system with an effective need. The problem statement for this project dissertation work is identified in Figure 2-2.

As the Remote Sensing industry is growing, more missions are being flown carrying variou payloads for different applications. Beside dedicated missions, the general purpose of RS industry is also growing with users in all kinds of applications. To deliver high quality an very high-resolution images of the Earth to meet specific applications in the remote sensin industry, it is required to a design an electronics subsystem that will constitute a part of th high resolution EO payload of the satellite.

Figure 2-2: Problem Statement for the project dissertation work.

Stakeholder analysis consists of the following components:

a. Identifying the relevant stakeholders and their roles in the system hierarchy, development and use;
b. Examining the stakeholders' documents to analyse their needs and desires with respect to the problem; and
c. Engaging in bidirectional communications about the requirements. [6]

The stakeholders can be classified as the customer, project manager, chief systems engineer, manufacturer, or designer of another subsystem who shares common interests and responsibilities in the project [10]. The stakeholders can possess different perspectives of the system and can affect or change the system's requirements.

Analysis of stakeholders is carried out to understand the effective needs and wants of the stakeholders with regard to the problem. It is also important that the stakeholders understand and effectively communicate the end user's needs. The system dynamics, such as the boundaries, stakeholder interactions, constraints, assumptions, limitations, and project scope, are first examined and reflected to provide an effective need for the subsystem [6]. The problem statement is then revised to meet the effective need, as shown in Figure 2-3.

To provide a high-quality imaging design for an Imager Electronics Subsystem that i intended to be used as a subsystem of the high resolution multispectral EO payload of th satellite, operating in low Earth orbit for a specified life. The subsystem will be switched ON during the non-eclipse period of the orbit and will image the surface of the Earth and transmi the captured image data to the satellite.

Figure 2-3: The Effective Need and statement for this project.

The subsystem can be considered as a system in its own domain and the systems engineering principles can be applied to the subsystem design process.

2.4 Requirements Definition, Analysis and Concept Refinement

The operational needs and requirements must exist for the subsystem or be derived from the systems requirements that are identified by the stakeholders [6].

Prof. Olivier de Weck [11] describes the importance of the process of technical requirements definition that:

- Sets up the basis for mutual understanding between stakeholders and developers on what the product is intended to do.
- Reduces the development effort by:
  - motivating the relevant stakeholders to consider rigorously all of the requirements before design starts
  - carefully reviewing for oversights, missings, misunderstandings, and inconsistencies early in the development cycle
- Provides a basis for estimating costs and schedules by providing true description of the product to be developed for a realistic estimation of costs and efforts
- Provides a baseline for verification by;
  - help developing effective validation and verification plans
  - providing a baseline for compliance measurement.
  - establishing a baseline for stakeholders for product acceptance
- Facilitates transfer of the product to new users
- Serves as a basis for future-upgrades or modifications of the products.

For requirements definition, requirement analysis is performed with the clearly defined effective need to analyse the subsystem's projected needs, determine what the operational goals are, determine the end user's Concept of Operations (CONOPs), interfaces, and project and design constraints. Depending on the complexity of the project, it becomes more beneficial to include the system engineers of the subsystems to make the requirement definition step effective by defining more realistic requirements and thereby reducing the iterative process of performing requirement analysis.

CONOPs' primary goal is to ensure the operational goals and requirements to all the stakeholders. The CONOPs should therefore be discussed with all the stakeholders in order to clarify the operational scenario envisaged by the CONOPs and to highlight the issues that may arise if certain components fail. The subsystem should be adequately prepared for the scenarios that are highly possible once the subsystem has been set up. These scenarios are developed to help stakeholders understand what possible functions are essential for the operation of the subsystem and allow alternative solutions to be considered later during the design phase. [6]

The requirements analysis converts the needs into baseline system technical or engineering requirements that are related to the characteristics or attributes of the architectural design concept and of the technologies needed for its implementation. The baseline technical requirements are specified at every level, for every component that make up the system/subsystem. These requirements must be traceable and verifiable to confirm the compliance of the design. Completeness and accuracy of all the requirements are deemed necessary to avoid costly (time and money) changes later in the development process [9].

2.5 Functional Analysis, Decomposition and Allocation

After discernment of the stakeholders' needs, CONOPs and constraints, a functional analysis is carried out to translate the system's operational objectives into the desired functions. The functional analysis phase allows individual component functions of a concept to be determined and then further developed into the means of performing functions in an operating environment [6].

Functional breakdown is performed to decompose the functions into sub-function forms [6]. The resulting functional architecture of the subsystem serves the following purposes [6]:

a. Defines all the relevant high-level functions;
b. Decomposes the functions and organize them into logical grouping of “high-level” and “derived” functions;
c. Organizes the functions into the functional diagrams with the logical ordering or relation amongst the functions;
d. Performs analysis to understand what is needed to be accomplished to make the concept valid.

When the subsystem's functional hierarchy is developed, the functions are implemented to determine the functional sequencing in the operational scenario [6]. A number of methods, techniques and tools are available to perform functional analysis and allocation. These include [9]:

- Functional Flow Block Diagrams (FFBD)
- Integrated Definition for Function Modelling (IDEF0)
- System Modelling Language (SysML™)
- Unified Modelling Language (UML)
- N^2 Diagrams
- Work Breakdown Structure (WBS)

Many relevant features of the subsystem are derived by decomposing the functions and these insights can be used to generate accurate system requirements. This provides a good framework

for the subsystem where it is possible to build other sub-functions. Further decomposition of the functions gives more insight into the plausible ways to solve the problem [6].

2.6 Search for Alternatives

Once the requirements and functions are established, an essential step in the SEP is to search for realizable alternatives that will perform the functions and fulfil the requirements. The SEP encourages the innovation and creativity in this regard. Beside this, the SEP also places great emphasis on delving into the testing and quantitative measures to show that the alternatives, which although they can be very creative and innovative, are viable ways to perform the functions and meet the requirements. The search for alternatives should follow an iterative process with the functions and requirements steps of the SEP involved. [7]

Selection amongst the viable alternatives should be based on predetermined criteria that should, in turn, be based on the objectives, goals and the values identified as the result of the mission analysis.

In most of the cases, the selection process considers cost, time, performance, and risk as more obvious criteria. However, it is also necessary to consider other less noticeable criteria e.g. organizational and stakeholder values, in the selection process as well. [7]
The iteration process should be kept under control and knowing when and where to stop the iterative processes is the key. Some of the indications when this process should be stopped are:

- a well-bounded end product has been identified and found affordable
- decomposition of functions is complete, and no more practical functional allocations exist
- an existing technology can be used to provide the end product
- enough information is available to make the right decisions for the future activities (e.g. continue to the next phase or stop project work)
- the level of complexity has reached a point that one team or organization cannot manage the information or work effectively (for example, discrete components are broken out to be worked on by different smaller teams or to outsource to other organization)
- the organization has reached to a level at which it performs a “make or buy” analysis.

If a make decision is made, the requirements are included in the specifications and drawings. On the other hand, if a buy decision is made, the requirements are included in the contract. [7]

2.7 Design Baseline

Preferred alternatives resulting from the selection process become the design baseline that serves as the basis for the control of the iterative processes. Iterative refinement and fine-tuning of this technical baseline adds details and eventually brings in the end product that is verified to perform the functions and fulfil the requirements. [7]

2.8 Interface Management

Interface management is an activity in the Systems Engineering Process that ensures the compatibility, proper operation and interoperability between the subsystems that interface with each other. This activity that begins with the concept definition includes identifying system interfaces, defining the interface requirements at each interface boundary, and continues by managing the interfaces during all steps of the SEP. The structure of an interface control is influenced by the system and subsystem Work Breakdown Structure (WBS), contracts and interoperability with other subsystems.

2.9 Validation and Verification

The design validation and verification activities are important for the system designers, the systems engineer, the project and program manager, and the customer [7]. These activities are carried out to ensure that the design fulfils the functions and requirements identified for the system. These efforts confirm the progress towards eventually fulfilling the customer's needs and the results assure that the end product would pass the customer's criteria. These activities not only provide proof that the end product performs as per the specifications, but also an indication of how well the system satisfies its operational requirements [9]. To carry out these activities a plan is formulated that:

a. Provides a verification and test plan describing the selected tests and procedures;
b. Serves as an input to the lower level verification.

In order to achieve a satisfactory outcome of the validation and verification process, it is planned early in the task timeline. These verification plans are established to provide satisfactory direction to complete the process for a verifiable design. Eventually, when the verification is completed for each requirement, the individual plan links each requirement to the results or test data that satisfies that requirement. This is a well thought and a very good approach to ensure that all the requirements are met.

3 REQUIREMENTS ANALYSIS, FUNCTIONAL ANALYSIS AND ALLOCATION

In this Chapter, an overview of the system and system requirements is given and the requirement analysis and the functional analysis for the Imager Electronics Subsystem is performed. Requirements are the prime focus because the main purpose of the SEP is to transform the requirements into designs.

The requirements analysis functions as an interface between the internal activities and the inputs fed by the external sources to the SEP by examining, evaluating, and translating the inputs into functional and performance requirements that become the basis for the Functional Analysis and Allocation [9]. The requirements analysis is performed to identify all the necessary and sufficient set of performance requirements, interface requirements, and design constraints for each identified function. Functional Analysis is performed to identify the functions needed for the IES subsystem to fulfil required goals and objectives. This provides an insightful physical realization and clarifies the understanding of what the product is supposed to do for the next step of the SE design process.

The outcome of the requirements and functional analyses establish the basis for the functional and physical architectures for the successful design definition. The requirements analysis and the functional analysis performed in this chapter provide guidance for the conceptual designs to be considered in Chapter 4 and also serve as a check list for the design phase.

3.1 System overview

The complete EO Payload system is defined to base on the following subsystems:

- Optical Subsystem (OPS)
- Imager Electronics Subsystem (IES)
- Payload Electronics Subsystem (PLS)

The OPS and the IES are to be designed, developed, manufactured and tested in the same organization (the contractor), and the PLS is to be designed, developed and tested at the customer site. The OPS and IES are to be integrated at the contractor site for testing and performance verification before handing over to the customer. The complete payload is to be assembled, integrated and tested at the customer site.

Each top-level system requirement is analyzed with all the systems engineers (of the system and subsystems). Top level system requirements are presented in section

Table 3-1: System Overview, showing the subsystems and their design responsibilities.

Subsystem	**Activities on Customer Site**			**Activities on Contractor Site**		
	Design and Development	Manufacturing and Assembly	Testing	Design and Development	Manufacturing and Assembly	Testing
OPS				✓	✓	✓
IES				✓	✓	✓
PLS	✓	✓	✓			

3.1.1 System Hierarchy

It is essential to establish common definitions and understandings among different teams of the project regarding general methods and terminology for effective communication, understanding and productivity [3]. The following definitions are used to define the lower-levels of the EO payload hierarchy.

- **System**: An integrated set of subsystems that accomplish a defined objective (Payload System).
- **Subsystem**: An integrated set of assemblies, units, components, and parts which performs a clearly separated function (OPS, IES, PLS)
- **Assembly**: An integrated set of units and/or components that make a defined part of a subsystem
- **Unit**: An integrated set of components and/or parts that comprise a well-defined portion of an assembly
- **Component**: a set of multiple parts; a cleanly identified
- **Part**: The lowest level of separately identifiable items (discrete components, resistors, capacitors, inductors, nuts, bolts).

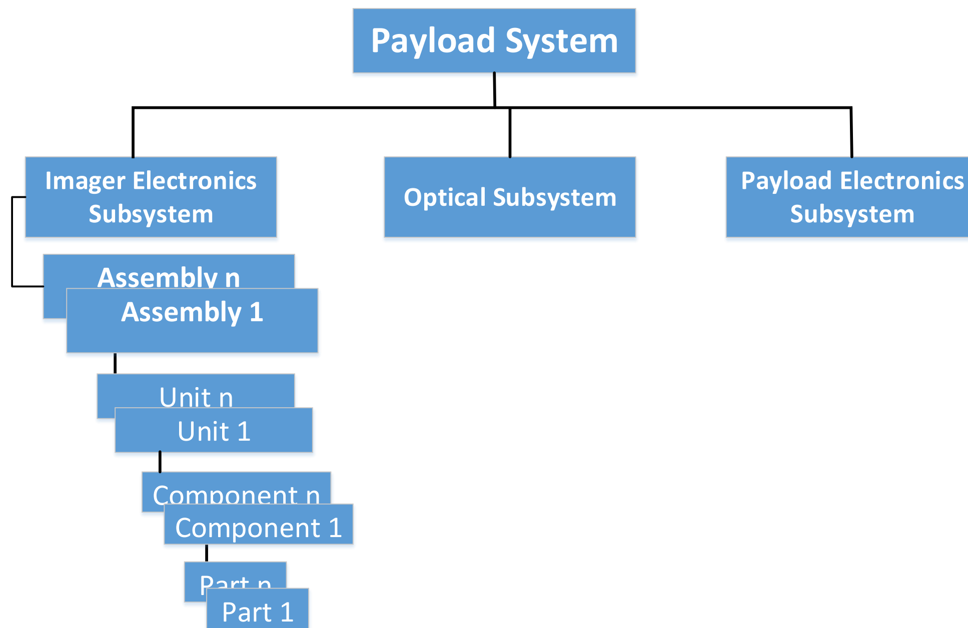

Figure 3-1: EO Payload System Hierarchy and level name conventions. The lower-levels of Imager Electronics Subsystem are elaborated in the hierarchy.

3.1.2 System Requirements

The Payload has top-level requirements for the design, that include the following:

3.1.2.1 Functional and Performance Requirements

1. The payload shall collect EM radiation from the Earth within the following spectral bands:
   - Pan 450-800nm
   - Blue 440-510nm
   - Green 510-580nm
   - Red 630-690nm
   - NIR 770-900nm
2. The Payload level MTF for the Panchromatic band shall be greater than 0.08 as a threshold with a goal of 0.1 at the Nyquist Frequency.
3. The Payload level MTF for the Panchromatic band shall be greater than 0.16 as a threshold with a goal of 0.2 at the Nyquist Frequency.
4. The total imaging swath width when nadir pointing at any location in the mission orbit, at an orbital height of 600km, shall be continuous and greater than or equal to 10km as a threshold with a goal of 11km.
5. The payload shall be able to support image acquisition time of 6 minutes per orbit over the complete design life.
6. The GSD for Panchromatic images when Nadir pointing at an orbital height of 600km, shall be 0.5m as a threshold with a goal of 0.4m when measured in along-track and cross-track direction.

7. The GSD for Multispectral images when Nadir pointing at an orbital height of 600km, shall be 4 times the GSD of panchromatic images when measured in nadir direction.
8. The SNR of the Payload for the Panchromatic band, averaged over a line of pixels, shall be at least 100 for the top-of-atmosphere spectral radiance of 100W/m2.sr.µm
9. The SNR of the Payload for the Multispectral bands, averaged over a line of pixel, shall be at least 100 for the top-of-atmosphere spectral radiance of 100W/m2.sr.µm.

3.1.2.2 Physical Requirements

10. The Payload shall have a longitudinal (Z-axis) natural frequency greater than 85Hz and less than 105Hz constrained at the Payload Mounting interface.
11. The Payload shall have a longitudinal (XY-axis) natural frequency greater than 45Hz and less than 60Hz constrained at the Payload Mounting interface.
12. The Payload mass shall not exceed 150kg as a threshold and 120kg as goal.
13. The dimensions of the payload shall be less than or equal to 2000x800x800mm3 as threshold and 1800x800x800mm3, as goal.

3.1.2.3 Design Life

14. The Payload shall have a design life of 7yrs comprising 5yrs in the mission orbit at an orbital height of 600km, and 2 years in the ground stage.

3.1.2.4 Reliability

15. The Payload shall be designed to ensure a reliability value better than 0.7 at end of life.

3.1.2.5 Manufacturability

16. All Payload parts shall be manufacturable within the specified tolerances and specifications.

These requirements are discussed among the system engineers, i.e. the chief system engineer of the EO Payload, and the system engineers of Optical Subsystem, Payload Electronics Subsystem and the Imager Electronics Subsystem for clarity, distribution and subsystem level requirements definition.

3.2 Subsystem Preliminary requirement definitions

The high-level requirements specification for the IES is based on the notion that the design is seeking a high-resolution, high quality imaging subsystem that:

- Can be used in outer space environment (Low Earth Orbit) as a part of Electro-Optical payload of a satellite;
- Will be able to be designed, developed and tested as a separate subsystem;

- Will be interfaced to the other subsystems to get the required functionality and performance at Payload i.e. system level.

The primary source of the requirements for the IES is the Payload system-level requirements as presented in the preceding section.

3.3 Requirements Analysis

Requirements analysis of the IES is performed to:

- Establish what the subsystem must have the capability of accomplishing;
- Identify the various environments in which the subsystem will operate;
- Quantify how well the subsystem must perform in measurable terms;
- Define the constraints which will affect design solutions.

Mainly the requirements, and constraints are derived from customer and stakeholder expectations, higher-level system requirements, project and enterprise constraints, and external constraints [3]. Requirements analysis is performed for the IES as explained in the following sections.

3.3.1 Subsystem Operation and Environment Analysis

A context analysis of the subsystem is performed to identify the environments of the subsystem in which it has to operate. Each environment is carefully analysed and different conditions and interfaces are thought through. This context analysis also highlights the interfaces that the subsystem has different environments throughout its life (on ground, during and after launch).

Analysis has been performed at broader level keeping in view the needs and objectives of the mission. The customer is also provided help to refine the needs, objectives, and MOEs considering the initial and evolving results of the requirements loop [9].

Various difficulties that arise because of conflicting requirements were resolved, for example, the operating time (minimum and maximum) required to accomplish the mission and its implications on the power/ thermal requirements and designs, and alternate technologies as upgrade path for future design. The customer wanted to have this imaging subsystem with full redundancy also on detector level. This customer desirement was analysed thoroughly, but the associated design complexities were analysed to be very high for thermal and electronics design and thus found not feasible with the agreement of the customer.

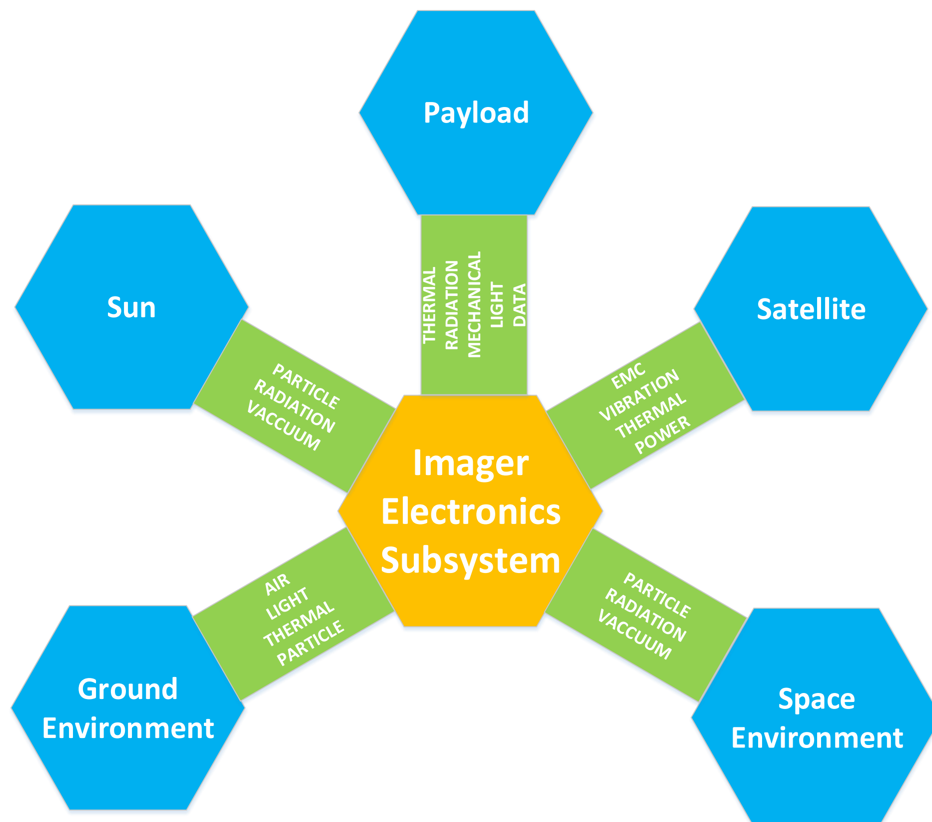

Figure 3-2: Context analysis of the subsystem showing the environments of the subsystem in which it has to operate and potential interaction with each type of environments.

The customer characterized as *mandatory* performance requirements in the form of "thresholds", and *desirable* performance in the form of "goals". Constraints that limit solutions are identified, analysed, and defined in detail, for example, technology limitations options, utilization environments (extremes of hot and cold cases, continuous imaging operation, etc.), or adverse effects in the space environments (e.g. direct sun pointing effects). While this analysis is performed early in the process, it is not a complete and finalized activity [9] and revisited a few times during the process and next phases of design.

For the requirements with "thresholds" and "goals", thresholds are minimum requirements that are needed to perform for the success of the mission and the customer has indicated that the mission may not be performed without these thresholds are met. Goals are beyond-threshold, good-to-have qualities that provide added benefit. It is agreed that achievement of a threshold is of utmost importance, whereas the goals are less critical to achieve, and the customer was made fully aware of any implications (cost, schedule, performance, and risks) involved in their accomplishment before proceeding. For example, the customer mentioned as a goal to have 0.4m GSD that was after the detailed brainstorming and concepts evaluation process (and regular discussions with chief system engineer and OPS system engineer) found that it would only be

possible if super-resolution techniques be used. Although it would have fulfilled the redundancy requirement as stated earlier, this would have made the thermal design extremely challenging and the overall design complexity and AIT effort would increase significantly. All the results were presented to the customer to see if the customer was still willing to accept the associated penalty. For this case, it is agreed to put the goal on hold for implementation at later stages, if possible (e.g. with the availability of suitable detectors for this, and better manufacturing experience to design and manufacture a larger aperture telescope). This was the customer's choice, but it was an obligation of the systems engineering to provide all the information necessary for the customers to make that decision [9].

This is understood that the validity of mission and environmental requirements are to be analyzed and assessed for mission deficiencies throughout the life of the program and are revisited [9] with the customer and the stakeholders whenever they have design alteration or exhibit adverse impact on cost, schedule, performance, or risk [9].

3.3.2 Identify Functional Requirements

The functions (presented in Section 3.4 Functional Analysis and Allocation) that the subsystem needs to perform are identified and the applicable subsystem-level attributes (requirements) are assigned to them. In this step, a subsystem hierarchy is established, and a subsystem-level specification tree developed [9]. Technical control is achieved by decomposing the subsystem level specifications into successively lower-level product specifications resulting in a specification tree in which the specifications for all the products are ultimately traceable to the subsystem specification. For this, the Product-structured WBS for the subsystem is created that has all the derived products of the subsystem (down to the components level for critical components) and that their hierarchical position in the WBS matches the hierarchical position in the build structure of the subsystem. The specification tree is shown in Figure 3-3 with the relationship between the specification tree and the PBS [12].

There are functions that involve more than one requirement. For example, the function to Process Light into raw data is primarily influenced by subsystem allocated power, spectral filtering, thermal ranges, and data interface. Further allocations of each such requirements are therefore necessary. For such requirements a derived set of attributes is assigned to a function because the subsystem-level attribute is not suitable to allocate directly, and it is assured that the assembly of functional requirements (derived or allocated) must equate to the originating specific and overall subsystem requirements. Re-assessment and balancing of functional requirements is necessary when:

a. system or subsystem requirements change; or

b. when analyses indicate that requirements assigned to a specific function might be more advantageously met in another function [9].

The traceability of functions-to-subsystem requirements is also recorded and maintained. The functional requirements become the starting point of the functional analysis and allocation. [9]

3.3.3 Identify Performance Requirements and design constraints

Measurable parameters are established by the means of preliminary level simulations, Excel worksheets and different software (Python 3.7) models to assign performance requirements to the functions/ subfunctions.

3.3.4 Identify design constraints

Functional requirements are used to initiate design requirements. The performance requirements, design requirements and constraints become the starting point of the overall subsystem analysis [9].

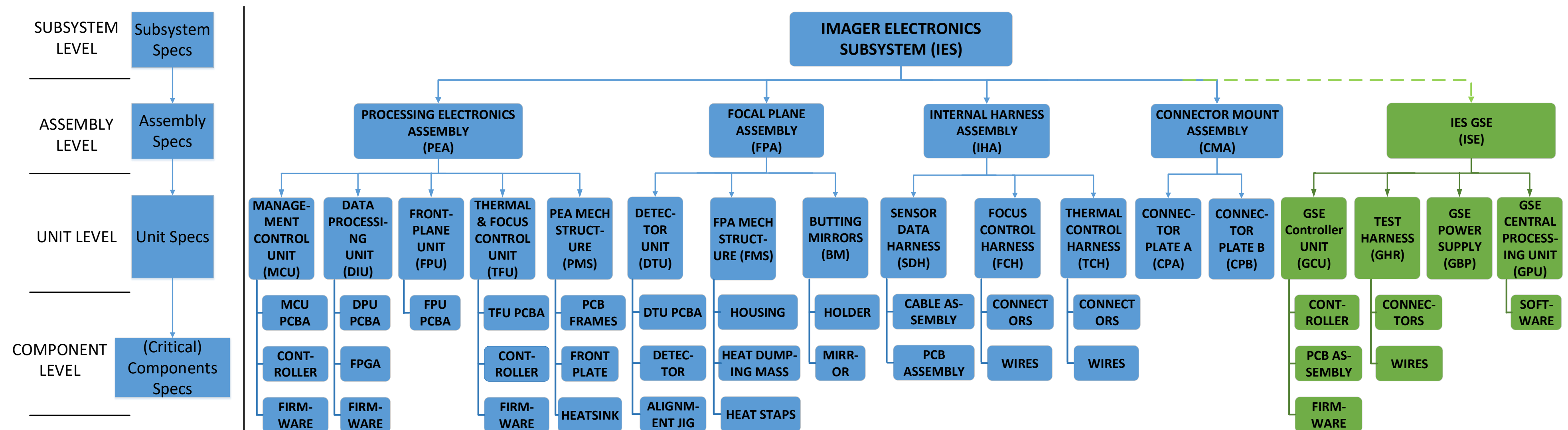

Figure 3-3: Subsystem Specification Tree.

The specifications tree is the representation of the extent to which the requirements are specified for the hierarchy. This level-of-details and organization of the specification tree is not just achieved in one go only, rather it took many iterations of requirements loop and design loop to reach this level of detailed organization. Level 4 contains the specifications of critical components only, like controllers, FPGAs, PCB etc. the PCBA represents the assembled PCB with parts and components (not just the bare Printed Circuit Board). The specification tree also highlights the importance of testability and verification of the subsystem by including the GSE specifications.

3.3.5 Tasks Performed

Following tasks are performed for the requirement analysis activity:

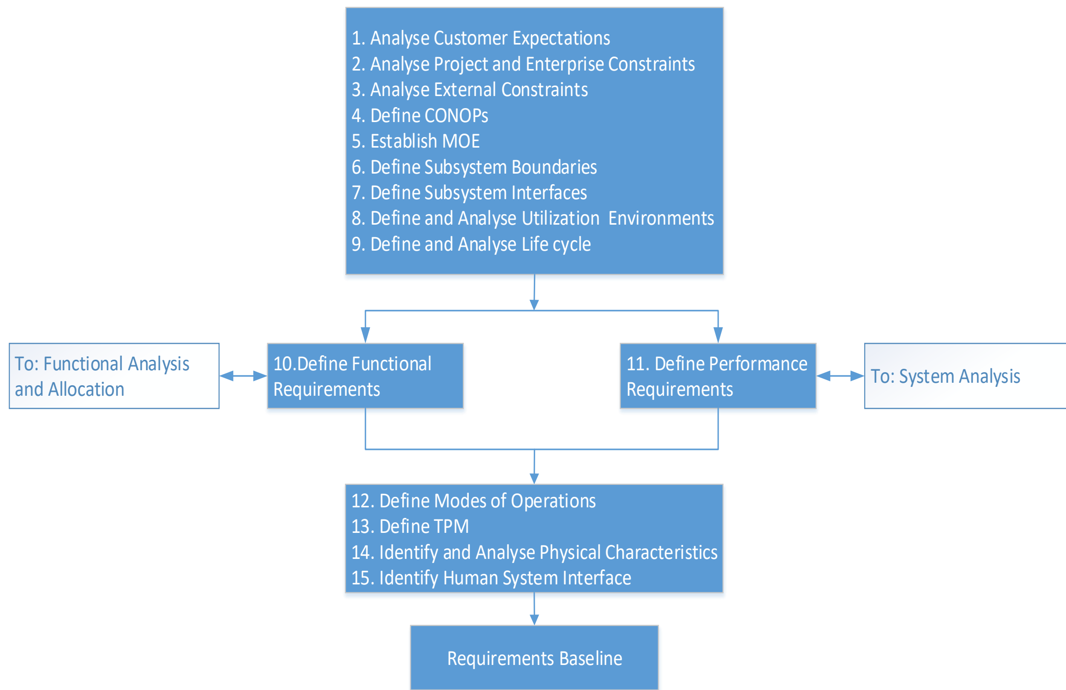

Figure 3-4: Tasks performed of the requirements analysis of the IES. These tasks are not performed in the sequence shown, rather there were many jumping and iterations between these tasks.

Table 3-2 explains the tasks performed for the requirements analysis of the IES, with the questions considered for the examination (inquiries) and the outcome (resolution) for each of the for each of the tasks.

Table 3-2: Tasks performed for requirements analysis with the inquiry for each task and the resolutions

Task	Inquiry	Resolution
1.Analyse Customer/ Stakeholders Expectation	- What are the customer/ stakeholders expectations? - What are the reasons behind the system development? - Who are the end-users and their intension to use the product? - What is their level of expertise of the customer/ user?	- Baselined Expectations: - The subsystem when integrated with the Telescope as a part of Payload shall be able to provide the GSD of better than or equal to 0.5m -The subsystem shall be able to image continuously for up to 300 seconds. - High performance with 5 years in-orbit life - All electronic parts shall be COTS with flight heritage or have passed testing to withstand a minimum of 5 years cumulative ionizing dosage. - compatible to the communication bus protocols of customers - Data interface to be compatible to the PLS data interface - Advanced technologies for image sensor - required documentation - agreed review process - Baselined Enabling Support Strategies: (needed to develop, test, produce, operate the end product and the support of the end product throughout the life-cycle) [10].
2. Analyse Project and enterprise constraints	- What are the Developing Organisation's Internal (enterprise) constraints? - What are the project constraints?	- Team Formation: - - System Engineer - - CAD designer and FE analyst - - Thermal Designer and Analyst - - Electronics designer and SI/PI analyst - - Software/ Firmware Designer

Task	Inquiry	Resolution
		- Project constraints: approved specifications; technical plans; team assignments and structure; automated tools availability for use; - Enterprise constraints: Decisions from preceding technical review; Domain technologies; Physical, financial, and human resource allocations to the project. Enterprise specifications, standards and guidelines; policies and procedures (SOPs); Established life-cycle process capabilities;
3. Analyse External constraints	- What are the external constraints which will impact design solutions or the implementation of systems engineering process activities [13]? - Is the technology ready for production? - Are facilities ready and enough resources available for production and operation?	- Imposed Constraints (Budgets, Schedules, Documentation & Reporting Requirements, Other) [14] - Use of Non ITAR components - Availability Facilities - Identification of (accessible) Manufacturing Industries - Parts/ components/ Materials availability - Understanding Public and international laws - Technology Base (analysis for best available technologies - International Standards and guidelines - Analysis of Competitor capability
4. Define Operational Scenarios	- What are the operational scenarios which define the range of the anticipated uses of system	Baselined Concept of Operations (CONOPs)

Task	Inquiry	Resolution
	product [13]?	
5. Establish MOE	- What are the subsystem effectiveness measures which reflect overall customer expectations and satisfaction? [12]	(MOEs identified during the Customers/ Stakeholders Expectations Definition Process as success criteria). -Performance -Reliability -Maintainability/ Future upgradeability -Operability - Single Point Failure Free - Establish other measurables
6. Define Subsystem Boundaries	- What subsystem elements are under design control of the performing activity? - What subsystem elements are outside the control? - What are the expected interactions among subsystem elements under design control [12]? -What are the external and/or higher-level and/or out of context interacting elements outside the subsystem boundary?	- Subsystem architecture - Division of units among IES, PLS and OPS on the basis of functions - Configuration flash to be used for NUC parameters also. - No mass memory (it is a part of PLS) - No Compression core (it is a part of PLS)
7. Identify System Interfaces	- What are existing and planned interfaces? - What are the functional and physical interfaces within the subsystem units? - What are the physics and functional interfaces to external subsystems?	Internal Interfaces - optical - Mechanical - Thermal - Electrical External Interfaces - optical - Mechanical

Task	Inquiry	Resolution
		- Thermal - Electrical
8. Define and Analyse Utilization Environments	- What environmental conditions the subsystem must comply? - What are the utilization environments for each of the operational scenarios [13]?	- Space conditions , temperature ranges, Orbit and time (for radiance levels), - induced (e.g., vibration, electromagnetic), - Imaging - Robust to direct solar irradiation for Sun pointing - Vibration and Shock Conditions - Temperature - Pressure - Humidity - Cleanliness - Radiation environment - - EM radiation - - Optical radiation - - Particle radiation - - - Single Event Latch Ups - - - Single Event Upsets - EMI/EMC interference - Prevention of creation of debris
9. Define and Analyse Life Cycle	- What are the life cycle process requirements of subsystem?	- Analysis outcomes of tasks 1 through 8 to define life-cycle process requirements for subsystem products. - Identification of higher risk elements and main cost drivers that are anticipated to impact subsystem affordability and supportability over its life
10. Define Functional Requirements	- What functions will the subsystem perform? expressed in customer language and derived from the system functions.	- Context Analysis and definition of the functional requirements (i.e. what the subsystem must accomplish or must be able to do)

Task	Inquiry	Resolution
11. Define Performance Requirements	- What are the performance requirements for each function of the system? [12]	-Performance requirements for each function of the subsystem - define how well functional requirements must be performed to satisfy the MOE. - Measures of performance (MOPs) for each MOE that are allocated to subfunctions during Functional Decomposition Analysis [13]
12. Define Modes of Operation	- What are the various modes of operation for the subsystem? - What are the various modes of operation for the subsystem products?	- Various modes of operation for the subsystem - Definition of the conditions (operational, environmental, configuration, etc) which determine the modes of operation [13] - Identification and definition of the conditions/events to which a subsystem must respond
13. Define Technical Performance Measurement	- What are the key indicators of system performance?	- The technical performance measures (TPMs) which are key indicators of subsystem performance (i.e. MOPs critical to the project and have associated cost, schedule, or performance risk). - SNR - Time synchronization and critical time delays for example imaging start-up time after Power ON command etc. - TID levels - Radiation levels - Resolutions (spectral, radiometric) - EMI/ EMC performance - Maximum image session duration - Fault detection capability

Task	Inquiry	Resolution
14. Identify and Analyse Physical Characteristics	- What are the required physical characteristics for the subsystem? - What will be the final form of the product?	- Identification and definition required physical characteristics (e.g., size, weight) for the subsystem - Identification of which physical characteristics are constraints and which can be changed based on trade studies [13] for example physical distance between units and from other interfacing subsystems for harness specifications, mounting orientation of the subsystem's units etc.
15. Identify Human System Interface	- Which human factors are constraints, and which can be changed based on trade studies? [13]	- Skills required to accomplish functions - Availability/ interaction and/or reach to critical human resource, - Ergonomics

3.3.6 Define and Refine Requirements

Various requirements of different types are established for the subsystem that have the following attributes:

- Transform the baselined customer/ stakeholder expectations (input) into unique, quantitative (measurable) technical requirements (output) [10]
- Expressed as well-written statements that can be used for defining a design solution for the WBS model of the end product (and related enabling products as well) [10]
- The following terms are used in requirements:
  - Shall: Expresses a binding/mandatory requirement
  - Should: Expresses a non-binding preference or goal and used for guidance
  - Will: Expresses intended purpose or simple futurity
  - Some of the requirements contain TBDs (To Be Determined) in places where further investigation is required in the process of the development.
  - Some of the requirements contain TBCs (To Be Confirmed) in places where values of the parameters are to be confirmed in the process of the development.

A list of TBDs and TBCs is provided at the end of the requirements document that is to be tracked and replaced with confirmed information as the project progresses.

Requirements are in normal text and have an identifier with the following format:

[Three-letter subsystem code]-TR-[Three-digit number requirement No.]-[Three-digit number sub-requirement No.]

Some requirements include additional information in the form of comments, it is identified with italics with no identifier. A section of the subsystem requirements, as example, is presented in Table 3-3.

Following different types of requirements are identified for the IES:

a. **Functional Requirements** define the functions that need to be done to accomplish the objectives. These requirements describe the top-level functions that the subsystem must perform that will be used for functional analysis.
b. **Performance Requirements** define how well the subsystem needs to perform the functions. These requirements are interactively developed for all identified functions and characterized in terms of the degree of certainty in their estimate, the degree of criticality to subsystem success, as well the extent to which functions must be executed in terms of quality (how well), quantity (how much), and timelines (how long) or periodicity (how often). Defining and refining these requirements involves calculations, technical details, and data manipulation to provide the defined functionality.
c. **Interface Requirements** are requirements that involve an interaction with another subsystem. It includes both the internal interfaces (within the subsystem units/ modules) as well as the external interfaces (the interfaces of the subsystem with other systems/subsystems) It also specifies standards and protocols to be used for these interfaces.
d. **Environmental Requirements** define different environments in which the subsystem has to survive and operate properly.
e. **GSE requirements** are established for the test equipment to be used to test and verify the subsystem functionality independent to the other subsystems while thinking about or deriving the subsystem requirements from the system requirements.
f. **Constraints** are the requirements that cannot be traded off with respect to cost, schedule or performance.
g. **Other Requirements:** The 'illities' requirement types include reliability requirements, human factors, and safety requirements. These also include material-specific or design-specific requirements or the characteristics that the subsystem is supposed to exhibit [10]

Derived requirements are implied or transformed from a higher-level requirement. For example, a requirement for continuous swatch width results in derived requirements for the number of detectors, overlap between detectors, and alignment of detectors in the cross-track direction.

Allocated requirements are those requirements that are established by dividing or otherwise allocating a high-level requirement into multiple lower-level requirements. Example: the

subsystem consists of different units that result in weight allocation requirements for these lower-level items.

Table 3-3: Template for recording the subsystem requirements.

Requirement ID	Requirement Title	Requirement Text
IES-TR-001-000	External Interfaces	The IES shall have the following external interfaces:
IES-TR-001-001		a. Handling Interface
IES-TR-001-002		b. Transportation Interface
IES-TR-001-003		c. FPA Mounting Interface
IES-TR-001-004		d. Connectors Mounting Interface
IES-TR-001-005		e. Electronics Mounting Interface
IES-TR-001-006		f. Electrical Power Interface
IES-TR-001-007		g. Payload Data Interface
IES-TR-001-008		h. Telemetry and Telecommand Interface
IES-TR-001-009		i. Temperature Sensor Interface
IES-TR-001-010		j. Imaging Interface
IES-TR-001-011		k. Radiated Thermal Interface
IES-TR-002-000	States	The IES shall have the following states:
IES-TR-002-001		a. ON state
IES-TR-002-002		b. OFF state
IES-TR-003-000	Operating Modes	The IES shall have the following operating modes:
IES-TR-003-001		a. Configuration Mode
IES-TR-003-002		b. Imaging Mode
IES-TR-003-003		c. Error Mode
IES-TR-004-000	Start Imaging	The IES, in Imaging mode, upon receipt of a “Start Imaging” command via the Telemetry and
IES-TR-005-000	Update Auxiliary Data	The IES, in Imaging mode, shall allow the AOCS telemetry and Time to be updated by
IES-TR-006-000	Spectral bands	The IES shall measure the quantity of electromagnetic radiation that is incident upon the Imaging
IES-TR-006-001	Panchromatic	450-800 nm
IES-TR-006-002	Blue	450-510 nm
IES-TR-006-003	Green	510-580 nm
IES-TR-006-004	Red	630-690 nm
IES-TR-006-005	NIR	770-900 nm

3.3.7 Requirements Baseline

The requirements baseline is established for well-formed and feasible requirements for the subsystem that are approved and put under configuration control. The requirements baseline consists of documented performance, functional, architectural, dependability, and constraints specifications. The requirements baseline includes:

- A documented (and configuration-controlled) list of system specifications (to be validated through customers/ stakeholder reviews)
- Analyses of requirements to ensure that it is valid, necessary, current, and satisfies the higher-level capabilities, requirements, or constraints from which they resulted [9]
- Documented method of verification for all requirements to demonstrate achievement of the specified characteristics (verification plan)
- All the standardization and interoperability constraints
- All the functional, architectural, performance, dependability, and constraint characteristics
- The interface characteristics with associated Configuration Items and other subsystems
- Identification of lower level Configuration Items, and the configuration documentation for items which are to be integrated or interfaced with the Configuration Items
- Preliminary analyses of lower level requirements/ unit and module specifications

3.3.7.1 Requirements Validation and Requirements Loop

The requirements validation performed with the following inquiries [10]:

1. Are the requirements written correctly? [10]
2. Are the requirements technically correct? [10]
3. Are the expectations of customers/ stakeholders included?
4. Are the requirements feasible?
5. Are the requirements verifiable?
6. Are the requirements unique (non-redundant or over-specified)?

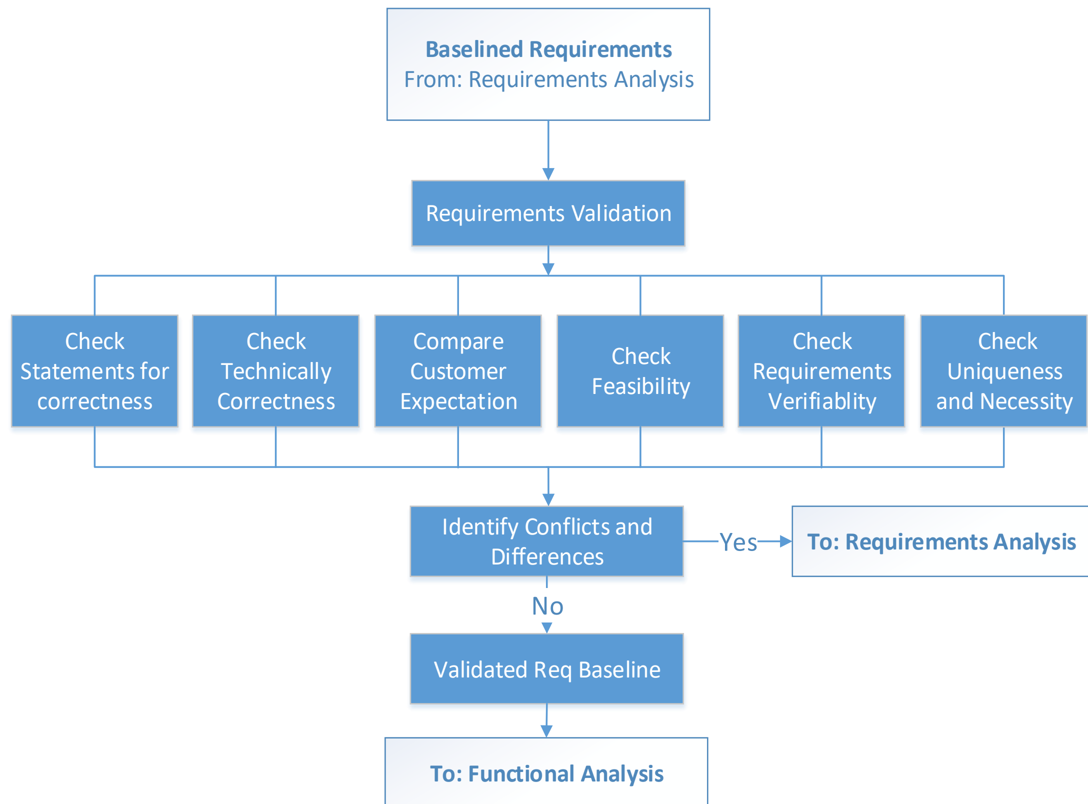

Figure 3-5: The process of requirements validation. It is an iterative process that is based on the results of the functional analysis and any changes in the requirements or analysis results.

3.3.7.2 Requirements Traceability

The traceability matrix is organized using MS Excel. There can be many commercial tools that can be tailored to cover the specific needs, but MS Excel is well-known, available and easy to use, so it was quite suitable to choose an existing and well-known tool. [15]

At subsystem level the number of specifications is less than 150, which remains a number that MS Excel can easily handle.

System to Subsystem Requirements Traceability is maintained in the template shown in Table 3-4.

Table 3-4: Example of the traceability of the system requirements to the subsystem requirements.

Payload Requirement		Subsystem Requirement	
ID	Title	ID	Title
PLD-TR-006	Panchromatic GSD	IES-TR-009-000	Panchromatic spatial resolution
PLD-TR-007	Multispectral GSD	IES-TR-010-000	Multispectral spatial resolution

3.3.8 Requirements Traceability

The subsystem to unit traceability for requirements is maintained in the template shown in Table 3-5. For each row the text reports a single specification, and there are as many rows as many the specifications are. The fields are explained in the following:

Requirement: ID. This is the project unique code used for the unit specification document. It is unique and describes only one specification. The code indicates the applicability to the level of product by having associated with a three-letter field of the abbreviations. For example, an FPA code refers to a specification directly related to the Focal Plane Assembly, FMS refers to a specification related to Focal Plane Assembly - Mechanical Structure, a SUB code is referring to a requirement that is applied to the entire subsystem in general. The requirement ID is formed as: [Three-letter code]-DS-[Three-digit number]

Requirement: Title. In this field the Specification title as per subsystem specification document is recorded.

Traceability: ID. Each specification answers to at least one requirement, so there exists a specification that answers to many requirements, but on the other hand, it is not possible to have a specification that traces to nothing. In this case the specification is not needed and should be removed from the specifications list [15].

Table 3-5: Example of the traceability of the subsystem requirements to the unit requirements.

Requirement		Description	Traceability		Verification
ID	Title	Statement	ID	Title	Reference
FMS-DS-009	FMS: Multipl detectors	The FMS shall support 6 detectors and thei accompanying electronics.	IES-TR-012-000	Light Measurement Width	FMS-VR-009-1R
FMS-DS-010	FMS: Overla between detectors	The detectors shall be placed next to each other on th FMS, with an overlap of no more than 150 pixel between each pair of consecutive detectors.	IES-TR-012-000	Light Measurement Width	FMS-VR-010-1A

Traceability: Title. In this field the Specification title of the parent requirement is reported.

Verification: Reference. The reference to the verification that gives an indication to the preferable verification method. Different verification methods are used where:

A specifies Analysis

R specifies Review,

I specifies Inspection,

T specifies Test, and

D specifies Demonstration**.**

At least one verification method is listed for each specification, but more than one method are also listed for many of the specifications.

3.4 Functional Analysis and Allocation

Functional analysis is performed to identify, describe, and relate the functions of the IES that it should perform to fulfill its goals and objectives. It is used to link the subsystem functions, interface characteristics, and rationales to requirements [10]. This process is elaborated in Figure 3-6, and the activities are described in the subsequent sections.

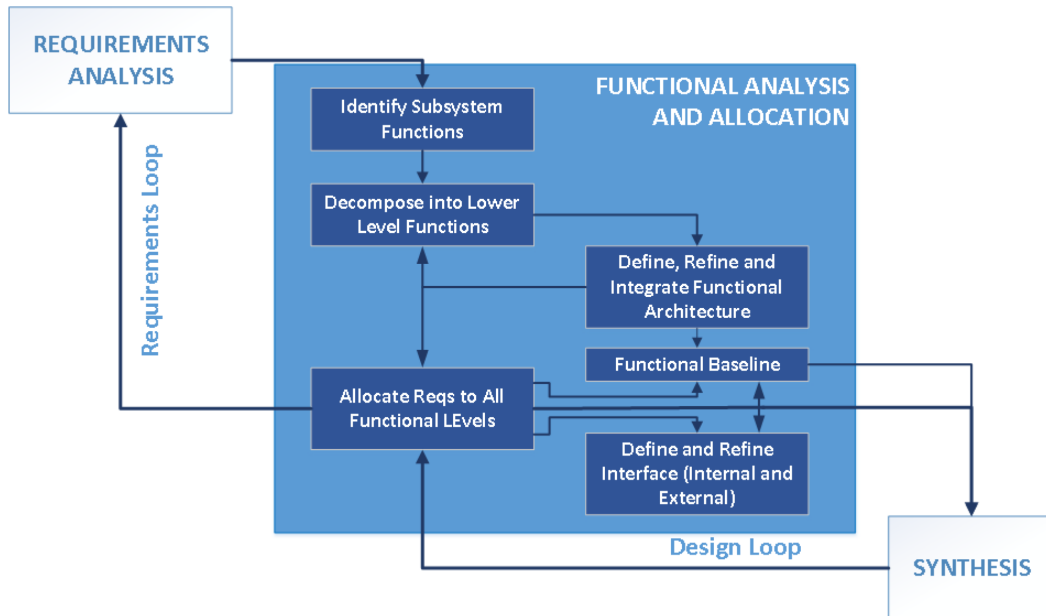

Figure 3-6: Functional analysis and allocations-with the requirements aids the synthesis process through the design loop.

Following activities are performed for the Functional Analysis and Allocation.

3.4.1 Identify Subsystem Functions

The payload level functional analysis is reviewed and the functions that are relevant to the IES subsystem are identified. These functions serve the First Level functions for the IES functional analysis. The extent to which the payload functions are relevant to the subsystem is also identified. For this, following terminologies are used:

Partially Subsystem Performed (PS): the functions that are relevant to the subsystem but need to be fulfilled only partially. Partly system functions are divided into FS and OC functions.

Fully Subsystem Performed (FS): the functions that are to be fulfilled by the subsystem.

Out of Context (OC): the functions that are not in the context of the subsystem and are not to be performed by the subsystem.

3.4.2 Decompose Each Function to Lower-Level Functions

Each FS function of the first level is decomposed into the lower levels of the product breakdown structure through a stepwise top-down problem-solving approach. Functional identification and

decomposition is performed with respect to logical groupings, time ordering, state transitions, data flow and control flow. The main objective of performing the decomposition further to greater details is to meet the functional requirements and to reduce the potential risks [3], but at some point the incremental risk reduction becomes smaller than the added benefits (i.e. cost, time, performance and effort). Therefore, the decomposition process is followed until a logical point where the functional requirement is clear and realizable (to the point that design work can be accomplished in hardware, software, and operations) and beyond which the effort provides no significant value addition. The subsystem functions are presented in Figure 3-7.

3.4.3 Allocate Requirements to All Functional Levels

The objective is that all the requirements of the top-level functions must be met by the aggregate of all lower-level functions and requirement allocated to a function and its subfunctions in the hierarchy. Performance requirements are decomposed, and additional requirements are also derived and allocated to all functional levels.

3.4.4 Define/Refine Functional Interfaces (Internal and External)

Interface definition and control begins in parallel with the development of functional architectures. Both types of interfaces i.e. physical and functional are defined in the functional architectures. The Interface Control Document (ICD) provides interface definitions for the interfaces to ensure that the required capabilities are achieved.

This is described in the interface management discussion in Chapter 5.

3.4.5 Functional Baseline

The output of the functional analysis is the functional baseline. The functional baseline describes functional, performance, interoperability, and interface requirements that are allocated from those of a system to subsystem and subsystem level to lower level configuration items. The baseline is established and put under configuration control by the management team of systems engineers. The baseline along with the requirements becomes the input to the design synthesis.

3.5 Modes of Operation

Modes of Operation for the IES (and also Payload) are presented in the figure.

Following parameters are stored on the IES:

- Platform ID
- Camera Configuration parameters.

These values can be updated, when necessary, by sending the appropriate set commands to the IES. The following parameters should be updated before an imaging scenario:

- Image ID,
- Time.

When entering from off state to ON state the MCU is turned ON and remains ON

3.5.1 Configuration Mode

Configuration Mode is used to update the configuration parameters and selects and sets telemetry reporting periods.

When entering Configuration Mode, the following functions are performed automatically:

- DPUs powered OFF (if not already OFF),
- DTUs powered OFF (if not already OFF)

Entry into either Playback Mode or Imaging Mode is possible with the Set Camera Mode command.

3.5.2 Imaging Mode

Imaging can only be done in Imaging Mode. When entering Imaging Mode, the following functions are performed automatically:

- DPUs powered ON (if not already ON),
- DTUs powered ON (if not already ON),
- Update the Auxiliary data to the DPUs. This includes the AOCS data.
- DTU setup Imaging is initiated upon receipt of Start Imaging command.

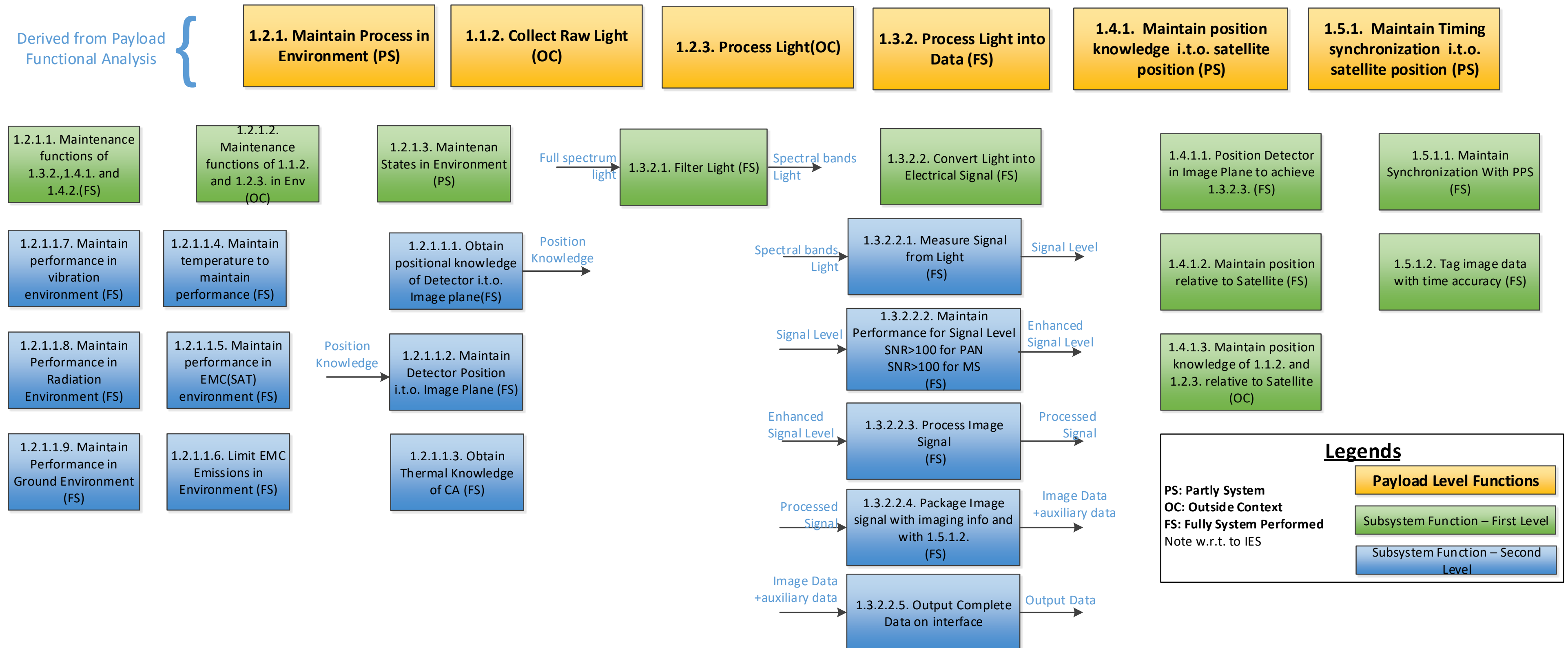

Figure 3-7: Functions of different levels identified for the IES through Functional Analysis.

3.5.3 Playback Mode

Data transmission and management is performed in the Playback mode. When entering Imaging Mode, the following functions are performed automatically:

- DPUs powered ON (if not already ON),
- DTUs powered OFF (if not already OFF)

Playback of image data is initiated upon receipt of Start Playback command or automatically when Auto Transmission has been selected for an imaging session.

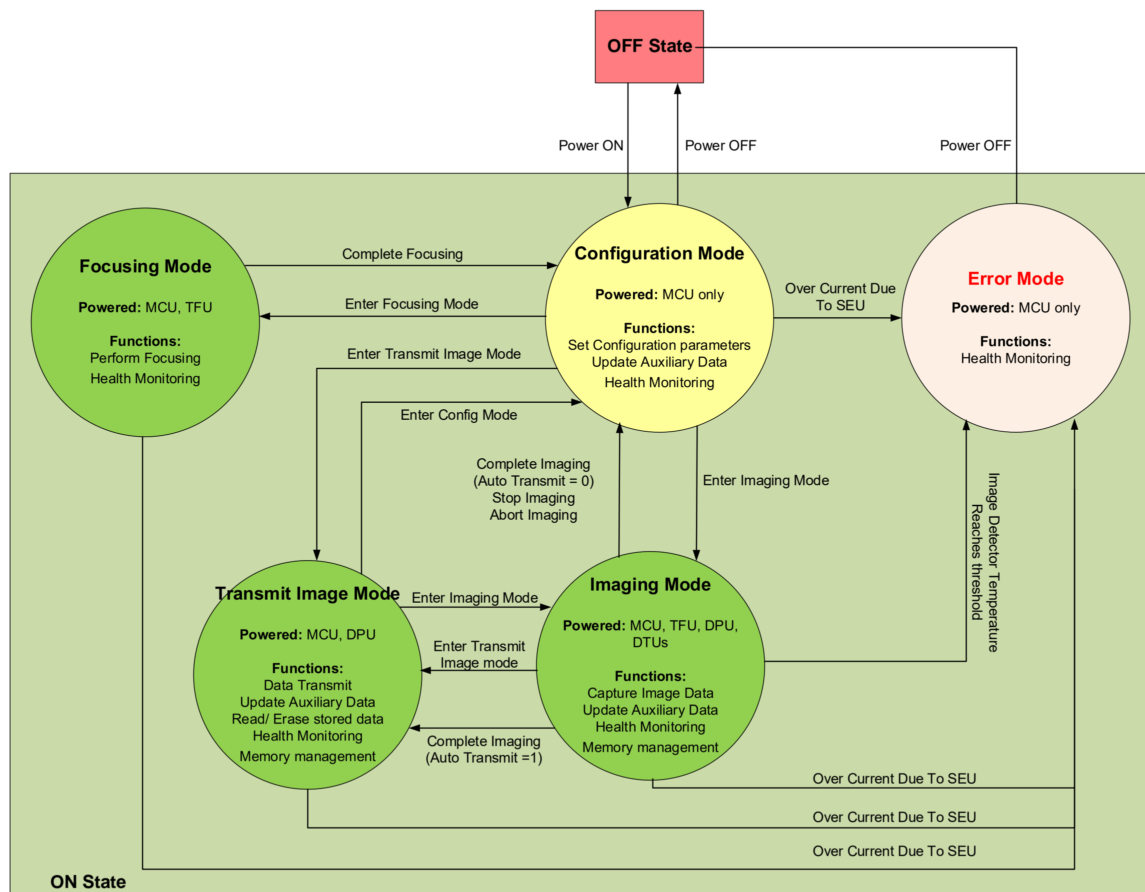

Figure 3-8: Operating modes of the IES with mode transitions

3.5.4 Focusing Mode

The IES enters in the focusing mode upon reception of dedicated command. The IES enters in this mode during the calibration campaigns only.

- TFUs powered ON

The focusing range is sent through the commands and feedback is received to monitor the range.

3.5.5 Error Mode

The IES enters Error mode under any of the following conditions:

- An overcurrent occurs in a DPU or MCU or TFU due to a latch-up caused by a Single Event Upset (SEU),
- DTUs overheat due to being ON for longer than maximum ON time limit. This will most likely only occur in orbit or TVC testing.

When entering Error Mode, the following functions are performed automatically:

- TFUs powered OFF (if not already OFF),
- DPUs powered OFF (if not already OFF),
- DTUs powered OFF (if not already OFF) Error mode provides the ability for the Payload health telemetry to be monitored and the reason for entry to Error mode to be determined.

The only exit from Error mode is the removal of primary power supply.

4 DESIGN SYNTHESIS, ALTERNATE-CONCEPTS AND EVALUATION

4.1 Introduction

The basic conception of the Imager Electronics Subsystem was encapsulated in the preceding chapter by describing the requirements and functional analysis. In this chapter different conceptual approaches are presented to implement the subsystem with those requirements and functions are considered by performing architecture synthesis. These conceptual approaches are presented in this chapter.

Architecture Synthesis is a search-for-alternatives process and is highly iterative that has the following objectives:

1. To satisfy the functional and interface requirements.
2. To negotiate with the stakeholders for any requirements changes and find solution with consensus.
3. To ensure that the solution is acceptably close to the true optimum within the constraints of available knowledge and skills, time, budget, and other resources [3].
4. To provide future upgradability to accommodate the introduction of new technologies and system growth
5. To provide the base of information for the subsystem definition, development and implementation to proceed with adequately defined internal interfaces.
6. To provide a robust architecture definition that would proceed with minimum backtracking as additional information is uncovered at later stages.
7. To understand the associated risks and technical maturity of available elements.

From the identified functions the like functions are grouped together to identify subsystem elements (i.e. assemblies and units). In this identification process, the functions are distributed amongst the subsystem elements (assemblies or units) and there could be potential overlap of the functions that can be performed by one element or the other. After a detailed brainstorming

process of iterative relocation of the functions amongst the elements and revisiting the functional analysis and allocation, and requirements analysis for the addition and completeness, different alternates are thought through.

More realistic alternates are chosen as candidates for trade-off. A preliminary search was performed to short list the most feasible alternates from a very large number of options. Based on the previous experience and to do a more directional work following agreements were made.

1. Detectors wouldn't be placed with more than one detector on the single detector PCB. This is so because it is important to align each of the detectors very carefully within very narrow alignment tolerances that is possible only if each of the detector can be aligned separately. The first detector will be aligned very carefully with respect to the housing, that will serve as a reference for the next detector and so on with respect to each other. On the other hand, if the detectors are placed on a single PCB in groups (of two, three, or all detectors on a single PCB) within these groups it is not possible to solder the detectors with tolerances and the larger group can't be aligned to achieve the required alignment accuracy.
2. The detector assembly would be made physically separate (although it will be electrically connected) from the rest of electronics and structure. On this detector assembly detectors (with their PCB) would be aligned with respect to the mechanical housing and with respect to each other and bended in place. This is decided because, once the detectors are aligned, the complete detector assembly must be aligned (within strict tolerances) with the telescope and if it would have its complete processing and power electronics with the detector assembly i.e. in essence the complete IES, then it would be a big challenge to design such a big alignment stage with a capability to handle the whole mass of the complete FPA (>5kg in the preliminary estimations) and yet to provide alignment accuracies of sub-micrometer. Making the detector part separate from the rest of the electronics would also be extremely helpful in thermal management. So, the IES design is based on two assemblies, i.e. the Focal Plane Assembly (FPA) and the Processing Electronics Assembly (PEA).
3. In a choice to use front plane or backplane based design, it is agreed beforehand that the front plane based design will be used. The rationale for this comes from an estimation of the number of expected connectors that would be required in the design. As discussed in item 1 above, the number of detector units would be equal to the number of detectors which implies that each detector's data and control signals require a separate cable that would attached to the PEA and the units would also have their own connectors for inter-board connectivity, communication with the satellite bus and image data output, etc. So it is decided to use a front plane to which all the connectors would be placed on both sides of the front plane PCB. Connectors on one side of this front plane PCB are used to

connect the unit internal to the PEA while connectors on the other side of the front plane PCB are for connections outside the PEA i.e. data output, Telemetry and Telecommand, power input, etc.

As discussed in the previous chapter that the customer has constrained the design for the use of detector to be provided by them. The detector attributes are listed in Table 4-1.

As discussed in item 2 above, that the IES design is based on FPA and PEA. For the design of both of these two assemblies, different alternates are considered. First, different candidates for the PEA are evaluated and then for the selected PEA Alternate-Different candidates of FPA are evaluated. The detector unit that is placed in the FPA influences the design of the PEA as discussed in the subsequent section 4.2. The design of the detector unit also plays an important part in the FPA design where the arrangement of detector units defines the number of connector plates required and the separation between the detectors, as discussed in the section 4.3.

Table 4-1: Parameters of the detector for the IES.

Parameter	Value	Unit
Type	Hybrid CCD and CMOS TDI*	
Number of bands	5	
Resolution	5x4096x256	bands x columns x TDI stages
Pixel		
Pitch	7	µm
Full Well Capacity	31600	Electrons
Readout noise	40	electrons rms at 25°C
Dark current	7000	electrons/s/pixel at 25°C
QE		
@550nm	90	%
@630nm	80	%
@700nm	65	%
Other		
Max line rate	300	kHz
ADC resolution	12 (or 10 bits) **	Bit
Power Consumption	<4.2	W
Physical Size	48 x 42	mm x mm

* CCD storage and CMOS readout circuitry

** Selectable

4.2 Alternates for Processing Electronics Assembly

Following are the different candidate alternates evaluated for the PEA.

4.2.1 Alternate-1

In this candidate alternate, each detector is placed on its corresponding PCB that contains the detector only. The PCB routes all the signals to and from the detector. The PCB has a rigid-flex-rigid construction where one of the rigid parts contains the detector and the flex part carries the signals to/from the other rigid part of the PCB that contains the connector for the incoming to /outgoing signals for the detector. The front-end electronics for detectors and the data processing electronics is placed on a separate PCB. This unit (Data Processing Unit-DPU) will route the power and the control signals to the detector. This unit also monitors health telemetry of the detectors and receives the image data from the detector units. The image data is processed by this unit, multiplexed and sent to the PLS on a dual redundant data interface. The DPU is made redundant by having another duplicating unit that works as a standby to the main DPU.

The Management Controller Unit (MCU) receives power from the satellite bus and converts it to the required levels to be used for the detectors and the rest of the electronics. This unit also

monitors the temperature of the Telescope and IES subsystems and controls the telescope heaters. It also monitors the focus of the Telescope and controls the focus on receiving the appropriate telecommand. The Management Controller Unit is responsible for all the communication with the satellite (Telemetry and Telecommand).

The front plane unit interconnects the units for routing the signals between the units as shown in Figure 4-1. The harness from the detector units is attached to the front plane connectors. The front plane contains all the data connectors and communication connectors.

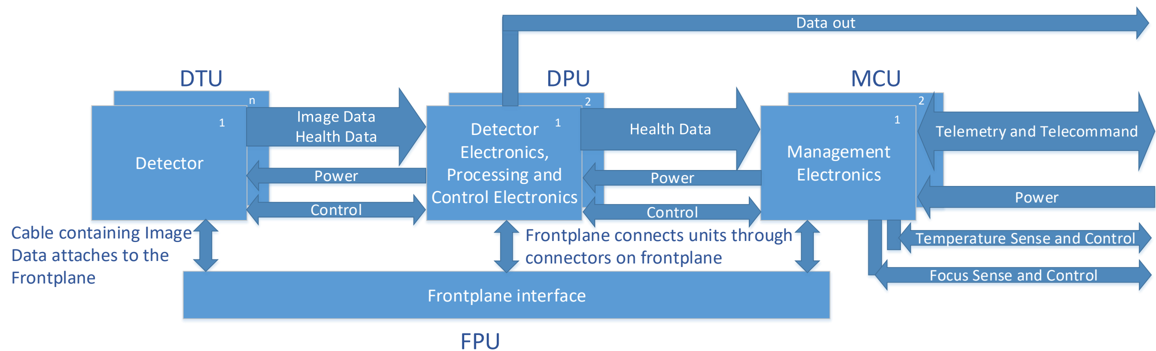

Figure 4-1: Block level representation of Alternate-1. For simplification only main interfaces are shown. The data output interface has two channels (main and redundant) from each DPU. TMTC and Power interfaces are also redundant interfaces for each MCU.

4.2.1.1 Pros

- The size of the detector PCB is small which makes it convenient for the alignment of the detectors.
- The supporting front-end electronics and the processing electronics for all detectors is on a single DPU (that has its redundant unit).
- The MCU acts as a central unit, does the power regulation for all electronics units and responsible for communication bus that simplifies the overall design.
- Smaller number of output data channels and thereby reduced number of harness.

4.2.1.2 Cons

- The supporting electronics for the detector unit is away from the detector, which could cause distortions in the power and signal lines.
- The DPU that contains front-end electronics and processing electronics is processing image data for all the detectors. This requires either a processing device with lots of resources or more than one device is required. In either case the programming and firmware becomes the extremely complex task.

- The Management Controller Unit (MCU) is providing the required power for the rest of the units and the detector power is routed through the DPU to the detectors. This long route for power requires a lot of design effort to route the required power levels and purity to the detectors.
- A very high data rate interface is required between the IES and PLS.
- A complex design for the Management Controller Unit is required for performing different tasks that includes circuits for power regulation and management, TMTC handling, bus communication, and performing thermal and focus control.

4.2.2 Alternate-2

In this candidate alternate, each detector is placed on its corresponding PCB that contains the supporting electronics for the detector. The PCB sends out all the image data and health data from the detector and receives the required power and control signals. The control signals go in both directions, i.e. the settings going into the detector unit for detector registers and the register values of the detector going out of the detector unit when read by the Data Processing Unit. Health data includes the temperature, voltage and current measurements of the detector unit to the DPU. The PCB has a rigid-flex-rigid type construction where one of the rigid part contains the detector with its electronics as explained above, the flex part carries the signals to/from the other rigid part of the PCB that contains the connector to be interfaced with the harness to the DPU.

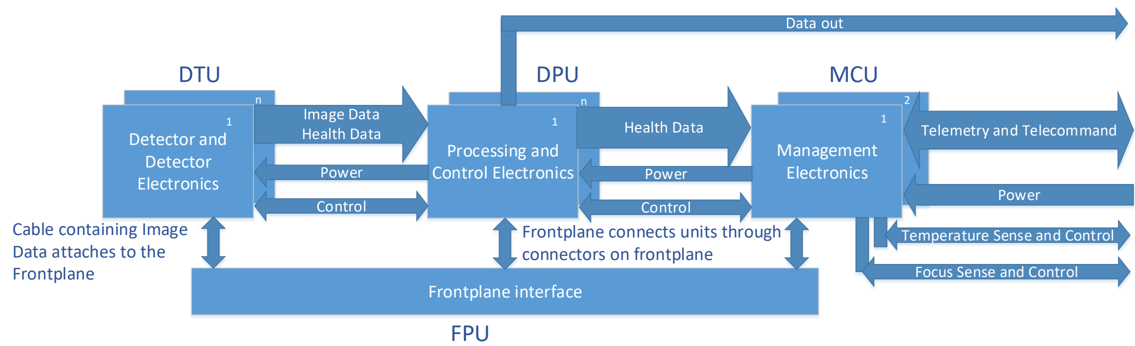

Figure 4-2: Block level representation of Alternate-2. For simplification only main interfaces are shown. The design alternate has equal number of DTUs and DPUs, i.e. one DPU for each DTU. The data out interface has two channels (main and redundant) from each DPU. TMTC and Power interfaces are also redundant interfaces for each of the MCU.

The processing electronics for detector data (DPU) is placed on a unit with a separate PCB. Each detector has its corresponding DPU that receives and processes the corresponding detector's data. This unit will route the power to the corresponding detector units where the regulators placed on the Detector Units perform the power regulation for detector and its supporting electronics. The DPU also sends the control signals to the respective detector unit and also monitors the health telemetry of the detector. The processed image data is sent to the PLS on a dedicated data interface. Each of these interfaces is made redundant.

The Management Controller Unit receives power from the satellite and converts it to the required levels to be used for components on the MCU and for the DPU. The Management Controller Unit also monitors the temperature of the Telescope and IES subsystems and controls the telescope heaters. It also monitors the focus of the Telescope and controls the focus on receiving telecommand. The Management Controller Unit is responsible for all the communication with the satellite and other subsystems.

The front plane unit interconnects the units for routing the signals between the units as shown in Figure 4-2. Harness from the detector units is attached to the front plane connectors. The front plane contains all the data connectors and communication connectors.

4.2.2.1 Pros

- The detector PCB performs power regulation for the detector that guarantees clean power for the detector.
- Equal numbers of DPUs as that of DTUs simplify the design making the design more modular.
- Separate data link for each of the detector's data requires a low-speed data interface (each interface has its redundant counter part).

- The Management Controller Unit is responsible for communication with the bus that simplifies the overall design.
- Similar design for all the detector units.
- Similar design for all the DPUs.
- The testing of the chain comprising of detector units and their corresponding DPUs is more convenient.

4.2.2.2 Cons

- The supporting electronics for the detector unit is on the detector unit with additional heat dissipation on the DTU. This is an important consideration as thermal distortions may cause pixel mis-alignments and require more design effort for the thermal design to maintain position and the required alignment at pixel level.
- Increased number of data interfaces for each detector's data and additional for the redundancy (as compared to alternate-1).
- A complex design for the MCU is required for performing different tasks that includes power management, TMTC handling and bus communication, and performing thermal and focus control.

4.2.3 Alternate-3

The detector unit and the Data Processing Unit for this alternate is same as Alternate-2.
The Management Controller Unit receives power from the satellite and converts it to the required levels to be used for components on the Management Controller Unit and for the DPU. The MCU is responsible for all the communication with the satellite bus and other subsystems.

The Thermal and focus control unit monitors the temperature of the Telescope and IES subsystems and control the telescope heaters. It also monitors the focus of the Telescope and controls the focus on command.

The front plane unit interconnects the units for routing the signals between the units as shown in Figure 4-3. The harness from the detector units is attached to the front plane connectors. The front plane contains all the data connectors and communication connectors. The MCU, DPU and the TFU are connected through the front plane.

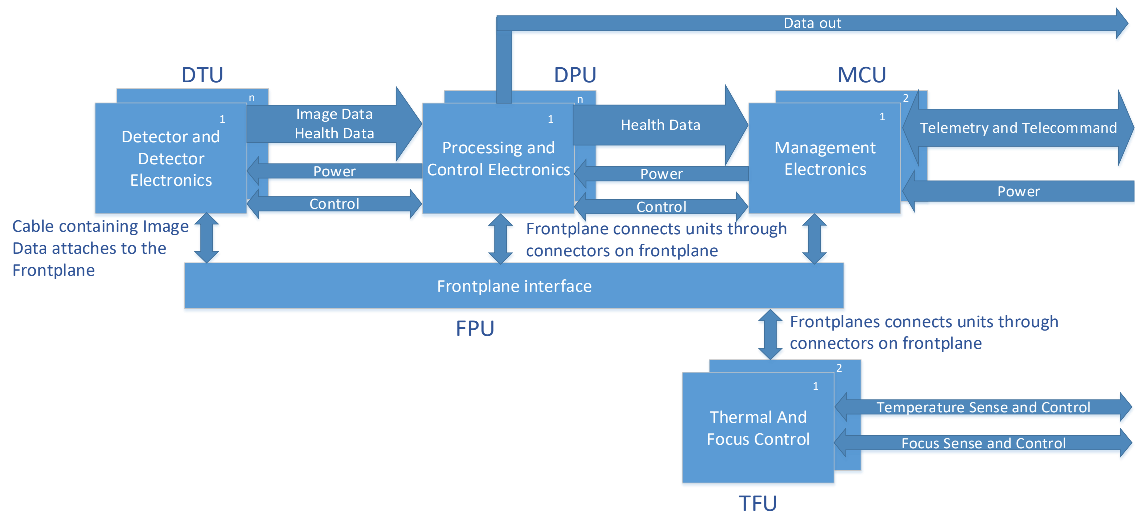

Figure 4-3: Block level representation of Alternate-3. For simplification only main interfaces are shown. The design alternate has equal number of DTUs and DPUs, i.e. one DPU for each DTU. The MCU and TFU are dual redundant. The data out interface has two channels (main and redundant) from each DPU. TMTC and Power interfaces are also redundant interfaces for each of the MCU.

4.2.3.1 Pros

- Simplified design of Management Controller Unit (as compared to alternate-1 and alternate-2).
- Dedicated unit for thermal and focus control.
- Power regulation is performed on the detector unit that guarantees the clean power for detectors.
- Equal number of DPUs as that of detectors units simplify the design with the use of smaller processing IC on DPU.
- Separate output data link for each of the detector's data requires low speed data interface (each interface has its redundant).
- The MCU is responsible for communication with the satellite that simplifies the overall design.
- Similar design for all the detector units.
- Similar design for all the DPUs.
- The modular arrangement makes the testing of the chain comprising of detector units and their corresponding DPUs more convenient.

4.2.3.2 Cons

- Increased number of units for the design (as compared to alternate-1 and alternate-2).
- The supporting electronics for the detector unit is on the detector unit, with additional heat dissipation. This is an important consideration as thermal distortions may cause

pixel mis-alignment and requires more design effort for the thermal design to maintain position and the required alignment at pixel level.

- Increased number of data interfaces for each detector's data and additional for the redundancy (as compared to alternate-1).

4.2.4 Alternate-4

The detector unit is same as Alternate-2. The Data Processing Unit for detector data is placed on a unit with separate PCB. Each detector unit has its corresponding Data Processing Unit that receives and process the corresponding detector's data. This unit will route the power to the regulators of the corresponding detector units and sends the control signals to the respective detector units. This unit also monitors health telemetry of the detector.

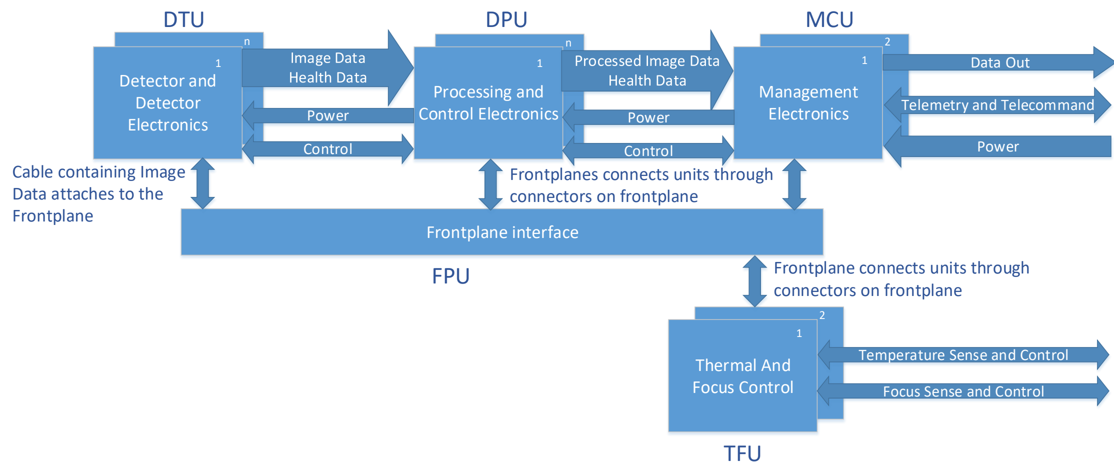

Figure 4-4: Block level representation of Alternate-4. For simplification only main interfaces are shown. The design alternate has equal number of DTUs and DPUs, i.e. one DPU for each DTU. The data out interface has two channels (main and redundant) from each MCU. TMTC and Power interfaces are also redundant interfaces for each of the MCU. Each of the MCU and TFU has standby (redundant) unit.

The Management Controller Unit receives power from the satellite and converts it to the required levels to be used for components on the MCU and for the components on the rest of the units. The Management Controller Unit is responsible for all the communication with the satellite and other subsystems. It employs a high-speed multiplexer that receives processed data from all the Data Processing Units and after multiplexing it sends it to the PLS on two (main and redundant) data channels.

The Thermal and focus control electronics is the same as Alternate-3. The front plane unit interconnects the units for routing the signals between the units as shown in Figure 4-4. The harness from the detector units is attached to the front plane connectors. The front plane contains all the data connectors and communication connectors. The front plane interconnects the MCU, DPU and the TFU by routing the signals between the units as shown in Figure 4-4.

4.2.4.1 Pros

- Reduced number of output data channels and thereby reduced number of harness.
- Dedicated unit for thermal and focus control.
- The detector PCB performs power regulation for the detector that guarantees clean power signals for detectors.
- Equal number of processing electronics units as that of detectors units simplify the design with the use of smaller processing Ics.
- The Management Controller Unit is responsible for communication with the bus, which simplifies the overall design.
- Similar design for all the detector units.
- Similar design for all the processing electronics and control units.

4.2.4.2 Cons

- Complexity added to Management Controller Unit by including a high-speed multiplexer.
- High speed links are required to send the image data to the PLS.
- Increased number of units for the design (compared to alternate-1 and alternate-2).
- The supporting electronics for the detector unit is on the detector unit with additional heat dissipation. This is an important consideration as thermal distortions may cause pixel mis-alignment and require more design effort for the thermal design to maintain position and the required alignment at pixel level.

4.2.5 Trede-off Criteria and weighting

The alternates represent different options for the data output interface. In the requirements it is mentioned that the output will be serialized LVDS, but the number of output channels were TBC (to be confirmed). This trade study will result in the confirmation of that.

All these alternates comply with this requirement. However, there is no requirement set for the output data rate. A weighting of criteria [9] is established to judge these alternatives on the basis of subjective weighting that assigns a score to each of the evaluation criteria and the distribution of points among the criteria. The criteria and scores are also discussed with the designers and the chief system engineer. The distribution of points shows the relative importance of the criteria in comparison to each other. The alternatives are assigned scores in the range of zero (0) to five (5) in each alternate for each of the criteria and then multiplied by the weightage. (The scores are assigned on the basis of best estimates that can always be challenged and recursion occurs as the program matures [9]). Final scores determine the preferred alternative.

The weighting criteria and the basis of weighting is explained in the following:

Performance: Performance is how well different design alternatives accomplish the required task for the completeness of IES. The power lines for the detector in Alternate-1 are more susceptible to noise since the power of the detector is coming from DPU. Whereas in other alternatives, the required power regulation for the detectors is performed on the detector PCB and less prone to noise for better performance. The detector units of Alternate-2,3, and 4 dissipate heat that can affect the alignment due to thermal effects of detectors and their electronics' heat dissipation, but the major contributor of this heat dissipation is still the detectors itself.

The thermal performance of Alternate-1 and 2 is not very good as it handles a lot of power dissipation on its Management Controller Unit beside performing thermal and focus control. Alternate-3 and Alternate-4 offer better performance as they have separate units for thermal and focus control and has better thermal management and performance.
So, in trade off, Alternate-3 and Alternate-4 offers best possible performance as compared to Alternate-1 and Alternate-2.

Reliability: Reliability rating is based on the general criteria without going into detailed reliability calculations (using software etc.). The criteria used for reliability rating is:

a) Safety factor and over specification: a pre-determined safety factor is set for different attributes on the basis of practices and previous experiences of the organisation, for example, the harness shall have 5% additional lines for signals, the efficiency of DC-DC converters will have 10% margin for estimations, the resource utilisation (of controllers' memory or FPGA resources) should be kept at 50-60%. These kinds of safety margins can be achieved with all the alternates easily.
b) Parallel arrangements: the use of parallel design chains to accomplish the similar tasks to support the overall function. Series arrangements are given a lower reliability rating.

Alternate-1 have more series-like architecture, where detectors are connected to dual redundant Data Processing Unit. Alternate-2 is more parallel than Alternate-1, where the chains of DPUs and detector units and the output data channels are parallel.

Alternate-3 has also parallel chains of DTUs, DPUs and output data (as Alternate-2) and separate Thermal and Focus Control unit connected to dual redundant Management Controller Unit.

Alternate-4 has the same arrangement as Alternate-3, except its output data channels are not parallel as in Alternate-2 and Alternate-3.

c) Redundancy (backup): A redundant unit is in reserve and comes into operation only when the main unit fails. All the alternates offer adequate levels of redundancy of units.

d) Extent of Fail-safe design: The inherent risk of failure for which the cost of any of the strategies would be prohibitively high. For example, having separate chains for DTUs and DPUs provides a better safety against the failure than the other non-parallel arrangements. Because in the former if one DTU or DPU fails the performance drops by 1/6 (Alternates-2, 3, and 4), but for the latter case if one Data Processing Unit fails the performance drops by half (Alternate-1).

Based on the above discussion and the trade-off between the reliability considerations, the scores for each Alternate-Are assigned.

Ease of manufacturing/ Effort: Ease of manufacturing indicates the effort for designing and fabrication that is required to achieve the design. This includes setting the components together and all the design steps that include schematics, analysis and layout, fabrication and software/ firmware. Alternate-1 has a very complex Data Processing Unit as it has to receive the data from six detectors and after processing has to multiplex the data on output data channel Management Controller Unit is also a complex unit in Alternate-1 that has to regulate the power for all the units and perform bus communication as well as to perform the thermal and focus control functions. This requires complex hardware (electronics, mechanical and thermal) and firmware design and in-turn more design effort and man hours.

Alternate-2 has same level of difficulty for the Management Controller Unit but the Data Processing Unit is much simpler and also some of the design is put on the detector unit that distributes the functionality and makes the design more modular and less complex. The replication of DTU-DPU chains makes the design simplified.

Alternate-3 has the same design for detector unit and Data Processing Unit as for Alternate-2 and it also has simpler Management Controller Unit by separating the thermal and focus control functionality. Whereas Alternate-4 has same design except that the Data Processing Unit sends the data to the Management Controller Unit that multiplexed the data and send on the output channel. This makes the hardware and firmware design of MCU a bit more complex as compared to Alternate-3.

Mechanical design and manufacturing of Alternate-1 is simpler than rest of the alternates as other alternates (2, 3, and 4) require additional frames/ slots in the mechanical housing to accommodate Data Processing Unit. Also, Alternat-3 and Alternate-4 require additional frames/ slots for TFU.

Complexity: Design complexity indicates how clearly different elements (of hardware and firmware) of the design alternatives are interacting with each other to fulfil the functions. As discussed, the electronic design of Alternate-1 is more complex design, then comes Alternate-4,

and Alternate-2 and Alternate-3 are even less complex. The thermal design for Management Controller Unit of Alternate-1,2 and 4 is considered to be more complex than Alternate-3.

Maintainability/ future upgradability: Maintainability or future upgradability is defined by how easy it is for a design to maintain and to adopt the changes to meet the future enhanced performance requirements. This kind of possible upgrades depend on the sensor technology changes that may include the use of detector with increased number of spectral channels, increased number of detectors for increased swath width, and increased number of detectors for enhanced GSD (for e.g. with smaller pixel and/or better performance) with same or increased swath. Alternate-2 and Alternate-3 are more adaptable for upgradability than Alternates 1 and Alternate-4 because of having more modular design and are capable to accommodate the above-mentioned possible changes with lesser modifications. Also, because of more modularity, Alternate-2 and Alternate-3 are easier to maintain in case any of the units need replacement.

Ease of Testing: Ease of testing is characterised by the modularity of the design. More modular design alternatives are easy to test at unit levels and then integrated testing also becomes easy to perform. Therefore, more modular designs are given higher ratings than the less modular and complex design Alternates. Alternate-1 is less modular of all the alternates because to test the Data Processing Unit and the data output interface all detector units need to be attached to it. And thermal and focus functions can only be tested with the Management Controller Unit. In Alternate-2, each detector unit and its corresponding Data Processing Unit forms a separate chain. There exists number of chains equal to the number of detectors units with the data output interface and each such chain that can be tested separate to rest of the design. But, similar to Alternate-1, thermal and focus functions can only be tested with the Management Controller Unit. Alternate-3 offers the best modularity among all the alternates where each chain of DTU-DPU chain can be tested separately with the data output interface, thermal and focus functions can also be tested separately, as well as the Management Controller Unit can be tested separately and then, after integration the whole design can be tested and verified. In Alternate-4, to test the output data channels chains of detector unit with their Data Processing Unit need to be attached to the Management Controller Unit because the output data path goes through the Management Controller Unit, however, thermal and focus functions can be tested separately.

Availability: Availability is the ease of getting the components and parts for the design. For example, a ready-to-use or already developed solution is given higher rating than a customised solution. The difference among the alternates in terms of availability of components is found to be the use of high-speed harness with large number of signals and high-speed MUX as required in Alternates 1 and Alternate-4.

Cost: Higher costs are given lower rating than the lower costs. Costs of the alternates are estimated on the basis of critical components for e.g. FPGA, processor, multiplexer, harness, PCB and mechanical housing, and relative time (man hours). In Alternate-1, the MCU and the DPU have more complex PCBs and the harness is high speed. The critical components on the DPU unit require more resources to handle, process and output large amount of data with enough resources (with resources margin) and high-speed MUX. The controller on the MCU also requires more resources to perform bus communication, Telemetry Telecommand handling and thermal and focus control functions. In Alternate-2, the design employs more DPUs, but these are smaller and much less complex PCBs that fit into the standard panel size of PCB manufacturers, therefore doesn't make any difference in the cost, so it will be cheaper than Alternate-1 because of less complexity. The MCU remains the same. The harness is also not very high-speed as the data is split for each detector. But more cables are required to send the output data. The FPGAs for data processing and output don't require very large resources but the number of FPGA increased as each DPU contains one FPGA. The controller on the MCU is same is in Alternate-1. In Alternate-3, the harness and PCB designs of the DPU remains the same as that of Alternate-2, whereas, the MCU is simpler with a smaller controller, but the separate thermal and focus control unit employs additional PCBs and controllers in the design. Alternate-4 requires a bigger controller (in terms of hardware resources), high-speed MUX and (a smaller number of) high-speed harness as compared to Alternate-3, however a smaller number of cables of high-speed harness with large number of signal lines balances the cost of more cables of relatively lower-speed harness and lesser number of signal lines.

Table 4-2: The comparison of Alternates for PEA using weighted criteria.

Criteria	Weight	Alternate							
		1		2		3		4	
		Score	Weighted score	Score	Weighted score	Score	Weighted score	Score	Weighted score
Performance	25	2	50	3	75	5	125	5	125
Reliability	20	2	40	3	60	4	80	3	60
Ease of Manufacturing/ Effort	15	2	30	3	45	4	60	3	45
Design Complexity	15	2	30	3	45	4	60	3	45
Maintainability/ Future upgradability	10	2	20	4	40	4	40	3	30

Criteria	Weight	Alternate							
		1		2		3		4	
		Score	Weighted score	Score	Weighted score	Score	Weighted score	Score	Weighted score
Ease of Testing	5	2	10	4	20	5	25	3	15
Cost	5	3	15	4	20	3	15	2	10
Availability	5	3	15	4	20	5	25	3	15
	100		210		325		430		345

4.3 Alternatives for the Focal Plane Assembly

For the FPA design, following are the important considerations that are regarded as inputs to the design Alternates:

1. The OPS can provide a circular image plane with diameter of 172mm that corresponds to a 11km swath on ground at 0.45m GSD if the pixels are arranged in single row of pixels. To fulfil the swath width requirement with 0.4m GSD (goal, with 11km swath width goal) 192.5mm is required if all the pixels are aligned with each other, with no across-track discontinuity or gaps between the pixels. For 0.5m GSD (threshold, with 11km swath width goal) it is 154mm. This defines the two extremes if a single pixel line would have been used the imaging and this would have been the required diameter of the circle of the image plane. But it is required to perform imaging in multiple spectral bands and for each band there are rows of pixels (for performing TDI), which implies that a rectangular area required on the image plane. Also, a single detector doesn't have enough pixels to fulfil the swath width requirement and therefore multiple sensors are required to be used. The detectors have a die around the active pixels' area that prevents the pixels to be placed next to each other with continuity even if the detectors ICs are placed side by side with physically no gap between the detector ICs. Therefore, these multiple detectors are to be used in a staggered arrangement to cover the required swath width with no across-track gaps. But this kind of arrangement would have along-track separation between the detectors (that is also temporal separation). Due to multiple rows of pixels and the staggered arrangement of the detectors, an inscribed rectangular area is required. The along-track length of this rectangle depends on the detectors' separation that in effect defines what swath width can be achieved. This size of image plane is a preliminary input from the OPS and the possibility is that it would be optimised in the later phases. Therefore, the FPA design considers and makes provisions in the design to

accommodate these optimization results and to reach the goal as far as possible. The same was communicated to the customer and got their consent for design to proceed.

2. The OPS requires an additional 1mm margin (0.5mm on each side) for extra pixels to be placed on the image plane across-track to compensate the beam steering caused by the focus adjustment mechanism to adjust the focus of the payload. (The focus adjustment mechanism is part of OPS and cause the beam steering only in the across-track length of the image plane)
3. The IES can support multiple TDI stages per spectral band to fulfil the SNR requirements. To maintain the MTF performance for the number of TDI stages requires increased stability from the satellite attitude control system [16] [17]. An indication of the required platform stability for the number of TDI stages is based on limiting the linear motion smear to 10% of a pixel [17]. The stability budget items are to be provided by the satellite. The stability of 1mdeg/sec is taken as the worst case for the calculations (WorldView-1 at an orbit altitude of 600 km, a GSD of 1 m and for a 96 TDI stages has 25 μrad/s (~=1.4mdeg/sec) [18].
4. In order to compensate for rotation of the Earth under the satellite during imaging, the satellite will need to perform a roll or yaw manoeuvre. Without this compensation, across-track pixel smear causes the drop in the MTF [19] and may cause discontinuity in the swath width [20]. The yaw error budget items are to be provided by satellite. For the estimation the yaw error it is assumed to be 0.5mdeg/sec [21].
5. An overlap of pixels between adjacent detectors is to be provided in order to ensure there are no gaps in the resulting images that depend on the along-track separation between the detectors (Appendix A), with an estimation that 100 pixels are required for image processing [22].
6. For the FPA design, light is coming along the Z axis and +Z side is reserved to be attached to the telescope and -Z side is reserved for the heatsink to be attached to the satellite panel to take the heat off the FPA. So, the accessible sides of the FPA for Connector Plate(s) for routing the signals in/out of the FPA and placing connectors to be attached to the PEA are +/-X and +/-Y.
7. The detectors are to be first aligned relative to the FPA mechanical housing and relative to each other, bonded in place, and then the complete FPA is to be aligned with the telescope and attached to telescope.
8. The thermal design is of prime importance to achieve the dimensional stability to maintain alignment and focus (The thermal design of the Pleaides, for example, uses thermal gradient of less than 1 degree C for the detectors [23])
9. From the OPS inputs, the dimension of the FPA in Z-direction restrict the detectors to be placed at no more than 90±0.015mm from the telescope interface.

The above described inputs are the basis of different Alternates for the FPA given in the subsequent text.

4.3.1 Alternate-A

This concept is based on arranging the detector units in a flat plane, as shown in Figure 4-5. Seven detector units are placed in a staggered arrangement with the required overlap. The circle is representing the circular image plane with diameter of 172mm, whereas the detectors placed in 170.5mm length are exposed to the incoming light and pixels in 169.5mm are used for imaging since the OPS requires 0.5mm on both sides for focus adjustment. A width of 169.5mm offers 10.9km swath width coverage that fulfils the requirement of 10km while close to goal of 11km swath width. The overlap pixels between each pair of detectors are indicated with the red-outlined rectangles. In the Top View, the larger part of the detectors' arrangement, i.e. the upper four sensors, are placed near the centre of the circle to make the most of the encircled energy. It is shown that the along-track distance between the detectors is 49mm, which requires 176 pixels overlap between the detectors. The direction of Flex PCBs indicate that the connectors are to be placed at two sides of the FPA. The arrangement of sensors shows that the PCB width cannot exceed the across track width of detectors.

4.3.1.1 Pros

- Simple arrangement of detector units
- Easy alignment of the detectors.
- Less complicated alignment setup required

4.3.1.2 Cons

- The along-track distance between detectors is large and that causes the temporal separation of the imaging areas on the ground.
- The large along-track distance between detectors requires more pixel overlap.
- Thermal design of the FPA is complex because all the detectors are placed on a single plane close to each other.
- The PCB width is restricted by the across track separation between the detectors.

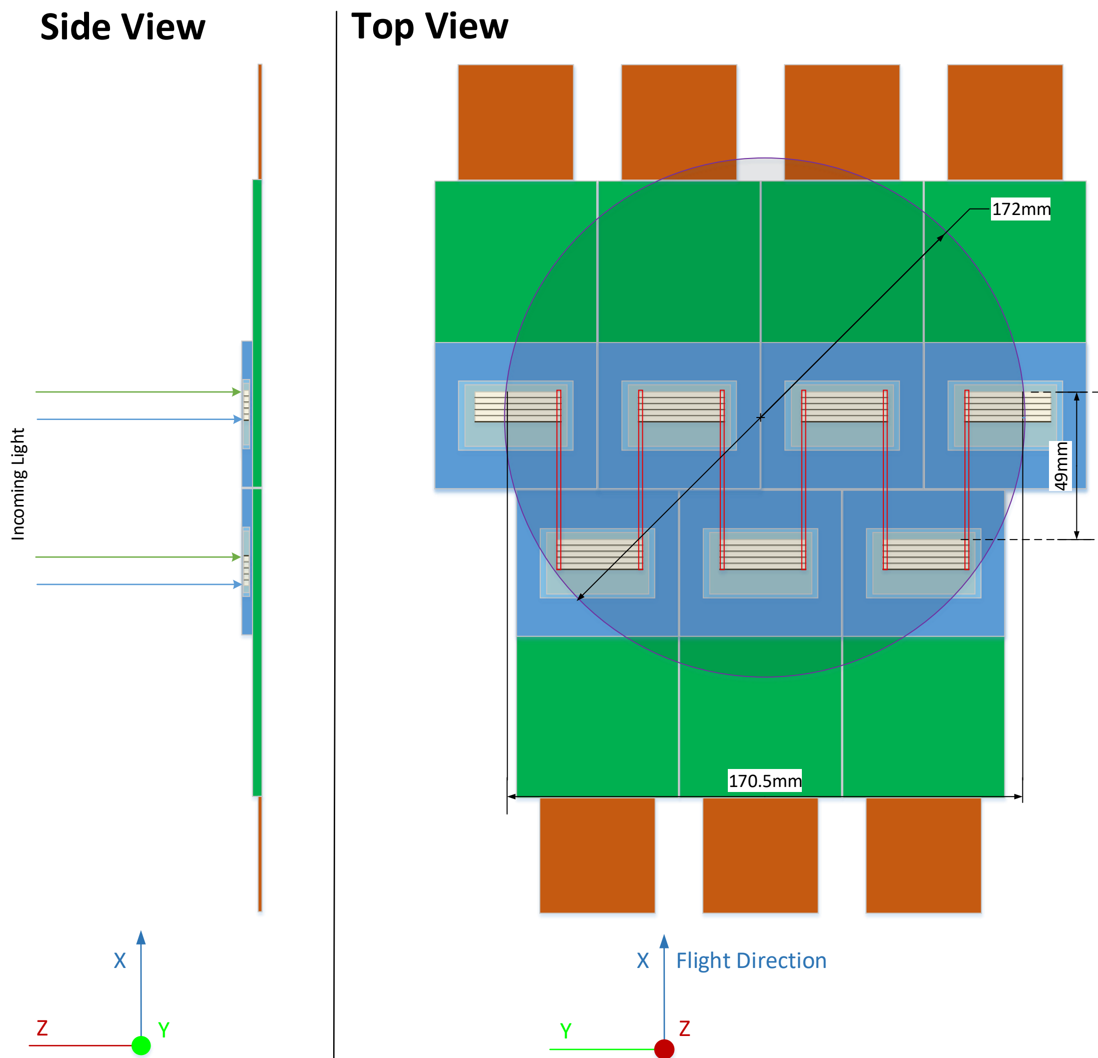

Figure 4-5: Alternate-A-The flatplane arrangement detector unit in Focal Plane Assembly.

4.3.2 Alternate-B

In this alternate design the detectors are place in two orthogonal planes. The light on the detectors placed in the XY plane falls at the incident angle of the incoming light whereas the detectors in the YZ plane receive the light reflected at 90 degrees with respect to the incident angle of the incoming light.

This alternate has two variants. The first variant uses a mirror to reflect light to illuminate the sensors placed in YZ plane, as shown in Figure 4-6.

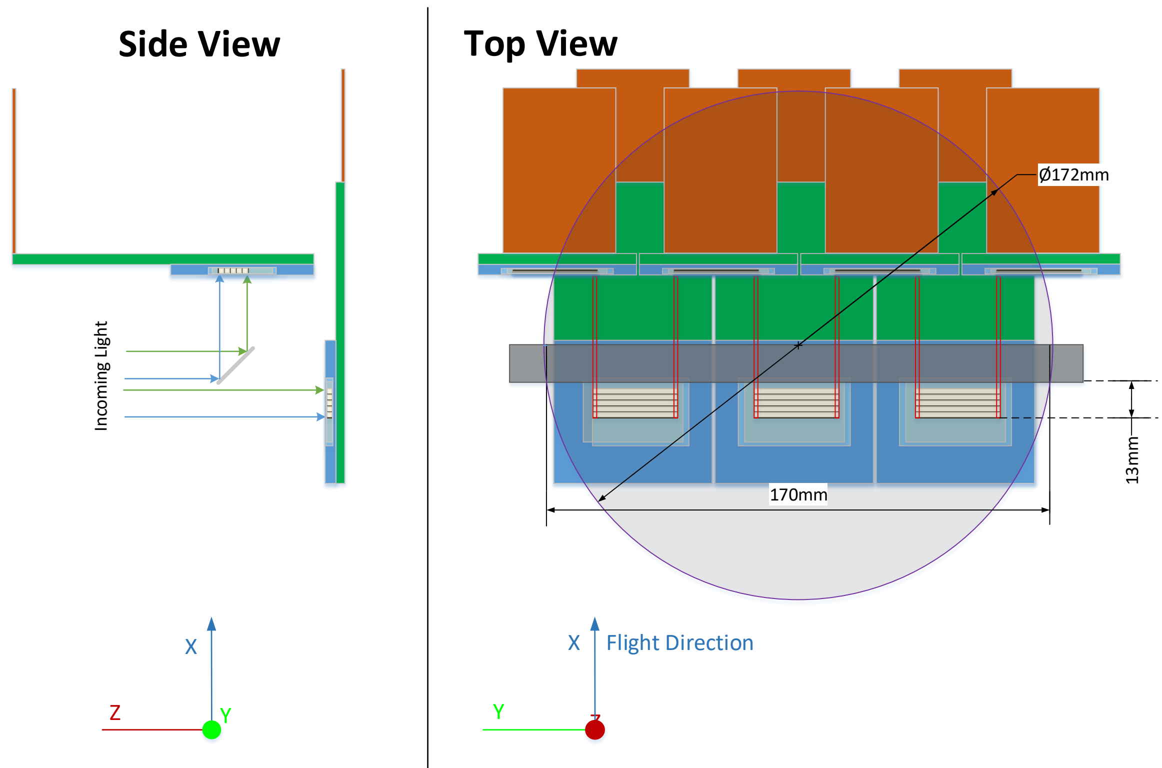

Figure 4-6: Alternate-B, variant-1- Focal Plane Assembly with mirror and arrangement detectors in two planes.

The downside of this layout is that mirrors will cause transmission loss due to the efficiency of the mirror coatings. The coating is applied on the top side of the mirror (at the first interaction of the mirror) to avoid any reflection losses at the glass-to-vacuum and vacuum-to-glass interfaces. With protected silver coatings, the reflection efficiency of 98% can be achieved [24] [25]. Mechanical design for holding the mirrors will make the design more complex. Figure 4-6, the circle represents the circular image plane with diameter of 172mm, whereas the detectors placed in 170mm length are exposed to the incoming light and pixels in 169mm are used for imaging since the OPS requires 0.5mm on both sides for focus adjustment. The 169mm width offers 10.8km (at 0.45m GSD) swath width coverage that fulfils the requirement threshold of 10km. The overlap pixels between each pair of detectors are indicated with the red-outlined rectangles. In the Top View, the mirror is placed near the centre to make the most of the encircled energy. The side view shows the incoming light rays that shows that the along-track distance between the detectors is 13mm because the light is reflected from the mirror and projected to the detectors placed in the YZ plane. This requires overlap of 120 pixels between the detectors. The direction of flex PCB indicate that the connectors are to be placed at one side of the FPA. The arrangement of sensors shows that the PCB width cannot exceed the across-track width of detectors.

This second variant uses one prism to reflect the light using the total internal reflection to illuminate the sensors placed sideways as shown in Figure 4-7.

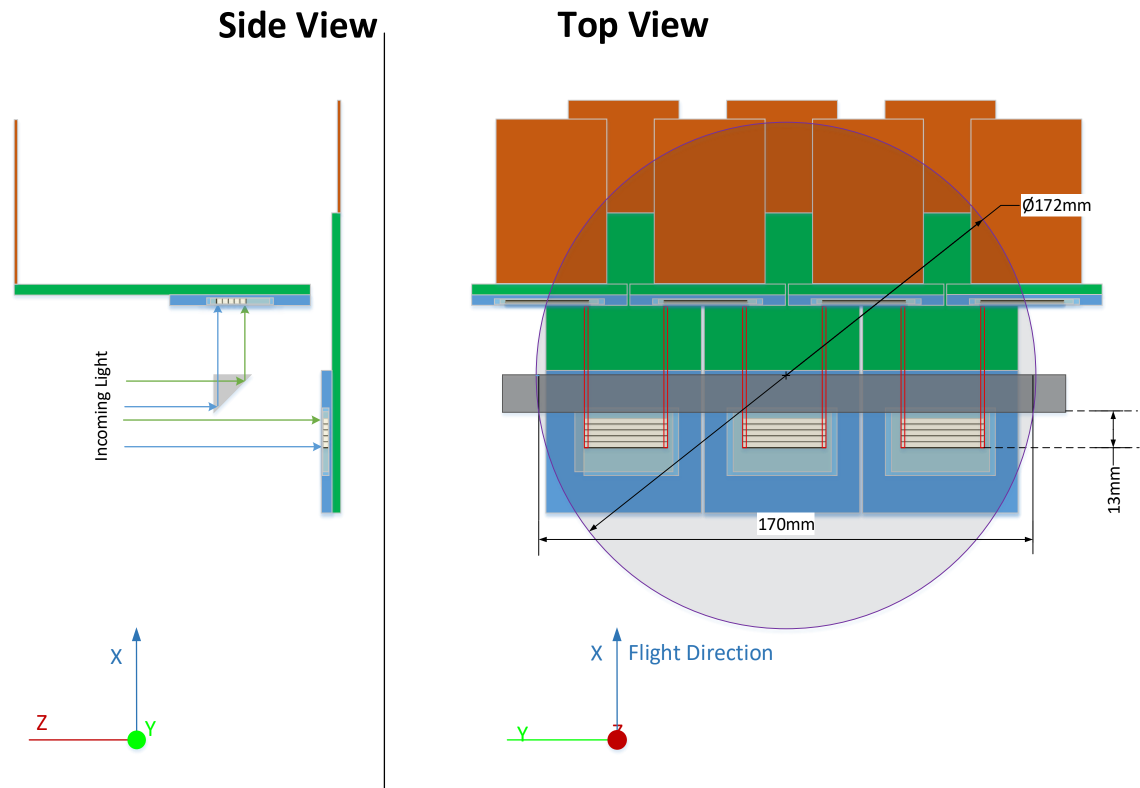

Figure 4-7: Alternate-B variant-2-FPA with prism and arrangement detectors in two planes.

The circle represents the circular image plane with a diameter of 172mm, whereas the detectors placed in 170mm length are exposed to the incoming light and pixels in 169mm are used for imaging since the OPS requires 0.5mm on both sides for focus adjustment. The 169mm width offers 10.8km swath width coverage (at 0.45m GSD) that fulfils the requirement threshold of 10km. The overlap pixels between each pair of detectors are indicated with the red-outlined rectangles. In the Top View, the prism is placed near the active area of the detectors placed in the XY plane. The side view shows the incoming light rays that shows that the along-track distance between the detectors is 13mm because the light is reflected by the prism using the total internal reflection and projected to the detectors placed in the YZ plane. This requires overlap of 120 pixels between the detectors. The direction of Flex PCBs indicate that the connectors are to be placed at one sides of the FPA. The arrangement of sensors shows that the PCB width cannot exceed the across track width of detectors.

The downside of this layout is that the prism will require complex mechanics to support the dimensions and weight of the prism for thermal and vibration loads. The distance of the detectors on the YZ plane needs to be carefully adjusted because the inclusion of the prism in the light path causes the optical path length difference [26] [27]. The transmission losses occur at the light

interfaces (glass-to-vacuum and Vacuum-to-glass) even with the use of anti-reflection coatings [28].

4.3.2.1 Pros

Variant-1:

- Single side of the FPA mechanical housing is used for detectors' data out.
- Smaller along track distance between detectors.
- Simpler thermal design because the detectors are placed in two planes.

Variant-2:

- Single side of the FPA mechanical housing is used for detectors' data out.
- Smaller along track distance between detectors even smaller than the variant-1.
- Simpler thermal design because the detectors are placed in two planes.

4.3.2.2 Cons

Variant-1:

- Complex mechanical design.
- Transmission loss due to efficiency of mirror.
- Alignment of detectors is difficult as compared to Alternate-A.

Variant-2:

- Although the Total internal reflection provides better efficiency than the mirror but transmission losses at the interfaces makes the efficiency lower even after the use of AR coatings.
- More complex mechanical design than the variant-1 because of weight of the prism glass.
- Alignment of detectors is difficult as compared to Alternate-A.
- It was empirically agreed and decided, that due to transmission efficiency of the prism-based design and the more complexity of the mechanical design, variant-2 is not feasible to be pursued further for the trade-off.

4.3.3 Alternate-C

Alternate-C is an extension of Alternate-B but the detectors are arranged in three planes; two parallel planes facing each other and orthogonal to the third plane as shown in Figure 4-8.Two mirrors are used to reflect the incoming light to the two planes in YZ whereas the detectors in the XY plane receive the incoming light directly. In the figure, the circle represents the circular image plane with diameter of 172mm, whereas the detectors placed in 170mm length are exposed to the incoming light and pixels in 169mm are used for imaging since the OPS requires 0.5mm on both sides for focus adjustment. The 169mm width offers 10.8km swath width coverage that fulfils the requirement threshold of 10km. The overlap pixels between each pair of detectors are indicated with the red-outlined rectangles. In the Top View, the mirror is placed

near the centre of the image plane to get the maximum utilisation of the encircled energy. The side view shows the incoming light rays that shows that the maximum along-track distance between the detectors is 27mm (This requires overlap of 142 pixels between the detectors). Light is reflected from the mirrors and projected to the detectors placed in the YZ plane and the direction of reflection of light is controlled by the tilt of the mirrors. The direction of Flex PCBs indicates that the connectors are to be placed at two sides of the FPA. Because of the arrangement of detectors in three rows, the gap between detectors allows the PCB width to exceed the width of the detectors.

4.3.3.1 Prons

- The design offers more better thermal management by having more planes to use for heat dumping.
- The gap between the detectors provides more area for components placement on the detector PCB and helpful in the signals' routing on the PCB

4.3.3.2 Cons

- The mechanical design is more complex than Alternate-A and B by having two mirrors.
- Larger along-track distance between the rows of detectors.
- Alignment of detectors in two planes is more difficult as compared to Alternate-B.

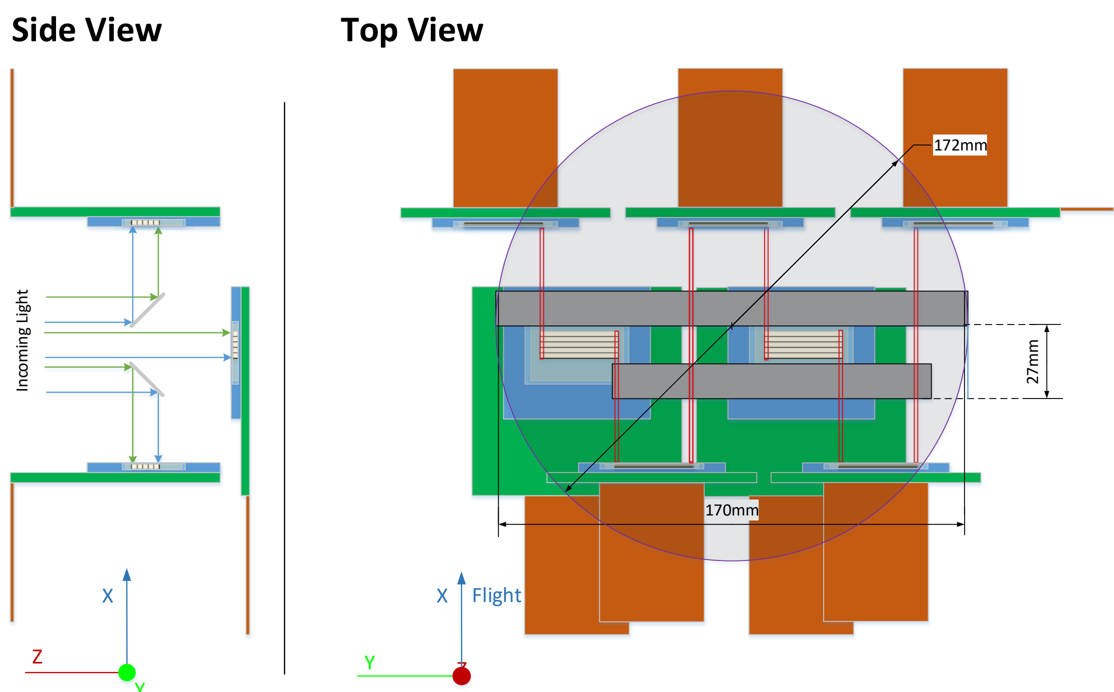

Figure 4-8: Alternate-C-The arrangement detectors in two YZ planes and one XY plane of Focal Plane Assembly.

4.3.4 Alternate-D

This alternate utilizes the concept of super-resolution for enhancing the resolution of the design by maintaining the 0.5pixel offset between the pixels [29]. The detectors on the Side ‘a’ are arranged at half pixel displacement arrangement from each other for super-resolution. Similarly, the detectors on the Side ‘b’ are arranged at half pixel displacement arrangement from each other for super-resolution. Sides ‘a’ and ‘b’ together provide the full swath width coverage with super-resolution. The circle is representing the circular image plane with diameter of 172mm, whereas the detectors placed in 170mm length are exposed to the incoming light and pixels in 169mm are used for imaging since the OPS requires 0.5mm on both sides for focus adjustment. The 169mm width offers 10.8km swath width coverage that fulfils the requirement threshold of 10km. The overlap pixels between each pair of the detectors are indicated with the red-outlined rectangles. In the Top View it is shown that the large mirror is placed near the centre of the image plane The side view shows the incoming light rays that shows that the largest along-track distance between the detectors is 49mm (this requires overlap of 176 pixels between the detectors). Light is reflected from the mirrors and projected to the detectors placed in the YZ plane and the direction of reflection of light is controlled by the tilt of the mirrors. The direction of Flex PCBs indicate that the connectors are to be placed at two sides of the FPA. Because of the arrangement of detectors in three rows, the gap between detectors allows the PCB width to exceed the width of detectors.

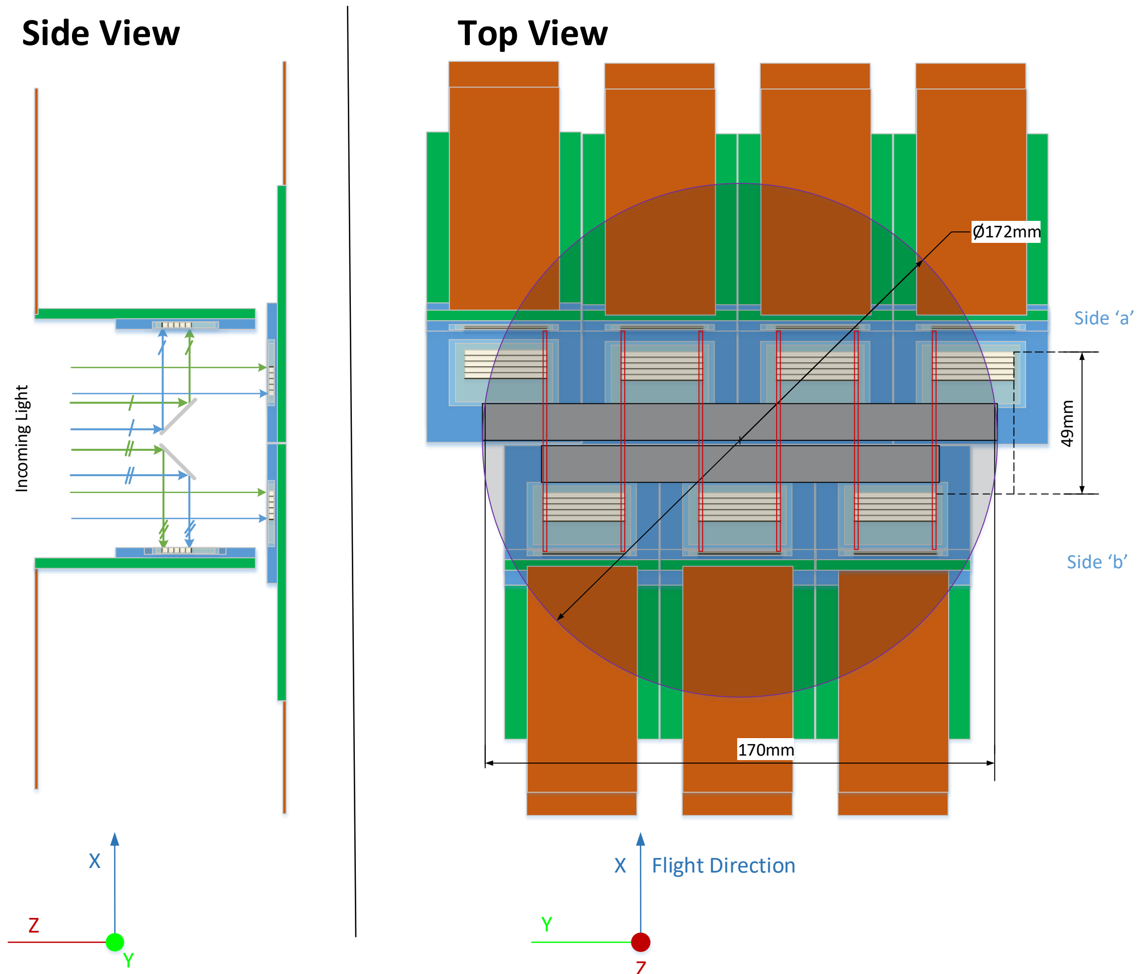

Figure 4-9: Alternate-D-The arrangement detectors for super-resolution in two YZ planes and one XY plane of Focal Plane Assembly.

4.3.4.1 Pros

- The GSD can be improved by arranging detectors for half pixel displacement achieving super-resolution through processing the image data on ground.
- The additional set of sensors also provides redundancy for normal resolution ensuring complete swath coverage in case of any sensor failure thus making the design completely Single Point Failure free.

4.3.4.2 Cons

- Very difficult alignment of detectors.
- Very complex mechanical design.
- Very complex thermal design.
- Complex PEA design with twice the number of DPUs required, twice the harness, more electrical power, more difficult thermal design and larger physical size.

- Very costly alternate, employing large number of devices, greater efforts and more man hours.

4.3.5 Trade-off Critera and Weighting

The trade-off of the FPA design alternates is presented below:

Performance: performance includes how well the alternate performs its functions. The functions to maintain detector position and convert light to signal are the prime importance. The function to maintain detector position also depends on the performance of thermal design. Alternate-A has large along-track separation that causes temporal separation on the ground. The thermal performance is difficult to achieve that can cause the pixel misalignment issues as a result of all the heat is being generated on the single plane. The optical performance of Alternate-B is slightly reduced because of the efficiency of the mirror. Whereas the placement of detectors on two planes provides better thermal management. The optical performance of Alternate-C is more reduced due to the use of two mirrors but the design provides even better thermal management by placing the detectors in three planes. For Alternate-D, the optical performance is much better than the other alternates (in terms of oversampling that potentially provides better GSD and MTF) but the thermal management is not good. The along-track distance between the detectors is largest in Alternate-D while the along track distance between detectors in Alternate-B is even smaller than Alternate-C.

Reliability: The reliability of Alternate-A is better than Alternate-B and C, since Alternate-B and Alternate-C both use mirrors as additional components. Alternate-D also has two mirrors but the use of additional set of detectors that can be used as redundant sensors make the reliability higher than the rest of the alternates.

Cost: Alternate-A being the simplest arrangement of detectors and having smaller number of components is the more cost-effective solution than the other alternates. Alternate-D is the most costly option as it has a lot more complexity in the design and more number of detectors that require more man hours and efforts for alignment of the detectors.

Ease of AIT: In Alternate-A, the detectors are placed in a flatplane that requires alignment with respect to FPA housing and with each other, but the signal lines are connecting through connectors that are placed on two sides of the FPA that makes AIT slightly more difficult. In Alternate-B the mirror is an additional element to be aligned. The signal lines are connecting through connectors that are placed on one side of the FPA that makes AIT easier. Alternate-C has two mirrors to align in addition to the detectors, and the signal lines are connecting through connectors that are placed on two sides of the FPA. Alternate-D requires alignment of twice the

number of detector units to align and the two mirrors. The signal lines are connecting through connectors that are placed on two sides of the FPA.

Manufacturability: The manufacturing of Alternate-A is the easiest among all the alternates. The placement of detectors on other planes and the mirrors in the alternates B, C and D make the manufacturing of these alternates more difficult. Also, the mounting and alignment of detectors in Alternate-D adds manufacturing difficulties.

Availability: The availability of alternates B, C and D use mirrors and the availability of these mirrors with exact characteristics makes their rating lower than that of Alternate-A.

Volume: volume or compactness is required based on the along track distance between the detectors and also the distance of the detectors on the FPA (requires to be 90±0.15mm) from the FPA-telescope mounting interface. The width of the detector PCB of Alternate-A and Alternate-D is restricted by the across track distance between the detectors. This increases the length of the PCB to accommodate the supporting electronics. For Alternate-B and Alternate-C, the across-track distance between the detectors allows the use of wider PCBs that can help reduce the length of the PCB and hence the overall volume. The detectors need to be at 90±0.15mm from the mounting interface of the FPA and with the preliminary estimates of the detector PCBs it is likely that they all fit well-within this dimension.

Mass: the mass of Alternate-A is less than all the other alternates where other alternates, which all have additional parts in the design that add more mass.
The scoring is based on the best estimates and can always be challenged with the developments happening in the project phases. After the weighted scores are summed, Alternate-B is the winner with a slight lead over Alternate-A.

Table 4-3: Trade-off among FPA candidate designs.

Criteria	Weighting Factor	Alternates							
		A		B		C		D	
		Score	Weighted score	Score	Weighted score	Score	Weighted score	Score	Weighted score
Performance	25	2,5	62,5	4,5	113	4	100	3,5	87,5
Reliability	20	4	80	3	60	3	60	5	100
Cost	15	5	75	4	60	3	45	2	30
Ease of AIT	10	4	40	4	40	3,5	35	2	20
Manufacturability	10	5	50	4,5	45	4,5	45	4,5	45
Availability	8	5	40	4,5	36	4	32	4	32
Volume	7	3,5	24,5	4	28	4	28	2	14
Mass	5	5	25	4,5	22,5	3,5	17,5	2	10
	100		397		404		363		339

4.4 Conclusion

Detailed brainstorming has been performed for the searching of the alternates. A trade-off analysis has been performed for the alternates and after detailed evaluation Alternate-3 of the PEA and Alternate-B of the FPA are selected for the baseline design.

5 BASELINE DESIGN

5.1 Introduction

After performing the trade-off among the candidate alternates and selecting the best option, this chapter describes the design that is based on the selected alternate. The functions of each of the unit of the design are described, critical components for the design are presented and the component selection strategy is explained. In the end the engineering budgets (estimates) for the design are presented.

5.2 Electronics Design Description

5.2.1 Overview

The electronics design of the IES consists of the Detector Unit (DTU), Image Data Processing Unit (DPU), Management Controller Unit (MCU) and Thermal Controller Unit (TCU). The DTU is a part of Focal Plane Assembly (FPA) and DPU, MCU and TCU are the parts of Processing Electronics Assembly (PEA). Each DTU in the FPA has its separate electrical interface with its respective DPU in the PEA forming seven independent DTU-DPU chains, Each DTU in the chain has an image detector for light-to-signal conversion and sending to the respective DPU. The DPU performs the processing of image signals and send the image data to the PLS. The MCU provides the IES interface to the satellite bus for power and Telemetry and Telecommand. It performs power isolation and regulation. A dual redundant CAN bus provides the Telemetry/telecommand interface with the satellite bus. A microcontroller performs the handling of the telecommands, telemetry and health monitoring of the DPUs and DTUs. The design has two MCUs in a cold redundant strategy. OPS temperatures are measured and control by the Thermal Control Unit (TCU) that has its separate power and communication interface with the satellite for the independent working of the TCU for maintaining the favourable conditions for the imaging.

The design employs seven DTUs, Each DTU has a detector. The detector is electrically connected to a multi-layer PCB with some of the internal layers extending beyond the rigid section in the form of a flexible PCB harness. This PCB includes a small amount of support

circuitry for the detector. The flex-PCB harness ends in a connector. The DPU forms rigid-flex-rigid construct and the connector side of this construct is mounted to the connector plate, located on the FPA.

The design employs seven DPUs, one for each DTU. The DPU performs the function of controlling the detector, reading the detector data, alignment/ reordering of data from different channels, perform binning, and tagging the image data. The DPU sends the high-speed serial data to the PLS through main and redundant high-speed serial channels. The DPU also collects the health telemetry of DTU, monitors the on-board telemetry and sends the combined telemetry to the MCU on SPI. The DPU receives the input voltage from the secondary power and generates the power for the DPU onboard electronics.

The TCU consists of power circuits, CAN bus, temperature measure input, heater drive circuits and onboard health monitoring. The OPS requires 20 heaters placed at different locations to be controlled and 40 thermistors for measurement. The design of the TCU is based on proportional control within the range (-10 to 20deg C) and on/off control outside the temperature range.

The front plane connects all the units of the IES subsystem for communication and signalling among them and the subsystems outside the IES. The subsystem functional block diagram is shown in Figure 5-1. The functionality of these units is defined in the subsequent sections.

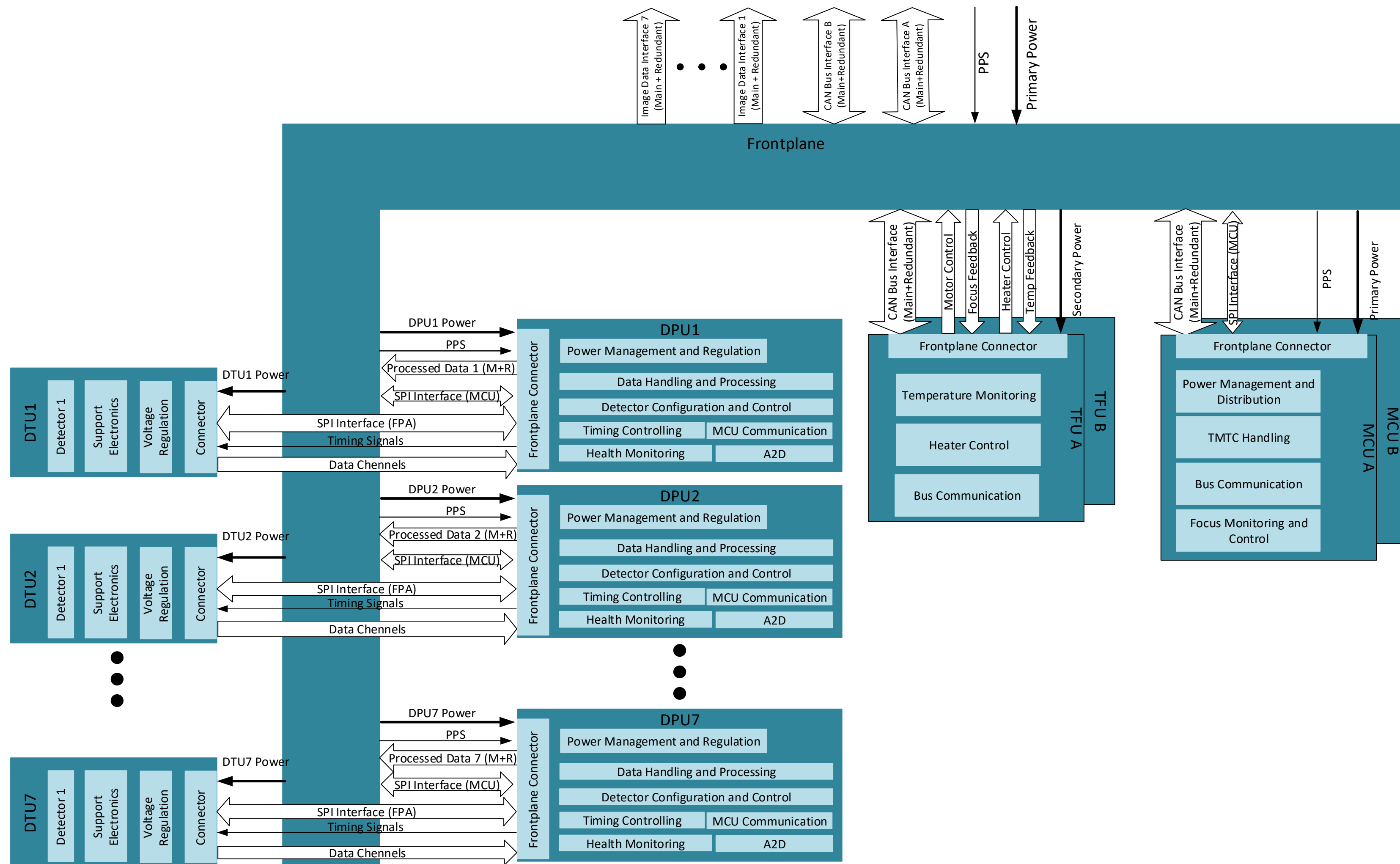

Figure 5-1: Detailed block Diagram of the Imager Electronics Subsystem showing the internal and external interfaces.

5.2.2 Focal Plane Assembly: Detector Unit (DTU)

The Focal Plane Assembly contains seven DPUs. Each DPU consists of Detector and rigid-flex-rigid PCB. The detector is 7μm x 7μm pitch CCD-in-CMOS detector. The PCB contains the Detector and the circuits required perform the required voltage regulation and for driving the sensor. The focal plane circuit provides the following main functions:

- Make the detector convert the light to digitized (LVDS) signal by;
  - Providing the detector the required power levels.
  - Providing the required sequence of power for detector start-up and turn-off.
  - Routing the timing signals to the detector chip.
  - Receiving the configuration parameters for the detector and providing the updated configuration parameters to the corresponding DPU on the SPI bus.
- Employ the health telemetry circuitry and send the health telemetry to respective DPU on the SPI.
- Send the overcurrent and latch-up event telemetry directly to the MCU.
- Output LVDS data to the corresponding DPU

The signal flow of the DTU is shown in Figure 5-2:

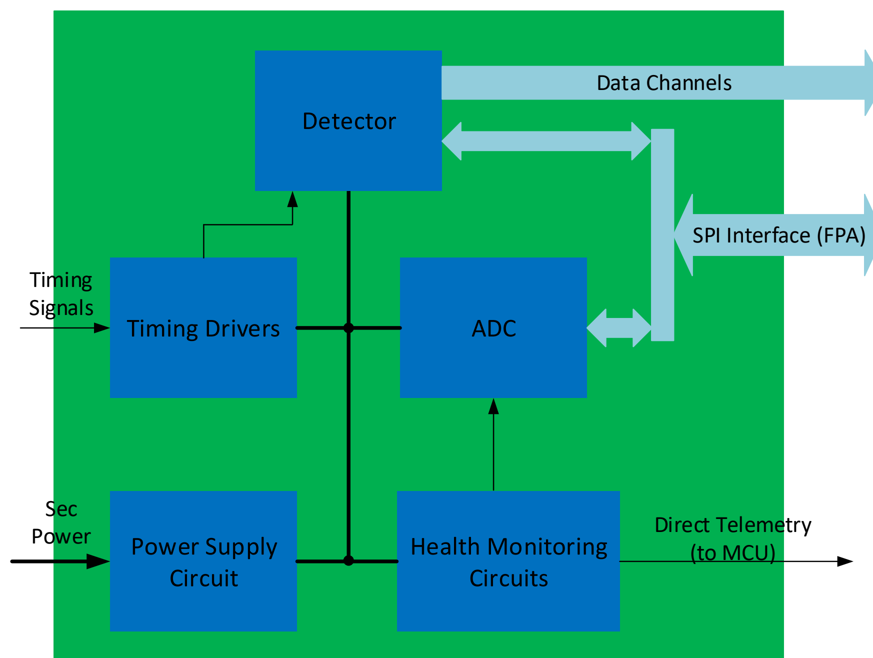

Figure 5-2: Block Diagram of Detector Unit.

The construction of DPU (flex-rigid-flex PCB) is shown in Figure 5-3.

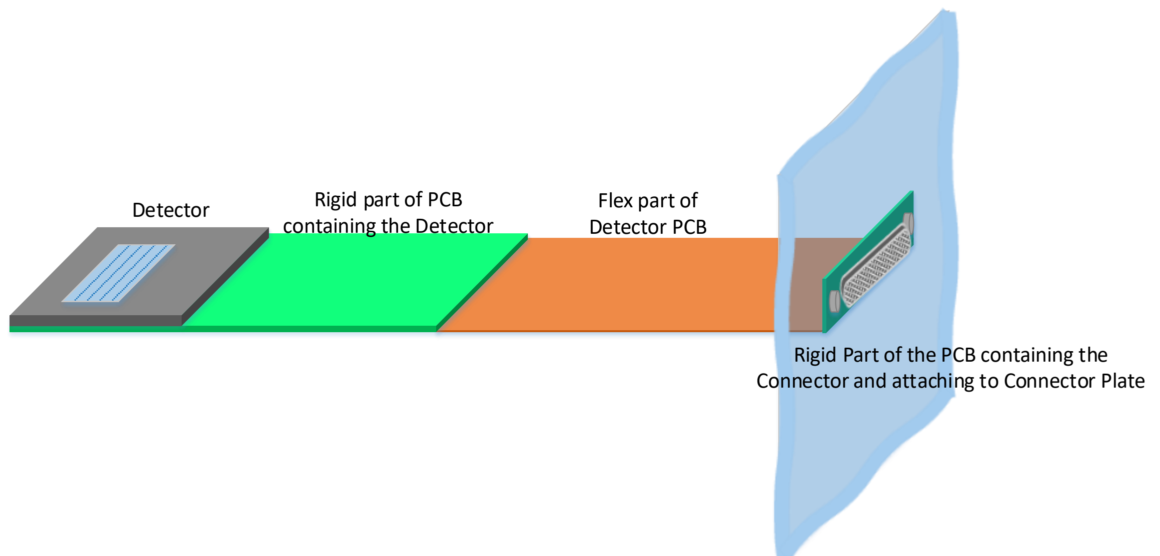

Figure 5-3: Rigid-Flex-Rigid construction of the DTU and attachment to the Connector Plate.

Characteristics of the detector are presented in Table 1 of Chapter 4.

Each interface of DPU (FPA) to the DPU (PEA) is shown in the Figure 5-4.

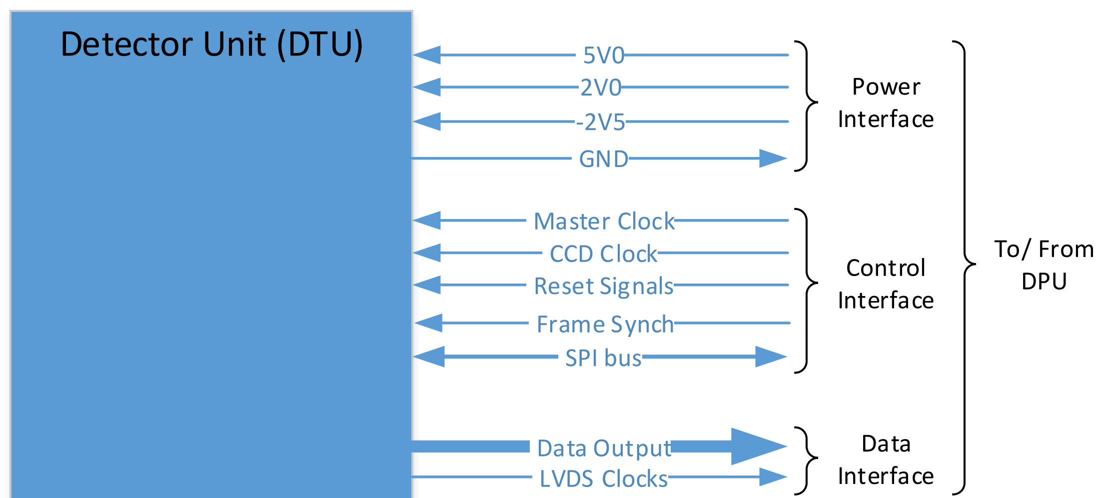

Figure 5-4: Interfaces of the DTU with respective DTU.

5.2.3 Processing Electronics Assembly: Image Data Processing Unit (DPU)

The DPU performs the operation of detector control and image data processing. The DPU receives the image data from the DTU and sends it to the bus after performing alignment, binning, tagging, and control operations. Each DPU performs the following main functions:

- Receive the detector data and perform data processing.
- Receive PPS and provides the time sequence signals to the DPU.

- Receiving the health telemetry of DPU and provide combined health telemetry of the DPU and DTU to MCU on SPI.
- Receive telecommands from the MCU on SPI. ell as giving the telemetry & telecontrol signals to the management circuit.
- Switching between the main and redundant configuration flash by receiving direct telecommand from OBC.
- Receive auxiliary data and transmit auxiliary data and image data to PLS.
- Receive the configuration parameters and setup detector's parameters.

The functional block diagram of the DPU is shown in Figure 5-5.

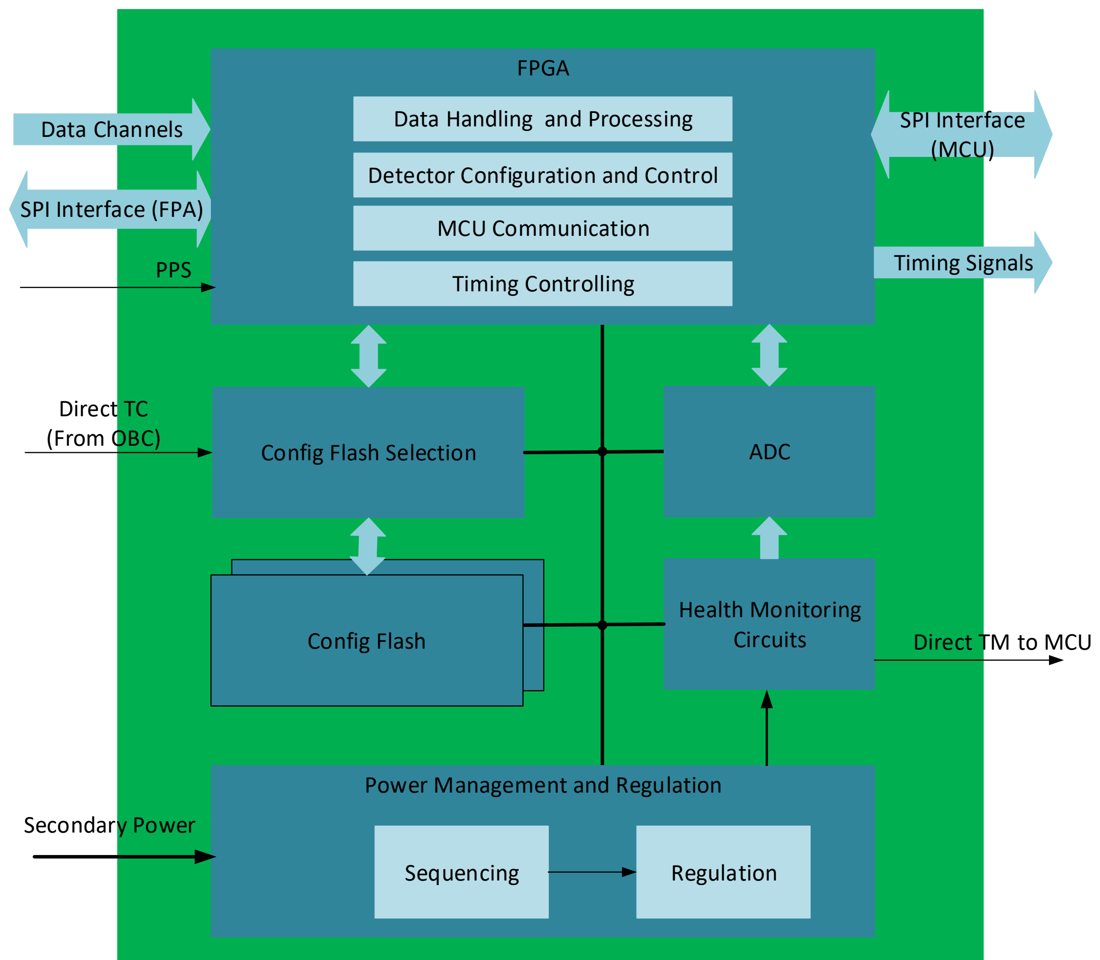

Figure 5-5: Functional Block Diagram of DPU.

The data processing is performed in the FPGA that is a chain of functions performed as shown in Figure 5-6 employed in the FPGA.

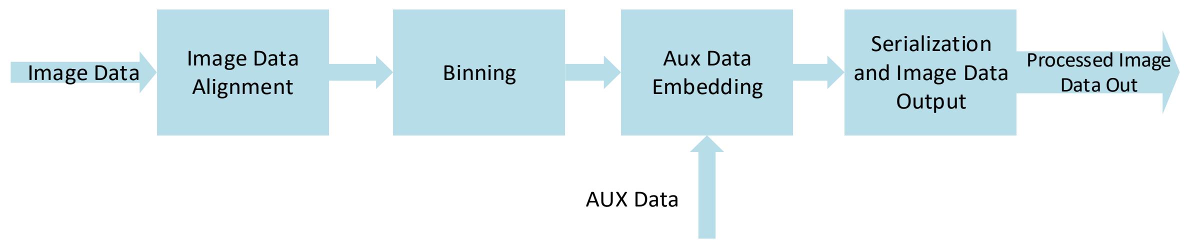

Figure 5-6: Data Processing chain of the FPGA

The detector configuration and control is also performed by the FPGA and the functional chain consists of the sequence of functions shown in Figure 5-7.

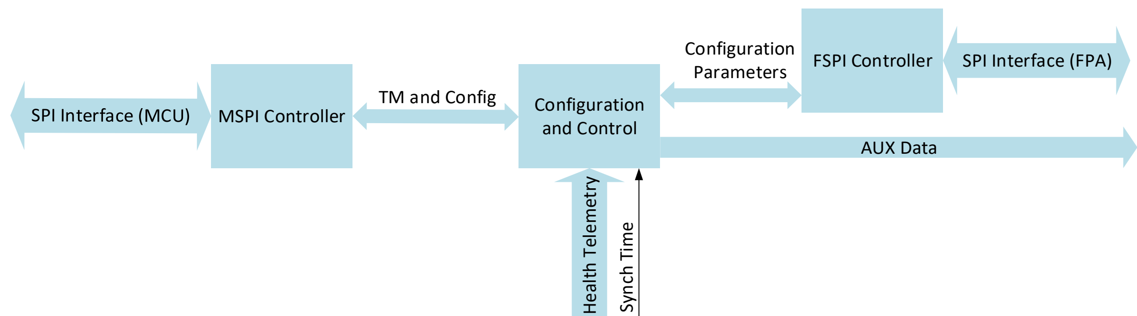

Figure 5-7: The Detector Configuration and Control chain of the DPU FPGA.

The timing controller receives the FPGA clock and PPS signal to provide all the required clocks and synch signals. These signals except the synch time are sent to the DTU. The synch time is sent to the configuration and control where it becomes the part of aux data (synch time has an accuracy equal to integration time and it is the time at which a row of pixels is imaged). Auxiliary data is embedded in image data and the combined data is sent to the PLS.

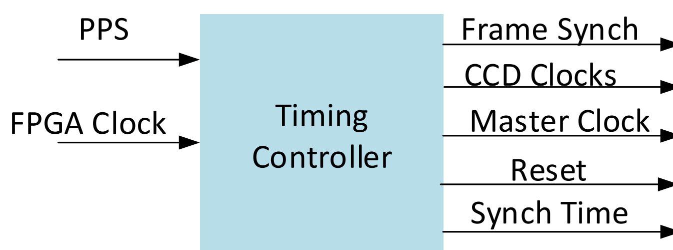

Figure 5-8: Inputs and outputs of the Timing Controller of FPGA.

Health telemetry circuits are the operational amplifier-based circuits that scales the input signal values to the levels acceptable for the ADC. These circuits also include comparators for critical current and temperature telemetries to be sent directly to the MCU in case of Latch-ups or overcurrent situations. Each DPU has following interface with the PEA for data output.

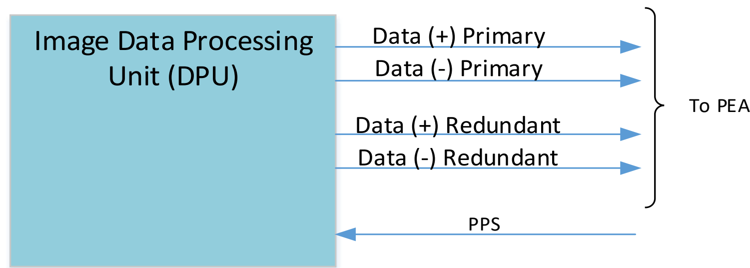

Figure 5-9: DPU to PEA interface for data output.

5.2.4 Processing Electronics Assembly: Management Controller Unit (MCU)

The MCU provides isolation between the primary and secondary power supplies, performs voltage (down) conversion and controls the power lines of all the DPUs and DTUs. A microcontroller performs the telecommand and telemetry interfacing and health monitoring of the DPUs and DTUs.

The MCU performs following functions:

- Receives the primary power from the satellite's Power Subsystem and converts the to various power supplies required by DTU, DPU and TCU.
- Perform power control functions for individual DTU and DPU turn off on latch up detection or over current conditions.
- Receive integration time, TDI settings and gain and offset settings on CAN bus to execute relevant settings.
- Receives the telemetry from the DPU and TCU.
- Perform communication on CAN bus for telemetry and working status sending, telecommand reception.
- Receive focusing command by CAN bus and controls the focus of the telescope subsystem by driving stepper motors.

The functional block diagram of the MCU is shown in Figure 5-11.

The power management and distribution section of the MCU provides the following main functions:

- converts the main power supply from the satellite to various power supplies required by the MCU electronics, DTU, and DPU.
- Sequence the power-on of regulators and circuits according to the required time sequence.
- provides Inrush (surge) protection and power isolation.

Main controller of the MCU performs the following functions:

- Receive and analyse CAN bus command, forward the time synchronization data, each parameter setting, and auxiliary data of the satellite to DPU.
- Collect the telemetry parameter from DPU and forward to OBC in the specified format.
- Receive and analyse CAN bus command and performs operation on the command.
- Control the focusing circuit through specified time sequence and achieve focus adjustment motor control. (the feedback from the motor is fed to the ADC. This feedback is a 0-5V analogue signal that comes from the position sensor installed in the OPS)
- Receive the direct command from OBC to switch the CAN bus.
- Set each parameter and forward the time synchronization data and auxiliary data to DPU.

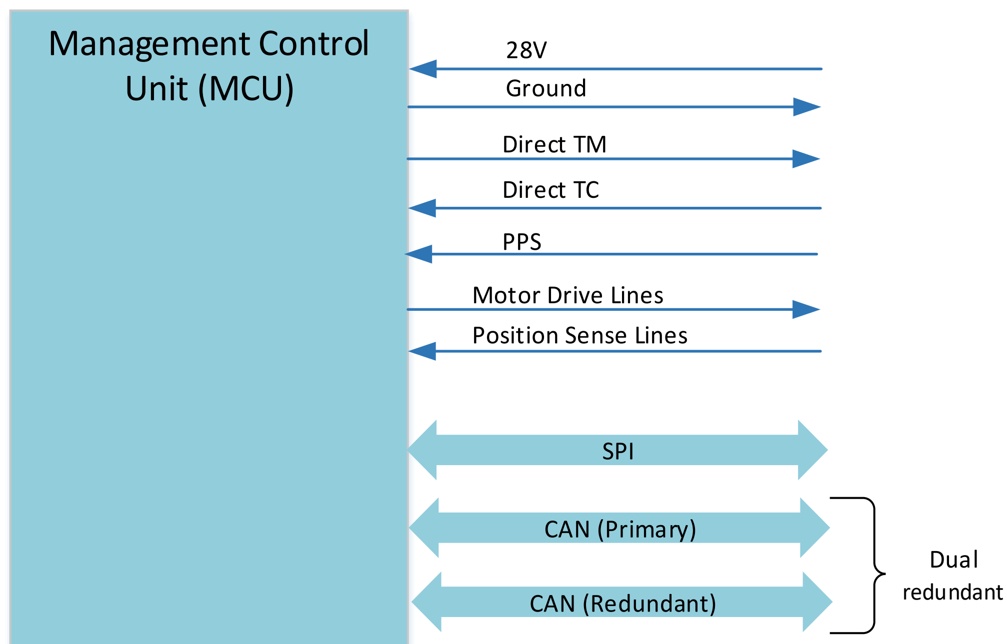

Figure 5-10: MCU interfaces.

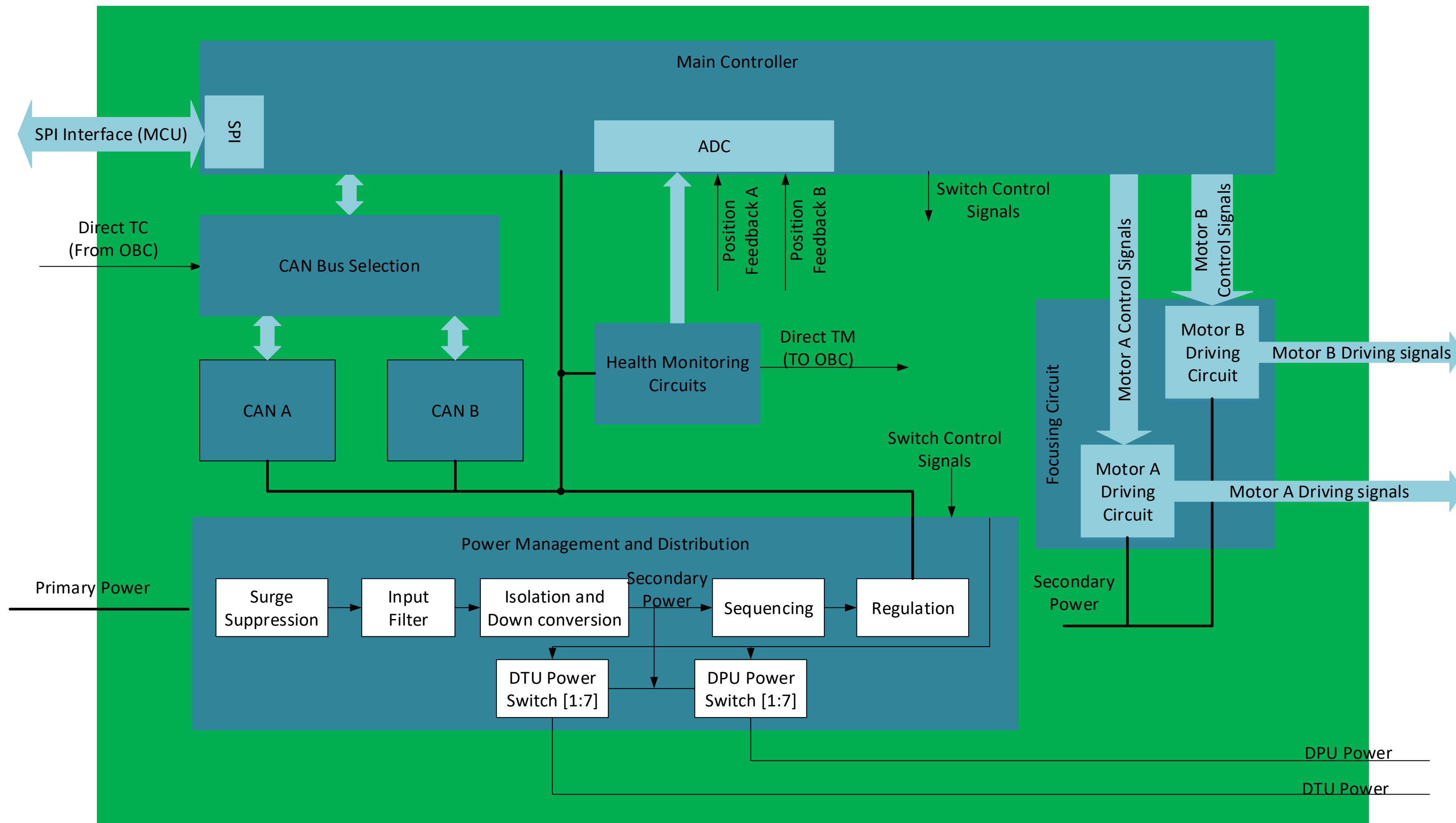

Figure 5-11: Functional Block Diagram of MCU.

- Receive the direct telemetries from the DTU and DPU for quick isolation in case of fatal errors/ high temperature or current rise of affected unit from rest of the subsystem to ensure safe operation.
- Receive the status of working parameters on the CAN bus after switching between the MCUs.

Table 5-1 shows the main technical parameters of MCU.

Table 5-1: Parameters of Management Controller Unit.

Item	Parameter
Quantity	Main and Redundant Management Controller
Power	28V±4V
Focus adjustment interface requirements	Step size 0.9°, Frequency 100Hz~500Hz
Communication (IES internal)	SPI
Communication (External)	CAN
Power consumption	Imaging : ≤7W Focus : ≤13W

5.2.5 Processing Electronics Assembly: Thermal Controller Unit (TCU)

The TCU performs the temperature monitoring and control of the OPS subsystem by employing proportional control. The functions of TCU are given in the following:

- perform accurate temperature control of the OPS subsystem.
- establish communication on CAN bus to achieve data exchange with the satellite with having main and redundant CAN bus.
- perform power management on board.

Due to large number of thermistors, an external ADC is used that is fed by the signals from the multiplexer after scaling. Interfaces of the TCU are shown in Figure 5-12:

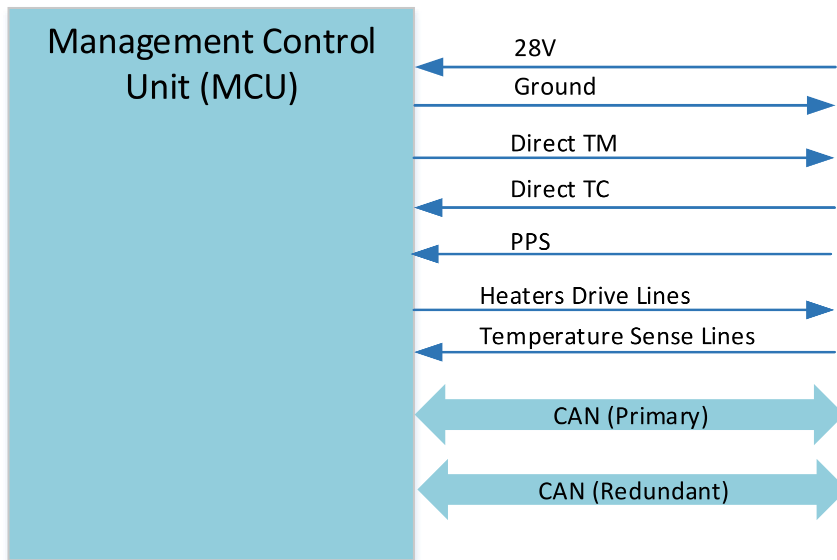

Figure 5-12: TCU interfaces.

The Functional block diagram of the TCU is shown in Figure 5-13.

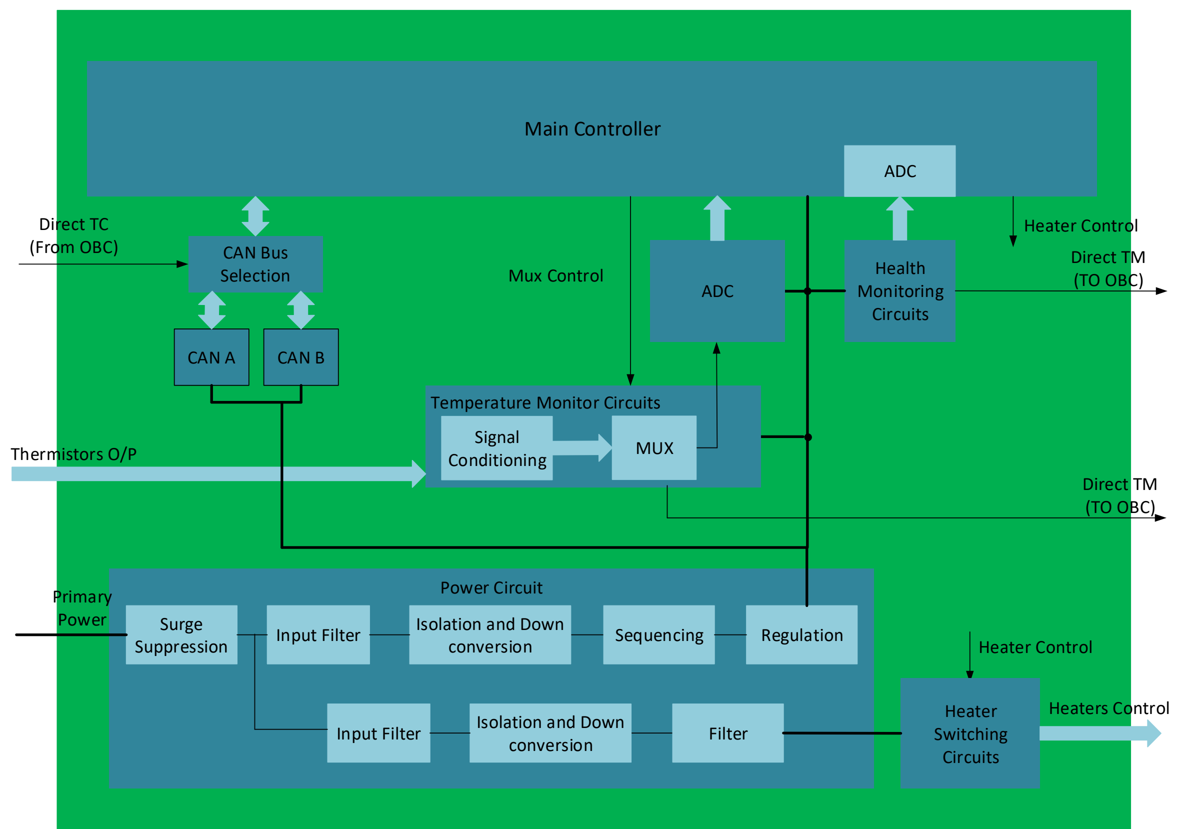

Figure 5-13: Functional Block Diagram of the TCU.

The power and communication bus is kept separate from the rest of the units because the TCU would be able to monitor the temperatures of the telescope before the imaging independently and can be configured separately. Table 5-2 shows the parameters of the TCU.

Table 5-2: Parameters of the TCU.

Item	Parameter
Input primary power voltage	28V±4V
Telescope Heaters	36
Thermistors	72
Power consumption	≤8.5W
Temperature accuracy (derived from requirements)	±0.1°C for temperatures range (-10~+20 deg C) ±0.5°C for temperature <-10°C and >+20°C)

5.2.6 Front Plane Unit (FPU)

The Front Plane Unit is connected to all the units of the PEA. On one side of the FPU all the connectors that are to be interfaced with the outside of the PEA (i.e. FPA, PLS, OPS, OBC, AOCS) are placed whereas on the other side the connectors that are going to the DPUs, MCUs and TCUs are attached as depicted in Figure 5-1. The FPU is helpful for the effective use of its area for placement of required connectors according to the interface requirements with the other subsystems and units, whereas on the other side it uses the Front Plane connectors for interfacing with the units inside the PEA, hence using both the sides for interfacing. This requires much less area than if the connectors would have been placed on the units directly and using the backplane for the interconnectivity among the PEA units because the physical separation between the units in the mechanical structure of the PEA and the dimension of the PCB limits the placement of the required number of connectors.

5.3 Components Selection

All the components in the design have prior heritage or have undergone the qualification tests for suitability of use for the required life-time and space conditions. For the component selection, preferred part list of the organisation was followed. However, for some cases, for example, the high (output) power DC-DC converters and MCU main controller are selected from the QPL of the customers by requesting them to suggest suitable components. To minimize the ground (return) loops and for better noise immunity and lower impedance [30] the twisted pair triples are used for the detector data, of which two of the lines are to be used for the differential signals and the third line carries the ground. It would increase the number of wires and the overall weight, but the improvement in signal quality is of more value. The critical components of the design are presented in Table 5-3

Table 5-3: Critical components of the IES design.

Item	Selected Part
Microcontroller	Siliconlab's C8051f120
FPGA	Xilinx's Viretx 5
Data/ Power wires	Axon shielded jacketed twisted triples for differential detector data [31] with 120 pin connector [32] Axon high speed microcoax interface for image data [33] Axon single wires for single ended and power signals
DC-DC Converters	12V (DCM Series) [34] 5V (DCM Series) [34]
CAN Transceiver	TJA1040

Note: Despite that the components will be selected form the preferred part list at this design stage, the designers will have the opportunity to choose components from different options inside the Preferred (or qualified) part lists. The trade-offs at component level, however, will be performed at the detailed design phase in future.

5.4 Engineering Budgets

Engineering budgets are presented in the following sections.

5.4.1 Power Budgets

The power is estimated by the detailed power break down [35] and working with the data sheets of the components for the power consumption estimates. The power consumption of different units during the different modes of EO payload are given in Table 5-4.

Table 5-4: Power consumption of IES units in different modes of EO Payload.

Unit / MODE	DTU	DPU	MCU	TCU	Total Power
Imaging Mode	49	42	5	125	221
Configuration Mode	0	0	6	125	131
Focus Adjustment Mode	49	42	27	125	243
Playback Mode	49	42	6	5	102
Error Mode	0	0	0	0	0

5.4.2 Data Budget

The data rate of the IES is presented in Table 5-5.

Table 5-5: Data rate of the IES.

Parameter	Value	Unit
No. of detectors	7	detector chips
No. of Pan bands per detector	1	band
No. of Multispectral bands per detector	1	bands
No. of Pixels per detector	4096	pixels
ADC Quantization	10	bits
Binning of Pixels in Pan Band	Nil	-
Binning of pixels in Multispectral Band	4	pixels
Flight Time per pixel (for 0,45m GSD)	65	µsec
AOCS aux data	100	bytes
Bits transmitted per pixel	16	bits
Total Bits of (Pan +MS) data per integration time	334080	bits
Total data rate	1.28	Gbits/sec

5.4.3 SNR Performance

The SNR of the IES is calculated using the method used in [36]. The transmission efficiency of the OPS is 59% that is used for these calculations. The SNR calculations are shown in Table 5-6 with the pixel binning for Multispectral bands (as the GSD of the MS band is four (04) times that of Pan band). The SNR is improved for the multispectral bands with the binning by a factor of *sqrt(pixel binning)* [37]. The SNR is also improved with the increased number of TDI stages [38], as shown in Table 5-6.

Table 5-6: SNR Performance estimates.

Spectral Band	TDI stages	Binning	SNR
450nm-800nm	1	Nil	27.0
	2	Nil	38.2
	4	Nil	54.0
	8	Nil	76.4
	16	Nil	108.0
	32	Nil	152.7
450nm-510nm	1	4x4	33.1
	2	4x4	46.8
	4	4x4	66.2
	8	4x4	93.7
	16	4x4	132.5
	32	4x4	187.4
510nm-580nm	1	4x4	40.3
	2	4x4	57.0
	4	4x4	80.6
	8	4x4	114.0
	16	4x4	161.3
	32	4x4	228.1
630nm-690nm	1	4x4	41.4
	2	4x4	58.5
	4	4x4	82.8
	8	4x4	117.1
	16	4x4	165.6
	32	4x4	234.2

6 ASSEMBLY INTEGRATION AND VERIFICATION PLANNING

6.1 Introduction

In this chapter the main constituents of the AIV planning for the IES are presented with verification events shared by different verification levels.

6.2 Verification of the IES

The IES verification plan is based on the flow as shown Figure 6-1, and aims at answering the following questions:

- Is the system built correctly?
- Does the system meet the end-to-end operational objectives?
- Does the system behave in a robust predictable way?

The whole process from NGO (needs goals and objectives) to the validated product requires planning that defines a logical flow for the verification and validation at different stages, i.e. a logical sequence to perform verification and validation of the design.

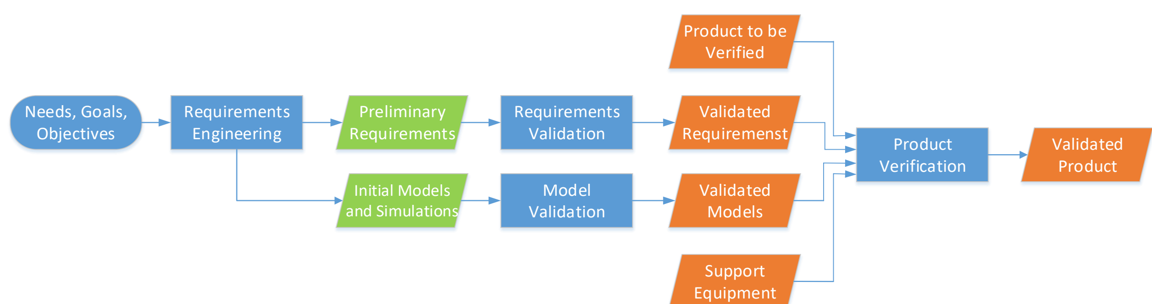

Figure 6-1: Complete Verification Flow of IES subsystem.

6.2.1 Verification Methods

The verification process of the IES shall be accomplished by one or more of the methods of verification as given below:

- Inspection
- Analysis
- Review
- Test

6.2.1.1 Inspection

Inspection provides a method for the verification of compliance with a given requirement with an emphasis on the verification/ observation of the physical characteristics with the use of special lab equipment. To perform the verification by inspection, standard quality control methods are used to verify the compliance with the requirements, manufacturing features, and compliance with document, drawings, and workmanship standards.

6.2.1.2 Analysis

Analysis is a method that uses established technical or mathematical models or simulations, algorithms, charts, graphs, or other scientific principles and procedures to provide verification of compliance to the requirement. Analysis techniques are used when:

- Accurate modelling and analysis is possible.
- Inspection is found not sufficient or adequate for the verification.
- The analysis can provide cost effective way of verification than testing.

6.2.1.3 Review-of-Design

Review of design is a verification method of performing formal assessment of presented data to provide evidence that requirements on the item are met. In general, it is applicable to data presented by external consultants, experts or subsystem/unit suppliers, design reports, engineering drawings and technical descriptions.

6.2.1.4 Test

The determination, by physical means, that the item can survive and/or operate in a particular environment and involves the application of established scientific principles and procedures.

Testing is selected as the principal method of requirements' verification when analytical techniques do not produce adequate results; failure modes exist which could compromise personnel safety, adversely affect flight systems, or result in a loss of mission objectives [39].

6.2.2 Verification Levels

The verification levels provide the basis that the verification shall be performed incrementally at product/component breakdown. Each requirement can be verified at one or more level. According to the plan, a detailed verification approach and descriptions are provided by each team in a dedicated document. The breakdown levels for the complete IES verification are:

- Subsystem level:
    - IES
- Unit Level:
    - Detector Unit
    - Image Data Processing Unit
    - Management Controller Unit
    - Thermal Control Unit

6.2.3 Verification Stages

The planning explains that the verification process shall be implemented in subsequent verification stages all along the program life cycle. The verification stages will be:

- Qualification (Q)
- Acceptance (A)

6.2.3.1 Qualification

In this stage the verification objective demonstrates that, at all levels, the design meets all applicable requirements and includes proper margins as determined by the design for qualification.

6.2.3.2 Acceptance

This stage of verification is applicable at all levels that demonstrate that the IES design is free of workmanship defects and integration errors and is ready for subsequent operational use.

6.3 Model Philosophy

The model philosophy will support the following objectives [39]:

- Verification of full compliance of the deliverable subsystem.
- Availability of development models to support verification of compliance with operational requirements and compatibility requirements.
- Early verification of critical and new design solutions and selected technologies.
- Reduction of risk.
- Minimize the number of models to accomplish schedule and cost constrains.

Different model philosophy approach will be defined for the verification levels: units and parts.

6.3.1 Units and Subsystems Model Philosophy

Depending on whether the subsystems and units are recurring items or not, different model philosophies will be applied for them that define the verification approach as a function of the individual units and the subsystem TRL. The approach is to perform:

- a full qualification test campaign and consequently a qualification approach on the new items.
- a reduced acceptance test campaign on the recurring items.

Table 6-1 provides an indication of the tests that will be performed at Unit, Subsystem and System level.

Table 6-1: Test per Units and Sub-system.

Tests		**Unit**	**Subsystem**
Functional tests	Power	Y	**Y**
	TMTC	Y	**Y**
Performance tests	Focal plane flatness/ alignment measurement	N	**Y**
	Spectral bands pattern and spectral calibration measurement	N	**Y**
	Spectral response uniformity	Y	**Y**
	Tests in darkness	Y	**N**
	Swath-width (Panchromatic, Multispectral)	N	**Y**
	Signal-to-Noise Ratio (SNR) measurement	N	**Y**
Mechanical tests	Physical properties (mass, centre of gravity,)	Y	**Y**
	Static tests	N	**Y**
	Dynamic tests:	N	**N**
	- - Frequency search	N	**Y**
	- - Sine	N	**Y**
	- - Random	N	**Y**
Thermal tests	Thermal cycling	N	**Y**
	Performance under thermal vacuum environment	N	**Y**
EMC test	**EMI/ EMC test**	**N**	**Y**

6.3.2 Development Plan

A three-model approach shall be followed. An Engineering Model (EM), a Qualification Model (QM) and a Flight Model (FM) shall be manufactured [40]. All units will be subjected to a complete verification campaign. The QM will be subjected to additional qualification testing.

The AIT Plan provides for EM, QM and FM models of the Camera Assembly.
Table 6-2 identifies the major differences in the AIT process between the models.

Table 6-2: Activities for EM, QM and FM.

Activity	EM	QM	FM
Baseline Procedures	N	Y	Y
Engineering Evaluation	Y	N	N
TID Testing	Y	N	N
SEE Testing	Y	N	N
EMI Screening	Y	Y	N
Extended Testing	N	Y	N
Functional Testing	Y	Y	Y
Acceptance Testing	N	N	Y

6.3.2.1 Electronic Engineering Verification

Engineering Models (EM) will be manufactured for the FPA and PEA, which will be used to perform additional engineering verification as shown in Table 6-3.

6.3.2.2 EMC, EMI and ESD Verification

Electromagnetic Radiation Compliance verification will be performed on EM, QM, as shown in Table 6-4.

6.3.2.3 Radiation Exposure Verification

Radiation exposure testing will be performed as indicated in Table 6-5.

6.3.2.4 Mechanical/ Structural Testing

Table 6-6 presents the mechanical testing to be performed for the IES.

Table 6-3: Electronic Engineering Verification.

Verifica-ation / Item	Power	Functional	Operational Test	Radiometric Tests	EMC	Thermal Cycling	Thermal Functional	Radiation	Interface compatibility
FPA-MS	N	N	N	N	N	N	N	N	Y
DTU	N	Y	Y	Y	Y	Y	Y	Y	Y
PEA	Y	Y	N	N	Y	Y	Y	N	Y
PEA-MS	N	N	N	N	N	N	N	N	Y
DPU	Y	Y	Y	Y	Y	Y	Y	Y	Y
MCU	Y	Y	Y	Y	Y	Y	Y	Y	Y
TCU	Y	Y	Y	Y	Y	Y	Y	Y	Y
Harness	Y	Y	Y	Y	Y	Y	Y	Y	Y

Table 6-4: EMI EMC and ESD Verification.

Verification / Item	Conducted Emissions (CE)	Radiated Emissions (RE)	Conducted Susceptibility (CS)	Radiated Susceptibility (RS)	Electrostatic Discharge (ESD)
DTU	Y	Y	Y	Y	Y
PEA-MS	N	Y	N	Y	N
DPU	Y	Y	Y	Y	Y
MCU	Y	Y	Y	Y	Y
TCU	Y	Y	Y	Y	Y
Harness	Y	Y	Y	Y	Y

Table 6-5: Radiation Exposure Verification.

Verification / Item	Total Ionization Dose (TID)	Single Event Effect (SEE): Proton	Single Event Effect (SEE): Heavy Ion (Direct Ionization)
DTU	Y	Y	Y
PEA Mech Housing	Y	Y	Y
DPU	Y	Y	Y
MCU	Y	Y	Y
TCU	Y	Y	Y
Harness	Y	Y	Y

Table 6-6: Mechanical/ Structural Testing.

Verification / Item	Physical properties	Modal Survey	Static Load	Transient	Random	Shock
FPA	Y	N	Y	N	N	N
DTU	Y	N	N	N	N	N
PEA	Y	Y	Y	Y	Y	Y
PEA-MS	Y	N	Y	N	N	N
DPU	Y	N	N	N	N	N
MCU	Y	N	N	N	N	N
TCU	Y	N	N	N	N	N
Harness	Y	N	N	N	N	N

6.4 Assembly, Integration and Test Flow

The AIT of the IES is planned to follow a logical progression of assembly and integration as shown in the following AIT flow diagram (Figure 6-2) that gives high level overview of the AIT process for each assembly and units.

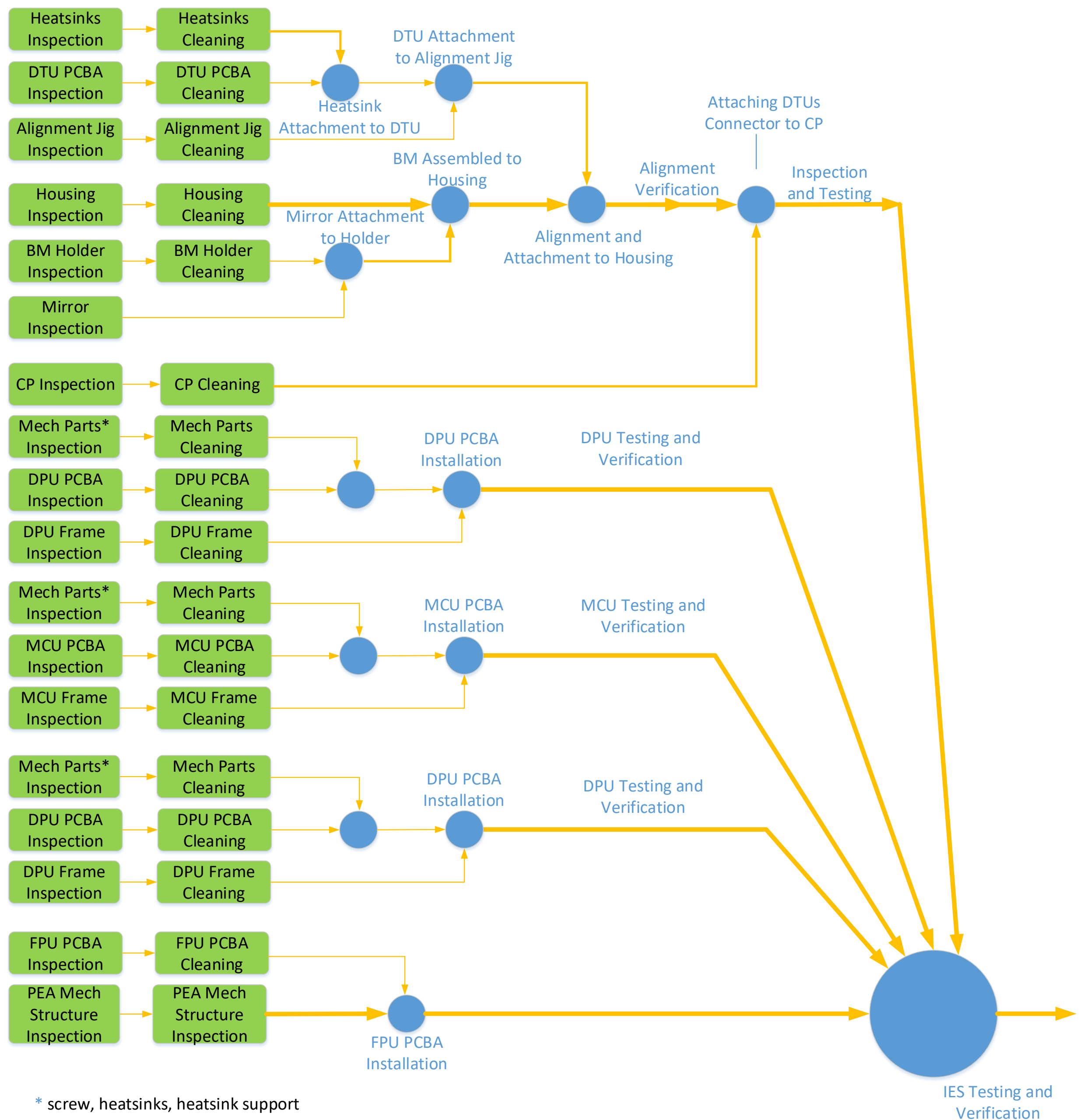

Figure 6-2: Assembly and Integration flow for the Assemblies and Units of the IES.

6.5 Electrical Ground Support Equipment

The Electrical Ground Support Equipment (EGSE) is needed to perform the preliminary tests (Functional Tests) on the Engineering Model (EM) and, to perform Final tests (performance Tests) on the QM/FM Model. The aim of the EGSE is to support testing and operations. A block diagram of the needed EGSE is illustrated in Figure 6-3.

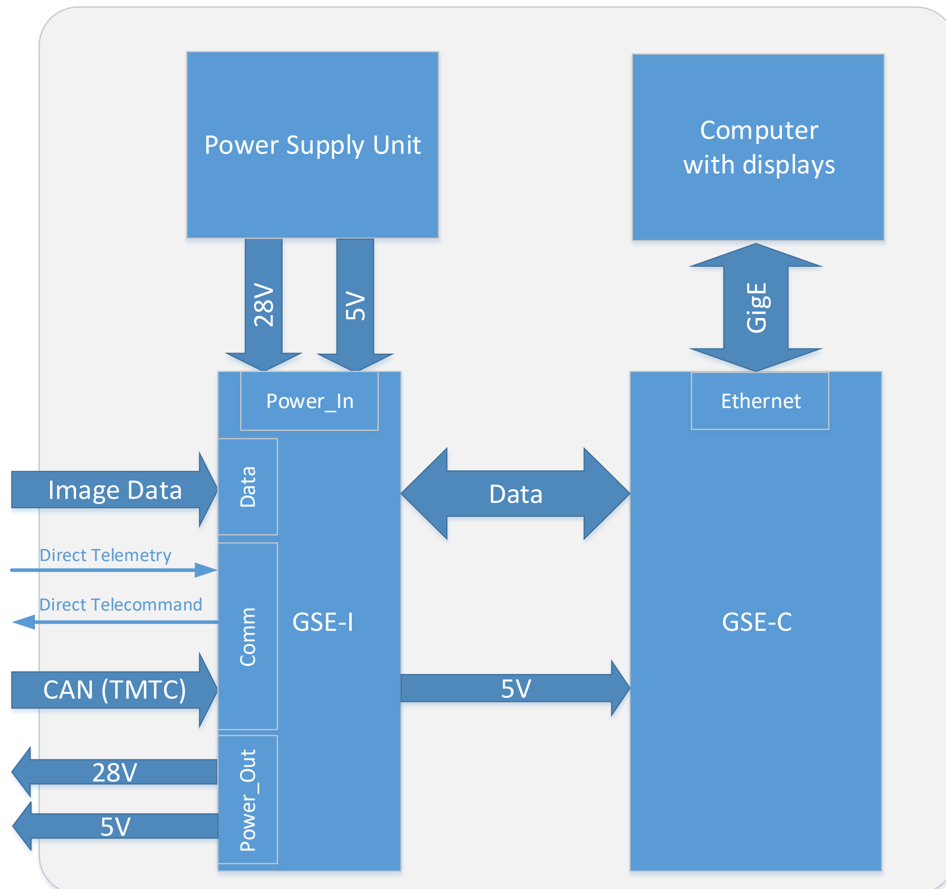

Figure 6-3: Block diagram of the EGSE for IES testing.

The EGSE is responsible for translating commands, telemetry and image data between a PC and the IES. The EGSE can interface directly with either a single or multiple DPUs or to a MCU or TCU. This is achieved by translating user commands from a PC to either the SPI interface to interface directly with a DPU or with the CAN protocol to interface with the MCU or TCU. The EGSE connects through GigE to a PC, making it possible to interface with any PC with the applicable port.

The EGSE hardware consists of a GSE controller (GSE-C) and a GSE Interface PCB (GSE-I), stacked through a high-density high-speed LVDS matched connector. The EGSE software includes the GSE-C low-level firmware on the GSE-C and the EGSE Software (EGSE-SW), on a computer.

The GSE-C utilizes various communication protocols, i.e. CAN controller, SPI controller, LVDS drivers, GigE PHY and general I/Os. The GSE can capture high-speed LVDS image data and transmit it via the GigE interface to the Computer. The firmware does all relevant translation between the commands and telemetry requests received on the GigE interface to the SPI or CAN interfaces.

The GSE-I acts as an interface PCB between either the Controller Unit or MCU and GSE-C. The GSE-I has the SPI PHY of the GSE-C connected to the debug connectors and the front plane connector of the DPU. To interface with the MCU and TCU, the GSE-I has CAN PHY's implemented between the GSE Controllers CAN driver pins and the MCU interface connector, and the TCU interface connectors.

The interface between the GSE-C and GSE-I is a high-density high-speed LVDS matched connector. The GSE-I has power switches to switch 28V to the MCU and TCU and to switch 5V to the DPUs, independently. Image data can be displayed, with a slight delay, on a display. The setup of the system (i.e. number of sensors, number of lines, frames per second) will determine the data rate of the system.

6.6 Facilities

AIT facilities breakdown for all the models is identified in Table 6-7.

6.7 Documentation

The documentation involved in the AIV process of the IES is presented in Figure 6-4, with a scheme showing the relationship between the different activities and the relevant documents.

Table 6-7: AIT facilities.

Test/ Activity	Facilities
- **Soldering of boards** - **Alignment of Detectors** - **Assembling of Units** - **Assembly and Integration of FPA, and PEA** - **Integrated Function Tests**	Manufacturer's (Onsite) Cleanroom facility (with laminar flow setup)
- **Radiation** - **Mass Properties** - **Vibration and shock testing** - **Thermal Balance/Thermal Vacuum,** - **EMC/EMI**	3rd party specific environmental test facility

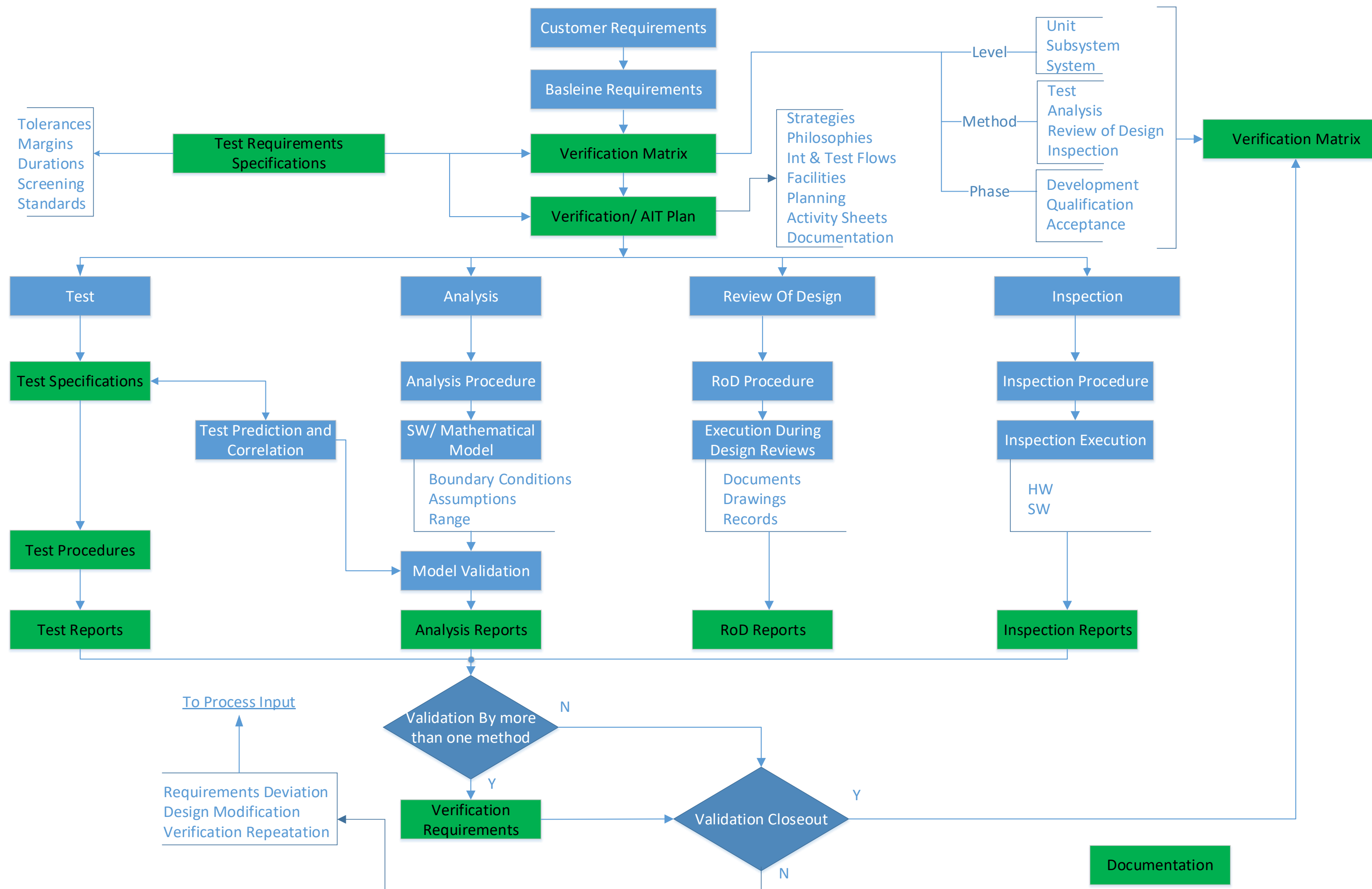

Figure 6-4: Relationship between AIT activities and documentation [39].

7 CONCLUSION

7.1 Summary

This dissertation has presented the evolution of the design of the Imager Electronics Subsystem of an Electro-Optical payload of an Earth-Observation satellite. Starting with the understanding of the mission objective and stakeholders' requirements, and then going through the systems engineering process, a functional and requirements analysis was performed. Based on the baseline requirements different alternates were sought through the brainstorming and a preferred alternate was selected by trade-off. This trade-off also included the support and concerns of the discipline engineers that perform the design work and provide required support (domain knowledge and competencies) to the systems engineers in the evaluation and selection of candidate alternates. The systems engineers also, in return, provide feedback to discipline engineers to improve knowledge and design guidelines.

The baseline is explained in detail, with the engineering budgets for complying with the defined requirements. The presented design has the heritage and qualified components that is to be developed and verified. During the verification, however, if it is required to replace a component then the part or component is selected from the preferred part list or the selected part/component has to undergo the screening and qualification campaign to prove its fitness for use. Also, any change in the interfaces outside the subsystem will require the update in the interfaces and might require change(s) in the IES design and is dealt through systems engineering approach.

In the end, the AIV planning is presented. That starts with the design process to ensure at each stage that all the design alternates and the baseline design is realizable and verifiable for the requirements compliance. This completes the scoped design of the IES for this dissertation.

7.2 Future Work

The design that is to be taken up in the future for development and verification, may require some changes in the design (or interface changes) as the design progresses with the inputs of different teams/ discipline engineers working on different parts of the design (detailed design and

analysis including electronics PCB/ hardware, mechanical, thermal and software/firmware will be performed as future work.).

In the dissertation design margins and interfaces are defined to guide the designers for the preliminary design work. However, these interfaces and design parameters would be reviewed again and revised during the detailed design phase. These needs to be addressed by communication with the stakeholders and other system engineers, and the scenarios would be thought through by analysing the risks and implications on the overall system performance leading to accepting, accepting with trade-off or rejecting the changes with the agreement of all parties.

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APPENDICES

Appendix A - Calculation for Overlap Pixels

Equatorial radius of the Earth (Re) = 6.38×10^{6} *m*

Gravitational Constant of the Earth (u) = 3.99×10^{14} $m^3 s^{-2}$

Orbit-geometry parameters

Altitude = h *m*

Semi-major axis = a = Re +h *m*

Mean motion = V_{rps} = $\sqrt{u/a^3}$ *rad/s*

Period (P) = $2\pi/V_{rps}$ *s*

Satellite speed = V = $(2\pi a)/V_{rps}$ *m/s*

Satellite ground speed = V_g = [Re/(Re+h)]V *m/s*

Imager-geometry parameters

Effective Focal Length = f *mm*

Pixel pitch = ρ *μm*

Ground Sampling Distance =GSD = [(h*ρ)/f] *m*

Separation between detectors (or bands on detectors)

Max yaw error (from AOCS system spec) =Φ *deg*

Separation between detectors (or bands) = dy *μm*

Separation between detectors (or bands) = (dy /ρ) *pixels*

Allowable displacement error due to yaw error = ε = [dy*tan(Φ)] *pixels*

Drift Calculations

Flight distance = Dy = [(dy*h)/f] *m*

Flight time = t = Dy/V_g *s*

Max drift (roll, from AOCS system spec) = ψ *rad/s*

= ψ_p = (ψ*h*t)/GSD *pixels*

Pixels overlap requirement

Pixels required for image processing = x *pixels*

Total pixels overlap = n_o = $(\varepsilon + \psi_p + x)$ *pixels*

Note: *Italics* indicate units.

Appendix B – Estimation for Required Number of Detectors After Overlap

Swath width		= SW *m*
Require number of pixels	$=N_p$	= (SW/GSD) *pixels*
Number of pixels per detector		= n_d *pixels*
Number of detectors required after overlap		$\geq [(N_p - n_o)/(n_d - n_o)]$ *detectors*

Note:

- The number of detectors is a discrete (whole) number next to the number that comes from the calculation, therefore the ≥ symbol is used.
- *Italics* indicate the units.

Appendix C – IES Technical Requirements

Req. ID	Req. Title	Requirement Statement
1.1	Identification of External Interfaces	
IES-TR-001-000	External Interfaces	The IES shall have mechanical interfaces, that will support it in following environments
IES-TR-001-001		Mounting Interface
IES-TR-001-002		Electrical Power Interface
IES-TR-001-003		Data Interface
IES-TR-001-004		Telemetry and Telecommand Interface
IES-TR-001-005		Test Interface
IES-TR-001-006		Imaging Interface
IES-TR-001-007		Radiated Thermal Interface
IES-TR-001-008		Solar Radiation Interface
IES-TR-001-009		Lifting Interface
IES-TR-001-010		Resting Interface
IES-TR-001-011		Transportation Interface
IES-TR-001-012		Conducted Thermal Interface
1.2	Identification of States and Modes	
IES-TR-002-000	IES Operation	The IES shall be in a clearly defined state/mode throughout the Mission life.

Req. ID	Req. Title	Requirement Statement
IES-TR-003-000	Mutual Exclusivity of Modes	All the operational modes of the IES shall be mutually exclusive.
IES-TR-048-000	Default Mode	The IES, when transitioning from OFF State to ON State, shall automatically enter Configuration Mode.
IES-TR-004-000	IES States	The IES shall have the following states:
IES-TR-004-001		ON state
IES-TR-004-002		OFF state
IES-TR-005-000	IES Modes	The IES shall have at least following operating modes:
IES-TR-005-001		Configuration Mode
IES-TR-005-002		Imaging Mode
IES-TR-005-003		Playback
IES-TR-005-004		Error Mode
IES-TR-005-005		Focusing Mode
1.3 Functional and Performance Requirements		
1.3.1 Collect Light 1.3.1.1 Imaging		
IES-TR-006-000	Spectral bands	The IES shall be able to produce image data for each spectral band defined in IES-TR-005-000 (Spectral Band Characteristics).
IES-TR-007-000	Spectral Band Characteristics	The IES shall measure the quantity of electromagnetic radiation that is incident upon the Imaging Interface in each of the defined spectral bands.

Req. ID	Req. Title	Requirement Statement
IES-TR-007-001	Panchromatic	450 to 800
IES-TR-007-002	Blue	440 to 510
IES-TR-007-003	Green	510 to 580
IES-TR-007-004	Red	630 to 690
IES-TR-007-005	NIR	770 to 900
IES-TR-008-000	Out Of Spectral Bands	The IES shall limit the collection of electro-magnetic radiation outside of the spectral bands specified herein to a mean value less than 2% of the maximum collection value.
IES-TR-009-000	Edge of spectral bands	The edges of the IES spectral bands specified herein shall transition from 10% of the maximum collection value to 90% of the maximum collection value within 10nm .
IES-TR-010-000	Panchromatic MTF	The IES level MTF for the panchromatic band shall be greater than 0.45 at the Nyquist Frequency .
IES-TR-011-000	Multispectral MTF	The IES level MTF for the multispectral bands shall be greater than 0.5 at the Nyquist Frequency .
IES-TR-012-000	Length of Light measurement Area	The area of Imaging Interface of the IES shall have the length of the electromagnetic radiation measurement in the Y axis of at least 170mm for all spectral bands.
IES-TR-011-000	Alignment of Elements	IES shall provide alignment and support to the optical elements without degrading its performance

Req. ID	Req. Title	Requirement Statement
1.3.2 Convert Light into Image data 1.3.2.1 Imaging Mode		
IES-TR-014-000	Start Imaging	The IES, in Imaging mode, upon receipt of a "Start Imaging" command via the Telemetry and Telecommand Interface, shall begin capturing image data in less than 100 milliseconds.
IES-TR-015-000	Stop Imaging	The IES, when in Imaging Mode, upon receipt of a "Stop Imaging" command via the Telemetry and Telecommand Interface, shall complete capturing and transmitting the current image line before exiting Imaging Mode and directly entering Configuration Mode.
IES-TR-016-000	Abort Imaging	The IES, when in Imaging Mode, upon receipt of an "Abort Imaging" command via the Telemetry and Telecommand Interface, shall abort capturing and transmitting the current image line, exit Imaging Mode and directly enter Configuration Mode.
IES-TR-017-000	Update Auxiliary Data	The IES, in Imaging mode, shall allow the Auxiliary telemetry and Time to be updated.
1.3.2.2 Imaging		
IES-TR-018-000	Selection of bands	The IES shall allow the selection of Panchromatic, Multispectral or Combined (Panchromatic and Multispectral) imaging.
IES-TR-019-000	Range of Imaging Lines	IES shall be able to acquire image scenes with length corresponding to any number of Image lines between One (1) and Five Million (5,000,000).
IES-TR-020-000	Operational Time	IES shall be able to support operational time of 8 min per orbit over the complete design life.
IES-TR-021-000	Pixel bit depth	The panchromatic and multispectral shall be quantized with bit depth of 12 bits.
IES-TR-022-000	Image data transmit Transmit	The IES shall transmit the image data with the first pixel captured transmitted first.

Req. ID	Req. Title	Requirement Statement
IES-TR-023-000	Minimum Time between imaging	The IES in imaging mode, shall be able to acquire new image after 90 minutes of previous image acquisition end.
IES-TR-024-000	Synchronization Signal	The IES shall be able to receive PPS synchronization signal from bus to synchronize payload time.
IES-TR-025-000	Time Synchronization	The error between payload time in image data and synchronized satellite time shall be less than 5 msec (TBC).
IES-TR-026-000	Time tagging	IES shall time tag each imaging line.
IES-TR-027-000	Imaging Preparation Time	The payload, when transitioned to imaging mode, shall take less than 5 seconds to prepare for imaging.
1.3.2.3 Imaging Performance		
IES-TR-029-000	Panchromatic spatial resolution	For IES, electromagnetic radiation in the Panchromatic band shall be measured with a distance between measurements less than or equal to 7 µm.
IES-TR-030-000	Multispectral spatial resolution	For IES, electromagnetic radiation in the Multispectral bands shall be measured with a distance between measurements equal to 4 times the Panchromatic band measurement distance.
CS-TR-031-000	Panchromatic SNR	The IES shall have SNR in Panchromatic band better than or equal to 100 at 62 W.m-2. sr-1.µm-1
CS-TR-032-000	Multispectral SNR	TheIES shall have SNR in Multispectral bands better than or equal to 100 at 48 W.m-2. sr-1.µm-1
IES-TR-034-000	Image scan rate	The IES shall operate with a projected point on image plane moving at a rate of 63 mm/s +/- in the X direction.

Req. ID	Req. Title	Requirement Statement
IES-TR-036-000	Radiometric Resolution	The IES shall have a radiometric resolution with NEΔL < 3.5W.m-2. sr-1.µm-1 in the Panchromatic band
1.3.2.4 Simultaneous Acquisition		
IES-TR-037-000	Simultaneous Acquisition	For simultaneous acquisition the configuration for panchromatic channel will be used for all channels Note: There will be a provision of different TDI stages for bands.
1.3.2.5 Transmit Image Data		
IES-TR-038-000	Data Transmission	The IES, when in Imaging Mode, shall begin transmitting the image data on the Data Interface within 1 second from the start of capturing image data.
IES-TR-039-000	Image Data Frame	The image data frame of IES shall consist of the following:
IES-TR-039-001		Start Sync marker
IES-TR-039-002		Image data
IES-TR-039-003		Auxiliary data
IES-TR-039-004		CRC (for Auxiliary data only)
IES-TR-040-000	Auxiliary Data	The Auxiliary data shall contain at least following parameters:
IES-TR-040-001		Header (including Image ID)
IES-TR-040-002		Configuration Parameters (Band TDI Stage, Band and Sensor ID)
IES-TR-040-004		UTC Time

Req. ID	Req. Title	Requirement Statement
IES-TR-041-000	End of Data Transmission	The IES shall cease transmitting when all the requested image data has been transmitted.
1.3.3 Set Configuration 1.3.3.1 Configuration Mode		
IES-TR-042-000	Configuration Parameters	The IES, in Configuration Mode, shall allow configuration of the internal parameters through Telemetry and Telecommand interface.
IES-TR-043-000	Enter Imaging Mode	The IES when in Configuration Mode, upon receipt of a "Set Camera Mode to Imaging" command via the Telemetry and Telecommand Interface, shall exit Configuration Mode and directly enter Imaging Mode.
1.3.4 Health Monitoring		
IES-TR-044-000	Health Monitoring Telemetry	The IES shall provide health monitoring telemetry
IES-TR-045-000	Health Telemetry Parameters	The health monitoring telemetry shall include but not limited to the following parameters:
IES-TR-045-001	Currents	Currents
IES-TR-045-002	Voltages	Voltages
IES-TR-045-003	Temperatures	Temperatures
IES-TR-046-000	Request Error Telemetry	The IES, in Error Mode, shall allow the requesting of health monitoring telemetry only.
IES-TR-046-000	Error Mode Configuration	The IES imaging sensors shall be unpowered in Error Mode.

Req. ID	Req. Title	Requirement Statement
1.3.5 Relationships between states 1.3.5.1 State to State Relationship		
IES-TR-047-000	Start-up time	The IES, when in OFF State, upon application of power on the Electrical Power Interface, shall transition to ON State in less than 5 seconds.
IES-TR-047-000	Shutdown time	The IES, when in ON State, upon removal of power on the Electrical Power Interface, shall transition to OFF State in less than 1 second.
1.3.6 Mounting Interface		
IES-TR-049-001	PEA natural frequency (Longitudnal)	The PEA shall have a lowest natural frequency greater than 75Hz (TBC) when mounted at the PEA Mounting Interface.
IES-TR-049-002	PEA natural frequency (Longitudnal)	The FPA shall have a lowest natural frequency that is greater than 30 (TBC) Hz in lateral direction when mounted at the FPA Mounting Interface.
IES-TR-050-001	FPA natural frequency (Longitudnal)	The FPA shall have a lowest natural frequency that is greater than 75 Hz in longitudinal direction when mounted at the FPA Mounting Interface.
IES-TR-050-002	FPA natural frequency (Lateral)	The FPA shall have a lowest natural frequency that is greater than 30 Hz in lateral direction when mounted at the FPA Mounting Interface.
IES-TR-051-000	FPA Thermal Conductance	The thermal conductance through the FPA Mounting Interface shall be able to maintin the temperature of FPA within Operating Temperature range.
IES-TR-052-000	PEA Thermal Conductance	The thermal conductance of the PEA Mounting Interface would be a value that shall keep the unit within operational temperature range.

Req. ID	Req. Title	Requirement Statement
IES-TR-053-000	PEA Mounting Interface	The PEA Mounting Interface shall provide a mounting surface to the Satellite able to support the mass of the unit in all the applicable environments.
IES-TR-054-000	FPA Mounting Interface	The FPA Mounting Interface shall provide a mounting surface to the Telescope able to support the mass of the Focal Plane Unit in all the applicable environments.
IES-TR-055-000	FPA Interface Flatness	The FPA Mounting Interface shall have a flatness of 0,1um over 100um
IES-TR-056-000	FPA Low Impedance Interface	The FPA shall provide an electrical conductance path to the Satellite Mount with DC impedance of smaller or equal than 30mΩ
IES-TR-057-000	PEA Low Impedance Interface	The PEA shall provide an electrical conductance path to the Satellite Mount with DC impedance of smaller or equal than 30mΩ
1.3.7 Electrical		
IES-TR-058-000	EMC/EMI interference	The IES configuration and electrical interfaces shall be EMC/EMI shall be compliant to the following MIL Std-461G tests.
IES-TR-058-001	CE102	CE102: Conducted emissions, radio frequency potential, power leads.
IES-TR-058-002	CS101	CS101: Conducted susceptibility, power leads
IES-TR-058-003	CS114	CS114: Conducted susceptibility, bulk cable injection.
IES-TR-058-004	CS115	CS115: Conducted susceptibility, bulk cable injection, impulse excitation
IES-TR-058-005	CS116	CS116: Conducted susceptibility, damped sinusoidal transients, cables and power leads
IES-TR-058-006	RE102	RE102: Radiated emissions, electric field
IES-TR-058-007	RS103	RS103: Radiated susceptibility, electric field

Req. ID	Req. Title	Requirement Statement
1.3.7.1 Electrical Power Interface		
IES-TR-059-000	Electrical Power	The IES shall consume at most 200W of electrical power.
IES-TR-060-000	Electrical Power Signals	The Electrical Power Interface shall pass the following signals from the Satellite to the IES:
IES-TR-060-001	Power Signal	a. Power Supply
IES-TR-060-002	Ground Signal	b. Power Return
IES-TR-061-000	Electrical supply voltage	The nominal electrical supply voltage for the IES shall be 28V ±4V.
IES-TR-062-000	Power Connector	The Electrical Power Interface shall use a DSUB8W8 Male type connector.
IES-TR-063-000	Redundant Power Interface	The IES shall provide a main and redundant Electrical Power Interface with the same configuration.
IES-TR-064-000	Bonding Stud	The IES shall provide a Bonding Stud of type M5 bolt for the PEA MS to be attached to the satellite structure with an impedance of less than 2.5 mΩ.
IES-TR-065-000	Galvanic isolation	The IES power supply shall provide galvanic isolation between the external primary power supply and the internal secondary power supply.
IES-TR-066-000	Secondary Ground	The IES secondary ground shall be connected to thePEA MS with a DC resistance less than 2.5 mΩ.
IES-TR-067-000	Local ground isolation	Any additional remote secondary grounds shall be isolated from the PEA housing each with a minimum 1MΩ at DC in parallel with a capacitance < 50nF
IES-TR-068-000	Support Satellite Power Harness	The Electrical Power Interface shall provide a mounting point for the Satellite harness to support the mass of the harness in all the applicable environments

Req. ID	Req. Title	Requirement Statement
1.3.7.2 Data Interface		
IES-TR-069-000	Data Interface	The IES shall use a high-speed serial data interface.
IES-TR-070-000	Data Connector	The IES Data Interface shall use the SMA type connector.
IES-TR-071-000	Support Satellite Data Harness	The Data Interface shall provide a mounting point for the Satellite data harness to support the mass of the harness in all the applicable environments.
IES-TR-072-000	Output Data Rate	For each data link, the IES shall provide a main and a redundant Payload Data Interface with the same configuration.
1.3.7.3 Telemetry and Telecommand Interface		
IES-TR-073-000	TMTC Signals	The Telemetry and Telecommand Interface shall pass the following signals from the IES to the Satellite:
IES-TR-073-001	Can High	a. Nominal CAN High
IES-TR-073-002	Can Low	b. Nominal CAN Low
IES-TR-073-003	Redundant Can High	c. Redundant CAN High
IES-TR-073-004	Redundant Can Low	d. Redundant CAN Low
IES-TR-074-000	TMTC Physical Layer	The Telecommand and Telemetry Interface OSI physical layer shall be CAN bus compliant to the ISO-11898-2:2003 standard.
IES-TR-075-000	TMTC Datalink Layer	The Telecommand and Telemetry Interface OSI datalink layer shall be CAN bus compliant to the ISO-11898-1:2003 standard.
IES-TR-076-000	TMTC Higher OSI Layers	The Telecommand and Telemetry Interface OSI application layer shall be compliant to "Space-Ground Interface Control Document".

Req. ID	Req. Title	Requirement Statement
IES-TR-077-000	TMTC Connector	The Telemetry and Telecommand Interface shall use a DB-15 Female type connector.
IES-TR-078-000	Redundant TMTC Interface	The IES shall provide a main and redundant Telemetry and Telecommand Interface with the same configuration.
IES-TR-079-000	Support Satellite TMTC Harness	The Telemetry and Telecommand Interface shall provide a mounting point for the Satellite TMTC harness to support the mass of the harness in all the applicable environments.
1.4 Environmental Requirements		
1.4.1 Classes of Environment		
IES-TR-081-000	Classes of environment	The IES shall meet environmental requirements for the following classes of environment:
IES-TR-081-001	Payload Integration Environment	a. Payload Integration Environment
IES-TR-081-002	Payload Test Environment	b. Payload Test Environment
IES-TR-081-003	Payload Transportation Environment	c. Payload Transportation Environment
IES-TR-081-004	Satellite Integration Environment	d. Satellite Integration Environment
IES-TR-081-005	Satellite Test Environment	e. Satellite Test Environment
IES-TR-081-006	Satellite Transportation Environment	f. Satellite Transportation Environment
IES-TR-081-007	Pre-launch Storage Environment	g. Pre-launch Storage Environment
IES-TR-081-008	Launch Vehicle Integration	h. Launch Vehicle Integration Environment

Req. ID	Req. Title	Requirement Statement
	Environment	
IES-TR-081-009	Launch Environment	i. Launch Environment
IES-TR-081-010	Orbit Survival Environment	j. Orbit Survival Environment
IES-TR-081-011	Orbit Operational Environment	k. Orbit Operational Environment
IES-TR-081-012	Disposal Environment	l. Disposal Environment
1.5 Physical Requirements		
IES-TR-094-000	IES Mass	The IES mass shall not exceed 11.0kg.
IES-TR-095-000	PEA Mass	The PEA mass shall not exceed 6.0kg.
IES-TR-097-000	FPA Mass	The Focal Plane Unit mass shall not exceed 3.0kg.
IES-TR-098-000	CHR Mass	The IES Harness mass shall not exceed 2kg.
IES-TR-099-000	PEA Size	The PEA dimensions shall not exceed 300mmx300mmx400mm
IES-TR-100-000	FPA Size	The FPA dimensions shall not exceed 170mmx220mmx320mm
IES-TR-101-000	CHR Mass	The IES Harness length shall not exceed 1.5m±0.1m.
1.6 Design Requirements		
IES-TR-102-000	Design Life	The IES shall have a Design Life of 7 years comprising 5 years in mission orbit and 2 years in ground storage.
IES-TR-103-000	Prevent Orbital Debris	The IES shall be designed to remain physically intact and prevent the creation of orbital debris in the Disposal Environment, particularly the interfaces defined for this environment in IES-TR-204-000.

Req. ID	Req. Title	Requirement Statement
IES-TR-104-000	Single point failure free	The IES shall be single point failure free, as any single part or unit failure which could cause payload mission failure except where technologically unavoidable.
IES-TR-105-000	Survivability	The IES shall be capable to withstand the Orbit Survival Environment in the OFF state without permanent damage or permanent degradation in its performance.
IES-TR-035-001	Reliability	The IES shall be designed to ensure a reliability value better than 0.9 at end of life.
IES-TR-106-000	Single Event Effects (SEE)	The IES shall withstand or mitigate Single Event Effects (SEE), without sustaining permanent damage or without interrupting image data output for maximum of 4 seconds.
IES-TR-107-000	Single Event Latch-ups (SEL)	IES shall mitigate any Single Event Latch-ups (SEL) that occur in Integrated Circuits (ICs).
1.7 Other Requirements		
CS-TR-108-000	EEE Part Derating	All electromechanical and optical parts in the IES shall be de-rated in accordance with space industry standards specification.
CS-TR-109-000	Prohibited EEE parts	The following EEE parts are prohibited for use in the IES:
CS-TR-109-001	Pure tin plating part	a. Components using pure tin plating
CS-TR-109-002	Hollow core resistors	b. Hollow core resistors
CS-TR-109-003	Potentiometers	c. Potentiometers
CS-TR-109-004	Wet slug tantalum capacitors	d. Wet slug tantalum capacitors (except CLR79, 81, 83, 90, 91 types with double seals and tantalum case)
CS-TR-109-005	Wire-link fuses	e. Wire-link fuses (for new designs)
CS-TR-110-000	Prohibited Materials	The following materials are prohibited for use in the IES:
CS-TR-110-001	Pure tin plating material	a. Pure tin plating

Req. ID	Req. Title	Requirement Statement
CS-TR-110-002	Cadmium	b. Cadmium
CS-TR-110-003	Zinc	c. Zinc
CS-TR-110-004	Mercury	d. Mercury and mercury containing compounds
CS-TR-110-005	Magnesium	e. Magnesium, unless under controlled conditions and environment according to ECSS-Q70-71A.
CS-TR-110-006	Polyvinyl chloride	f. Polyvinyl chloride
CS-TR-110-007	Brass	g. Brass used in vacuum environment above 121 °C, unless plated with an approved material.
CS-TR-110-008	Dissimilar metals	h. Dissimilar metals in contact if the E.M.F. is >0.5V
CS-TR-110-009	Organic materials	i. Organic materials of any type unless flight qualification is properly justified
CS-TR-110-010	Pure tin solder	j. Pure tin solder with tin purity >97%
CS-TR-111-000	Parts and Materials to be reviewed	The Plastic parts and materials shall be reviewed and approved for use in the IES.
CS-TR-112-000	Out-gassing	The IES shall comply with ASTM-E-595-84 material out- gassing requirements as follows:
CS-TR-112-001	TML	a. TML ≤ 1.0%
CS-TR-112-002	CVCM	b. CVCM ≤ 0.1%
CS-TR-112-003	24 hour vaccuming	c. 24 hours vacuum testing
CS-TR-113-000	Radiation Exchange	The IES radiation interface shall have the capability to operate in all environments as per its radiation exchange, that shall not degrade performance.