

# A Compact High-Energy Particle Detector for Low-Cost Deep Space Missions

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Masters Dissertation



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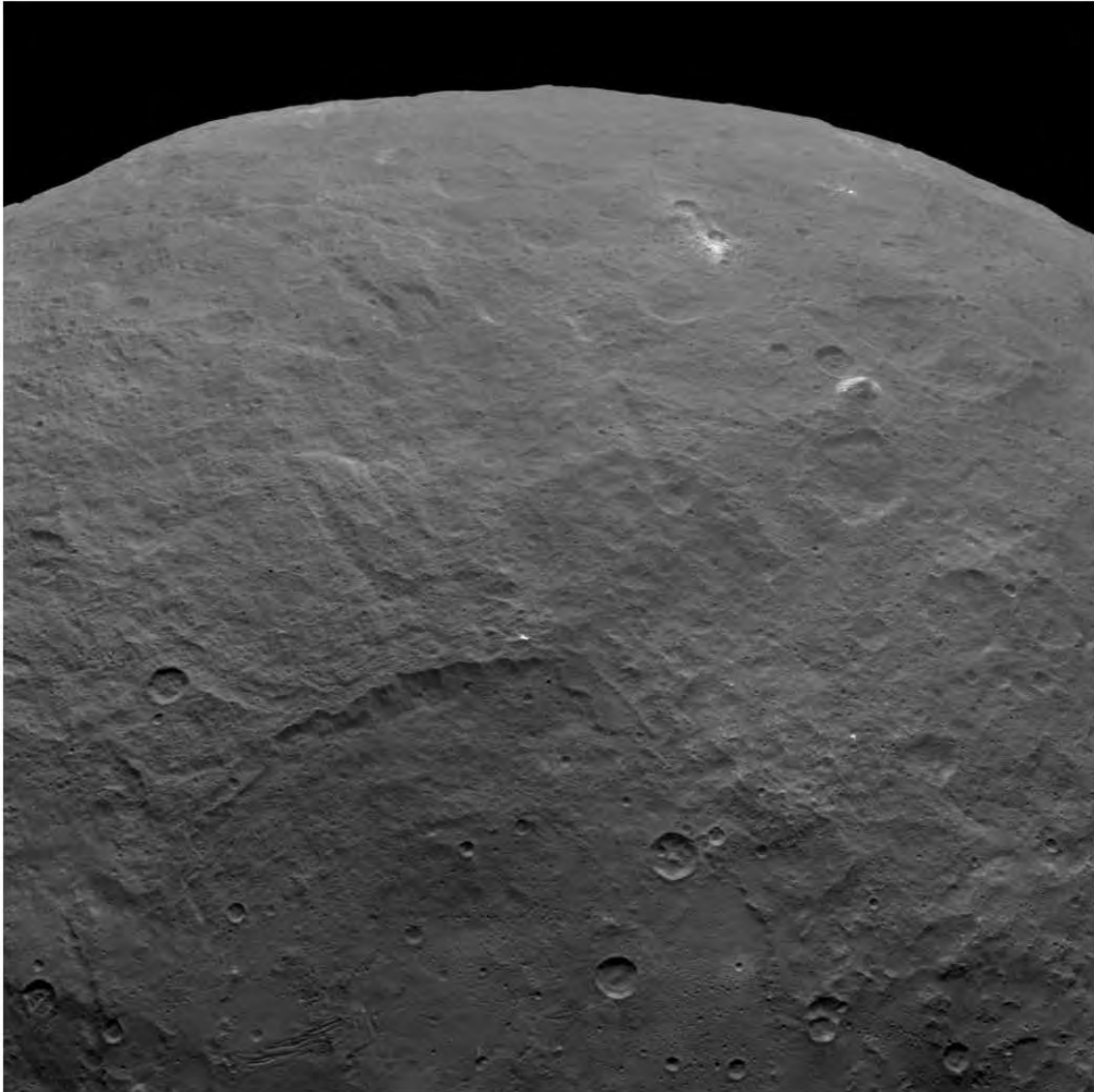


Image of a 3-mile-tall pyramid on Ceres, captured and processed by a Xilinx FPGA onboard the Dawn spacecraft[1].

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# Declaration

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# Abstract

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Over the last few decades particle physics has led to many new discoveries, laying the foundation for modern science. However, there are still many unanswered questions which the next generation of particle detectors could address, potentially expanding our knowledge and understanding of the Universe. Owing to recent technological advancements, electronic sensors are now able to acquire measurements previously unobtainable, creating opportunities for new deep-space high-energy particle missions. Consequently, a new compact instrument was developed capable of detecting gamma rays, neutrons and charged particles. This instrument combines the latest in FPGA System-on-Chip technology as the central processor and a 3x3 array of silicon photomultipliers coupled with an organic plastic scintillator as the detector. Using modern digital pulse shape discrimination and signal processing techniques, the scintillator and photomultiplier combination has been shown to accurately discriminate between the different particle types and provide information such as total energy and incident direction. The instrument demonstrated the ability to capture 30,000 particle events per second across 9 channels - around 15 times that of the U.S. based CLAS detector. Furthermore, the input signals are simultaneously sampled at a maximum rate of 5 GSPS across all channels with 14-bit resolution. Future developments will include FPGA-implemented digital signal processing as well as hardware design for small satellite based deep-space missions that can overcome radiation vulnerability.

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# Chapter 1

## Introduction

### 1.1 Background to the Study

Over the past few decades, particle physics has led to many ground-breaking discoveries, laying the foundation for modern science. However, despite these amazing achievements, little is known and truly understood about the Universe. For example, the most widely accepted theory regarding energy and matter suggests that atoms only account for around 4 % of the Universe with the rest being dark matter (24 %) and dark energy (71 %), yet dark matter and dark energy are both purely hypothetical.

It is clear that the Universe still holds many mysteries and the next generation of particle detectors are likely to assist us in gaining a better understanding of these. With the recent technological advancement in high-speed electronics and hypersensitive optical detectors there are many new scientific opportunities and possibilities arising that were previously unachievable.

Space agencies such as the National Aeronautics and Space Administration (NASA) have recently announced their intentions to send humans to asteroids and planets within our solar system by 2025-2030. Using particle detectors and dosimeters preceding these missions is critical in determining the environmental conditions that astronauts will be exposed to. Moreover, interplanetary endeavors will be, for the foreseeable future, limited to robotic missions and will require environmental analyzers to determine if distant celestial bodies may be inhabitable or not.

This study forms part of a collaboration with the University of Cape Town's Physics Department which also has an interest in the detector's development.

### 1.2 Objectives of this Study

#### 1.2.1 Problem to be Investigated

The problems to be investigated in this study are centered around the feasibility of a compact high energy particle detector for low-cost space missions. The primary objectives of this study are to develop a platform that:

- can support particle detection based on silicon photomultipliers and a plastic scintillator

- incorporates all the necessary processing capabilities for particle identification and discrimination
- is compact and robust such that it is able to fit inside a small spacecraft

Furthermore, the secondary objectives which apply to the long-term vision for the detector are as follows:

- demonstrate detection of neutrons, gamma-rays and charged particles and accurately discriminate between them
- operate with a low overall power consumption to remain within the limited power budget inherent to small satellites
- keep final costs low in terms of small satellite budgets

Only once these objectives have been met can the particle detectors technical readiness level (TRL) be increased to a point where it is ready for integration with a spacecraft. Given the inherently expensive nature of deep space missions, flight heritage will first need to be achieved in low-altitude, Earth orbiting missions to further prove the technology.

### 1.2.2 Purpose of the Study

Although neutron and gamma-ray detectors are not new, they are traditionally bulky and fragile due to their detection architecture. These traditional technologies also usually require high voltages ( $>1\text{kV}$ ) and final results are only obtained after post-processing. An example of this is a neutron detector which consists of a toxic liquid scintillator and a large, fragile vacuum-tube photomultiplier. Thus, there is a desire and need for a compact detector that is more power efficient and robust.

The short-term purpose of this study was to determine whether a compact high-energy particle detection platform can be developed that satisfies the primary objectives outlined above. If proven feasible, the device could be proposed as a space mission to further develop the technology into a space-ready detector. In addition to its application in space, however, this type of particle detector can also satisfy a large number of terrestrially-based applications, such as:

- detecting sources of radiation for border control, embassy security and cargo inspection
- personal radiation dosage monitoring
- characterization of the morphology of materials in the field of material science
- enhancing neutrino detectors in the field of particle physics
- monitoring nuclear reactor and particle accelerator performance

The long term vision is to have a constellation of these particle detectors characterizing the space environment in different parts of our Universe, starting with our own planet and extending out to our solar system and beyond. For the purposes of this study, NASA scientists and engineers were asked the following question:

*“Presume you had a particle detector that could detect gamma-rays, neutrons and charged particles and could provide information such as particle type, total energy deposited and incident direction. If you could place this detector in any orbit, anywhere in the Universe where would you place it, what would you measure and why?”*

Three of the responses received are summarized below, demonstrating the broad spectrum of applications the particle detector can satisfy:

*“Flying a particle detection mission spiraling outward from Earth through the heliopause into interstellar space would give a holistic view of heliospheric particles and high energy photons. Ideally you’d want to stagger observations so you could observe time dependence as a function of orbit radius throughout one or more solar cycles.*

*- Radiation Environment Control Engineer”*

*“Along biological lines, a small radiation detector could accompany a Cube-Sat plant growth experiment on Google X-flights to the Moon. The detector can assist in testing plant germination and initial growth under combined lunar gravity and lunar cosmic ray environment. Also, a radiation sensor on the surface of Mars at two locations: one in the area of strong crustal magnetism in the southern highlands and another in a northern location with no crustal magnetism. The detector could determine if the presence of the strong crustal magnetism has a significant effect on solar particle radiation.*

*- Planetary Scientist”*

*“A useful application for the detector would be in a nanosatellite placed around planetary systems to better understand the interaction of solar wind and background radiation with planetary atmospheres (e.g., Mars) or surfaces (e.g., moons of Mars, Moon, and outer planet moons).*

*- Space Scientist”*

### 1.3 Scope and Limitations

The scope of the project was to develop a compact platform capable of supporting particle detection, identification and discrimination that satisfied the primary objectives defined above. Furthermore, the key components the study was to identify are as follows:

- particle detection technology and appropriate power source
- data collection architecture
- signal conditioning and distribution techniques
- processing technology to support identification and discrimination

The detector was limited to:

- nine individual detection channels

- correct scale, in terms of physical size, for implementation on a small satellite.
- gamma/neutron detection up to energies of 6 MeV and 60 MeV respectively
- laboratory testing only
- part selection from commercial off the shelf (COTS) components

Although the long-term vision for the particle detector is application in space, this study does not require electrical design immediately compatible with the space environment. However, components were chosen with the long-term vision in mind, therefore making future developments simpler for spacecraft implementation. Finally, the study was to be completed over a 24 month period within a limited budget.

## 1.4 Plan of Development

This study is organized into six primary sections, namely Introduction, Literature Review, Research Methodology, Results, Conclusion and Recommendations.

The **Introduction** starts by providing background and context to the study. The primary objectives of the study are established and the long-term vision of the project is discussed. Furthermore, the scope and limitations of the project are defined.

The **Literature Review** explores the work done in the fields of particle detection, both terrestrial and space-based, preceding this study. Various particle detection and processing technologies are investigated to make an informed decision moving forward.

The subsequent chapters make up the **Research Methodology** which delves into the particle theory necessary to understand the detection, identification and discrimination mechanisms. Hardware is designed for various aspects of the particle detector based on the preceding research. Finally, software is developed to support the hardware and, ultimately, the detector platform.

The **Results** chapter presents the results obtained from testing the specific detector architecture, independent from the hardware developed. Thereafter, results are presented specific to the hardware developed in the research methodology.

Finally, the **Conclusions** addresses the progress made throughout the study and highlights what was achieved. In the **Recommendations** chapters, the implications of these achievements are discussed and recommendations are made for future work.

## Chapter 2

# Literature Review

### 2.1 The Space Environment

The space environment is unlike any experienced on Earth and introduces new hazards that must be understood and mitigated for any space mission - manned or unmanned. It is a common misconception that space is a void that lies beyond Earth's atmosphere, empty of any matter apart from the stars. On the contrary, space is filled with countless objects, varying in size and traveling at very high speeds.

There are many hazards in the space environment that may or may not affect a spacecraft, dependent on its mission and orbit type. NASA conducted a thorough study on these environmental effects, part of which was the comparison of the severity of effects, the results of this study can be seen in Table 2.1[2, 3]. A '0' corresponds to effects that are negligible to a mission and a '10' to effects that are so severe that it would negate the mission.

Many of the effects discussed in [2] are relevant to an entire spacecraft in Low-Earth Orbit (LEO). For the purposes of this study, only effects relevant to the particular payload for interplanetary missions will be considered. As an example, neutral gases primarily affect LEO spacecraft, and more specifically the overall spacecraft rather than the payloads within. For this reason, despite the 9-7 severity rating on the table, these effects will be ignored.

#### 2.1.1 Space Debris

Space debris refers to both naturally occurring micrometeoroids and man-made debris found in space. Micrometeoroids are solid particles (primarily ice with a small amount of higher density minerals) traveling towards or nearby Earth in interplanetary space. The particle sizes range from sub-micron to several meters in diameter with speeds of 3-72 km/s. Man-made debris consists of defunct spacecraft, launch vehicle upper stages, remnants from spacecraft collisions etc. This debris has been rapidly increasing since the start of human space endeavors - the launch of Sputnik 1 in October of 1957[2, 3].

In 2012 there were more than 21,000 debris objects with a radius greater than 10 cm orbiting Earth. Additionally, there are an estimated 500,000 objects between 1-10 cm in diameter and in excess of 100 million objects smaller than 1cm[4]. Space

Table 2.1: Table comparing magnitudes of space environmental severity[2]

Spacecraft Environment	LEO <sup>(1)</sup> Low Incl.	LEO High Incl.	MEO <sup>(2)</sup>	GEO <sup>(3)</sup>	Int'l Space Station 500 km 51.6° incl	EOS 500 km 28.5° incl	TRMM 600 km 28.5° incl	GPS 20,000km 55° incl	DSCS GEO Classified
Direct Sunlight	4 <sup>(4)</sup>	4	4	4	4	4	4	4	4
Gravity Field	3	3	3	0	3	3	3	0	0
Magnetic Field	3	3	3	0	3	3	3	0	0
Van Allen Belts	0-5	2-5	8-5	1	2-5	2-5	2-5	5	1
Solar flare Particles	0	4	3	5	4	0	0	3	5
Galactic Cosmic Rays	0	4	3	5	4	0	0	3	5
Debris Objects	7	7	3-0	3	7	7	7	0	3
Micrometeoroids	3	3	3	3	3	3	3	3	3
Ionosphere	3	3	1	0	3	3	3	0	0
Hot Plasma	0	3	0	5	0	0	0	3	5
Neutral Gases	9-7	9-7	3-0	0	9-7	9-7	9-7	0	0

(1) Low Earth orbit (LEO) extends up to 1000 km.

(2) Mid Earth orbit (MEO) is above 1000 km and extends up to 35,000 km.

(3) Geosynchronous orbit (GEO) is ~35,000 km and higher.

(4) This ranking, from an impact of 0 (the effects can be ignored) to an impact of 10 (the effects will negate the mission)

debris poses a very significant hazard to spacecraft missions as it can significantly degrade a satellite's performance or destroy it completely.

Space debris has recently become a big concern in the space industry due to its potentially devastating effect on future space technology and exploration. The Kessler syndrome describes a scenario in which space debris becomes so dense in LEO that a collision could cause a chain reaction of further collisions. Each new collision increases the likelihood of a subsequent collision rendering LEO useless and dangerous to pass through[5].

### 2.1.2 Radiation

Radiation in the space environment comes from one of three sources:

1. trapped radiation
2. solar events
3. cosmic rays

Trapped particles, such as those in the Van Allen belts, consist of protons and electrons with energies ranging from the tens of keV(electrons) to MeV (protons). These particles only pose a risk to spacecraft in Earth orbit (or orbit around any other celestial body with trapped particles) and often have sufficient energy to penetrate spacecraft and cause ionization effects. Solar event particles and cosmic rays consist of electrons and protons with energies ranging from 10 MeV to  $10^{16}$  MeV. These high energy, heavy ion particles are usually the source of single event effects (SEE) caused by their ability to directly ionize silicon material.

Different electronic components have varying degrees of vulnerability to space radiation. The two main concerns are total ionizing dose (TID) which refers to

components being exposed to high doses of radiation over a long period of time and single-events effects, such as single event upsets (SEU), which are potentially problematic events caused by a single ionizing particle.

As TID increases over the lifetime of a spacecraft's mission so does the level of material degradation, leading to threshold shifts, timing changes, changes in power consumption and, ultimately, altered performance. TID effects can be mitigated to a certain degree through the use of radiation hardened components and shielding. SEUs cause bitflips in integrated circuits which could be completely harmless if this occurs in unused memory or completely devastating if critical program memory is affected. Single event latch-ups (SEL) are events that cause circuits to short circuit their power rails to ground which has obvious, and potentially catastrophic, repercussions. Although these events can, in most cases, be corrected for through power cycling, damage through over-current and over-temperature is irreversible[2, 3].

### 2.1.3 Plasma

Plasma is a quasineutral gas that consists of both charged and neutral particles that exhibit a collective behavior. The movement of this gas, caused by magnetic fields and solar wind, generates a localized electric and magnetic field. A spacecraft in this local region accumulates a negative surface charge in an attempt to establish an equilibrium with the plasma - this is known as spacecraft charging.

Spacecraft charging can adversely affect onboard electronics and scientific payloads by generating stray signals and spurious commands. Furthermore, ion deposition on spacecraft surfaces can cause contamination and degradation of performance, particularly in solar arrays. Deep dielectric charging can cause electrical breakdown of the dielectric leading to destruction of components and contamination of nearby surfaces[2, 3].

### 2.1.4 Thermal Properties

There are two aspects to the space thermal environment to consider when designing a satellite. The first is the temperature range that the payload will be subjected to due to heat energy being absorbed from external radiation sources such as the sun, albedo<sup>1</sup>, the Earth and the Earth's atmosphere. In spacecraft with simple passive thermal control a temperature range of  $-20\text{ }^{\circ}\text{C}$  to  $60\text{ }^{\circ}\text{C}$  is not uncommon. The large majority of today's electronics can survive these temperatures and there are always higher specification components that could be used if affordable. For temperature sensitive detectors an active thermal control system may be necessary.

The second aspect to the space thermal environment is internal heat generation and dissipation techniques. Throughout a spacecraft's operational lifetime, the internal heat generation will vary depending on the mode of the mission. This heat generation must be carefully considered and accounted for due to the lack of heat convection in the absence of an atmosphere. Common practice is to create a heat conduction path to radiator surfaces to dissipate the heat into space[2, 3].

---

<sup>1</sup>Albedo is the fraction of radiation reflected from a planet back into space

### 2.1.5 Vacuum

Beyond the Earth's atmosphere is a near-perfect vacuum which has a very low density and pressure and poses challenges for spacecraft. Firstly, spacecraft can release gasses trapped or contained inside its materials through desorption, sublimation and evaporation, this is called outgassing. This process can result in significant performance degradation due to contaminants deposited on surfaces forming a molecular layer that can darken or be eroded.

Secondly, cold welding is the process of two flat similar metal surfaces fusing together in a vacuum. This process could be detrimental to mechanical subsystems that need to deploy after launch such as solar panels or scientific experiments. Finally, heat convection does not take place in a vacuum and is therefore limited to heat radiation and conduction[6, 2, 3].

## 2.2 Particle Detection

Eugene Wiegner defines a particle as “an irreducible representation of the inhomogeneous Lorentz group”[7]. Although this may seem like a complex definition, its implications are actually quite simple; a particle is a very small fragment of matter that has a non-negative and non-zero mass. Particles can vary in size ranging from the smallest sub-atomic particles to much larger macroscopic particles significantly larger than atoms and molecules. Particles are usually characterized by their properties such as:

- position
- direction
- momentum
- energy
- mass
- velocity

In order to detect a particle, it has to interact with some form of matter and deposit part, or all, of its energy into it. The final detector output is therefore as a result of charged particles interacting with one another. Some particles are very difficult to detect such as neutrinos that can pass through a detector without any trace. In these cases the detector either has to be physically large or capable of detecting minute signals.

A particle detector is an instrument that is able to measure one or more of a particle's characteristics. In order to develop and build a particle detector, the following aspects must be defined:

- particle(s) to be detected
- properties of the particle(s) to be detected
- accuracy, resolution and quality of measurements

- maximum rate of detection
- physical size and operating environment of detector

“Particle detection” usually refers to detecting the presence of a particle only, however, for the purposes of this study the term also refers to particle identification.

### 2.2.1 Solid State Detectors

Solid state detectors are commonly used in nuclear and particle physics to measure the energy of charged particles due to their high “stopping power” (or loss per unit path length). Also, due to the multiple electronic energy level structure inherent to a semiconductor, only  $\sim 3$  eV is required to detect every charge pair produced, compared to 20-30 eV in gas detectors and 100 eV in scintillating detectors. This usually results in a desirable high energy resolution[8].

The detector, however, has no internal amplification and therefore requires sophisticated readout electronics to provide low-noise amplification and digitization. The device is also not suitable for detecting fast neutrons as the detector would have to be very large. Moreover, the power requirements and high number of readout channels lead to a costly detector[9].

The Timepix Chip, shown in Figure 2.1, is an example of a solid state detector developed through a collaboration hosted by CERN. The device has good spatial resolution and energy discrimination, no noise or dark current and unlimited dynamic scale. However, the device is very costly and is limited to detecting 11,810 events per second.

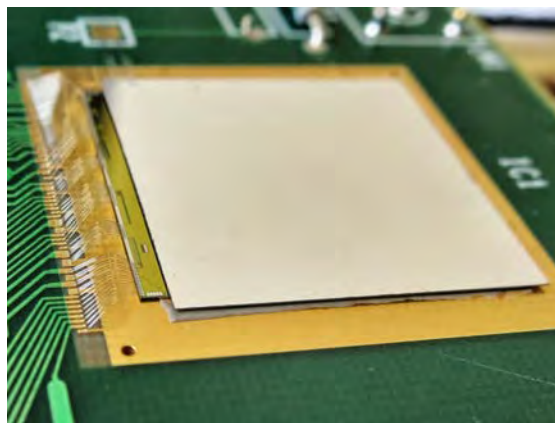


Figure 2.1: A 100um-on-100um Timepix Assembly[10]

### 2.2.2 Gas Ionization Detectors

Gas-filled detectors were some of the earliest ionization-based detectors and can be divided into three groups:

1. ionization chambers
2. proportional counters
3. geiger counters

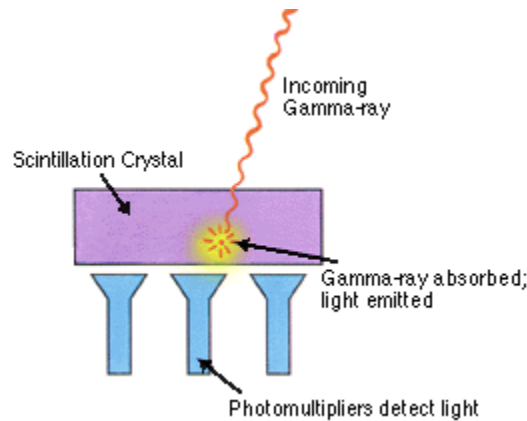


Figure 2.3: Diagram of a typical scintillation detector[12]

All three gas detectors consist of an anode and a cathode, separated by initially ionized fill gas. Gas detectors are capable of measuring very high radiation rates and can be constructed to cover very large areas. However, these detectors have a very small resultant output and therefore also require sophisticated readout electronics. Moreover, sustained high radiation levels can degrade the fill gas on certain detectors[8].

A common example of a gas ionization detector is an ionization-type smoke detector found in many homes and commercial settings, see Figure 2.2. These devices wait for smoke to interrupt the ionization process between the anode and cathode and once this happens, an alarm is triggered.



Figure 2.2: A commercial ionization-type smoke detector[11]

### 2.2.3 Scintillation Detectors

A scintillation detector, as the name suggests, consists of a scintillating material and a photosensor, see Figure 2.3. The basic principle of operation relies upon a particle striking the scintillator, depositing energy and emitting a photon. The emitted light is then detected by a nearby photosensor.

### 2.2.3.1 Scintillating Material

A scintillator is a material whose properties allow for the conversion of an incoming particle's deposited energy into luminescence light. This light can then be detected by a nearby photosensor, resulting in the final electrical output signal.

Scintillators are available in a solid, liquid and gaseous form and can be developed to satisfy almost any application's requirements. Generally scintillators can be grouped into two categories, organic or inorganic[13]:

**Organic Scintillators** are composed of aromatic hydrocarbons (which may be in plastic or liquid form) and contain fluorescent organic compounds. No crystal structure is needed for scintillation, unlike inorganic scintillators, as scintillation occurs on a molecular level. The scintillation process in organic scintillators is very fast, making them ideal for use in physics detectors where triggering and precise timing information is important. Particles are often not fully absorbed due to the scintillator's low density.

**Inorganic Scintillators** are crystals made of alkali halides or oxides and scintillate due to their crystalline structure. They are primarily used in X-ray and gamma-ray spectroscopy and due to their higher density. Inorganic scintillators are usually designed to fully absorb incident particles.

### 2.2.3.2 Scintillation Process

When a charged particle strikes and travels through a scintillating material, it interacts with neighboring atomic electrons. This interaction results in the charged particle losing energy and the atomic electrons becoming excited/ionized (1-electrons are lifted from the singlet ground state up into an excited singlet state). The energy loss per distance traveled for the charged particle is described mathematically by the Bethe-Bloch formula[13].

Luminescence occurs when these electrons return back to their original unexcited state (a radiative transition from the excited singlet state to the singlet ground state). Three types of luminescence exist: fluorescence, phosphorescence and delayed fluorescence. For the purposes of this study, fluorescence is the desired process as it occurs shortly after particle interaction, therefore allowing precise timing measurements. Scintillators can be developed such that the probability of the other luminescence processes occurring is greatly reduced.

### 2.2.3.3 Stokes' Shift

If scintillators are not designed appropriately, the emitted fluorescence light could be immediately reabsorbed. In this case the only light that would ever escape the scintillator is that which is emitted near the boundary surface, greatly limiting the number of useful scintillator geometries.

To mitigate this reabsorption the emission spectrum of the material must be offset from the absorption spectrum. This difference between the two spectra is known as Stokes' shift, see Figure 2.4. As a result the emitted light can pass

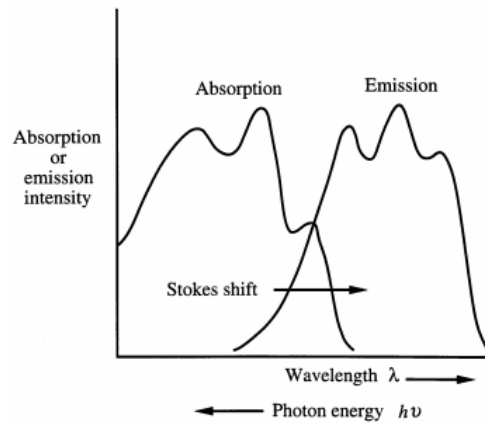


Figure 2.4: Graph of offset absorption and emission spectrum[13]

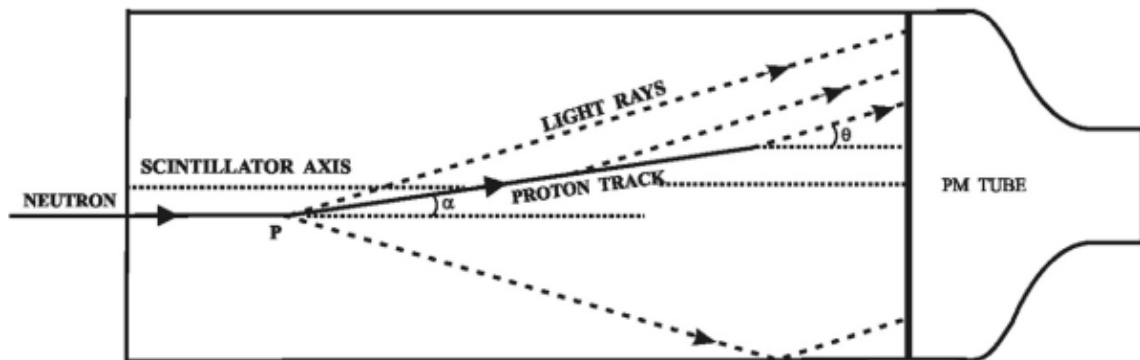


Figure 2.5: Diagram of neutron scintillation in an organic plastic scintillator[14]

through the scintillator without being absorbed so that it can make its way to the photosensor for detection.

#### 2.2.3.4 Neutron Detection

Neutrons are generally difficult to detect due to their weak interaction with matter and their large range in energies. Neutrons will, however, interact with hydrogen atom-rich (or proton-rich) organic materials through elastic scattering. During this process a small portion of the neutron's kinetic energy is transferred to a proton, see Figure 2.5. This secondary "generation" of energetic protons (charged particles) can be used to indirectly detect neutrons through the regular scintillation process described above.

#### 2.2.3.5 Gamma-Ray Detection

Gamma-rays are high energy photons and interact with matter in three ways:

1. photoelectric absorption
2. Compton scattering
3. pair production

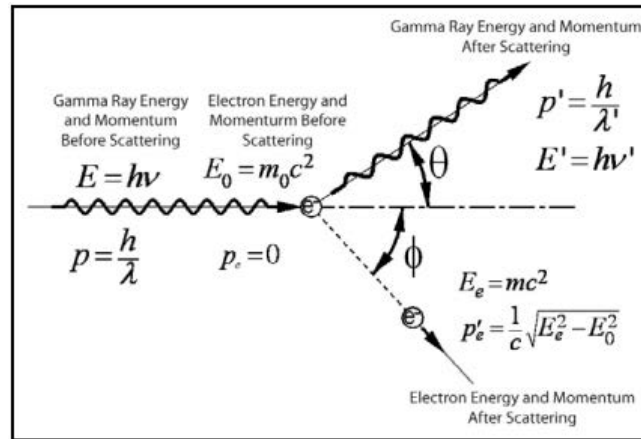


Figure 2.6: Compton scattering process for Gamma-Rays in a scintillating material

Due to the inherently low number of electrons per atom in organic scintillators and the strong dependency of the probability of photoelectric absorption and pair production on the number of electrons in the scintillator, these interactions can be neglected. Therefore, only *Compton scattering* need be considered.

Compton scattering, for the purposes of the detector, refers to the process of inelastic scattering of a gamma-ray (high energy photon) by an electron, causing a decrease in energy of the gamma-ray and an increase in energy of the electron. This secondary “generation” of energetic electrons (charged particles) can be used to indirectly detect gamma-rays through the regular scintillation process.

### 2.2.3.6 Detection Summary

The instrument envisioned for this study should have the ability to detect neutrons, gamma-rays and charged particles. Figure 2.7 summarizes the different detection principles and shows how a scintillation detector can satisfy the outlined requirements.

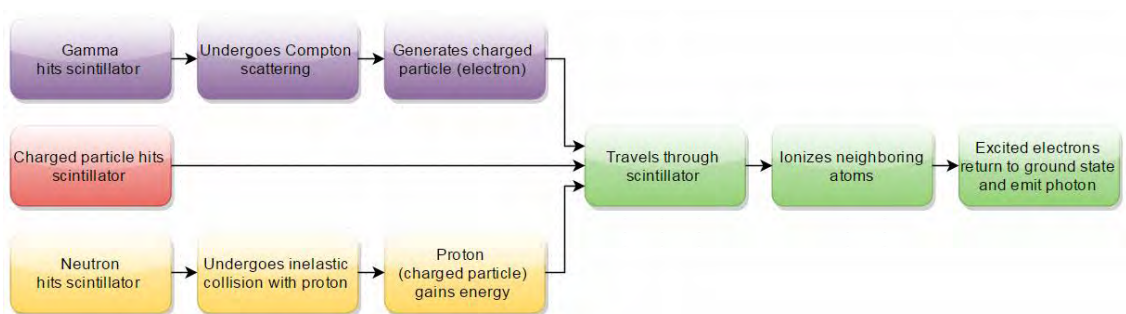


Figure 2.7: Particle detection principles using a scintillating material

## 2.2.4 Radiation Sources

A particle detector can be tested in a lab environment to characterize its efficiency, sensitivity and performance. To conduct these tests, a source for each particle type, namely gamma-rays, neutrons and charged particles (such as protons), was required.

#### 2.2.4.1 Gamma-Rays

Certain radionuclides will emit electromagnetic radiation (photons) of discrete energies when decaying. Examples of such radionuclides which could be used to test the detector's response to gamma-rays are as follows:

- Caesium-137 (Cs-137)
- Sodium-22 (Na-22)
- Manganese-54 (Mn-54)
- Cobalt-60 (Co-60)

These sources can be readily, and inexpensively, purchased online, in most cases without the need of a license[15].

#### 2.2.4.2 Neutrons

In a lab setting, neutrons can be easily generated in one of two ways:

1. The nuclear reaction caused by bombarding low atomic weight isotopes with alpha particles results in a neutron source. A common combination is americium-beryllium (AmBe) where americium is used as the alpha source and beryllium is the low atomic weight isotope. This is known as an **AmBe source**.
2. A sealed neutron tube, such as a **tritium generator**, generates neutrons by inducing fusion between tritium ions and metal hydride targets.

#### 2.2.4.3 Charged Particles

The Earth is being continually bombarded by highly energetic nuclei, consisting mainly of high-energy protons, referred to as "cosmic rays." The origin of these cosmic rays is still under debate today but they are thought to arise from supernova explosions, active galactic nuclei, gamma-ray bursts etc[16]. These naturally and ever-occurring cosmic rays are a useful source to test the detector's response to charged particles directly.

Alternatively, one could use an electron or proton beam but because this usually requires a cyclotron or particle accelerator it results in a very expensive process.

### 2.3 Light Detection

A photosensor needs to be used in conjunction with a scintillating detector to convert the emitted photon into a signal that can be detected electronically. The final electrical signal can then be used to infer information about the particle interaction that took place in the scintillator.

An ideal photosensor will have the following features:

- a linearly proportional response to incident photon flux
- low dark current or count rates
- robust and not susceptible to damage from radiation

- high internal gain
- broad spectral response
- fast response time (sub nanosecond)

There are many photosensors available that satisfy some, or most, of these characteristics but there is usually a trade-off between features such as internal gain and dark current or spectral response and proportionality. It is therefore important to consider all of the various available detectors with the end application in mind to determine whether or not the technology is, in fact, suitable.

### 2.3.1 Photomultiplier Tube

A Photomultiplier Tube (PMT) is a vacuum tube photodetector that has been around for over five decades and remains one of the fastest and most sensitive optical detectors available. These detectors are used extensively in the fields of high-energy physics, medicine, biotechnology, aerospace and many more. PMTs are also one of the only vacuum tube technologies still being manufactured today because, in many cases, they are still able to out-perform their silicon counterparts.

PMTs consist of five main components, namely:

1. a sealed housing with an input window
2. a photocathode
3. a focusing electrode
4. multiple dynodes
5. an anode

The configuration of these components can be seen in Figure 2.8.

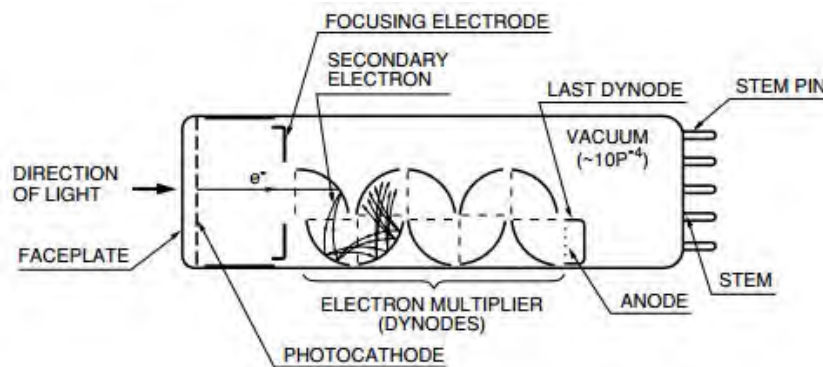


Figure 2.8: Diagram of a photomultiplier tube[17]

The basic operational principle is based on photons (light) entering the housing through the input window where, by means of the photoelectric effect, electrons in the photocathode can be excited. These excited electrons are emitted into the vacuum where they are accelerated onto the first dynode via the focusing electrode. Through secondary electron emission, the photoelectrons are multiplied at each

dynode stage and are finally collected at the anode. The PMT's final output is a current proportional to the incident photon flux that can be read out with a transimpedance amplifier or similar.

PMTs boast very high gains ( $10^6$ ) and photosensitivities ( $1 \text{ A}/\mu\text{W}$ ) making them ideal for photon counting and other low-light applications. They are generally stable, low-noise and require very little operating power but one of their main advantages is their incredibly fast picosecond response times.

However, PMTs require large bias voltages (1-2 kV), resulting in the use of costly high-voltage power supplies, are expensive ( $\sim \$ 2\,000$  and up), have a limited spectral range (100 nm-1000 nm) and a poor quantum efficiency ( $< 30\%$ ). They are also bulky and delicate due to their vacuum tube structure and can be adversely affected by magnetic fields which may limit their suitability for some applications[18, 17].

### 2.3.2 PIN Photodiode

A PIN photodiode, as the name implies consists of a *P*-type region, an undoped Intrinsic region and an *N*-type region. It differs to a regular diode in that it has the additional intrinsic region making it sub-optimal as a rectifier but optimal as a photodetector. Due to a PIN photodiode's high bandwidth (tens of gigahertz) they are commonly employed in high-speed optical fiber communication receivers.

When light enters a PIN photodiode, see Figure 2.9, with an incident energy greater than that of the band gap energy, electron-hole pairs are generated (electrons elevate into the conduction band, leaving holes in their place in the valence band). PIN photodiodes are usually operated in photoconductive mode where a moderate reverse bias is applied across the diode.

During the "quiescent" period no current flows through the diode until a photon strikes an atom in the intrinsic region and generates an electron-hole pair. Under the influence of a reverse bias, the electrons are accelerated towards the N-layer and the holes towards the P-layer. This movement of charge is detected as a small current and the number of electron-hole pairs generated is proportional to the amount of incident light.

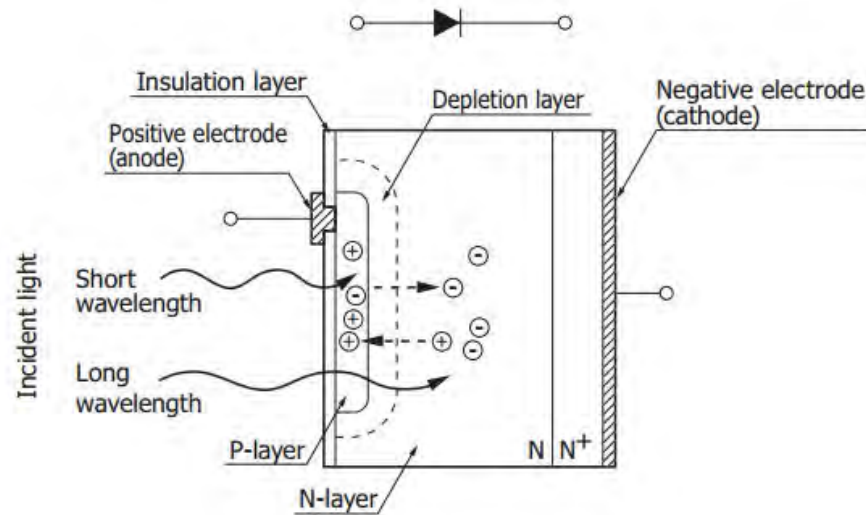


Figure 2.9: Cross section of a silicon PIN photodiode[19]

PIN photodiodes are rugged, compact and lightweight making them ideal for applications such as handheld radiation detectors. They are also highly linear at high frequencies, generate very little noise and have a wide spectral response. These diodes are available with various substrate materials such as silicon (Si), indium gallium arsenide (InGaAs) and germanium (Ge), each optimized for a particular purpose and operating wavelength.

Unfortunately, PIN diodes are severely limited by their complete lack of internal gain. Moreover, these diodes need to be selected very carefully for a particular application due to their poor reverse recovery times and non-linear characteristics at low frequencies. One could increase the size of the intrinsic region to increase the diode's linearity at low frequencies but this adversely affects the turn off time[19].

### 2.3.3 Avalanche Photodiode

Avalanche photodiodes (APDs) are similar to regular PIN photodiodes but are faster and more sensitive. Due to these improved characteristics APDs are able to measure lower light levels and are therefore used in applications such as long-distance optical communications, optical distance measurements etc.

When light enters an APD electron-hole pairs are generated - provided that the incident light energy is greater than that of the band gap energy. If a sufficiently large reverse bias is applied to the diode's PN-junction while these additional electron-holes pairs are generated, avalanche multiplications of the photocurrent can be achieved. Figure 2.10 depicts the avalanche process as well as the relative electric field within the PN-junction.

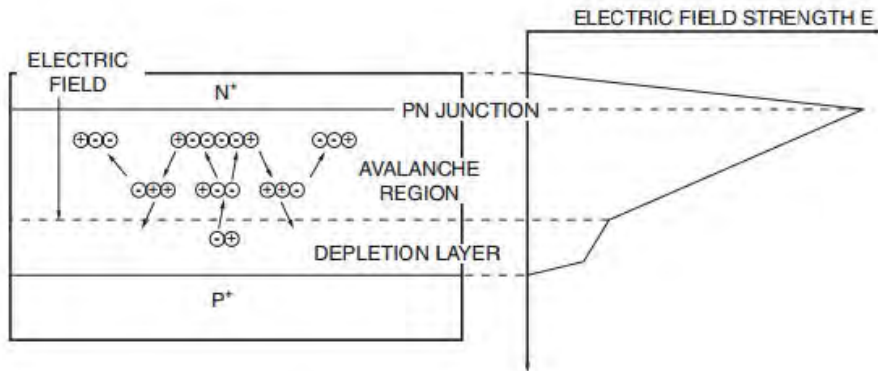


Figure 2.10: Diagram of the avalanche process with the APD[20]

APDs have similar advantages to PMTs in that they are very sensitive and very fast but they do not need as high a bias voltage and have a higher photon detection efficiency. Furthermore, APDs are solid-state devices, are much smaller and more robust, are insensitive to magnetic fields and the device is not damaged if over-exposed.

The main drawbacks associated with APDs are that they still require a relatively high bias voltage, they are much slower than the alternatives (nanoseconds rather than picoseconds) and they exhibit a lot of noise (associated with the stochastic APD multiplication process). APDs must also be selected carefully as their capacitance (directly related to speed of response) increases with device area and thickness. For this reason, for any “high-speed” applications their detector size is limited to a diameter under 10 mm[20, 18].

### 2.3.4 Silicon Photomultiplier

Silicon photomultipliers (SiPMs) are photosensitive devices that consist of an array of APDs. These APDs usually share a common silicon substrate, hence the term “silicon” photomultiplier. These devices are also referred to as multi-pixel photon counters (MPPCs) by some manufacturers. Figure 2.11 shows an image of a SiPM manufactured by Sensl.

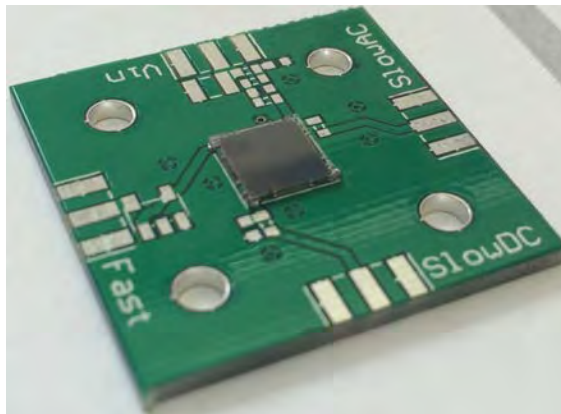


Figure 2.11: A Sensl SiPM on a custom breakout board

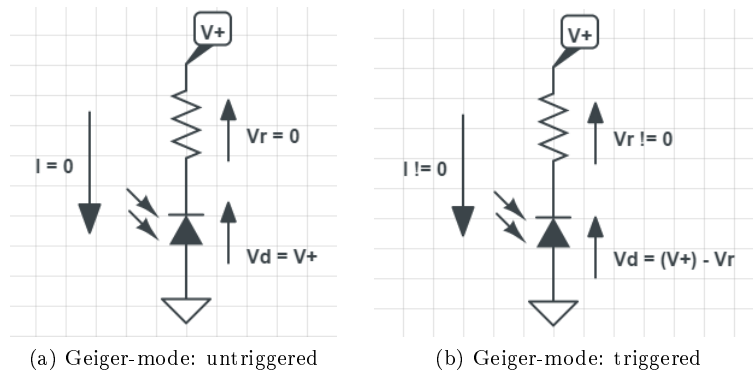


Figure 2.12: SiPM Geiger-mode demonstration [Author’s own images]

The SiPM is a relatively new technology but due to its adoption into industries such as nuclear medicine, a large amount of research and development has been conducted. Today, these devices are being used in a large variety of applications ranging from medical imaging and biophotonics to LiDAR and hazard/threat detection. The following section pertains to SiPMs in general but has particular relevance to Sensl’s range of photomultipliers[21, 22].

SiPMs are compact, robust, high-gain, low-cost and require a relatively low bias voltage ( $\sim 30$  V). Furthermore, they have a fast response time ( $< 100$  ps) and are insensitive to magnetic fields. They do, however, suffer from increased dark current rates for large area devices. Moreover, due to surface transmission and fill factor, SiPMs have a relatively low quantum efficiency (10-30 %)[21].

#### 2.3.4.1 Operating Principle

Photons incident on the surface of silicon can either be absorbed or reflected. Those that are absorbed may have the ability to transfer their energy to a valence electron and transport it from the valence band to the conduction band. Electrons found in the conduction band can be considered as “free” and in the presence of an electric field these electrons would move in a net direction, known as a current. This effect is used and achieved by many photo-detectors by applying a reverse bias across a purpose-built PN-junction.

If a sufficiently high electric field is applied across the PN-junction an electron transported from the valence to conduction band could possess sufficient kinetic energy to create secondary “free” electrons. This process is called *impact ionization* and allows a single photoelectron to trigger a self-perpetuating ionization cascade that will spread through the silicon diode. This mode of operation is called Geiger mode.

During regular operation a reverse bias is applied across a silicon photomultiplier and series resistor. Before a photon is absorbed by the SiPMs, the full voltage is seen across the individual avalanche diodes as there is no net current, see Figure 2.12a. Once an APD undergoes impact ionization, known as the “triggered” state, a current begins to flow and the voltage across the diode decreases because of the voltage developed across the resistor, see Figure 2.12b.

This resistor, known as a quenching resistor, is intentionally placed in series with the APDs in order to reduce the voltage across the APDs to below their respective breakdown voltages, thus “resetting” the diodes and allowing them to further detect photon absorption events.

The main disadvantage of Geiger-mode APDs is the lack of proportionality as the method is either off (no current) or on (macroscopic current). A silicon photomultiplier overcomes this limitation by using a dense array of small, isolated Geiger-mode APDs or “microcells”, see Figure 2.13. To generate a proportional output based on incident photons the Geiger currents from each microcell are summed to generate the final output. Thus, although each individual APD operates in a digital “on/off” fashion, the final output is considered to be analog and proportional.

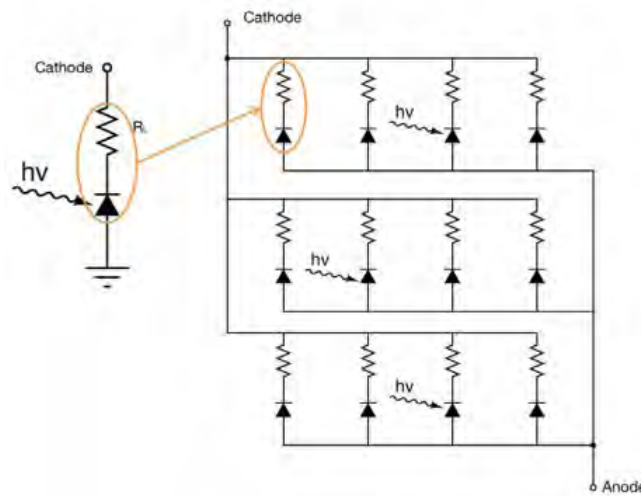


Figure 2.13: An array of isolated Geiger-mode photodiodes or microcells[21]

#### 2.3.4.2 Performance Parameters

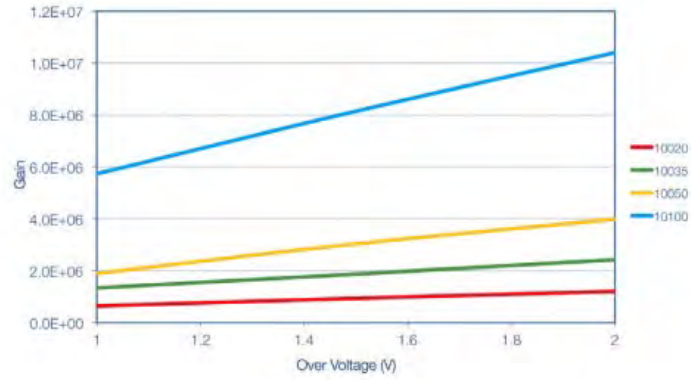
**Over-Voltage, Gain and Noise:** Each silicon photomultiplier has a breakdown voltage at which the electric field strength generated across the junction is sufficient to cause a Geiger current. The term “over-voltage” refers to the additional voltage, above the breakdown voltage, at which the silicon photomultiplier is operated.

The overall gain achieved by a silicon photomultiplier is as follows:

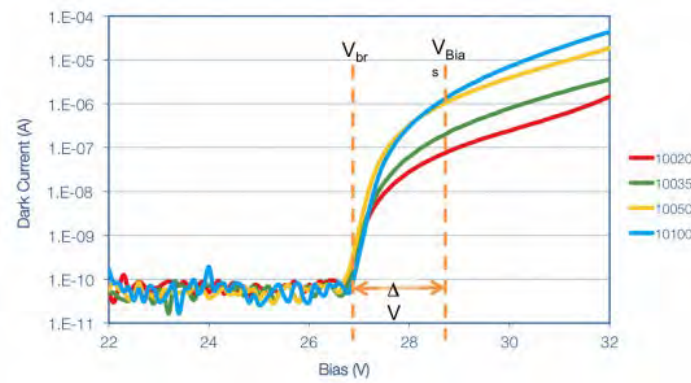
$$G = \frac{C\Delta V}{q} \quad (2.1)$$

where  $C$  is the effective capacitance of the PN-junction,  $\Delta V$  is the over-voltage and  $q$  is the charge of an electron.

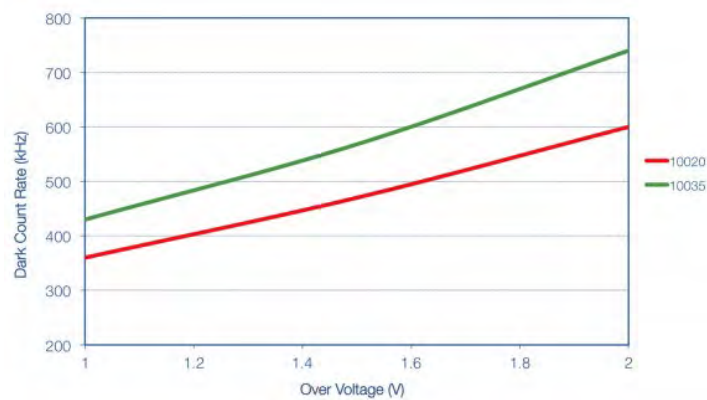
From Equation 2.1 it is clear that the silicon photomultiplier gain is linearly proportional to the applied over-voltage. Although this may suggest that a higher over-voltage is required for more sensitive applications the noise and dark current generated by the silicon photomultiplier are also proportional to the applied over-voltage, see Figure 2.14b.



(a) Gain vs. Over-Voltage



(b) Dark Current vs. Bias Voltage



(c) Noise vs. Over-Voltage

Figure 2.14: Silicon Photomultiplier Performance Trade-Offs for Various Sensl Models[21]

Noise in silicon photomultipliers is primarily due to thermally excited electrons that have sufficient energy to cause band gap jumps. Ultimately, the noise generated in the PN-junction determines the minimum signal that can be detected when an incident photon is absorbed. For applications where minute signals are to be detected, the smallest over-voltage may be of interest. See Figure 2.14c.

**Photon Detection Efficiency:** The photon detection efficiency (PDE) is similar to quantum efficiency (QE) and is commonly used to characterize the performance of photo-detectors. Where QE refers to the percentage of incident photons that strike a photo-sensor that produce light, PDE refers to the probability of an incident photon producing a Geiger current on any one of the microcells.

The PDE for a silicon photomultiplier is described by the following formula:

$$PDE = \frac{Rhc}{G\lambda e} \quad (2.2)$$

where  $R$  is the responsivity (photocurrent / incident optical power),  $h$  is Planck's constant,  $c$  is the speed of light,  $G$  is the gain of the silicon photomultiplier,  $\lambda$  is the incident light's wavelength and  $e$  is the charge of an electron.

Silicon photomultipliers have relatively low PDEs (<30%) compared to some technologies but have many other advantages in their favor. Figure 2.15 describes the relationship between the PDE and the incident photon wavelength for various Sensl SiPM models.

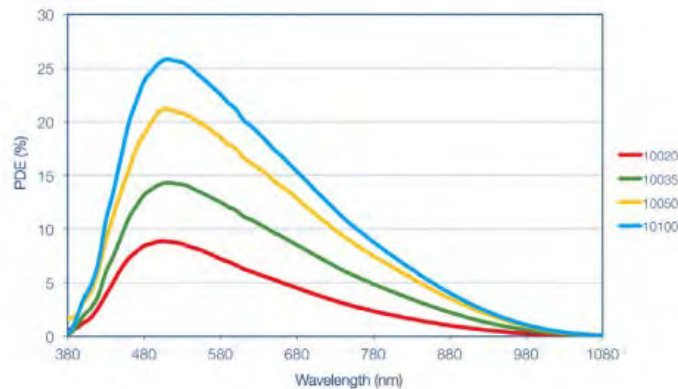
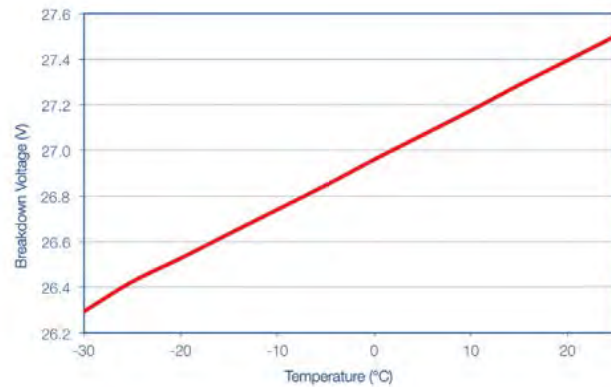


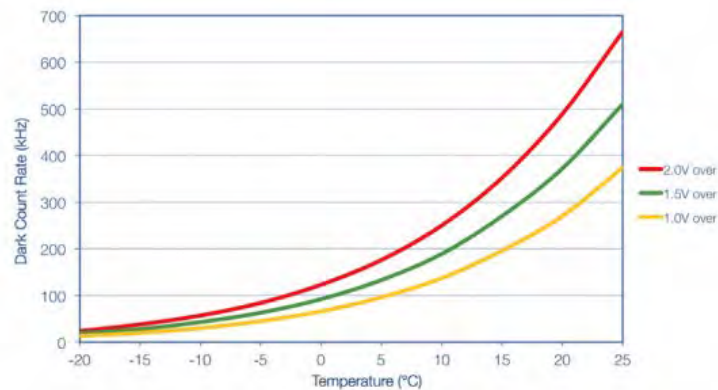
Figure 2.15: Comparison of the PDE vs. wavelength for four of Sensl's SiPM models[21]

**Temperature Dependence:** A SiPM's breakdown voltage and dark rate count (noise) is sensitive to temperature changes and this may need to be taken into consideration for certain applications. Figure 2.16a and 2.16b demonstrates this temperature dependence for an particular SiPM device.

Fortunately the breakdown voltage is linearly proportional to temperature over a particular temperature range making it easier to compensate for. The temperature dependence can be dealt with by either regulating the SiPM's temperature or dynamically adjusting the applied voltage.



(a)



(b)

Figure 2.16: SiPM temperature dependence[21]

Similarly, the noise is proportional to the temperature but in this case it has an exponential relationship. For every 10 °C the device is cooled, there is a 50 % improvement in noise. Therefore, for low light level detection it may be critical to incorporate active cooling.

#### 2.3.4.3 Comparison

A comparison of the four primary photodetector technologies considered for the study can be found in Table 2.2. The comparison factors were chosen due to their relevance to the harsh space environment and their applicability to a scintillation detector[22, 18]. The values quoted assume the implementation on a spacecraft with moderate thermal control and ideal power supplies and readout electronics for a fair and relevant comparison.

Table 2.2: Comparison of photodetector technologies considered for the study

	PIN	APD	PMT	SiPM
<b>PDE/QE</b>	75%	50%	20%	12%
<b>Gain</b>	1	100-200	$10^6 - 10^7$	$10^6$
<b>Voltage</b>	10-50 V	100-500 V	1-2 kV	10-50 V
<b>Speed/Rise-Time</b>	~100ps	~10ns	~100ps	~50ps
<b>Electronic Complexity</b>	Medium	Medium	High	Low
<b>Robustness</b>	High	Medium	Low	High
<b>Magnetic Field Sensitivity</b>	Low	Low	High	Low
<b>Noise</b>	Low	Medium	Low	High
<b>Temperature Sensitivity</b>	Low	High	Low	Low
<b>Large Area Availability</b>	Low	Low	High	High

### 2.3.5 Related Research

A group from Sensl, a leading silicon photomultiplier manufacturer, published a paper discussing tiling of silicon photomultipliers for large area, low light sensing applications[23]. The paper thoroughly discusses the theory, experimental setup and results, and concludes that their technology has potential for large area detection and 2D spatial resolution.

Similarly, in [24], a silicon photomultiplier was assessed at low temperatures to determine its suitability as a scintillation readout device in liquid argon particle detectors. The dark current was shown to reduce exponentially with temperature for all tested bias voltages and the probability of crosstalk was linearly proportional to the gain. However, it was also shown that both the probability of crosstalk and the photon detection efficiency was temperature independent when tested across the temperature range of  $-196\text{ }^\circ\text{C}$  to  $+25\text{ }^\circ\text{C}$ .

[25] explored the suitability of silicon photomultipliers for space missions. The study focused on testing the silicon photomultiplier’s response to both single photoelectrons and “many-photons”. It was shown that the SiPM had an excellent single photoelectron resolution and could undergo real time calibration on flights.

Lockheed Martin and Stanford University in [26] discuss the design and testing of a solid state charged particle detector for CubeSats. The payload made use of a solid state charged particle detector produced by Ortec but testing was still to be conducted for the ongoing project.

## 2.4 Data Collection

The very small analog signals received from the photodetectors would have to be adequately amplified and digitized before the acquired data could be processed and analyzed. Furthermore, the high frequency signals would only arrive periodically making continuous data collection a wasteful process. Consider the case where a high-energy physics (HEP) detector is to identify a particle by analyzing the resultant signal’s shape at a rate of 10,000 events per second, where each event lasts for approximately 200 nanoseconds. Sampling continuously at multiple gigahertz would result in a large amount of data to process. More importantly, however, only

0.2 % of the data would have any relevance suggesting that 99.8 % of the data collected would be useless.

The encircled blocks in Figure 2.17 outlines a possible data collection topology to explain the relevance of the following sections.

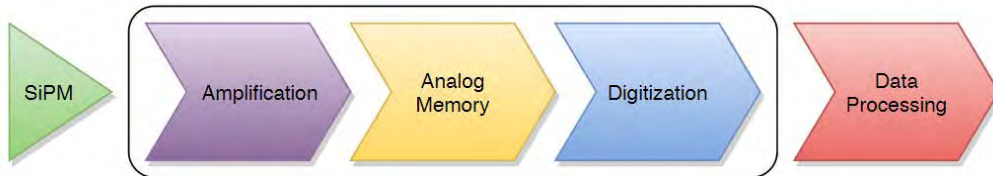


Figure 2.17: Example of a data collection topology

### 2.4.1 Amplification

The signals obtained from photosensors are usually very small, particularly when detecting very low light levels (near single photon). Therefore, before a signal can be digitized it must be adequately amplified thereby allowing it to make full use of the digitizer's finite resolution.

#### 2.4.1.1 Single-Ended Configurations

A photodetector usually has a single-ended output (one output signal) that needs to be amplified. In single-ended digitization systems, the conversion is based on the signal level relative to ground and therefore relies on ground being constant (0 V) at the photodetector and at the digitizer. This assumption is unfortunately not true, particularly in high speed applications, and usually leads to offset errors. Furthermore, single-ended configurations are highly susceptible to noise from spurious neighboring sources. Due to the nature of the configuration, the receiver (or digitizer in this case) has no way of distinguishing between the signal and noise.

#### 2.4.1.2 Differential Configurations

A differential configuration has two output signals (usually out+ and out-) that run parallel to one another. At the digitizer the signal of interest is the difference in voltage between the two output signals, rather than the absolute value of either. This configuration improves on both the ground and noise issues inherent to single-ended configurations because interference or offsets added to both lines will not be detected by the digitizer, provided that the signals remain within the differential voltage range[27].

There are a few specifications to keep in mind when using differential configurations, namely common-mode voltage, differential-mode voltage and common-mode range. It is imperative that these values are well understood to avoid violating the device's input limitations. Incorrect voltages can cause distortion, saturation and in some cases device destruction.

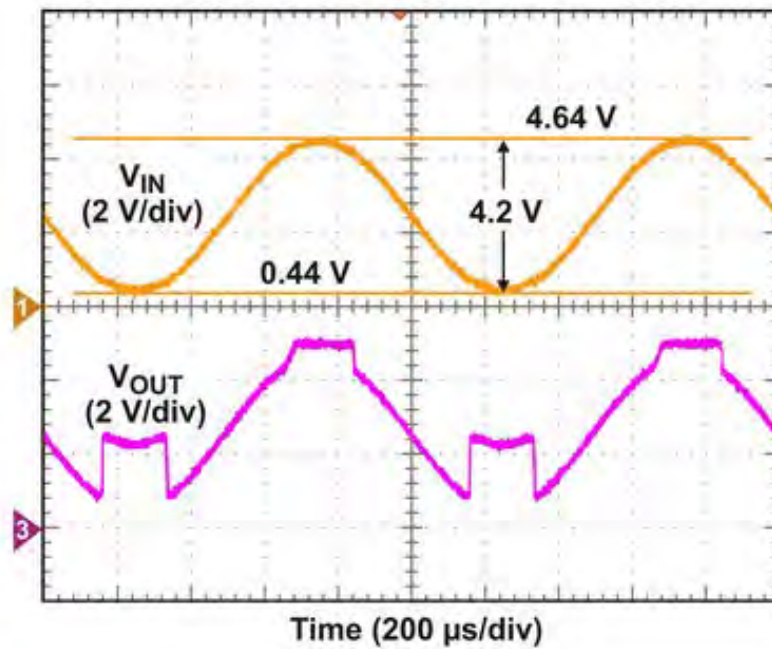


Figure 2.18: Example input (1) and output (3) signals showing the effects of a common mode voltage range violation on an amplifier[28]

**Common-Mode Voltage** is the voltage that is common to both inputs and can be calculated as follows:

$$V_{CM} = \frac{V_+ + V_-}{2}$$

The common-mode voltage is also defined as the average value of the differential mode voltage and is approximately 2.5 V for the input signal shown in Figure 2.18.

**Common-Mode Range** describes how closely a signal can approach limits inherent to a particular device such as its voltage rails. As an example, consider a device that has a common-mode range of 1.15 V to 3.85 V, such as the TL971 opamp. If an input with a peak-to-peak voltage of 4.2 V is applied, with a common-mode voltage of 2.5 V, these limits are violated. Figure 2.18 shows this input signal and the resultant, badly distorted, signal[28].

**Differential-Mode Voltage** describes the maximum difference between the two differential inputs:  $V_+ - V_-$ .

#### 2.4.1.3 Termination

In order to reduce reflections on the differential lines at high switching frequencies, thereby improving signal integrity, the lines must be correctly terminated. Optimal termination to reduce signal reflection is defined by matching the transmitting device's output impedance to the receiving device's input impedance, sometimes referred to as "double termination".

For single-ended configurations, outputs are matched by placing a  $50\ \Omega$  series resistor close to the source and inputs are matched by placing a  $50\ \Omega$  resistor down to ground near the sink (or receiver). Differential lines follow a similar convention with the output matching using a  $50\ \Omega$  series resistor on each line, however, the inputs usually make use of a  $100\ \Omega$  across the two lines at the sink. Although  $50\ \Omega$  termination is the most common value for modern high-speed electronics, there are other termination values too. An example of double termination is shown in Figure 2.19.

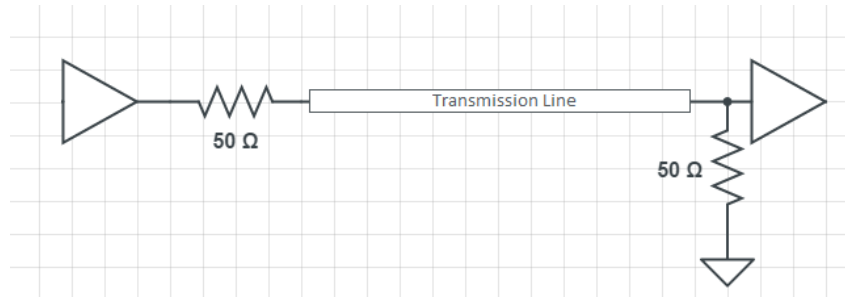


Figure 2.19: Example of  $50\ \Omega$  termination for a non-inverting opamp input

#### 2.4.1.4 Programmable Amplifiers

Fixed gain differential amplifiers are very common, particularly for RF applications that have a single task. However, particle detection requires different amplification levels dependent on the particle under scrutiny. As an example, gamma-rays will have a significantly smaller amplitude response than that of an ultra high-energy cosmic ray.

Therefore, in a multi-particle detector, a dynamic amplification value may be critical for the accurate detection of particle type and to determine pulse shape information. In this case, a programmable gain amplifier (PGA) is ideal as it can alter its gain based on inputs from an external controller, thereby giving maximum effective resolution. To solve the issue raised in the previous example, when detecting cosmic rays the gain can be adequately lowered and, conversely, increased when attempting to detect gamma-rays.

As these amplifiers are not optimized to operate at a particular gain set-point they are not as efficient, in most cases, as their prime counterparts. They should therefore be used cautiously to avoid unreasonable power and thermal requirements. Figure 2.20 shows the block diagram of an 8 channel, high-bandwidth, analog front-end from TI designed specifically for data acquisition systems.

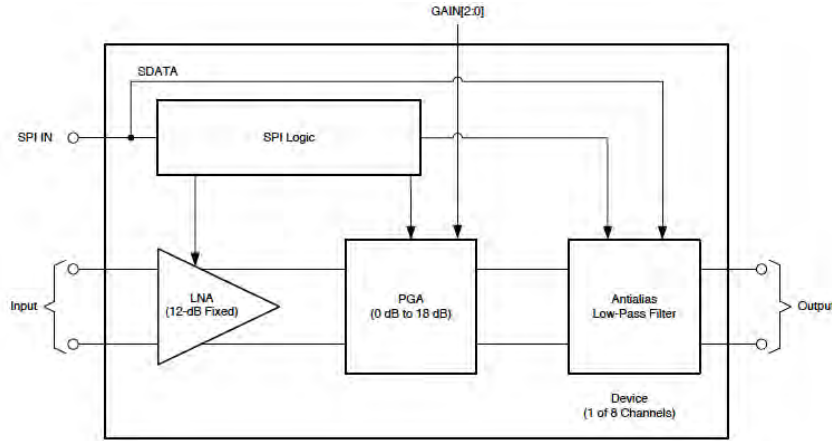


Figure 2.20: Block diagram of TI's PGA5807A programmable gain amplifier[29]

### 2.4.2 Analog Memory

High-speed ADCs operating in the giga-sample-per-second (GSPS) range are not only very expensive but also require a great deal of electrical power. This leads to complex power supply requirements and thermal constraints. Furthermore, these systems are usually limited to 8 bits per sample which results in fairly coarse resolution.

An alternative to this method is using analog memory, such as a switched capacitor array (SCA), that is able to store data at very high rates (gigahertz) on small signal capacitors (picofarads) while using little electrical power. Figure 2.21 depicts a simplified schematic for a single SCA memory channel. Once triggered the data stored on the capacitors can be read out at a much slower rate (tens of megahertz), drastically reducing the ADC requirements. SCAs are commonly used on digital oscilloscopes.

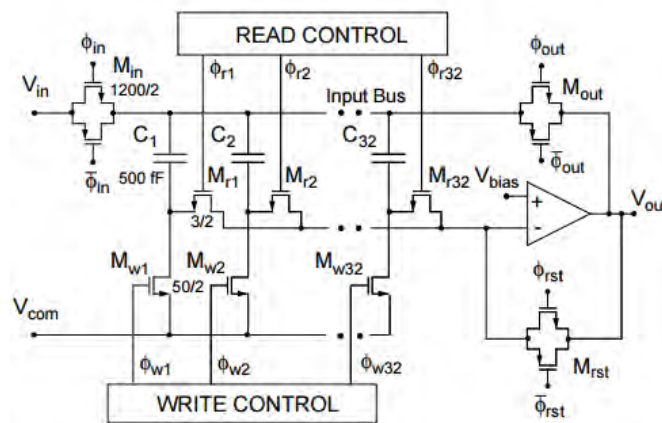


Figure 2.21: Simplified schematic of an SCA memory channel[30]

Systems based on SCAs have been shown to perform better than their high-speed ADC equivalent in terms of cost, density, dynamic range, and power dissipation. SCAs do have their drawbacks though; the analog data has to be read out within

microseconds of storage to avoid the small capacitors discharging through leakage current. Moreover, most SCA topologies require that the entire analog memory bank be read out before a new waveform can be acquired enforcing a set minimum dead-time between data acquisitions.

SCA analog waveform storage is not a new concept by any means. In [31], which dates back to June 1990, a 4096 cell SCA integrated circuit was designed, fabricated and tested. Similarly, three years later, Stanford University described an analog memory integrated circuit that was able to run at 900 MHz[30].

### 2.4.3 Digitization

The digitization process requires an analog-to-digital converter (ADC) which samples a continuous analog signal and converts it into a discrete digital word.

#### 2.4.3.1 ADC Types

There are many types of ADCs such as direct conversion (or flash), successive-approximation, sigma-delta and time-interleaved ADCs, each with their own set of advantages and disadvantages. Below is an explanation of the relevant ADC architectures, as well as a summary in the form of a chart, see Figure 2.22[32, 33].

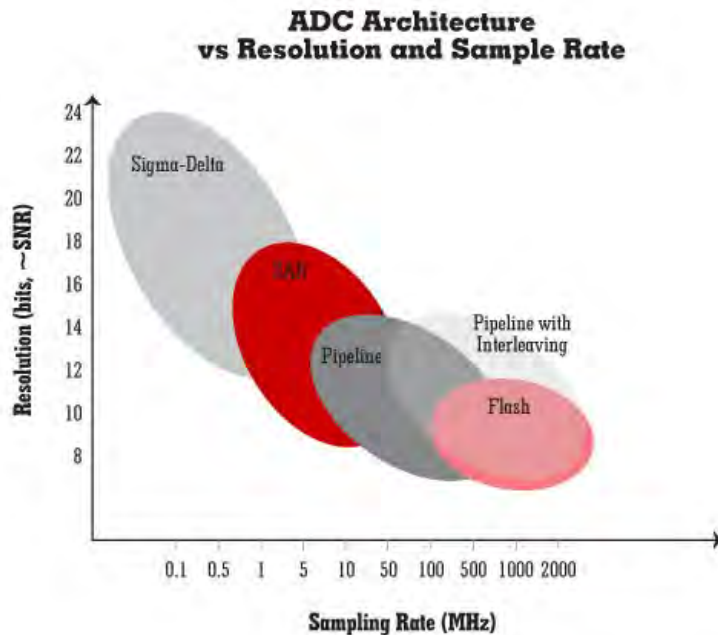


Figure 2.22: Available ADC architectures with varying resolution and sampling rate[32]

**Integrating** ADCs sample by integrating the input voltage for a known period and comparing it to a known reference value. They are best for low frequency applications such as digital multimeters where low power consumption, low-noise and high resolution is of interest. These ADCs are slow and their conversion time doubles for every extra bit of resolution.

**Sigma-Delta ( $\Sigma - \Delta$ )** ADCs operate by oversampling the input voltage and then filtering around the desired signal band. These ADCs offer high resolution (16-24 bits) and do not require any high-precision external components and have therefore almost completely replaced integrating ADCs. However, they are still slow (hundreds of kilohertz) and the noise is proportional to the output data rate.

**Successive-Approximation (SAR)** architecture is one of the most common architectures found in ADCs, particularly for multiplexed data-acquisition applications. These devices use a binary search algorithm, which traces back to the 1500s[34], to achieve sampling and they are generally limited to very low (<10) MSPS. They offer medium to high resolution (8-16 bit), are small in size and require relatively little power.

**Pipelined** architecture offers very fast sampling rates (100+ MSPS) while still maintaining medium to high resolution (8-16 bits). Pipelined ADC's harness the power of parallelism by working on a small subset of bits, via sub-ranging, and this allows higher sampling rates. Although still lower-powered than flash, this architecture requires more power than its slower alternatives.

**Flash** converters are some of the fastest ADCs available, entering the low gigahertz range. The flash architecture is limited to around 6-8 bits of resolution, requires a considerable amount of power and is significantly more expensive than its slower alternatives. These converters achieve these speeds by implementing a bank of comparators and sampling the input signal simultaneously.

#### 2.4.3.2 Performance Parameters

Choosing the correct ADC requires an understanding of the performance parameters and how they relate to the particular application under consideration. Figure 2.23 shows an example of a fast-Fourier transform (FFT) of an ADC's output as a result of an input sine wave, from which four power levels can be defined:

- Signal power ( $P_S$ ) - Amplitude of fundamental (largest) signal component
- Noise floor power ( $P_N$ ) - Amplitude of noise floor
- Power of harmonics ( $P_D$ ) - Amplitude of harmonics (smaller apparent signal components)
- Power of next highest spur ( $P_H$ ) - Amplitude of highest harmonic

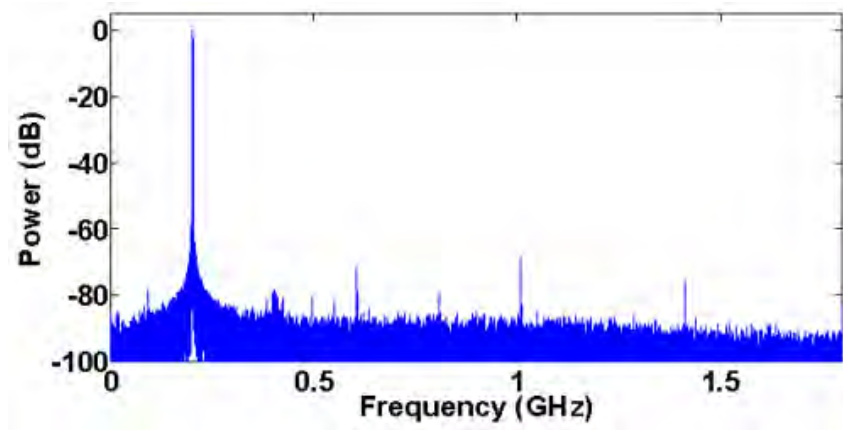


Figure 2.23: Example frequency domain for an ADC's output[35]

With this in mind, five of the most common ADC performance metrics will be explored[36, 35]:

**Signal-to-Noise Ratio (SNR)** is defined as the ratio of the signal power ( $P_S$ ) to the noise floor ( $P_N$ ) and is usually specified in decibels relative to the carrier (dBc) or decibels relative to full scale (dBFS) due to the signal's wide dynamic range.

$$SNR = 10 \log_{10} \left( \frac{P_S}{P_N} \right)$$

At the very least the SNR should be greater than 0 dBc (1:1) which means that signal power is greater than the noise power.

**Spurious Free Dynamic Range (SFDR)** is defined as the ratio of the signal power ( $P_S$ ) to the next highest spur power ( $P_H$ ) and is also specified in dBc or dBFS.

$$SFDR = 10 \log_{10} \left( \frac{P_S}{P_H} \right)$$

This is a particularly important metric as it defines the smallest signal value that can be distinguished from an interfering signal.

**Total Harmonic Distortion (THD)** is defined as the ratio of signal power ( $P_S$ ) to the power of the harmonics ( $P_D$ ) and is specified in dBc.

$$THD = 10 \log_{10} \left( \frac{P_S}{P_D} \right)$$

THD is a quality metric that describes how linear, pure and accurate the digital reconstruction of the analog signal is.

**Signal Noise and Distortion (SINAD)** is defined as the ratio of signal power to the sum of the power of the harmonics and power of the noise. It is also known as the total harmonic distortion plus noise (THD+N). The bandwidth over which the noise must be measured must be specified.

$$THD + N = 10 \log_{10} \left( \frac{P_S}{P_D + P_N} \right)$$

SINAD is equivalent to THD+N when the bandwidth for the noise measurement is  $F_S/2$ :

$$SINAD = 10 \log_{10} \left( \frac{P_S}{P_N + P_D} \right)$$

Like THD, SINAD is a quality metric that measures the degradation of a signal by unwanted spurious signals, noise and distortion. The greater the SINAD value, the better the quality of the output signal.

**Effective Number of Bits (ENOB)** specifies the actual performance of an ADC after factoring in noise sources and non-linearities and is defined as follows:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

The two numbers in the equation come from converting decibels into bits ( $20 \log_{10} 2 \approx 6.02$ ) and incorporating quantization error of an ideal ADC ( $10 \log_{10}(3/2) \approx 1.76$ ). ENOB is therefore the recalculated ADC resolution after considering the altered dynamic range (SINAD).

## 2.5 Data Processing

### 2.5.1 Graphics Processing Unit (GPU)

High-performance GPU computing, as it is known today, started with basic non-programmable 3G-graphics accelerators with a very different idea in mind. In the late 1990's these basic graphic accelerators evolved from their simple pixel-drawing functions to much more complex 3D pipelining. Subsequently, regular computer graphics cards were manufactured with highly sophisticated GPUs onboard, designed to rapidly manipulate and alter memory in a way that supports functions such as image transforms, texture mapping, translation, shading etc.

Over the last few years, however, GPUs have been further evolving to perform non-graphical processing, and so the general-purpose GPU (GPGPU) was born. By cleverly manipulating shader code, regular data could be represented as vertex or texture information and collected at a later stage in the pipeline as results. NVIDIA launched a range of PCI Express add-in boards called the Tesla which are similar to their regular graphics card except that the drivers are optimized for high-performance computing rather than 3D rendering and they do not contain any display ports. Due to the new set of Tesla drivers, the GPU can be treated like a many-core processor rather than a 3D rendering device[37, 38].

As an example, the NVIDIA Tesla K80 24 GB which ranges in price between \$ 4 000 - \$ 5 000. The K80, see Figure 2.24, boasts the following features:

- two Kepler GK210 GPUs
- 24 GB of GDDR5 RAM



Figure 2.24: The NVIDIA® Tesla® K80 GPU Accelerator[39]

- 4992 CUDA cores
- 480 GB/sec memory bandwidth
- 2.91 Tflops double precision performance with NVIDIA GPU Boost

The main difference between a CPU and a GPU is that a CPU usually consists of between one and eight cores, optimized for single instruction, single data (SISD) operations, guided by simple registers whereas a GPU consists of thousands of much smaller cores, optimized for single instruction, multiple data (SIMD) operations. Both devices are still powerful and have specific advantages for particular tasks and neither would be able to replace the other.

GPUs have not typically been used for spacecraft which could be attributed to them only recently advancing to a point where they are suitable for high performance computing. Moreover, GPUs are only suitable for tasks that can be highly parallelized, such as image processing, and they still require a lot of power ( $>20$  W). Nonetheless, these devices are still very popular in the space industry but are more commonly found in terrestrial-based systems such as satellite-imaging post processing, real-time adaptive optics for telescopes and other similar applications.

### 2.5.2 Digital Signal Processor (DSP)

DSPs are specialized microprocessors that are optimized for real-time, high-speed processing. Their particular niche is performing a large number of repetitive numeric calculations on a stream of data, representing a continuous real-world analog signal. DSP technology has played a critical role in enabling and advancing applications such as speech and audio processing, image and video processing, digital filtering etc.

Regular microcontrollers are usually simple integer math-based processors and are commonly integrated into basic embedded system applications. Although, more powerful microcontrollers may include additional features such as hardware multiplication units. DSPs, however, are suited for performance-critical roles and therefore contain special instructions such as multiply-accumulate and can be designed as integer, fixed-point or floating-point processors. Modern DSPs have a host of new features including special address generating units, Direct Memory Access (DMA), pipelining and multiple arithmetic units.



Figure 2.25: TMS320C6678 Evaluation Module[41]

A DSPs execution time is highly deterministic, therefore ensuring repeatability for a particular system. Furthermore, a DSP system can be reconfigured by re-coding the device and its algorithms rather than having to change physical hardware. Unfortunately, DSP systems do not allow for batch processing and operations must be completed within a fixed time frame[40].

Over the past two decades, the number of DSP vendors has drastically decreased with the primary survivors being Analog Devices, Texas Instruments and Microchip. An example of a modern DSP is TI’s multicore fixed- and floating-point TMS320C6678 DSP, see Figure 2.25. These devices contain eight DSPs each running at speeds of up to 1.25 GHz and cost around \$ 160 - \$ 240. They also incorporate a host of additional features such as hardware peripherals (I<sup>2</sup>C, SPI), 64 bit DDR3 interface, PCIe Gen 2 lanes and much more.

DSPs have been used in space before and specialized radiation hardened space DSPs, such as Atmel’s TSC21020F, exist. The AGILE<sup>2</sup> mission, hosted by the Italian Space Agency, consists of a small satellite observing in the gamma-ray and X-ray bands. AGILE’s payload data unit contains a TEMIC 32 bit floating-point TSC21020F Digital Signal Processor that runs the software for internal payload control, science data processing, etc. The DSP also provides the various serial interfaces required to communicate with the power supply unit, scientific subsystems and the data unit’s system bus[42].

### 2.5.3 Field Programmable Gate Array (FPGA)

An FPGA is an array of programmable digital logic blocks and is therefore, architecturally, very different from a microprocessor or GPU. The function of an FPGA is defined by how these logic blocks are connected through programmable interconnects. For example, an FPGA can be configured to be a microprocessor - referred to as a soft core. Also, FPGAs do not traditionally contain non-volatile memory and therefore, when powered off, the FPGA loses its previous configuration and must be reconfigured on the next power-up.

In addition to the programmable logic blocks, modern FPGAs may also contain dedicated memory banks, I/O banks, digital clock managers and several other peripherals and features. The term “field programmable” refers to the FPGA’s ability

<sup>2</sup>AGILE - Astrorivelatore Gamma ad Immagini LEggero

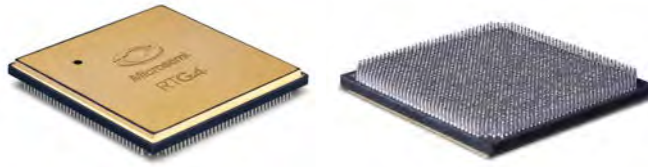


Figure 2.26: The RTG4 space-grade, radiation hardened FPGA manufactured by Microsemi[43]

to have changes made to the internal logic blocks once in the “field” making these devices perfect candidates for re-configurable computing and application specific solutions. Because of the low-level hardware nature of FPGAs, they are able to ride the Moore’s Law curve therefore increasing in complexity and performance with each new iteration.

FPGAs, however, do not generally have analog interfaces due to their digital architecture and are sequentially slower (hundreds of megahertz) than alternatives such as GPUs which run at several gigahertz. It is therefore imperative that the FPGA tasks are parallelized to make full use of the available resources. FPGAs also require more power and are more expensive (in large production runs) than Application-Specific Integrated Circuits (ASICs) and have limited internal memory.

A interesting device that has recently gained traction in the re-configurable computing community is the System-on-Chip (SoC). An SoC is a combination of an FPGA and an ARM processor on the same silicon wafer, thereby fusing two powerful technologies. These technologies are usually connected by a high-speed backbone allowing for high-bandwidth data transfers. SoCs are particularly useful as they provide the best of both worlds in terms of sequential and parallel processing, allowing for the most optimal system possible.

The use of FPGAs onboard satellites is not uncommon, particularly where signal or image processing is of importance. Space-grade, radiation hardened FPGAs are readily available from manufactures such as Xilinx and Microsemi. As an example, the RTG4 is a flash-based FPGA from Microsemi, see Figure 2.26. The RTG4 is a powerful FPGA offering in excess of 150,000 logic blocks, up to 24 3.125 Gbit/sec SERDES lanes and much more, while maintaining resistance to single event upsets in radiation environments[43].

The COVE<sup>3</sup> payload, developed by JPL which is to be flown on the University of Michigan’s M-Cubed CubeSat, is aimed at exploring the capabilities of Xilinx’s Virtex 5 in the context of enabling future CubeSat missions. The primary mission for COVE is to read and process image data collected from an onboard Omnivision camera. Although a simple mission, it achieves on-orbit validation and takes one step further in the Technology Readiness Level (TRL)[44].

#### 2.5.4 Comparison

Based on the characteristics and performance metrics, as well as the following review of literature comparing the different device types, FPGAs were deemed the most appropriate technology for this study.

<sup>3</sup>COVE - CubeSat Onboard processing Validation Experiment

#### 2.5.4.1 FPGA vs. GPU

In 2013, a Norwegian student conducted a comparison between GPU and FPGA technologies as their Master of Science in Electronics[37]. The study focused on well known image filtering techniques and their relevant implementations on each platform. For the FPGA, a ZedBoard development kit was used which has the Xilinx Zynq Z-7020 SoC fusing a dual-core ARM Cortex A9 processor with the Artix-7 FPGA. For the GPU, a CARMA development kit was used which features an NVIDIA Tegra-3 ARM Cortex A9 Quad-Core CPU and an NVIDIA Quadro 1000M GPU. The author concluded the following:

**Time:** The FPGA development was the most time consuming aspect of the project. However, it should be noted that the author used pre-compiled, ready-to-implement libraries for the GPU but developed the FPGA code from scratch.

**Performance:** The execution time for each of the architectures showed that the GPU implementation was slightly faster than that of the FPGA.

**Power Consumption:** The power consumption for the FPGA was said to be 0.69 W compared to the GPU's consumption of 9.69 W in the idle state and 19 W during benchmarking. That equates to the GPU requiring around 27 times more power.

As an addition to the study, the ZedBoard costs \$ 395 and the CARMA 529 (~\$ 590).

#### 2.5.4.2 FPGA vs. CPU vs. GPU

A similar study compared the performances of an FPGA, CPU and GPU running Basic Linear Algebra Subroutines (BLAS) using double-precision floating point[45]. To test C, the Intel Math Kernel libraries and the CUDA kernels an HP xw4600 workstation with a 3.16 GHz Intel Core 2 Duo E8500 processor was used. For the GPU evaluation an NVIDIA Tesla C1060 with 240 streaming processor cores running at 1.3 GHz was added. To test the FPGA architecture, a BEE3 platform was used which contained four Virtex-5 LX155T FPGAs

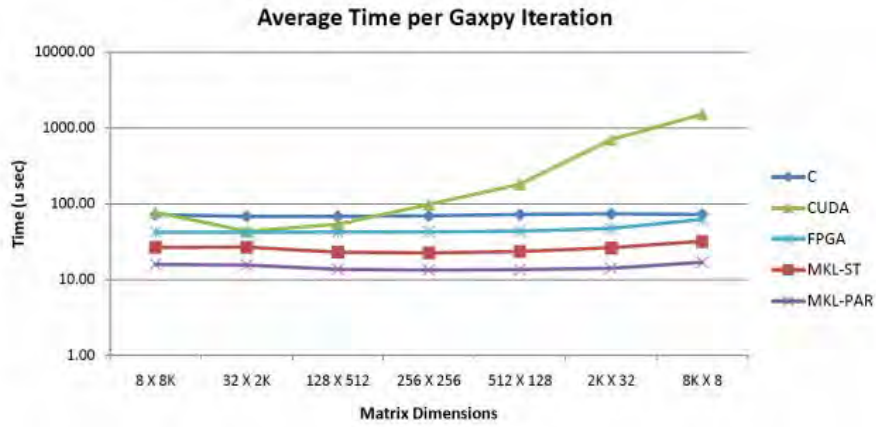
The author concluded that the FPGA offered comparable performance with up to 293 times better energy efficiency, see Figure 2.27. Additionally, the FPGA was able to provide a flexible platform that could handle a variety of matrix aspect ratios.

#### 2.5.4.3 FPGA vs. DSP

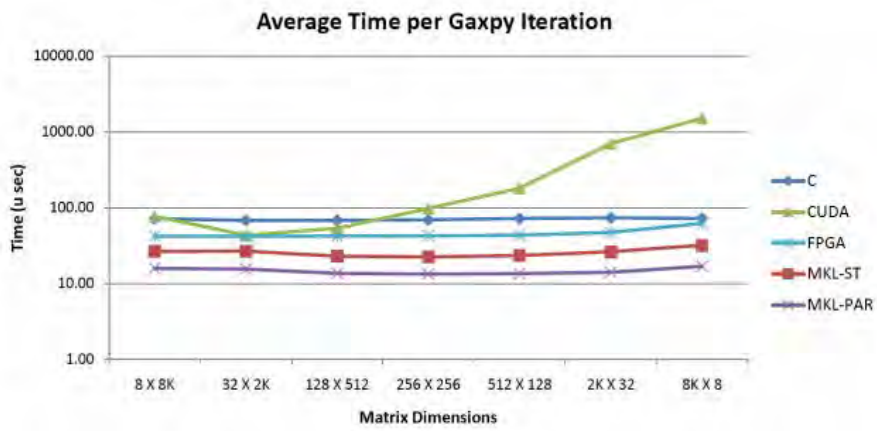
BTDi<sup>4</sup> is a Californian, U.S. based company that claims that they are "the most trusted source of analysis, advice, and engineering for embedded processor technology and applications." An article written by their staff discusses FPGAs and their role in digital signal processing[46].

The authors believe that FPGA's most significant advantage is flexibility and that this is the key to the high performance and cost effectiveness of the technology,

<sup>4</sup>BTDi - Berkeley Design Technology, Inc.



(a)



(b)

Figure 2.27: Comparison of the execution time (a) and power-consumption (b) for the Gaxpy kernel on C, MKL, CUDA BLAS and an FPGA [45]

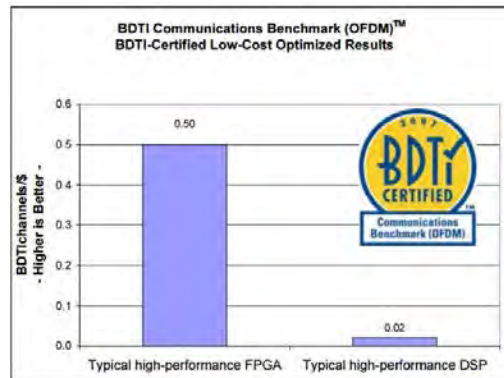


Figure 2.28: An independent benchmark comparing FPGAs and DSPs for an OFDM receiver[46]

see Figure 2.28. Furthermore, they expect FPGAs to replace ASICs and DSPs in a large number of applications and be used alongside ASICs and DSPs in many others.

## 2.6 Signal Integrity

Due to the high-speed nature of the particle detector, the interconnects between the various subsystems and modules must be carefully considered to ensure adequate signal integrity is maintained. Signal integrity refers to the quality and timing of a signal and applies to both analog and digital systems. If signal integrity is not managed correctly the relevant receiver could experience signal distortion, corruption, logic errors, data loss, false switching or even complete system failure.

Once a system has been designed and manufactured it is very difficult to detect and diagnose signal integrity issues. It is therefore recommended that every effort is made to correctly manage all sources of noise that the designer has control over. The three main sources of noise to consider are:

- Power/Ground Noise - Due to parasitics of the power and ground systems.
- Reflection Noise - Due to impedance mismatch or other discontinuities.
- Crosstalk Noise - Due to electromagnetic coupling between signal carriers.

The following discusses methods and technologies that assist in reducing the noise generated by an electronic system[47].

### 2.6.1 Low-Speed Communications

In addition to high-speed communication between components and the host processor, low-speed communications to transfer setup commands, informational messages and updates are also common in satellite systems. There are many communication protocols available for this, each with their own set of advantages and disadvantages. The following information comes directly from the author's B.Sc. Eng[18]:

**Inter-Integrated Communication (I<sup>2</sup>C)** is a bi-directional, two-wire serial bus with built-in device addressing. Devices can be connected in parallel onto the bus which consists of a serial data line (SDA) and a serial clock line (SCL). The bus generally runs at transfer speeds of 100 - 400 kHz. There is some overhead in the transmission making it more suitable for multi-slave applications but it readily supports multi-masters applications too. I<sup>2</sup>C also offers an acknowledgment mechanism to confirm receipt of data.

**Serial Peripheral Interface (SPI)** is a synchronous serial interface which is able to communicate with multiple SPI-based peripherals and is capable of full-duplex communication at relatively high data rates ( $> 10$  MHz). The SPI interface requires a serial clock line, a chip select line (if multiple slaves are present) and two serial data lines. Although having more than one master is technically possible, every SPI system is limited to one master and at least one slave at any particular point in time. The SPI bus does not have built-in device addressing and therefore requires an external line for this. It also does not offer any hardware slave acknowledgment and no error-checking protocol is defined. However, it has very little overhead and is thus more efficient for point-to-point applications.

Table 2.3: Comparison of low-speed data communication options

Interface	Format	No. of Devices	Max Length	Max Data Rate
<b>I2C</b>	Sync Serial	~20 (400 pF)	~3 m (400 pF)	400 kHz (typical)
<b>SPI</b>	Sync Serial	Infinite (GPIOs)	~5 m	>10 MHz
<b>RS485</b>	Async Serial	2 (32 with MODBUS)	~1000 m (@50 kbits/s)	10 MHz
<b>CAN</b>	Async Serial	120	~1000 m (@50 kbits/s)	1 MHz

**RS485** defines the electrical characteristics for the physical link which usually uses a differential line. It is a well-defined and well tested standard used in many systems and applications due to its robustness and reliability. The standard defines a half-duplex communication link which means that any device can communicate with any other device but only one device may transmit at a time. It is able to achieve bus speeds up to 10 Mbits/s (max dist of 12 m) and can have an unlimited amount of data per frame. In order to use RS485, nodes can be connected in parallel to achieve the typical bus topology.

**Controller Area Network (CAN)** is a serial, multi-master, multicast protocol and operates in half-duplex mode which means that when the bus is free, any node may send a message. The CAN Bus was invented in the early 1980's and was initially intended exclusively for the automotive industry. Due to its inherent features such as collision avoidance, transmission failure handling, auto-retransmission and so on, it has been used in various other applications such as in aerospace and medical equipment. CAN is typically implemented with a differential pair of twisted wires and interconnects a network of nodes.

### 2.6.2 Transmission Lines

As the wavelength of data transmission starts to approach the physical size and dimensions of components and connecting traces, the assumption that the signal magnitude and phase at the transmitter and receiver is the same is no longer valid. It is therefore necessary to introduce transmission lines, the most common of which is the planar transmission line. These lines consist of conducting metals strips that lie in parallel planes allowing for easy manufacture and lower cost.

Microstrip is the most commonly implemented form of planar transmission line consisting of a single conducting strip of width  $W$  placed on a substrate of thickness  $H$  under which lies a ground plane, see Figure 2.29a. A differential form of microstrip is known as coupled microstrip lines and is shown in Figure 2.29b. Microstrip transmission lines do not support pure Transverse Electromagnetic (TEM) waves as the dielectric does not completely surround the signal-carrying conductor(s). Instead, microstrip transmission lines support quasi-TEM waves for which the electric and magnetic fields need to be solved separately in order to determine its characteristic impedance .

As microstrip transmission line theory is well developed and understood, there is little to be gained from an in-depth analysis of how signals propagate down these

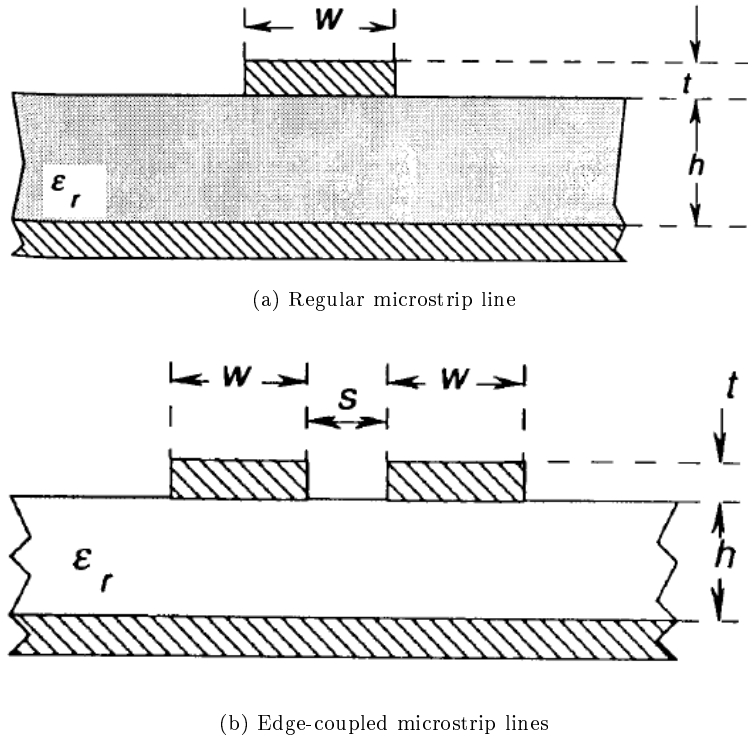


Figure 2.29: Microstrip transmission line diagrams[48]

lines. Instead, the readily available formulae can be used, the first set of which can be used to calculate the characteristic impedance of regular microstrip based on specific circuit board specifications[49, 48]:

$$Z_0 = \frac{\eta_0}{2\sqrt{2\pi}\sqrt{\varepsilon_r + 1}} \ln \left\{ 1 + \frac{4h}{w'} \left[ \frac{14 + 8/\varepsilon_r}{11} \frac{4h}{w'} + \sqrt{\left(\frac{14 + 8/\varepsilon_r}{11}\right)^2 \left(\frac{4h}{w'}\right)^2 + \frac{1 + 1/\varepsilon_r}{2} \pi^2} \right] \right\} \quad (\Omega) \quad (2.3)$$

where  $\varepsilon_r$  is the relative dielectric constant,  $w$  is the width of the trace,  $t$  is the thickness of the trace and  $h$  is the thickness of the dielectric. The equations for  $w'$  can be found in Appendix C.1.

The second set of formulae are for edge-coupled (differential) microstrip lines. These lines are constructed with two traces with the same dimensions and are referenced to the same ground plane. The odd-mode impedance is of interest as it refers to a system driven differentially, opposed to even-mode impedance where the two lines are driven with a common signal.

$$Z_{0,odd(0)} = \frac{Z_0(0) \sqrt{\frac{\varepsilon_{eff}(0)}{\varepsilon_{eff,odd}(0)}}}{1 - \frac{Z_0(0)}{\eta_0} \sqrt{\varepsilon_{eff}(0)} Q_{10}} \quad (\Omega) \quad (2.4)$$

where  $Z_0(0)$  is defined by equation 2.3,  $\varepsilon_{eff}(0)$  is defined by equation C.5 or C.6, and  $Q_{10}$  and  $\varepsilon_{eff,odd}(0)$  can be found in Appendix C.1.

	Industry Standard	Maximum Data Rate	Output Swing ( $V_{OD}$ )	Power Consumption
LVDS	TIA/EIA-644	3.125 Gbps	$\pm 350$ mV	Low
LVPECL	N/A	10+ Gbps	$\pm 800$ mV	Medium to High
CML	N/A	10+ Gbps	$\pm 800$ mV	Medium
M-LVDS	TIA/EIA-899	250 Mbps	$\pm 550$ mV	Low
B-LVDS	N/A	800 Mbps	$\pm 550$ mV	Low

Figure 2.30: Industry standards for various differential technologies[47]

### 2.6.3 High-Speed Technologies

High-speed signaling requires that special attention is paid to the communication protocol and technologies used to ensure signal integrity is maintained. Differential signaling technologies have three main advantages over their single-ended counterparts, namely:

1. Noise Immunity - As the two lines run adjacent to one another, any noise absorbed will be common to both lines and will therefore not be present at the output.
2. Low EMI Generated - The current source at the driver is always on and the MOSFETs simply “steer” current, therefore eliminating “switching noise” generated by transistors. Also, because each line is carrying the same magnitude of current but in opposite directions minimum EMI is generated.
3. Voltage Swing - Differential lines require half the voltage swing to achieve the same signal-to-noise ratio and bit error rate (BER).

Within differential signaling there are a number of technologies to choose from each with their own set of advantages and disadvantages. Due to the nature of the particle detector’s architecture, only point-to-point differential topologies need be investigated. In determining the optimal signaling technology for a particular application, there are three primary factors to consider:

1. Data Rate - The maximum data rate to be utilized during transmission.
2. Power Consumption - The power allocated for the operation of the communication link.
3. Transmission Medium - The transmission medium used for the link as well as its physical length and layout.

Three of the most commonly employed differential technologies in industry are Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) , Current-Mode Logic (CML) and Low-Voltage Differential Signaling (LVDS) . Figure 2.30 and 2.31 outlines some of the technologies’ advantages, disadvantages and trade-offs.

#### 2.6.3.1 Low-Voltage Differential Signaling (LVDS)

LVDS is one of the most power efficient differential technologies available and is capable of data rates up to 3.125 Gbps. An example of an LVDS transmitter and receiver pair can be seen in Figure 2.32a. The LVDS transmitter sinks and sources 3.5 mA of current through the differential line pair to signal a logic 0 or 1. At the LVDS receiver a differential voltage of 350 mV is generated across an external 100  $\Omega$  terminating resistor, resulting in a very low overall power consumption[47].

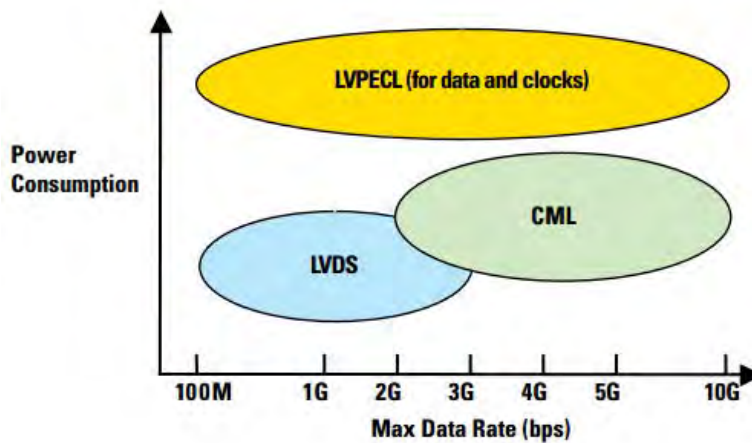


Figure 2.31: Power consumption vs. data rate for commonly employed differential technologies[47]

### 2.6.3.2 Current-Mode Logic (CML)

CML is similar to LVDS in its operation but is capable of data rates in excess of 10 Gbps. Unlike LVDS, however, CML requires termination networks at both the receiver and the transmitter, see Figure 2.32b. Furthermore, because CML is usually AC coupled, it requires that the data used is DC-balanced, that is that the bits transmitted have to, on average, have an equal number of ones and zeros to avoid charge on the receiver terminals from slowly decaying[47].

### 2.6.3.3 Low-Voltage Positive-Emitter-Coupled Logic (LVPECL)

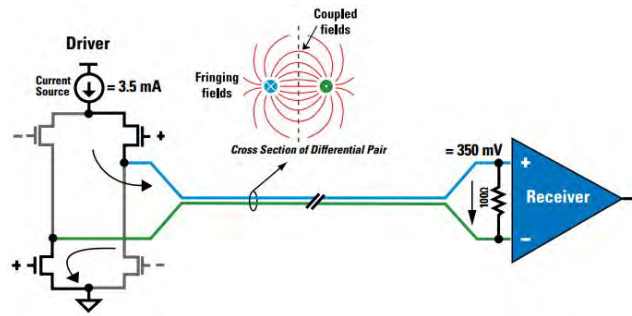
LVPECL is based on the original Emitter-Coupled Logic standard and, like CML, is also capable of data rates in excess of 10 Gbps. LVPECL has one of the highest output drive capabilities, making it ideal for longer distance communications, and it also maintains sharp and balanced edges accounting for its high-speed capabilities. This technology, however, has the highest power consumption of the three and often requires a separate termination rail for successful implementation[47]. An example of an LVPECL transmitter-receiver pair can be seen in Figure 2.32c.

## 2.6.4 Serializer/Deserializer (SerDes)

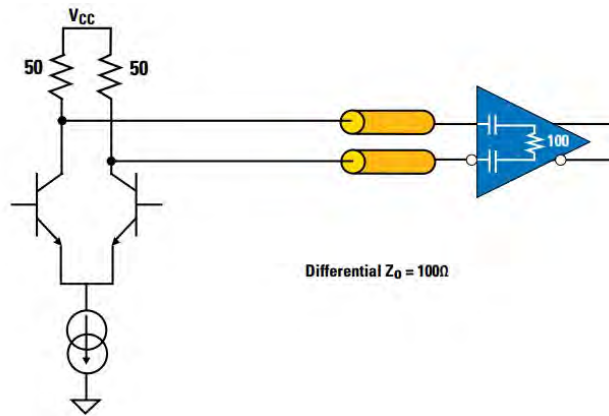
A Serializer/Deserializer, or SerDes, is a generic name for a module that converts serial data to parallel data or vice-versa. A SerDes is often used in applications where low-speed parallel TTL signals are combined into a serial stream for high-speed data transmission and then converted back to serial at the receiver.

An example of such an application would be an analog-to-digital converter that collects data in the form of multiple TTL signals (data bits) that need to be transmitted to a microprocessor or FPGA for further analysis. Similarly, an FPGA could have parallel data it needs to send to a digital-to-analog converter and could make use of SerDes modules. [47]

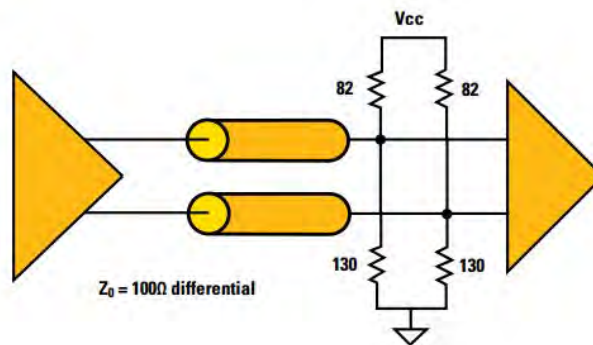
Four common SerDes standards are discussed and compared based on their respective advantages and disadvantages. A summary of the information can be found



(a) LVDS



(b) CML



(c) LVPECL

Figure 2.32: An example of a transmitter-receiver pair for various differential technologies[47]

in Table 2.4.

#### 2.6.4.1 Parallel Clock SerDes

A parallel clock SerDes is a hybrid system as it combines serial and parallel data along with a clock line. Instead of serializing an entire data word it breaks it up into a bank of  $n$ -to-1 multiplexers, each serializing its own portion and transmitting the data. In parallel to these multiplexers a clock pair is transmitted too. An example of such a system would be a set of TTL signals representing a 32 bit word. Four multiplexers could be used to represent the word, resulting in four serialized data streams and one synchronization clock.

This system is useful as it reduced the effective data rate when compared to a single data stream system. However, it requires more signal lines and since the clock and data travel on multiple different paths, the pair-to-pair skew must be minimized to meet specific timing requirements.

#### 2.6.4.2 Embedded Clock Bits SerDes

An embedded Clock SerDes transmits both the data signal and clock signal on a single line. A parallel signal is serialized onto a single serial stream which starts with a clock low, then a clock high and then the data. The receiver then monitors for the period clock that always has a rising edge transition which can be detected as the bits are constantly changing but the clock signal is always constant.

The embedded clock is useful for locking onto an unknown signal, which is particularly useful when the transmitter does not have the ability to transmit a training pattern. The system is simple as it only consists of a single line and many data width options are available. However, the baud rate is very high because of the added clock signal and lack of parallelism.

#### 2.6.4.3 8b/10b SerDes

The 8 bit to 10 bit SerDes system maps an 8 bit word (byte) to a 10 bit code, developed by IBM, and transmits on a single serial pair. The 10 bit code is specially designed to ensure DC balance (equal number of highs and lows) as well as multiple edge transitions every cycle. At the receiver, the 10 bit code can be used for synchronization due to the frequent edge transitions, after which it can re-map the codes to the original data byte.

Due to the DC balance, the system is ideal for AC-coupled applications. The system is, however, limited to 8 bits and also requires accurate clocking to lock onto the signal at the receiver.

#### 2.6.4.4 FPGA-Attach SerDes

The FPGA-Attach SerDes implements the SerDes process in two stages. The first stage combines several data bits onto multiple LVDS streams. The second stage then multiplexes these LVDS streams onto a high-speed serial channel. This architecture allows high-speed data to be transmitted with fewer data lines while reducing the EMI, noise sensitivity and power consumption of the system. This system is limited to FPGAs but because of this has enormous flexibility.

Table 2.4: SerDes type comparison[47]

Technology	Advantages	Disadvantages
Parallel Clock SerDes	Serializes wide buses Low cost Automatic transmitter/receiver sync	More pairs/wires needed Tight pair-to-pair skew requirements
Embedded Clock (Start-Stop) Bits SerDes	10-, 16-, 18- and 24-bit widths available Lock-to-random-data capability Relaxed clocking requirements	No inherent DC balance Not well suited for AC-coupled or fiber applications (except 24-bit devices)*
8b/10b SerDes	DC-balance coding Works well in AC-coupled and fiber environments Widely available	Byte-oriented Tight clocking requirements Requires comma for sync
FPGA-Attach SerDes	LVDS "parallel" interface lowers board traces, EMI, and power FPGA-friendly interface Lock to "any" data Integrated signal conditioners No external reference clock	Requires small "glue" code inside FPGA

## Chapter 3

# SiPM Boards

### 3.1 Breakout Board

The silicon photomultiplier used in this study was a Sensl's MicroFB 60035 which, depending on the bias configuration, could operate in fast mode, standard mode or a combination of the two. In order to evaluate the silicon photomultiplier, a breakout board was designed that could support all configurations.

#### 3.1.1 Bias Filter

As previously mentioned, a silicon photomultiplier's gain is directly related and highly sensitive to the applied bias voltage. For this reason it is important that an adequately stable and noise-free power supply be used. To further assist in stability and noise-rejection, the recommended generic biasing filter was implemented at the bias input on the breakout board, see Figure 3.1.

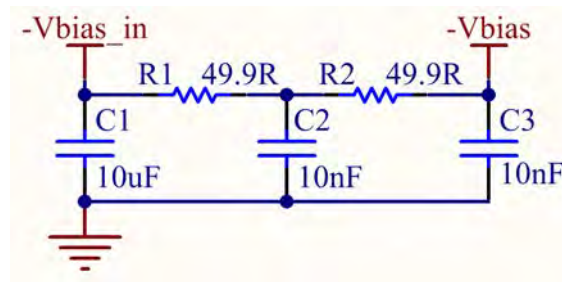


Figure 3.1: Schematic of a generic bias voltage filter

Passive filters are able to filter out unwanted frequency content generated by the original power supply or subsequent noise generated in the voltage supply line through EMI. There is no critical cut-off frequency for these power filters and therefore the absolute values are not particularly significant, however, the lower the bandwidth, the lower the resultant noise, assuming operation above the flicker noise corner frequency. The capacitors had a low ESR, relative to  $50 \Omega$ , and were placed very close to the SiPM pins to ensure that any high frequency content had a low impedance path to ground.

To ensure that there were no unwanted resonant modes due to parasitic effects, and to evaluate the attenuation factor as a function of frequency, a basic AC analysis was conducted on the filter and the silicon photomultiplier's RC model. Figure 3.2 shows the gain and phase as a function of frequency and there are evidently no unwanted resonant modes.

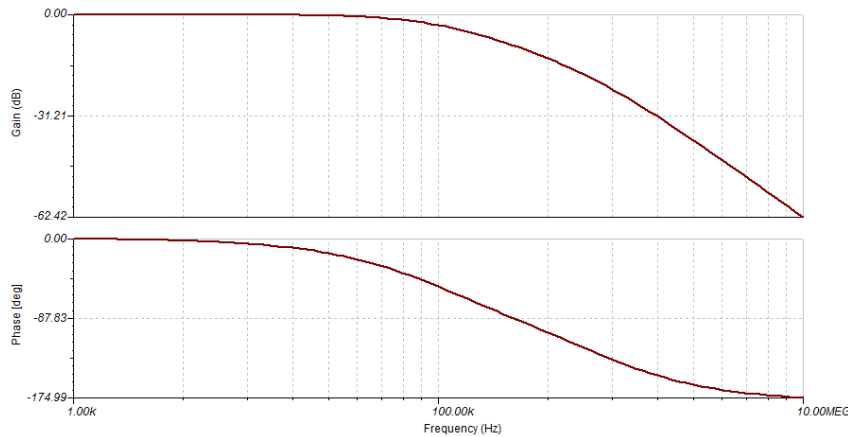


Figure 3.2: Bode plot for the proposed SiPM passive power filter

### 3.1.2 Operating Configuration

The MicroFB-60035 effectively has two outputs, both of which provide useful information. There are many different configuration options for the SiPM but, because the sensor was being evaluated, the breakout board was designed such that all configurations of interest were supported. The most likely configuration for the fast- and standard-mode outputs to be used on the final detector is shown in Figure 3.3.

#### 3.1.2.1 Fast-Mode Output

The fast-mode output has rise times as fast as 300 ps and pulse-widths as short as 600 ps which requires RF design techniques to maintain signal integrity. Furthermore, as the output is referenced to the cathode (substrate) of the photomultiplier, a negative bias voltage is applied to the anode to prevent the return current from flowing through the SiPM. With sufficient decoupling, however, a positive bias voltage should ensure equivalent performance.

The fast-mode output was AC-coupled and resulted in a positive polarity output signal. The MicroFB 60035 has a large capacitance between its anode and cathode and it was therefore not ideal to directly drive a  $50\ \Omega$  impedance transmission line. Instead, the fast-mode output was connected to a 1:1 RF balun<sup>1</sup> to improve impedance matching. Figure 3.4 shows the configuration implemented on the breakout board for the fast-mode output.

<sup>1</sup>Balun - A device that converts between a balanced signal and an unbalanced signal

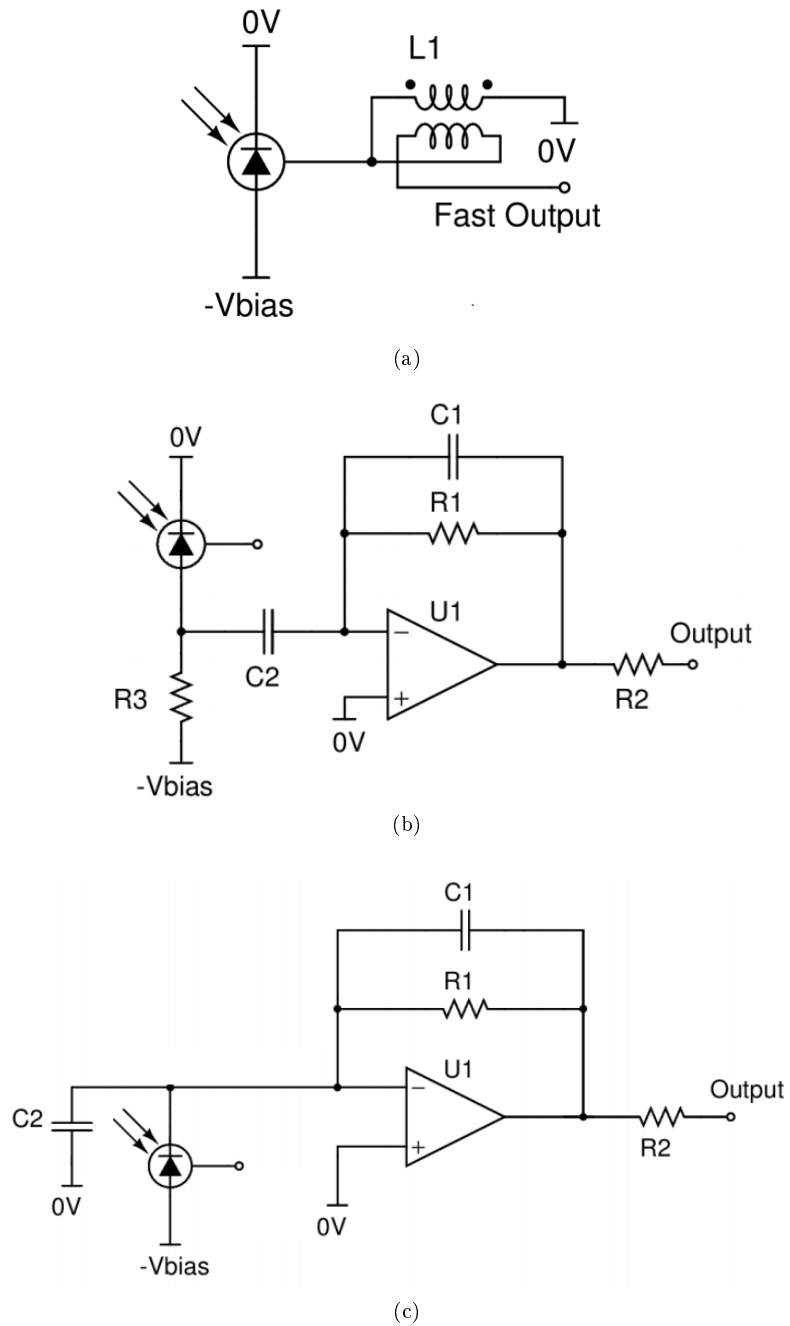


Figure 3.3: Recommended configurations for fast-mode (a) as well as standard-mode AC-coupled (b) and DC-coupled (c)[50]

### 3.1.2.2 Standard-Mode Output

The standard-mode signal was significantly slower than the fast-mode signal and optimal for low-light applications. Typical rise times for the standard-mode output are between 1 - 10 ns with a decay time of several hundred nanoseconds. Although this is significantly slower than the fast-mode output, care was still taken during the PCB routing process to maintain signal integrity.

Two configurations for the standard-mode output are shown in Figure 3.3, each with their own advantages. DC-coupling is ideal for slow-varying signals where the absolute value of the signal at any given time is of importance. AC-coupling, however, is ideal for obtaining faster pulse-like signals allowing for the DC offset to be removed and reducing the likelihood of signal saturation. Considering the fact that the detector is concerned primarily with pulse-like signals, the default option populated on the breakout board is the AC-coupled configuration, see Figure 3.4.

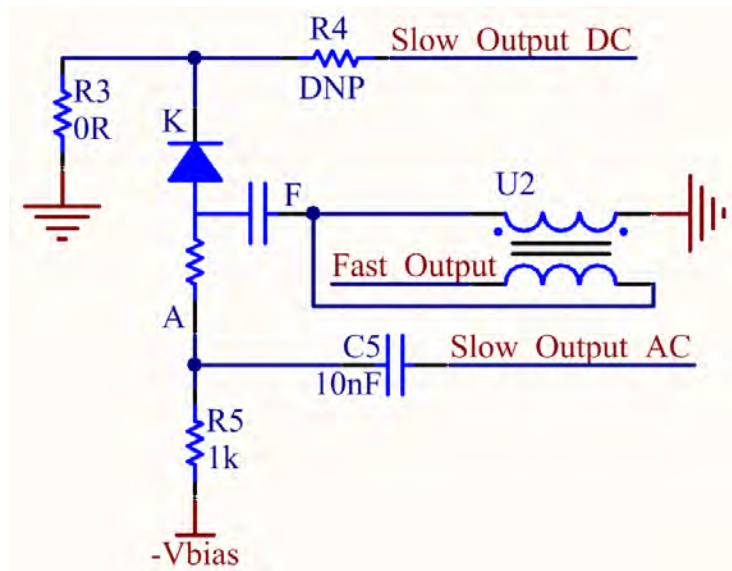


Figure 3.4: Schematic of SiPM's output configuration

### 3.1.3 Breakout Connections

The SiPM's outputs had to be matched to  $50 \Omega$  and therefore required the correct RF routing and connectors. Small RF connectors are notoriously fragile and known to shear off circuit boards. Given the number of insertions associated with testing and evaluation, a more robust connector was necessary.

A micro coaxial connector (MCX) was found to be ideal for this particular application. MCX connectors are smaller than SMA and SMB connectors, are available with a  $50 \Omega$  impedance and can operate up to 6 GHz with less than 0.2 dB insertion loss. They are rated up to 250 V RMS, have an isolation resistance of greater than  $1 \text{ G}\Omega$  and a contact resistance of less than  $5 \text{ m}\Omega$ . Furthermore, they comply to MIL-STD-202 for corrosion, thermal shock, vibration, mechanical shock and temperature[51].

### 3.1.4 PCB Layout

The SiPM's inputs and outputs were matched to a  $50\ \Omega$  characteristic impedance and therefore all traces were designed accordingly. Small (0402) surface mount components were used, because they are physically small relative to the anticipated signal wavelengths, and ground stitching was implemented along the four I/O lines to ensure that none of the copper acted as a stub. The majority of the copper on the top and bottom layer was ground pour to minimize EMI and crosstalk as well as to provide a low inductance ground path for all the components.

All bypass capacitors and termination resistors were placed as close to the photomultiplier as possible, however, sufficient space had to be left for the scintillating material to mate on top of the device. Four mounting holes were added, far away from sensitive signals, that could be used to mount the breakout board in an enclosure or to attach it to a thermoelectric cooler (TEC).

The  $7 \times 7\ \text{mm}^2$  MicroFB 60035 SiPM has solder pads that are located under the glass-like housing, requiring the device to be soldered in a reflow oven. Details of the reflow process and testing can be found in Appendix B.4. As the device was ESD sensitive, the necessary precautions were taken during the assembly process. A 2D and 3D model of the circuit board can be seen in Figure 3.5.

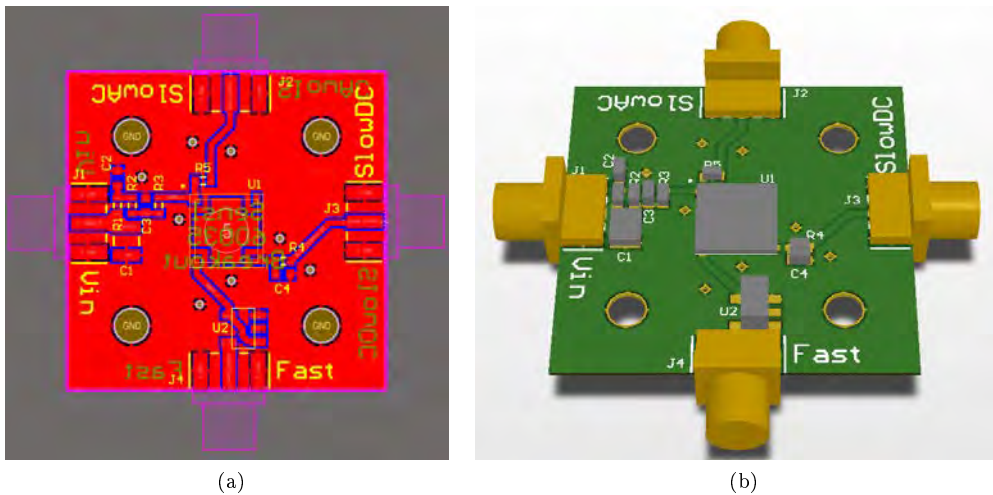


Figure 3.5: A 2D (a) and 3D (b) view of the final SiPM breakout PCB model

## 3.2 SiPM Power Supply

Although SiPMs were determined to be the most suitable technology for the proposed detector, they are silicon-based devices and are therefore affected by temperature variations. Furthermore, no two SiPMs have exactly the same specifications, such as breakdown voltage. This poses potential problems when trying to create an array of “identical” SiPMs.

To overcome these issues, a dynamically adjustable power supply was developed that allowed for the compensation of unwanted temperature variations, thereby keeping performance parameters, such as gain, constant. Each SiPM had its own adjustable power supply, therefore allowing individual bias voltage trimming to ensure equivalent performance.

### 3.2.1 Specifications and Requirements

The MicroFB 60035 SiPM has a breakdown voltage between 24 - 25 V (nominally 24.5 V) and an overvoltage range of 1 - 5 V. The power supply therefore requires an adjustable voltage over the range of 24 - 30 V. Because the SiPM requires a reverse bias at the cathode, the output voltage has to be negative with respect to ground. Furthermore, the maximum output current required for the MicroFB 60035 is 20 mA per SiPM tile. Accuracy and repeatability were important to ensure that subsequent SiPM testing was done under the same conditions, particularly during the characterization phase of the project.

Due to the highly dependent and sensitive relationship between gain and overvoltage, see Figure 3.6, the voltage ripple and noise has to be kept to a minimum. Moreover, the SiPMs power supply has to have excellent load regulation to ensure a steady bias voltage during the small current bursts as a result of particle events.

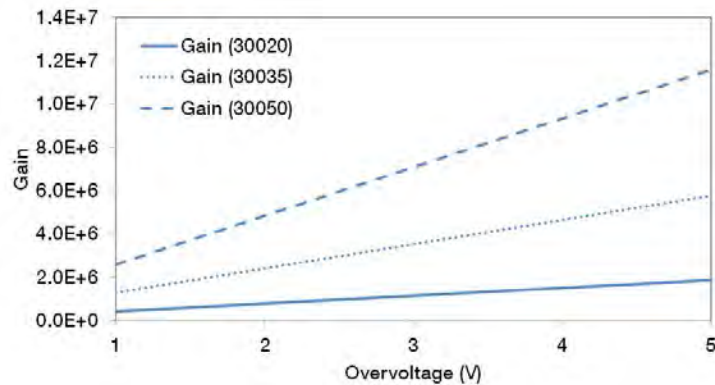


Figure 3.6: Gain vs overvoltage for the Sensl’s MicroFB SiPMs[52]

### 3.2.2 Circuit Design

A high-level block diagram of the SiPM power supply is shown in Figure 3.7. The circuit begins with a switch-mode power supply converting a readily available pos-

itive voltage into a larger negative voltage. A low-noise low-dropout linear regulator is used for post regulation due to the inherently noisy nature of switch-mode converters. Finally, a current-mode DAC is used to inject current into the linear regulator's voltage-setting resistor divider to allow for a digitally adjustable output.

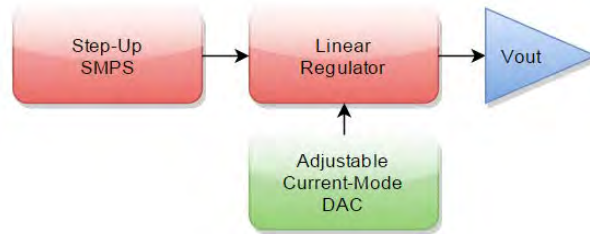


Figure 3.7: Block diagram of digitally-adjustable SiPM power supply

### 3.2.2.1 Switch-Mode Regulator

Linear Technology's LT3579 switching regulator is used to convert the low input voltage (5 V) to a large negative voltage (-33 V). The LT3579 accepts a wide voltage input range of 2.5 - 16 V and contains a 6 A power switch, allowing for a number of switching topologies. By slightly modifying the regulator's recommended SEPIC topology, an inverting converter was realized. The converter also offers a host of additional useful features such as a configurable voltage lockout, optional synchronization, shutdown pins, over-current shutdown etc.[53]. Detailed component value calculations can be found in Appendix C.2.

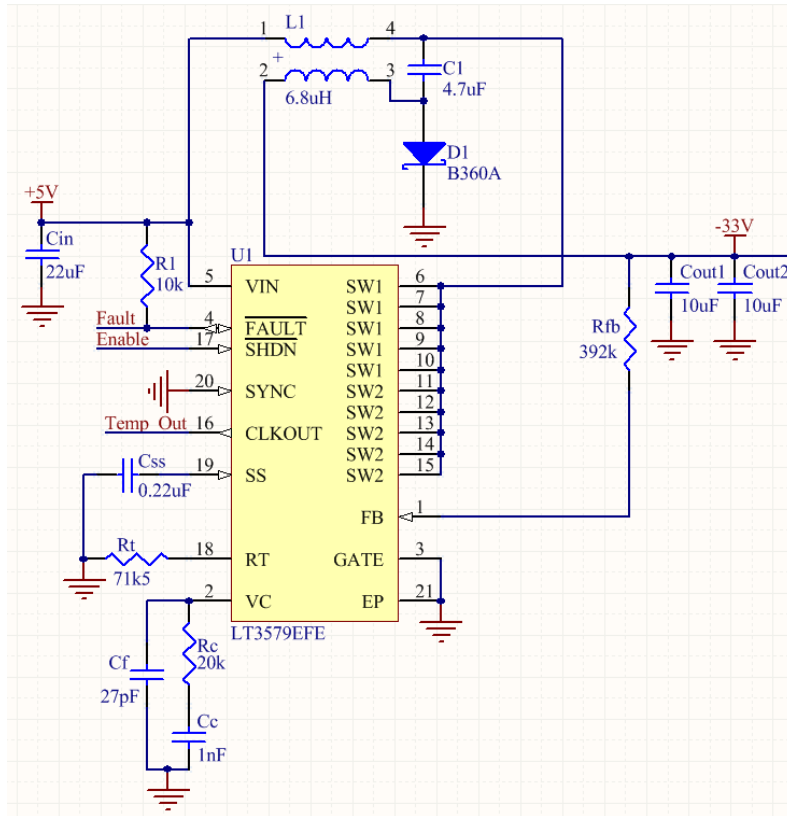


Figure 3.8: Circuit diagram of the SiPM power supply's switch-mode converter

### 3.2.2.2 Linear Regulator

After the -33 V output was generated by the switching regulator it was then passed through an ultralow-noise linear voltage regulator from Texas Instruments. The TPS7A33 regulator is capable of a 1 A output current, has a noise specification of  $16 \mu V_{RMS}$  and a power-supply rejection ratio (PSRR) of 72 dB, making it an ideal candidate as a post-SMPS conditioner. Furthermore, the regulator has built in current-limiting and thermal shutdown protection. Figure 3.9 shows the final circuit diagram for the linear regulation.

Ceramic capacitors with X7R dielectrics are used at the input and output of the regulator due to their low ESR and relatively good over-temperature performance. To ensure stability under all load conditions, as well as to maximize AC performance,  $50 \mu F$  of capacitance was placed at the output with a voltage rating in excess of 35 V. A noise-reduction capacitor, C3, was placed on the NR pin to minimize noise and to improve the regulator's AC performance, while simultaneously providing soft-start functionality to slowly increase the output voltage at startup. Finally, a feed-forward capacitor, C4, was added at the output for noise and stability reasons.

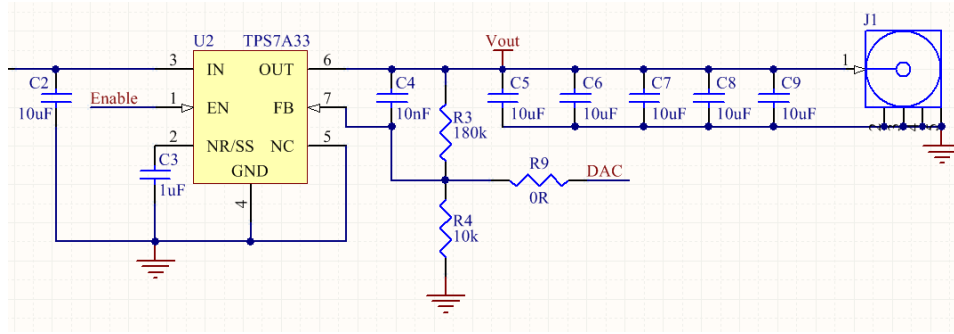


Figure 3.9: Circuit diagram of the SiPM power supply's linear regulator

### 3.2.2.3 Current-Mode DAC

To implement a dynamically adjustable voltage output, Linear Technology's 10-bit LTC1427-50 current-output DAC is used to inject current into the linear regulator's voltage-setting resistor divider. The DAC has an I<sup>2</sup>C serial interface to control the current output from 0 to 50  $\mu$ A. A detailed operational description can be found in Appendix C.2.

The circuit diagram for the current-output DAC can be seen in Figure 3.10. Connecting the AD0 and AD1 pins to +5 V set the I<sup>2</sup>C address but, more importantly, it sets the startup current output to 25  $\mu$ A, as opposed to 50  $\mu$ A. The lower current is preferred as it results in a lower default overvoltage being applied to the silicon photomultiplier.

The DAC only requires a single bypass capacitor, C10, at the power input and a short trace to the current injection point, to reduce noise. During regular operation the DAC consumed 115  $\mu$ A and can be shut down into a low power state, where it retains the DAC contents, and reduces current consumption down to 10  $\mu$ A.

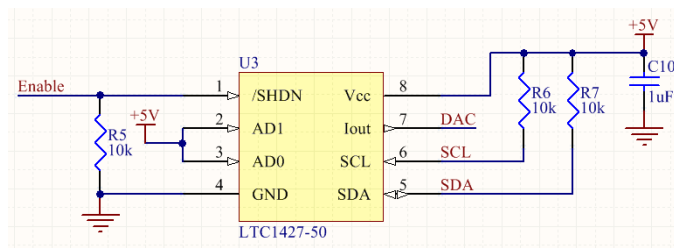


Figure 3.10: Circuit diagram of the SiPM power supply's current-mode DAC

### 3.2.2.4 Power Supply I/Os

The SiPM power supply has a breakout header to connect to an external power source and controller. Power is supplied via pin 6 (+5 V) and pin 5 (ground). An additional ground pin is available, pin 1, in case the main power supply is isolated

from the I<sup>2</sup>C controller. The remaining pins, and their functions, are described below:

Temp_Out	Output representative of the SMPS's junction temperature
Fault	Active-low fault output for the switching regulator
Enable	Active high input for the switching regulator, linear regulator and DAC
SCL	I <sup>2</sup> C clock line
SDA	I <sup>2</sup> C data line

### 3.2.2.5 PCB Design

The SiPM power supply was implemented on a small, double-layer circuit board, shown in Figure 3.11. During the layout for the SMPS the following actions were taken to ensure optimal performance:

- The power bypass capacitors were placed as close to the IC as possible and the inductor bypass capacitor was placed as close to the inductor as possible.
- The analog signal traces and filter components were placed as close to the IC as possible while keeping them as far away from any switching components and pins as possible.
- The top and bottom copper layers contain a large ground plane around the IC to prevent switching noise from propagating into the rest of the circuitry. For the same reasons, the high-speed switching traces were kept as short and direct as possible.
- The top ground plane and the exposed pad of the IC were connected to the bottom ground plane with multiple vias. This was done to ensure a uniform ground potential as well as to assist with heat dissipation.
- Finally, the ground paths from the switching circuitry were kept separate from all other analog grounding and were only joined at the exposed thermal ground pad of the IC. This was done to minimize the amount of switching noise coupled into the output and surrounding circuitry.

Similarly, during the layout for the linear regulator, a ground plane was placed on both layers around the linear regulator IC to suppress noise and to prevent it from coupling into nearby circuitry. The bypass and noise-reduction capacitors were chosen to have a low ESL and ESR and were placed as close to the device as possible to ensure stability and optimal AC performance.

There was very little to consider for the current-mode DAC apart from placing the bypass capacitor close to the IC and keeping the trace from the DAC to the resistor divider as short as possible.

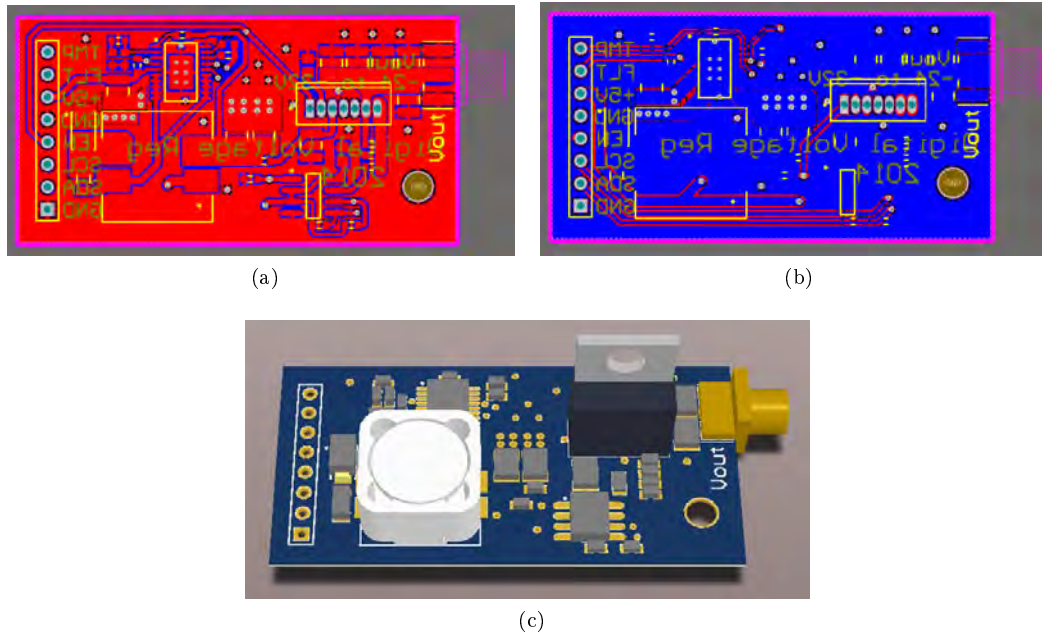


Figure 3.11: A top (a) and bottom (b) 2D and 3D (c) view of the basic SiPM power supply model

### 3.3 Integrated SiPM Power Supply

After the SiPM power supply was shown to demonstrate good performance, a new version was designed that incorporated a microcontroller, allowing the supply to act as a standalone solution. Furthermore, the new design could be connected to a computer via a mini USB connector to run user profiles in real-time. An overview of the new design can be seen in Figure 3.12.

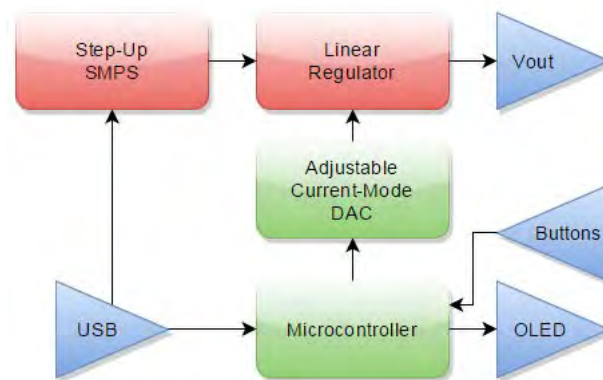


Figure 3.12: Block diagram of the integrated digitally-adjustable SiPM power supply

For simplicity, the system is powered via the same USB connector used for data transfer between the circuit board and a remote computer. The USB input voltage is filtered with a PI-type circuit containing bypass capacitors and a ferrite bead

to ensure a clean, low noise supply voltage, see Figure 3.13. The circuit's overall operating principle is identical to that of the previously discussed power supply.

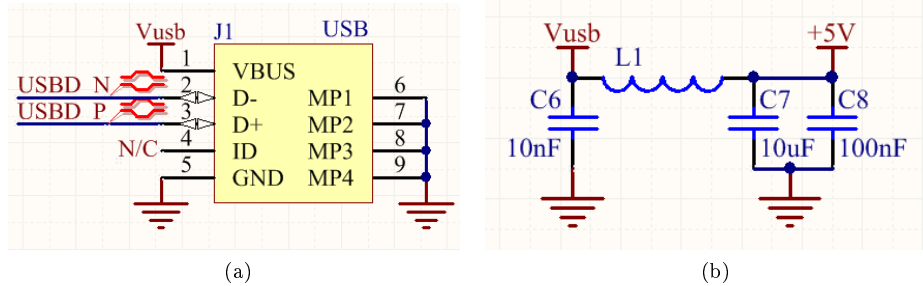


Figure 3.13: Schematic of the power supply's USB connector (a) and power filter (b)

A high-performance, 8-bit Atmel ATmega168 is used as the central controller, see Figure 3.14. The device has a number of desirable features such as an extended RISC instruction set, low operating current ( $250 \mu\text{A}$ ) and even lower power-down current ( $0.1 \mu\text{A}$ ). However, the primary reason for selecting this particular microcontroller was because it supports the Arduino bootloader which makes customizing firmware significantly simpler for a user who is not versed in low-level microcontroller programming.

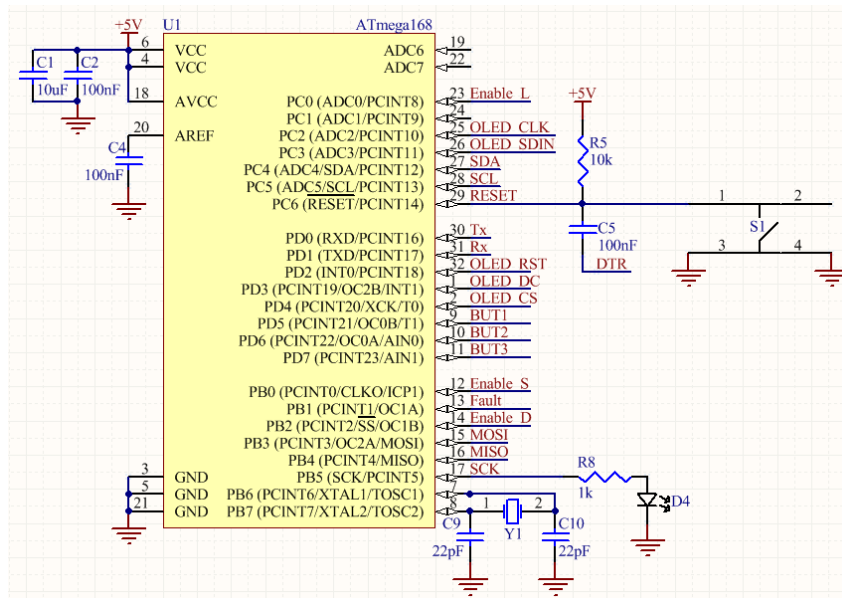


Figure 3.14: Schematic of the ATmega168 microcontroller

Connected to the microcontroller as supporting peripherals are a USB-to-UART converter, three user-programmable push-buttons, an in-circuit serial programming (ICSP) header and an OLED display. The ICSP header is required for uploading

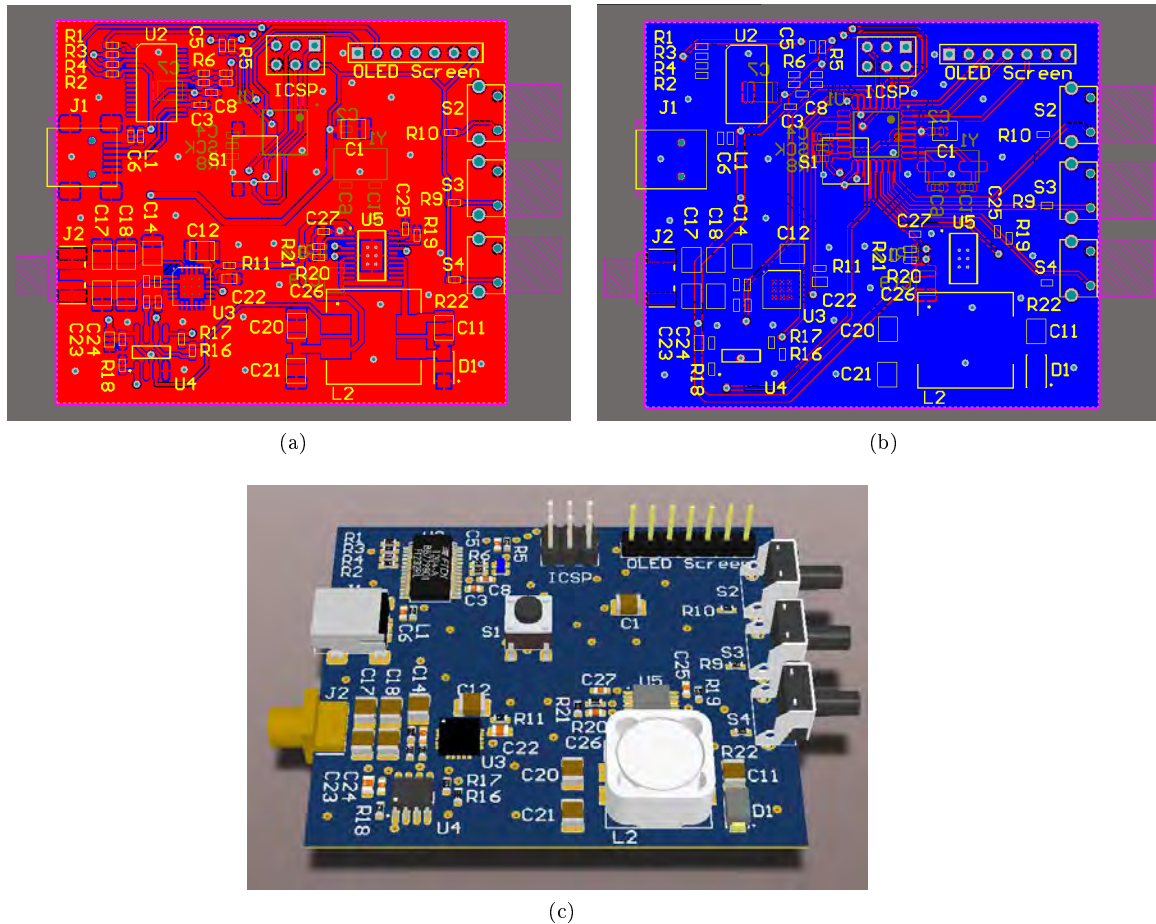


Figure 3.15: The 2D top (a), bottom (b) and 3D (c) view of the fully-integrated SiPM power supply

the Arduino bootloader or program memory onto the microcontroller and the USB-to-UART converter allows for the power supply to be connected to a computer.

The new PCB is larger (50 x 60 mm) than the original power supply because of the additional components and features, see Figure 3.15. With the exception of the voltage generation and regulation layout, discussed previously, the board layout process was simple and did not require any special techniques to optimize performance due to the slow, digital nature of the signals.

### 3.4 High-Voltage Controller

In addition to the silicon photomultiplier power supplies, a high-voltage (HV) power supply controller was designed, manufactured and tested for vacuum tube photomultipliers. Vacuum tube photomultipliers have been used for high energy physics experiments for many decades and therefore serve as an excellent benchmark. UCT's physics department already had an extremely stable, low-noise ORTEC high voltage power supply but unfortunately it lacked a digitally adjustable output.

The ORTEC 556 High Voltage Power Supply, see Figure 3.16, can supply a positive or negative voltage ranging from 0 - 3000 V at a current of 0 - 10 mA. The power supply is housed in a standard double-width NIM module<sup>2</sup> and its output can be programmed via an external controller. It also offers excellent regulation with less than 0.0025 % of variation and 50 ppm/°C of temperature instability. The supply was specifically designed for the biasing of photomultiplier tubes, ionization chambers, and semiconductor detectors.



Figure 3.16: Image of an ORTEC Model 556 high voltage power supply

An external controller was designed to digitally adjust the high voltage power supply via the rear-mounted BNC input plug. Considering that many high energy physics experiments require two vacuum photomultipliers, a dual channel controller was designed. The HV controller uses the same microcontroller and USB power system as the integrated SiPM voltage supply.

### 3.4.1 Digital-to-Analog Converter

To control the ORTEC power supply, an analog control voltage has to be applied to the supply's "External Control" BNC connector. The full voltage range of 0 - 3000 V can be swept through with a control voltage ranging from 0 to 6.9 V. To activate the external control, the "Ext" switch has to be toggled, disabling the front panel controls.

To set a positive voltage, the polarity switch has to be switched to the "Pos" position and a positive voltage (0 -> 6.9 V) applied to the external control pin. Conversely, for a negative voltage, the "Neg" position has to be selected with the polarity switch and a negative voltage (-6.9 -> 0 V) has to be applied to the external control pin.

To generate two stable and precise analog voltages, TI's DAC8563 16-bit, dual-channel, voltage-output DAC was used. The DAC offers  $\pm 5$  mV initial accuracy, 4 ppm/°C temperature drift and can sink or source up to 20 mA. The power supply

<sup>2</sup>The Nuclear Instrumentation Module (NIM) standard defines mechanical and electrical specifications for electronics modules used in experimental particle and nuclear physics[Wikipedia].

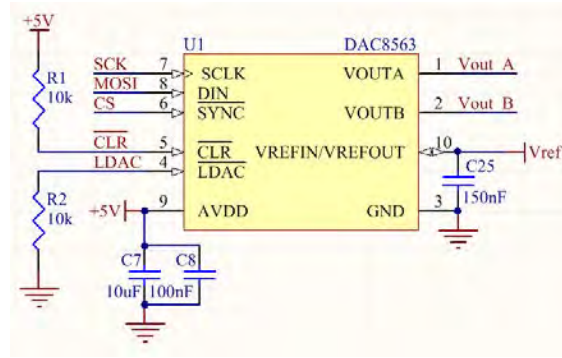


Figure 3.17: Schematic of the dual-channel DAC used to control the HV controller's outputs

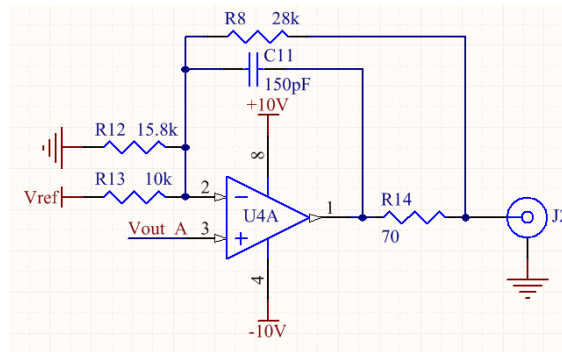


Figure 3.18: Circuit diagram of the unipolar to bipolar converter

pin requires basic decoupling capacitors and a 150 nF noise filtering capacitor for the reference output. The final schematic can be seen in Figure 3.17 and more details can be found in Appendix C.3.

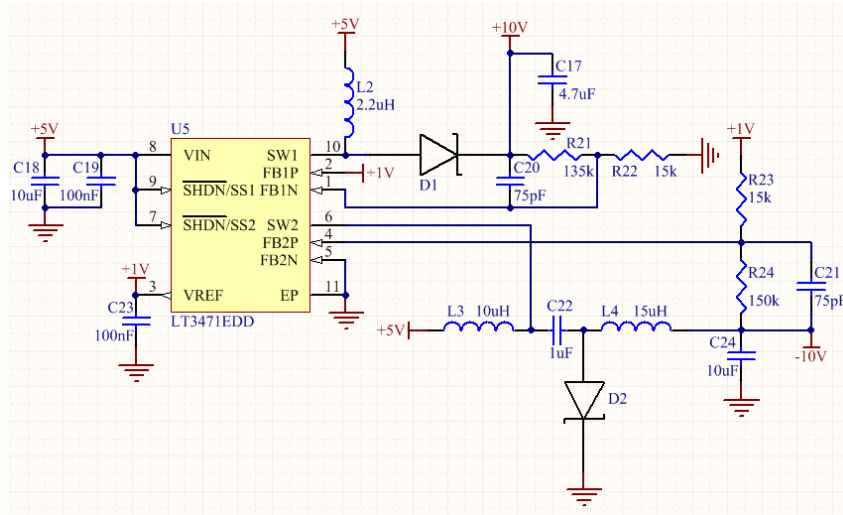
### 3.4.2 Unipolar-to-Bipolar Converter

The DAC's desired output range is -6.9 to 6.9 V. Consequently, TI's dual-output, rail-to-rail OPA2188 opamp is used to convert the USB's unipolar voltage to a bipolar voltage, see Figure 3.18. The OPA2188 has a low offset voltage, zero-drift, low noise and high DC precision. More details are available in Appendix C.3.

With the bipolar conversion, the DAC achieves a resultant resolution of 92 mV over the full voltage range of -3000 to 3000 V. The DAC was specifically chosen to set the output to mid-scale at power-on to ensure that the output voltage is 0 V by default (0 V is in the center of the bipolar output range).

### 3.4.3 Power Rails

The circuit design requires 5 V, 10 V and -10 V to operate. In the interest of keeping the system as simple as possible the USB power is used as the 5 V supply. The  $\pm 10$  V rails are generated using the LT3471 dual switching regulator from

Figure 3.19: Circuit diagram of the  $\pm 10$  V power supply

Linear Technology. The relevant calculations for the power converter can be found in Appendix C.3.

A Schottky diode with a voltage rating of 20 V and a forward current rating of 0.5 A is used for components D1 and D2, keeping the physical size small while still maintaining sufficient current carrying capability. Low ESR bypass capacitors were added to the input, reference output and final voltage outputs. The remainder of the components, and specifically the inductors, were chosen based on recommended values in the datasheet and tested through simulation, see File “LT3471\_Bipolar\_ - Supply.asc”.

### 3.5 PCB Design

The circuit board layout process was very simple as there were only three new subsystems added since the previous silicon photomultiplier power supply, namely the bipolar voltage regulation, dual-output DAC and opamp buffers. A 2D and 3D model of the circuit board can be seen in Figure 3.20.

Both the DAC and opamp have reasonably simple layouts due to the low-speed nature of the design. However, because these two circuits were concerned with distributing and amplifying analog signals, care was taken to keep the signals away from the high-speed switching circuitry of the regulator as well as the data and clock lines near the microcontroller.

The switching regulator, operating at 1.2 MHz, required more attention. Separate ground return paths were used for all the high current paths and these were joined at the exposed ground pad of the regulator. Moreover, the high-current switching traces were kept as short as possible and away from any sensitive analog circuitry.

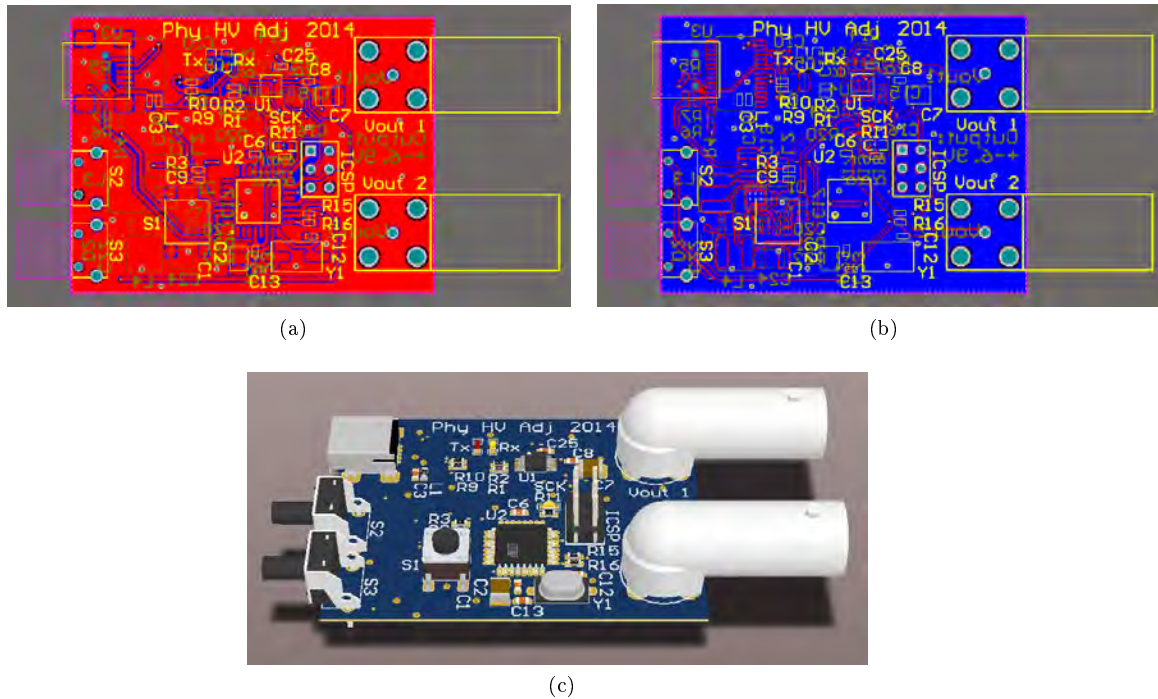


Figure 3.20: A 2D top (a), bottom (b) and 3D (c) view of the HV controller

### 3.6 Light Box

The SiPM has to detect light down to single-photon levels and therefore requires that all other light sources be removed during experiments. Consequently, a light box was built from laser-cut MDF wood in which these experiments could be placed, see Figure 3.21. To support comparison tests, the box was made large enough to house a variety of physics experiments, rather than just for the SiPM and its scintillator.

The interior of the box was painted with a matte black paint to reduce reflections and all joining surfaces were coated with a thick, black silicon paste to block any light from entering. The box's lid has side walls, lined with black optical foam, to create a light-proof seal. The two holes, visible in Figure 3.21, are present on three sides of the box and housed high voltage, panel-mount BNC connectors. This provides the components inside the box access to power sources, oscilloscopes etc. while keeping the box light-tight.

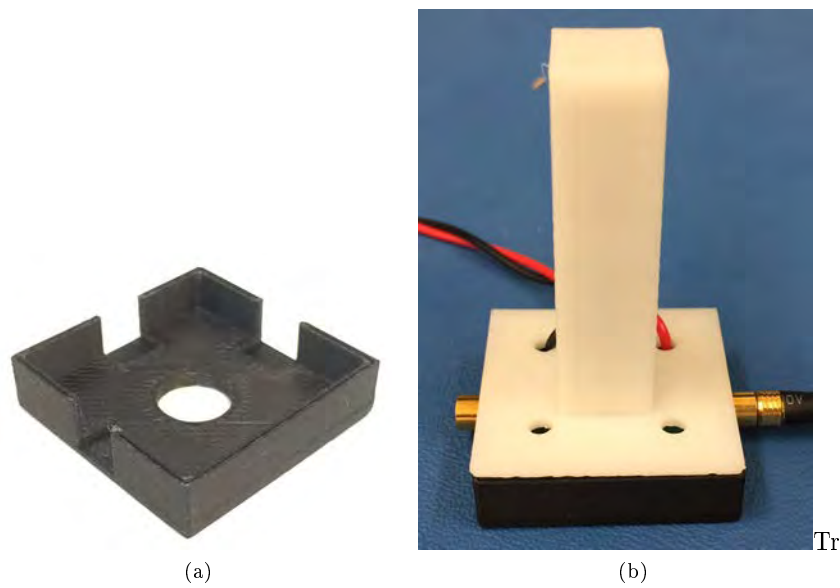


Figure 3.22: 3D printed SiPM holder base (a) and full setup (b)



Figure 3.21: A SolidWorks model of the light box

### 3.7 SiPM Holder

To test the silicon photomultiplier, without the need for the bulky light box and its supporting equipment, UCT's physics department designed a small 3D-printed enclosure that could house the silicon photomultiplier breakout board and the scintillating material. The design consists of two parts and ensures that the scintillator mates optimally with the photomultiplier when assembled. The breakout board's MCX connectors are accessible to provide power and access to the signal outputs.

## Chapter 4

# Circuit Design

Based on the research conducted in the Literature Review, and the preliminary results obtained and documented in Appendix B, a high-level block diagram for the envisioned particle detector was created, see Figure 4.1.

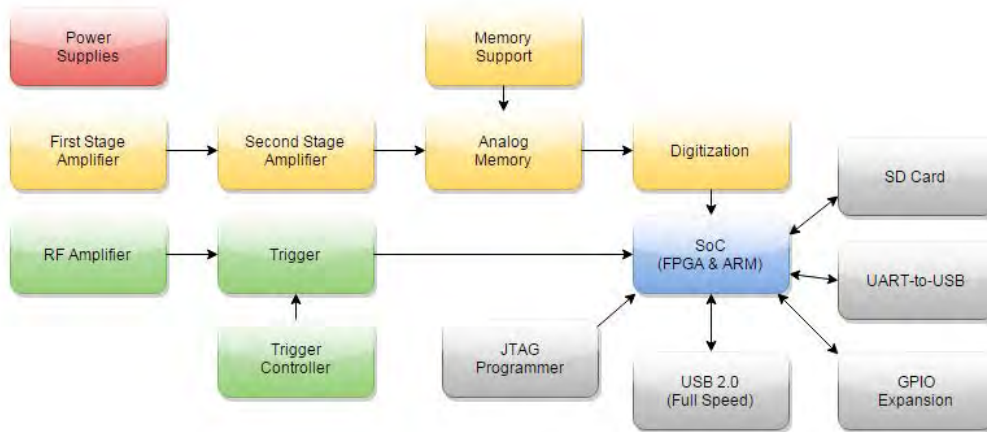


Figure 4.1: Block diagram of overall detector hardware

The yellow and green blocks represent the two signal paths, each consisting of 9 channels, both of which feed into the SoC for further processing. The yellow path amplifies and digitizes the SiPMs' standard outputs and the green signal amplifies and determines a trigger state from the SiPMs' fast outputs. The gray blocks indicate support hardware that could possibly be omitted in a final application.

The following sections describe the various aspects of the block diagram and how each individual block contributes to the overall particle detector.

### 4.1 Power Supplies

The detector requires various voltage sources for all the different components used. Furthermore, some of the supplies are to be enabled/disabled via the FPGA and some have to be isolated from others to avoid noise coupling into sensitive circuitry.

In the interest of keeping the detector portable, the system was designed to accept one input voltage and then generate all the necessary voltages onboard, see Figure 4.2.

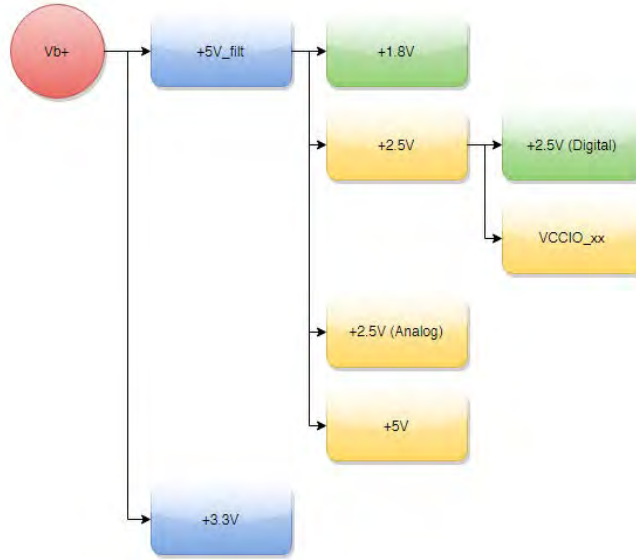


Figure 4.2: Block diagram of overall power routing and distribution

#### 4.1.1 Input and Protection

The power regulation stages were designed for use with a single set of lithium-ion batteries. Two parallel sets of two series lithium-ion cells (four cells in total) were combined to generate a nominal voltage of 7.4 - 8.4 V. The combination of the 2800 mAh, 18650 form-factor cells (LG's LC-18650-28LG), is able to supply over 10 A for an hour and was housed in a protected battery holder (#2S2P-18650) that manages overcharging, discharging, over draining and short circuits.

The input power jack was chosen to support the maximum input voltage and current with the smallest contact resistance. Considering that the detector is to operate in the space environment, as well as undergo vibration testing, the connector (Cui Inc PJ-002BH) was chosen based on its terminal strength and its number of rated operational cycles.

An N-channel MOSFET was used at the input of the detector to protect it against reverse polarity during testing and final implementation, see Figure 4.3. The MOSFET was chosen to have a very low on-resistance ( $R_{DS(on)} = 1 \text{ m}\Omega$ ) and continuous drain current ( $I_D = 100 \text{ A}$ ) so that it will have a negligible effect on the circuit during regular operation. When a reverse voltage is present, the MOSFET will not turn on, thereby blocking any current from entering, and potentially damaging, the circuit.

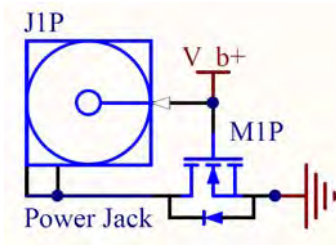


Figure 4.3: Schematic of the input power jack and reverse polarity protection

#### 4.1.2 1.8 V Supply

The ADCs require a 1.8 V analog and digital power supply and consume a combined maximum input current of 120 mA per ADC. Considering the large current requirement for powering five ADCs, a high efficiency step-down switching regulator is used to generate the 1.8 V output voltage, see Figure 4.4. The component values were chosen based on an application circuit from the regulator’s datasheet.

The TPS62293 converter has an enable pin and mode control pin which is connected directly to the FPGA. The enable pin is pulled down with a 100 k $\Omega$  resistor to disable the converter by default. The mode pin allows switching the converter between forced PWM mode and power save mode. This pin is also pulled down with a 100 k $\Omega$  resistor, resulting in a default power saving mode.

Although the ADCs are not as susceptible to noise as the preceding amplification stages, the output of the switching regulator is filtered with a PI-type filter and a ferrite bead. It should be noted that most of the voltage regulator designs incorporate a “Do Not Place” (DNP) resistor in series with its output. This resistor was added to allow testing of the regulators before the sensitive electronics were powered.

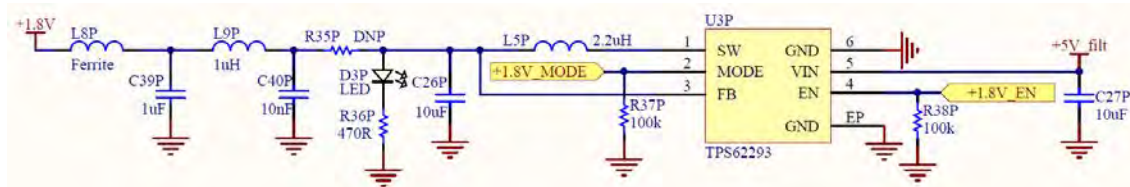


Figure 4.4: Schematic of the 1.8 V step-down, switching regulator

#### 4.1.3 2.5 V Supply

At startup, the FPGA I/O banks require a 2.5 V power supply. A permanently-enabled, low-dropout linear regulator with post-filtering is used to satisfy this requirement, see Figure 4.5. The common resistor divider formula was used to calculate the values of the voltage-setting resistors.

The TPS7A3701 offers an ultra low dropout voltage (200 mV at 1 A), excellent load transient response, excellent accuracy (0.23 %) and very low output noise (27  $\mu\text{V}$ ). Moreover, it has built-in reverse current protection and consumes less than 20 nA in shutdown mode, making it ideal for the application.

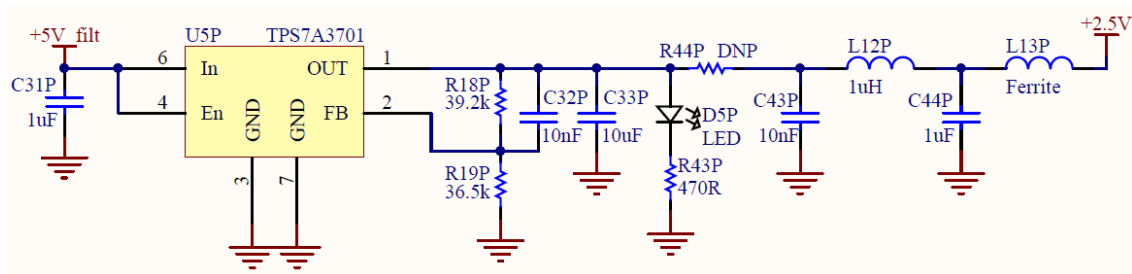


Figure 4.5: Schematic of the 2.5 V step-down, switching regulator

#### 4.1.3.1 Digital Supply

The trigger reference level translation circuitry, supporting the DRS4 DACs and the digital portion of the DRS4 was to be powered from the same “digital” 2.5 V power line but requires an enable line to allow for these components to be disabled when not in use. For this reason a low on-resistance (5.3  $m\Omega$ ), integrated load switch was added between the power line and these components, see Figure 4.6. A 100 k $\Omega$  resistor, R47P, is used to disable the output switch by default.

The load switch can operate with a continuous current of 4 A and has slew-rate control to avoid high inrush currents. Furthermore, it incorporates a built-in discharge resistor to avoid the output being left in an unknown, floating state.

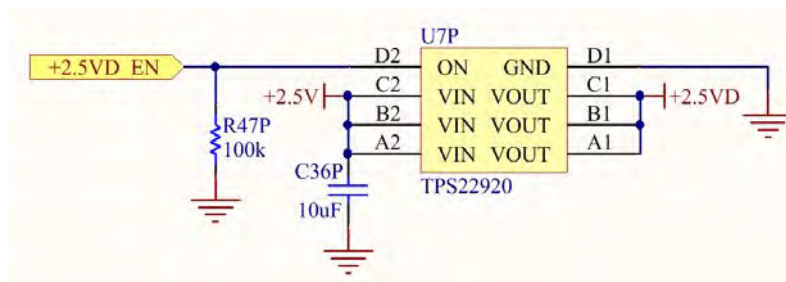


Figure 4.6: Schematic of the 2.5V load switch

#### 4.1.3.2 Analog Supply

The DRS4 and supporting electronics, as well as the first stage amplifier, also requires a 2.5 V power supply. However, due to these components’ sensitivity and susceptibility to noise, they are powered by a separate identical TPS7A3701 regulator.

#### 4.1.4 3.3 V Supply

TI's TPS62182 2-phase step-down converter is used to supply the FPGA board's secondary, high-current, 3.3 V power line. The fixed output converter was simple to implement and only requires two small 1  $\mu\text{H}$  inductors at the output. The converter offers built-in over-current protection, over-temperature protection and automatic efficiency enhancement which is based on the load current.

The soft-start capacitor, C24P, ensures a smooth startup and mitigates high inrush current. Furthermore, resistors R13P and R14P as well as capacitor C23P set a specific undervoltage lockout thereby disabling the regulator when the input voltage is insufficient to power the entire system.

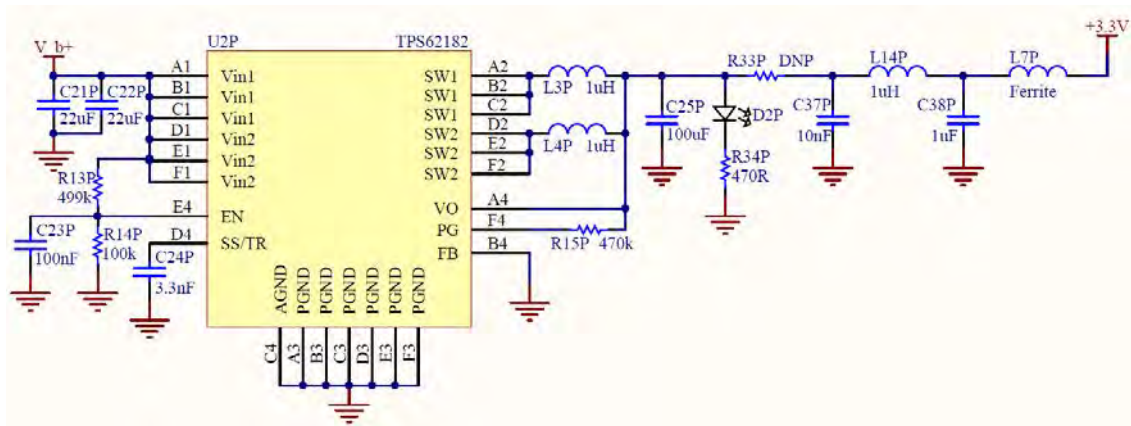


Figure 4.7: Schematic of the 3.3V step-down, switching regulator

#### 4.1.5 5 V Supply

The primary input voltage to the FPGA board is 5 V and the current requirement is highly dependent on the FPGA resource utilization, peripheral usage etc. Furthermore, the majority of the detector's components also requires a 5 V supply, thereby leading to a large overall current. Consequently, a high-efficiency synchronous buck converter is used that can source 20 A continually. The calculation for the converter's component values can be found in Appendix C.4.

The TPS53353 automatically adjusts modes to ensure optimal efficiency, based on load current, and offers a very fast transient response. In addition, it also features over-current, over-voltage, over-temperature and under-voltage lockout. As the 5 V line also powers high-current, noise-sensitive amplifiers, the converter's output is filtered with a PI-type filter preceded by a ferrite bead. The filtered 5 V power line is permanently enabled and supplies the FPGA and certain peripherals (such as USB 2.0) directly.

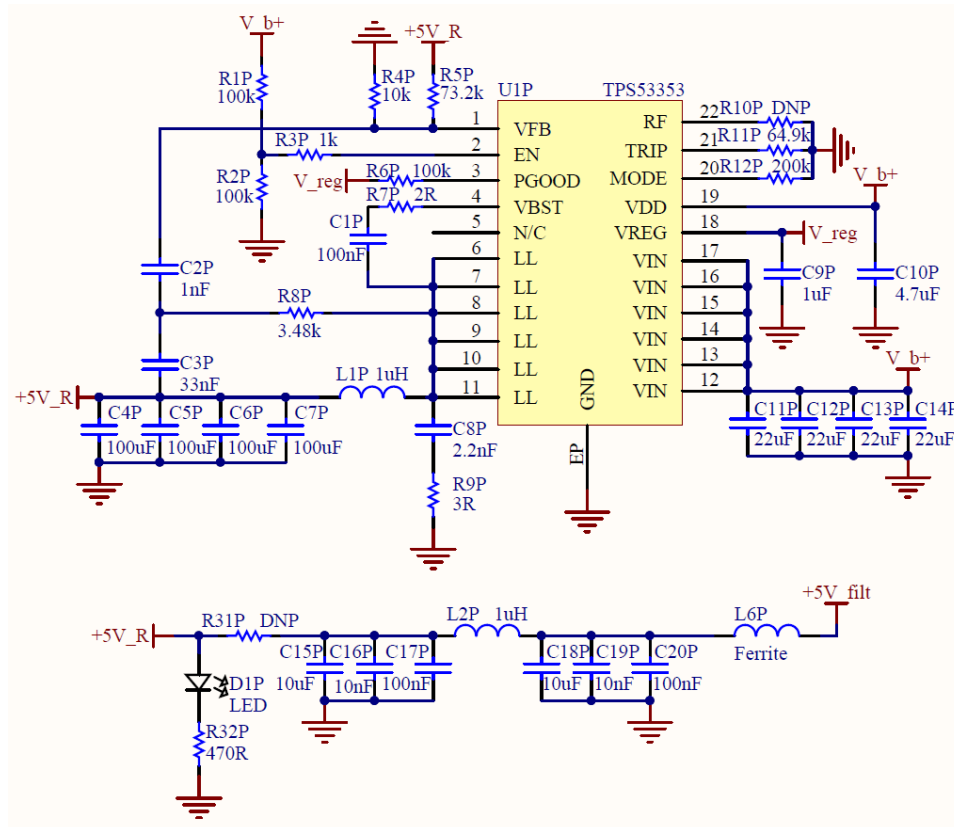


Figure 4.8: Schematic of the 5 V step-down, switching regulator

The DRS4 DAC, second stage amplifier, wideband amplifier, trigger comparator, trigger reference and programmable first stage amplifier also operate off a 5 V supply. However, due to their high quiescent current they required a means of being enabled and disabled. Therefore, a low on-resistance (16 m $\Omega$ ) load switch was connected in series with the filtered 5 V supply and the components' supply lines, see Figure 4.9.

The load switch can support 6 A of continuous current and has a configurable rise time to limit the inrush current. Furthermore, the switch has a built-in discharge resistor to ensure that the output voltage defaults to a known state when powered off.

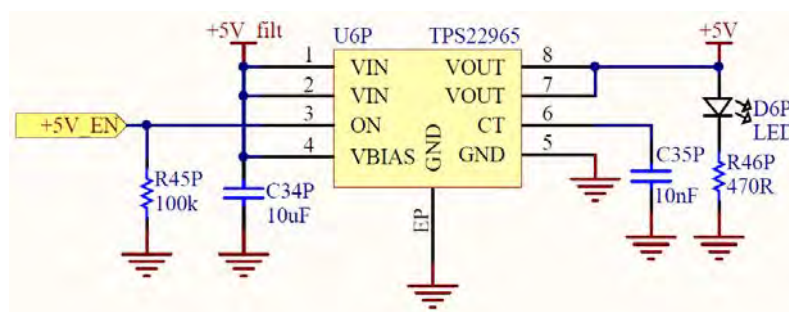


Figure 4.9: Schematic of the 5V load switch

## 4.2 Fast-Mode Input

Each of the nine silicon photomultipliers has two outputs, a standard- and fast-mode output. The fast-mode signal is used to trigger the detector, thereby notifying the system that a particle event took place. Figure 4.10 shows the fast-mode signal input and the respective trigger components for each of the nine channels.

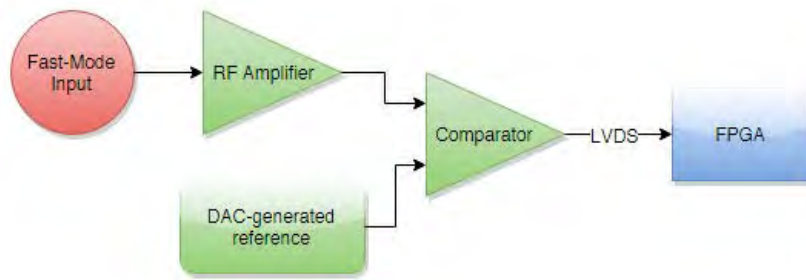


Figure 4.10: Diagram of the fast-mode signal chain

### 4.2.1 Signal Input

For implementation in a spacecraft, the silicon photomultipliers would be placed some distance away from the readout electronics. For example, in a small satellite, the readout electronics could be placed anywhere in a stack of circuit boards, deep within the thermally controlled spacecraft whereas the scintillators would be on, or near, the surface of the spacecraft. Therefore, a means of remotely connecting the sensors to the detector is required.

Consequently, a surface-mount, female MCX socket is used as the breakout connector for each of the photomultipliers' outputs. The connector is made from gold-plated beryllium copper with an internal Teflon insulator providing excellent contact surfaces while keeping separate electrical nets well insulated. The connector is matched for  $50\ \Omega$  and can support frequencies up to 6 GHz. A single-shielded RG316 coaxial cable, matched for  $50\ \Omega$ , is used between the two connectors and is capable of supporting a maximum frequency of 3 GHz.

### 4.2.2 Wideband Amplifier

The wideband amplifier is the first stage for the trigger input and is responsible for amplifying the input signal using a BGM1013 amplifier. This high-linearity, RF-class amplifier is internally matched to  $50\ \Omega$  and provides very high gain (35.5 dB at 1 GHz). Furthermore, it consumes a maximum of 27.5 mA and can operate over a wide temperature range (-40 to 85 °C).

The input was AC-coupled and did not require any external matching. The DC blocking capacitors on the input (C3) and output (C4) were chosen to support

frequencies above 100 MHz. The 100 nH inductor was placed at the output to act as an RF choke, thereby DC-biasing the output to ensure that the output remained within the voltage limits. Two optional DNP resistors were placed at the output to re-bias the output if required.

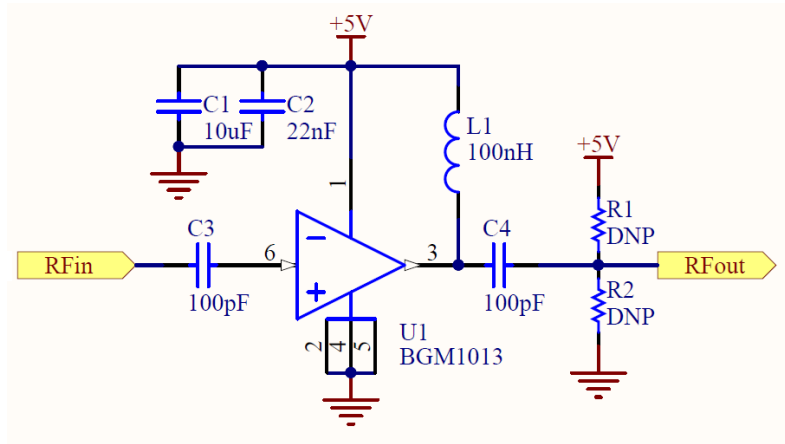


Figure 4.11: Schematic of the wideband amplifier

Given the high-frequency nature of this device, Agilent's Advanced Design System (ADS) software was used to simulate the circuit and confirm its frequency response. The circuit diagram for simulation is shown in Figure 4.12. The source was set up to sweep from 100 MHz to 3 GHz and had an output impedance of 50  $\Omega$ . The output was measured across a 50  $\Omega$  load for a true representation of the actual implementation.

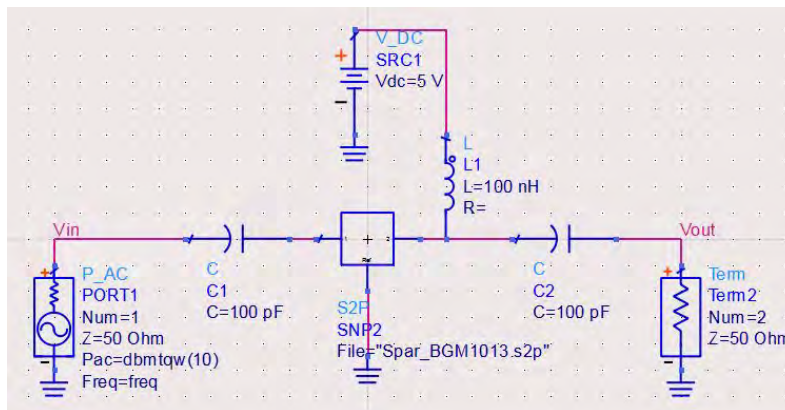


Figure 4.12: Schematic of the wideband amplifier in ADS

Figure 4.13 shows the amplitude and phase versus frequency for the ADS simulation. The amplitude, from  $V_{in}$  to  $V_{out}$ , remains above 34 dB and the phase decreases linearly between 100 MHz and 1.5 GHz. Beyond 1.5 GHz the amplitude decreases at a rate of approximately 7 dB per Gigahertz and the phase changes polarity. This was the expected result given the information from the datasheet.

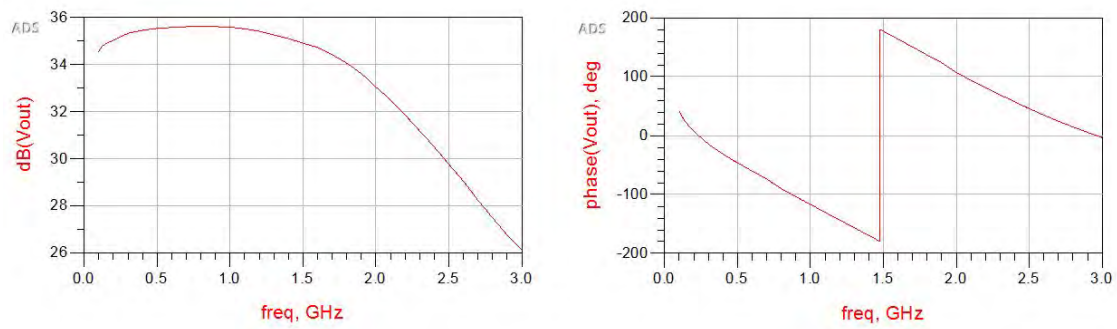


Figure 4.13: Amplitude and phase plots of the wideband amplifier

Figure 4.14 shows a Smith chart containing  $S_{11}$  and  $S_{21}$ .  $S_{11}$  represents the reflection seen at the input and is a function of the input match and  $S_{21}$  represents the signal at the output as a function of the input.  $S_{11}$  can only barely be seen at the center of the Smith chart showing that the source is well matched to the amplifier's input.  $S_{21}$  is a spiral starting on the far right and tends towards the center with an increase in frequency. This result is typical of an RF amplifier in that it has a large gain (far away from center), has a varying phase with frequency (spiral nature) and tends to zero with an increase in frequency.

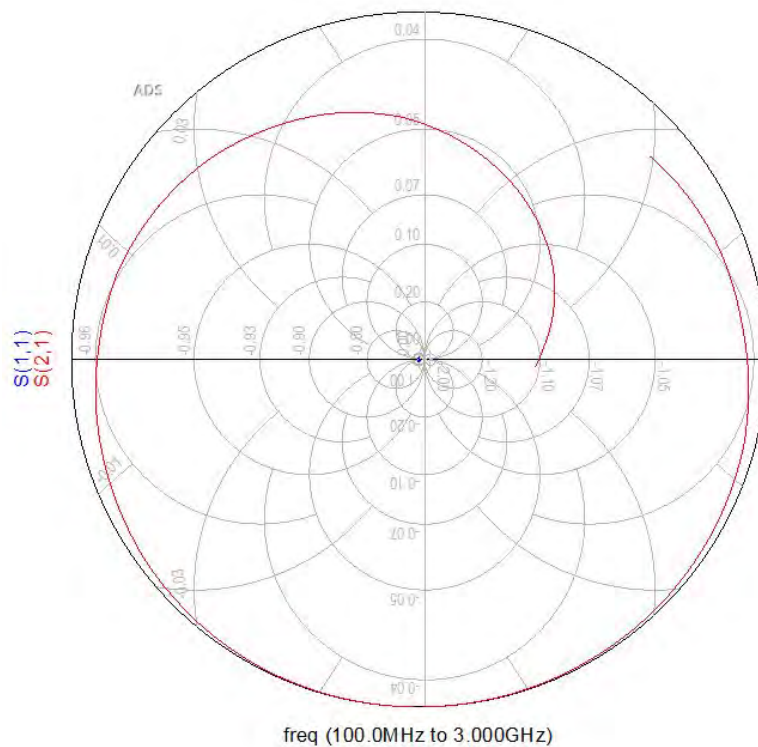


Figure 4.14: Smith chart of the wideband amplifier

### 4.2.3 Trigger Comparator

The second stage of the trigger input is a high-speed comparator and this is the last component of the fast-mode signal chain before the FPGA, see Figure 4.15. The comparator is responsible for comparing a trigger reference voltage, generated by supporting electronics, to the signal obtained from the wideband amplifier. The resultant output is then fed to the FPGA where further action can be taken.

The LMH7220 comparator has a modest current consumption of 6.8 mA and very fast rise and fall times of 0.6 ns. The LMH7220 also has an LVDS output capable of switching a 3.25 mA current source, resulting in a 325 mV voltage swing when using a 100  $\Omega$  termination resistance. The current-mode differential output has the advantage of low power consumption, regardless of switching rate, while maintaining a high level of suppression for common-mode noise.

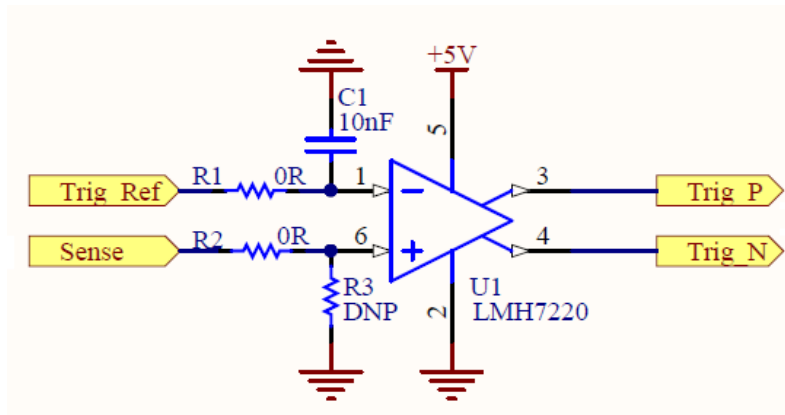


Figure 4.15: Schematic of the high-speed trigger comparator

The trigger voltage reference is generated by a 16-bit, ultra-low glitch DAC, allowing for the reference to be changed on the fly, see Figure 4.16. The DAC8560 boasts high accuracy (0.02 %) and temperature stability (2 ppm/ $^{\circ}$ C) and incorporates a 2.5 V internal reference that is enabled by default. Furthermore, the DAC has a low-power SPI-compatible serial interface compatible with 3.3 - 5 V systems. Because the FPGA's I/O pins operate at 2.5 V, a level translator was added between the FPGA and the DAC. The 4-bit bidirectional TXB0104 voltage-level translator is capable of automatically sensing push-pull CMOS logic data direction between its two ports. It also offers very low power consumption (5  $\mu$ A) and excellent ESD protection ( $\pm$ 15 kV).

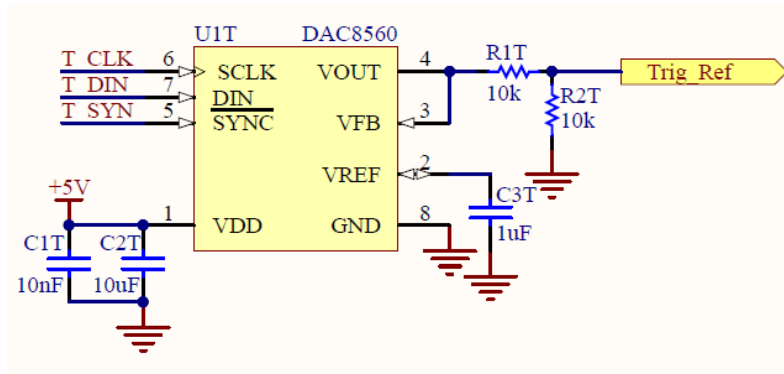


Figure 4.16: Schematic of the single channel 16-bit DAC

### 4.3 Standard-Mode Input

The silicon photomultiplier's standard-mode outputs contain the sensitive particle information that is to be analyzed. Figure 4.17 shows the standard-mode input, signal conditioning and digitizing stages for each SiPM channel before being collected and analyzed by the FPGA.

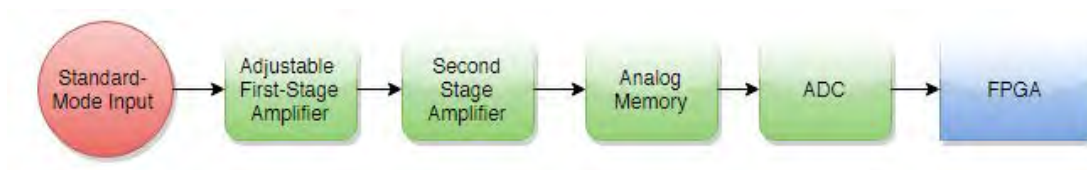


Figure 4.17: Diagram of the standard-mode signal chain

#### 4.3.1 First Stage Amplifier

The first stage amplifier has the delicate task of amplifying the single-ended input by a programmable gain value and outputting the result on a differential pair. The LMH6882 programmable differential amplifier offers a variable gain over 6 - 28 dB in 0.25 dB steps and is therefore used to accomplish this task.

The high-linearity, dual input LMH6882 has a bandwidth of 2.4 GHz and is optimized for signal path applications up to 1 GHz. The AC-coupled inputs were matched to 50  $\Omega$ , as shown in Figure 4.18, and zero ohm resistors were placed at the output in case output impedance matching became an issue. The gain can be controlled via an SPI-compatible serial interface allowing for automatic gain control during regular operation.

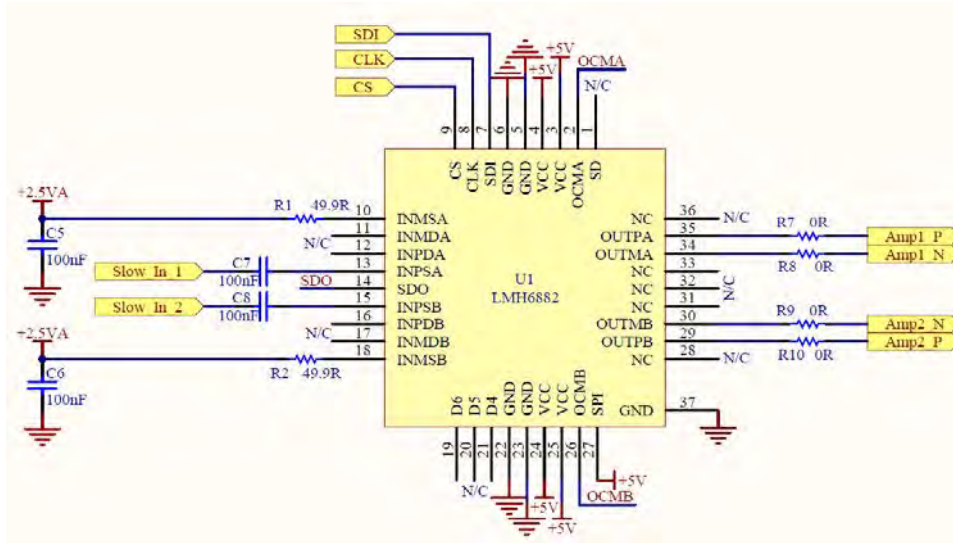


Figure 4.18: Schematic of the dual-channel programmable first stage amplifier

### 4.3.2 Second Stage Amplifier

The second stage amplifier uses TI's THS770006 to provide an additional fixed gain step along the standard-mode signal chain. THS770006 is a fully-differential amplifier that is optimized for driving digitizers and provided +6 dB of gain across a 2.4 GHz bandwidth. The device has a 100  $\Omega$  input impedance, and therefore does not require placement of additional termination resistors. It also includes an enable pin connected directly to the FPGA.

As before, two zero ohm resistors were placed at the output to account for potential impedance mismatching caused by the subsequent passive component network. The subsequent network contains a differential bandpass filter to prevent anti-aliasing during the sampling process and a re-biasing network to maintain the signal within the linear region of the next stage's NMOS transistors.

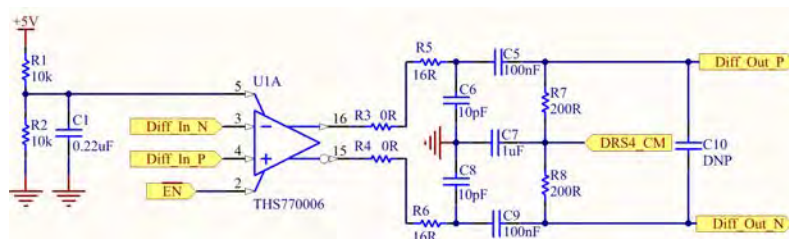


Figure 4.19: Schematic of the fixed-gain, fully differential, second stage amplifier

Given the relatively complex nature of the two amplification stages, the overall circuit was simulated with TINA-TI to ensure the amplifiers operated correctly when connected, see Figure 4.20. A signal obtained from the SiPM breakout board

was digitized and used as the input signal to the simulation and the output was monitored at different stages of the circuit to ensure correct operation.

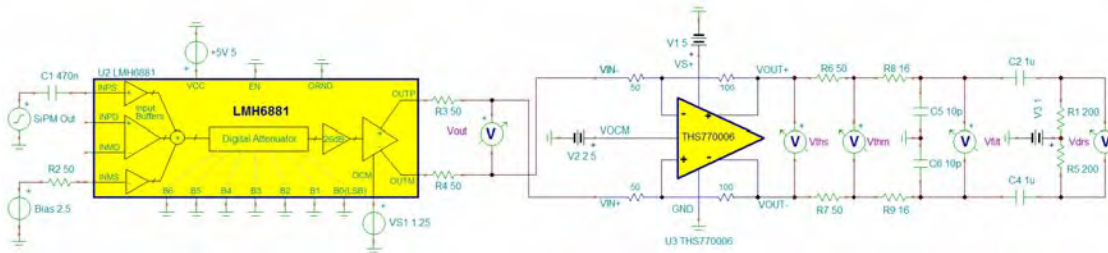


Figure 4.20: Schematic of the two amplifier stages in TINA

The results of the simulation are shown in Figure 4.21. Note that the input voltage (SiPM Out) is amplified from 39 mV to 418 mV at the output of the first amplifier. This is a gain of 10.59 (20 dB), not 19.95 (26 dB) as expected. This apparent loss of gain is caused by the impedance matching at the output of the LMH6881 amplifier. If the voltage is measured before the 50  $\Omega$  matching resistors, the full 26 dB gain is seen.

The second stage output ( $V_{thn}$ ) shows a gain of two, as expected, and demonstrates the same apparent gain loss when matched at the output ( $V_{thm}$ ). The bandpass filter further reduces the amplitude slightly ( $V_{filt}$ ) but the re-biasing network has no effect on the amplitude.  $V_{drs}$  cannot be seen as it lies directly behind the  $V_{filt}$  output.

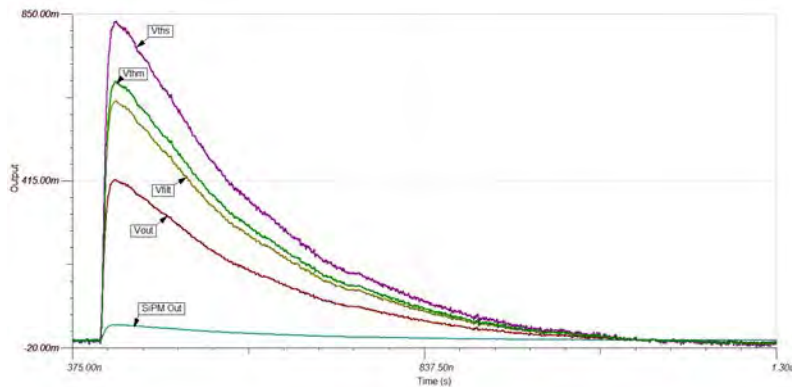


Figure 4.21: Simulation results of the two amplifier stages

### 4.3.3 Analog Memory

ADCs capable of sampling at a continuous rate of 1 - 5 GSPS, producing an output rate of 14 - 70 Gbit/s, are rare, complex, expensive and power hungry. Therefore, to achieve these GSa/s sampling rates, an SCA is used to temporarily store analog

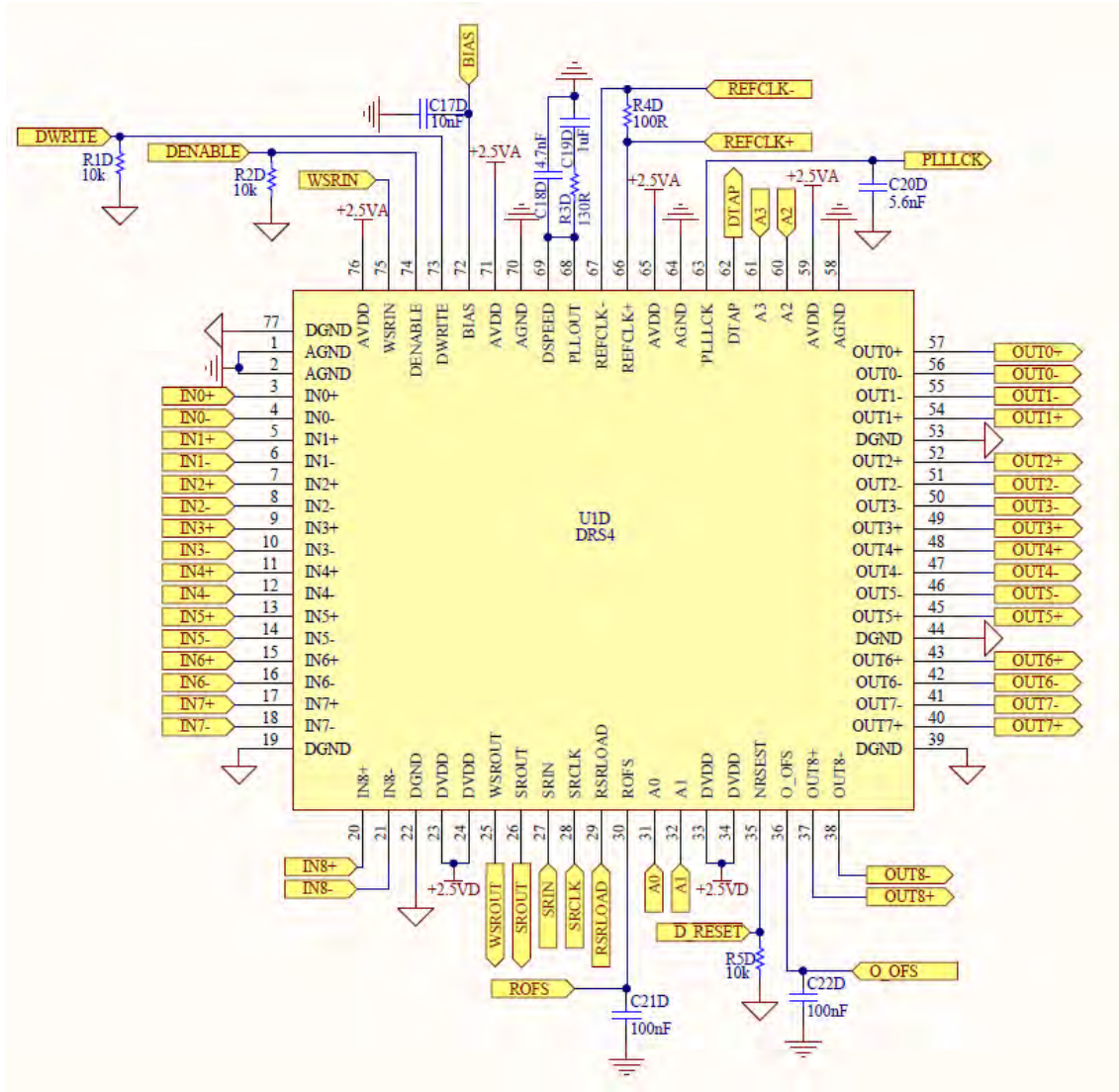


Figure 4.22: Schematic of the DRS4 switch capacitor array

samples of the signal which are later read out with a 14-bit ADC at a significantly slower rate, see Figure 4.22.

The DRS4 9-channel switched capacitor array offers sampling speeds ranging from 700 MSPS to 5 GSPS. It contains 9 sets of 1024 storage cells (150 fF capacitors) which are activated through an FPGA-controlled write (DWRITE) and enable (DENABLE) switch. The DRS4 consumes very little power (17.5 mW per channel at 2 GSPS) and offers a high signal to noise ratio (69 dB). Detailed calculations and explanations of the various inputs and outputs are documented in Appendix C.5. The operational details for the DRS4 are discussed further in Chapter 6.

The DRS4 requires four digitally-adjustable analog voltages (BIAS, ROFS, O\_<sub>-</sub>OFS and DRS4\_CM). These voltages are generated using TI’s 16-bit, quad-channel, ultra-low glitch DAC8565, see Figure 4.23. The DAC has an internal 2.5 V reference that is enabled by default and offers excellent initial accuracy (0.004 %) and

temperature drift (2 ppm/°C). Furthermore, the DAC consumes very little power (1 mA at 5 V) and has a serial interface compatible with SPI that can operate at data rates as high as 50 MHz.

The DAC8565 is configured to reset all DAC-channels to mid-scale when powered up, ensuring that the DRS4 can operate optimally. The DAC requires two power supplies, one for the analog output voltage and one for the digital I/O interface, thereby negating the need for a level translator. Using the internal voltage reference, the resultant output resolution was 38  $\mu\text{V}$  with a full-scale voltage range of 0 to 2.5 V.

Although the DAC contains an internal rail-to-rail output buffer, two of the outputs require an additional dedicated buffer to drive their respective loads. This is achieved with a dual-output, low-noise opamp that offers a low-offset voltage, an internal EMI filter and rail-to-rail operation.

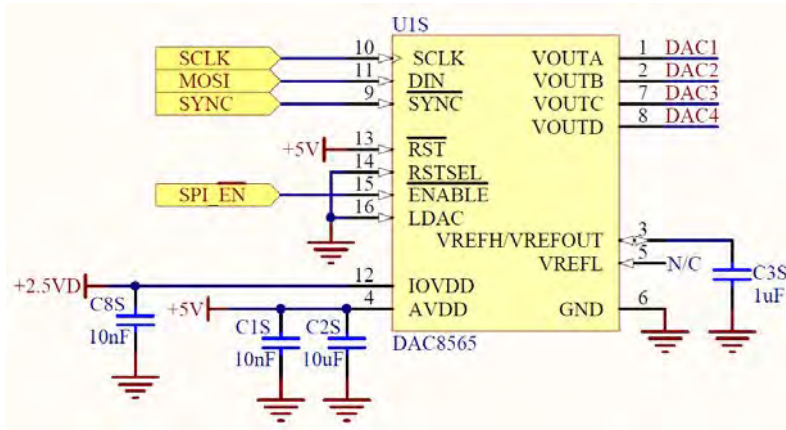


Figure 4.23: Schematic of the four-channel DAC

#### 4.3.4 Digitization

Once a trigger signal has been received, and the analog memory has been halted, the analog samples are digitized via Linear Technology's 14-bit 65 MSPS dual ADC, see Figure 4.24. The LTC2265-14 has a full power bandwidth of 800 MHz, an excellent 73.7 dB signal to noise ratio and a 90 dB spurious free dynamic range. Furthermore, the differential analog inputs and LVDS digital outputs ensure good signal integrity and immunity from EMI. An SPI-compatible serial interface allows the ADC to be configured for different power and readout modes, sampling frequencies, output currents etc.

The LTC2265-14 has differential analog inputs, and their common-mode voltages are set by the corresponding VCMx outputs. Anti-aliasing filtering and re-biasing is addressed in Appendix C.6. The FPGA is used to generate the required reference clock for the ADC. Because the ADC's noise performance is strongly related to the signal quality of the reference clock, the LVDS standard is used to drive the ADC's clock input in differentially encoded mode.

The data outputs also make use of the differential LVDS standard to transmit data from the ADC to the FPGA. The output stage consists of a data clock (DCO), data frame output (FR) and two channels of data (OUTx). The ADC is configured to transmit data in 1-lane output mode with 14-bit serialization using the default output current level of 3.5 mA. The outputs are discussed in more detail in Chapter 6.

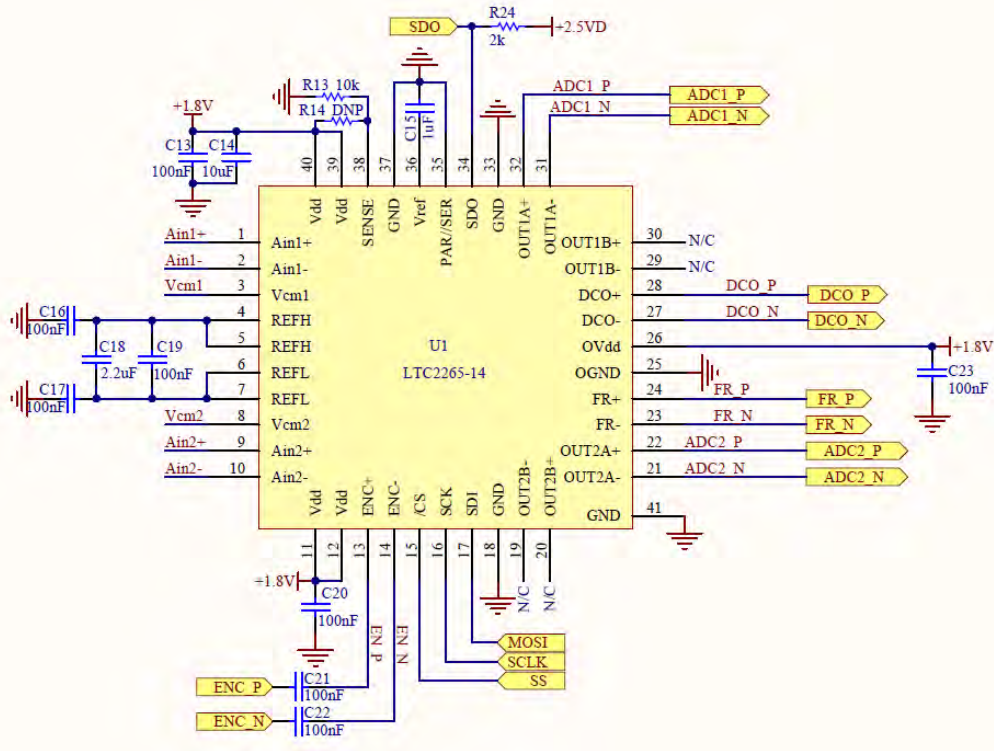


Figure 4.24: Schematic of the dual-channel, 14-bit ADC

## 4.4 System-on-Chip

### 4.4.1 Trenz TE0720

The Trenz Electronic TE0720 is an industrial-grade system-on-chip (SoC) module incorporating the Xilinx Zynq Z020 SoC. The module measures only 50 x 40 mm and is rated to withstand temperatures ranging from -40 to 85°C as well as high shock and vibrational environments. In addition to the onboard SoC, the module incorporates a host of additional features and peripherals, some of which are mentioned below:

- 1 GB of DDR3 SDRAM
- gigabit Ethernet
- 4 GB of eMMC
- USB 2.0

- high-efficiency DC-DC power converters
- MEMS sensor (3D accelerometer and magnetometer)

Figure 4.25 shows a photograph of the device as well as a functional diagram. The module has three high-speed hermaphroditic board-to-board connectors allowing access to 152 FPGA I/O pins and 14 processor pins. Furthermore, the module has four corner-located mounting holes to securely fasten the breakout board to any carrier board. This module was mounted onto the custom board designed for the readout electronics, providing the necessary processing power for the particle detector.

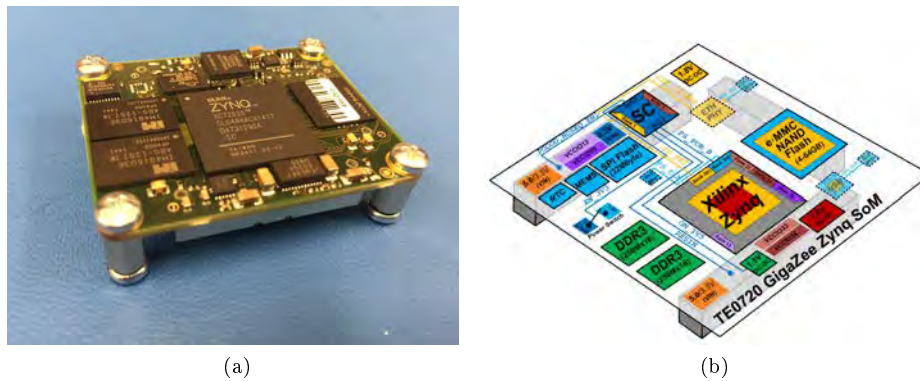


Figure 4.25: Photo (a) and functional diagram (b) of the Trenz TE0720 module[54]

#### 4.4.2 Xilinx Zynq-7000

The TE0720 module is essentially a breakout board for Xilinx Zynq Z020 SoC. The Zynq-7000 series SoCs are devices that contain both FPGA fabric and an ARM dual-core Cortex-A9 MPCore processing system, implemented in 28 nm technology. The powerful combination of the FPGA’s parallelism and the dual-core processor’s high clock speeds and floating-point capabilities, results in a device that is both scalable and flexible. A more detailed overview of the TE0720, the Zynq SoC, as well as a comparison between the different models, can be found in Appendix ??.

#### 4.4.3 Power

The TE0720 has two power inputs called “Vin” and “Vin 3.3 V”. The first input can be powered from any voltage ranging from 3.3 - 5.5 V at a maximum current of 8 A. To optimize the power transfer across the connector, 5 V (close to the upper voltage limit) is used to power the module. A lower voltage would require more current for the same amount of power to be transferred, leading to more power loss ( $P_{loss} = I^2 R$ ). The second input, as the name suggests, requires a regulated voltage of 3.3 V with a maximum input current of 300 mA. The regulated 3.3 V supply is generated by a permanently-enabled switch-mode regulator on the custom circuit board.

A voltage source has to be provided for the four FPGA I/O banks, accessible via the TE0720's breakout connectors. Three of these banks, VCCIO\_13, 33, and 35 are unmonitored by the system management controller and accept voltages in the range of 1.2 to 3.3 V. VCCIO\_34, however, is monitored and has to be powered at all times with a voltage ranging from 1.5 to 3.3 V. Based on the constraints posed by the readout electronics, all the FPGA banks are powered with 2.5 V by default, however, the option for a 3.3 V power source for the banks is reserved with a DNP resistor.

In addition to the module's inputs, it also has a few voltage outputs. The 1.8 V and 3.3 V outputs are used to power peripherals solely related to the module such as the MicroSD card, the JTAG programmer, reset buttons etc. The 1.8 V output can source up to 1.5 A and the 3.3 V output up to 2 A.

#### 4.4.4 System Management Controller

The System Management Controller (SMC) is implemented using a Lattice CPLD on the TE0720 module and is responsible for power sequencing, reset generation and initial configuration of the Zynq SoC. Although the SMC can be completely reprogrammed for custom applications, most functionality is controlled through user-accessible I/O pins connected to the CPLD.

##### 4.4.4.1 EN1 Pin

The EN1 input pin controls the DC-DC converters onboard the TE0720 module and contains an internal weak pull-up to power the module by default. A DNP resistor was placed connecting the input to ground in case the DC-DC converters were to be disabled during testing.

##### 4.4.4.2 PGOOD Pin

The PGOOD pin is an open-drain output that is forced LOW until all the module's power supplies were operating correctly. For a quick visual indication of power status, an LED and current-limiting resistor were placed in series with this pin.

##### 4.4.4.3 MODE Pin

The TE0720 supports two boot modes, namely Quad Serial Peripheral Interface (QSPI) and SD Card mode. In QSPI mode, the Zynq loads the first-stage bootloader (FSBL) from the SPI flash and executes it, after which processor object code or FPGA configuration is loaded. In SD Card mode, the QSPI is not used at all, and the same procedure occurs, but originates from the SD Card instead. The MODE input pin is able to select between these two modes by applying a logic LOW for QSPI mode and a logic HIGH for SD Card mode. Since both these modes would be tested, a selector switch was installed to allow the user easy access to both boot modes.

##### 4.4.4.4 RESIN Pin

The RESIN pin is mapped directly to the Zynq processor's reset pin. The reset input is active-low and is therefore pulled-up with an external resistor during regular

operation. Additionally, a push button that grounded the pin when actuated was added, giving the user a means of resetting the Zynq SoC at will.

#### 4.4.4.5 NOSEQ Pin

The NOSEQ input pin controls the 1 V and 1.8 V power converters at boot up. Depending on the application, the module can be booted with or without power sequencing. The dual power supply ( $V_{in} = 5\text{ V}$  and  $V_{in} 3.3\text{ V} = 3.3\text{ V}$ ) configuration requires “no sequencing” and the NOSEQ pin is therefore pulled-up with an external resistor. The pin has an internal weak pull-down that forces the converter to regular sequencing mode once the external resistor is removed.

#### 4.4.5 SD Card

A MicroSD card was added to the custom circuit board to allow the module to boot from a larger operating system, such as Linux, which is not supported by the onboard QSPI flash. The Zynq’s SD card interface operates at 1.8 V and the MicroSD card requires a 3.3 V interface. To bridge the different logic levels, a TXS02612 SDIO voltage level translator is used which supports data rates up to 120 Mbps and incorporates latch-up and ESD protection. In addition to booting from larger operating systems, the MicroSD card also acts as additional, non-volatile storage.

#### 4.4.6 JTAG Programming

Although the overall system will usually boot from QSPI or the SD card, the FPGA and processor can also be initialized manually through a JTAG header placed on the custom board. The header was designed to accommodate most JTAG programmers but was only tested with the JTAG HS1 programming cable.

#### 4.4.7 USB 2.0

An additional requirement posed by UCT’s physics department was the option to stream raw particle data from the detector to a computer. The TE0720 module incorporates a USB3320 USB 2.0 transceiver from Microchip Technology which, theoretically, only requires the addition of a USB connector. USB 2.0 offers data transfer rates of up to 480 Mbit/s which is sufficient for transferring 1024 data points at a maximum rate of 33 kHz. Furthermore, the USB3320 supports full USB On-The-Go (OTG) which allows the protocol to be dynamically configured as a host or device.

In addition to the MicroUSB connector added to the custom PCB, a common-mode choke and a load switch were included too. The common-mode choke is used on the differential data lines to prohibit noise from entering the circuit from the USB lines. Certain USB devices, such as flash drives, require a powered USB connector, hence the addition of a load switch that can provide USB power when necessary.

#### 4.4.8 GPIO Expansion

To provide sufficient opportunity for expansion and additional features for future developments, a small 12-pin breakout header was added to the custom board. The header allows access to seven FPGA I/O pins as well as two processor pins. Furthermore, access to the Zynq's VBATT pin and a ground reference was made available. The VBATT pin provides backup power to the RTC chip on the TE0720 to retain state data when the main power is removed or lost.

#### 4.4.9 UART-to-USB

The Zynq's UART protocol is used as a low-speed communication link between the detector and a computer. This communication link had three main purposes:

1. Simple control of peripherals, allowing enabling and disabling of different aspects of the detector during testing.
2. General status monitoring of the detector such as particle event counts, operating temperature etc.
3. Simulating a preset space mission by selecting different mission modes and monitoring the detector's performance.

The link was realized with a UART-to-USB converter (FTDI's FT232RQ) and a small-footprint MicroUSB connector.

#### 4.4.10 Board-to-Board Connectors

The custom board included three shielded Samtec Razor Beam LSHM connectors to mate with the TE0720 module. The two parallel connectors contain 100 pins each (two rows of 50) and the remaining perpendicular connector contained 60 pins (two rows of 30). The overall mating height could be adjusted using ten different options ranging from 5 to 12 mm. The default height of 8 mm was chosen by using the corresponding identical connector at each location. The LSHM connectors were ideal for the application having been rated for 100 G shock for 6 ms and 7.5 G of random vibration for three hours in three axes.

#### 4.4.11 LVDS

The vast majority of the FPGA I/O pins are used as LVDS inputs and outputs to support all the data collection from the ADCs. The Zynq uses the LVDS\_25 I/O standard which is capable of 1250 Mbits/s per LVDS pair and requires that the relevant I/O banks are supplied with 2.5 V. Each differential I/O block (set of 2 I/O pins) contains an integrated current-mode differential driver as well as an optional termination resistor, see Figure 4.26[55].

Each differential input pair, such as ADC1\_P and ADC1\_N, consists of two transmission lines, matched to 50  $\Omega$ , and entered the FPGA at an I/O block. The FPGA's internal 100  $\Omega$  termination resistor is used as it is much closer to the differential voltage comparator within the FPGA. If an external termination resistor was used, the lines would still have to be routed to the board-to-board connectors and then to the FPGA which could lead to a significant reduction in signal integrity.

The use of the internal termination requires that VCCIO be powered at 2.5 V, setting the power requirements mentioned previously.

Similarly, for the output pairs, a  $50\ \Omega$  transmission line started at the FPGA I/O block and was routed to the relevant receiving device. External  $100\ \Omega$  termination resistors were placed as close to the receiving chips as possible when internal termination was not available. In no case was the FPGA's internal termination resistor used for the LVDS outputs.

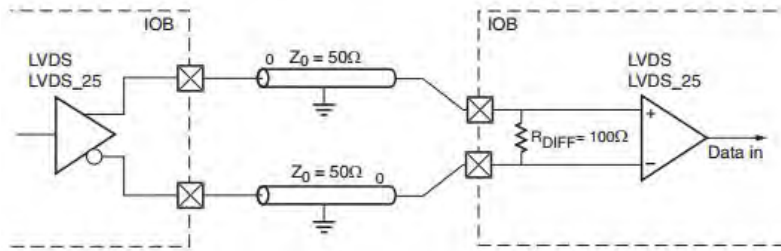


Figure 4.26: Example of an LVDS transmitter/receiver pair implemented on a Xilinx Zynq[55]

## Chapter 5

# PCB Layout

*TraX Interconnect* was chosen as the PCB fabrication house and *Barracuda Holdings* as the assembly house. Both these companies have IPC-compliant facilities and are located in Cape Town, South Africa. They were consulted with during the PCB design and layout process for guidance and to determine their capabilities and limitations.

### 5.1 PCB Substrate

A PCB's substrate is a critical design choice when dealing with high performance circuitry. There are many different substrates available, varying in performance and cost. Based on the particle detector's high-speed analog and digital circuitry, and the intention to deploy the detector in a space environment, the following substrate characteristics were desired:

- A low dielectric constant ( $D_K$ ) which results in faster signal propagation and lower stray capacitance. Furthermore,  $D_K$  should be constant with temperature variations to ensure consistent performance throughout the temperature range on a spacecraft.
- A low dissipation factor ( $D_f$ ) to minimize signal distortion and to preserve signal integrity.
- An identical coefficient of thermal expansion (CTE) if multiple substrates are used for the stackup to avoid warping or other manufacturing defects.
- High thermal conductivity to assist in heat dissipation from circuitry to a heat-dissipating structure. This is particularly important for a space application due to the lack of convection cooling.
- Low moisture absorption to avoid outgassing when deployed in a space environment which could lead to a significant degradation in performance.

The standard substrates that TraX stock are FR4, Rogers 4003C, Mercurywave 9350, Aluminum Metal Core and Copper Metal Core. Although Rogers 4003C stood out as the most suitable substrate, Mercurywave 9350 was chosen instead as it offered similar performance but cost significantly less.

Mercurywave 9350 is a high thermal reliability, non-PTFE substrate that is designed for use in high frequency, low loss systems. The relevant performance parameters are as follows:

Dielectric Constant:	3.5 @ 10 GHz (Stripline)
Dissipation Factor:	0.004 @ 10 GHz (Stripline)
CTE (X and Y):	10-14 ppm/°C (-40 to +125°C)
Thermal Conductivity:	0.5 W/mK
Moisture Absorption:	0.15 wt. %

TraX stocks Mercurywave prepregs and cores in various thicknesses<sup>1</sup>. At the time of fabrication, TraX had the following Mercurywave cores available, all sold in 305 x 457 mm sheets:

Core Thickness	Copper Thickness
0.2 mm	17/17 $\mu m$
0.5 mm	35/35 $\mu m$
1.0 mm	35/35 $\mu m$
1.52 mm	35/35 $\mu m$

For custom stackups, the bare prepregs were also available:

Prepreg	Effective Thickness
1080	0.083 mm
2116	0.104 mm

## 5.2 PCB Stackup

To support the sensitive, high-speed, digital and analog signals, as well as the high current power lines, a custom six layer circuit board was designed. The first step in the design was defining the different copper layers and their primary purpose:

- |                        |  |
|------------------------|--|
| 1. Top Signal Layer    | High speed analog signals for standard mode output |
| 2. Top Ground Plane    | Supporting ground plane                            |
| 3. Inner Power Plane   | High-current, power distribution plane             |
| 4. Inner Signal Layer  | Low-speed digital signal distribution              |
| 5. Bottom Ground Plane | Supporting ground plane                            |
| 6. Bottom Signal Layer | High speed analog signals for triggering           |

The next step was choosing the substrate of the isolating material between the copper layers. The initial plan was to use regular FR4 adjacent to the two inner copper layers as these did not require a specialized high-speed substrate. By ensuring that the stackup was symmetrical around the core layer, warping and mismatched CTEs should not have been an issue. However, to increase manufacturing reliability and due to no cost increase, Mercurywave was used throughout the stackup.

In addition to the aforementioned Mercurywave prepregs and cores, TraX also stocks the following copper foil options available for custom stackups:

<sup>1</sup>Prepreg refers to the substrate only whereas a core consists of the substrate with bonded copper layers

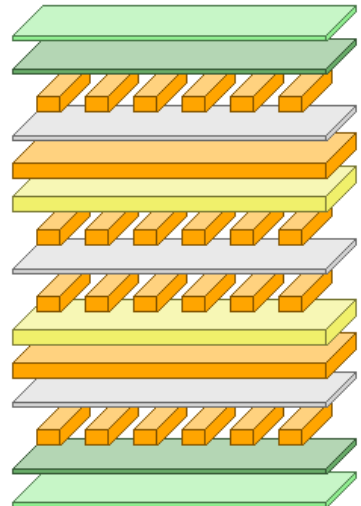
Copper Foil Description	Old imperial name	Effective thickness
17 micron	1/2 oz.	15 microns
35 micron	1 oz.	30 microns
70 micron	2 oz.	60 microns
105 micron	3 oz.	90 microns

Based on the available resources, the final stackup for the final PCB fabrication is shown in Figure 5.1.

As the outer layers require specific dielectric and copper thicknesses for accurate impedance matching, the center-most dielectric was used to set the overall circuit board thickness above 1.2 mm for structural purposes. The available prepregs were all too thin so the center-most dielectric was constructed out of 0.5 mm Mercury-wave core, with the 35  $\mu\text{m}$  copper layers removed, along with an additional 1080 prepreg on either side.

The four inner copper layers were then added by placing a 1 mm Mercurywave core, which contained two copper layers, on either side of the center-most dielectric. Before additional copper could be placed for the final outer layers, a 2116 Mercury-wave prepreg was added to each side of the stackup, followed by 17  $\mu\text{m}$  copper foil which was later plated to a thickness of 35  $\mu\text{m}$ .

The final pressed thickness was 1.194 mm which increased to 1.294 mm after the additional plating, finishing and masking. A more detailed stackup report from TraX can be found in Appendix F.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material
Top Overlay	Overlay			
Top Solder	Solder Mask/Co...	Surface Material	1.968	Solder Resist
Top Layer	Signal	Copper	0.669	
Dielectric	Dielectric	Prepreg	4.095	2116
Gnd_Top	Internal Plane	Copper	1.378	
Dielectric	Dielectric	Core	4.173	MW9350
Power Plane	Signal	Copper	1.378	
Dielectric	Dielectric	Prepreg	26.614	2x1080 + 0.51
Inner Signal	Signal	Copper	1.378	
Dielectric	Dielectric	Core	4.173	MW9350
Gnd_Bottom	Internal Plane	Copper	1.378	
Dielectric	Dielectric	Prepreg	4.095	2116
Bottom Layer	Signal	Copper	0.669	
Bottom Solder	Solder Mask/Co...	Surface Material	1.968	Solder Resist
Bottom Overlay	Overlay			

Figure 5.1: Final PCB stackup in Altium Designer

### 5.3 Finishing Processes

Once the layers were fabricated and bonded together, there were three additional finishing processes which aided in the reliability and assembly of the circuit board:

### 5.3.1 Surface Plating

Electroless Nickel/Immersion Gold (ENIG) was used to plate the copper to a thickness of  $35\ \mu\text{m}$  using the Rohm and Haas process. ENIG was chosen because of its excellent surface planarity which was critical because of the BGA and fine-pitch QFN components used in the design. ENIG also offers a good oxidation resistance and is inherently lead-free.

### 5.3.2 Soldermask

Regular matte, dark green soldermask was used on the top and bottom layers of the circuit board to provide protection against oxidation and solder bridges during assembly. The  $25\ \mu\text{m}$  soldermask coating thickness was accounted for in the controlled impedance line calculations.

### 5.3.3 Silkscreen

Due to the high-density nature of the circuit board design, silkscreen was not used to indicate component designators. However, standard white silkscreen was used to mark component outlines and orientations to assist in the assembly process.

## 5.4 Final Design

The final fabrication package consisted of the following files and documents:

- GERBER files - Vector image files used for circuit board fabrication
- Drill files - An Excellon format drill file used to guide CNC drilling and routing machines
- Fabrication drawing - Specifies critical design features such as layer stack-up, drill chart, dimensioned board outline etc.
- Assembly drawing - Specifies component orientation and location with designators

The final PCB was designed in Altium Designer and can be seen in Figure 5.2 and 5.3. The board measured 69 mm x 100 mm and was approximately 1.3 mm thick. All the design files can be found in Appendix F.

The costs for the PCB fabrication and assembly are itemized below:

Table 5.1: PCB fabrication and assembly costs

Company	Description	Cost
TraX	PCB Fabrication	R 6,181.01
Barracuda	Laser Cut Stencil	R 3,184.03
Barracuda	PCB Assembly	R 2,922.00
Digikey	Components	R 9,152.82
PSI	DRS4	R 1,103.50
<b>TOTAL</b>		<b>R 22,543.36</b>

TraX, Barracuda and PSI provided the author with a student discount. TraX and Barracuda were significantly cheaper than many of their competitors, in some

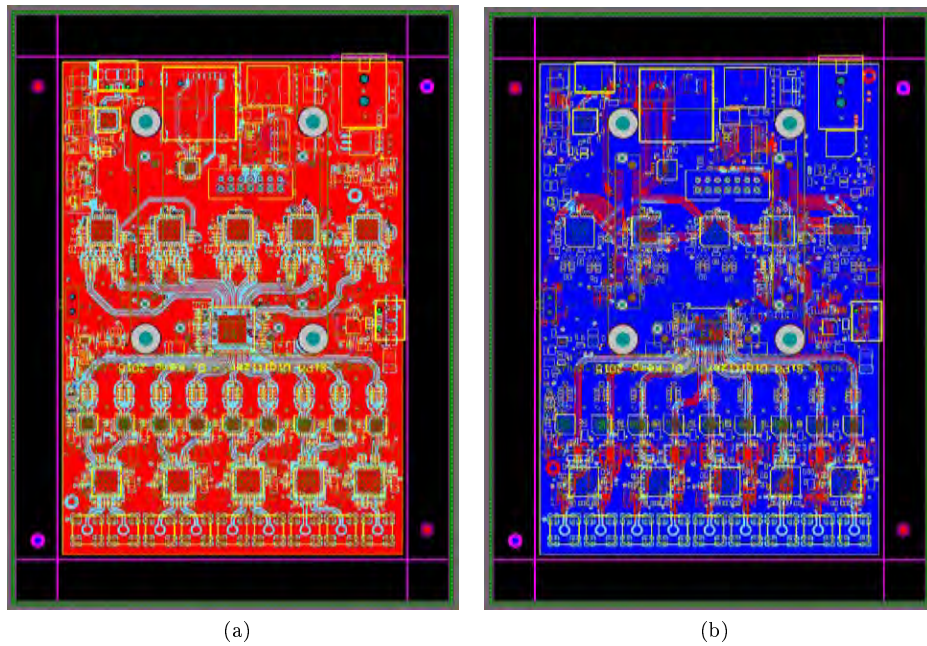


Figure 5.2: 2D Image of the top (a) and bottom (b) of the PCB layout

cases by a factor of nearly 10. As an example, Sierra Circuits in California, U.S. quoted approximately R 65,800.00 for fabrication and R 18,600.00 for assembly (excluding component, testing and shipping costs).

## 5.5 3D Model

The fabrication, assembly and shipping was estimated to take 4 - 6 weeks during which support firmware and hardware was to be developed. To ensure the PCB would fit and interface with the additional hardware, such as battery holders, FPGA daughter boards etc., a model of the circuit board was 3D printed on an industrial-grade Stratasys Dimension 1200es printer. The part was printed using ABSplus material, with a layer thickness of 0.254 mm, and required soluble support material to print the detailed components on both sides of the circuit board. The final part can be seen in Figure 5.4 and was a good representation of the actual assembled circuit board.

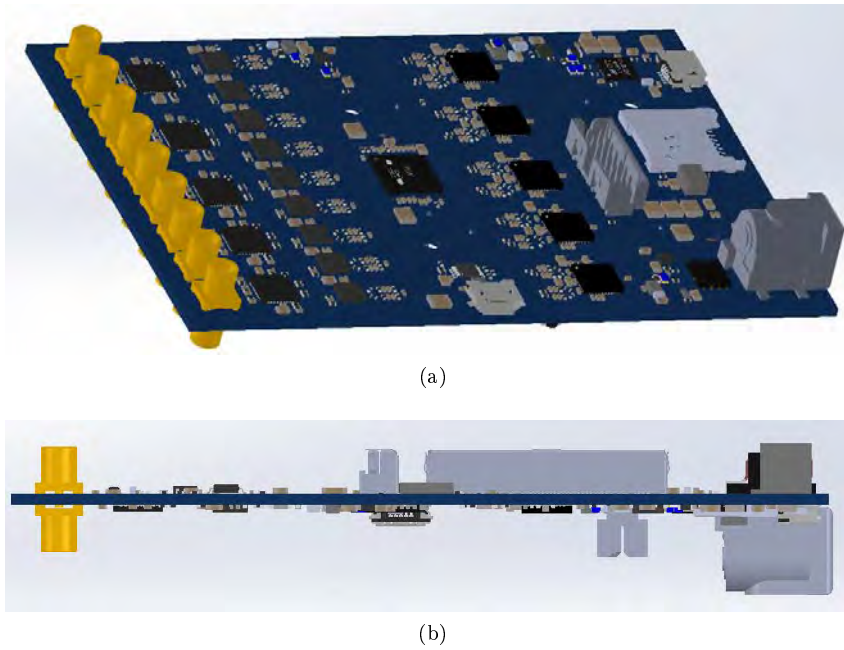


Figure 5.3: 3D model of the final circuit board

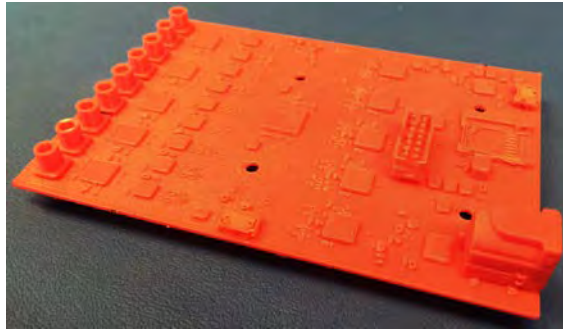


Figure 5.4: Image of the 3D printed PCB model

## Chapter 6

# Software Development

### 6.1 Introduction

Two sets of code had to be developed for the particle detector in Xilinx’s software suite, one for the FPGA and the other for the processor. The FPGA software was developed in VHDL using Xilinx’s Vivado Design Suite 2014.4 and the processor software in C using Xilinx’s Software Development Kit (SDK) 2014.4.

Figure 6.1 shows the process followed to obtain a platform that was able to boot the processor from QSPI flash and automatically program the FPGA bitstream at startup. The following sections describe the FPGA and processor code developed to support the different aspects of the hardware.

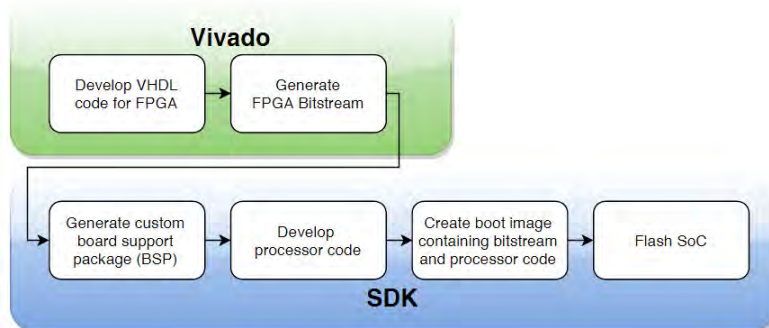


Figure 6.1: Diagram of the Xilinx software development process

### 6.2 Register Sharing

Two registers are used to send and receive basic commands and status messages between the FPGA and the processor. One register (`gpio_in_tri_i`) is used to write data from the FPGA to the processor and the other (`gpio_out_tri_o`) to write data from the processor to the FPGA. An AXI interface, with an AXI GPIO core, is used to communicate between the two architectures, see Figure 6.2.

When connected to a computer, the UART-to-USB converter allows the processor to receive commands from a computer in the form of a text string. This text

string can then be interpreted and relayed as a message via the `gpio_out_tri_o` register. Similarly, information can be received from the FPGA via the `gpio_in_tri_i` register and relayed to a computer in human-readable form. As an example, the DRS4's phase lock loop indicator (PLLCK) is routed to the `gpio_in_tri_i` register. The processor can read the value of this register and transmit it via the UART-to-USB converter to a computer.

The FPGA achieves this communication by mapping different bits of the register to general purpose inputs and outputs:

- Output: `gpio_in_tri_i(1) <= PLLCK`
- Input: `P18VEN <= gpio_out_tri_o(0)`

The processor uses the XGpio library for reading from and writing to the two registers with the following commands:

- Reading: `XGpio_DiscreteRead(&xgpio, FPGA_Status_Reg)`
- Writing: `XGpio_DiscreteWrite(&xgpio, FPGA_Control_Reg, command_reg)`

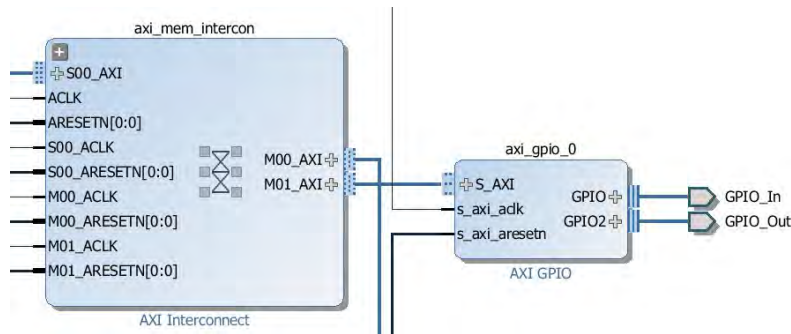


Figure 6.2: Diagram of the AXI Interface and GPIO Core

### 6.3 Power Supplies

Some of the power supplies have the option to be enabled/disabled from the FPGA for power conservation purposes. During a flight mission these states would be determined by the mission mode. For example, once data is collected for an experiment the amplifiers, SCA and ADCs can be disabled, saving a considerable amount of power while the FPGA and processor does further data processing.

During bench testing, however, these power supplies are controlled from a computer via the aforementioned register sharing mechanism. Text strings received by the SoC's processor via UART are translated and used to set/clear bits in the "gpio\_out\_tri\_o" register. The FPGA has the following mapping for the register to control the corresponding power supplies:

```

P18VEN    <= gpio_out_tri_o(0) // +1.8V Enable
P18VMD    <= gpio_out_tri_o(1) // +1.8V Mode Control
BO_7      <= gpio_out_tri_o(2) // +2.5VA Enable
P25VDEN   <= gpio_out_tri_o(3) // +2.5VD Enable
BO_5      <= gpio_out_tri_o(4) // +5V Enable

```

For example, if “Enable +5 V” is transmitted by a computer, the processor will interpret the text string and change bit 4 of the `gpio_out_tri_o` to HIGH, thereby enabling the +5 V power line. It can also be turned off by sending “Disable +5 V”.

## 6.4 Fast-Mode Input

The FPGA trigger system consists of two components, both of which are controlled by the FPGA. Firstly, the DAC controlling the trigger’s comparator reference voltage requires initialization as well as on-the-fly trimming based on the mission mode. Secondly, the nine LVDS trigger inputs have to be interpreted and used to control the DRS4 readout process.

### 6.4.1 Trigger Reference

The trigger reference DAC (DAC8560) uses an SPI-compatible serial interface that can operate at clock speeds of up to 30 MHz. This serial interface is implemented in VHDL code on the FPGA and a visual representation is shown in Figure 6.3.

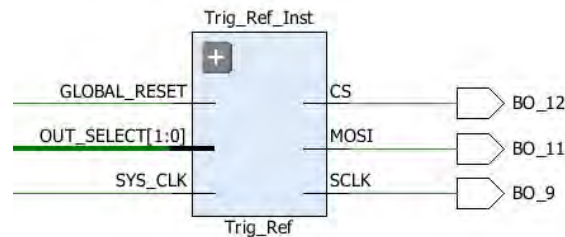


Figure 6.3: Instantiation of the SPI controller for the trigger reference

The controller has three inputs; a reset line, a clock line and a voltage selection logic vector. The reset line allows for an immediate asynchronous reset of the SPI controller including the SPI driver and the output selector. The 50 MHz input clock line is used to generate a 2.5 MHz SPI clock (SCLK) through a divisor of 20.

In a final flight-ready instantiation of the code, the voltage selection vector would represent the 16-bit word to be used for the DAC output. However, for testing purposes, only 2 bits are used to represent the output value, therefore constraining the output to four options. This is achieved with a simple case statement which uses two bits from the GPIO Core’s `gpio_out_tri_o` register as follows:

```

WHEN "00" => trig_value <= 16384;
WHEN "01" => trig_value <= 32768;

```

```

WHEN "10" => trig_value <= 49152;
WHEN "11" => trig_value <= 65535;

```

The statement is embedded in a process sensitive to the two `gpio_out_tri_o` bits, thereby loading the new DAC value as soon as a change in the bits is detected. The DAC is controlled with a single data input register and follows the format shown below, assuming the internal reference is enabled by default and left unmodified:

DB23																DB0								
0	0	0	0	0	0	0	PD	PD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							1	0																

Bit 16 and 17 control the operating mode of the device where “00” corresponds to regular operation and the remaining options are different power-down modes. Bits 0 - 15 represents the 16-bit value to be converted to an output voltage ranging from 0 - 2.5 V.

The three controller outputs are connected to the FPGA’s GPIO pins to communicate with the external DAC directly. A testbench was written to simulate the trigger reference controller and the results are shown in Figure 6.4. The initialization takes place from 0 - 10  $\mu$ s which sets the DAC to normal operation power mode with an output of 1.25 V (midway). At 15  $\mu$ s, the `OUT_SELECT` bits are changed and the DAC updates the output to 2.5 V (max value) and remains in regular power mode.



Figure 6.4: Simulation of the trigger reference initialization

### 6.4.2 Trigger Input

The detector contains nine fast-mode inputs, each representing a particle event when triggered. The comparators making the trigger decision have LVDS outputs which each contain two differential lines that require a 100  $\Omega$  termination near or in the FPGA.

Almost every pin pair on the Zynq can be used as a differential receiver, with only a few limited to single-ended applications. Moreover, the receivers can be configured for the LVDS\_25 I/O standard with an internal 100  $\Omega$  termination for optimal signal integrity. Each input pair (`TrigX_P` and `TrigX_N`) is connected to a differential input buffer (IBUFDS) to obtain a single-ended trigger signal within the FPGA fabric.

The trigger signal has to notify the SCA when to stop sampling but, because the trigger signal occurs at the beginning of the sampling process, an accurate delay

had to be incorporated. This delay is generated within the FPGA by counting the number of system clock rising edges since the asynchronous detection of the trigger signal.

Asynchronous detection was implemented for the detection of the trigger signal because in some cases, as seen at approximately 70 ns in Figure 6.5, the trigger signal can be much shorter than a single clock cycle. This figure shows an example of counting 15 rising edges which equates to 286 ns from when the trigger signal is received from the fast input to when the DRS4 is signaled to stop sampling.

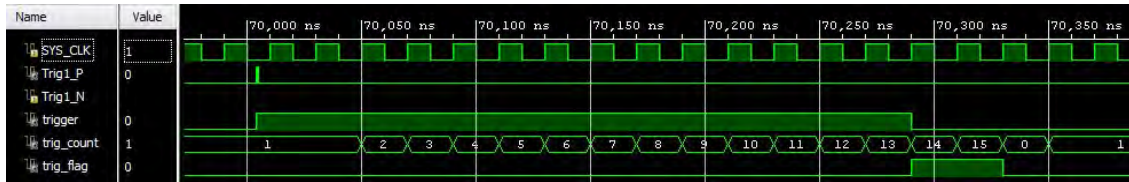


Figure 6.5: Simulation of the trigger delay process

## 6.5 Standard-Mode Input

### 6.5.1 First Stage Amplifier

The standard-mode input has two amplification stages with the first being a programmable differential amplifier. Through an SPI-compatible interface, operating between 10 - 50 MHz, the gain can be adjusted between 6 - 26 dB in 0.25 dB increments.

The controller for the first-stage amplifier requires initialization, as well as on-the-fly trimming to adjust the gain setpoint such that the full range of the digitizers is used. The FPGA-based controller consists of three inputs and three outputs, see Figure 6.6.

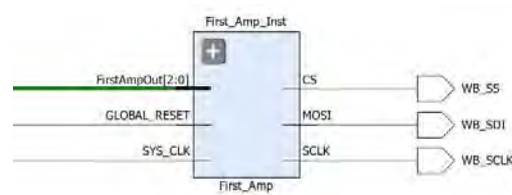


Figure 6.6: Instantiation of the SPI controller for the first stage amplifier

The inputs to the controller are very similar to that of the trigger reference controller, with the only difference being the length and purpose of the selection vector. Instead of controlling an output voltage, the selection vector controls the amplifier's gain.

The 16-bit SPI interface outputs were routed to each of the five dual amplifiers. Although the amplifiers are capable of operating at the input clock rate of 50 MHz, the SPI clock (SCLK) was reduced to the minimum rate of 10 MHz to ensure maximum signal integrity and reliability.

There are four data registers that need modification to initialize the device and make on the fly adjustments, namely power, channel and two gain registers, see Figure 6.7.

Table 5. Serial Word Format for Register 2: Power Control							
7	6	5	4	3	2	1	0
RES	RES	CHA1	CHB1	CHA2	CHB2	RES	RES
CHA1 and CHA2 = 0 for ON, CHA1 and CHA2 = 1 for OFF							
CHB1 and CHB2 = 0 for ON, CHB1 and CHB2 = 1 for OFF							

Table 6. Serial Word Format for Registers 3, 4: Gain Control							
7	6	5	4	3	2	1	0
RES	Gain = 26 — (register value * 0.25) valid range is 0 to 80						

Table 7. Serial Word Format for Register 5: Channel Control							
7	6	5	4	3	2	1	0
RES					SYNC	Load A	Load B

Figure 6.7: Serial registers for the LMH6882 programmable differential amplifier

The power register is critical for the overall design as each amplifier's power consumption during regular operation was around 1 W. The amplifiers are therefore only configured to power-on, via the serial interface, when absolutely necessary. A hex value of 0x00 is written to register 2 for regular operation and 0x3C is written for power-down mode.

The 7-bit gain control register actually specifies attenuation which means that a higher value corresponds to a smaller resultant gain. A hex value of 0x00 sets the gain to 26 dB and a value of 0x7F to 6 dB. The formula for the resultant gain is shown in Table 6 of Figure 6.7.

The dual-channel amplifier can adjust the gain of each channel individually or jointly. If the sync bit of register 5 is set, the gain indicated by register 3 will be loaded for both channels simultaneously. Alternatively, if the sync bit is cleared, the corresponding Load x bits are used to load the gain value for the relevant channel.

During initialization, the device is set to power-down mode, loaded with the minimum gains and set to load simultaneously. This process, as well as any subsequent updates, requires four 16-bit serial transmissions. As with the trigger reference, an update process is triggered by a change in the input vector. A flight-ready instantiation of the code would incorporate many different options, therefore requiring a 16 - 18 bit long vector, but for testing purposes only 3 bits from the GPIO Core's `gpio_out_tri_o` register were used to select between different modes and gains.

The five primary options tested were as follows:

```

WHEN "000" => Power-Down Mode
WHEN "001" => Gain = 25%
WHEN "010" => Gain = 50%
WHEN "011" => Gain = 75%
WHEN "100" => Gain = 100%

```

A testbench was written to simulate the controller's operation during initialization and a subsequent update to power up the device and set the gain to 50%, see Figure 6.8. The initialization took place from 0 - 115  $\mu\text{s}$  and the update from 150 - 265  $\mu\text{s}$ .

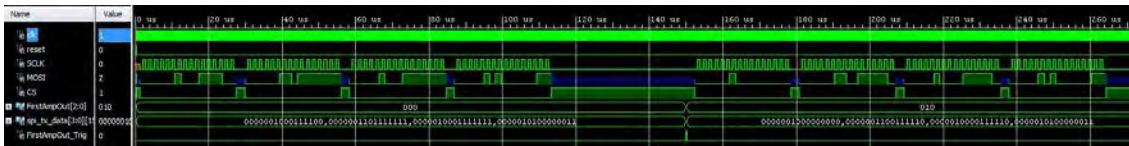


Figure 6.8: Simulation of the first stage amplification SPI controller

### 6.5.2 Second Stage Amplifier

The second stage amplifier provides a fixed 6 dB (factor of 2) of gain. Although not programmable, all nine of the second stage amplifiers can be enabled/disabled via a single line connected to the FPGA. Just as the first stage amplifiers would be controlled by the mission mode, so would the second amplifiers. For testing purposes, however, the enable line was connected to the shared register to allow user control of the amplifiers' power states:

```
BO_8 <= gpio_out_tri_o(5) // Second Amplifier Enable
```

## 6.6 DRS4

The Domino Ring Sampler v4 (DRS4), is a switched capacitor array (SCA) capable of sampling 9 independent analog waveforms at a rate of 700 MSPS to 6 GSPS. Each channel contains 1024 sampling cells that can be read out and digitized via a shift register at 33 MSPS. The following section describes the operation of the SCA and how it is coupled with the external digitizer.

### 6.6.1 DRS4 Serial Controller

The DRS4 has four analog input control voltages that are set via an external 16-bit, quad-output DAC. Each of the DAC's outputs can be individually adjusted from 0 to 2.5 V, in 38  $\mu\text{V}$  increments. The four analog voltages set the DRS4's input common-mode voltage (DRS4\_CM), the read offset voltage input (ROFS), the output offset voltage (O\_OFs) and the bias voltage for the internal buffers (BIAS). The details for each of these inputs can be found in Appendix C.5.

When using the DAC's internal voltage reference, its outputs are controlled with a single 24-bit register, via an SPI-compatible serial interface, as shown below:

DB23								DB12			
0	0	LD1	LD0	0	DAC Select 1	DAC Select 0	PD0	D15	D14	D13	D12
DB11								DB0			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The LDx bits determine when the outputs are updated and, to maintain independence, each output is chosen to update immediately once written to, without affecting the other outputs (LD1 = 0, LD0 = 1). The final control bit, PD0, sets the device's power mode. During particle detection the device is enabled (PD0 = 0) and disabled (PD0 = 1), along with the DRS4 and ADCs, once particle detection is complete.

A simulation of the DAC initialization during testing is shown in Figure 6.9. As this was a test case, the outputs were set to test the full-scale range of the device. Consequently, the four SPI transactions set the buffers for channel A to 0 V (0 % FSR), channel B to 0.83 V (33 %), channel C to 1.66 V (66 %) and channel D to 2.5 V (100 %). After each of the four SPI transactions, the corresponding channel's output was updated immediately.

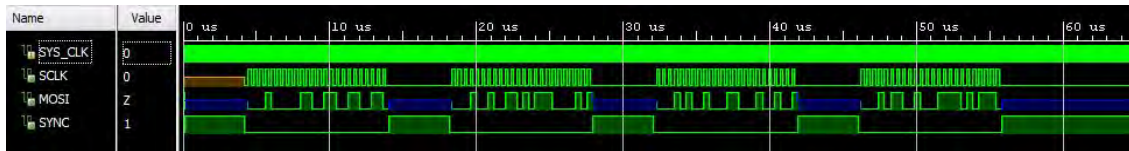


Figure 6.9: Simulation of the DRS4's DAC initialization

## 6.6.2 DRS4 Data Interface

The DRS4's data interface has to control the sampling process at the SCA's input and the analog output for further digitization. With the SCA's maximum analog sampling rate of 6 GSPS and the ADC digitization 14-bit word length, particle data could effectively be collected at a rate of 84 Gbit/s per channel. Therefore, using all 9-channels, the maximum effective input data rate is around 756 Gbit/s. Although the particle detector could only collect data in 1024-sample bursts, this impressive data input rate was possible primarily due to the DRS4 SCA and the time domain advantages it provides.

### 6.6.2.1 Sampling Process

The "Domino Ring" name originates from the on-chip inverter chain generating a frequency as high as 6 GHz, called the domino wave circuit. This domino wave runs continuously, propagating through the SCA, and produces a write signal for each of the sampling cells sequentially, allowing for the Gigahertz-level sample rates. The wave can be started by setting the DENABLE signal HIGH. For a sample to be stored in the storage cells, two conditions must be met: the domino wave must provide a HIGH signal and an external DWRITE signal must be set HIGH, see Figure 6.10.

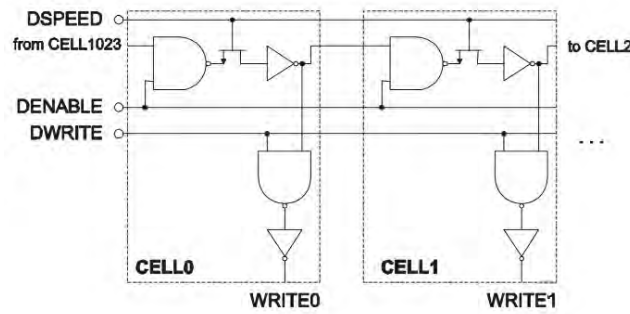


Figure 6.10: DRS4 sampling cell architecture[56]

Devices that offer high sampling frequencies ( $> 1$  GSPS) usually require complex clock generation and distribution. To avoid this, the DRS4 incorporates an internal PLL that multiplies the input frequency to the desired sampling rate. The internal PLL contains a PLLCK output that goes HIGH once the PLL has settled and locked on the frequency, indicating that the device is ready for sampling.

To generate an internal frequency of 2.048 GHz, a reference clock of 1 MHz is provided to the DRS4 SCA. This reference clock is generated by the FPGA by dividing its internal 50 MHz clock by 50 and driving the DRS4's LVDS lines with a differential output buffer. Despite the clock being less complex at 1 MHz, care was still taken with the generation and distribution as the input clock's jitter directly affects the sampling jitter.

The DRS4 has two modes of sampling, controlled with the DMODE signal. When DMODE is LOW, the domino wave only propagates through the sampling cells once and then stops. Subsequent propagation requires that DENABLE be toggled briefly which, unfortunately, induces some delay caused by the internal PLL having to re-lock. When DMODE is HIGH, the wave propagates indefinitely and the sampling process is controlled with the DWRITE signal only. Although the latter mode consumes marginally more power, it is used to avoid the startup delays.

It is important to note that the DENABLE and DWRITE signals have to be kept LOW until the power-supply voltages stabilize to avoid the DRS4 entering a mode in which it draws large amounts of current. Although the FPGA could be set to use an internal pull-down, the I/O pins contain a default pull-up during the startup phase. Therefore, to avoid this undesirable current mode, external pull-down resistors were added.

### 6.6.2.2 Full Readout Mode

Once a trigger signal has been obtained via the FPGA, the sampling process is stopped and the readout process begins. The readout process uses a read shift register to clock out the content of the sampling cells to individual outputs. This process is carefully coordinated with the attached ADC to ensure effective digitization. It is also possible to read out only a portion of the waveform, rather than all 1024 sampling cells, thereby reducing the digitization time.

The DRS4 contains four configuration registers, accessible via a 4-bit selection register (A3 - A0). The selection register controls the input decoder and output multiplexer of the configuration registers, see Figure 6.11. In addition to controlling the configuration registers, the 4-bit selection register is also used to select different channels and modes.

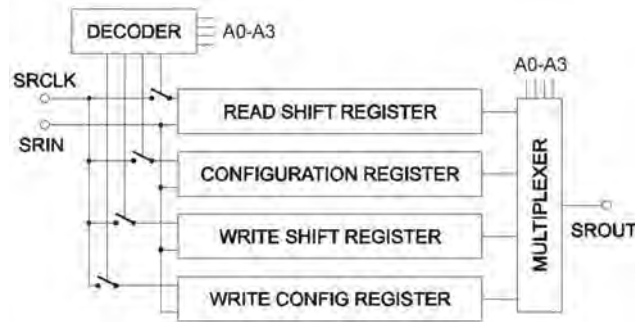
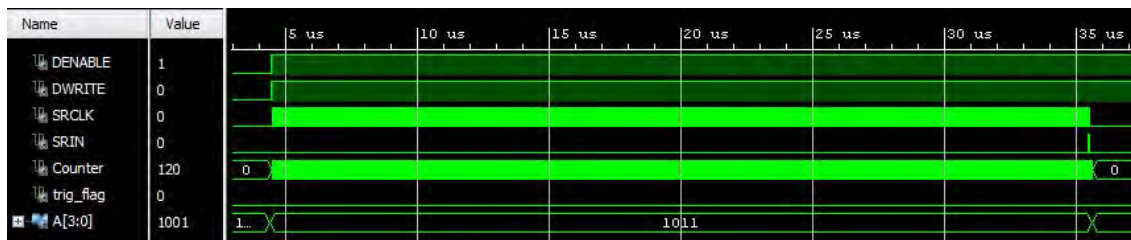
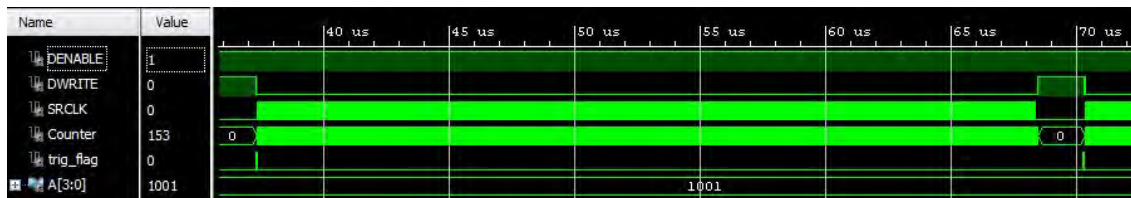


Figure 6.11: Diagram of the four configuration registers and their access mechanism[56]

To initialize the Read Shift Register, a “1” is clocked into the first register. This is achieved through selecting the Read Shift Register, by setting  $A = 1011$ , and issuing 1024 SRCLK cycles during the last of which SRIN is set HIGH. At this stage, the output reflects the contents of the first cell, see Figure 6.12a. To complete a full-readout of the cells, another 1023 SRCLK clock cycles have to be issued where each clock produced the next sample at the output. One additional clock cycle has to be issued to wrap the read bit from the last cell back to the first cell, see Figure 6.12b.



(a)



(b)

Figure 6.12: Simulation of the DRS4 initialization (a) and full readout (b)

### 6.6.2.3 Readout Clock Generation

Although the DRS4's readout clock, SRCLK, supports a maximum output rate of 40 MSPS, a rate of 33 MSPS was chosen for regular operation because the DRS4's datasheet specified this value for "optimal performance". The quality of the clock signal strongly affects the DRS4 and subsequent ADCs' noise performance. Therefore, the Zynq's dedicated MMCME2 clocking primitive is used to generate a low-jitter, high-quality clock signal.

The MMCME2 primitive supports clock network deskew, frequency synthesis and jitter reduction. In order to make use of these features, however, the internal voltage controlled oscillator (VCO) had to conform to the following constraints:

$$F_{VCO} = F_{CLKIN} \times \frac{M}{D}$$

and

$$600MHz \leq F_{VCO} < 1200MHz$$

where  $M$  corresponds to the `CLKFBOUT_MULT_F` setting and  $D$  to the `DIVCLK_DIVIDE`.

When the clock primitive is used for frequency synthesis, the output frequency can be calculated as follows:

$$F_{OUT} = \frac{F_{VCO}}{O}$$

where  $O$  corresponds to the `CLKOUT_DIVIDE` setting.

Using an input clock of 50 MHz and `CLKFBOUT_MULT_F` => 33.000, `DIVCLK_DIVIDE` => 2 and `CLKOUT_DIVIDE` => 25.000, the resultant  $F_{VCO}$  was 825 MHz and  $F_{OUT} = 33$  MHz. This provided the exact frequency required to drive the sampling process and the frequency of the voltage controlled oscillator was well within its limits.

During the readout process, the DRS4 outputs analog samples which the ADC has to digitize. Precise synchronization between the two devices is required to ensure that the analog samples are digitized at the right moment. With reference to Figure 6.13, the time from the rising edge of SRCLK to the time the analog sample begins to appear at the output,  $t_0$ , is approximately 10 ns. At this stage the analog sample requires additional time to settle at the output. The optimal time,  $t_s$ , before sampling the analog output from the corresponding rising edge is 38 ns.

Based on a 33 MSPS output rate, and a delay of 38 ns, the ADC digitization clock has to be offset by 455.04 degrees. As the offset is greater than 360 degrees, and therefore greater than one clock cycle, an equivalent offset of 95.04 degrees is used. To demonstrate this, consider that the rising edge, labeled "1" in Figure 6.13, corresponds to sample 1,  $s_1$ , but is only digitized 38 ns later which is halfway through the subsequent clock cycle's rising edge. The timing mechanism had to be accurate enough such that the sample could be digitized as long after it appeared at the output as possible but before the next sample appeared.

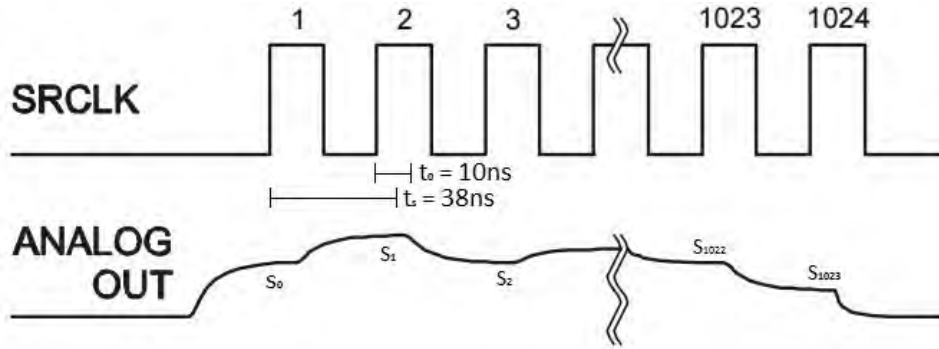


Figure 6.13: Timing diagram for the ADC sampling process[56]

The ADC clock is generated by the same MMCME2 primitive used for the SRCLK clock, with the above-mentioned phase shift. One constraint for the phase shift, imposed by the clock primitive, is that it has to be a multiple of  $45 / \text{CLKOUT1\_DIVIDE}$ . With `CLKOUT1_DIVIDE` set to 25, the phase shift had to be a multiple of 1.8, allowing the closest match of 95.4 degrees.

Finally, to lower the skew and duty cycle distortion and to improve the jitter tolerance, a global buffer primitive (BUFG) was added to the output of the MMCME2 clock generator. The buffer then drove six differential LVDS output clock drivers (OBUFDS), one for the DRS4 and five for the ADCs.

#### 6.6.2.4 Transparent Mode

To test the overall design, the DRS4 was placed in transparent mode for initial testing by setting  $A = 1010$ . In this mode, the signal at the input of the DRS4 is immediately available at its output. Although this mode does not provide any speed advantages, it allows for digitization of the signal at the maximum conversion speed of the external ADC. The data could then be validated to ensure all the biasing, common-mode adjustments etc. were working as expected. The transparent mode also allowed for triggering and post-trigger digitization, allowing for more FPGA code validation.

## 6.7 ADC System

The overall function of the FPGA-based ADC system controller is to initialize and set up the five dual-channel ADCs and read in the digitized data. The ADC system consists of two components; an SPI controller for initialization and a high-speed data interface.

### 6.7.1 ADC Serial Controller

The LTC2265-14 uses a 16-bit, SPI-compatible serial interface for initialization that can operate at speeds of up to 25 MHz. Once the initialization process is complete, the ADCs do not need any further instruction unless the system is reset.

The initialization process is concerned with the four registers, shown below:

REGISTER A1: FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h)							
D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_2	X	X	NAP_1
REGISTER A2: OUTPUT MODE REGISTER (ADDRESS 02h)							
D7	D6	D5	D4	D3	D2	D1	D0
ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE2	OUTMODE1	OUTMODE0
REGISTER A3: TEST PATTERN MSB REGISTER (ADDRESS 03h)							
D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST	X	TP13	TP12	TP11	TP10	TP9	TP8
REGISTER A4: TEST PATTERN LSB REGISTER (ADDRESS 04h)							
D7	D6	D5	D4	D3	D2	D1	D0
TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

Figure 6.14: List of primary ADC registers[57]

The format and power-down register is used to set the power state of the ADCs as well as the output data format. There is no need to control the power state of the two channels individually and they are therefore set to either normal (000) or sleep (1xx) mode. Furthermore, the data format was set to offset binary for initial testing.

For the output mode register, the default settings are used for the LVDS output current (3.5 mA) and internal termination (disabled). More importantly, however, the ADC is configured for 1-lane, 14-bit serialization by setting the OUTMODE bits to “101”, see Figure 6.15.

The choice of 1-lane mode was driven by the number of FPGA pins available. With five dual-channel ADCs, 1-lane mode required 20 differential lines (40 I/Os) whereas 2-lane mode would require 30 differential lines (60 I/Os). Given the limited number of FPGA I/O pins accessible via the board-to-board connectors, and that the trigger signals already occupied 18 of those, 1-lane mode was the only feasible option.

Furthermore, as FPGAs are not governed by multiples of bytes, the most efficient way to transfer the 14-bit data value was with 14-bit serialization. The alternative option was using 16-bit serialization which contained the same 14-bit value with two extra zeroes appended, resulting in an unnecessary increase in data rate for the same amount of resultant data.

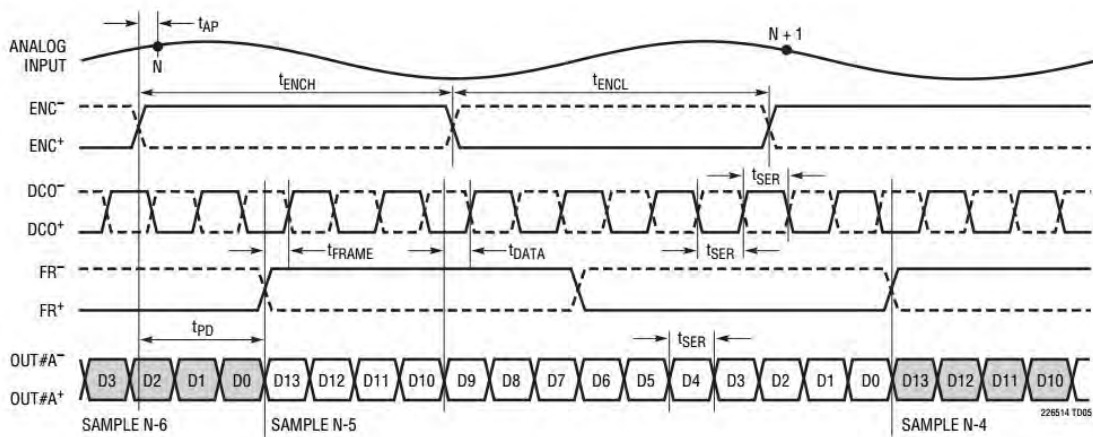


Figure 6.15: Example of 1 lane, 14-bit mode at the ADC output[57]

Thus far, these settings could have been achieved using the simple parallel programming mode, negating the need for serial initialization. However, parallel programming mode was unable to provide a digital output test pattern, required to align the bits in the FPGA. To enable and setup a custom test pattern, the test pattern MSB and LSB registers were modified. Bits 0 - 5 of register A3 set the test pattern's MSB (101101) and bits 0-7 of register A4 the LSB (10110111). Bit 7 of register A3 was set to enable the test pattern (and to start the FPGA training) and cleared to revert back to real data. The training, or bit alignment process, is discussed in more detail in the next subsection.

Once the FPGA is trained to accept aligned data from the ADC, the SPI interface is not used until the system is reset. Figure 6.16 shows a simulation of the ADC's SPI interface during initialization.

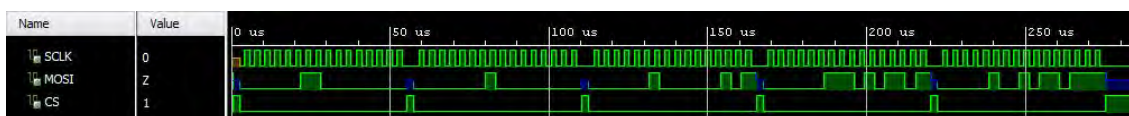


Figure 6.16: Simulation of the ADC SPI controller initialization

## 6.7.2 ADC Data Interface

### 6.7.2.1 ADC Clock Input

The ADC's output clock sets the rate at which data is digitized, and starts a conversion on every rising edge. This output clock is generated and controlled by the DRS4 Data Interface due to the tight coupling and synchronization between the two devices. The frequency of the clock is set to 33 MHz to obtain optimal performance from the DRS4. This rate, by design, falls perfectly within the ADC's frequency range of 5 to 65 MSPS.

### 6.7.2.2 ADC Data Outputs

Using the ADC in 1-lane, 14-bit serialization mode, shown in Figure 6.15, each of the five ADC data interfaces consists of two sets of differential data outputs (ADC1 and ADC2), a differential clock output (DCO) and a differential frame output (FR). Based on a 33 MSPS sampling rate ( $f_S$ ), the frequency of the different outputs are as follows:

Data Output	(ADCx)	$14f_S$	= 462 MHz
Clock Output	(DCO)	$7f_S$	= 231 MHz
Frame Output	(FR)	$f_S$	= 33 MHz

These input data rates are well within the FPGA's I/O speed limitations which range between 950 and 1250 MB/s, depending on the Zynq's speed grade.

### 6.7.2.3 FPGA Data Inputs

All the ADC data outputs are read as LVDS inputs with internal termination in the Zynq's high-range (HR) I/O banks. Before the signals are routed to their deserialization and bit alignment processes, differential buffer primitives are used to support the LVDS\_25 I/O standard as well as the internal termination.

The ADCx data inputs are passed through an IBUFDS primitive that uses complimentary outputs (IBUFDS\_DIFF\_OUT). The requirement for the differential output are imposed by the subsequent deserialization process. Similarly, each of the ADC clock inputs (DCO) are passed through an IBUFDS primitive, but the subsequent bit alignment process does not require differential outputs. The ADC frame inputs (FR) initially used the IBUFDS\_DIFF\_OUT primitive for buffering but the signal was later completely removed for reasons discussed next.

### 6.7.2.4 SERDES

The original deserialization technique was achieved through first principles, as shown in Figure 6.17, and used the ADC data, clock and frame lines.

The deserialization began with a DDR block that clocked out the value of the data line at either the rising or falling edge of the clock. The outputs of the DDR block were then fed to two chains of flip-flops (one associated with the rising-edge and the other with the falling edge) that moved the data bit down the chain on each new clock cycle. The output of the DDR block and all the subsequent flip-flops were fed into the final 14-bit output register, resulting in a deserialized word that was clocked out with the ADC frame line.

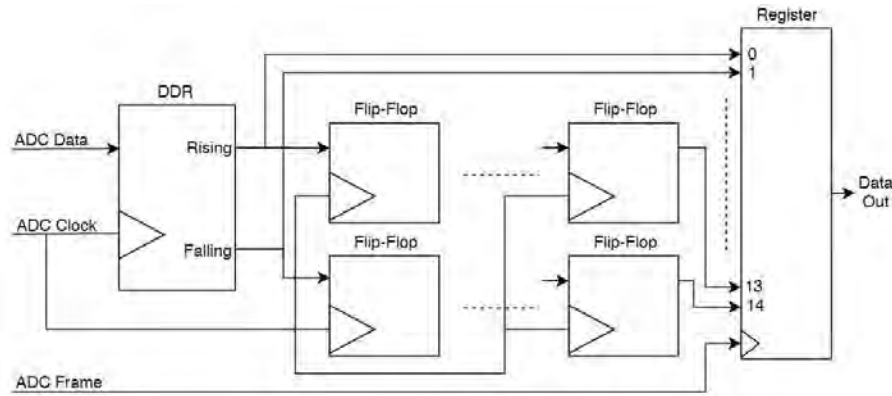


Figure 6.17: Original deserialization technique used for the ADC data

This method was shown to work and the relevant VHDL code is included in the suite of software. However, there was a more efficient method that was discovered later which reduced the resource utilization and maintained good performance:

Each I/O tile <sup>1</sup> contains dedicated hardware resources that add functionality, such as double-data rate operation and programmable input delays, without using any additional FPGA resources. Most importantly, however, one such function is a dedicated serial-to-parallel converter (ISERDESE2) with specific clocking and logic resources that can facilitate the implementation of high-speed source-synchronous applications, see Figure 6.18.

The ISERDESE2 module supports DDR-mode signals and, when two I/O tiles are combined, 10- or 14-bit wide words can be deserialized. The module also includes a built-in bitflip submodule that allows for the input data stream to be reordered. This reordering process can be used to train the ISERDESE2 module to lock onto a training pattern output by the ADC.

For 14-bit serialization, two ISERDESE2 modules are used, configured in DDR-mode with a data-width of 14. The interface type is set to “Networking” which is the only option that allows the desired data width. A re-aligned differential ADC clock is used to drive the module’s complementary clock inputs (CLK and CLKB). Similarly, a re-aligned, single-ended ADC frame clock is used to drive the module’s divided clock input (CLKDIV). The “re-alignment” aspect is discussed in the next subsection.

The first ISERDESE2 module is configured as the master and uses the positive-end of the differential ADC data lines as the serial data input. The module’s outputs, Q1-Q8, represent the first 8 bits of the deserialized word. The second module is configured as the slave and uses the negative-end of the differential ADC data lines as the serial data input. The slave module’s outputs Q3-Q8 represent the remaining 6 bits of the serialized word. For the two modules to work in unison, the master module has two shift register outputs connected to the slave module.

<sup>1</sup>An I/O tile is an individual block associated with each I/O pin, containing dedicated hardware resources

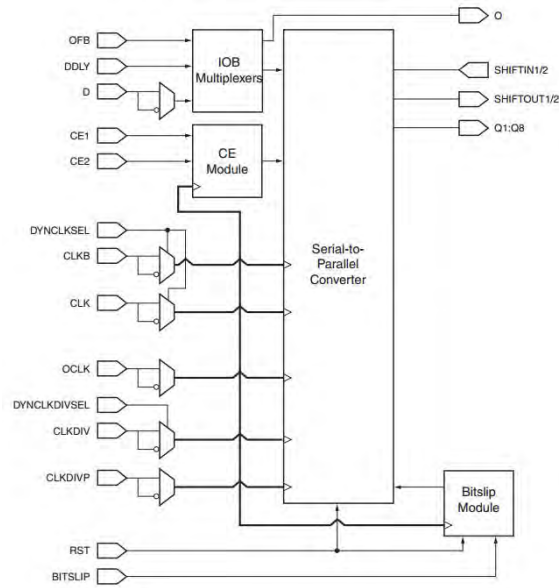


Figure 6.18: Diagram of the ISERDESE2 module embedded in each Zynq I/O tile[55]

Finally, the bitslip inputs are controlled by an external process which re-orders the input data stream. This process is described in an upcoming subsection.

#### 6.7.2.5 Clock Realignment

The ISERDESE2 module requires that the ADC bit (DCO) be realigned such that it is  $90^\circ$  out-of-phase with the ADC data (ADCx) and frame clock (FR). Furthermore, instead of trying to realign the frame clock with bit clock using picosecond-level delay taps, the frame clock is regenerated from the realigned bit clock instead. The following methodology was originally described in Xilinx's XAPP524 application note[58].

Figure 6.19 shows a functional diagram of the clock realignment process. The ADC bit clock (DCO) is first fed through a IDELAYE2 block set to variable mode and is controlled by the bit clock state machine. Using an internally generated clock reference of 200 MHz, the IDELAYE2 block has 32 taps of 78 ps each. Subsequently, the new reconstructed bit clock (BitClock) is realized with an IBUFIO primitive and the new frame clock (FrameClock) with a BUFR primitive that implements a divisor of 7. The resultant BitClock is therefore simply a delayed version of the original DCO signal.

The DCO input is also applied to the D input of an ISERDESE2 module, located in the same I/O tile as the IDELAYE2 primitive. The new bit and frame clock is routed to the module's CLK and CLKDIV inputs respectively. This implementation results in the DCO signal registering itself in the ISERDESE2 module using a delayed version of itself, allowing the position of the rising and falling edges of the DCO signal to be determined.

There are three ISERDESE2 output cases that are addressed to align the input DCO clock to the newly generated bitclock, namely:

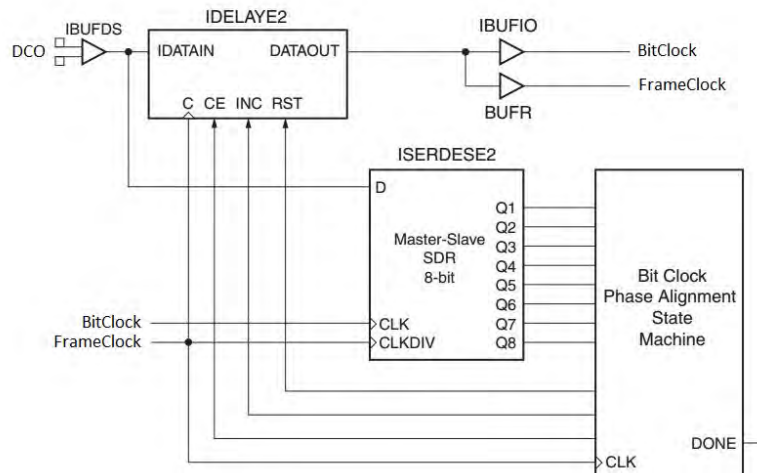


Figure 6.19: Functional overview of the clock realignment[58]

1. The output contains seemingly random data and changes on every clock cycle.
2. The output is all '1's
3. The output is all '0's

The first case occurs when the two clocks are already phase-aligned and the random nature is caused by the clock jitter in the crossover region. Although phase-aligned, it is still unclear if the new bit clock is aligned to the input clock's rising or falling edge. To determine the clock edge the IDELAYE2 delay tap is temporarily decreased. A change in the ISERDESE2 output to all '1's indicates that the new bit clock's rising edge is aligned to the original clock's falling edge. Conversely, a change to all '0's indicates that the new bit clock's rising edge is aligned to the original clock's rising edge.

The second case occurs when the rising edge of the bit clock corresponds to the LOW region of the original clock. By reducing the IDELAYE2 delay tap until the ISERDESE2 output becomes unstable, or all '0's, the bit clock is aligned to the original clock's rising edge.

The third, and final, case occurs when the rising edge of the bit clock corresponds to the HIGH region of the original clock. By reducing the IDELAYE2 delay tap until the ISERDESE2 output becomes unstable, or all '1's, the bit clock is aligned to the original clock's falling edge.

To implement this process, the output of the ISERDESE2 module is fed into a bit clock state machine which, in turn, alters the magnitude of the delay employed by the IDELAYE2 module.

#### 6.7.2.6 Bitslipping

The bitslip process is quite a lot simpler than the clock realignment due to the functionality provided by the Zynq's hardware resources. Instead of relying on the frame signal from the ADC being perfectly aligned with the data after the PCB

routing, FPGA fabric routing and buffering, the ISERDESE2’s bitslip submodule is used. The submodule assumes that data is being collected from the ADCs, via the ISERDESE2 module, and allows an incorrect, or non-existent, frame reference.

A rising-edge on the bitslip slip (an input on the ISERDESE2 module) triggers a bitslip operation, synchronous to the re-aligned frame clock (CLKDIV). A bitslip operation effectively results in the output word shifting in a barrel-shifter manner. In DDR-mode this is achieved by alternating the output pattern by shifting right by one and shifting left by three.

A custom bitslip process was written which monitored the ISERDESE2 module’s 14-bit output word and compared it to a training pattern generated by the ADC. At start up, the ADC is configured to output a 14-bit, non-ambiguous training pattern (10110110110111) for this purpose. The bitslip process compares the two values and asserts a bitslip command to the ISERDESE2 module until the values match. At this time the bitslip process’s job is complete and the ADC returns to regular sampling mode.

### 6.7.2.7 Simulation

Figure 6.20 shows a simulation of the overall ADC data interface. The ADC input data (Diff\_Data) is shown along with the reconstructed bit and frame clocks. The bitslip lock indicator, Bitslip Lock, is also shown and goes HIGH at approximately 2,035 ns showing that the ADC input data has been correctly re-ordered.



Figure 6.20: Simulation of data interface and bitslipping

## 6.8 Memory Controller

The data collected by the FPGA, from the ADC, has to undergo low-level processing after which it can be transferred to the processing system for higher-level processing. In order to share the information between the FPGA and processor, the data is stored in RAM accessible by both technologies.

### 6.8.1 FPGA Data Writing

A VHDL process was written to store data directly to block RAM (BRAM) after low-level processing. The BRAM generator interface consists of an enable line, an address register, a data register and a clock signal. It is configured as “True Dual Port RAM” which allows multi-processor storage and uses the default 32-bit read and write data widths. Furthermore, the data depth is set to the minimum setting of 2048 for each channel which only uses 2 of the 140 36 KB BRAMs available.

The storage process begins by waiting for the bitslip indicator to signal that the subsequent data is valid and correctly organized. The ISERDESE2's output is routed to the BRAM data register and the re-aligned bit clock to the BRAM's clock signal. To start writing to the RAM, the enable line is brought HIGH and an address, starting at 0 and ending at 1023, is fed to the BRAM. This process is repeated for every new particle event.

During bench testing, the process was modified to a “single-shot” mode where a user could issue a command to collect and store a single 1024-bit sample for debugging purposes.

### 6.8.2 Processor Data Reading

Unlike the FPGA, the processor cannot communicate with the BRAM directly and therefore requires an AXI Interconnect. Furthermore, an AXI BRAM controller is used to handle the clocking and communication protocol between the processor and the BRAM itself, see Figure 6.21.

The BRAM Controller uses the AXI4 Protocol with a default 32-bit data width. In addition to providing an AXI-to-BRAM interface, the controller also provides ECC functionality which allows the AXI master to detect and correct single and double bit errors in the BRAM block. Once implemented, the processor can access the data as if the BRAM was an internal register.

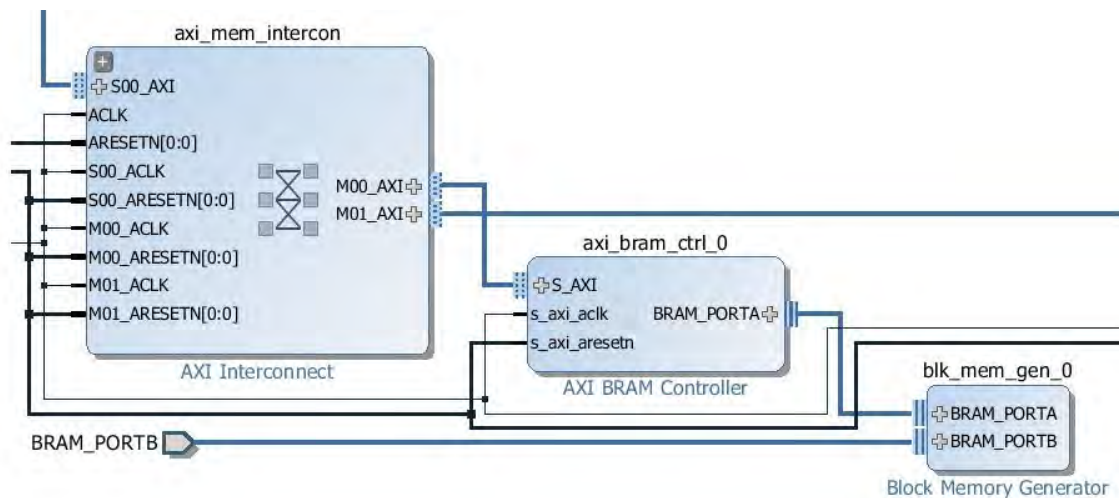


Figure 6.21: Diagram of the block memory generator IP

### 6.8.3 Simulation

Figure 6.22 shows a simulation of the data storage process in the FPGA when used in debug mode. Once the memory request is received from the user at  $4.5 \mu\text{s}$ , and the bitslip indicator is HIGH, data is stored sample-by-sample until all 1024 14-bit values have been stored (for each channel).

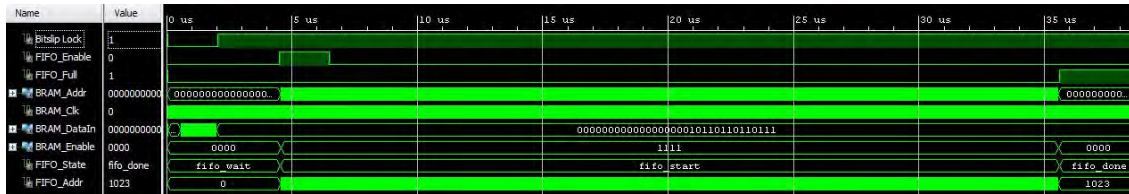


Figure 6.22: Simulation of the ADC sample storage process

## 6.9 System on Chip

### 6.9.1 Processing System

The Xilinx Zynq XC7Z020's processing system is used as a standalone, low-level processor that provides functions such as caches, interrupts and exception as well as features such as external I/Os and hardware peripherals. Figure 6.23 shows a block diagram of the Zynq processing system implemented within the Vivado toolset. The block contains all the processor's configuration data such as clocking resources, fixed I/O mapping, peripherals etc.

Once the bitstream hasz been generated in Xilinx, the hardware files were exported to SDK where a board support package was created. This board support package was then used to further develop basic C code which was later compiled with the *arm-xilinx-eabi-gcc* compiler.

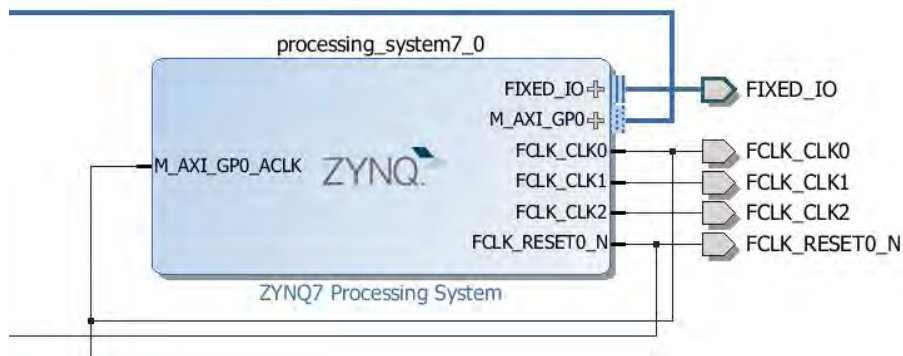


Figure 6.23: Block diagram of the ZYNQ7 processing system implemented in Vivado

### 6.9.2 UART

Although the final particle detector only requires one hardware UART instantiation, both the UART0 and UART1 peripherals were enabled. This decision was motivated by the custom particle detector board using UART1 and the original development board using UART0. By enabling both, the Trenz TE0720 daughter board could be plugged into either carrier board and still provide a UART interface. Both UART peripherals were configured to operate at a baud rate of 115200. UART0 utilized MIO pins 14 and 15 and UART1 pins 12 and 13.

### 6.9.3 AXI Master

The Advanced eXtensible Interface (AXI) protocol is part of ARM Advanced Microcontroller Bus Architecture (AMBA) and provides a high-speed, high performance interconnect between the FPGA and processor. The general purpose AXI master interface 0 (M AXI GP0 interface) was enabled on the Zynq's processing system, thereby allowing the interconnection of the aforementioned AXI BRAM and GPIO Controllers.

### 6.9.4 Booting

The SoC was configured as a low-level standalone processor and therefore did not require booting from an SD card. Consequently, the processing system was configured to boot from Quad SPI flash which required MIO pins 1 - 6 for the single speed SPI connection and pin 8 for the feedback clock.

From within SDK, a boot image (BOOT.bin) was created that contained the the FPGA bitstream, the first stage bootloader (FSBL) and the standalone processor code. The boot image ensured that when powered up, the bitstream was programmed onto the FPGA and the processor executed the relevant C code.

### 6.9.5 Clocking

Ciiva's SIT8008AI SiTime MEMS oscillator was used to generated a 33.333333 MHz clock reference. The oscillator has a stability of  $\pm 50$  ppm and feeds the processor's PS\_CLK clock pin. From this input, two internal PLLs are used to generate the operational clocks for the processor and FPGA. The first PLL is used to multiply the reference clock by 20 to generate a clock of 666.6 MHz for the ARM processor and AXI interface.

The second PLL is used to generated three fabric clocks for the FPGA:

1. FCLK\_CLK0 => 50 MHz
2. FCLK\_CLK1 => 100 MHz
3. FCLK\_CLK2 => 200 MHz

Three clocks are necessary to support all the VHDL code discussed previously, ranging from clock realignment and bitslipping to SPI controllers and ADC readout.

# Chapter 7

## Results

### 7.1 SiPM Sensor Testing

#### 7.1.1 Testing Environment

All PCB assembly and rework conformed to IPC's J-STD-001ES, and more specifically to Class 3 standards and the space addendum. Furthermore, all necessary ESD precautions were taken during assembly, rework and testing to conform to QS.0026 & ANSI S20.20 standards. This constrained all work to moderate room temperatures and a relative humidity between 30 - 70 %. When the humidity dropped below 30 %, an air ionizer was used to mitigate triboelectric charging issues.

All the equipment used during testing had been calibrated and their descriptions and model numbers are listed below:

Table 7.1: List of testing equipment

<b>Description</b>	<b>Brand</b>	<b>Model</b>
Triple-output 30 V, 5 A DC power supply	BK Precision	1671A
6j Digit, Truevolt digital multimeter	Keysight	34460A
1 GHz, 5 GSPS, Mixed signal oscilloscope	Tektronix	MSO 4104B-L
1.5 GHz Single-ended, active probe	Tektronix	TAP1500
1.0 GHz Single-ended, passive probe	Tektronix	TPP1000
20 MHz Function/arbitrary waveform generator	Keysight	33220A
2 GHz Analog RF signal generator	Keysight	E4420B

#### 7.1.2 SiPM Power Supply

##### 7.1.2.1 Visual Inspection

The simple digitally-adjustable SiPM power supply, as well as the fully-integrated version, were both received as bare circuit boards from the PCB fabrication house. Before assembly began, the bare boards were inspected under a microscope to check for any defects. Once assembled, the boards were inspected again for any potential problems such as solder bridges, misaligned components etc.

Figure 7.1 shows images of the simple and fully-integrated circuit boards after assembly. Both boards passed the initial inspection without any concern.

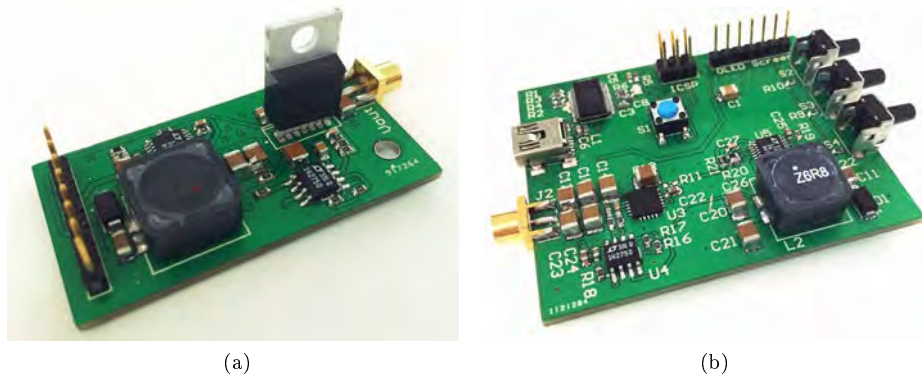


Figure 7.1: Image of the simple (a) and integrated (b) SiPM power supply and the output display (c)

### 7.1.2.2 Test Procedure

Both of the SiPM power supplies used the same voltage generation and regulation components and therefore only one was thoroughly tested and documented. The test procedure began by powering the supply with 5 V and taking the ENABLE line HIGH. Once powered, the following procedure was followed:

Table 7.2: Test procedure for SiPM power supply

#	Procedure	Result	Expected	Min	Max
1	Measure LT3579 output voltage	32.05 V	32 V	31 V	33 V
2	Measure FAULT output	5.02 V	5.00 V	4.95 V	5.05 V
3	Measure TPS7A33 output	22.38 V	22.40 V	22.00 V	22.50 V
4	Run voltage profile script		See note below		
5	Measure TPS7A33 output		See note below		
6	Bring ENABLE line LOW	-			
7	Measure LT3579 output voltage	0 V	0 V		
8	Measure TPS7A33 output	0 V	0 V		

The SiPM power supply performed as expected without any issues. Figure 7.2 shows an example output message on the SiPM's OLED display indicating the output voltage, the voltage regulator's temperature and the status of the supply.



Figure 7.2: Image of the OLED display during the test procedure

**Note:** A script called “SiPM\_Supply\_Tester.ino” stepped through the full range of the power supply’s output voltages, starting at 22.5 V and ending at 31.0 V in 500 mV steps. To obtain a specific voltage, a value of 0 - 1023 had to be written to the current-output DAC. This was achieved with the following formula:

$$DAC = \frac{V_{desired} - V_{min}}{V_{step}} = \frac{V_{desired} - 22.4}{(V_{max} - V_{min})/1023}$$

The power supply’s output voltage was monitored with a bench-top multimeter, showing a constant offset of 200 mV across the output’s full range. For example, when a voltage of 25.00 V was requested, the resultant output was 24.80 V. This offset indicated a small error in the DAC value calculation and could easily be corrected through calibration.

### 7.1.3 Breakout Boards

The breakout boards were received as bare PCBs and had to be assembled by hand. The initial visual inspection of the circuit board showed no evidence of bulging, cracking or other damage. The first step in the assembly process was preparing the SiPM for the reflow oven, see Figure 7.3a. After reflow, the board was visually inspected again and the remaining components were soldered by hand.

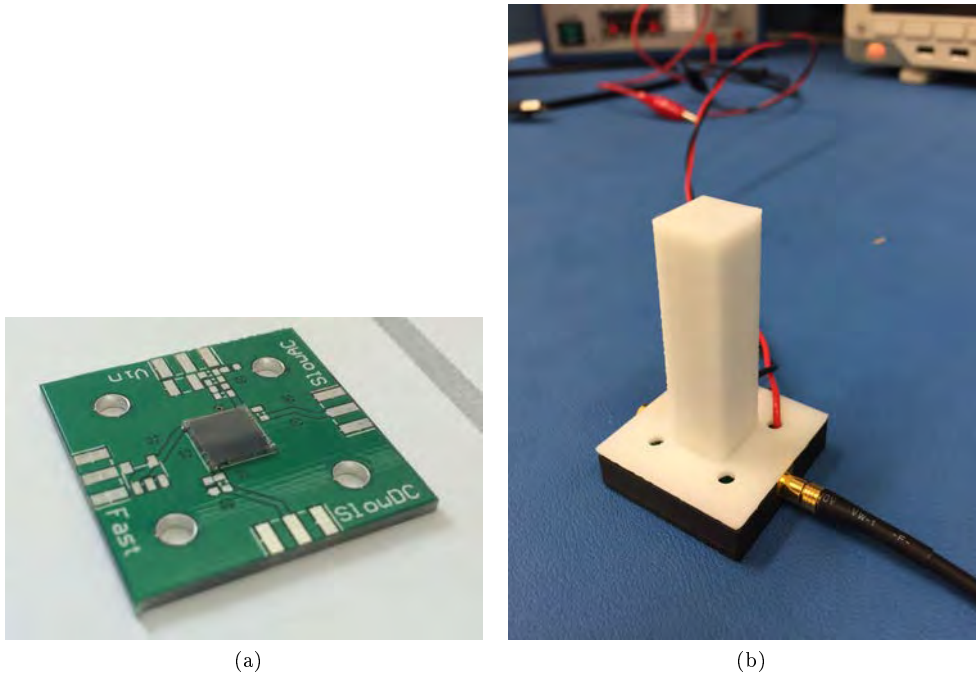
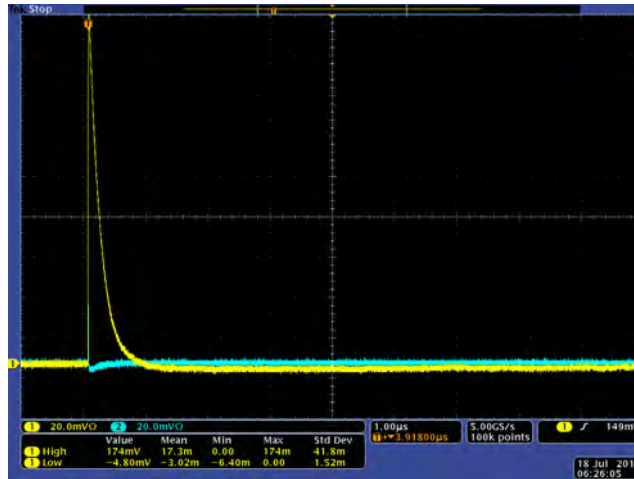


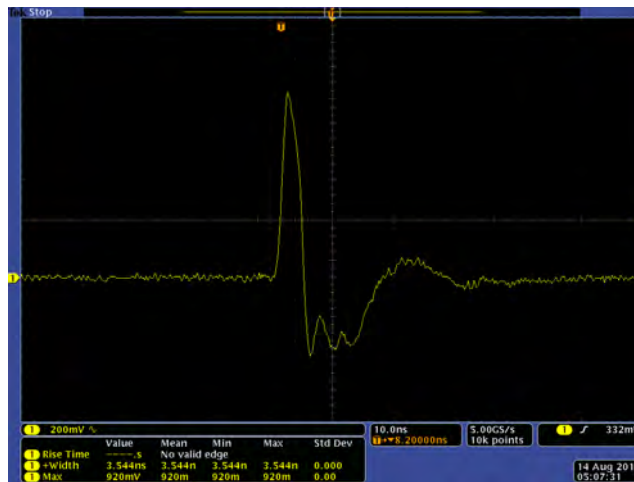
Figure 7.3: Image of the SiPM breakout board after the reflow process (a) and once ready for testing (b)

To test for correct operation, the circuit board was placed in a 3D printed enclosure, see Figure 7.3b. The SiPM was biased with  $-27.5$  V and the fast and slow outputs were monitored on an oscilloscope. Figure 7.4a shows the two signals on the same time and amplitude scale for comparison purposes.

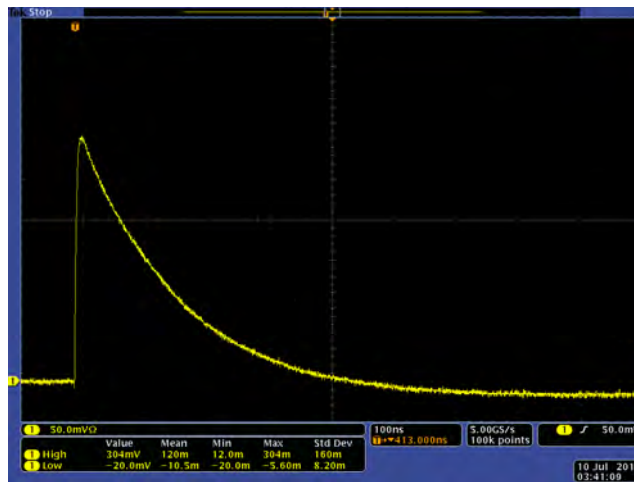
Figure 7.4b shows an individual fast-mode pulse that has a rise-time of approximately 2 ns and a total duration of 5 ns. Similarly, Figure 7.4c shows an individual standard-mode pulse that has an equally fast rise time but a much longer decay and an overall duration of hundreds of nanoseconds.



(a)



(b)



(c)

Figure 7.4: SiPM output signals during testing

### 7.1.4 PSD Comparison

During the initial design phase the optimal sampling rate of the SiPM's standard output was unknown. In order to begin the detector design, the optimal sampling rate was determined by comparing the figure of merits (FoM) at different rates. These tests were performed by University of Cape Town's physics department using an encapsulated EJ301 liquid scintillator optically coupled to an ETL 9214B series photomultiplier negatively biased at 950 V. The photomultiplier's output (anode) was connected to a 2-channel, 10-bit CAEN Vx1761 digitizer.

Figure 7.5 shows the counts versus the ratio of the long and short integrals output by the photomultiplier for events within a specific energy range. This particular test was concerned with neutrons (left) and gamma-rays (right). A higher FoM corresponded to a better detector, as discussed in Chapter B. At 250 MSPS the FoM was 1.73, at 500 MSPS 1.92, at 1 GSPS 2.25 and at 4 GSPS 2.80. In order to maintain a FoM greater than 2, a minimum sampling frequency of 1 GSPS was defined as a requirement.

## 7.2 SiPM Digitizer Testing

### 7.2.1 Visual Inspection

The SiPM Digitizer was received in a fully-assembled state with the exception of a few basic components. The first test process involved inspecting the circuit board under a microscope for any evidence of bulging, cracking or other damage to the circuit board or components. Furthermore, the ICs were checked for correct alignment and any solder bridges across adjacent pins.

Figure 7.6 shows a selection of images obtained from the microscope during inspection. Figure (a) shows the DRS4 switched capacitor array, (b) a second-stage fixed-gain amplifier, (c) a first-stage programmable amplifier, (d) a dual-channel ADC, (e) the input protection diode and a load switch and (f) the fast-mode wideband amplifier. There was no sign of any potential issues.

### 7.2.2 Power Supplies

Each power supply contained a "Do Not Place" resistor in series with its output which meant that the "fully-assembled" circuit board's power supplies were all disconnected from their respective loads. This allowed for each supply to be tested for correct functionality before the subsequent, sensitive circuitry was powered.

#### 7.2.2.1 1.8 V Supply

The 1.8 V supply was used to power the ADCs and could be controlled via the FPGA. The first step in testing the 1.8 V supply was ensuring that the +5 V supply operated correctly (see later subsection). The next steps in the test procedure are tabulated below:

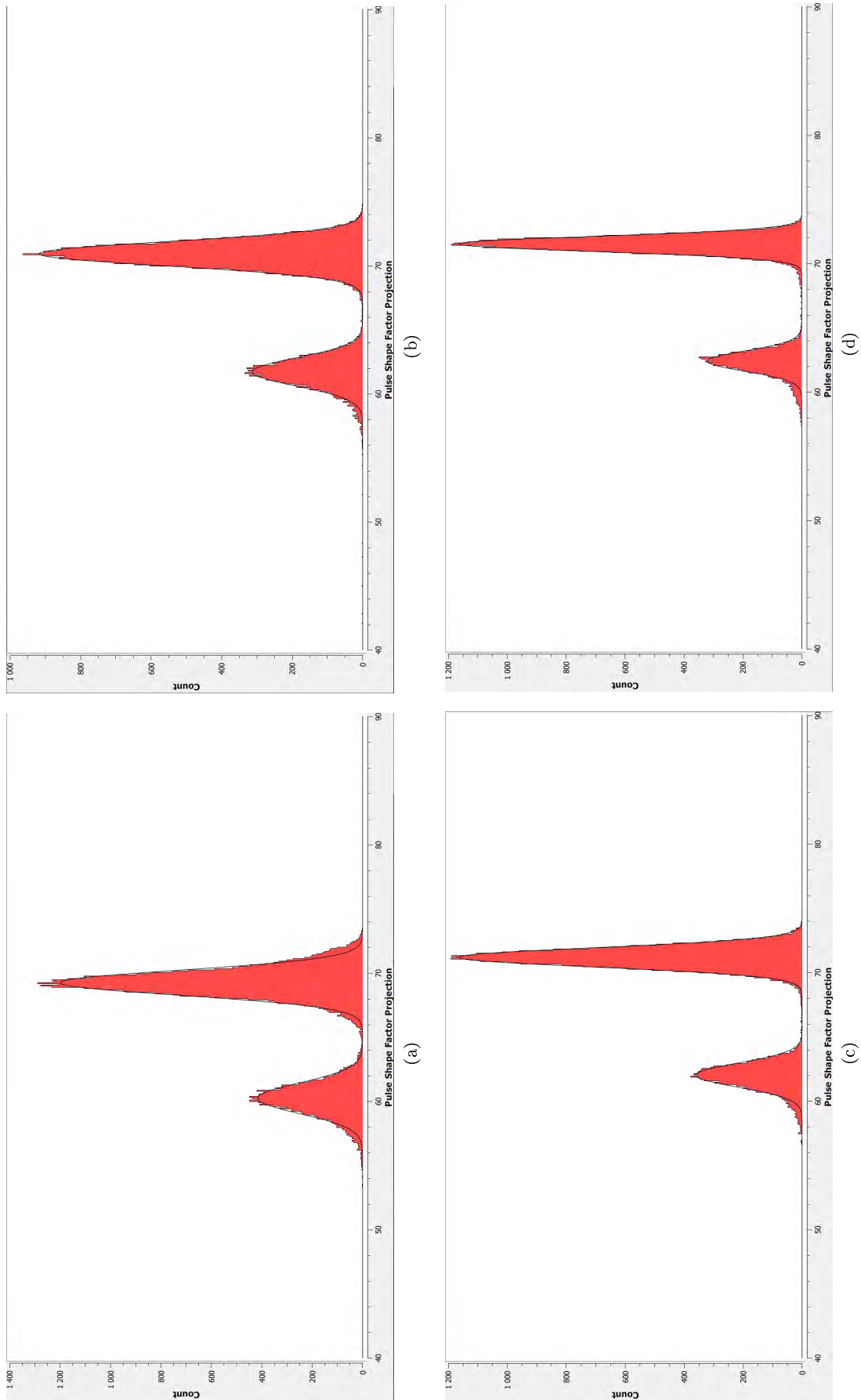


Figure 7.5: PSD comparison at 250 MSPS (a), 500 MSPS (b), 1 GSPS (c) and 4 GSPS (d)

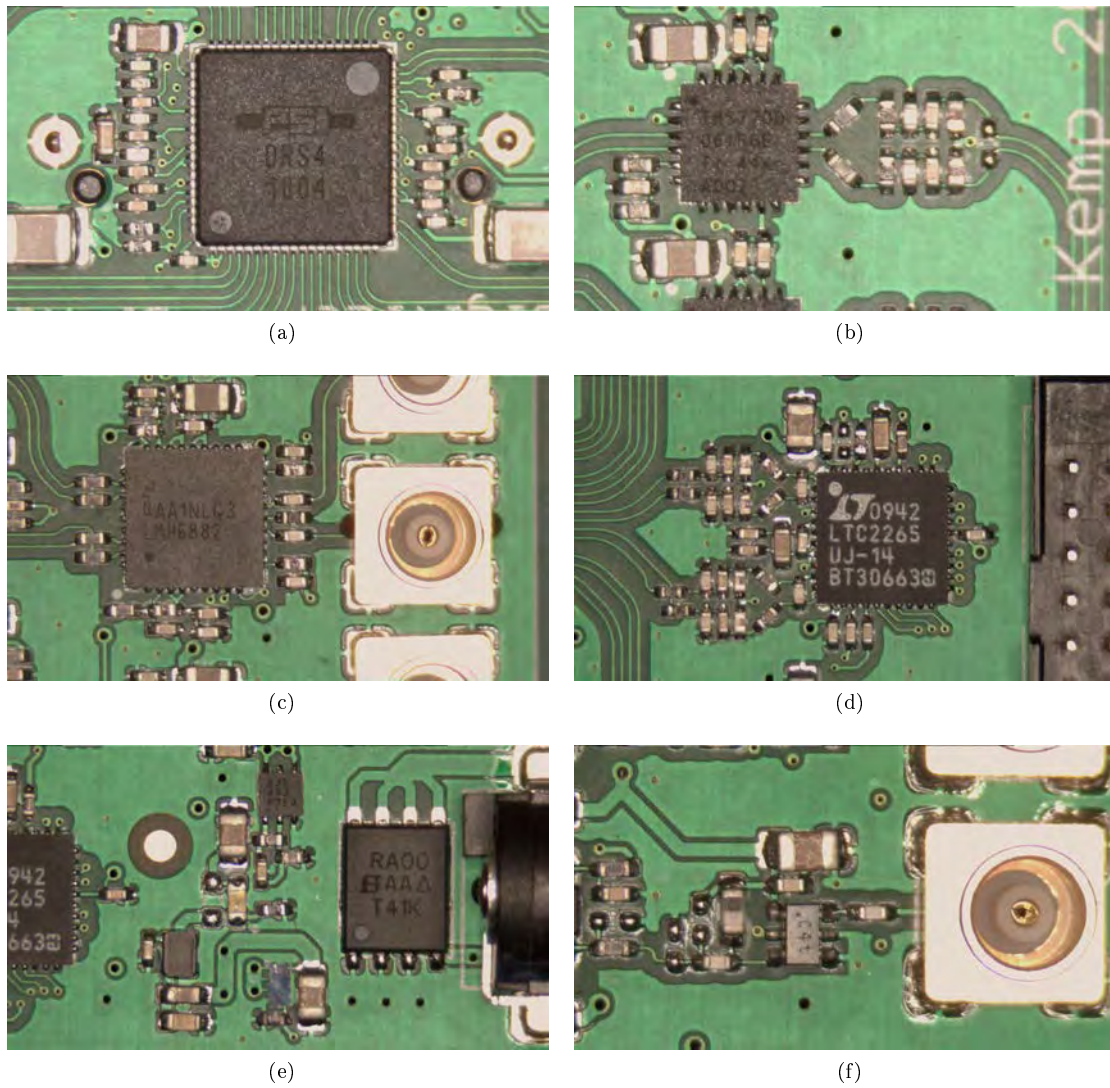


Figure 7.6: Images from microscope during visual inspection

Table 7.3: Test procedure for 1.8 V power supply

#	Procedure	Result	Expected	Min	Max
1	Manually connect +1.8V_EN net to +5 V	-			
2	Check status of +1.8 V LED	Off		On	
3	Replace LED		See note below		
4	Check status of +1.8 V LED	On		On	
5	Check output voltage at DNP resistor	1.787 V	1.80 V	1.78 V	1.82 V
6	Place 0R resistor	-			
7	Check +1.8V output voltage	1.786 V	1.80 V	1.78 V	1.82 V
8	Disconnect +1.8V_EN net from +5 V	-			
9	Using SoC, issue "1.8V Enable" command	1.786 V	1.80 V	1.78 V	1.82 V
10	Using SoC, issue "1.8V Mode 0" command	1.786 V	1.80 V	1.78 V	1.82 V
11	Using SoC, issue "1.8V Mode 1" command	1.786 V	1.80 V	1.78 V	1.82 V
12	Using SoC, issue "1.8V Disable" command	0 V	0 V		

**Note** During the 1.8 V supply testing, procedure item #2 failed because the LITE-ON LED, used as an indicator, had a forward voltage greater than 1.8 V. To rectify this issue, the LED was replaced with a different LED that offered a lower forward voltage. Once replaced, the 1.8 V supply worked as expected and did not dissipate a considerable amount of heat when enabled.

### 7.2.2.2 2.5 V Supply

The particle detector consisted of three 2.5 V supply rails, each with their own purpose. The supplies were all tested independently.

**General 2.5 V Supply:** The first of the 2.5 V supplies to be tested was the permanently enabled, general 2.5 V supply that provided power to the FPGA's I/Os as well as the digital 2.5 V line. The following test procedure was carried out:

Table 7.4: Test procedure for general 2.5 V power supply

#	Procedure	Result	Expected	Min	Max
1	Complete +5 V Testing	-			
2	Check status of +2.5V LED	On		On	
3	Check output voltage at DNP resistor	2.501 V	2.50 V	2.48 V	2.52 V
4	Place 0R resistor	-			
5	Check +2.5V output voltage	2.482 V	2.50 V	2.48 V	2.52 V
6	Check the four VCCIO_xx voltages	2.482 V	2.50 V	2.48 V	2.52 V

All the voltages were within the criteria set for the test parameters, however, the final 2.5 V output was very close to the minimum specification. Although adequate, if this became a problem, the voltage could be increased by replacing the voltage-setting resistor with a more appropriate value.

**Digital 2.5 V Supply:** The next power supply tested was the digital source, which could be controlled by the FPGA, and provided power to digital circuitry on the particle detector. The test procedure followed is tabulated below:

Table 7.5: Test procedure for digital 2.5 V power supply

#	Procedure	Result	Expected	Min	Max
1	Complete +5 V Testing	-			
2	Manually connect +2.5VD_EN net to +5 V	-			
3	Check +2.5VD output voltage	2.48 V	2.50 V	2.48 V	2.52 V
4	Disconnect +2.5VD_EN net from +5 V	-			
5	Using SoC, issue “2.5VD Enable” command	2.48 V	2.50 V	2.48 V	2.52 V
6	Using SoC, issue “2.5VD Disable” command	0 V	0 V		

The output voltage only just met the minimum specification, mainly due to the preceding general 2.5 V supply being too low. The digital 2.5 V supply consisted only of a load switch, rather than a regulator. Therefore, to improve the output voltage, the preceding regulator would have to be corrected.

When the digital 2.5 V supply was enabled, a large increase in current (0.36 A to 1.5 A) was noticed on the external power supply caused by the DRS4 entering an undesirable state at startup. This issue was attributed to VHDL code operating incorrectly and, once fixed, the current dropped down to approximately 0.4 A.

**Analog 2.5 V Supply:** The last of the 2.5 V supplies was the low-noise, analog source. The analog supply required that the +5 V be operational before testing could begin. The test procedure followed is tabulated below:

Table 7.6: Test procedure for analog 2.5 V power supply

#	Procedure	Result	Expected	Min	Max
1	Manually connect +2.5VA_EN net to +5 V	-			
2	Check status of +2.5VA LED	On		On	
3	Check output voltage at DNP resistor	2.495 V	2.50 V	2.48 V	2.52 V
4	Place 0R resistor	-			
5	Check +2.5VA output voltage	2.490 V	2.50 V	2.48 V	2.52 V
6	Disconnect +2.5VA_EN net from +5 V	-			
7	Using SoC, issue “2.5VA Enable” command	2.490 V	2.50 V	2.48 V	2.52 V
8	Using SoC, issue “2.5VA Disable” command	0 V	0 V	-	-

The analog power supply worked without any issues and all measurements were nominal.

### 7.2.2.3 3.3 V Supply

The 3.3 V supply provided power only to the FPGA and had to be permanently enabled. The regulator took the raw battery input voltage and generated a 3.3 V power line capable of supplying up to 4 A. The test procedure followed is tabulated below:

Table 7.7: Test procedure for 3.3 V power supply

#	Procedure	Result	Expected	Min	Max
1	Connect 8V to V <sub>b+</sub> input	-			
2	Check status of +3.3V LED	On		On	
3	Check output voltage at DNP resistor	3.29 V	3.3 V	3.27 V	3.33 V
4	Place 0R resistor	-			
5	Check +3.3V output voltage	3.29 V	3.3 V	3.27 V	3.33 V
6	Sweep input voltage from 6.5 - 15 V	-			
7	Check +3.3V output voltage	Short	3.3 V	3.27 V	3.33 V

The initial testing of the 3.3 V supply passed all the criteria with excellent results. However, during procedure #7 the voltage regulator short circuited the output to ground when the input voltage exceeded 10 V. The regulator was permanently damaged during this event and the short across the output remained even when the input voltage was reduced back down to 6.5 V.

The exact cause of this failure is unknown because the regulating IC was designed to handle input voltages above 15 V. The most likely explanation is that a capacitor with a lower voltage rating was placed at the input of the regulator. The PCB utilized both 10 V and 25 V 10  $\mu$ F capacitors and a mistake could have been made during the assembly process. Replacing the BGA component was too risky due to the sensitive components adjacent to the regulation circuitry and, therefore, an external 3.3 V supply was used to power the rail directly instead.

#### 7.2.2.4 5 V Supply

**Main Regulator:** The final power supply to be tested was the 5 V supply and the 5 V load switch. The main switch-mode regulator was designed to source 12 A to the FPGA and various other circuitry. The test procedure followed is shown below:

Table 7.8: Test procedure for 5 V power supply

#	Procedure	Result	Expected	Min	Max
1	Connect 8V to V <sub>b+</sub> input	-			
2	Check status of +5V <sub>filt</sub> LED	On		On	
3	Check output voltage at DNP resistor	5.166 V	5 V	4.9 V	5.1 V
4	Place 0R resistor	-			
5	Check +5V <sub>filt</sub> output voltage	5.146 V	5 V	4.9 V	5.1 V
6	Sweep input voltage from 6.5 - 15 V	-			
7	Check +5V <sub>filt</sub> output voltage	5.146 V	5 V	4.9 V	5.1 V

The 5 V supply operated correctly but produced a voltage 66 mV greater than the specified maximum, caused by a slightly sub-optimal standard resistor value used for the voltage-setting divider. Although this problem could be easily fixed, the 5 V supply was left as is for further testing as all the relevant components were tolerant above 5.5 V.

**Load Switch:** The 5 V load switch, which selectively provided power to certain components, followed a similar test procedure, shown below:

Table 7.9: Test procedure for 5 V load switch

#	Procedure	Result	Expected	Min	Max
1	Complete +5V_filt Testing	-			
2	Manually connect +5V_EN net to +5 V	-			
3	Check +5V output voltage	5.135 V	5 V	4.9 V	5.1 V
4	Disconnect +5V_EN net from +5 V	-			
5	Using SoC, issue “5V Enable” command	5.135 V	5 V	4.9 V	5.1 V
6	Using SoC, issue “5V Disable” command	0 V	0 V	-	-

Once again, the output voltages exceeded the specified maximum for the same reasons stated above.

**Power Analysis:** The +5 V load switch controlled power to the various components used during data acquisition. Due to the very large overall power consumption, the current requirements imposed by each set of components were plotted on a pie chart, see Figure 7.7. It is clear from the chart that the first-stage amplifier (LMH6882), the second-stage amplifier (THS770006) and the wideband amplifier (BGM1013) account for the large majority of the total current with 40 %, 33 % and 23 % respectively.

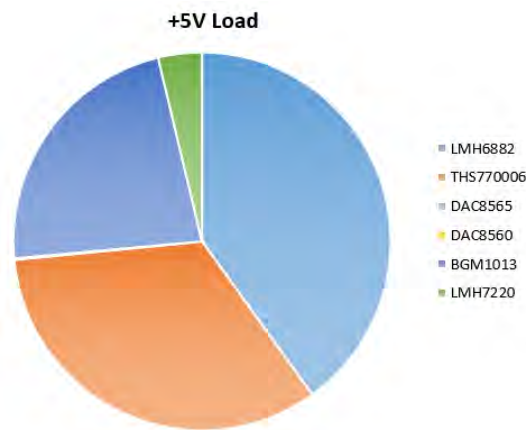


Figure 7.7: Pie chart showing the itemized +5 V current consumption

## 7.2.3 Fast-Mode Input

### 7.2.3.1 Wideband Amplifier

The wideband amplifier was a simple device to test as it contained only an input, for the SiPM’s fast output, and an output, for further triggering. The test began by sending the “5 V Enable” command from a computer to the SoC which enabled

the +5 V supply. The amplifier’s supply voltage was measured and fell within the acceptable range defined earlier. A sample pulse signal was fed into the amplifier’s input, RFin, and the output, RFout, was monitored on an oscilloscope using a 50  $\Omega$  terminated, single-ended active probe.

Figure 7.8 shows a pulse generated by the silicon photomultiplier due to a cosmic ray (muon) event<sup>1</sup> and the amplifier’s resultant output. The overall gain from 20 mV to 950 mV is approximately 47.5 (33.5 dB) which is less than the anticipated gain of 60 (35.5 dB) . This apparent loss was attributed to an impedance mismatch caused by an additional 50  $\Omega$  load introduced by the probe because, theoretically, two parallel 50  $\Omega$  loads will result in a load reflection coefficient of 0.3 and a return loss of 9.54 dB. Additionally, the gain at frequencies under 100 MHz is not well defined, as shown in the Chapter 4.2.2, and the signal generated by the cosmic event has a pulse duration of 20 ns, almost 10 times slower than the trigger signal expected from gamma or neutron particle event.

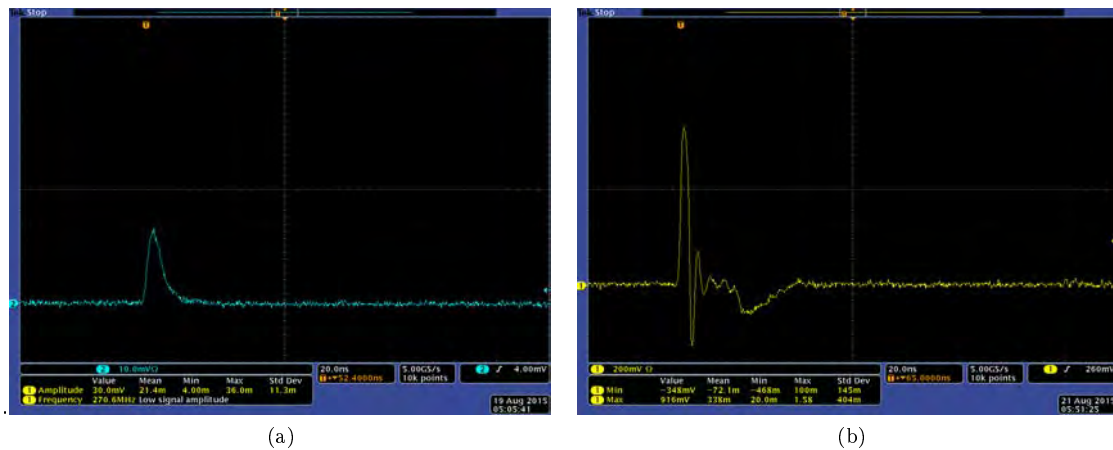


Figure 7.8: Waveform of wideband amplifier’s input (a) and output (b)

### 7.2.3.2 Trigger Reference

During the initial testing of the trigger reference DAC, the results were variable and inconsistent. This inconsistency was caused by the logic level mismatch between the FPGA (2.5 V) and the DAC (5 V). This result was not unexpected and the SPI voltage level translator (TXB0104), that was originally accommodated for, was added to the circuit board via hand soldering.

Once the level translator had been installed, testing started by enabling the +5 V and +2.5 VD lines via the SoC with the “5 V Enable” and “+2.5VD\_EN” commands, respectively. The 16-bit trigger reference DAC was ready for testing which followed the procedure tabulated below:

<sup>1</sup>About 10,000 muons reach every square meter of the earth’s surface in a minute and have a unique pulse shape signature

Table 7.10: Test procedure for trigger reference DAC

#	Procedure	Result	Expected	Min	Max
1	Using SoC, issue “Level Shift Enable” command	-			
2	Using SoC, issue “Trigger Mode 0” command	-			
3	Measure DAC Vout	0.622 V	0.625V	0.620 V	0.630 V
4	Measure Trig_Ref output voltage	0.493 V	0.3125V	0.310 V	0.315 V
5	Using SoC, issue “Trigger Mode 1” command	-			
6	Measure DAC Vout	1.247 V	1.250 V	1.245 V	1.255 V
7	Measure Trig_Ref output voltage	0.793 V	0.625V	0.620 V	0.630 V
8	Using SoC, issue “Trigger Mode 2” command	-			
9	Measure DAC Vout	1.872 V	1.875 V	1.870 V	1.880 V
10	Measure Trig_Ref output voltage	1.098 V	0.9375V	0.935 V	0.940 V
11	Using SoC, issue “Trigger Mode 3” command	-			
12	Measure DAC Vout	2.497 V	2.500 V	2.495 V	2.505 V
13	Measure Trig_Ref output voltage	1.404 V	1.250V	1.247 V	1.253 V

The Trig\_Ref output was consistently higher than expected where it should have been exactly half the Vout value due to the resistor divider network. It seemed as though one, or multiple, of the trigger comparators was pulling the line up to the 5 V supply line through a resistor value of approximately 120 k $\Omega$ . By removing the 0  $\Omega$  series resistors between the Trig\_Ref output and the comparator’s input, the voltage after the resistor divider represented the correct/expected voltage. This indicated that one, or more, of the comparators were damaged.

This damage could be explained by one of two possible events. The first is that a comparator may have been damaged through an electrostatic discharge (ESD). The comparator’s input had an ESD protection diode connected to the positive supply rail. If the ESD limit was exceeded, this diode may have created a permanent resistive path to the 5 V supply rail. The second possibility is that the inputs may have been exposed to a slight negative transient during testing, causing one of the input transistors to latch up. Due to the high-speed nature of the device, the input transistors are very sensitive to small reverse voltages.

The faulty comparator was found through individual testing and replaced by hand rework and soldering. To test the comparator, the DAC reference was set to 1.25 V and a 20 MHz square wave, with a peak-to-peak voltage of 2.5 V, was applied to the non-inverting input. Figure 7.9 shows the resultant output at the positive and negative differential outputs. Note that the common-mode output voltage is around 1200 mV, as expected.

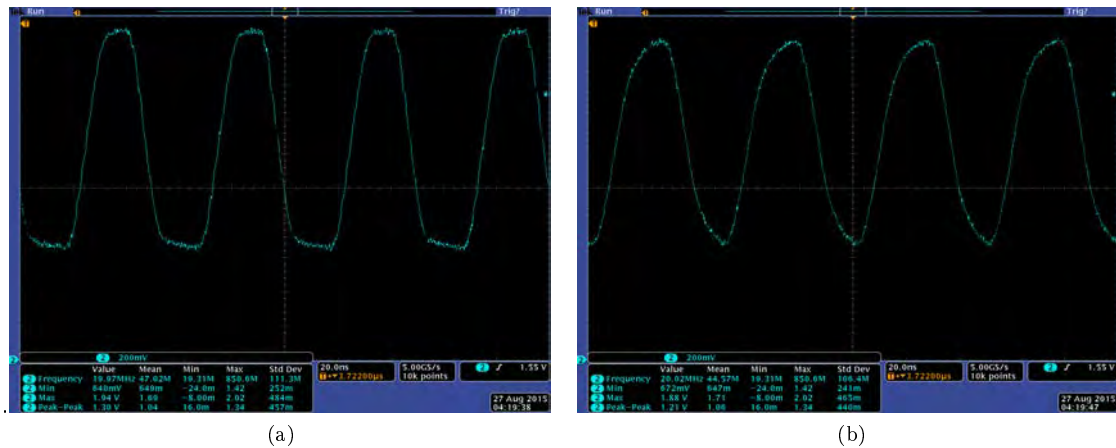


Figure 7.9: Waveform of trigger comparator's positive (a) and negative (b) differential outputs

Figure 7.10a shows the SPI transaction between the FPGA and the trigger reference DAC during initialization. The 24-bit word enables the DAC and sets the output to midway ( $V_{out} = 1.25$  V). Figure 7.10b shows the SPI transaction when the “Trigger Mode 3” command is issued by the FPGA. The new 24-bit word leaves the device enabled but sets the output voltage to the maximum value of 2.5 V.

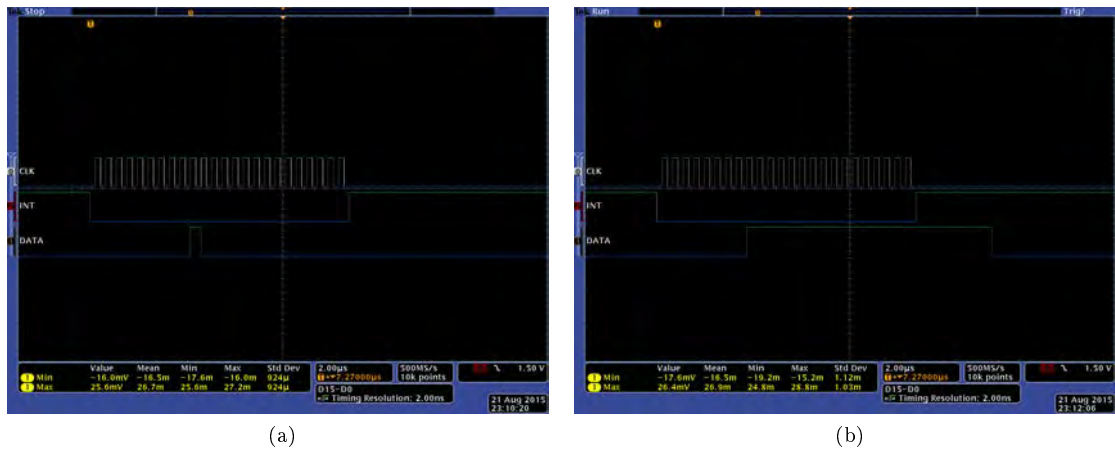


Figure 7.10: Waveforms of the trigger reference SPI transactions

## 7.2.4 Standard-Mode Input

The standard-mode signal chain consisted of two amplifier stages, analog memory and a digitizer. Each aspect of the signal chain is addressed individually after which waveforms are presented in Section 7.2.4.3.

### 7.2.4.1 First Stage Amplifier

The first stage amplifier had a programmable gain of 6 to 26 dB in 0.25 dB steps, adjustable via an SPI interface. In order to test the amplifier, the “5V Enable” and “2.5VA Enable” commands were issued to enable the +5 V and analog 2.5 V supply rails respectively. Once enabled, the voltage at the amplifier’s OCM pins were measured to ensure that common-mode output voltage was set correctly. OCMA measured 1.243 V and OCMB 1.244 V which was within 7 mV of the desired 1.25 V setpoint and was considered adequate.

The next step of the test was to ensure that the FPGA could adjust the amplifier’s gain via the SPI interface. To do so, the “Amp Mode x” command was issued via a computer to the SoC which, in turn, triggered the relevant SPI transactions. Figure 7.11a shows the SPI waveform in response to the “Amp Mode 0” command which puts the amplifier in standby mode and disables the outputs. Figure 7.11b shows the SPI waveform in response to the “Amp Mode 4” command which enables the amplifier and sets the gain to the maximum setting of 26 dB.

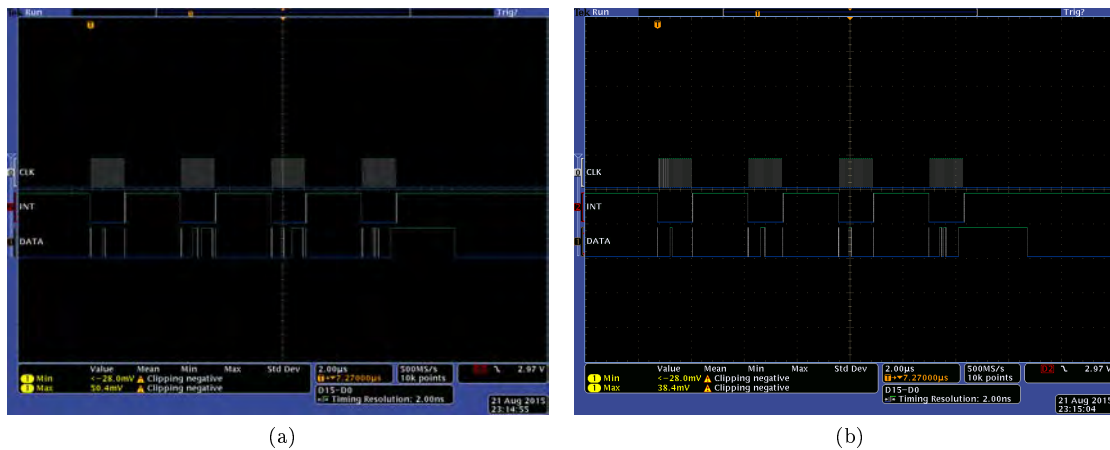


Figure 7.11: Waveform of SPI commands controlling the first-stage amplifier

Finally, a 20 MHz sine wave, with an amplitude of 100 mV and positive offset of 50 mV, was fed into one of the standard input channels. The peak-to-peak resultant output was monitored at the output of the amplifier for 6 dB, 13 dB, 19 dB and 26 dB. Since only one of the differential lines could be measured with a single-ended probe, it did not make sense to compare the output to the input because (1) the introduction of a 50  $\Omega$  load due to the probe would result in an impedance mismatch and (2) the signal would represent half of the full differential signal. Instead, the output was compared to itself for different gain values:

Table 7.11: Table of gain vs. peak-to-peak values

Gain	Peak-to-Peak
6 dB	168 mV
13 dB	264 mV
19 dB	584 mV
26 dB	1150 mV

These results suggested that the amplifier was working correctly as the peak-to-peak voltage increased when the gain value increased. More specifically, however, as the gain increased by a factor of approximately 2 (6 dB) so did the peak-to-peak output voltage. The resultant waveforms are presented in a later subsection.

#### 7.2.4.2 Second Stage Amplifier

The second stage amplifier provided a fixed 6 dB gain, when enabled via the FPGA. The amplifier's common-mode output voltage was determined by the voltage applied to its OCM pin and measured 2.44 V which closely matched the desired 2.50 V setpoint. The voltage on the OCM had to be maintained within the operating range of 2.25 V to 2.75 V and the exact value was not critical because of the subsequent filter and re-biasing network.

With the first stage gain set to 6 dB, the same 20 MHz sine wave applied to the standard-mode input. Once again, the values obtained at the outputs were not compared to the input but rather to itself while varying the first-stage gain. The following table summarizes the peak-to-peak voltages measured at the output of the first stage amplifier, the second stage amplifier and the re-biasing network:

Table 7.12: Table of gain vs peak-to-peak values at different stages

Gain	First Stage	Second Stage	Re-Biasing
6 dB	168 mV	280 mV	272 mV
13 dB	264 mV	488 mV	472 mV
19 dB	584 mV	1140 mV	1060 mV
26 dB	1150 mV	2245 mV	2230 mV

The gain between the first stage and the second is approximately 6 dB for each gain value tested. The slight loss of signal magnitude can be attributed to the impedance mismatch caused by probe loading. There is very little loss between the second stage amplifier and the re-biasing and filter network which was expected as a 20 MHz signal should be well within the network's passband.

#### 7.2.4.3 Resultant Waveforms

Figure 7.12a shows the 100 mV, 20 MHz, standard-mode input signal used to test the system. The first-stage amplifier was set to a gain of 19 dB (Amp Mode 2) and the second stage was enabled to achieve its fixed 6 dB gain. Figure 7.12 shows the

resultant outputs of the first-stage amplifier (b), the second stage amplifier (c) and the re-biasing network (d). All the outputs were monitored with an AC-coupled TPP1000 passive probe terminated into 1 M $\Omega$ .

#### 7.2.4.4 Thermal Imaging

During testing the PCB ran very hot in certain areas which was cause for concern. To quantify this heat and to determine if it was in fact problematic, thermal images were taken of the circuit board in full-power mode using a Fluke Ti25 Thermal Imager, see Figure 7.13. The maximum temperature recorded was around 75 °C and this was localized around the first-stage amplifiers.

The datasheet specified a maximum junction temperature as 150 °C. With a junction-to-case thermal resistance of 16.9 °C/W, operating at a maximum of 1 W, the junction temperature should have been below 92 °C. This temperature was well below the maximum limit and was therefore deemed acceptable.

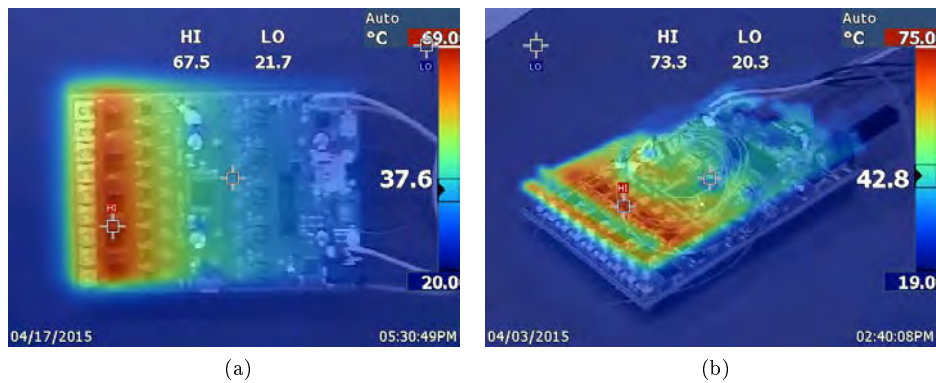
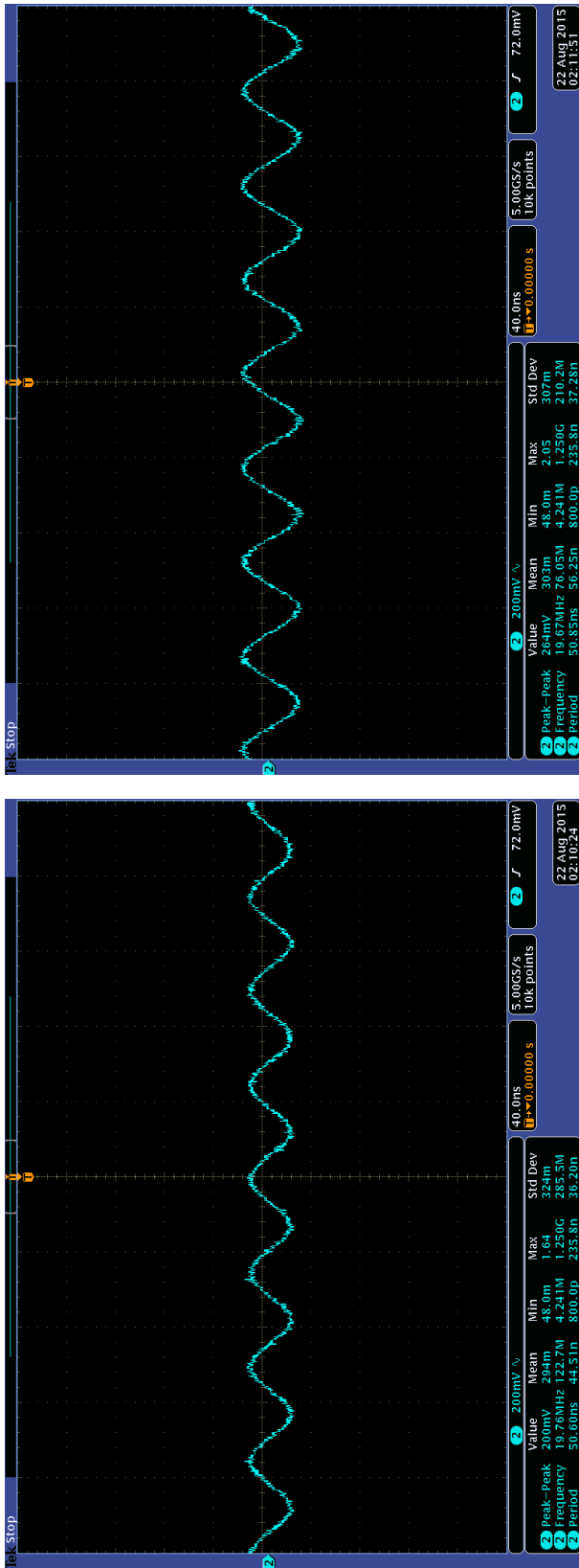


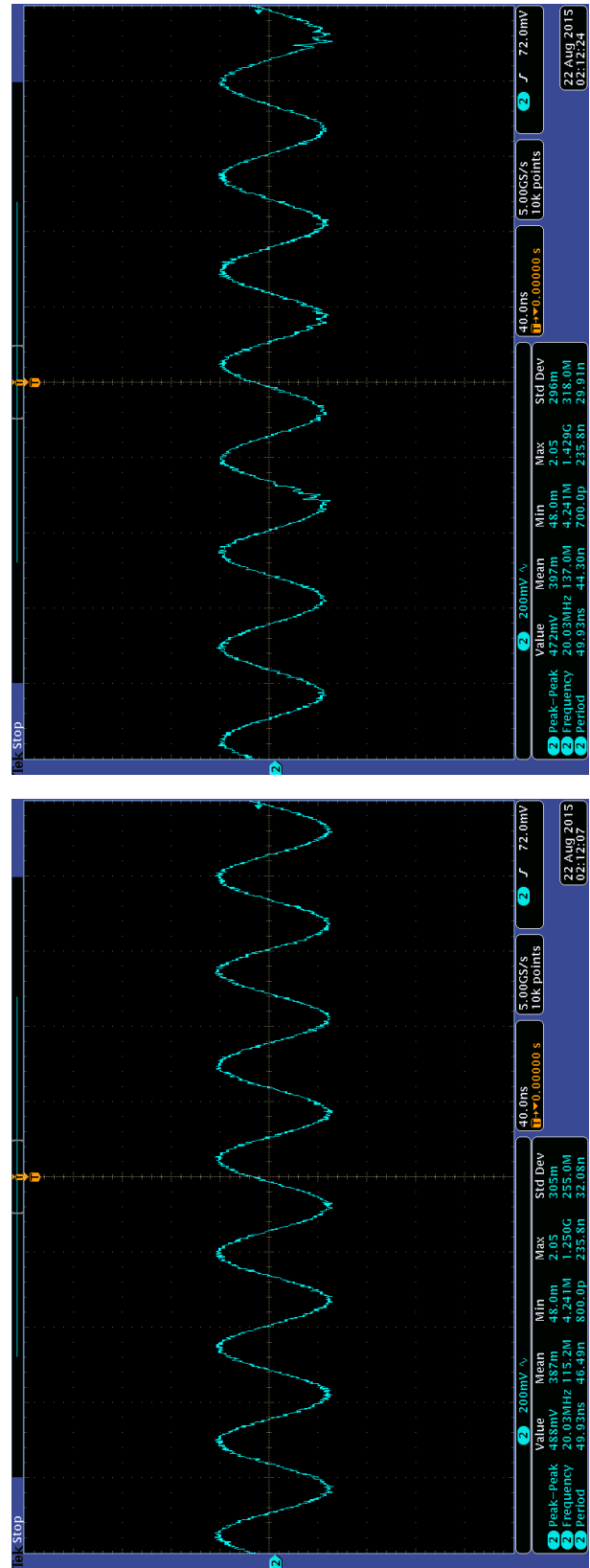
Figure 7.13: Thermal images of the PCB during full-power mode test

#### 7.2.4.5 Analog Memory

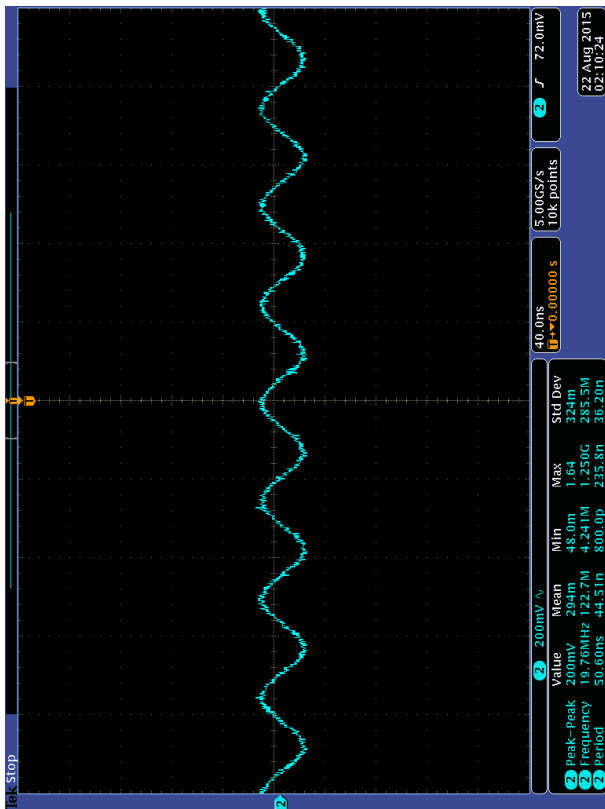
The nine standard mode signal chains were sampled at giga-sample-per-second rates by a single DRS4 SCA and then read out at 33 MSPS for further digitization. Before the SCA could be tested, the preceding amplifiers had to be powered and configured and the digital and analog supplies had to be enabled, if not already, by issuing the “2.5VA Enable” and “2.5VD Enable” commands. The SPI transaction at startup can be seen in Figure 7.14. Each one of the four transactions sends and loads a value to the corresponding DAC output.



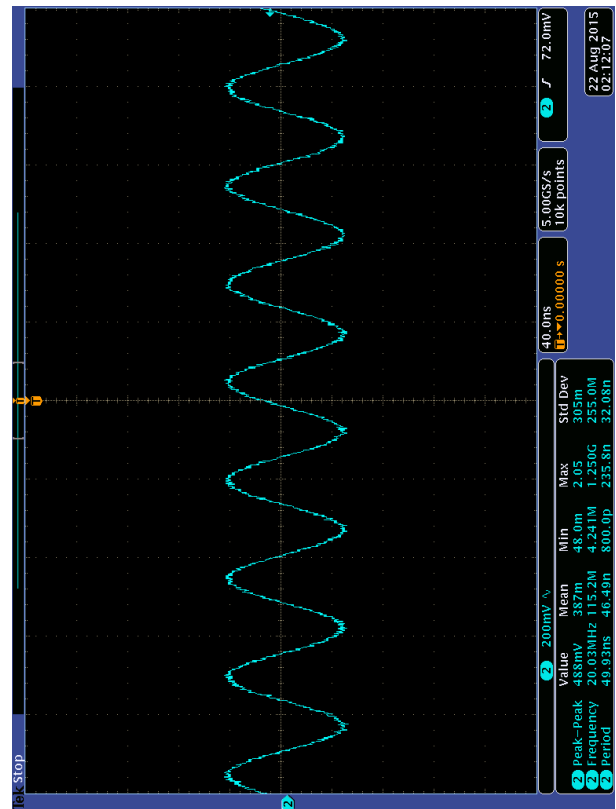
(a)



(b)



(c)



(d)

Figure 7.12: Waveforms measured along the standard-mode signal chain



Figure 7.14: Waveform of the SPI transaction during the DRS4 initialization

The four DAC output voltages were measured to ensure the various inputs were biased correctly. Unfortunately, however, the measurements taken were spurious and inconsistent, and required further investigation. It was found that the DAC’s lower-bound reference voltage pin was left floating rather than being grounded. To fix this problem, the DAC’s Vref(L) pin was bridged with solder to the adjacent ground pin. Once fixed, the following measurements were taken:

Table 7.13: Test procedure for DRS4 DAC

Description	Result	Expected	Min	Max
DRS4_CM	0.998 V	1.00 V	0.995 V	1.005 V
BIAS	0.695 V	0.70 V	0.695 V	0.705 V
O_OFS	1.367 V	1.37 V	1.365 V	1.375 V
ROFS	1.046 V	1.05 V	1.045 V	1.055 V

This time all the results were nominal, with the largest error being only 0.72 %. The final test for the SCA was to check the output of the device. This was achieved by bringing the active-low reset line HIGH and providing a reference clock from the FPGA. In addition, the SCA was set to “transparent mode” and the DWRITE and DENABLE lines were set HIGH. As a result, the PLLCK pin went high (monitored via the AXI GPIO sharing on the SoC) indicating that the internal PLL was working correctly and had locked onto the desired frequency.

Figure 7.15 shows the DRS4 SCA’s output with a 100 mV, 32 kHz test signal applied to the standard-mode input. Furthermore, the first-stage amplifier was set to mode 2 and the second-stage amplifier was enabled. The output signal’s peak-to-peak voltage was around 500 mV, which would occupy 50 % of the ADC’s full-scale range, and showed no sign of distortion.

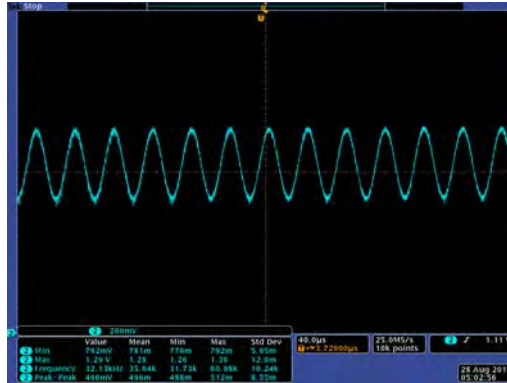


Figure 7.15: Waveform of the DRS4 SCA's output

#### 7.2.4.6 Digitization

The digitization stage took nine streams of data and converted the analog samples to 14-bit digital words at a rate of 33 MSPS, using five dual-channel ADCs. To begin testing, the preceding circuitry had to be enabled and correctly configured and the +1.8 V supply line had to be enabled with the “1.8V Enable” command. The ADC was initialized via the SPI interface with four serial transactions, see Figure 7.16. During initialization, the ADC was configured to operate in 1-lane mode with 14-bit serialization and the output test pattern was enabled.

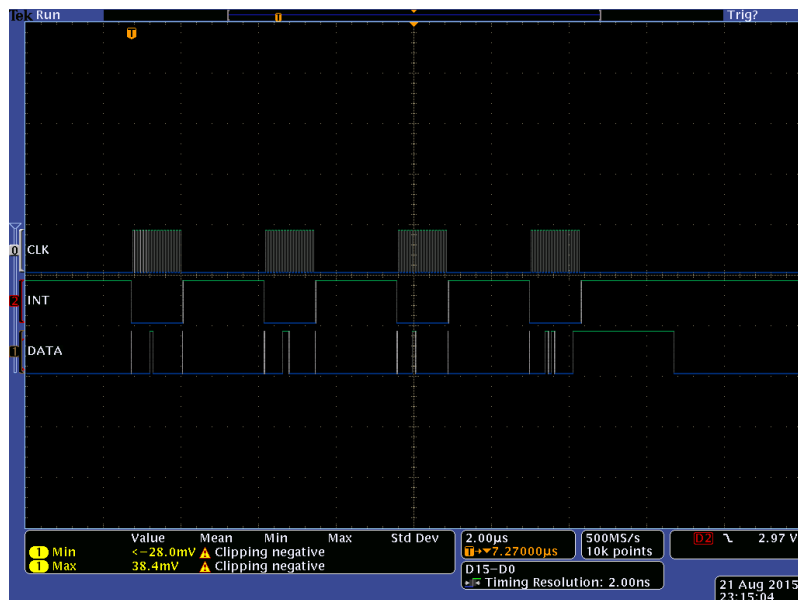


Figure 7.16: Waveform of ADC's SPI initialization

To ensure the ADC was configured correctly, five of the voltage levels at the IC were measured, as tabulated below:

Table 7.14: Test procedure for digitization voltage levels

#	Measurement	Result	Expected	Min	Max
1	1.8 V supply	1.787 V	1.80 V	1.79 V	1.81 V
2	Vcm1 output	0.866 V	0.90 V	0.89 V	0.91 V
3	Vcm2 output	0.866 V	0.90 V	0.89 V	0.91 V
4	REFH output	1.125 V	1.120 V	1.115 V	1.125 V
5	REFL output	0.605 V	0.600 V	0.595 V	0.605 V

The 1.8 V supply and the two common-mode input voltages were below their minimum specification. All three of these measurement failures were due to the 1.8 V regulator providing a slightly lower voltage than anticipated. To fix this issue, the supply voltage could have been corrected by replacing the voltage-setting resistor for a more suitable value. However, because a slight decrease in supply voltage would not significantly affect the ADC’s performance, the voltage was left as is.

In addition to the five static voltages measured, the input encode clock and output data and frame clock was monitored. Figure 7.17a shows the input signal to the ADC, after the anti-aliasing filter and re-biasing network. The common-mode input voltage was as expected and the peak-to-peak voltage was within the ADC’s measurement capabilities. Figure 7.17b shows the ADC’s 33 MHz encode clock input which controlled the sample rate of the ADC. Finally, Figure 7.17c and 7.17d shows the ADC’s output data and frame clock respectively. The frame clock matched the encode clock’s frequency but was aligned with the output data and the data clock was 7 times faster due to the 14-bit DDR digitization.

The final step was to check the interface between the ADC and the FPGA. With 14-bit serialization, at a rate of 33 MSPS and across 9 channels, the total instantaneous data input rate was just over 4 Gb/s. To verify that the interface was, in fact, operating as intended the AXI GPIO sharing was used to send commands and receive status updates. At startup, the SoC passed both the UART and RAM self-test after which the following commands were issued:

Table 7.15: Test procedure for ADC-FPGA interface

#	Procedure	Command	Status	Description
1	Issue “Reset” command	0x080	0x28	All power off, hold in reset.
2	Issue “Power” command	0x0DD	0x28	Enable all power rails.
3	Issue “Unreset” command	0x05D	0x2A	Release from reset. PLL locks successfully.
4	Issue “Amp Enable” command	0x07D	0x2E	Enable second amp. Bitslip locks successfully.
5	Issue “FIFO Enable” command	0x17D	0x2E	Enables RAM storage
6	Issue “FIFO Disable” command	0x07D	0x2E	Stops storage after filling memory
7	Check status again	-	0x2F	FIFO indicates that it is full

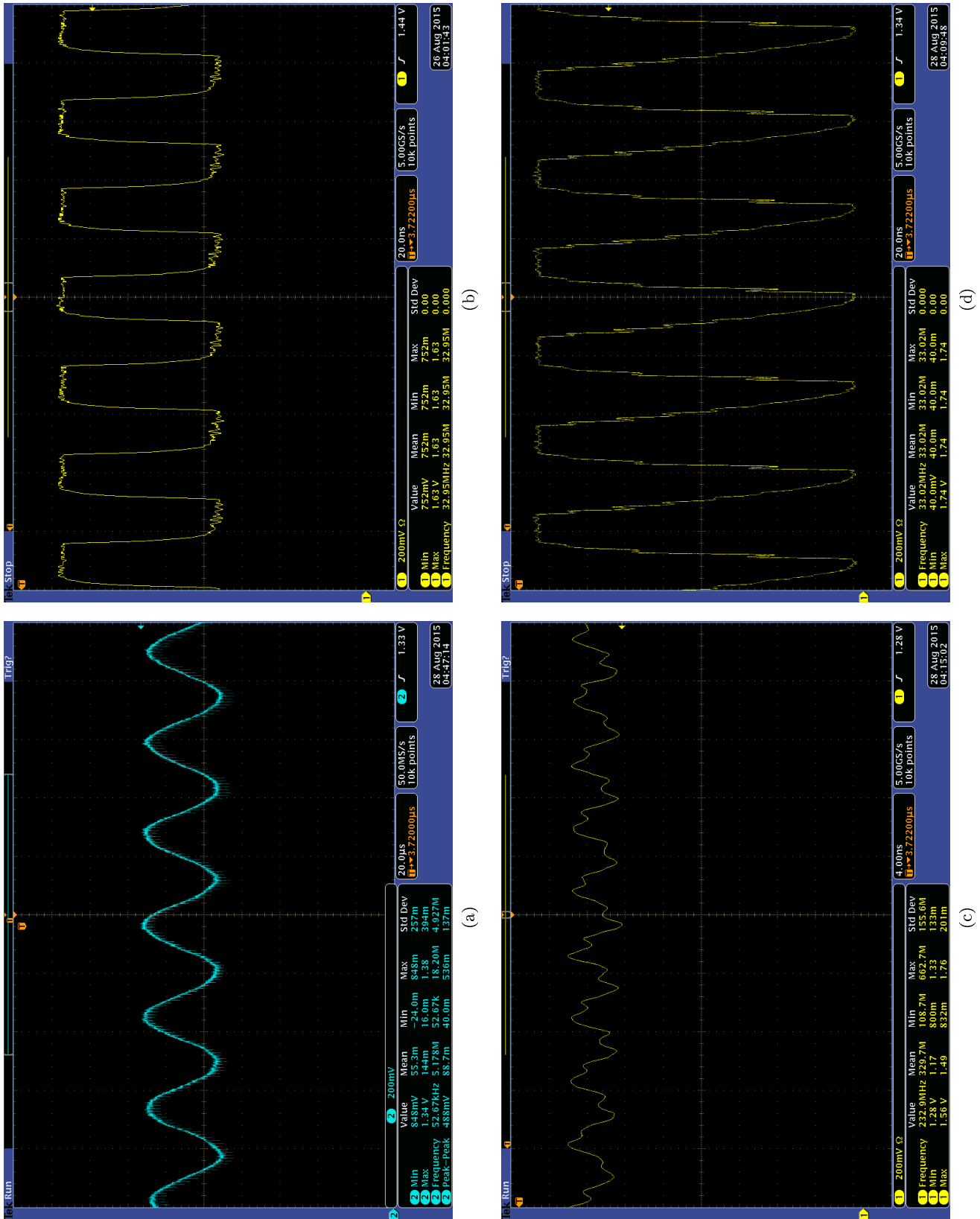


Figure 7.17: Waveforms of the ADCs inputs and outputs

The first three commands simply enabled the power supplies and initialized all the components on the detector. The only useful status message received was that the DRS4's PLL had locked onto the desired frequency and was ready for sampling. The most significant result was at #4 when the status message reported that the bitflip lock was successful. As a reminder, this meant that the high-speed input data pattern was recognized and aligned and the ADC was instructed to disable the test pattern and transmit real data. This data was captured in RAM via a FIFO controller and accessed via the processor, see Figure 7.18.

Address	0 - 3	4 - 7	8 - B	C - F	10 - 13	14 - 17	18 - 1B	1C - 1F	20 - 23	24 - 27	28 - 2B	2C - 2F	30 - 33	34 - 37	38 - 3B	3C - 3F
40000000	CE100000	Bf180000	82180000	A5180000	A0180000	90180000	8D180000	61180000	6E180000	52180000	65180000	51180000	4E180000	26180000	0D180000	13180000
40000040	00180000	Fc170000	D8170000	CD170000	85170000	8C170000	97170000	84170000	81170000	60170000	56170000	45170000	34170000	2E170000	07170000	F5160000
40000080	EE160000	D6160000	87160000	9B160000	84160000	7D160000	62160000	55160000	3B160000	1A160000	13160000	12160000	F9150000	FA150000	C7150000	C0150000
400000C0	A1150000	83150000	79150000	57150000	41150000	25150000	1B150000	F7140000	F3140000	C1140000	8A140000	8E140000	8B140000	72140000	55140000	4C140000
40000100	22140000	12140000	E9130000	C9130000	D1130000	AD130000	87130000	79130000	44130000	2C130000	0A130000	04130000	F4120000	D9120000	C8120000	83120000
40000140	76120000	5A120000	45120000	0B120000	09120000	D8110000	89110000	A8110000	8A110000	72110000	4E110000	33110000	11110000	FD100000	DF100000	AD100000
40000180	93100000	76100000	50100000	2A100000	00100000	DE0F0000	D20F0000	A00F0000	890F0000	820F0000	430F0000	240F0000	010F0000	E40E0000	D00E0000	880E0000
400001C0	930E0000	710E0000	390E0000	230E0000	080E0000	D90D0000	8F0D0000	980D0000	750D0000	550D0000	2F0D0000	1A0D0000	E60D0000	C40C0000	A90C0000	880C0000
40000200	510C0000	400C0000	160C0000	F30C0000	CD0B0000	800B0000	890B0000	630B0000	2E0B0000	1A0B0000	F40A0000	CD0A0000	820A0000	920A0000	5D0A0000	530A0000
40000240	2D0A0000	F8090000	CB090000	9A090000	7A090000	5C090000	33090000	0F090000	D8080000	89080000	98080000	65080000	48080000	28080000	F4070000	07070000
40000280	8A070000	87070000	50070000	3F070000	0F070000	EE060000	BD060000	A6060000	76060000	32060000	25060000	04060000	D9050000	A4050000	8C050000	63050000
400002C0	3E050000	35050000	EF040000	BF040000	A9040000	88040000	53040000	27040000	F4030000	E1030000	8A030000	8E030000	70030000	48030000	D8030000	F9020000
40000300	CE020000	A5020000	7A020000	43020000	1B020000	01020000	CE010000	A4010000	83010000	50010000	35010000	0C010000	DF000000	87000000	8C000000	64000000
40000340	39000000	1F000000	07000000	D43F0000	A53F0000	6C3F0000	483F0000	2C3F0000	013F0000	CF3E0000	A23E0000	903E0000	493E0000	343E0000	FE3D0000	DE3D0000
40000380	AE3D0000	883D0000	693D0000	463D0000	163D0000	EC3C0000	CA3C0000	983C0000	7E3C0000	603C0000	1F3C0000	083C0000	D33B0000	AB3B0000	813B0000	4E3B0000
400003C0	273B0000	133B0000	F23A0000	D53A0000	A33A0000	8E3A0000	543A0000	1F3A0000	023A0000	D8390000	A2390000	8A390000	65390000	25390000	19390000	D7380000
40000400	0C380000	99380000	86380000	60380000	29380000	06380000	D9370000	CB370000	91370000	64370000	4A370000	21370000	FC360000	C4360000	B0360000	89360000
40000440	62360000	3A360000	20360000	F2350000	D1350000	AC350000	78350000	58350000	34350000	1C350000	F8340000	D7340000	AA340000	81340000	52340000	32340000
40000480	07340000	F8330000	C0330000	A2330000	81330000	64330000	29330000	02330000	F3320000	DA320000	AB320000	92320000	66320000	41320000	1F320000	F5310000
400004C0	D8310000	BE310000	81310000	78310000	56310000	40310000	18310000	E4300000	A0300000	89300000	8D300000	7E300000	56300000	2E300000	1B300000	F32F0000
40000500	D82F0000	B32F0000	902F0000	652F0000	4F2F0000	262F0000	052F0000	E72E0000	C52E0000	B02E0000	952E0000	812E0000	682E0000	482E0000	112E0000	802E0000
40000540	E12D0000	C32D0000	9C2D0000	812D0000	602D0000	422D0000	3A2D0000	182D0000	FF2C0000	E52C0000	C52C0000	A72C0000	8C2C0000	792C0000	492C0000	442C0000
40000580	1E2C0000	0A2C0000	C72B0000	AE2B0000	922B0000	7C2B0000	5E2B0000	462B0000	2F2B0000	072B0000	252B0000	072B0000	ED2A0000	D72A0000	8D2A0000	862A0000
400005C0	882A0000	822A0000	652A0000	492A0000	312A0000	152A0000	092A0000	F8290000	E1290000	D0290000	B0290000	A8290000	98290000	77290000	7A290000	58290000
40000600	46290000	48290000	2A290000	16290000	EF280000	DF280000	BD280000	C7280000	F8280000	AE280000	A2280000	88280000	76280000	68280000	65280000	46280000
40000640	29280000	24280000	20280000	03280000	FC270000	E4270000	BC270000	8B270000	A6270000	A7270000	8E270000	76270000	7A270000	6F270000	6A270000	5A270000

Figure 7.18: ADC input data stored in shared RAM

The figure shows the first 416 of the 1024 data points collected. The data points are constantly increasing and decreasing, tracking the input signal, and are presented in 2's complement format. By re-enabling and disabling the FIFO, new data could be collected and the memory cells would be automatically updated. The full scale range of the ADC's inputs were tested manually by varying the input signal's amplitude from 0 V peak-to-peak to the point where the digital output saturated.

### 7.2.5 System-on-Chip

The overall system was controlled primarily by the SoC, either by the FPGA or processor. Figure 7.19 shows the complete SiPM detector, fully assembled and integrated with the SoC daughter-board.

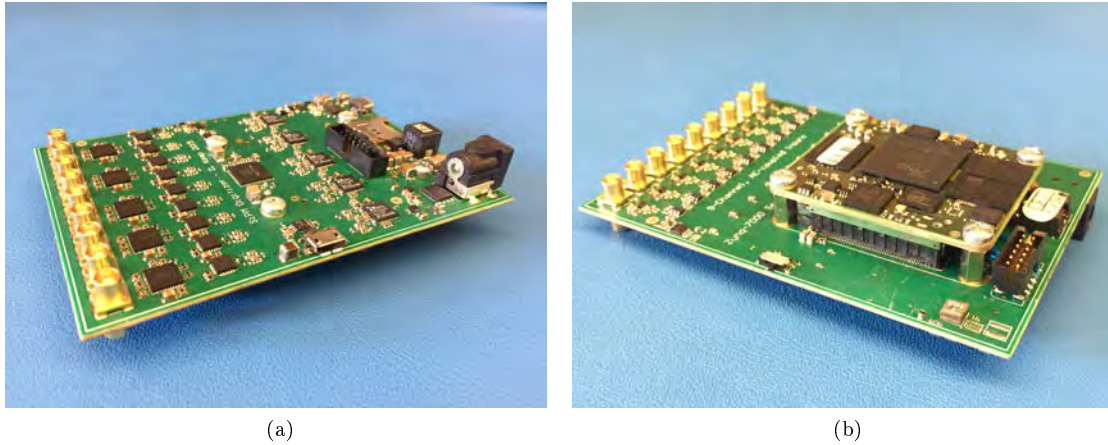


Figure 7.19: Image of the top (a) and bottom (b) of the final SiPM particle detector

### 7.2.5.1 Power Consumption

The SoC daughter-board was powered primarily by a 3.3 V power supply and consumed 70 - 100 mA of current during regular operation. This equates to a peak power consumption of approximately 3.3 W shared between the FPGA, the on-board processor and all the other components and peripherals on the daughter-board (RAM, Ethernet controllers etc). Xilinx's Vivado tool estimated that approximately 1 W of this power was consumed by the SoC and this is itemized in Figure 7.20.

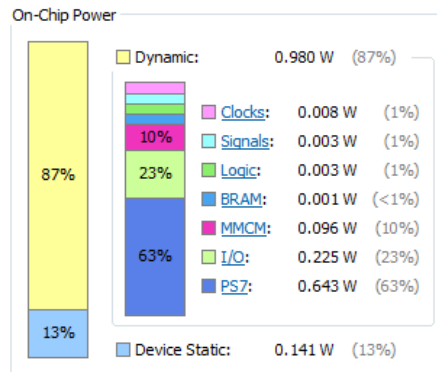


Figure 7.20: Summary of the FPGA's power usage

From the figure it is clear that the majority of the power was consumed by the onboard processor (PS7), accounting for 63 % of the power usage. The closest contender is the FPGA and processor's I/Os that account for an additional 23 % of the overall power. The remaining 14 % is distributed between clocks, internal logic, internal memory etc. Assuming an ambient temperature of 25 °C and reasonable

airflow (no heatsink), the SoC was predicted to dissipate 1.122 W of heat with a junction temperature of 38 °C.

The overall particle detector consumed between 0.3 and 2 A at an input voltage of 8 V. This equates to a total power consumption of 2.4 W during low-power mode and 16 W at maximum performance. Low-power mode would allow for basic “off-line” processing of data, keeping regulators enabled and providing the quiescent current for certain components. Maximum performance refers to when all amplifiers and supporting electronics are running at peak performance which would be required during particle detection.

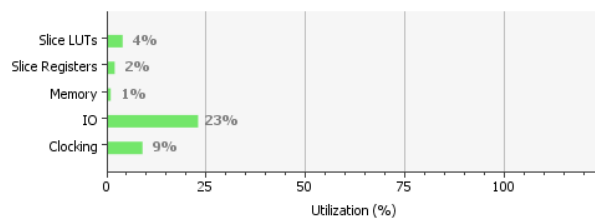
### 7.2.5.2 Resource Utilization

After the VHDL synthesis and optimization, the Vivado toolset was able to provide a resource utilization summary for the FPGA, see Figure 7.21. The three primary “performance” resources for the FPGA (LUTs, registers and memory) did not exceed more than 4 % per category, suggesting that the FPGA’s performance was heavily underutilized. These three resources are referred to as “performance parameters” as they are directly involved in the parallel processing of data.

Clock and I/O utilization were not of any concern for the design for the following reasons. Firstly, once all the clocks had been generated for a particular design, the device could be scaled up to support additional channels without the need for generating additional clocks. Secondly, the number of I/Os can be increased by simply choosing a physically larger FPGA, of which there were many to choose from within the same family.

Resource	Utilization	Available	Utilization %
Slice LUTs	1875	53200	3.52
Slice Registers	2406	106400	2.26
Memory	2	140	1.43
IO	45	200	22.50
Clocking	3	32	9.38

(a)



(b)

Figure 7.21: Summary of the FPGA’s resource utilization

### 7.2.5.3 GPIO Expansion

The GPIO expansion header was initially intended for future developments and project expansion. However, there were 7 nets routed to the SoC daughter-board that turned out to be unsuitable for the intended purpose. Six of these were routed to the pins that were reserved for use with the TE0720’s onboard Ethernet controller

and could not be easily re-purposed, contrary to the documentation. The remaining net, WB\_SS, was routed to an output-only pin which could not be placed in a high-impedance state.

Therefore, to retain the original functionality, these nets were rerouted to the expansion header pins with thin jumper wire. The pinout for the expansion header with the original name and new functionality is shown below:

Table 7.16: GPIO expansion header function list

Pin #	Original Name	New Function
1	MIO15_Tx	MIO15_Tx
2	V_Bat	V_Bat
3	GND	GND
4	GND	GND
5	Pin 5	+5V_Enable
6	Pin 6	Level Shift Enable
7	Pin 7	+2.5VA Enable
8	Pin 8	Amplifier Enable
9	Pin 9	Trig_SCLK
10	MIO14_Rx	MIO14_Rx
11	Pin 11	Trig_SDI
12	Pin 12	Trig_SS

## Chapter 8

# Conclusion

This study sought to determine the feasibility and suitability of a silicon photomultiplier-based particle detector for use in a space environment, within our solar system and beyond. More specifically, the study was concerned with the development and testing of three primary sub-systems, namely a SiPM breakout board, SiPM power supply and the digitizing particle detector. All the sub-systems were developed successfully and, when integrated, performed well together as a potential space-based particle detector.

The SiPM power supplies worked as expected, providing a negative bias voltage ranging from 22.5 V to 31 V. Using the current output DAC, the power supplies were adjustable in sub-9 mV increments. During testing, the full output range was successfully tested and the supply could be enabled and disabled at will.

The SiPM breakout board was hand-assembled to ensure that the fragile SiPM detector was not damaged. The board was tested with a negative bias of 27.5 V with a plastic scintillator and 3D printed enclosure. Both the fast and standard mode outputs produced the expected high-speed signals with good signal integrity. This setup allows for characterization of various plastic scintillators for different particle events which is a key aspect in developing particle identification and discrimination algorithms.

The main circuit board, whose primary function was high-speed digitization, performed adequately as an overall platform to support particle detection. The fast-mode signal chain worked well both in terms of amplification and triggering as well as power consumption. The amplification stage provided sufficient gain for a trigger decision and did not require significant electrical power. Despite one of the comparators failing during testing, possibly due to ESD or unintentional negative biasing, the remaining comparator stages operated as expected with minimal propagation delay and high switching speeds.

The standard-mode signal chain performed well in terms of signal amplification and conditioning but the first- and second-stage amplification stages dissipated a considerable amount of heat. The passive thermal heatsinking techniques used on the circuit board were insufficient to eliminate thermal concerns. Despite these concerns, however, the amplifiers performed as expected across the full gain range and could be enabled and disabled, at will, via the FPGA.

The DRS4 SCA is critical to the overall particle detector design and allows an effective input data rate of 756 Gb/s (6 GSPS at 14 bits across 9 channels).

The DRS4 SCA is also inherently radiation tolerant, making it an ideal candidate for space applications. The high-speed ADC and its interface to the Zynq SoC work very well, allowing the stored analog samples to be digitized at a maximum rate of approximately 8 GSPS (65 MSPS at 14 bits across 9 channels). The final implementation tested operated at half this speed (33 MSPS) to ensure optimal performance from the DRS4 SCA.

In addition to the components and peripherals mentioned, the JTAG programmer, power supplies, UART-to-USB converter, GPIO expansion headers and other supporting electronics all worked well. As mention in Chapter 7.2, minor modifications were made to correct for PCB routing errors, thereby still providing all the features initially desired. The SD card and USB 2.0 interface were not tested during the study as these features were added for future developments only and did not impact the primary functionality of the SiPM particle detector.

In conclusion, the study successfully demonstrated a working platform that could support particle detection, identification and discrimination. However, more work is required to increase the technical readiness level (TRL) of the device, thereby ensuring that the device is capable of space-flight. Furthermore, NASA Ames Research Center has been very impressed by the prospect of a silicon photomultiplier-based particle detector and the results of this study. Consequently, a collaboration with the University of Cape Town is being pursued to continue with this project in the form of a PhD research project, hosted at and funded by NASA Ames Research Center.

## Chapter 9

# Recommendations

Although the overall particle detector demonstrated its ability to perform particle detection, identification and discrimination, the device can only be classified as TRL 5 or 6. This means that the underlying technology has been developed and demonstrated but still needs further development and must undergo environmental testing before it can be integrated into a spacecraft.

The SiPM breakout board worked flawlessly but was designed for testing and evaluation purposes only. Therefore, it is recommended that a mission-specific array of silicon photomultipliers be designed and tested. Furthermore, once placed in an array, the silicon photomultipliers performance should be evaluated in terms of cross-talk, bias mismatches and output summing. This research would be critical for a final implementation in a spacecraft.

The SiPM power supplies were also purposed for lab testing and therefore require a simple redesign. It is recommended that the power supply is integrated into one of the other circuit boards, either the SiPM array or digitizer, to reduce the detector's overall footprint and unwanted noise coupling. Finally, the output voltage range should be optimized for the SiPM array chosen as well as the particular application, thereby allowing higher accuracy and incremental resolution.

Although the main particle detector circuit board provided the intended functionality and desired signal integrity, a fundamental amplifier-stage architectural change is recommended. This could involve one of two options, or a combination of the two:

1. Reduce the detector's channel count
2. Use an alternative amplifier architecture

The total power consumption of the particle detector is directly proportional to the detector's channel count. Therefore, by reducing the number of channels, the power consumption, and thermal dissipation, would go down considerably. However, to maintain the same functionality, a new method to non-ambiguously determining which SiPM was responsible for a particle event would need to be developed. The outputs of the different SiPMs would also need to be summed in some way.

Using an alternative amplifier architecture could reduce the total power consumption of the device considerably. The flexibility offered by programmable gain

amplifiers is very convenient but unfortunately leads to a high-power system. Therefore, it may be worth considering alternative architectures such as multistage amplification with switchable amplifiers, specifically optimized for a particular gain.

In addition to the architectural change, the physical location of the amplifier stages should change too. Due to the small, sensitive signals output by the SiPMs, it is recommended that pre-amplifiers are placed as close to the SiPMs as possible. This location change will begin to alleviate the thermal issues generated by multiple high-power devices placed within close proximity to one another.

Another recommended architectural change is moving away from the SoC approach which incorporates both an FPGA and processor to a design which utilizes only an FPGA. This recommendation is driven by the large power requirement imposed by the processing system, as discovered in Chapter 7.2. Moreover, the FPGA is more than capable of supporting the particle identification and discrimination algorithms, making the processor redundant. Using a basic radiation-hardened FPGA will also lead to a more robust, space-ready system.

During the course of the study, three other issues were encountered, listed below:

1. Failure of the 3.3 V regulator
2. Routing of nets to reserved pins
3. Amplifiers that were automatically enabled at startup

Although failures and errors are not uncommon during a research project, all of these issues could have been mitigated with the correct procedures in place. For example, the failure of the 3.3 V regulator which was most likely due to an input capacitor with an insufficient voltage rating. This risk could have been mitigated by not having capacitors of the same value with multiple voltage ratings. Although this could increase the cost of the overall project, the additional cost is worthwhile if it insures that the final board operates correctly and without failure. Furthermore, it is not recommended to use components with a BGA footprint in the prototyping phase of a project due to the complexity in replacing the components on a fully-assembled circuit board.

For a final spacecraft implementation of the circuit board, the large, barrel-type power connector should be removed and replaced with a more appropriate connector that can provide connectivity to the relevant spacecraft bus, capable of providing power and full-duplex communication. Similarly, the USB 2.0 interface, the MicroSD card and the UART-to-USB interface would not be necessary in space and could be removed completely.

A particularly important aspect that needs to be addressed in future developments is FPGA firmware development, especially if the processor aspect is removed from the detector. Although firmware and software has been written to support the hardware, the particle detection algorithms need to be converted from C, Python or MATLAB code to VHDL. This includes, but is definitely not limited to, automatic bias removal, short and long integration, dynamic trigger and amplifier gain adjustment, constant fraction discrimination and more.

Finally, environmental tests should be conducted on the final particle detector to ensure that the device can operate in the space environment. This should include

vibration, thermal and vacuum chamber testing to simulate all the aspects of a space mission.

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# Appendix A

## Additional Theory

The following sections supplement the relevant sections from the Literature Review.

### A.1 Particles in Space

#### A.1.1 Gamma-Ray Astronomy

Gamma-ray bursts, although first detected in 1967, are still under investigation today. These flashes of photons, ranging from a few milliseconds to hundreds of seconds in duration, are thought to originate from distant collapsing stars. The Gamma-Ray burst Investigation via Polarimetry and Spectroscopy (GRIPS) mission is in progress at the Max Planck Institute and has a primary mission objective to investigate and understand the early Universe using gamma-ray bursts. The project envisions a hybrid telescope capable of imaging gamma-rays from 200 keV to 50 MeV via Compton scattering and pair production at unprecedented sensitivity[59].

A particular area of interest for the high-energy astronomy community is the poorly explored hard X-ray and medium energy gamma-ray bands[60]. The main scientific driver behind exploring these bands is to identify and generate a complete census of accreting black holes in the Universe. Additionally, medium-energy gamma-ray astronomy detectors can monitor extreme physical conditions in the Universe and improve our understanding of nucleosynthesis and the origin of radiation.

A previous NASA mission, the Compton Gamma-Ray Observatory (CGRO), was launched in 1991 and provided answers to some of the galaxy's mysteries[61]. It was, however, limited by its insensitivity and coarse measurements (by today's standards) which could be substantially improved upon with modern technologies. Consequently, the Fast Compton Telescope (FACTEL) mission, lead by the University of New Hampshire, aims to further and improve on the research CGRO began by replacing the detectors with fast scintillators. The upgrade will improve the experiments' performance by orders of magnitude, thereby producing much sharper images.

Silicon photomultipliers were used as a focal plane detector for the Imaging Atmospheric Cherenkov Telescopes (IACTs), a terrestrially-based gamma-ray observatory[62].

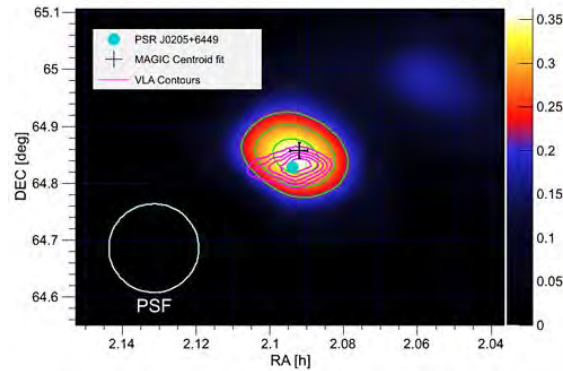


Figure A.1: A skymap obtained from MAGIC showing a gamma-ray emission[63]

The research group at the observatory successfully developed a 256-channel prototype camera consisting of a 4x4 array of 16-channel MPPC<sup>1</sup> modules. Similarly, the Major Atmospheric Gamma Imaging Cherenkov (MAGIC) telescopes, located on the Canary island of La Palma, are IACTs and succeeded in discovering VHE gamma-rays emitted by the 3C58 pulsar wind nebula, see Figure A.1.

### A.1.2 Space Weather and Radiation

A constellation of satellites that could monitor the dynamic interactions between the solar wind plasma and the Earth and Sun's magnetic fields could provide early warnings to both terrestrial stations and space-borne craft to prevent potential radiation damage. This particular application of particle detection could be of interest to the South African National Space Agency (SANSA) given their expertise in the field[64].

Physical Sciences Inc., in cooperation with the Boston University Center for Space Physics, developed and tested a lightweight scintillator-based sensor, called LEPIS, for satellites that is able to monitor the space weather environment[65]. Although LEPIS only made it to a breadboard model, it demonstrated a novel imaging spectrometer for space.

A recent NASA “Tech Briefs” article discusses a neutron spectrometer for inner radiation belt studies aimed at nanosatellites. The spectrometer's primary mission is to detect the main source of high-energy proton albedo neutron decay. With this information, the potential radiation hazards to spacecraft can be better assessed and the local space weather better understood[66].

Similarly, ALTCRISS<sup>2</sup> is a physics experiment, located onboard the International Space Station (ISS), whose mission is to monitor cosmic rays and the radiation environment in low earth orbit. Various effects on the particle flux will be monitored such as coronal mass ejections, orbital dependence, solar modulation etc. and the data collected will be compared to similar experiments already onboard the ISS[67]. Figure A.2 shows the ALTCRISS experiment installed on the ISS.

<sup>1</sup>Multi-Pixel Photon Counter (MPPC) is Hamamatsu's name for their range of silicon photomultipliers

<sup>2</sup>ALTCRISS - Alteino Long Term Cosmic Ray Measurements on board the International Space Station



Figure A.2: Image of the ALTCRISS experiment in the service module of the ISS[68]

### A.1.3 Cosmic Ray Astrophysics

The study of cosmic ray astrophysics led to the discovery of new fundamental particles (muons, positrons etc.) and broadened our understanding of matter. Continuing the study of cosmic radiation could assist in solving the current mysteries surrounding supernova remnants, black holes and the nature of dark matter[69]. The HIREs (High Resolutions Echelle Spectrometer) is an example of a terrestrial high energy cosmic-ray detector that makes use of large area photodetectors and high-frequency, high-speed digital signal processors (DSPs) for processing[70].

Similarly, a research group from Ewha Womans University's Department of Physics conducted a study which discusses the design and simulation of silicon photomultiplier arrays for space experiments[71]. One of the space experiments mentioned was a space telescope that is being developed to measure weak fluorescence signals generated from high-energy cosmic rays and silicon photomultipliers were determined to be highly suitable for this application.

A nanosatellite called Cosmic X-ray Background Nanosatellite (CXBN) was launched on September 13, 2012 with the aim to increase the precision of measurements of the cosmic X-ray background in the 30-50 keV range and produce data that may shed light on the underlying physics of the diffuse X-ray background[72]. The project team tracked the satellite until January 2013 and collected some telemetry data but due to an anomalous low power mode, could not collect sufficient data to complete the mission.

A less formal, but highly interesting, project emerged from a Hackathon held at CERN in 2014 called "Cosmic Pi". The Cosmic Pi is a small, low-cost cosmic ray (muon) detector and the project's goal was to collect, store, share and analyze cosmic data. The project is not likely to produce novel scientific discoveries but the educational value of having a small, low-cost particle detector for experimenting at home or in a classroom is significant.

### A.1.4 Neutrinos

Neutrinos are particularly important elementary particles due to their tiny mass and their ability to travel through the interstellar medium almost completely unhindered. These properties suggest that a high-energy neutrino detector would



Figure A.3: Image of the CXBN spacecraft launched from Vandenberg Air Force Base[72]

allow much deeper exploration of our Universe, more so than any other detector has previously allowed, and this could lead to new discoveries.

A silicon photomultiplier-based detector for ultra high energy neutrinos was designed and tested at Sphinx Observatory Center in Switzerland. The aim of the experiment was to measure particle showers produced by high energy neutrino interactions in the Earth’s crust. The detector performed well, despite the harsh environmental conditions, and was able to discriminate between both up- and down-going particles[73].

The ANTARES<sup>3</sup> experiment is a similar neutrino detector located 2.5 km under the Mediterranean Sea. It consists of 12 vertical strings of detectors spaced 60-70 m apart and covers a surface area of  $0.03 \text{ km}^2$ . Each string contains 75 vacuum photomultiplier tubes that are able to detect Cherenkov light caused by a high-energy neutrino undergoing a charged current interaction. A method for determining whether or not the neutrino was produced by a gamma-ray burst is described in [74] and relies on the ANTARES detector as well as real-time data sharing from gamma-ray burst detecting satellites.

### A.1.5 Dark Matter

The CALorimetric Electron Telescope (CALET) is a Japanese led, international, high-energy particle physics mission that will be installed on the International Space Station. One of CALET’s main objectives is to search for signatures of dark matter by surveying the sky for electrons and gamma-rays in energy ranges up to 10 TeV. The primary charge measuring device on CALET consists of scintillator strips and photomultiplier tubes[75].

A smaller mission called “Antiproton Flux in Space (AFIS)” plans on measuring the flux of antiprotons trapped in the Earth’s magnetic field, particularly in the South Atlantic Anomaly, at very low frequencies. The detector makes use of scintillating plastic fibers and is able to measure particle energies in the range of 25-100 MeV per nucleon, a previously poorly explored energy range. The first test of the

<sup>3</sup>ANTARES - Astronomy with a Neutrino Telescope and Abyss environmental RESearch project

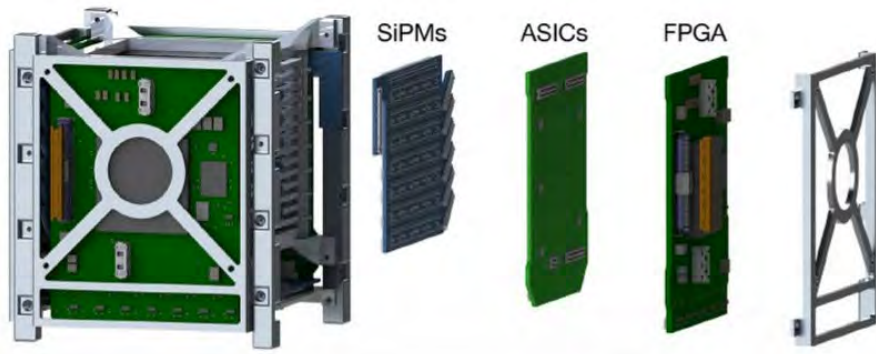


Figure A.4: Exploded view of the AFIS detector in the nanosatellite[76]

device is planned onboard a BEXUS 18 stratospheric research balloon after which it will be inserted into LEO.

### A.1.6 Matter Composition

All matter is composed of protons, neutrons and electrons. The number of protons within an atom's nucleus defines the atomic number ( $Z$ ) which also designates a specific elemental identity ( $Z=1$ =Hydrogen,  $Z=2$ =Helium etc.). A nucleus with a specific atomic and mass number is called a nuclide and is represented by its chemical symbol and mass number as follows:  ${}^3\text{H}$  or H-3. An isotope of an element is a nuclide that has the same number of protons ( $Z$ ) but a different number of neutrons ( $A$ ), see Figure A.5.

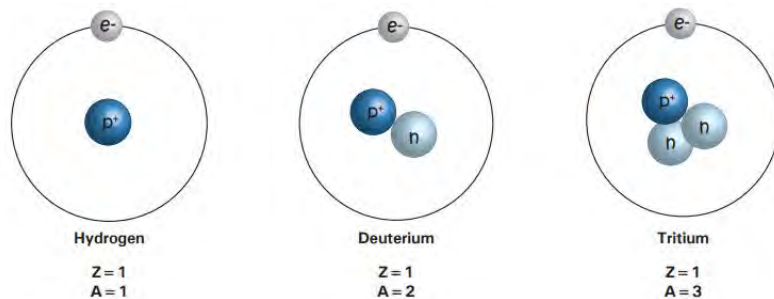


Figure A.5: Three naturally occurring isotopes of hydrogen[77]

If an isotope of a particular element is unstable (dependent on the ratio of neutrons to protons) the nuclei will disintegrate, also known as radioactive decay. During this process of decay, an atom can emit *ionizing radiation* that can be harnessed for testing purposes. Nuclides which undergo radioactive decay are called radionuclides[77].

## A.2 SiPM Biasing Alternatives

Figure A.6 shows four alternative biasing methods for silicon photomultipliers. These methods do not all provide optimal performance and are shown for compar-

ative purposes only. The figures show the biasing topology as well as the resultant signal polarity for the fast and standard mode outputs.

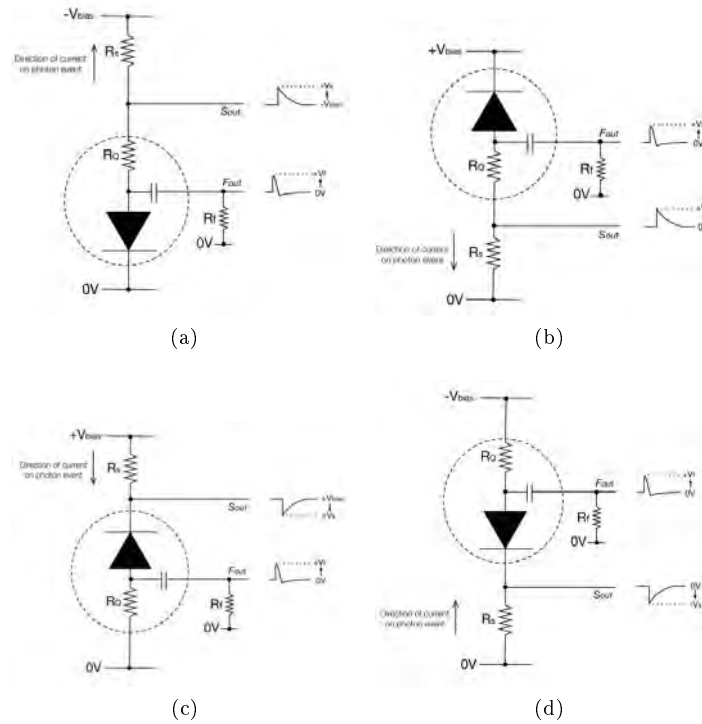


Figure A.6: Four biasing alternatives for SiPMs[52]

Figure A.6a shows the recommended biasing scheme, particularly if the fast-mode is of interest. The resultant fast mode output swings positive with respect to ground but the standard mode output swings positive with respect to  $-V_{bias}$ .

Figure A.6b shows an example of a positive biasing scheme, where the cathode is connected to  $+V_{bias}$ . If the bias voltage is sufficiently decoupled, there should be very little, if any, degradation in performance. Both the standard and fast mode output signals swing positive with respect to ground, making interface electronics relatively simple.

Figure A.6c and A.6d are not recommended for use with applications requiring precise timing or the fast-output. However, the relative output swing of the standard-mode output may be of interest for applications where pulse timing is not critical. For the purposes of this study, the last two bias configurations were not considered.

## Appendix B

# Particles and Photomultipliers

The raw data collected from a silicon photomultiplier has to be processed, analyzed and presented as information to an end user. In order to generate this information, the particle interactions with the scintillator and the resultant silicon photomultiplier output has to be sufficiently understood. This chapter explores the silicon photomultiplier as a detector in more detail, as well as the underlying particle detection theory.

*Note that the particle detection theory is based primarily on the work and publications from UCT's physics department[78, 79, 80, 81].*

### B.1 SiPM Output

Sensl's 60035 B-Series SiPMs are unique in that they have a high Photon Detection Efficiency (PDE), sensitivity up into the UV portion of the spectrum and two outputs; a standard and fast output. Figure B.1 shows the symbol used to depict a SiPM, the recommended biasing topology and the SiPM's outputs. Each of these SiPMs contain 18,980 microcells that cover a  $6 \times 6 \text{ mm}^2$  area with a 64 % fill factor. To create a larger area detector these SiPMs can be "tiled" together to form an array.

#### B.1.1 Biasing

In general, the exact bias voltage required for SiPMs is highly dependent on the photomultiplier itself and can range from 20 - 100 V. Although these voltages may

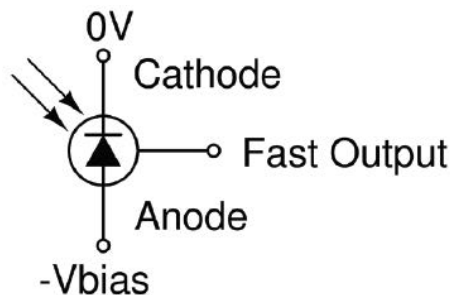


Figure B.1: SiPM model and recommended biasing[21]

seem high, they are actually very low in comparison to any other photodetector with an equivalent gain.

The recommended bias configuration for the Sensl SiPM is grounding the cathode and applying a negative voltage, with respect to ground, to the anode. This is a typical reverse-bias configuration, as shown in Figure B.1. There are, however, other biasing topologies available if negative voltages are unattainable but these have the potential to adversely affect the SiPM’s performance. For more information, please refer to Appendix A.2.

The Sensl 60035 has a breakdown voltage of 24.5 V and an over-voltage rating of 1 - 5 V. This means that in regular operation the SiPM should be biased with a voltage in the range of -25.5 V to -29.5 V. Fortunately, the current requirements for these photomultipliers are very low with a maximum current of 20 mA when using the “SMT” package. Similar SiPMs from Sensl, with a smaller active area, will consume a maximum of 1.5 mA.

### B.1.2 Fast Output

The fast output of Sensl’s B-series has very fast rise and fall times (100-600 ps) and very short pulse widths (1-2 ns). The signal itself is AC-coupled and represents the derivative of the slow output. When correctly biased the signal rises positive with respect to ground. An example of a fast-mode signal can be seen in Figure B.2.

It is imperative that the fast-mode signals are correctly routed to readout or trigger electronics due to their high bandwidth. Sensl recommends applying common microwave/RF design rules and the use of RF transformers for better impedance matching. Amplification of these high bandwidth signals can be achieved using 50  $\Omega$  low-noise RF amplifiers.

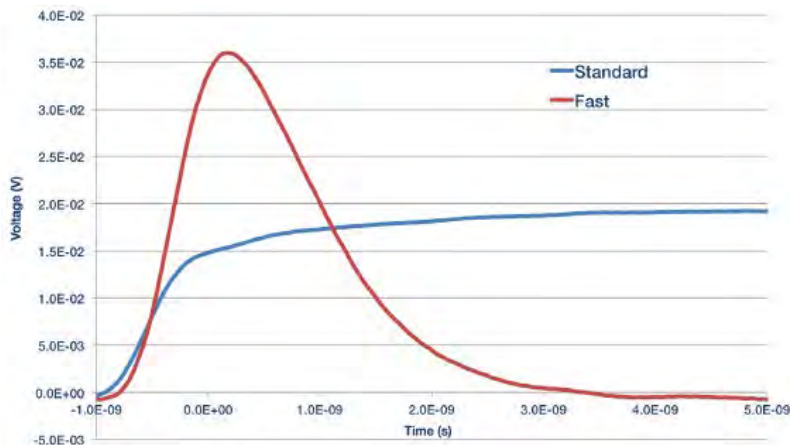


Figure B.2: Sensl SiPM example output signals[21]

### B.1.3 Slow Output

The slow (or standard) output has a rise time of 1-10 ns and a decay time in the hundreds of nanoseconds. This output can be used where the application involves slow-varying, continuous light levels or applications where pulse shape is critical. An example of the standard output can be seen in Figure B.2.

The standard output can be used in AC- or DC-coupled configurations. In DC-coupled configurations the output is a small current that can be amplified through the use of a transimpedance amplifier (TIA). In this configuration the SiPM can detect steady unchanging signals as well as the higher-speed signals.

When using AC-coupling the DC bias is removed but the pulse shape and amplitude is retained. This is particularly useful if the application only requires the detection of changes or high-speed signals. With the AC-coupled configuration the readout electronics are also less likely to saturate when compared to their DC-coupled alternatives as the signal of interest is not added to the DC bias.

## B.2 Particle Energy

When a particle strikes a scintillator it deposits a portion of its energy into the material through elastic and/or inelastic scattering, thereby transferring energy to other charged particles, such as protons or electrons. The amount of energy transferred is dependent on the angle of scattering of the charged particles. The scattered charged particle then leads to scintillation (emission of light), whose intensity is related to the initial deposited energy.

An incident particle's energy can therefore not be measured directly, but the amount of light produced through the scintillation process can be, this is shown in the equation below:

$$E \propto \int_{t_0}^{t_L} V.dt$$

where  $V$  is the pulse generated.  $t_0$  is the start of the pulse and  $t_L$  is the end of the pulse.

The integral of the light produced,  $E$ , must then be scaled to a light output parameter,  $L$ , using a known gamma source. Using the Compton equation, and the measurement of the Compton edge, the energy deposited can be calculated. As the absolute scaling is unknown, the units of  $L$  are "electron equivalence",  $MeV_{ee}$ .

It has been found that the light output for electron scattering is, for practical purposes, linear across the energy range of interest. This is not true for protons, however, whose light output is quadratic as a function of energy and becomes linear at higher energies.

## B.3 Particle Discrimination

It is seldom that only one type of particle is to be detected in the absence of any other particles, resulting in the need for particle discrimination. As an example, it is rare to find neutrons without the presence of gamma-rays. There are many ways to identify and to discriminate between particle types but this study will focus on pulse shape discrimination (PSD). Established in the 1950s, PSD is concerned with identifying particles based on the shape of the pulse they generate in a light detector, due to scintillation.

More specifically, the *charge comparison* method of PSD employs the difference between two integrals of the pulse to discriminate between particle types. The pulse generated by light striking a silicon photomultiplier can be described as having a fast and slow component. The fast component is defined from time  $t_0$  to  $t_s$  and the slow component from time  $t_0$  to  $t_L$ , see Figure B.3.

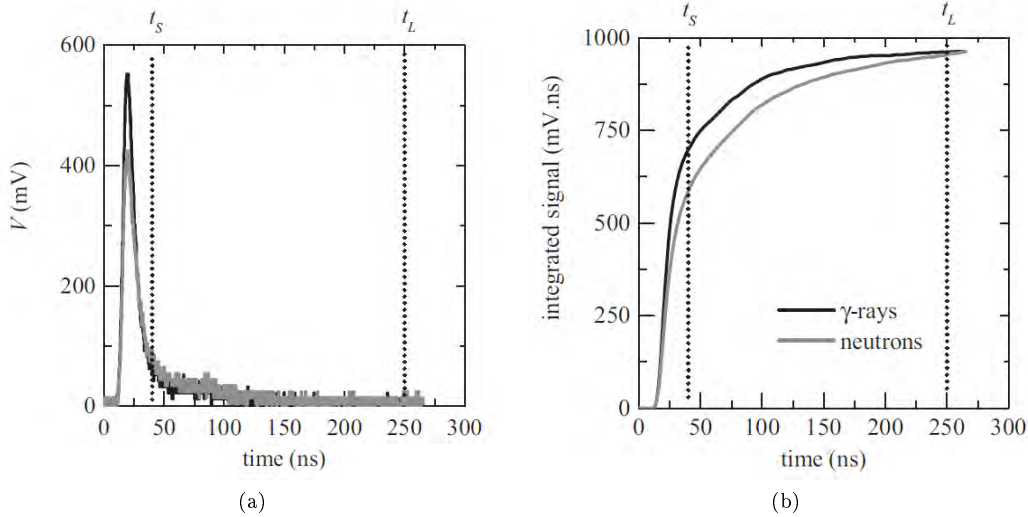


Figure B.3: A pulse (a) and pulse integral (b) of a typical neutron and gamma event chosen to have the same total integral[78]

Before a pulse is analyzed, the baseline is removed to avoid the adverse effects of voltage drift. This is usually achieved by monitoring the DC component of the signal before the pulse is detected and subtracting this component value from each discrete point making up the digitized signal, resulting in a signal starting and ending around 0 V. When using an AC-coupled system, baseline removal is often unnecessary.

### B.3.1 Start Time

The start time of the pulse,  $t_0$ , is non-trivial to define due to the variations caused by noise, amplitude and pulse shape. To minimize the effect of these unknowns, a digital constant fraction discriminator (dCFD) is applied to each signal to determine an optimal start time. A dCFD is simply the difference of two moving average (low-pass) filters where one is scaled and the other offset:

$$v_i = \sum_{j=1}^N fV_{i-j} - V_{i-j-D}$$

where  $V$  is the unfiltered signal,  $N$  is the filter length,  $D$  is the filter offset and  $f$  is the filter fraction. The resultant, filtered signal, is a bipolar pulse, see Figure B.4.

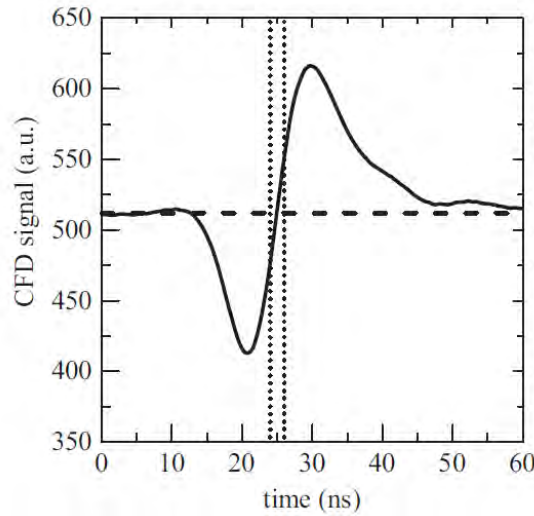


Figure B.4: An example of a typical pulse after application of a dCFD filter[78]

The start time,  $t_0$ , is defined as the time at which the bipolar signal crosses zero, minus a fixed offset. The offset must be included to avoid omitting the very start of the signal. The filter constants  $N$ ,  $D$  and  $f$  are determined empirically by monitoring multiple particle events with two digitizers and comparing the full width at half maximum (FWHM) of the distribution of the difference in signal start times. When sufficiently optimized, a time resolution substantially faster than the sampling interval is achievable.

### B.3.2 Short Integral

The short integral represents the signal's fast component and is defined as the integral of the original pulse from the start time to a pre-defined short time interval:

$$Q_s = \int_{t_0}^{t_s} V.dt$$

where  $V$  is the original pulse,  $t_0$  is the start time and  $t_s$  is the short time interval.

As an example, for a neutron/gamma-ray discriminator the optimal definition for  $t_s$  is the time at which a gamma and neutron signal of the same total integral intersect. Referring to Figure B.3a, this occurs when the signal with the smaller peak becomes the signal with the larger magnitude.

### B.3.3 Long Integral

The long integral represents the slow component and is defined as the integral of the original pulse from the start time to a pre-defined long time interval:

$$Q_L = \int_{t_0}^{t_L} V.dt$$

where  $V$  is the original pulse,  $t_0$  is the start time and  $t_L$  is the long time interval.

The value of  $t_L$  is chosen to be long enough to ensure that the entire significant decaying tail of the signal is captured while short enough to ensure that subsequent particle events are not recorded. Additionally, the maximum value of  $t_L$  may be limited by the digitizer used.

### B.3.4 Pulse Shape

The basis of the charge comparison method is the ratio of the fast component to the slow component, or pulse shape parameter, and is defined by:

$$Q_R = \frac{Q_S}{Q_L}$$

Different particles have different rates of decay, leading to uniquely different values for  $Q_R$ . Figure B.5 shows the different decay rates for alpha particles, fast neutrons and gamma-rays. This example illustrates that gamma-rays exhibit a faster rate of decay than neutrons and alpha particles. In other words, a large portion of the light emitted from a gamma-ray event occurs in a shorter time interval when compared to other particles, thereby leading to a higher value of  $Q_R$ .

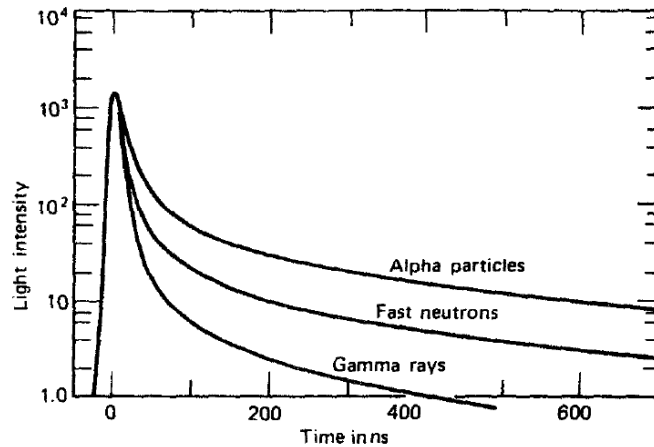


Figure B.5: Comparison of decay rates for three different particle types[82]

When comparing the quality of the PSD for different detectors, the pulse shape parameter is often scaled and offset as follows:

$$S = k \frac{Q_S}{Q_L} + C$$

where  $k$  and  $C$  are constants chosen such that the loci to be compared are adequately aligned. Figure B.6 shows an example of two distributions that have been scaled and shifted for direct comparison.

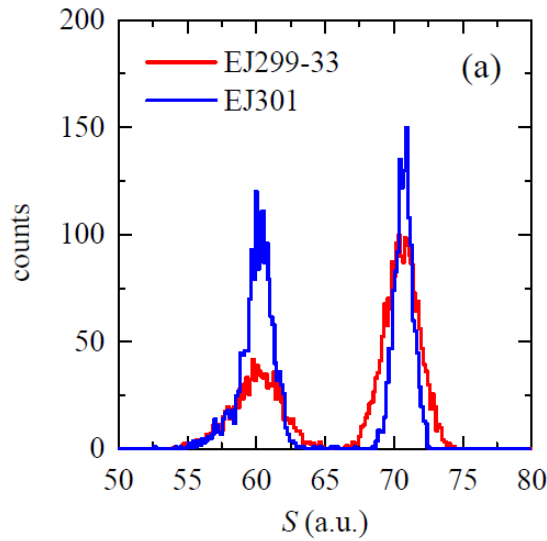


Figure B.6: Graph of counts versus adjusted pulse shape parameter for two plastic scintillators[81]

### B.3.5 Distribution of Events

At relatively low energies, incident neutrons result only in recoiled protons due to elastic scattering off hydrogen and carbon nuclei. Similarly, gamma-rays result in recoiling electrons from Compton scattering. These simple interactions lead to two distinct loci forming when plotting the counts of the pulse shape parameter versus the corresponding light output, see Figure B.7a.

However, above a certain threshold, neutrons have sufficient energy to cause inelastic reactions and, as the energy increases, so does the dominance of this reaction type. A proton beam, capable of producing very high energy neutrons, results in a very different set of loci, see Figure B.7b. At these higher energies ( $\sim 40$  MeV) the combination of elastic and inelastic scattering results in a host of different decay products. In this particular example, the resultant particles released by the two reactions are electrons (e), escaped protons (ep), protons (p), deuterons (d), tritons (t) and alpha particles ( $\alpha$ ). Due to the particles' strong dependence of pulse shape on energy loss the different loci are still discernible.

### B.3.6 Figure of Merit

In order to quantitatively measure the separation between distributions of  $S$ , such as those found in Figure B.8, a figure of merit (FoM) was defined as:

$$FoM = \frac{|\mu_e - \mu_p|}{FWHM_e + FWHM_p}$$

As an example, consider Figure B.8 which shows counts versus the pulse shape parameter for particles detected from a D-T generator. Parameters  $\mu_e$  and  $\mu_p$  refer to the pulse shape value at each of the respective peaks. The full width at half maximum parameters,  $FWHM_e$  and  $FWHM_p$ , refer to the full width of each respective pulse at half of its maximum count. A larger FoM indicates a better discriminator. It is common to adjust the short integral time period,  $t_S$ , to optimize (maximize) the FoM.

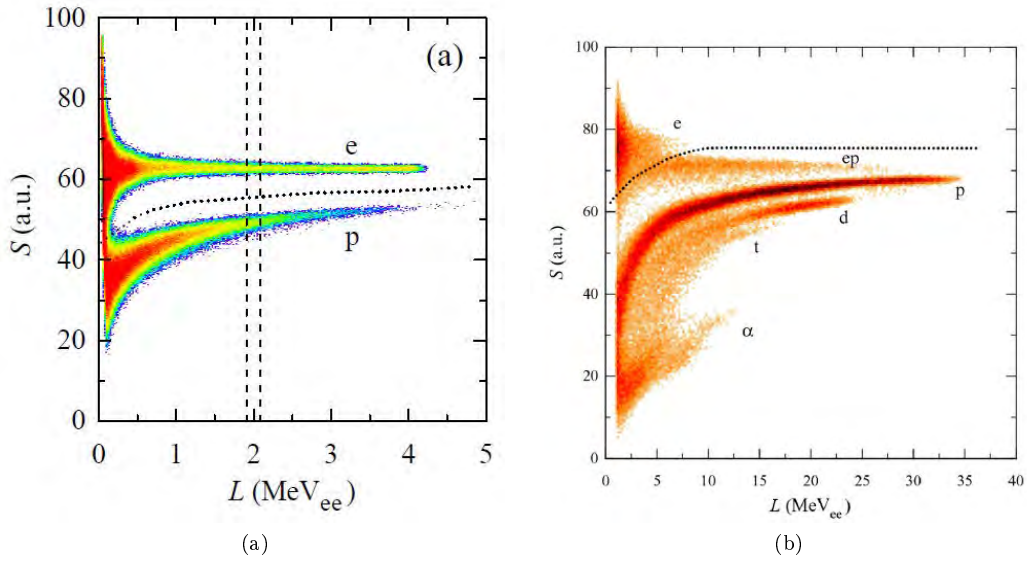


Figure B.7: Graph of pulse shape parameter versus light output when exposed to neutrons and gamma-rays (a) and when exposed to a proton beam (b)[81, 79]

## B.4 Reflow Process

The Sensl MicroFB 60035 silicon photomultiplier has an SMT package option, compatible with standard reflow processes (J-STD-20). Once the SiPMs are removed from their moisture barrier bags, they have to undergo reflow within 72 hours.

The oven available in UCT's Electrical Engineering department was a converted toaster oven. Therefore, to avoid damaging the delicate SiPM detectors, the oven was tested. To support this test, a hole was drilled in a spare SiPM breakout board, into which a thermocouple could be placed. The circuit board and thermocouple were then placed inside the oven, see Figure B.9.

Three tests were run with the same reflow profile to determine the maximum temperatures attained, as well as the maximum rate of change of temperature. The maximum temperature recorded was approximately 232 °C, well below the peak package body temperature of 260 °C. Due to the large thermal inertia of the oven, assisted by the additional insulation added, the temperature rates of change were very low and there was therefore no risk of excessive thermal shock. Additional reflow footprints and information regarding reflow with SiPM arrays can be found in [50].

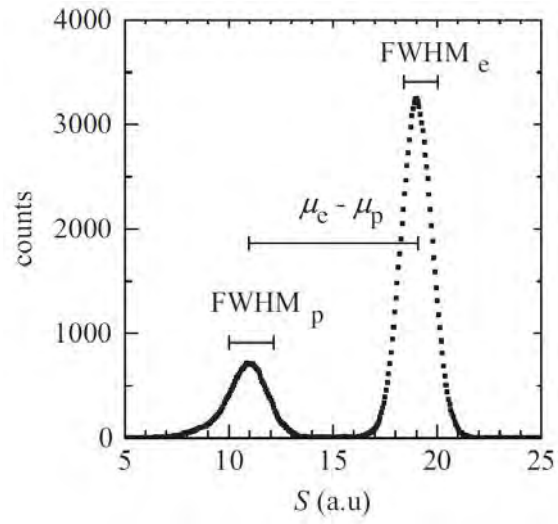


Figure B.8: Graph of counts versus pulse shape parameter for particles generated by a D-T generator[78]

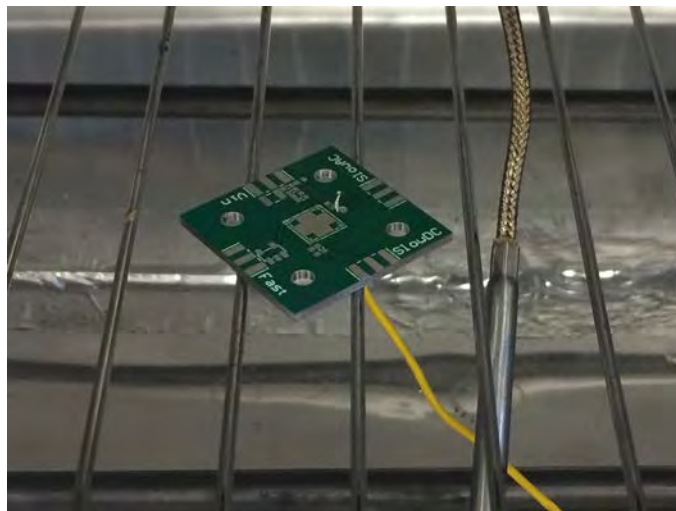


Figure B.9: Thermal test of the reflow oven

## Appendix C

# Circuit Calculations

The following sections supplement the relevant chapters of this dissertation.

### C.1 Microstrip Equations

A regular surface microstrip line consists of a “flat” conductor separated, by a layer of dielectric, from a ground plane, see Figure C.1a. Differential microstrip is similar to surface microstrip but consists of two conductors placed parallel to one another, spaced a specific distance apart, see Figure C.1b.

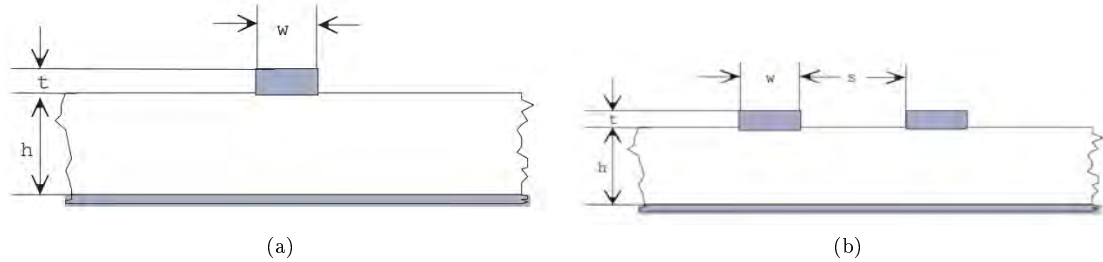


Figure C.1: Microstrip line types for high-speed signaling[83]

The characteristic impedance for regular surface microstrip is calculated as follows[83]:

$$Z_0 = \frac{\eta_0}{2\sqrt{2\pi\sqrt{\epsilon_r + 1}}} \ln \left\{ 1 + \frac{4h}{w'} \left[ \frac{14 + 8/\epsilon_r}{11} \frac{4h}{w'} + \sqrt{\left(\frac{14 + 8/\epsilon_r}{11}\right)^2 \left(\frac{4h}{w'}\right)^2 + \frac{1 + 1/\epsilon_r}{2} \pi^2} \right] \right\} (\Omega) \quad (C.1)$$

where  $\eta_0$  is the wave impedance of free space and:

$$w' = w + \Delta w' \quad (C.2)$$

$$\Delta w' = \Delta w \left( \frac{1 + 1/\epsilon_e}{2} \right) \quad (C.3)$$

$$\Delta w = \frac{t}{\pi} \ln \left( \frac{4e}{\sqrt{(t/h)^2 + \left(\frac{1/\pi}{w/t+1.1}\right)^2}} \right) \quad (\text{C.4})$$

The effective dielectric constant,  $e_{eff}$ , is dependent on the ratio of  $\frac{w}{h}$ . For  $\frac{w}{h} \leq 1$ :

$$e_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left[ \left(1 + \frac{12h}{w}\right)^{-0.5} + 0.04 \left(1 - \frac{w}{h}\right)^2 \right] \quad (\text{C.5})$$

and for  $\frac{w}{h} > 1$ :

$$e_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + \frac{12h}{w}\right)^{-0.5} \quad (\text{C.6})$$

The equation for differential microstrip is slightly more complex. The odd mode impedance refers to differential microstrip driven with opposite (differential) signals, opposed to even mode which is driven with a common signal. This study was concerned with differentially-driven signals only and the odd mode impedance was therefore calculated using the following formula:

$$Z_{0,odd(0)} = \frac{Z_0(0) \sqrt{\frac{\varepsilon_{eff}(0)}{\varepsilon_{eff,odd(0)}}}}{1 - \frac{Z_0(0)}{\eta_0} \sqrt{\varepsilon_{eff}(0)} Q_{10}} (\Omega) \quad (\text{C.7})$$

where:

$$\varepsilon_{eff,odd(0)} = [0.5(\varepsilon_r + 1) + a_0(u, \varepsilon_r) - \varepsilon_{eff}(0)] e^{-c_0 g^{d_0}} + \varepsilon_{eff}(0) \quad (\text{C.8})$$

Only the primary formulae have been presented and the remaining variables can be found in [83]. Furthermore, there are additional equations necessary to correct for frequency-dependent dispersion which can be found in [48].

## C.2 SiPM Power Supply

The SiPM power supply consists of three stages and required a number of calculations to achieve the desired adjustable output voltage. These stages and calculations are discussed below.

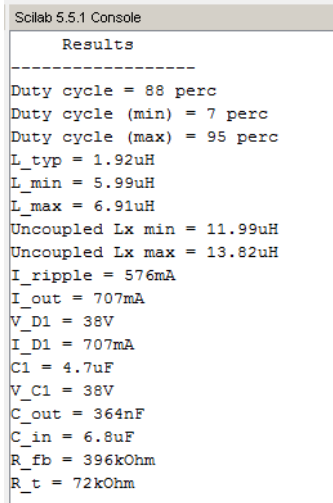
### C.2.1 Switch-Mode Converter

The switch-mode converter is required to generate a large negative voltage, with respect to ground, for further linear regulation. The driving constraints for the step-up switch-mode converter (LT3579) are as follows:

- minimum input voltage of 2.5 V
- minimum Off-Time of 34 ns
- minimum On-Time of 55 ns
- maximum combined switch current of 7.5 A

- max frequency of 2.8 MHz

A set of design formulae were available in the device’s datasheet. With the input voltage,  $V_{in}$ , set to 5 V and the output voltage,  $V_{out}$ , set to 33 V, a Scilab script, called “SMPS\_Calc.sce”, was developed to assist in the parameter calculations. The script’s results are shown in Figure C.2.



```

Scilab 5.5.1 Console
-----
Results
-----
Duty cycle = 88 perc
Duty cycle (min) = 7 perc
Duty cycle (max) = 95 perc
L_typ = 1.92uH
L_min = 5.99uH
L_max = 6.91uH
Uncoupled Lx min = 11.99uH
Uncoupled Lx max = 13.82uH
I_ripple = 576mA
I_out = 707mA
V_D1 = 38V
I_D1 = 707mA
C1 = 4.7uF
V_C1 = 38V
C_out = 364nF
C_in = 6.8uF
R_fb = 396kOhm
R_t = 72kOhm

```

Figure C.2: SMPS calculation results from SciLab

The first calculation determined the resultant duty cycle based on the input and output voltages. From the aforementioned timing constraints, the resultant duty cycle had to lie within the range of 7 to 95 % for the conversion from input voltage to output voltage to be possible.

$$DC = \frac{|V_{out}| + 0.5}{V_{in} + |V_{out}| + 0.23} = 88\%$$

The second step was to determine the value of the switching inductor. From the formula below it was clear that the inductance value was inversely proportional to the operating frequency. To keep the overall design as compact as possible, a higher frequency was preferable as the physical size of an inductor is usually inversely proportional to its value. After an iterative simulation process in Scilab, a frequency of 1.2 MHz was chosen.

$$L_{typ} = \frac{(V_{in} - 0.27) DC}{1.8f_{osc}} = 1.92\mu H$$

$$L_{min} = \frac{(V_{in} - 0.27) (2DC - 1)}{4f_{osc} (1 - DC)} = 5.99\mu H$$

$$L_{max} = \frac{(V_{in} - 0.27) DC}{0.5f_{osc}} = 6.91\mu H$$

The value calculated for the “typical” inductance was not within the minimum and maximum bounds and could therefore not be used. Instead, a readily available

value of  $6.8 \mu\text{H}$  was chosen for use as the coupled inductor as it fell within the upper and lower bounds. The lower bound describes the smallest inductor required to achieve the output voltage at a particular frequency. The upper bound ensures that the inductor does not reduce the ripple current beyond the discrimination ability of the converter, leading to poor regulation. This particular topology, with an inductor in series with the output, results in an inherently low-ripple output, ideal for the application.

The inductor ripple current refers to the amount by which the current in the inductor changes during a switching cycle and is different to output voltage ripple. It is usually a large fraction of the maximum output current and is calculated as follows:

$$I_{\text{ripple}} = \frac{(V_{\text{in}} - 0.27) DC}{f_{\text{osc}} L} = 576 \text{mA}$$

This value is well within the switch's combined current rating of 7.5 A. Using this value, the maximum output current could be determined:

$$I_{\text{out}} = \left(6 - \frac{I_{\text{ripple}}}{2}\right) (1 - DC) = 707 \text{mA}$$

This output current was significantly higher than necessary which makes future developments simpler, particularly if one switch-mode converter is to supply multiple linear regulators. At this particular voltage and current output, the recommended Schottky diode had to conform to the following minimum specifications:

$$V_R > V_{\text{in}} + |V_{\text{out}}| = 38 \text{V}$$

$$I_{\text{avg}} > I_{\text{out}} = 707 \text{mA}$$

In addition to these minimum ratings, the diode had to have a low parasitic capacitance to reduce reverse current spikes through the power switch. The series capacitor, C1, took the recommended value of  $4.7 \mu\text{F}$  and conformed to the following voltage rating:

$$V_{\text{rating}} > V_{\text{in}} + |V_{\text{out}}| = 38 \text{V}$$

C1 also provides a useful feature in that it disconnects the output voltage from the input voltage when the internal switch is open, thereby blocking any residual voltage from damaging components at the input when the device is switched off.

The minimum output capacitance is calculated as follows and required a minimum voltage rating of 33 V:

$$C_{\text{out}} = \frac{I_{\text{ripple}}}{0.04 \cdot f_{\text{osc}} |V_{\text{out}}|} = 0.364 \mu\text{F}$$

This value was much lower than the recommended value of 22 - 47  $\mu\text{F}$  and was therefore ignored. A total output capacitance of 47  $\mu\text{F}$  was used instead. The capacitors were chosen to have a low ESR to reduce the output ripple voltage and to supply reactive power for the application's small burst current requirements.

The input capacitor only required a voltage rating of 6 V and the minimum capacitance was calculated as follows.

$$C_{in} = \frac{I_{ripple}}{0.04f_{osc}V_{in}} + \frac{6DC}{0.2f_{osc}V_{in}} = 6.8\mu F$$

This value, again, seemed low considering the large current requirement so a larger value of 22  $\mu F$  was used instead. A low ESR ceramic capacitor was chosen to ensure the inductor ripple current could be adequately supplied.

The feedback resistor was responsible for setting the output voltage to the desired 33 V and was calculated as follows:

$$R_{fb} = \frac{|V_{out}| + 0.009}{83.3 \times 10^{-6}} = 396k\Omega$$

Finally, the timing resistor was responsible for setting the operating frequency and was calculated as follows:

$$R_t = \frac{87.6}{f_{osc}} - 1 = 72k\Omega$$

### C.2.2 Linear Regulator

The subsequent linear regulator acts both as a post-SMPS filter and as the adjustable regulation stage. The linear regulator's output voltage is set with a simple resistor divider and was calculated as follows:

$$V_{out} = V_{ref} \left( \frac{R_1}{R_2} + 1 \right)$$

where  $V_{ref} = -1.175$  V.

For a stable output voltage, sufficient current has to flow through the divider and satisfy the following inequality:  $\frac{|V_{ref(max)}|}{R_2} > 5\mu A$ . The output voltage was set to -22.325 V with a 180 k $\Omega$  and 10 k $\Omega$  resistors for R1 and R2 respectively. The reason for this particular voltage, as well as the external "DAC" signal connected to R9, will become evident in the next subsection.

### C.2.3 Current-Mode DAC

The current-mode DAC controlled the output voltage by converting a value received from a digital controller to an output current. To understand how current injection was able to change the output voltage, consider Figure C.3. When the DAC was set to output 0  $\mu A$  it had no effect on the resistor divider and therefore set the output as expected. The current through the divider was set by the 10 k $\Omega$  resistor because of its placement between two controlled voltages, namely ground (0 V) and Vref (-1.175 V):

$$I = \frac{V}{R} = \frac{0 - 1.175}{10k} = 117.5\mu A$$

The output voltage,  $V_{out}$ , was therefore:

$$V_{out} = IR = -117.5\mu \times (180k + 10k) = -22.325V$$

Therefore, during regular operation without any current injection, the output voltage is -22.325 V.

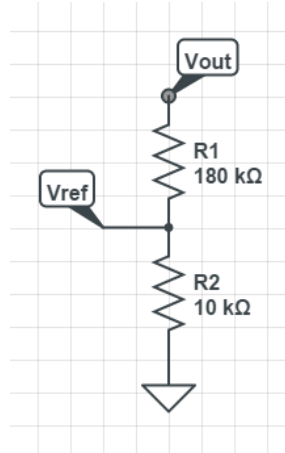


Figure C.3: Basic voltage-divider circuit

When the DAC was set to output the maximum current of  $50 \mu\text{A}$  at the point labeled “Vref”, the injected current flowed through the  $180 \text{ k}\Omega$  resistor to the smallest potential (Vout) adding to the current already set by the  $10 \text{ k}\Omega$  resistor. The new output voltage was therefore calculated as:

$$V_{out} = I_{R2}R_2 + I_{R1}R_1 = (-117.5\mu \times 10k) + [(-117.5\mu - 50\mu) \times 180k] = -31.325V$$

This resulted in a 9 V swing across the full range of the DAC, covering the required 24 - 30 V adjustable output with a few volts to spare at each end. With a 10-bit resolution the voltage resolution was:

$$\Delta V = \frac{9V}{2^{10} - 1} \simeq 8.8mV$$

## C.3 High Voltage Controller

The high-voltage controller was able to digitally adjust the output of an ORTEC 556 High Voltage Power Supply. The controller consisted of three main stages, discussed below, excluding the microcontroller and USB interface.

### C.3.1 Digital-to-Analog Converter

The high-voltage controller’s DAC is controlled via SPI and the output voltage is defined by the following function:

$$V_{out} = \left( \frac{D_{in}}{2^n} \right) \times V_{ref} \times Gain$$

where  $V_{ref}$  was 2.5 V when the internal reference was enabled (disabled by default),  $Gain$  was automatically set to a value of 2 and  $D_{in}$  is the 16-bit value written to the DAC from a digital controller.

### C.3.2 Unipolar-to-Bipolar Converter

The DAC's output is a unipolar voltage ranging from 0 to 2.5 V. The unipolar-to-bipolar circuit, presented in Chapter 3.4, converts this output into a bipolar voltage ranging from -6.9 to +6.9 V. The basic transfer function relating the input,  $V_{outA}$ , to the output,  $J2$ , is as follows:

$$J2 = \left[ 1 + \frac{R_8}{R_{13}} + \frac{R_8}{R_{12}} \right] V_{outA} - \frac{V_{ref} R_8}{R_{13}}$$

Based on this formula, the values for the different components were determined such that the full scale range of the DAC resulted in an output voltage range of -6.9 to +6.9 V. Capacitor C11 and resistor R14 were added for stability reasons and their values were determined through simulations, see File "Unipolar\_Bipolar.tsc". The opamp also acted as a buffer to drive the power supply's relatively low input impedance of 45 k $\Omega$ .

The resolution of the system, translating to the incremental voltage by which the bias voltage can be adjusted, was calculated as follows:

$$\Delta V = \frac{3000 - (-3000)}{2^{16} - 1} \simeq 92mV$$

### C.3.3 Power Rails

The high voltage controller requires voltage rails of  $\pm 10$  V to support the bipolar output control voltage. These rails are generated with Linear Technology's LT3471 dual switching regulator. The device's datasheet contains an application circuit that converts a 3.3 V input to a bipolar  $\pm 7$  V power supply. This particular circuit was modified slightly to support the conversion of a 5 V input to a  $\pm 10$  V power supply. The converter's duty cycle was calculated as follows:

$$DC = \frac{|V_{out}| + |V_D| - |V_{in}|}{|V_{out}| + |V_D| - |V_{CESAT}|}$$

where  $V_D$  is the diode's forward voltage drop and  $V_{CESAT}$  is 330 mV in the worst case.

The resultant duty cycle, assuming the above-mentioned input and outputs, was around 50 %, falling well within the duty cycle limits of 15 - 94 %. The resistor values required to set the non-inverting voltage output (+10 V), were determined using the following formula:

$$V_{out} = V_{FB1P} \left( 1 + \frac{R_{21}}{R_{22}} \right)$$

Similarly, for the inverting voltage output (-10 V), the resistor values were governed by:

$$V_{out} = -V_{REF} \left( \frac{R_{24}}{R_{26}} \right)$$

## C.4 5 V Supply

The SiPM digitizer requires a 5 V voltage rail capable of supplying around 12 A of current. To achieve this large output current, TI's TPS53353 synchronous buck converter was used as it incorporates the necessary switching MOSFETs. The supply's design is discussed briefly in Chapter 4.1.5, and the value calculations and motivations are addressed below. Only the primary formulae and variables are presented in the section and further details can be found in the device's datasheet.

The converter's switching frequency is set by connecting a particular value of resistor from its RF pin down to ground. A switching frequency of 500 kHz was chosen, based on a trade-off between efficiency and inductor size, which required that the RF pin be left open. However, to support any changes in the future, a DNP resistor was placed from the RF pin down to ground.

The converter has a power-good output that, when HIGH, indicates the switcher output is within its target output voltage range. The indicator pin is an open-drain output and therefore requires a pull-up resistor. Consequently, a 100 k $\Omega$  was placed from the pin up to  $V_{reg}$ . This output is not monitored by the SoC, as the 5 V supply powers the SoC, but it provides additional debugging capability for the testing phase of the study.

Incorporated into the buck converter is cycle-by-cycle over-current limiting, controlled by the resistor,  $R_{trip}$ , connected from the TRIP pin to ground. A set current,  $I_{trip}$ , of 10  $\mu$ A flows through the trip resistor and generates a trip voltage,  $V_{trip}$ . The voltage generated across the internal MOSFET is compared to the trip voltage. During an over-current, or short-circuit, condition the trip voltage will be exceeded and the regulator will be turned off. As described, the relationship between the trip voltage, current and resistance is:

$$V_{trip} = R_{trip} \times I_{trip}$$

The trip resistance can be calculated based on the MOSFET's thermally compensated on-time resistance value,  $R_{DS(on)}$  as follows:

$$R_{trip} = \frac{32R_{DS(on)} \left[ I_{OCP} - \left( \frac{1}{2 \times L \times f_{sw}} \right) \frac{V_{out}(V_{in} - V_{out})}{V_{in}} \right]}{I_{trip}}$$

Please see the device's datasheet for an explanation of the additional variables.

A 200 k $\Omega$  resistor was placed from the MODE pin to ground. This set a soft-start time of 2.8 ms and enabled auto-skip mode. Auto-skip mode is a feature offered by the TPS53353 converter that automatically reduces the switching frequency at light loads to maximize efficiency.

The inductor, L1P, was chosen to have a sufficiently high value to ensure a good signal-to-noise ratio while still being small enough to reduce core losses. This

value was identified by using the following formula with a ripple current setting of approximately 1/3 of the maximum output:

$$L = \frac{1}{I_{IND(ripple)} F_{SW}} \frac{V_{out} (V_{IN(max)} - V_{out})}{V_{IN(max)}}$$

Finally, the output voltage is set by two resistors, R4P and R5P. The calculation governing the output voltage is shown below:

$$R5P = R4P \frac{V_{out} - \frac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6}$$

## C.5 DRS4 Stage

### C.5.1 Sampling

The sampling frequency of the SCA can be adjusted between 700 MSPS and 6.2 GSPS and is governed by the following equation:

$$f_{ref} = \frac{1}{2048} \times f_{sampling}$$

where  $f_{ref}$  is the reference clock fed to the DRS4 from the FPGA (REFCLKx) and  $f_{sampling}$  is the desired sampling frequency. For example, if a sampling frequency of 2.048 GHz is required, a reference clock of 1 MHz must be applied to the differential REFCLKx inputs.

The reference clock was generated by the FPGA and transmitted to the DRS4 using the LVDS\_25 standard. A 100  $\Omega$  termination resistor, R4D, was placed at the clock input pins of the DRS4 to ensure optimal signal integrity. Furthermore, a 50 % duty cycle was used for the reference clock to ensure correct operation of the PLLCK status output, even though not necessary for the overall DRS4 operation. Finally, an external compensation filter was added (C18D, C19D and R3D) for the internal PLL which is dependent on the sampling frequency. The sampling process is discussed in more detail in Chapter 6.

The bias voltage for the internal buffers, relevant to the next two subsections, are nominally set to 0.7 V by default. To provide flexibility, one of the DAC channels was routed to control the DRS4's BIAS pin. For regular operation, a digital value of "18350" is transmitted to the DAC channel to apply the default 0.7 V setting.

### C.5.2 Input Stage

The DRS4 had a set of nine differential inputs with a 3 dB bandwidth of 950 MHz. A low-pass filter and re-biasing network was added between the second stage amplifier and the DRS4's inputs to avoid aliasing, see Figure C.4.

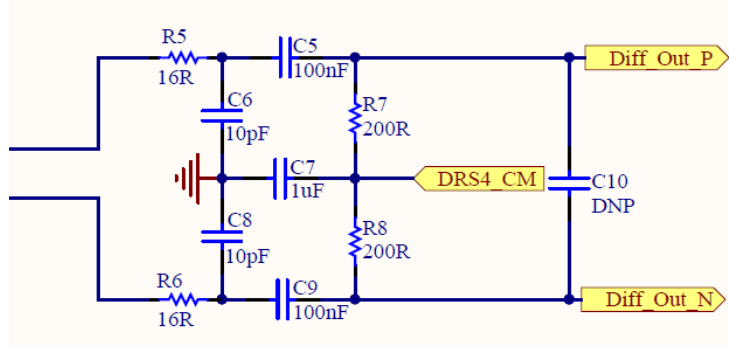


Figure C.4: Schematic of the rebiasing network for the DRS4 input stage

Each sampling cell consists of a capacitor ( $C_s = 150fF$ ), four NMOS transistors and a buffer, see Figure C.5. When the WRITE signal is HIGH the NMOS transistors allow for the capacitor to be charged to the differential voltage supplied by  $IN+$  and  $IN-$ . The voltage across the capacitor after a write cycle would therefore be:

$$V_C = V_{IN+} - V_{IN-}$$

The NMOS transistors have good linearity characteristics for input signals between 0.1 and 1.5 V. Furthermore, the readout buffer has good linearity characteristics for an input between 1.05 V and 2.05 V. In order to maintain operating voltages in this range the ROFS rail can be used to offset the voltage. The voltage then becomes:

$$V'_C = V_{IN+} - V_{IN-} + V_{ROFS}$$

Therefore, to support a differential input voltage of 0 - 1 V,  $V_{ROFS}$  would be set to 1.05 V. Similarly, to support a differential input voltage of -0.5 to 0.5 V,  $V_{ROFS}$  would be set to 1.05 V. Given that the preceding amplifiers and re-biasing network provides a differential input voltage of 0 - 1 V,  $V_{ROFS}$  is set to 1.05 V at startup by transmitting a digital value of “27525” to the relevant DAC channel. The default value of 1 V was used for the common-mode input voltage for the DRS4. This was achieved by transmitting a digital value of “26214” to the relevant DAC register.

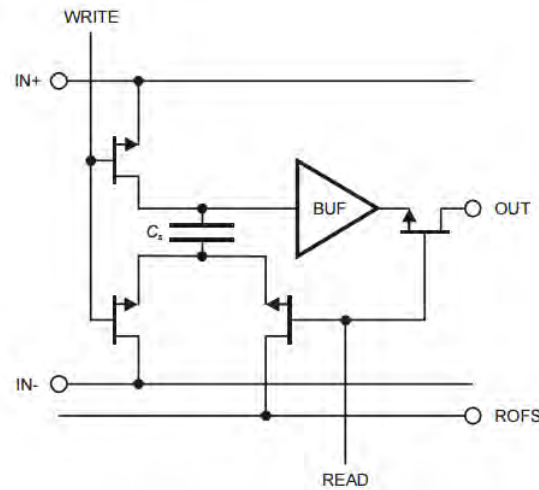


Figure C.5: Diagram of the DRS4's input stage[56]

### C.5.3 Output Stage

The DRS4's analog output can be sampled at rates ranging from 5 - 65 MSPS. Similar to the input stage, the output stage also contains a buffer which shifts the output range to 0.8 to 1.8 V. The overall gain from input to output is 0.985. To avoid signal degradation due to capacitor leakage, the outputs should be sampled within 1 ms of writing.

The output voltage can also be shifted by applying a voltage to the O-OFS pin, and is governed by the following equation:

$$U_{ofs} = \frac{U_+ + U_-}{2}$$

To obtain a differential output range of  $\pm 0.5$  V the default value of 1.37 V was applied to the O-OFS pin. This was achieved by transmitting a digital value of "35913" to the relevant DAC channel.

## C.6 ADC Stage

### C.6.1 Input Signal

An anti-aliasing filter and re-biasing network was placed between the DRS4's outputs and the ADC's inputs, see Figure C.6. The  $V_{cmx}$  outputs of the ADC were used to appropriately re-bias the input signal around half the 1.8 V supply voltage. Therefore, provided that the input signals remained within the power rail limits, and did not exceed  $1 V_{pp}$ , the DRS4's common-mode output voltage was irrelevant.

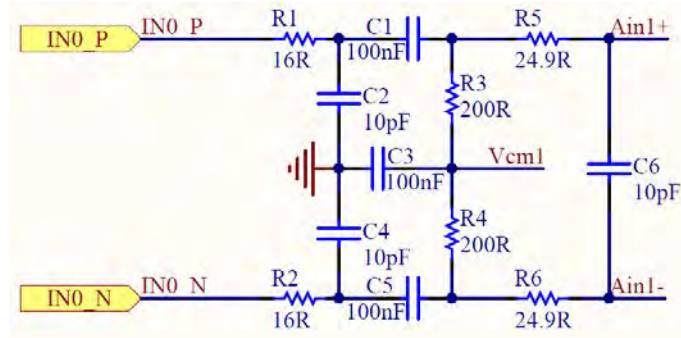


Figure C.6: Schematic of the re-biasing network for the ADC input stage

### C.6.2 Input Range

The ADC has a SENSE input that allows the input range of the ADC to be altered. By connecting the SENSE pin to the 1.8 V supply voltage, an internal reference is selected that supports a  $\pm 1$  V input range. When grounded, however, a different internal reference is used resulting in a  $\pm 0.5$  V input range. Although a  $\pm 0.5$  V input range was required, the option for both input ranges was reserved by placing a  $0 \Omega$  resistor from the SENSE pin to ground and a DNP resistor from the pin to supply.

# Appendix D

## SoC Overview

A brief overview of the Trenz TE0720 module and accompanying Xilinx Zynq SoC is provided in this Appendix.

### D.1 Trenz TE0720 Module

The TE0720 module is an industrial grade module that incorporates Xilinx's Zynq Z020 SoC. In addition to the SoC, the TE020 module also contains the following:

- 10/100/1000 tri-speed Gigabit Ethernet transceiver
- USB 2.0 high speed ULPI transceiver
- 32-bit-wide 1 Gbyte DDR3 SDRAM
- 32 Mbyte SPI Flash memory
- 4 Gbyte e-NAND
- temperature compensated RTC
- MEMS sensor (3D accelerometer and magnetometer)
- high-efficiency DC-DC power converters

Furthermore, the module provides access to 152 FPGA I/Os and 14 MIOs via three high-speed hermaphroditic connectors. Trenz had six different TE0720 modules available, ranging in the size of the DDR RAM and operating temperature range.

Mass is always an important consideration for spacecraft and the TE0720's low mass made it an ideal candidate for spaceflight. Once the board was received, new mass measurements were taken to get a true value. Figure D.1 shows two images of the module being weighed. The left image shows a mass of 14 grams for the bare SoC module. However, the right image shows a mass of 24 grams once the metal fasteners are added. This is a significant increase in mass for basic mechanical support.

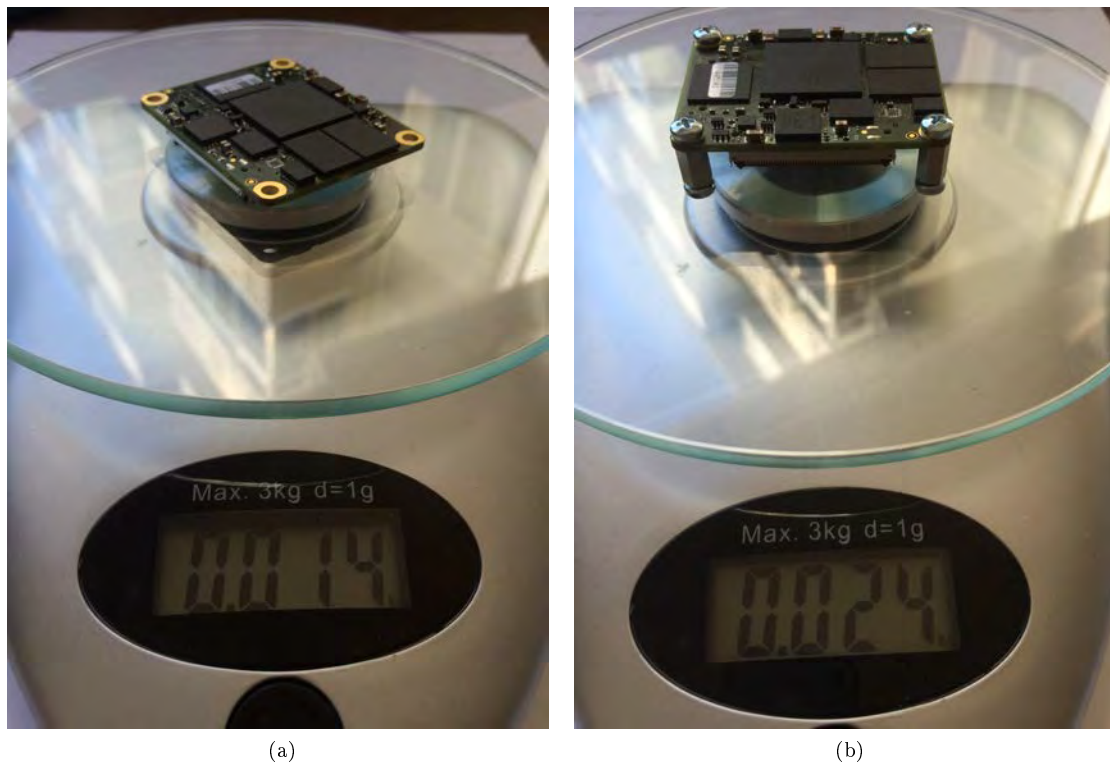


Figure D.1: Mass measurements of the SoC

## D.2 Xilinx Zynq SoC

As mentioned, the TE0720 module incorporates a Zynq SoC. The Zynq-7000 family has a range of different device options but all include the following base features[84]:

- Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
- NEON™ & Single / Double Precision Floating Point for each processor
- L1 Cache: 32 KB Instruction, 32 KB Data per processor
- L2 Cache: 512 KB
- On-Chip Memory: 256 KB
- External Memory Support: DDR3, DDR3L, DDR2, LPDDR2
- External Static Memory Support: 2x Quad-SPI, NAND, NOR
- DMA channels: 8 (4 dedicated to Programmable Logic)
- Peripherals: 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
- Peripherals w/ built-in DMA: 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO

- Security: RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot
- Processing System to Programmable Logic Interface Ports: 2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts
- Analog Mixed Signal (AMS) / XADC(2) 2x 12 bit, MSPS ADCs with up to 17 Differential Inputs
- Temperature Options: Commercial (0-85), Extended (0-100) and Industrial (-40 to 100C)

There are, however, significant differences between the various models, some of which are highlighted in the following table:

Table D.1: Zynq-7000 device comparison[84]

	Z-7015	Z-7020	Z-7045	Z-7100
Maximum Frequency	866 MHz	866 MHz	1 GHz	1 GHz
7-Series Equivalent	Artix-7	Artix-7	Kintex-7	Kintex-7
Logic Cells	74 K	85 K	350 K	444 K
Look-Up Tables	46,200	53,200	218,600	277,400
Flip-Flops	92,400	106,400	437,200	554,800
Block RAM	380 KB	560 KB	2,180 KB	3,020 KB
DSP Slices	160	220	900	2,020
DSP Performance	200 GMACs	276 GMACs	1,334 GMACs	2,622 GMACs
PCI Express	Gen2 x4	-	Gen2 x8	Gen2 x8
Serial Transceivers	4	0	8	16
Max Serial Speed	6.25 Gb/s	N/A	12.5 Gb/s	10.3125 Gb/s
Cost	\$160	\$115	\$1850	\$4500

The Zynq-7000 series consists of two main components, the processing system (PS) and the programmable logic (PL), see Figure D.2. The particle detector utilizes both the PS and PL and Chapter 6 describes the implementation of, and communication between, the two technologies.

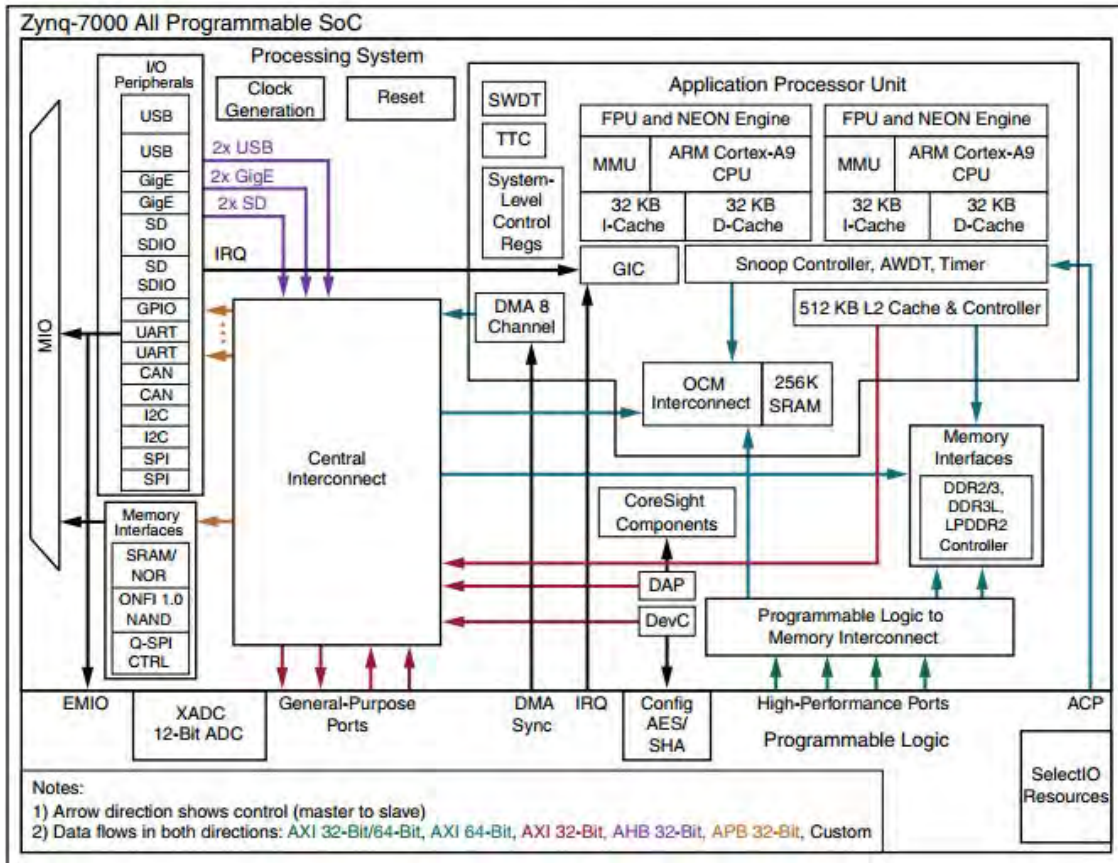


Figure D.2: Zynq-7000 SoC Overview[85]

# Appendix E

## PCB Layout

The following Appendix describes the various layout techniques used during the circuit board design process.

### E.1 Component Sizes

Small surface mount components (0402) were used for the large majority of the passive components due their their low parasitic capacitance and low inductance. These small components, as mentioned before, were also more suitable than their leaded counterparts due to their size relative to the wavelength of the signal propagating through the component.

### E.2 Plane Configuration

Ground layers were placed at layers 2 and 5, thereby allowing for high-frequency microstrip traces on the outer-most layers (1 and 6), see Figure 5.1. The alternative embedded stripline approach would have required a large number of vias from the components to the inner layers, leading to significant signal degradation.

Layers 2 and 5 were dedicated ground planes and were therefore unbroken throughout and provided increased EMI immunity. Analog and digital grounds were kept apart where necessary and joined in localized star configurations.

A power plane was located at layer 3, beneath the first ground plane. This layer provides a low-impedance power path from the voltage sources to the various components and also acted as an EMI shield. Furthermore, because of its placement adjacent to the ground plane, it acted as a capacitor (two adjacent conductors separated by an insulator) thereby providing inherent AC bypassing.

### E.3 Buried and Blind Vias

Buried and blind vias provide flexible routing ability in multi-layer stackups but unfortunately come at a cost. After a discussion with TraX, the most cost effective solution was blind vias only, limited to connecting layers 1 to 2 and layers 5 to 6. This allowed for easy and effective grounding where through-hole vias were prohibited by components and traces on the opposite side of the circuit board.

## E.4 Controlled Impedance Routing

Microstrip on the outer layers were used to distribute high-speed signals across the circuit board. Microstrip is a well understood technique that uses trace geometry and dielectric thickness to control the impedance of transmission lines. Although microstrip requires an “infinite” ground plane below the trace, a sufficient approximation is ground plane directly beneath the microstrip trace with a width five times that of the signal trace width.

There are many calculators for microstrip traces available but none of them provided agreeing results due to the different assumptions used to simplify the calculation. Therefore, a small SciLab script, “Impedance\_Calc.sce”, was written which implemented the original formula, defined in Appendix C.1, and did not make any assumptions. Figure E.1 shows an example of an impedance controlled area. The traces on the right are a set of differential, impedance controlled lines.

A spacing of three trace widths was used between all impedance controlled lines and the adjacent ground pour on the signal layers. TraX could only guarantee  $\pm 10\%$  accuracy on the controlled impedance lines and the minimum trace and gap widths are both 0.125 mm (4 mil).

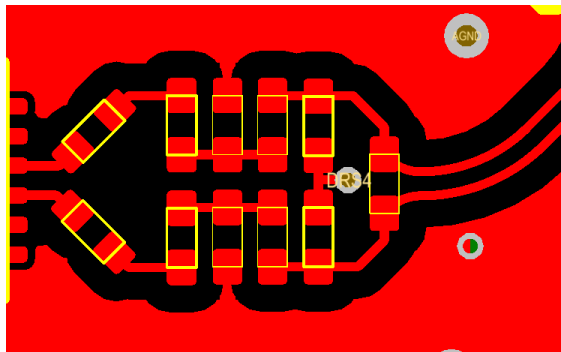


Figure E.1: Example of an impedance controlled area

## E.5 Connector Strengthening

Small RF connectors are notorious for breaking off their circuit boards. This issue is usually related to the bonding strength of the PCB copper to the substrate, rather than the solder connection of the connector to the copper. Therefore, to strengthen the pads, and create a more reliable RF connection, four vias were placed on each of the four MCX solder pads that extended all the way through the PCB to the opposite MCX connector pads, see Figure E.2.

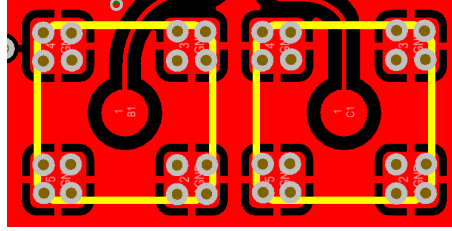


Figure E.2: MCX connector strengthening technique

## E.6 Ground Stitching

The design makes use of two dedicated ground planes and large ground pours on the signal layers to create a low impedance path to ground for the various components to minimize noise and crosstalk and to dissipate heat away from sensitive circuitry. Although the ground layers are very useful, they had to be carefully managed at high-frequencies to avoid the copper acting as stubs or transmission lines.

Consequently, ground stitching (vias connecting the different ground segments together) was used along the high-frequency signal paths, see Figure E.3. A general rule of thumb to ensure all ground segments act as a ground net is to place these vias an  $1/8$  of a wavelength (or less) apart. As an example, at 1 GHz, and  $1/8$ th of a wavelength in the Mercurywave substrate equates to 20 mm. At higher frequencies, such as 5 GHz, the stitching must be as close as 4 mm apart.

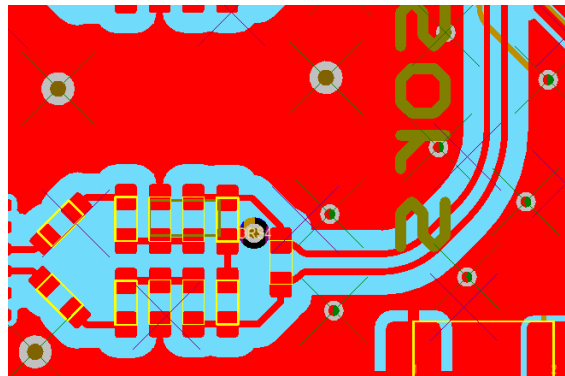


Figure E.3: PCB stitching along RF path

## E.7 Exposed Pads

All the components' exposed/thermal pads were connected to the signal layer ground pour, as well as the nearest ground plane. A large number of vias were used to connect the pad to the ground plane to minimize the total parasitic inductance of the connection and to provide even and effective thermal distribution, see Figure E.4.

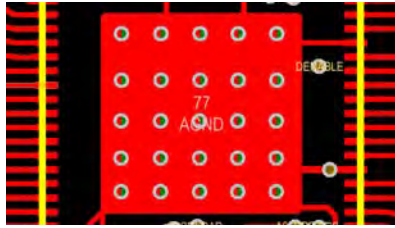


Figure E.4: Exposed pad connection to nearest ground plane

## E.8 Soldermask Pullback

Many of the supporting connectors and switches had guide pins that had to be accommodated on the circuit board, see the two large circles in Figure E.5 as an example. These guide pins did not connect to any net and acted only as mechanical support. To prevent the soldermask from inadvertently filling these holes, thereby reducing the radius and effectively blocking the hole, the mask was pulled back a  $1/4$  of a diameter of the hole size.

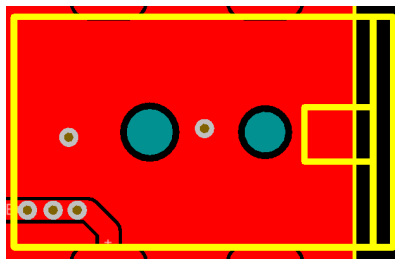


Figure E.5: Soldermask pullback to accommodate guide pins

## E.9 Ground Pour Cutout

Noise from the high-frequency amplifier ICs' outputs and surrounding circuitry can be coupled into its sensitive inputs if optimal layout techniques are not utilized. Furthermore, appreciable voltage gradients can cause board leakage currents leading to signal degradation. To mitigate these potential issues, the ground pour on the signal layer was cutout around the sensitive ICs. Although not necessary, guard rings could have been placed to further reduce these leakage currents. Figure E.6 shows two of the wideband amplifiers and the cutouts in the surrounding copper.

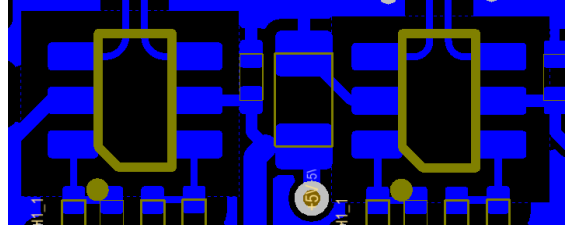


Figure E.6: Ground pour cutout around ICs

## E.10 Ground Pour Isolation

Switch-mode regulators generally generate more noise than their linear-mode counterparts. To reduce the amount of noise coupled into the rest of the circuitry, the surrounding ground pour was isolated on the signal side and only connected through a localized star grounding scheme near the regulator IC. Figure E.7 shows an example of ground isolation for the high-current output, 3.3 V regulator.

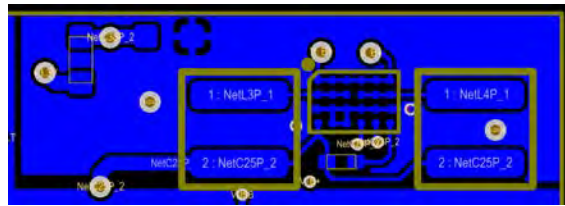


Figure E.7: Ground pour isolation around switching regulator

## E.11 Supply Decoupling

Power supply decoupling capacitors were placed as close to the various ICs on the circuit board as possible to minimize current loops. This was especially important near the high-speed digital circuitry which inherently generated more noise. Where possible, each decoupling capacitor used its own via down to the two primary ground planes to mitigate the effects of capacitive coupling.

### E.11.1 Design for Manufacture

In addition to following TraX's PCB manufacturing rules, the PCB layout and assembly was designed to conform to IPC's Class 3 standards. This included PCB footprints, soldering criteria, assembly etc.

To assist in the soldering and assembly process, all component footprints were designed individually. All solder pads had rounded edges to create a more natural solder joint with an adequate fillet at both the front and aft of the leads. These

joints also provide balanced surface tension, reducing the probability of passive components “tombstoning”<sup>1</sup>.

The assembly house, Barracuda, required that the circuit board edges were free of components for their tools to grip the board but because of the board’s high density, there were no exposed edges. Therefore, a 10 mm edge was added to each side of the circuit board making up the assembly panel. For easy removal of the additional edging, four V-score lines were placed along the limits of the PCB.

Barracuda also required that the PCB incorporated fiducials with a 1.5 - 2 mm diameter and a surrounding copper clearance of one radius on both sides of the circuit board. Two global fiducials were placed at the extremities of the assembly panel, providing the best accuracy. However, once the edges were snapped off these fiducials were no longer available. Therefore, to allow for later rework, two additional local fiducials were placed on the PCB itself.

Finally, Barracuda was tasked with laser cutting a stencil for the application of solder paste.

---

<sup>1</sup>Tombstoning is the partial or complete lifting of passive surface-mount components during the reflow process

## Appendix F

# Additional Documentation

This final appendix chapter contains all additional document relevant to the study. The documents appended, in order of appearance, are as follows:

1. Final circuit board stackup document provided by TraX
2. Final quotation from TraX for the fabrication of two SiPM digitizer circuit boards
3. Final quotation from Barracuda for the manufacture of a laser cut stencil and assembly of one SiPM digitizer circuit board
4. Circuit diagram of the Sensl MicroFB-60035 breakout board
5. Circuit diagram of the digitally adjustable SiPM power supply (basic version)
6. Circuit diagram of the digitally adjustable SiPM power supply (fully-integrated version)
7. Circuit diagram of the high-voltage power supply controller
8. Circuit diagrams of the SiPM digitizer circuit board

**MULTILAYER TABLE -6 Layer Stackup**

**Special - All materials are MW9350**

**SPEC.**

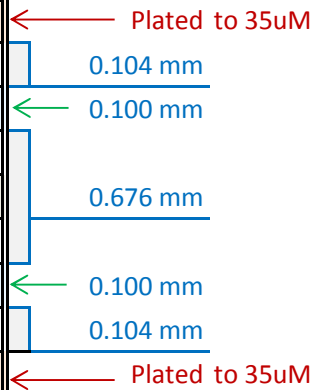
Finished	=	1.29 mm	
a. Innerlayers	=	0.10 mm	Core
	=	35 μm	Copper
b. Innerlayers	=	0.51 mm	Core
	=	00 μm	Copper
Prepreg	=	1080 x 2	
Prepreg	=	2116 x 2	
Foils	=	17 μm	
Pressed	=	1.19 mm	

Note: 0.51mm core used (with copper removed for building up to required dielectric thickness)



Item	Material	Type	Thickness (effective)
1	Copper foil	17 micron	0.015
2	Pre-preg	2116	0.104
4	a Innerlayer 2+3	0.10 mm 35 μm	0.140
5	Pre-preg	1080	0.083
7	a Core layer	0.51 mm	0.510
9	Pre-preg	1080	0.083
10	a Innerlayer 6+7	0.10 mm 35 μm	0.140
11	Pre-preg	2116	0.104
13	Copper foil	17 micron	0.015
		Pressed thickness	1.194
	Plating + mask	100 micron	0.100
	etc.		
		TOTAL mm.	1.294

Dielectrics [Er=3.5]



Note 1: This stackup is shown using MW9350 materials that TraX presently have in stock.

The 0.1mm inner layer is shown with 35 micron copper because this is all we have in 0.1mm.

Note 2: If a similar stackup is needed in RO4350B / RO4450B (bond ply), then the customer would have to supply the materials.



Vat Reg No. 4540118413

2 Estmil Road  
Diep River  
Cape Town 8000  
Tel : (021) 712 5011  
Fax : (021) 712 5798  
P.O. Box 180  
Plumstead 7801  
South Africa

Reg. No. 1991/00696/07

Invoice to : UNIVERSITY OF CAPE TOWN  
CREDITORS SECTION  
FINANCE DEPARTMENT  
PRIVATE BAG X3  
RONDEBOSCH  
7701  
Ph : 021650 4534/3336  
Fax : 021 650 3663

Deliver to :

13 February 2015

Your Ref :  
Attention : DAYNE KEMP

**QUOTATION FOR PRINTED CIRCUIT BOARDS (Quote #1039767)**

Part Number: SIPM\_DIGITIZER  
Issue/Revision: 1.1  
Board Quantity: 2  
Panel Quantity: 2  
Boards per Panel: 1

Board Length x Width (mm): 102.0 x 71.1  
Panel Length x Width (mm): 120.0 x 89.0  
Panel Area (cm<sup>2</sup>): 106.8  
V-Score: Yes  
Rout: Yes  
Bare Board Test: Flying Probe

Number of Layers: 6-Layer  
Material Type: Mercurywave  
Board Thickness (mm): 1.3  
Final Cu Thickness(μm): 35  
Final Finish: ENIG  
No. of Gold Tabs: 0  
No. of Holes/Board: 1345

Component Side Legend: White  
Solder Side Legend: White  
Component Side Mask: Green Matt  
Solder Side Mask: Green Matt  
Peelable Ink/Conductive Ink: No/No  
Conformance Certificate: No  
Batch Coding: No

**BOARD COSTS**

2 Board/s @ R 1578.15 / board  
2 Panel/s @ R 1578.15 / panel  
Total Board Price: R 3156.30

**ONCE OFF SETUP**

Origination: R 1730.00  
Bare Board Test Jig: R 0.00  
Flying Probe: R 220.00  
Paste Plot CS: R 0.00  
Paste Plot SS: R 0.00  
Paste Stencil CS: R 0.00  
Paste Stencil SS: R 0.00

**TESTING & SUNDRIES**

Flying Probe @ R 157.82 / board  
Flying Probe Total: R 315.64  
Sundries: R 0.00

**TOTALS**

Subtotal: R 5421.94  
VAT: R 759.07  
Invoice Total: R 6181.01

Factory Completion Time: 12 working days  
Terms of Payment: 30 days  
30 days net

**Please Note:**

- \* This quotation is valid for 4 Weeks.
- \* The price is subject to review should production data vary from information supplied for this quotation.
- \* Origination is a once off cost but becomes applicable for changes in production data.
- \* All sales are subject to our standard terms and conditions of sale.
- \* The Factory Completion Time is calculated from the date of order, provided finalised production files are received no later than 12h00 on that day.
- \* Please allow up to 2 days for delivery, unless arrangements have been made for collection.

Kind Regards  
Anton Tait

Doc No. 7.2.1\_1

# Barracuda Holdings (Pty) Ltd

Unit 1, Bataleur Park  
Olive Grove Industrial Estate  
Ou Paardevlei Road

Telephone **+27(0)218513357**  
Fax **+27(0)862106255**

# Quotation

PO Box 544  
Somerset Mall  
7137

Registration **1995/013557/07**

Page 1 of 1

**To:**  
**UNIVERSITY OF CAPE TOWN**  
Upper Campus  
University of Cape Town  
Rondebosch  
7700

**Document No.**   
**Account**   
**Date**

<u>Item Code</u>	<u>Item Description</u>	<u>Details</u>	<u>Quantity</u>	<u>Price /Unit</u>
1000	PCB Assembly Multi-FMC		1	3184.03
1000	Laser Cut Stencil ( will try fit both top and bottom onto one sten		1	2922.00

**Please Note - This quotation is subject to the following:**

- All prices are VAT exclusive and valid for 7 days unless specified otherwise.
- Prices exclude specialised packaging.
- Prices are based on information supplied to Barracuda at the time of quoting.
- Where facts or information are not apparent / disclosed at the time of quoting and these affect the cost of production, the customer will be liable for these additional costs.
- Prices quoted are based on uninterrupted production flow - all changes / deviations / delays caused by the customer will incur additional charges.
- Delivery is quoted as Ex-Works.
- Products containing imported materials are subject to ROE variations and will be invoiced at the prevailing ROE at the time of the materials payment unless specified otherwise above.
- No cancellations, returns or deferments will be accepted once the order has been placed and confirmed by Barracuda.
- Free issued materials:
  - Must be clearly marked with all part information and quantity supplied .
  - Packaged appropriately for automated assembly where assemblies are required to be machine assembled.
  - Components on tape and reel must have at least 20cm of leader or additional components for feeder insertion.
  - Supplied with sufficient additional quantity in order to cater for automated assembly machine drop-out ( 2.5% typical on tape and reel components).
  - Free issued materials are not covered by Barracuda Holdings insurance policy and the customer is responsible for appropriate insurance while materials are on the premises of Barracuda .

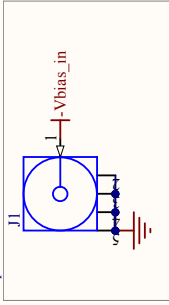
A

B

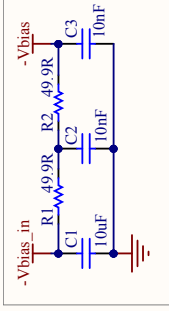
C

D

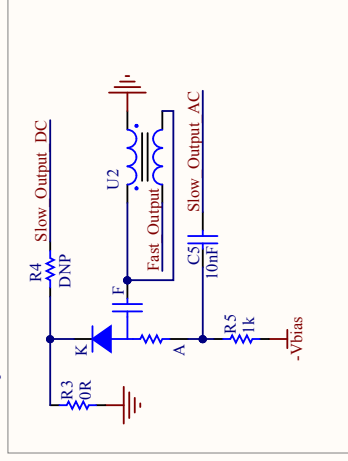
Input



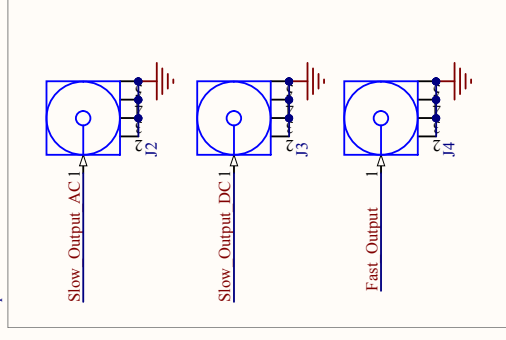
Power Filter



SIPM Setup



Outputs

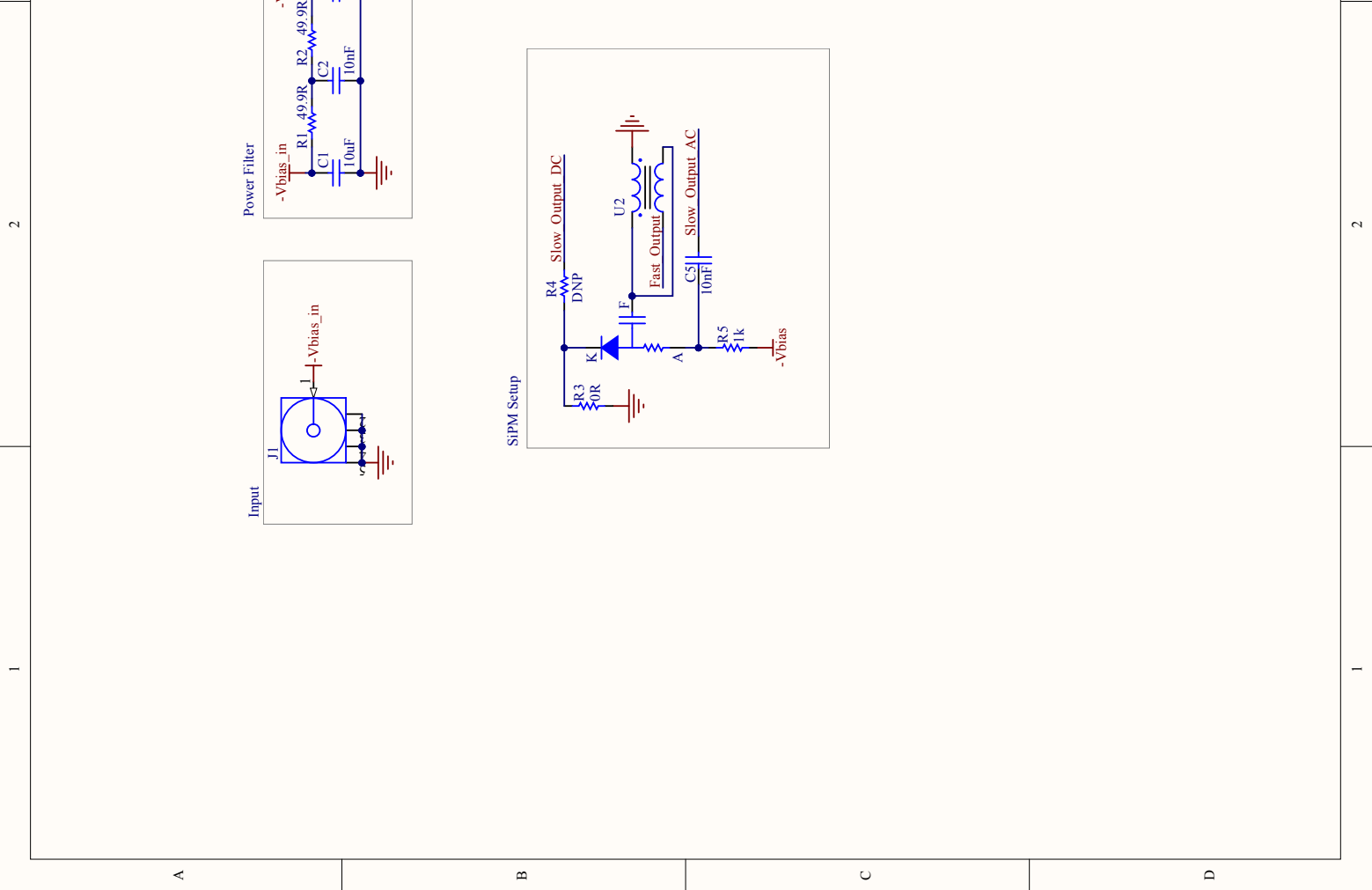


A

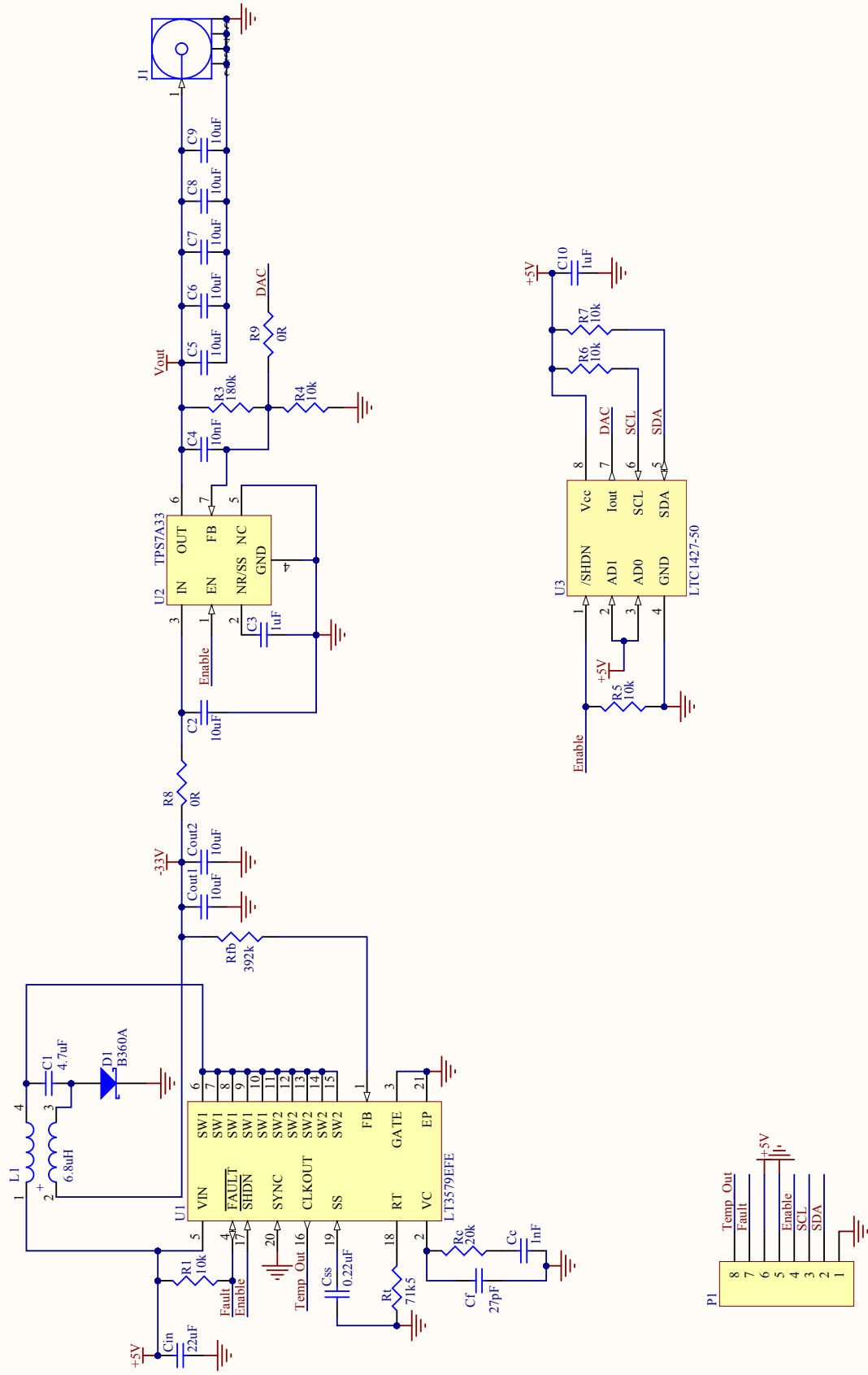
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C

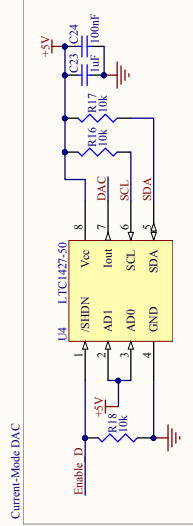
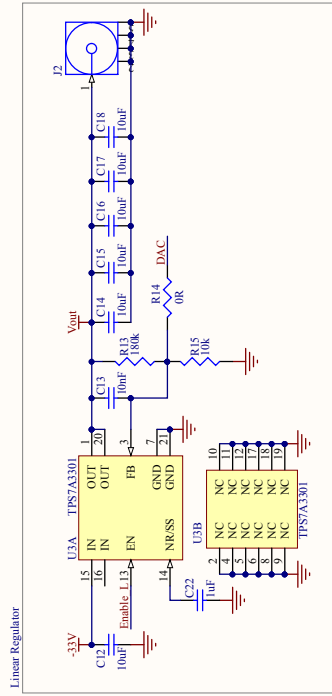
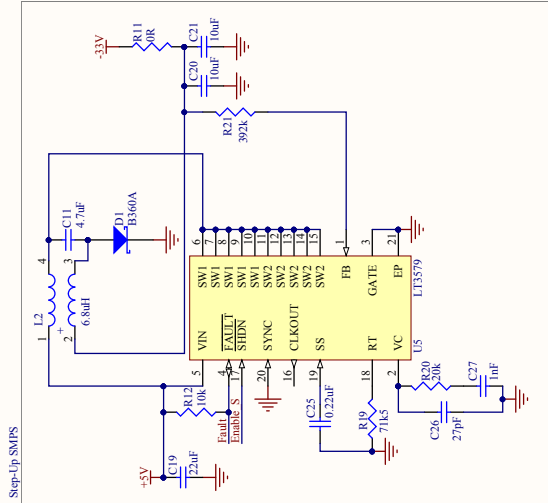
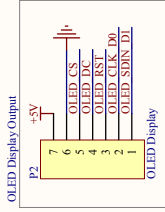
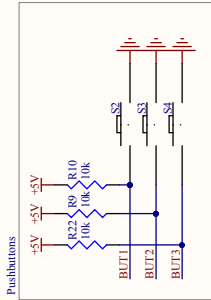
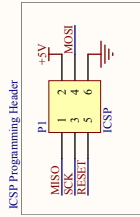
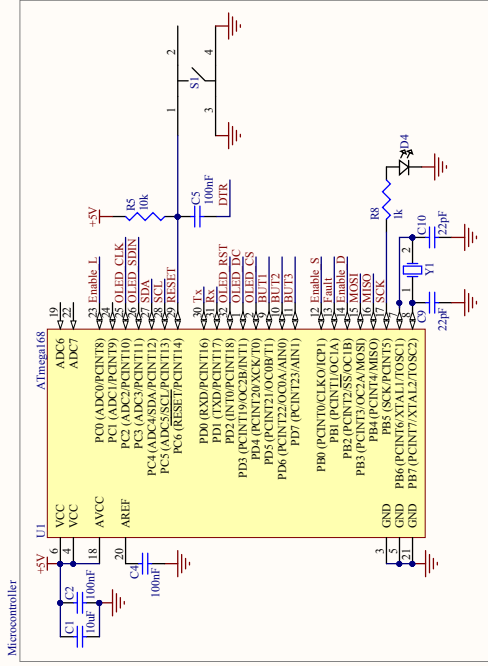
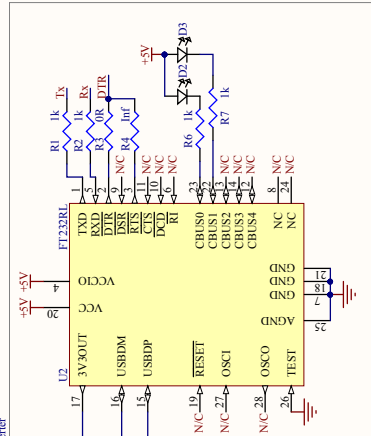
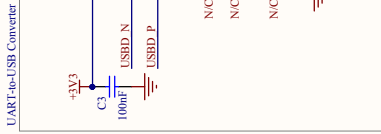
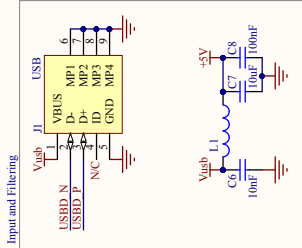
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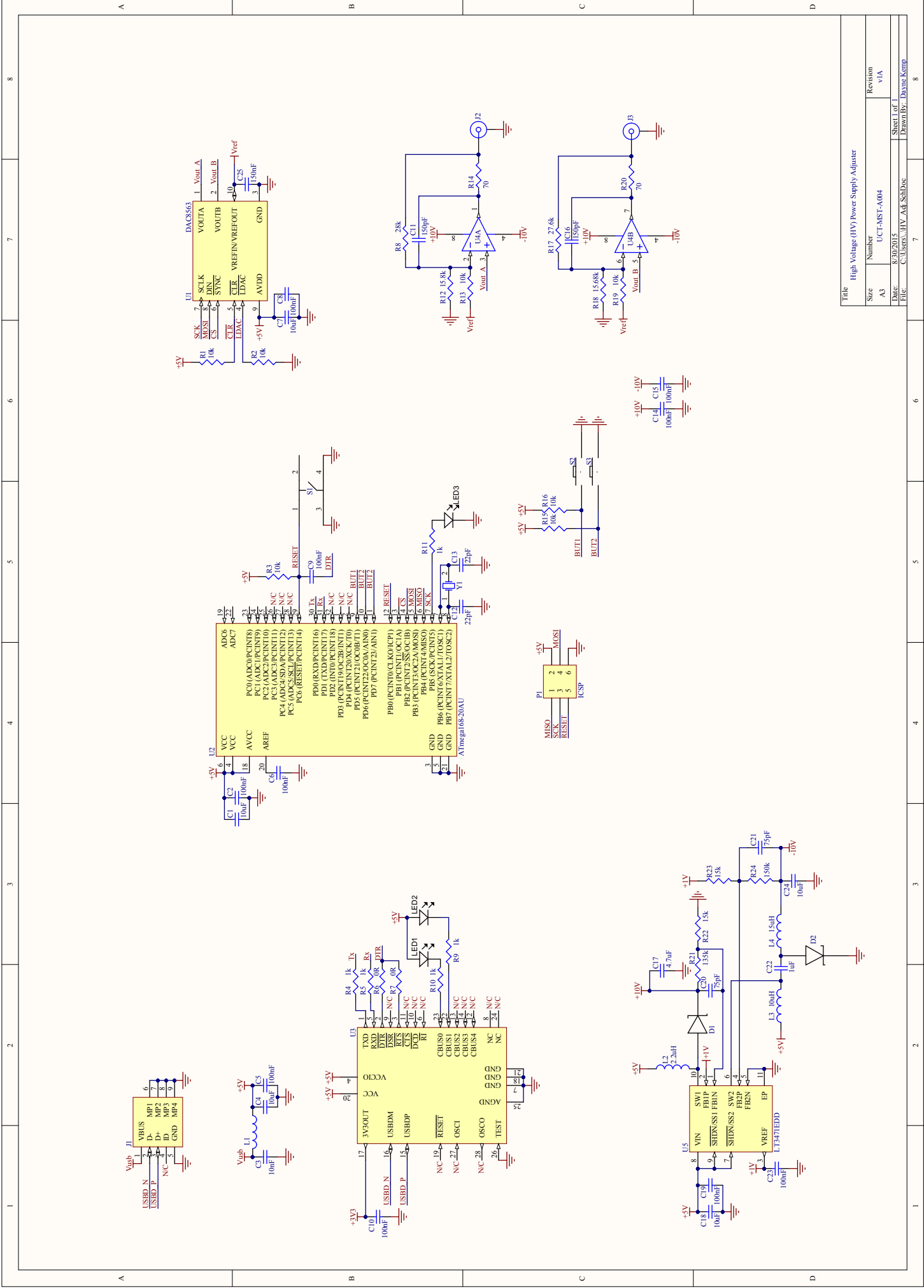
Title				MicroFB 60035 Breakout Board				
Size	Number	Revision		v1A				
Letter	UCT-MST-A005							
Date:	7/6/2015	Sheet	of	1	1			
File:	C:\Users\...MicroFB60035 Breakout.Sch						Drawn By:	Dayne Kemp



Title		Digitally Adjustable SiPM Power Supply	
Size	Number	Revision	v1A
Letter	UCT-MST-A001		
Date:	7/6/2015	Sheet 1 of 1	
File:	C:\Users\...Power_Supply_SchDoc	Drawn By:	Dayne Kemp

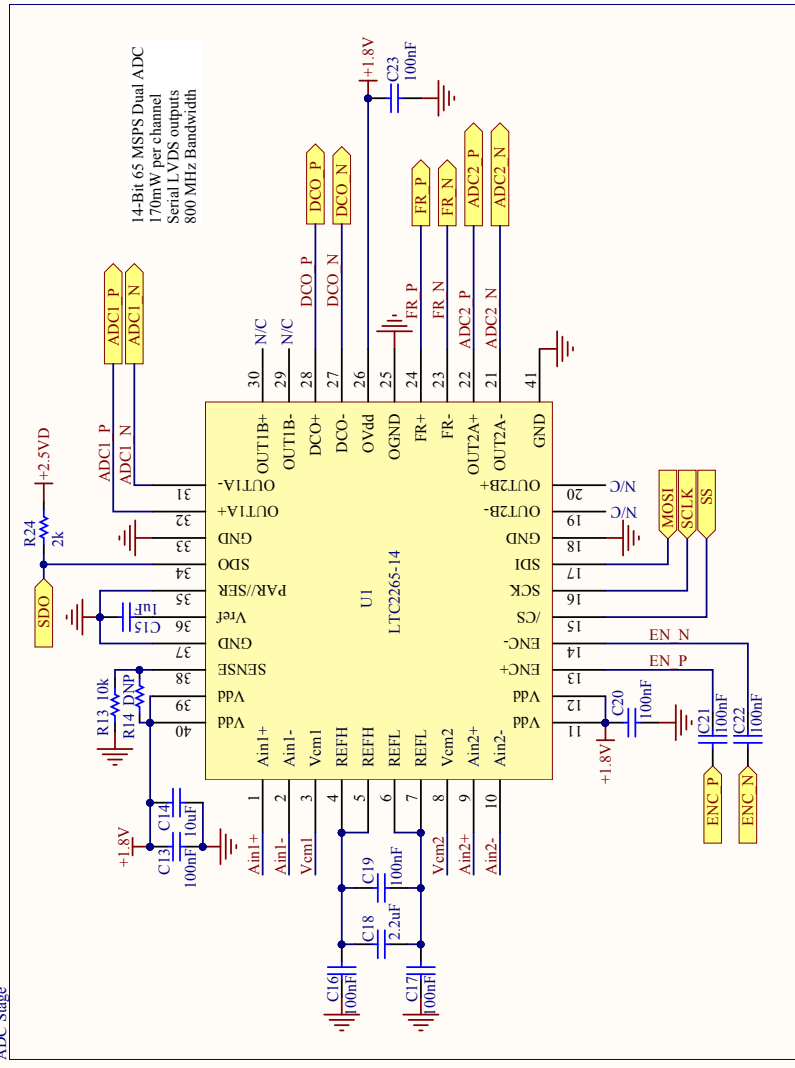


Title		Digitally Adjustable SPWM Power Supply with Microcontroller	
Size	Number	Revision	v1A
A3	UCT-MST-A002	Date:	7/6/2015
File:	C:\Users\ASPM\Supply_SchDoc	Sheet 1 of 1	
		Drawn By:	Davone Kemp

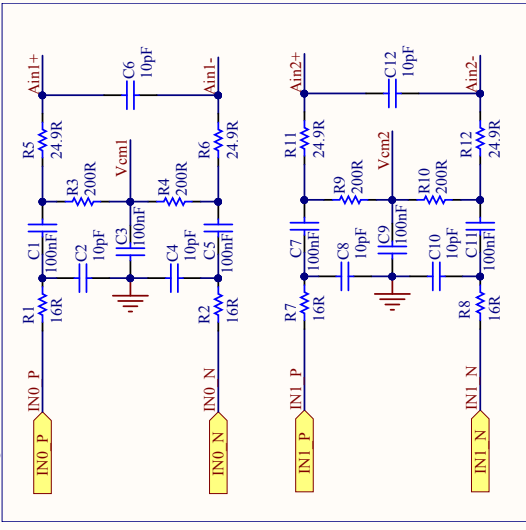


Title		High Voltage (HV) Power Supply Adjuster	
Size	Number	Revision	v1A
A3	UCT-MST-A004		
Date:	8/30/2015	Sheet 1 of 1	
File:	C:\Users\AIV_Ash\ShDoc	Drawn By:	Dayne Kemp

ADC Stage



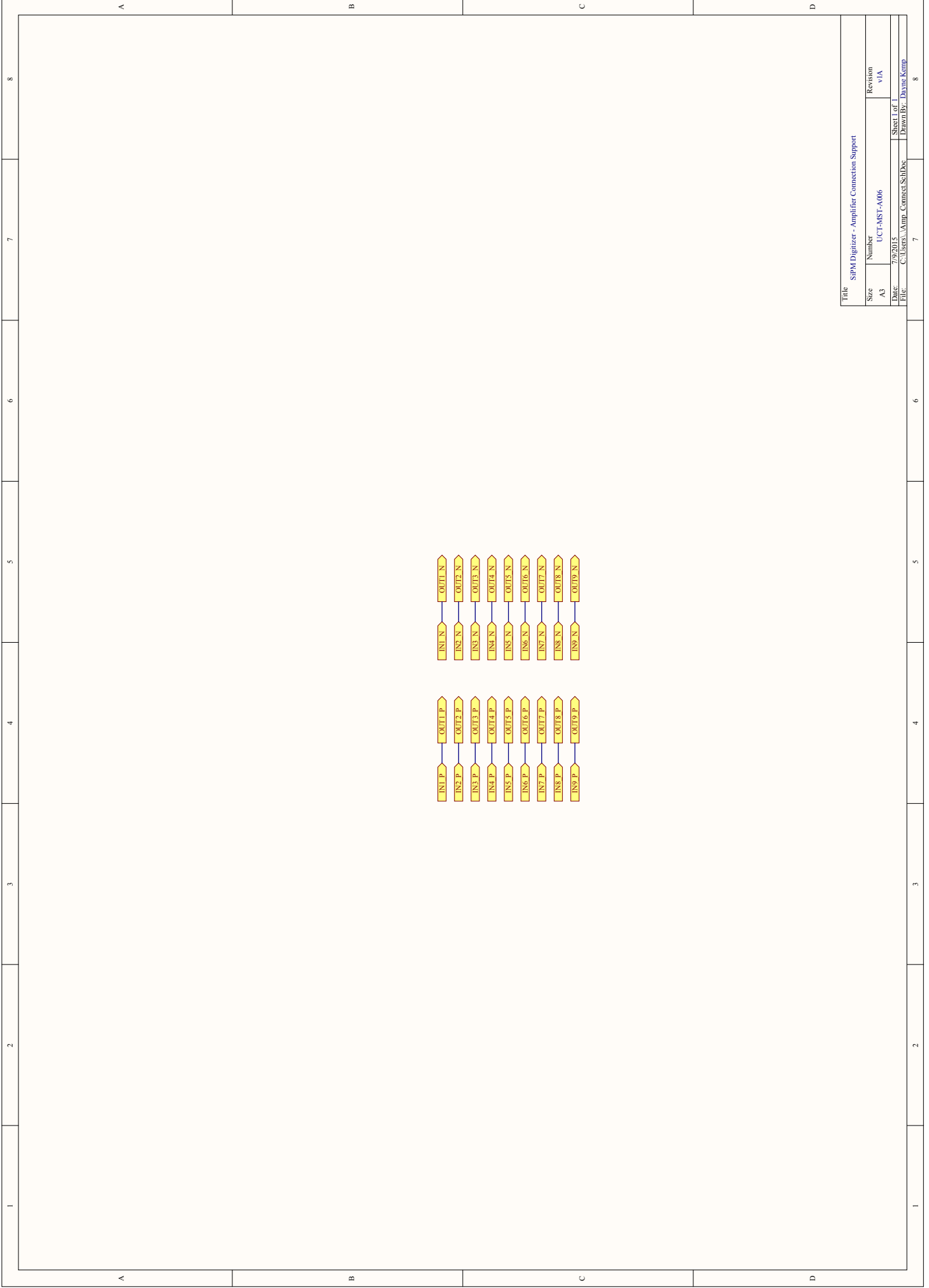
Re-biasing for ADC



Title: SIFM Digitizer - ADC Stage

Size	Number	Revision
A4	UCT-MST-A006	V1A

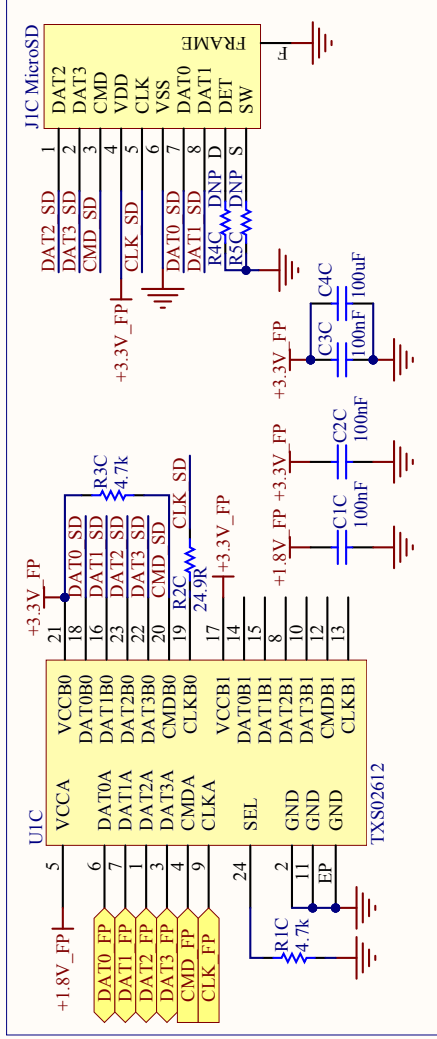
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\...ADC Stage.SchDoc	Drawn By: Dayne Kemp



Title: SIPM Digitizer - Amplifier Connection Support

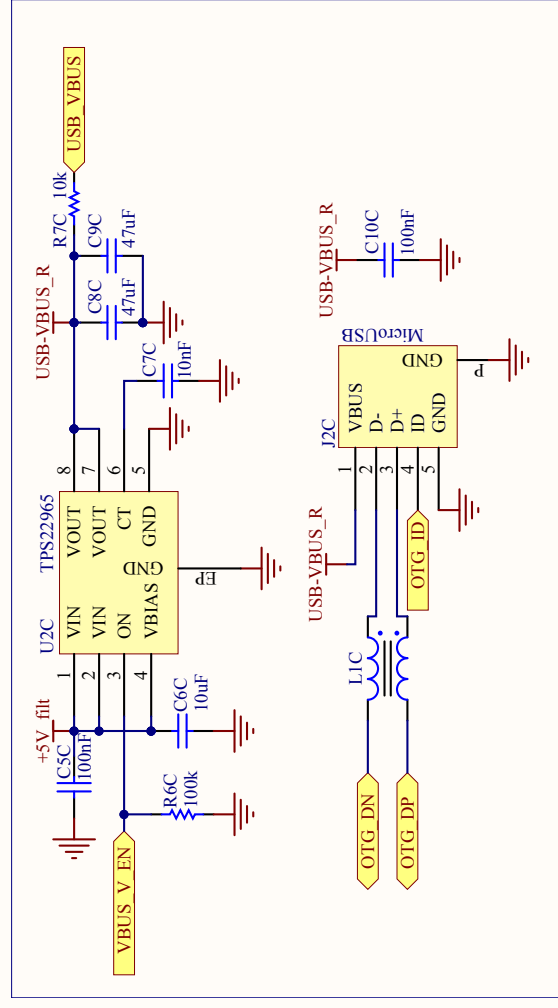
Size	Number	Revision
A3	UCT-MST-A006	VIA
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\j\App\Connect_Sch.Dwg	Drawn By: Dayne Kemp

MicroSD for Boot



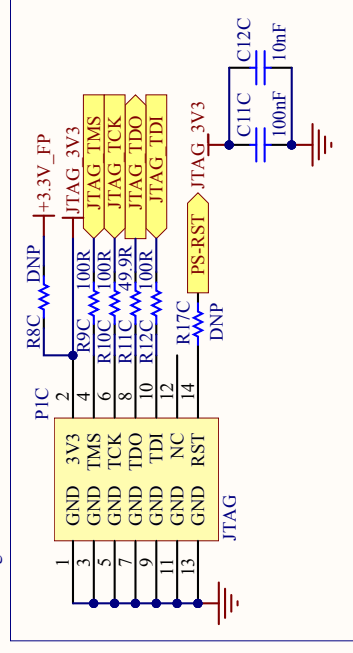
A

USB 2.0 Connector



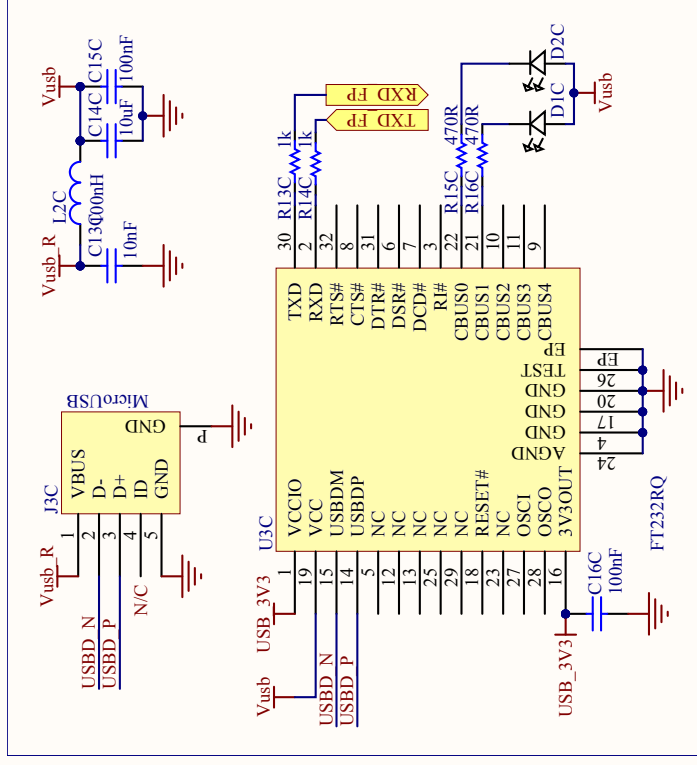
B

JTAG Programmer



A

USB-UART Converter



B

C

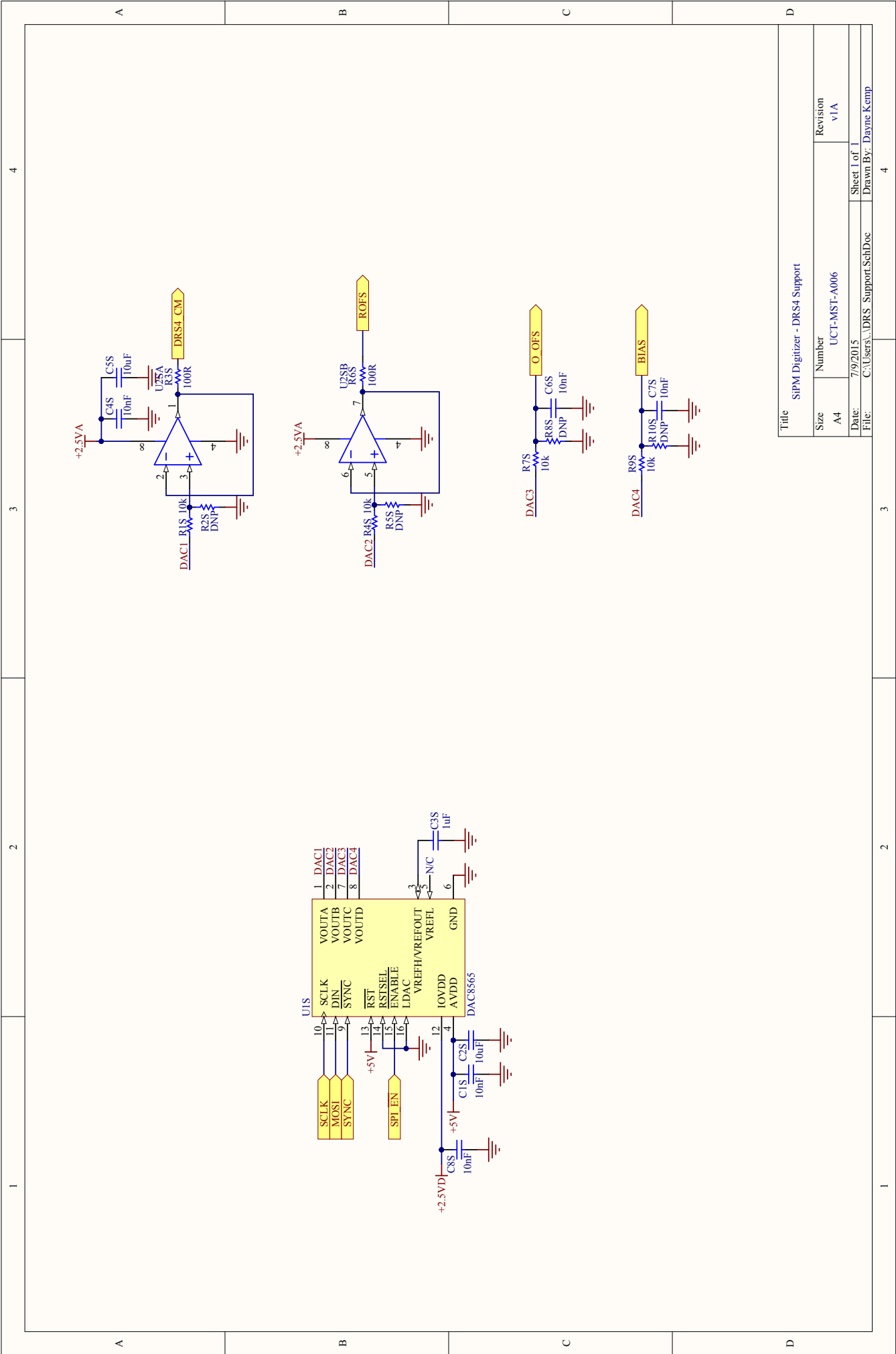
Title: SiPM Digitizer - Programming, Communication and Additional Feature Support

Size: A  
Number: UCT-MST-A006  
Revision: v1A

Date: 7/9/2015  
File: C:\Users\...Data\_Connectors\SchDoc

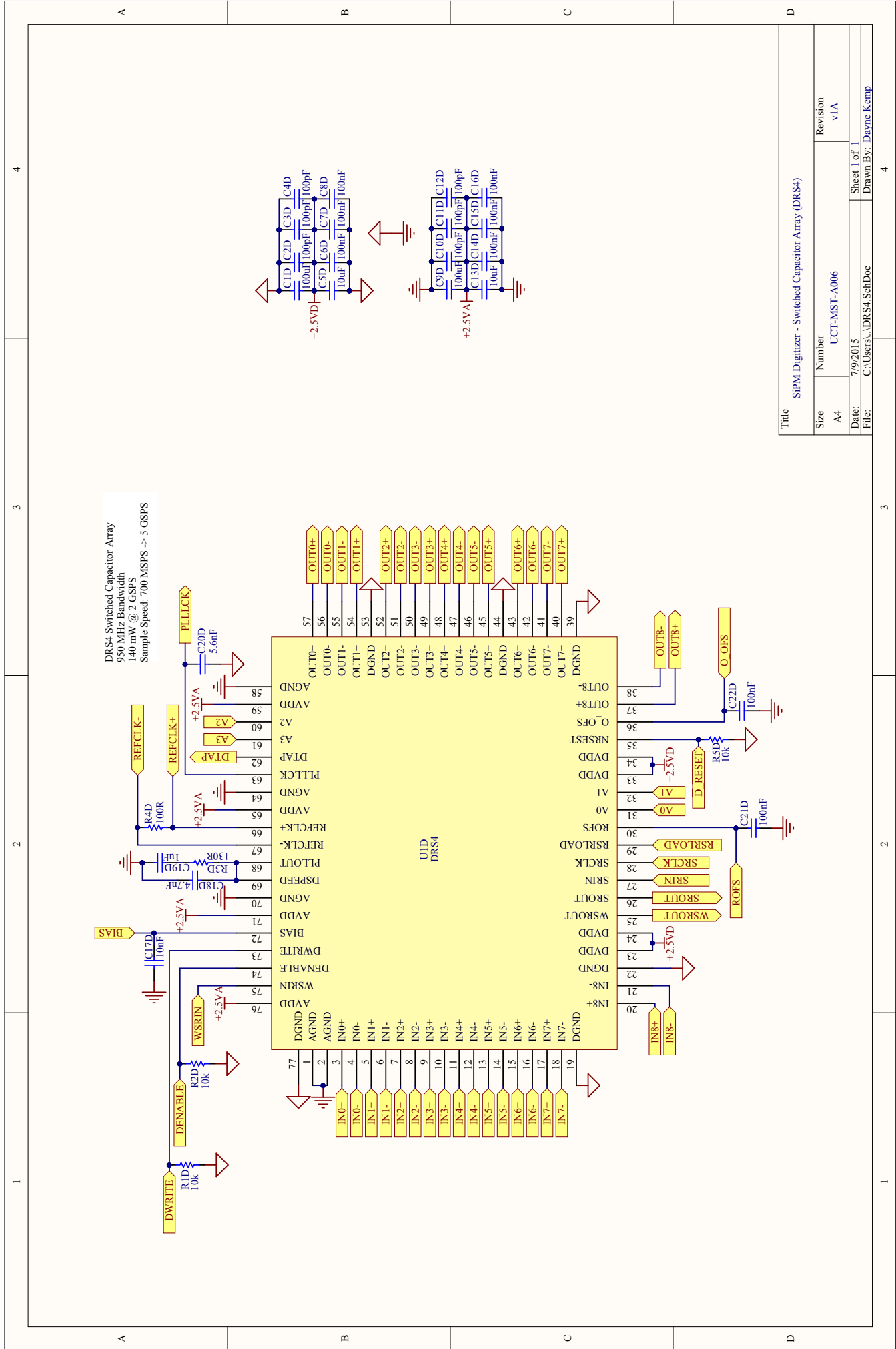
Sheet 1 of 1  
Drawn By: Dayne Kemp

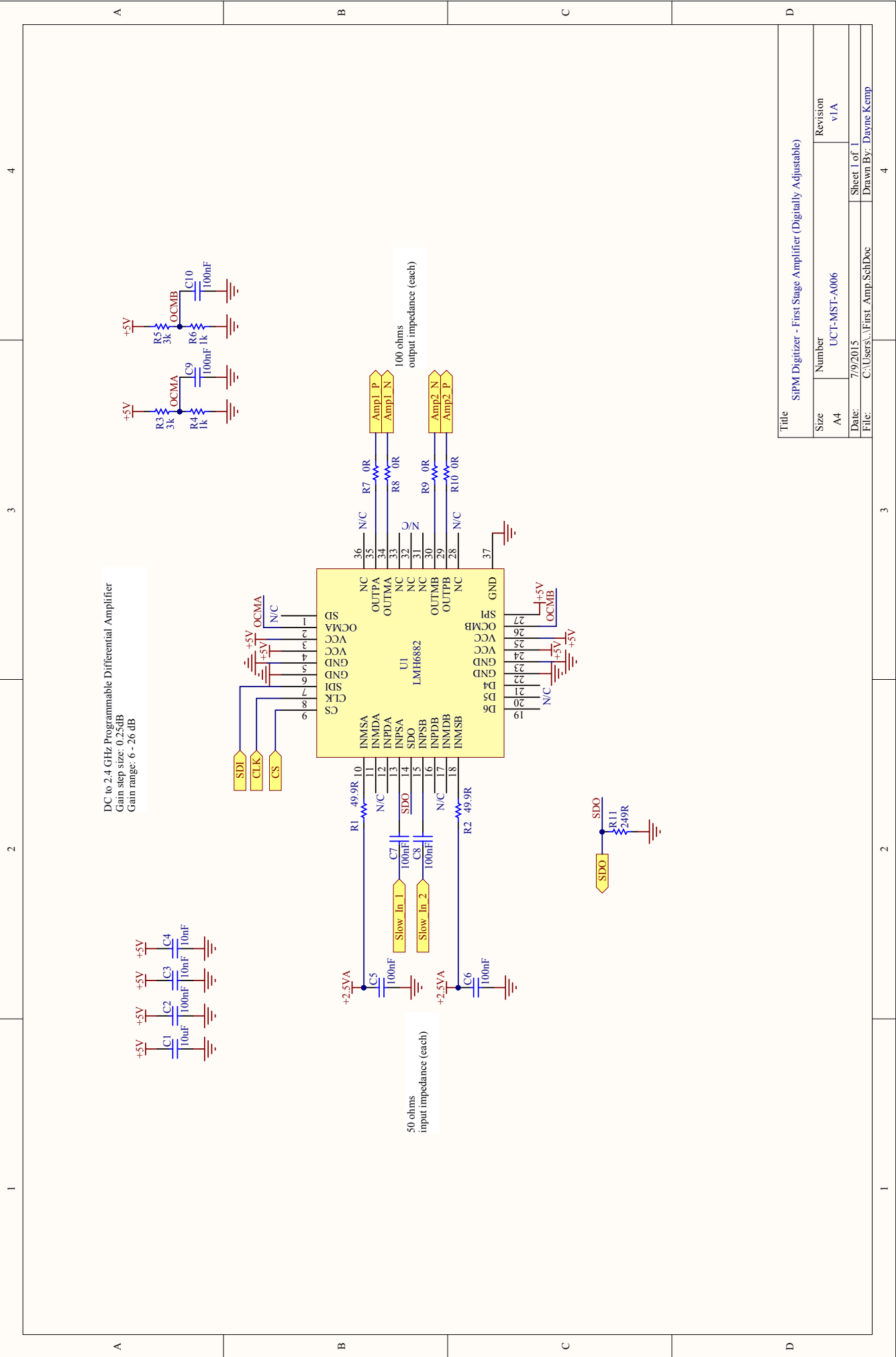
D



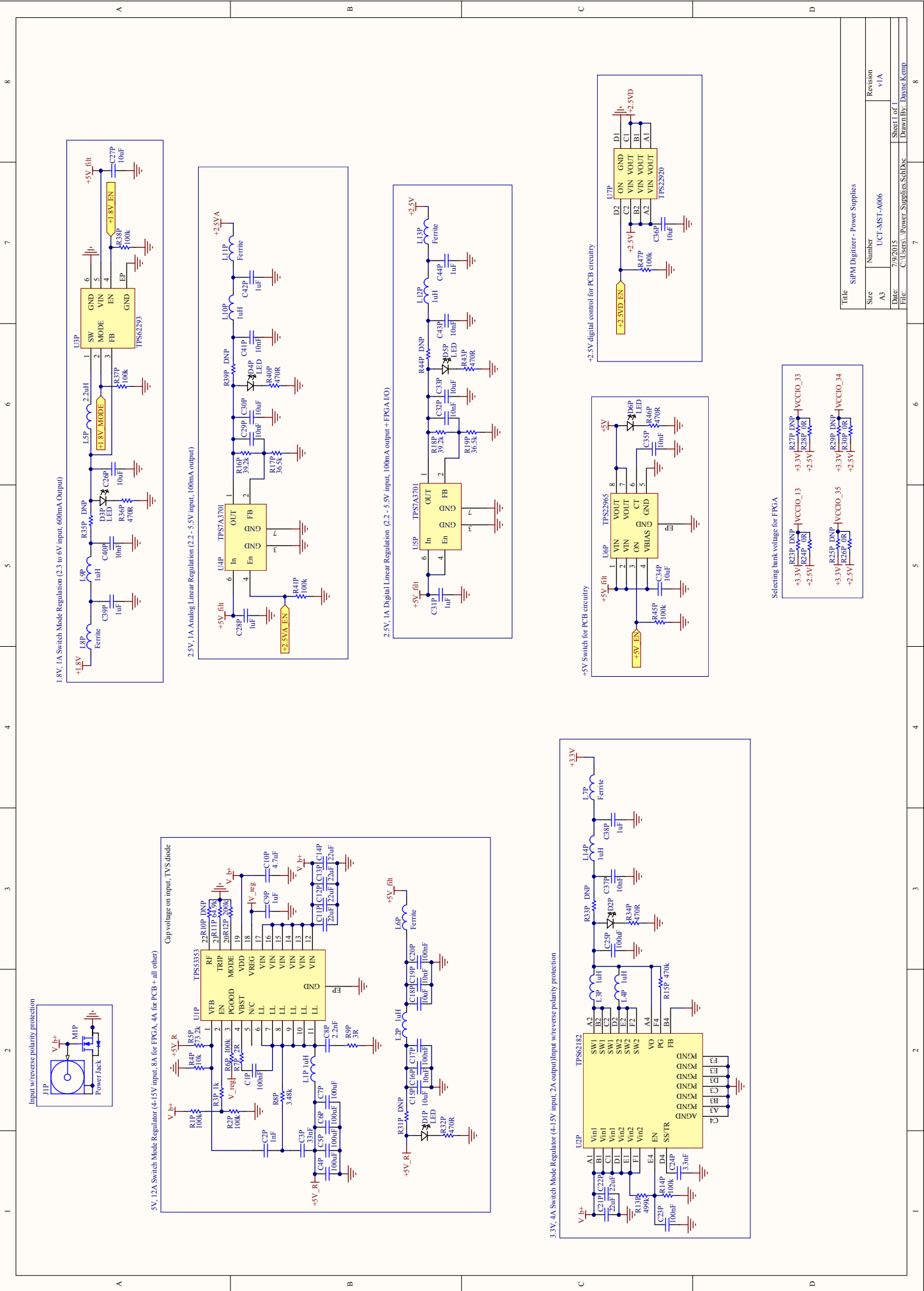
Title: SIFPM Digitizer - DRS4 Support

Size	Number	Revision
A4	UCT-MST-A006	V1A
Date:	7/9/2015	
File:	C:\Users\... \DRS4_Support_SchDoc	





Title		SIFPM Digitizer - First Stage Amplifier (Digitally Adjustable)	
Size	Number	Revision	
A4	UCT-MST-A006	v1/A	
Date:	7/9/2015	Sheet 1 of 1	
File:	C:\Users\... \First_Amp_SchDoc	Drawn By:	Dayne Kemp



1.8V, 1A Switch Mode Regulation (2.2 to 6V input, 600mA Output)

2.5V, 1A Analog Linear Regulation (2.2 - 5.5V input, 100mA output)

2.5V, 1A Digital Linear Regulation (2.2 - 5.5V input, 100mA output + FPGA IO)

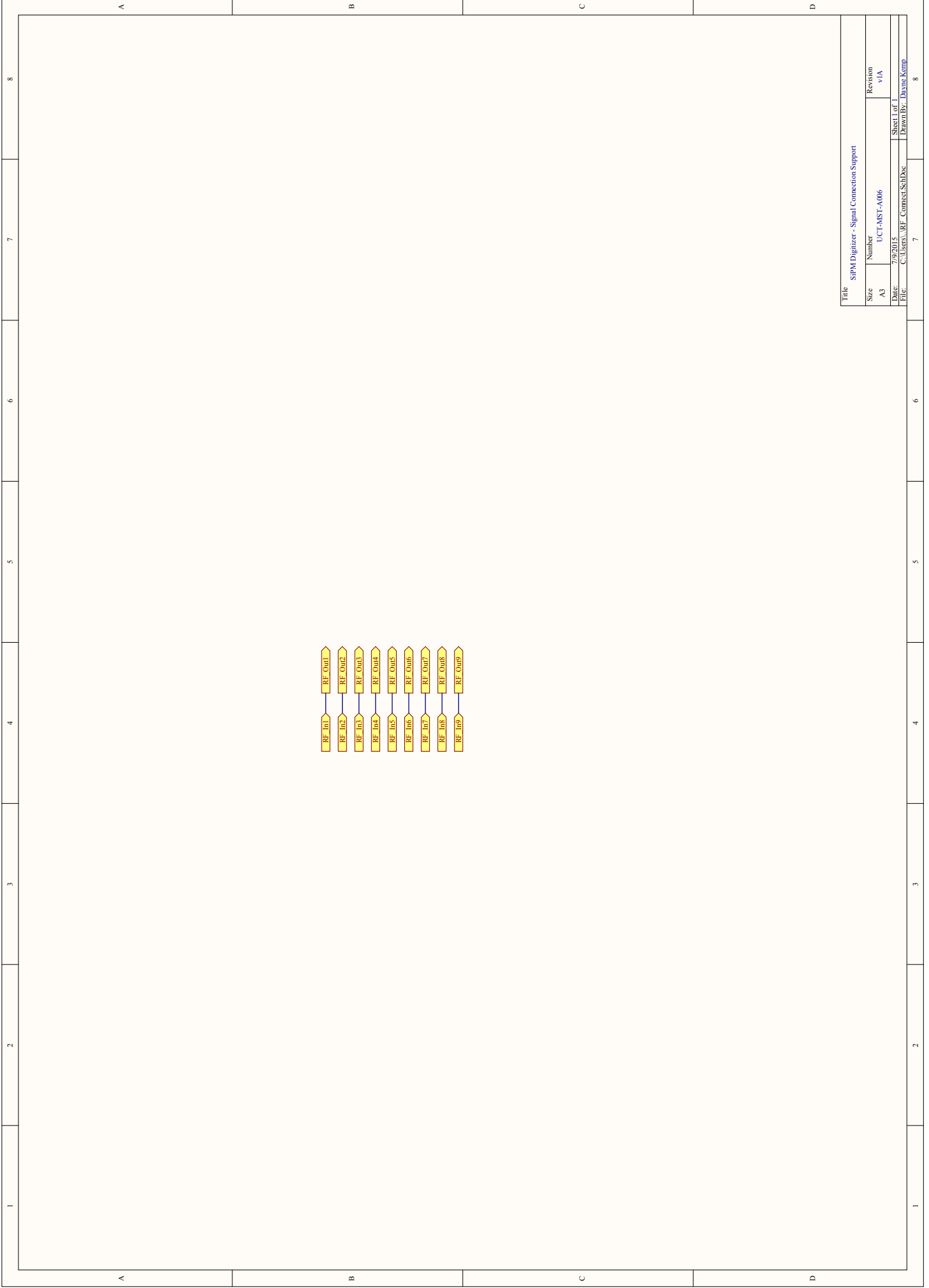
3.3V, 4A Switch Mode Regulator (4-15V input, 2A output/Input reverse polarity protection)

5V, 12A Switch Mode Regulator (4-15V input, 8A for FPGA, 4A for PCB + all other)

Cap voltage on input, TVS diode

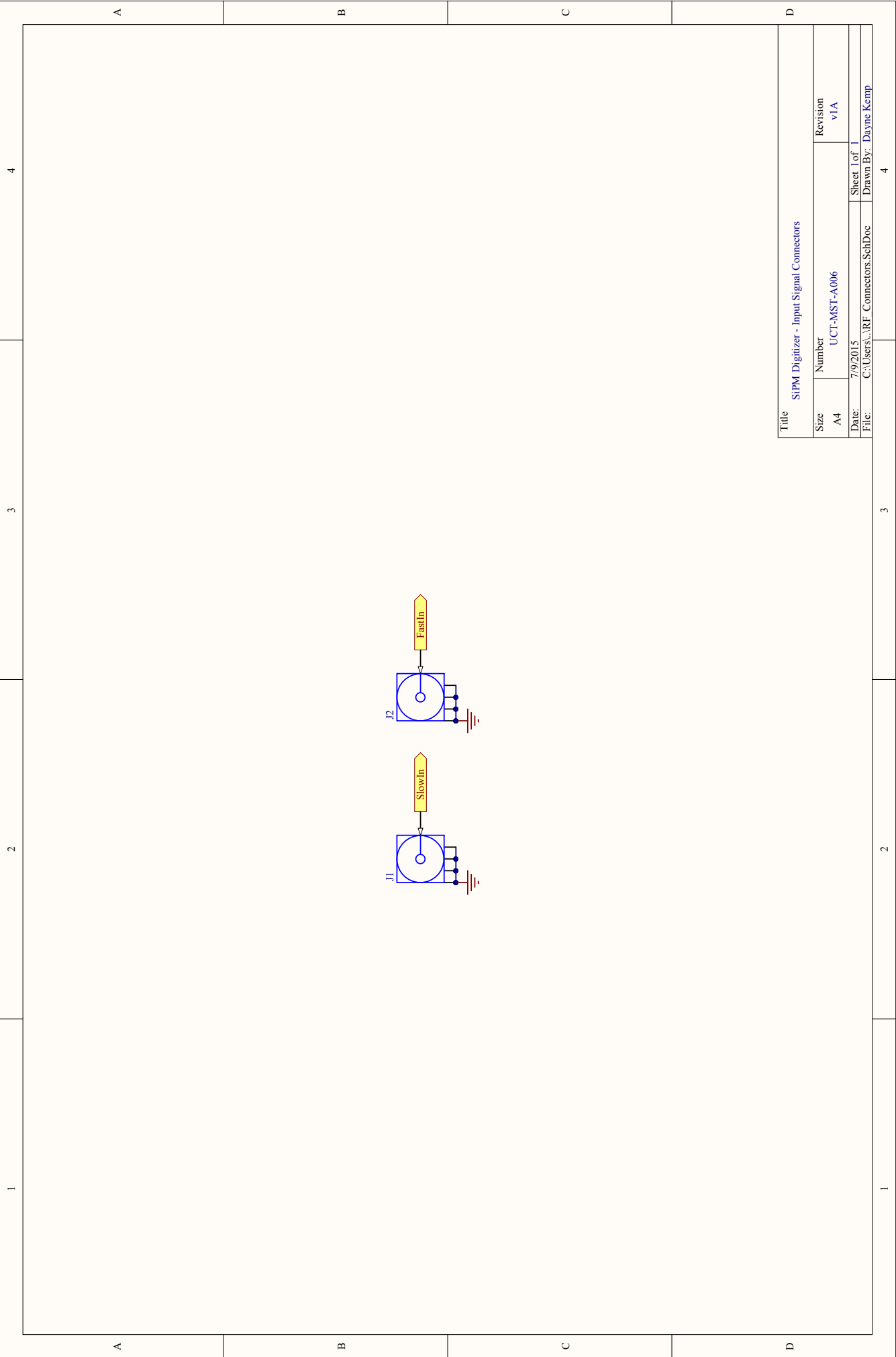
Selecting bank voltage for FPGA

Title		SIPM Digitizer - Power Supplies	
Size	Number	Revision	v1A
A3	UCT-MST-A006	Date:	7/9/2015
File:	C:\Users\...Power_Supplies\SchDoc	Sheet 1 of	8
Drawn By:		Davone Kemp	



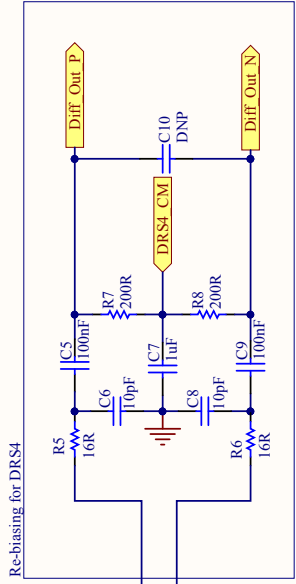
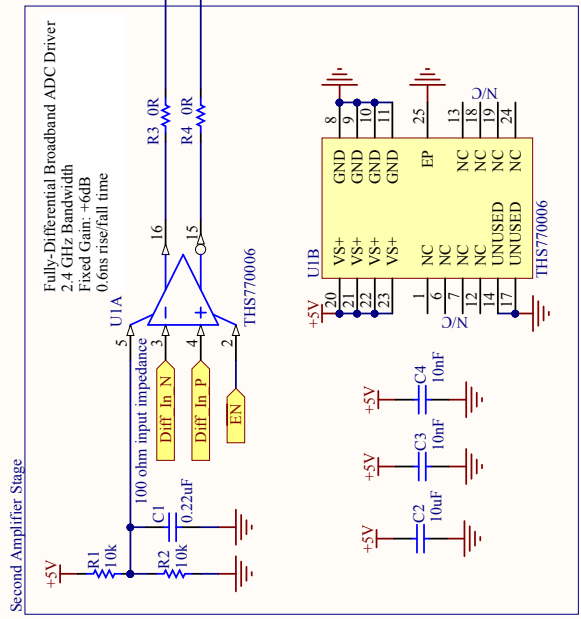
Title: SPM Digitizer - Signal Connection Support

Size	Number	Revision
A3	UCT-MST-A006	VIA
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\...RF_Connect\SchDoc	Drawn By: Dayne Kemp

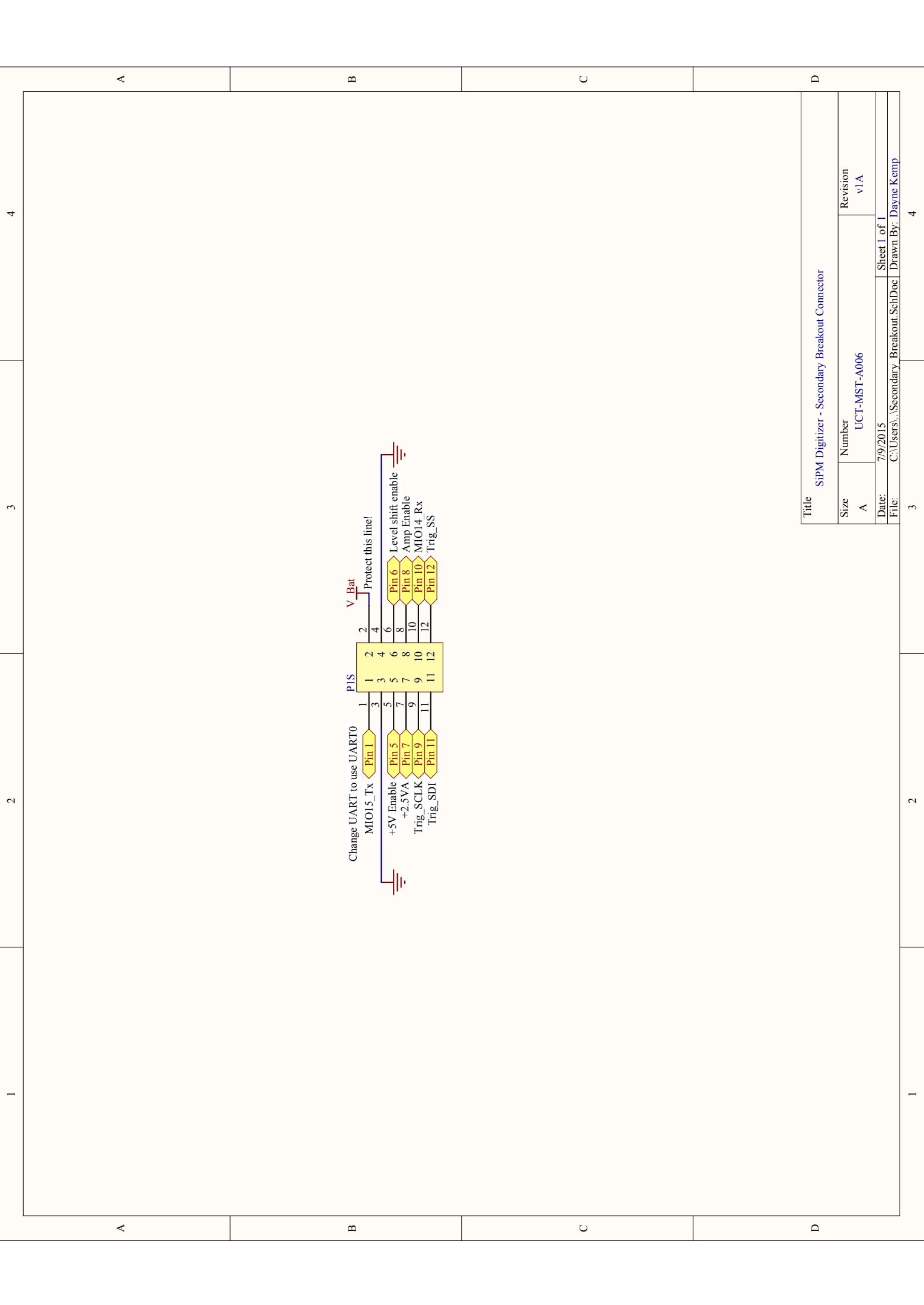


Title: SIPM Digitizer - Input Signal Connectors

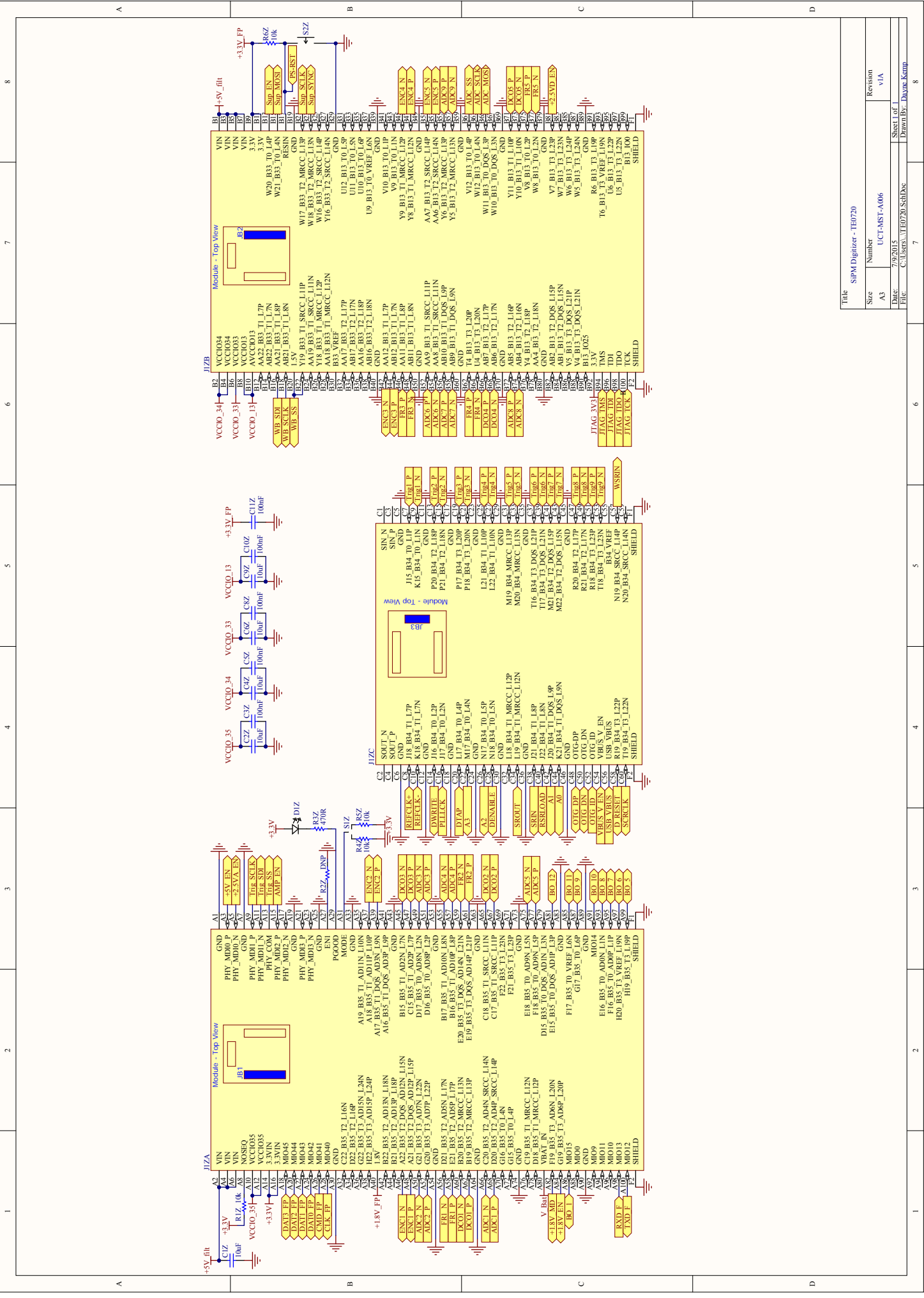
Size	Number	Revision
A4	UCT-MST-A006	V1A
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\...RF - Connectors.SchDoc	Drawn By: Dayne Kemp



Title	
SIFM Digitizer - Second Stage Amplifier (Fixed Gain)	
Size	Revision
A4	V1A
Date:	7/9/2015
File:	C:\Users\...Second_Amp_SchDoc
Sheet 1 of 1	
Drawn By: Dayne Kemp	



Title		SiPM Digitizer - Secondary Breakout Connector	
Size	Number	Revision	
A	UCT-MST-A006	v1A	
Date:	7/9/2015	Sheet 1 of 1	
File:	C:\Users\...\Secondary Breakout.SchDoc   Drawn By: Dayne Kemp		



Title SIPM Digitizer - TE0720

Size	Number	Revision
A3	UCT-MST-A006	VIA
Date:	7/9/2015	Sheet 1 of
File:	C:\Users\TE0720\ShellDoc	Drawn By:
		DAVINE KOMP

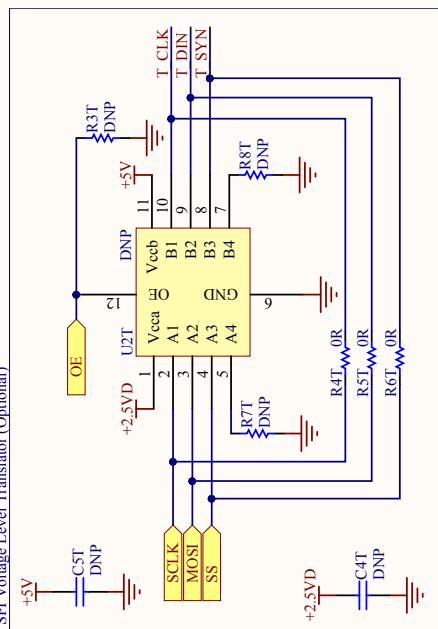
A

B

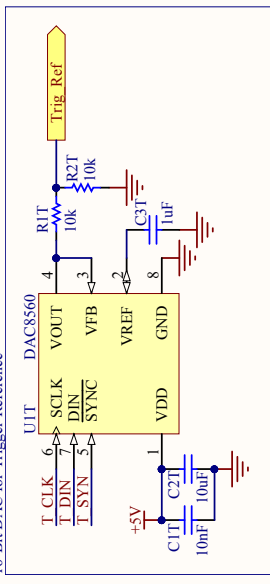
C

D

SPI Voltage Level Translator (Optional)



16-Bit DAC for Trigger Reference



Title: SJPM Digitizer - Trigger Reference and Support

Size: A4  
 Number: UCT-MST-A006  
 Revision: v1A

Date: 7/9/2015  
 File: C:\Users\... \Trig\_RefSchDoc

Sheet 1 of 1  
 Drawn By: Dayne Kemp

A

B

C

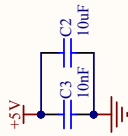
D

A

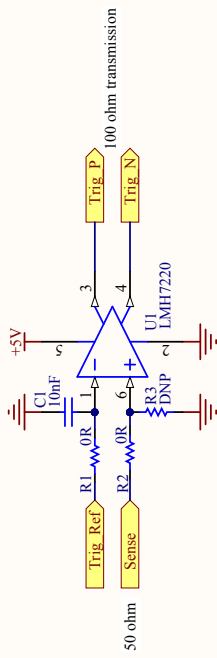
B

C

D



High-Speed Comparator  
 LVDS Output  
 6.8mA @ 5V  
 0.6ns rise/fall time



Title: SIFPM Digitizer - Trigger

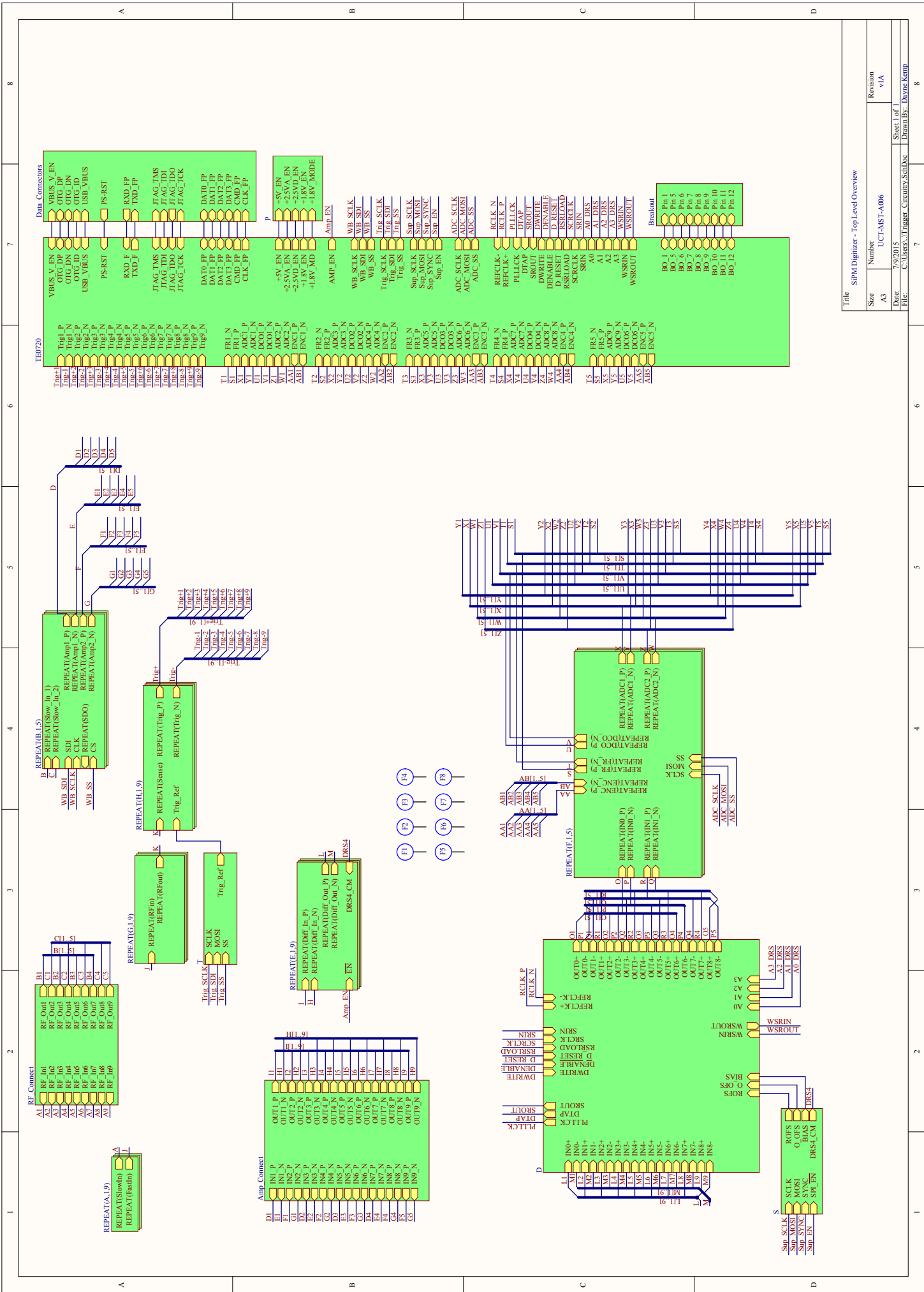
Size	Number	Revision
A4	UCT-MST-A006	V1A
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\... \Trigger_SchDoc	Drawn By: Dayne Kemp

A

B

C

D



Title: SIPM Digitizer - Top Level Overview

Size	Number	Revision
A3	UCT-MST-A006	v1A
Date:	7/9/2015	Sheet 1 of 1
File:	C:\Users\j.trigler\Circuitry\SIPM	Drawn By: Davyne Kemp

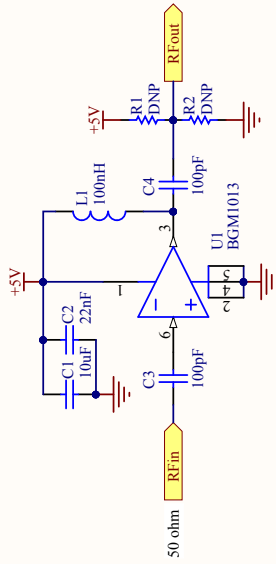
A

B

C

D

35.5dB @ 1 GHz  
 Corner freq: 2.1 GHz  
 40dB isolation  
 28mA DC supply current



Title: SIFM Digitizer - Wideband Amplifier

Size: A4  
 Number: UCT-MST-A006  
 Revision: v1A

Date: 7/9/2015  
 File: C:\Users\...Wideband\_Amp\_SchDoc  
 Sheet 1 of 1  
 Drawn By: Dayne Kemp

A

B

C

D

## EBE Faculty: Assessment of Ethics in Research Projects

Any person planning to undertake research in the Faculty of Engineering and the Built Environment at the University of Cape Town is required to complete this form before collecting or analysing data. When completed it should be submitted to the supervisor (where applicable) and from there to the Head of Department. If any of the questions below have been answered YES, and the applicant is NOT a fourth year student, the Head should forward this form for approval by the Faculty EIR committee: submit to Ms Zakiya Chikte ([Zakiya.chikte@uct.ac.za](mailto:Zakiya.chikte@uct.ac.za)); New EBE Building, Ph 021 650 5739). Students must include a copy of the completed form with the dissertation/thesis when it is submitted for examination.

Name of Principal Researcher/Student: Dayne Kemp

Department: Electrical Engineering

If a Student: Yes

Degree: MSc.Eng Electrical

Supervisor: Samuel Ginsberg

If a Research Contract indicate source of funding/sponsorship:

Research Project Title:

A Compact High-Energy Particle Detector for Low-Cost Deep Space Missions

### Overview of ethics issues in your research project:


<b>Question 1: Is there a possibility that your research could cause harm to a third party (i.e. a person not involved in your project)?</b>		NO
<b>Question 2: Is your research making use of human subjects as sources of data?</b> If your answer is YES, please complete Addendum 2.		NO
<b>Question 3: Does your research involve the participation of or provision of services to communities?</b> If your answer is YES, please complete Addendum 3.		NO
<b>Question 4: If your research is sponsored, is there any potential for conflicts of interest?</b> If your answer is YES, please complete Addendum 4.		NO

If you have answered YES to any of the above questions, please append a copy of your research proposal, as well as any interview schedules or questionnaires (Addendum 1) and please complete further addenda as appropriate.

### I hereby undertake to carry out my research in such a way that

- there is no apparent legal objection to the nature or the method of research; and
- the research will not compromise staff or students or the other responsibilities of the University;
- the stated objective will be achieved, and the findings will have a high degree of validity;
- limitations and alternative interpretations will be considered;
- the findings could be subject to peer review and publicly available; and
- I will comply with the conventions of copyright and avoid any practice that would constitute plagiarism.

Signed by:

	Full name and signature	Date
Principal Researcher/Student:		31/08/2015

This application is approved by:

Supervisor (if applicable):		31/08/2015
HOD (or delegated nominee): Final authority for all assessments with NO to all questions and for all undergraduate research.		31/08/2015
Chair : Faculty EIR Committee For applicants other than undergraduate students who have answered YES to any of the above questions.		