White RHINO: A Low-Cost Communications Radar Hardware Platform

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Declaration

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

Signature of Author .....

Cape Town
1 December 1999

Abstract

The Electromagnetic spectrum has always been a very expensive resource and hence, has not been accessible to everyone. Yet, it is under-utilized. The new Whitespace Technology standards provide an efficient way to use the spectrum. However, the concept of shared spectrum introduced by the Whitespace Technology promises to reduce the cost of accessing the spectrum by a huge margin. Also, because the standards utilize the television channels, the VHF and UHF frequencies facilitate wireless transmission over large distances. This has provided impetus to various application developers. Using Whitespace Technology for Communications Radar is one such novel application which has great benefits for the African scenario. Here, the population is scattered and infrastructure for navigation and tracking is inadequate. But, there is a shortage of low-cost commercially available hardware platforms tailored for the application.

In order to boost Whitespace-based Communications Radar application development, the White RHINO(Reconfigurable Hardware Interface for computatioN and radiO) hardware platform was developed. It aims to fill the gap of low-cost commercial hardware platforms available for Whitespace-based Communications Radar.

Being a Communications Radar platform, the White RHINO had to be designed keeping the standards and regulating body norms as yardsticks. However, an achievable radar performance of the platform under various scenarios was also estimated. The White RHINO contains an FPGA(the Zynq7000 series) which has dual embedded ARM processing cores. For the wireless interface, it contains a field programmable RF transceiver and an RF frontend section. The platform contains wired networking capability of 2 Gbps. The platform also has 512 MB DDR3 and 128 Mbit NAND flash as onboard memory. Finally, it has USB host, SDIO and JTAG for programmability and temperature sensors for system monitoring.

The manufactured boards were tested under lab environment. It was found that except a failure on the RF transceiver section(due to a PCB footprint error), other interfaces were functional. The White RHINO successfully runs both U-Boot and Linux as operating systems. The error and other minor bugs have been corrected for the next fabrication run.

Also, the cost of the complete White RHINO system is less than 1000 USD which makes it a very powerful platform and yet, less expensive than most of the commercially available platforms designed for similar applications.

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Nomenclature

VHF—Very High Frequency.

UHF—Ultra High Frequency.

dB—Decibels.

P1dB—1 dB compression point.

JTAG—Joint Test Action Group.

USB—Universal Serial Bus.

DDR—Dual Data rate.

SDIO—Secure Digital Input Output.

WRAN—Wireless Regional Area Networks.

TVBD—Television Band Device.

EIRP—Equivalent Isotropically Radiated Power.

ACPR—Adjacent Channel Power Ratio.

PSD—Power Spectral Density.

MAC—Medium Access Control.

TDD—Time Division Duplex.

FDD—Frequency Division Duplex.

UART—Universal Asynchronous Receiver Transmitter.

RGMII—Reduced Gigabit Medium Independent Interface.

PLL—Phase Locked Loop.

Beamwidth—The angular width of a slice through the mainlobe of the radiation pattern of an antenna in the horizontal, vertical or other plane.

Doppler frequency—A shift in the radio frequency of the return from a target or other object as a result of the object's radial motion relative to the radar.

Range—The radial distance from a radar to a target.

Chapter 1

White RHINO

1.1 Introduction to Whitespace Technology

The Electromagnetic Spectrum, being a very expensive resource, has always remained accessible only to the top corporations. Just to provide you with a vague picture, let us consider the following examples. In 2013, the Hutchison bought two 5 megahertz(MHz) 3G channels of the 800 MHz band at a whopping cost of 261 million Euros [1]. In 2010, in India, the 3G spectrum auctions generated revenue of 12 billion US Dollars(USD) [2]. But, is the spectrum efficiently utilized? The answer to this question turns out to be a no. A recent survey done in Southern Africa shows wide spaces of under-utilized spectrum in the rural as well as urban regions [3]. So, in that case, are the towering prices of the spectrum justified? This too, turns out to be a glaring no. Such discrepancies, however, have not gone unnoticed. The international research communities backed by corporations have been working for almost a decade to optimize the usage of the spectrum.

As we now know, there is a lot of un-used or under-utilized spectrum. These are called Whitespaces. The transition from Analogue to Digital TV also witnessed a major creation of whitespaces spanning over hundreds of megahertz. The obvious reason being that Digital TV(DTV) uses advanced modulation and coding techniques which its analog counterpart cannot implement. And thus, using lesser bandwidth to transmit more information leading to better picture quality than ever before. These whitespaces are popularly known as TV whitespaces. Even before the transition began, research groups around the world observed the potential of the TV whitespaces. The concept of shared spectrum was envisaged

which would in turn optimize the usage of the spectrum, thereby bringing down the costs. The initial stages of this development saw research being focused more towards finding answers to the fundamental problems posed by the concept of shared spectrum [4–6]. Many such pioneering works laid the foundations for what we now know as Whitespace Technology.

In 2007, the first prototype tests were carried out by a consortium of corporations led by Microsoft, Motorola and Phillips called the Whitespace coalition. These tests confirmed that many devices can coexist while using the spectrum in a shared basis without interfering with the DTV signals. As a result of the successful tests, USA became the first country in the world to open up the TV Whitepace spectrum for unlicensed use. More tests followed. One of the largest commercial tests were carried out in Cambridge, UK, in 2011. These test involed live high-definition(HD) video streaming under a highly challenging radio propagation environment with signal degradation of over 120 decibels(dB) through buildings, foliage, walls, people etc. and with severe multipath effects [7]. In the meantime, Institute of Electrical and Electronics Engineers(IEEE) developed a framework for the reliable operation of Whitespace devices. This specification, the Wireless Regional Area Networks(WRAN) IEEE 802.22, was released in 2011 [8]. Another Whitespace specification, called the Wireless Local Area Networks(WLAN) IEEE 802.11af shall be released in 2014 [9].

To summarize, now we have,

- A standardized specification for Whitespace Communications, the WRAN IEEE 802.22 tailored specifically for devices operating in the TV whitespaces.
- More and more countries around the world gradually opening up the spectrum for unlicensed use.

Hence, this greatly accessible spectrum promises to attract Innovators who shall use this new engineering playground for Novel applications.

1.2 Networked Whitespace Radar: Novelty and Challenges

A United Nations, World Bank report on Africa's Transport Infrastructure points out how the Air Traffic Control(ATC) and Navigation in Africa is Inadequate

and Poorly Financed. Firstly, ground based navigation installations are sparse. Many of the existing equipment have become too expensive even to maintain and hence, cannot be used. Many ATC installations do not use radar separation. Radar separation is used to issue direction and headings to aircrafts based on radar images. Adding to that, many airports switch to radar procedures only if the weather conditions demand, [10].

The traditional radar systems are very expensive and huge infrastructure cost is involved. But, if the radar functionality could become a commensal function of the wireless communication networks, then, there could be a huge cut down of the expenditure on separate radar infrastructure. Study of radars which rely on TV or FM boradcast signals has picked up pace in recent years because they do not contribute to further infrastructure cost apart from being useful in millitrary surveillance scenarios [11–15]. As it has been observed, successful radar detection can be done using such illuminators, which are popularly known as illuminators of opportunity. On the other hand, due to high propagation losses and low power of standard communication signals which operate at frequencies close to 1 GHz or above, radar ranges achieved were too low for any practical purpose. However, wireless communication networks based on TV whitespace signals can overcome that limination of range because of lower propagation losses of TV signals which are in the range of 50 to 700 MHz. Another advantage is the fact that, wider bandwidths are available at disposal which will mean better range resolution for the radar system [16].

Hence, such a system which can operate as a communication node as well as facilitate the radar functionality is feasible. However, it's implementation which spans across radio frequency hardware, digital hardware to software algorithms is a non-trivial design problem with various interdependencies. Adding to that, the tight Whitespace Emmision rules are almost contradictory to the requirements of a good radar system which will put limitations on the detection capability and hence, will decide the geographical spacing of the communciation nodes.

Existing hardware platforms available for sofware defined radio(SDR) which could be used for testing out such a system are very expensive and not tailored for the current problem. Among the popular ones, the USRP N210 [17] costs around 1800 USD without the RF front-end which willl be required to boost the signal to the required power levels.

And so, we deduce that for rapid development of a Networked Whitespace Radar system, a more accessible (cost-wise) and a tailored open-source hardware platform is needed.

1.3 The White RHINO Hardware Platform

In order to bridge the above mentioned gap, the endeavour to develop Whitespace Reconfigurable Hardware Interface for ComputatioN and RadiO(White RHINO) was conceived. The White RHINO intends to provide researchers from academia and industry the equipment on which the complex algorithms required for a Networked Whitespace Radar can be successfully implementated.

Dr Alan Langman, a researcher affiliated with the University of Cape Town, who also contributed for a provisional patent "Whitespace based Commensal Radar" envisaged the project [18]. The system outline that he provided shall be the User Requirements. They have been stated as follows:

1. The primary System on Chips (SoCs) to be used should be Xilinx Zynq7000 and Lime Micro LMS6002D.
2. The Processing System Architecture should be similar to the Digilent Zedboard [19].
3. The board should be able to boot the operating system using flash memory as well as SD card.
4. The board should have two 1000 Base-T Ethernet connections.
5. The board should be capable of being powered by external 12V battery or AC-DC adapter as well as by Power over Ethernet (PoE).
6. The final per unit cost should be less than or equal to 800 USD.

1.4 Analysis of Requirements

With the outline of the White RHINO system defined, now it is our task to find out if the outlined hardware shall be sufficient for the functionalities that we want to implement. The board should be able to able to perform the following functions:

1. Implement the WRAN IEEE 802.22 for wireless communications.
2. Detect airborne or surface based targets while operating commensally under the restrictions imposed by the TV Whitespace regulations.

In order to make sure that the system outline mentioned in the user requirements is sufficient to obtain the functional requirements out of the system, a feasibility study was performed. The details of the study can be found in Appendix A. This study was performed on the two most critical devices mentioned in the first point of the user requirements. Firstly, it was found that the Xilinx Zynq7000 has sufficient resources to implement major physical layer blocks leaving out ample resources for other functional blocks. Secondly, it was found that the Lime Micro LMS6002D RF transceiver meets the RF performance requirements except the output power. Hence, both the critical devices can be used for the design. The Whitespace communication requirements and constraints shall be further discussed in chapter 2. And, finally under the given constraints, an estimation of radar capability was performed which shall be discussed in chapter 3. Together, the two main functional requirements expected from the system shall be achieved. Even though White RHINO hardware requirements shall be studied in reasonable detail in the coming chapters but they have been summarized in Tables 1.1 to 1.4 for the sake of completeness of this section and also, for the ease of tracking. A mindmap of the White RHINO hardware requirements is also presented in Figure 1.1.

Table. 1.1: Requirements: Computational

S.No	Requirement	Description
1	Programmable Logic	Resources present in Zynq7000's programmable logic
2	Processing System	Dual-Core ARM^{TM} Cortex A-9 processors with Single-Precision Floating Point NEON^{TM} Media Processing Engines(MPEs)
3	Memory	512 MB DDR3 SDRAM

Table. 1.2: Requirements: Performance

S.No	Requirement	Description
1	Transmit Power	30 dBm or 1 Watt
2	Bandwidth of Operation	512 MHz to 698 MHz
3	Instantaneous Bandwidth	A minimum of 6 MHz
4	Networking	2 X 1 Gbps Ethernet
5	Power Consumption	Less than 25 Watts

Table. 1.3: Requirements: External Interfaces

S.No	Requirement	Description
1	Power Supply	12 Volt External supply(AC-DC Adapter or Baterry powered) and Power Over Ethernet(PoE)
2	Network Ports	2 X 1000 Base-T (Copper)
3	User Interfaces	Universal Serial Bus(USB) and Joint Test Action Group(JTAG) Interfaces
4	Air Interfaces	TV Whitespace and Global Positioning System(GPS) Antenna ports

Table. 1.4: Requirements: Other

S.No	Requirement	Description
1	Enclosure size	17cm x 17cm x 5 cm
2	Cost	Less than 1000 USD

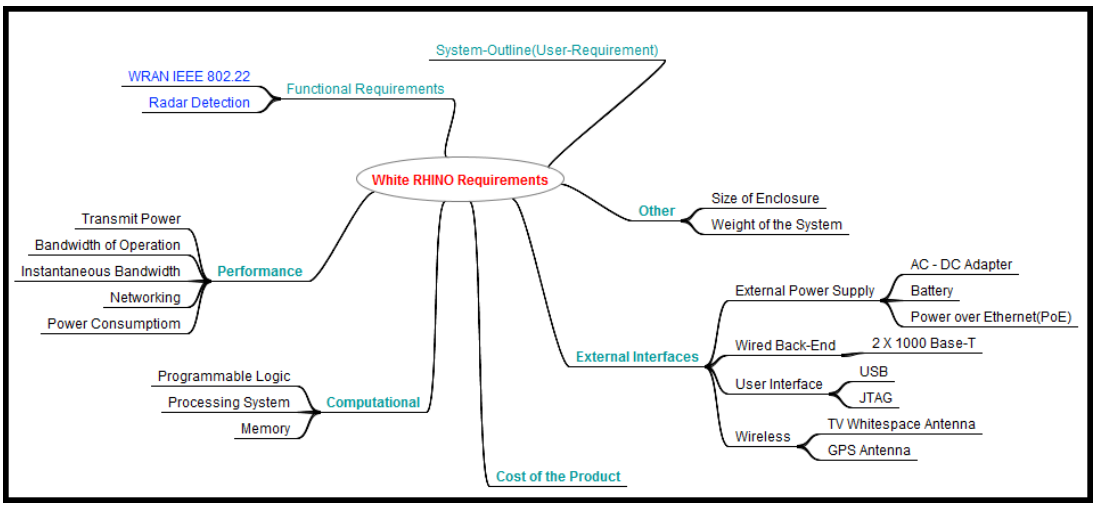

Figure. 1.1: Mindmap: White RHINO Requirements

1.5 Scope of the Dissertation

The Design, Development and Hardware Validation of the White RHINO Communications Radar platform for Whitespace Technology is the defined scope of the thesis.

This thesis does not discuss Functional Verification of the board.

However, the capability of the board shall be inferred from the derived Hardare Requirements that it aims to qualify through the Hardware Validation Process.

1.6 Document Outline

In this chapter, we have only mentioned the Requirements for the White RHINO board. Deriving these requirements needed a more detailed study. So, before we actually go into the hardware design aspects, the requirements shall be extracted or derived(when required). To do that, a study of the Spectrum Regulations and the only existing wireless standard for Whitespace Technology, the WRAN IEEE 802.22 [20] have been presented in Chapter 2. The Spectrum Regulations have been taken from the Second Memorandom and Opinion Order provided by Federal Communications Commission(FCC) which opened up the Whitespace spectrum for Unlicensed use in the USA [21]. In the final section, the key hardware design parameters are discussed.

After reviewing the standards, a study of Radar Detection capability has been done in Chapter 3. Starting of with basic simulations to assess the feasibility of such a radar, we go for a more rigorous and realistic approximation. The CARPET tool has been used to perform the simulations. These simulations have been performed under the restrictions imposed by the standards. Some of the included parameters coming from standards are Transmit Power, Bandwidth, Antenna height and so on. Finally, the results of those simulations have been noted.

In Chapter 4, a study of various Hardware Architectures is done. Except the USRP N210 [17], which is used as a yardstick for evaluating the current state of Network Hardware, the other Architectures have been studied to obtain a better understanding of the design aspects related to the SoCs that have been defined in the user requirement. These are the Zedboard , the NUTAQ Radio420X board, the TOYON Chillipepper board and the NUAND Blade RF board. In the final section, the remaining hardware requirements are discussed which do not emerge from the standards in an obvious way but board design aspects have to be considered as well [19, 22–24].

After the prelimiary study of requirements and various hardware architectures, the White RHINO Hardware Architecture is defined in Chapter 5. The Architecture is first presented in the form of a block diagram and then, the various

blocks have been explained. The architecture has been decided upon by keeping the important aspect of testability in view. This is followed by a discussion on the selection of the devices. This discussion focusses on the various trade-offs that were considered before zeroing in on a particular device. Also, a design decision was made to split the design into two boards, one with the digital and low power RF sections and the other with the higher power RF front-end section.

With the Architecture completed and major devices selected, we move on to the schematic design for the project in chapter 6. Rest of the components were selected during this phase of the project. The RF schematics were drawn after verifying them through Genesys Simulations. These simulations have been done with the S-Parameter files that have been obtained from the manufacturers as well as realistic lumped and distributed elements available from its libraries. Simulation results are also presented in one of the sections. This chapter also discusses many design decisions that were made to optimize cost without losing out much on performance and testability.

In Chapter 7, the White RHINO Printed Circuit Board(PCB) design is described. It includes design decisions taken to finalize the PCB stackup, component placement, trace impedance, trace thicknesses, routing topologies, split planes and so on. Many of these decisions were taken keeping view of factors like board fabrication cost, thermal performance, electromagnetic interference(EMI), timing issues and signal integrity. This chapter also provides simualtion plots of DDR3 signal integrity simulations at various desired clock rates. Also, some of the post-fabrication and assembly RF optimization related provisions kept on the White RHINO RF front-end board are discussed as well. This chapter winds up with a short note on the generation of manufacturing files.

The whole of Chapter 8 deals with post assembly Hardware Validation. This process starts of with visual board inspection, some passive tests, board bring up by checking if all the power supplies and clocks are working as desired. Then, both the boards, the White RHINO core and White RHINO RF are tested if they meet the performance parameters. This leads to the identification of hardware bugs and suggested fixes to be implemented in the next version. Finally, the results of this design verification process are noted and discussed.

Finally, the design summary, conclusions and future work for the White RHINO hardware platform are discussed in Chapter 9. The note on whether the platform meets the requirements, user as well as functional, are discussed in this chapter. The future work section discusses some hardware updates (or fixes) or upgrades.

Apart from the main chapters, there are two appendices as well. In Appendix A, the feasibility calculations for the Xilinx Zynq7000 deivce is presented. Appendix B lists the names of all the files included in the attached CD.

Chapter 2

Whitespace Communications and Hardware Requirements-I

2.1 Whitespace Regulations(FCC)

In this section, we shall discuss the regulatory constraints for the operation of a White Space Device. The regulatory norms have been directly extracted from FCC orders, [21, 25]. Most of the specifications have direct implications on the hardware design. Before we look at the specifications, let us introduce some terminologies defined by FCC:

- Television band device (TVBD):
  Intentional radiators operating on Available Channels in the broadcast television frequency bands at 54-60 MHz, 76-88 MHz, 174-216 MHz, 470-608 MHz and 614-698 MHz
- Modes of Operation:
  Mode I - client, whereby a personal/portable device is controlled by a fixed or a personal/portable device operating in Mode II that has determined the available channels in the area and/or,
  Mode II - independent, whereby a personal/portable device determines the available channels using its own internal geo-location/database access capabilities

As it can be observed, there are four classes of devices as shown in Table 2.1

Table. 2.1: Device Classes

A. Mode-I, Fixed	B. Mode-II, Fixed
C. Mode-I, Personal/Portable	D. Mode-II, Personal/Portable

2.1.1 Frequencies of Operation

The frequency bands which have been made open to the unlicensed users are part of the Very High Frequency(VHF) and the Ultra High Frequency(UHF) bands which are used for TV signal transmission. These bands are scattered from 54 MHz to 698 MHz. All the bands have been shown in Table 2.2. All of these bands are split into channels having bandwidths of 6 MHz. However, not all the channels can be used by all the classes of devices mentioned in Table 2.1.

Table. 2.2: Frequencies of Operation: Each of these channels have a bandwidth of 6 MHz. In total, there are 47 available channels of operation

Device Type	Frequency Bands(MHz)
All TVBDs	512-608 614-698
Only for Communication Between Fixed TVBDs	54-60 76-88 174-216 470-512

2.1.2 Antenna Specifications

The Antenna Height of the TVBDs have been defined under two specifications. First, is the height above ground and then, height above average terrain(HAAT) of the transmitting antenna, Table 2.3.

Table. 2.3: Antenna Specifications

Antenna Type	Max Antenna Height Above Ground (Metres)	Absolute Maximum Height above Average Terrain, HAAT (Metres)
Fixed	30	250

2.1.3 Transmit Power

The various classes of devices have different transmit power limits due to possible interference to the TV subscribers. So, the personal/portable devices have to operate at a lower power than the fixed devices. There is also an absolute maximum to the equivalent isotropically radiated power(EIRP) so that, the TVBDs cannot use extremely directive antennas at the specified maximum conducted power which again could lead to interference. These have been summarized in Table 2.4

Table. 2.4: In-Band Power: These specifications define the maximum limits of In-Band power levels and spectral densities radiated by the different classes of TVBDs.

Device Type	Typical Conducted Power Output (dBm)	Typical Antenna Gain (dBi)	Absolute Maximum EIRP (dBm)	Max Power Spectral Density, PSD (in 100 KHz Band) (in dBm EIRP)	Power Control
Fixed-Devices	30	6	36	12.6	Required
Personal/portable device(operating @ Adjacent channel to TV channels)	20	0	20	-1.4	Required
Sensing-only devices	-	-	-	-0.4	-
All other personal/portable devices	20	0	20	2.6	Required

2.1.4 Adjacent Channel Power

Adjacent channel power is one of the most important of the emission specifications. These regulations make sure that the devices do not spill unnecessary

radiation due to insufficient roll-off of transmit filters. Again, these requirements vary for the various classes of TVBDs, Table 2.5.

Table. 2.5: Adjacent Channel Power: These specifications define the maximum limits of Adajacent Channel Emmisions radiated by the different classes of TVBDs

Device Type	Absolute Maximum Emissions, EIRP(dBm)	Minimum Measurement RBW(KHz), Detector Type
Fixed-Devices	-42.8	100, Average
Personal/portable device(operating @ Adjacent channel to TV channels)	-56.8	100, Average
Sensing-only devices	-55.8	100, Average
All other personal/portable devices	-52.8	100, Average

2.1.5 Interference Avoidance Mechanisms

FCC has suggested two Interference Avoidance Mechanisms for the Unlicensed subscribers, so that the TV channels do not become susceptible to the interference from the TVBDs. Each of these mechanisms of operation contain a set of specifications. These mechanisms are "Geo-Location and Database Access" and "Spectrum Sensing".

1. Geo-Location and Database Access, The TVBDs using this kind of Interference Avoidance mechanism have to know or find out its own geographical location and then, through a wired or a wireless link, they have to access the database for the currently available channels of operation and transmit accordingly. In Tables 2.6 and 2.7, the Information Update specifications are defined.

2. Spectrum Sensing, The TVBDs using this kind of Interference Avoidance Mechanism have to sense the spectrum to find out the channels, available or empty and hence, apt for transmission. This kind of mechanism has to use cognitive sensing techniques which will be discussed in the next

section when we discuss the WRAN architecture. In Tables 2.8 and 2.9, the Spectrum Sensing specifications are provided.

Table. 2.6: Interference Avoidance, Geolocation and Database Update: Geo-Location Update specifications

Device Type	Geo-Location Accuracy(Metres)	Location Update Time(Secs)	Location Update Procedure
Fixed-Devices (Mode II)	[-50,+50]	N/A	Manual(During Installation)/Automated Geo-Location Capability of the Device
Personal/Portable Mode II Devices	[-50,+50]	Not specified(But required every time the device is powered ON)	Automated Geo-Location Capability of the Device
Mode II Devices	N/A	N/A	N/A

Table. 2.7: Interference Avoidance, Geolocation and Database Update: Database Update specification

Device Type	Available Channels Update time	Remark
Fixed-Devices (Mode II)	Atleast Once a Day	Update required when powered ON
Personal/Portable Mode II Devices	Atleast Once a Day	Update required when powered ON
Mode II Devices	Every 60 seconds	It has to get update from a Mode II device

2.1.6 Interference Protection Mechanism

The FCC has also defined some Interference Protection Mechanisms as well. These define the physical separation of the TVBD's with different antenna heights with the licensed subscribers occupying the same or the adjacent channels, in Figure 2.1.

Table. 2.8: Interference Avoidance, Spectrum Sensing: Sensitivity specifications

Signal Type	Sensitivity-Threshold (dBm)	Integration Bandwidth	Detetctor Type
ATSC, digital TV	-114	6 MHz	Average
NTSC, analog TV	-114	200 kHz	Average
Wireless Microphone	-114	100 kHz	Average

Table. 2.9: Interference Avoidance, Spectrum Sensing: Update specifications

Specification Type	Min Time (secs)	Max Time (secs)
TV channel availability check time (Duration of check)	30	-
In-service monitoring (Repetition time)	30	-
Channel move time (Time to leave the occupied channel)	-	2

Antenna height above average terrain of unlicensed device	Required separation (km) from digital or analog TV (full service or low power) protected contour	
	Co-channel (km)	Adjacent channel (km)
Less than 3 meters	4.0	0.4
3-Less than 10 meters	7.3	0.7
10-Less than 30 meters	11.1	1.2
30-Less than 50 meters	14.3	1.8
50-Less than 75 meters	18.0	2.0
75-Less than 100 meters	21.1	2.1
100-Less than 150 meters	25.3	2.2
150-Less than 200 meters	28.5	2.3
200-250 meters	31.2	2.4

Figure. 2.1: Interference Protection Mechanism: The plot shows the specifications for the physical separation of Antennas. Please note that, operation of fixed and personal/portable TVBDs is prohibited on all channels within 2.4 kilometres of the Radio Astronomy Sites

2.2 Wireless Regional Area Networks(WRAN) IEEE 802.22

As previously stated, the IEEE built the framework under which Whitespace devices can successfully operate. This specification which defines all the network layers is the WRAN IEEE 802.22. However, here we will only look at the physical layer(PHY) in detail and some medium access control(MAC) layer features. The obvious reason is that, it's the physical layer which defines most of the hardware specifications. [20]

The pictorial representation of the Cognitive WRAN Architecture is shown in Figure 2.2, the protocol reference model(PRM). Here, the architecture is partitioned into three logical planes, namely, the Data plane, the Control and Management plane and the Cognitive plane. The functionality of the Cognititve plane is to constantly monitor the White-Spaces, and pass-on the information to the other planes so that, the device can operate smoothly without causing interference to the TV subscribers.

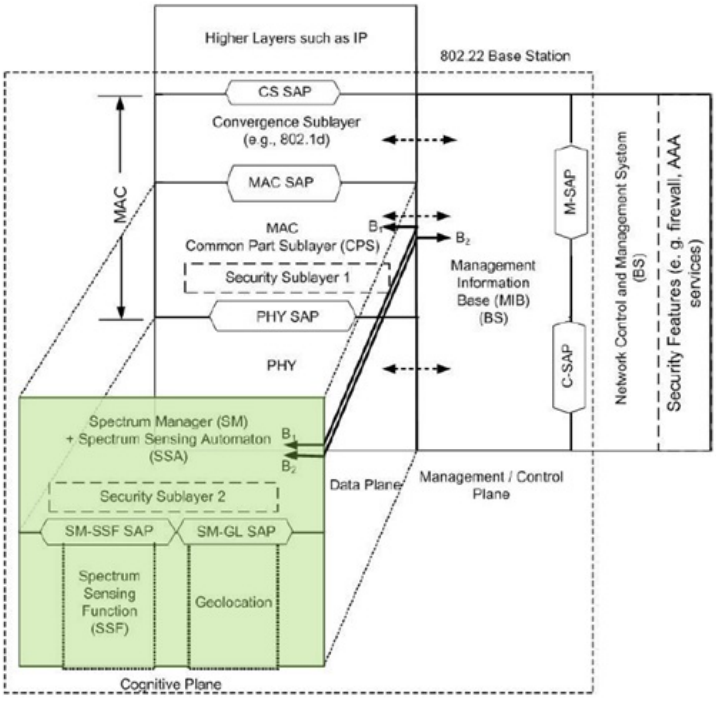

Figure. 2.2: Protocol Reference Model(WRAN IEEE 802.22)

2.2.1 Data Plane

The data plane is formed by three stacked layers. They are the PHY, the MAC and the Convergence sublayer(CS). Without going in further details, we would just like to mention that the CS layer sits on top of the MAC layer. It classifies various packet data transport protocols and then, provide the correct connections. The supported protocols are the IEEE Ethernet 802.3 and the Internet Protocol(IP).

2.2.1.1 Physical Layer

The Open Systems Interconnection(OSI) model of computer networking defines seven abstraction layers which characterize and standardize the internal functions of a communication system. The physical layer(PHY) is the lowest layer and defines the networking hardware transmission technologies of a network [26, 27]. This fundamental layer is perhaps the most complex in terms of the varying characteristics. These characteristics are mostly concerned with the quality of transmitted data which eventually, impacts the information throughput. The features of the WRAN IEEE 802.22 physical layer are listed below:

1. **Operation and Power related:** The operation and power related specifications depend on the Spectrum Emmission specifications given the the regulatory bodies. In our case, we have taken these from the FCC guidelines which have been mentioned in the previous section.

2. **Transport:** The device should support Orthogonal Frequency Division Multiplexing (OFDM) as transport mechanism. Orthogonal Frequency Division Multiple Access (OFDMA) is used in the Uplink. The OFDM Specifications are shown in Table 2.10.

3. **Modulation:** The supported modulation schemes should be Quadarature Phase Shift Keying(QPSK), 16-Quadarture Amplitude Modulation(QAM) and 64-QAM. The corresponding IQ constellation diagrams are shown in Figure 2.3.

4. **Frame Structure:** The supported frame structure of the Cognitive WRAN is Time-Division Duplex(TDD). TDD provides better flexibility in terms of resource allocation for transmit, receive or cognitive functionalities and hence, better for the optimization of the spectrum. The frame structure is divided into 160 ms super-frames which are again subdivided into 10 ms frames. These 10 ms frames are composed of the transmit bursts, the

Table. 2.10: OFDM Requirements

Property of OFDM	Value	Remark
Total number of sub-carriers(N_FFT)	2048	-
Number of Guard Sub-carriers(N_G)	368	(184,1,183)
Number of Used Subcarriers(Nt = Nd + Np)	1680	-
Number of Data Subcarriers(Nd)	1440	-
Number of pilot sub-carriers(Np)	240	-
Data Sub-carriers/channel Pilot Sub-carriers/channel	24 4	Total of 28 subcarriers/channel
Total number of Channels	60	-
Length of cyclic prefix	74.7	in usecs (to compensate for unequal channel fadings)
Total Size of the Guard Bands	1.08	in MHz

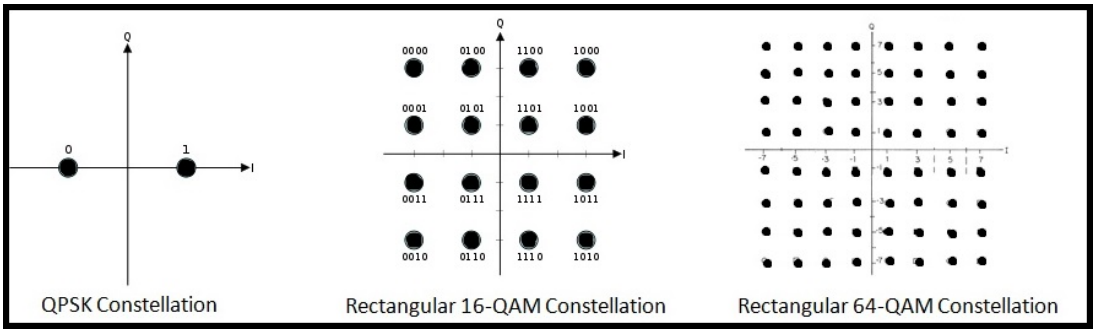

Figure. 2.3: Constellation Diagrams

receive bursts and the coexistence beacon protocol(CBP) bursts. The provision of CBP burst is kept to facilitate self co-existence. This burst shall contain information like backup channel sets, sensing times etc. The frame structure is portrayed in figure Figure 2.4.

2.2.1.2 MAC Layer specifications:

Some of the MAC layer specifications are,

Frame Structure		TDD
Frame Lengths	Superframe	160 ms
	Frame	10 ms
Frame Contents	Downlink	
	Uplink	
	Co-Existence Beacon	

Figure. 2.4: Frame Structure

1. **Connection-oriented MAC:** Establishes connection IDs and service flows which are dynamically created,
2. **QoS:** It should support QoS(Quality of Service) like UGS, rtPS, nrtPS, BE and Contention as tabulated in Figure 2.5.

QoS	Application
UGS	VoIP, T1 / E1
rtPS	MPEG video streaming
nrtPS	FTP
BE	E-mail
Contention	BW request etc.

Figure. 2.5: QoS: UGS(Unsolicited Grant Service), rtPS(Real-Time Polling Service), nrtPS(Non-Real-Time Polling Service)

2.2.2 Control and Management Plane

The functional requirements of the Control and Management Plane are beyond the scope of this version of the document. But, this Plane has serious implications on the computational capability and memory availability of the platform, so its requirements cannot be neglected altogether. Hence, while designing the hardware, we have make sure to leave out enough computational and memory resources after Data and Cognitive Plane resource allocations so that, the Control and Management functionalities can be implemented.

2.2.3 Cognitive Plane

Finally, the Cognitive plane is the logical plane which renders the special feature to the platform. This plane is again sub-divided into Spectrum Sensing block and the Geo-Location block as shown in Figure 2.2.

2.2.3.1 Spectrum Sensing

The spectrum sensing is one of the Interference Avoidance Mechanism suggested by FCC. And, from Table 2.8, we know that the system implementing a spectrum sensing mechanism has to sense a TV signal with a signal power of -114 dBm, with a 6 MHz integration bandwidth. This specification has serious implications on the hardware design. Just to illustrate the implications, lets consider Figure 2.6. Here, a simple Signal-to-Noise Ratio(SNR) calculation has been done for the signals needed to be protected from interference. By considering the thermal noise at 300 K and a typical receiver noise figure of 10 dB, we can see that the TV signal has to be detected with an SNR of around -18 dB. To detect such a signal, one has rely on good digital signal processing(DSP) techniques. Some of these, are mentioned in Figure 2.7.

Type of Device to be protected from Interference	Sensitivity Power level Requirement (dBm)	Thermal Noise (dBm/Hz)	Integration BW(in MHz)	10log(BW)	Integrated Noise Power (dBm)	Typical Receiver Noise Figure (dB)	Required SNR (dB)
Digital TV	-114	-174	6	67.78	-106.21	10	**-17.78**
Microphone	-114	-174	0.2	53.01	-120.98	10	**-3.01**

Figure. 2.6: Required Detection SNR

Blind(or Feature Based)	Signal Specific
Eigen Value Based sensing	Spectral Correlation
Multi-resolution sensing	FFT based Pilot sensing
Energy detection	Higher Order Statistics Sensing
	Time Domain Cyclostationarity

Figure. 2.7: Sensing Techniques

2.2.3.2 Geo-Location

Along with spectrum sensing, the system should also have a Geo-Location capability which requires the system to have either of,

- a Global Positioning System(GPS) as its sub-system, or
- terrestial geo-location capability(through triangulation).

2.3 Analysis of Hardware Requirements - I

After going through the FCC and WRAN IEEE 802.22 specifications, now, we shall lay down the requirements of a system operating in the TV Whitespaces. These requirements have been classified into the following categories:

1. Performance requirements
2. Computational requirements
3. External Interfaces

2.3.1 Performance Requirements

The system performance requirements that we have observed in the previous two sections have been noted in Table 2.11. These requirements are:

2.3.1.1 Bandwidth and Power

As we have seen from Tables 2.2 and 2.4, various classes of devices are defined which can operate in different bands and with different power levels. But, to fit our goal of providing a cost-effective solution which provides radar detection as well, we have chosen the widest band of continous available channels and the highest allowed operating power. So, our band of operation shall be 512 MHz to 698 MHz and the transmit power equal to 1 Watt.

2.3.1.2 Instantaneous Bandwidth

Again from Table 2.2, we know that the allowed TV channels have a bandwidth of 6 MHz. Hence, the hardware should be capable of transmitting and receiving signals having a least instantaneous bandwidth of 6 MHz.

2.3.1.3 Networking

The convergence sublayer of the WRAN requirements require compatibility with IEEE Ethernet 802.3. However, IEEE 802.3 has various versions defining different speeds [28]. Since, two 1 Gbps ethernet ports were defined in the user requirement. Hence, the system shall have a maximum datarate of 2 Gbps or 250 MB/s.

Please note that the adjacent channel power(ACP) requirement mentioned in Table 2.5 has not been included in the list of hardware requirements as, the raw ACP of an RF transmit chain can be corrected through feedback linearizing methods like digital pre-distortion. Such methods can be used to achieve the ACP emmission requirements of the TV band device. Power control shall also be achieved the same way.

Table. 2.11: Performance Requirements

S.No	Requirement	Value	Standard Specification
1	Transmit Power	30 dBm or 1 Watt	FCC Table 2.4
2	Bandwidth of Operation	512 MHz to 698 MHz	FCC Table 2.2
3	Instantaneous Bandwidth	Atleast 6 MHz	FCC Table 2.2
4	Networking	2 X 1 Gbps Ethernet	Compatibility with IEEE 802.3 and IP. System data rate of 250MB/s

2.3.2 Computational Requirements

As we have seen, the computational requirements defined by the standards include cognitive plane update Tables 2.6 to 2.9, PHY and MAC requirements of the previous section. In order to meet these requirements, a feasibility study on the Zynq7020 device has been done which shall be solely responsible for meeting those requirements. This is noted in Table 2.12

Table. 2.12: Computational Requirements

Requirement	Value	Standard Specification
Computational	Refer to Appendix A(for Zynq7000 feasibility)	IEEE 802.22, all logical planes(digital)

2.3.3 External Interfaces

The standard datapath external interfaces required for the TV band device are noted in table Table 2.13.

Table. 2.13: External Interfaces

S.No	Requirement	Value	Standard Specification
1	Network Ports	2 X 1000 Base-T	Compatibility with IEEE 802.3 and IP. System data rate is 250 MB/s
2	Air Interfaces	TV Whitespace and Global Positioning System(GPS) Antenna ports	Whitespace RF transceiver and Cognitive plane requirement respectively

Chapter 3

Whitespace Radar Capabilities

Defined as one of the functional requirements in Chapter 1, the White RHINO board should be able to perform Radar Detection under the regulatory restrictions. A pictorial depiction of an networked radar detecting airborne targets is shown in Figure 3.1. In this chapter, we shall show that even though the Whitespace regulations impose very tight restrictions which are not conducive for obtaining long radar ranges but, in the presense of networked radar nodes, efficient radar detection can be performed.

3.1 The Signal to Noise Ratio(SNR) vs. Radar Range

Here, we start with some very simplistic simulations. These simulations do not take into consideration any of the environmental signal degradation. They have been done just to obtain the trend of dependencies of the radar detection range on the various system parameters. Simulations have been done in GNU Octave for different Radar cross section (σ), duty factors (τf_p) and the number of pulses integrated (n) values. The the Radar range equation used for the simulations is given in Equation (3.1), [16]. The simulation scripts have been provided in Appendix E.

$$R_{max}{}^4 = \frac{P_{av} G \sigma n}{16\pi^2 k T B \frac{S}{N} \tau f_p}, \tag{3.1}$$

where,

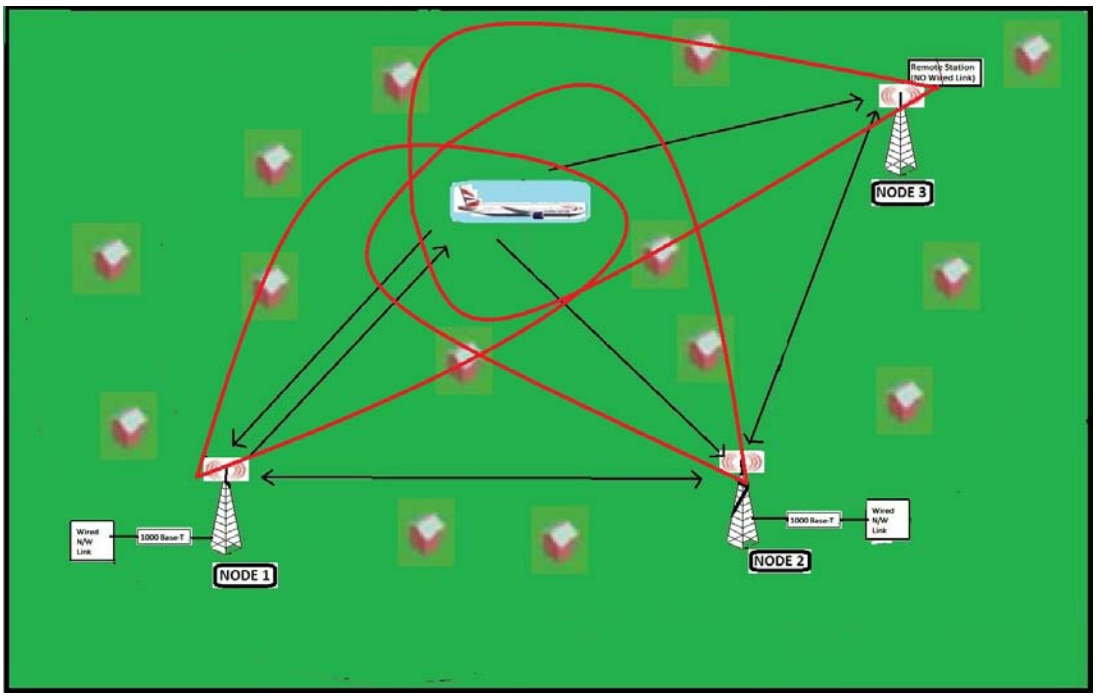

Figure. 3.1: Networked Radar: Airborne Target Scenario

- P_{av} is average power transmitted;
- G is antenna gain;
- σ is radar cross section (RCS);
- n is pulse integration factor;
- k is Boltzmann constant;
- T is noise temperature;
- B is signal bandwidth;
- $\frac{S}{N}$ is signal to noise ratio, SNR;
- τ is pulse width; and
- f_p is pulse repetition frequency.

Using a dummy variable ID defined by

$$ID = \frac{1}{\tau f_p}. \tag{3.2}$$

In these simulations, since, the only channel effect being considered is the thermal noise, a further degradation of the range and correspondingly, the required SNR, is expected. Conditions which greatly degrade the radar performance are clutter effects, environmental effects like attenuation, dispersion, and target effects like fluctuation losses etc. In Figures 3.2 to 3.4, we show the SNR vs Range plots at various values of ID and n. Figure 3.5 shows the comparison of plots of the test cases Figure 3.3, and Figure 3.4. The range values at 0 dB SNR have been tabulated in Table 3.1. Through these simulations, we have noticed that the number of pusles integrated positively impact the detection capability of the radar. This shall be used in the next section to optimize radar detection capabilities.

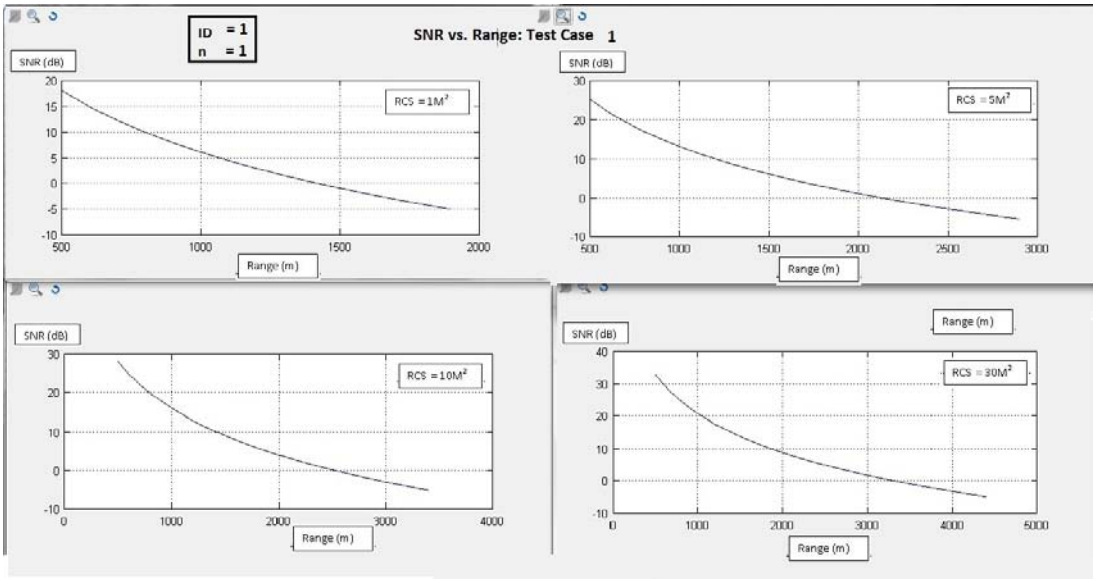

Figure. 3.2: Results: Test Case - 1 (SNR vs Range at $ID = 1$ and $n = 1$)

Table. 3.1: Results at 0 dB SNR

-	Range (km)	Range (km)	Range (km)
RCS (m^2)	$n = 1$; $ID = 1$	$n = 100$; $ID = 100$	$n = 1000$; $ID = 100$
1	1.4	14	25
5	2.1	21	40
10	2.5	25	42
30	3.1	31	48

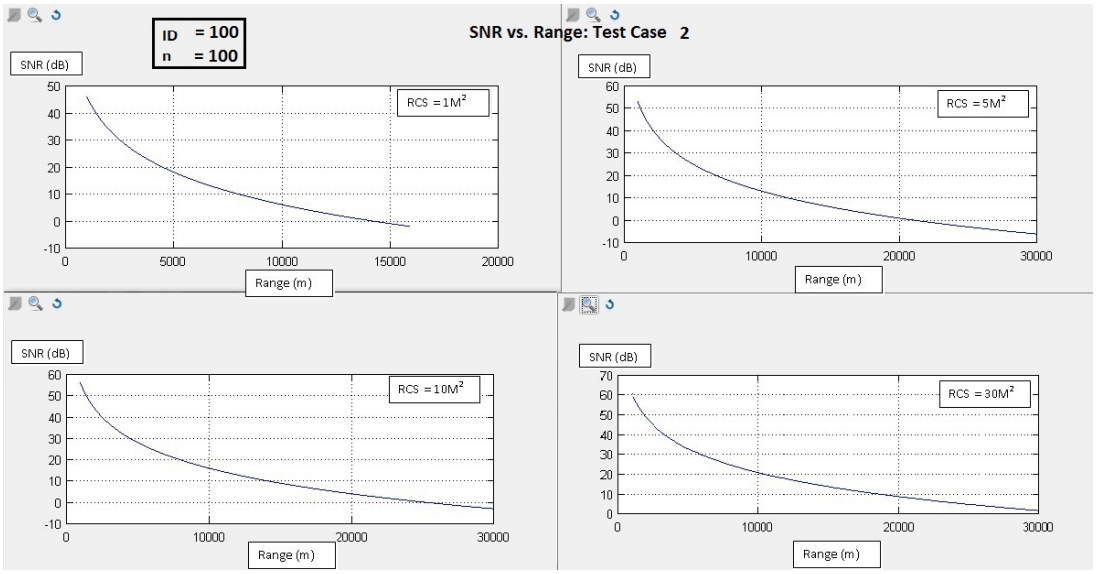

Figure. 3.3: Results: Test Case - 2, (SNR vs Range at $ID = 100$ and $n = 100$)

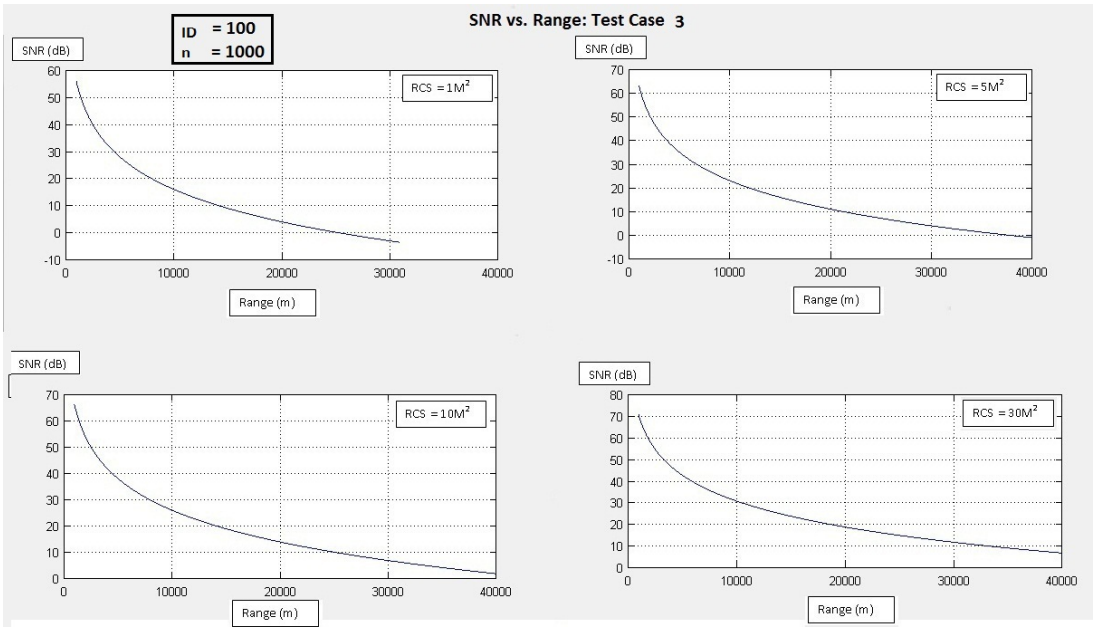

Figure. 3.4: Results: Test Case - 3 (SNR vs Range at $ID = 100$ and $n = 1000$)

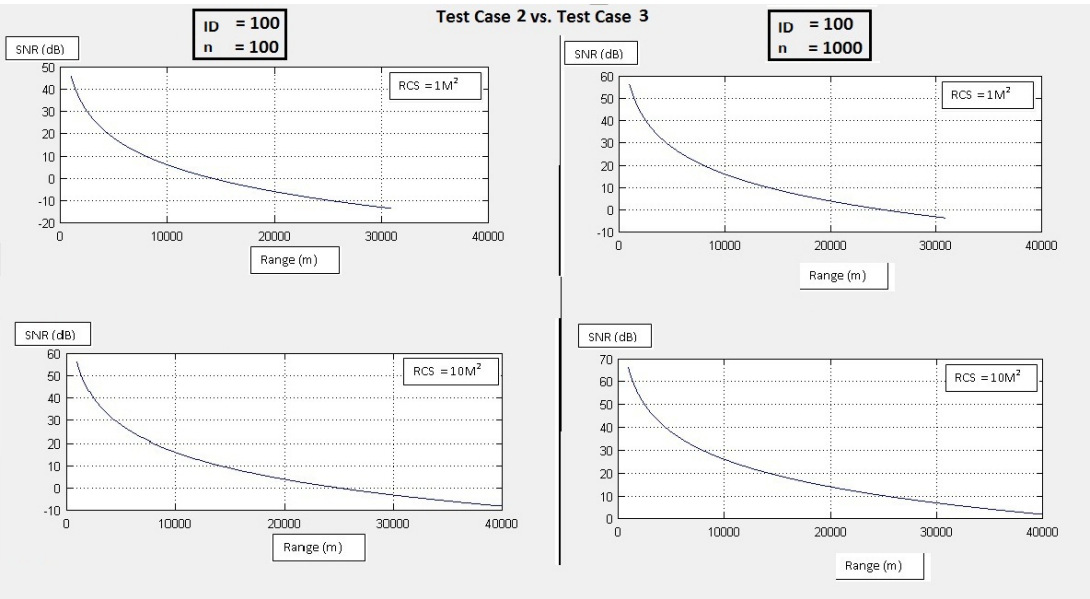

Figure. 3.5: A Comparison across test cases

3.2 Realistic Radar Simulations using CARPET

So far, we have been able to identify some parameters which can help us to enhance Radar detection. In this section, we shall exploit those parameters to obtain the radar detection capabilities under realistic environmental scenarios. This simulations have been performed using the CARPET tool shown in Figure 3.6.The tool allows us to tweak the various radar system and environment parameters. The list of environmental effects which have been considered for the simulations are Atmospheric Attenuation, Land Clutter and Rain Clutter. These have been noted in Table 3.2. Further, specific environmental parameters which include propagation parameters like atmospheric pressure, relative humidity, air temperature, water temperature, land clutter reflectivity, rainfall rate and so on are tabulated in Table 3.3. The simulations have been split up into four categories with varying target parameters like surface based or airborne and radar cross section values. In those target scenarios, the system parameters have been optimized to obtain best possible detection.
The transmitter and antenna parameters used for the simulations are well within the regulatory specifications that we discussed in chapter 2. These parameters along with other parameters used for the simulations have been noted in Tables 3.4 to 3.7. The probability of false alarm threshold is kept at 10^{-6}. Depending on the range and target parameters, some parameters like the pulse width,

pulse repetition frequency and number of integrated pulses have been optimized to achieve best possible detection.

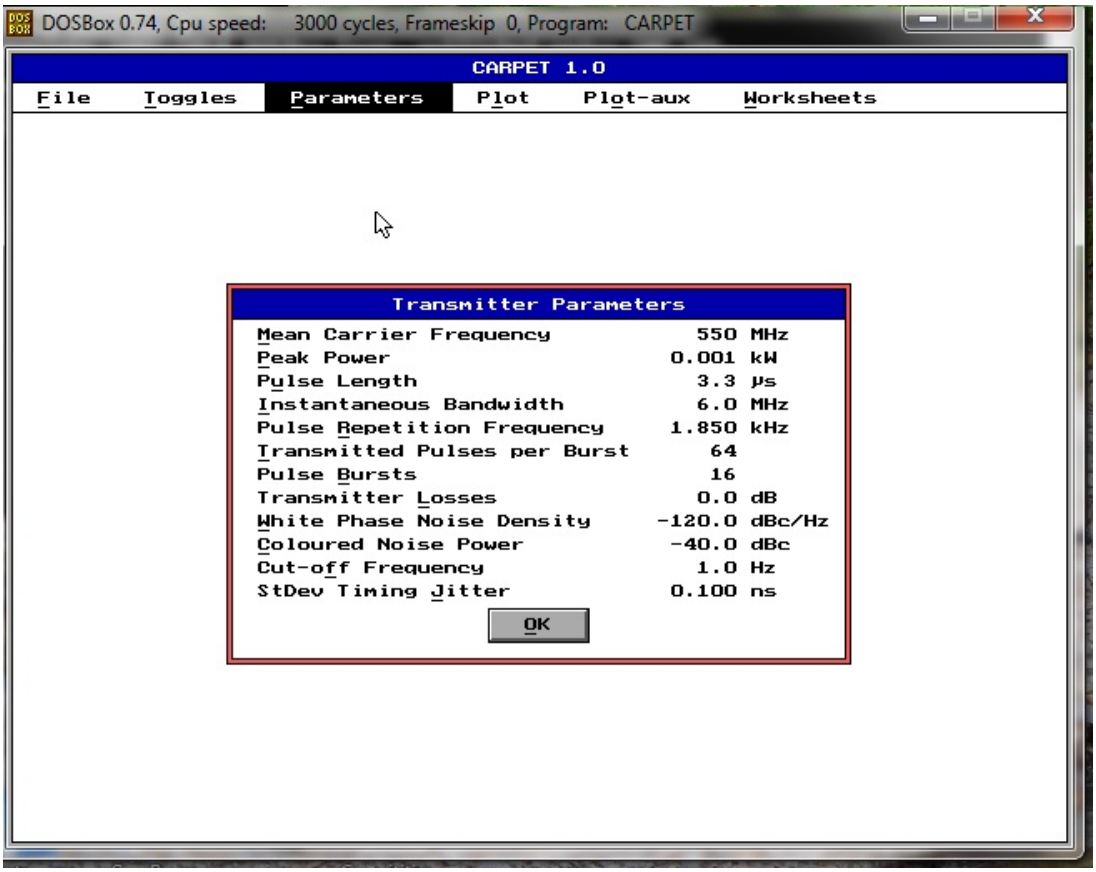

Figure. 3.6: CARPET Radar Simulation Tool

Table. 3.2: Parameter Table: Toggles

TOGGLES	VALUE
Propagation	Attenuation
Clutter	Land clutter, Rain
Jammer	N/A
Radar	Doppler Processing

3.2.1 System Test Scenario - Aerial I

The first scenario is an airborne target scenario where the target has an RCS of 10 m^2 and flying at a speed of 250 m/s at a height of 500 metres. The target

Table. 3.3: Parameter Table: Environment

PROPAGATION PARAMETERS	VALUE
Atmospheric Pressure	1020 mbar
Relative Humidity	70 percent
Air Temperature	15.0 deg celcius
Water Temperature	10.0 deg celcius
Surface Refractivity	328 Nunits
CLUTTER PARAMETERS	**VALUE**
Land Clutter Reflectivity	-38.0 dBm^2/m^2
Rainfall rate	4 mm/hr
Minimum Range Rain	5 km
Maximum Range Rain	15 km
Maximum Height Rain	3 km

is assumed to be fluctuating according to swerling-I distribution. The intial received powers have been plotted without doppler filtering. We can observe that, the land clutter has higher powers and so, in such a scenario we are unlikely to detect the signal reflected from the target with a good probability of detection, Figure 3.7. So, a doppler filter with a three-pulse canceler moving target indicator(MTI) and a hanning window has been implemented. The number of pulses per burst is 64 and the number of bursts is 16. All the parameters have been tabulated in Table 3.4. Now, we activate the doppler filter toggle. As we can see from the doppler filter transfer function in Figure 3.8, we achieve a processing gain of over 60 dB. This is reflected in the new plot for the received powers as shown in Figure 3.9. We have managed to remove all of the land clutter from the plot and now, we can have an acceptable value for the range of detection. The probability of detection per scan and the cumulative probability of detection plots for the simulated scenario have been shown in Figures 3.10 and 3.11. Here, we can observe that for a single scan we can easily detect an airborne target within a range of 2.1 kms with a probability of detection of 80%. However, the cumulative probability of detection plot provides us with an even better picture. Here, we note that, the achievable range after coherent integration of pulses has been increased conforming to our simplistic simulations in the previous section. We, therefore can achieve a range of over **3 kms** with an 80% cumulative probability of detection.

Table. 3.4: Parameter Table: System Test Scenario - Aerial I

TRANSMITTER PARAMETERS	VALUE
Mean Carrier Frequency	550 MHz
Peak Power	0.001 kW
Pulse Length	3.3 us
Instantaneous Bandwidth	6.0 MHz
Pulse Repitition Frequency	1.85 kHz
Transmitted Pulses per Burts	64
Pulse Bursts	16
ANTENNA PARAMETERS	VALUE
Type	Rectangular
Vertical Illumination	Parabolic
Polarization	Horizontal
Transmit Gain	7.0 dBi
Receive Gain	7.0 dBi
Azimuth Beamwidth	77.0 deg
Elevation Beamwidth	77.0 deg
Beamshape losses	1.0 dB
Tilt	1 deg
Height	30 m
RECEIVER PARAMETERS	VALUE
MTI	3 pulse canceler
Doppler filter bank	ON
Taper Doppler filter	Hanning
Noise Figure	3.0 dB
Receiver losses	1.0 dB
False Alarm probability	10^{-6}
TARGET PARAMETERS	VALUE
RCS	10.0 m^2
Velocity	250 m/s
Height	500.0 m
Swerling case	1

3.2.2 System Test Scenario - Aerial II

The second scenario is again an airborne target scenario where the target is much bigger and has an RCS of 50 m^2. Its speed has been taken to be 250 m/s and assumed to be flying at a height of 500 metres. Again, the target is assumed to be fluctuating according to swerling-I distribution. The intial

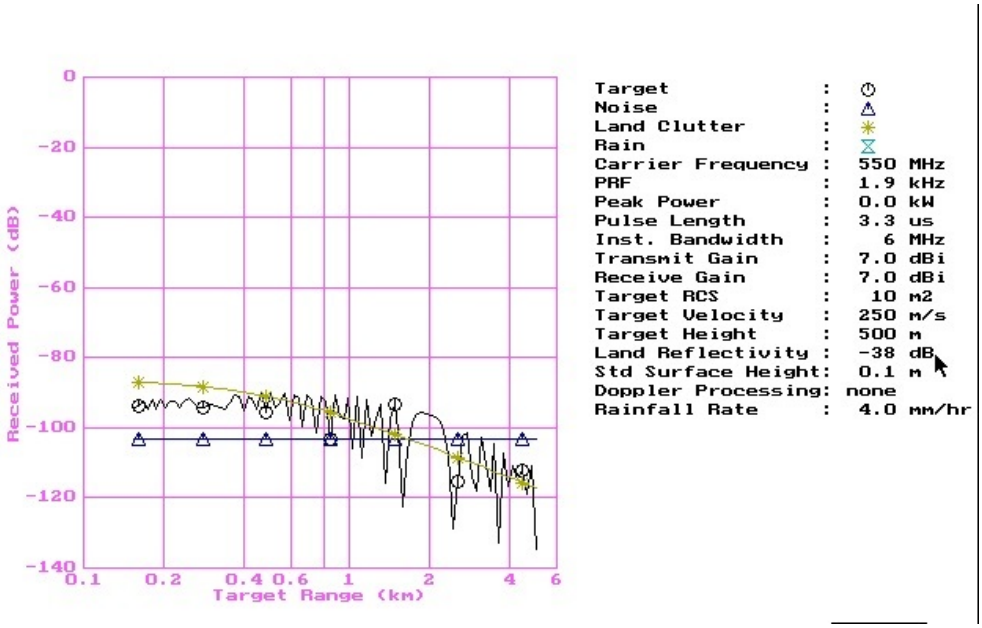

Figure. 3.7: System Test Scenario - Aerial I: Received Powers with No Doppler filter

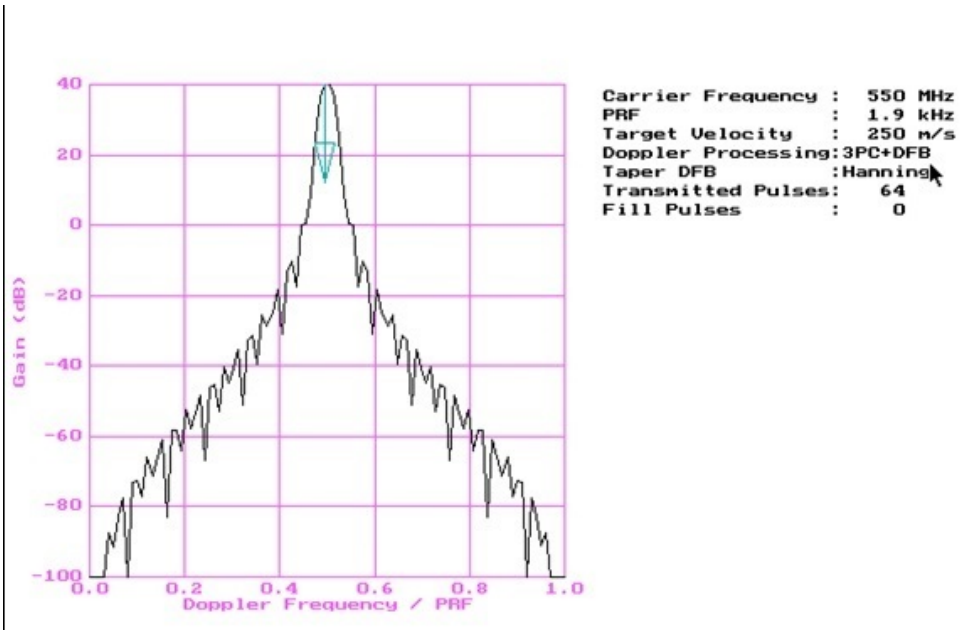

Figure. 3.8: System Test Scenario - Aerial I: Transfer Function Doppler Filter

received powers have been plotted without doppler filtering. Like the previous case, we can observe that, even though the target is larger but we are unlikely to

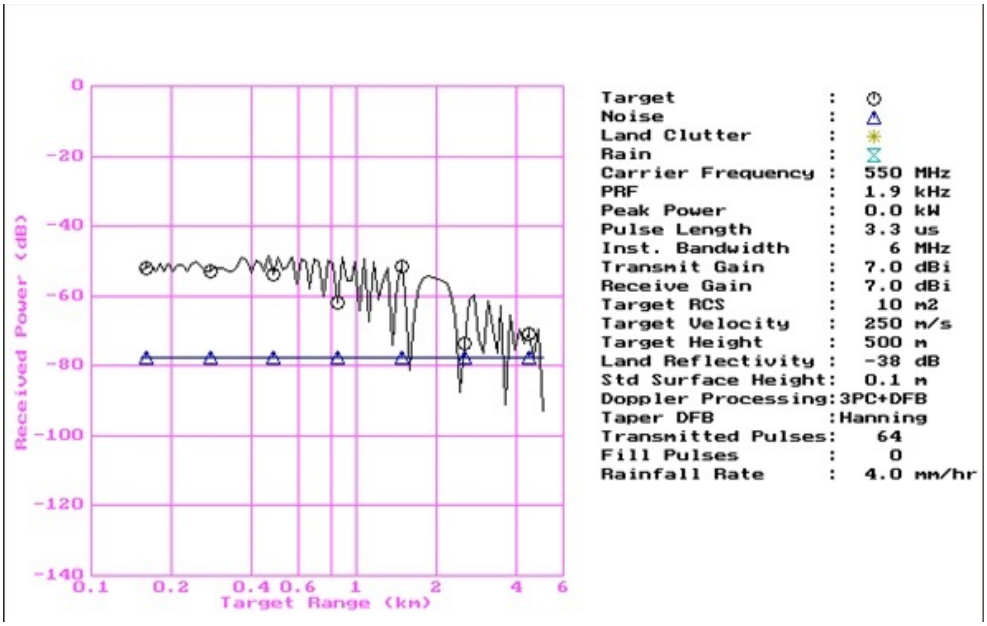

Figure. 3.9: System Test Scenario - Aerial I: Received Powers

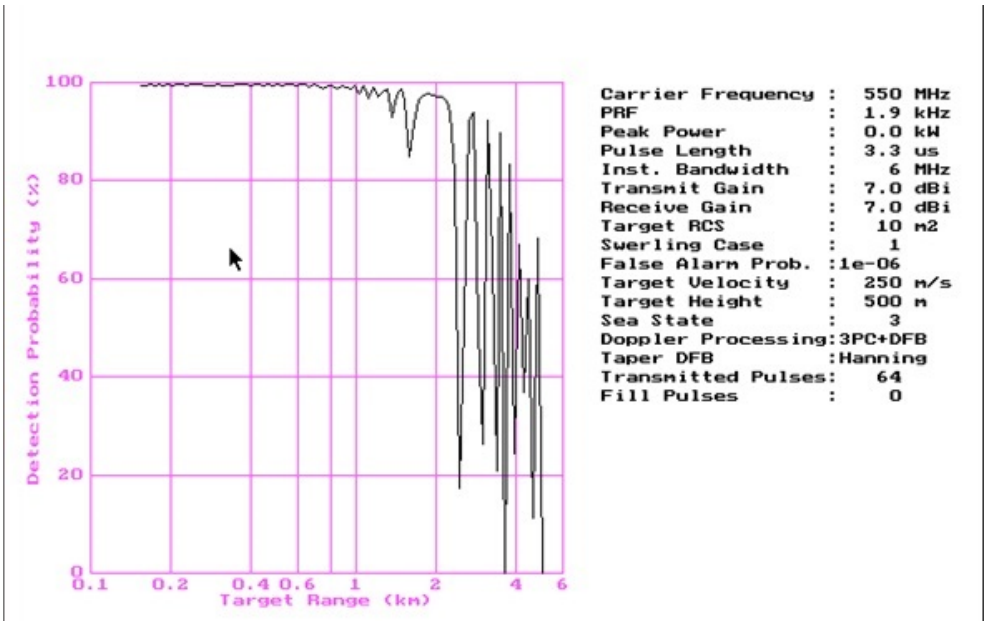

Figure. 3.10: System Test Scenario - Aerial I: Detection Probability

detect the signal reflected from the target with a good probability of detection due to presense of land clutter, Figure 3.12. With a three-pulse canceler MTI and doppler filter having Blackman window, we again manage to achieve a processing

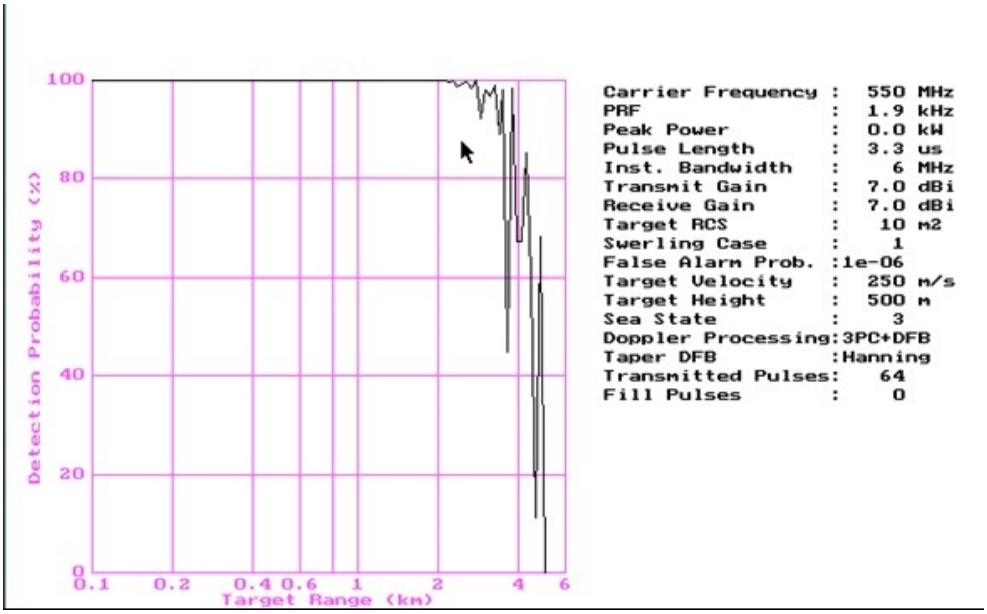

Figure. 3.11: System Test Scenario - Aerial I: Cumulative Detection Probability

gain of over 60 dB, Figure 3.13 . The number of pulses per burst is 64 and the number of bursts is 16. All the parameters have been tabulated in Table 3.5. The improvement of signal to noise and clutter ratios in the new plot for the received powers is obvious, Figure 3.14.The probability of detection per scan and the cumulative probability of detection plots for the simulated scenario have been shown in Figures 3.15 and 3.16. We can observe that in the single scan probability of detection plot, we still shall be able to achieve a range of over 2 kms with an 80% probability of detection. However, due to the dip an around 1.5 kms, there is a blind range where, the target will not be detected. This limitation can be eliminated by using integration. The cumulative probability of detection plot shows that using integration we can easily achieve a range of over **4 kms** with an 80% probability of detection.

3.2.3 System Test Scenario - Aerial III

The third test scenario is similar to the previous two. The only difference is that the RCS of the target is very small. The RCS for this set of simulations is taken to be 1 m^2. The parameters of this simulation have been noted in Table 3.6. After doppler filtering, the received powers, single scan probability of detection and cumulative probability of detection have been plotted in Figures 3.17 to 3.19. As expected, the received power reflected from the target is very less due to the

Table. 3.5: Parameter Table: System Test Scenario - Aerial II

TRANSMITTER PARAMETERS	VALUE
Mean Carrier Frequency	550 MHz
Peak Power	0.001 kW
Pulse Length	3.3 us
Instantaneous Bandwidth	6.0 MHz
Pulse Repitition Frequency	1.85 kHz
Transmitted Pulses per Burts	64
Pulse Bursts	16
ANTENNA PARAMETERS	**VALUE**
Type	Rectangular
Vertical Illumination	Parabolic
Polarization	Horizontal
Transmit Gain	7.0 dBi
Receive Gain	7.0 dBi
Azimuth Beamwidth	77.0 deg
Elevation Beamwidth	77.0 deg
Beamshape losses	1.0 dB
Tilt	1 deg
Height	30 m
RECEIVER PARAMETERS	**VALUE**
MTI	3 pulse canceler
Doppler filter bank	ON
Taper Doppler filter	Blackman
Noise Figure	3.0 dB
Receiver losses	1.0 dB
False Alarm probability	$10^{-}6$
TARGET PARAMETERS	**VALUE**
RCS	50.0 m^2
Velocity	250 m/s
Height	500.0 m
Swerling case	1

small size of the target and fluctuations cause many blind ranges. However, after integration of pulses, we can achieve a detection range of **2 kms** with 80% cumulative probability of detection. The parameters have been noted in Table 3.6.

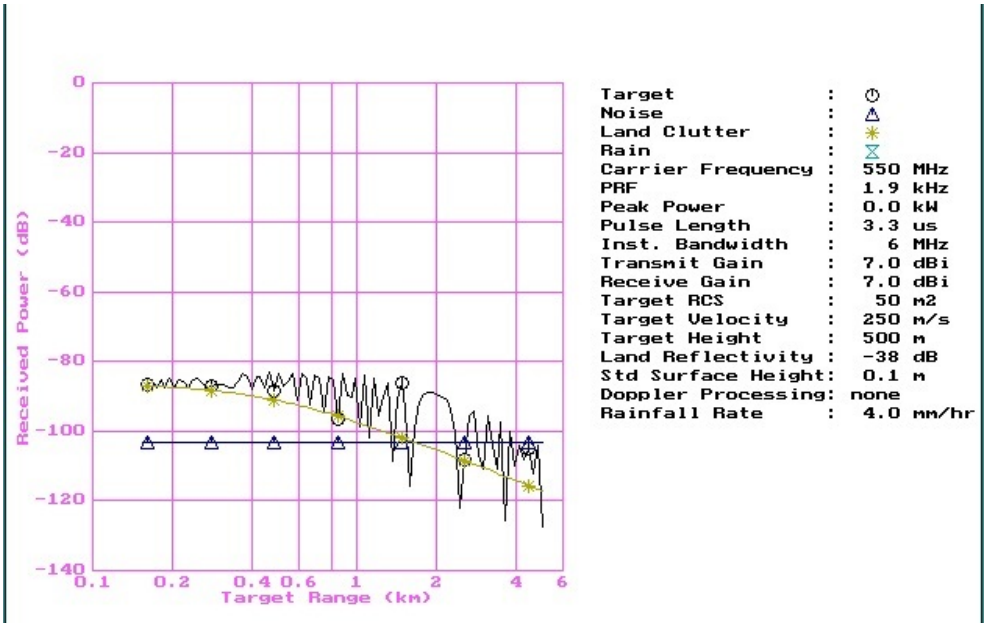

Figure. 3.12: System Test Scenario - Aerial II: Received Powers with No Doppler filter

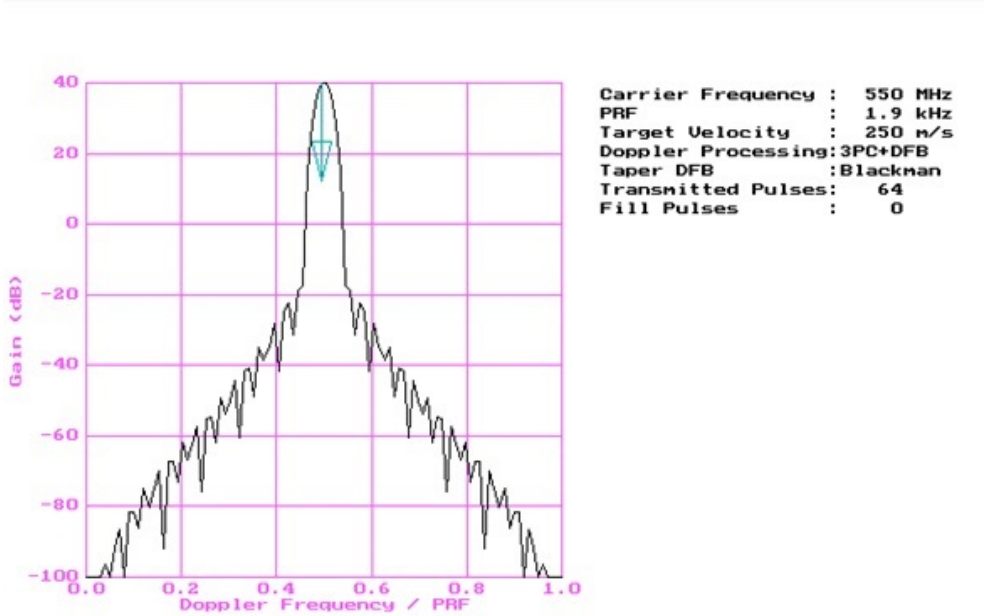

Figure. 3.13: System Test Scenario - Aerial II: Transfer Function Doppler Filter

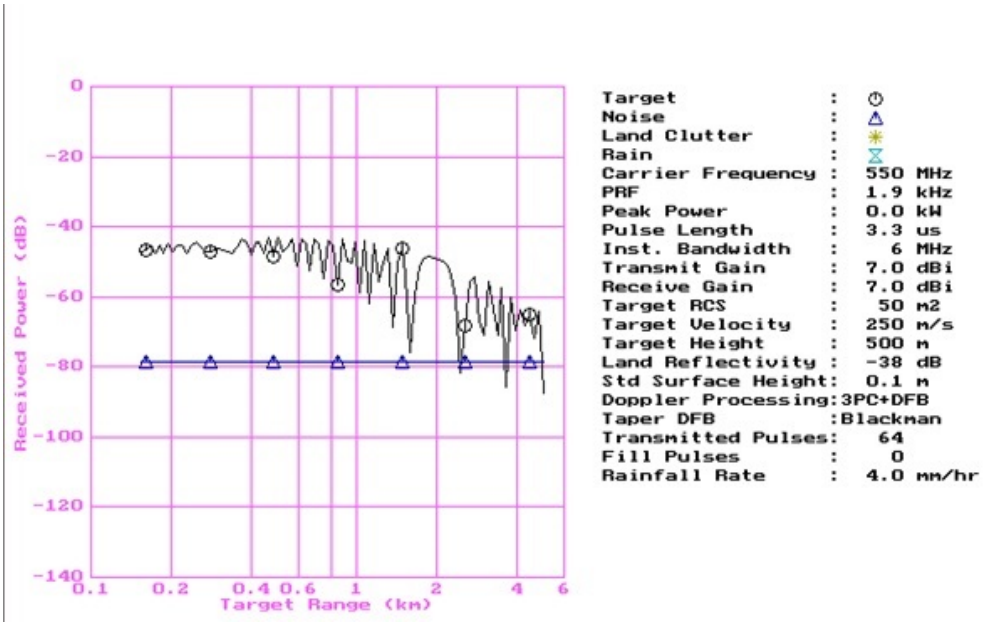

Figure. 3.14: System Test Scenario - Aerial II: Received Powers

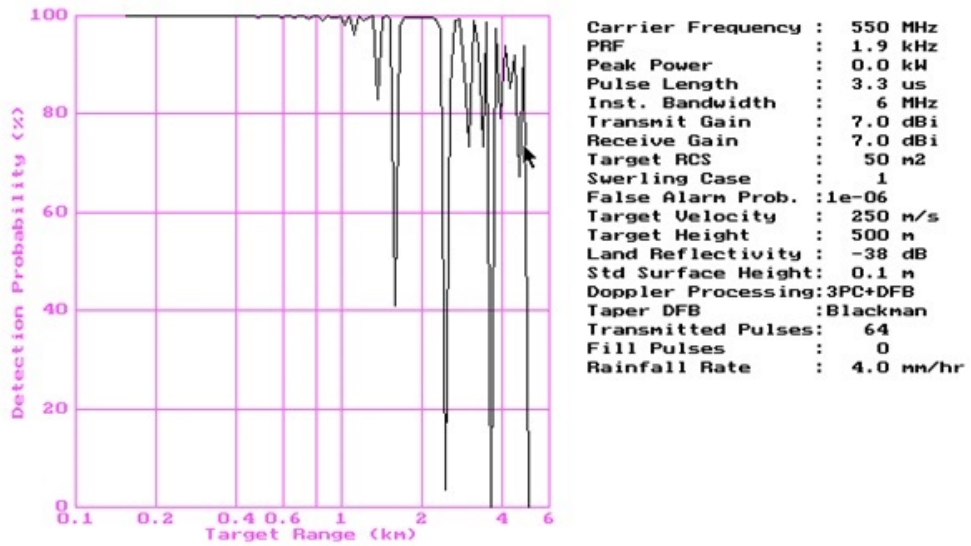

Figure. 3.15: System Test Scenario - Aerial II: Detection Probability

3.2.4 System Test Scenario - Surface

Our final simulated scenario is a ground based target having an RCS of 2 m^2. It is assumed to be moving at a velocity of 14 m/s and fluctuating accoring to

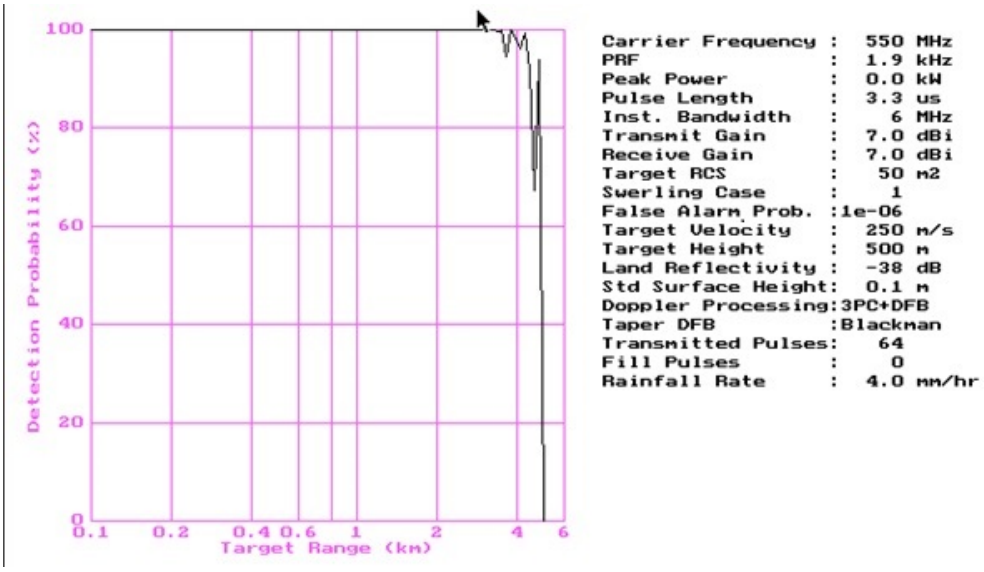

Figure. 3.16: System Test Scenario - Aerial II: Cumulative Detection Probability

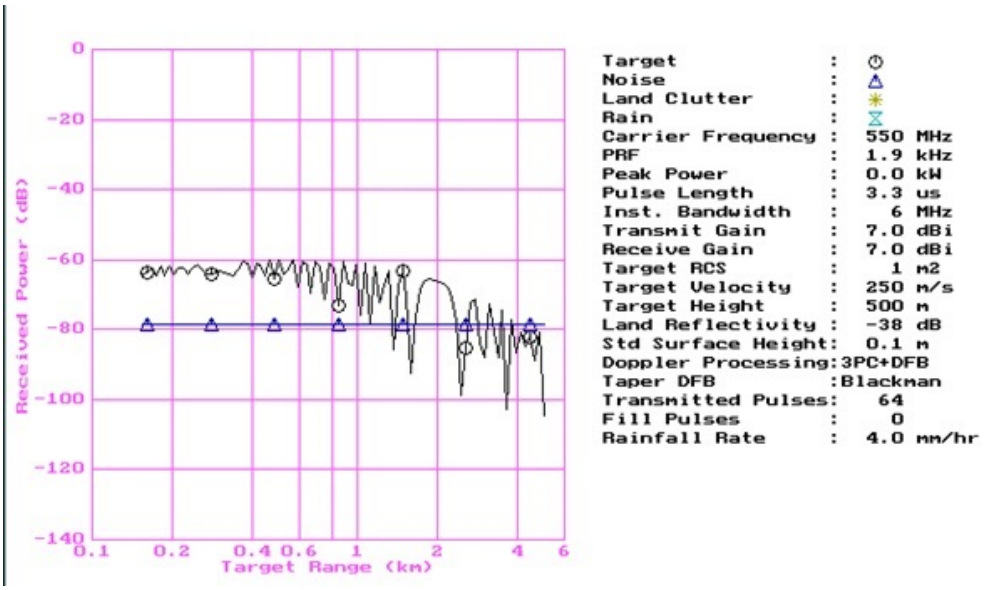

Figure. 3.17: System Test Scenario - Aerial III: Received Powers

Swerling-I distribution. Due to different velocity than the scenarios portrayed in the previous section, the pulse repition frequency and the pulse length parameters have been changed. This has been done to optimize the radar range detection. These sets of parameters have been noted in Table 3.7. Here, we note that land clutter causes severe degradation in the signal to clutter ratio. We also observe

Table. 3.6: Parameter Table: System Test Scenario - Aerial III

TRANSMITTER PARAMETERS	VALUE
Mean Carrier Frequency	550 MHz
Peak Power	0.001 kW
Pulse Length	3.3 us
Instantaneous Bandwidth	6.0 MHz
Pulse Repitition Frequency	1.85 kHz
Transmitted Pulses per Burts	64
Pulse Bursts	16
ANTENNA PARAMETERS	**VALUE**
Type	Rectangular
Vertical Illumination	Parabolic
Polarization	Horizontal
Transmit Gain	7.0 dBi
Receive Gain	7.0 dBi
Azimuth Beamwidth	77.0 deg
Elevation Beamwidth	77.0 deg
Beamshape losses	1.0 dB
Tilt	1 deg
Height	30 m
RECEIVER PARAMETERS	**VALUE**
MTI	3 pulse canceler
Doppler filter bank	ON
Taper Doppler filter	Blackman
Noise Figure	3.0 dB
Receiver losses	1.0 dB
False Alarm probability	$10^{-}6$
TARGET PARAMETERS	**VALUE**
RCS	1.0 m^2
Velocity	250 m/s
Height	500.0 m
Swerling case	1

that in this scenario, the target fluctuations are not significant. The received powers without doppler filtering have been plotted in Figure 3.20. Using the blackman tapering, we observe a processing gain of over 60 dB, Figure 3.21. The range vs. probability of detection plots are shown in Figures 3.23 and 3.24. It can be inferred that after integration, ground based targets with RCS 2 m^2 can be easily detected within a range of **2 kms**, with an 80% probability of detection.

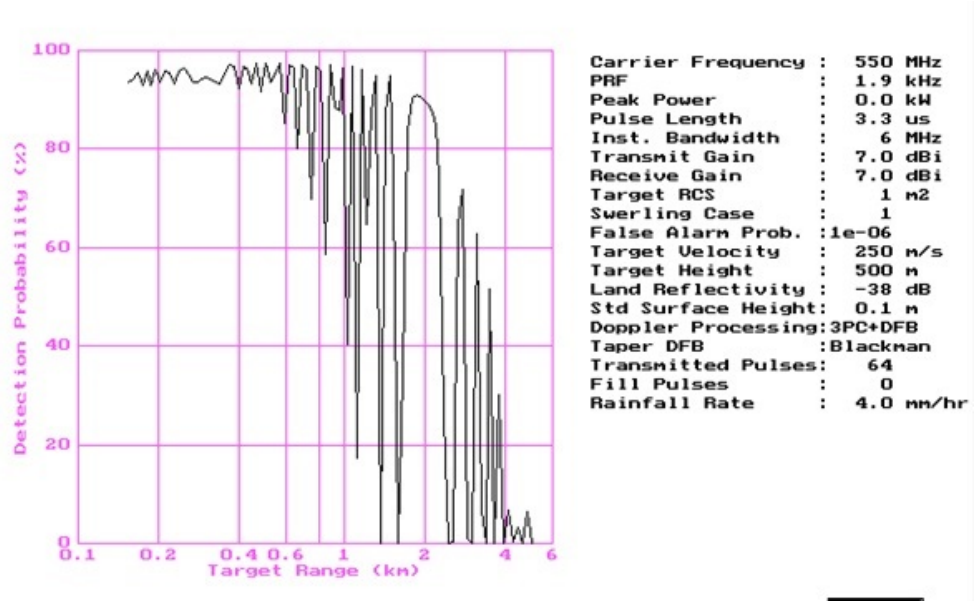

Figure. 3.18: System Test Scenario - Aerial III: Detection Probability

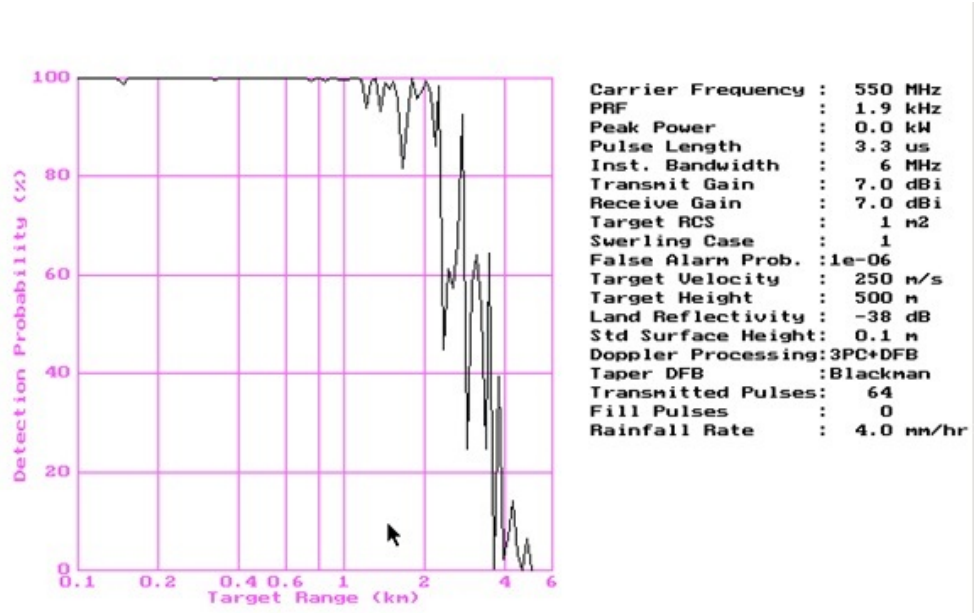

Figure. 3.19: System Test Scenario - Aerial I: Cumulative Detection Probability

Table. 3.7: Parameter Table: System Test Scenario - Surface

TRANSMITTER PARAMETERS	VALUE
Mean Carrier Frequency	550 MHz
Peak Power	0.001 kW
Pulse Length	3.3 us
Instantaneous Bandwidth	6.0 MHz
Pulse Repitition Frequency	1.85 kHz
Transmitted Pulses per Burts	64
Pulse Bursts	16
ANTENNA PARAMETERS	**VALUE**
Type	Rectangular
Vertical Illumination	Parabolic
Polarization	Horizontal
Transmit Gain	7.0 dBi
Receive Gain	7.0 dBi
Azimuth Beamwidth	77.0 deg
Elevation Beamwidth	77.0 deg
Beamshape losses	1.0 dB
Tilt	1 deg
Height	30 m
RECEIVER PARAMETERS	**VALUE**
MTI	3 pulse canceler
Doppler filter bank	ON
Taper Doppler filter	Blackman
Noise Figure	3.0 dB
Receiver losses	1.0 dB
False Alarm probability	10^{-6}
TARGET PARAMETERS	**VALUE**
RCS	2.0 m^2
Velocity	14.0 m/s
Height	1.0 m
Swerling case	1

3.3 Summary of Radar Simulations

In this chapter, we started of with very basic simulations to observe the trends, which helped us in identifying the parameters which affect the radar performance. Then, we went on to perform realistic pulsed radar simulations with the

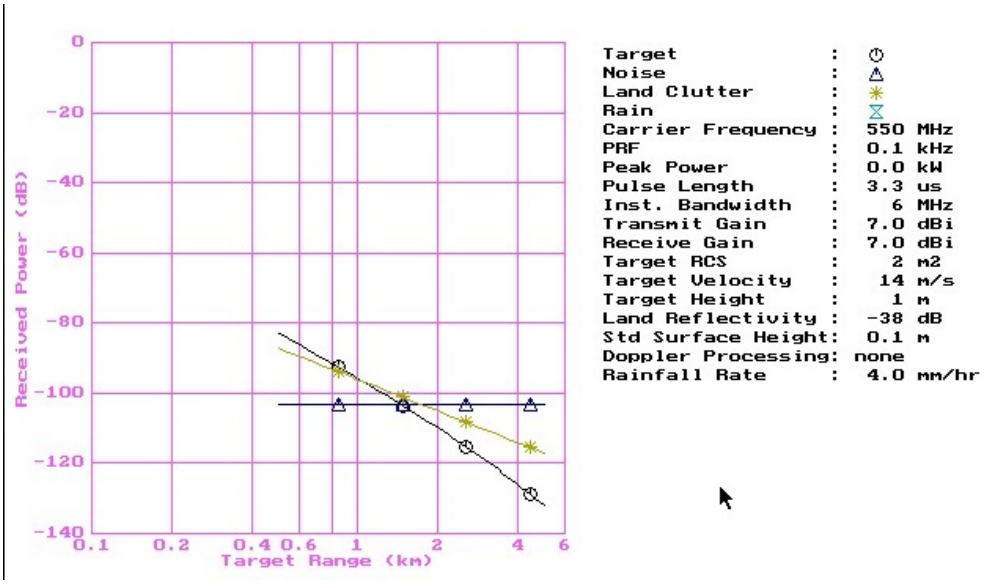

Figure. 3.20: System Test Scenario - Surface: Received Powers with No Doppler filter

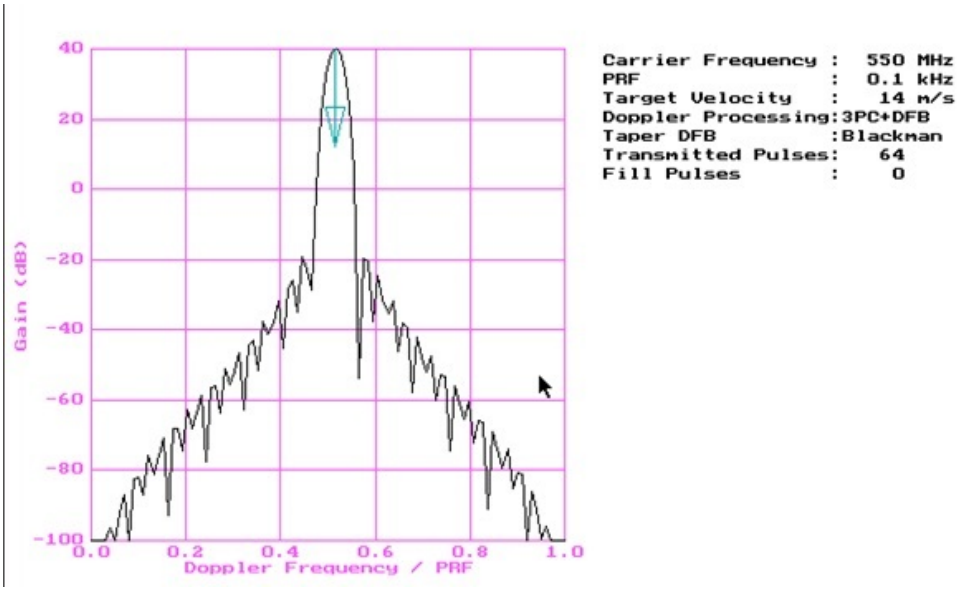

Figure. 3.21: System Test Scenario - Surface: Transfer Function Doppler Filter

CARPET tool. The simulations were classified into four different target scenarios. Through these simulations, we were able to obtain a realistic estimate of the radar range that can be achieved by the White RHINO platform. Under the simulated conditions, the radar detection capabilities are noted in Table 3.8.

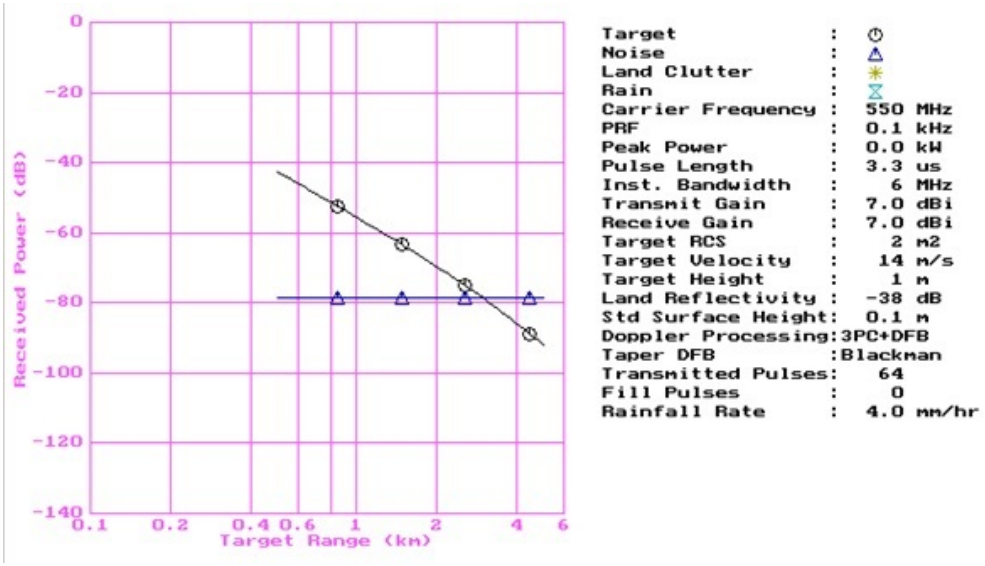

Figure. 3.22: System Test Scenario - Surface: Received Powers

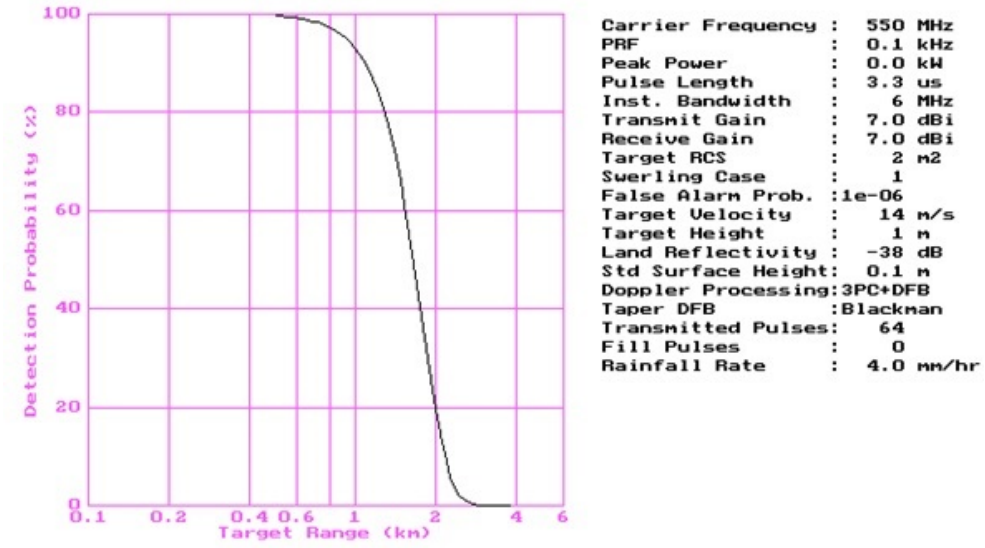

Figure. 3.23: System Test Scenario - Surface: Detection Probability

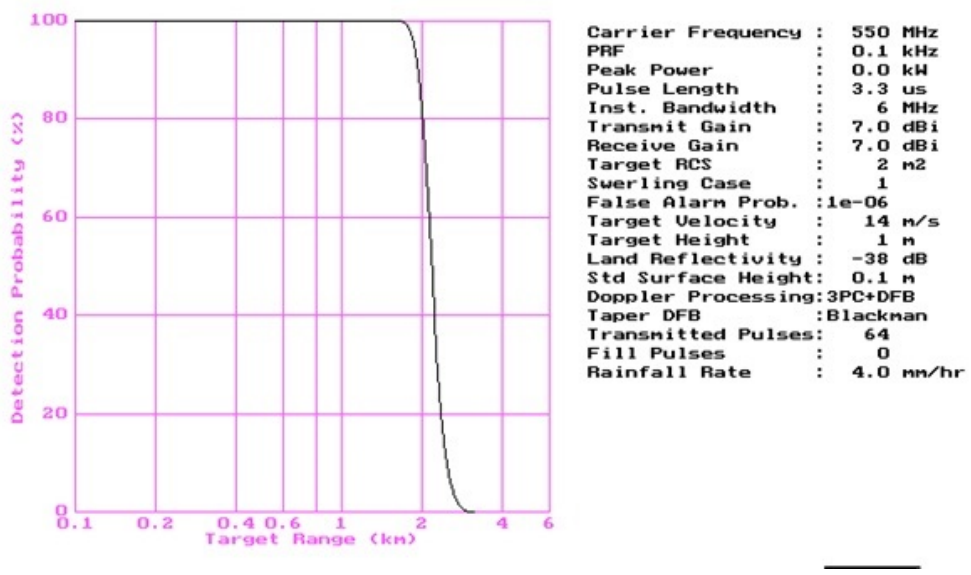

Figure. 3.24: System Test Scenario - Surface: Cumulative Detection Probability

Table. 3.8: Radar Simulations Summary

Scenario	Target RCS(m^2)	Target Speed(m/s)	Range(kms)
Aerial	1	250	2
Aerial	10	250	3
Aerial	50	250	4
Ground	2	14	2

Chapter 4

Hardware Review and Hardware Requirements-II

Before going ahead and laying out the hardware architecture, we review some existing hardwares which shall help us in taking better design decisions and hence, help us design the hardware in a better way. The hardwares that have been considered for this review are the ZedBoard, the NUTAQ Radio420S board, the TOYON Chillipepper board, NUAND Blade RF board and the USRP N210. Among these boards, the USRP N210 and the NUAND Blade RF boards are software defined radio boards and the other are general hardware platforms which use the Xilinx Zynq7000 or Lime Micro LMS6002D devices. The Zedboard is the Zynq7000 board. The NUTAQ Radio420S board and the TOYON Chillipepper are LMS6002D boards. For each board we have studied their features, their hardware architectures. We also have noted their merits and de-merits looking from the perspective of the requirements for a Whitespace Technology based Low Cost Networked radar platform.

4.1 ZedBoard

The ZedBoard is a very low cost Xilinx Zynq7000 development platform, Figure 4.1 [19]. It is a very generic board which allows one to use it for a wide range applications. Due to its expandable features, the Zedboard is very convenient for rapid prototyping. The notable feature of the Zedboard are:

- Xilinx XC7Z020-1CLG484CES Zynq-7000 AP SoC: It can be configured through QSPI flash, cascaded JTAG and SD card
- Memory: 512 MB DDR3 and 126 Mb QSPI flash
- Interfaces: USB JTAG, 10/100/1G Ethernet, USB OTG 2.0, SD Card, Digilent PMOD Headers, LPM FMC(FPGA Mezzanine card) header and so on.
- Display or Audio: The Zedboard comes with various display or audio connectors like HDMI, VGA, OLED display, audio line in, line out and microphone.

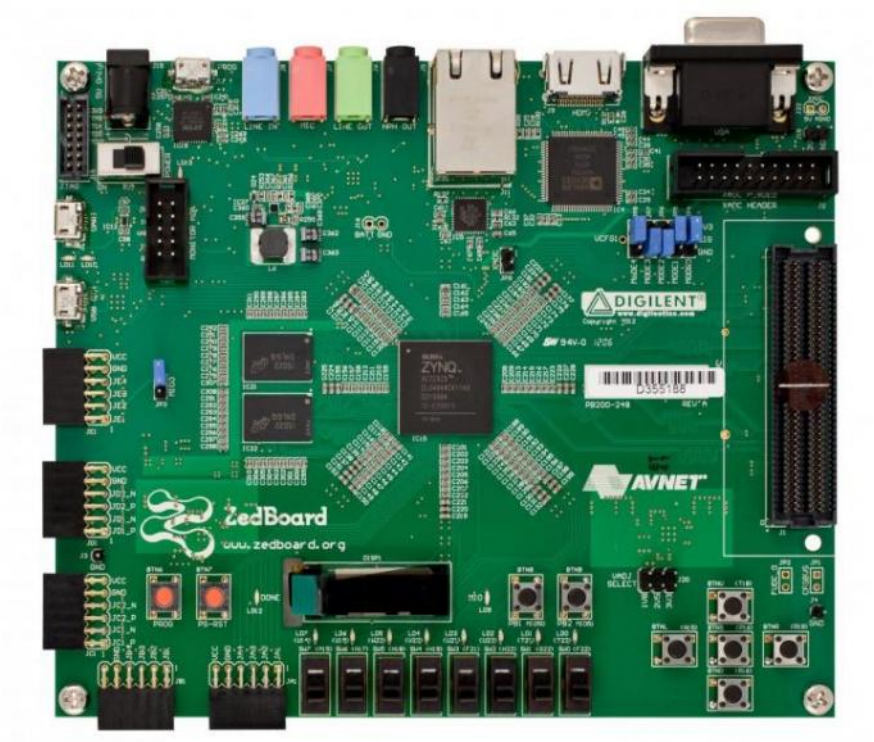

Figure. 4.1: Zedboard - Hardware Architecture. Photo Courtesy - `http://www.zedboard.org`

4.1.1 Hardware Architecture

The hardware architecture of the ZedBoard is shown in Figure 4.2. Even though we shall discuss the Zynq-7000 SoC architecture in greater detail later, we would

just like to mention that the SoC is partitioned into programmable logic(PL) and processing sysem(PS) elements. The processing sysem consists of the embedded dual core ARM Cortex A-9 processors with NEON floating point arithmatic logic units(ALUs). The programmable logic blocks have standard Xilinx FPGA elements like configurabe logic blocks(CLBs), DSP slices, RAM block and so on. There are also multiplexed IO pins which can be accessed either from the PS or the PL blocks. However, the MIOs refer to the PS pins and EMIO refer to the PL pins. As we can observe from Figure 4.2, all the control, configuration and memory interfaces like USB UART, Ethernet PHYs, DDR3, SD card, clocks, resets etc are connected to the processing system or its MIOs. The application related peripherals like the FMC, general purpose IOs(GPIOs), audio and video interfaces are connected to the programmable logic [29].

The ZedBoard has a 10-Layer PCB stackup [30]. As we can see in Figure 4.3, there are six signal layers. Three important aspects of the ZedBoard PCB design are noticeable from this stackup:

1. The two sets of internal signal layers are not standard striplines because each set has two signal layers placed adjacently to each other.
2. The internal signal layers are coupled to power planes as well instead of being coupled to just grounds
3. Due to low layer count, each power supply does not have a single plane. Instead, planes have been split to accomodate for all the various power supplies.

As a result of these three design aspects, the cost of the ZedBoard PCB is very low.

4.1.2 Merits

Following are the merits of the ZedBoard:

1. Very Low Cost, less than 400 USD.
2. Very Generic and can cater to wide variety of applications due to its expandability and various features.

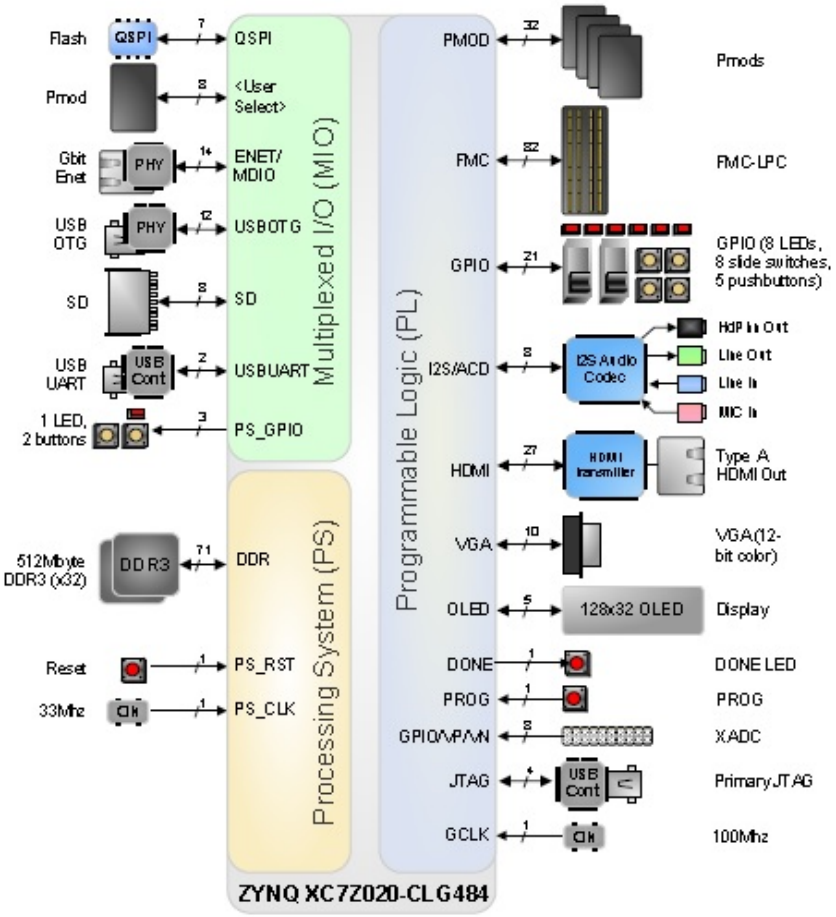

Figure. 4.2: Zedboard. Photo Courtesy - ZedBoard (Zynq Evaluation and Development) Hardware Users Guide

3. A convenient platform to learn and evaluate all capabilities of the Zynq7000 SoC.

4. Standard FMC interface for connection to daughter boards.

4.1.3 De-Merits

Following are the de-merits of the ZedBoard:

1. Not application specific as its meant to be an evaluation board.

Figure. 4.3: Zedboard - Layer Stackup. Photo Courtesy - ZedBoard, Power Distribution and Decoupling System

2. Addional plugin boards have to be used if the final goal is to have a complete communication or radar system.

3. Due to many peripherals and connectors which consume a lot of space, the size of the board(5.3" by 6.3") is large when compared to more application specific modules.

4.2 NUTAQ Radio420S board

The Radio420S FPGA mezzanine card (FMC) is a software defined radio(SDR) RF transceiver module which uses the Lime Micro LMS6002D SoC, Figure 4.4. It is a multi-mode module which supports time division duplex(TDD) as well as frequency division duplex(FDD) modes. The board has an operating frequency of 300 MHz to 3 GHz with an instantaneous bandwidth of 1.5 to 28 MHz. The board has to be connected through an FMC connector to a digital motherboard for configuration and data transfer [24]. This board is aimed for communication applications like MIMO systems, cognitive radios, WiMAX, White Space, Wi-Fi,

GSM, WCDMA and so on.

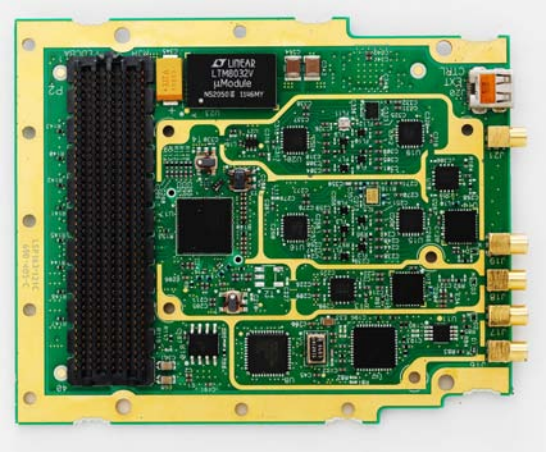

Figure. 4.4: NUTAQ - Radio420S. Photo Courtesy - `http://nutaq.com/en/products/view/+nutaq-radio420x`

4.2.1 Hardware Architecture

The board has a simple hardware architecture as shown in Figure 4.5. It contains the RF transceiver LMS6002D whose all the digital control and data line are connected to the low pin count(LPC) FMC connector. It has a selectable clock reference input. There are two RF output connectors, one for transmit and the other for receive. The outputs are connected through a set of baluns which convert the various differential transmit/receive outputs/inputs to 50 Ohm single-ended outputs/inputs respectively.

4.2.2 Merits

The merits of the NUTAQ Radio420X board are:

1. Simple design.
2. Utilizes all the features of the LMS6002D SoC.
3. Standard FMC connector for interfacing with motherboards.

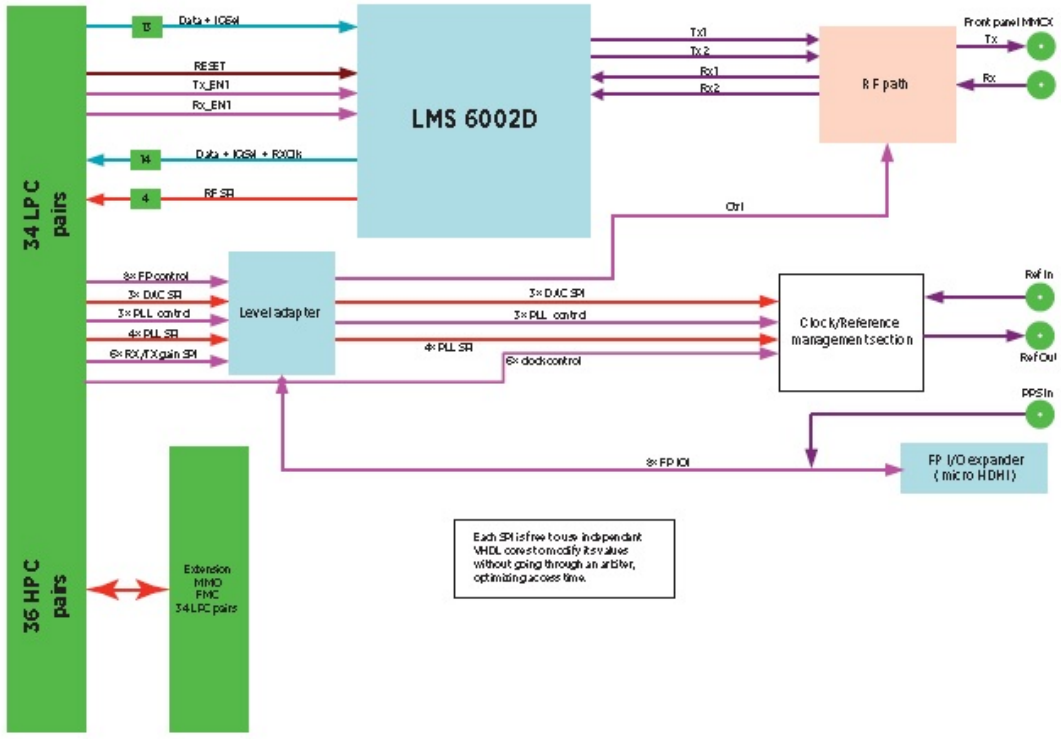

Figure. 4.5: NUTAQ - Radio420S Hardware Architecture. Photo Courtesy -`http://nutaq.com/public/files/products/Radio420x-low-res/Radio420x_Wireless_Nutaq_LowRes.pdf`

4.2.3 De-Merits

1. Lacks proper frontend section. Even though its TDD and FDD compatible but implementation of those features would require a further RF frontend board.

2. Low output power for an RF module. The peak Output power is only 10 dBm.

3. The FMC connnector consumes a major portion of the board space.

4. Again like the Zedboard, its too generic and not a particular application or communication standard oriented board.

4.3 TOYON Chillipepper board

The Chillipepper board from Toyon is another FMC based transceiver board Figure 4.6. It also consists of the Lime Micro LMS6002D as the transceiver chip however unlike the NUTAQ - Radio420S board, this board has an onboard microcontroler, amplifer and RF switches [23].

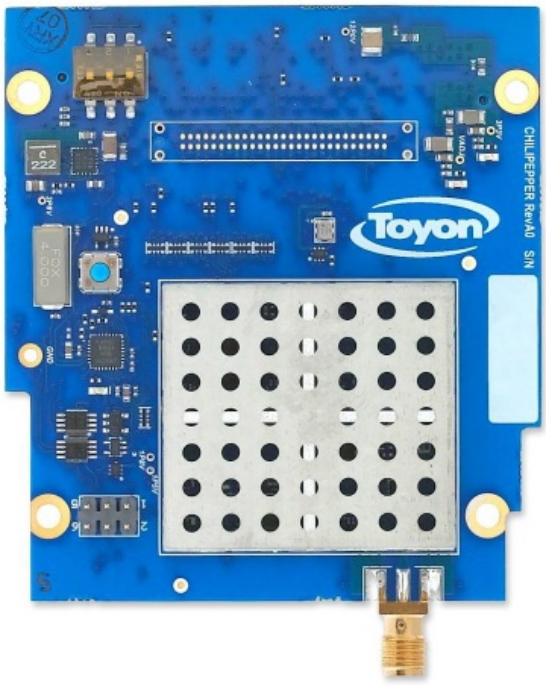

Figure. 4.6: TOYON - Chillipepper Board. Photo Courtesy - `http://www.toyon.com/downloads/Chilipepper.pdf`

4.3.1 Hardware Architecture

The hardware architecture of the Chilli Pepper board is shown in Figure 4.7. The board uses the ATMEGA168A-MMH microcontroler for the configuration of the LMS6002D SoC. The digital data interface to the SoC is connected to an FMC LPC connector. Complying with the FMC standard, this board works on voltages from 1.8V to 3.3V. It also has onboard duplexing systems which can be configured for either TDD or FDD modes. However, the FDD works at around 2.1 GHz and the TDD works at around 2.4 GHz. The TXOUT2 and RXIN2 pins of the chip are used for FDD operation and, the TXOUT1 and

RXIN1 pins are used for TDD operation. However, both the chains after getting duplexed respectively go through an Antenna Switch which allows only one of the two modes of operation. The amplifiers used offer a peak transmit power of 25 dBm [31].

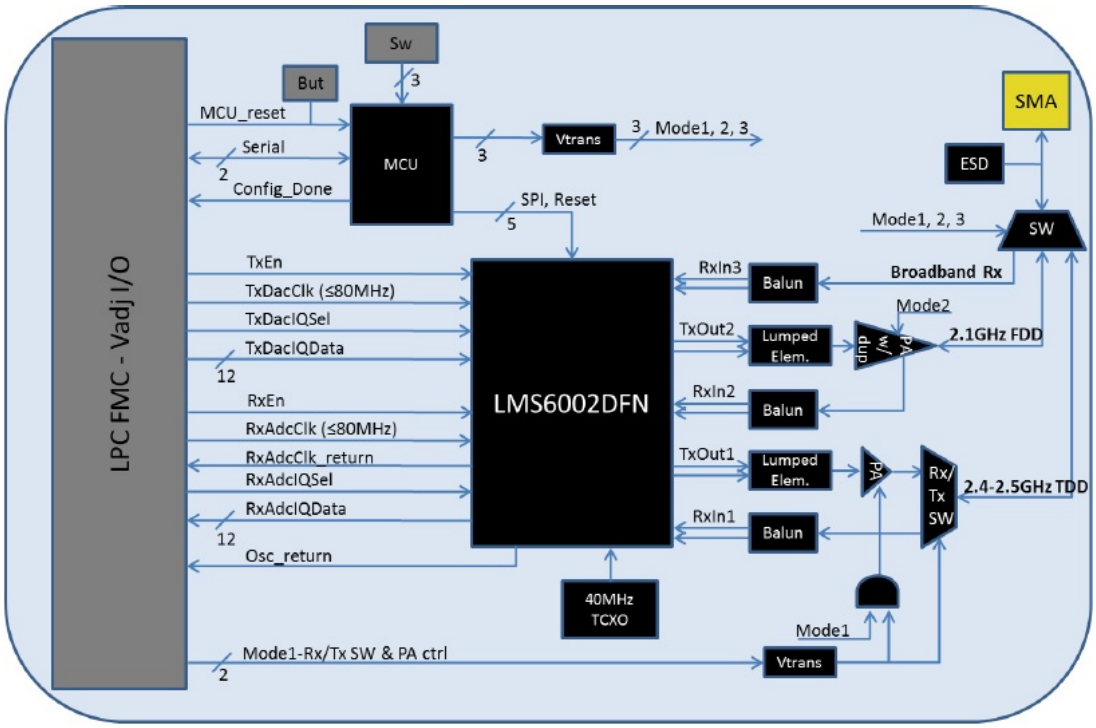

Figure. 4.7: TOYON - Chillipepper Hardware Architecture. Photo Courtesy - `http://www.toyon.com/downloads/Chilipepper.pdf`

4.3.2 Merits

The Chillipepper board has the following merits:

1. Its a compact standalone transceiver board with many desirable features. Does not need further RF boards to achieve system functionality.
2. Software Design support with HDL Coder MATLAB is available.
3. Standard FMC interface for integration with high-speed digital motherboards.

4.3.3 De-Merits

The de-merits of the Chillipepper board are as follows:

1. Priced at 750 USD, it is not a very cheap board with the functionalities available.
2. Frequencies of operation limited to around 2.1 GHz for FDD and 2.4 GHz for TDD modes.

4.4 NUAND Blade RF board

The NUAND Blade RF board is an open source USB 3.0 software defined radio(SDR) board, Figure 4.8. It contains a micro processor, an FPGA for configurable logic and the LMS6002D RF transceiver [22]. It has SMA connectors which have to connect to an RF front end. This board is capable for MIMO operation. The platform runs Linux, Windows, Mac and has GNURadio software support [32].

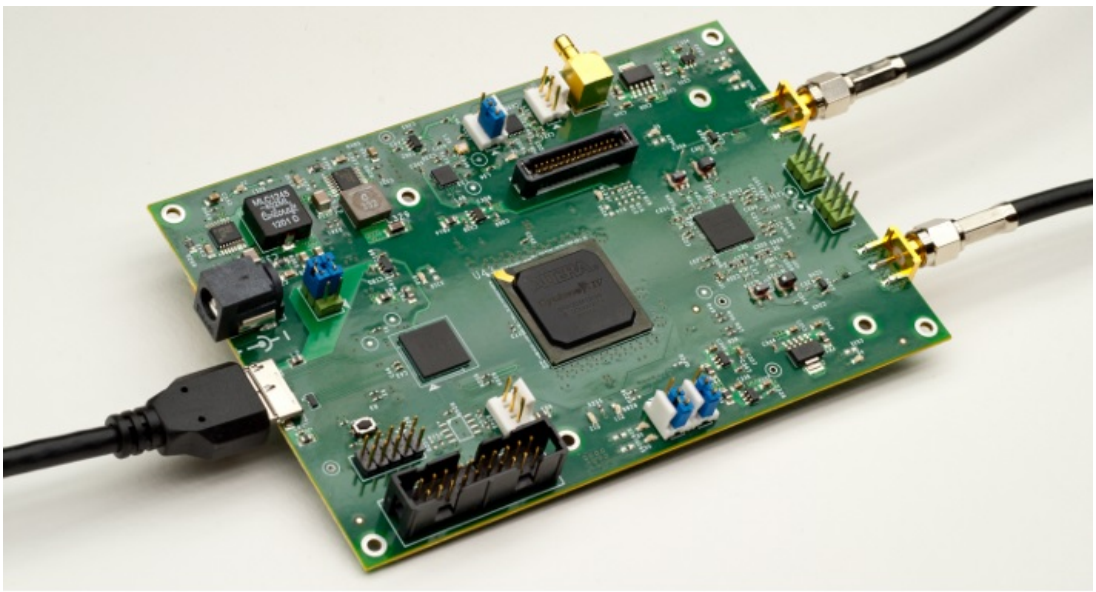

Figure. 4.8: NUAND - bladeRF board. Photo Courtesy - `http://nuand.com/`

4.4.1 Hardware Architecture

The bladeRF board has a processing core which is the ARM A-9 microprocessor, a programmable logic IC which is the Altera Cyclone-4 FPGA and the LMS6002D RF transceiver. The FPGA provides the interface between the ARM and the transceiver. Its RF section is similar to the NUTAQ Radio420S board and does not provide specific duplexing facilities. It just makes the transmit and the receive outputs available at its two SMA connectors. This board can be powered by USB and has a 512 MB embedded SRAM. The transceiver is configured through the SPI interface from the Cyclone-4 FPGA [33]. The board comes with external JTAG interfaces for both the processor and the FPGA for the debug and configuration.

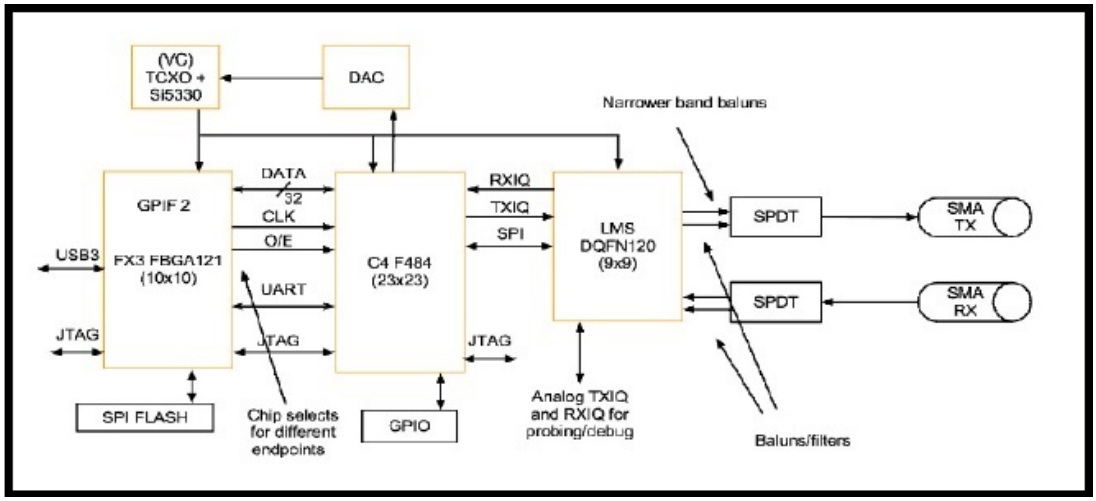

Figure. 4.9: NUAND - bladeRF Hardware Architecture. Photo Courtesy - `http://nuand.com/bladerf.pdf`

4.4.2 Merits

The board has the following merits:

1. Priced at 650 USD, it is a cost effective board which has all elements for a radio frequency system functionality.
2. GNU Radio support [32].
3. With 115 KLE(K logic elements), it offers high amount of onboard programmable resources.

4. High Speed USB 3.0 functionality.
5. Small form factor of 5" by 3.5"

4.4.3 De-Merits

Inspite of the obvious merits, the NUAND bladeRF has the following de-merits

1. Absence of ethernet functionality. In order to interface the board with packetized networks, an additional board has to be connected.
2. Absence of a duplexing system for transmit and receive ports.
3. Peak output power of 6dBm is low.

4.5 USRP N210

The USRP(Universal Software Radio Peripheral) N210 is the highest among the the classes of SDR hardwares available from Ettus Research,Figure 4.10. Its a complete system which includes digital and RF subsystems allowing users to use this piece of hardware for various applications. Packed witrh high speed FPGA, dual ADC's, DAC's and Ethernet connections, its very powerful for data streaming to and from host processors. The USRP also provides seamless integration with the GNU radio which makes it an convenient platform for rapid prototyping [17].

The notable feature are:

- Xilinx Spartan 3A-DSP 3400 FPGA: Comprises of 54 K logic cells
- Interfaces: Gigabit ethernet, 2 gbps expansion interface, RF interfaces with SMA connectors etc.
- ADC/DACs: The USRP comes with high speed dual 100 msps 14-bit ADCs and dual 400 msps 16-bit DAC.
- Software compatibility: GNU Radio, LAB VIEW and Simulink.
- Other features: DC - 6GHz operaration bandwidth, fully coherent MIMO capability, 2.5 ppm TCXO reference.

Figure. 4.10: USRP N210 - Ettus Research. Photo Courtesy - `https://www.ettus.com/product/details/UN210-KIT`

4.5.1 Hardware Architecture

The Hardware Architecture of the USRP is shown in Figure 4.11. As we can see, the Spartan 3A-DSP FPGA forms the core of the USRP N210 system. The control and management is handled by a softcore microblaze processor. At the backend, it connected to one ethernet PHY and at the front end, its connected to the high-speed dual ADCs and DACs.The FPGA is also connected to a MIMO expansion header. Two USRP have to be connected to form a 2 X 2 MIMO configuration.
The USRP without connecting to the RF daughter board consumes around 8 Watt of power. With the WBX daughter card designed to work with the USRP, it can transmit a maximum RF power of 15 dBm. The WBX has a receive noise figure of 5 dB [34].

4.5.2 Merits

The merits of the USRP N210 are as follows:

1. The board has standard connectors and standard interfaces which makes it a ready to use commercial platform.

2. The processing bandwidth is 100 MHz which is very useful for spectrum

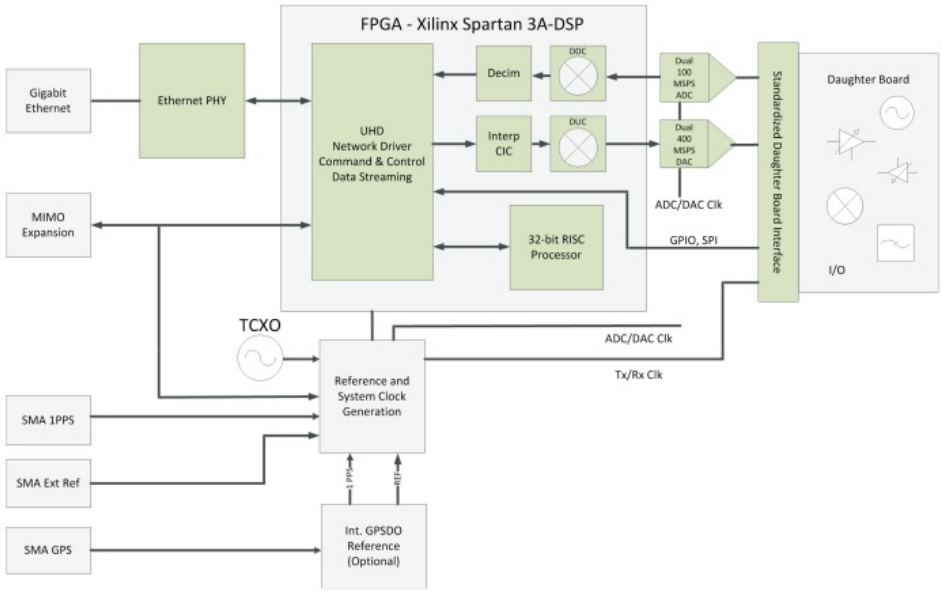

Figure. 4.11: USRP N210 - Hardware Architecture. Photo Courtesy - `https://www.ettus.com/content/files/07495_Ettus_N200-210_DS_Flyer_HR_1.pdf`

sensing kind of applications

3. Since, it integrates well with GNU Radio, fast prototyping capability of this board is a great advantage [32].

4. It does not have unnecessary extra-peripherals and hence, very application specific.

4.5.3 De-Merits

The USRP N210 has many de-merits:

1. Spartan 3A-DSP is a low end FPGA.

2. By implementing a softcore processor like the micro blaze consumes a third of its space leaving out very less space for other blocks.

3. Absense of on-board RAMs make it almost impossible to perform much signal processing on the board.

4.6 Analysis of Hardware Requirements - II

So far, we studied some of the hardware platforms currently available in the market. We also evaluated their merits and de-merits. Now, before we analyze the remaining hardware requirements, we have highlighted them in Tables 4.1 to 4.4. These requirements are ones which require a more detailed analysis and cannot be derived extracted immediatly from the Whitespace Standards.

Table. 4.1: Requirements: Computational

S.No	Requirement	Description
1	Programmable Logic	Resources present in Zynq7000's programmable logic
2	Processing System	Dual-Core ARM^{TM} Cortex A-9 processors with Single-Precision Floating Point NEON^{TM} Media Processing Engines(MPEs)
3	Memory	512 MB DDR3 SDRAM

Table. 4.2: Requirements: Performance

S.No	Requirement	Description
1	Transmit Power	30 dBm or 1 Watt
2	Bandwidth of Operation	512 MHz to 698 MHz
3	Instantaneous Bandwidth	A minimum of 6 MHz
4	Networking	2 X 1 Gbps Ethernet
5	**Power Consumption**	**Less than 25 Watts**

Table. 4.3: Requirements: External Interfaces

S.No	Requirement	Description
1	**Power Supply**	**12 Volt External supply(AC-DC Adapter or Baterry powered) and Power Over Ethernet(PoE)**
2	Network Ports	2 X 1000 Base-T (Copper)
3	**User Interfaces**	**Universal Serial Bus(USB) and Joint Test Action Group(JTAG) Interfaces**
4	Air Interfaces	TV Whitespace and Global Positioning System(GPS) Antenna ports

Table. 4.4: Requirements: Other

S.No	Requirement	Description
1	**Enclosure Size**	**17cm x 17cm x 5cm**
2	**Cost**	**Less than 1000 USD**

4.6.1 Requirements: External Interfaces, User Interfaces

The White RHINO is aimed to be an application specific board. However, in this first prototype, we would like to have more than one of the standard configuration and debug interfaces so that the hardware design flaws can be indentified, fixed and hence, the design can optimized. So, a USB host bridge connected with internal interfaces like UART, JTAG and I2C is highly recommended. Also, a direct JTAG interface, which is very useful for testing and debug, incase the USB interface does not perform as desired due to some unforseen reasons. Thus, justifying the use of these two external configuration and debug interfaces in Table 4.3.

4.6.2 Requirements: External Interfaces, Power Supply

A network node which shall be installed in remote locations should be capable of being powered by multiple sources. Power over ethernet(PoE) is a technique through which power can be transferred from a power sourcing equipment(PSE) to a powered device(PD). The advantages of PoE are:

- Power can be transferred over long cables
- Power can transferred on the same conductors as data

Hence, using such a means of powering a network device has the following advatages:

- Makes the system less bulky: Does not require the system to have heavy and bulky power mains transformers.
- Makes the system less dependent on the local power availability: Since, the system derives power from a remote cabled network, its operation and performance is not dependent on the power fluctuations or cutouts. In interior locations, power scarcity is very common.

Inspite of the obvious advantages, we have decided to go with a switchable power supply between the PoE and the 12 V DC supply. The decision has been made to reduce the testing interdependencies.

4.6.3 Requirements: Performance, Power Consumption

Here, the requirements quote a value of 25 Watts as the maximum power consumption of the White RHINO board. First, let us consider a following points,

1. PoE power classes: The specification IEEE 802.3at PoE+ defines two major classes. One(Type-I) is for PDs operating at a power levels less than 13 Watts and then, there is a power class(Type-II) under which a PSE can supply upto 25.5 Watts of power to the PD [35].
2. Typical power consumption: RFPA 3800 is a power amplifier from RFMD. It has an output P1dB of 36 dBm which means that it can transmit a maximum output opwer of 5 Watts. This amplifier requires a supply of 7 V and draws typically 1.4 A current at that power. Thus, the device draws close to 10 Watt [36].

Clearly, the PoE class of the system cannot be Type-I as just the final stage power amplifier itself consumes around 10 Watts of power. Hence, in order to make the system PoE compatible, the power consumption should be less than 25 Watts which is the highest power available from the PSE under PoE+. Thus, justifying the requirement.

4.6.4 Other Requirements

Among the other requirements, firstly we have the Size of the Enclosure requirement. The size of the enclosure for the White RHINO is an item which should be taken care of while performing the PCB design of the system. The size of the PCB decides the size of the enclosure. Finally, cost of the system has to be ensured by making wise design decisions at every step of the design process. These include component selection, schematic design and PCB design respectively.

Chapter 5

White RHINO: The Harware Architecture

So far, we have discussed the various requirements for the design of the White RHINO hardware platform. We also reviewed various commercially available platforms and analyzed their advantages as well as disadvantages. Now, we shall present the White RHINO hardware architecture in the form of a block diagram and then, discuss its salient features. We shall justify the presence of subsystems from requirements point of view. In this chapter, we shall also discuss the selection of the major components and then, go on to discuss a critical design decision of splitting the hardware into two printed circuit boards(PCBs).

5.1 Hardware Architecture: Major Blocks

The hardware architecture of White RHINO is presented in Figure 5.1. In order to comply with the White RHINO requirements in Tables 1.1 to 1.4, the following hardware blocks have been identified:

5.1.1 Power supply and Clock Blocks

These blocks are responsible for providing power and all major clock signals to the various devices onboard.

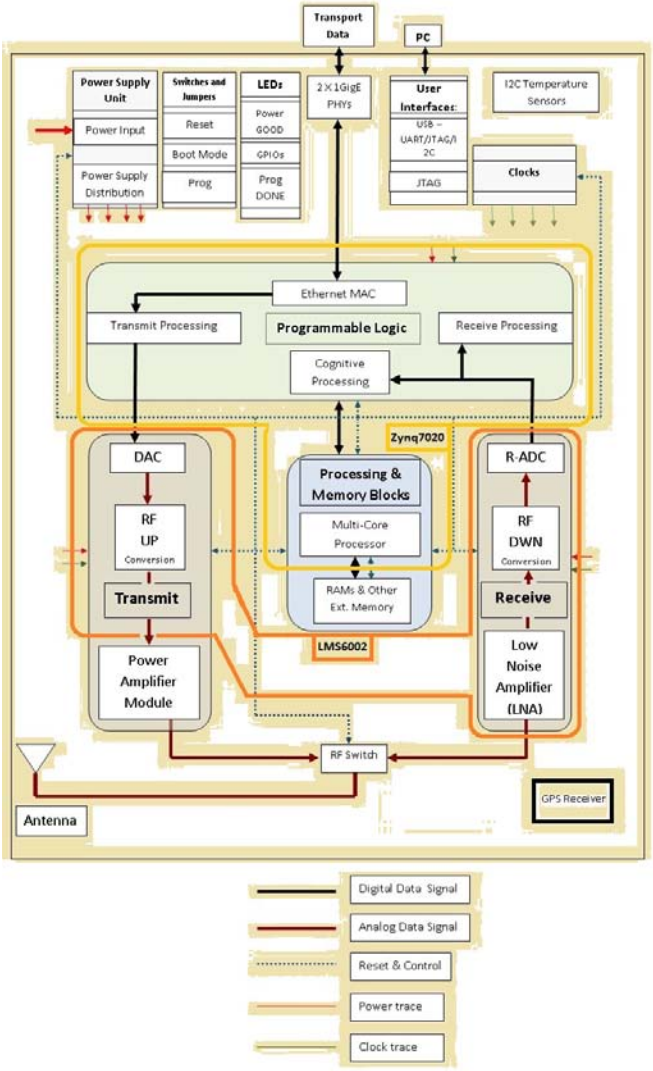

Figure. 5.1: White RHINO Hardware: High Level Block Diagram

5.1.2 Processing and Memory Blocks

These blocks shall handle all the configuration and management related tasks of the platform. Adding to that, they shall perform high-speed computational operations for the cognitive plane defined in IEEE 802.22, [37].

5.1.3 Data-Path Blocks

White RHINO is a communication system and hence, we require data-path elements on the board. Following are the required Data-Path Blocks in the system:

- **Ethernet PHY:** At the digital back-end, this is the first block in the Data Path. This block is responsible for converting the Ethernet Data from the Media Dependent Interface (like Base-T,Copper or Base-X,Optical fiber) to a Media Independent Interface(MII,GMII,SGMII,RGMII etc) and vice-versa.
- **Programmable Logic Block:** The Programmable logic then, shall handle the bulk of digital transmit and receive data-path tasks e.g, scheduling/de-scheduling, coding/de-coding, modulation/de-modulation, OFDM/OFDMA etc.
- **RF Blocks:** Finally, we have the RF blocks which shall be responsible for digital to analog/analog to digital conversion, up/down conversion, power amplification, filtering, and TDD switching. After the TDD switch the signal is tranmitted or received through the TV Antenna.

5.1.4 Cognitive Blocks

As we know now, the IEEE802.22 defines a cognitive plane. Hence, we require specific blocks for the implemention of this plane. At the hardware level, the only extra block that needs to be implemented is the GPS system for Geolocation. The cognitive processing shall be facilitated through the Data-Path blocks and the Processing and Memory Blocks but its discussion is beyond the scope of the document since they are at the algorithm level.

5.1.5 User Blocks

There shall be various user blocks on the board. These blocks shall facilitate the user to set operating conditions and allow the user to efficiently debug. These include the various switches, jumpers, LED's, USB-UART/JTAG/I2C and JTAG interfaces. Together, they will allow the user to have absolute control over the system and hence, facilitate implementation of efficient applications.

5.1.6 Control and Monitoring Block

This block ensures that the system functions in a reliable way. Its functions shall be to estimate the system performance as well as provide system shutdown in conditions when the system cannot function in a reliable way. There shall be temperature sensosrs at various critical locations on the board. These sensors shall provide the board temperature at those locations through the I2C interface which can be accessed by the processing block. The processing block then will take necessary actions.

5.2 Selection of major components

In order to reduce the size, complexity and hence, the cost of the board, following critical devices have been selected. The feasilibity of these devices have been performed and documented in Appendix B.

5.2.1 Zynq7020(Xilinx) for Processing and Programmable Logic

The Zynq7020 has embebbed dual core 800 MHz ARM Cortex-A9 processors with NEON single precision floating point ALUs, 85K logic cells and 220 DSP slices [38]. This component has been specified as a user requirement. However, through our feasibility study in Appendix B, we have found that the Zynq7020 is very suited for our purpose. The IEEE802.22 defines some highly resource consuming DSP blocks. The major share of the cognitive processing shall be done in one of the two cores of the embedded ARM Cortex A9 floating point processors. In our study, we use a single complex multiplier for the generation of the covariance matrix. This process is required for the Eigen Value method of Spectrum Sensing which has been proposed as a preferred algorithm in the IEEE802.22 standard documents. Since, the matrix data shall be stored in an external memory, the amount of resources consumed (for LUTs, FFs and DSP slices) shall be less than 3 percent of the available respurces as presented in Appendix B. The remaining resources in the FPGA shall be used for other data-path and management blocks. Hence, Zynq7020 is a compact and powerful SoC which provides us with enough computational resources in the form of its programmable logic and processing system blocks.

5.2.2 LMS6002(Lime Micro) as RF Transceiver

LMS6002 from Lime Micro has been chosen for the platform because of its wide-band performance of 3 GHz and a maximum instantaneous bandwidth of 28 MHz [39]. It has embedded ADCs, DACs, synthesizers, Up/Down Convertors, variable gain amplifiers, Time Division Duplex (TDD) support and hence, is apt for a compact system. However, it has a maximum transmit output power of 6 dBm and hence, an additional amplifier section shall be used to boost it to the specified power levels. Some of its general specifictions have been shown in Figure 5.2

General Specifications						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
REFCLK	Reference Clock	No gaps in Freq resolution.	26	-	41	MHz
PN	Phase Noise	1MHz Offset		-130		dBc/Hz
Transmit						
WEVM	Transmitter EVM	UMTS test model 1		2		%
WACLR1	1st Adjacent channel Leakage				-50	dBc
GTx	Transmit Gain control range	TXVGA1, TXVGA2, 1dB steps		60		dB
Receive						
RX NF	Noise figure			5.5		dB
SENS GSM	GSM Sensibility (Listen Mode)	GSM (2dB FE loss)		-105		dBm
WSens	UMTS Sensitivity (Full duplex)	12.2kBs Single Code (2dB FE loss)			-115	dBm

Figure. 5.2: LMS6002(Lime Micro): General Specifications. Photo Courtesy - `http://www.limemicro.com/download/Lime_ProductBrief.pdf`

5.2.3 RFPA3800(RFMD) as Final Stage Amplifier

There is a dearth of wide-band, low power amplifiers operating in the VHF and UHF frequencies in the open market. However, we aim to build a low cost platform. Hence, this device has been chosen for the first prototype, which has a maximum wide-band output power of around 25 dBm. Its still has to be matched to achieve a wider bandwidth of operation in order to meet the specifications, [36]. Some of its specifications at 460MHz have been shown in Figure 5.3

5.2.4 MT41K128M16JT-125(Micron) as DDR3 SDRAM

The User Requirements define that the processing system architecture of the White RHINO board has to be similar to that of the Zedboard. So, the DDR3

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
460 MHz					V_{CC}=7.0V, V_{BIAS}=7.0V, I_{CQ}=650mA
Frequency	450	460	470	MHz	EVB tuned for linear operation
Input Power (P_{IN})			23	dBm	V_{CC}<7.5V, load VSWR<2:1
Gain (S21)		18		dB	
OIP3		48		dBm	20dBm/tone, tone spacing=1MHz
P1dB		36.7		dBm	EVB tuned for linear operation
Efficiency at P3dB		50		%	At P3dB, EVB tuned for linear operation
Input Return Loss (S11)		15		dB	
Output Return Loss (S22)		9		dB	
Noise Figure		5		dB	
WCDMA Ch Power at -65dBc ACPR		19.5		dBm	3GPP 3.5, Test Model 1, 64 DPCH
WCDMA Ch Power at -55dBc ACPR		24.5		dBm	3GPP 3.5, Test Model 1, 64 DPCH

Figure. 5.3: RFPA3800: General Specifications. Photo Courtesy - `http://www.rfmd.com/CS/Documents/RFPA3800DS.pdf`

SDRAM interface design has been done with the Zedboard design as the reference. However, the 2 X 128MB DDR3 part(Micron MT41J128M16HA-15ED) that the Zedboard uses is an out of stock component. Hence, we had to search for an alternate component. A similar but newer part(Micron MT41K128M16JT-125) which has even the same pin mapping and the footprint as the previous device has been chosen as the DDR3 SDRAM part. Two of these 128 MB devices have been used to achieve 512 MB of DRAM memory. Some general specifications have been tabulated in Table 5.1, [40].

Table. 5.1: MT41K128M16JT-125(Micron): General specifications

Package	Density	Clock Rate	Width	Depth	Pin Count
FBGA	2Gb	800 MHz	x16	128 Mb	96-ball

5.2.5 DP83865(National Semiconductor) as Ethernet PHY

The White RHINO user requirements specify 2 X 1 Gbps Ethernet connection through copper. In order to facilitate the 1 Gbps ethernet communication, we require Ethernet PHY devices. These devices convert the signal from the MDI interface to the MDIO interface and vice versa. The Ethernet PHY device that has been chosen for the purpose is the DP83865 from National Semiconductors which supports tri-speed Ethernet functionality of 10/100/1000 Mbps. It also consumes very low power of about 1.1 Watt and has the auto MDIX capability. The auto MDIX capability implies that, the PHY can identify the Ethernet cable

type and correct the packets going to the RGMII interface. The RGMII is the chosen interface for the media independent interface as the Zynq7020 processing system supports only RGMII. The features of the device have been noted below:

- Supports 10/100/1000 Mbps modes.
- Capable of autonegotiation.
- Capable of auto-MDIX for cable type identification as well as differential pair correction.
- Low power consumption of about 1.1 Watt.

5.2.6 FT4232(FTDI) as USB-UART/JTAG/I2C Bridge

The FT4232 device from FTDI is a four channel USB to Serial Protocol bridge [41]. This device is particularly useful. The four channels of the device can be used for various protocols and hence, provide a very space and cost optimized single debug interface. All the four serials get automtically enumerated when connected to a PC through a USB cable. However, to read or write to the respective serial protocol devices(UART/JTAG/I2C), respective drivers need to be present. Hence, there shall be two UARTs connected to the Zynq PS and PL respectively, one JTAG and one I2C(for temperature monitoring). Hence, we elliminate the need for a bulky connector like the DB9. There are different USB-Serial convertors available in the market. However, the benfits of the FT4232 definitely outweighs the price difference. The comparison is shown in Table 5.2

Table. 5.2: USB-Serial Part Comparison

Device	Manufacturer	Channels	Price
FT232	FTDI	1	4.5 USD
CY7C64225	Cypress Semiconductors	1	2.77 USD
FT2232	FTDI	2	6.5 USD
FT4232	FTDI	4	8.7 USD

5.2.7 TDD Switches

The chosen TDD switches for the deisgn are PE42440(Peregrine) and HMC849LP4CE(Hittite). As we have seen in chapter 2, the IEEE802.22 specifies a time division du-

plex(TDD) system. This means we require switches which can alternate between the transmit and the receive bursts. To accomplish this purpose, we have selected two components which together provide transmit to receive isolation of 90dB. The PE42440 is the final TR switch which has an output 1dB compression point of 41dBm which is apt for our purpose. These switches shall be digitally controlled from the Zynq7020 PL fabric. Together with the RFMD3800, they shall form the RF frontend of the system. Both the devices offer return losses of better than 15dB, when matched well.

5.3 Onboard Digital Interfaces

The White RHINO has many digital as well as Analog data interfaces. Some of them are high-speed which require special care in order to counteract transmission line effects.

5.3.1 High-Speed Digital Interfaces

5.3.1.1 Medium Dependent Interface(MDI)

This is the interface through which the Ethernet packets are transmitted over a long distance through cables(optical or copper). A signal(especially a high-speed one) transmitted over long distances is prone transmission line effects, like insertion and return losses. Hence, this interface is very medium dependent. This property requires us to take special measures to ensure that the signal quality is maintained even over long distances. The MDI interface is a standardized interface under IEEE802.3 [42] and there are specialized devices known as Ethernet PHYs which handle all the medium dependencies including conversion to and from the media independent interface. In this interface, the data is transmitted or received using four pairs of 100 Ohm differential lines which connect to an external cable through an RJ-45 connector.

5.3.1.2 Reduced Gigabit Media Independant Interface(RGMII)

The Ethernet PHY device converts the signal from MDI to a media independent interface. However, currently there are many existing standards for the media independent interface. They are the media independent interface(MII),

gigabit media independent interface(GMII), serial gigabit media independent interface(SGMII), reduced gigabit media independent interface(RGMII) and so on. The Zynq7020 supports only the RGMII interface. The GMII uses 8 bit transmit as well as receive data buses. However, the RGMII uses only 4 bit transmit and receive data buses which is advantageous for our purpose. Lesser bus width implies lesser high-speed routing and hence, space is more effectively utilized. The RGMII uses a 125 MHz clock to achieve the required data rate.

5.3.1.3 Zynq-LMS6002 Digital IO Interface

The Zynq-LMS6002 Digital IO Interface is a critical 12-bit data bus which is responsible for carrying baseband data between the Zynq7020 and the LMS6002 ADC/DACs. The sampling clock can reach a maximum frequency of 40 MHz. The interface is serial IQ interleaved. On the Zynq7020 side, the IO lines shall be connected to the PL fabric banks. The bus includes 12-bit data for each transmit and receive, TX/RX clocks and IQ selects.

5.3.1.4 DDR3 Interface

The DDR3 is a high-speed memory interface. The DDR3 IO lines will be connected to the DDR controller present in the Zynq7020 PS fabric. The DDR3 shall be running with a clock rate of 533 MHz. The data bus width with two 16 bit DDR3 SDRAMs form an effective data bus width of 32 bits. The data bus width along with the clock rate provides us with an achievable throughput shall be more than 16 Gbps. Other high speed lines that constitute the interface are 16 bit address bus, bank select, DQS differential strobes and a differential clock. The signalling levels are compatible with the high-speed Stub-Series Terminated Logic(SSTL) 1.5V family.

5.3.2 Other Digital Interfaces

- **UART:** The Universal Anynchronous Transceiver Receiver(UART) is a slow speed serial communication interface which is mostly used for printing on to the console. This interface is particularly useful during the early bringup stages when hardware bugs are yet to be identified. It works at various datarates(termed as baudrates) like 110, 300, 9600, 19200, 115200 and so on.The two UARTs shall have transmit and receive data lines connecting the FT4232 bridge and the Zynq7200.

- **JTAG:** The Joint Test Action Group(JTAG) is a very popular and powerful debug interface which provides access to the registers of the devices connected in the JTAG boundary chain. In the White RHINO, to keep the JTAG chain simple, only the FT4232 device and the Zynq7020 shall be connected. The JTAG shall be available to the user through the 7-pin JTAG hearder as well as through the USB-JTAG bridge in the form of the FT4232 device. The JTAG interface consists of TCK,TDI,TDO and TMS(Test-clock, data input, data output, mode state respectively). And, it can operate at frequencies like 250 kHz, 500 kHz, 1 MHz, 10 MHz, 40 MHz and so on.

- **QSPI Flash:** QSPI stands for Quad Serial peripheral interface. This interface is particularly used to control a boot flash device from the Zynq7020. The interface has four data lines, a clock and a chip select.

- **Secure Digital(SD) IO interface:** The SD card is an alternative option present on the board to boot the operating system. This interface has been kept because the SD card is portable and the memory is expandable. This adds the flexibility to the booting options on the White RHINO. The SD interface has four data line, a clock, a command signal and a couple of other extra functionlities like write protect and card detect. This interface is connected to the Zynq PS.

- **SPI Interface:** The White RHINO has a Serial Peripheral Interface connected to the Zynq PS. This interface shall be used to configure the LMS6002 device. The interface signals are clock, Master in slave out(MISO), Master out slave in(MOSI), and the Slave enable(SEN).

- **I2C Interface:** There shall be five temperature sensors at various locations on the White RHINO board. These temperature sensors shall provide the board temperature at those locations through the I2C interface. The I2C interface has two interface signals, the serial data(SDA) and the serial clock(SCL). The I2C signals are connected to the PL fabric of the Zynq7020 and the FT4232 device so that the temperature can be monitored on the board as well as through the extermal debug interface.

- **GPS information interface:** As we know that global positioning system(GPS) is required by the IEE802.22 specifications. The GPS data is transferred by the GPS receiver in the form of magnitude and sign. And, the magnitude and the signs are sent out along with a clockout from the GPS receiver. Along with the three above mentioned signals, there is an extra signal which is the data enable signal. The clockout frequency is

about 20 MHz. The GPS information interface signals shall be connected to the PL fabric.

- **RF Control:** In this list of digital signals, the RF control interface is the last but an important one. It is an LVCMOS 3.3V interface which is used to control the TDD switching. The interface is controlled through the PL fabric of the Zynq7020 and is a three bit digital control.

5.4 Some critical design decisions

The LMS6002 is a 300 MHz to 3 GHz transceiver with a maximum instantaneous bandwidth of 28 MHz. However, an RF frontend section comprising of a power amplifier transmitting about 1 Watt of power is usually band limited. Even if the amplifier may support an instantaneous bandwidth of 28 Mhz, it surely cannot have an operational bandwidth of about 3 GHz. So, if we plug such an amplifier in front of the LMS6002 on the same board, we restrict the capability of the LMS6002 device. Even though, the White RHINO is meant to be a strictly TV Whitespace platform, however, there is no noticeable compromise in choosing to split the White RHINO into two separate boards. These boards shall be interfaced with RF and digital connectors. Also, a decision was made after discussion with the project guides that Power Over Ethernet(PoE+) section shall be kept on a different board which shall not be fabricated due to time constraints for design and test. These design decisions of splitting the White RHINO into White RHINO core baseband low power RF board, the White RHINO RF frontend board and the PoE+ board has the following advantages:

- We shall be able to use the White RHINO as a generic SDR platform. This SDR platform can have an operational bandwidth of 300 to 3 GHz with minor lumped component changes.
- The White RHINO RF fronend section remains isolated from the core and hence, we have better control over the RF design which is very critical in terms of performance.
- The thermal performance of the White RHINO with sensitive onboard digital components will be better as the power amplifier contributes to a major share of power dissipation.
- The White RF frontend being a simple board with lesser traces shall not require with more than two PCB layers. Hence, a heat sink can be mounted

on the grounded bottom layer. This in turn, shall contribute towards better thermal performance and hence, better linearity performace of the amplifiers.

- The PoE+ stays as a pluggable module which can be used as and when required. The module can be interfaced with on board headers.

Chapter 6

White RHINO: Schematic Design

In this chapter, we shall discuss the schematic designs of the White RHINO core and the RF boards. The schematics have been drawn in Altium designer. The schematic entry flow has been hierarchical so that is easy to debug and track changes. In order to track the components used for the design, a components database was prepared which contains part numbers, schematic symbols, footprint, manufacturer information and so on.

6.1 White RHINO Core: Subsystems

The White RHINO hardware schematic design has been logically partitioned into various sub-systems. This partitioning has been done keeping the design hierarchy, ease of implementation and error tracking in view. The various subsystems are the Power Supply distribution, the Zynq7020, the DDR3, the Peripherals, the Ethernets and the RF sections. The naming convention is very intuitive and except the subsystem named peripherals, the other names are not very generic. So, just to highlight, the peripherals section includes hardware blocks like the Quad SPI flash interface, the USB-UART/JTAG/I2C interface, the GPS receiver and the temperature sensors. The top level connections shall be explained in the first subsection which is the White RHINO Top Level itself.

6.1.1 White RHINO Top Level

The White RHINO Top Level diagram has been shown in Figure 6.1. The Top Level diagram shows the Zynq7020 subsystems on the left hand side which interfaces with every block on the White RHINO hardware through its dual core ARM processing systems or the programmable logic. Hence, the Zynq7020 forms the central block of the system. The Zynq7020 interfaces with all the other subsystems through high or low speed interfaces. On the right hand side, we can see the Power Distribution subsystem at the very top which provides as well as receives some control signals to and from the Zynq respectively. Then, there is the high-speed DDR3 interface at the very bottom of the diagram. Just below the Power Distribution block, we have the RF block which is connected to the Zynq through various digital control and data signals. Then, there is the Ethernet block comprising of two 1 Gigahertz Ethernet PHYs. They also connect to the Zynq through a high-speed RGMII digital interface and a slow speed control and management interface. Finally, we see the peripherals block in green. As mentioned above, this subsystem features various interfaces like the system debug, flash memory and GPS(required by the IEEE 802.22 for Geolocation).

6.1.2 Power Supply Distribution

The first subsystem that we are going to discuss here is the Power supply distribution subsystem. As the name suggests, this subsystem is responsible for generating all the required power rails for the White RHINO. The power supply distribution is depicted in the form of a block diagram in Figure 6.2. The various power rails required are as follows:

1. Zynq7020 - 1.0V Core, 1.5 V DDR, 1.8V Auxilliary and 3.3V IO.
2. DDR3 - 1.5 V.
3. Ethernet PHY(DP83865) - 1.8 V Core, 2.5 V Analog and 3.3 V IO.
4. LMS6002 1.8 V internal, 3.3 V IO, 1.8 V TXLO and 1.8 V RXLO.
5. FT4232 1.8 V core and 3.3 V IO.

Many of these power supplies requiring same voltage level demand different supplies and hence, the power supply split has been done accordingly. The Power supply chain starts with the 48 V supplied from the PoE+. This votage is then

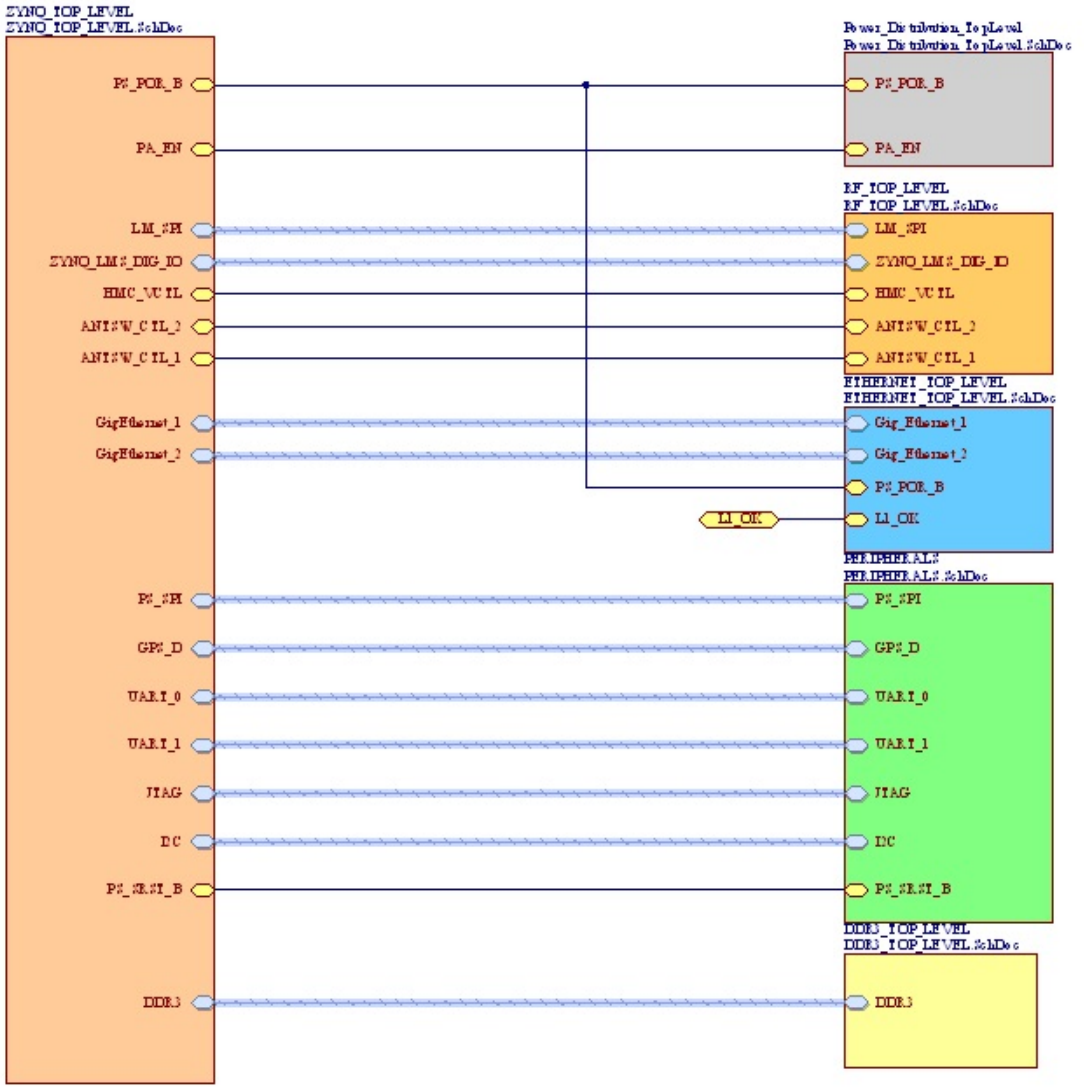

Figure. 6.1: White RHINO: Top Level

down-converted to a 12 V supply. Since, the PoE+ board shall be a different board hence, there is a provision for a 12 V auxilliary supply. The single pull double throw(SPDT) switch shall be used to select the 12 V power source. The 12 V is then downconverted to 5 V which in turn generates all the digital supplies. The RF supplies are generated from a 6 V supply which is generated from the 12 V source. The selection of this supply voltage level has been done on the basis on DC to DC switching regulators readily available in the market. The Power Supply Top Level splits into 11 sheets. Five of these sheets are dedicated to digital power generation, three to RF power, one to Ethernet Analog power

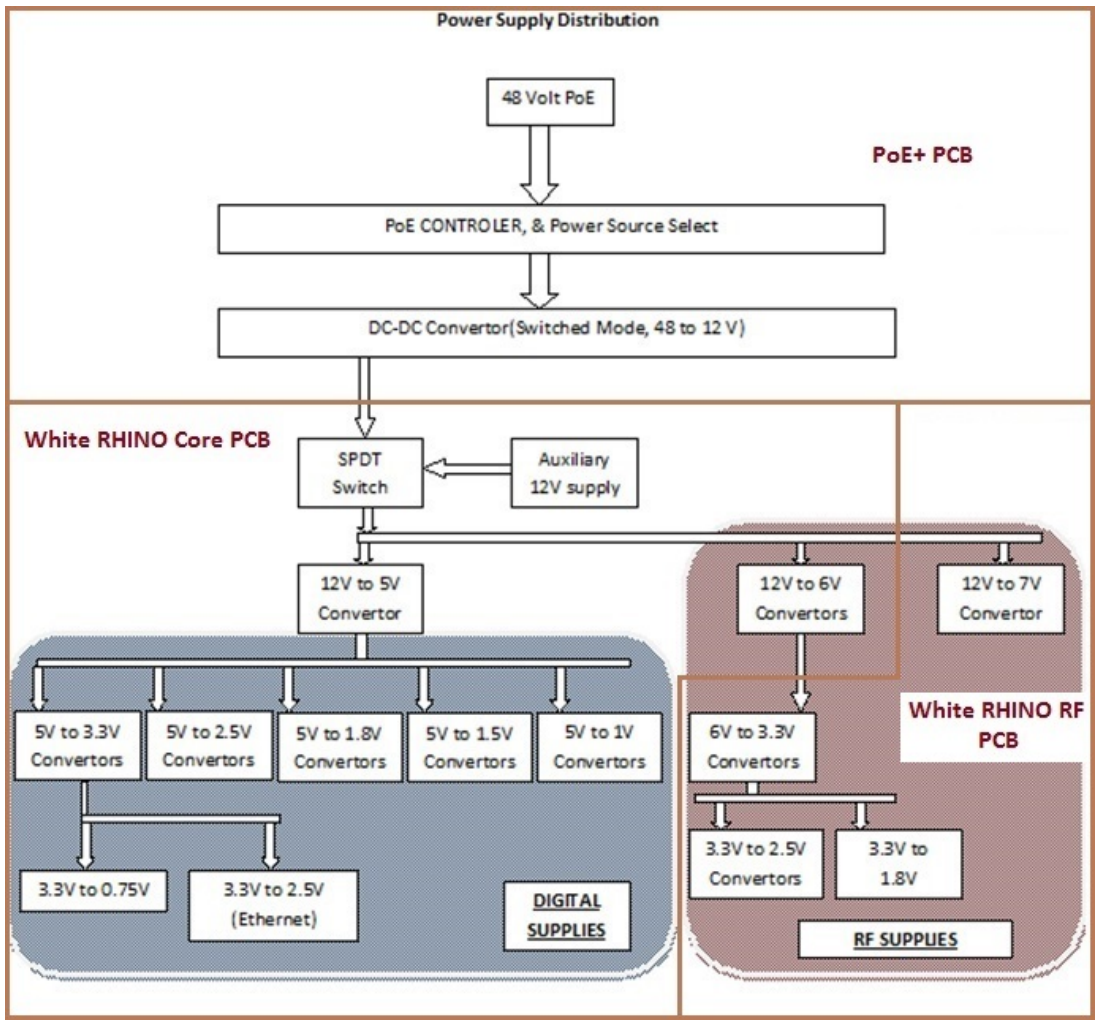

Figure. 6.2: White RHINO: Power Distribution

and the rest for power switch and Shutdown mechanism respectively. The power sequencing for the digital supplies is done through a simple four channel comparator which takes the power good signals from the rest of the digital supplies and generates the power good all signal. This power good all signal in turn generates the power-on-reset signal for the Zynq7020 device shown as an interface signal in Figure 6.1. The various power good signals(in their order of occurance) are as follows:

- **PGOOD_VCC5V0 -** 5.0 V.
- **PGOOD_VCC1V0 -** 1.0 V.

- **PGOOD_1V8 -** 1.8 V Aux
- **PGOOD_DDR -** DDR 1.5 V.

Apart from the power-on-reset signal, there is one more interface signal with the Zynq device. And, that is the PA_EN signal. This is the power amplifier enable signal controlled by the Zynq. This signal shall turn off the power supply to the power amplifier and hence, lessen system power dissipation. Finally, the power consumed by the various devices have been noted in Figure 6.2. As we can observe, the total amount of power consumed by the major devices on the board is 19.5 Watt and the power provided by the PoE+ standard is 25 Watt. Please note that this consumtion chart includes all the major devices present on both the boards. Hence, the White RHINO is capable of getting power up through the PoE+, mentioned as a requirement.

	Current Consumption in the Voltage Domains(A)						
Major Power Consuming Devices	1V	1.5V	1.8V	2.5V	3.3V	6V	7V
Zynq(PS)	0.6	0.25			0.3		
Zynq(PL), Power ON	1.2		0.3		0.05		
Zynq(PL), Average					1.5		
DDR3		0.425					
DDR Term.		0.36					
PHY(DP83865)			0.43	0.19	0.01		
LMS6002D(Typ with WCDMA carrier)			0.1		0.6		
SGA6489						0.075	
RFPA3800							0.8
Total Current(A)	1.8	1.035	0.83	0.19	2.46	0.075	0.8
Total Power(Watt)	1.8	1.5525	1.494	0.475	8.118	0.45	5.6

TOTAL CONSUMPTION(Watt)	19.5
Power Available from PoE+(Watt)	25

Figure. 6.3: Overall Power Consumption

6.1.3 Zynq7020 Top Level

All of the subsystems are connected to the Zynq device. This makes the Zynq subsystem a very important one. The Zynq schematics are partitioned into 9 sheets, Figure 6.4. The first sheet is the Zynq configuration sheet. The next four are the programmble logic banks 13, 33, 34 and 35. Then, there are two processing systems banks(500 and 501) and the DDR bank. And finally, there is the Zynq power sheet. The interfaces connected to the various banks are as follows:

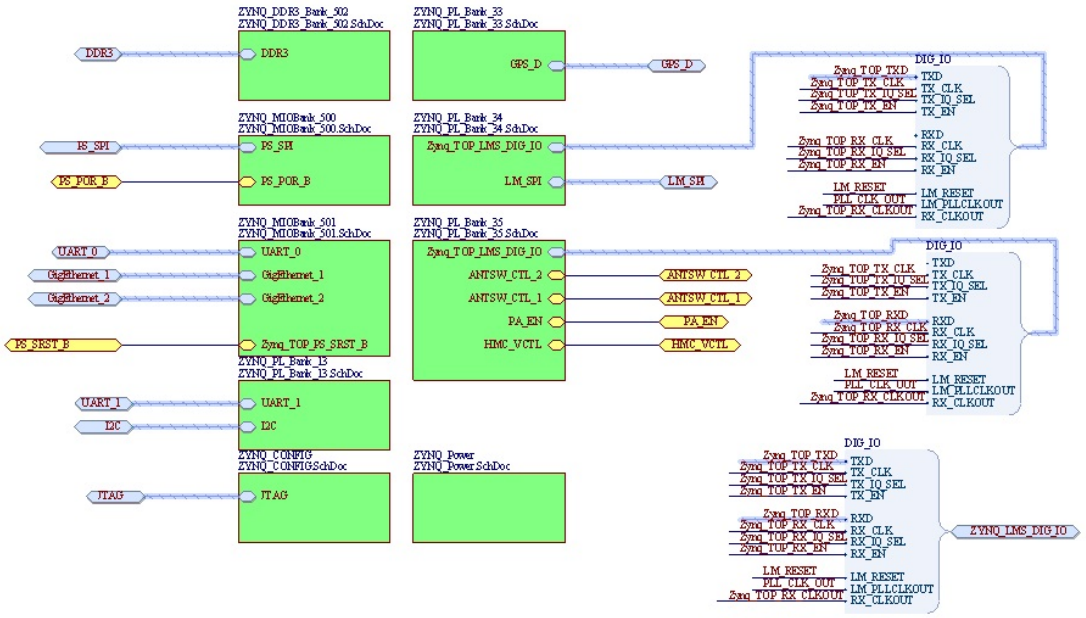

Figure. 6.4: White RHINO: Zynq Top Level

- **Config -** JTAG.
- **PL Bank 13 -** UART and I2C.
- **PL Bank 33 -** GPS and PMOD(Auxilliary peripheral).
- **PL Bank 34 -** LMS6002 ADC interface(13 bit LVCMOS + 3bit clock and control) and a user LED.
- **PL Bank 35 -** LMS6002 DAC interface(13 bit LVCMOS + 3bit clock and control), LMS6002 Reset, RF frontend control and a user LED.
- **PS Bank 500 -** QSPI Flash, LMS6002 SPI, power-on-reset, 3 user LEDs and bootmode select.
- **PS Bank 501 -** UART, 2 RGMII Ethernet interfaces and SDIO
- **PS Bank 502 -** DDR interface

All of these interfaces have been discussed in the previous chapter. However, it is worth mentioning at this point that all the peripheral controllers on the processing system are memory mapped. So, apart from the non-standard interfaces

like the LMS6002 digital IO and the GPS, usage of the rest of the interfaces is to a great extent, simplified. Here in, lies the utility of the Zynq device which makes it a very powerful for systems requiring heterogeneous architecures.

6.1.4 DDR3 Top Level

The dual 256 MBs of DDR3 memory ICs are connected to the DDR bank of the Zynq device. Both the devices share 14 bit address lines, bank address and other control lines. The 16 bit data buses of each of the DDR3 SDRAMs together form the 32 bit data bus of the Zynq DDR3 bank. The DDR3 interface is a the high-speed SSTL 1.5 V logic family interface and the DDR3 ICs can operate at the maximum clock frequency of 1 GHz. Hence, this requires impedance matching and termination resistors. However, the termination resistors are placed only on the address, bank address, control line and the differential clocks. There are no termination resistors for the data bus. The signal integrity of the data bus is taken care by the ODT(On Die Termination) present in the DDR3 devices. The data bus requires this special technology because they are bidirectional and hence, static termination does not always provide best signal integrity. And, this is because the driver and the receivers have different input or output impedances respectively. Hence, a configuration of read and write termination resistances are selected which provide optimal signal integrity.

6.1.5 Peripherals Top Level

There are four schematic sheets dedicated to peripherals. These peripherals are the Quad SPI flash(which shall be used as boot flash), the debug interface(with USB-UART/JTAG/I2C bridge), the GPS receiver and the I2C temperature sensors. The top level schematic sheet of the peripherals has been shown in Figure 6.5.

6.1.5.1 Quad SPI Flash

This schematic sheet consists of the 128 MBit(16 MB) flash device and the harness which connects this device to the Zynq PS bank 500. The device is powered by a 3.3 V power supply. The digital interface consists of a clock, chip select and four data lines. The programming data rate is 1.5 M Bytes per second.

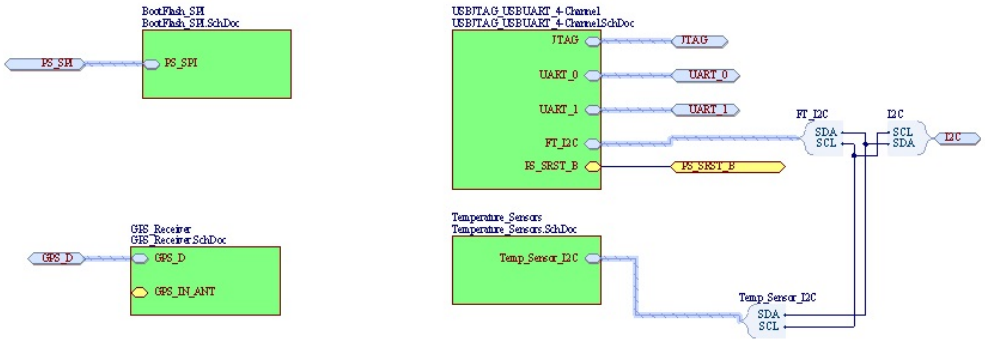

Figure. 6.5: White RHINO: Peripheral Top Level

6.1.5.2 GPS Receiver

The White RHINO receives a GPS signal centered at 1575.42 MHz through an onboard SMA connector which shall be connected to an external antenna. This GPS signal is taken by the Skyworks SE4110L device which directly downconverts and demodulates the BPSK signal. After the signal processing, the GPS information is provided in the form of magnitude and sign. The harness to the the Zynq PL bank 33 contains the mag, sign, the clock and the data enable signals. On the RF side, there is a matching circuitry which has been drawn using the datacheet recommendations. The GPS receiver requires two 3.3 V supplies, one RF and the other, digital.

6.1.5.3 USB-UART/JTAG/I2C

The host PC can get access to the debug interface through the micro USB port. There are ESD diodes for the circuit protection. The USB signal is taken to the FT4232 through 90 ohm differential traces. This signal is then converted by the FT4232 into the corresponding protocols and made available at the channels A to D. The channels A and B are dedicated to JTAG and I2C respectively and the channels C and D are dedicated to the PS and the PL UARTs respectively. Both I2C and the JTAG go through signal buffers to increase the drive strength of the signals. Also, there is an EEPROM connected to the FT4232 device which stores configuration information for the device. The EEPROM has 2K Bits memory and is connected to the FT4232 device through a 3-wire serial IO interface consisting of clock, chip select and data. Finally, the clock is supplied

to the FT4232 through a 75 MHz crystal.

6.1.5.4 Temperature Sensors

The temperature sensors shall be placed at various critical locations on the board. The locations shall be discussed more in the PCB design chapter. These temperature sensors are powered by 3.3 V and connected to the I2C bus. There are three of them on the White RHINO board and couple more of them will be present on the RF board.

6.1.6 Ethernet Top Level

The Ethernet schematic contains six sheets. Three are dedicated to each of the two Ethernets. These are the main ethernet sheet consisting of the all major connections to and from the Ethernet PHY, an MDIO sheet which shows the connections between the MDIO pins of the Ethernet PHY and the RJ-45 connectors and the Ethernet PHY power sheet which contains the various power supply connections and decoupling capacitors. The Ethernet Top Level is shown in Figure 6.6.

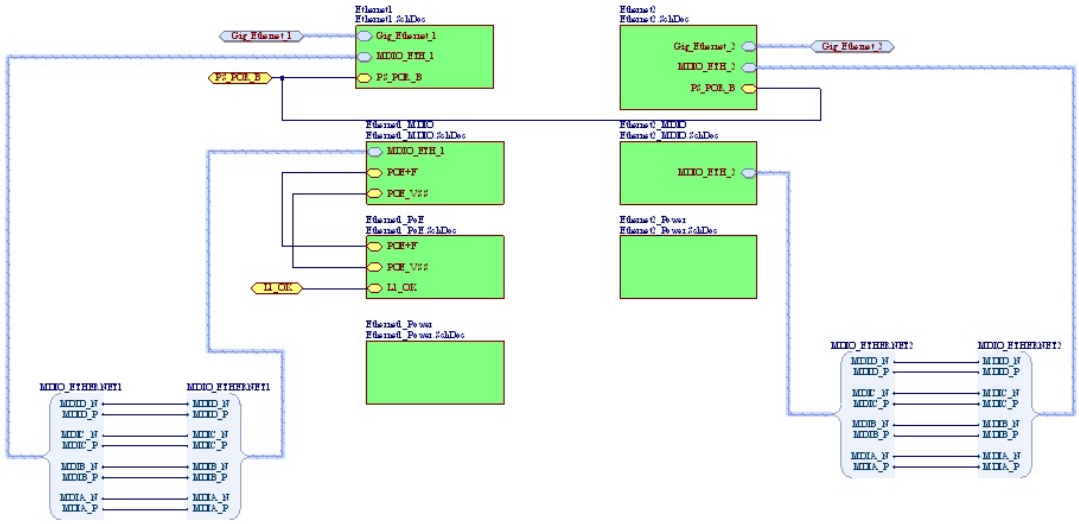

Figure. 6.6: White RHINO: Ethernet Top Level

Now, the RGMII interface between the Zynq and the DP83865 is a 12-bit interface as shown in Figure 6.7. The figure also shows the management interface bus which shall be used to configure the ethernet PHY chip. Since, DP83865 supports multi-protocol media independent interfaces(MII,GMII,RGMII-3COM,RGMII-HP), there are two jumpers dedicated for the mode select of the media independent interface. The DP83865 receives a 25 MHz clock from a crystal. The transmit and the recieve clocks are obtained and then reconstructed from the Ethernet hosts. In case of the 1 gbps mode, this shall be a 125 MHz clock signal. Now, the data in the media dependent interface(MDIO) is analog data which is carried through four pairs of 100 Ohm difeerential traces onto the RJ-45 connector. However, the Ethernet1 schematic also includes an isolation transformer in between which shall provides access to the 48 V PoE+ through its center taps. These power lines are then carried over to a separate header which shall interface with a PoE+ board. The device receives the reset from the same power-on-reset signal from the power distribution schematics through a schematic port.

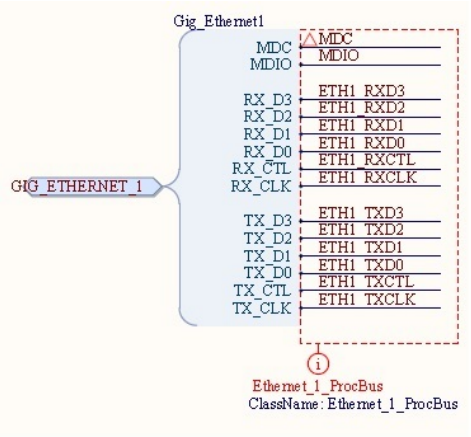

Figure. 6.7: Ethernet: RGMII Harness and Management bus

6.1.7 RF Top Level

The low power RF subsystem on the White RHINO consists of the LMS6002(with its digital and RF interfaces) and the transmit and the receive baluns(which convert differential transmission lines to the single ended 50 Ohm transmission lines). The RF top level is shown in Figure 6.8. The RF top level comprises of the LMS6002 top level, the transmit and the receive sections. Then, LMS6002

top level consists of the LMS6002 main sheet, the PLL clocks sheet and the LMS6002 power sheet.

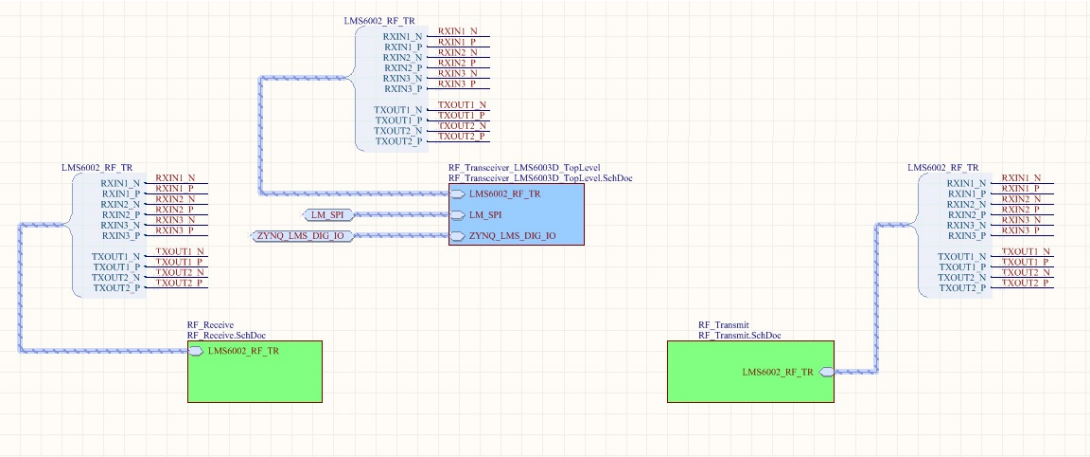

Figure. 6.8: White RHINO: RF Top Level

The LMS6002 power sheet contains all the various power supplies required for powering up the LMS6002 and the decoupling capacitors. The various power supplies required for the LMS6002 are as follows:

- **Digital core supply for ADC and DACs -** 1.8 V
- **Analog supply for DAC -** 3.3 V
- **Analog supply for ADC -** 1.8 V
- **TX LO supply -** 1.8 V
- **RX LO supply -** 1.8 V

The LMS6002 PLL clocks sheet consists of the 40 MHz temperature controlled crystal oscillator(TCXO). There is also a level convertor which converts the 2.8 V signal to a 3.3 V signal. Finally, the main LMS6002 sheet consists of all the interfaces(digital, analog and control) apart from the lumped PLL loop filters. The Digital IO lines have 22 Ohm series terminations to improve signal integrity. The two RF outputs used have 65 Ohm(for transmit output) and 50 Ohms(for receive input) differential traces. These traces connect to the RF transmit and the receive sheet through the RF harness.

The RF transmit sheet consists of a lummped 65 Ohm to 100 Ohm lumped filter and then a discrete transformer which converts the signal from 100 Ohm differential to 50 Ohm single ended signal. This 50 Ohm signal is then launched on to the SMA connector so that it can be taken to the RF board where this signal shall be amplified. The amplitude and phase imbalance of the 65 Ohm to 100 Ohm lumped balun can be observed inFigures 6.9 and 6.10. We require a balun that transforms from unbalanced to unbalanced configuration to ideally result in zero amplitude shift and 180 degrees of phase shift. As we can observe from the plots, our lumped filter achieves very good performance in the Genesys simulated environment. The amplitude imbalance over 500 MHz to 700 MHz is negligible and the phase imbalance is less than 0.5 degrees. In the RF receive

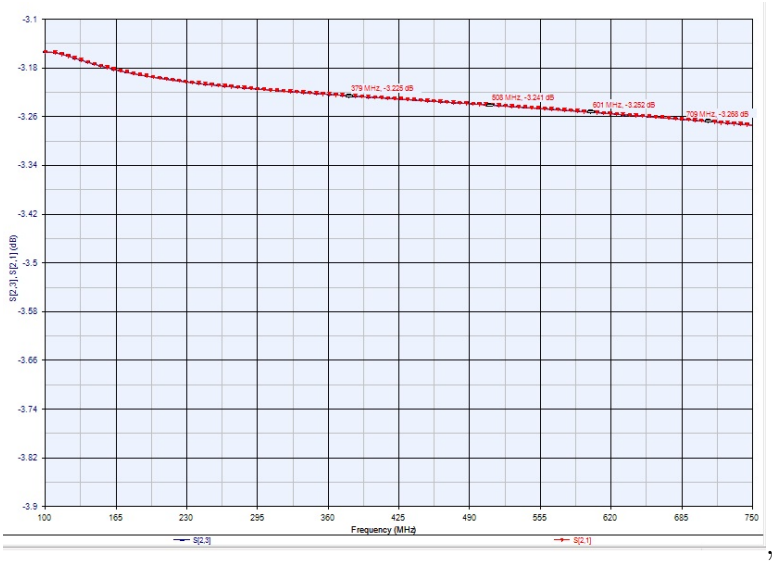

Figure. 6.9: Transmit Lumped Balun(65 Ohm to 100 Ohm balanced): Amplitude Imbalance. The S21 and S23 potray the through response(Amplitude) between 32.5 Ohm unbalanced ports and 100 Ohm balanced port. Here, port 1 and port 3 are 32.5 Ohm port and the port 2 is the 100 Ohm port.

sheet, there is a discrete transformer B0322J5050 from Anaren which converts the 50 Ohm unbalanced input from the antenna port to 50 Ohm balanced signal required by the LMS6002. Now, that we have discussed the White RHINO schematics, we shall now explore the White RHINO RF schematic design.

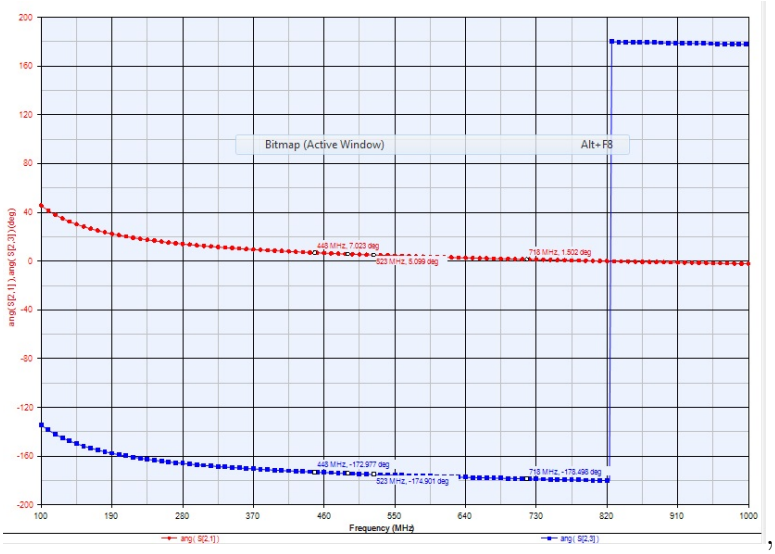

Figure. 6.10: Transmit Lumped Balun(65 Ohm to 100 Ohm balanced): Phase Imbalance. The S21 and S23 potray the through response(Phase) between 32.5 Ohm unbalanced ports and 100 Ohm balanced port. Here, port 1 and port 3 are 32.5 Ohm port and the port 2 is the 100 Ohm port.

6.2 White RHINO RF: Subsystems

The White RHINO RF is a small board which shall consist of the transmit power amplifier and the TDD switch in the signal path. The board shall also house a power distribution section which will generate all the power supplies required for the onboard devices. As we can observe from Figure 6.11, the White RHINO RF consists of a signal header which interfaces this board with the core board.The White RHINO RF schematics consist of the transmit and receive sheets, the Antenna switch sheet, the power distribution sheets and finally the sheet containing the onboard I2C temperature sensors for monitoring system performance. The signal header provides the following signals from the White RHINO board(apart from 6 V supply and ground):

- ANTSW_CTL_1 and ANTSW_CTL_2 for controlling the Antenna switch Peregrine PE42440 [43].
- HMC_VCTL for controlling the Receive switch Hitite HMC849LP4CE [44].
- PA_EN for enabling and disabling the power supply to the final stage amplifier, RFPA3800 [36].

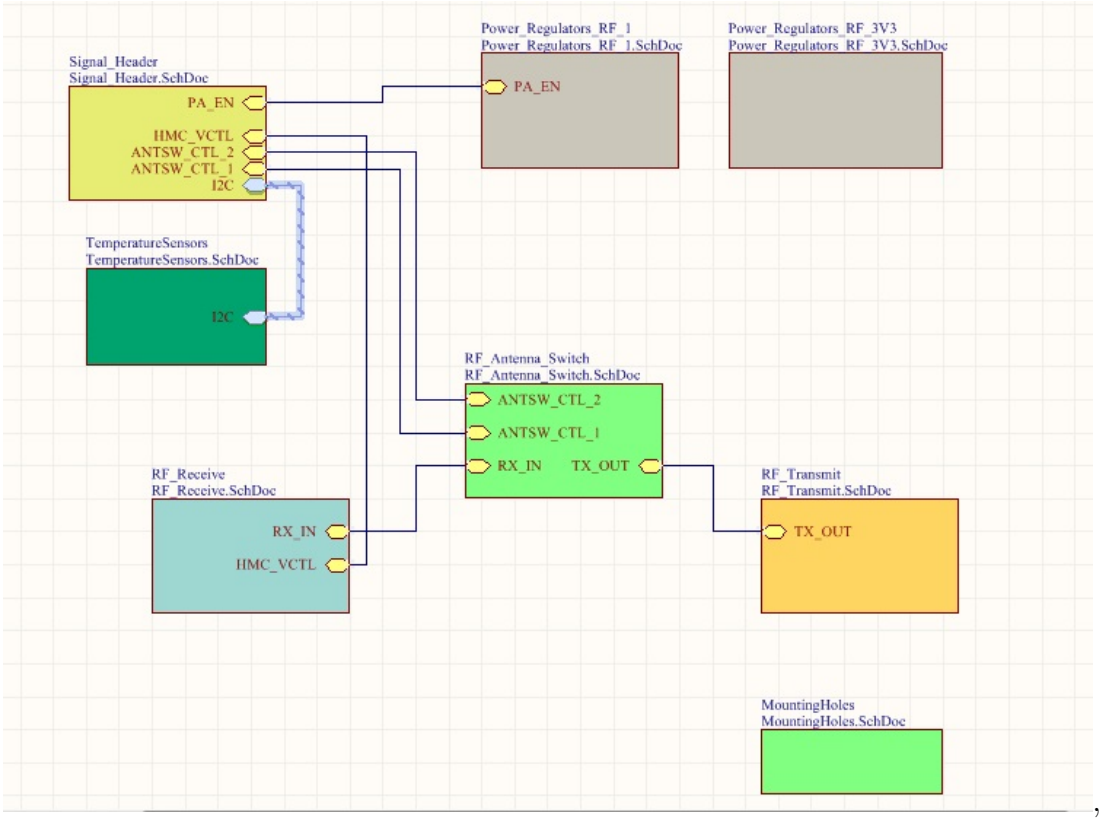

Figure. 6.11: White RHINO RF: Top Level

- I2C signals of SDA and SCL.

6.2.1 Power supply Distribution

This board requires three power supplies. The main power amplifier RFPA3800 requires 7 V, the pre-amplifier SGA6489 requires 6 V and the switches require 3.3 V. Now, the signal header provides the 6 V supply from the White RHINO which inturn is used to generate the 3.3 V supply. The 7 V supply is generated from a 12 V supply which again is the main power supply for the White RHINO board. The 7 V regulator LT1376CS8PBF is enabled and disabled using the PA_EN signal.

6.2.2 RF Transmit Chain

The RF transmit chain has been shown in Figure 6.12. As it can be observed, the transmit block provides about 35 dB gain to the signal from the White RHINO which is less than 6 dBm. Both the amplifiers operate at class A region to achieve maximum linearity. The amplifiers have 220 pF dc block capacitors. The drain feed and the input and the output matching circuits have been implemented using datasheet guidelines and after discussions with the component vendor. Genesys simulations have been done with the S2P(2 port S-parameter) files for the SGA6489 and the RFPA3800 device. The simulation schematic is shown in Figure 6.13. Now, in Figure 6.14, there are two sets of plots. One tagged as original are the values of components L4, L5 and L6 which have been recommended by the manufacturer. We also see that by changing their values, we obtain a more wide band response of the amplifier block. However, even though the simulations show us a trend that the frequency response can be made more wideband, on the schematics, the values of the inductors used are same as the ones suggested by the vendor [36, 45]. And the reason for that is the fact that, performance on the PCB may vary with the simulated plots and that is because:

- Simulations do not incorporate parameters like transmission line and drain feed mismatch effects.
- S2P files do not provide a complete picture of the amplifier since, they are small signal response files.

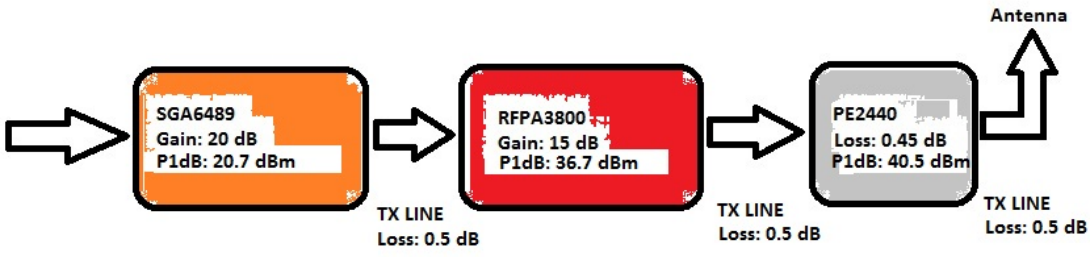

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Figure. 6.12: White RHINO RF: Transmit Linup

6.2.3 RF Receive and Antenna Switches

There are two RF high power switches which together provide enough isolation between the transmit and the receive chains for the TDD application.These

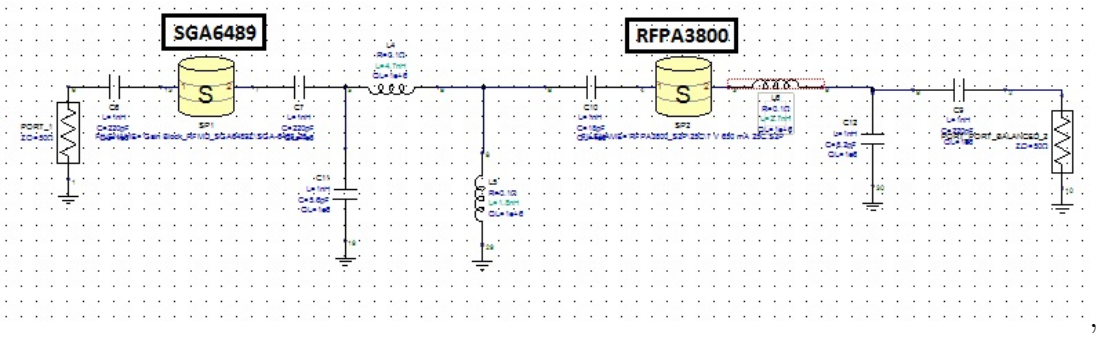

Figure. 6.13: White RHINO RF: Amplifier Block Simulation Schematic

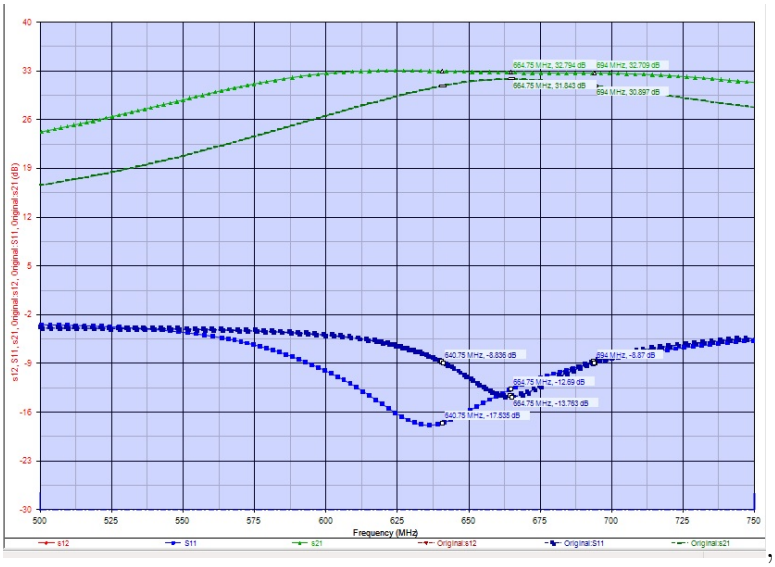

Figure. 6.14: White RHINO RF: Amplifier Block Simulation Plots. The plots show the gain(S21) and return losses(S11) of the original configuration of indutors and final configuration of inductors. Original values(L4 - 1.2nH, L5 - 1.2nH, L6 - 1.8nH) and Final values(L4 - 4.7nH, L5 - 1.8nH, L6 - 2.7nH).

switches are Hittite HMC849LP4CE and Peregrine PE42440. The Hittie switch has a one bit 3.3 V control and the Peregrine switch has a 2 bit 3.3 V control. The Peregrine switch is a 4-channel and hence, requires 2 bit control. However, we shall be using only two of its channels [43, 44]. These vendors have also provided S2P files and we performed Genesys simulations. The performance of the receive linup have been plotted in Figure 6.15. As it can be clearly observed from the plot the forward path losses are less than 2.5 dB, and the return loses are better than -12 dB and the transmit-receive isolation is better than 96 dB over the whole 500-700 MHz band.

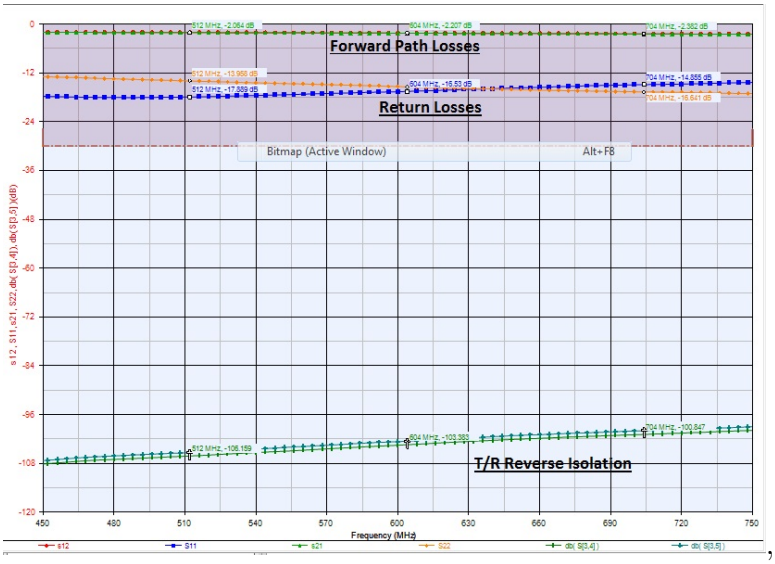

Figure. 6.15: White RHINO RF: Receive Linup Simulations.

6.2.4 Temperature Sensors

Finally, there are two temperature sensors on the RF board. One of them shall be used to monitor the transmit chain temperature and the other one for the receive chain temperature. These temeperature sensors shall facilitate constant monitoring of the board and thus allow calibration routines to function effectively.

6.3 Overall RF linup

For the ease of parameter tracking, all the The RF paramters of the White RHINO design have been tabulated in Table 6.1. While the gain control range is a paramter of the LMS6002, the amplifier gain and the P1dB emerge from the White RHINO RF transmit section as we have seen in the previous section. The balun amplitude and phase imbalance are internal parameters but they directly affect the error vector magnitude(EVM) and hence, the bit error of the transmitted ro the received data. Even though simulations provide better values than these, most of these paramters have been noted keeping the board tolerances in view.

Table. 6.1: Overall RF parameters

S.No	Parameter	Value
1	Transmit P1dB	36.7 dBm
2	Amplifier gain	Over 30 dB
3	Transmit Gain Control Range	56 dB
4	Receive gain control range	61 dB
5	T/R isolation	Over 90 dB
6	Transmit Balun: Amplitude imbalance	Less than 1 dB
7	Transmit Balun: Phase imbalance	Less than 5 degrees
8	Receive Balun: Amplitude imbalance	Less than 1 dB
9	Receive Balun: Phase imbalance	Less than 5 degrees

6.4 Chapter Summary

In this chapter, we discussed the schematic design of the White RHINO and the White RHINO RF board. We also discussed how we divided the design into various subsystems for the ease of tracking changes and debugging. Then, we discussed all the top levels of both the boards. Finally, we provided simulation plots for the various RF design sections and provided RF linup parameters. Now, in the next chapter we shall discuss the printed circuit board design of the White RHINO and the White RHINO RF boards.

Chapter 7

White RHINO: PCB Design

So far, we have discussed the hardware architecture of the White RHINO and the schematic design. The third and very important part of the system design process in the PCB design. PCB desgn includes placing the physical footprints of the components(unlike the schematic symbols which just have the pin mapping) on the PCB design file and then doing the actual routing of the nets. Historically, PCB designers had to draw the traces manually on the copper board which were then etched to form the printed circuit board. Nowadays, we use CAD tools to aid us with that process because the traces have to be very thin, the components have to be placed very close and its a multi-layer design which cannot be done without the CAD and CAM tools. We shall now discuss the design of the White RHINO and the White RHINO RF PCBs separately. We shall also discuss how both required very different approaches.

7.1 White RHINO Core

In this section we shall discuss the PCB design of the White RHINO core board. This shall include design aspects such as component placement, PCB stackup, design rules, design of split power planes, signal integrity simulations and so on. We shall also highlight various design decisions that were taken to reduce the cost of the board. PCB design parameters such as the board size, number of layers and so on play a pivotal role in deciding the cost of the product. We shall also discuss how the design decisions do not significantly affect the performance of the system.

7.1.1 Component placement

The first step during a PCB design is the placement of major ICs and the space consuming connectors. In our design the major components are as follows:

- Zynq7020
- Two DDR3 ICs
- The QSPI flash device
- FT4232 device
- Two Ethernet PHYs
- LMS602 device
- GPS receiver
- Power supply devices

And, the major connectors are as follows:

- Two RJ-45 connectors
- Micro USB connectors
- SD Card connector
- 12 V Power Jack
- SPDT Power Switch
- JTAG header
- Three SMA connectors

These components together with the connectors are most critical and space consuming. Now, the placement has to be done keeping the following constraints in view:

- Minimum trace crossovers
- Minimum trace length

The above constraints play a major role in the signal integrity as well the price of the PCB. Minimum crossovers ensure that the number of PCB layers are minimum and hence, optimize the price of the board. Mimimum trace length provides better signal integrity of the traces and hence, better performance and reliability can be achieved from the system. Keeping all the contraints in view, we placed the major components on a 121 mm x 121 mm form factor PC board. This has been shown in Figure 7.1.

In the figure, the boxes painted with black are the ICs and the ones painted with

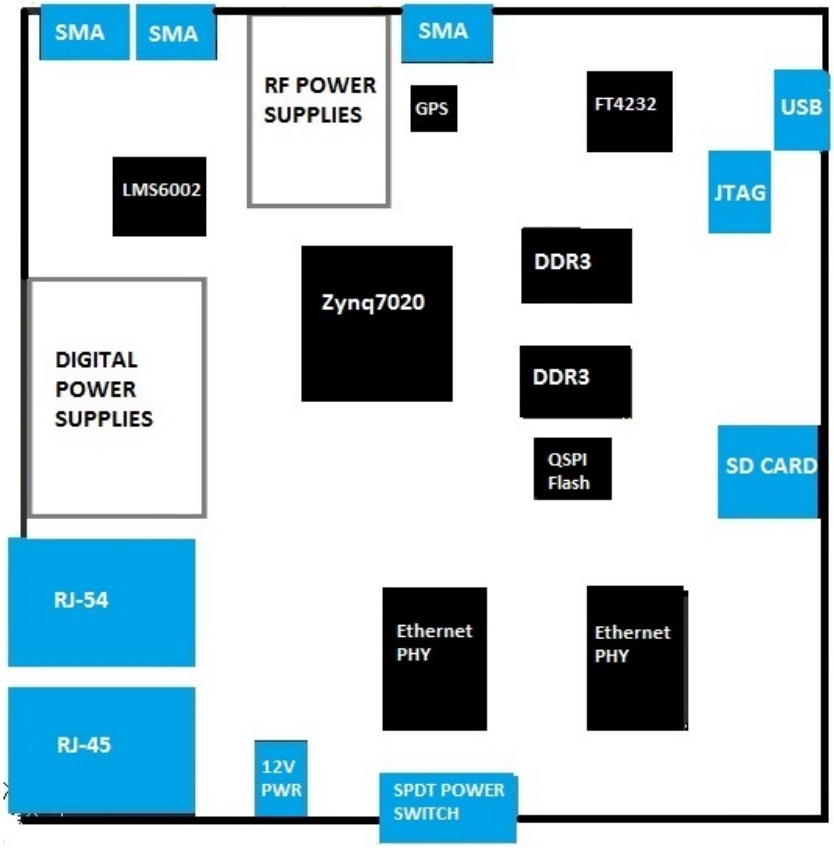

Figure. 7.1: Placement of major components

blues are the various connectors. There are also two regions enclosed with gray boxes. These depict the power distribution sections. The DDR3 ICs have been placed to the right of the Zynq device because the Zynq DDR3 interface pins lie on the left side of the device. Simmilarly, the two ethernet PHYs are placed to the south of the Zynq device because the ethernet pins are present towards

the south of the IC. Finally, the RF trasceiver LMS6002 is placed at the top left hand corner for the following reasons. Firstly, the whole RF section is kept at a corner to minimize interaction with the digital traces. And secondly, the Zynq-LMS Digital IO pins lie on the left hand side of the Zynq device. So, these are some of the logical decisions that were taken while placing the components.

Now, the connectors have been placed close to the corresponding devices and at the same time they had to be kept on the edge of the board. And, so we observe that two RF SMA connectors are placed on the board edge close to the LMS6002 device. The micro USB connnector is placed next to the FT4232 device on the top right edge of the board. The RJ-45 connectors could not be placed very close to the Ethernet PHY devices because they had to be kept at the board edge. This justified the placement of those connectors at the location on the bottom left corner of the board.

7.1.2 PCB Stackup

The next task is to define the PCB stackup. the White RHINO PCB stackup has a few very prominent features which has led to low layer count and hence, reduction in cost of manufacturing of the board. These features are:

- Two signal layers between planes: Even though it is highly reccomended to have single striplines sandwiched between ground planes, we decided to go for two assymmetric striplines sandwiched between planes. This deviation from standard design technique does not lead to significant loss of signal integrity as we shall observe from our signal integrity simulations.
- Coupling of signal layers with power planes: Even though, best parctices includes keeping the striplines between ground planes, we decided to couple them with corresponding power planes wherever possible. This again has been done to reduce layer count.
- Split Power planes: As we have seen in the previous chapter, the design has many power supplies and dedicating a plane to each supply would have contributed to an immense increase in the cost of PCB fabrication. Hence, the planes have been split to accomodate many power split planes on a single layer of the PCB.

The White RHINO stackup is shown in Figure 7.2. There are twelve layers comprising of 7 signal layers, 3 ground planes and 2 power planes. The total height of

the PCB is 1.43 mm. In Figure 7.3, we can observe the various critical nets of the interfaces and their charecteristic impedances. The DDR3 interface consists of single-ended address, data and bank select lines whose charecteristic impedance is 50 Ohms. The differential nets of the DDR3 interface are the clocks and the DQS nets. The Ethernet too has both single ended and differential nets. The singled-ended nets are the RGMII interface signal and the 100 Ohm differential nets are the analog MDIO interface nets. These nets are launched on to the four pairs of the RJ-45 connector. Now, the USB nets of the USB-UART/JTAG/I2C interface are 90 Ohm differential. Finally, the RF transmit and receive nets are 65 Ohm and 50 Ohm differential which are converted from and to the standard 50 Ohm RF traces by the balanced-unbalanced baluns respectively. We have noted the performance of these baluns in the previous chapter.

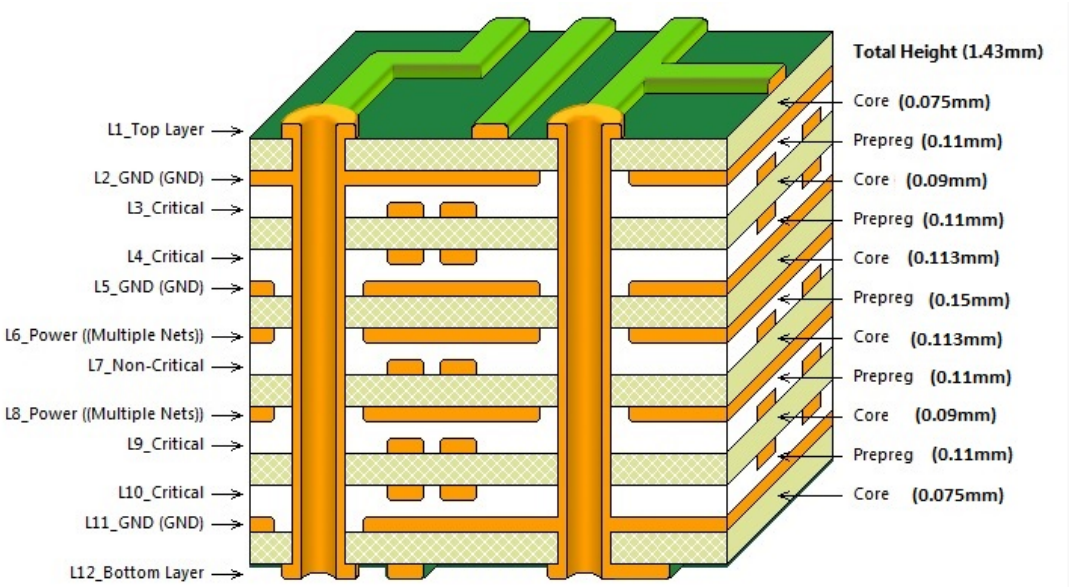

Figure. 7.2: PCB Stackup

	DDR3	Ethernet	USB	LMS6002(RXIN1)	LMS6002(TXOUT1)	RF IN/OUT
Single Ended(Ohm) Zo	50	50		-	-	50
Differential(Ohm) Zo	100	100	90	50	65	-

Figure. 7.3: Critical Nets and their Characteristic Impedances

7.1.3 PCB rules

Finally, before actual routing of the traces, PCB rules must be defined. These rules ensure the following:

- Signal integrity is maintained.
- The design paramters meet manufacturer specifications so that there are no unexpected escalation of cost.
- Component legends are distinct and readable.

Now, we shall discuss some of the critical rules of the White RHINO PCB design.

7.1.3.1 Minimum Trace Width

The minimum trace width has been defined as 0.1 mm(4 mils) or wider. For traces thinner than 0.1 mm, the fabrication costs are very high. Most of the impedance controlled traces have widths wider than 0.1 mm and the trace width of those traces have to be maintained within 10% tolerance.

7.1.3.2 Minimum copper to copper clearance

There are high-speed as well as slow-speed traces on the board. While the high-speed traces are very prone to cross-talk effects, the slow speed traces are not. Hence, there are two sets of minimum copper to copper clearance values. The slow-speed nets have a clearance of 0.1 mm so that routing can be optimised and hence, the board space can utilized effectively. The high-speed nets have a copper to copper clearance of 0.2 mm. This value has been chosen because the high-speed traces couple to ground planes which are less than or equal to 0.15 mm away from those traces.

7.1.3.3 Length Matching

Length matching is a very important aspect of high-speed routing. Just to provide an example, the DDR3 has 32 data lines. Now, the if the data on all these lines arrive at different times then, the data has to be internally synchronized. Even though, the devices and their software drivers perform delay

related synchronization, the tolerance of the synschronization routines are also very marginal. Hence, it reccomended by the device manufacturers to minimize the skew. This is implemented on the hardware by matching the trace lengths using curly matching elements as shown in Figure 7.4. The matched length tolerance of all the DDR3 traces is 1 mm. The matched length tolerance of other high-speed traces mentioned in Figure 7.3 is 2 mm.

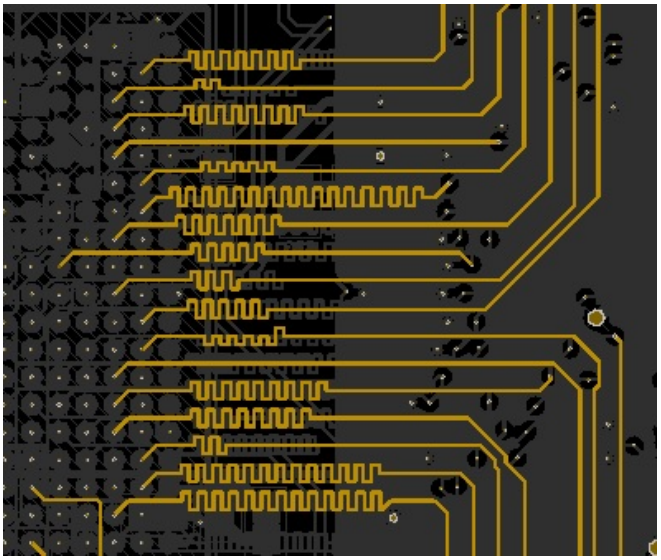

Figure. 7.4: Length Matching

7.1.3.4 Width of the Power Nets

The power nets carry the power from the power supply ICs to the respective ICs(Power Supply/Digital/RF IC). The traces are made of copper and hence are resistive. Now, if the trace resistance lead to a potential drop of more than the tolerance value of the device receiving the power, then it will not function as desired. Hence, it is important that the widths of the power supply traces are designed carefully. In Figure 7.5, we estimate the voltage drops across the various power supply traces at 60 degrees of board temperature. The voltage drops have been calculated with approximate value of trace lengths. Finally, the widths of the supply traces are taken in the way so that, the voltage does not drop beyond a particular level. Now, this figure has been taken as a guideline to route the various power supply traces. We should however note that in most cases, the maximum length is never reached because of the presense of the power planes.

Voltage Specific Parameters									
Voltages	12	7	6	5	3.3	2.5	1.8	1.5	1
Max Current Supplied(A)	2.1	0.8	1.5	3	3	0.2	0.83	1.035	1.8
Max Trace length(cm)	5	3	3	2	2	2	2	5	1
Max Trace length(m)	0.05	0.03	0.03	0.02	0.02	0.02	0.02	0.05	0.01
Trace Width(mm)	0.8	0.4	0.5	0.5	1	0.15	0.28	1	0.3
Trace Width(m)	0.0008	0.0004	0.0005	0.0005	0.001	0.00015	0.00028	0.001	0.0003
Trace Resistance(Ohm)	0.08092	0.097104	0.077683	0.051789	0.025894	0.172629	0.09248	0.064736	0.043157
Voltage Drop(V)	0.169932	0.077683	0.116525	0.155366	0.077683	0.034526	0.076758	0.067002	0.077683
Worst Case Voltage(V)	11.830	6.922	5.883	4.845	3.222	2.465	1.723	1.433	0.922
Percentage Dropped	1.416	1.110	1.942	3.107	2.354	1.381	4.264	4.467	7.768

Figure. 7.5: Power trace widths

7.1.4 Power planes

The power planes of the White RHINO PCB have been shown in Figures 7.6 and 7.7. The split power floods have been designed in a way so that they lie below or above only the corresponding nets and hence, provide a return path to those signals. Also, these power floods have been designed in a way such that the power trace lengths are minimized.

7.1.5 Signal Integrity Simulations

As we have observed in the previous sections, the White RHINO consists of many non-traditional PCB design aspects. Hence, its very important to perform signal integrity simulations to verify the high speed traces. We used Altium's signal integrity tool to verify the design. In Figures 7.8, 7.10 and 7.12, we have plotted the DDR3 single-ended clock, address and data lines. The trigger is a 2 ns pulse. And then, in Figures 7.9, 7.11 and 7.13 we have plotted them after triggering with a 1 ns pulse. The maximum allowed overshoot for the SSTL 1.5 V DDR3 interface is 0.4 V which makes the maximum overshoot voltage equal to 1.9 V. Simmilarly, maximum allowed undershoot is again equal to 0.4 V which makes the minimum voltage equal to -0.4 V [40]. The DDR3 data lines have be simulated with 40 Ohm driver impedance of Zynq7020 and 60 Ohm On-Die-Termination(ODT). Now, from all the DDR3 plots, we can draw the following inferences:

- The overshoots and the undershoots are within acceptable limits.

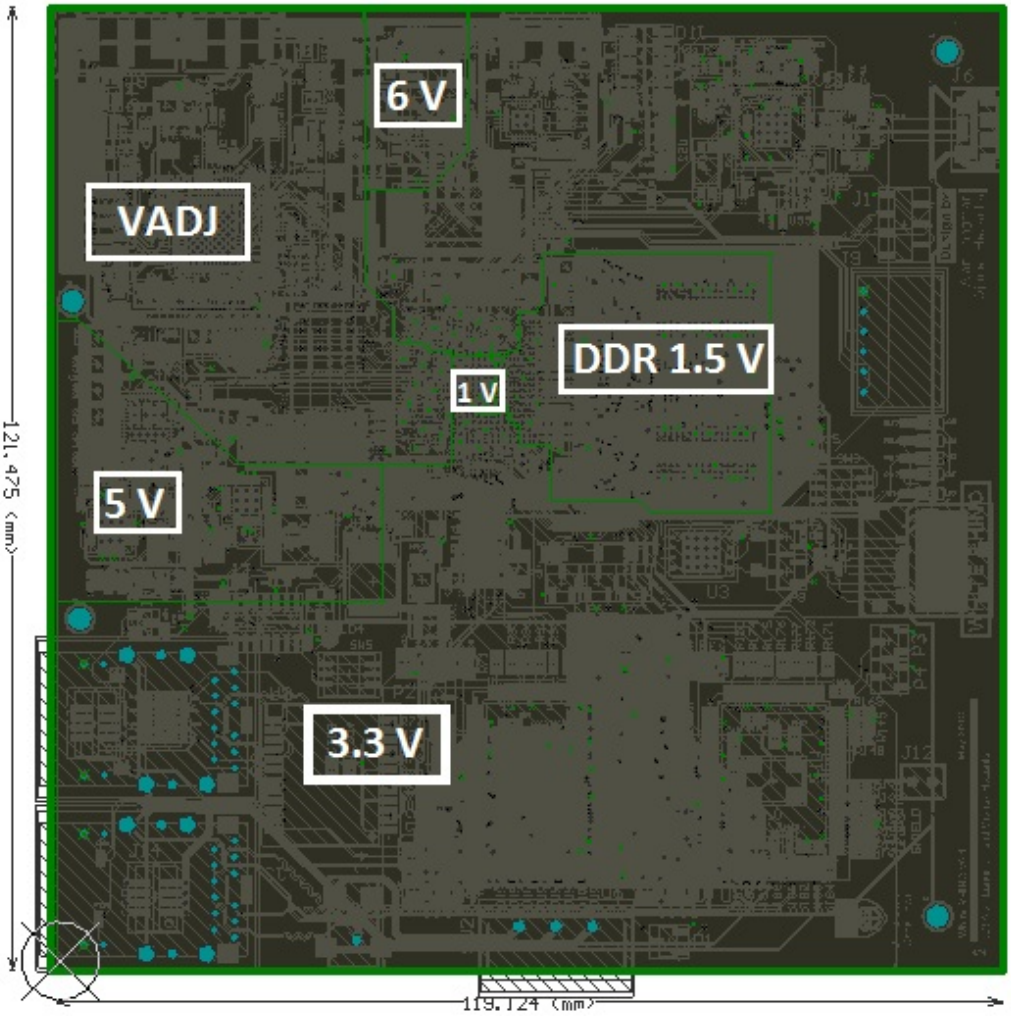

Figure. 7.6: Power Plane - I

- Even though the quality of the signals degrade when the trigger pulse is 1ns, there are no observable metastable regions which can lead to false latching.
- Some amount of ringing is observable. However, the datasheet suggests that ringing within the overshoot and undershoot limits is acceptable.

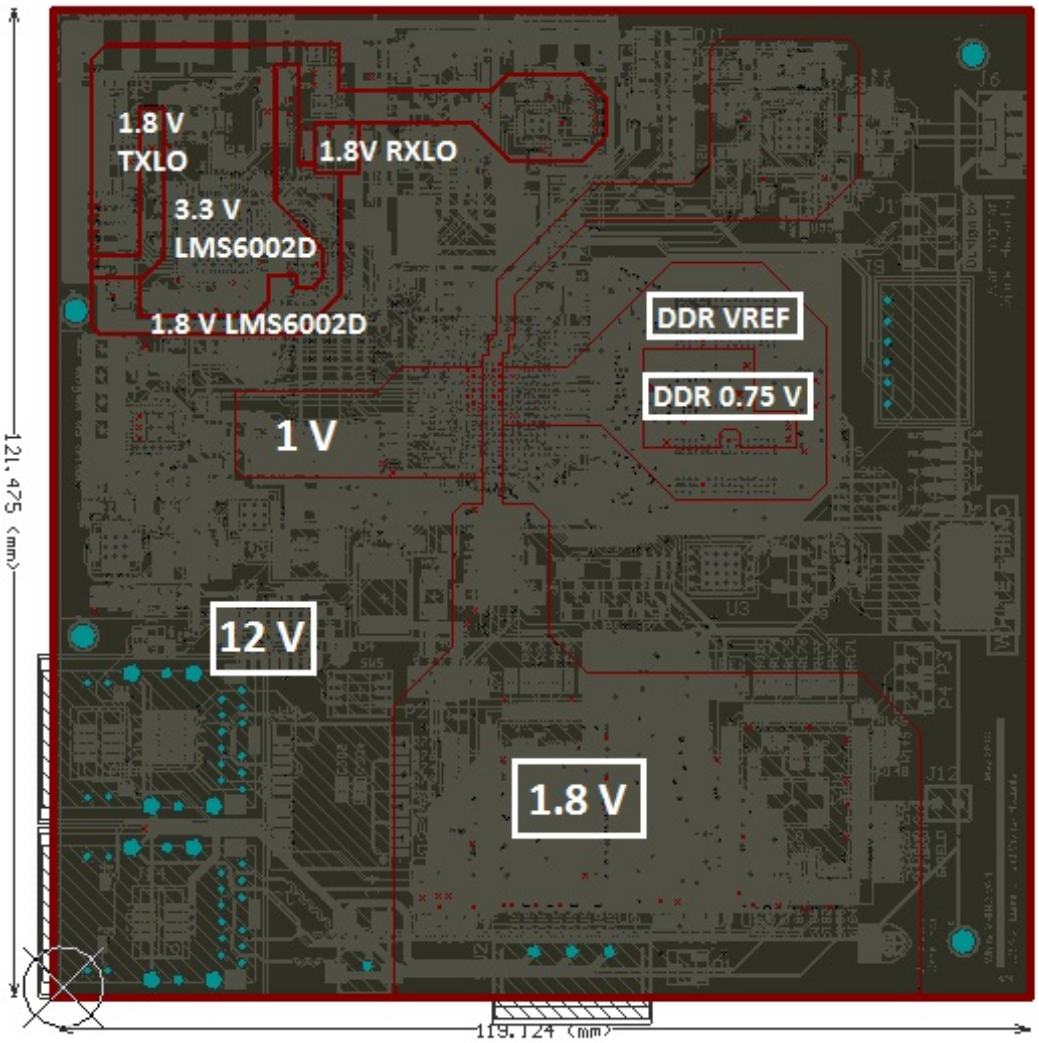

Figure. 7.7: Power Plane - II

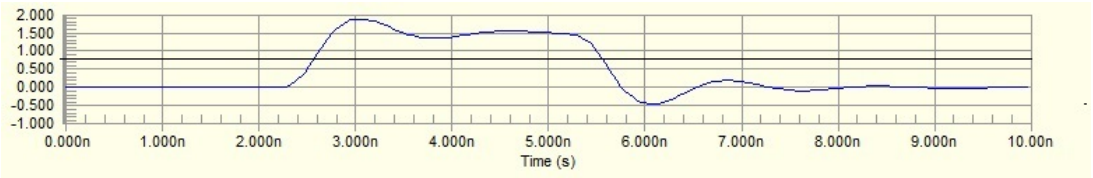

Figure. 7.8: DDR3 Clock(Single-ended) - 2ns pulse

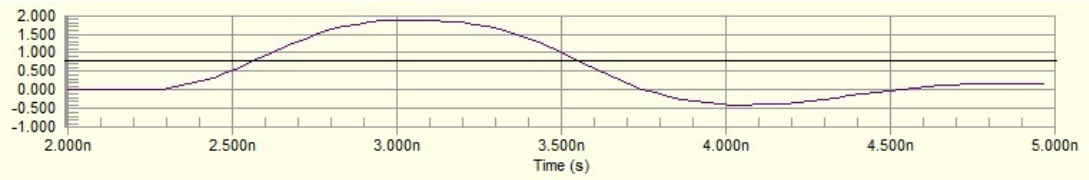

Figure. 7.9: DDR3 Clock(Single-ended) - 1ns pulse

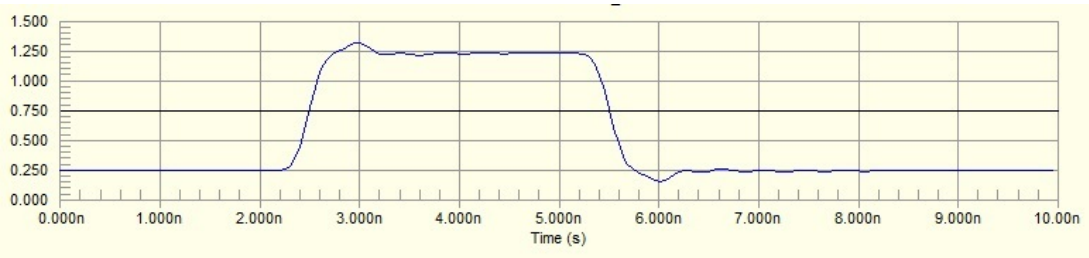

Figure. 7.10: DDR3 Address - 2ns pulse

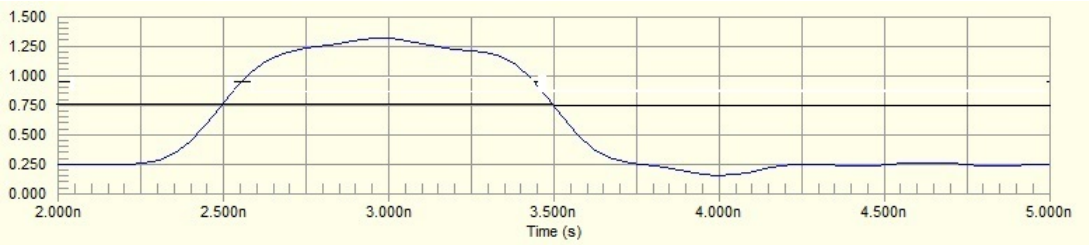

Figure. 7.11: DDR3 Address - 1ns pulse

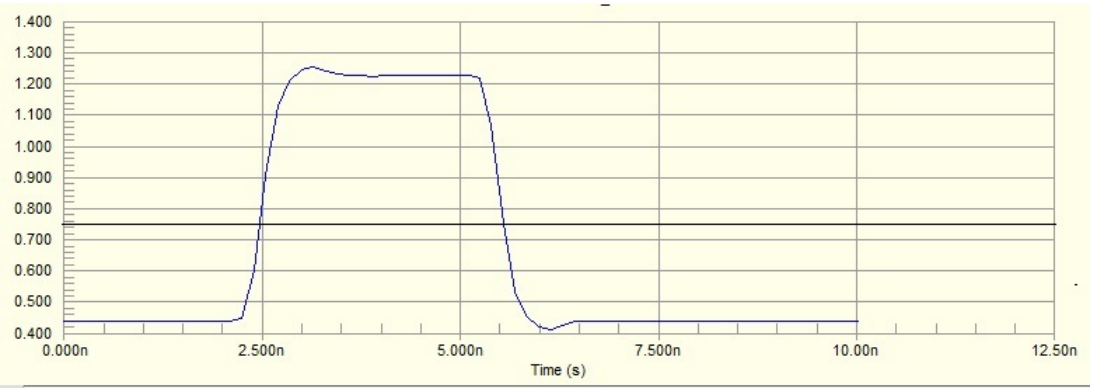

Figure. 7.12: DDR3 Data - 2ns pulse

7.1.6 White RHINO PCB

After routing all the traces with no auto-route tools used, the White RHINO

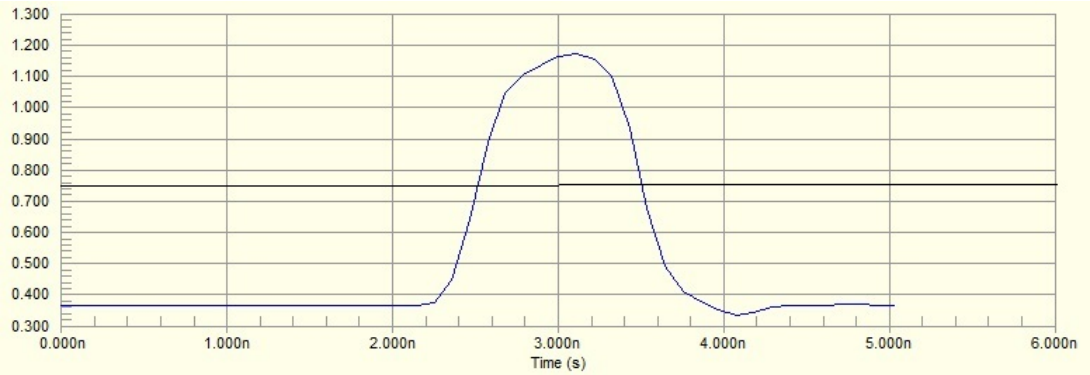

Figure. 7.13: DDR3 Data - 1ns pulse

PCB design was completed. During the design of footprints, step models were assigned in order to prevent component collisions. Using these step models, a 3-D view of the White RHINO PCB was generated by the Altium designer. This 3-D view of the White RHINO has been shown in Figure 7.14.

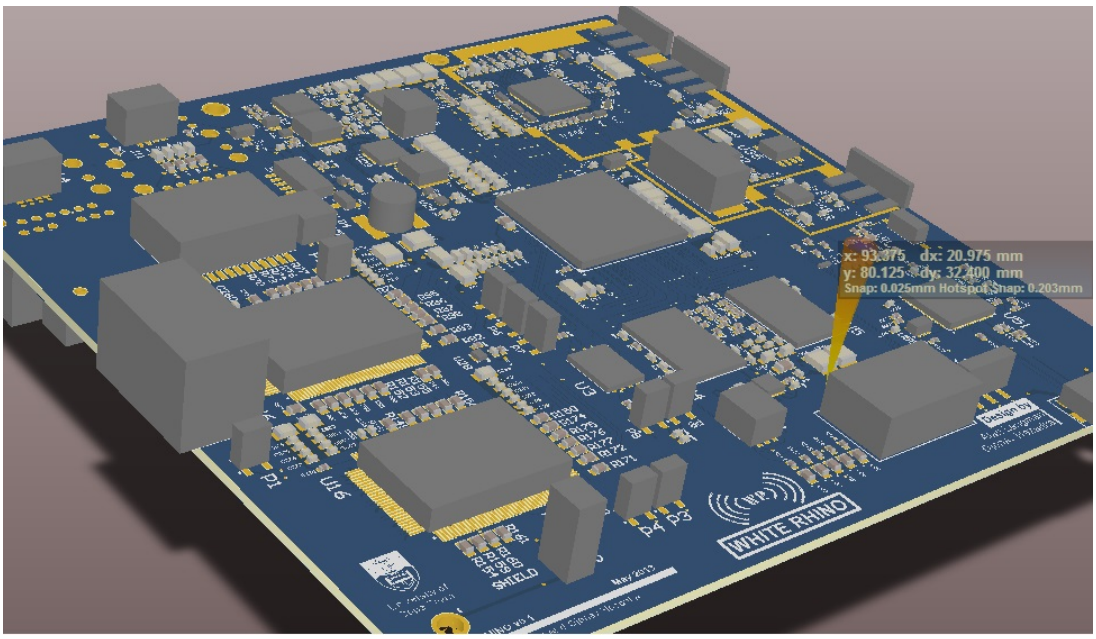

Figure. 7.14: White RHINO Complete PCB - 3D View

7.2 White RHINO RF

In this section, we shall discuss the PCB design of the White RHINO RF board. This small form factor board shall contain the front end section of the White RHINO Architecture. This board being a medium power RF board has thicker traces than the White RHINO for the same characteristic impedance. Again, we shall discuss the various design aspects of the RF board such as component placement, the PCB stackup, rules and so on.

7.2.1 Component Placements

The component placement of this board has been done in a different way and with a different goal. Unlike the White RHINO, this is a small board with very few digital and power traces. Hence, the component placement has been done to keep provisions for RF optimizations. The RF design requires careful PCB design and here, we follow the manufacturer guidelines keeping enough provisions for further tweaking. If we observe Figure 7.15, there are six gray regions. These regions shall be used for input, output and drain feed matching optimizations of the transmitter. The region A, B and C are the input, drain feed and output matching regions for the SGA6489 device. Simmilarly, the regions D, E and F are input, output and drain feed matching regions for the RFPA3800 device.

The rest of the components have been placed keeping space and isolation between power, digital and RF circuitry in view. Now that the components have been placed, we shall move on to define the stackup for this boad.

7.2.2 PCB Stackup

This board contains power amplifiers and hence, temperature will rise phenomenally. Keeping in view of the thermal effects of the amplifiers whose performance degrade rapidly with increase in temperature, the White RHINO RF board shall be a 2 layer board. The bottom layer shall be majorly ground. This has been done in order to attach heat sink and keep the temperature of the board in control. The stackup of this board is shown in Figure 7.16. The bottom layer has not been assigned a plane here because, in course of the design, we found that while routing some digital traces, crossovers became unevitable and so, some of those traces had to be routed through the bottom layer. However, as we shall see later, the bottom layers consists of very few traces and the rest is ground.

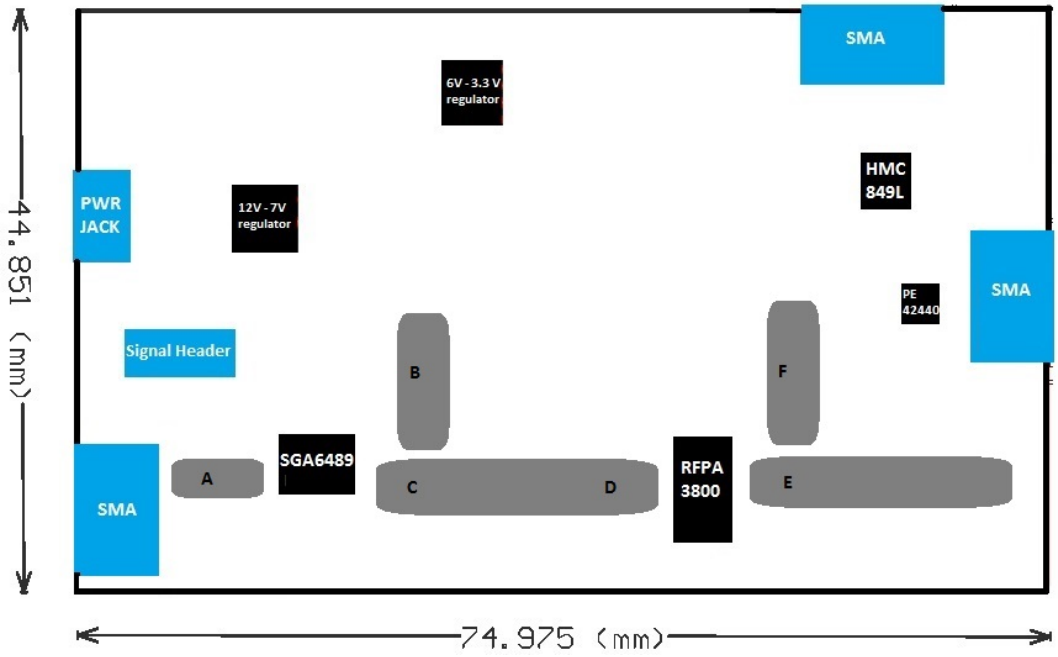

Figure. 7.15: Component Placement

These traces do not cause the ground plane to split underneath the RF traces.

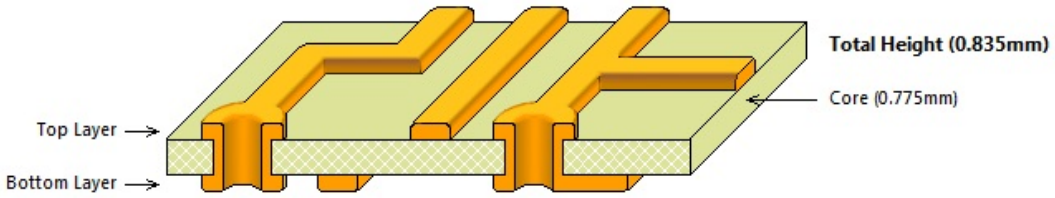

Figure. 7.16: White RHINO RF: PCB Stackup

7.2.3 PCB rules

Unlike the White RHINO, there are very few rules. This is due to the fact that there are no high speed digital traces. Only notable rule is the 0.1 mm copper to copper spacing. This rule abides by the fabrication house specifications. Another rule is that the minnimum trace width is 0.254 mm. We do not require very thin

traces on this board so this rule ensures that the cost of the board does not escalate unnecessarily.

7.2.4 White RHINO RF PCB

3-D step models have been assigned to the White RHINO RF board as well. The finished PCB model has been shown in Figure 7.18.As shown in Figure 7.18, the bottom layer is mostly ground except for a bunch of traces that move around the board without interfering with the RF traces. We can also observe all the stiched vias and mounting holes that shall facilitate the flow of heat from the device to the heat sink.

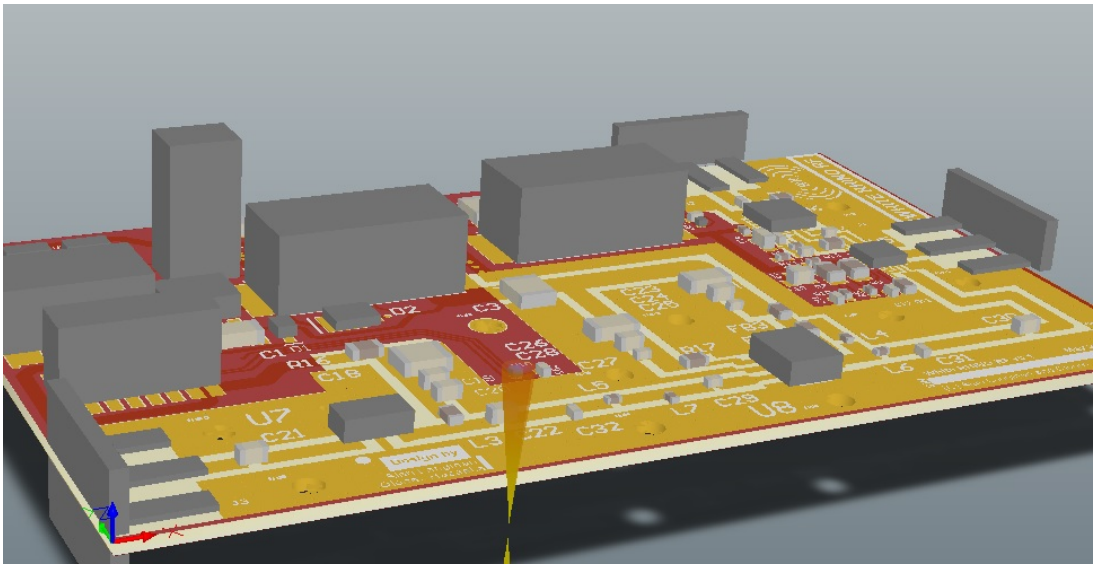

Figure. 7.17: White RHINO RF Complete PCB - 3D View

7.3 Manufacturing files

Finally, after the PCBs have been designed, the design files have to sent to the fabrication house. This is a two step process. First, the bare board is fabricated and then, the assembly is done. The files required for fabrication are:

- Gerber files or ODB++ files - These files contain the layer-wise copper etching information. These are the primary CAM files.

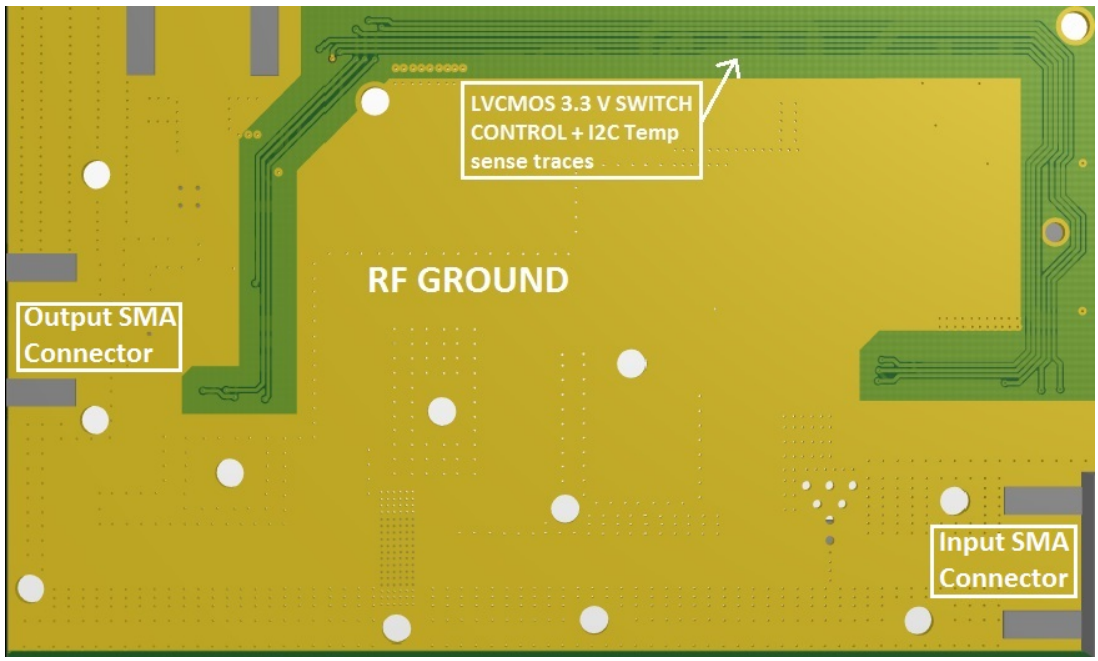

Figure. 7.18: White RHINO RF Complete PCB - Bottom Layer

- NC drill files - These files contain the drill information and drill report files containing the drill sizes, locations and so on.
- Drill Drawing - This is .pdf file which contains drill information and other customer instructions to the manufacturer.
- CAM ReadMe - This is a note created by the customer to provide general information about the files sent to the manufacturer.

And finally, the files required for the assembly are:

- Pick and place file - As the name suggests, this file contains the coordinate information for the pick and place machine.
- Bill of materials - This document contains all the components with manufacturer, part number, footprint information and so on.
- Gerber files - The assembly house uses the gerber files as a reference.
- Schematics - The assembly house uses the design schematics also as reference.

- Assembly drawing - The assembly drawing contains the main assembly drawing of the top and bottom layers and other assembly related instructions provided by the customer.

So, after the files have been sent for fabrication and then for assembly, the finished PC boards are shipped. Till now, we have discussed the design of the White RHINO boards. In the next chapter we shall discuss the testing of the boards and finally conclude in the last chapter..

Chapter 8

White RHINO: Testing and Verification

Testing and verification is a very important part of the PCB design. The design is not complete without thorough testing. The White RHINO boards too had to undergo this process. First passive tests were done with the boards and then the board was powered up. When all the basic blocks were working, then more complex tests were carried out. In this chapter, we shall discuss the testing and verification of the White RHINO boards.

At this juncture we should note that John Mudumbe from CSIR, South Africa supported the White RHINO testing. He played a key role in the testing process by building the U-Boot and the Linux images apart from supporting with the general software testing.

8.1 Initial Board Bring-Up

The board bring up is a three step process. First, basic passive tests are done with the bare and the assembled boards and only then board is powered up and other elementary tests are done.

8.1.1 Post-fabrication Tests: Passive

The White RHINO bare boards are shown in Figure 8.1. Even though the PCB files also included fabrication test points, after the bare boards were shipped, we decided to perform basic short circuit tests on the power nets. This was done to double-check that there was no fabrication fault.

This was done using a multimeter. All the power nets were checked for shorts.

Result: No fabrication Shorts were found.

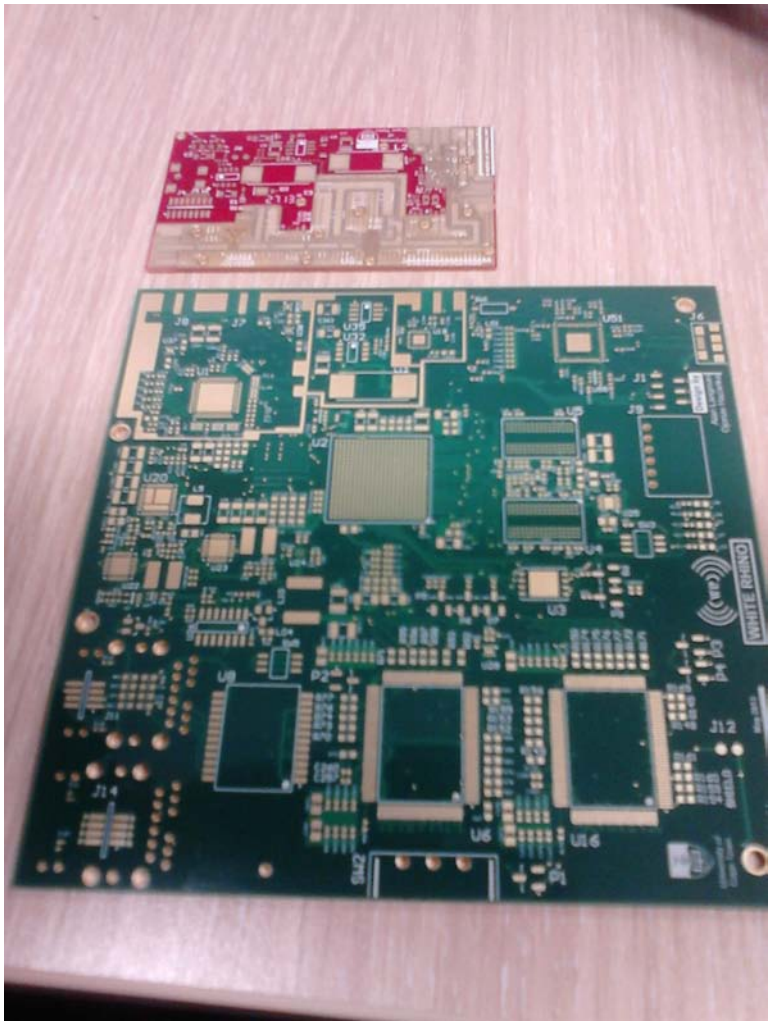

Figure. 8.1: Bare Boards

8.1.2 Post Assembly Tests: Passive

After the bare board tests, the board were shipped for assembly. The White RHINO assembled board is shown in Figure 8.2. Before powering up the board, the same tests were done to ensure that there were no shorts on the power lines. This again was done with a multimeter.

Result: Assembly short found on the 3.3 V power supply rail. Location of such ohmic shorts are difficult to find with a multimeter. They can be found with X-Ray scans or after powering up the board. Without X-Ray scan facility, this had to be done by powering up the board. We shall discuss this in the next section.

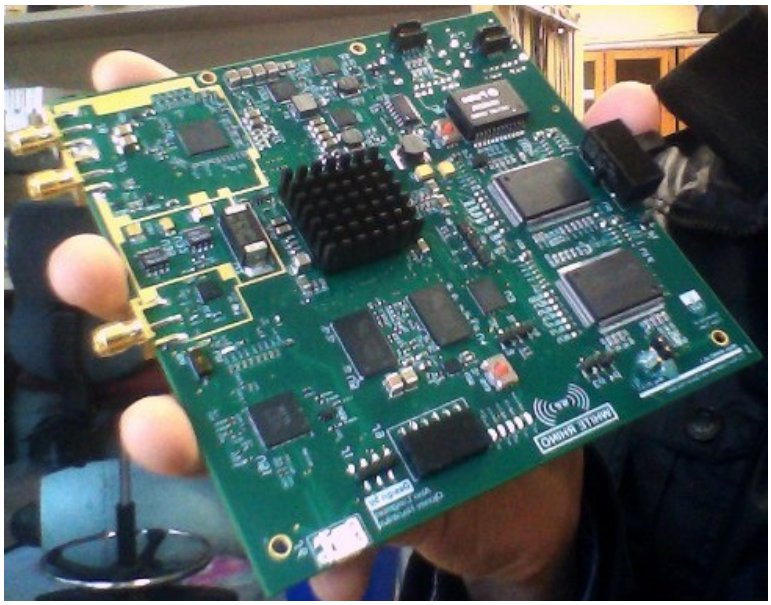

Figure. 8.2: White RHINO: Assembled

8.1.3 Powering up the board

As we found out that the 3.3V power supply rail has a short somewhere on the board, the location of the short had to found and that region of the board had to be isolated. The technique to do that is as follows:

Connect the board to a 12 V bench supply. Then, reduce the constant current to 0

A. Turn on the supply and slowly increase the constant current. The location has to be found out by an infrared scan or manually checking the board(with hand) for regions with higher temperature. The region where the board temperature is higher than the average temperature is where the short is.

After performing the above test, it was found that R181 - R187(Ethernet-2 termination resistors) were getting hotter than the surrounding components. This meant that the MDIO pins of the Ethernet-2 PHY device were shorted. Removing the resisters solved the issue. This also meant that Ethernet-2 became un-usable for this current board.

Result: The 3.3 V was no longer shorted.

8.1.3.1 Power Supply test

After performing the above changes, the power distribution generated all the votages correctly. The Power-Good signal turned high and the Power-Good LED turned on. However, the processor power-on-reset did not turn high as expected. This meant that the Zynq7020 device would not work as expected. The reason to this was found to be minor. The Quad-comprator did not receive a reference volatage to compare with the PGOOD_ALL signal. The pin was open circuited. Hence, a wire was connected to the 3 V reference zener diode D22.

Result: Zynq power on reset was available and hence, the device was brought out of reset.

8.1.3.2 Clocks test

Clocks are the heartbeats of an electronic system. So, its necessary to check if the crystal oscillators are generating clocks to the respective devices because without them, the devices will not function. This test was done with a 5GS/s Oscilloscope. The observed clocks are shown in Figures 8.3 to 8.6.

Result: All the crystal oscillators were generating the correct frequencies. These include:

- Zynq7020 - 33.33 MHz, 3.3 V
- Ethernet PHY - 25 MHz, 3.3 V

- FT4232 - 12 MHz, 3.3 V
- LMS6002 TCXO - 40 MHz, 2.5 V. This clock output is a clipped-sine waveform.

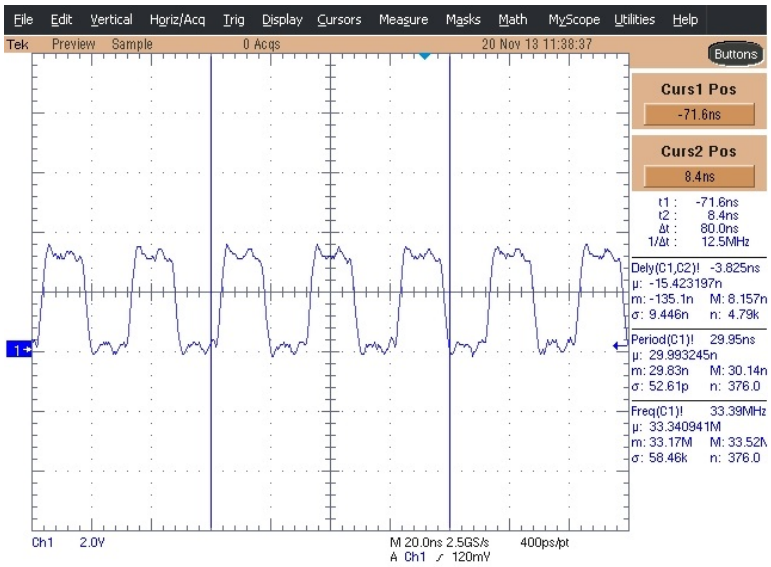

Figure. 8.3: PS Clock: 33.3333 MHz

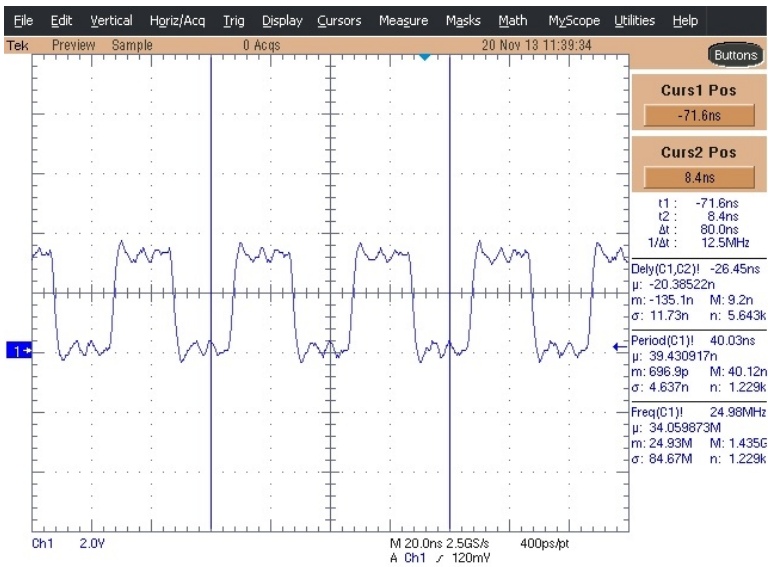

Figure. 8.4: Ethernet Clock: 25 MHz

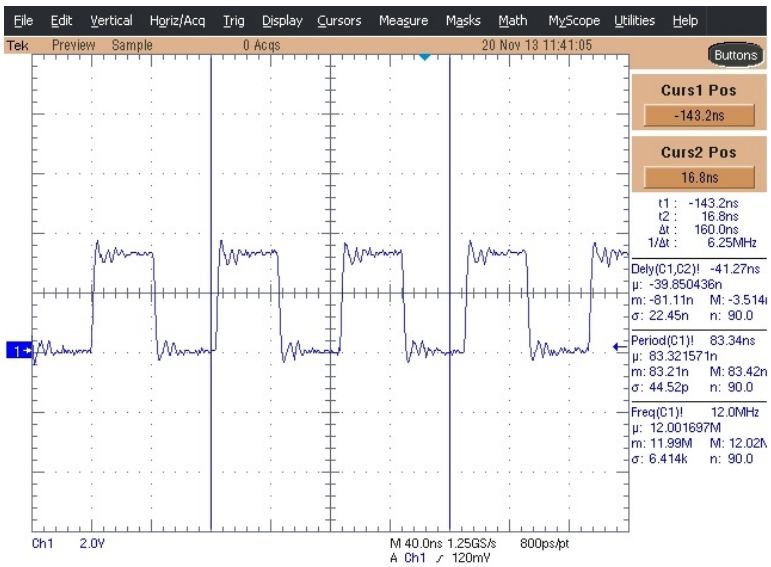

Figure. 8.5: FT4232 Clock: 12 MHz

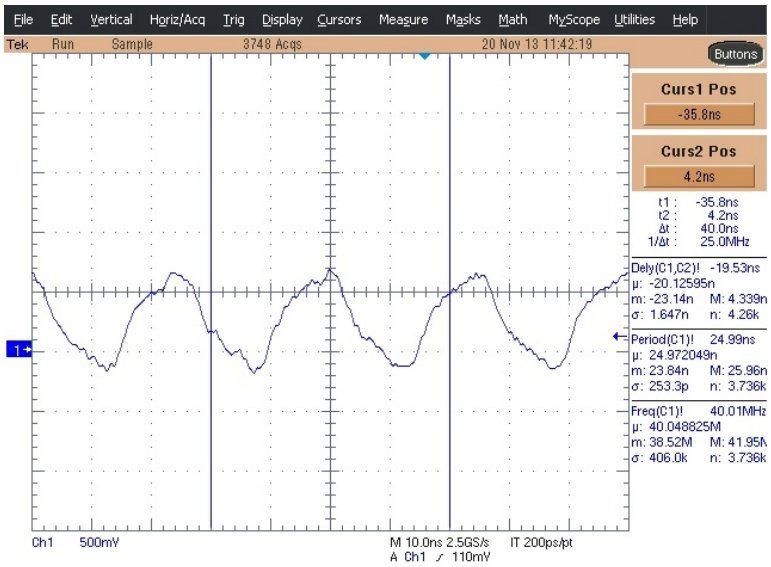

Figure. 8.6: LMS6002 TCXO: 40 MHz

8.2 Basic FPGA Tests

In the previous section, we found out that all the onboard devices were getting accurate power suplies and clocks. So now, we turn to functional tests on the board. The first set of these tests is the Zynq7020 test. The setup requirements

for these tests are:

- JTAG connection - This was provided with a Digilent USB-JTAG cable(HS1). The USB side was connected to the host PC and the JTAG side was connected to the onboard JTAG header(J1).
- Xilinx Impact - This is a software tool which is used to download the FPGA bitstream.
- Xilinx ISE - This is an FPGA development tool.

8.2.1 JTAG Chain Test

This first test was done to check if we could even detect the Zynq device. As shown in Figure 8.7, the impact tool was able to successfully detect the Zynq PL and the ARM DAP(Debug Access Port). It also passed the Chain Integrity test at 40 MHz and device staus values could be read correctly. The tool detected the manufacturer ID of the Zynq device as 0x23727093.

Result: JTAG Chain test passed.

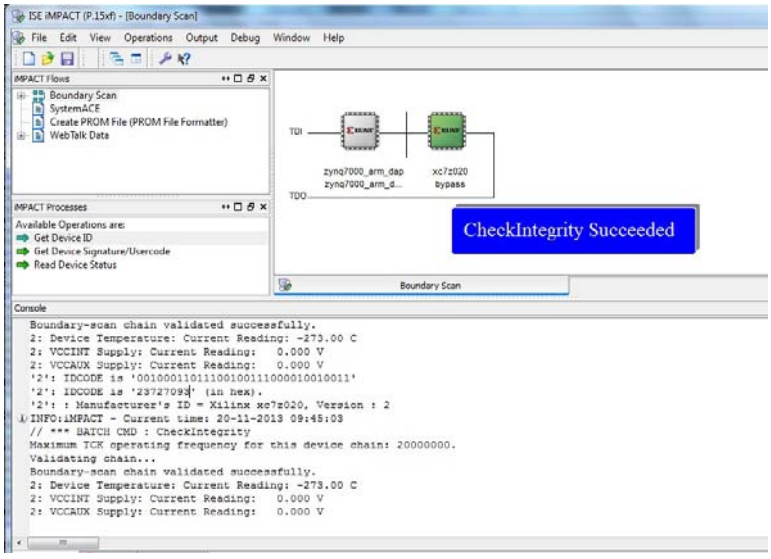

Figure. 8.7: JTAG Test

8.2.2 LED Test

After successful detection of the JTAG chain, the next task was to run a simple test to ensure that the Zynq PL was working as expected. A bitstream containing a program which internally pulled up a GPIO LED connected to the Zynq PL was downloaded.

Result: The Program DONE LED(LD1) and the GPIO LED(LD6) turned on confirming that the Zynq PL is functional.

After these tests, we shall move on to the discussion on the tests that were carried out on the ARM processing system of the Zynq7020.

8.3 Processor Tests

The processor tests of the Zynq7020 required embedded software development tools. The information about these tools and design flows can be found in [46–48]. The Zynq device has multiplexed IOs(MIOs) which can be alternatively used to connect with different peripherals. This has been provided by the Zynq to facilitate flexible board design. However, since the IOs are multiplexed, our first task was to assign IO ports to various onbard peripherals. This process is called the PS7 initialization. Only after the PS7 initialization is done further software development can be done. The software development flow for the White RHINO is shown in Figure 8.8. The development tools required for this set of tests are as follows:

- Xilinx XPS - The Xilinx Platform Studio(XPS) is an embedded design tool which was primarily used to design of the Zynq MIO structure.
- Xilinx SDK - The Xilinx Software Development Kit(SDK) is an eclipse based Software development tool. Apart from stadard tools, it also contains the Xilinx Microprocessor Debugger(XMD) console which was extensively used to communicate with the processor. This debugging facility is facilitated through the JTAG port.
- Tera Term - This is an open source terminal emulator program. This software was also extensively used to observe serial console prints.

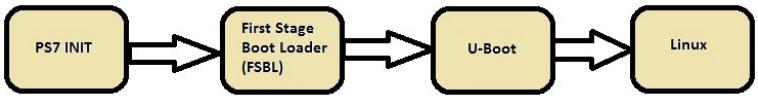

Figure. 8.8: Software Development Flow

8.3.1 Processor Initialization: PS7 Initialization

As mentioned above, the first step of the software development is the PS7 Initialization. The PS7 initalization basically initializes and sets various registers of the Zynq. Most of these registers are part of the system level control register(SCLR, Base Address: 0xF8000000). The primary functions of this PS7 initialization are:

- PLL Initialization - There are three clocks domains on the Zynq. These are ARM PLL, DDR PLL and the IO PLL. All the clocks inside the device are generated by either of these three PLLs. The purpose of this initialization process is to set the right PLL divider values and enable them.
- Clock Initilization - After the PLLs are initialized, next step is to initialize the clocks. These clocks include are the peripheral and the PL clocks. In this process, the correct clock divisors are set and then they are enabled. In this step, the CPU clock ratio is also selected. For our design it has been chosen as 6:2:1.
- DDR Initialization - As the name suggests, in this step various DDR related registers values are set. This includes DDR IO bank configurations, IO bank slew rates and so on.
- MIO Initialization - During this initialization, the MIO configurations are done. Here, the MIO pins of the Zynq are assigned to various peripherals. This is done according to the schematic design of the board. For example, the register 0XF8000714 was assigned a value of 0x00000702 which means that the pin MIO 6 shall be the QuadSPI clock output and is rightly connected to the QuadSPI flash clock.
- Peripherals Initialization - After the MIO initialization is done, the peripheral parameters such as clock dividers, data enable/disable, Interrupt settings and so on are set. However, we must note that all these settings can also be done also in the application software.

Result: The PS7 initialization was successfully done through a .tcl file. The values of the registers written were confirmed by doing a memory read using the XMD. After the successful PS7 initialization and before porting an operating system, we decided to perform some basic tests. These tests were done to confirm if the processor was functioning as required.

8.3.2 Application-I: Standaone Processor "Blinky"

A simple program involving turning on and turning off of GPIO LEDs connected to the MIO pins was performed. This was done by downloading and then running a .elf from the XMD.

Result: Test was successful and the LEDs blinked in a periodic fashion as expected. An oscilloscope reading was taken to demonstrate the LED inputs with time. Its shown in Figure 8.9

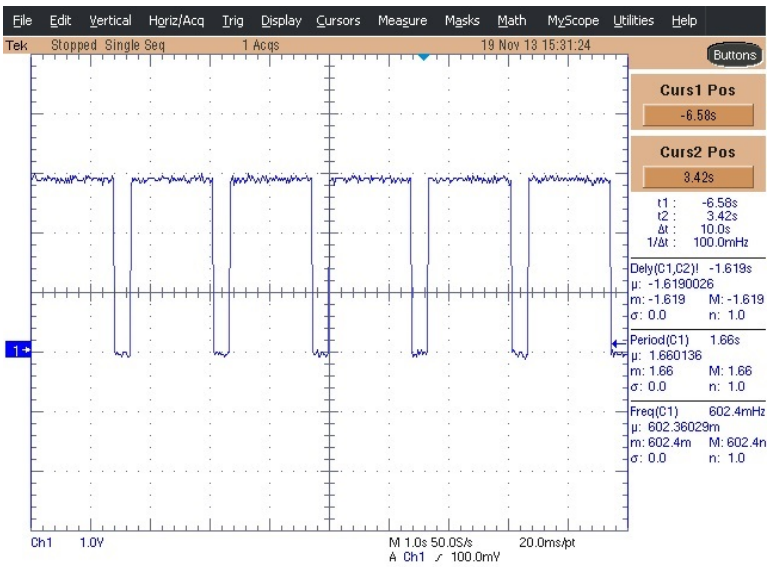

Figure. 8.9: PS Blinky Oscilloscope Reading

8.3.3 Application-II: Standalone Processor "Hello World"

The next standalone appllication program that was tested was a simple UART print. The application periodically prints "Hello World" to the serial console.

This required the Zynq board support packge(BSP). The Zynq BSP is available for use in the Xilinx SDK and also available to download from the Xilinx website. The UART print is then sent via the USB port by the FT4232 device. The baudrate of the print was set to 115200 bauds. Initially, we did not receive a print on the Tera Term Serial Console. Then, we found out that the FT4232 CTS pin had to be grounded in order to facilitate communication. The pin was externally connected to ground with a wire soldered to the CTS pin.

Result: The print was observed on the Tera Term console, Figure 8.10.

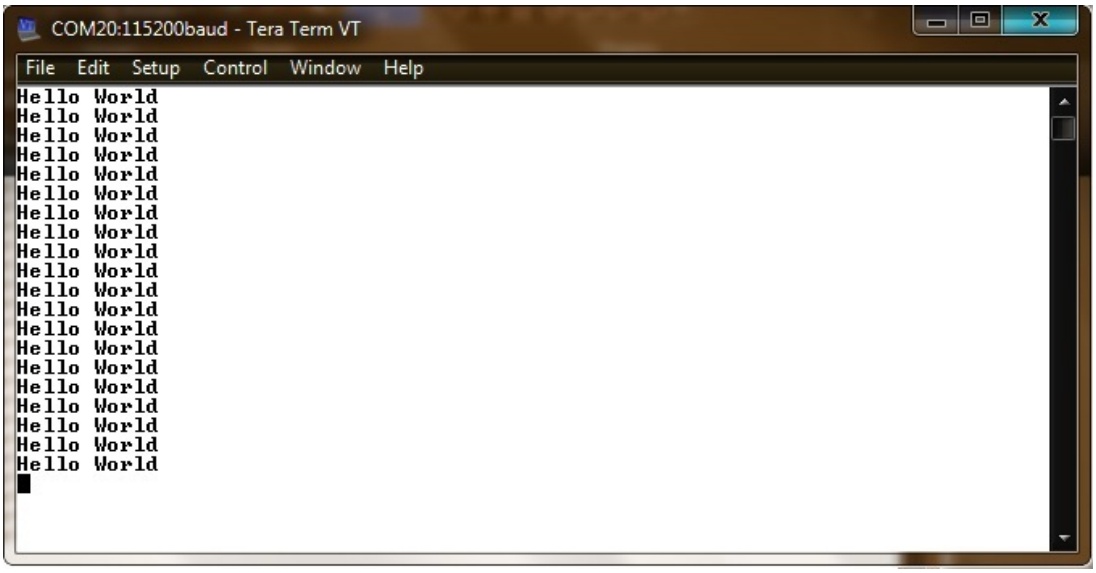

Figure. 8.10: UART Print: "Hello World"

8.3.4 Zynq FSBL and U-Boot

In order to port an operating system into the Zynq, the first stage bootloader(FSBL) has to be built first. Apart from the PS7 initialization that we discussed above, the Zynq FSBL contains boot related information. The White RHINO U-Boot initializes the peripherals, provides command line environment for testing hardware peripherals and run applications. The White RHINO U-Boot prompt is shown in Figure 8.11, commands in Figure 8.13 and the environment in Figure 8.12. We shall discuss the testing of the Peripherals in greater detail in the

next section. The boot images can be found in the attached CD.

Result: U-Boot successfully ported and command line interface was available to use.

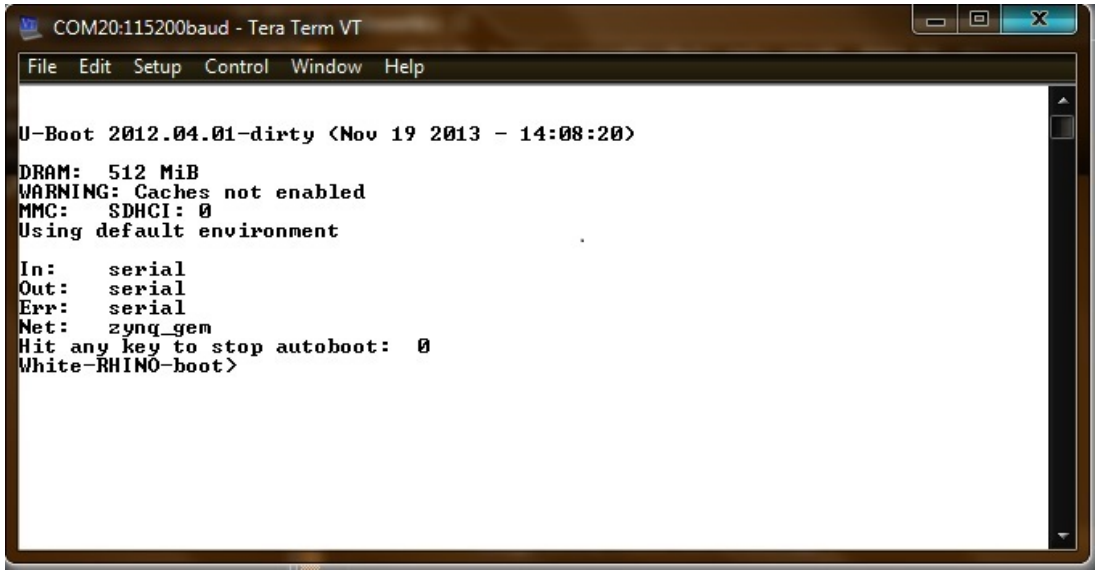

Figure. 8.11: White RHINO: U-Boot Promt

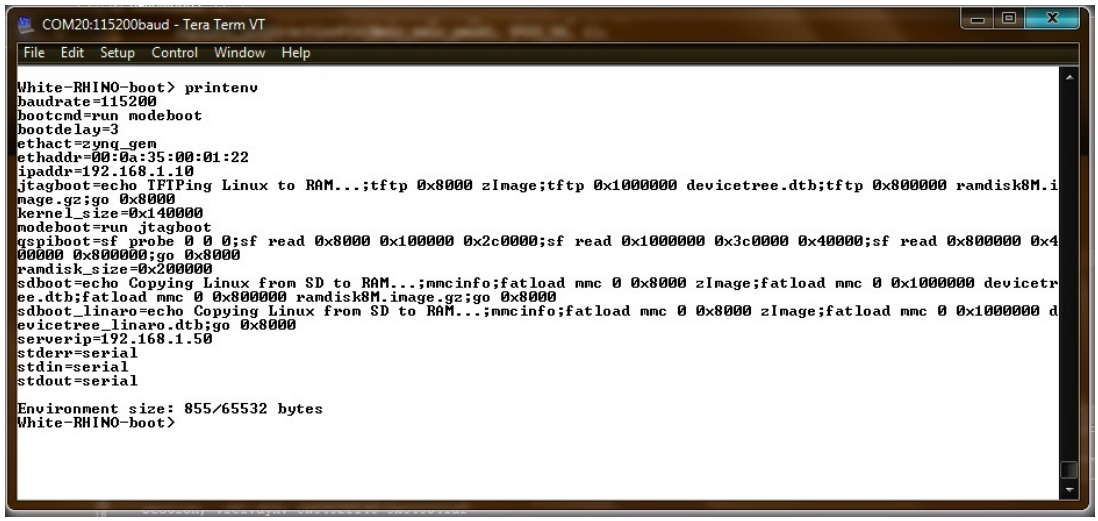

Figure. 8.12: White RHINO: U-Boot Environment

Figure. 8.13: White RHINO: U-Boot Commands

8.3.5 Zynq Linux

The running operating system on the White RHINO has to be Linux. So, after porting U-Boot on to the White RHINO, a Linux image was built using the Zedboard souce code. This image was ported into the Zynq memory along with the Root File System and the Device Tree. The Linux booted successfully and an image of the boot process is shown in Figure 8.14

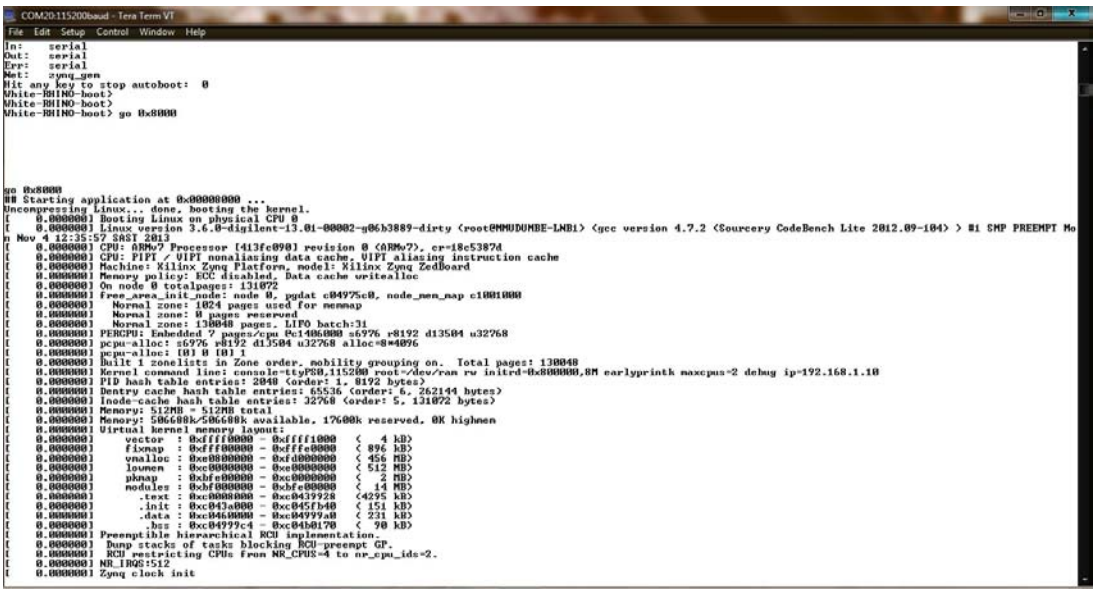

Figure. 8.14: White RHINO: Linux Boot

8.4 Application III - Memory and Peripherals Tests

After porting operating system to the White RHINO, we now shall discuss that various peripheral tests that were done to validate the design. These tests include the memory tests of the DDR and QSPI flash, general Zynq Peripheral test, the 1 Gbps Ethernet test and so on. These tests valiadted through software prints and some of the signals have also been observed on the oscilloscope.

8.4.1 Memory Test

The first test is the memory test. This has been done using a Standalone application. The application initializes the DDR and the flash memories and prints the test result on to the UART console. This application program is available as a Zynq test template in the Xilinx SDK. The test results have been shown in figure Figure 8.15. The SD interface has been verified through the U-Boot which detects the SD card as shown in Figure 8.16.

Result: The memory interface tests were successful.

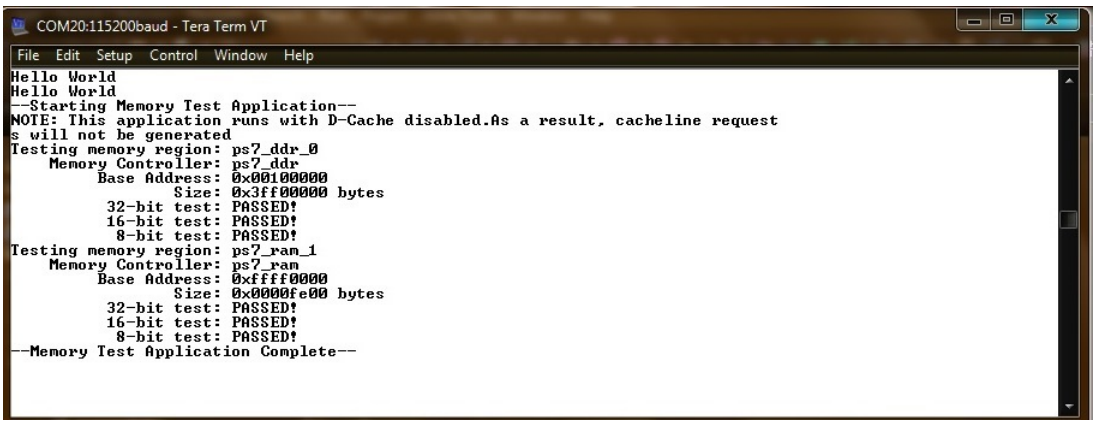

Figure. 8.15: Memory Tests

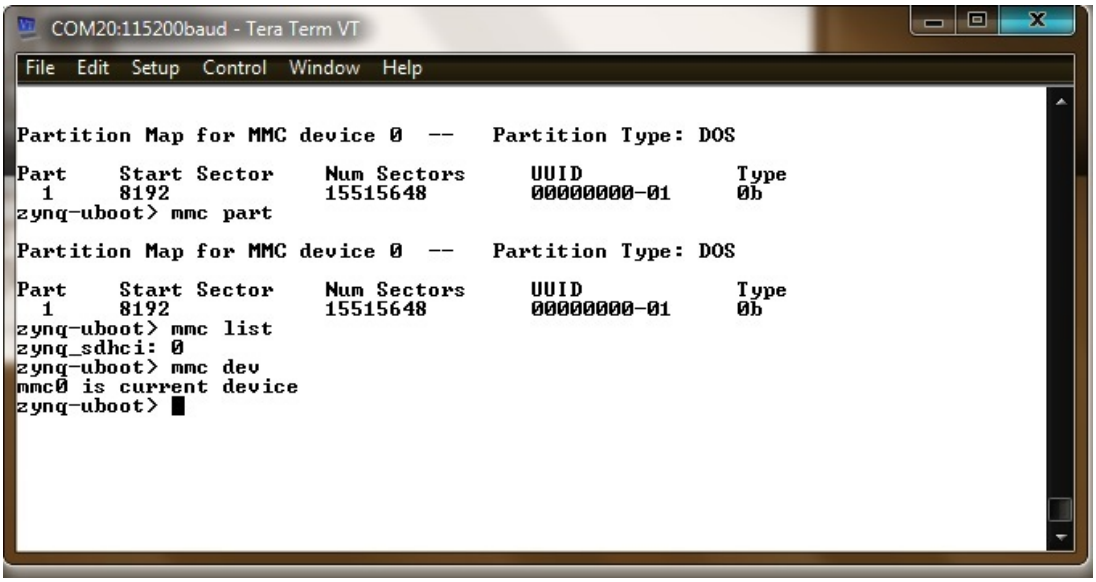

Figure. 8.16: MMC Info: U-Boot

8.4.2 Application IV - General peripheral test

One more test which is available as a Zynq test template in the Xilinx SDK is the general peripheral test. This test checks the devcfg(Device Configuration), scugic(Snoop control Unit General Interrupt Controller), scutimer(Snoop control Unit timer) controller and so on.

Result: The General Peripheral Tests were successful.

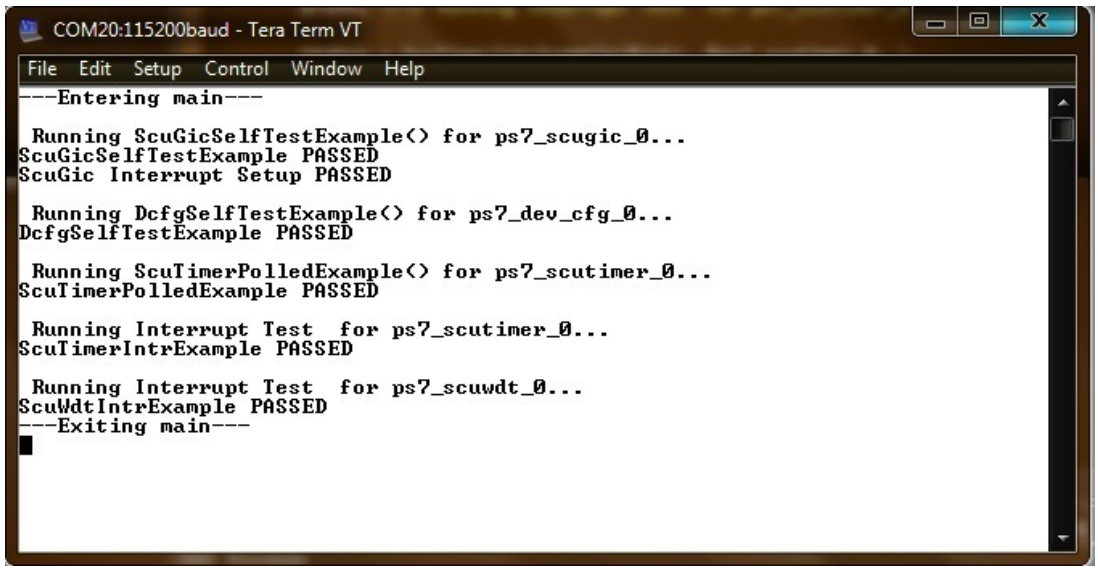

Figure. 8.17: General Peripheral Test

8.4.3 Application V - 1Gig Ethernet test

The 1Gig Ethernet subsystem is a datapath block of the White RHINO communictions. This test includes the following subtests:

- Verifying the MII interface
- Verifying the MDIO interface
- Performing an MII Loopback
- Performing a ping from the White RHINO to the host PC and vice-versa.

Before performing these tests, the RGMII select jumpers(P1 and P2) on the board have to be set to 1,1. This select the RGMII-3COM mode for the media-independant interface. The U-Boot incorporates some Ethernet PHY commands. These commands are passed to the Ethernet PHY through the management and control interface. These commands allow us to check if the PHY device is available and read and write to its registers. As shown in Figure 8.18, the device detected has a manufacturer ID of 0x80017 which is the correct ID for the DP83865 device. In the same figure, we can also see the standard PHY registers being read back. We can also see the MDIO info in Figure 8.19.

Now, after we ascertained that the PHY device is alive, we ported Linux into the Zynq and performed an MII loopback test using the local loopback IP address. Finally, after the MII loopback, we connected the White RHINO to the host PC using a CAT-5 Ethernet cable. After changing the IP address of the host PC to 192.168.1.50, PING was run on both White RHINO and the host PC. The PC ping replies from the host observed on the White RHINO linux prompt is shown in Figure 8.20 and the 125 MHz data clock measured on the oscilloscope is shown in Figure 8.21

Result: The 1 Gbps Ethernet test on the Ethernet1 port was successful.

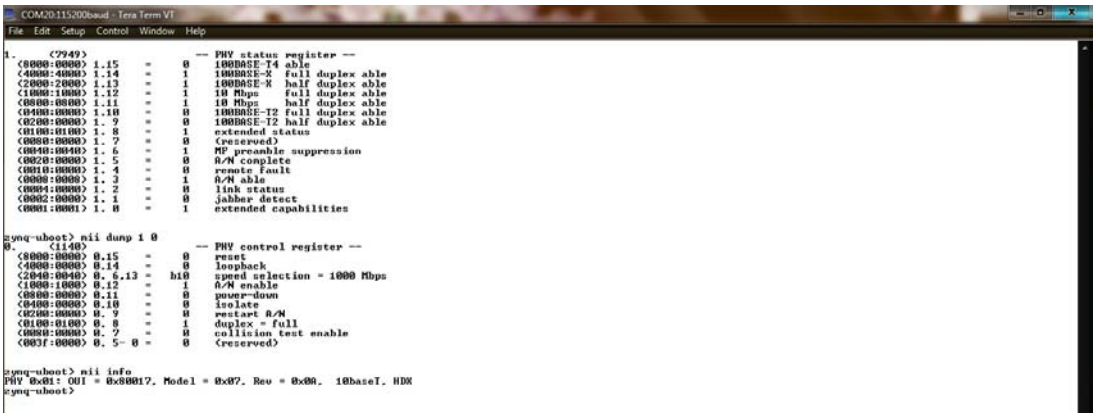

Figure. 8.18: MII Info: U-Boot

Figure. 8.19: MDIO Info: U-Boot

8.4.4 LMS6002 Test

There was an accidental footprint error on the LMS6002. Even though the size of the pads are correct, there has been a pin numbering error. The pin numbering

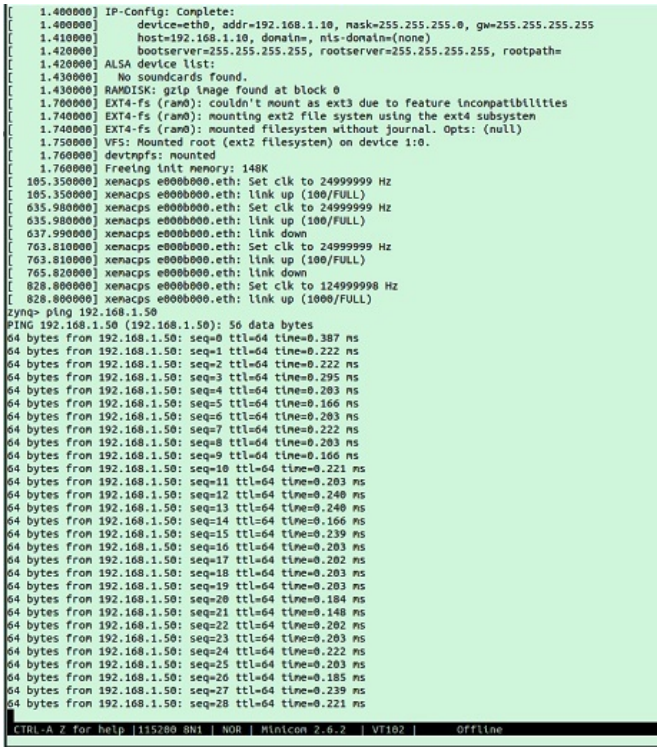

Figure. 8.20: Host PC Pinging the White RHINO at 1 Gbps

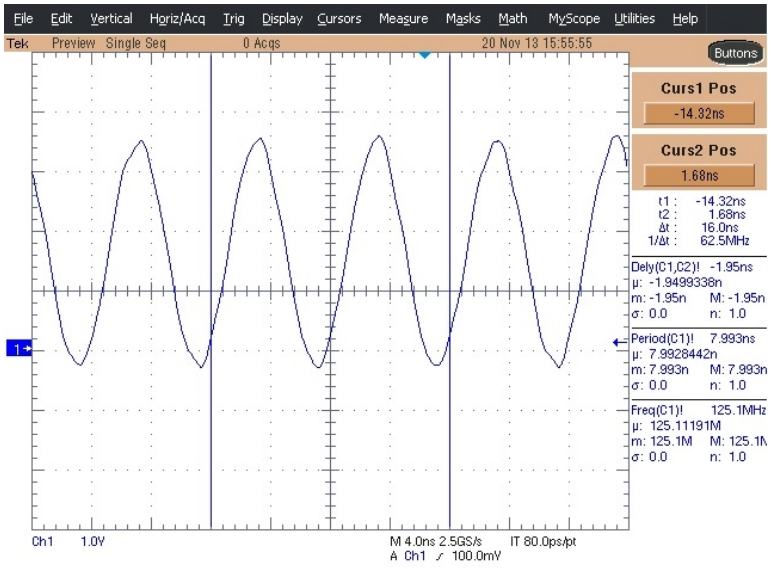

Figure. 8.21: Ethernet Data Clock: 125 MHz

mismatch is shown in Figure 8.22. This mismatch happened while drawing the footprint of the device. This error has rendered the whole LMS6002 interface non-functional. This error shall be corrected in the next version on the White RHINO fabrication outputs. The design files attached in the CD contain the updated PCB that do not have this error.

Result: LMS6002 test Failed.

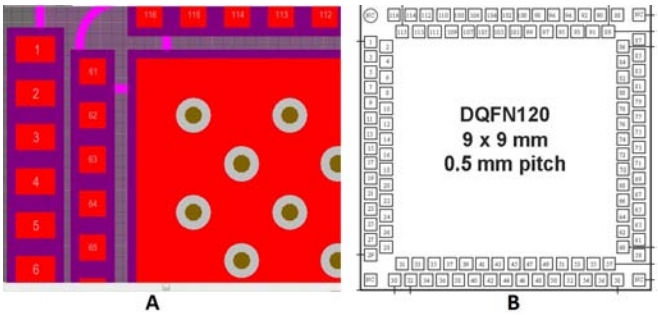

Figure. 8.22: LMS6002 Footprint Error. A - White RHINO LMS6002 footprint and B - Actual LMS6002 footprint

8.5 Tests involving FPGA-Processor Communication

After all the tests noted in the last section, we tested the MIO-EMIO interface of the Zynq. This involved routing the processor signal to the PL using the XPS. The sampling clock for this test is the FCLK0 which is an FPGA clock. For this particulal test, a PL blinky was performed for which the GPIO LED(LD6) connected to the PL was controlled by a PS program. The changing state of the LD6 has been captured in the oscilloscope for demonstrantion, Figure 8.23.

Result: The PS of the Zynq successfully controlled a PL LED and thus validating the PS-PL communication.

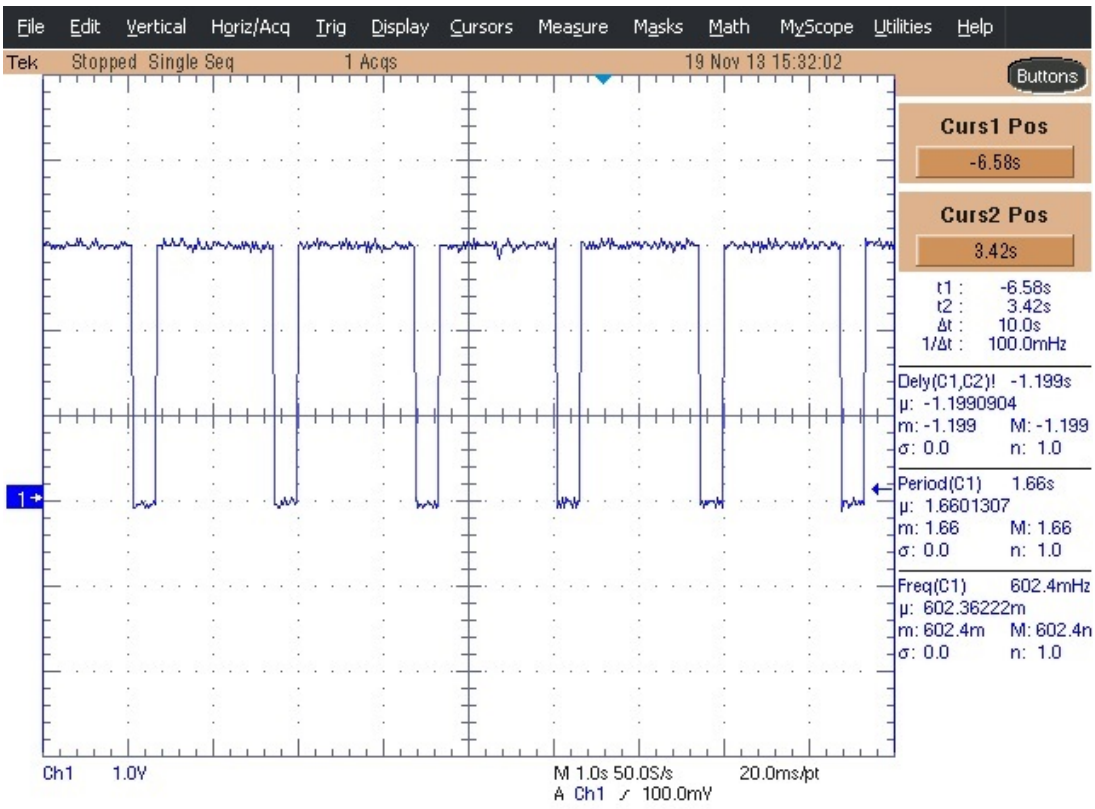

Figure. 8.23: ARM Controlled PL LED Blinky

8.6 RF frontend Tests

Finally, we tested the RF frontend board. We tessted the board for mid-band gain at various power levels and the gain flatness over the whole bandwidth of operation. The The test setup included the following:

- Signal Generator.
- Spectrum Analyzer.
- SMA Cables.
- Attenuators.

The output from the signal generator was connected to the the input connector on the White RHINO RF board and the input to the Attenuators was connected

to the Antenna connector of the same board. The output of the Attenuators was then taken to the Spectrum Analyzer. The RF controls were as follows:

- ANTSW_CTL_2: 0V.
- ANTSW_CTL_1: 3.3.
- HMC_VCTL.

The above control levels ensured that the transmit path was turned on. Now, we shall discuss the tests carried out on the board. Here, we should note that tests were carried out with only continuous wave(CW) signals due to absense of desired signal personality in the signal generator.

8.6.1 Mid-Band Gain

In order to perform this experiment at first a measurement of the through power levels excluding just the design under test(DUT) was done at 610 MHz. Then, the DUT was inserted and the power reading were taken again at the various power levels measured in the previous step. The spectrum analyzer plot has been shown in Figure 8.24. Here, the power level shown is not the true power level because the signal has been attenuated by various amounts at the various power levels and hence, reference level offset was not set. In fig. 8.25, the measure gain values at the various power levels have been plotted. As we can observe, the DUT achieves a midband gain of 31.5 dBm.

8.6.2 Gain Flatness

In order to measure the Gain Flatness of the DUT, the signal generator frequency was swept from 512 MHz to 698 MHz which is our desired bandwidth of operation. Then, the spectrum analyzer trace was kept on max hold. As we can observe from Figure 8.26, there is about 6 dB variation over the band. However, as we have seen from chapter 6, the White RHINO RF linup provides a variable gain range of 56 dB. Hence, this variation of gain can be easily compensated using power control.

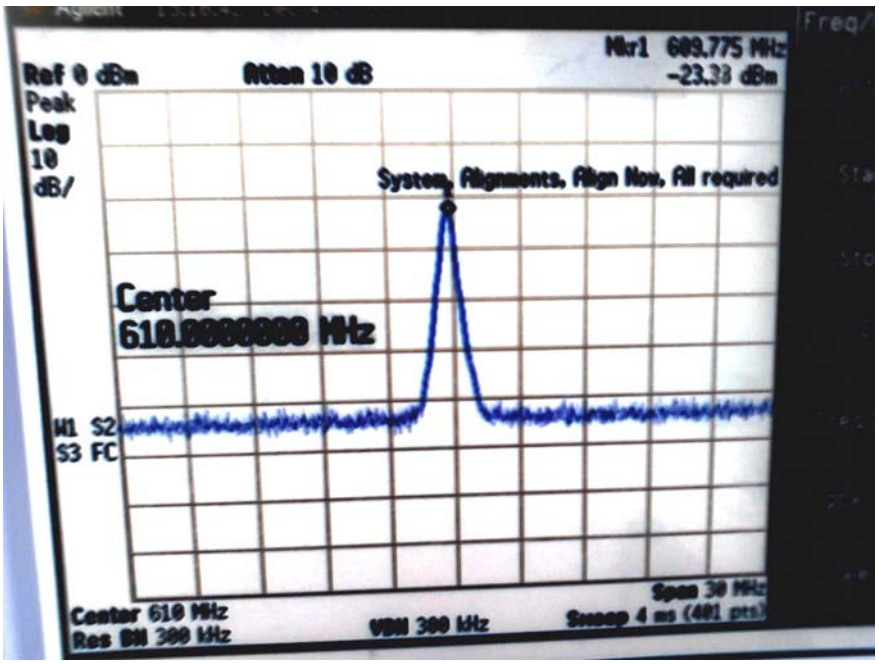

Figure. 8.24: Single Tone Signal at 610 MHz

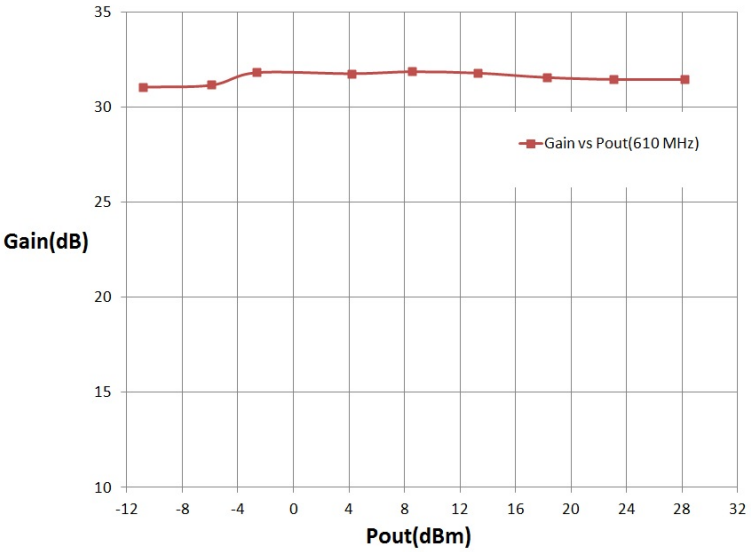

Figure. 8.25: Gain vs. Output Power

Figure. 8.26: Measured Gain Flatness

8.7 Bugs and Fixes

Now, we have come to stage where we can note down all te bugs and the fixes implemented on the White RHINO boards. All of them have been noted in Table 8.1. Please note that the bugs and fixes marked with a '*' could not be implemented on the current White RHINO boards. So, these changes have been implemented for the next versions of the boards.

8.8 Cost of the White RHINO boards

After having figured out the bugs and fixes to be carried out, we requested a quote for the manufacturing of 100 pieces of the boards. As shown in Table 8.2, the White RHINO system shall cost us less than 1000 USD. This makes the White RHINO system computationally more powerful, with more features and at the same time much less expensive than the USRP N210.

Table. 8.1: White RHINO Bugs and Fixes

S.No	Bug	Fix
1*	Wrong ESD Diode footprint	PCB library file for the ESD diode has to be modified
2*	Wrong LMS6002 footprint	PCB library file for LMS6002 has to be modified.
3	Host PC unable to communicate with Zynq UART	CTS pin has to be connected to ground.
4	Zynq does not receive power on reset	3 V reference to pin 8 of Quad-comparator LM339M has to be provided.
5*	Boot mode jumpers cannot be identified unless referred to the schematics	Clearer silkscreen labels have to be provided.
6	Enable signals do not attain correct voltages	The drain resistors of FDV301 have to be changed to 100 Ohms.
7*	Power Disable does not attain correct voltage	Voltage drop occurs due to resistor loading. The enable circuitry has to be appended using a 3 V reference diode.

Table. 8.2: Cost of the White RHINO boards

S.No	Item	Cost
1	PCB Fabrication Cost	85 USD
2	Component Cost	600 USD
3	Assembly Cost(Estimate)	250 USD
-	**Total Cost**	**935 USD**

Chapter 9

Conclusions and Future Work

In this dissertation, we discussed the concept, design, implementation and testing of the White RHINO system. We found out that apart from the accidental error in the RF transceiver section, rest of the subsystems on the boards could be tested successfully and validated. In this final chapter, first we shall summarize the design process that took the White RHINO from a concept to a working system. Then, we shall analyze whether the White RHINO meets system requirements. And finally, we shall discuss work that remains to be done.

9.1 Design Summary

The design of the White RHINO was envisaged keeping Whitespace-based Communications Radar functionality in view. The initial user requirements, standard specifications (FCC and IEEE802.22) and review of existing hardwares together formed the final set of requirements for the White RHINO. We also reviewed the radar detection capabilities of a system that could operate in the TV Whitespace spectrum and comply with its norms.

Then, the actual design process was started. The requirements paved the way for the design of the Hardware Architecture. The Hardware Architecture defined the selection of primary components, the interfaces(external as well as internal) and provisions for debug.

After the Hardware Architecture was laid down, subsystems were defined and their requirements were laid down. This led to the selection of the rest of the

components for the system. Then, the schematics were drawn which were validated by simulations. Schematic design included drawing of schematic symbols, the actual schematics and the PCB footprints. The completed schematics were then exported for PCB design. Here, first the components were placed, the stackup was decided and then routing was done. The fabrication and assembly outputs were generated after the PCB was completed.

After the assembled boards arrived, testing was started. It started with initial board bring-up. This led to basic hardware tests which then led to more complex tests. These tests required gateware and firmware softwares to be developed. With the use of software development tools, software tests were developed and run on the White RHINO. The board passed all the tests except the LMS6002 test which could not run due to incorrect pin numbering of the footprint. The White RHINO RF board was tested and its performance was noted.

9.2 Conclusions

In the previous chapter, we have discussed the tests that the White RHINO passed and the ones that it failed. Now, we shall dicuss where does the White RHINO stand in terms of the system requirements. In Tables 9.1 to 9.4, all the requirements have been listed. Each table also has a column that states whether those requirements have been met or not.

Here, the requirements marked with an '*' are the paramters which could not be tested for a fully integrated system. The RF frontend section was tested in a standalone manner due to the non-functional LMS6002 subsystem. It has been assumed that since both the Ethernet ports are connected in a similar way, successful functioning of one implies that the other one shall function simmilarly. As we know from the chapter 8, one Ethernet could not be tested due to the Assembly short.

Apart from the above mentioned faults, the rest of the system functions the way it was expected to and the system requirements have been met under the condition that they will be rectified in the next version of the White RHINO system.

Table. 9.1: Requirements: Computational

S.No	Requirement	Description	Met?	Remarks
1	Programmable Logic	Resources present in Zynq7000's programmable logic	Met	Zynq PL is being tested and is functional
2	Processing System	Dual-Core ARM^{TM} Cortex A-9 processors with Single-Precision Floating Point NEON^{TM} Media Processing Engines(MPEs)	Met	Both the A-9 processors are tested and Linux has been ported successfully.
3	Memory	512 MB DDR3 SDRAM	Met	The DDR3 interface has been tested successfully.

9.3 Future Work

Being a Whitespace-based Communications Radar platform, the White RHINO shall require implementation of complex algorithms and Network Layers before it can be called a fully-functional product. However, here we shall discuss only the work that remains to be done at the hardware level. The important things to be done for the White RHINO system are:

- Build the Next Version Boards - As we have seen that RF transceiver section of the board is non-functional due to the footprint error, its becomes the primary test objective once the next version boards arrive. The next version boards shall also incorporate other minor fixes.
- Final Stage Power Amplifier - Currently, there is a scarcity of amplifier devices which are tailored for Whitespace applications and have about 200 MHz of bandwidh of operation. Hence, once they are commercially available, the final stage amplifier RFPA3800 which has a relatively narrow bandwidth of operation has to be replaced.
- Rigorous Compliance Testing - White RHINO is a platform which aims to compete with commercial Whitespace devices. Hence, one has to ensure

Table. 9.2: Requirements: Performance

S.No	Requirement	Description	Met?	Remarks
1*	Transmit Power	30 dBm or 1 Watt	Met	The Transmit chain has a P1dB of over 2 Watts
2*	Bandwidth of Operation	512 MHz to 698 MHz	Met	There is a 6dB Gain Variation over the bandwidth of operation which has to be compensated through power control.
3*	Instantaneous Bandwidth	A minimum of 6 MHz	Met	The transmit power amplifier is capable of handling an instantaneous of bandwidth of 6 MHz.
4	Networking	2 X 1 Gbps Ethernet	Met	The 1Gbps operation of the Ethernet has been successfully tested.
5	Power Consumption	Less than 25 Watts	Met	The White RHINO board has not been tested to full utilization of power and power consumption is below 15 Watts. Theoritical projection 20 Watt.

that its performance is maintained even under extreme conditions. Meeting industry compliance will require rigorous testing under extreme weather conditions.

- Enclosure Design - The White RHINO mechanical enclosure is yet to be designed.
- PoE+ Board - The design and fabrication of the PoE+ board was defined to be beyond the scope of current masters dissertation and so, the PoE+ daughter board is another item that remains to be done.

Table. 9.3: Requirements: External Interfaces

S.No	Requirement	Description	Met?	Remarks
1	Power Supply	12 Volt External supply(AC-DC Adapter or Baterry powered) and Power Over Ethernet(PoE) capability	Met	-
2	Network Ports	2 X 1000 Base-T (Copper)	Met	-
3	User Interfaces	Universal Serial Bus(USB-UART) and Joint Test Action Group(JTAG) Interfaces	Met	Both the interfaces have been successfully tested
4	Air Interfaces	TV Whitespace and Global Positioning System(GPS) Antenna ports	Met	-

Table. 9.4: Requirements: Other

S.No	Requirement	Description	Met?	Remarks
1	Enclosure size	17cmx17cmx5cm	Met	The system can be conveniently fitted into a 17cmx17cmx5cm enclosure
2	Cost	Less than 1000 USD	Met	The overall cost of the White RHINO boards is less than 1000 USD

Appendix A

Zynq7000 Feasibility Calculations

The there two devices which have been provided in the user requirements. They are the Zynq7000 and the LMS6002 devices. While the LMS6002 with 300 MHz to 3 GHz band of operation and 28 MHz of maximum instantaneous bandwidth is a suitable device, it was necessary to perform the feasibility calculations for the Zynq7000 to verify if it would actually meet the hardware requirements.

In Figure A.1, we can observe the amount of resources present in the Zynq7020 device. We can see that it contains 53200 look up tables(LUTs), 106400 flip flops(FFs) and 220 DSP slices. In Figures A.2 and A.3, we show two sets of calculations. These calculations have been done to find out the amount of resources consumed for implementing the two most resource consuming blocks of the White RHINO. First is the covariance matrix generation using a single complex multiplier. We can see that, total time taken to perform this operation takes 559.24 ms and the amount of resources consumed are 0.27% LUTs, 0.27% FFs and 7.27% DSP slices. Then, we calculated the resources consumed for the transmit and the receive OFDM and the OFDMA respectively. These operations consume 3.32% LUTs,2.35% FFs, 1.82% DSP slices and 7.14% block RAMS. So, it takes up less than 4% LUTs, 3% FFs, 10% DSP slices and 8% block RAMs leaving out enough resources for the implementation of other block. Hence, the Zynq7020 has been deemed apt for the design of White RHINO.

Zynq-7000 Extensible Processing Platform					
	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix-7 FPGA	Kintex™-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(2)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600	218,600
	Flip-Flops	35,200	106,400	157,200	437,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)	2,180 KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	58 GMACs	158 GMACs	480 GMACs	1,080 GMACs
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security(1)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication			

Figure. A.1: Zynq Resources

COVARIANCE MATRIX GENERATION: TYPICAL COMPUTATIONAL TIME CALCULATION							
	Typical No. of Complex multiplications	Typical Clock Speed (MHz)	Typical Read/Write Access Times(2 Reads + 1 Write/ Multiplication)(msec)	Latency (Cycles)	Typical Latency (msec)	Typical Time required to compute all multiplications using a "Single Complex Multiplier"(msec)	Typical total time of computation (msec)
Covariance Matrix Generation	4194304	300	419.43	10	3.3E-05	139.81	559.24
Note: Typical Read/Write Instruction time is taken to be 10 cycles							

RESOURCES CONSUMED(with Single Complex Multiplier)				
	LUT/FF Pairs	LUTs	FFs	Xtreme DSP slices
Covariance Matrix Generation	150	145	285	16
Available Resources		53200	106400	220
% of resources consumed		0.27	0.27	7.27

Figure. A.2: Resource Utilization: Covariance Matrix Generation

The Xilinx LogiCORE™ IP Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm									
	Number of Points	LUT/FF Pairs	LUTs	FFs	Xtreme DSP slices	Block RAMs	Max clock freq(MHz)	Latency cycles	Latency @ max clock frequency(us)
OFDM Transmit	2048	1175	884	1249	2	5	395	26807	67.87
OFDM Receive	2048	1175	884	1249	2	5	395	26807	67.87
Total Resources consumed	2048	2350	**1768**	**2498**	**4**	**10**			
Available Resources			**53200**	**106400**	**220**	**140**			
% of resources consumed			**3.32**	**2.35**	**1.82**	**7.14**			

Figure. A.3: Resource Utilization: OFDM and OFDMA

Appendix B

Files Included on the CD

The following files have been included on the attached CD:

- WhiteRHINO_Dissertation - This document.
- WhiteRHINO_Manufacturing_files - Complete set of White RHINO and the White RHINO RF PCB manufacturing and assembly files. These are the updated version 1.0 files.
- WhiteRHINO_Softwares - Contains all the softwares used for the testing of White RHINO. They are the U-Boot image, the Linux image and other application softwares.

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