Dynamic Modelling and Emulation of a High Temperature Proton Exchange Membrane Fuel Cell (HT PEMFC)

By

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DECLARATION

The thesis is submitted for the fulfilment of the requirements for the degree of Master of Science in Electrical Engineering at the University of Cape Town. It has not been submitted before for any degree at this or any other university. The author confirms that he knows the meaning of plagiarism and declares that all the work in the document, save for that which is properly acknowledged, is his own.

Chris de Beer

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Supervisor: Dr. P.S. Barendse
Co-Supervisor: Dr. M.A. Khan

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SUMMARY

Fuel cells (FC) are power sources that convert chemical energy into electrical and thermal energy in a clean and efficient manner. In the 21st century, fuel cells appear poised to meet the power demands of a variety of applications, ranging from portable electronics to utility power plants. Compared to systems utilizing fossil fuels, fuel cells offer greater efficiency and superior reliability. In particular, proton exchange membrane FCs (PEMFCs) presents a good alternative energy source for distributed generation (DG) systems.

FCs however, have had limited commercial success despite their performance, durability and low environmental impact in comparison to other energy conversion and power generation devices. This lack of success has led to low commercial production levels resulting in high costs. Therefore, an increase in research and development is being conducted with the aim of producing cost effective, more efficient and reliable fuel cells for portable transportation and stationary applications.

This dissertation aims to produce an emulator design for a HT PEM FC system. A model is developed that takes into account the steady state and the dynamic characteristics of the fuel cell. The emulator hardware is developed from first principles and tested to evaluate performance under dynamic operating conditions. Phenomena such as polarization curve hysteresis and fuel starvation is investigated, simulated and reproduced with the emulator system. The experimental results are compared with that of an actual HT PEM FC stack and evaluated.

It was shown that the final system is able to deliver accurate steady state and transient state outputs when compared with the fuel cell stack. The final design can be used for hardware in the loop applications, specifically for fuel cell power conditioning system development.

TABLE OF CONTENTS

NOMENCLATURE

Symbol	Unit	Definition
A_l	nH/turn^2	Normalized inductance
C_{cdl}	F	Charge double layer capacitance
C_{dc}	F	DC link capacitance
C_t	F	Thermal capacitance
D		Duty ratio
E_m	V	Peak line to neutral voltage
E^0_{rev}	V	Reversible cell potential at standard operating conditions
F		Faraday's constant
f_{sw}	Hz	Switching frequency
i	A/cm^2	Cell current density
i_d	A	Direct axis current
i_0	A/cm^2	Exchange current density
i_{lim}	A/cm^2	Limiting current density
i_L	A	Inductor current
i_q	A	Quadrature axis current
K_I		Integral gain
K_P		Proportional gain
L_{eq}	H	Equivalent system inductance
L_n	H	Inductance per phase
N_{cell}		Number of series cells in the FC stack
P	atm	Gas pressure

Symbol	Unit	Definition
R		Universal gas constant
R_c	Ω	Capacitor series resistance
R_l	Ω	Inductor series resistance
R_{ohm}	Ω	Cell ohmic resistance
S		Entropy
s		Laplace operator
T	K	Temperature
T_s	s	Sampling time
T_{sw}	s	Switching time
U_{act}	V	Cell activation voltage
U_{conc}	V	Cell concentration voltage
U_f	%	Utilization factor
U_{rev}	V	Reversible open circuit voltage
U_{ohm}	V	Cell ohmic voltage
V	slpm	Flow rate
V_t	V	Terminal voltage of the FC stack
z		Number of electrons
ρ	atm	Partial pressure
τ_a	s	Anode flow delay
τ_c	s	Cathode flow delay
ω_c	rad/s	Cut-off frequency
ω_{cr}	rad/s	Crossover frequency
φ	°	Phase margin

1. INTRODUCTION

I. MOTIVATION

As we further proceed into the 21st century, the demand for oil, coal and other fossil fuel sources will continue to soar. This is attributed to the global economies and the world population. It is this demand that has spurred the research and development of new energy technologies that will supply future energy markets.

Renewable energy systems have become a viable solution for sustainable development. The increased market share and production has led to a reduction in the $/kW index for renewable energy products. The most promising of these was hydrogen, since it is the most abundant element on earth and has vast potential as an energy carrier.

The production of hydrogen gas through the use of solar, wind and other renewable electrical power sources is possible through a simple electrochemical process known as electrolysis. The hydrogen can then be stored or transported to remote areas where there is limited or no existing electrical infrastructure. By re-combining the hydrogen gas with oxygen, electrical and thermal power can be produced with water as the only by product. The electrochemical devices responsible for the realization of this process are known as fuel cells. The fuel cells are thus electrochemical power generators with a wide variety of uses as will be explained in the following chapters.

Each of these systems has a large number of internal mechanisms that influence the quality and output power capability, which makes the system rather complex. Since the primary purpose of the fuel cell system is to produce electricity, it is critical that the output be regulated to the specifications of the load. This is achieved through the use of power conditioning systems. To facilitate and reduce development times, emulator systems are used as a replacement during the prototyping phases.

II. BACKGROUND

Hydrogen South Africa (HySA), a subsidiary of the department of science and technology in South Africa, was formed to conduct research and development on a HT PEM FC system that will form part of a combined heat and power (CHP) solution.

The majority of the literature is focused towards LT PEM fuel cells, however very little has been done on the HT PEM FC systems. Working at higher operating temperatures has inherent advantages and will be highlighted throughout this dissertation.

The use of emulator systems allows designers to quickly make changes in operating conditions to evaluate the effects on the output and performance. For applications such as the automotive industry, the effects of transient loads on the output of the fuel cells are of great concern.

III. PROBLEM STATEMENT

The objectives of this research are as follows:

- Develop an understanding of PEM FC system with emphasis on high temperature operation;
- Produce an accurate HT PEM FC model that can predict the steady state and transient behaviour that may be easily implemented in a real time processing platform;
- Conduct a literature survey on emulator systems and highlight the shortcomings of each;
- Design a new emulator topology that improves performance when compared to existing systems;
- Design the control systems that interface with the fuel cell model to accurately reproduce the output of the fuel cell system;
- Investigate dynamic phenomena that occur during normal fuel cell operation and reproduce the effects in real time with the emulator system.

IV. CONTRIBUTIONS

The major contributions made by this research include the development of an HT PEM FC model that incorporates the effects of the three main dynamic domains, and the design of a new two stage emulator topology based on the multiphase interleaved synchronous buck. Concepts such as critical inductance are used to improve the dynamic performance of the system without compromising the quality of the output. The effects of polarization curve hysteresis, frequency response and fuel starvation on the fuel cell output is reproduced and demonstrates the ability of the emulator to replace an actual fuel cell during interface hardware and control system development.

V. RESEARCH APPROACH

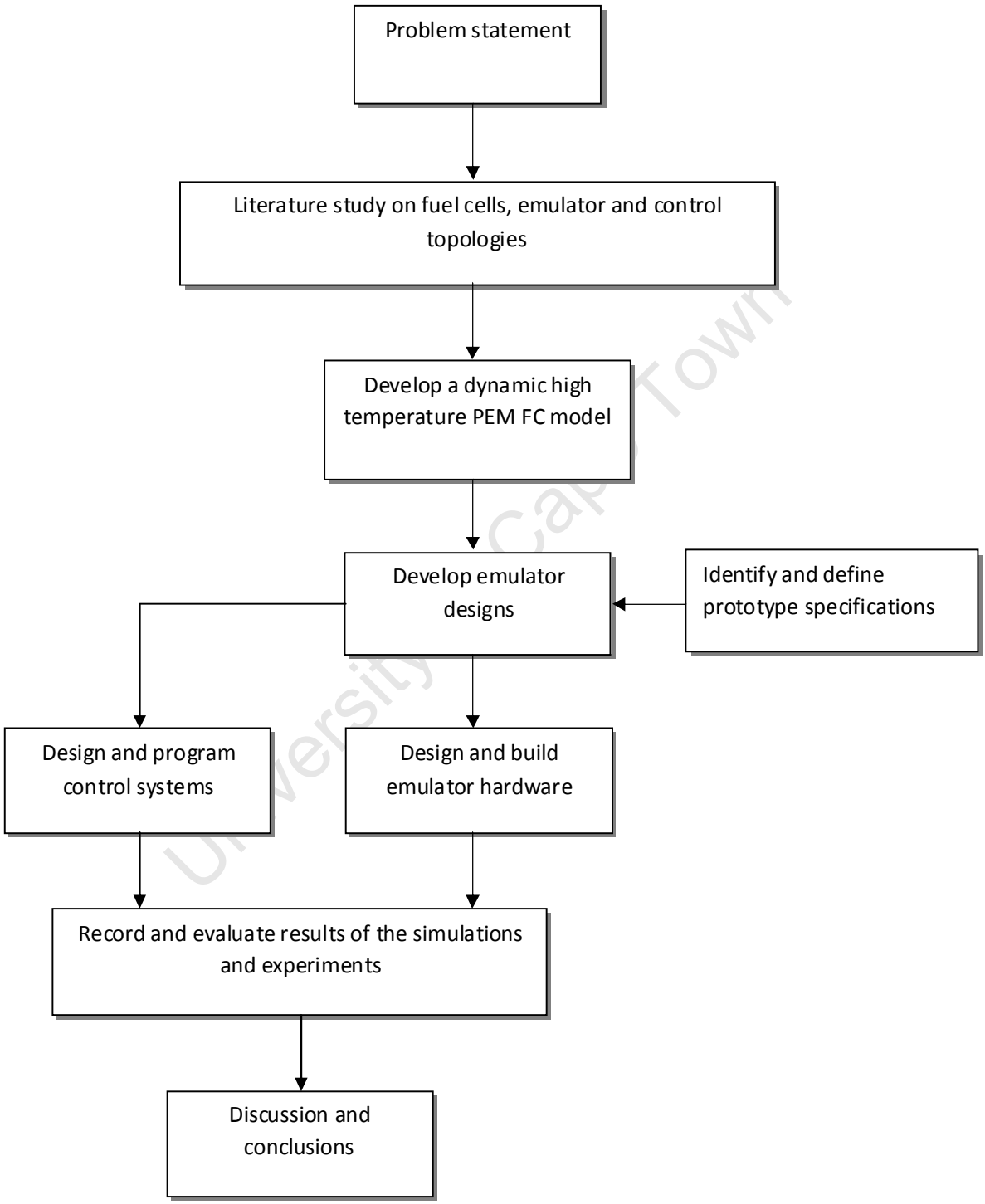

Figure 1.1. Research approach for the dissertation.

The identification of the research problem forms the first step of the research approach and also defines the research goals. The problem statement formulated in section 1.3 is the result of the first step and defines the outcomes of the work.

The literature study is performed to gain an understanding of the operation of the internal chemical and electrical characteristics of a fuel cell system. This leads to the derivation of the mathematical model that will be implemented in the emulator. The literature survey also gives background information on the existing emulators and their limitations.

The next steps involve the design of the emulator. A detailed analysis on the topology is conducted to determine the best design to meet system specifications. The control systems are developed to meet requirements and tuned until satisfactory results are obtained. The filter components and hardware are designed according to the system specifications identified.

Following the modelling and design stages of the emulator, a prototype is built and tested. The results of the experiments are recorded and compared to that obtained from the model and the experimental fuel cell stack. Comparisons and deviations are discussed and commented upon. Based on the outcome, it can be decided if the emulator meets the required operational capability and can successfully reproduce the electrical output of an actual fuel cell system.

VI. LIMITATIONS OF THE RESEARCH

The following limitations are applicable to the experimental prototype, HT PEM FC model and the research in general:

- The model derived is applicable to HT PEM fuel cells only and cannot represent the low temperature counterpart;
- The control systems were designed according to recognised methods and were adapted to be practically implemented on the dSpace DS1104 platform;
- The testing of the system is performed under laboratory conditions and no attempt is made to recreate industrial operating conditions.

VII. DISSERTATION OUTLINE

The second chapter presents a literature survey on fuel cell systems and the modelling and characterization methods employed to represent them. The dominant voltage loss mechanisms and the mathematical expressions used to represent them are also presented.

Chapter 3 presents the developed HT PEM FC model and the simulated results obtained for both the steady state and transient domains. The three main dynamic components are identified and integrated with the model components. Selected operational phenomena that can occur in the fuel cell are presented and simulated using the developed model. The results are compared to that available in literature for similar tests conducted on fuel cell systems.

Chapter 4 presents an overview of existing and the proposed emulator topology. The shortcomings of the existing systems are highlighted and used to justify the use of the proposed system. In particular, the two stage approach allows the double phase interleaved DC-DC converter to run at an optimal operating point. The operation of the system is discussed and the benefits are quantified.

The control systems are designed for each of the two stages of the emulator in chapter 5. Recognised design methods are employed to arrive at a starting point for the controller gains used during experimental implementation. The open loop response of the prototype converters is presented, discussed and used to determine a final design. The closed loop response of the vector control system is presented, which demonstrates the stability of the system under transient states.

The design of the hardware for the emulator system is discussed in chapter 6. The experimental results obtained from the initial prototype system is shown and used to design the final emulator hardware. The filter components were designed to meet both steady state and transient requirements.

Chapter 7 presents the experimental results obtained from the complete emulator. Both steady state and transient test results are shown and compared to the simulated results and the test results obtained from the HT PEM FC stack. The performance of the system is then discussed.

Chapter 8 is a summary of the work and a discussion. The shortcomings of the system are identified and future work is recommended.

2. FUEL CELLS AND MODELLING APPROACHES

I. INTRODUCTION

Fuel cells are currently one of the leading technologies that generate electrical energy by converting various sources of fuels to electricity without the need for combustion. The different types currently available or in development are polymer electrolyte fuel cells (PEMFC), direct-methanol fuel cells (DMFC), solid oxide fuel cells (SOFC), phosphoric acid fuel cells (PAFC), molten carbonate fuel cells (MCFC), alkaline fuel cells (AFC), photonic ceramic fuel cells (PCFC) and zinc-air fuel cells (ZAFC) [1]. Current applications for fuel cells include transportation systems, stationary power sources as well as portable communication systems.

The many fuel cell models and emulator systems available in literature were developed for low temperature fuel cell systems. These are thus not applicable to the high temperature counter parts as the operating philosophy and operating parameters are different. The methods used to derive these models can however be applied on the high temperature systems.

The electrical output characteristics of the HT PEMFC systems can be expected to behave in a similar manner to the low temperature systems as observed in the available literature. There are however, applications such as combined heat and power (CHP) systems, whereby the system model must be flexible enough to adapt and incorporate the operating principles behind such a system. This chapter presents the operation of a PEM fuel cell and the subsystems required. A brief overview of high temperature systems is given where after the different modelling approaches for the electrochemical system is discussed. The dominant loss mechanisms, governing equations and testing methodologies to determine model parameters are described.

II. FIELDS OF RESEARCH IN PEM FUEL CELL TECHNOLOGY

A. Fuel cell development

The proton exchange or polymer electrolyte fuel cell (PEMFC) is considered to be the one of the most promising of the fuel cell technologies. This type of fuel cell has a long cell life and a high current density. This enables it to perform well as a portable power source or a medium voltage power generation system [1].

PEMFCs use hydrogen and oxygen as the primary fuel source. In the past, hydrogen was produced by the steam reforming of hydrocarbons such as natural gas or by the gasification of coal. These processes generate high carbon dioxide emissions as well as carbon monoxide which are known to increase the risk of anode electro-catalyst poisoning.

Hydrogen can also be generated from wind and solar power by using water electrolysis. PEM fuel cells operating from these hydrogen sources are classified as renewable energy sources since no fossil fuels are utilized to generate electrical power.

PEM fuel cells have a hydrated polymer membrane that is situated between two electrodes [2], [3]. The membrane acts as an electrolyte and a filter, allowing hydrogen ions to flow and forcing the electrical current out of the cell via the anode to the external circuit as shown in figure 2.1. The catalytic electrodes consist of activated carbon and finely dispersed platinum at the electrode-electrolyte interface [3]. A single cell generates a very low open circuit voltage, typically in the range of 1.2V. To generate significant output voltage and power, the cells are stacked in series separated by bipolar plates.

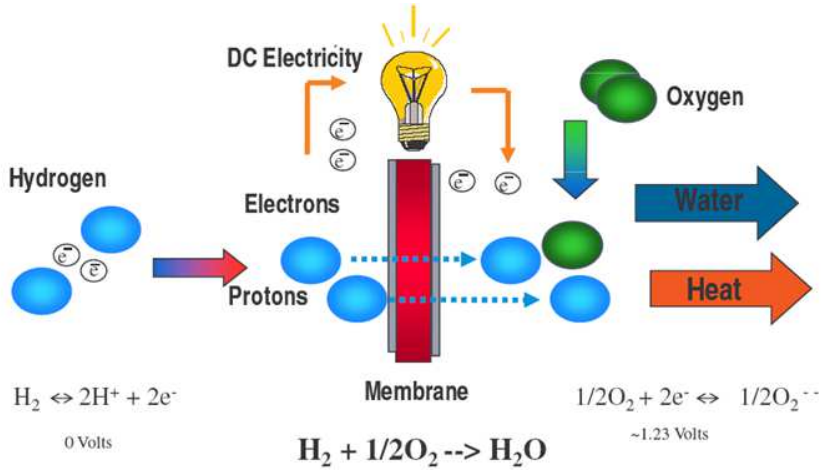

Figure 2.1. Representation of PEM FC reaction.

The cells themselves can be considered as the power source of the fuel cell system. A large amount of research and development has been carried out to increase reactant flow, power density and efficiency by developing new materials for the cell components. The fuel cell as a whole however, consists of many subsystems that control temperature, pressure, humidity and the output power as shown in figure 2.2[4].

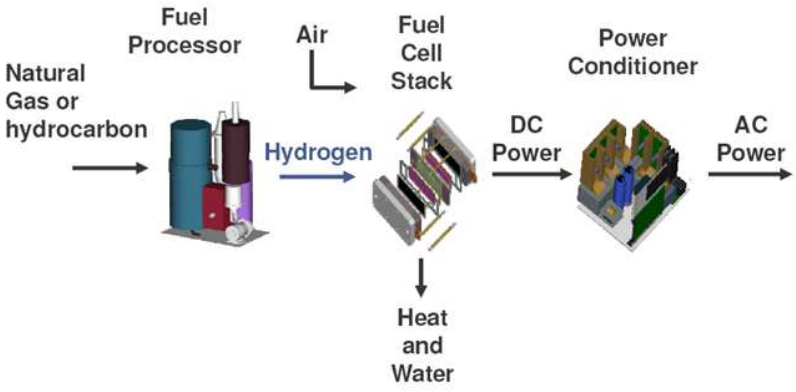

Figure 2.2. System representation of a PEM FC.

Many mathematical models for the dynamic behaviour of the chemical systems are available in the literature [5], [6] and have been incorporated into global models for the fuel cell systems. These have been developed to optimize control systems for the compressor, humidifier and valve controllers [4], [7].

B. Advantages of high temperature operation

Generally PEM fuel cells operate at temperatures lower that 100°C and are classified as normal or low temperature fuel cells. The most recent research has focused on the development of cells that operate at higher temperatures [8]. The most compelling advantage of HT operation is improved efficiency and power density mainly due to the enhanced electrochemical kinetics, simplified water management and a simplified cooling system [8]. High temperature operation also increases CO tolerance and reduces the amount of stack poisoning. This also allows the cell to operate from hydrogen generated from a standard reformer.

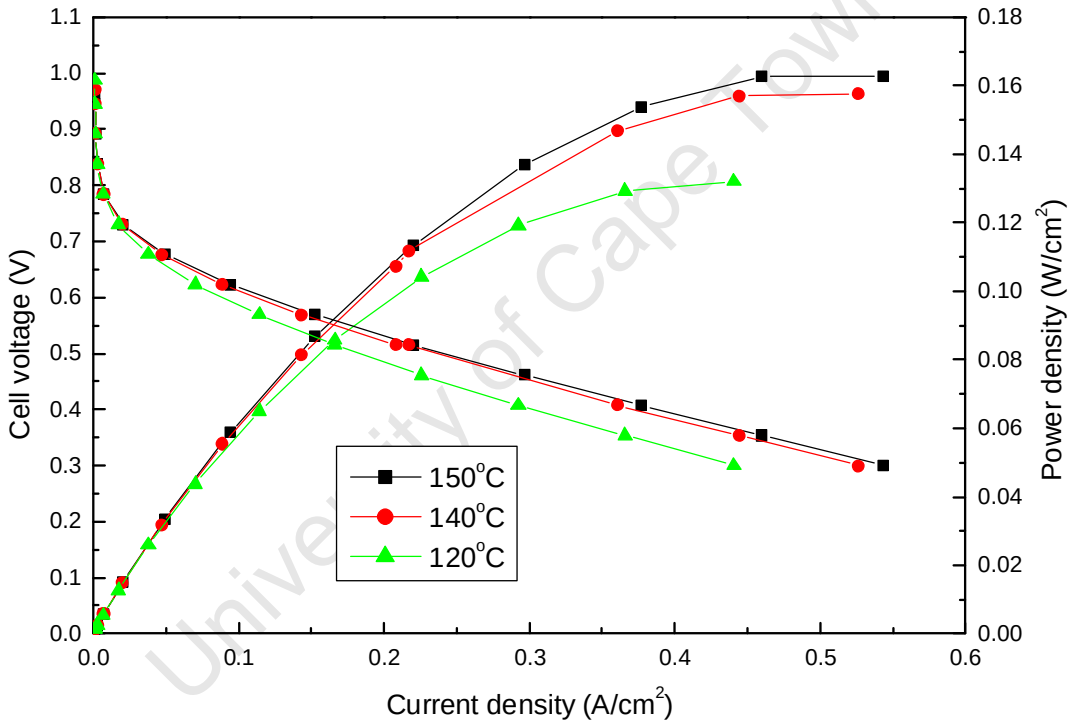

Figure 2.3. Polarization and power density curves for a HT PEMFC at different operating temperatures.

III. BACKGROUND OF MODELLING

Various models that describe the dynamic and static behaviour of the fuel cell have been developed in recent years. These models can generally be grouped into two categories namely

semi-empirical models, which have been derived from experiments, and theoretical models based on laws of conservation [9].

The most recent models available in literature are quite complex and take into consideration a large number of parameters. These are based on previous models which were much simpler and sequentially built into more comprehensive models. Some of these improvements include enhancing physical factors that were previously assumed to be constant that are now modelled as dynamic. Also, the effects of stack temperature and pressure on internal resistance were eventually incorporated by forming semi-empirical mathematical models based on curve fitting techniques [9].

Full three dimensional models that incorporate non-linear effects and equations are presented in [5]. Individual cells are usually characterized by some form of the Nernst and Tafel equation [5], [7], [9] that calculate the voltages by taking into account gas temperatures, pressures, concentrations and polarization effects.

Many thermodynamic models are described in the literature. They are however very specific to the particular fuel cell under investigation and is not applicable to all types of commercially available systems [4]-[9]. The most recent publications incorporate many variations on the pressure and temperature such that the models become very complex and difficult to integrate into control and emulator system models.

Migrating to high temperature operation has presented grounds for developing new models and formulae because of the large variation in physical parameters and complexity of materials when compared to the low temperature systems. The introduction of computational fluid dynamics (CFD) and improved transport models have produced more realistic computer simulations [10], [11].

The charged double layer effect, where the interface between the electrodes and the electrolyte stores a large amount of charge, is taken into account by modelling it as a capacitive element within the circuit. Most high temperature models incorporate the Butler-Volmer equation to model electrode current densities. Arrhenious equations are used to model the temperature dependence of the ionic conductivity of the membrane [10], [11].

IV. EMPIRICAL MODELLING METHODOLOGIES

A. V-I curve evaluation

The analysis and interpretation of the polarization or voltage-current curves of a fuel cell is one of the most widely used characterization methods for a fuel cell. The curve is obtained by varying the load or the output current of the fuel cell while keeping the main operating characteristics constant. This includes the gas pressure, gas concentration, stack operating temperature and the cell humidity.

The three main loss mechanisms can be identified and quantified from the resulting curves as shown in figure 2.4. The first is often referred to as the activation loss and occurs at low current densities. During start-up of the electrochemical process, a finite amount of energy is required to start the chemical reaction. This is also known as the threshold energy [12]. This phenomenon mainly occurs at the electrode-electrolyte interface and is also known as the initial charge transfer loss. The ohmic losses occur in the linear region and are a function of the internal cell and external component resistances. At high current densities the voltage will start to decay exponentially, as shown on the polarization curve, as a result of concentration losses.

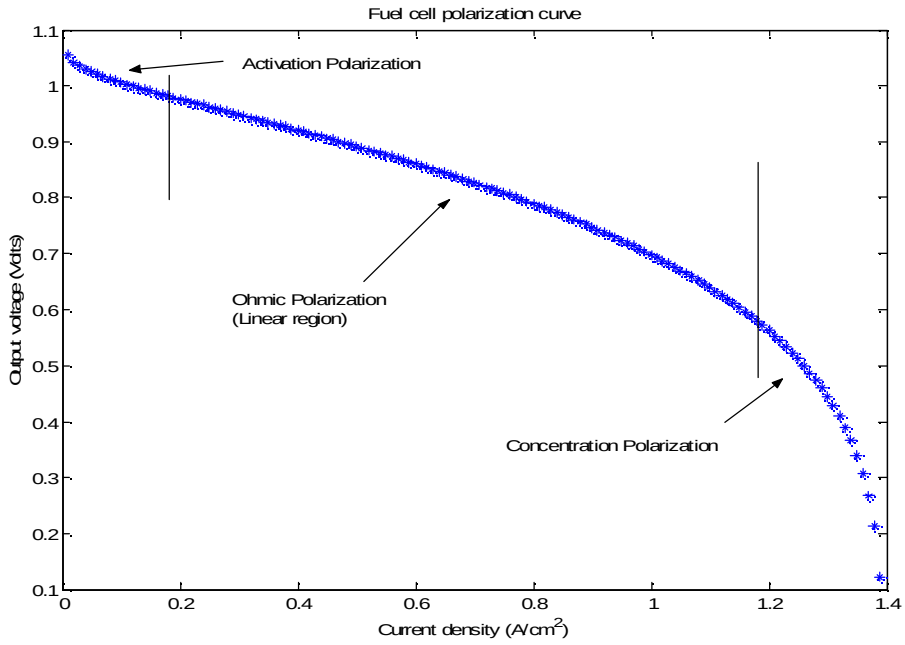

Figure 2.4. Polarization curve defining the different operating regions [13].

The output power of the fuel cell stack can be calculated by multiplying each of the obtained operating points with the number of cells in the stack and the area of the cells. This produces the power curve of the fuel cell as shown in figure 2.5. It is clear that there exists a maximum power point on the curve.

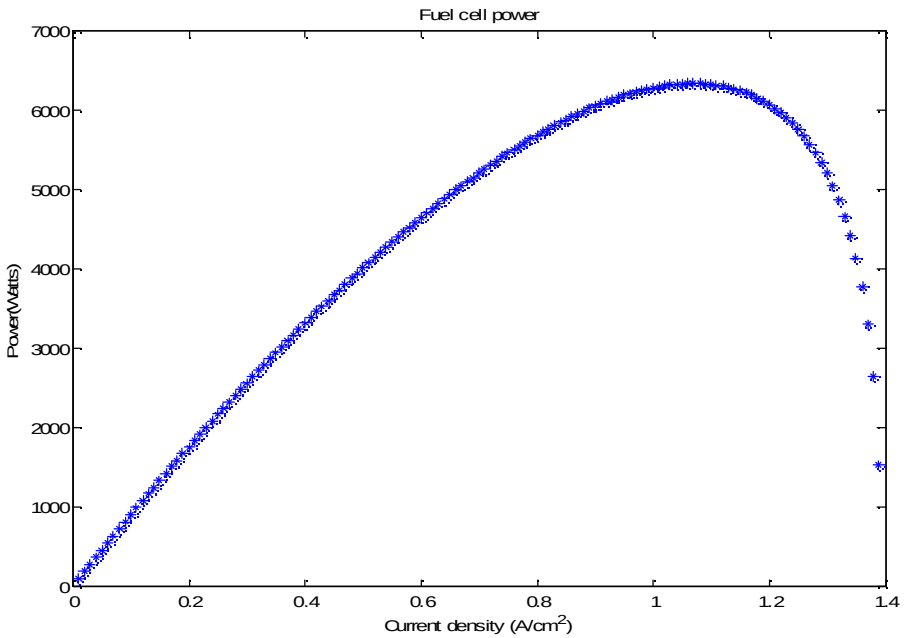

Figure 2.5. Output power vs. current density for a PEM FC [13].

The activation voltage drop is calculated as follows:

$$U_{act} = \frac{RT}{F} ln(^{i}/_{i_0}) \tag{2.1}$$

where i represents the cell current density, R the universal gas constant, T the temperature in Kelvin, F is Faraday's constant and i_0 depends on the characteristics of the electrode. For a platinum electrode i_0 can be described as follows:

$$i_0 = i_{0pt} S_{pt} W_{pt} U_{pt} \tag{2.2}$$

where i_{0pt} represents the exchange current density for a platinum catalyst, S_{pt} is the surface area of the platinum catalyst, W_{pt} is the catalyst loading and U_{pt} is the catalyst loading factor.

The activation potential can be modelled as a current and temperature dependant voltage source as shown in figure 2.6.

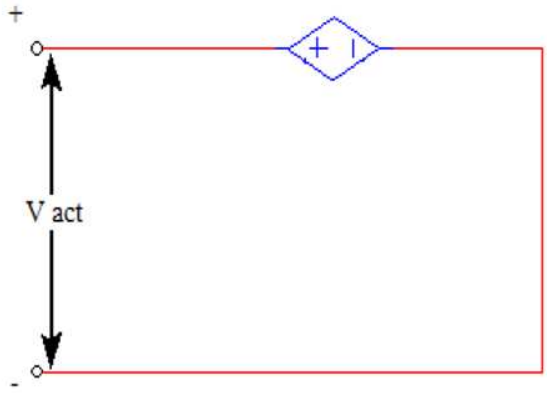

Figure 2.6. Circuit representation of the activation potential.

The linear decrease in voltage as shown in figure 2.4 is mainly due to the membrane ionic resistance as well as the electrical resistance of the current collectors and the electrodes. These losses are usually modelled as current dependant resistors as shown in figure 2.7.

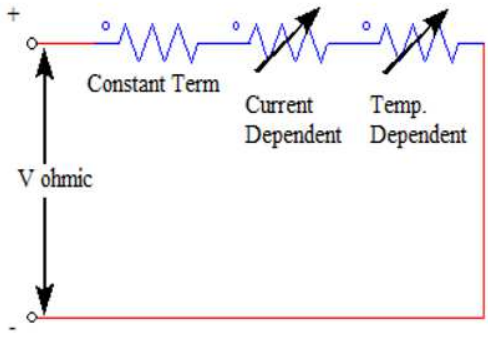

Figure 2.7. Circuit representation of the ohmic voltage drop.

$$U_{ohm} = i(a_{ohm} + Ta_{ohm1}) \tag{2.3}$$

where a_{ohm} represents constant resistance of the components and a_{ohm1} the temperature dependant resistance.

At high current the voltage starts to drop dramatically. This is generally referred to as the concentration voltage drop or the diffusion/mass transport loss. The concentration voltage drop is

caused by the inherent limits of the chemical system and is classified as the limiting rate at which the products and reactants are transported from the active areas. The circuit representation of this loss is shown in figure 2.8.

The concentration voltage drop is calculated as follows:

$$U_{con} = \frac{RT}{zF}\ln(1 - {}^{i}/_{i_{lim}}) \tag{2.4}$$

The term i_{lim} refers to the limiting current of the system and z the number of electrons taking part in the reaction. If this is exceeded the output voltage will become zero.

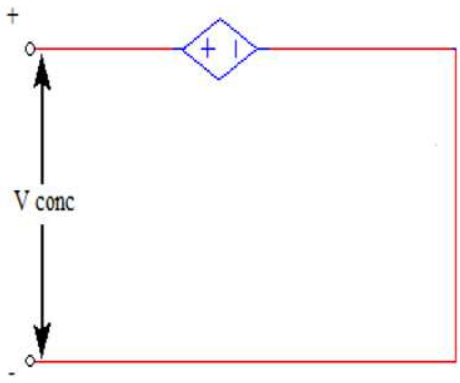

Figure 2.8. Circuit representation of the concentration voltage drop.

The total output voltage of the stack can thus be defined as follows:

$$V_T = N_{cell}(U_{rev} - U_{ohm} - U_{act} - U_{conc}) \tag{2.5}$$

where N_{cell} represents the number of series cells in the stack and U_{rev} represents the theoretical open circuit voltage as derived from the Nernst equation:

$$U_{rev} = 1.23 - 0.9 \times 10^{-3}(T - 298) + \frac{RT}{2F}\ln\left(\frac{\rho H_2 \rho {O_2}^{1/2}}{\rho H_2 O}\right) \tag{2.6}$$

where ρ represents the partial pressure of the different gas species.

B. EIS method

The electrochemical impedance spectroscopy (EIS) or AC impedance injection method is generally accepted as a more accurate method for determining fuel cell characteristics and producing an equivalent stack model. Figure 2.9 depicts the experimental set-up for and EIS test.

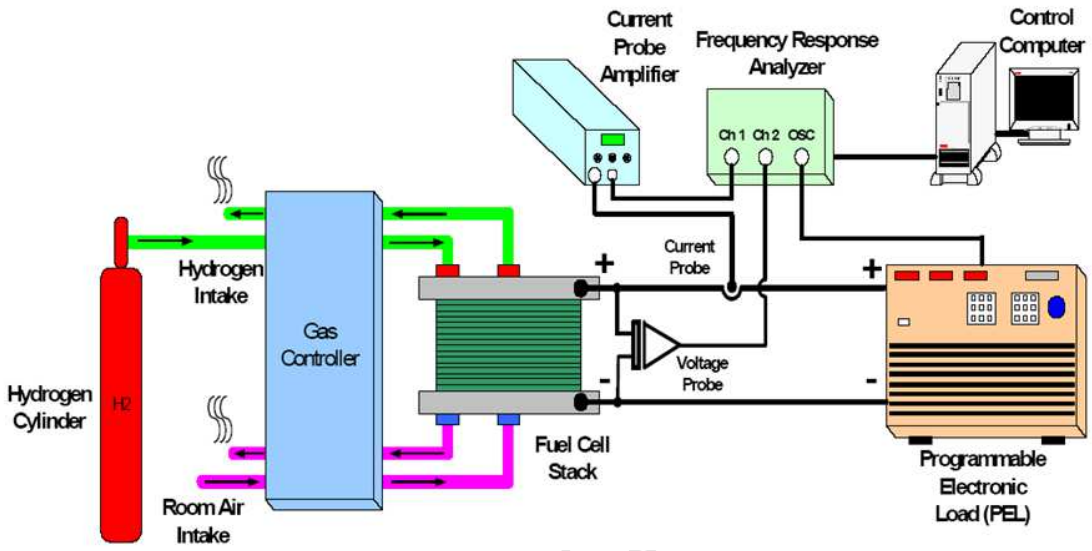

Figure 2.9. Test setup for the EIS method [14].

The impedance spectrum in the form of a Nyquist plot is generated by injecting a low amplitude voltage or current into the cell while it is operating at a certain load point on the V-I curve. The voltage or current response is measured and the impedance is calculated from the amplitude and phase angle. To obtain a full frequency spectrum the frequency of the input signal is varied, typically between 10mHz and 100kHz [3]. The amplitude of the injected signal is adjusted so that it does not disturb the normal operating voltage of the fuel cell.

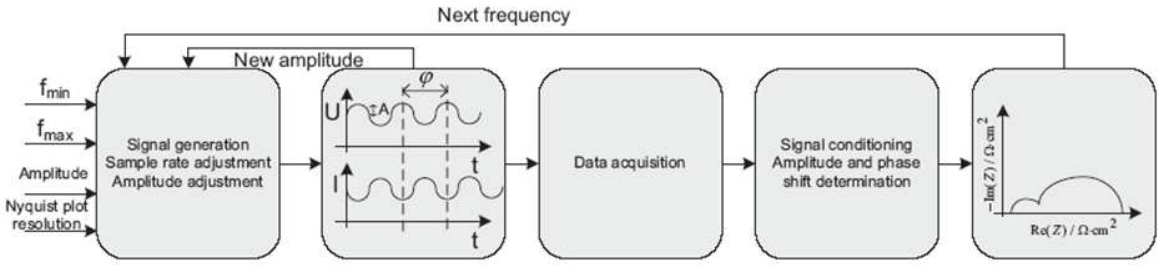

Figure 2.10. EIS operating principle [14].

The EIS method quantifies the loss mechanisms with respect to a certain frequency range. Typically, the impedance measured at low frequencies mainly result from the membrane ionic resistance. The impedance in the mid frequency range results from the charge transfer resistance and at high frequencies from mass transport or diffusion losses.

The equivalent fuel cell model can be obtained by following a curve fitting procedure that will generate a similar frequency response as the actual system. This method is limited to the number of operating parameters which might be considered. During testing, these parameters are kept constant and produce a single Nyquist plot. If the pressure, temperature or any other parameter is adjusted the obtained Nyquist plot will shift as seen in fig. 2.11, for a change in temperature. This method is thus limited in terms of the active elements of the fuel cell system and the dynamic response.

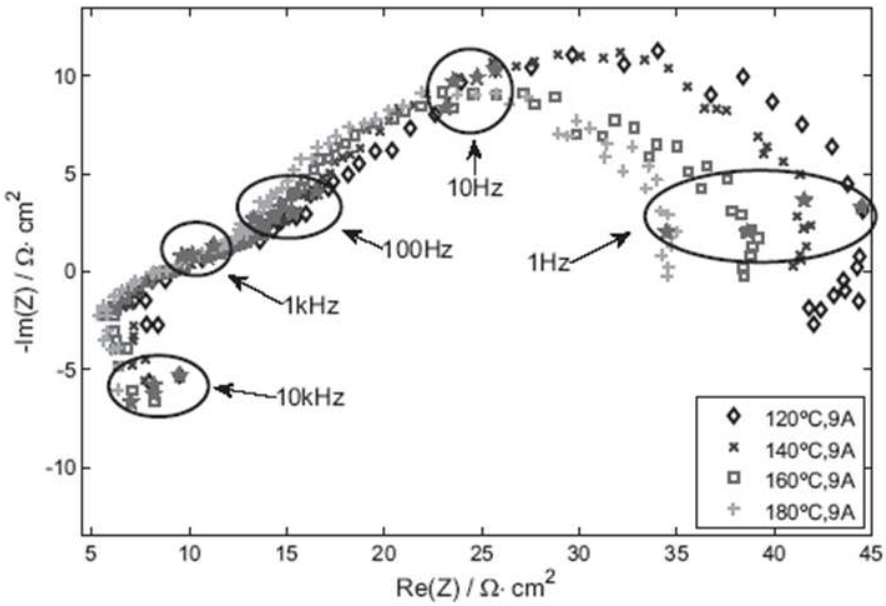

Figure 2.11. Nyquist plot of a HT PEMFC at different operating temperatures [14].

C. Current interrupt method

The current or pulse interrupt method is a much simpler methodology to employ than the EIS method and does not require the complex equipment associated with EIS. This method requires that the operating fuel cell be subjected to a sudden step change in load while measuring the

resulting voltage transient response. Another variation subjects the fuel cell to a short duration current pulse.

Figure 2.12 represents the voltage response for a sudden step change in current for two different reactant flow responses. It can clearly be seen that the dynamic response of the fuel cell system is greatly dependant on the characteristics of the subsystems. The current interrupt method can be employed to generate accurate models not only for the fuel cell but also for the compressor and some of the other subsystems. It is the most widely used method for developing dynamic models of fuel cell systems [3], [4] and [15].

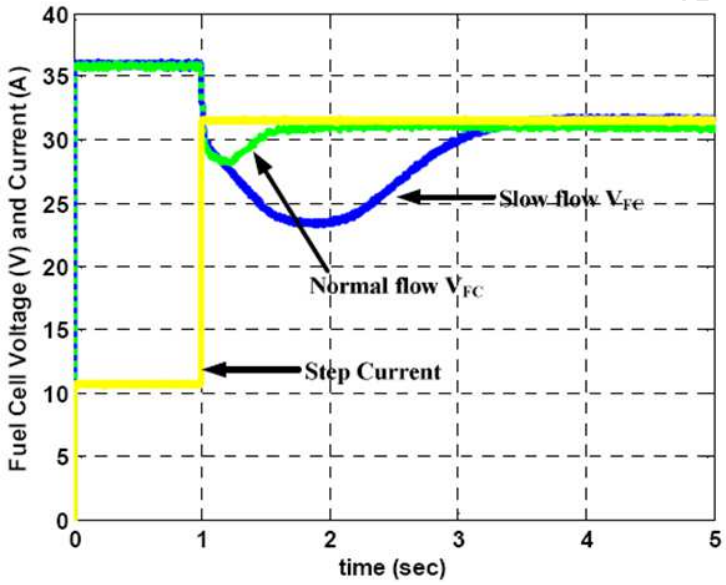

Figure. 2.12. Output from a current interrupt test [4].

The step response is used to calculate the ohmic resistance, from the instantaneous voltage drop, and the charge transfer loss, from the gradual change in potential as it approaches steady state. Another phenomenon that has been quantified by use of this method is the charge double layer effect and is represented by the knee point characteristics before steady state is reached.

Another variation of the current, pulse interrupt method has been used in [3] to derive an equivalent circuit model. In essence, the cells are connected to a test circuit as indicated in figure 2.13. The cells are charged through a resistor R_{charge}. Once steady state is reached, switch S_1 is

opened and the cells are placed in open circuit. After a specified time a step change in load is applied via the discharge resistors.

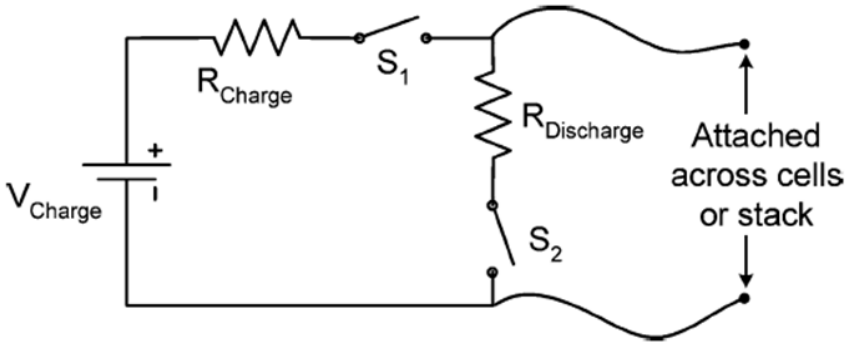

Figure 2.13. Test setup of the proposed current interrupt method in [3].

From the results obtained, as shown in figure 2.14, they have identified the four regions of interest. This corresponds to the behaviour of a double layered capacitor and is modelled accordingly. The most noticeable characteristic is the self recharge region. This is due to a small amount of charge that is still present after the step load is removed. This coupled with the decreasing dielectric constant will result in this rise in potential.

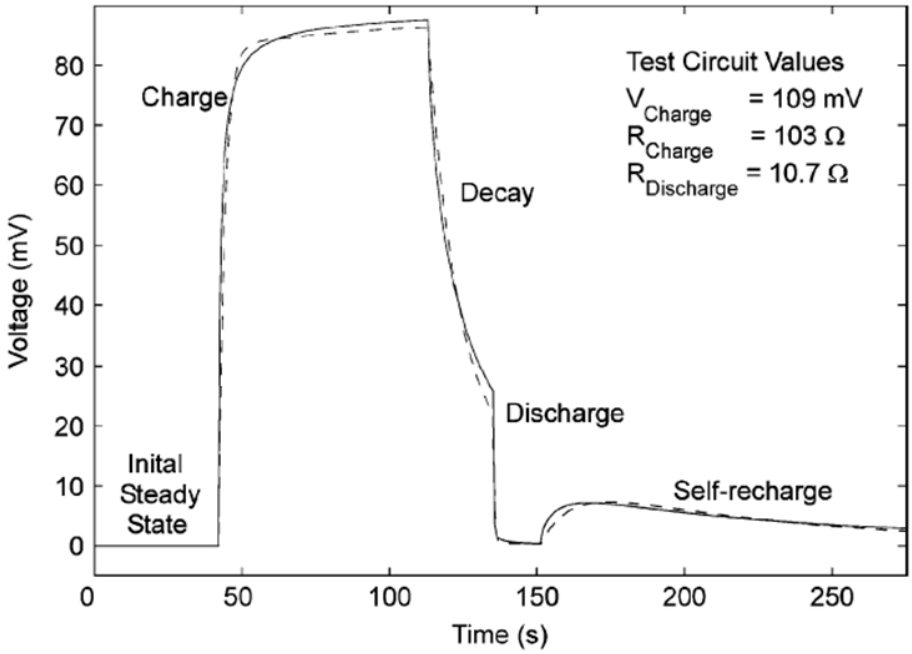

Figure 2.14. Results obtained from the proposed current interrupt method in [3].

D. Cyclic Voltammetry

Cyclic Voltammetry is a technique used to quantify the electrochemical surface area of the gas diffusion electrodes [16]. A linear voltage sweep with respect to time is performed while the current is measured as shown in figure 2.15. When a potential is reached that relates to an electrochemical reaction, the current will peak and then stabilize once all the reactants have been depleted. These peaks are related to the diffusion and reaction rates of the chemical system.

CO stripping voltammetry is another technique used to quantify the electrochemical surface area.

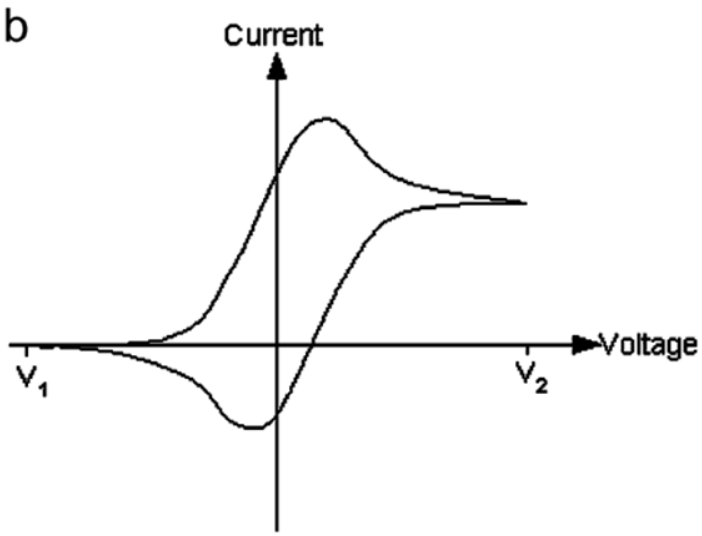

Figure 2.15. Current vs. voltage output from the cyclic voltammetry test [15].

E. Other analytical methods used

Other test methods used to characterize fuel cells include pressure drop analysis, polarization curve hysteresis, current density mapping, temperature mapping, flow visualization, neutron imaging and magnetic resonance imaging [17]. Most of these methods require very complex equipment to perform the tests as well as great computing power. Each of the methods is specialized to quantify only a specific set of parameters.

V. ANALYTICAL MODELLING

Ab initio or analytical modelling of fuel cells is a full theoretical approach to producing a complete multidimensional mathematical model for the fuel cell stack. This is accomplished by formulating the appropriate mass and energy balance equations and following the laws of conservation.

The ohmic resistance of the cells are calculated as follows:

$$R_{ohm} = \int_0^{Lm} \frac{dx}{A_m \sigma T_{op}(x)} \tag{2.7}$$

where σ is the membrane conductivity at the specified operating temperature, L_m is the thickness of the membrane and A_m is the effective area of the membrane.

The activation voltage is modelled as follows:

$$U_{act} = \gamma_1 + \gamma_2 T_{op} + \gamma_3 T_{op} \log(c_{o2}) + \gamma_4 T_{op} \log(I) \tag{2.8}$$

where the coefficients, γ, are dependent on individual cell characteristics [2]. The characteristics of an individual fuel cell can be represented via the following equation:

$$U_{cell} = U_{rev} - U_{act} - U_{ohm} - U_{conc} \tag{2.9}$$

The above model represents only the cathode catalyst kinetics and incorporates a number of assumptions including constant temperature and total system pressure.

The influence of CO and CO_2 on the anode catalytic layer can be incorporated into the cathode model via the following equations:

$$U_a = \frac{RT}{\alpha F} \arcsin h \left(\frac{i}{2k_{eh}\theta_H}\right) \tag{2.10}$$

The coverage of hydrogen, θ_H, and CO at steady state are described as a set of differential equations in [18].

The open circuit voltage of the fuel cell is described as follows:

$$U_{rev} = E_{rev}^{0} + \left(\frac{\Delta S}{zF}\right)_p (T - 298) + \frac{RT}{2F} ln\left(\frac{p_{H2} {p_{O2}}^{1/2}}{p_{H2O}}\right) \tag{2.11}$$

The change of entropy, ΔS, as a function of temperature can be expressed as follows [11]:

$$\Delta S = 33.64 + 4.52564 \times 10^{-2} T - 2.98397 \times 10^{-5} T^2 + 3.40625 \times 10^{-9} T^3 - 2.60417 \times 10^{-12} T^4 \tag{2.12}$$

Equations 2.7 to 2.12 give a fairly accurate polarization curve of a low temperature fuel cell at different operating temperatures. Another type of analytical model that can provide a more accurate dynamic response and takes into account the contour of local current densities, the charge double layer effect and the electrolyte phase potential is presented in [10], [11]. This method calculates the resulting current density at a specific cell operating voltage while the previous model calculates the resulting cell voltage as a function of cell current and losses.

The normal current density in the membrane is calculated as follows:

$$I_{avg} = \frac{1}{A_{mem}} \int_0^{A_{mem}} I \; dA \tag{2.13}$$

where A_{mem} is the active area of the cell and I is the local current density of the membrane and is defined as follows:

$$I = -\kappa_{mem} \nabla \emptyset_{mem} \tag{2.14}$$

The membrane ionic conductivity as a function of temperature is described by the Arrhenius equation:

$$\kappa_{mem} = \kappa_0 exp\left[-\frac{E_{A,\kappa}}{R}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right] \tag{2.15}$$

where $E_{A,k}$ is the activation energy and κ_0 is the pre-exponential factor at reference T_0.

The anode and cathode current densities are described by the Butler-Volmer equations:

$$j_a = i_a^{ref}\left(\frac{pH_2}{p^0H_2}\right)^{\beta}\left[exp\left(\frac{\alpha_a F\eta_a}{RT}\right) - exp\left(-\frac{\alpha_c F\eta_a}{RT}\right)\right] \tag{2.16}$$

$$j_c = i_c^{ref}\left(\frac{pO_2}{p^0O_2}\right)^{\beta 1}\left(\frac{pH_2O}{pH_2O}\right)^{\beta 2}\left[exp\left(-\frac{\alpha_c F\eta_c}{RT}\right) - exp\left(-\frac{\alpha_a F\eta_c}{RT}\right)\right] \tag{2.17}$$

The reference exchange current densities are defined as follows:

$$i_a^{ref} = i_{a,0}^{ref} exp\left[-\frac{E_{A,a}}{R}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right] \tag{2.18}$$

$$i_c^{ref} = i_{c,0}^{ref} exp\left[-\frac{E_{A,c}}{R}\left(\frac{1}{T}-\frac{1}{T_0}\right)\right] \tag{2.19}$$

where E_A represents the respective anode and cathode active energy and i_0^{ref} is the respective anode and cathode reference exchange current densities at the reference temperature T_0.

The local over-potentials are defined as follows:

$$\eta_a = \phi_{sol} - \phi_{mem} \tag{2.20}$$

$$\eta_c = \phi_{sol} - \phi_{mem} - V_0 \tag{2.21}$$

where φ_{sol} is the solid electrode phase potential and φ_{mem} is the membrane electrolyte phase potential.

The current densities and thus the total cell current is obtained by solving the six governing vector differential equations in [10], [11] that are based on the laws of conservation of mass, momentum, chemical species, energy and charge.

All other known fuel cell phenomena, as illustrated in figure 2.16, including the membrane hydration and flow fields can be integrated into the final system model by implementing an electrochemical balanced equation based on the results obtained from the chemically based tests as discussed in E of section IV.

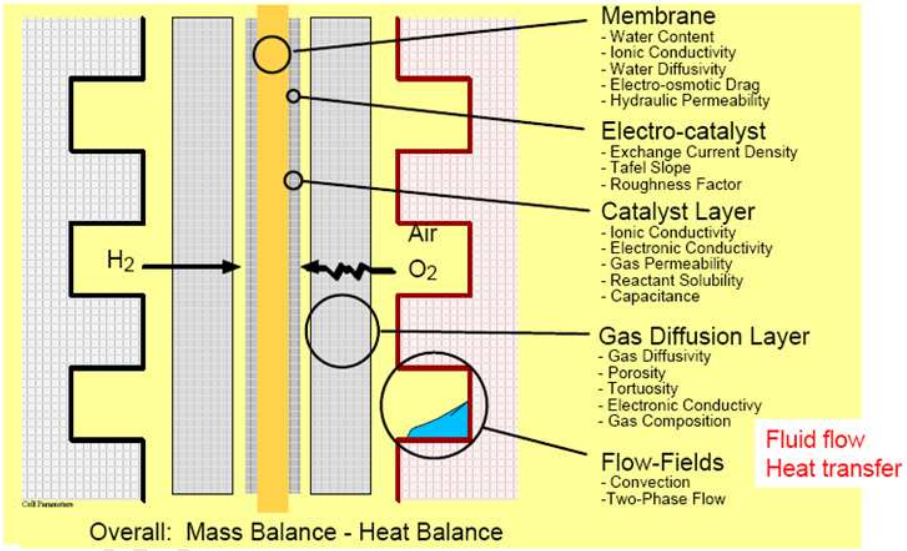

Figure 2.16. Fuel cell phenomena during operation [19].

VI. ELECTRICAL CIRCUIT MODELS OF THE CHEMICAL SYSTEM

Any type of fuel cell can be modelled by implementing a modified version of Randle's equivalent circuit [3], [14]. The model generally consists of an anode and cathode each consisting of a resistance and a parallel capacitor connected via a series resistance. The resistor represents the Faradic resistance of the electrode reactions. The capacitor represents the charge

double layer capacitance and the series resistor models the resistance of the fuel cell [14]. Diffusion losses may be incorporated by modelling it as a frequency dependant component.

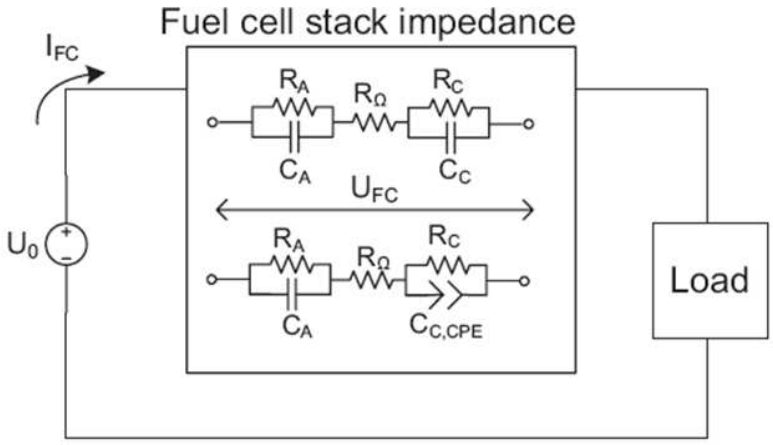

Figure 2.17. Randle's equivalent circuit representation of a PEM FC stack [14].

All the circuit components are dependent upon physical parameters; the most important being the stack temperature, pressure and gas concentration. The components of the equivalent circuit are not constant values but functions dependent on the above mentioned parameters. These functions, whether they are frequency dependant or parameter dependant, are obtained by using the electrochemically derived techniques.

The effects of actual loads on fuel cell performance play an important part in obtaining an accurate circuit model for a PEM fuel cell. The cell output voltage is regulated by a DC/DC converter and then fed through an inverter for final integration with the grid or other AC applications. As discussed in section IV, the frequency response analysis or EIS method of PEM fuel cells is the most preferred testing method for acquiring circuit parameters [14], [20]. The impedance is calculated and a Nyquist plot is produced. A curve fitting process is followed to derive the equivalent circuit, as shown in figure 2.18.

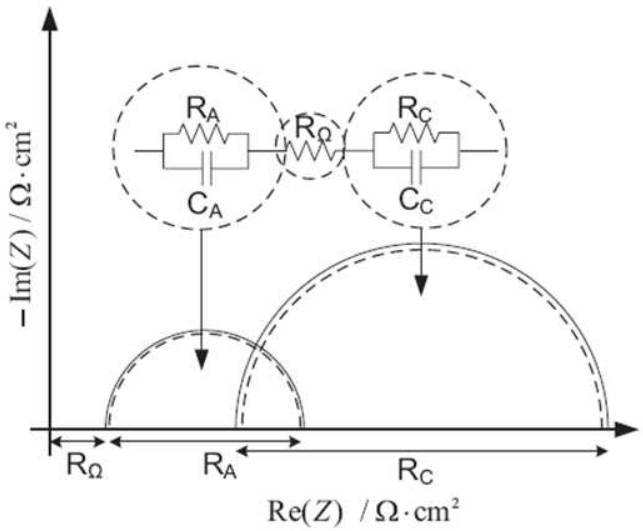

Figure 2.18. Illustration of the Nyquist plot regions corresponding circuit elements [12].

Equivalent circuits with active elements cannot be obtained by use of the EIS method. The active element particulars can be determined by the use of the current interrupt method [15]. By using a controlled load, the current from the cell stack is interrupted. This produces an instantaneous voltage rise that can be used to model the ohmic voltage drop in and across the fuel cell stack, as shown in figure 2.19.

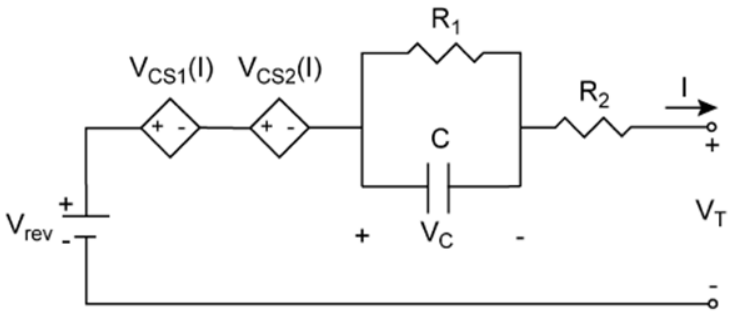

Figure 2.19. PEM FC circuit incorporating active elements [15].

VII. CONCLUSION

The current state of research in fuel cell technologies, including the modelling and characterization methodologies, is presented. High temperature operation is still in development and most of the research is still focused on improving the chemical performance of the system.

Many publications propose new modelling theories, especially in the CFD and thermodynamic domains. Most of the electrical circuit based modelling techniques presented have identified and incorporated the dynamic chemical behaviour and other physical parameters associated with an actual PEM fuel cell system into the model.

The semi-empirical models that have been developed and integrated into the proposed circuits are limited by the accuracy of the testing methodologies. The more recent models have begun to incorporate the characteristics determined by more than one test method and are therefore more accurate in reproducing the dynamic performance as compared to their older counter parts.

Circuit models and emulator designs for high temperature PEM fuel cells are still mostly in the theoretical stage since the actual chemical systems are still in development. New testing methodologies and emulator designs for high temperature operation were notably absent. Many of the existing circuit models and injection techniques used for the low temperature cells are still employed to represent their high temperature counter parts.

3. HIGH TEMPERATURE PEM FC MODEL

I. INTRODUCTION

Chapter 2 gives a brief introduction to the model used for HT PEM systems. As discussed, there are advantages to running the PEM FC system at temperatures higher than 100 degrees C. These types of PEM FC systems make use of phosphoric acid doped poly-benz-imidazole(PBI) membranes that can effectively withstand the higher operating temperature while delivering acceptable performance in terms of the losses normally associated with a PEM FC system.

The increased system temperature has some significant impacts on system performance when compared to the low temperature based Nafion PEM FC systems. The most significant of these are listed:

- Increased system dynamics
- Higher system efficiencies
- Less susceptible to CO poisoning
- Simplified temperature regulating systems
- Less complex start-up and shut down procedures
- Absence of liquid water makes the system capable of handling very low temperatures
- Waste heat can be recovered and used in CHP systems

The increased system efficiencies are partly due to the inherent chemical characteristics of the PBI based membranes that result in lower resistances at higher operating temperatures. The models for these resistances will be discussed in the following sections.

The mechanical degradation of the MEA materials is currently being studied extensively and has resulted in a number of empirical models. One of the first complete CHP models was presented by Korsgaard et al.[18], [21]-[23], and takes into account system components such as actuators and the fuel processor. The authors presented an empirical cell model that is based on extensive laboratory work.

This chapter presents the high temperature PEM FC model that will be integrated with the emulator system. The static elements derived in chapter 2 are adopted to reflect the characteristics of the PBI MEA. To limit model complexity, only the three main dynamic domains are incorporated into the model. Figure 2.16 illustrates the different mechanisms that come into play for a fuel cell. As can be seen from figure 3.1, the structural assembly of the HT PEM FC is similar to that of the low temperature system. It was thus assumed that the dynamics will behave in a similar manner and will be modelled accordingly in the following sections.

The polarization curves generated by the model are compared to that obtained from an experimental stack to illustrate the static performance of the model. To evaluate the dynamic response, the model results are compared to the experimental stack for two separate current step tests.

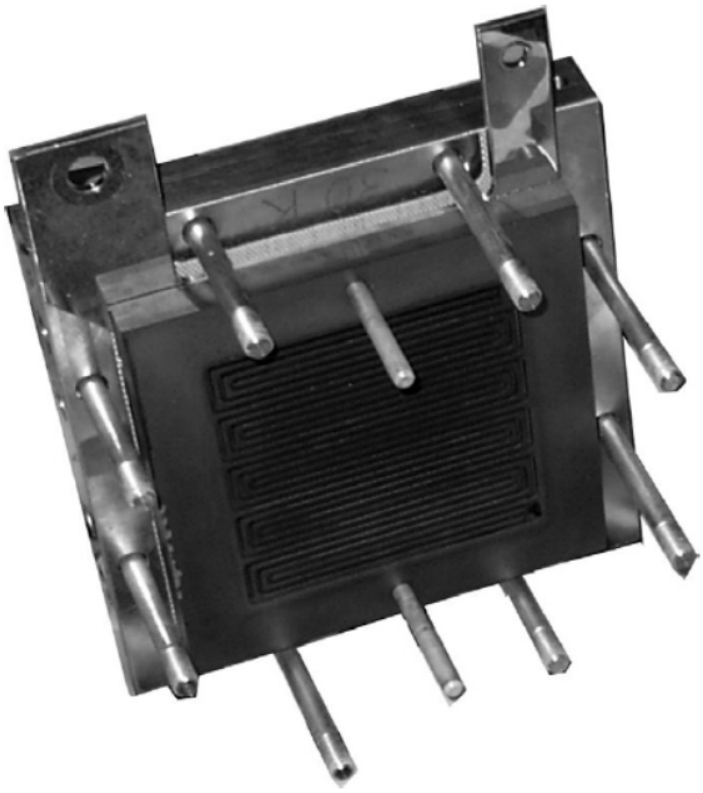

Figure 3.1. Single cell high temperature MEA [21].

II. MODEL BACKGROUND

The static model for LT operation was derived and presented in chapter 2 section IV, and will be adopted and modified to reflect the operation of a high temperature system. The static model produces voltage set points for a respective current density at the specified system operating conditions. If the current density is varied from 0 to the limiting current of the fuel cell, a polarization curve can be obtained.

The complexity of the model plays a very important role in the performance of the emulator. The more detailed and complex the model, the more processing power will be required from the hardware to compute it in real time. Gao et al. [24]-[26], produced a cell layer scale multidomain model for a LT PEM system that contained more than 25000 state variables. For this model to be computed in discrete time with a sampling period in the micro second range, a very powerful processing platform is required and as a result will be very costly to implement. It is possible to reduce the complexity of the model and still obtain an acceptable error between the model and the experimental system. To achieve this, the following assumptions are made:

1. The flow and the distribution of the gas species inside the fuel cell are evaluated on a one dimensional basis. The effect of the flow fields in the bipolar plates is thus ignored.
2. The gasses are uniformly distributed across the reaction sites.
3. Pressures across the flow channels are constant and pressure drops inside the stack are considered negligible and thus ignored.
4. The properties of the gasses are assumed to be ideal.
5. It is assumed that the flow of the gasses is laminar and incompressible.
6. The HT PEMFC operates between 100°C and 200°C.
7. The temperature across the stack is assumed to be constant and individual cells do not undergo different temperature variations.
8. The heat capacity of the stack is assumed to be constant during operation.
9. The stack model is a lumped parameter model of a number of single cells.

The lumped parameter model is kept as simple as possible to reduce computational effort and increase performance on the real time platform. Parameters that do not vary a great deal with a

change in operating conditions are assumed to be constant. To keep the accuracy to an acceptable level, especially during transient states, the governing equations were directly implemented in the model as derived in the following sections.

III. STATIC MODEL

The voltage for each cell is expressed in equation 2.9 of chapter 2. For the lumped parameter model of the stack, this is rewritten as follows:

$$V_T = N_{cell}(U_{rev} - U_{ohm} - U_{act} - U_{conc}) \tag{2.5}$$

where N_{cell} represents the series number of cells in the stack. The reversible open circuit voltage is given by equation 2.11 of chapter 2 and is repeated below for further discussion.

$$U_{rev} = E_{rev}^0 + \left(\frac{\Delta S}{zF}\right)_p (T - 298) + \frac{RT}{2F} ln\left(\frac{p_{H2} {p_{O2}}^{1/2}}{p_{H2O}}\right) \tag{2.11}$$

The reversible cell potential, E_{rev}^0, at standard operating conditions is calculated to be 1.229V [13]. The change in entropy, ΔS, is calculated from equation 2.12 of chapter 2. Variation of temperature has a small effect on this value and it is thus assumed to be constant at -44.43 to reduce computational effort.

The utilization of fuels at the anode and cathode sides of the cells is dependent on the current density at the specific operating point. The mole flow rate at the anode of the reacting hydrogen in mol/s can be determined from Faradays law and is given by equation 3.1.

$$M_{H_2 r} = \frac{i}{2F} \tag{3.1}$$

The mole flow rate at the cathode of the reacting oxygen in mol/s can be determined from Faradays law and is given by equation 3.2.

$$M_{O_2 r} = \frac{i}{4F} \tag{3.2}$$

where i represents the current density in A/cm^2 and F is Faraday's constant.

The utilization factor of hydrogen and oxygen is defined as the normalized reacted fuel flow divided by the normalized input fuel flow. The utilization factor at the anode is defined as follows [27]:

$$U_{fH_2} = \frac{n_{H_2}^r}{n_{H_2}^{in}} = \frac{60000RTi}{zFp_{fuel}V_{lpm(fuel)}x\%} \tag{3.3}$$

The utilization factor at the cathode is defined as follows:

$$U_{fO_2} = \frac{n_{O_2}^r}{n_{O_2}^{in}} = \frac{60000RTi}{2zF\,p_{air}V_{lpm(air)}y\%} \tag{3.4}$$

where R is the universal gas constant, T is the temperature in Kelvin, i is the current density, p the inlet air and fuel pressures, V the flow rate of the air and hydrogen at the inlets and x,y the percentage of hydrogen and oxygen in the gas mixture.

The partial pressures of the gas species are defined as follows:

$$p_{H_2} = \left(1 - U_{fH_2}\right)x\%p_{fuel} \tag{3.5}$$

$$p_{O_2} = \left(1 - U_{fO_2}\right)y\%p_{air} \tag{3.6}$$

The partial pressure of the water content is defines as follows:

$$p_{H_2O} = \left(\omega + 2y\%U_{fO_2}\right)p_{air} \tag{3.7}$$

where ω is the percentage of water vapour in the oxidant.

The activation voltage drop for the HT system is defined as follows [18]:

$$U_{act} = \frac{RT}{4\alpha F} ln\left(\frac{i + i_0}{i_0}\right) \tag{3.8}$$

where

$$\alpha = a_0 T + b_0 \tag{3.9}$$

and a_0 and b_0 are the charge transfer constants.

$$i_0 = a_3 e^{-b_3 T} \tag{3.10}$$

and a_3 and b_3 are the limiting current constants.

The ohmic resistance of the cells are defined as follows:

$$R_{ohm} = a_1 T + b_1 \tag{3.11}$$

and a_1 and b_1 are the ohmic loss constants.

The concentration voltage loss is described as follows:

$$U_{conc} = k_{amp} \times i^{k_{masst}} \times ln\left[1 - \frac{i}{i_{lim}}\right] \tag{3.12}$$

where k_{amp} and k_{masst} represent the respective amplification constants and i_{lim} the limiting current density of the cells.

Rewriting the above equations results in the following steady state output voltage equation used in the model:

$$U_{cell} = U_{rev} - \frac{RT}{4\alpha F} ln\left(\frac{i + i_0}{i_0}\right) - R_{ohm} i - k_{amp} \times i^{k_{masst}} \times ln\left[1 - \frac{i}{i_{lim}}\right] \tag{3.13}$$

IV. DYNAMIC MODEL

Under transient conditions several phenomena inside the fuel cell cause delays in the response time of the output voltage from the initial steady state value to the new steady state value at the respective operating conditions. The three main mechanisms that contribute to these delays are incorporated into the model. These are the electrical dynamics, gas flow dynamics and the thermo dynamics.

A. Electrical Dynamics

The main mechanism that drives the electrical dynamics is the charge double layer capacitance. The anode and the cathode inside a PEM fuel cell are separated by a porous membrane. The function of the membrane is to block the flow of electrons while allowing the positively charged hydrogen ions to flow across and combine with the oxygen to form water. The electrons are forced to flow through the current collectors to the external load. There are thus two charged layers of opposing polarity across the cathode and the membrane [28]. This layer has the ability to store charge and effectively behave like a super capacitor.

This capacitance can be determined by diagnostic tests such as EIS as described in chapter 2. The charge double layer capacitance changes with the frequency of the applied current to the fuel cell stack. Kim et al. [29], have conducted experimental tests on a fuel cell stack to determine the effects of pulsed current frequency variation of the performance of the fuel cell. As the capacitance has an effect on the voltage response in the sort time range, it was modelled as an input parameter and can be changed in real time on the emulator system. For experimental validation as shown in the following sections, the value was set to fit the voltage response of the experimental stack.

The effect of the charge double layer on stack voltage is expressed as follows:

$$\frac{dV_{act}}{dt} = \frac{i_{stack}}{C_{cdl}} - \frac{V_{act}}{R_{stack}C_{cdl}} \tag{3.14}$$

Where V_{act} represents the activation voltage loss, i_{stack} the total stack current, R_{stack} the effective resistance of the stack at the operating point and C_{cdl} is the value of capacitance in Farads.

B. Gas Flow Dynamics

During transient state, there are delays between the change in current and the flow rates of the fuel and the oxygen. These dynamics are modelled by using the mass balance as shown below [25].

$$\frac{M_{gas}V_{ch}}{RT}\left(\frac{d}{dt}P_{ch}\right) = \sum_{in/out}^{Ch} \dot{q}_{fluid} \tag{3.15}$$

where V_{ch} is the volume of the channels in m^3, P_{ch} is the pressure of the gas in the channel, M_{gas} is the molar mass and $\dot{q}_{fluid}$ is the fluid mass flow.

The net mole flow rates during steady state are given by equations 3.1 and 3.2. During transient state equation 3.15 is modified to produce the following first order differential equations for flow rates in the anode and cathode gas channels [28]:

$$\tau_a \frac{dM_{H_2net}}{dt} = \frac{i}{2F} - M_{H_2net} \tag{3.16}$$

$$\tau_c \frac{dM_{O_2net}}{dt} = \frac{i}{4F} - M_{O_2net} \tag{3.17}$$

The time constants τ_a and τ_c represent the flow delays at the anode and cathode respectively. M_{H_2net} and M_{O_2net} represent the net molar flow rates of the hydrogen and oxygen in the fuel cell.

C. Thermo Dynamics

The temperature rise of the fuel cell due to the internal heat generation rate is caused by the inherent exothermal chemical reaction. The experimental stack uses oil as the heat transfer

material, referred to as the coolant, and heat exchangers/heaters to regulate the temperature of the coolant. Figure 3.2 represents the flow of thermal energy in the fuel cell stack. The main mechanisms for the transfer of thermal energy to and from the stack are conduction, convection and to a lesser extent, radiation.

Under steady state conditions the fuel cell will operate at a constant temperature. Under transient conditions the fuel cell will either heat up or cool down depending on the operating point. The temperature rise/fall of the fuel cell can be approximated by calculating the electrical losses. This is represented by the following differential equation:

$$C_t \frac{dT}{dt} = i_{stack}(V_{rev} - V_o) - h(T_{coolant} - T) \tag{3.18}$$

The thermal capacitance, C_t of the stack can be in the order of several farads and the heat transfer coefficient is represented by h in the thermal model.

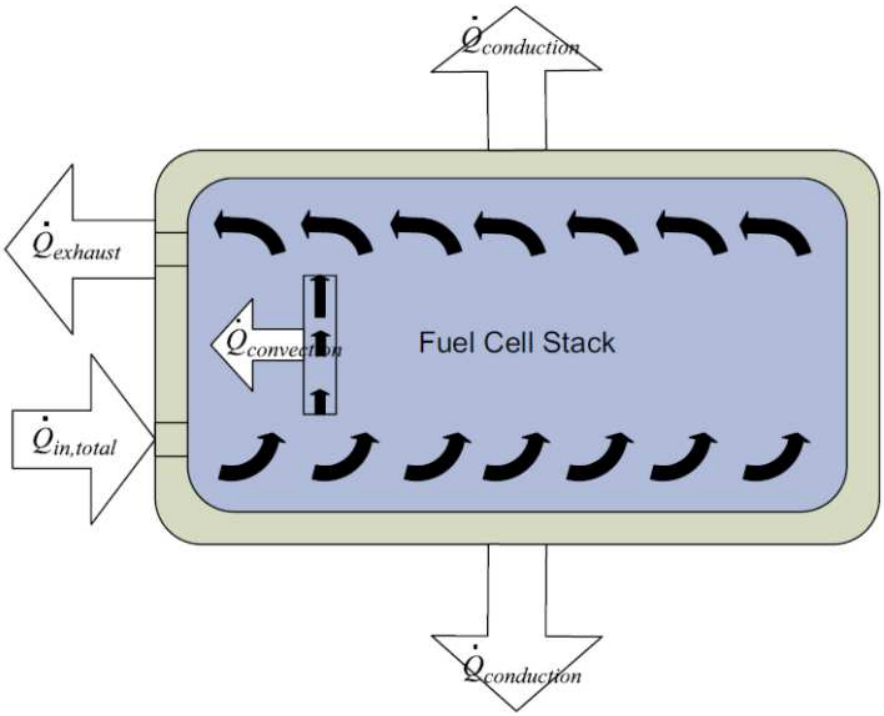

Figure 3.2. Thermal energy flows in an air cooled FC stack [23].

V. MODEL IMPLEMENTATION

The model, as derived in the previous section, was implemented in MATLAB Simulink. All the static and dynamic components were modelled as separate sub system blocks in the main model. This allowed for the evaluation of the performance of each separate block to optimize the total system accuracy.

The flow chart in figure 3.3 represents the integration of the sub elements of the model. The complete Simulink model and the dynamic element blocks are attached in Appendix 2 for reference purposes. The input parameters can be changed in real time during program execution on the digital signal processor (DSP). The current and voltage feedback from the load are required to determine the operating point of the system.

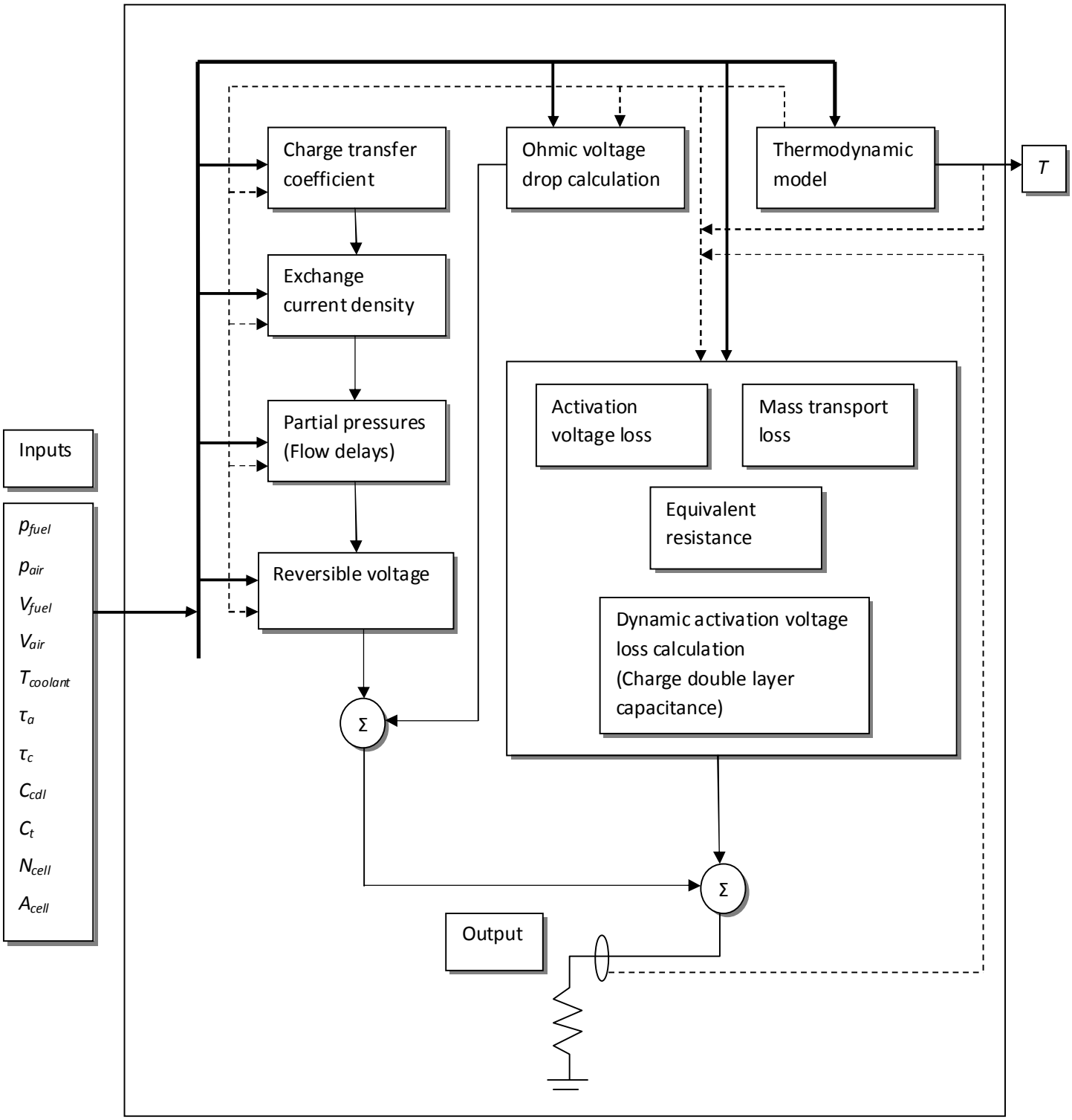

Figure 3.3. Diagram depicting integration of model elements.

The units and operating ranges of the input parameters are defined in table 3.1.

Table 3.1: Model input parameters

Parameter	Unit	Range
Coolant temperature	$°C$	110-180
Hydrogen pressure	Atm	System dependant
Air pressure	Atm	System dependant
Hydrogen flow rate	$slpm$	System dependant
Air flow rate	$slpm$	System dependant
Number of series cells in stack	N	System dependant
Area of cells	cm^2	System dependant
Anode reactant flow delay	s	System dependant
Cathode reactant flow delay	s	System dependant
Charge double layer capacitance	F	System dependant
Thermal capacitance	F	System dependant

The fuel cell parameters in the model were adjusted to fit the response of a ZSW 667 high temperature stack. The stack data is given in table 3.2.

Table 3.2: Experimental stack data

Parameter	Value
Manufacturer	ZSW Germany
Rated power	1000W
Rated voltage	30V
Rated current	$35A$
Nominal operating temperature	$140°C$
Number of series cells in stack	48
Area of cells	$100cm^2$

VI. RESULTS

This section presents the experimental results obtained during steady state and transient testing for the HT PEM FC described in table 3.2. Firstly, the results obtained from a single HT cell are discussed. The following sections detail the responses of the 1kW stack and are compared to that generated by the model. The error between the stack voltage and the model on a cellular level is compared to that generated by a more complex modelling approach. As the emulator is required to represent a 1kW stack, the model was not fit to the results obtained for the single cell or smaller stacks and was optimized for higher power ratings.

During operation, certain phenomena may occur that has an effect on the fuel cell output. It is thus required that the model be able to replicate these characteristics to a certain extent. For the emulation of the electrical outputs, three main phenomena were selected and modelled. These include polarization curve hysteresis, stack voltage response to pulsed currents and the effect of fuel starvation on the output voltage. Experimental results from the fuel cell stack were obtained for the polarization curve hysteresis effect and are compared to that generated by the model. The other operating phenomena were modelled to respond according to experimental results obtained in literature.

A. Single cells

The experimental results obtained from a HT PEMFC under development in HySA (Hydrogen South Africa) systems are presented in figure 2.3 and 3.4. It can clearly be seen that the output voltage and power for the cells are higher at higher operating temperatures. The main loss factor that undergoes improvement is the membrane ohmic losses in the linear operating region. The acid based PBI membrane has a reduced resistance at higher operating temperature compared to the low temperature NAFION based membranes.

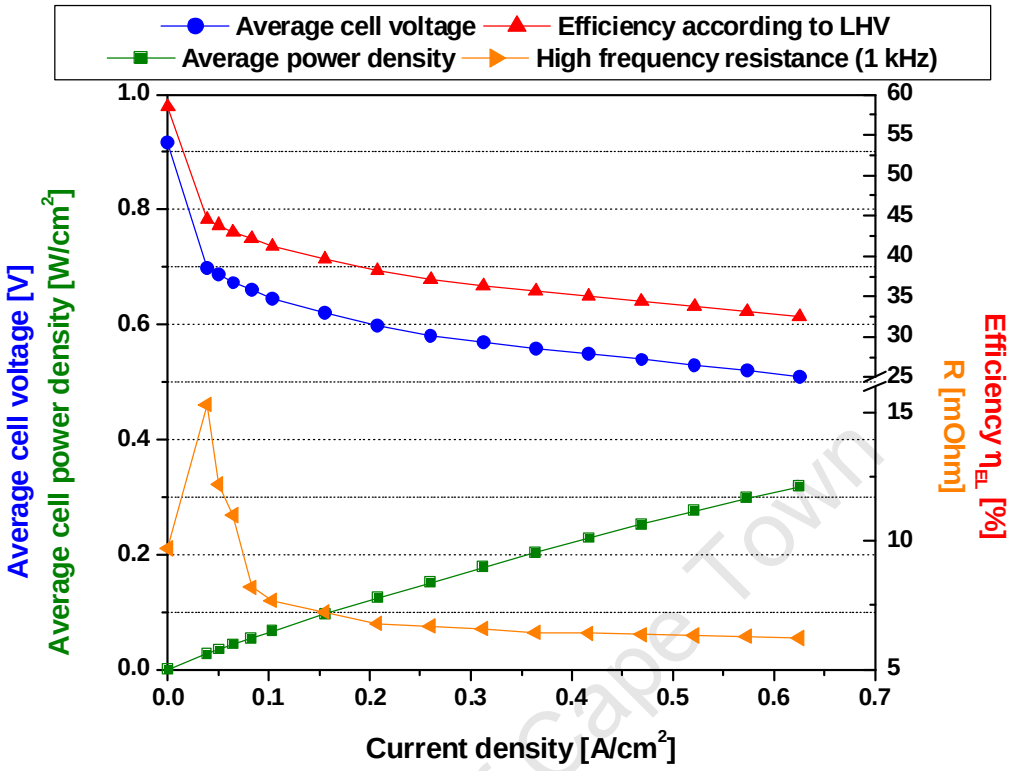

Figure 3.4. Polarization curve for a 5 cell stack at 160°C

Figure 3.5 represents the measured experimental voltages of the individual cells inside the stack as well as that of the model. It is clear that there are small differences in the voltages between the individual cells as a result of the differences in pressure, temperature, reactant flow etc.

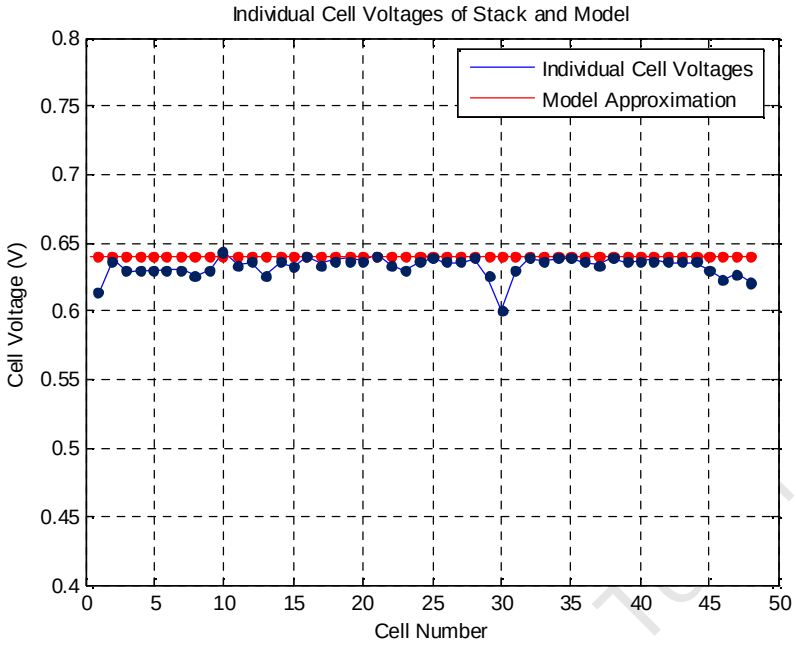

Figure 3.5. Individual cell voltages of the stack and the model approximation.

Figure 3.6 represents the model results obtained from the cell based model of [26]. It is clear that the model prediction can be far more accurate than that presented in figure 3.5 for a lumped parameter model. The gain in error margin for the cell voltages between the two modelling approaches does however not achieve adequate benefits for the emulator to justify its use as well as the additional costs of the processing hardware required for the real time implementation during the development of the emulator system.

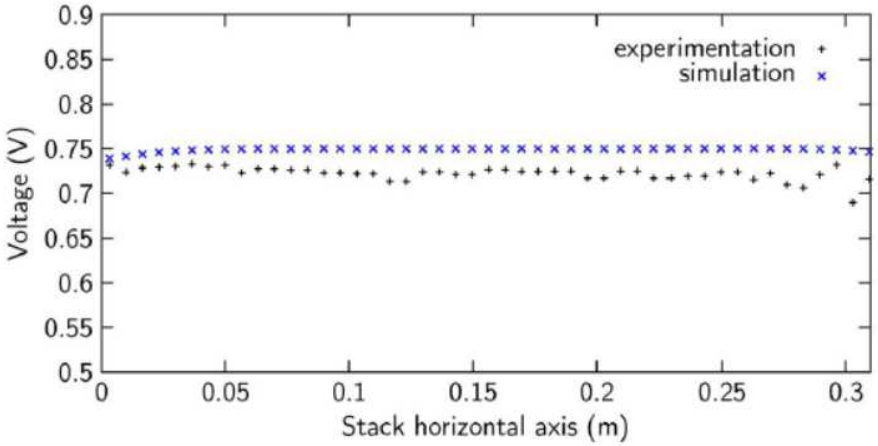

Figure 3.6. Individual cell voltages of the stack and the model approximation from the cell layer model in [26].

B. Stack polarization curves

The experimental results obtained from the ZSW stack (table 3.2) are compared with those generated by the model at different operating conditions. The model was optimized for the standard operating conditions at 140°C.

The polarization curves were generated under steady state conditions. The current was linearly increased over time to allow the temperature and flow rate loops to remain in steady state. As shown by figure 3.7 the modelled voltage drop in the activation region has a good fit relative to the actual system. The predicted voltage by the model does tend to differ in the linear ohmic region. This is mainly attributed to the resistive parameters in the model and to the fact that the lumped parameter model assumes an even temperature distribution across the complete stack. This is however not the case in the real system as the cells at the ends of the stack will have a higher mean temperature compared to the centre cells since they are cooled more effectively. This will result in an uneven temperature and voltage distribution across the series connected cells.

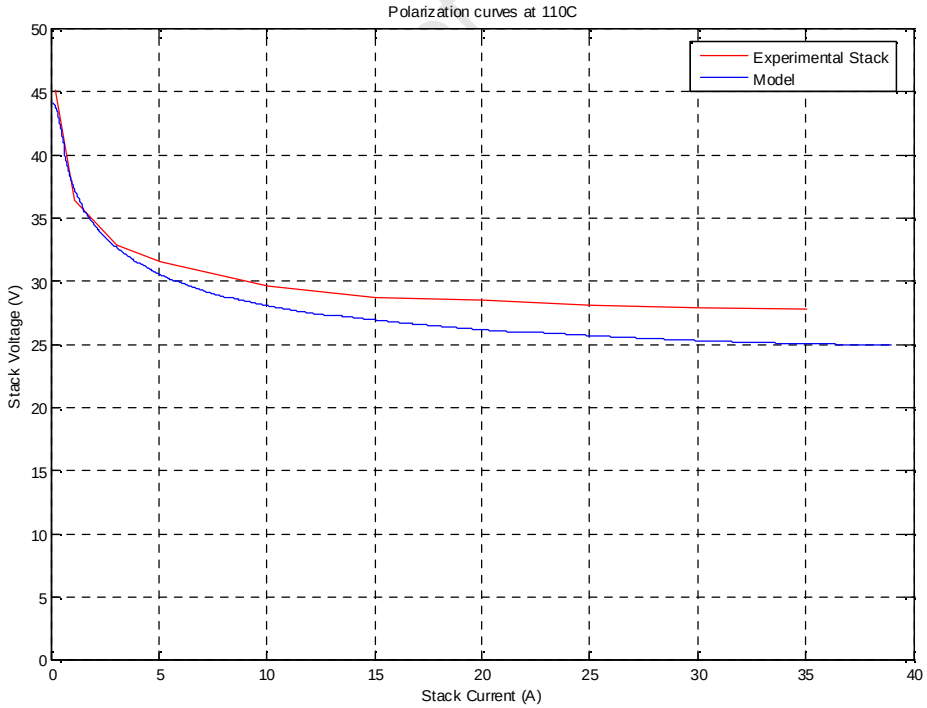

Figure 3.7. Polarization curves at 110°C.

Figure 3.8 and 3.9 shows the polarization curves at higher operating temperatures; the error in stack voltage between the model and the experimental system decreases with an increase in system temperature. This can be attributed to the increase in effectiveness of the cooling system at higher operating temperatures and the decreased error for the lumped parameter model that assumes constant temperature across the stack.

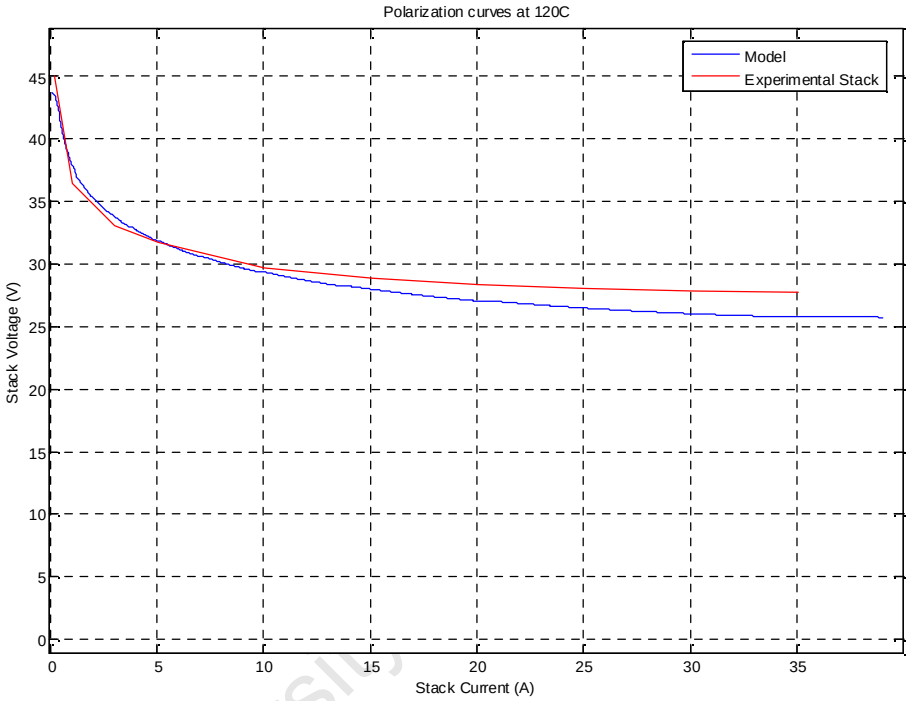

Figure 3.8. Polarization curves at 120°C.

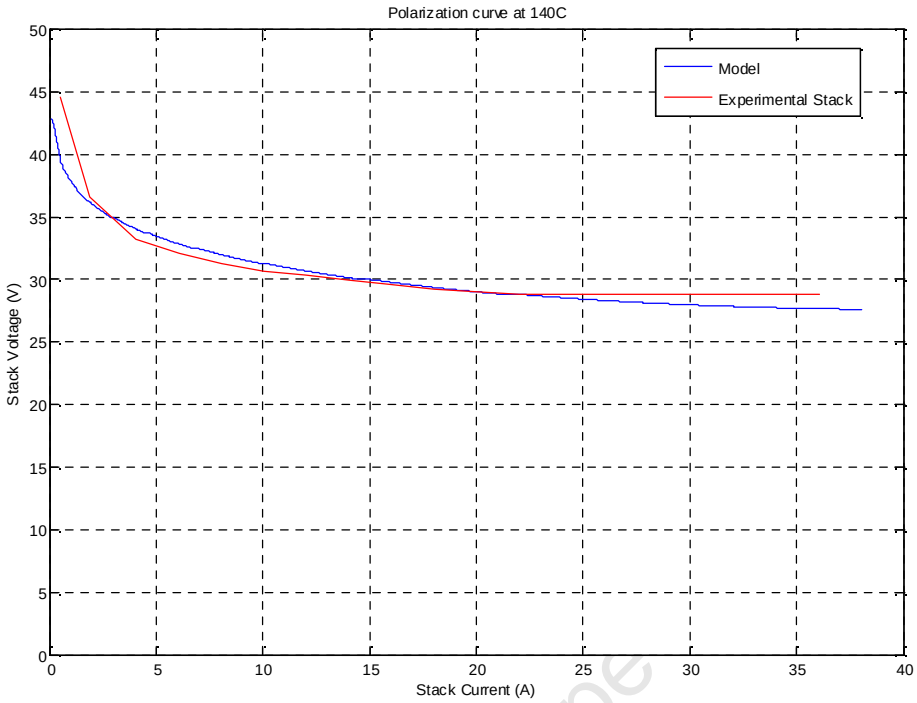

Figure 3.9. Polarization curves at 140°C.

Figure 3.10 represents the power outputs of the model and the experimental stack. At the rated current of 35A and rated stack temperature of 140°C the output equals the rated 1kW. Increased temperature will result in higher output and system efficiencies while operating at lower temperatures the stack will perform less effectively. It should be noted that the current of the stack was never increased above rated value. The fuel cell will start to operate in the concentration region and the voltage will drop exponentially as the current is increased above the peak power point.

The sensitivity of the model, with regards to temperature changes, is greater than that of the actual fuel cell stack. The most sensitive operating point will be at the rated current of 35A. For a 30°C rise in temperature, the voltage of the model will increase by 11.2% compared to the 2.85% of the tested fuel cell stack. The model temperature will thus change by 0.37% per 1°C compared to the 0.095% of the tested fuel cell at the 35A operating point in the linear ohmic region. The difference is due to the assumptions made for the lumped parameter model.

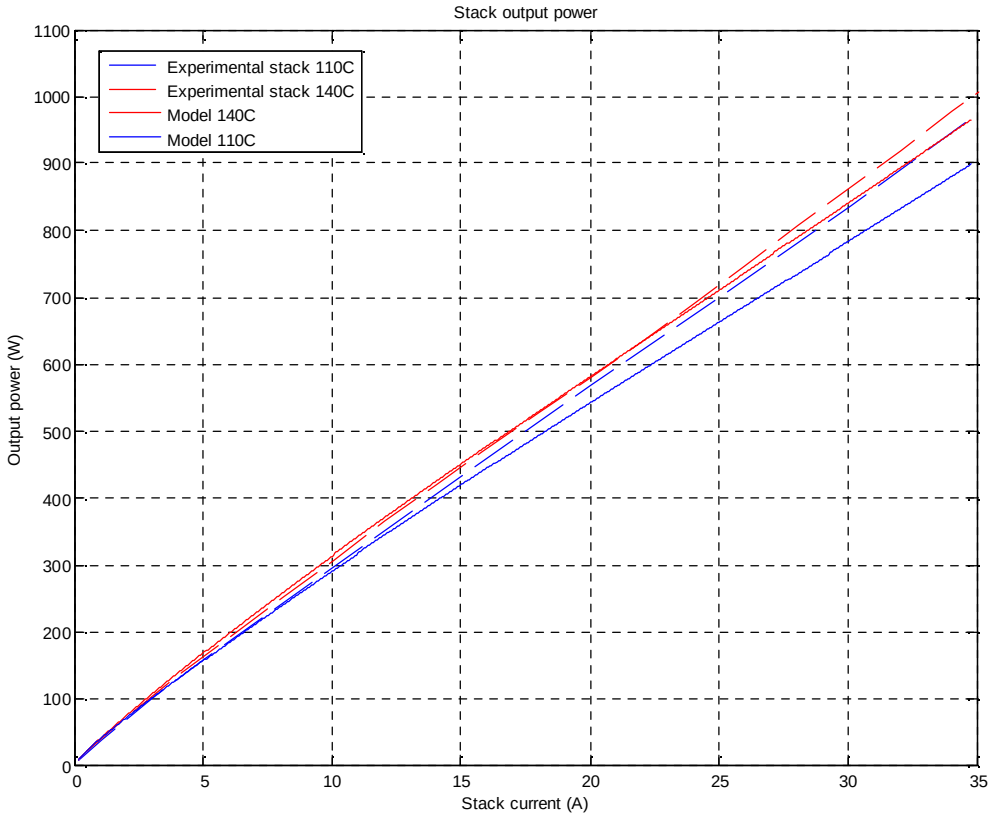

Figure 3.10. Output power predicted by the model

C. Stack response to current steps

The experimental stack has various subsystems that control the temperature, current, gas pressures and other parameters to ensure safe operation. These systems are set up to limit the rates of change of the operating parameters. The parameter safety limits, as set up in the control systems, cannot be exceeded under normal operating conditions. The maximum stack current that could be delivered was set to 25A, well below the peak power threshold. The current ramp rate was limited to 0.6A/second to ensure the system does not undergo fuel starvation and other operating phenomena that can occur during dynamic testing. The model was fit to the data acquired, while assumptions were made to predict the effects under more extreme dynamic conditions.

Figure 3.11 and 3.12 shows the long time voltage response of the model and the stack for two separate current transient tests. The stack voltage under and overshoots in the long time range are primarily caused by the thermal dynamics and the hydrogen and oxygen flow delays.

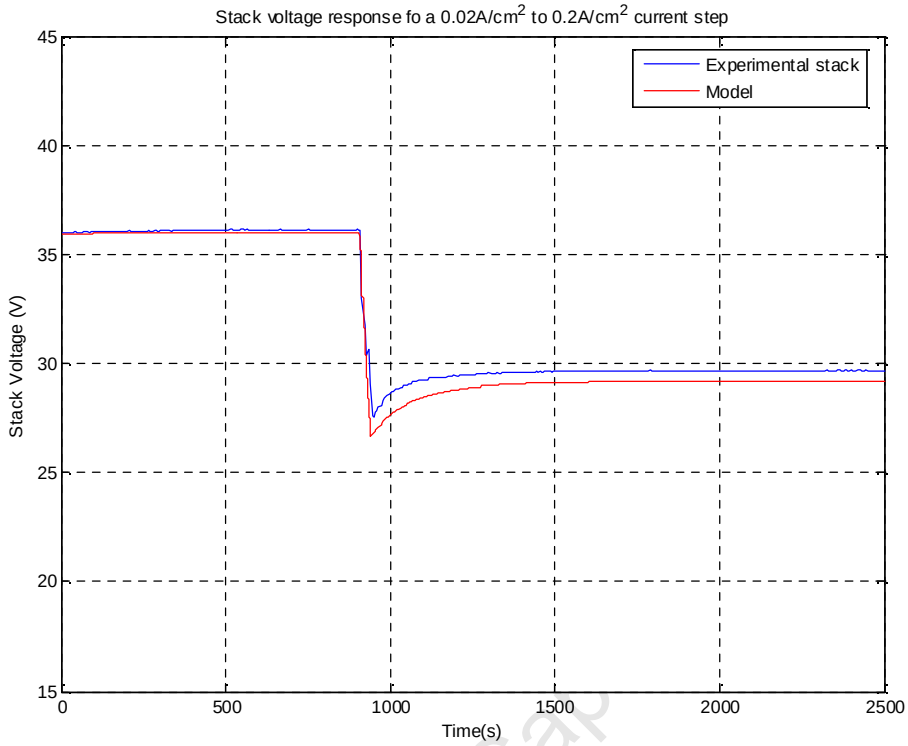

Figure 3.11. Long time response for a 0.02A/cm^2 to 0.2 A/cm^2 current step.

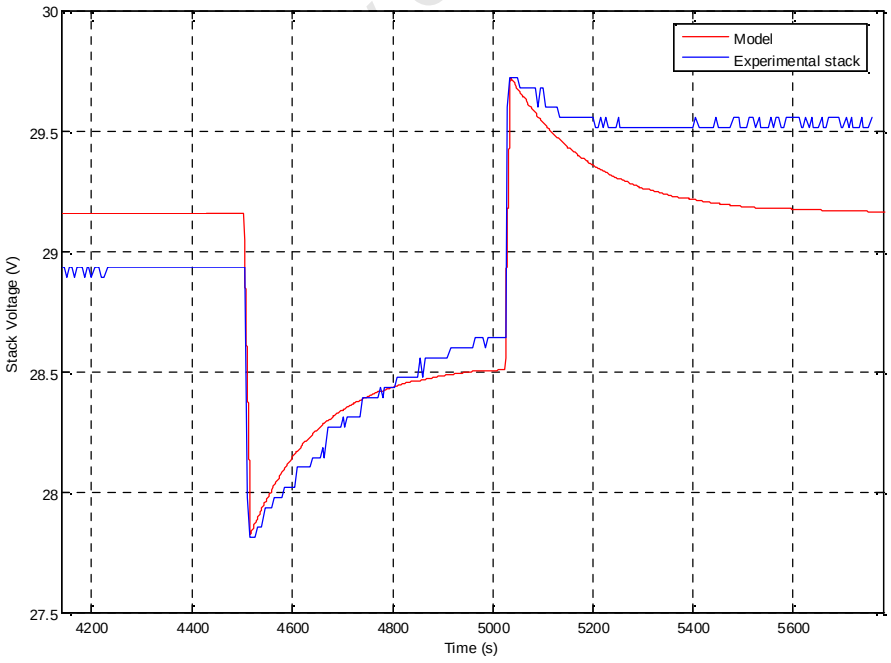

Figure 3.12. Long time response for 0.2A/cm^2 to 0.25 A/cm^2 current pulse.

The temperature response of the stack was simulated for a similar current pulse as performed during the experimental test in figure 3.12. From the simulation in figure 3.13 it can be seen that the stack is operating at about 177°C for a current density of 0.2A/cm^2. Once the current density is further increased to 0.25A/cm^2 the temperature will rise to a new steady state operating point. Reducing the current density will result in an exponential decay of temperature to the original steady state operating point.

The long time temperature response for a coolant temperature of 110°C is shown in figure 3.14. It is clear that the initial change in temperature, ΔT, until steady state is achieved at lower temperatures is higher than that achieved at higher operating temperatures. This is due to the reduction in the effectiveness of the cooling system at lower operating temperature.

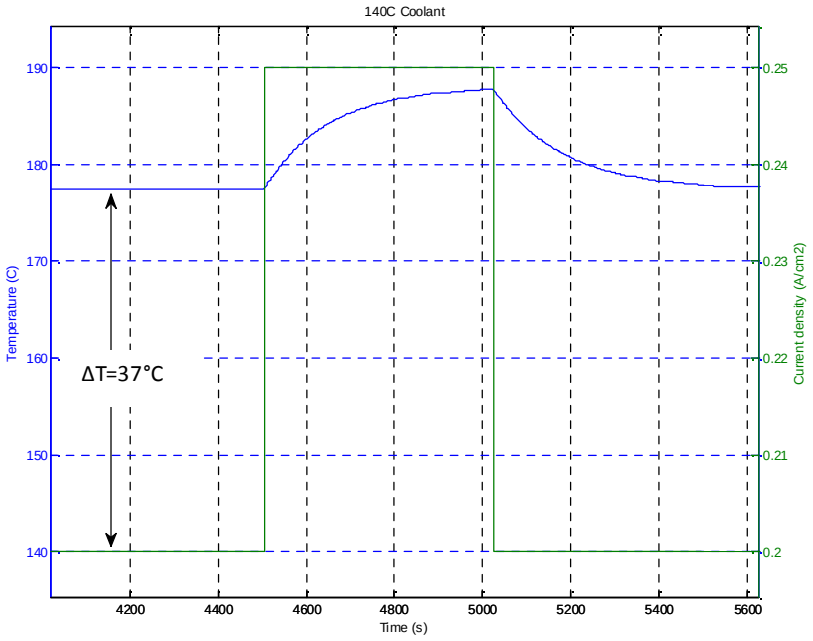

Figure 3.13. Long time temperature response for 0.2A/cm^2 to 0.25 A/cm^2 current steps at 140°C as predicted by the model.

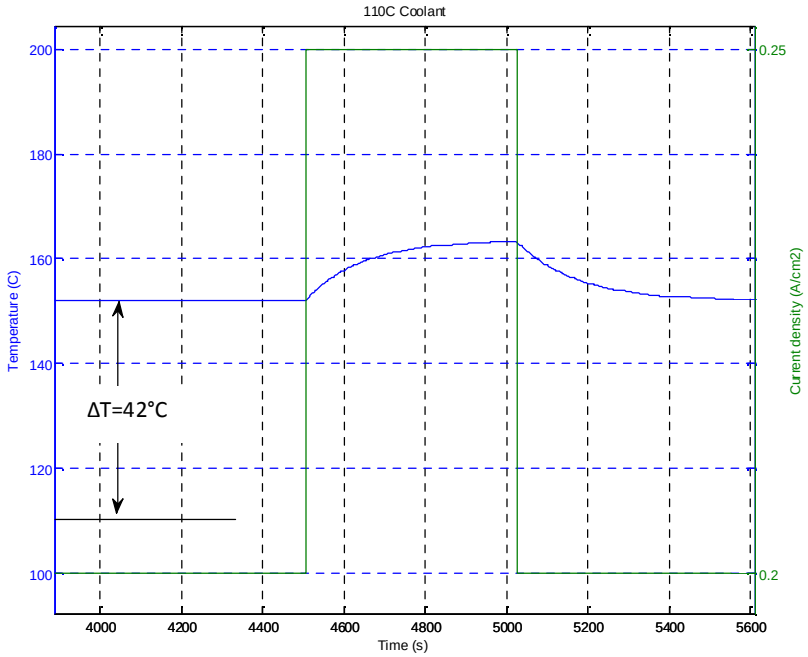

Figure 3.14. Long time temperature response for 0.2 A/cm^2 to 0.25 A/cm^2 current steps at 110°C as predicted by the model.

Figure 3.15 and 3.16 shows the response for the partial pressures in the gas flow channels at the cathode for the current steps. At higher current densities the partial pressure will be reduced as more oxygen is consumed by the chemical reaction. During transient state there is a delay between the load current and the molar flow of hydrogen and oxygen. The change in pressure over the long time range results from the change in stack temperature. An increase in temperature will result in a reduction in partial pressure. The effect for a change in coolant temperature can also be seen in the change in magnitude of the two curves in the figures.

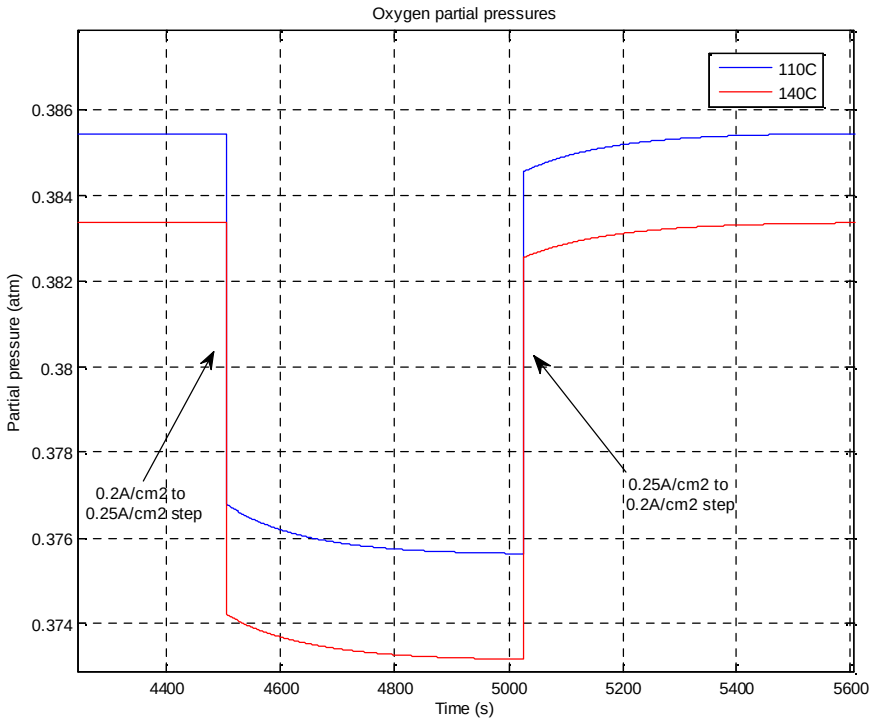

Figure 3.15. Long time response for oxygen partial pressure for 0.2 A/cm^2 to 0.25 A/cm^2 current steps as predicted by the model.

Figure 3.16 shows the short time response of the reactant flow delays as modelled by the time constants in equations 3.16 and 3.17. The delays in the partial pressure change contribute to the output voltage response of the stack in the short time as well as the long time range.

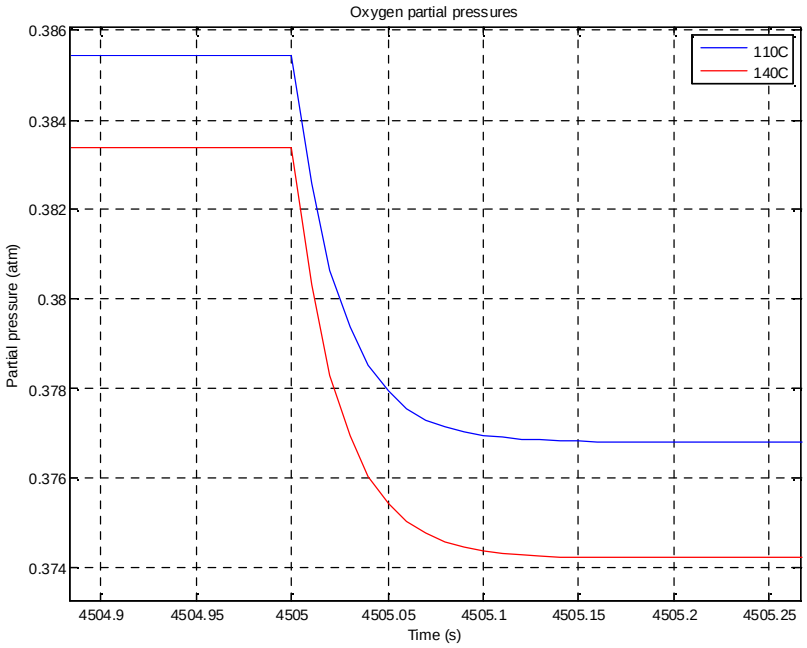

Figure 3.16. Short time response for oxygen partial pressure for 0.2A/cm^2 to 0.25 A/cm^2 current steps as predicted by the model.

The same response can be observed in the partial pressure of the hydrogen in the anode gas channels over the short and long time ranges as shown in figure 3.17 and 3.18. The time constants for reactant flow delays in the anode and cathode were both set at 30ms.

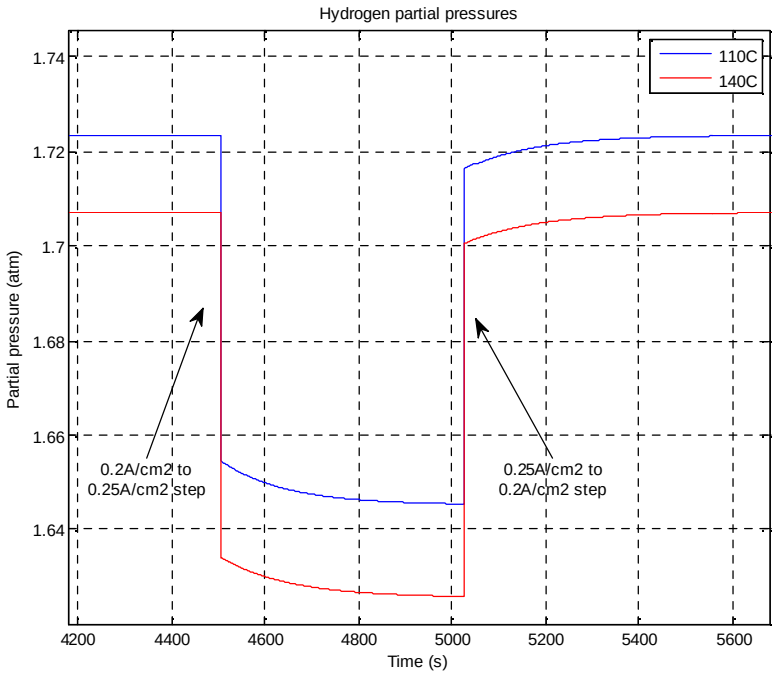

Figure 3.17. Long time response for hydrogen partial pressure for 0.2A/cm^2 to 0.25 A/cm^2 current steps as predicted by the model.

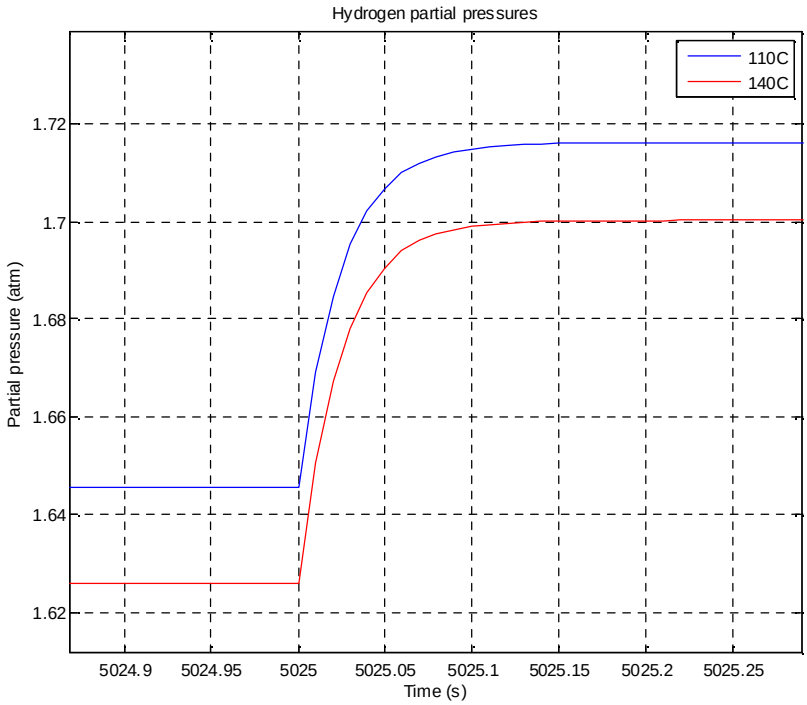

Figure 3.18. Short time response for hydrogen partial pressure for 0.25 A/cm^2 to 0.2 A/cm^2 current steps as predicted by the model.

The short time voltage response of the stack is depicted in figures 3.19 and 3.20. The initial drop in voltage is due to the internal cell and total stack resistance which can clearly be seen. The exponential decay in voltage is a result of the electrical dynamics. As described previously, this is mainly due to the charge double layer phenomenon inside the membrane electrode assembly (MEA) [30]. The reactant flow delays also contribute to the voltage transients in the short time range.

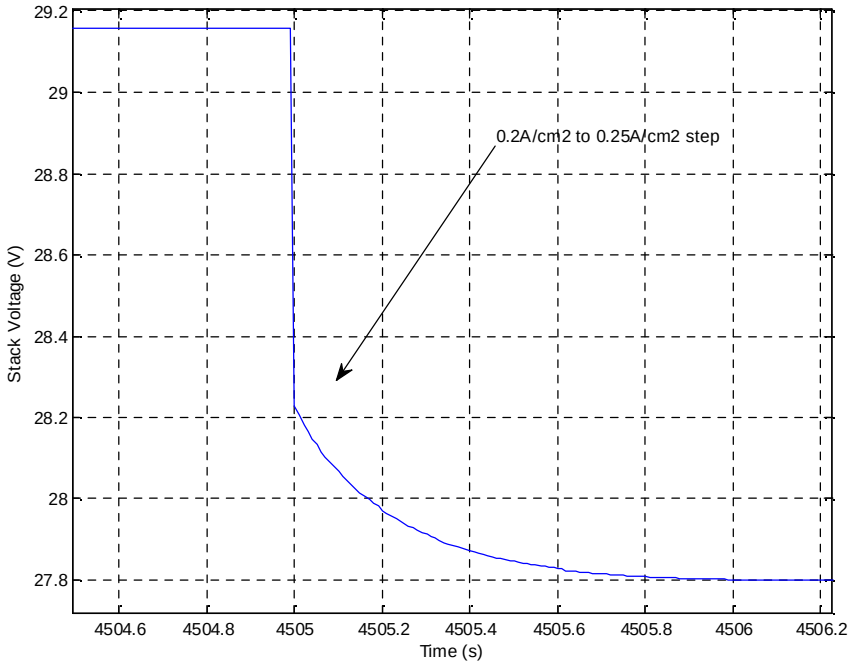

Figure 3.19. Short time response of the stack voltage for a 0.2 A/cm^2 to 0.25 A/cm^2 current step as predicted by the model.

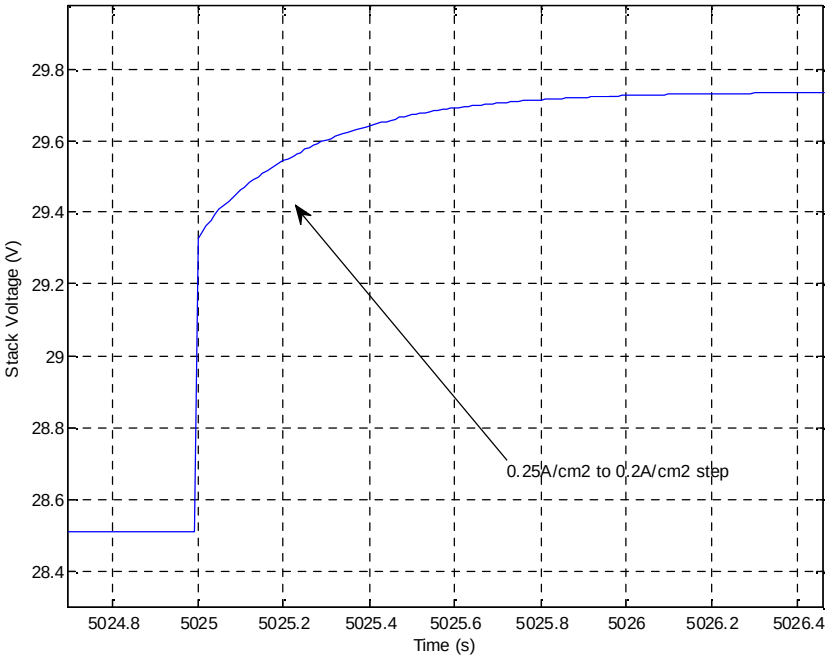

Figure 3.20. Short time response of the stack voltage for a 0.25 A/cm^2 to 0.2 A/cm^2 current step as predicted by the model.

The change in response in the short time range of the stack voltage for a change in coolant temperature is shown in figure 3.21. There is an increase in the initial instantaneous voltage drop due to the increase in membrane resistance. It is therefore beneficial to operate the fuel cell at higher operating temperatures to increase the transient response characteristics.

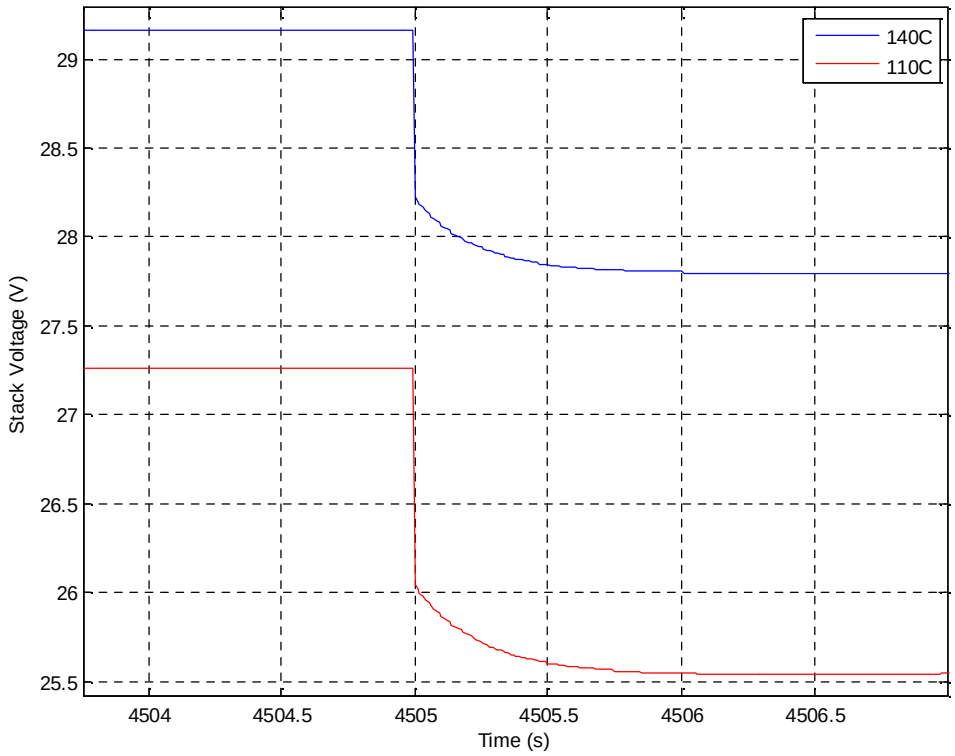

Figure 3.21. Short time response for the stack voltage for a 0.2 A/cm^2 to 0.25 A/cm^2 current step at different operating temperatures.

D. Variable frequency response

For fuel cells to interface with the load or the grid, the output voltage must be conditioned and converted to a constant DC or AC voltage. This requires a power conditioning system that may consist of an inverter and/or a DC-DC converter as shown in figure 3.22.

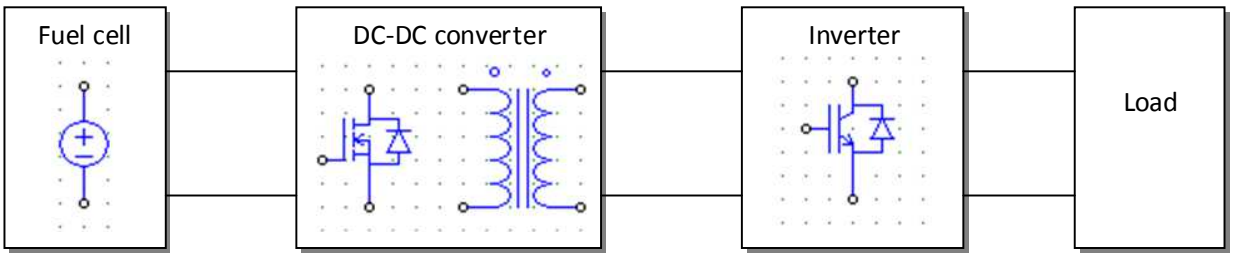

Figure 3.22. Block diagram depicting a fuel cell power conditioning system.

The addition of these power conditioning converters to the fuel cell system causes the flow of ripple current or pulsed current into the fuel cell stack. The output voltage response of the fuel cell has been investigated in a number of published works including the effects of degradation in performance over time as a result of these pulsed currents [29].

From this study, the captured output voltage ripple at different pulsed current frequencies is presented in figure 3.23. The results clearly demonstrate the increased ripple magnitude at lower frequencies. From the EIS data, the study also concluded that the charge double layer capacitance increases with an increased pulsed current frequency.

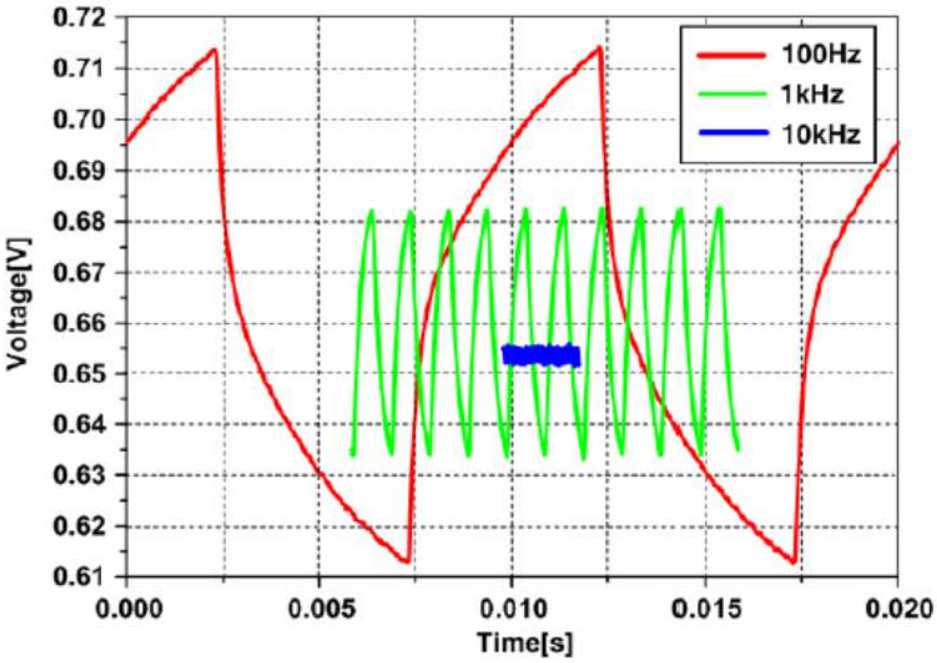

Figure 3.23. Fuel cell output voltage ripple at different frequencies [29].

At lower frequencies, the fuel cell will exhibit the same response with an increased ripple magnitude. The high temperature model was used to generate simulated responses for a 5Hz and 10Hz pulsed current as shown in figure 3.24. It is clear that the voltage ripple magnitude is extensive at such low frequencies.

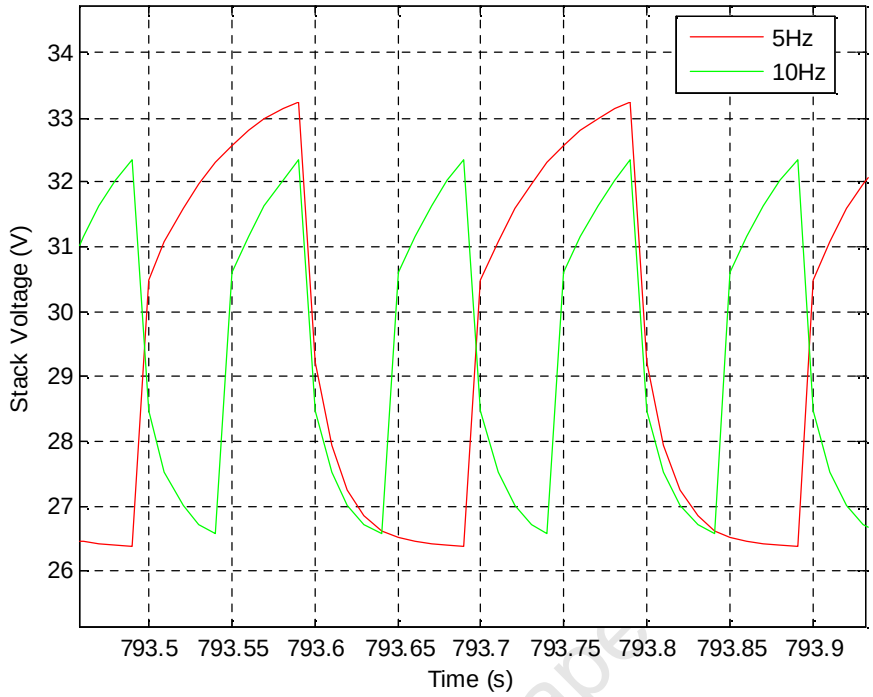

Figure 3.24. Fuel cell model output voltage ripple at different frequencies.

E. Polarization curve hysteresis

In the experimental results obtained, the polarization curves were recorded for both increasing and decreasing current densities. The curves demonstrated a hysteresis effect at all the coolant operating temperature set points (110°C, 120°C and 140°C). In low temperature fuel cells, the polarization curves obtained may exhibit a hysteresis effect as a result of flooding or drying [31].

The model was used to generate the polarization curves under the same operating conditions for increasing and decreasing current densities. The output curves obtained demonstrated the same polarization effect as shown in figure 3.25. The stack temperature curves obtained during simulation are presented in figure 3.26. It is clear that the stack is operating in a higher temperature band during a ramp down test which results in the increased output voltage of the polarization curve.

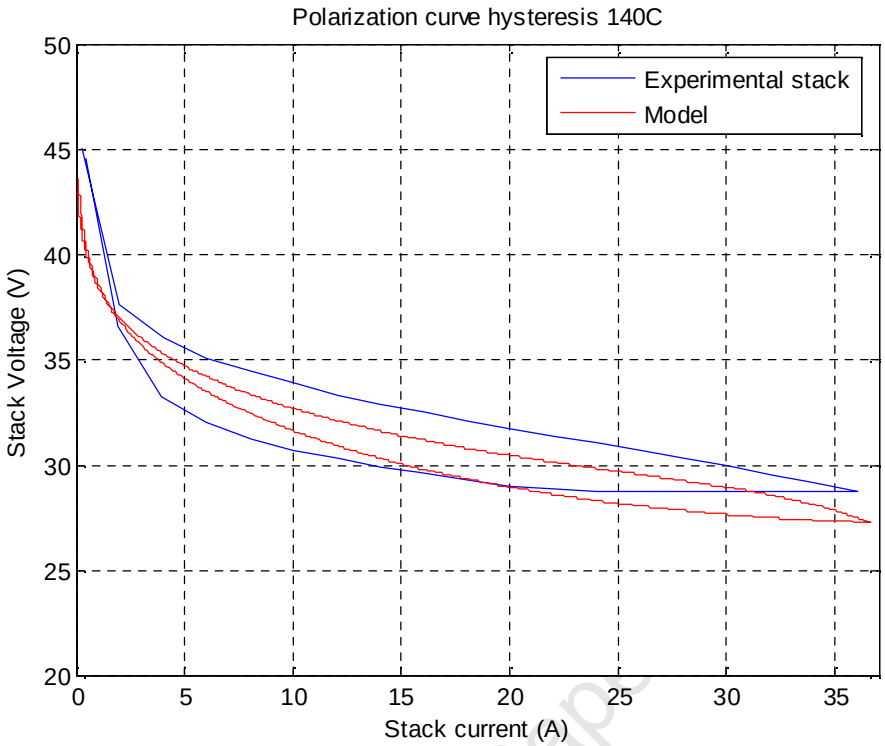

Figure 3.25. Fuel cell polarization curve hysteresis.

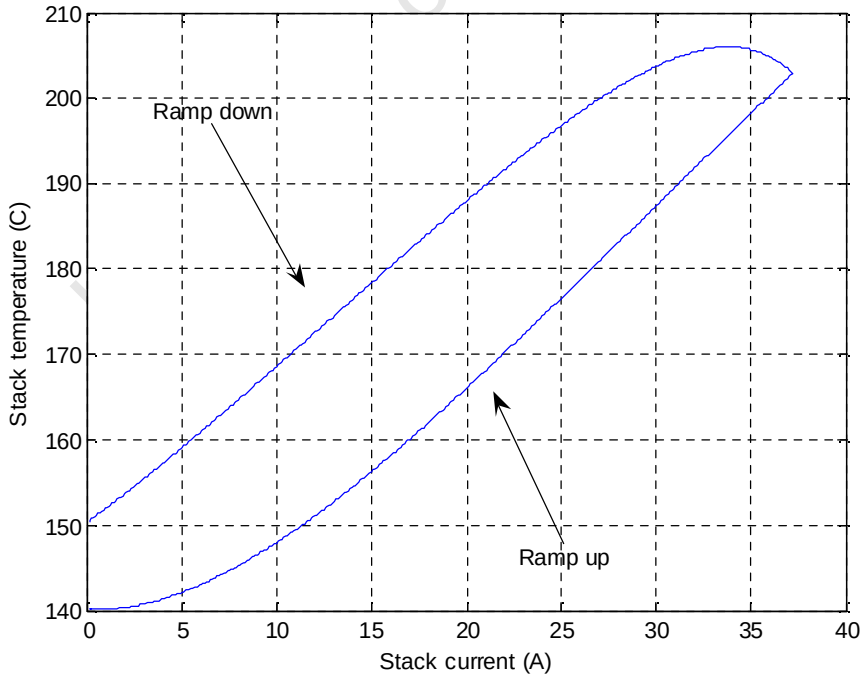

Figure 3.26. Fuel cell model temperature response.

F. Fuel starvation phenomenon

Operating a fuel cell system close to the limits may result in operational anomalies occurring during dynamics. One of these is the reaction of the stack due to fuel starvation, typically oxygen. As discussed in section IV B of this chapter, there are flow delays in the gas channels for the hydrogen and oxygen during dynamic load conditions. If the flow delays are such that the gas at the reaction site gets depleted during an increase in current, the fuel cell output voltage will drop as a result of the fuel starvation. Extensive experimental work has been done in [32] to illustrate the short and long term detrimental effects on a fuel cell as a result of starvation. The effect on the stack voltage during a load transition is shown in figure 3.27.

Fuel starvation can be modelled by increasing the time constant for the oxygen partial pressure in equation 3.17 to a large value, about 0.5 seconds, to model the delay of the flow of oxygen for a change in load current. The simulated effect on the stack voltage for a load step is shown in figure 3.28.

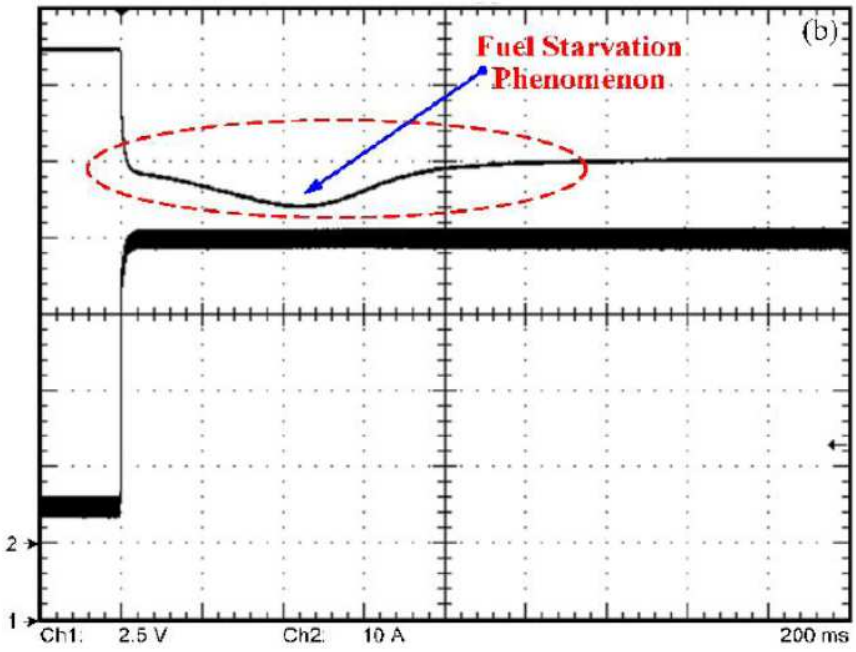

Figure 3.27. Fuel starvation during a current step from [32].

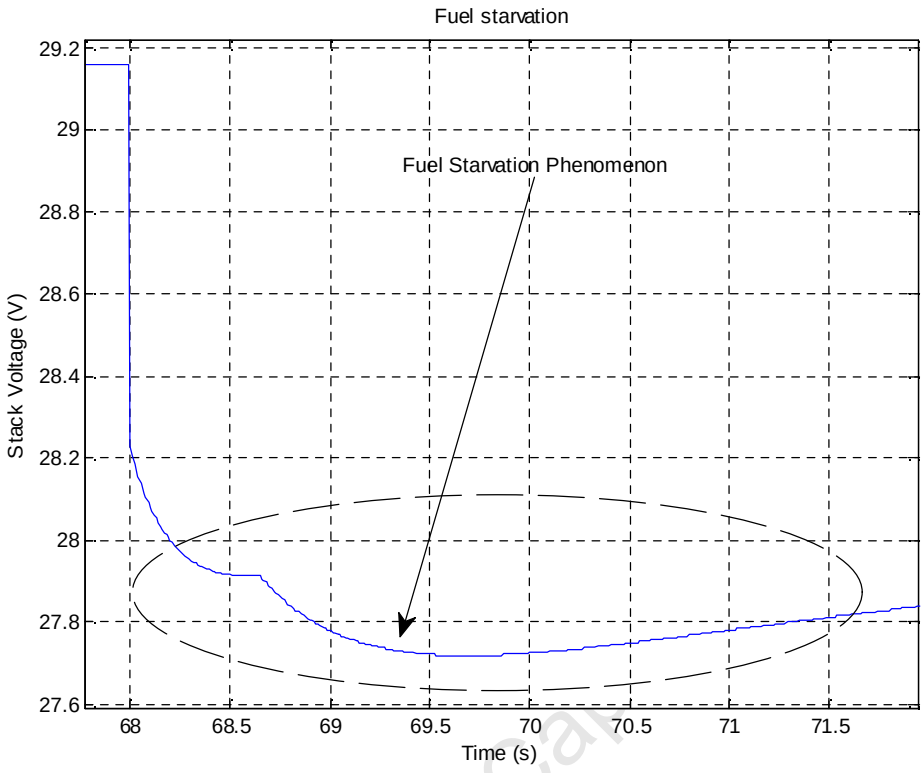

Figure 3.28. Fuel starvation during a current step as predicted by the model.

VII. CONCLUSION

This chapter presented the high temperature PEM fuel cell model that was implemented to replicate the electrical output characteristics of a 1kW ZSW stack. The polarization curves at different operating temperatures were generated by the model and compared to that captured from the experimental stack. The model exhibits an error at lower operating temperatures due to the assumption of constant temperature distribution across the stack. Despite the error in the ohmic region, the model is able to deliver acceptable accuracy for a simplified lumped parameter model.

The dynamic characteristics of the fuel cell stack were modelled in the three main domains. The delays in fuel flow rate, temperature change and electrical charge were modelled by implementing the recognised differential equations applicable to each domain. The step response

for each domain corresponds with that in available literature. The output voltage responses for current steps were compared to that of the experimental stack and demonstrated acceptable accuracy.

The effect of temperature on the dynamic response is clearly identifiable in the results indicating the benefits of running the PEM fuel cell stack at higher operating temperatures. The increase in transient voltage performance can be used on variable loads, such as electric vehicle motors, to great effect.

As the primary focus of the model is to replicate the electrical output characteristics of an actual stack, the response to pulsed currents as injected by a power conditioning system had to be generated. The model response corresponds to that available in literature and will be used in the actual emulator system to test power electronic hardware that interfaces the fuel cell to a load.

Other phenomena such as polarization curve hysteresis and fuel starvation were observed to be present in the experimental stack and were thus also incorporated into the model to increase the effectiveness of the emulator system.

4. AN OVERVIEW OF THE EMULATOR TOPOLOGY

I. INTRODUCTION

Emulator circuits were developed to accurately reproduce the V-I output characteristics of the electrochemical system [12]. Many do not take into account the complex chemical and thermodynamic effects, instead focussing on the steady state output characteristics at various operating conditions.

Emulator circuits that physically reproduce the static and dynamic behaviour of fuel cells consist mainly of DC-DC converters of various topologies. Increasing the amount of switching devices increases the accuracy of the emulator output characteristics while decreasing the overall system efficiency.

The converter topology presented in [33] reproduces the various dynamic chemical effects including polarization, charge double layer and stack voltage undershoot by using electronic component dynamics. Since it operates from a fixed DC link voltage, the flexibility of the system is limited to particular operating regions. Some recent emulator designs include an active three phase rectifier that is connected to a buck converter [34]. Small signal models and dq0 models are obtained and controlled using linear control theory. To deliver accurate output in the dynamic regions two control loops were employed. The slower outer loop incorporated a PI controller for the active rectifier. The fast responding inner control was based on an open loop controller for the buck converter [34].

Fuel cell system emulators reproduce the output characteristics of the stack, both static and dynamic, as well as the coolant circuit, air supply system and the humidifier. Controllers for each of the subsystems are replicated within the main control philosophy of the DC-DC converters for the emulator system. Commercialized systems can be represented by using these types of emulators, thus enabling product development and testing without the use of the costly chemical systems [35].

Low temperature PEM FC emulators that have been presented in recent works [24], [25], [36], include the effects of the subsystems but are still limited with respect to the emulation of transient phenomena. The emulators designed by Gao et al., [24] and [25], use a complex multiphysical model as described in chapter 3. The drawback of these systems is the use of conventional DC-DC converter topologies that require large filter components to produce the DC output. As stated in [25], these systems cannot replicate fuel cell dynamic phenomena in the short time range below 100ms.

The work presented by Abrahams for a Solid Oxide emulator [37], uses an expensive linear power amplifier to deliver the electrical outputs. The model does however not include the effects of all the transient domains.

The focus of emerging fuel cell emulators is to replicate the voltage response of fuel cells when a pulsed current load at a certain frequency is applied. This will allow designers to predict the effect a DC-DC converter may have on the performance of the fuel cell. Variation of the magnitude and frequency of the pulsed currents changes the voltage response and will affect control system requirements.

It should however be noted that there is a limit to the dynamic response of any power electronic system due to the switching frequency and filter component size. Emulating the dynamic effects of the output voltage of the fuel cell caused by the power conditioning system is not possible if both converters are operating in the same frequency range.

II. SYSTEM DESCRIPTION

The drawback of a conventional emulator system is the fixed DC link voltage at the input of the converter which is usually supplied by a DC power supply. This configuration limits the dynamic capabilities of the system. It was therefore decided that the emulator will be divided into two stages. The first section of the system is the power stage and will function as a controllable power supply. The output of the power stage converter will be connected to the second stage of the emulator system that will replicate the fast dynamic responses of the fuel cell

as predicted by the model. This part of the system will be referred to as the control stage converter of the emulator. Figure 4.1 presents an overall block diagram of the emulator detailing the integration of the hardware, control systems and the fuel cell model.

The power stage converter will serve the following functions:

- Supply the required input power for the system from the three phase grid supply,
- Control the DC link voltage to improve system performance,
- Maintain the system power factor at unity,
- Track the steady state polarization curve of the stack as predicted by the model.

The power stage converter will thus function as an independent emulator that will replicate the steady state output characteristics of the fuel cell.

The control stage converter will perform the following functions:

- Accurately produce the steady state voltage response of the fuel cell,
- Output the dynamic response of the fuel cell,
- Replicate transient and operating phenomena of the fuel cell as predicted by the model.

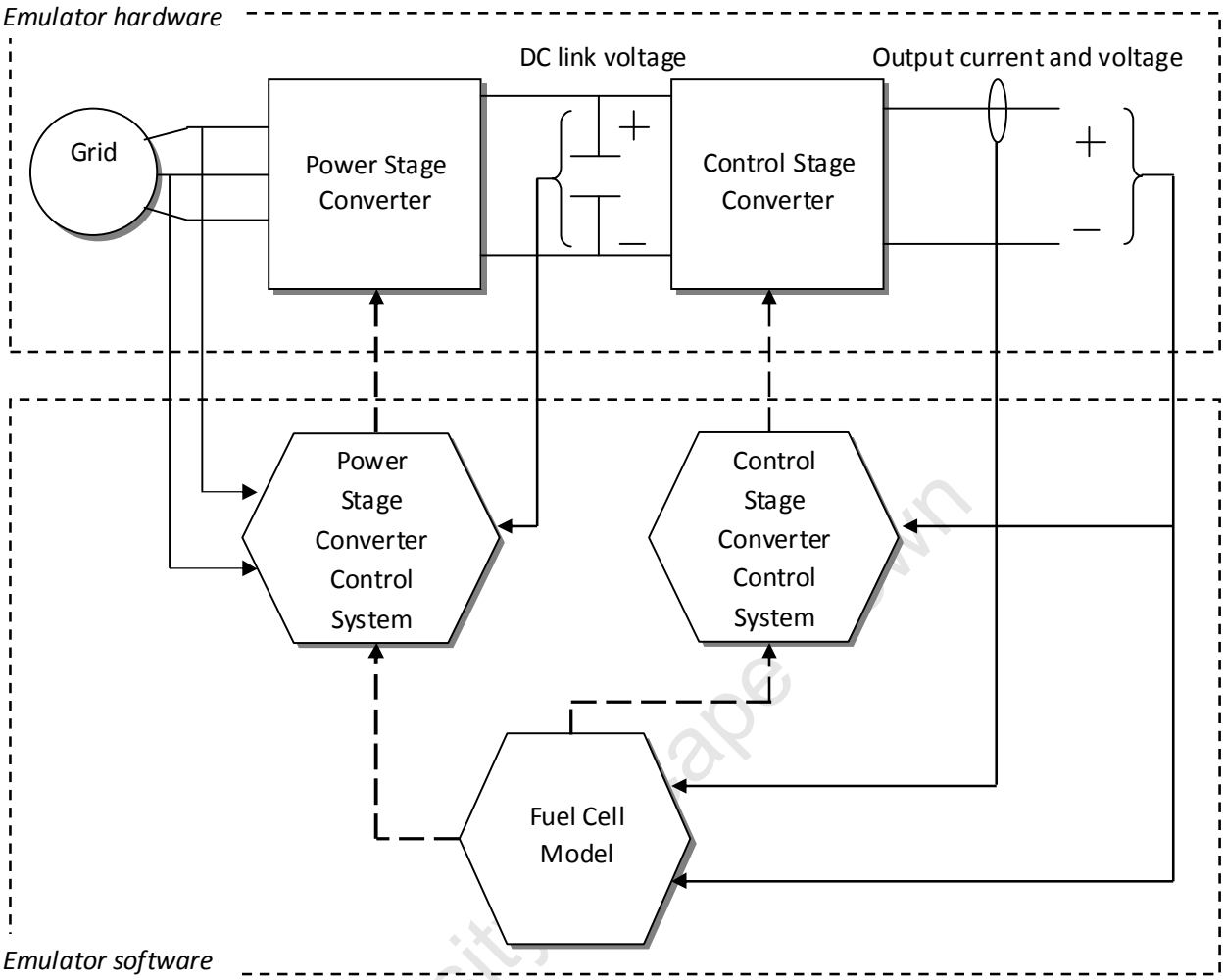

Figure 4.1. Block diagram of the emulator system.

A. Power stage converter topology

The most widely used method to generate a DC voltage from a sinusoidal grid supply is by employing a diode bridge rectifier with a large output filter [38]. The drawbacks of these systems include low input power factor, high level of harmonic content and poor efficiencies. To overcome these effects, controlled rectifiers with pulse width modulated (PWM) switching schemes are used.

The power stage converter is based on the universal voltage source inverter (VSI) topology as shown in figure 4.2. The VSI operates by controlling the DC link voltage and depending on the control strategy employed, the phase currents [39], [40]. The system consists of six fully controlled power electronic switches that are connected to a DC link capacitor, used to smooth

the output current. The three phase input lines can consist of line chokes and capacitors to reduce harmonic feedback into the grid. LCL filter combinations and the damping techniques have been the focus of recent research to improve performance and the reduce filter size [40].

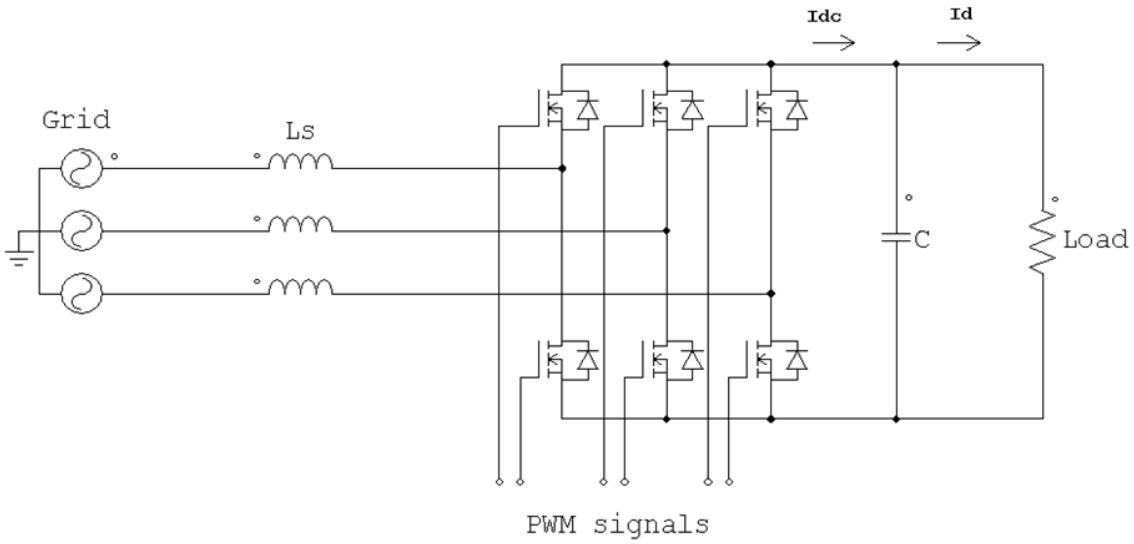

Figure 4.2. Schematic of the voltage source inverter.

The VSI has the capability to operate in all four quadrants by controlling the magnitude and phase angle of the line currents. This allows the system to maintain unity power factor while also controlling the magnitude of the DC link voltage. During rectifier operation, the load will discharge the DC link capacitor. The control system will generate the required error signal and generate the PWM gating signals for the switches to draw more current from the grid side. This will recharge the capacitor and maintain the DC voltage at the required set point. Inverter operation requires that the capacitor be overcharged. The control system will generate the required gating signals to discharge the capacitor and return power to the mains. The space vector control theory that is implemented to achieve this functionality is discussed in chapter 5.

B. Control stage converter topology

The main function of the control stage converter is to emulate the transient behaviour of the fuel cell. Special consideration must be given to the control and hardware design of the converter to accommodate for the fast dynamics of the fuel cell. The converter must respond to sudden changes in load while maintaining the output voltage within a tightly controlled band. As the

power stage generates the steady state DC voltage for the emulator, the control stage topology is a DC-DC converter with specific design consideration for fast dynamics with minimum ripple. The current emulator circuits include the standard buck, boost or full bridge DC-DC converters with large output filter components.

The standard buck converter, as shown in figure 4.3, has thus far been the most widely used topology due to the simplicity of the hardware [25], [33], [36]. A DC power supply generates a fixed DC link voltage which is then stepped down to a desired value as determined by the fuel cell model.

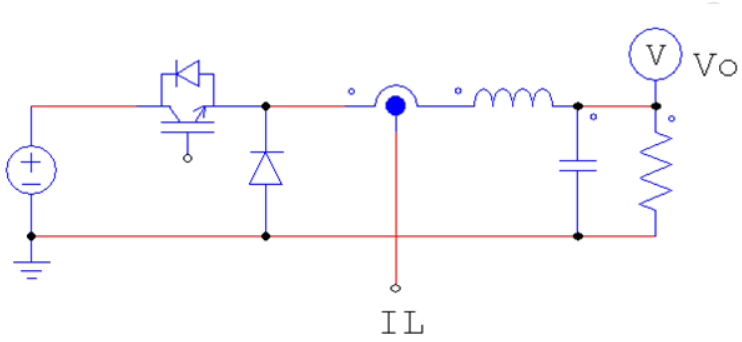

Figure 4.3. Schematic of the standard buck DC-DC converter.

The buck converter is usually designed to operate in the continuous conduction mode to reduce the peak to peak current ripple in the inductor. This requires that the inductance be relatively large. Large filter components have a negative impact on the dynamic response, reducing the ability of the circuit to track a non-linear voltage reference.

Modern DC-DC converters make use of a synchronous topology. This requires that the power Schottky diode that is typically used in DC-DC converters, be replaced by a power semiconductor as shown in figure 4.4. This change in topology mainly increases efficiency as a controlled power semiconductor has a very low on resistance and voltage drop compared to that of the diode.

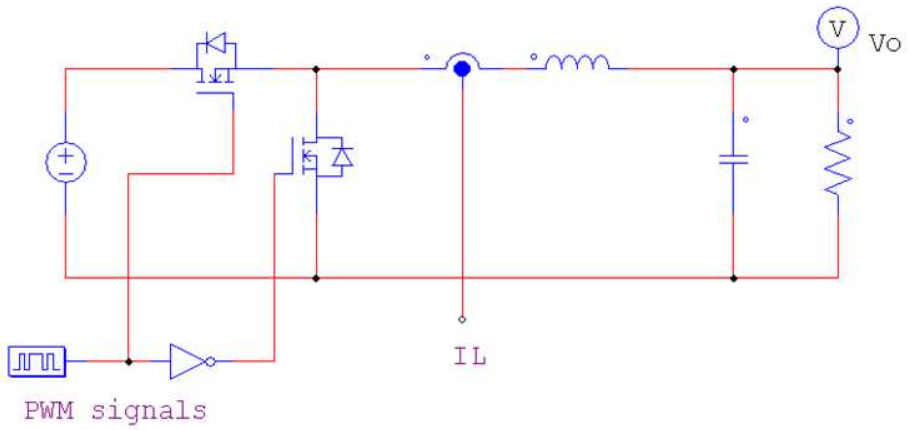

Figure 4.4. Schematic of a synchronous buck DC-DC converter.

The implementation of a synchronous buck converter is a bit more complex that the standard topology. As can be seen in figure 4.4, the converter requires two PWM signals which are inverted relative to each other. To prevent the converter from short circuiting the input, the driver circuit must have a shoot through prevention function and dead time generation built in. This topology does not increase transient performance.

Further modifications were made to the buck converter. An application which requires the buck converter to process very fast dynamics is the VRM (voltage regulator module) for a CPU. These supplies need to deliver a large amount of current with a tightly regulated output voltage to ensure that the CPU operates safely [41]. To reduce the size of the VRM while maintaining performance the multiphase interleaving principle is used.

By using the synchronous buck as the building block, two or more phases can be connected in parallel as shown in figure 4.5. This effectively divides the load current between the parallel phases, increasing the load capacity. The interleaving approach modifies the PWM control scheme by shifting the control signal of each phase by 360°/N, where N represents the total number of phases that are interconnected. With two phases, each control signal is shifted by 180° from each other within the phase spectrum [42].

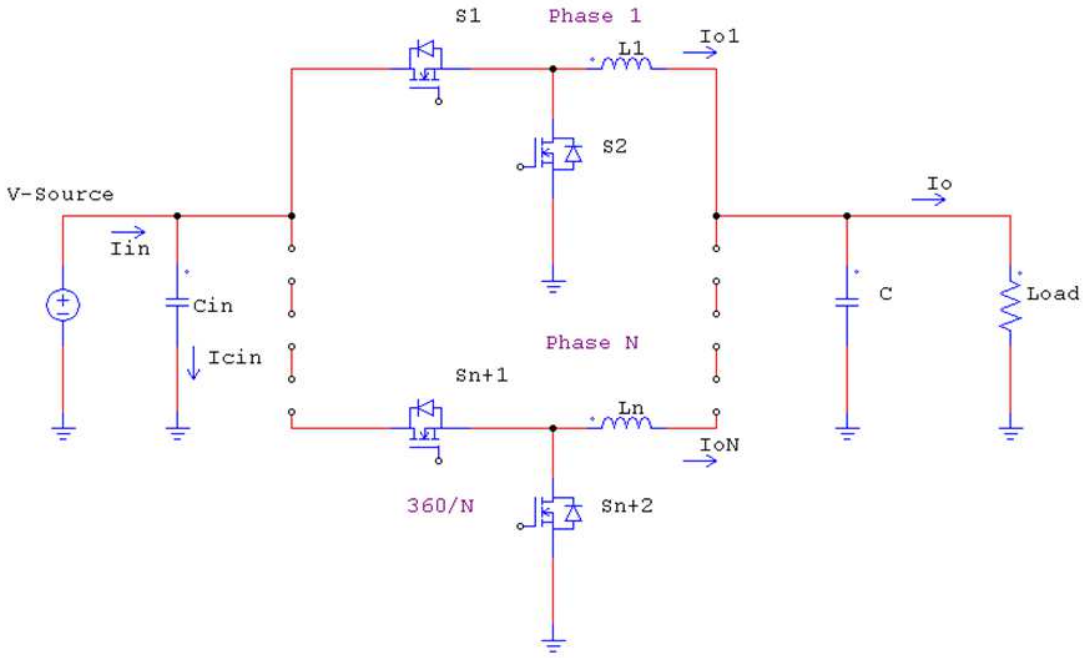

Figure 4.5. Schematic of a multiphase interleaved synchronous buck DC-DC converter.

This operating principle has many advantages over the standard topology. The first, as mentioned before, is the increased load handling capability and efficiency. The second is the increased output ripple frequency allowing the use of smaller filter components. To increase the transient response of the converter, high inductor current slew rates are preferred [43]. By reducing output filter inductance, the current slew rate is increased allowing the use of smaller filter capacitors and increasing transient performance.

The phase shifting operation of the interleaved topology introduces a ripple cancelation effect in the output voltage, as can be seen in figure 4.6, and a decrease in capacitor current as shown in figure 4.7.

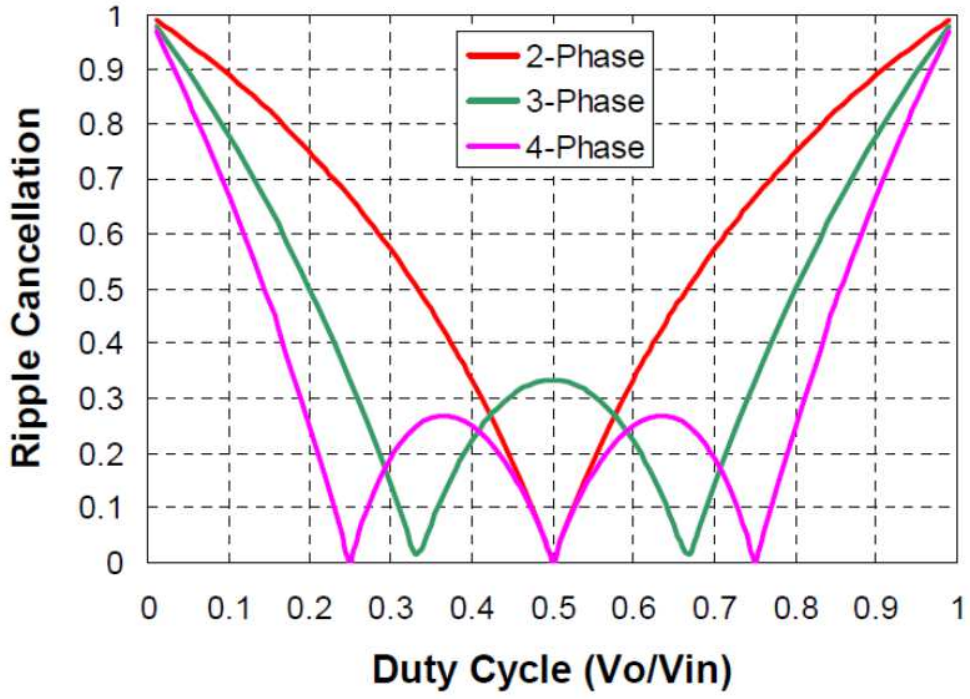

Figure 4.6. Current ripple cancelation effect in the multiphase interleaved buck [43].

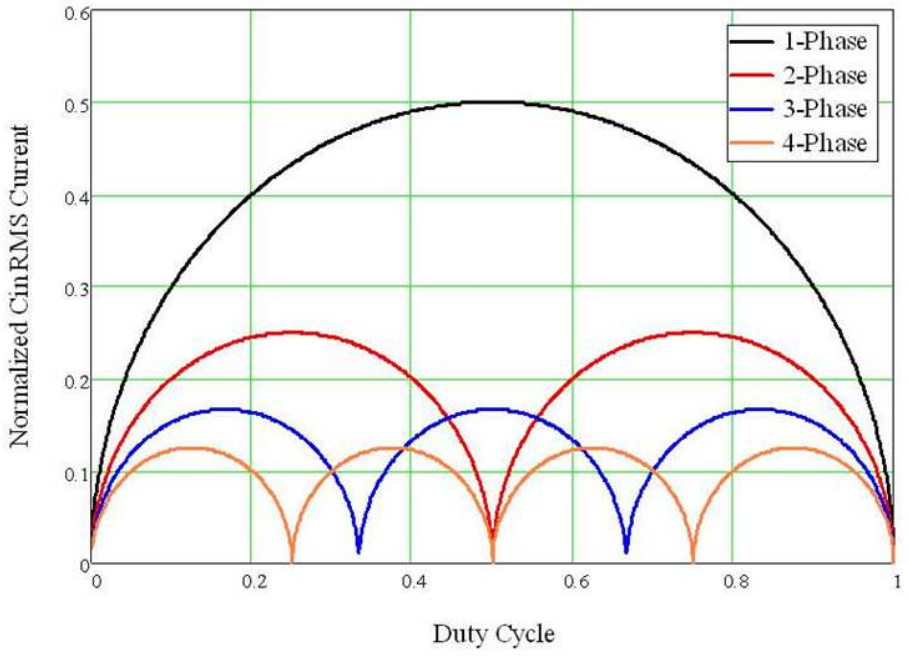

Figure 4.7. Normalized capacitor RMS current in the multiphase interleaved buck [44].

As can be seen from figure 4.6 and 4.7, there is a complete ripple cancelation at certain duty ratios depending on the number of parallel phases used. This phenomenon will be used to greatly improve the emulator performance during steady state.

Besides the benefits of improved transient response and output ripple, the multiphase buck topology also more evenly distributes the thermal losses in the system. Studies have also shown that the cost of the converter in high current applications can be reduced by using this approach [43].

The multiphase interleaved topology does have some inherent drawbacks when implementing. These include the increased complexity of the system by adding more active components, more complex transistor driver circuitry and phase shifted control signals. All these factors must be considered when designing the system and deciding on the number of phases to be used.

Further topology modifications have been presented in recent research; this includes coupled inductors, the introduction of more switches per phase to reduce switching transient effects and the interconnection of phases. Each of these has inherent advantages and disadvantages; however the overriding challenge lies with the implementation of the system as it becomes more complex.

III. EMULATOR OPERATION

To ensure maximum control effort can be executed by the control system via a change in duty ratio for both an upward and downward change in reference during transient conditions, a critical duty ratio of 50% is required. From figure 4.6 and 4.7 it can be seen that both the double and four phase interleaved topologies can be used. Under steady state conditions the control stage converter should operate at a critical duty ratio to ensure that there is a complete cancellation of output voltage ripple as discussed in section II B of this chapter. The control stage and power stage converters are connected back to back as shown in figure 4.8. The two control systems are decoupled to ensure stability under transient conditions.

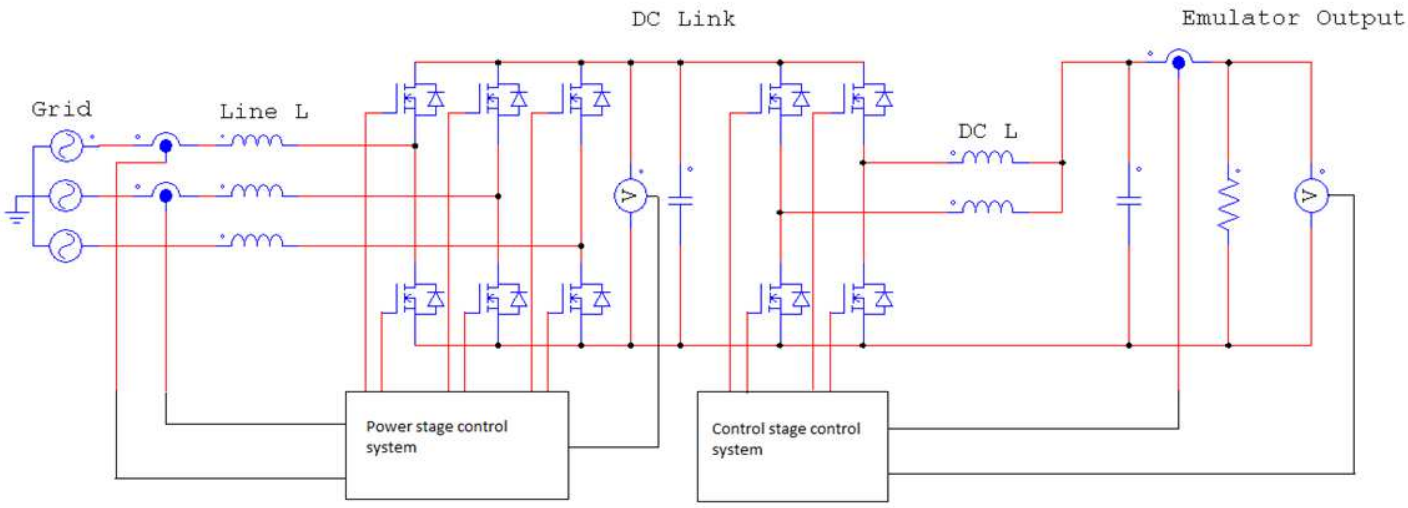

Figure 4.8. Final emulator topology.

Since the four phase system requires a large amount of active devices and control hardware, the double phase system was implemented. A reduced number of phases will also reduce the effect of phase unbalance that may occur in the system.

The salient performance criteria for the control stage converter are reaction time for transients and output ripple cancellation as will be discussed in the following chapters. The power stage converter must ensure that the DC link is kept constant at twice the output voltage to ensure that the control stage converter is operating at 50% duty ratio during steady state conditions. During transient and sub-transient states, the reference voltage of the power stage will be a delayed average of twice the emulator output voltage reference to ensure that instability between the two control systems does not occur.

IV. CONCLUSION

This chapter presented the different topologies that are currently employed in emulator systems. The inherent limitations of normal DC-DC converters were highlighted and used to justify the development of a new emulator design.

The proposed emulator design, based on a two stage approach is presented. First, the power stage is introduced based on a VSI topology. This will produce the DC link voltage and keep input power factor at unity. The second stage is the control stage converter that is based on a multiphase interleaved buck topology, as used in voltage regulator modules for CPUs. The advantages and disadvantages of this type of system is presented and used to select the final number of phases that are employed.

By controlling the DC link voltage to a set value that is twice that of the output of the system, the double phase interleaved buck will operate at a critical duty ratio of 50%. The ripple cancelation at this operating point is such that the output voltage will be DC with a negligible ripple component. This will allow for the design of smaller filter components ensuring that the transient response requirements of the emulator are met.

5. CONTROL SYSTEM DESIGN

I. INTRODUCTION

The multiphase interleaved synchronous step down converter is one of the most widely used topologies in VRM systems that supply power to the central processing units of modern computers. The reduction of filter component size and the corresponding increase in transient response is required to emulate the dynamic phenomena of a fuel cell system. Section II will determine a state space averaged model to derive the small signal transfer functions required for control system design. The open loop responses of the four proposed step down converters are obtained and used for evaluation of the transient response capability. The power stage converter is based on a voltage source converter topology as discussed in chapter 4. Section VII will present the control strategy employed to control the DC link voltage while maintaining grid power factor at unity. The experimental responses of the power stage for reference changes as well as disturbance rejection are presented and evaluated.

II. SMALL SIGNAL MODELS OF THE MULTIPHASE INTERLEAVED BUCK CONVERTER

A. Average model

A very common method for deriving the small signal model of the step down converter is by using the average model. Figure 5.1(a) represents a single phase synchronous buck converter and figure 5.1(b) represents the equivalent average model.

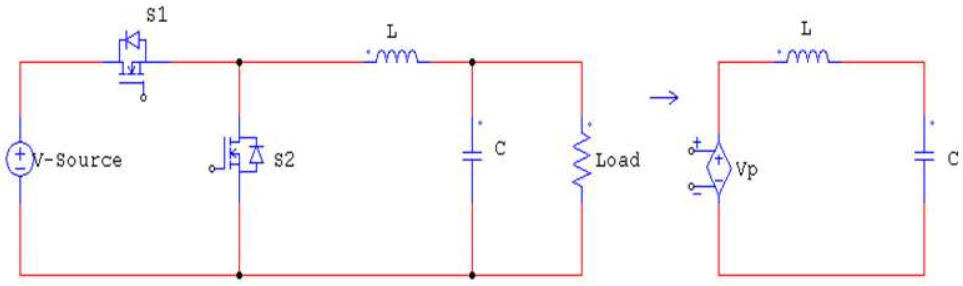

Figure 5.1. Synchronous buck converter (a) equivalent average model (b).

The small signal variations are represented by the controlled voltage source in figure 5.1(b) and are expressed as follows:

$$\tilde{V}_p = (\tilde{V}_{in} + v_{in}) \times (D + \tilde{d}) - v_{in} \times D \tag{5.1}$$

where $\tilde{V}in$ represents the variations in the input voltage and $\tilde{d}$ represents the variations in the duty cycle.

The same principle can be applied to derive the average model of a multiphase interleaved step down converter. The figure 5.2 represents an N-channel multiphase synchronous buck converter and its equivalent average model.

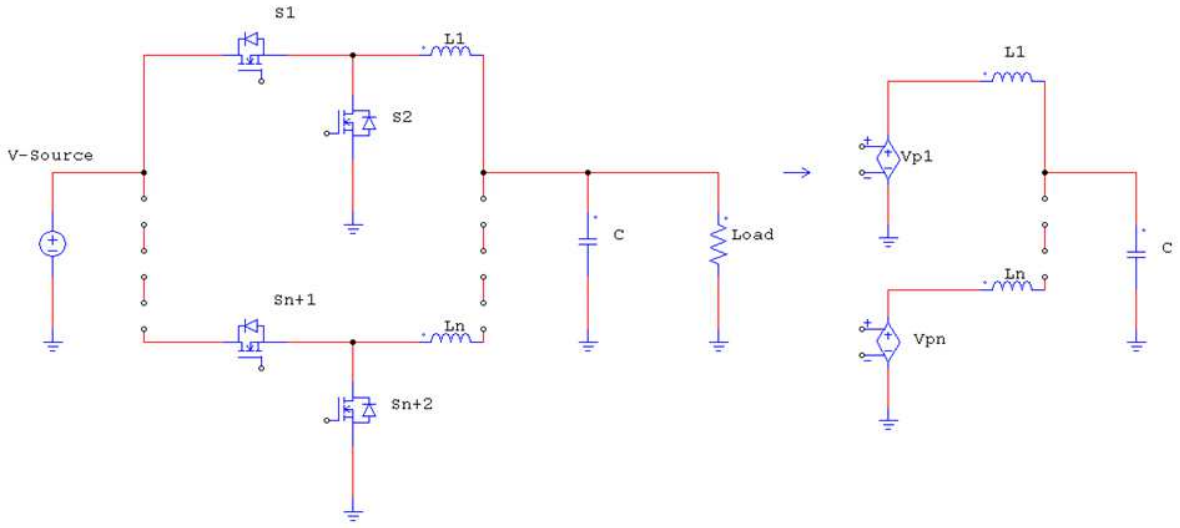

Figure 5.2. Multiphase synchronous buck converter (a) equivalent average model (b).

The following will be assumed for this analysis:

- The input voltage for each phase leg will be equivalent,
- The feedback compensator will generate a single duty ratio that will be fed to all the interconnected phases,
- The small signal variations in the duty cycle and the voltages will be the same for all the interconnected phases.

From the above assumptions it can be concluded that the inductors will effectively be operating in parallel. The equivalent average model can thus be reduced to a single voltage source and equivalent inductance [45].

The equivalent inductance for a symmetric multiphase buck is thus

$$L_{eq} = \frac{L_n}{n} \tag{5.2}$$

where *n* represents the number of interconnected phases. The simplified equivalent circuit model is shown in figure 5.3.

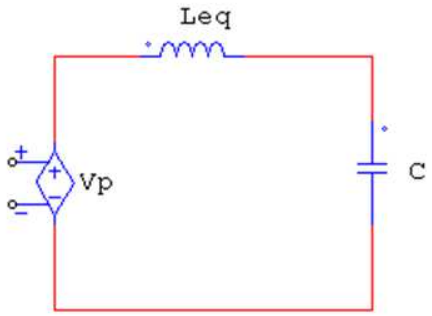

Figure 5.3. Simplified equivalent average model for multiphase buck converter.

B. State space averaged model

The small signal transfer functions of the converter are required to model behaviour under transient conditions and to meet the required control objectives. The state space averaging technique combines the advantages of the circuit averaging and the state space models to obtain accurate small signal models. This technique is described in detail in [46] for a single phase system.

By applying the equivalent multiphase model derived in the previous section we can define the open loop and closed loop transfer functions for a multiphase interleaved step down converter.

For a standard buck converter the small signal control to output transfer function can be defined as follows:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \left(\frac{V_o}{D}\right)\left[\frac{1 + sR_cC}{1 + s\left(R_CC + \left[\frac{R \times R_L}{R + R_L}\right]C + \frac{L}{R + R_L}\right) + s^2LC\left(\frac{R + R_C}{R + R_L}\right)}\right]$$

(5.3)

The small signal input to output transfer function is defined as follows:

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \left(\frac{DR}{R + R_L}\right)\left[\frac{1 + sR_cC}{1 + s\left(R_CC + \left[\frac{R \times R_L}{R + R_L}\right]C + \frac{L}{R + R_L}\right) + s^2LC\left(\frac{R + R_C}{R + R_L}\right)}\right]$$

(5.4)

By replacing the inductance with the equivalent multiphase inductance and ignoring the series resistances of the capacitor and the inductor, the following open loop transfer functions are obtained for a multiphase synchronous system:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \left(\frac{V_o}{D}\right)\left[\frac{1}{1 + s\left(\frac{L_{eq}}{R}\right) + s^2L_{eq}C}\right]$$

(5.5)

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = (D)\left[\frac{1}{1 + s\left(\frac{L_{eq}}{R}\right) + s^2L_{eq}C}\right]$$

(5.6)

The transfer functions will be used to design the linear control system. As can be seen, the system is a standard two-pole low pass filter with a cut-off frequency of $\omega_c = \frac{1}{\sqrt{LC}}$. The magnitude will decay at a rate of -40dB/decade after the cut-off frequency. Variations in D will not cause the shape of the magnitude bode plot to change [46]. If D is increased the magnitude will shift upwards and vice versa.

III. OPEN LOOP RESPONSE OF THE BUCK CONVERTERS

The open loop responses of the four proposed converters are determined and evaluated. These include the standard buck, double phase buck, synchronous buck and double phase synchronous buck converters. To demonstrate the effect of filter component size on the transient response of the converters, an initial capacitor value of 470µF was tested before implementing the designed value of 10µF. The standard buck and double phase buck converters were tested using the following operating parameters:

- V_{in} = 60V,
- V_{out}(nominal)=30V
- D=50%
- C=470µF
- L=250µH
- R=1Ω

The control to output transfer function is as follows:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{30}{5.875e-008\,s^2 + 0.000125\,s + 0.5} \tag{5.7}$$

The bode diagram obtained for the transfer function in figure 5.4 indicates a crossover frequency of 2.3×10^4 rad/s. The simulated overshoot in figure 5.5 is 30% compared to the 44% overshoot obtained for the experimental step response as shown in figure 5.6. The difference between the simulated and experimental results can be attributed to the parasitic resistances and the actual component values of the output filter.

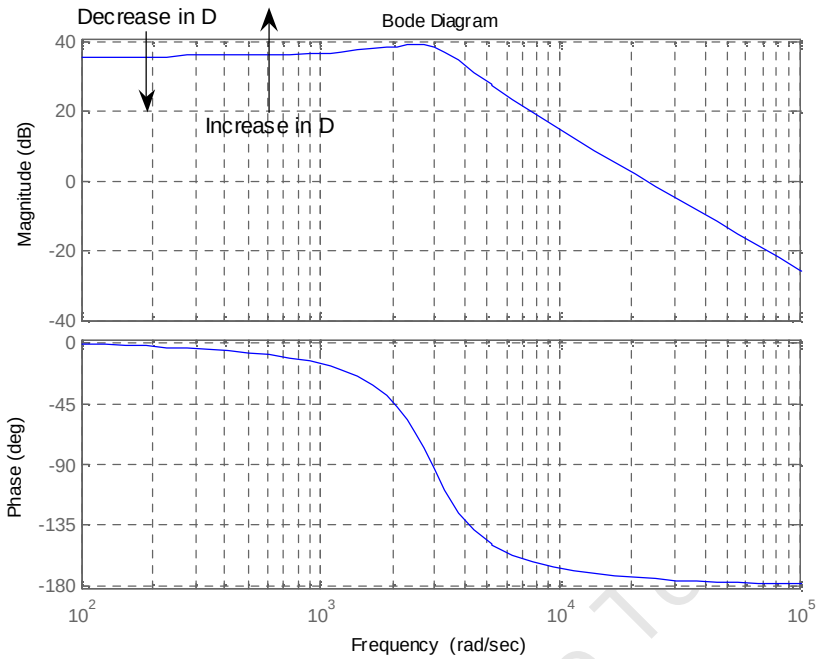

Figure 5.4. Bode Diagram of the single phase buck converter.

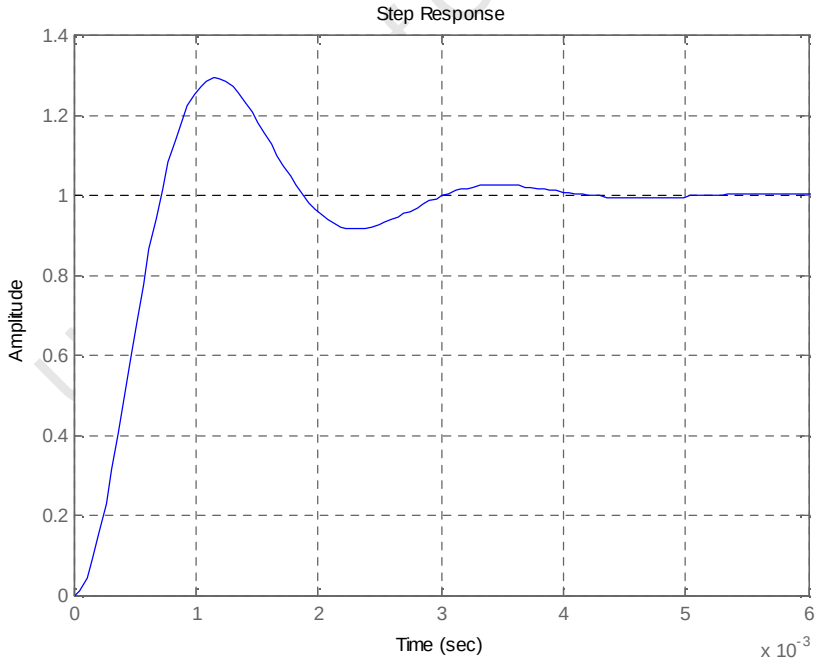

Figure 5.5. Simulated unit step response of the single phase buck converter.

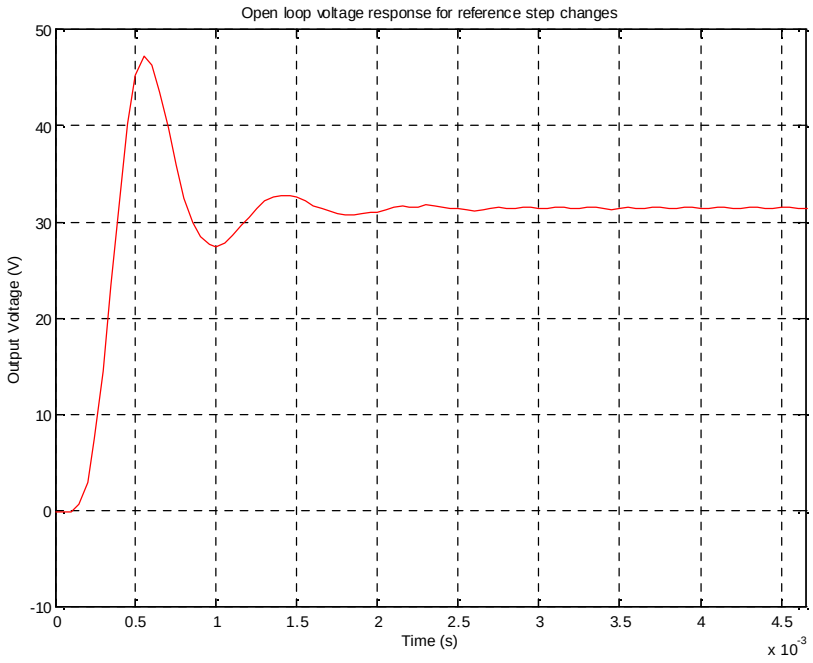

Figure 5.6. Experimental step response of the single phase buck converter.

The double phase system has the same operating parameters as the single phase system with the equivalent inductance now equal to

$$L_{eq} = \frac{250\mu H}{2}$$
$$= 125\mu H$$

The control to output transfer function is as follows:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{30}{2.938e-008\ s^2 + 6.25e-005\ s + 0.5} \tag{5.8}$$

The bode diagram obtained for the transfer function of the double phase system in figure 5.7 shows an increase in the crossover and the cut-off frequency when compared to the single phase system. The simulated overshoot of the system in figure 5.8 is 40% and that of the experimental system is 34% as shown in figure 5.9. The effective inductance is halved and the series resistance

of the two inductors are now connected in parallel, reducing the effect on the system and the error between the simplified transfer function and the experimental system.

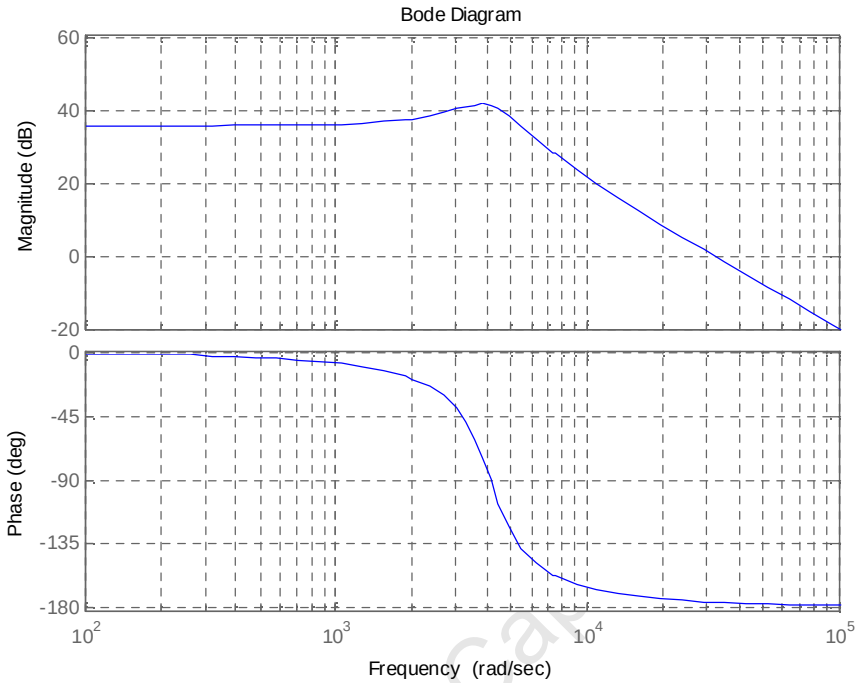

Figure 5.7. Bode Diagram of the double phase interleaved buck converter.

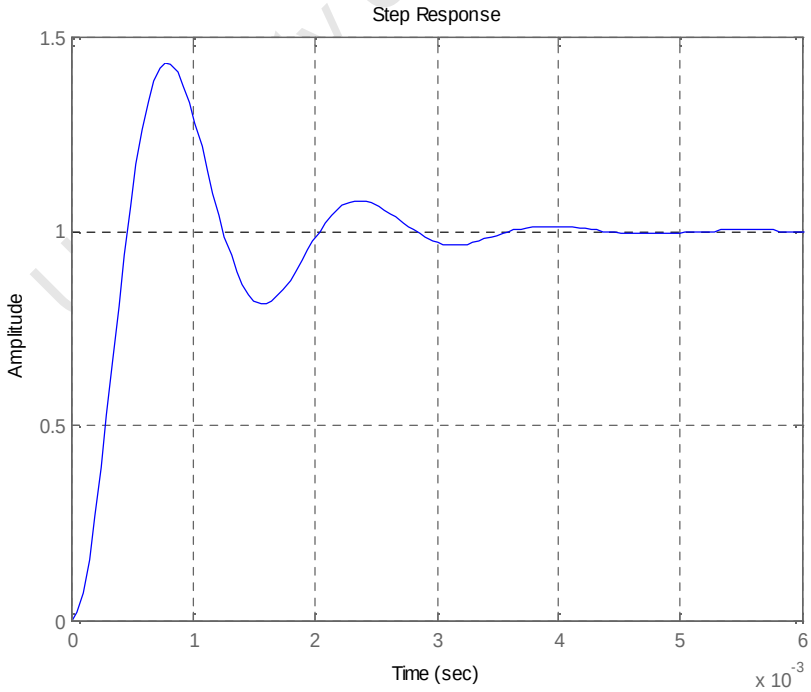

Figure 5.8. Simulated unit step response of the double phase interleaved buck converter.

Figure 5.9 compares the step responses of the experimental single phase and double phase systems. As can be seen there is reduction in rise time and settling time as a result of the reduction in effective filter inductance.

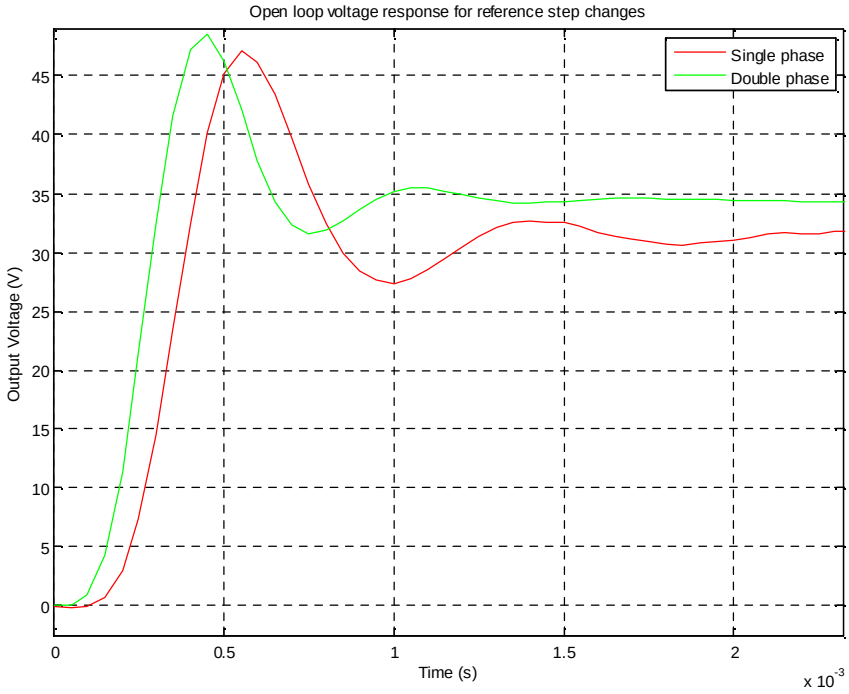

Figure 5.9. Experimental step response of the single phase and double phase interleaved buck converters.

The synchronous double phase interleaved buck converter has the same parameters as the normal double phase interleaved buck during open loop testing; the capacitance is reduced to the design value of 10µF as calculated in chapter 6 to demonstrate the effect on the transient response.

The control to output transfer function is as follows:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{30}{6.25e-010\ s^2 + 6.25e-005\ s + 0.5} \tag{5.9}$$

The synchronous buck converter under discussion has an output filter capacitance that is reduced to 10µF compared to the 470µF filter capacitance of the normal freewheeling diode based buck converters. The reduction in filter capacitance has a great effect on the system bandwidth and

transient response as shown in the bode plot, figure 5.10, and the unit step response, figure 5.11. The final design implemented for the emulator control stage was the double phase interleaved synchronous buck with a smaller output capacitor. The reduction in open loop settling time and increase in system bandwidth is required to achieve acceptable dynamic performance and simulate the transient response of the fuel cell system.

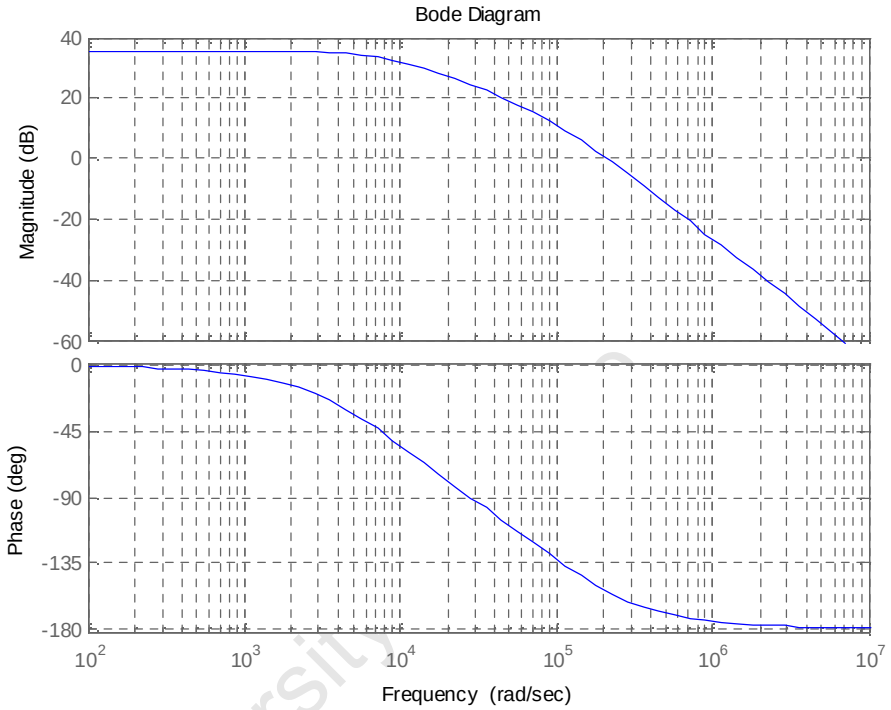

Figure 5.10. Bode Diagram of the double phase interleaved synchronous buck converter.

The cut off frequency of the final output filter design is calculated as follows:

$$\omega_c = \frac{1}{\sqrt{LC}}$$

$$= \frac{1}{\sqrt{125 \times 10^{-6} \times 10 \times 10^{-6}}}$$

$$= 28284.27 rad/s$$

$$= 4500 Hz$$

(5.10)

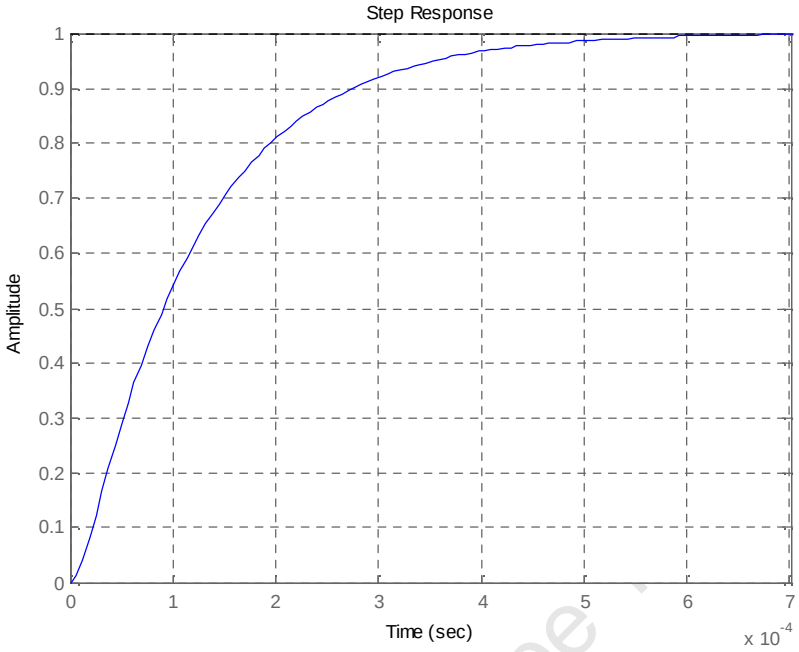

Figure 5.11. Simulated unit step response of the double phase interleaved synchronous buck converter.

The transducers employed are quite susceptible to noise pickup and will transfer the switching noise from the converter output to the analogue to digital converters (ADC) of the control system. Figure 5.12 shows the raw voltage response signal as converted from the ADC channels. To ensure stable converter operation, the values from the ADC are fed through a second order low pass filter with a cut-off frequency of 2500Hz and a damping factor of 0.5. The under damped filter allows the control system to respond to actual variations in output voltage and cuts out the high frequency voltage spikes caused by the switches in the synchronous converter. The filtered output voltage signal is shown in figure 5.12. There is a delay of about 100µs caused by the filter. This was deemed acceptable as the maximum sampling frequency of the control hardware while running the fuel cell model was 100µs, thus causing a delay of only a single sampled value.

The experimental step responses for the double phase converters, using a 470µF and 10 µF filter capacitor respectively, are shown in figure 5.13. The smaller filter capacitor size results in a significant reduction in rise time and overshoot.

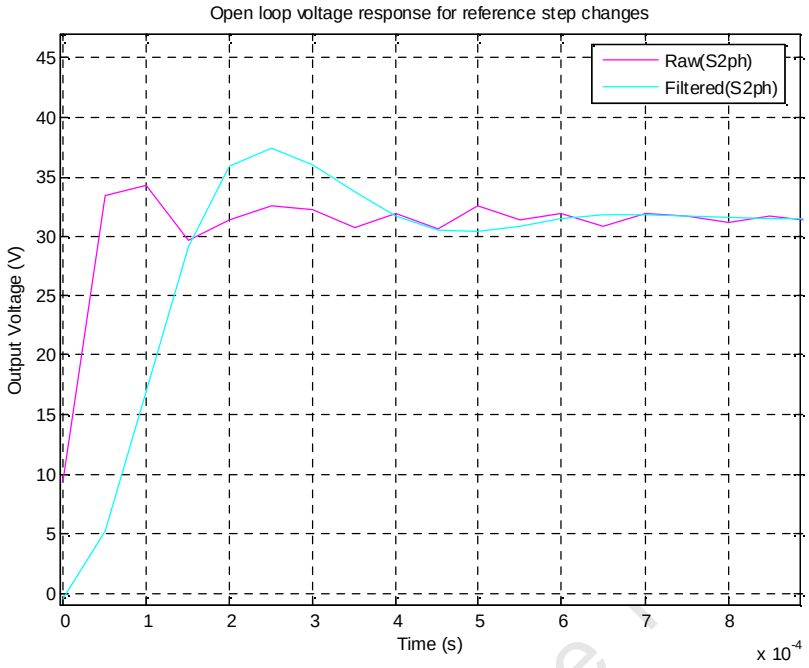

Figure 5.12. Experimental step response of the synchronous double phase interleaved buck converter, filtered and unfiltered.

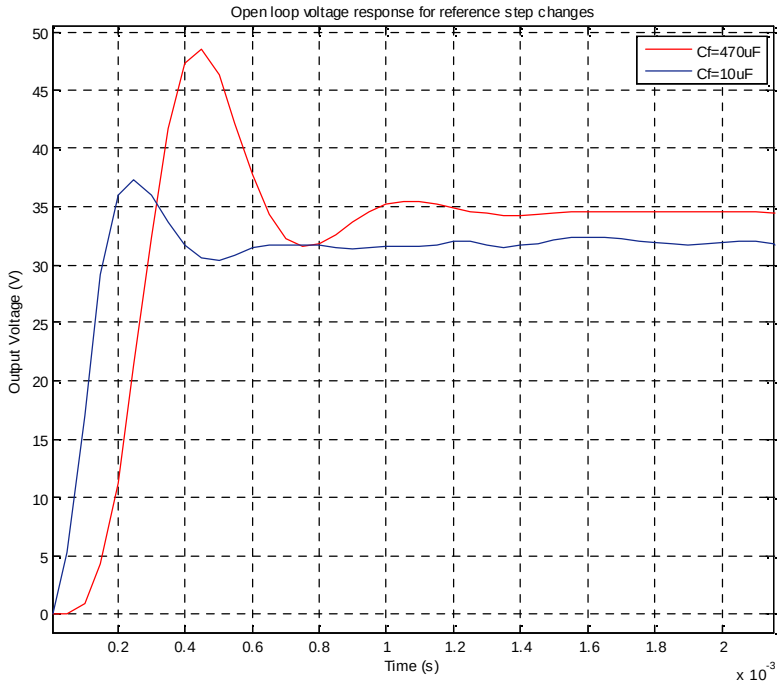

Figure 5.13. Experimental step response of the double phase and synchronous double phase interleaved buck converters.

IV. IMPLEMENTATION OF THE DIGITAL CONTROL SYSTEMS

The digital controller was implemented on a dSpace DS1104 prototyping system. The dSpace platform allows for real time implementation and parameter variation. This allows for quick control system verification. The DS1104 has a 250MHz Digital Signal Processor (DSP) with a 64bit floating point math processor. The dSpace platform loads C code generated by the real time workshop of the MATLAB Simulink interface directly to the DSP. The control system is modelled in Simulink and is dependent on the sampling time selected in the solver.

The eight analogue to digital converters (ADC) are incorporated into the model and are used to import the feedback from the transducers implemented in the hardware platform. The sampling time selected in the solver also determines the speed of the feedback loops in the control system. This causes a limitation on the speed of the control system as the sampling time is limited by the complexity of the MATLAB code.

Figure 5.14 illustrates the different actions taking place during each clock cycle. If the computational time exceeds the sampling time an overflow error occurs resulting in a failure to execute the code in real time.

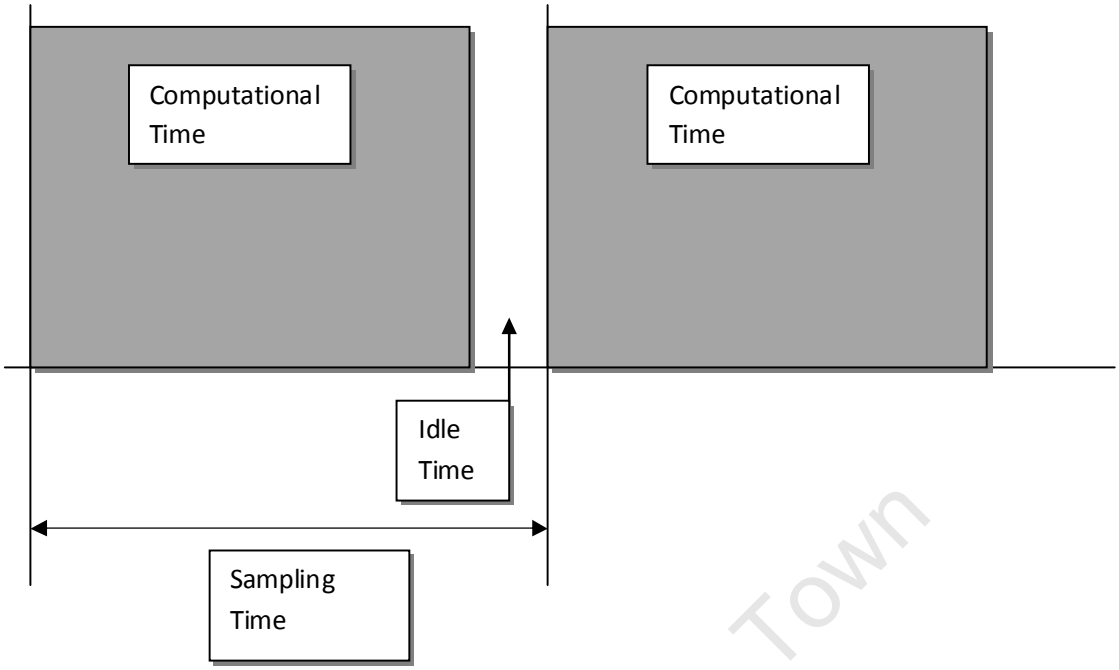

Figure 5.14. Illustration of each clock cycle on the DSP.

V. CONTROL STAGE CONTROLLER DESIGN

For DC-DC converters the output voltage has to track the reference voltage with a negligible error under steady state and a fast recovery time under transient conditions. For a linear control system negative feedback or feed forward compensation can be used. These types of compensators will adjust the duty ratio to achieve the required output voltage with good disturbance rejection characteristics [47].

The feedback compensation network of the closed loop converter is used to create the required frequency response such that the converter remains stable in the presence of noise or disturbances. Commonly used frequency response techniques are used to design the digital controller that will be implemented in the dSpace platform.

The relative stability of the control system can be determined from the bode plots by interpreting the gain and phase margins. The gain margin is the value of the system gain when the phase shift reaches -180°. If the value of the gain is forced below zero while the phase response is -180° or

smaller, the system will be unstable. The gain of the system should be high at low frequencies to ensure minimal steady state error. The phase margin is the value of phase shift at unity gain or at 0dB on the bode plot. The phase margin determines the transient response of the output voltage under fast changes in load or input voltage.

The crossover frequency of the system is the frequency where the gain is 1 or 0dB. Ideally the crossover frequency should be as high as possible but about an order of magnitude below the switching frequency. This will ensure that the system will respond quickly under transient conditions and will not be affected by the switching noise caused by the converter.

A phase margin of 45° to 60° and a gain margin of 6dB are desirable. This can be achieved by implementing a linear controller.

The three conventional types of linear controllers are PI, PD and PID controllers and are termed as phase-lead, phase-lag or lead-lag compensators. The lead type or differential controllers can become unstable for significant amounts of derivative gain in the presence of electromagnetic interference (EMI) and switching noise. As such only the PI or phase-lag compensator was employed.

The transfer function of the PI controller as depicted in figure 5.15 is:

$$\begin{aligned} G_c(s) &= K_P + \frac{K_I}{s} \\ &= \frac{K_P s + K_I}{s} \\ &= \frac{K_P s + \frac{K_P}{T_I}}{s} \end{aligned} \tag{5.11}$$

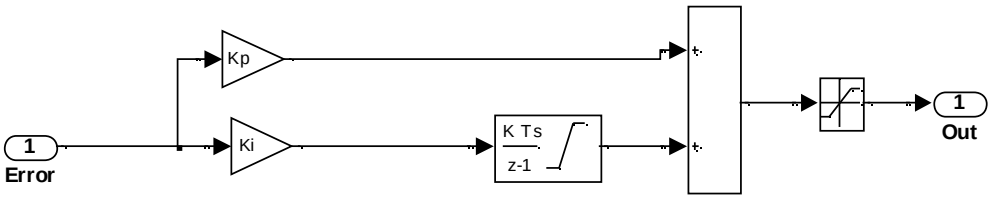

Figure 5.15. Block diagram of the discrete PI controller.

The settling time of the open loop step response from the implemented double phase synchronous buck was experimentally determined to be around 150µs as shown in figure 5.12. As discussed in the previous section, the sampling time of the control system in dSpace is limited to 100µs while running the fuel cell model. It is thus not practically viable to reduce the settling time of the voltage response in the emulator system without moving the control system to an external embedded DSP that runs at a higher clock frequency. The gains of the PI controller were thus designed to reduce the error under steady state and to reduce the amount of overshoot during transients at the cost of a slower settling time.

The DC gain of the PI controller was adjusted in real time to achieve satisfactory results. The PI controller places one pole at the origin and one zero was placed at 5000 radians/s. The resulting transfer function of the controller is given as follows:

$$G_c(s) = 0.5 + \frac{2500}{s} \tag{5.12}$$

The simulated step response of the control system is presented in figure 5.16 for both continuous and discrete time. The response is under-damped with a settling time of 3ms. The converter was modelled in Power Simulator (PSIM) to verify the response. As shown in figure 5.17, the response is similar to that of the unit step response for the closed loop transfer function.

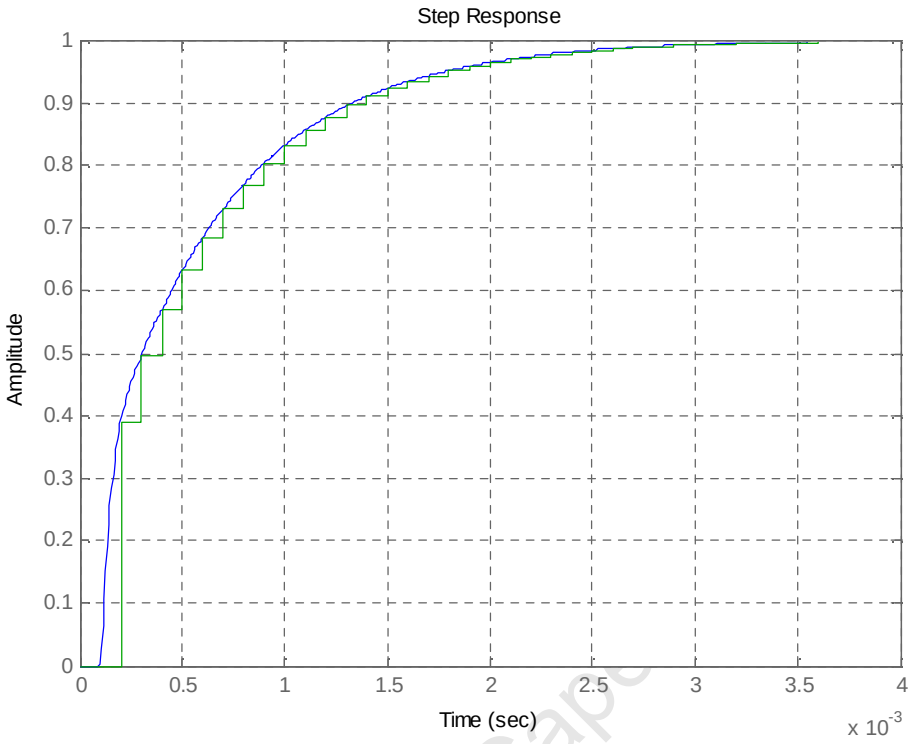

Figure 5.16. Simulated unit step response of the closed loop transfer function.

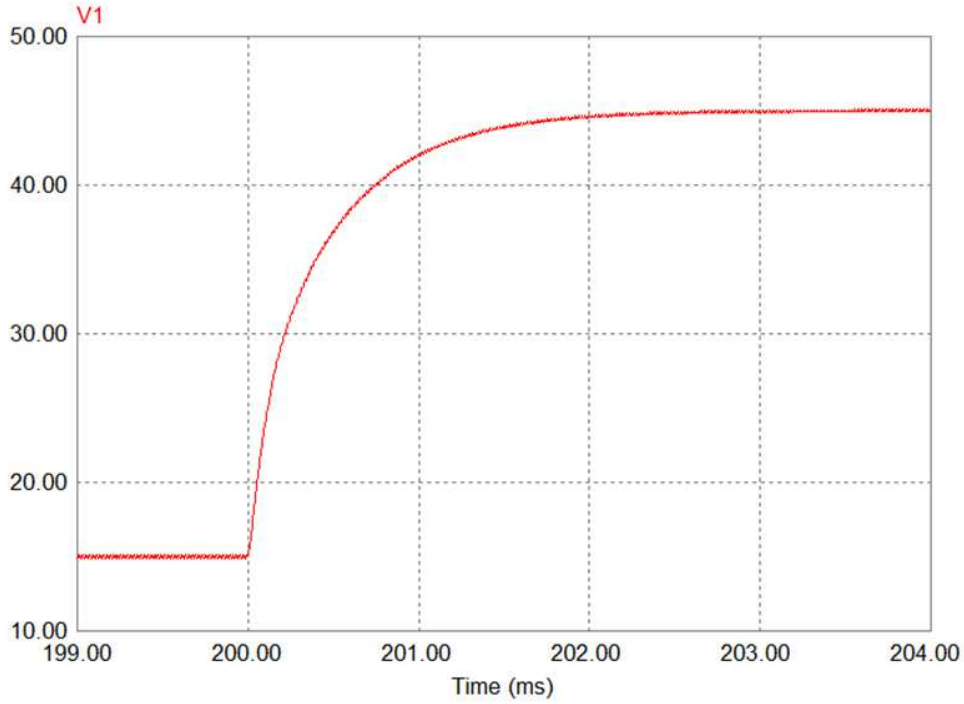

Figure 5.17. Step response of the converter modelled in PSIM.

The obtained experimental step response for the closed loop system is shown in figure 5.18 and confirms the results obtained in simulation.

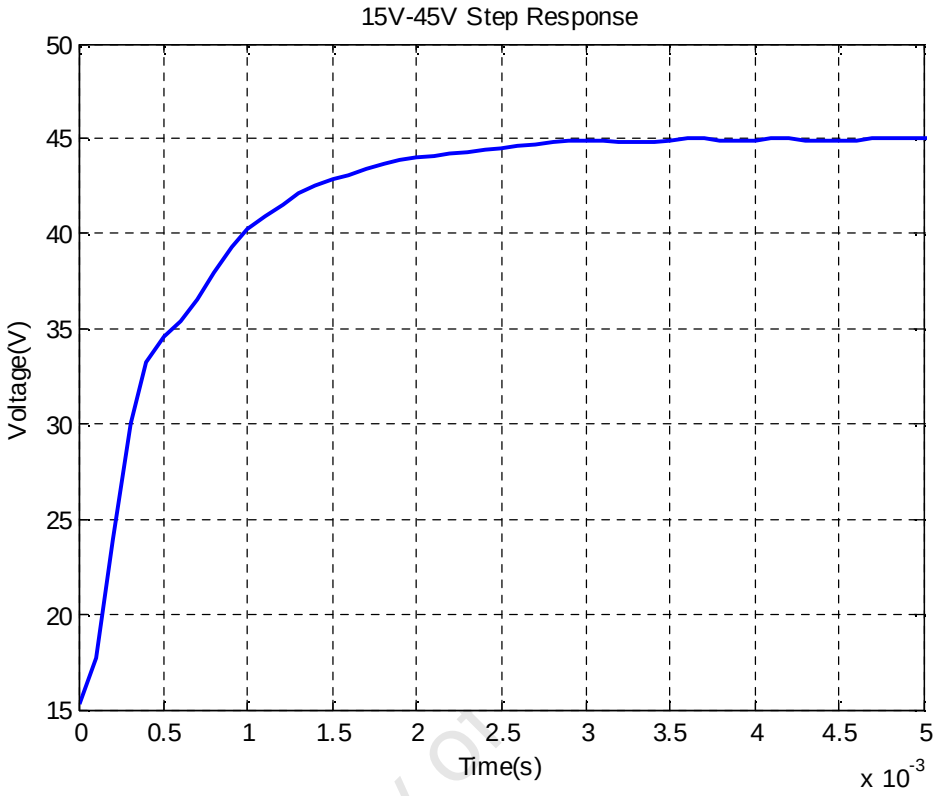

Figure 5.18. Step response of the experimental system.

VI. INTEGRATOR WINDUP

In the feedback control system the output of the actuating subsystem can saturate due to system limitations. Once this occurs the output of the control to the process stops changing and the feedback path is opened. If the error between the reference and the feedback is still applied to the input of the integrator, the output of the integrator will increase or wind up. The result of this process is a very large overshoot and very poor transient response. The integrator is thus an unstable element under open loop conditions and must be stabilized.

This problem is overcome by using antiwindup techniques. Two of these are integrator reset and back calculation.

VII. CONTROL OF THE POWER STAGE CONVERTER

Any three phase system can be represented as set of rotating vectors. By locking on to the rotation ωt with the use of a phase locked loop (PLL), the rotational effect can be removed and the system can be analysed in DC components. Transformation from a three phase system to a synchronous reference frame is accomplished by using the Park and Clarke transforms as given in equation 5.13.

$$\begin{bmatrix} A_q \\ A_d \\ A_0 \end{bmatrix} = \frac{\sqrt{2}}{3} \begin{bmatrix} cos\emptyset & \cos\left(\emptyset - \frac{2\pi}{3}\right) & \cos\left(\emptyset + \frac{2\pi}{3}\right) \\ sin\emptyset & \sin\left(\emptyset - \frac{2\pi}{3}\right) & \sin\left(\emptyset + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a_a \\ a_b \\ a_c \end{bmatrix} \tag{5.13}$$

The control of the power stage converter is based on standard voltage orientated control (VOC) for active rectifiers [48]. This type of control is based on the use of the dq0 frame with the d-axis aligned on the grid voltage vector as shown in figure 5.19.

The direct axis current component reference, i_d^*, is used to control the magnitude of the DC link voltage while the quadrature axis current component reference, i_q^*, is controlled to obtain unity power factor.

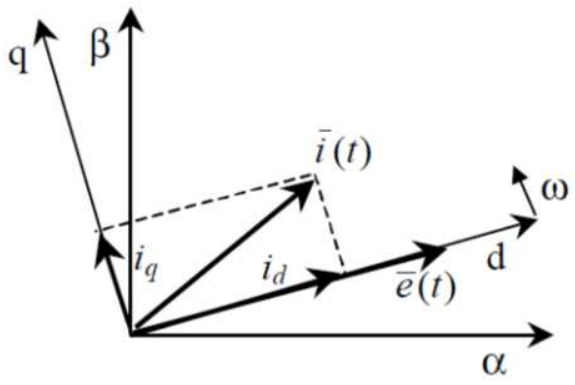

Figure 5.19. Current components used for voltage oriented control.

Figure 5.20 depicts the control system as used with the SV PWM scheme. The grid voltages and currents are transformed to the dq-frame using the angle calculated from the PLL.

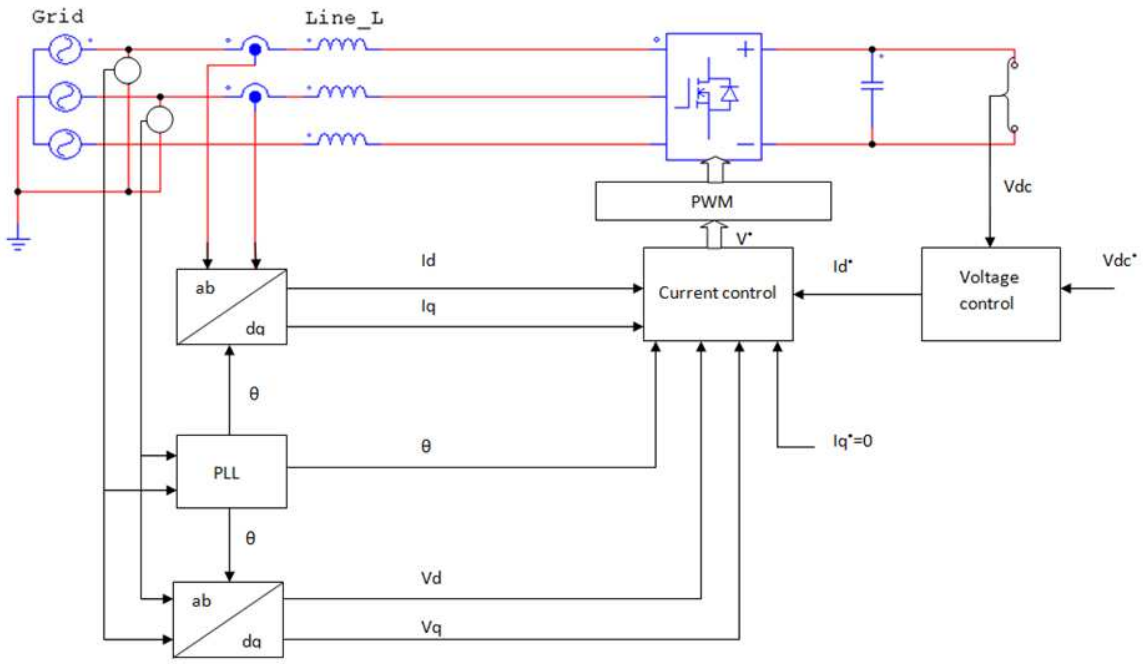

Figure 5.20. Block diagram of the power stage control system.

Figure 2.21 shows the cascaded control structure of the system. The outer voltage control generates the direct axis current reference to maintain the DC link voltage at the required set point. By keeping the quadrature current at 0, the system ensures that the displacement power factor is kept at unity, thus drawing only active power from the grid connection. The calculated direct and quadrature axis voltage references are added to the measured values and transformed to a voltage reference phasor V_s.

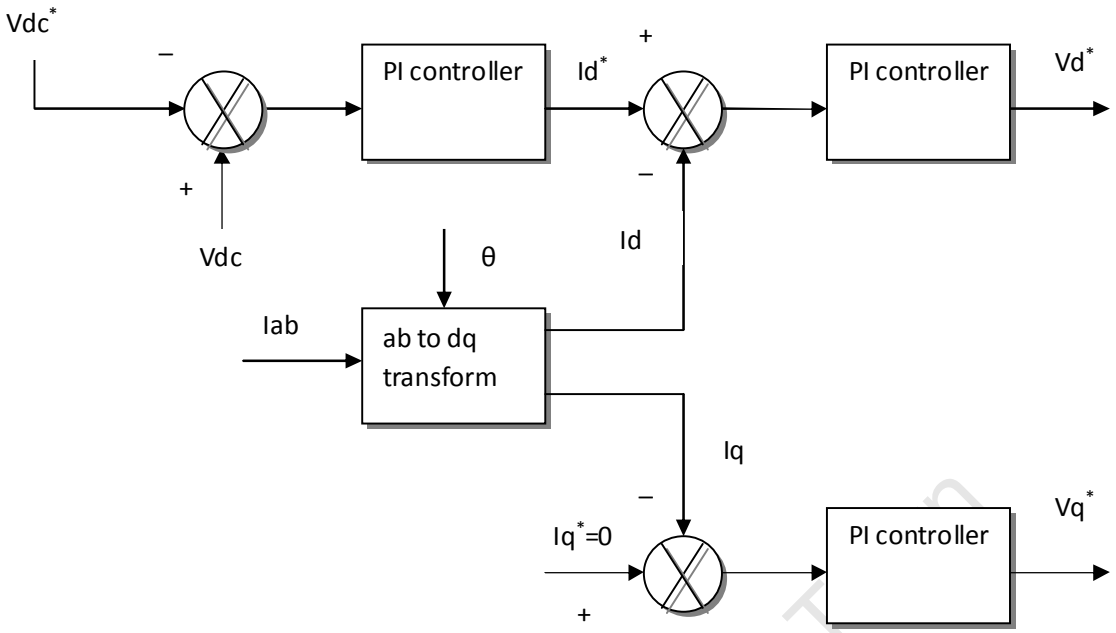

Figure 5.21. Block diagram of the current and voltage control.

As can be seen from figure 5.22, the reference phasor V_s can be represented by turning the two adjacent phasors on for a period of time. Each phasor represents a certain set of switch states that will be used to drive the semiconductor devices via the gate circuitry. A detailed explanation on SVM theory and other inverter control methods can be found in [49].

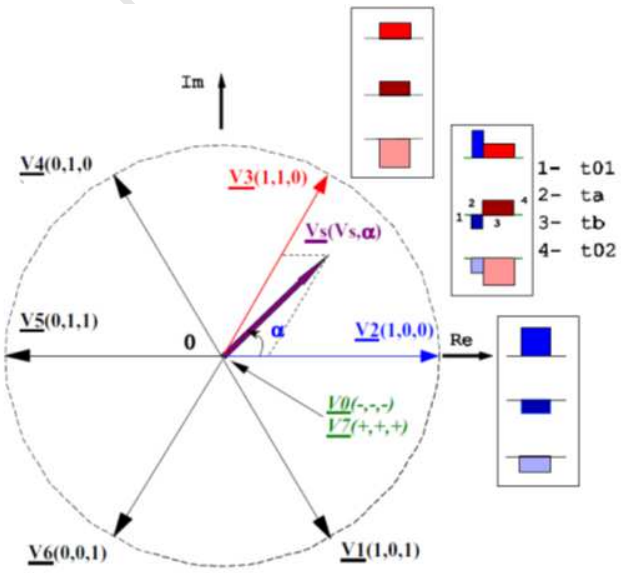

Figure 5.22. State phasors and switched states for each of the sectors used in SV PWM [49].

VIII. POWER STAGE CONTROLLER DESIGN

A. Digital current controller design

The current control loop consists of several blocks that make up the final transfer function as shown in figure 5.23.

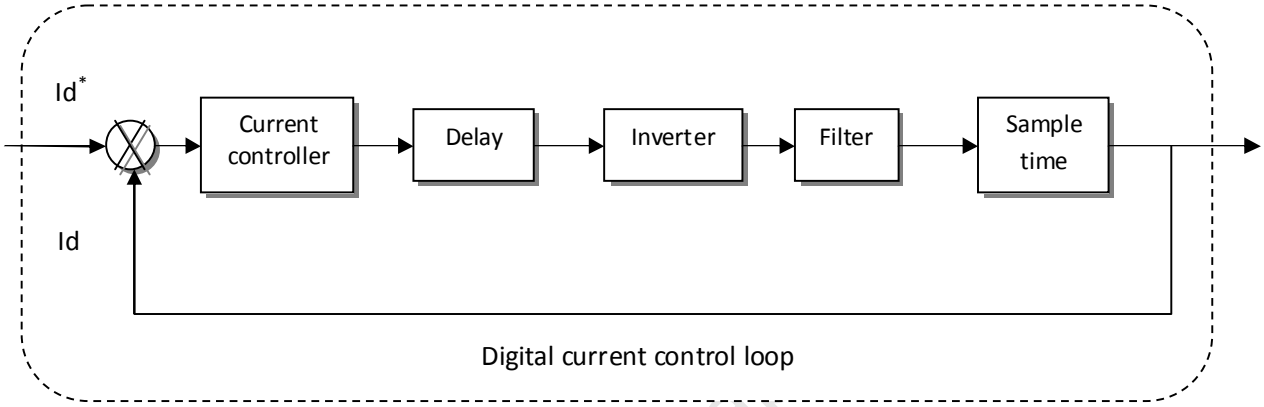

Figure 5.23. Block diagram of the digital current control loop.

The first is the transfer function for the PI controller as stated in equation 5.11. The other blocks are as follows:

Control block transfer function:

$$G_c = \frac{1}{1 + sT_s} \tag{5.14}$$

where T_s represents the sampling time of 170µs.

Converter block transfer function:

$$G_{conv} = \frac{1}{1 + s.0.5T_{sw}} \tag{5.15}$$

where T_{sw} represent the switching period of 200µs of the converter.

The transfer function of the grid side filter:

$$G_{filter} = \frac{1}{R + Ls} \tag{5.16}$$

where L and R represent the sums of the grid and filter inductance and resistance.

The transfer function of the sampling:

$$G_{sample} = \frac{1}{1 + s.0.5T_s} \tag{5.17}$$

The transfer function of the complete current loop in a simplified form is as follows [40]:

$$G_{current} = \left(\frac{K_p s + K_i}{s}\right)\left(\frac{1}{1 + sT_{\sum 1}}\right)\left(\frac{K_e}{sT_e + 1}\right) \tag{5.18}$$

where K_e =1/R, T_e=L/R and $T_{\sum 1} = T_s + 0.5T_{sw} + 0.5T_s$.

By using the optimal modulus criterion and rearranging the relations the current loop is written as follows:

$$G_{current} = \frac{1}{2sT_{\sum 1}(1 + sT_{\sum 1})} \tag{5.19}$$

The gains of the current controllers are calculated using equations 5.18 and 5.19 as follows [40]:

$$K_p = \frac{T_e}{2K_e T_{\sum 1}} = 3.097 \tag{5.20}$$

$$K_i = \frac{K_p}{T_e} = 37.17 \tag{5.21}$$

During physical implementation of the current controller on the dSpace platform it was found that the gains for the direct axis current control had to be reduced by a factor of three to reduce the effects of instability.

The quadrature current controller gains were reduced to K_p=0.5 and K_i=1. This was done as the output from the dq transformation block produces an oscillation at twice the grid fundamental frequency. The oscillations are caused by the unbalance in the magnitude of the currents and voltages; the oscillatory effect is increased when only two phases are used to determine the dq component values.

B. Digital voltage controller design

The PI controller gains for the outer voltage loop were designed using the symmetric optimum criterion [50]. The block diagram for the digital control loop is presented in figure 5.24.

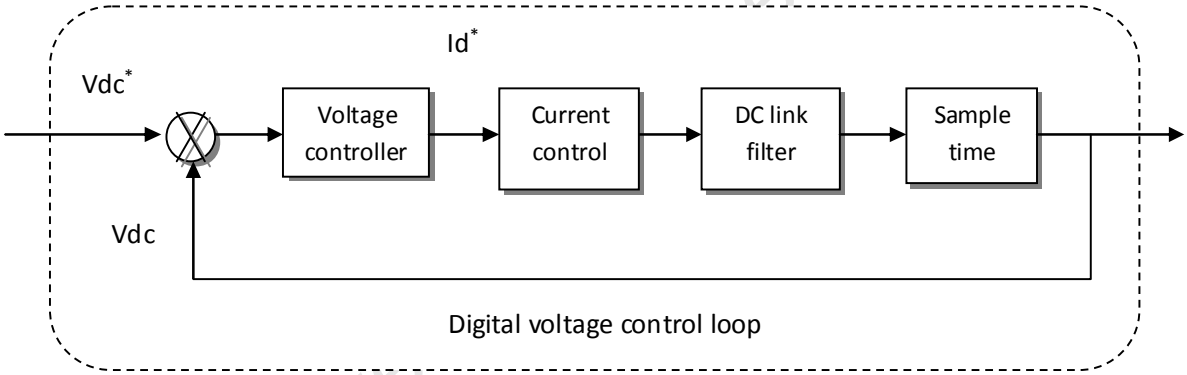

Figure 5.24. Block diagram of the digital voltage control loop.

The closed loop transfer function of the current control can be simplified to a first order function:

$$G_{cur} = \frac{1}{3sT_s + 1} \tag{5.22}$$

The controller gains for a transfer function with a double integrator can be determined by using the symmetric optimum method [48].

The crossover frequency (ω_{cr}) and phase margin (φ) for the voltage loop are related as follows:

$$\omega_{cr} = \frac{1}{3aT_s} \tag{5.23}$$

$$a = \frac{1 + cos\varphi}{sin\varphi} \tag{5.24}$$

$$a = \sqrt{\frac{T_I}{3T_s}} \tag{5.25}$$

The proportional gain of the PI controller at the crossover frequency is given as

$$K_p = \frac{C_{dc}}{2\sqrt{3}aT_s} \tag{5.26}$$

If a 45° phase margin is chosen then a=2.4 and the gains of the PI controller are derived as follows [48]:

$$K_p = 0.12\frac{C_{dc}}{T_s} = 3.317 \tag{5.27}$$

$$K_I = \frac{K_p}{17T_s} = 1148 \tag{5.28}$$

During implementation it was found that such high gains made the controller extremely aggressive and susceptible to overcompensation for switching noise running on the feedback path. As the main goal of the DC bus was to remain stable and react relatively slowly when

compared to the response times of the control stage converter it was deemed acceptable to reduce the gains to 0.1 for K_p and 5 for K_I.

IX. EXPERIMENTAL RESULTS OF THE POWER STAGE CONTROL SYSTEM

A. Reference step response

The system was connected to the three phase grid supply at the input terminals and to a resistive load at the DC link. A change in DC voltage results in a proportional change to the output current. The simultaneous change in voltage and current for a DC voltage reference step is done to verify the closed loop stability of the cascaded control system.

The DC link voltage step response for changes in voltage reference is shown in figure 5.25. As shown, the DC link voltage was varied from the minimum design value of 50V to the maximum value of 70V with a maximum step size of 15V. There is an overshoot/undershoot of about 16% before settling at the new set point. The settling time is about 300ms as shown in figure 5.26. The slow response is acceptable as long as there is no instability or oscillatory effects as the control stage converter will react fast enough to stay on the fuel cell reference during transient states. The main function of the power stage control system is to remain stable and to maintain the DC link at an average of twice the emulator output voltage during operation. Very fast reaction times were thus not required for the power stage converter and a settling time of 0.3s was deemed acceptable.

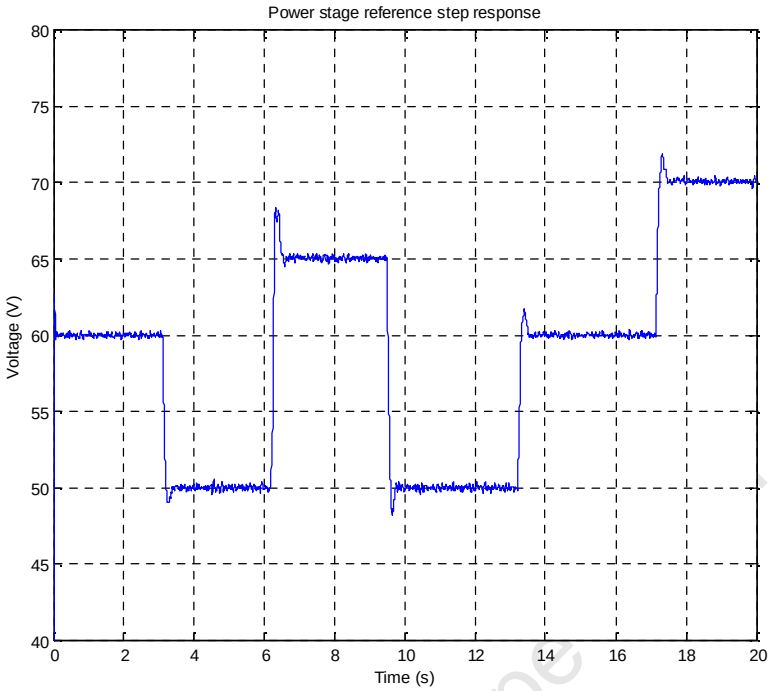

Figure 5.25. DC link voltage response.

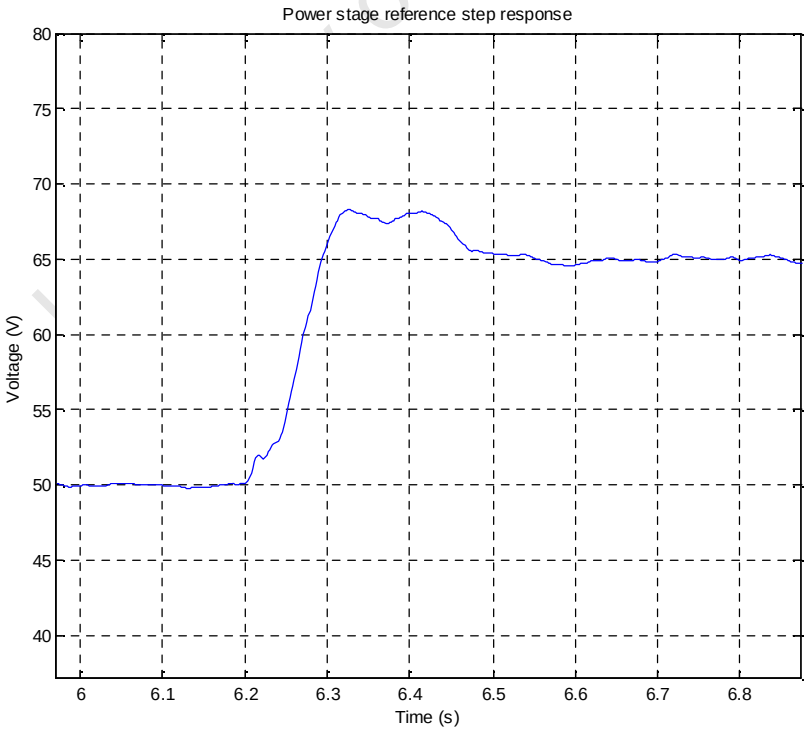

Figure 5.26. DC link voltage overshoot and settling time.

As shown in figure 5.27, there is a change in the grid direct axis voltage as a result of the current change and the grid impedance. The 100Hz component that is superimposed on the DC component is also clearly identifiable. These are produced by the unbalance in the three phase supply and the impedance mismatch on the grid.

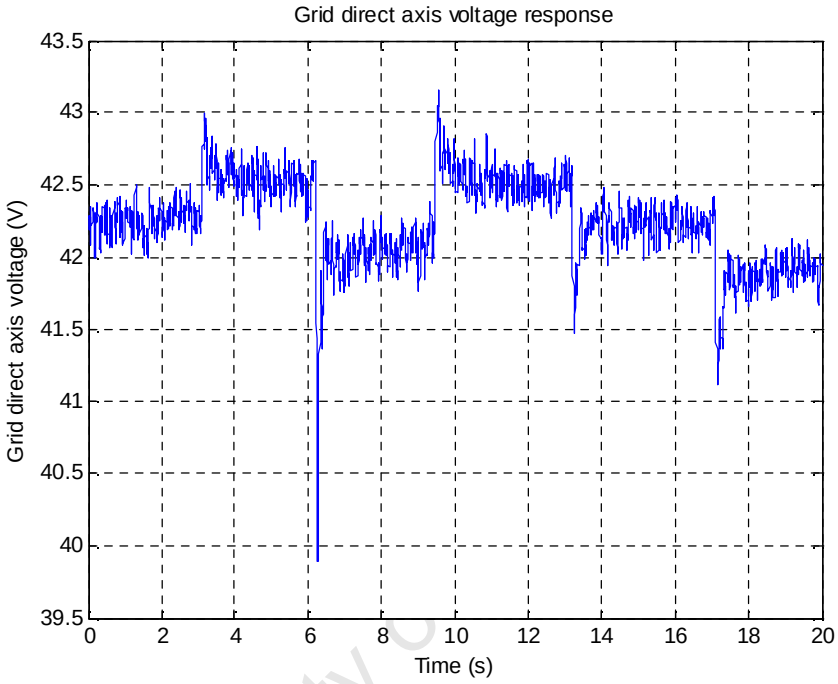

Figure 5.27. Grid direct axis voltage component.

The direct relationship between the DC link voltage and output current results in step changes on the direct axis current component for DC voltage reference step changes.

The response of the direct axis current is shown in figure 5.28. The oscillations on the dc component are also present as a result of unbalanced conditions. Large steps in output voltage and thus load current result in significant current overshoot while stability is maintained.

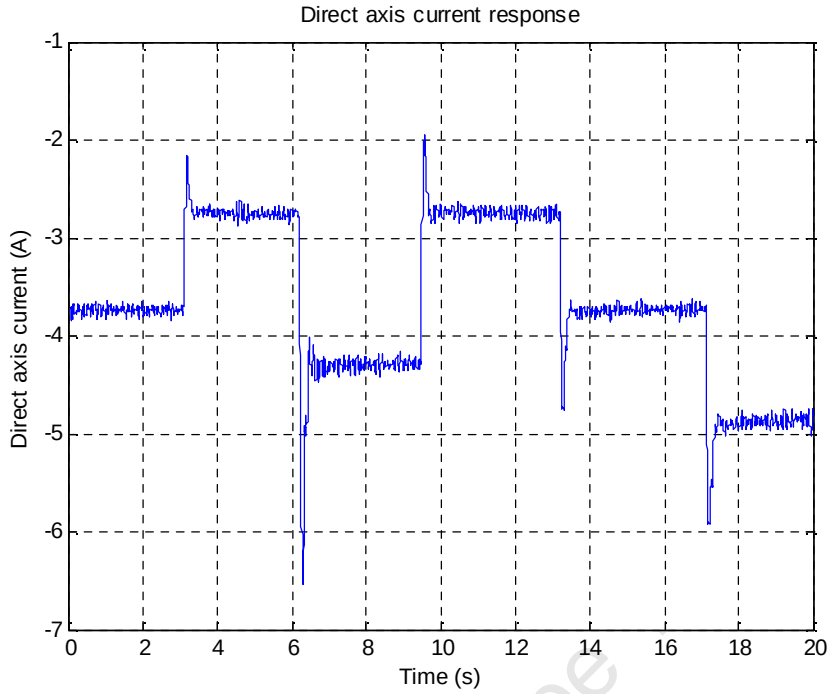

Figure 5.28. Grid direct axis current response.

The quadrature axis current response is shown in figure 5.29. The settling time is slower than that of the direct axis current as a result of the reduced controller gains. By utilizing only two of the three phases for feedback in the control loop, the oscillations due to unbalanced conditions are magnified and present a problem on the q-axis control system. The system stability was compromised for high controller gains.

This effect can be reduced by introducing low pass filters in the feedback path of the controller. An additional time delay has to be incorporated into the closed loop transfer function to accommodate the filter. This option also slows down the response time of the controller but minimises the probability that the system may become unstable during transient states.

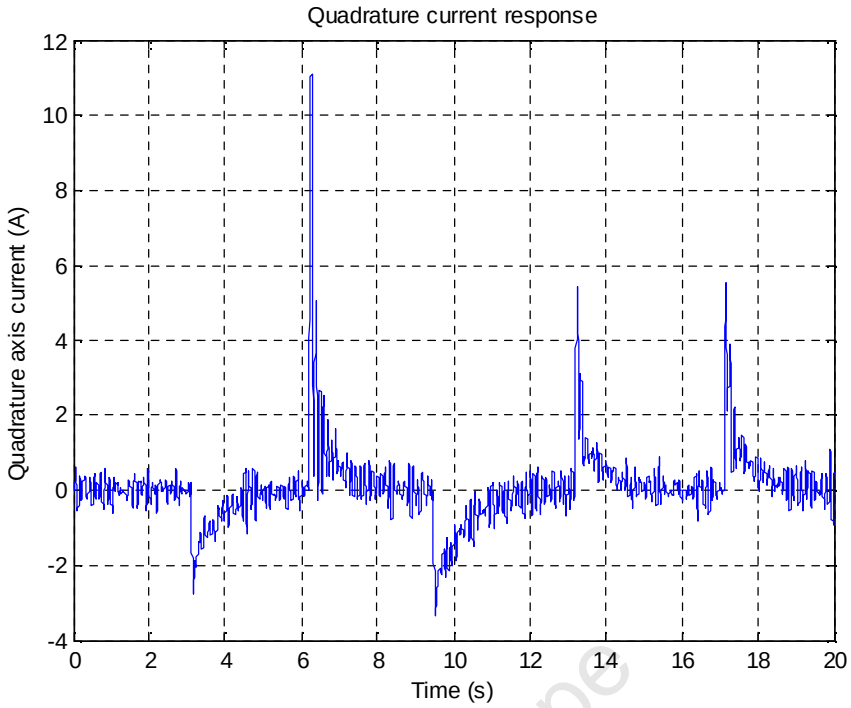

Figure 5.29. Grid quadrature axis current response.

B. Load current step response

The response of the control systems were tested for steps in load current by connecting the DC link to an electronic load and a resistive load in parallel. The electronic load will draw a programmed amount of current from the DC link. The current drawn by the resistive load is dependent on the magnitude of the DC link voltage. A change in voltage magnitude during a current step will increase the transient effect on the current components in order to test the stability of the control system. The DC link voltage during the load changes were recorded in figure 5.30. The voltage overshoot and settling time for a decrease in load current is shown in figure 5.31. As can be seen there is an overshoot of 9% and a settling time of 0.5s.

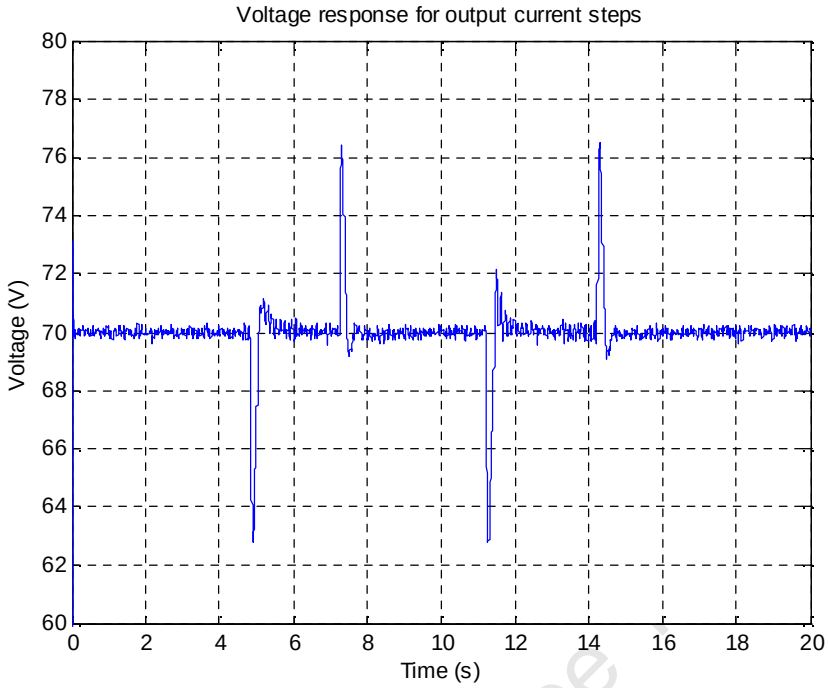

Figure 5.30. DC link voltage response.

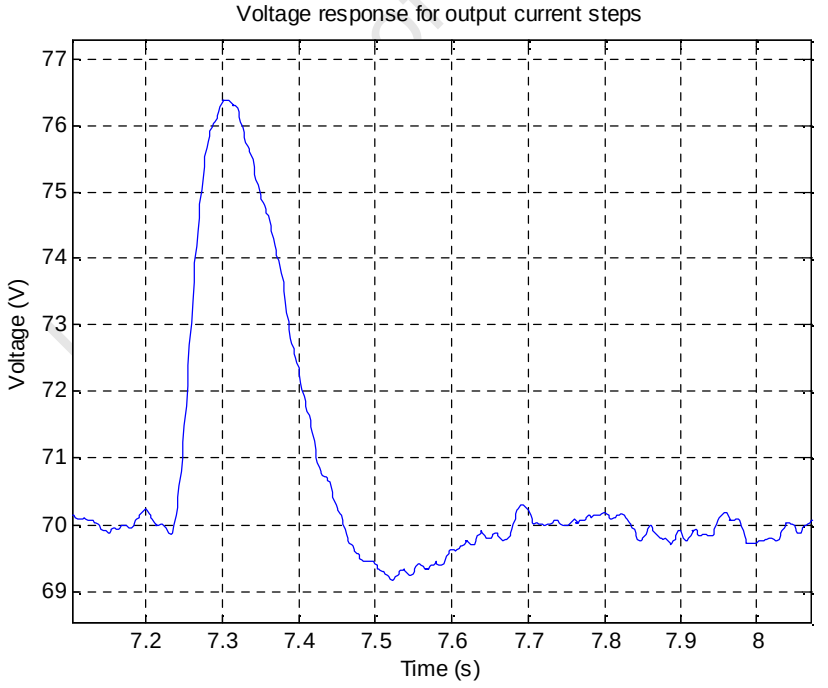

Figure 5.31. DC link voltage overshoot and settling time.

The grid direct axis voltage shown in figure 5.32, illustrates the effect of the grid side impedance on supply voltage magnitude during current transients.

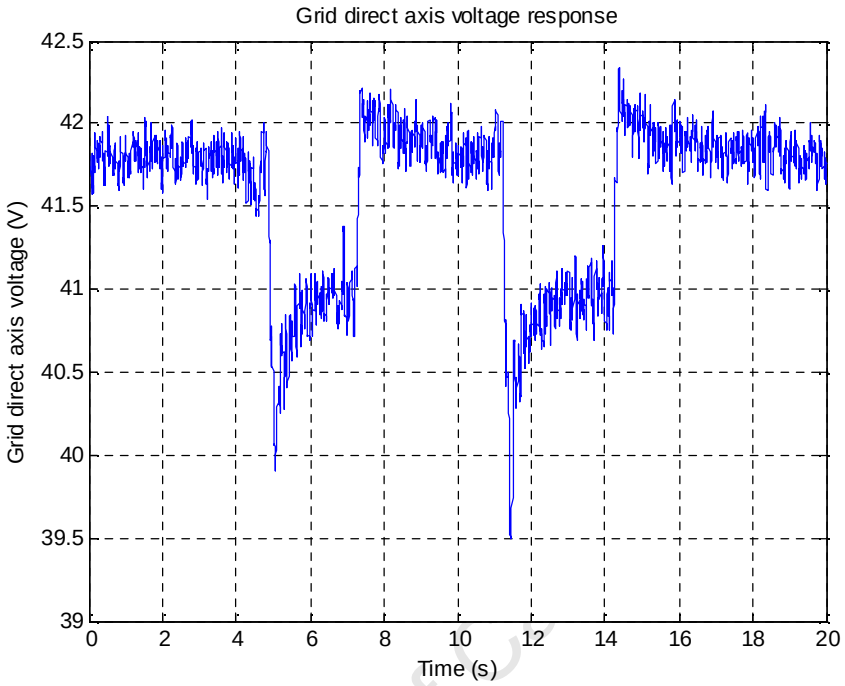

Figure 5.32. Grid direct axis voltage component.

The slow response of the power stage converter will allow the control stage converter to vary the output duty cycle to compensate for the change in DC link voltage while tracking the output voltage reference without becoming unstable. This was confirmed during final system testing.

The current response is shown in figures 5.33 and 5.34. The direct axis current overshoots and undershoots results from the DC link voltage change and the resultant change in current on the connected resistive load.

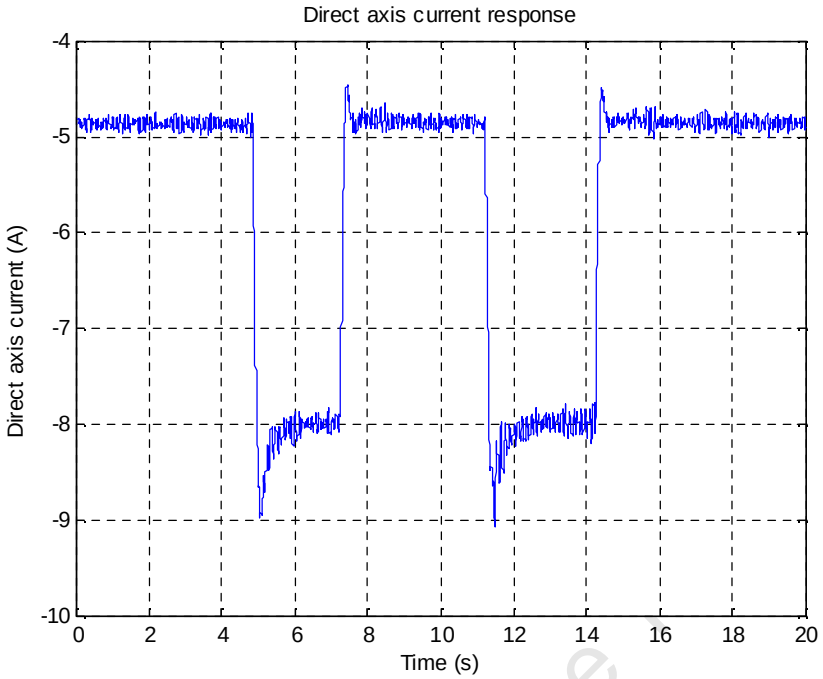

Figure 5.33. Grid direct axis current response.

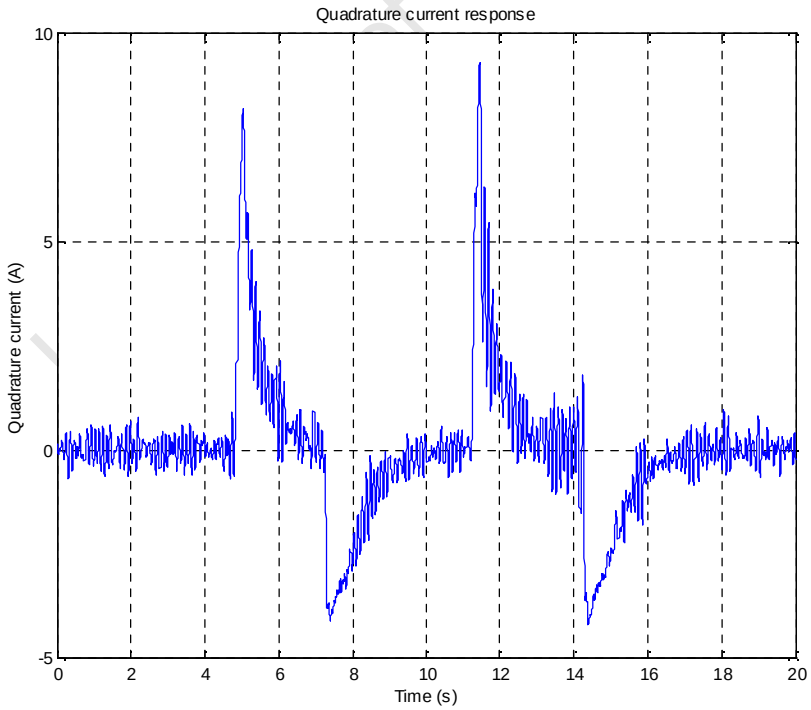

Figure 5.34. Grid quadrature axis current response.

The system is able to maintain the quadrature current at 0 during steady state and slow changes in load and reference. This results in unity displacement power factor operation as can be seen from figure 5.35. Grid side voltage and currents are in phase resulting in only active power being supplied. The unbalanced grid side conditions are also clearly visible in the figure and are the cause of the oscillations propagating on the dq components.

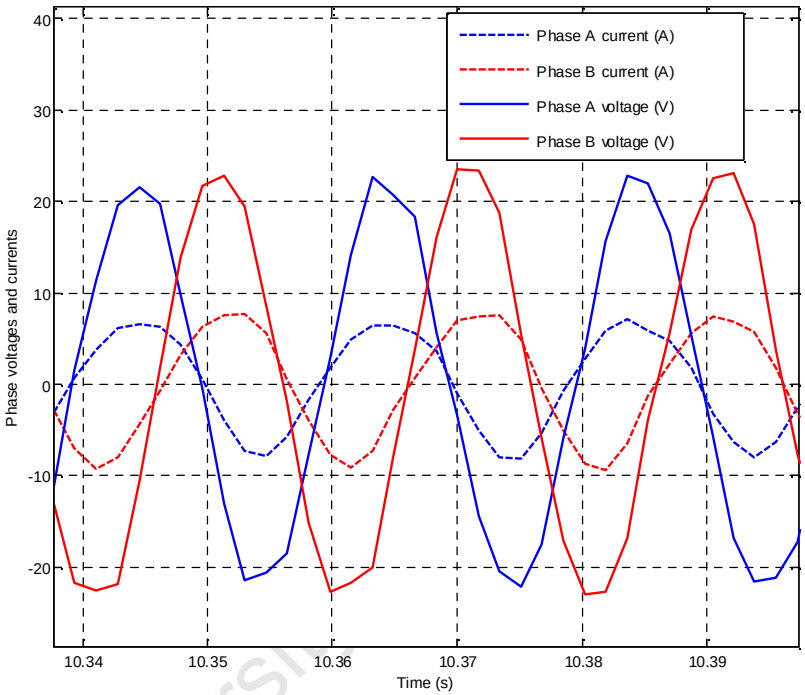

Figure 5.35. Grid voltages and currents.

X. CONCLUSION

From the simulated and experimental responses it can be concluded that the change from single phase to a double phase interleaved system results in an improvement in transient response times. The effective inductance is halved and results in an increase in system bandwidth as shown by the increase in the cut off frequency of the output filter. The same effect on response times was demonstrated for a reduction in capacitor size.

The control system for the control stage was designed to react effectively when integrated with the dSpace hardware. The response time from open loop to closed loop could not be improved due to hardware limitations; the overshoot and steady state error was eliminated to obtain better results when tracking a non linear reference.

The power stage converter control system is based on voltage vector oriented control. The voltage and current loops were derived and designed using the symmetric and modulus optimum methods. The experimental results for both voltage and current step responses are presented and demonstrate good stability under transient states. By maintaining the quadrature current component at a nominal reference of 0, results in unity displacement power factor operation for the system.

6. DESIGN OF THE EMULATOR SYSTEM

I. INTRODUCTION

As discussed in chapter 4, the emulator system consists of two separate converters that are connected back to back in order to meet the system requirements. The control stage converter is based on a multiphase interleaved synchronous buck topology and the power stage is a three phase voltage source converter.

Each of the converters was designed to meet certain performance and operational criteria which will be discussed in this chapter. Filter component sizes plays an important role in the transient as well as steady state characteristics of the outputs and were designed accordingly.

The initial prototypes that were designed and built to test the performance and operational viability of the converters will be mentioned but not discussed in too much detail. The results will be discussed briefly and were used to design the final systems.

To implement the control system for the power stage and control stage converters, a number of transducers are required for the feedback signals. The control platform implemented was the dSpace DS1104 system. The total number of ADC channels that could be utilized was 8 on the connector panel.

For the emulator to work accurately up to the high millivolt range for high current values, the circuit boards implemented had to be designed with the reduction of EMI (electromagnetic interference) in mind. The gate drive circuitry and switching circuits had to be implemented in such a way as to minimize the disturbances on the control signals as well as the feedback to the dSpace system.

This chapter details the designs of the hardware that realized the experimental results for the emulator. Circuit board designs and the reduction of switching noise are shown to have a major effect on system performance. The ripple cancellation effect is demonstrated to be effective in the generation of a clean DC output.

II. CONTROL STAGE CONVERTER DESIGN

The additional phases that are introduced in the interleaved topology, as discussed in chapter 4, reduce the total current that is carried by each phase leg and increases the frequency of the output voltage ripple. This allows for the reduction of filter component sizes during the design process. As the size of the output filter components determine the transient response, as shown in chapter 5, the components should be designed as small as possible to meet the system specifications as outlined in table 6.1

The phase shift interleaved PWM scheme reduces output voltage ripple and distortion with a lower switching frequency [42]. An additional benefit is the output voltage ripple cancelation factor that is introduced. For the double phase system, there is a complete cancelation of ripple at a duty ratio of 50%. This operating point will thus be used as the nominal design parameter.

Table 6.1: Control stage converter specifications

Parameter	Specification
Maximum input voltage	70V
Rated output voltage	50V
Nominal output voltage	35V
Maximum output current	$30A$
Rated power	$1500W$
Switching frequency	25kHz/phase
Output voltage ripple	1% of V_o nom
Inductor current ripple	10% of maximum phase current

A. Inductor design

To achieve the specifications as set out in table 6.1, the average operating conditions will be considered. The voltage across the inductor is given as follows:

$$V_L = L\frac{di_L}{dt} \tag{6.1}$$

The minimum inductance required to maintain continuous conduction mode up to 15A is derived as follows:

$$L_{min} = \frac{V_o(1-D)}{2f_{sw}I_{oB}} = 23.33\mu H \tag{6.2}$$

The inductance required to maintain a minimum peak to peak ripple current of 1.5A is as follows:

$$L = \frac{(V_{dc} - V_o)D}{\Delta i_L f_{sw}} = 466.67\mu H \tag{6.3}$$

The concept of critical inductance is explained in [45]. During transient state the duty cycle is varied to compensate for the change in output voltage. The change in duty cycle is as follows:

$$\Delta D_{max} = D_{max} - D \tag{6.4}$$

where D_{max} represents the maximum duty cycle of the system. If this value is exceeded, the circuit is considered saturated [45].

Inductor current slew rate can be defined as follows:

$$\frac{di}{dt} = \frac{V_{dc}\Delta D_{max}}{L} \tag{6.5}$$

To ensure the system does not become saturated during transient state, there exists a maximum critical inductance value. For an increase in inductor size, the current slew rate will increase and there will be an increase in transient voltage spikes. The interleaved system produces a ripple cancellation effect. This allows for the use of smaller inductance values to increase transient performance without compromising the steady state ripple requirements of the system. Figure 6.1

demonstrates the effect of increased inductor size on voltage transients for the system developed in [45].

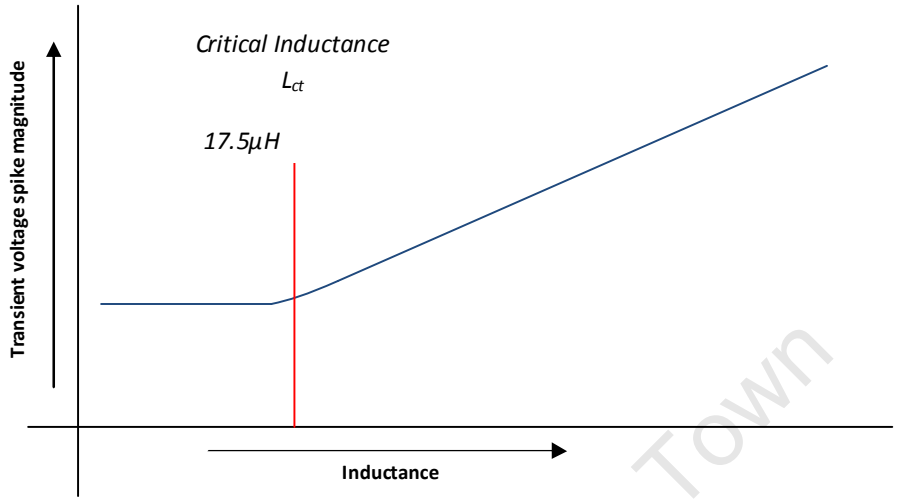

Figure 6.1. Transient voltage spikes vs. inductance for the system demonstrated in [45].

The value for the critical inductance is calculated as follows:

$$L_{ct} = \frac{(\pi/2)V_{dc}}{\Delta I_o \omega_{cs}} \Delta D_{max} \tag{6.6}$$

where ω_{cs} represents the control system bandwidth.

The peak to peak output current that flows into the capacitor is calculated as follows:

$$\Delta I_o = \frac{V_o}{L_n f_{sw}} \left[1 - \frac{m}{ND}\right] [1 + m - ND] \tag{6.7}$$

where N is the number of phases and m=floor(N.D) and returns the greatest integer value less than or equal to the argument. From this relationship it is evident that there is a cancellation effect on the output ripple current at the critical duty ratio of 50% for the double phase system.

For an N-channel interleaving buck, ΔI_o at the critical duty ratio can be defined as 1/N of the total load step current magnitude during transient state [45]. For a maximum load step of 20A, ΔI_o is equal to 10A for the double phase system.

If the control bandwidth is set at twice the switching frequency, the critical inductance was calculated to be 17.5µH.

The final inductor size was chosen as 250µH. This is a larger value than the calculated critical inductance. This inductor size will ensure that the system delivers acceptable transient performance while maintaining the ripple current in each inductor closer to the design parameter than that of the critical inductance value. The reduction of inductor size up to the critical inductance value will always improve transient performance.

The N27 ferrite core material was chosen for the inductor core as it gives good performance for frequencies up to 100kHz. The core-specific constants according to the manufacturer are given as follows:

K1=716, K2=-0.762, K3=1213 and K4=-0.847.

The saturation current of the core is calculated as follows:

$$I_{dc} = \left(\frac{0.9A_L}{K_3}\right)^{\frac{1}{K_4}} \tag{6.8}$$

Where A_L represents the normalized inductance in nH/turn^2 and Idc is the saturation current of the core.

The required airgap value is calculated as follows:

$$s = \left(\frac{A_L}{K_1}\right)^{\frac{1}{K_2}} \tag{6.9}$$

The number of turns is calculated as follows:

$$n = \sqrt{\frac{L}{A_L}}$$

(6.10)

The limits imposed on the above relationships by the manufacturer are as follows:

$$0.2mm \leq s \leq 5mm$$

$$200 \leq A_L \leq 2290$$

By setting the airgap value to the maximum of 5mm to obtain maximum saturation current, the following values were calculated for the manufactured inductors:

Saturation current I_{dc} = 8.977A with a practical inductance of 257.2µH. The total number of turns was 35 with a wire size of 1.5mm^2.

B. Output capacitor design

Using the implemented inductance of 250µH per phase, the minimum value for the output capacitor was calculated as follows:

$$C_o = \frac{(1-D)}{8L_{eq}{f_o}^2}\left(\frac{V_{out}}{\Delta V_{out}}\right) = 20\mu F$$

(6.11)

where L_{eq} represents the equivalent inductance of 125µH. Note that the output voltage ripple frequency is twice the switching frequency due to the interleaving effect, which reduces the filter requirements.

The relationship between the transient voltage drops and filter components is described as follows:

$$\Delta v_o = \frac{(\Delta I_o)^2 L_n}{2V_{dc}\Delta D_{max}C_o}$$

(6.12)

For a maximum transient voltage drop of 5V, the output capacitor value was calculated to be 35.7µF. As the control stage converter will normally run at a critical duty cycle of 50%, resulting in complete ripple cancellation, the final value for capacitance was chosen as 10µF. The increase in output voltage ripple for the short duration of the transients was deemed acceptable.

The filter capacitor was chosen as small as possible to reduce the cut-off frequency of the LC filter. This increases the bandwidth of the hardware enabling the system to react to transients at a faster rate as discussed in chapter 5.

C. Mosfet selection

As the semiconductor devices available on the market become more advanced, the selection process during design becomes more complex. Figure 6.2 gives a basic selection chart between an IGBT or MOSFET as the primary switching device. As can be seen, at lower voltages and higher switching frequencies, the MOSFET is the recommended device.

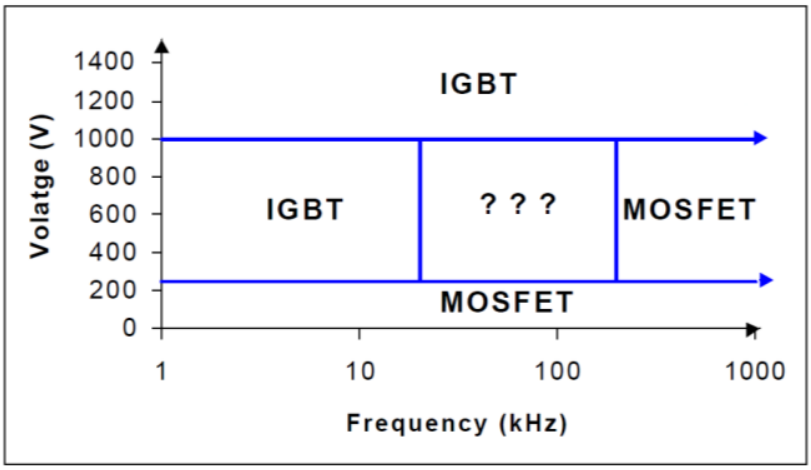

Figure 6.2. IGBT and MOSFET operating areas [51].

Since the converter will run at a nominal duty cycle of 50%, both the top and bottom switches will have the same amount of switching and conduction losses. To reduce the dynamic losses, the gate charge value of the switch should be kept to a minimum. The conduction losses of the switches can be reduced by selecting a switch with a low $R_{ds\ on}$ value.

As shown in figure 6.3, the minimum gate to source voltage required for the MOSFET to switch on and start conducting is referred to as the threshold voltage. A higher gate to source voltage

will reduce the conduction resistance of the MOSFET and will increase the total gate charge. For a higher gate charge, the switching losses will increase. A balance must thus be struck between the desired conduction and switching losses required for optimal operation to reduce losses and increase system efficiency.

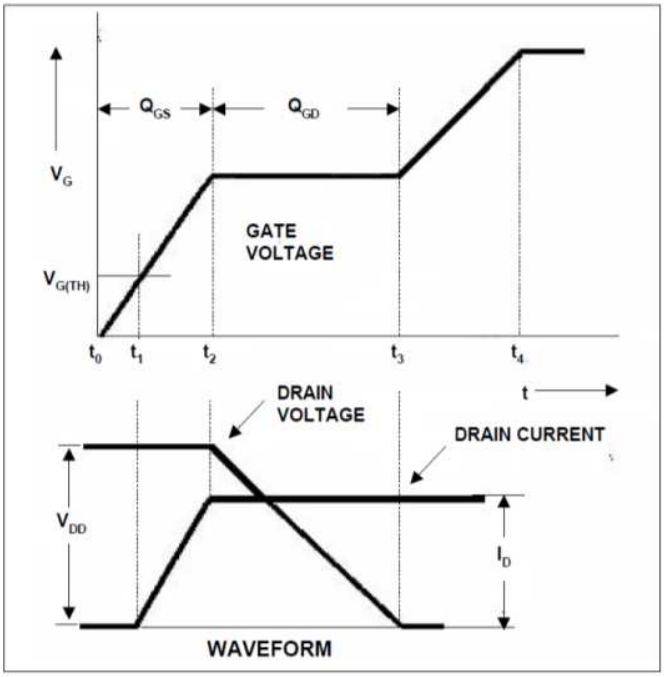

Figure 6.3. Basic gate charge waveforms [52].

The selected switch for the synchronous multiphase system was the IRF 3710 N channel MOSFET from International Rectifier. This switch has an on resistance of 23mΩ and a gate charge value of 130nC. The rated voltage is 100V and the rated current is 57A. The operating range for this switch is dictated by the device temperature and losses as shown in figure 6.4.

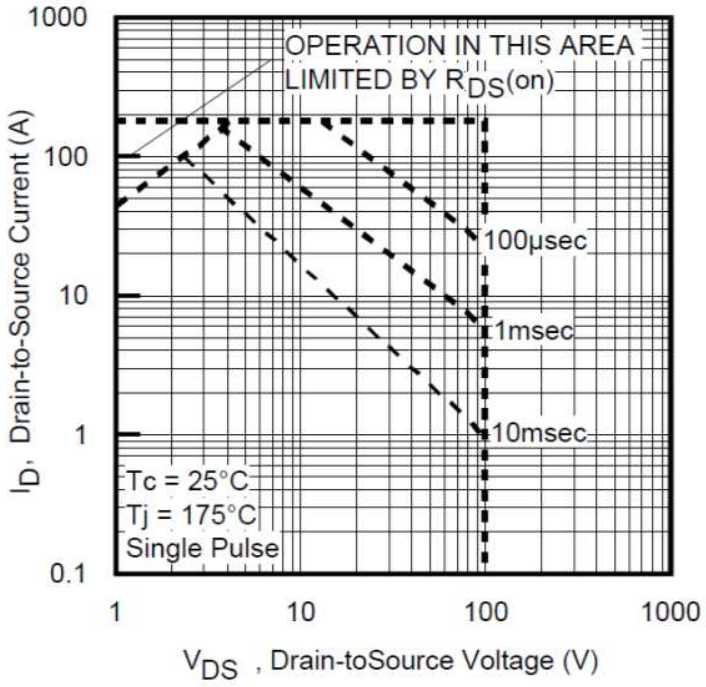

Figure 6.4. Safe operating area of the IRF3710 [52].

D. Phase shift interleaved PWM

The interleaved synchronous buck requires a separate gate drive signal for each individual switch as shown in figure 6.5. To accomplish the desired effect regarding ripple cancellation, the gate drive signal of each phase must be shifted by 360°/N in the phase spectrum. To achieve this, the control hardware must generate separate carrier waveforms that are delayed from each other as shown in figure 6.6.

For the double phase system, two carrier waveforms were generated each running at 25kHz. The second carrier waveform is delayed by exactly 20µs. The modulation index running on the carrier waveforms for each of the phases were identical as this simplifies the control strategy. The PWM patterns generated for each switch is shown in figure 6.6. These signals are at TTL levels and were sent to the control card of the Control Stage converter.

To ensure that the phases do not create a direct connection between the positive and negative input terminals, the gate drive hardware must incorporate shoot-through protection as well as sufficient dead time generation for each switch pair.

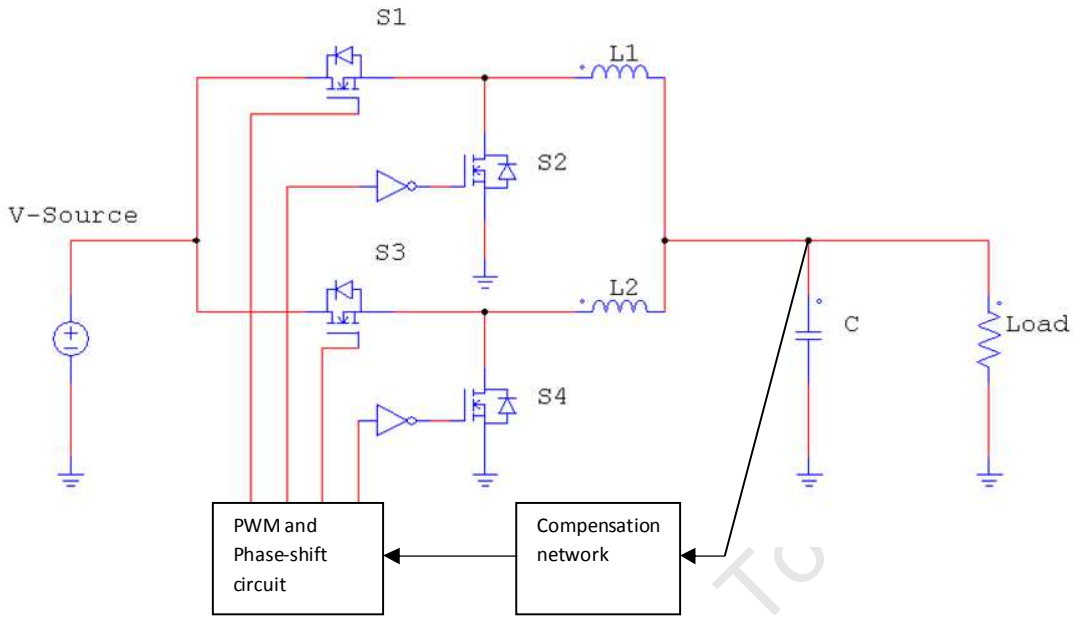

Figure 6.5. Connection of the gating signals to the double phase system.

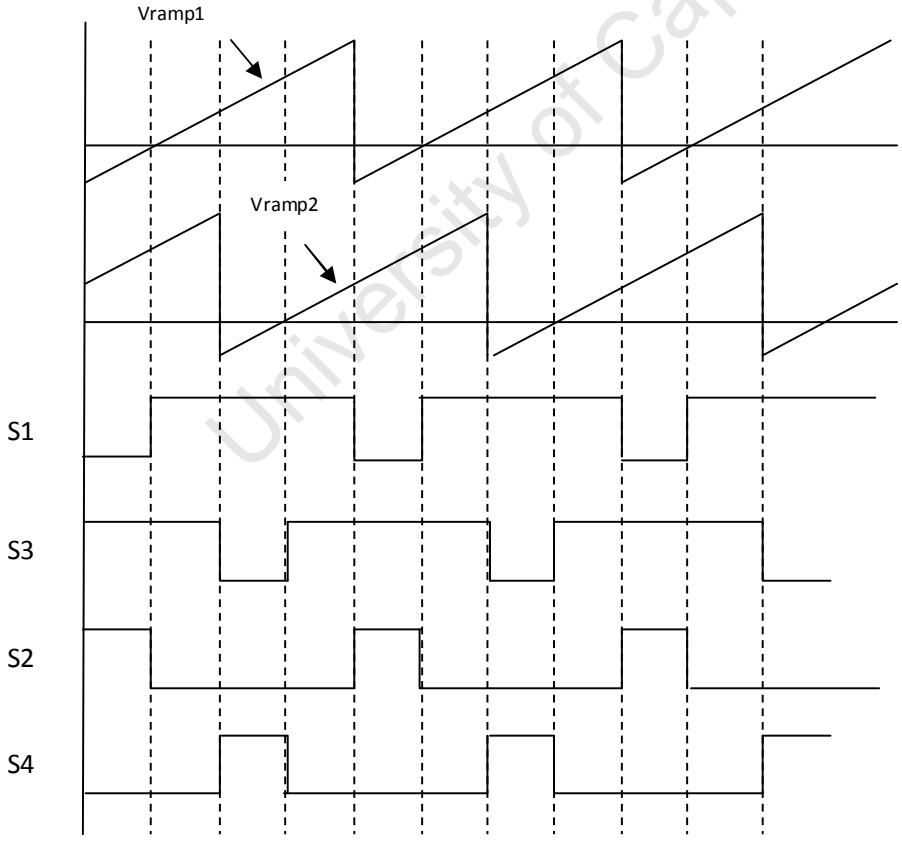

Figure 6.6. Carrier waveforms and generated gate signals.

III. POWER STAGE CONVERTER DESIGN

The design of the power stage was based on a standard voltage source converter. There exists a minimum DC link voltage for the system to operate properly. If the DC link voltage is dropped below the minimum value, the body diodes of the rectifier will start to conduct and the system will try to behave as a normal rectifier. The maximum DC voltage of the system is limited by the input current. To negate the rectifier effect, the body diode must be disabled by placing another diode in series with the switch or the rectifier input voltage must be kept below a certain value. The former introduces more active devices in the hardware and increases system complexity.

Buck type active rectifiers, also known as current source rectifiers, allow the DC voltage to drop below the minimum rectified voltage. The control design of these systems is more complex due to the higher system order of the filters that have to be employed on the AC and DC side. Other topology modifications have also been done to achieve this type of operation [53], [54].

To simplify the design of the hardware and the control, the voltage source converter was used and the supply voltage was dropped accordingly by using a variable transformer. The specifications of the system are detailed in table 6.2.

Table 6.2: Power stage converter specifications

Parameter	Specification
Maximum input voltage	$30V_{LL\,rms}$
Rated output voltage	100V
Nominal output voltage	70V
Maximum output current	$20A$
Rated power	$1400W$
Switching frequency	5kHz

A. Design of the DC link capacitor

The minimum DC link voltage that the converter will deliver can be calculated as follows:

$$V_{dc\,min} = V_{LL\,(rms)} \times \sqrt{2} = 42.5V \tag{6.13}$$

The minimum voltage at the output of the control stage, according to the polarization curves of chapter 3, will be 25V. Thus, the minimum required DC link voltage to maintain a duty cycle of 50% on the control stage at high current densities is set as 50V, higher than the required system minimum. The filter capacitor was selected based on availability and ripple magnitude estimation via simulation. The final value was chosen as 4700µF.

B. Input filter selection

The design of the input inductance should be done carefully as a low inductance will result in a high current ripple making the system more dependent on the line impedance [55]. If the inductance chosen is too large, the operating range of the system will be limited. At high current ratings, the DC link voltage must be high or the inductance made small to ensure throughput power capability. The maximum inductance is determined as follows [55]:

$$L_{max} = \frac{\sqrt{\frac{{u_{dc}}^2}{3} - {E_m}^2}}{\omega i_{Ld}} = 2.43mH \tag{6.14}$$

where E_m represents the peak line to neutral voltage, u_{dc} the minimum DC link voltage of 50V, ω the grid angular frequency and i_{Ld} the direct axis component of the grid side current (chosen as 20A).

The final inductor sizes were chosen as 2.2mH due to availability.

C. Mosfet selection

The selection procedure of the switches is the same as for the control stage converter as detailed in section II of this chapter. To comply with the system requirements as set out in table 6.2, the IRFB 4321 was chosen. This switch has a drain to source voltage rating of 150V and a current rating of 70A.

IV. CIRCUIT LAYOUT

Figure 6.7 shows the basic layout of a half bridge leg connected to the gate driver. It is evident from the figure that the tracks of the circuit board will have a finite amount of parasitic inductance. During switching transients, there will be a sudden change in current. The inductance present will cause very sharp voltage spikes during these changes in current and increase the generation of noise present on the outputs.

The general rule is to keep the loops between the switches and the drivers as short and as thick as possible to minimise this effect.

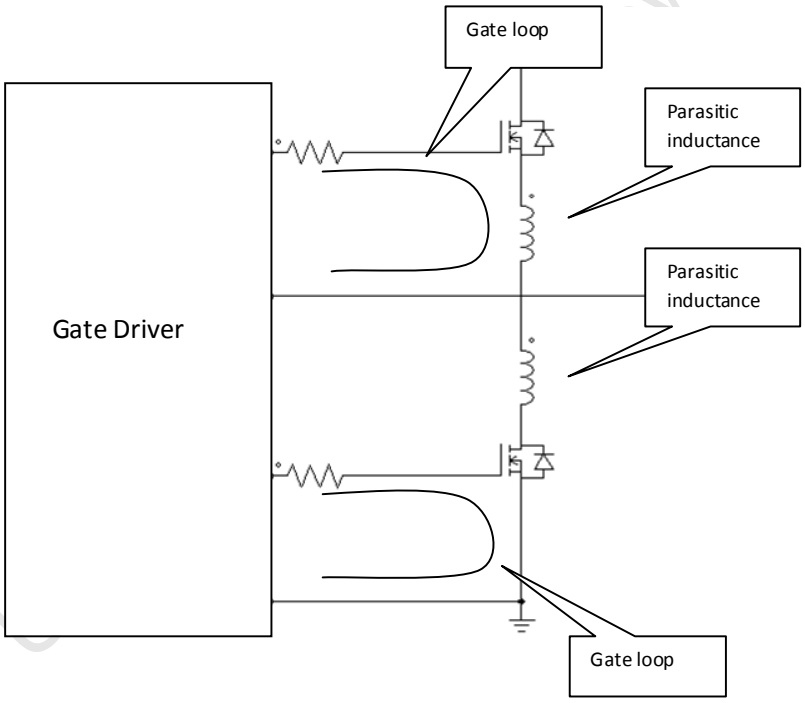

Figure 6.7. MOSFET half bridge leg.

The proper placement of ground planes will minimise the noise pickup of the control signals and maintain the integrity of the control. The final layout of the circuit boards used for the power and control stage converters are detailed in Appendix 4.

A. Snubber design

Snubber circuits are used to reduce the electrical stresses of the switching devices during turn on and turn off. These circuits are able to shape the switch trajectory as well as clamp voltages that appear across the devices.

Figure 6.8 shows the blocking voltage across one of the MOSFETs used in the initial prototype of the system. There is a large overvoltage spike as well as a ringing effect. Both of these had a detrimental effect on the quality of the output voltage waveform, compromising the performance of the emulator system. The large overvoltage spike increased in magnitude as the switched current increased, causing failure in the switches as soon as the maximum device rating was exceeded.

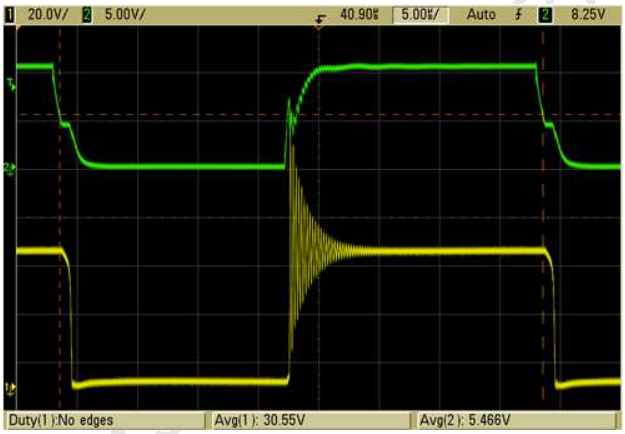

Figure 6.8. MOSFET blocking (Ch1) and gating voltages (Ch2).

In order to eliminate the ringing effect caused by the stray inductances on the circuit, an RC circuit was added across each switch to shape the turn off trajectory. The resultant blocking waveform is shown in figure 6.9. To clamp the overvoltage an additional RC snubber was added across the half bridge pairs. The final experimental result for the snubber circuits are shown in the second set of waveforms in figure 6.9.

Figure 6.9. MOSFET blocking (Ch1) and DC output voltages (Ch2).

The addition of a diode can reduce the amount of power dissipated in the snubber circuits at the cost of an increase in overvoltage magnitude. Since the primary goal of the emulator is the output DC voltage quality, the increase in losses was deemed acceptable. Active damping circuits include the addition of more switching devices, which increases the complexity of the whole system including the driver and control circuitry. Therefore this was not attempted during implementation.

B. Gate driver design

The gate driver circuit is one of the most important parts of the system as it functions as the interface between the control system and the high power circuitry. This circuit should effectively isolate the primary control signal side of the system from hard switched high current devices. If during operation, device failure should occur on the power side, this must not propagate over to the control hardware and risk damaging it as it is expensive and difficult to replace.

To accommodate these requirements, the use of optical isolation is the common practice. A 6N137 optocoupler was used as the primary connection point between the control signals and the driver circuitry. This specific device accommodates TTL signal levels and provides a peak overvoltage isolation of 3kV. It has a high bandwidth as well as very good common mode noise shield between the primary and secondary sides to maintain control signal integrity as shown in figure 6.10.

The gate driver used had to be able to drive a halfbridge configuration as shown in figure 6.7. The gate voltage of the High side MOSFET must be bootstrapped onto the source as this is not

constant during converter operation. The chosen device was the IRF 21804 driver. This circuit has an integrated under-voltage lockout and shoot through protection. The dead time generated between the gate signals of the high and low side is set by adjusting an external resistance value. The device automatically inverts the low side control signal and enables the use of a single control line from the control system for each half bridge pair.

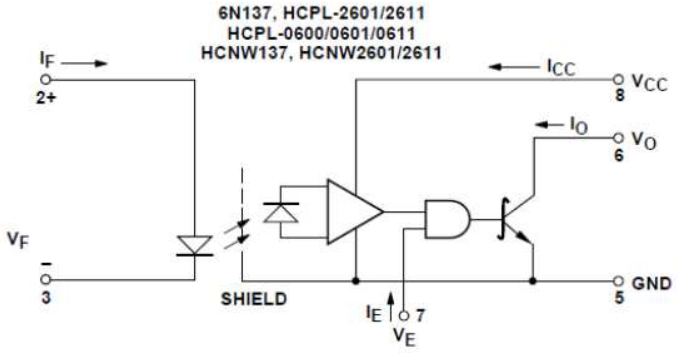

Figure 6.10. 6N137 device schematic [56].

The effect of dead time on system performance was evaluated in [57]. To achieve optimal system performance, this value must be set as low as possible while ensuring that the devices have enough time to turn off before the alternate one in the bridge pair turns on. A general timing diagram is depicted in figure 6.11

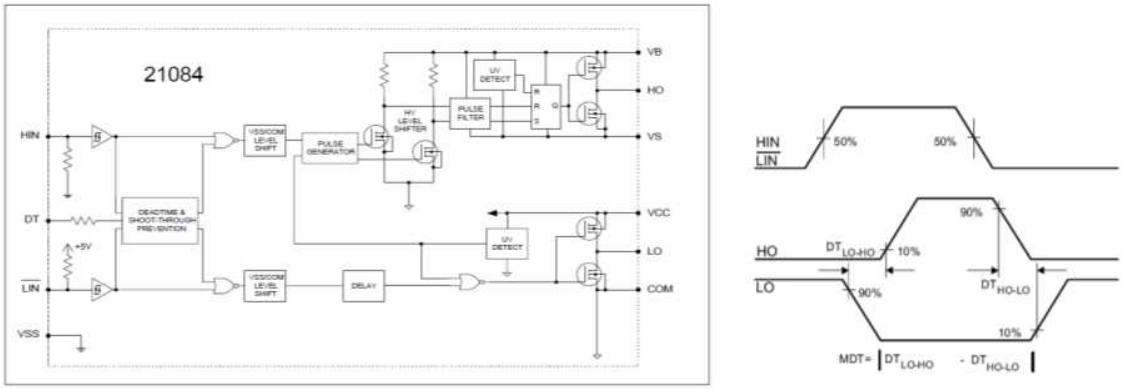

Figure 6.11. Driver schematic and switch timing diagram [58].

The design of the driver interface card is attached in Appendix 4.

C. Transducer selection

The transducers required to realize the control systems as discussed in the previous chapters are as follows:

- 2 Current transducers to monitor grid side line currents; range: 0 – 30A
- 2 Voltage transducers to monitor grid side voltages; range: 0 – 150V
- 1 Voltage transducer to monitor the DC link; range: 0 – 150V
- 1 Current transducer to monitor emulator load current; range: 0 – 30A
- 1 Voltage transducer to monitor emulator output voltage; range: 0 – 80V

The monitored number of phase currents and voltages was reduced to two due to the availability of ADC channels on the dSpace system.

To maintain feedback signal integrity, the transducers must have very good linearity, high bandwidth, good common mode and external noise rejection ratios as well as high overvoltage isolation levels. The LEM LV25P and LA25P are commonly used and provide good performance. A circuit board housing three voltage and current transducers was designed to increase the noise immunity and disturbance rejection of the transducers. The final design is attached in Appendix 3.

V. PROTOTYPE SYSTEM

The initial system developed to test the operating principle and performance of the single and double phase buck converter is shown in figure 6.12. As discussed in chapter 5, this design was based on a standard buck topology with a Schottky diode implemented in each phase. The MOSFET was moved to the low side, simplifying the initial driver circuit development. It should be noted that this design implemented a Texas Instruments TPS2812 low side driver. The transient responses of the prototypes were discussed in chapter 5. Further discussion on the design of the prototype will thus not be done. The circuit diagrams and board layouts can be found in Appendix 4. The generated gate signals of the prototype driver are shown in figure 6.13.

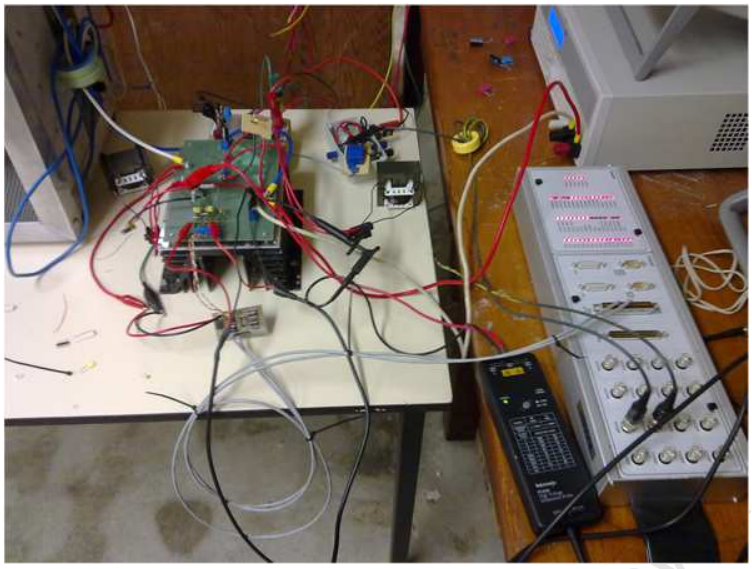

Figure 6.12. Prototype system during testing.

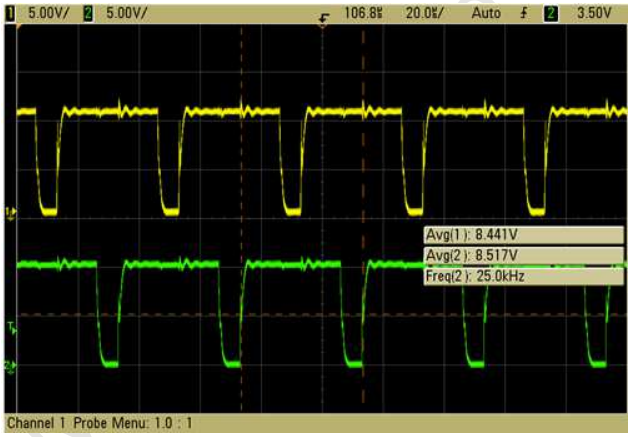

Figure 6.13. Prototype gate drive signals.

The steady state output of the double phase prototype is shown in figure 6.14. At 50% duty ratio there is a complete ripple cancellation effect. At higher duty ratios, the voltage ripple becomes evident. The transient spikes from the switching of the MOSFETs are still evident on the output voltage waveforms.

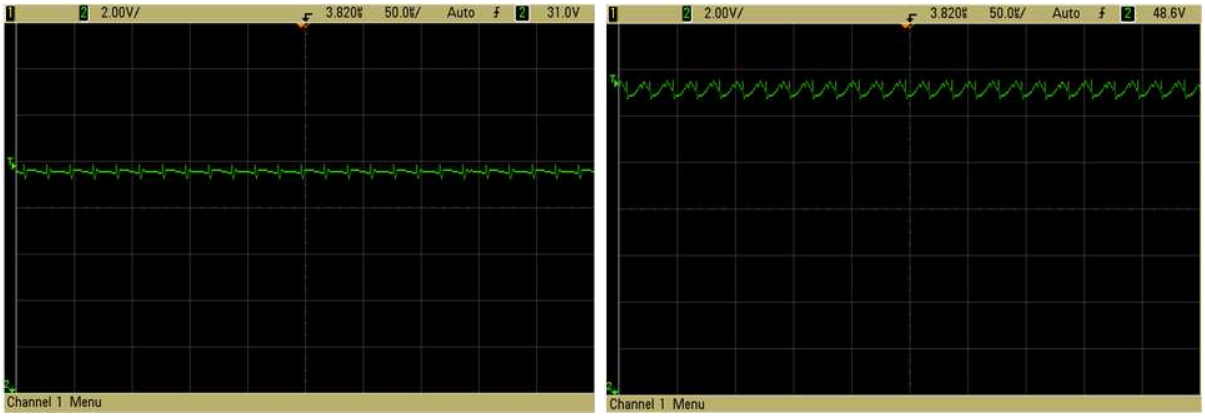

Figure 6.14. Output voltages at 50% and 80% duty ratios for the double phase prototype.

VI. FINAL SYSTEM

The assembled emulator system is shown in figure 6.15. Figures detailing the assembly of the power and control stage converters are attached in Appendix 3. Shielded twisted pair cable was used as far as possible for the control and feedback signals to limit noise pickup from the main power cables. The large switched currents propagating through the lines caused a large amount of EMI on the dSpace connector panel. This problem was minimised by connecting the mains earth directly to the dSpace connector as well as the ground planes of the transducer cards.

Circuit breakers were placed at the terminals of the three phase rectifier input and on the DC link. To protect the power electronic circuits, fast blow fuses were placed after the three phase circuit breaker on the input lines to the power stage converter.

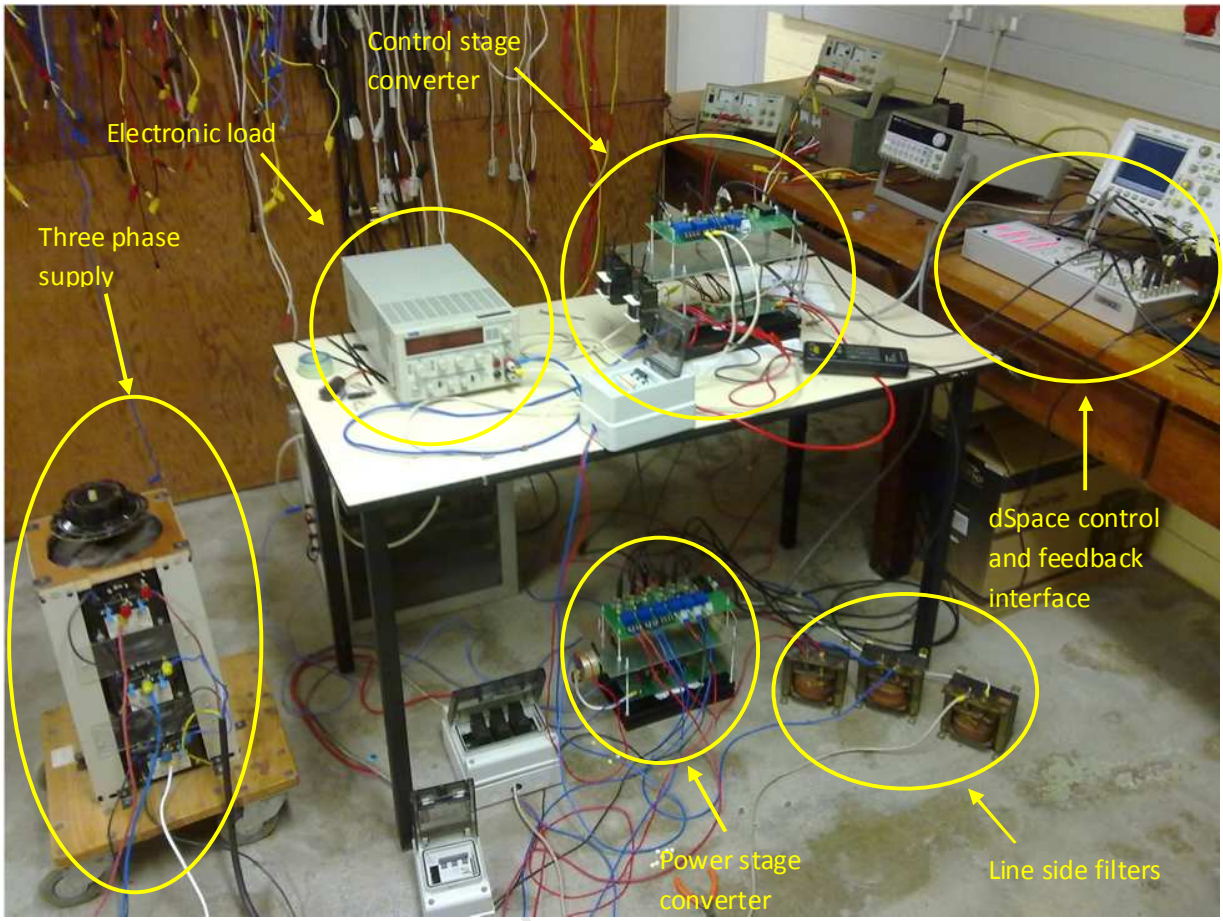

Figure 6.15. Final system during testing.

The performance of the system will be discussed in the following chapter.

VII. CONCLUSION

This chapter presented the design of the filter components for the control stage and power stage converter required to meet the system specifications. The ripple cancellation factor of the multiphase system was used to reduce the filter component sizes in order to increase transient response capability. The critical inductance value for the control stage converter was calculated and used to determine a final design value that will deliver optimal performance.

The component selection was done to realize the operating parameters of the system and incorporates the required safety factors for safe operation up to the maximum ratings. The circuit layout and PCB design was done in accordance with standard practice utilized in the industry.

The experimental prototype of the control stage was presented and verifies the ripple cancellation capability of the topology. The prototype board layout showed significant switching noise propagating on the output voltage as a result of the parasitic inductances. The final system was designed to eliminate EMI as far as possible to increase the quality of the emulator output. The required safety mechanisms were appropriately placed to ensure safe operation during testing.

7. EXPERIMENTAL RESULTS AND DISCUSSION

I. INTRODUCTION

This section details the experimental results obtained during laboratory testing of the final system. The outputs of the model, experimental stack and emulator are compared for the tests done. The dynamic phenomena that was emulated, however could not be replicated on the experimental fuel cell stack, is instead compared to results available in literature.

II. POLARIZATION CURVES

A. Operating under standard conditions

The polarization curves were obtained by increasing the output current on the electronic load from 0.2A to 30A. Figure 7.1 represents the polarization curves of the model, emulator and the tested 1kW HT PEM FC stack. It is evident that there is very good correlation between the model and the emulator response. The difference between the captured stack output and the emulator is due to the assumptions made in the lumped parameter model as explained in chapter 3. The load current was not reduced below 200mA to avoid operating the control stage converter in discontinuous current conduction mode.

The error between the model and the emulator output can be attributed to the current slew rate. A faster slew rate will increase the average temperature in the thermal model, resulting in a higher output voltage in the linear ohmic region.

The operation of the control stage converter at 50% resulted in a complete ripple cancellation effect during steady state operation due to the phase shifted interleaving principle. The polarization curves obtained detail the quality of the DC output despite the small size of the filter components. The system achieved unity power factor while these tests were performed, increasing its efficiency.

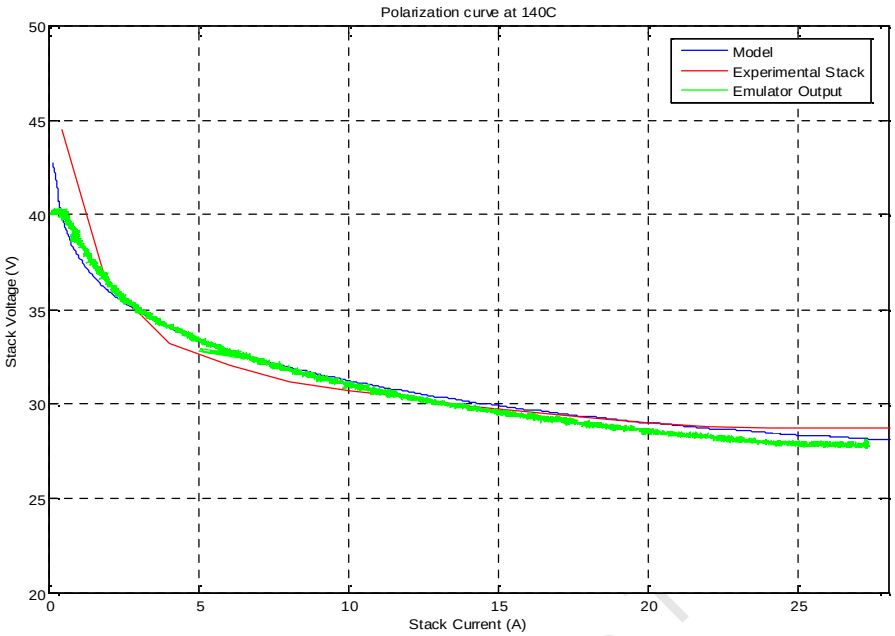

Figure 7.1. Polarization curves at 140°C.

B. Emulation of the hysteresis effect

The hysteresis effect was emulated by increasing the current density of the system from 0.002A/cm^2 up to 0.3A/cm^2 and then reducing it back to 0.002A/cm^2. The test was done for two thermal capacitance values to demonstrate the effect of the thermal model on the output of the system. As shown in figure 7.2, the emulator demonstrated the capability to reproduce the hysteresis phenomenon which is discussed chapter 3, section VI E. Increasing the thermal capacitance resulted in a wider hysteresis band being formed.

The exact temperature response of the experimental stack was not recorded during initial testing and could thus not be compared to the emulator temperature prediction. A further increase in thermal capacitance would result in a reduced error between the emulated output and the stack data.

The output of the power stage converter is shown in figure 7.3. The system will operate at the safety limit of 70V until the current density is increased to a value that generates a lower set point in the control system. The power stage accurately replicates the polarization curves at twice the emulator output voltage, maintaining the control stage converter duty ratio at 50% at high current densities.

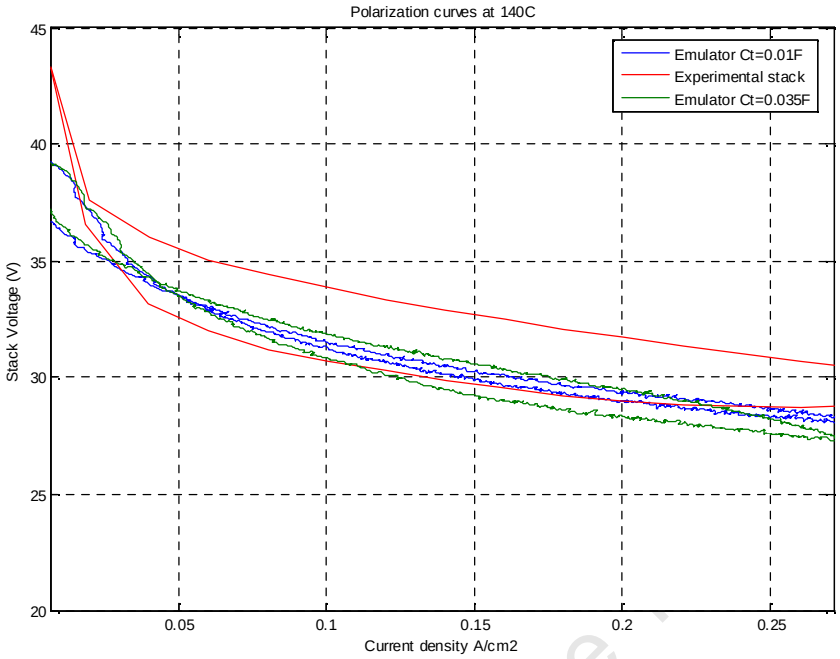

Figure 7.2. Polarization curve hysteresis at 140°C.

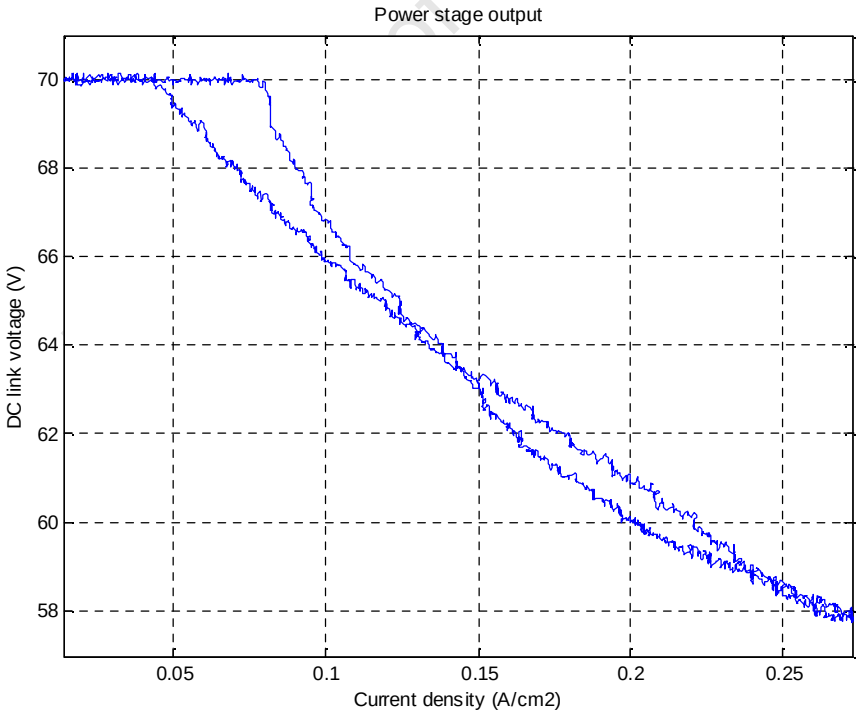

Figure 7.3. Power stage output during polarization curve testing.

III. TRANSIENT RESPONSE

A. Emulation of long time range step response

The response of the fuel cell system is mainly dependant on the stack temperature response and the reactant flow delays. During experimental testing of the fuel cell stack, the current slew rate was slowed to 0.6 A/s to ensure that the reactant controllers can keep up with the load demand. The load step conducted on the emulator system during testing was made more aggressive to demonstrate system performance. As shown in figure 7.4, the emulator demonstrated a faster initial voltage drop and a slower recovery rate to the new steady state value when compared to the stack and model voltage response.

The switching noise of 200mV peak to peak is evident on the captured emulator waveform. Despite this effect, the quality of the output waveform is not compromised.

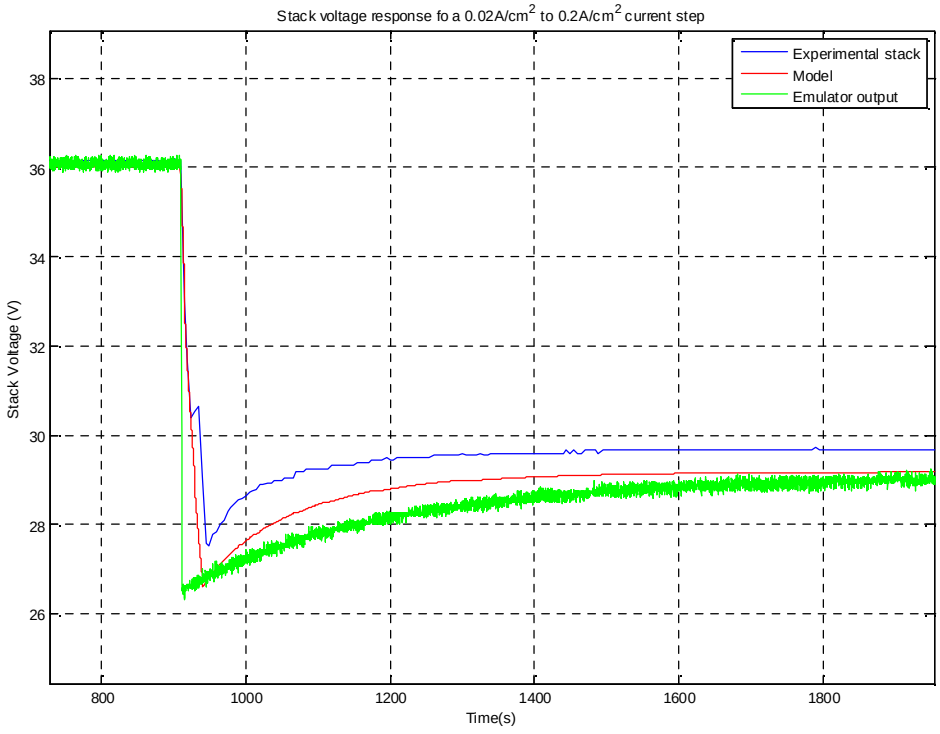

Figure 7.4. Comparison of voltage responses for a 0.02A/cm^2 to 0.2A/cm^2 step.

The control stage is operating at a duty cycle of 50% during steady state and deviates only during transient state until the power stage output has reached the new steady state operating point. It is evident that there is negligible voltage ripple on the output with only the switching noise propagating on the recorded voltage waveform. Even during the transient state, the control stage does not deviate too much from the critical duty ratio for more than 5 seconds. This results in a good ripple cancellation effect as discussed in chapter 4.

The voltage recovery of the system is mainly dependant on the temperature response of the stack. Figure 7.5 depicts the current step and the corresponding temperature prediction from the emulator as calculated in real time. Before the current step is applied (920s), the coolant system is still slowly achieving a final steady state value. This does not affect the system voltage as can be seen from the corresponding waveforms. As the current step is applied, the temperature of the stack will slowly start to rise as the rate of the exothermic chemical reaction increases to supply the respective load current.

The large step in current density results in a large change in stack temperature. The large thermal capacitance results in a settling time to the new operating temperature of about 18 minutes.

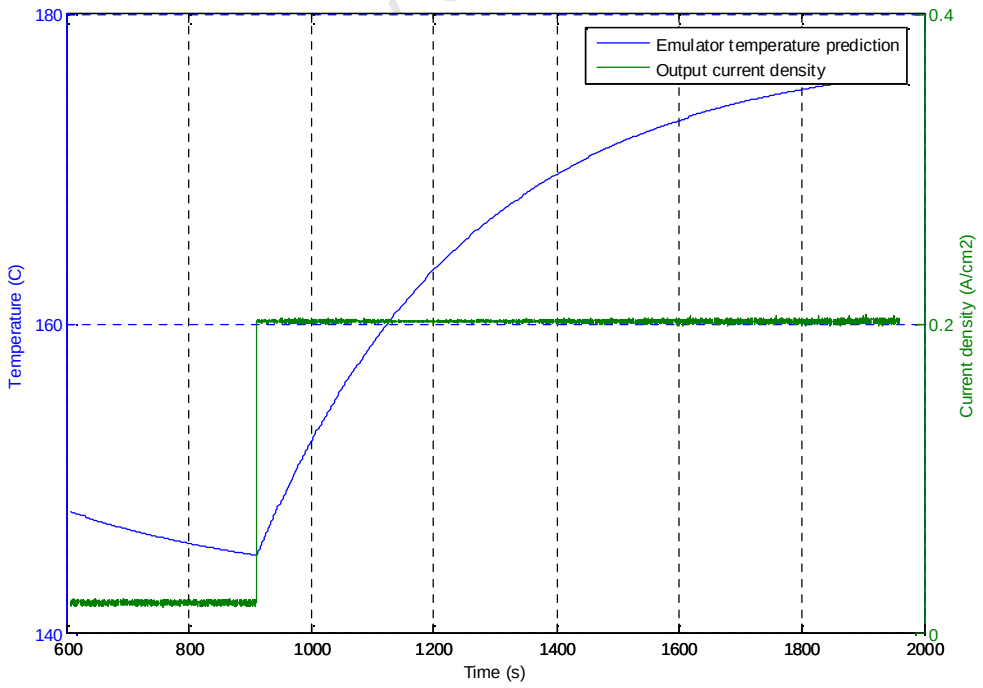

Figure 7.5. Emulator output current density and temperature prediction.

Smaller current steps were performed at higher current densities to evaluate response times and performance. The small load steps have a large effect on stack voltage under and overshoot as shown in figure 7.6. The more aggressive current step has the same effect on the recovery rate as the larger step discussed above. The emulator output demonstrates good correlation to the experimental stack and the model. Voltage ripple is barely visible as a result of the interleaving effect despite the small output filter size.

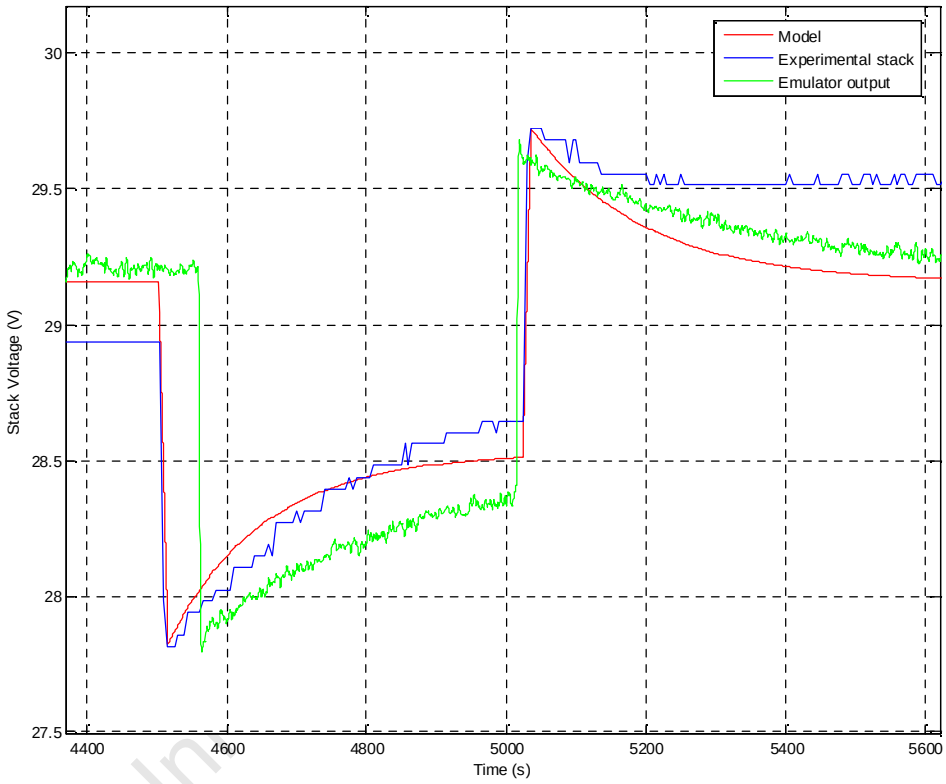

Figure 7.6. Comparison of voltage responses for 0.2A/cm^2 to 0.25A/cm^2 steps.

The output current density and the corresponding temperature of the system are shown in figure 7.7. The temperature of the system does not reach steady state before the current is reduced at 5020s during the test. The increase in stack temperature is directly proportional to the increase in output power as can be seen from the smaller ΔT in the response.

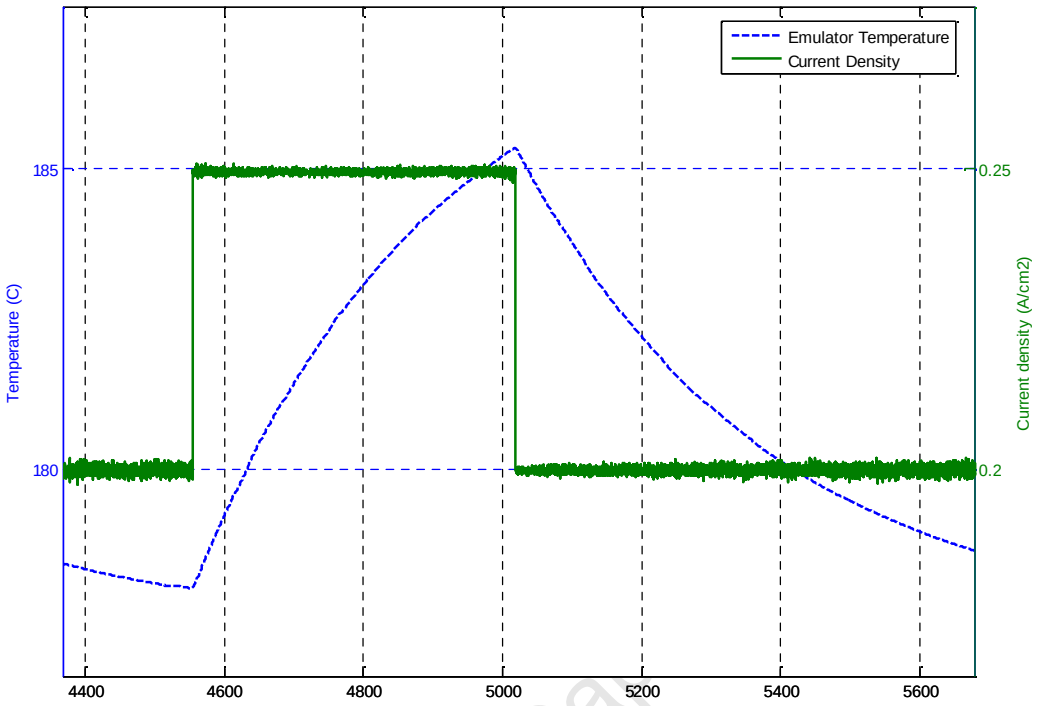

Figure 7.7. Emulator output current density and temperature prediction.

The delay in flow rates affects the stack voltage to a lesser extent over the long time range as discussed in chapter 3.

B. Emulation of short time range step response

To demonstrate the ability of the emulator system to reproduce the short time and long time range dynamics of the fuel cell, the 0.2 A/cm^2 to 0.25A/cm^2 current steps were reproduced under accelerated conditions. This was done by appropriately modifying the dominant time constants in the model to reach steady state in a shorter period of time. The outputs of the power stage and control stage converters were recorded to demonstrate system performance.

The emulator output voltage response is shown in figure 7.8. The settling time as a result of the temperature response has been reduced to a great extent. This ability allows the emulator to reproduce test results within a short period of time. If power conditioning control systems are being tested by utilizing the output, it will significantly reduce development time. The electrical and fluidic time constants influencing the short time response of the emulator were left

unchanged. These are now visible on the accelerated long time response in figure 7.8 as indicated.

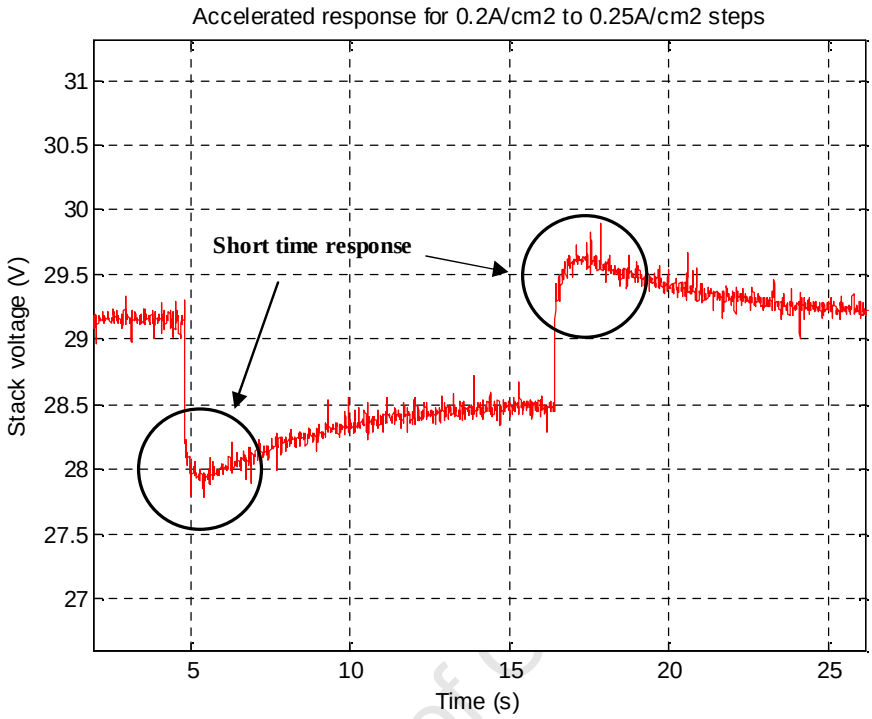

Figure 7.8. Emulator output voltage for an accelerated test.

The short time response is detailed in the magnified results of figure 7.9. Upon the initial load step there is an instantaneous rise in voltage as a result of the internal cell and stack level resistance. It is evident that the emulator is able to maintain output at the reference despite the sudden change in current. There is no significant rise or drop in voltage due to the filter components themselves. It is then followed by a slower rise in voltage, which is caused by the electrical dynamic components as predicted by the model. This is similar to that of large capacitor being charged or discharged. This component is represented by the charge double layer capacitance of the fuel cell which is incorporated in the model

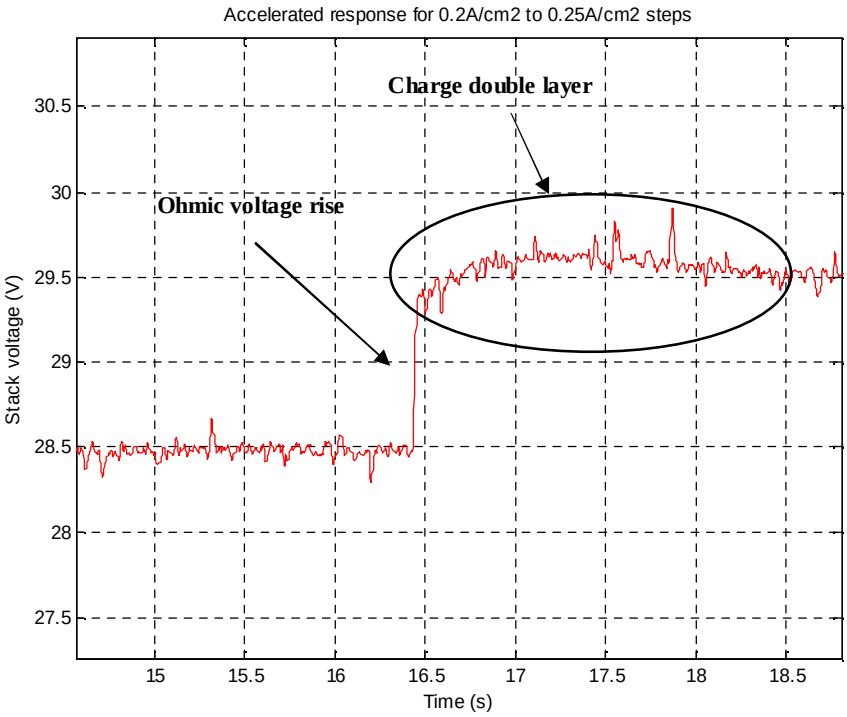

Figure 7.9. Emulator output voltage for an accelerated test (magnified).

The switching noise propagating on the recorded signal in the dSpace platform is still evident with a peak to peak magnitude of about 200mV. The implemented oscilloscope has a better noise rejection ratio and was used to verify the dynamic performance of the emulator system. The emulated voltage step response for a load step is depicted in figure 7.10. The clean DC component is clearly visible and confirms the results captured by the dSpace software. The interleaving effect of the control stage demonstrates good ripple cancellation capabilities under transient state for high output current values.

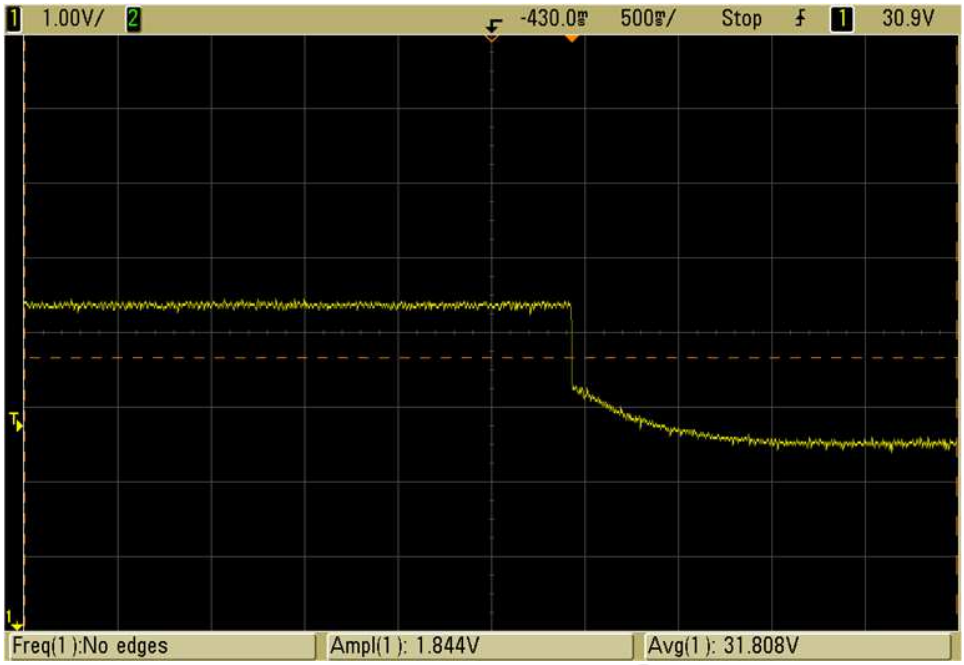

Figure 7.10. Emulator output voltage during a current step as captured on a digital oscilloscope.

The DC link voltage generated by the power stage converter is shown in figure 7.11. The voltage under and overshoots are clearly identifiable. A slow response time on the DC link allows the control side converter to adjust the duty cycle as required to maintain the output voltage at the fuel cell reference since the control systems are decoupled. The DC link value will track a delayed average of twice the emulator output voltage as can be seen in the figure, allowing the control stage to operate at a nominal duty ratio of 50%.

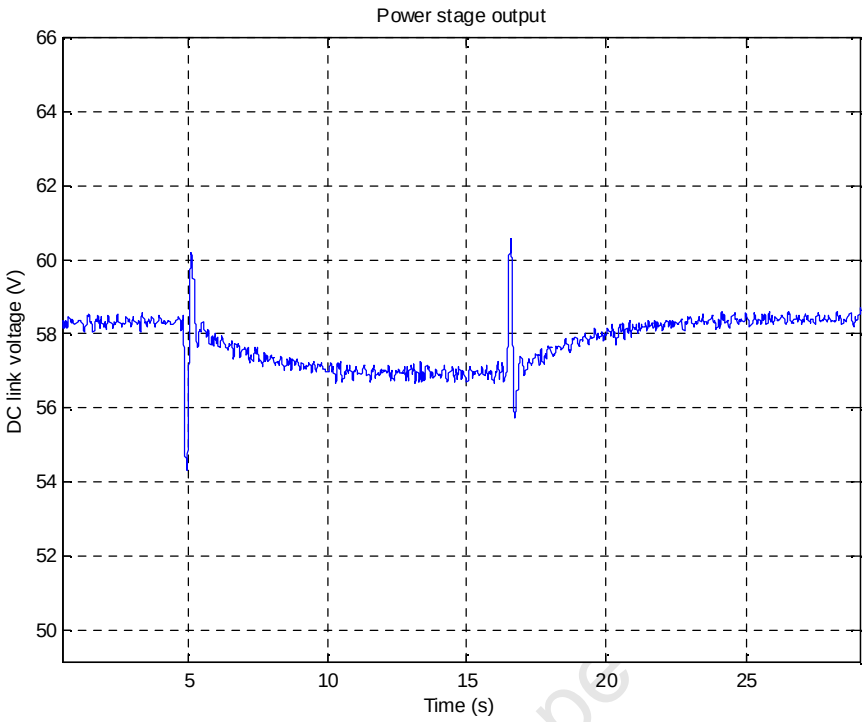

Figure 7.11. Power stage output voltage during test.

The two stage approach for the emulator hardware was mainly adopted to make use of the ripple cancelation ability of the multiphase interleaving principle. This resulted in the use of smaller filter components and allows the hardware to respond fast enough during transients to emulate the fuel cell dynamics. The power stage converter can operate as a standalone emulator, for mimicking steady state behaviour, if required. The quality and response times of the output does however not demonstrate the same performance as that of the combined system.

The standard dq0 transformation used for the vector control principle is susceptible to unbalance in the three phase system. This results in oscillations propagating on the DC components at twice the grid fundamental frequency and is increased by the use of only two phases in the transformation. This is evident in the captured direct and quadrature current waveforms in figure 7.12 and 7.13.

Despite this, the system is able to keep the quadrature current at the zero reference point, allowing for unity displacement power factor operation under steady state conditions. The direct axis component reacts fast enough to recover the DC link voltage under transient state and deliver the required power to the control stage converter.

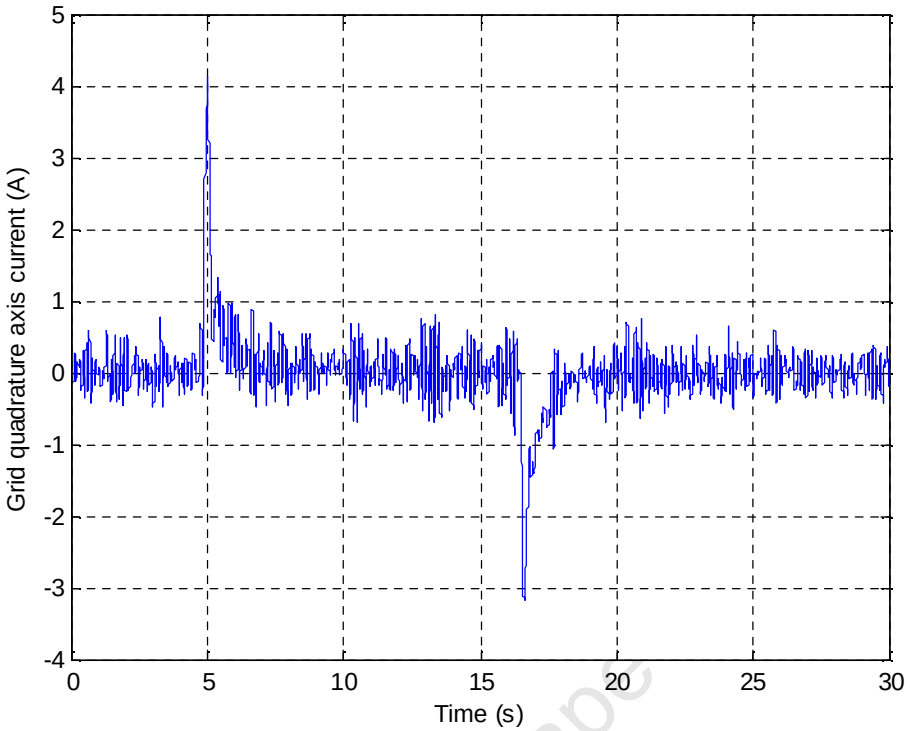

Figure 7.12. Grid quadrature current.

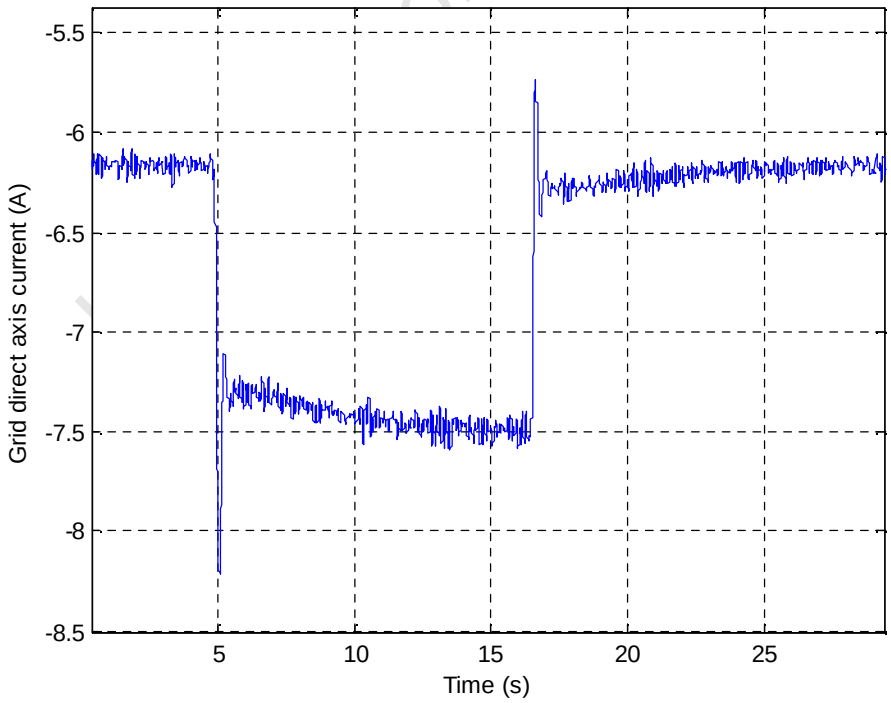

Figure 7.13. Grid direct current.

IV. RESPONSE TO PULSED CURRENTS

As discussed in chapter 4, the fuel cell stack will produce a specific response for a pulsed current. As the frequency of the pulses is increased, the peak to peak magnitude of the voltage response will decrease. Figure 7.14 shows the voltage response of the emulator for a very low pulsed current frequency of 0.1Hz. The voltage undergoes a complete transition from one set point to the new set point in the short time range. The effect of the charge double layer capacitance will dominate the shape of the waveform at such a low frequency.

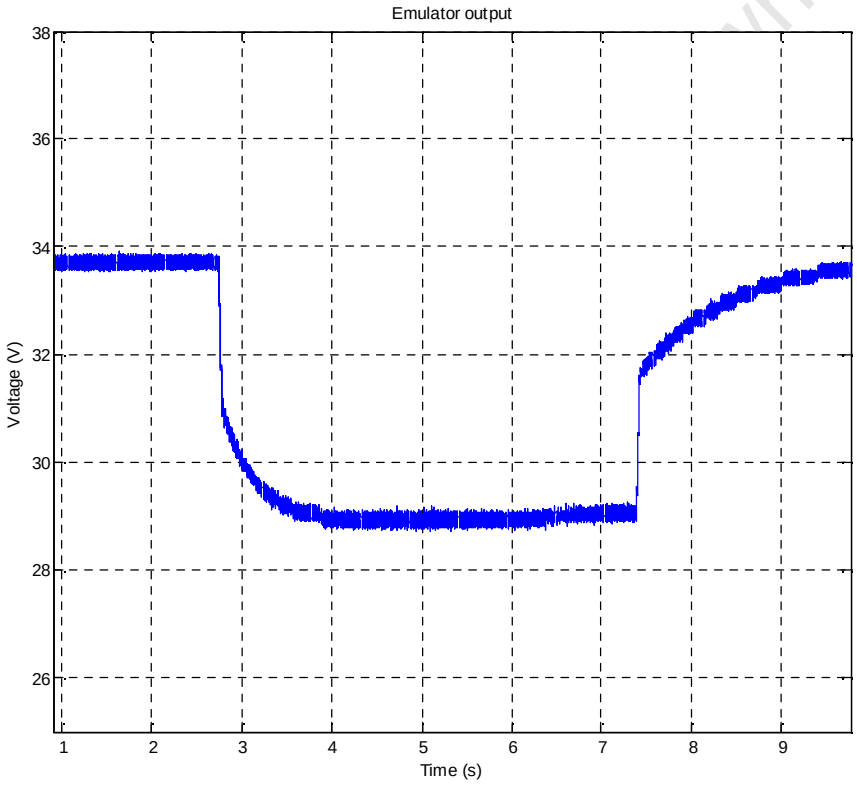

Figure 7.14. Emulator output for a 0.1Hz pulsed current.

For an increase in current frequency, the peak to peak magnitude of the voltage decreases as the capacitance of the fuel cell does not have sufficient time to charge or discharge. The drop over the internal and stack resistance will dominate the shape of the waveforms at higher frequencies as can be seen in figure 7.15.

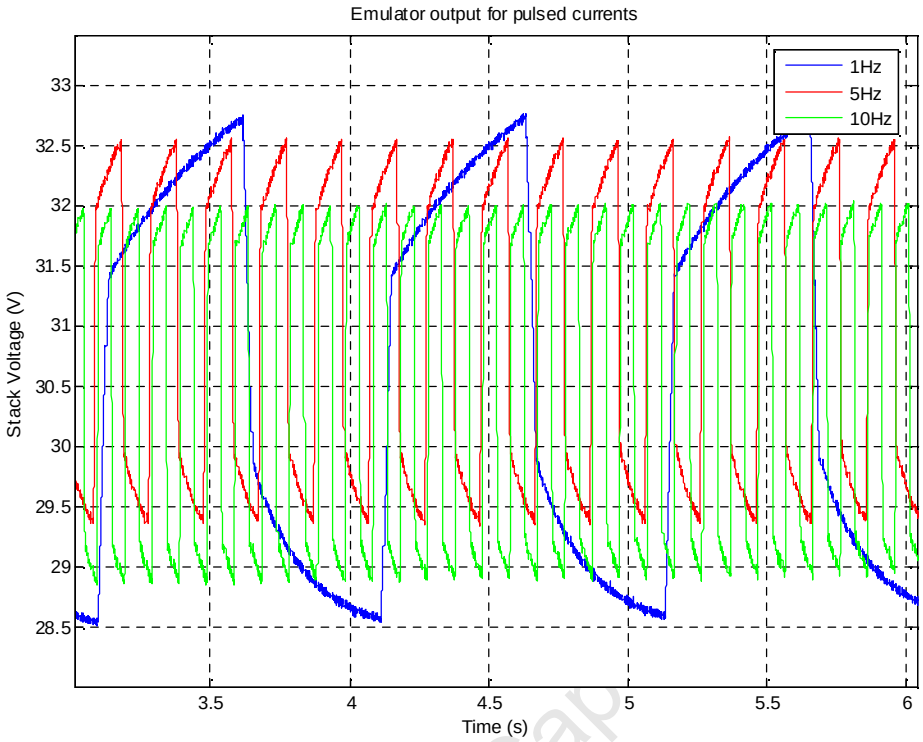

Figure 7.15. Emulator output for a 1Hz, 5Hz and 10Hz pulsed current.

The value of the charge double layer capacitance varies with frequency as shown in the experimental response of [14], [29], where EIS tests were conducted on the fuel cell stacks. At higher frequencies, the effect of the capacitance will still be visible on the output voltage waveforms.

The output of the emulator for the pulsed currents can accurately replicate the fuel cell dynamics up to a frequency of about 25Hz. This functionality can be used to predict the effects of stack degradation when connected to a fuel cell power conditioning system. Replicating the exact waveforms at frequencies up to the switching frequencies of the converter itself is not achievable since the emulator is itself operating in this range.

The control systems for the power conditioning systems can be tested by running the emulator in the low frequency range and predicting the effects at higher frequencies as the non linear ouput waveform will follow the same magnitude trajectory.

The response of the control stage converter control system for these pulsed currents is shown in figure 7.16. The output voltage is able to remain locked to the non linear reference with a delay of about 1ms. The control systems as designed in chapter 5, delivered good results during testing and produced no visible voltage under or overshoots during the fast transient reference tracking.

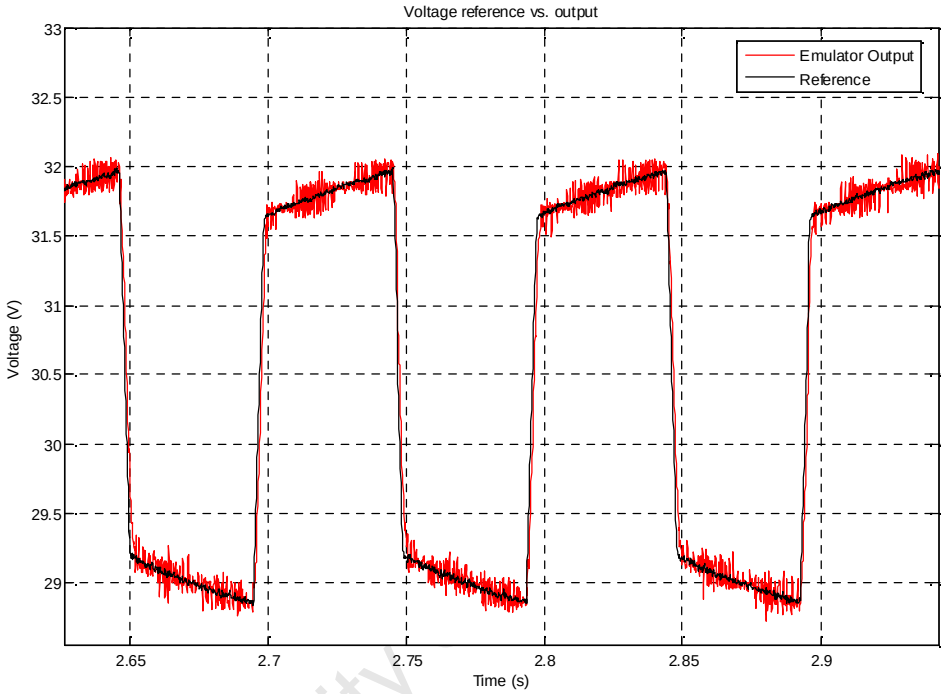

Figure 7.16. Emulator output and reference during a 10Hz pulsed current test.

The output voltage of the emulator for a 1Hz pulsed current test captured on the digital oscilloscope is shown in figure 7.17. No significant voltage overshoots are visible; the emulator is able to deliver acceptable performance for this type of test.

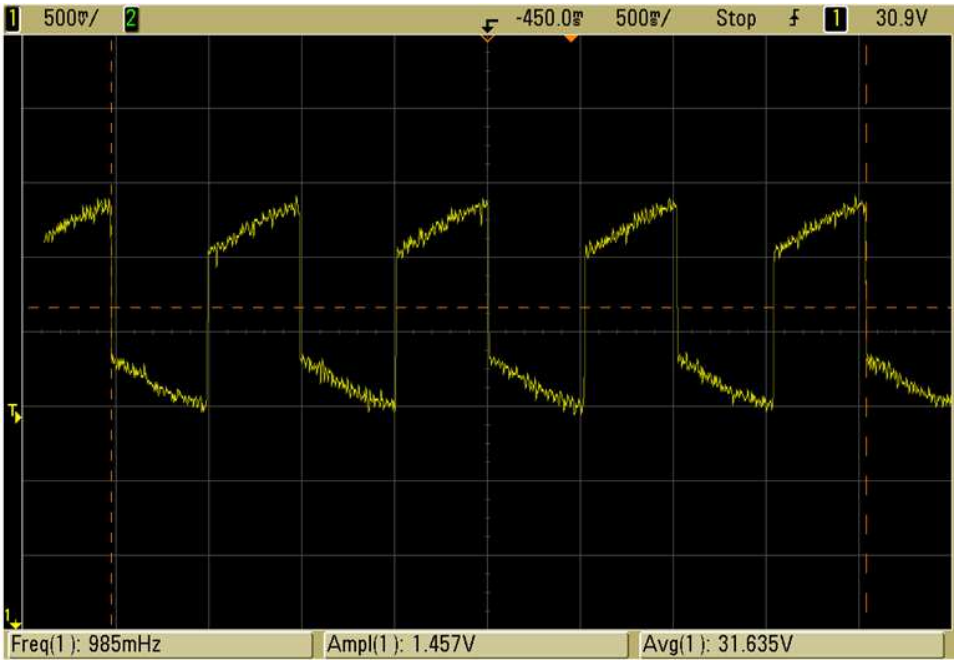

Figure 7.17. Emulator output during a 1Hz pulsed current test as captured on the digital oscilloscope.

V. EMULATION OF THE FUEL STARVATION PHENOMENON

The fuel starvation phenomenon, which is discussed in chapter 3 section VI F, was emulated by increasing the air flow delay time constant in the system. During a current step the required oxygen cannot be delivered to the reaction sites and the output voltage will drop. This effect combines the normal short time response with an additional component, requiring the emulator to undergo a number of voltage changes during the test. To demonstrate the accuracy of the system, only a small amount of starvation was reproduced resulting in an additional voltage loss of 250mV during the current step.

The output of the emulator is compared to the simulated results in figure 7.18. The resulting voltage drop as a result of the starvation is indicated. It is evident that the voltage drop across the resistance and the charge double layer effect is still present in the outputs. The emulator is able to reproduce the voltage waveform very accurately in real time when compared to the simulated voltage output. The switching noise is still present on the dSpace data acquisitioning channels;

the same waveform was captured on the digital oscilloscope to demonstrate the accuracy of the system for the combination of dynamic phenomena.

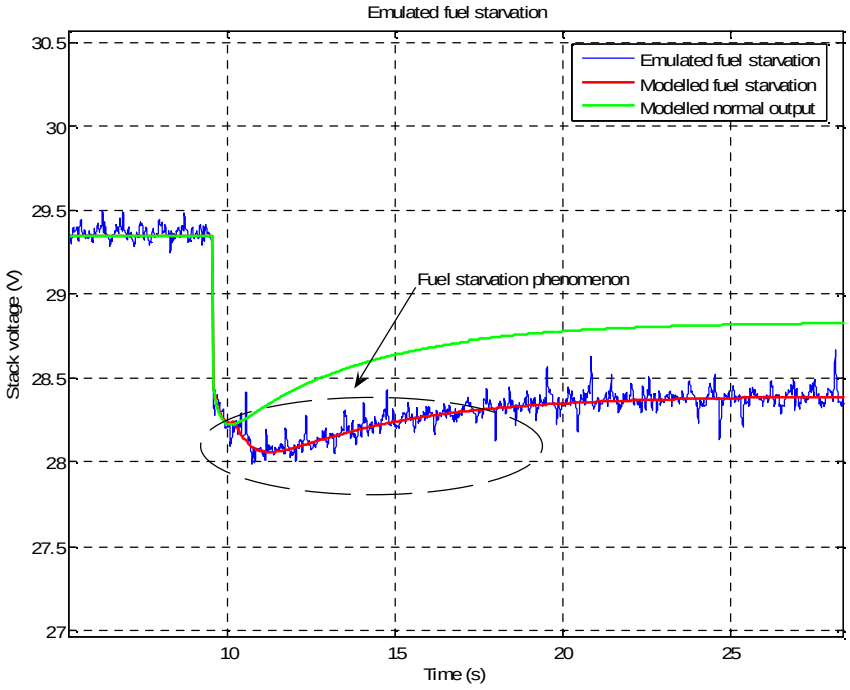

Figure 7.18. Emulator output and model output for fuel starvation and normal fuel cell output.

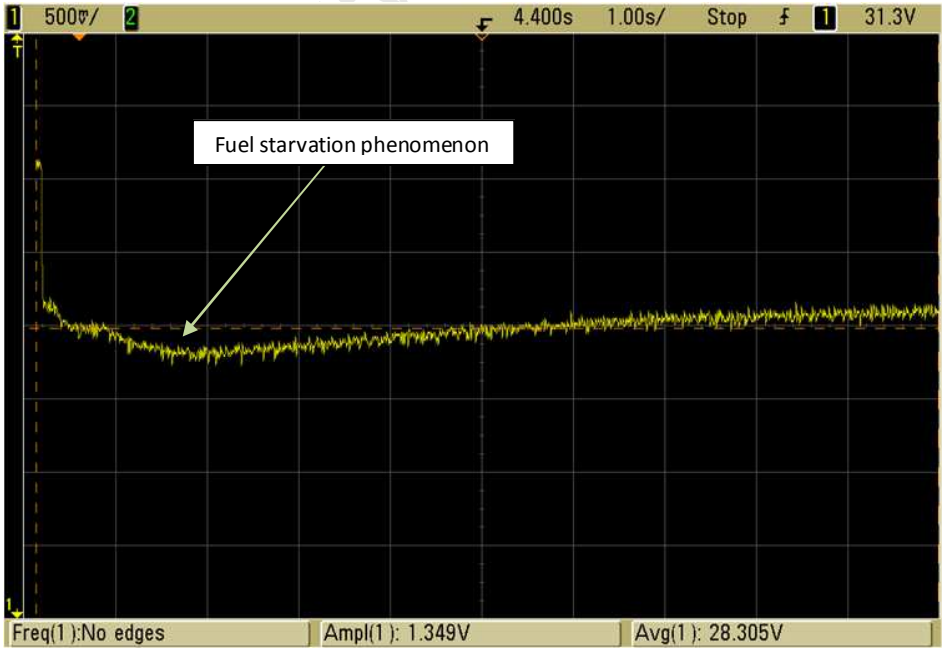

Figure 7.19. Emulator output captured on the digital oscilloscope during the fuel starvation test.

VI. CONCLUSION

This chapter presented the experimental results for the final emulator system for both steady state and transient load tests. The emulator polarization curves obtained were compared to the simulated and experimentally obtained curves and demonstrate acceptable accuracy. Small changes in load slew rate and temperature response are shown to have an impact on the generated polarization curves.

The transient response of the emulator was tested for two separate load current steps and compared to that obtained in simulation and during testing of the experimental stack. The emulator is able to replicate the transient voltage response with a small error margin. To demonstrate the flexibility of the emulator when compared to the actual fuel cell system, the step response was reproduced under accelerated conditions. The short time and long time response were shown to correspond with the actual stack and that available in literature. For rapid prototyping applications, the emulator system can be used to great effect.

The ability of the emulator system to replace an actual stack during prototyping was verified by reproducing selected steady state and transient phenomena that would occur during use. The polarization curve hysteresis phenomenon shows the effect of temperature on the output voltage during steady state. This was successfully reproduced and the voltage hysteresis band can be varied by changing the appropriate parameter in the emulator.

Transient effects such as the response to pulsed currents were shown to produce a non linear voltage response. The emulator was able to remain locked to the reference with minimal overshoot and good response times. The effect of fuel starvation on the output voltage was emulated by reducing the response time of the oxygen in the system. The small drop in output voltage was successfully reproduced at high current densities.

The switching noise propagating on the system could not be eliminated and is inherent to the operation of the MOSFETs. Despite this, the quality of the output voltage was not reduced to a great extent.

8. CONCLUSION AND FINAL REMARKS

I. SUMMARY

The results obtained through simulation of the HT PEM FC model, the control systems and the experimental results of the prototype emulator confirmed the following:

- The lumped parameter model of the high temperature system is able to reproduce the steady state and transient behaviour of the actual electrochemical system with good accuracy. The modelling approaches and characterizations methods were presented in chapter 2 for the low temperature systems. The model was adapted for high temperature operation and reflects the increase in efficiency and output power at higher operating temperatures. The three main dynamic components were incorporated into the model and delivers good accuracy when compared to that of the actual systems and more complex models available in literature.
- Operational phenomena that occur in an actual fuel cell system during use were presented and reproduced by the model. This includes polarization curve hysteresis that occurs in steady state and reactions to dynamic conditions such as pulsed current response and the fuel starvation effect.
- A study on existing emulator designs was presented, highlighting the limitations. The salient performance criteria of the hardware were used to justify a more complex topology. To reproduce the outputs of the fuel cell during transient state, a control stage converter based on a multiphase interleaved buck topology is presented. The ability of the topology to produce an output with a small ripple component with the use of smaller filter components allows the system to perform well under transient state.
- A comparison between the dynamic performance of a normal buck and a double phase system was presented in chapter 5. The reduction in filter sizes and the increased number of phases produced the expected enhancements in dynamic performance. The design of the control system for the control stage converter was done in accordance with recognised frequency response techniques.

- The power stage converter was designed to generate the steady state response of the fuel cell at double the output voltage. A vector control strategy was employed to generate the DC link from a three phase source while maintaining unity power factor. The control systems were designed based on the modulus and symmetric optimum techniques.

II. CRITICAL EVALUATION OF OWN WORK

The system performed as expected during experimental testing as shown in chapter 7. The performance specifications in terms of dynamic response as required by the simulated response of the HT FC system were successfully met. The step responses done on the control stage and power stage converters confirmed the theoretical and design requirements. It is shown in this dissertation how to design the hardware and control systems for a two stage emulator with emphasis on the dynamic response and stability based on the transfer functions obtained.

The contributions made by this work includes the design of the emulator system based on the multiphase interleaved buck topology and the use of the ripple cancellation effect by employing an active front end that allows the multiphase system to operate at a critical duty ratio during steady state. The prototype system demonstrated exceptional voltage ripple cancelation during steady state as well as transient state considering the size of the filter components and the output power of the system. The concept of critical inductance as introduced by [45] is used to design the filter components to increase transient performance to an acceptable level.

The dynamic model for a HT PEM FC system was successfully integrated with the control systems for the power electronics on a single processing platform. The shortcomings of the DS1104 system had an impact on system performance as discussed in chapter 5. The system nevertheless demonstrated good control and stability while conducting tests. This included making changes to model parameters in real time to evaluate the effects on the output. The use of a three phase voltage source converter with a space vector control system delivered unity displacement power factor during steady state. Due to the limit of ADC channels on the feedback interface, only two of the three phases were monitored and used for the abc to dq0 transformations resulting in oscillations from the unbalanced three phase system.

The ability of the final system to emulate small dynamic effects was demonstrated in chapter 7. The fuel starvation voltage decay occurs immediately after the voltage decay caused by the charge double layer effect and required the system to respond accurately and quickly. The final system was able to reproduce the non linear voltage waveforms required during a pulsed frequency test. Variations in the reference were tracked up to 1ms thus improving emulation capability for fuel cell dynamics as done by conventional systems by a factor of 10.

III. FUTURE WORK

Although the experimental results obtained during testing represent that of a fully functional emulator system, the following improvements are suggested for future work:

- Incorporate soft switching techniques to reduce the amount of switching noise propagating on the feedback;
- Implement the control stage converter control system on a dedicated DSP with a high clock frequency and sampling time to increase the response times;
- Introduce the third phase of the grid voltage and current to reduce the amount of oscillations on the dq0 transformations;
- Implement positive and negative sequence component compensation on the space vector control of the power stage converter to operate the system under unbalanced conditions;
- Investigate the performance of a four phase interleaved buck converter for the control stage converter;
- Increase the switching frequency of the converters to reduce filter component size even further;
- Increase the complexity of the HT PEM FC model by running a multilayer model that predicts the output of each independent cell and determine the cost of the additional processing power required versus the gain in system accuracy.

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10. RESEARCH PAPERS BASED ON THIS WORK

Conference Papers

C. de Beer, P.S. Barendse and M.A. Khan, "Dynamic Modelling and Emulation of a High Temperature Proton Exchange Membrane Fuel Cell (HT PEMFC)", South African Universities Power Engineering Conference (SAUPEC), Cape Town, 2011.

Journal Papers

C. de Beer, P.S. Barendse and M.A. Khan, "Development of a HT PEM Fuel Cell Emulator Using a Multiphase Interleaved DC-DC Converter Topology", Submitted to the IEEE Transactions in Power Electronics.

APPENDIX

I. MATLAB CODE

Adapted from [13] to reproduce the PEM FC polarization curves presented in chapter 2.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculating the Voltage Losses for a Polarization Curve
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Inputs
R = 8.314; % Ideal gas constant (J/molK)
F = 96487; % Faraday's constant (Coulombs)
Tc = 80; % Temperature in degrees C
P_H2 = 3; % Hydrogen pressure in atm
P_air = 3; % Air pressure in atm
A_cell=100; % Area of cell
N_cells=90; % Number of Cells
r = 0.19; % Internal Resistance (Ohm-cm^2)
Alpha = 0.5; % Transfer coefficient
Alpha1 = 0.085; % Amplification constant
io = 10^-6.912; % Exchange Current Density (A/cm^2)
il = 1.4; % Limiting current density (A/cm2)
Gf_liq = -228170; % Gibbs function in liquid form (J/mol)
k = 1.1; % Constant k used in mass transport
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Convert degrees C to K
Tk = Tc + 273.15;
% Create loop for current
loop = 1;
i = 0;
for N = 0:150
i = i + 0.01;
% Calculation of Partial Pressures
% Calculation of saturation pressure of water
x = -2.1794 + 0.02953 .*Tc-9.1837 .*(10.^-5) .*(Tc.^2) + 1.4454 .*(10.^-7) .*(Tc.^3);
P_H2O = (10.^x)
% Calculation of partial pressure of hydrogen
pp_H2 = 0.5 .*((P_H2)./(exp(1.653 .*i./(Tk.^1.334)))-P_H2O)
% Calculation of partial pressure of oxygen
pp_O2 = (P_air./exp(4.192 .*i/(Tk.^1.334)))-P_H2O
% Activation Losses
b = R .*Tk./(2 .*Alpha .*F);
V_act = -b .*log10(i./io); % Tafel equation
% Ohmic Losses
V_ohmic = -(i .*r);
% Mass Transport Losses
term = (1-(i./il));
if term > 0
V_conc = Alpha1 .*(i.^k) .*log(1-(i./il));
else
V_conc = 0;
end
% Calculation of Nernst voltage
E_nernst = -Gf_liq./(2 .*F)-((R .*Tk) .*log(P_H2O./(pp_H2 .*(pp_O2.^0.5))))./(2 .*F);
% Calculation of output voltage
V_out = E_nernst + V_ohmic + V_act + V_conc;
```

```
if term < 0
V_conc = 0;
break
end
if V_out < 0
V_out = 0;
break
end
figure(1)
title('Fuel cell polarization curve')
xlabel('Current density (A/cm^2)');
ylabel('Output voltage (Volts)');
plot(i,V_out,'*')
hold on
disp(V_out)
% Calculation of power
P_out = N_cells .*V_out .*i .*A_cell;
figure(2)
title('Fuel cell power')
xlabel('Current density (A/cm^2)');
ylabel('Power(Watts)');
plot(i,P_out,'*');
hold on
disp(P_out);
end
```

II. SIMULINK MODELS

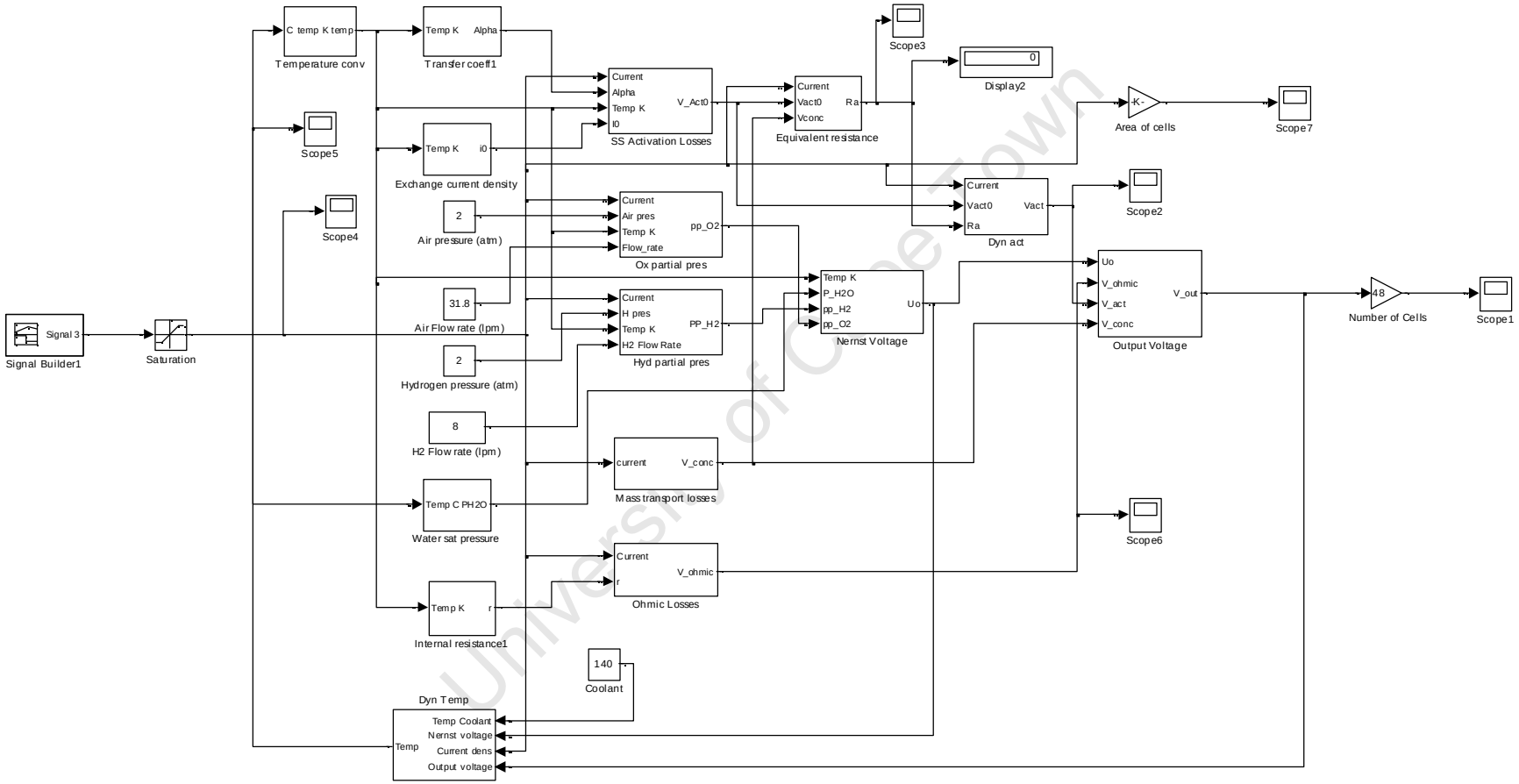

Figure A1. Block diagram of the complete HT PEM FC model in SIMULINK.

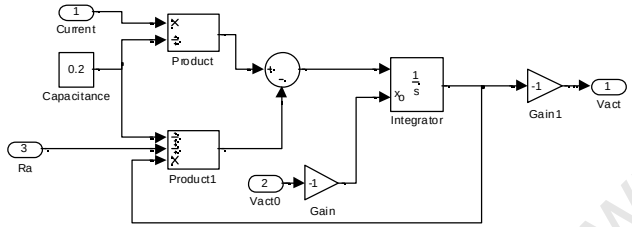

Figure A2. Block diagram of dynamic activation voltage drop calculation in SIMULINK.

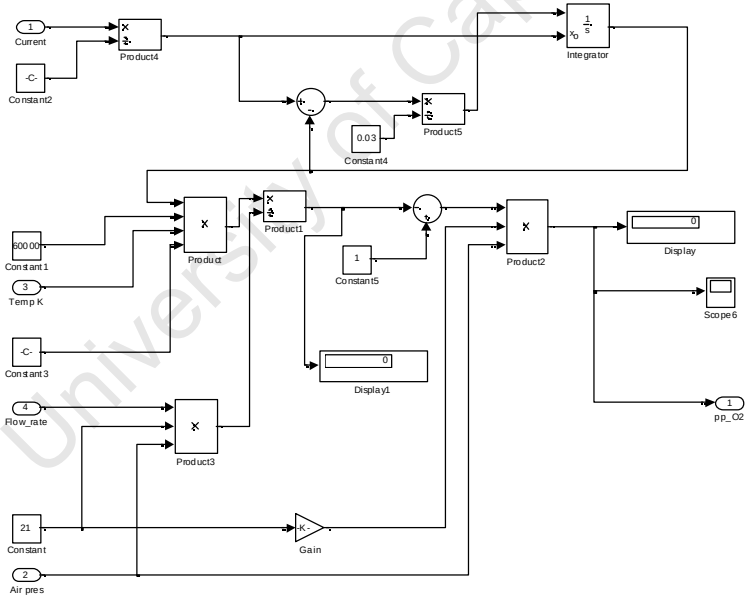

Figure A3. Block diagram of the dynamic oxygen partial pressure calculation in SIMULINK.

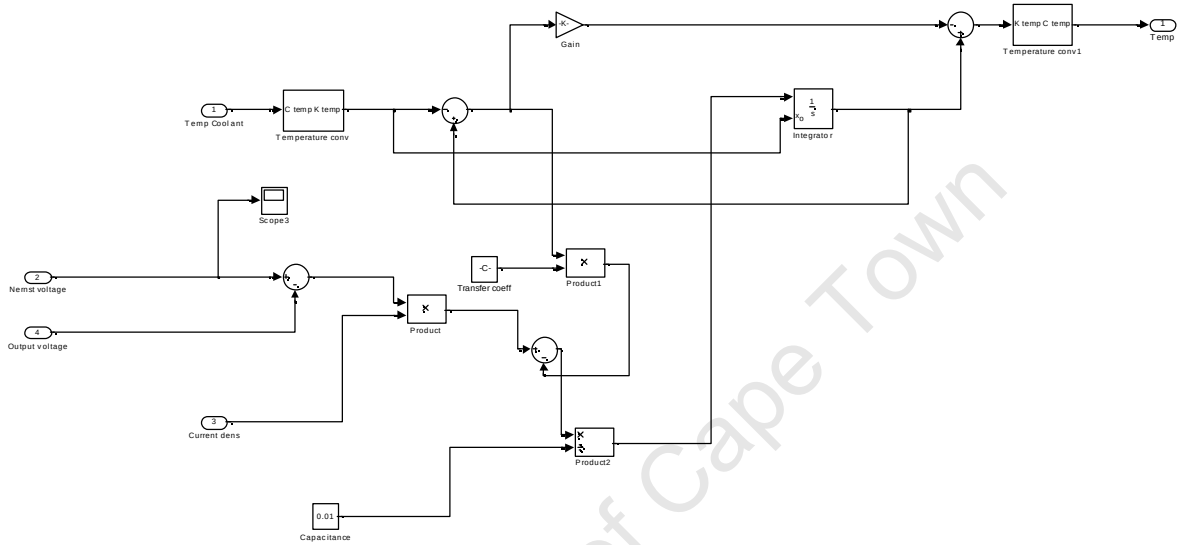

Figure A4. Block diagram of the dynamic temperature calculation in SIMULINK.

III. SELECTED PHOTOGRAPHS

Figure B1. DS1104 prototyping board.

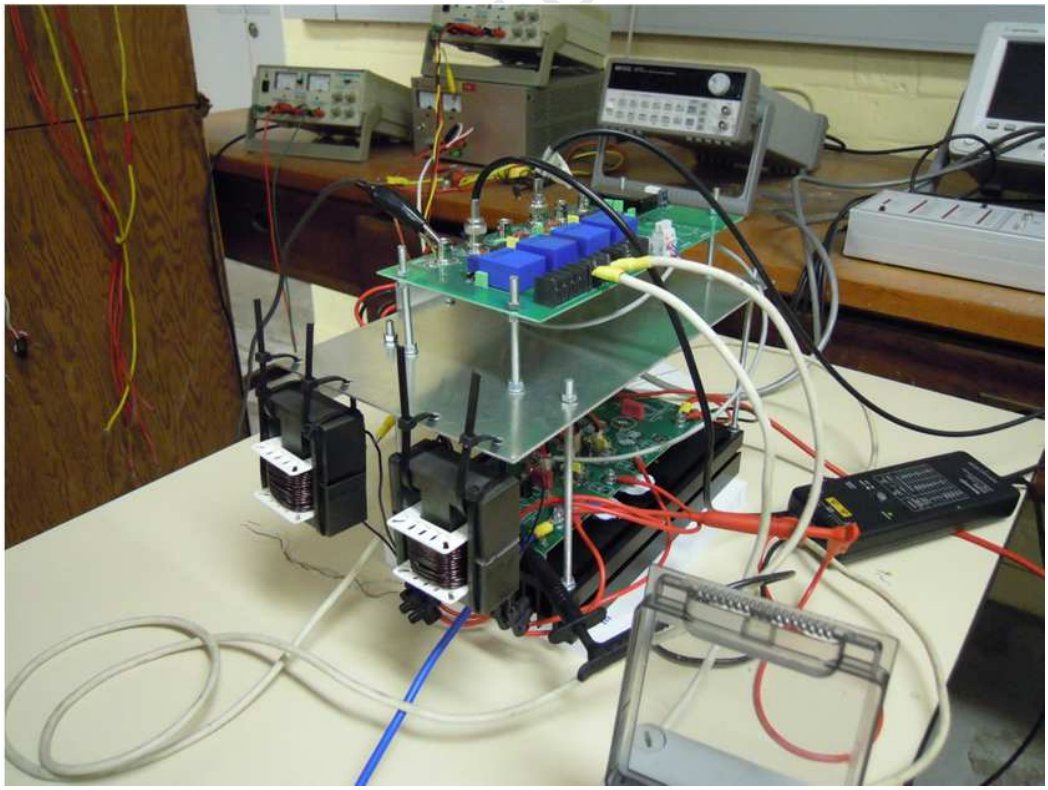

Figure B2. Assembled control stage converter.

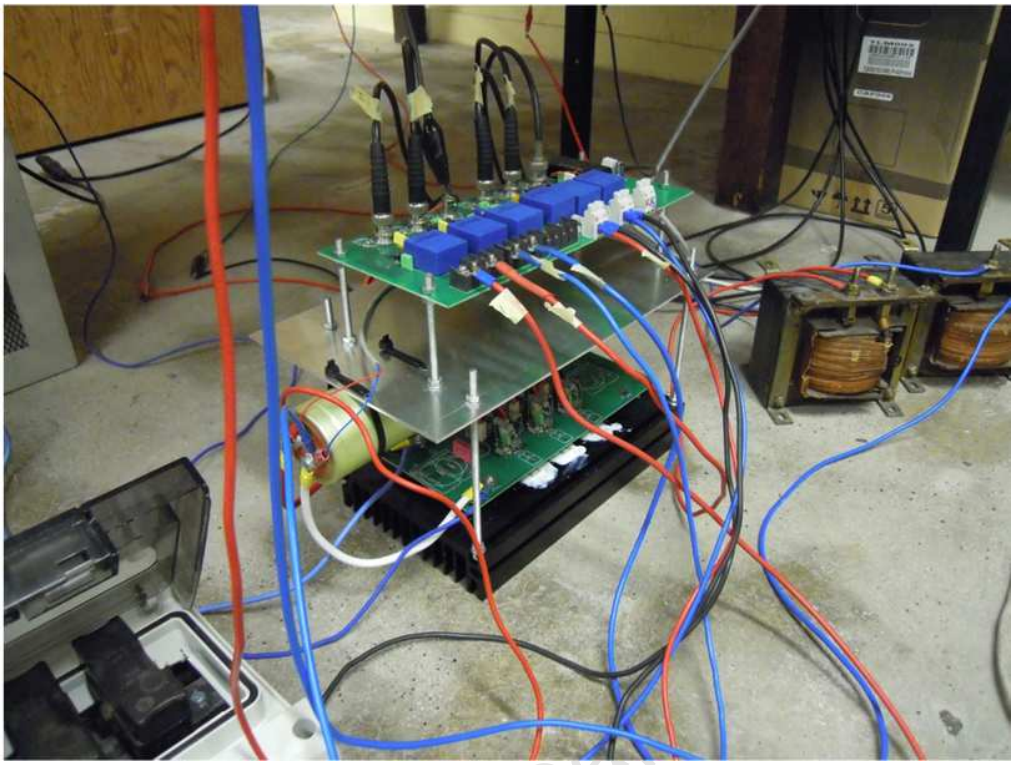

Figure B3. Assembled power stage converter.

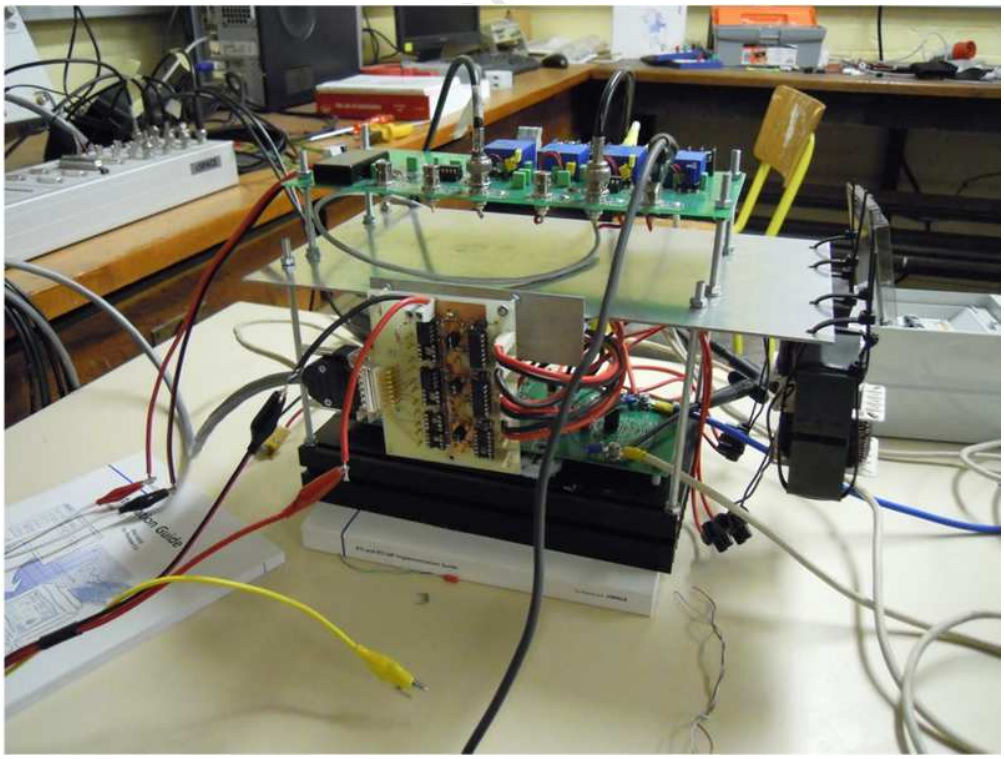

Figure B4. Connection from the dSpace system to the control stage converter interface card.

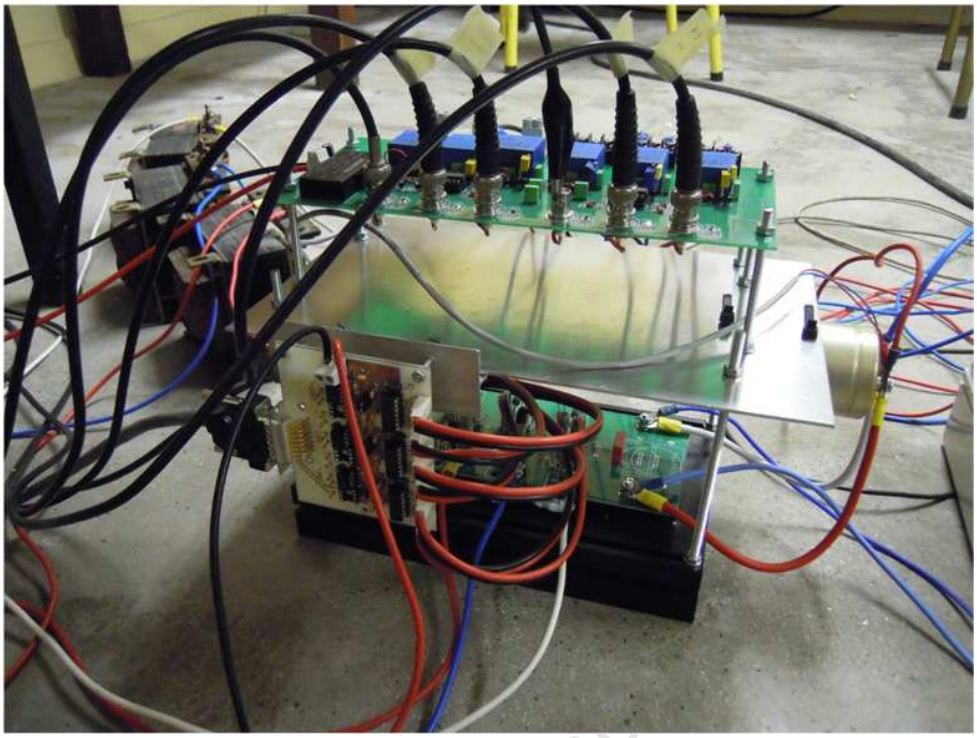

Figure B5. Connection from the dSpace system to the power stage converter interface card.

Figure B6. Fully assembled emulator system.

Figure B7. LEM transducer board.

IV. PCB DESIGNS

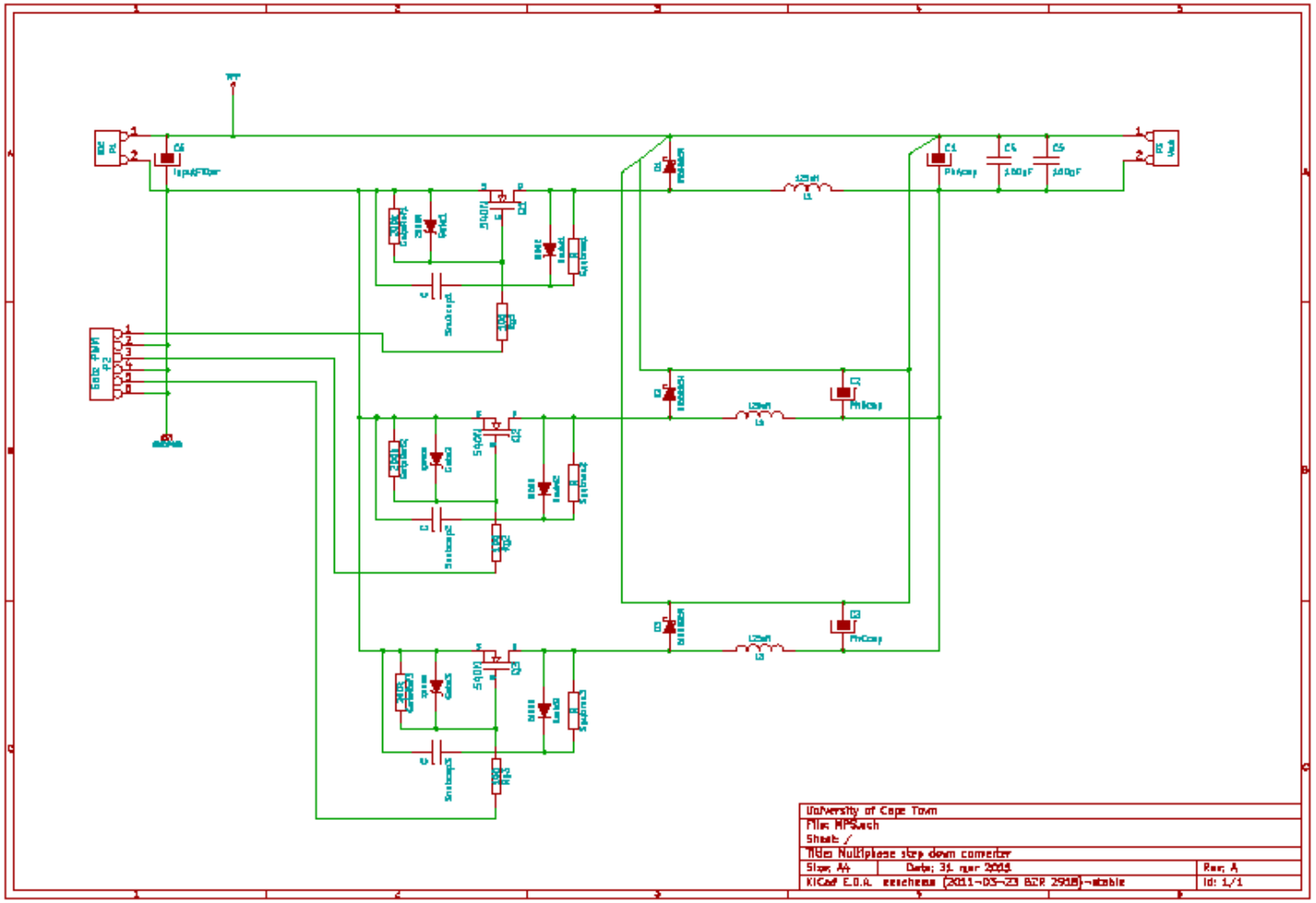

Figure C1. Circuit design of the prototype multiphase interleaved buck converter board.

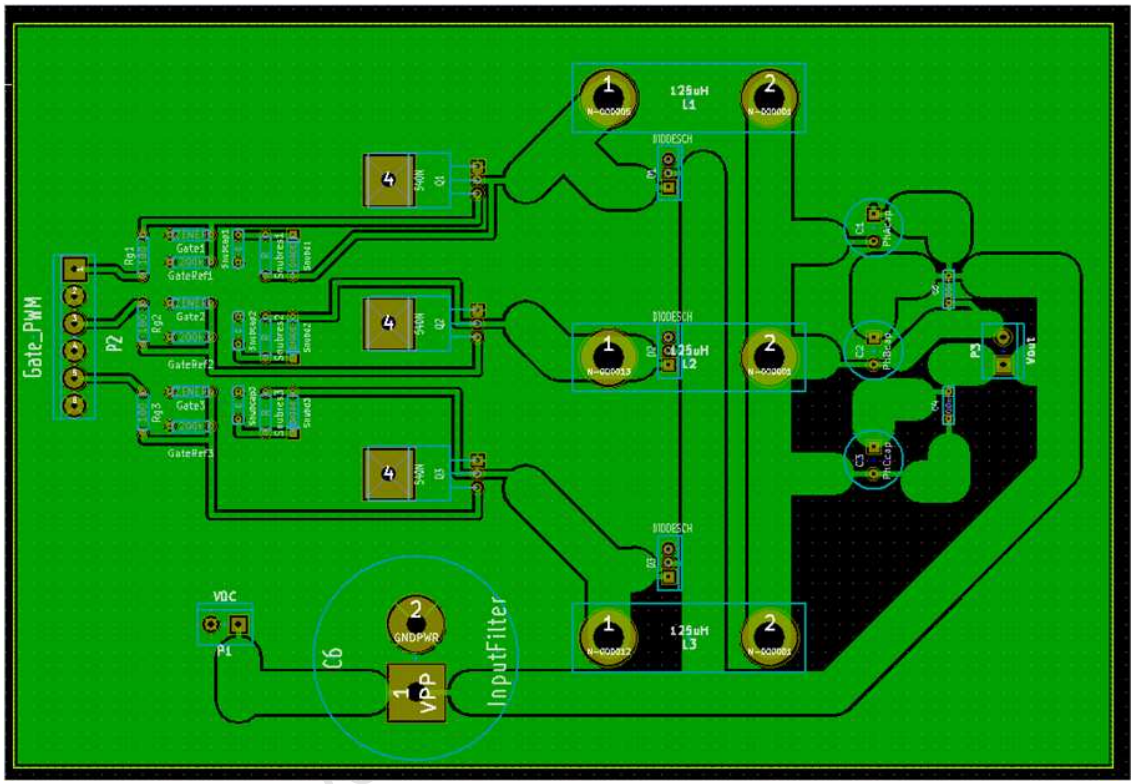

Figure C2. Circuit layout of the prototype multiphase interleaved buck converter board.

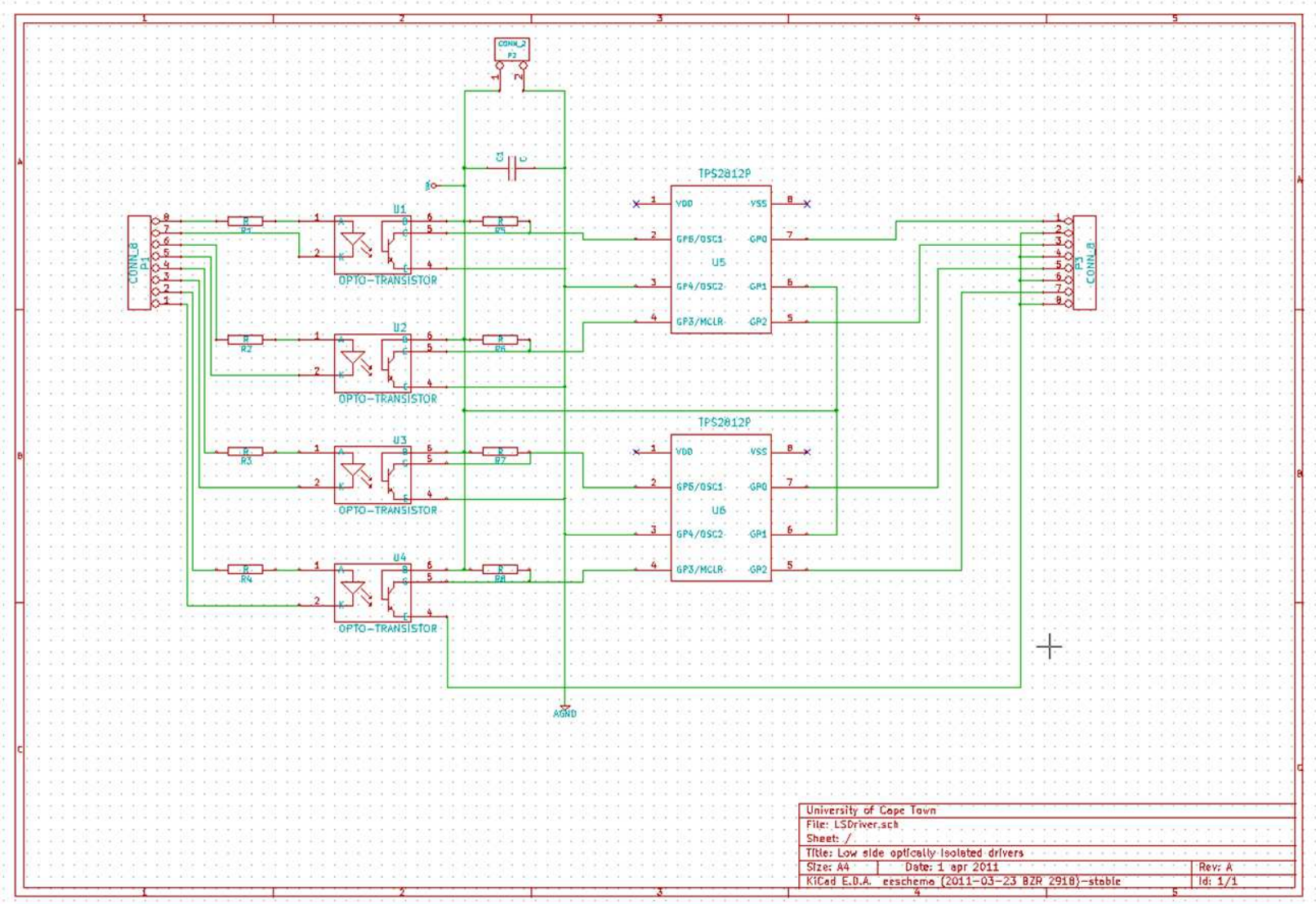

Figure C3. Circuit design of the prototype MOSFET driver board.

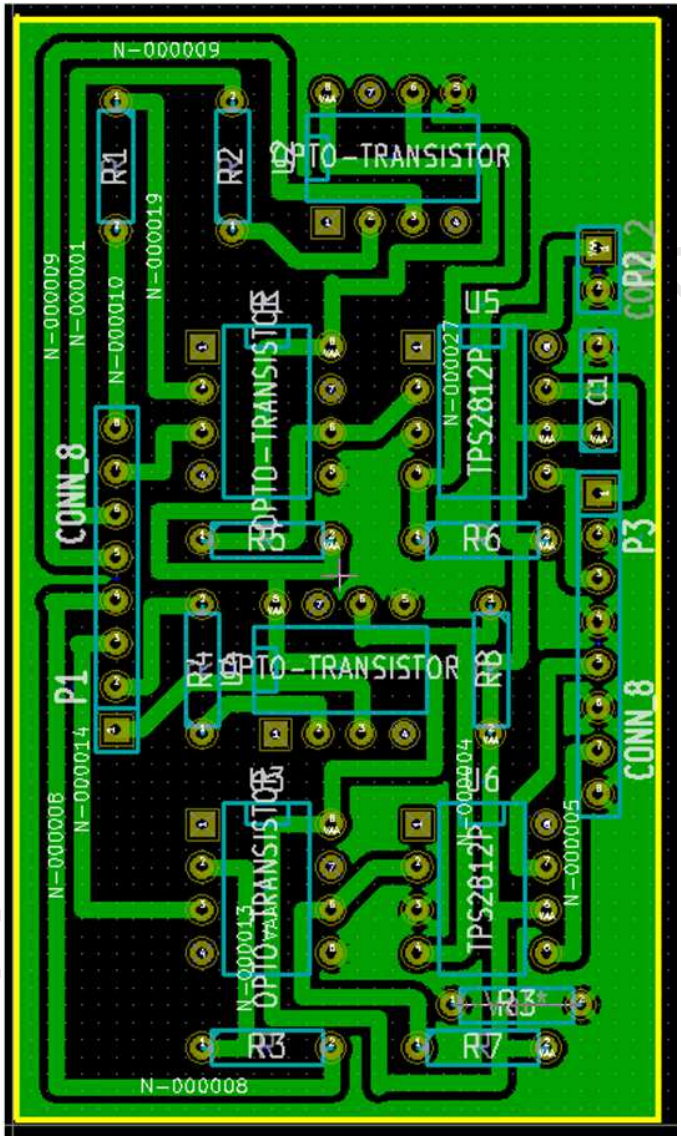

Figure C4. Circuit layout of the prototype MOSFET driver board.

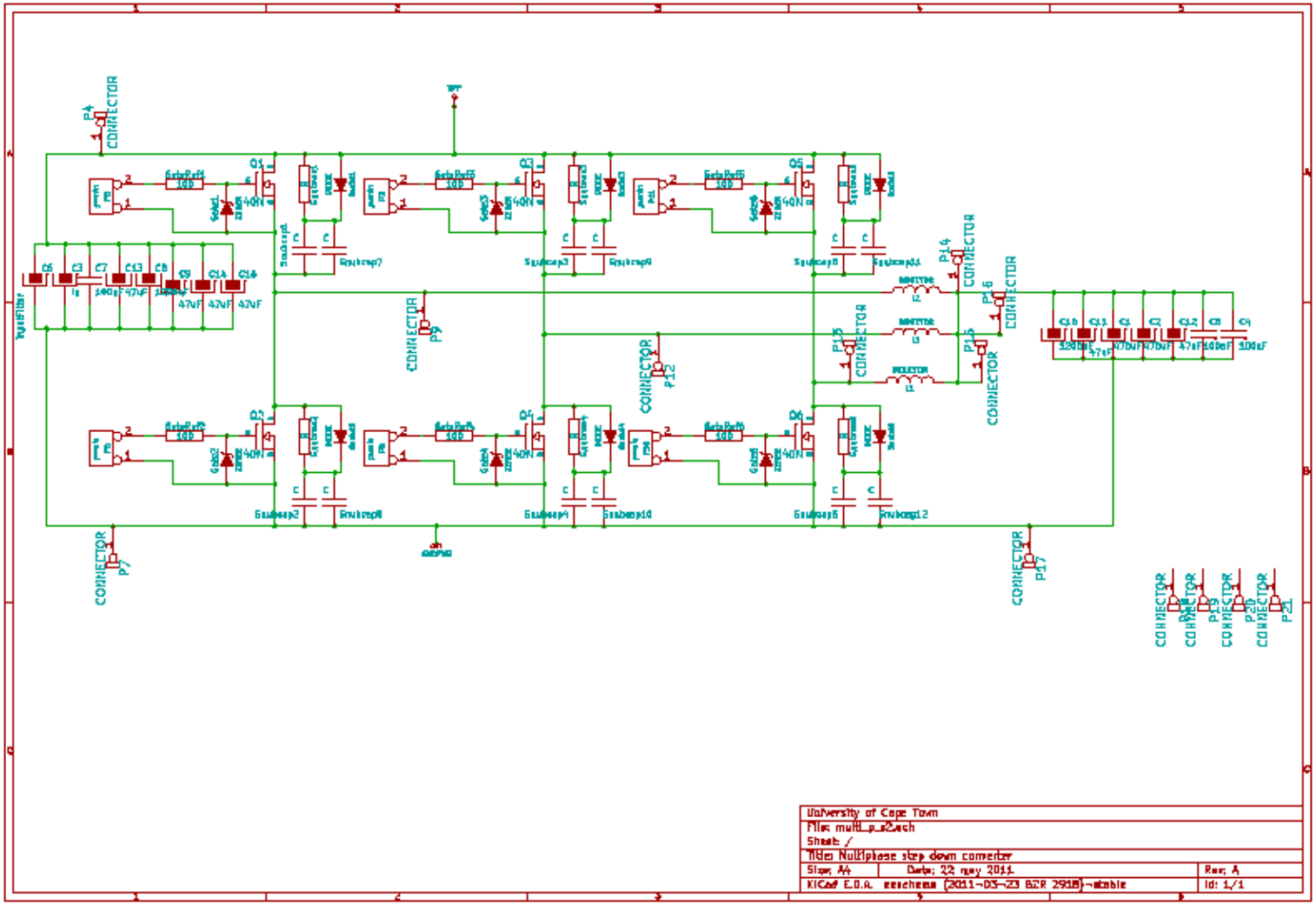

Figure C5. Circuit design of the final multiphase interleaved buck converter board.

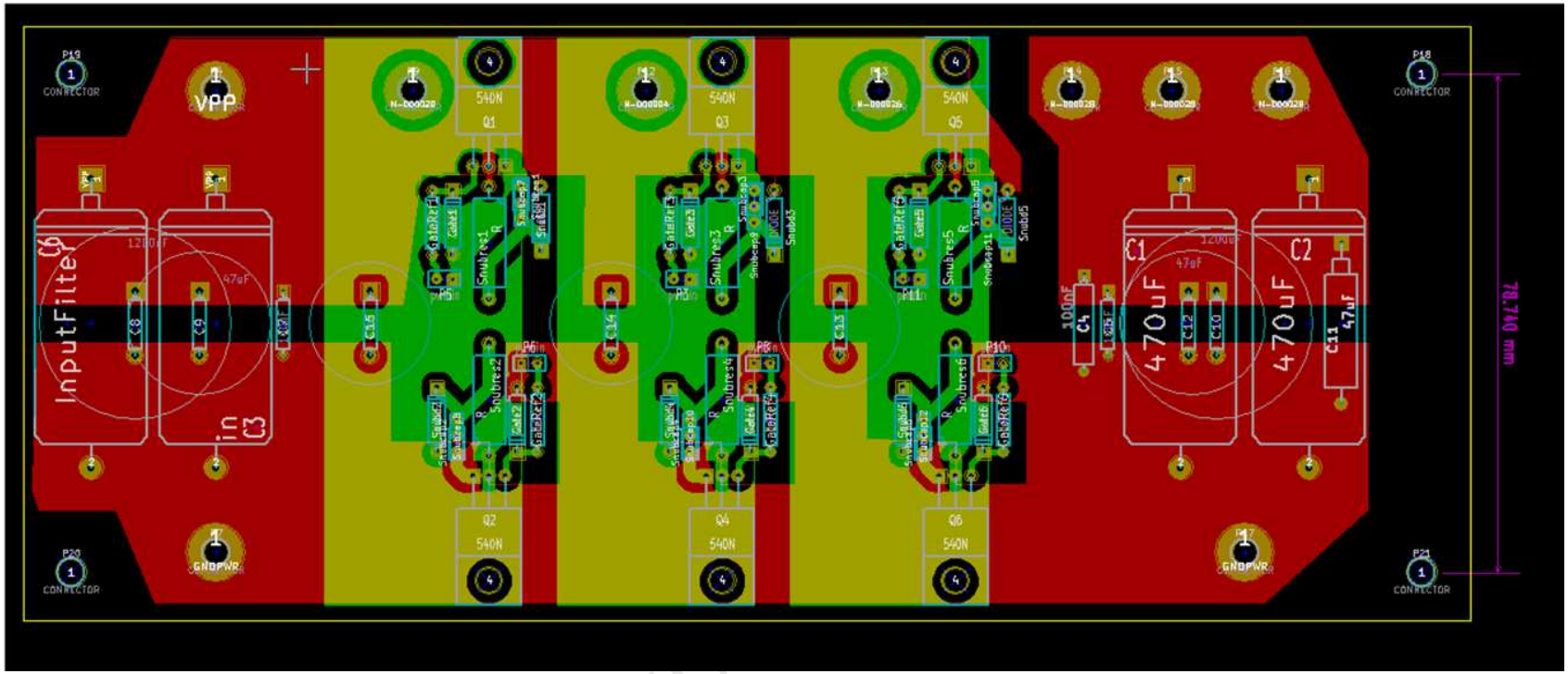

Figure C6. Circuit layout of the final multiphase interleaved buck converter board.

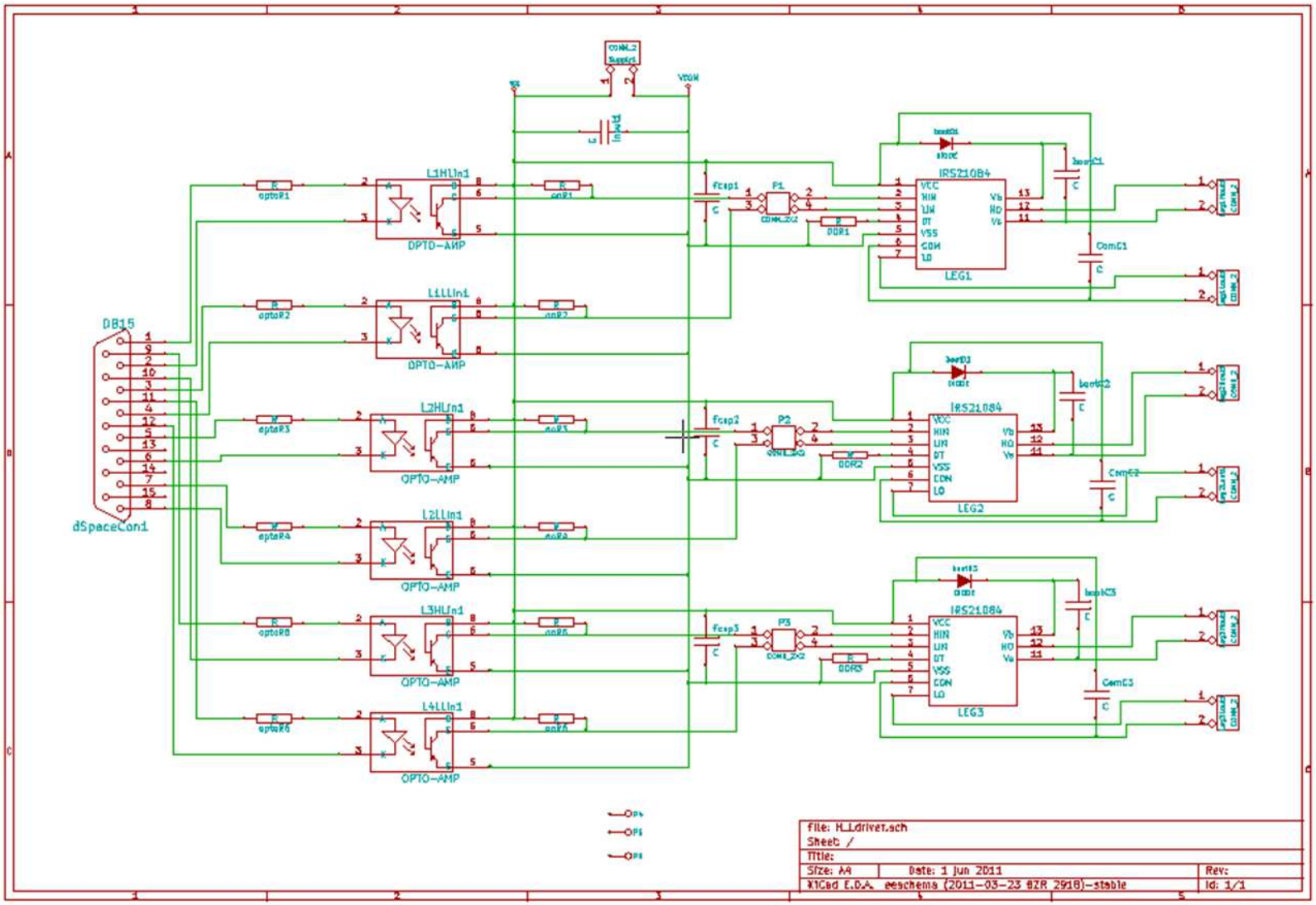

Figure C7. Circuit design of the final MOSFET driver board.

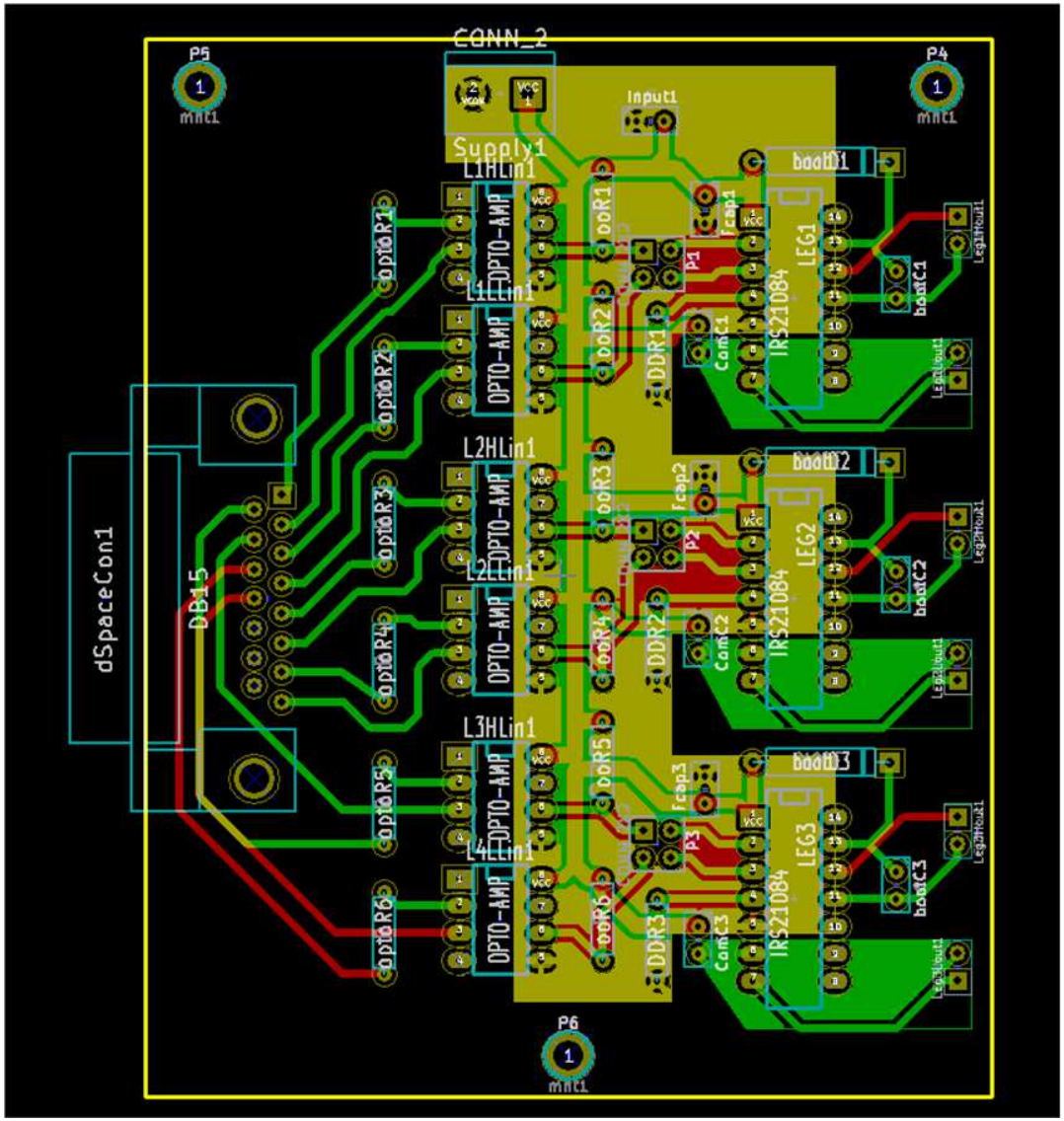

Figure C8. Circuit layout of the final MOSFET driver board.