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UNIVERSITY OF CAPE TOWN

# Design and Implementation of a 500 kVAr Hybrid Power Factor/Current Unbalance Compensator

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Date: December 12, 2007

This thesis submitted in fulfillment of the requirements of the degree of Masters of Science in Electrical Engineering at the University of Cape Town.

## Declaration

I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own.

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Date: 29/12/2007

Christopher Goldschmidt

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## Acknowledgements

I would like to thank the following people who have helped me throughout the course of this thesis:

Mr Michel Malengret, my thesis supervisor, for his wisdom and guidance.

Mr Martin Becker for his invaluable assistance in all aspects of this project.

The entire MLT Drives CC. team for their support of the DSP and interface boards and the programming thereof.

My friends and family for their constant support and encouragement.

University of Cape Town

## Synopsis

The goal of this thesis project was to design, build and test a 500 kVA<sup>r</sup> hybrid power factor/current unbalance correction unit. The unit will be used to reduce the maximum demand and reactive power consumption through power factor correction of large electricity users as well as minimize power disruption and improve power quality through unbalance correction.

Through literature research, it was discovered that a particular combination of delta and wye connected capacitors exist for a particular unbalanced load that result in a reduction of unbalance (given enough load inductance). Simulation of the proposed compensator topology allowed for the verification of this and an appropriate control strategy could be developed. Simulations also revealed the average portion of available capacitors that would be required for each of the delta and wye connected filters.

Once the hardware design that was tested in simulation was manufactured, controller boards hosting a powerful digital signal processor and control signals for each of the available capacitor contactors were designed, built and programmed with the control strategy that was developed in simulation.

Failure to locate an appropriate, full scale test site (that would have low consequential losses should power flow be disrupted) resulted in the de-rating of the unit to a one in thirty scale model. This de-rating was achieved by adding in series with each filter additional capacitors to boost filter reactance. This de-rating allowed for the unit to be installed onto a much smaller circuit breaker in a laboratory environment where comprehensive testing was performed.

After confirming that the unit was indeed operating properly as a one in thirty scale model, it was placed into automatic mode and allowed to compensate for unbalanced currents.

Due to the specific combination of phase power levels being consumed by the load, it was simulated that the unit would have an approximate impact on unbalance of 3.5 percent (from 19% to 15.5%). In practice, a reduction in unbalance of 3 percent was achieved.

A financial analysis on the project shows the combination of load sizes with corresponding power factors required for which the project would become financially viable (typically larger loads with very poor lagging power factor).

### **Conclusions:**

It was concluded that the unit was a success and met its required specifications. The cost of manufacture of the unit was minimized through the alteration of a pre-existing power factor correction unit. Given enough load inductance, the unit was able to reduce the unbalance of the source currents over several logging periods and all recorded results closely correlated with expectations.

### **Recommendations**

The author recommends that further software be written to enable wireless communication such that remote logging becomes possible. A user-friendly graphical user interface should also be created through which all important variables should be displayed and all system set-points should be settable.

# Table of Contents

<b>Declaration</b> .....	<b>i</b>
<b>Acknowledgements</b> .....	<b>ii</b>
<b>Synopsis</b> .....	<b>iii</b>
<b>Table of Contents</b> .....	<b>v</b>
<b>Table of Figures</b> .....	<b>ix</b>
<b>List of Tables</b> .....	<b>xiii</b>
<b>Glossary</b> .....	<b>xiv</b>
<b>1 Introduction</b> .....	<b>1</b>
1.1 Background.....	1
1.2 Problem Description.....	2
1.3 Thesis Objectives.....	3
1.4 Scope and Limitations.....	3
1.5 Thesis Outline.....	3
<b>2 Unbalance Compensation Techniques</b> .....	<b>6</b>
2.1 Static VAR Compensation.....	7
2.1.1 Basic TCS Structure.....	8
2.1.2 TCS with Modified Structure.....	9
2.2 Adaptive VAR Compensation.....	10
2.2.1 Topology Operation.....	11
2.2.2 AVC Advantages and Disadvantages.....	13
2.3 D-Statcom Compensation.....	14
2.3.1 Topology Operation.....	14
2.3.2 D-Statcom Advantages and Disadvantages.....	15
2.4 Hybrid Static VAR Compensator and Series Active Filter.....	16
2.4.1 Topology operation.....	17
2.4.2 Hybrid SVC Compensator Advantages and Disadvantages.....	18
2.5 Comparative Analysis.....	19
2.5.1 Hybrid Delta-Wye Static VAR Compensator.....	19

2.5.2	<i>Hybrid Delta-Wye SVC Advantages and Disadvantages</i> .....	20
<b>3</b>	<b>Theory Review</b> .....	<b>21</b>
3.1	Unbalance Measurement .....	21
3.2	Unbalance Correction .....	24
3.2.1	<i>Delta Filter Power Transfer</i> .....	24
3.2.2	<i>Wye Filter Power Transfer</i> .....	28
3.2.3	<i>Unbalance Correction Algorithm – Grounded-Wye Connected Load</i> .....	28
3.2.4	<i>Unbalance Correction Algorithm – Non-Grounded Wye or Delta Connected Load</i> .....	32
3.3	Harmonic Amplification .....	34
<b>4</b>	<b>Hardware Design</b> .....	<b>35</b>
4.1	System Overview .....	35
4.2	Hardware Modification .....	37
4.3	Contactors Sizing .....	40
<b>5</b>	<b>Simulation: Current Balancer</b> .....	<b>43</b>
5.1	Capacitor Power Flow Theory .....	43
5.2	Current Balancer Overview .....	45
5.3	Phase Power Calculator .....	45
5.4	Unbalance Level Calculator .....	46
5.5	Unbalance Reduction Algorithm .....	46
5.6	Simulation Results .....	47
5.7	Discrete Current Unbalance Control Algorithm .....	50
5.7.1	<i>Delta Connected Filter:</i> .....	50
5.7.2	<i>Wye Connected Filter:</i> .....	50
5.7.3	<i>Power Factor Correction:</i> .....	51
5.8	Contactors Switching Transients .....	51
<b>6</b>	<b>Financial Analysis</b> .....	<b>54</b>
<b>7</b>	<b>Digital Signal Processor Board</b> .....	<b>59</b>
7.1	Digital Signal Processor .....	59
7.2	Programming the Digital Signal Processor .....	62
7.3	Available DSP Board Peripherals .....	63
<b>8</b>	<b>Multi-Interface Card Design</b> .....	<b>64</b>

8.1	Microcontroller Requirements .....	64
8.1.1	<i>Liquid Crystal Display</i> .....	64
8.1.2	<i>Keypad</i> .....	65
8.1.3	<i>Communications</i> .....	66
8.1.4	<i>Relay and Acknowledge Signals</i> .....	66
8.2	Multi-Interface Board Microcontroller .....	66
8.3	Schematic Design .....	67
8.3.1	<i>Board Power Supply</i> .....	67
8.3.2	<i>Voltage Measurement Signal Conditioning</i> .....	68
8.3.3	<i>Current Measurement Signal Conditioning</i> .....	69
8.3.4	<i>Relay Drive and Acknowledge Signals</i> .....	71
8.3.5	<i>Completed MIC Board</i> .....	73
<b>9</b>	<b>Software Design</b> .....	<b>74</b>
9.1	Set Point and Data Point Definitions .....	74
9.2	MIC PIC Microcontroller Software .....	74
9.2.1	<i>Software Overview</i> .....	75
9.2.2	<i>Keypad Button Press Detection and De-Bounce Software</i> .....	76
9.2.3	<i>LCD Menu Structure Flowchart</i> .....	78
9.2.4	<i>LCD Module Interface and Control</i> .....	80
9.2.5	<i>Output and Input Tables</i> .....	83
9.2.6	<i>System Faults, Fault Conditions and Fault Handling</i> .....	83
9.2.7	<i>Emergency Stop</i> .....	85
9.3	DSP Controller Software .....	86
9.3.1	<i>DSP Software Overview</i> .....	86
9.3.2	<i>System Timing</i> .....	87
9.3.3	<i>USART Communications and Protocol</i> .....	89
9.3.4	<i>Analogue to Digital Converter</i> .....	90
9.3.5	<i>Unbalance Measurement</i> .....	92
9.3.6	<i>Main Control Algorithm</i> .....	94
<b>10</b>	<b>Laboratory Setup</b> .....	<b>95</b>
10.1	Hybrid System De-Rating .....	95
10.2	Current Transformer Setup .....	98
10.2.1	<i>Source Current Transformers</i> .....	100

10.2.2	<i>Unit Current Transformers</i> .....	101
10.3	<i>System Calibration</i> .....	102
<b>11</b>	<b>Laboratory Results</b> .....	<b>103</b>
11.1	<i>Initial Test Results</i> .....	103
11.1.1	<i>System De-rating</i> .....	103
11.1.2	<i>System Power Flow</i> .....	104
11.1.3	<i>LCD Display Signal Filter</i> .....	105
11.2	<i>Harmonic Impact on the Utility Grid</i> .....	107
11.2.1	<i>Uncompensated Utility Grid Voltage and Current Waveforms</i> .....	107
11.2.2	<i>Impact of Full Power Factor Correction</i> .....	109
11.2.3	<i>Impact of Full Delta Filter Compensation</i> .....	111
11.2.4	<i>Impact of Full Wye Compensation</i> .....	112
11.3	<i>Contactors Testing</i> .....	114
11.3.1	<i>Auxiliary Timing</i> .....	114
11.3.2	<i>Current Waveform Transients</i> .....	116
11.4	<i>Impact on Unbalanced Currents</i> .....	119
11.4.1	<i>Source and Load Current Waveform Comparison</i> .....	119
11.4.2	<i>Analysis of Unbalance Estimation Algorithm</i> .....	125
<b>12</b>	<b>Conclusions</b> .....	<b>129</b>
<b>13</b>	<b>Recommendations</b> .....	<b>131</b>
	<b>References</b> .....	<b>132</b>
	<b>Appendices</b> .....	<b>135</b>

## Table of Figures

Figure 1: Basic Compensator Scheme.....	6
Figure 2: Static VAr Compensation .....	7
Figure 3: Basic TCS Structure.....	8
Figure 4: TCS with Modified Structure (3) .....	9
Figure 5: Adaptive Var Compensator (5).....	10
Figure 6: Waveform - Capacitor Voltage of AVC Topology .....	12
Figure 7: Waveform - Capacitor Current of AVC Topology .....	12
Figure 8: D-Statcom Compensator (6) .....	14
Figure 9: Single Line Diagram - Hybrid SVC Compensator (8) .....	16
Figure 10: Hybrid SVC Compensator - SVC Filters (8) .....	17
Figure 11: Hybrid SVC Compensator - Active Filter (8).....	18
Figure 12: Hybrid Delta-Wye SVC Compensator .....	20
Figure 13: Vector Diagram Illustrating Space-Vector Construction .....	21
Figure 14: Vector Diagram - Sequence Decomposition .....	23
Figure 15: Vector Diagram of a Line to Line Capacitor .....	25
Figure 16: Capacitor Power Equation Flowchart.....	31
Figure 17: Power Factor Correction with Wye Connected Capacitors.....	32
Figure 18: Delta Connection of a Wye connected Capacitor bank (non-grounded) ..	33
Figure 19: Hardware - Proposed Modifications .....	36
Figure 20: Photo - Rewired 50 kVAr delta Capacitor Bank (Bank 4) .....	37
Figure 21: Photo - Rewired 100 kVAr Delta Capacitor Bank (Bank 5) .....	38
Figure 22: Photo - Rewired 100 kVAr Wye Capacitor Bank (Bank 8).....	38
Figure 23: Photo - Rewired 2 x 50 kVAr Wye Capacitor Banks (Banks 6 & 7).....	39
Figure 24: Simulation Schematic - Power Flow Through a Capacitor .....	43
Figure 25: Simulation Waveform - Capacitor Current Versus Line Voltage.....	43
Figure 26: Simulation Waveform - Capacitor Current Versus Line to Neutral Voltages .....	44
Figure 27: Simulation - Current Balancer .....	45
Figure 28: Phase Real and Imaginary Power Calculator.....	45
Figure 29: Simulation - Unbalance Calculator.....	46
Figure 30: Simulation - Unbalance Control Algorithm Function Block .....	46

Figure 31: Simulation - Maximum Reducible Unbalance Versus Load Size.....	49
Figure 32: Photo - Contactor with Auxiliary Resistor Wires.....	52
Figure 33: Simulation - Contactor Switch-in without Auxiliary Resistive Wires.....	52
Figure 34: Waveform - Current Transient without Resistive Wires.....	52
Figure 35: Schematic - Contactor Switch-in with Resistive Wires.....	53
Figure 36: Waveform - Current Transient with Resistive Wires.....	53
Figure 37: Graph - Excess Imaginary Power of Several Load Sizes Versus Power Factor.....	55
Figure 38: Graph - Available Imaginary Power Compensation of Several Load Sizes Versus Power Factor.....	55
Figure 39: Graph - Monthly Savings Due to Power Factor Correction Versus Power Factor.....	56
Figure 40: Graph - Months to Break-Even Versus Power Factor.....	57
Figure 41: Graph - Project Annuity Present Value Versus Power Factor.....	58
Figure 42: Photo - DSP Board, Top Side.....	60
Figure 43: Photo - DSP Board, Bottom Side.....	60
Figure 44: Schematic – Inter-board Connectors.....	61
Figure 45: Photo - Liquid Crystal Display.....	65
Figure 46: Photo - Keypad.....	65
Figure 47: Schematic - LC Filtering of 12V Power Signal.....	67
Figure 48: Schematic - LC Filtering of -12V Power Signal.....	67
Figure 49: Schematic - Conditioning of +3.3V Power Signal from +5V Power Signal.....	67
Figure 50: Schematic - 1.5 Volt Offset Supply.....	68
Figure 51: Schematic - Voltage Signal Conditioning Circuitry.....	68
Figure 52: Schematic - Current Measurement Signal Conditioning.....	70
Figure 53: Schematic - Level Shifter for Relay Drive Signals.....	72
Figure 54: Photo - Completed Interface Board.....	73
Figure 55: Flowchart - PIC Software Overview.....	75
Figure 56: Flowchart - Keypad Button Detection and De-Bounce.....	77
Figure 57: Flowchart - Menu Structure Diagram for LCD Screen.....	78
Figure 58: Flowchart - LCD Screen Set point Editor.....	79
Figure 59: Flowchart - LCD Initialization.....	81
Figure 61: ASCII table for LCD Characters.....	82

Figure 60: Flowchart - Writing Characters to LCD Module .....	82
Figure 62: Flowchart - DSP Software Overview .....	86
Figure 63: Phase Locked Loop Block Diagram (23) .....	87
Figure 64: DSP System Clock and PLL Block Diagram (24) .....	88
Figure 65: Block Diagram - ADC Clock Chain (26) .....	90
Figure 66: Flowchart - ADC Sampling .....	91
Figure 67: Flowchart - RMS Calculations .....	92
Figure 68: Flowchart - Main Control Algorithm .....	94
Figure 69: Photo - Additional De-rating Capacitor Banks .....	97
Figure 70: Photo - Connection of Additional Capacitors, Discharge Resistors .....	97
Figure 71: Photo - Completed Installation .....	98
Figure 72: System Overview - Current Transformer Placement .....	98
Figure 73: System Overview - New Current Transformer Placement .....	99
Figure 74: Photo - Main Distribution Board: Source Current Transformers .....	100
Figure 75: Photo - Unit Current Transformers .....	101
Figure 76: Photo - LCD Module Signal Filter .....	106
Figure 77: Oscilloscope Trace - Natural Grid Voltage and Current Waveforms .....	107
Figure 78: Harmonic Composition of the Natural Grid Voltages .....	108
Figure 79: Harmonic Composition of the Natural Grid Currents .....	108
Figure 80: Utility Grid Voltage and Current Waveform under Full Power Factor Correction .....	109
Figure 81: Voltage Waveform Harmonic Content under Full Power Factor Correction .....	109
Figure 82: Current Waveform Harmonic Content under Full Power Factor Correction .....	110
Figure 83: Utility Grid Voltage and Current Waveforms under Full Delta Compensation .....	111
Figure 84: Voltage Waveform Harmonic Content under Full Delta Compensation .....	111
Figure 85: Current Waveform Harmonic Content under Full Delta Compensation .....	112
Figure 86: Oscilloscope Trace - Grid Voltage and Current Waveforms with 22 kVAr Wye Filter .....	112
Figure 87: Voltage Waveform Harmonic Content under Full Wye Compensation .....	113
Figure 88: Current Waveform Harmonic Content under Full Wye Compensation .....	113
Figure 89: Schematic - Contactor Test Setup (9) .....	114

Figure 90: Waveform - Contactor Test 1(9).....	114
Figure 91: Waveform – Contactor Test 2 (9).....	115
Figure 92: Waveform - Contactor Test 3 (9).....	115
Figure 93: Schematic - Current Transient Test Setup (9).....	116
Figure 94: Waveform - Current Transient 1 (9) .....	116
Figure 95: Waveform - Current Transient 2 (9) .....	117
Figure 96: Waveform - Current Transient 3 (9) .....	117
Figure 97: Waveform - Current Transient 4 (9) .....	117
Figure 98: Graph - Load Side Currents .....	120
Figure 99: Graph - Supply Side Currents .....	120
Figure 100: Graph - Load Side Apparent Power .....	121
Figure 101: Graph - Supply Side Apparent Power .....	121
Figure 102: Graph - Load Side Real Power .....	122
Figure 103: Graph - Supply Side Real Power .....	122
Figure 104: Graph - Load Side Reactive Power.....	123
Figure 105: Graph - Supply Side Reactive Power.....	123
Figure 106: Graph - Wye Filter Switching Pattern .....	124
Figure 107: Graph - Delta Filter Switching Pattern.....	124
Figure 108: Graph - Unbalance Levels (Proper Definition).....	125
Figure 109: Graph - Unbalance Levels (NEMA Definition).....	126
Figure 110: Graph - Unbalance Levels (Standard Deviation from the Mean).....	127
Figure 111: Graph - Simulation of Impact on Unbalance Level .....	127

## List of Tables

Table 1: Capacitor Bank Powers and Functions .....	42
Table 2: Comparison Between Current Unbalance Theory and Simulation .....	44
Table 3: Simulation - Zero Inductance Load .....	47
Table 4: Simulation – Inductance Starved Load .....	47
Table 5: Simulation - Fully Balanced Load .....	48
Table 6: Simulation - Maximum Unbalance Power .....	48
Table 7: Simulation - Maximum Reducible Unbalance versus Load Size .....	49
Table 8: DSP Inter-board Connectors and Their Functions .....	62
Table 9: LCD Module Pin-outs .....	80
Table 10: Comparison of Expected and Actual Current Flow .....	103
Table 11: Impact of Wye Connected Filters on Imaginary Power Flow .....	104
Table 12: Impact of Delta Connected Filters on Real Power Flow .....	104
Table 13: Impact of Delta Connected Filters on Reactive Power Flow .....	105

## Glossary

(x)	: Refer to Reference 'x'
AC	: Alternating Current
ADC	: Analogue to Digital Converter
APV	: Annuity Present Value
AVC	: Adaptive VAr Compensator
DAC	: Digital to Analogue Converter
DC	: Direct Current
DP	: Data Point
DSP	: Digital Signal Processor
GSM	: Global System for Mobile Communication
Hz	: Hertz
IO	: Input-Output
JTAG	: Joint Test Action Group
kA	: Kilo-Amperes
kHz	: Thousands of Hertz
kW	: Kilo-Watts
LCD	: Liquid Crystal Display
MIC	: Multi-Interface Card
MSPS	: Mega Samples Per Second
PCB	: Printed Circuit Board
PIC	: PIC Microcontroller
RAM	: Random Access Memory
RMS	: Root Mean Square
SP	: Set Point
TCS	: Thyristor Controlled Susceptance
Wi-Fi	: Wireless Fidelity

# 1 Introduction

## 1.1 Background

Reactive power compensation, also known as power factor correction, is a widely used tool for reducing an electricity utility bill for large electricity users. A typical industrial installation will have a power factor correction unit that measures the power factor of a reference phase and injects enough capacitive power to compensate for the load's inductive nature. Because the typical power factor correction unit compensates for the reactive power on one reference phase only, it is assumed by the manufacturer that the other phases are transferring an approximately equal amount of inductive reactive power. However, should the load not be fully balanced, it is possible for the power factor correction unit to be overcompensating on the unmeasured phases, thus increasing the utility bill once again.

Current unbalance compensation has typically received little attention by industries, since the consequences of drawing unbalanced currents from the utility grid are often not directly seen. However, a heavily unbalanced load does introduce some problems when consuming electricity that may have a devastating effect on an electricity system. The first effect commonly cited is the induction of a voltage unbalance. Voltage unbalance is a by-product of current unbalance since all electricity sources have a source impedance, over which a voltage drop is seen. If one phase conducts more current than the other phases, then that phase will be subject to a larger voltage drop, resulting in unbalanced voltages on the load side. The main issue caused by voltage unbalance is seen in induction machines, where the machine is de-rated according to the level of voltage unbalance. The machine must be de-rated since a negative sequence component introduced into the voltage phasor produces an equivalent reverse torque on the rotor. Failure to de-rate an induction machine under unbalanced conditions can easily lead to machine failure.

The second problem caused by current unbalance is seen when a consumer is

operating near the limit of their supply side circuit breaker: where a slight increase in current consumption on one phase may cause the breaker to trip. Under more severe current unbalance situations, it is possible for the user to consume power well below the rated power limit and yet draw enough current on one phase to trip the supply side breaker. This may cause unnecessary and expensive power outages resulting in significant loss of data, production and revenue.

The main cause of current unbalance is the unequal loading of the three phase utility grid where more load is placed on one phase. Large loads such as arc welders and furnaces may also be the root of a current unbalance problem and must be accounted for when designing distribution boards. It should also be noted that although electricity producers rely on the average consumption of an area to be equal over all three phases, some place a limit on the maximum unbalance that may be drawn by an individual load. For South Africa, Eskom places a limit of 15 kVA on power consumption unbalance, which may not be exceeded (1).

This thesis project was instigated by Mr. Michel Malengret, lecturer at the University of Cape Town in conjunction with an industrial partner.

## 1.2 Problem Description

Current unbalance may be alleviated by the insertion of reactive elements (capacitors and inductors) into the utility grid at the load side. However, because reactive elements contribute to the amount of reactive power drawn by the load, the load's power factor will be influenced by the amount of current unbalance compensation that is taking place. Because the power factor of a load can significantly influence the utility bill received at the end of each month by the electricity user, it makes sense to create a hybrid unit that achieves both power factor correction as well as current unbalance compensation and will find the optimum balance between the compensation of both factors so as to present a balanced load to the supply. One restraint placed on this hybrid system is that it must be cheap as well as reliable, since it is being installed into an industrial load where profits are key.

### 1.3 Thesis Objectives

The objectives of this thesis project are, in accordance with section 1.2, as follows:

- Research current unbalance compensation techniques and perform a comparison.
- Simulate the proposed compensator to ensure correct topology operation.
- Design and build a hybrid power factor correction/current unbalance compensator proto-type with a reactive power of approximately 500 kVAr.
- Ensure that any possible design is robust in nature.
- Ensure that any possible design is built as cost effectively as possible.
- Perform laboratory testing on the impact of the system on source power transfer.
- Draw conclusions and make recommendations about the operation of the system and its topology.

### 1.4 Scope and Limitations

The scope of this thesis project is limited to the design and implementation of a hybrid power factor/current unbalance compensator. No attention will be paid to voltage unbalance as it is assumed for the DSP algorithms that all voltages are fully balanced.

### 1.5 Thesis Outline

This thesis is outlined as follows:

Chapter 2 details the existing possible compensator techniques discovered during the literature review process and lists the advantages and disadvantages of each topology. A final topology is then discussed and reviewed.

Chapter 3 examines the theory of the operation of the final topology discussed in

chapter 2 and a control strategy for that topology is created.

Chapter 4 details the practical hardware design of the compensator unit and shows calculations that examine the required filter rated current and the resulting selection of components to produce the desired topology.

Chapter 5 covers an in-depth simulation of all major aspects of the unit. Firstly, a comparison is made for each filter type with regard to current flow such that the theory covered in chapter 3 is verified to be correct. Next, a measure of unbalance is discussed and implemented in software in the simulation package such that the influence of each filter type of the source unbalance can be seen. An algorithm is then created in software that determines the correct filter combination required to reduce unbalance.

Chapter 6 examines the financial viability of the project subject to the size and original power factor of the load under scrutiny. A graph of project net present value versus load size and power factor is created.

Chapter 7 details the digital signal processor controller board and its available peripherals and programming method.

Chapter 8 shows the design and implementation of an appropriate interface board for the digital signal processor board mentioned in chapter 7. Peripheral choice and design as well as some schematic design is given.

Chapter 9 covers the software design of both the DSP and interface boards. Flowcharts detail various critical software procedures and processor timing is also analyzed.

Chapter 10 details the installation of the unit onto a test load in a laboratory environment. Various de-rating issues are explained along with appropriate calculations and photographs.

Chapter 11 gives results obtained from laboratory testing. Current flow from each filter is measured to ensure that it complies with rated current and the impact of each filter type on the utility grid is tabulated and compared to the theoretical and simulated impact. Various difficulties and their solution encountered during the testing procedure are discussed before the unit is allowed to run under fully automatic mode. Trend graphs of all relevant variables are given.

Chapters 12 and 13 list the author's conclusions based on the findings and list recommendations based on those conclusions for future work to be done on this project.

## 2 Unbalance Compensation Techniques

There are a multitude of current unbalance compensation techniques that have been tested to date, all with varying degrees of complexity and cost. However, all compensators operate according to the same basic principle to physically reduce unbalanced currents thereby creating the effect that the source sees a fully balanced load at near unity power factor. This principle is outlined in (2), where currents are injected into the utility grid in parallel with the load in such a way as to reduce the unbalance as seen by the source, see Figure 1.

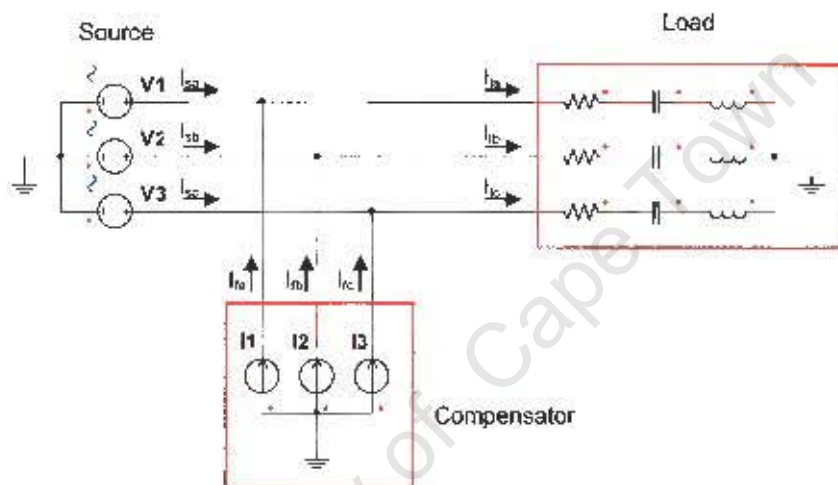


Figure 1: Basic Compensator Scheme

The objective of the basic compensator is thus to inject currents  $I_{fa}$ ,  $I_{fb}$ ,  $I_{fc}$ , (calculated from currents  $I_{la}$ ,  $I_{lb}$ ,  $I_{lc}$ ) such that all currents  $I_{sa}$ ,  $I_{sb}$ ,  $I_{sc}$  are of equal magnitude and transfer purely real power. It is shown in (2) that the reference currents generated by the compensator may be calculated with the following formulae:

$$i_{fa} = i_{la} - \frac{V_{sa} + (V_{sb} - V_{sc})\beta}{|A|} P_{lav} \quad (2-1)$$

$$i_{fb} = i_{lb} - \frac{V_{sb} + (V_{sc} - V_{sa})\beta}{|A|} P_{lav} \quad (2-2)$$

$$i_{fc} = i_{lc} - \frac{V_{sc} + (V_{sa} - V_{sb})\beta}{|A|} P_{lav} \quad (2-3)$$

Where  $|A| = V_{sa}^2 + V_{sb}^2 + V_{sc}^2$  and  $P_{lav} = V_{sa}i_{sa} + V_{sb}i_{sb} + V_{sc}i_{sc}$

Also  $\beta = \tan\phi/\sqrt{3}$  where  $\phi$  is the phase angle

It should be noted that Figure 1 depicts a grounded wye connection, in which neutral

currents may flow prior to unbalance compensation. However, should the load be connected in a delta format, the format of the compensator remains the same (however, no neutral connection is required) (2).

## 2.1 Static VAR Compensation

It is explained in section 3.2.1 that both real and imaginary power can be induced to flow through a susceptance if two sinusoidal waveforms of differing phase are placed across the susceptance. For this reason, the most basic of compensation techniques is to place a combination of inductors and capacitors across the three phases such that the appropriate compensation currents are generated. This method of compensation is detailed in (3) and is generalized for a three phase, three wire system as shown below:

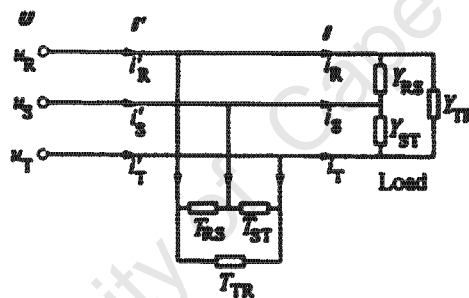


Figure 2: Static VAR Compensation

This basic type of compensator consists of fixed capacitor and inductor values, calculated as detailed in (3), where the load current is decomposed into four components; active, harmonic, reactive and unbalanced. Compensation is thus required for the reactive, unbalanced and harmonic currents to provide a perfect load as seen by the source. However, typically, reactors as shown above increase third order harmonics thereby allowing only for the compensation of the unbalanced and reactive currents (3). The above topology may thus be summarized as shown below:

### Advantages:

- Simple topology, little design required.
- Low cost components, none of which are easily damaged.

- Simple solution to reactor values as detailed in (3).

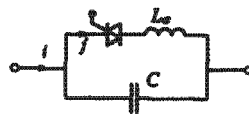
**Disadvantages:**

- Compensator may only compensate for a fixed unbalanced load.
- Possible resonance between the compensator and the source inductance.
- Cannot compensate for zero sequence currents – will not be as effective for three phase, four wire loads.
- Injection of third order harmonics into the utility grid (3).
- May only perform three phase power factor correction (average of three phases).

It should be noted that in (4) it is suggested that for the compensator to be able to reduce zero sequence currents (generated in an unbalanced three phase, four wire system), the load must first be separated by a delta-wye grounded transformer. In this way, all zero sequence currents are blocked and the compensator structure remains intact.

**2.1.1 Basic TCS Structure**

For a dynamically changing load, the compensator susceptances must also change accordingly for system balance to be maintained. For this purpose, the TCS (Thyristor controlled susceptances) structure is proposed in (3) below where each branch of the compensator is replaced with the following topology:



*Figure 3: Basic TCS Structure*

In the TCS topology, the firing angle of the triac is adjusted to adjust the susceptance seen at the branch terminals. Thus the values of  $C$  and  $L_c$  are chosen to match the range of the dynamically varying load, such that an in depth load analysis must first be performed to determine the range of powers consumed. Often, due to the

generally inductive nature of most loads, the inductor will only be used to de-rate the capacitor's influence of the circuit, but may, if the load requires it, be large enough to provide an inductive susceptance to the load.

"The basic structure of the TSC has two main disadvantages. The shunt capacitor  $C$  may form a parallel resonance circuit with the supply source inductance for the current harmonics generated by thyristors. As a consequence, the distortion of the TCS current may be even higher than the distortion of the TSI (Thyristor switched inductor) current (3)." "The second disadvantage of the basic structure may appear only if the supply voltage is distorted. Namely, a strong distortion of the supply current may occur as a consequence of the series resonance of the compensator capacitor with the supply source inductance (3)."

### 2.1.2 TCS with Modified Structure

"Due to the high distortion of the supply current, a balancing compensator built of TCS with the basic structure may supersede the asymmetry of the supply current for the current distortion, with probably even much more harmful effects than the current asymmetry. A substantial reduction in the waveform distortion is necessary for a satisfactory performance of the balancing compensator. The TCS should attenuate current harmonics generated by the switched inductor. Moreover, it cannot be so sensitive to the supply voltage harmonics as the TCS with the basic structure (3)." To overcome the above mentioned problems, the TCS with modified structure is then proposed:

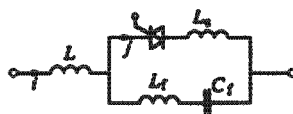


Figure 4: TCS with Modified Structure (3)

The TSC with modified structure "contains a shunt  $L_f C_f$  filter tuned to the third-order harmonic and an additional series inductor  $L$ . The filter provides a low impedance path for the third-order current harmonics generated by the TSI (Thyristor switched

inductor). The series inductor increases compensator impedance for the supply voltage harmonics (3)."

The TSC with modified structure may be summarized as follows:

Advantages:

- Simple solution to reactor values as detailed in (3).
- Reduced possibility of resonance with supply side inductance.
- Exact compensation may be achieved within the compensator's bounds.
- Reduction in generation of third-order harmonics.

Disadvantages:

- Complex topology, many components required.
- Design is less robust with the addition of solid state switches.
- Expensive switches and control hardware required.
- More complicated switching scheme required.
- Heat dissipation is required.
- May not compensate for inductive power on a single phase only.

## 2.2 Adaptive VAR Compensation

The operating principle of the adaptive VAR compensator from (5) is in line with the basic compensation principle shown in Figure 1, where a combination of injected currents work to balance the load as seen from the source; however some slight topology changes may be seen:

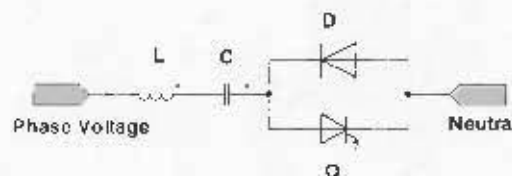


Figure 5: Adaptive Var Compensator (5)

Figure 5 shows one branch of a three phase filter, where the branch current produces one reference/compensating current.

### **2.2.1 Topology Operation**

During the positive half cycle of the phase voltage, the thyristor, Q, is off whilst the diode, D, is reversed biased thereby preventing current flow through the circuit. However, as the phase voltage goes into its negative half cycle, diode 'D' is now forward biased and allows current to flow from the neutral connection into the capacitor 'C'. This continues until the voltage waveform has reached maximum negative amplitude and the diode becomes reversed biased again. This process allows for the pre-charging of the capacitor such that the capacitor always remains at the peak amplitude of the phase voltage until the thyristor is switched.

The driving signal to each thyristor gate is now synchronized to the reference grid voltage such that the thyristor is only switched when the phase voltage is at its maximum negative voltage. This voltage corresponds to the natural zero phase current of a capacitor since the current through a capacitor always leads the phase voltage by 90 degrees. Because of this, and because the capacitor was pre-charged to the peak phase voltage, the thyristor now has a zero voltage potential across it whilst simultaneously, the circuit is attempting to conduct zero current. Any switching of the thyristor at this stage would result in a near natural commutation of the thyristor (as if it were a diode) resulting in the introduction of near zero voltage and current harmonics, see Figure 6.

It is worth noting though that because the thyristor may only be switched at one point in the voltage waveform, the inductor-capacitor circuit may not be tuned by an appropriately timed thyristor trigger as is possible in the TCS with modified structure topology laid out in section 2.1.2. Thus the filter may only present one susceptance value to its inputs (to the phase voltage), determined by the combination of 'L' and 'C'.

It should be noted that 'L' is simply a de-tuning inductor to ensure that the filter does not form a possible resonant circuit with the source inductance.

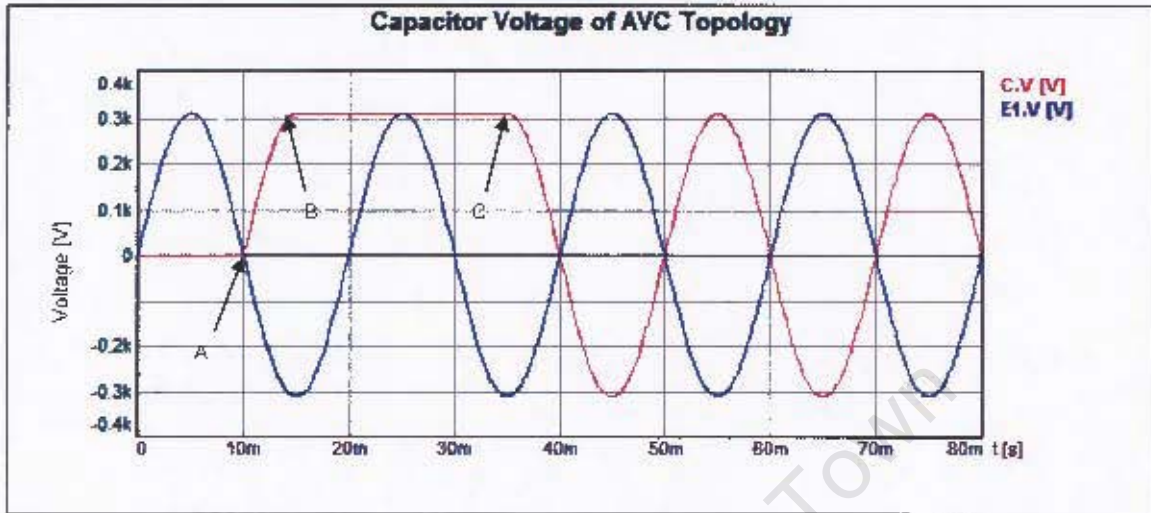


Figure 6: Waveform - Capacitor Voltage of AVC Topology

Figure 6 shows the start of the capacitor pre-charge cycle (point 'A'), the end of the pre-charge cycle (point 'B') and the capacitor voltage at thyristor switching (point 'C'). It can be seen that the capacitor voltage naturally joins the cycle of the phase voltage, thereby introducing zero voltage harmonics.

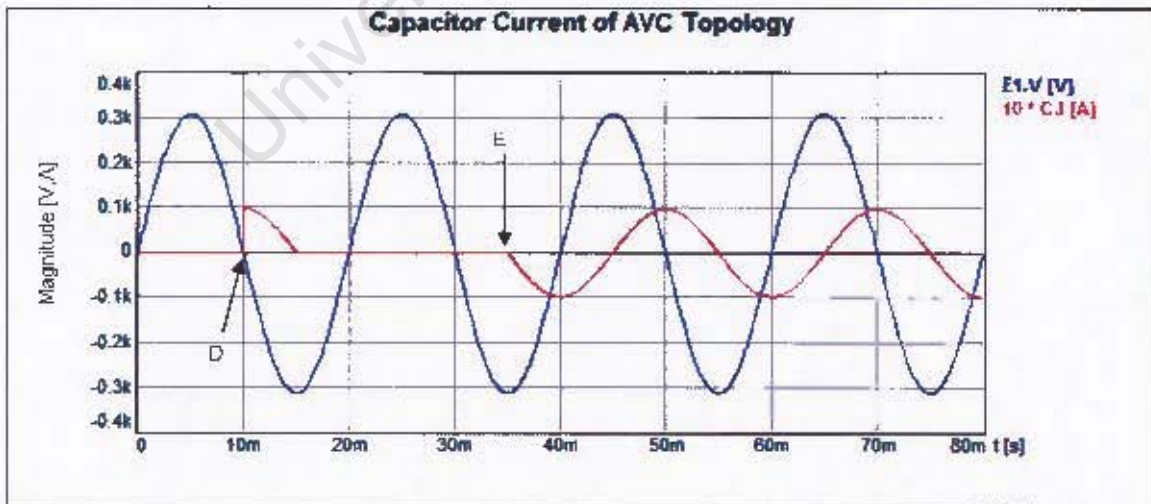


Figure 7: Waveform - Capacitor Current of AVC Topology

Figure 7 shows the current through capacitor 'C' upon pre-charge (point 'D') and thyristor switch (point 'E'). It can be seen that capacitor current begins to flow naturally (sinusoidally from zero) and introduces no harmonics.

### 2.2.2 AVC Advantages and Disadvantages

Each branch of the AVC filter presents a fixed susceptance to the phase source and thus contributes fixed reactive power to the utility grid. Thus, to be able to achieve compensation for a dynamic load, many filter branches are required of differing susceptance such that a combination of which makes up the required total susceptance. Each branch is sized to be double the capacitive power rating of the previous, to maximize total susceptance range. For this reason, the resolution of the system is defined to be half the reactive power of the smallest branch (5).

The AVC may be summarized as follows:

Advantages:

- Reduced possibility of resonance with supply side inductance.
- Zero generation of third-order harmonics.
- Low component stress due to switching strategy.
- Simple Switching scheme.

Disadvantages:

- Many filter branches required, depending on load.
- Design is less robust with the addition of solid state switches.
- Expensive switches and control hardware required.
- Heat dissipation is required.
- May not compensate for inductive power on a single phase only.

## 2.3 D-Statcom Compensation

Reactive power, unbalance and harmonic compensation through the use of a D-Statcom compensator (Distribution Static Compensator) is described in (6), where a three phase inverter is used in conjunction with a DC side capacitor (see Figure 8) to inject the required compensation currents, as described in section 2.

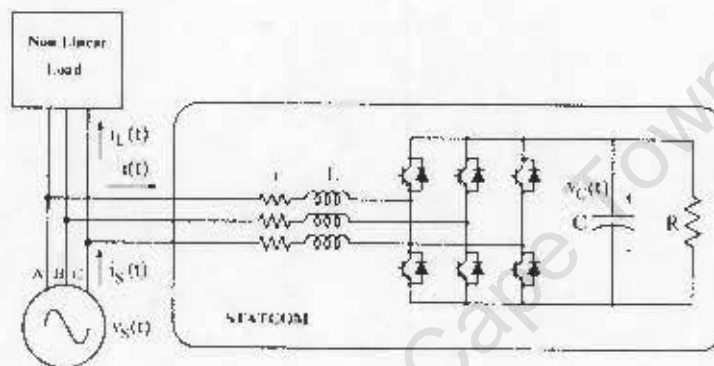


Figure 8: D-Statcom Compensator (6)

### 2.3.1 Topology Operation

Figure 8 shows the topology of the D-Statcom compensator, where a three phase inverter made up of six IGBTs create the required compensation currents  $i(t)$ . The inverter interfaces to the utility grid via inductors  $L$  with parasitic resistance  $r$  such that the phase angle of the inverter may differ slightly from that of the source. In this way, power transfer may be realized by the inverter through the following equations as described in (7) where the power is supplies by the source to the inverter:

$$P = \frac{V_s^2}{\omega L_s} \left( \frac{V_{inv}}{V_s} \sin \delta \right) \quad (2-4)$$

$$Q = \frac{V_s^2}{\omega L_s} \left( 1 - \frac{V_{inv}}{V_s} \cos \delta \right) \quad (2-5)$$

Where  $V_s$  is the source voltage,  $V_{inv}$  is the inverter side voltage,  $L_s$  is the connecting

inductance and  $\delta$  is the angle between source and inverter voltage phasors.

Using purely the inverter and connecting inductance, the system would be able to compensate for all reactive power, since no real power is being transferred by either the source or the inverter (6). This can be verified by examining the above equations, where reactive power absorbed or injected into the source depend only upon the magnitudes of the source and inverter voltages and the phase angle between them. However, because the system must compensate for unbalanced currents as well, where some real power transfer is taking place (from one phase to the next), some energy storage system is required in the form of a capacitor, C. The three phase inverter simultaneously acts as a three phase rectifier when connected to the source, thereby maintaining the capacitor voltage at a constant DC voltage. Note that in this topology the capacitor is not acting as a reactive power source itself, but merely as an energy storage device. Resistor 'R' in Figure 8 represents only the losses in the system. Because the inverter section must act to both inject currents into the utility and as an active rectifier to maintain the DC side capacitor voltage, complicated control algorithms are required to calculate the appropriate switching patterns and ensure correct operation as described in (6).

### **2.3.2 D-Statcom Advantages and Disadvantages**

The D-Statcom compensator may be summarized as follows:

Advantages:

- No possibility of resonance with supply side inductance.
- Precise control over compensation currents.
- Fast compensation.
- Few Components.
- May perform per phase power factor correction

Disadvantages:

- Design is less robust with the addition of solid state switches.
- Expensive switches and control hardware required.

- Harmonics generated by switched inverter.
- Complicated control is required.
- Compensator electrical size limitations due to semi-conductor capabilities.
- Heat dissipation is required.
- Cannot compensate for zero sequence currents as it is a three phase, three wire system.
- Limited power factor correction (current limitations).

## 2.4 Hybrid Static VAR Compensator and Series Active Filter

The topology described in (8) is the most comprehensive topology detailed in this thesis and aims to compensate for all unwanted reactive power, unbalance and harmonic currents for a severely unbalanced, non-linear load. The authors of (8) have proposed a combination of a delta connected SVC, a wye connected SVC and a passive filter with series active filter (see Figure 9 below).

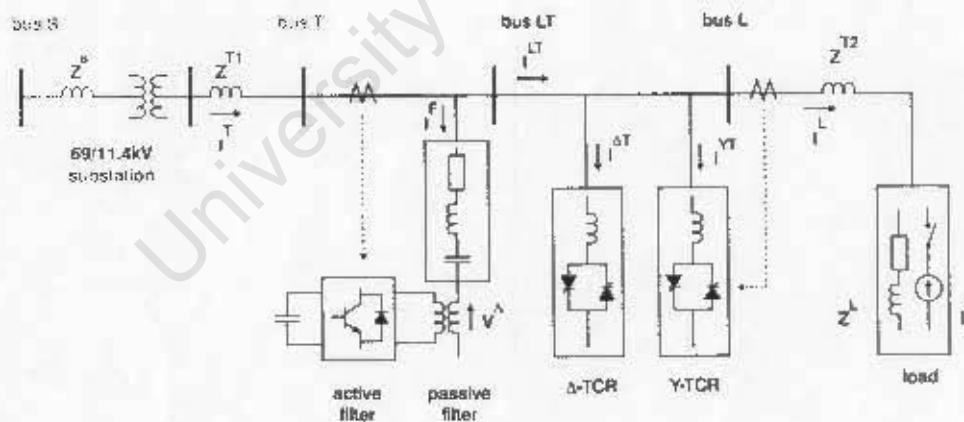


Figure 9. Single Line Diagram - Hybrid SVC Compensator (8)

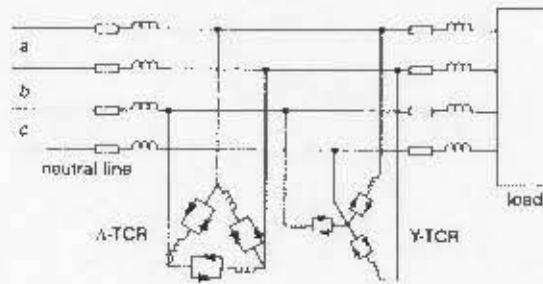


Figure 10. Hybrid SVC Compensator - SVC Filters (8)

### 2.4.1 Topology operation

The hybrid SVC compensator is the first topology to make use of a combination of both delta connected as well as wye connected SVC filters, as shown in Figure 10. Here, the load may be wye or delta connected and may still be compensated for completely by the compensator. The delta connected SVC is used to compensate for the negative phase sequence, or the real unbalanced part of the load current whilst the wye connected SVC compensates for the zero sequence currents (neutral currents) as well as the imaginary part of the positive phase sequence where per phase power factor correction is achieved (8). Each SVC section is made up of a thyristor controlled reactor as well as a de-tuning filter to minimize the introduction of switching harmonics. To further reduce the injection of harmonics into the utility grid, a passive filter is added in a shunt connection and tuned to the harmonic frequencies of the TCRs (8), thereby providing a low impedance path for those harmonics to the neutral connection.

As shown in Figure 9, an active filter is added in series with the shunt passive filter to further improve system performance. "The active filter is operated to present a low fundamental frequency resistance and a high harmonics resistance for the source currents. To appear as a resistor for the source harmonics currents, the output voltages to the active filter should be in phase with the source harmonics currents (8)." Galvanic isolation is also provided for the active filter with the addition of a transformer on each inverter stage as shown in Figure 11 below.

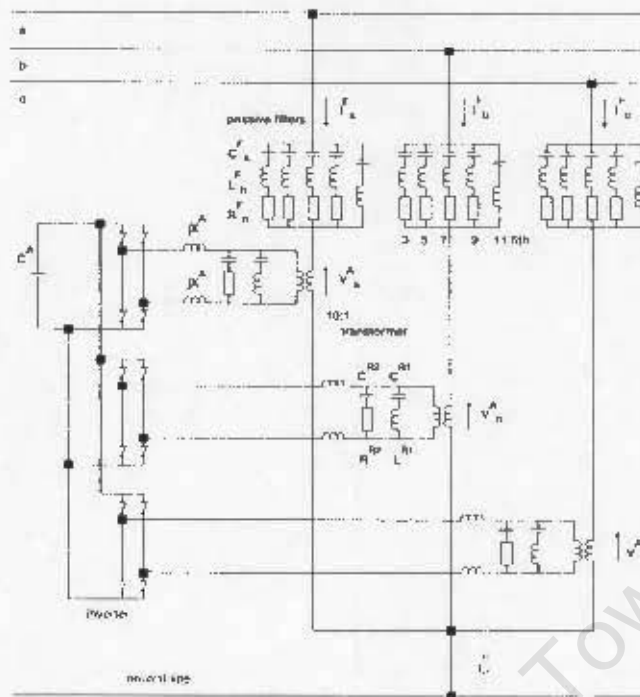


Figure 11: Hybrid SVC Compensator - Active Filter (B)

#### 2.4.2 Hybrid SVC Compensator Advantages and Disadvantages

The hybrid SVC compensator may be summarized as follows:

Advantages:

- Little possibility of resonance with supply side inductance.
- Precise control over compensation currents.
- Fast compensation.
- Full harmonic compensation.
- May compensate for delta and wye connected loads.
- May perform full per phase power factor correction

Disadvantages:

- Design is less robust with the addition of solid state switches.
- Expensive switches and control hardware required.
- Complicated control is required.
- Heat dissipation is required
- Many components, expensive topology.

## 2.5 Comparative Analysis

As explained in section 1.3, the objectives of this thesis is to design, build and test a hybrid system capable of both power factor correction as well as current unbalance compensation. Because this thesis began as a joint project between the University of Cape Town and an industry partner to create a system that may be marketable and sold to industries with current unbalance problems and poor power factor, the system must be a robust and competitively inexpensive product. This places limitations on the complexity and type of components used in the topology of the final system which must be able to compensate for all negative sequence, imaginary positive sequence and zero sequence currents.

For the above reasons, it was suggested by (9) that a delta connected static VAR compensator be used with contactors (in place of thyristors) for cost, but was modified in accordance with the topology suggested in (8) by the author to the topology shown in 2.5.1.

### 2.5.1 Hybrid Delta-Wye Static VAR Compensator

Figure 12 below shows the topology of the hybrid delta-wye static VAR compensator. It consists of two individual filters, a delta connected filter to compensate for the bulk of the imaginary part of the positive phase sequence and the negative phase sequence, and a wye connected filter to compensate for the zero phase sequence as well as the per phase power factor (should phase power factors differ slightly).

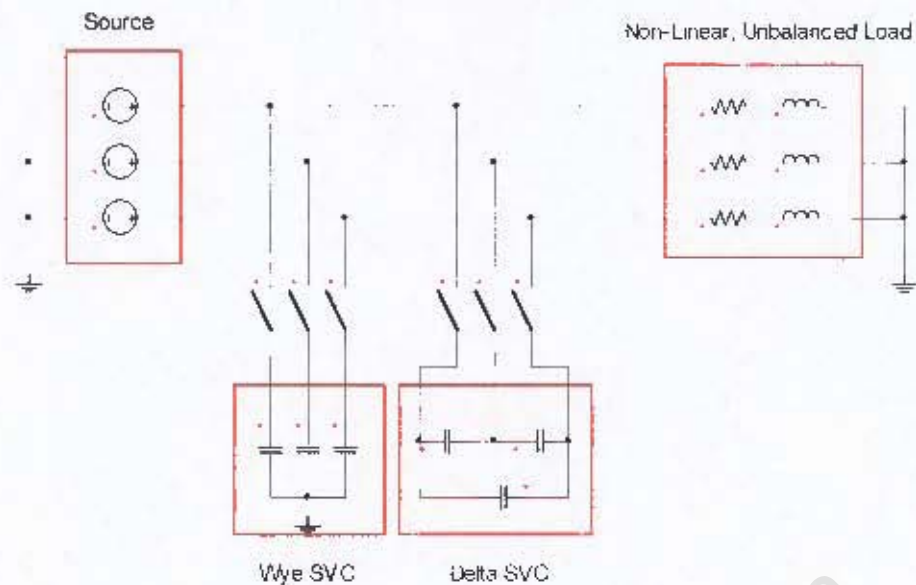


Figure 12: Hybrid Delta-Wye SVC Compensator

### 2.5.2 Hybrid Delta-Wye SVC Advantages and Disadvantages

The hybrid delta-wye svc may be summarized as follows:

Advantages:

- Inexpensive design – few components required.
- Robust design – may withstand utility grid transients
- No heat dissipation required.
- May compensate for both delta and wye connected loads.
- May perform full power factor correction with per phase compensation.
- More basic control strategies will be required with limited control hardware.
- No switching harmonics are generated on a constant basis.

Disadvantages:

- Compensation is step-wise, exact compensation currents may not be achieved.
- Possibility of resonance with supply side inductance.
- Generation of third order harmonics by reactors.
- Slow compensation, will not compensate for harmonics.
- Load must be inductive in nature to compensate for unbalance without creating a leading power factor.

### 3 Theory Review

Before the theory of current unbalance reduction can be examined, it is prudent to examine what current unbalance is comprised of and how it can be measured. As described in Section 1.2, it is assumed for the scope of this thesis that the load is fed by a three phase, four wire supply. This type of connection is the most common connection type to the utility grid, where a large building (factory or shopping center) comprises the load. Because this thesis is dealing with current unbalance, it is also assumed that currents must flow through the neutral conductor, the magnitude of which depends of the level of unbalance. Once the theory for a three phase, four wire system is examined, modifications will then be made for non-grounded wye and delta connected circuits.

#### 3.1 Unbalance Measurement

A useful method of representing a three-phase system (three vectors) is to use space-vector theory, where the instantaneous summation of the three current vectors represent the magnitude of a rotating vector in the stationary reference frame with a frequency equal to the system's voltage frequency (10), see Appendix B. The space vector ( $I_s$ ) is illustrated below where  $\alpha$  represent the real part of the vector and  $j\beta$  represents the imaginary part:

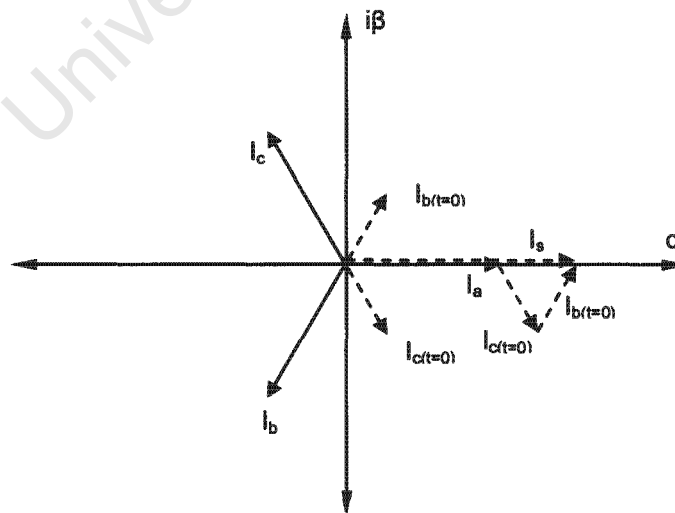


Figure 13: Vector Diagram Illustrating Space-Vector Construction

The effect of the space-vector on the system will thus have the same effect as the three current vectors together and will, in a balanced system, trace out a circle of radius  $|I_s|$  (where  $|I_s| = 1.5 \times I_a$ ) around the vector plane. As unbalance is introduced into the network, and the magnitudes and angles of each phase current changes, so the space-vector magnitude changes as it rotates around the vector plane, thereby tracing out a non-circular trace. The greater the deviation of the trace is from a perfect circle, the greater the level of unbalance present in the network.

A space-vector that has a current unbalance component may be decomposed into three sequences – positive ( $I_+$ ), negative ( $I_-$ ) and zero ( $I_0$ ) (11), see Appendix C. The vector sum of these sequences at any given time therefore makes up the original current system or space-vector.

The positive sequence represents the wanted current sequence, and would comprise the entire current network in the case of a fully balanced system. This current sequence is represented by a rotating vector in the stationary reference frame with a frequency equal to that of the utility grid's voltage frequency (typically 50 Hz).

The negative current sequence represents the current flow that is caused by unequal loading of the voltage source and is represented by a rotating vector in the stationary reference frame with a magnitude that is dependent on the level of load unbalance and a direction opposing the positive sequence vector.

The zero sequence vector is a non-rotating vector in the stationary reference frame that is caused by current flow in the poly-phase neutral conductor. This vector adds a fixed offset to the positive and negative current sequence vectors in the reference frame and is also caused by load unbalance. A vector diagram representing the sequence vectors is given below:

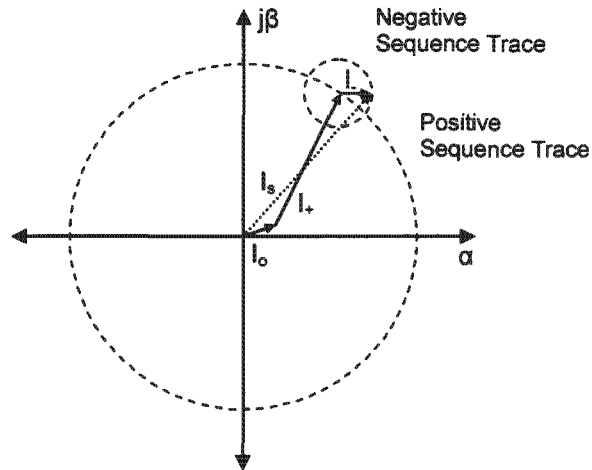


Figure 14: Vector Diagram - Sequence Decomposition

Current Sequences can be calculated from the natural grid currents via the following equations (11):

$$I_0 = \frac{1}{3}(I_a + I_b + I_c) \quad (3-1)$$

$$I_+ = \frac{1}{3}(I_a + \alpha I_b + \alpha^2 I_c) \quad (3-2)$$

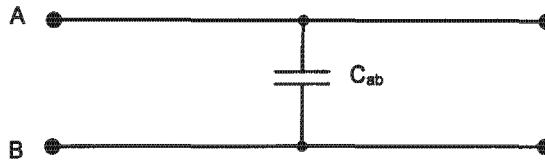
$$I_- = \frac{1}{3}(I_a + \alpha^2 I_b + \alpha I_c) \quad (3-3)$$

where  $\alpha = e^{j(\frac{2\pi}{3})}$

Once all three current sequences are known, a measure for the level of unbalance may be calculated, where the negative and zero sequence form a portion of the positive sequence is required. This can be summarized as shown below:

$$Unbalance [\%] = \frac{I_0 + I_-}{I_+} \times 100 \quad (3-4)$$

constant ( $400 V_{rms L-L}$ ,  $120^\circ$ ). If it is assumed that a capacitor of random capacitive power is placed across two lines each connected to a voltage source of  $230 V_{L-N}$  and a  $120^\circ$  phase angle difference:



The following vector diagram describes the waveforms present in the above setup:

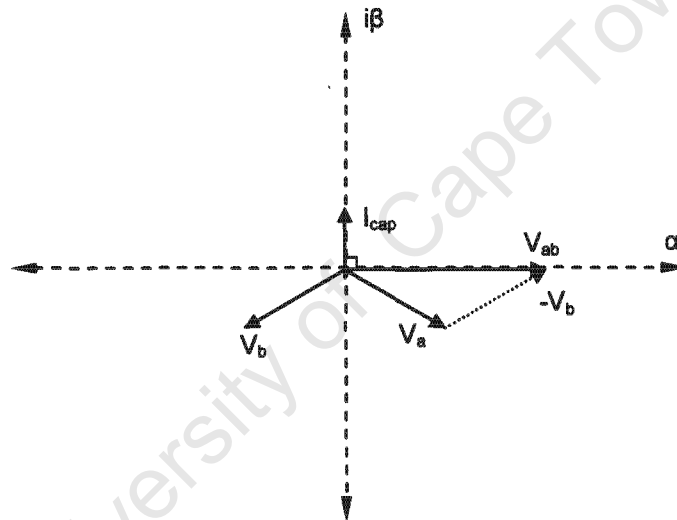


Figure 15: Vector Diagram of a Line to Line Capacitor

It can be seen that line to line voltage,  $V_{ab}$ , induces a current through the capacitor, labeled  $I_{cap}$ . This current leads the phase voltage by  $90^\circ$ , as a purely capacitive load must. However, if the capacitor current is referenced to the phase to neutral voltages, both a real and reactive component is seen in the capacitor current by the line to neutral voltages. This results in both a real and imaginary power transfer by the capacitor. The power flow through the capacitor may be calculated by using the equations described below:

$$P = V_{rms(L-N)} I_{rms} \cos \theta \quad (3-5)$$

$$Q = V_{rms} I_{rms} \sin \theta \quad (3-6)$$

Where 'θ' is the angle between the voltage and current phasors.

Phase 'A' powers:  $P_{cap\_a} = V_{rms} I_{cap} \cos(-120^\circ) = -\frac{1}{2} V_{rms} I_{cap} \quad (3-7)$

$$Q_{cap\_a} = V_{rms} I_{cap} \sin(-120^\circ) = -\frac{\sqrt{3}}{2} V_{rms} I_{cap} \quad (3-8)$$

Phase 'B' powers:  $P_{cap\_b} = V_{rms} I_{cap} \cos(120^\circ) = -\frac{1}{2} V_{rms} I_{cap} \quad (3-9)$

$$Q_{cap\_b} = V_{rms} I_{cap} \sin(120^\circ) = \frac{\sqrt{3}}{2} V_{rms} I_{cap} \quad (3-10)$$

Also:  $I_{cap} = \frac{P_{cap}}{V_{L-L}} = \frac{P_{cap}}{\sqrt{3}V_{L-N}} \quad (3-11)$

Thus:  $P_{cap\_a} = -\frac{1}{2} |V_{L-N}| \frac{P_{cap}}{\sqrt{3}|V_{L-N}|} = -\frac{1}{2\sqrt{3}} P_{cap} \quad (3-12)$

$$Q_{cap\_a} = -\frac{\sqrt{3}}{2} |V_{L-N}| \frac{P_{cap}}{\sqrt{3}|V_{L-N}|} = -\frac{1}{2} P_{cap} \quad (3-13)$$

$$P_{cap\_b} = -\frac{1}{2} |V_{L-N}| \frac{P_{cap}}{\sqrt{3}|V_{L-N}|} = -\frac{1}{2\sqrt{3}} P_{cap} \quad (3-14)$$

$$Q_{cap\_b} = \frac{\sqrt{3}}{2} |V_{L-N}| \frac{P_{cap}}{\sqrt{3}|V_{L-N}|} = \frac{1}{2} P_{cap} \quad (3-15)$$

Because the capacitor current lags phase 'B' and leads phase 'A', a power flow is seen from phase 'B' to phase 'A'. This means that power from phase 'B' can supplement some of the power requirements of the phase 'A' load, thereby reducing the load as seen from phase 'A'. From the perspective of phase 'B', real power is being supplied, whilst reactive power is being absorbed, equivalent to adding the negative  $P_{cap\_b}$  and negative  $Q_{cap\_b}$  powers to the load, seen by the source on phase 'B'. In the two phase situation described above, the power drawn from the source ( $P_a, Q_a, P_b, Q_b$ ) can be written in terms of the power drawn from the load ( $P_x, Q_x, P_y,$

$Q_y$ ) and the power of the capacitor added between the two phases.

$$P_a = P_x - \frac{1}{2\sqrt{3}} P_{cap\_ab} \quad (3-16)$$

$$Q_a = Q_x - \frac{1}{2} P_{cap\_ab} \quad (3-17)$$

$$P_b = P_y + \frac{1}{2\sqrt{3}} P_{cap\_ab} \quad (3-18)$$

$$Q_b = Q_y - \frac{1}{2} P_{cap\_ab} \quad (3-19)$$

In the three phase situation with phases A,B and C being  $120^\circ$  apart with source powers ( $P_a, Q_a, P_b, Q_b, P_c, Q_c$ ) and load powers ( $P_x, Q_x, P_y, Q_y, P_z, Q_z$ ), the above equations can be extended as follows:

$$P_a = P_x - \frac{1}{2\sqrt{3}} P_{cap\_ab} + \frac{1}{2\sqrt{3}} P_{cap\_ca} \quad (3-20)$$

$$Q_a = Q_x - \frac{1}{2} P_{cap\_ab} - \frac{1}{2} P_{cap\_ca} \quad (3-21)$$

$$P_b = P_y - \frac{1}{2\sqrt{3}} P_{cap\_bc} + \frac{1}{2\sqrt{3}} P_{cap\_ab} \quad (3-22)$$

$$Q_b = Q_y - \frac{1}{2} P_{cap\_bc} - \frac{1}{2} P_{cap\_ab} \quad (3-23)$$

$$P_c = P_z - \frac{1}{2\sqrt{3}} P_{cap\_ca} + \frac{1}{2\sqrt{3}} P_{cap\_bc} \quad (3-24)$$

$$Q_c = Q_z - \frac{1}{2} P_{cap\_ca} - \frac{1}{2} P_{cap\_bc} \quad (3-25)$$

### 3.2.2 Wye Filter Power Transfer

The impact on power transfer by a wye connected filter is far simpler than that of a delta connected one since the impact of the element's reactive power affects the relevant phase only. The above equations can thus be modified to include wye connected filters as follows:

$$P_a = P_x - \frac{1}{2\sqrt{3}}P_{cap\_ab} + \frac{1}{2\sqrt{3}}P_{cap\_ca} \quad (3-26)$$

$$Q_a = Q_x - \frac{1}{2}P_{cap\_ab} - \frac{1}{2}P_{cap\_ca} - P_{cap\_a} \quad (3-27)$$

$$P_b = P_y - \frac{1}{2\sqrt{3}}P_{cap\_bc} + \frac{1}{2\sqrt{3}}P_{cap\_ab} \quad (3-28)$$

$$Q_b = Q_y - \frac{1}{2}P_{cap\_bc} - \frac{1}{2}P_{cap\_ab} - P_{cap\_b} \quad (3-29)$$

$$P_c = P_z - \frac{1}{2\sqrt{3}}P_{cap\_ca} + \frac{1}{2\sqrt{3}}P_{cap\_bc} \quad (3-30)$$

$$Q_c = Q_z - \frac{1}{2}P_{cap\_ca} - \frac{1}{2}P_{cap\_bc} - P_{cap\_c} \quad (3-31)$$

### 3.2.3 Unbalance Correction Algorithm – Grounded-Wye Connected Load

Thus, for a given unbalanced system, a capacitor combination ( $P_{cap\_ab}$ ,  $P_{cap\_bc}$ ,  $P_{cap\_ca}$ ,  $P_{cap\_a}$ ,  $P_{cap\_b}$  &  $P_{cap\_c}$ ) must be found such that:

$$P_a = P_b = P_c \quad (3-32)$$

$$Q_a = Q_b = Q_c = 0 \quad (3-33)$$

It should be noted that capacitors may only be added between two line to line voltages since adding the third capacitor would simply result in power factor correction. It should also be noted that the required power transfer from each phase to the next can easily be found by knowing that the total real power flow before compensation must equal to the total real power flow after compensation (since the law of conservation of energy must be satisfied). Because of this, and because all phases must transfer equal amounts of real power under balanced situations, each phase should then transfer real power equal to the average of the real power over all

phases. To calculate the required real power transfer, the required change in real power can be found by comparing actual power flow to the average power flow as follows:

$$P_{ave} = \frac{1}{3}(P_a + P_b + P_c)$$

$$\Delta P_a = P_a - P_{ave} \quad \Delta P_b = P_b - P_{ave} \quad \Delta P_c = P_c - P_{ave}$$

Thus:

$$\Delta P_a = -\frac{1}{2\sqrt{3}}P_{cap\_ab} + \frac{1}{2\sqrt{3}}P_{cap\_ca} \quad (3-34)$$

$$\Delta P_b = -\frac{1}{2\sqrt{3}}P_{cap\_bc} + \frac{1}{2\sqrt{3}}P_{cap\_ab} \quad (3-35)$$

$$\Delta P_c = -\frac{1}{2\sqrt{3}}P_{cap\_ca} + \frac{1}{2\sqrt{3}}P_{cap\_bc} \quad (3-36)$$

To find the combination of capacitors that will result in the transfer of power as described by  $\Delta P_a$ ,  $\Delta P_b$  and  $\Delta P_c$ , a matrix  $A^{-1}$  must be found where:

$$\begin{bmatrix} \Delta P_a \\ \Delta P_b \\ \Delta P_c \end{bmatrix} = \frac{1}{2\sqrt{3}}A \begin{bmatrix} P_{cap\_ab} \\ P_{cap\_bc} \\ P_{cap\_ca} \end{bmatrix}$$

$$A = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$$

However, for matrix 'A' to be invertible, it must have a non-zero determinant:

$$\text{Determinant}(A) = |A| = -1 \begin{vmatrix} -1 & 0 \\ 1 & -1 \end{vmatrix} - 0 \begin{vmatrix} 1 & 0 \\ 0 & -1 \end{vmatrix} + 1 \begin{vmatrix} 1 & -1 \\ 0 & 1 \end{vmatrix} = -1 - 0 + 1 = 0$$

Thus a matrix  $A^{-1}$  does not exist. However, matrix A is the solution to the general case where capacitor sizes for all three phases are considered. It is, however, known

that the connection of capacitors over all three phases must not occur, since this would result in normal power factor correction. Thus, for each current unbalance situation, one of the three capacitor variables may be eliminated from the calculations, allowing an invertible solution to the new matrix to exist. To determine which variable to eliminate for any given solution, some logic needs to be applied as shown below.

For any given  $\Delta P_a$ ,  $\Delta P_b$  and  $\Delta P_c$  set, there must exist at least one  $\Delta P_n$  that is negative (below average) and at least one  $\Delta P_n$  that is positive (above average). Knowing this, and knowing that real power is always transferred around the phases in the order from leading to lagging ( $V_a$  to  $V_b$  to  $V_c$  to  $V_a$  again) reveals which phase must have zero capacitance.

Let 's' equal the number of  $\Delta P_n$  ( $n = a, b, c$ ) that is greater than zero.

*if s = 1:*                    Begin at  $\Delta P_n$  where  $P_n$  is the only phase with above average power transfer. Transfer  $\Delta P_n$  to  $P_{n+1}$ . Then Transfer  $\Delta P_n + \Delta P_{n+1}$  to phase  $\Delta P_{n+2}$ . For example:

*if  $\Delta P_a > 0$*

*Transfer power to the value of  $\Delta P_a$  to phase 'B'.*

*Then transfer power to the value of  $\Delta P_a + \Delta P_b$  to phase 'C'.*

*if s = 2:*                    Begin at  $\Delta P_{n+1}$  where  $P_n$  is the only phase whose power transfer is below average; transfer all  $\Delta P_{n+1}$  to  $P_{n+2}$ . Then transfer  $\Delta P_{n+1} + \Delta P_{n+2}$  to  $P_n$  to result in real power balance. For Example:

*if  $\Delta P_a < 0$*

*Transfer power to the value of  $\Delta P_b$  to phase 'C'.*

*Then transfer power to the value of  $\Delta P_b + \Delta P_c$  to phase 'A'.*

The above control logic may be summarized into a flowchart, as seen in Figure 16 below.

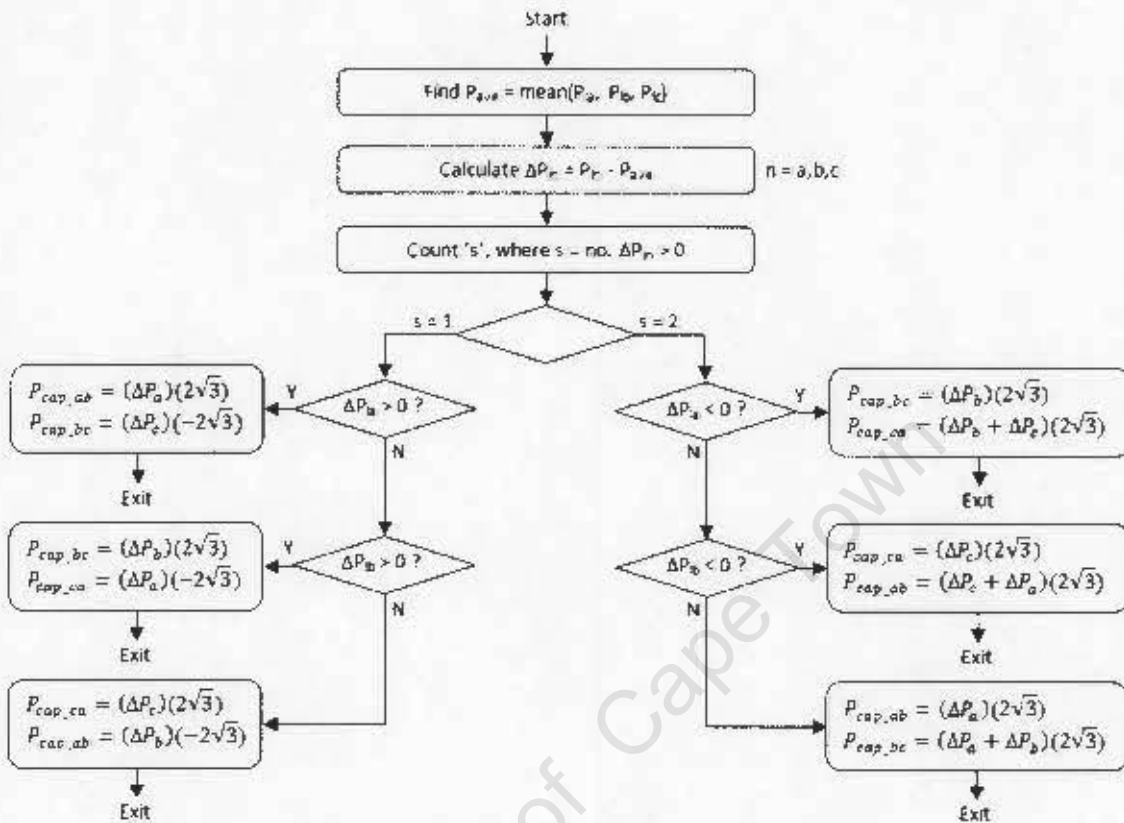


Figure 16: Capacitor Power Equation Flowchart

The next step in the algorithm is to calculate the amount of power factor correction and wye filtration required to bring the system to full balance and unity power factor on each individual phase. This is easily accomplished by measuring the level of inductive reactive power left on each phase. If all three phases are still transferring inductive reactive power, then the level of power factor correction is increased to the value of the smallest phase reactive power, leaving only two phases with capacitive reactive power transfer. Wye connected filter levels are then increased on these phases until all inductive reactive power is removed.

### 3.2.4 Unbalance Correction Algorithm – Non-Grounded Wye or Delta Connected Load

So far, only grounded wye connected loads (three phase, four wire networks) have been dealt with, since this is the more general case. However, a solution may also be found for the non-grounded wye or delta connected cases, in which no neutral (or therefore zero sequence) currents may flow. Because no neutral currents exist (and therefore no zero sequence currents) in these circuit types, all wye connected filters would become redundant. It is well known that a non-grounded wye connected load can be transformed to an equivalent delta connected load (since neither have a neutral connection), such that a voltage source would not be able to see a difference between the two circuits (12). The transformation equations, along with their proofs from (12) are given in Appendix A. It should be noted that because of the  $\Delta$ -Y transformation mentioned above, only one connection type needs to be examined (the delta connection type) for simplicity. It would be possible to use a wye connected filter as either power factor correction or as a delta filter; however, a significant effective capacitor power capacity loss will be seen due to the fact that the capacitor is still wired as a wye filter (and thus sees a line to neutral voltage instead of a line to line voltage). This is demonstrated below:

For 100 kVAR Capacitor (nominal):

$$\text{Single Capacitor Impedance} = \left( \frac{3\Phi \text{ Power}}{3(V_L - I)^2} \right)^{-1} = \left( \frac{100000}{3(400)^2} \right)^{-1} = 4.8\Omega$$

If 100 kVAR Wye connected bank were used for PFC:

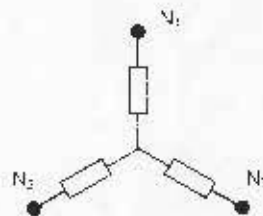


Figure 17: Power Factor Correction with Wye Connected Capacitors

$$\text{Effective Power}_{3\phi} = 3 \frac{V^2}{(Z_{L-N})} = 3 \frac{230^2}{(4.8)} = 33062 \text{ VAr} \quad (66\% \text{ Power loss})$$

If 100 kVAr Wye connected bank were used as a delta filter:

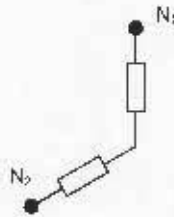


Figure 18: Delta Connection of a Wye connected Capacitor bank (non-grounded)

$$\text{Single Capacitor Impedance} = \left( \frac{3\phi \text{ Power}}{3(V_{L-L})^2} \right)^{-1} = \left( \frac{100000}{3(400)^2} \right)^{-1} = 4.8\Omega$$

$$\text{Impedance seen Line to Line} = 2 \times Z_{L-N} = 9.6\Omega$$

$$\text{Effective Power} = \frac{V_{L-L}^2}{Z} = \frac{400^2}{9.6} = 16667 \text{ Var} \quad (83\% \text{ Power loss})$$

A similar power loss effect is seen with a 50 kVAr (nominal) capacitor bank and thus, it would be prudent to wire all capacitor banks into a delta configuration to avoid such power loss when a delta or non-grounded wye connected load is being compensated for. All of the theory demonstrated in section 3.2.1, still holds for real power transfer around a poly phase network and thus the equations set out in section 3.2.2 remain correct.

### 3.3 Harmonic Amplification

It is stated in section 2 that the introduction of capacitors into a system increases harmonic content, in particular, the 3<sup>rd</sup> order harmonic. It should be noted, however, that capacitors themselves do not create harmonics; they simply amplify pre-existing harmonics present in the utility grid (13). This phenomenon may be explained by examining the equation governing the impedance seen by a voltage source:

$$X_c = \frac{1}{2\pi fC} \quad (3-37)$$

It can be seen that as the frequency of the applied voltage waveform is increased, so the impedance of the capacitor for that waveform decreases. This means that a capacitor presents a lower impedance to a higher order harmonic, resulting in a larger current flow at that harmonic frequency. Thus, a capacitor simply amplifies the harmonic content of the voltage waveform placed across it by transforming that voltage harmonic into a current harmonic. A large source impedance would thus also mean that the newly amplified current harmonics could further increase voltage harmonics (due to the added source impedance voltage drop), thereby perpetuating the situation. The most common harmonic orders that engineers face are called the 'Triplen' harmonics and constitute the 3<sup>rd</sup>, 9<sup>th</sup> and 15<sup>th</sup> harmonic orders (14). These harmonics are a concern because the consequences of the resultant increased current flow is cable failure, nuisance tripping and other equipment failure.

It should also be noted that harmonic generation is caused by the addition of non-linear loads to the utility grid, where a non-linear load consumes a disproportionate amount of current to the voltage level as a particular phase cycle is completed. The most common non-linear load is a rectifier, where the diodes of the rectifier conduct only at the peak of the voltage waveform. Another common harmonic source is switch-mode power supplies, where the current is constantly being switched.

## 4 Hardware Design

### 4.1 System Overview

For ease of manufacture and for cost effectiveness, it was decided upon that the current balancer hardware would consist of a modified version of a standard power factor correction unit.

A standard unit consists of a series of capacitor banks, each connected in a delta fashion and driven by a three phase contactor, this is easily modified to satisfy the requirements defined in section 3.2. The power factor correction unit must also consist of capacitor banks that have individual capacitor connections (i.e. a total of 6 connections such that they may be rewired into a wye configuration). One such unit that satisfies the above requirements is one from Electro-Mechanica (product code: 51500) and is a 500 kVAR system consisting of four 100 kVAR and two 50 kVAR capacitor banks.

At least one of the capacitor banks will have to be rewired to a wye configuration, resulting in a corresponding effective power decrease (since the voltage seen by the capacitors decreases from a line to line value to a line to neutral value). This would leave the system at an effective power rating:

$$P_{\text{effective}} = 400 + \frac{100}{\sqrt{3}\sqrt{3}} = 433 \text{ kVAR}$$

To compensate for this power decrease, and to maintain the overall power rating of the system at 500 kVAR, an extra capacitor bank will be added to the system and will consist of another standard 100 kVAR bank that will be rewired to a double 50 kVAR bank in a wye configuration. The proposed system modifications are outlined in Figure 19 below.

Original System			Proposed System		
Capacity	Function	Contactors	Capacity	Function	Contactors
100 kVAr	PFC	1 x 3 $\Phi$	100 kVAr	PFC	1 x 3 $\Phi$
100 kVAr	PFC	1 x 3 $\Phi$	100 kVAr	PFC	1 x 3 $\Phi$
100 kVAr	PFC	1 x 3 $\Phi$	50 kVAr	PFC	1 x 3 $\Phi$
100 kVAr	PFC	1 x 3 $\Phi$	50 kVAr	$\Delta$	3 x 1 $\Phi$
50 kVAr	PFC	1 x 3 $\Phi$	100 kVAr	$\Delta$	3 x 1 $\Phi$
50 kVAr	PFC	1 x 3 $\Phi$	50 kVAr	Wye	3 x 1 $\Phi$
			50 kVAr	Wye	3 x 1 $\Phi$
			100 kVAr	Wye	3 x 1 $\Phi$

Additional Bank →

Figure 19: Hardware - Proposed Modifications

It can be seen in Figure 19 that the capacitor banks that are to be rewired into a delta or wye filter require three contactors each, one contactor for each phase. This is so that each bank may compensate for unbalance on any phase, as required by the unbalance of the load. It should also be noted that if all three contactors are closed, each bank then performs normal power factor correction resulting in a power factor correction/current unbalance hybrid system.

## 4.2 Hardware Modification

To complete the conversion, the following steps need to be completed:

Remove the tray consisting of the double 50 kVAr capacitor banks. One of these 50 kVAr sections is rewired, along with additional contactors to be under single phase control, described in the above diagram as a 'delta filter'. Here, each of the three phases is controlled by an individual contactor and will require two of those contactors to be closed for the bank to be connected to the grid.

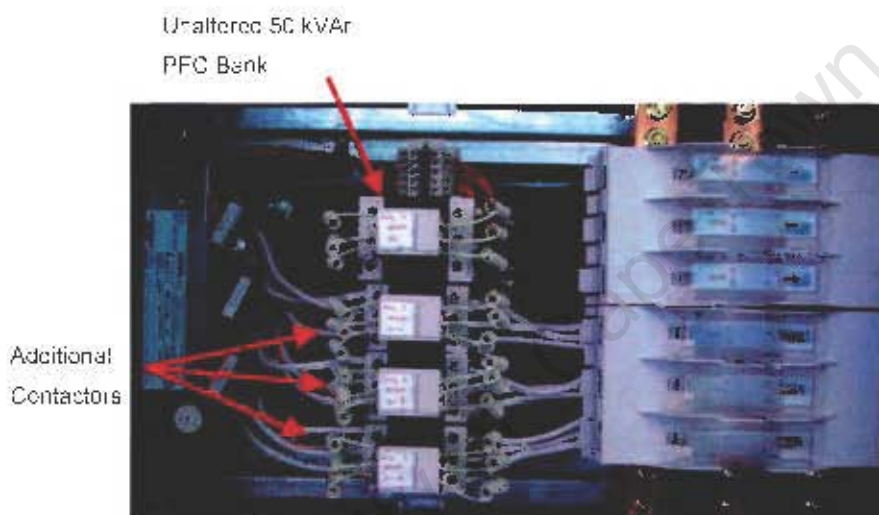


Figure 20: Photo - Rewired 50 kVAr delta Capacitor Bank (Bank 4)

Next, one of the 100kVAr banks is removed and, in the same manner described above, is rewired to be under single phase control to form part of the delta connected filter. Note that because each contactor is used to control a single phase, the phase current is paralleled across each of the three contactor terminals, thus reducing the required contactor size.

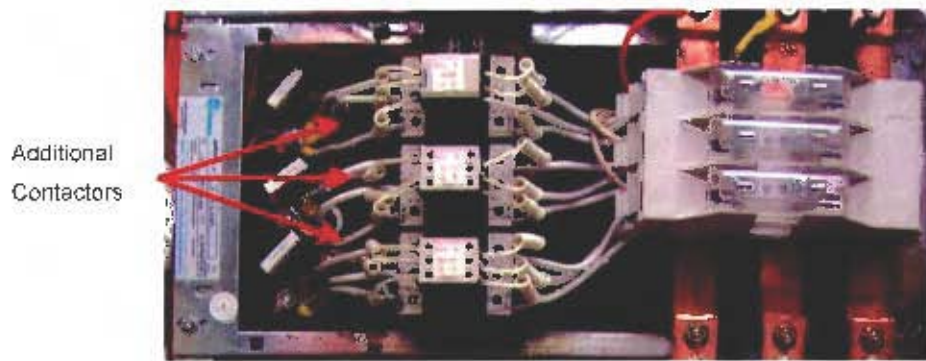


Figure 21. Photo - Rewired 100 kVAR Delta Capacitor Bank (Bank 5)

Another 100kVAR bank is then also removed and rewired to form part of the wye filter upon which a small section of DIN rail is added to house the connector terminal for the neutral point of the wye connection.

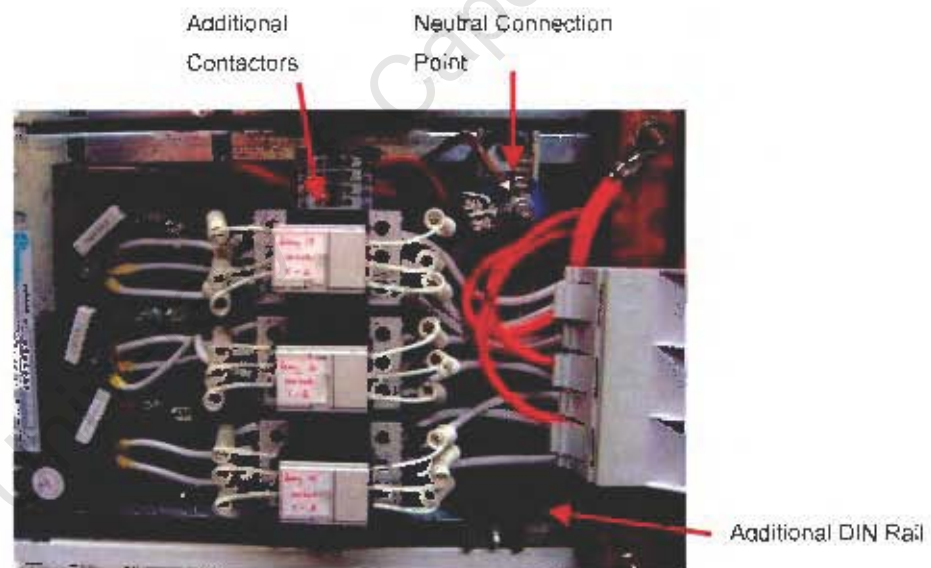


Figure 22: Photo - Rewired 100 kVAR Wye Capacitor Bank (Bank 8)

The additional bank that was purchased to add to the cabinet (2 x 50 kVAr sections) is also rewired to form two wye connected filters. Here, there are six contactors for single phase control as well as added DIN rail to support the neutral point connector block. This bank is inserted below the main cabinet breaker in the 'spare' slot and all neutral points are connected together via copper cable.

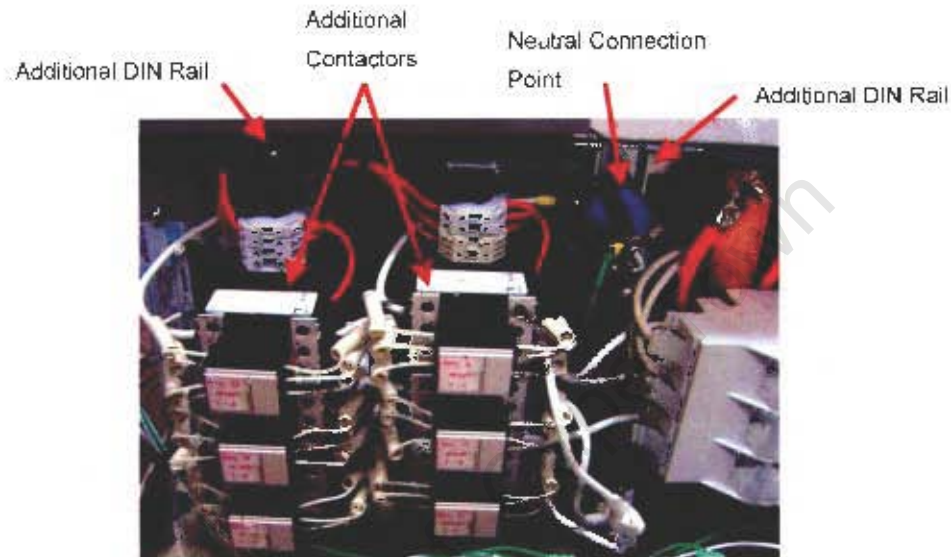


Figure 23: Photo - Rewired 2 x 50 kVAr Wye Capacitor Banks (Banks 6 & 7)

### 4.3 Contactor Sizing

Each new additional contactor must be rated according to the capacitor size and therefore current drawn by each capacitor. Capacitor values can be calculated from their rated three phase power with the equations below:

$$|X_C| = \frac{1}{2\pi fC} \quad (4-1)$$

$$P = \frac{V^2}{X_C} = VI \quad (4-2)$$

$$C = \frac{P/3}{2\pi fV^2} \quad (4-3)$$

**Banks 1 & 2:** 100 kVAr – 3Φ power factor correction

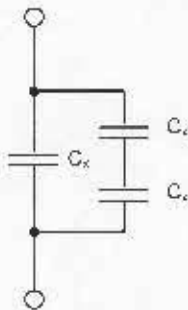
$$I = \frac{P}{3V_{L-N}} = \frac{100000}{3 \times 230} = 145 \text{ A}_{rms} \text{ per phase} \quad \text{where } V_{L-N} = 230 \text{ V}_{rms}$$

**Bank 3:** 50 kVAr – 3Φ power factor correction

$$I = \frac{P}{3V_{L-N}} = \frac{50000}{3 \times 230} = 72.5 \text{ A}_{rms} \text{ per phase} \quad \text{where } V_{L-N} = 230 \text{ V}_{rms}$$

**Bank 4:** 50 kVAr - 1Φ delta filter

Note: only two of the three connection contactors will be closed at any given time, resulting in an equivalent circuit shown below.



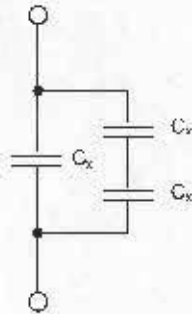
$$C_{apparent} = (1C_x + 0.5C_x) = 1.5C_x$$

$$P_{equivalent} = P_{3\Phi} + 2 = 25 \text{ kVAr}$$

$$I = \frac{P}{V_{L-L}} = \frac{25000}{400} = 62.5 \text{ A}_{rms}$$

**Bank 5:** 100 kVAr - 1Φ delta filter

Note: only two of the three connection contactors will be closed at any given time, resulting in an equivalent circuit shown below.

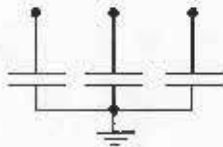


$$C_{\text{apparent}} = (1C_x + 0.5C_x) = 1.5C_x$$

$$P_{\text{equivalent}} = P_{3\Phi} \div 2 = 50 \text{ kVAr}$$

$$I = \frac{P}{V_{L-N}} = \frac{50000}{400} = 125 \text{ A}_{\text{rms}}$$

**Banks 6 & 7:** 50 kVAr - 1Φ Wye filter

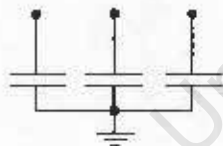


$$C_{1\Phi} = \frac{P/3}{2\pi f V^2} = \frac{50000/3}{2\pi 50 (400)^2} = 331.5 \mu\text{F}$$

$$P_{\text{apparent}} = \frac{V^2}{Z} = V_{L-N}^2 (2\pi 50) C_{1\Phi} = 5509 \text{ VAr}$$

$$I = \frac{P}{V} = 23 \text{ A}_{\text{rms}}$$

**Bank 8:** 100 kVAr - 1Φ Wye filter



$$C_{1\Phi} = \frac{P/3}{2\pi f V^2} = \frac{100000/3}{2\pi 50 (400)^2} = 663.1 \mu\text{F}$$

$$P_{\text{apparent}} = \frac{V^2}{Z} = V_{L-N}^2 (2\pi 50) C_{1\Phi} = 11020 \text{ VAr}$$

$$I = \frac{P}{V} = 48 \text{ A}_{\text{rms}}$$

The following contactor sizes are calculated (some over rating allowed) as per the above formula and tabulated below. Also, note that three phase contactors being used for a single phase may have their terminals paralleled.

Bank No.	Power	Function	Contactor
1	100kVAr	PFC	90 A - 3 $\Phi$
2	100kVAr	PFC	90 A - 3 $\Phi$
3	50kVAr	PFC	43 A - 3 $\Phi$
4	50kVAr	Delta	25A - 3x1 $\Phi$
5	100kVAr	Delta	43A - 3x1 $\Phi$
6	50kVAr	Wye	20A - 3x1 $\Phi$
7	50kVAr	Wye	20A - 3x1 $\Phi$
8	100kVAr	Wye	20A - 3x1 $\Phi$

Table 1: Capacitor Bank Powers and Functions

## 5 Simulation: Current Balancer

To ensure that the theory described in the previous sections is accurate, and that the system will have the desired effect in reality, the system is simulated using the "MATLAB Simulink" computer simulation package.

### 5.1 Capacitor Power Flow Theory

To ensure that the equations that were calculated in section 3 are correct, a simple simulation was set up as shown below to examine the power flow through the capacitor and its effect on the line currents.

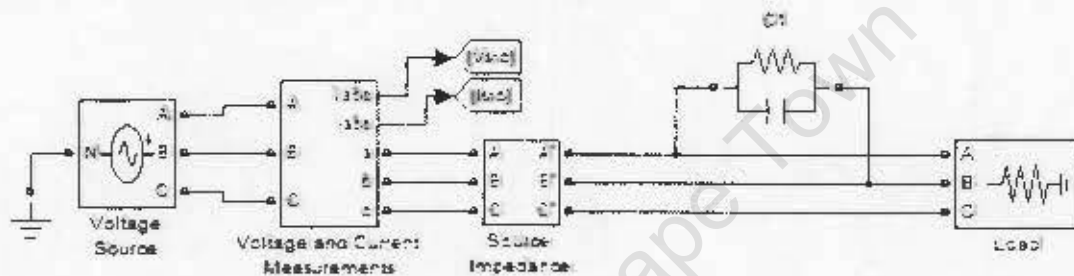


Figure 24: Simulation Schematic - Power Flow Through a Capacitor

The load in the above setup was programmed to have a large impedance, thereby allowing the power flow measurements that are calculated from the voltage and current measurement block to be influenced by the capacitor power flow only. Voltage waveforms of voltages across and current through the capacitor, C1, are examined in detail below:

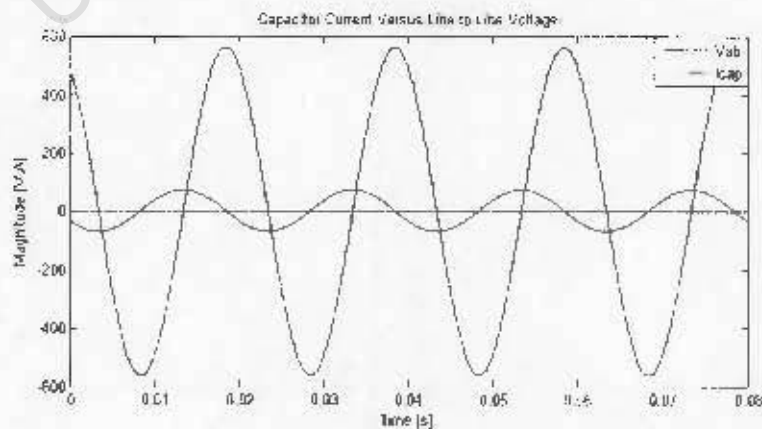


Figure 25: Simulation Waveform - Capacitor Current Versus Line Voltage

It can be seen in Figure 25 that the current through capacitor C1 (green waveform) leads the line voltage across the capacitor (blue waveform) by  $90^\circ$  resulting in the consumption of purely capacitive reactive power by the capacitor. If this current flow is now referenced to the line to neutral voltages  $V_a$  and  $V_b$  that comprise the line to line voltage  $V_{ab}$ , the following results are seen:

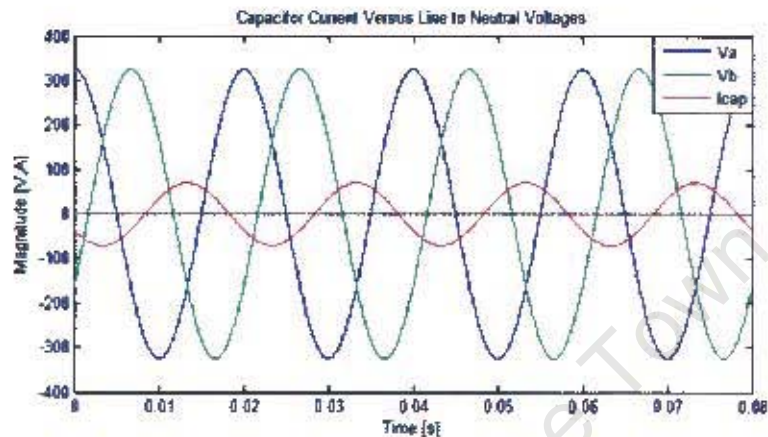


Figure 26: Simulation Waveform - Capacitor Current Versus Line to Neutral Voltages

It can be seen in Figure 26 that the capacitor current leads  $V_a$  by  $120^\circ$  and lags  $V_b$  by  $120^\circ$ , as predicted in section 3.2.1, Figure 15. By tabulating simulation results with several different capacitor values and comparing the power transfer to that predicted by theory, it can be seen that the simulation agrees with theory:

Capacitor Power	1000	5000	10000
Predicted $\Delta P_a$	-288.7	-1443.4	-2886.8
Simulated $\Delta P_a$	-288.5	-1443.7	-2888
Predicted $\Delta P_b$	288.7	1443.4	2886.8
Simulated $\Delta P_b$	289	1443.1	2886
Predicted $\Delta Q_a$	-500	-2500	-5000
Simulated $\Delta Q_a$	-500	-2499	-4999
Predicted $\Delta Q_b$	-500	-2500	-5000
Simulated $\Delta Q_b$	-500	-2501	-5001

Table 2: Comparison Between Current Unbalance Theory and Simulation

## 5.2 Current Balancer Overview

Once it was confirmed that the theory set out in section 3 was in fact accurate and that the simulation package is in agreement, the entire current balancer hardware can be simulated as a whole as shown below:

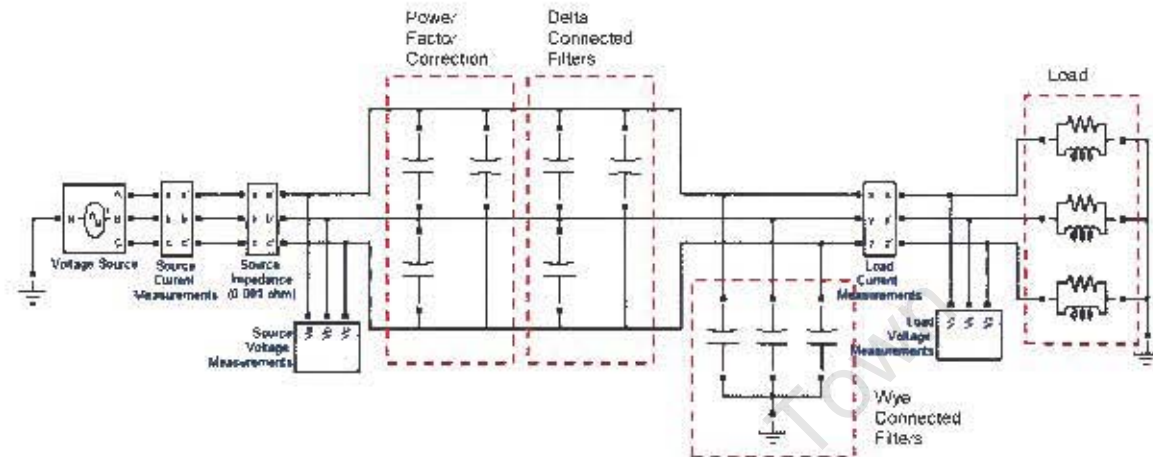


Figure 27: Simulation - Current Balancer

## 5.3 Phase Power Calculator

Next, power measurement blocks were set up as shown below (for phase 'n'), the calculated phase real and reactive power will be used in the control algorithm set out in section 3.2.3 to calculate the optimum compensation capacitor values. Power calculations are performed for each source phase as well as load phase.

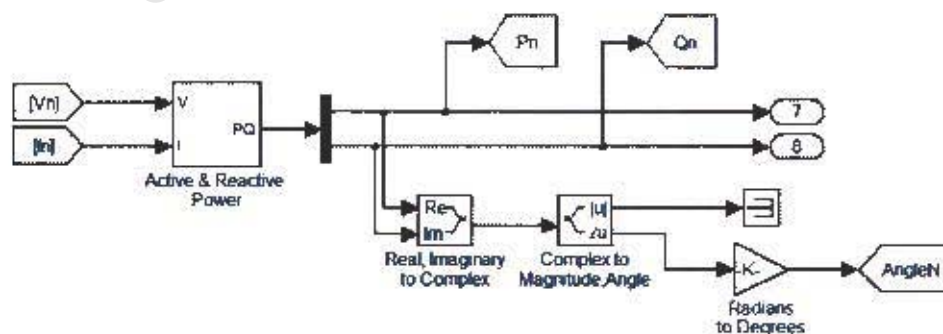


Figure 28: Phase Real and Imaginary Power Calculator

## 5.4 Unbalance Level Calculator

To be able to analyze the effect of the current balancer algorithm on the unbalance seen by the source in the simulation in Figure 28, the level of unbalance is measured both before and after current balancing has taken place. This is accomplished in line with the method set out in section 3.1 and is calculated in Simulink as shown below:

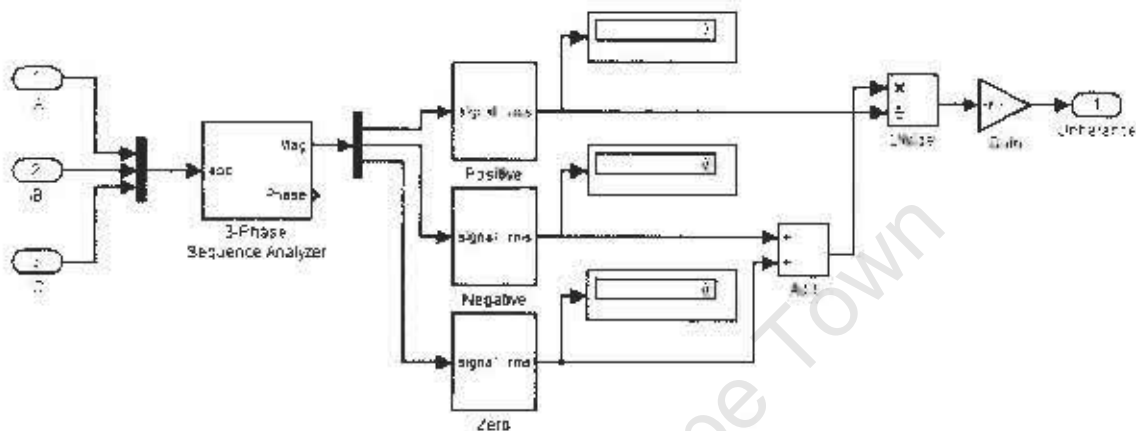


Figure 29: Simulation - Unbalance Calculator

## 5.5 Unbalance Reduction Algorithm

To test the unbalance reduction algorithm, an embedded MATLAB function was created within the simulation that accepted the load real and imaginary powers and returns the various delta filters, wye filters and power factor correction levels. This is achieved in conjunction with the algorithm set out in section 3.2.3.

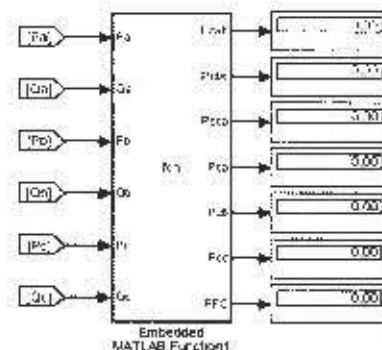


Figure 30: Simulation - Unbalance Control Algorithm Function Block

See Appendix D for the embedded function.

## 5.6 Simulation Results

The current unbalance control block described in the section above (section 5.5) is configured to return the exact number of capacitive VARs required in each filter to achieve current balance and unity power factor, however, should the load not be sufficiently inductive, the algorithm returns the best available solution without allowing the source to see a capacitive load. The algorithm achieves this by scaling the capacitor values down until the phase with the least inductive load achieves unity power factor. By running the simulation with several differing load unbalances and power factors, the effect of the system on unbalance can be seen in table form below. An initial test was also performed on the control algorithm where a purely real, unbalanced load was placed onto the source. The algorithm returns a zero value for all capacitive filters as required since any capacitor addition would result in a leading power factor and less efficient energy consumption by the load.

Phase	Load		$\Delta$ -Filter [kVAr]	Wye- Filter [kVAr]	PFC Power	Source	
	[kW]	[kVAr]				[kW]	[kVAr]
A	122624	0	0	0	0	122624	0
B	78934	0	0	0	0	78934	0
C	100910	0	0	0	0	100910	0
<b>Unbalance</b>	25.00%					25.00%	

Table 3: Simulation - Zero Inductance Load

Table 3 above shows the simulation results of the balancer unit on a purely resistive load. Since no capacitors can be added without reducing the power factor of the load, no real power balance can be achieved.

Phase	Load		$\Delta$ -Filter [kVAr]	Wye- Filter [kVAr]	PFC Power	Source	
	[kW]	[kVAr]				[kW]	[kVAr]
A	122645	15107	15100	0	0	113918	0
B	78982	15102	15100	0	0	87717	0
C	100833	15104	0	15095	0	100835	-140
<b>Unbalance</b>	24.76%					15.04%	

Table 4: Simulation - Inductance Starved Load

Table 4 above shows the simulation results of the balancer unit operating on a load

that is badly unbalanced and is composed of a complex load. However, the load is not inductive enough to be fully balanced by the balancer and only a partial decrease in the level of unbalance can be seen.

Phase	Load		$\Delta$ -Filter [kVAr]	Wye- Filter [kVAr]	PFC Power	Source	
	[kW]	[kVAr]				[kW]	[kVAr]
A	100820	30216	0	22500	7700	100818	-200
B	110891	35252	17500	10000	7700	100784	-65
C	90744	25180	17500	0	7700	100860	-42
<b>Unbalance</b>	12.40%					0.16%	

Table 5: Simulation - Fully Balanced Load

It can be seen in Table 5 that a load that is sufficiently inductive for the balancer can be fully balanced from the source perspective.

Phase	Load		$\Delta$ -Filter [kVAr]	Wye- Filter [kVAr]	PFC Power	Source	
	[kW]	[kVAr]				[kW]	[kVAr]
A	122652	40317	37500	0	2290	100975	261
B	78923	40300	37500	0	2290	100587	251
C	100885	24650	0	22000	2290	100894	-90
<b>Unbalance</b>	20.27%					0.25%	

Table 6: Simulation - Maximum Unbalance Power

Table 6 shows an unbalanced load that requires the maximum capacitor power available to it by the current balancer (75 kVAr line to line plus 22 kVAr line to neutral). The load unbalance (20%) represents the maximum unbalance that may be compensated for a load of that particular size (average of 100 kW per phase). As average load size increases, so the maximum reducible unbalance decreases proportionally. This proportionality is shown below where load networks of varying sizes are balanced with maximum balancing power. Because power transfer through delta connected filters occurs only from the leading phase to the lagging phase, the optimum unbalance situation would exist where one phase (say phase 'A') transfers

power above the three phase average by an amount of 21650 kW [(maximum delta filter power)/(sqrt(3)\*2)], whilst phase 'B' transfers power below average by 21650 kW and phase 'C' transfers average power. This is because all delta filters can be connected across one line to line voltage (phase 'AB' in this case). If the average phase size in the situation described above is adjusted and the simulation run, a graph of maximum reducible unbalance versus load size may be plotted (see Figure 31).

Total 3Φ Load Size [kW]	Maximum Reducible Unbalance
300	20%
500	13%
750	9.67%
1000	6.96%
1200	5.87%
1500	4.96%
1700	4.22%
2000	3.60%
2200	3.29%
2500	2.90%

Table 7: Simulation - Maximum Reducible Unbalance versus Load Size

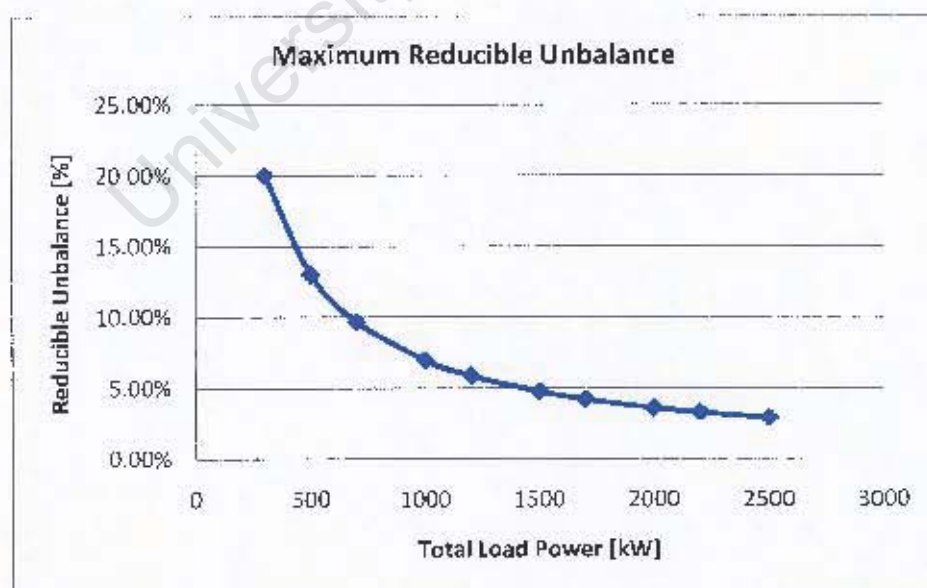


Figure 31: Simulation - Maximum Reducible Unbalance Versus Load Size

It can thus be said that the control algorithm set out in section 3.2.3 does indeed work correctly and can exactly balance a load given that the load is sufficiently inductive in nature for its unbalance.

## 5.7 Discrete Current Unbalance Control Algorithm

Because the balancer unit does not have access to an infinite number of capacitor powers, the control algorithm must be adjusted to return the nearest level of compensation as allowable, given the number of capacitor banks and the number of steps in compensation power. The available steps are set out below for each type of filter:

### 5.7.1 Delta Connected Filter:

If only one phase requires compensation:

<b>Power Level</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>
<b>Power [kVAr]</b>	0	25	50	75

If two phases require compensation:

<b>Power Level</b>	<b>0</b>	<b>1</b>	<b>2</b>
<b>Power (Major Phase) [kVAr]</b>	0	25	50
<b>Power (Minor Phase) [kVAr]</b>	0	0	25

### 5.7.2 Wye Connected Filter:

Any phase may have, simultaneously, the following power levels:

<b>Power Level</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
<b>Phase Power [kVAr]</b>	0	5.5	11	16.5	22

### 5.7.3 Power Factor Correction:

In unbalance correction mode, the following levels of power factor correction are available:

Power Level	0	1	2	3	4	5
3 $\Phi$ Phase Power [kVAr]	0	50	100	150	200	250

Once a solution has been found for the power required for the delta filters, the control algorithm then finds the nearest appropriate delta power level (determined by the capacitor sizes) and subtracts this from the remaining compensation required by the wye filters. Once a solution has been determined for the total required reactive compensation required for each phase, the power factor correction level is set such that the wye filters compensate with the least required power. In other words, the three phase power factor correction power is set to the smallest of the required reactive power required over the three phases. This is done since the wye filter power combinations are much finer than that of the delta or power factor correction levels. This allows for a more accurate solution with finer effective resolution.

### 5.8 Contactor Switching Transients

Figure 32 shows a contactor that was provided with the standard power factor correction unit, clearly visible is the addition of an auxiliary contactor above the main unit. This auxiliary contactor is mechanically connected to the main unit's contacts and will temporarily conduct during the main unit's switch-in cycle before allowing the load current to pass through the main contactor's terminals. During the auxiliary contactor's conduction cycle, current is limited by the additional resistive wires (of resistance 2.2  $\Omega$  per wire, or 4.4  $\Omega$  per phase). This allows for the pre-charging of the load capacitor, thereby reducing inrush current and protecting both the capacitor and contactor. To be able to simulate what transients will be created during a switch-in cycle of the contactor, the length of time for which the auxiliary contactor conducts must be determined (see section 11.3). After laboratory testing, it was found that the average time for which the auxiliary is conducting for is 4ms.

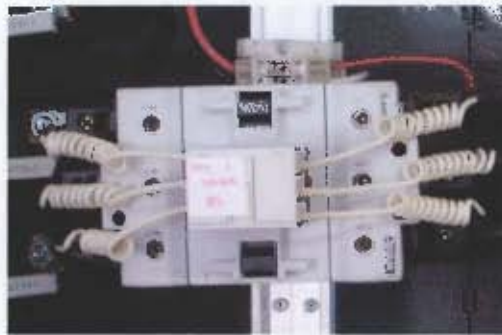


Figure 32. Photo - Contactor with Auxiliary Resistor Wires

To be able to determine the influence of the additional resistive wires, a contactor switch-in cycle was simulated first without resistive wires. The model is shown below:

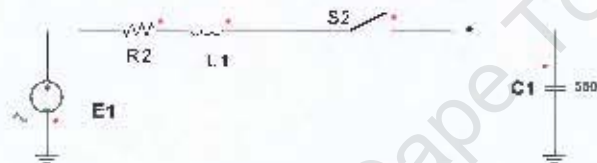


Figure 33. Simulation - Contactor Switch-in without Auxiliary Resistive Wires

To ensure that the worst possible case is accounted for, the switch 'S2' was programmed to close at the peak of the voltage waveform. A source impedance of 15 mΩ with inductance of 1 μH was estimated.

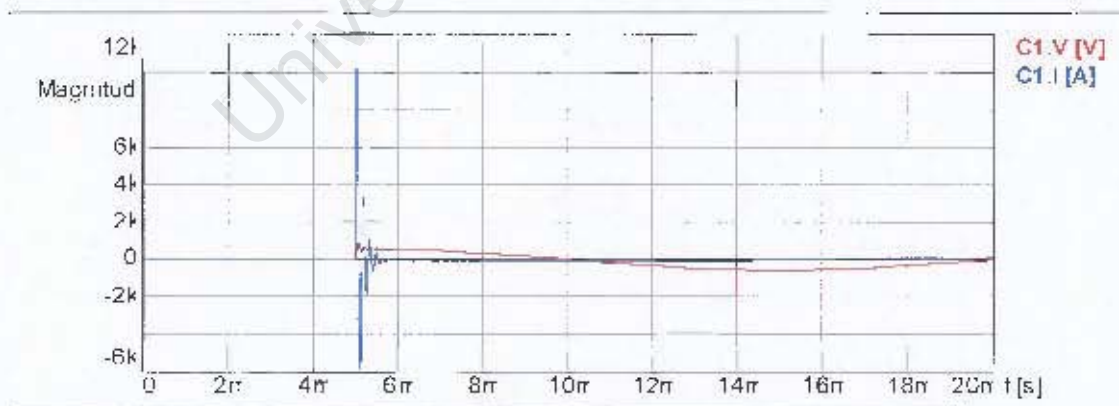


Figure 34: Waveform - Current Transient without Resistive Wires

It can be seen that the transient created has a maximum amplitude of 11 kA and oscillates for approximately 1 ms.

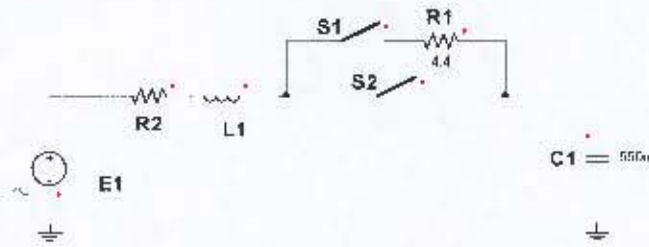


Figure 35: Schematic - Contactor Switch-in with Resistive Wires

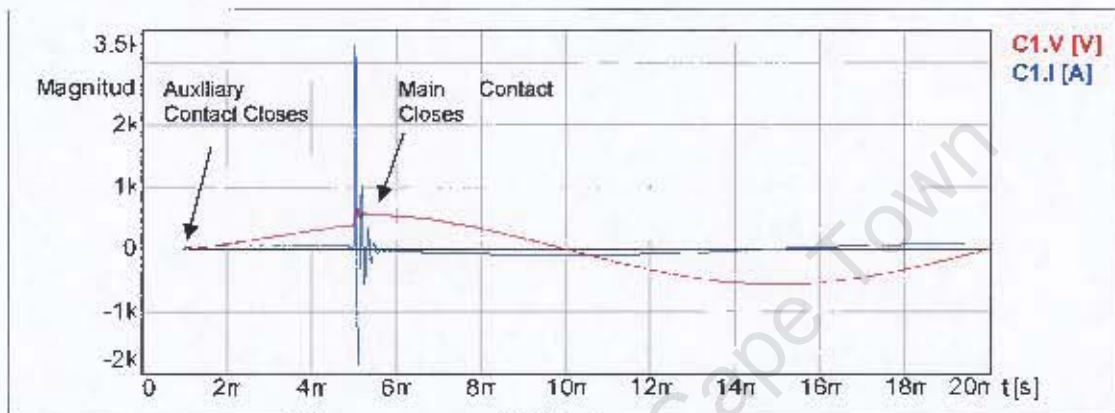


Figure 36: Waveform - Current Transient with Resistive Wires

Figure 36 shows the current transient generated with the use of resistive wires; the maximum current amplitude has been reduced to 3.5 kA whilst the transient persists for approximately 1ms. This will significantly reduce the strain placed on each contactor, thereby increasing the contactor lifespan.

## 6 Financial Analysis

The ultimate aim of the hybrid system is to save the end user money on a month to month basis. It is thus prudent to examine the financial viability of such a system and its impact on a utility bill. For this analysis, several load sizes at a range of power factors are analyzed and a comparison is made. To be able to calculate the actual savings achieved per month, an appropriate electricity tariff schedule must be chosen. By examining the relationship of load size and reducible unbalance (Figure 31), it can be seen that to achieve a significant reduction in unbalance for a 500 kVAR compensator system, a load size of 500 kVA to 1.5 MVA must be compensated for. However to ensure that all load size ranges are examined, load sizes in the range of 300 kVA to 2 MVA will be analyzed (300 kVA, 500 kVA, 1 MVA, 1.5 MVA and 2 MVA).

Load sizes in this range fall into ESKOM's 'MINI FLEX' tariff schedule, available from (15). In this tariff structure, provision is made for a network access charge of R7.14 per KVA, as well as a reactive energy charge of 1.39 cents per kVARh supplied in excess of 30 percent of the real energy usage. This means that the customer will only be charged for reactive energy if their power factor is 0.96 or worse. It should be noted that all maximum demand charges are included in the real and reactive energy charges.

To be able to calculate the savings gained, an examination of the excess reactive power (reactive power used in excess of 0.96 power factor) used by each load size is graphed in Figure 37.

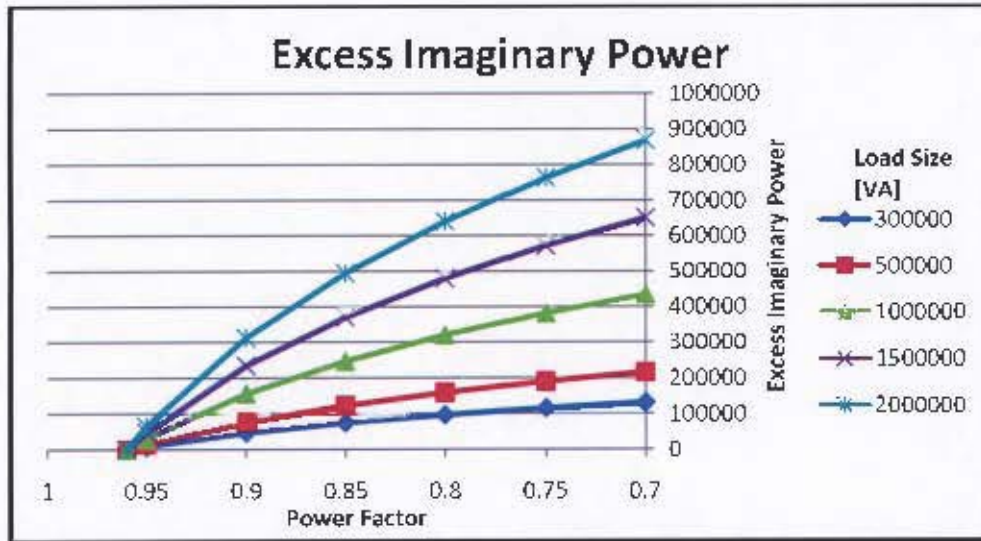


Figure 37: Graph - Excess Imaginary Power of Several Load Sizes Versus Power Factor

Considering that the proto-type hybrid system may compensate for 500 kVAR of reactive power, the reactive power for which the unit may compensate is graphed in Figure 38 below.

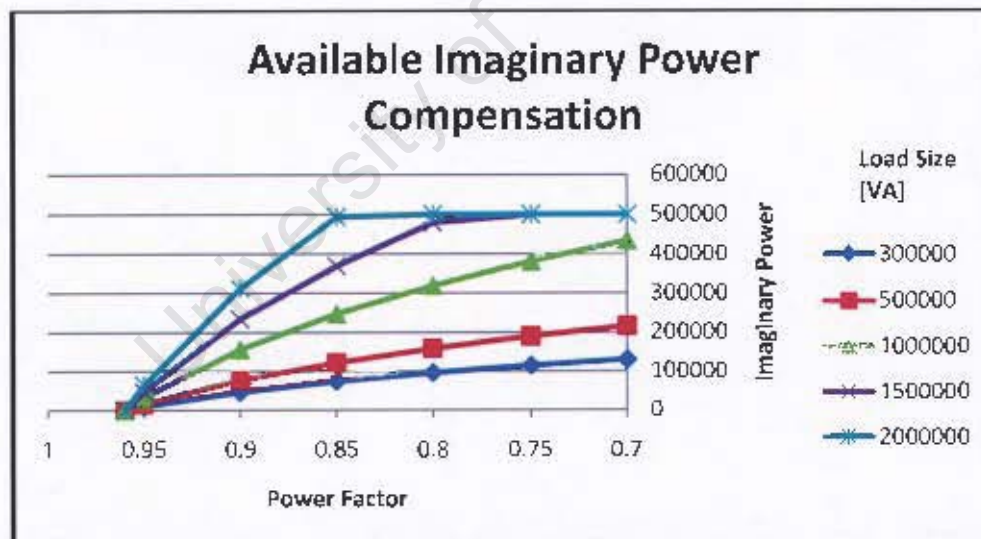


Figure 38: Graph - Available Imaginary Power Compensation of Several Load Sizes Versus Power Factor

By considering the influence that the hybrid system would have on a utility bill should it compensate for all of the above imaginary power in accordance with the 'MINI FLEX' tariff schedule, the monthly savings achieved is graphed in Figure 39.

$$\text{Monthly Saving} = (\text{Access Charge} \times \text{Apparent Power Saving}) + (\text{Reactive Energy Charge} \times \text{Compensated Reactive Power})$$

(6-1)



Figure 39: Graph - Monthly Savings Due to Power Factor Correction Versus Power Factor

By comparing the above monthly savings to the initial capital cost of the system (R91,000.00) as described in the bill of materials and costing, attached as appendix G, the number of months to project break-even may be determined.

$$\text{Months to Break - Even} = \frac{\text{Initial Capital Cost}}{\text{Monthly Saving}} \quad (6-2)$$

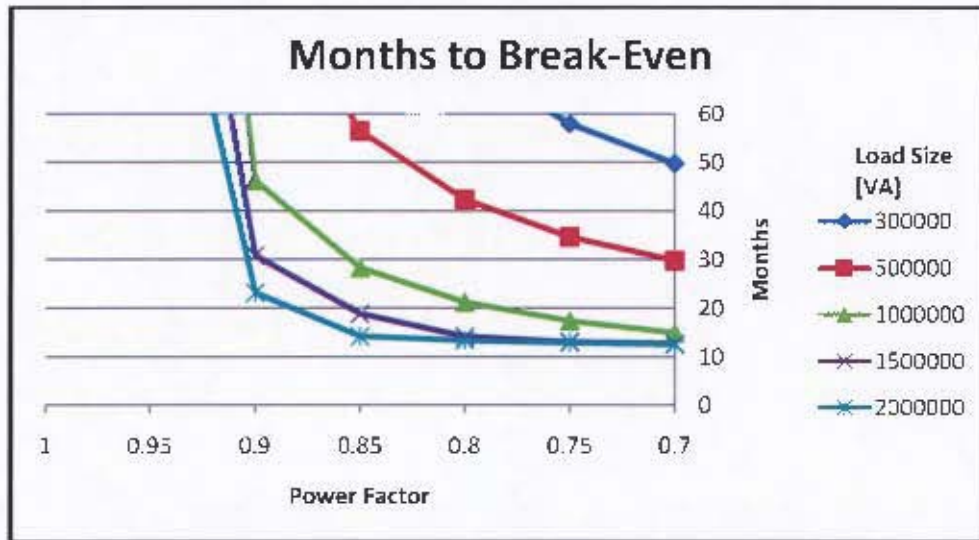


Figure 40: Graph - Months to Break-Even Versus Power Factor

It can be seen in Figure 40 that a large load of 1.5 MVA to 2 MVA at a power factor of 0.8 or worse will take just 12 months to break-even on a cash basis, however, a smaller load, with less imaginary power to compensate for, may take very many more months before it has reached break-even point. It should also be noted that the number of months to break-even increases steeply as each graph nears the 0.96 power factor mark since no charges are applied to imaginary power beyond this power factor.

The total value of the project may now be calculated as an annuity present value since the monthly savings gained will be approximately equal. The value of the annuity is calculated according to the number of months left in the project life after break-even has been attained. It is estimated that the project life-span is 60 months (5 years) - before the unit's contactors will have to be replaced.

$$\text{Annuity Present Value} = C \left( \frac{1-(1+r)^{-t}}{r} \right) \quad (6-3)$$

In the above equation, 'r' is the discount rate of the company, normally linked to the prime lending rate. It is estimated that the discount rate used should be 13.5%, as this is the prime lending rate as of October 2007 (16). 'C' in the above equation is the monthly savings attained, whilst 't' is the number of months left of the project life after

project break-even. It should be noted that a positive annuity present value (APV) indicates a financially viable project whilst a negative one indicates a poor financial investment.

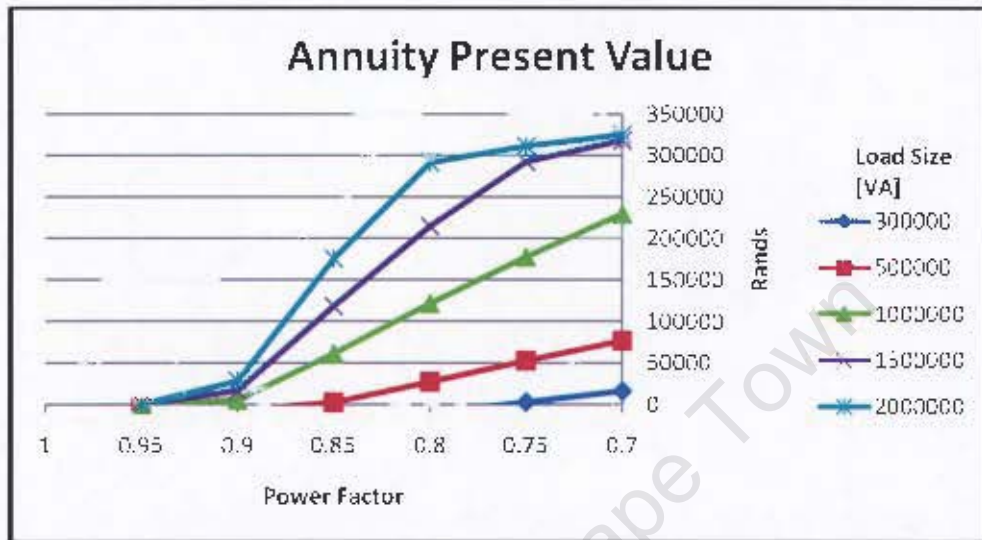


Figure 41: Graph - Project Annuity Present Value Versus Power Factor

Figure 41 shows that for the 1MVA, 1.5 MVA and 2 MVA loads, a positive APV exists indicating a financially viable project. Positive APV's exist also for the 500 kVA and 300 kVA loads, however, because the unit's full capacity is not being made use of, the APV is only positive if the uncompensated loads have very poor power factor to begin with. For the 500 kVA load, a power factor of 0.87 or worse is required before the APV becomes positive, whilst a power factor of 0.77 or worse is required for the 300 kVA load.

Note that at the end of the project life-span, only the contactors will be considered as 'used' since all other components do not degrade with time or usage. As a result, a small additional capital injection could extend the project life-span, thus increasing the APV of each load size.

## **7 Digital Signal Processor Board**

To be able to perform current balancing, the current balancer must be controlled by an intelligent control card that is capable of performing appropriate measurements, calculations as well as event logging. For this, a digital signal processor must be used.

### **7.1 Digital Signal Processor**

The design and implementation of a DSP board is beyond the scope of this project, and thus a readily available DSP card will be used. The DSP card is available from MLT Drives, South Africa (9) and uses the TMS320F2812 processor from Texas Instruments (17).

The TMS320F2812 is a 32 bit, high performance, fixed point processor that can perform 150 million instructions per second. Although this computing power is far beyond the requirements of the project, the DSP board will still be used since:

- The board is readily available
- There is easy access to sample code
- The board provides a stable platform on which to build a system
- Communication and programming software is readily available along with technical support from MLT Drives CC.

An outline of the technical specifications of the TMS320F2812 is listed below; however, a full copy of the technical datasheet is provided on the CD included at the back of this document:

- 32 Bit , fixed point CPU

- On board memory (128KB flash, ROM)
- Serial peripheral interface port
- 2 USART (Universal Synchronous Asynchronous Receiver Transmitter) ports
- 12 bit, 16 channel analogue to digital converter



Figure 42: Photo - DSP Board, Top Side

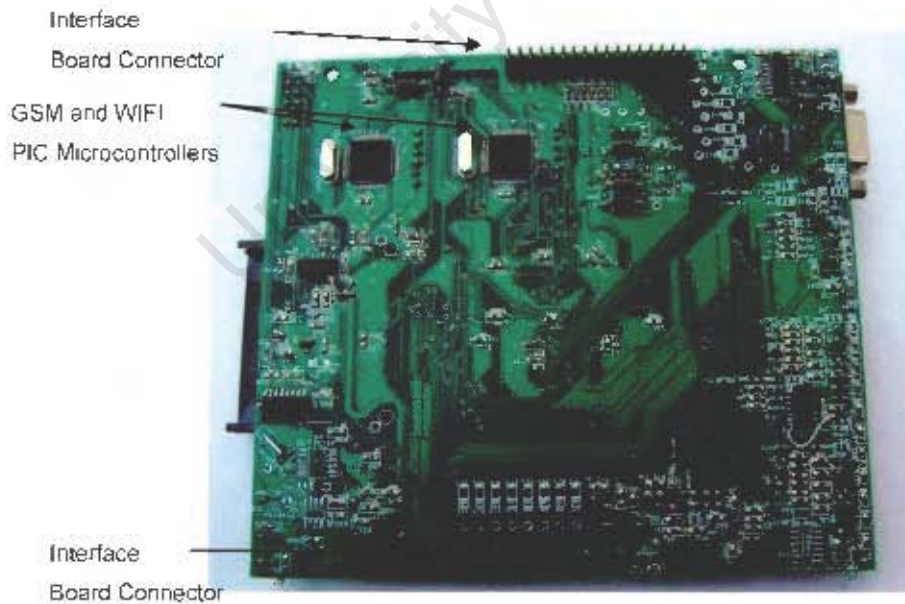


Figure 43: Photo - DSP Board, Bottom Side

As explained in section 8, the DSP board will require an interface card to condition the appropriate system signals and to act as a port expander for the DSP chip. The DSP board will interface with the interface card via two 34 pin connectors, the pin-outs of which are shown in the below schematic:

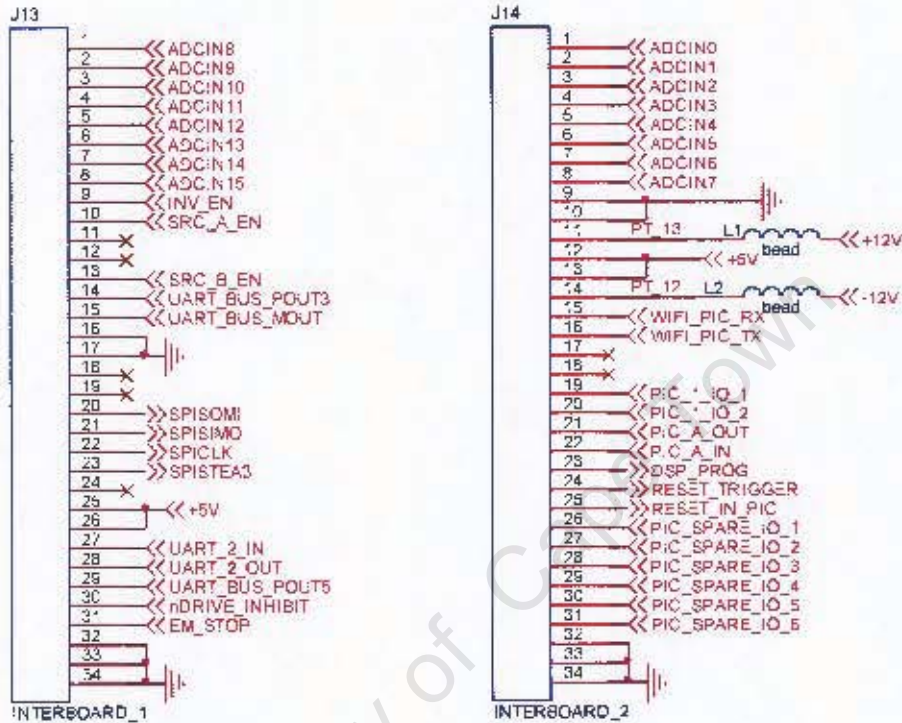


Figure 44: Schematic – Inter-board Connectors

The design of the interface board will thus need to centre on the pin-outs shown in the above schematic. The pin-outs that will be used by the interface board are tabulated below:

Net Name	Description
ADCIN0-7	Analogue to digital converter inputs, for use for current measurements 0-7
ADCIN8-11	Analogue to digital converter inputs, for use for voltage measurements 0-4
ADCIN12	Analogue to digital converter inputs, for use for temperature measurement
ADCIN13-15	Analogue to digital converter inputs, spare inputs to be routed to a connector

Net Name	Description
UART_BUS_POUT3	UART Communications, Peripheral Transmit (out)
UART_BUS_MOUT	UART Communications, DSP (master) out
SPISOMI	SPI Communications, Slave OUT, Master IN.
SPISIMO	SPI Communications, Slave IN, Master OUT.
SPICLK	SPI Communications, Clock source
SPISTEA3	SPI Communications, Slave Transmit Enable
UART_2_IN	UART Communications, DSP Debug Input
UART_2_OUT	UART Communications, DSP Debug Output
EM_STOP	Emergency Stop input.
WIFI_PIC_RX	UART Communications, WIFI PIC Controller Input
WIFI_PIC_TX	UART Communications, WIFI PIC Controller Output
DSP_PROG	IO Line, to Indicate Program Status of DSP and to Silence Communications
RESET_TRIGGER	Hard Reset from Keypad to both MIC Controller and DSP Reset Lines
RESET_IN_PIC	Reset line to the MIC Controller, Driven by the DSP
GND	DSP board ground connection
+5V	DSP Power Supply, 5 Volts
+12V	DSP Power Supply, 12 Volts
-12V	DSP Power Supply, -12 Volts

*Table 8: DSP Inter-board Connectors and Their Functions*

## 7.2 Programming the Digital Signal Processor

The DSP will be programmed in the standard Texas Instruments development environment, 'Code Composer Studio V3.3'. This environment supports the 'C' coding language and compiler for the TMS320F2812 and outputs a HEX file with which to program the DSP core.

The HEX file is placed onto the DSP via a serial port with the use of 'SDFlash', a programmer developed by Texas Instruments.

### **7.3 Available DSP Board Peripherals**

The DSP board itself, available from (9), has a multitude of peripherals, some of which will be useful in this thesis. The board peripherals are detailed below:

- 16 channel, 12 bit ADC inputs
- 3 PWM Ports
- JTAG Interface
- Display Keypad Port
- Compact Flash Connector
- Real Time Clock with super capacitor backup
- RS232 Serial Interface port, two channels
- WiFi PIC Microcontroller
- GSM PIC Microcontroller
- DB9 Serial Modem Port
- Serial Peripheral Interface (SPI)

It should be noted that the Wifi and GSM PIC Microcontrollers are pre-programmed devices and are simply designed to act as an interface between different media and the debug USART port of the DSP.

## **8 Multi-Interface Card Design**

The DSP board accepts signals that are conditioned to within the voltages boundaries of 0 to 3.3 volts. Thus, an interface card is required to condition all voltage, current and temperature signals, as well as to act as a port expander for the DSP board, where ports are available to drive 18 relays and 18 acknowledge lines. Because only a few spare IO lines are available from the DSP board, the multi-interface board requires a microcontroller to act as an intelligent interface to the DSP board, where the microcontroller has at least 36 spare IO ports, after all peripherals have been taken into account.

### **8.1 Microcontroller Requirements**

The microcontroller will be used to drive a host of peripherals independently from the DSP board. These peripherals will mostly form part of a human-machine interface where the fitness, status and set points of the system may be viewed or changed.

#### ***8.1.1 Liquid Crystal Display***

An LCD screen will be driven by the microcontroller to display system information such as present value of unbalance, system set points, load and source statistics (such as real power, imaginary power, apparent power, power factor, line voltages) and calibration points. For this purpose, the LCD chosen for availability, price, size and intelligence is the PC1602-L LCD module from POWERTIP (18). This LCD can display two lines of text at 16 characters per line and has an intelligent interface through which communication to the module is simplified. See included CD for the PC1602-L datasheet and instruction set.

The LCD requires 10 microcontroller IO's; 8 data bus lines, an enable line and a register select line.



Figure 45: Photo - Liquid Crystal Display

### 8.1.2 Keypad

To enable the user to view the various LCD screens, and to be able to edit the system's set points, a small keypad is required. Here, the keypad chosen is a custom made keypad by MLT Drives (9). This keypad was chosen because of its simplicity, cost and availability.

The keypad consists of 6 buttons (Up, Down, Enter, Menu, On/Stdby and Reset), 5 of which will require microcontroller IO's. The reset button will be hardwired to the controller's reset line.



Figure 46: Photo - Keypad

### **8.1.3 Communications**

The DSP board will have to communicate information to the multi-interface board to enable the microcontroller to display information on the LCD module. Another useful function that the MIC board will fulfill is non-volatile storage for the system set points, where the controller must have EEPROM (electrically erasable programmable read only memory), since this is a faster (and easier) storage medium when it comes to code execution than Flash memory. This is because Flash memory generally has to be erased and written to in large blocks, rather than in single bytes (19).

Upon system startup, these set points will be requested for by the DSP and transmitted by the microcontroller for later use. For this reason, the DSP will communicate via a USART (Universal Synchronous Asynchronous Receiver Transmitter) bus, a common feature of modern microcontrollers. For debugging purposes, a second USART bus will also be utilized for debugging purposes through which a computer can be connected via its serial port.

### **8.1.4 Relay and Acknowledge Signals**

As stated before, the MIC board will act like a port expander for the DSP board and will therefore drive all relay signals, as well as accept contactor acknowledge signals. For this, a further 38 controller IO's will be required.

## **8.2 Multi-Interface Board Microcontroller**

One microcontroller that satisfies the requirements set out in section 8.1 is the PIC18F8621 microcontroller by Microchip (20). The PIC18F8621 has the following features, amongst others:

- 80 Input/output pins
- 64 KB Enhanced flash memory
- Up to 10 million instructions per second operation
- Two USART ports

- Master synchronous serial port with SPI (Serial peripheral interface) support
- 8 bit CPU architecture

### 8.3 Schematic Design

See Appendix E for the full MIC board schematic, however, some of the finer details surrounding the design of the MIC board circuitry are shown below along with their calculations.

#### 8.3.1 Board Power Supply

The MIC board will require several voltage levels to be able to run all of the required peripherals. The required levels will be supplied by a multilevel external power supply unit with +5, +12 and -12 volt outputs. These supply voltages will need to be conditioned and filtered as follows:



Figure 47: Schematic - LC Filtering of 12V Power Signal

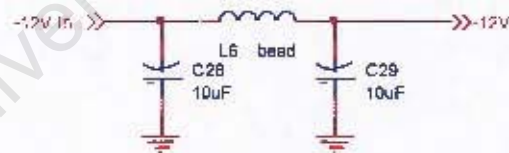


Figure 48: Schematic - LC Filtering of -12V Power Signal

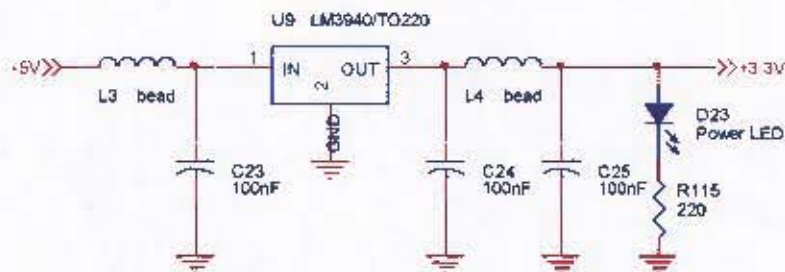


Figure 49: Schematic - Conditioning of +3.3V Power Signal from +5V Power Signal

### 8.3.2 Voltage Measurement Signal Conditioning

The system must be able to measure the grid voltages for logging, information and safety purposes. Thus the MIC board must accept the grid voltages and condition these to a suitable voltage level for the DSP board. Because the DSP's analogue to digital converter accepts an input voltage in the range 0 to 3 Volts, the input voltage signal must be reduced from 230 Volts (line to neutral) to 3 Volts (peak to peak) with a DC offset of half of the ADC voltage (1.5 Volts). The signal is given a 1.5 Volt offset so that the negative half cycle of the voltage waveform remains a positive signal for the DSP's ADC. A potentiometer is added for fine adjustments:

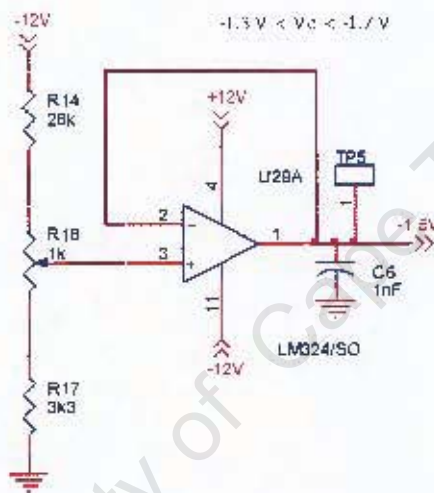


Figure 50: Schematic - 1.5 Volt Offset Supply

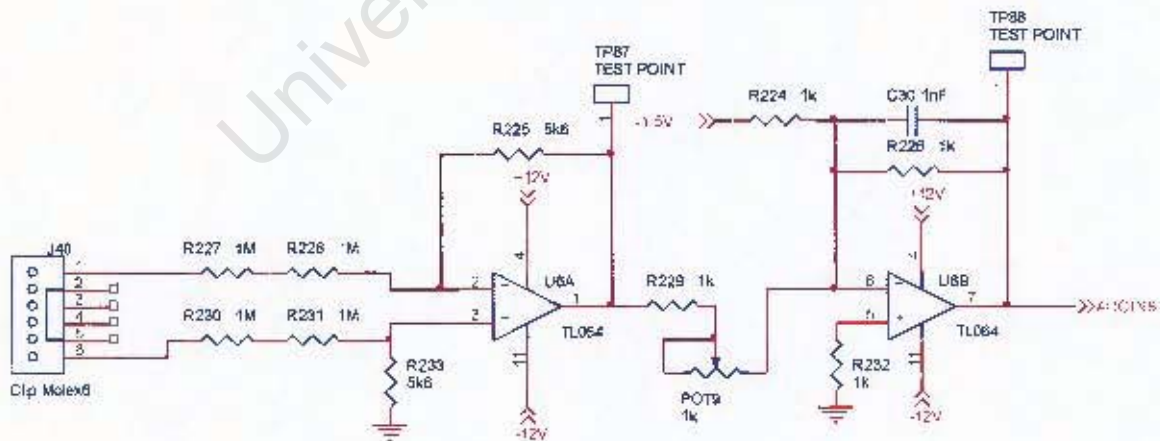


Figure 51: Schematic - Voltage Signal Conditioning Circuitry

It can be seen in Figure 51 that the grid voltage (line to neutral) is inserted directly

into the interface board, on opposing ends of the connector block to minimize the possibility of arcing. The voltage signal is then fed into an inverting differential amplifier followed by a second inverting amplifier with a low pass filter. The second amplifier has been set up with an adjustable gain in the range 0.5 to 1 (for fine tuning). The differential amplifier therefore requires a gain as calculated below:

$$\text{Required Gain} \leq \frac{2\sqrt{3}V_{L-N}}{\text{Max ADC Voltage}} = \frac{2\sqrt{3} \times 230}{3} = 0.00375 \quad (8-1)$$

To ensure that the voltage input sees a high impedance into the MIC board (for safety reasons and for current limiting), the input resistance is set to 2 M $\Omega$ , requiring the differential amplifier to have a resistance of 7500  $\Omega$  or less for resistor R225. Also, to ensure that the voltage waveform never saturates the ADC input during voltage spikes, R225 is set to 5600  $\Omega$ , yielding a gain of 0.00285 for the system. This means that the maximum input voltage for a waveform in the range 0 to 3 V is:

$$\text{Maximum Input Voltage}_{RMS\ L-N} = \frac{1.5}{0.00285\sqrt{2}} = 372\ V \quad (8-2)$$

The TMS320F2812 has a 12 bit ADC, yielding  $2^{12}$  (4096) individual digitized levels. This results in a voltage waveform resolution of:

$$\text{Resolution} = \frac{\text{Maximum Signal Spread}}{\text{Number of Digitised Levels}} \quad (8-3)$$

$$\text{Resolution} = \frac{372 \times 2\sqrt{2}}{4096} = 0.26\ V\ \text{per bit} \quad (8-4)$$

### 8.3.3 Current Measurement Signal Conditioning

Current Measurements of the source and load phases will be made with current transformers on each phase line (note that the sum of the instantaneous line currents gives the neutral current). Typical current transformers are rated to give a secondary current of 5 amperes at maximum primary current (21), whilst the current transformer core is designed for a power transfer of 10 VA. Thus, given these

values, a maximum resistor value can be calculated to develop maximum voltage across the current transformer as follows:

$$P = I^2 R \quad (8-5)$$

$$10 = 5^2 R$$

$$R = 0.4 \Omega$$

The maximum voltage developed over the current transformer is thus:

$$V_{rms} = I_{rms} R = (5)(0.4) = 2 V_{rms} \quad (8-6)$$

$$V_{peak} = 2\sqrt{2} = 2.83 V \quad (8-7)$$

Thus, given that the maximum allowable voltage is 3 V, the conditioning circuitry required should have a gain of 0.5 to allow for a 1.5 volt offset.

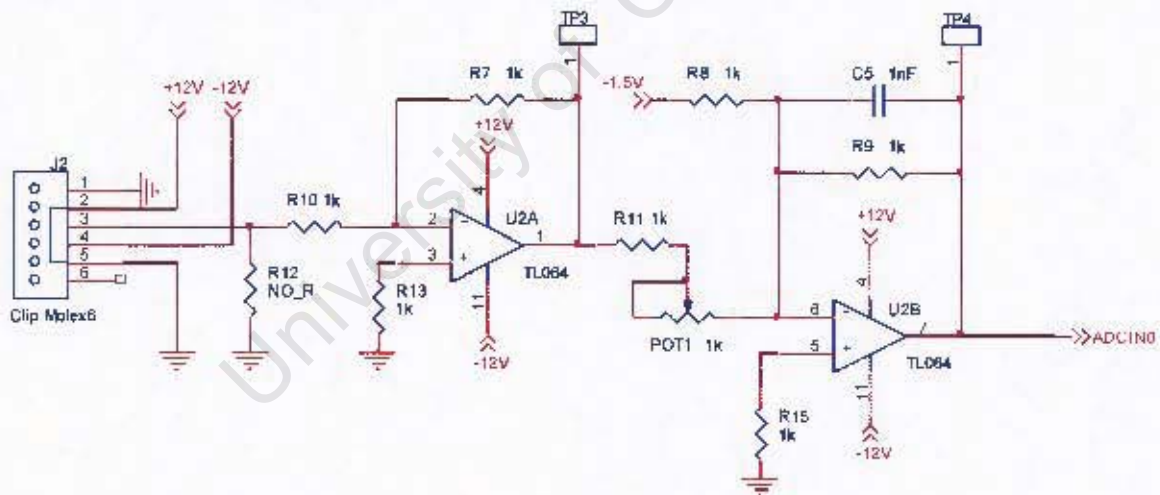


Figure 52: Schematic - Current Measurement Signal Conditioning

The resolution that the ADC achieves for the current measurements then depends on what maximum current the current transformer is rated for (i.e. the turn ratio of the current transformer). This rating will be dependent on the load size, but resolution may be calculated as follows:

$$\text{ADC Volts per Division} = \frac{3}{4096} = 0.73\text{mV per bit} \quad (8-8)$$

$$\begin{aligned} \text{Input Signal Resolution} &= (0.73 \times 10^{-3})(\text{Circuit Gain}) = (0.73 \times 10^{-3})(2) \\ &= 1.46\text{mV per bit} \end{aligned} \quad (8-9)$$

$$\begin{aligned} \text{CT Secondary Current Resolution} &= \frac{(2 \times 3) \div \text{Load Resistor}}{4096} = \frac{6 \div 0.4}{4096} \\ &= 3.66 \text{ mA per bit} \end{aligned} \quad (8-10)$$

$$\text{CT Primary Resolution} = \frac{\text{CT Secondary Current Resolution}}{1/\text{CT Turns Ratio}} \text{ [A per bit]} \quad (8-11)$$

This means that for a 1500 A to 5 A current transformer with 0.4  $\Omega$  load resistor, a resolution of 1.098 A per bit will be achieved.

#### 8.3.4 Relay Drive and Acknowledge Signals

Each contactor will need to be driven with a 220  $V_{L-N}$  signal, driven by the MIC board. This means that the MIC board will need a 220  $V_{L-N}$  supply signal as well as a small PCB mountable relay for each control signal, giving the PIC microcontroller complete isolation from the high voltage signals. A readily available relay that matches the requirement specifications is the Finder 32.21 type relay available from (21). The chosen relay can switch 220  $V_{L-N}$  and requires a 12 V drive signal. Thus, an interface circuit is required between the PIC's IO pin (that outputs 3.3 V) and the relay drive coil. For this, a level shifter is implemented as shown in Figure 53.



### 8.3.5 Completed MIC Board

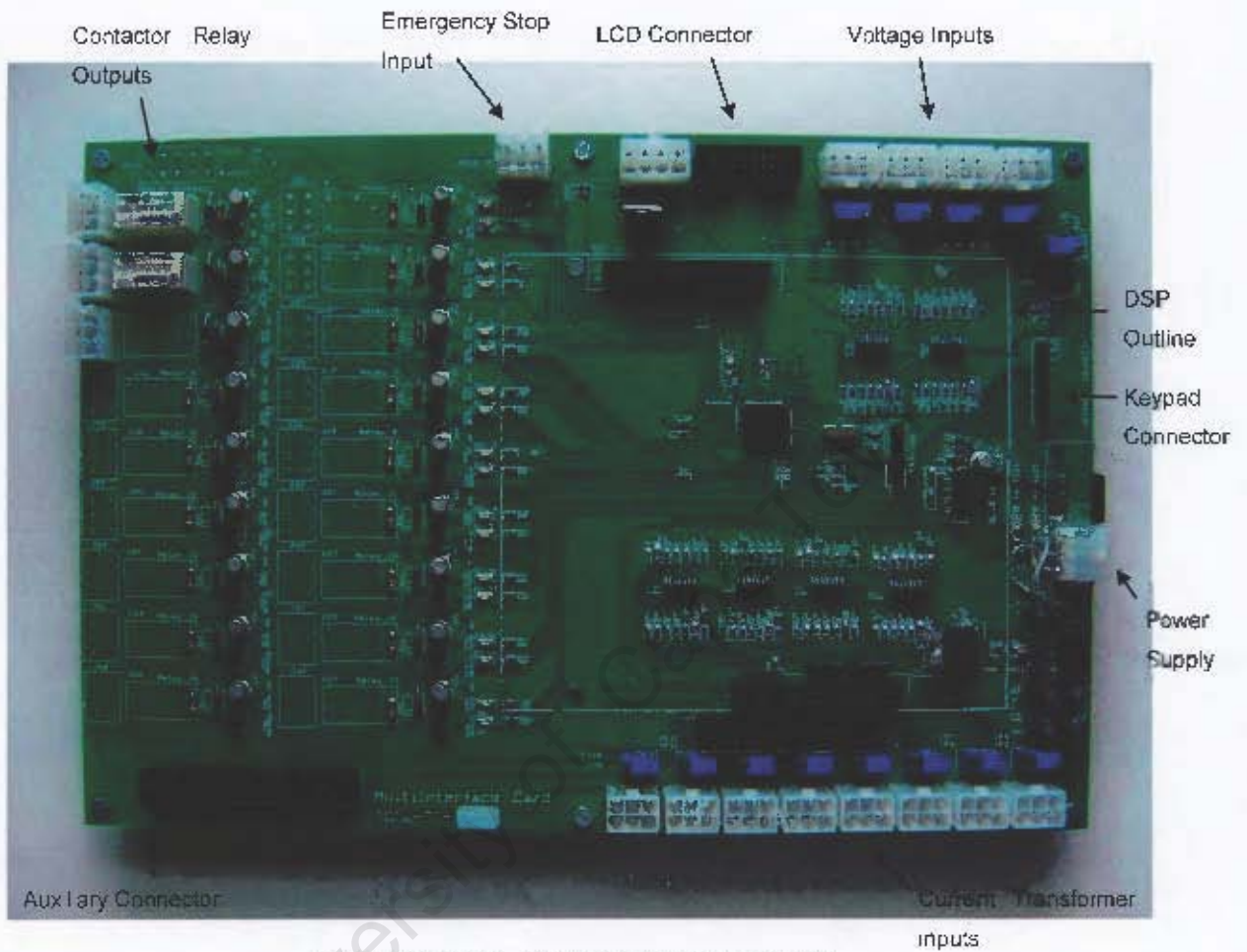


Figure 54: Photo - Completed Interface Board

## **9 Software Design**

### **9.1 Set Point and Data Point Definitions**

As stated in the previous sections, all control algorithms and analogue to digital conversions will take place in the digital signal processor (DSP) where a fast CPU and 12 bit ADC can optimize performance, whereas relay switching, keypad monitoring and liquid crystal display control will be performed by the PIC microcontroller, since these are not time critical processes. Because both controllers need access to some system variables (for example: all variables that are computed by the DSP, but are displayed by the PIC on the LCD screen), these variables will have to be communicated, via the USART port from one processor to the other. For this purpose, and for ease of communications, these variables will be split into two parts; variables that continuously change and that do not need to be stored in non-volatile memory will be stored in a 'data point table', whilst variables that are user settable, define how the system operates and need to therefore be stored in non-volatile memory will be stored in a 'set point table'. Before software code development can take place, these set points and data points must be defined to ensure code consistency; see appendix F for the set point and data point table defines and their descriptions.

### **9.2 MIC PIC Microcontroller Software**

As described in section 8, the PIC microcontroller must perform the following duties:

- Store system set points in non-volatile memory.
- Monitor the system keypad for button presses, de-bounce button presses.
- Write to the LCD.
- Operate a menu structure for the LCD screen.
- Monitor USART port for communications with the DSP.
- Monitor acknowledge lines from all inputs (contactors).
- Drive relay control signals.
- Monitor USART2 port for debug via RS232 to a personal computer.

### 9.2.1 Software Overview

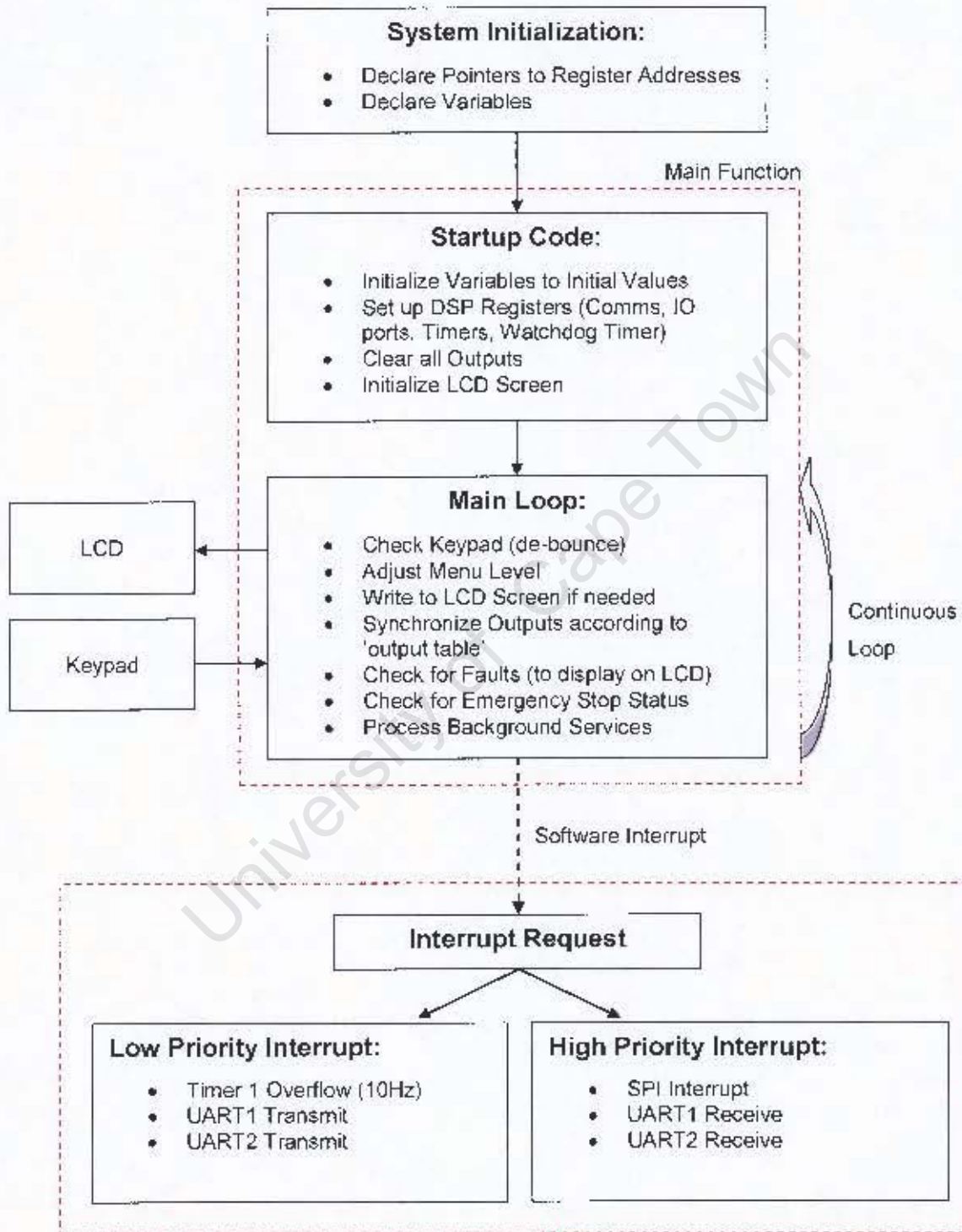


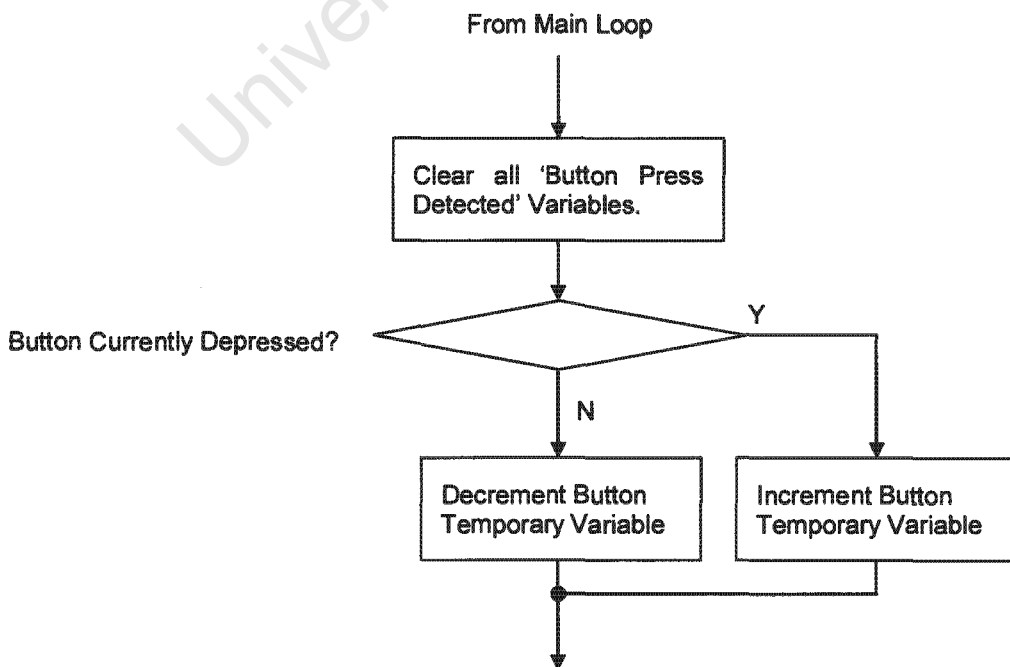
Figure 55: Flowchart - PIC Software Overview

Figure 55 above shows the PIC software overview in flowchart form. It can be seen that when the PIC starts up, it runs through several initialization commands, during which time all variables are set to initial values whilst all timer registers, communication channel registers and input/output ports are set to the correct values. The LCD screen is also initialized and all outputs are set to 'off' or 'low' so that all relays are off upon startup.

Once these are correctly setup, the system enters its infinitely recurring main loop, in which all run-time functions are called. In the main loop, the controller checks for keypad presses by examining the IO port associated with that key, adjusts the menu level according to a possible keypad press, writes to the LCD screen every second or every keypad button press (whichever comes first), synchronizes all output signals with the status of an output table sent by the DSP, checks for any fault status or emergency stop requests and processes all other background services (UART receive buffer, clear the watchdog timer).

### 9.2.2 Keypad Button Press Detection and De-Bounce Software

The flowchart below illustrates the keypad button press detection software and how its de-bounce routines operates, the function is called once every time the main loop runs:



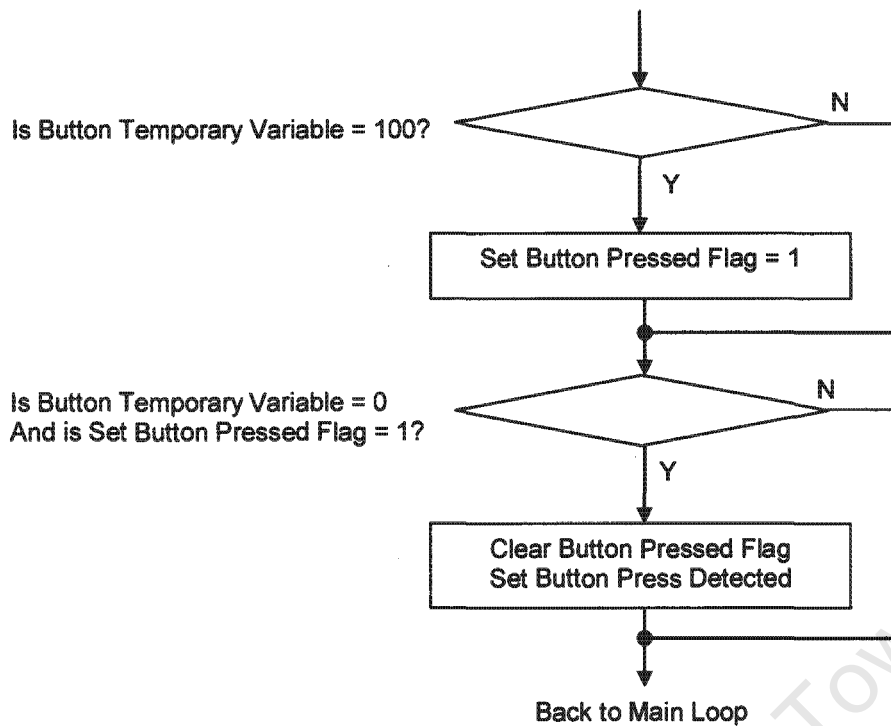


Figure 56: Flowchart - Keypad Button Detection and De-Bounce

It can be seen in Figure 56 above that the user must press and hold the keypad button for 100 cycles of the main software loop (this will be a short time by human standards), once 100 cycles are completed, a flag is set. The user must now release the button, which will decrement the temporary variable back down to zero over another 100 main loop cycles. Once the temporary variable has reached zero, and the button pressed flag is set, an actual button press is detected. This means that the actual button press is 'detected' once the user releases the button only and prevents multiple button presses should the user hold the button down over a long period.

### 9.2.3 LCD Menu Structure Flowchart

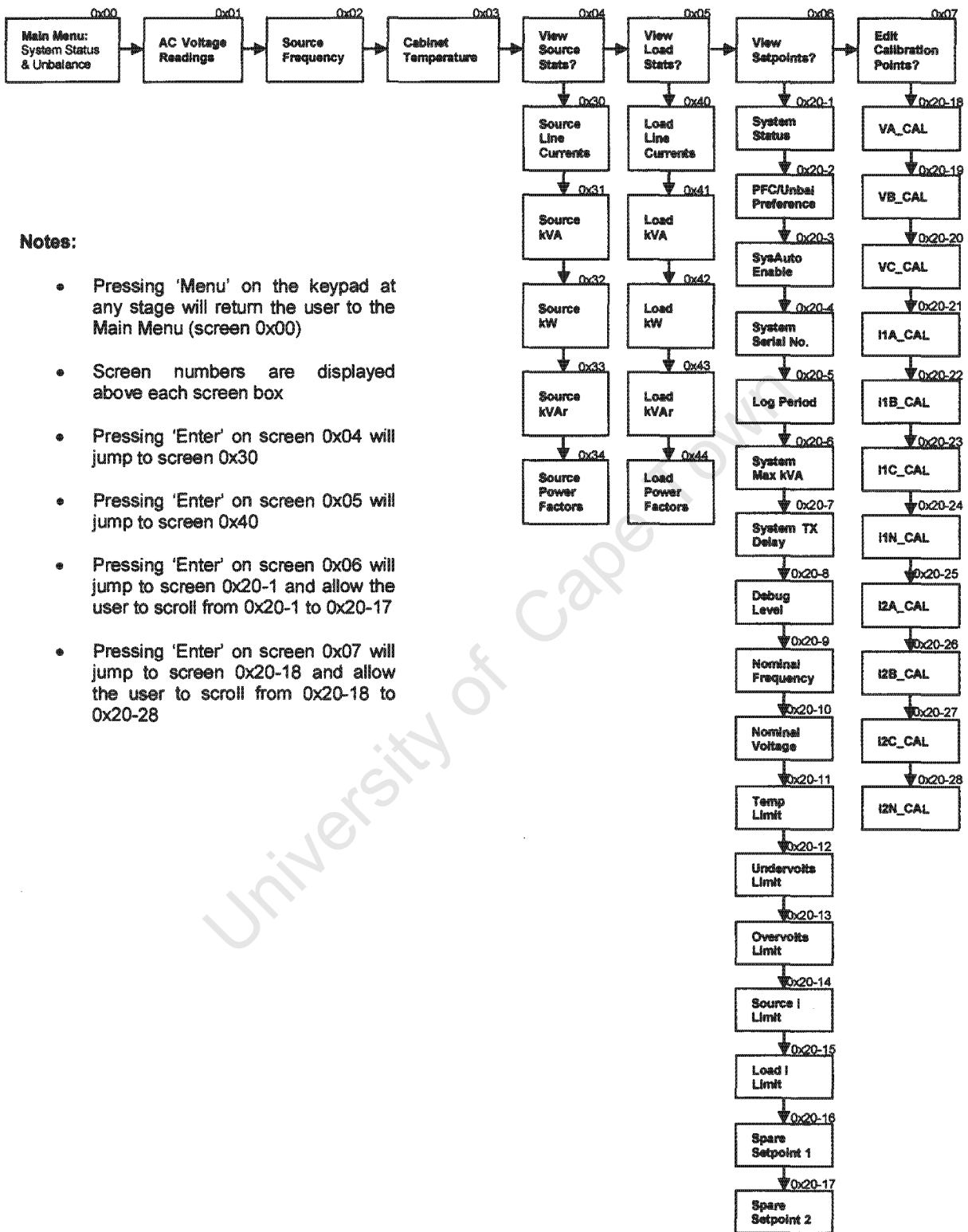


Figure 57: Flowchart - Menu Structure Diagram for LCD Screen

Figure 57 shows the LCD menu structure required to display all set points, calibration points and statistics. It was stated in section 8.1.2 that the keypad has an 'on/stdby' button, which can be used to alternate the system from 'run' mode to 'standby' mode. This button may only operate on menu level 0x00 (the home menu) so that the user does not mistakenly activate the system. Set points must also be user settable via the keypad and LCD and thus if 'Enter' is pressed on any screen that is displaying a set point, the LCD curser will become active (flashing) and by pressing 'up' or 'down' adjust the set point value. For this, a hidden screen is required – screen 0x21. The operation of the set point editor (screen 0x21) is illustrated below:

Assume, set point 'x' is being viewed on screen 0x20-x

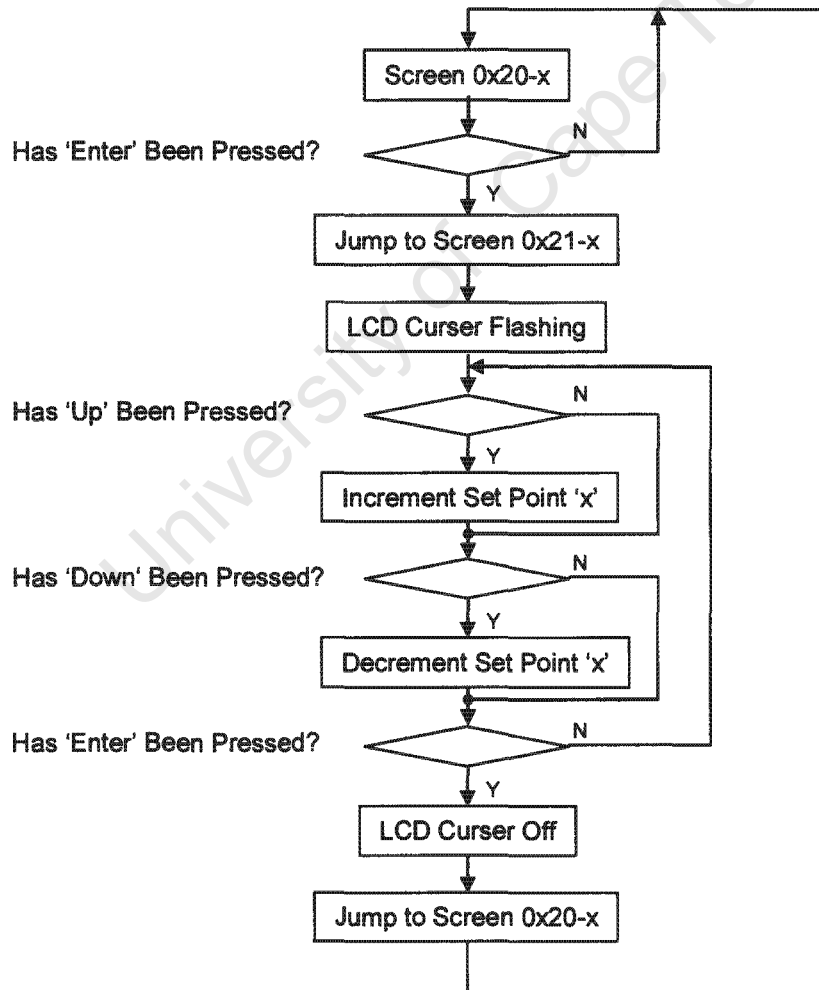


Figure 58: Flowchart - LCD Screen Set point Editor

#### 9.2.4 LCD Module Interface and Control

As described in section 8.1.1, the LCD module used for the user interface is the PC1602-L module from (18). This module can display two lines of text with 16 characters per line and is controller with an intelligent controller – based on the HD44780 LCD module controller (22). The LCD pin-outs according to the manufacturer's datasheet (18) are tabulated below:

Pin No.	Symbol	Function
1	$V_{ss}$	Power Supply – Ground
2	$V_{dd}$	Power Supply – Positive
3	$V_o$	Contrast Adjust
4	RS	Register Select Signal
5	R/W	Data Read/Write
6	E	Enable Signal
7	DB0	Data Bus Line
8	DB1	Data Bus Line
9	DB2	Data Bus Line
10	DB3	Data Bus Line
11	DB4	Data Bus Line
12	DB5	Data Bus Line
13	DB6	Data Bus Line
14	DB7	Data Bus Line

Table 9: LCD Module Pin-outs

- Pin number 4, the register select signal, is used to tell the LCD controller if a command is being written to the controller (if RS = 0), or if a character is being written to the screen itself (if RS = 1).
- Pin number 5, the data read/write line, must be logic high to be able to read text from the LCD module and logic low to be able to write to it. Since text will always be written to the module in this project, this line will be pulled to logic low (ground) via a pull-down resistor.
- Pin number 6, the enable signal, is used to tell the LCD module controller when to clock the data put onto the data bus (pins 7 to 14) and will therefore be controlled by a PIC IO line.

To save on the number of IO pins required to drive the LCD module, it is possible to use the module in 4 bit mode, where all instructions and characters are written to the controller in two halves (four bits each). If IO pins are not in short supply (as in this instance), the module can also be written to in 8 bit mode, a much faster communication method that utilizes all LCD module pin-outs. LCD Initialization is accomplished as shown below:

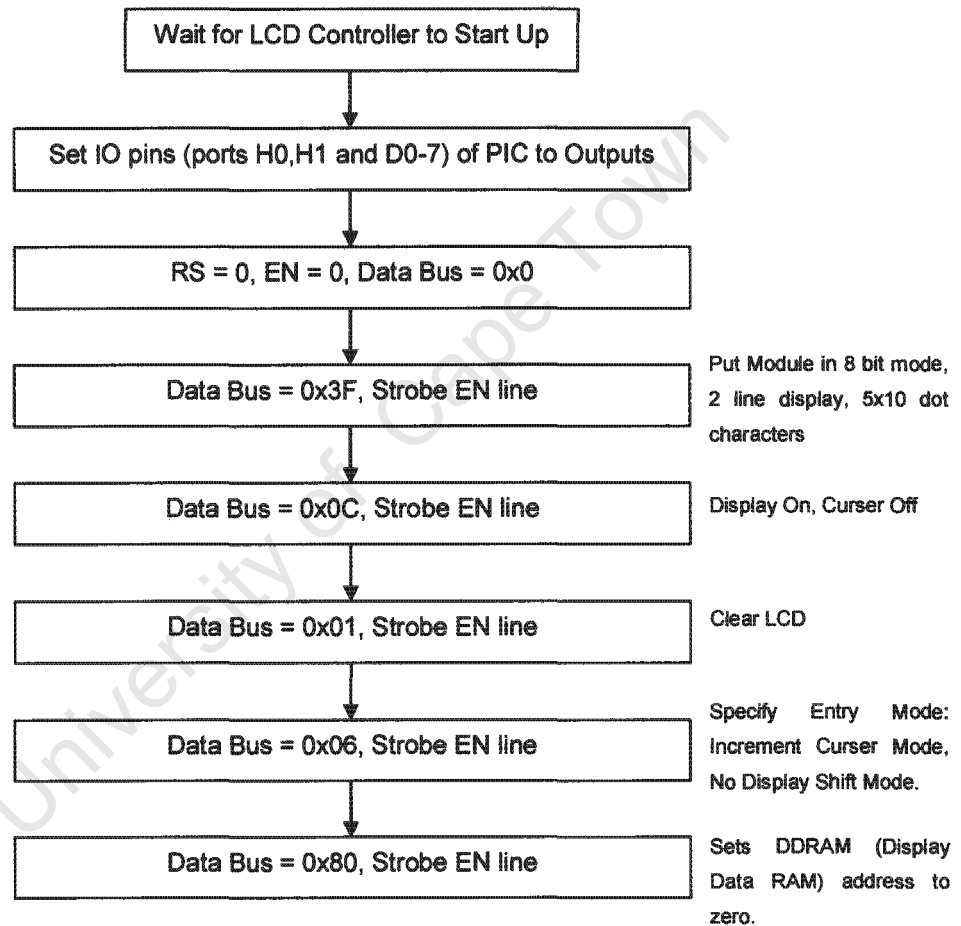


Figure 59: Flowchart - LCD Initialization

Once the initialization routine has been completed, data (represented by 'NN') may be written to the screen as shown in the below flowchart:

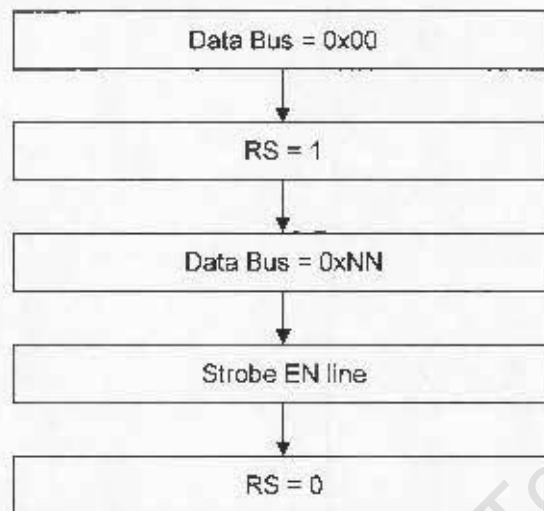


Figure 60: Flowchart - Writing Characters to LCD Module

Where 'NN' represents high and low nibbles of the character byte as shown in the ASCII table below:

Char. code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
xxxx0001	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
xxxx0010	W	X	Y	Z	[	\	]	^	_	`	a	b	c	d	e	f
xxxx0011	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v
xxxx0100	w	x	y	z	{		}	~	?							
xxxx0101																
xxxx0110																
xxxx0111																
xxxx1000																
xxxx1001																
xxxx1010																
xxxx1011																
xxxx1100																
xxxx1101																
xxxx1110																
xxxx1111																

Figure 61: ASCII table for LCD Characters

### 9.2.5 Output and Input Tables

Because calculations and switching algorithms are performed by the DSP, the DSP must communicate via USART the required status of all outputs, as well as request the status of all inputs to and from the MIC PIC. For this purpose, two tables will be created, an output table and an input table. The required status of all outputs (output 0 to output 17) will be stored by the DSP in the output table, the status of which is transmitted to the MIC PIC every time an entry in the output table changes. Because a software reset of either PIC or DSP may cause the output tables stored by each party to get out of synchronization, the entire table will be resent by the DSP, irrespective of status changes, every ten seconds. A similar system is utilized for the input table, where the PIC records the status of its input pins in the input table and transmits any status changes to the DSP. Again, the entire input table will be resent, irrespective of status changes, to the DSP every ten seconds.

### 9.2.6 System Faults, Fault Conditions and Fault Handling

To be able to protect the system, and for safety reasons, the system must recognize a host of fault situations and take actions appropriate to protect the system. To be able to communicate fault conditions to the user (to be displayed on the LCD screen), fault conditions must be transmitted to the PIC. To ensure simple, fast code, the fault conditions will be encoded onto a data point variable (data point no. 53) by associating each bit of the 'fault' variable with a fault condition. Because the data point table is a 16 bit variable, 16 different fault conditions may exist (they may exist simultaneously). Possible fault conditions are listed below along with their required actions:

<b>Fault Code:</b>	<b>0x0001 = 0000 0000 0000 0001</b>
<b>Fault Name:</b>	<b>High <math>V_{ab}</math></b>
<b>Condition:</b>	<b><math>V_{ab\_rms} &gt; \text{OverVolts set point}</math></b>
<b>Action:</b>	<b>Remove all capacitors from utility grid, display "Fault: High <math>V_{ab}</math>" on LCD Screen, Log fault, Wait for user to clear fault by pressing 'Enter' on system keypad.</b>

**Fault Code:** 0x0002 = 0000 0000 0000 0010  
**Fault Name:** High  $V_{bc}$   
**Condition:**  $V_{bc\_rms} > \text{OverVolts set point}$   
**Action:** Remove all capacitors from utility grid, display "Fault: High  $V_{bc}$ " on LCD Screen, Log fault, Wait for user to clear fault by pressing 'Enter' on system keypad.

**Fault Code:** 0x0004 = 0000 0000 0000 0100  
**Fault Name:** High  $V_{ca}$   
**Condition:**  $V_{ca\_rms} > \text{OverVolts set point}$   
**Action:** Remove all capacitors from utility grid, display "Fault: High  $V_{ca}$ " on LCD Screen, Log fault, Wait for user to clear fault by pressing 'Enter' on system keypad.

**Fault Code:** 0x0008 = 0000 0000 0000 1000  
**Fault Name:** Low Line Frequency  
**Condition:**  $\text{Src Frequency} < \text{System Nominal Frequency} - 10\%$   
**Action:** Remove all capacitors from utility grid, display "Fault: Low Src Freq" on LCD Screen, Log fault, Wait for source frequency to come back within specification, then restart control algorithm.

**Fault Code:** 0x0010 = 0000 0000 0001 0000  
**Fault Name:** High Line Frequency  
**Condition:**  $\text{Src Frequency} > \text{System Nominal Frequency} + 10\%$   
**Action:** Remove all capacitors from utility grid, display "Fault: High Src Freq" on LCD Screen, Log fault, Wait for source frequency to come back within specification, then restart control algorithm.

**Fault Code:** 0x0020 = 0000 0000 0010 0000  
**Fault Name:** Cabinet Over Temperature  
**Condition:**  $\text{Cabinet Temperature} > \text{Temperature Limit}$   
**Action:** Remove all capacitors from utility grid, display "Fault: Over Temp" on LCD Screen, Log fault, Wait for cabinet temperature to come back within specification, then restart control algorithm.

**Fault Code:** 0x0040 = 0000 0000 0100 0000  
**Fault Name:** Phase Rotation Error  
**Condition:** ( $V_b < 0$ ) and ( $V_c > 0$ ) at zero crossing of  $V_a$   
**Action:** Remove all capacitors from utility grid, display "Fault: Phase Rotation" on LCD Screen, Log fault, wait for user to swap phase rotation and clear fault by pressing 'Enter' on system keypad.

**Fault Code:** 0x0080 = 0000 0000 1000 0000  
**Fault Name:** Source Over Current  
**Condition:** Any Source Phase Current<sub>RMS</sub> > Source Maximum Current  
**Action:** Remove all capacitors from utility grid, display "Fault: Src Over Current" on LCD Screen, Log fault, wait for user to clear fault by pressing 'Enter' on system keypad.

**Fault Code:** 0x0100 = 0000 0001 0000 0000  
**Fault Name:** Load Over Current  
**Condition:** Any Load Phase Current<sub>RMS</sub> > Load Maximum Current  
**Action:** Remove all capacitors from utility grid, display "Fault: Load Over Current" on LCD Screen, Log fault, wait for user to clear fault by pressing 'Enter' on system keypad.

### 9.2.7 Emergency Stop

As shown in the MIC board schematics (appendix E), the emergency stop button is connected directly to a DSP IO line. The DSP will check the status of the emergency stop once every loop of the DSP's main loop for fast response. Should the emergency stop function be activated, all output states in the output table will be set to zero and a data table variable, EM\_STOP\_EN, will be set to one. This will allow the MIC PIC to quickly receive the emergency stop status and remove all capacitors from the utility grid whilst displaying "Emergency Stop Activated" on the LCD. Contactors may not be inserted manually or automatically once in this state. The user must reset the system by releasing the emergency stop latch, once this is done, the system will return to its standby state.

### 9.3 DSP Controller Software

The DSP board peripheral functions were described in section 7.3 however, not all of these peripherals will be needed for this thesis and may thus be neglected. All PWM, display keypad and JTAG ports may be neglected whilst all other functions will have to be accounted for when designing the software for the DSP core.

#### 9.3.1 DSP Software Overview

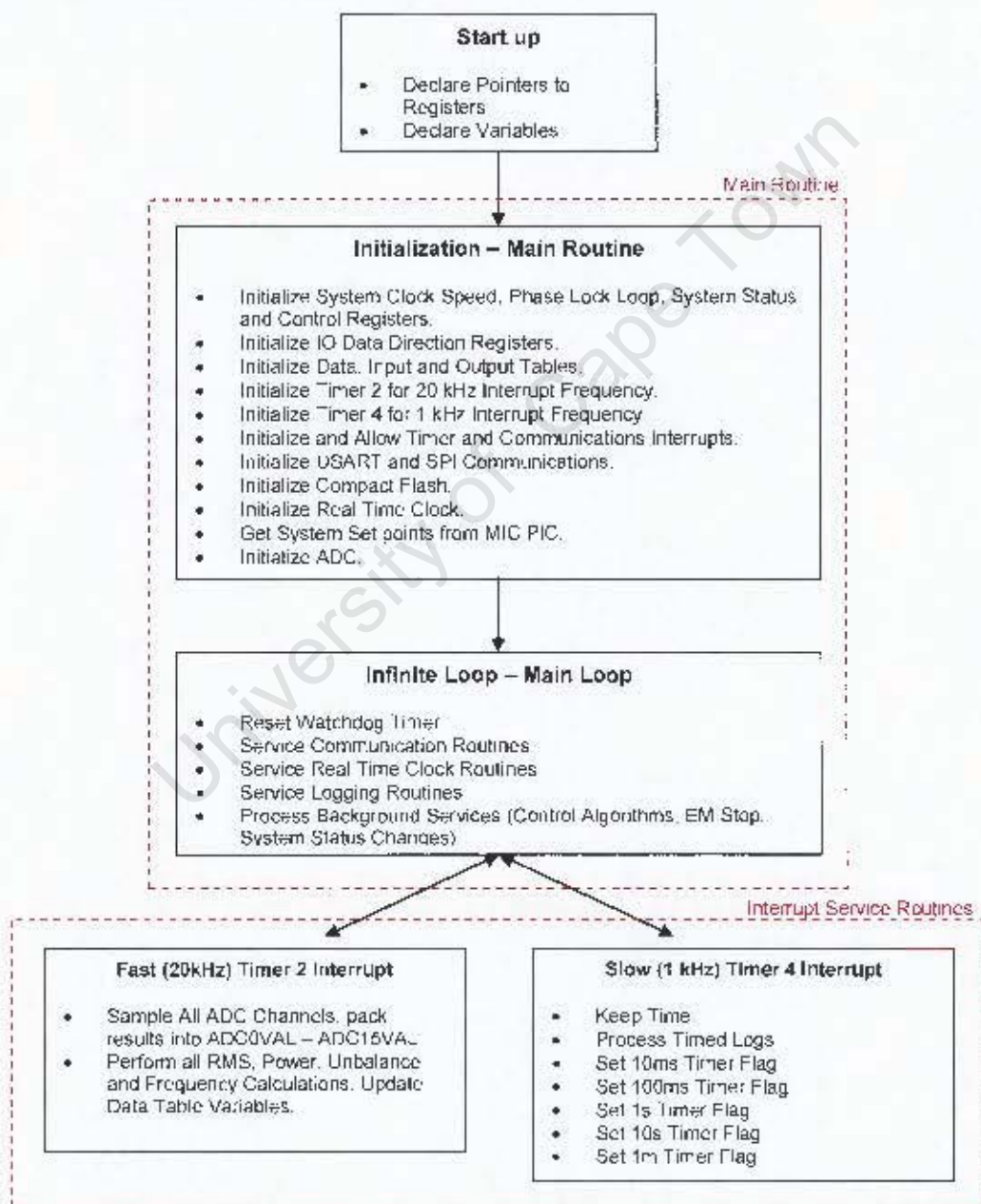


Figure 62: Flowchart - DSP Software Overview

Figure 62 above outlines the DSP control software to be run on the TMS320F2812 DSP core. The DSP board is populated with a 30 MHz quartz crystal for the system clock, the DSP core is also fitted with a built in phase lock loop, used to multiply the clock frequency up to 150 MHz (by dividing the feedback loop of the phase locked loop by 5). This achieves the rated 150 million instructions per second speed rating of the DSP core.

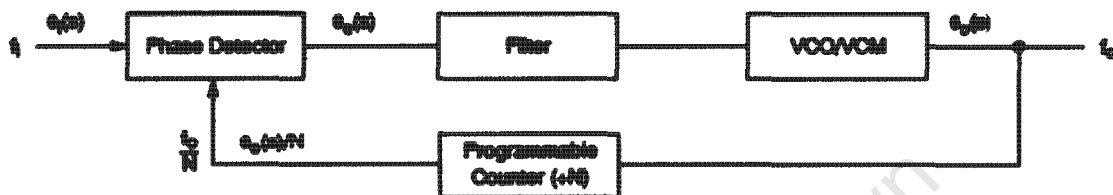


Figure 63: Phase Locked Loop Block Diagram (23)

The DSP core is also fitted with multiple timers, four of which are general purpose, 16 bit timers. General purpose timers 2 and 4 will be used to keep system timing (since these two timers are on different event managers), where timer 2 will be used to keep a 20 kHz interrupt frequency whilst timer 4 will be used to keep a 1 kHz interrupt frequency.

ADC conversions will thus be requested by the timer 2, 20 kHz interrupt to allow for accurate waveform readings whilst all timer flags (10ms, 100ms, 1s, 10s and 1m) are set by the 1 kHz interrupt routine.

### 9.3.2 System Timing

Section 9.3.1 explains that the DSP core clock input is driven by a 30 MHz quartz crystal. This reference signal is then fed into a phase locked loop that multiplies the clock frequency up to 150 MHz. Using this clock frequency, all other peripheral clock frequencies must be derived, along with the event manager (general purpose timers). Before the system clock is fed to the peripheral clocks, it undergoes a divide by two as shown in Figure 64.

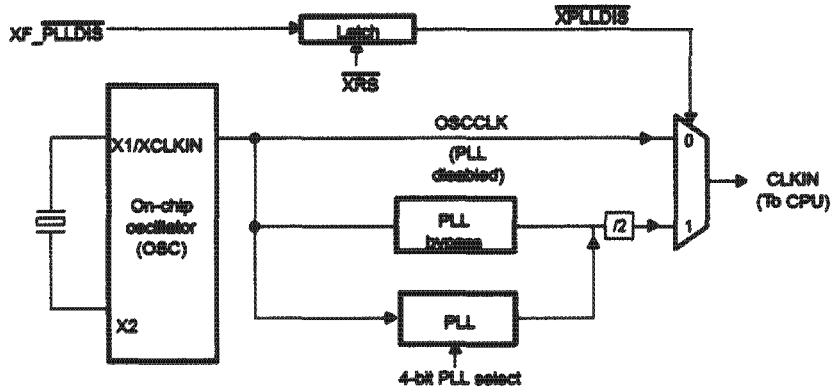


Figure 64: DSP System Clock and PLL Block Diagram (24)

It is shown in (24) that all DSP peripherals are split up into two groups, a high speed group (such as the event managers) and a low speed group (such as the SCI and SPI modules). Each group is run off its own clock source, derived from the CPU clock source, 'CLKIN', and each with its own settable clock pre-scalar. Taking the above information into consideration, the clock speeds may be calculated as follows:

$$\text{SysCLKOUT} = \frac{\text{XCLKIN} \times \text{PLL divider}}{2} = \frac{30 \times 10^6 \times 10}{2} = 150 \times 10^6 \text{ Hz} \quad (9-1)$$

$$\text{Hi Speed Clock} = \frac{\text{SysCLKOUT}}{\text{Hi Speed Prescalar}} = \frac{150 \times 10^6}{6} = 25 \times 10^6 \text{ Hz} \quad (9-2)$$

$$\text{Lo Speed Clock} = \frac{\text{SysCLKOUT}}{\text{Lo Speed Prescalar}} = \frac{150 \times 10^6}{6} = 25 \times 10^6 \text{ Hz} \quad (9-3)$$

Because the event manager peripherals receive their clock sources from the hi speed clock source (running at 25 MHz), the number of timer cycles required to create a 20kHz and a 1kHz interrupt is shown below:

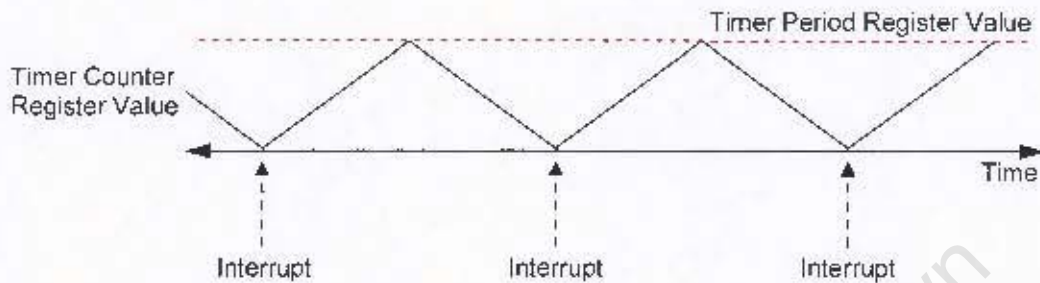
$$\text{Timer Cycles} = \frac{\text{Clock Frequency}}{\text{Required Interrupt Frequency}} \quad (9-4)$$

$$20\text{kHz Interrupt Clock Cycles} = \frac{12.5 \times 10^6}{20000} = 1250 \quad (9-5)$$

$$1\text{kHz Interrupt Clock Cycles} = \frac{12.5 \times 10^6}{1000} = 25000 \quad (9-6)$$

Both timers 2 and 4 will be set up into a continuous up/down count mode, where the

timer register counts from zero up to the value in the period register, and then back down to zero again where the process repeats. When the timer counter register reaches zero each time, an interrupt is generated which will then activate the ADC (if it is timer 2) or increment time flags (if it is timer 4).



Because the timer counter register must count up to the timer period register and down again each cycle, the process of which must take precisely 1250 clock cycles for a 20 kHz interrupt, then the timer 2 period register must be loaded with a value of 1250/2 or 625. The same system applies for the 1 kHz interrupt, where the timer 4 period register must be loaded with a value of 25000/2 or 12500.

### 9.3.3 USART Communications and Protocol

To be able to communicate to the MIC PIC, the DSP will utilize its USART port, as described in section 8.1.3. For this, the USART port will be set to 8 bit character mode, at 115200 baud rate. The baud rate may be calculated as a function of the low speed peripheral clock and the BRR bits in the SCIHBAUD and SCILBAUD registers, as shown below (25):

$$BRR_{decimal} = \frac{LSPCLK}{Baud\ Rate \times 8} = \frac{25 \times 10^6}{115200 \times 8} - 1 = 26 = 0x001A \quad (9-7)$$

This will allow the DSP to transmit bytes of information to the MIC PIC (and vice versa). Some form of communication protocol must now be formed such that particular command bytes yield some desired response from either party. For this purpose, the communication protocol formed by (9), the DSP board manufacturer,

will be utilized since this protocol has been field tested and found to be a robust, flexible system. The full protocol has been included on the attached CD.

### 9.3.4 Analogue to Digital Converter

The TMS320F2812 has a 16 channel, 12 bit analogue to digital converter capable of a maximum sample rate of 12.5 MSPS (mega samples per second), equivalent to an 80 ns conversion time (depending on clock speed). The ADC clock speed may be scaled by the ADCLKPS and ADCTRL registers as shown below:

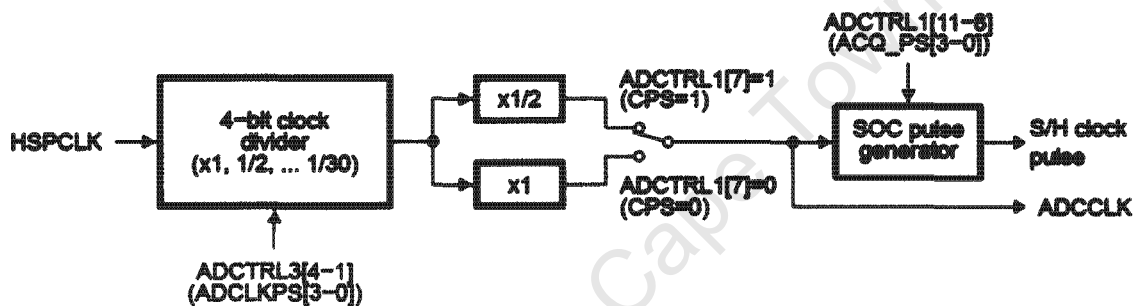


Figure 65: Block Diagram - ADC Clock Chain (26)

The ADCTRL3[bits 4-1] register will be set to have a clock pre-scalar of 2, whilst the ADCTRL1[bit 7] will be set to '1' resulting in an ADCCLK frequency of  $HSPCLK/4 = 6.25 \text{ MHz}$ . The ADC requires an acquisition time before each sample can take place, this time allows the system's sample and hold circuitry to charge to the sampled signal's voltage for an accurate sample. The acquisition time can also be set via software and will be set to 17 clock cycles by writing 0xF to ADCTRL1[bits 11-8]. This will result in an acquisition time of  $(17 \times (1/6.25 \times 10^6)) 2.72 \mu\text{s}$  and a conversion time of  $(18 \times (1/6.25 \times 10^6)) 2.88 \mu\text{s}$ . If 16 signals are sampled at each ADC start of conversion, then total conversion time is  $46.08 \mu\text{s}$ , resulting in a maximum conversion frequency of 21 700 Hz. The ADC start of conversion will thus be able to be called at a frequency of 20 kHz by the 20 kHz timer 2 interrupt.

The ADC will thus sample all 16 ADC channels every 50 us, and process the information of the result registers accordingly. Because many of the ADC channels

are given a 1.5 volt DC offset (to be able to measure AC waveforms), the ADC process code will thus remove this offset according to a long term average of the sampled waveform. This will result in a very accurate representation of the sampled waveform with zero DC offset. The process of ADC channel 'n' is shown in the below flowchart:

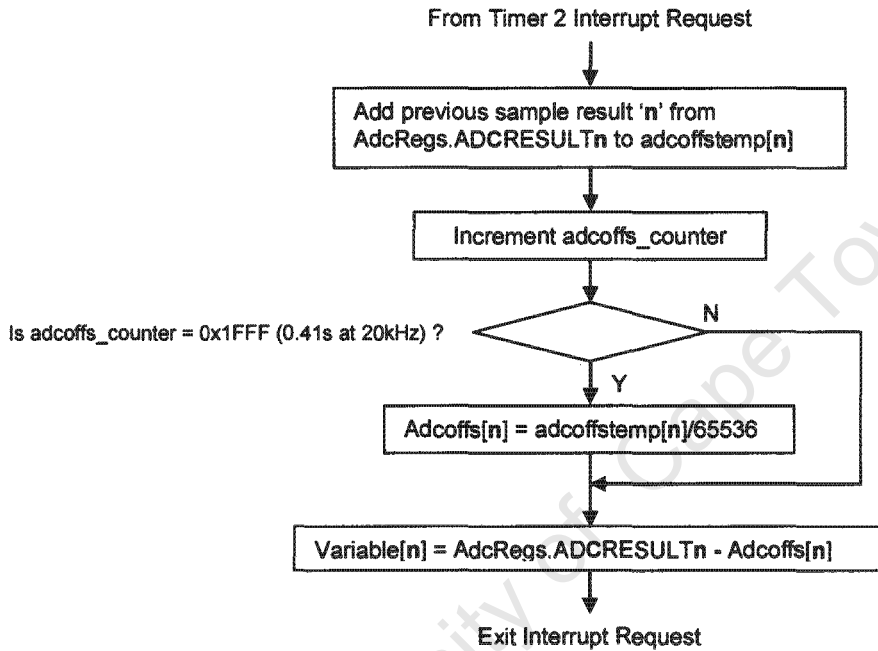


Figure 66: Flowchart - ADC Sampling

The ADC interrupt request thus returns the instantaneous value of the waveform at ADC input 'n' with all DC offsets removed. A calibration factor may now also be added to the sampled waveform where the instantaneous value is multiplied by a value, 'x', and divided by 1024 ( $2^{10}$ ). The user may thus set the calibration factor 'x' to either increase or decrease the sampled waveform by a factor ( $x/1024$ ).

The waveform RMS value may now be calculated for use in the control algorithms. For this calculation, the instantaneous waveform must be squared, and the mean of the square taken over a long term average as shown below:

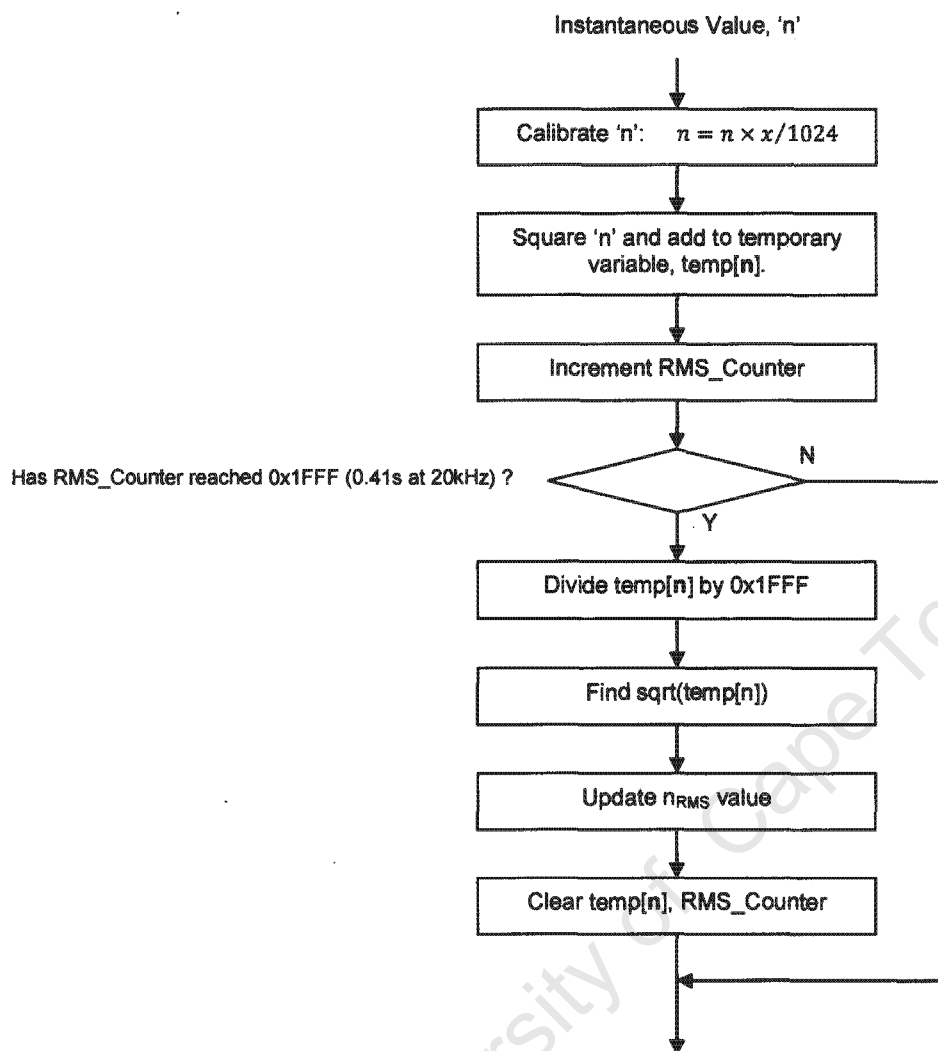


Figure 67: Flowchart - RMS Calculations

### 9.3.5 Unbalance Measurement

It was stated in (27) that the negative and positive sequence currents may be calculated by using the following formulae, where 'T' is the period of the waveform being examined and  $I_{\alpha}$ ,  $I_{\beta}$  are calculated with the Clarke transform (see appendix B):

$$I_{\alpha}^{+} = I_{\alpha} - I_{\beta} \left( t - \frac{T}{4} \right) \quad (9-8)$$

$$I_{\beta}^{+} = I_{\alpha} \left( t - \frac{T}{4} \right) + I_{\beta} \quad (9-9)$$

$$I_{\alpha}^{-} = I_{\alpha} + I_{\beta} \left( t - \frac{T}{4} \right) \quad (9-10)$$

$$I_{\beta}^{-} = -I_{\alpha} \left( t - \frac{T}{4} \right) + I_{\beta} \quad (9-11)$$

To be able to recall the value of each variable from T/4 samples ago, each variable must have a running array, the length of which will be the number of samples taken by the ADC in T/4 seconds. Thus two arrays will be needed, one to store each component making up the space vector, and two pointers to store the array entry number of the most recent array entry. Thus, because the array length is T/4 samples long, the array entry one ahead of the array pointer will be the value of the variable from T/4 seconds ago. Once the pointer reaches the end of the array, it rolls over to entry zero once again, thereby closing the loop.

Using these arrays, and the equations given by (27) above, the instantaneous magnitude of both the positive and negative sequence currents may be found:

$$I_{mag}^{+} = \sqrt{I_{\alpha}^{+2} + I_{\beta}^{+2}} \quad (9-12)$$

$$I_{mag}^{-} = \sqrt{I_{\alpha}^{-2} + I_{\beta}^{-2}} \quad (9-13)$$

The RMS value of the sequence magnitudes may now be found by using the method set out in section 9.3.4 above, whilst the percentage unbalance is calculated as shown below:

$$Unbalance = \frac{I_{RMS}^{-} + I_{RMS}^{0}}{I_{RMS}^{+}} \times 100 \quad (9-14)$$

### 9.3.6 Main Control Algorithm

Once all required variables have been sampled, and their RMS values found, the control algorithms that determine actual contactor switching may then be run. Because the unit has two modes of operation (unbalance reduction and pure power factor correction), these two algorithms are run depending upon the user set points. The main control software loop is setup as shown below:

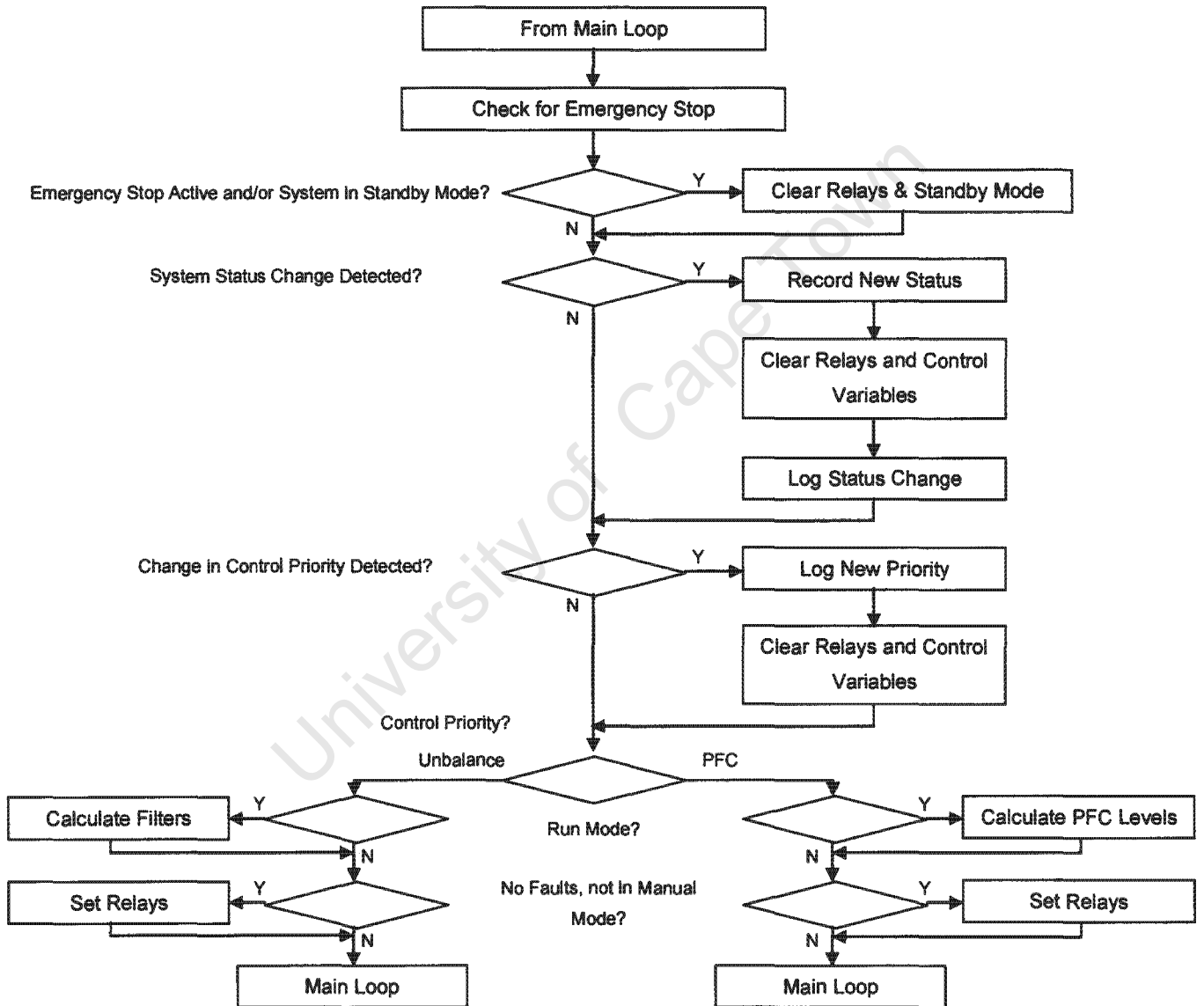


Figure 68: Flowchart - Main Control Algorithm

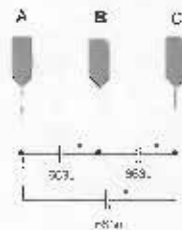
## 10 Laboratory Setup

Because the hybrid system is rated to 466 kVAr, equal to a line current of 675 amperes, finding a suitable test site of 1 MVA capacity or higher was extremely difficult. The problem was exasperated because the test site would need to have low consequential losses should a failure occur, as well as a spare 700 ampere breaker for the unit's connection. It was decided that the untested unit should undergo its initial testing in a laboratory environment, such that proper test results could be achieved. For this purpose it was decided to de-rate the unit by adding, in series with each capacitor bank connection, additional capacitors as shown below. A readily available, three phase connection at the University of Cape Town was a 25 ampere per phase connection. It was thus decided to scale the unit to 1 in 30, such that at full power the connection will be fully utilized. Additional capacitor sizes, their connection and calculations are shown in section 10.1. It should be noted that to ensure that all software will operate correctly when the system is placed into a real industrial environment, each relevant analogue to digital sample (currents and voltages) will be multiplied up by a factor of 30 such that possible overflow errors plus other miscellaneous errors can be detected.

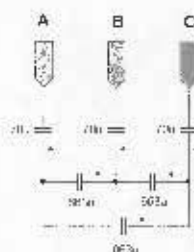
### 10.1 Hybrid System De-Rating

Each capacitor bank will be de-rated by adding in series with each phase additional capacitors as shown below:

Banks 1 & 2 & 5 (Original):

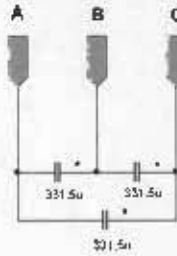


Modified Banks:



$$\begin{aligned} \text{Line Current} &= 145 \text{ A} \\ \text{Input Impedance} &= \frac{230}{1.45} = 1.6 \Omega \\ \text{Required Impedance} &= 47.6 \Omega \quad (1.6 \times 30) \\ \text{Thus an additional } 46 \Omega \text{ capacitor is required on} \\ &\text{each phase.} \\ C &= \frac{1}{2\pi f X_c} = \frac{1}{2\pi 50 \times 46} = 69.2 \mu\text{F} \end{aligned}$$

Banks 3 & 4 (Original):



$$\text{Line Current} = 72.5 \text{ A}$$

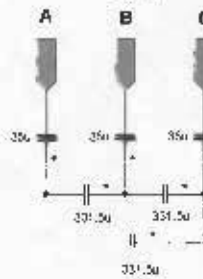
$$\text{Input Impedance} = \frac{230}{72.5} = 3.2 \Omega$$

$$\text{Required Impedance} = 96 \Omega \quad (3.2 \times 30)$$

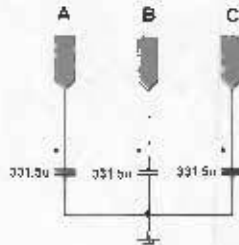
Thus, an additional 93  $\Omega$  capacitor is required on each phase:

$$C = \frac{1}{2\pi f X_c} = \frac{1}{2\pi 50 \times 93} = 34.3 \mu\text{F}$$

Modified Banks:



Banks 6 & 7 (Original):



$$\text{Line Current} = 24.2 \text{ A}$$

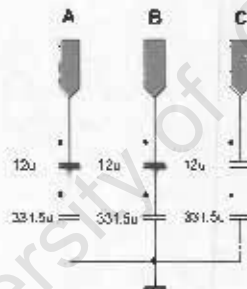
$$\text{Input Impedance} = \frac{230}{24.2} = 9.52 \Omega$$

$$\text{Required Impedance} = 286 \Omega \quad (9.5 \times 30)$$

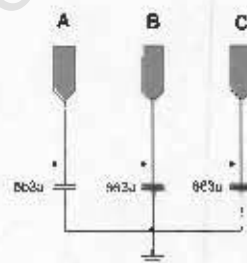
Thus, an additional 276.5  $\Omega$  capacitor is required on each phase:

$$C = \frac{1}{2\pi f X_c} = \frac{1}{2\pi 50 \times 93} = 11.5 \mu\text{F}$$

Modified Banks:



Bank 8 (Original):



$$\text{Line Current} = 48.3 \text{ A}$$

$$\text{Input Impedance} = \frac{230}{48.3} = 4.76 \Omega$$

$$\text{Required Impedance} = 143 \Omega \quad (9.5 \times 30)$$

Thus, an additional 138  $\Omega$  capacitor is required on each phase:

$$C = \frac{1}{2\pi f X_c} = \frac{1}{2\pi 50 \times 138} = 23 \mu\text{F}$$

Modified Bank:

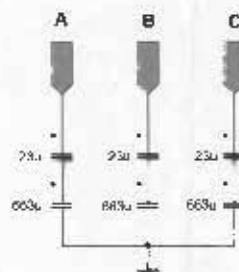




Figure 69. Photo - Additional De-rating Capacitor Banks

Figure 69 above shows the additional capacitors added to the system as calculated in section 10.1.



Figure 70: Photo - Connection of Additional Capacitors, Discharge Resistors

Figure 70 shows the connection of one bank of additional capacitors and their discharge resistors. The discharge resistors are added for safety purposes, where the capacitors are discharged after disconnection of the system from the utility grid. The discharge resistors have a resistance of 100 k $\Omega$  and dissipate the capacitor charge to safe levels (less than 40 volts) within 10 seconds of disconnection.



Figure 71: Photo - Completed Installation

## 10.2 Current Transformer Setup

Originally, the software for the hybrid system was designed such that the current transformers were divided into two sets, one for the source currents and one for the load currents as shown in Figure 72 below.

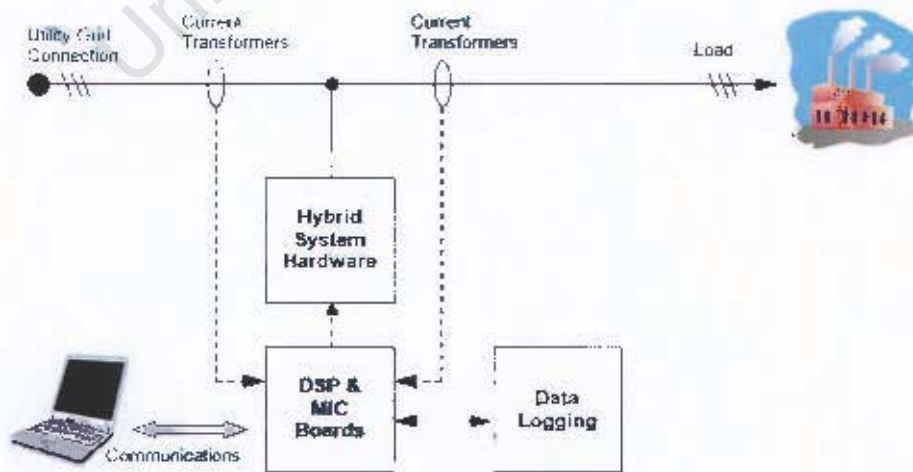


Figure 72. System Overview - Current Transformer Placement

It was decided upon installation of the unit that the load current transformers be moved as shown in Figure 73, where the unit currents are measured instead.

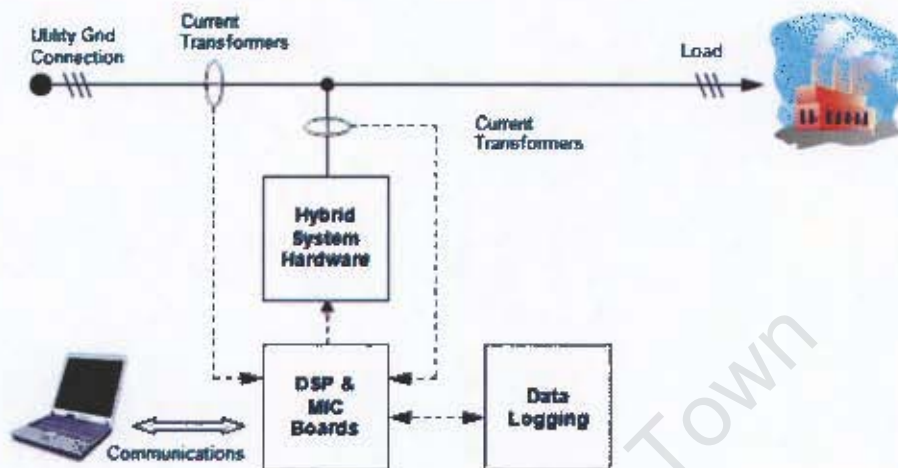


Figure 73: System Overview - New Current Transformer Placement

This change of placement now means that the unit may be installed at any stage after the utility grid connection point and still operate in the same manner as intended. In other words, the hybrid system need not be installed between the source and load; it may become a part of the load instead. The load currents may be calculated by using Kirchhoff's current law where the sum of all currents entering a junction is zero (28), as shown below.

$$I_{Source} + I_{unit} + I_{Load} = 0 \quad (10-1)$$

$$\text{So } I_{Load} = -I_{Source} - I_{unit} \quad (10-2)$$

The size of the current transformers required for the load also now become smaller, as only the unit's currents are measured (up to 700 amperes) instead of the full load current. Also, should the unit be installed online, then only the source current transformers need be of a clamp on type, making the installation cheaper.

### 10.2.1 Source Current Transformers

The main distribution board (DB), onto which the hybrid unit will be connected has a main incoming breaker of 160 A<sub>rms</sub> per phase, with an average load of approximately 45 A<sub>rms</sub> per phase. However, a current transformer set with a 400 to 5 ampere winding ratio were readily available and were small enough to install into the DB itself. A load resistance of 0.235 Ω was chosen for the current transformers because a 1.175 V<sub>rms</sub> signal will be generated across its terminals at full current (5 amperes). This resistance was created with two 0.47 Ω resistors in parallel.

Using equations (8-10) and (8-11):

$$\begin{aligned} \text{CT Secondary Current Resolution} &= \frac{(2 \times 3) \div \text{Load Resistor}}{4096} = \frac{6 \div 0.235}{4096} \\ &= 6.23 \text{ mA per bit} \end{aligned}$$

$$\text{CT Primary Resolution} = \frac{0.00623}{1/80} = 0.5 \text{ [A per bit]}$$

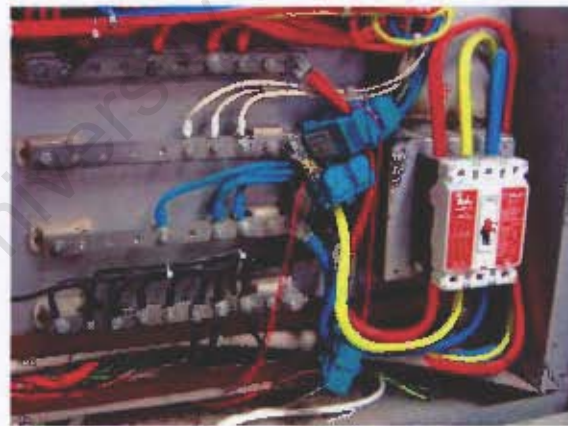


Figure 74: Photo - Main Distribution Board: Source Current Transformers

Figure 74 shows the placement of the source current transformers, installed into the main distribution board of the laboratory. Clearly visible is the incoming breaker and the bus bars for each phase as well as the signal cables (red and black wires) that run into the unit.

### 10.2.2 Unit Current Transformers

Because the hybrid system is rated to a maximum of 675 A<sub>rms</sub> per phase, 800 A<sub>rms</sub> current transformers are required to be able to measure the unit's current consumption. Note that although real current flow will be one thirtieth of the current flow when the system is not being de-rated, 800 A<sub>rms</sub> current transformers were still installed in preparation for industry trials. To increase the current resolution of such a large winding ratio, a larger resistance (2.2 Ω) was placed across the transformer terminals resulting in a larger current signal.

Using equations (8-10) and (8-11):

$$\begin{aligned} \text{CT Secondary Current Resolution} &= \frac{(2 \times 3) \div \text{Load Resistor}}{4096} = \frac{6 \div 2.2}{4096} \\ &= 0.66 \text{ mA per bit} \end{aligned}$$

$$\text{CT Primary Resolution} = \frac{0.000666}{1/160} = 0.107 \text{ [A per bit]}$$



Figure 75: Photo - Unit Current Transformers

Figure 75 shows that current transformers used to measure the unit's current. These are installed at the bottom of the system's cabinet. Clearly visible are the 2.2 Ω load resistors and signal wires (green and white wires).

### **10.3 System Calibration**

Calibration of all current and voltage measurements may now take place to ensure accurate operation of the controller software. This was performed by first disabling all contactor control lines and powering up the DSP and interface boards. Through the DEBUG port of the DSP, the measured values of all currents and voltages were compared to all real values (measured with a true RMS multi-meter and a current clamp). These real valued measurements were then scaled up by a factor of thirty to gain the value that the DSP should return. By adjusting the calibration factors of each ADC channel, the DSP values were adjusted to the correct values. Once calibrated, all calibration levels are saved by the DSP, to be recalled every time the system is started.

University of Cape Town

## 11 Laboratory Results

### 11.1 Initial Test Results

Before the unit was allowed to run under fully automatic mode, initial manual testing was performed to ensure that the de-rating of the system was successfully completed and that the expected current flow is achieved during system operation.

#### 11.1.1 System De-rating

To test if the de-rating occurred correctly, capacitor banks were manually inserted into the grid and the expected current flow compared to the actual current flow. Results of this test are tabulated below:

Bank	Filter	Power [kVAr]	Phase	Current Flow (100%)	Expected Current Flow (3.333%)	Actual Current Flow (3.333%)
1	PFC	100	A	145	4.83	4.9
			B	145	4.83	4.9
			C	145	4.83	5
2	PFC	100	A	145	4.83	5
			B	145	4.83	4.9
			C	145	4.83	5
3	PFC	50	A	72.5	2.42	2.6
			B	72.5	2.42	2.6
			C	72.5	2.42	2.6
4	Δ	25	A	62.5	2.08	2.2
			B	62.5	2.08	2.2
			C	62.5	2.08	2.2
5	Δ	50	A	125	4.17	4.2
			B	125	4.17	4.3
			C	125	4.17	4.3
6	Wye	5.5	A	23	0.77	0.9
			B	23	0.77	0.9
			C	23	0.77	0.9
7	Wye	5.5	A	23	0.77	0.9
			B	23	0.77	0.9
			C	23	0.77	0.9
8	Wye	11	A	48	1.60	1.7
			B	48	1.60	1.8
			C	48	1.60	1.7

Table 10: Comparison of Expected and Actual Current Flow

As shown in Table 10, the actual current flow closely correlates to the expected current flow of the de-rated system. In all cases, the actual current flow is within 200 mA of the expected current flow and, given that the current clamp had a resolution of 100 mA, it can be said that all capacitor banks were successfully de-rated to a one thirtieth scale model.

### 11.1.2 System Power Flow

Once it was shown that the system was successfully transformed into a one in thirty scale model, the actual impact of all capacitor banks on the measured source currents were tested. For this test, both wye and delta connected banks were manually inserted into the grid and the source and load power levels recorded. The impact on the source currents are then compared to anticipated values. The results of the comparison are tabulated below:

Capacitive Power (Line to Neutral)	Source Reactive Power [kVAr]	Load Reactive Power [kVAr]	Impact on Reactive Power [kVAr]	Expected Impact [kVAr]
5 kVAr	22	28	6	5
11 kVAr	15	27	12	11
16 kVAr	11	28	17	16
22 kVAr	17	40	23	22

Table 11: Impact of Wye Connected Filters on Imaginary Power Flow

It can thus be said that the impact of each wye filter on the reactive power flow as seen by the source closely matches the expected impact.

Capacitive Power (Line to Line: BC)	Source Real Power [kW]			Load Real Power [kW]			Impact on Real Power [kW]			Expected Impact [kW]		
	A	B	C	A	B	C	A	B	C	A	B	C
25 kVAr	286	269	266	285	276	260	1	-7	6	0	-7.2	7.2
50 kVAr	281	218	271	279	233	258	2	-15	-13	0	-14.4	14.4
75 kVAr	296	213	282	295	236	261	1	-23	-21	0	-21.6	21.6

Table 12: Impact of Delta Connected Filters on Real Power Flow

Capacitive Power (Line to Line: BC)	Source Reactive Power [kVAr]			Load Reactive Power [kVAr]			Impact on Reactive Power [kVAr]			Expected Impact [kVAr]		
	A	B	C	A	B	C	A	B	C	A	B	C
25 kVAr	22	16	7	21	28	20	1	-12	-13	0	-12.5	-12.5
50 kVAr	19	4	-5	19	28	19	0	-24	-24	0	-25	-25
75 kVAr	19	-9	-16	17	27	21	2	-36	-37	0	-37.5	-37.5

Table 13: Impact of Delta Connected Filters on Reactive Power Flow

The impact of the delta connected filters thus also closely matches the expected impact on both real and reactive power flow as seen by the source. This means that the theory examined in section 3 is correct and may be used to balance unbalanced currents.

### 11.1.3 LCD Display Signal Filter

During the above test procedures, it was discovered that the electromagnetic interference (EMI) of a commutating contactor was significant enough to confuse the LCD module. This rendered the module useless until re-initialized. To overcome this problem, a low pass filter was placed onto the LCD communications cable such that the lower frequency information could pass unimpeded, but that all high frequency EMI would be rejected. This was achieved by adding an inductance into the signal line by wrapping the line around a ferrous toroidal core until the desired response was achieved. Too many turns would yield an inductance large enough to begin to reject the required LCD signal, too few turns and the EMI could still pass. The optimum number of turns in this instance was three for correct LCD operation.

In addition to the low pass filter, the Interface board software was modified to re-initialize the LCD module every 20 seconds to ensure that the module will be able to recover from any confusing EMI. The re-initialization code was also significantly

optimized to allow for a very fast re-initialization of the LCD module such that the procedure is barely noticeable by the user.

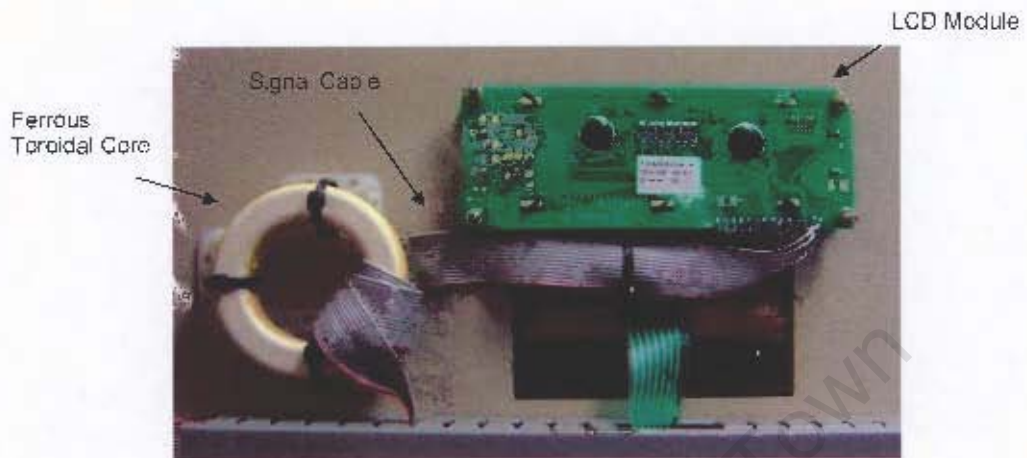


Figure 76: Photo - LCD Module Signal Filter

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## 11.2 Harmonic Impact on the Utility Grid

One of the disadvantages listed in section 2 is that capacitors amplify harmonics present on the utility grid, resulting in many topologies utilizing de-tuning inductors as a method of keeping these harmonics under control. To examine the actual impact of the unit on the harmonics of the grid, the voltage and current waveforms are examined along with a fast Fourier Transform of the current waveform.

To determine the impact of different filter types on the current harmonics, a comparison is performed for full power factor correction, for full delta compensation and for full wye compensation.

### 11.2.1 Uncompensated Utility Grid Voltage and Current Waveforms

To be able to make an accurate comparison of the impact of the various filters on the harmonic content of the voltage and current waveforms, the uncompensated waveforms are first analyzed below:

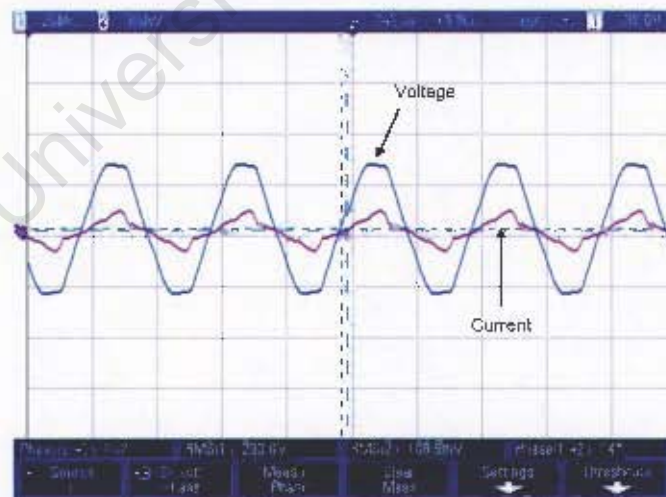


Figure 77: Oscilloscope Trace - Natural Grid Voltage and Current Waveforms

Figure 77 shows the laboratory voltage (blue trace) and current (pink trace) waveforms without system compensation. It can be seen that both waveforms are

severely non-sinusoidal and are thus subject to several additional harmonics. These additional harmonics will be amplified with system compensation, as explained in section 3.3. The harmonic content of the uncompensated utility grid is shown below and was attained with the use of the 8334 Qualistar power analyzer from Chauvin-Arnoux (29).

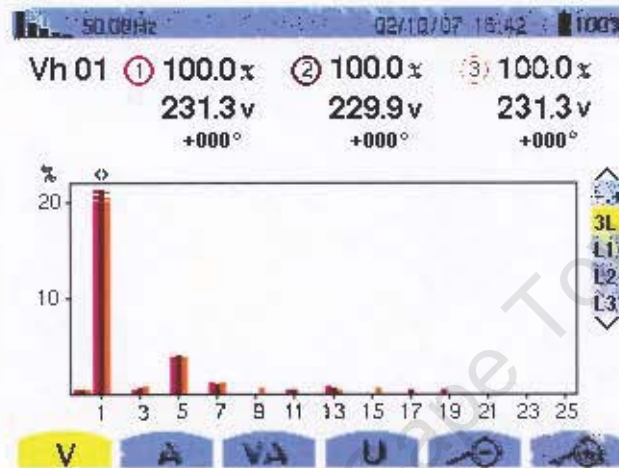


Figure 78: Harmonic Composition of the Natural Grid Voltages

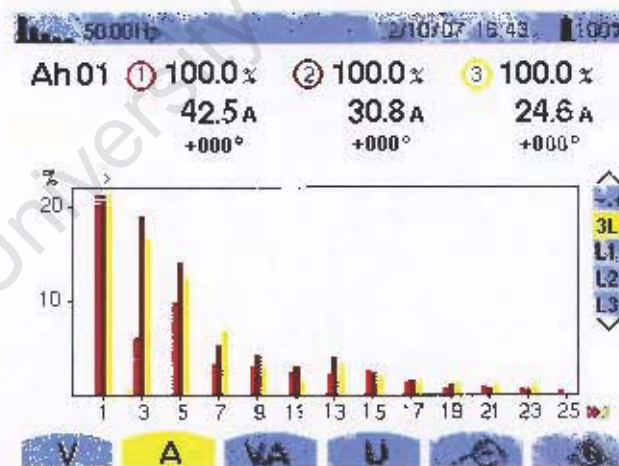


Figure 79: Harmonic Composition of the Natural Grid Currents

Figure 78 and Figure 79 show the percentage composition of the harmonic content of the three grid voltage and current waveforms in relation to the fundamental harmonic, where the magnitude of the fundamental harmonic is always 100 % and each higher order harmonic is shown as a percentage of that fundamental

magnitude. Note that to be able to capture any possible increase in harmonic content, the Y-axis of each bar graph is scaled to show only 20 % of the fundamental magnitude, such that even a small change in harmonic amplitude may be seen.

### 11.2.2 Impact of Full Power Factor Correction

To determine the impact of the system when performing full power factor correction (466 kVAr), the system was placed into manual mode and all contactors were closed. The new utility grid voltage and current waveforms are shown below:

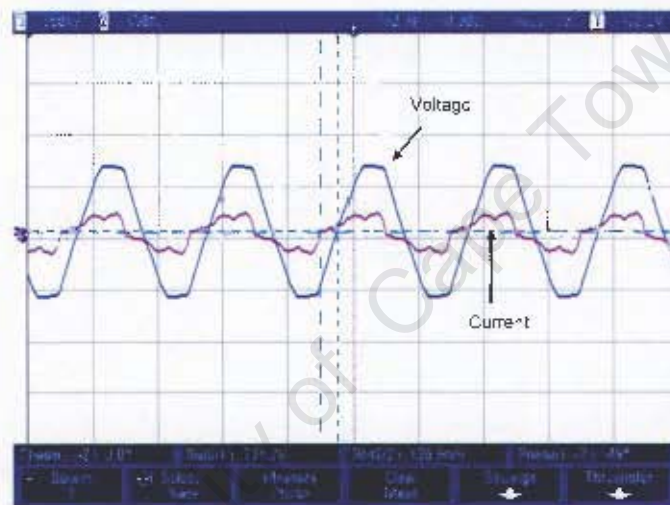


Figure 80: Utility Grid Voltage and Current Waveform under Full Power Factor Correction

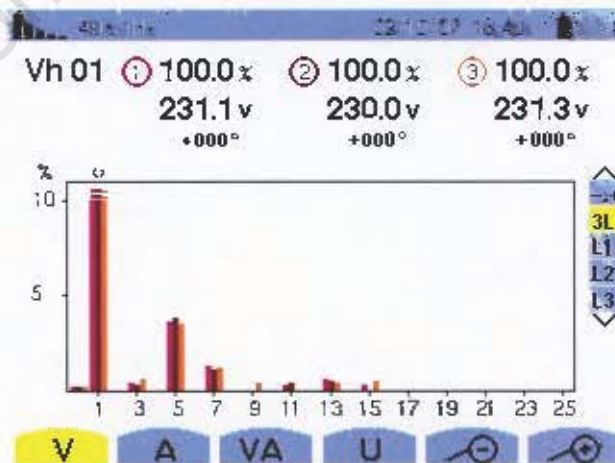


Figure 81: Voltage Waveform Harmonic Content under Full Power Factor Correction

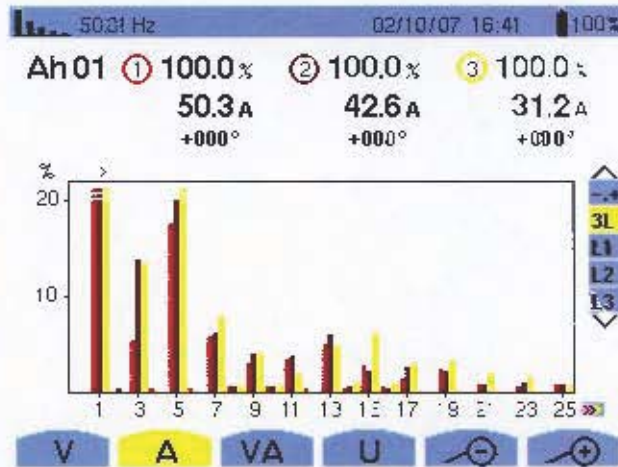


Figure 82: Current Waveform Harmonic Content under Full Power Factor Correction

Comparing Figure 81 with Figure 78 shows that an increase is seen in the harmonic content of the voltage waveforms, particularly the 5<sup>th</sup> and 7<sup>th</sup> harmonic. A comparison of Figure 82 with Figure 79 shows that an increase is also seen in virtually all current harmonics, with the largest gain seen in the lower, odd order harmonics. This increase in both voltage and current harmonics correlate with expectations, as laid out in section 3.3.

### 11.2.3 Impact of Full Delta Filter Compensation

To determine the impact of delta connected filters on the harmonic content of the voltage and current waveforms, the system was again placed into manual mode and both delta filter banks were inserted across phases 'B' and 'C'. The resulting waveforms are shown below (Figure 83):

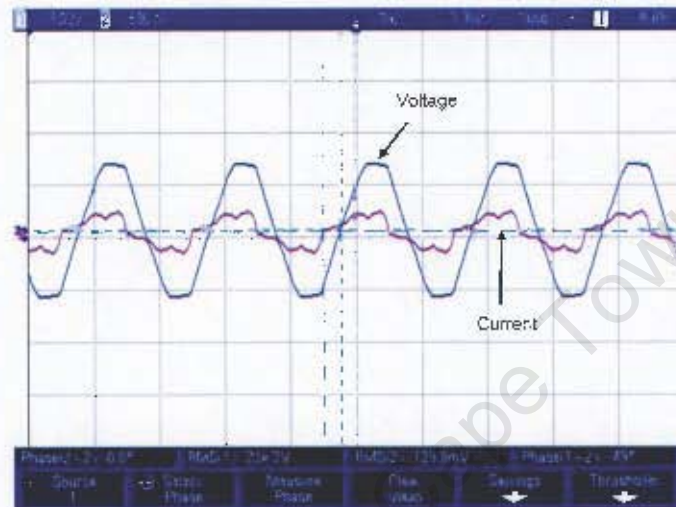


Figure 83: Utility Grid Voltage and Current Waveforms under Full Delta Compensation

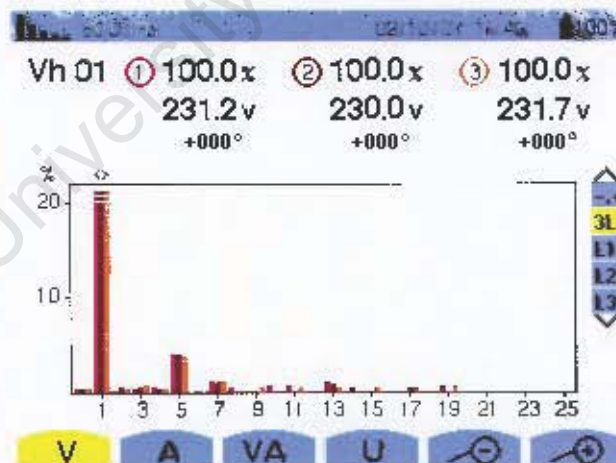


Figure 84: Voltage Waveform Harmonic Content under Full Delta Compensation

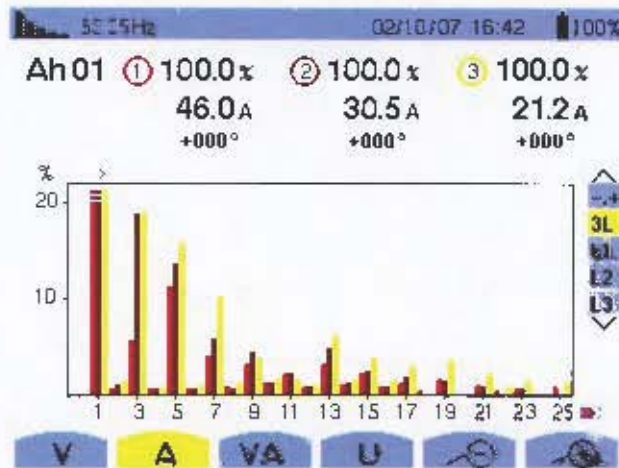


Figure 85: Current Waveform Harmonic Content under Full Delta Compensation

Clearly visible in Figure 85 above is the introduction of additional harmonics in the current waveform, when compared to Figure 79. The introduction of even order harmonics and the amplification of odd order harmonics can be seen.

#### 11.2.4 Impact of Full Wye Compensation

To determine the impact of wye connected filters on the harmonic content of the voltage and current waveforms, the system was again placed into manual mode and all wye filter banks were inserted on phase 'B'.

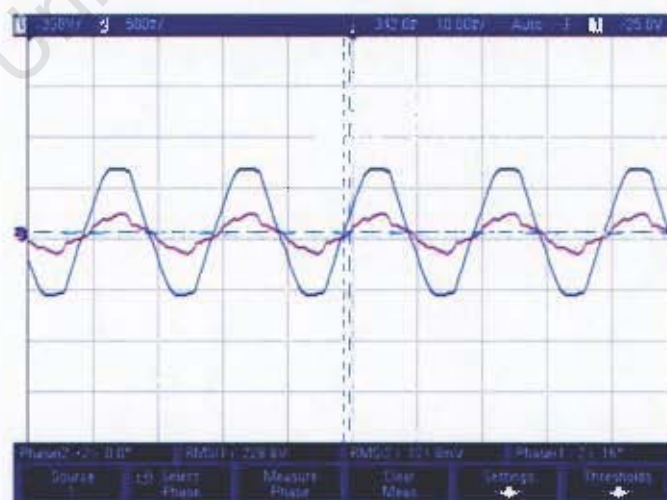


Figure 86: Oscilloscope Trace - Grid Voltage and Current Waveforms with 22 kVAr Wye Filter

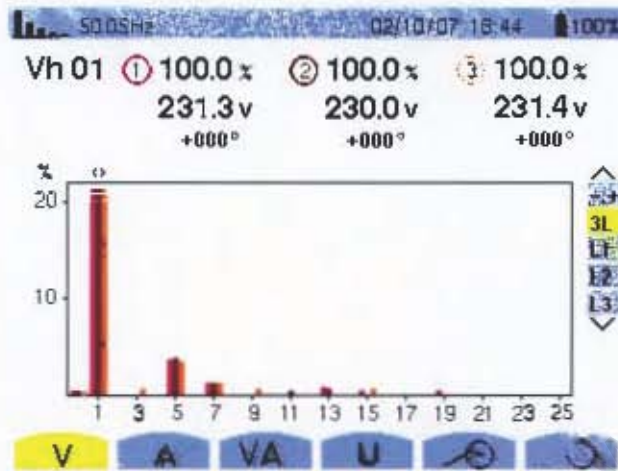


Figure 87: Voltage Waveform Harmonic Content under Full Wye Compensation

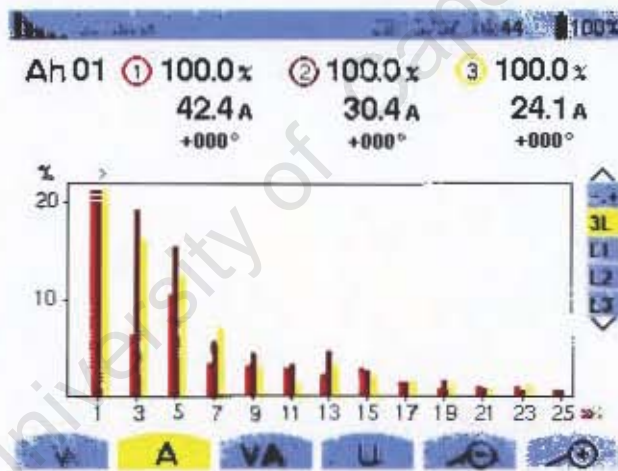


Figure 88: Current Waveform Harmonic Content under Full Wye Compensation

A small increase may be seen in the phase 'B' harmonic content (brown line), mostly on the 3<sup>rd</sup>, 5<sup>th</sup> and 13<sup>th</sup> order harmonics.

## 11.3 Contactor Testing

### 11.3.1 Auxiliary Timing

As stated in section 5.8, each contactor is equipped with an auxiliary contactor/resistor wire set. This additional set is intended to extend the lifespan of the main contactor terminals by reducing the inrush current to the capacitor banks. To be able to determine the impact a switch-in cycle on the utility grid current waveform, the timing of the contactor/auxiliary set must be determined. This was performed by repeated switch-in cycles of a contactor in the following setup:

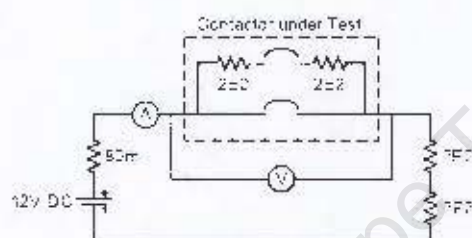
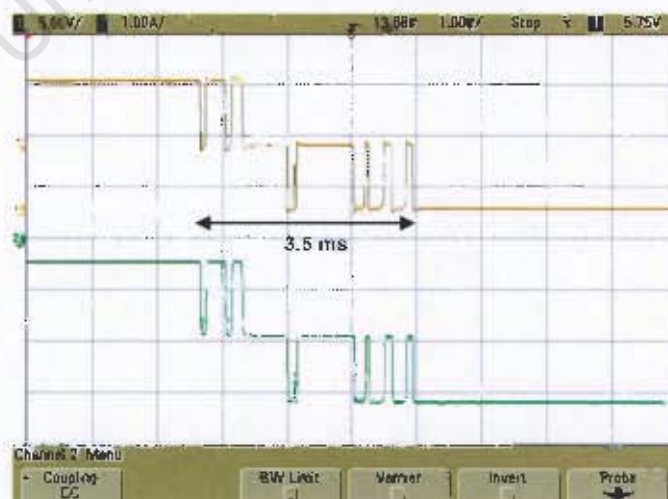


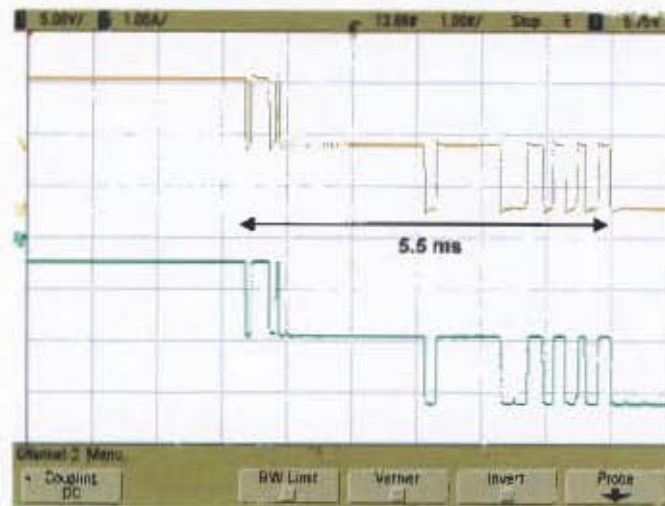
Figure 89: Schematic - Contactor Test Setup (9)

The voltage potential developed across the contactor will thus be the full supply voltage (12 V) when completely open, half supply voltage (6 V) when only the auxiliary is closed and zero volts when the main contactor is closed. Repeated switch cycles were performed and the voltage measured across the contactor under test was recorded.



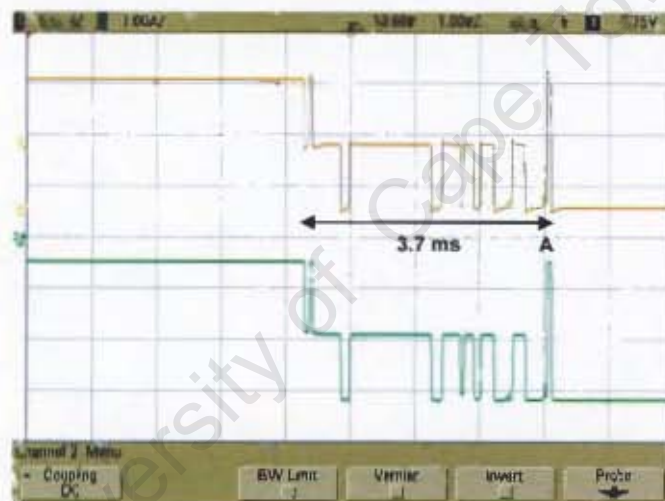
Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 90: Waveform - Contactor Test 1(9)



Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 91: Waveform – Contactor Test 2 (9)



Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 92: Waveform - Contactor Test 3 (9)

It can be seen in all three contactor test cycles (Figure 90 to Figure 92) that some switch-bounce takes place by both the auxiliary and the main contactor contacts. This results in the recorded voltage and current waveforms oscillating between voltage levels before settling. Shown on each test waveform is the length of time that lapsed between the first auxiliary switch and the last main contact switch, if these values are averaged, then the average auxiliary conduction time is 4.2 ms. Figure 92 also shows that the switch-bounce experienced by the main contactor may be severe enough to cause the contactor to fully disengage before engaging once again (see point 'A', Figure 92).

### 11.3.2 Current Waveform Transients

To be able to confirm results found in section 5.8, the current waveform of a 100 kVAR capacitor bank was recorded during a switch cycle with a contactor equipped with auxiliary resistor windings. The schematic of the laboratory test is shown below:

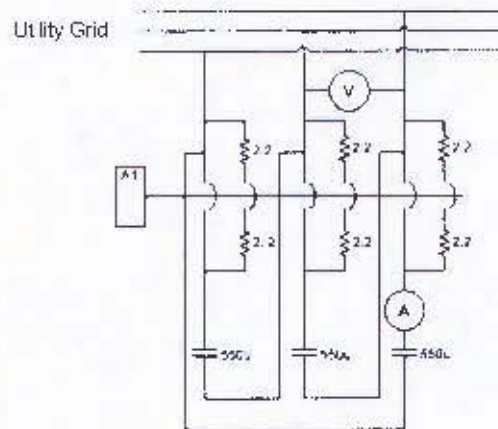
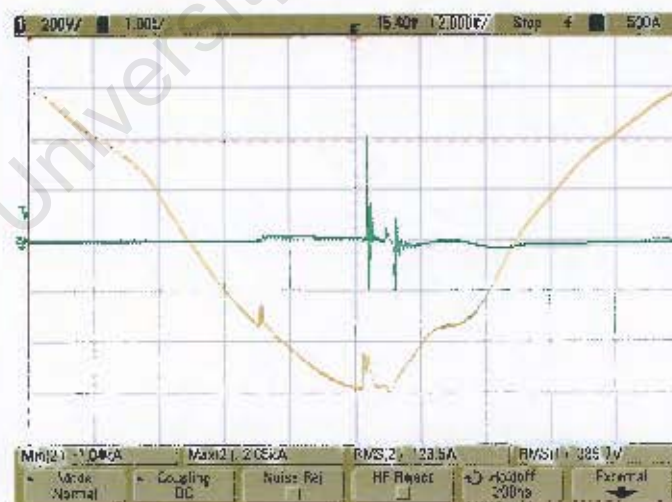


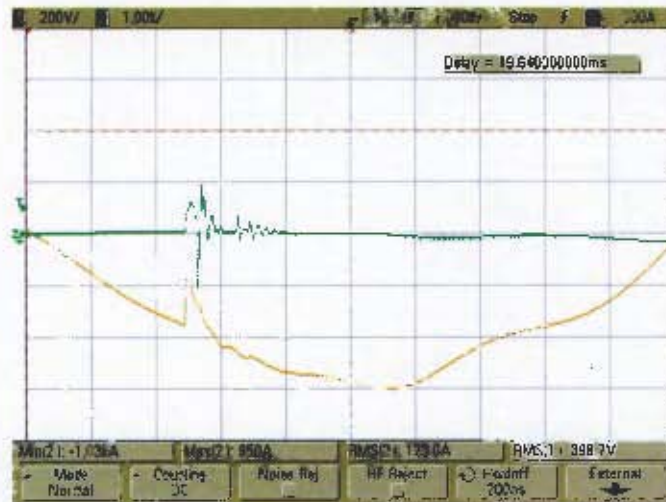
Figure 93: Schematic - Current Transient Test Setup (9)

Several switching cycles were completed such that the switching transient could be captured over a range of positions on the voltage waveform. Note that the current trace (green trace) has a scale of 1kA per division.



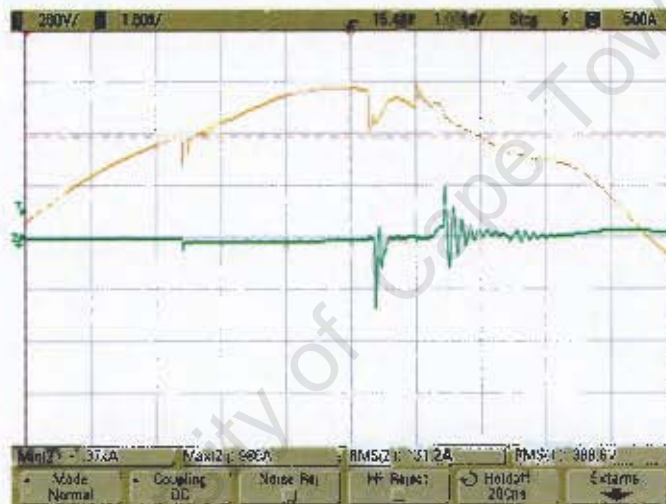
Note:  
Orange Trace - Voltage  
Green Trace - Current

Figure 94: Waveform - Current Transient 1 (9)



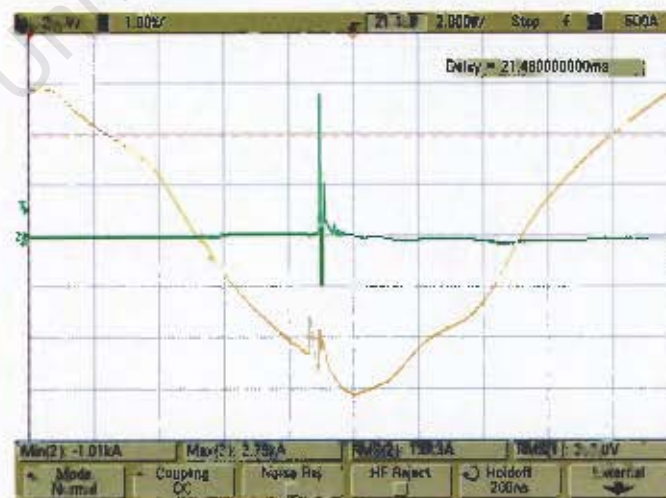
Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 95: Waveform - Current Transient 2 (9)



Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 96: Waveform - Current Transient 3 (9)



Note:  
Orange Trace – Voltage  
Green Trace – Current

Figure 97: Waveform - Current Transient 4 (9)

Figure 97 shows that the maximum amplitude of the current waveform can be as high as 2.8 kA, depending on where on the voltage waveform the main contactor is closed. This is slightly less than the value determined in section 5.8, indicating that the supply used during the laboratory tests had a slightly higher source impedance than that used in simulations, however, a correlation may be made between simulations and laboratory waveforms thereby verifying results.

Maximum current amplitude of a switch transient is thus reduced by the auxiliary resistive wires from 11 KA to 3 KA, thus drastically increasing the lifespan of each contactor. This both increases the reliability of the system as well as increases the project life-span, after which contactors would have to be replace

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## 11.4 Impact on Unbalanced Currents

Through observation, the average real current flow per phase into the laboratory main distribution board is 60 Amperes during the afternoon peak demand times. This equates to a three phase power flow of 41400 VA. However, if the actual apparent power flow is subject to the one in thirty scaling factor of the compensator, then a scaled apparent power flow of 1.2 MVA is recognized by the compensator unit. By comparing this scaled power flow to Figure 31, it can be seen that, at best, a maximum unbalance of 6 % may be compensated for.

Data logging of the system's performance was achieved by setting 'Docklight', a PC communication tool, to request various data values from the DSP's data table. These values were returned in comma separated format which could then be imported into Microsoft Excel. Graphs of all relevant variables could then be created. Several logging sessions were run, extracts of which are shown in the results below.

### *11.4.1 Source and Load Current Waveform Comparison*

The impact on the source current phase RMS values is shown in Figure 99 below and is compared to the load side current phase RMS values (Figure 98). It can be seen in the results below that phase 'C' currents are drastically reduced from the load side to the supply side. A small increase in the phase 'B' currents can also be seen as some of the load is being shifted (as the supply sees it) from phase 'C' to phase 'B'. This motion of the outer phase currents (smallest and largest RMS values) towards the average can be seen as a reduction in current unbalance.

It should be noted that in the graphs below, the control algorithm was only activated after an initial minute of logging, such that a differential impact may be seen on the supply side graphs.

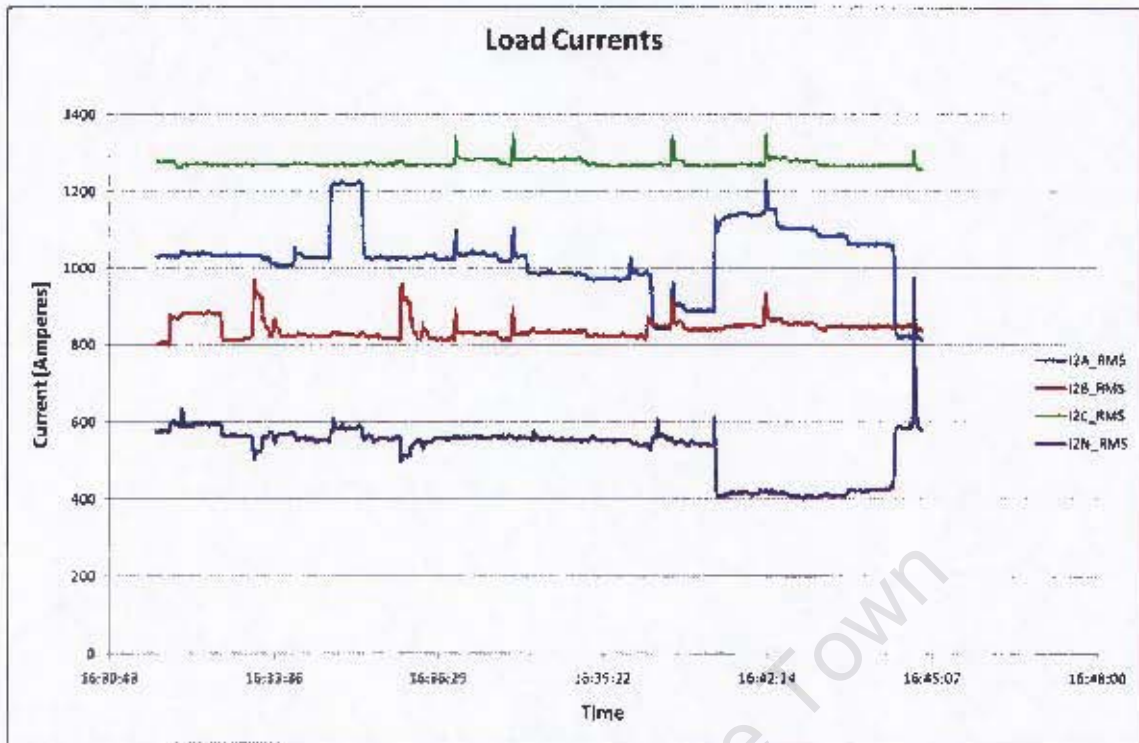


Figure 98: Graph - Load Side Currents

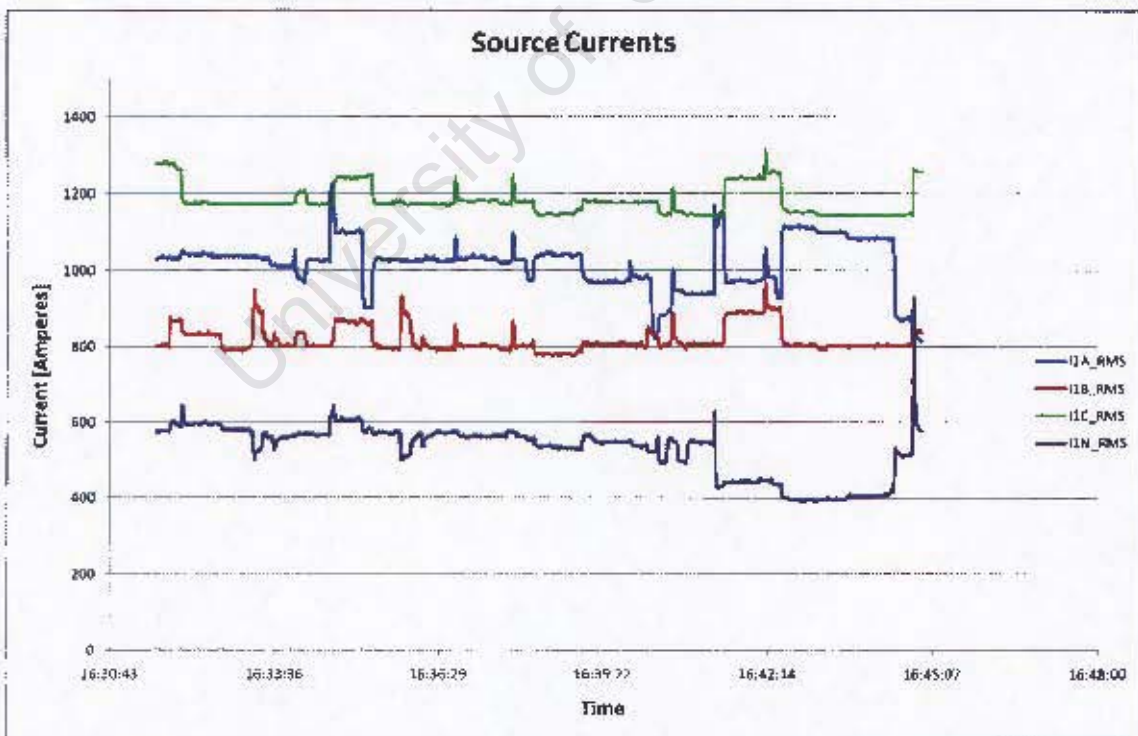


Figure 99: Graph - Supply Side Currents

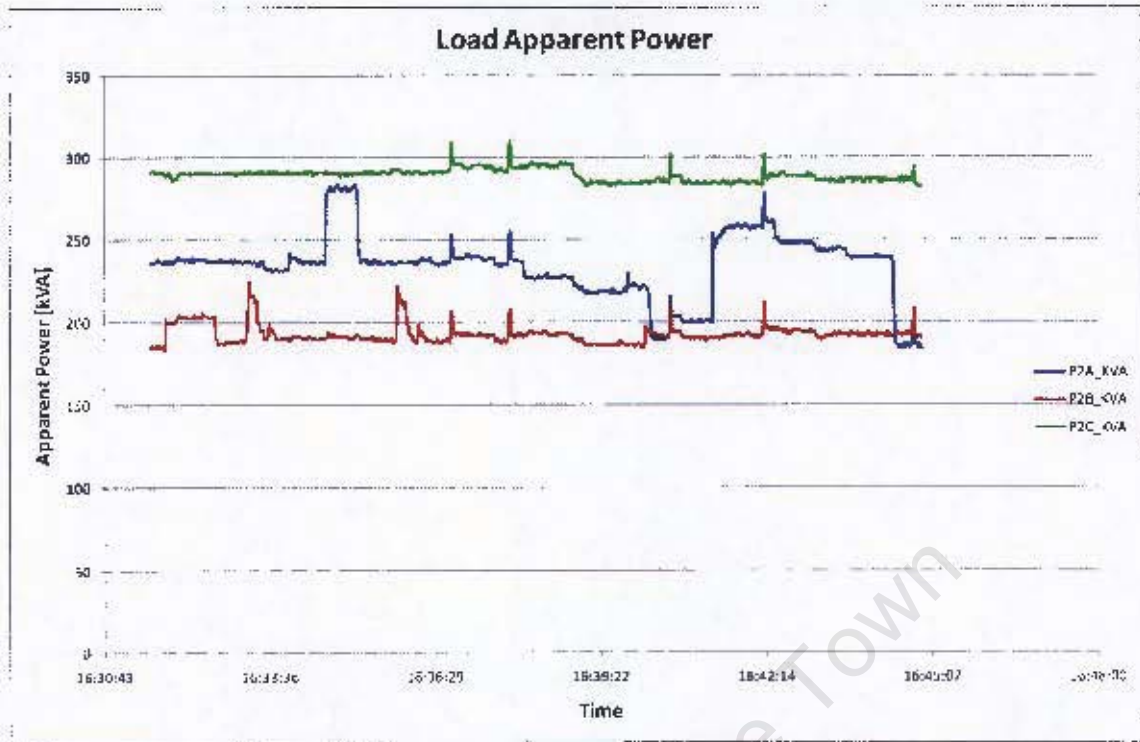


Figure 100: Graph - Load Side Apparent Power

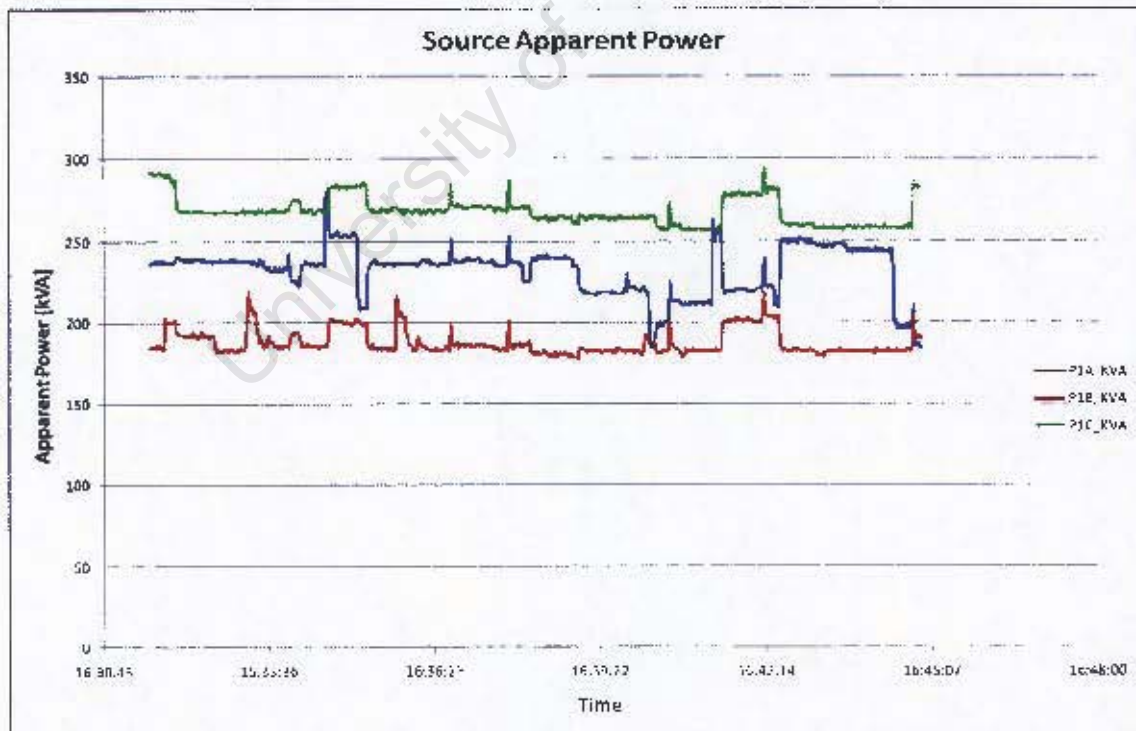


Figure 101: Graph - Supply Side Apparent Power

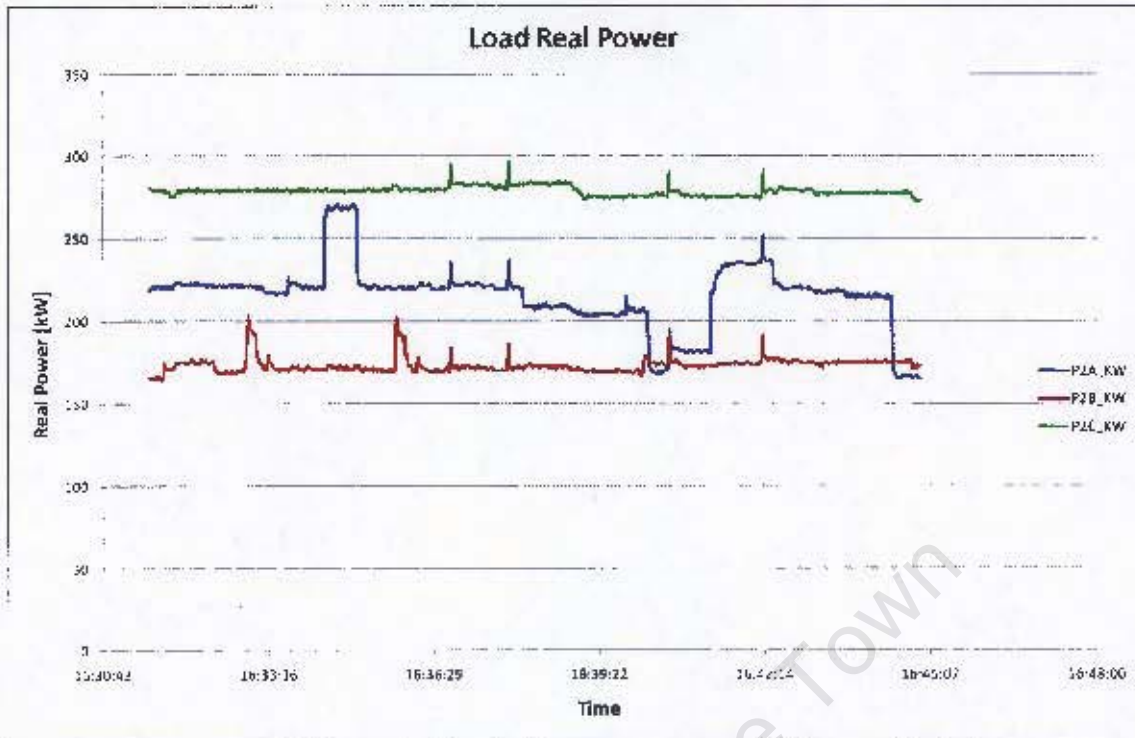


Figure 102: Graph - Load Side Real Power

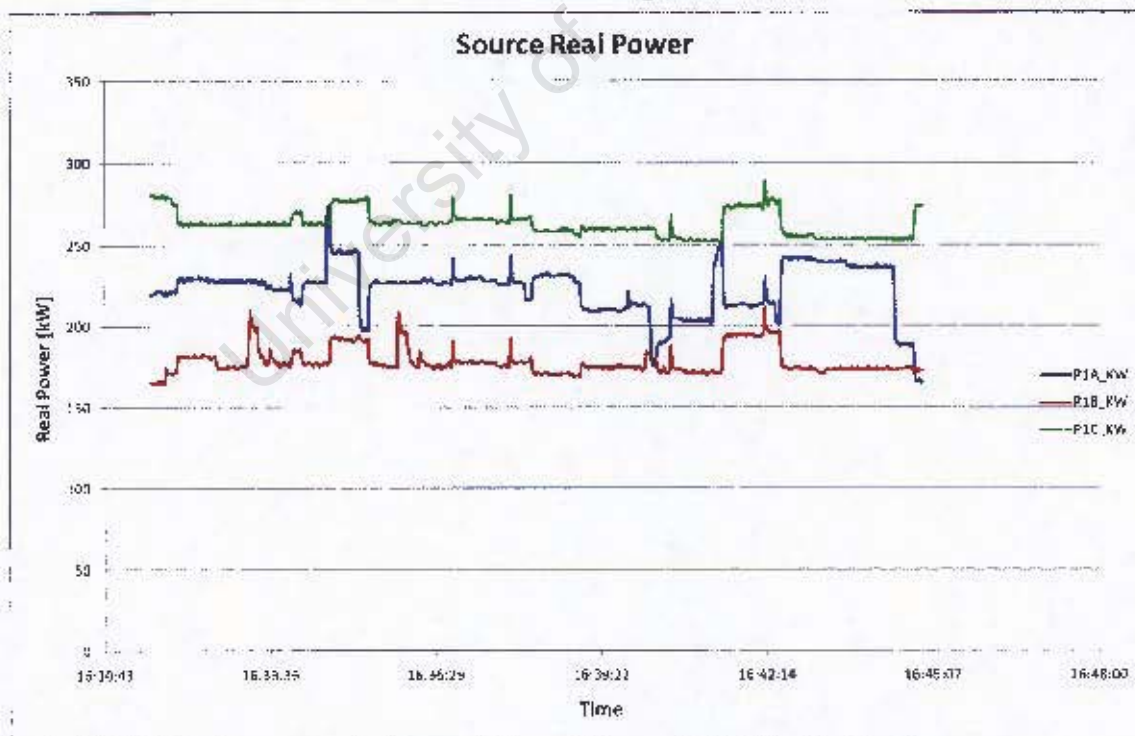


Figure 103: Graph - Supply Side Real Power

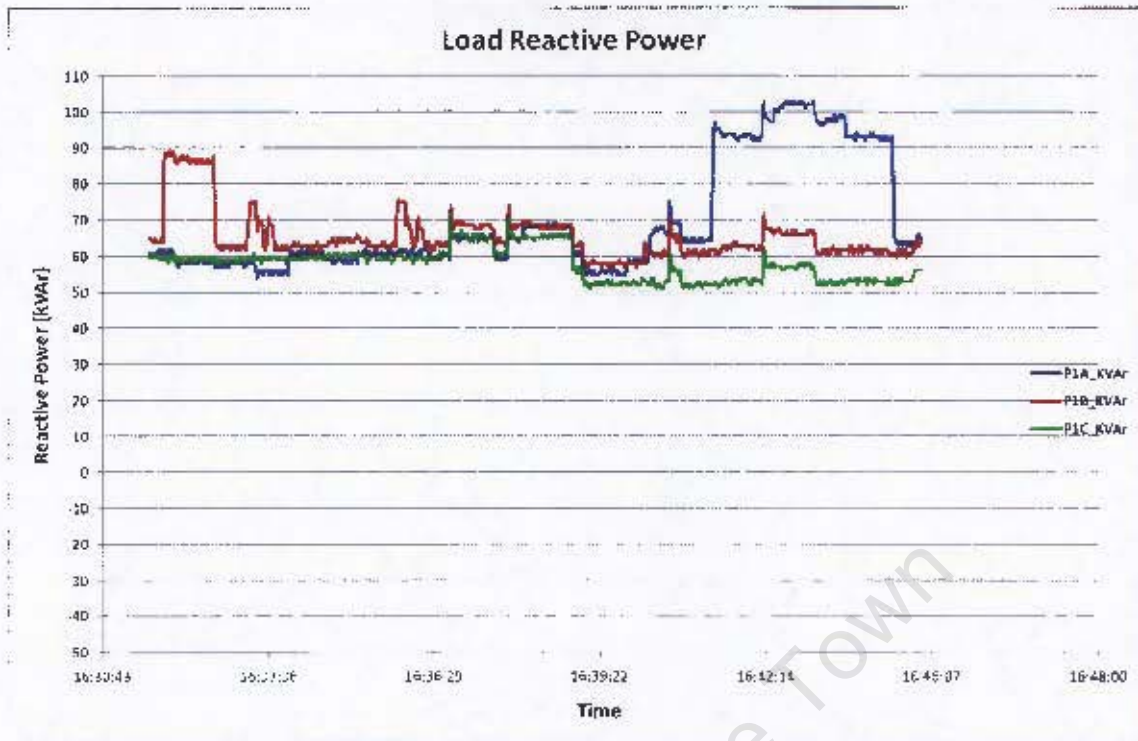


Figure 104: Graph - Load Side Reactive Power

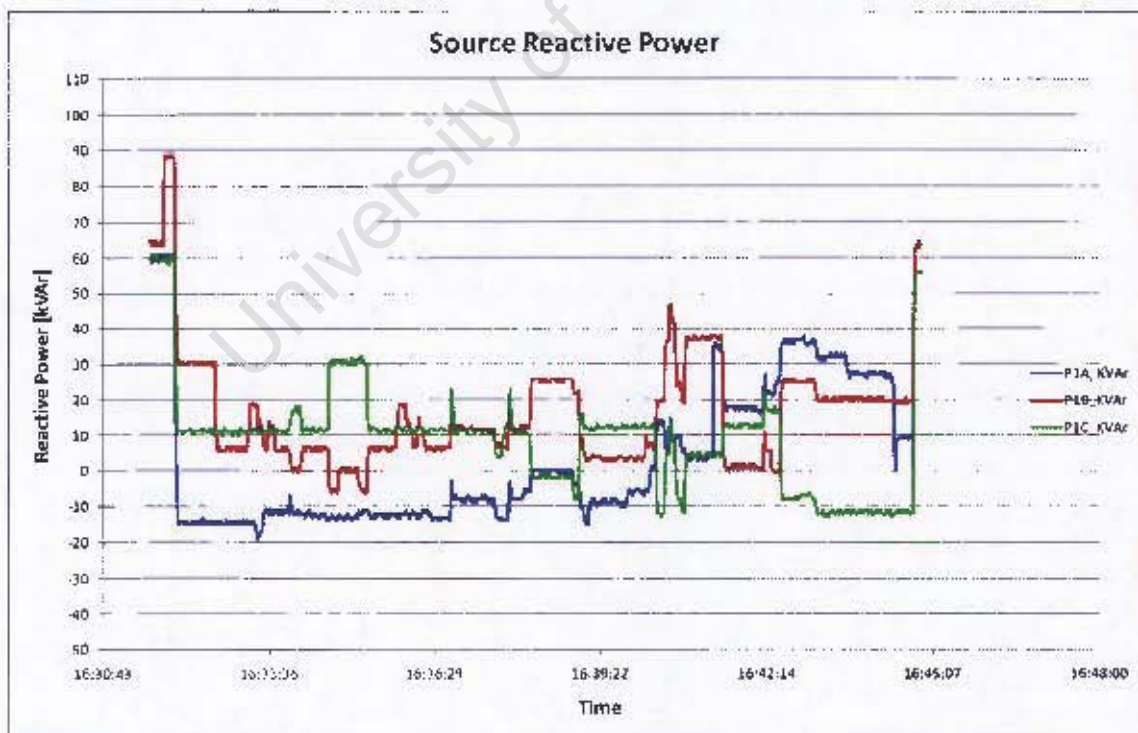


Figure 105: Graph - Supply Side Reactive Power

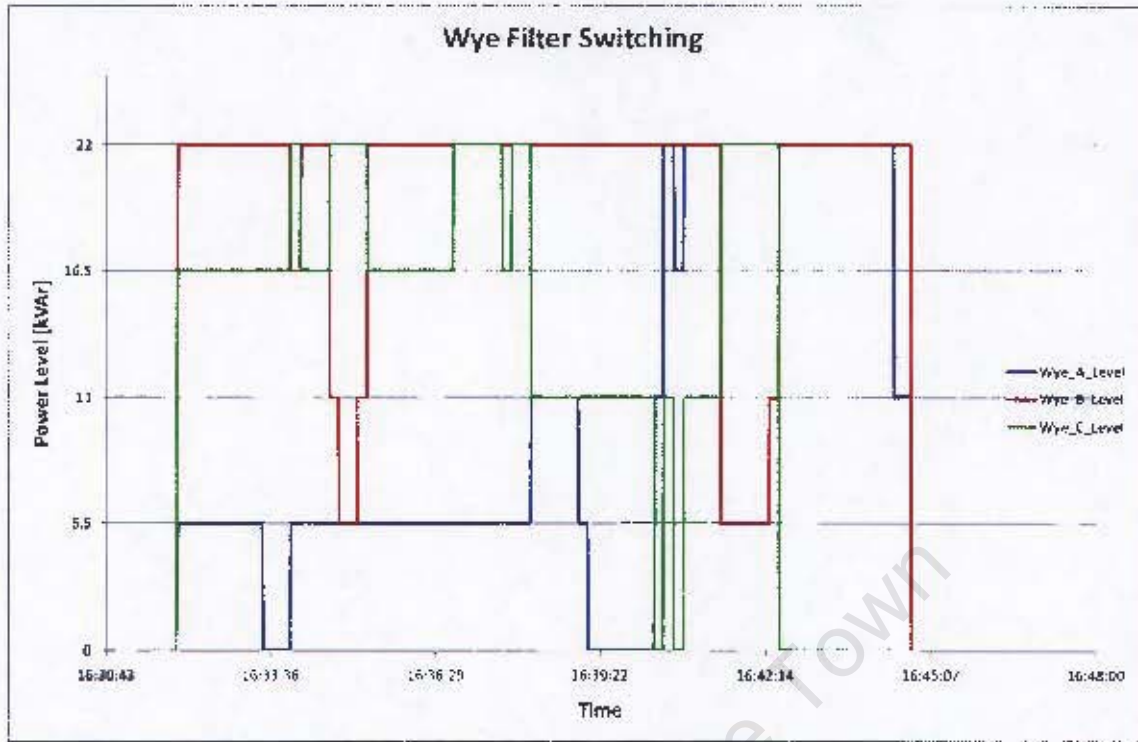


Figure 106: Graph - Wye Filter Switching Pattern

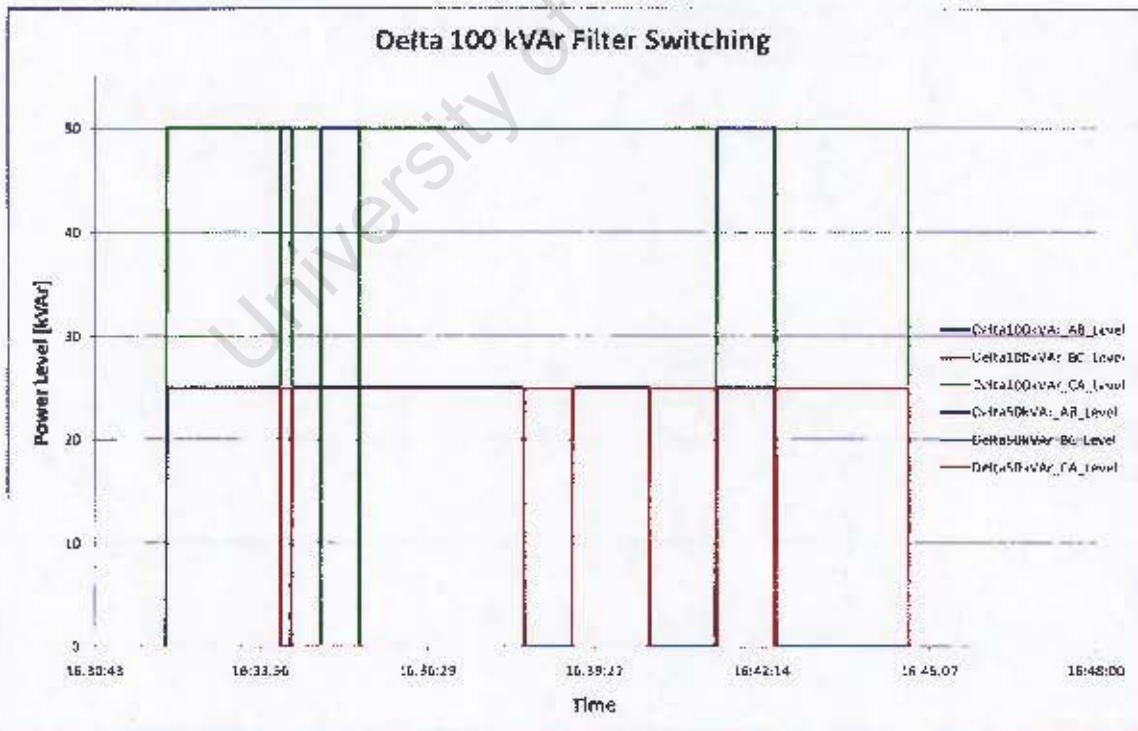


Figure 107: Graph - Delta Filter Switching Pattern

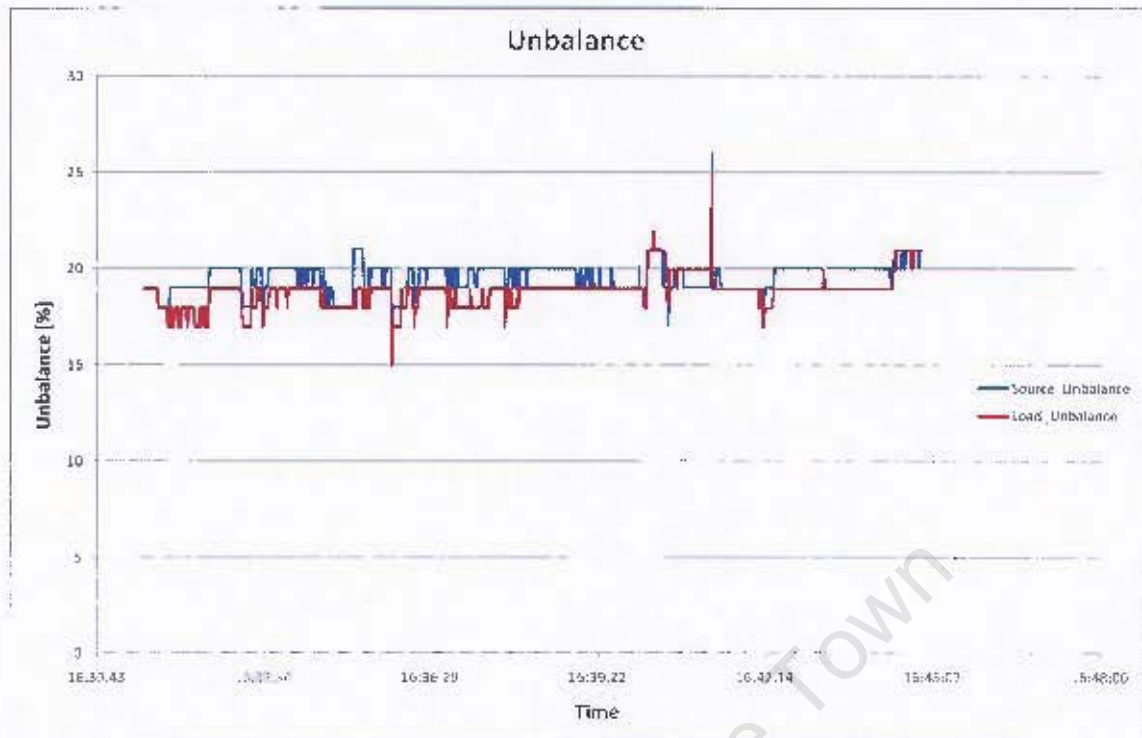


Figure 108: Graph - Unbalance Levels (Proper Definition)

#### 11.4.2 Analysis of Unbalance Estimation Algorithm

It can be seen in Figure 108 above that the source unbalance level is generally higher than the load unbalance level, contrary to expectations. As stated previously, a reduction in unbalance of up to 6 percent may be seen for such a load size, but expectations lie in the 2 to 3 percent range (depending on phase currents relative to each other, since to achieve maximum compensation the unit must be able to use all delta connected filter across one line to line voltage). An analysis of the impact of harmonic content on the unbalance algorithm was performed using computer simulation software, MATLAB 7 (see Appendix H) and was found to be the cause of the increase in unbalance shown above. To be able to accurately determine the impact of the system on the utility grid, the author considered the use of the NEMA definition (30) of unbalance:

$$\text{Unbalance} = \frac{\text{Maximum Deviation from the Mean of } (I_a, I_b, I_c)}{\text{Mean}(I_a, I_b, I_c)}$$

(11-1)

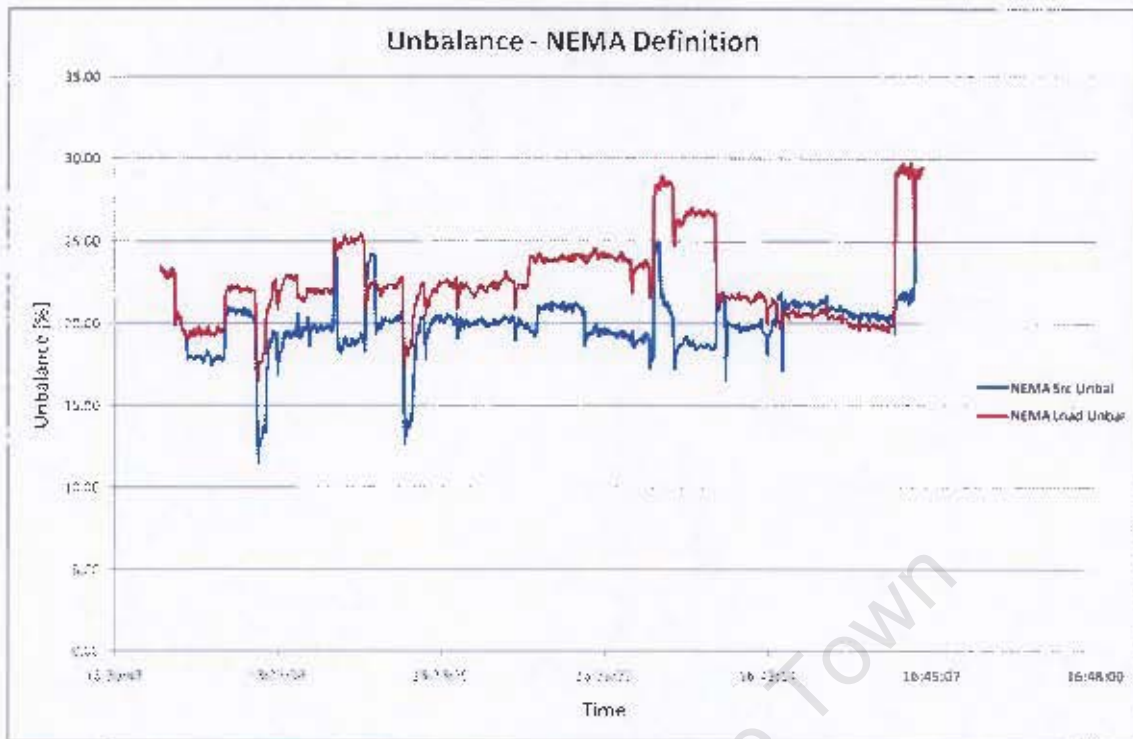


Figure 109. Graph - Unbalance Levels (NEMA Definition)

Figure 109 above shows the impact of the system on the source unbalance using the NEMA definition. An improvement of approximately 2 to 3 percent of the source side currents may now be seen, however, referring to (30), it can be seen that only the current that is furthest from the average of the three phase currents is accounted for. This means that the true impact of the system on the supply currents is understated and another measure of the system's impact is required. This new measure of unbalance is calculated by using the real and reactive power flow in each phase (refer to Appendix I) and is thus not directly influenced by harmonic content (since RMS value for current and voltage are used), nor is any phase neglected. Here, the standard deviation of the phase real and reactive powers from the average is used as a ratio of the average phase real and reactive power. The unbalance results, using this new measure of unbalance, are shown in Figure 110.

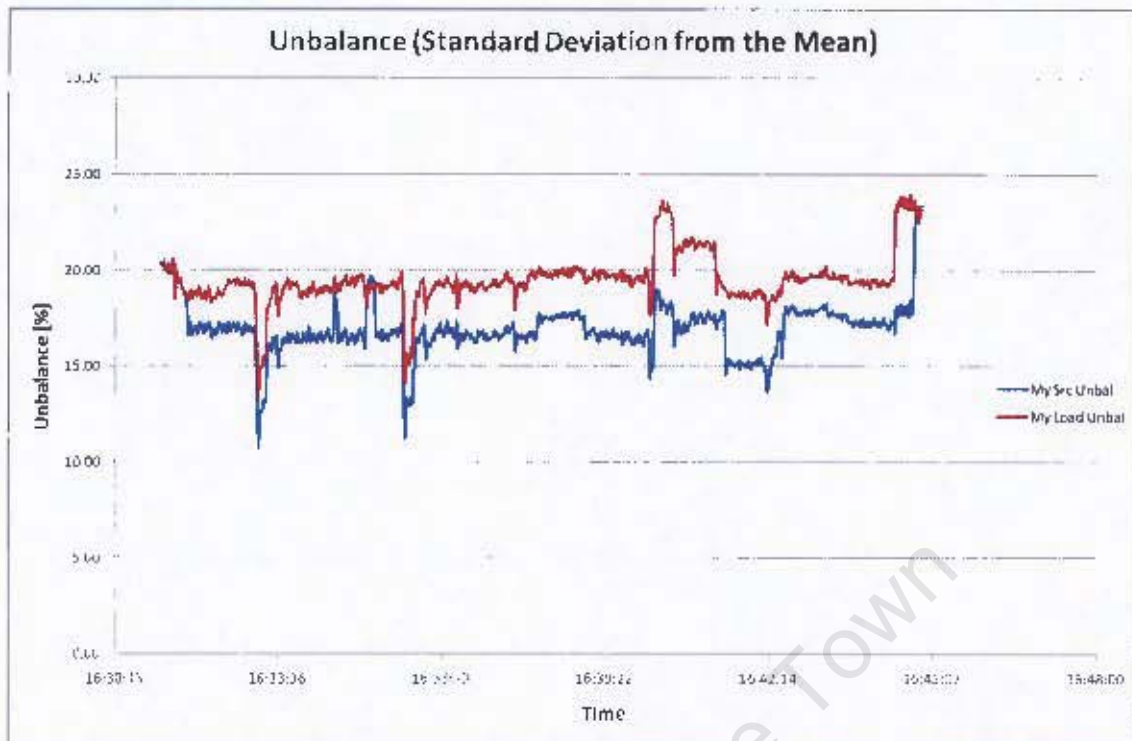


Figure 110: Graph - Unbalance Levels (Standard Deviation from the Mean)

Figure 110 shows that the unbalance as seen by the supply (utility grid) is less than that of the load, where the average impact of the system is approximately 3 percent. A comparison as to the simulated impact of the system on the utility grid may now be performed. This is achieved by programming the simulation with a load equal to the average load recorded in Figure 102 and Figure 104. After running the simulation, the following impact on unbalance was seen:

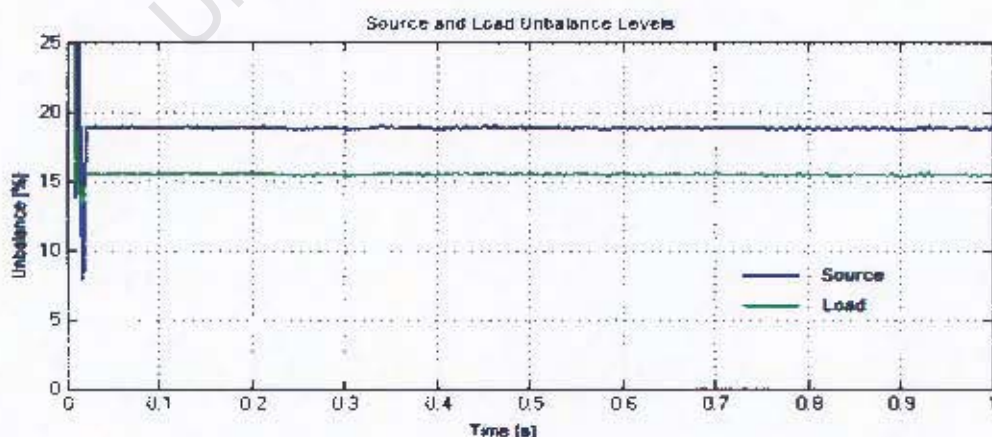


Figure 111: Graph - Simulation of Impact on Unbalance Level

Figure 111 shows that the average decrease in unbalance as seen by the source is 3.5 percent and the results, therefore, closely match that expected from simulations. It should be noted that the percentage unbalance returned by this new measure of unbalance is closely comparable to the results returned by the proper unbalance definition, as shown in appendix I.

Figure 106 and Figure 107 show that the capacitor filter switching patterns can be slightly oscillatory around transition points before settling down to the required combination. It was found that despite the addition of some hysteresis, the measured power flow oscillated around the true value due to measurement errors that were scaled up by a factor of thirty (in accordance with scaling of the entire system). This scaling error would thus not occur when installed on a full scale load as the current measurements would have far greater resolution.

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## 12 Conclusions

Based on the above chapters, the following may be concluded:

- A hybrid power factor/unbalance compensator unit could be built easily and cost effectively by modifying a standard power factor correction unit.
- The control strategy laid out in section 3.2.3 was proven through simulation and practical observation to be correct and able to reduce current unbalance.
- Simulations show that a maximum level of unbalance exists, beyond which the unit may not compensate. This level is inversely proportional to load size, given sufficient load inductance.
- Auxiliary resistive wires installed over each contactor terminal were able to reduce in-rush currents from a maximum of 11 kA to 3.5 kA, thereby increasing contactor lifespan.
- Calculations show that a project based on the hybrid system would be financially viable subject to load size and load power factor restrictions.
- The hybrid system was successfully installed in a laboratory environment and successfully de-rated with additional capacitors to a one in thirty scale model. All current measurements were calibrated and tested to read the correct scaled values (thirty times larger than the real value). Overflow errors encountered in the software during this process were corrected.
- All fault and emergency stop conditions were tested and were found to operate according to specifications. All contactors were removed from the utility grid within 300 milliseconds of any fault or emergency stop condition.
- Electromagnetic interference was found to be the cause of the LCD malfunction. This interference was caused during contactor commutation and was reduced by adding inductance to the LCD signal cable near to the LCD module.

- Addition of capacitors from any filter was found to amplify harmonic content present on the utility grid, but was not significant enough to disrupt the grid or cause fault with any other machinery connected to the grid. No other resonance conditions were detected.
- The DSP unbalance control algorithm was tested and compared to the required switching pattern returned by the simulation program. Both switching patterns were identical for many different unbalance situations and resulted in the reduction of unbalance as seen by the source.
- Data logging during several test runs show a decrease in the spread of the phase currents, apparent power and real power whilst reactive power was reduced to near zero.
- Filter switching patterns were found to be slightly oscillatory near transition periods despite the addition of hysteresis in the control algorithm. This was attributed to the fact that power measurements are unsteady due to the scaled up current measurements. This problem should be reduced when installed onto a full scale load.
- Harmonic interference was found to be the cause of the inflation of the unbalance measurement results. This was verified with the computer simulation package, MATLAB, and a new measure of unbalance was developed. A comparison of the two measures of unbalance was performed in simulation and found that both measures return similar results for the same load (refer to appendix I).
- The unit was able to reduce the source side unbalance of the test load by an average of 3 percent over several logging periods. This is comparable to the 3.5 percent reduction attained in simulation.

## **13 Recommendations**

The author recommends that the continuation of the project should proceed as follows:

- Connect the unit to a full scale, unbalanced load and test the operability of the system under those conditions.
- Build a user-friendly graphical user interface for a personal computer through which all system data variables may be monitored and system set points may be changed. Retrieval and subsequent graphing of data logs stored on the unit's flash card should also be included.
- Write software to interface through the WiFi connection to a host PC, upon which the above interface is installed such that remote monitoring and logging is possible.

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# Appendices

<b>Appendix A:</b>	<b><math>\Delta</math>-Y and Y-<math>\Delta</math> Transformations</b>
<b>Appendix B:</b>	<b>Reference Frame Transformation Proofs</b>
<b>Appendix C:</b>	<b>Symmetrical Component Decomposition</b>
<b>Appendix D:</b>	<b>Embedded MATLAB Function Code</b>
<b>Appendix E:</b>	<b>Multi-Interface Controller Board Schematics</b>
<b>Appendix F:</b>	<b>Set-Point and Data-Point Descriptions</b>
<b>Appendix G:</b>	<b>Bill of Materials and Costing</b>
<b>Appendix H:</b>	<b>Harmonic Impact on Unbalance Calculation Algorithm</b>
<b>Appendix I:</b>	<b>Unbalance Calculation with Real and Reactive Powers Using Standard Deviation from the Mean</b>

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## Appendix A $\Delta$ -Y and Y- $\Delta$ Transformations

### I. $\Delta$ -Y Transformation

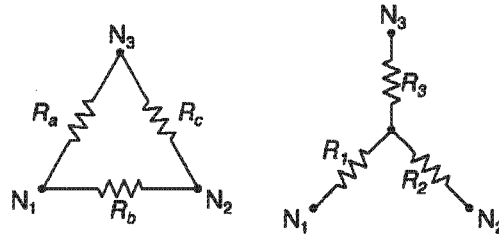


Figure: Delta Wye Equivalent Circuits [11]

If it is assumed that  $R_a$ ,  $R_b$  and  $R_c$  from the delta configuration is known, then if  $N_3$  is not connected in the delta configuration [11]:

$$\text{Resistance from } N_1 \text{ to } N_2 (\Delta), R_{(N_1, N_2)} = R_b \parallel (R_a + R_c) = \frac{R_b(R_a + R_c)}{R_a + R_b + R_c} = \frac{R_a R_b + R_b R_c}{R_a + R_b + R_c}$$

$$\text{Resistance from } N_1 \text{ to } N_2 (\Delta), R_{(N_1, N_2)} = R_1 + R_2$$

$$\text{Thus, } R_1 + R_2 = \frac{R_a R_b + R_b R_c}{R_a + R_b + R_c} \quad (1)$$

$$\text{Similarly: } R_2 + R_3 = \frac{R_c R_a + R_c R_b}{R_a + R_b + R_c} \quad (2) \quad \text{and} \quad R_3 + R_1 = \frac{R_a R_b + R_a R_c}{R_a + R_b + R_c} \quad (3)$$

By adding the two equations (1) and (3), and subtracting (2) yields:

$$R_1 + R_2 + R_1 + R_3 - R_2 - R_3 = \frac{R_b R_a + R_b R_c}{R_a + R_b + R_c} + \frac{R_b R_a + R_a R_c}{R_a + R_b + R_c} + \frac{R_c R_a + R_b R_c}{R_a + R_b + R_c}$$

$$\text{Thus} \quad R_1 = \frac{R_a R_b}{R_a + R_b + R_c}$$

$$\text{Similarly} \quad R_2 = \frac{R_b R_c}{R_a + R_b + R_c}$$

$$R_3 = \frac{R_c R_a}{R_a + R_b + R_c}$$

## II. Y- Δ Transformation

Beginning with the equations calculated in section I:

$$R_1 = \frac{R_a R_b}{R_a + R_b + R_c} \quad (1) \quad R_2 = \frac{R_b R_c}{R_a + R_b + R_c} \quad (2) \quad R_3 = \frac{R_c R_a}{R_a + R_b + R_c} \quad (3)$$

Multiplying each equation pair yields:

$$R_1 R_2 = \frac{R_a R_b^2 R_c}{(R_a + R_b + R_c)^2} \quad (4) \quad R_1 R_3 = \frac{R_a^2 R_b R_c}{(R_a + R_b + R_c)^2} \quad (5) \quad R_2 R_3 = \frac{R_a R_b R_c^2}{(R_a + R_b + R_c)^2} \quad (6)$$

Summing all three equations above yields:

$$R_1 R_2 + R_1 R_3 + R_2 R_3 = \frac{R_a^2 R_b R_c + R_a R_b^2 R_c + R_a R_b R_c^2}{(R_a + R_b + R_c)^2} \quad (7)$$

Dividing (7) by  $R_1$  and substituting (1) into the result yields:

$$\frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_1} = \frac{R_c (R_a + R_b + R_c)}{R_a + R_b + R_c} \quad (8)$$

$$\text{Thus: } R_c = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_1} \quad (9)$$

Similarly, by dividing (7) by  $R_2$  and substituting (2), and by dividing (7) by  $R_3$  and substituting (3) yields the equations for  $R_a$  and  $R_b$ :

$$R_a = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_2} \quad (9) \quad R_b = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_3} \quad (10)$$

## Appendix B Reference Frame Transformation Proofs

When dealing with multiphase electrical systems, especially where manipulation of system parameters is taking place, simple system analysis is often required where the analysis of only a few variables is required to determine the instantaneous values of all system variables. For this purpose, reference frame transformations are utilized where each phase voltage or current is depicted in vectorial form on either a stationary or rotating reference frame. Each type of reference frame has its uses in control theory, where rotating reference frame are often used in control of electrical machines (where only two DC control variables need manipulation), whilst stationary reference frame are often used to determine the health or state of the system (where only two sinusoidal control variable require monitoring).

Since this thesis is dealing with the health of the utility grid and the manipulation thereof, the stationary reference frame analysis is used, the proof and operation of which is detailed below.

Let it be assumed that a balanced three phase electrical system exists, where the instantaneous phase current flowing in each of the three phases can each be represented by a vector, with magnitude equal to the instantaneous phase current and mutual  $120^\circ$  displacement. It follows that the addition of each of the phase vectors along its positive phase axis for positive instantaneous values, or negative phase axis for negative instantaneous values, will combine to form a resultant space vector that, by itself, describes that instantaneous state of the phase currents.

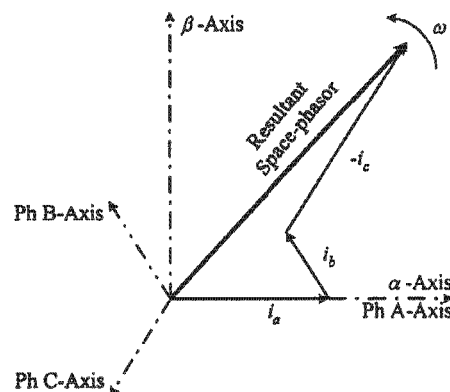


Figure: Combination of Individual Phase Vectors to Create the Resultant Space Vector [10]

The resultant space vector thus has a magnitude of one and a half times that of the peak phase current and may therefore be scaled by a factor of 2/3, such that the magnitude of the space vector equals that of the phase currents.

Algebraically, the resultant space vector may be calculated as follows:

$$\vec{I}_s = \frac{2}{3} \left[ I_a + I_b e^{j\frac{2\pi}{3}} + I_c e^{j\frac{4\pi}{3}} \right] \quad (1)$$

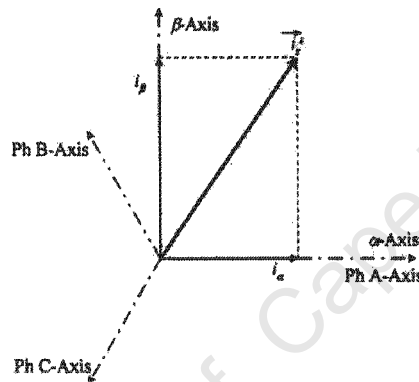


Figure: Resultant Space Vector in the Stationary Reference Frame [10]

Thus:

$$\vec{I}_s = i_\alpha + j i_\beta \quad (2)$$

By equating equations (1) and (2), the Clarke transformation is derived.

$$\begin{aligned} \vec{I}_s &= \frac{2}{3} \left[ I_a + I_b e^{j\frac{2\pi}{3}} + I_c e^{j\frac{4\pi}{3}} \right] \\ &= \frac{2}{3} \left[ I_a + I_b \left( \cos\left(\frac{2\pi}{3}\right) + j \sin\left(\frac{2\pi}{3}\right) \right) + I_c \left( \cos\left(\frac{4\pi}{3}\right) + j \sin\left(\frac{4\pi}{3}\right) \right) \right] \end{aligned}$$

So:

$$\vec{I}_s = \frac{2}{3} \left[ I_a - \frac{1}{2} I_b + j \frac{\sqrt{3}}{2} I_b - \frac{1}{2} I_c - j \frac{\sqrt{3}}{2} I_c \right]$$

And:

$$I_{\alpha} = \frac{2}{3} \left[ I_a - \frac{1}{2} I_b - \frac{1}{2} I_c \right]$$

$$I_{\beta} = \frac{2}{3} \left[ j \frac{\sqrt{3}}{2} I_b - \frac{\sqrt{3}}{2} I_c \right]$$

Thus:

$$\begin{bmatrix} I_{\alpha} \\ I_{\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

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## Appendix C Symmetrical Component Decomposition

The idea of symmetrical sequence decomposition was originally proposed by Charles Fortescue in a paper in 1918, in which he proposed that a three phase system can be decomposed into three components: zero sequence, negative sequence and positive sequence components. From [11], the sequences are defined as follows:

**Zero Sequence:** “Zero sequence components, consisting of three phasors with equal magnitudes and with zero phase displacement.”

**Negative Sequence:** “Negative sequence components, consisting of three phasors with equal magnitudes,  $\pm 120^\circ$  displacement and negative sequence.”

**Positive Sequence:** “Positive sequence components, consisting of three phasors with equal magnitudes,  $\pm 120^\circ$  displacement and positive sequence.”

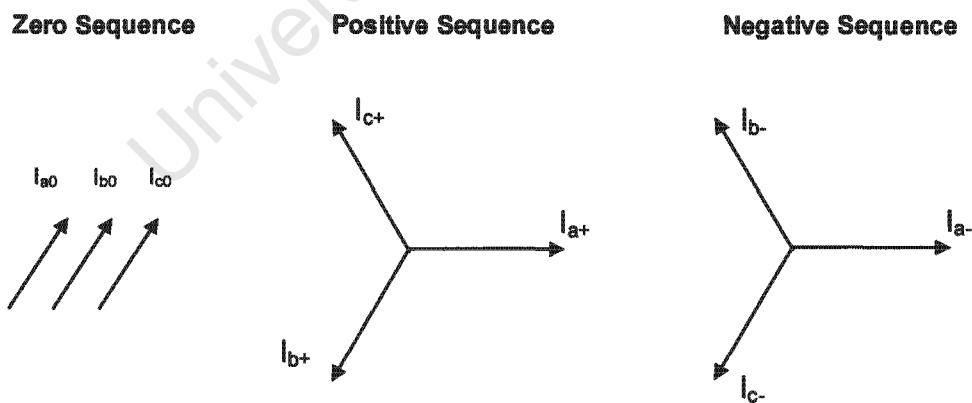


Figure: Decomposed Sequence Vector Diagrams

Each symmetrical sequence is composed in such a way that when re-combined with each other, the normal phase vectors are produced. Thus, from [11], the phase currents are calculated as follows:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} I_0 \\ I_+ \\ I_- \end{bmatrix}$$

Where  $a = 1e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$

To find the three sequences in terms of the phase currents, the transfer matrix must be inverted, for this to be possible, the matrix must have a non-zero determinant [33]:

$$\text{Determinant}(A) = \begin{vmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{vmatrix}$$

$$|A| = 1 \begin{vmatrix} a^2 & a \\ a & a^2 \end{vmatrix} - 1 \begin{vmatrix} 1 & a \\ 1 & a^2 \end{vmatrix} + 1 \begin{vmatrix} 1 & a^2 \\ 1 & a \end{vmatrix} = a^4 - a^2 - a^2 + a + a - a^2$$

But, since  $a = e^{j\frac{2\pi}{3}}$ , then  $a^4 = a$

$$|A| = -3a^2 + 3a$$

'A' Thus has a non-zero determinant and may be invertible.

Finding the cofactor matrix of A [34]:

$$\text{Cofactor}(A) = \begin{bmatrix} (a^4 - a^2) & (a - a^2) & (a - a^2) \\ (a - a^2) & (a^2 - 1) & (1 - a) \\ (a - a^2) & (1 - a) & (a^2 - 1) \end{bmatrix}$$

Thus:

$$A^{-1} = \frac{1}{|A|} \text{Cofactor}(A) = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \left(\frac{a^2-1}{a-a^2}\right) & \left(\frac{1-a}{a-a^2}\right) \\ 1 & \left(\frac{1-a}{a-a^2}\right) & \left(\frac{a^2-1}{a-a^2}\right) \end{bmatrix}$$

But:  $\left(\frac{a^2-1}{a-a^2}\right) = \left(\frac{a^2-1}{a-a^{-1}}\right) = \left(\frac{a(a^2-1)}{a^2-1}\right) = a \quad (\text{since } a^2 = a^{-1})$

Also:  $\left(\frac{1-a}{a-a^2}\right) = \left(\frac{1-a}{a(1-a)}\right) = \frac{1}{a} = a^{-1} = a^2$

$$A^{-1} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}$$

The current sequences can now be written in terms of the current vectors:

$$\begin{bmatrix} I_0 \\ I_+ \\ I_- \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

Thus, for a positive sequence utility grid connection, the Clarke transformation may be represented as follows:

$$I_+ = I_\alpha + jI_\beta = \frac{1}{3} \left( I_a + \left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right) I_b + \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right) I_c \right)$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

## Appendix D Embedded MATLAB Function Code

```

function [Pcab,Pcbc,Pcca,Pca,Pcb,Pcc,PFC] = fcn(Pa, Qa, Pb,Qb, Pc,Qc)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Function to calculate the value of all delta, wye and power factor correction filters required to bring an inductive, %
% unbalanced load to a fully balanced load at unity power factor %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Pave = (1/3)*(Pa + Pb + Pc); % Calculate average real power flow per phase.
deltaPa = Pa - Pave; % Calculate deviation per phase from the mean.
deltaPb = Pb - Pave;
deltaPc = Pc - Pave;

s = 0; % Clear all variables.
Pcab = 0;
Pcbc = 0;
Pcca = 0;
Pca = 0;
Pcb = 0;
Pcc = 0;
PFC = 0;
Scale = 0;

if deltaPa>0 % Find the number of deviations that are above
    s = s+1; % the mean. Because at least one of the deviations
end % must be negative, 's' must either be 1 or 2.

if deltaPb>0
    s = s+1;
end

if deltaPc>0
    s = s+1;
end

% Start of actual algorithm

if (s == 1) % If only one deviation is above the mean.
    if deltaPa >0
        Pcab = deltaPa*2*(sqrt(3)); % Calculate required delta filter capacitors
        Pcbc = -deltaPc*2*(sqrt(3)); % According to: Ptx = 2*sqrt(3)*DeltaPn
    end
    if deltaPb >0
        Pcbc = deltaPb*2*(sqrt(3));
        Pcca = -deltaPa*2*(sqrt(3));
    end
end

```

```

if deltaPc > 0
    Pcca = deltaPc*2*(sqrt(3));
    Pcab = -deltaPb*2*(sqrt(3));
end
end

if (s == 2) % If two deviations are above the mean.
    if deltaPa < 0
        Pcbc = deltaPb*2*(sqrt(3));
        Pcca = (deltaPb + deltaPc)*2*(sqrt(3));
    end

    if deltaPb < 0
        Pcca = deltaPc*2*(sqrt(3));
        Pcab = (deltaPc + deltaPa)*2*(sqrt(3));
    end

    if deltaPc < 0
        Pcab = deltaPa*2*(sqrt(3));
        Pcbc = (deltaPa + deltaPb)*2*(sqrt(3));
    end
end

% So that the system does not go into leading power factor, if any phase will enter a leading power factor state, scale
% back delta filter values.

% Test for possible leading power factors
if (((0.5*Pcab + 0.5*Pcca) > Qa) || ((0.5*Pcab + 0.5*Pcbc) > Qb) || ((0.5*Pcbc + 0.5*Pcca) > Qc))

    % If Phase 'A' will be the first phase to enter a leading power factor state, scale until 'A' is unity power factor.
    if (((0.5*Pcab + 0.5*Pcca - Qa) > (0.5*Pcab + 0.5*Pcbc - Qb)) && ((0.5*Pcab + 0.5*Pcca - Qa) > (0.5*Pcbc + 0.5*Pcca - Qc)))
        Scale = Qa/(0.5*Pcab + 0.5*Pcca);
    End

    % If Phase 'B' will be the first phase to enter a leading power factor state, scale until 'B' is unity power factor.
    if (((0.5*Pcab + 0.5*Pcbc - Qb) > (0.5*Pcab + 0.5*Pcca - Qa)) && ((0.5*Pcab + 0.5*Pcbc - Qb) > (0.5*Pcbc + 0.5*Pcca - Qc)))
        Scale = Qb/(0.5*Pcab + 0.5*Pcbc);
    End

    % If Phase 'C' will be the first phase to enter a leading power factor state, scale until 'C' is unity power factor.
    if (((0.5*Pcbc + 0.5*Pcca - Qc) > (0.5*Pcab + 0.5*Pcca - Qa)) && ((0.5*Pcbc + 0.5*Pcca - Qc) > (0.5*Pcab + 0.5*Pcbc - Qb)))
        Scale = Qc/(0.5*Pcbc + 0.5*Pcca);
    end

    Pcab = Scale * Pcab; % Scale each capacitor value down if needed.
    Pcbc = Scale * Pcbc;
    Pcca = Scale * Pcca;

end

```

% Calculations for Wye connected Caps:

$P_{ca} = Q_a - (0.5 \cdot P_{cab} + 0.5 \cdot P_{cca});$

$P_{cb} = Q_b - (0.5 \cdot P_{cab} + 0.5 \cdot P_{cbc});$

$P_{cc} = Q_c - (0.5 \cdot P_{cbc} + 0.5 \cdot P_{cca});$

% Calculate total required Wye filter levels.

if( $P_{ca} > 0$  &&  $P_{cb} > 0$  &&  $P_{cc} > 0$ )

% If all three wye filters are needed,

% increase power factor correction level

% to the minimum of { $P_{ca}$ ,  $P_{cb}$ ,  $P_{cc}$ }.

% If 'A' is the least lagging phase.

if( $P_{ca} < P_{cb}$  &&  $P_{ca} < P_{cc}$ )

$PFC = P_{ca};$

end

% If 'B' is the least lagging phase.

if( $P_{cb} < P_{ca}$  &&  $P_{cb} < P_{cc}$ )

$PFC = P_{cb};$

end

% If 'C' is the least lagging phase.

if( $P_{cc} < P_{ca}$  &&  $P_{cc} < P_{cb}$ )

$PFC = P_{cc};$

end

$P_{ca} = P_{ca} - PFC;$

$P_{cb} = P_{cb} - PFC;$

$P_{cc} = P_{cc} - PFC;$

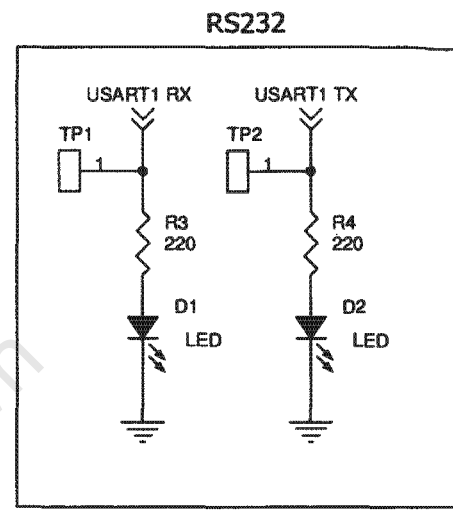
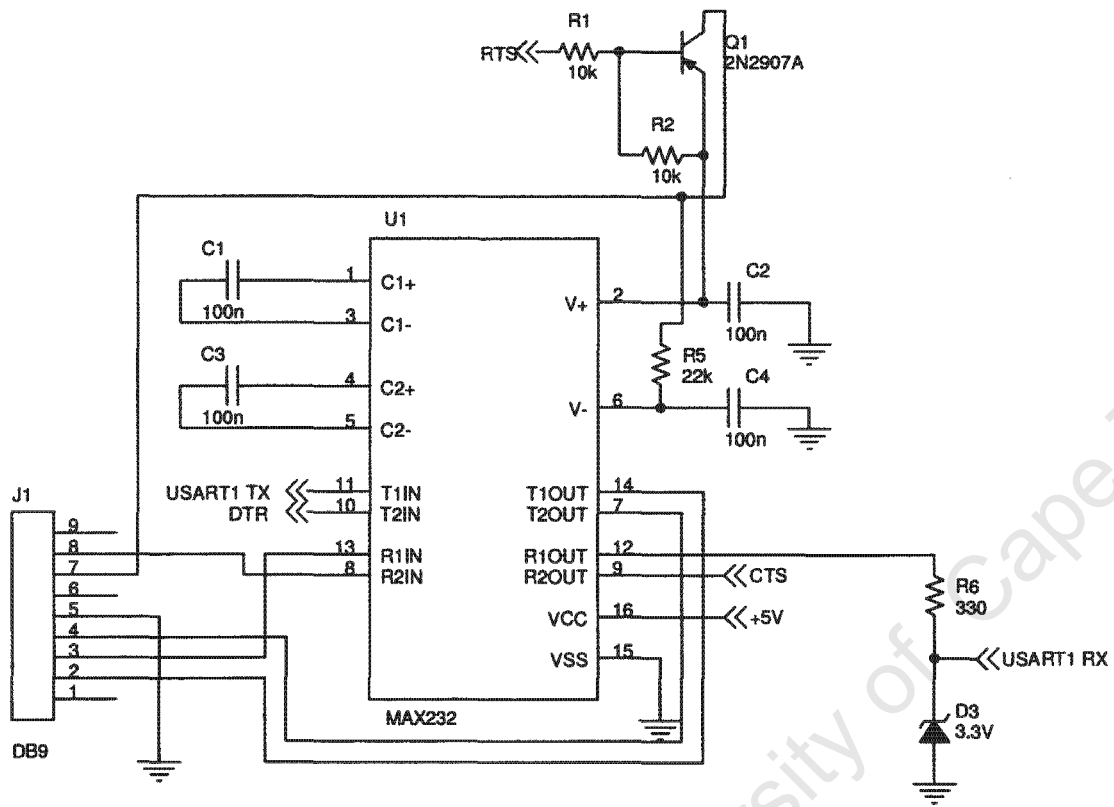
end

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## **Appendix E**

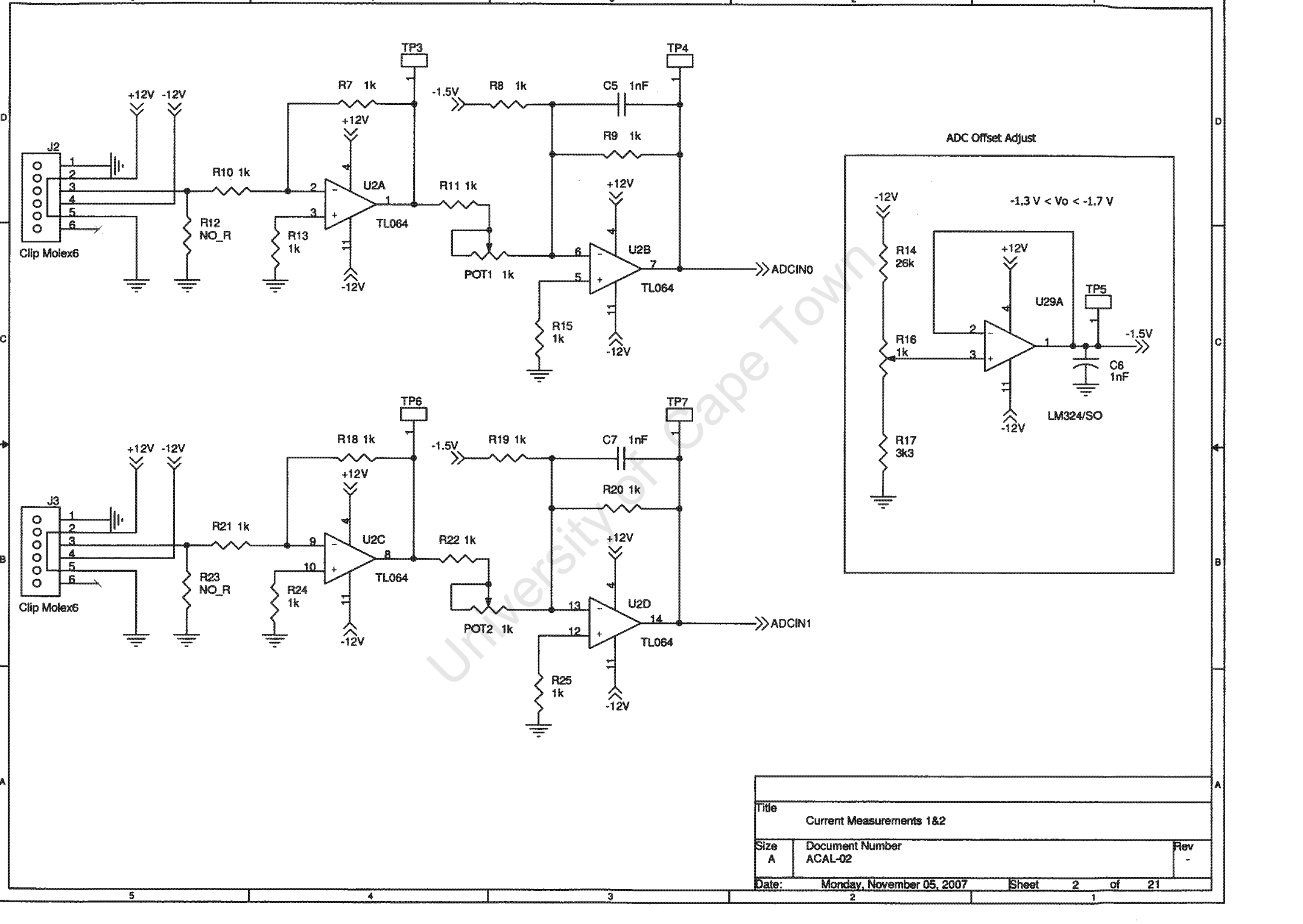
### **Multi-Interface Controller Board Schematics**

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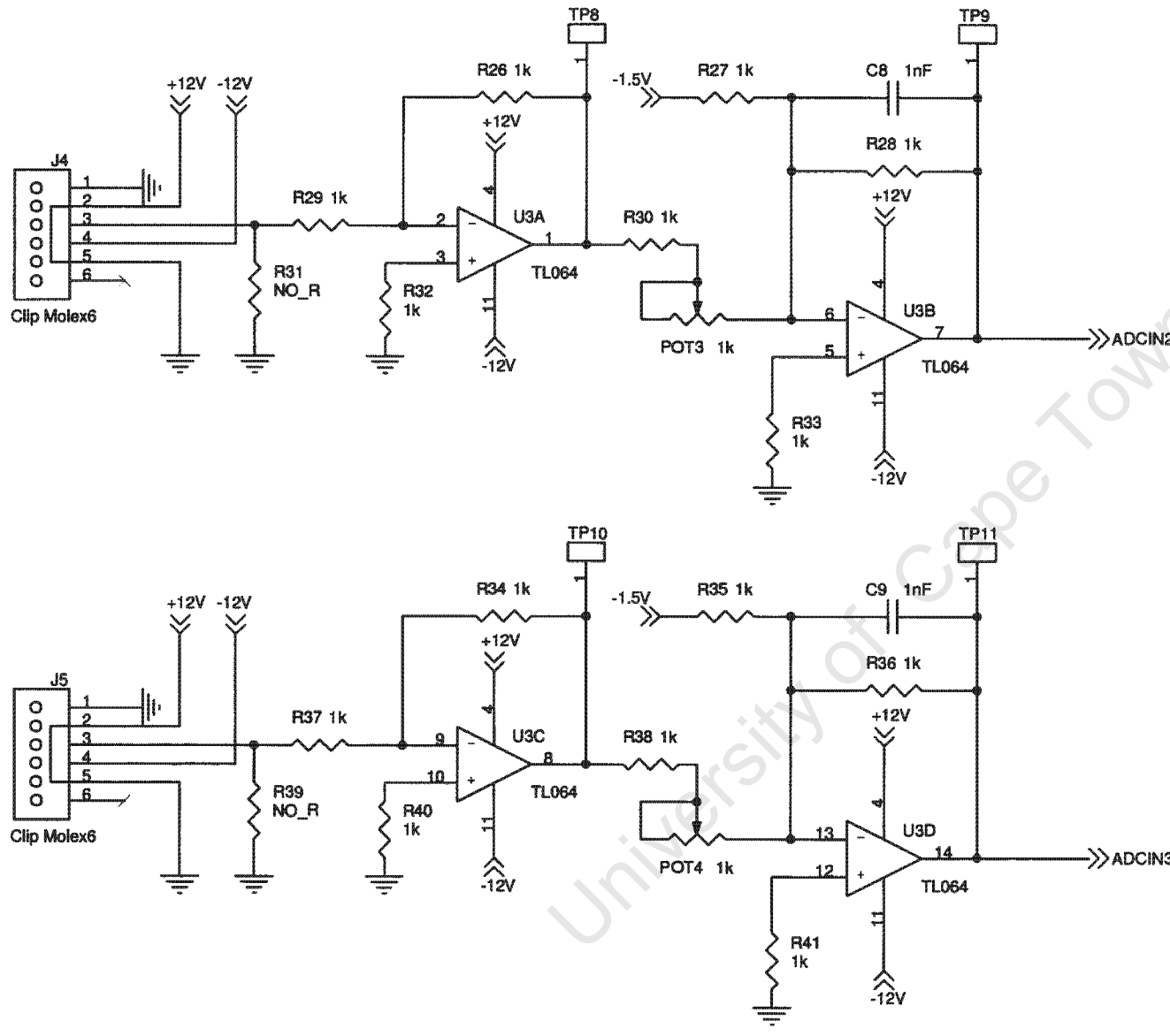


- ### DB9 Connections
- 1 - CD - Carrier Detect
  - 2 - RXD - Receive Data
  - 3 - TXD - Transmit Data
  - 4 - DTR - Data Terminal Ready
  - 5 - GND - System Ground
  - 6 - DSR - Data Set Ready
  - 7 - RTS - Request to Send
  - 8 - CTS - Clear to Send
  - 9 - RI - Ring Indicator

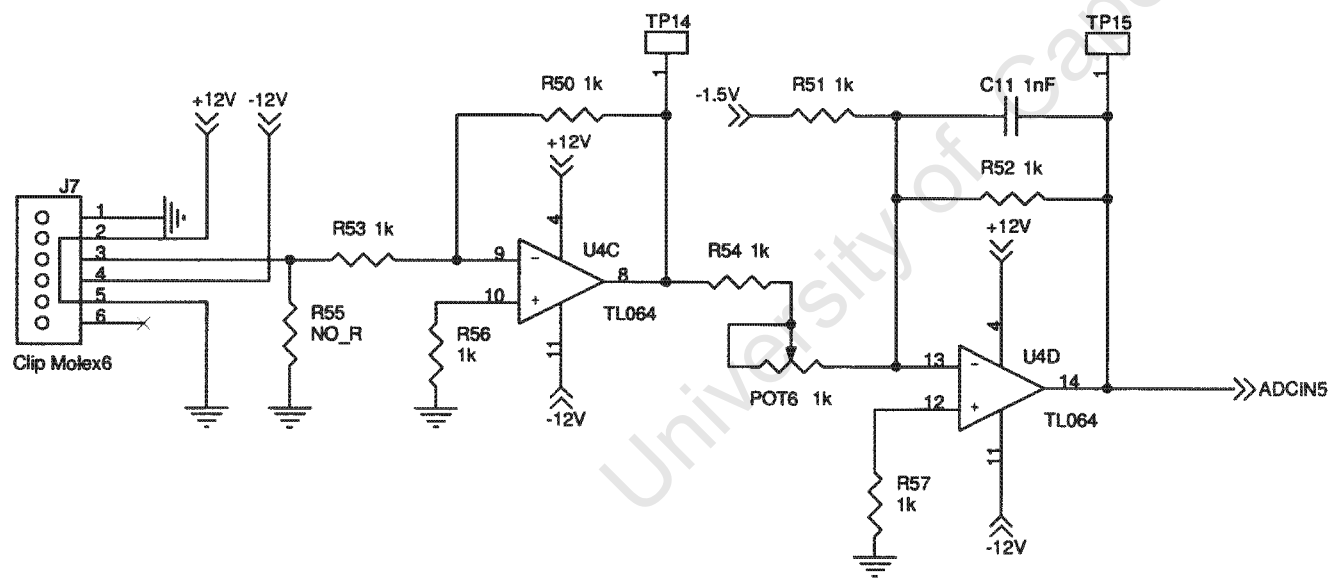
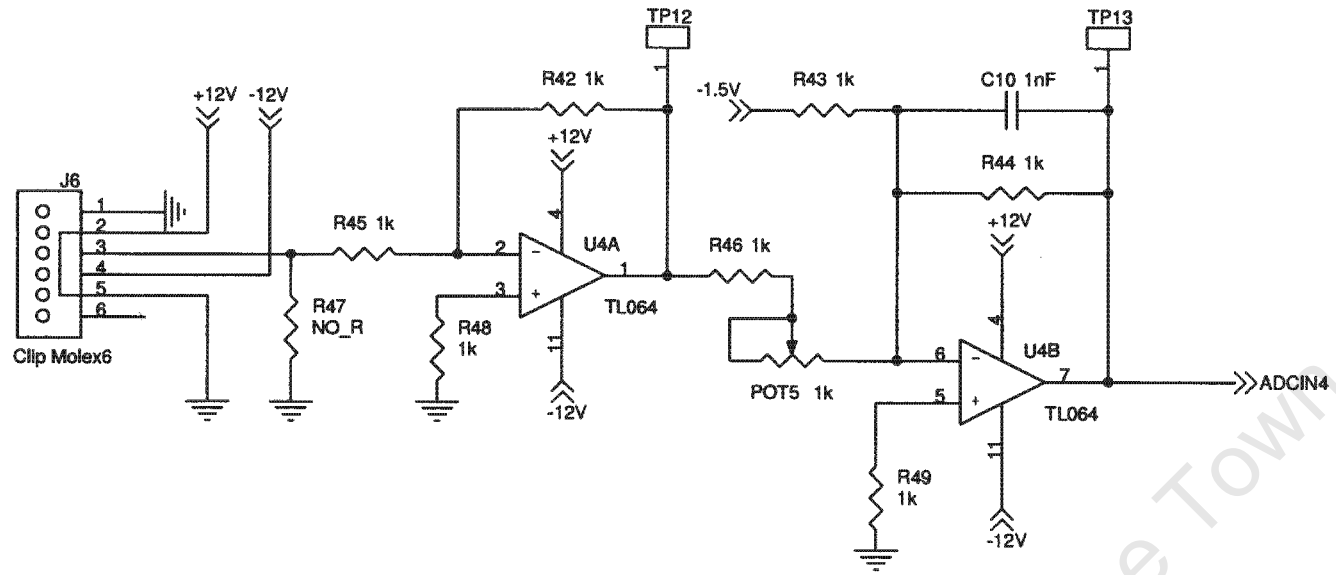
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Date:	Monday, November 05, 2007	Sheet 1 of 21



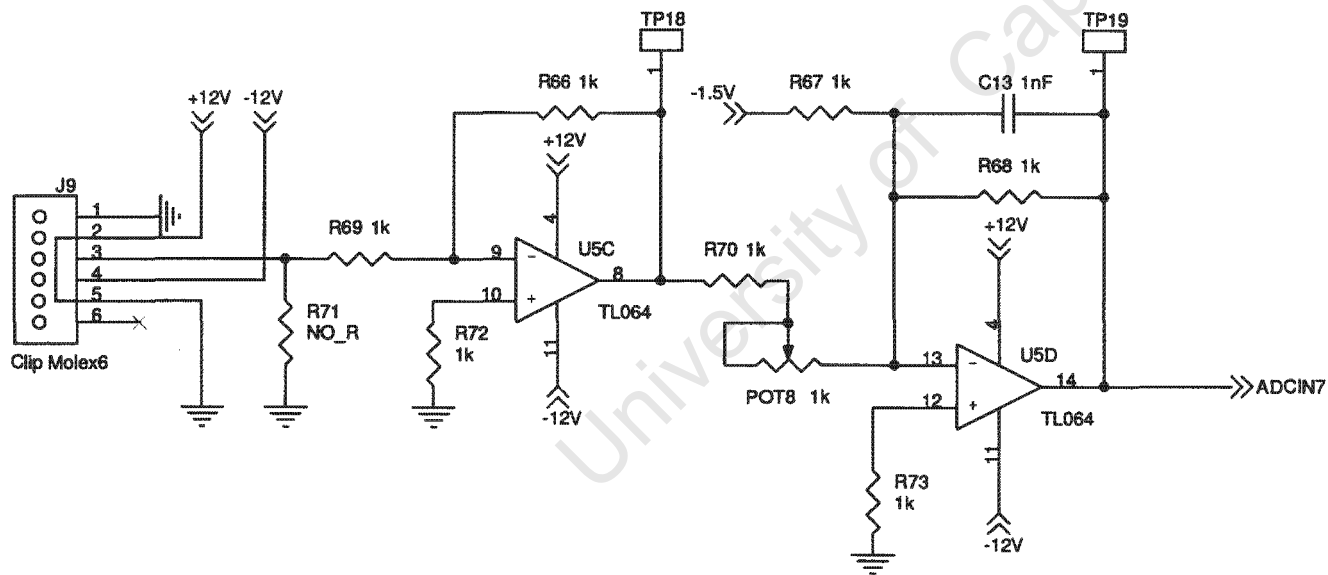
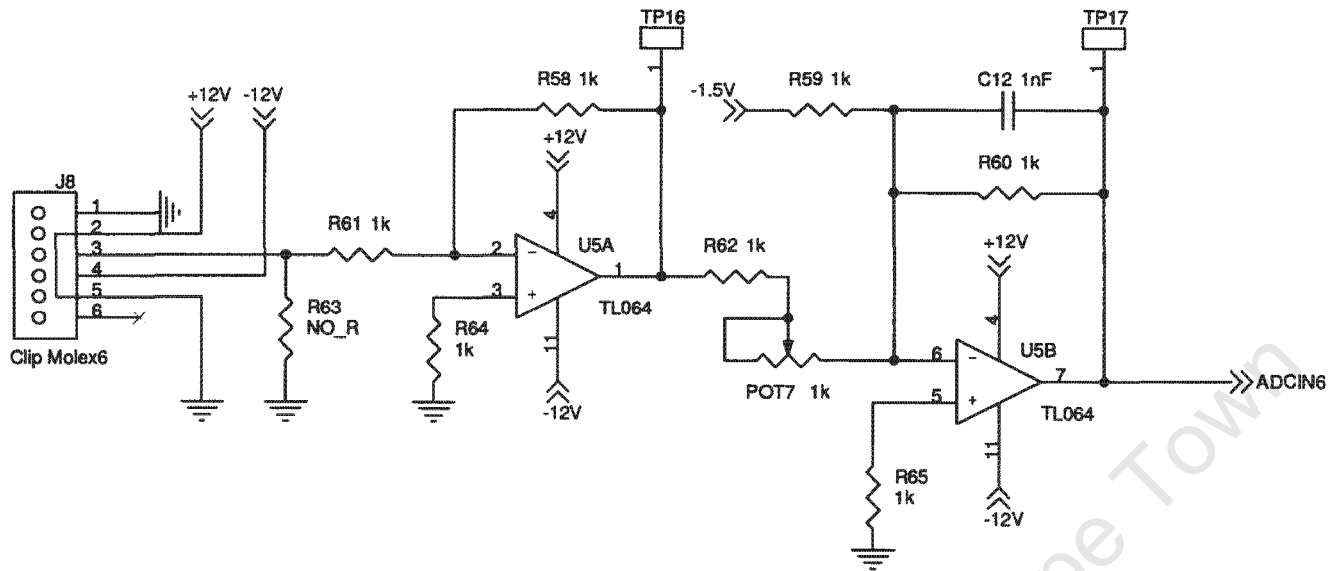
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Date:	Monday, November 05, 2007	Sheet 2 of 21



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Date:	Monday, November 05, 2007	Sheet 3 of 21

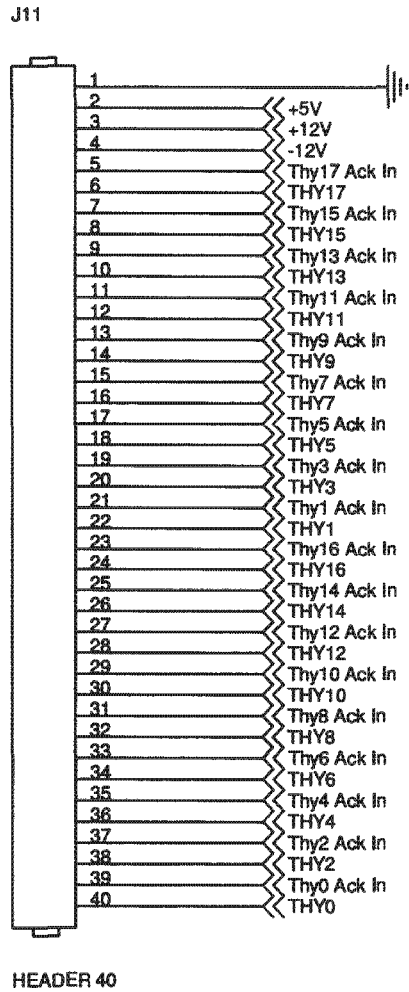


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Date:	Monday, November 05, 2007	Sheet 4 of 21

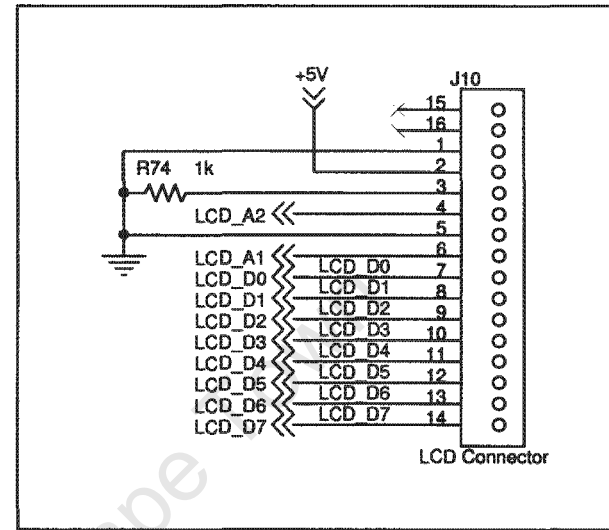


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Date:	Monday, November 05, 2007	Sheet 5 of 21

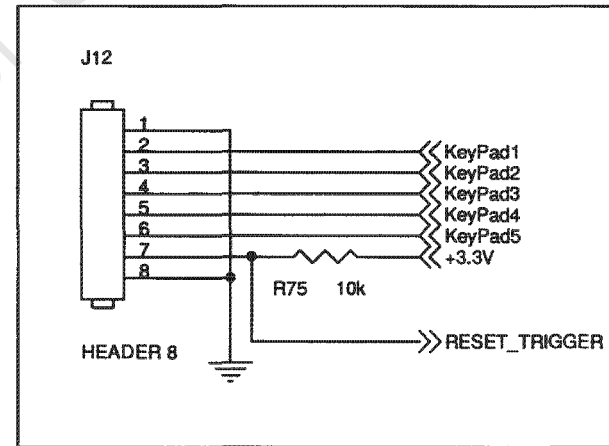
### IO Connections



### LCD Connector

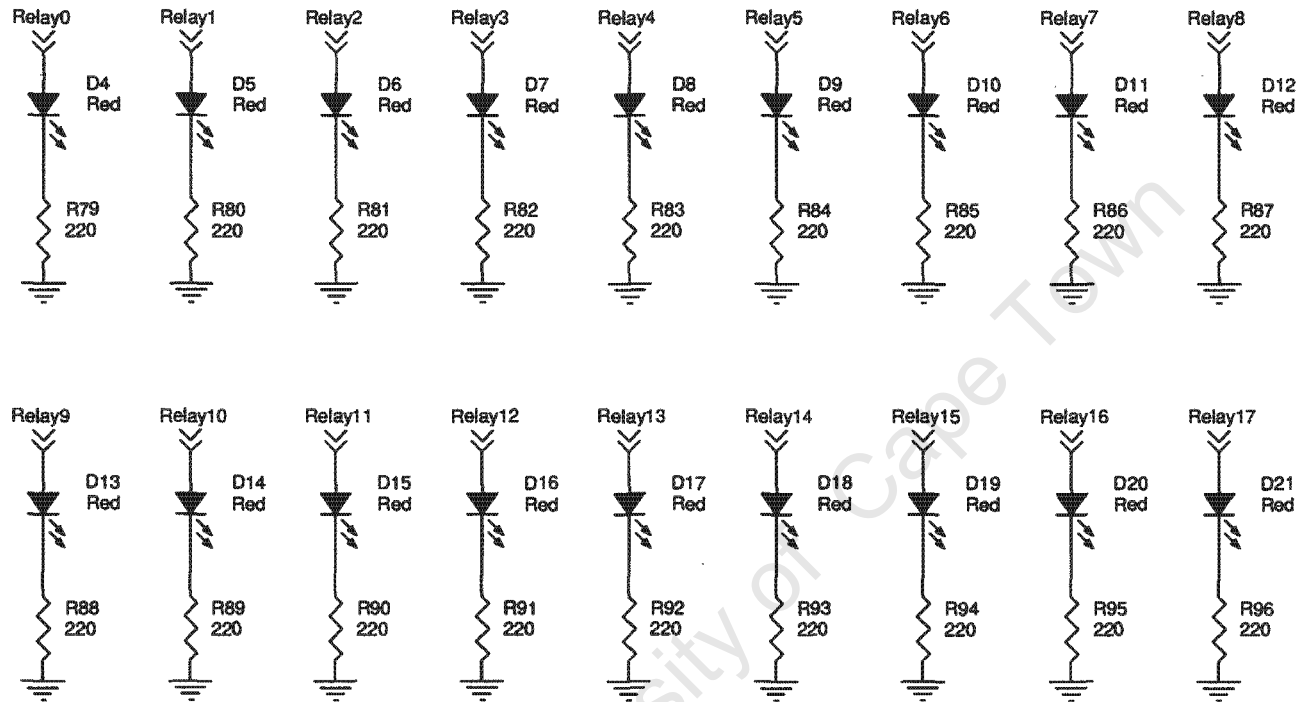


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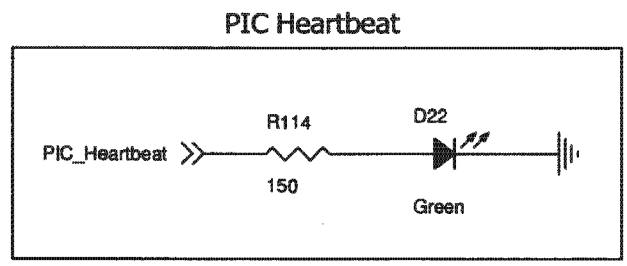
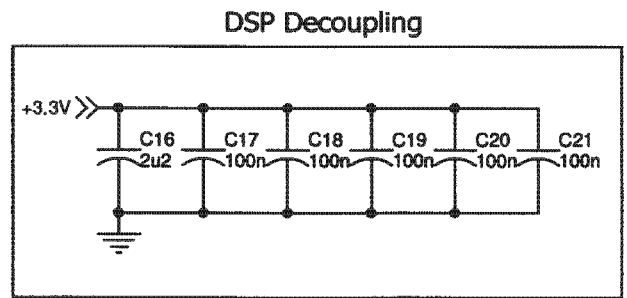
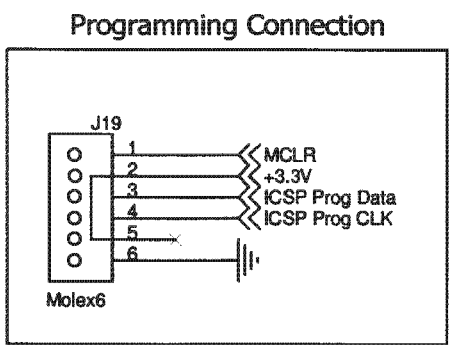
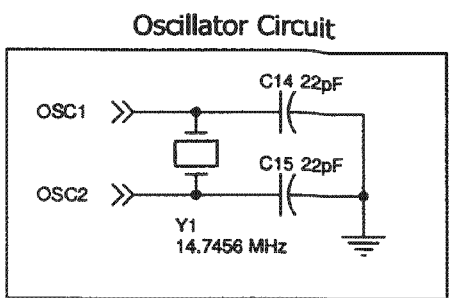
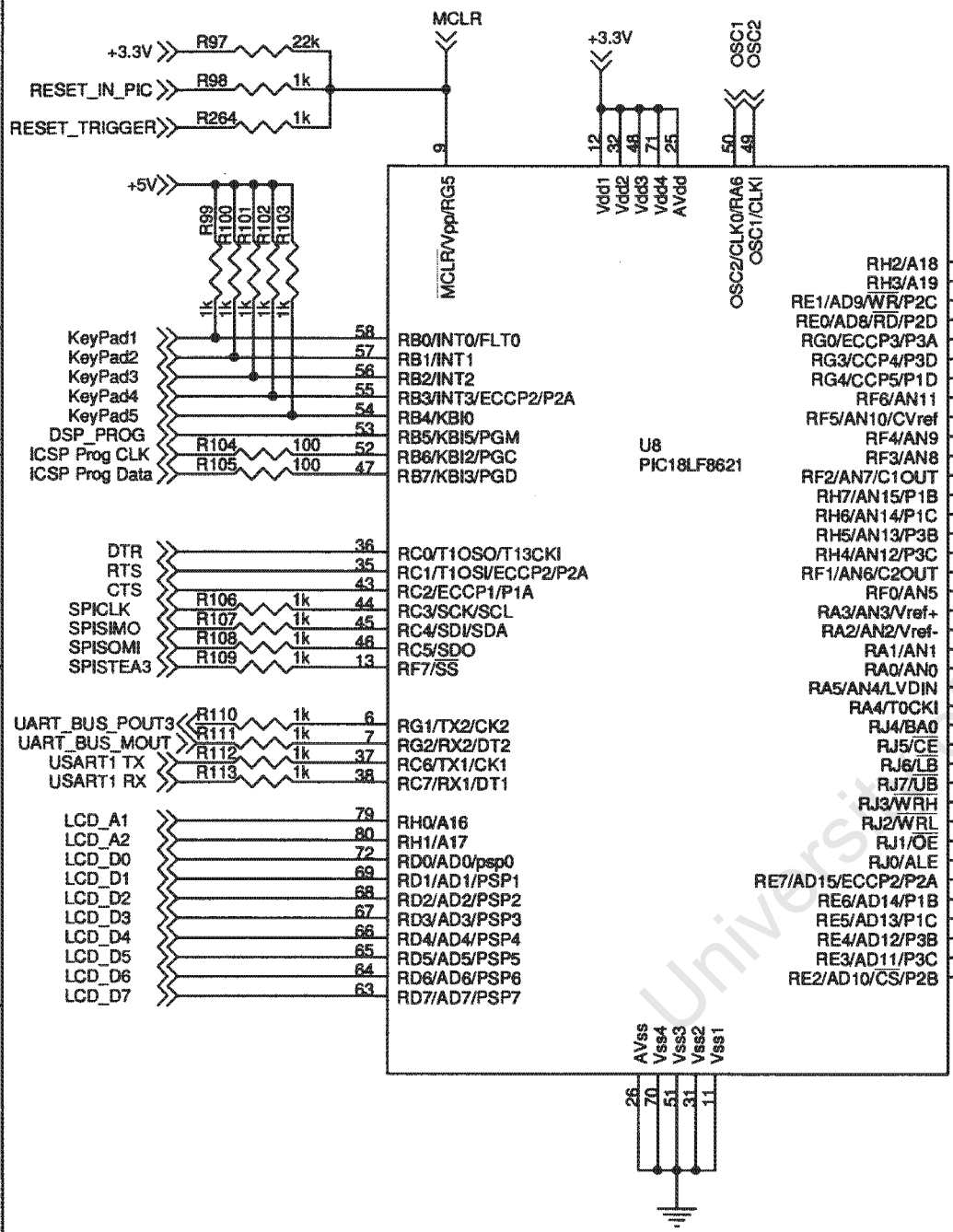


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Date:	Monday, November 05, 2007	Sheet 6 of 21



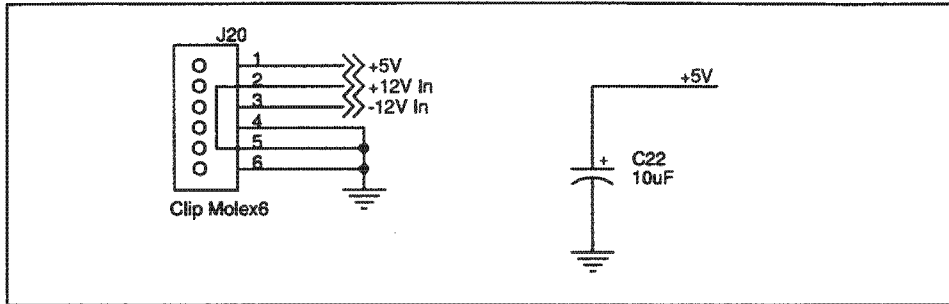


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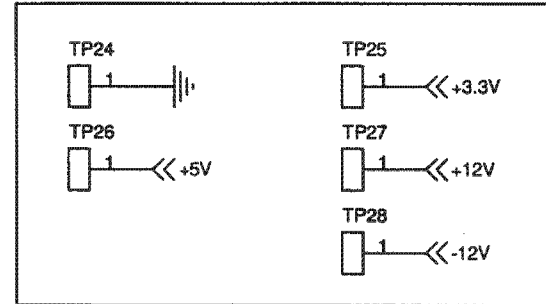


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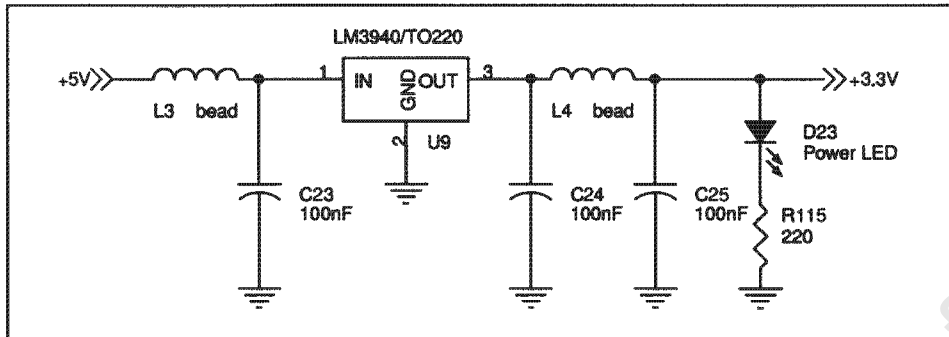
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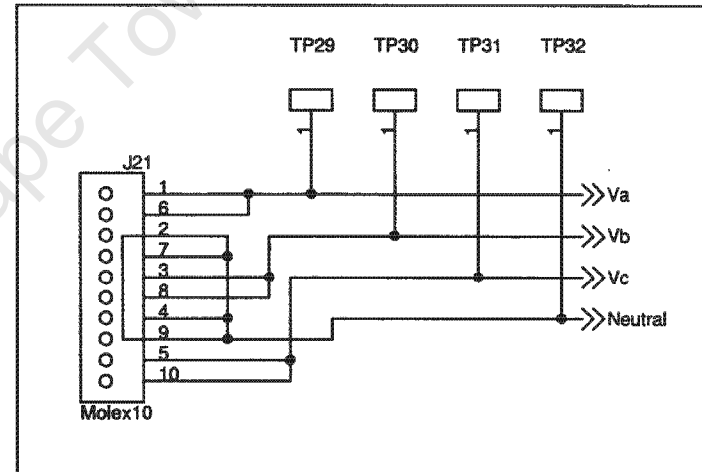
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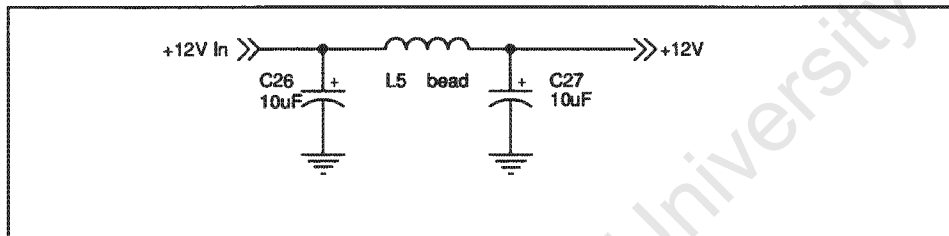
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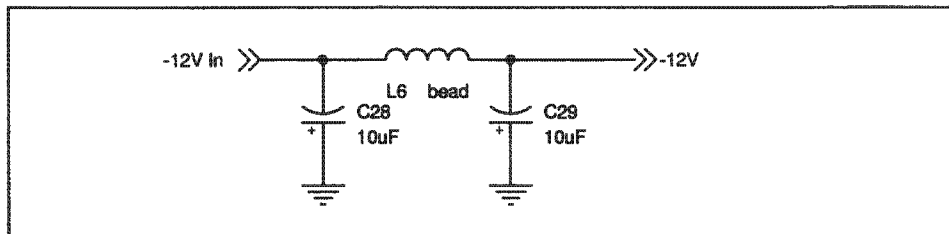
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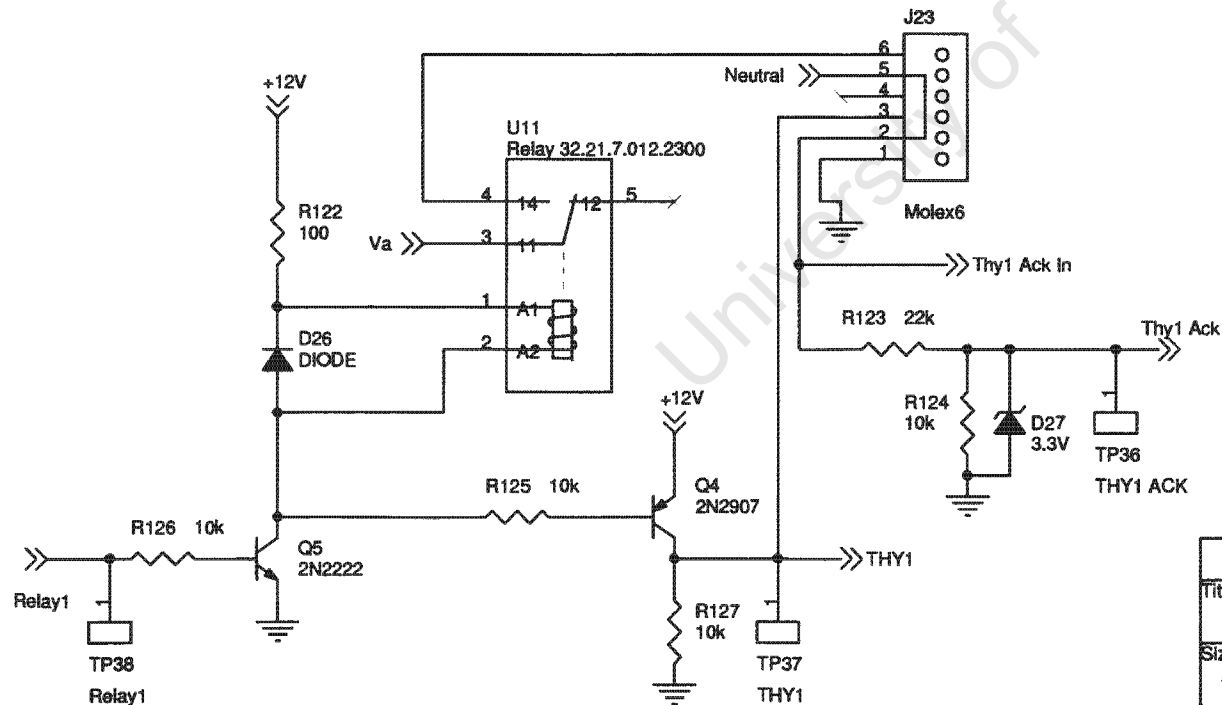
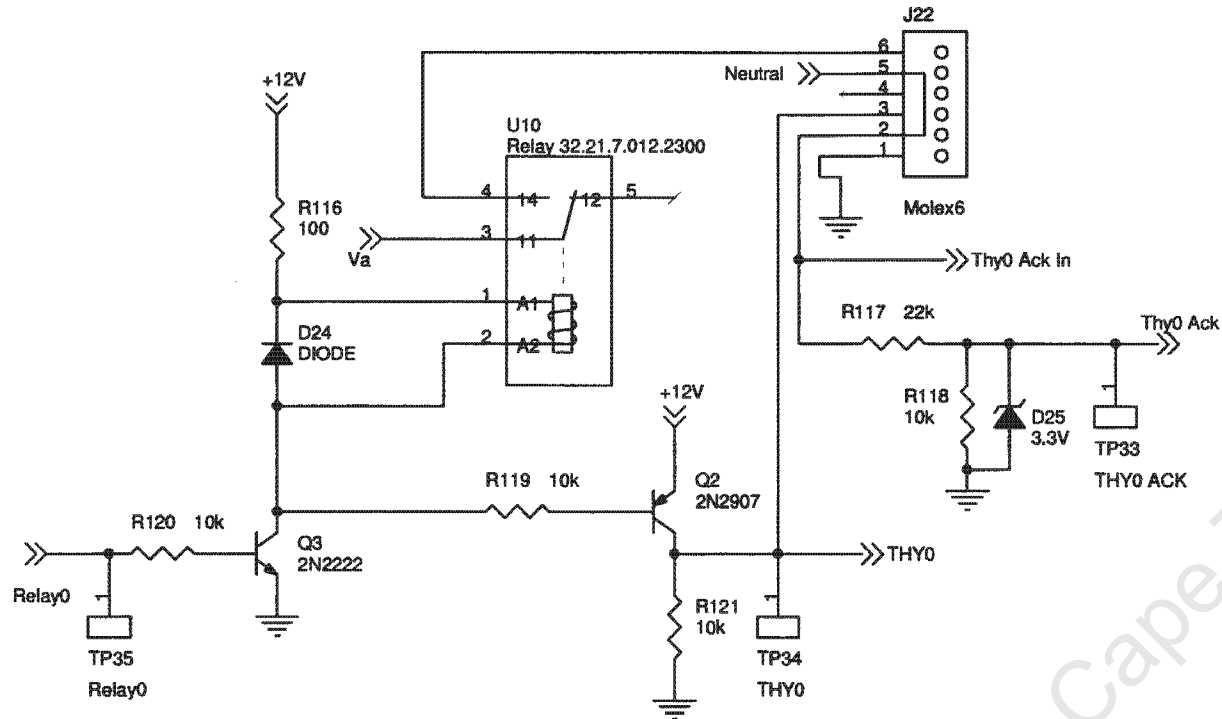
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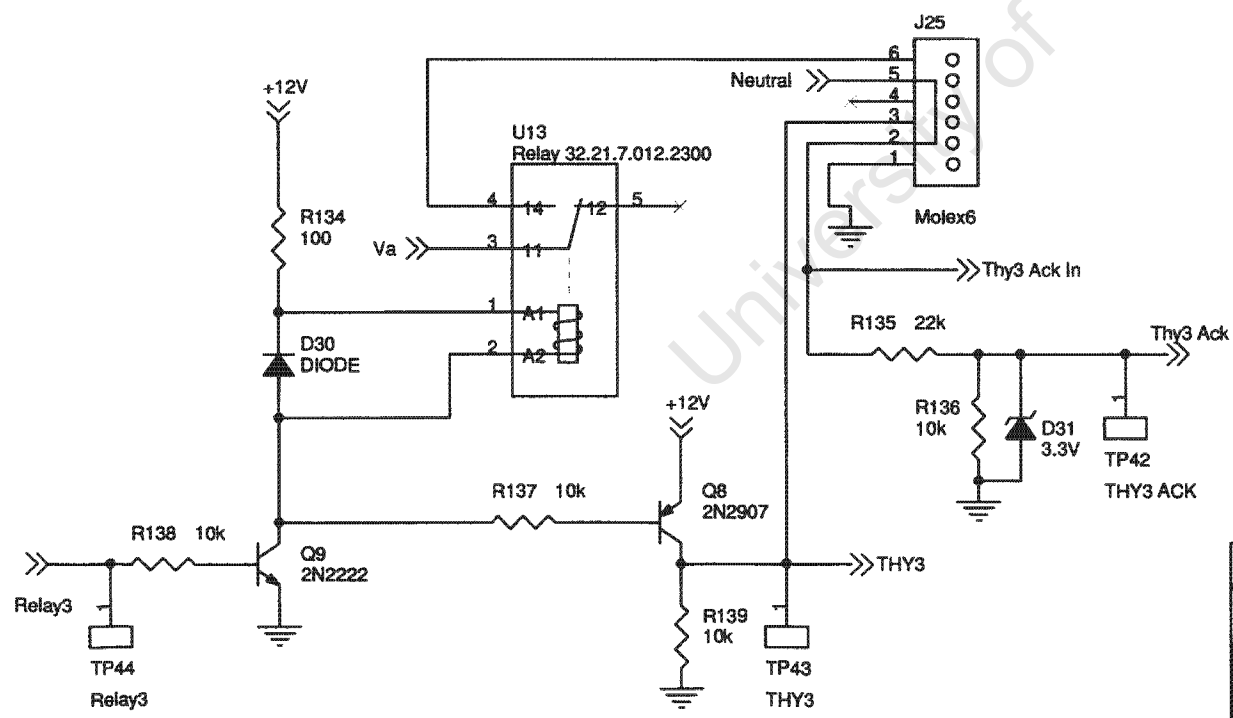
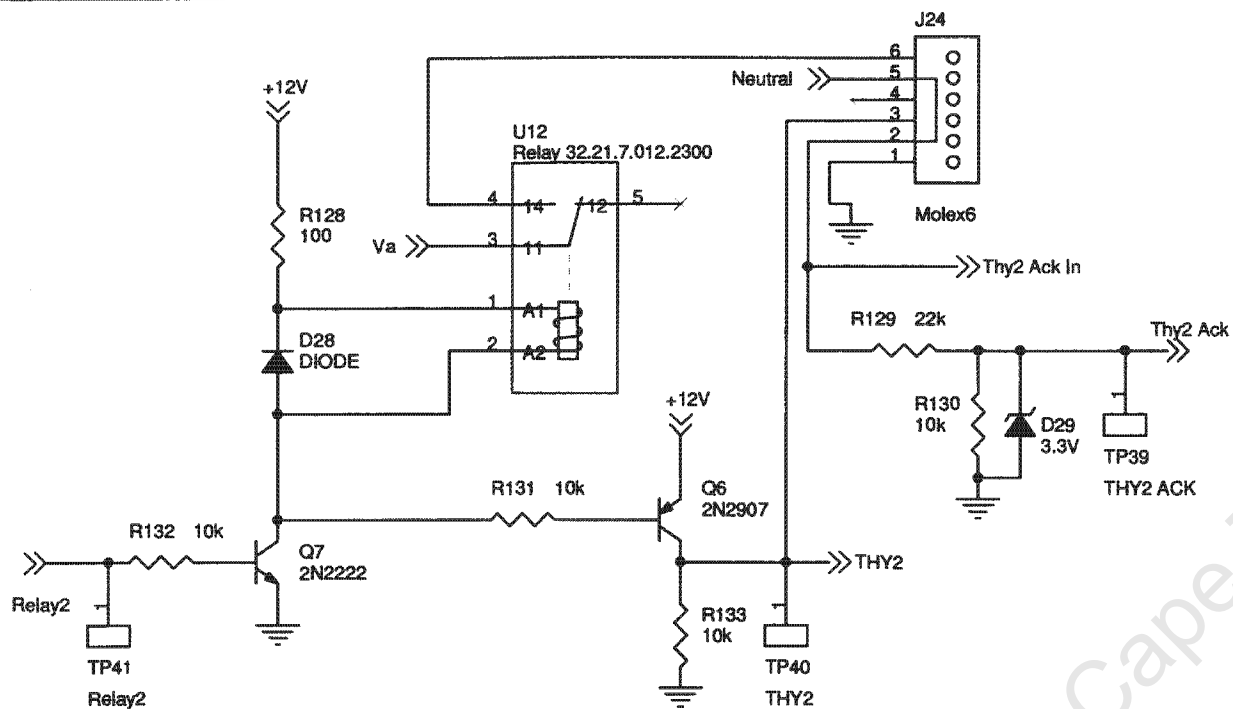
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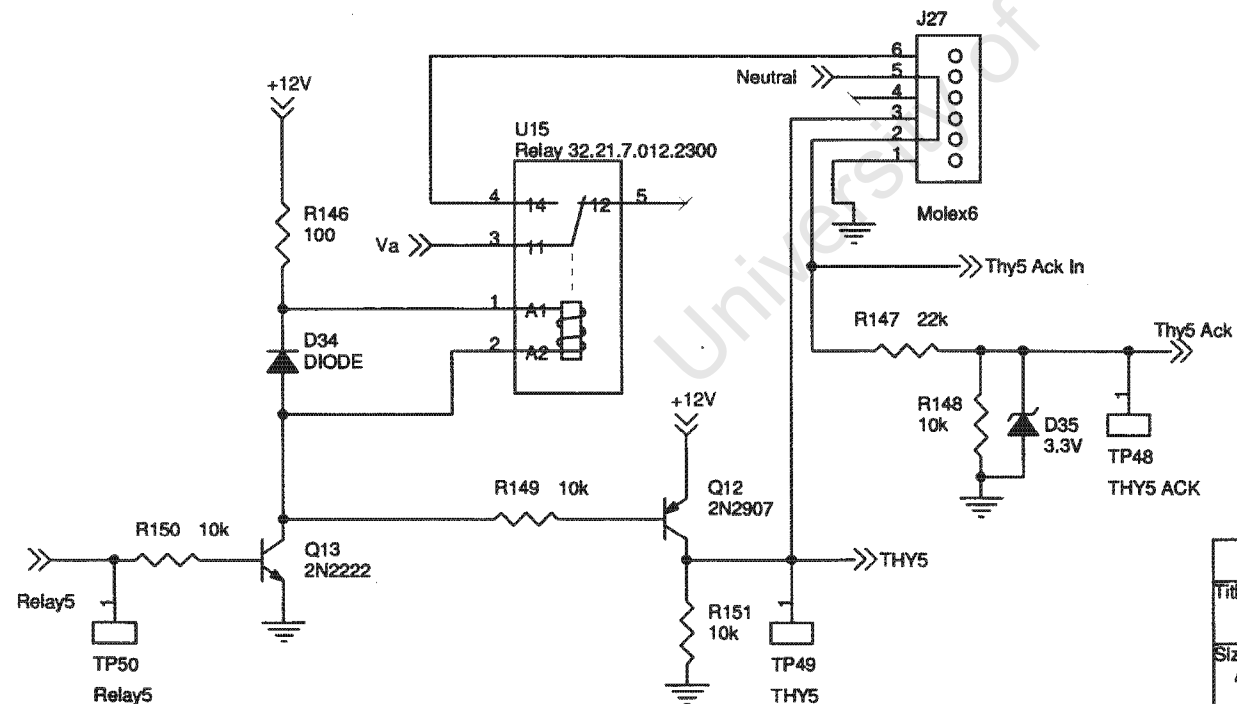
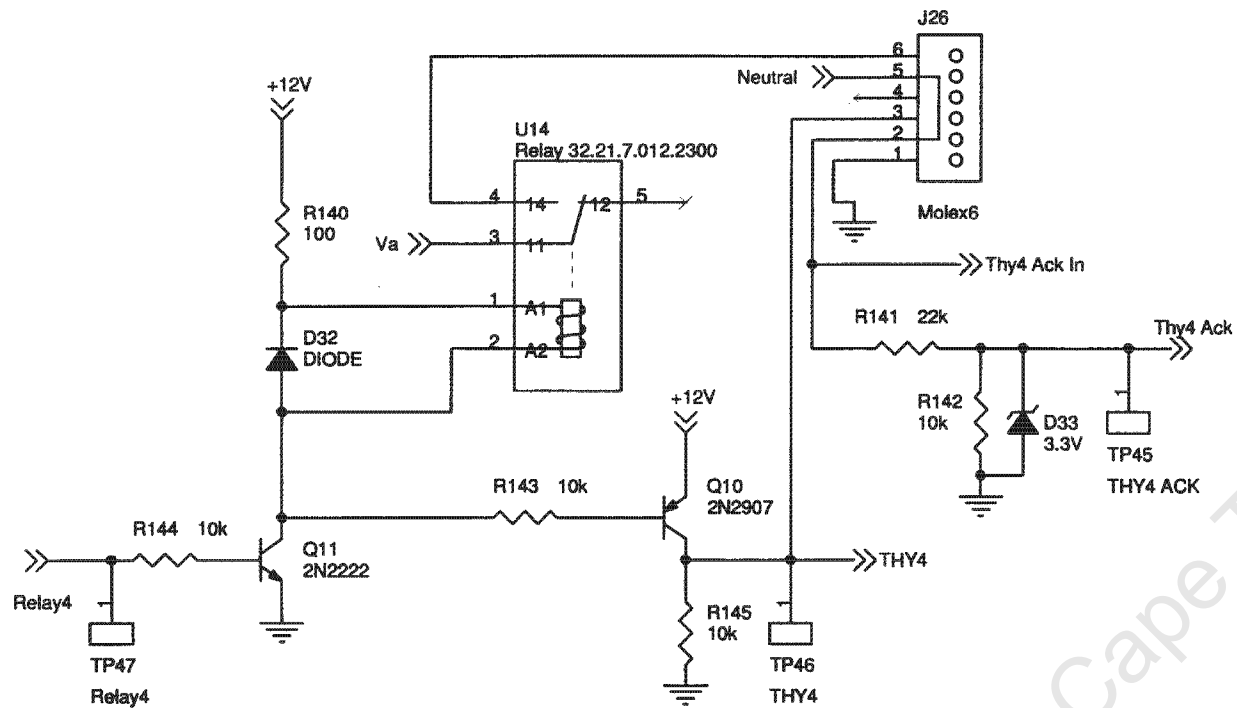
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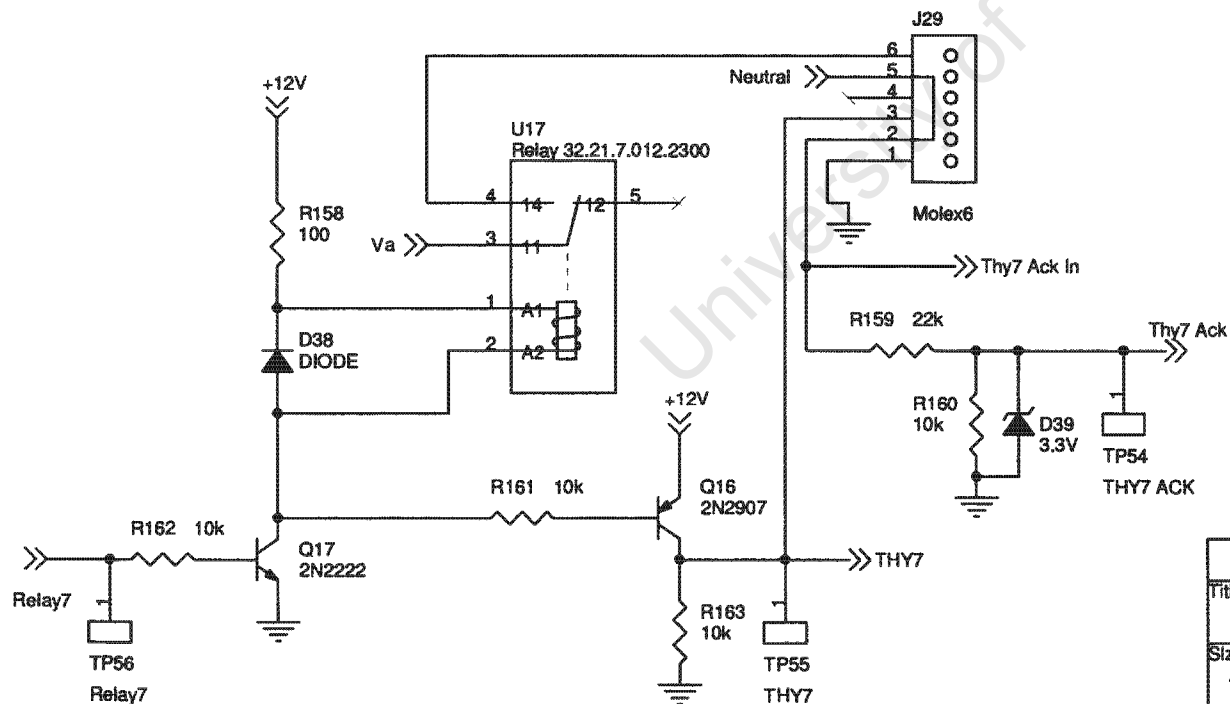
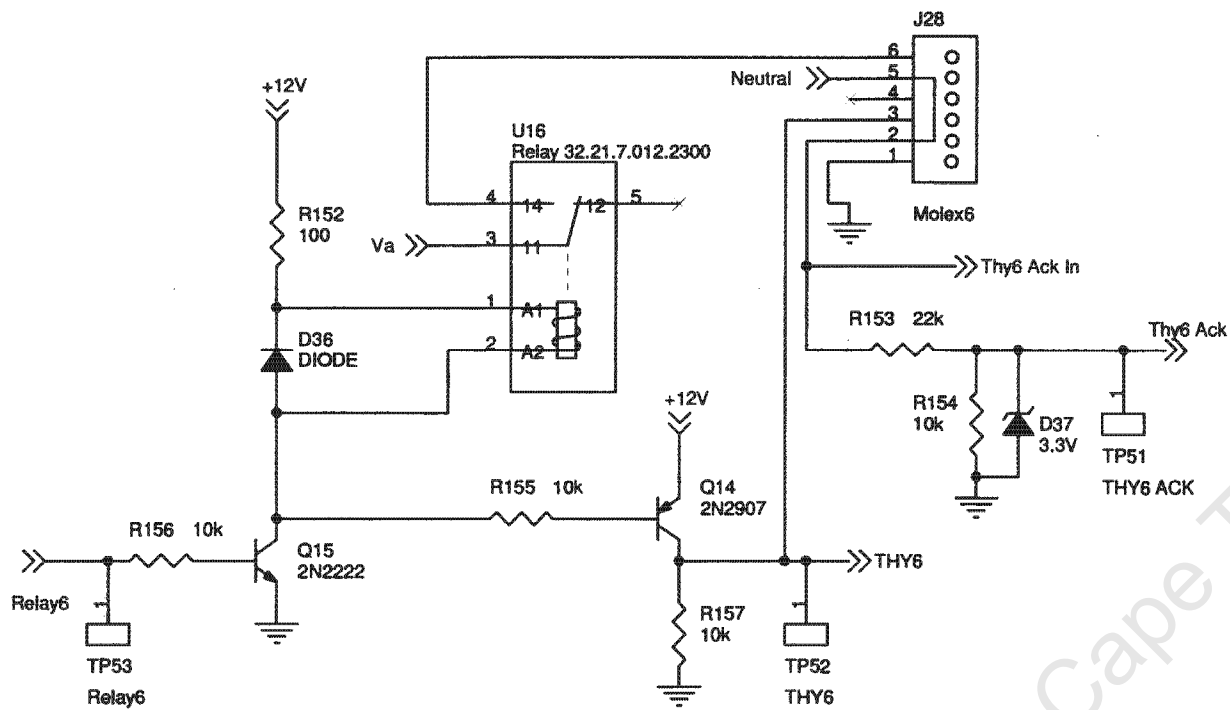
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Date:	Monday, November 05, 2007	Sheet 11 of 21



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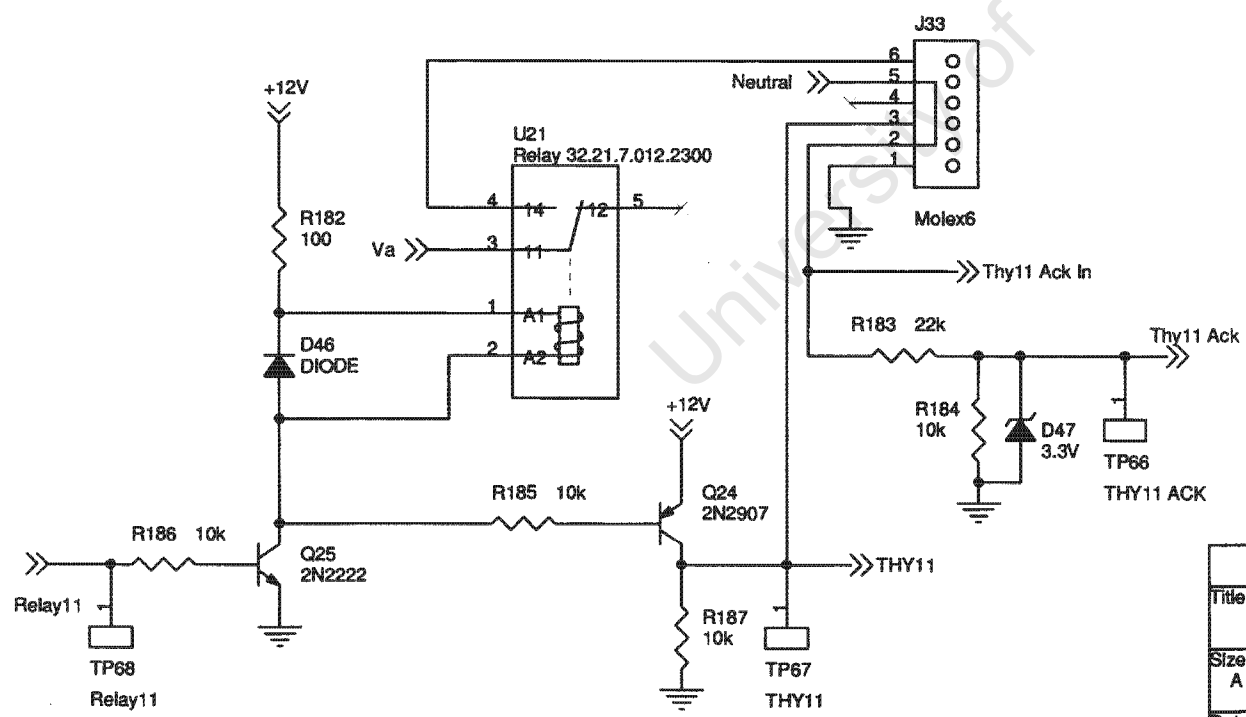
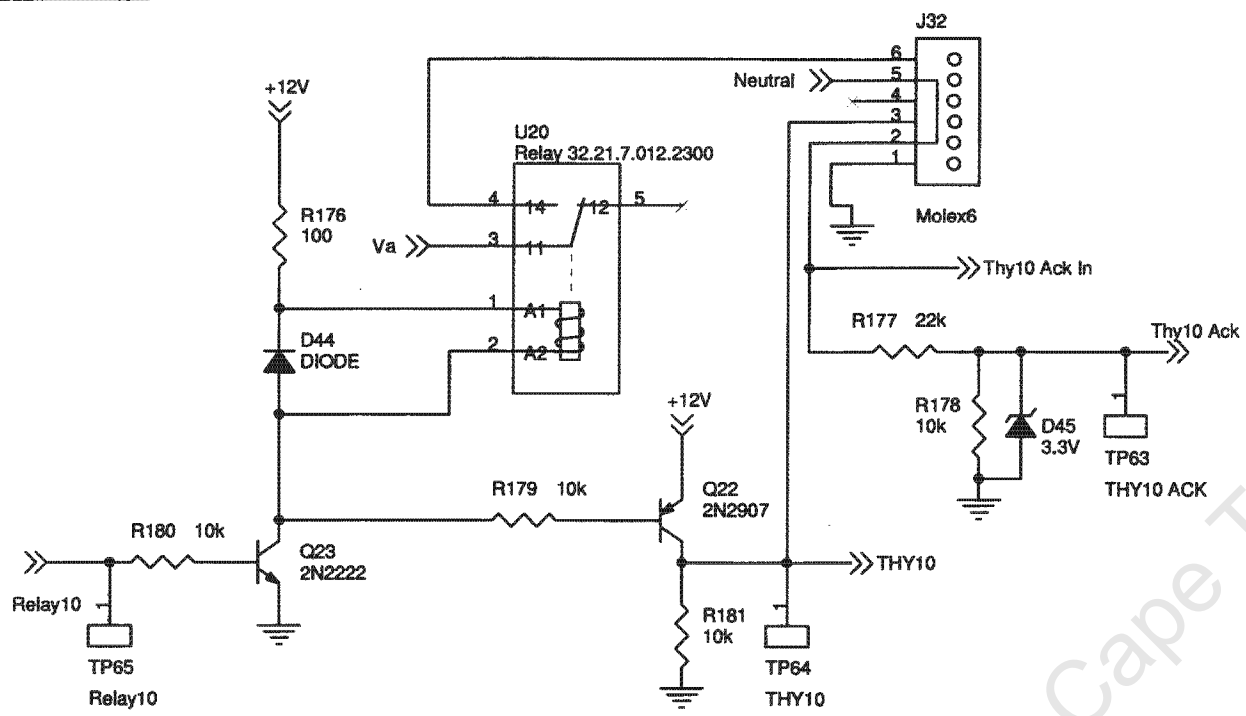


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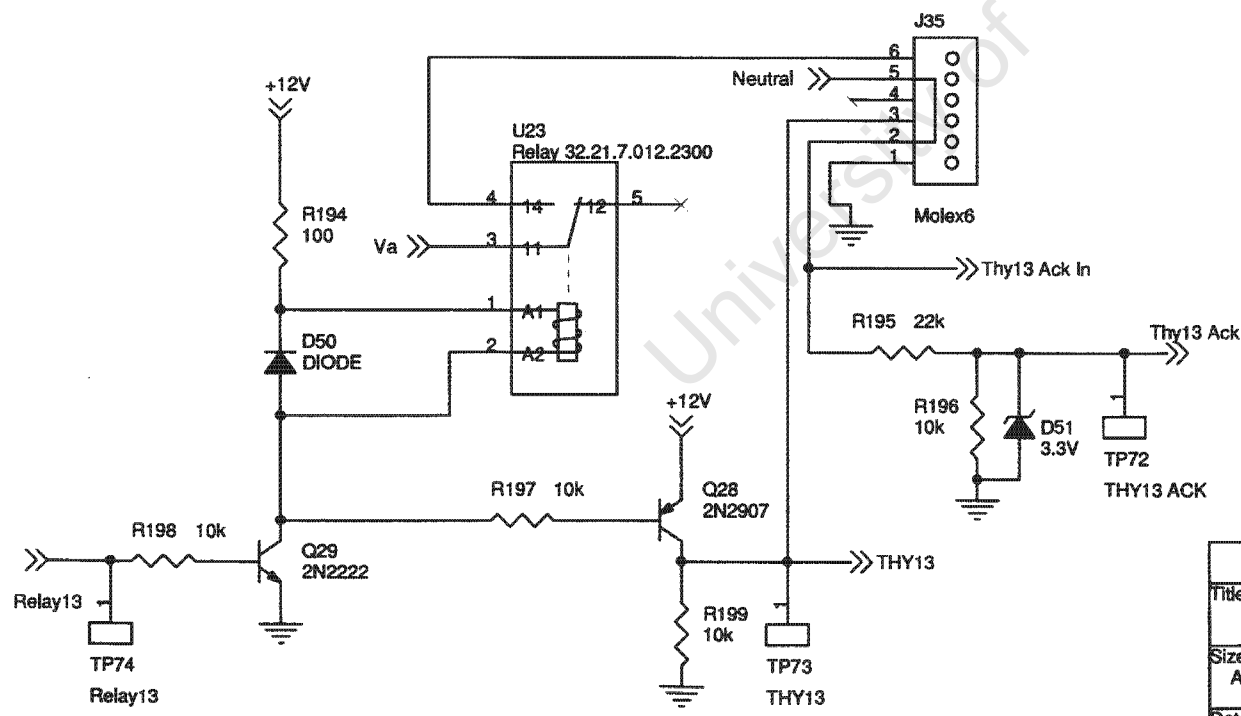
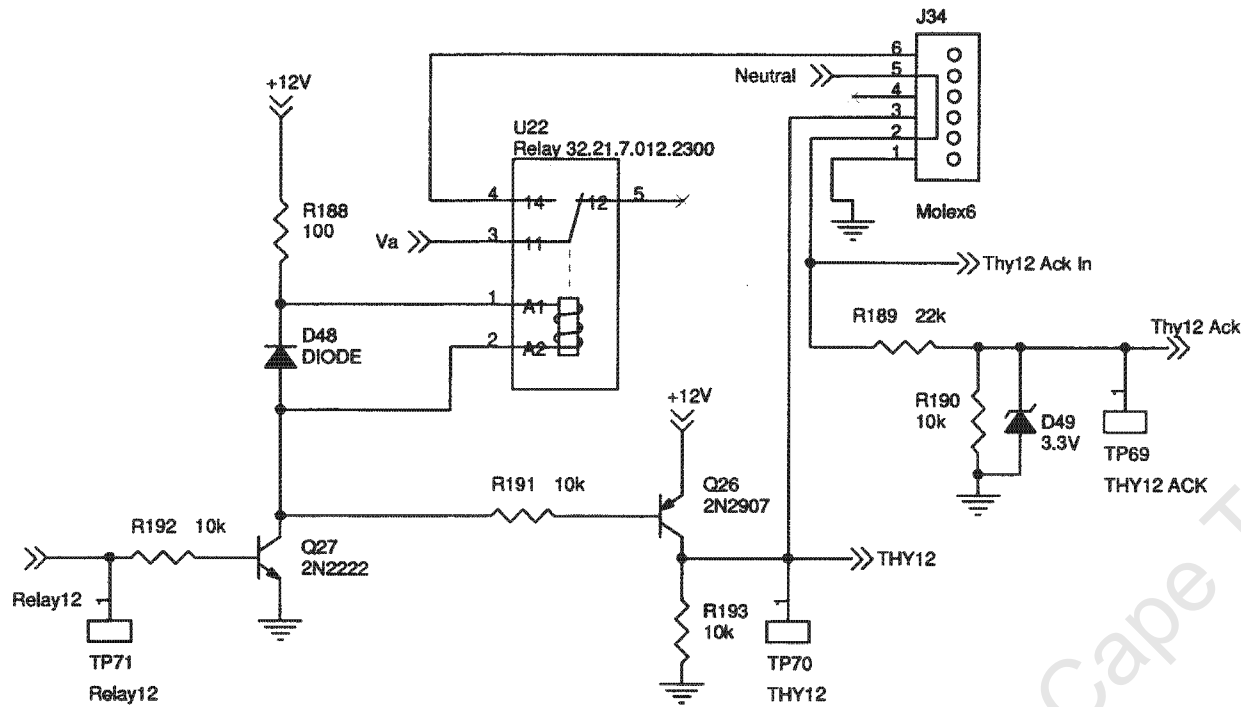


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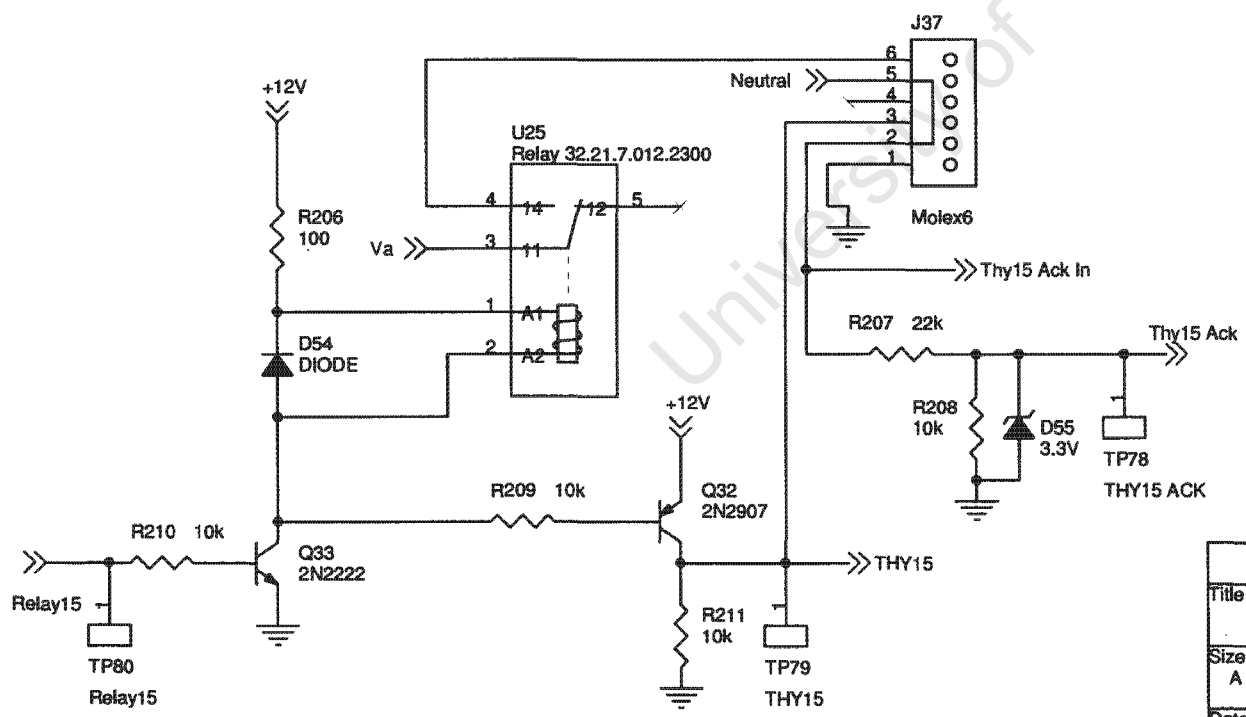
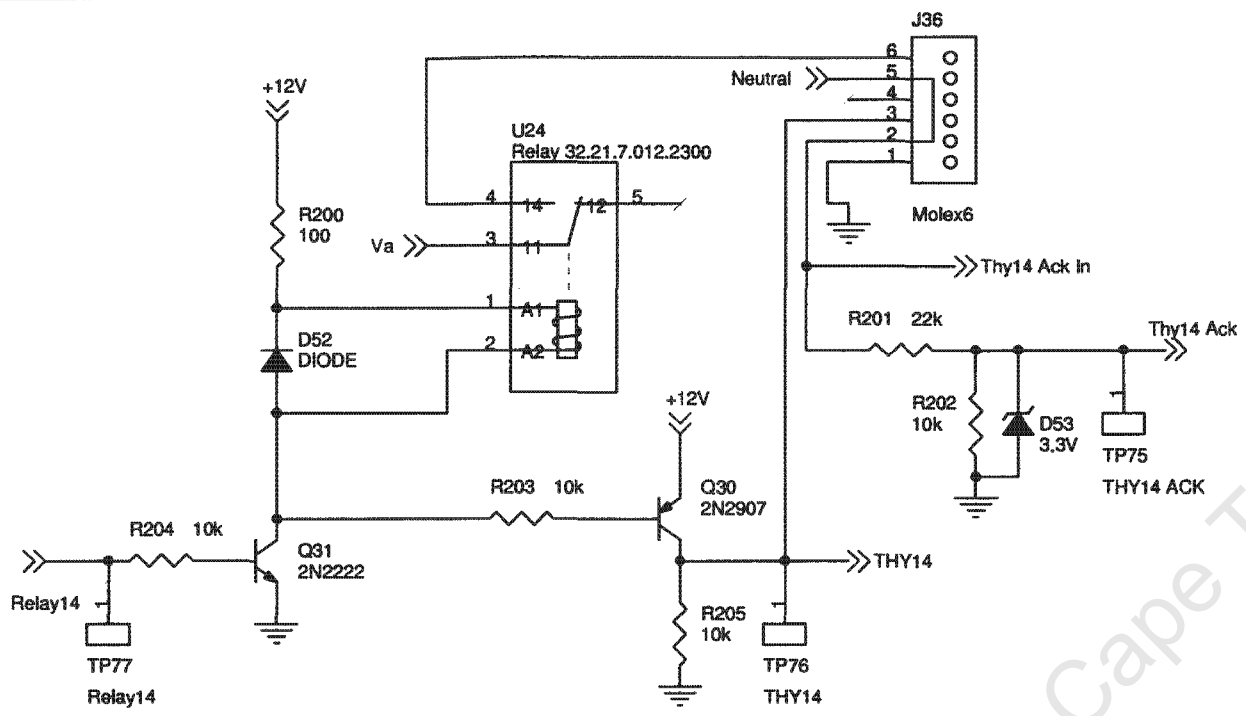




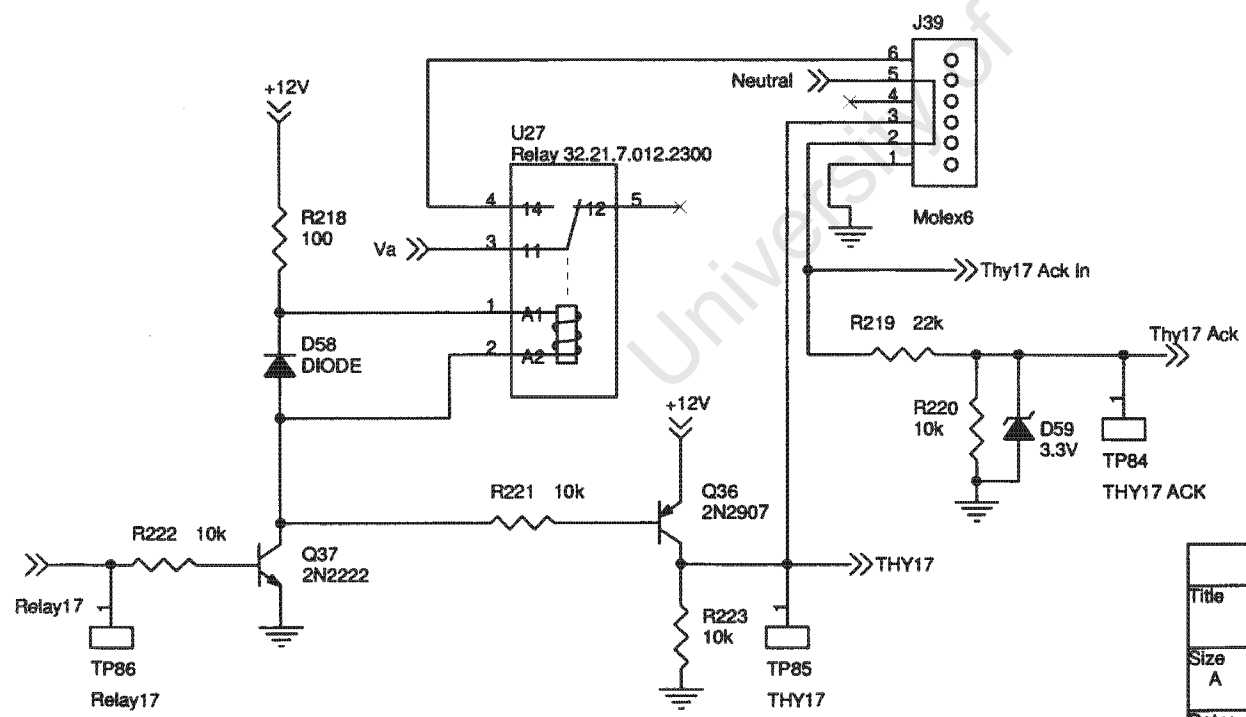
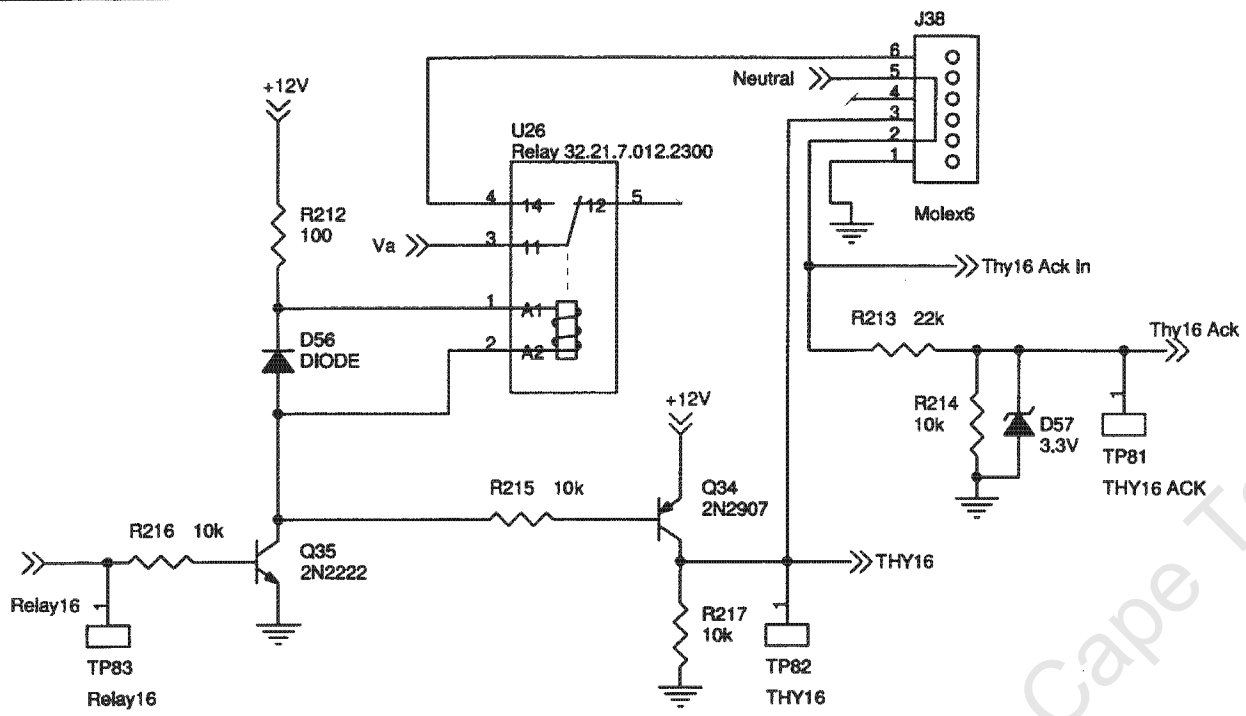
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Date:	Monday, November 05, 2007	Sheet 16 of 21



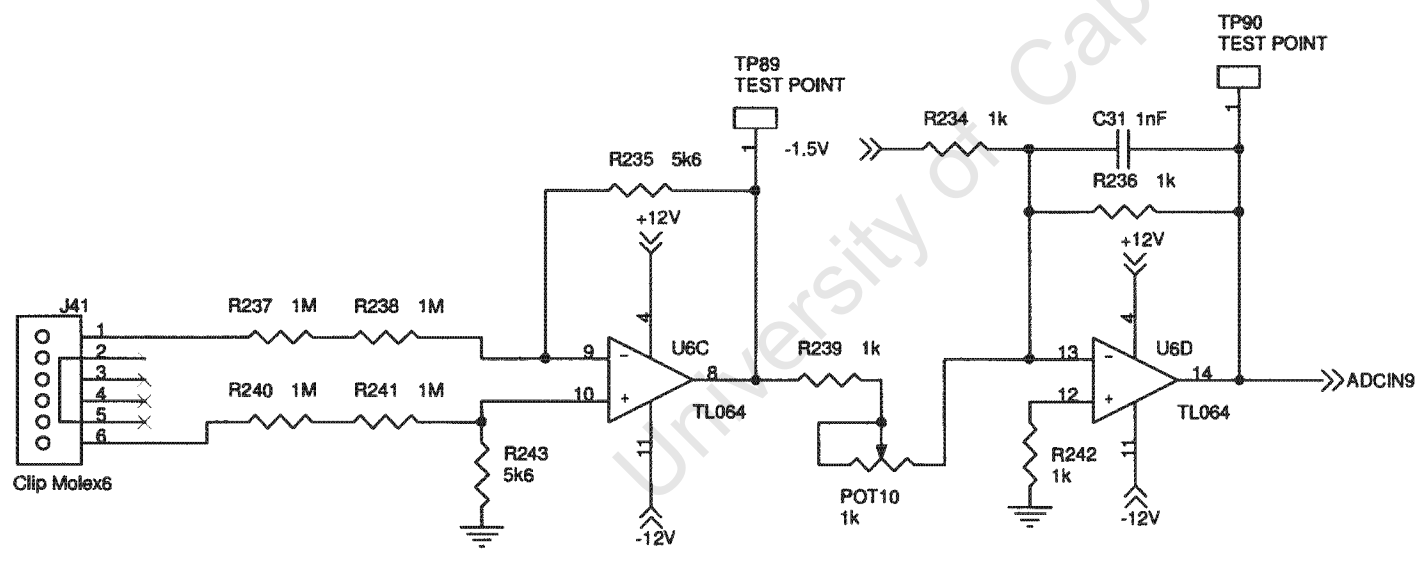
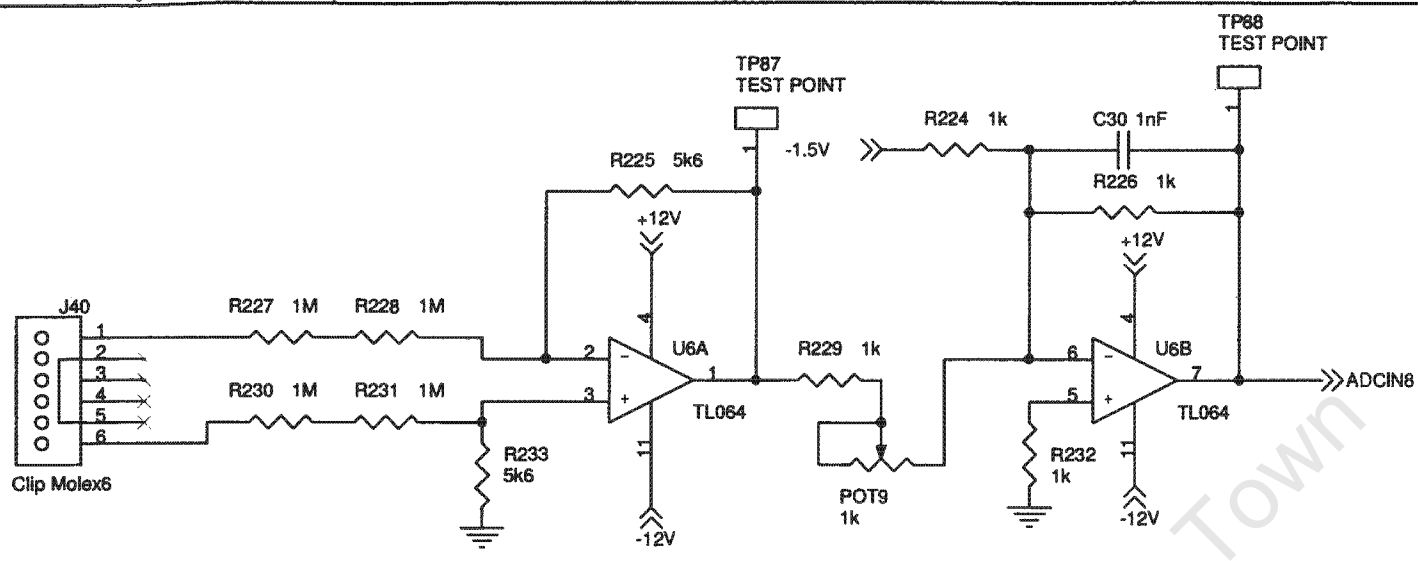
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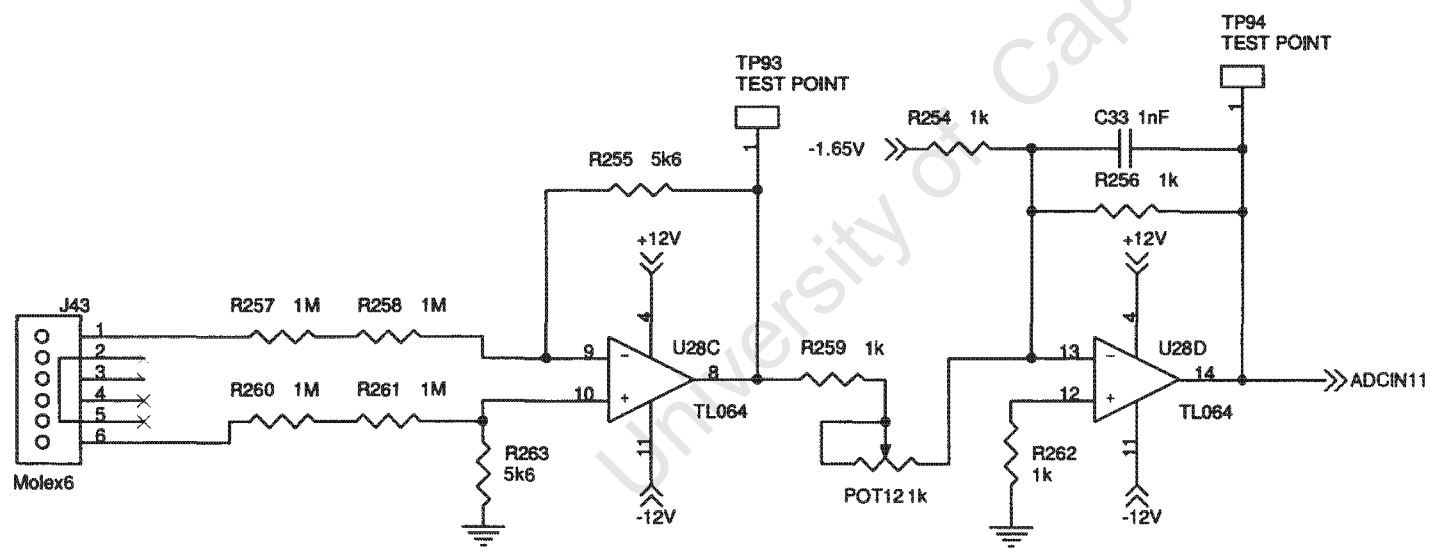
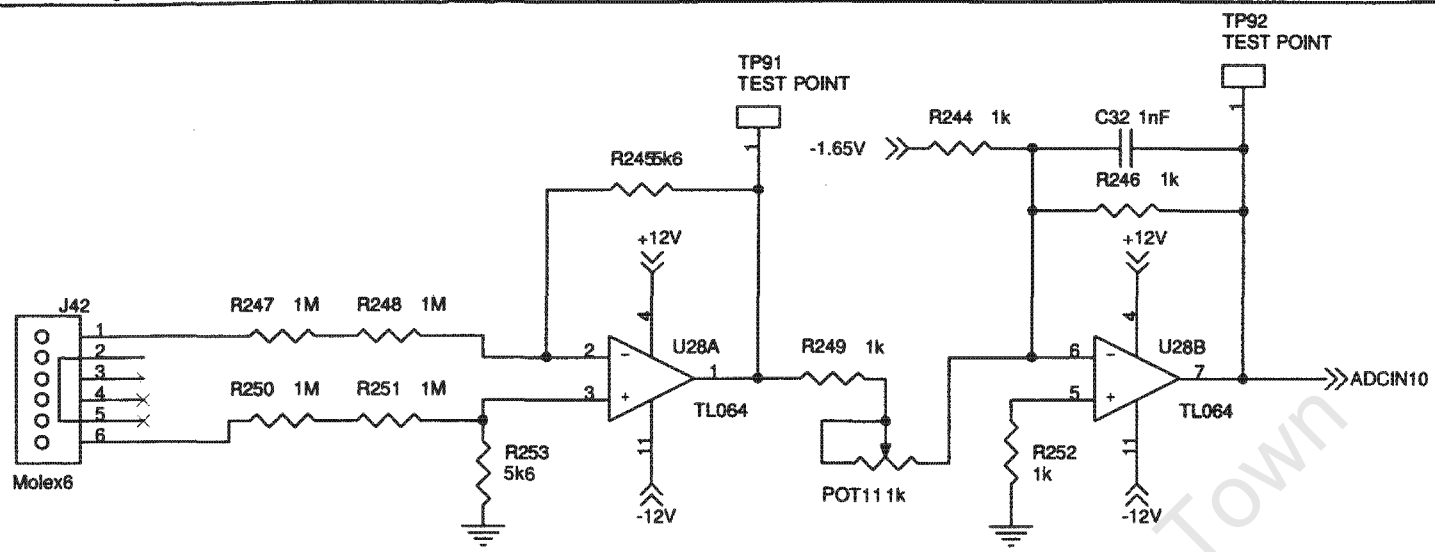
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Date:	Monday, November 05, 2007	Sheet 19 of 21



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A	ACAL-02	-
Date:	Monday, November 05, 2007	Sheet 20 of 21



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Voltage Measurements 3&4		
Size	Document Number	Rev
A	ACAL-02	-
Date:	Monday, November 05, 2007	Sheet 21 of 21

**Appendix F**  
**Set-point and Data-point Descriptions**

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Number	Chr	Hex	QID SP Number	Type	Microcontroller Tag	Description	Min Value	Default Value to DSP	Range	Units	Scaling
SP0	0	0x00	SP0	System Variables	System	System	0	0	0 to 255	SP	1
SP1	1	0x01	SP1		System	System	1	1	0 to 255	SP	1
SP2	2	0x02	SP2		System	System	2	2	0 to 255	SP	1
SP3	3	0x03	SP3		System	System	3	3	0 to 255	SP	1
SP4	4	0x04	SP4		System	System	4	4	0 to 255	SP	1
SP5	5	0x05	SP5		System	System	5	5	0 to 255	SP	1
SP6	6	0x06	SP6		System	System	6	6	0 to 255	SP	1
SP7	7	0x07	SP7		System	System	7	7	0 to 255	SP	1
SP8	8	0x08	SP8		System	System	8	8	0 to 255	SP	1
SP9	9	0x09	SP9		System	System	9	9	0 to 255	SP	1
SP10	10	0x0A	SP10		System	System	10	10	0 to 255	SP	1
SP11	11	0x0B	SP11		System	System	11	11	0 to 255	SP	1
SP12	12	0x0C	SP12		System	System	12	12	0 to 255	SP	1
SP13	13	0x0D	SP13		System	System	13	13	0 to 255	SP	1
SP14	14	0x0E	SP14		System	System	14	14	0 to 255	SP	1
SP15	15	0x0F	SP15		System	System	15	15	0 to 255	SP	1
SP16	16	0x10	SP16		System	System	16	16	0 to 255	SP	1
SP17	17	0x11	SP17		System	System	17	17	0 to 255	SP	1
SP18	18	0x12	SP18		System	System	18	18	0 to 255	SP	1
SP19	19	0x13	SP19		System	System	19	19	0 to 255	SP	1
SP20	20	0x14	SP20		System	System	20	20	0 to 255	SP	1
SP21	21	0x15	SP21		System	System	21	21	0 to 255	SP	1
SP22	22	0x16	SP22		System	System	22	22	0 to 255	SP	1
SP23	23	0x17	SP23		System	System	23	23	0 to 255	SP	1
SP24	24	0x18	SP24		System	System	24	24	0 to 255	SP	1
SP25	25	0x19	SP25		System	System	25	25	0 to 255	SP	1
SP26	26	0x1A	SP26		System	System	26	26	0 to 255	SP	1
SP27	27	0x1B	SP27		System	System	27	27	0 to 255	SP	1
SP28	28	0x1C	SP28		System	System	28	28	0 to 255	SP	1
SP29	29	0x1D	SP29		System	System	29	29	0 to 255	SP	1
SP30	30	0x1E	SP30	System	System	30	30	0 to 255	SP	1	
SP31	31	0x1F	SP31	System	System	31	31	0 to 255	SP	1	
SP32	32	0x20	SP32	System	System	32	32	0 to 255	SP	1	
SP33	33	0x21	SP33	System	System	33	33	0 to 255	SP	1	
SP34	34	0x22	SP34	System	System	34	34	0 to 255	SP	1	
SP35	35	0x23	SP35	System	System	35	35	0 to 255	SP	1	
SP36	36	0x24	SP36	System	System	36	36	0 to 255	SP	1	
SP37	37	0x25	SP37	System	System	37	37	0 to 255	SP	1	
SP38	38	0x26	SP38	System	System	38	38	0 to 255	SP	1	
SP39	39	0x27	SP39	System	System	39	39	0 to 255	SP	1	
SP40	40	0x28	SP40	System	System	40	40	0 to 255	SP	1	
SP41	41	0x29	SP41	System	System	41	41	0 to 255	SP	1	
SP42	42	0x2A	SP42	System	System	42	42	0 to 255	SP	1	
SP43	43	0x2B	SP43	System	System	43	43	0 to 255	SP	1	
SP44	44	0x2C	SP44	System	System	44	44	0 to 255	SP	1	
SP45	45	0x2D	SP45	System	System	45	45	0 to 255	SP	1	
SP46	46	0x2E	SP46	System	System	46	46	0 to 255	SP	1	
SP47	47	0x2F	SP47	System	System	47	47	0 to 255	SP	1	
SP48	48	0x30	SP48	System	System	48	48	0 to 255	SP	1	
SP49	49	0x31	SP49	System	System	49	49	0 to 255	SP	1	
SP50	50	0x32	SP50	System	System	50	50	0 to 255	SP	1	
SP51	51	0x33	SP51	System	System	51	51	0 to 255	SP	1	
SP52	52	0x34	SP52	System	System	52	52	0 to 255	SP	1	
SP53	53	0x35	SP53	System	System	53	53	0 to 255	SP	1	
SP54	54	0x36	SP54	System	System	54	54	0 to 255	SP	1	
SP55	55	0x37	SP55	System	System	55	55	0 to 255	SP	1	
SP56	56	0x38	SP56	System	System	56	56	0 to 255	SP	1	
SP57	57	0x39	SP57	System	System	57	57	0 to 255	SP	1	
SP58	58	0x3A	SP58	System	System	58	58	0 to 255	SP	1	
SP59	59	0x3B	SP59	System	System	59	59	0 to 255	SP	1	
SP60	60	0x3C	SP60	System	System	60	60	0 to 255	SP	1	
SP61	61	0x3D	SP61	System	System	61	61	0 to 255	SP	1	
SP62	62	0x3E	SP62	System	System	62	62	0 to 255	SP	1	
SP63	63	0x3F	SP63	System	System	63	63	0 to 255	SP	1	
SP64	64	0x40	SP64	System	System	64	64	0 to 255	SP	1	
SP65	65	0x41	SP65	System	System	65	65	0 to 255	SP	1	
SP66	66	0x42	SP66	System	System	66	66	0 to 255	SP	1	
SP67	67	0x43	SP67	System	System	67	67	0 to 255	SP	1	
SP68	68	0x44	SP68	System	System	68	68	0 to 255	SP	1	
SP69	69	0x45	SP69	System	System	69	69	0 to 255	SP	1	
SP70	70	0x46	SP70	System	System	70	70	0 to 255	SP	1	
SP71	71	0x47	SP71	System	System	71	71	0 to 255	SP	1	
SP72	72	0x48	SP72	System	System	72	72	0 to 255	SP	1	
SP73	73	0x49	SP73	System	System	73	73	0 to 255	SP	1	
SP74	74	0x4A	SP74	System	System	74	74	0 to 255	SP	1	
SP75	75	0x4B	SP75	System	System	75	75	0 to 255	SP	1	
SP76	76	0x4C	SP76	System	System	76	76	0 to 255	SP	1	
SP77	77	0x4D	SP77	System	System	77	77	0 to 255	SP	1	
SP78	78	0x4E	SP78	System	System	78	78	0 to 255	SP	1	
SP79	79	0x4F	SP79	System	System	79	79	0 to 255	SP	1	
SP80	80	0x50	SP80	System	System	80	80	0 to 255	SP	1	
SP81	81	0x51	SP81	System	System	81	81	0 to 255	SP	1	
SP82	82	0x52	SP82	System	System	82	82	0 to 255	SP	1	
SP83	83	0x53	SP83	System	System	83	83	0 to 255	SP	1	
SP84	84	0x54	SP84	System	System	84	84	0 to 255	SP	1	
SP85	85	0x55	SP85	System	System	85	85	0 to 255	SP	1	
SP86	86	0x56	SP86	System	System	86	86	0 to 255	SP	1	
SP87	87	0x57	SP87	System	System	87	87	0 to 255	SP	1	
SP88	88	0x58	SP88	System	System	88	88	0 to 255	SP	1	
SP89	89	0x59	SP89	System	System	89	89	0 to 255	SP	1	
SP90	90	0x5A	SP90	System	System	90	90	0 to 255	SP	1	
SP91	91	0x5B	SP91	System	System	91	91	0 to 255	SP	1	
SP92	92	0x5C	SP92	System	System	92	92	0 to 255	SP	1	
SP93	93	0x5D	SP93	System	System	93	93	0 to 255	SP	1	
SP94	94	0x5E	SP94	System	System	94	94	0 to 255	SP	1	
SP95	95	0x5F	SP95	System	System	95	95	0 to 255	SP	1	
SP96	96	0x60	SP96	System	System	96	96	0 to 255	SP	1	
SP97	97	0x61	SP97	System	System	97	97	0 to 255	SP	1	
SP98	98	0x62	SP98	System	System	98	98	0 to 255	SP	1	
SP99	99	0x63	SP99	System	System	99	99	0 to 255	SP	1	
SP100	100	0x64	SP100	System	System	100	100	0 to 255	SP	1	
SP101	101	0x65	SP101	System	System	101	101	0 to 255	SP	1	
SP102	102	0x66	SP102	System	System	102	102	0 to 255	SP	1	
SP103	103	0x67	SP103	System	System	103	103	0 to 255	SP	1	
SP104	104	0x68	SP104	System	System	104	104	0 to 255	SP	1	
SP105	105	0x69	SP105	System	System	105	105	0 to 255	SP	1	
SP106	106	0x6A	SP106	System	System	106	106	0 to 255	SP	1	
SP107	107	0x6B	SP107	System	System	107	107	0 to 255	SP	1	
SP108	108	0x6C	SP108	System	System	108	108	0 to 255	SP	1	
SP109	109	0x6D	SP109	System	System	109	109	0 to 255	SP	1	
SP110	110	0x6E	SP110	System	System	110	110	0 to 255	SP	1	
SP111	111	0x6F	SP111	System	System	111	111	0 to 255	SP	1	
SP112	112	0x70	SP112	System	System	112	112	0 to 255	SP	1	
SP113	113	0x71	SP113	System	System	113	113	0 to 255	SP	1	
SP114	114	0x72	SP114	System	System	114	114	0 to 255	SP	1	
SP115	115	0x73	SP115	System	System	115	115	0 to 255	SP	1	
SP116	116	0x74	SP116	System	System	116	116	0 to 255	SP	1	
SP117	117	0x75	SP117	System	System	117	117	0 to 255	SP	1	
SP118	118	0x76	SP118	System	System	118	118	0 to 255	SP	1	
SP119	119	0x77	SP119	System	System	119	119	0 to 255	SP	1	
SP120	120	0x78	SP120	System	System	120	120	0 to 255	SP	1	
SP121	121	0x79	SP121	System	System	121	121	0 to 255	SP	1	
SP122	122	0x7A	SP122	System	System	122	122	0 to 255	SP	1	
SP123	123	0x7B	SP123	System	System	123	123	0 to 255	SP	1	
SP124	124	0x7C	SP124	System	System	124	124	0 to 255	SP	1	
SP125	125	0x7D	SP125	System	System	125	125	0 to 255	SP	1	
SP126	126	0x7E	SP126	System	System	126	126	0 to 255	SP	1	
SP127	127	0x7F	SP127	System	System	127	127	0 to 255	SP	1	
SP128	128	0x80	SP128	System	System	128	128	0 to 255	SP	1	
SP129	129	0x81	SP129	System	System	129	129	0 to 255	SP	1	
SP130	130	0x82	SP130	System	System	130	130	0 to 255	SP	1	
SP131	131	0x83	SP131	System	System	131	131	0 to 255	SP	1	
SP132	132	0x84	SP132	System	System	132	132	0 to 255	SP	1	
SP133	133	0x85	SP133	System	System	133	133	0 to 255	SP	1	
SP134	134	0x86	SP134	System	System	134	134	0 to 255	SP	1	
SP135	135	0x87	SP135	System	System	135	135	0 to 255	SP	1	
SP136	136	0x88	SP136	System	System	136	136	0 to 255	SP	1	
SP137	137	0x89	SP137	System	System	137	137	0 to 255	SP	1	
SP138	138	0x8A	SP138	System	System	138	138	0 to 255	SP	1	
SP139	139	0x8B	SP139	System	System	139	139</				

Symbol	Enc.	Pos.	Out of Range	Type	Microcontroller Eq.	Default Value	Default Value in CDP	F-Code	Letter	Setting
L2P	6	000		Char	Char	0	0	0-00000		
L2S	7	001		Char	Char	0	0	0-00000		
L2C	8	002		Char	Char	0	0	0-00000		
L2E	9	003		Char	Char	0	0	0-00000		
L2F	10	004		Char	Char	0	0	0-00000		
L2G	11	005		Char	Char	0	0	0-00000		
L2H	12	006		Char	Char	0	0	0-00000		
L2I	13	007		Char	Char	0	0	0-00000		
L2J	14	008		Char	Char	0	0	0-00000		
L2K	15	009		Char	Char	0	0	0-00000		
L2L	16	010		Char	Char	0	0	0-00000		
L2M	17	011		Char	Char	0	0	0-00000		
L2N	18	012		Char	Char	0	0	0-00000		
L2O	19	013		Char	Char	0	0	0-00000		
L2P	20	014		Char	Char	0	0	0-00000		
L2Q	21	015		Char	Char	0	0	0-00000		
L2R	22	016		Char	Char	0	0	0-00000		
L2S	23	017		Char	Char	0	0	0-00000		
L2T	24	018		Char	Char	0	0	0-00000		
L2U	25	019		Char	Char	0	0	0-00000		
L2V	26	020		Char	Char	0	0	0-00000		
L2W	27	021		Char	Char	0	0	0-00000		
L2X	28	022		Char	Char	0	0	0-00000		
L2Y	29	023		Char	Char	0	0	0-00000		
L2Z	30	024		Char	Char	0	0	0-00000		
L2A	31	025		Char	Char	0	0	0-00000		
L2B	32	026		Char	Char	0	0	0-00000		
L2C	33	027		Char	Char	0	0	0-00000		
L2D	34	028		Char	Char	0	0	0-00000		
L2E	35	029		Char	Char	0	0	0-00000		
L2F	36	030		Char	Char	0	0	0-00000		
L2G	37	031		Char	Char	0	0	0-00000		
L2H	38	032		Char	Char	0	0	0-00000		
L2I	39	033		Char	Char	0	0	0-00000		
L2J	40	034		Char	Char	0	0	0-00000		
L2K	41	035		Char	Char	0	0	0-00000		
L2L	42	036		Char	Char	0	0	0-00000		
L2M	43	037		Char	Char	0	0	0-00000		
L2N	44	038		Char	Char	0	0	0-00000		
L2O	45	039		Char	Char	0	0	0-00000		
L2P	46	040		Char	Char	0	0	0-00000		
L2Q	47	041		Char	Char	0	0	0-00000		
L2R	48	042		Char	Char	0	0	0-00000		
L2S	49	043		Char	Char	0	0	0-00000		
L2T	50	044		Char	Char	0	0	0-00000		
L2U	51	045		Char	Char	0	0	0-00000		
L2V	52	046		Char	Char	0	0	0-00000		
L2W	53	047		Char	Char	0	0	0-00000		
L2X	54	048		Char	Char	0	0	0-00000		
L2Y	55	049		Char	Char	0	0	0-00000		
L2Z	56	050		Char	Char	0	0	0-00000		
L2A	57	051		Char	Char	0	0	0-00000		
L2B	58	052		Char	Char	0	0	0-00000		
L2C	59	053		Char	Char	0	0	0-00000		
L2D	60	054		Char	Char	0	0	0-00000		
L2E	61	055		Char	Char	0	0	0-00000		
L2F	62	056		Char	Char	0	0	0-00000		
L2G	63	057		Char	Char	0	0	0-00000		
L2H	64	058		Char	Char	0	0	0-00000		
L2I	65	059		Char	Char	0	0	0-00000		
L2J	66	060		Char	Char	0	0	0-00000		
L2K	67	061		Char	Char	0	0	0-00000		
L2L	68	062		Char	Char	0	0	0-00000		
L2M	69	063		Char	Char	0	0	0-00000		
L2N	70	064		Char	Char	0	0	0-00000		
L2O	71	065		Char	Char	0	0	0-00000		
L2P	72	066		Char	Char	0	0	0-00000		
L2Q	73	067		Char	Char	0	0	0-00000		
L2R	74	068		Char	Char	0	0	0-00000		
L2S	75	069		Char	Char	0	0	0-00000		
L2T	76	070		Char	Char	0	0	0-00000		
L2U	77	071		Char	Char	0	0	0-00000		
L2V	78	072		Char	Char	0	0	0-00000		
L2W	79	073		Char	Char	0	0	0-00000		
L2X	80	074		Char	Char	0	0	0-00000		
L2Y	81	075		Char	Char	0	0	0-00000		
L2Z	82	076		Char	Char	0	0	0-00000		
L2A	83	077		Char	Char	0	0	0-00000		
L2B	84	078		Char	Char	0	0	0-00000		
L2C	85	079		Char	Char	0	0	0-00000		
L2D	86	080		Char	Char	0	0	0-00000		
L2E	87	081		Char	Char	0	0	0-00000		
L2F	88	082		Char	Char	0	0	0-00000		
L2G	89	083		Char	Char	0	0	0-00000		
L2H	90	084		Char	Char	0	0	0-00000		
L2I	91	085		Char	Char	0	0	0-00000		
L2J	92	086		Char	Char	0	0	0-00000		
L2K	93	087		Char	Char	0	0	0-00000		
L2L	94	088		Char	Char	0	0	0-00000		
L2M	95	089		Char	Char	0	0	0-00000		
L2N	96	090		Char	Char	0	0	0-00000		
L2O	97	091		Char	Char	0	0	0-00000		
L2P	98	092		Char	Char	0	0	0-00000		
L2Q	99	093		Char	Char	0	0	0-00000		
L2R	100	094		Char	Char	0	0	0-00000		
L2S	101	095		Char	Char	0	0	0-00000		
L2T	102	096		Char	Char	0	0	0-00000		
L2U	103	097		Char	Char	0	0	0-00000		
L2V	104	098		Char	Char	0	0	0-00000		
L2W	105	099		Char	Char	0	0	0-00000		
L2X	106	100		Char	Char	0	0	0-00000		
L2Y	107	101		Char	Char	0	0	0-00000		
L2Z	108	102		Char	Char	0	0	0-00000		
L2A	109	103		Char	Char	0	0	0-00000		
L2B	110	104		Char	Char	0	0	0-00000		
L2C	111	105		Char	Char	0	0	0-00000		
L2D	112	106		Char	Char	0	0	0-00000		
L2E	113	107		Char	Char	0	0	0-00000		
L2F	114	108		Char	Char	0	0	0-00000		
L2G	115	109		Char	Char	0	0	0-00000		
L2H	116	110		Char	Char	0	0	0-00000		
L2I	117	111		Char	Char	0	0	0-00000		
L2J	118	112		Char	Char	0	0	0-00000		
L2K	119	113		Char	Char	0	0	0-00000		
L2L	120	114		Char	Char	0	0	0-00000		
L2M	121	115		Char	Char	0	0	0-00000		
L2N	122	116		Char	Char	0	0	0-00000		
L2O	123	117		Char	Char	0	0	0-00000		
L2P	124	118		Char	Char	0	0	0-00000		
L2Q	125	119		Char	Char	0	0	0-00000		
L2R	126	120		Char	Char	0	0	0-00000		
L2S	127	121		Char	Char	0	0	0-00000		
L2T	128	122		Char	Char	0	0	0-00000		
L2U	129	123		Char	Char	0	0	0-00000		
L2V	130	124		Char	Char	0	0	0-00000		
L2W	131	125		Char	Char	0	0	0-00000		
L2X	132	126		Char	Char	0	0	0-00000		
L2Y	133	127		Char	Char	0	0	0-00000		
L2Z	134	128		Char	Char	0	0	0-00000		
L2A	135	129		Char	Char	0	0	0-00000		
L2B	136	130		Char	Char	0	0	0-00000		
L2C	137	131		Char	Char	0	0	0-00000		
L2D	138	132		Char	Char	0	0	0-00000		
L2E	139	133		Char	Char	0	0	0-00000		
L2F	140	134		Char	Char	0	0	0-00000		
L2G	141	135		Char	Char	0	0	0-00000		
L2H	142	136		Char	Char	0	0	0-00000		
L2I	143	137		Char	Char	0	0	0-00000		
L2J	144	138		Char	Char	0	0	0-00000		
L2K	145	139		Char	Char	0	0	0-00000		
L2L	146	140		Char	Char	0	0	0-00000		
L2M	147	141		Char	Char	0	0	0-00000		
L2N	148	142		Char	Char	0	0	0-00000		
L2O	149	143		Char	Char	0	0	0-00000		
L2P	150	144		Char	Char	0	0	0-00000		
L2Q	151	145		Char	Char	0	0	0-00000		
L2R	152	146		Char	Char	0	0	0-00000		
L2S	153	147		Char	Char	0	0	0-00000		
L2T	154	148		Char	Char	0	0	0-00000		
L2U	155	149		Char	Char	0	0	0-00000		
L2V	156	150		Char	Char	0	0	0-00000		
L2W	157	151		Char	Char	0	0	0-00000		
L2X	158	152		Char	Char	0	0	0-00000		
L2Y	159	153		Char	Char	0	0	0-00000		
L2Z	160	154		Char	Char	0	0	0-00000		
L2A	161	155		Char	Char	0	0	0-00000		
L2B	162	156		Char	Char	0	0	0-00000		
L2C	163	157		Char	Char	0	0	0-00000		
L2D	164	158		Char	Char	0	0	0-00000		
L2E	165	159		Char	Char	0	0	0-00000		
L2F	166	160		Char	Char	0	0	0-00000		
L2G	167									



**Appendix G**  
**Bill of Materials and Costing**

University of Cape Town

## University of Cape Town - Current Balancer/Power Factor Correction Hybrid System

Component Designation	Units/Meter	Description	Manufacturer	Supplier	Supplier Stock Code	Price per Unit	Total Price	
CAB1	1	Standard Power Factor Correction Unit	Alpes	Electromechanica	41100	R 83,970.00	R 83,970.00	
BANKS	1	Additional Capacitor Bank, 100 kVAR	Alpes	Electromechanica	42100	R 9,250.00	R 9,250.00	
Relay6-B	3	Contactors, BF25k	Levato	Electromechanica	BF25k	R 540.00	R 1,620.00	
Relay9-17	9	Contactors, BF20k	Levato	Electromechanica	BF20k	R 441.00	R 3,969.00	
CT1-8	8	Current Transformers	Electro	Electromechanica	IBR1/08	R 145.00	R 1,168.00	
EMSTOP1	1	Latched Mushroom Head Emergency Stop Button		Mantech	61903	R 40.00	R 40.00	
PSU1	1	Switch Mode Power Supply	ASTECC	Mantech	LPT45	R 250.00	R 250.00	
DISP1	1	Intelligent LCD Module	PowerTip	Communica	PC1602L	R 80.00	R 80.00	
KEY1	1	MLT Drive Keypad	MLT Drives CC.	MLT Drives CC.	-	R 100.00	R 100.00	
ACAL-09	1	MLT Drives DSP Card	MLT Drives CC.	MLT Drives CC.	-	R 9,500.00	R 9,500.00	
ACAL-02	1	Multi-Interface Card	MLT Drives CC.	MLT Drives CC.	-	R 800.00	R 800.00	
SW1	1	CB DSP Software						
SW2	1	CD M/C Software						
	4	25 mm <sup>2</sup> Cable				R 28.00	R 112.00	
	8	6 mm <sup>2</sup> Cable				R 7.38	R 59.04	
	8	2.5 mm <sup>2</sup> Cable				R 3.66	R 29.28	
	45	1.5 mm <sup>2</sup> Cable				R 2.28	R 102.60	
	26	DIN Rail Connector Blocks	Weland	Electromechanica	WK5/J	R 8.40	R 218.40	
	4	DIN Rail End Stops	Weland	Electromechanica	9708/S35	R 2.90	R 11.60	
	4	DIN Rail End Plates	Weland	Electromechanica	AP6	R 2.30	R 9.20	
	1	DIN Rail	Weland	Electromechanica	DR35A	R 26.00	R 26.00	
	50	Cable Ties	Heliermann Tyton	Electromechanica	T30R		R 20.00	
	1	Cable Trunking, 25 x 30mm	LucaSystem	Electromechanica	55143		R 22.00	
	1	Cable Trunking, 40 x 40mm	LucaSystem	Electromechanica	55155		R 33.00	
	85	Ring Lugs, 10 - 8mm	Jeeson	Electromechanica	ANE 3-M8		R 100.00	
	20	Ring Lugs, 15 - 10mm	Jeeson	Electromechanica	ANE 5-M10		R 46.00	
	6	Ferrules, 6mm diameter	Jeeson	Electromechanica	NC50000		R 3.00	
	0.5	Spiral Wrap, 10mm		Electromechanica			R 5.00	
	0.5	Spiral Wrap, 25mm		Electromechanica			R 5.00	
<b>Total System Cost:</b>								<b>R 91,549.12</b>

## Appendix H Harmonic Impact on Unbalance Calculation Algorithm

To be able to determine the impact of harmonic content on the result returned by the unbalance calculation, the unbalance algorithm was entered into a computer simulation package, MATLAB, such that all variables could be monitored and manipulated (see the full MATLAB code of the end of this appendix). The algorithm, as shown in the main body of this thesis document, uses the equation below to calculate the orthogonal components of both the positive and negative sequence currents.

$$I_{\alpha}^{+} = I_{\alpha} - I_{\beta} \left( t - \frac{T}{4} \right)$$

$$I_{\beta}^{+} = I_{\alpha} \left( t - \frac{T}{4} \right) + I_{\beta}$$

$$I_{\alpha}^{-} = I_{\alpha} + I_{\beta} \left( t - \frac{T}{4} \right)$$

$$I_{\beta}^{-} = -I_{\alpha} \left( t - \frac{T}{4} \right) + I_{\beta}$$

To be able to see the impact of harmonics on the returned result, first the unbalance of an unbalanced harmonic-free system is examined. The fundamental phase current magnitudes listed in the code are indicative of a typical situation seen at the unit's test site.

### Results:

Harmonic Content	Nil	50 A	100 A
Harmonic Order	N/A	3 <sup>rd</sup>	3 <sup>rd</sup>
Phase 'A' Current	1060 A	1060 A	1060 A
Phase 'B' Current	860 A	860 A	860 A
Phase 'C' Current	1300 A	1300 A	1300 A
Returned Unbalance	14.64 %	15.1%	16.32 %

It can thus be said that the addition of harmonic content may cause the results returned by the unbalance calculations to be inflated, yielding an inaccurate unbalance level.

### MATLAB Code:

```

% M-file is written to test the performance of the unbalance calculation
% algorithm under harmonic conditions. Analysis suggests that
% harmonic content significantly influences the result.

t = 0:0.0001:0.2;          % Time Resolution & Duration

Harmonic_Amplitude = 150;    % Harmonic Amplitude
Harmonic_Frequency = 150;    % Harmonic Frequency (50 x n)

a_amplitude = 1060;         % Phase currents with unbalance
b_amplitude = 860;
c_amplitude = 1300;

% Calculating vector of instantaneous current samples
Ia = a_amplitude*sin(100*pi*t + 0) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t + 0);
Ib = b_amplitude*sin(100*pi*t - 2.0944) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t - 2.0944);
Ic = c_amplitude*sin(100*pi*t + 2.0944) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t + 2.0944);

offset = -1.5708;          % Offset to produce exact 90 degree phase shift, as required

% Calculating vector of instantaneous current samples from 90 degrees back
Ia_90 = a_amplitude*sin(100*pi*t + 0 + offset) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t + 0);
Ib_90 = b_amplitude*sin(100*pi*t - 2.0944 + offset) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t - 2.0944);
Ic_90 = c_amplitude*sin(100*pi*t + 2.0944 + offset) + Harmonic_Amplitude*sin(2*pi*Harmonic_Frequency*t + 2.0944);

% Clarke transformation for instantaneous currents
I_alpha = ((Ia) - (Ib/2) - (Ic/2));
I_beta = (((sqrt(3)/2)*Ib) - ((sqrt(3)/2)*Ic));
I_zero = (Ia + Ib + Ic)/3;

% Clarke transformation for shifted instantaneous currents
I_90_alpha = ((Ia_90) - (Ib_90/2) - (Ic_90/2));
I_90_beta = (((sqrt(3)/2)*Ib_90) - ((sqrt(3)/2)*Ic_90));
I_90_zero = (Ia_90 + Ib_90 + Ic_90)/3;

% Calculate orthogonal components of positive sequence
Ipos_alpha = I_alpha - I_90_beta;
Ipos_beta = I_90_alpha + I_beta;
Ipos_mag = sqrt(mean(Ipos_alpha.^2 + Ipos_beta.^2));

```

```

% Calculate orthogonal components of negative sequence
Ineg_alpha = I_alpha + I_90_beta;
Ineg_beta = I_beta - I_90_alpha;
Ineg_mag = sqrt(mean(Ineg_alpha.^2 + Ineg_beta.^2));

I_zero_mag = sqrt(mean(I_zero.^2)); % Calculate magnitude of zero sequence

Unbalance = 100*(I_zero_mag + Ineg_mag)/Ipos_mag % Calculate actual unbalance.

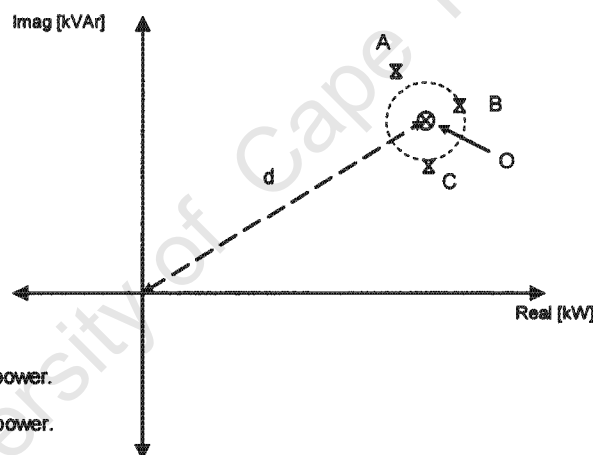
% Plotting Options for Debug/testing purposes:
%plot(t, Ia, 'r', t, Ia_90, 'b')
plot(t, I_alpha, 'r', t, I_beta, 'b', t, I_zero, 'k');
%plot(t, I_90_alpha, 'c', t, I_90_beta, 'm', t, I_90_zero, 'y');
%plot(t, Ipos_alpha, 'r', t, Ipos_beta, 'b', t, Ipos_mag, 'k');
%plot(t, Ineg_alpha, 'r', t, Ineg_beta, 'b', t, Ineg_mag, 'k');
%plot(t, Ipos_mag, 'r', t, Ineg_mag, 'b', t, I_zero_mag, 'k');

```

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## Appendix I Unbalance Calculation using Real and Reactive Power

Because the proper unbalance definition is subject to harmonic interference and because the NEMA unbalance definition only analyzes one phase current, a new definition of unbalance may be formulated that negates the above two problems where the position of each phase real and reactive power on the real-imaginary plane is examined. Here, the standard deviation of the distance from each phase Cartesian point on the real-imaginary plane is taken as a ratio of the distance from the origin to the average of all phase real and imaginary powers. This is demonstrated below:



**Note:**

A, B & C are the location of each phase power.

'O' is the location of the average phase power.

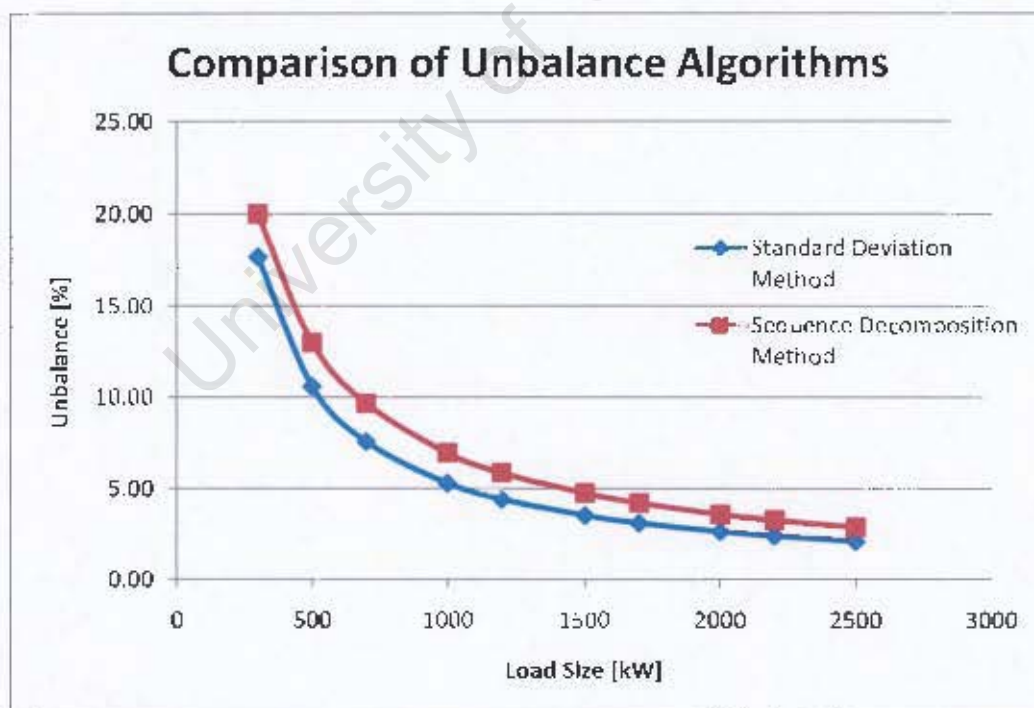
'd' is the distance from the origin to 'O'

's' marks the locus of the standard deviation of the distances from 'A', 'B' and 'C' to 'O'.

It can thus be said that the radius of the circle defined as the standard deviation from the average of the phase powers is a measure of unbalance in the system since in a fully balanced system all points 'A', 'B' and 'C' would occupy the same Cartesian point and the standard deviation would become zero. A measure of unbalance can thus be found by taking the standard deviation of all three phase points as a ratio (percentage) to the distance from point 'O' to the origin (distance 'd'). This method of estimating unbalance accounts for all three phases and will not be heavily influenced by harmonics (since it deals with powers, derived from RMS voltage and current flow). It would be useful to determine the difference between the above unbalance

calculation (using standard deviation from the mean) and the proper method (using sequence decomposition). For this reason, the test performed to calculate the maximum reducible unbalance in section 5 of the main document body is repeated using the new unbalance calculation method.

Load Size [kW]	Maximum Unbalance [%] (Std Deviation)
300	17.68
500	10.61
700	7.58
1000	5.30
1200	4.42
1500	3.54
1700	3.12
2000	2.65
2200	2.41
2500	2.12



Another unbalance method comparison may be performed where the returned unbalance percentages from the two methods are directly compared. This is achieved by running the simulation with the following load sizes:

Phase A:  $200000 + x$  [W]  
Phase B:  $200000 - x$  [W]  
Phase C:  $200000$  [W]

Where 'x' is incremented in increments of 5000 Watts. The results from each unbalance method is recorded and graphed below:

