GROWTH AND CHARACTERISATION OF PLATINUM AND PALLADIUM CATALYSED SILICON BASED NANOSTRUCTURES FOR NANO-DEVICE FABRICATION

by

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LIST OF ABBREVIATION

Pt	Platinum
Pd	Palladium
Si	Silicon
Ti	Titanium
Cu	Copper
Ga	Gallium
O	Oxygen
CH_4	Methane
MBE	Molecular Beam Epitaxy
EBE	Electron Beam Evaporator
RBS	Rutherford Backscattering Spectrometry
PIXE	Particle induced X-ray emission
SEM	Scanning Electron Microscopy
EDX	Energy Dispersive X-ray Spectroscopy
PLD	Pulsed laser deposition

XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
TEM	Transmission electron microscopy
STEM	Scanning transmission electron microscopy
HRTEM	High resolution transmission electron microscopy
BF	Bright Field
ADF	Annular Dark Field
FEB	Focused electron beam
FIB	Focused ion beam
FIB-SEM	focused ion beam-Scanning Electron Microscope
OR	Oxide-reduced
SiNWs	Silicon nanowires
NWs	nanowires
SLS	Solid-liquid-Solid
VSS	Vapour-solid-solid
VLS	Vapour-liquid-Solid

HF	Hydrofluoric acid
ml/m	Millilitres per minute
UHV	Ultra-high vacuum
RT	Room temperature
SAD	The selected area diffraction
ICDD	International centre for diffraction data
FET	Field effect transistors
SOI	Silicon on insulator

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TABLE OF CONTENTS

ABSTRACT……………………………………………………………………………….......xix

CHAPTER 1 .... INTRODUCTION AND LITERATURE 1

1.1 Introduction and motivation 1

1.2 Scope of work presented 2

1.3 Literature review 3

1.3.1 Metal-silicide formation through solid state dewetting...3

1.3.1.1 Platinum and palladium reaction with silicon leading to droplets formation 7

1.3.1.2 Platinum and palladium silicide nanowires 8

1.3.2 Silicon nanowires 10

1.3.2.1 Thermal oxidation of silicon 12

1.4 Metal-Semiconductor contacts 22

CHAPTER 2 ....ANALYTICAL TECHNIQUES 28

2.1 Rutherford backscattering spectrometry 28

2.2 X-ray photoelectron spectroscopy 31

2.3 X-ray diffraction 32

2.4 Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray Spectroscopy (EDX) 35

2.5 High resolution Transmission Electron Microscope technique 36

CHAPTER 3 .... SAMPLE PREPARATION 41

3.1 Preparation of the coatings using molecular beam epitaxy (MBE) 41

3.1.1 MBE coating deposition in the presence of silicon flux 43

3.2 Preparation of the Pt coating using an electron beam evaporator (EBE)....44

3.3 Platinum and palladium catalysed silicon nanowires growth 46

3.3.1 Fabrication of platinum catalysed silicon nanowires based device....47

3.3.2 Fabrication of palladium catalysed silicon nanowires based device....49

CHAPTER 4 .... RESULTS 57

4.1 Platinum silicide formation on MBE deposited samples 57

4.1.1 Self-aligned platinum silicide nanowires and nanoclusters 65

4.2 Platinum silicide formation on the EBE deposited sample 72

4.2.1 SEM and PIXE analysis of the EBE deposited sample 76

4.2.2 First diffusing element during platinum-silicon reaction (EBE deposited sample) 82

4.3 Silicon nanowire growth using platinum as a metal catalyst 85

4.3.1 EBE deposited platinum catalyst 85

4.3.2 MBE deposited platinum catalyst 87

4.4 Palladium silicide formation 101

4.4.1 Growth of nanowires in palladium-silicon system 106

4.4.1.1 Self-aligned palladium silicide nanowires and nanoclusters 107

4.4.1.2 Crystalline core-amorphous shell silicon nanowires using palladium silicide as a catalyst 113

4.4.1.2.1 Electrical properties of FEB deposited platinum contacted oxidation reduced (OR) silicon nanowires..121

CHAPTER 5 .... DISCUSSION AND CONCLUSION 129

5.1 Platinum silicide 129

5.2 Palladium silicide 134

5.3 Nanowire growth summary 136

5.3.1 In-plane nanowires 136

5.3.2 Free standing nanowires 138

CHAPTER 6 ....REFERENCES 140

LIST OF FIGURES

Figure 1.1: Schematic representation of the metal-silicon nano-droplets formation on the Si substrate followed by the growth of the silicon nanowire as the droplets become supersaturated with silicon 5

Figure 1.2: Schematic representation of the metal-silicon droplets onto surface showing the three surface tensions as well contact angle (θ) 6

Figure 1.3: Schematic representation of silicon oxidation given by the Deal-Grove model....15

Figure 1.4: Planar growth of Si oxide (SiO_2) on Si surface..22

Figure 1.5: Energy-band diagrams (a) showing a metal and an n-type semiconductor before contact (b) resultant band diagram after contact and showing the formation of Schottky barrier...24

Figure 1.6: Characteristics of a Schottky barrier in the metal-semiconductor contact 25

Figure 2.1: (a) Van de Graaf accelerator experiment setup, (b) *In situ* real-time RBS and PIXE chembers; inserted images show more detailed features inside both chambers... 30

Figure 2.2: Thermo Scintific (ESCALAB 250Xi model) XPS instrument..............................32

Figure 2.3: D8 Advance Bruker diffractometer used for phase identification 34

Figure 2.4: Photograph showing the Zeiss Auriga field emission scanning electron microscope (FEG-SEM) used for image acquisition 36

Figure 2.5: Possible signals generated upon the interaction of the accelerated beam of electrons with the analysed sample. 38

Figure 2.6: Photograph showing the Tecnai G2 F20 X-Twin Mat 200 kV Field Emission TEM used to obtain coating cross-section and its compositional gradient 40

Figure 3.1: (a) Sample mounting and transfer process, (b) image of MBE (MECA 2000) 42

Figure 3.2: PLD experimental setup, the ablation of silicon inside the PLD (insert image). The silicon vapour (plume) can be seen in blue expanding towards the substrate holder mounted on the heating stage (in red) to account for silicon nanowire growth 46

Figure 3.3: Schematic representation of electron lithography preparation of the Pt-catalysed silicon nanowire based device 47

Figure 3.4: Silicon oxide substrate (about 300 nm SiO_2 layer) showing a nanowire alignment mark 48

Figure 3.5: FEB/FIB instrument: FEI Helios NanoLab 600i 51

Figure 3.6: Silicon nano-wire device fabrication: (a) Oxidised silicon substrate cross-section showing a 92 nm SiO_2 layer (b) isolated Pd catalysed crystalline core-amorphous shell silicon nanowire (c) FE/FIB prepared silicon nanowire device 52

Figure 3.7: (Not to scale) 3D rendered images depicting the fabrication of a silicon nanowire device, using focused ion/electron beam (FIB/FEB), for electrical measurements: (a) silicon nanowires on the SiO_2 substrate (b) FEB-deposited platinum contact lines, (c) EB-deposited platinum contact pads and (d) FIB-deposited platinum contact pads..54

Figure 3.8: Semi-automatic wafer prober-Semiconductor device..55

Figure 3.9: Reference sample showing the device structure without a SiNWs........................56

Figure 4.1: Formation of the Pt silicide on the Si substrate, (a) *In situ* real-time RBS contour map illustrating the sample composition during the reaction of platinum and silicon from room temperature to 600°C. (b) Silicide formation, stability and consumption as a function of the annealing temperature......................................59

Figure 4.2: XPS results showing the binding energies of pure Pt4f spectra recorded at different temperatures 61

Figure 4.3: *In situ* XRD (a) Contour map showing the formation of platinum silicide as a function of temperature (b) Side view of the *in situ* XRD data showing phase formation from the region shown by the red rectangular box 62

Figure 4.4: Imaging of the PtSi silicide after annealing at 950°C for 2 hours. (a) PtSi silicide nano-droplets on silicon <100> substrate, (b) self-aligned PtSi silicide nanoclusters and nanowires on silicon<111> substrate. (c-d) Enlarged areas of image (b) showing different shapes of the PtSi silicide..66

Figure 4.5: The mechanism of the self-aligned PtSi silicide nanostructures. (a) Si (111) substrate, (b) Platinum coated silicon (111) substrate using MBE, (c) PtSi thermomigration at high temperature, (d) silicon incorporation into the moving droplets and formation of silicon steps and (e) Self aligned PtSi nanostructures ..68

Figure 4.6: XRD analysis of the sample with PtSi silicide nanostructures 69

Figure 4.7: Elemental analysis of the self-aligned PtSi silicide nanowire structures...............70

Figure 4.8: (a) Bright Field (BF) TEM image showing a PtSi nanowire situated close to the surface of the silicon substrate. Insert image is the Annular Dark Field (ADF) STEM image with the EDX line scan. (b) Variation of Pt (filled stars) and Si (open triangles) content through the cross-section of the PtSi wire 71

Figure 4.9: *In situ* real-time RBS results showing a colour coded plot of the total spectra collected from RT to 360 °C. Right vertical axis shows temperature regions (1-5) where particular phases are formed 73

Figure 4.10: RBS spectra extracted from figure 1 at three different annealing temperatures. (a) room temperature (b) 230 °C, (c) 300 °C and (d) 350 °C. The surface position of Pt (channel 470) and Si (channel 290) are marked 75

Figure 4.11: SEM images taken from (a) sample after in-situ real-time RBS experiment and (b) sample annealed at 800 °C for 30 minutes under vacuum, showing different morphology 77

Figure 4.12: PIXE scan images of Pt distribution (using multi-layered system in GeoPIXE software) taken from (a) sample after in-situ real-time RBS experiment, and (b) sample annealed at 800 °C for 30 minutes under vacuum, using Si as a host element and Pt as an impurity in GeoPIXE software. Marked regions are the areas where low Pt counts were recorded 78

Figure 4.13: SEM image used to analyse the elemental distribution by EDX (spectra 1-4_ spot analysis and spectrum 5_area analysis), corresponding PIXE image in **fig. 4.12 (b)**..80

Figure 4.14: Cross-sectional TEM of the Pt/Si droplets, corresponding PIXE image in **fig. 4.12 (b)**. Inset, blue and red, images shows the mapping of the distribution of Pt and Si in the droplet 82

Figure 4.15: First diffusing element in the Pt deposited on the Silicon wafer. (a) Ti energy channel position before and after the reaction of Pt and Si. (c) *In situ* XRD analysis of Pt reacting with Si and separated by Ti barrier....................................84

Figure 4.16: Pt silicide catalysed Si nanowires using different growth methods (a) Annealing at 1000 °C in N_2 gas, showing out of plane growth of the wires and (b) Pulsed laser ablation of the silicon target at 800 °C in vacuum, showing in-plane growth of the SiNWs on a silicon substrate. Red arrows are pointing at the nanowire's tips while numbers show the growth of the flower-like structures..86

Figure 4.17: SEM image of crystalline core-amorphous shell silicon nanowires grown on the surface of a Si (100) substrate which was coated with platinum as catalyst 87

Figure 4.18: Crystalline core-amorphous shell silicon nanowires obtained by annealing 20 nm Pt-coated Si<100> substrate at 1000 °C for 15 minutes in 200 ml/m Ar atmosphere (a) Low-magnification TEM image showing several wires and (b) HRTEM image of image-(a) and the zoomed region is shown by the yellow circle. The insert image (b) shows the lattice fringes of the two crossing nanowires 88

Figure 4.19: Crystalline core-amorphous shell silicon nanowires obtained by annealing 20 nm Pt-coated Si<100> substrate at 1000 °C for 15 minutes in a mixture of Ar and CH_4, 250 and 10 ml/m, respectively. (a) SEM image showing SiNWs, (b) corresponding TEM image showing SiNWs with their crystalline core and amorphous shell, insert is a HRTEM showing the lattice fringes of the crystalline core...90

Figure 4.20: (a-b) selected nanowire based devices with their unique device numbers. Red arrow shows the drop-casted silicon nanowires, including the contacted ones between the electrodes. (c) Shows the electrical (I-V) measurement of the selected wires (1, 2 and 3). (d) Shows the temperature dependence of I-V characteristics of a nanowire...91

Figure 4.21: (a) TEM image of a crystalline core silicon nanowires after etching for 40 seconds using 7% HF. (b) zoom image of (a) at the circled area, no oxide shell is left after etching. (c) HRTEM image showing lattice fringes of the crystalline core 93

Figure 4.22: Pt/SiO_x multi–layer structure on silicon substrate (a) in situ real-time RBS analysis, (b) XPS results showing the binding energies of Pt4f spectra recorded at different temperatures 95

Figure 4.23: Pt/SiO_x multi–layer structure on silicon substrate in situ XRD 97

Figure 4.24: Pt/SiO_x multi–layer structure on silicon substrate (a) XPS depth profile analysis below 300 ^oC, (b) XPS depth profile analysis above 300 ^oC and (c) Oxygen depth profile comparison at different temperatures. 98

Figure 4.25: Core-Shell SiNW, (a) decorated with Pt silicide particles after annealing a Pt layer deposited on the nanowires, (b) HRTEM showing the particles in contact with the crystalline core of the SiNW 100

Figure 4.26: **:** *In situ* real-time RBS contour map showing the formation of the palladium-silicide during the palladium and silicon reaction from room temperature to 600°C at 2°C/min ramping rate..102

Figure 4.27: *In situ* XRD (a) Contour map showing the formation of Pd silicide as a function of temperature (b) Side view of the in situ XRD phase formation 104

Figure 4.28: Wide range XRD analysis of the 20 nm coated silicon samples, after in situ XRD (red) and in situ real-time RBS (black)..106

Figure 4.29: SEM images of Pd deposited on Si after thermal annealing in silicon flux: (a-b) the formation of droplets in Pd-coated Si (100), (c-d) the self-aligned wire-like

structures and droplets were observed after thermal annealing the Pd coated Si (111) 108

Figure 4.30: (a) Bright filed (BF) TEM, ADF STEM images and Pd and Si maps taken from a droplet, (b) Variation of Pd and Si concentration across a droplet......................109

Figure 4.31: (a) ADF (STEM) images and maps of a NW, and (b-c) EDS line scans showing the Pd and Si concentration gradients across nanowire......................................110

Figure 4.32: Selected area electron diffraction (SAD) patterns obtained from the Si substrate showing the zone axis [116] (left), and SAD from the Si substrate and NW (right)112

Figure 4.33: Crystalline core-amorphous shell silicon nanowires obtain by annealing Pd-coated (20 nm) n-Si<100> substrate at 1000 ^{o}C for 5 minutes, in Ar gas (a) SEM image showing SiNWs, (b-c) corresponding TEM images showing SiNWs with their crystalline core and amorphous shell (zoomed image). Arrows are pointing at the SiNWs tips 114

Figure 4.34: Crystalline core-amorphous shell silicon nanowires obtained by annealing a Pd-coated (20 nm) n-Si<100> substrate at 1000 ^{o}C for 5 minutes, in a mixture of Ar+CH_4 gas (a) SEM image showing SiNWs, (b-c) corresponding TEM images showing SiNWs with their crystalline core and amorphous shell (zoomed image)115

Figure 4.35: SEM image of SiNWs obtained by thermal annealing in Ar/CH_4 mixture, (a) SEM image showing wool-like SiNWs (b) TEM image showing a single SiNW placed

on a carbon film, (c-d) HRTEM of SiNW with a crystalline core-amorphous shell (circled area) 116

Figure 4.36: Crystalline core-amorphous shell silicon nanowires obtained by annealing a carbon coated n-Si<100> substrate at 1000 ^{o}C for 5 minutes (a) SEM image showing several nanowires and (b-c) corresponding TEM image showing silicon nanowire with crystalline core and OR amorphous shell 117

Figure 4.37: Silicon nanowire device fabrication: (a) oxidised silicon substrate cross-section showing a 92 nm SiO_2 layer (b) palladium-catalysed OR amorphous shell-crystalline core silicon nanowire, along with the contacts for IV measurements. The insert shows contacted nanowire with EB platinum contact lines................122

Figure 4.38: I-V behavior of the 4-point probe nano-device structure recorded at room temperature, OR amorphous shell-crystalline core silicon nanowire (spherical dots) and the reference device sample with no silicon nanowire (square dots)...123

Figure 4.39: I-V behaviour of the 2-point probe nano-device structure recorded at room temperature for the OR amorphous shell-crystalline core silicon nanowire........125

Figure 4.40: I-V behaviour of the 2-point probe Pt contact to n-type Si and Pt/a-Si contact to n-type Si substrate, recorded at room temperature...127

LIST OF TABLES

Table 1.1: Deal-Grove model oxidation coefficients 18

Table 1.2: Show the parameters obtained from the oxidation of the silicon nanowires as presented by Fazzini *et al.* and Liu *et al.* **[79, 81]** 20

Table 4.1: *In situ* real time RBS, in-situ XRD and XPS phase identification for ~20 nm platinum-coated silicon sample deposited using MBE 64

Table 4.2: Data from low Pt and high Pt regions of **fig. 4.12 (a)** 79

Table 4.3: Data from low Pt and high Pt regions of **fig. 4.12 (b)** 79

Table 4.4: EDX data from the dewetted silicide layer 81

Table 4.5: Ratios of amorphous shell to crystalline core of the synthesised SiNWs 120

ABSTRACT

This thesis first describes the application of ion beam techniques for the analysis of synthesised metal silicide nano-droplets which are used to synthesis silicon nanowires. This analysis was performed for both Molecular Beam Epitaxy (MBE) and Electron Beam Evaporator (EBE) deposited metal coated silicon substrates. The formation of platinum silicide phases as a function of annealing temperature and time was investigated using *in situ* real-time Rutherford Backscattering Spectrometry (RBS). *In situ* real-time RBS revealed the reaction of platinum and silicon to start at about 200 °C and 230 °C, for MBE and EBE coatings respectively, forming platinum silicide phases (Pt_2Si and PtSi) in sequence. Further analysis on the EBE deposited coatings using a scanning electron microscope confirmed the formation of droplets at 800 °C. Particle induced X-ray emission analysis showed the variation of platinum concentration, in droplets regions, between 1600 and 2000 counts. The surrounding regions were left almost uncovered due to platinum coating dewetting.

Work was then carried out to investigate the growth of silicon nanowires from the produced droplets. Silicon nanowires were observed to form at 800 °C and 1000 °C using pulsed laser ablation and thermal annealing techniques, respectively, for the EBE deposited coatings. Furthermore, MBE was shown to produce self-aligned platinum silicide (PtSi) nanoclusters and nanowires on Si (111) substrates near the eutectic point (T = 978 °C and 67 *at*% Si) of the platinum silicon system. With an added silicon source in the MBE annealing chamber, the formation of two different silicon steps (straight and wave-like) is reported. The steps determine the position and the shape of the thermomigrating PtSi droplets. Nanoclusters preferentially form

in the triple point of the wave-like steps while nanoclusters that form on the straight steps combine and grow into silicide nanowires.

We report, for the platinum (MBE deposited) catalysed core-shell silicon nanowires, a reproducible method for eliminating hazardous acids during lithography device preparation with the use of silicide forming metal.

With regard to palladium coatings, self-aligned polycrystalline palladium-silicide nanowires and palladium catalysed crystalline core-amorphous shell silicon nanowires were synthesised. The catalyst (palladium) was deposited on a silicon substrate using MBE. As a result of thermal annealing in the silicon flux, self-aligned and fully crystalline palladium-silicide nanowires were synthesised while crystalline core-amorphous shell silicon nanowires were grown when an argon gas was introduced. These results highlight the mechanisms to synthesise specific types of nanowires to be used in a variety of electronic devices depending on their applications.

Furthermore, for the application of the produced core-shell nanowires in nanodevice fabrication, we present two approaches to reduce the oxidation of the nanowires during the thermal annealing growth method. The ratios of the amorphous shell to crystalline core on the nanowires produced, from the two methods, are compared and show a remarkable drop in oxide thickness when compared to nanowires fabricated using the current techniques available. In addition, focused ion beam was utilised to contact the oxide reduced nanowires, without first removing the thin oxide shell, for transport measurements. The oxygen reduced core-shell silicon nanowires showed very low electrical resistivity (4×10^{-1} Ω.cm). The techniques employed presents a new alternative to the production of low cost, high yield, high conducting silicon nanowires that will find use in a range of semiconductor based technology.

CHAPTER 1 INTRODUCTION AND LITERATURE

1.1 Introduction and motivation

The use of platinum (Pt) and palladium (Pd) as metal silicides for electrode contacts in the fabrication of electronic devices, alternative interconnecting material for nanoelectronics device fabrication **[1-3]**, biomolecular sensing **[4]**, in the direct development of Schottky barrier photodetectors **[5-7]** and as a catalyst for the growth of silicon nanowires (SiNWs) **[8-10]** is studied in this research. South Africa is one of the largest producers of Pt group metals and amongst them, Pt and Pd to date, remain the most economically significant. Despite Pt being denser and heavier than Pd, both metals share interesting and important properties, making these materials serviceable in a wide range of applications (electronic, optical, catalysts, high temperature applications, biomedical application and chemical applications, to name a few). They are also good conductors of electricity making them applicable as contact metals in nano-device fabrication **[1-4, 11-12]**.

Nano-devices, i.e. transistors, are mostly fabricated on silicon (Si) substrates and the phase diagram of Pd and Pt in contact with Si at elevated temperatures shows the formation of a liquid solution (metal silicide alloy) **[13-14]**. It is this liquid solution phase (in droplets form) that catalyses the growth of SiNWs, usually near the liquid eutectic temperatures through Vapour-liquid-Solid (VLS) or Solid-liquid-solid (SLS) growth mechanisms **[9-10]**. However, the use of these metals as catalysts for the growth of SiNWs do not appear as widespread when compared to other metals. In this research therefore we investigate the uses of these metals (Pd and Pt) for the production of Si and their silicide nanowires demonstrating their importance and economic significance to the electronic industry for nano-device fabrication. Amongst the SiNWs'

common growth methods Pulsed laser deposition (PLD), chemical vapour deposition (CVD), chemical etching and thermal annealing, PLD and CVD are the least cost effective to have in any laboratory. In addition, CVD requires the use of very expensive gases like SiH_4 or $SiCl_4$ as the source for the growth of the SiNWs, when utilising the VLS growth method. Furthermore, the etching synthesis method has raised questions of safety that comes with the use of hazardous acids. In this research, the reported work is based mostly on a cost cutting and user friendly SiNWs synthesis method (thermal annealing) through SLS mechanism that uses no external Si source. We also detail the production and characterization of Pd and Pt based silicide nanowires with the view to use them as alternative interconnecting materials for nanoelectronic device fabrication and in the fabrication of infrared detectors.

1.2 Scope of work presented

The focus of this work is as follows: (1) to investigate the reaction of Pd and Pt with Si substrates at different annealing conditions. At first the coating thicknesses were varied, however, the report is limited to 20 nm thick layer of the two coatings. (2) Study the effect of annealing the prepared coatings in the presence of Si flux inside the deposition chamber without breaking the vacuum. (3) Study the application of these coatings as a catalyst for the growth of the SiNWs and (4) to determine the electrical properties of the selected SiNWs, for which carbon incorporated Pt contacts, were used. The challenges that come with the use of lithography techniques for the fabrication of core-shell SiNWs incorporated into nano-devices are addressed and possible solutions are presented. The investigation began with the deposition of the coating films (Pt and Pd) on the Si substrate for which two deposition techniques, molecular beam epitaxy (MBE) and electron beam evaporator (EBE) were employed.

Chapter 2 describes the basic principles of the analytical techniques and the approach used to investigate the interfacial reaction of Pt and Pd with the Si substrate as a function of temperature and time. This part of the investigation is accomplished by using complimentary techniques, *in situ* real-time Rutherford Backscattering Spectrometry (RBS), *in situ* X-ray diffraction (XRD) and X-ray photoelectron Spectroscopy (XPS). The reaction of these metals with Si turns the deposited film into silicide nanostructures at high temperatures and the details of the surface morphology analysis using scanning electron microscopy (SEM) is presented. In addition, the observed nanostructures are used as a catalyst to grow SiNWs for which high resolution transmission electron microscope (HRTEM) was used to get more details about the nature of the grown nanowires at the atomic scale resolution. **Chapter 3** describes in detail the sample preparation involving the experimental setup for the deposition of the films. It further details the synthesis and fabrication of the SiNW based devices. The obtained results are presented in **Chapter 4** while the discussions and conclusion are presented in **Chapter 5**. **Chapter 6** list all the references used in this work.

1.3 Literature review

1.3.1 Metal-silicide formation through solid state dewetting

The coating of materials by a thin metal film is widely used in the scientific research as that improves the performance of a coated system in different applications **[1-3]**. However, the performance of such new systems may also change due to the exposure to the different environmental factors, such as temperature. The coated systems under annealing conditions changes the contact structure resulting in the formation of a new phase/s **[15]** developing at the interface. Therefore, the formation of these phases may influence the performance of the coated

system. Depending on the substrate to which the thin films are deposited, the annealing temperature may also introduce thin film dewetting of the new phase layer **[16-26]**. This phenomenon (dewetting process) implies that the surface layer has changed to droplet structures as a result of the annealing effects. It has been reported however that as the thin film begins to dewet, the performance of thin film (Si) on insulator (SOI) based devices is affected **[23-25]** and therefore the phenomenon is not wanted in such device structures. On the other hand, the dewetting of thin films is used as the approach to initiate the growth of SiNWs to be incorporated into nano-device fabrication for better and improved performances **[27]**. For the growth of SiNWs, different metal thin films have been deposited on silicon substrates, as catalyst, and annealed to eutectic temperatures of the metal-silicon systems. Wagner *et al*. **[27]** reported the used of this phenomenon to grow SiNWs, with the growth method termed VLS as the nanowires were growing from the liquid gold (Au) silicide droplets. Then after their work, the metal (Au) became a dominant metal catalyst owing to its binary phase diagram which shows only eutectic point at 360 °C with about 19 at.% Si **[28]**. However, other silicide forming metals can also be used to catalyse the SiNWs at different temperatures based on their phase diagrams with silicon. They are classified according to Bootsma *et al*. **[29]** as (i) Type-A, (ii) Type-B and (iii) Type-C. Type A and type B catalyst metals are dominated by a single eutectic and low Si concentration, above 10 at.% Si and less than 1 at.% Si for type A and B, respectively. Type-C catalysts are high temperature catalysts forming one or more silicide phases at different Si concentrations and comprising of metals like Pd and Pt which are investigated in the current work.

Metal catalysed SiNWs can be grown using a top down or a bottom up approach for which VLS, VSS and SLS growth mechanisms **[30-32]** are applicable. Depending on the synthesis technique and intended application, SiNWs can grow laterally **[33-35]** or perpendicularly **[36]** to the Si

substrate utilising any of the growth mechanisms (VLS, VSS and SLS). Therefore the process of producing these nanostructures requires better understanding of the catalyst seeds (metal-silicide) nucleation, Type-A, Type-B or Type-C, on Si template substrates. The formation of metal silicide phases is dependent on the reaction of the deposited metal on the Si substrate surface at a particular temperature **[36-39]** hence solid-state dewetting in this particular case is viewed as an innovative method for producing well-ordered metal silicide seeds on the Si surface necessary to catalyse nanowire growth **[40-41]**. Therefore the seeds are prepared by depositing a metal catalyst (thin film of few nanometers) onto the Si substrate followed by annealing at high temperatures **[8-10]**. **Fig. 1.1** shows a three step procedure for the growth of Si nanowires applicable for all growth methods, VLS, VSS and SLS.

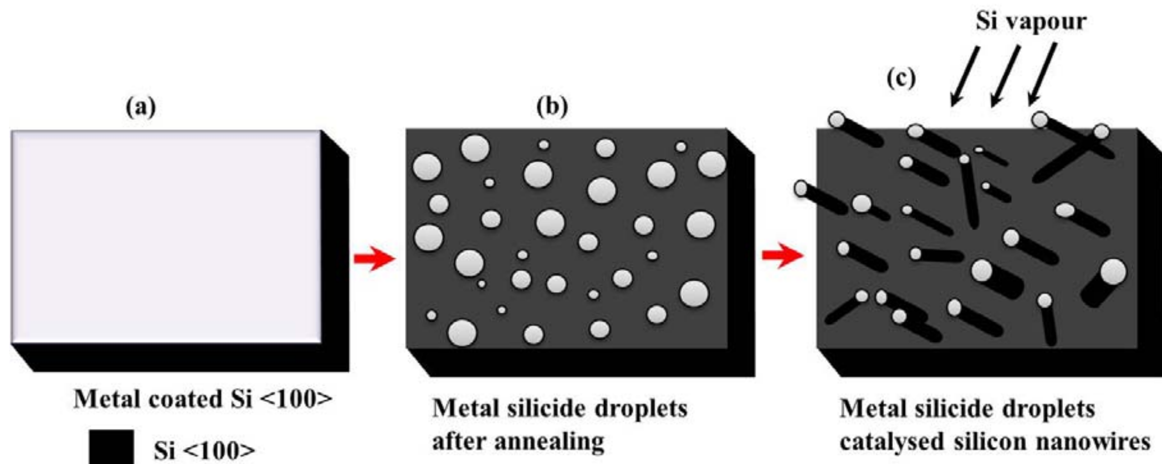


Figure 1.1: *Schematic representation of the metal-silicon nano-droplets formation on the Si substrate followed by the growth of the silicon nanowire as the droplets become supersaturated with silicon*

Figure 1.1 (a) is a schematic representation of the deposited metal catalyst on the Si substrate. Upon annealing at high temperatures, dewetting of the metal layer occurs, **fig. 1.1 (b)**, whereby the thin film experiences difference surface forces leading to the film changing into droplets. The shape of the metal-Si nano-seeds/droplets are determined by the magnitude of the forces at the droplet/surface interface, as schematically shown in **fig. 1.2**. At high temperatures, they appear like a drop of liquid on substrate surface given by Young's equation **1.1 [42]**. The Young's expression relates the three distinct interfaces that exist in the droplet vapour-solid, vapour-liquid and liquid-solid with their corresponding surface tensions, δ_{vs}, δ_{vl}, δ_{sl}, respectively. The contact angle (θ), between the solid substrate and liquid droplet, as well as the shape (size) of the droplet are determined by the surface tensions between three phases (solid, liquid and vapour).

$$\delta_{vl} Cos(\theta) = \delta_{vs} - \delta_{ls} \qquad \textbf{1.1}$$

Where δ_{vl} , δ_{vs} and δ_{ls} are the vapour-liquid, vapour-solid and liquid-solid surface tensions, respectively.

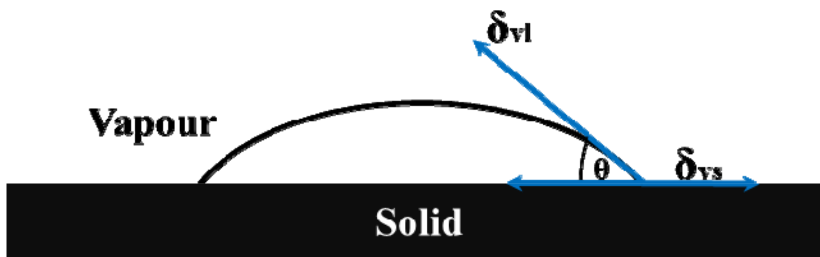


Figure 1.2: *Schematic representation of metal-silicide droplets onto surface showing the three surface tensions as well as contact angle (θ)* ***[42]****.*

In the case of nanowire growth by VLS, VSS and SLS mechanisms, the growth proceeds through the following steps **[43]**: (i) absorption of Si from the gas environment onto the surface of molten metal (molten droplet serving as catalyst), (ii) diffusion of Si through the droplets, (iii) nucleation and crystallisation of Si at the liquid-solid interphase, and (iv) nanowire growth, **fig. 1.1 (c)**. The incorporation of Si atoms into the nano-droplets, for the growth of SiNWs, can be achieved using either sputtering **[44]**, PLD **[45]**, amongst other modalities.

1.3.1.1 Platinum and palladium reaction with silicon leading to droplets formation

The present investigation is limited to Pt and Pd metal catalysts. The reaction between Pt and Si results in the formation of a stable phase (PtSi) at temperatures above 400°C **[37, 46]**, and therefore an extended annealing above this temperature introduces the formation of PtSi island structures (droplets) on the Si substrate, see i.e **fig. 1.1 (a-b)**. There are several stable Pt silicide compounds in the 800 °C - 1000 °C temperature range where SiNWs growth is expected to take place **[14]**. From the phase formation sequence point of view, the reaction in Pt and Si results in the formation of Pt_2Si and PtSi (Pt-Pt_2Si-PtSi) reported to nucleate sequentially **[37, 46]**. The reaction is a two-step process: (i) diffusion of Pt into Si resulting in the formation of Pt_2Si and (ii) diffusion of Si into Pt_2Si for the formation of PtSi. Larrieu *et. al.* **[37]** reported the diffusion of Pt into Si, for the formation of the Pt_2Si phase, to have started at 245 °C and reached completion at 258 °C, while the formation of the PtSi phase by the diffusion of Si into the Pt_2Si phase was found to take place in the 324 °C to 338 °C temperature range. Their results are in good agreement with the findings of Stark *et al*. **[46]** who reported that the conversion of Pt to Pt_2Si to be completed at 261 °C while the conversion of Pt_2Si to PtSi was found to be completed at 335 ^{o}C. The above reports confirm that when annealing at high temperatures, above 350 °C,

the formation of a single PtSi silicide phase is observed. There are no other Si rich phases to form after the PtSi **[14]**, therefore continuing to anneal above this temperature will change the PtSi phase from layer to island structure (droplets) on the surface. The eutectic transformation of the Pt-Si system takes place at 979 °C and 67 at.% Si, for which above this temperature and composition, the precipitation of Si is thermodynamically favourable because of the supersaturation of the droplets with Si.

Regarding Pd, its reaction with Si at low temperatures results in the formation of Pd-silicide, with Pd_2Si reported to be the most stable phase **[47-49]**. The formation of the Pd_2Si silicide phase was found to have reached completion around 200 °C having started with a 100 nm Pd over-layer. Defect in the Pd_2S-Si interface were reported to have contributed to the appreciable Si diffusion from the substrate through silicide phase (Pd_2Si) to the surface above 600 °C. The phase was found to be stable up to 800 °C. Due to the PdSi being the high temperature phase with the last eutectic transformation (L→PdSi+Si) of the Pd-Si system (above 892 °C) **[13, 50]**, the formation of the SiNWs catalysed by PdSi, through VLS, SLS, are therefore expected to grow via liquid PdSi phase droplets. Schrauwen *et al* **[50]** observed, using the *in-situ* XRD, the formation of the PdSi phase to start at 850 °C and transform into liquid phase at 910 °C. Upon cooling, the phase has been found to reverse back to Pd_2Si composition **[13]** and therefore at temperatures below 892 °C, the growth of SiNWs should be initiated by the Pd_2Si solid phase through VSS growth mechanism.

1.3.1.2 Platinum and palladium silicide nanowires

The formation of the PtSi silicide phase has been discussed in section 1.3.1.1 above. It is also the most commonly used compound in photodetection devices due to the ability to detect infrared

light in the 3-5 μm spectral range **[5]**. However, it has only been tested in photodetection applications in the form of thin films, with PtSi thin films on porous-Si substrates reported to have shown good photon collection efficiency **[6-7]**. This compound (PtSi) can be made into nanowires **[1-4]** utilizing a range of different growth modalities for a wide range of applications. Zhang *et al.* **[1]** fabricated platinum silicide nanowires using a sidewall transfer lithography method. The nanowires were reported to have low resistivity (26 μΩ.cm). Their findings were complemented by Lin *et al*. **[2]** who synthesised PtSi silicide nanowires by the silicidation of SiNWs. The nanowires showed good electrical properties with low resistivity of a similar order (28.6 μΩ.cm) and high breakdown/failure current density (> 1×10^{8} A/cm^{2}). However, Tang *et al.* **[3]** reported a higher electrical resistivity (43 μΩ.cm) of the PtSi nanowires fabricated on a silicon-on-insulator wafer. The different growth methods were reported to be the contributing factor to the observed differences in the above characterisation results.

In another approach to grow Pt silicide nanowires, Kavanagh *et al*. **[51]** reported the effect of the Pt deposition temperature on the formation of the silicide nanowires using Si (110) substrates. The elongated silicide nanowires were only observed when the Pt deposition was done at high temperatures. Their findings were complemented by Visikovskiy *et al.* **[52-53]** who also reported their silicide nanowires to be dependent on Pt thickness coverage. In this work, we will present a simple method to synthesis PtSi nanostructures using Molecular Beam Epitaxy (MBE), to fabricate (1) a nano-template of self-arranged PtSi nanoclusters which can subsequently be used as a seed for the growth of ordered SiNWs and (2) self-aligned PtSi nanowire arrays for future use in photodetector fabrication.

The formation of Pd silicide is also reviewed in section 1.3.1.1. It is also a two-step formation process involving a low temperature stable Pd_2Si phase with the formation of a second phase, (PdSi) only at high temperatures. This means that after cooling to room temperature the phase to be identified is Pd_2Si. The phase has been studied for its use as contact material to SiNWs during the fabrication of hydrogen sensor nano-devices that reliably and reversibly detect H_2 at very low concentrations **[11]**. With the advantage of Pd having the similar properties with Pt, Pd_2Si has also been tested for applications in photodetection devices **[54]**. The phase can also be made into nanowires with the view to use them as alternative interconnecting material for nanoelectronics device fabrication **[55]**.

1.3.2 Silicon nanowires

SiNWs (crystalline, crystalline core-amorphous shell and amorphous) have a wide appeal to the wider community owing to their outstanding electronic and optical properties. They are used in different applications such as field effect transistors (FET) **[56]**, biological and chemical sensors **[57]**, in solar energy conversion (e.g. solar hydrogen generation) **[58]** to name a few. Physical vapour deposition, CVD and chemical etching are the most common synthesis methods for growing one dimensional structured SiNWs. Owing to their variety of useful applications in nanoelctronic devices, the structural nature (amorphous or crystalline), diameter and the level of hole and electron doping (n-type and p-type) are important as they contribute significantly to the performance of the nanoelectronic devices incorporating these materials. Many studies on the experimental conditions that determine the nature of the resulting nanostructure have been conducted. Thermal annealing of the source-drain contact and passivation of oxide defects using chemical modification were reported to increase the average transconductance of the FETs

incorporating SiNWs [**56**]. Furthermore, SiNWs present a promising basis for high-performance sensing devices **[59]** due to their high surface to volume ratio. With this added advantage, antigen-functionalized SiNWs were found to detect molecules down to several picomolars **[60]**. Regarding the electrical properties of SiNWs, it has been found that growth direction, size, morphology and surface reconstruction are regarded as important characteristics **[61]**. As the diameter of the SiNWs decreases there is an increase in its band gap which slowly deviates from that of the bulk Si. The studies on the band gap of SiNWs have been done by Nolan *et al.* **[62]** who found that, the band gap modification of SiNWs with smaller diameters exhibit a direct band gap that increases as the wire diameter narrows. Sacconi *et al.* **[63]** also compared the band gap of hydrogenated and SiO_2 terminated SiNWs surfaces and reported a bigger band gap on the hydrogenated wires. With a decrease in diameter from 3.2 to 1.6 nm, the band gap of the hydrogenated wires increased from 1.56 eV to 2.44 eV, while in the SiO2 terminated wires, the band gap went from 1.50 eV to 1.88 eV, with a decrease in diameter of 3.2 nm to 1.6 nm. Zheng *et al.* **[64]**, also reported the effects of wire thickness on the band gap. According to their observation, the band gap falls from about 2.5 eV for a 1.2 nm wire to about 1.56 eV for a 2.7 nm wire.

In this work, we will focus on the syntheses and characterization of Pt/Pd catalysed SiNWs grown using thermal annealing. Depending on the experimental conditions, the annealing method results in the formation of (1) amorphous Si oxide nanowires **[65-67]**, (2) crystalline silicon oxide (c-SiO_x) nanowires **[68-69]**, and (3) crystalline core-amorphous shell silicon nanowires **[70-72]**. Deepak *et al.* **[68]** synthesised crystalline SiO_x nanowires, 50 and 100 nm in diameter with lengths tens of microns long. The crystalline SiO_x nanowires were found to be sheathed with an amorphous layer (a-SiO_x). This is in contrast to the crystalline-core (c-Si)

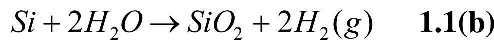
SiNWs also sheathed with a layer of amorphous Si oxide (a-SiO_x) reported by other researchers **[70-75]** using the SLS mechanism. This SLS mechanism is an attractive method for producing SiNWs in large quantities with long lengths (several hundreds of micrometres) without using an external Si source. Studies have been carried out on the effective use of core-shell SiNWs in nano-electronics devices. Cui *et al.* **[72]** studied core-shell SiNWs for high capacity and high current battery electrode applications for Lithium batteries, highlighting the importance of such heterostructure nanowires. These versatile wires have also been used as the building blocks in field effect transistors (FET). Cui *et al.* **[56]** studied the influence of source-drain contact annealing and surface passivation on the transistor properties incorporating core-shell SiNWs. Thermal annealing was found to increase the average transconductance. Further electrical properties studies of these nanowires were carried out by Lee *et al.* **[75]**. Their nanowires were grown using Ni as the metal catalyst deposited onto a cleaned n-type Si (100) substrate. The amorphous shell was first etched away to reveal the ≈10 nm (diameter) crystalline Si core and then followed by the fabrication of Ti/Au contacts creating a SiNW FET device. The device was reported to have displayed good FET device characteristic comparable to that of a VLS grown SiNWs. The current investigation includes the production of oxide reduced (OR) SiNWs using the thermal annealing method, with Pd as a metal catalyst. The electrical properties of single crystalline core-amorphous shell SiNWs without the removal of the outer amorphous shell are presented in this work.

1.3.2.1 Thermal oxidation of silicon

As highlighted previously (**section 1.3.2**) the SLS growth method results in the oxidation of SiNWs which might be a challenge depending on the intended application. Therefore the

understanding of the growth and how to control the formation of oxide shell around the growing SiNWs is of great importance. The oxidation kinetics of the planar bulk Si is explained using the Deal-Grove model **[76]** based on the fundamental diffusion-Ficks law. There are two Si oxide growth methods, dry and wet oxidation, governed by reactions **1.1 (a)** and **1.1 (b)** respectively **[76-80]**.

$$Si + O_2 \rightarrow SiO_2 \qquad \textbf{1.1(a)}$$



$$Si + 2H_2O \rightarrow SiO_2 + 2H_2(g) \qquad \textbf{1.1(b)}$$

Fig. 1.3 shows the schematic of the inward movement of the oxygen atoms during the oxidation of the Si substrate resulting in an oxide layer (x_o). During the oxidation process three steps are considered:

1. The transportation of the oxidant atoms (O_2 in dry oxidation) from the oxidizing gas phase to the outer surface, given by **eq. 1.2**.

$$F_1 = h(C^* - C_o) \qquad \textbf{1.2}$$

Where, F_1 is the number of the oxidant atoms crossing a unit surface area in a unit time (flux), h is the gas-oxide interface reaction rate constant, C_o is the concentration of the oxidant at the outer surface of the oxide and C^* is the equilibrium concentration of the oxidant in the oxide layer.

2. The transportation of the oxidant atoms (F_2) across the oxide layer of thickness x_o to the Si oxide-Si substrate interface assumed to be given by the Fick's law **eq. 1.3**.

$$F_2 = D_{eff} \frac{C_o - C_1}{x_o} \qquad \textbf{1.3}$$

Where, D_{eff} is the effective diffusion coefficient and C_1 is the concentration of the oxidant near the oxide-silicon interface.

3. At the oxide-Si interface, oxygen flux (F_3) reacts with Si to form a new oxide layer (SiO_2) which is expressed by the first-order relation, **eq. 1.4**.

$$F_3 = kC_1 \qquad \textbf{1.4}$$

Where, k is the oxide-Si interface reaction rate constant.

It is discussed by Mahajan *et al.* [**77**] that when oxygen atoms react with Si they turn to occupy interstitial sites in the Si crystal structure and diffuse by hopping between different interstitial site.

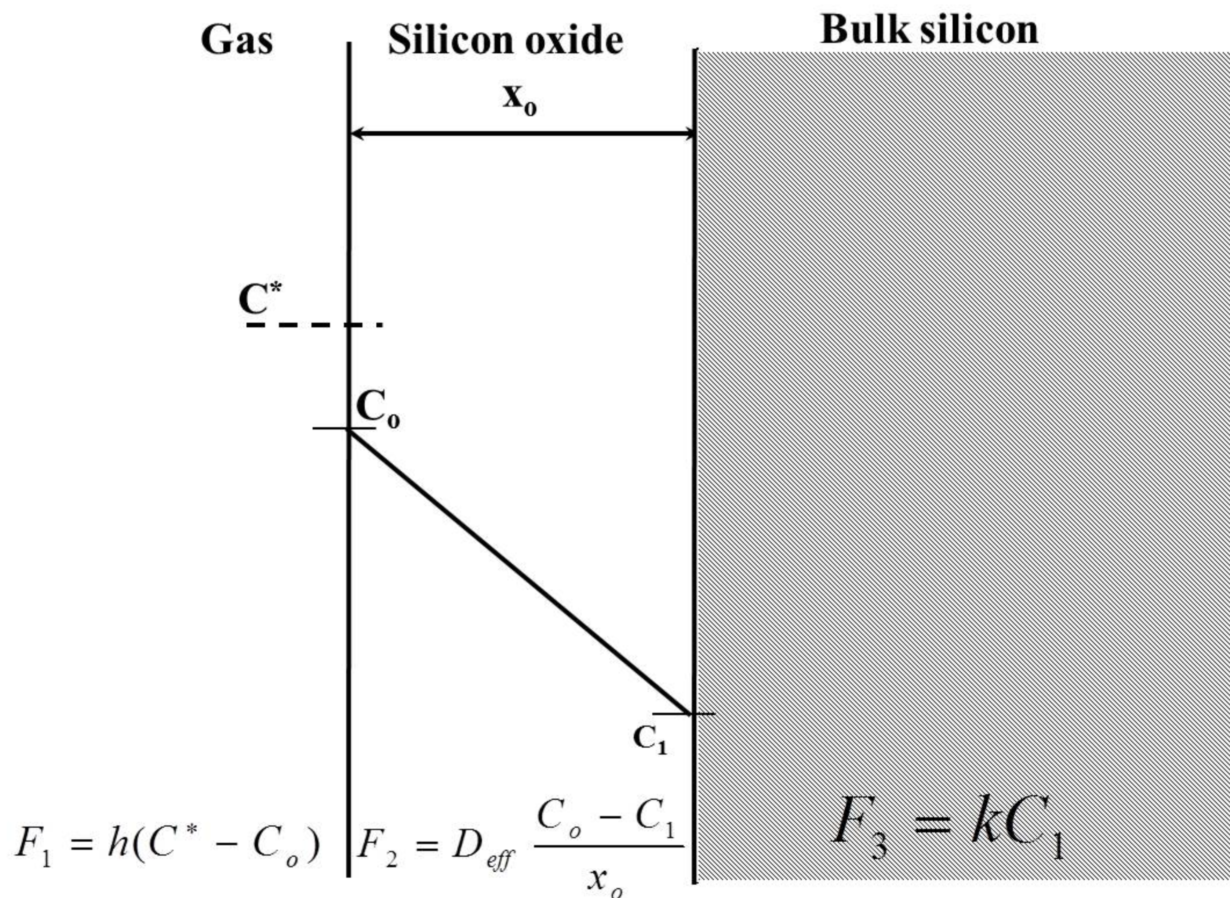


Figure 1.3: *Schematic representation of silicon oxidation given by the Deal-Grove model* ***[76]***

Steady-state diffusion conditions were assumed for which the diffusion flux does not change with time, therefore the oxidant flux is given by the **eq. 1.5**:

$$F = F_1 = F_2 = F_3 = \frac{kC^*}{1 + k/h + kx_o/D_{eff}} \qquad \textbf{1.5}$$

The rate of growth of the oxide layer is given by the differential **eq. 1.6**, considering the number of the oxidant molecules to be incorporated into a unit volume of the oxide layer.

$$\frac{dx_o}{dt} = \frac{F}{N_1} = \frac{kC^*/N_1}{1 + k/h + kx_o/D_{eff}} \qquad \textbf{1.6}$$

Where, N_1 is the number of oxidant molecules required to produce a unit volume of oxide which is 2.3×10^{22} molecules/cm^3 and 4.6×10^{22} molecules/cm^3 for dry and wet oxidation processes, respectively. The solution of the differential, **eq. 1.7**, considering the initial conditions that $x_o = x_i$ at $t = 0$, where x_i represents the initial oxide layer present on the surface prior to the oxidation process is as follows:

$$x_o^2 + Ax_o = Bt + x_i^2 + Ax_i \qquad \textbf{1.7}$$

And can be rewritten in the form:

$$x_o^2 + Ax_o = B(t + \tau) \text{ or } x_o = B\frac{(t+\tau)}{x_o} - A \qquad \textbf{1.8}$$

where,

$$A \equiv 2D_{eff}\left(1/k + 1/h\right) \qquad \textbf{1.8(a)}$$

$$B \equiv 2D_{eff}\, C^*/N_1 \qquad \textbf{1.8(b)}$$

$$\tau \equiv (x_i^2 + Ax_i)/B \qquad \textbf{1.8(c)}$$

The τ term in **eq.1.8** stands for the time shift due to the presence of the initial oxide layer x_i. In addition, the simplification of this equation (**1.8**) gives the oxide thickness as a function of time, **eq. 1.9**.

$$\frac{x_o}{A/2} = \left[1 + \frac{t+\tau}{A^2/4B}\right]^{\frac{1}{2}} - 1 \qquad \textbf{1.9}$$

At a high and law oxidation times, $t >> A^2/4B$ and $t << A^2/4B$, **eq. 1.9** reduces into a parabolic oxidation law and linear law relationship, **eq. 1.9 (a) and (b)** respectively.

$$\frac{x_o}{A/2} \cong \left[\frac{t}{A^2/4B}\right]^{\frac{1}{2}} \text{ or } x_o^{\ 2} \cong Bt \qquad \textbf{1.9(a)}$$

$$\frac{x_o}{A/2} \cong \left[\frac{t}{A^2/4B}\right]^{\frac{1}{2}} \text{ or } x_o \cong \frac{B}{A}(t+\tau) \qquad \textbf{1.9(b)}$$

Where, B and $\frac{B}{A} = \frac{kh}{k+h}\left(\frac{C^*}{N_1}\right)$ are referred to as the parabolic rate and linear rate constants, respectively.

Using the above reviewed relationships, it was possible for the Deal-Grove model to estimate the important Si oxidation parameters as given in the **table 1.1**, which compares the oxidation coefficients from dry and wet oxidation processes. Shown in the table is D_{eff} which is the diffusivity of the oxidants in the oxide layer with their corresponding activation energies (E_A). C^* is the solubility of the oxidant in the oxide and k is the surface reaction rate constant.

Table 1.1: *Deal-Grove model oxidation coefficients*

Deal-Grove model oxidation coefficients	Dry (O_2)	Wet (H_2O)
C^*	5×10^{16} cm^{-3}	3×10^{19} cm^{-3}
k	3.6×10^{4} μ/h	1.8×103 μ/h
D_{eff}	1.0×10^{-1}μ^2/h (E_A = 28.5 kcal/mole)	1.0×10^{1}μ^2/h (E_A = 28.5 kcal/mole)

It should be said that the Deal-Grove model is only applicable for the oxidation of bulk planar Si, however, to look at the oxidation of cylindrical structures (i.e. nanowires) which is of interest in this work, the model has been extended [**74**, **78-79**]. Kao *et. al* [**78**] extended the Deal-Grove model to the non-uniform structures thereby introducing additional factors to be considered as follows:

- Effects of different crystal orientations of curved Si surface on the local oxidation rates,
- Dependence of oxidant diffusion on the shapes of the boundary surfaces,
- Viscous flow in the non-uniform deformation of the oxide, and
- Effects of the stress on the oxide growth rate.

The rate of the oxidation at the Si-SiO_2 is proportional to the product of the surface reaction rate constant (k) and the oxidant concentration at the interface, **eq. 1.10**.

$$\frac{dx_o}{dt} = \frac{1}{N}k_s C_i = \frac{1}{N}\frac{C^*}{1/k_s + (1/h)(a/b) \pm (1/D)a\log(b/a)} \qquad \textbf{1.10}$$

Similar to the Deal-Grove model, **eq. 1.6**, for planar bulk Si oxidation, **eq. 1.10** also describes the growth rate of the new oxide layer at the interface of a cylindrical structure, where, a is the cylindrical structure core radius and b is the total cylindrical structure radius (oxide shell plus Si core radius). It should be mentioned that the physical parameters contained in the above **eq. 1.10** are similar to the one in the Deal-Grove model **eq. 1.6**. Due to the curvature of the surface in the cylindrical structure, the diffusion of the oxidants is different from the convex and concave surfaces. The researchers **[78]** found high oxidant concentration in the convex surface and low concentration in the concave surfaces. It was attributed to the different exposure to the ambient making the convex surface to oxidise faster than the concave surface. In addition, it should also be highlighted that the newly formed and growing oxide layer expands and pushes the previously formed oxide layer which then rearranges through viscous flow. Furthermore, in the convex surface the growing oxide results in the building up of a tensile hydrostatic pressure (P) inside the oxide volume and of a compressive surface stress (σ) at the Si-Si oxide interface. Taking into account the effect of these stresses, tensile (P) and compressive surface stress (σ), Kao *et al.* **[78]** modified the Deal-Grove model oxidation constants for cylindrical structures and their work was later complemented by Fazzini *et al* **[79]** and Liu *et al.* **[81]**, **table 1.2.**

Table 1.2: *The parameters obtained from the oxidation of the silicon nanowires as presented by* Fazzini *et al.* and Liu *et al.* **[79, 81]**.

Silicon nanowire's oxidation parameters	Dry (O_2)	Wet (H_2O)
η_o (poises)	1.5×10^{15}	2.5×10^{14}
V_a [µm]	6×10^{-10}	6×10^{-10}
V_s [µm^3]	2×10^{-11}	7.5×10^{-12}
σ [µm^3/J]	1.5×10^{10}	1.5×10^{10}
C^* [nm^{-3}]	0.015	--------
D [nm^2.h^{-1}]	1.92×10^{8}	--------
h [nm.h^{-1}]	1.0×10^{11}	--------
k[nm. h^{-1}][Deal *et. al*]	3.6×10^{7}	1.8×10^{6}
N[nm^{-3}][Deal *et. al*]	22.5	22.5

The oxidation constants for cylindrical structures are therefore given by **eqs. 1.11-1.13**.

$$k_s = k \times \exp\left\{\frac{-\sigma \times (\Omega_{SiO_2} - \Omega_{Si})}{kT}\right\} \qquad \textbf{1.11}$$

$$D = D_{eff} \times \exp\left\{-\frac{P \times V_a}{kT}\right\} \qquad \textbf{1.12}$$

$$C^* = C^{\,*} \times \exp\left\{-\frac{P \times V_s}{kT}\right\} \qquad \textbf{1.13}$$

Where, k , D_{eff} and C^* are the values of the coefficients determined in the Deal-Grove model for planar oxidation, **table 1.1**, while V_a and V_s are the activation volume of diffusivity and solubility, respectively. Given that the volume of the Si oxide molecules (45 Å^3) is twice the volume of the single Si atom (20 Å^3), the oxide thickness x_o' as well as the new radius of the Si surface r_o' can be estimated using **eqs. 1.14**, **1.15** respectively.

$$x_o' = x_o + \left(\frac{r_o}{r_o + x_o}\right)\frac{25}{45}\Delta x_o + \frac{20}{45}\Delta x_o \qquad \textbf{1.14}$$

$$r_o' = r_o \pm \frac{20}{45}\Delta x_o \qquad \textbf{1.15}$$

Where, r_o is the original radius of the Si surface while x_o represents the original oxide layer. The "-" and "+" signs in **eq. 1.15** represents the convex and concave surface, respectively. However, Buttner *et al.* **[74]** used **eq. 1.16** to calculate the thickness of their newly formed oxide r_{ox} assuming that the original oxide layer was successfully removed from the Si nanowires (r_{NW}) through etching with hydrofluoric acid.

$$r_{ox} = -r_{Si} + \sqrt{\left(1 - \frac{45}{20}\right)r^2{}_{Si} + \frac{45}{20}r^2{}_{NW}} \qquad \textbf{1.16}$$

They found that the oxide thickness reaches the value observed for the planar bulk Si for SiNWs above 44 nm in radius. Mahajan *et al.* [**77**] reported that for the growth of the silicon oxide of thickness t_2, see **fig. 1.4**, the $0.445t_2$ of the silicon is consumed. From this discussion, it therefore

appears that, one can estimate the oxide layer thickness as well as the initial radius of the oxidised structure.

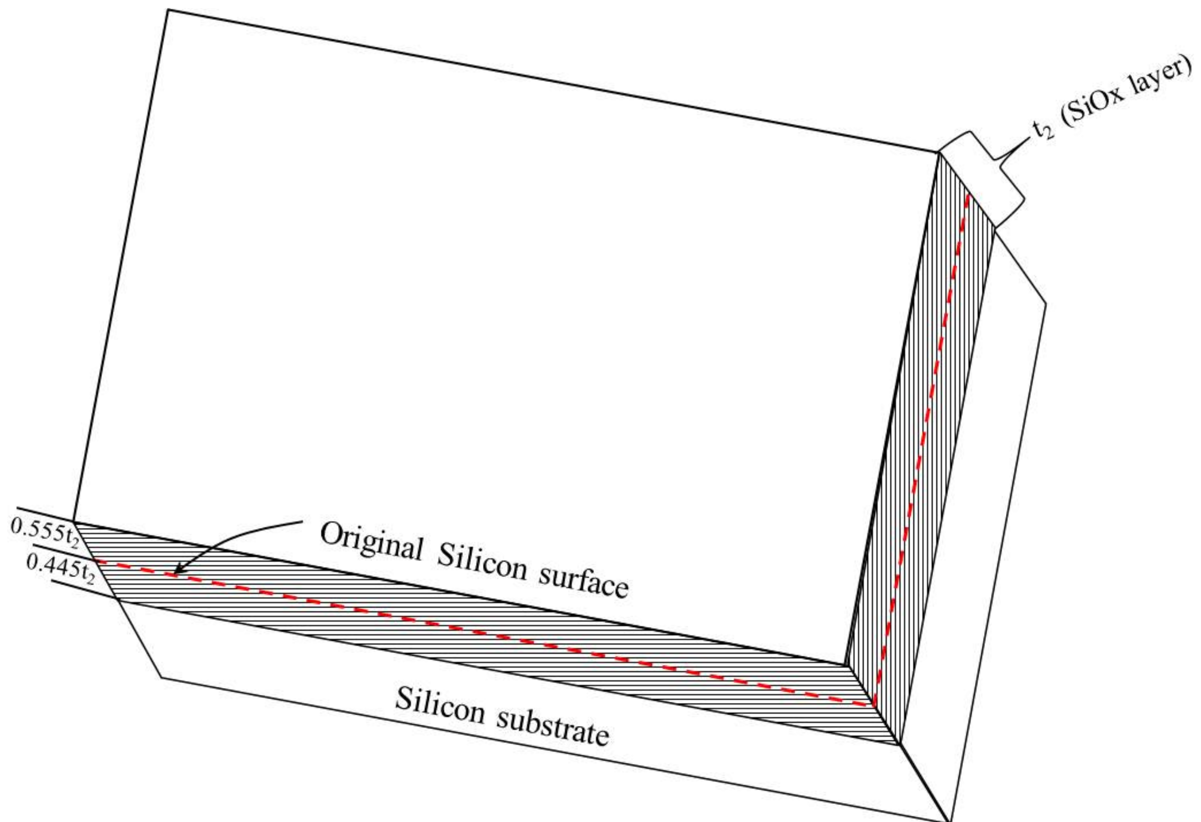


Figure 1.4: *Planar growth of Si oxide (SiO_2) on Si surface* ***[77]***.

1.4 Metal –Semiconductor contacts

In device fabrication processes, the selection of metals to make electrical contact to individual SiNW is an important step that determines the device performance for the intended application. Many metals (e.g. Al, Ti, W, Au, Ag, Pt, Ni, Pd) and silicide (e.g. PtSi, NiSi, TiAu, Pd_2Si) have been used in the fabrication of Si nano-devises as contact materials **[11-12, 56, 75, 82]**. When a metal film is in contact with the surface region of a semiconductor material (during devise

fabrication) the interface between the outside electrical circuitry and the internal current carriers (electron and holes) is created **[77, 83]**. It is the property of the resulting interface that determines whether or not electrons are easily transported from metal to semiconductor when voltages are applied to the device. When the metal contact is made on a heavily doped semiconductor the non-rectifying junction or Ohmic behaviour with a linear (I-V) characteristic is observed. The metal-semiconductor (**M-S**) junction can also form rectifying junctions which are referred to as Schottky barrier junctions, see **fig. 1.5**, when the metal contact is made onto a slightly doped semiconductor, wherein the current-voltage (I-V) characteristics are nearly identical to that of a p-n junction diode **[77, 83]**. In the conductor material (metals) valence bands (E_v) and conduction bands (E_c) overlap, hence electrons are free to move through the vacancies or interstitial sites, as a result, metals are classified as conductors. In semiconductor material, however, there is a band gap between the valence band (E_v) and the conduction band (E_c) as shown in **fig. 1.5 (a)** and electrons in that material are therefore not free to move. A work function ($e\phi_m$) for metal in **fig. 1.5 (a)** is the energy difference between the Fermi level E_f and the vacuum energy level which can be explained as the energy that is required to move an electron from a solid to the vacuum level. In the semiconductor, the energy needed to move an electron from the bottom of the conduction band (E_c) to the vacuum level is called the electron affinity ($e\chi$). It can be seen that, in **fig. 1.5 (a)**, the work function of a metal is greater than the work function of a semiconductor ($e\phi_m > e\phi_s$) which results in the band energy diagram shown in **fig. 1.5 (b)** when the metal-semiconductor come into contact. The Fermi levels of the two materials line up and a potential (Schottky barrier $e\phi_b$) is produced. This is the energy barrier that the electrons must overcome when they jump from the metal region into the semiconductor region.

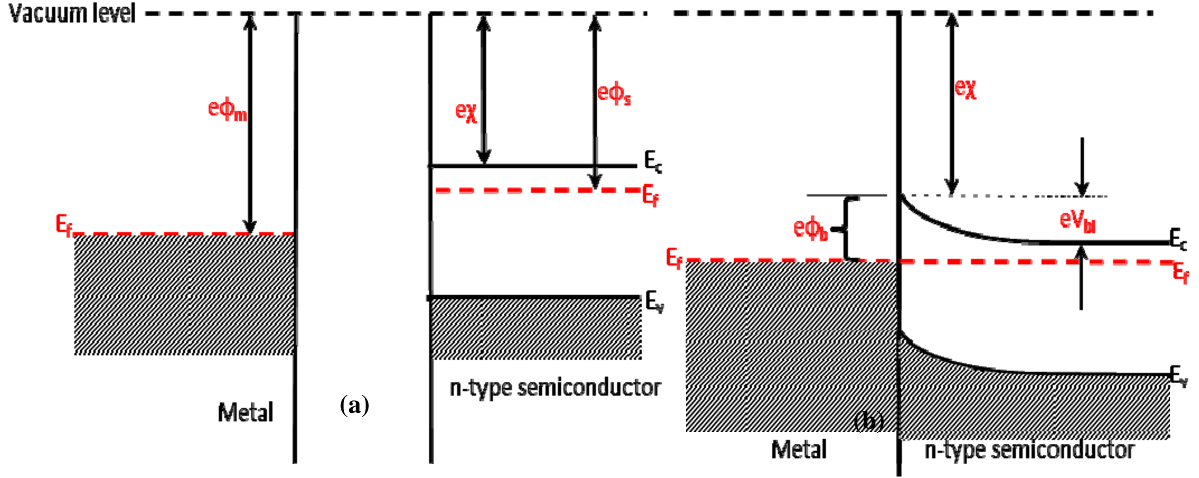


Figure 1.5: *Energy-band diagrams (a) showing a metal and an n-type semiconductor before contact (b) resultant band diagram after contact and showing the formation of Schottky barrier* **[83, 77]**

More simply, it can be regarded as the area in energy space that shows the discontinuity between the Fermi level of the metal and semiconductor. In addition, a space charge region in the semiconductor as well as a potential barrier (eV_{bi}) in the n-type semiconductor near the metal-semiconductor interface are produced by the equalization or lining up of the Fermi levels. The electrons in the semiconductor therefore must cross this barrier eV_{bi} when jumping into the metal region. The above discussed barriers ($e\phi_b$ and eV_{bi}) can be simplified as shown in **eq. 1.21**:

$$e\phi_b = e\phi_m - e\chi \qquad \textbf{1.21(a)}$$

$$eV_{bi} = e\phi_b - \left(E_c - E_f\right) \qquad \textbf{1.22(b)}$$

Where (E_c – E_f), which can be given by eV_n, is dependent on the concentration of the dopant used in the semiconductor material. The characteristics of a Schottky barrier in a metal-semiconductor contact (rectifying behaviour) are schematically shown in **figs. 1.6 (a-b)**. When a negative voltage (forward biased) is applied, the barrier that the electron must overcome in going from semiconductor to metal is changed or pushed up, **fig. 1.6 (b)**. Electrons in the semiconductor region will then jump (over the barrier bridge) into the metal, this phenomenon is referred to as thermionic emission. The potential barrier $e\phi_b$ on the metal side of the diode remains unchanged under forward biasing. Therefore, the potential barrier (eV_{bi} for V = 0 (no voltage applied)) decreases under negative voltage/ forward biasing to eV_{bi} - eV_F and increases to eV_{bi} + eV_F when reverse biasing (V_R) is applied. This means that the current will flow in one direction when forward biasing is applied and the potential barrier becomes eV_{bi} - eV_F, which is characteristic of a normal diode. However, a Schottky junction can sometimes possess characteristics of a near Ohmic contact, which means that one can still observe the flow of electrons from the metal side into the semiconductor region under reverse bias.

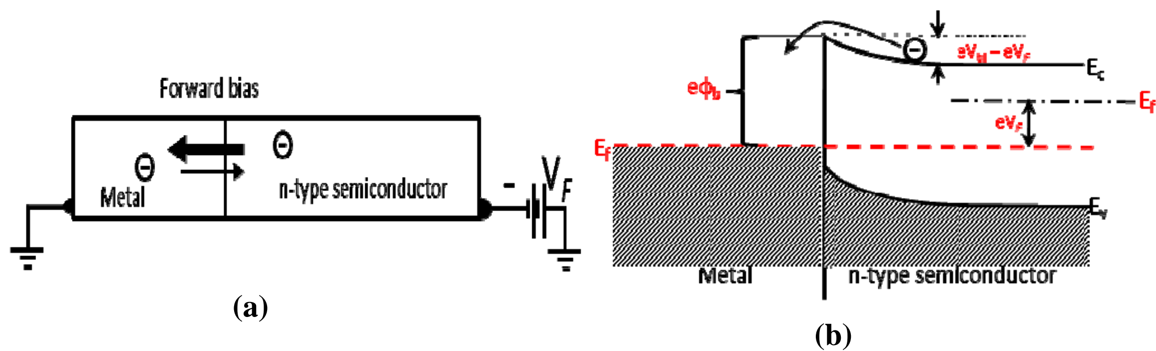


Figure 1.6: *Characteristics of a Schottky barrier in the metal-semiconductor contact* **[77, 83]**

The near Ohmic contact can be created by contacting a metal to a heavily doped n^+-type or p^+-type semiconductor **[77, 83]**. The doping of the semiconductor reduces the new bandwidth that exists after the metal comes into contact with the semiconductor. A tunnelling current is then possible if the electron in the metal region has the energy equal to the energy of the valance state. Therefore, the likelihood of tunnelling current depends on the new bandwidth, which also depends on the dopant level of the semiconductor. With a heavily doped semiconductor, one expects to achieve a reduced bandwidth, hence more electrons will move from the metal to the semiconductor under reverse bias, with ohmic I-V characteristic behaviour **[83]**. The electron flux (direction and magnitude) in the metal-semiconductor barrier is determined by the change in the potential. The electron current flux from metal to semiconductor $J_{m\rightarrow s}$ is equal to the electron current flux from semiconductor to metal $J_{s\rightarrow m}$, **eq. 1.22**, when no voltage is applied to the system. This implies that the net current flux (J) is equal to zero.

$$J_{m\rightarrow s} = J_{s\rightarrow m} \qquad \textbf{1.23}$$

For the I-V characteristics investigation of the metal-semiconductor system, it is important to first know the number of electrons that have energies greater than the potential barrier. The number of electrons in the metal side of the system having energies greater than the barrier height $e\phi_b$ is given by Maxwell-Boltzmann statistics, **eq. 1.23**. This equation applies when a reverse bias (positive voltage) is applied to a n-type semiconductor for electrons to jump from the metal region to the semiconductor region. On the other side, the number of electrons able to overcome the potential barrier eV_{bi}, when moving from the semiconductor region to the metal region, is given by **eq. 1.24** below.

$$J_{m\to s} = \exp\left(e\phi_b / kT \right) \qquad \textbf{1.24}$$

$$J_{s\to m} = \exp\left(eV_{bi} / kV \right) \qquad \textbf{1.25}$$

Under no applied voltage, the two equations are equal. However, when the forward bias is applied to the system which results in the reduction of the potential barrier by eV_{bi} - eV_F, which means therefore that $J_{s\to m} >> J_{m\to s}$, **fig. 1.6**, the number of electrons that can flow from semiconductor to the metal region increases by a factor $\exp(eV_F/kT)$ as shown in **eq. 1.26**.

$$J_F = J_{ST} \exp\left(eV_F / kT \right) \qquad \textbf{1.26(a)}$$

$$J_{ST} = AT^2 \exp\left(-e\phi_b / kT \right) \qquad \textbf{1.26(b)}$$

where J_F is the forward bias current density, J_{ST} is a constant which is independent of the voltage and A is the Richardson's constant (A ≈ 100Amp/cm^{2}K^2) for thermionic emission of electrons from a semiconductor to metal.

CHAPTER 2 ANALYTICAL TECHNIQUES

The basic principles of the analytical techniques used for sample analysis, Pt-Si, Pd-Si coated specimens, in as-deposited and annealed conditions, are described in this chapter. The samples were characterized using *in situ* real-time RBS in order to determine the kinetics of phase transformation, SEM for the investigation of the annealing effect on the surface morphology of the coatings, HRTEM for the morphology, structure and composition analysis of a single nanowire, EDX and PIXE for compositional analysis of the costed samples after annealing, and XRD for the phase identification analysis. The XRD and RBS results for phase identification were complemented by using XPS. The basic principles of these complementary techniques are described in this chapter.

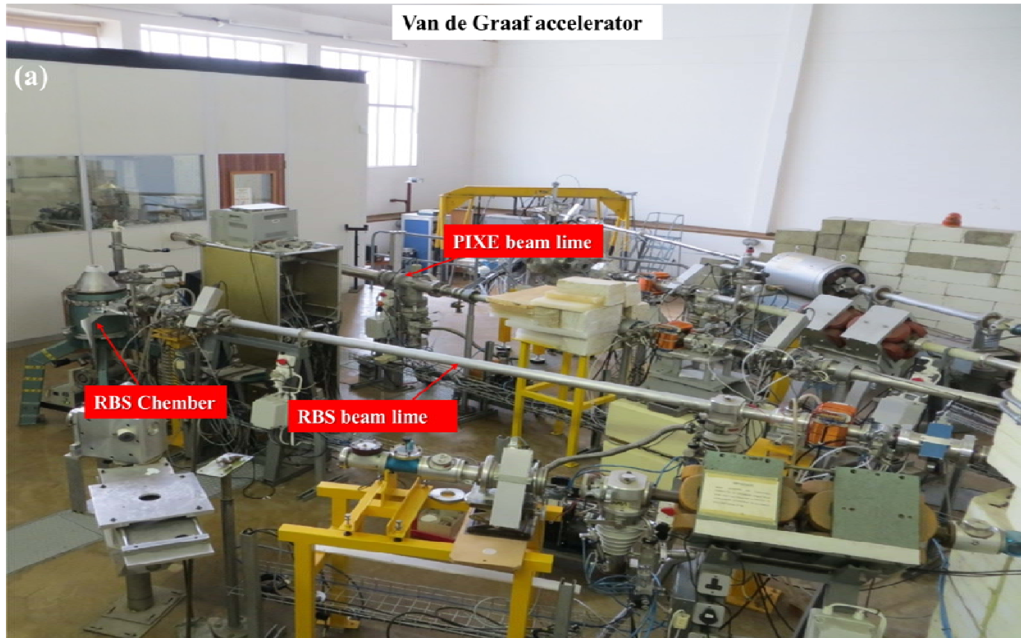
2.1 Rutherford backscattering spectrometry

The phase transformation sequence as well as diffusion species on metal coated Si system were of interest in this work. Therefore, *in situ* real-time RBS was performed on the Pt-Si and Pd-Si coatings to investigate the interfacial reaction and compound composition. The experiments were done using a mono-energetic beam of alpha particles (2 MeV) on a Van de Graaf accelerator. In the experiment, the alpha particles collides with the target atoms of Pt/Pd and Si and are scattered in a backward direction and measured by a surface barrier detector (with 20 keV resolution), at 165 degrees (θ) with respect to the oncoming beam. The measured energy (E_1) of the backscattered particles depends on both masses of incident beam (M_1) having energy E_0, and target atoms (M_2) according to the following **eq. 2.1 [84-85]**:

$$\frac{E_1}{E_0} = K = \left[\frac{(M_2{}^2 - M_1{}^2 \sin^2 \theta)^{1/2} + M_1 \cos\theta}{M_2 + M_1} \right]^2 \qquad \textbf{2.1}$$

Where: K is the kinematic scattering factor, described as the energy ratio of the particles before and after the collision. From the recorded backscattered energy data, one can identify the target atoms as well as the compound composition and the thickness of the thin film. To study the reaction kinetics of Pt or Pd with Si, the coated wafers were cut into small samples of approximately 1 cm × 1 cm and analysed using *in situ* real-time RBS. The *in situ* real-time RBS experiments as well as PIXE were performed in a Van de Graaf accelerator, **fig. 2.1**. For the *in situ* real-time, 2 MeV alpha particles, at a backscattering angle of 165°, a beam spot size of 2 mm and in a vacuum of $5x10^{-6}$ mbar, was used. The data was collected using a surface barrier detector (with 20 keV resolution) and the angle between the sample surface and the incident beam was -10°. The sample was mounted on a flat copper surface heating stage with a thermocouple mounted at the back. The thermal annealing was carried out with linear temperature ramping from room temperature (RT) to a maximum of 600 °C at 2 °C per minute. The recorded *in situ* real-time spectra were simulated using RUMP software **[86]** for compound composition determination.

As an extended fixture of the ion beam analyses technique, PIXE **[83, 87]** was used for the mapping of elemental distribution in the coated surface. Contrary to the bombardment of the samples with the beam of electrons in the EDX technique, in PIXE, the analysed samples are bombarded with ions of energy in the order of MeV protons in the accelerator, i.e. Van de Graff accelerator. Therefore, a 3 MeV focused proton beam of about 3.5 µm × 3.5 µm lateral resolution was raster scanned on the sample surface (area of 20 µm × 20 µm) using an electrostatic scanning coil. Beam current was kept at about 100 pA with minimum instability in order to avoid sample damage. Scanned areas were analysed in a square pattern of up to a maximum of 28 × 28 pixels, with a dwell time of 10 ms/pixel.



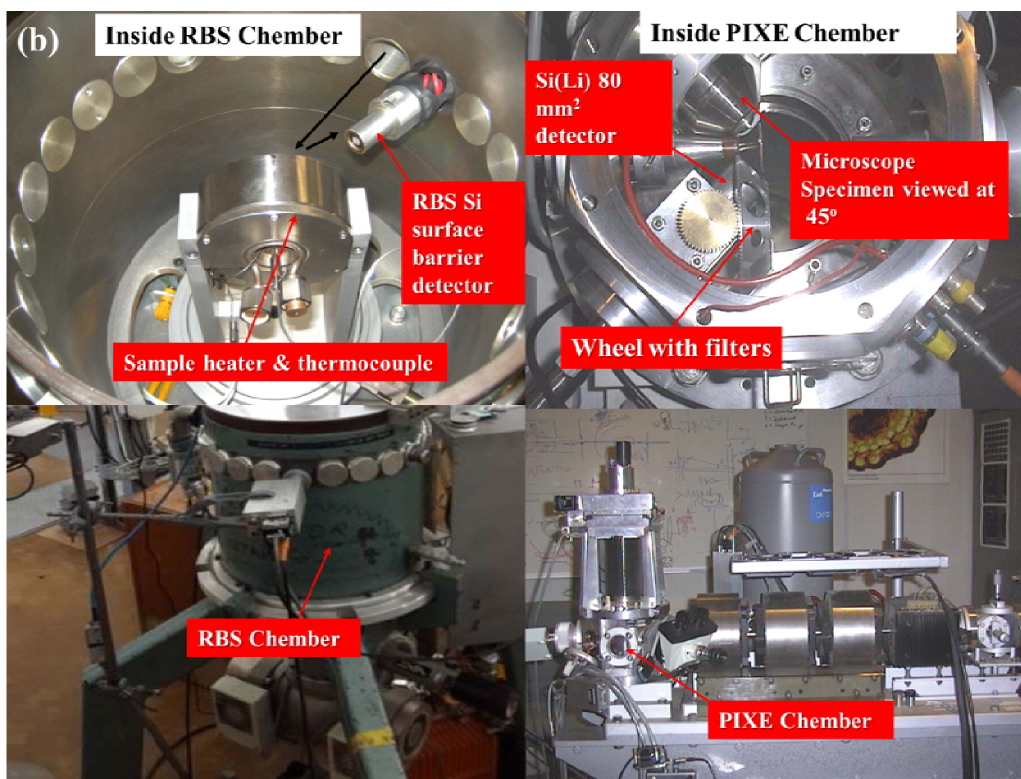


Figure 2.1: (a) *Van de Graaf accelerator experiment setup, (b) In situ real-time RBS and PIXE chembers; inserted images show more detailed features inside both chambers.*

Spectra of PIXE coupled with a proton backscattering detector (at 176 °C scattering angle) were acquired in an event-by-event mode, using a Si (Li) X-ray detector positioned at an angle of 135° and shielded with a 125 μm Beryllium (Be) filter. The GeoPIXE II software **[88]** was used to interpret the data.

2.2 X-ray photoelectron spectroscopy

To complement the RBS results, the surface elemental and compound composition analyses was performed using X-ray photoelectron spectroscopy (XPS) technique. The fundamental principle of this technique is based on the photoelectric effect **[89]**. Upon the absorption of the photons by the surface atoms of the samples, the energy of the generated photoelectron can be calculated according to **eq. 2.2**. The energy of the X-ray would have to be greater than the binding energy of the electron plus the work function of the metal for the photoelectric effect to take place.

$$KE = E_{X-ray} - BE - \varphi \qquad \textbf{2.2}$$

Where, $E_{X\text{-}ray}$ is the energy of the incident X-rays, BE is the binding energy of the electron and φ is the minimum energy required to move an electron from the surface (work function) of the metal.

Atoms from different elements present in the surface of the analysed sample have a unique set of binding energies within the different energy levels (orbitals) and therefore the detected KE energies are used to fingerprint the surface elements as well as the compound composition. The Thermo Scientific (ESCALAB 250Xi model) XPS instrument, **fig. 2.2**, used was equipped with Aluminium (Al) as a source of X-rays with a monochromatic beam energy and diameter of 1487

eV and 900 μm, respectively. Experiments were performed in ultra-high vacuum conditions (10^{-9} mbar base pressure).

Figure 2.2: *Thermo Scintific (ESCALAB 250Xi model) XPS instrument*

2.3 X-ray diffraction

Another technique for the analyses of the phases present in a crystalline sample is XRD. It was therefore used to complement RBS and XPS results. In the XRD experiment, X-rays interaction with the periodic arrangement of atoms in a crystalline sample leads to the coherent scattering by the electrons of the atomic planes thus revealing the structural (phase) information of the sample. This is possible when geometric conditions given by Bragg's law, **eq. 2.3**, are met **[90]**.

$$n\lambda = 2d\sin\theta \qquad \textbf{2.3}$$

d, is the separation of the periodical arrangement of atoms in the sample, λ-wavelength of the Cu X-ray beam, *n*-whole number of wavelengths and θ-diffraction angle. By scanning the specimen over a large range of diffraction angles, one obtains the diffraction pattern with different peaks (*d*-spacing), plotted in 2θ (in degrees) versus intensity (arb.units) which represents the atomic bonding in the sample. From the resulting diffraction pattern, the phases present are identified. In this work, room temperature (RT) and *in situ* XRD measurement were performed. For RT XRD experiments, data were collected at room temperature using a D8 Advance Bruker diffractometer, **fig. 2.3**. A Copper (Cu) target, as a source of X-ray (CuKα radiation ($\lambda \approx 1.54$Å) was used and was operated at 40 kV and 40 mA. The configuration of the diffractometer used was in such a way that the detector and the X-ray tube move in a locked coupled mode, θ-θ scan mode while the analysed sample remains at a fixed position. The patterns were then compared to the reference diffraction patterns contained in the XRD database, international centre for diffraction data (ICDD) 1998, to identify the phase/s present in the sample. Regarding the *in situ* XRD, measurements were carried out in a He flow (200 ml/m), ramp rate of 30°C/min and measurement time of 3s using a D8 Discover Bruker diffractometer. Data were collected between 27° and 48° in 2θ.

Figure 2.3: *D8 Advance Bruker diffractometer used for phase identification*

2.4 Scanning Electron Microscope (SEM) and Energy Dispersive X-ray Spectroscopy (EDX)

The effects of annealing on the morphology of the coated substrate were analysed using SEM. SEM uses a focused beam of electrons from a tungsten filament to scan the surfaces of the analysed samples. The electron beam is directed to the surface of the samples by means of electromagnetic lenses (condenser and objective lenses) through the lenses aperture to acquire the surface morphologies. Amongst the generated signals (Backscattered electrons, characteristics X-rays, secondary electrons, cathodoluminescense, auger electrons and specimen current) upon the interaction of the electron beam with the atoms of the samples **[91-92]**, characteristics X-rays (for average elemental composition) and secondary electrons (for surface morphology) were of interest in this work. The surface morphologies of samples were acquired using a Zeiss Auriga field emission SEM (FEG-SEM), **fig. 2.4**, operated in secondary electron mode with the electron energy in keV. The characteristics X-rays generated upon the interaction of electrons with the atoms of the analysed samples were analysed for the determination of the elements in the sample. This technique is termed energy dispersive X-ray spectroscopy (EDX), making it an additional feature of the SEM. The determination of the element therefore is based on the spectral analysis of the characteristic X-rays emitted from the atoms of the sample upon irradiation with the electron beam **[91-93]**. The produced X-rays were recorded and measured using an energy dispersive detector.

Figure 2.4: *Photograph showing the* Zeiss Auriga field emission scanning electron microscope (FEG-SEM) *used for image acquisition*

2.5 High Resolution Transmission Electron Microscope technique

The structural properties of the grown SiNWs were investigated using a HRTEM. The technique allowed for better imaging of single SiNW leading to more detailed identification of its features at the atomic scale resolution. Such details can not be obtained using light microscopes due to the limited resolution, which is approximated by Rayleigh criterion given by **eq. 2.4 [91-94]**.

$$\delta = \frac{0.61\lambda}{\mu \sin \beta} \qquad \textbf{2.4.}$$

Where, λ is the wavelength of the radiation, β the semi-angle of collection of the magnifying lens, and μ the refractive index of the viewing medium.

Using **eq. 2.4**, the resolution of the light microscope (with about 550 nm wavelength, visible light) is estimated to be 300 nm, about half the wavelength of the light source **[94]**. With such resolution, more detail about the nanomaterials can not be resolved as this is viewed to correspond to about 1000 atom diameters. With this limitation, electron microscopy was the instrument of choice in this work. The wavelength (λ) of the resulting electron wave, generated from the source (electron gun) and accelerated by the voltage applied, depends on its acceleration energy according to the Louse de Broglie's equation, **eq. 2.5 [94]**.

$$\lambda = \frac{1.22}{\sqrt{E}} \qquad \textbf{2.5}$$

Where, E is the energy of the accelerated electron in electron volts (eV).

Given the acceleration voltage (e.g. 100 keV), one can estimate the wavelength of the electron wave to about 0.004 nm, which is two orders of magnitude smaller than the diameter of a single atom. It is therefore possible to get more details about the atomic structure of the materials using electrons (described as a plane wave, **eq. 2.6**) instead of light.

$$\psi = \psi_0 e^{2\pi ikr} \qquad \textbf{2.6}$$

Where, ψ_0 and $2\pi ikr$ are the amplitude and phase of the wave, respectively.

The beam of electrons (from the source) travels in vacuum through condenser lenses which determines the beam diameter as they land on the sample. **Fig. 2.5** shows all the possible signals generated upon the interaction of the accelerated beam of electrons with the analysed sample.

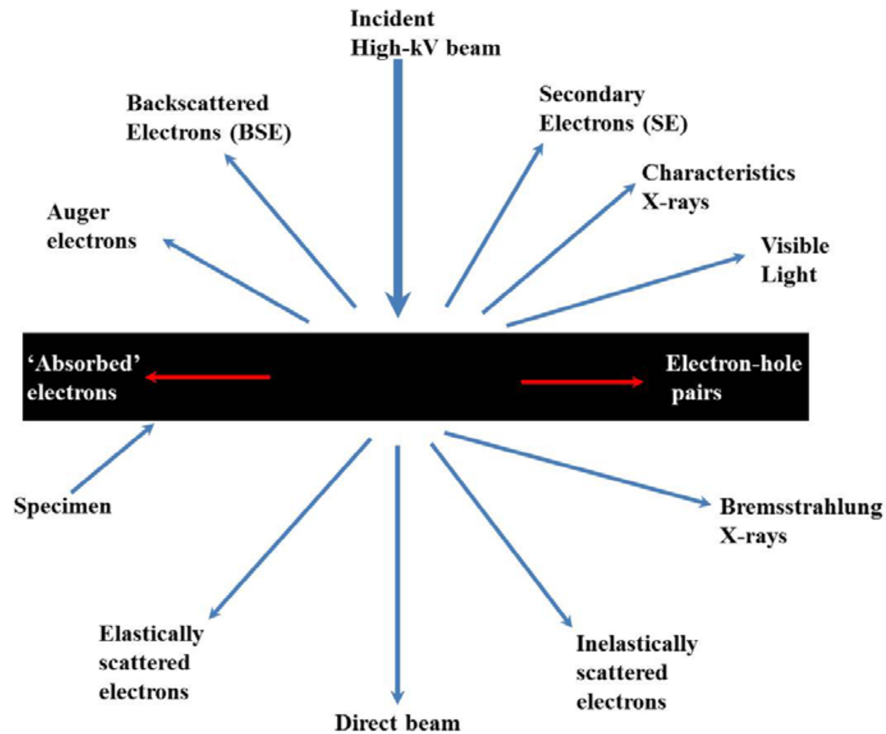


Figure 2.5: *Possible signals generated upon the interaction of the accelerated beam of electrons with the analysed sample **[94]**.*

Contrary to the SEM technique, some electrons are transmitted through to the objective lens located just below the specimen. The objective lens is regarded as the most important lens of the TEM instrument that controls the formation of the image. The TEM instrument can be operated in ether Dark-field (DF) or Bright field (BF) mode. In the BF mode only the direct beam, see **fig. 2.5,** is selected to form the image and the information to be included in the final image is determined by the size of the objective aperture. In the DF mode, electrons that are not in the

direct beam are selected to form the image. The last part of the instrument is the projector system that magnifies the image and focuses it on the viewing screen. For the HRTEM experiment performed in this work, the SiNWs were first removed from the Si substrate using a razor blade. A few drops of ethanol were put on the surface of the scratched area so as to obtain an ethanol solution with SiNWs. Then, a copper grid with an amorphous carbon thin film was pulled through the ethanol-SiNWs solution. The grid was then dried in air before transferring it into the HRTEM instrument. The micrographs of the nanowires were acquired using the Tecnai G2 F20 X-Twin instrument, **fig. 2.6**, which was operated at an accelerating voltage of 200 kV. The transmitted electrons were detected by the Si(Li) EDAX detector while the source of electrons used was a Schottky Field Emission Gun.

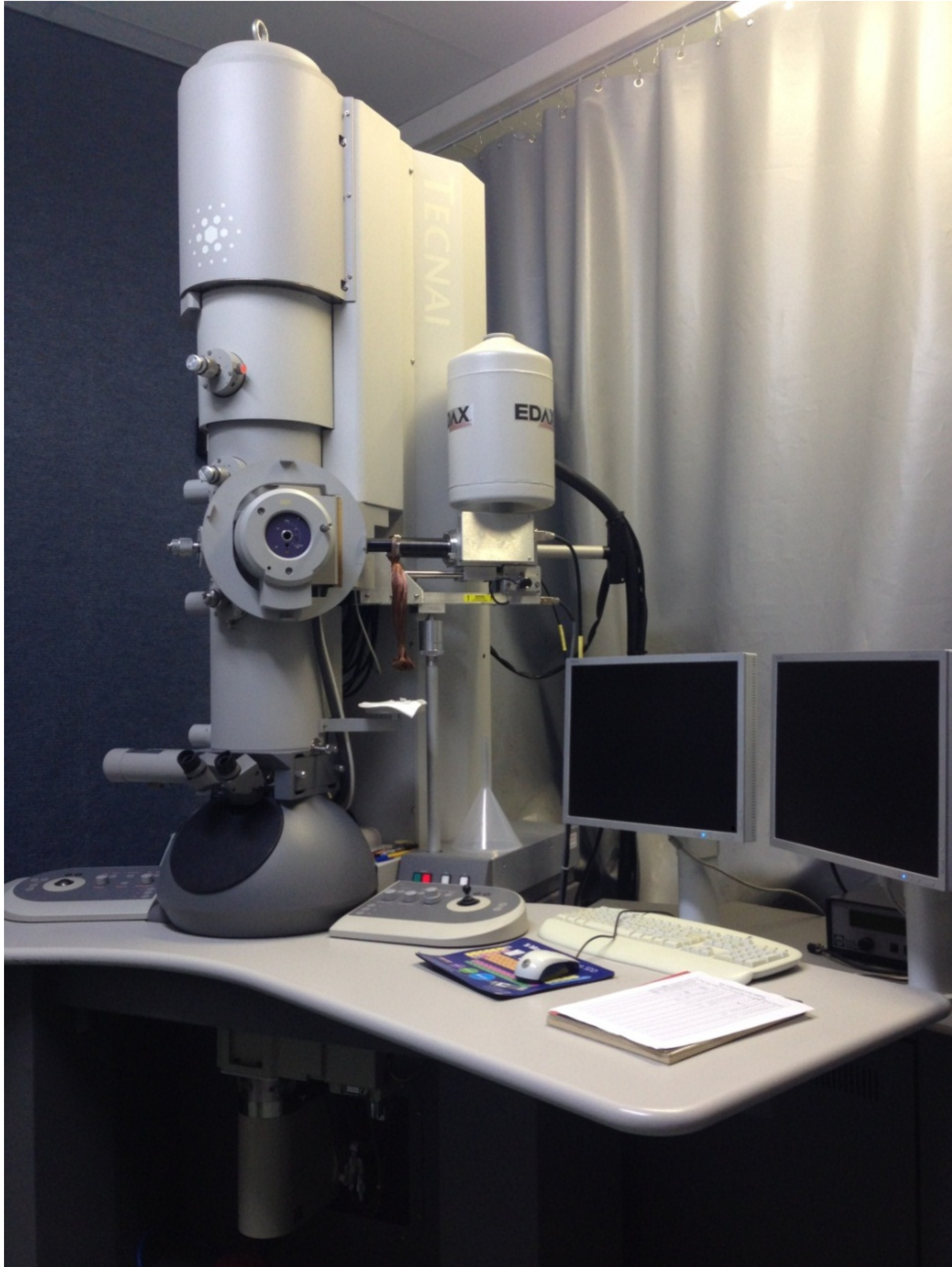
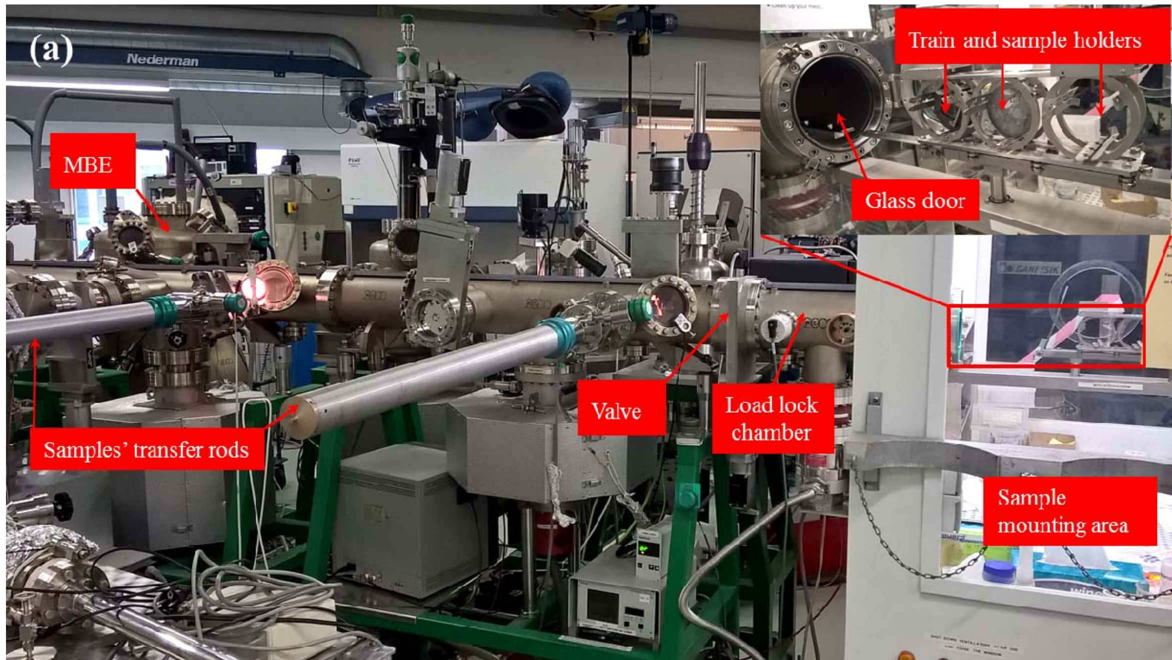


Figure 2.6: *Photograph showing the Tecnai G2 F20 X-Twin Mat 200 kV Field Emission TEM used to obtain coating cross-section and its compositional gradient*

CHAPTER 3 SAMPLE PREPARATION

3.1 Preparation of the coatings using molecular beam epitaxy (MBE)

To investigate the reaction of Pt and Pd with a Si substrate, the coatings were prepared using an ultra-high vacuum (UHV) molecular beam epitaxy (MECA 2000) system at the institute for Nuclear and Radiation Physics, KU Leuven (Belgium), **fig. 3.1**, on two Si substrates: (1) n-type Si (100), 5 cm in diameter, 280 μm thick and with a resistivity of 1-10 ohm.cm and (2) p-type Si (111) also 5 cm in diameter and 1-10 ohm.cm resistivity. The cleaning of the substrates and deposition conditions were kept similar for the two Si substrates. The substrates were cleaned using a RCA-cleaning procedure [**95**] consisting of four steps: (1) To remove all the organic compounds residing on the substrate surface, the substrates were placed into a mixture of 120 ml deionised water, 40 ml sulphuric acid and 40 ml hydrogen pentoxide and boiled at about 70 ^{o}C for 10 minutes. (2) Samples were then immersed into the solution consisting of 100 ml deionised water, 20 ml ammonium solution and 20 ml hydrogen pentoxide and boiled for 10 minutes so as to etch away metallic compound contaminants and metal oxides. (3) The aim of the third step was to remove all ionic contaminates bound to the surface by placing the substrates in the solution of 100 ml deionised water, 20 ml hydrochloric acid and 20 ml hydrogen pentoxide. The solution was also boiled at 70 ^{o}C for 10 minutes. (4) The fourth step involved the removal of a thin layer of oxide by dipping the substrates for 1 minute into a diluted 2% HF solution. The substrates were afterwards dried using N_2 gas and immediately loaded into the sample holders and then placed into the train (insert image). Since MBE is a UHV system, many steps to maintain the good vacuum of the system were followed. Firstly, after the samples were cleaned as described above, they were mounted on the substrate holders which were then placed in the train and rolled into the load lock through the glass door, see the insert in **fig. 3.1 (a)**.



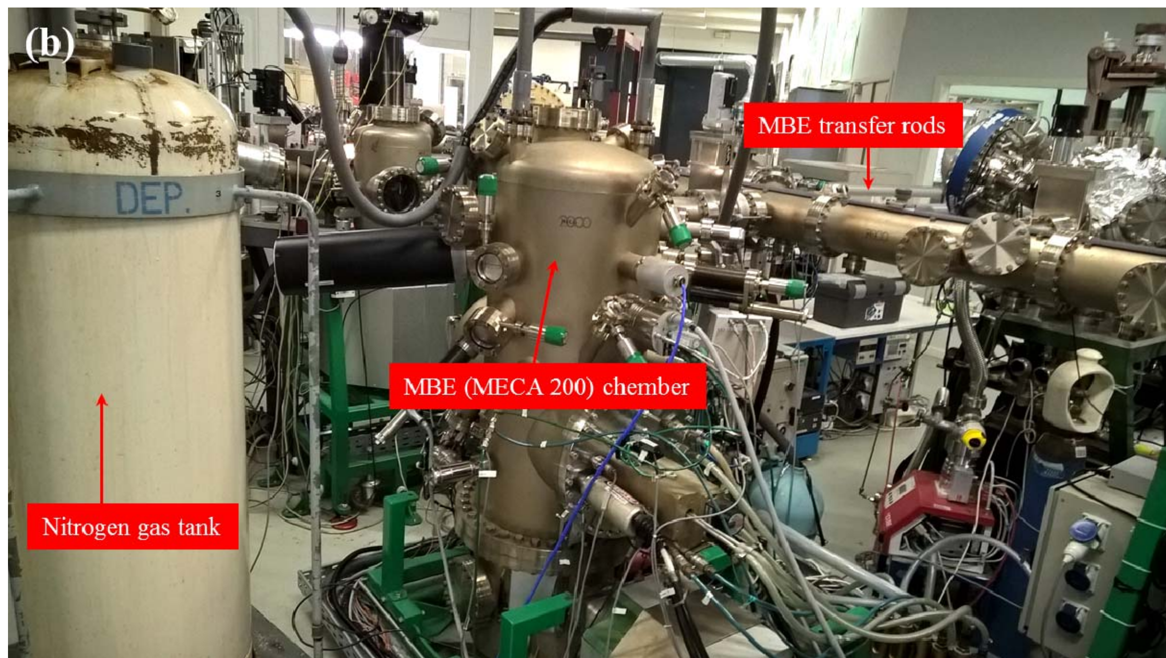


Figure 3.1: *(a) Sample mounting and transfer process, (b) image of MBE (MECA 2000)*

The train was designed to take up to nine sample holders. Once the train was in the load lock, the load lock was pumped to below 1.5 $x10^{-6}$ mbar before opening the valve to roll the train into the transport tube using the magnet and the valve was closed again. The train was rolled until it was opposite to the MBE chamber whereby the transfer rod, shown in **fig. 3.1 (b)**, was used to take the sample holders (with the cleaned substrate mounted), one at the time, into the MBE chamber which was at a pressure of $8x10^{-9}$ mbar. Once the deposition was done, the coated substrate was taken back into the train and another substrate moved into the chamber for another deposition without leaving the vacuum system. The deposition of Pt/Pd was monitored using a thin film thickness monitor, inficon XTM/2 deposition monitor, used to track the coating thicknesses. The rate at which the coatings were deposited was 0.1Å/s using 110 mA current for Pt and between 0.1-0.2 Å/s using 50 mA for Pd. To study the phase formation, the Pt and Pd coated substrates of approximately 1 cm × 1 cm, cut from the 5 cm diameter coated wafer, were analysed using *in-situ* real-time RBS. SEM was used to study the surface morphology of the annealed coatings. The structural information of the observed phase/s was analysed using room temperature and *in situ* XRD. The binding energies of the surface composition of the coated samples were analysed using Thermo Scientific (ESCALAB 250Xi model) X-ray Photoelectron Spectroscopy XPS. The experimental details of the characterization techniques are presented in **chapter 2**.

3.1.1 MBE coating deposition in the presence of silicon flux

The Pd and Pt coating deposited by MBE under Si flux were investigated using microscopic and X-ray diffraction techniques. In this case the deposition conditions were changed. After the deposition of either Pt or Pd (20 nm thick), the temperature of the coated system was ramped up to near the eutectic temperature (950 °C) in the presence of Si flux without breaking the vacuum chamber. This is the temperature where liquid transformation into two solid phases (PtSi+Si and

PdSi+Si) is expected. A focused ion beam-Scanning Electron Microscope (FIB-SEM), FEI Helios NANOLAB 650, was used to obtain the cross-section of the resulting silicide nanowires, from the 20 nm Pt/Pd coated p-type silicon (111) samples. The FIB-SEM comprised of the SEM system, equipped with the ion source that produces a beam of Ga^+ ions which was used to mill the selected sample. Prior the milling of the sample, a protective layer (carbon) was deposited on the surface using chemical vapour deposition within the FIB-SEM. For the milling process, the FIB-SEM instrument was operated at 30 kV and the milled section (sample cross-section) was attached into the omniprobe liftout needle and transferred onto a copper grid where final polishing was carried out to obtain a thinner sample of ~ 100 nm. This was done at 2kV using Ga^+ ions. The imaging and elemental composition (line scanning mode) of the nanowire cross-section were obtained using Transmission Electron Microscope (TEM), Joel JEM 2100F, operated in Scanning a Transmission Electron Microscopy (STEM) mode. The images were acquired at a 200 kV accelerating voltage. X-ray diffraction (XRD), at room temperature, was used for phase identification using a D8 Advance Bruker diffractometer.

3.2 Preparation of the Pt coating using an electron beam evaporator (EBE)

An electron beam evaporator was also used to prepare Pt coatings. In this case, a 20 nm thick Pt coating was deposited on four n-type Si (100) substrates (1 cm × 1 cm), at a vacuum pressure of 5 $x10^{-6}$ mbar and a deposition rate of 0.8 Å/s. The substrates were ultrasonically cleaned in a sequence of several solvents (methanol, acetone, trichloroethylene, acetone, methanol and de-ionized water) for the duration of 10 minutes for each step. As done with the MBE Pt deposited coatings for phase formation studies, an *in situ* real-time RBS experiment was conducted on the first coated sample, see **chapter 2** for the full experimental details. *In situ* real-time RBS spectra

were extracted at different temperatures (230 °C, 300 °C and 350 °C) and simulated using Rump software. For the formation of droplets, the second sample was annealed at 800 °C for 30 minutes, below the eutectic point (978 °C) using a STF 1200 series split tube furnace. Two other samples were used for nanowires growth investigation. The first was annealed at 1000 °C while flowing argon gas at a flow rate of 250 millilitres per minute (ml/m). In the second sample, Si was deposited using a PLD technique, **fig. 3.2**, with a 255 nm wavelength laser (Nd:YAG) at 800 °C. During the PLD experiments, the high-power laser beam was focused into the chamber which was at $6x10^{-6}$ mbar pressure as shown by the blue line. The substrates were mounted 7 cm away from the rotating Si target. The surface morphologies of all the samples were investigated using a JEOL JSM-7001F-SEM, in secondary electron mode and operated at 2 keV. Particle Induced X-ray Emission (PIXE) technique was used to map the elemental distribution, particularly Pt, on the surfaces of both the annealed (800 °C) and *in situ* real-time RBS analysed sample. PIXE and energy dispersive X-ray spectroscopy (EDX) techniques are complementary techniques and both are used for the determination of the elements present in the sample. However, with PIXE one can map the distribution of elements making up the sample, including trace elements.

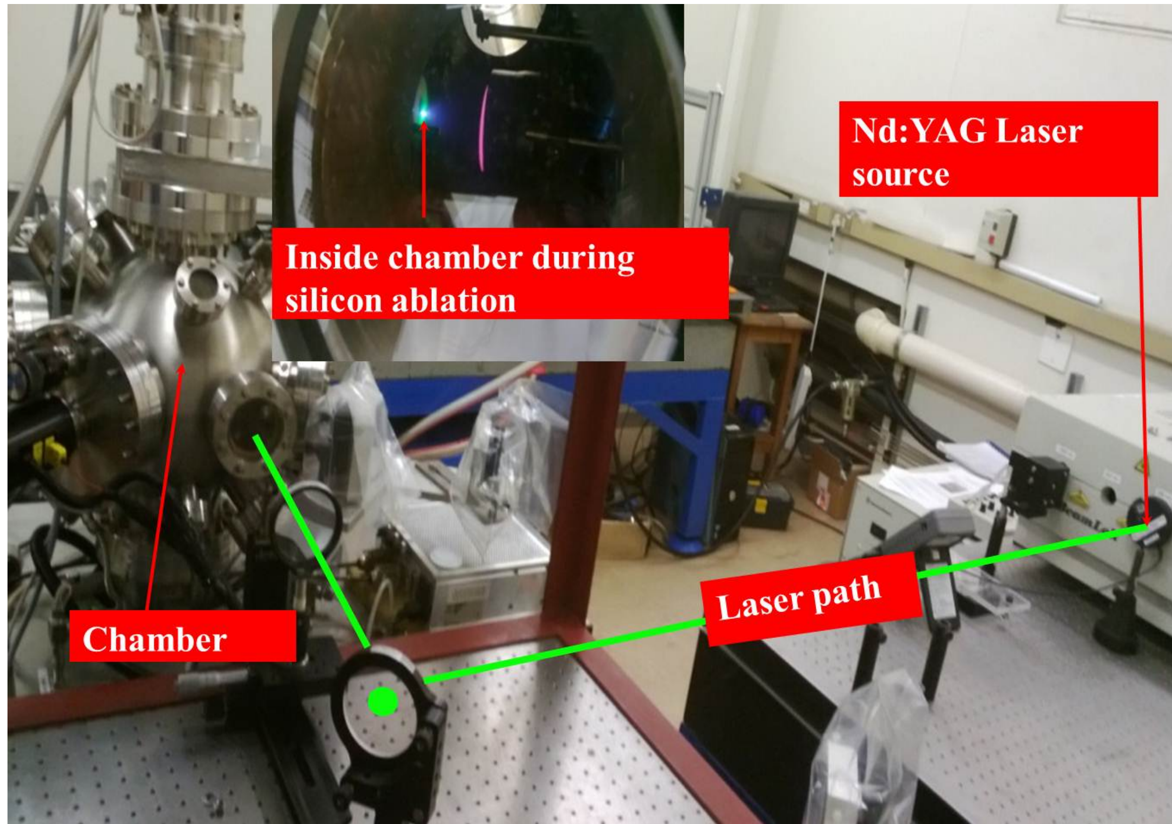


Figure 3.2: *PLD experimental setup, the ablation of silicon inside the PLD (insert image). The silicon vapour (plume) can be seen in blue expanding towards the substrate holder mounted on the heating stage (in red) to account for silicon nanowire growth*

3.3 Platinum and palladium catalysed silicon nanowire growth

For the growth of SiNWs catalysed by Pt and Pd, the deposited samples (by MBE or EBE) were subjected to annealing. The samples were annealed at 1000 °C in the gas flow in ml/m, using a STF 1200 series split tube furnace. The Pt/Pd coated Si samples (20 nm thick) were placed in a ceramic boat and transferred into the furnace for the annealing experiment. After heating the

samples at 1000 °C, analysis using SEM and TEM was performed and the results are presented in the result section, **chapter 4**.

3.3.1 Fabrication of platinum catalysed silicon nanowires based device

The Pt-catalysed SiNWs were synthesised through the SLS mechanism to which a core-shell structure (crystalline-amorphous) was obtained. The electrical properties of this core-shell SiNWs were investigated. The device was fabricated on a Si oxide substrate of about 300 nm SiO_2 layer, with different pre-prepared device electrodes, using electron beam lithography as schematically shown in **fig. 3.3**.

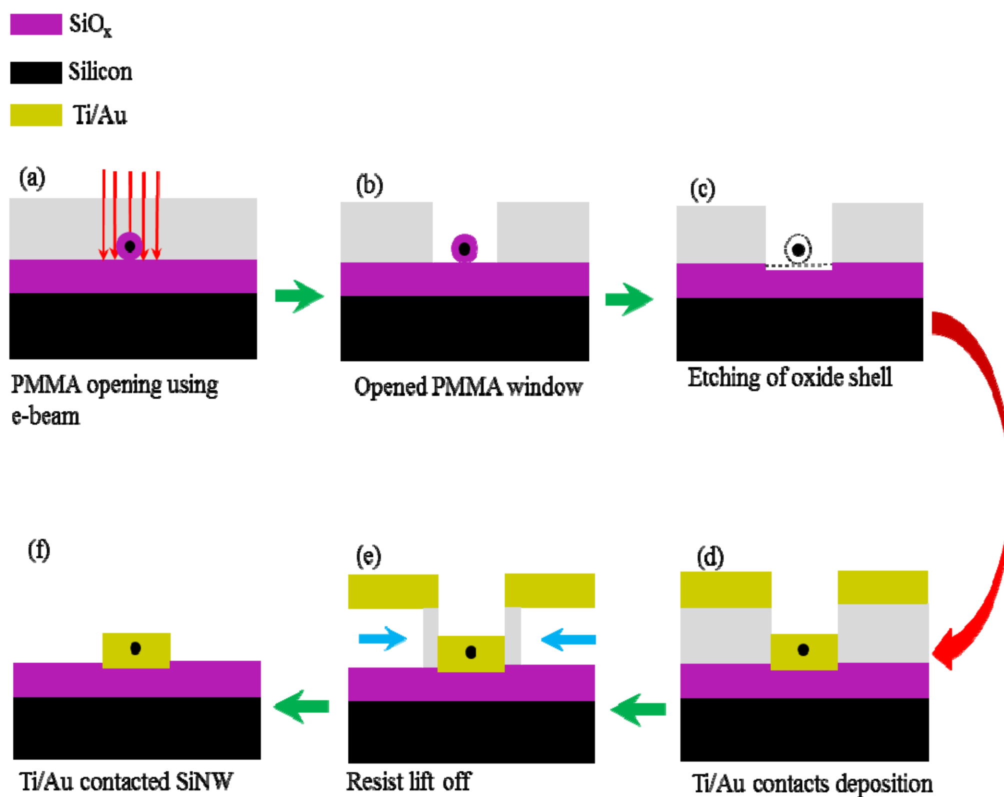


Figure 3.3: *Schematic representation of electron lithography preparation of the Pt-catalysed silicon nanowire based device.*

The prepared device electrodes were given a unique number (nanowire alignment marks) to distinguish them from one another, **fig. 3.4**. The lithography process was performed using a JEOL JSM-6460 SEM with NANOMAKER lithography extension.

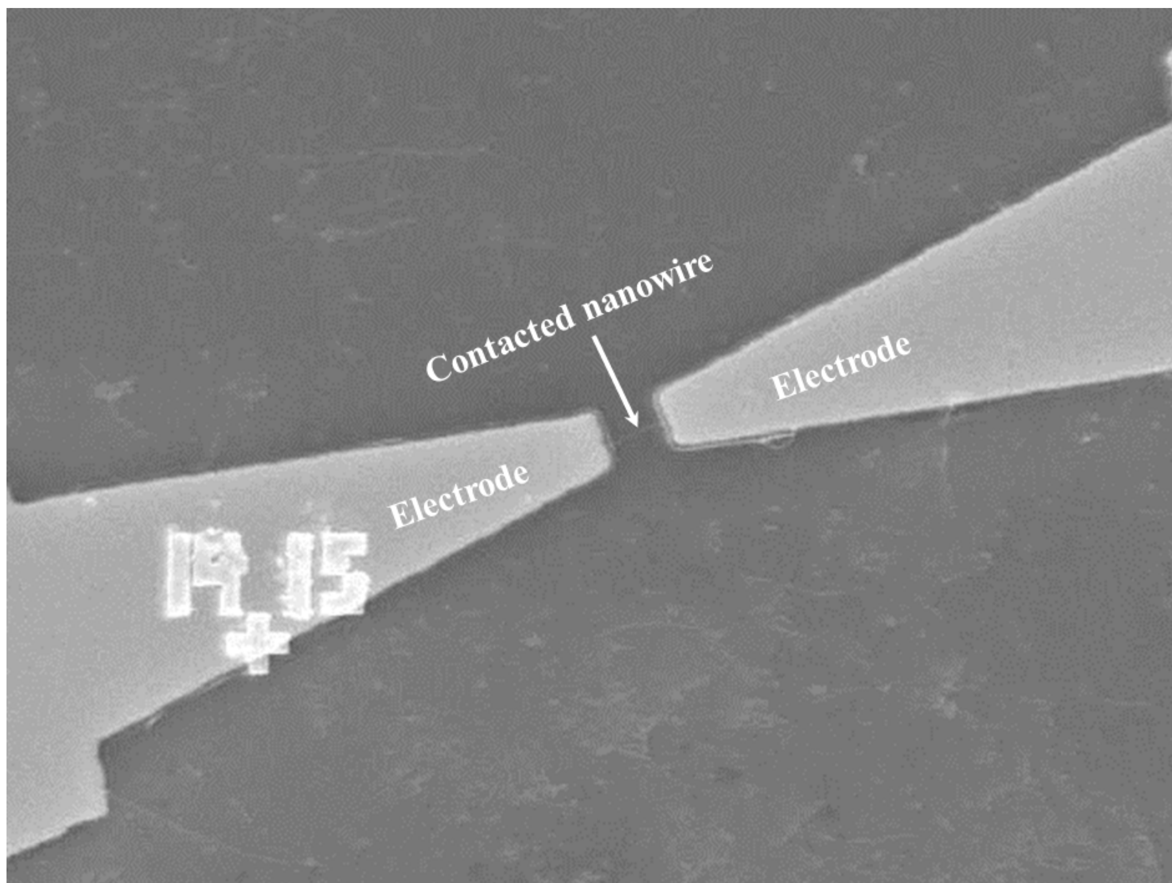


Figure 3.4: *Silicon oxide substrate (about 300 nm SiO_2 layer) showing a nanowire alignment mark*

The nanowires were drop-casted onto the oxide substrate and allowed to dry. The dry substrate was then visually inspected using an optical microscope (up to x1500) to select and register the suitable nanowires for device fabrication. The fabrication process included utilising Microchem PMMA 950K electron resist and (PMMA/MAA) copolymer, **fig. 3.3 (a)**. The two layered resist, comprises of copolymer as a bottom layer and PMMA as an upper layer, was prepared to obtain a necessary undercut for better lift-off. The thickness of the resist was made to be approximately twice as the thickness of the deposited metal film. The PMMA coated substrate was taken back into the SEM where the registered marks were located and the contacts were prepared. Using the CAD module of the lithography system, the alignment of the electron beam lithography on the SiNW to open the window for the metal contacting was performed, **fig. 3.3 (b)**. Due to the core-shell structure of the nanowire, the oxide shell had to be etched using hydrofluoric acid, **fig. 3.3 (c)**. The contact films, Titanium (10 nm) and Gold (370 nm) (Ti/Au), were prepared, **fig. 3.3 (d)**, using the Von Ardenne Anlagentchnik LS 730 S magnetron sputtering plant. **Fig. 3.3 (e)** shows the PMMA lift off stage which was done using dymethylformamide. The current-voltage relationship of a number of SiNWs was then measured.

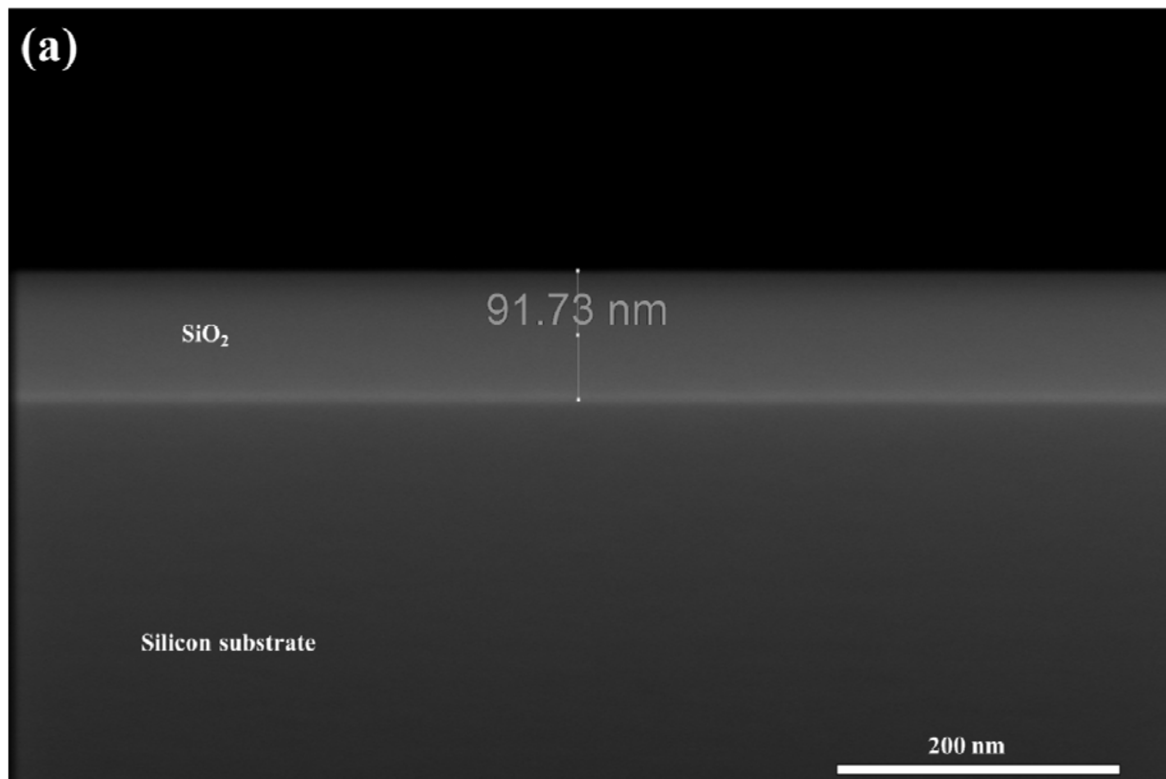
3.3.2 Fabrication of palladium catalysed silicon nanowires based device

Similar to the Pt-catalysed SiNWs, a core-shell structure was observed for the Pd catalyst. However, in this case, reduction in the oxidation of the nanowires was implemented, resulting in the formation of Oxide-reduced (OR) SiNWs. For the growth of these OR SiNWs, the MBE system, **fig. 3.1**, was used to deposit a Pd catalyst layer onto a n-type Si (100) substrate. Prior to the deposition, the Si substrate was cleaned using a RCA cleaning procedure described in **section 3.1**. The Pd-coated Si wafer was cut into samples of approximately 1 cm × 1 cm. Some samples

were further coated with carbon using an AJA magnetron sputter system at a pressure of $4x10^{-3}$ mbar, with the aim to reduce the oxidation of the SiNWs during growth. The SiNWs were grown at 1000 °C using an STF 1200 series split tube furnace under a mixture of argon (300 ml/m) and methane (10 ml/m) gas. Using the secondary electron mode of a FEG-SEM operated at an accelerating voltage of 5 kV, micrographs of the annealed samples were acquired. The structural properties of the SiNWs were then investigated using HRTEM (FEI Tecnai G2 F20 X-Twin), **fig. 2.6**. Furthermore, the electrical properties of these OR-SiNWs were investigated. The OR-SiNWs based device was fabricated using focused ion beam techniques (FEB/FIB). A FEI Helios NanoLab 600i instrument, **fig. 3.5**, was used.

Figure 3.5: *FEB/FIB instrument: FEI Helios NanoLab 600i*

The OR-SiNWs were transferred to an oxidised Si substrate, **fig. 3.6 (a)**, with a 92 nm thick oxide layer by gently pressing the oxidised substrate onto the Si substrate containing the ethanol-SiNWs solution.



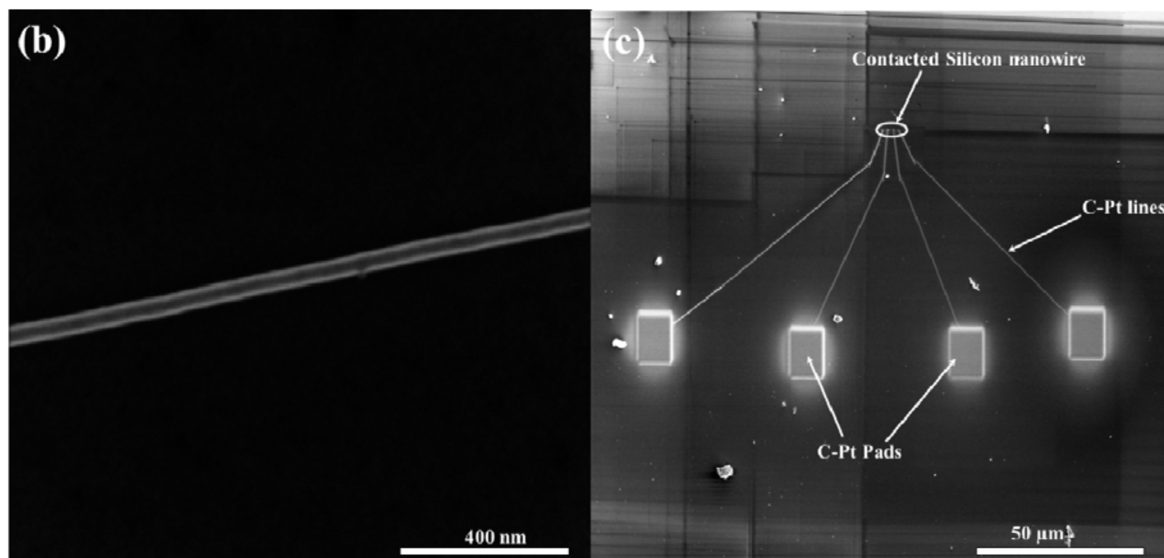
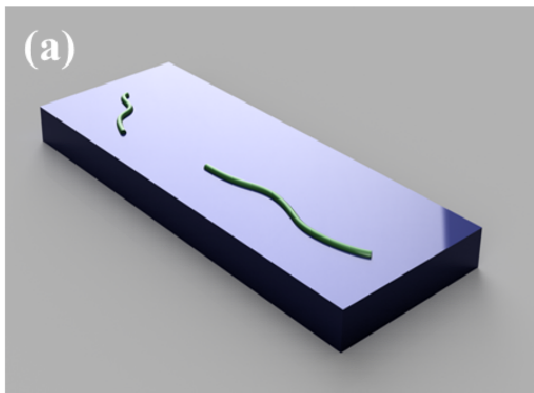


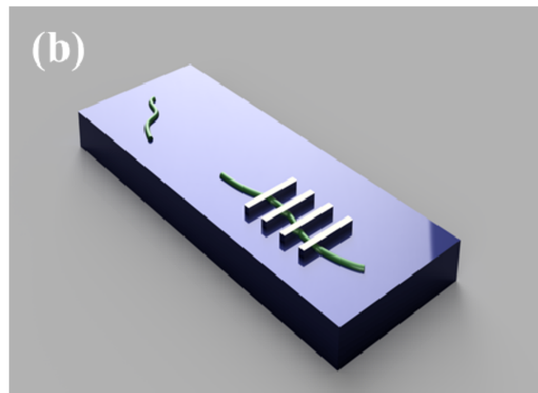
Figure 3.6: *Silicon nanowire device fabrication: (a) Oxidised silicon substrate cross-section showing a 92 nm SiO_2 layer (b) isolated Pd catalysed crystalline core-amorphous shell silicon nanowire (c) FEB/FIB prepared silicon nanowire device*

The isolated core-shell nanowires, i.e. **fig. 3.6 (b)**, were identified using FIB-SEM followed by nanowire contacting, **fig. 3.6 (c)**, using a methylcyclopentadienyl (trimethyl) Pt ($C_9H_{16}Pt$) precursor. It should be mentioned that, in the FIB based technique one can use an electron beam or Ga^+ beam for the deposition of the contacts lines or contact pads, **fig. 3.6 (c)**. **Fig. 3.7** shows 3D rendered images depicting the fabrication process of SiNW devices prepared in this section. After the transfer of the nanowire into the oxidised Si substrate, the isolated wires were identified and carbon incorporated Pt (c-Pt) contact lines of about 300 nm in width and several tens of micrometres in length were prepared, as detailed in **fig. 3.7 (b)**. These contacts were prepared using focused electron beam (FEB) assisted deposition at 3 kV and 5.5 nA. Two reasons lead to the use of an electron beam for the Pt (+carbon) deposition instead of the ion beam; firstly Ga contamination to the nanowires from the Ga^+ ion beam had to be avoided, and secondly a halo of unwanted Pt (+carbon) deposition in the surrounding of the desired patterning fields can be heavily reduced. At the end of each contact line, contact pads were prepared. It has to be emphasized that long contact lines were used to enable contact pad deposition without irradiating the nanowire itself by the Ga-beam. During pad preparation, the nanowire was not in the field of view. The pads consist of a first layer of electron beam deposited c-Pt (500 nm thick), **fig. 3.7 (c)**, which served as a protective layer for the Si oxide layer to shield against the Ga+ beam during the c-Pt deposition. The final step of the preparation involved the deposition of a thick layer of c-Pt, at 30 kV and 0.43 nA, using the Ga-beam, **fig. 3.7 (d)**. The size of the final contact pad structures was 10 µm x 10 µm and 3.5 µm in height. It should be noted that, the SiNWs were contacted without first removing the oxide shell, potentially resulting in a high contact resistance. However, it was reported in the literature that the EB-deposited Pt incorporates up to 70 % carbon **[96]** into the contact structure. In addition, the carbon content in the Si oxide layer

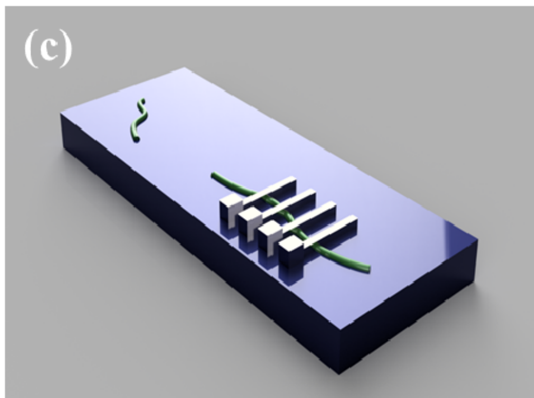
has been found to decrease the resistivity of the oxide by orders of magnitude as measured by Faraby *et al* **[97]**. Therefore, carbon from c-Pt creates a Si-C bond which then replaces a Si-O bond in the oxide layer thereby creating a path for electrons to flow.



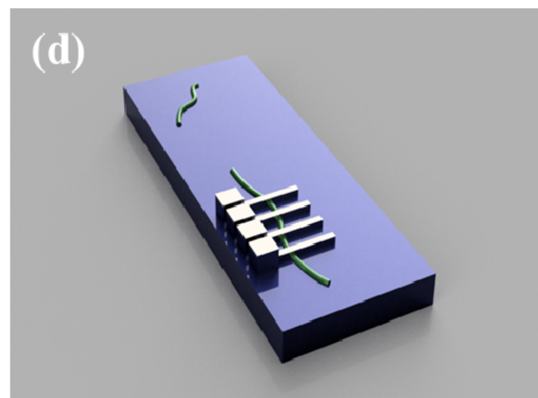
Silicon nanowires are first drop casted onto an oxidised silicon wafer



EB platinum contacts 300nm thick deposited using an e-beam at 3 kV and 5.5 nA.



First layer of EB platinum contact pads 500nm thick deposited using an e-beam at 3 kV and 5.5 nA.



EB platinum contacts 3000nm thick are deposited using a Ga^{+} beam e-beam at 30 kV and 0.43 nA.

Figure 3.7: *(Not to scale) 3D rendered images depicting the fabrication of a silicon nanowire device, using focused ion/electron beam (FIB/FEB), for electrical measurements: (a) silicon nanowires on the SiO_2 substrate (b) FEB-deposited platinum contact lines, (c) EB-deposited platinum contact pads and (d) FIB-deposited platinum contact pads.*

Four-point and two-point probe electrical measurements were performed on the fabricated nano-devices at room temperature. Metal probes (1 µm in diameter) were contacted onto the Pt pad structures using a semi-automatic wafer prober-semiconductor device analyser (Agilent B1500A Semiconductor Device Analyser, Süss PM5), **fig. 3.8**. Prior to the electrical measurements, the average (mean) thickness (diameter) of the tested nanowires were estimated using imageJ software by selecting 5 or 6 areas along the shell/core, hence the standard deviation as well as the uncertainty were obtained.

Figure 3.8: *Semi-automatic wafer prober-Semiconductor device analyser*

Furthermore, the calibration uncertainties of the SMU's (which was in the order of -100 fA) were found to not contribute much to the measured current values. To remove random statistical error the test on the same nanowire was repeated, in the same configuration. To determine if there was any current through the substrate leading to false conductivity measurements, a reference sample, **fig. 3.9**, with no nanowire was measured. The recorded current in this reference sample was compared to the current recorded for the SiNW incorporated device at the same applied voltage.

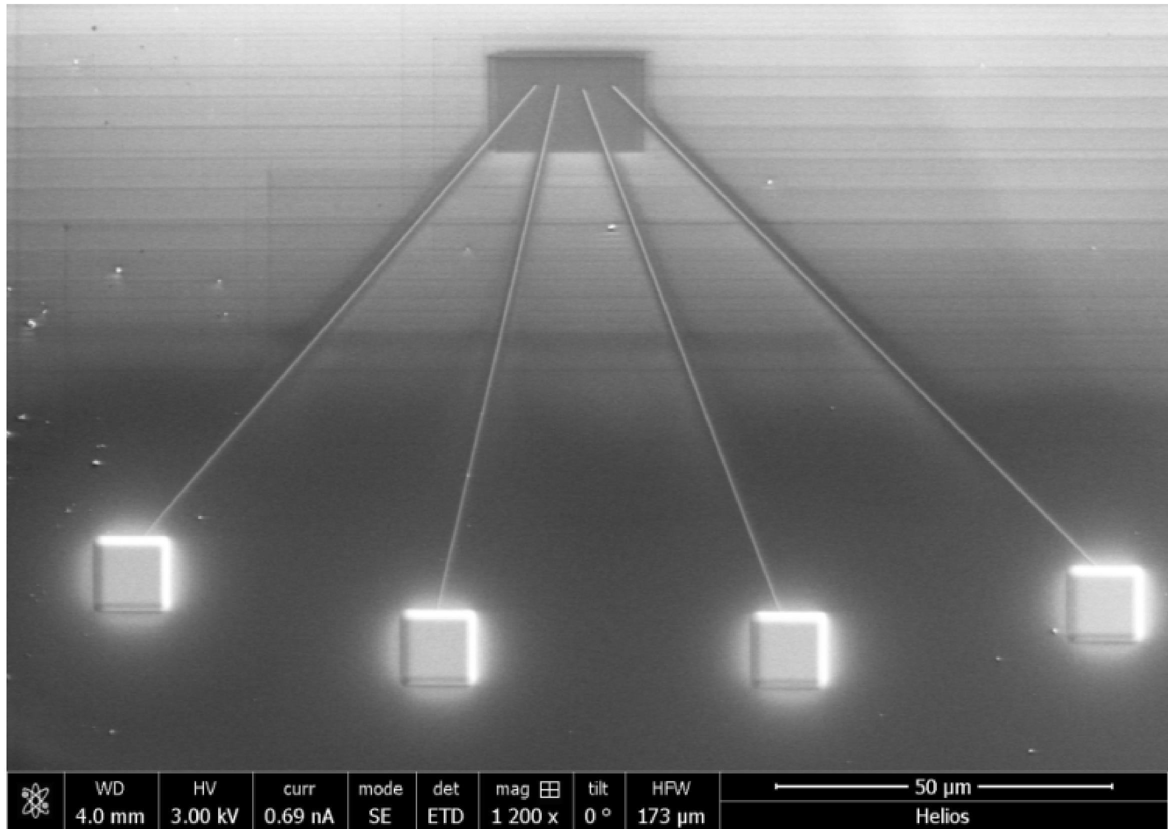


Figure 3.9: *Reference sample showing the device structure without a SiNW.*

CHAPTER 4 RESULTS

This chapter first presents a comprehensive investigation of the reaction between Pt and Si as a function of the annealing temperature and time. Two deposition techniques (MBE and EBE) were employed for the Pt coating depositions. Regarding the MBE deposition, the effect of annealing samples inside the MBE chamber without breaking the vacuum was also investigated. The idea is to propose a simple method to synthesis PtSi nanostructures using MBE, to fabricate (1) a nano-template of self-arranged PtSi nanoclusters which can subsequently be used as a seed for the growth of ordered SiNWs and (2) self-aligned PtSi nanowire arrays for future use in photodetector fabrication. The reaction between Pt and Si leads to the formation of Pt silicide seeds that initiate the growth of SiNWs, therefore the use of Pt silicide seeds for the growth of SiNWs is presented. In the second part of the results section for Pd, similar approaches were used with however only the MBE deposited Pd coatings.

4.1 Platinum silicide formation on MBE deposited samples

Three Si wafers, cleaned using the RCA procedure (see **section 3.1**), two p-type (111) and two n-type (100) 5 cm in diameter and 1-10 ohm.cm resistivity, were used as substrates in this investigation. The clean wafers were immediately loaded into the load lock chamber by means of the sample holder transfer train which was then pumped to below 1.5 x10^{-6} mbar. The MBE chamber vacuum was kept at 8x10^{-9} mbar during deposition. The first two substrates (one p-type (111) and one n-type (100)) were coated with a 20 nm thick Pt film at room temperature. The other two substrates, also p-type (111) and n-type (100), were also coated with a 20 nm Pt film at room temperature followed by annealing at 950 °C in the presence of Si flux within the MBE chamber. The Si deposition was done for two hours at 0.4-0.5 Å/s with a total of a 290 nm thick

Si layer recorded by the inficon XTM/2 deposition monitor. For the investigation of the reaction kinetics of Pt and Si, the first coated wafers (in as-deposited conditions) were cut into small samples of approximately 1 cm × 1 cm and analysed using *in situ* real-time RBS. **Fig. 4.1 (a)** shows the contour map of the *in situ* real-time RBS spectra of the MBE deposited Pt on p-type Si (111) substrate, collected continuously during the heating process from room temperature to 600 °C, at 2 °C/min ramping rate. The results of the spectra simulation, compound composition determination, are plotted in **fig. 4.1 (b)**. Similar results were observed on the n-type coated Si (100) substrate. The spectra were summed up into appropriate time intervals followed by the simulation of the individual spectrum, using Rump software. The simulation of the spectra from room temperature up to around 190 °C required a single layer with pure Pt which is attributed to the film being thermally stable in this temperature range. This is shown in red on the contour map. However, above 190 °C a second layer was used consisting of a Pt_2Si phase (67 *at.*% Pt and 33 *at.*% Si composition) with varying thickness as the annealing temperature increases, to about 240 °C, **figs. 4.1 (a-b)**. This is an indication of the reaction between Si and Pt, marked as Pt_2Si growth from Pt in the contour map, resulting in the broadening (represented by a shoulder in the contour map) as well as a decrease in the yield (shown by the disappearance of the red colour region in the contour map) of the Pt signal. After the complete growth of the phase from pure Pt, the Pt_2Si phase was found to be stable up to 270 °C, see **figs. 4.1 (a-b)**, for about 15 minutes before transforming to the second phase (PtSi silicide). Above this temperature (~ 290 °C) the second shoulder, marked in the contour map as PtSi growth from Pt_2Si, was observed. This growth is noticed by the colour change in the contour map as the yield of the Pt signal decreases. It can be confirmed therefore that when Pt has fully converted to the Pt_2Si silicide, an additional temperature of 30 °C is needed for the nucleation of the second silicide (PtSi). Similar

observations were presented by Abbes *et al.* **[98]** reporting a temperature delay of about 50 °C having started with a 50 nm thick Pt layer.

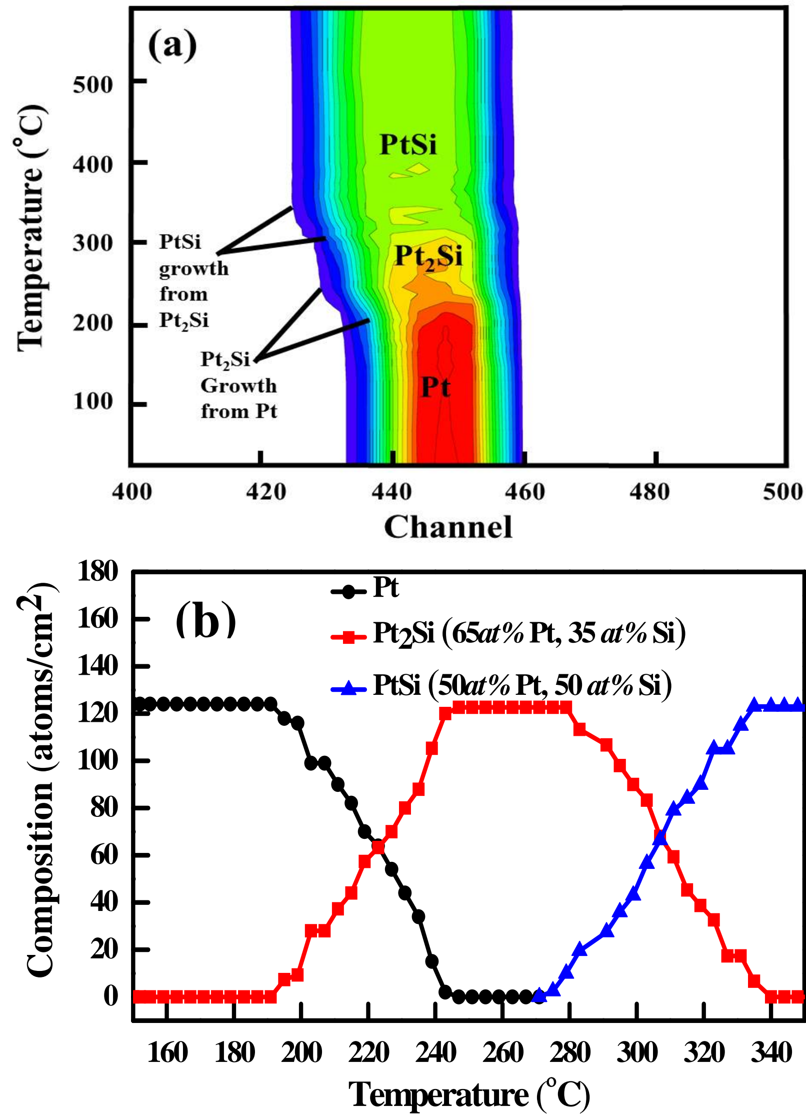


Figure 4.1: *Formation of the Pt silicide on the Si substrate, (a) In situ real-time RBS contour map illustrating the sample composition during the reaction of platinum and silicon from room temperature to 600°C. (b) Formation of silicides and their thermal stability as a function of the annealing temperature. Red colour in the contour map shows the intensity of Pt signal which disappears during reaction with Si*

Therefore, our results confirm that Pt_2Si is stable for only a short period of time (15 minutes) at a constant ramping rate of 2°C/min. However, annealing at a fixed temperature between 200 °C and 250 °C may prolong the stability of the Pt_2Si phase **[98]**. The growth of the second phase (PtSi) reached completion at 340 °C and is a stable phase of the system. These observations were followed by the analyses of the system using XPS and the results are presented in **fig. 4.2**. The analysed sample (1 cm × 1 cm) was cut from the same 20 nm Pt coated wafer (5 cm in diameter). The spectra for the Pt4f binding energy were recorded at selected temperatures based on the *in situ* real-time RBS results. The binding energy of the Pt4f7 level for the metallic Pt can be observed at 71.4 eV, marked by the dotted line (1), for the spectrum recorded at room temperature. However, as the temperature was increased to 200 °C a split in the Pt4f7 peak into two binding energies (71.4 eV and 72.5 eV, marked by the dotted line (1) and (2), respectively, was observed. This is an indication of the metallic Pt reacting with Si to form Pt_2Si (72.5 eV). The spectrum recorded at 230 °C confirmed the existence of only the Pt_2Si phase with the shift in binding energy of 1.1 eV, from 71.4 eV (metallic Pt) to 72.5 eV. With more Si atoms diffusing onto the surface, the broadening of the Pt_2Si phase peak, from 72.5 eV to 73 eV-dotted line (3), was observed as shown by the spectrum recorded at 270 °C. This was attributed to the formation of the PtSi silicide phase growing from the Pt_2Si at this temperature, which is in good agreement with the *in situ* real-time RBS, in **figs. 4.1 (a-b)**. The spectrum recorded at 320 °C showed a shift (0.5 eV) in binding energy indicating the presence of only the PtSi phase and this was also the case for temperatures above 320 °C, i.e. 370 °C, 420 °C and 470 °C, which proves the stability of this phase at high temperatures.

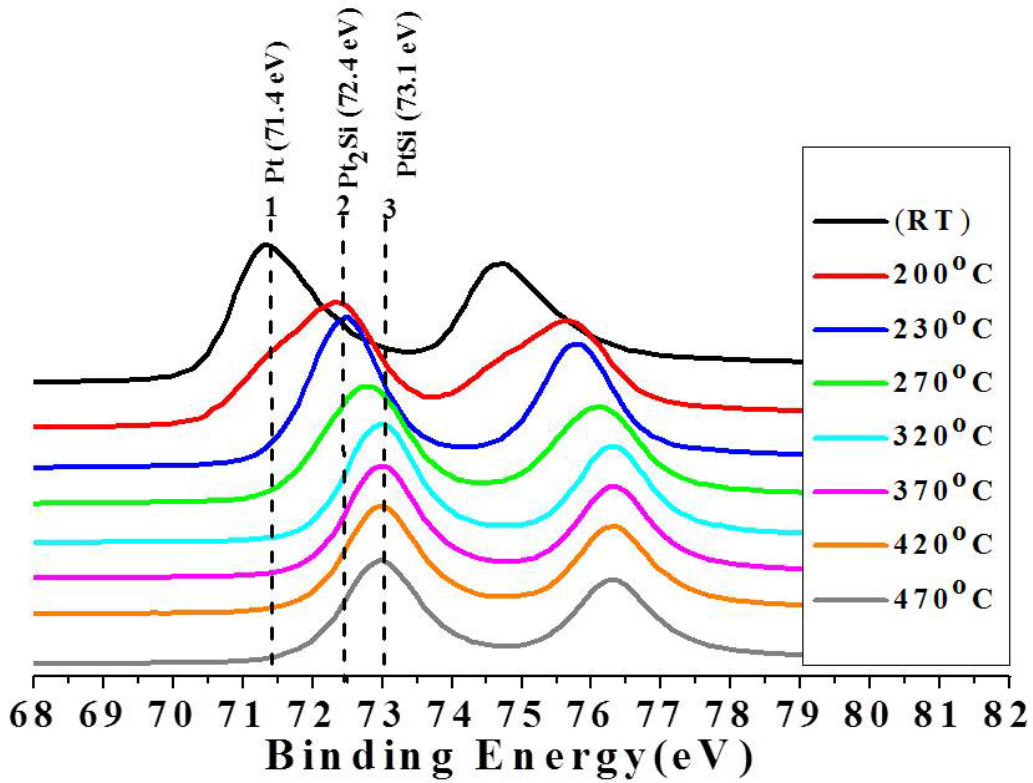
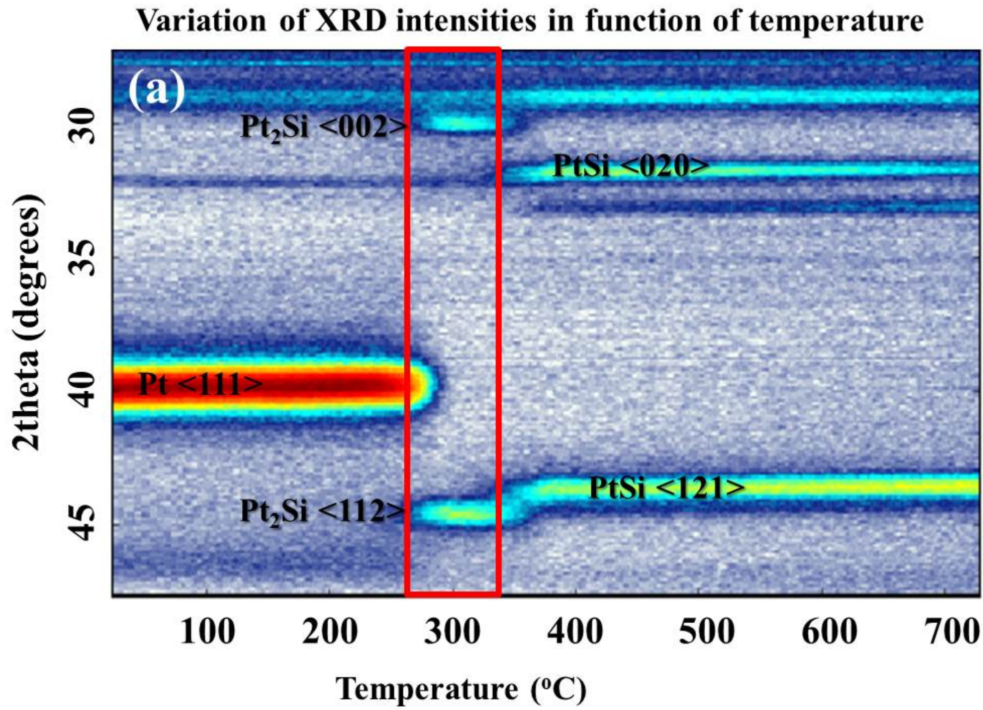


Figure 4.2: *XPS results of Pt coated system showing the binding energies of pure Pt4f spectra recorded at different temperatures*

To complement the *in situ* RBS and XPS results, *in situ* XRD was used to investigate the structural information of the silicides while annealing from room temperature at a ramping rate of 30°C/min, **fig. 4.3**. The colours in the contour plot show the intensity of the diffracted peak. **Fig. 4.3 (b)** shows the side view of the diffraction spectra from the region shown by the red rectangular box in **fig. 4.3 (a)**, about 245 °C to 315 °C temperature range.



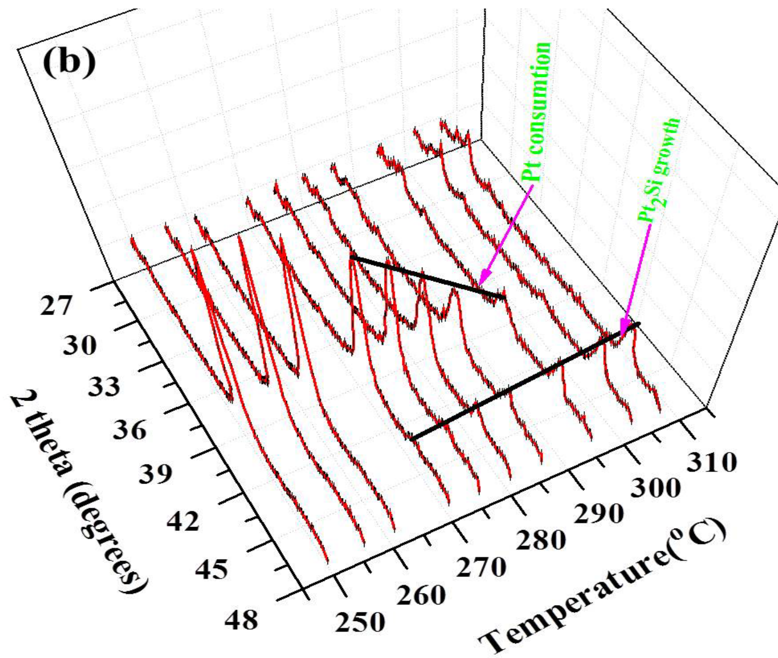


Figure 4.3: *In situ XRD (a) Contour map showing the formation of platinum silicide as a function of temperature (b) Side view of the in situ XRD data showing phase formation from the region shown by the red rectangular box.*

The *in situ* XRD spectra were collected between 27° (2θ) and 47° (2θ) using a D8 Discover Bruker diffractometer, in a Helium gas flow of 200 ml/m. The data was analysed using the XRD database, international centre for diffraction data (ICDD) 1998 to identify/confirm the phases present at different temperatures. The main diffraction peak is found at 40° (2θ), matching the <111> plane orientation of the face centred cubic Pt, with unit cell parameters a = b = c =3.92310 Å (file number 00-004-0802), **figs. 4.3 (a-b)**. Pt-rich body centred tetragonal (Pt_2Si) phase, with unit cell parameters (a = b = 3.933 Å and c = 5.910 Å: file number 00-017-0683), was observed to form around 270 °C. Two diffraction peaks at about 2θ = 30° <002> and 45° <112> are assigned to the Pt_2Si phase, using the XRD database. The phase was observed to be growing at the expense of the Pt layer as evident in **figs. 4.3 (a-b)** with the disappearance of the Pt peak as the Pt_2Si peaks grows. The growing Pt_2Si phase reached completion at 300 °C and was stable up to 330 °C before transforming to the second phase, **fig. 4.3 (a)**. The new XRD diffraction peaks matches those of the PtSi phase, identified as an orthorhombic crystal structure with unit cell parameters a = 5.938 Å, b = 5.59600 Å and c = 3.60350 Å, file number 00-007-0251. Two diffraction peaks at 2θ = 31.984° <020> and 43.583° <121> are assigned to it (PtSi), also shown in **fig. 4.3 (a)**. **Table 4.1**, summarises the Pt silicide phase formation using *in situ* XRD, *in situ* real-time RBS and XPS. Noticeable differences between *in situ* real-time RBS and *in situ* XRD were evident in the phase formation temperatures as well as the duration of the stability of the Pt_2Si phase. In the *in situ* XRD, the formation of the two silicides (Pt_2Si and PtSi) was observed at 70 °C higher. In addition, the Pt_2Si phase was stable for only 1 minute, contrary to the 15 minute in the *in situ* real-time RBS results. The observed differences were attributed to the temperature ramping rate used during the experiments, 2 °C/min and 30 °C/min for the *in situ* real-time RBS and *in situ* XRD, respectively. Both results however confirm that when Pt has

fully converted to the Pt_2Si silicide, in a non-isothermal annealing approach, an additional temperature (30 °C) is needed for the nucleation of the second silicide (PtSi) to begin. This PtSi nucleation barrier (delay) has been attributed to the strain relaxation in the Pt_2Si silicide phases **[98]**.

Table 4.1. *In situ real-time RBS, in situ XRD and XPS phase identification for ~20 nm platinum-coated silicon sample deposited using MBE*

Temperature (°C)	In situ RBS (phase/s)	XPS (phase/s)	In situ XRD (phase/s)
RT	Pt	Pt	Pt
200 °C	Pt+Pt_2Si	Pt+Pt_2Si	Pt
230 °C	Pt+Pt_2Si	Pt_2Si	Pt
240 °C	Pt_2Si	-	Pt
250 °C	Pt_2Si	-	Pt
260 °C	Pt_2Si	-	Pt
270 °C	Pt_2Si+PtSi	Pt_2Si+PtSi	Pt+Pt_2Si
285°C	Pt_2Si+PtSi	-	Pt+Pt_2Si
310 °C	Pt_2Si+PtSi	-	Pt_2Si
320 °C	Pt_2Si+PtSi	PtSi	Pt_2Si
320 °C	Pt_2Si+PtSi	-	Pt_2Si
340 °C	PtSi	-	Pt_2Si+PtSi
360 °C	PtSi	-	PtSi
370 °C	PtSi	PtSi	PtSi
420 °C	PtSi	PtSi	PtSi

4.1.1 Self-aligned platinum silicide nanowires and nanoclusters

The post-MBE deposition investigation using *in situ* real-time RBS, *in situ* XRD and XPS confirmed the formation of a stable single PtSi silicide phase during the Pt and Si reaction from 340°C, **figs. 4.1** to **4.3**. Therefore, the other deposited samples (20 nm Pt-coated Si (100) and (111)) were annealed (950 °C) inside the MBE to investigate the effect of annealing inside the MBE chamber with added Si flux. The annealing temperature used was chosen based on the eutectic temperature for the Pt-Si binary system, which is around 978 °C **[14]**. At around this temperature (978 °C), the PtSi phase (in the bulk system) is in the liquid form, with 67 at.% Si. It has been found that, the addition of Si into the PtSi droplets results in the formation of molten PtSi droplets at temperatures lower than the melting temperature of Pt **[99-100]**. **Figs. 4.4 (a)** and **(b-d)** shows SEM micrographs of Pt-coated Si <100> and (111), respectively, after annealing at 950 °C inside the MBE chamber.

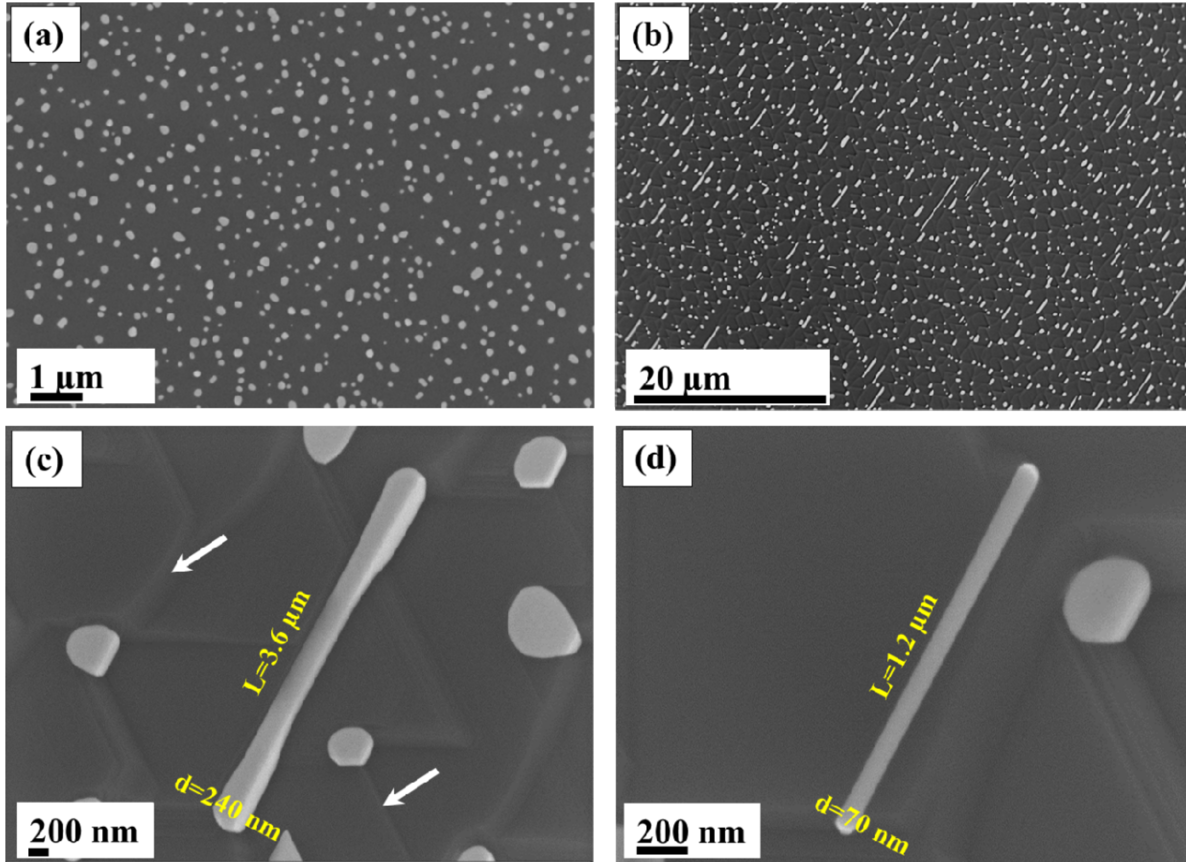


Figure 4.4: *Imaging of the PtSi silicide after annealing at 950°C for 2 hours. (a) PtSi silicide nano-droplets on silicon <100> substrate, (b) self-aligned PtSi silicide nanoclusters and nanowires on silicon<111> substrate. (c-d) Enlarged areas of image (b) showing different shapes of the PtSi silicide*

Randomly arranged spherical shaped PtSi silicide nanoclusters, with diameters ranging from 70 nm to 200 nm, were observed on the smooth surface of the silicon (100) substrate, **fig. 4.4 (a)**. However, the micrographs of the Pt -coated silicon (111) substrate, **figs. 4.4 (b-d)**, annealed under the same conditions, showed the formation of self-arranged PtSi nanoclusters and

nanowires. The nanowires are rectangular (faceted) and cylindrical in shape, **figs. 4.4 (c)** and **(d)**, respectively. They have a width ranging from 70 nm to 300 nm while their length ranged from 1 μm to 15 μm. It appears that the self-assembly of these nanostructures is influenced by the surface of the Si (111) substrate which shows evidence of straight and wavelike steps, indicated by the white arrows in **fig. 4.4 (c)**. The growth mechanism of these self-aligned nanostructures appears to be a combination of a two-step process: (1) surface thermomigration of the PtSi nano-droplets across the Si substrate at high temperatures **[99-100]** and (2) homoepitaxial growth of the Si on Si (111) substrate, creating the straight and wavelike steps **[101-102]**. The growth mechanism is schematically shown in **fig. 4.5**. As the temperature increases from 340 °C, after the formation of the PtSi monosilicide phase as discussed in **figs. 4.1** and **4.3**, the stable silicide phase layer starts to transform into droplets which migrate across the Si surface. The moving PtSi droplets reveal the Si substrate, **fig. 4.5 (c)**. Incorporating Si into the annealed sample, **fig. 4.5 (d)**, results in the homoepitaxial growth of Si on the Si (111) substrate that creates two Si surface steps. The steps govern the shape and location of the nanostructures, **fig. 4.5 (e)**. On the straight steps, nanoclusters combine and grow into straight nanowires, **fig. 4.5 (d)**, in what can be referred to as a step guided Ostwald ripening of Si on Pt-Si nanoclusters. The wavelike steps are reported to be stable at temperatures below 900 °C but start to transform into straight steps at about 950 °C **[101-102]**. The migration of the nanostructures already starts at a temperature of 900 °C, with a reported speed of 0.1 μm/second **[100]**.

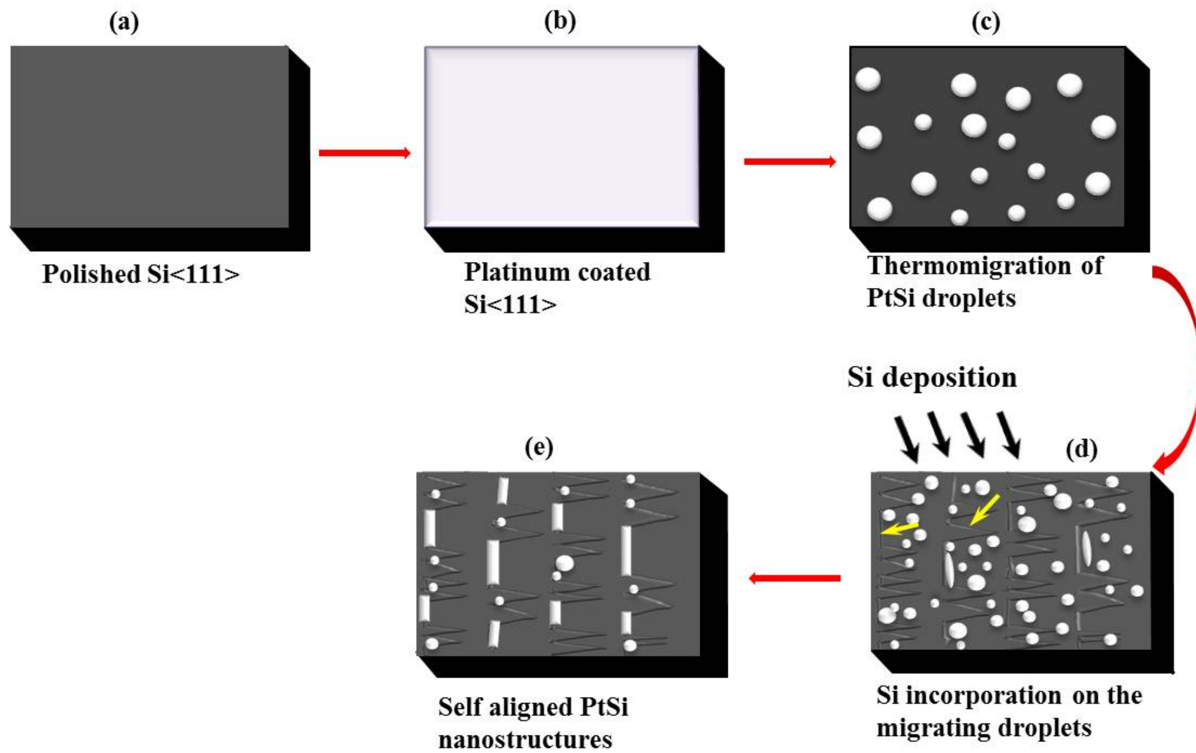


Figure 4.5: *The mechanism of the self-aligned PtSi silicide nanostructures. (a) Si (111) substrate, (b) Platinum coated silicon (111) substrate using MBE, (c) PtSi thermomigration at high temperature, (d) silicon incorporation into the moving droplets and formation of silicon steps and (e) Self aligned PtSi nanostructures.*

It is expected that annealing at higher temperatures (> 950 °C), would not only increase the migration speed of the droplets but also create more straight steps in the Si substrate to guide the moving droplets into PtSi nanowires. X-ray diffraction (XRD) analysis of the sample annealed at 950 °C confirmed the presence of only the orthorhombic PtSi silicide phase, **fig. 4.6**.

Diffraction peaks matching this phase are indicated by the green stars while only two peaks from the silicon substrate were observed and are indicated by the red dot. The JEOL JSM-7001F-SEM used to acquire the images of the annealed samples was equipped with energy dispersive X-ray spectroscopy (EDX) which allowed for the analysis of the elements of the samples, **fig. 4.7**.

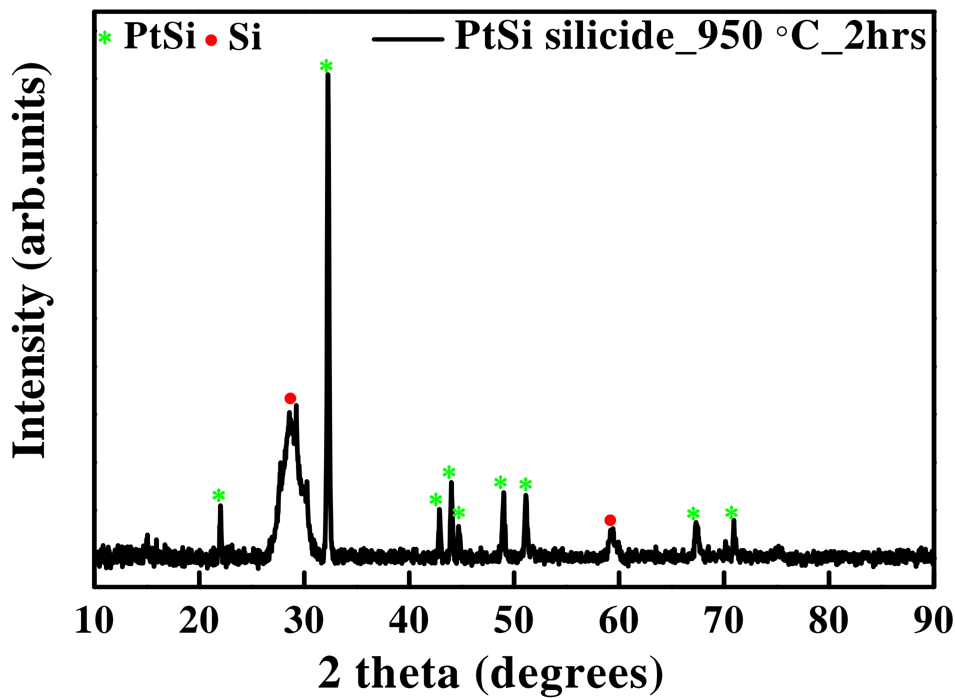


Figure 4.6: *XRD analysis of the sample with PtSi silicide nanostructures*

It was found that, the distribution of Pt along the nanowires was not homogeneous with higher concentration on the edges of the nanowires as compared to the middle. This was due to the diameter of the nanowire being thinner in the middle than on the edges, hence more Si contribution from the substrate according to the depth of the electron penetration, **eq. 4.1 [92]**, in the PtSi silicide absorber. The depth of electron (20 keV) penetration in Si is approximately 3

μm while in PtSi silicide is 0.55 μm, therefore with the diameter of these PtSi silicide nanowires in the range of 70 nm to 100 nm, more penetration into the Si substrate is expected which explains the observed increased Si counts (6800) as compared to the Pt counts (200) in the two selected nanowires, **figs. 4.7(a-b)**. With more counts from the Si substrate, the compositional analysis could not be used to relate the stoichiometry of the silicide phase identified in this sample using XRD. Therefore the contribution of the substrate was eliminated by performing compositional analysis across the cross-section of the selected nanostructure, **figs. 4.8 (a-b)**.

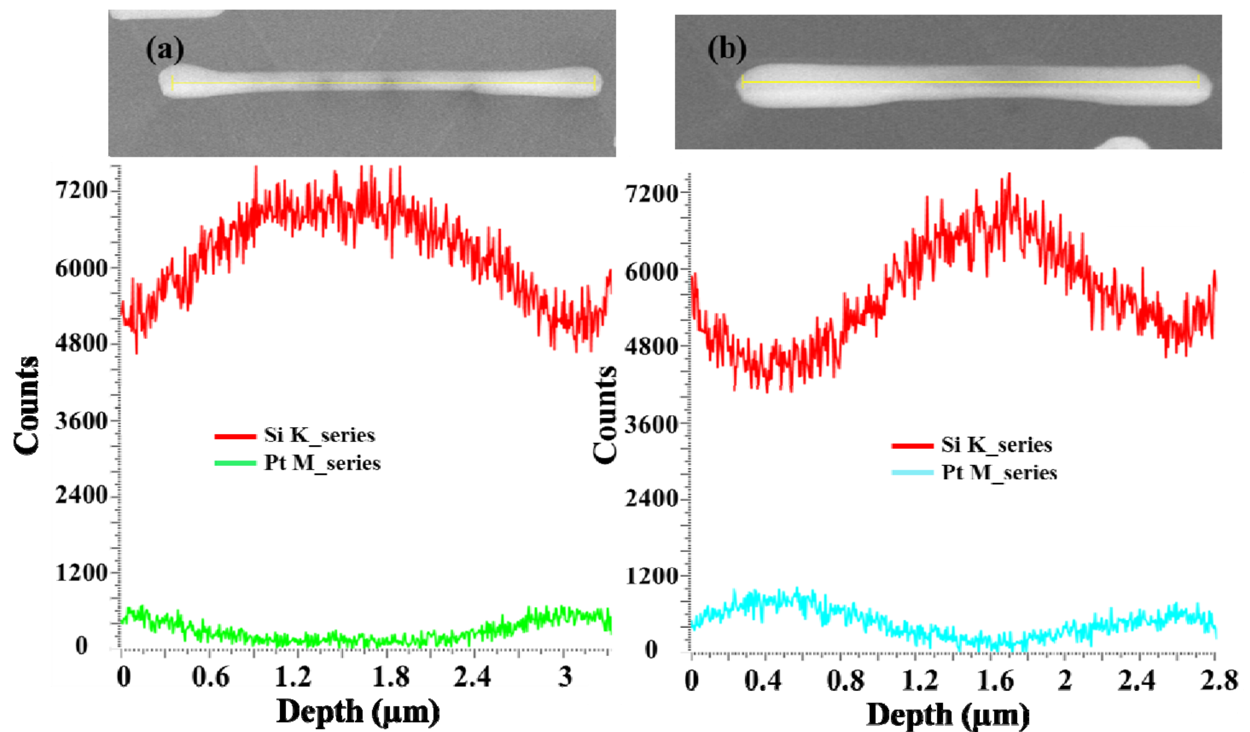


Figure 4.7: *Elemental analysis of the self-aligned PtSi silicide nanowire structures*

$$R = \frac{4120}{\rho} E^{(1.265 - 0.0954 \ln E)} \qquad \textbf{4.1}$$

where: R is the depth of electron penetration in microns, E is the primary electron energy in MeV and ρ is the absorber density in g/cm^3.

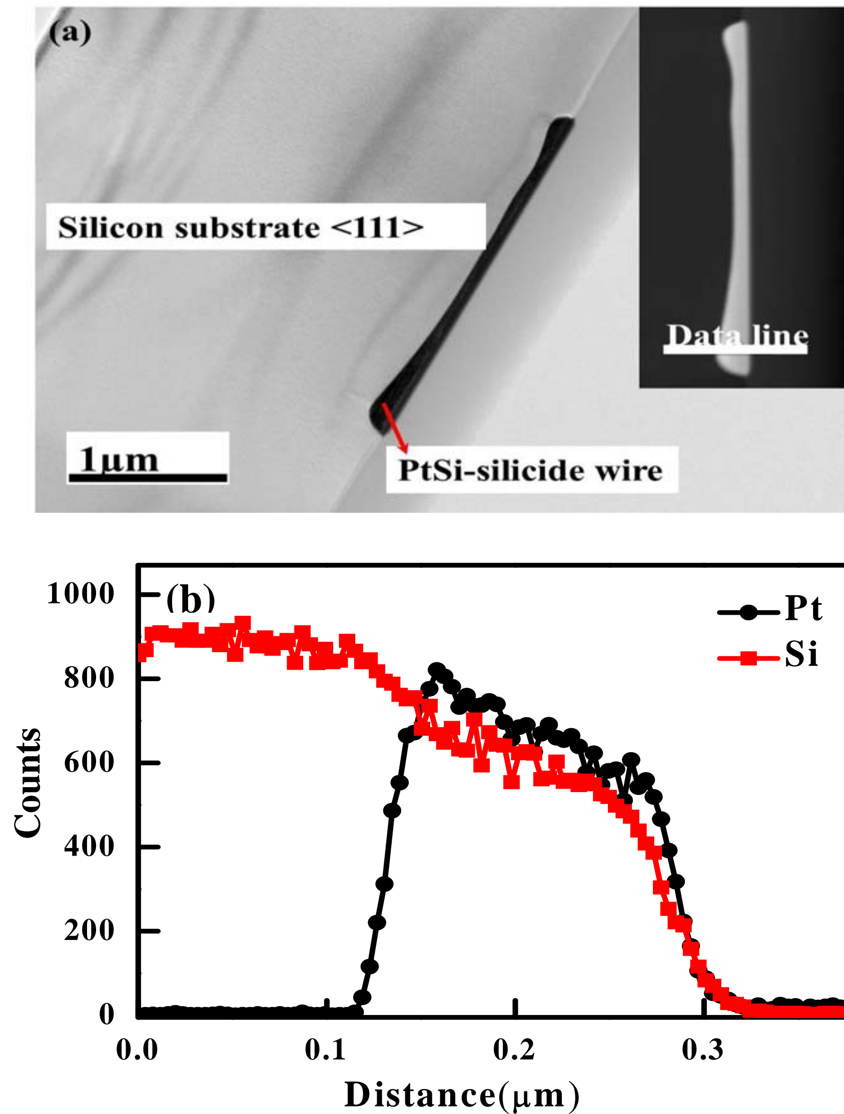


Figure 4.8: (a) *Bright Field (BF) TEM image showing a PtSi nanowire situated close to the surface of the silicon substrate. Insert image is the Annular Dark Field (ADF) STEM image with the EDX line scan. (b) Variation of Pt and Si content through the cross-section of the PtSi wire, along the data line in the inset image (a)*

The Bright field (BF) TEM image, **fig. 4.8 (a)**, shows the PtSi nanowire which extends below the Si substrate surface. The insert shows the Annular Dark Field (ADF) STEM image with the EDX line scan. The average Pt and Si counts through the cross section of the wire, **fig. 4.8 (b)** were found to be comparable, about 750 counts. This could only be explained by the existence of the PtSi monosilicide with 50 *at*% Pt and Si which is in good agreement with the stoichiometry of the PtSi phase identified using XRD, **fig. 4.6**.

4.2 Platinum silicide formation on the EBE deposited sample

The phase formation in the Pt-coated Si system was also studied on the electron beam deposited (EBE) sample with the same Pt thickness (~20 nm) as with the MBE sample. The experimental details are presented in **section 3.2**. **Fig. 4.9** displays the *in situ* real-time RBS results showing a colour coded plot of the total spectra collected from RT to 360 ^{o}C. During the temperature ramping process from RT up to ~220 ^{o}C, real time monitoring of the Pt-coated Si sample, indicated no reaction between Pt and Si (region 1), contrary to the MBE deposited sample of the same thickness where the reaction started at 200 ^{o}C, despite annealing at the same ramping rate (2°C/min), **fig. 4.1 (a)**. This indicates that in this EBE deposited sample the film was thermally stable in this temperature range. However, above 220 ^{o}C (region 2), real time RBS analysis indicates that the Pt starts to react with the Si to form a silicide phase, this is shown by the disappearance of the red colour code of the contour map. At 320 ^{o}C, the reaction between Pt and Si has reached completion and the formation of a stable silicide that existed up to the maximum temperature of the *in situ* real-time RBS experiment (360 °C) was observed (region 5). **Figs. 4.10 (a-d)** shows the RBS experimental (dotted line) and simulated data (solid line) spectra extracted from **fig. 4.9** at four different annealing temperatures, RT, 230 °C, 300 °C and 350 °C. Two

peaks of alpha particles backscattered from Si and Pt atoms can be seen at channels 275 and 470, respectively, **fig. 4.10 (a)**. The surface channel position of Si is at 290, however with the energy loss in the Pt layer, the Si signal appears at the 275 channel position. The peaks are clearly defined with no tails on either side of the peaks and the thickness of the Pt film, from the simulation (solid line), was found to be 125×10^{15} atoms/cm^2 (~20 nm) in good agreement with the thickness set during deposition. The simulation of the spectra from RT up to about 220 °C produced similar results.

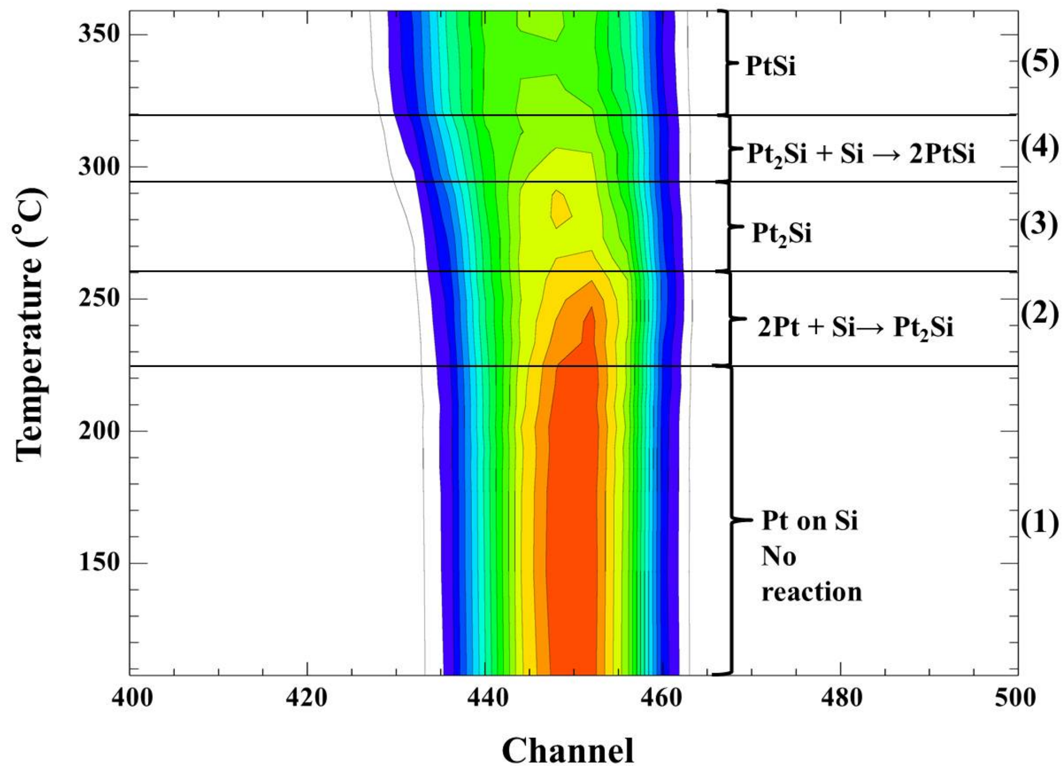


Figure 4.9: *In situ real-time RBS results showing a colour coded plot of the total spectra collected from RT to 360 °C. Right vertical axis shows temperature regions (1-5) where particular phases are formed.*

As shown in **fig. 4.9**, the increase in temperature triggered the reaction between Si and Pt, therefore **figs. 4.10 (b-d)** represents three stages of the Si and Pt reaction, the beginning (2), the continuation (3) and the final stage of the reaction (4).

In all spectra, a change in the Si and Pt peaks are noticeable, with a shoulder developing at the high energy side of the Si peak and a decrease of the yield at the lower energy side of the Pt peak. These changes are an indication of the interfacial reaction between Si and Pt which causes extra energy loss and thereby decreases the peak signal. The degree of change of the peak signal is linked to the amount of reacted Pt species i.e. the more the Pt atoms react with Si, the lower the signal on the lower energy side of the Pt peak and the higher the shoulder in the higher energy side of the Si peak as shown in **fig. 4.10 (b-d)**. Furthermore, the simulation of spectra revealed the following:

(i) At 230 °C, Pt reacted with Si to form the silicide phase with stoichiometry 67 at.% Pt and 33 at.% Si (Pt_2Si), with a thickness 70×10^{15} atoms/cm^2 (**fig. 4.10 (b)**). At 260 °C, all Pt had fully converted into the Pt_2Si with a thickness 178×10^{15} atoms/cm^2 (region 2, **fig. 4.9**).

(ii) In region (3), the Pt_2Si phase was found to be stable from ~260 ^{o}C to ~290 ^{o}C before reacting with Si to form PtSi at about ~300 °C. **Fig. 4.10 (c)** shows a simulation of a spectrum extracted at 300 °C, region (4) in **fig. 4.9**, and it was found that Pt_2Si had reacted with Si to form another silicide phase with stoichiometry 50 at.% Pt and 50 at.% Si which corresponds to the PtSi phase. The spectrum was simulated with 97×10^{15} atoms/cm^2 and 110 $\times10^{15}$ atoms/cm^2, for Pt_2Si and PtSi, respectively. The existence of these two phases further increased the energy loss, and as a result the broadening of the Pt peak was observed.

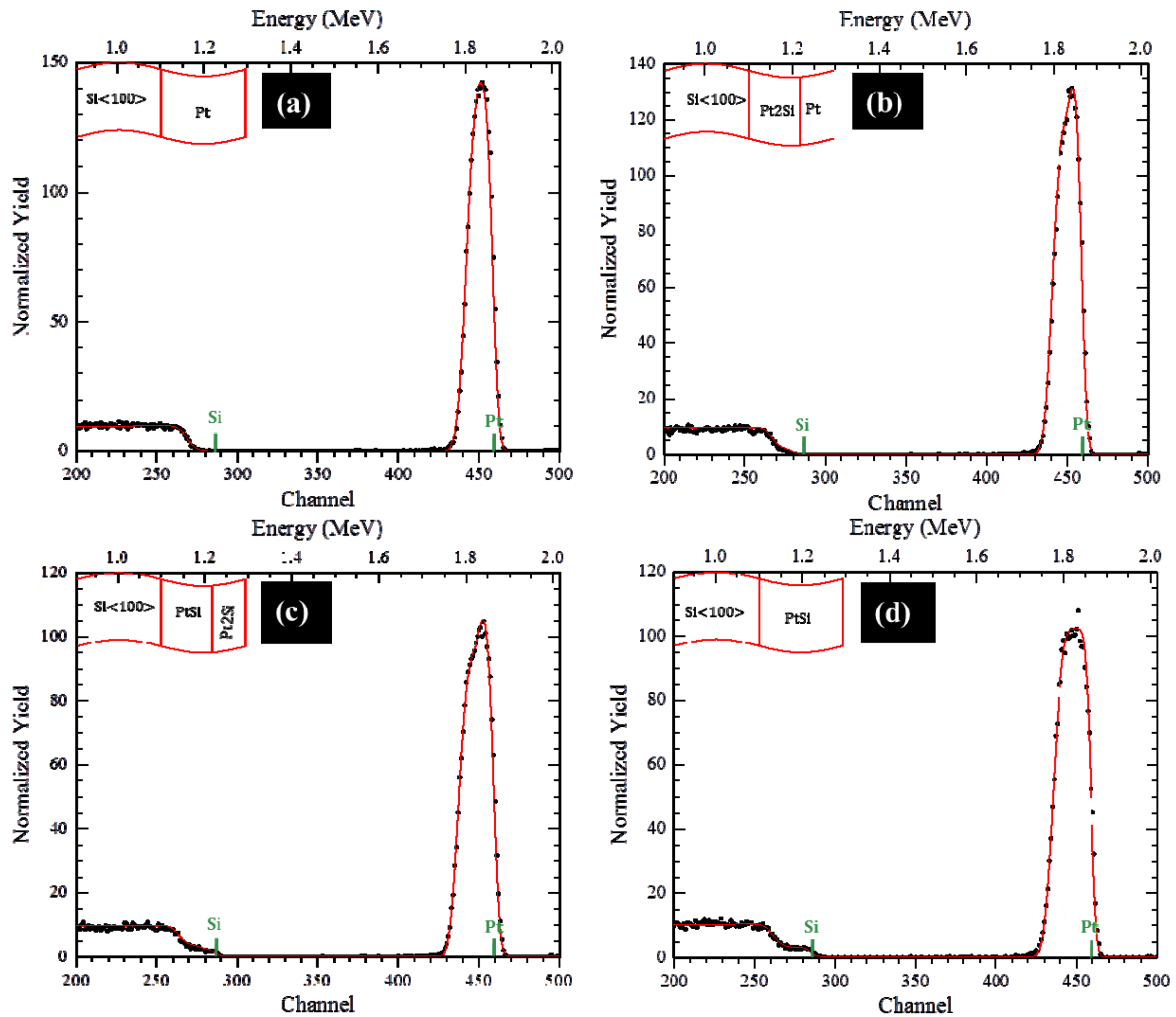


Figure 4.10: *RBS spectra extracted from figure 1 at three different annealing temperatures. (a) room temperature (b) 230 °C, (c) 300 °C and (d) 350 °C. The surface position of Pt (channel 470) and Si (channel 290) are marked.*

At about ~320 °C, the reaction between Pt_2Si and Si to form PtSi appeared to have reached its completion. Therefore, a spectrum at 350 °C, **fig. 4.10 (d)**, was extracted and simulated with one

layer of stoichiometry 50 at.% Pt and 50 at.% Si and 238 $\times 10^{15}$ atoms/cm^2. This phase existed even beyond 350 °C indicating that, it is the final stable phase of the Pt and Si reaction.

The formation of Pt_2Si and PtSi in sequence is observed in both the EBE and MBE deposited samples, however a delay of about 30 °C in the phase nucleation in the EBE deposited sample was observed. The different experimental conditions such as pressure, 8x10^{-9} mbar (MBE) and 5 x10^{-6} mbar (EBE), as well as cleaning methods are viewed as the contributing factors to the observed difference in the nucleation temperature of the first silicide. Regarding the second phase, the delay may be related to the nucleation barrier or strain relaxation as observed in the MBE sample (*in situ* XRD and *in situ* real-time RBS). These results (EBE sample) are, however, in reasonable agreement with the work published by Stark *et al.* **[46]** who reported a sequential formation of the Pt_2Si and PtSi phases in a Pt-coated Si system.

4.2.1 SEM and PIXE analysis of the EBE deposited sample

The EBE deposited sample was further analysed using a scanning electron microscope and the image is shown in **fig. 4.11 (a)** together with an image taken from the EBE deposited sample annealed at 800 °C for 30 minutes under vacuum (**fig. 4.11 (b)**). **Fig. 4.11 (a)** shows an overall smooth surface with small clusters (red arrows). However, due to the cooling effects on the coating layer morphology, the observed small coating cracks cannot be unambiguously attributed to the onset of the dewetting silicide layer. **Fig. 4.11 (b)** shows a rough surface morphology with randomly distributed PtSi droplet structures (red arrows) after annealing the Pt-coated Si sample at 800 °C. The formation of these droplets is the consequence of the dewetting process **[16-26, 103]**. With PtSi being the final and the most stable phase of the analysed system as the annealing temperature is ramped up, see **fig. 4.9**, the PtSi layer starts to dewet and at 800 °C, the

dewetting PtSi layer produces randomly distributed droplets, consequently, the underlying Si substrate is exposed, **fig. 4.11 (b)**.

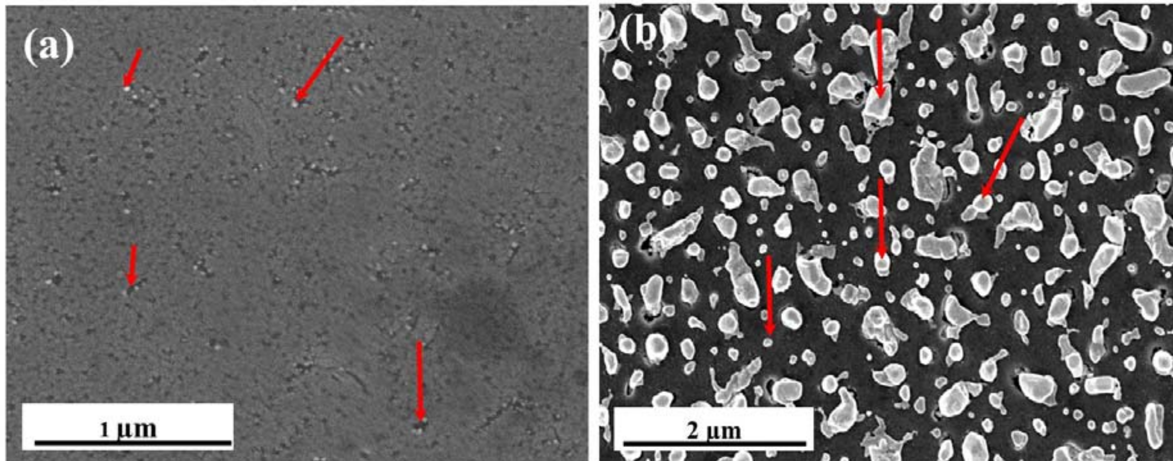


Figure 4.11: *SEM images taken from (a) sample after in situ real-time RBS experiment and (b) sample annealed at 800 °C for 30 minutes under vacuum, showing different morphology*

To investigate the elemental distribution on these samples, PIXE was employed. Even though the contribution from the Si substrate was high due to the penetration depth of the proton beam (3 MeV), using GeoPIXE software, it was possible to extract relevant information about the elemental distribution on the dewetted Si silicide layer. With the view that the Pt film (~20 nm) was thin compared to the Si substrate and the surface of the sample annealed at 800 °C was inhomogeneous, Pt was set-up as the impurity while Si the host element. **Fig. 4.12 (a)**, shows scan images of the Pt distribution after being subjected to *in situ* real-time RBS analysis, while **fig. 4.12 (b)** shows a scan image of the sample annealed at 800 °C for 30 minutes under vacuum. Comparing the two images, it can be seen that in **fig. 4.12 (a)** there are very few areas with low

Pt intensity, ~ 1000 counts, indicated by arrows. The lager part of the sample surface shows the Pt intensity in the range 4000 to 5000. In **fig. 4.12 (b)** many areas with low intensity of Pt (below 200 counts) were observed, numbered regions.

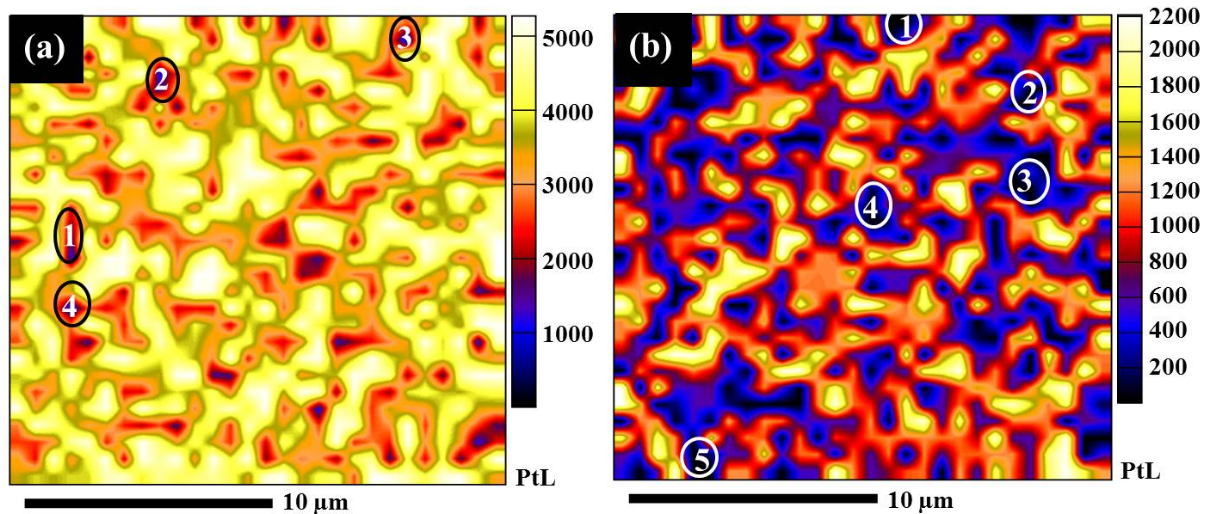


Figure 4.12: *PIXE scan images of Pt distribution (using multi-layered system in GeoPIXE software) taken from (a) sample after in situ real-time RBS experiment, and (b) sample annealed at 800 °C for 30 minutes under vacuum, using Si as a host element and Pt as an impurity in GeoPIXE software. Marked regions are the areas where low Pt counts were recorded*

Due to the spot size of the proton beam, used for the PIXE experiment, ~1.7 µm, the areas with high Pt intensity can be attributed to the dewetted Pt layer into droplets (not individual droplet) as identified in **fig. 4.11 (b)**. The areas with low Pt intensity correspond to areas of Si substrate left exposed. Additional analysis of the maps, by extracting data from low Pt (marked regions) and high Pt regions (high counts regions) of both **figs. 4.12 (a-b)**, was performed and data is

presented in **table 4.2** and **4.3**. By looking at the data obtained from this short analysis, we can conclude that the changes seen on the figures are significant and the difference in intensities between the two regions is larger than the statistical uncertainty. Furthermore, additional information on the dewetted sample to complement the PIXE results, **fig. 4.12 (b)**, was acquired using EDX. The results obtained using PIXE showed consistency with the complemental EDX technique. The SEM image, where the EDX was taken, is presented in the **fig. 4.13**.

Table 4.2: *Data from low Pt and high Pt regions of* ***fig. 4.12 (a)***

Pt counts (low conc. zones)	**Pt counts (high conc. Zones)**	**Difference (high-low)**
1463	5446	3983
1215	5312	4097
515	5905	5390
828	4577	3749

Table 4.3: *Data from low Pt and high Pt regions of* ***fig. 4.12 (b)***

Pt counts (low conc. zones)	**Pt counts (high conc. Zones)**	**Difference (high-low)**
0	1844	1844
0	1853	1853
0	2194	2194
0	2165	2165
0	2119	2119

The elemental analysis of the dewetted Pt silicide layer on the lager selected area, 7 µm (spectrum 5), data in the **table 4.4**, shows a high contribution from the Si substrate with about 98 at.% Si and about 1.5 at.% Pt. However, the analysis on the single droplets (spectra 1-3) showed increased Pt signals confirming that regions that give high Pt counts are regions with high droplet concentration, confirming the high Pt intensity in the PIXE results of **fig. 4.12 (b)**. Furthermore, no Pt was detected in spectrum 4. This is the area of the sample with no droplets which confirms that Pt is collected into droplets during the dewetting stage with very little to none remaining elsewhere on the substrate. This is confirmed by the low Pt areas of the same sample analysed by PIXE, **fig. 4.12 (b)**.

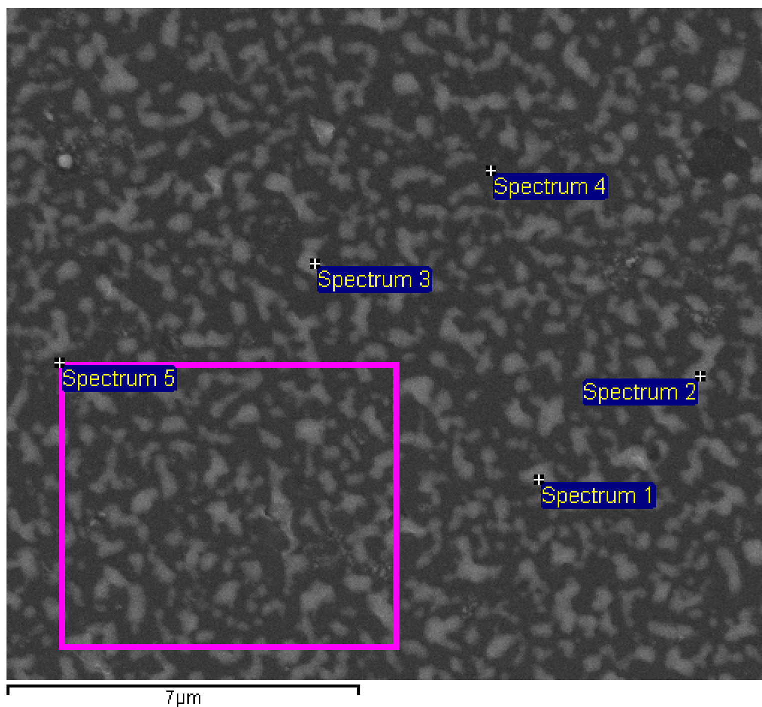


Figure 4.13: *SEM image used to analyse the elemental distribution by EDX (spectra 1-4_ spot analysis and spectrum 5_area (7µm ×7µm) analysis), corresponding PIXE image in* ***fig. 4.12 (b)***.

Table 4.4: *EDX data from the dewetted silicide layer*

Analysed region	Si (at%)	Pt (at%)
Spectrum 1	92.93	7.07
Spectrum 2	91.98	8.02
Spectrum 3	91.7	8.3
Spectrum 4	100	0
Spectrum 5	98.53	1.47

Furthermore, **fig. 4.11 (b)** shows how the Pt layer reacts with Si resulting in the formation of a silicide phase layer which eventually dewets into droplets. The droplets were mapped to determine the distribution of Pt and Si elements. **Fig. 4.14** shows the Bright field (BF) TEM image of the PtSi droplets situated close to the surface of the Si substrate. The inserts show the Annular Dark Field (ADF) STEM image with the compositional (Pt and Si) maps of a droplet on the Si substrate. The maps show that the droplets contained both Pt and Si elements. With this insight, the detected high Si counts (EDX and PIXE) are not only coming from the substrate itself but also from the Si atoms that have diffused into the Pt layer during silicide and droplet formation. The cross-sectional image also shows no Pt contrast between the droplets after the dewetting process affirming the zero Pt counts in spectrum 4 in the EDX table of **fig. 4.13**, supporting also the findings from the PIXE analysis (**fig. 4.12 (b)**).

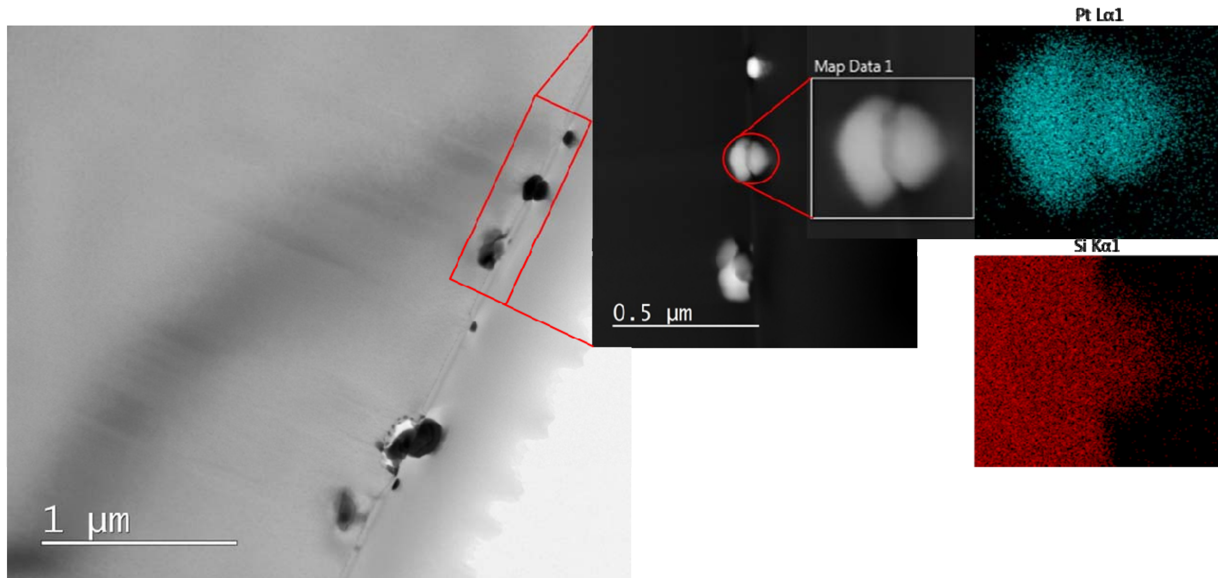


Figure 4.14: *Cross-sectional TEM of the Pt/Si droplets, corresponding PIXE image in* ***fig. 4.12 (b)****.Inset, blue and red, images shows the mapping of the distribution of Pt and Si in the droplet.*

4.2.2 First diffusing element during platinum-silicon reaction (EBE deposited sample)

Having studied, and understood the phase transformation sequence in the Pt-coated Si system, it is also important to investigate the first element that diffuses in this system. *In situ* real-time RBS analysis was carried out on a sample with titanium (Ti) diffusion barrier of 1 nm, deposited between the Pt coating and the silicon substrate using EBE technique. The barrier serves to impede the reaction between the Pt and Si that has been observed to start around 200 °C, **fig. 4.1 (a)** and 230 °C, **fig. 4.9**. During the *in situ* real-time RBS, the channel energy of the barrier was monitored at the start of the reaction with the assumption that if Si diffuses first, the energy channel position of Ti would shift to the lower channel position whereas if Pt would diffuse first than the energy channel of the Ti barrier would move to a higher channel position (to the surface

position). The in-situ analysis shows that the reaction between Pt and Si started at about 360 °C, **fig. 4.15 (a)** due to the presence of the barrier. The spectrum at room temperature (25 °C) was simulated (red line) with two layers (Pt and Ti) with the Ti channel position appearing at 355. The spectrum was compared to the one extracted after the reaction had occurred, (blue plot). The channel position of the Ti was noticed to have shifted towards the surface and appears at channel position 340, after 377 °C. With this observation, the diffusion of Pt atoms towards the silicon substrate for the formation of the Pt rich silicide phase is reported. These results are in good agreement with the information presented in the literature **[104-105]**.

After the reaction had started, it was somehow difficult to simulate the spectra so as to conclude whether or not the phase sequence (Pt-Pt_2Si-PtSi) took place, hence *in situ* XRD was used, **fig. 4.15 (b)**. The Pt diffraction peaks appears at about 2θ ~ 40° (high intensity diffraction peak) and 2θ ~ 46° (small intensity diffraction peak). Since the Pt film was deposited into a Si substrate, the additional reflections (e.g. at 2θ ~ 28 ° and a small intensity, but broad, peak at 2θ ~ 32 °) are attributed to the contribution from the substrate. The experiment was conducted using a ramping rate of 30 °C/min and the reaction of Pt with Si was observed at 450 °C. The first phase to form in this experiment could not be unambiguously identified as the temperature at which Pt diffuses through the Ti (1 nm) barrier to react with the Si substrate was high resulting in the diffraction peaks matching the second phase (PtSi) also identified. However, these results are in reasonable agreement with the findings of Larrieu *et al*. **[37]** who found that the formation of the Pt_2Si could be completed in less than 3 seconds due to the rapid thermal annealing at 300 °C.

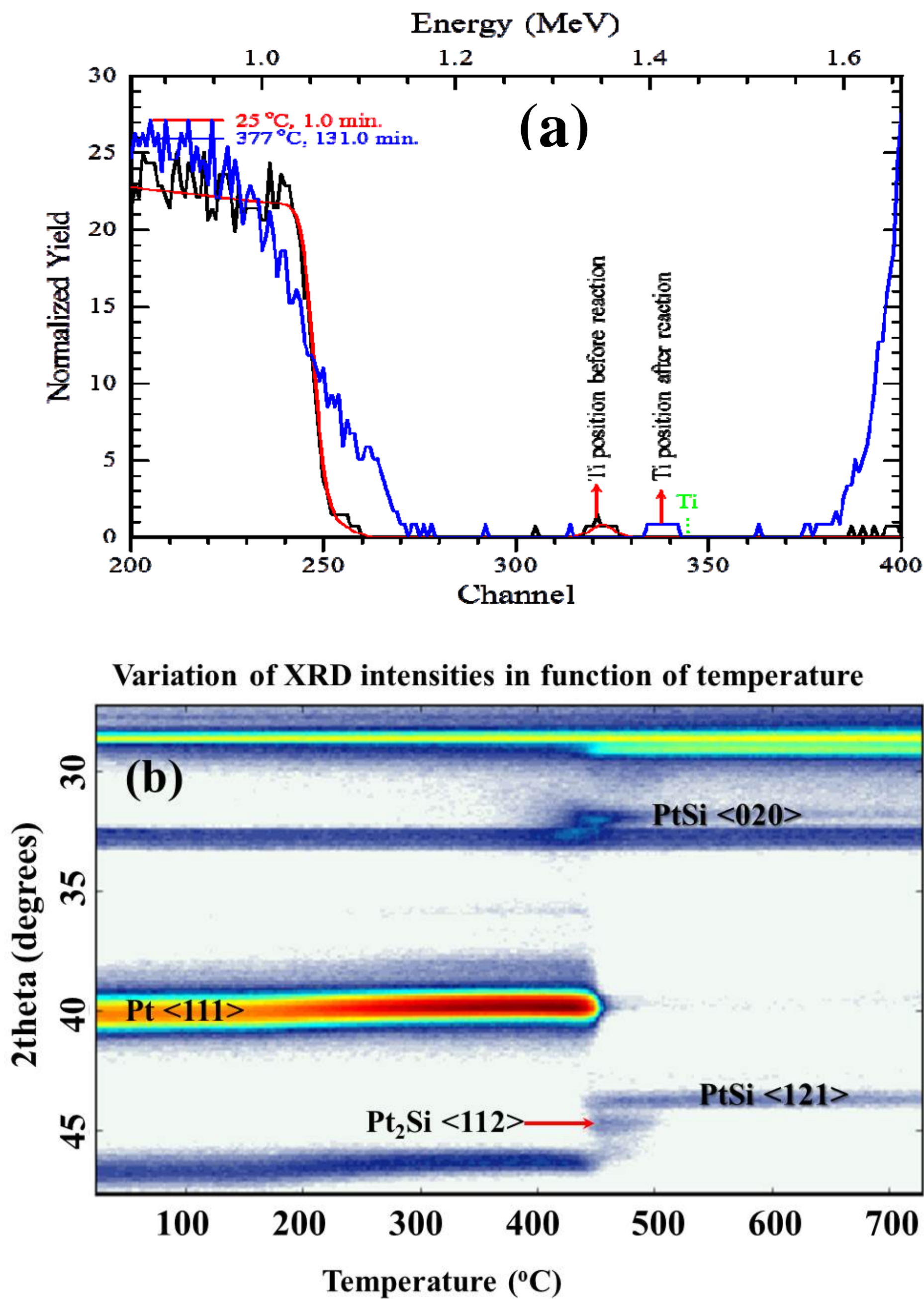


Figure 4.15: *First diffusing element in the Pt deposited on the Silicon wafer. (a) Ti energy channel position before and after the reaction of Pt and Si. (b) In situ XRD analysis of Pt reacting with Si and separated by Ti barrier.*

In our experiment the reaction is taking place above 400 °C which could mean that the formation of the Pt_2Si phase could happen way below their reported 3 seconds, hence no precise identification of the phase sequence in these conditions. The main diffraction peaks of the identified phases can be seen at $2\theta = 44.693°$ and $2\theta = 43.583°$ for Pt_2Si and PtSi, respectively. However, Pt_2Si ceases to exist after 500 °C with only the PtSi phase present.

4.3 Silicon nanowire growth using platinum as a metal catalyst

4.3.1 EBE deposited platinum catalyst

In the previous section, phase sequence and droplets formation was investigated to better understand the process leading to the SiNWs growth using a metal catalyst. It has been shown that PtSi is the last and most stable phase to form on the Pt-coated Si substrate with the subsequent dewetting of the phase into droplets occurring at high temperatures. In this section, these droplets, **figs. 4.11 (b)**, **4.13**, **and 4.14**, act as catalyst seeds for the growth of SiNWs. The sample with PtSi silicide droplets was subjected to annealing at a high temperature (1000 ^{o}C) for 10 minutes in flowing argon gas (250 ml/m). A SEM micrograph of the annealed product is given in **fig. 4.16 (a)**. Out of plane SiNWs with 100–150 nm diameter and 2-3 μm length were observed. No external silicon vapour was used in this sample and therefore the nanowire growth mechanism was attributed to the SLS growth mechanism. This SiNWs' growth method has been reported to take place at high temperatures for the incorporation of the Si atoms (from the substrate) into the silicide droplets. **Fig. 4.16 (b)** shows a lateral grown PtSi-catalysed SiNWs which were synthesised using PLD to provide a Si flux (external silicon supply), **see section 3.2** for experimental details. These in-plane grown nanowires were found to have diameter and length in the ranges 200-500 nm and 2-3 μm, respectively. Due to the growing interest in in-

plane SiNWs for their incorporation into modern planar technology, different growth methods have been reported **[33-35, 106]**. In this work, Si flux was incorporated into the PtSi droplets at 800 ^{o}C by the ablation of a Si target inside the PLD chamber. We therefore propose that the PLD technique can be used to grow these nanostructures below the eutectic temperature where the liquid phase transforms into two solid phases (L $\rightarrow$ PtSi + Si). The temperature used in this work (800 °C) is about 180 °C lower than the eutectic temperature (978 °C) therefore the growth of the in-plane nanostructures is attributed to the vapour-solid-solid (VSS) mechanism. The Pt-silicide tips can be seen at the end of the wires, shown by the red arrows, in both **figs. 4.16 (a) and (b)**.

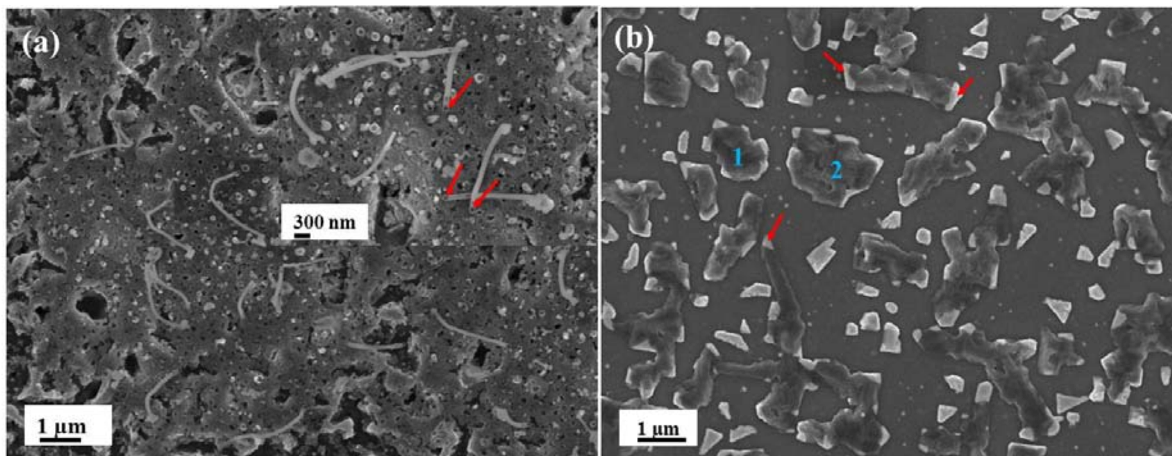


Figure 4.16: *Pt silicide catalysed Si nanowires using different growth methods (a) Annealing at 1000 °C in argon gas, showing out of plane growth of the wires and (b) Pulsed laser ablation of the silicon target at 800 °C in vacuum, showing in-plane growth of the SiNWs on a silicon substrate. Red arrows are pointing at the nanowire's tips while numbers show the growth of the flower-like structures.*

In addition, the growth mechanism seems to initiate from around the droplet edges, hence the bigger droplets produced a flower-like Si structures consisting of PtSi droplet catalyst, marked as 1and 2 in **fig. 4.16 (b)**.

4.3.2 MBE deposited platinum catalyst

Figure 4.17 (a) shows the image of the MBE 20 nm Pt-coated sample after annealing at 1000 °C in an argon atmosphere for 15 minutes. The micrograph shows the tangle and curved SiNWs.

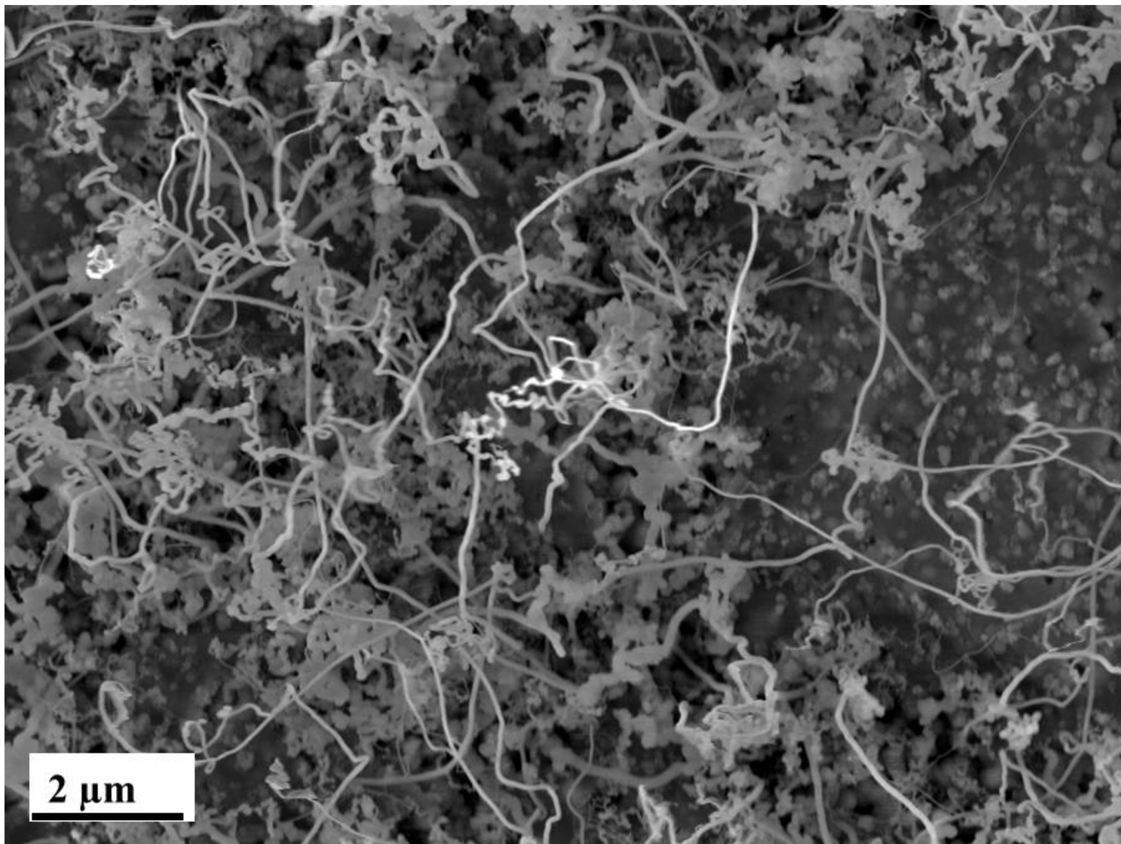


Figure 4.17: *SEM image of crystalline core-amorphous shell silicon nanowires grown on the surface of a Si (100) substrate which was coated with platinum as catalyst.*

A closer look at these nanomaterials using HRTEM confirmed that the synthesised SiNWs consist of a heterostructure with crystalline core and Si oxide shell, **fig. 4.18**. TEM images of the Pt-catalysed SiNWs, annealed at 1000 ^{o}C for 15 minutes in 250-300 millilitres per minute (ml/m) Argon atmosphere, are shown in **figs. 4.18 (a-b)**.

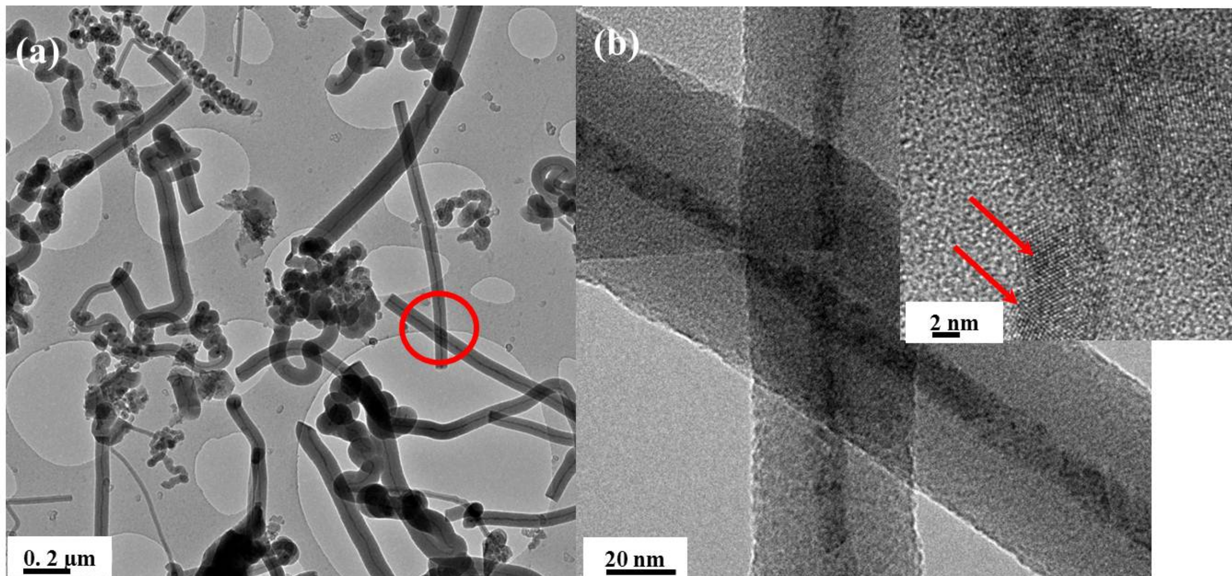


Figure 4.18: *Crystalline core-amorphous shell silicon nanowires obtained by annealing 20 nm Pt-coated Si<100> substrate at 1000 °C for 15 minutes in 250-300 ml/m Ar atmosphere (a) Low-magnification TEM image showing several wires and (b) HRTEM image of image-(a) and the zoomed region is shown by the red circle. The insert image (b) shows the lattice fringes of the two crossing nanowires*

The images show the core-shell structures consisting of a crystalline Si core sheathed with an amorphous SiO_x. The diameter (core plus shell) of the SiNWs ranged from 20 nm to 90 nm. The core diameter of the selected nanowires was found to be about 11 nm while the amorphous layer

was approximately twice the core size (20 nm), **fig. 4.18 (b)**. The circle in image **4.18 (a)** shows two core-shell SiNWs crossing each other. The area was enlarged for more details as presented in the image **4.18 (b)**. In addition, the inset is a HRTEM image zoomed at the interception point of the two wires. The image clearly reveals the lattice fringes for the two crossing wires. The two nanowires consists of crystalline cores with lattice fringes separated by a spacing of about 0.2 nm. Some lattice defects, stacking faults, in the area pointed at by the arrows were observed. The application of SiNWs in nano-electronic device was of particular interest in this research. The observed thicker amorphous layer increases the resistance of the contact from a nano-device fabrication point of view.

Carbon in the form of methane gas (CH_4), was introduced into the growth chamber in the attempt to minimize the oxidation of the nanowires during growth. From the SEM image analysis, similar wool-like morphology was observed, **fig. 4.19 (a)**. However, HRTEM analysis of these nanowires shows that the crystalline core (insert) is different from the previous sample as no evidence of stacking fault defects were observed. The diameter of the nanowires (core plus shell) ranged from 20 nm to about 80 nm. Due to the observed highly crystalline Si core and reduced amorphous shell, the electrical properties of these SiNWs were tested. The thinner amorphous shell can be removed using hydrofluoric acid (HF) during device preparation. For the electrical measurement, a Si substrate with a 300 nm SiO_2 layer with pre-prepared device electrodes was used for the SiNWs device fabrication using electron beam lithography, see details in **section 2.3.2**. The prepared device electrodes were given a unique number to distinguish them from one another. The nanowires were drop-casted onto this substrate and located for contacting. **Figs. 4.20 (a-b)** shows the drop-casted amorphous shell-crystalline core SiNWs, pointed by red arrows, on the surface of the device substrate.

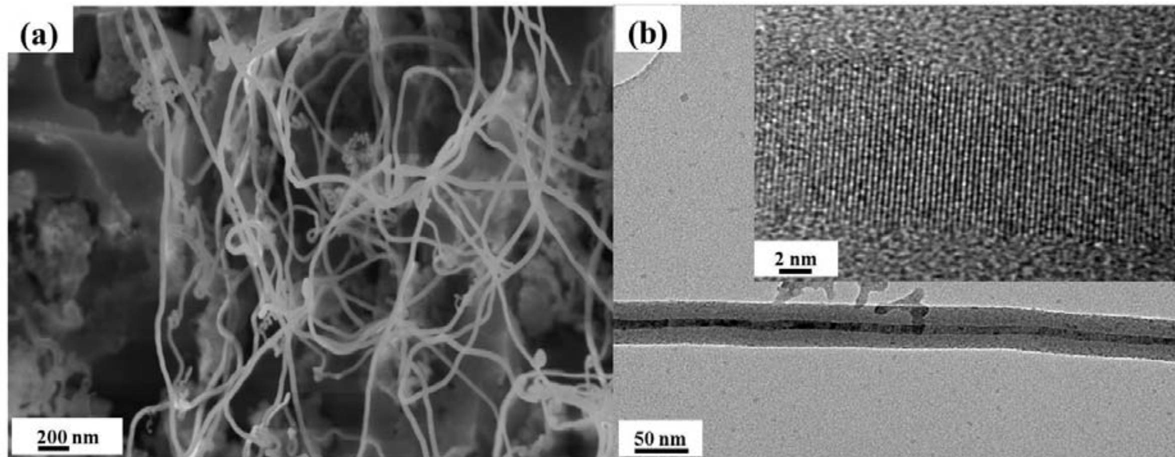


Figure 4.19: *Crystalline core-amorphous shell silicon nanowires obtained by annealing Pt-coated Si<100> substrate at 1000 ^{o}C for 15 minutes in a mixture of Ar and CH_4, 250 and 10 ml/m, respectively. (a) SEM image showing SiNWs, (b) corresponding TEM image showing SiNWs with their crystalline core and amorphous shell, insert is a HRTEM showing the lattice fringes of the crystalline core.*

The electrical current-voltage relationship of a number of SiNWs, at room temperature, is given in **figs. 4.20 (c-d)**. A very low current was measured from three selected nanowires, in the range of 2 to 30 pico-amperes. It should be noted that the SiNWs consist of a different diameter with a different thickness of amorphous shell. With the same etching time of all nanowires, some nanowires may still be coated with an oxide shell, resulting in high contact resistance. In addition, non-Ohmic behaviour of the Ti/Au contact was observed. However, annealing the device that initially showed a very low current (approximately 3 pA at 30 V) between 65 ^{o}C and 95 ^{o}C showed a slight improvement in both Ohmic behaviour as well as current measured, **fig. 4.20 (d)**.

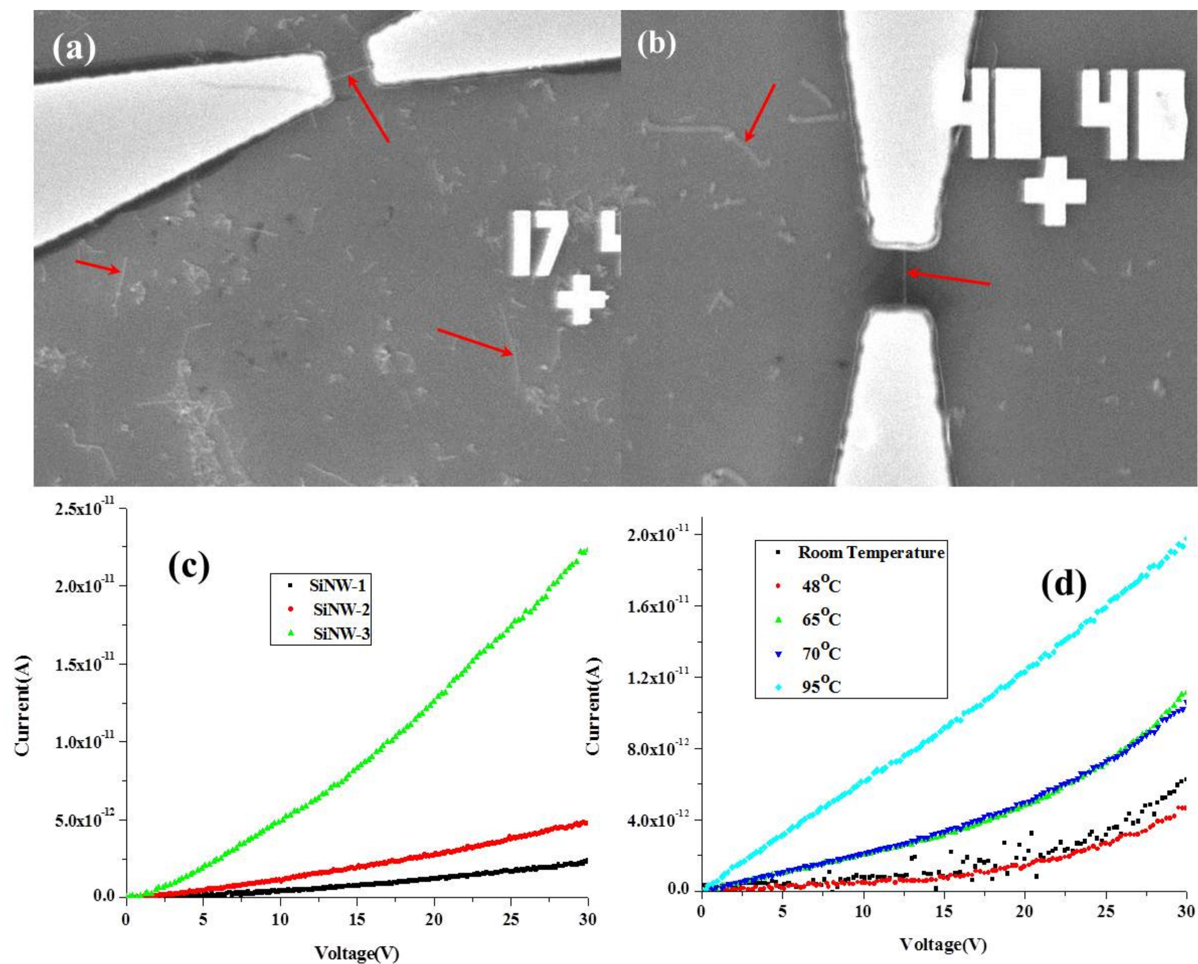


Figure 4.20: *(a-b) selected nanowire based devices with their unique device numbers. Red arrow shows the drop-casted silicon nanowires, including the contacted ones between the electrodes. (c) Shows the electrical (I-V) measurement of the selected wires (1, 2 and 3). (d) Shows the temperature dependence of I-V characteristics of a nanowire.*

The current improved from 3 pA, at room temperature, to about 23 pA, at 95 ^{o}C. This improvement in the conductivity of the devices is a true indication of a contact resistance lowering by the annealing of the device contact structure. The conductivity of the Ti/Au

contacted SiNW devices has been reported to improve after annealing at high temperature, in 450 ^{o}C-850 ^{o}C temperature range due to the formation of the titanium silicide **[107]**. Higher temperatures could not be investigated in this research as 100 °C was the limit during the device analysis. In addition, Lee *et. al* **[75]** found that the conductivity of the Ti/Au contacted SiNWs is also dependent on the gate voltage, as their device gate voltage was increased, the conductivity also increases, while the I-V relationship becomes linear. Despite the limitation in the temperature used in the current report, the behaviour of the tested devices did indicate the dependence of the conductivity of the contact structure to the annealing which is found to be in reasonable agreement with the literature reports **[75, 107]**. From the above analysis we therefore propose the following:

(i) High temperature annealing of the device structure is recommended to improve the non-linear contact behaviour when using Ti/Au to contact the SiNWs.

(ii) Since the oxide shell of the tested SiNWs was etched during the device fabrication, we highly recommend this step to be avoided during device fabrication as some of the nanowires may still be coated with the oxide shell due to the difference in their oxide thicknesses. In addition, the etching of the oxide layer on the substrate will be avoided when the etching of the nanowire shell is done prior to electron beam lithography device preparation, see **fig. 4.21**. In this image, it is shown that the Si oxide shell can be removed by etching with 7% HF for 40 seconds while the SiNWs are still embedded on the substrate. **Fig. 4.21 (c)** shows the HRTEM of an etched nanowire with no oxide shell. The lattice fringes have a spacing of ~ 0.19 Å which corresponds to the d-spacing of the 220 plane of the Si crystal structure.

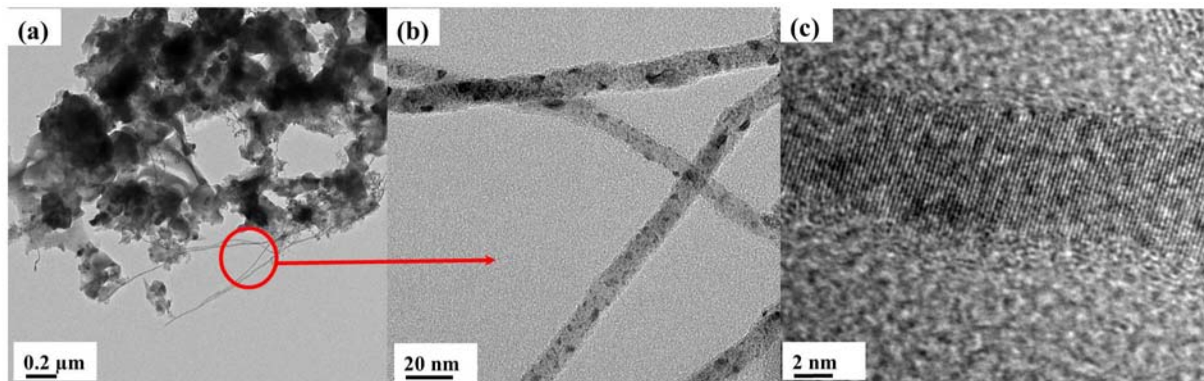


Figure 4.21: *(a) TEM image of a crystalline core silicon nanowires after etching for 40 seconds using 7% HF. (b) zoom image of (a) at the circled area, no oxide shell is left after etching. (c) HRTEM image showing lattice fringes of the crystalline core.*

Whether etching before device fabrication, see (ii), or during device fabrication, **fig. 3.3 (c)**, the use of non-user friendly (HF) acid can be eliminated completely. Below we present the possibility of using silicide forming metals (presented here is Pt) as an alternative contact material for the as-prepared core-shell SiNWs. Contacting Pt to the oxide shell of the SiNW does result in high contact resistance due to the presence of the dielectric SiO_x layer. However, it has been shown, in this research, **fig. 4.1** and **4.9** that Pt reacts with Si at temperatures between 200 ^oC and 400 ^oC to produce silicides that are used in device electrode preparation. Based on these results, it was also of interest to study the behaviour of the Pt in contact with Oxygen (O) contaminated silicon (referred to as SiO_x) contact structure under annealing. Electron beam evaporation was used to deposit a multilayer consisting of O contaminated Si layer (70 nm) as a first layer and Pt (100 nm) as a second layer on Si substrate. The samples were analysed using *in situ* real-time RBS, **fig. 4.22 (a)**. XPS was used for surface elemental and compound composition analyses, **4.22 (b)**. To confirm the phase nucleation in this system, *in situ* XRD was used **fig. 4.23.** The *in situ* real-time RBS spectra, collected continuously during the heating process from room temperature to 450 °C, at 2 °C/min ramping rate, were summed up and presented in a contour map, **fig. 4.22 (a)**. The simulation of the spectra from room temperature up to around 300 °C required two layers, the first layer with pure Pt and the second layer with about 3:1 ratio of Si to O (approximately 70 at.% Si and 30 at.% O). Due to this amount of O in the Si layer, which acted as a diffusion barrier for Pt to react with Si at lower temperatures, the reaction between Pt and Si was observed to have started around 300 °C, **fig 4.22 (a)**. This indicates a reaction temperature delay, between these two elements (Pt and Si), of about 70 °C when compared to the reaction temperature (230 °C) of the sample with no O contamination, **fig. 4.9**.

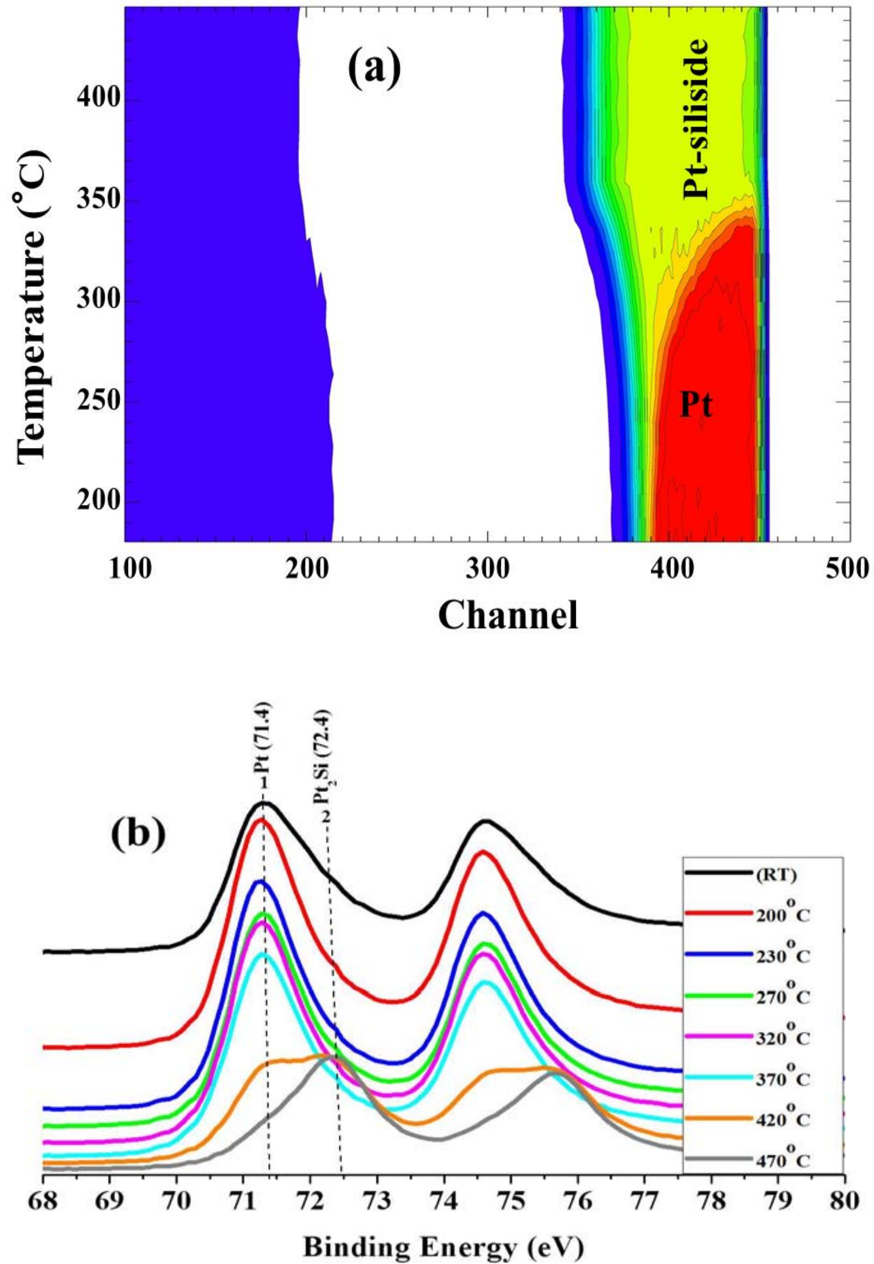


Figure 4.22: *Pt/SiO$_x$ multi–layer structure on silicon substrate (a) in situ real-time RBS analysis, (b) XPS results showing the binding energies of Pt4f spectra recorded at different temperatures.*

It was found, during RBS spectra simulation that the channel position of O before reaction was at about 140. After reaction, however, O was found at the surface channel position of about 170. This was tentatively attributed to the O moving to the surface when Si reacts with Pt. In addition, the thickness of the O contaminated Si layer was found to have decreased with the increasing Pt silicide layer with stoichiometry of about 67 at.% Pt and 33 at.% Si (~ Pt_2Si). The *in situ* real-time RBS results were complemented by the XPS analyses of the sample cut from the same wafer. **Fig. 4.22 (b)** shows the binding energy of the metallic Pt (Pt4f7 level) at different annealing temperatures. No changes in the Pt4f7 level (at 71.4 eV, dotted line (1)) were observed from the spectra recorded at room temperature, 200 °C, 230 °C, 270 °C, 320 °C and 370 °C. However, above 370 °C (e.g. 420 °C) a split in the Pt4f7 peak into two binding energies (71.4 eV and 72.5 eV, dotted line (1) and (2), respectively) was observed. This split was attributed to the Pt reacting with Si to form Pt_2Si (72.5 eV). At 470 °C, the pure Pt had been fully converted to Pt-silicide with the shift from 71.4 eV to 72.5 eV. No presence of the second silicide (PtSi) was observed at these conditions. We found these results to be in good agreement with the *in situ* real-time RBS.

In situ XRD, **fig. 4.23**, was used to investigate the structural information of the silicides. The analyzed sample was cut from the same wafer as the *in situ* real-time RBS and XPS samples. The annealing was performed at a ramping rate of 30 °C/min from room temperature to 850 °C. From the results, the phase sequence (Pt_2Si-PtSi) during the Pt reacting with the O contaminated Si layer can be expected. The difference in the phase formation temperature is attributed to the temperature ramping rate used during the experiments, 2 °C/min and 30 °C/min for the *in situ* real-time RBS and *in situ* XRD, respectively. In terms of the first phase to form, the results are in reasonable agreement with the compound composition from XPS and *in situ* real-time RBS. It is

therefore believed that the temperature was below the formation of the second composition (PtSi), XPS and *in situ* real-time RBS experiments, considering that Pt was reacting with the O contaminated Si and the maximum temperature used was around 450 °C.

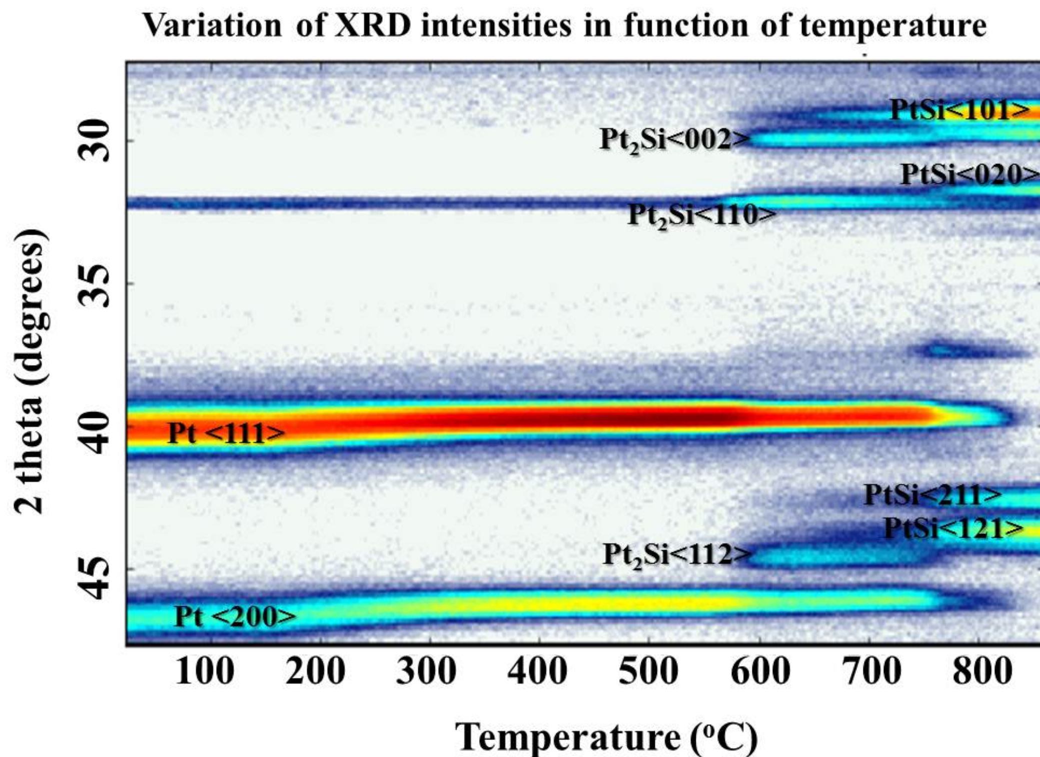


Figure 4.23: *Pt/SiO$_x$ multi–layer structure on silicon substrate in situ XRD.*

The O distribution in the sample thickness (before and after annealing) was obtained using depth profile analysis (XPS), **fig. 4.24**. The x-axis is presented in etching time as there was no standard sputter rate for the different elemental composition to precisely convert the time axis to thickness. A Pt signal appeared on the surface up to 800 seconds etching time, after which, the

interface, Pt/SiOx layer, was reached and then Si and O appeared, **fig. 4.24 (a)**. The silicon counts on the Pt surface are attributed to the noise.

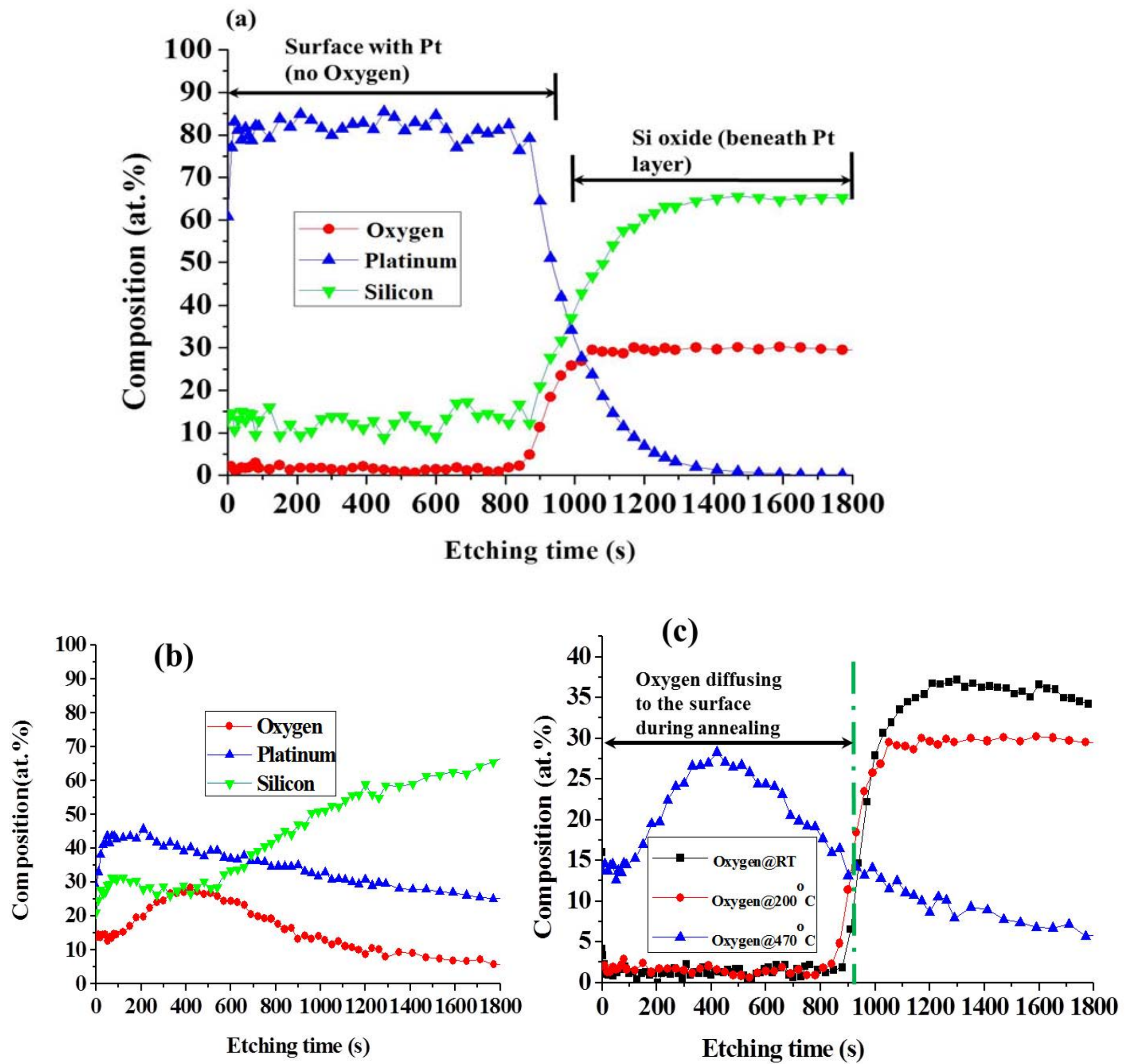


Figure 4.24: *Pt/SiO$_x$ multi–layer structure on silicon substrate (a) XPS depth profile analysis below 300 ^oC, (b) XPS depth profile analysis above 300 ^oC and (c) Oxygen depth profile comparison at different temperatures.*

When the temperature of the sample was raised above 300 °C, Pt reacted with Si from the O contaminated layer, **fig. 4.24 (b)**. It is therefore shown that during the Pt reaction with Si, the O peaked shift towards the surface. **Fig. 4.24 (c)** shows the comparison of oxygen positions at different temperatures. Initially O was buried underneath the Pt layer however it is detected on the surface during the Pt and Si reaction. These observations are in good agreement with the work of Nava *et al.* **[108]** who observed, using Auger electron spectroscopy, that the O peak moves to the surface on the reaction of O contaminated (< 1 at.%) Pt layer with the Si substrate. These results suggest the high possibility of using silicide forming Pt and other silicide forming metals (i.e. Pd) as contact materials to the O contaminated (core-shell) SiNWs without first removing the oxide shell using hazardous acid (HF). These desirable observations can be implemented in both n-type and p-type core-shell SiNW structures, depending on the intended application of the SiNW based device. With the above results, we propose the non-usage of the hazardous acid to remove the oxide shell during the lithography preparation of the core-shell SiNW based devices. We further demonstrate this by depositing a very tiny Pt layer (1 nm) on the core-shell SiNWs using EBE. The coated nanowires were annealed in vacuum at 800 ^{o}C, **fig. 4.25**. The idea was to simulate the Pt contact to the core-shell SiNW structure (Pt/SiO/c-SiNW). The annealing of the Pt coated SiNWs showed the formation of the Pt silicide nanoparticles with diameters ranging from 4 to 20 nm, **fig. 4.25 (a)**. A closer look at the annealed Pt silicide nanoparticles decorated core-shell SiNW, **fig. 4.25 (b)**, shows that the particles are fully crystalline and some appeared to have created contacts to the crystalline core of the nanowire. This is in agreement with the XPS results in **fig. 4.24**, that the deposited Pt reacts with Si, of the O contaminated Si shell, and at the same time O diffuses outward to the surface of the nanowire leaving Pt silicide contacted to the crystalline core of the nanowire.

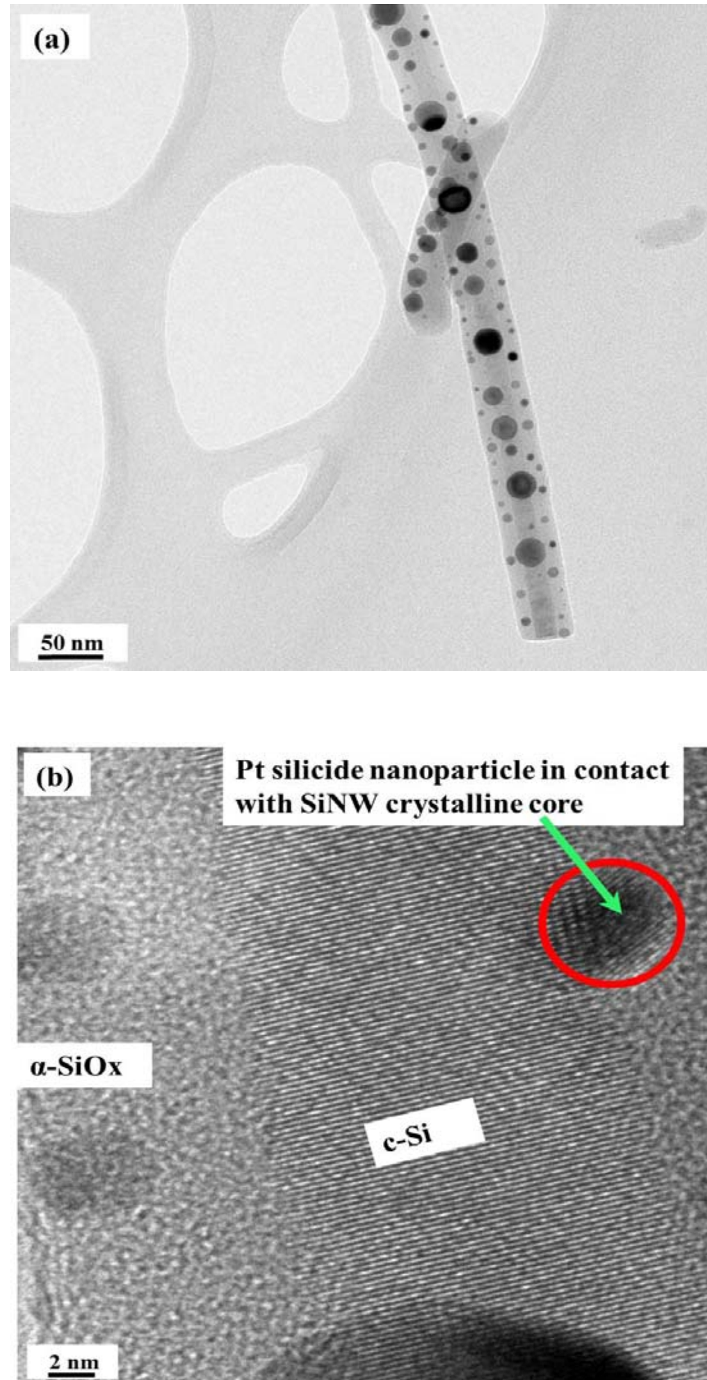


Figure 4.25: *Core-Shell SiNW, (a) decorated with Pt silicide particles after annealing a Pt layer deposited on the nanowires, (b) HRTEM showing the particles in contact with the crystalline core of the SiNW.*

Furthermore, the decoration of the core-shell SiNWs, (**fig. 4.25**) serve not only to describe the reaction process taking place when silicide forming metals are used as contact to the core-shell SiNWs but the decorated nanowires could be of great benefit in a wide range of applications, such as building blocks in hydrogen production from water using solar energy **[109]**. Pt is used in this process because it is a hydrogen evolution reaction catalyst with very high activities which enables the high performance H_2O reduction reaction, facilitating the transfer of the photogenerated charge from the NW to the solution. Furthermore, the material could also be compared to other silicide forming metals (Ag and Au) decorated SiNWs **[110-111]**.

4.4 Palladium silicide formation

This section presents the comparison of the *in situ* XRD and *in situ* real-time RBS for the formation of Pd silicide leading to the formation of SiNWs. The formation of Pd silicide nanowires at high temperature, in the presence of Si vapour, inside the MBE chamber is presented. Four RCA cleaned Si wafers (two p-type (111) and two n-type (100)) with 5 cm in diameter and 1-10 ohm.cm resistivity were used in this investigation. The Pd coatings were prepared as described in **section 3.1**. The reaction between Pd and Si as a function of temperature was investigated on one p-type (111) silicon wafer coated with a 20 nm Pd layer using *in situ* real-time RBS, **fig. 4.26**. The spectra were collected continuously during the heating process from room temperature to 600 °C and summed up into appropriate time intervals followed by the simulation of the individual spectrum. The simulation of the spectra before 100 °C required only one layer (palladium of approximately 20 nm) for the coating layer and it was found to be in agreement to the thickness given by the thickness monitor during the MBE deposition.

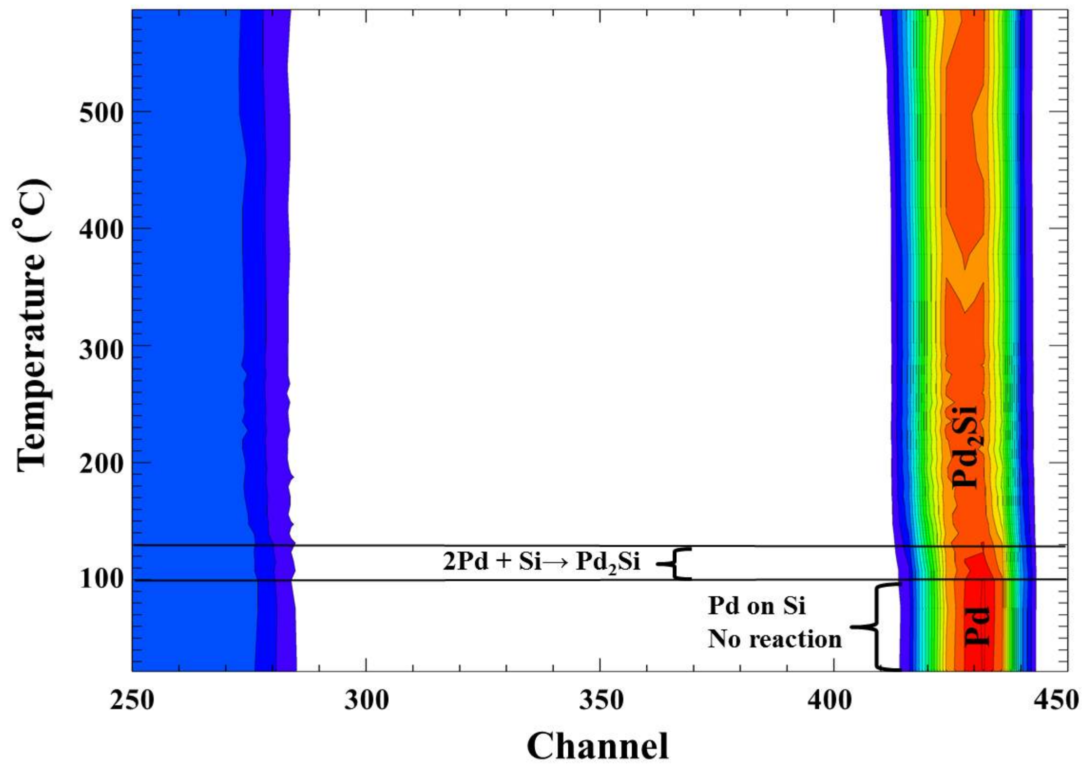


Figure 4.26: *In situ real-time RBS contour map showing the formation of the palladium-silicide during the palladium and silicon reaction from room temperature to 600°C at 2*°C/min ramping rate.

The consumption of pure Pd by growing the Pd silicide phase was observed to have started at about 100 °C and reached completion at 130 °C (marked area in **fig. 4.26**). The composition used to simulate the spectra collected above 130 °C corresponds to the stoichiometry of the Pd_2Si phase, classified as a hexagonal crystal structure with unit cell parameters a = b = 6.497 Å, c = 3.432 Å. This means therefore that according to the *in situ* rea-time RBS analysis of the 20 nm Pd-coated silicon wafer, the formation of the Pd_2Si phase can be expected at about 100 °C and will grow at the expense of Pd up to 130°C (no pure Pd is available above 130°C). Also using in

situ real-time RBS, Theron **[112]** observed the nucleation of the Pd_2Si phase around 200 °C, with 65 nm thick layer found at 223 °C after 60 minutes (0.78 K/min ramp rate). However, our results show that the phase (Pd_2Si) can readily be found at about 100 °C at 2 °C/min ramping rate. It has been observed in this work (Pt-Si system) that the MBE prepared sample shows the nucleation of the first phase at a lower temperature (30 °C) than the EBE prepared sample. We made use of MBE (preparation of the Pd coated system), with ultra-high vacuum conditions and utilised the RCA cleaning procedure, while the researcher **[112]** used EBE, resulting in the observed temperature difference. This can be attributed to the different cleaning procedure and deposition techniques offering different vacuum conditions, hence there may be some impurities in the EBE prepared sample delaying the nucleation of the first phase.

The Pd_2Si phase, in this work, was observed to be stable in the temperature range studied (up to 600 °C). To complement the results, *in situ* XRD was performed on the 1 cm x 1cm piece of 20 nm Pd -coated silicon sample, cut from the same wafer for the *in situ* real-time RBS sample, with the results given in **figs. 4.27 (a-b)**. The pure Pd main diffraction peak <111> is noticeable at about 40° (2θ), **fig. 4.27 (a)**. The reaction of Pd and Si was observed to have started around 130 °C with the decrease in the palladium peak as shown in **fig. 4.27 (b)**. This confirmed the formation of the Pd rich phase, with Pd_2Si the expected phase according to the *in situ* real-time RBS compositional analysis.

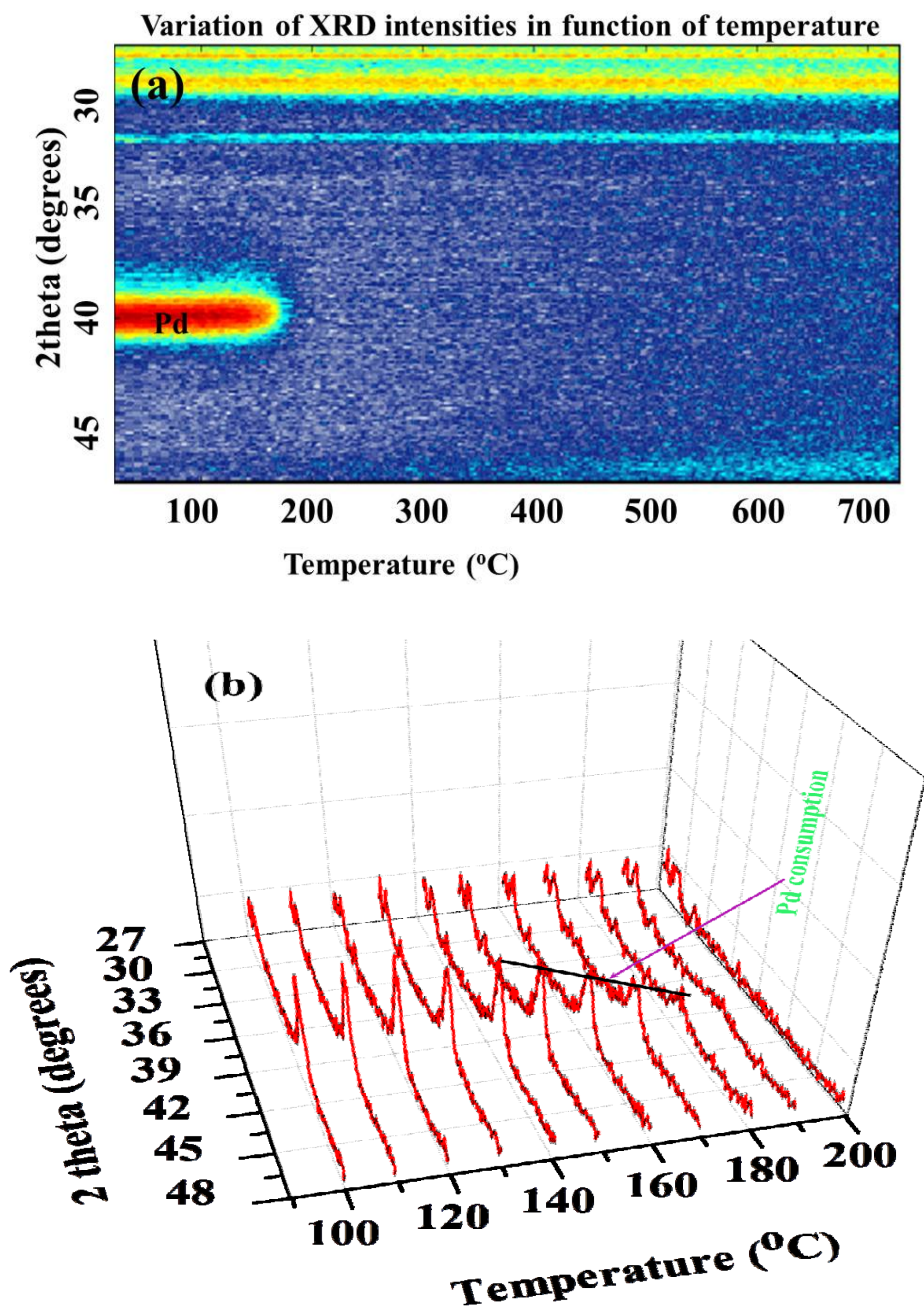


Figure 4.27: *In situ XRD (a) Contour map showing the formation of Pd silicide as a function of temperature (b) Side view of the in situ XRD phase formation.*

However, no additional reflections were observed. As the temperature increased from 130 °C, the decrease in the intensity of the Pd diffraction peak was noticeable and at about 200 °C the peak completely disappeared, however no diffraction peaks corresponding to the expected Pd_2Si phase were observed. The main diffraction peaks of the Pd_2Si phase according to Aronsson *et al.* **[113]** are expected in the range that the *in situ* XRD was carried out (e.g. 2θ = 31.782° (200), 38.113° (111), 41.47° (201) and 42.473 (210)), reference code 01-089-3048. Therefore, from the *in situ* XRD analysis it is tempting to think that the phase formed on the consumption of Pd by the Si substrate is amorphous. It should be mentioned however that there are other reflections of this phase in the extended range of 2 theta diffraction angles, hence a wide range XRD scan was performed on the two samples (the *in situ* XRD and *in situ* real-time RBS analysed samples) and the results are given in **fig. 4.28**. It was observed that the *in situ* real-time RBS sample also revealed no diffraction peaks in the 25° to 48° 2θ range, complementing the results of the *in situ* XRD analysed sample. However, both samples have a diffraction peak at 2θ = 53.345° and this peak matches the diffraction peak of the Pd_2Si with <002> plan orientation. Therefore this observation can be attributed to the growth of the Pd_2Si phase along a <002> plane orientation.

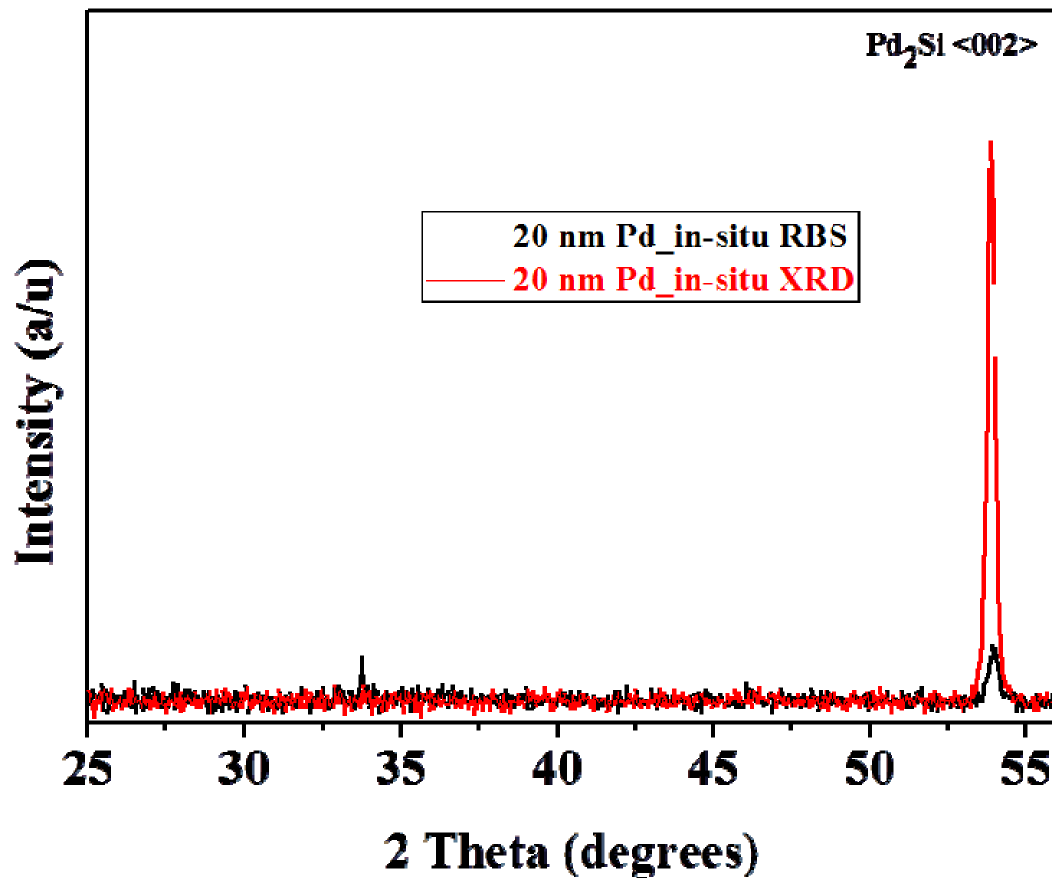


Figure 4.28*: Wide range XRD analysis of the 20 nm Pd coated silicon samples, after in situ XRD (red) and in situ real-time RBS (black).*

4.4.1 Growth of nanowires in palladium-silicon system

This section presents the synthesis of self-aligned polycrystalline Pd silicide nanowires and crystalline Si core-amorphous shell nanowires, synthesised using Pd as a catalyst. In both cases, a thin Pd layer was deposited on a Si wafer using MBE and the system was thermally annealed in different environments, at UHV (which formed Pd-silicide nanowires) and in an argon gas or

argon+methane gas mixture (forming core-shell SiNWs). In both methods the synthesised nanowires were characterised using high resolution electron microscopy techniques.

4.4.1.1 Self-aligned palladium silicide nanowires and nanoclusters

In order to investigate the process of the formation of NWs in a step-by-step way, two (one p-type (111) and one n-type (100)) of the four MBE deposited samples were thermally annealed at 950 °C in Si flux for 2 hours. In the first sample, thermal annealing at a temperature above the Pd-Si eutectic temperature (892°C) affected the Pd layer causing its morphological instability, hence the formation of the silicide droplets through the dewetting layer. The droplets formed act as catalysts for the subsequent NWs growth upon the supersaturation of the droplets with Si vapour. **Figs. 4.29 (a-b)** shows the morphology of the Pd-coated Si (100) substrate after being thermally annealed in the Si flux; the SEM shows the presence of randomly distributed spherical and faceted droplets ranging in size between 200 and 500 nm. In the second sample, Si (111), the droplets were formed as described for the first sample; however, additional Si from the flux diffuses into the droplets causing their saturation and subsequent nanowire growth. The morphology of the sample thermally annealed in the Si flux, is shown in **figs. 4.29 (c-d)**. Despite the two substrates (Si (100) and Si (100)) being exposed to the same amount of Si flux, two types of structures were observed. The structures for Si (100) were only faceted-spherical droplets while elongated wire-like structures for Si (111). The different shapes can therefore be attributed to the influence of the substrate orientation. The Si (111) structures are of distinct rectangular shape with a width of ~ 1 μm and a length between 15 and 25 μm, they are grown in-plane and are specifically orientated with respect to the substrate surface (self-aligned). In addition to the

large nanowires, significantly smaller ones were also observed due to the size being predetermined by the size of the PdS droplets.

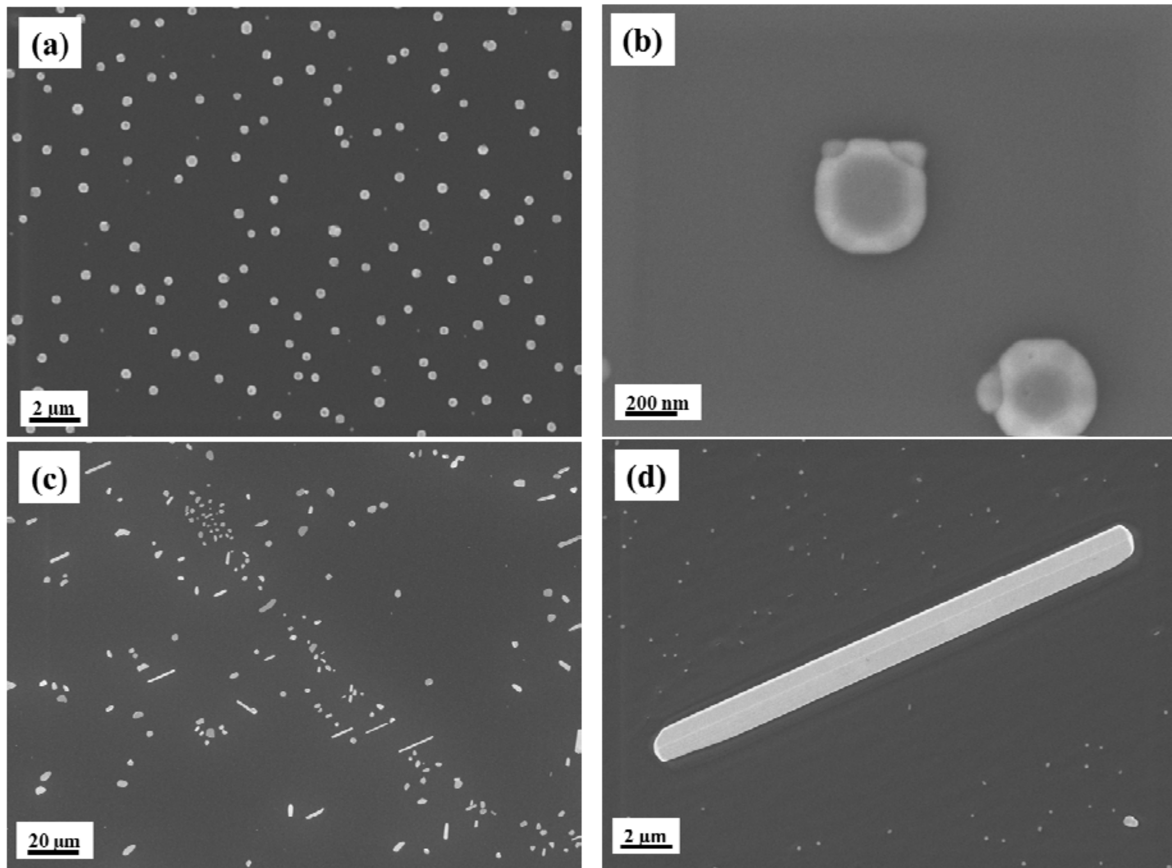


Figure 4.29: *SEM images of Pd deposited on Si after thermal annealing in silicon flux: (a-b) the formation of droplets in Pd-coated Si (100), (c-d) the self-aligned wire-like structures and droplets were observed after thermal annealing the Pd coated Si (111).*

The structural characteristics of both, the droplets and NWs were further investigated by TEM. **Figure 4.30 (a)** shows the bright field (BF) TEM, the annular dark field (ADF) STEM images, and compositional (palladium and silicon) X-ray maps of a droplet partially embedded in the surface of the Si substrate.

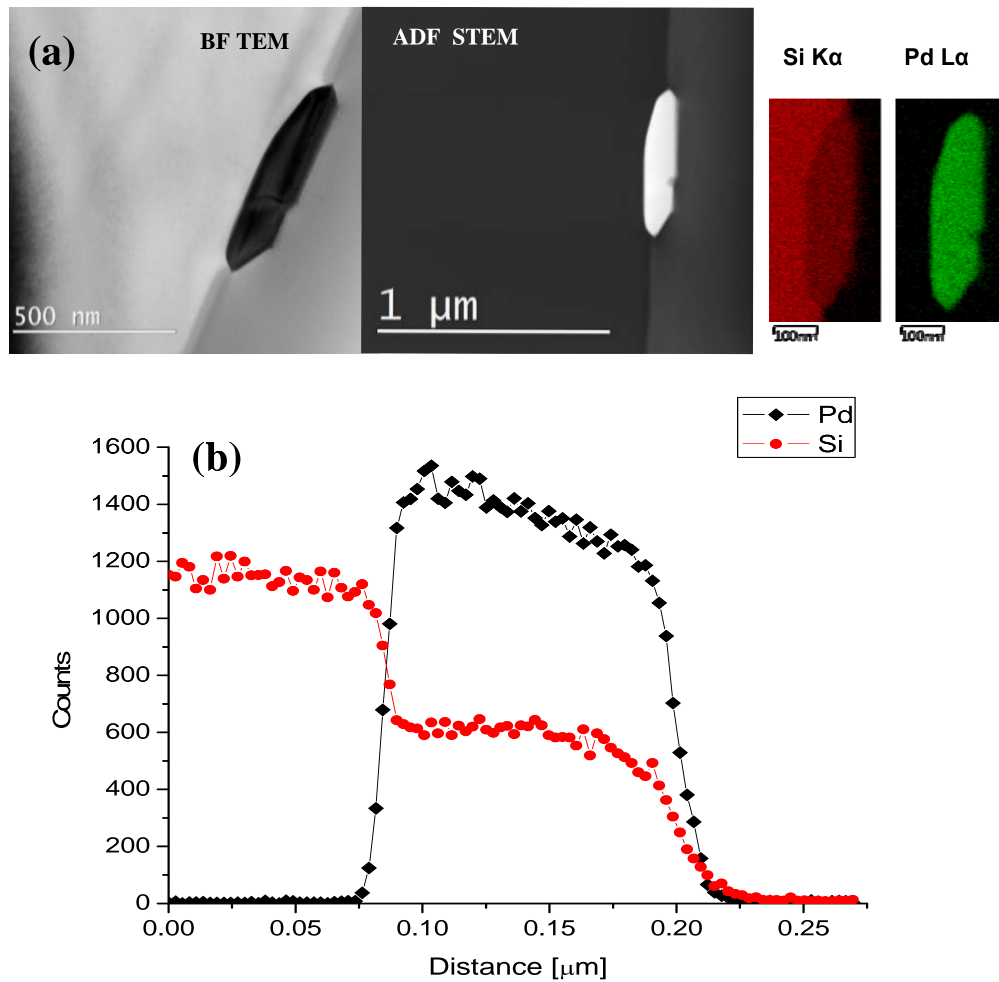


Figure 4.30: *(a) Bright filed (BF) TEM, ADF STEM images and Pd and Si maps taken from a droplet, (b) Variation of Pd and Si concentration across a droplet.*

The contrast shows no indication of strain in the Si surrounding the droplet. The energy dispersive X-ray spectroscopy (EDX) line scan taken across the droplet, **fig. 4.30 (b)**, shows the variation of palladium (1300 counts) and Si (600 counts) indicating the formation of Pd-rich silicide. The ratio of Pd to Si counts roughly corresponds to the stoichiometry of the Pd_2Si phase, the first phase to form in the Pd-Si binary system.

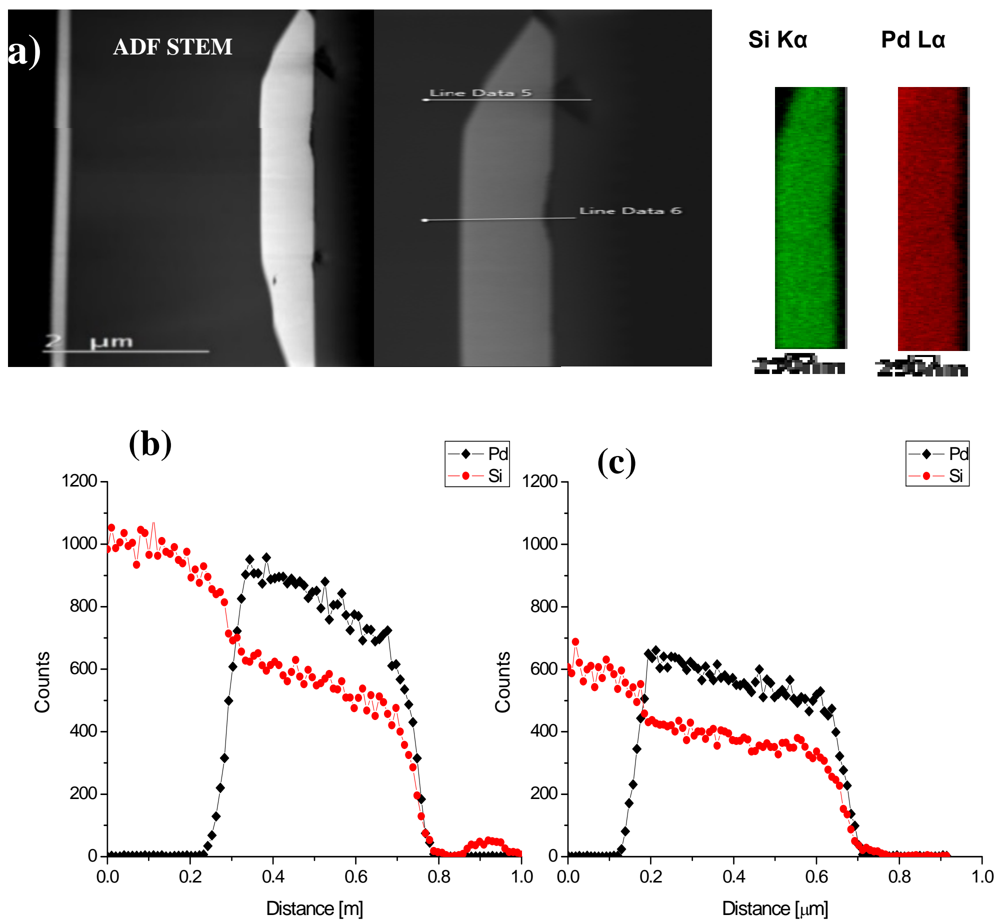


Figure 4.31: *(a) ADF (STEM) images and maps of a NW, and (b-c) EDS line scans showing the Pd and Si concentration gradients across nanowire.*

The detected Pt and Si counts are not surprising as the phase transformation in the Pd-Si system is reversible **[50, 39]**, with Pd_2Si reported to be stable up to around 800 °C and above this temperature, only the PdSi is stable. However, upon cooling below 800 °C the PdSi phase is transformed back to Pd_2Si hence the detected counts in **figs. 4.30 (b)** complements the presence of the Pd_2Si phase. **Fig. 4.31 (a)** shows the ADF (STEM) images and compositional maps for Pd and Si of a nanowire situated close to the surface of the Si substrate. The EDS line, **fig. 4.31 (b)**, scans taken across the NW at two different positions show the compositional variation of Pd and Si: Pd/Si (800/600 counts along the line-1) and (550/400 counts, line-2). These relative concentrations still suggest more counts from Pd as compared to the Si which can also be linked to the stable Pd_2Si. In addition to the compositional analysis, the selected area electron diffraction (SAD) patterns were taken for the same nanowire and substrate material. The SAD patterns, **fig. 4.32**, shows a spotted ring pattern which indicates that the nanowire is composed of a number of small grains with similar crystal structure.

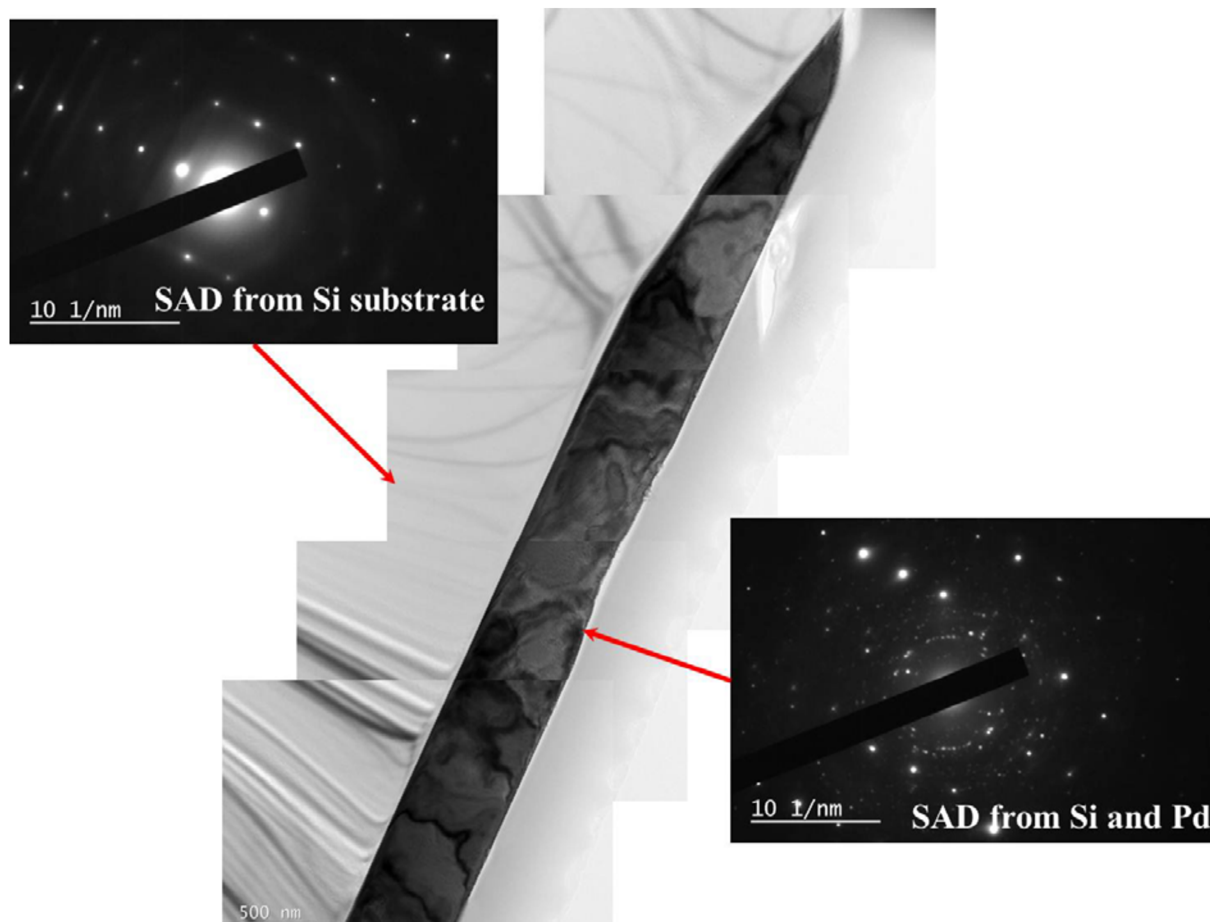


Figure 4.32: *Selected area electron diffraction (SAD) patterns obtained from the Si substrate showing the zone axis [116] (left), and SAD from the Si substrate and NW (right).*

This feature is a signature of the polycrystalline nature of the nanowire which could possibly exhibit metallic type-resistivity of in-plane nanowires. The selected area diffraction (SAD) patterns obtained from the substrate serves as a reference to account for the contribution from the substrate itself when analysing the nanowires using SAD. The contrast surrounding the nanowires shows no indication of strain in the substrate surrounding the nanowire despite the significant difference in the Pd and Si thermal coefficients. This is mainly due to the fact that the

Pd silicide nanowires are formed in-plane and are firmly attached to the substrate surface. The nanowires tend to “select” the orientation that minimises the stress at the wire-catalyst interface. A number of methods for the formation of metal-silicides are reported in the literature **[114-115]**. Most methods for forming metal silicides using Pd, Pt and Ti are directly related to the making of semiconductor integrated device circuits in which silicides are used as electric contacts characterised by lower resistance and better thermal stability compared to SiNWs. Joshi *et al.* **[115]** reported the synthesis of vertically self-aligned nanowires via the VLS mechanism using a microwave plasma enhanced chemical vapour deposition system. The nanowires were grown in an atmosphere of hydrogen and they had a stoichiometry of Pd_2Si.

4.4.1.2 Crystalline core-amorphous shell silicon nanowires using palladium silicide as a catalyst

One of the palladium MBE deposited n-type (100) Si substrates was thermally annealed in Ar as well as $Ar+CH_4$ mixture using a conventional annealing furnace. The SEM micrograph in **fig. 4.33 (a)** shows a large quantity of the wool-like Si nanowire structures still rooted onto the substrate after annealing the palladium coated (20 nm) Si substrate at 1000 ^oC for 5 minutes in an argon atmosphere (300 ml/m). The nanowires were found to have an average diameter of 60 nm with a length up to several tens of micrometres. In addition, a bright contrast at the tips (Pd_2Si silicide) of some of the nanowires was observed, indicated by the red arrows in **fig 4.33 (a)**. Further details of the wires were acquired using a HRTEM, **figs. 4.33 (b-c)**. The TEM micrograph shows a core-shell structure consisting of a crystalline silicon core sheathed with an amorphous SiO_x. Using image J software, the average thickness of the crystalline core and

amorphous shell of these nanowires were approximately 8 nm and 31 nm respectively, giving a total thickness of around 70 nm.

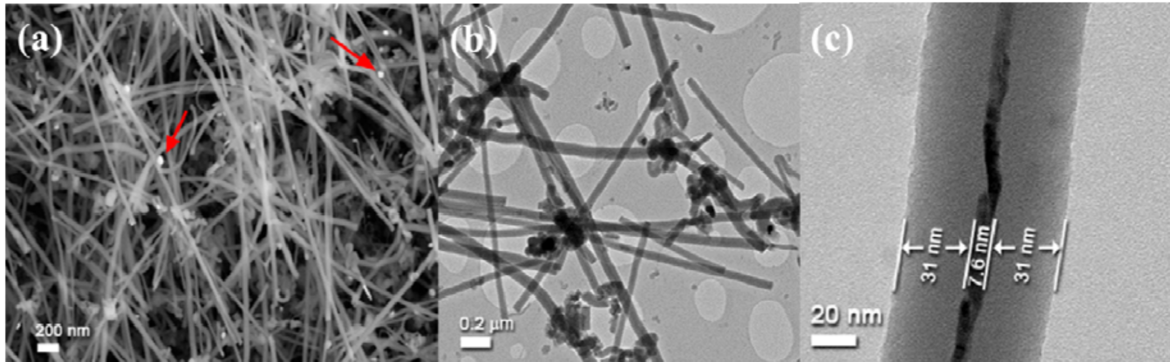


Figure 4.33: *Crystalline core-amorphous shell silicon nanowires obtain by annealing Pd-coated (20 nm) n-Si<100> substrate at 1000 ^{o}C for 5 minutes, in Ar gas (a) SEM image showing SiNWs, (b-c) corresponding TEM images showing SiNWs with their crystalline core and amorphous shell (zoomed image). Arrows are pointing at the SiNWs tips.*

The reduction of the observed SiNW oxidation (31 nm thick oxide layer), during growth, was achieved by carbon incorporation methods. In the first approach, methane gas (mixed with Argon gas) was used. In the second method, the deposition of an amorphous carbon coating onto the palladium-coated silicon substrate was implemented.

Fig. 4.34 (a) shows the SEM micrographs of the sample annealed in a mixture of argon (300 ml/m) and methane (10 ml/m). Although the entire wire grown was coated with an amorphous oxide shell, this outer SiO_x shell layer was heavily supressed from around 30 nm to approximately 9 nm as shown in **figs. 4.34 (b-c)**. Furthermore, the crystalline core of these

nanowires was found to have increased from about 8 nm to around 12 nm. Consequently, the overall SiNW diameter was reduced from 70 nm to about 30 nm.

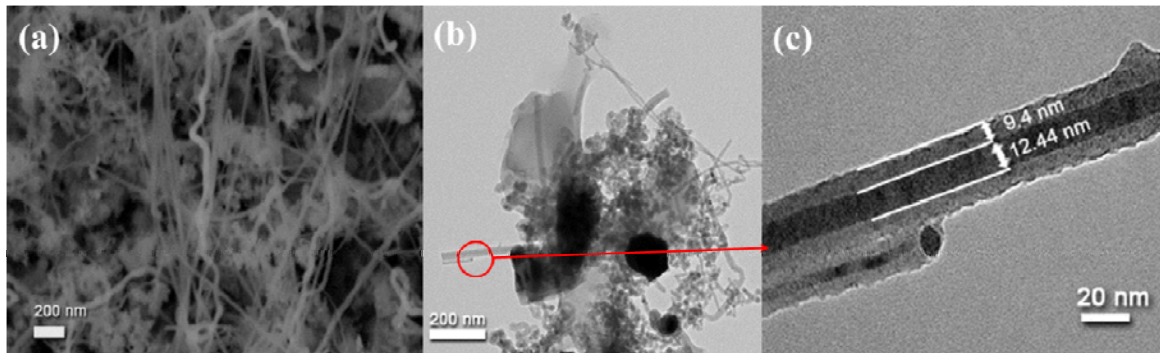


Figure 4.34: *Crystalline core-amorphous shell silicon nanowires obtained by annealing a Pd-coated (20 nm) n-Si<100> substrate at 1000 ^{o}C for 5 minutes, in a mixture of Ar+CH_4 gas (a) SEM image showing SiNWs, (b-c) corresponding TEM images showing SiNWs with their crystalline core and amorphous shell (zoomed image).*

Similar results were obtained with the 10 nm Pd coated Si substrate, annealed at the same conditions, **fig. 4.35**. The SEM image, **fig. 4.35 (a)**, shows a high population of very long nanowires, while the HRTEM reveals their inner structure, **figs. 4.35 (b-d)**. In contrast to the growth of nanowires by the “normal” VSL mechanism, where the Si diffuses from the vapour, the interaction between the droplet and the SiNWs is far more complex under these thermal annealing conditions. As a result, the nanowires consist of a crystalline Si core and a SiO_x shell, as was also the case for Pt. The HRTEM micrographs, **figs. 4.35 (b-d)**, shows that the selected nanowire consists of a highly crystalline core of approximately 11.5 nm and an outer SiO_x shell layer of less than 6 nm. The crystalline core was found to have lattice fringes with a spacing of

approximately 0.19 nm which corresponds to the d-spacing of the silicon crystal structure, (220) plane.

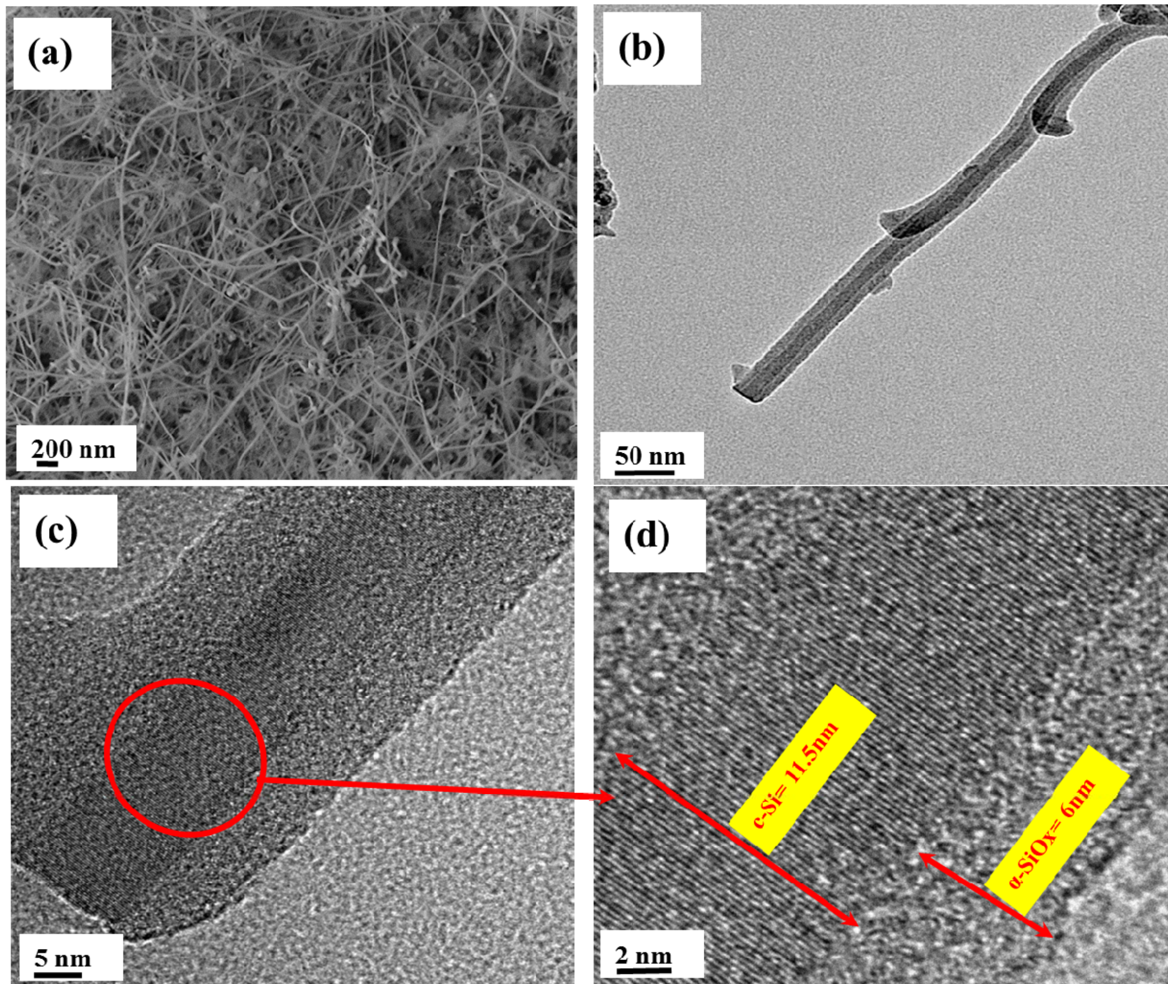


Figure 4.35: *SEM image of SiNWs obtained by thermal annealing in Ar/CH_4 mixture, (a) SEM image showing wool-like SiNWs (b) TEM image showing a single SiNW placed on a carbon film, (c-d) HRTEM of SiNW with a crystalline core-amorphous shell (circled area).*

The observed reduction of the oxide layer was also investigated on the carbon deposited sample. These SiNWs were synthesised using the same experimental parameters, 1000 ^{o}C for 5 minutes in an argon plus methane mixture. The SEM and TEM analyses of the sample are shown in **figs. 4.36 (a-c)**. As was the case for the sample without the carbon layer, large quantities of wool-like SiNW structures were observed on the surface of the Si substrate as well, **fig. 4.36 (a)**. However, a closer look at these nanowires using HRTEM, **fig. 4.36 (b)**, shows the oxidation of the nanowire on one side and an extremely reduced oxide shell on the other side. The crystalline core of the OR SiNWs was about 14 nm, with a total diameter of the nanowire varying from 20 to 30 nm.

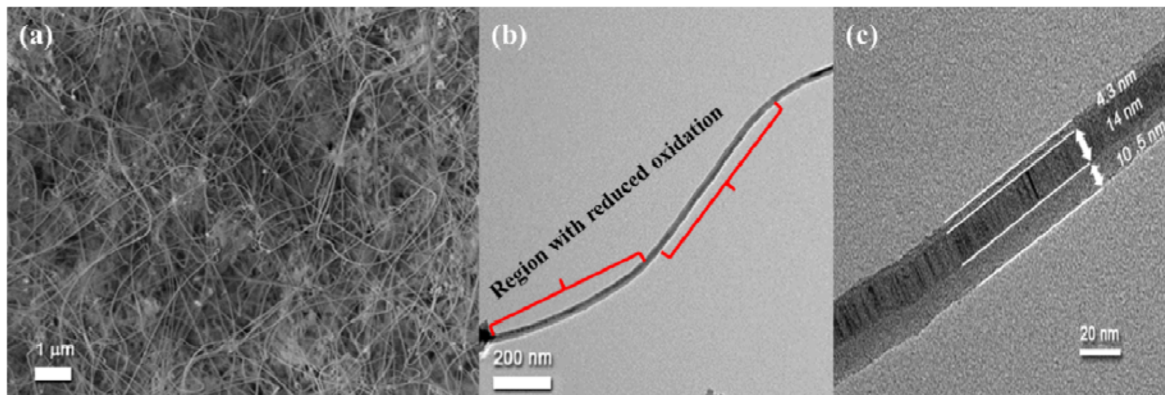
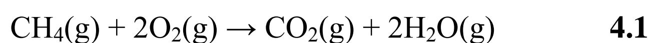


Figure 4.36: *Crystalline core-amorphous shell silicon nanowires obtained by annealing a carbon coated n-Si<100> substrate at 1000 ^{o}C for 5 minutes (a) SEM image showing several nanowires and (b-c) corresponding TEM image showing silicon nanowire with crystalline core and OR amorphous shell.*

This self-limiting oxidation was not observed in the nanowires prepared without a deposited carbon layer, **fig. 4.34-4.35**. The reduced oxide regions of the nanowire are shown in the **figs. 4.36 (b-c)** and appear to be under a compressive stress. The prevention of oxygen diffusion to the Si-SiO_x interface during the SiNW growth can be attributed to the residual stresses in the nanowire. Kao *et al.* **[78]** and Fuzzini *et al.* **[79]** proposed a model that predicts the rate at which the new oxide in the cylindrical structures (e.g. SiNWs) grows at the interface. The model also incorporates the stress-dependent parameters, surface reaction rate coefficient, solid solubility of the oxidants and diffusivity coefficient. They found that, due to the volume of the silicon oxide molecules (45 Å^3) being twice the volume of a single Si atom (20 Å^3), growing oxide in the convex surface results in the stretching of the old oxide as it is pushed out while in the concave surface the oxide is compressed as it is pushed in, resulting in the two opposite stresses, tension and compression, respectively. Therefore, high oxidant concentration in the convex and low in the concave surfaces can be expected. Based on this, the stress observed in the current SiNWs can be attributed to the different exposure of the growing SiNW to the oxidants making the convex surface to oxidise faster than the concave surface. In the current results, we attribute the oxidant limiting mechanism to the following two mechanisms:

Firstly, some oxidant atoms react with the introduced methane gas to form carbon dioxide and water gases, according to the chemical reaction **4.1** below **[116]**.



$$CH_4(g) + 2O_2(g) \rightarrow CO_2(g) + 2H_2O(g) \qquad \textbf{4.1}$$

This reduces the oxidant flux, hence the oxide layer as observed in **fig. 4.34** and **4.35 (c)** when compared to **fig. 4.33 (c)**, where no methane gas was introduced.

Secondly, the increase in the carbon content in the chamber from the deposited carbon layer, introduced another oxidant reduction mechanism according to the chemical reaction **4.2 [116]**.

$$C(s) + O_2(g) \rightarrow CO_2(g) \qquad \textbf{4.2}$$

It is therefore assumed that the presence of the two reactions in the experimental chamber give rise to the different oxidation rates, hence the growing SiNW is exposed to the different oxidant molecules resulting in the observed wires, e.g. **fig. 4.36 (c)**, experiencing both tensile and compressive stresses. The results of the two oxidant reduction methods are summarised in **table 4.5** and compared to the results from literature. The ratio of the amorphous shell (combined shell layers) to crystalline core was calculated and presented in the last row of the table. A drastic decrease in the amorphous shell to crystalline core ratio, from 8.15 to 1.51, was observed when methane gas was introduced into the experimental chamber. The use of methane to reduce the oxidation of the growing SiNWs, during thermal annealing, is therefore proposed according to the chemical reaction 1. The amorphous shell to crystalline core ratio further reduced to 1.06 when a carbon layer was deposited prior to the annealing in a methane mixture. The amorphous shell to crystalline core ratio of the core-shell nanowires synthesised by Li *et. al.* **[70]** is 1.72 which is larger than both ratios obtain from the two methods presented in this work.

The effects of oxidation method can be further explained by estimating the original diameter of the nanowire. It is shown in **fig. 1.4** that the oxide layer of the oxidized structures consist of the two parts, the consumed portion of the original structure, given by $0.445t_2$ while the top part is given by $0.555t_2$, where t_2 is the oxide layer thickness.

Table 4.5: Ratios of amorphous shell to crystalline core of the synthesised SiNWs.

-	**This work (no OR)**	**This work (OR method 1)**	**This work (OR method 2)**	**Reference [70]**
Core-shell (SiNW)	in Ar gas	in $Ar+CH_4$ mixture	in $Ar+CH_4$ mixture plus Carbon layer	Using carbon layer
Core	7.6 nm	12.44 nm	14 nm	20.97 nm
$SiO_{x\ (side\ 1)}$	31 nm	9.4 nm	10.5 nm	18 nm
$SiO_{x\ (side\ 2)}$	31 nm	9.4 nm	4.3 nm	18 nm
Total SiNW diameter	70 nm	30 nm	< 30 nm	57 nm
Ratio of $SiO_{x\ (1+2)}$ to the core	8.15	1.51	1. 06	1.72

We are interested in the consumed portion of the original structure which will be added to the core diameter after oxidation. The initial diameter of the synthesized core-shell structures presented in **figs. 4.33**, **4.34 and 4.36** were estimated to be ~35 nm, ~20 nm and ~21 nm, respectively. The effects of the oxidation reduction mechanism when comparing the initial diameters of the nanowires to the diameters after oxidation can be observed. The first nanowire, which was grown in argon atmosphere, was consumed by the oxidant molecules from 35 nm down to 7.6 nm. However, after introducing methane, almost twice the core diameter (12.44 nm)

was observed, despite the initial core diameter being smaller than the initial diameter of the nanowire without methane. The estimated diameter of the third nanowire was found to be similar to the second one, however, the third wire was exposed to the more oxidation reduction mechanism with the added sputtered carbon. It is this reason that third wire showed better crystalline core after oxidation (~14 nm). This further explains the good effects of carbon based mechanisms in reducing the oxidation of the growing nanowire during SLS growth mechanism, further complements the results presented in **table 4.5**. It should be mentioned that the comparison was performed in many wires for the three experiments and the similar results were observed.

4.4.1.2.1 Electrical properties of FEB deposited platinum contacted oxidation reduced (OR) silicon nanowires

SiNWs with an oxide reduced amorphous shell present a better surface structure allowing for a better metal contact to the crystalline core for transport measurement and any subsequent device integration. A contacted nanowire-device was therefore fabricated (as detailed in **Section 3.3.2**) from the fabricated OR core-shell SiNWs for transport measurements, **fig. 4.37**.

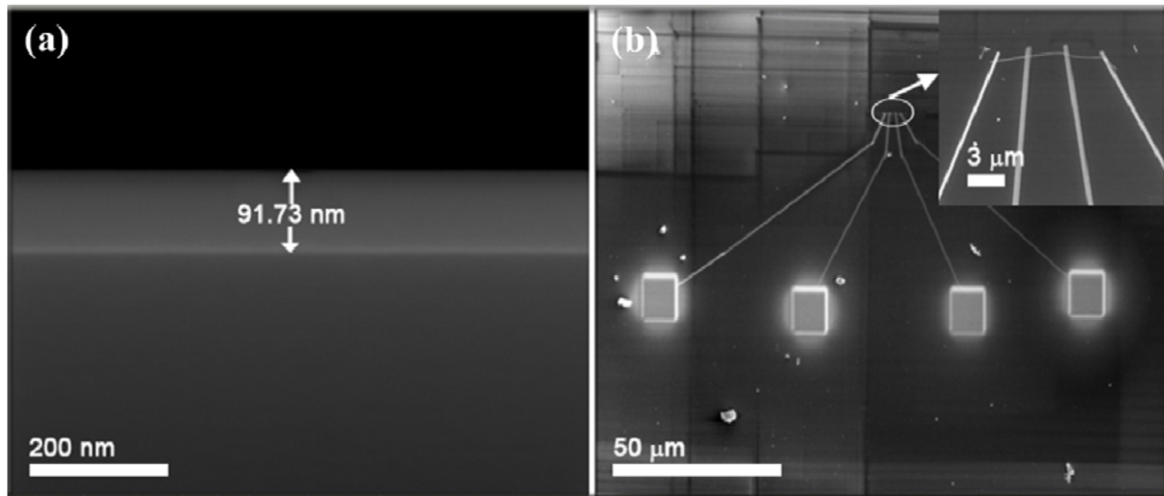


Figure 4.37: *Silicon nanowire device fabrication: (a) oxidised silicon substrate cross-section showing a 92 nm SiO_2 layer (b) palladium-catalysed OR amorphous shell-crystalline core silicon nanowire, along with the contacts for IV measurements. The insert shows contacted nanowire with EB platinum contact lines.*

The SiNW was contacted without any additional treatment such as a hydrofluoric (HF) etch. A device with contacts on the substrate itself without a SiNW (reference sample) was also fabricated to investigate any possible contribution to the measured I-V curve by the transport between the contacts through the substrate or due to any metal contamination during electrode preparation. **Fig. 4.38** shows a four-point probe current versus voltage (I-V) plot of the OR SiNW (spherical dots) and the reference sample (square dots).

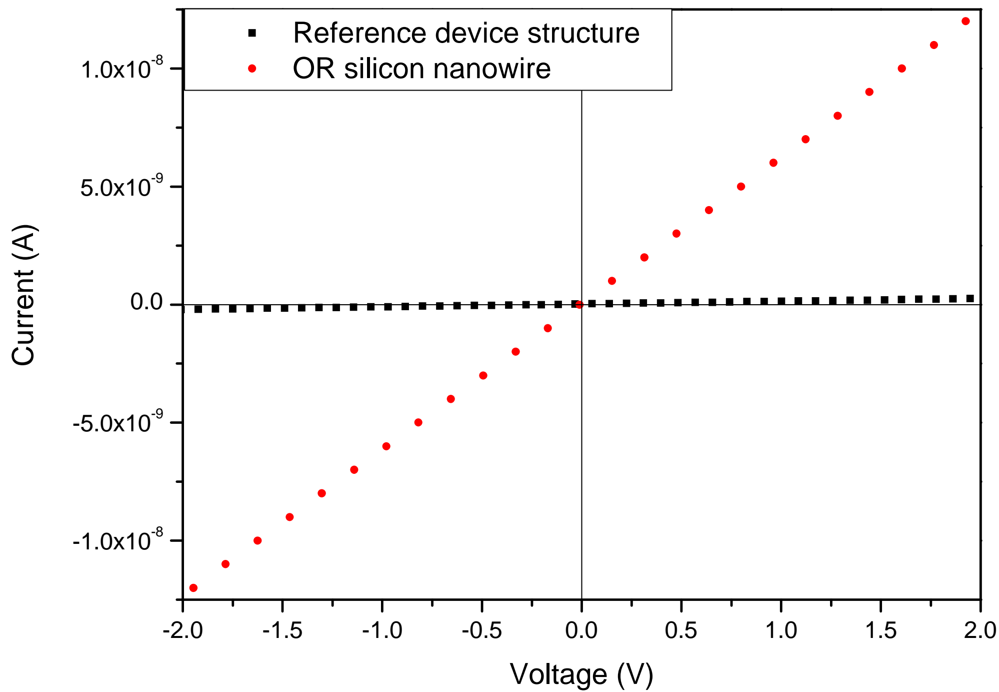


Figure 4.38: *I-V behavior of the 4-point probe nano-device structure recorded at room temperature, OR amorphous shell-crystalline core silicon nanowire (spherical dots) and the reference device sample with no silicon nanowire (square dots).*

The analysis of the I-V data of the nanowire shows a resistance of about 160 MΩ. With the estimated SiNW mean core diameter of 15 nm, the active area of the wire was found to be about 2×10^{-12} cm^2. Therefore a resistivity of about 4×10^{-1} Ω.cm for the tested OR SiNW, having an effective length of 5 µm, was found. On the other hand, a current of less than 0.1 nA (square dots plot) was recorded for the reference sample, **fig. 3.9**, compared to the 12 nA recorded for the silicon nanowire device at the same applied voltage (2 V). With no current expected for this reference sample due to the Si dioxide substrate, the measured current can be tentatively attributed to contamination of the substrate by atmospheric elements as the measurements were

performed under uncontrolled environmental conditions (atmospheric pressure). Prior to the four point probe measurement, two point probe analysis was performed. **Fig. 4.39** shows the I-V characteristics of the OR SiNW at different points (1-2, 1- 3, and 1-4). The Ohmic behaviour was observed indicating an easy flow of electron from the contact structure into the nanowire. The variation in the slopes of different measurements using different contact pads can be attributed to the varying degree of the oxide shell as seen in the SEM images of the OR SiNWs as well as the length of the nanowire (measured at different contact pads). It should be highlighted that, since the work function ($e\phi_m$) for pure Pt is 5.65 eV and the electron affinity for semiconductor Si is 4.05 eV, it is therefore expected that when these materials are brought into contact with each other an energy band diagram described in **section 1.4**, **fig. 1.5**, is expected. For such an energy band diagram, the current-voltage (I-V) characteristics are expected to be identical to that of a p-n junction diode (non-Ohmic behaviour) wherein under reverse bias no current flows from the metal into the semiconductor region. However, **section 1.4** also discussed the possibility of the electrons flowing from the metal into the semiconductor under a reverse bias, changing the non-Ohmic to Ohmic characteristic behaviour. This however is created by contacting a metal to a heavily doped n^+-type semiconductor for which a tunnelling current is possible under reverse bias. This is attributed to a reduced bandwidth as a result of the dopant level in the semiconductor, hence more electrons move from the metal to the semiconductor. The dopant concentration of the produced nanowires could not be unambiguously determined, however, the estimated electrical resistivity was one order of magnitude lower than that of the Si substrate which the nanowires were growing from. This can be a direct indication that the nanowires were slightly higher doped than the Si substrate source and that could be a possible first explanation to the observed Ohmic behaviour characteristics.

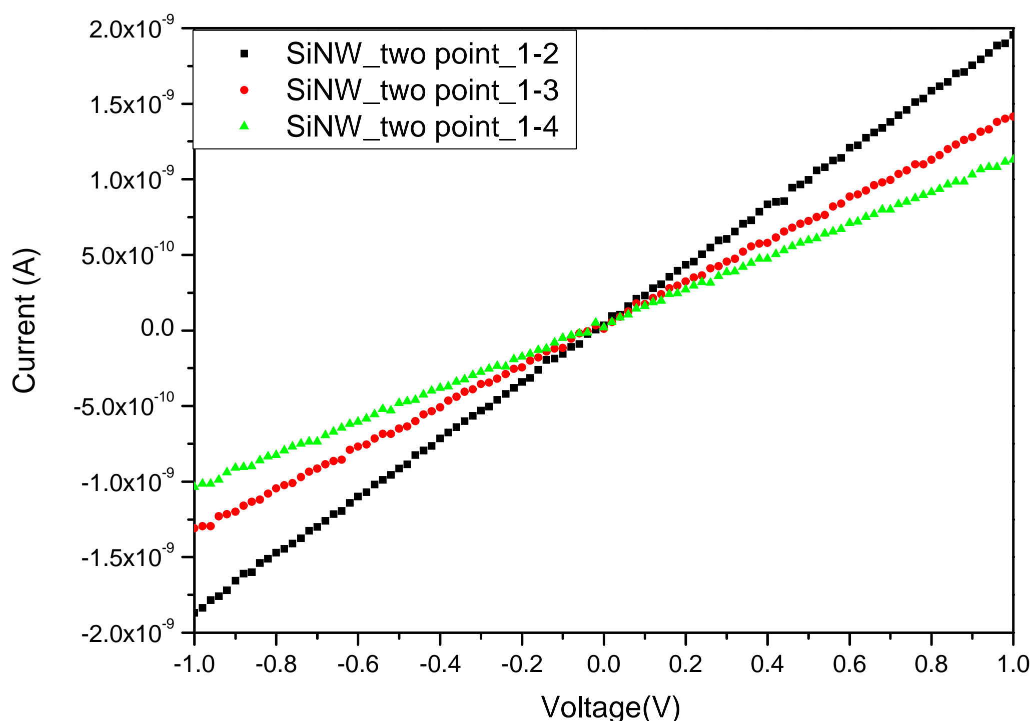


Figure 4.39: *I-V behaviour of the 2-point probe nano-device structure recorded at room temperature for the OR amorphous shell-crystalline core silicon nanowire.*

Another important point to be taken from these results is that the FIB-deposited Pt is not pure but incorporates carbon into the contact structure. It is our view that the contact structure of pure Pt to n-type Si can not be compared to the contact structure of the carbon incorporated Pt contact to n-type Si. This has been explained in the work of Ke *et al.* **[117]**. They have demonstrated that when both n-type and p-type SiNWs are contacted with the focused ion beam deposited Pt contact, Ohmic behaviour can be expected. A very low specific contact resistivity of 1.2×10^{-6} $\Omega.cm^2$ was reported for n-type SiNWs in their report. They however, attributed the unusual low

resistance (Ohmic behaviour) to the amorphization of the SiNW induced by the Ga^+ ion beam irradiation during Pt deposition. They explained the mechanism of current flow (under reverse bias) through the system (FIB-Pt contact/n-type SiNW) by diffusion theory, **eq. 4.2**. Applying this theory, they found a barrier height of 0.015 eV and that the low barrier height was attributed to the Ohmic characteristics of their FIB deposited Pt contact to n-type SiNWs.

$$J_S = q\mu N_c E_s \exp\left(-q\phi_{eff} / k_B T\right) \qquad \textbf{4.2}$$

Where, ϕ_{eff} is the effective barrier height, N_c is the effective conduction band density of states, while μ and E_s are electron mobility and surface electric field, respectively.

In the current work, focused electron beam (FEB), was used to deposit Pt contacts to SiNWs. The FEB technique is believed to be less damaging than the FIB technique which uses energetic Ga^+ ions. From our results, it is therefore believed that the less damaging FEB technique could have also amorphized the area of the SiNW underneath the Pt contact resulting in the easy flow of current observed as discussed in by Ke *et. al*. **[117]**. In understanding our observation and relating it back to the report of these researchers **[117]**, we further investigated the behaviour of the Pt contact to n-type Si, having an amorphous layer between the metal and semiconductor. MBE was used to deposit a multilayer of an amorphous Si and pure Pt on the n-type 1 cm x 1 cm Si substrate, with a mask in the middle to separate the contacts (Pt/a-Si contact to crystalline Si). For comparison purpose, another sample with pure Pt deposited on the masked n-type 1 cm x 1 cm Si substrate was prepared (Pt contact to crystalline Si). **Fig. 4.40** shows the electrical properties of the two prepared samples. As one would expect from the literature in **section 1.4**, when metals like Pt with their work function (5.65 eV) higher that the electron affinity of the n-

type semiconductor (Si = 4.05 eV), the current-voltage characteristics of such materials are nearly identical to that of a p-n junction diode and that is the case with the prepared Pt contact to crystalline n-type Si, black square dot plot. However, with a layer of amorphous Si in between the pure Pt and n-type Si, the current-voltage characteristic is Ohmic, red dot plot. This appears to be in reasonable agreement with Ke *et al.* who attributed similar results to the diffusion theory, **eq. 4.2**, giving rise to a low specific contact resistance as well as very low effective barrier height.

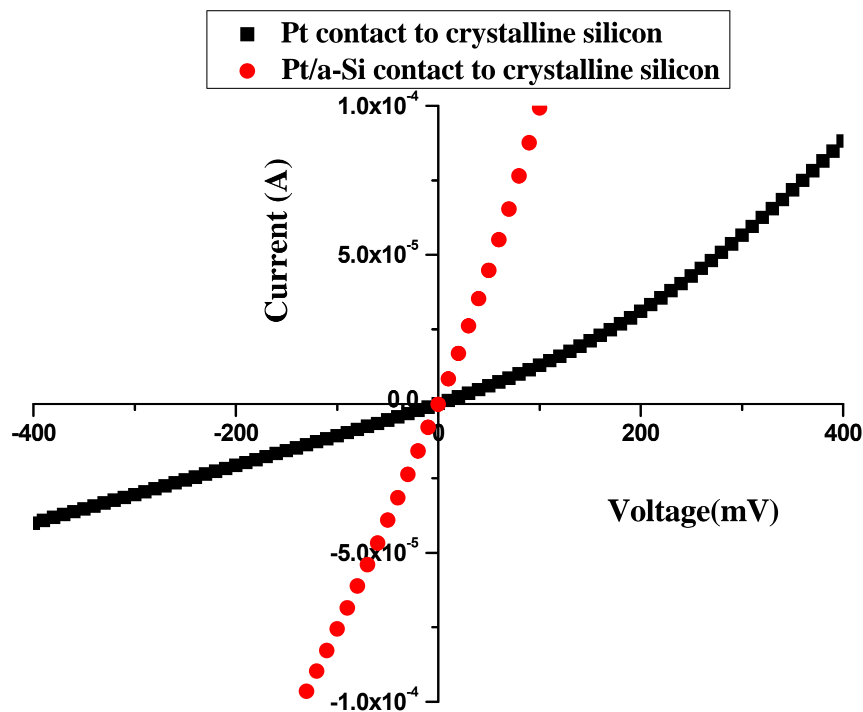


Figure 4.40: *I-V behaviour of the 2-point probe Pt contact to n-type Si and Pt/a-Si contact to n-type Si substrate, recorded at room temperature*

The above **(fig. 4.40)** results may be used to tentatively explain the current flow in our FEB deposited Pt contact to OR core-shell SiNWs **(fig. 4.39)**. With these results, the interface between the c-Pt electrodes and the OR SiNW allows for Ohmic electron transport through the nanowire. This desired outcome can therefore be explained as follows: (1) similar to the ion (FIB) deposited Pt contact **[117]**, the use of an electron beam to deposit c-Pt contact amorphised the SiNW underneath, resulting in less contact resistance and easy flow of electrons from metal to semiconductor under reverse bias, according to diffusion theory as well as the results shown in **fig. 4.40**. (2) The tiny oxide layer of the OR SiNWs would normally contribute to the contact resistance, however, with the use of FEB deposited Pt which incorporates carbon into the contact structure, the dielectric constant of the SiO_x is reduced by changing the Si-O polar bond to a Si-C non-polar bond, allowing for the easy flow of electrons under applied voltages. This is to conclude that the incorporation of carbon modifies the surface of the SiNWs by passivating the SiO shell resulting in excellent performance of the prepared OR SiNWs. Using chemical methods to passivate the oxide shell, Cui *et. al* **[56]** also found an improved field effect transistor device performance. This is in good agreement with our findings. The advantage of our method, however, is that it is a one step process that involves both oxide passivation as well as metal contacting.

CHAPTER 5 DISCUSSION AND CONCLUSION

The aim of this work was to investigate the use of Pt and Pd as catalysts for silicon nanowires (SiNWs) growth, possible interconnect materials (silicide nanowires) as well as contact electrodes. In the first part of the investigation, the reaction between the two precious metals with a Si substrate were investigated in detail for a better understanding of the process leading to the formation of catalyst droplet seeds using complementary techniques. Furthermore, we report on the high possibility of eliminating the health threatening step (the use of hydrofluoric acid) during the core-shell based device preparation.

5.1 Platinum silicide

Molecular beam epitaxy (MBE) and electron beam evaporator (EBE) deposition techniques were used to prepare the coatings (20 nm) on Si substrates. *In situ* real-time RBS analysis confirmed the diffusion and reaction of Pt with Si at 200 °C, for the MBE deposited sample, while at 230 °C for the EBE deposited sample. In both samples, the reaction resulted in the formation of a Pt rich (Pt_2Si) phase with 67 at.% Pt and 33 at.% Si composition. This, in combination with *the in situ* XRD, confirms Pt_2Si as the first phase to form in the Pt-Si system and was found to grow until there was no more Pt available for the growth to proceed. The growth of the phase from the Pt layer reached completion at 240 °C and 260 °C, for MBE and EBE deposited samples, respectively. Furthermore, the phase (Pt_2Si) was found to be stable up to 270 °C (MBE) and 300 °C (EBE), at the same temperature ramping rate, before transforming into the second phase (PtSi monosilicide). It was of the view that, due to the different cleaning procedures and conditions for the deposition techniques (EBE and MBE) used for the two samples, the effect will only be on the first phase to form as the temperature at which the Pt_2Si has fully formed, also favours the

nucleation of the second phase (PtSi). However, the simulation of the spectra (EBE) from ~260 °C to ~290 °C required only one layer with Pt and Si stoichiometry that corresponds to the Pt_2Si phase. Therefore despite reaching the temperature of the PtSi phase formation, there seemed to be some nucleation barriers which can be tentatively attributed to the strain relaxation in the Pt_2Si silicide phase for the formation of the second silicide as reported by Abbes *et al.* **[98]**. The growth of the second phase (PtSi) from Pt_2Si phase reached completion at about 330 °C for both the EBE and MBE samples. The difference in the experimental pressure, $8x10^{-9}$ mbar (MBE) and $5x10^{-6}$ mbar (EBE), was attributed to the observed difference in the silicides nucleation temperatures.

Analysing the Pt-coated samples, cut from the same MBE deposited wafer, using XPS, confirmed only the presence of Pt at room temperature with the binding energy of Pt4f7 level at 71.4 eV. A shift in binding energy of 1.1 eV to 72.5 eV (Pt_2Si) at temperatures 200 °C to 230 °C was observed signalling the formation of the Pt_2Si phase. Furthermore, a shift of 0.5 eV, from 72.5 eV to 73 eV, between 270 °C and 320 °C, signalling the presence of the PtSi monosilicide phase, was observed. The XPS results were found to be in good agreement with the sequential formation of Pt_2Si and PtSi silicides identified using *in situ* real-time RBS. However, the *in situ* XRD showed a delayed formation of these two sequentially nucleating phases, Pt_2Si and PtSi, as they were observed at 270 °C and 330 °C, respectively. The delay however was attributed to the temperature ramping rate (30 °C/min) when compared to the *in situ* real-time RBS (2 °C/min) of the sample cut from the same Pt-coated Si wafer.

In summary we found that upon annealing the Pt-coated Si substrate, Pt_2Si can be expected at 200 °C and it is the first silicide to nucleate in this system. It should be pointed out that to

achieve this low temperature nucleation of this phase, the prior surface preparation and experimental vacuum condition during deposition would need to be carefully controlled. In this investigation, high vacuum conditions could only be achieved using a MBE deposition technique. Furthermore, PtSi monocilicide was found to be the last and most stable silicide of the system. With PtSi being the most stable phase of this system, it has been shown that at high temperatures, the PtSi layer dewetts into droplet structures on the surface of the Si substrate making this silicide a good catalyst for the growth of SiNWs. We found, using PIXE, that when the deposited layer has dewetted due to the annealing effects, the entire Pt species can only be detected in the droplets areas with the Si substrate left uncovered. Therefore the areas in the PIXE image with high Pt intensity are attributed to the areas with droplets necessary to initiate the growth of Si nanowires. EDX, as a complementary technique to PIXE confirmed that such droplets composed of both the Pt and Si elements, making them silicide droplets, in good agreement with *in situ* real-time RBS, XPS and XRD results.

No other silicide is expected to nucleate in the Pt-Si system after the formation of the PtSi and our results are in agreement with the phase diagram of this system. Therefore, when Si atoms are added into these PtSi droplets they precipitate at the interface, initiating the growth of the nanowires. Different techniques were used to incorporate Si into the silicide droplets, MBE, pulsed laser deposition (PLD) and thermal annealing.

Using MBE, it was found that incorporating Si into the droplets on the Si<111> substrate, near the eutectic point (T = 978 °C and 67 at% Si) results in self-aligned faceted PtSi silicide nanoclusters and nanowires. The second method used to incorporate Si flux into droplets was PLD whereby in-plane SiNWs were successfully grown. The PLD technique presents the

advantage of growing the in-plane SiNWs at temperatures lower than the eutectic temperature of the PtSi and Si through the vapour-solid-solid (VSS) mechanism. To the best of our knowledge, the use of PLD to grow Pt-catalysed SiNWs, lateral to the substrate, appears to be a novel result and the approach can be tested using other metal catalyst with even lower eutectic phase transformation temperatures.

The third method used was thermal annealing to which the Si substrate acted as the source of Si atoms to be incorporated into PtSi silicide droplets at high temperature. Using this method, out of plane SiNWs were observed and were grown above the eutectic point of the Pt-Si system (PtSi+Si) and as a result the growth is attributed to the solid-liquid-solid mechanism. Small quantities of the wool-like SiNWs, with diameters of 20 nm to 90 nm were observed. The grown nanowires were consisted of a shell (between 20 nm to 25 nm), about twice the diameter of the crystalline core (11 nm). The incorporation of carbon into the growth chamber, through methane (CH_4) gas, was found to improve the crystalline core of the nanowire. The electrical properties of the synthesised Pt-catalysed SiNWs were investigated. We found that the complexity of the device preparation process, using lithography, may have increased the uncertainty of the results as the devices were less conducting. Given that SiNWs on the same substrate consisted of different thicknesses of oxide shell and that the etching time for the oxide removal was the same for all nanowires on the substrate, some nanowires may have had their shells not completely removed, resulting in different and higher resistivity results. Therefore for future core-shell SiNWs based devices preparation, the etching during the device preparation would have to be eliminated to minimize any arising uncertainty. This can be achieved by etching the nanostructures while still on the substrate. The etching of the nanowire while still on the substrate was implemented in this work and it proved that the oxide shell thickness can be

controlled prior to contact preparation. This will allow for a better selectivity of the nanowires, using SEM techniques, with their oxide shell completely removed for better contacting.

Having observed high device resistance, we investigated the effect of the temperature on the device contact structure. As the device temperature was increased, an improved device performance (I-V linear behaviour as well as current measured) was observed indicating the dependence of the device contact structure to the annealing temperature. We therefore conclude that devices of this nature (Ti/Au contacted SiNWs) would require a testing instrument that allows for the annealing of the structure to high temperatures for the formation of the metal silicide contact with lower contact resistance. Unfortunately, 100 ^{o}C was the maximum temperature available in the system used. Many devices were prepared and showed the same results with the exception of devices with broken nanowires where no current was measured.

It should be highlighted that, the use of hazardous and harmful acids (hydrofluoric) during device preparation is of a concern. We therefore considered looking into methods that can be implemented to eliminate the etching step for future device preparation using lithography techniques. A possibility of contacting the core-shell nanowires without removing the oxide shell was investigated using depth profile (XPS) analysis at different temperatures. Firstly, a metal/SiO_x/Si contact structure was simulated by depositing a Si oxide layer on the crystalline Si substrate followed by a Pt layer. We found that when Pt reacts with Si in the presence of oxygen there is a delay in the sequence that is observed when Pt reacts with Si in the absence of oxygen. The reaction was observed to start at 300 ^{o}C, which was about 70 ^{o}C more when compared to the Pt-coated Si sample, deposited under similar conditions using EBE. The idea here was to track the movement of the oxygen when the reaction starts. We made an observation that, when Pt

starts reacting with Si for the formation of silicides, oxygen diffuses towards the surface. This desirable effect presents a high possibility of contacting the core-shell SiNWs without having to use acids to etch the oxide, hence eliminating the health threatening step (etching).

To investigate this further, a thin layer of Pt was deposited on the core-shell SiNWs. When annealing the prepared sample (Pt coated core-shell SiNWs), decoration of the nanowires with Pt silicide during the inward diffusion of Pt as well as outward diffusion of oxygen was observed. The Pt silicide was therefore found to have made contact to the crystalline core of the nanowires. With the above discussion, we therefore have proposed a reproducible method for eliminating hazardous acids during lithography device preparation of core-shell SiNWs with the use of silicide forming metal.

5.2 Palladium silicide

As in the case with Pt metal, the reaction of Pd and Si was investigated using *in situ* real-time RBS, *in situ* XRD, HRTEM and SEM. For a better understanding of the Pd-Si system leading to the formation of droplets and SiNWs, *in situ* XRD (at 30°/min) as well as *in situ* real-time RBS (at 2°/min) studies of the 20 nm Pd-coated Si substrate were conducted. It was found that the formation of the Pd_2Si phase can be expected at 100 °C and will co-exist with Pd up to 130 °C. The phase (Pd_2Si) was stable in the temperature range studied (600°C). Using *in situ* XRD, we observed the reaction of Pd and Si to start around 130 °C and the difference was not surprising due to the higher temperature ramping rate (30°/min versus 2°/min in the *in situ* real-time RBS analysis). The XRD results confirmed the growth of the Pd_2Si phase along a preferred (002) plane orientation, with only one diffraction peak at $2\theta = 53$ for both samples.

For the growth of SiNWs using Pd as a catalyst, thermal annealing was used. Similar to the Pt metal, the HRTEM micrograph showed a core-shell structure consisting of a crystalline Si core surrounded by an amorphous shell (SiO_x). However, the high density wool-like core-shell SiNWs in comparison to the small density of the Pt catalysed core-shell SiNWs were observed. This is attributed to the difference in the silicide eutectic temperatures of the two systems, 892 °C and 979 °C for L→PdSi+Si and L→PtSi+Si, respectively. The core-shell SiNWs catalysed by these systems were growing at 1000 °C which is 21 °C above the eutectic temperature of the Pt-Si system and 108 °C above the eutectic temperature of the Pd-Si system, as a result high density of Pd silicide nanowires were observed. In trying to improve the density of the Pt catalysed nanowires, growth time had to be increased. For both metals, the growth of the nanowires was attempted below eutectic temperatures and no nanowires were formed. Therefore, nanowires were grown from the PtSi and PdSi liquid phases making the growth process solid-liquid-solid with observed silicide nanowire tips.

The average diameter of the crystalline core of the synthesised Pd silicide core-shell nanowires was ~ 8 nm while the thickness of the amorphous shell was found to be approximately 31 nm. Seeing the thicker oxide shells in these nanowires, which was also the case for the Pt catalysed SiNWs, two oxide shell reduction methods (carbon incorporation) were implemented. In the first method, a mixture of methane and argon was used while in the second method amorphous carbon was sputtered on the Pd-coated Si substrate and the methane-argon gas mixture was used as a carrier gas. The first method (methane-argon gas mixture) was found to have reduced the outer SiO_x shell layer to approximately 9 nm, with an increased crystalline core (12 nm) when compared to the 31 nm (shell) and 8 nm (core) observed in the sample with only argon gas used. The second method appeared to have heavily supressed the oxide layer with an estimated 14 nm

crystalline core. The two reported methods limit the oxidants molecules resulting in the oxide reduced (OR) layer in the produced nanowire. Furthermore, the second method also exposes the growing SiNWs into different rate of oxidation limiting mechanism according to reaction 4.1 and 4.2, hence the wire experiences different types of stresses (tension and compression) as described in **section 1.4**, **chapter 1**. This was further explained by estimating the initial core diameter of the nanowires. The rate of oxidation in the nanowire with only argon used as a carrier gas was found to be high, resulting in the initial diameter of the nanowire to be consumed to about 8 nm from 35 nm while its total diameter increased to about 70 nm due to the thicker oxide layer. The incorporation of carbon proved to have limited the oxidant molecules resulting in the initial diameter to be consumed to 12 nm from 20 nm while the third wire with increased carbon content showed that the initial diameter was reduced to 14 nm from about 20 nm.

5.3 Nanowire growth summary

5.3.1 In-plane nanowires

The results of this study show that two types of NWs can be synthesised using Pd or Pt as metal catalysts depending on the fabrication method and the diffusion mechanism involved during growth. Two experimental approaches were adopted and in the both cases NWs were synthesised, however, they significantly differ from each other in terms of their size, shape, crystallinity and composition.

In the first nanowire method, when the annealing process was performed in the presence of a Si vapour phase, self-aligned (in-plane) NWs were formed. Depending on the technique used, the nanowires were found to grow through a vapour-liquid-solid diffusion mechanism (MBE growth technique) and VSS diffusion mechanism (PLD technique). For the VLS growth mechanism, the

Si present in the vapour phase supersaturates the droplets, and ultimately results in the lateral growth of PtSi or Pd_2Si nanowires through Ostwald ripening of the thermomigrating silicides of these metals. The produced nanowires in this approach were rectangular in shape, relatively short, and fully crystalline (polycrystalline). Via the use of electron beam lithography techniques and standard cleanroom wet chemistry, the PtSi and Pd_2Si nanowires can be readily incorporated into nanoelectronic devices for application in field effect transistors as well as in the direct development of Schottky barrier photodetectors. PtSi and Pd_2Si silicide thin films are currently popular in the production of such photodetectors and these nanowires present opportunities for investigating the advantages of lower dimensional PtSi material in the performance of photodetectors. Further work is required to determine the electrical and optical characteristics of these nanomaterials. In determining the electrical properties of these nanowires in their current state (PtSi silicide nanowires on the p-type Si substrate), it should be highlighted that there may be small uncertainty in the results. P-type Si is known to create good Ohmic contacts (low schottky barrier ~ 0.2 eV) with PtSi silicide which may result in a possible current leak to the substrate. However, the leak is expected to be minimal considering that the flow of electrons will choose the path with lowest resistance, that of the highly conducting silicide nanowire (R_{nw}), rather than the higher resistance, the interfaces of the PtSi silicide and substrate ($R_{i\text{-}Si}$), $R_{nw} <<< R_{i\text{-}Si}$. However, the most viable option would be the growth of these materials on a range of Si substrates (doped n-type, and intrinsic Si (111)) to produce different electrical and optical wire characteristics in an attempt to improve the performance of the material for different applications. Growing the nanowires on n-type Si (111) substrate presents a higher Schottky barrier contact to PtSi (~ 0.8 eV). It is known that this will result in diode characteristic contact behaviour with low resistance if biased in one direction and very high resistance if biased in the

opposite direction, **see section 1.4**. The idea in this approach would be to test the device below the threshold voltage of the Si based diodes characteristic (~ 500 mV) to avoid any possible current leak for the direction with a low resistance.

Contrary to the incorporation of Si flux using PLD, in-plane SiNWs catalysed by PtSi droplets were successfully grown through the vapour-solid-solid mechanism at temperatures lower than the eutectic point of the catalyst.

5.3.2 Free standing nanowires

In the second method, when thermal annealing was performed in an argon-methane mixture, free-standing nanowires were formed for both metal catalyst (Pt and Pd). Their growth occurs via the SLS mechanism. The source of the Si is different in this case; elemental Si diffuses from the substrate material and serves as the source for nanowire growth. A large (Pd) and small (Pt) population of nanowires was observed. The nanowires grew into a "wool" like form, were very long and thin, and they consisted of a crystalline Si core and amorphous SiO_x shell. The oxidation reduction mechanism, producing oxide reduced (OR) SiNWs, was implemented by means of carbon incorporation in the nanowire growth chamber. This method was successfully demonstrated during the growth of Pd-catalysed SiNWs.

An argon-methane gas mixture was found to reduce the oxidation of the grown nanowires, resulting in a 1.51 ratio of the amorphous to the crystalline core. A combination of this gas mixture (argon-methane) with a carbon layer heavily suppressed the formation of an oxide shell around the SiNWs further, with a 0.96 ratio of amorphous to crystalline core. Electrical transport measurements of these OR SiNWs was investigated and to the best of our knowledge, we have

reported for the first time on the electrical properties of a focused electron/ion beam fabricated OR amorphous shell-crystalline core SiNWs heterostructure (1) without the passivation of the oxide shell surrounding the core, using chemical methods (e.g. 4-nitrophenyl octadecanoate), (2) without the thermal annealing of the fabricated device and (3) without the removal of the oxide layer, using dangerous acids such as HF. The nanowires showed good electrical properties with a resistivity of about 4×10^{-1} Ω.cm and presents a viable material for easy device fabrication and integration.

As an additional electrical property of the prepared core-shell OR-SiNWs based device, further testing to determine the effect of the device gate voltage on the conductance may be performed. This will complement the obtained low resistivity of the device and determine the carrier mobility of the synthesised and highly conducting core-shell OR-SiNWs.

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