ON THE WAVEFORM FIDELITY OF BROADBAND DIGITAL STORAGE ARCHITECTURES

by
T. W. Küsel

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Synopsis

Recent advances in digital technology resulted in the advent of high-density, very large-scale and very high-speed integrated circuit devices. For the first time it has become viable to store and/or process digitally sufficient lengths of very broadband signals. The digital capturing, storage and processing of a signal has some obvious advantages over traditional analogue methods. Given such a digital receiver technology, the system designer has at his disposal complete, real-time, receiver and processor reconfigurability. In this thesis, a number of architectures for the digital capture, storage and reconstruction of broadband signals are investigated. A comparison of these architectures is made, based on the fidelity of the reconstructed signal. Techniques for improving the quality of the reconstructed signal are also investigated. The results are aimed at aiding the system designer in choosing a receiver architecture for a specific system requirement.

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List of Abbreviations

A/D	-	Analogue-to-Digital
AE	-	Amplitude Encoding
AGC	-	Automatic Gain Control
BDR	-	Broadband Digital Repeater
BPF	-	Band-pass Filter
BW	-	Bandwidth
CW	-	Continuous Wave
D/A	-	Digital-to-Analogue
dB	-	Decibel
dBc	-	Decibel with reference to carrier power
DFT	-	Discrete Fourier Transform
DHT	-	Discrete Hilbert Transform
DRFM	-	Digital Radio Frequency Memory
DSSM	-	Digital Single Sideband Modulator
EBAE	-	Extended Bandwidth Amplitude encoding
EBPE	-	Extended Bandwidth Phase encoding
ECM	-	Electronic Countermeasures
FFT	-	Fast Fourier Transform
FM	-	Frequency Modulation
FML	-	Frequency Memory Loop
GaAs	-	Gallium Arsenide
I	-	In-phase
IF	-	Intermediate Frequency
ILS	-	Interlaced sampling
IM	-	Intermodulation
LO	-	Local oscillator
LPF	-	Lowpass Filter
PDS	-	Power Density Spectrum
PE	-	Phase Encoding
PSK	-	Phase Shift Keying
Q	-	Quadrature
RAM	-	Random Access Memory
RF	-	Radio Frequency
S/N	-	Signal-to-Noise ratio
SSB	-	Single Sideband

Chapter 1

Introduction

1.1 Aim

This thesis is aimed at comparing different techniques to store and recall broadband signals digitally. The main focus of this comparison is the waveform fidelity of the recalled signal. Different signal properties defining this 'fidelity' are thus investigated in detail, and the different storage techniques are then compared on the basis of these signal properties. It is therefore a further aim of the thesis to investigate existing techniques to improve the waveform fidelity of the output signal. Since digital frequency translation techniques are often used in such architectures, it seemed prudent to investigate such translation techniques, and their effect on the waveform fidelity. The eventual goal is to provide a system designer with a reference of advantages and disadvantages for each architecture, in order to be able to make a choice on a specific architecture for his system.

1.2 Scope of the work

A literature study (presented in Chapter 2) has been conducted to determine existing techniques to digitally store and recall broadband signals, the possible advantages and disadvantages of each, as well as typical criteria which are used to compare the techniques. A brief history of previous techniques used as well as an overview of state-of-the-art technology is included in Chapter 2. It gives a background to the problem of the storing of broadband signals, including a summary of the problems caused by coarse quantization and sampling. Limitations in terms of bandwidth and waveform fidelity of such signals are also discussed. A description of all viable architectures is given, as well as the criteria, in terms of hardware and signal properties, which are used to compare these architectures.

Since simulations are used for the greatest part of the comparison, it is important to know the simulation limitations in terms of hardware and software, as well as the actual parameters used. Chapter 2 continues to give a background to the simulations, in which their limitations are described in terms of frequency resolution, simulation sampling frequency etc. It is also important to know how to model each system component. Some components can be considered ideal, others have to be modified in order to make the simulation results more applicable to practical implementations. A short description of the simulated components, the induced component imperfections, as well as other factors that have an influence on the simulation results, is given.

In the main body of the thesis (Chapters 3 to 7), the simulation results are discussed. These results are presented in terms of the output waveform fidelity and bandwidth limitations.

Chapter 3 concentrates on the spurious signal level of the stored signal. A number of different sources and their contribution to the total spurious signal level are discussed. Special attention is paid to spurious signals introduced by coarse quantisation and sampling. Results of practical measurements are included, and compared to the simulation results. An interesting outcome of the literature study described in Chapter 2 was a proposal for a technique [12] - [15] for reducing spurious levels in the storage process. Simulations were done to compare this technique to conventional methods. A description of these proposed spurious reduction techniques as well as simulation results are presented.

The phase and frequency accuracy with which the incoming signal can be stored and reproduced, is discussed in Chapter 4. Phase jitter, which is also very dependent on quantization coarseness, is one of the most important system considerations discussed in this chapter.

The frequency response and instantaneous bandwidth of the different architectures are described in Chapter 5. Interlaced sampling is often used to increase the bandwidth of such systems. The problems introduced by this method of bandwidth extension are discussed in this chapter.

Waveform fidelity is not easily defined. A more thorough investigation than purely spurious levels and phase jitter for a single-tone input is usually required, especially when considering a typical wideband receiver, in which case the quality of the incoming signal is determined by the receiver output. Chapter 6 attempts to compare the waveform fidelity of the different encoding architectures from a receiver point of view. A matched filter receiver is used as a basis for the comparison.

In many applications it is necessary to induce a frequency translation in a signal. In Chapter 7 one or more ways of achieving such a frequency shift are suggested for each encoding architecture. These techniques inherently induce further waveform distortions, especially in the case where such a translation is achieved by using digital techniques. Simulations were done in an attempt to quantify these distortions. The results of these simulations are discussed in this chapter.

Chapter 8 summarises the results of the detailed investigations in the form of a table. Areas requiring further investigation are outlined.

Chapter 2

Literature study and background

The broadband digital repeater (BDR) is specialised hardware that is able to store very broad bandwidth signals digitally and recall them at any desired time. The fidelity of the recalled signal depends on numerous factors, each of which will be discussed in detail in this dissertation. After storage, the digital data may be manipulated as desired:

- The stored signal may be read out at any time or as often as desired without any degradation in quality as a function of time.
- The stored signal may be read out of memory at any speed and used in slower digital processing units for more thorough analyses of such broadband signals.
- Continuous wave (CW) signals may be generated by continuous read-out of a single signal cycle.

The versatility of the BDR makes it useful for many applications. Some of these applications include the storing of short RF pulses, television pictures, and also for applications in digital oscilloscopes. The BDR may also be used to synthesise broadband pulses. One of the great advantages is that complex, phase encoded waveforms may be handled with ease, making it useful for the analysis and synthesis of such signals. By applying the appropriate digital transforms, filter functions can also be created that have no simple analogue equivalent for handling special receiver and environment interaction.

One of the BDR's most common applications is found in the military market, where it is used as an electronic countermeasure to protect aircraft from enemy radar. The Digital Radio Frequency Memory (DRFM) is used to store an incoming enemy radar signal and recall it (once or several times) after a time delay, thereby deceiving the enemy radar's range estimations. The BDR is very successful in this field of operation, even for modern radar's using complex phase-encoded signals. The BDR can also be used to induce a Doppler shift in the signal, thereby deceiving the target velocity estimations of the radar.

Most of the work published on this topic was found in articles and patents, and was either very brief and incomplete or considered at most two of four possible architectures. It was therefore necessary to find all existing architectures, summarise existing facts and to investigate their system characteristics further by means of simulations.

2.1 HISTORY AND APPROPRIATE TECHNOLOGY SURVEY

Prior art of the storage of signals at radio frequencies, and specifically storage of pulses of microwave energy, has been short-term storage, at best. This has been accomplished by means of:

- delay lines,
- distributed electrical parameter delay lines and
- recirculating delay lines.

These delay lines were used to simply capture the incoming signal, delay it, and retransmitting it once (or several times by means of a circulating delay line). These devices clearly have some severe limitations in terms of signal storage length, signal processing capability, and the ability to repeat the stored signal after long delays or at electronically controlled intervals.

These shortcomings, together with the technology advances in high speed digital storage devices, led to the development of the first DRFM devices in the early seventies [24]. Their original use was simply to replace the recirculating microwave memory. The early models had limited bandwidth and memory size with few ECM functions. As the potential of the DRFM became better understood, additional ECM functions were incorporated. Bandwidth and memory size capabilities have also increased dramatically. Modern DRFMs (circa. 1994) exist with instantaneous bandwidth capabilities in the order of 1000MHz and with total memory lengths in excess of 340 microseconds [1]. A number of producers compete in terms of instantaneous bandwidth, memory length, signal quality (number of bits quantisation), throughput time, physical size and weight, etc.

Speed still appears to be a significant factor driving DRFM technology. Important operational benefits are expected with the introduction of gallium arsenide (GaAs) digital microcircuits. Another promising area of research is to achieve digital modulation over both the amplitude and phase of the captured signal on a sample-by-sample basis. Ultimately, all the required converters, memory and control functions will be placed on a single chip [1].

New developments (circa. 1993) in the area of RF memories include patents on coherent optical RF memories [2] and optical acoustic charge transport devices[3]. These developments seem to move away from digital devices in order to utilise the high speed capabilities of optical signal processing.

2.2 PROBLEMS INVOLVED IN THE DIGITAL STORAGE OF BROADBAND SIGNALS

According to the Nyquist sampling theorem, a minimum sampling rate of $2B$ Hz is required for the sampling of a signal with a B Hz bandwidth. For broadband input signals, this requires extremely high speed analogue-to-digital (A/D) conversion, digital-to analogue (D/A) conversion and digital data processing. The instantaneous bandwidth of the BDR is therefore usually limited by the A/D conversion speed. Flash A/D converters are commonly used to obtain a fast conversion speed. The hardware complexity of flash converters increases rapidly with an increase in the number of bits used. As a result, coarse quantization is usually used in wideband BDR architectures.

Another (usually not as critical) complication resulting from the high speed sampling is that the capturing and storing of a signal of only short duration uses up relatively large amounts of memory space. In some (for example military) applications where physical space, power consumption, etc. are major considerations, the issue of memory space can also become an important one.

While reducing A/D conversion complexity and memory space requirements, signal fidelity is lost due to the coarse quantisation. The coarse quantisation, together with the sampling, induces unwanted spurious signals which cause the recalled signal to be of poorer quality than the incoming signal.

The storing of broadband signals therefore becomes a trade-off between *instantaneous bandwidth* (sampling rate), *stored signal length* (memory size) and *signal quality* (number of quantisation bits).

At the end, it is the BDR architecture which will determine the signal fidelity of the system once the abovementioned trade-offs have been chosen. Each architecture has its advantages and disadvantages in terms of bandwidth and signal fidelity. It is thus the aim of the thesis to compare these architectures on the basis of such criteria. The architectures are described in the following section.

2.3 DESCRIPTION OF ARCHITECTURES

As previously mentioned, four basic configurations are being referred to in the literature. In the following sections a block diagram and short description of each configuration is given.

2.3.1 Amplitude Encoding (AE)

Figure 2.1. shows the basic block diagram of the AE architecture. It usually consists of two down-conversion stages, an IF stage and two up-conversion stages. The incoming signal is demodulated to IF by two mixers and two local oscillators. The IF signal is then filtered by a lowpass filter to prevent aliasing in the sampling process (i.e. the IF is filtered to the Nyquist bandwidth, i.e. half the sampling frequency). It is then sampled and quantised by a conventional A/D. After digitisation, the data is sometimes demultiplexed or pipelined (not shown in the block diagram) in order to reduce data rates, thus making it more compatible with the operating speed of the memory module. The data is then stored in random access memory (RAM), which is usually managed by a memory controller to regulate storage space, addresses, delay times and other desired amendments to the data. In the recalling process, the data is multiplexed into the D/A and filtered to the same band as for the first lowpass filter. The baseband signal is then modulated by the first mixer and local oscillator. After the first up-conversion stage, the lower sideband is filtered out by a bandpass filter, after which the final mixer stage modulates the signal to the original input frequency.

By using a frequency detector to estimate the centre frequency of the incoming signal, the frequency of the first local oscillator can be tuned to the desired RF band in order to be able to capture signals over a wide range of input frequencies.

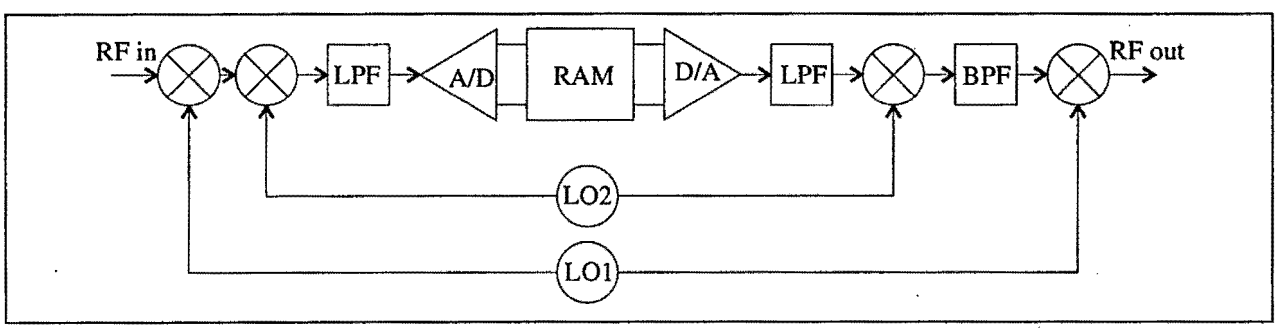

Figure 2.1. *Block diagram of AE architecture*

2.3.2 Extended Bandwidth Amplitude Encoding (EBAE)

The EBAE configuration (*Figure 2.2*) has only one down-conversion and one up-conversion stage. The second mixer stage is not needed because it is not necessary to filter out the sideband signal. This is done by adding or subtracting the quadrature channels in order to cancel the upper or lower sidebands. This concept is described in more detail in *Section 3.2.1.* The incoming signal is split up by a power divider and quadrature mixer into an in-phase (I) and quadrature (Q) channel. Since the sideband is suppressed by the mixing process, the input signal is down-converted to baseband rather than IF, as was

the case in the AE configuration. The baseband stage of each channel has basically the same operation as the AE configuration described above. After quadrature up-conversion, the sum/difference of the I/Q channels yields the desired output signal. The cancellation of sidebands by quadrature up- and down-conversion provides the EBAE configuration with a factor 2 bandwidth advantage over the AE configuration for the same sampling frequency - hence the name of this architecture.

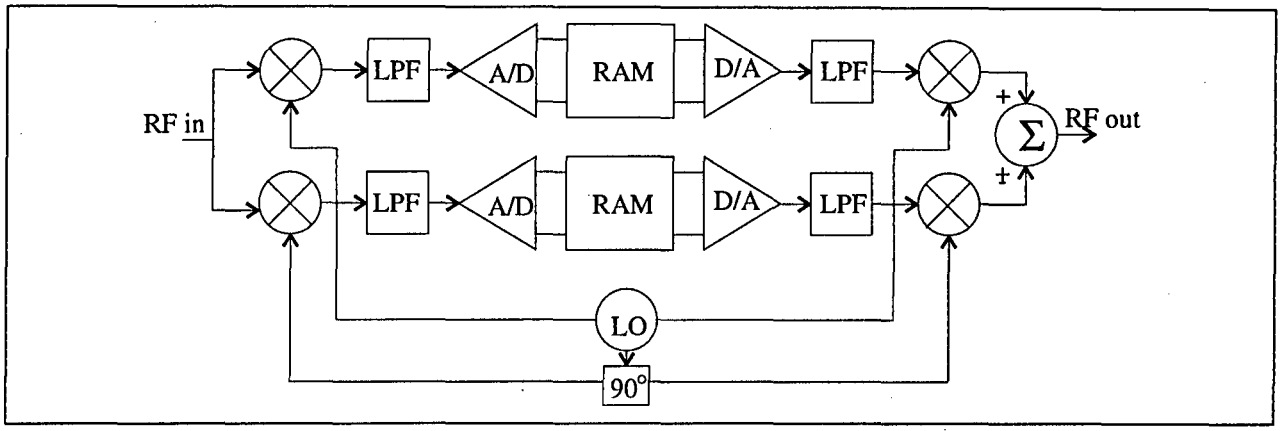

Figure 2.2. *Block diagram of EBAE architecture*

2.3.3 Phase Encoding (PE)

In the PE configuration (*Figure 2.3*), the two mixer stages together with the bandpass filter are once again required to eliminate the unwanted sideband. After the first mixer stage, a power splitter and quadrature mixer split the signal into an I and Q channel, which are both filtered to prevent aliasing. The 'Phase A/D' converter then compares the *relative* amplitudes of the I and Q channels to encode the phase of the incoming signal digitally. Absolute amplitude information is discarded. In the recalling process, the cosine of the encoded angle is converted to analogue form by the 'cos(...) D/A' converter, thus producing a constant amplitude, phase accurate output IF signal. The same up-conversion and sideband cancellation as described for the AE then follow.

The 'Phase A/D' is a device which calculates the phase of the incoming signal by comparing the relative amplitudes of the I and Q channels. Once the phase has been determined, it is quantised into a number of phase levels, each of which is assigned a binary code. This concept is illustrated in *Figure 2.5*. The assumption is thus made that the incoming signal has a constant amplitude, i.e. all amplitude information is discarded.

The 'cos(...) D/A' simply retrieves the I-channel information from the phase encoded signal, i.e. it calculates the cosine of the encoded angle. The Q-channel information is thus discarded, whereas it could be used to suppress the sideband signal, as is done in the EBPE architecture, which is described below:

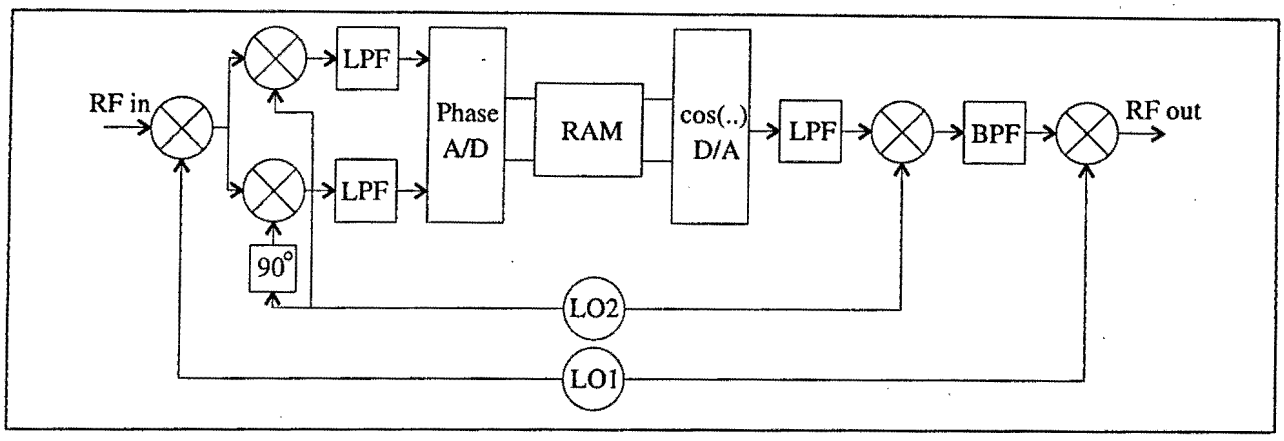

Figure 2.3. Block diagram of PE architecture

2.3.4 Extended Bandwidth Phase Encoding (EBPE)

The signal encoding techniques of the EBPE (*Figure 2.4*) and PE configurations are the same. The up-conversion stages differ in that a 'phase D/A' and quadrature up-conversion are used to eliminate the sideband instead of using a bandpass filter, hence the need for only one up- and one down-conversion stage. As in the EBAE configuration, the input signal can therefore be down-converted to baseband instead of IF.

The 'phase D/A' converts the digitally encoded phase into two quadrature amplitude signals. These two amplitude signals are then added to eliminate one of the sidebands. The quadrature channel system therefore gives the EBPE a factor 2 bandwidth advantage over the PE configuration.

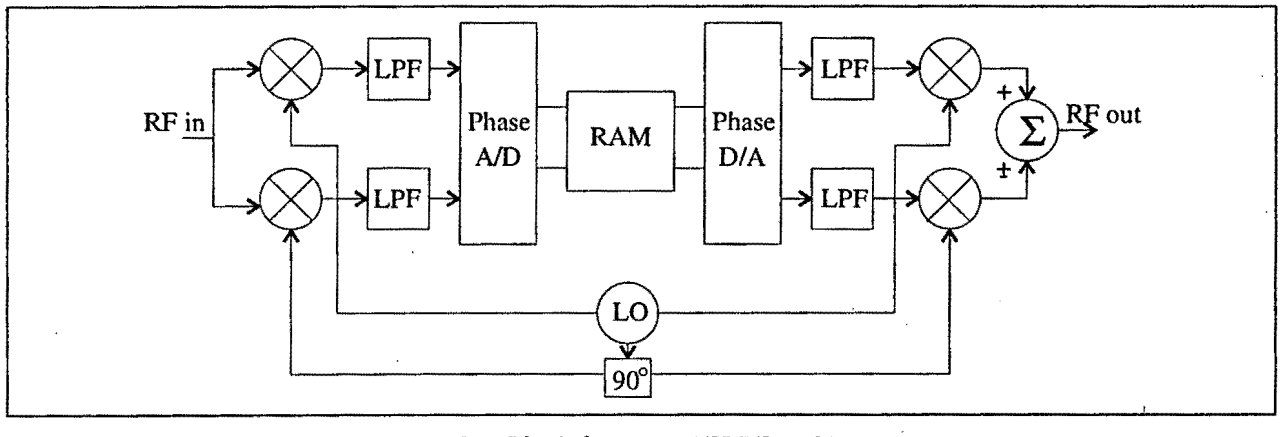

Figure 2.4. Block diagram of EBPE architecture

For all four configurations described above, the memory controllers, multiplexers, antennas and other hardware necessary to support such a system were left out of the description since they were considered of no significance to this dissertation.

Figure 2.5. shows the signal space diagrams for all four architectures for the 4-bit quantisation case, illustrating how each architecture quantises and digitally encodes the amplitude/phase information of the signal in terms of amplitudes of the I and Q channels.

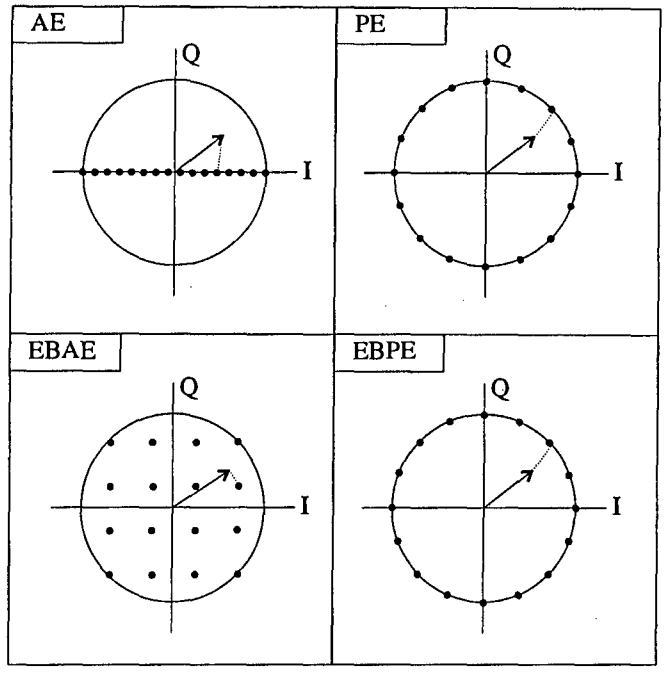

Figure 2.5. *Signal space diagrams for all four encoding architectures*

2.4 BASIS FOR COMPARISON OF TECHNIQUES

Keeping in mind the trade-offs for digital broadband signal storage discussed in *Section 2.2* (i.e. sampling rate, memory size and number of bits quantisation), it was decided to compare the four architectures by keeping the hardware parameters (sampling rate and memory size) fixed and comparing the signal fidelity of the stored signal. Since hardware complexity is directly proportional to memory size, and since sampling rate is limited by state-of-the-art technology, it was decided to keep these two factors constant for all four architectures. This would give the performance of each architecture for a roughly fixed production cost and complexity. The following restrictions are therefore implied:

- The same sampling frequency is used to sample the incoming wave, i.e. at each sampling period each A/D converter digitally encodes one sample of the incoming signal and stores it in memory. The EBAE configuration would therefore store two samples at each sampling period (one sample for each A/D).

- The same amount of memory is assigned to each of the four architectures, i.e. at each sampling period a fixed number of bits are available for quantisation. This implies that the AE and both phase encoding configurations have the full number of bits available for their single A/D converter. The EBAE architecture, on the other hand, has to divide the number of bits between the two A/D converters, which are clocked at the same time (for example, a '4-bit' EBAE configuration would therefore have two 2-bit A/D converters).

All results are based on the assumption that these two conditions have been met.

The only exception is discussed in *Section 5.2*, which is concerned with instantaneous bandwidth extension by interlaced sampling and the complications that are caused thereby. This sampling technique implies the exact duplication of the hardware modules described in *Section 2.3* (i.e. increasing the memory size and sampling frequency) and using them in parallel to increase the bandwidth.

It will be seen that 4-bit quantisation is used throughout the simulations to compare the architectures. In most cases the results for different numbers of bits quantisation are given in the appendices. This choice was made since it was found in the literature study that the 4-bit case is the most commonly used architecture, probably making a good trade-off between memory size and signal fidelity.

2.5 SIMULATION BACKGROUND AND LIMITATIONS

All simulations were done in MATLAB. This software package includes powerful and convenient signal processing functions and tools, making it ideal for simulations of this kind. Functions such as filtering, sampling, quantisation, etc. allow easy simulation of components in such a system, while mathematical functions such as the FFT, Hilbert transform, etc. provide fast methods of extracting frequency spectra, phase and other relevant information from the simulated signals. Faster programming, lower complexity and the easy attainability and displaying of results make up for lower processing speeds than those attainable with lower level programming languages such as C.

2.5.1 Sampling rates and the FFT

Since the FFT is the core function used to obtain most of the simulation results, it was decided to devote a section to briefly describe the usage of the FFT in terms of frequency resolution, sampling rates, etc.

Figure 2.6 illustrates the frequency spectrum obtained by calculating the FFT of the simulated signals. The signals were in total 10000 data points long, i.e. 5000 data points per FFT sideband. The simulated sampling frequencies and information sidebands were then chosen, as indicated by the shaded areas. As can be seen from the figure, the simulated sampling frequency (i.e. the sampling frequency of the A/D's used in the simulation) was chosen one tenth (1/10) of the simulation sampling frequency. The reason for choosing such a high simulation frequency was to prevent aliasing with the implementation of non-linear operations such as quantisation. Another reason was the need for an RF band for the input and output signal of the BDR, as indicated in the figure.

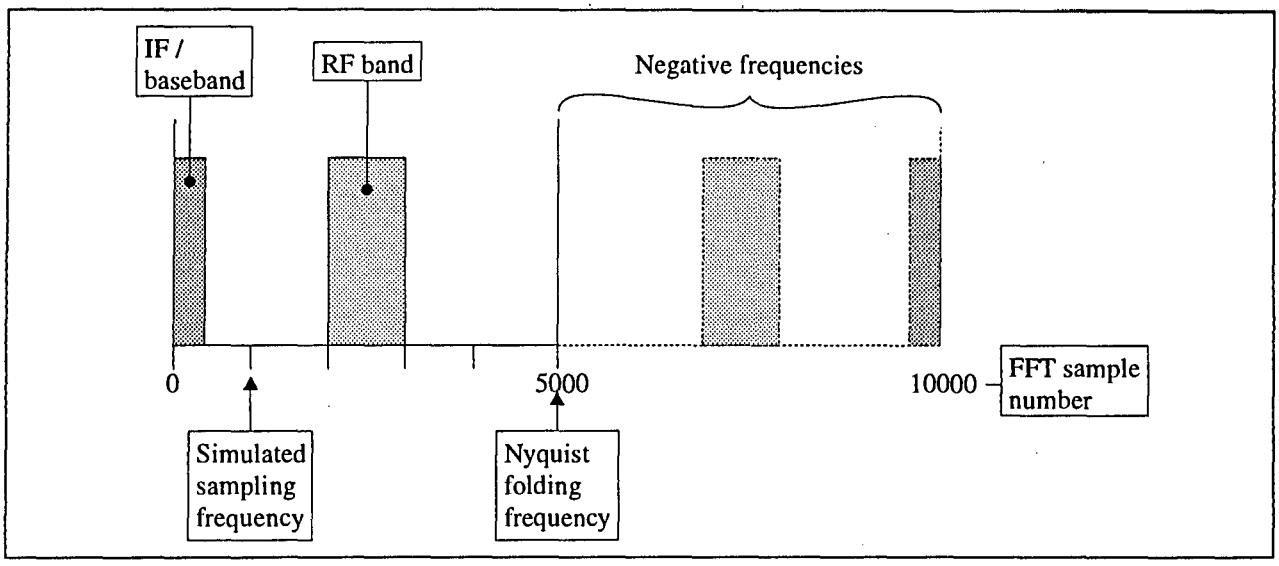

Figure 2.6. FFT spectrum, showing sampling frequencies and information bandwidth

The information band (i.e. the RF band) contains 1000 data points, making the frequency resolution $f_{res} = f_s/1000$ where f_s is the sampling frequency of the A/D converters used in the simulations. All input frequencies were therefore chosen at multiples of this frequency in order to obtain an accurate representation of the real frequency spectrum.

2.5.2 Other limitations

The 8 byte per sample simulation amplitude resolution corresponds to spurious levels in the order of -250dB, therefore rendering this issue irrelevant to possible simulation limitations.

The ability to simulate practical components accurately is probably the greatest limitation when it comes to simulating real-life systems. *Section 2.6* deals with this issue in more detail. Other practical considerations such as noise levels, power levels, etc. are only briefly mentioned in the analysis of the systems, since they are difficult to simulate and are considered of secondary importance to the study.

2.6 COMPONENT IMPERFECTIONS

In order to make the results more applicable to a typical practical implementation, component imperfections were introduced in the component models in order to simulate non-ideal components. Only component imperfections having a noteworthy effect on the output signal fidelity were considered in the simulations.

Table 2.1. lists the most important components that were used in the simulations and the imperfections that were taken into account for each component. Most of these imperfections were dealt with separately, as pointed out in the simulation results.

Table 2.1. Important components and their imperfections included in the analyses

Component	**Imperfection**
90° hybrid coupler	I/Q phase difference error in order to simulate an I/Q phase imbalance.
A/D converter	Ideal, different # bits
Bandpass filter	Typical filter type and number of poles, as used in practical hardware
D/A converter	Ideal, different # bits
Local oscillator	Ideal
Lowpass filter	Typical filter type and number of poles, as used in practical hardware
Mixer	LO leakage Intermodulation products
Power combiner	Ideal
Power splitter/divider	Amplitude imbalance

2.7 FACTORS INFLUENCING SYSTEM CHARACTERISTICS

As mentioned earlier, the comparison of the four encoding architectures is based on the waveform fidelity of the output signal, given a common input. In Chapters 3,4 and 5, the term "waveform fidelity" is defined by the following system characteristics:

1. **Spurious signal suppression**
2. **Phase/frequency accuracy**
3. **Instantaneous bandwidth**
4. **Dynamic range**
5. **Frequency response**

There are numerous external and system factors influencing these system characteristics. *Table 2.2* gives a list of the most important factors. The × indicates which of the abovementioned characteristics are influenced by each system factor. All of the factors listed below are addressed in the simulation results, which are discussed in the following chapters.

Table 2.2. Factors influencing system characteristics

		1	2	3	4	5
1	*Architecture*	×	×	×	×	×
2	*Digital frequency translation*	×				×
3	*Filter type and order*	×	×	×		×
4	*I/Q amplitude imbalance*	×	×			
5	*I/Q phase imbalance*	×	×			
7	*Input signal frequency*	×	×			
8	*Input signal level*	×	×		×	
9	*Input signal waveform*	×				
10	*Interlaced sampling*	×		×		×
11	*Intermodulation products*	×				
12	*LO leakage*	×				
13	*LO modulation*	×	×			
14	*Thermal noise*	×				
15	*Quantisation (No. of bits)*	×	×		×	
16	*Sampling rate*			×		

Chapter 3

Spurious signal level

The suppression of spurious signals is probably the most important factor when considering the waveform fidelity of BDR systems. Different sources of spurious signals are described in this section. The extent of the contribution of each source's spurious to the final output spurious level is determined. The results are largely based on simulations.

Sections 3.1 to *3.5* deal with the 5 most important sources of spurious signals in a typical system, discussing the effect of each component's imperfection on the output spurious signal level. One source of spurious signals not mentioned in this chapter is interlaced sampling. This issue is addressed in *Section 5.2*.

3.1 QUANTISATION AND SAMPLING

As mentioned in the literature study, coarse quantisation is the predominant source of spurious noise in a digitised signal. It is therefore important to know the exact cause and extent of this waveform deformation. Thorough analyses of the quantisation and sampling process for the AE architecture have been done by Bil [4] (amongst others). A summary of this work is given, in addition to the more important results obtained. An extension of these analyses to other architectures (mostly by means of simulations) was done in order to investigate other relevant aspects concerning spurious noise caused by quantisation and sampling. Results from the practical measurement of spurious noise from a hardware implementation are also included to support the practical relevance of such analyses.

3.1.1 Quantisation noise

Once quantised, the instantaneous amplitude values of a continuous signal can never be exactly reconstructed. The random errors introduced are called *quantisation noise*. To calculate the mean-square quantisation noise, equal amplitude increments between quantisation levels are assumed. Another assumption is that the quantisation error has a uniform probability density function over the amplitude of the incoming signal. Under these circumstances the peak-signal-to-rms-quantisation-noise ratio is given by Stremler [5, *pp543, equation 9.22b*] as

$$\left[\left(\frac{S}{N}\right)_{pk\_qnt}\right]_{dB} = 4.8 + 6 \cdot m \quad \text{.....(3.1)}$$

where $n = 2^m$ is the number of quantisation levels, i.e. m is the number of bits used in the quantisation process.

The **rms**-signal-to-rms-quantisation-noise ratio (for a sinusoidal input) is therefore

$$\left[\left(\frac{S}{N}\right)_{rms\_qnt}\right]_{dB} = 1.8 + 6 \cdot m \quad \text{.....(3.2)}$$

It can therefore be seen that the **rms**-signal-to-rms-quantisation-noise increases by exactly 6dB for each bit which is added to the A/D quantisation process. It must be stressed that these results are applicable to amplitude quantisation only.

3.1.2 Harmonics caused by Quantisation

It is a well-known fact that any non-linear operation on a sinusoidal signal results in the generation of harmonics at multiples of the frequency of the input signal. It can further be shown that a symmetric amplitude distortion generates harmonics at only the odd multiples of the input frequency. Quantisation, which is a symmetric amplitude distortion, therefore creates only odd harmonics (assuming no DC offset and symmetric A/D swings). The harmonics created by N-bit amplitude quantisation of a sinusoidal waveform can be determined by calculating the Fourier Transform of an N-bit quantised waveform. With reference to an analysis of N-bit amplitude quantisation by Bil [4], *Equation 3.3* gives

a formula for the calculation of the magnitude of such harmonics, C_n. The first ten harmonics for different numbers of bits quantisation [4] are given in *Table 3.1*.

$$C_n = \frac{1}{n\pi \cdot 2^{N-1}} \left[\sum_{j=1}^{2^N-1} \sin(na_j) \right] \quad \text{.....(3.3)}$$

where:

$$a_k = \cos^{-1}\left(\frac{2k}{2^N} - 1\right)$$

It must again be stressed that these results are applicable only to amplitude quantisation.

Table 3.1 Harmonic levels due to quantisation

Harmonic	*Spurious levels (dBc) versus number of bits quantisation*							
	1-bit	**2-bit**	**3-bit**	**4-bit**	**5-bit**	**6-bit**	**7-bit**	**8-bit**
1	0	0	0	0	0	0	0	0
3	-9.542	-18.272	-27.045	-35.892	-44.807	-53.770	-62.764	-71.776
5	-13.979	-25.418	-29.219	-36.770	-45.201	-53.957	-62.853	-71.817
7	-16.902	-28.341	-34.887	-38.466	-45.876	-54.257	-62.996	-71.887
9	-19.085	-27.815	-51.365	-41.717	-46.945	-54.694	-63.192	-71.980
11	-20.828	-20.828	-35.324	-49.103	-48.616	-55.306	-63.454	-72.101
13	-22.279	-22.278	-39.649	-57.010	-51.299	-56.146	-63.789	-72.250
15	-23.521	-32.252	-36.260	-45.897	-56.059	-57.296	-64.215	-72.433
17	-24.609	-36.048	-33.739	-44.952	-69.125	-58.887	-64.746	-72.650
19	-25.575	-37.014	-33.546	-53.233	-61.946	-61.158	-65.411	-72.910

3.1.3 Sampling a quantised signal

In the analysis of the combined effect of sampling and quantisation, it is important to look at the real life situation. In practice one tends first to sample and then quantise the signal. In a mathematical analysis, however, it is usually easier first to quantise the signal, determine the output spectrum, and then consider the sampling process as causing spectral aliasing. The "quantisation before sampling" analysis allows the determination of errors introduced by quantisation first (harmonic distortion), and then the effects of aliasing separately. Janant and Noll [6] state that the operations of sampling and quantisation could be performed in either order.

As mentioned in *Section 3.1.2*, quantisation is a highly non-linear process, creating spurious signals occurring at odd harmonics of the input frequency. This increases the effective bandwidth of the output signal to many times its original bandwidth. When this quantised signal is now sampled at a rate which

would have been sufficient for the original input signal, the baseband spectrum is replicated at multiples of the sampling frequency. Because the baseband spectrum is now much wider, the signal is effectively undersampled and spectral aliasing occurs. This effect is illustrated in *Figure 3.1.* It can be seen that harmonics from the replicated spectra fold back into the baseband. In order to keep these "aliased spurious signals" in the baseband low, a sampling rate many times higher than the Nyquist sampling rate of the original signal would therefore be required, which is not viable in such broadband systems.

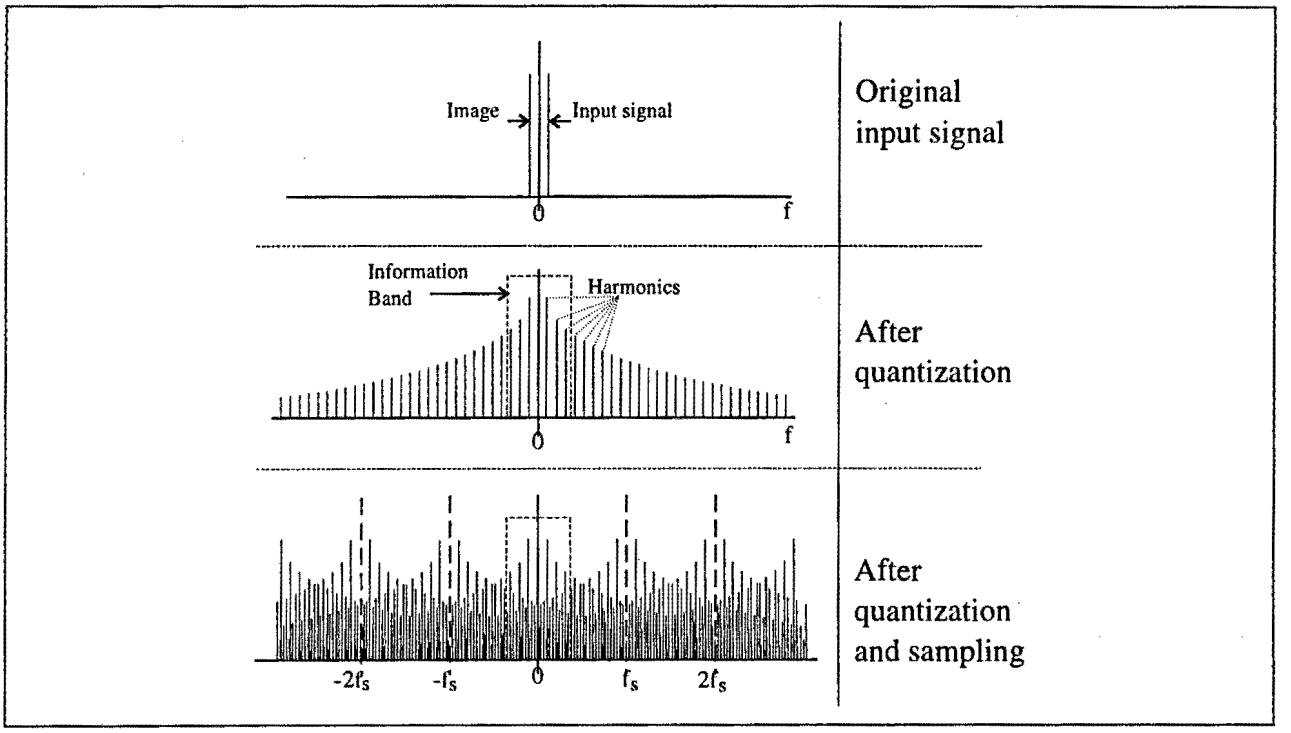

Figure 3.1. Effect of coarse digitisation and sampling

Looking at *Sections 3.1.1, 3.1.2* and *3.1.6,* it can be seen that the analyses are done only for amplitude quantisation. The reason for this is that analyses on waveform distortions caused by amplitude quantization are widely available in the literature. The theory is therefore only used as a reference to test the credibility of the simulations. The actual comparison of the different encoding architectures, which is the essence of the study, is done in the simulations. The results of these simulations are discussed in the following sections.

3.1.4 Output power density spectra

In order to see the effect of sampling and quantisation for each encoding architecture, three different types of signals were used as input to each configuration: a single tone (sinusoid), an amplitude modulated signal, and a wideband chirp signal. The corresponding output spectra were determined by means of simulations. The output spectra illustrated below are plotted in dB relative to the output power of the desired signal. The frequency scale represents the baseband signal and is expressed in terms of *f/fs* where *fs* is the sampling frequency of the A/D. The frequency value of *f/fs=0* corresponds to the LO frequency.

It must be stressed that no component imperfections are included in these simulations. The spurious noise is therefore caused only by sampling and quantisation. 4-bit quantisation is used throughout these simulations, as explained in *Section 2.4*. Output spectra for different numbers of bits quantisation are provided in *Appendix B1* to *B3*.

3.1.4.1 Single tone

A sinusoid of arbitrary frequency (in this case $0.213 \times f_{sample}$) was used as input signal for the simulation. The following can be seen from the results illustrated in *Figure 3.2*:

- The AE configuration has substantially lower spurious levels than the other configurations (in the order of 10dB lower than the phase encoding techniques)
- The bandwidth advantage of the double sideband architectures is evident.
- The spurious signal levels for the two phase encoding techniques are roughly the same
- Spurious signals caused by quantisation and aliasing are spread over the whole information band.

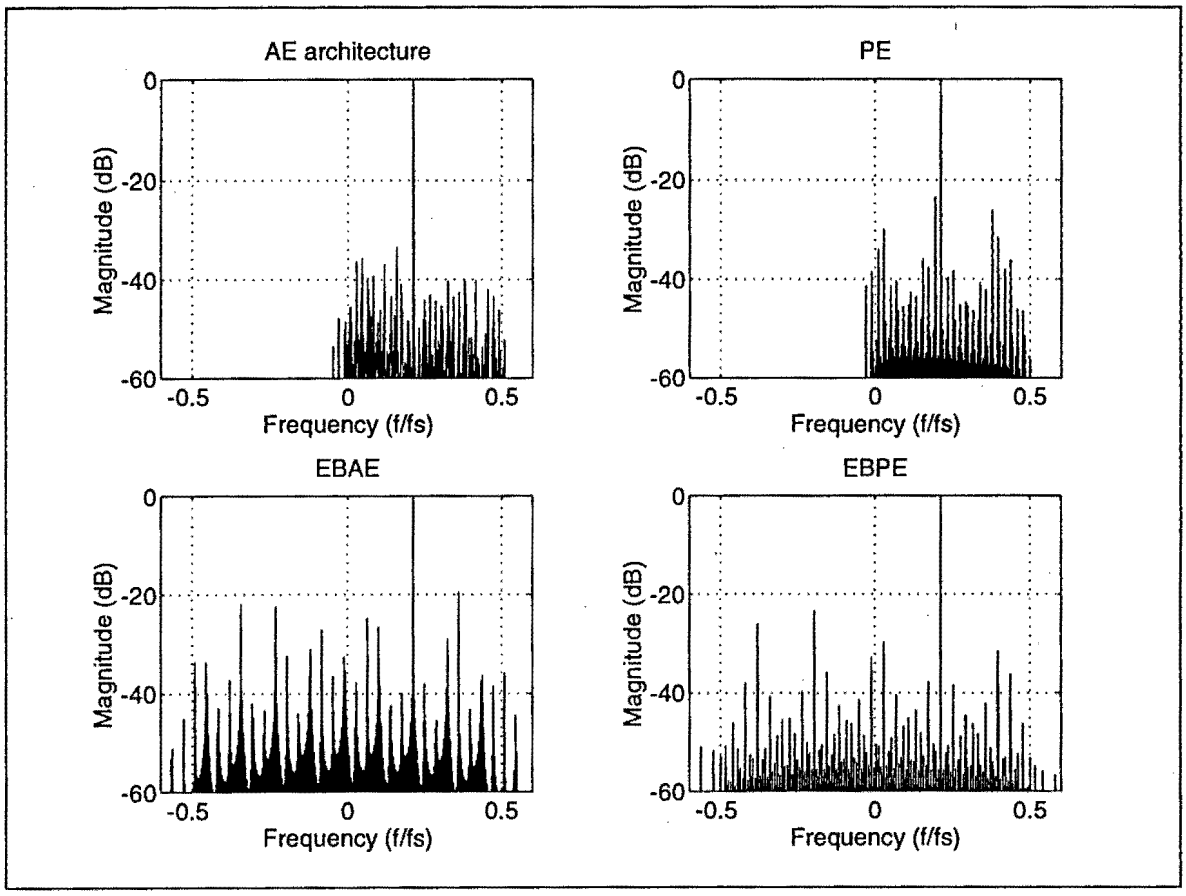

Figure 3.2. Output spectra for single tone input

3.1.4.2 Amplitude modulated input

For this simulation the sum of two sinusoids with equal amplitude but different frequencies (in this case arbitrarily chosen as 0.213×*fs* and 0.297×*fs*) was used as an input signal for each configuration. The following trigonometric identity indicates that the input is an amplitude modulated signal:

$$\cos(2a) + \cos(2b) = 2.\cos(a+b).\cos(a-b) \quad \text{.....(3.4)}$$

Simulations with different input frequencies indicated that the position (frequency) of the highest spurious signals changed, but not their amplitudes.

The following points can be made about the simulation results illustrated in *Figure 3.3*:

- As for the single frequency input, the AE displays the best results regarding spurious levels.
- For both the AE and EBAE architectures there is no noticeable difference in the spurious levels between the single frequency input (illustrated in *Figure 3.2.*) and the amplitude modulated input (illustrated in *Figure 3.3.*)
- As can be expected, the performance of the phase encoding techniques is poor for amplitude modulated signals, the reason being that the amplitude information is discarded in the phase encoding process. It can therefore be concluded that these architectures are not suitable for storing signals which contain important amplitude information.

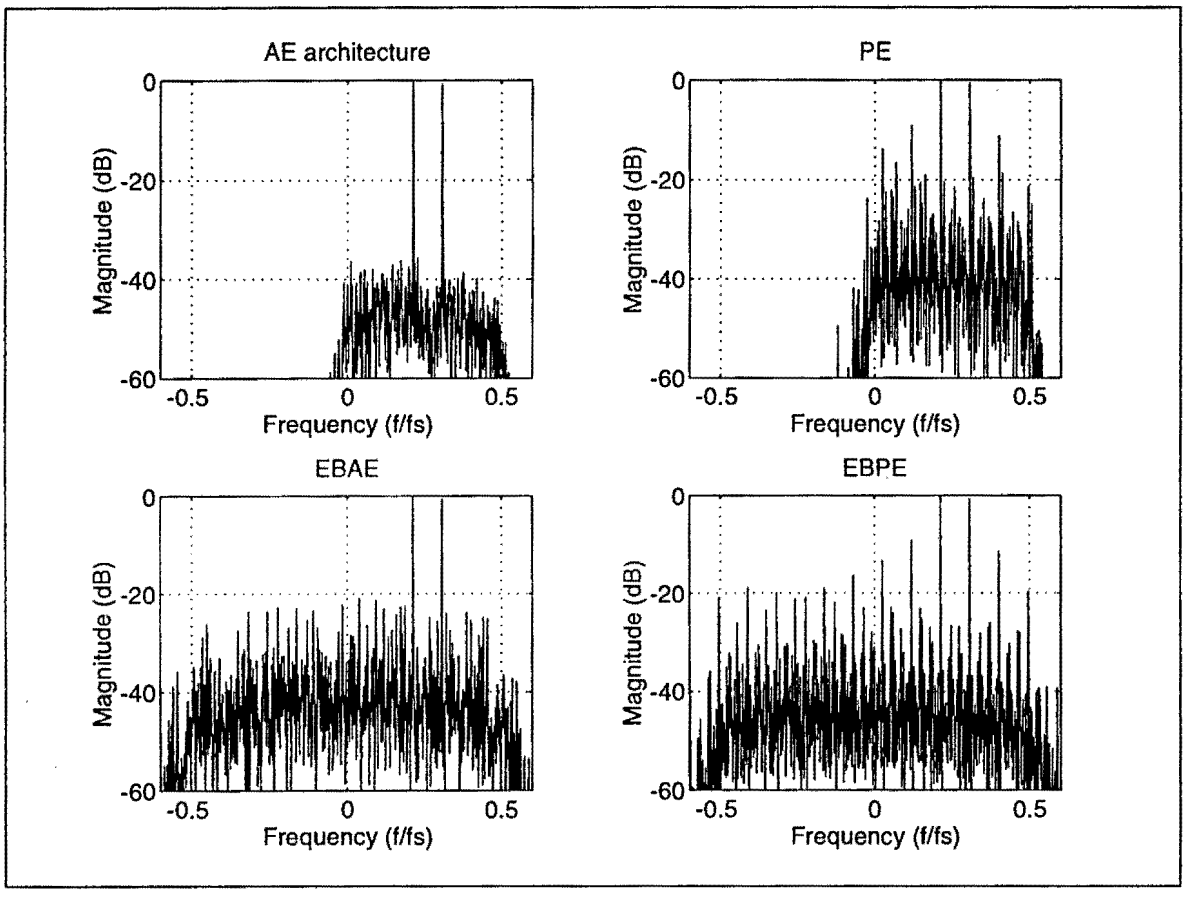

Figure 3.3. Output spectra for amplitude modulated input

3.1.4.3 Wideband Chirp

In this case a wideband linear FM chirp with Hamming amplitude weighting was used as the input signal. This specific input signal was chosen in order to test the ability of the different architectures to replicate both phase and amplitude information. The centre frequency and bandwidth of the chirp were chosen as $0.22f_s$ and $0.15f_s$ respectively. The input and resulting output spectra are illustrated in *Figure 3.4,* from which the following conclusions can be made:

- Once again the AE configuration shows superior spectral purity.
- This example clearly illustrates the ability of the different architectures to store amplitude information. The AE configuration is clearly the most successful in this objective, accurately duplicating the Hamming shape of the incoming spectrum. The results for the EBAE architecture indicate that this configuration is less successful, quantising the amplitude in larger amplitude steps than the AE configuration, but nevertheless roughly reproducing the shape of the window. Both phase encoding techniques discard the amplitude information altogether, reproducing a constant amplitude linear FM chirp.

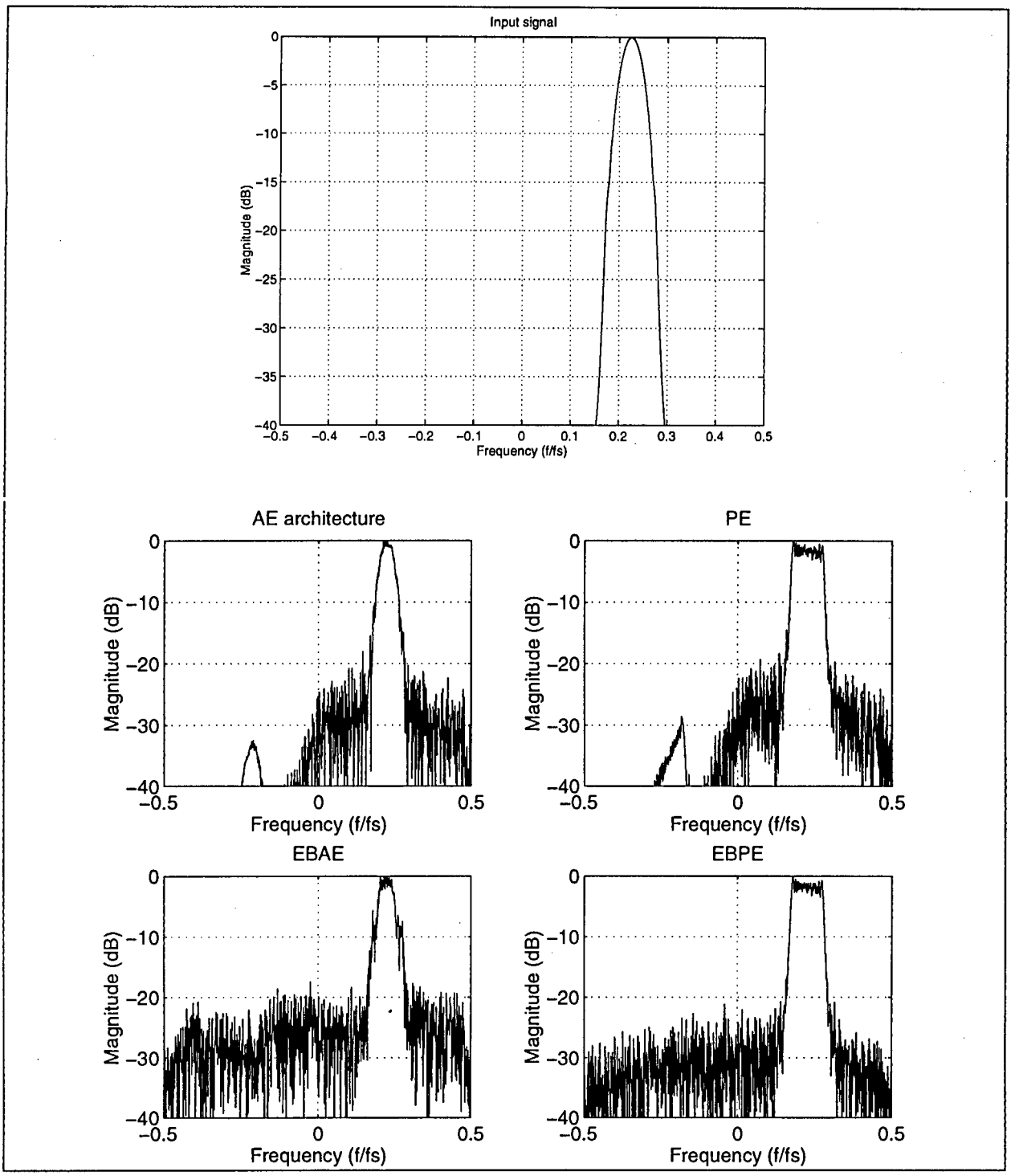

Figure 3.4. Output spectra for Hamming amplitude weighted wideband FM chirp input

3.1.5 Spurious signal level versus input frequency.

As explained in *Section 3.1.3,* harmonics from the replicated spectra fold back into the baseband after sampling and quantisation. With a change in input frequency, the position (frequency) of these harmonics change in relation to each other, causing harmonics to overlap and add/subtract at certain input frequencies. The maximum spurious level is therefore not expected to be constant with a change in input frequency. Furthermore, at higher input frequencies the harmonics (which occur at odd multiples of the input frequency) are further apart and consequently the spectral aliasing becomes more pronounced. It can therefore be expected that the spurious signal level will be higher for input frequencies at the upper end of the Nyquist bandwidth.

In the simulation results illustrated in *Figure 3.5*, the input frequency to the different encoding architectures was swept over the whole information band for each architecture. For every input frequency the maximum spurious signal in the Nyquist band was determined and plotted versus this input frequency. This method of displaying spurious outputs is becoming popular with the industry due to the advent of direct digital synthesis. *Figure 3.5* is a comparison of the architectures for different quantisation coarseness' (2-bit, 4-bit, 6-bit and 8-bit quantisation). Results for different numbers of quantisation bits (i.e. odd numbers of bits for the AE, PE and EBPE architectures) are given in *Appendix B4* .

The following can be concluded from the results illustrated in *Figure 3.5.*

- The maximum spurious in the output spectrum is input frequency dependent due to spurious overlap. The overlapping spurious can add up or subtract, depending on the relative phases of the applicable spurs. As the frequency of the input signal is swept through the band, the spurious move (in frequency) relative to each other add and subtract at different positions (frequencies), resulting in a rugged 'highest spurious vs. input frequency' graph, as depicted in *Figure 3.5.*
- At certain input frequencies some of the highest spurs overlap, causing the maximum spurious level to rise or fall (depending on the relative phases of the overlapping spurs) for that specific frequency. This causes positive or negative 'spikes' in the 'highest spurious vs. input frequency' graph.
- The spurious levels increase slightly near the upper end of the information band.

A method is required to compare the architectures for the different numbers of quantised bits. Displaying of graphs like those given in *Figure 3.5* for each individual case of quantisation coarseness is over-elaborate and tends to lead to confusion. A better solution is to compare architectures by comparing average spurious levels. The results illustrated in *Figure 3.5* and *Appendix B4* are thus summarised in *Table 3.2* by calculating the **average maximum spurious** levels for each architecture and quantisation coarseness. For the purpose of this analysis, the average maximum spurious level, S_{av} is defined as follows:

- $S_{av} = E\left[S_{\max}\left(f_{in}\right)\right]$ where $E[x]$ denotes the expected value of x and $S_{\max}\left(f_{in}\right)$ denotes the maximum spurious level for an input frequency of f_{in}

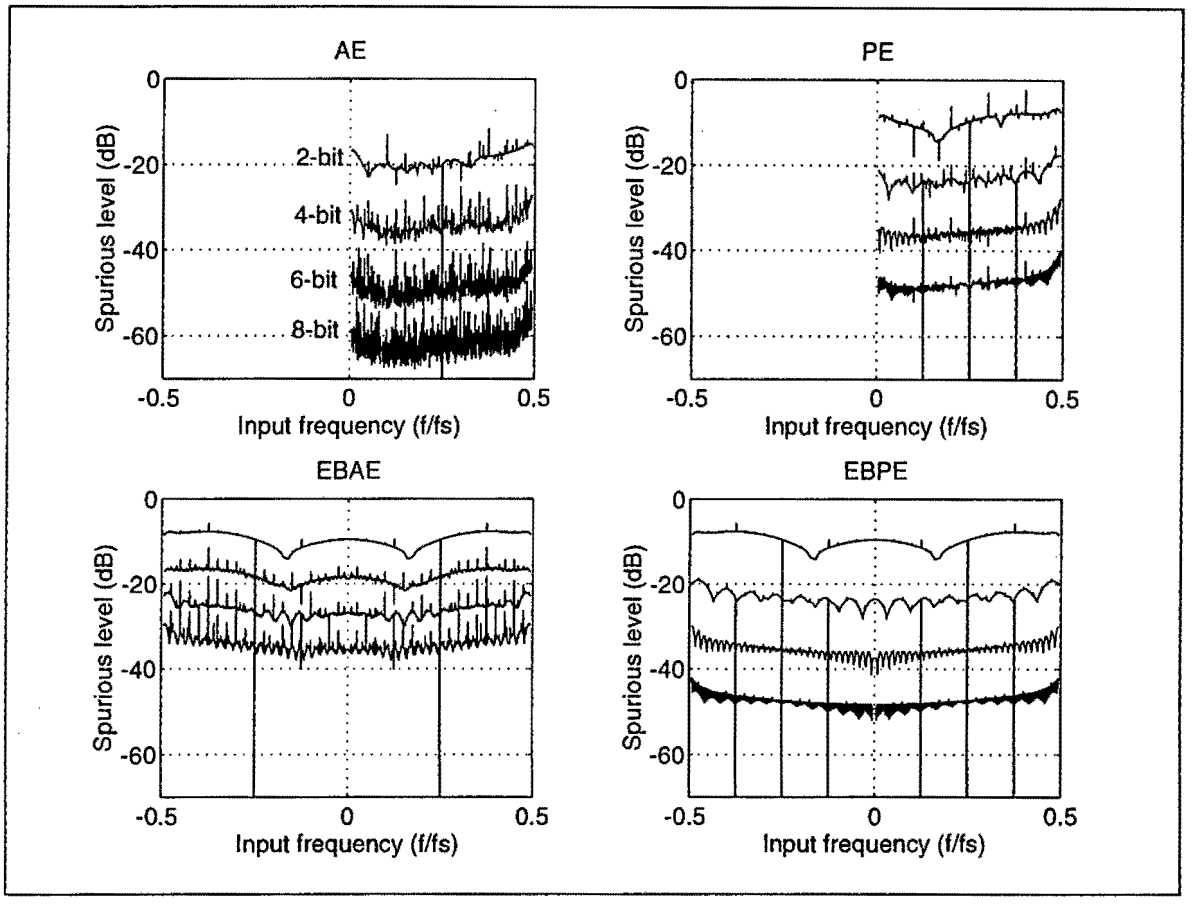

Figure 3.5. Maximum spurious vs. input frequency - comparison of architectures

Table3.2 Average spurious levels for different encoding architectures and different numbers of bits quantisation

Architecture	Average spurious level (dB) vs. Number of bits quantisation							
	1-bit	**2-bit**	**3-bit**	**4-bit**	**5-bit**	**6-bit**	**7-bit**	**8-bit**
AE	-9.633	-19.29	-26.88	-34.22	-41.88	-48.83	-55.35	-61.67
EBAE	--	-9.733	--	-18.33	--	-26.36	--	-34.38
PE	-9.623	-9.618	-17.06	-23.38	-29.58	-35.62	-41.61	-47.57
EBPE	-9.735	-9.731	-17.25	-23.64	-29.77	-35.82	-41.74	-47.74

3.1.6 Theoretical analysis

When doing a simulation, it is important not to neglect the theory. A theoretical analysis is a handy tool which can be used as a benchmark to check simulation results, as well as a guide in the interpretation of results. In this section a theoretical analysis of an amplitude quantised and sampled sinusoidal waveform is presented. This analysis is used later on in the chapter to verify samples of the simulation results.

With reference to Berger and Meer [7], the location and magnitude of the harmonics generated by the quantisation and sampling of a pulsed sinusoidal wave is given by

$$\left|D(lf_p)\right| = \frac{t_s \tau_p}{t_p} \cdot \left|\frac{\sin(lf_p\pi)}{(lf_p\pi)}\right| \cdot \left\{\left[\sum_{k=1}^{n} a_k \cdot \cos(\alpha_p l t_s (k-1))\right]^2 + \left[\sum_{k=1}^{n} a_k \cdot \sin(\alpha_p l t_s (k-1))\right]^2\right\}^{\frac{1}{2}} \quad \text{.....(3.5)}$$

where:

$n = \dfrac{f_s}{greatest\_common\_devisor(f_s, f_0)}$ where f_s is the sampling frequency and f_0 the sinusoid input frequency, i.e. n = number of samples in one digital period

t_s = sampling period

τ_p = pulsewidth of the signal

$t_p = nt_s$

$f_p = 1/t_p$

a_i = quantisation level of the i^{th} sample

$\alpha_p = 2\pi f_p$

$l = 0,1,2, \ldots ,s$ where $sf_p < f_s/2$, i.e. l is the harmonic number.

$|D(l.f_p)|$ is therefore a series of harmonics occurring at multiples of the digital period f_p.
The spectrum of the stored signal can therefore be calculated using this formula.

In order to confirm the accuracy of the results presented in *Section 3.1.4* and *3.1.5*, the output spectra for a single tone input as well as the 'spurious level vs. input frequency' graphs were calculated using *Equation 3.5*. These analytical results were then compared to the simulation results and illustrated in *Figure 3.6* and *3.7*. The comparison was done for the AE architecture with 4 bit quantisation (Also compare these results to *Figures 3.2* and *3.5*). From *Figures 3.6* and *3.7* it can be seen that the simulation results compare well with the analytical prediction and it can therefore be concluded that the simulations provide an accurate enough representation of the real-life situation.

Calculating the FFT of the digitally stored signal, which is the method used in the simulations, is more useful than the analytical approach when determining the combined effects of sampling and

quantisation. This is because of the advantage of computation speed. Another advantage of the simulations is the option of including component imperfections.

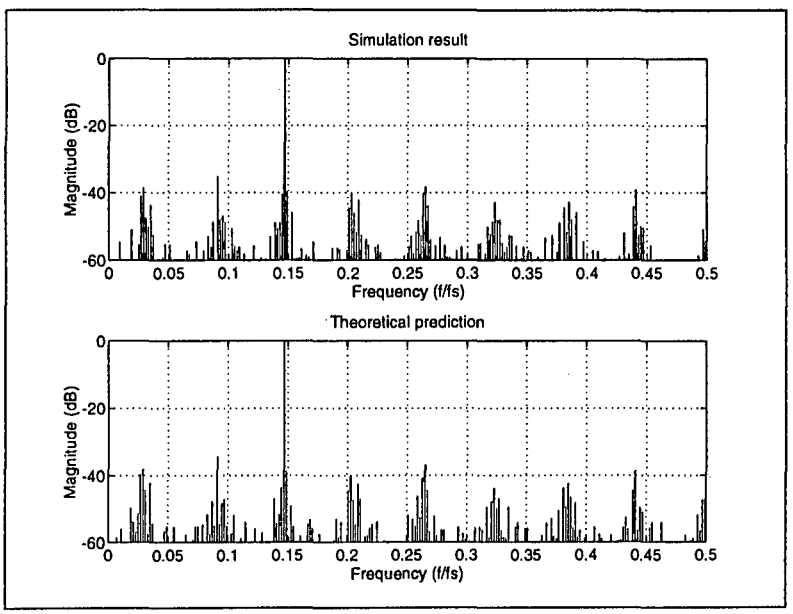

Figure 3.6. Comparison between analytical and simulation results - Output spectrum for single tone input

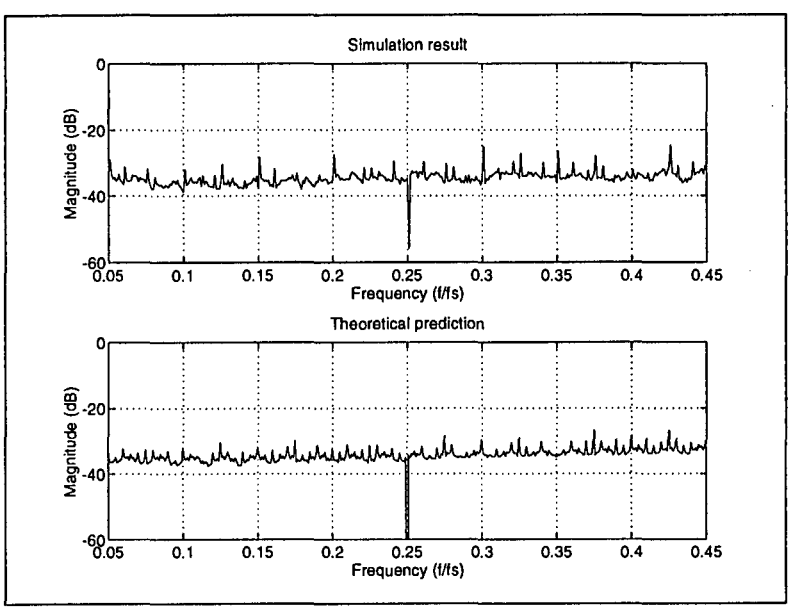

Figure 3.7. Comparison between analytical and simulation results - Highest spurious vs. input frequency

3.1.7 Practical measurements

Results were obtained from laboratory measurements on the output spurious signal level of a 3-bit AE BDR architecture. These results are illustrated in *Figure 3.8* together with the simulation results for the 3-bit AE architecture (*Appendix B4*). The simulation predicts slightly lower spurious levels than the actual measurements show. General trends of output spurious level vs. input frequency are, however, satisfactory. The (relatively small) errors can possibly be attributed to the test set-up and/or measurement errors. Simulations are therefore a meaningful way of predicting the spurious level output of BDR architectures.

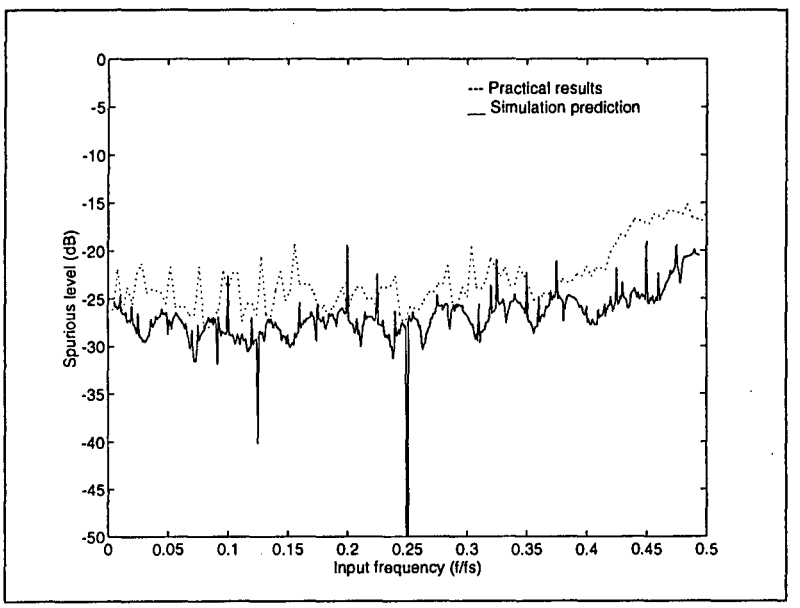

Figure 3.8 Comparison of practical measurements and simulation results - output spurious levels

3.2 I/Q IMBALANCE

3.2.1 Phase imbalance

Like other single sideband systems, the EBAE and EBPE systems remove the unwanted sideband by a "phasing out" process. The output of the I and Q channels are added or subtracted to produce a single sideband output signal, as indicated in the following equation:

$$\phi_{SSB\mp}(t) = f(t)\cos(\omega_{lo}t) \pm \hat{f}(t)\sin(\omega_{lo}t) \quad \text{.....(3.6)}$$

where $f(t)$ is the input signal, $\hat{f}(t)$ is the Hilbert transform of $f(t)$ and ω_{lo} is the local oscillator angular frequency.

The 90° phase shift required for the generation of the Hilbert transform as well as the sin(.) term in *Equation 3.6* is achieved by generating a 90° phase shifted version of the local oscillator using a quadrature hybrid, as indicated in *Figure 2.2*. The generation of such a 90° phase shift is not easy to achieve over a wide frequency range at RF frequencies. Other factors contributing to the I/Q phase imbalance are power dividers, mixers, filters as well as any other source (analogue or digital) which might induce a timing difference in the I and Q channels.

Simulations were done to investigate the effect of such a phase imbalance on the sideband level of the output spectra. The phase imbalance was varied from -20° to 20° in 0.5° increments. The simulations were done for the EBAE, EBPE and PE architectures for no quantisation i.e. only the measurement of the sideband level. *Figure 3.9* illustrates the results, from which the following can be deduced:

- It can be seen that the magnitude of the sideband is very sensitive for a phase imbalance of a few degrees, especially for the EBAE and EBPE architectures. For example, in the EBAE architecture the relative timing precision between the 'I' digital memory and 'Q' digital memory must be equivalent to a value of the order of two degrees (2°) or less to maintain a sideband suppression of better than 35dB. This means that if the I/Q memories are operating at a clock rate of f_sHz, a relative timing difference of $\frac{2}{360 \cdot f_s}$ seconds is required to maintain a sideband suppression of better than 35dB. This becomes a very stringent requirement for high speed systems.
- The PE architecture is less sensitive to a phase imbalance than the other two architectures.
- Simulations which included quantisation as well as a phase imbalance, showed that spurious signals caused by quantisation are unaffected by an I/Q phase imbalance. This can be deduced from the fact that the quantisation noise remains roughly constant with a change in phase imbalance. The spurious signals caused by quantisation, and the sideband image caused by an I/Q phase imbalance can therefore be considered separately.

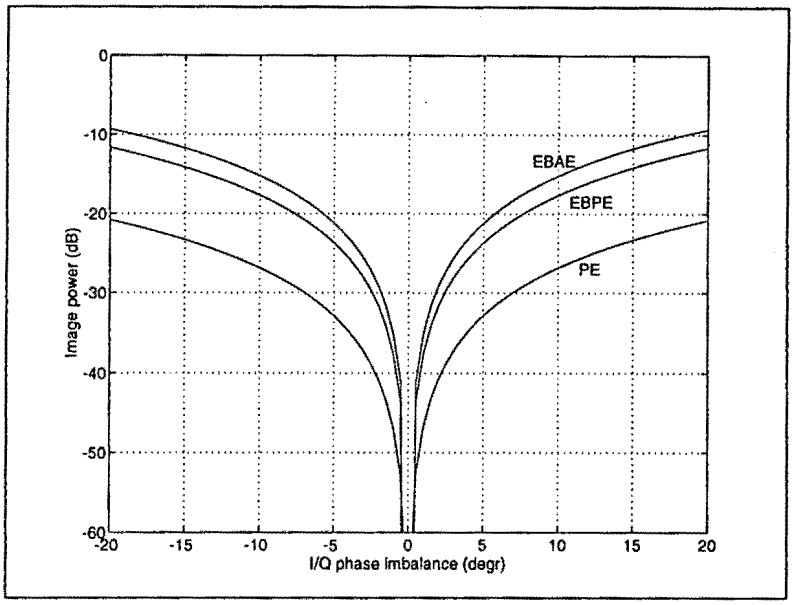

Figure 3.9. *Sideband magnitude caused by an I/Q phase imbalance*

3.2.2 Amplitude imbalance

In a practical implementation, the power splitters, filters and mixers used in the EBAE, PE and EBPE architectures can cause an amplitude imbalance in the I and Q channels. This amplitude imbalance disturbs the single sideband cancelling process as given in *Equation* 3.7. *Figure 3.10* illustrates the effect of such an imbalance on the SSB cancellation process. The figure illustrates the power density spectra of an input signal (*f*), its Hilbert transform ($\hat{f}$) and the resulting sum. This is done for both the ideal and imbalanced cases.

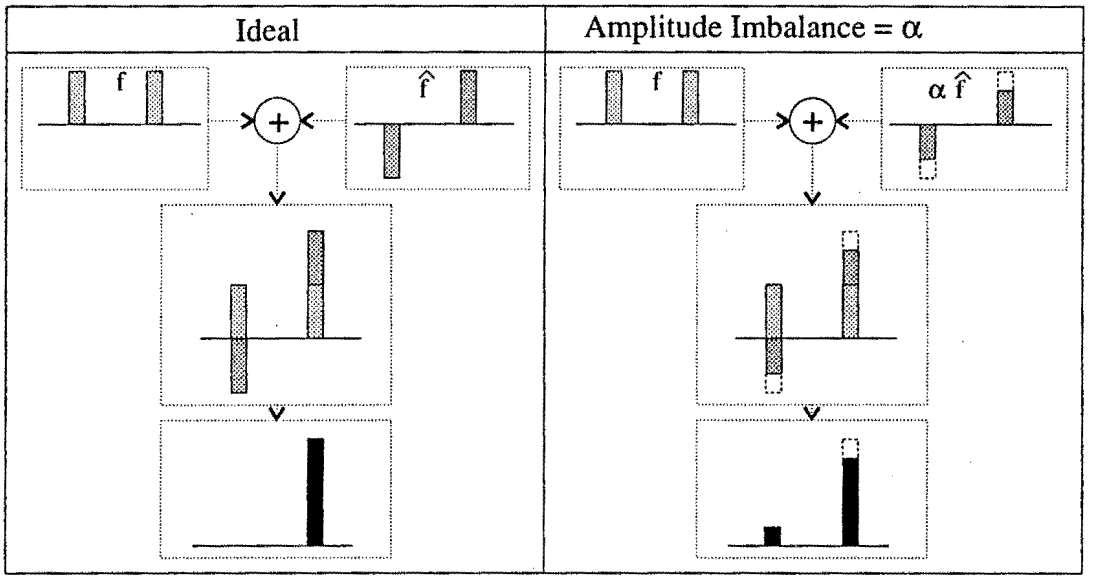

Figure 3.10 *Cancellation process for SSB architectures*

For an amplitude imbalance of magnitude α (i.e. the amplitude of one channel is α times as large as that of the other, $\alpha<1$), a sideband image is therefore created with magnitude $|1-\alpha|$. The magnitude of the desired signal becomes $|1+\alpha|$. The resulting signal-to-sideband level (i.e. 'spurious signal' level with reference to the desired output), is therefore:

$$S/I = \frac{|1+\alpha|}{|1-\alpha|} \quad \text{.....(3.7)}$$

Datasheets [8] show that values for the amplitude imbalance of wideband power splitters is typically in the order of 0.1 to 1dB. Such low levels of imbalance would therefore produce only very low levels of spurious signals, and can be ignored in most cases. Amplitude imbalances caused by mixers and filters depend on component accuracy, but are typically very small.

3.3 DYNAMIC RANGE

Up until now, only the ideal case of A/D conversion in terms of input signal level has been considered, i.e. the input signal was considered to be large enough to utilise the full range of the A/D's digital levels, whilst at a level low enough to avoid 'clipping' or limiting of the input signal. Simulations were therefore done to investigate the effect of the input signal level on the output spurious signal level. Automatic Gain Control (AGC) circuits are often used to regulate the input signal level of an A/D converter. In such cases, it would be useful to know how efficient an AGC would have to be to keep quantisation spurious below a specified level.

The simulation was done for all four configurations and the results for the 4-bit quantisation case are illustrated in *Figure 3.11*. Results for 2-bit and 6-bit quantisation are included in *Appendix B5*. The input signal level was varied from -20dB to +20dB in 0.4dB steps where 0dB represents the optimum input level (i.e. where the input signal level is high enough to utilise the full range of A/D quantisation levels, whilst avoiding clipping). The output spectrum was calculated for each input level, and the maximum spurious determined. As it was found that the results are influenced to a small extent by a change in input frequency, the simulation was performed for a number of different input frequencies. These results were then averaged in order to generate more widely applicable data. The following can be deduced from the results illustrated below:

- The maximum spurious level for an optimum input level (0dB) corresponds to the quantisation spurious levels listed in *Table 3.2*, i.e. these spurious are caused only by quantisation.
- As can be expected, the phase encoding techniques are insensitive to input signal level because all amplitude information is discarded in the phase encoding process. This makes these encoding architectures ideal for systems which cannot guarantee constant input signal levels. It must be stressed that these results are applicable only for the **ideal** phase encoder. In a practical implementation the phase encoding architectures will also have operational limits in terms of input signal levels (for example, the input signal may not saturate). The important point made by the simulation results is, however, that the phase encoding architectures are much less sensitive to input signal level variations.
- For the amplitude encoding architectures with input levels smaller than the optimum value (0dB), the spurious level rises in a roughly linear fashion to the maximum value of about -10dB. This happens when the input signal is so small as to use only one quantisation level in the A/D, i.e. equivalent to 1-bit quantisation. Theoretically this happens when the signal is at a level of $1/2^{n-1}$ times the optimum, where n is the number of quantisation bits. For the 4-bit AE architecture this implies an input level of -18dB, which agrees with simulation result.
- Clipping occurs for the amplitude encoding architectures with input signal levels higher than the optimum level. The spurious levels therefore increase rapidly until they saturate again at the -10dB level. This is intuitively a satisfactory result because, for very high input signals, the A/D would see the input as a hard-limited signal. The input signal would therefore be encoded only in the highest

and lowest quantisation level, which corresponds to a 1-bit case of which the spurious are again in the order of -10dB (see also *Table 3.1* for the 1-bit quantisation spurious levels).

- Spurious levels increase more rapidly for an increase than for a decrease in input signal level relative to the optimum (0dB) level. It would therefore be advisable for an AGC to operate below the optimum signal level (For example, an AGC with a 4dB output range would produce better spurious suppression if it were to operate in the -4dB to 0dB range than in the -2dB to +2dB range). Clipping should therefore be avoided wherever possible.

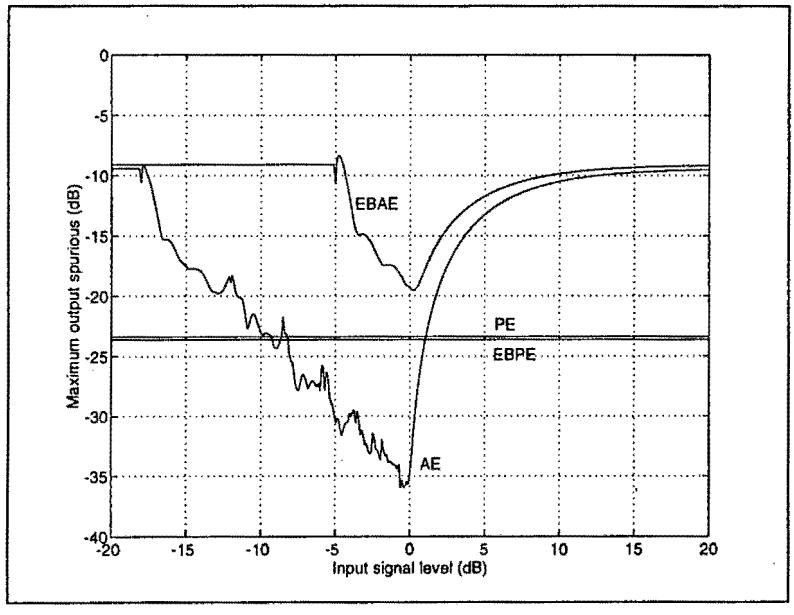

Figure 3.11. Dynamic range simulation - maximum output spurious vs. input signal level

3.4 NON-IDEAL FILTERING

Another source of spurious signals in practical implementations is the non-ideal filtering of the information band in order to eliminate the sampling images and sidebands. It is therefore once again a very implementation-related problem since the suppression of the image/sideband would depend directly on the transfer function of the filter used in the specific application.

Once again typical order filters and other system parameters were used to illustrate the principle. *Figure 3.12* shows the image and sideband levels for a single tone input of which the input frequency was swept over the whole information band. The magnitude of the images on both sides of the information band for each input frequency were calculated and plotted on the graph. 12'th order Butterworth lowpass filters and 6'th order Butterworth bandpass filters were used for the 'typical' filters. The magnitude of the spur can easily be calculated by determining the transfer function of the filters outside of the information band.

By comparing this result with *Figure 3.5*, which is the result for the identical systems but with ideal filtering and 4-bit quantisation, it can be seen that the image/sideband level exceeds the quantisation spurious levels near the edges of the information band. This might be another consideration which would have to be taken into account when determining the 'useable bandwidth' of such systems if it is required that the 'spurious level' (which could also include the image or sideband frequency) is not to exceed a specified level. The non-ideal filtering also induces phase jitter for input frequencies near the edges of the information band due to increasing image levels. This issue is dealt with in *Section 4.2*. Further aspects concerning bandwidth limitations are discussed in *Chapter 5*.

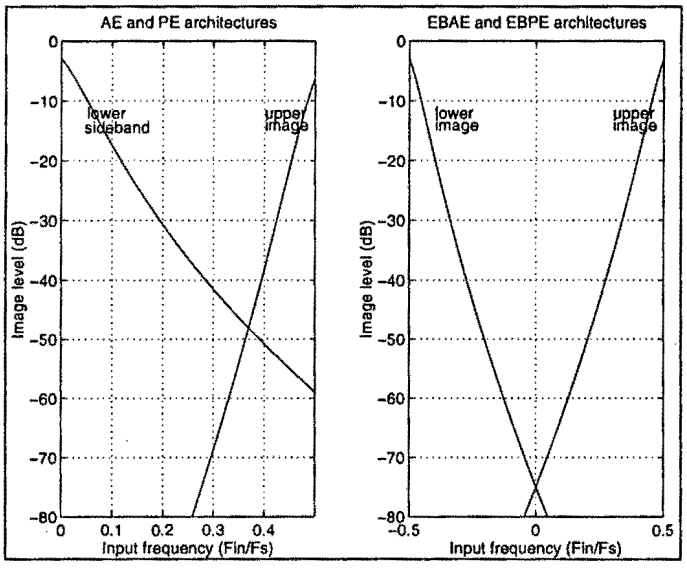

Figure 3.12. *Image/sideband level vs. input frequency for non-ideal filtering*

3.5 MIXER IMPERFECTIONS

It was found in the literature study [10] that the two most important mixer imperfections having an influence on spurious signal levels are *LO leakage* and *intermodulation products*. These two factors are defined and briefly discussed in the following sections. LO leakage levels and intermodulation harmonic charts are also included. These are based on typical values for wideband mixers, as found in a number of datasheets [8,9,10].

3.5.1 LO leakage

LO leakage can be defined as the ratio in dB between the LO frequency power level incident at the LO port of the mixer and the LO frequency power emanating from the IF port. For the down-conversion stage this poses no problem since the LO frequency will be eliminated by the lowpass anti-aliasing filters. After the up-conversion stage, however, the LO frequency will be situated in the centre of the information band (for the EBAE and EBPE architectures). The LO leakage spurious signal will therefore appear at the centre of the information band in the output signal of these architectures. For the other two architectures (AE and PE) the LO leakage component will be situated at the edge of the information band.

Typical values for LO leakage levels given in datasheets are [8]:
20 to **35dB** for 'low-frequency' mixers (IF = DC to 1000 MHz);
20 to **25dB** for 'high-frequency' mixers (IF = 5 MHz to 4000 MHz);

3.5.2 Intermodulation products

Ideally, the output of a mixer would contain signal components only at the modulated frequencies of the LO and the input signal. In practical mixers, however, the output also contains undesirable components located at numerous other frequencies. These frequency components are called *intermodulation products*. Two types of intermodulation (IM) products exist: single-tone and multiple-tone. Single-tone IM products are composed of a single input RF signal mixing with the LO and have the following frequencies [10]:

$$f = \pm mf_R \pm nf_L \quad \text{.....(3.8)}$$

where m = 1,2,3,... f_R = frequency of input signal
n = 1,2,3,... f_L = frequency of LO

Multiple-tone intermodulation products are composed of two or more input RF signals mixing with the LO, and have the following frequencies [10]:

$$f = \left(\pm m_1 f_{R1} \pm m_2 f_{R2} \pm m_3 f_{R3} \ldots\right) \pm nf_L \quad \text{.....(3.9)}$$

where $m_1, m_2, m_3, \ldots = 0,1,2,3, \ldots$

$n = 0,1,2,3, \ldots$

The level of output power of individual IM products is greatly affected by input LO and RF power levels and frequencies. However, charts exist that show general trends in intermodulation suppression. *Tables 3.3* and *3.4* are two such charts showing trends for single-tone intermodulation suppression for high-frequency and low-frequency double-balanced mixers [8]. Suppression numbers are for an RF signal level at -10dBm and LO signal level at +7dBm, which represent typical drive values for mixers. It can be noticed that the even-by-even IM products (both n and m even) are suppressed more than the odd-by-odd products. This is a typical characteristic of a double-balanced mixer.

Table 3.3 Intermodulation suppression - High frequency mixers

LO Harmonic / RF Harmonic	1	2	3	4	5
1	0	35	18	40	35
2	55	55	55	58	55
3	65	>70	65	>70	65
4	>70	>70	>70	>70	>70

Table 3.4 Intermodulation suppression - Low frequency mixers

LO Harmonic / RF Harmonic	1	2	3	4	5
1	0	42	10	30	30
2	53	71	59	58	62
3	63	70	69	>70	64
4	>70	>70	>70	>70	>70

Intermodulation charts are not generally tabulated for multiple-tone IM products because each coefficient (m_1, m_2, m_3, ... and n) requires its own axis on the chart. Charts for single-tone IM products, on the other hand, require only two axes for m and n. One important multiple-tone IM product specified in most datasheets is the 2-tone, 3rd-order suppression of a mixer. Two-tone, third-order IM products have the following frequencies:

$$(\pm 2f_{R1} \pm f_{R2}) \pm f_L \quad and \quad (\pm f_{R1} \pm 2f_{R2}) \pm f_L \qquad \text{.....(3.10)}$$

This value represents the highest IM product introduced by a mixer for a 2-tone input. It is used to compare different mixers and also to determine the spurious signal level introduced by mixer imperfections. The 2-tone, 3rd-order suppression is also very dependent on RF input signal and LO signal power levels. This relation is illustrated in *Figure 3.13* [8]

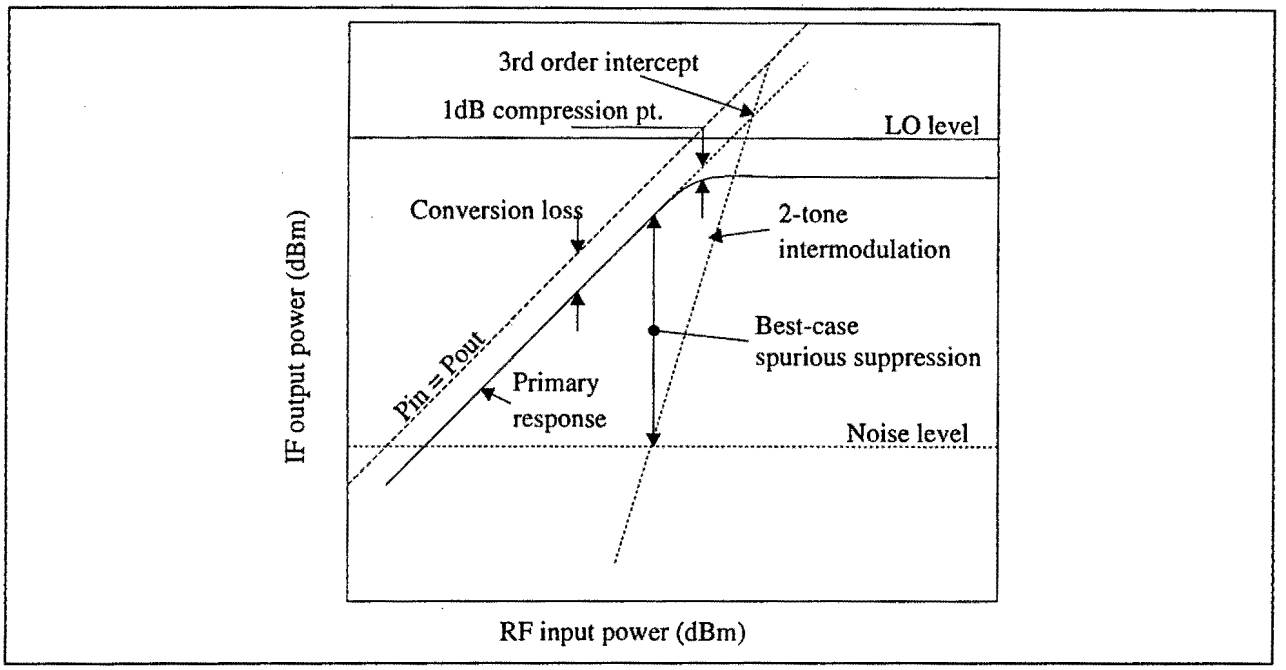

Figure 3.13 Intercept diagram

The primary response indicates the power level of the desired output signal. The power of the 2-tone, 3rd-order IM product increases at twice the rate than that of the primary response as the input power is increased. The conversion loss, 1dB compression point and best-case spurious level suppression are also indicated on the figure. The 3rd-order intercept point, as indicated in the figure, is usually a good indication of the IM product suppression capability of a mixer. This 3rd-order intercept point changes as the LO drive level increases. This relationship is shown in *Table* 3.5 [8] for typical LO drive levels.

Table 3.5 3rd-order intercept point vs. LO drive level

LO Drive Level	LO Drive Level Range (dBm)	Typical Input Intercept Point per min LO Drive Level (dBm)
Low Drive	+10 to +13	+14
Medium Drive	+13 to +15	+17
High Drive	+17 to +19	+20
Super High Drive	+20 to +23	+25

As can be seen from the analysis, the spurious level contribution of mixers is very complex and implementation-specific. It would therefore be difficult to generalise by giving typical values for spurious signal levels without prior knowledge of particular system details. The tables and other data given in this section are therefore only guidelines in order to present an idea of the extent of spurious levels introduced by the aforementioned mixer imperfections.

3.6 System Thermal Noise

The contribution of thermal noise to the system spurious signal level is once again a very implementation-related problem. The system noise level (or signal-to-noise-ratio) depends on numerous practical parameters which will vary to a large extent from system to system. This section merely attempts to illustrate the principles of system noise analysis. This is done by making an analysis of the system noise of a simple, but typical BDR reciever configuration (illustrated in *Figure 3.14*). This is an example of a typical front-end of the AE BDR architecture. The following section illustrates a useful method of system noise analysis.

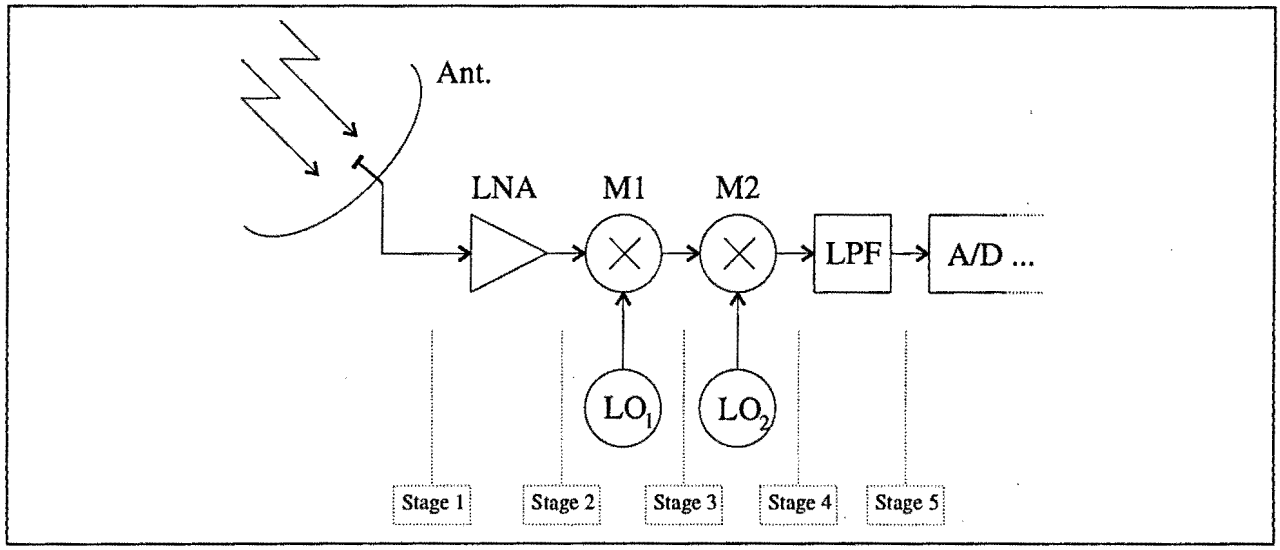

Figure 3.14. BDR Receiver front-end

System noise temperature is a useful concept in receivers, since it provides a way of determining how much thermal noise is generated by active and passive devices in the receiving system. At microwave frequencies, all objects with physical temperature greater than 0°K generate electrical noise at the receiver frequency. The available noise power is given by [11, *pp113, equation 4.12*]:

$$P_n = kT_nB \quad \text{.....(3.11)}$$

where k = Boltzmann's constant = 1.38×10^{-23} J/K

T_n = noise temperature of source in Kelvins

B = bandwidth of power measurement device in Hertz

To determine the performance of a receiving system we need to be able to find the total thermal noise against which the signal must be demodulated. We do this by determining the *system noise temperature*, T_s. T_s is the noise temperature of a noise source, located at the input of a noiseless receiver, which gives the same noise power as the original receiver, measured at the output of the receiver. *Figure 3.15* illustrates the equivalent circuit of the receiver. The noisy devices are replaced by a single noise source plus noiseless amplifiers.

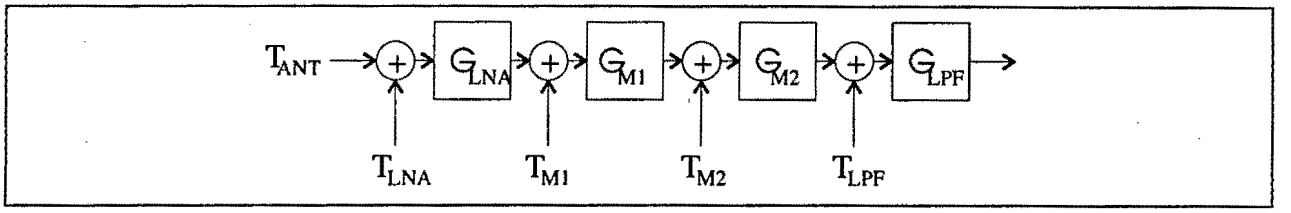

Figure 3.15. Equivalent circuit of receiver front-end

Using this model, the system noise temperature can now be calculated as [11, *pp116, equation 4.16*]:

$$T_s = T_{ANT} + T_{LNA} + \frac{T_{M1}}{G_{LNA}} + \frac{T_{M2}}{G_{LNA}G_{M1}} + \frac{T_{LPF}}{G_{LNA}G_{M1}G_{M2}} \quad \text{.....(3.12)}$$

It can be seen that if the low-noise amplifier (LNA) gain is large, the system noise temperature can be approximated by the first two terms. The noise temperatures of the front-end components (i.e. before the first amplifier stage) therefore make the major contribution to system noise.

Once the system noise temperature has been calculated, the noise contribution of the system can be determined by calculating the system *noise figure*. Noise figure (NF) is frequently used to specify the noise generated within a device. The operational noise figure is defined by the following formula [11, *pp117, equation 4.18*]:

$$NF = \frac{(S/N)_{in}}{(S/N)_{out}} \quad \text{.....(3.13)}$$

The relationship between the noise figure and noise temperature is [11, *pp117, equation 4.19*]:

$$T_s = T_0(NF - 1) \quad \text{.....(3.14)}$$

where T_0 is the reference temperature - usually 290K.

If the peak input power and dynamic range of an A/D converter are specified, the peak input to the receiver as well as the system noise floor can be calculated. The peak input power can be calculated by simply dividing the desired maximum output by the total cumulative gain of the system. Noise floor can then be calculated by using the noise figure of the system and the peak input power. The following example illustrates this method of signal/noise floor calculation.

Suppose that a 6-bit A/D converter (i.e. 36dB dynamic range) is used which saturates with an input power level of 1mW (-30dB). The other system parameters are as follows:

LNA : Gain = 40dB
NF = 1.8
M1: Gain = -7dB
NF = 2.24
M2: Gain = -8dB

NF = 2.51

LPF: Conversion loss: 1dB

NF = 1.12

Figure 3.16 illustrates the results of the signal/noise power calculations. Plot (1) illustrates the peak signal level, the minimum detectable signal, and the noise floor level as one progresses through the system. It can be seen that the input signal has to be in the range of -90.12dB to -54.0dB for the output to lie in the detectable A/D range. This means that the input signal has to be limited to -54dB, while the input noise has to remain below -96.78dB. The best-case signal-to-noise ratio is illustrated in plot(2). It decreases slightly as noise is added by each system component. Plot(3) illustrates the system NF, which is dominated by the effect of the LNA. It reflects the importance of using a front-end amplifier with a low NF.

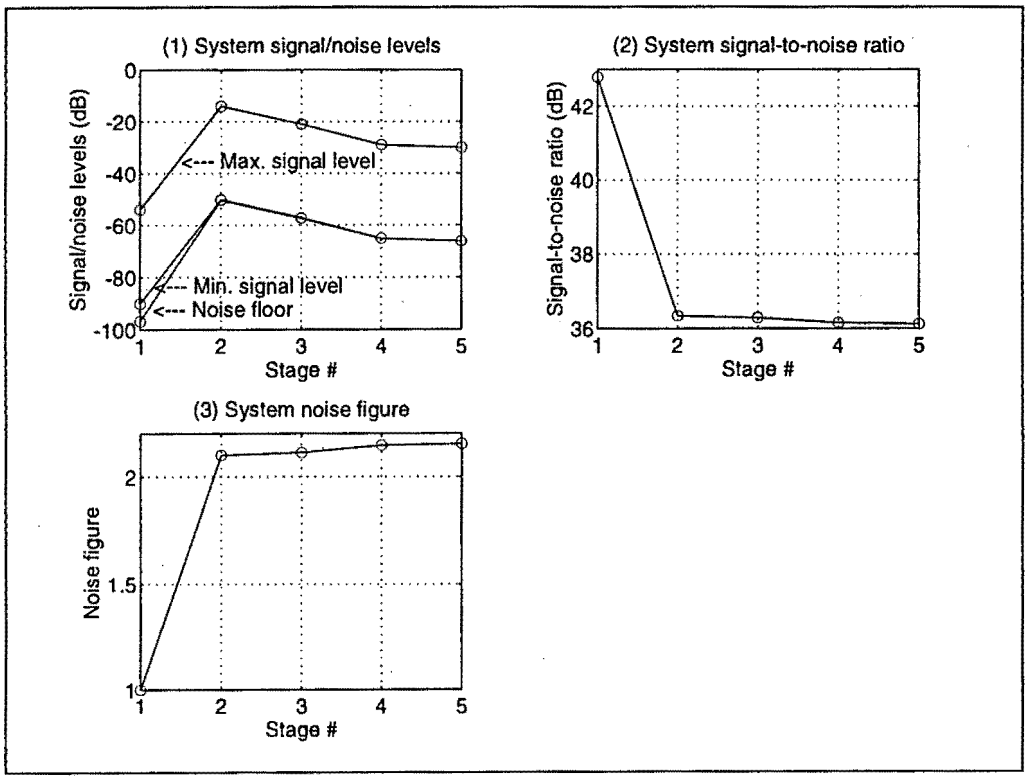

Figure 3.16. Signal/noise power analysis of receiver front-end.

3.7 SPURIOUS SIGNAL REDUCTION TECHNIQUES

An interesting outcome of the literature study was the claim by Wiegand [12] that modulation of the local oscillator by a random waveform could drastically reduce spurious levels in digital storage units such as those described in this dissertation. This decreases the number of required bits of digitisation for a specified spurious level. In addition to reduced spurious, a useable bandwidth up to the full sampling frequency (i.e. twice that for conventional architectures) was possible with this technique "thereby providing an overall 75% reduction in digital memory requirements". Further investigations revealed several articles on such 'spurious reduction techniques' [12] - [16].

Since spurious levels and bandwidth limitations are of major interest in this dissertation, it was decided to investigate these techniques and, by using simulations, comparing the signal fidelity to that of the conventional architectures.

3.7.1 Basic configurations

Two basic configurations were found in the literature. A brief description of each technique is given below:

3.7.1.1 Local oscillator modulation

This technique, described in detail by Wiegand [12], can be used with any one of the four architectures described in *Section 2.2* by simply modulating the local oscillator with a random waveform. The incoming RF signal is applied to the mixer along with the modulated local oscillator to produce an IF signal for application to the A/D converter. During the reconstruction process, the local oscillator (which is modulated with the identical waveform used in the down-conversion) is applied to the output mixer along with the stored signal to produce the original input RF signal. The technique, as applied to an AE architecture is illustrated in *Figure 3.17.*

The local oscillator can be frequency- or phase modulated. A random modulation waveform is preferred, as it gives better spur reduction. The modulation waveform can be a repeating pattern, or even a pseudo random waveform, which is easy to generate and duplicate in the reconstruction cycle. The frequency and amplitude of the modulation wave are the two important properties which determine how effectively the spurious levels are suppressed, as will be discussed in the simulation results.

The modulation in the local oscillator signal causes the spurs to decorrelate in the output signal when it is converted by the mixers. The spurs, rather than being at a level sufficient to influence the intelligence in the converted signal, are spread over a noise floor in the signal. As the local oscillator frequency changes, the position of the sideband image as well as that of the spurs changes relative to the position of the desired signal, thus causing the spurs and the sideband to decorrelate. This concept is illustrated for three different local oscillator (LO) frequencies in *Figure 3.18.* Since this modulation also reduces

the sideband images, it changes the previously single sideband architectures (the AE and PE) into double sideband configurations, therefore doubling the available bandwidth.

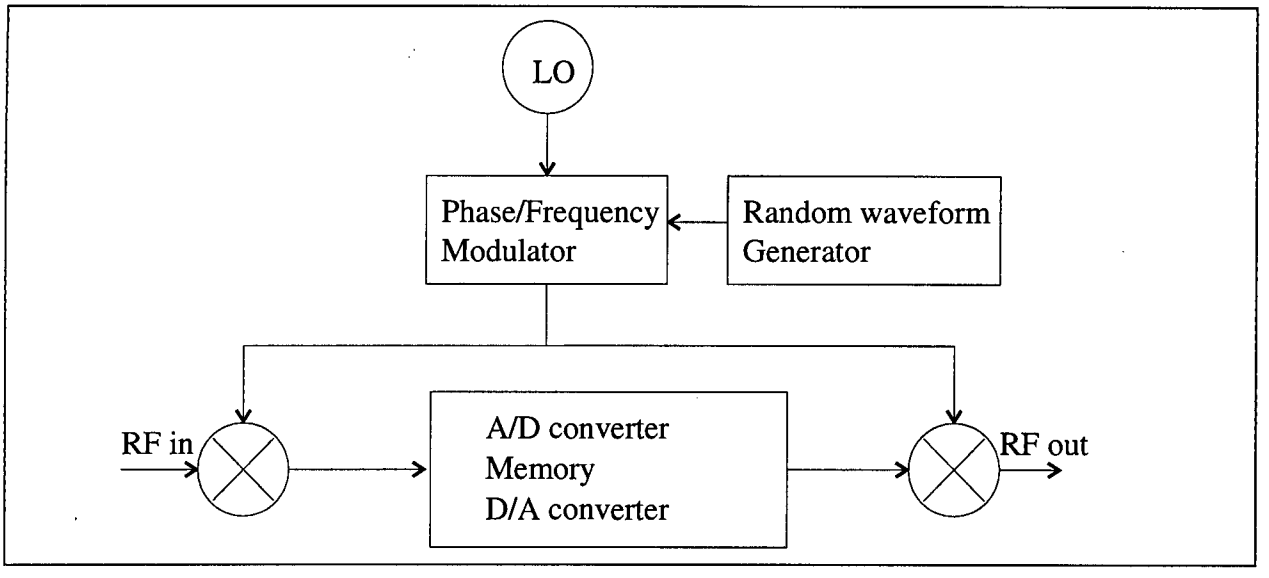

Figure 3.17. Block diagram of local oscillator modulation technique

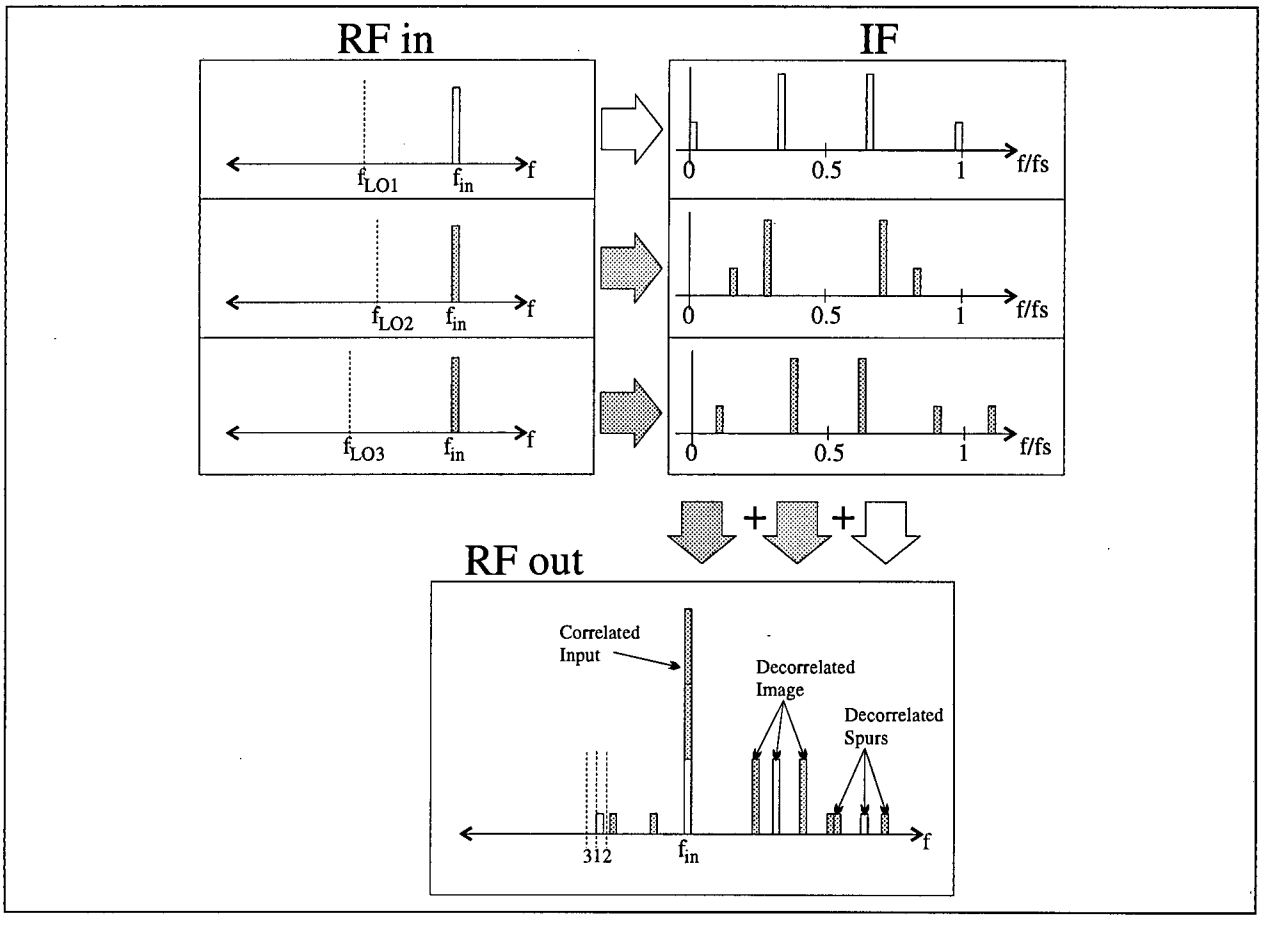

Figure 3.18. Local oscillator modulation to reduce spurious and sideband images

3.7.1.2 Random linearisation

This technique can only be used in quadrature channel architectures (EBAE and EBPE). It makes use of the quadrature up- and down-conversion, together with the principle of 'Random linearisation of A/D converters', as described by Barnes and Horn [16]. By adding an identical random waveform to the in-phase and quadrature channels (illustrated in *Figure 3.19*), this technique reduces the spurious levels. Unlike the previous technique, this one has no bandwidth extension capabilities.

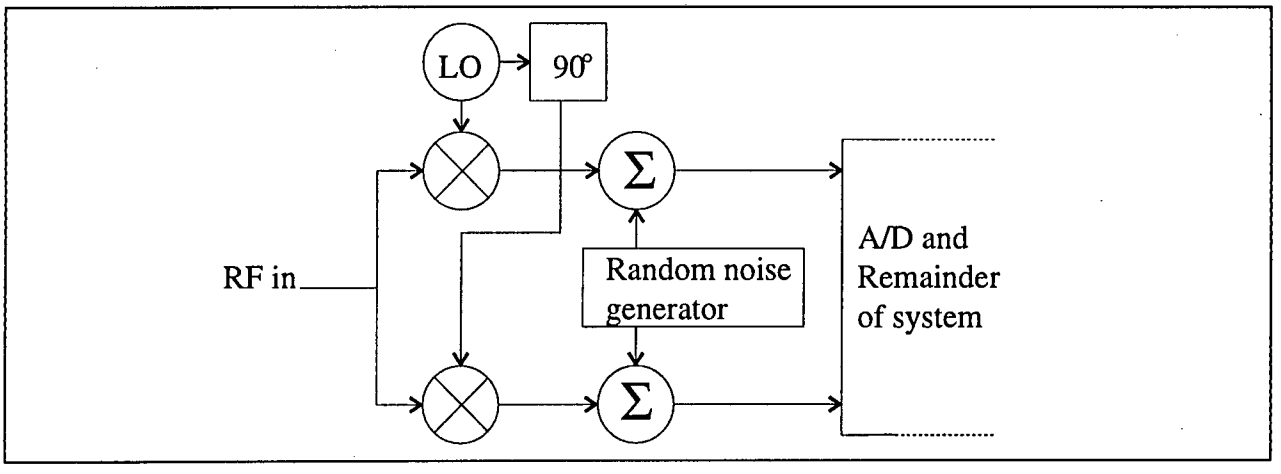

Figure 3.19. Block diagram of 'Random linearisation' spurious reduction technique

3.7.2 Simulation results

3.7.2.1 Local oscillator modulation

Very little is mentioned in the literature about the extent of the spurious suppression achievable in such systems. Optimum modulation waveforms are also not mentioned. Many simulations were therefore done to determine possible factors having an influence on the extent of spurious suppression and to find a 'good' LO modulation. A summary of such factors is given below.

3.7.2.1.1 Factors influencing spurious suppression

- **Type of modulation** - As mentioned earlier, either frequency or phase modulation of the LO can be used. The expressions for the local oscillator signal after frequency- or phase modulation are respectively:

$$Lo_{FM}(t) = \sin\left(2\pi t\left[f_{LO} + A \cdot n_B(t)\right]\right) \quad \text{.....(3.15)}$$

$$Lo_{PM}(t) = \sin\left(2\pi f_{LO} t + A \cdot n_B(t)\right) \quad \text{.....(3.16)}$$

  where f_{LO} is the local oscillator frequency and $n_B(t)$ is the modulation waveform with amplitude A and bandwidth B.
- **LO Modulation waveform** - Band-limited Gaussian distributed white noise yielded the best results. Other possibilities that were investigated are sinusoidal and pseudo-random noise waveforms, which have the advantage of easy duplication.
- **LO Modulation waveform amplitude and bandwidth** - Once a modulation type and waveform have been chosen, amplitude and bandwidth of the modulation wave (A and B respectively in

Equations 3.15 and *3.16*) are the two parameters which can be set in order to obtain the best spurious suppression. *Figure 3.20* illustrates an example of a simulation for a phase modulated local oscillator where the amplitude and bandwidth of the modulating wave are changed in order to find an optimum modulation. This example was done for the AE configuration for a 1800 sample pulsewidth and for 1-bit quantisation. For each amplitude/frequency point on the graph, the output spectrum of the AE architecture was determined and the magnitude of the maximum spurious signal calculated and recorded on the graph (the black areas show optimum parameters for this specific configuration). Graphs like this can be used to find the best LO modulation waveform for a given encoding architecture, modulation type and pulsewidth.

- **Number of quantisation bits, recorded pulsewidth and encoding architecture -** It was found that all of these factors have an influence on the optimum modulating waveform as well as on the extent of spurious suppression. In general, the spurious suppression is more dramatic for coarse quantisation (1-bit and 2-bit) and for long pulses.

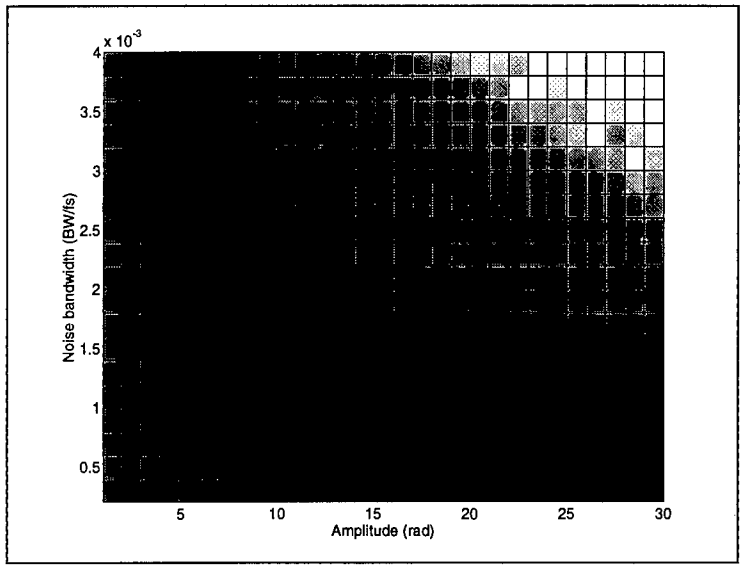

Figure 3.20. *Spurious suppression vs. modulation waveform amplitude and noise bandwidth*

The large number of factors that have to be taken into consideration therefore makes it difficult to find general guidelines for a 'good LO modulation waveform'. It would be necessary to make an investigation into each individual case of encoding architecture, number of quantisation bits and pulsewidth, like the one illustrated in *Figure 3.20.*

3.7.2.1.2 Simulation results

Some simulation results are given below in order to illustrate the spurious suppression and bandwidth extension capabilities of this technique. The output spectra illustrated in *Figure 3.21* are for the following special case:

- 1-bit quantisation
- 1000 memory sample pulsewidth
- AE architecture

- Phase modulation of the LO
- Band-limited Gaussian distributed white noise modulation signal.

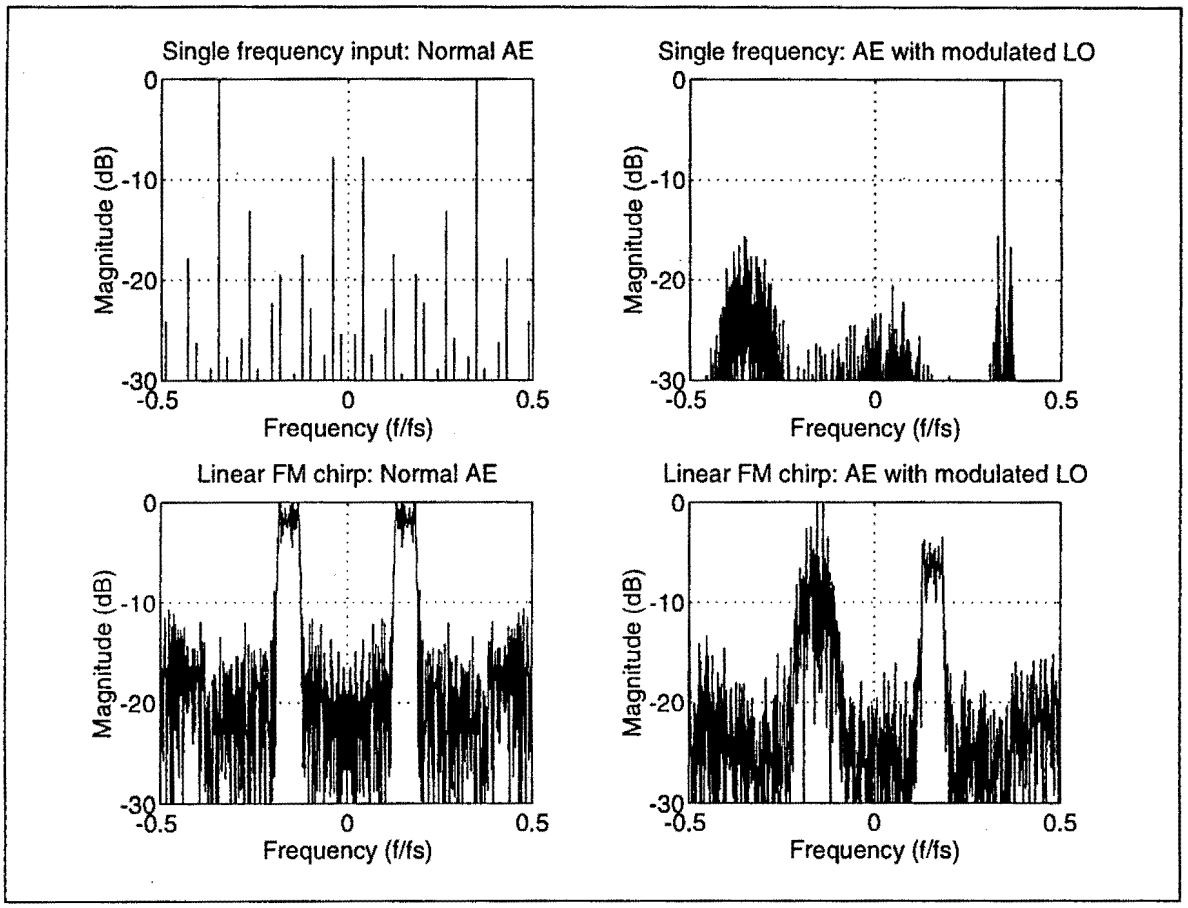

Figure 3.21. Output spectra for comparing normal encoding with LO modulation techniques

The first two graphs illustrate the output spectra for a single tone input. It illustrates the drastic spurious level improvement (in this case nearly 10dB) over conventional architectures. The bandwidth extension caused by the decorrelation of the sideband frequency can also be seen from the 'Modulated LO' graph.

The other two graphs illustrate the output spectra for a wideband chirp input. It can be seen that this technique shows no improvement over the conventional method. It was found throughout the simulations that periodic signals benefit a great deal from LO modulation techniques. Non-periodic signals like the wideband chirp, show hardly any improvement at all.

Simulation results showed that there is no significant increase in the input-output phase jitter caused by such a system compared to conventional architectures.

3.7.2.1.3 Conclusions

It is evident that this local oscillator modulation technique has significant advantages (in terms of spurious levels and bandwidth) for the capturing of periodic data such as a single-tone signal. In such

cases, a suitable modulation waveform has to be found, which is dependent on a number of system factors. For general communication and other wideband signals, however, this technique only adds complexity to the system without having meaningful benefits.

3.7.2.2 Random linearisation

Once again no literature was available on optimum modulation waveforms. Since the noise is added to the quadrature channels, the matter is simplified somewhat. It is only the amplitude and bandwidth of the noise which has an influence on the optimum modulation parameters. Similar analyses to the one illustrated in *Figure 3.20* can therefore be done to assess the best modulation parameters for a specific configuration (including number of bits quantisation, pulsewidth and encoding architecture).

3.7.2.2.1 Simulation results

A sample of the simulation results is given below to illustrate the spurious suppression capabilities of this technique. The output spectra illustrated in *Figure 3.22* are for the following special case:

- 1-bit quantisation
- 1000 memory samples pulsewidth
- EBAE architecture
- Bandlimited Gaussian white noise is used as the noise source

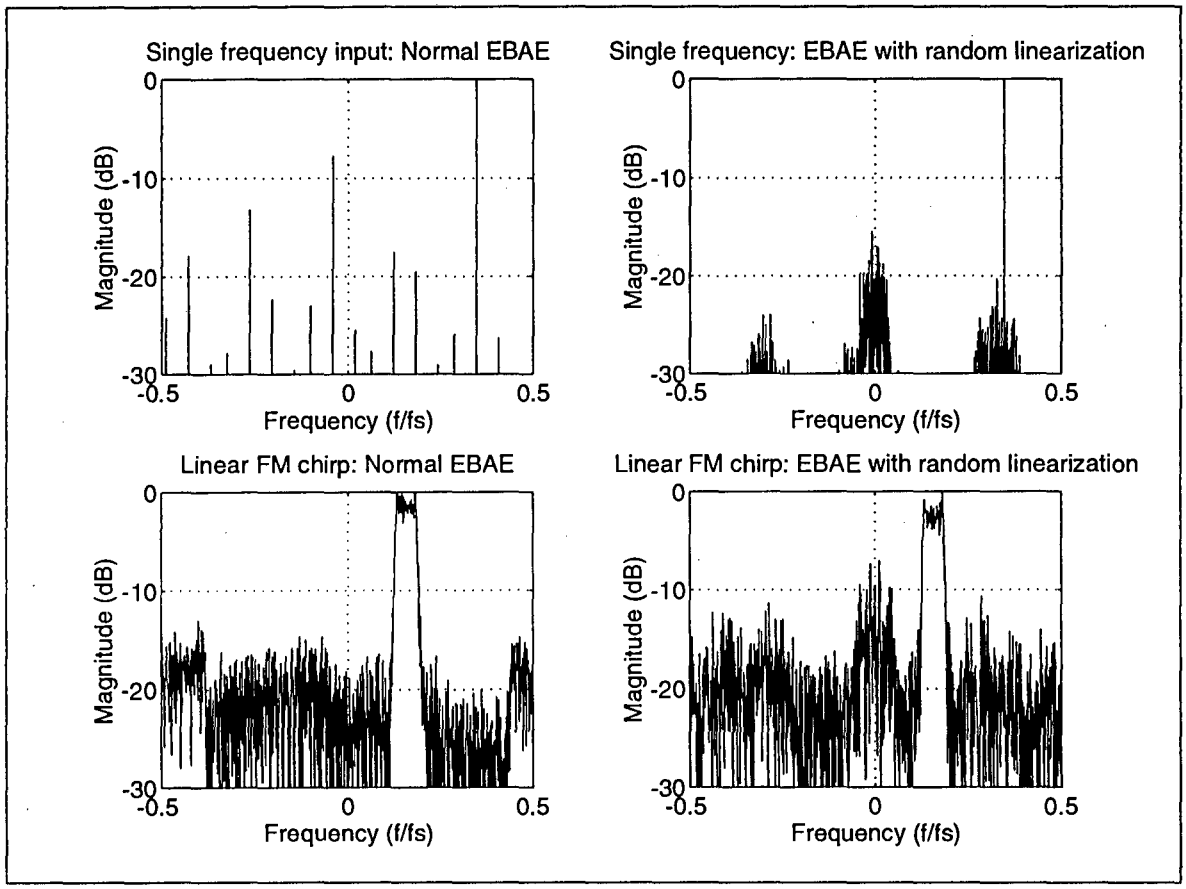

Figure 3.22. Output spectra for comparing normal encoding with Random linearisation techniques

The first two graphs illustrate the output spectra for a single tone input. It can be seen that once again the technique shows a spurious level improvement (in this case about 9dB) over conventional encoding architectures. The other two graphs illustrate the output spectra for a wideband linear FM chirp input. It can be seen that the random linearisation process degrades the quality of the stored signal somewhat, rather than enhancing it. It can therefore be concluded that periodic signals benefit from the random linearisation technique, while non-periodic signals show no improvement.

Chapter 4

Phase / Frequency accuracy

This system characteristic is of special importance to systems using phase modulated or phase encoded signals. In such systems it is often required that the phase error, phase jitter or frequency error do not exceed a certain threshold in order to regain the encoded information with sufficient accuracy. Simulations were therefore done to assess the extent to which the four proposed signal storage modules influence the phase and frequency accuracy of an incoming signal.

The terms phase error, phase jitter and frequency error as used in this section are defined below to avoid confusion. For the purpose of this analysis, the defenitions are as follows:

- *Phase error* is defined as the **average** input/output phase difference or phase offset between the input and output signals: $\phi_{error} = \mathrm{E}(\phi_{out} - \phi_{in})$ where E(x) denotes the expected value of x.
- *Phase jitter* is defined as the maximum instantaneous deviation of the input/output phase difference from the average phase difference (i.e. the deviation of the phase difference from the phase error): $\hat{\phi}_{jitter} = \max[(\phi_{out} - \phi_{in}) - \mathrm{E}(\phi_{out} - \phi_{in})]$.
- *Frequency error* is defined as the average difference between the input and output frequencies: $f_{error} = \mathrm{E}(f_{out} - f_{in})$

4.1 PHASE ERROR

The three main sources of phase error in the systems are:

4.1.1 Digital time delay

The time delay (throughput delay) caused by the intentional and/or non-intentional delay of the digital data through the RAM and other digital circuitry (e.g. latches) is hardware and application dependent. Such a time delay causes a linear phase delay and is thus easy to calculate. The Fourier transform of a signal $f(t)$ delayed by a time t_0 is given by:

$$F\big(f(t-t_0)\big)=e^{-j\omega t_0}\cdot F(f(t)) \quad \text{.....(4.1)}$$

The phase error caused by a time delay of t_0 seconds is therefore:

$$\phi_{error}=-2\pi f_{in}\cdot t_0 \quad \text{.....(4.2)}$$

where f_{in} is the input frequency.

4.1.2 Sampling phase error

Figure 4.1 shows the effect of a sample-and-hold operation on a sinusoidal wave. The timing error caused by the sampling can be considered as a combination of phase error and phase jitter, as illustrated in the figure . The phase error caused by sampling is therefore:

$$\phi_{error}=\frac{360^\circ\left(\frac{f_{in}}{f_{sample}}\right)}{2} \quad \text{.....(4.3)}$$

This amounts to a very small phase error relative to the digital timing error and filter delay and can therefore be ignored in most cases. The phase jitter caused by sampling, however, is quite substantial, as will be discussed in *Section 4.2.1.*

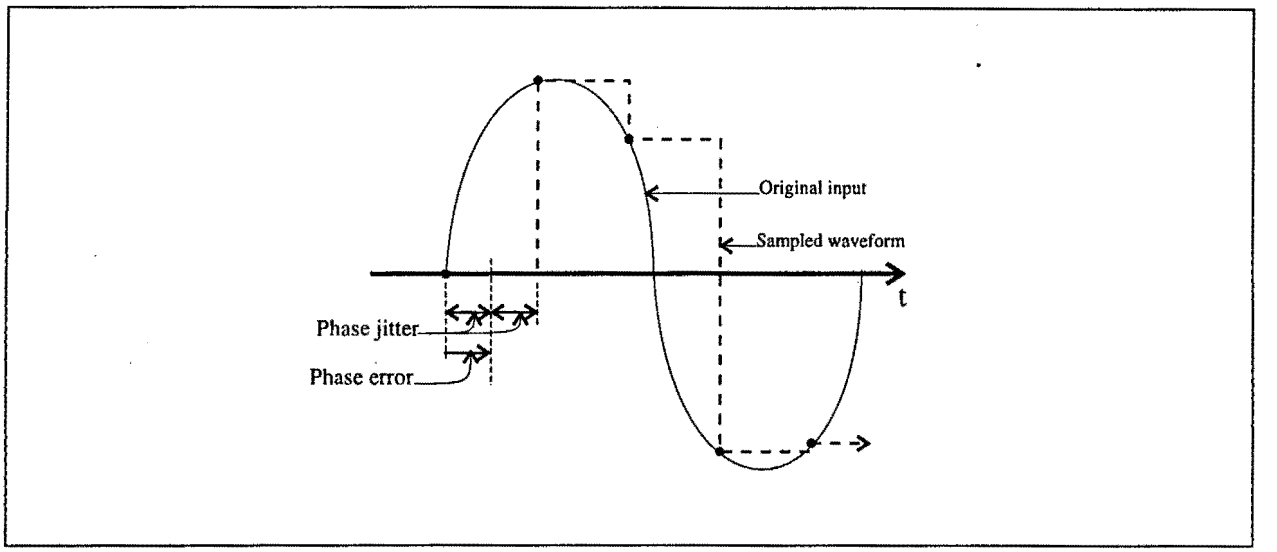

Figure 4.1. Phase error/jitter caused by the sample-and-hold operation

4.1.3 Filter phase delay

The phase error caused by the filters is dependent on their order, type and bandwidth. In the AE and PE configurations the error is caused by the series connection of two lowpass and one bandpass filter. In the other two configurations only two lowpass filters contribute to the error. The phase error therefore accumulates as the signal moves through the module and the total filter phase delay can easily be calculated by adding the phase responses of the cascaded series of filters.

4.2 PHASE JITTER

There are various sources contributing to the total phase jitter induced into a signal by the capturing and repeating processes of the BDR module. The most important sources are discussed in the following sections.

4.2.1 Quantisation/sampling phase jitter

The deformation of a waveform caused by the quantisation and sample-and-hold operations in the sampling process is probably the most important source of phase jitter. It is mainly a function of the quantisation coarseness, but is also influenced by the relation between the input- and sampling frequency. As mentioned in *Section 3.4*, the image/sideband which is present due to imperfect filtering, also induces phase jitter. Since it is difficult to isolate the effects of the individual sources of phase jitter, all of the abovementioned factors are combined in this section and in the simulation results which follow.

4.2.1.1 Quantisation phase jitter

Theoretically the phase jitter caused by quantisation (without sampling) is frequency-independent. With reference to Schneider [17], the phase resolution (i.e. the peak-to-peak phase jitter) for an *amplitude encoded* waveform is given by:

$$\phi_{resolution} = \arcsin\left(\frac{1}{2^{n-1}}\right)$$

$$\therefore \hat{\phi}_{jitter} = \frac{\arcsin\left(\frac{1}{2^{n-1}}\right)}{2} \quad \text{.....(4.4)}$$

where n is the number of quantisation bits (for the EBAE architecture, n is the number of quantization bits used in each of the A/D converters in the I and Q channels). The corresponding phase jitter for the *phase encoded* techniques is [17]:

$$\phi_{resolution} = \frac{360°}{2^n}$$

$$\therefore \hat{\phi}_{jitter} = \frac{360°}{2^{n+1}} \quad \text{.....(4.5)}$$

4.2.1.2 Sampling phase jitter

Referring to *Section 4.1.2* and *Figure 4.1* the phase jitter caused by a sample-and-hold operation (without quantisation) is directly proportional to the ratio of the input and sampling frequencies, as shown by the following equation:

$$\hat{\phi}_{jitter}(f_{in}) = \frac{\left(360° \cdot \frac{f_{in}}{f_{sample}}\right)}{2} \quad \text{.....(4.6)}$$

The phase jitter caused by sampling therefore increases with an increase in input frequency and approaches a maximum of 90° for an input signal with a frequency near the Nyquist limit of $f_{sample}/2$.

4.2.1.3 Simulation results

It can be seen from *Equations 4.4, 4.5* and *4.6* that the separate operations of sampling and quantisation induce very high levels of phase jitter. It is, however, important to remember that filtering of these signals smoothes the waveform and reduces the phase jitter substantially. The aim of the simulation is therefore to obtain an insight into the combined effect of quantisation, sampling and filtering on the phase jitter of the output signal. The simulation also illustrates the input frequency dependence of the phase jitter. The signal storage architectures as illustrated in *Figures 2.1* to *2.4* were thus considered as a whole. A sinusoid with known phase was used as input to each unit. The output waveform as well as its phase was calculated. The input phase was then subtracted from the output phase to obtain the phase error and phase jitter caused by the relevant unit.

The results of the simulations for 2-bit, 4-bit and 6-bit quantisation are illustrated in *Figure 4.2.* The input frequency was swept over the whole information band. Sixth order Butterworth bandpass- and twelfth order Butterworth lowpass filters were once again used to represent typical practical filters. From the simulation results the following conclusions can be made:

- As was the case for the simulations on the maximum spurious, the AE configuration shows the best results, followed by the phase encoded techniques which show similar performance. In general, the EBAE configuration has the highest phase jitter. It can therefore be assumed that the magnitude of the phase jitter is related to the spurious level.
- The phase jitter is largely frequency independent, except for a sharp increase near the edges of the band due to the upcoming images/sideband. This indicates that the phase jitter caused by sampling (without quantisation) is cancelled to a large extent by the filtering process.
- The phase jitter is very much dependent on the number of bits quantisation. It can therefore be concluded that the quantisation process is the predominant source of phase jitter. This can be confirmed by calculating the phase jitter caused by 4-bit quantisation, given in *Equations 4.4* and *4.5* (3.6° for AE, 11.25° for PE and EBPE, 15° for EBAE). These values are slightly lower, but nevertheless correspond well to the results obtained in the simulation.
- It can therefore be concluded that a good approximation for the total phase jitter in BDR modules can be obtained by calculating the phase jitter caused only by quantisation (*Equations 4.4* and *4.5*). This statement remains valid for the central parts of the information band. The phase jitter at the upper and lower edges are dominated by phase jitter caused by insufficient image/sideband suppression, and are therefore dependent only on the type and order of the filters used in the application.

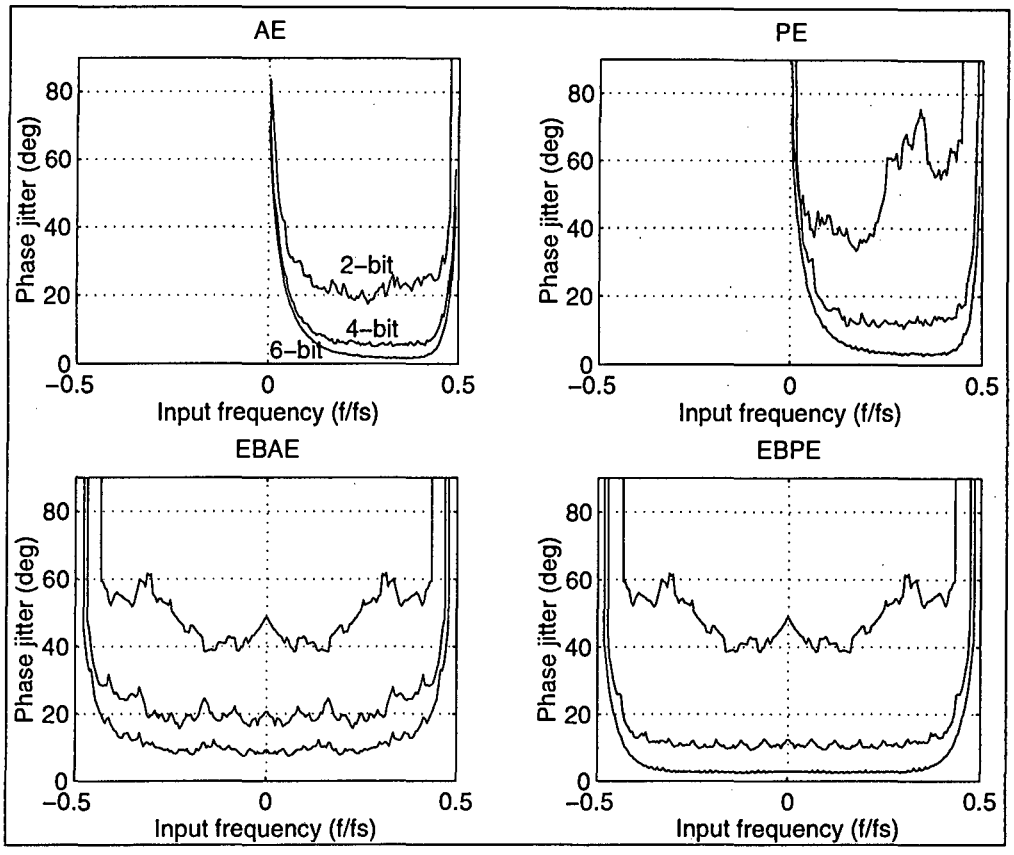

Figure 4.2. Phase jitter vs. input frequency for different BDR architectures

4.2.2 Dynamic range

As in *Section 3.3*, a simulation was done to investigate the effect of the input signal level on the output waveform fidelity, only this time in terms of phase jitter.

The simulation was done for all four configurations, and the results for the 4-bit case are illustrated in *Figure 4.3*. The results for the 2-bit and 6-bit quantisation are given in *Appendix B6*. Once again the input signal level was varied between -20dB and +20dB in 0.4dB steps. As was the case in *Section 3.3*, the simulation was performed for different input frequencies and then averaged to obtain a more general result. From the results the following can be noted:

- As can be expected, the phase encoding techniques are insensitive to input signal level.
- As explained for the maximum spurious in *Section 3.3*, the phase jitter of the amplitude encoded techniques increases to both sides of the 0dB optimum input signal level to a saturation value corresponding to the one-bit quantisation case.

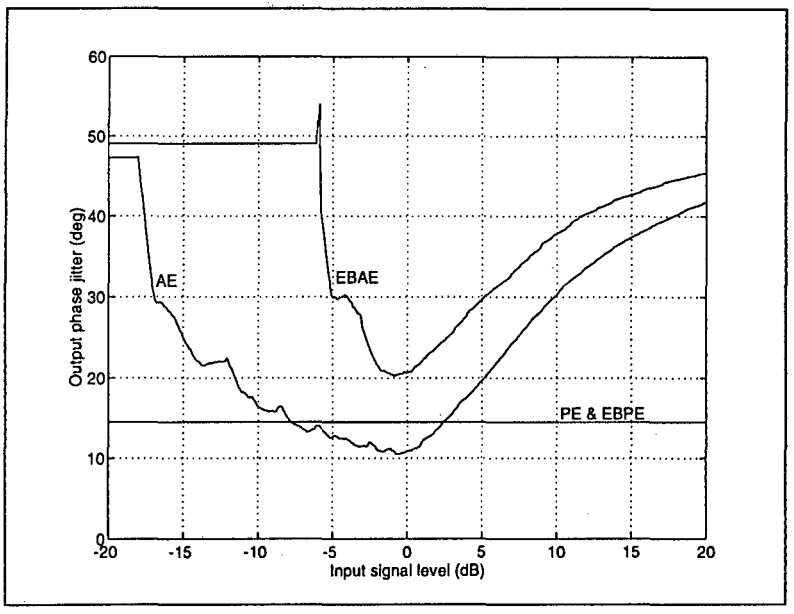

Figure 4.3. Phase jitter vs. input signal level for 4-bit quantisation

4.3 FREQUENCY ERROR

4.3.1 Pulsed CW frequency error

Theoretically, the capturing and recalling of an infinitely long continuous wave (CW) using the proposed encoding architectures would result in a zero average frequency error. However, when a pulse of finite length is stored, which is obviously the more relevant case, a small frequency error, the magnitude of which depends on the phase jitter and pulsewidth, can occur.

Frequency can be estimated by recognising that frequency is the rate of change of phase. The (average) frequency of a finite length pulse can therefore be calculated by dividing the total accumulated phase by the pulselength. To calculate the frequency error of a pulse, the total accumulated phase error must be divided by the pulsewidth. Recognising that the total accumulated phase error can never exceed the phase resolution (i.e. 2 times the maximum phase jitter) at that frequency, the maximum frequency error of a finite length CW pulse can be calculated as follows:

$$F_{error\_max}(f) = \frac{\phi_{resolution}(f)}{pulsewidth} \quad \text{.....(4.7)}$$

The phase *error* as defined in 4.2 only results in a phase offset, and this has no influence on the instantaneous frequency

Since the phase jitter is dependent on the input frequency as well as quantisation coarseness (see *Figure 4.2*), the maximum frequency error of a finite length pulse would therefore also be a function of the input frequency and quantisation coarseness. The phase jitter of a specific architecture, quantisation coarseness and input frequency therefore have to be known in order to be able to calculate the maximum frequency error of a pulsed CW signal.

4.3.2 FML mode

In the FML (Frequency Memory Loop) mode, the BDR storage unit aims to mimic a long CW signal by recalling a short pulse (which is stored in its memory) many times in a head-to-tail fashion. This causes the output signal to contain a phase discontinuity at each repetition period of the short pulse, thus inducing a frequency error as shown in the analysis below:

Figure 4.4 illustrates the output waveform of a short pulse with length τ repeated N times to produce an output pulse of length τ_2 (i.e. $\tau_2 = N\tau$). A phase error of ψ is occurs at every repetition period.

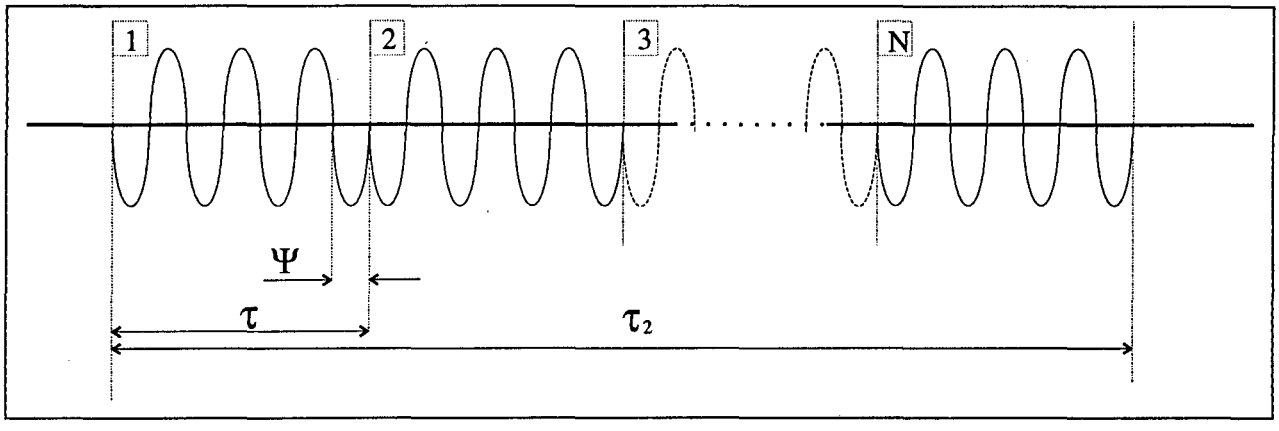

Figure 4.4. Typical output wave in the FML mode

The derivation of an expression for the frequency spectrum, $G(\omega)$, of such a signal is given in *Appendix A1*, of which the results are given below:

$$G(\omega) = 2\pi\tau_2 \cdot \sum_{n=-\infty}^{\infty} F_n \cdot Sa\left(\frac{\tau_2}{2}(\omega - n\varpi)\right) \quad \text{.....(4.8)}$$

where

$$F_n = \pi\left[Sa\left(\frac{\tau}{2}(n\varpi - \omega_o)\right) + Sa\left(\frac{\tau}{2}(n\varpi + \omega_o)\right)\right]$$

and $$\varpi \equiv \frac{2\pi}{\tau}$$

In order to illustrate the abovementioned results, *Figure 4.5* shows the spectrum of such a signal produced in the FML mode for the special case of $\psi = 180°$, $\tau.f_0 = 1.5$ and $\tau_2.f_0 = 13.5$

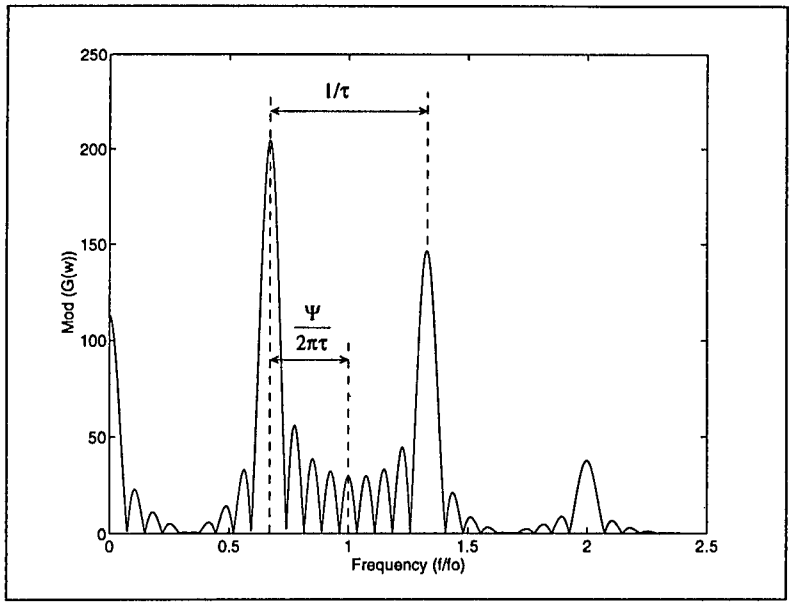

Figure 4.5. Output spectrum for FML mode

It can be seen that the frequency error is directly proportional to the phase error, Ψ, and indirectly proportional to the original recorded pulsewidth, τ. The frequency error can therefore be minimised by recording a longer sample of the original input signal and by minimising the head-to-tail phase error when repeating the pulse.

In order to reduce the frequency error in the FML mode, phase matching can be done. This means that the starting phase of the repeated pulse is matched to the tail-end phase of the previous one. Since the data is stored digitally, this phase matching can be done digitally. In such cases it is important to know how accurate the matching has to be if it is required that the frequency deviation not exceed a given limit. With reference to *Equation 4.8* and *Figure 4.5* the maximum frequency deviation, Δf, from the original input frequency f_0 is equal to:

$$\Delta f = \frac{\Psi}{2\pi} \cdot \frac{1}{\tau}$$

$$\therefore \Psi = 2\pi\tau \cdot \Delta f \quad \text{.....(4.9)}$$

Using *Equation 4.9*, the required phase accuracy (Ψ) can be calculated.

Chapter 5

Instantaneous bandwidth

The frequency response and instantaneous bandwidth of the different BDR architectures are described in this Chapter. Interlaced sampling is often used to increase the bandwidth of such systems. This technique of bandwidth extension, as well as the waveform and spectral distortions introduced by it, is also discussed in this chapter.

5.1 INSTANTANEOUS BANDWIDTH AND FREQUENCY RESPONSE

As explained in *Chapter 2*, the **theoretical** instantaneous bandwidth of the systems is equal to the Nyquist bandwidth and therefore directly proportional to the sampling frequency of the A/D and D/A converters, as indicated by the following equations:

$$BW_{AE,PE} = \frac{f_{sample}}{2} \quad \text{.....(5.1)}$$

$$BW_{EBAE,EBPE} = f_{sample} \quad \text{.....(5.2)}$$

The **'useable'** instantaneous bandwidth, on the other hand, depends on the application of the system. It might be influenced by one or more of the following factors:

- Spurious signal level
- Phase jitter
- Frequency response

High image/sideband levels (*Figure 3.12*) as well as phase jitter induced by these images (*Figure 4.2*), exist in the upper and lower edges of the information band. In *Chapter 7* it will be shown that digital frequency translation techniques can also induce high image levels at the information band edges. Due to these problems, the edges of the band are usually avoided, therefore reducing the available bandwidth. The third criteria defining this 'useable' bandwidth, namely frequency response, is discussed in this chapter.

Factors obviously having an effect on the frequency response are the type and order of the filters as well as the sample-and-hold operation of the D/A. Once again the typical order butterworth filters described in *Section 3.4* were used to illustrate the principle. The theoretical transfer function of the combination of the two lowpass and one bandpass filters of the AE and PE configurations is illustrated in *Figure 5.1* (trace A). The omission of the bandpass filter results in the filter transfer function of the EBAE and EBPE configurations (trace B).

The transfer function of a sample-and-hold circuit is given by Hayken [18, *pp159, equation 4.64*] as:

$$H(f) = T_s \frac{\sin(\pi T_s f)}{(\pi T_s f)} e^{-j\pi f T_s} \quad \text{.....(5.3)}$$

where T_s is the sampling period of the D/A converter. The effect of such a circuit in the system is therefore to multiply the frequency transfer function by a *sin(x)/x* function, thus attenuating the higher frequencies, as illustrated in *Figure 5.1* (Traces C and D). Two solutions exist to reduce the extent of this attenuation:

- The hold-times (i.e. sampling period) of the sample-and-hold circuit can be reduced, thus widening the *sin(x)/x* function and reducing the effect.

- An equaliser who's amplitude response equals $\frac{1}{|H(f)|}$ can be added to the system in order to eliminate the problem.

Both of these operations and their associated problems are described by Haykin [18, *pp156, section4.5*].

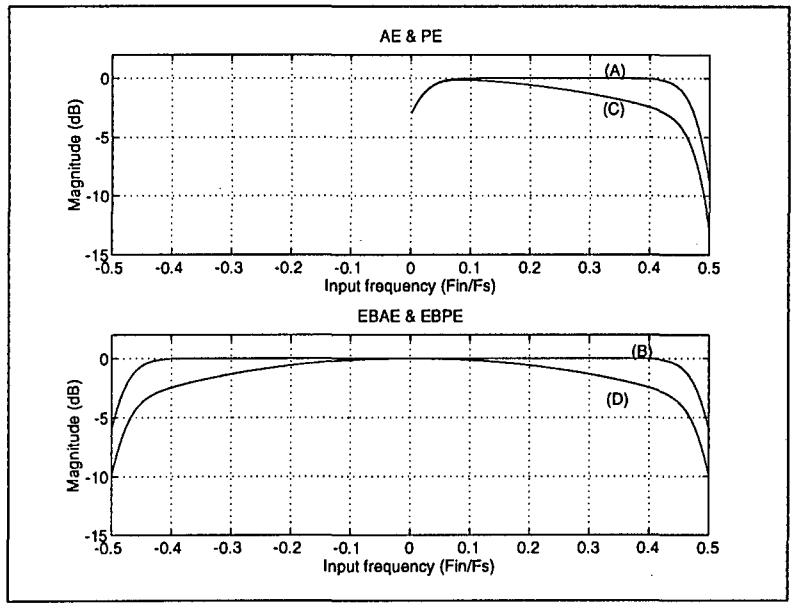

Figure 5.1. Frequency response for different architectures

Simulations were done in order to investigate the effect of other system parameters (for example quantisation) on the frequency response of the system. These simulation results were virtually identical to the theoretical prediction for the combined effect of filtering and sample-and-hold (traces C and D), thus showing that the rest of the system (including coarse quantisation) has no significant influence on the frequency response. Simulations that were done for all four configurations as well as for different numbers of bits quantisation yielded similar results.

It can therefore be concluded that the filter response and *sin(x)/x* spectral deformation are the only factors influencing the frequency response of BDR modules such as those described in this thesis.

5.2 BANDWIDTH EXTENSION BY INTERLACED SAMPLING

As mentioned earlier, the instantaneous bandwidth of wideband systems is usually limited by the state-of-the-art technology in terms of the sampling speed of the A/D conversion as well as digital processing speed. One way to overcome this problem is by using interlaced sampling to reduce the sampling- and data speeds. The incoming signal is divided into a number of channels(N). Each channel has a separate A/D. The different A/D's are clocked in turn by a time-delayed version of a low duty-cycle clock, as illustrated in *Figure 5.2*. The time delays induced in the different channels are multiples of T_s/N where T_s is the clock period. Each A/D therefore reads only one sample every T_s seconds. The system as a whole, however, reads a sample every T_s/N seconds, thus increasing the Nyquist bandwidth from $1/2T_s$ to $N/2T_s$. The data processing is done in parallel, therefore decreasing the data speeds to $1/N$ times the normal rate. The system is illustrated in *Figure 5.2*

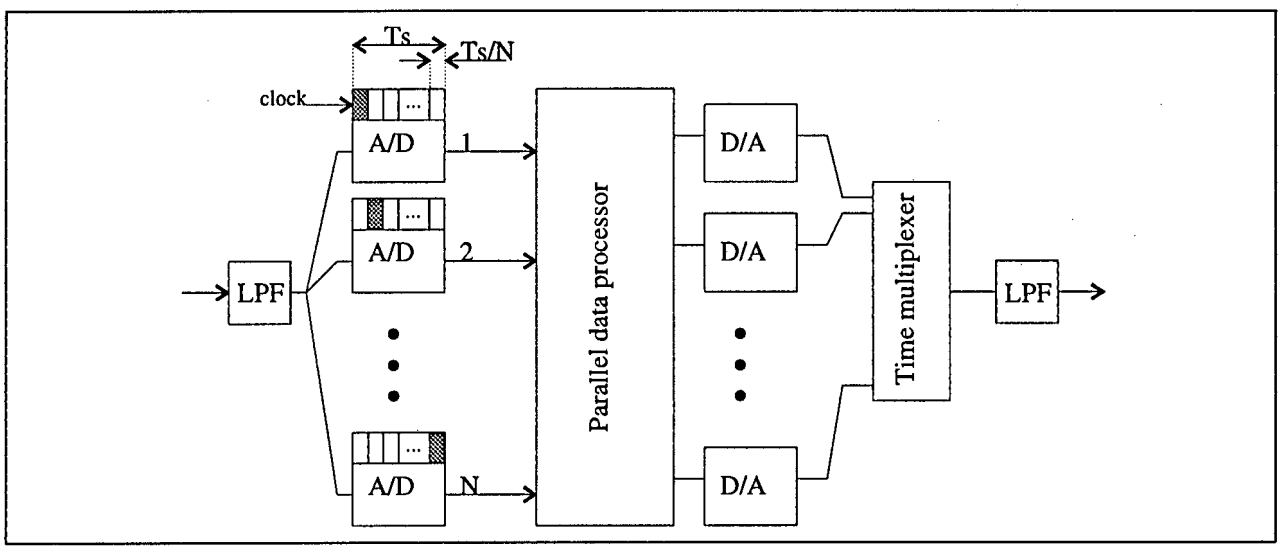

Figure 5.2. Descriptive block diagram for Interlaced sampling

The biggest problem in such a system is the timing accuracy required for the sampling process. It is usually difficult to obtain a very accurate delay between the sampling times of the different channels. An objective of this section was therefore to investigate the effect of such a timing error on the waveform fidelity of the system.

As Bracewell [19, *pp201*] shows, interlaced samples are not required to be equidistant in order to regain the original signal exactly. The sampling channels therefore do not have to be perfectly timed. This argument holds only if the original timing relation between the interlaced samples is retained when the samples are read from the RAM during the reconstruction of the signal. Another condition is that the filtering be adapted to the sampling timing error, i.e. a unique filter is required for a specific timing error. As not one of these conditions can be met in a practical implementation, it was decided to investigate the effect of imperfectly timed channels.

5.2.1 2-Channel Interlaced sampling

In order to gain insight into the effect of interlaced sampling in a typical practical implementation, a mathematical analysis was done for the following special case (illustrated in *Figure 5.3*):

- Two-channel system (N=2).
- Sinusoidal input signal.
- A relative sampling timing error τ_1 is made in the interlaced sampling process.
- The original timing relation between the interlaced samples is **not** retained during the reconstruction of the signal (i.e. a further timing error of τ_2 is induced in the readout process).
- A normal ideal lowpass filter is used (instead of 'interlaced sampling filters', as described by Bracewell [19, *pp201*])

The 2-channel system was chosen since it simplifies the calculations, yet most of the results are directly applicable to higher order systems. In most cases these results therefore represent the best-case situation (i.e. a system using more channels would show poorer results).

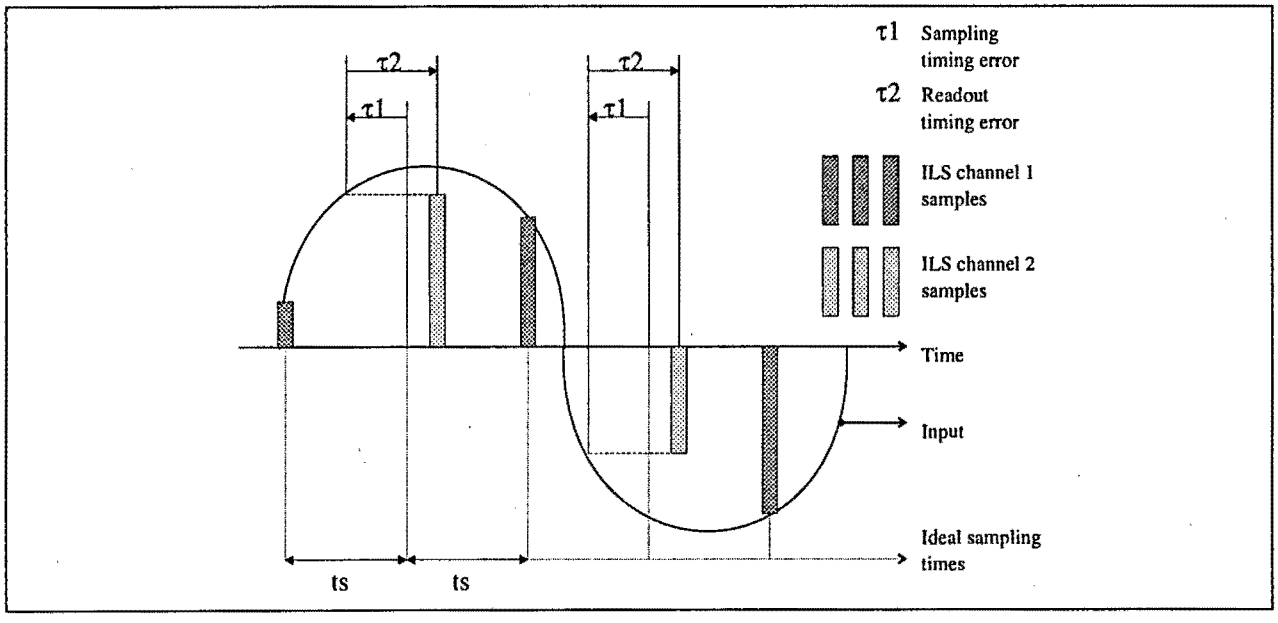

Figure 5.3. Sinusoidal signal being sampled by a 2-channel ILS system

The derivation of the expression for the Fourier transform ($G_2(f)$) of the output signal of such a system, given an input signal $p(t)$, is given in *Appendix A2* . The results are given below and are illustrated in *Figure 5.4*:

$$p(t) = \cos(2\pi f_1 t) \quad \text{.....(5.4)}$$

$$G_2(f) = H(f) \cdot \frac{\pi}{t_s} \cdot \delta_{\frac{1}{2t_s}}(f \pm f_1) \cdot \left[1 + e^{-j2\pi[(f \mp f_1)(t_s - \tau_1) + f\tau_2]}\right] \quad \text{.....(5.5)}$$

where $H(f)$ is the ideal Nyquist lowpass filter transfer function:

$$H(f)=\begin{cases}1 & |f|<\frac{f_s}{2} \\ 0 & otherwise\end{cases} \quad \text{.....(5.6)}$$

where $\delta_{f_0}(f)=\sum_{n=-\infty}^{\infty}\delta(f-nf_0)$

and where f_s is the sampling rate of the interlaced signal and $t_s=\frac{1}{f_s}$, as indicated in *Figure 5.4*, i.e. $T_s=Nt_s$ if T_s is the sampling period of each individual A/D converter.

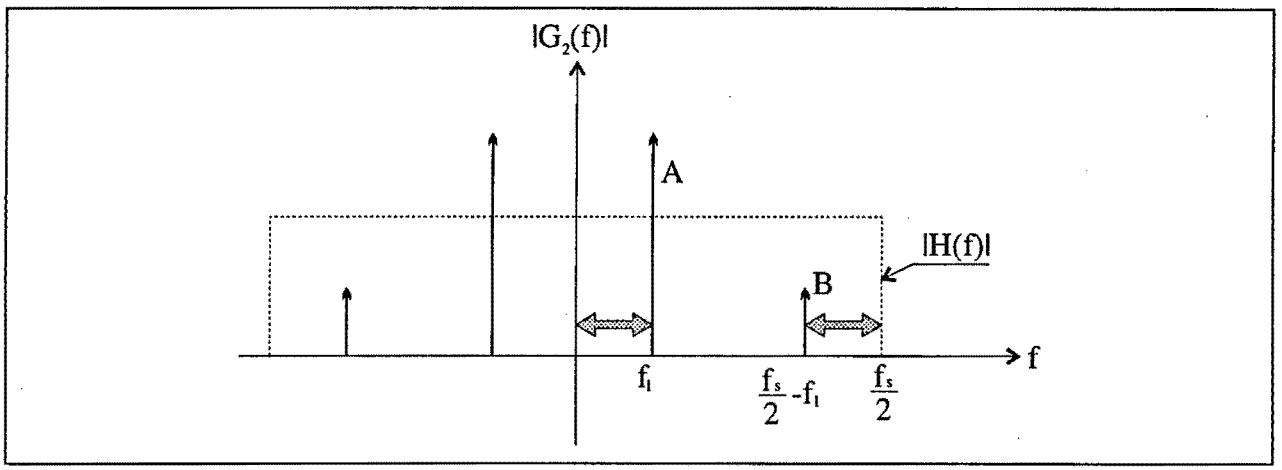

Figure 5.4. Frequency spectrum of sinusoid with interlaced sampling

It can be seen from *Figure 5.4* that an additional unwanted spur (B) appears in the information band (at $f=\frac{f_s}{2}-f_1$) due to timing errors in the interlaced sampling process. The magnitude and phase of the spur are respectively:

$$|B|=\frac{2\pi}{t_s}\left|\cos(\phi_B)\right| \quad \text{.....(5.7)}$$

$$\phi_B=\frac{\pi}{2}\left[1-\tau_1 f_s+\tau_2(f_s-2f_1)\right] \quad \text{.....(5.8)}$$

The magnitude and phase of the desired output component (A) are respectively:

$$|A|=\frac{2\pi}{t_s}\left|\cos(\phi_A)\right| \quad \text{.....(5.9)}$$

$$\phi_A=-\pi\tau_2 f_1 \quad \text{.....(5.10)}$$

Imperfectly timed interlaced sampling therefore has two major effects on the output spectrum:

- Generation of an 'image' at a frequency of $f = \frac{f_s}{2} - f_1$
- Attenuation of the main signal at input frequency f_1.

The magnitude of the spurious and the extent of the attenuation of the main signal are both functions of the input frequency, f_1. This input frequency dependence is illustrated in *Figure 5.5* for different ILS timing errors, τ.

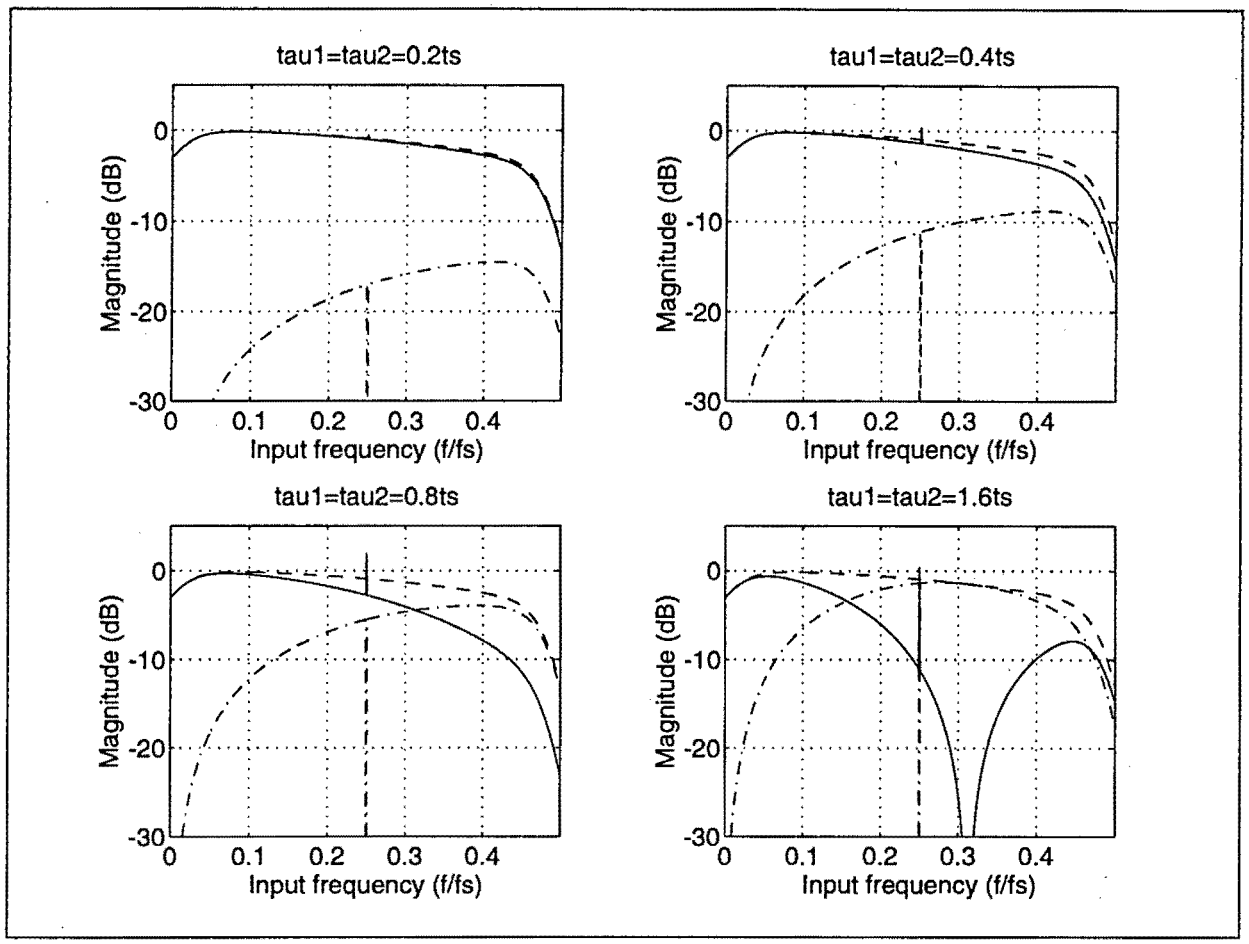

Figure 5.5. *Frequency response and image magnitude for different ILS timing errors*

Trace A (- - -) represents the ideal case (i.e. the filter response together with the *sin(x)/x* deformation caused by the sample-and-hold operation of the time multiplexer). *Trace B* (——) depicts the frequency response of a system using interlaced sampling and having timing errors τ_1 and τ_2, as was shown in *Figure 5.3*. It can be seen that the attenuation introduced by the timing errors increases for an increase in input frequency. *Trace C* (— · — · —) shows the magnitude of the 'image' created by the timing errors versus the frequency of the input signal. It attains its maximum value as the input frequency reaches the upper end of the information band. Its magnitude can even exceed that of the main signal for large timing errors.

At the centre of the information band ($0.25 f_s$), the input signal and the 'image' overlap, creating either a peak or a gap in the frequency response, depending on the relative phases of the input signal and the created 'image'.

It can be seen from *Figure 5.5* that a large 'hole' is created in the frequency response for timing errors larger than t_s. At a certain input frequency the desired output signal vanishes and all the energy is concentrated in the image. This might seem to be an extreme case of timing error. In systems using a large number of channels, though, the occurrence of such a situation becomes more likely.

5.2.1.1 Relative signal/image magnitudes

In order to get a better overview of the timing accuracy needed for a given required image suppression, the relative signal/image magnitudes were calculated for different ILS timing errors, τ_1 and τ_2. This can easily be done by using *Equations 5.7* and *5.9*:

$$\frac{|A|}{|B|} = \frac{\cos(-\pi\tau_2 f_1)}{\cos\left(\frac{\pi}{2}(1-\tau_1 f_s + \tau_2(f_s - 2f_1))\right)} \quad \text{.....(5.11)}$$

Figure 5.6 illustrates this timing error/relative magnitude relationship for the following special cases:

1. Worst-case signal/image relationship, i.e. $f_1=f_s/2$ and with $\tau_1=\tau_2=\tau$. This graph thus represents the worst case image levels if the total available information band is used in the final application. For this special case *Equation 5.11* simplifies to:
$$\frac{|A|}{|B|} = \cot\left(\frac{\pi\tau f_s}{2}\right) \quad \text{.....(5.12)}$$
2. Worst-case signal/image relationship for 90% bandwidth utilisation, i.e. $f_1=0.45f_s$ and with $\tau_1=\tau_2=\tau$. This graph therefore represents the worst case image levels if only the lower 90% of the available information band is used in the final application. For this special case *Equation 5.11* simplifies to:
$$\frac{|A|}{|B|} = \cot\left(\frac{0.9\pi\tau f_s}{2}\right) \quad \text{.....(5.13)}$$

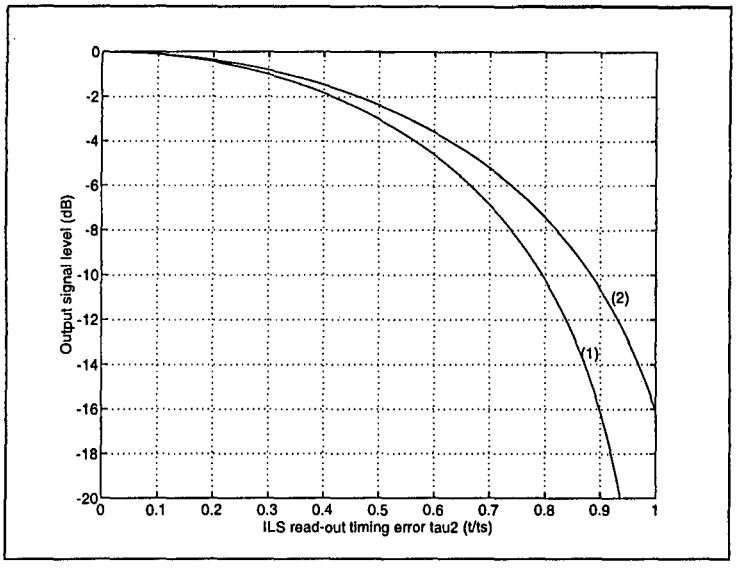

Figure 5.7. *Signal attenuation vs. ILS readout timing error*

It can be seen that signal attenuation caused by ILS timing errors poses no serious problem and that relatively large ILS timing errors are still acceptable (i.e. for a 2-channel system).

5.2.2 Extension to more channels

Looking at the derivation of the expression for the Fourier transform of the output signal of a 2-channel ILS system (*Equation 5.5*), given in *Appendix A2*, it can be seen that this special case can be extended to an ILS system using N channels. The expression $(G_N(f))$ for the output frequency spectrum of such an N-channel system for a sinusoidal input can therefore be derived as:

$$G_N(f) = H(f)\cdot\frac{2\pi}{Nt_s}\cdot\delta_{\frac{f_s}{N}}(f \pm f_o)\cdot\left[1+\sum_{n=2}^{N} e^{j\phi_n}\right] \quad \text{.....(5.16)}$$

where: $\phi_n = -2\pi\left[(t_s - \tau_{1|n})(f \mp f_o) + f\tau_{2|n}\right]$

and where $\tau_{1|n}$ is the read-in timing error of channel n and $\tau_{2|n}$ is the read-out timing error of channel n, as shown in *Figure 5.3* for the 2-channel case.

It can therefore be seen that N 'images' or spurious appear in the information band for an N-channel ILS system, their magnitudes depending on the channel timing errors as well as the input frequency. As N increases, the attenuation of the desired signal becomes larger as more power is distributed into the spurious signals. This is illustrated in *Figure 5.8* by plotting the frequency response of both a 2-channel and a 4-channel system, both having approximately the same timing errors (in this case $\pm 0.5t_s$). It can be seen from the figure that the attenuation at the end of the information band increases rapidly with an increase in the number of channels used, thereby making the timing accuracy requirements more

stringent for larger N. The number of peaks/gaps in the frequency response, created by the overlapping of the desired signal with the 'images', increases as the number of channels increase.

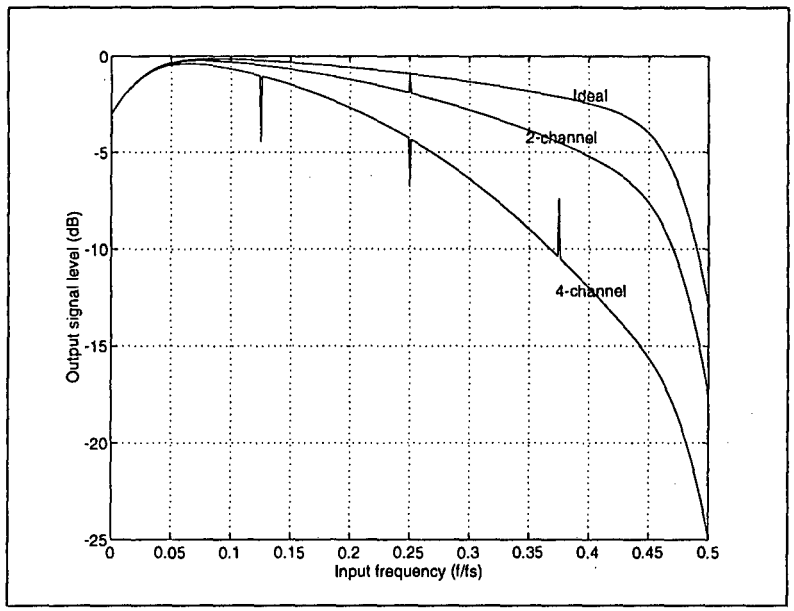

Figure 5.8. *Frequency response of 2-channel and 4-channel ILS systems*

It can finally be concluded that interlaced sampling requires very accurate timing if low spurious levels (i.e. good 'image' suppression) or low attenuation of the main signal is required. The timing accuracy requirements increase with an increase in the number of channels used.

Chapter 6

Effect on matched filter receiver

In most digital communication and other detection systems, we are interested in maximising the peak pulse signal in the presence of additive white noise. In 1943, North devised the *matched filter* for this optimum detection of a known signal. The matched filter is used extensively in the receivers of communication and detection systems. It was therefore considered important to investigate the effect of a BDR on the matched filter receiver in order to see how "transparent" the BDR is to such a system.

A number of different signals were chosen in order to test the ability of the BDR to accurately replicate phase and amplitude information. The BDR systems were simulated with the coded signal as input. The output signal of the BDR was then used as input to the matched filter. Finally, the output of the matched filter was used to compare the different BDR architectures with different internal wordlengths. *Figure 6.1* illustrates the simulation procedure.

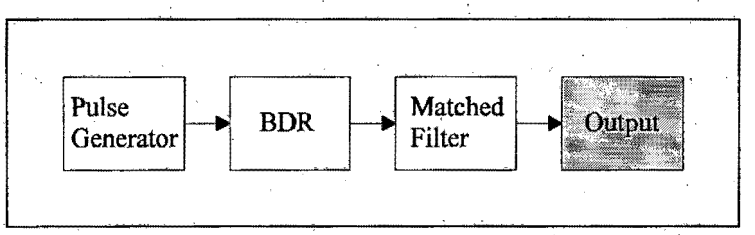

Figure 6.1 Simulation procedure

The ability of the matched filter to distinguish a given signal in additive white noise depends on the relative main-lobe-to-sidelobe magnitudes of the matched filter output. The main criterion used to judge the transparency of a given BDR architecture was therefore the magnitude of the time sidelobes of the matched filter output. The signals used in the simulations were therefore also coded in such a way as to minimise the time sidelobes.

6.1 DESCRIPTION OF MATCHED FILTER CODES

6.1.1 Linear FM chirp with Hamming amplitude weighting

The linear FM chirp (quadratic phase modulation) is "by far the most widely implemented technique for pulse compression" [20, *pp498, section 13.2*] in RADAR applications (The term 'pulse compressor' is in essence the same as 'matched filter receiver'). The first time sidelobe resulting from a uniformly weighted linear FM chirp can be shown to be ≈13.5dB below the main lobe peak [20, *pp521, section 13.9*]. By amplitude weighting the FM chirp, the sidelobes may be reduced. While substantially reducing the sidelobes, the main-lobe peak is reduced in amplitude and also broadened. Hamming amplitude weighting was used in this case, resulting in sidelobes ≈59dB below the main lobe peak and a broadening of the main lobe by a factor of 2. The time-bandwidth product (i.e. expanded pulselength × bandwidth) of the pulse was chosen as 200, thus resulting in a pulse compression ratio of 1:200. *Figure 6.2* illustrates a time plot of the chirp together with plots of its frequency spectrum, frequency vs. time relation and ideal pulse compressor output.

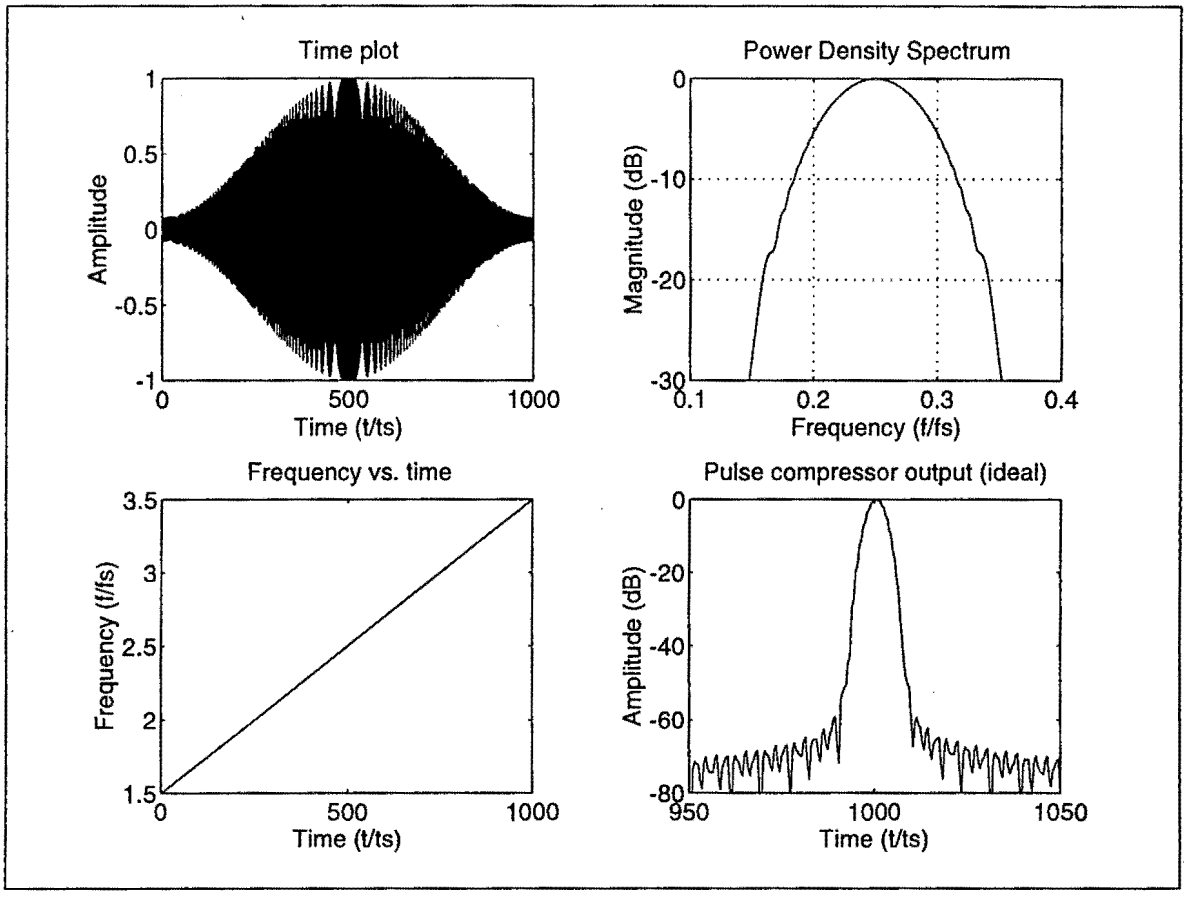

Figure 6.2 Description of linear FM, Hamming amplitude weighted chirp

6.1.2 Constant amplitude Non-linear FM pulse with Hamming frequency weighting

By increasing the FM rate near the ends of the transmitted pulse and decreasing it near the centre, the transmitted spectrum of the chirp may be tapered. This spectral weighting therefore replaces the amplitude weighting as described in *Section 6.1.1*, thereby producing a constant amplitude pulse with a matched filter response which has low sidelobes. Constant amplitude chirp signals are usually easier to generate than signals requiring accurate amplitude weighting.

If the FM slope is made to vary inversely with the square root of the weighting function, the energy spectrum will be weighted by the same function [21, *pp226, section 5.2*]. The Hamming function was once again chosen to shape the spectrum, producing sidelobes ≈43dB below the main-lobe peak. A chirp time-bandwidth product of 200 was also chosen. *Figure 6.3* illustrates a time plot of the chirp, as well as plots of its frequency spectrum, frequency vs. time relation, and ideal pulse compressor output.

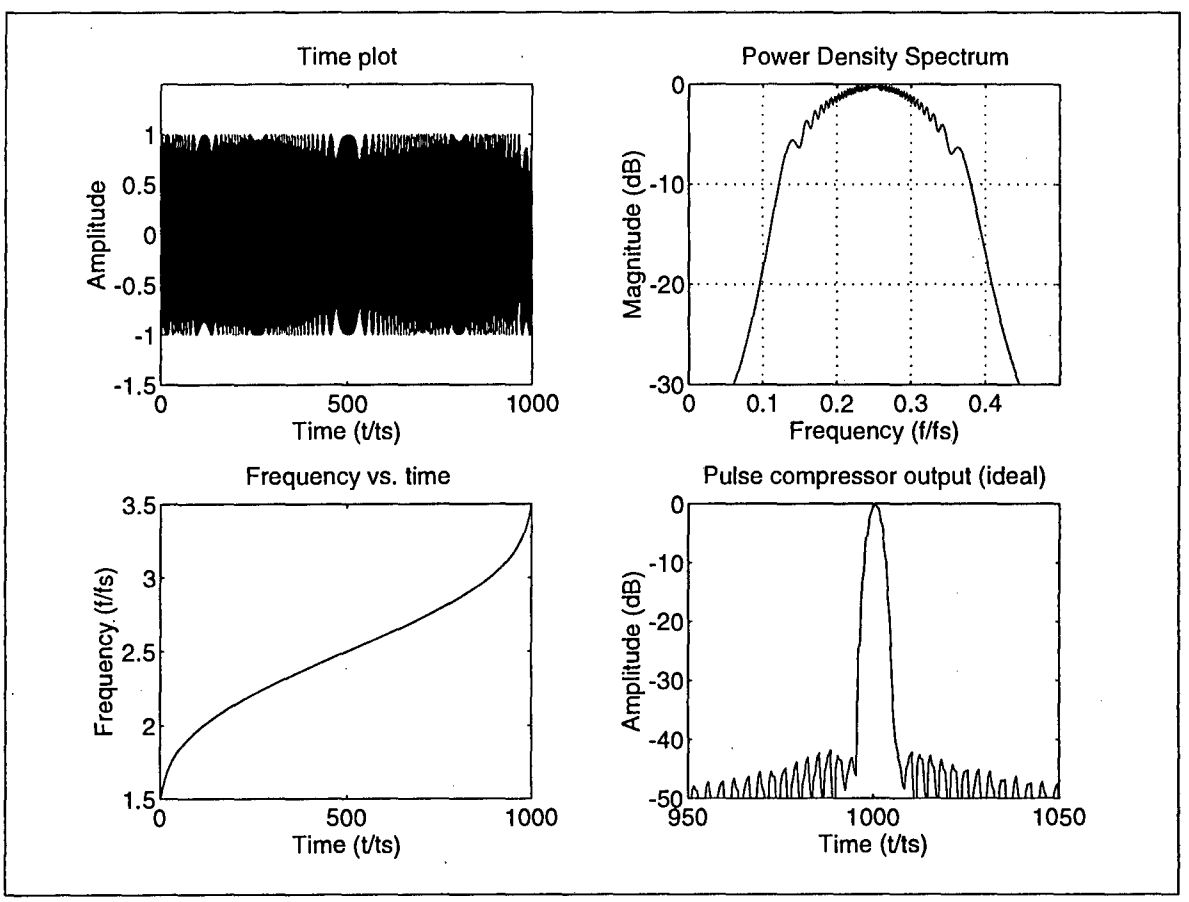

Figure 6.3 Description of non-linear FM, Hamming spectral weighted chirp

6.1.3 13-chip PSK Barker code

The longest known Barker code of length 13 was chosen to test the ability of the BDR system to replicate a binary coded Phase Shift Keying (PSK) pulse, a waveform very commonly used in digital communication systems. The Barker code was chosen since it exhibits good aperiodic autocorrelation,

and therefore a matched filter response with low time sidelobes. The 13-chip Barker code has an aperiodic autocorrelation with sidelobes no greater than 1/13 times that of the main lobe (i.e. sidelobe suppression of ≈22.3dB). *Figure 6.4* illustrates the signal properties of the pulse.

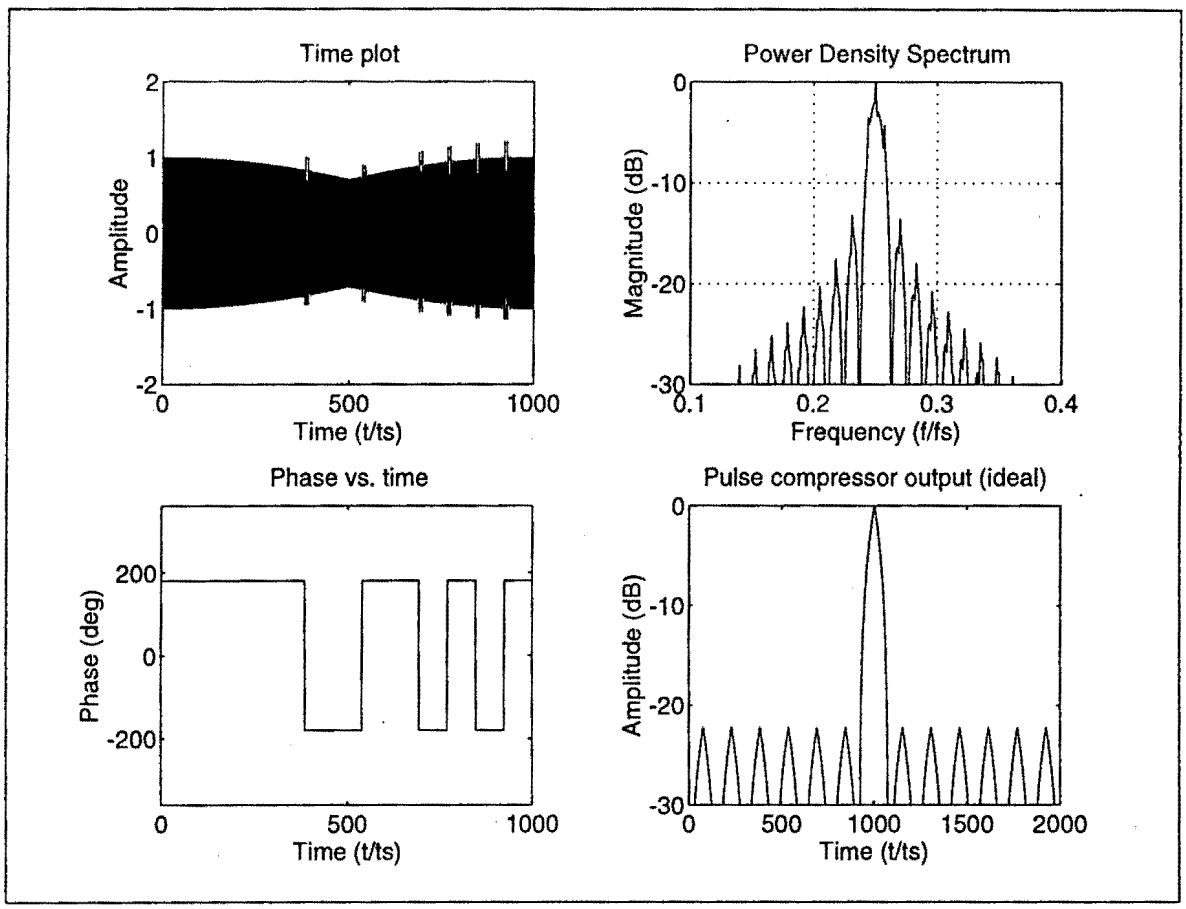

Figure 6.4 Description of 13-chip Barker coded PSK pulse

6.2 SIMULATION RESULTS

For all three input signals, the matched filter output was calculated for different BDR architectures and with different internal wordlengths. In each case the maximum time sidelobes were determined and plotted against the number of bits quantisation used. The matched filter outputs for the 4-bit architectures are also presented in the results to illustrate the effect of typical architectures on the matched filter output.

6.2.1 Linear FM chirp with Hamming amplitude weighting

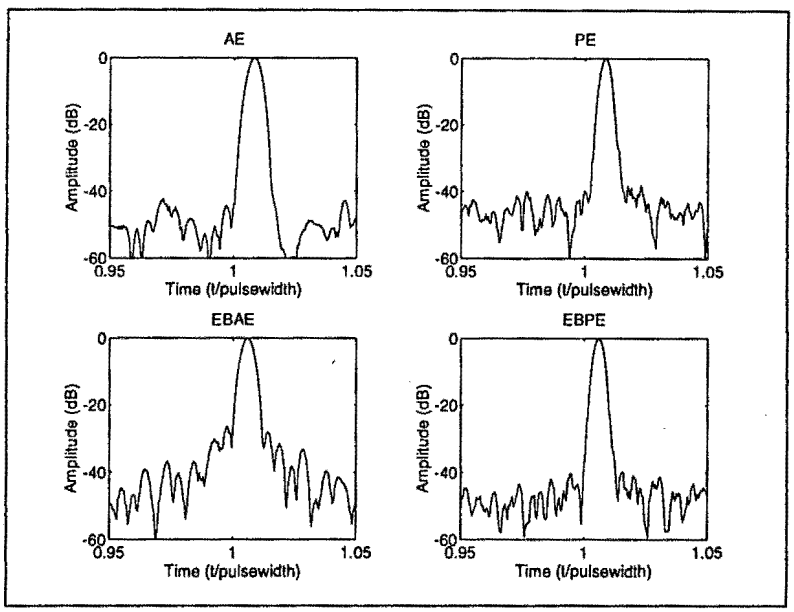

Figure 6.5 Matched filter output - 4-bit quantisation

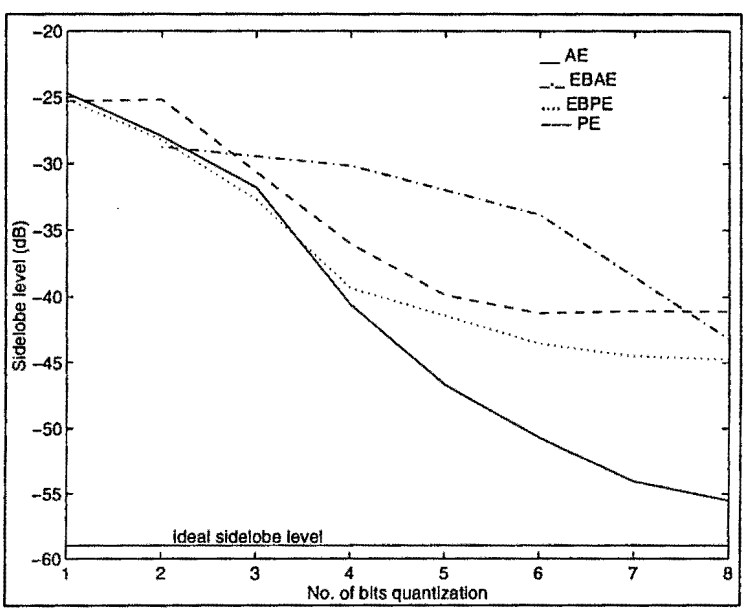

Figure 6.6 Matched filter output sidelobe levels for different BDR architectures

It can be seen that the AE architecture shows superior transparency, especially for fine quantisation, its performance flattening off at about 7-bit quantisation. The phase encoded architectures produce somewhat poorer results, exhibiting no major improvement for internal wordlengths longer than about 5 bits. The inferior performance of the phase encoding architectures is intuitively correct, since the amplitude weighting function is disregarded in the digitisation process used in the capturing of the signal. The performance of the EBAE architecture is comparable to that of an AE architecture using only half of its A/D quantisation bits (i.e. a 6-bit EBAE architecture produces similar results to a 3-bit AE architecture). The EBAE architecture therefore needs twice the amount of internal memory to store a signal of the same length and with similar signal fidelity.

6.2.2 Constant amplitude Non-linear FM pulse with spectral Hamming weighting

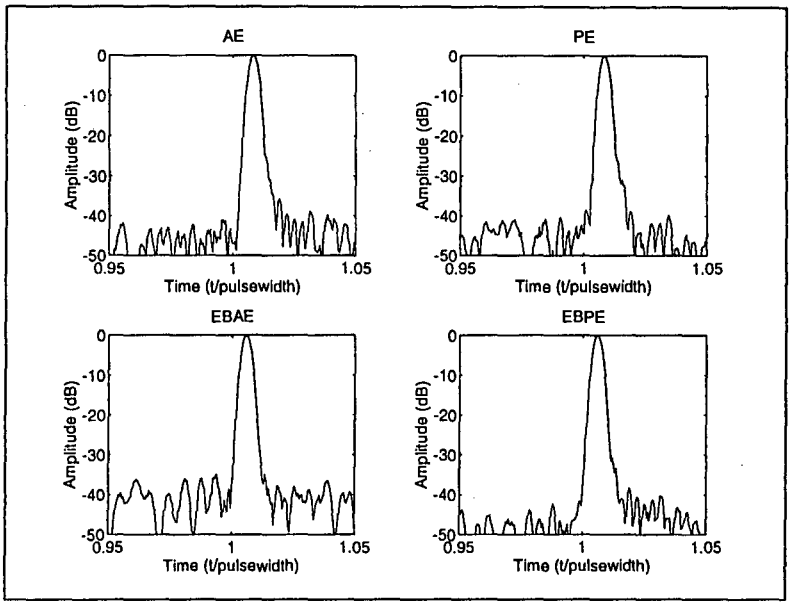

Figure 6.7 Matched filter output - 4-bit quantisation

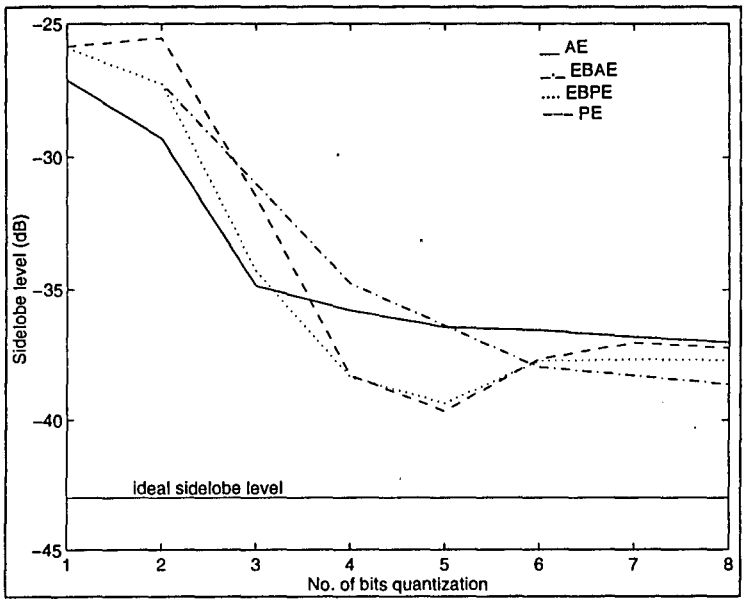

Figure 6.8 Matched filter output sidelobe levels for different BDR architectures

For the constant amplitude chirp, the ability of the AE and EBAE architectures to store amplitude information is disregarded. This chirp is therefore a good means of comparing the accuracy with which the architectures can replicate *phase and frequency information.* From the results it can be seen that the phase encoding architectures show a slightly better transparency than the AE architecture, especially for finer quantisation. The EBAE again needs long internal wordlengths for good transparency. The performance of the AE, PE and EBPE architectures shows no major improvement for quantisation finer than 5 bits.

6.2.3 13-chip PSK Barker code

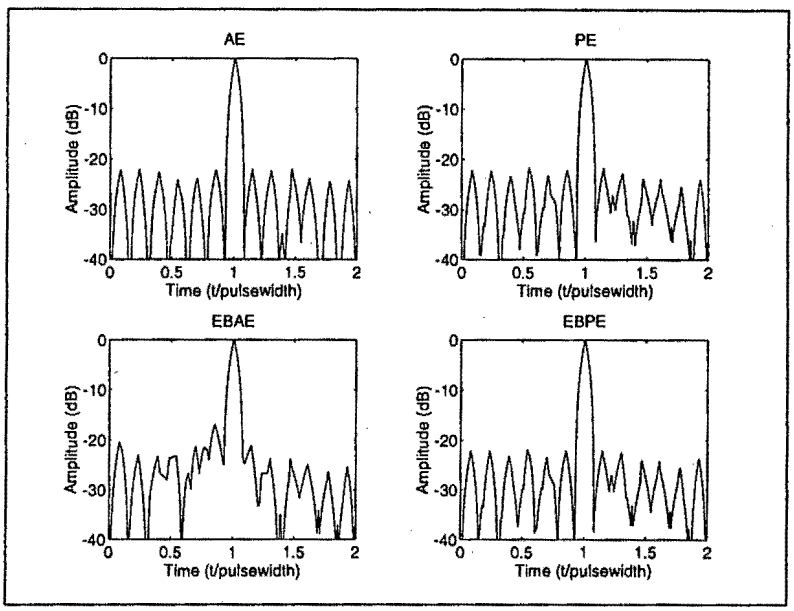

Figure 6.9 Matched filter output - 4-bit quantisation

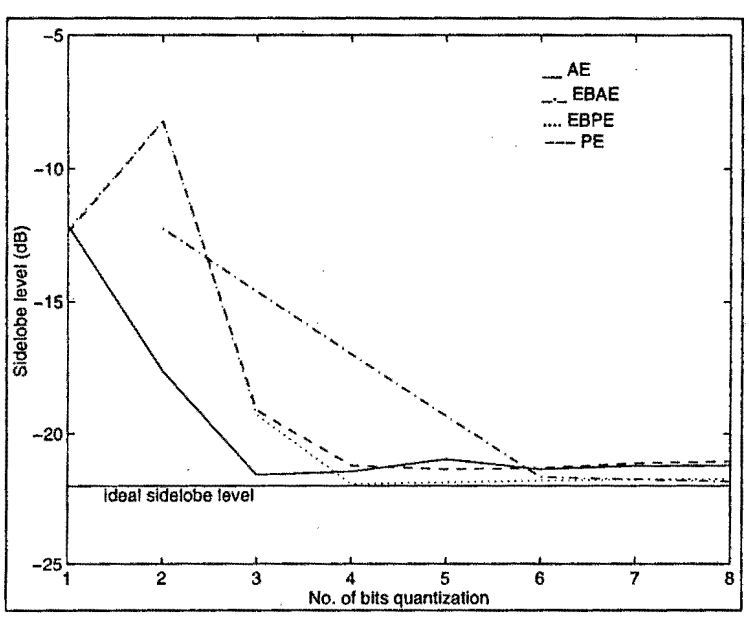

Figure 6.10 Matched filter output sidelobe levels for different BDR architectures

The AE architecture reaches its peak performance with 3-bit quantisation, the PE and EBPE architectures with 4 bits, and the EBAE with 6 bits. Once again the performance of the EBAE architecture is nearly the same as that of an AE architecture using half its internal wordlength. Looking at *Figure 6.10*, a surprising result is that 2-bit quantisation produces higher sidelobes than 1-bit quantisation for the phase encoding architectures. It was found that the magnitude of the sidelobes is dependent on the location of the carrier frequency of the PSK pulse in the information band of the BDR.

In order to investigate this effect, the carrier frequency of the PSK pulse was varied over the entire information band of the BDR, and the corresponding sidelobe levels were measured in each case. This simulation was done for all four architectures for the 1-bit, 2-bit and 4-bit quantisation cases. The results for the 2-bit simulations are illustrated in *Figure 6.11* The results for the other two cases are included in *Appendix B7.* It can be seen from *Figure 6.11* that the sidelobe levels show large variations as the carrier frequency is changed. By comparing the 1-bit and 2-bit cases, it can also be seen that 2-bit quantisation produces generally better results than 1-bit quantisation, therefore giving a more satisfactory result than the one depicted in *Figure 6.10*

It was found that the magnitude of the sidelobe levels for the two frequency chirp signals described in *Section 6.1.1* and *6.1.2* show hardly any variation with a change in centre frequency. The simulations were therefore not repeated for these two cases.

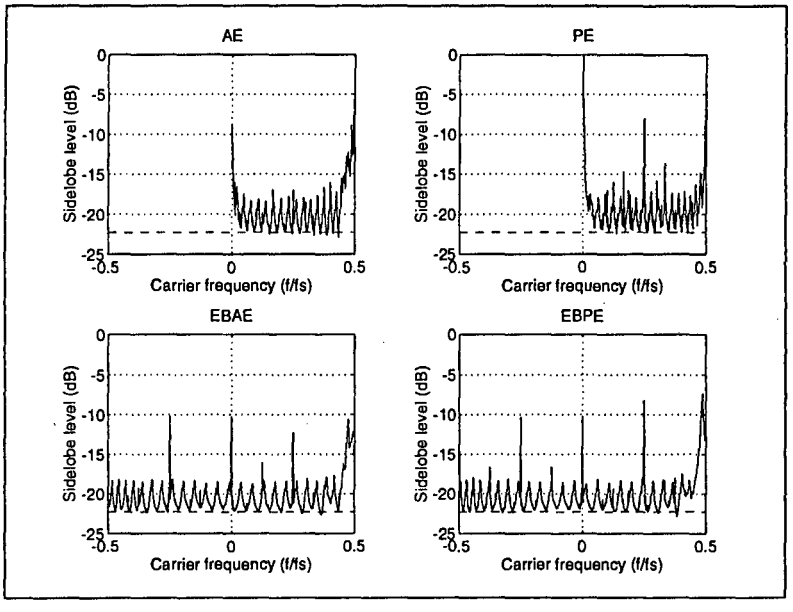

Figure 6.11 Sidelobe level vs. carrier frequency for 2-bit BDR architectures

6.3 COMPLETE RECEIVER/TRANSMITTER SIMULATION

A common application of matched filter receivers is found in the detection system of a RADAR. MATLAB subroutines were obtained which simulate complete RADAR transmit and receive systems. The subroutines simulate all subsystems of a typical modern RADAR, and include optimisation techniques which minimise the sidelobe levels of the pulse compressor output. It was decided that this simulation software would be a meaningful way of comparing BDR architectures in the light of transmitter/receiver transparency.

The comparison was done, as described in the previous sections, by comparing the sidelobe levels of the pulse compressor (in this case receiver) output. The time plot, the PDS and the ideal pulse compressor output of the chirp pulse are illustrated in *Figure 6.12.* The pulse is also a constant amplitude, non-

linear FM chirp, but with a much smaller time-bandwidth product than the one discussed in *Section 6.1.2*. It can be seen that the ideal pulse compressor output has very low sidelobes (± 62dB below the main lobe) due to the sidelobe level optimisation.

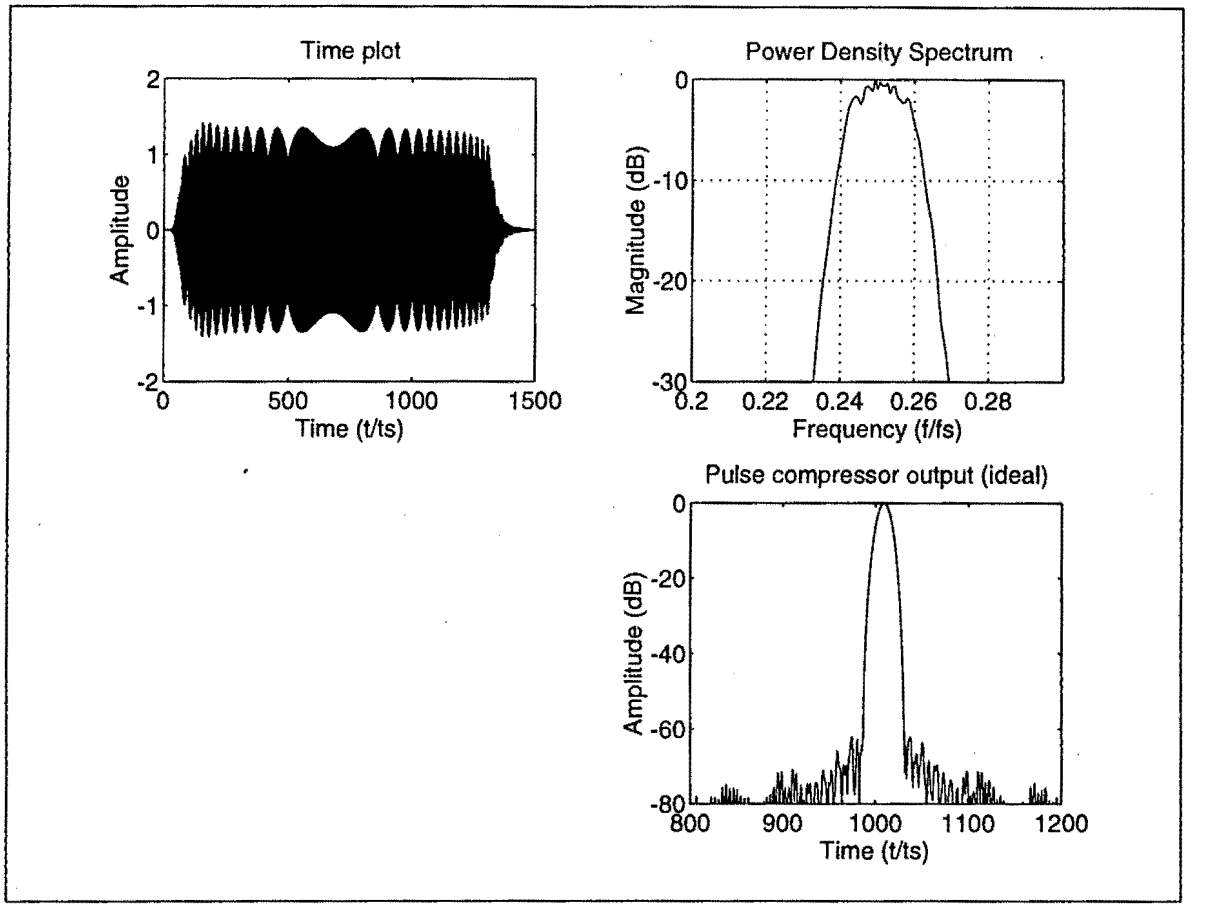

Figure 6.12 Description of non-linear FM chirp used in transmitter-receiver simulation.

Figure 6.13 illustrates the effect on sidelobe levels by inserting the different BDR architectures in the transmitter/receiver path. It shows drastic differences between the AE, EBAE and the phase encoding techniques. The amplitude encoding seems far superior to the phase encoding. This difference in performance is much more profound than that obtained in the normal matched filter simulations, as described in *Section 6.2*. The difference in performance can be attributed to receiver subsystems other than the matched filter itself. However, the understanding of such receiver subsystems was considered beyond the scope of this thesis. It is believed that different performances can be expected from different receiver configurations (in this case a modern RADAR). A more thorough investigation into the BDR/receiver interaction might therefore be necessary in order to quantify the effect of a BDR on a specific receiver system.

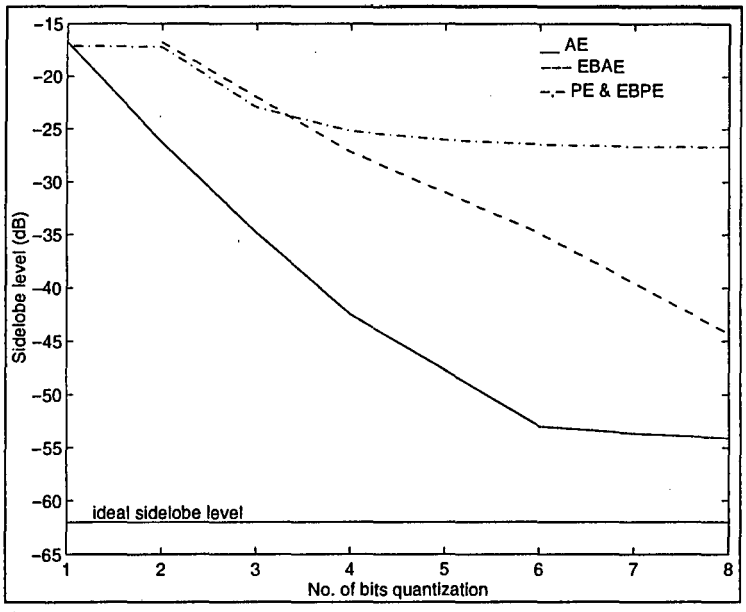

Figure 6.13 Receiver output sidelobe levels for different BDR architectures

Chapter 7

Digital frequency translation techniques

In many applications a need exists to induce a frequency translation (also commonly referred to as 'Doppler shift') in the captured signal. A reason for this might be to compensate for a Doppler shift induced by relative transmitter/receiver movement. This is a common problem in aircraft and satellite communication systems. Another reason might be the deliberate induction of a Doppler shift in order to deceive enemy detection systems. This technique is used, for example, in ECM systems to deceive enemy RADAR.

Since the input signal of the BDR is stored digitally, the Doppler shift can be induced by using digital signal processing techniques. The digital modulation techniques clearly have advantages over traditional analogue methods. The modulation frequency can be set very accurately, for example, by recalling pre-programmed frequency words from memory. The modulation frequency can also be changed very easily by simple software control. A further advantage of digital techniques is that digital multipliers and adders are used instead of analogue mixers and combiners. This simplifies the architecture and also avoids the practical imperfections inherent in such analogue devices.

Digital frequency translation techniques are suggested for each of the four proposed BDR encoding architectures. The functioning of each of these techniques is described in the following sections. The effect of each of these digital frequency translation techniques on the BDR output signal fidelity, is also briefly discussed.

7.1 DIGITAL SINGLE SIDEBAND MODULATOR (DSSM)

This modulation technique, described by Foltz [22], can be used to induce a Doppler shift in a single-channel, amplitude encoded signal. It would therefore be a good technique to implement a frequency translation in the AE architecture. A simplified block diagram of the DSSM is illustrated in *Figure 7.1* .

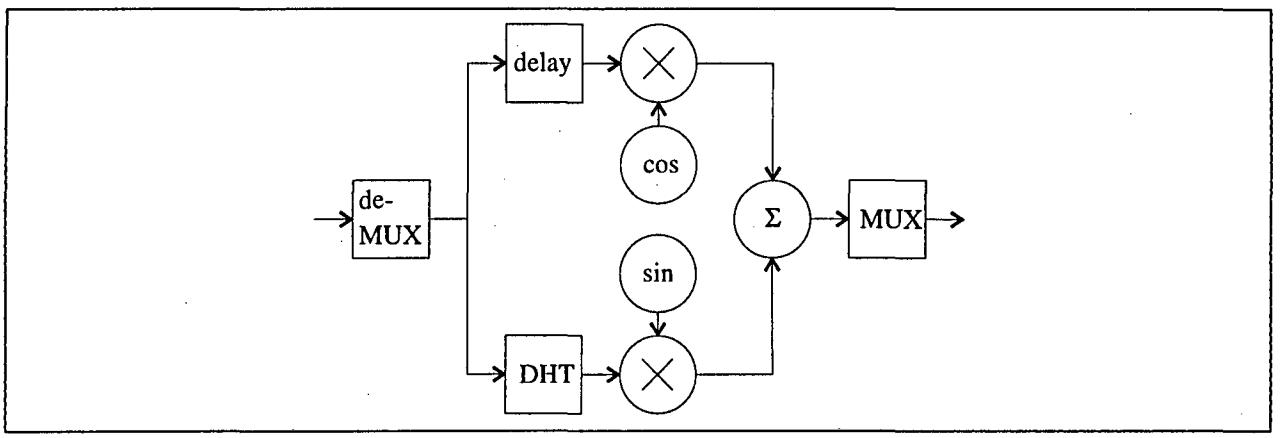

Figure 7.1 Block diagram of the Digital Single Sideband Modulator

The modulator has a demultiplexer and multiplexer to process the digitised signal in parallel, thereby reducing the digital processing speed requirements. It has a discrete Hilbert transformer (DHT) to shift the phase of the incoming signal by 90°, thereby producing the quadrature (Q) channel. A digital delay has to be induced in the in-phase (I) channel to compensate for the delay caused by the Hilbert transformer. Frequency synthesisers and digital multipliers modulate both the I and Q channels with the desired Doppler frequency. The two channels are then added by a digital summer to produce the modulated output.

Most of the subsystems of the DSSM can be considered ideal (except for the fact that a limited number of bits are used to represent the signal samples, frequency synthesiser samples, etc.). The same cannot, however, be said about the discrete Hilbert transformer (DHT). Simulation results showed that this subsystem has the biggest effect on the output signal quality. It is hence the most important consideration in the design of such a system. The DHT is therefore discussed in more detail in the following section.

7.1.1 The Discrete Hilbert Transformer

Oppenheim and Schafer [23, *pp679, equation 10.68*] give the impulse response of an ideal discrete Hilbert transformer as:

$$h(n)=\begin{cases}\dfrac{2\sin^2(\pi n/2)}{\pi n} & |n|>0 \\ 0 & n=0\end{cases} \qquad \text{.....(7.1)}$$

and n = {...,-2,-1,0,1,2,...}

It can be seen from *Equation 7.1* that the Hilbert transformer has an infinite impulse response and is non-causal. In order to be able to implement the DHT with an FIR filter, *h(n)* has to be truncated to some odd value *N* and shifted to the right *(N-1)/2* samples until the left most value is at the origin. This shift of the impulse response causes a delay of *(N-1)/2* times the sampling period in the Q-channel. The same delay must therefore be induced in the I-channel (see *Figure 7.1*) in order to maintain I/Q phase coherence. Furthermore, the filter coefficients, *h(n)* have to be quantised in order to be able to represent them digitally. There are thus two major differences between the ideal DHT and the practical implementation of an FIR filter DHT:

- Truncation of the impulse response in order to implement an FIR filter
- Quantisation of the filter coefficients

These two factors cause the DHT (and therefore also the Q-channel) to have a non-ideal frequency response. This is illustrated in *Figure 7.2*, plot(1) for the following special case:

- Impulse response length N = 15
- 6-bit filter coefficient quantisation
- Hamming impulse response windowing

The magnitude of the frequency response of the I-channel is constant throughout the band. The Q-channel magnitude response, however, changes due to the DHT, as can be seen from plot(1) in *Figure 7.2*. This causes an amplitude imbalance in the I/Q channels, therefore creating a sideband image component, as is explained in *Section 3.2.2*. The magnitude of this sideband can be calculated by using *Equation 3.6*. The sideband level vs. input frequency is illustrated in plot(2) of *Figure 7.2* for the special case described above. The sideband is a 'Doppler sideband' and is situated at a frequency $f=f_{in}-f_{Dopp}$.

Hamming windowing of the filter coefficients is used to reduce the ripples in the frequency response of the DHT [22], which are caused by the truncation of the impulse response. It therefore also reduces the Doppler sideband level.

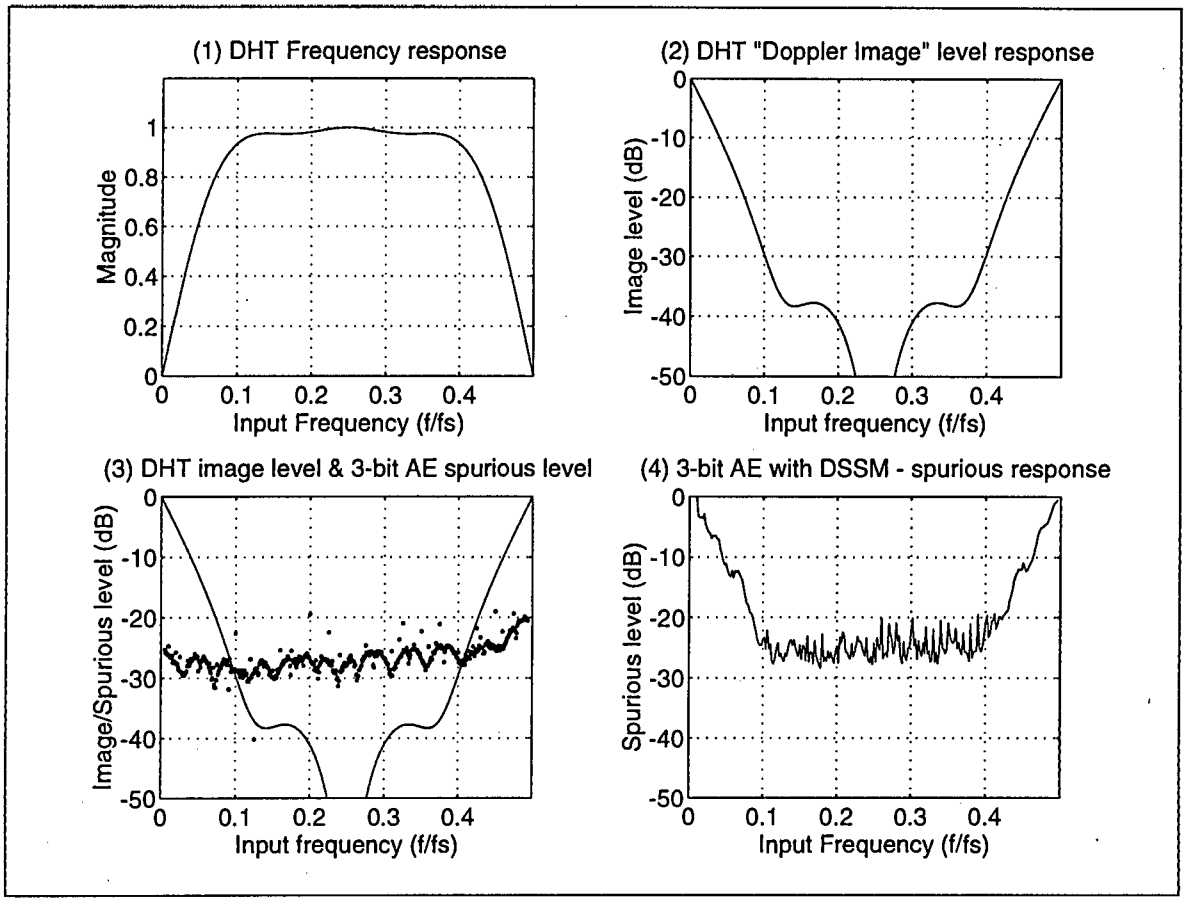

Figure 7.2 Comparison between DHT sideband level, 3-bit AE spurious level, and spurious level of 3-bit AE with DSSM

7.1.2 Simulation results

The simulation results showing the spurious level response of a 3-bit AE architecture, including a DSSM and the abovementioned DHT filter, are illustrated in plot (4) of *Figure 7.2*. Plot (3) illustrates the separate graphs of the normal 3-bit AE spurious characteristics (without DSSM - see also *Appendix B4*) as well as the DHT sideband response. The similarity of these two plots is clear. It leads one to the conclusion that, except for the Doppler sideband, the DSSM adds no substantial levels of spurious to the normal AE architecture. Simulations using different AE and DHT architectures produced similar results.

It can finally be concluded that the DSSM introduces no substantial levels of spurious, except for the Doppler sideband, which is created by the non-ideal frequency response of the DHT. The contribution of the DSSM to the total spurious response can therefore easily be calculated by simply calculating the Doppler sideband magnitude. The DHT frequency response is dependent on the filter length (N) and the coarseness of quantisation of the filter coefficients. These two parameters would therefore be the key factors in determining the performance of a DSSM subsystem.

7.2 QUADRATURE MODULATOR

The only viable technique found for digitally inducing a Doppler shift in the EBAE architecture, without influencing its extended bandwidth capability, is illustrated in *Figure 7.3*. It simply makes use of two DSSM units, as described in the previous section. Both the I and Q channels are modulated by the DSSM before being read out by the D/A. The modulation technique therefore adds a great deal of complexity to the system. Similar signal fidelity considerations as discussed in the previous section have to be taken into account in the design of such a system.

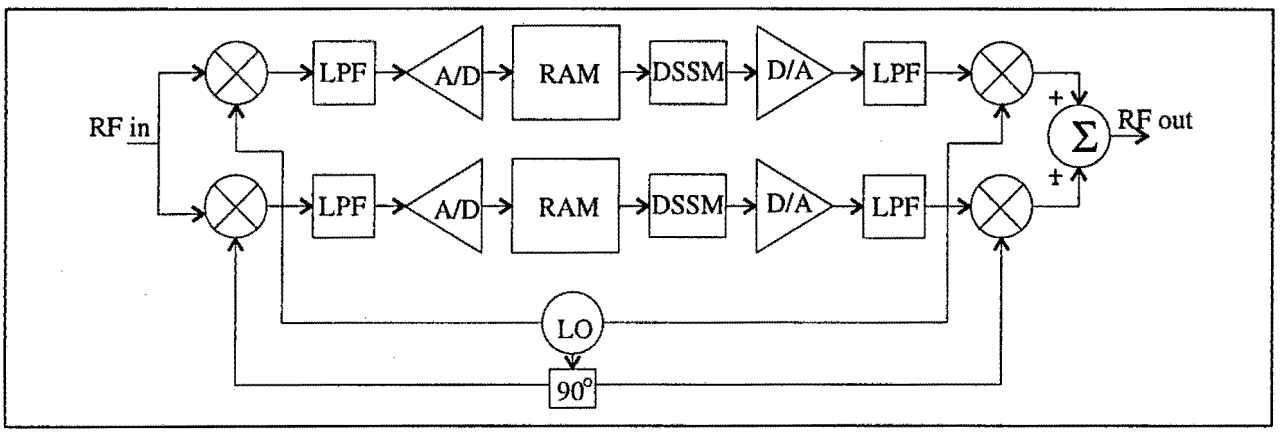

Figure 7.3 Block diagram for implementing a Doppler shift in the EBAE configuration

7.3 PHASE ADDER

The implementation of a frequency translation in the phase encoding techniques (PE and EBPE) is relatively simple compared to the techniques described in the previous two sections. Since the phase of the incoming signal is stored directly, it is easy to change the phase or frequency information of the stored signal.

To induce a frequency translation, a digital adder can simply be introduced somewhere in the digital path of the signal. This concept is illustrated in *Figure 7.4* as implemented in the EBPE architecture. Since frequency is the rate of change of phase, a linear increase in phase would represent a constant frequency offset. As the rate of change of the phase is increased, the induced Doppler frequency increases. This relationship is indicated by the following equation and the implementation thereof is shown in *Figure 7.4*

$$Phase_{Dopp} = f_{Dopp} \cdot t \quad \text{.....(7.2)}$$

In addition to its advantage of ease of implementation, this technique leads to no further degradation of signal quality. The phase is directly added to the stored signal without the introduction of any spurious or image frequencies. The ease of the manipulation of phase and frequency information makes the phase encoding architectures very attractive for this kind of application.

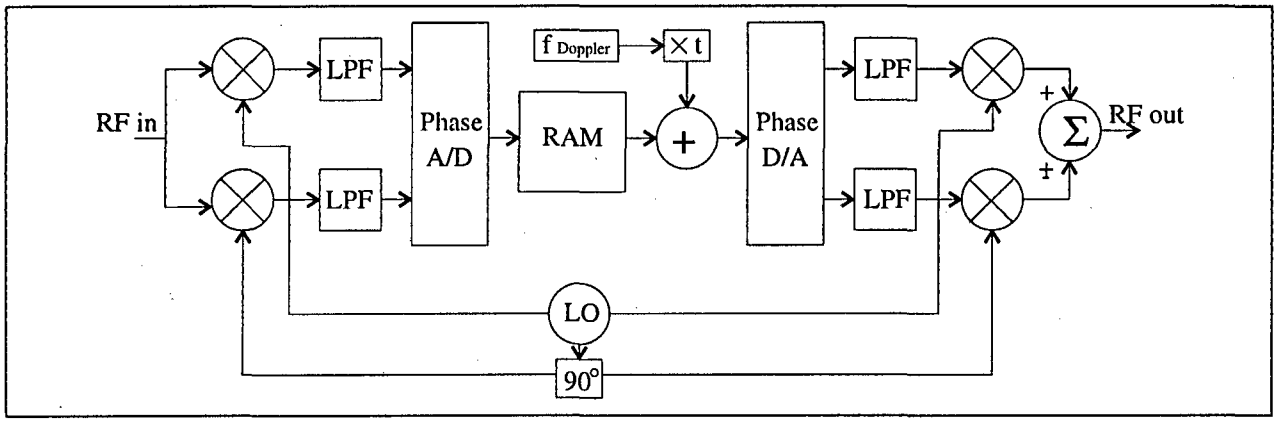

Figure 7.4 Block diagram of frequency translation technique using phase adding

Chapter 8

Conclusion

In this thesis a comparison of different techniques for the digital storage of broadband signals has been presented. There are many factors which contribute to the definition of a 'good' BDR architecture. These factors have been discussed in detail in the previous chapters by means of mathematical analyses and simulations. The core results are briefly summarised in this chapter to provide an overview of the advantages and disadvantages of each architecture.

8.1 OVERVIEW OF BDR ARCHITECTURES

Table 8.1 is a comparative table, giving the order of merit of the different architectures for each measure of comparison. Each architecture is awarded an order of merit: from a '2' for the architecture showing the best results, to a '0' for the worst. The characteristics are also weighted according to importance. By multiplying the characteristic weighting with the order of merit and by adding these scores for each architecture, an overall comparison of the architectures can be derived. This is indicated in the bottom row of the table. It is apparent that the characteristic weightings are a matter of opinion and will therefore vary from person to person and for different applications.

Overall, the AE architecture seems to produce the best results. Its disadvantages are sensitivity to input level and difficulty of implementing a frequency translation. Its instantaneous bandwidth is only f_s compared to the $2f_s$ bandwidth available to the EBAE and EBPE architectures.

The EBAE architecture shows generally poor results compared to the other architectures. The main reason for this being that the number of quantisation bits have to be divided between the two A/D converters. Consequently both A/D converters on the EBAE architecture have only half the quantisation bits, as compared to the A/D converters of the other architectures. This architecture would typically need more quantisation bits (i.e. more storage space) to achieve a comparative performance. Its main attraction is its $2f_s$ instantaneous bandwidth compared to the f_s available bandwidth of the AE architecture.

The two phase encoding architectures show very similar results. Instantaneous bandwidth is again the main advantage of the EBPE architecture, while the PE architecture shows slightly lower sensitivity to an I/Q phase imbalance. The main advantages of the phase encoding architectures are their insensitivity to input signal level as well as the ease of manipulating the phase and frequency information of the stored signal. Their inability to store amplitude information (for example amplitude modulated signals) is a noteworthy disadvantage of the phase encoding architectures.

It can be seen that each architecture has advantages and disadvantages. It would therefore be the final application and environment which would determine the 'best' architecture for that application.

Table 8.1 Overview of BDR architectures

	Weighting of character-istic	Unit of measure	AE	EBAE	PE	EBPE
SPURIOUS SIGNAL SUPPRESSION						
Quantisation and sampling: Constant amplitude signal	1	Spurious level	2	0	1	1
Quantisation and sampling: Amplitude modulated signal	1	Spurious level	2	1	0	0
I/Q imbalance	1	Sensitivity to I/Q imbalance	2	0	1	0
Dynamic range	1	Sensitivity to input level	0	0	2	2
PHASE/FREQUENCY ACCURACY	2	Level of phase jitter	2	0	1	1
INSTANTANEOUS BANDWIDTH	2	f_{sample}	0	2	0	2
EFFECT ON MATCHED FILTER RECEIVER						
linear FM	1/2	time sidelobe level	2	0	1	1
non-linear FM	1/2	"	1	1	1	1
Barker	1/2	"	2	0	1	1
RADAR transmitter/receiver	1/2	"	2	1	0	0
FREQUENCY TRANSLATION TECHNIQUES	2	ease of implementation	1	0	2	2
TOTAL			**15.5**	**6**	**11.5**	**14.5**

8.2 TECHNIQUES FOR IMPROVING BDR CHARACTERISTICS

8.2.1 Spurious signal reduction techniques

It was found (in *Section 3.7*) that the techniques for reducing spurious signal levels by the random modulation of the local oscillator have significant advantages (in terms of spurious levels and bandwidth) for the capturing of periodic data such as a single-tone signal. In such cases, a suitable modulation waveform has to be found, which is dependent on a number of system factors. For general communication and other wideband signals, however, this technique only adds complexity to the system without having meaningful benefits.

8.2.2 Bandwidth extension by interlaced sampling

It was found (in *Section 5.2*) that the technique of bandwidth extension by means of interlaced sampling requires very accurate read-in and read-out timing if low spurious levels (i.e. good 'image' suppression) or low attenuation of the desired signal is required. The timing accuracy requirements increase with an increase in the number of interlaced channels used.

8.3 FUTURE WORK

A thorough investigation into the waveform and spectral distortions caused by coarse quantization was presented in Chapters 3 and 4. Most of this work (for example on spurious signal content, phase error, phase jitter, etc.) was performed for a single-tone input. As was also mentioned in the introduction, waveform fidelity is not easily defined. A more thorough investigation than purely spurious levels and phase jitter for a single-tone input is usually required, especially when considering a typical wideband receiver, in which case the quality of the incoming signal is determined by the receiver output. In Chapter 6 a comparison was made of the waveform fidelity for the different encoding architectures from a receiver point of view. A matched filter receiver and a number of wideband signals were used as a basis for the comparison.

Since most broadband repeaters are used for the capture and re-transmission of wideband signals, future work could include a more thorough investigation into the distortions caused by BDR architectures in broadband signals. Different classes of broadband signals which are typically used in BDR-related applications would have to be identified, as well as the signal properties which define their 'quality'. Typical transmitter/receiver architectures could also be identified and simulated in conjunction with the BDR simulations in order to quantify the extent of signal distortions caused by BDR architectures. Digital frequency translation techniques could also be included in such simulations and their effect on the signal fidelity be investigated.

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Appendix A

Appendix A1.

Derivation of an equation for the frequency spectrum of the Frequency Memory Loop (FML) mode.

Figure A1 illustrates the output waveform of a short pulse with length τ repeated N times to produce an output pulse of length τ_2 (i.e. $\tau_2 = N\tau$). A phase error of ψ occurs at every repetition interval.

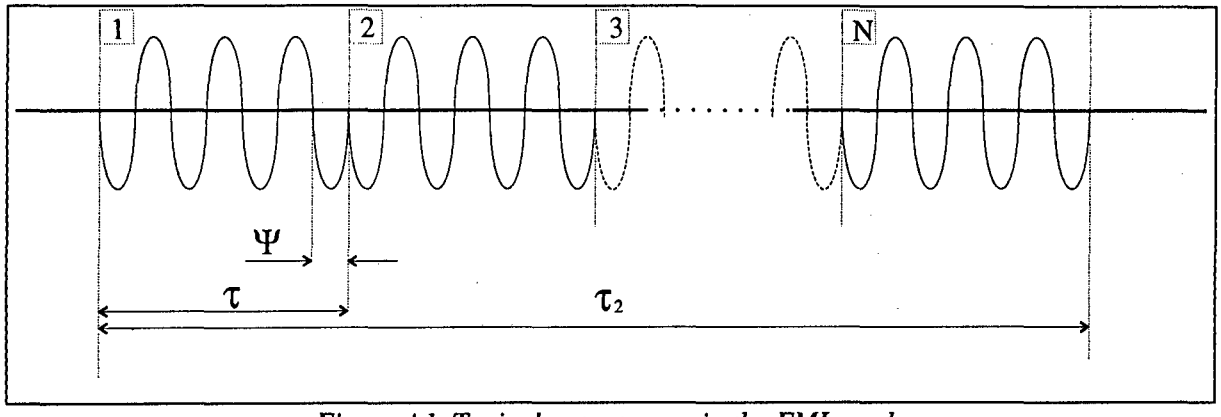

Figure A1 Typical output wave in the FML mode

The Fourier transform of the sinusoidal modulation signal with frequency f_o is given by

$$\cos(\omega_o t) \xleftrightarrow{F} \pi\left[\delta(\omega-\omega_o)+\delta(\omega+\omega_o)\right] \quad \text{.....(A1.1)}$$

A sample of length τ of this signal is now read into the memory:

$$rect\left(\frac{t}{\tau}\right) \xleftrightarrow{F} \tau \cdot Sa\left(\frac{\omega\tau}{2}\right)$$

$$\therefore \cos(\omega_o t)\cdot rect\left(\frac{t}{\tau}\right) \xleftrightarrow{F} \tau\pi\left[Sa\left(\frac{\tau}{2}(\omega-\omega_o)\right)+Sa\left(\frac{\tau}{2}(\omega+\omega_o)\right)\right] \quad \text{.....(A1.2)}$$

where:

$$Sa(x) \equiv \frac{\sin(x)}{x}$$

$$rect\left(\frac{t}{x}\right) \equiv \begin{cases} 1; -\frac{x}{2} < t < \frac{x}{2} \\ 0; otherwise \end{cases}$$

and:

$$\tau = mT_o + \Psi$$

where ψ is the phase discontinuity, m is any integer and T_o is the period of the original sinusoid.

This pulse is now repeated with period τ.

The Fourier coefficients, F_n, can thus be calculated as:

$$F_n = \pi\left[Sa\left(\frac{\tau}{2}(n\varpi - \omega_o)\right) + Sa\left(\frac{\tau}{2}(n\varpi + \omega_o)\right)\right] \quad \text{.....(A1.3)}$$

where:

$$\varpi = \frac{2\pi}{\tau}$$

From this the Fourier transform of the repeated sample, $F(\omega)$, can be written as:

$$F(\omega) = 2\pi \sum_{n=-\infty}^{\infty} F_n \cdot \delta(\omega - n\varpi) \quad \text{.....(A1.4)}$$

This repeated sample is now multiplied by a rectangular window of length τ_2 so that the Fourier transform of the output of the DRFM, $G(\omega)$, can be written as:

$$G(\omega) = 2\pi\tau_2 \cdot \sum_{n=-\infty}^{\infty} F_n \cdot Sa\left(\frac{\tau_2}{2}(\omega - n\varpi)\right) \quad \text{.....(A1.5)}$$

where

$$F_n = \pi\left[Sa\left(\frac{\tau}{2}(n\varpi - \omega_o)\right) + Sa\left(\frac{\tau}{2}(n\varpi + \omega_o)\right)\right]$$

Appendix A2.

Derivation of an equation for the frequency spectrum of a sinusoidal signal being sampled interlaced with imperfect sampling and readout timing relations

Figure A2. illustrates a sinusoidal signal being sampled by a system using interlaced sampling and having the following system characteristics:

- Two-channel system (N=2).
- Sinusoidal input signal.
- A relative sampling timing error τ_1 is made in the sampling process.
- The original timing relation between the interlaced samples is **not** retained during the reconstruction of the signal (i.e. a further timing error of τ_2 is induced in the readout process).
- A normal ideal lowpass filter is used in the reconstruction process.

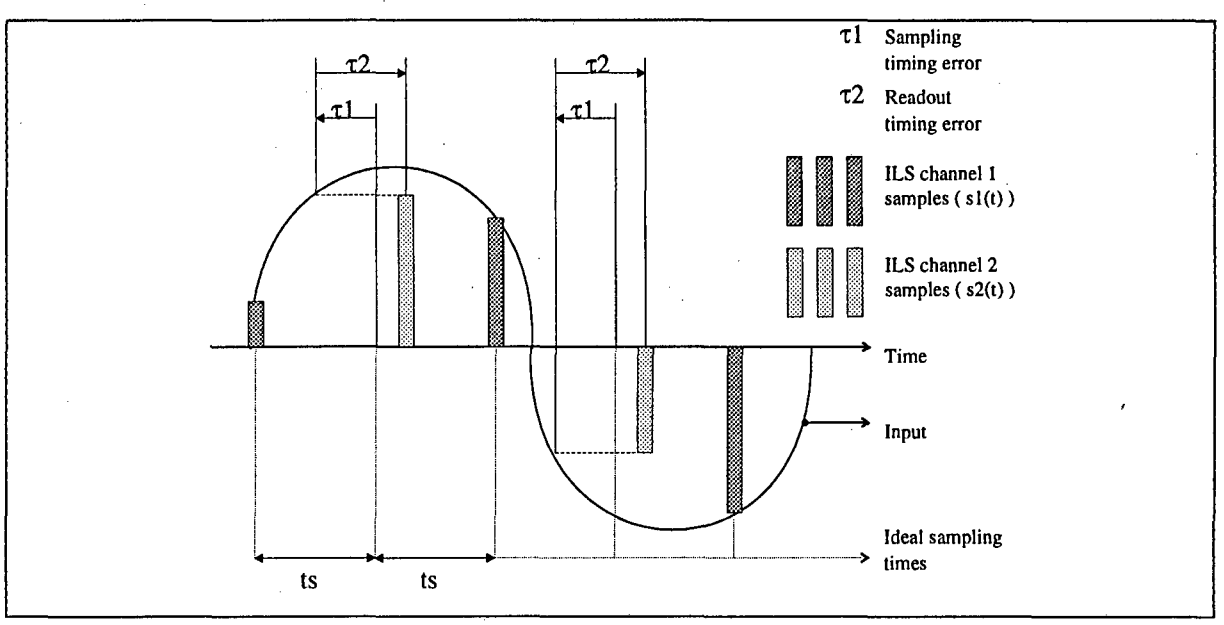

Figure A2. Sinusoidal signal being sampled by a 2-channel interlaced sampling process

The sequence of sample impulses *s(t)* can be seen as the sum of the channel(1) and channel(2) impulse sequences:

$$s(t) = s_1(t) + s_2(t)$$
$$= \left\{p(t)\cdot\delta_{2t_s}(t)\right\} + \left\{p(t-\tau_2)\cdot\delta_{2t_s}(t-t_s+\tau_1-\tau_2)\right\} \quad \text{.....(A2.1)}$$

where $\delta_{t_o}(t) = \sum_{n=-\infty}^{\infty} \delta(t - nt_0)$

and $p(t)$ is the input signal, in this case: $p(t) = \cos(2\pi f_1 t)$

The output spectrum ($G(f)$) of such a system can therefore be written as:

$$\begin{aligned} G(f) &= H(f) \cdot \left\{ F\left\{ p(t) \cdot \delta_{2t_s}(t) \right\} + F\left\{ p(t-\tau_2) \cdot \delta_{2t_s}(t - t_s + \tau_1 - \tau_2) \right\} \right\} \\ &= H(f) \cdot \left\{ F\left\{ p(t) \cdot \delta_{2t_s}(t) \right\} + e^{-j2\pi f \tau_2} F\left\{ p(t) \cdot \delta_{2t_s}(t - t_s + \tau_1) \right\} \right\} \end{aligned} \quad \text{.....(A2.2)}$$

where $F(.)$ denotes the Fourier transform and $H(f)$ is the ideal filter transfer function used to reconstruct the original input from the impulse sampling sequence:

$$H(f) = \begin{cases} 1 & |f| < \frac{f_s}{2} \\ 0 & otherwise \end{cases} \quad \text{.....(A2.3)}$$

Looking at the terms in *Equation A2.2.* separately:

- $$\begin{aligned} F\left\{ p(t) \cdot \delta_{2t_s}(t) \right\} &= F\left\{ p(t) \right\} * F\left\{ \delta_{2t_s}(t) \right\} \\ &= \delta(f \pm f_1) * \left[\frac{\pi}{t_s} \cdot \delta_{\frac{1}{2t_s}}(f) \right] \quad \text{.....(A2.4)} \\ &= \frac{\pi}{t_s} \cdot \delta_{\frac{1}{2t_s}}(f \pm f_1) \end{aligned}$$

- $$\begin{aligned} F\left\{ p(t) \cdot \delta_{2t_s}(t - t_s + \tau_1) \right\} &= F\left\{ p(t) \right\} * F\left\{ \delta_{2t_s}(t - t_s + \tau_1) \right\} \\ &= \delta(f \pm f_1) * \left[\frac{\pi}{t_s} \delta_{\frac{1}{2t_s}}(f) \cdot e^{-j2\pi f(t_s - \tau_1)} \right] \quad \text{.....(A2.5)} \\ &= \frac{\pi}{t_s} \cdot \delta_{\frac{1}{2t_s}}(f \pm f_1) \cdot e^{-j2\pi(f \mp f_1)(t_s - \tau_1)} \end{aligned}$$

Substituting these two factors into *Equation A2.2.* it can be seen that the output spectrum is a series of impulses multiplied by the windowing function $H(t)$:

$$G(f) = H(f) \cdot \frac{\pi}{t_s} \cdot \delta_{\frac{1}{2t_s}}(f \pm f_1) \cdot \left[1 + e^{-j2\pi[(f \mp f_1)(t_s - \tau_1) + f\tau_2]}\right] \quad \text{.....(A2.6)}$$

There are thus four impulses in the frequency span limited by the windowing function H(f). For $|f_1| < f_s/2$:

at $f = f_1$: $$G(f_1) = \frac{\pi}{t_s}\left[1 + e^{j\phi_1}\right] \quad \text{.....(A2.7)}$$

at $f = (f_1 - f_s/2)$: $$G\left(f_1 - \frac{f_s}{2}\right) = \frac{\pi}{t_s}\left[1 + e^{j\phi_2}\right] \quad \text{.....(A2.8)}$$

at $f = -f_1$: $$G(-f_1) = \frac{\pi}{t_s}\left[1 + e^{-j\phi_1}\right] \quad \text{.....(A2.9)}$$

at $f = (-f_1 + f_s/2)$: $$G\left(-f_1 + \frac{f_s}{2}\right) = \frac{\pi}{t_s}\left[1 + e^{-j\phi_2}\right] \quad \text{.....(A2.10)}$$

where $\phi_1 = -2\pi f_1 \tau_2$

and $\phi_2 = \pi\left[1 - \tau_1 f_s + \tau_2 (f_s - 2f_1)\right]$

Appendix B

Appendix B1 : Output PDS for single-tone input

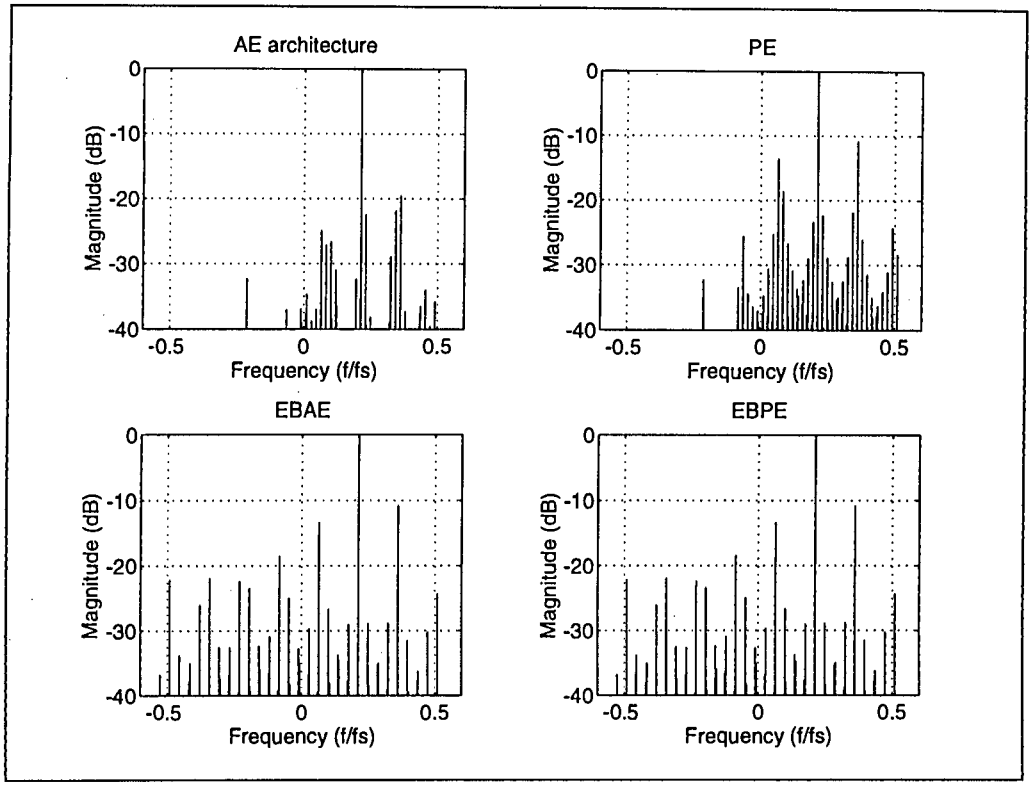

Figure B1.1 Output PDS for single-tone input: 2-bit quantisation

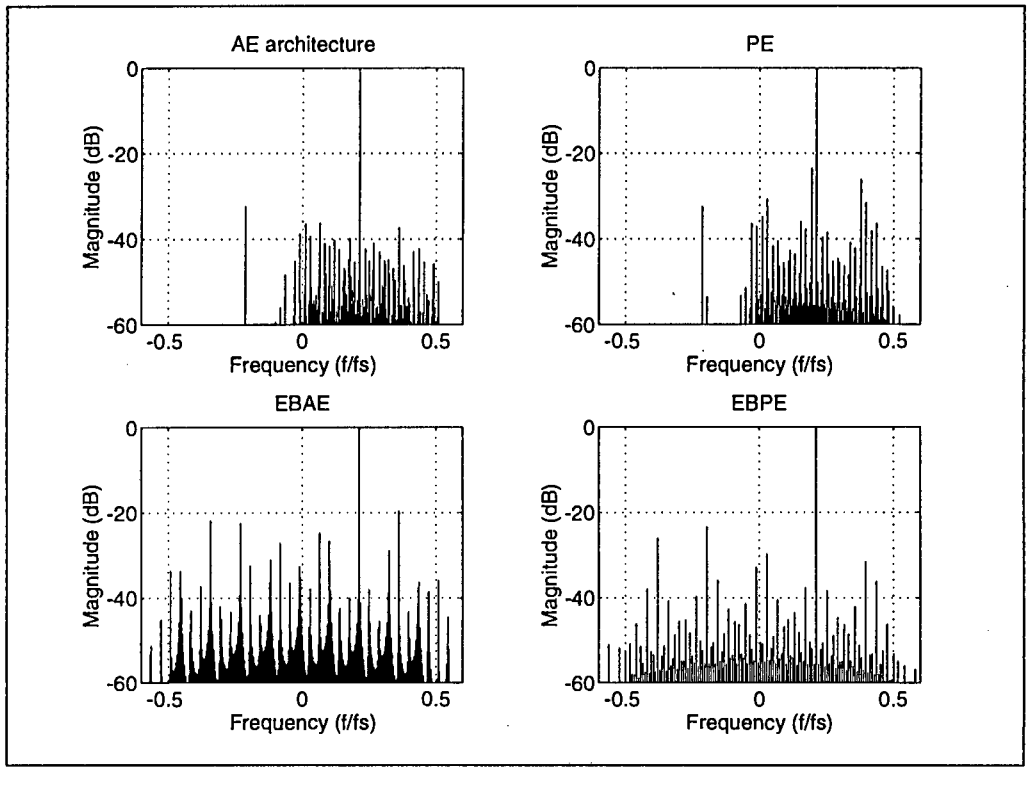

Figure B1.2 Output PDS for single-tone input: 4-bit quantisation

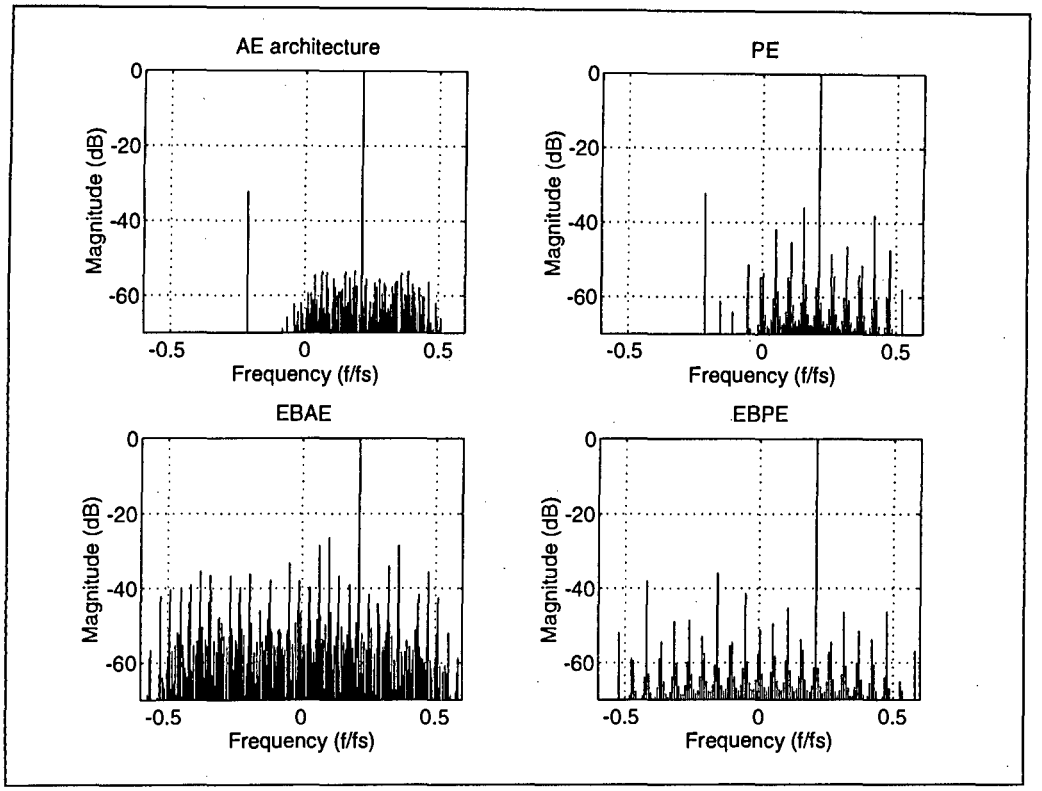

Figure B1.3 Output PDS for single-tone input: 6-bit quantisation

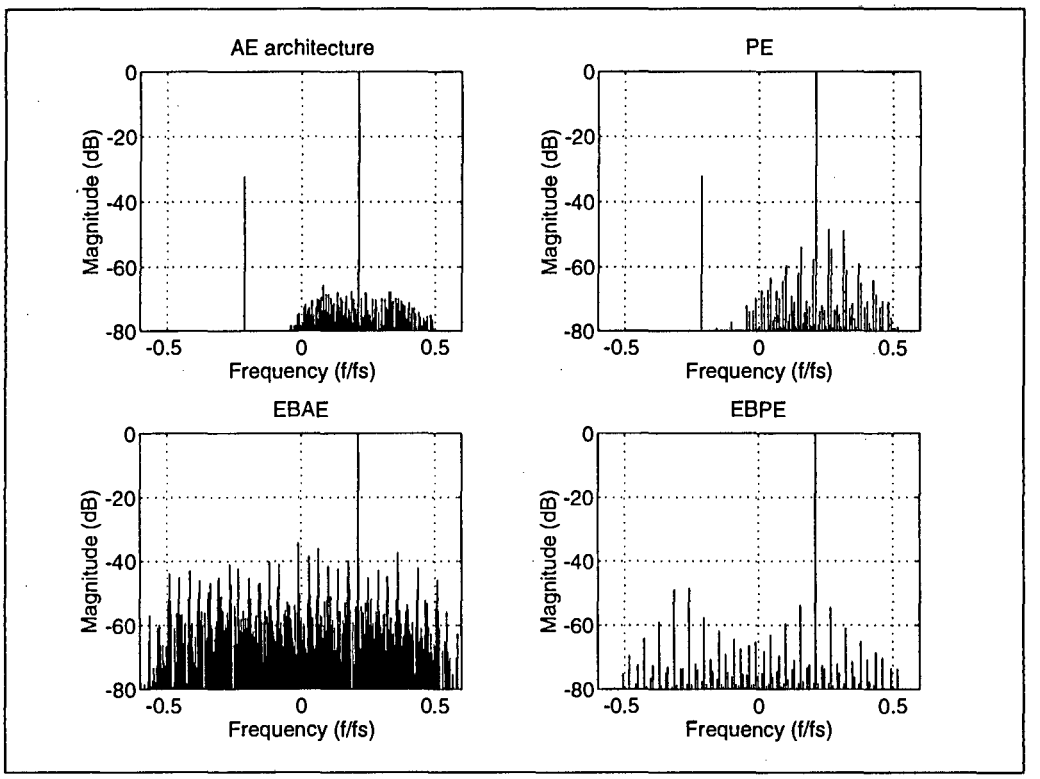

Figure B1.4 Output PDS for single-tone input: 8-bit quantisation

Appendix B2 : Output PDS for two-tone input

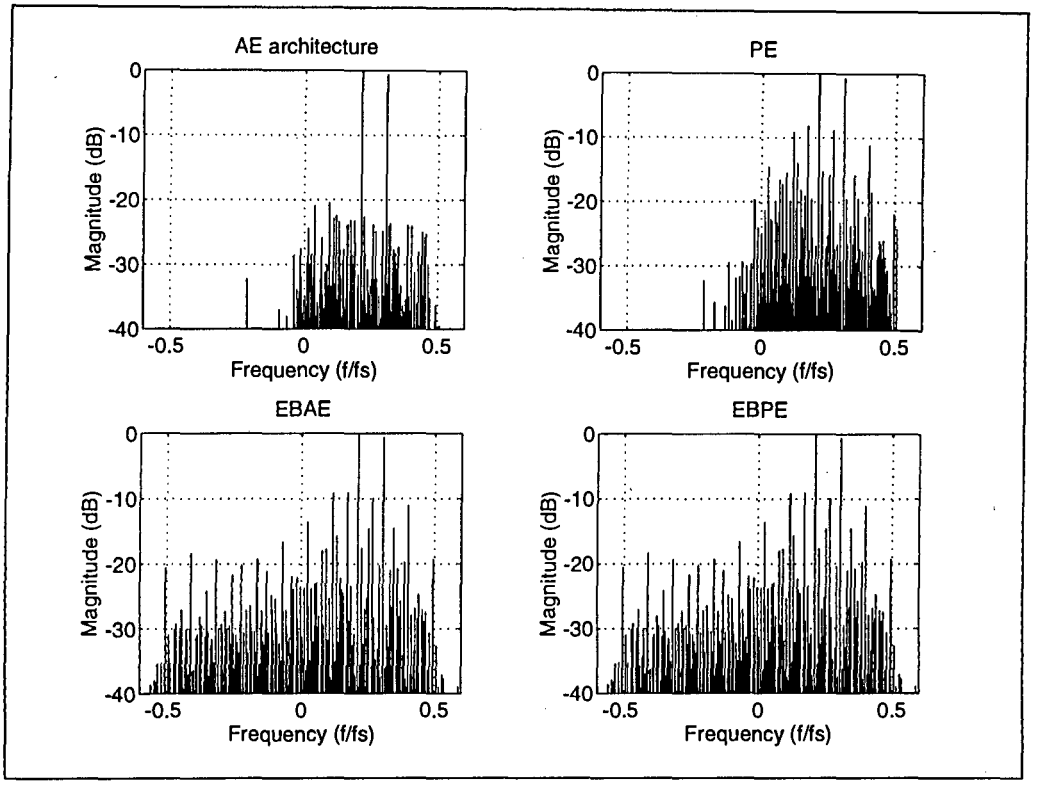

Figure B2.1 Output PDS for two-tone input: 2-bit quantisation

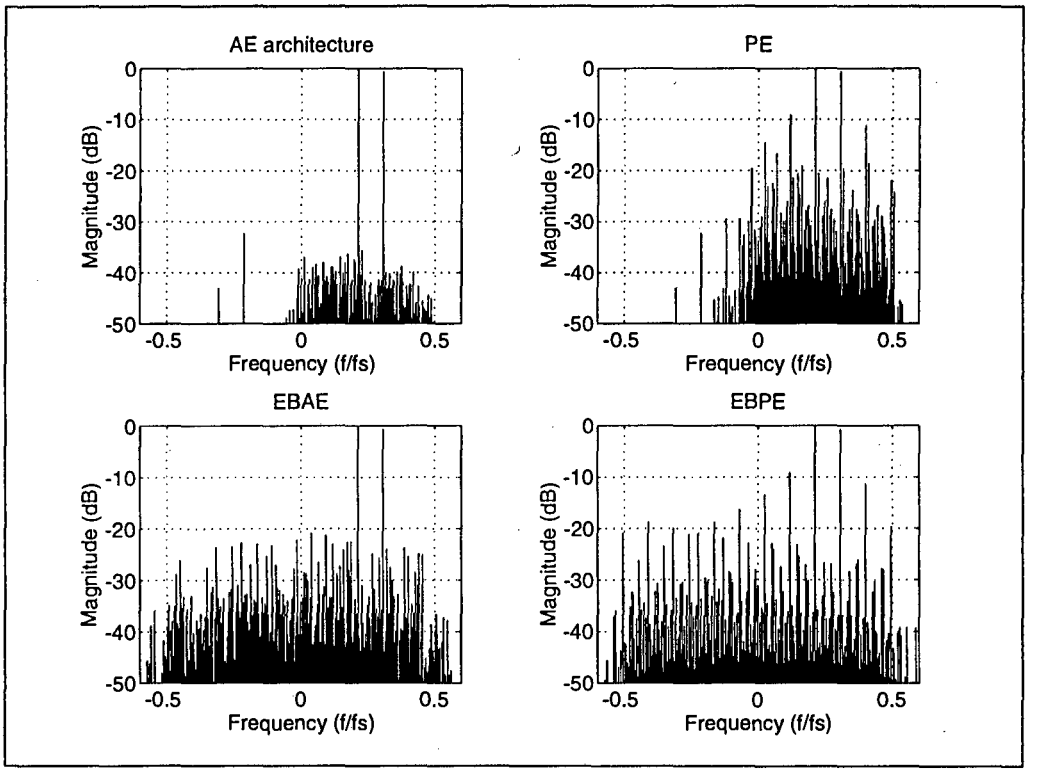

Figure B2.2 Output PDS for two-tone input: 4-bit quantisation

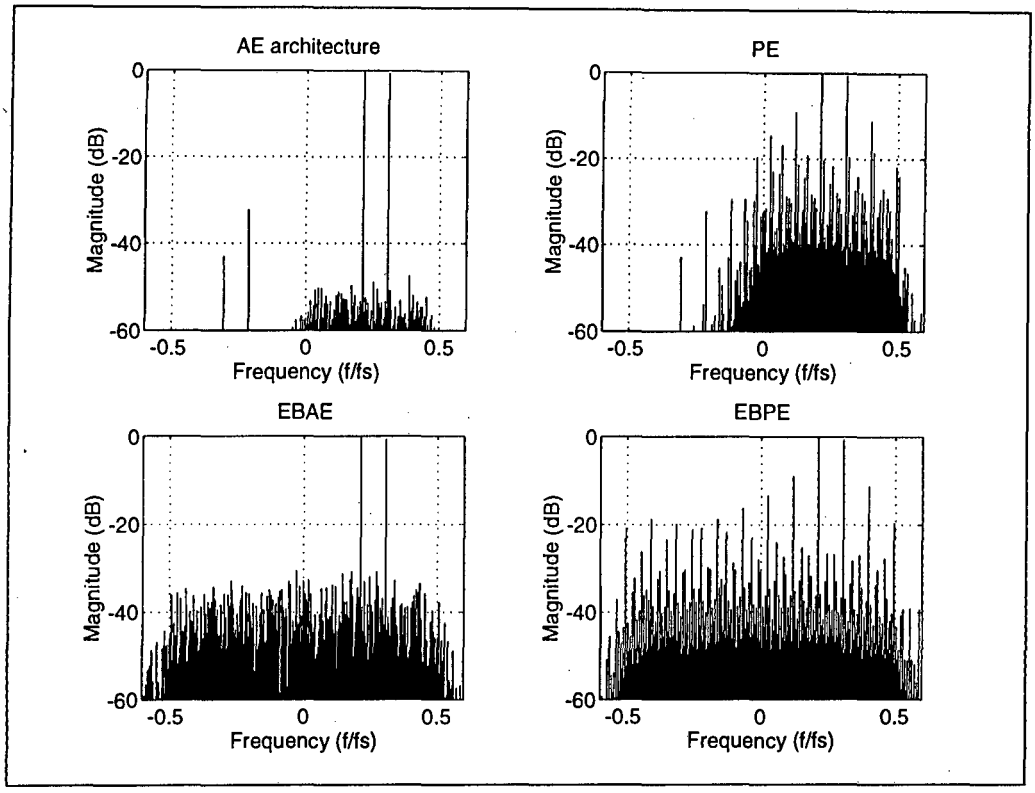

Figure B2.3 Output PDS for two-tone input: 6-bit quantisation

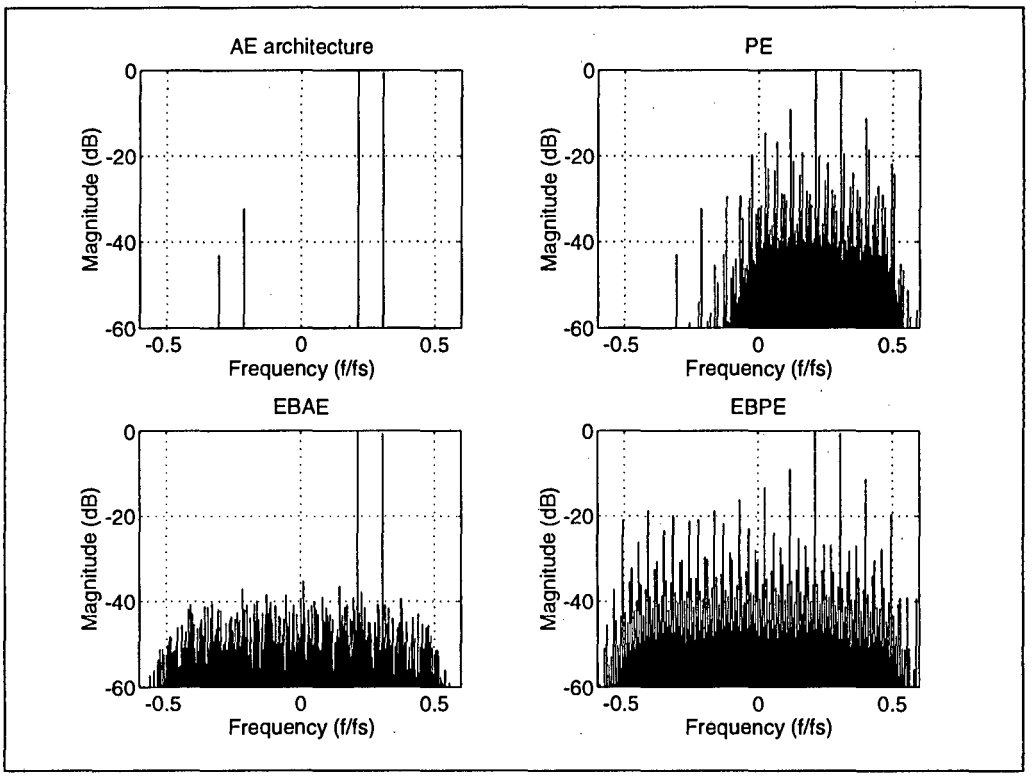

Figure B2.4 Output PDS for two-tone input: 8-bit quantisation

Appendix B3 : Output PDS for wideband chirp input

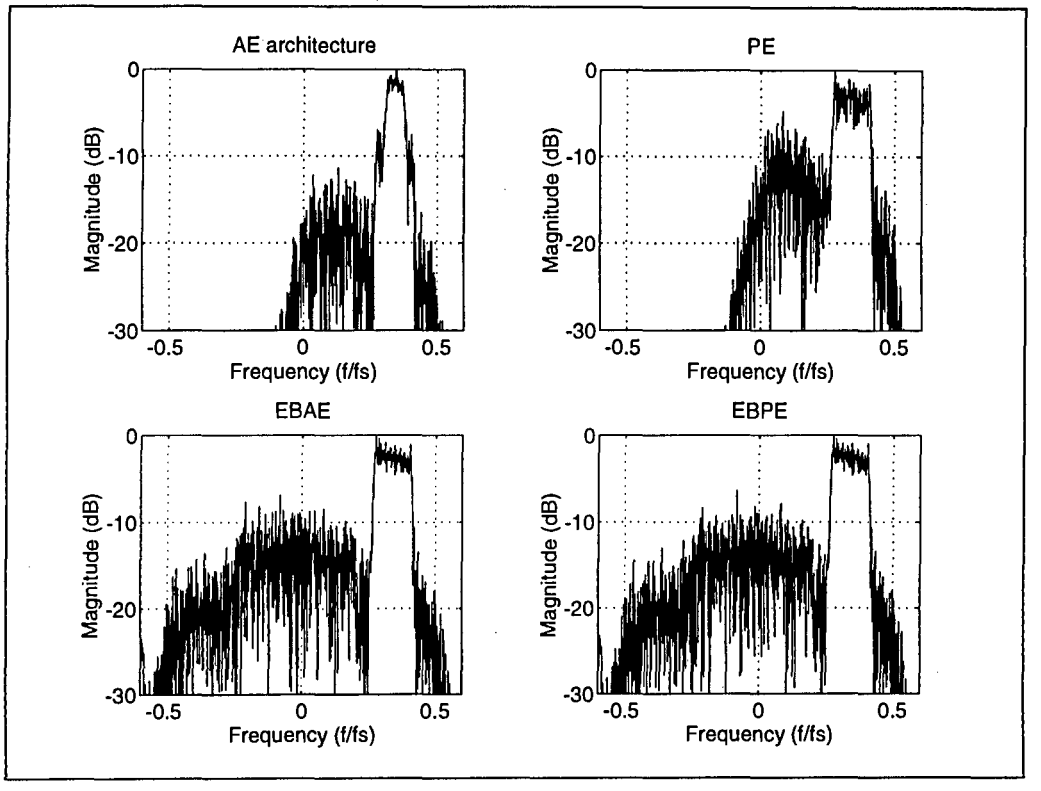

Figure B3.1 Output PDS for wideband chirp: 2-bit quantisation

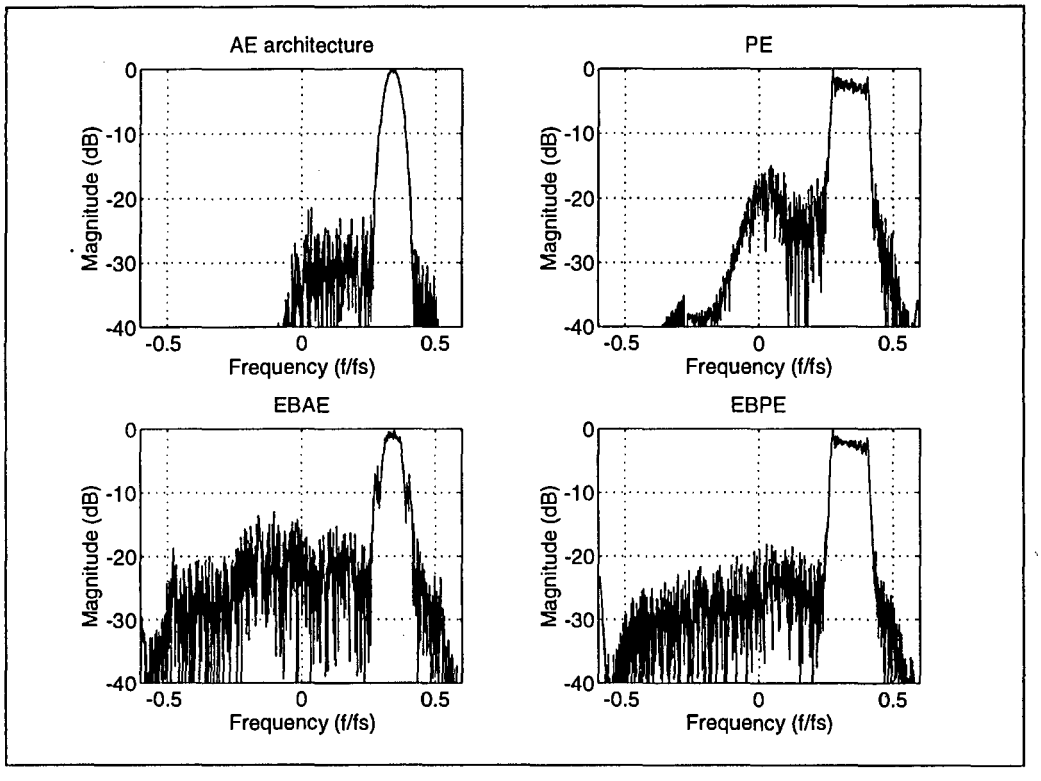

Figure B3.2 Output PDS for wideband chirp: 4-bit quantisation

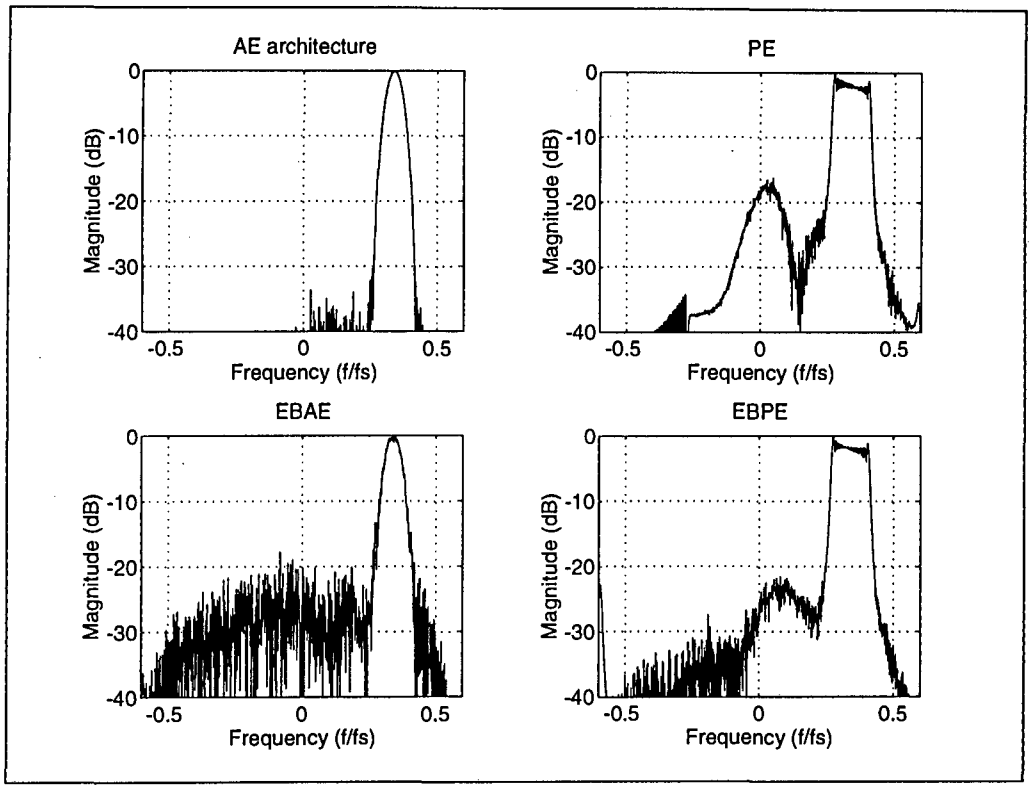

Figure B3.3 Output PDS for wideband chirp: 6-bit quantisation

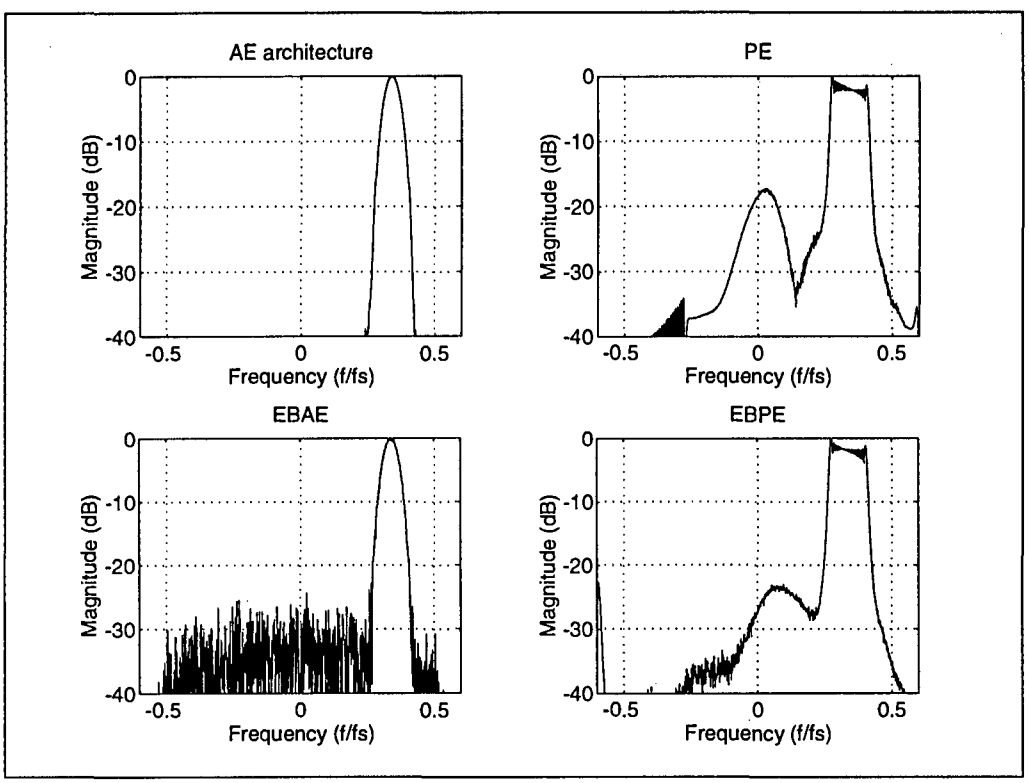

Figure B3.4 Output PDS for wideband chirp: 8-bit quantisation

Appendix B4 : Spurious signal level vs. input frequency

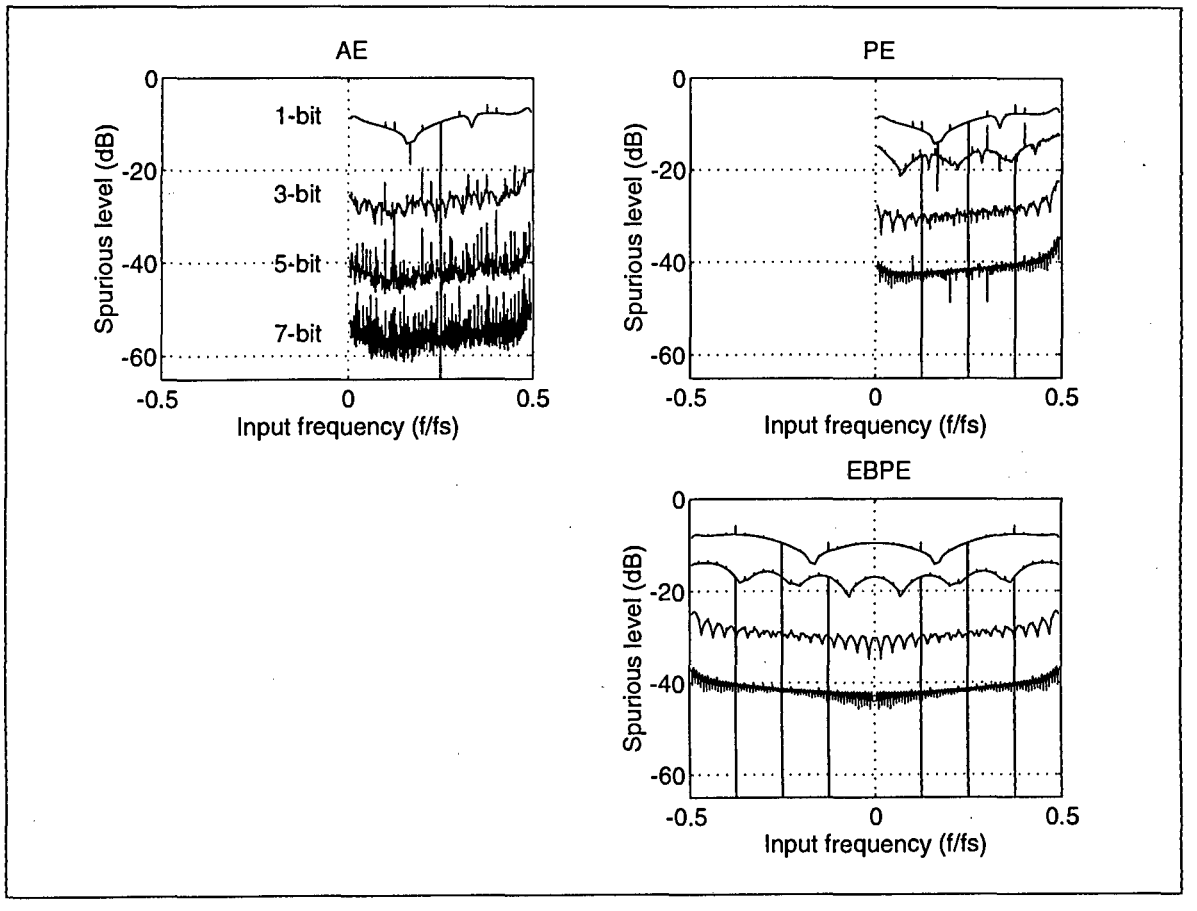

Figure B4. Spurious vs. input frequency for different BDR architectures

Appendix B5 : Spurious signal level vs. input signal level

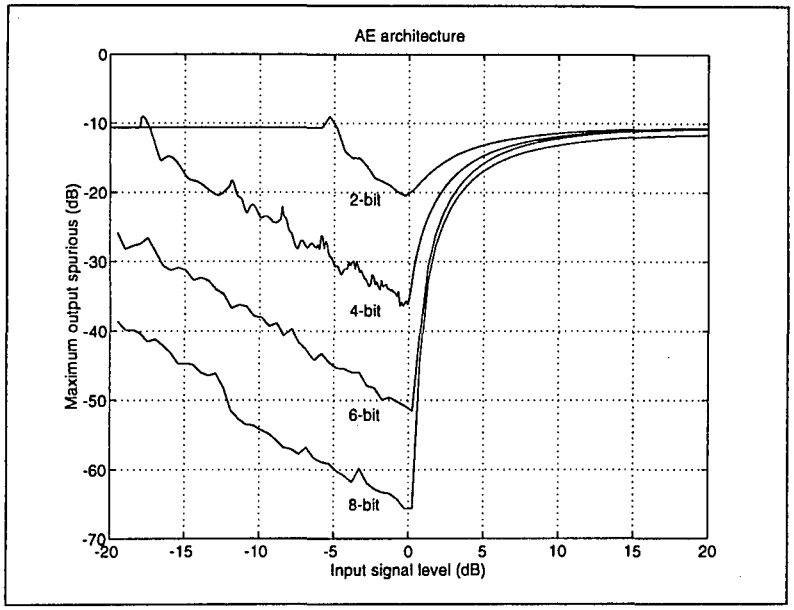

Figure B5.1 Spurious signal level vs. input signal level: AE architecture

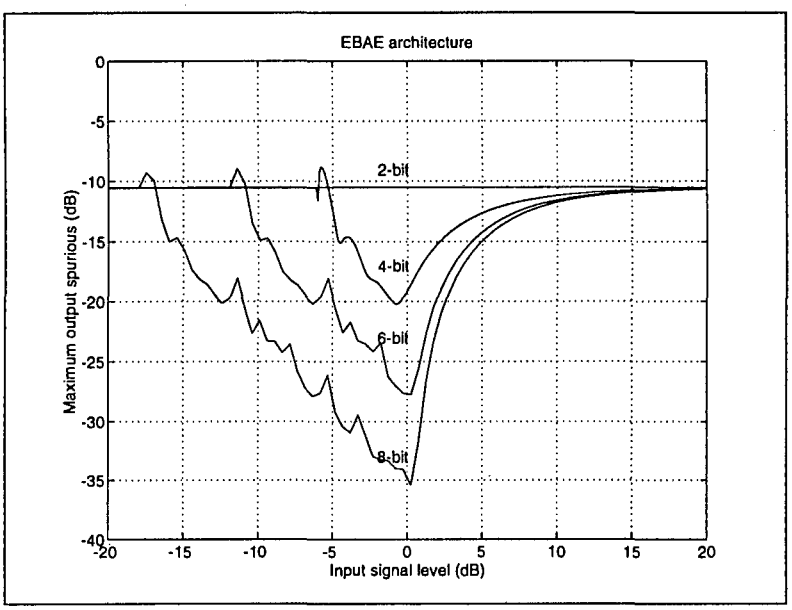

Figure B5.2 Spurious signal level vs. input signal level: EBAE architecture

The spurious signal levels of the PE and EBPE architectures are independent of input signal level. The reader is referred to *Table 3.2* for values of output spurious signal levels for the phase encoding architectures and for different numbers of quantisation bits.

Appendix B6 : Phase jitter vs. input signal level

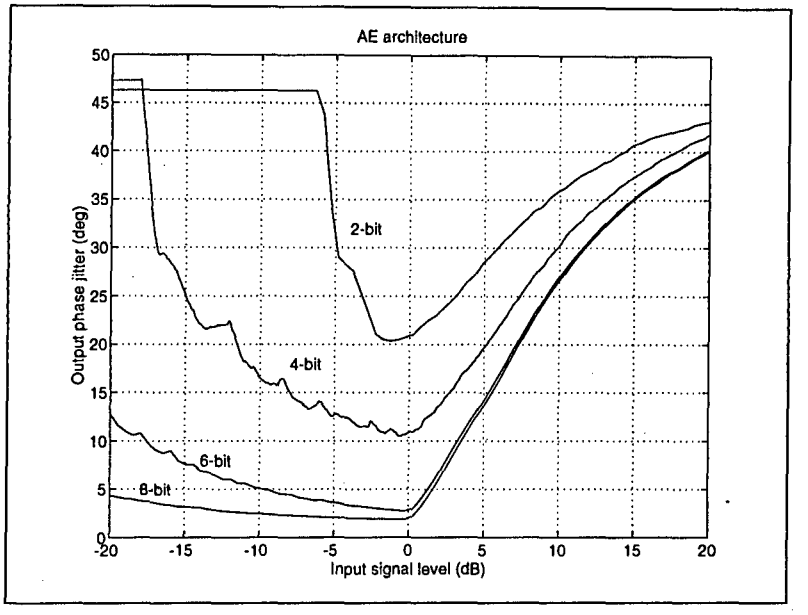

Figure B6.1 Output signal phase jitter vs. input signal level: AE architecture

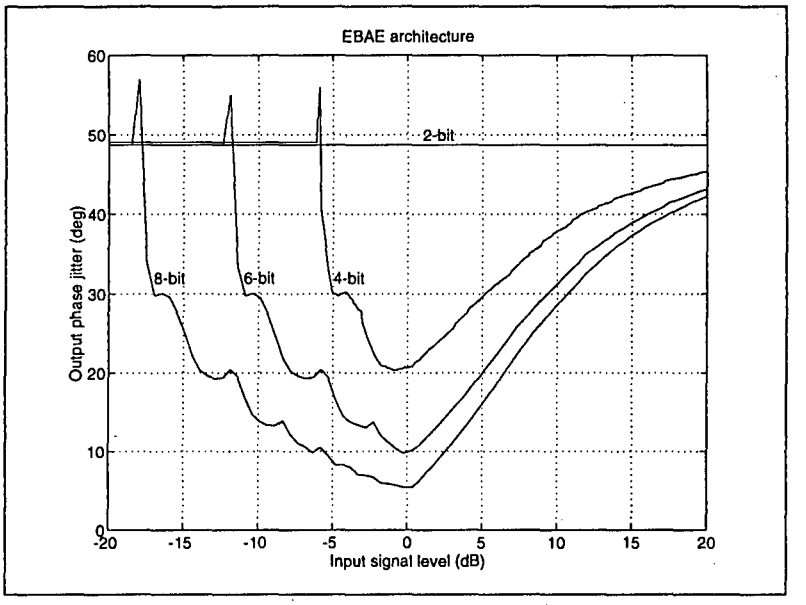

Figure B6.2 Output signal phase jitter vs. input signal level: EBAE architecture

The output signal phase jitter of the PE and EBPE architectures is independent of input signal level. The reader is referred to *Equation 4.5* for the calculation of phase jitter for the phase encoding architectures and for different numbers of quantisation bits.

Appendix B7 : Matched filter sidelobe levels vs. carrier frequency for 13-chip Barker code

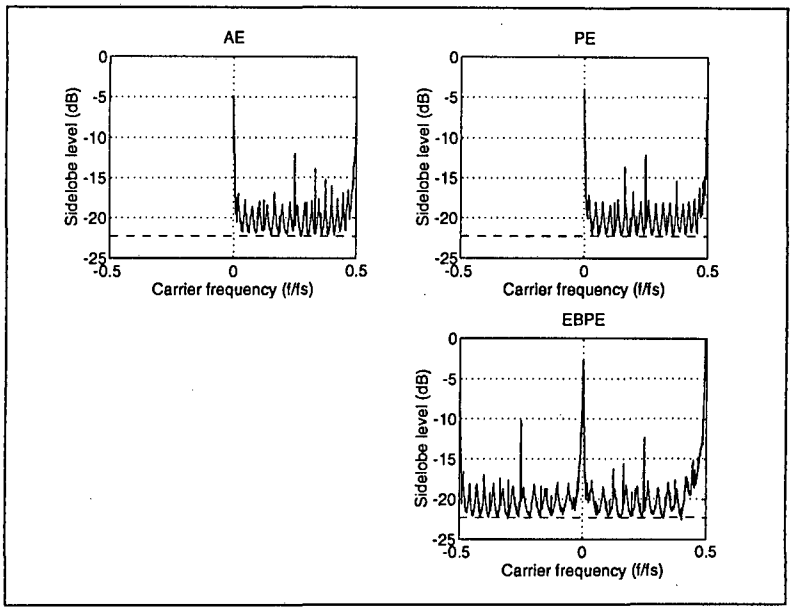

Figure B7.1 Sidelobe level vs. carrier frequency for 1-bit BDR architectures

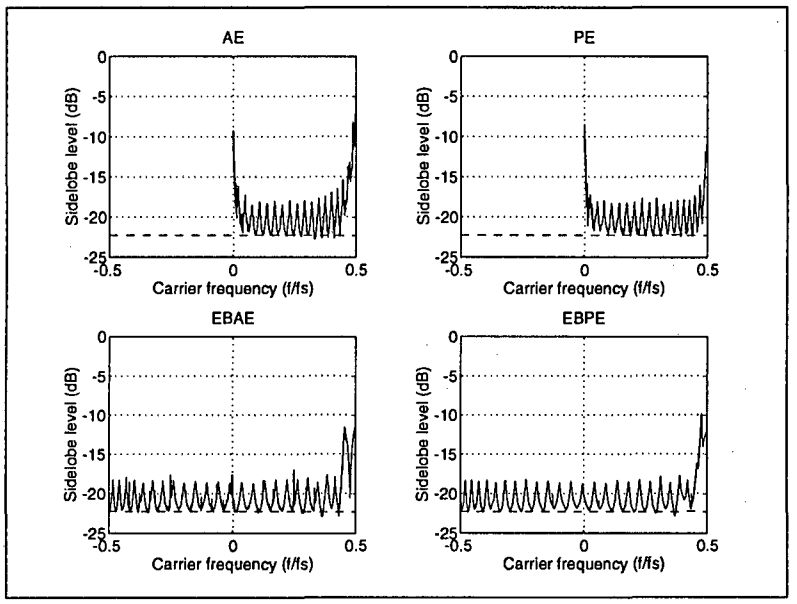

Figure B7.2 Sidelobe level vs. carrier frequency for 4-bit BDR architectures