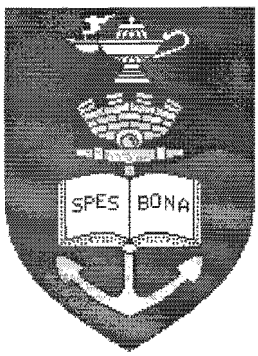

UNIVERSITY OF CAPE TOWN
DEPARTMENT OF ELECTRICAL ENGINEERING

A SINGLE TO THREE PHASE VARIABLE SPEED DRIVE WITH UNITY POWER FACTOR

PREPARED FOR : The Department of Electrical Engineering
University of Cape Town

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SYNOPSIS

The new proposed topology for a single three-phase variable speed drive was developed after considering the advantages and disadvantages of previous topologies. The new topology employs only six switches that form an active front-end rectifier and a four-switch inverter. The active front-end rectifier is the first leg of the three-phase bridge. It not only rectifies the voltage source but it also regulates one of the phases for the motor. The four-switch inverter produces the variable frequency.

Excessive distortion currents drawn by a converter can cause voltage distortions. For this reason the converter should draw a high quality sinusoidal current from the supply. Excessive currents drawn from the supply are also the result of poor power factors. The converter should therefore operate at close to unity power factor. N Mohan, T Underland, W.P Robins [3].

The drive was simulated using the simulation package ORCAD version 9. The simulation proved that the previous method of DC bus regulation by phase shifting could never guarantee a unity power factor operation. M Malengret [2]. The previous method calculated a DC bus voltage needed and kept it constant by phase shifting the fundamental, of the first leg of the converter, to the voltage source.

A unity power factor control strategy is introduced. The strategy shows that if the power factor is fed back instead of the DC bus voltage, then unity power factor is guaranteed. The DC bus will always rise according to following equation :

$V_d = \frac{2}{ma} VSec(\delta)$ for unity power factor.

where :

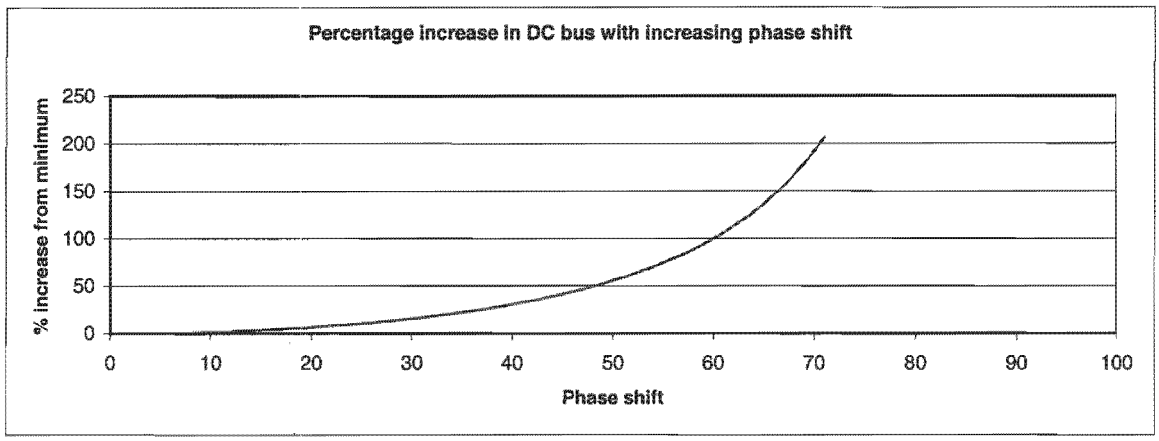
V_d is the DC voltage across the DC bus.

V is the peak AC voltage of the voltage source.

ma is the modulation index.

δ is the amount of phase shift between the voltage source and the fundamental of the first leg of the converter.

The equation shows that the DC bus voltage will rise as the phase shift is increased.



The above plot shows the percentage rise in DC bus voltage with increasing phase shift. The maximum amount of phase shift is derived by choosing the maximum voltage for the DC bus. A 10% rise in DC bus voltage, from the minimum, requires a 25^0 phase shift.

The choice of inductance used in the converter depends on the amount of phase shift required as well as the power rating of the converter. The equation relating the inductance, phase shift and output power was derived. The equation shows that

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}.$$

If the phase shift, δ, is obtained by considering the increase in DC bus voltage then the inductance can be determined by the output power requirements of the converter.

The hardware was set up and a 110V line to line 1 horse power motor was used test the performance of the drive. A Texas Instruments digital signal processor was used to control the drive. The experimental results were obtained and found to correlate with the mathematical derivations and simulation results.

The new topology has both advantages and disadvantages.

The advantages are:

- The drive draws a high quality sinusoidal current.
- The drive does real time power factor correction and maintains a unity power factor.
- Power flow is bi-directional
- The drive delivers a high quality three phase output current and voltage even when the source voltage was distorted.

The disadvantages are:

- The high DC link voltage causes the voltage rating of the semiconductors and capacitors to be higher.
- The high line to neutral voltage can cause problems with the insulation of the motor windings.

The advantages over the previous topologies are :

- The line to line voltages are all symmetrical and therefore this system does not suffer from negative sequence harmonics.

In the topology used in this project, the modulation index of the front-end charger had to be less than 1 and kept constant. This resulted in a DC bus voltage that increased with an increase in phase shift. The rise in DC bus is shown by the following equation,

$$V_d = \frac{2}{ma} VSec(\delta).$$

If the modulation index were to be varied then the DC bus voltage can be kept constant. Space vector modulation allows over modulation to 115%. This method of modulation will facilitate the maintenance of a constant DC bus voltage. It is therefore recommended that space vector modulation be implemented to maintain a constant DC bus voltage.

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CHAPTER 1
INTRODUCTION

This thesis describes the development of a new topology for a single to three-phase variable speed drive.

1.1 BACKGROUND TO THE STUDY

The supply of single-phase power is more economically viable than the supply of three-phase power for low power applications. The use of a single to three-phase variable speed drive drastically reduces the cost of the transmission equipment needed to transmit power from the distribution. For this reason a low power three phase motor rated at a few kilowatts can be powered from a single phase supply with the aid of a single to three phase variable speed drive.

When converters are connected to the power grid, the quality of the currents drawn from the supply can affect the voltage at the receiving end of the transmission line. The quality of the currents drawn depend on the type of topology used in the converter design. Ideally a purely sinusoidal current should be drawn from the supply, however in practice most converters draw distorted currents. These distortion currents cause the voltage at the receiving end to be distorted. As a result other equipment connected to the receiving end of the transmission line will also receive a distorted voltage waveform. N Mohan, T Underland, W.P Robins (3).

Bi-directional power flow is necessary if regenerative braking is to be used. Power should be able to flow to and from the supply. In this case the drive also has to be synchronized to the frequency of the supply. The drive should be immune to fluctuations in the frequency and voltage of the supply.

1.2 OBJECTIVES OF THIS THESIS

The objective of this thesis is to design an efficient single to three phase variable speed drive for low power three phase applications. The drive should have the following features:

- Active input current shaping for sinusoidal input currents.
- Bi-directional flow of power.
- Close to unity power factor operation.
- A high quality variable three phase voltage and frequency output.
- A simple control scheme.
- A reduced number of power electronic devices.

1.3 CONSTRAINTS OF THE THESIS

The constraints of the thesis were on simulation time, hardware and software.

1.3.1 Limitation of simulation time

The simulations were done using the simulation package ORCAD version 9. The simulation time was extremely long due to the complexity of the circuitry being simulated. Most simulation traces took one and a half hours even on an above average computer. The processor used for the simulation was a pentium III 450MHz. These simulation traces generated data files that were as big as 250 megabytes per trace. This caused a huge strain on the computer used for simulation.

1.3.2 Limitations on the hardware and software

The first design used an INTEL microcontroller with PWM generator. It was found that this microcontroller was too slow to cope with the mathematical complexity of the drive operation. The second design used a Motorolla DSP. This DSP was fast enough but it lacked the necessary timers for the generation of the variable frequency. It was also found that the Motorola DSP could only be programmed using ASSEMBLER language. This was undesirable because software development was slow using Assembler. The final design used a Texas Instruments F240 DSP. It was found that this board satisfied all the

hardware and software requirements of the project. This DSP could be programmed using a C compiler.

1.4 SCOPE OF THE THESIS AND PLAN OF DEVELOPMENT

The thesis begins by describing the development of variable speed drive topologies from the conventional topology to the modern day topologies. It then proposes the new topology for a single to three-phase variable speed drive. The topology is analyzed and the mathematical equations associated with the topology are derived and discussed.
The drive is simulated using the package Orcad 9. The simulation is done in two sections. Firstly the front-end rectifier is simulated and then the full system is simulated. The hardware and software implementation is then described. The experimental results obtained are discussed and conclusions and recommendations are made.

CHAPTER 2
LITERATURE REVIEW

This chapter outlines the developments in the topologies for single to three phase variable speed drives.

2.1 THE CONVENTIONAL TOPOLOGY

A conventional single-phase to three-phase topology, employs an input rectifier and smoothing capacitor to generate a DC voltage. Six switches are then driven by PWM to produce three phase power. This topology has a poor input current quality. Methods to shape the input current waveform include the addition of a boost convertor and a blocking diode shown in figure [2.1] Other topologies use resonant circuits to shape the input current and can be seen in figures [2.2 and 2.3]. Although the harmonic current requirements of the converter are improved, the additional semiconductors add to the overall cost and power losses of the convertor. These convertors do not allow regenerative braking since the power flow is unidirectional. N Mohan, T Underland, W.P Robins[1].

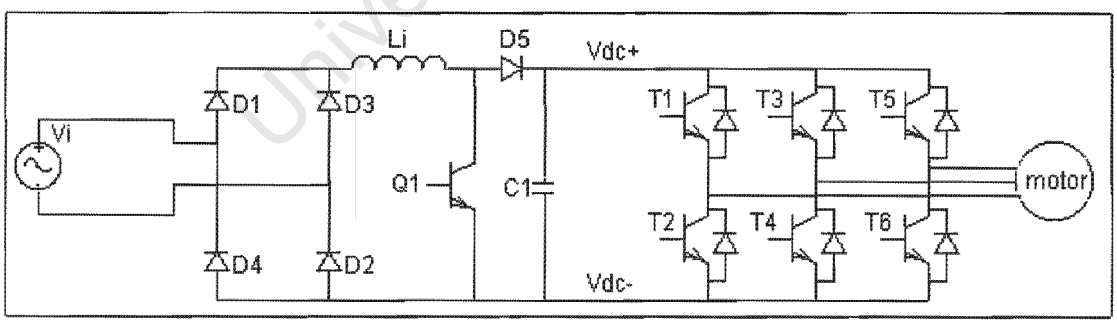


Figure 2.1 A convetional single to three phase variable speed drive with input current shaping.

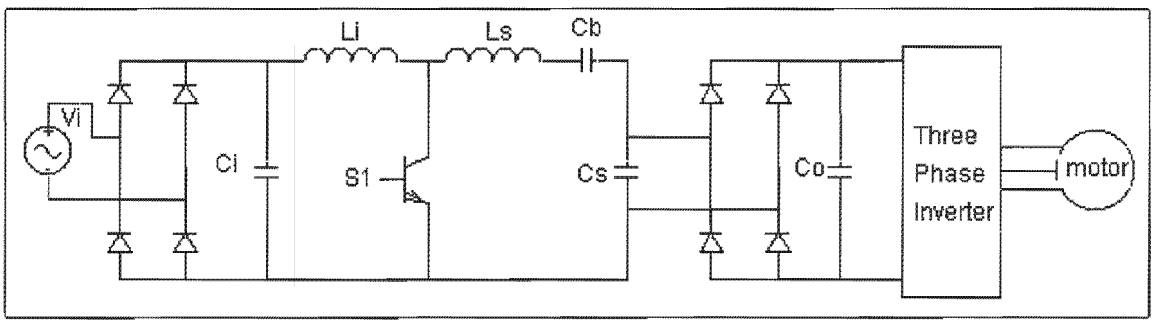


Figure 2.2 Class E type resonant circuit topology

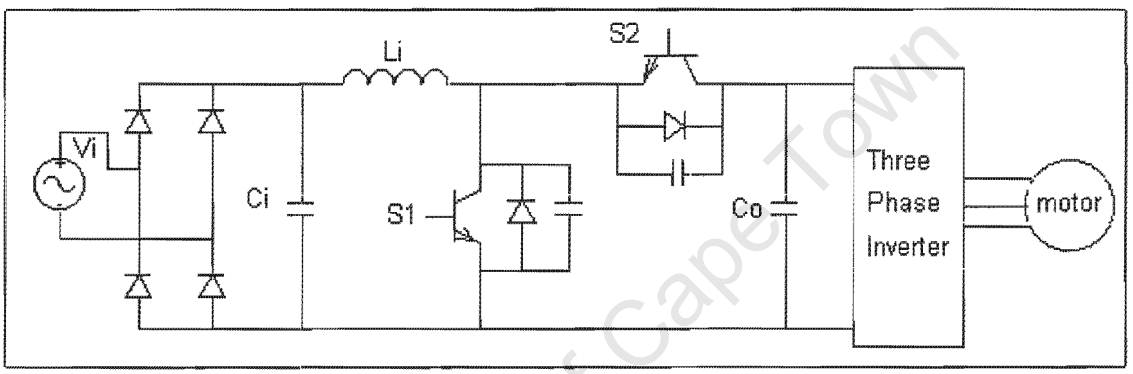


Figure 2.3 A Zero-voltage switching type resonant circuit topology

Recent topologies have suggested many improvements to the conventional converter. These improvements include:

- Sinusoidal currents being drawn from the supply.
- Operation at unity power factor.
- A high quality Three Phase output being supplied to the load.
- Performance immunity to noise in the mains supply

2.2 THE IMPROVED CONVERTOR BY ENJETI AND RAHMAN

In the topology proposed by P.N.Enjeti and A.Rahman, figure [2.4], the conventional diode bridge rectifier is replaced by employing two switches and two capacitors. This enables bi-directional power flow between the DC link and the AC source. The proposed topology employs only six power switches to provide single-phase to three-phase power conversion. P.N. Enjeti and A Rahman(1)

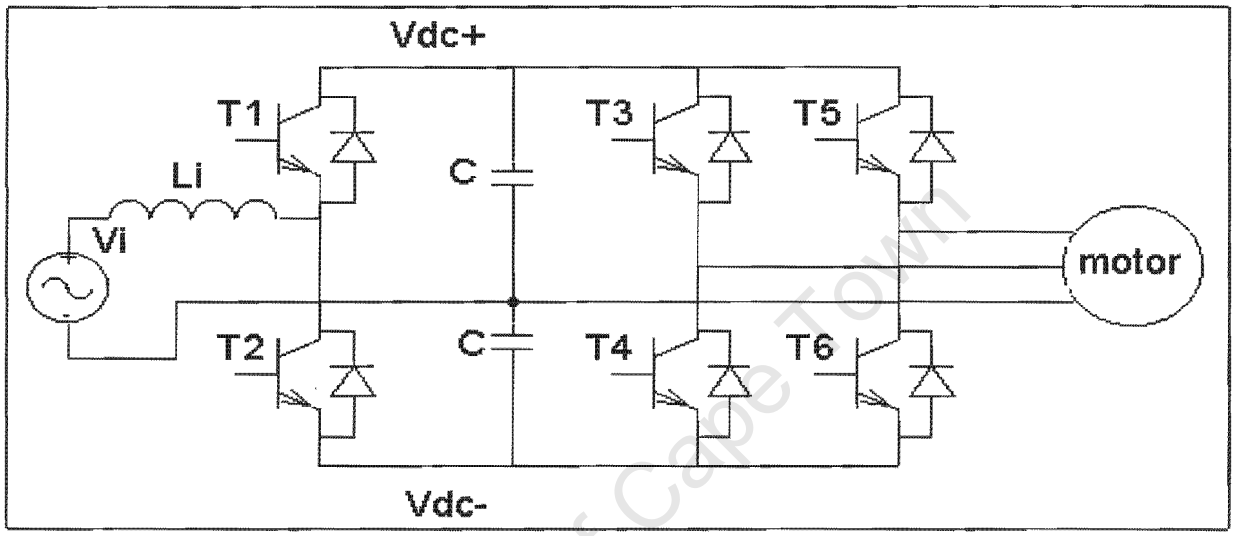


Figure 2.4 The topology by Enjeti and Rahman

This topology has a switching current shaping front-end rectifier and split capacitor system. In Enjeti's topology, the neutral of the supply is used as one of the three phases at the output of the converter. The second and third phases are produced by asymmetrical PWM (APWM). The neutral of the supply is connected to the centre of the capacitors. The first leg or active rectifier only charges up the DC bus and forms part of a boost convertor. This rectifier is able to shape the current drawn from the supply.

The converter has the following improvements over the conventional topology:

- Active input current shaping for sinusoidal input currents.
- Bi-directional flow of power
- Close to unity power factor operation
- Reduced number of power electronic devices implies that it is cheaper

CHAPTER 3

ANALYSIS OF THE PROPOSED TOPOLOGY

The analysis of the proposed topology was based on the theory discussed in "*Theory of operation of a static VAR Generator* ",M Malengret, University of Cape Town.

The 3-phase convertor can be divided into two sections with their own specific functions. The first leg of the convertor front has a dual function. It serves as an active rectifier that shapes the input current so that nearly sinusoidal currents are drawn from the supply. It also serves as a phase regulator for the first leg of the convertor. The second and third legs of the convertor form a four-switch inverter that produces a variable voltage and frequency across a three-phase load connected to the convertor.

The variable speed drive is shown in figure 3.1. V represents the sinusoidal source. L represents the inductance. N represents the neutral. E represents the PWM voltage with respect to neutral at the midpoint of the first leg. F represents the PWM voltage with respect to neutral at the midpoint of the second leg. G represents the PWM voltage with respect to neutral at the midpoint of the third leg.

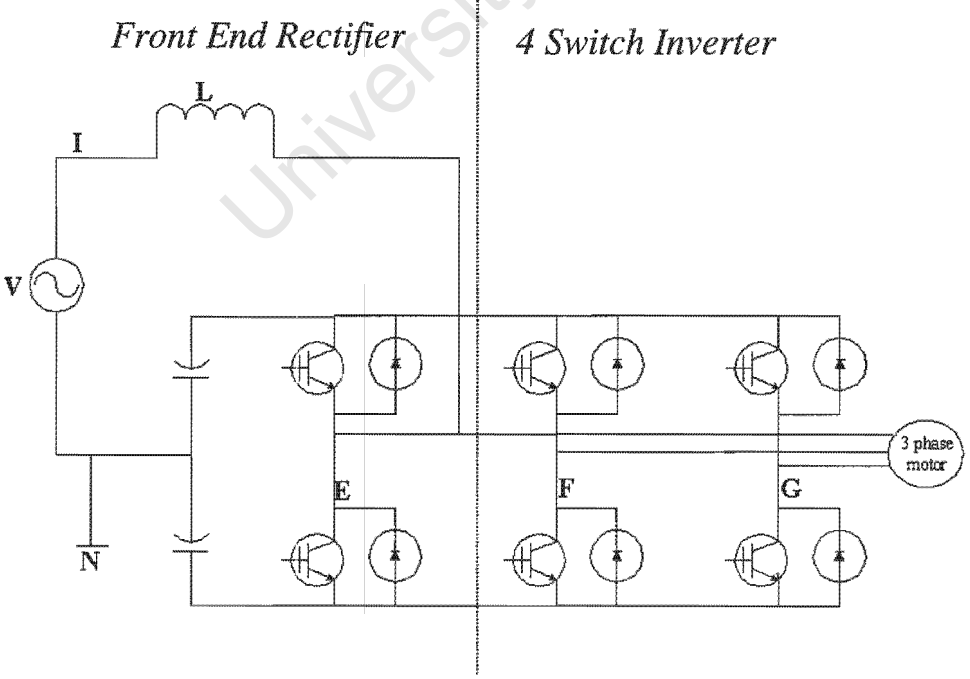


Figure 3.1 New proposed Single to Three Phase Variable Speed Drive

3.1 THE FRONT END RECTIFIER / PHASE REGULATOR

A simplified representation of the front end rectifier is shown in figure (3.3) The diagram represents a sinusoidal AC voltage source, an inductance and shows the voltage **E** which is the midpoint of the first leg of the convertor. Note that voltage **E** is in fact PWM and is not purely sinusoidal as the voltage source. The rectifier produces $\mathbf{E_1}$, the fundamental of **E**, at a phase shift of δ with respect to the voltage source V. The frequency of $\mathbf{E_1}$ is the same as the voltage source.

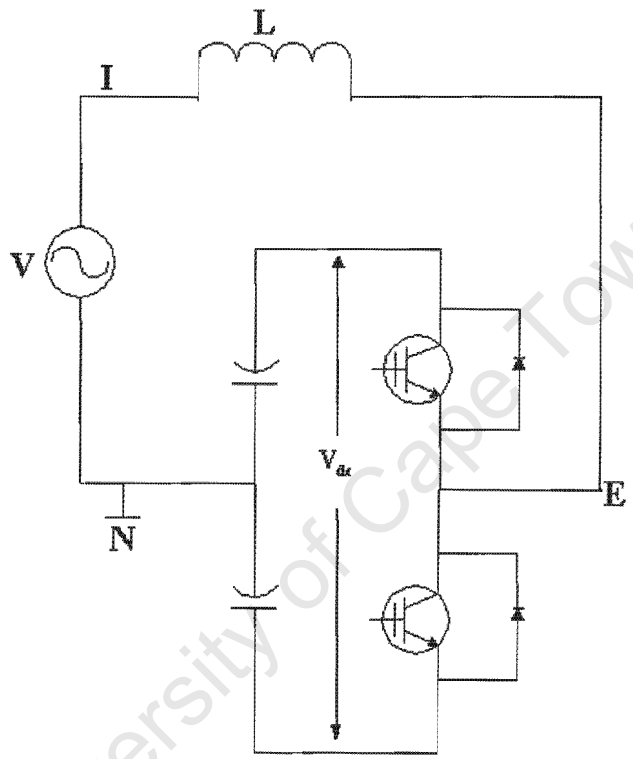


Figure 3.2 The Front End Rectifier

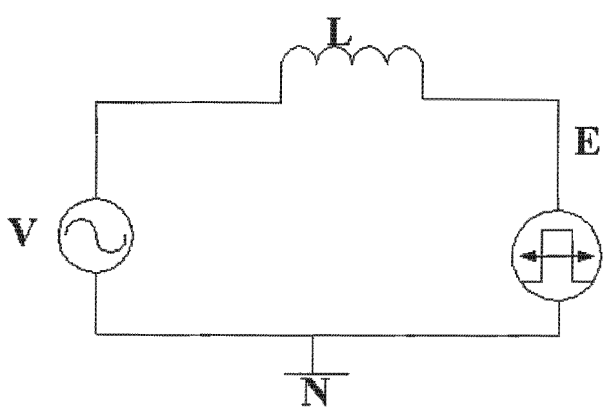


Figure 3.3 A simplified representation of the front end rectifier.

The operation of the front end rectifier is explained with reference to the following phasor diagram of figure (3.4)

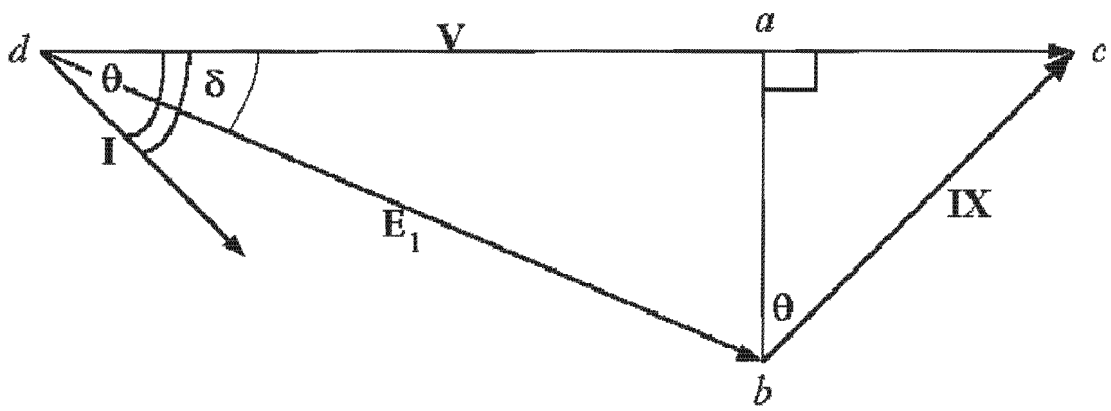


Figure 3.4 Phasor Representation of the front-end rectifier

From the above figure 3.4,

V represents the sinusoidal voltage phasor at the source.

I represents the current phasor drawn from the supply.

$\mathbf{E_1}$ represents fundamental of the PWM seen at the midpoint of the rectifier.

θ represents the angle between the source voltage **V** and current **I**.

δ represents the phase shift between voltages **V** and $\mathbf{E_1}$

IX represents the voltage phasor across the inductance.

3.1.1 DERIVATION FOR THE POWER DRAWN FROM THE SUPPLY

Referring to the phasor diagram of figure 3.4

$$|ab| = IXCos(\theta)$$

but

$$|ab| = E_1 Sin(\delta)$$

Therefore,

$$IXCos(\phi) = E_1 Sin(\delta)$$

$$I = \frac{E_1 Sin(\delta)}{XCos(\theta)} \qquad (1)$$

By definition the real power entering at the source, P_{in} is derived as follows

$$P_{in} = VICos(\theta)$$

therefore

$$I = \frac{P_{in}}{VCos\theta} \qquad (2)$$

By equating equations (1 and 2)

$$\frac{E_1 Sin(\delta)}{XCos(\theta)} = \frac{P_{in}}{V\cos(\theta)}$$

Simplifying and making P_{in} the subject of the formula

$$P_{in} = \frac{VE_1 Sin(\delta)}{X} \qquad (3)$$

$$P_{ave} = \frac{VE_1 Sin(\delta)}{\sqrt{2}X}$$

Since $Sin(\delta)$ can vary between 1 and –1, it can be shown that the power drawn from the source can be either positive or negative depending on the value of δ. The power is therefore bi-directional.

3.1.2 DERIVATION FOR THE POWER FACTOR ANGLE IN TERMS OF P_{IN}, V, E_1 AND X

Referring to the phasor diagram figure (3.4),

$$Tan(\theta) = \frac{V - ECos(\delta)}{E_1 Sin(\delta)}$$

$$\therefore Tan(\theta) = \left[\frac{V - ECos(\delta)}{E_1 Sin(\delta)}\right]$$

Noting that $Cos(\delta) = \sqrt{1 - Sin^2(\delta)}$

$$Tan(\theta) = \left[\frac{V - E_1\sqrt{1 - Sin^2(\delta)}}{E_1 Sin(\delta)}\right]$$

Now from equation (3)

$$P_{in} = \frac{VESin(\delta)}{X}$$

$$Sin(\delta) = \frac{P_{in}X}{VE_1}$$

Substituting into equation (5)

$$Tan(\theta) = \left[\frac{V - E_1\sqrt{1 - \frac{P_{in}^2 X^2}{V^2 E_1^2}}}{\frac{P_{in}X}{V}}\right]$$

$$Tan(\theta) = \left[\frac{V^2 - VE_1 \sqrt{\frac{V^2 E_1^2 - P_{in}^2 X^2}{V^2 E_1^2}}}{P_{in}X} \right]$$

$$\theta = Arc\tan\left[\frac{V^2 - \sqrt{V^2 E_1^2 - P_{in}^2 X^2}}{P_{in}X} \right] \qquad (4)$$

3.1.3 DERIVATION FOR THE POWER FACTOR IN TERMS OF P_{IN}, V, E_1 AND X

$$pf = Cos(\theta)$$

referring to the phasor diagram of figure (3.4)

$$pf = \frac{ab}{cb}$$

$$ab = E_1 Sin(\delta)$$

Using the cosine rule,

$$cb = \sqrt{V^2 + E_1^2 - 2VE_1 Cos(\delta)}$$

$$pf = \frac{E_1 Sin(\delta)}{\sqrt{V^2 + E_1^2 - 2VE_1 Cos(\delta)}}$$

from equation (3), $Sin(\delta) = \frac{P_{in}X}{VE_1}$

$$pf = \frac{E_1 \frac{P_{in}X}{VE_1}}{\sqrt{V^2 + E_1^{\ 2} - 2VE_1 Cos(\delta)}}$$

$$pf = \frac{\frac{P_{in}X}{V}}{\sqrt{V^2 + E_1^{\ 2} - 2VE_1 Cos(\delta)}}$$

$$pf = \frac{\frac{P_{in}X}{V}}{\sqrt{V^2 + E_1^{\ 2} - VE_1 Cos(\delta)}}$$

$$pf = \frac{P_{in}X}{V\sqrt{V^2 + E_1^{\ 2} - VE_1 Cos(\delta)}}$$

Noting that $Cos(\delta) = \sqrt{1 - Sin^{\ 2}(\delta)}$

$$pf = \frac{P_{in}X}{V\sqrt{V^2 + E_1^{\ 2} - 2VE_1\sqrt{1 - Sin^{\ 2}(\delta)}}}$$

from equation (3), $Sin(\delta) = \frac{P_{in}X}{VE_1}$

$$pf = \frac{P_{in}X}{V\sqrt{V^2 + E_1^{\ 2} - 2VE_1\sqrt{1 - \frac{P^2{}_{in}X^2}{V^2E_1^{\ 2}}}}}$$

$$pf = \frac{P_{in}X}{V\sqrt{V^2 + E_1^{\ 2} - 2\sqrt{VE - P^2{}_{in}X^2}}} \qquad (5)$$

3.1.4 DERIVATION FOR THE DC BUS VOLTAGE AT UNITY POWER FACTOR

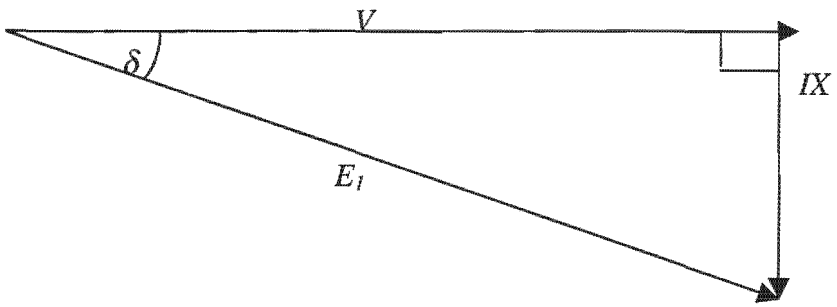


Figure 3.5 Phasor diagram of the front end rectifier at unity power factor

From figure 3.5,

$$E_1^{\,2} = V^2 + I^2X^2$$

$$E_1^{\,2} = \frac{1}{2}maV_d$$

$$\frac{1}{4}ma^2V_d^{\,2} = V^2 + I^2X^2$$

$$V_d^{\,2} = \frac{4}{ma^2}(V^2 + I^2X^2)$$

$$V_d = \frac{2}{ma^2}\sqrt{(V^2 + I^2X^2)} \qquad (6)$$

from equation 3, $Sin(\delta) = \frac{IX}{E_1}$

$$Sin(\delta) = \frac{IX}{\frac{1}{2}maV_d}$$

$$Sin(\delta) = \frac{2IX}{maV_d}$$

$IX = \frac{maV_dSin(\delta)}{2}$ substituting into equation 6,

$$V_d = \frac{2}{ma}\sqrt{V^2 + \frac{ma^2 Sin^2(\delta)}{4}}$$

$$\frac{maV_d}{2} = \sqrt{V^2 + \frac{ma^2 Sin^2(\delta)}{4}}$$

$$\frac{ma^2 V_d^{\,2}}{4} = V^2 \frac{ma^2 Sin^2(\delta)}{4}$$

$$\frac{ma^2 V_d^{\,2}}{4} - \frac{ma^2 Sin^2(\delta)}{4} = V^2$$

$$\frac{ma^2 Vd^2}{4}(1 - Sin^2(\delta)) = V^2$$

$$\frac{ma^2 V_d^{\,2}}{4}\ Cos^2(\delta) = V^2$$

$$V_d^{\,2} = \frac{4V^2}{ma^2 Cos^2(\delta)}$$

$$V_d = \frac{2V}{ma\ Cos(\delta)} \qquad (7)$$

$$V_d = \frac{2}{ma} VSec(\delta)$$

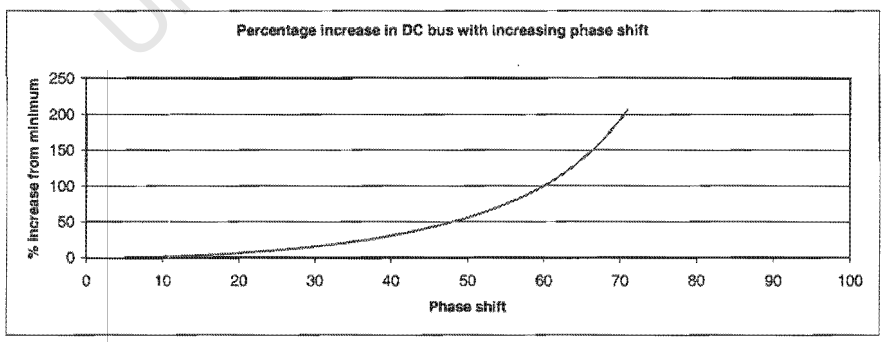


Figure 3.6 Percentage rise in DC bus with increasing phase shift δ

Figure 3.6 Shows the percentage rise in DC bus voltage from the minimum when δ is equal to zero to a phase shift of about 70^0. If the DC bus is to kept as low as possible then the phase shift δ should be limited to small values.

3.1.5 DERIVATION FOR THE OUTPUT POWER IN TERMS OF δ

For power balance, the average input power, P_{ave} , must be equal P_{out}.

$$P_{ave} = \frac{VE_1 Sin(\delta)}{\sqrt{2}X} = P_{out}$$

$$Sin(\delta) = \frac{\sqrt{2}XP_{out}}{VE_1}$$

where $E_1 = \frac{1}{2} maV_d$

$$Sin(\delta) = \frac{\sqrt{2}XP_{out}}{V\frac{1}{2}maV_d}$$

where $X = 2\pi FL$

$$Sin(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V\frac{1}{2}M_aV_d}$$

$$Sin(\delta) = \frac{4\sqrt{2}\pi FLP_{out}}{VmaV_d}$$

from equation 7, at unity power factor, $V_d = \frac{2}{ma} V \frac{1}{Cos(\delta)}$

$$Sin(\delta) = \frac{4\sqrt{2}\pi FLP_{out}}{Vma\frac{2}{ma}V\frac{1}{Cos(\delta)}}$$

$$Sin(\delta) = \frac{2\sqrt{2}\pi FLP_{out}Cos(\delta)}{V^2}$$

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2} \qquad (8)$$

3.2 THE FOUR SWITCH INVERTER

The purpose of the four switch inverter is to produce a variable voltage and frequency across the three phase load. This is achieved by reproducing voltage E and adding a varying frequency component on each of the two legs. The varying frequency should be generated in such a manner so that the line to line voltage seen by the load is only the variable frequency. The inverter is shown in figure (3.7)

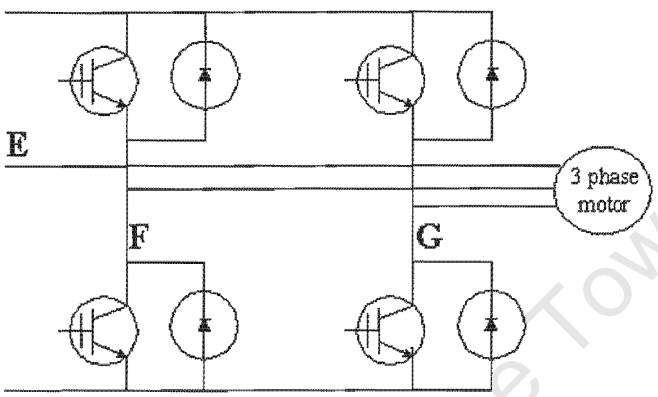


Figure 3.7 The four switch inverter.

From figure 3.7,

E represents the line to neutral voltage at the midpoint of the first leg.

F represents the line to neutral voltage at the midpoint of the second leg.

G represents the line to neutral voltage at the midpoint of the third leg

The voltage **E** is a PWM waveform containing only the fundamental, E_1, and the carrier. The frequency of E_1 is the same as that of the voltage source. E_1 is phase shifted with respect to the voltage source to control the power flowing through the convertor. The modulation index used in the first leg, ma_1, is kept constant.

The voltage **F** is a PWM waveform that contains 2 fundamental frequencies, F_1 and F_2, as well as the carrier. The fundamental F_1 is an exact copy of E_1. The fundamental F_2 represents the fundamental of the variable frequency. The frequency of F_2 varies between 0 and 50Hz. The amplitude of F_2 is controlled by the modulation index ma_2. Ma_2 is adjusted so that a constant volt per frequency ratio is obtained. When looking at the fundamentals of the line to line voltages across **E** and **F**, the line to neutral voltages need to be subtracted. The fundamental of **E** with respect to neutral is E_1.

The fundamentals of **F** with respect to neutral are F_1 and F_2. Knowing that E_1 is equal to F_1, the resulting fundamental in the line to line voltage is only F_2, the variable frequency, since the fixed frequencies cancel out.

The voltage **G** is a PWM waveform that contains 2 fundamental frequencies, G_1 and G_2, as well as the carrier. The fundamental G_1 is an exact copy of E_1. The fundamental G_2 represents the fundamental of the variable frequency. The fundamental G_2 is phase shifted by 60^0 with respect to F_2. The frequency of G_2 is the same as the frequency of F_2 . The amplitude of G_2 is controlled by the modulation index ma_2. When looking at the fundamentals of the line to line voltages across F and G, the line to neutral voltages need to be subtracted. The fundamentals of F with respect to neutral are F_1 and F_2 .The fundamentals of G with respect to neutral are G_1 and G_2. Knowing that F_1 is equal to G_1, the resulting fundamental in the line to line voltage is F_2 - G_2. This is a variable frequency, since the fixed frequencies cancel out.

3.2.1 GENERATION OF THE PHASE VOLTAGES.

The following notation is used for the referencing of the voltages.

0 refers to the neutral.

1 refers to the midpoint of the first leg.

2 refers to the midpoint of the second leg.

3 refers to the midpoint of the third leg.

3.2.1.1 THE LINE TO NEUTRAL VOLTAGE AT THE MIDPOINT OF THE FIRST LEG

The fundamental in line to neutral voltage at the midpoint of the first leg can be described by equation 9.

$$E_{10} = \sqrt{2}E_1 Sin(\varpi_1 t + \delta) \qquad (9)$$

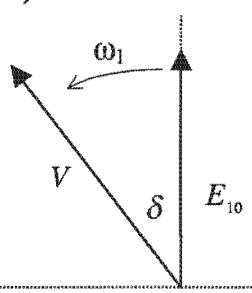


Figure 3.8 Phasor diagram of E_1 showing the phase shift δ

3.2.1.2 THE LINE TO NEUTRAL VOLTAGE AT THE MIDPOINT OF THE SECOND LEG

The fundamental in line to neutral voltage at the midpoint of the second leg can be described by equation (10).

$$F_{20} = \sqrt{2}E_1 Sin(\omega_1 t + \delta) + \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}F_2 Sin(\omega_2 t) \qquad (10)$$

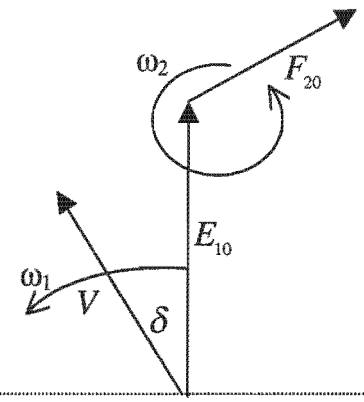


Figure 3.9 Phasor diagram of the line to neutral voltage at the midpoint of the second leg.

3.2.1.3 THE LINE TO NEUTRAL VOLTAGE AT THE MIDPOINT OF THE THIRD LEG

The fundamental in line to neutral voltage at the midpoint of the third leg can be described by equation 11.

$$G_{30} = \sqrt{2}E_1 Sin(\omega_1 t + \delta) + \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}G_2 Sin\left(\omega_2 t + \frac{\pi}{3}\right) \qquad (11)$$

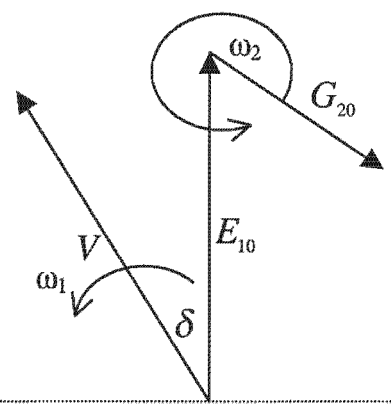


Figure 3.10 Phasor diagram of the line to neutral voltage at the midpoint of the third leg.

The following phasor diagram can therefore represent the complete convertor.

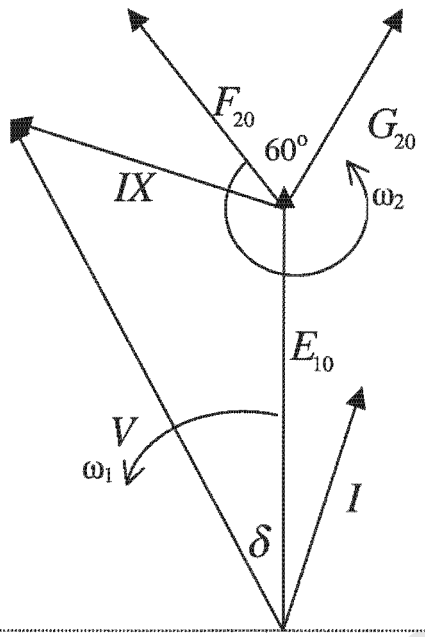


Figure 3.11 Phasor diagram of the line to neutral voltages for the complete convertor.

3.2.2 GENERATION OF THE LINE TO LINE VOLTAGES

The line to line voltages can be derived by subtracting the following line to neutral voltages.

$$E_{10} = \sqrt{2}E_1 Sin(\omega_1 t + \delta)$$

$$F_{20} = \sqrt{2}E_1 Sin(\omega_1 t + \delta) + \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}F_2 Sin(\omega_2 t)$$

$$G_{30} = \sqrt{2}E_1 Sin(\omega_1 t + \delta) + \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}G_2 Sin\left(\omega_2 t + \frac{\pi}{3}\right)$$

$$V_{phase1} = E_{10} - F_{20} = -\left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}F_2 Sin(\omega_2 t) \quad (12)$$

$$V_{phase2} = F_{20} - G_{30} = \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}F_2 Sin\left(\omega_2 t - \frac{\pi}{3}\right) \quad (13)$$

by definition G_2 is equal to F_2

$$V_{phase3} = G_{30} - E_{10} = \left(\frac{\omega_2}{\omega_1}\right)\sqrt{2}F_2 Sin\left(\omega_2 t + \frac{\pi}{3}\right) \quad (14)$$

This results in the following phasor diagram for the line to line voltages

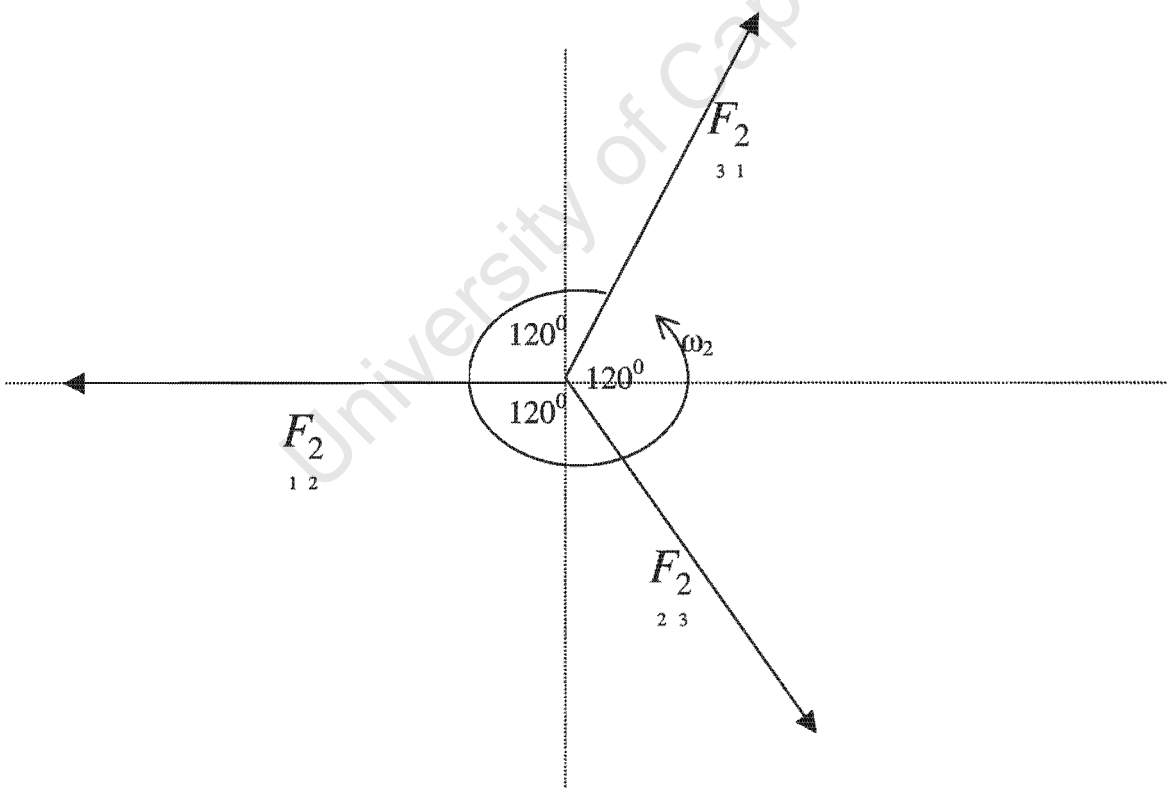


Figure 3.12 Phasor diagram for the line to line voltages

Figure 3.12 shows that a balanced three phase line to line voltage is obtained from the unbalanced line to neutral voltages.

CHAPTER 4

COMPUTER SIMULATION

The circuit was simulated using the software package Orcad version 9.

The simulation was done in two sections. The first examines the operation of the front end rectifier and the second examines the whole system. This simulation investigates the possibility of controlling the DC bus voltage by phase shifting techniques. Observations for unity power operation are made and conclusions are drawn.

4.1 THE FRONT END RECTIFIER

The first aim of this simulation is to investigate the effect that the angle δ has on the DC bus voltage. The phase shift angle, δ, is the phase difference between the voltage source and the fundamental of the line to neutral voltage at the midpoint of the first leg of the convertor. A simple system is set up using a 1000W load, 400V DC bus and an AC source voltage of 100V RMS. The 400V DC bus was chosen to examine the step-up ability of the convertor. A resistive load of 160Ω was calculated and this was kept constant. The strategy is to keep the load resistance constant and vary the phase shift δ to see if we can control the DC Bus. A DC bus of 400V will correspond to an output power of 1000W. Once this is achieved different inductances are used to observe the effects on input current, power factor and phase shift δ.

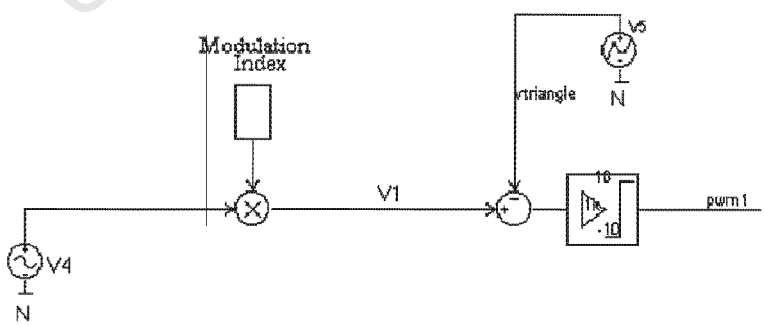


Figure 4.1 The schematic diagram for the control signal generator of the front end rectifier.

In figure 4.1, V4 represents a reference sinusoid that is scaled by a constant to produce V1.The phase of V4 can be adjusted to be leading or lagging the mains source voltage by manually setting the attributes of V4 in the simulator. V1 is in phase with V4. V1 is compared to a triangular waveform,V5, and the result is limited to +10V and -10V. The result is indicated by the label pwm1. This PWM signal is used to control the switches of the first leg of the convertor. This can be seen from figure 4.3.

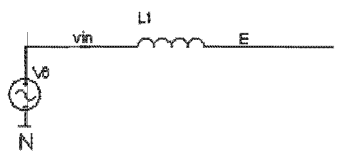


Figure 4.2 The schematic diagram for the voltage source and input inductance.

In figure 4.2, V6 represents the mains source voltage. The output of the inductance, L1, is connected to the centre point of the first leg of the convertor as shown in figure 4.3. The voltage at the centre point is labelled E. The label N shows the neutral of the system.

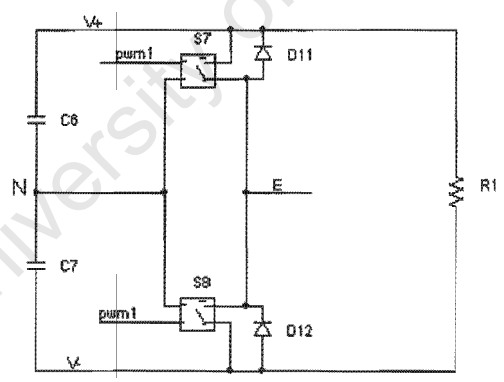


Figure 4.3 A schematic diagram of the front-end rectifier.

In figure 4.3, the capacitors C6 and C7 form the spilt capacitor bank. The switches S7, S8 and diodes D11 and D12 form the first leg of the convertor. The PWM1 control signal generated in figure 4.1 is used to control the switches S7 and S8. The midpoint of the capacitors is connected to the neutral, N. R1 is the load connected across the DC bus.

4.1.1 SIMULATION OF THE DC LINK REGULATION BY PHASE SHIFTING

For the simulation traces in this section, the following symbols are used :

V(VIN) represents the sinusoidal source voltage referenced to the neutral.

I(L1) represents the current drawn from the source.

$V(V^+,V^-)$ represents the voltage across the DC bus.

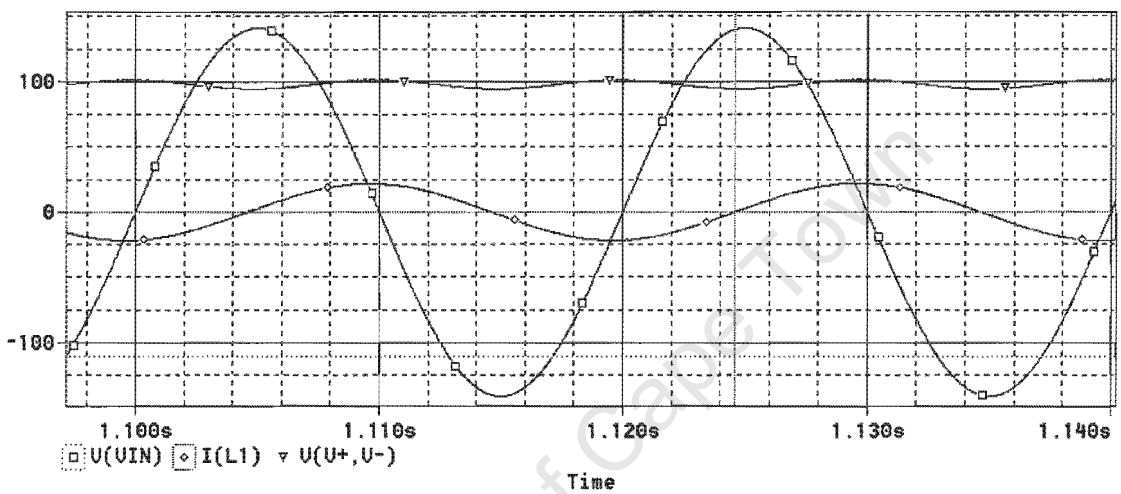


Figure 4.4 Transient plot for L=15mH and δ=0.

From figure 4.4 the following is observed:

Imax = 22A

DC bus = 100 V

Phase difference between input voltage and current = 4.6ms lagging.

Power factor angle $\theta = 82.8^0$

Power factor = 0.125 lagging

It is clear that the desired DC bus voltage of 400V DC has not been obtained. A poor power factor of 0.125 lagging was obtained and this is undesirable. The next step is to increase the phase shift, δ, to see if the DC bus voltage of 400V can be achieved.

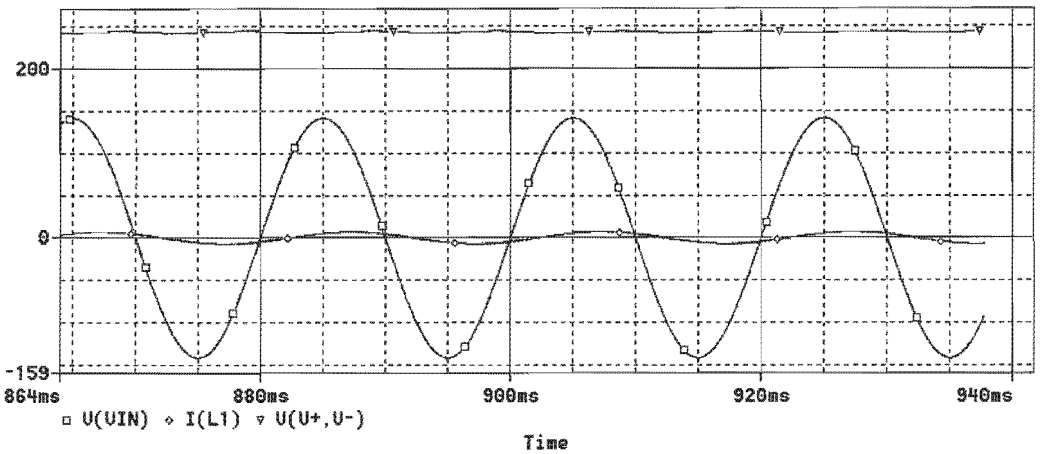


Figure 4.5 Transient plot for L=15mH and $\delta=10^0$

From figure 4.5 the following is observed:
Imax = 7A
DC bus = 242 V
Phase difference between input voltage and current = 2.4ms lagging.
Power factor angle $\theta = 43.2^0$
Power factor = 0.73 lagging
We can see that the 10^0 increase of δ has increased the DC bus voltage from 100V to 242V. The power factor has improved from 0.125 lagging to 0.73 lagging.

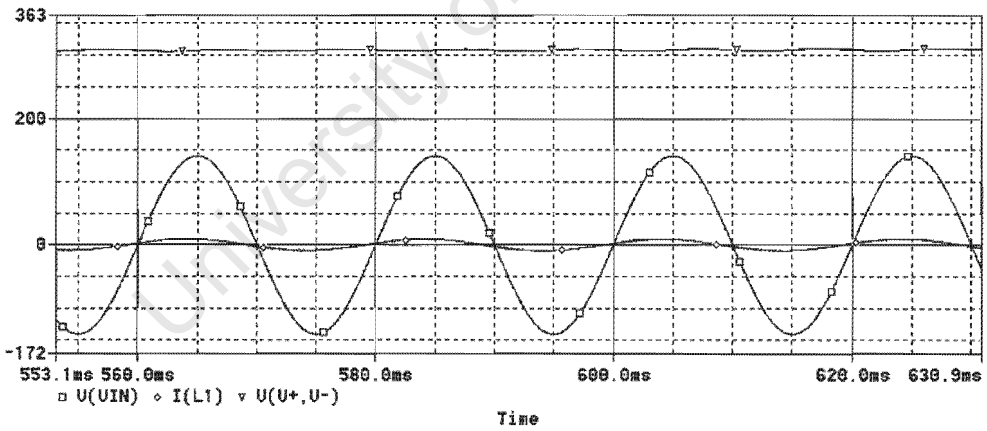


Figure 4.6 Transient plot for L=15mH and $\delta=15^0$

From figure 4.6 the following is observed:
Imax = 9A
DC bus = 307 V
Phase difference between input voltage and current = 0.7ms leading.
Power factor angle $\theta = 12.6^0$
Power factor = 0.98 leading
A further increase of 5^0 in δ has increased the DC bus voltage to 307V. The power factor has increased from 0.73 lagging to 0.98 leading. Although this is an excellent power factor the desired DC bus voltage has still not been achieved.

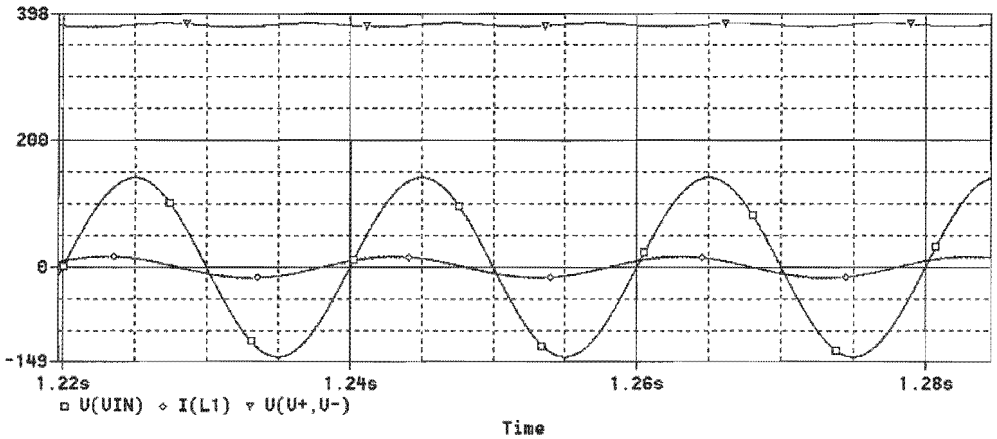


Figure 4.7 Transient plot for L=15mH and $\delta=20^0$

From figure 4.7 the following is observed:
Imax = 17A
DC bus = 380 V
Phase difference between input voltage and current = 2.1ms leading.
Power factor angle $\theta = 37.8^0$
Power factor = 0.79 leading
Increasing δ a further 5^0 has increased the DC bus to 380V. The power factor has dropped to 0.79 leading. This drop in power factor is undesirable.

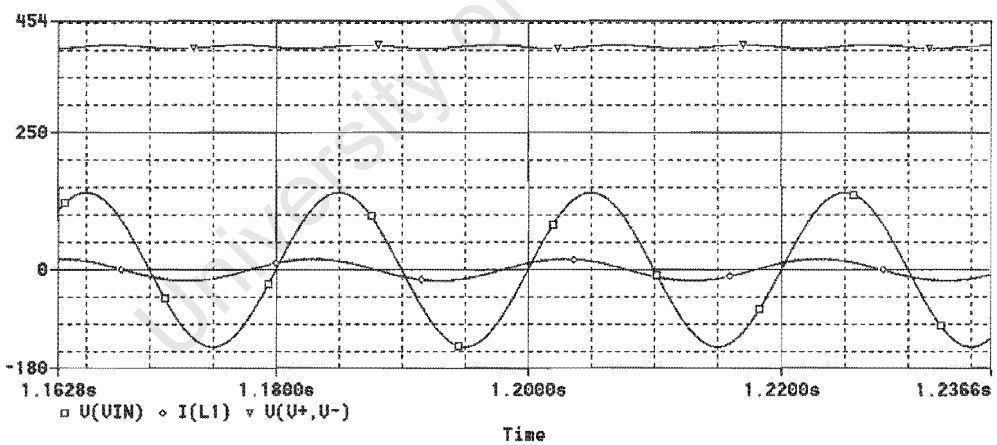


Figure 4.8 Transient plot for L=15mH and $\delta=22^0$

From figure 4.8 the following is observed:
Imax = 20A
DC bus = 405 V
Phase difference between input voltage and current = 2.2ms leading.
Power factor angle $\theta = 39.6^0$
Power factor = 0.77 leading
A DC bus voltage of 405V has been achieved and this is close to the desired voltage of 400V DC. A phase shift of 22^0 is needed if a 15mH inductor is used. We have therefore proven that the DC bus voltage can be controlled by phase shifting.

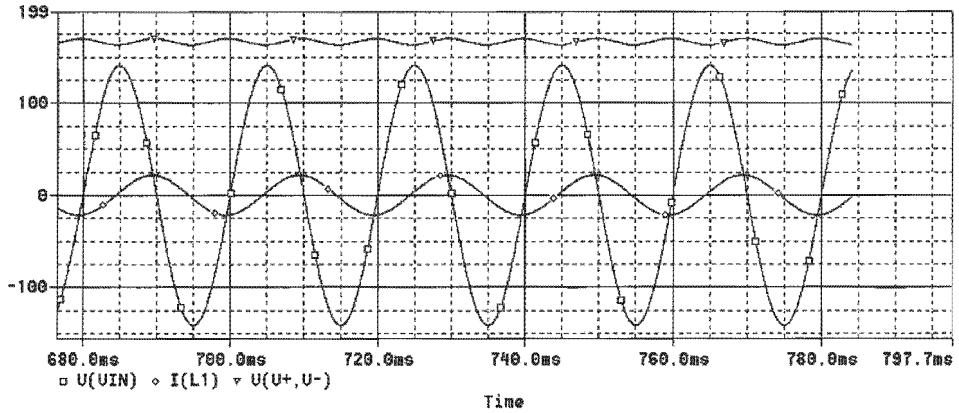


Figure 4.9 Transient plot for L=10mH and $\delta=0^0$

From figure 4.9 the following is observed:
Imax = 22A
DC bus = 166 V
Phase difference between input voltage and current = 4.4ms lagging.
Power factor angle $\theta = 79.2^0$
Power factor = 0.19 lagging
The inductance has been decrease to 10mH. At $\delta=0$, the DC bus is 166V. This is higher than the previous case where the inductance was 15mH. (see figure 4.4). The power factor is 0.19 lagging and this is undesirable.

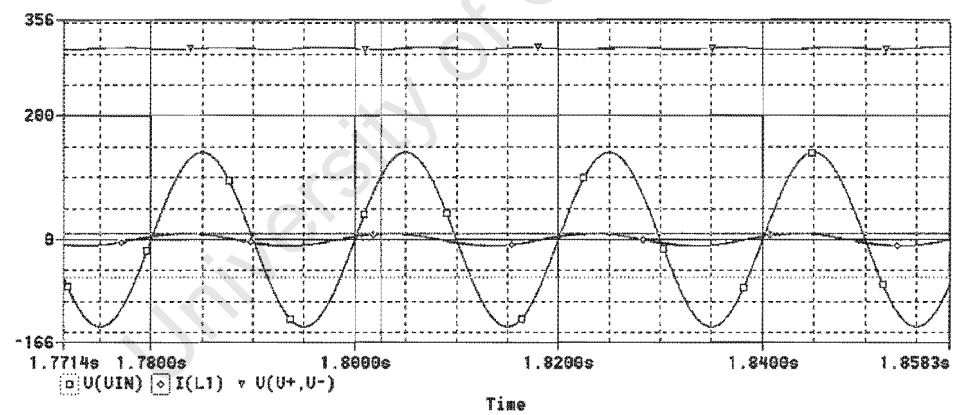


Figure 4.10 Transient plot for L=10mH and $\delta=10^0$

From figure 4.10 the following is observed:
Imax = 10A
DC bus = 277 V
Phase difference between input voltage and current = 1.1ms leading
Power factor angle $\theta = 19.8^0$
Power factor = 0.94 leading
The phase shift, δ, has been increased to 10^0 and the DC bus has increased from 166V DC to 277VDC. The power factor has increased from 0.19 lagging to 0.94 leading. It should be noted that the change from lagging to leading power factor needed a 15^0 shift when the inductance used was 15mH. (see figure 4.6)

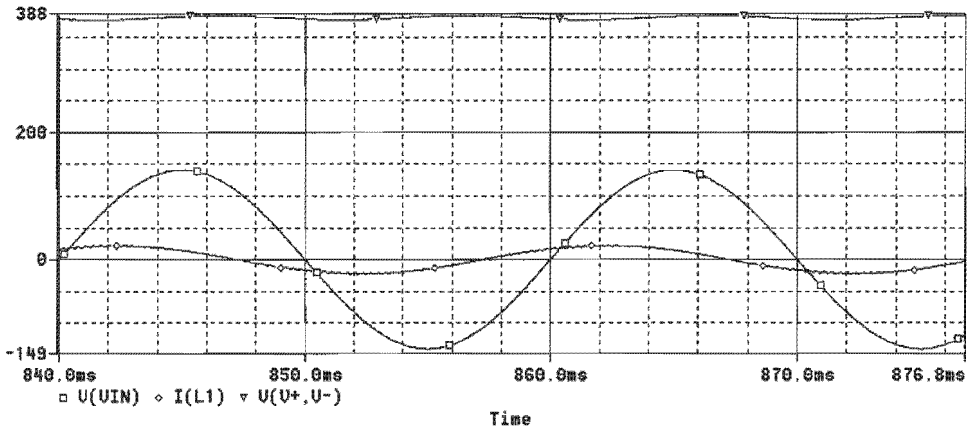


Figure 4.11 Transient plot for L=10mH and $\delta=15^0$

From figure 4.11 the following is observed:
Imax = 20A
DC bus = 381 V
Phase difference between input voltage and current = 2.73ms leading.
Power factor angle $\theta = 49.14^0$
Power factor = 0.65 leading
The phase shift, δ, has been increased to 15^0 and the DC bus voltage has consequently increased from 277V to 381V. The power factor has decreased to 0.65 leading.

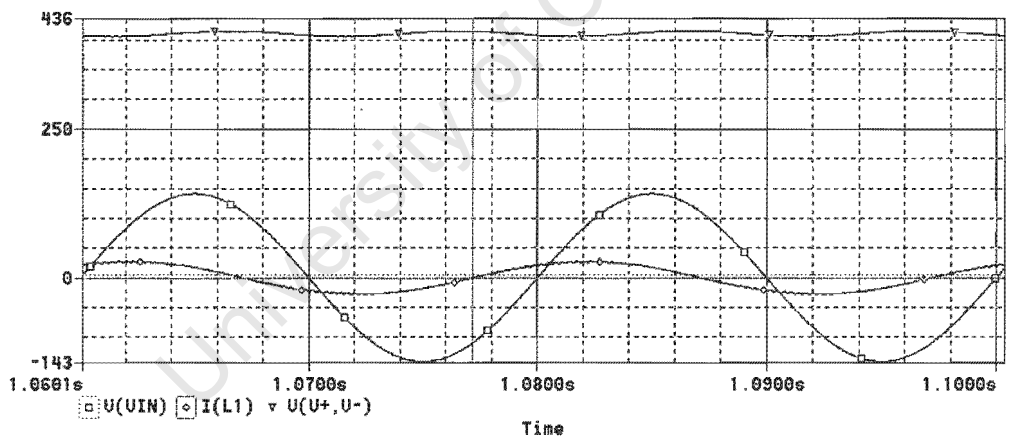


Figure 4.12 Transient plot for L=10mH and $\delta=17^0$

From figure 4.12 the following is observed:
Imax = 27A
DC bus = 411 V
Phase difference between input voltage and current = 2.8ms leading.
Power factor angle $\theta = 50.4^0$
Power factor = 0.64 leading
The required DC bus of about 411V has been achieved at a phase shift of 17^0. This is less phase shift than when an inductance of 15mH was used. (See figure 4.8)
The power factor is 0.64 leading at the desired DC bus voltage. This is not an improvement to the case when 15mH was used because a power factor of 0.77 leading was obtained. (See figure 4.8)

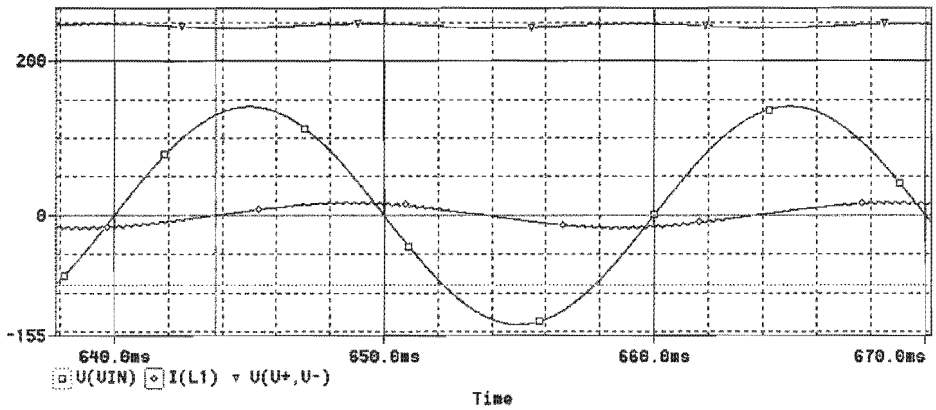


Figure 4.13 Transient plot for L=5mH and δ=0

From figure 4.13 the following is observed:
Imax = 17A
DC bus = 246 V
Phase difference between input voltage and current = 3.7ms lagging
Power factor angle $\theta = 66.6^0$
Power factor = 0.4 lagging
The inductance has been decrease to 5mH. At δ=0, the DC bus is 246V. This is higher than the previous case where the inductance was 10mH. (see figure 4.9). The power factor is 0.4 lagging and this is undesirable.

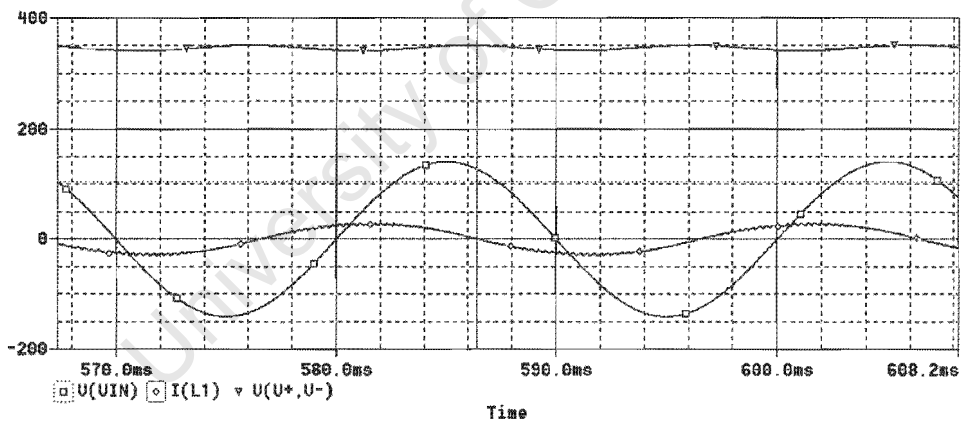


Figure 4.14 Transient plot for L=5mH and $\delta=10^0$

From figure 4.14 the following is observed:
Imax = 26A
DC bus = 346 V
Phase difference between input voltage and current = 3.65ms leading.
Power factor angle $\theta = 65.7^0$
Power factor = 0.41 leading
The phase shift, δ, has been increased to 10^0 and the DC bus has increased from 246V DC to 346VDC. The power factor has changed from 0.4 lagging to 0.41 leading. It should be noted that a small change in δ has brought about a large change in the power factor when compared to using 10mH and 15mH inductors (see figures 4.6 and 4.10)

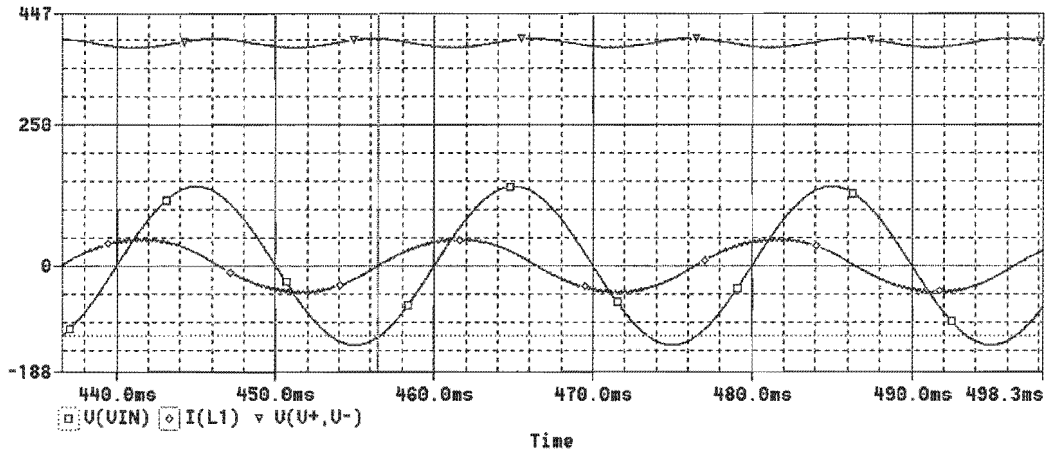


Figure 4.15 Transient plot for L=5mH and $\delta=15^0$

From figure 4.15 the following is observed:
Imax = 46A
DC bus = 402 V
Phase difference between input voltage and current = 4.0ms leading.
Power factor angle $\theta = 72^0$
Power factor = 0.31 leading

The required DC bus of about 402V has been achieved at a phase shift of 15^0. This is less phase shift than when inductances of 15mH and 10mH were used. (See figures 4.8 and 4.12) The power factor is 0.31 leading at the desired DC bus voltage. This is not an improvement to the case when 10mH was used. With an inductance of 10mH a power factor of 0.64 leading was obtained. (See figure 4.12) With an inductance of 15mH a power factor of 0.77 leading was obtained. (See figure 4.8).

It is clear that a smaller phase shift is required to obtain a desired DC bus voltage if a small inductance is used. We can also observe that a larger inductance will produce a better power factor for the same load.

4.1.2 SUMMARY OF RESULTS FOR DC LINK REGULATION USING PHASE SHIFTING

L=15mH

δ	Imax (A)	DC Bus Voltage (V)	Power Factor Angle θ	Power Factor
0	22	100	82.8	0.125 lagging
10^0	7	242	43.2	0.73 lagging
15^0	9	307	12.6	0.98 leading
20^0	17	380	37.8	0.79 leading
22^0	20	405	39.6	0.77 leading

L=10mH

δ	Imax (A)	DC Bus Voltage (V)	Power Factor Angle θ	Power Factor
0	22	166	79.2	0.187 lagging
10^0	10	309	30.6	0.86 leading
15^0	20	381	49.14	0.65 leading
17^0	27	411	50.4	0.637 leading

L=5mH

δ	Imax (A)	DC Bus Voltage (V)	Power Factor Angle θ	Power Factor
0	17	246	66.6	0.4 lagging
10^0	26	346	64	0.43 leading
15^0	46	402	72	0.31 leading

Table 1 Summary of the results for different inductances

4.1.3 OBSERVATIONS FROM RESULTS OF DC BUS REGULATION BY PHASE SHIFTING

From table [1], in all the above cases ie L=15mH, L=10mH and L=5mH we have started with a phase shift of 0 and then increased the phase shift until the required DC bus of 400V was achieved. At this DC bus voltage the output power is 1000W.

The following conclusions can be made:

- The DC bus can be controlled by varying the phase shift δ.
- The smaller the inductance the larger the input current needed to achieve the desired DC bus voltage.
- A large inductance results in a larger range of δ and smaller input current.
- A large inductance will give a better power factor at the required DC bus voltage.
- Unity power factor can only be obtained at a certain DC bus voltage.

The next step in the simulation was to find a method of controlling the and at the same time obtain a unity power factor.

4.1.4 UNITY POWER FACTOR OPERATION WITH MODULATION INDEX OF 1

In this section unity power factor operation is achieved using different inductances. Observations are made about the amount of phase shift needed as well as the value of the DC bus at unity power factor.

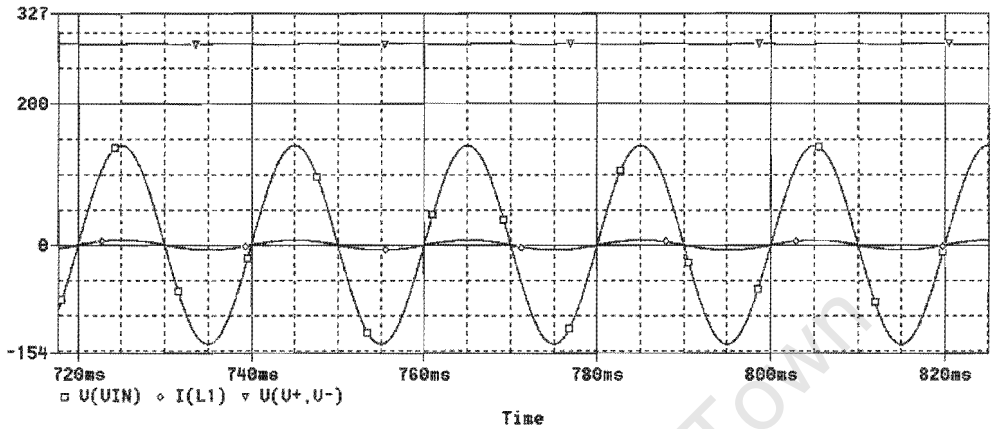


Figure 4.16 Transient plot showing unity power factor with L=15mH and $\delta=13^0$

From figure 4.16 the following is observed:
Imax = 7A
DC bus = 288 V
Phase difference between input voltage and current = 0
Power factor angle $\theta = 0$
Power factor = 1

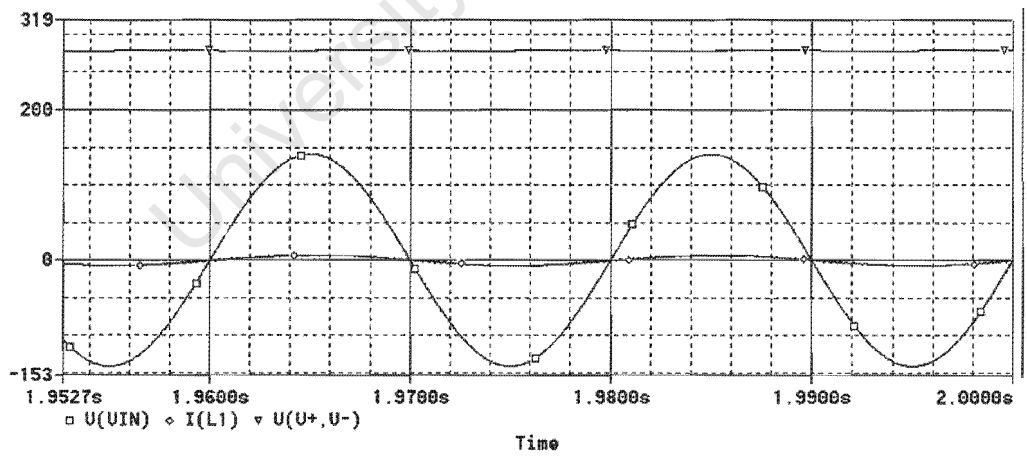


Figure 4.17 Transient plot showing unity power factor with L=10mH and $\delta=8^0$

From figure 4.17 the following is observed:
Imax = 7A
DC bus = 286 V
Phase difference between input voltage and current = 0
Power factor angle $\theta = 0$
Power factor = 1

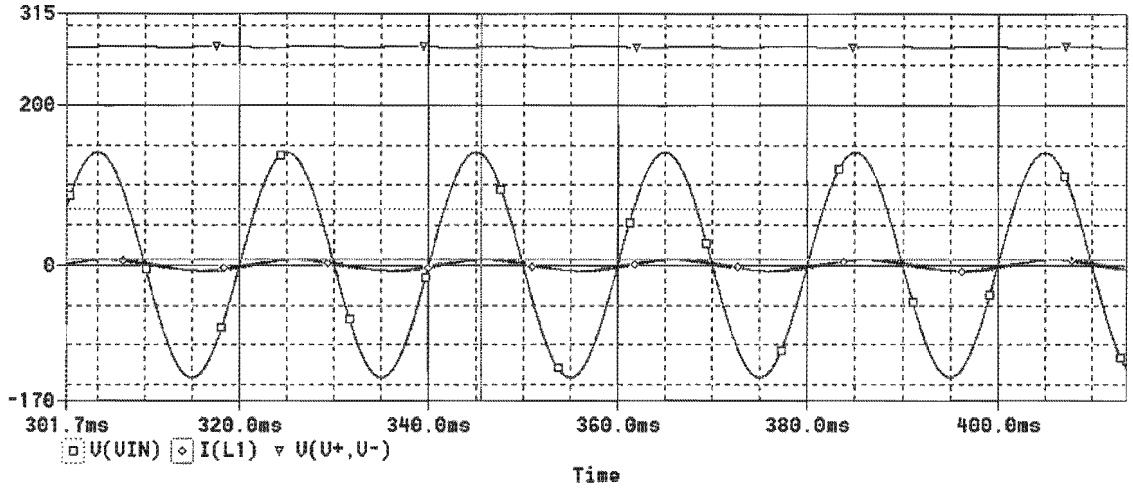


Figure 4.18 Transient plot showing unity power factor with L=5mH and $\delta=3^0$

From figure 4.18 the following is observed:

Imax = 7A
DC bus = 281 V
Phase difference between input voltage and current = 0
Power factor angle $\theta = 0$
Power factor = 1

4.1.5 SUMMARY OF RESULTS FOR UNITY POWER FACTOR OPERATION

Inductance mH	Phase Shift δ	Input Current A	Source Voltage V(RMS)	DC Bus V	Power Factor
15	13^0	7	100	288	1
10	8^0	7	100	286	1
5	3^0	7	100	281	1

Table 2 Summary of results for unity power factor

4.1.6 OBSERVATIONS FOR UNITY POWER FACTOR WITH A MODULATION INDEX OF 1

In this simulation we kept the previous load resistance of 40Ω and varied the phase shift, δ, to observe if unity power factor can be achieved.

From the results in table [2] we can observe the following:

- The 15mH inductance needed a 13^0 phase shift to obtain unity power factor. Unity power factor occurred at a DC bus voltage of about 288V.
- The 10mH inductance needed a 8^0 phase shift to obtain unity power factor. Unity power factor occurred at a DC bus voltage of about 286V.
- The 5mH inductance needed a 3^0 phase shift to obtain unity power factor. Unity power factor occurred at a DC bus voltage of about 281V.

We can also observe that the size of the inductors does not affect the voltage at which unity power factor operation occurs. The size of the inductors only affects the amount of phase shift needed to obtain a unity power factor. From table 1 we can observe that a larger inductance requires more phase shift to obtain unity power factor for the same load.

Using equation 7, $V_d = \frac{2V}{ma\ Cos(\delta)}$ we can calculate the DC bus voltage.

Inductance mH	Phase Shift δ	Source Voltage V(RMS)	Simulated DC Bus Voltage	Calculated DC Bus Voltage
15	13^0	100	288	290.2
10	8^0	100	286	285.6
5	3^0	100	281	283.2

Table 3 Comparison between the simulated and calculated DC bus voltages.

4.1.7 UNITY POWER FACTOR WITH MODULATION INDEX OF HALF

In this section unity power factor operation is achieved using a modulation index of a half. Observations are made about the amount of phase shift needed as well as the value of the DC bus at unity power factor. An inductance of 10mH is used with three loads namely, 1000W, 500W and 250W. These loads are resistive and connected across the DC bus. The main aim of this simulation is to investigate whether unity power factor is determined by the inductance used, the modulation index or the amount of power being drawn from the system.

The motivation behind lowering the modulation index is because there are two fundamental voltages at the midpoints of the second and third legs with respect to neutral, namely the fixed frequency (50Hz) and a variable frequency. The sum of these modulation indexes cannot be greater than 1 in order to avoid over-modulation. The modulation index of the fixed frequency is the same for all three legs of the convertor and therefore has to be less than 1 if other frequencies are present. For this reason it should be investigated if unity power factor can be obtained for modulation indexes less than 1.

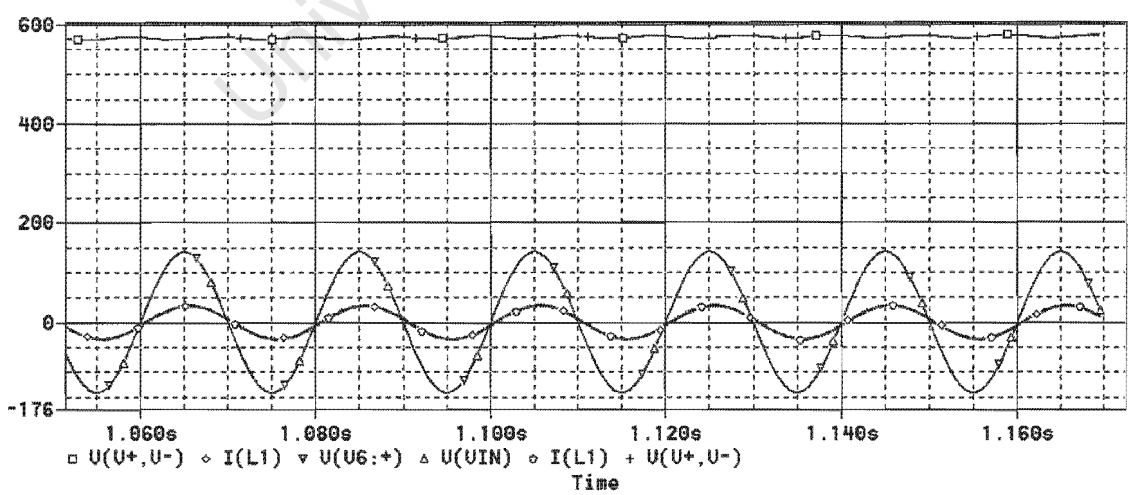


Figure 4.19 Transient plot showing unity power factor with L=10mH and $\delta=13^0$ (1000W)

In figure 4.19, the modulation index is decreased from 1 to a 0,5. An inductance of 10mH is used and a phase shift of 13^0 is required to maintain the DC bus voltage of about 572V at a load of 1000W. Unity power factor operation occurs at about 572V. Referring to the results obtained section 4.1.6, we can see that unity power factor occurred at a dc bus voltage of 286V when a modulation index of 1 was used. By observation we can see that the DC bus voltage at which unity power factor occurs is indirectly proportional to the modulation index used. By halving the modulation index, we double the DC bus voltage.

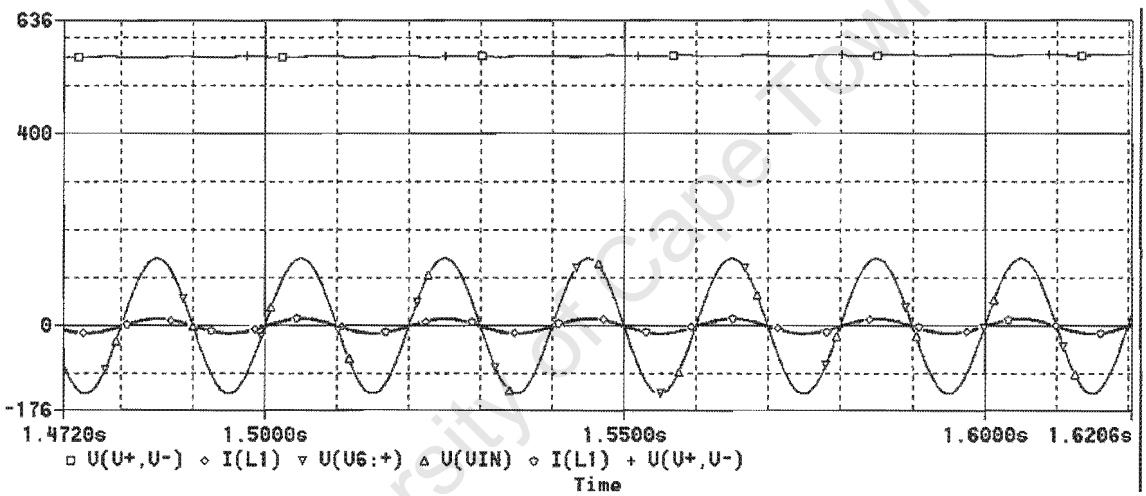


Figure 4.20 Transient plot showing unity power factor with L=10mH and $\delta=6^0$ (500W)

In figure 4.20, the same inductance of 10mH was used. The load was decreased to 500W. For the same previous phase shift of 13^0, it was found that the DC bus voltage increased and the power factor decreased. A new phase shift of 6^0 was used and it was found that the DC bus voltage decreased until unity power factor operation was obtained.

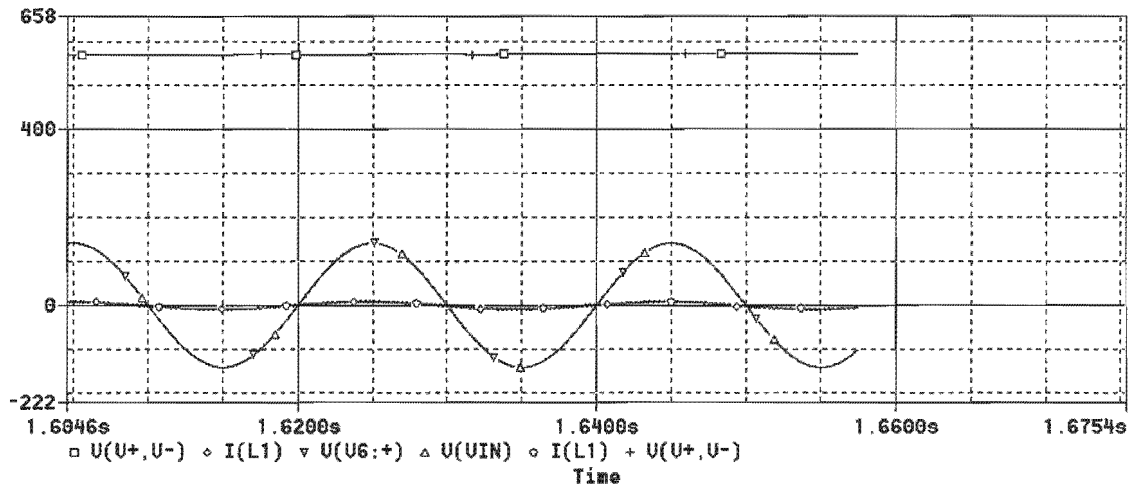


Figure 4.21 Transient plot showing unity power factor with L=10mH and δ=3 (250W)

In figure 4.21, the load was decreased to 250W. This had the same effect as in figure 4.20. The DC bus voltage increased and the phase shift had to be decreased to drop the DC bus voltage and obtain unity power factor operation again.

4.1.8 OBSERVATIONS MADE FROM THE SIMULATION USING A MODULATION INDEX OF A HALF AT UNITY POWER FACTOR

From figures [4.19 to 4.21] we can observe that unity power factor operation can be obtained using the same inductance, under different loads and a modulation index of ½ .

When a load of 1000W was used, a phase shift of 13^0 was needed to obtain unity power factor. When a 500W load was used, a phase shift of 6^0 was needed and similarly with a load of 250W a 3^0 phase shift was needed. In all these scenarios the same inductance of 10mH was used and unity power factor was obtained.

Referring to section 4.1.7 we observed that the size of the inductors does not affect the voltage at which unity power factor operation occurs. The size of the inductors only affects the amount of phase shift needed to obtain a unity power factor. From figures 4.19 to 4.21 we can observe that when the modulation was decreased to 0.5, the DC bus voltage at unity power factor operation has doubled when compared to section 4.1.6. This correlates with equation [7] and shows that the DC bus is inversely proportional to the modulation index for small values of δ.

A very important recommendation can be made at this point. Instead of feeding back a high DC bus voltage and varying the phase angle δ to control the power we can use a different control strategy. It is important to realise that maintaining ANY ARBITRARY DC bus does not guarantee a unity power factor. Unity power factor will only occur at a DC bus voltage that is derived from equation [7].

The new control strategy will therefore be as follows:
The power factor angle θ is fedback and the phase shift δ is adjusted until θ is equal to zero. This will guarantee a unity power factor. At unity power factor the DC bus voltage will always be determined by equation [7].

4.2 THE FULL SINGLE TO THREE PHASE VARIABLE SPEED DRIVE

The full drive is now simulated with the following variables. Vin = 100Vrms (50Hz) L=10mh load =1000VA(delta) Output frequency = 25Hz at half output voltage, 50Hz at full output voltage. Full output line to line voltage = 100Vrms.

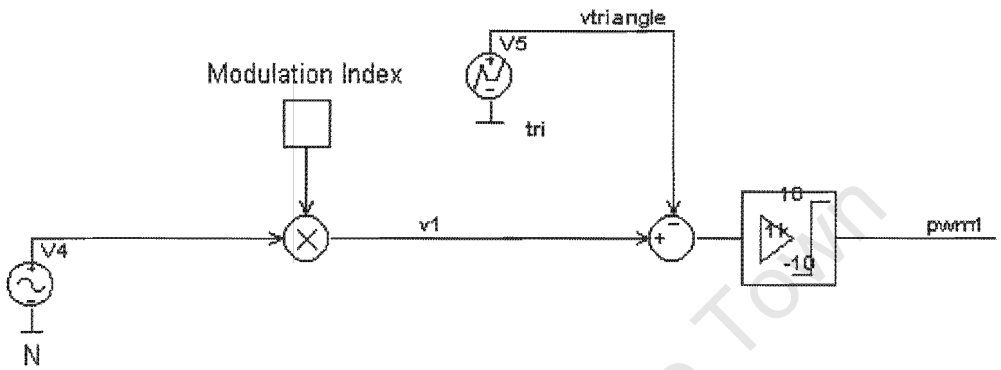


Figure 4.22 Schematic of the PWM control signal generator for the first leg of the convertor

In figure 4.22, V4 represents a reference sinusoid that is scaled by a constant to produce v1.The phase of V4 can be adjusted to be leading or lagging the mains source voltage by manually setting the attributes of V4 in the simulator. V1 is in phase with V4. v1 is compared to a triangular waveform,V5, and the result is limited to +10V and -10V. The result is indicated by the label pwm1. This PWM1 signal is used to control the switches of the first leg of the convertor.

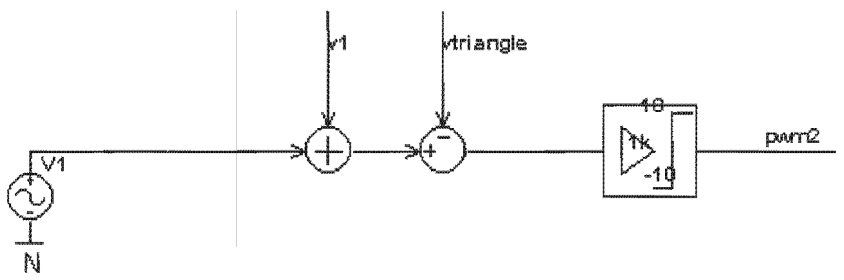


Figure 4.23 Schematic of the PWM control signal generator for the second leg of the convertor

In figure 4.23, V1 represents a sinusoid of a variable frequency. The variable frequency is added to the phase shifted sinusoid, v1, and then compared to the triangular waveform,

vtriangle. The resulting PWM2 is limited to +10V and -10V. The PWM2 signal is connected to the switches of the second leg of the convertor.

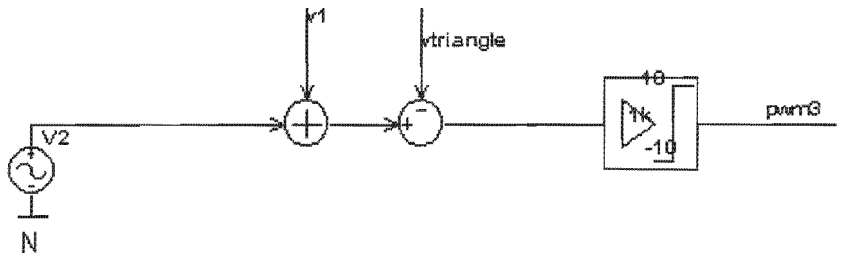


Figure 4.24 Schematic of the PWM control signal generator for the third leg of the convertor

In figure 4.24, V2 represents a sinusoid of a variable frequency. The voltage V2 is phase shifted by 60^0 to the voltage source, V1,in figure 4.23. The variable frequency is added to the phase shifted sinusoid, v1, and then compared to the triangular waveform, vtriangle. The resulting PWM3 is limited to +10V and -10V. The PWM3 signal is connected to the switches of the third leg of the convertor.

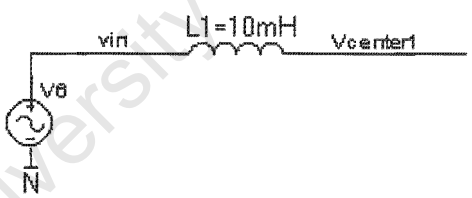


Figure 4.25 The schematic diagram for the voltage source and input inductance

In figure 4.25, V6 represents the mains source voltage. The output of the inductance, L1, is connected to the centre point of the first leg of the convertor as shown in figure 4.26. The voltage at the midpoint of the first leg is labelled Vcenter1. The label N shows the neutral of the system.

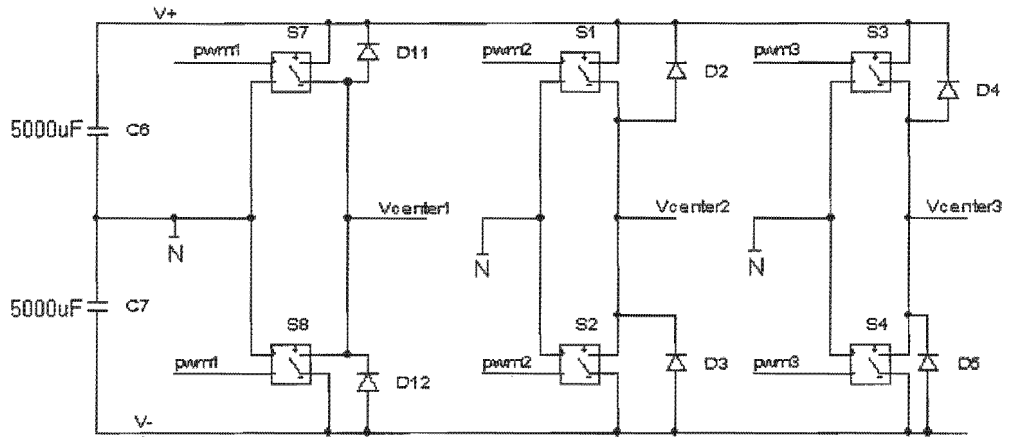


Figure 4.26 Schematic diagram of the three phase bridge and spit capacitor bank

In figure 4.26, there are three pairs of switches for the three legs of the convertor. The first leg of the convertor is still the front end rectifier . The front end rectifier comprises of switches S7, S8 and diodes D11 and D12. The control signals for the first leg are generated in figure 4.22. The four switch inverter comprises of the second and third legs of the convertor. The second leg is made up of the switches S1,S2 and diodes D2 and D3. The third leg is mad up of the switches S3,S4 and diodes D4 and D5. The source voltage, see figure 4.25, is connected to the inductance and the output of the inductance is connected to the centre point of the first leg. This point is labelled Vcenter1 in figure 4.25. A split capacitor bank is connected across the DC bus and is made up of capacitors C6 and C7. The centre of the capacitor bank is connected to the neutral of the system. The three centre points Vcenter1,Vcenter2, Vcenter3 are connected to the load as shown in figure 4.27

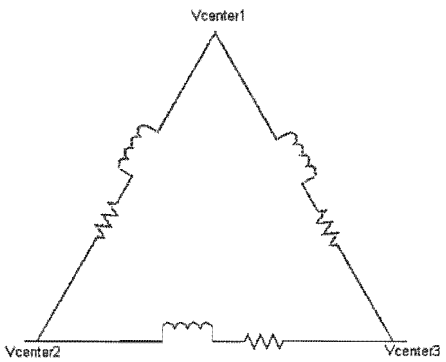


Figure 4.27 Schematic diagram of the delta three phase load

4.2.1 SIMULATION OF THE VARIABLE SPEED DRIVE

In this simulation "fixed frequency" refers the fundamental of the phase shifted wave found at the midpoint of the first leg of the convertor.

The term "variable frequency" refers to the fundamental of the variable output frequency found at the midpoints of the second and third legs of the convertor.

For the simulation traces in this section, the following symbols are used :

V(VIN) represents the sinusoidal source voltage.

I(L1) represents the current drawn from the source.

$V(V^+,V^-)$ represents the voltage across the DC bus.

V(Vcenter1) represents the line to neutral voltage at the centre of the first leg

V(Vcenter2) represents the line to neutral voltage at the centre of the second leg

V(Vcenter3) represents the line to neutral voltage at the centre of the third leg

V(Vcenter1, Vcenter2) represents the voltage across the first and second leg

V(Vcenter2, Vcenter3) represents the voltage across the second and third leg

V(Vcenter3, Vcenter1) represents the voltage across the third and first leg

δ represents the phase difference between the voltage source and the fundamental of the line to neutral voltage at the midpoint of the first leg of the convertor

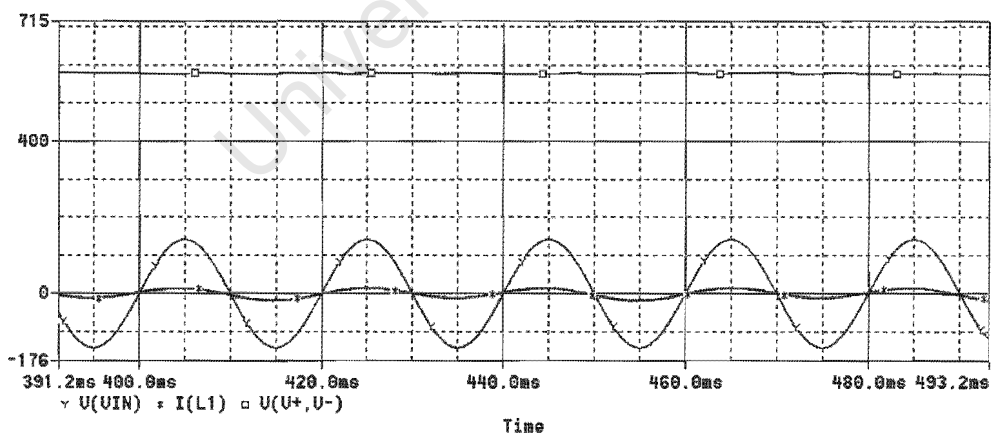


Figure 4.28 Transient plot of Input Voltage, Input Current and DC Bus voltage

In this simulation an inductance of 10mH is used. The sinusoidal voltage source is 100VRms. The load is a 1000VA three phase delta load as shown in figure 4.27. From figure 4.28 we can observe that unity power factor has been achieved. At unity power factor the DC bus voltage is about 580Vand δ is 13^0.

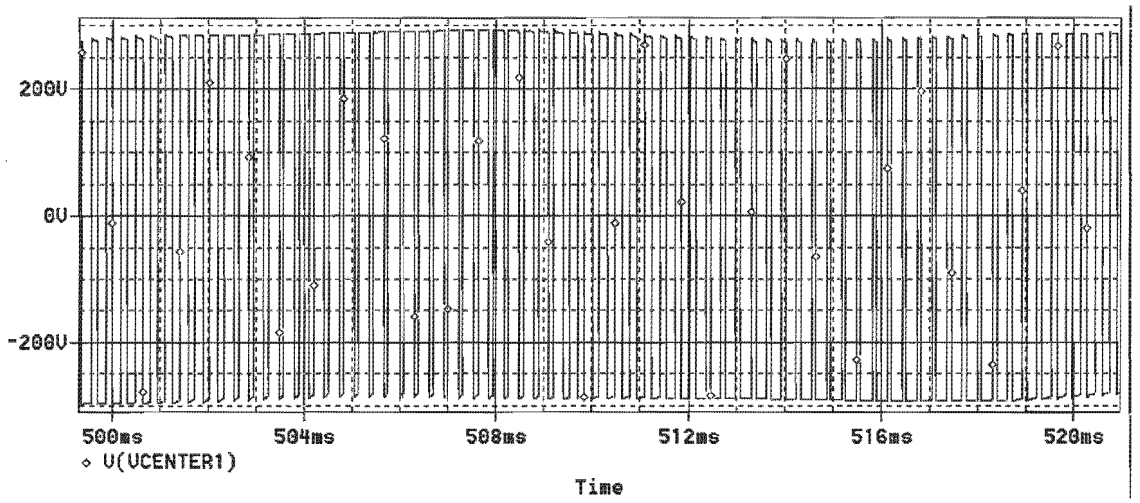


Figure 4.29 Transient plot of voltage at the midpoint of the first leg of the convertor

Figure 4.29 represents the voltage seen at the midpoint of the first leg with respect to the neutral. Embedded in this PWM waveform is a fundamental, that is frequency locked to the voltage source and phase shifted by δ, as well as the high frequency carrier.

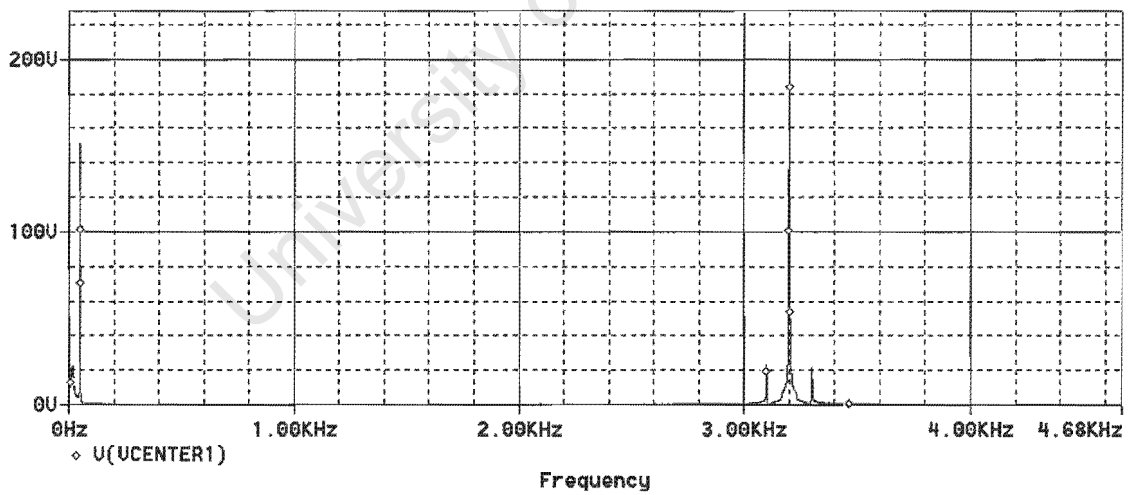


Figure 4.30 Frequency plot of voltage at the midpoint of the first leg of the convertor

Figure 4.30 shows the fundamental frequency at 50Hz as well as the carrier at 3.2KHz. The peak voltage of the fundamental is 141V. Referring to figure 4.28, the DC bus voltage is about 580V. This correlates with the fact that the modulation index is 0.5

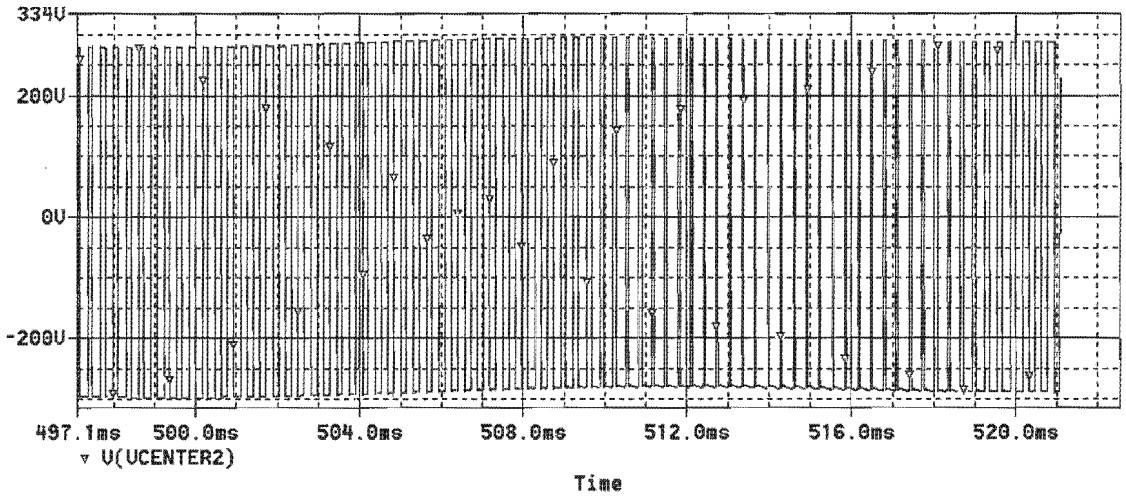


Figure 4.31 Transient plot of voltage at the midpoint of the second leg of the convertor

Figure 4.31 represents the voltage seen at the midpoint of the second leg with respect to the neutral. Embedded in this PWM waveform is the fundamental of the fixed frequency, at a modulation index of 0.5 and fundamental of the variable frequency at a modulation index of 0.5.

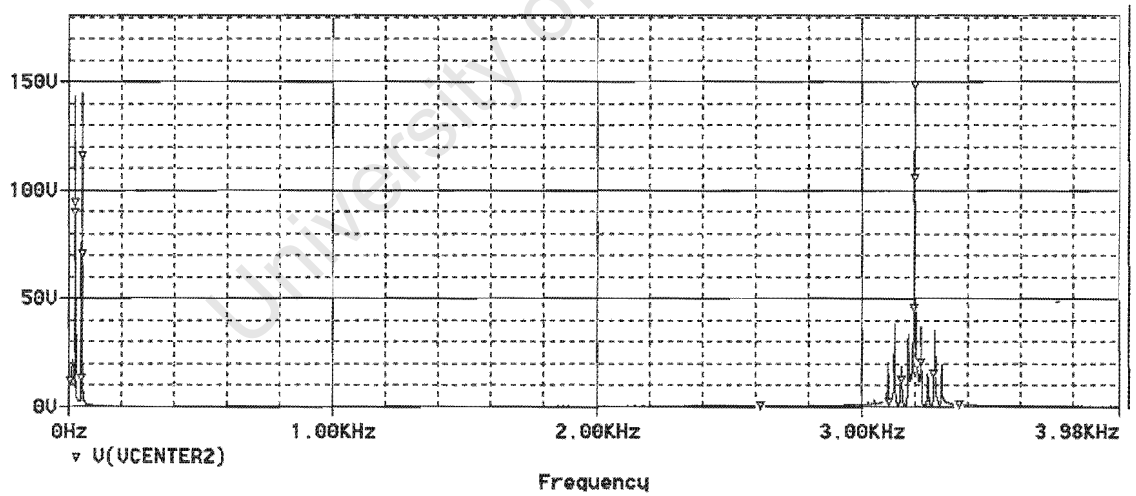


Figure 4.32 Frequency plot of the midpoint of the second leg with respect to neutral

Figure 4.32 shows the fundamental of the fixed frequency phase shifted fundamental at 50Hz. For clarity purposes a variable frequency of 25Hz was used for this plot. The two distinct fundamentals can bee seen in figure 4.32. If both fundamentals were at 50Hz it would be difficult to distinguish between the two.

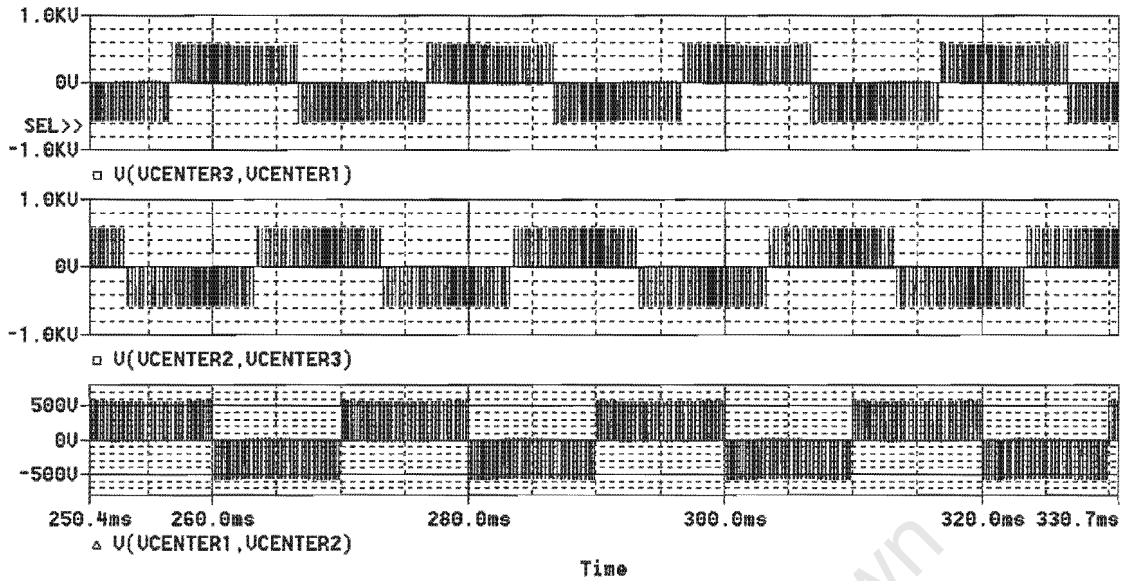


Figure 4.33 Line to line voltages seen by the three phase load (50Hz output)

Figure 4.33 shows a symmetrical 3 level PWM seen by the three phase load. In this case both the fixed frequency fundamental and the variable frequency are at 50HZ. When observing the line to line voltages, the common fixed frequency cancels out and only the variable frequency is seen. In this case the variable frequency is 50Hz and the fixed frequency is 50Hz and therefore only 50Hz is seen by the three phase load.

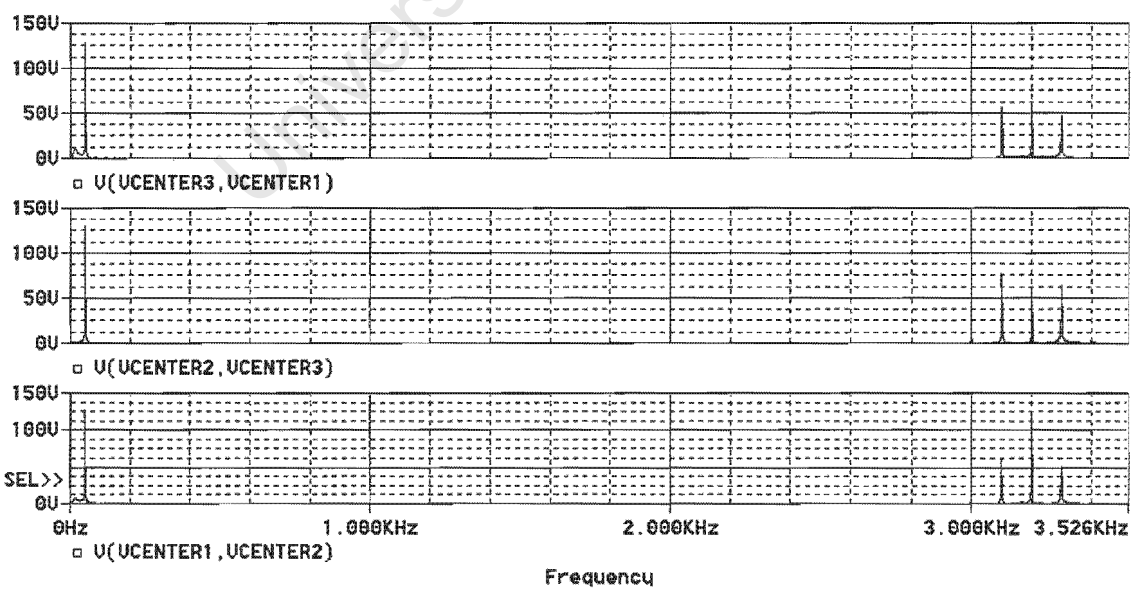


Figure 4.34 Frequency plot of the line to line voltages seen by the load (50Hz output)

Figure 4.34 shows the fundamental as well as high frequency carrier seen by the load.

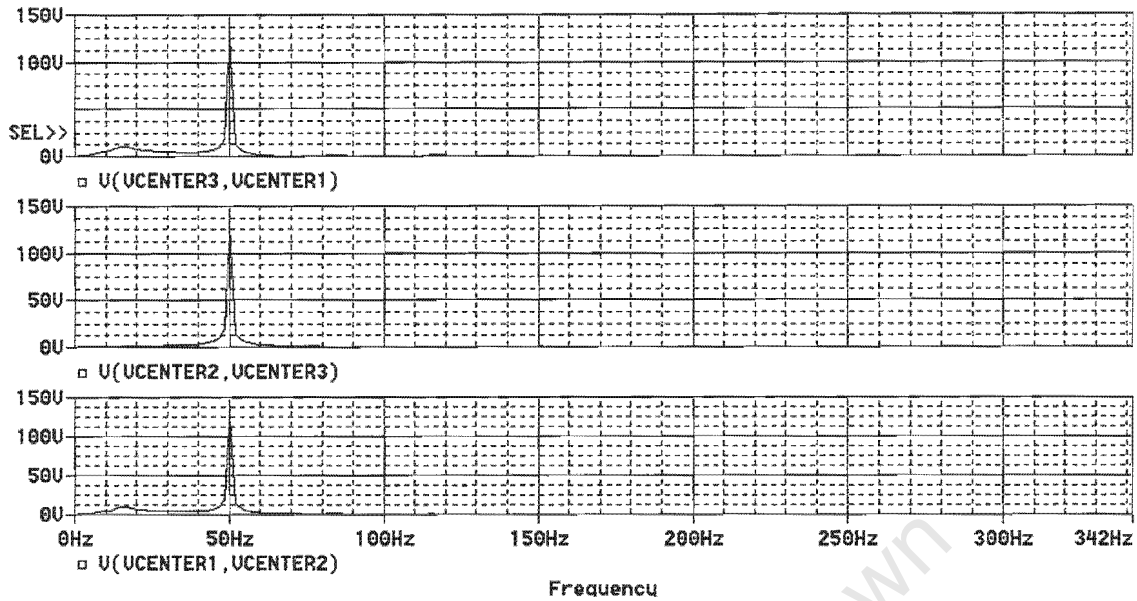


Figure 4.35 Frequency plot of the line to line voltage (magnified)

Figure 4.35 shows a magnified view of the frequency spectrum of the line to line voltages. Here we can observe that the fundamentals of the line to line voltages seen by the three phase load are at a frequency of 50Hz and a voltage of 100V RMS. (full output voltage)

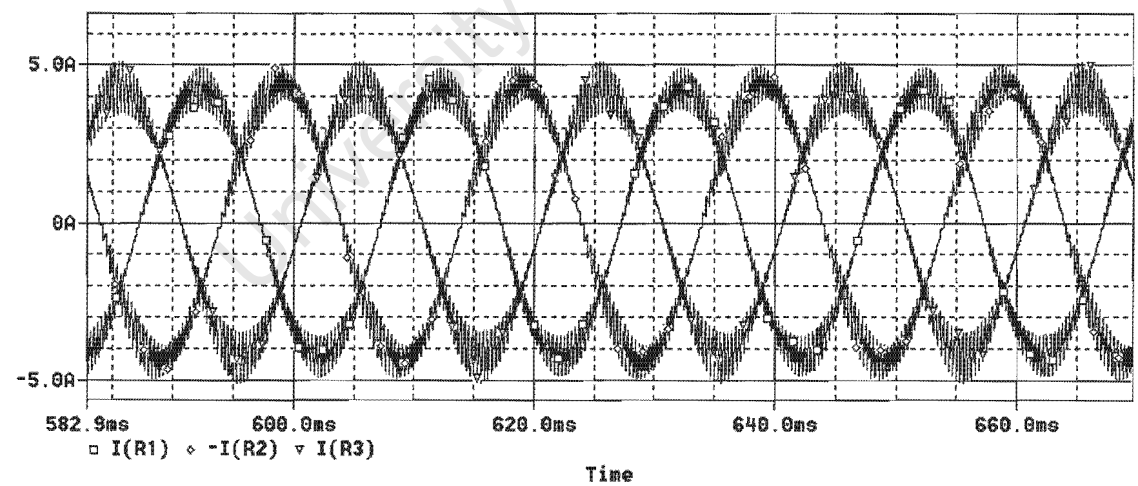


Figure 4.36 Transient plot of the line currents at 50Hz at full output voltage (100Vrms)

Figure 4.36 shows the line currents at full output voltage and full load power of 1000VA. The delta load of figure 4.27 was used to obtain these results. These results conclude that a full output voltage at 50Hz is obtainable at full load.

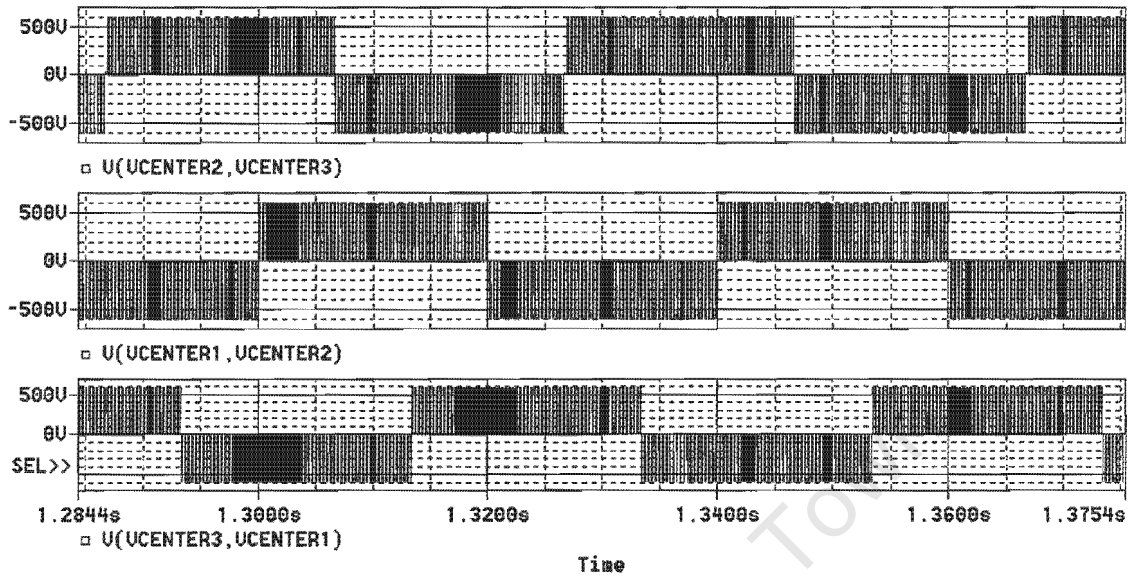


Figure 4.37 Line to line voltage seen by the three phase load at 25Hz output

The next step in the simulation is to obtain a 25Hz output frequency at half the output voltage. In figure 4.37 the variable frequency has been set to 25Hz and a modulation index of 0.25. The fixed frequency 50Hz component cancels out in the line to line voltages. As a result only the 25Hz variable frequency and carrier is seen by the load.

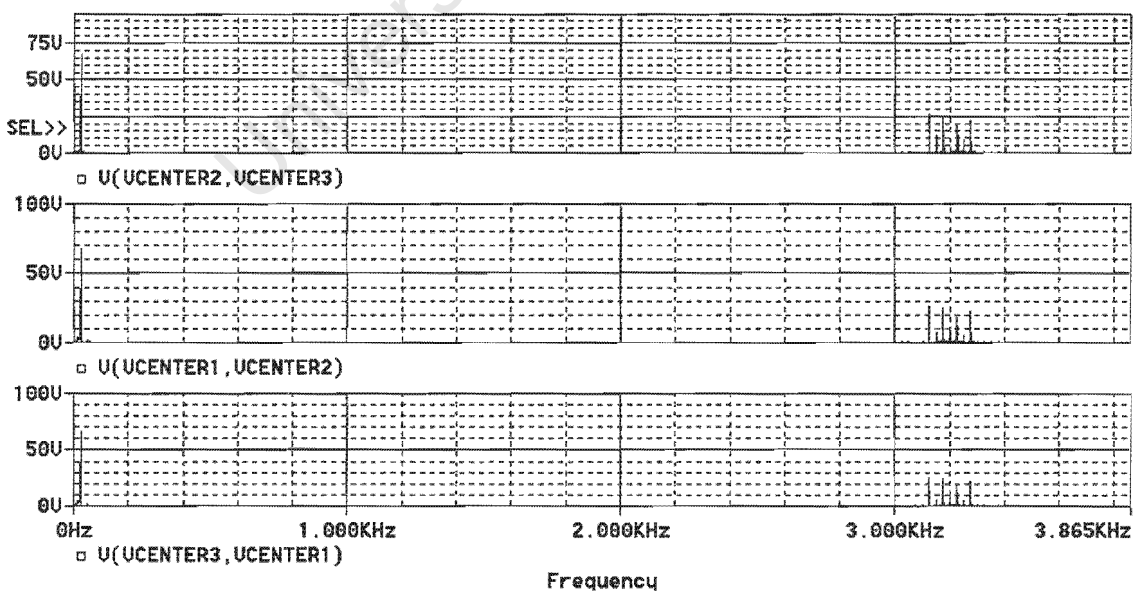


Figure 4.38 Frequency plot of the line to line voltage seen by the load (25Hz output)

Figure 4.38 shows a 25Hz output line to line voltage at half the full output voltage.

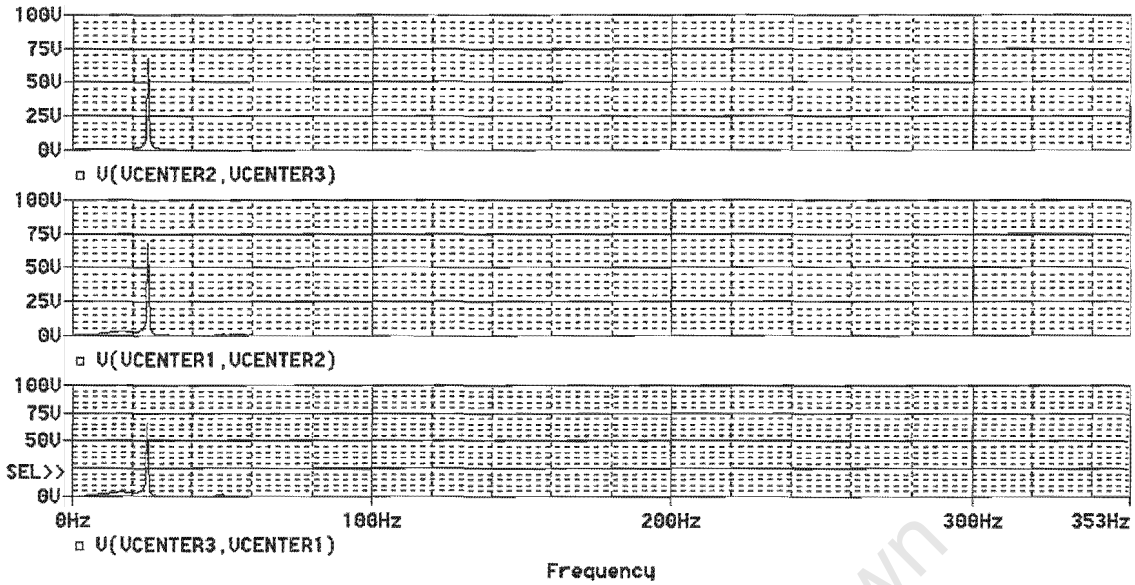


Figure 4.39 Frequency plot of the line to line voltages (magnified)

Figure 4.39 shows a magnified frequency plot of the line to line voltages when the output frequency is 25Hz and output voltage is half the full output.

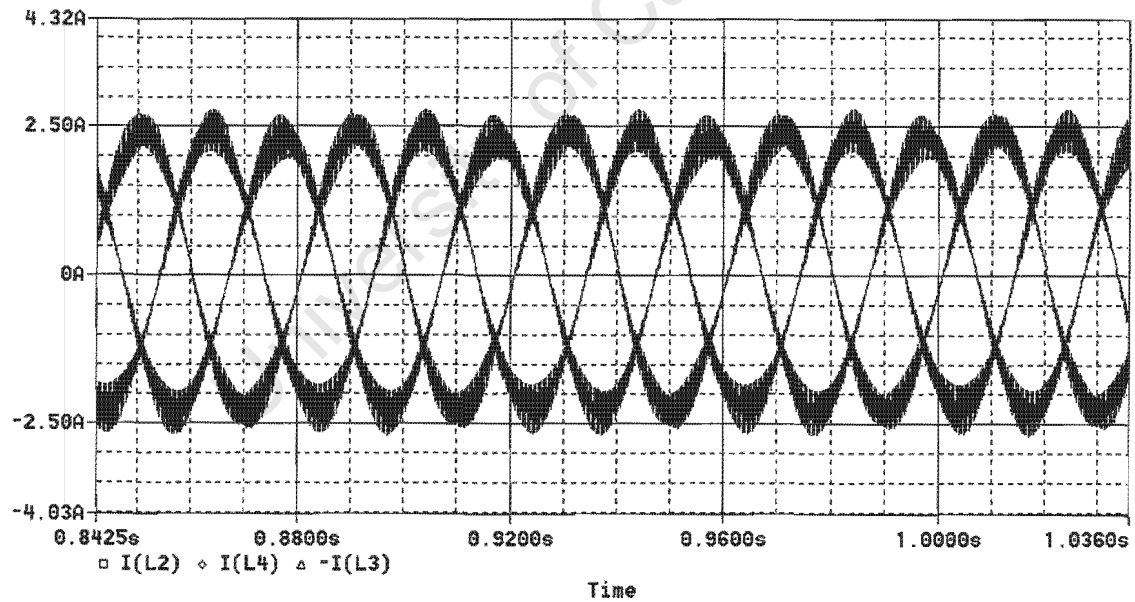


Figure 4.40 Line currents at 25Hz and half output line to line fundamental voltage

Figure 4.40 shows the line currents at half the full output voltage and half the full load power. The delta load of figure 4.26 was used to obtain these results. These results conclude the magnitude and frequency of the fundamental in the line to line voltage can be can be controlled.

4.3 CONCLUSIONS DRAWN FROM THE SIMULATION

The conclusions drawn here are made by observation of the various simulation traces of sections 4.1 and 4.2.

4.3.1 THE FRONT END RECTIFIER

The front end rectifier comprises of the first leg of the convertor as shown in figure 4.3. The frequency of the fundamental at the midpoint of the first leg, labelled E in figure 4.3, is fixed. This frequency is the same as the frequency of the voltage source but phase shifted by δ.

From figures 4.5 to 4.15 it is evident that the degree of phase shift is proportional to the increase in DC bus voltage for small values of δ. By observation of the results in table 1, it is evident that the power factor is affected by the amount of phase shift. These results conclude that unity power factor is not guaranteed for any DC bus voltage.

When examining the inductances used in table 1, it is evident that the smaller inductances produce a larger increase in DC bus voltage for the same phase shift. This could place constraints on the minimum size for the inductance used. If too small an inductance is used and a specific DC bus value is needed, there could be a situation where the increase in DC bus per degree of phase shift is too large. As a result the required DC bus voltage will never be obtained and this results in a DC bus that oscillates around the required DC voltage.

When referring to the results in table 2, we can observe that unit power factor is only obtainable at a specific DC bus voltage. The DC bus voltage should be derived by equation [7]. We can also observe that the size of the inductors does not affect the voltage at which unity power factor operation occurs. The size of the inductors only affects the amount of phase shift needed to obtain a unity power factor. From table 2 we can observe that a larger inductance requires more phase shift to obtain unity power factor for the same load.

In sections 4.1.6 and 4.1.7 we observe the relationship between the modulation index and the DC bus voltage at which unity power factor operation occurs. By observation it is found that for small values of δ, the DC bus voltage is indirectly proportional to the modulation index of the first leg.

4.3.2 THE FULL SINGLE TO THREE PHASE VARIABLE SPEED DRIVE

The results of the simulation are shown in figures 4.28 to 4.40. A three phase variable frequency and voltage is obtained in the line to line voltages seen by the load.

In the simulation an inductance of 10mH is used. The sinusoidal voltage source is 100VRms. The load is a 1000VA three phase delta load as shown in figure 4.27. From figure 4.28 we can observe that unity power factor has been achieved. At unity power factor, the DC bus voltage is about 580Vand δ is 13^0. This correlates with equations 7 and 8. When the load is decreased to 500W, δ is about 6^0.

By examine figures 4.28 to 4.40 we can observe the following :

- A balanced three phase line to line voltage is generated by the convertor.
- The magnitude and frequency of the output voltage is controllable.
- A three level symmetrical PWM is found in the line to line voltages.

We can therefore conclude, by observation, that three phase power can be generated from a single phase supply and unity power factor can be achieved.

CHAPTER 5

HARDWARE IMPLEMENTATION

5.1 POWER CIRCUITRY

Figure [5.1] shows a layout of the power circuitry used in the drive. A 2KVA variac is used to convert the 220VRms supply to a variable 0 - 110V supply. A small 2VA transformer is placed across the output of the variac. This small transformer is used to obtain the phase and frequency of the supply. A LEM unit is used to obtain a voltage representation of the current flowing from the source. The output of the small transformer and LEM unit is fed to the control circuitry. The inductances used in the circuitry varied from 1mH to 9mH and are all capable of conducting 30A of current. A Semikron 3 phase IGBT bridge forms the front end rectifier as well as the 4 switch inverter. Two banks of capacitors are connected to form a split capacitor configuration.

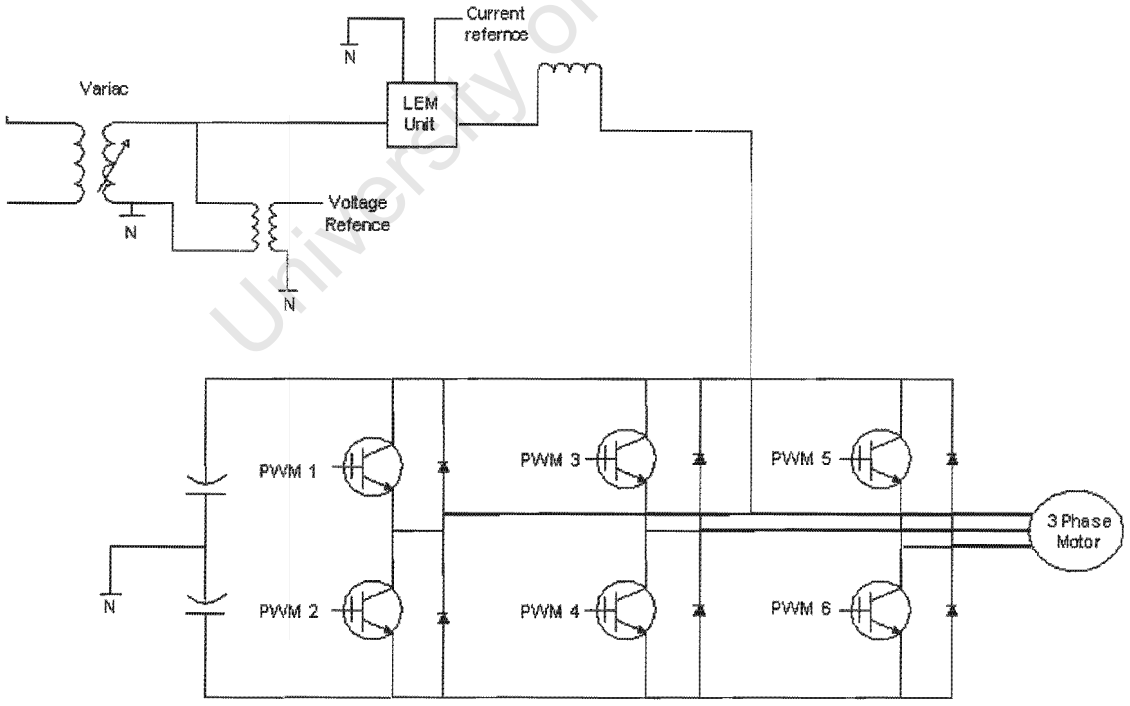


Figure 5.1 A hardware layout of the power circuitry

5.2 CONTROL CIRCUITRY

The control circuitry can be divided into three sections namely the control feedback interface, the DSP controller and the PWM driver board.

5.2.1 THE CONTROL INTERFACE BOARD

The source voltage and current drawn are obtained via the small transformer and LEM unit. These signals have to be squared and limited so that they can be used to trigger the DSP's external interrupts. The sinusoidal voltages are fed through a zero crossing detector. The output of the zero crossing detector is then limited to 5V as to protect the DSP from damage. This is shown in figure [5.2 and 5.3].

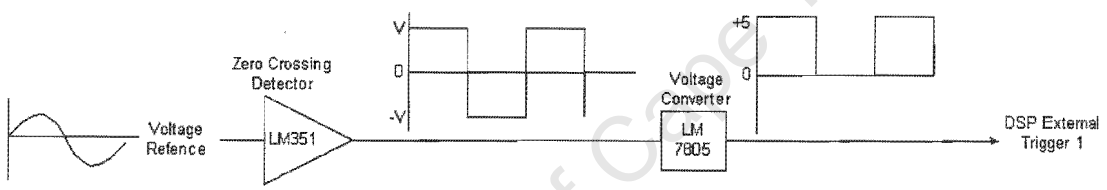


Figure 5.2 The voltage phase and frequency detector

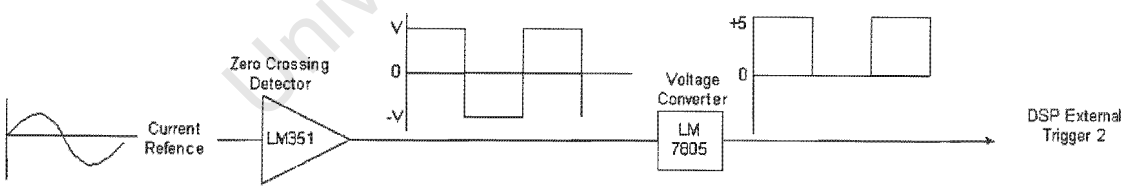


Figure 5.3 The current phase detector

5.2.2 THE DSP CONTROLLER

The DSP continuously samples a voltage derived from a potentiometer as seen in figure 5.4. The level of the voltage is used to determine the output frequency and amplitude of the ouptput voltage of the drive. The control interface board continuously triggers the external interrupts of the DSP. The first external interrupt is triggered by the voltage reference. The second external interrupt is triggered by the current reference. The output of the DSP is a PWM signal that has a 0 to 5V amplitude.

5.2.3 THE IGBT DRIVER BOARD

The input to the IGBT driver board must be 15V signal and therefore a level shifter is used to convert the 5V DSP output signal to a 15V signal. The driver board provides an isolation between the DSP and the power circuitry. This prevents any high voltages from damaging the DSP board. The PWM outputs of the IGBT driver board interfaces with the power circuitry and controls the IGBTs.

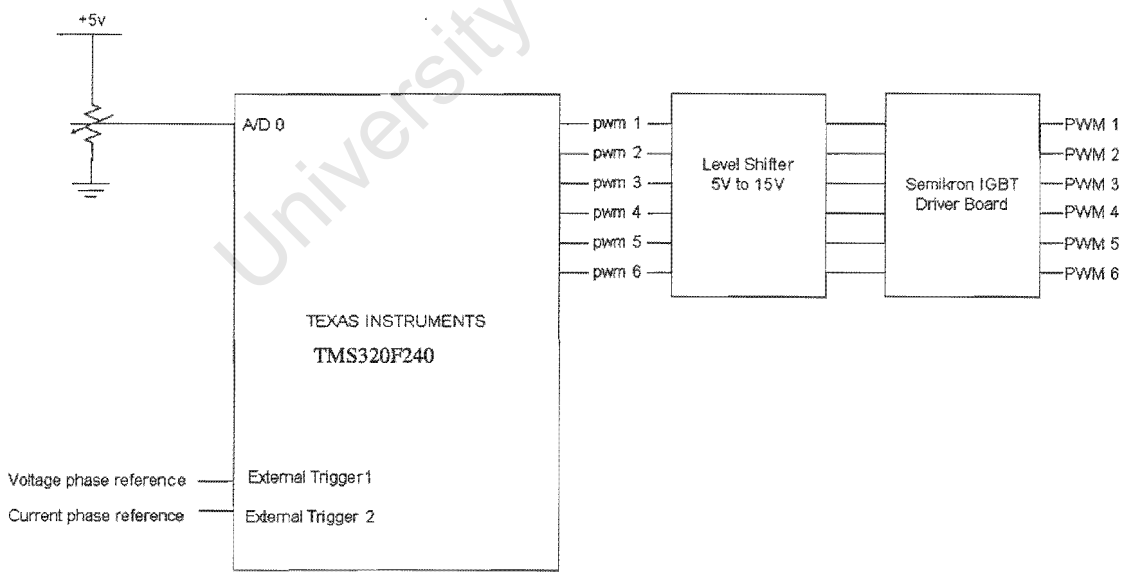


Figure 5.4. The DSP controller, level shifter and IGBT driver board

CHAPTER 6

SOFTWARE IMPLEMENTATION

6.1 THE SINETABLE

A sinetable is extensively used to generate the control signals for the PWM. The values of the sinetable are shown in figure [6.1]. The sinetable consists of 256 points.

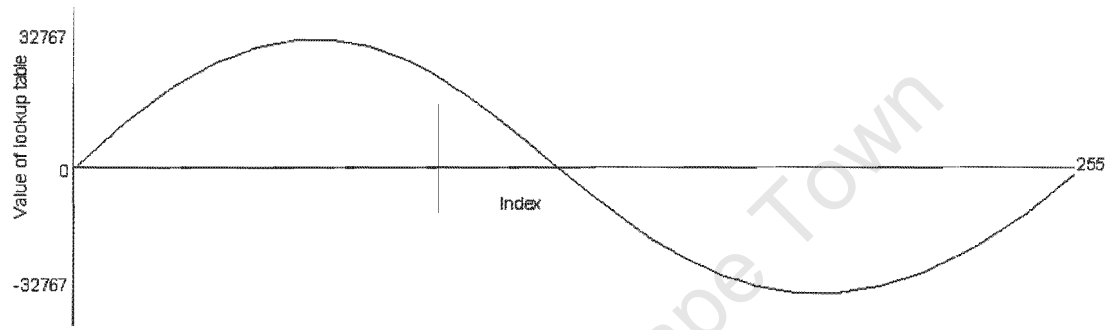


Figure 6.1 Lookup table used by the software.

6.2 CARRIER FREQUENCY GENERATION

Synchronous PWM is used in this converter because it generates a fundamental frequency and low frequency harmonics. Noting that for a 256 point sinetable we can calculate the carrier the carrier as follows:

$$f_c = 50\text{x}256 = 12.8KHz$$

It should be noted that the frequency of the mains voltage source is not always constant and therefore the frequency of the carrier needs to be adjusted as the mains frequency varies. This process is done in real-time with the software.

6.3 PWM GENERATION

Synchronous PWM is achieved by comparing the instantaneous value of the lookup table to the instantaneous value of a triangular carrier . The triangular waveform is produced by configuring a timer (T1) to count up and down continuously. The comparison is done by writing the value of the sinetable to a compare register. This will set or reset the PWM outputs depending on the comparison.

6.4 GENERATION OF THE PHASE LOCK

A simple phase lock loop algorithm is used for simplicity. Referring to the program listing in appendix [A], the waveform referenced by the variable "X" is used to phase and frequency lock the system to the mains voltage. Referring to the program listing, the phase locking is done by the interrupt called C_INT1(). Figure 6.2 shows a flow chart of the phase locking algorithm. The waveform is generated by using the following algorithm.

- The process is started when the external interrupt 1 is triggered by the voltage reference. This occurs during zero crossing.
- The frequency of the mains is measured and the carrier frequency is adjusted to maintain synchronous PWM.
- The position of the variable X on the lookup table is examined.
- If the X variable is more than 0 but less than 127 it means that the locked waveform is lagging and therefore the frequency is sped up slightly to catch up with the mains frequency.
- If the X variable is more than 127 it means than the locked waveform is leading the mains frequency and should be slowed down.
- This is done continuously in real-time on a per cycle basis

6.5 GENERATION OF THE PHASE SHIFTED VOLTAGE *E*.

Referring to the program listing in appendix [A] we can see that the variable "shift" points to a waveform that is phase shifted from the phase locked waveform. The shifted waveform is updated at the same rate as the phase locked waveform. This shows that they are synchronized to the same frequency. The amount of phase shift is controlled by the power factor correction interrupt.

6.6 GENERATION OF THE UNITY POWER FACTOR

The power factor is controlled by the degree of phase shift. Referring to the program listing, the power factor correction is done by the interrupt C_int6(). The procedure is called when current waveform passes through the zero crossing. Figure 6.3 shows a flow chart of the algorithm. The control is achieved using the following algorithm.

- The process is started when the external interrupt 2 is triggered by the current reference. This occurs during zero crossing.
- The phase of the phase locked wave is compared to the phase of the current.
- The value of the index "X" is examined to see if there is a leading or lagging power factor.
- If x = 0 it implies that unity power factor has been achieved and consequently the phase shifted wave is unaffected.
- If 0 < x < 90 it implies that the power factor is lagging. The shift variable is increased.
- If 192 < x < 255 it implies that the power factor is leading. The shift variable is decreased.

6.7 GENERATION OF THE OUTPUT VARIABLE FREQUENCY

The variable output frequency is found at the midpoints of the second and third legs of the converter. Referring to the program listing in appendix [A], the indexes "y" and "z" point to the instantaneous values of the variable frequency. The two waveforms are locked at 60 degrees. The variable frequency is controlled by C_int(3). Figure 6.4 shows a flow chart of the PWM generators. The PWM is generated by the following algorithm,

- A DC voltage is sampled and the value is stored in the main program.
- The timer T2 is used to update the variable frequency.
- The frequency of T2 is adjusted by the DC value.
- The modulation index of the variable frequency is adjusted.
- The variable frequency is added to the phase locked frequency.
- The sum of the two frequencies is compared to the carrier to produce PWM.

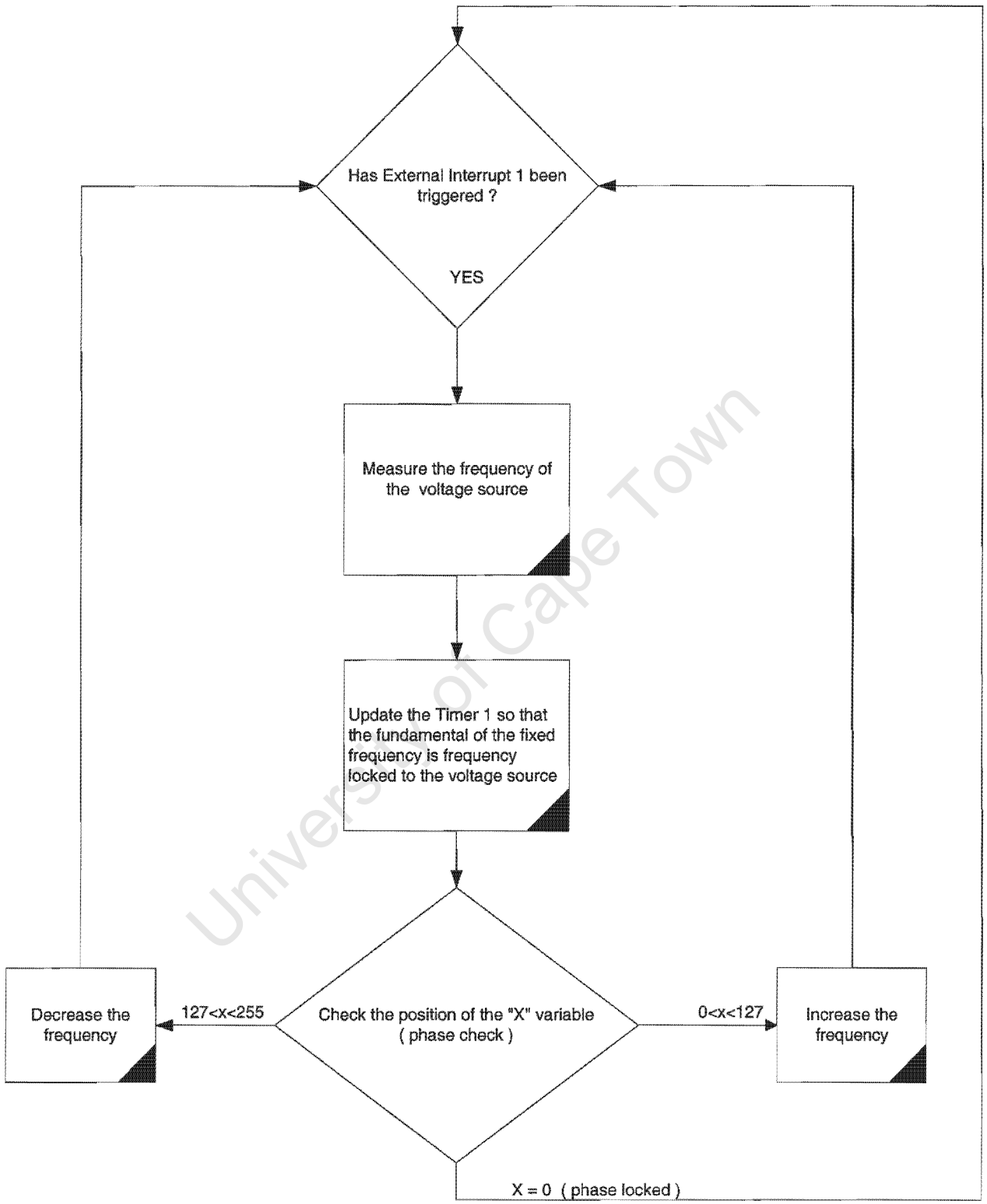


Figure 6.2 Flow chart for the Phase locking algorithim

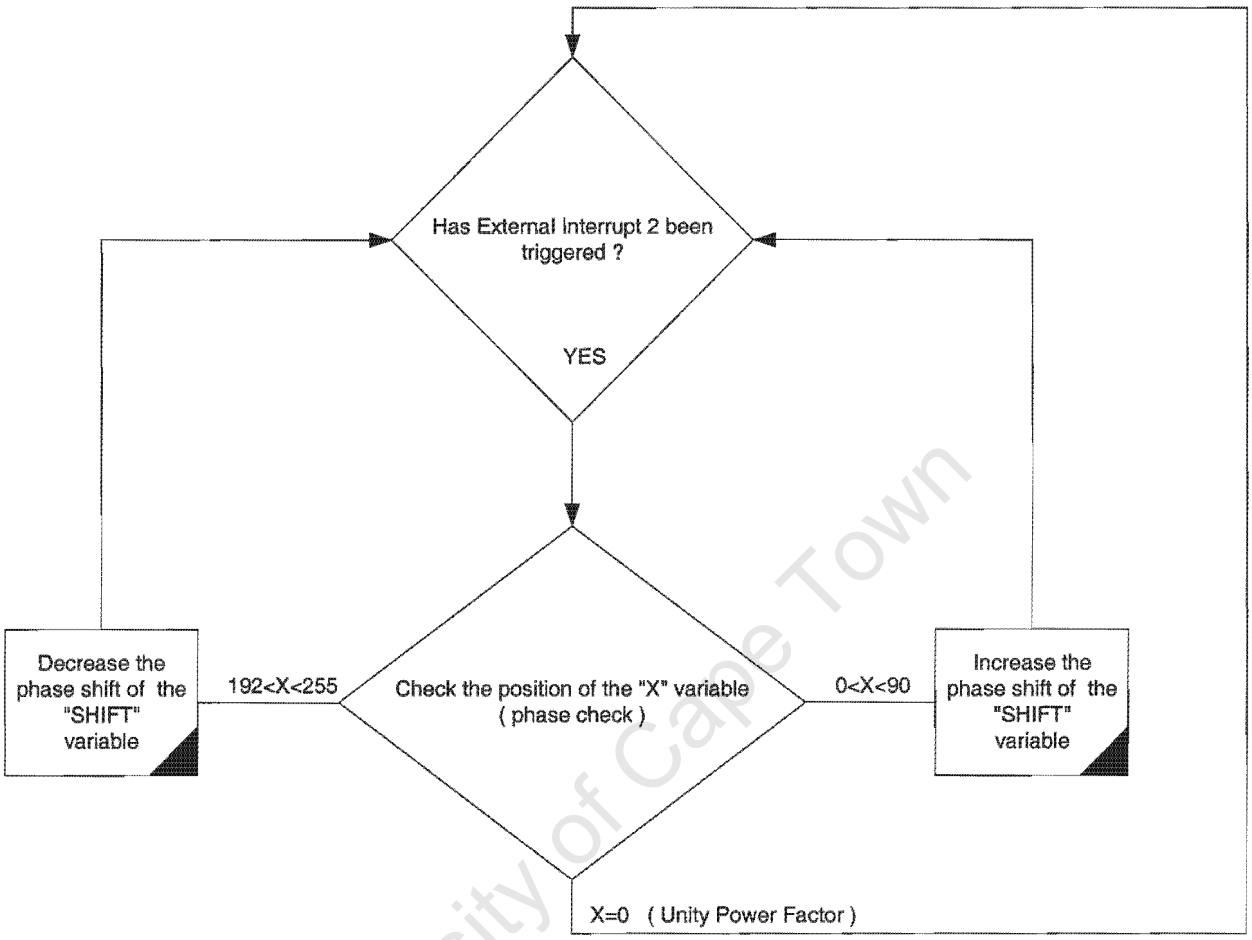


Figure 6.3 Flow chart for the Unity power factor algorithim

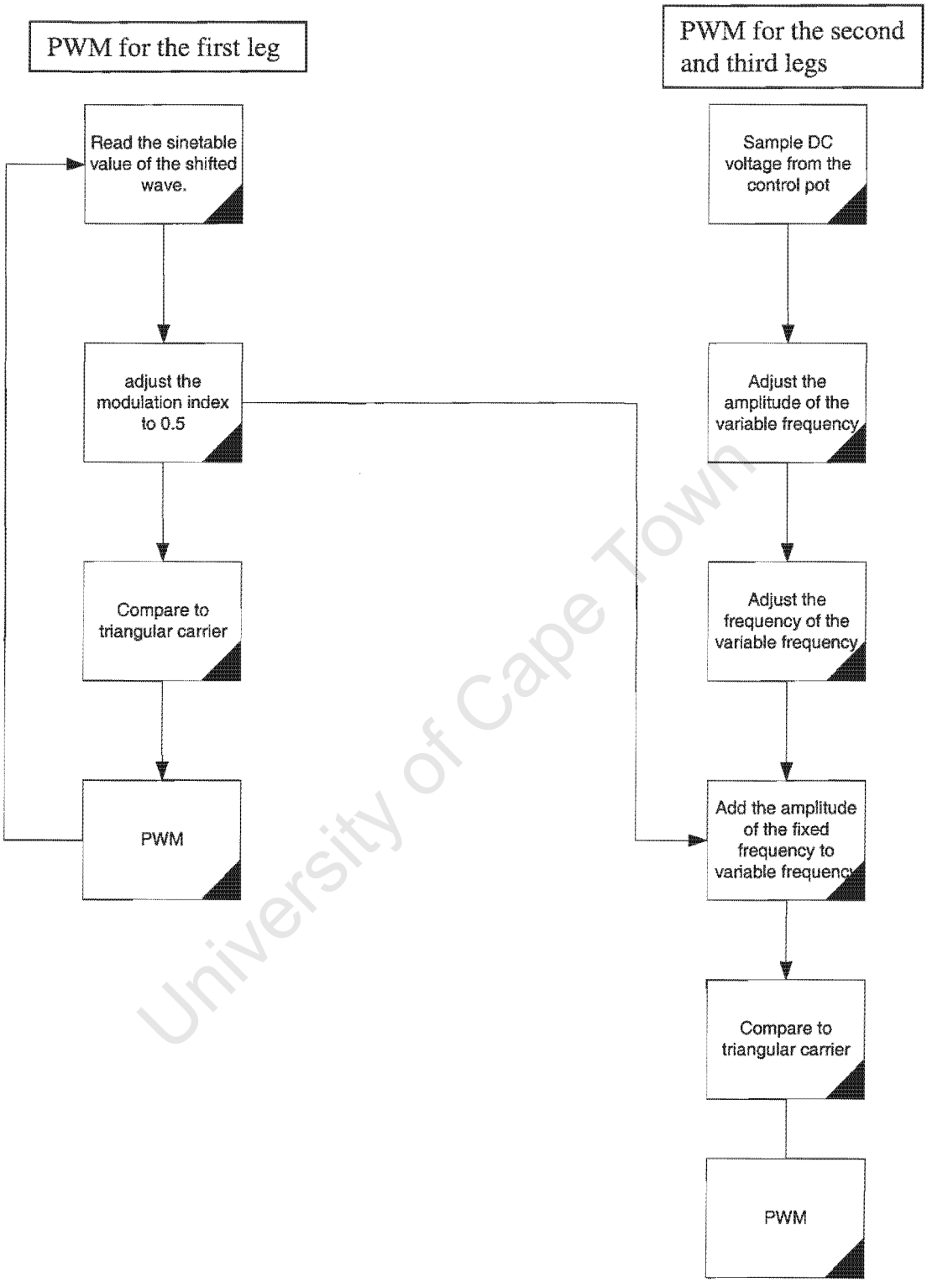


Figure 6.4 Flow chart for the PWM generation algorithim

CHAPTER 7

EXPERIMENTAL RESULTS

7.1 THE FRONT END RECTIFIER

When examining the first and second legs of the convertor, it is evident that the DC bus voltage should be high enough to accommodate the peak of the fundamentals of the fixed frequency and variable frequency. The modulation index and phase shift of the fixed frequency at the center point of the first leg determines the DC bus voltage.

There should be a method of choosing the correct DC bus voltage based on the voltage requirements of the load, the magnitude of the voltage source and the modulation index of the fixed frequency. From the results in chapter 4.1.2 and 4.1.3 it was concluded that at unity power factor the DC bus voltage was inversely proportional to the modulation index for small values of δ. This is also found when examining equation 7. This implies that if the modulation index is less than 1 then the DC bus voltage will be much larger. In fact a modulation index of 0.5 results in a minimum DC bus voltage that is 4 times the value of the peak source voltage. The maximum DC bus voltage is limited by the capacitor and semiconductor voltage ratings of the devices. This implies that there is a limit to the minimum modulation index used in the first leg of the convertor.

When examining the second and third legs of the convertor it is evident that there are two modulation indexes. The first index is that of the fixed frequency that charges up the DC bus. The second index is that of the variable frequency that controls the magnitude of the output voltage. The sum of these two indexes should not exceed 1 if over-modulation is to be avoided. It is therefore evident that in order to maximize the output voltage, you have to minimize the modulation index of the fixed frequency. This causes a problem because the DC bus voltage needed is determined by the modulation index of the fixed frequency. A decrease the modulation index of the fixed frequency will increase the DC

bus voltage. For this reason the modulation index of the fixed frequency was kept constant at a half. The maximum modulation index of the variable frequency was limited to half. This ensured a minimum DC bus voltage for a maximum output voltage.

7.1.1 CALCULATIONS FOR THE INDUCTANCE

In the experimental setup the voltage source was chosen to be 100V RMS. The maximum output power of the convertor should be 1000W. The modulation index used for the first leg of the convertor was kept constant at 0.5.

The inducatance can be calculated using equation 8,

$$Tan(\delta) = \frac{2\sqrt{2}\pi F L P_{out}}{V^2}$$

P_{out}=1000W V=$\sqrt{2}$.100 V F=50Hz

$$Tan(\delta) = \frac{2.\sqrt{2}\pi.50.L1000}{(\sqrt{2}.100)^2}$$

$$Tan(\delta) = 22.2L$$

In order to calculate the inductance the degree of phase shift has to be known. This can be done by examining equation 7,

$$V_d = \frac{2V}{ma\ Cos(\delta)}$$

The minimum DC bus required is found when δ is equal to 0. Using equation 7 the minimum DC bus voltage is calculated to be 565.7V . As the phase shift, δ, increases the DC bus voltage will increase at a rate of $\frac{1}{Cos(\delta)}$. We therefore have to choose a maximum DC bus and consequently a maximum phase shift. This is done by plotting the percentage increase in DC bus voltage from the minimum voltage against an increase in phase shift. Figure 7.1 shows the relation between the percentage increase in DC bus with an increasing phase shift.

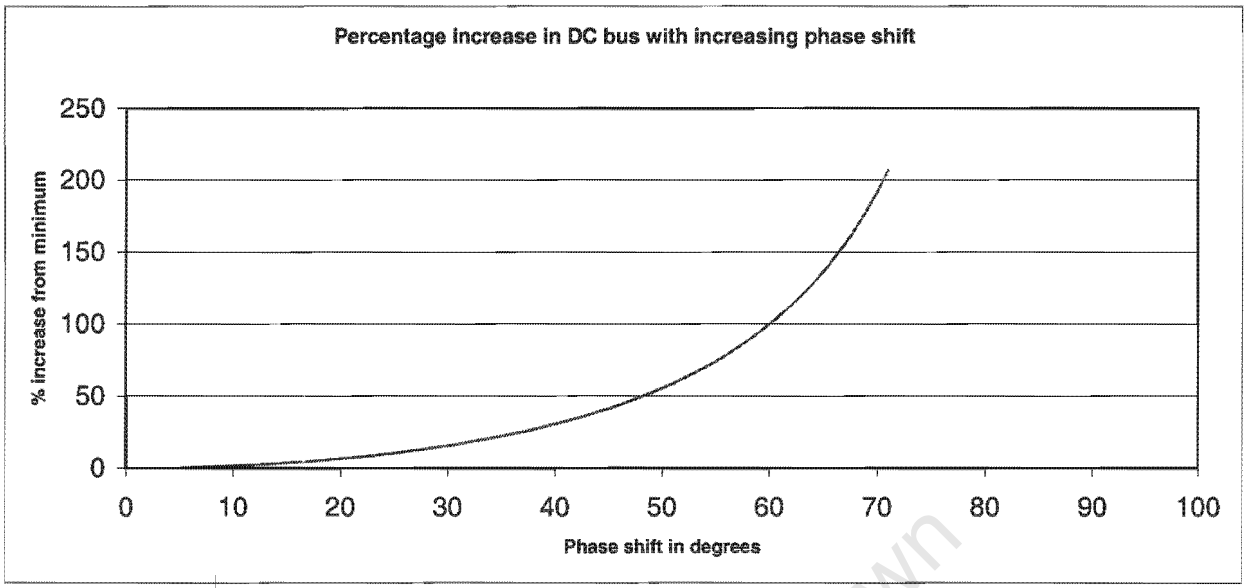


Figure 7.1 Percentage rise in DC bus with increasing phase shift δ

For the experimental setup the increase in DC bus voltage from the minimun voltage was chosen to be 10%. This corresponds to a maximum phase shift of 25^0. The minimum DC bus voltage would therefore be 565V and the maximum would be 621V.

Previously it has been shown that for the experimental setup, $Tan(\delta) = 22.2L$. The maximum phase shift has been chosen to be 25^0. Using $\delta = 25^0$ we can calculate the inductance to be 21mH.

The inductance of 21mH had to be made up by combining several high current inductors. The inductors used were all rated at 20A to 30A so that the I^2R losses could be minimal.

7.1.2 EXPERIMENTAL RESULTS USING A LOAD OF 100W

Using equation 8 we can determine the amount of phase shift needed to obtain an output power of 100W.

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}$$

$$Tan(\delta) = \frac{2\sqrt{2}\pi.50.21.10^{-3}100}{(\sqrt{2}.100)^2}$$

$$\delta = 2.6^0$$

The DC bus can be calculated using equation 7.

$$V_d = \frac{2V}{ma\ Cos(\delta)}$$

$$V_d = \frac{2\sqrt{2}.100}{\frac{1}{2}\ Cos(2.6)}$$

$$V_d = 566.3\,\text{V}$$

Using the experimental setup the following results were obtained.

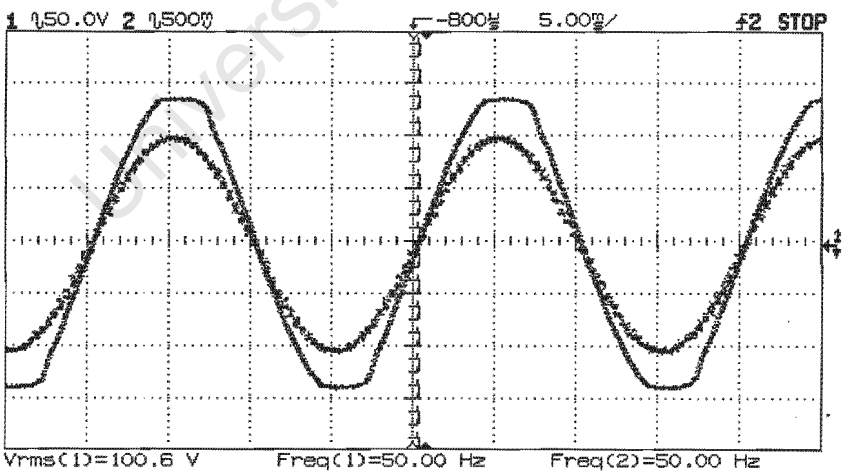


Figure 7.2 Phase shift at 100W output

Figure 7.2 shows the phase difference between the voltage source and the control signal of the fundamental in the first leg of the convertor. The flattened wave is the voltage source.

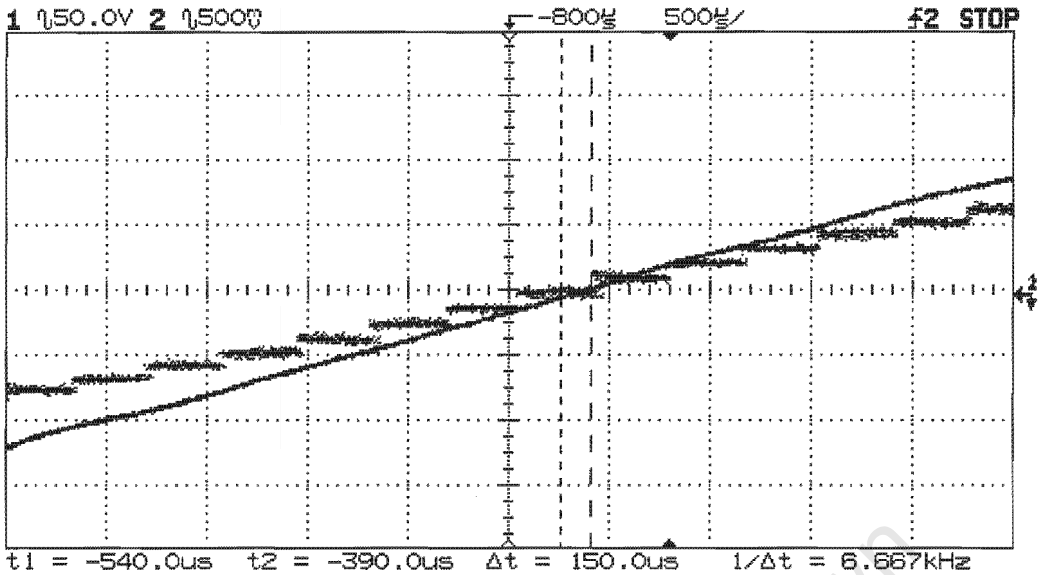


Figure 7.3 Phase shift at 100W (magnified)

Figure 7.3 shows a magnified view of the zero crossing points. From the diagram the phase shift is measured to be 150uS. Converting this to degrees results in a phase shift of 3^0. This correlates with the calculated value of 2.7^0.

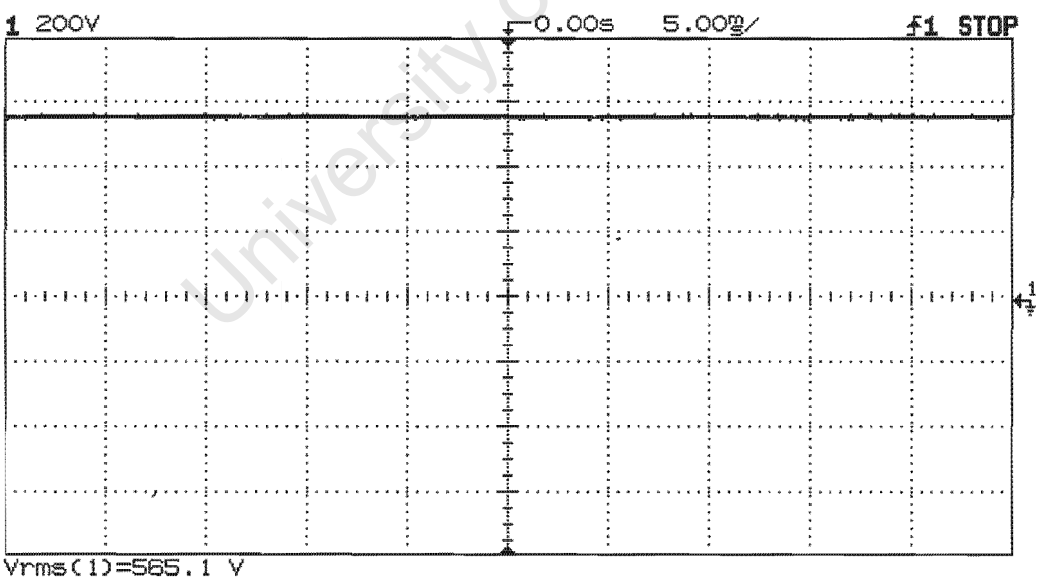


Figure 7.4 DC bus voltage at 100W output

Figure 7.4 shows the DC bus voltage at a load of 100W. The observed value at this load is 565V. This is aproximately the calculated value of 566.3V.

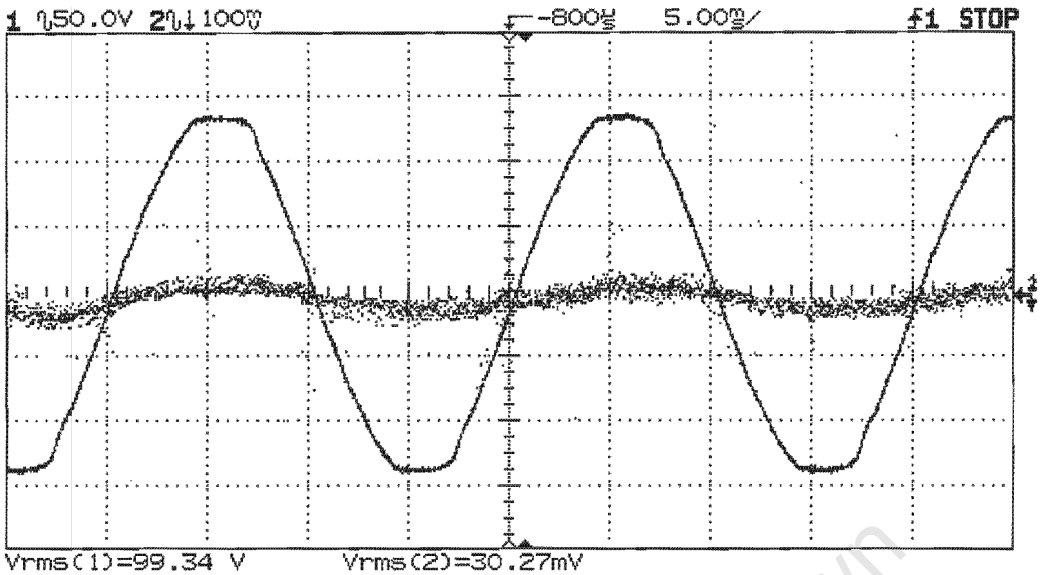


Figure 7.5 Source Voltage and Current at 100W load

Figure 7.5 shows that unity power factor has been achieved. The measured value for the current is 1.18A. This corresponds to an input power of 118W. The effeciency of the convertor is therefore $\frac{100}{118} = 85\%$

7.1.3 EXPERIMENTAL RESULTS USING A LOAD OF 250W

Using equation 8 we can determine the amount of phase shift needed to obtain an output power of 250W.

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}$$

$$Tan(\delta) = \frac{2\sqrt{2}\pi.50.21.10^{-3}250}{(\sqrt{2}.100)^2}$$

$$\delta = 6.7^0$$

The DC bus can be calculated using equation 7.

$$V_d = \frac{2V}{ma\ Cos(\delta)}$$

$$V_d = \frac{2\sqrt{2}.100}{\frac{1}{2}\ Cos(6.7)}$$

$$V_d = 569.6\,V$$

Using the experimental setup the following results were obtained.

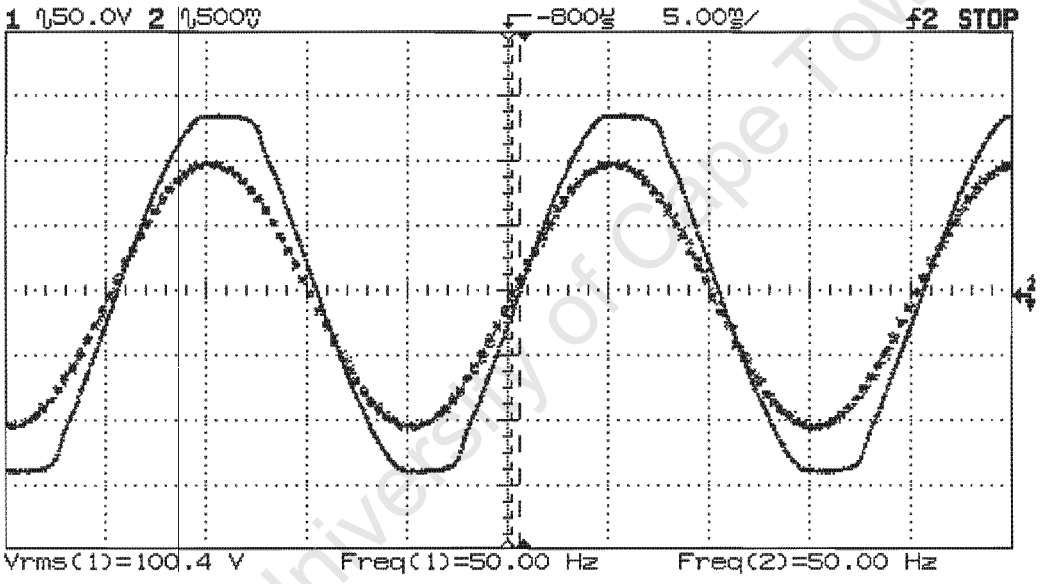
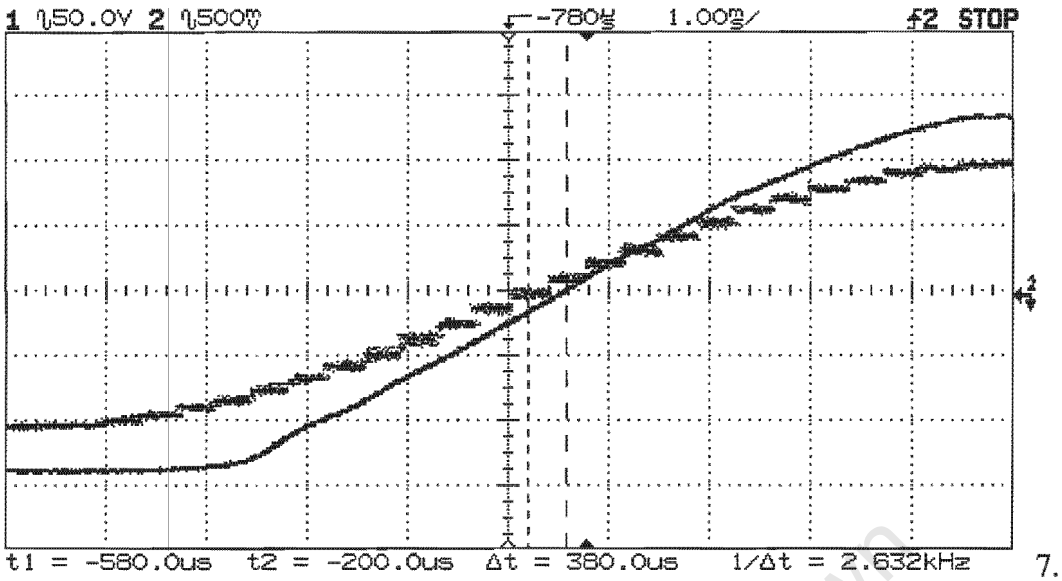


Figure 7.6 Phase shift at 250W output

Figure 7.6 shows the phase difference between the voltage source and the control signal of the fundamental in the first leg of the convertor. The flattened wave is the voltage source. The control signal was obtained by writing he instantaneous values of the phase shifted wave to the digital to analogue convertor.



7.

Figure 7.7 Phase shift at 250W (magnified)

Figure 7.4 shows a magnified view of the zero crossing points. From the diagram the phase shift is measured to be 380uS. Converting this to degrees results in a phase shift of 7^0. This correlates with the calculated value of 6.7^0.

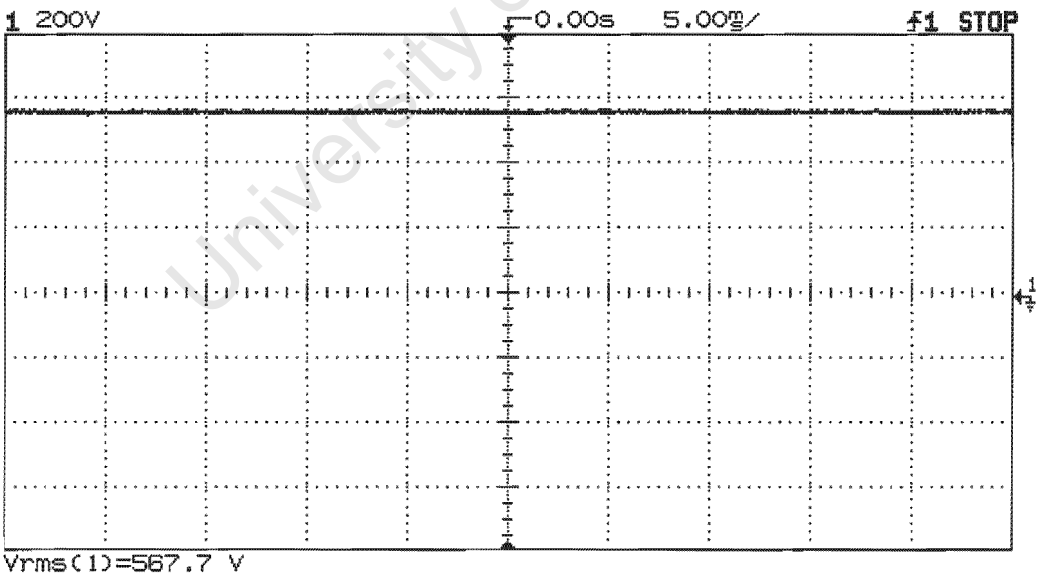


Figure 7.8 DC bus voltage at 250W output

Figure 7.4 shows the DC bus voltage at a load of 250W. The observed value at this load is 567V. This is aproximately the calculated value of 569.6V.

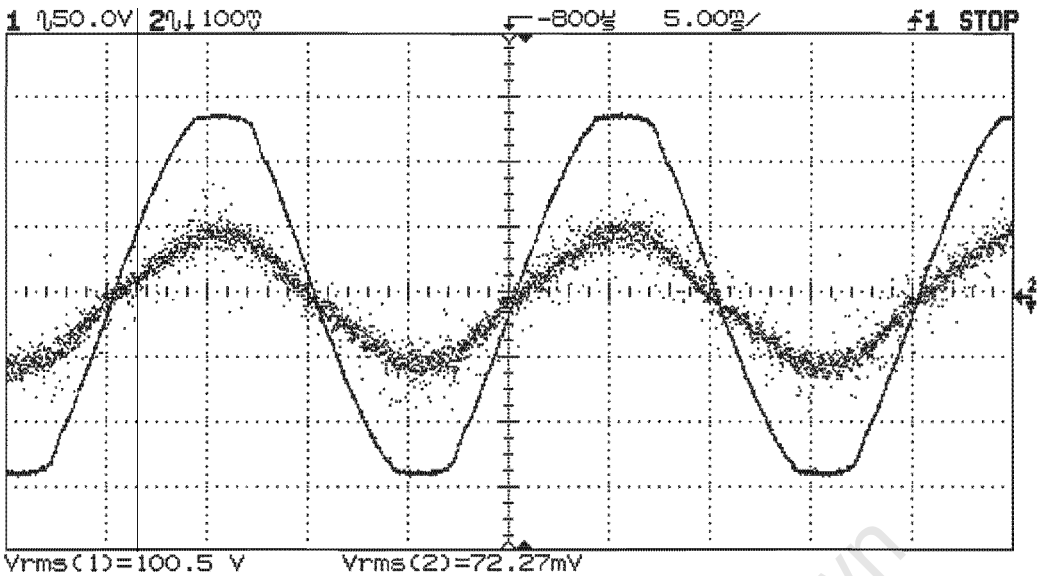


Figure 7.9 Source Voltage and Current at 250W load

Figure 7.9 shows that unity power factor has been achieved. The measured value for the current is 2.9A. This corresponds to an input power of 290W. The effeciency of the convertor is therefore $\frac{250}{290} = 86.2\%$

7.1.4 EXPERIMENTAL RESULTS USING A LOAD OF 500W

Using equation 8 we can determine the amount of phase shift need to obtain an output power of 500W.

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}$$

$$Tan(\delta) = \frac{2\sqrt{2}\pi.50.21.10^{-3}500}{(\sqrt{2}.100)^2}$$

$$\delta = 13.1^0$$

The DC bus can be calculated using equation 7.

$$V_d = \frac{2V}{ma\ Cos(\delta)}$$

$$V_d = \frac{2\sqrt{2}.100}{\frac{1}{2}\ Cos(13.1)}$$

$$V_d = 580\,\text{V}$$

Using the experimental setup the following results were obtained.

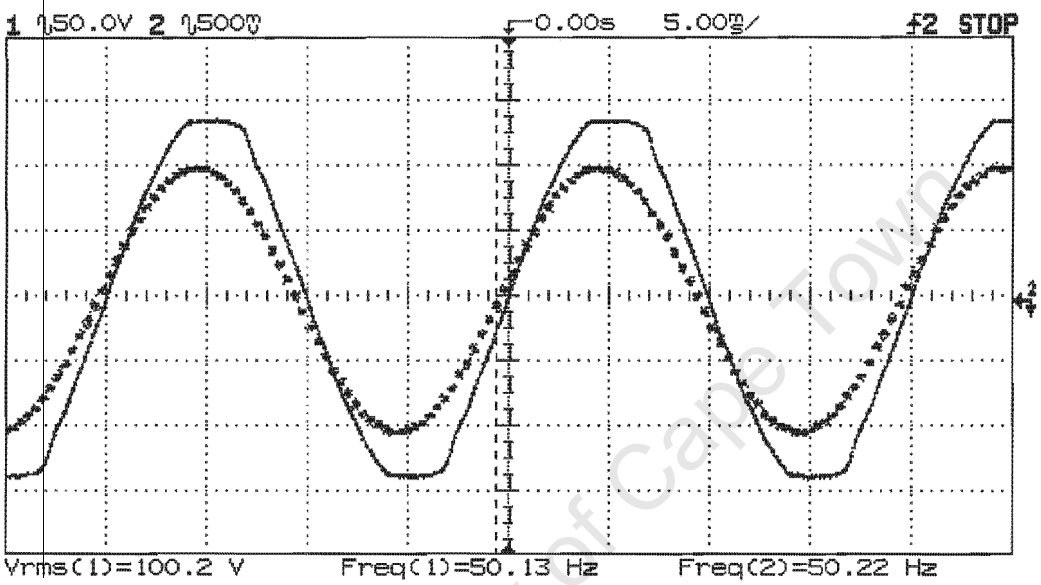


Figure 7.10 Phase shift at 500W output

Figure 7.10 shows the phase difference between the voltage source and the control signal of the fundamental in the first leg of the convertor. The flattened wave is the voltage source.

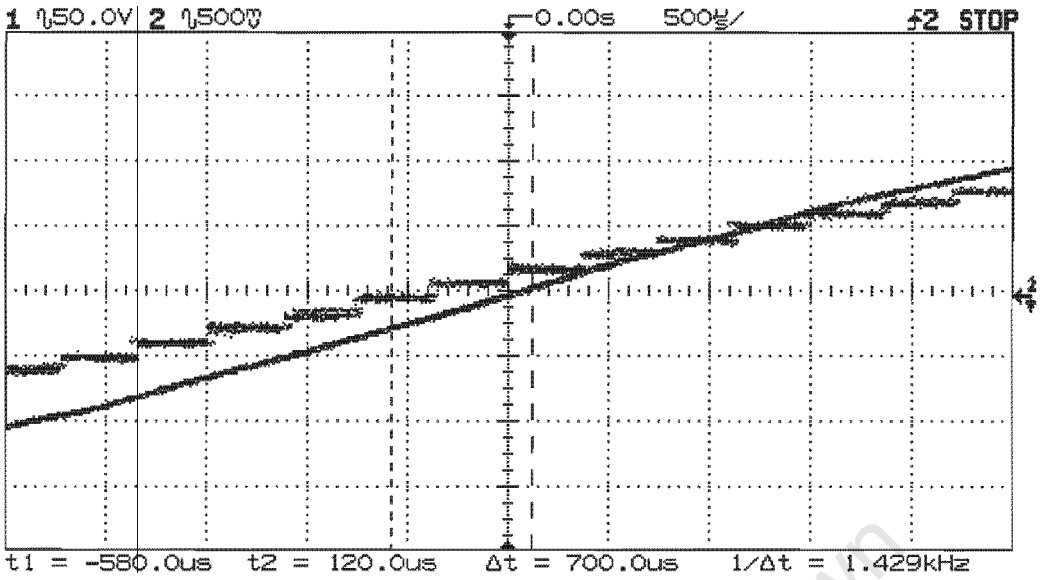


Figure 7.11 Phase shift at 500W (magnified)

Figure 7.11 shows a magnified view of the zero crossing points. From the diagram the phase shift is measured to be 700uS. Converting this to degrees results in a phase shift of 12.6^0. This correlates with the calculated value of 13.1^0.

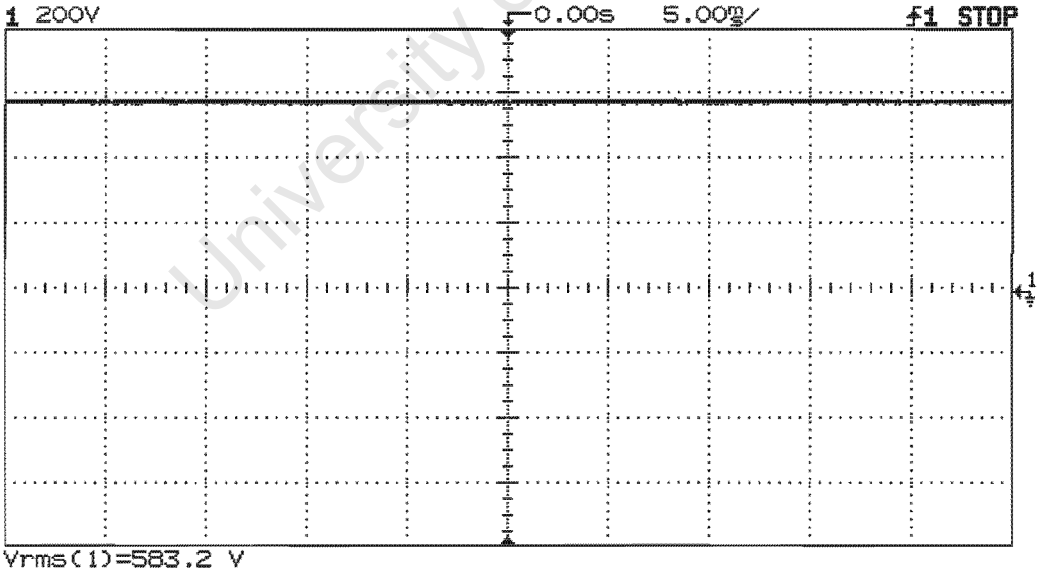


Figure 7.12 DC bus voltage at 500W output

Figure 7.12 shows the DC bus voltage at a load of 500W. The observed value at this load is 583V. This is aproximately the calculated value of 580V.

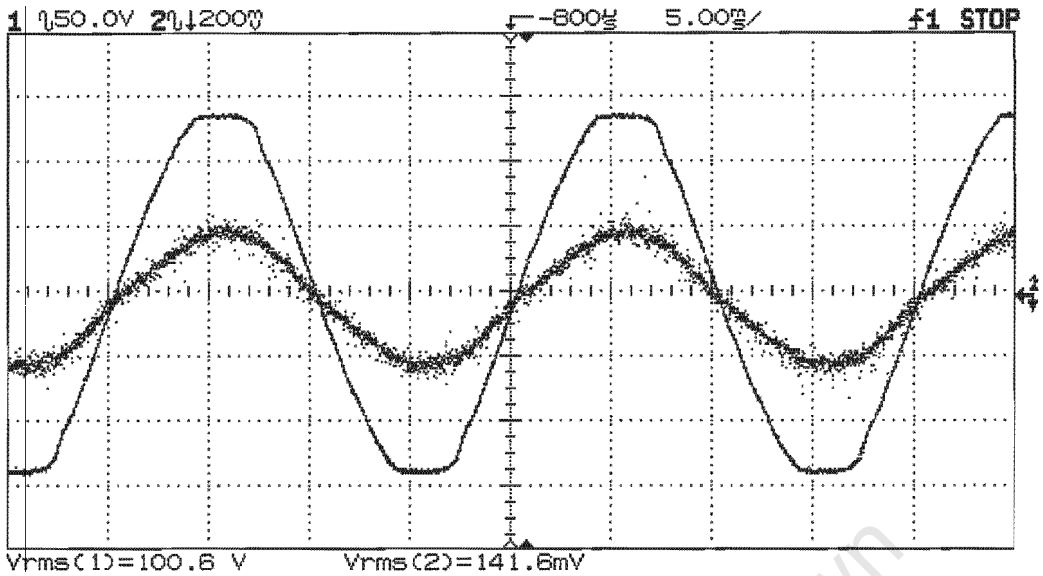


Figure 7.13 Source Voltage and Current at 500W load

Figure 7.13 shows that unity power factor has been achieved. The measured value for the current is 5.8A. This corresponds to an input power of 583W. The effeciency of the convertor is therefore $\frac{500}{583} = 86.2\%$

7.1.5 EXPERIMENTAL RESULTS USING A LOAD OF 750W

Using equation 8 we can determine the amount of phase shift need to obtain an output power of 750W.

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}$$

$$Tan(\delta) = \frac{2\sqrt{2}\pi.50.21.10^{-3}750}{(\sqrt{2}.100)^2}$$

$$\delta = 19.3^0$$

The DC bus can be calculated using equation 7.

$$V_d = \frac{2V}{ma\ Cos(\delta)}$$

$$V_d = \frac{2\sqrt{2}.100}{\frac{1}{2}\ Cos(13.1)}$$

$$V_d = 599\,V$$

Using the experimental setup the following results were obtained.

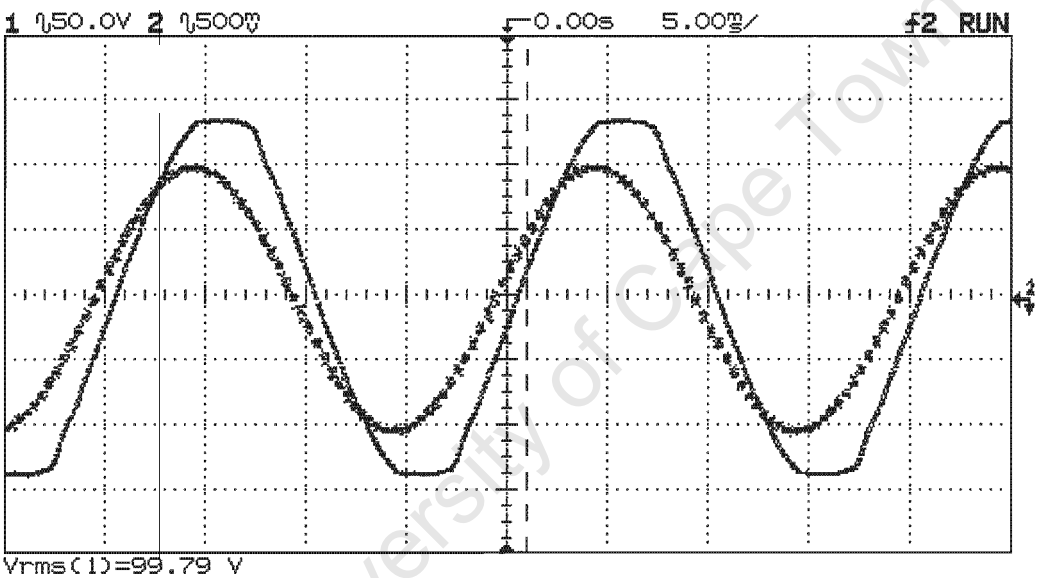


Figure 7.14 Phase shift at 750W output

Figure 7.14 shows the phase difference between the voltage source and the control signal of the fundamental in the first leg of the convertor. The flattened wave is the voltage source.

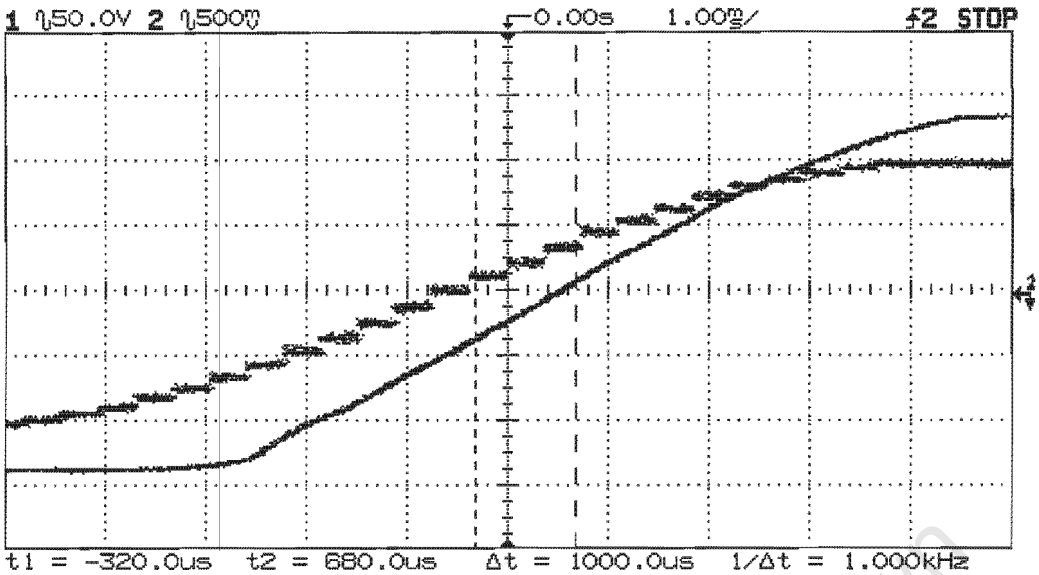


Figure 7.15 Phase shift at 750W (magnified)

Figure 7.15 shows a magnified view of the zero crossing points. From the diagram the phase shift is measured to be 1000uS. Converting this to degrees results in a phase shift of 18^0. This correlates with the calculated value of 19.3^0.

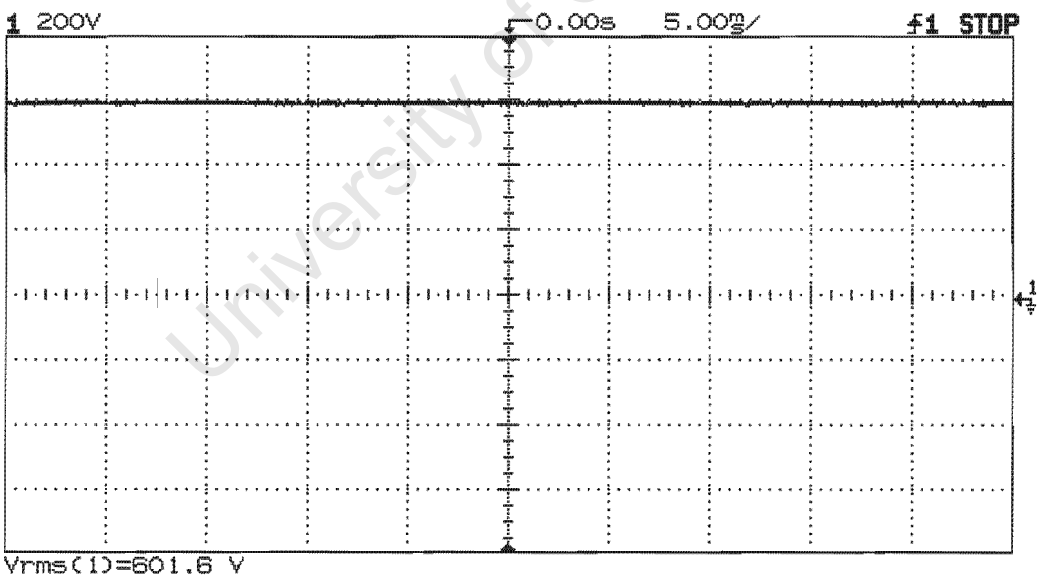
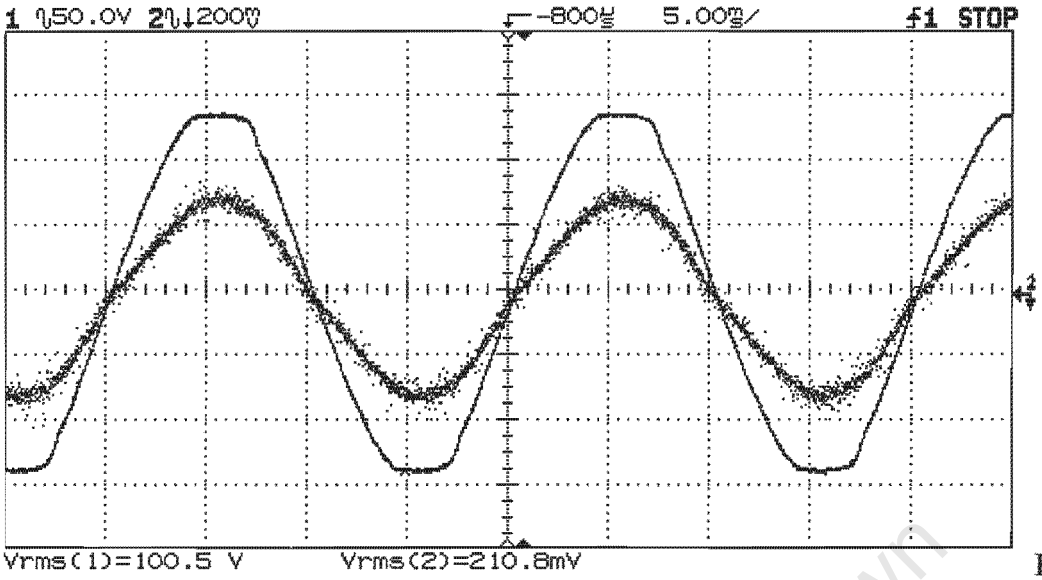


Figure 7.16 DC bus voltage at 750W output

Figure 7.16 shows the DC bus voltage at a load of 750W. The observed value at this load is 601.6V. This is aproximately the calculated value of 599V.



Figure

Figure 7.17 Source Voltage and Current at 750W load

Figure 7.17 shows that unity power factor has been achieved. The measured value for the current is 8.7A. This corresponds to an input power of 875W. The effeciency of the convertor is therefore $\frac{750}{875} = 85.7\%$

7.1.6 SUMMARY OF THE RESULTS OBTAINED

Output power	Measured Phase shift	Calculated Phase Shift	Measured DC Bus Voltage	Calculated DC Bus Voltage
100W	3^0	2.6^0	565	566.3
250W	7^0	6.7^0	567	569.6
500W	12.6^0	13.1^0	583	580
750W	18^0	19.3^0	601.6	599

Table 4

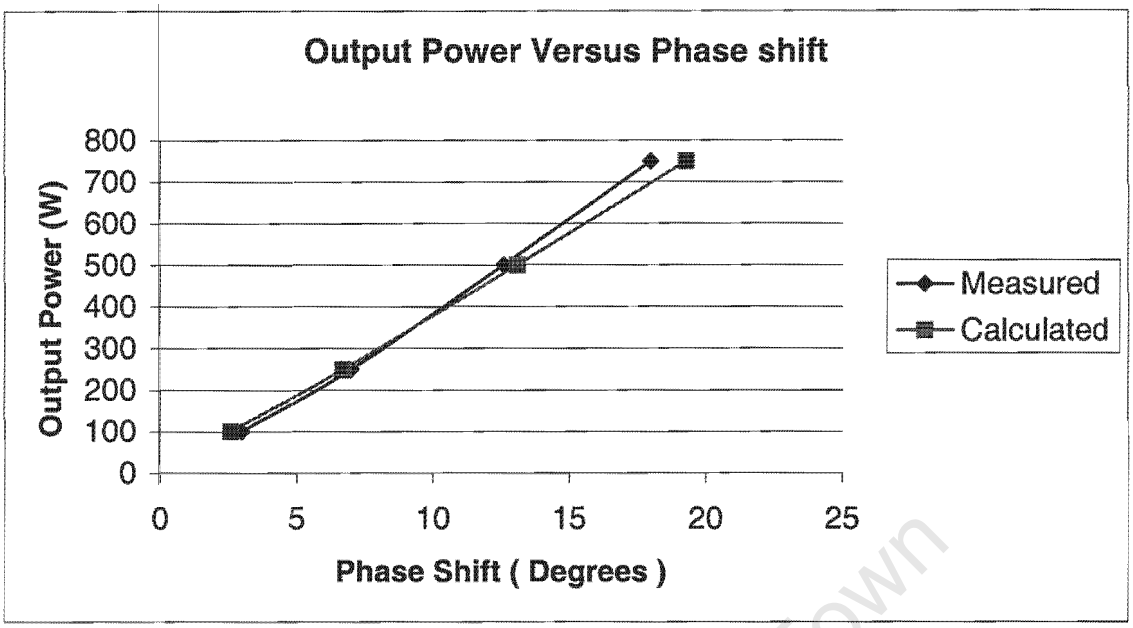


Figure 7.18 A plot of Output power versus the Phase shift

Figure 7.18 Shows the relationship between the measured and calculated values. From the figure we can observe that the ouput power is linearly proportional to the phase shift for values of δ less than 25^0.

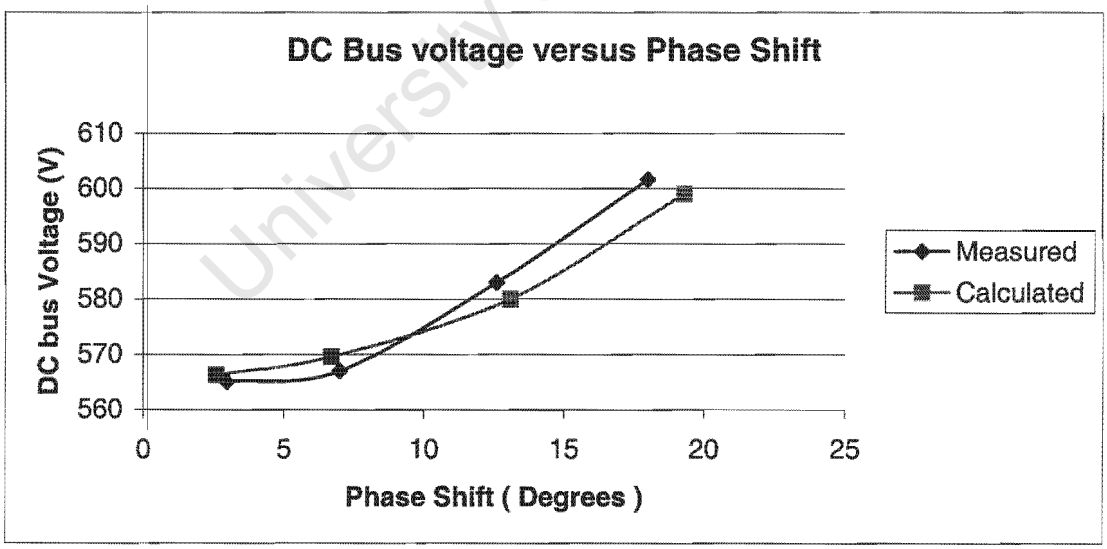


Figure 7.19 A plot of DC Bus voltage versus the Phase shift

Figure 7.19 shows the relationship between the calculated and measured DC Bus voltage. The measured values correlate with the calculated values.

7.2 THE VARIABLE SPEED DRIVE

The following results were obtained using a 110V line-line Delta motor. The source voltage was 100V. The the motor used was rated at 1 horse power.

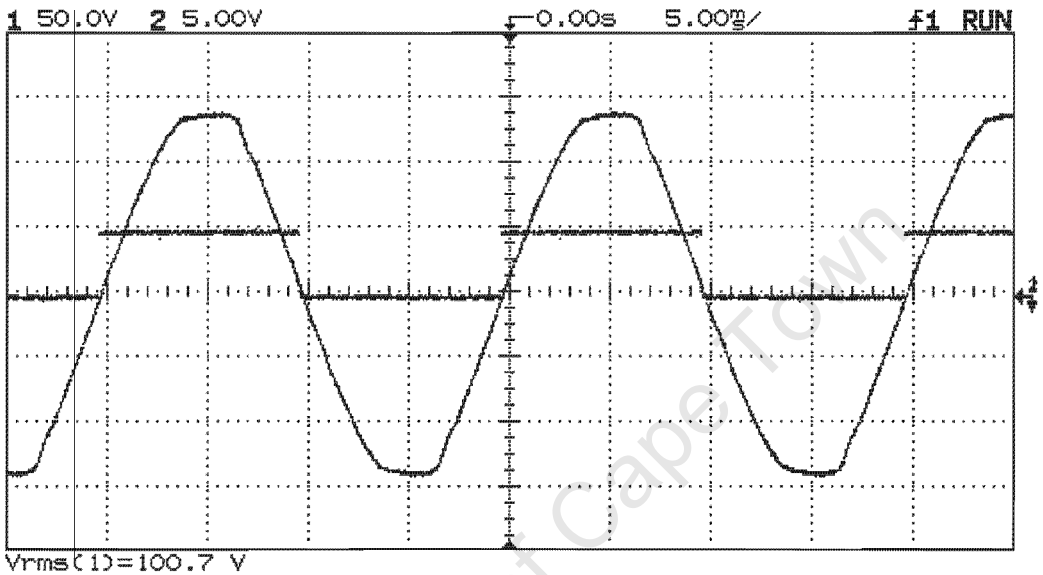


Figure 7.20 The Voltage source as well as signal triggering the DSP

From figure 7.20 we can see the distorted sinusoidal mains voltage (50 Hz).This is a typical capture of the voltage supply in the laboratory. The signal is sent to a zero crossing detector. The level of the square signal is limited to 5V so that it can interface with the digital signal processor. The square signal trigger's an external interrupt in the digital signal processor.

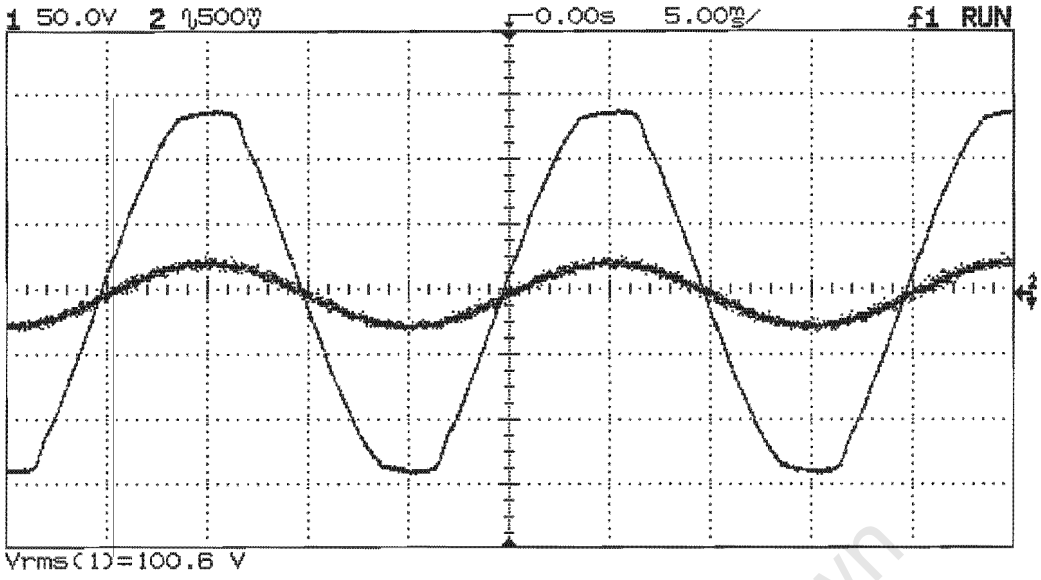


Figure 7.21 Voltage source as well as the phase lock control signal.

Figure 7.21 Shows the voltage source (flattened) as well as the generated phase locked control signal. The control signal was obtained by writing the values of the phase locked variable "X" to the digital to analogue convertor. The variable "X" can be found in the program listing in Appendix A.

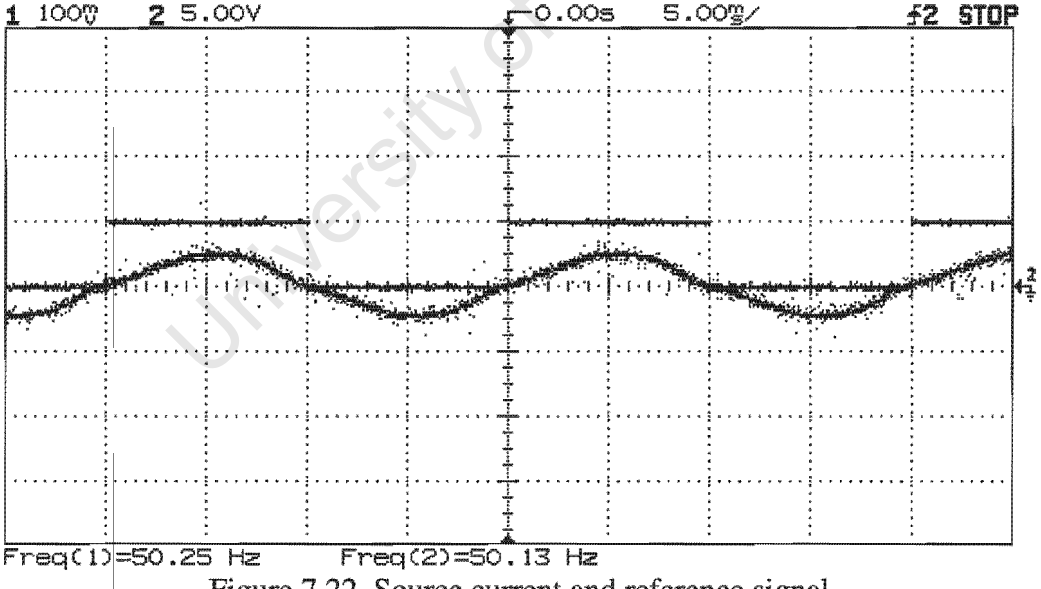


Figure 7.22. Source current and reference signal

From figure 7.22 the sinusoidal current is shown as well as the reference signal generated by the analogue circuitry. The square wave is used to trigger the external interrupts of the DSP. The current waveform was obtained by looking at the output of the LEM unit. The current was measured to be 1.5A

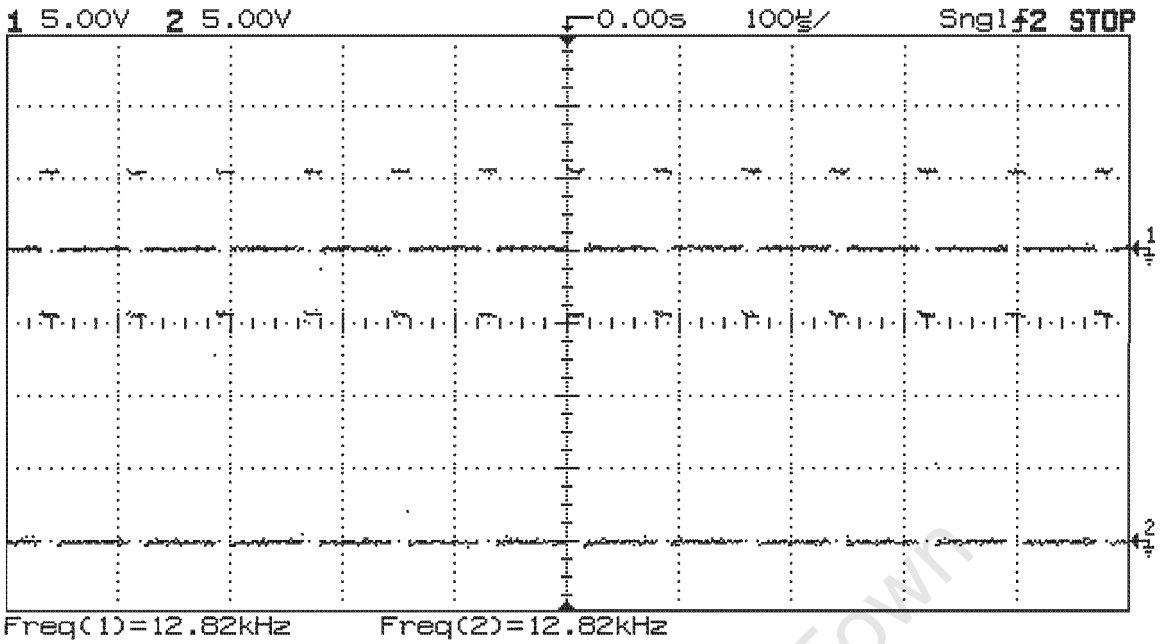


Figure 7.23 Output of the DSP and level shifter

Figure 7.23 shows the output PWM signal from the DSP board (5V) as well as the level shifter (15V). The measured switching frequency is 12.8KHz.

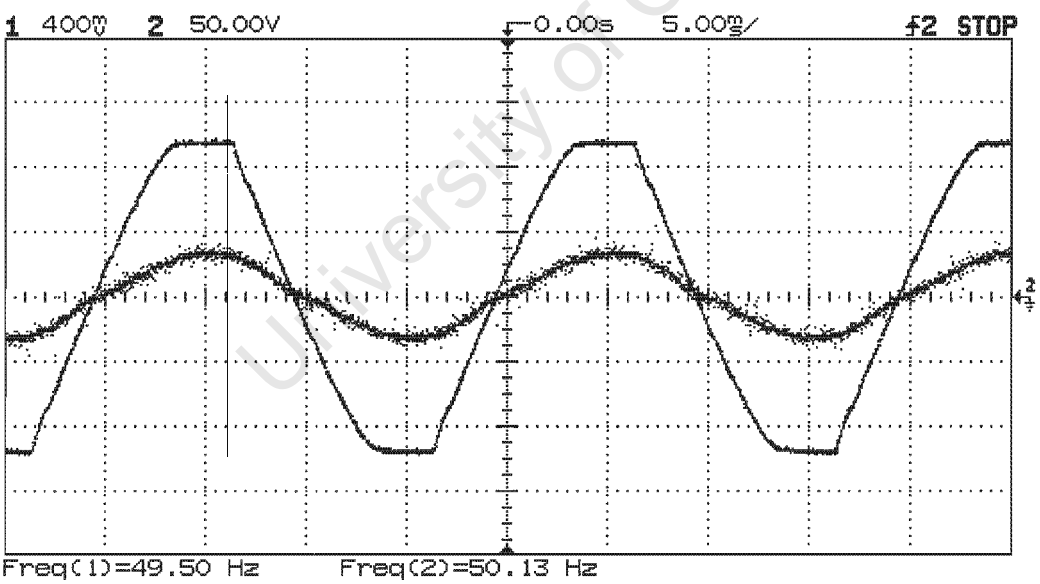


Figure 7.24. The voltage source and current drawn from the source.

Figure 7.24 shows that the voltage and current waveforms are in phase. This implies unity power factor operation. The current was measured to be 6.5A .This corresponds to approximately 650W being drawn from the source.

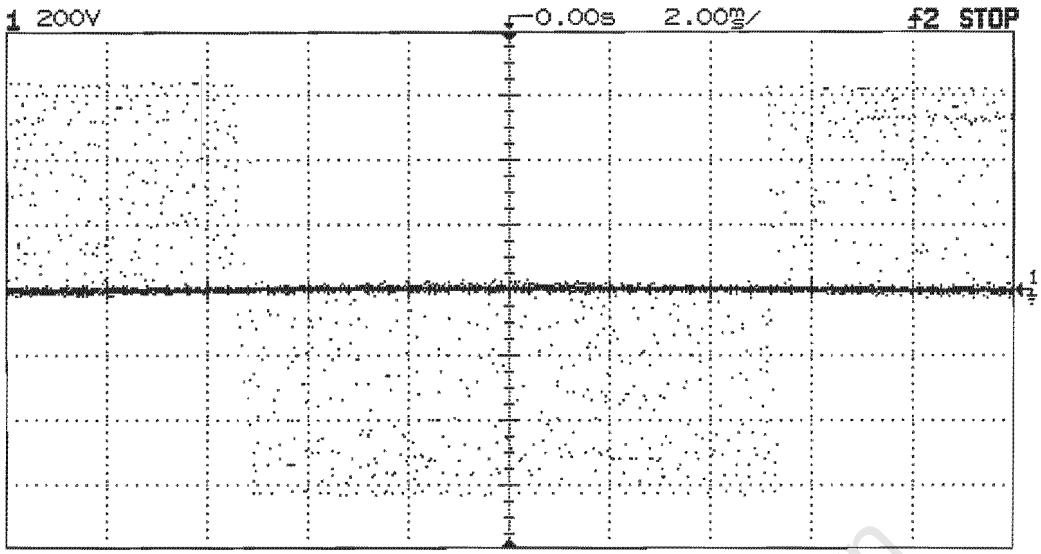


Figure 7.25. Line to line voltage

Figure 7.25 shows a 3 level symmetrical PWM line to line voltage seen by the motor. The image is not very clear due to the low sampling rate of the oscilloscope. It will be replaced as soon as a higher frequency oscilloscope is available. The voltage switches between +600V, 0V and -600V.

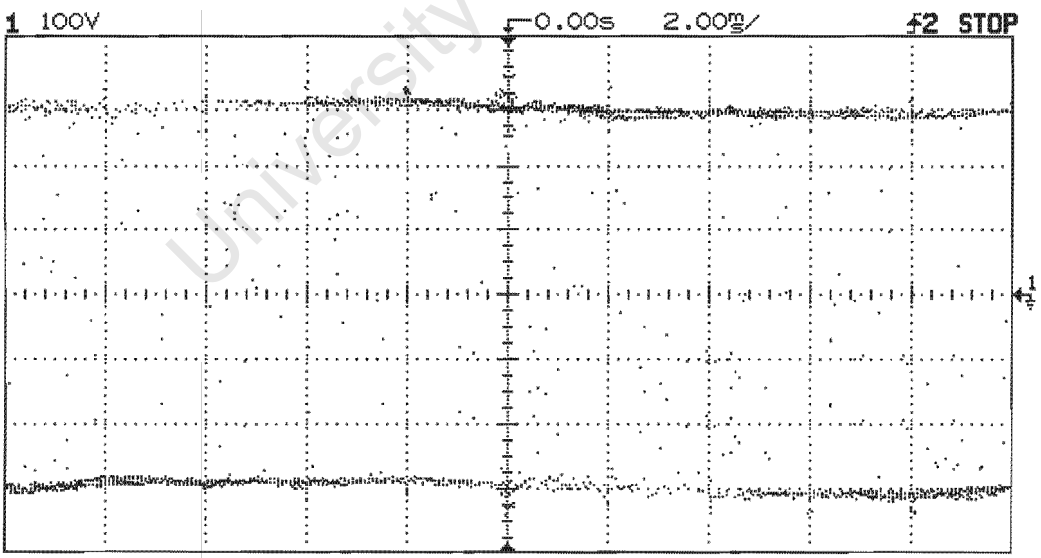


Figure 7.26 Line to Neutral voltage of the first leg of the converter.

Figure 7.26 shows the PWM signal at the midpoint of the first leg of the converter with respect to neutral. The voltage switches between +300V and -300V. This corresponds to a DC bus voltage of about 600V as shown in figure 7.27.

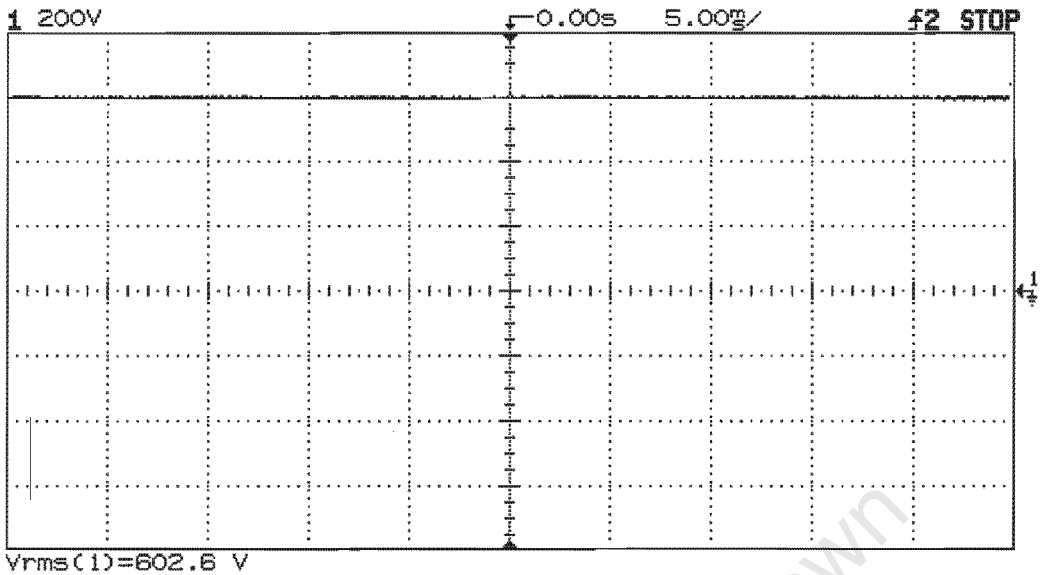


Figure 7.27 DC Bus Voltage

Figure 7.27 shows the DC voltage across both sets of capacitors at an output load of 504W.

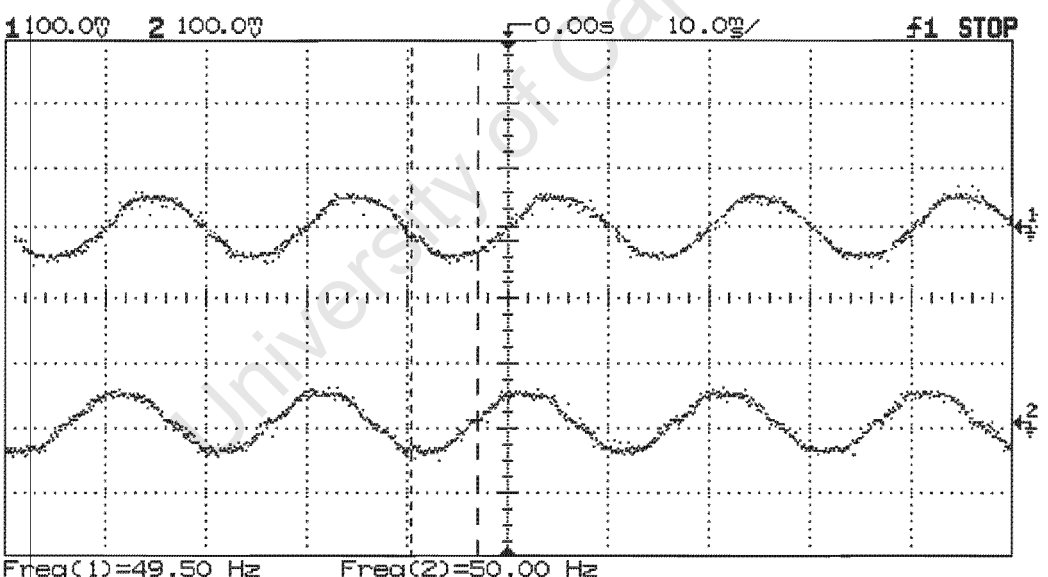


Figure 7.28. Motor line currents at 50Hz

Figure 7.11 shows the line currents of 2 phases at full rated voltage of 110V line to line and a frequency of 50Hz. The current was measured to be 1.13A per phase. The measured output power of the convertor was 503W. The power factor between the convertor and the motor was 0.92. The apparent output power of the convertor was 547VA. Referring to figure 7.24 , 650W was drawn from the supply. The efficiency of the convertor is therefore 78%. This efficiency could be higher if more accurate wattmeters were used.

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

The following conclusions can be drawn based on the simulations and experimental results.

The proposed topology for a single to three phase variable speed drive has been simulated and tested. The experimental results show a correlation with the simulations.

Based on the simulations results, the following conclusions can be drawn if a unity power factor is not required:

- The DC bus can be controlled by varying the phase shift δ.
- The smaller the inductance the larger the input current needed to achieve a desired DC bus voltage. See chapter 4.1.3
- A large inductance requires a larger phase shift and smaller input current. See chapter 4.1.3
- A large inductance will give a better power factor at the required DC bus voltage. See chapter 4.1.3

Based on the simulations and experimental results, the following conclusions can be drawn if a unity power factor is required :

A larger inductance requires more phase shift to obtain unity power factor. This is shown in the simulation of chapter 4.1.4. It is also shown by equation [8].

$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}$. If the output power were to be kept constant then,

$Tan(\delta) \propto L$. If the inductance L were increased then Tan(δ) would also increase and as a result δ will also increase.

The DC bus cannot be kept constant if unity power factor operation is desired. This is illustrated by equation [7].

$$V_d = \frac{2}{ma} VSec(\delta)$$

If the modulation index ma is kept constant then $V_d = \propto Sec(\delta)$. As δ increases , Sec(δ) increases and therefore the DC bus voltage will increase. The increase in δ is shown in the following diagram.

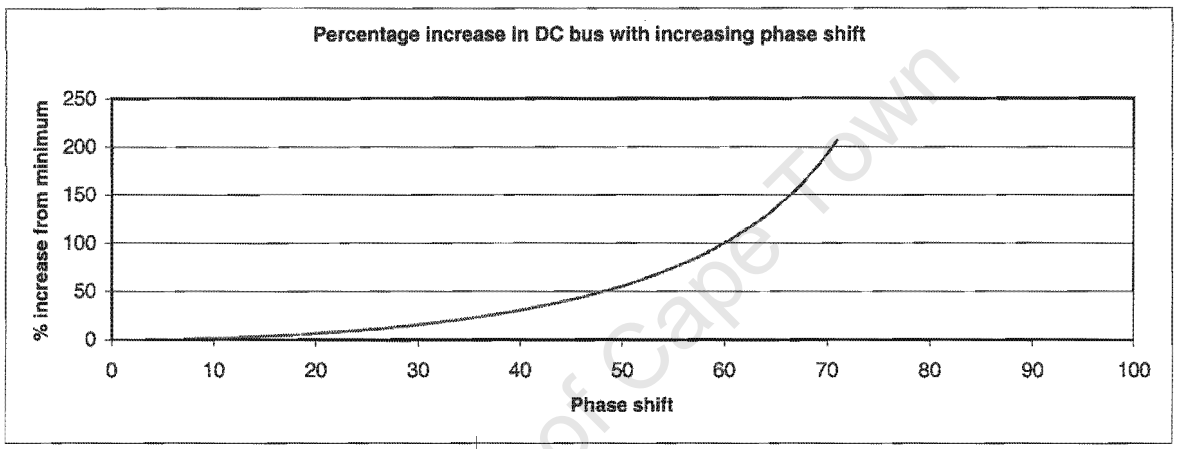


Figure 8.1 Percentage rise in DC bus with increasing phase shift δ

If the maximum rise in DC bus voltage, from the minimum when δ is approximately 0, is to be limited to 10% then the maximum phase shift should be limited to 25^0.
This was clearly observed in the simulations of chapter 4 as well as the experimental results of chapter 7.

The inductance used in the converter should be calculated using equation [8],

$$Tan(\delta) = \frac{2\sqrt{2}\pi FLP_{out}}{V^2}.$$

The maximum amount of phase shift should first be determined using figure 8.1. The inductance is therefore calculated based on the maximum acceptable amount of phase shift and DC bus voltage.

Referring to section 4.1.7 we observed that the size of the inductors does not affect the voltage at which unity power factor operation occurs. The size of the inductor only affects the amount of phase shift needed to obtain a unity power factor. This correlates with equations [7] and [8].

Unity power factor can be obtained if the modulation index is made less than 1. From figures 4.19 to 4.21 we can observe that when the modulation index was decreased to 0.5, the DC bus voltage at unity power factor operation was doubled. This correlates with equation [7] and shows that the DC bus is inversely proportional to the modulation index for small values of δ.

Unity power factor operation can never be achieved for any ARBITRARILY chosen DC bus voltage. For unity power factor, the DC bus must be maintained by using equation [7]. The minimum DC bus is obtained by making δ equal to zero. The resulting equation is as follows

$$V_d = \frac{2}{ma} VSec(\delta) \quad \text{if } \delta = 0 \text{ then}$$

$$V_{d\,\min} = \frac{2}{ma} V$$

If the DC bus voltage drops below the minimum then unity power factor operation cannot be achieved.

Instead of feeding back a high DC bus voltage and varying the phase angle δ to control the power we can use a different control strategy. It is important to realise that maintaining ANY ARBITRARY DC bus does not guarantee a unity power factor. Unity power factor will only occur at a DC bus voltage that is derived from equation [7].

The control strategy will therefore be as follows:
The power factor angle θ is fedback and the phase shift δ is adjusted until θ is equal to zero. This will guarantee a unity power factor. At unity power factor the DC bus voltage will always be determined by equation [7].

In the topology used in this project, the modulation index of the front end charger had to be less than 1 and kept constant. This results in a DC bus voltage that increases with an increase in phase shift. The rise in DC bus is shown in equation 7,

$$V_d = \frac{2}{ma} VSec(\delta).$$

If the modulation index were to be varied then the DC bus voltage can be kept constant. Space vector modulation allows over modulation to 115%. This method of modulation will facilitate the maintenance of a constant DC bus voltage.

The new topology has both advantages and disadvantages.

The advantages are:

- The drive draws a high quality sinusoidal current.
- The drive can do real time power factor correction and maintains a unity power factor within the maximum output power range.
- Power flow is bi-directional .
- The drive delivers a high quality three phase output current and voltage even when the source voltage was distorted.

The disadvantages are:

- The high DC bus voltage causes the voltage rating of the semiconductors and capacitors to be higher.
- Higher voltage rating components increase the overall cost of the convertor.

The advantages over the pervious topology by Prasad and Enjeti are :

- The line to line voltages are all symmetrical and therefore this system does not suffer from negative sequence harmonics.

REFERENCES

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APPENDIX A

PROGRAM LISTING

```
/*************************************************************************
This section of the program includes the library files "f240.h" and "math.h"
"f240.h" contains the default addresses of the registers found in the f240 DSP
chip. "math.h" contains the mathematical functions used by the program.
*************************************************************************/

#include "f240.h"
#include "math.h"



/*************************************************************************
This section declares the variables port00 to port03 as the DAC outputs.
Port0c is defined as the outputs to the LED's. Port0ffff defines the output
register that controls the wait state generator. These ports are only found
on the TMS320F240 evaluation board.
*************************************************************************/

ioport unsigned port00; /* DAC1 */
ioport unsigned port01; /* DAC2 */
ioport unsigned port02; /* DAC3 */
ioport unsigned port03; /* DAC4 */
ioport unsigned port04; /* DAC update */
ioport unsigned port0c; /* LEDS */
ioport unsigned port0ffff;  /* Wait State Gen */




/*************************************************************************
This section defines the variables used in the program.
loop - keeps the program running in a continuous loop.
x - index for the phase locked waveform
shift - index for the shifted waveform
y - index for the variable frequency on the second leg.
z - index for the variable frequency on the third leg.
lock - used to detect if the voltage phase lock has been achieved
t2inc - used to increase or decrease the variable frequency.
p1 - instantaneous value of fundamental of the first leg
p2 - instantaneous value of fundamental of the second leg
p3 - instantaneous value of fundamental of the third leg
dc - instantaneous value of the voltage read in from the A/D
amp - used to adjust the modulation index
period - stores the measured frequency of the mains
mains - an array that stores the sine lookup table
*************************************************************************/

unsigned int loop;
unsigned int x;
unsigned int shift;
```

```
unsigned int y;
unsigned int z;
unsigned int lock;
unsigned int t2inc;


float p1;
float p2;
float p3;
float dc;
float amp;
float period;
signed int mains[256];



/************************** MAIN PROGRAM ******************************/
The main program is divided into 3 sections namely :
1) Initialisation of variables
2) Initialisation of DSP registers
3) Main loop that controls the drive
**********************************************************************/

void main ()
{
      shift=64;  /* sets the phase shift to 90 degrees */
      loop=1;
      p1=0;
      x=0;
      y=0;
      z=42;     /*  locks the phase between the variable frequency to 60*/
      dc=1;
      t2inc=0;
      period=0;

      init_sintable();   /* calls the procedure to setup the lookup table */


      WDCR=0X006F;       /* disable the watch dog */

      asm(" .include f240asm.h");
      asm(" setc INTM");  /*   disable interrupts */

      IMR=0x0027;         /* Unmasks the interrupts */
      XINT1CR=0x0001;     /* enables the external interrupt 1 */
      XINT2CR=0x0003;     /* enables the external interrupt 2 */

      EVIMRA=0x0080;     /* unmask the timer 1 interrupt */
      EVIMRB=0x0001;     /* unmask the timer 2 interrupt */
      EVIMRC=0x0000;

      EVIFRA=0x0000;    /* reset the interrupt flags */
      EVIFRB=0x0000;    /* reset the interrupt flags */
      EVIFRC=0x0000;    /* reset the interrupt flags */
```

```
      SYSCR=0x40C0;      /* setup the system control register */
      RTICR=0X0000;
      CKCR1=0x00BB;      /* setup the system clock */
      CKCR0=0x00C3;
      por‡0ffff=0x004;   /* setup the wait states  */


      DBTCON=0XAFE0;     /* setup the dead time */

      ACTR=0X0666;        /* setup the action control register */
      CMPR1=0x0000;       /* initialise the compare registers */
      CMPR2=0x0000;
      CMPR3=0x0000;

      COMCON=0X0207;    /* setup the compare modes ie PWM mode */
      COMCON|=0X8000;
      OCRA=0xFF01;       /* setup port A for 1 A/D input and 6 PWM outputs*/
      PADATDIR=0X0f0f;   /* sets the direction of port A */
      PBDATDIR=0X3F00;   /* sets the direction of port B */


      GPTCON=0x006A;     /* setup the general timer control */
      T1PR=0x0000;       /* timer 1 period */
      T1CNT=0x0000;      /* timer 1 count register */
      T1CON=0x2842;      /* timer 1 control register */

      T2PR=0x0000;       /* timer 2 period */
      T2CNT=0x0000;      /* timer 2 count register */
      T2CON=0x2842;      /* timer 2 control register */

      T3PR=0x0000;       /* timer 3 period */
      T3CNT=0x0000;      /* timer 3 count register */
      T3CON=0x1742;      /* timer 3 control setup */

      ADCTRL1=0XAC01;    /* initialises the A/D   */


 asm(" .include f240asm.h");
 asm(" clrc INTM");      /*  enable interrupts   */


while(loop!=0)
     {
/*  This is the main loop. It samples the dc voltage at the A/D. This
    value is save in the variables "amp" and "dc". The variable "amp"
    is used to scale the modulation index of the variable output frequency.
    The variable "dc" is used to modify the frequency of the output voltage.*/
         dc=ADCFIFO1;   /* sample the control pot voltage */
         amp=dc;        /* store the DC control value */
         amp=amp/11;    /* scale the stored DC value  */
         if(amp<=120)   /* set a minimum amplitude */
            amp=120;
         dc=dc/2;       /* scale control pot voltage */
     }

}
```

```
/************************** INTERRUPT DEFINITIONS *********************/

 void  c_int0(void)
  {
   main();
   }




void  c_int1(void)
  {
/*  This procedure is called when the DSP is triggered on the second external
    interrupt. The frequency of the mains is measured by Timer 3.This frequency
    is scaled so that the carrier frequency will always be 256 times the mains
    frequency. This ensures synchronous PWM. The frequency of the phase locked
    wave is set to be the same as the mains frequency. The phase difference
    is then determined and the frequency of the locked wave is adjusted until
    the two waves are in phase. It also updates the frequency of the variable
    output.                                                                  */

     T3CON &= 0xffbf;  /* stop timer */
     lock=x;           /* save the index of the locked wave */
     period=T3CNT;     /* save the period measured */
     T3CNT=0x0000;     /* reset the counter */
     T3CON=0x1742;     /* start timer 3 */
     period=period/4;  /* scale the frequency for the carrier */

   if(lock == 0 )
       { }
        else
         {
        if(lock<=127)
          {
           period++;
                 }
        if(lock > 128)
                {
           period--;
                    }
        T1PR=period;        /* update the timer 1 frequency */
          t2inc=period+dc;   /* scale the variable frequency */
          T2PR=t2inc;        /* update the timer2 frequency  */

          }


 }
```

```
void  c_int2(void)
  {

   asm(" .include f240asm.h");
   asm(" ldp      #IVRA/128");
   asm(" lacc     IVRA");

         T1CMPR=p1;    /* compare P1 to the carrier */
         p1=mains[shift]; /* instantaneous value of the phase shifted wave */

         p1=p1/340;    /*  approx 50% modulation index  */
         p1=p1+390;    /*       add a dc offset         */

         x++;         /* increment the index */
         shift++;     /* increment the index */

         if(x >= 255)   /* reset the index on overflow */
          {  x=0;
           }

         if(shift >= 255)  /* reset the index on overflow */
          {  shift=0;
           }
 }



void  c_int3(void)
  {

   asm(" .include f240asm.h");
   asm(" ldp      #IVRB/128");
   asm(" lacc     IVRB");


       CMPR2=p2; /* compare P2 to the carrier */
       CMPR3=p3; /* compare p3 to the carrier */

       p2=mains[y]; /* instantaneous value of the first variable frequency */
       p3=mains[z]; /* instantaneous value of the second variable frequency/*

       p2=p2/amp;    /* set the amplitude of the variable frequency */
       p2=p2+p1;     /* add the phase shifted wave */

       p3=p3/amp;   /* set the amplitude of the variable frequency */
       p3=p3+p1;    /* add the phase shifted wave */

       y++;         /* increment the index */
       z++;         /* increment the index */

       if(y >= 255)   /* reset the index on overflow */
          {  y=0;
               }
       if(z >= 255)   /* reset the index on overflow */
          {  z=0;
           }
   }
```

```
void  c_int4(void)
  {
   }
void  c_int5(void)
  {
   }


void  c_int6(void)
  {
/* This procedure is called when the DSP is triggered on the 2nd
   external interurpt. This corresponds to the zero crossing of the current
   waveform. The position of the X variable is check. If X = 0 it implies that
   unity power factor has been obtained, therefore no chages are made to the
   "shift" index. If 127 < x < 255, it implies that the current is leading the
   voltage and the "shift" variable is decresed. if 1 < X < 127, it implies that
   the voltage is leading the current and the "shift" variable is increased
   The phase shift is limited to +90 and -90 degrees.                    */

       if( (x==0))
         { }
           else
             {
               if( (x<=255)&& (x>127)  )
                  shift--;

             if( (x>=1) && (x<127))
                  shift++;
             }
if((shift>64)&&(shift< 127)) /* limit maximum positve shift to 90 degrees */
          shift=64;
if((shift>127)&&(shift<192))/* limit the minimum negative shift to -90 degrees*/
         shift=192;

 }
```

APPENDIX B

REGISTER DECLARATIONS

```
/* #ifndef __C240_H_
#define __C240_H_ */
/*********************************************************************/
/* Watchodg and Real time Interrupt Control Registers */
/*********************************************************************/
#define RTICNTR *(volatile unsigned int*) 0x7021
#define WDCNTR *(volatile unsigned int*) 0x7023
#define WDKEY *(volatile unsigned int*) 0x7025
#define RTICR *(volatile unsigned int*) 0x7027
#define WDCR *(volatile unsigned int*) 0x7029

#define IMR *(volatile unsigned int*) 0x0004
#define IFR *(volatile unsigned int*) 0x0006

/*********************************************************************/
/* pll Clock Registers */
/*********************************************************************/
#define CKCR0 *(volatile unsigned int*) 0x702B
#define CKCR1 *(volatile unsigned int*) 0x702D
#define OCRA *(volatile unsigned int*) 0x7090
#define OCRB *(volatile unsigned int*) 0x7092
#define PADATDIR *(volatile unsigned int*) 0x7098
#define PBDATDIR *(volatile unsigned int*) 0x709A

#define ISRA *(volatile unsigned int*) 0x7094

/*********************************************************************/
/* Definitions for SCI Module */
/*********************************************************************/
/* SCI communications control register */
#define SCICCR *(volatile unsigned int*) 0x7050
/* SCI control register */
#define SCICTL1 *(volatile unsigned int*) 0x7051
/* Baud rate select MSB */
#define SCIHBAUD *(volatile unsigned int*)0x7052
/* Baud rate select LSB */
#define SCILBAUD *(volatile unsigned int*)0x7053
/* Transmitter int. control and status reg*/
#define SCICTL2 *(volatile unsigned int*)0x7054
/* Receiver int. control and status reg */
#define SCIRXST *(volatile unsigned int*)0x7055
/* Receiver data buffer */
#define SCIRXEMU *(volatile unsigned int*)0x7056
/* Transmit data buffer */
#define SCIRXBUF *(volatile unsigned int*)0x7057
/* Transmit data buffer */
#define SCITXBUF *(volatile unsigned int*)0x7059
/* Port control register #2 */
#define SCIPC2 *(volatile unsigned int*)0x705E
/* Interrupt priority control register */
#define SCIPRI *(volatile unsigned int*)0x705F
```

```
/*********************************************************************/
/* Definitions for ADC Module */
/* structures are computed uncorrectly by the C Compiler v6.60 ! */
/* therefore following approach has to be used */
/*********************************************************************/
#define ADCTRL1 *(volatile unsigned int*) 0x7032 /* ADC Control register 1 */
#define ADCTRL2 *(volatile unsigned int*) 0x7034 /* ADC Control register 2 */
#define ADCFIFO1 *(volatile unsigned int*) 0x7036 /* ADC1 result FIFO */
#define ADCFIFO2 *(volatile unsigned int*) 0x7038 /* ADC2 result FIFO */
/*********************************************************************/
/* Definitions for EV Module */
/* structures are computed uncorrectly by the C Compiler v6.60 ! */
/*********************************************************************/
#define GPTCON *(volatile unsigned int*) 0x7400
#define T1CNT *(volatile unsigned int*) 0x7401
#define T1CMPR *(volatile unsigned int*) 0x7402
#define T1PR *(volatile unsigned int*) 0x7403
#define T1CON *(volatile unsigned int*) 0x7404
#define T2CNT *(volatile unsigned int*) 0x7405
#define T2CMPR *(volatile unsigned int*) 0x7406
#define T2PR *(volatile unsigned int*) 0x7407
#define T2CON *(volatile unsigned int*) 0x7408
#define T3CNT *(volatile unsigned int*) 0x7409
#define T3CMPR *(volatile unsigned int*) 0x740A
#define T3PR *(volatile unsigned int*) 0x740B
#define T3CON *(volatile unsigned int*) 0x740C
#define COMCON *(volatile unsigned int*) 0x7411
#define ACTR *(volatile unsigned int*) 0x7413
#define SACTR *(volatile unsigned int*) 0x7414
#define DBTCON *(volatile unsigned int*) 0x7415
#define CMPR1 *(volatile unsigned int*) 0x7417
#define CMPR2 *(volatile unsigned int*) 0x7418
#define CMPR3 *(volatile unsigned int*) 0x7419
#define SCMPR1 *(volatile unsigned int*) 0x741A
#define SCMPR2 *(volatile unsigned int*) 0x741B
#define SCMPR3 *(volatile unsigned int*) 0x741C
#define CAPCON *(volatile unsigned int*) 0x7420
#define CAPFIFO *(volatile unsigned int*) 0x7422
#define CAP1FIFO *(volatile unsigned int*) 0x7423
#define CAP2FIFO *(volatile unsigned int*) 0x7424
#define CAP3FIFO *(volatile unsigned int*) 0x7425
#define CAP4FIFO *(volatile unsigned int*) 0x7426

#define EVIMRA *(volatile unsigned int*) 0x742C
#define EVIMRB *(volatile unsigned int*) 0x742D
#define EVIMRC *(volatile unsigned int*) 0x742E
#define EVIFRA *(volatile unsigned int*) 0x742F
#define EVIFRB *(volatile unsigned int*) 0x7430
#define EVIFRC *(volatile unsigned int*) 0x7431
#define EVIVRA *(volatile unsigned int*) 0x7432
#define EVIVRB *(volatile unsigned int*) 0x7433
#define EVIVRC *(volatile unsigned int*) 0x7434
#define SYSCR *(volatile unsigned int*) 0x7018
#define PCDATDIR *(volatile unsigned int*) 0x709C
#define XINT1CR *(volatile unsigned int*) 0x7070
```

APPENDIX C

THE SINETABLE

```
/*********************************************************************
The values of the sine table is written to memory by the following
procedure
*********************************************************************/

void init_sintable()
{
mains [     0     ]     =     0     ;
mains [     1     ]     =     804   ;
mains [     2     ]     =     1608  ;
mains [     3     ]     =     2410  ;
mains [     4     ]     =     3212  ;
mains [     5     ]     =     4011  ;
mains [     6     ]     =     4808  ;
mains [     7     ]     =     5602  ;
mains [     8     ]     =     6393  ;
mains [     9     ]     =     7179  ;
mains [     10    ]     =     7962  ;
mains [     11    ]     =     8739  ;
mains [     12    ]     =     9512  ;
mains [     13    ]     =     10278 ;
mains [     14    ]     =     11039 ;
mains [     15    ]     =     11793 ;
mains [     16    ]     =     12539 ;
mains [     17    ]     =     13279 ;
mains [     18    ]     =     14010 ;
mains [     19    ]     =     14732 ;
mains [     20    ]     =     15446 ;
mains [     21    ]     =     16151 ;
mains [     22    ]     =     16846 ;
mains [     23    ]     =     17530 ;
mains [     24    ]     =     18204 ;
mains [     25    ]     =     18868 ;
mains [     26    ]     =     19519 ;
mains [     27    ]     =     20159 ;
mains [     28    ]     =     20787 ;
mains [     29    ]     =     21403 ;
mains [     30    ]     =     22005 ;
mains [     31    ]     =     22594 ;
mains [     32    ]     =     23170 ;
mains [     33    ]     =     23731 ;
mains [     34    ]     =     24279 ;
mains [     35    ]     =     24811 ;
mains [     36    ]     =     25329 ;
mains [     37    ]     =     25832 ;
mains [     38    ]     =     26319 ;
mains [     39    ]     =     26790 ;
mains [     40    ]     =     27245 ;
mains [     41    ]     =     27683 ;
mains [     42    ]     =     28105 ;
```

```
mains [     43    ]     =     28510 ;
mains [     44    ]     =     28898 ;
mains [     45    ]     =     29268 ;
mains [     46    ]     =     29621 ;
mains [     47    ]     =     29956 ;
mains [     48    ]     =     30273 ;
mains [     49    ]     =     30571 ;
mains [     50    ]     =     30852 ;
mains [     51    ]     =     31113 ;
mains [     52    ]     =     31356 ;
mains [     53    ]     =     31580 ;
mains [     54    ]     =     31785 ;
mains [     55    ]     =     31971 ;
mains [     56    ]     =     32137 ;
mains [     57    ]     =     32285 ;
mains [     58    ]     =     32412 ;
mains [     59    ]     =     32521 ;
mains [     60    ]     =     32609 ;
mains [     61    ]     =     32678 ;
mains [     62    ]     =     32728 ;
mains [     63    ]     =     32757 ;
mains [     64    ]     =     32767 ;
mains [     65    ]     =     32757 ;
mains [     66    ]     =     32728 ;
mains [     67    ]     =     32678 ;
mains [     68    ]     =     32609 ;
mains [     69    ]     =     32521 ;
mains [     70    ]     =     32412 ;
mains [     71    ]     =     32285 ;
mains [     72    ]     =     32137 ;
mains [     73    ]     =     31971 ;
mains [     74    ]     =     31785 ;
mains [     75    ]     =     31580 ;
mains [     76    ]     =     31356 ;
mains [     77    ]     =     31113 ;
mains [     78    ]     =     30852 ;
mains [     79    ]     =     30571 ;
mains [     80    ]     =     30273 ;
mains [     81    ]     =     29956 ;
mains [     82    ]     =     29621 ;
mains [     83    ]     =     29268 ;
mains [     84    ]     =     28898 ;
mains [     85    ]     =     28510 ;
mains [     86    ]     =     28105 ;
mains [     87    ]     =     27683 ;
mains [     88    ]     =     27245 ;
mains [     89    ]     =     26790 ;
mains [     90    ]     =     26319 ;
mains [     91    ]     =     25832 ;
mains [     92    ]     =     25329 ;
mains [     93    ]     =     24811 ;
mains [     94    ]     =     24279 ;
mains [     95    ]     =     23731 ;
mains [     96    ]     =     23170 ;
mains [     97    ]     =     22594 ;
mains [     98    ]     =     22005 ;
mains [     99    ]     =     21403 ;
```

```
mains [     100   ]     =     20787 ;
mains [     101   ]     =     20159 ;
mains [     102   ]     =     19519 ;
mains [     103   ]     =     18868 ;
mains [     104   ]     =     18204 ;
mains [     105   ]     =     17530 ;
mains [     106   ]     =     16846 ;
mains [     107   ]     =     16151 ;
mains [     108   ]     =     15446 ;
mains [     109   ]     =     14732 ;
mains [     110   ]     =     14010 ;
mains [     111   ]     =     13279 ;
mains [     112   ]     =     12539 ;
mains [     113   ]     =     11793 ;
mains [     114   ]     =     11039 ;
mains [     115   ]     =     10278 ;
mains [     116   ]     =     9512  ;
mains [     117   ]     =     8739  ;
mains [     118   ]     =     7962  ;
mains [     119   ]     =     7179  ;
mains [     120   ]     =     6393  ;
mains [     121   ]     =     5602  ;
mains [     122   ]     =     4808  ;
mains [     123   ]     =     4011  ;
mains [     124   ]     =     3212  ;
mains [     125   ]     =     2410  ;
mains [     126   ]     =     1608  ;
mains [     127   ]     =     804   ;
mains [     128   ]     =     0     ;
mains [     129   ]     =     -804  ;
mains [     130   ]     =     -1608 ;
mains [     131   ]     =     -2410 ;
mains [     132   ]     =     -3212 ;
mains [     133   ]     =     -4011 ;
mains [     134   ]     =     -4808 ;
mains [     135   ]     =     -5602 ;
mains [     136   ]     =     -6393 ;
mains [     137   ]     =     -7179 ;
mains [     138   ]     =     -7962 ;
mains [     139   ]     =     -8739 ;
mains [     140   ]     =     -9512 ;
mains [     141   ]     =     -10278      ;
mains [     142   ]     =     -11039      ;
mains [     143   ]     =     -11793      ;
mains [     144   ]     =     -12539      ;
mains [     145   ]     =     -13279      ;
mains [     146   ]     =     -14010      ;
mains [     147   ]     =     -14732      ;
mains [     148   ]     =     -15446      ;
mains [     149   ]     =     -16151      ;
mains [     150   ]     =     -16846      ;
mains [     151   ]     =     -17530      ;
mains [     152   ]     =     -18204      ;
mains [     153   ]     =     -18868      ;
mains [     154   ]     =     -19519      ;
mains [     155   ]     =     -20159      ;
mains [     156   ]     =     -20787      ;
```

```
mains [     157   ]     =     -21403     ;
mains [     158   ]     =     -22005     ;
mains [     159   ]     =     -22594     ;
mains [     160   ]     =     -23170     ;
mains [     161   ]     =     -23731     ;
mains [     162   ]     =     -24279     ;
mains [     163   ]     =     -24811     ;
mains [     164   ]     =     -25329     ;
mains [     165   ]     =     -25832     ;
mains [     166   ]     =     -26319     ;
mains [     167   ]     =     -26790     ;
mains [     168   ]     =     -27245     ;
mains [     169   ]     =     -27683     ;
mains [     170   ]     =     -28105     ;
mains [     171   ]     =     -28510     ;
mains [     172   ]     =     -28898     ;
mains [     173   ]     =     -29268     ;
mains [     174   ]     =     -29621     ;
mains [     175   ]     =     -29956     ;
mains [     176   ]     =     -30273     ;
mains [     177   ]     =     -30571     ;
mains [     178   ]     =     -30852     ;
mains [     179   ]     =     -31113     ;
mains [     180   ]     =     -31356     ;
mains [     181   ]     =     -31580     ;
mains [     182   ]     =     -31785     ;
mains [     183   ]     =     -31971     ;
mains [     184   ]     =     -32137     ;
mains [     185   ]     =     -32285     ;
mains [     186   ]     =     -32412     ;
mains [     187   ]     =     -32521     ;
mains [     188   ]     =     -32609     ;
mains [     189   ]     =     -32678     ;
mains [     190   ]     =     -32728     ;
mains [     191   ]     =     -32757     ;
mains [     192   ]     =     -32767     ;
mains [     193   ]     =     -32757     ;
mains [     194   ]     =     -32728     ;
mains [     195   ]     =     -32678     ;
mains [     196   ]     =     -32609     ;
mains [     197   ]     =     -32521     ;
mains [     198   ]     =     -32412     ;
mains [     199   ]     =     -32285     ;
mains [     200   ]     =     -32137     ;
mains [     201   ]     =     -31971     ;
mains [     202   ]     =     -31785     ;
mains [     203   ]     =     -31580     ;
mains [     204   ]     =     -31356     ;
mains [     205   ]     =     -31113     ;
mains [     206   ]     =     -30852     ;
mains [     207   ]     =     -30571     ;
mains [     208   ]     =     -30273     ;
mains [     209   ]     =     -29956     ;
mains [     210   ]     =     -29621     ;
mains [     211   ]     =     -29268     ;
mains [     212   ]     =     -28898     ;
mains [     213   ]     =     -28510     ;
```

```
mains [     214   ]     =     -28105      ;
mains [     215   ]     =     -27683      ;
mains [     216   ]     =     -27245      ;
mains [     217   ]     =     -26790      ;
mains [     218   ]     =     -26319      ;
mains [     219   ]     =     -25832      ;
mains [     220   ]     =     -25329      ;
mains [     221   ]     =     -24811      ;
mains [     222   ]     =     -24279      ;
mains [     223   ]     =     -23731      ;
mains [     224   ]     =     -23170      ;
mains [     225   ]     =     -22594      ;
mains [     226   ]     =     -22005      ;
mains [     227   ]     =     -21403      ;
mains [     228   ]     =     -20787      ;
mains [     229   ]     =     -20159      ;
mains [     230   ]     =     -19519      ;
mains [     231   ]     =     -18868      ;
mains [     232   ]     =     -18204      ;
mains [     233   ]     =     -17530      ;
mains [     234   ]     =     -16846      ;
mains [     235   ]     =     -16151      ;
mains [     236   ]     =     -15446      ;
mains [     237   ]     =     -14732      ;
mains [     238   ]     =     -14010      ;
mains [     239   ]     =     -13279      ;
mains [     240   ]     =     -12539      ;
mains [     241   ]     =     -11793      ;
mains [     242   ]     =     -11039      ;
mains [     243   ]     =     -10278      ;
mains [     244   ]     =     -9512 ;
mains [     245   ]     =     -8739 ;
mains [     246   ]     =     -7962 ;
mains [     247   ]     =     -7179 ;
mains [     248   ]     =     -6393 ;
mains [     249   ]     =     -5602 ;
mains [     250   ]     =     -4808 ;
mains [     251   ]     =     -4011 ;
mains [     252   ]     =     -3212 ;
mains [     253   ]     =     -2410 ;
mains [     254   ]     =     -1608 ;
mains [     255   ]     =     -804  ;
}
```

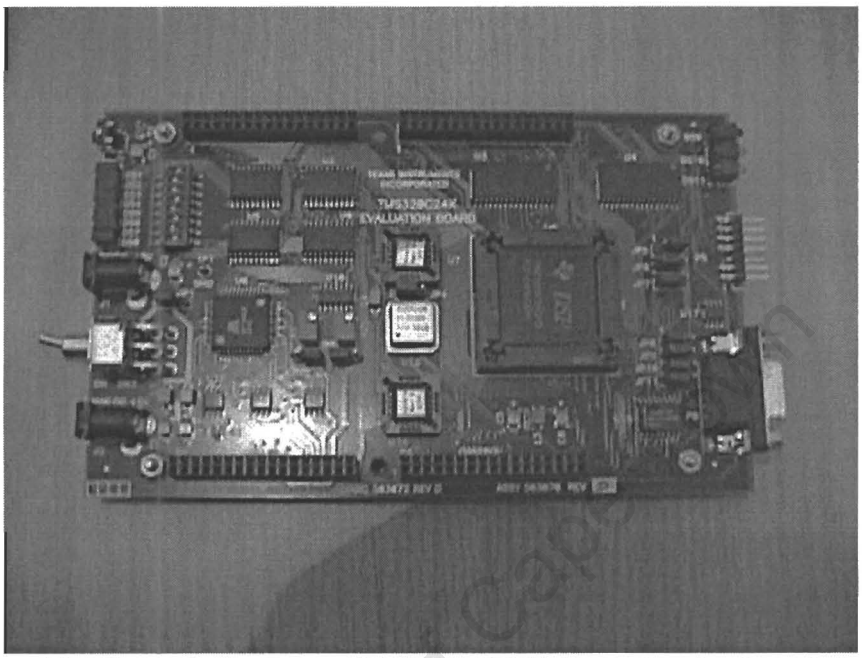
APPENDIX D

MEMORY MAP OF THE F240

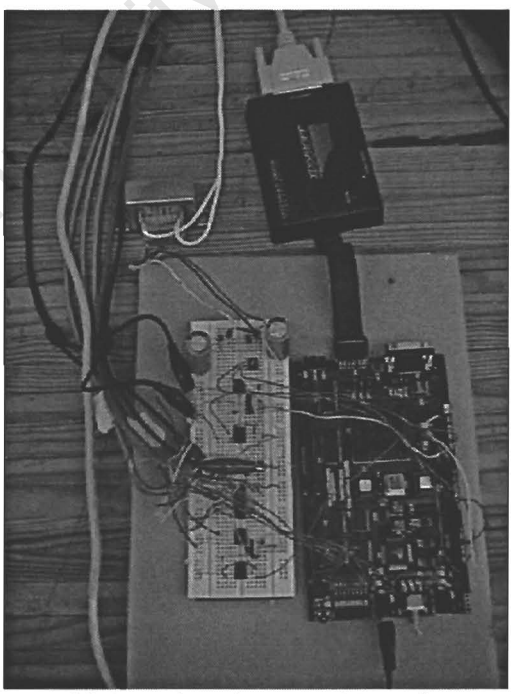
```
/************************************************************************/
/* File Name:       leds.cmd                                            */
/* Target System: C24x Evaluation Board                                 */
/*                                                                      */
/* Description:   A basic linker command file for the 'F240 device.     */
/*                This file is used by the linker to determine where    */
/*                certain sections of code should reside in memory.     */
/*                                                                      */
/* Revision:      1.00                                                  */
/************************************************************************/

/*----------------------------------------------------------------------*/
/*  LINKER COMMAND FILE - MEMORY SPECIFICATION for the F240             */
/*----------------------------------------------------------------------*/

MEMORY
{
    PAGE 0 :   VECS    : origin =    0h , length =   040h   /* VECTORS */
               PROG    : origin =   40h , length = 0FFC0h   /* PROGRAM */

    PAGE 1 :   MMRS    : origin =    0h , length =   060h   /* MMRS    */
               B2      : origin = 0060h , length =   020h   /* DARAM   */
               B0      : origin = 0200h , length =  0100h   /* DARAM   */
               B1      : origin = 0300h , length =  0100h   /* DARAM   */
               DATA    : origin = 8000h , length =  8000h   /* XDM     */
}

/*----------------------------------------------------------------------*/
/* SECTIONS ALLOCATION                                                  */
/*----------------------------------------------------------------------*/
SECTIONS
{
    .vectors : { } > VECS      PAGE 0   /* Interrupt vector table     */
    .reset   : { } > VECS      PAGE 0   /* Reset code                 */
    .start   : { } > PROG      PAGE 0   /* Code                       */
    .text    : { } > PROG      PAGE 0   /* Code                       */
    .data    : { } > PROG      PAGE 0   /* Initialization data tables */
    .mmrs    : { } > MMRS      PAGE 1   /* Memory mapped registers    */
    .bss     : { } > DATA        PAGE 1   /* Block B2                   */
    .blk0    : { } > B0        PAGE 1   /* Block B0                   */
    .blk1    : { } > B1        PAGE 1   /* Block B1                   */
    .blk2    : { } > B2        PAGE 1   /* Block B2                   */
    .blk3    : { } > DATA      PAGE 1   /* External data memory       */
}
```

APPENDIX E

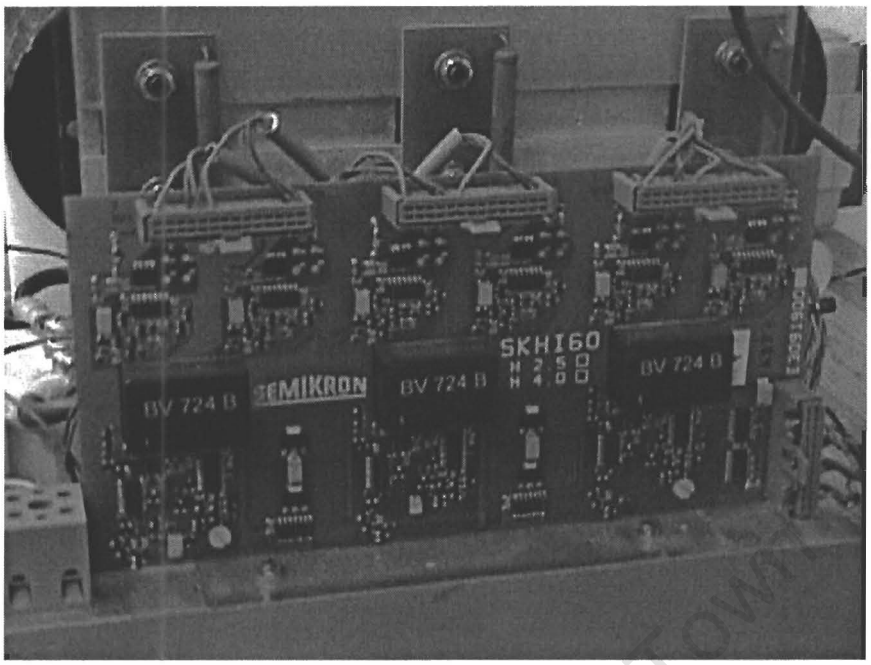
PHOTO'S OF THE EXPERIMENTAL SETUP



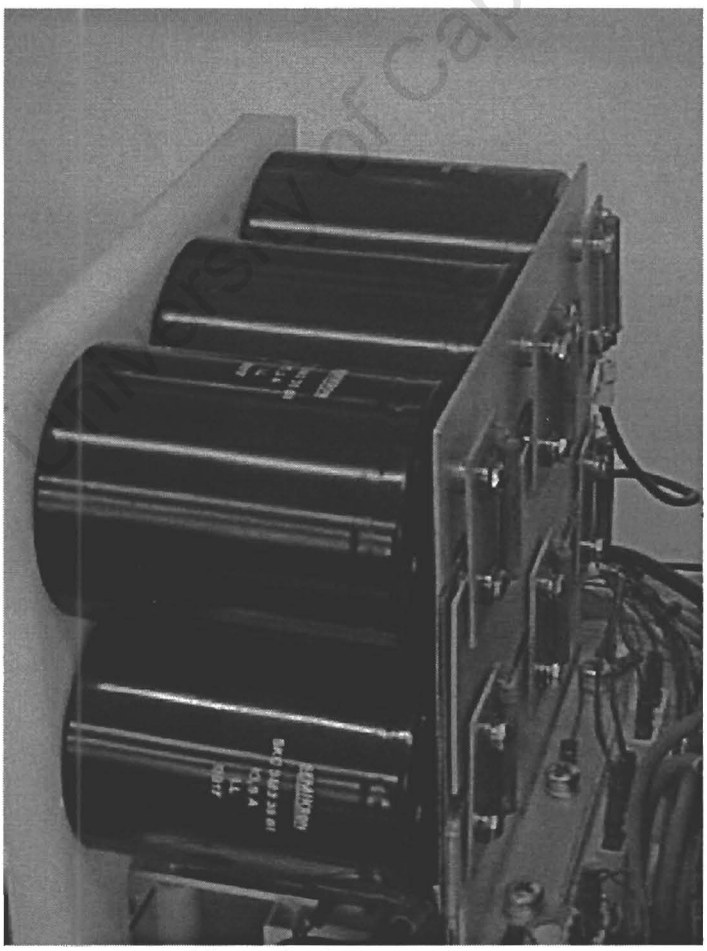
The Texas Instruments TMS320F240 DSP evaluation board



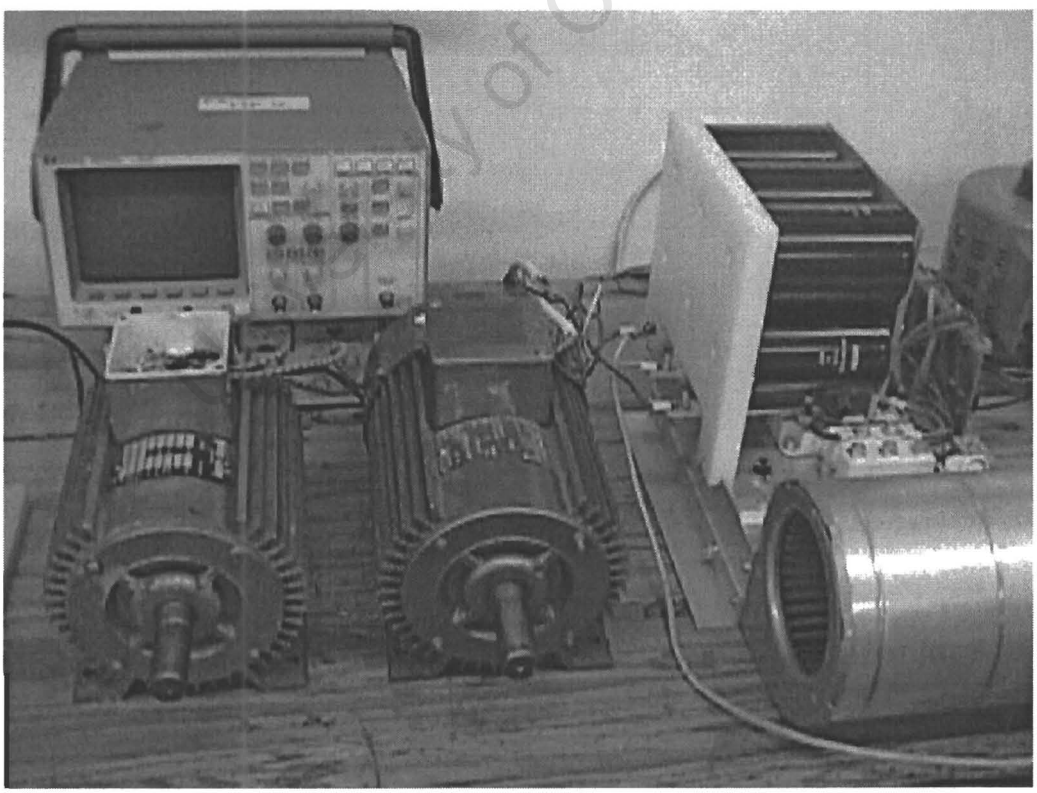
DSP board with control interface



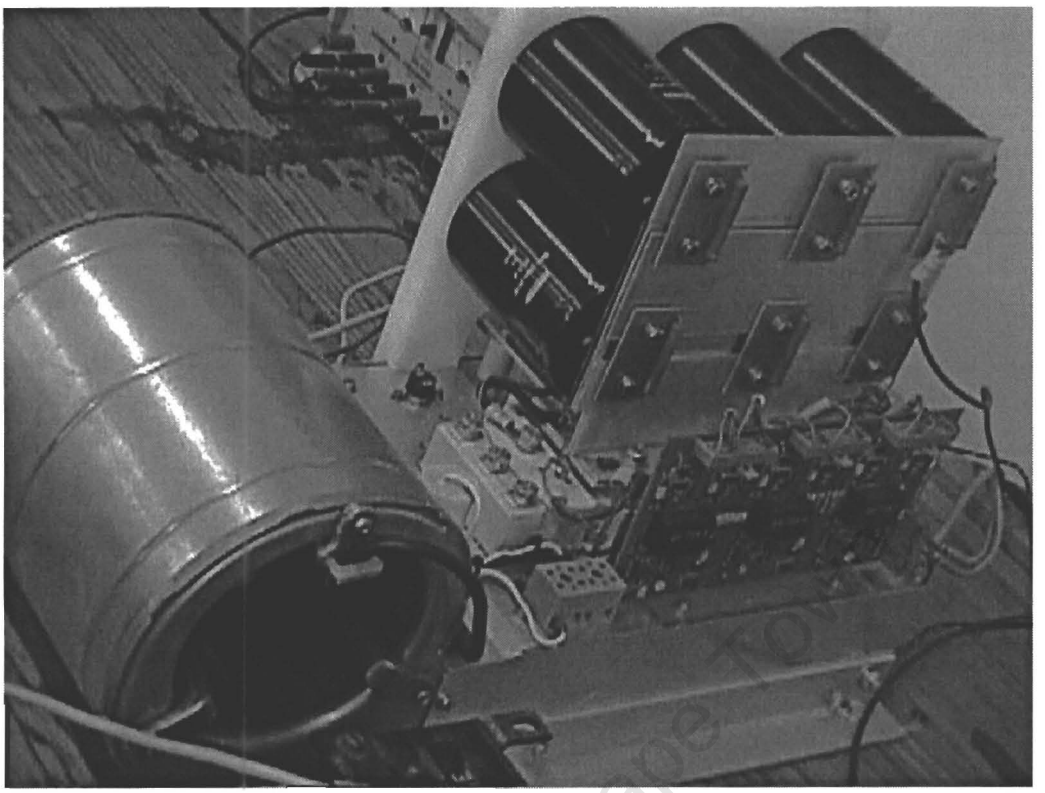
The IGBT driver board


The Split Capacitor Bank

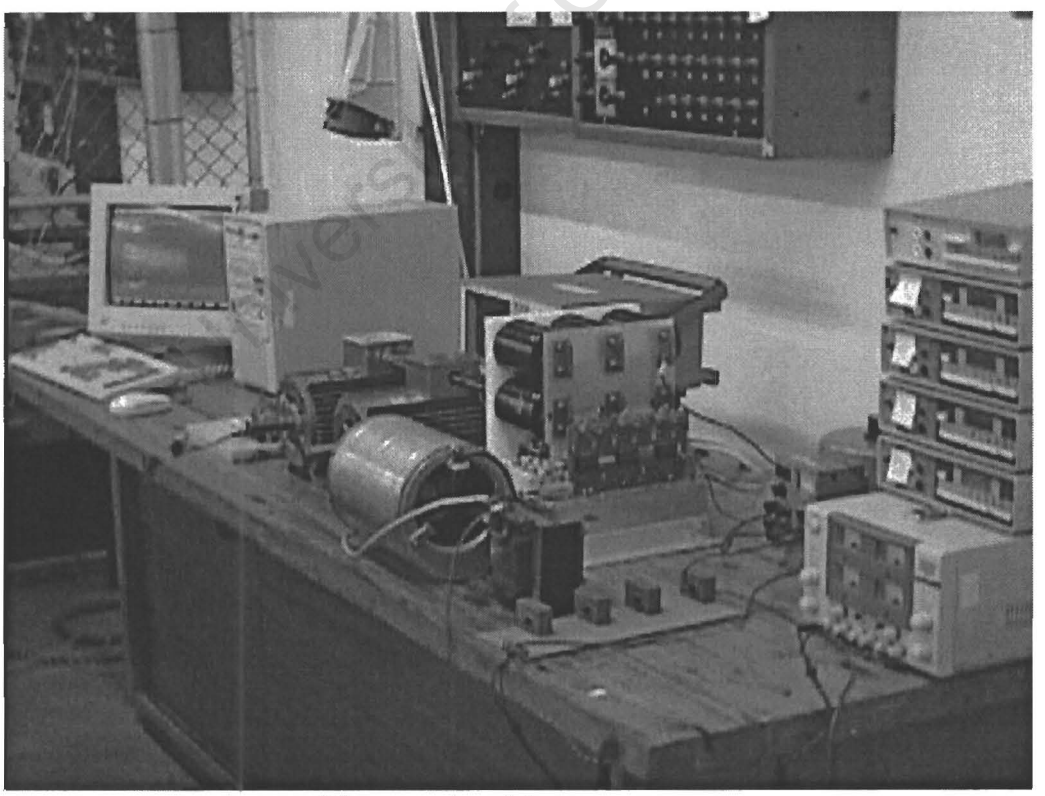
Inductance used in the experiments



3 phase motors used in the epxeriment



The three phase bridge showing the DC link and driver board



The complete laboratory setup