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ELECTRICAL CHARACTERISATION OF SIMPLE a-Si:H AND nc-Si DEVICES ON PAPER SUBSTRATES DEPOSITED BY HOT WIRE CHEMICAL VAPOUR DEPOSITION AND PRINTING TECHNIQUES

University of Cape Town

Thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Physics

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November 2004

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and has not previously in its entirely or part been submitted at any university for degree.

signature removed

Signature .... Date 22-11-2004

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ABSTRACT

In this work we report on the electrical transport properties of two classes of silicon: hydrogenated amorphous silicon (a-Si:H) obtained by hot wire chemical vapour deposition (HWCVD), and printed nanocrystalline silicon (nc-Si), both deposited on a flexible, lightweight substrate of 80 g m^{-2} wood-free paper. For different devices such as field effect transistors and n-i-p solar cells, electrical measurements will be discussed. A special emphasis is placed on field effect mobility and amplification factor measurements because these provide information about the quality of the material.

For the first a-Si:H devices a locally developed chamber, with a maximum sample size of 25 mm was used for production. For later devices, a commercial system from MVSystem Inc, which is equipped with a load-lock and is capable of accepting substrates up to 10 x 10 cm square, was used. The first series of transistors show standard characteristics, requiring a low drain current (I_d= 0.005 μA) to reach the threshold (turn on) voltage, V_t = 25V. The device shows a high amplification factor of 4.81, with carrier mobility, μ_{FE} = 0.0486 ± 0.0025 m^2/Vs. The second series of the a-Si:H transistors shows good characteristic results for a top-gate FET, with V_t ~ 4V, an amplification factor of A = 0.726, and a high carrier field effect mobility, μ_{FE} = 1.063 ±0.0125 m^2 V^{-1} s^{-1}.

The nc-Si FETs show an amplification factor of 0.533, with the highest mobility, μ_{FE} = 38.16 ± 0.25 m^2/Vs compared to other devices.

For the solar cells, the I-V characteristic curves show an effect on the current as the illumination changes, with a diode effect voltage ranging between -10V and 30V.

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CHAPTER 1

1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) and nano-crystalline silicon (nc-Si) materials are widely used in solar cells, transistors and other large area electronics applications such as active matrix flat panel displays or light sensors in image scanners. This is due to the possibility of depositing this material over large areas at low cost and because of its good optical and electronic properties upon light exposure or bias application, in spite of its low carrier field effect mobility ($\mu_{FE} \approx 1$ cm^2/Vs) [1,2].

Device quality a-Si:H and nc-Si are normally deposited by rf-plasma enhanced chemical vapor deposition (PECVD) [3]. The deposition rate for a-Si:H from undiluted SiH_4 is low, and normally hydrogen dilutions (>95%) are required [3]. A much faster technique for growing device quality a-Si:H films is hot wire chemical vapor deposition (HWCVD) which can give deposition rates 5 to 25 times higher than those obtained by PECVD. This is a relatively new deposition technique developed during the last two decades. Several aspects of this deposition process are uncertain and are still in the developmental phase. The large quantity of atomic hydrogen supplied to the surface of the growing film is responsible for the good electronic quality of films deposited at substrate temperatures in the range 150-350 ^{0}C [2,3], as it passivates dangling bonds and reconstructs stressed Si-Si bonds in the subsurface region.

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For flexible devices the most common substrate is steel foil, with the advantage of deposition and processing temperatures as high as 1000 ^{o}C [4,5]. Other flexible substrates discussed so far are plastic foils, where the device production temperatures must be lower than the working temperature of the specific polymer. For example a-Si:H has been successfully deposited on polyethylene tetraphthalate (PET) by PE-CVD at 110 ^{o}C [6] and by HW-CVD at 100 ^{o}C [7]. Besides the restriction in deposition temperature, to use flexible substrate materials such as thin plastics, the control of mechanical stress due to the differences in thermal expansion coefficients of the components and the deposition process itself [8] must be taken into account [9]. Other factors which must be considered are chemical stability, adhesion of the layer, and surface roughness [5]. In contrast to flexible plastic substrates, we present the results of depositing a-Si:H and nc-Si on a flexible, lightweight, economical low cost substrate ordinary paper using HW-CVD at low temperatures and transfer printing techniques.

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What all these materials, deposited at low substrate temperatures, have in common is poorer optoelectronic properties and higher defect densities than their counterparts deposited (or annealed) at high temperature. However, the question remains if these layers deposited at low substrate temperatures have a good enough quality to make a device. The first low temperature thin film transistors (TFTs) reported, were deposited on glass at 150 ^{0}C by Feng *et al* [9], and at 125 ^{0}C by McCormick *et al* [10].

Among various kinds of solar cells, those based on a-Si:H show the most promise for use in large scale electrical power generation because of their low production cost, the abundance of silicon on earth, and their reasonable efficiency. a-Si:H solar cells have

an advantage over crystalline or polycrystalline silicon solar cells because film thickness of only 0.3-0.4 μm is sufficient to absorb incident light. The most serious obstacle to the large-scale employment of a-Si:H solar cell is light induced degradation of a-Si:H film due to the photogeneration of defect states in the band gap of a-Si:H films [11]. Material in the mixed phase or nano-crystalline regime has higher stability against light-induced degradation than traditional hydrogenated amorphous silicon [12,13].

1.1 AMORPHOUS SILICON - PRODUCTION AND PROPERTIES

Over the past years, much effort has been devoted to the understanding of the properties of the amorphous material. Amorphous silicon and hydrogenated amorphous silicon are particularly important due to their potential applications in micro-electronics and opto-electronics such as solar cells, thin film transistors, optical sensors etc [14]. While the ability to fabricate large area devices, either by PECVD, or HW-CVD is an uncompromising advantage, they all suffer from low charge carrier drift mobilities compared with their crystalline counterparts [15].

On the other hand amorphous semiconductors have many advantages over their crystalline counterparts where applications are concerned. The low density of localized states in the mid gap allows either n or p-type doping, to function, and this leads to an increase in conductivity [16] compensating the low mobility. The high conductivity, a direct band electron transfer, and the ability to be deposited over large areas afford them many applications in microelectronics and opto-electronics. In this

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section some of the more important technological applications of hydrogenated a-Si are surveyed. One of the main advantages of amorphous silicon over crystalline silicon is that it is much more uniform in thickness over large areas. Since the a-Si is naturally full of defects, any other defects, such as impurities, do not affect the overall characteristics of the material too drastically [17]. Amorphous silicon produced by plasma enhanced CVD is used as the active layer in thin film transistors which are most widely used in large area electronics applications, mainly for liquid crystal displays (LCDs). Large area solar cells now use amorphous silicon, however, the small solar cells used in pocket calculators have been made with a-Si for many years [17].

Amorphous silicon can also be deposited at temperatures as low as 75 ^{0}C [17], which allow not only deposition on glass, but on plastics as well. Amorphous silicon is receiving much more attention at the present time because of the potential for roll-to-roll processing, whereby circuits are deposited onto long sheets of plastic or metal foils. This processing technique is expected to be much cheaper than modern crystalline semiconductor manufacturing.

The hot wire chemical vapor deposition (HWCVD) technique has shown its ability to grow hydrogenated amorphous silicon (a-Si:H) and hydrogenated nanocrystalline silicon (nc-Si:H) thin film transistor (TFTs) at low substrate temperatures [18,19]. In 1989 Matsumura [20] showed that the hydrogen concentration of device-quality hot wire CVD a-Si films is much less than that of plasma enhancement CVD film, and is as low as 3 at.% [21].

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The photovoltaic efficiency for a-Si:H is low (<10%) compared to crystalline silicon, but this deficiency is outweighed by the fact that a considerable amount of large area films can be produced cheaply [22]. The importance of solar cells cannot be understated. Beside their low scale power generation abilities, their potential for large scale power generation capable of meeting terrestrial energy requirement is immense [22]. However, if they are to be competitive with other methods their cost must be reduced substantially and the operating conversion efficiency increased.

The most important problem of a-Si:H for device applications is the well known degradation phenomenon, which leads to a strong reduction of performance compared to their initial state [23]. Light induced degradation of a-Si:H films is the most important obstacle to the large-scale employment of a-Si:H solar cells due to the photogeneration of defect states in the band gap of a-Si:H films [24-28]. Defect states act as recombination centres of electrons and holes, leading to a decrease in carrier lifetime [24]. Moreover, charge carriers are trapped at defect states, inducing steep band-bending regions near the interfaces and a flat-band region in the middle of a-Si:H films where the separation of electron-hole pairs becomes difficult [26,27]. Consequently, the conversion efficiency of a-Si:H solar cells decreases by 20-40% with prolonged irradiation [26,28]. In 1977 Staebler and Wronski (S-W) discovered the phenomenon that the photo-conductivity slightly reduces but the dark-conductivity of a-Si:H films increases substantially on prolonged irradiation due to the photogeneration of defect states [24].

Up to now, the main technological progress that has improved both material and cell stability is the use of hydrogen (H_2) dilution [29,30]. However, this technique also

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results in an increase in the material's optical band gap (E_g) and thus, in a decrease of its absorption capability [31]. Improving the stability of a-Si:H under light illumination is still a major subject of research for a-Si:H based devices. Other techniques developed later on, such as very high frequency deposition (VHFCVD, up to 100MHz) and an annealing process where the growth process is interrupted at regular intervals, have improved on the S-W effect.

An amorphous silicon solar cell has a thermal recovery of the Staebler-Wronski Effect, in that the light induced degradation under sunlight recovers to the initial state on thermal annealing for several hours at 150 ^{o}C. Heating under operation in sunlight is preferred to enhance the thermal recovery effect and to increase the generating power for the a-Si solar cell [32].

One of the drawbacks of the a-Si:H technology is the fact that the hole drift mobility in a-Si:H is two to three orders of magnitude smaller than the electron mobility which means that it is even more difficult to fabricate useful p-channel FETs and implement complementary circuits. Nonetheless, low speed electronics is just as important as high speed electronics in the electronic market. A low speed flat panel display made from hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) costs very roughly the same as a high speed crystalline Si microchip that runs the CPU [33].

The electrical properties of a-S:H depends on a number of factors including the temperature of deposition, discharge conditions and concentration of dopant gases in the discharge, optical and thermal history in a reversible way, *i.e.* exposure to light decreases conductivity, and heating it above 150 ^{0}C returns it to its original value [9].

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The structure of hydrogenated amorphous silicon is characterized as an irregular arrangement of atoms in contrast with crystalline silicon, whose structure has a periodic array of atoms. Although the longer range order is broken, the short range order is retained and this feature is reflected in its properties [16].

1.2 NANO CRYSTALLINE SILICON - PRODUCTION AND PROPERTIES

Nanocrystalline silicon (nc-Si) has attracted much attention in the optoelectronic industry, integrated photo sensors and imaging device applications, because of its unique and useful physical properties [34,35]. These properties include the strong photoluminescence of nc-Si films [34]. Nevertheless, silicon is the dominant material in microelectronics and there is an increasing interest in silicon nanocrystals due to their potential application in nanoelectronics [34]. The use of self-organization and possible manufacturing cost reduction makes this interest even stronger.

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However, it is surprising that the knowledge concerning electrical transport properties of nc-Si is rather fragmentary. For devices based on the use of dispersed nanocrystals in polymers [35], there is considerable interest for low cost manufacturing using simple solution coating techniques. These are, however, optoelectronic structures based on isolated nanoparticles (quantum dots).

Materials can be made nanocrystalline using quite a variety of techniques. These include ball milling, chemical synthesis, laser ablation, and SiH_4 decomposition

techniques for nanocryastalline powder production, and chemical vapour deposition (CVD) and physical vapour deposition (PVD) techniques for film production.

For many types of application, the advantages of using PVD techniques are becoming increasingly clear. Using for example, dc or rf sputtering at relatively low temperatures and high inert gas pressures, one can produce nanocrystalline thin films of different types of materials with a reasonably well controlled particle size and stoichiometry [36]. The need for a post annealing or calcination step "commonly required in most wet chemical techniques" is obviated in this case. This is very useful, since such thermal treatment usually leads to a coarsening in the particle size, and a broadening of the size distribution, in addition to undesirable chemical reactions [37,38]. It would be extremely advantageous if one could modify such PVD techniques to directly obtain a surface-passivated nano-crystalline thin film on a substrate at low temperature, or even at room temperature. One option that has been utilized with some success is to co-sputter the material of interest and a capping material, in appropriate proportions [36].

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Chemical vapour deposition (CVD) is a widely used method for depositing thin films of a large variety of materials. Applications of CVD range from the fabrication of microelectronic devices to the deposition of protective coatings [39]. This technique will be discussed in detail in chapter 3 "deposition techniques".

Mechanical attrition by ball milling has been a popular method to make nanocrystalline materials because of its simplicity, relatively inexpensive equipment, and applicability to essentially all classes of materials. However the ball milling

technique does not produce nanostructures by cluster assembly but by structure fragmentation [40]. Applying various ball milling and annealing parameters such as the nature of the milling tools and apparatus, ball to powder mass ratio, milling atmosphere, rotation speed, number and size of the balls, and temperature, different final microstructures (amorphous, nano-/amorphous or nanocrystalline) can be obtained [41]. The formation of the amorphous phase and its subsequent crystallization, as well as solid state reactions, during milling and annealing have been studied, in order to obtain complete transformation of nanocrystallinity by ball milling and ball milling with annealing [41]. Two phase a-Si and nc-Si has been produced by ball milling of polycrystalline element silicon. The nanocrystalline component contains some defects such as dislocations, twins, and stacking faults, which are typical of defects existing in conventional coarse-grained polycrystalline materials [42].

Ball milling involves heavy deformation of the powder and induces high concentration of strain and defects [43,44]. High energy ball milling, which is a well known process for preparing amorphous alloys, metal carbides alloys and nanocrystalline materials, has been considered as a powerful technique for synthesizing nanocrystalline materials.

For coatings, new techniques, such as pulsed laser deposition or electrodeposition, or variants of chemical vapor deposition techniques, have been developed that can be used to coat a surface with nanocrystalline metals, semiconductors and other materials [45]. Pulsed laser ablation (PLA) is also a well known method to produce thin films by ablating material from a solid target of known composition [46,47]. PLA usually

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occurs in vacuum, or sometimes in a background of inert gas such as Ar or more reactive gases such as ammonia or nitrogen. Diamond nanocrystals have been produced by the pulsed laser ablation of graphite at room temperature [46]. The liquid phase plasma laser ablation (LP PLA) technique has been used to produce a variety of materials, including diamond-like carbon films from liquid aromatic hydrocarbons [48], nanocrystals of carbon nitride by ablating graphite in ammonia solution [49] and nanometer-sized particles [50]. Nanocrystalline diamond has also been produce by LP PLA using a graphite target along with water or acetone as the liquid medium [51].

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Nanocrystalline silicon powder can be also prepared by decomposition of SiH_4 gas using an excimer laser beam. Increased reactivity is also seen in bulk nanocrystalline materials because of increased surface area. This can be useful with respect to direct chemical reactions or in terms of catalytic activity [41]. Nanocrystalline material need not appear just as a bulk solid or a layer, but can be a powder, or a nanopowder, thus there is overlap of the use of the terms nanocrystal and nanoparticle for some materials. In general, the important properties of nanocrystalline particles stem from their nanoparticulate nature, for example, nanocrystalline semiconductor quantum dots, where size is the critical property. Nanomaterials can, however, be the source of material for the production of nanocrystalline solids and coatings [41]. An increasingly popular way of converting the new generation of nano-powders into nano-crystalline coatings is thermal spraying.

Nanocrystalline silicon has useful advantages over amorphous silicon: One being, that if grown properly, it can have higher carrier mobility, due to the presence of silicon crystallites. One of the most important advantages of nanocrystalline silicon, however

is that it has increased opto-electronic stability over a-Si:H, one of the reasons being because of its lower hydrogen concentration. As mentioned above its carriers cannot attain the mobility of poly-Si, but it has the advantage over poly-Si that it is easier to fabricate, as it can be deposited using conventional low temperature a-Si deposition techniques, such as Plasma Enhanced CVD or hot wire CVD [35].

For the use of nc-Si:H in TFT fabrication considerably more research is needed. The structural evolution of nc-Si, from amorphous silicon close to the substrate, to an increasingly granular structure as the film grows, has two consequences. One is a rise in the carrier field effect mobilities in the top layer of the film. The electron field effect mobility increases from that in a-Si:H to about 40 cm^2/Vs and the hole mobility to about 0.2 cm^2/Vs in fully connected nc-Si layer. It is expected that the values for maximum mobility are likely to go up with progress in device fabrication [52]. The rise in mobility with film thickness reflects the change in the dominating mechanism, from trapping and re-emission out of band gap states to emission over electrostatic barriers at grain boundaries. The structures of CVD grown nc-Si explain why top gate TFTs of nc-Si exhibit much higher field effect mobilities than bottom gate TFTs [53]. A second consequence of the a-Si:H to nc-Si evolution is the electrical activation in nc-Si of (unwanted) impurities that are inactive in a-Si:H. As is already known from solar cell research [54], the electrical conductivity of normally undoped nc-Si can be quite high. While the conductivity of intrinsic crystalline silicon is about 10^{-5} Scm^{-1}, that of unintentionally doped nc-Si may reach $10^{-2} Scm^{-1}$, and can be brought to a values as low as $10^{-7} Scm^{-1}$ [53]. Because the "off" current of TFTs is set by the conductance of the channel layer, care must be taken to keep the thickness-averaged electrical conductivity of the channel layer low, and still grow a top layer with high

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field effect mobilities. This combination ensure low "off" current and high "on" current, and can be obtained by careful adjustment of nc-Si growth conditions and layer thickness, which may be as low as 50 nm [54] or as high as 300 nm. All TFT technologies using low temperature substrates share the need for a high quality gate dielectric made at low temperature. The gate dielectric will remain at the focus of TFT research for some time to come regardless of the type of channel semiconductor.

In this work we report on the electrical transport properties of two classes of silicon: a-Si:H obtained by HWCVD, and printed nc-Si, both deposited on a flexible, lightweight substrate, i.e. ordinary paper. For different devices such as field effect transistor and n-i-p solar cells, electrical measurements will be discussed. A special emphasis lays on field effect mobility measurements because it allows obtaining information about the quality of the material. Application of nanocrystalline silicon as quantum dots is not used in this work.

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CHAPTER 2

BACKGROUND TO THE DEVICES AND MATERIALS

2.1 SOLAR CELL

A solar cell is a photovoltaic device designed to convert sunlight directly into electric power, in which a voltage is set up across a p-n junction when photons from the sun fall on the surface. The basis of a solar cell is high purity amorphous or crystalline silicon from which high efficiency devices can be made.

The application of solar cells is a clean and reliable method of generating electricity. It is attractive from an energy point of view as it represents a potentially inexhaustible source of energy, unlike depletable resources such as coal, gas and oil. For many applications, however, the high cost of solar cell production makes them uncompetitive in comparison to electricity from conventional sources such as coal fired power stations. Solar cells have therefore been limited primarily to remote applications, such as for telecommunications and marine navigation systems, where low maintenance and high reliability are required [55]. Much solar cell research has concentrated on reducing costs, thus making solar cells commercially viable. A large focus on reducing cost is in the development of thin film solar cell technologies, an alternative to "bulk silicon" technologies, where a thin layer of semiconductor is deposited onto a supporting material such as glass [55].

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Because of the difference in material, the efficiencies of amorphous silicon solar cells are significantly lower than those of bulk silicon: less than 8% for the best commercial devices. High efficiency is not critical for applications as small consumer products e.g. monocrystalline, but is critical for large scale applications such as supply of grid connected electricity. As mentioned before, amorphous cells tend to degrade when exposed to sunlight. Despite these problems, significant improvements have recently been made in improving and stabilizing the performance of a-Si:H solar cells. Hydrogenated amorphous silicon films, can readily be deposited onto large area substrates, and can even be deposited onto a continuous flexible substrate. Thus, although the photovoltaic efficiency of a-Si:H is considerably lower than that of its crystalline counterparts, this deficiency is ameliorated to a considerable extent by the fact that large area films of a-Si:H can be produced relatively cheaply [16].

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The breakthrough of doping a-Si:H made it suitable for various technological applications, in which it now can act as p-n junction, and could be used for manufacturing solar cells. This resulted in a rapid increase of research activities in this field. Shortly after this discovery the first a-Si:H solar cell was produced, which consisted of an intrinsic layer sandwiched between a p-type and n-type layer [56].

2.1.1 PRINCIPLE OF P-N JUNCTION SOLAR CELL

One of the crucial keys to solid state electronics is the nature of the P-N junction. When p-type and n-type materials are placed in contact with each other, the junction behaves very differently than either type of material alone. Specifically, current will flow readily in one direction (forward biased) but not in the other (reverse biased), creating the basic diode. This non-reversing behaviour arises from the nature of the charge transport process in the two types of materials.

In its simplest form, the solar cell consists of a junction formed between n-type and p-type semiconductors, either of the same material or different materials illustrated in figure 2.1.

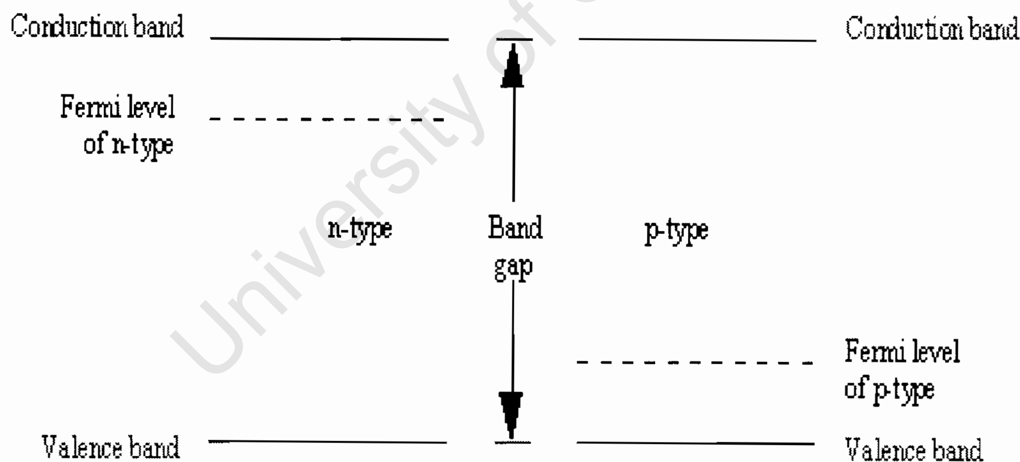

Figure 2.1: Principle of band structure of differently-doped semiconductors [57]

When the two halves of the junction are brought together, the Fermi levels on either side are forced to coincide, causing the valence and conduction bands to bend as shown in figure 2.2.

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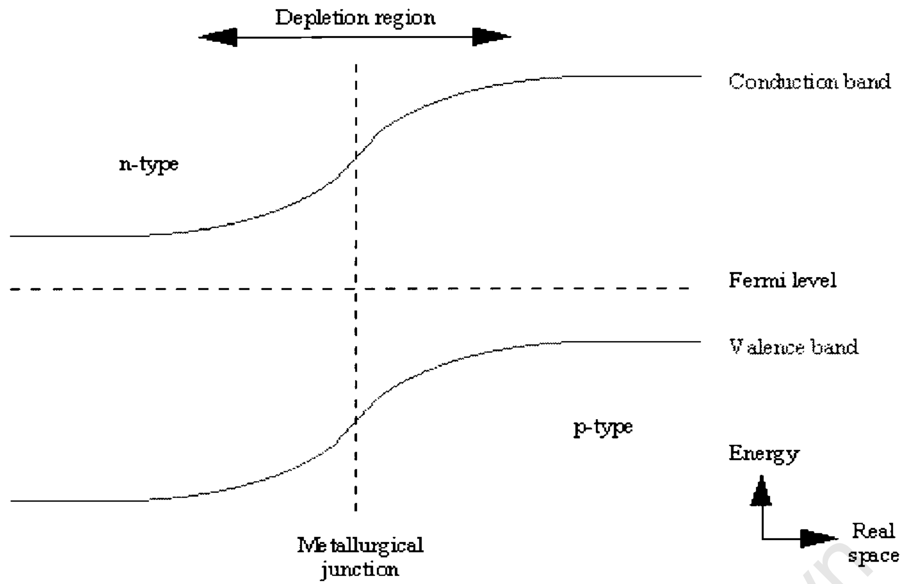

Figure 2.2: Heterojunction band-bending [57]

These bent bands represent a built-in electric field over what is referred to as the depletion region (fig 2.3). When a photon, with energy greater than the band gap of the semiconductor, passes through the solar cell, it may be absorbed by the material.

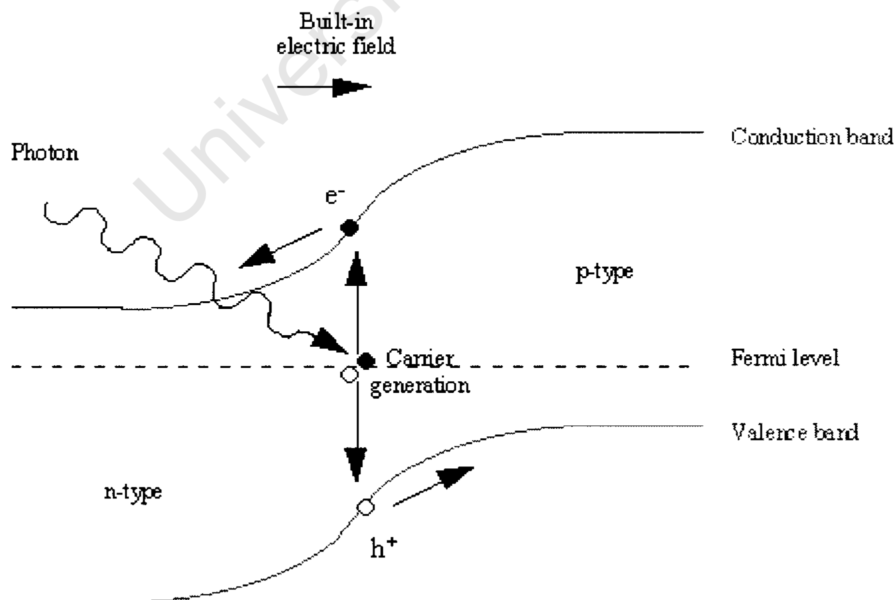

Figure 2.3: A Principle of photovoltaic device with a built in electric field [57]

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This absorption takes the form of a band-to-band electronic transition, so an electron/hole pair is produced (fig 2.3). If these carriers can diffuse to the depletion region before they recombine, they are then separated by the electric field, causing one quantum of charge to flow through an external load. This is the origin of the solar cell's photocurrent [57].

The p-n junction is the basis of a diode, which is a circuit component which is used to control current flow through a circuit. When a P-type material and an N-type material are placed in close contact, a PN junction is formed. Due to electron-hole annihilation across the PN junction, an electric field is formed. This field prevents current flow in one direction across the junction and encourages current flow in the opposite direction [58].

When the polarity of the battery is such that electrons are allowed to flow through the diode, the diode is said to be *forward-biased*. Conversely, when the battery is "backward" and the diode blocks current, the diode is said to be *reverse-biased*. A diode may be thought of as a kind of switch: "closed" when forward-biased and "open" when reverse-biased. When the diode is forward-biased and conducting current, there is a small voltage dropped across it, leaving most of the battery voltage dropped across the lamp. When the battery's polarity is reversed and the diode becomes reverse-biased, it drops *all* of the battery's voltage and leaves none for the lamp. If we consider the diode to be a sort of self-actuating switch (closed in the forward-bias mode and open in the reverse-bias mode), this behaviour makes sense.
This forward-bias voltage drop exhibited by the diode is due to the action of the depletion region formed by the P-N junction under the influence of an applied

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voltage. When there is no voltage applied across a semiconductor diode, a thin depletion region exists around the region of the P-N junction, preventing current through it. The depletion region is for the most part devoid of available charge carriers and so acts as an insulator. If a reverse-biasing voltage is applied across the P-N junction, this depletion region expands, further resisting any current through it as shown in fig 2.4 [58].

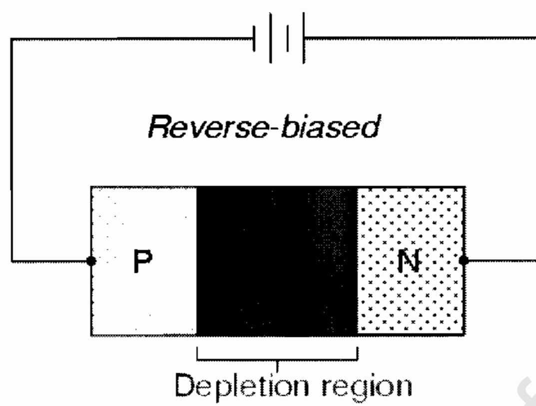

Fig 2.4 Reverse-biasing voltage applied across the P-N junction, expands the depletion region [58].

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Conversely, if a forward-biasing voltage is applied across the P-N junction, the depletion region will collapse and become thinner, so that the diode becomes less resistive to current through it. In order for a sustained current to go through the diode, though, the depletion region must be fully collapsed by the applied voltage. This takes a certain minimum voltage to accomplish, called the *forward voltage (fig 2.5)*

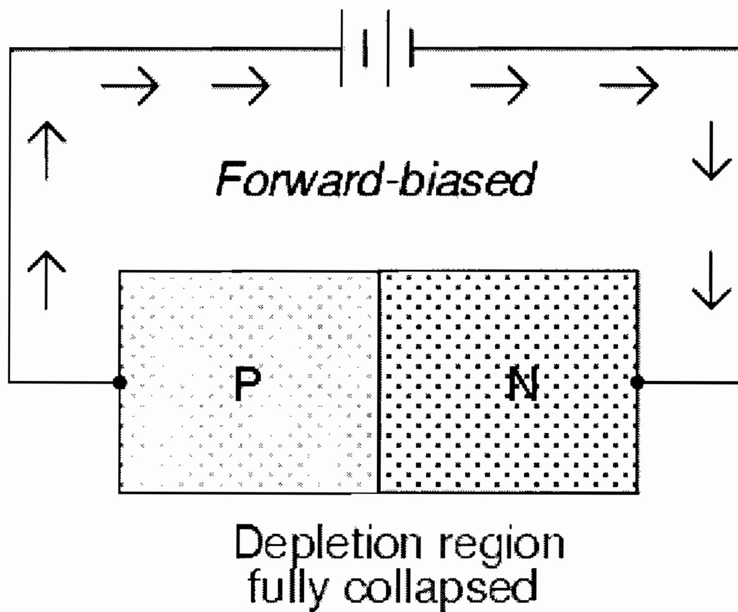

Fig 2.5 Forward-biasing voltage applied across the P-N junction, with fully collapse depletion region [58].

The forward voltage drop remains approximately equal for a wide range of diode currents, meaning that diode voltage drop not like that of a resistor or even a normal (closed) switch. For most purposes of circuit analysis, it may be assumed that the voltage drop across a conducting diode remains constant at the nominal figure and is not related to the amount of current going through it.

In actuality, things are more complex than this. There is an equation describing the exact current through a diode, given the voltage dropped across the junction, the temperature of the junction, and several physical constants. It is commonly known as the *diode equation* [58]:

$$I_d = I_s(e^{qV_d/NkT} - 1) \qquad (2.1)$$

Where,

I_d = diode current in amps

I_s = Saturation current in amps (typically 1 x 10^{-12} amps)

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V_d = voltage applied across diode in volts

N = "Nonideality" or "emission" coefficient (typically between 1 and 2)

k = Boltzman's constant (1.38 x 10^{-23} J/K)

T = Junction temperature in degrees Kelvin

The quantity kT/q describes the voltage produced within the P-N junction due to the action of temperature, and is called the *thermal voltage*, or V_t of the junction.

A reverse-biased diode prevents current from going through it, due to the expanded depletion region. In actuality, a very small amount of current can and does go through a reverse-biased diode, called the *leakage current*, but it can be ignored for most purposes. The ability of a diode to withstand reverse-bias voltages is limited, like it is for any insulating substance or device. If the applied reverse-bias voltage becomes too great, the diode will experience a condition known as *breakdown*, which is usually destructive. A diode's maximum reverse-bias voltage rating is known as the *Peak Inverse Voltage*, or *PIV*. Like the forward voltage, the PIV rating of a diode varies with temperature, except that PIV *increases* with increased temperature and *decreases* as the diode becomes cooler -- exactly opposite that of forward voltage [58].

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2.1.2 SILICON BASED SOLAR CELL

Semiconductors are materials which become electrically conductive above a certain (very low) temperature, and in which the conductivity increases with temperature. Over 95% of all the solar cells are produced world wide are composed of the semiconductor material silicon (Si). As the second most abundant element in earth's

crust, silicon has the advantage, of being available in sufficient quantities, and additionally processing the material does not burden the environment excessively. To produce a solar cell, the semiconductor is contaminated or "doped". Doping is the intentional introduction of certain chemical elements, with which one can obtain a surplus of either positive charge carriers (p-conducting semiconductor layer) or negative charge carriers (n-conducting semiconductor layer) from the semiconductor material. If two differently doped semiconductor layer are combined, then a so-called p-n junction results at the boundary of the layers [59].

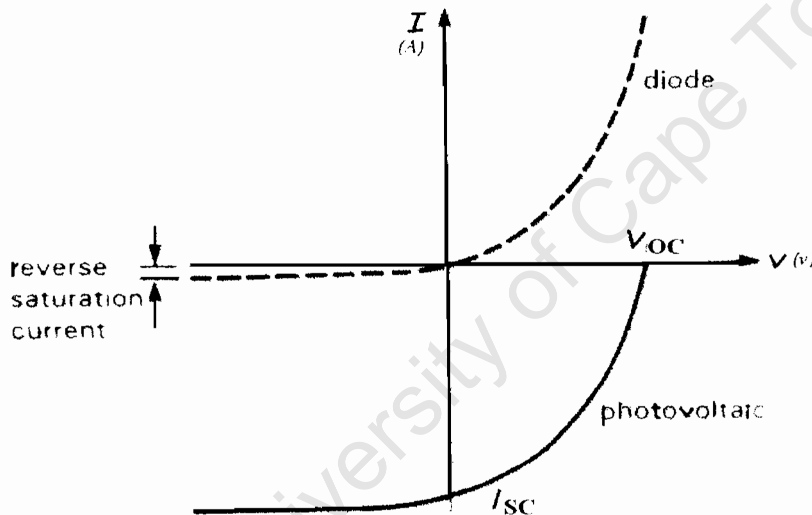

Figure 2.6 Solar cell out put voltage versus load current is simply a displaced diode V-I curve, where I_{SC} represent the short circuit current [59].

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As seen in figure 2.6 silicon solar cells have simple and very useful Ampere-Voltage (I-V) characteristics. The open circuit voltage, V_{oc} is almost independent of the light [59], and the current voltage characteristic curve is simply a displaced diode curve.

The terminal voltage stays nearly constant as the load current is increased up to a maximum current, at which point the solar module become roughly a constant source

for further decreases in load impedance. The maximum current scales linearly with light levels, giving a set of characteristic curves (fig 2.7). Solar cells work best when cold, since the open-circuit voltage drops with increasing temperature [60].

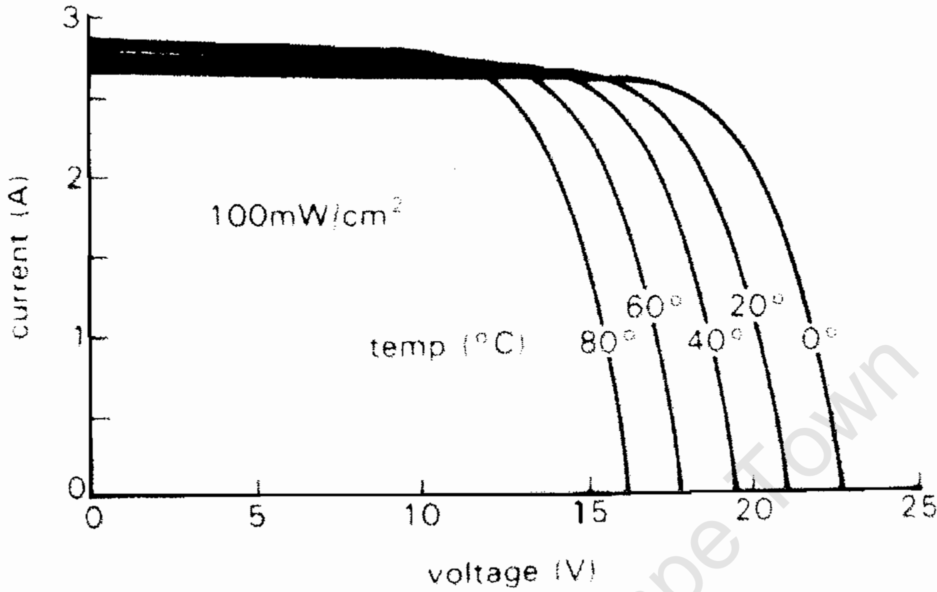

Figure 2.7 Solar-panel output versus temperature (Solavolt MSVM4011) [60]

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The ideal energy conversion efficiency η of the solar cell is defined by [61]

$$\eta = \frac{j_{sc} V_{oc} ff}{P_{in}} \qquad (2.2)$$

where j_{sc} is the short circuit current density, V_{oc} the open circuit voltage, P_{in} the incident power and ff is the fill factor.

V_{oc} is generally limited by the direct band-to-band recombination of photo-generated carriers. However a non-uniform density of states within the mobility band-gap, especially those at the band edges of the valence and conduction band, inherent to amorphous material, leads to recombination via these defects states and provides an upper limit to V_{oc}. The fill factor is given by [61]

$$ff = \frac{I_m V_m}{j_{sc} V_{oc}} \tag{2.3}$$

where $(I_{m,} \ V_m)$ is the maximum power point on the solar cell current- voltage characteristics. The conversion efficiency of a practical solar cell is limited by the intrinsic or extrinsic losses due to the inability of a cell with a band gap E_g to properly match the broad solar spectrum, or an incomplete extraction of photo-generated carriers and non-radiative recombination of carriers.

As Henry [62] showed, the theoretical maximum efficiency of an ideal photovoltaic cell reaches 31% for a semi-conducting material with a band gap of 1.35 eV, although material with gaps in the range 1-2 eV are predicted to have ideal photovoltaic efficiencies higher than 25 %. These calculations are based on AM1.5 (AM = Air Mass) illumination conditions, provided by a solar simulator consisting of a high power air cooled lamp that provides uniform illumination over a large area (150 mm x 150 mm): The AM1.5 standard is typically used at the latitudes of northern Europe and the irradiance is 1000W m^{-2} and the colour temperature is 5600 Kelvin [62].

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2.2 FIELD EFFECT TRANSISTOR

The Field Effect Transistor (FET) is defined as, a three-terminal active device, which has many applications in both analog and digital electronics [63]. In figure 2.8 the structure of a field effect transistor with its three terminals, Drain (D), Source (S) and the Gate (G) is shown.

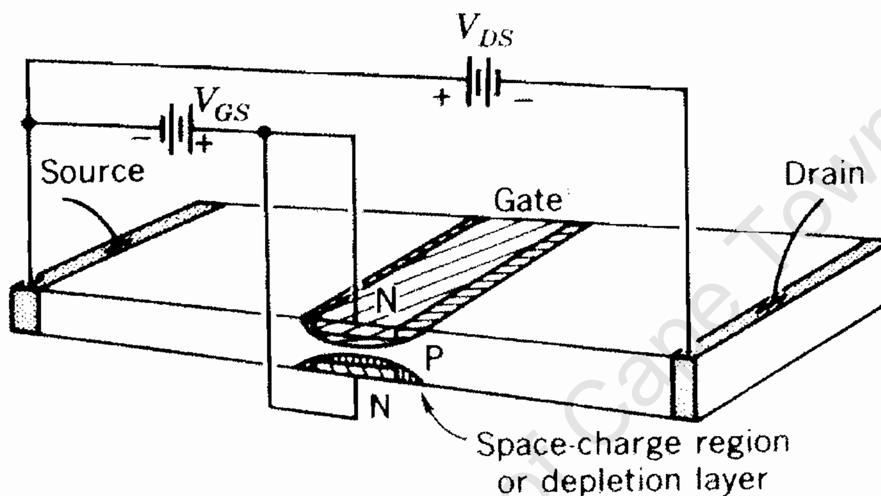

Figure 2.8: Structure of Field Effect Transistor with three terminal layers; Gate, Drain and Source [63]

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Where:

Source (S)- is the terminal through which the majority carriers enter the bar. conventional current entering the bar at S is designated by I_s.

Drain (D)- is the terminal through which the majority carriers leave the bar. conventional current entering the bar at D is designated by I_d, the drain to source voltage is called V_{ds}, and is positive if D is more positive than S.

Gate (G) – is the terminal which control the conductivity of the transistor between the source and drain without the flow of the gate current for both the n-channel and p-channel devices.

Field effect transistor are different from conventional transistors (sometimes called "bipolar transistors," "bipolar junction transistors," or BJT, to distinguish them from FETs). Broadly speaking, however, they are similar devices, which we might call charge –control devices: In both cases we have a three terminal device in which the conduction between two electrodes depends on the availability of charge carriers, which is controlled by a voltage applied to a third control electrode.

In an npn BJT the collector-base junction is back-biased, so no current normally flows. Forward-biasing the bias-emitter junction by approximately 0.6 volts overcomes its diode "contact potential barrier," causing electrons to enter the base region, where they are strongly attracted to the collector: although some base current results, most of these "minority carriers" are captured by the collector [64]. This results in a collector current, controlled by a (smaller) base current. The collector current is proportional to the rate of injection of minority carriers into the base region, which is an exponential function of the base-emitter (BE) potential difference. One can think of a bipolar transistor as a current amplifier or as a transconductance device [64].

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In a FET, as the name suggests, conduction in a channel is controlled by an electric field, produced by a voltage applied to the gate electrode. There are no forward-biased junctions, so the gate draws no current; this is perhaps the most important advantage of the FET. As with BJT, there are two polarities, n-channel FETs (conduction by electrons) and p-channel FETs (conduction by holes). These two polarities are analogous to the familiar npn and pnp bipolar transistors, respectively.

Conventional transistors exhibit inherently low (but not zero) input impedances except when operating at very small currents [65]. In the early years of transistor circuit design this characteristic, plus the current orientated amplification requirements, appeared as major restrictions to the engineers who had originally worked with vacuum tubes. Time has proved that many of these objections existed only in the designers' mind, and they vanished as they learned to work with the device.

Nonetheless, there are applications where high input impedance is essential, such as switches. In these cases, conventional transistor circuitry is often awkward or impossible to design [65]. The development of the field effect transistors (FETs) was mainly prompted by this need. However, the FET offers additional advantages which have encouraged wide acceptance:

(i) FET's do not depend upon minority carriers, thus their radiation resistance is good.

(ii) FET's are free from certain sources of noise that occurs in common transistor action, for example, Schottky noise.

(iii) The power gain of a FET far exceeds that of a common transistor at audio frequencies and tends to increase with the current capability, so that power FET's shows considerable promise.

In the field effect transistor, current flows along a semiconductor path called the channel. The source and drain electrodes are at each end of the channel. The physical dimensions of the channel are fixed, but its effective electrical width can be varied by the application of a voltage to the gate electrode. The conductivity of the FET depends, at any given instant in time, on the electrical width of the channel. A small

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change in gate voltage can cause a large variation in the current from the source to the drain, allowing the field effect transistor to act as an amplifier.

Field effect transistors exist in two main classes: the junction field effect transistor (JFET) and the metal oxide semiconductor FET (MOSFET). In a junction field effect transistor the gate forms a semiconductor junction with the underlying channel. This has the important consequence that a JFET gate should not be forward biased with respect to the channel, to prevent gate current. For example, diode conduction will occur as the gate of an n-channel JFET approaches +0.6 volt with respect to the more negative end of the channel (which is usually the source). The gate is therefore operated reverse-biased with respect to the channel, and no current flows in the gate circuit. However, under some conditions there is a small current through the junction during part of the input signal cycle (diode leakage).

In the MOSFET, the gate is insulated from the channel by a gate dielectric (usually an oxide), which permits the gate to source voltage to be either positive or negative without the flow of gate current for both the n-channel and the p-channel devices. There are several kinds of MOSFET, each of which operates either in the depletion mode or enhancement mode, or, in a certain instances, in a combination of both [64]. In each, the current that flows on the drain to source channel is a function of the voltage applied from gate to source. In the depletion mode device, the channel is conducting when the gate to source voltage is zero. FETs (both JFET and MOSFET) are nearly symmetrical, but the gate-drain capacitance is usually designed to be less than the gate-source capacitance, making the drain the preferred output terminal.

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An important parameter in the MOS transistor is the threshold voltage V_t, which is the minimum gate voltage required to induce the channel. In general, the positive gate voltage of an n-channel device must be larger than some value V_t before a conducting channel is induced. Similarly, a p-channel device requires a gate voltage more negative than some threshold value to induce the required positive charge (mobile holes) in the channel. The value of V_t is controlled during device fabrication and typically lies in the range 0.5 to 3V [66]. In the enhancement mode device, the opposite situation occurs and the channel is non-conducting when the gate to source voltage is zero. For an enhancement mode device, the drain current is zero until the gate to source voltage exceeds a value that is known as the threshold voltage (V_t).

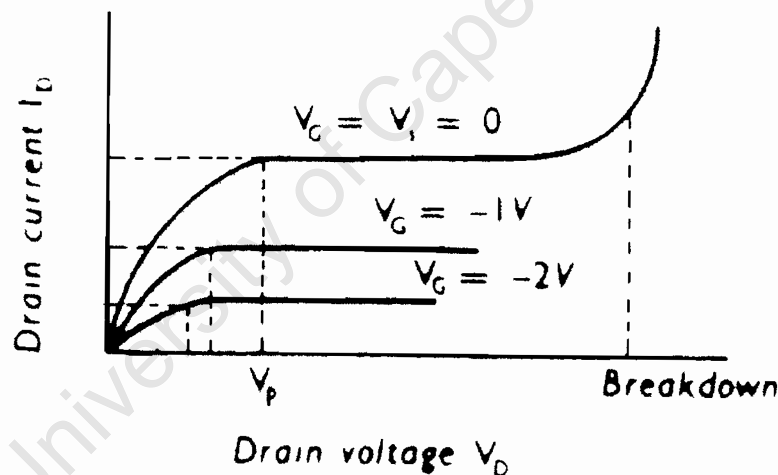

Figure 2.9 Characteristic curves of Field Effect Transistor at different constant gate voltages [66].

Applying a negative voltage to the gate will also increase the size of the depletion layers, and hence the pinch-off voltage (when the depletion layers first meet, the drain voltage is called pinch-off voltage, V_p) condition will be reached at a lower drain voltage, at a voltage above pinch off, the depletion layers extend further into the drain region, but remains essential constant in the channel until such a value breakdown occurs as shown in fig 2.9.

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Breakdown voltages are measured at a specific current level which is set high enough to be in the constant voltage region of the breakdown characteristic. Measurements in this region, however, may result in damage to the device from excessive power dissipation. For this reason breakdown characteristics are usually guaranteed as a leakage current which is measured in the nearly constant current region of the characteristic curve.

When a guaranteed breakdown voltage at high current level is required (known), then the measurement of that device must not exceed that voltage, which means the breakdown voltage will be used as a maximum voltage applied to that device.

Field effect transistors (FETs) are commonly used for weak-signal amplification, for example in wireless communications and broadcast general, used for high-power amplification, such as is required in large wireless communication and broadcast transmitters. Field effect transistors are often fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousand of FETs, along with other components such as resistors, capacitor and diodes.

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2.3 THIN FILM TRANSISTOR

A thin film transistor (TFT) is generally a field effect transistor whose active, current-carrying layer is a thin film, usually a film of silicon, in contrast to insulated gate field effect transistors, which are made on silicon wafers and use the bulk silicon as the active layer. Thin Film Transistors are used in active matrix displays, which are display screens composed of a grid (or matrix) of picture elements ("pixel").

Thousand or millions of these pixels together create an image on the display. Having a transistor at each pixel means that the current that triggers pixel illumination can be smaller and therefore can be switched on ("light") and off ("dark") more quickly.

Low temperature substrate materials demand a broad revision of TFT materials, device geometry, and processes. Amorphous silicon thin film transistors may be deposited on low quality materials by careful adaptation of the established 250-350 ^{0}C processes to the temperatures of 150 ^{o}C or lower tolerated by plastic [49].

2.3.1 SILICON FOR THIN FILM TRANSISTORS

The two important research directions for TFTs are high mobility and flexible substrates. All TFT applications benefit from a high "on" current, which is proportional to carrier mobility. Simple switches and "on" pixel circuits (e.g. preamplifiers) can be implemented with n channel TFTs. Monolithic integration with peripheral circuits and reduction of power consumption need also p channel TFT current sources. The need for high mobility makes the grain size of silicon films take on overriding importance, regardless of the substrate material on which the silicon is deposited [5]. In consequence the correlation between mobility/grain size and process temperature dominates the research on channel materials for silicon TFTs.

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Table 2.1. Properties of Silicon materials for CVD grown thin film transistors [5]

Attribute	a-Si:H	nc-Si:H	μc-Si
Standard deposition T (^{0}C)	250	250	150
Highest T process/material (^{0}C)	350	280	Laser
	SiNx	n^+, p^+	μc-Si
Lower reported process T ^{0}C	110	150	Laser
Grain size (μm)	Amorphous	<0.1	
Efficiency	8-13	3~10	
Electron mobility (cm^2/Vs)	0.5-1	40	300-
Hole μ (cm^2/Vs)	~0.01	0.2	50
Conductivity (S/cm)	10^{-11}	10^{-7}-10^{-2}	10^{-6}
Growth rate (nm/s)	0.1-1	0.1	0.1-1
Gate and Source/Drain geometry	Bottom	Top	Top

Table 2.1 above, represents the modifications of amorphous silicon, nanocrystalline silicon and microcrystalline silicon material available for TFTs, as well as their approximate hole and electron carrier mobilities and device type with their standard deposition temperature. An indication of grain size is also given in this table.

Hydrogenated amorphous silicon thin film transistors (TFT), commonly deposited by plasma enhanced chemical vapor deposition (PECVD) at 13.56 MHz, are widely used as pixel switching devices in large area electronics [49]. The low field effect mobility in amorphous silicon material (<1 cm^2/Vs), as shown in table 2.1, and the limited stability under gate stress, due to defect creation in the a-Si:H, complicates the utilization in applications where high performance is demanded, such as organic light-emitting diode (OLED) displays and column/row-addressing circuitry. While the low mobility is attributed to the inherent disorder of a-S:H, the microscopic details of the defect-creation mechanism (Staebler-Wronski effect) are still elusive [67].

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TFTs incorporating PECVD a-Si:H with high compressive stress exhibit a poor stability. Since 'device-quality' a-Si:H usually has high compressive stress, combining a high field mobility with a high TFT stability seems to be contradictory. Therefore, alternative deposition techniques, such as HWCVD have been used for TFT deposition. It could be shown that TFT with a high stability, maintaining a high mobility, are feasible [67].

Most commercially available AMLCDs use glass as the starting material in the display fabrication process. Glass has excellent optical clarity and is compatible with chemicals used in standard semiconductor processing. However, glass has the undesirable characteristics of being fragile and heavy. As a result, displays must be handled carefully to avoid breakage. However, lately plastic has been employed as the starting material for display fabrication, and good displays have been achieved on materials that are, not only lightweight and rugged, but also flexible [67].

There is significant room for improvement in ultra-low temperature production. High mobilities, low leakage currents and threshold voltages are desirable for high-performance active-matrix LCD applications, particularly for the integration of driver circuitry, but low processing temperatures (<150ºC) must be maintained for compatibility with low-cost substrate materials [67]. All thin film transistor applications benefit from a high 'on' current, which is related to carrier mobility. Simple switches and on-pixel circuits can be implemented with n channel TFTs.

Table 2.2, presents a chart of compatibility of silicon with the main groups of substrate materials. Because steel can be processed at temperatures up to 1000 °C, all conceivable silicon TFT fabrication can be carried out on it, from a-Si:H to μc-Si, like

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on quartz glass. Plastic can be transparent, but may be processed only up to 100 °C or 200 °C. Plastics substrates present many challenges, which have been recognized only in part [49].

Table 2.2: Compatibility of direct deposited Si channels with substrate materials [5].

Substrates material and T limit	Plastic	Glass	Steel
TFT use	≤ 150 °C	≤ 600 °C	≤ 1000 °C
Preferred for cell switch (n-channel)	a-Si:H	a-Si:H	a-Si:H
Preferred for peripheral circuits (n and p channel)	nc-S:H	μc-Si or nc-Si:H	μc-Si or nc-Si:H

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The direct deposition of device-grade silicon onto plastic brings up many substrate issues. Desirable properties are thermal and chemical stability, low coefficients of thermal and humidity expansion, low shrinkage during circuit fabrication, low solubility of water, good film adhesion, low chemical and mechanical inhomogeneity, and low surface roughness [68,69].

2.4 THE INFLUENCE OF THE SILVER LAYER

As described in the next chapter silver was printed on the devices' substrates as the contact layer, therefore here is a brief overview. Silver is a metal widely used in low-emissivity coatings or electromagnetic interference (EMI) shielding. A continuous layer of silver has low absorption and very good electrical conductivity. Thin layers of silver become transparent in the visible spectrum range. Below a critical layer thickness the material properties differ considerably from those of the bulk material,

both the electrical resistivity and the absorption of light increase rapidly with further decreasing of the layer thickness. This behavior is attributed to a transition from a continuous film to the formation of distinct islands of silver atoms. The critical thickness for this transition depends on the substrate and the deposition conditions and is mostly between 10 and 20 nm averaged thickness. As a result, a maximum of the total film absorption is found between 5 and 10 nm averaged thickness [70].

2.5 PROPERTIES OF PAPER

Wood is made up of cellulose fibres held together by a resinous substance called lignin. It is from these fibres that paper is made. Paper is made by turning wood into pulp, in a pulping process in which wood is broken down into individual fibres. Hardwoods, like Eucalyptus, have short fibres which help to fill in the sheet of paper, making it smooth and dense. If you tear a piece of paper you will see a number of whiskers sticking out from the line of the tear, these are the wood fibres.

Chemical pulp is needed for blending with ground wood and thermo-mechanical pulps to strengthen the paper. It is a very pure pulp, the fibres having been separated by dissolving the lignin, which binds them via a process of cooking the wood in a chemical 'soup'. Hence the fibres are not mechanically damaged. Paper made from chemical pulp is usually referred to as wood free [71].

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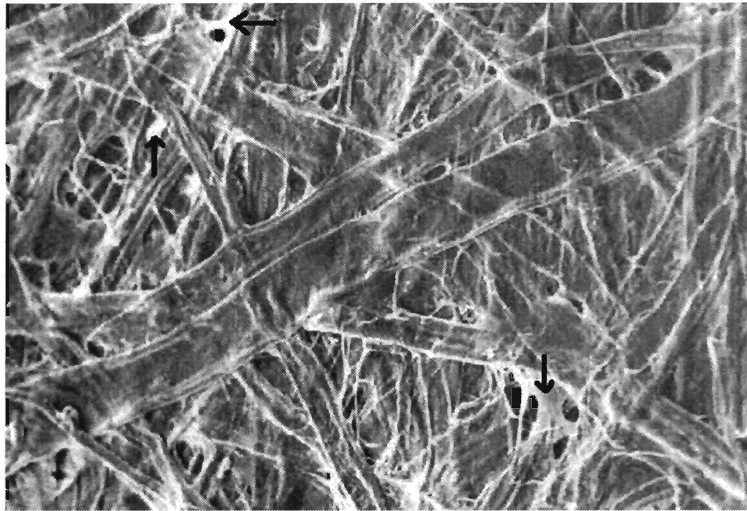

Figure 2.10. Cross-sectional scanning electron microscope (SEM) of pure white mondi paper, showing some wood fibres and calcium carbonate (arrows) on the paper.

In addition paper contains other particulate materials. For example Mondi paper's ingredient, Precipitated Calcium Carbonate filler (PCC) has resulted in a superior paper product [71], which is claimed by the manufacturer to deliver:

1. Brilliant whiteness for good colour contrast and aesthetic appeal
2. smooth sheet surface for less abrasion and better copying
3. Increased opacity to eliminate show-through
4. Stiff sheet for constant runnability (feed through printing press)

Points 2 and 4 described above are desirable properties for a future mass (roll to roll) production of electronic devices.

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CHAPTER 3

DEVICE PREPARATION

3.1 DEPOSITION TECHNIQUES

In the following chapters electric characterisation of FETs, and solar cells will be discussed. Here the different production techniques, chemical vapour deposition and transfer printing will be described, starting with an overview of these deposition techniques.

3.1.1 CHEMICAL VAPOR DEPOSITION

(a). GENERAL OVERVIEW

In a typical CVD process, reactant gases (often diluted in a carrier gas) at room temperature enter the reaction chamber. The gas mixture is heated as it approaches the deposition surface, which is either heated radiatively or placed upon heated substrates. Depending on the process and operating conditions, the reactant gases may undergo homogeneous chemical reactions in the vapour phase before striking the surface. Near the surface thermal, momentum, and chemical concentration boundary layers form as the gas stream heats, slows down due to viscous drag, and the chemical composition changes. Heterogeneous reactions of the source gases or reactive intermediate species (formed from homogeneous pyrolysis) occur at the deposition surface forming the deposited material. Gaseous reaction by-products are then transported out of the reaction chamber [39]. Chemical vapour deposition uses chemical reactions whose

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energy is supplied from thermal energy, optical energy, plasma and hotwire processes. These are called thermal CVD, photo, plasma CVD, and hotwire CVD respectively.

Until recently, plasma enhanced chemical vapour deposition (PECVD) was the most commonly used technique for deposition of a-Si:H. A new technique for the deposition of a-Si:H was introduced by Wiesmann *et.al.* in 1979 [72]. This technique relies on the catalytic reaction to fracture silane into Si-H_x (x=1,2,3) radicals by hotwire filament. This technique is referred to as the hotwire chemical vapour deposition (HWCVD) process or catalytic chemical vapour deposition (cat-CVD). For device fabrication Matsumura [20] showed in 1986 that by using HWCVD, device–quality a-Si:H film can be deposited from silane at a substrate temperature of 300 ^{o}C or less with a deposition rate of about 5 Å/s.

(b). DEPOSITION CONDITIONS

The devices studied were produced by members of the research group within the framework of a larger multidisciplinary project. Both HWCVD a-Si:H and transfer printed nc-Si were made available.

The intrinsic amorphous silicon (a-Si:H) was deposited by hot wire vapour deposition on 80 g m^{-2} wood-free paper (pure white mondi rotatrim). Two different deposition systems were used. For the first devices a locally (University of Western Cape) developed chamber, with a maximum sample size of 25 mm was used. For later devices, a commercial system from MVSystem Inc [73], which is equipped with a load-lock and is capable of accepting substrates up to 10 x 10 cm square, was used.

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With the exception of the filaments used, the nominal deposition conditions were identical. For the first devices a single tungsten filament, operating at a temperature of 1800 °C, was employed. In the commercial system an array of thin tantalum wires, at 1600 °C, is used to obtain better uniformity of deposition. In all cases the deposition atmosphere was pure silane gas (SiH_4), and the sample was pre-heated for two minutes (100 ^{0}C) before deposition. The base pressure obtained was 8 x 10^{-8} mbar. In the deposition process the substrate was maintained at a temperature of 100 ^{0}C, a total gas pressure of 80 μbar, flow rate of 60 sccm and a deposition time of approximately 10 minutes, were chosen. The filament current of 14.2 A adjusted to 13.3 A after the gas inlet, and the filament temperature 1800 ^{0}C was maintained. After the deposition, the silane gas was switched off and the sample stage temperature increased to 150 ^{0}C.

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3.1.2. TRANSFER PRINTING

Transfer printing was used to apply the metal contacts (silver layer), indium tin oxide (ITO) film as a window layer for the solar cells, as well as the semiconductor layer on paper substrates. Thin film transistors, field effect transistors, and solar cells based on nc-Si were produced exclusively by printing.

The printed semiconductor layer is a mixture of nanocrystalline silicon powder and polymer binder in an organic solvent. In the nc-Si transistor, the gate, source and drain were printed using silver layers, with the nc-Si semiconductor printed between the source-drain layer and gate layer to form the gate channel. In this case, rubber or linoleum sheet mounted on wood blocks, or massive synthetic rubber block cut as a stamp block was used for transfer printing. All layers, nc-Si as well as silver and ITO

were printed in this way. During the process of printing, the block was inked with the mixture of active material and binder in the solvent, using a roller, and then transferred to the substrate as a first layer. The same process was applied to produce different layers, in order to construct different types of nanocrystalline silicon transistors in the form of top and bottom gate device, as well as solar cells. After each step the block was wiped and pre-wet with solvent. Loose material was removed by brushing between each step.

3.2.1 SAMPLE PREPARATION AND DESCRIPTION

(a). HYDROGENATED AMORPHOUS SILICON DEVICES

For the CVD deposition using the locally produced system, two top gate field effect transistors and two photodiodes were produced in one run. Preceding the HWCVD deposition of a-Si:H the silver base contacts were printed on the paper. The gate channel between the source and drain was made by masking with a thin strip of adhesive tape. During the deposition of the intrinsic amorphous silicon, the substrates were mounted on a steel support with a paper shadow mask on top, see fig 3.2. After deposition the mask was removed by a scalpel and the top contacts printed. The sample was cut leaving four separate devices: T1 and T2 as top gate transistors, C1 and C2 as photo-diodes. For the transistors the top contact was silver and for the photodiodes ITO. The n-i-p photodiode (solar cell) structure was constructed with the i-layer as a-Si:H, the n-layer as silver (Ag) and the p-layer as indium tin oxide (ITO). The p^+-n^- junction was at the ITO/Si interface, the schottky barrier (metal semiconductor junction) at Ag/Si interface, and the depletion layer at both junctions.

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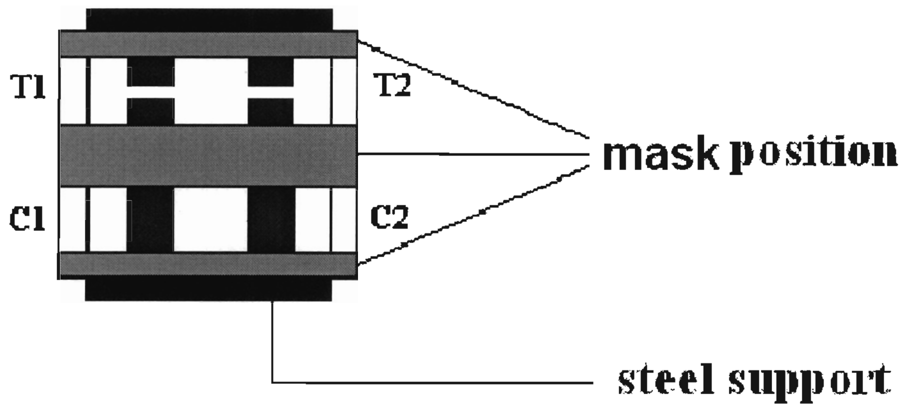

Fig 3.1 Sample configuration preceding the HWCVD process indicating two top gate FET (T1 and T2), and two photodiodes (C1 and C2), mounted on a steel support.

For devices produced in the commercial system, a metal shadow mask with an array of 8mm diameter holes replaced the paper strip mask used in earlier devices (fig 3.1). The build sequence of the solar cell panel is illustrated in figure 3.2. On a 10 x 10 cm piece of paper, ten silver strips of width 5mm and separation of 5mm were printed. In the HWCVD process part of the silver layers and substrate was covered by a paper shadow mask.

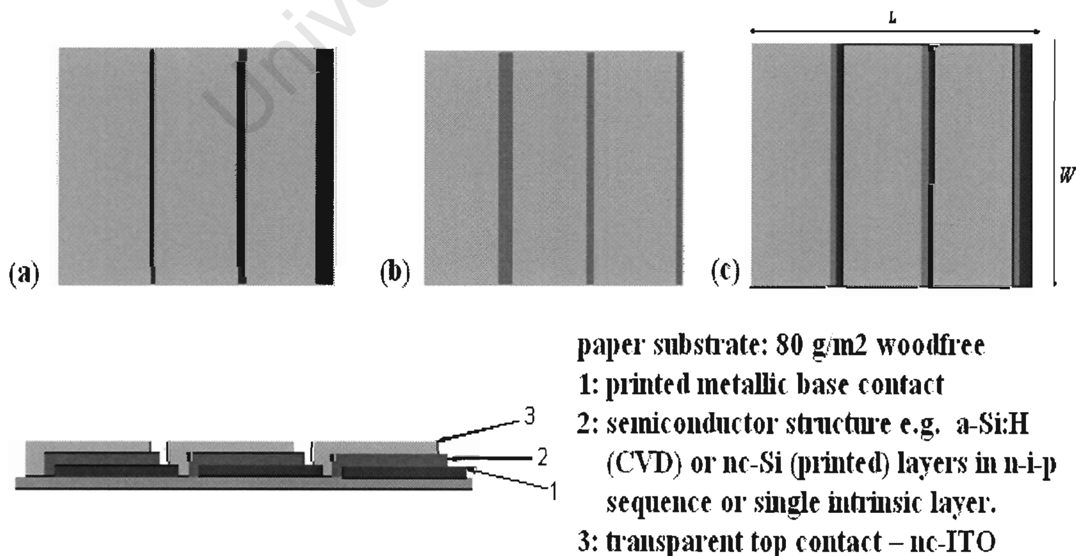

Figure 3.2 Sequence of solar cell panel in top and side view (a) arrangement of silver base contact, (b) arrangement of a-Si:H and (c) final solar cell battery structure.

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The result after deposition was a structure of nearly equally spaced strips of a-Si:H, silver and paper substrates (figure 3.2b). On this structure the window layer was simply applied by painting to achieve a thin layer so that sunlight can penetrate through. The final structure of the solar cell battery is shown in figure 3.2c.

(b). NANOCRYSTALLINE SILICON DEVICES

The nanocrystalline silicon devices, in the form of top gate and bottom gate field effect transistors were produced exclusively by the transfer printing technique, where the drain source and gate terminals were made by the silver layer, and the gate was insulated by the nc-Si layer. The configuration of the layers can be seen in figure 3.3.

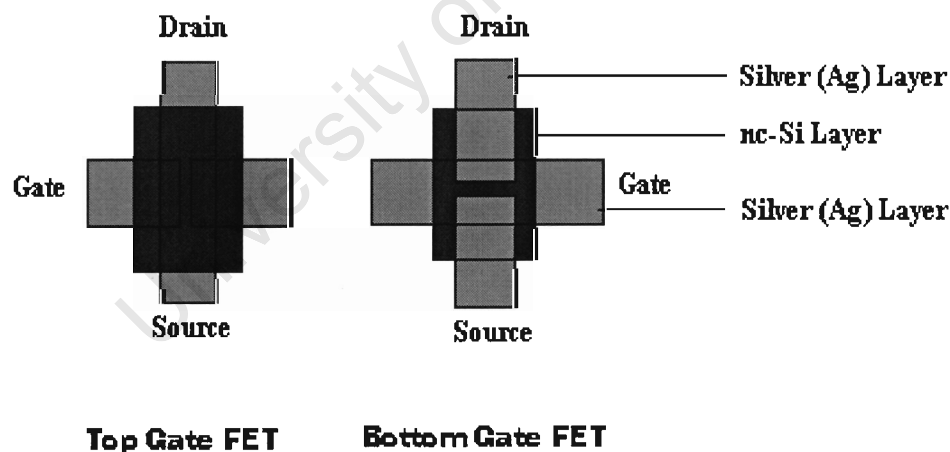

Fig.3.3 Configuration of top and bottom gates nc-Si field effect transistors produced exclusively by transfer printing technique with silver contact layers and nc-Si as semiconductor layer.

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(c). DEVICE MOUNTING

Each device was individually glued on a cardboard base. The electrical contacts were made by M2-brass screws connected with DUPONT 5000 conductor applied by painting.

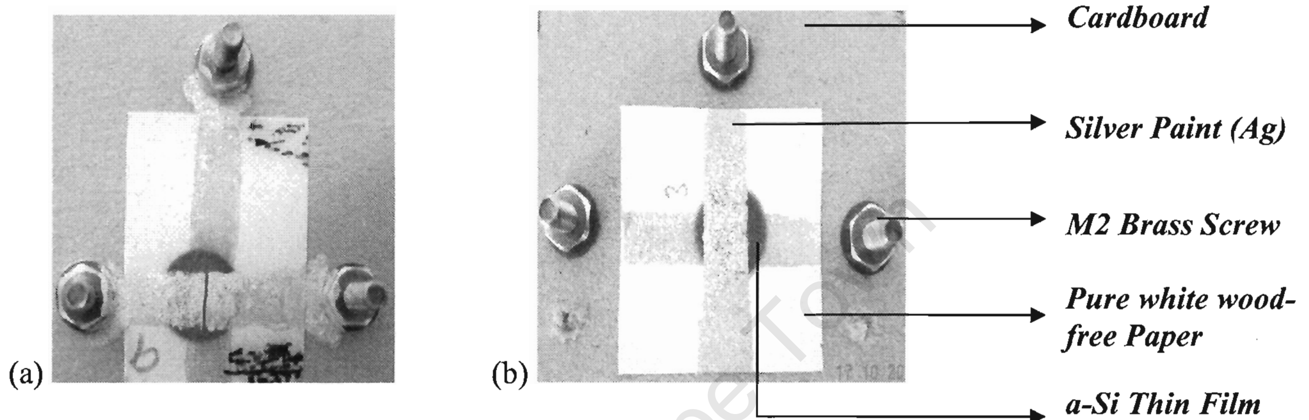

Fig 3.4 Photograph of a bottom (a) and top (b) gate a-Si:H TFT prepared on paper substrate by HWCVD with three electrical contacts made by brass screws.

The drain, source and the gate contacts for the transistors were arranged as shown in the photograph figure 3.4 above.

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Photodiode (Single solar cell)

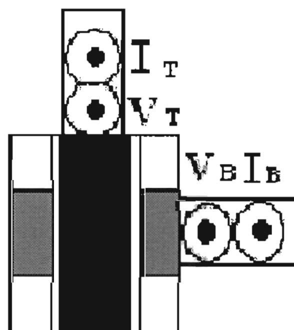

Fig 3.5 Single solar cell sample design with four electrical contacts, where T and B referred to top and bottom.

For the photodiode, four pairs of contacts to monitor current and voltage were applied as shown in fig 3.5. The single solar cells was fabrication on wood free paper substrates using HWCVD techniques with the p^+-n^- junction at ITO/Si, schottky barrier (metal semiconductor junction) at Ag/Si, and the depletion layer at both junctions, and most photoconductivity expected at ITO/Si.

3.3. PROPERTIES OF LIGHT BOX

The light box was used to investigate the illumination changes of the solar cells and the photo diode, as well as the light condition of the devices. The chamber is a square wooden box lined with mirrors on the inside. The internal dimensions of the box are 0.5 x 0.5 x 0.5 m^3. The outside of the box is constructed from supa-wood which is relatively stable under temperature fluctuations. As wood is a poor conductor of heat it is fitted on all sides with forced air cooling. This is necessary because as the glass mirror heats up during operation it expands and after operation when the light is switched off, the glass contracts and it may break [74].

The lamp of the light box is a metal halide lamp with a colour temperature of 5800 K (OSRAM HQI 400 W/D), which is mounted horizontally on the back of the mirrored box; 40 cm from the bottom mirror and 10 cm from the top mirror (see fig 3.6). The sample stage is placed in the middle of the box so that the sample's position is 30 cm below the light bulb. The stage was covered with aluminium foil so as to reflect light from the lamp [74].

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Fig. 3.6 Inside view of the box with metal halide lamp and sample stage [74]

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The use of this mirror box increases the illuminance by a factor of 20, compared to the naked bulb at the same distance (40cm). Before the actual experiment the conditions of the box (inside) were investigated as follows, an electronic thermometer and the light meter were placed inside the box under operational conditions to measure the environment at the sample position. The temperature was found to stabilize at $30 \pm 1\ ^{o}C$ and the intensity of $75 \pm 5 \times 10^3$ lux [74].

CHAPTER 4

ELECTRICAL CHARACTERISATION

In this chapter the general methods and theory of the electrical characterization of the two types of device studied are presented, for the transistor structures, the important quality is the carrier field effect mobility which is determined from the electrical parameters as described below. The solar cell structures are characterised in terms of their behavior as photo-diodes.

4.1 TRANSISTOR CHARACTERISATION

The simple electrical circuit, as shown in fig 4.1, for characterisation of transistors was built using two-power supplies (ISO-TECH MODEL: IPS60A), a picoammeter (model:DPM-111) and a digital voltmeter (KEIHTLEY 2000 model) with the device under the investigation forming the central element in the circuit.

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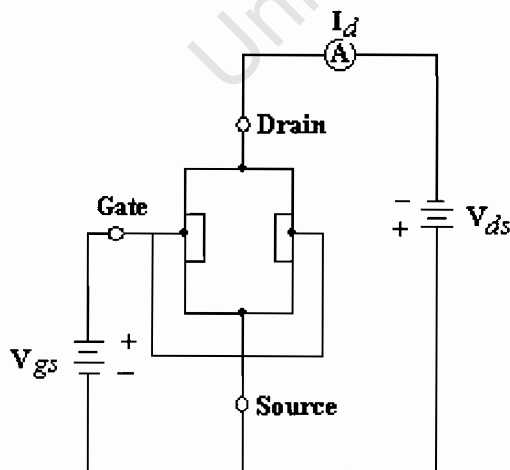

Fig 4.1. P-channel MS-FET (junction FET) set-up circuit with the source terminal grounded. For reverse bias measurements the polarity of gate terminal was changed.

The I-V characteristics measurements according to the general example in fig. 2.7 were obtained were by drain voltage V_{ds} measuring the current I_d (V_{ds}) flowing from drain to source for a set of constant gate-source voltage V_{gs}. The transfer characteristics were determined by measuring the drain current I_d (V_{gs}) flowing from drain to source as a function of the gate voltage V_{gs} fo a set of constant drain-source voltages V_{ds}.

Bias stress effects in each sample were determined by measuring the drain current as a function of time with constant applied gate-source voltages and drain-source voltages, and use their characteristic curves to see the stress at each set of constant voltages applied. The amplification factor, A, of each transistor was determined from the slope of current-voltage characteristics curves and the transfer characteristics curves using eq. 4.1 [63]

$$A = g_m \times r_d \tag{4.1}$$

where

$$g_m \equiv \frac{\partial I_d}{\partial V_{gs}} \approx \frac{\Delta I_d}{\Delta V_{gs}}, \tag{4.2}$$

is the mutual conductance, which is the slope of transfer characteristics (I_d vs V_{gs}) curve. The drain (or output) resistance, r_d, is defined as

$$r_d \equiv \frac{\partial V_{ds}}{\partial I_d} \approx \frac{\Delta V_{ds}}{\Delta I_d}, \tag{4.3}$$

which is the reciprocal of the slope of current-voltage characteristic *(I_d vs V_{ds})* curve. From the drain current-voltage and the transfer characteristics curves, the pinch off voltage (V_p), the threshold voltage (V_t) and the breakdown voltages of the transistor devices was determined.

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The field effect mobility can be estimated from the mutual conductance at a given V_{ds} by

$$\mu_{FE} \equiv \frac{L}{WC_g} \times \frac{g_m}{V_{ds}} \tag{4.4}$$

where L is the length of the gate, W is the gate width and C_g is the gate capacitance. The largest uncertainty is in determining the effective gate capacitance. In this work, the gate and source-drain contacts are assumed to form a parallel plate capacitor with the silicon as the dielectric layer. The effective capacitance is then

$$C_g \equiv K_{Si}\varepsilon_o \frac{W^2}{d} \tag{4.5}$$

where K_{Si} is taken to be the static dielectric constant of silicon, with a value of 11.7 [75]. The values of C_g used are given in table 5.1.

The pinch-off voltage, V_p occurs when the depletion layers at the source-gate and gate-drain junctions meet. At drain voltages above the pinch-off, the depletion layers extend further into the drain region, but remain approximately constant in the channel (as seen in fig 4.2). The current therefore remains essentially constant depending on the device temperature until the voltage reaches such a value that breakdown occurs. Carriers arriving at the pinch-off point, E are swept across the depletion layer into the drain region.

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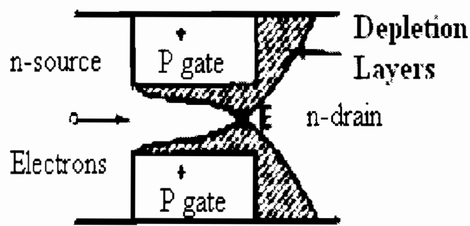

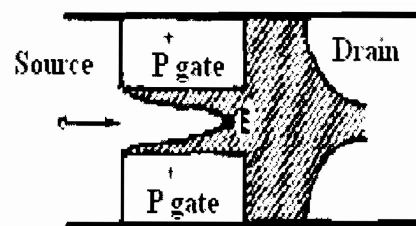

Figure 4.2 The Structure of Field Effect Transistor shows the condition of drain voltage just before the pinch off voltage (1) and above the pinch off voltage (2)

Applying a negative voltage to the gate also increases the size of the depletion layers. As the gate voltage is increased, the depletion zone spread further into the n-type material, narrowing the channel through which the current must pass from the source to the drain and thus decreasing the conductivity of the device.

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4.2 SOLAR CELL CHARACTERISATION

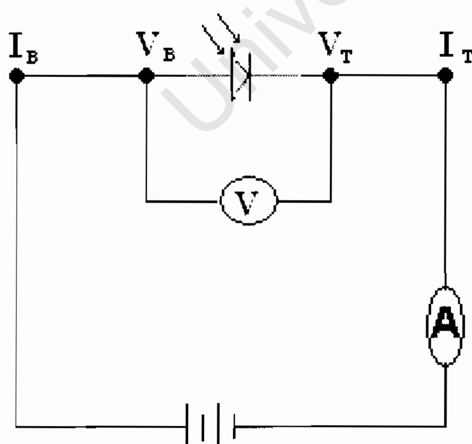

Fig 4.3 Set-up for current-voltage characteristics measurements of photodiode/solar cell structures (photo-voltaic battery and single solar cells), with the voltages V_B, V_T and the currents I_T, I_B described in fig 3.5.

The current-voltage characteristics measurements of the solar cells were carried out by placing the devices in different ambient conditions, and applying the voltage from the power supply to determine how current changes in each condition using the circuit shown in fig 4.3 with the voltages V_B, V_T and the currents I_T, I_B defined as top and bottom voltages and currents as described in fig 3.5. The three conditions applied when determining the I-V characteristics were darkness, ambient light and simulated daylight using the light box described in section 3.3. From the shift of the I-V curves, the diode and photodiode behaviour of the devices can be determined. Also the photocurrent can be directly measured.

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CHAPTER 5

EXPERIMENTAL METHOD

Table 5.1 lists the devices studied in this project, including details of their preparation conditions and physical geometry. For the transistors, devices labelled FET are junction FETs (MS-FET) produce on the smaller substrate using the locally manufactured deposition system. Devices labelled TFT are the junction FETs produced on the larger substrates using the commercial system. Devices labelled nc-FET are fully printed nc-Si junction FETs. All the solar cell structures were produced with CVD grown a-Si:H

Table 5.1 shows the properties of the devices in details

Device	Type	Gate Length (L)	Gate Width (W)	Si Layer Thickness (d)	Deposition condition	Estimated C_g values
FET 1	FET	≈ 400 μm	8 mm	~1 μm	HW-CVD	6.63 nF
TFT 1	FET	≈ 400 μm	5 mm	~1 μm	HW-CVD	2.59 nF
nc-FET 1	FET	≈ 400 μm	6 mm	~50 μm	Printing	0.075 nF
FET 2	FET	≈ 400 μm	8 mm	~1.2 μm	HW-CVD	6.24 nF
TFT 2	FET	≈ 400 μm	5 mm	~1.1 μm	HW-CVD	2.353 nF
nc-FET 2	FET	≈ 400 μm	6 mm	~42 μm	Printing	0.089 nF
		Geometry				
PV Battery	Solar cell	10 strips 10 x 5 cm			HW-CVD	
C1	Solar cell	8 x 8 mm			HW-CVD	
C2	Solar cell	8 x 8mm			HW-CVD	

The devices were mounted as described in section 3.2.1.

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The bias stress effect of a-Si:H top gate thin film transistors (TFTs) results was studied out by plotting the change in drain-source current as a function of time taken in an interval of 2 minutes, to determine the current leakage on the device as the constant gate and drain voltages applied as seen in figure 6.1.

The monolithic solar cell was also tested to see if an open circuit voltage and short circuit current could be obtained directly in sunlight. This was determined by comparing the solar cell with the multimeter, in the dark condition and in sunlight.

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CHAPTER 6

RESULTS

6.1 BIAS STRESS EFFECT

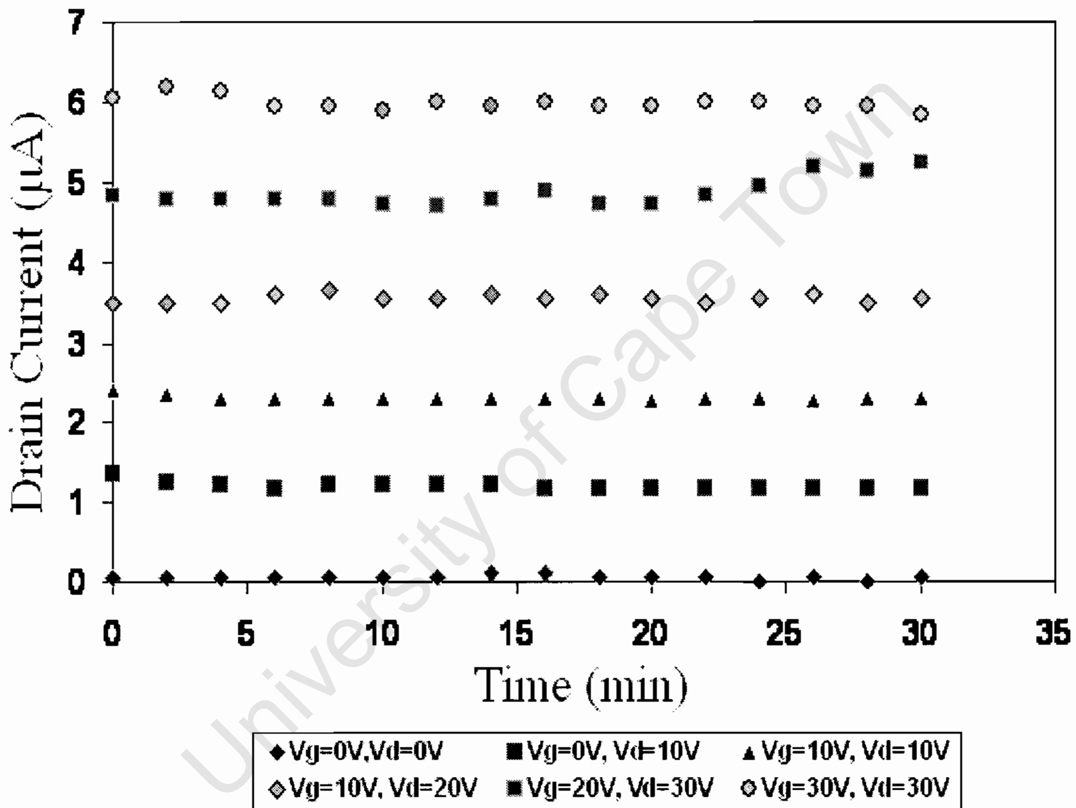

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Fig 6.1 Drain- source current (I_d) as a function of time taken under constant applied drain V_d and gate V_g voltages, to determine the bias stress effect on a-Si:H top-gate thin film transistor.

Figure 6.1 shows the bias stress effect on TFT 1. As can be seen the device shows the small bias stress effect on the first small constant gate and drain voltages applied, while it shows some fluctuations as the applied voltages increases (i.e. V_g=20V, V_d=30V), hence the current leakage increase as the applied voltages increases.

6.2 FET SERIES MS-FETs

This series of devices represents the first ever silicon transistors produced on paper substrates, which differ from the later series by a slight change in geometry of the shadow mask and substrate size as described earlier.

Drain Current as a function of drain voltage at constant gate voltages			
	Vds =10.0V	Vds =20.0V	Vds =30.0V
Vgs(V)	Ids (µA)	Ids (µA)	Ids (µA)
0	0	0	0
5	0.53	0.52	0.53
10	1.06	1.07	1.075
15	1.07	1.561	1.545
20	1.07	1.985	2.051
25	1.07	1.985	2.549
30	1.07	1.985	2.95
35	1.07	1.985	2.95
40	1.07	1.985	2.95
45	1.07	1.985	2.95
50	1.07	1.985	2.95
55	1.08	1.985	2.95
60	1.57	1.985	2.95

(a)

Drain Current as a function of Gate voltage at constant drain voltages				
	Vds =0.00V	Vds =10.0V	Vds=20.0V	Vds =30.0V
Vgs (V)	Ids (µA)	Ids (µA)	Ids (µA)	Ids (µA)
0	0	0	0	0
5	0	0	0	0.034
10	0	0	0	0.035
15	0.167	0	0	0.035
20	0.69	0	0	0.035
25	1.18	0.0005	0	0.035
30	1.72	0.605	0.005	0.035
35	2.243	1.124	0.135	0.035
40	2.75	1.679	0.598	0.035
45	3.226	2.12	1.093	0.135
50	3.72	2.579	1.57	0.598
55	4.238	3.09	2.128	1.135
60	4.76	3.669	2.585	1.595

(b)

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Table 6.1 Current –voltage characteristics (a) and the transfer characteristics (b) measurements results of a top gate a-Si:H metal field effect transistor.

Table 6.1 shows the current-voltage characteristic data of a top gate amorphous silicon (a-Si) metal semiconductor field effect transistor (MS-FET). The data were taken at room temperature using the p-channel circuit set-up shown in fig 4.1. From the results, the I-V characteristics curves and the transfer characteristics curves of the MS-FET devices were determined.

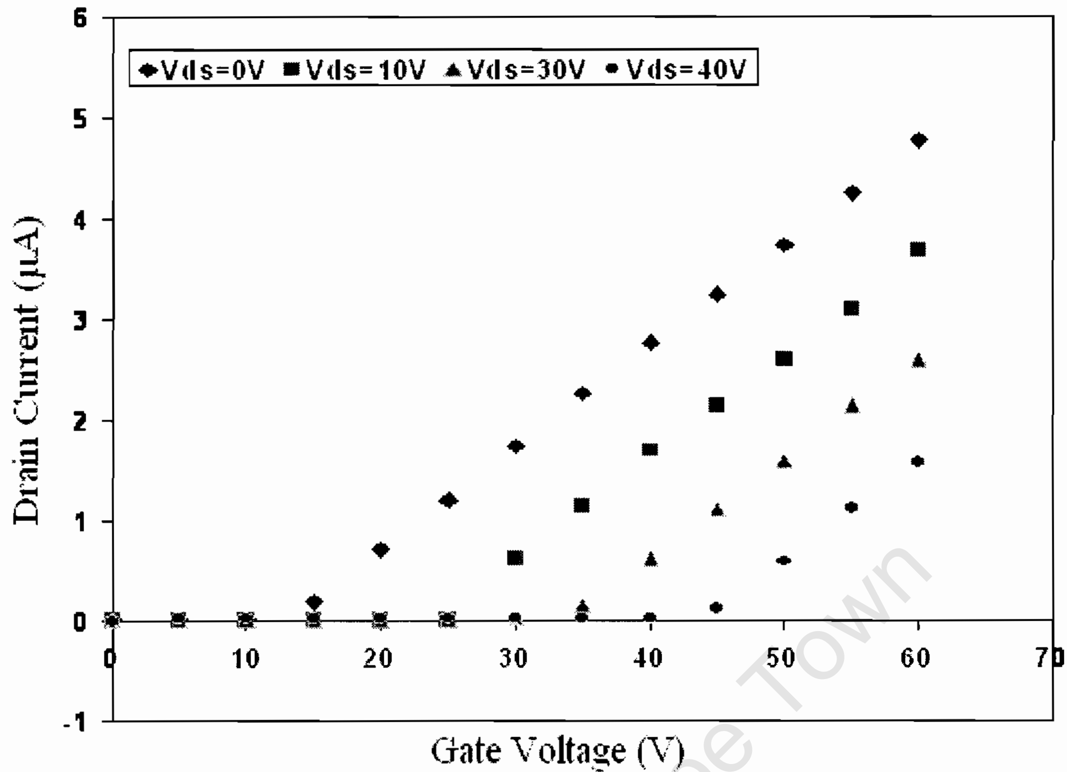

Fig 6.2 Transfer characteristics curves for the enhancement mode of the top gate a-S:H MS-FET prepared on paper substrate by HWCVD technique.

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The transfer characteristics curves (fig 6.2) $I_d(V_{gs})$ as defined in chapter 4.1 shows the behaviour of the top gate FET 1 device with different drain-source voltages V_{ds} applied and a threshold (turn on) voltage of 25V at 0.005 μA drain current is obtained, when a constant drain-source voltage of 10V is applied to the device (shown by red squares in fig 6.2).

The slope of the transfer characteristics curves was used to determine the mutual conductance, g_m. Using equation 4.2 the value of the mutual conductance was found to be $g_m = 0.0644 \pm 0.0015$ μA/V.

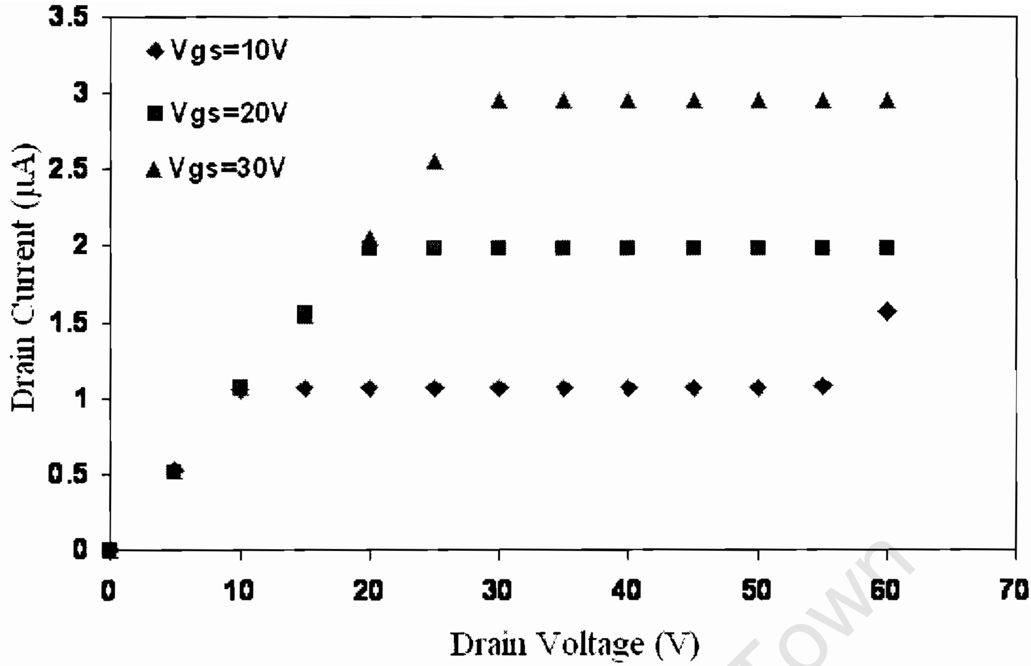

Fig 6.3 I-V characteristics curves for the enhancement mode of the top gate a-S:H MS-FET prepared on paper substrate by HWCVD technique.

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Figure 6.3 shows the behaviour of the I-V characteristics curves $I_d(V_{ds})$ of the top gate FET1 device, with pinch-off voltage of 10V at 1.075 μA drain current, when a gate-source voltage of 10V is applied. The breakdown voltage (maximum voltage at constant gate voltage) occurs at 55 Volts drain voltage. The reciprocal slope of characteristic curves was used to determine the drain (or output) resistance, $r_{d,}$ of the device, using Eq.4.3 and was found to be $r_d = 74.6 \pm 0.11$ (MΩ).

Finally by using the results of mutual conductance and drain resistance from the transfer and the I-V characteristics curves respectively, using Eq. 4.1, the amplification factor is estimated as $A = 4.81$, and the field effect mobility according to Eq. (4.4) is $\mu_{FE} = 0.0486 \pm 0.0025$ m^2 V^{-1} s^{-1}

6.3 TFT SERIES TRANSISTOR

This is the second series of devices produced on the larger area substrates using commercial CVD system.

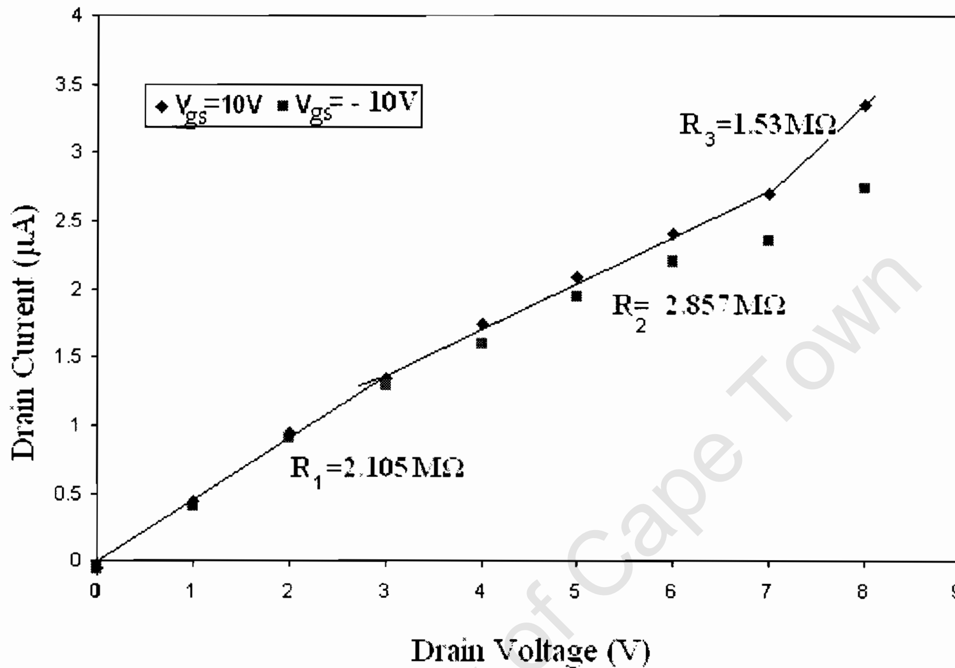

Fig 6.4 I-V characteristics curves $I_d(V_{ds})$ for the p-channel enhancement mode of bottom gate a-S:H thin film transistor (TFT) prepared on a paper substrate by HWCVD technique. The solid lines are a guide to the eye for the +10V gate voltage with the change of slope(resistance).

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Figure 6.4 shows I-V characteristics curves of a top gate FET (TFT1). The pinch-off voltage is approximately 3V at a drain-source current of 1.35 μA, when a gate voltage of 10V is applied. The current above pinch-off voltage was not exactly constant as expected, because of a current leakage on the device. The breakdown voltage of the device occurs at a drain voltage of 7V with a drain current (turn on current) of 2.7 μA. As before, by using Eq. 4.3 the reciprocal of the slope of I-V characteristics curves

determines the drain resistance of the device and the value of $r_d = 2.11 \pm 0.01$ MΩ was obtained, when a constant gate voltage V_{gs} of 10V is applied.

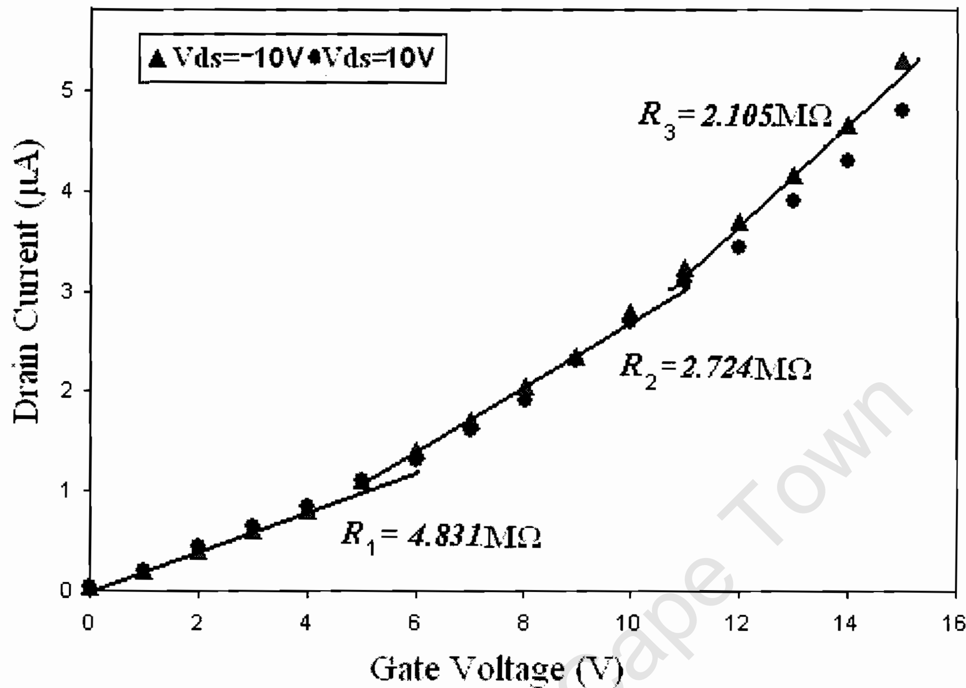

Fig 6.5 Transfer characteristic curves $I_d(V_{gs})$ at constant applied drain voltages for enhancement mode of bottom gate a-S:H thin film transistor (TFT) prepared on a paper substrate by HWCVD technique. The solid lines are a guide to the eye for -10V drain voltage with the change of slope (resistance).

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From the transfer characteristic curves (fig 6.5) of a threshold (turn on) voltage of 4 V at 0.8 μA drain current was found at constant drain-source voltage of V_{ds} = 10V. From the slope of the transfer characteristics curves and by using equation 4.2, the mutual conductance, g_m of the device, was found to be $g_m = 0.344 \pm 0.015$ μA/V.

Finally by using the results of mutual conductance and the drain resistance from the transfer and the I-V characteristics curves respectively, using Eq. 4.1, the amplification factor was estimated as $A = 0.726$, with the field effect mobility of $\mu_{FE} = 1.063 \pm 0.013$ m^2 V^{-1} s^{-1} according to Eq. (4.4).

6.4 NANO-CRYSTALLINE TRANSISTORS

In nano-crystalline silicon field effect transistors (nc-Si FET), the current-voltage characteristics curves show the behaviour of the transistor with a different division of the saturation region as shown in fig 6.6 for nc-Si.

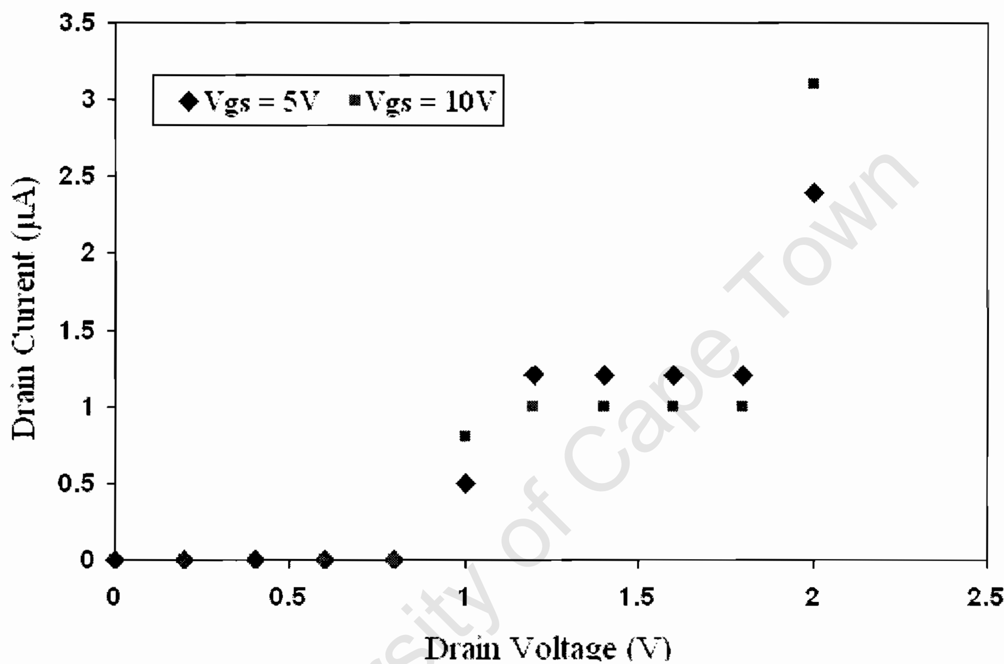

Fig 6.6 I-V characteristics curves $I_d(V_{ds})$ of the top gate nanocrystalline field effect transistor at two constant applied gate voltages for the p-channel enhancement mode prepared on a paper substrate by transfer printing technique.

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The pinch-off voltage of 1.2V was obtained at a drain current of 1.35 μA, when a voltage of 5V is applied to the gate. In a similar manner as for the a-Si:H field effect transistors, by using the reciprocal of the slope of characteristics curve the drain resistance of the device was determined using eq. 4.3, and the value of r_d = 1.25 ± 0.11 MΩ was obtained. The breakdown voltage of this nc-Si transistor occurs at a drain voltage of approximately 1.8V and a drain current (off current) of 1.1 μA, when a constant gate voltage of V_{gs} = 10V is applied to the gate.

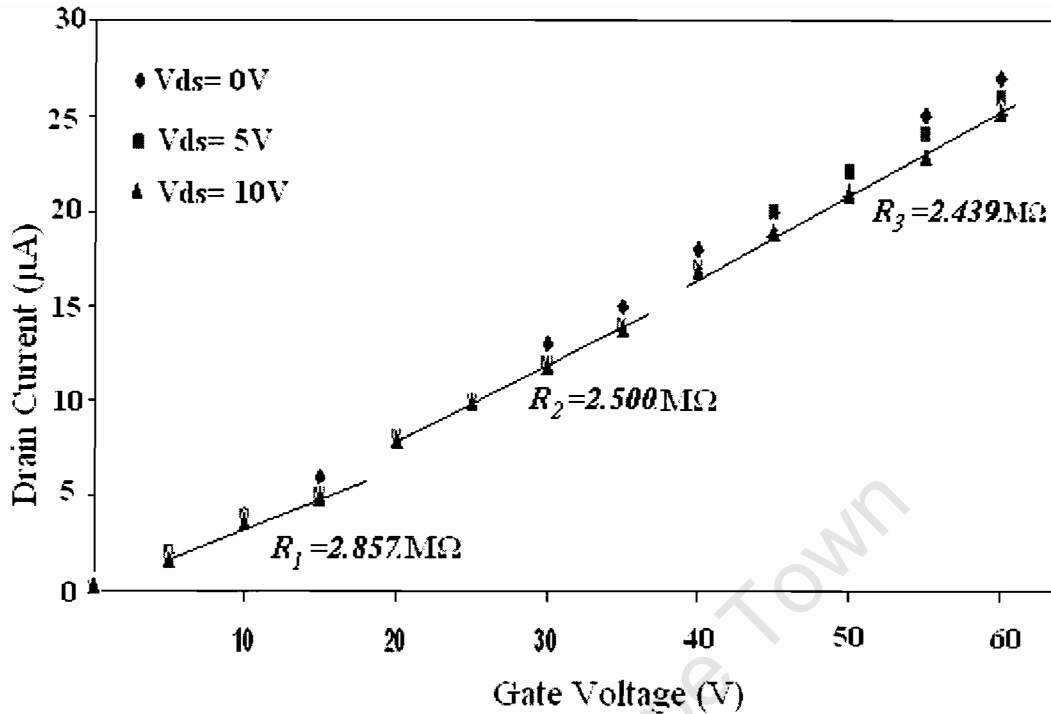

Fig 6.7 Transfer characteristic curves $I_d(V_{gs})$ of top gate V_{gs} nanocrystalline field effect transistor at constant applied drain voltages for the p-channel enhancement mode prepared on a paper substrate by transfer printing technique. The solid lines are a guide to the eye for 10V drain voltage indicating a change of slope (resistance).

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The transfer characteristics curves of this top-gate nano-crystalline silicon field effect transistor (nc-Si FET) in fig. 6.7 show no clear transistor behaviour, since the graph shows almost ohmic resistance. Hence the threshold (turn on) voltage of the device was not easily seen. But closer inspection shows a threshold voltage at approximately 15 V gate voltage and 5.4 μA drain current when a constant voltage of 10V is applied between the source and the drain of the device. From the slope of transfer characteristic curve, using equation 4.2, the mutual conductance of the device, with the value of $g_m = 0.427 \pm 0.02$ μA/V was found.

Finally by using the results of mutual conductance, g_m and the drain resistance, $r_{d,}$ from the transfer and the characteristics curves respectively, the amplification factor in this device was estimated as A = 0.533 and the carrier field effect mobility, μ_{FE} = 38.16 ± 0.25 $m^2 V^{-1} s^{-1}$ was obtained.

6.5 SOLAR CELL RESULTS

The behaviour of the amorphous silicon solar battery was determined from its current-voltage characteristics curve under different ambient conditions. As can easily be seen from the figure 6.8, the device shows a diode effect in the voltage range from -10V to 30V. The characteristic curves also show that the current changes as the illumination on the solar cell changes.

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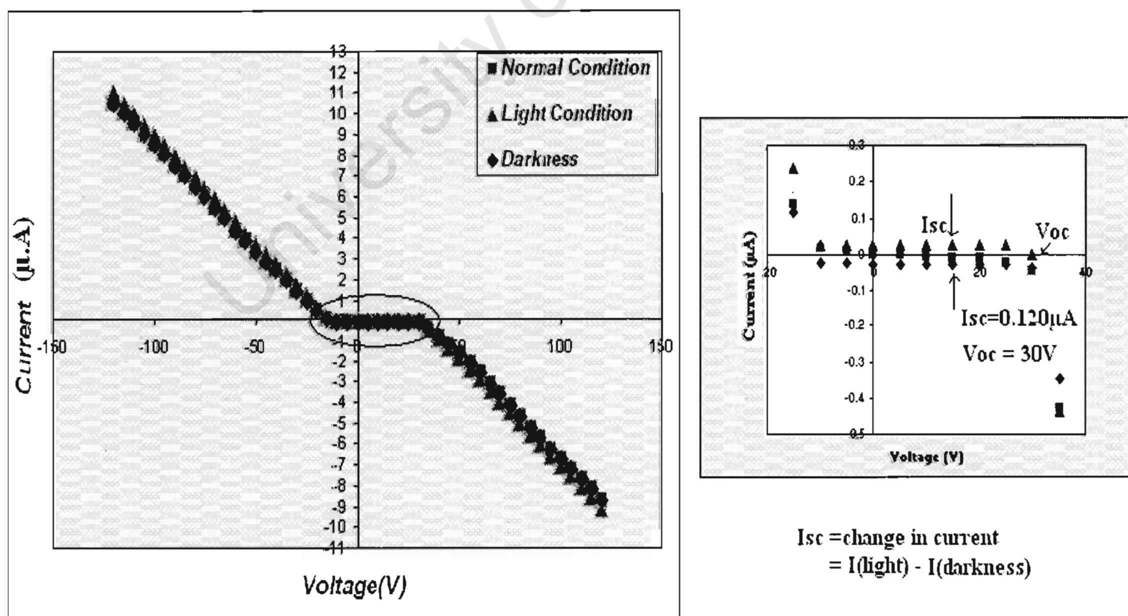

Fig 6.8 Current-Voltage characteristic of the solar cell panel prepared on paper substrates by HWCVD techniques, with i-layers made of amorphous silicon materials. The circled part of the I-V curves is shown enlarged on the right.

The circled part of the I-V characteristics curves of the solar battery, shows the measured short circuit current, $I_{sc} = 0.120$ µA and an open voltage at $V_{oc} = 30$ volts.

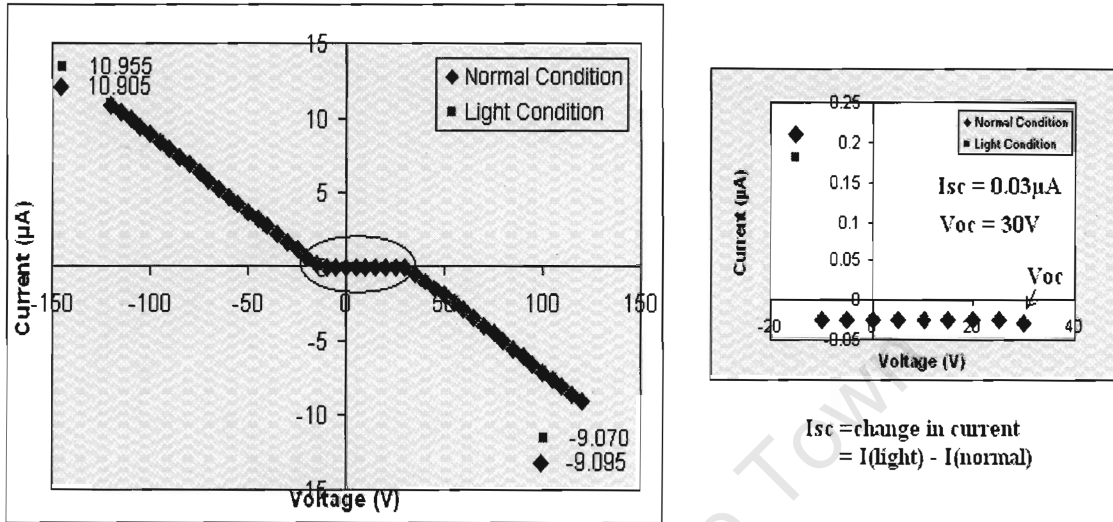

Fig 6.9 Current-Voltage characteristics curves of single solar cell (capacitor) prepared on paper substrates by HWCVD techniques. The circled part of the I-V curves is shown enlarged on the right.

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The single solar cell structures show similar diode behaviour as the monolithic battery. As can be seen in figure 6.8 and 6.9, the shape of these curves is similar, with a diode effect in the voltage range from -10V to 30V. And the characteristic curve shows a slight change of current as the illumination changes on the device. There is also a photoconductivity effect, which, however, is lower than in the solar battery in fig 6.8. The circled part of the I-V characteristics curves (fig. 6.9) of the single solar cell, shows the measured short circuit current, $I_{sc} = 0.03$ µA and an open voltage at $V_{oc} = 30$ volts.

CHAPTER 7

DISCUSSION

The current –voltage characteristic curves of both studied transistors series show that, when a positive voltage is applied to the drain, electrons in the source are attracted into the drain and flow through the channel between the source and drain. As the drain voltage increases, depletion layers associated with the p-n junction increase in size and reduce the cross sectional area of the channel, thus increasing the drain-source resistance of the device, since:

$$R = \frac{\rho L}{A} \qquad 7.1$$

The different pinch-off condition was reached at a low drain voltage for different devices, and the drain voltage above pinch-off voltage was clearly seen to be constant at first series a-Si:H FET and nc-Si FET and not on second series a-Si:H FET (TFT) because of some leakage current on the device, and a family of characteristics was generated for different values of gate bias (as shown in fig 6.3, fig 6.4, and fig 6.6). The gate voltage is therefore used to modulate the channel conductivity between the source and the drain in our devices.

The second series of the top gate a-Si:H TFT produced by HWCVD on paper substrate show standard characteristic results with threshold voltages $V_t = 4$V and the pinch off condition was reached at $V_p = 3$V when a voltage of 10V is applied between the gate and the source, Using the drain resistance r_d, and the mutual conductance g_m,

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the amplification factor A of 0.726, a high carrier field effect mobility, μ_{FE} = 1.063 ±0.0125 m^2 V^{-1} s^{-1} was obtained. Therefore highly stable thin film transistors can be prepared on a wood free paper by the HWCVD process.

The first MS-FET series transistors (chapter 6.2) show good characteristics, as it takes a small current (drain current, I_d = 0.005 μA) to reach the threshold (turn on) voltage (V_t = 25V), when a constant drain voltage of V_{ds} = 10V is applied in both cases between the drain and the source. The pinch off condition is reached at a lower drain voltage (V_p = 10V) with a drain current of 1.075 μA, when a constant gate voltage of V_{gs} = 10V is applied in both cases between the gate and the source. By using the drain resistance from the I-V characteristics and the mutual conductance from the transfer characteristics, the device shows high amplification factor of 4.81, with carrier field effect mobility of 0.0486 ± 0.0025 m^2/Vs.

In case of the nano-crystalline field effect transistors (chapter 6.4), the characteristic results show a pinch off condition at a lower drain voltage (V_p = 1.2V) than in a-Si:H devices at a drain current of 1.35 μA, and a threshold (turn on) voltage at, $V_t \approx$ 15V with a drain current of 5.4 μA, when a constant drain-source voltage of 10V is applied. From drain resistance and mutual conductance the device shows amplification factor of 0.533, with carrier field effect mobility of 38.16 ± 0.25 m^2/Vs .

There was a large variation of carrier field effect mobility, μ_{FE} = 0.0486 m^2/Vs for the a-Si:H FET and μ_{FE} = 38.6 m^2/Vs for nc-Si FET, which is three orders of magnitude. These kinds of variations were caused by the different silicon thickness layer for these

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devices (table 5.1), since according to Eq. 4.4 and Eq. 4.5, it shows that the higher the thickness layers, the lower the gate capacitance and higher field effect mobility.

The current-voltage characteristics show clearly the different onset of the pinch-off voltage and a clear voltage region before the breakdown voltages occurs. This was less so obvious for the printed nc-Si FET, but the different regions on the characteristics could be discerned. When two sets of curves between the two different materials (a-Si:H and nc-Si) compared, is easily seen that they both show the same behavior, as the maximum drain current in the drain current versus gate voltage curves increases with the decreasing constant drain source applied. While in the current-voltage characteristics curves, the maximum drain current increases with the increasing gate voltages applied as it was expected.

In the solar cells, the current voltage characteristic curves show an effect on the current as the illumination changes (as shown in fig 6.8). The diode effect of the devices was seen when the current breakdown between the range of -10V and 30V, with a short circuit current of I_{sc} = 0.120 μA and an open voltage at V_{oc} = 30V. Small changes on illumination are seen for the single solar cell (fig 6.9), and a similar diode behavior was observed between -30V and 10V with a short circuit current I_{sc} = 0.03 μA and an open voltage at V_{oc} = 30V.

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CHAPTER 8

CONCLUSION

In the solar cells, the current-voltage characteristic curves show an effect on the current as the illumination changes. The diode effect of similar kind was seen in both the solar battery and single solar cell structures with a short circuit current of I_{sc} = 0.120 μA and I_{sc} = 0.03 μA respectively at an open voltage of V_{oc} = 30 volts . Thus the fabrication of n-i-p solar cells on wood free paper substrates using HWCVD techniques with i-layer as a-Si:H, n-layer as silver (Ag) and p-layer as indium tin oxide (ITO) has been successfully achieved without back reflectors at low operating temperature.

The I-V characteristic curves $I_d(V_{ds})$ of the MS-FET series show that above the pinch-off voltage the current remains nearly horizontal, i.e. the conductivity is virtually independent of V_{ds} in this region. A small change in gate voltage causes a large variation in the current from the source to the drain, so the field effect transistor can act as an amplifier. The slope of the characteristics curves (I_d/V_{ds}) indicates that the input impedance of the transistor is high, and when the gate voltage is increased, the depletion zone spreads further into the semiconductor material, narrowing the channel through which charge carriers must pass from the source to the drain and thus decreasing the conductivity of the device. These features all combine to offer an attractive amplifying device. Hence we produce a working FET with a field effect mobility of 0.0486 ± 0.0025 m^2/Vs. Therefore MS-FET can be fabricated on a wood-free paper substrate using HWCVD technique.

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For the TFT series produced FETs on a wood-free paper substrate by HWCVD technique, using hydrogenated amorphous silicon as an active thin film, the calculated carrier field effect mobility of $\mu_{FE} = 1.063 \pm 0.0125$ m^2/Vs is obtained, with threshold voltages of approximately 4 Volts. The TFT performance is combined with a low bias stress effects. Hence we have fabricated quality TFTs on a flexible, and low cost substrate of paper using HWCVD technique, since high carrier mobilities, low leakage currents and low threshold voltages are the most desirable properties for high performance active matrix LCD application.

Nano-crystalline silicon transistors prepared by transfer printing technique on wood-free paper substrates show I-V characteristics results with a pinch off voltages at approximately 1.2V. And the current above the pinch-off voltage remains constant until the breakdown voltage (maximum voltage) of approximately 1.8V occurs. A high carrier field effect mobility of $\mu_{FE} = 38.16 \pm 0.25$ $m^2V^{-1}s^{-1}$ was attained. Hence a working device of nc-Si FET series with high field effect mobility was successfully prepared on a paper substrate.

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The results from the field effect transistors (FETs) based on amorphous silicon thin film are surprisingly good, and definitely show good promise for further development of these types of devices on a paper substrates. This was less obvious for the printed nc-Si FET, but the different regions on the characteristics could be discerned. Hence it has been successfully proven that a range of devices can be fabricated on a flexible, low cost substrate of pure white wood free paper using hot wire chemical vapour deposition (HWCVD) and transfer printing techniques or the combination of both.

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APPENDIX

A. SOLAR CELL CHARACTERISTICS MEASUREMENTS

Results In the Darkness Condition Range from the Multimeter=10mA			Results In the Light Condition Range from the Multimeter=10mA			Results In the Normal Condition Range from the Multimeter=10mA		
	Negative Polarity(V)	Positive Polarity(V)		Negative Polarity	Positive Polarity		Negative Polarity(V)	Positive Polarity(V)
Voltage(V)	Current(micr.A)	Current(micr.A)	Voltage(V)	Current(micr.A)	Current(micr.A)	Voltage(V)	Current(micr.A)	Current(micr.A)
0	-0.026	-0.025	0	0.025	0.025	0	0	0.045
5	-0.025	-0.025	5	0.025	0.025	5	0.005	0.043
10	-0.023	-0.026	10	0.028	0.025	10	0.01	0.038
15	0.115	-0.027	15	0.235	0.025	15	0.14	0.035
20	0.489	-0.028	20	0.756	0.025	20	0.595	0.035
25	0.97	-0.029	25	1.27	0.025	25	1.125	0.023
30	1.438	-0.035	30	1.751	0	30	1.585	0
35	1.955	-0.345	35	2.263	-0.435	35	2.125	-0.471
40	2.439	-0.76	40	2.765	-0.941	40	2.588	-0.975
45	2.888	-1.169	45	3.25	-1.425	45	3.05	-1.422
50	3.345	-1.625	50	3.735	-1.882	50	3.515	-2.021
55	3.887	-2.105	55	4.222	-2.389	55	4	-2.495
60	4.377	-2.579	60	4.79	-2.9	60	4.515	-3
65	4.98	-3.122	65	5.33	-3.464	65	5.025	-3.548
70	5.485	-3.61	70	5.88	-4	70	5.56	-4.08
75	5.98	-4.158	75	6.415	-4.499	75	6.055	-4.591
80	6.495	-4.7	80	6.914	-5.021	80	6.535	-5.078
85	6.999	-5.23	85	7.445	-5.56	85	7.075	-5.6
90	7.505	-5.745	90	7.96	-6.065	90	7.57	-6.092
95	8.045	-6.25	95	8.49	-6.58	95	8.1	-6.6
100	8.515	-6.76	100	9.005	-7.078	100	8.6	-7.075
105	9.005	-7.26	105	9.505	-7.575	105	9.061	-7.58
110	9.535	-7.733	110	9.999	-8.055	110	9.57	-8
115	10.015	-8.199	115	10.5	-8.575	115	10.035	-8.56
120	10.518	-8.725	120	11.035	-9.075	120	10.54	-9.105

Table (a).The current voltage measurements results p-n junction monolithic solar cell taken in different condition (dark, normal and light), showing how the current changes when voltages applied

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B. PHOTO-DIODE CHARACTERISTICS MEASUREMENTS

Results In the Normal Condition
Range from the Multimeter=10mA

	Negative Polarity(V)	Positive Polarity(V)
Voltage(V)	**Current(micr.A)**	**Current(micr.A)**
0	0	-0.025
5	0	-0.025
10	0	-0.025
15	0.21	-0.025
20	0.715	-0.025
25	1.238	-0.025
30	1.727	-0.028
35	2.251	-0.46
40	2.745	-0.975
45	3.23	-1.45
50	3.715	-1.924
55	4.238	-2.415
60	4.75	-2.938
65	5.305	-3.48
70	5.84	-4
75	6.342	-4.513
80	6.89	-5.06
85	7.42	-5.57
90	7.933	-6.1
95	8.439	-6.6
100	8.975	-7.115
105	9.441	-7.599
110	9.945	-8.1
115	10.445	-8.625
120	10.905	-9.095

Results In the Light Condition
Range from the Multimeter=10mA

	Negative Polarity	Positive Polarity
Voltage(V)	**Current(micr.A)**	**Current(micr.A)**
0	-0.025	-0.025
5	-0.025	-0.025
10	-0.025	-0.025
15	0.18	-0.025
20	0.675	-0.025
25	1.21	-0.025
30	1.705	-0.028
35	2.245	-0.43
40	2.74	-0.915
45	3.225	-1.395
50	3.699	-1.88
55	4.18	-2.382
60	4.755	-2.915
65	5.3	-3.46
70	5.815	-4
75	6.358	-4.52
80	6.888	-5.025
85	7.399	-5.579
90	7.925	-6.052
95	8.465	-6.579
100	8.95	-7.063
105	9.456	-7.555
110	9.928	-8.085
115	10.45	-8.565
120	10.955	-9.07

Table (b) The current voltage measurements results of p-n junction single solar cell taken in different condition (normal and light), showing how the current changes when voltages applied.

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TABLE (C) AND (D) SHOWS THE BIAS STRESS MEASUREMENTS RESULTS FOR SECOND SERIES FET (THIN FILM TRANSISTOR.)

TOP GATE THIN FILM TRANSISTOR BIAS STRESS RESULTS

Time(m)	Vds=0V	Vgs=0V	Ids (μ)		Time(m)	Vds=10V	Vgs=0V	Ids (μ)
	from	to	Avrg			from	to	Avrg
0	-0.3	0.3	0		0	0.6	1	0.8
2	-0.3	0.3	0		2	0.7	1.1	0.9
4	-0.3	0.3	0		4	0.7	1	0.85
6	-0.3	0.4	0.05		6	0.7	1.1	0.9
8	-0.3	0.4	0.05		8	0.6	1	0.8
10	-0.3	0.4	0.05		10	0.7	1.1	0.9
12	-0.3	0.3	0		12	0.7	1	0.85
14	-0.3	0.4	0.05		14	0.7	1.1	0.9
16	-0.3	0.4	0.05		16	0.6	1	0.8
18	-0.3	0.3	0		18	0.6	0.9	0.75
20	-0.3	0.4	0.05		20	0.6	1	0.8
22	-0.3	0.3	0		22	0.7	1.1	0.9
24	-0.3	0.4	0.05		24	0.6	1	0.8
26	-0.3	0.4	0.05		26	0.8	1.1	0.95
28	-0.3	0.3	0		28	0.6	1	0.8
30	-0.3	0.3	0		30	0.7	1.1	0.9

C.

	Vds=10V	Vgs=10V	Ids (μ)		Time (m)	Vds=20V	Vgs=10V	Ids (μ)
Time(m)	from	to	Avrg			from	to	Avrg
0	1.2	1.5	1.35		0	2.8	3	2.9
7.4	1.3	1.5	1.4		2	2.8	3.1	2.95
13.3	1.3	1.6	1.45		4	2.9	3.2	3.05
15.58	1.4	1.6	1.5		6	2.9	3.3	3.1
20.01	1.3	1.6	1.45		8	2.9	3.3	3.1
25.07	1.3	1.6	1.45		10	2.9	3.3	3.1
30.21	1.3	1.5	1.4		12	3	3.4	3.2
34.22	1.3	1.5	1.4		14	2.9	3.3	3.1
35.38	1.2	1.5	1.35		16	2.9	3.3	3.1
39.1	1.3	1.4	1.35		18	2.9	3.3	3.1
43	1.2	1.5	1.35		20	3	3.3	3.15
45.02	1.2	1.5	1.35		22	2.9	3.3	3.1
47.26	1.2	1.5	1.35		24	3	3.3	3.15
49	1.2	1.5	1.35		26	2.9	3.3	3.1
50	1.3	1.4	1.35		28	3	3.3	3.15
					30	3	3.3	3.15

D.

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