Multilevel inverters for renewable energy systems

Pride Chiwaridzo
CHWPRI001

20 February 2018

Dissertation submitted for the degree of
Master of Science in Electrical Engineering

Faculty of Engineering and the Built Environment
Department of Electrical Engineering
University of Cape Town

Key Words: Harmonics, machine learning, multilevel inverter, PWM.

Declaration

Declaration

1. I know that plagiarism is wrong. Plagiarism is to use another's work and pretend that it is one's own.
2. I have used the IEEE convention for citation and referencing. Each contribution to, and quotation in, this MSc dissertation from the work(s) of other people, has been attributed and has been cited and referenced.
3. This MSc project report is my own work.
4. I have not allowed, and will not allow, anyone to copy my work with the intention of passing it off as their own work or part thereof

This thesis/dissertation has been submitted to the Turnitin module and I confirm that my supervisor has seen my report and any concerns revealed by such have been resolved with my supervisor

Name: **Pride Chiwaridzo**

Signature: Signed by candidate

Date: 22 February 2018

i

Acknowledgements

I would like to thank my former supervisor Dr. M. Hanif who was instrumental in guiding the ideas behind this thesis. I am also very grateful to my current supervisor Prof. P. Barendse who took over from where Dr. Hanif left.

This thesis would not have been possible without help from technical workshop staff such as Mr Chris Wozniak and Mr Philip Titus who always encouraged me to keep on experimenting especially when hardware was not working as expected.

A big thank you to my office colleagues for your company and support during this time.

To my lovely wife Penelope, my daughter Zoey and my son Ezekiel, thank you for standing by me even if it meant sacrificing some of our family time.

And to God, who made it all possible, may your praise forever be on my lips.

Abstract

Voltage source inverters have become widely used in the last decade primarily due to the fact that the dangers and limitations of relying on fossil fuel based power generation have been seen and the long term effects felt especially with regards to climate change. Policies and targets have been implemented such as from the United Nations climate change conference (COPxx) concerning human activities that contribute to global warming from individual countries. The most effective way of reducing these greenhouse gases is to turn to renewable energy sources such as the solar, wind etc instead of coal. Converters play the crucial role of converting the renewable source dc power to ac single phase or multiphase. The advancement in research in renewable energy sources and energy storage has made it possible to do things more efficiently than ever before. Regular or 2 level inverters are adequate for low power low voltage applications but have drawbacks when being used in high power high voltage applications as switching components have to be rated upwards and also switch between very high potential differences. To lessen the constraints on the switching components and to reduce the filtering requirements, multilevel inverters (MLI's) are preferred over two level voltage source inverters (VSI's). This thesis discusses the implementation of various types of MLI's and compares four different pulse width modulation (pwm) techniques that are often used in MLI under consideration: three, five, seven and nine level inverters. Harmonic content of the output voltage is recorded across a range of modulation indices for each of the three popular topologies in literature. Output from the inverter is filtered using an L only and an LC filter whose design techniques are presented. A generalized prediction algorithm using machine learning techniques to give the value of the expected THD as the modulation index is varied for a specific topology and PWM switching method is proposed in this study. Simulation and experimental results are produced in five level form to verify and validate the proposed algorithm.

Table of Contents

List of Figures

List of Tables

1. Introduction

1.1 Background to the study

Voltage Source Inverters (VSI) are now widely used to generate alternating output voltage when only a DC power source is available. Multilevel inverters have developed since their debut in the 1970s. Switches have also developed from diodes and thyristors in the early days of the invertor followed by MOSFETS and IGBTs which are still improving to this very day. There are basically three types of multilevel inverters (MLI's), namely Diode Clamped (also called the Neural Point Clamped, NPC), Flying Capacitor (also called the Capacitor Clamped, CC) and Cascaded H-Bridge that are extensively employed in power applications. Different types of carrier based pulse width modulation (PWM) techniques are employed on each of the three topologies mentioned above.

It is generally agreed that phase disposition PWM produces outputs with the least harmonics. This is verified both in simulation and hardware. The various switching techniques mentioned before are employed across varied modulation indices to see their effect on the THD and individual harmonics of the output voltage and current. In the past few years various ways have been suggested to predict the harmonics in the output waveforms. Among these are methods that use neural networks to predict harmonics in a particular level. Most of these methods use more than 50% of the data available to train the network but this research shows that even less data can be used to train a network that can predict harmonics correctly.

Output voltage and current are sent to a filtering device whose design is briefly discussed.

1.2 Objectives of this study

1.2.1 Problems to be investigated

These questions are going to be answered in this research: How are Multilevel inverters different from regular or two level inverters? Is there significant reduction of harmonics as the levels are increased and how do they change with each level of MLI? How are the MLIs implemented both in software and hardware? How are the PWM switching schemes for the regular inverters modified to suit MLIs? How does one filter the output voltage or current from these MLIs? Is the design of the filter different from the two level inverters? Can harmonics be predicted and what about the THD?

1.2.2 Purpose of the study

This research gives an easy to understand review on the diode clamped, capacitor clamped and cascaded h-bridge multilevel inverter topologies. It details how the different topologies are built using circuit illustrations, how the PWM switching is achieved (PD-PWM, POD-PWM, APOD-PWM, PS-PWM and VSF-PWM) for regular inverters and develops this so as to be applicable for MLIs. The control of each MOSFET switching gate is examined and the output filter design (L only filter and LC filter) is discussed both in software and practically in hardware. Harmonics from these inverters are studied and a better way of predicting them is suggested using neural networks. The suggested machine learning method uses about 20% less training data than the methods in literature as will be discussed in literature review.

1.3 Scope and Limitations

This thesis reviews the available multilevel inverter topologies. The diode clamped, capacitor clamped and cascaded h-bridge inverters are discussed in detail. Hybrids or modifications of the basic topologies are also discussed. The basic topologies are all implemented in software for the 3, 5, 7 and 9 level MLI and results compared briefly before only the cascaded h-bridge starts being the only one

being considered. The modulation index is varied from the lowest applicable to a maximum of one (linear region). In terms of hardware verification, only the 5 level cascaded h bridge is looked at because of time and resources. An L only and LC filter are designed and used with the inductors and capacitors bought over the shelf and not specially made for this project. Hardware will not be implemented on the other two topologies and the three, 7 and 9 levels will not be verified by hardware.

1.4 Plan of development

Chapter two is the Literature review. It looks into what has been done already in this field and what will be contributed to by this work. Chapter three introduces the topic of voltage source inverters in more detail than the small introduction section above. The basic topologies of MLIs are looked at, the PWM schemes talked about and assignment of switching patterns briefly discussed but not in full. Chapter four improves the discussion on the assignment of switching patterns from the previous chapter and illustrates how this is done by implementing them in MATLAB-Simulink. This chapter also gives motivation for the components used such as switches, switching scheme, and MLI topology. Chapter 5 implements the software simulations in real voltage source inverter hardware. The design of the output filter is discussed here before finishing the chapter with the prediction of harmonics in MLIs. All relevant results from both software and hardware are given in chapter 6. Chapter 7 continues the discussion on some of the significance of the results from chapter 6. Conclusions and recommendations follow in chapter 8 and 9. The list of references is made in chapter 10. Chapter 11 is the appendix section which includes some of the figures which were put there to avoid a lengthy main section.

2. Literature review

Different methods have been proposed and implemented to predict harmonics and THD for either voltage or current outputs. The first method involves the separation of the output fundamental components and high frequency components in the frequency domain [8] [9] [11]. A generalization is made in [8] after assuming there are no distortions on the input AC side and understudying a special case where the non-fundamental voltage components have a phase angle and magnitude that varies linearly with the fundamental component. Harmonics generated by nearby loads are also accounted for but the assumptions and generalization only work for systems with a maximum voltage THD of 12%. A slightly different approach in [9] builds a THD model based on current ripples. The THD is split into two groups which are below and above the 50^{th} harmonic component. The paper suggests excluding the electromagnetic interferences and so switching behaviors and their harmonics are ignored. Assumptions of ideal switches and no load operations are made when producing the harmonic distortion model in [11]. Also, in [11] a transfer function using z-transform is generated that relates the output current to the input current.

The Harmonic Balance method, which was previously limited to nonlinear microwave circuits and electromagnetic field analysis, was used in [31] to predict harmonics in power systems. It models different subsystems at circuit level and also takes into account interferences induced during operation. A similar approach is also done in [28] which assume that the non-linear load is supplied from a network which has series impedances and disturbances from neighbor loads. It then predicts multiple outputs at a specified measuring point, which are the real and imaginary components of the fundamental and harmonic currents.

Several other publications such as [2], [5], [7] and [43] have used neural networks to provide a suitable approximation to harmonics by taking measurements at the filter connection point. Among them, [5] takes in both the input voltage and current to train the prediction algorithm using 75% of the data and validates it using the remaining 25%. The paper then compares the accuracy of different data resolutions used when collecting data and training the algorithm. A slightly different approach is taken in [7] where a two layer feed-forward network is used in the estimation of the stator voltage THD. A good proportion of the data is used in training the network (70%) but the paper only focused on distortions up to the 30^{th} harmonic. A single layer network is used in [2] in which distortions up to the 39^{th} harmonic component are used when training the network but only validated for up to the 23^{rd} harmonic. The paper however does not reveal how much of the data was used to train the network. Half of the data collected was used to train the network in [43]. Two different machine learning techniques were applied and it was concluded that both methods could not predict THD values above 12%.

This proposal builds upon the foundations laid up in the above studies where a single layer feed-forward network is used to train the network. A sigmoid function, being global, is used as the basis or activating function. Only 20% of the data was used for training the network and predictions of both the low frequency harmonics and high frequency harmonics (above the switching frequency) were made successfully. Popular multicarrier PWM techniques were used across the three multilevel topologies and outputs compared for various levels of the inverter. Of the three

topologies, the CHB-MLI topology is chosen for hardware validation as a five level inverter and the results are compared against the output from the machine learning algorithm.

3. Voltage Source Inverters

3.1 Two level Inverters

Inverters are primarily used to convert a dc voltage to an ac output waveform. Where the output waveform is an alternating voltage, the inverters are called voltage source inverters (VSIs). These can also be used in the production of a multiphase voltage when only a single phase supply is available. They are used in a number of areas including uninterruptible power supplies (UPSs), flexible AC transmission systems (FACTSs), static var compensators, adjustable speed drives (ASDs), hybrid and electric vehicles amongst other things. If the ac output is a current waveform, then the inverter is referred to as a current source inverter (CSI).
Power electronic switches are used in the construction of these inverters and as such the output waveform features fast transitions rather than smooth ones. This makes the output waveform appear non sinusoidal even though its fundamental is. The behaviour of the output waveform is governed by the modulation technique which monitors the amount of time and sequence used to do the switching. There are different modulation techniques such as the carrier based sine pulse width method and the space vector method. The fundamental building block of VSIs in general is shown in Fig. 3-1.

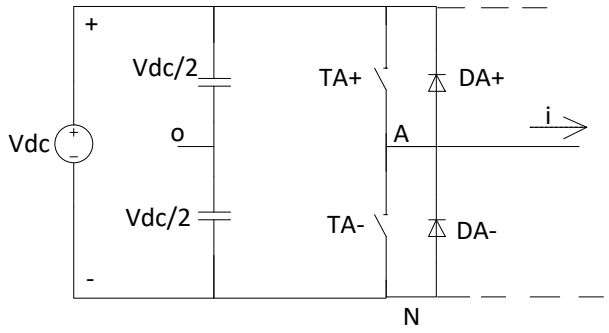


Fig. 3-1: One leg of a switched mode inverter.

The above figure shows a single leg (or phase) from a switched mode inverter. The switches T_{A+} and T_{A-} operate complementarily. This avoids short circuit conditions. DA+ and DA- are freewheeling diodes. It is desired that the output of the inverter be sinusoidal with controllable magnitude and frequency. The output (drawn from point A) with respect to the negative of the DC bus (N above) is called the terminal voltage. The output goes high when T_{A+} is ON and the reverse is true.
Cascading two such legs produces a full bridge as shown in circuit below.

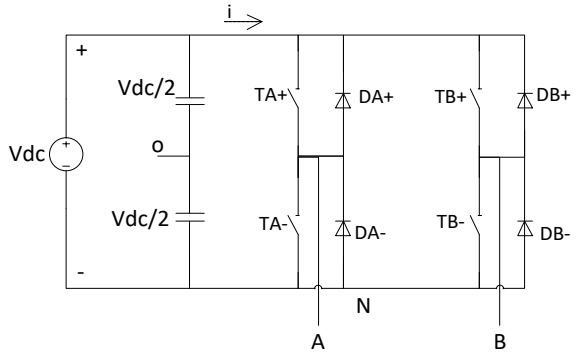


Fig. 3-2: Single phase full bridge VSI

The switch combinations used to control the circuit in Fig. 3-2. are described in the table below. The load is connected between the two output terminals A and B.

Table 3-1: Switch sates for a full bridge single phase VSI

state	**switch**				**V_{AN}**	**V_{BN}**	**V_{out}**
	TA+	TA-	TB+	TB-			
1	ON	off	off	ON	V_{dc}	0	V_{dc}
2	off	ON	ON	off	0	V_{dc}	$-V_{dc}$
3	ON	off	ON	off	V_{dc}	V_{dc}	0
4	off	ON	off	ON	0	0	0

If N (the negative of the dc link) is taken as the reference, terminal A swings to V_{dc} with respect to N when switch TA+ is switched ON in Table 3-1 above. V_{out} is the resultant from subtracting the output at B from that at A. When three single legs are put in parallel and each inverter's output is displaced by 120° (of the fundamental frequency), a three phase 2 level inverter is formed. A schematic is shown below:

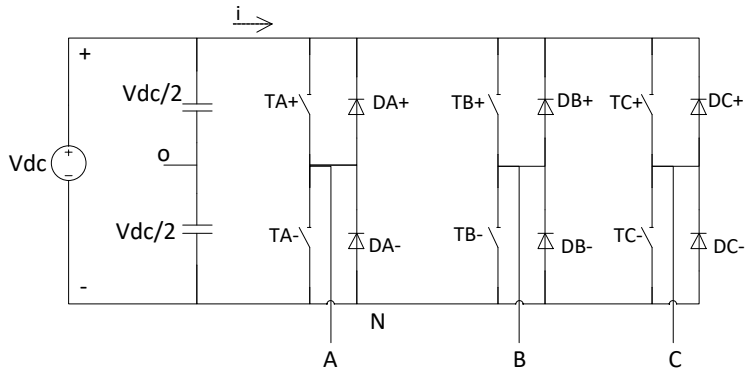


Fig. 3-3: three phase inverter circuit

In Fig. 3-3, outputs A, B, and C are the three phase outputs from the 2 level VSI. The different inverter topologies can be controlled using various schemes. If the above three phase two level inverter has its switching devices controlled by Sinusoidal Pulse Width Modulation, the resultant voltages will take the shapes illustrated in below.

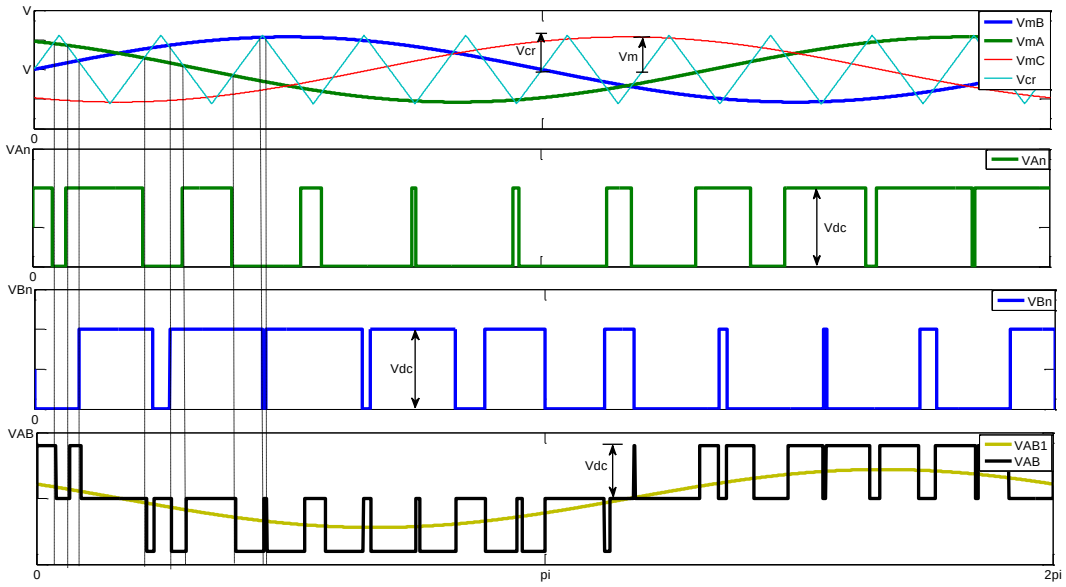


Fig. 3-4: PWM signal generation and different outputs from the inverter

Fig. 3-4 above shows sinusoidal PWM waveforms for a 3 phase 2 level inverter. Sinusoids V_{mA}, V_{mB} and V_{mC} are the modulating signals for leg A, leg B and leg C respectively being compared to the carrier signal, V_{cr} (a triangle in this case). It can be seen that when V_{mA} is greater than V_{cr}, a 'high' is sent from the logic comparator to the upper switch T_{A+} which in turn goes ON. This will make the output V_{AN} swing to V_{dc} with respect to the negative terminal N. Alternatively, when Vma is less than Vcr, the switch T_{A+} is turned OFF and the complementary switch T_{A-} is switched ON. This makes the output V_{AN} go to zero.

The same logic applies to the other legs. Each leg's output with respect to N is the phase voltage and the line voltage is the difference of two phase voltages as shown by V_{AB}, which is the difference between V_A and V_B. Although V_{AB} does not look sinusoidal, its fundamental, V_{AB1}, is sinusoidal. The phase voltage has 2 levels and the line voltage has 3 levels as expected.

3.1.1 Modulation techniques

There are several modulation techniques which can be broadly divided into two categories; fundamental switching frequency and high switching frequency. including the sinusoidal PWM method used above. This special case of carrier based PWM method occurs when the modulating signal is a sine wave (hence the name sinusoidal PWM) and the carrier waveform is a triangular wave. For a modulating wave V_m, whose magnitude is v and frequency f_m, the modulation index m_a is defined as

$$m_a = \frac{v}{V_{tri}} \tag{3.1}$$

where v_{tri} is the amplitude of the carrier wave. The normalised carrier frequency m_f (also called the frequency modulation ratio) is defined as

$$m_f = \frac{f_{tri}}{f_m} \tag{3.2}$$

where f_{tri} is the frequency of the carrier waveform. Analysis of the half bridge circuit (one leg) it can be seen that the output v_{out} satisfies

$$v_{out} = \frac{V_{dc}}{2} m_a \tag{3.3}$$

in the linear region ($m_a \leq 1$). This makes sense as the output can swing to a maximum of half the supply voltage (positive or negative). The output line voltage's spectrum is shown below.

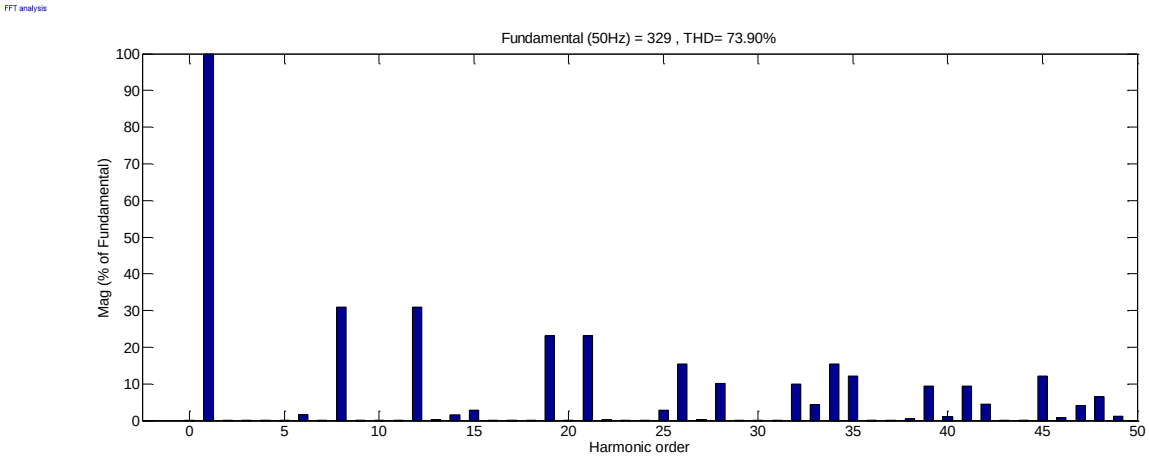


Fig. 3-5: output voltage spectrum

The first fifty harmonics in the output voltage V_{AB} of Fig. 3-4 are shown in Fig. 3-5 above. Harmonics can be seen at locations

$$h = lm_f \pm k \quad l = 1,2,3,\ldots \tag{3.4}$$

where h is the harmonic location, k=2,4,6,… for l =1,3,5,…; and k=1,3,5,… for l=2,4,6,… For a switching frequency of 500Hz (illustrative purpose only), the biggest distortions are close to the switching frequency (h=10) and multiples thereof. Therefore, harmonics appear as sidebands with the centre being the switching frequency and its multiples at m_f, $2m_f$, $3m_f$, and so on. This is true for modulation indices in the linear range.

Other modulation techniques which will not be implemented in this paper are the square wave modulation, the selective harmonic elimination PWM, sub harmonic PWM and switching frequency optimal PWM. The square wave modulated inverter has an output ac voltage whose magnitude is controlled by varying the input dc voltage thus the inverter only controls the output frequency. In other words, for square wave PWM inverters, v_{out} has a constant relationship to v_{dc} unlike in equation (3.3). Selective harmonic elimination works by injecting negative harmonic components into the modulating signal thereby removing the selected harmonics in the output which may have been generated by the original pure sinusoidal reference. Sub harmonic PWM uses m-1 carriers for an m level inverter. These identical carriers of magnitude v_{tri} and frequency f_{tri} are arranged such that the bands they occupy are contiguous. The reference or modulating signal is then continuously compared to these carriers, output going high whenever the reference is greater than the carrier. Lastly, switching frequency optimal PWM is similar to sub harmonic PWM except that the third harmonic (or zero sequence) is added to each of the carriers. A different modified reference is used unlike in the other modulation techniques. This modified reference is got from subtracting an offset voltage (which is the instantaneous average of the three reference waveforms in a three phase system) from the original reference voltage for that phase.

3.1.2 Unipolar and Bipolar PWM

Bipolar PWM switching involves simultaneously switching the two switch pairs in Table 3-1. Therefore, TA+ is directly connected with TB- while TB+ is directly connected to TA- and thus the four switches are controlled by two signals instead of four. Since the signals powering one pair complements the other, the output from a circuit implementing bipolar PWM has leg A output being the negative of leg B output as illustrated in Fig. 3-6 below.

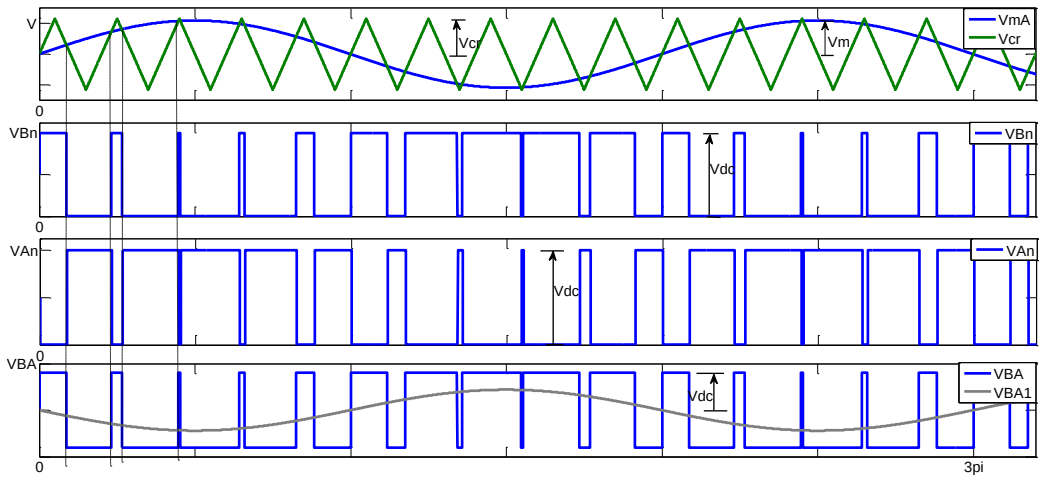


Fig. 3-6: Bipolar switching

Output V_{BA} is obtained from subtracting V_{An} from V_{Bn} in Fig. 3-6 above. Thus bipolar switching utilizes states 1 and 2 in Table 3-1.

Unipolar switching however can utilize all of the switching states in Table 3-1 to make the output voltage. This means that the output voltage synthesised this way can take values of V_{dc}, 0, and $-V_{dc}$ at any instant in time. A carrier based technique can be used to generate the pulses such as illustrated in Fig. 3-4 and the output can be seen to occupy the three voltage states mentioned ealier.

3.2 Multilevel inverters (MLIs)

Multilevel inverters have become widely used in high power inverter applications as well as in the renewable energy sector. Among the converters, the DC/AC converters play a different role to their DC/DC counterparts. DC/DC converters are used to generate a high output DC voltage from a DC source where a DC/DC boost converter cannot achieve the desired voltage level. They also can act as the link between primary DC low voltage sources and high voltage multilevel inverters (DC/AC converters). These sources could be batteries, fuel cells, photovoltaic solar panels, wind turbines or superconducting magnetic energy storages. When interfaced with multilevel inverters, the DC/DC converter balances the input voltage of the inverter thereby removing the need for complex control for the multilevel inverter's input voltage.

Multilevel inverters have an output AC voltage unlike their DC counterparts. They are useful in many applications where AC voltage is required especially from a DC source as explained above. Renewable energy and DC supplies can be interfaced to the grid using these inverters and their output is closer to a perfect sinusoidal waveform than the two level inverters. Other applications include those listed under the two level inverters except with the difference being the power ratings of the applications. There are three basic topologies used in multilevel inverters. These are the Diode Clamped (DC-MLI), Flying Capacitor (FC-MLI) and Cascaded H-Bridge (CHB-MLI) multilevel inverters. Other forms of inverters can be produced as hybrids or derivatives of these three basic topologies.

The regular PWM methods for the two level inverters can be extended to multilevel inverters. With multiple carriers, (3.1) becomes

$$m_a = \frac{\mathrm{v}}{(m-1)V_{tri}} \tag{3.5}$$

where the variables v, v_{tri} and m_a retain their meanings as earlier and m is the number of levels.

3.2.1 Diode Clamped Multilevel Inverter (DC-MLI)

This inverter uses clamping diodes and DC capacitors to produce multilevel/multistep ac voltage. In two level form, this inverter is called the Neutral Point Clamped (NPC) inverter. Diode clamped inverters have the basic configuration illustrated below.

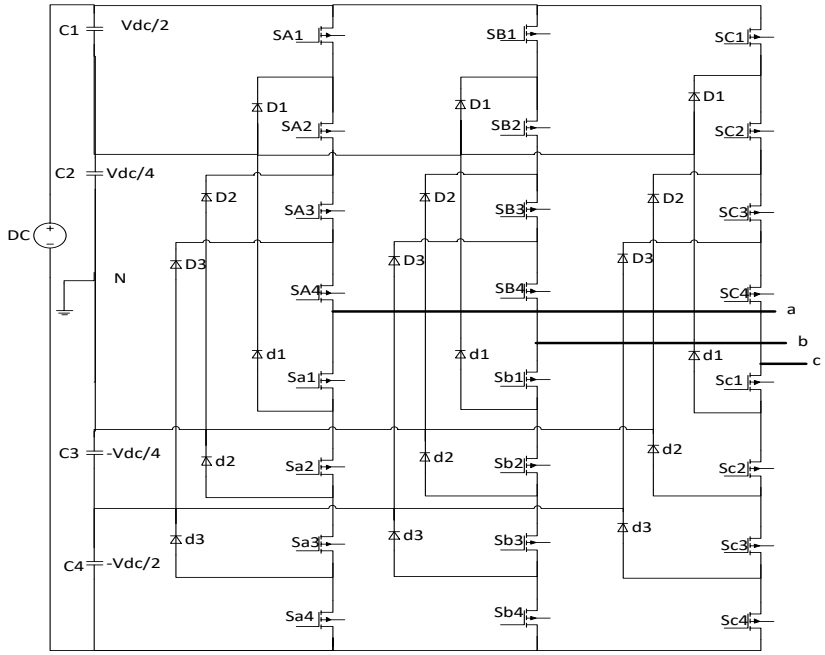


Fig. 3-7:three phase DC-MLI

The midpoint of the capacitors in the middle in Fig. 3-7 (C2 and C3) determines the neutral point and the output voltages can be referenced to this point when available. Each of the 3 phase outputs share a common DC bus voltage. This voltage is divided into m levels (or steps), each capacitor having a voltage of $\frac{Vdc}{(m-1)}$ across it. However, it is noted that some scholars prefer to assign each voltage level a value of V_{dc} and also reference the output to the negative rail which means the actual DC bus voltage will be a value of (m-1)V_{dc}, where V_{dc} is the voltage across one capacitor, not across the DC link. The subtle difference is illustrated in Fig. 3-8 below.

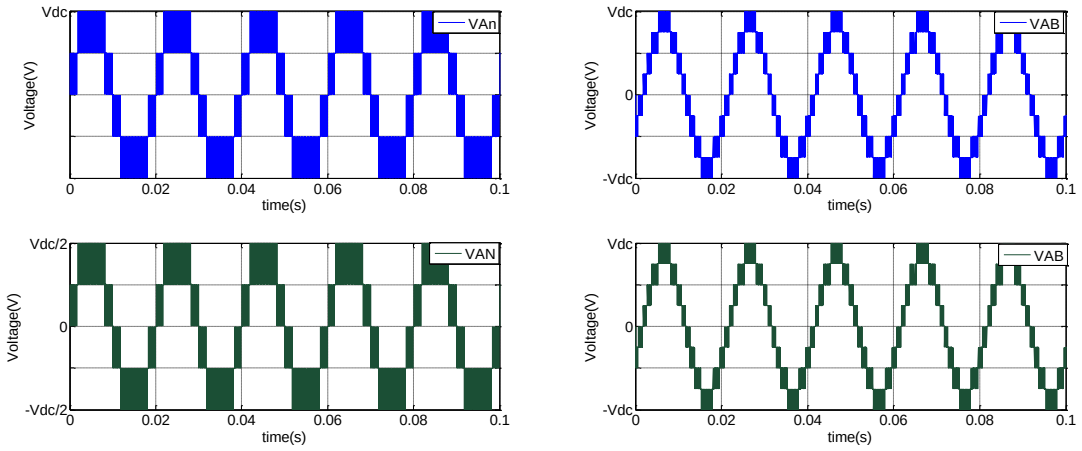


Fig. 3-8: Output phase and line voltage waveforms when different references are used

When the midpoint N is used in Fig. 3-8, the output with respect to this point is V_{AN}. If the negative rail was used instead of the midpoint, then the output will be as shown by the plot V_{An} showing s translation relationship between the two plots. However, the reference point does not affect the line to line output as indicated by the identical plots of V_{AB}.
As with 2 level inverters, the switches making up each leg (or phase) are complementary. In Fig. 3-7, 4 switches are ON at any given time. By considering different m level values of the inverter, it can be seen that the circuit requires (m-1) capacitors at the DC side.
The number of freewheeling (antiparallel) diodes per phase is 2(m-1) and this will be the same as the number of switching devices needed.
Table 3-2 below shows the switching states and the corresponding voltage levels for a 5 level DC-MLI when the midpoint N is used as the reference.

Table 3-2: switching states and their voltage levels for a five level DC-MLI

Voltage V_{aN}	**Switching States**							
	S_{A1}	**S_{A2}**	**S_{A3}**	**S_{A4}**	**S_{a1}**	**S_{a2}**	**S_{a3}**	**S_{a4}**
$V_4=V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3=V_{dc}/4$	0	1	1	1	1	0	0	0
$V_2=0$	0	0	1	1	1	1	0	0
$V_1=-V_{dc}/4$	0	0	0	1	1	1	1	0
$V_0=-V_{dc}/2$	0	0	0	0	1	1	1	1

It can be seen that a top switch cannot be ON at the same time as a corresponding bottom switch in Table 3-2. It is also evident from the table that some switches will be ON for longer than others, for example S_{A4} and S_{a1} will be ON for twice as long as S_{A2} and S_{a3}. Thus the current rating of the inner switches will be higher than that for the outer switches and as a result, the clamping diodes require different current ratings for the appropriate amount of current they will be blocking. A total of (m-1)(m-2) clamping diodes per phase are required if it is assumed that every clamping diode has a blocking voltage rating which is the same as the switching device. This is normally the case in hardware implementation as it will be easier to replace diodes or any other component if the value is the same throughout. In this case, the DC-MLI's leg will take the configuration shown below:

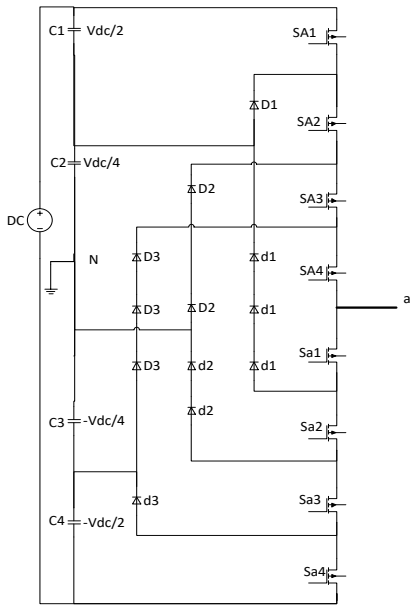


Fig. 3-9: DC-MLI with identical clamping diodes

From Fig. 3-9 above, a total of (m-1)(m-2) which equals 12 clamping diodes for the 5 level MLI are required. As m is increased, the number of clamping diodes required rises even quicker (following a quadratic rule) and the design becomes bulky to implement. To illustrate how the number of clamping diodes is achieved, let us say an output voltage of V_{dc} is required between the output terminal and the negative rail. From Table 3-2, all switches S_{A1} to S_{A4} needs to be ON whilst all the complementary switches S_{a1} to S_{a4} are OFF. Each diode has a reverse voltage blocking of $V_{dc}/(m-1)$. Now the voltage between C1 and C2 is $V_{dc}/4$, therefore diode D1 has to block $V_{dc}/4$, diode D2 block a voltage of $2V_{dc}/4$, and diode D3 block $3V_{dc}/4$. Therefore D1 needs 1 diode rated $V_{dc}/4$, D2 requires 2 similar rated diodes and D3 requiring 3 diodes. The same logic is applied when a zero output voltage is required and instead all the bottom switches are ON.

Advantages:

An advantage of DC-MLIs is that since all of the phases share a common dc bus, the capacitor requirements of the inverter are easy to meet. This enables the implementation of back-to-back converter topology for use in applications such as in adjustable speed drives. In back-to-back topology, two converters are connected to one common DC link. One converter works as a rectifier, and the other works as an inverter thus allowing for power transfer in both directions. The capacitors of a DC-MLI can be pre-charged as a group. Efficiency is high as the devices can be switched at the fundamental frequency. If the level is high enough, harmonic content will be low and there will not be a need for a filter. It is possible to control the reactive power flow.

Disadvantages:

A disadvantage is that real power flow is difficult to achieve as it is dependent on the DC levels in the capacitors being maintained [41]. Without precise control and monitoring, current may have a non-zero net flow through the cells in one period of the output voltage since the capacitor plates may become unbalanced during operation. Another disadvantage is that as the level (m) of the

inverter increases, so does the number of clamping diodes required by the topology which makes implementation bulky.

3.2.2 Flying Capacitor Multilevel Inverter (FC-MLI)

FC-MLIs were introduced more than two decades ago as an alternative to DC-MLIs. There are similarities in the main structure with that of DC-MLIs but instead of using clamping diodes, FC-MLI uses DC capacitors in a ladder form. Their name is such because the capacitors' voltage 'float' with respect to the earth's potential. Fig. 3-10 below shows the schematic of a five level FC-MLI.

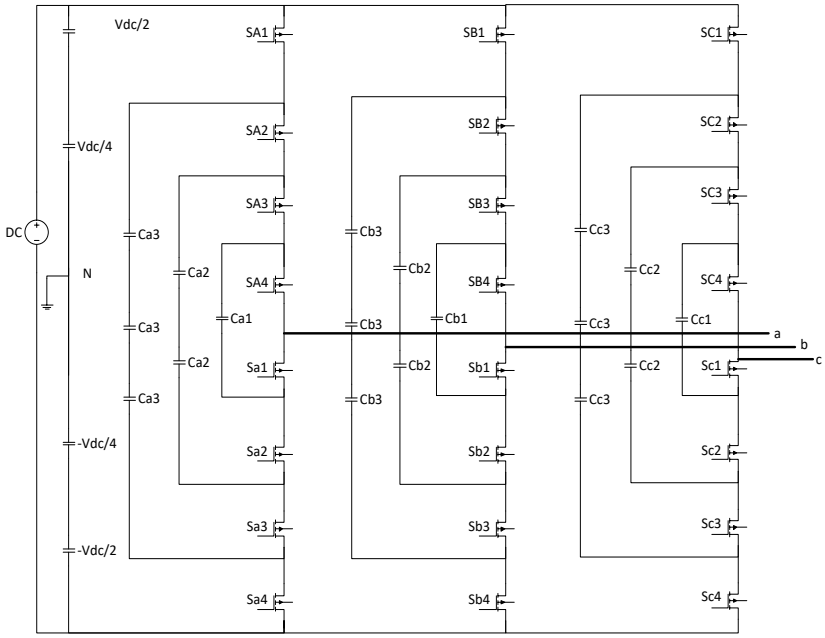


Fig. 3-10: Three phase 5 level FC-MLI topology.

C_{a1}, C_{a2}, and C_{a3} are auxiliary capacitors in Fig. 3-10 which are pre-charged to specific levels; $V_{dc}/4$, $V_{dc}/2$ and $3V_{dc}/4$ respectively. The inverter comprises of a DC source, four capacitors for the DC bus (equal to m-1), 8 switches per leg (four sets of two switches complementing each other) and clamping capacitors. The ratios (1:2:3:4) of the clamping capacitors to the DC link are the classical ratios used for the five level MLI and results in an output voltage that has levels equal to the number of switches (half of the leg) plus one. There are ways which have been developed to increase the number of levels just by altering the ratios in the capacitor voltages [23]. The voltage difference between two neighbouring capacitor legs gives the size of the voltage steps at the output side. An advantage of FC-MLI is that it allows for different switching combinations to yield the same voltage level for the inner voltage levels. This is illustrated in Table 3-3 below.

Table 3-3: five level FC-MLI switching states and voltage levels.

Voltage	**Switching State**							
V_{aN}	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 =$	1	1	1	0	1	0	0	0

$V_{dc}/4$	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
$V_2=0$	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$V_1=$ $-V_{dc}/4$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$V_0=$ $-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 3-3 above shows the switching states and the corresponding voltage levels for a 5 level FC-MLI. There are alternative/redundant switching states for voltage levels Vdc/4, 0 and –Vdc/4. This shows the phase redundancies of FC-MLI. The number of DC link capacitors (m-1) required is obviously the same as in DC-MLIs. If the voltage rating of the capacitors is the same as that of the switching devices (just like the diodes may have the same voltage rating as that of the switching devices), then the number of auxiliary capacitors required per phase is (m-1)(m-2)/2; which is six when m is equal to five. Table 3-3 also shows that unlike in DC-MLIs, the FC-MLI does not require that all the switches that are ON (conducting) to be switched ON consecutively. In other words, to get a certain voltage at the output of DC-MLI requires a specific switching pattern as shown by Table 3-2 which is not the case for the FC-MLI in Table 3-3. In fact, S_{A4} and S_{a1} in the above table are divided by what may be thought of as a mirror line whereby the columns at identical places either side of the line are complementary.

Advantages:

Phase redundancies give the advantage that switching combinations can be chosen for best voltage balancing on the capacitors. This is done to ensure that the inner capacitors have net charge and discharge cycles that are equal [41]. Thus with suitable control schemes the power flow can be monitored and controlled (real and reactive). Another advantage is that the charge stored in capacitors ensures that the inverter is resistant to voltage surges or small power outages.

Disadvantages:

As the level of the inverter increases, the many capacitors involved become hard to accurately charge and discharge. Their control becomes complex as tracking or monitoring of each capacitor is needed. Also, the cost of the inverter goes up and so does the physical size of the inverter due to the increase in the number of capacitors. Switching utilization and efficiency are poor.

3.2.3 Cascaded H-Bridge Multilevel Inverter (CHB-MLI)

As the nameplate suggests, this topology is made of series connected H-Bridges that have separate DC sources. The outputs of the H-Bridges are connected in series hence the need to use separate or isolated DC sources. An illustration of this topology is given in Fig. 3-11 below.

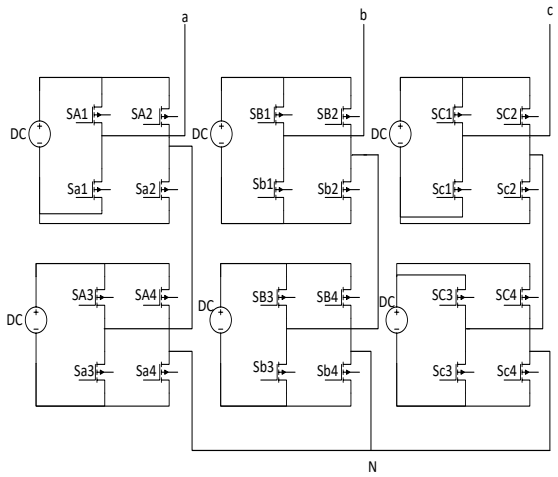


Fig. 3-11: three phase 5 level CHB-MLI topology

In Fig. 3-11 above, S_{A1} acts complementarily with S_{a1}. Should these two be ON simultaneously an obvious short circuit results. Each single phase or leg can generate three different output voltages. The output of the cell at the top in leg A is V_{DC} if S_{A1} and S_{a2} are ON. This swings to the negative rail ($-V_{DC}$) if S_{a1} and S_{A2} are ON. A zero (0V) output results when either S_{A1} and S_{A2} OR S_{a1} and S_{a2} are ON. The actual generation of switching pulses and how they are assigned to each switch will be detailed in the next chapter. In reality, a smoothing capacitor is put across the dc source and a small pull up resistor in series with the capacitor. Hence, each cell will need a separate DC source parallel with a capacitor which will be connected to a series resistor.

When outputs in Fig. 3-11 are all loaded and connected to a star common point the outputs can be derived by use of equations. The star point (load side) will be the zero or reference voltage and the common point of the bottom cells will be the neutral point N which is usually not equal to zero volts as shown in Fig. 3-11. Thus $V_a = V_{aN} - V_{0N}$. The line voltages can also be derived by observation: $V_{ab} = V_{aN} - V_{bN}$. These observed equations can be put in matrix form for all the line voltages and for all the phase voltages.

The phase voltages will be expressed as:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V_{xN}(t) \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} - \begin{bmatrix} V_{0N}(t) \\ V_{0N}(t) \\ V_{0N}(t) \end{bmatrix} \tag{3.6}$$

where the matrix with abc is just replacing the subscript x in $V_{xN}(t)$ with a or b or c depending on phase.

The line voltages can be expressed as:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{xN}(t) \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{3.7}$$

where the matrix with abc is defined as in (3.6) above. With both the phase and the line voltages, the voltage of the star point created by joining the loads can be calculated:

$$V_{0N} = \frac{V_a + V_b + V_c}{3} \tag{3.8}$$

Advantages:

The number of output voltage levels is more for the same number of input dc sources than for other topologies. The individual H-bridge cells can be made and assembled separately allowing for a modular testing. This modularity allows individual cells to be controlled independently of the other cells meaning different controllers can be used on different modules, unlike in the other topologies.

Disadvantages:

This topology requires separate DC sources as inputs to the individual H-bridge cells. This obviously adds unwanted costs. The cost of separate DC sources may be mitigated by using transformers or a single transformer with multiple tap points which are isolated.

3.3 PWM techniques in Multilevel Inverters

PWM techniques employed in regular two level inverters can be modified for applications in multilevel inverters. These are Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM), Selective Harmonic Elimination PWM (SHEPWM) and Delta PWM (DPWM) among others. The techniques can be classified by their switching frequency into two groups; fundamental switching frequency and high switching frequency. Some of the switching methods can fall into either of the groups as it is possible for them to work both at the fundamental frequency and at any selected high frequency. The switching method selected affects the DC bus utilization, which is the ratio of the output voltage compared to the DC bus voltage.
The sine PWM method illustrated in Fig. 3-4 can be expanded and used in multilevel inverters as well. This requires the use of ‘m-1’ carriers for an ‘m’ level inverter instead of just a single carrier in the conventional sine PWM method. This multicarrier PWM technique can also be referred to as Sub-harmonic PWM. Having multiple carriers raises the possibility that they can be arranged in several ways with respect to the modulating waveform. Of these ways, the popularly used methods are considered and compared against each other. One phase shifted method and three level shifted methods are described below for a five level inverter.

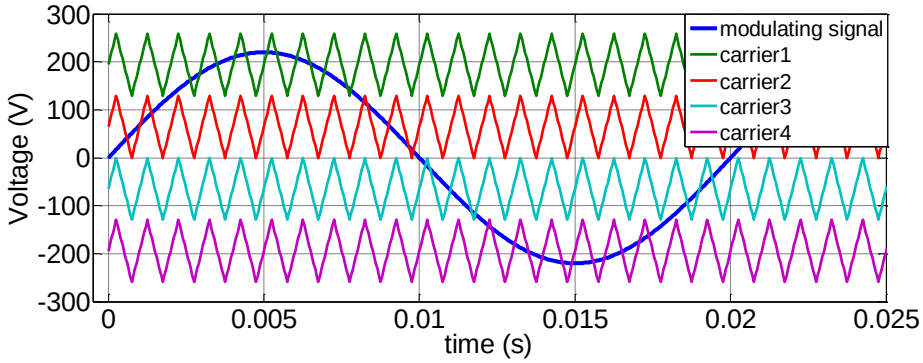


Fig. 3-12: Phase Disposition PWM

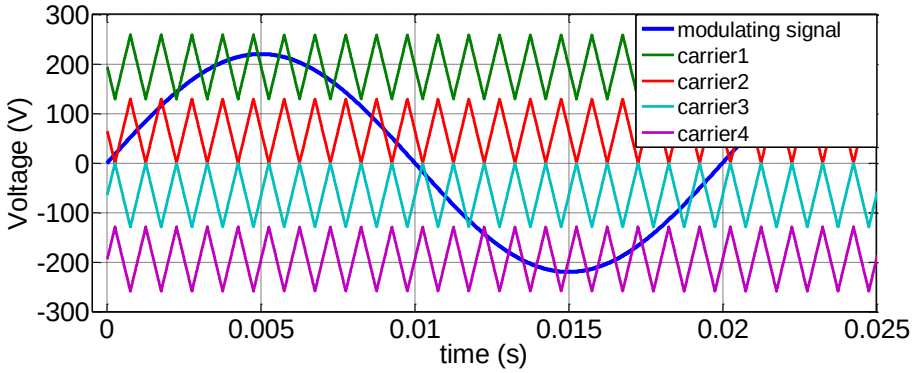


Fig. 3-13: Phase Opposite Disposition PWM

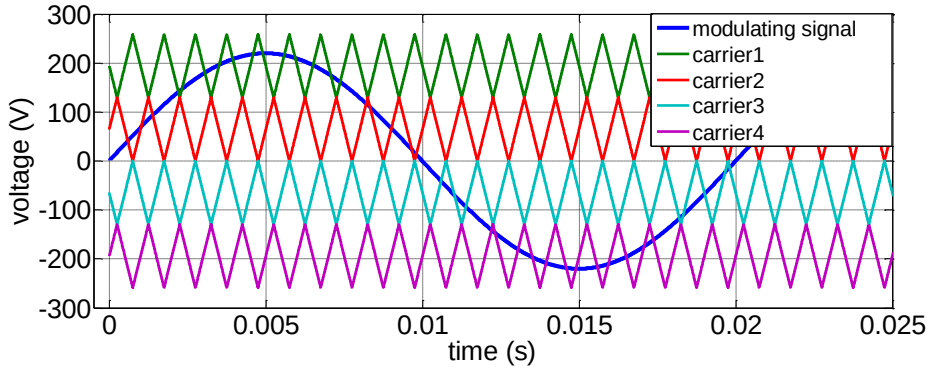


Fig. 3-14: Alternative Phase Opposite Disposition PWM

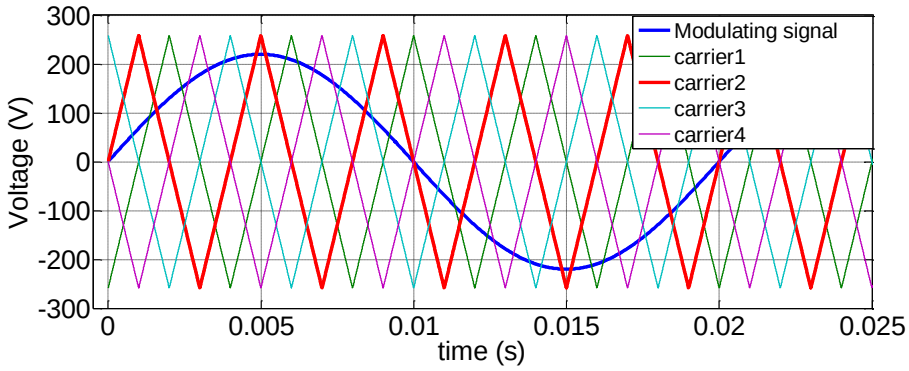


Fig. 3-15: Phase Shifted PWM

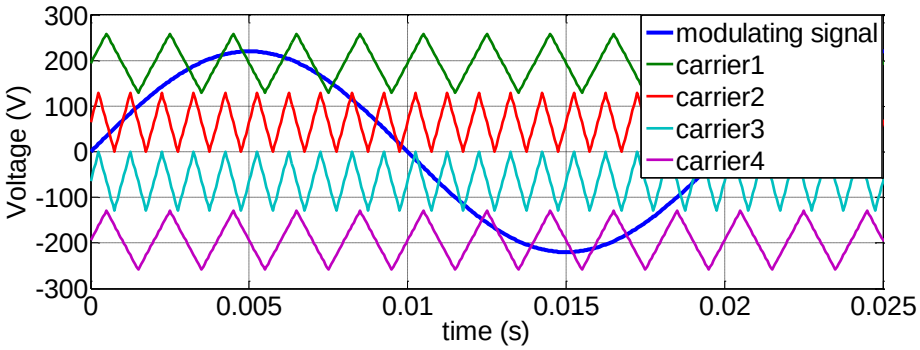


Fig. 3-16: Variable Frequency Pulse Width modulation

Fig. 3-12 shows four carriers evenly distributed about a modulating signal for a five level inverter. The carriers are contiguous and are distributed evenly across the entire amplitude of the sinusoid with the zero crossing separating the top two signals from the bottom two. Phase disposition PWM (PD-PWM) has carriers that start and finish at the same time (carriers are said to be in phase) as shown in Fig. 3-12. When the top two carrier signal are in phase but are 180 degree out of phase with the two bottom carriers, the modulation technique become known as Phase Opposite Disposition PWM (POD-PWM) as illustrated by Fig. 3-13. If otherwise each carrier is 180 degrees out of phase with the next then an Alternative Phase Opposite Disposition PWM (APOD-PWM) is produced as shown in Fig. 3-14. The carriers can also occupy the same bands in amplitude but have different angles therefore start at different points in their cycles as illustrated by Fig. 3-15.

There are other switching schemes which will not be used in this project but will be mentioned for completeness. The Variable Switching Frequency PWM (VSFPWM) in Fig. 3-16 recognises that the top most and bottom most switches are ON most of the time when compared to innermost switches. It therefore switches the outermost switches at a lower frequency than the inner switches all in pairs; topmost paired to bottom most, second from top paired to second from bottom and so on. Another similar switching technique swaps the switching angles after a specific time interval to ensure the switches are ON for similar times hence avoiding overcharging/over-discharging of one capacitor more than the others.

3.4 Other Multilevel Inverter Topologies

There are various derivatives or combinations of the basic multilevel inverter topologies discussed before. These aim to fill in the gap that may be left by using the basic inverter topologies and normally are just tailor made for specific applications. A few are discussed below for the sake of completeness.

3.4.1 Generalised Multilevel Inverter Topology

A generalised multilevel topology (called the P2 topology) proposed by Peng can be used to derive the basic multilevel inverter topologies. This topology has a characteristic that its voltage levels can 'self-balance' in situations of varying load patterns, whether there is active or reactive power flow.

Each capacitor and switch has a voltage Vdc across it which is Vdc/(m-1). This is shown in Fig. 3-17 below.

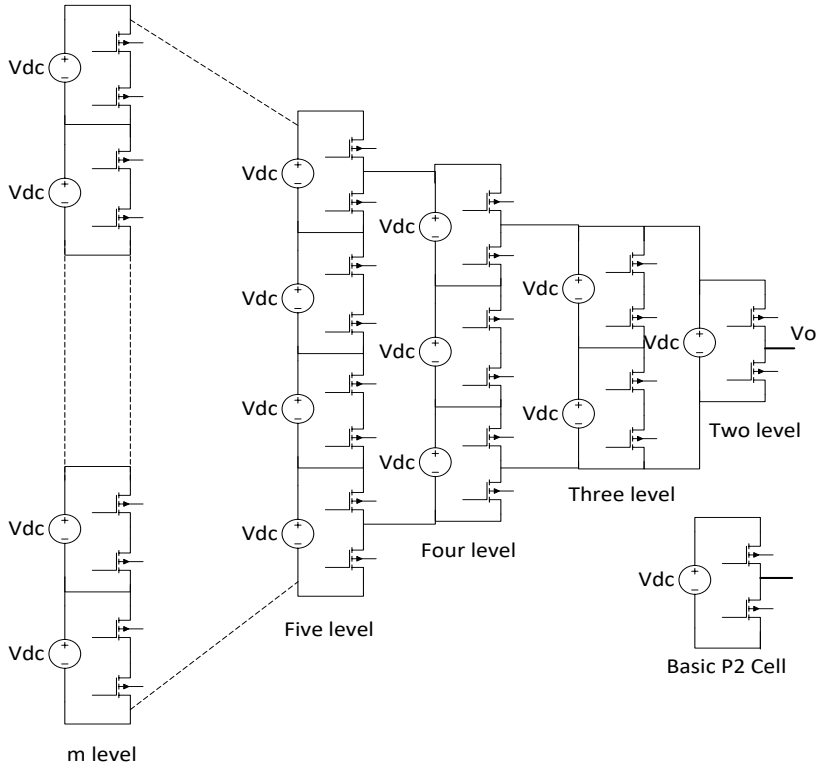


Fig. 3-17: single phase generalized P2 MLI

Fig. 3-17 above shows the P2 MLI structure being composed of individual basic P2 cells. There is therefore a similarity between and the CHB-MLI in the sense of being modular and being composed of basic cells.

3.4.2 Mixed-level hybrid MLI

Multiple DC sources may be required in high voltage high power applications and the cost of separate sources may inhibit the application of certain topologies. To reduce the number of sources, several ways exists that can be used among them the use of DC-MLI or CC-MLI as units or basic cells to a CHB-MLI. This is illustrated below.

It can be seen in Fig 3-18 that the resultant hybrid nine level cascaded MLI is composed of 3 level DC-MLI as the basic cells. A ‘pure’ 9 level CHB-MLI would require 4 separate DC sources to produce the same single phase output. This means that 12 separate DC sources would be required for a three phase MLI, which may be too expensive.

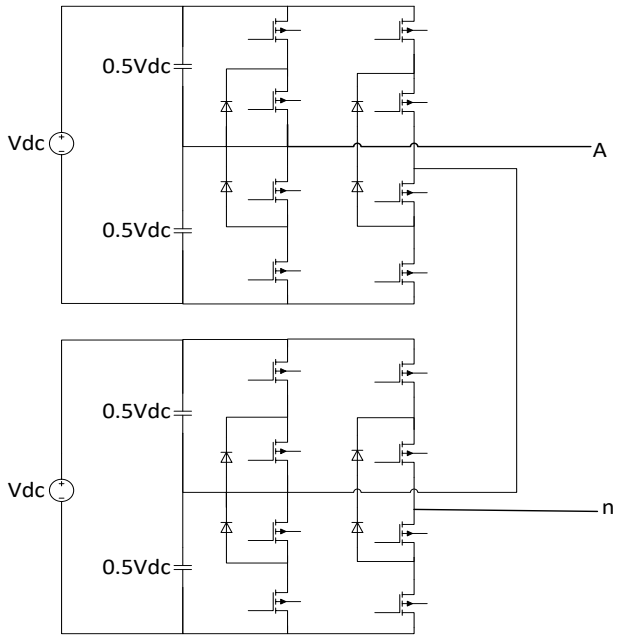


Fig 3-18: Mixed-level hybrid MLI

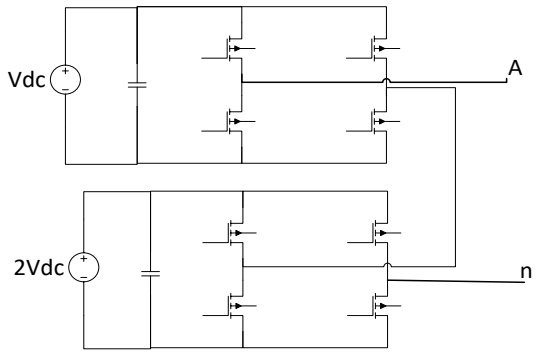


Fig 3-19: Mixed-level hybrid MLI with unequal sources

In the above mixed-level hybrid MLI, the number of DC sources required per phase has been reduced by half. The number of levels which can be achieved from a symmetric CHB-MLI is

$$m = 2n + 1 \tag{3.9}$$

where m is the number of levels and n the number of dc sources.
On the other hand, in asymmetric CHB-MLI more output levels can be achieved for the same number of dc sources as with symmetric CHB-MLI. Where the DC sources are said to be binary (taking values of multiples of two only) the number of levels expected is:

$$m = 2^{n+1} - 1 \qquad \{DC\ source\ voltage = u, 2u, 4u, \dots, 2^{n-1}u \tag{3.10}$$

where m and n are defined as in 3.9.

Should the sources be ternary (that is dc source values being multiples of three) then the number of levels becomes:

$$m = 3^n \qquad \{DC\ source\ voltage = u, 3u, 9u, \dots, 3^{n-1}u \tag{3.11}$$

where m and n are defined as in 3.9.
So for the example in Fig 3-18, it can be deduced from 3.9 to 3.11 that 2 voltage sources on a single phase will yield a 5 level CHB-MLI if the sources are equal in voltage. Should the sources not be equal and in such a way that one's voltage is twice the voltage of the other then a 7 level CHB-MLI is realised as in Fig 3-19. For dc sources where one's voltage is three times the other then a nine level MLI is realised.

4. Software Simulations

There are various ways to simulate voltage source inverters. Simulation in software allows designers to test if their suggested method or idea works before implementing it on a prototype. This may save time and money and as such it is important that thorough experimenting and testing is done in software. It therefore makes a lot of sense to choose a software package that can simulate; as much as is possible, the proposed idea in a way that resembles the finished product. Fortunately, there are many software packages that exist today and some are even open source(free). Notable examples are PSpice, Simplorer, MATLAB and LabVIEW. In this project, MATLAB Simulink software was used. Simulink allows drawing schematics that have editable parameters and runtime environment similar to what real life components would do.

There are various switching devices that are used in power electronics among them bipolar junction transistors (BJTs), intrinsic gate bipolar transistors (IGBTs) and metallic oxide semiconductor field effect transistors (MOSFETs). BJTs are made by fusing two diodes back to back which results in two PN- junctions sharing a common P or N terminal. The P or N denotes positive or negative semiconductor materials. By applying a small voltage, the transistor can be controlled to operate in different zones, namely; active region (can be forward active or reverse active), saturation and cut-off. BJTs have three legs (emitter, base and collector) which can be paired in different configurations when connected in an electrical circuit with one connection common to both. The common emitter (or grounded emitter) has the emitter connected to both the input and output sides of the circuit. There is also the common base and common collector configuration. The different ways of connecting the transistor legs means that the output behaves differently in each case. Common emitter has both current and voltage gain (amplification). Common base only has voltage gain whilst common collector only current gain. Applications of these different transistor configurations can be seen in amplifiers, oscillators, on/off switches, rectifiers and filters. For the purposes needed in this research, only the configuration that makes a BJT operate as a switch will be considered. To operate as a switch, logically the BJT has to be operated in the saturation and cut off regions alternately. The downside is that even in cut off mode, there will be some leakage current flowing through the transistor. Furthermore, BJTs are relatively slow to turn off (a characteristic feature called current tail) and are susceptible to thermal runaway due to their negative temperature coefficient. Also, when the transistor is fully on, there is also some voltage dropped across the internal resistance of the transistor.
Similar in structure and properties to the BJTs are the Field Effect Transistors (FETs) which differ in that they are voltage controlled and not current controlled. A three legged representation is shown in Fig 4-1. Just as a small current is used in BJTs to switch on a much higher current through a circuit, so is a small voltage required at the gate of the FET to operate a much higher current in the circuit. FETs can be made smaller than equivalent BJTs and have lower power consumption. FETs, unlike BJTs, also have high input impedance, which means they put little or negligible load on the external components or circuitry. They can be classified as Junction Field Effect transistors (JFETs) and the more common Metallic Oxide Semiconductor Field Effect Transistors (MOSFETs) which are also called Insulated Gate Field Effect Transistors.
Unlike the BJTs which were made from two PN- junctions, JFETs are made from a piece of high resistance semiconductor material which may be doped (impurities intentionally added to alter the

electrical properties). When the doped material has a lot of positive charge carriers or holes it is referred to as being p-type(or p-channel). Alternatively, the doped material may contain a lot of negative charge carriers or electrons and will be referred to as being n-type (or n-channel). At each end of the semiconductor material are two ohmic contacts called the gate and drain.

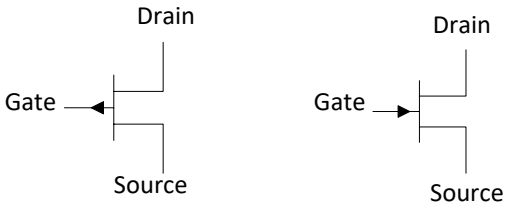


Fig 4-1: Schematic of a MOSFET

So the channel of the JFET is a resistive path through which a voltage between drain and source causes a current to flow through the drain. JFETs can conduct current either way through them depending on the voltage applied between the gate and source which biases the gate-source pn-junction thereby widening or restricting the depletion layer (region on channel that does not have mobile carriers). The amount of current flowing between the drain and source is controlled by the voltage applied at the gate, which is reverse biased.

It is possible to connect JFETs in 3 different ways just like in BJTs. There is the widely used common source configuration whereby the input is applied to the gate and the output taken from the drain. This way, the JFET will have high input impedance. Another way of connecting the JFET is the common gate configuration which does not have high input impedance and has the input applied to the source with the output taken from the drain. Lastly is the common drain (or source follower) configuration with unity voltage gain, high input impedance and low output impedance.

Another type of FET besides the JFETs is the MOSFETs whose input gate is electrically insulated from the current carrying channel. The name of MOSFETs can be a bit of misnomer as the ‘metal’ or ‘oxide’ part of it may not be an actual metal or an oxide since different dielectric materials can used for the semiconductor, e.g. silicone. Just like the JFETs, MOSFETs also have high input impedance and should be handled appropriately as they can easily be damaged with static electricity. The actual three leg chip comes either as a normally ON or normally OFF depending on enhancement type. The former indicates that current can flow through the channel even if gate voltage is zero whilst the later means no current flows through the channel with zero applied gate voltage.

The last switching device considered is the Insulated Gate Bipolar Transistor (IGBT). This mixes the advantages of a BJT namely; the low saturation voltage and combines them with those of the MOSFETs; high input impedance and high switching speed. In essence, this is a Darlington type of transistor made from an FET and a MOSFET. The only drawback is the relative cost of this device compared to BJTs and MOSFETs.

Choosing between the various switching components has become more complex than before, not that it is difficult but that there now exist a wide range of choices. For the task at hand, any of the switching devices discussed above can work, with some better than others. To elaborate, the BJTs can be used as switches in this application (operation in saturation and cut-off regions alternately), but being current controlled means the leakage current results in too much unwanted power losses (which may compound on heating problems as well). The relatively large turn-ON current required is just dissipated as heat and the current tails negatively affect the turn-OFF characteristics of BJTs.

On the contrary, FETs are voltage controlled and turn OFF or ON without significant current tails. As such, the voltage controlled devices tend to be preferred. This leaves the IGBTs and MOSFETs as the switching devices of choice.
Previously, MOSFETs were preferred in low applications whilst IGBTs would be preferred for medium to high voltage applications. In terms of switching frequency, IGBTs were considered for applications below 20khz whilst MOSFETS would generally be used in much higher switching frequencies. This is depicted in Fig 4-2 [53] below.

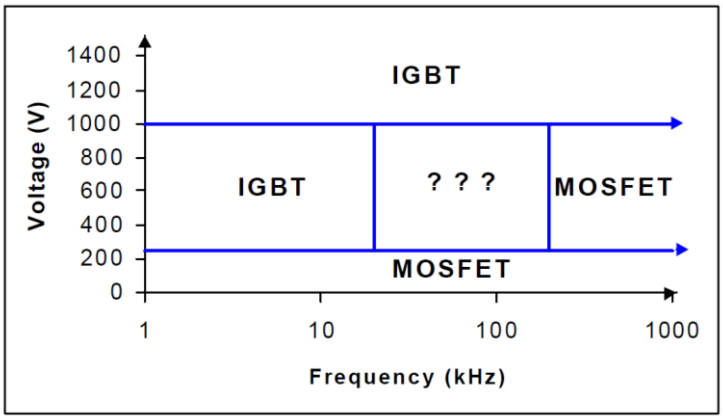


Fig 4-2: guide for selecting MOSFET or IGBT

The criteria set in Fig 4-2 have 'grey' areas where each of the two switching devices has no absolute advantage over the other thus leaving the choice of switch to the designer. Of utmost importance to the designer is the breakdown voltage rating (amongst other voltage ratings) and switching frequency. From figure above, a breakdown voltage of below 260V automatically meant MOSFETs would be used whilst switching below 20kHz meant IGBTs would be the default choice. However, research has since improved on either of the above two switching devices and the strides in the advancement of each so vast that the overlap region is even bigger [53]. This means device selection is application specific taking into account variables such as costs, heat dissipation, size and maybe speed as well. Typical operations for MOSFETs are high frequency, wide load variation, low power (or voltage) applications such as in switched mode power supplies and battery charging systems. IGBTs on the other hand are prevalent in low frequency, small load variations, high voltage (or power) applications such as in motor control, UPS and welding. This project will utilize MOSFETs as the switching devices as it will focus on low voltage - low power applications.

The previous chapter introduced how the control or gate signals are generated for each switch. It also included a summary of the most common PWM modulation techniques that are applicable to MLIs. As previously mentioned, five level DC-MLI requires the use of four carriers (m-1). Depending on PWM method, the carriers can be arranged to mimic the illustrations in chapter 3. Below is the Simulink block diagram showing PD-PWM.

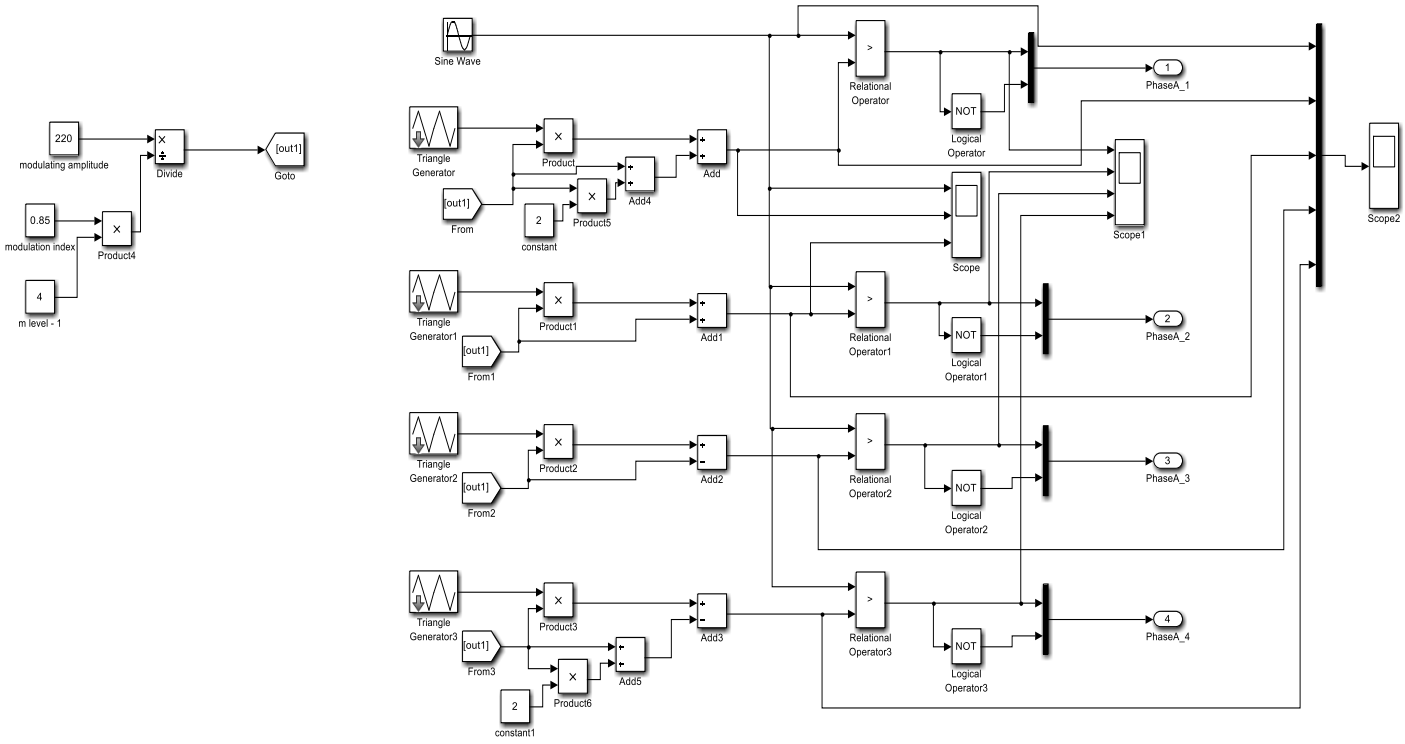
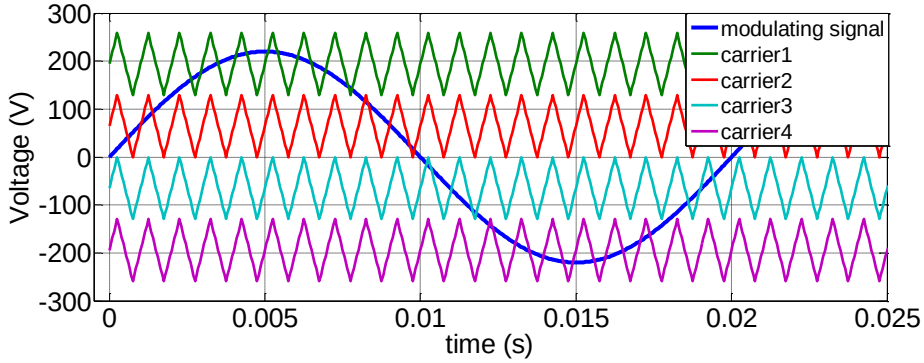


Fig. 4-3: Generation of signals using PD-PWM

Since the modulating signal's amplitude is fixed, the carrier's amplitude changes as the modulation index varies in Fig. 4-3 above. Blocks are used to compute the modulation index using (3.5) from chapter 3. The comparator compares the values of the modulating and carrier waveforms. Whenever the modulating signal is more positive than the carrier a positive or high signal is sent to the output. Part of this output is sent through a logic NOT gate to produce the complement of the high output signal which is also needed. The 'Go to' block above is used to store the value of the carrier amplitude. Since the triangle generator function outputs a triangle wave centred about zero with peak unit value, its output must be multiplied by the carrier amplitude then the same amplitude added or subtracted to the resultant for the waveform to be shifted from the zero centre. The triangle waveforms above the zero crossing are shifted to their positions by adding multiples of the carrier amplitude to the function generator's output. Those below the zero crossing are obtained by subtracting multiples of the carrier amplitude from the resultant of the function generator.

The blocks named 'Triangle Generator' to 'Triangle Generator3' in Fig. 4-3 represent the carrier signals with unity magnitude. 'Triangle Generator' represents carrier1 and carrier4 is represented by 'Triangle Generator3'. Fig. 3-12 is repeated from the previous chapter below.



The amplitude of the carriers can be calculated using the modulation index equation (3.5). Suppose the modulation index is m_a = 0.8 and that the modulating signal is the normal household ac voltage (220V), then the carrier's amplitude is calculated as:

$$m_a = \frac{V_m}{(\mathrm{m}-1)V_{tri}}$$

$$0.8=\frac{220}{(5-1)V_{tri}}$$

Hence the carrier's amplitude required is $V_{tri} = 68.75V$. The above calculation is what the blocks on the right in Fig. 4-3 are accomplishing and since the MI is varied in this study it is necessary to have a block just to adjust one parameter and not all numbers.

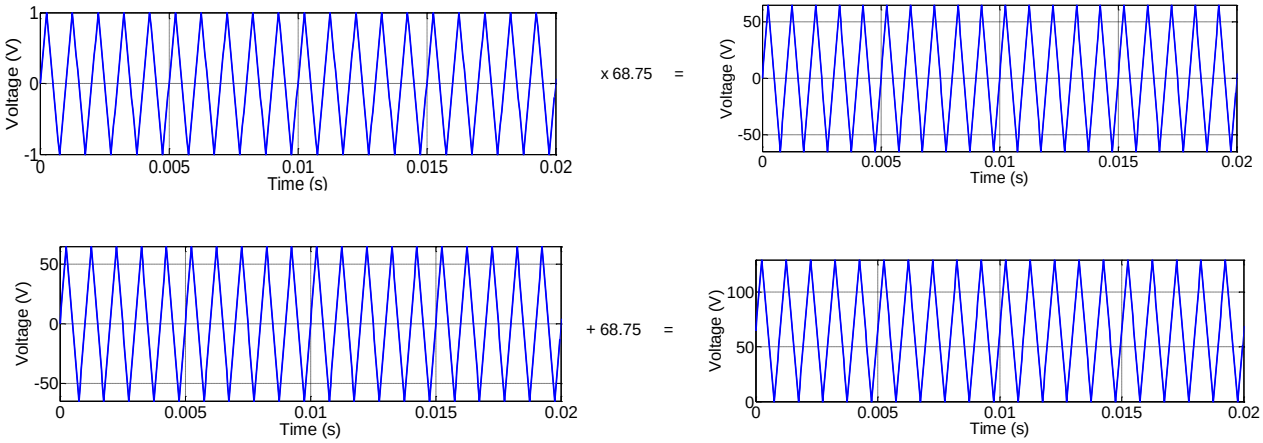


Fig. 4-4: Generation of carrier waves

The illustration above in Fig. 4-4 shows how the carriers are made using Simulink block diagrams in Fig. 4-3. First the carrier is amplified (by multiplication to the required amplitude) and then translated (by addition or subtraction of multiples of carrier amplitude) to the required voltage level. The four carriers will occupy contiguous bands as their centre values only differ by multiples of carrier amplitude. The other carriers are made by adding or subtracting multiples of the amplitude as described above to shift the carrier to the desired centrum.

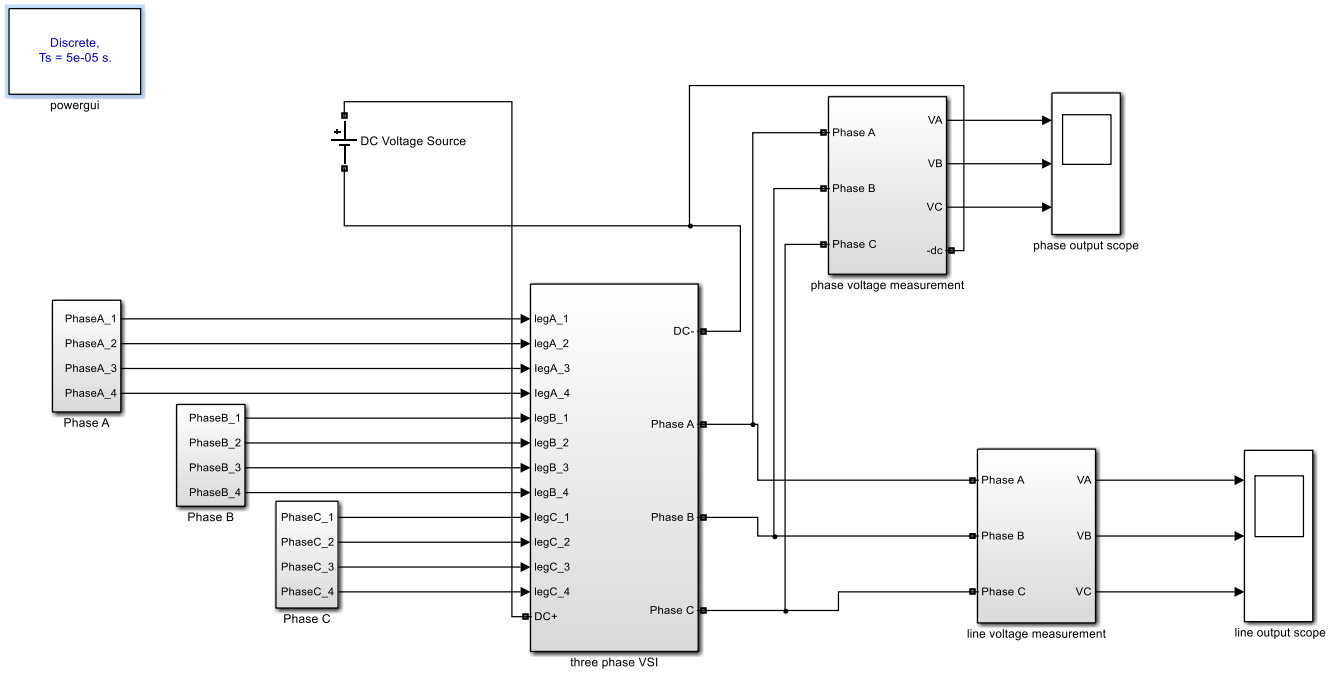


Fig. 4-5: block diagrams combined into subsystems

The block diagrams for the production of the gate signals can be combined to form a subsystem and connected to the main VSI circuit as in Fig. 4-5 above. Fig. 4-3 is transformed by the subsystem function in Simulink to become a single block such as 'Phase A' block in Fig. 4-5. The block named 'three phase VSI' is the Simulink representation of Fig. 3-7 and each of the phases are controlled by the blocks named phase A, phase B and phase C. As described above, each of the blocks has eight signals, four from the original output and four from complementing the original output. Voltage and current measurement blocks are added before the scope.

The blocks for generating pulses used for the DC-MLI will resemble those for the FC-MLI due to the similarities in the structure of these topologies. As such, Simulink diagrams both look like the above figures (Fig. 4-3 and Fig. 4-5) except for the routing of each signal to the gates as that depends on topology.

To view the contents of each subsystem blocks such as in Fig. 4-5, simply right-click on the block and select look 'under subsystem' or 'mask'.

4.1 DC-MLI Voltage Source Inverter Simulink setup

The three phase five level DC-MLI with similarly rated diodes is shown in Fig. 4-8. As described in the previous chapter, the VSI has 'm-1' top switches and the same number for the corresponding bottom switches per leg or phase. The number of top switches is also equal to the number of capacitors that are required for establishing the DC link, which can be shared in the case of the DC-MLI or the FC-MLI. A total of '(m-1)(m-2)' clamping diodes are needed when the diodes used are identically rated. The block named 'three phase VSI' is made up of three series connected single phase blocks such as the one shown below in Fig. 4-8. With regards to the control signals for each switch, the topmost control signal (going to the topmost switch 'Mosfet') comes from the first control signal 'phase_A1'. The complement of this control signal (called 'phase_A5') is sent to the complement of the topmost switch, which is 'Mosfet4', the mosfet or switch at the top of the bottom half set of switches. Similarly, the second switch from the top set of switches from Fig. 4-8

is named ‘Mosfet1’ and is controlled by the signal named ‘phase_A2’ whilst the complement control signal ‘phase_A6’ controls the second complement switch ‘Mosfet5’. The other control signals all power the remaining gates in the very same way described above. The distribution of the control signals is illustrated in Fig. 4-6 below.

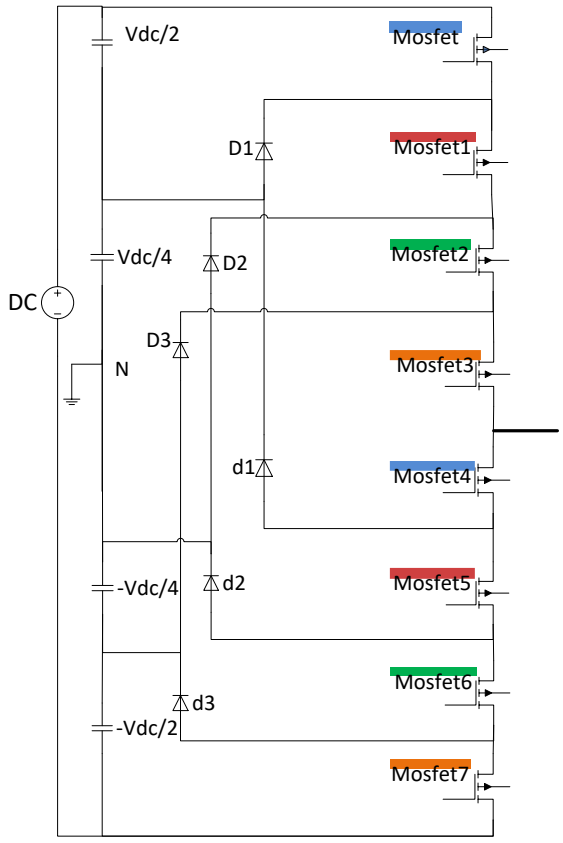


Fig. 4-6: gate control signals distribution DC-MLI

The topmost signal (for ‘Mosfet’, colour blue) in the top switches is complementary to the topmost signal of the bottom switches (‘Mosfet4’, colour blue) in Fig. 4-6 above.

4.2 FC-MLI Voltage Source Inverter Simulink setup

Fig. 4-9 shows the configuration for the five level FC-MLI in Simulink. Just like the DC-MLI, this too has ‘m-1’ top switches with the same number of the bottom complementary switches per phase. Likewise, the number of top switches is also equal to the number of capacitors that makes up the DC link. In the place of clamping diodes which the DC-MLI uses are clamping capacitors. A total of ‘ $\frac{(m-1)(m-2)}{2}$ ’ clamping capacitors per phase are required, meaning the FC-MLI will have half the number of clamping components than its DC-MLI counterpart. Although the FC-MLI and DC-MLI have a similar VSI structure, the switching or control of gates is different. For the DC-MLI the topmost gate was controlled by the topmost signal whilst the gate’s complement would be powered by the complement of the first signal. Here, the output line (the middle section dividing the top four switches from the bottom four switches) acts as a mirror line for the gate control signals. This means the complement of the signal powering the topmost switch goes to control the bottom most switch. Similarly, the bottom switch from the top set of switches is complemented by the topmost switch in the bottom half. The switching combinations are illustrated in Fig. 4-7 below.

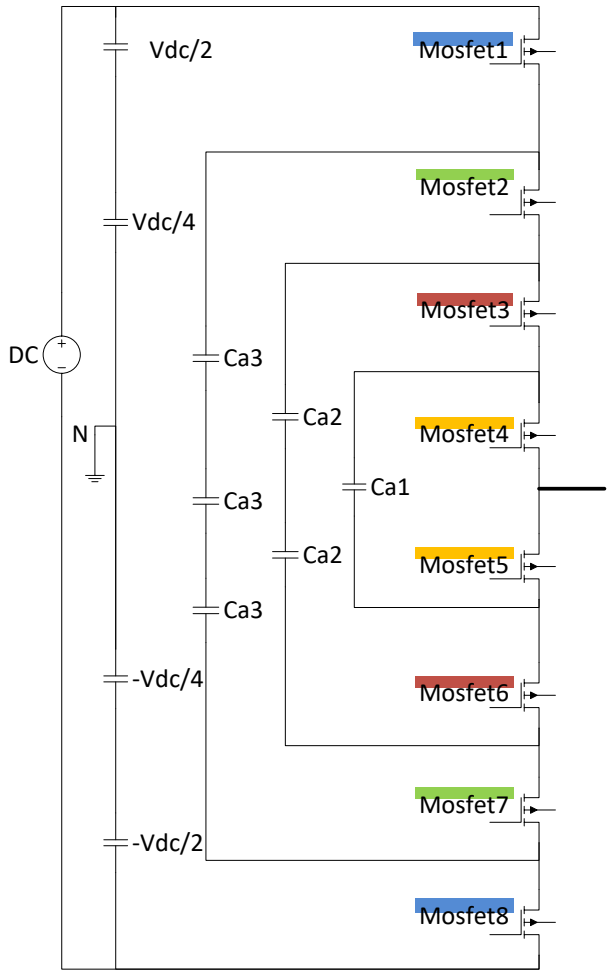


Fig. 4-7: gate control signal distribution CC-MLI

Mosfet4 (orange) is the last switch from the top group of switches and has the next switch (Mosfet5) as its complement in Fig. 4-7 above. The consequences of not correctly assigning the switches or their complements will be discussed in the following chapter for all the inverter topologies.

4.3 CHB-MLI Voltage Source Inverter Simulink setup

CHB-MLI has a different structure to the above two topologies but the block diagrams at subsystem level may be made to be similar. This topology uses less DC bus capacitors in single phase applications when compared to the other two topologies, but more when used in three phase application as each dc source may require a smoothing capacitor. A total of $\frac{(m-1)}{2}$ cascaded cells per phase are required for the 'm' level inverter as illustrated in Fig. 4-10. The advantages and rules pertaining to how dc sources are reduced have been covered in the previous chapter under "Other Multilevel Inverter topologies" and under "Cascaded H-Bridge MLI". Just like the two above topologies, this topology requires a certain pattern in order to work properly. Some combinations may seem to work under open circuit or no load conditions but fail to work properly when under load. Again, this will be illustrated in the following chapter. The distribution of the gate control signal is shown in Fig. 4-10 below.

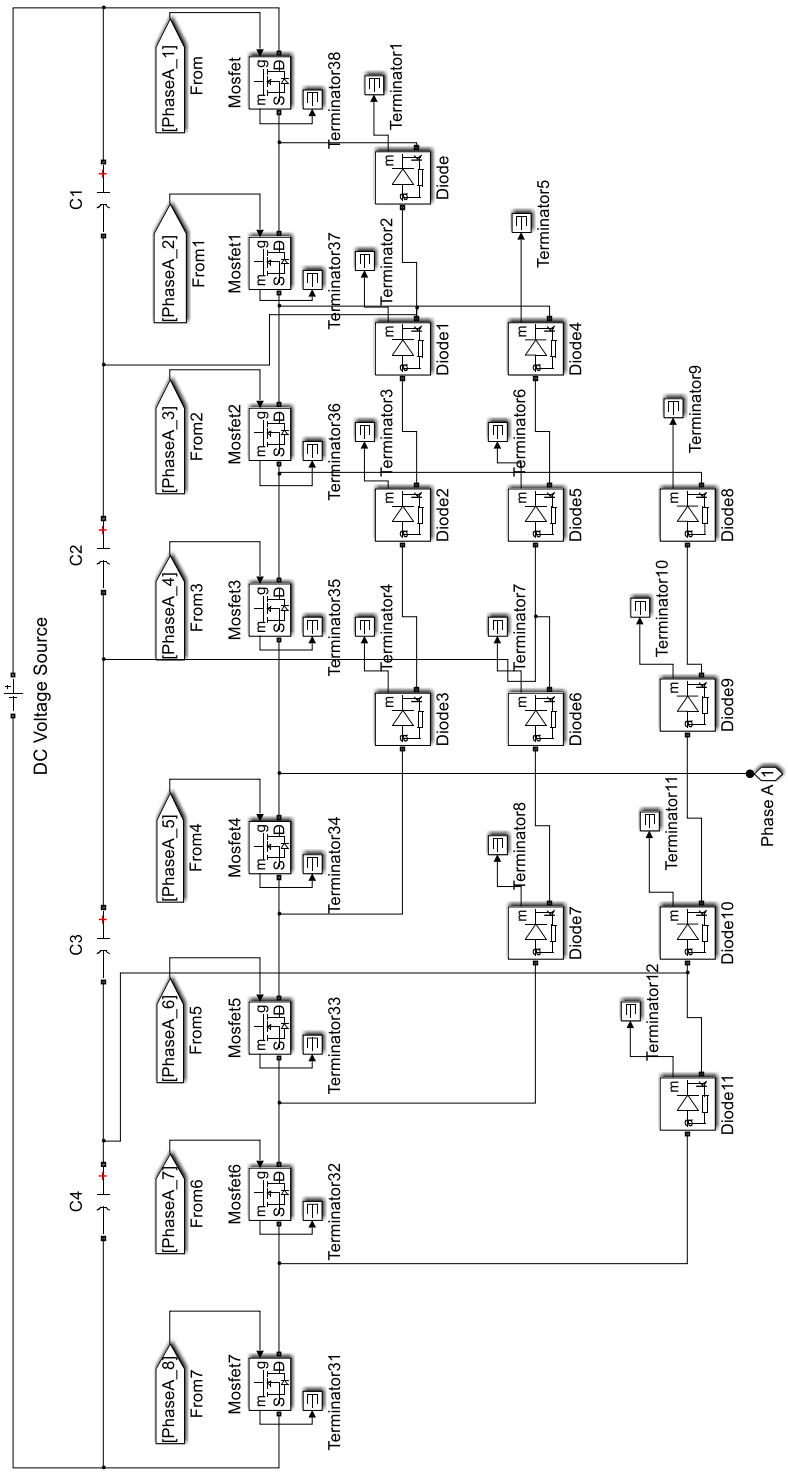


Fig. 4-8: single phase five level DC-MLI Simulink model

Fig. 4-8 above shows the Simulink model for a five level DC-MLI. From Fig. 4-6, it can be seen that the control signal 'PhaseA_1' powers the topmost switch and its complement is signal 'PhaseA_5'.

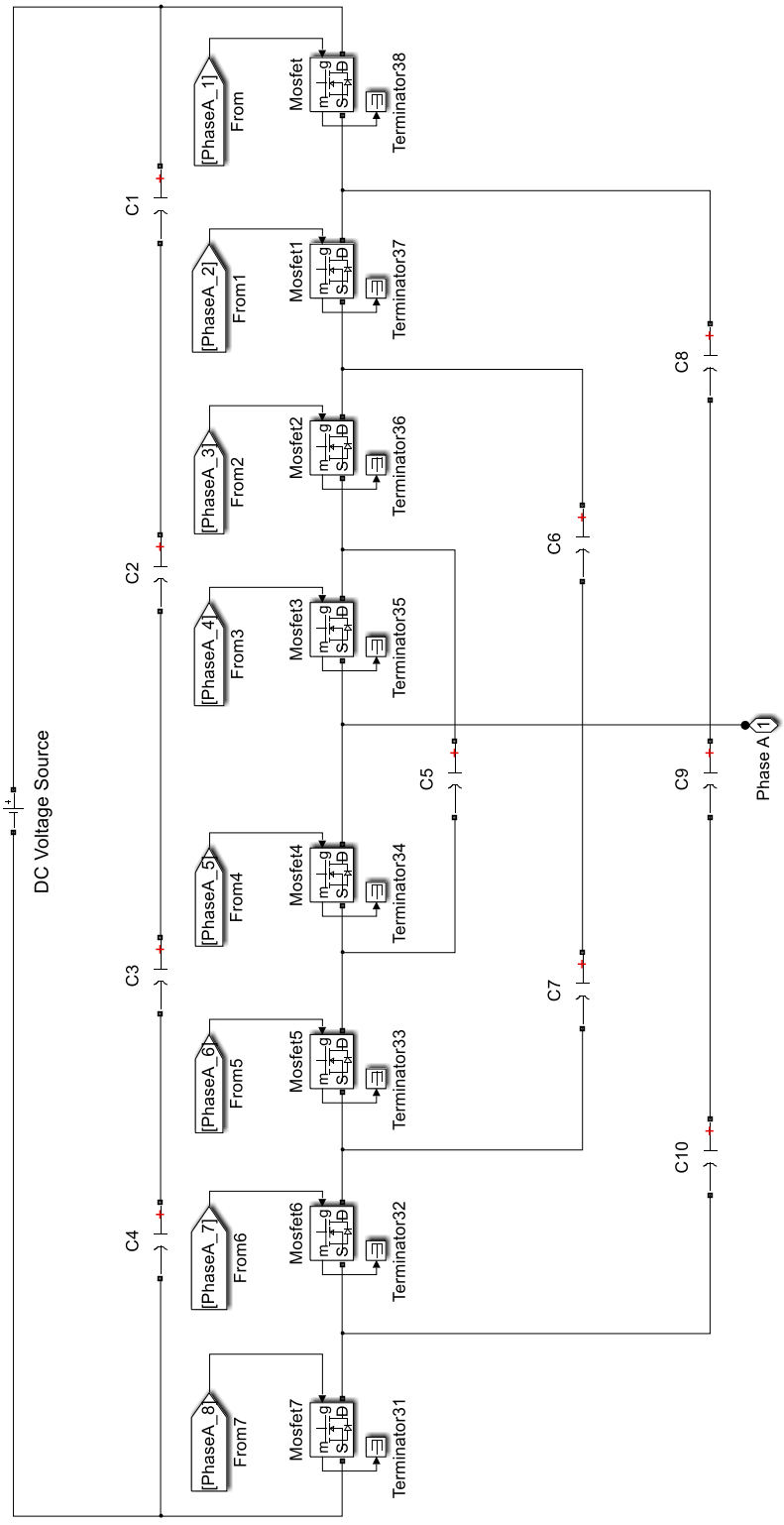


Fig. 4-9: single phase five level FC-MLI Simulink model

Fig. 4-9 above shows a Simulink model for the five level CC-MLI (or FC-MLI). It can be seen that control signal ‘PhaseA_1’ and ‘PhaseA_8’ are complements by the help of the illustration in Fig. 4-7.

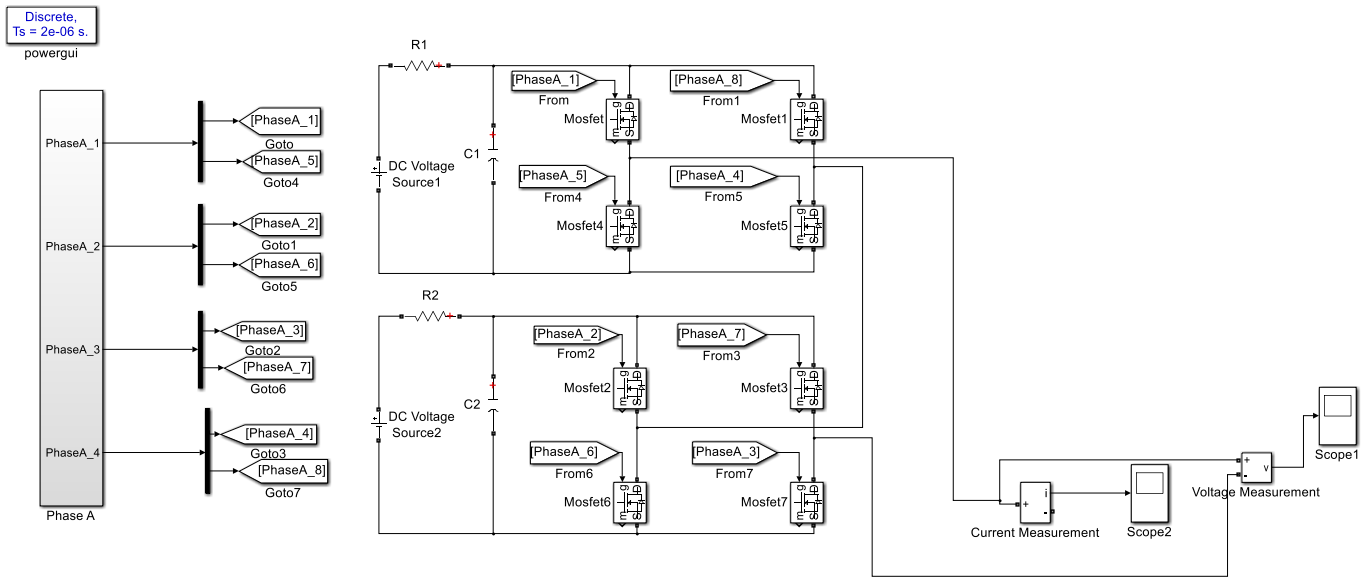


Fig. 4-10: Single phase 5 level CHB-MLI

In Fig. 4-10, the subsystem block ‘Phase A’ contains the model circuit for the generation of signals as illustrated in Fig. 4-3. In essence, if the subsystem block was to be recreated it would be identical to the one shown there. As shown in Fig. 4-3, two complementing signals are sent to out port named ‘PhaseA_1’ by means of a mux. Above in Fig. 4-10, a demux is used to separate the combined signal into the constituent signals to be sent to complementing gates. As such, signal ‘PhaseA_1’ is a compliment of signal ‘PhaseA_5’ and both are sent to one leg of the first unit in the CHB-MLI model which requires complement signals to avoid short circuit conditions within the leg of the h-bridge.

The above figures have illustrated how 5 level MLIs are applied. Fig. 11-1 up until Fig. 11-3 show how 3 level MLIs are implemented, Fig. 11-4 up until Fig. 11-7 show how the 7 level MLIs are implemented and lastly Fig. 11-8 up until Fig. 11-11 show how the 9 level MLIs are implemented.

5. Hardware implementation, Filtering and Harmonics Prediction

Hardware implementation and testing follows from satisfactory software simulation. A good design allows the hardware setup to mimic as much as is possible the software setup of the VSI circuits. A few conversion or modifying blocks such as an analogue to digital (ATD) or digital to analogue converter (DAC) and gain amplifiers may be added to the hardware setup whereas it may have been not necessary when doing software simulation. This is to be expected when working with hardware components from software simulations. This will be explained in detail below.
The output from hardware will require some form of filter before being used or sent to storage or into the grid. This is because normally there are unwanted harmonics that are within the output and are removed or reduced to the allowable percentages by using filters. The steps when designing a suitable filter will be explained.
Finally, the unwanted harmonics can be predicted in several ways. A few of these ways are described before a novel approach is used employing statistical analysis to better predict harmonics.

5.1 Hardware Implementation

Since software simulations are done in Simulink, it is logical first to search for microcontrollers or microprocessors which have MATLAB-Simulink support. This would mean that instead of codding everything from the beginning, only a few registers are necessary to set up or initialize and the rest the support package will do. This means either converting Simulink diagrams into code for the controller and running from the controller after 'building' this new code automatically or having some sort of bridge that links the Simulink software to a specific runtime routine running from the controller. In the event that no support is offered for Simulink with a desired microcontroller or should more control be needed over finer details in what is transpiring within the converted code, then it would be necessary to code everything from the beginning although this would be more time consuming.
A Texas Instruments controller was selected for this project. The reasons for selecting this were that it has a powerful 32bit CPU, many I/O ports, good precision with an IEEE754 single precision floating point and that it has support for Simulink hence no need for extensive coding. Support packages for the Texas Instruments Digital Signal Processing unit (DSP) are downloaded which runs alongside Code Composer software. As said before, these enable users to run simulations directly off MATLAB-Simulink into a DSP controller. Pulses for the gates of the inverter drivers are generated in MATLAB and are passed out via the I/O ports on the controller. The controller used is an F28335 in the Texas Instruments c2000 micro-controller family. The output signals from the controller are between 0-3V. These are for controlling the gates of the switches. However, the MOSFETs used require gate signals of 15V for a 'high' and 0V for a 'low'. To do this, a voltage level shifter is used. A block diagram summarises the process for hardware implementation below.

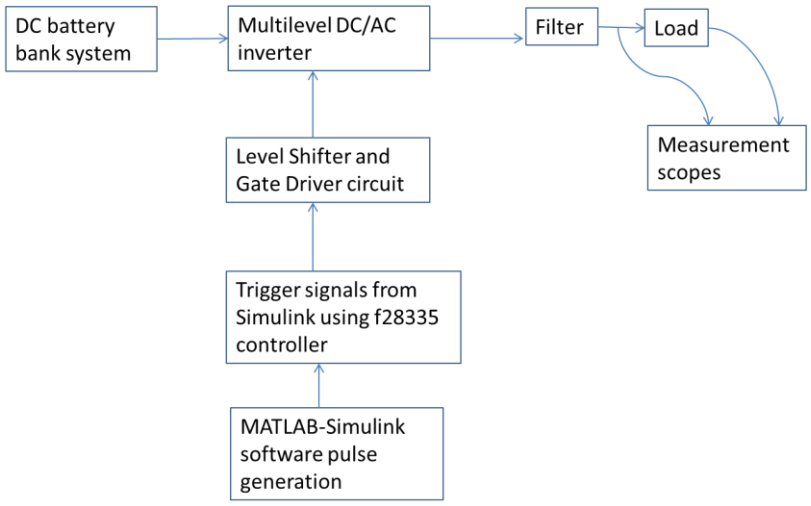


Fig. 5-1: Block diagram for hardware implementation

The DC battery system in Fig. 5-1 is assumed to be self-reliant with its own charge controllers and regulators. Simulink simulations are run on a computer generating the required signals which are sent out from the I/O ports of the controller. The controller outputs are 0-3 V so there is need of level shifting the signals to the required voltages depending on switching components used. One leg implementation of the five level CHB-MLI is shown below.

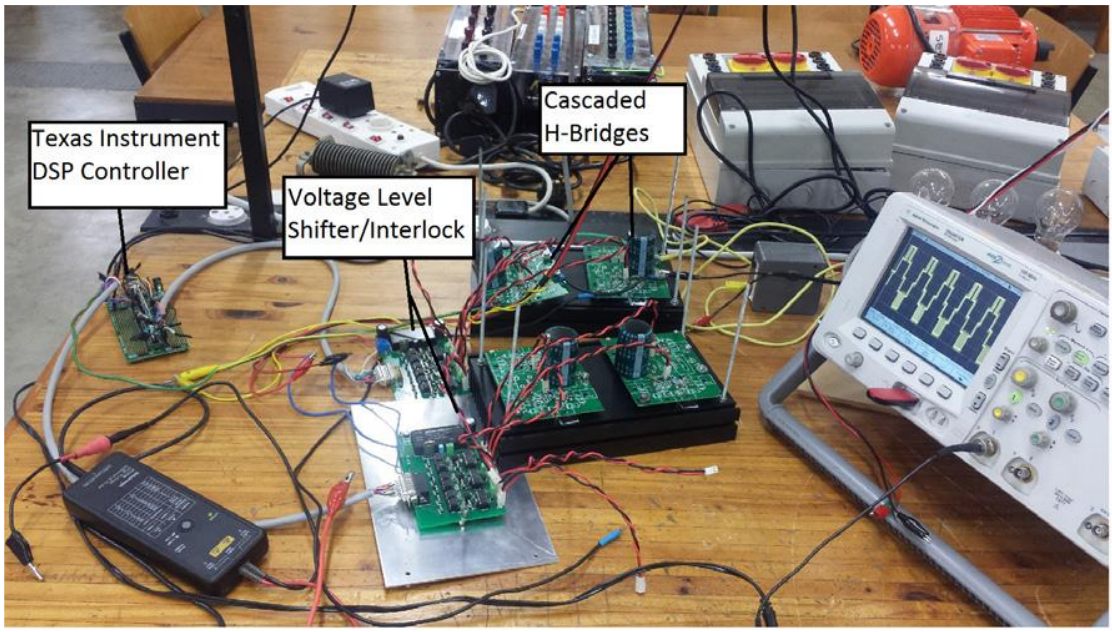


Fig. 5-2: single phase implementation for the 5 level CHB-MLI

Fig. 5-2 above shows the hardware setup before the filter and load are connected to the 5 level CHB-MLI. Switching signals are generated from a computer whose specifications are as follows; Intel core i7 4GHz, 16Gb ddr3 Ram. These signals run from the computer to the DSP controller through a USB cable shown connected to the controller from which they are sent to the level shifter circuit. The level shifter circuit ensures that the signals that are about to be sent to the actual MOSFETs are in fact within the right range, for example, the 3V 'High' signal from the controller would not be high enough to switch the MOSFET ON. Therefore, without the level shifter circuit the switch would interpret the 3V the same way as the 0 volts or 'Low' signal, which is not the desired outcome. Besides shifting the voltage values to the correct ranges the level shifter circuit incorporates interlocks to ensure that there are no short circuit conditions just in case one switch

tries to go ON before its complement is fully OFF. From the level shifter, the signals are then sent to their respective H-bridges. The DC bus voltages are 25.5V for both DC sources supplying the two H-bridges in the single leg above. The oscilloscope is from Agilent Technologies, model DSO6012A, 100MHz and can sample up to 2GSa/s. The high voltage differential probe in Fig. 5-2 is a Tektronix P5200 model, with an output tolerance of ± 2.6V, 1MΩ. The components used and their key specifications are given in Table 11-1 in the appendix section. The results from hardware will be shown and discussed in the next chapter.

5.2 Output filtering in MLIs.

The goal of using MLIs as opposed to 2 level inverters is to achieve more sinusoidal output which has fewer distortions than that of the regular inverters. However, output from a MLI may have a good reduction of harmonics but still requires a filter to further reduce them to meet IEEE standards. Several methods have been discussed by various authors of how best to design the output filter for a VSI. Some designs are based on the current ripple calculations, iterative algorithms, and power losses optimization [3]. Internationally acceptable output voltage distortions are governed by different standards – IEEE 519-1992 (revised slightly in IEEE 519-2014), EN-62040-3:2005 and IEC 61000-2-2 are examples. IEEE Std 519 requires that the output THD be less than 5% and that the largest single harmonic be less than 3% of the fundamental. It is therefore important to note both the fundamental switching harmonics and the THD when examining the harmonics spectrum. Fig. 5-3 below show how the filter is connected between the output of the VSI and the load.

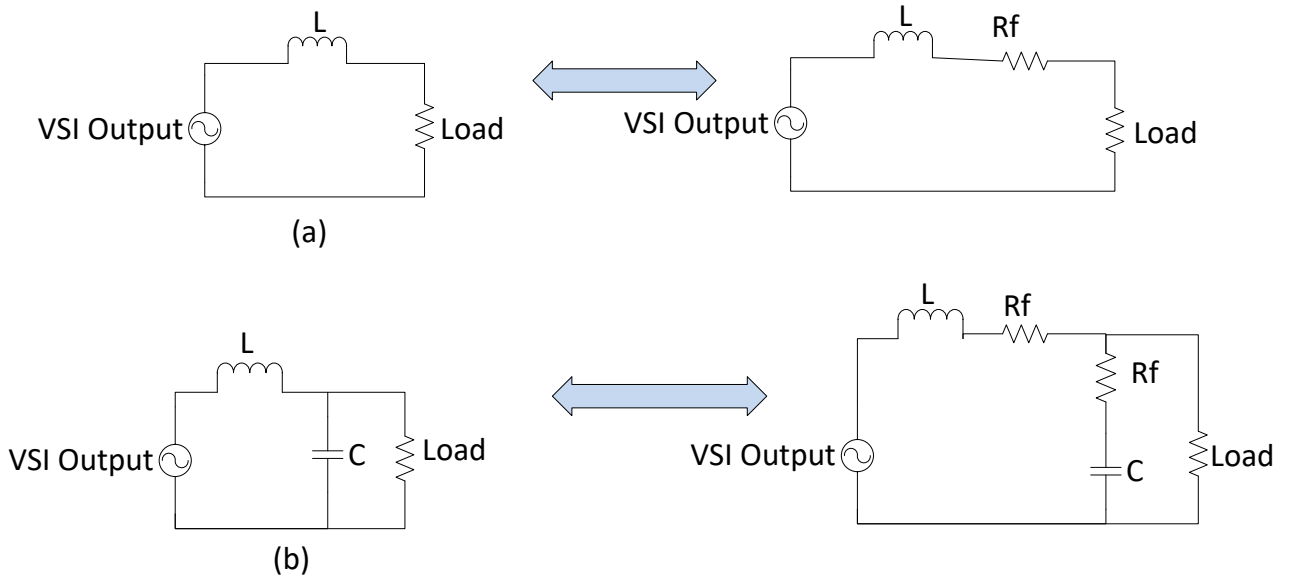


Fig. 5-3: VSI output filtering circuit and equivalent; a) L only filter and equivalent, b) LC filter and equivalent.

In Fig. 5-3 above, (a) is the L only filter whose actual model may include the internal resistance from the filter inductor Rf. (b) shows that when two components are connected their internal resistances may be included separately as shown by the two filter resistances Rf in series with either the inductor or the capacitor. However, in the last scenario, the internal resistances may be lumped into one internal resistance. Now suppose the impedance of the capacitor is Z_c, the impedance of the

inductor Z_L, and the impedance of the internal resistance combined is Z_R. The output voltage for (b) can be found by:

$$V_{out} = \frac{Z_c}{Z_c+Z_L+Z_R} V_{in} \tag{5.1}$$

Thus the transfer function H(jω) is found by:

$$H(\omega) = \frac{Z_c}{Z_c + Z_L + Z_R} = \frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + j\omega L + R}$$

$$= \frac{\frac{1}{j\omega C}}{\frac{1 + j\omega C j\omega L + j\omega CR}{j\omega C}}$$

$$= \frac{\frac{1}{j\omega C}}{\frac{1 - \omega^2 CL + j\omega CR}{j\omega C}}$$

$$= \frac{1}{1-\omega^2 CL+j\omega CR} \tag{5.2}$$

When these equations are derived, there are many assumptions that are made and more still when they are being interpreted. For instance the last term in the denominator of (5.2) may be neglected if it is assumed that because of the small equivalent series resistance value of the inductor that $|\omega^2 CL| \gg |j\omega CR|$.

If the load current is treated as a disturbance then (5.2) will hold, otherwise there is a term which needs to be included in it should the load current be non linear or when applied to a varying load. The finer details of other filter selection or design will not be discussed further. Rather, a paper which goes into good detail and easily satisfies the filter requirements of this thesis is used here[44], [45]. It gives equations to determine the LC filter parameters for each phase which will satisfy IEEE Std 519. These are applicable to any of the basic topologies. For more than 3 levels:

$$l_f = \sqrt{\frac{1}{(m-1)M}} \times \frac{1}{f_s} \times R \tag{5.3}$$

where l_f is the filter inductor whose value is to be found, m is the number of levels, M is the modulation index, f_s is the switching frequency and R is the load resistance value. In a similar way, [44], [45]defines the capacitor value C_f in an LC filter as:

$$C_f = \sqrt{\frac{1}{(m-1)M}} \times \frac{1}{f_s} \times \frac{1}{R} \tag{5.4}$$

For a three level VSI, the equations are:

$$l_f = \frac{1}{f_s} \times R \tag{5.5}$$

$$C_f = \frac{1}{f_s} \times \frac{1}{R} \tag{5.6}$$

As for the two level VSI (excluding the cascaded H bridge topology) the filter parameters are found in the same way as the parameters for more than 3 levels. The only difference will be that the (m-1) term would disappear as m is 2 in a two level VSI. Results of unfiltered output and those after implementing the filter are shown in the next chapter appropriately called 'Results'.

5.3 Prediction of harmonics using machine learning

The principle behind machine learning is based on the fact that any function f(x), can be approximated with arbitrarily a small error as a linear weighted sum of a finite number of distinct basis functions. These basis functions should fit the points and interpolate smoothly between the points. This makes it possible to predict the function value for new points outside the training data. In other words, given a known small value ε, an unknown function f(x) can be approximated using single layer feed forward network (SLFN) with a sufficiently large number of hidden layers, L. An illustration using basic functions is shown below.

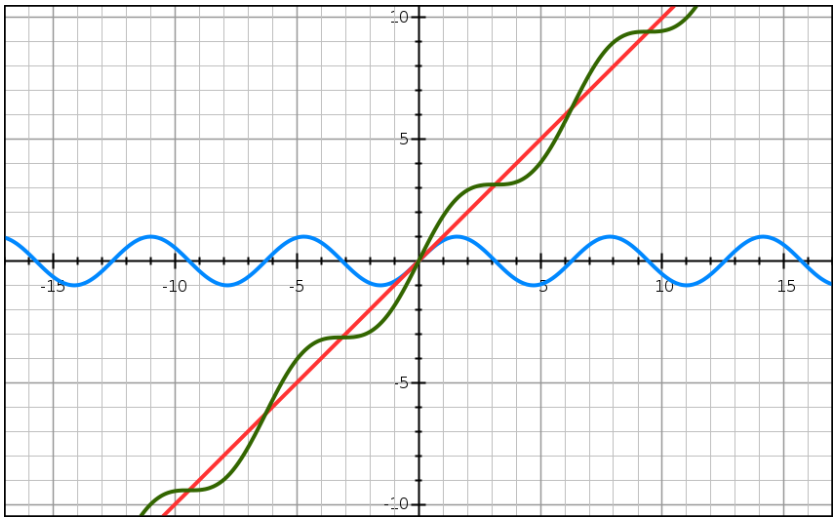


Fig. 5-4: example of addition of functions

The blue waveform ($f_1(x) = \sin x$) and the red waveform ($f_2(x) = x$) can be added to form the green waveform $f(x) = \sin x + x$ in Fig. 5-4 above. It can be said that f(x) is composed of $f_1(x)$ and $f_2(x)$ as the basic building blocks. Similarly, more complicated waveforms can be thought of as being made up of many distinct basic functions coming together to produce one complex waveform. When a large number and layers (which may do functions like multiplication for gain or addition for translating points linearly) is approximated, there is obviously an error which may arise as approximations are not always equal to the functions being approximated. This can be seen in equation below.

$$| f_L(x) - f(x) | < \varepsilon \tag{5.7}$$

where L is the number of hidden nodes.

Consider the SLFN shown in below where inputs 'x' give output 'o'.

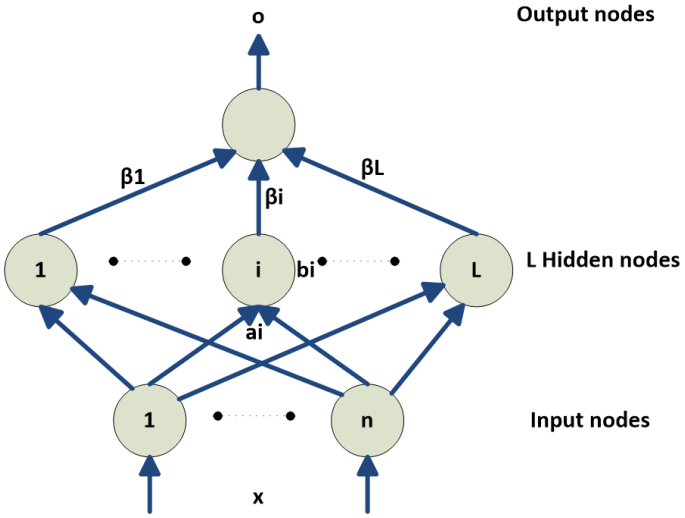


Fig. 5-5: single layer feed forward network

Fig. 5-5 shows the process of using neural networks to determine an unknown function or value through the output of the neural network.
The hidden nodes output is determined by the equation:

$$G(a_i, b_i, x) = g(a_i \cdot x + b_i) \tag{5.8}$$

where a_i are the input weights connecting the i^{th} hidden nodes and input nodes, b_i is the hidden nodes threshold or bias factor, x are the inputs, β the weight vector connecting the hidden node to the output and 'o' is the output of the SLFN.
The output of the network is:

$$f_L(x) = \sum_{i=1}^{L} \beta_i G(a_i, b_i, x_j) = t_j \tag{5.9}$$

and can be written in matrix form as

$$H_{tr}\beta = T \tag{5.10}$$

where H_{tr} is the hidden layer output matrix (from training data hence the tr subscript) and T is the output or target matrix.
Using the same matrix form, the individual matrix components in (5.10) can be written as:

$$H(a_1, \dots, a_L, b_1, \dots, b_L, x_1, \dots, x_N) = \begin{pmatrix} G(a_1, b_1, x_1) & \cdots & G(a_L, b_L, x_1) \\ \vdots & \ddots & \vdots \\ G(a_1, b_1, x_N) & \cdots & G(a_L, b_L, x_N) \end{pmatrix} \tag{5.11}$$

$$\beta = \begin{pmatrix} \beta_1^T \\ \vdots \\ \beta_L^T \end{pmatrix} \tag{5.12}$$

$$T = \begin{pmatrix} T_1^T \\ \vdots \\ T_N^T \end{pmatrix} \tag{5.13}$$

where H is an N×L matrix, β an L×m matrix and T an N×m matrix.
In summary, ELM involves a three step process. Firstly, assign randomly the input weights a_i, and then the hidden nodes impact/bias factor b_i. This will enable the calculation of the hidden node matrix, H, the second step. Lastly, calculate the output weights by making the weights β the subject of interest in (5.10) to yield

$$\beta = TH_{inv} \tag{5.14}$$

where H_{inv} is the pseudo- inverse of the matrix H. The pseudo-inverse is taken in order to ensure that H is invertible.
From (5.7), a cost function, C, can be derived so as to tune the design parameters.

$$C = \sum_{j=1}^{N} | f_L(x) - f(x) |^2 \tag{5.15}$$

To minimize the cost function, the parameters of the network (a_i, b_i and β) are adjusted.

There are various basis/activating functions which can be used to estimate unknown functions in SLFN. Examples include the sinusoidal, radial and sigmoidal functions. For this paper, the sigmoidal basis function is used. Varying the number of basis functions then recording how far the true values are from the predicted values gives the rms error, which is related to the cost function in (5.15) that is to be minimized. Results for choosing the number of basis functions are shown in the next chapter.

6. Results

Various performance markers or indices can be used when evaluating the difference between the numerous MLI topologies. They can be quantitative markers such as the magnitude of the output voltage (V_{out}) or current (I_{out}), or qualitative indices, such as the amount of distortions in the output voltage or current. In this research, the magnitude of the output voltage (and current under specified load), the THD in the output and the filter components required to bring the harmonics to acceptable levels are discussed. Software results are introduced first and later in the chapter they will be compared with the output from hardware.

6.1 PWM schemes comparison

PD PWM, POD PWM and APOD PWM all work in a similar manner with slight differences in the orientation of individual carriers with respect to each other. The other PWM technique which will be compared to the level shifted PWM techniques is the PS PWM which differs from the previously mentioned ones as being the only one which does not do level shifting. To determine how the different switching scheme affects the output voltage, 3, 5, 7 and 9 levels of MLIs are used.

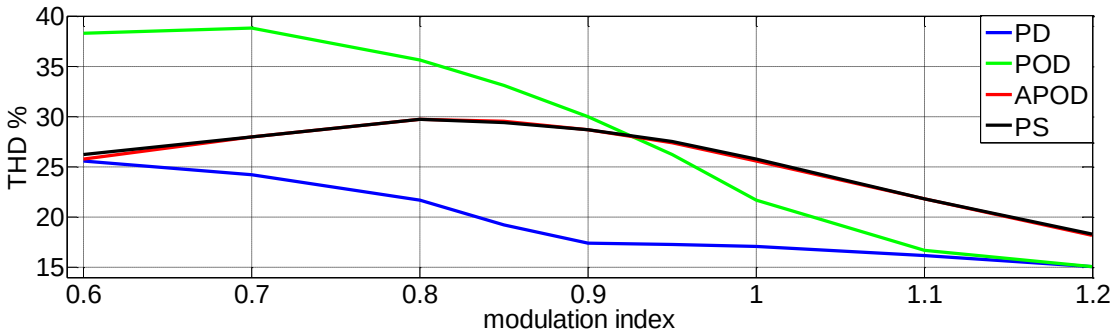


Fig 6-1: PWM comparison 5 level MLI

Fig 6-1 shows the effects of the various PWM schemes on a standard CHB-MLI circuit that has all the other things kept constant except for the PWM switching. The PD PWM produces the least THD across the range of MI used as is expected. THD ranges from just below 15% to a maximum of about 37% when POD-PWM is used. The modulation range is allowed to go into the over-modulation region just to illustrate how these PWM methods differ when in that region but this research will only focus on modulation indices less than or equal to 1. Similar plots are obtained for the seven and nine level MLIs, with PD-PWM having the least THD across the MIs used. These are shown in Fig. 6-2 and Fig. 6-3 below.

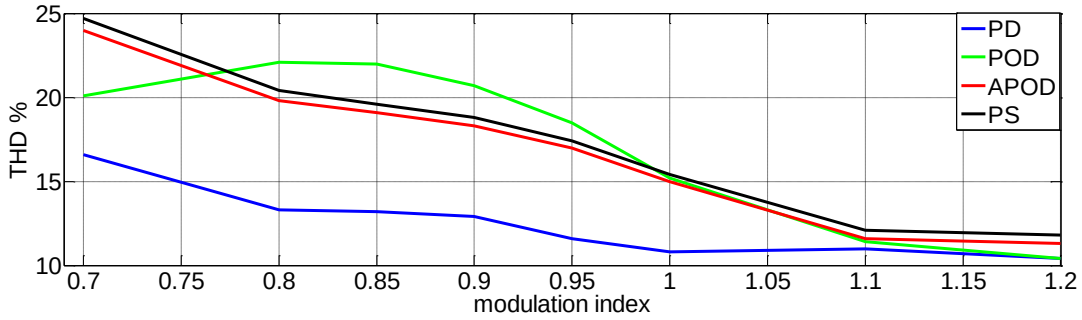


Fig. 6-2: PWM comparison 7 level MLI

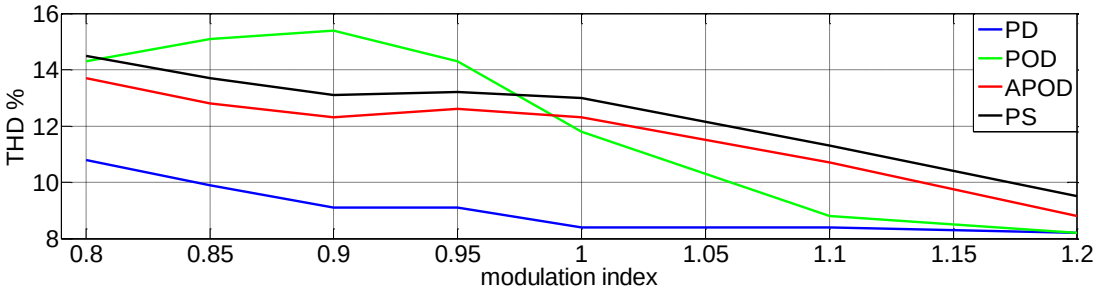


Fig. 6-3: PWM comparison 9 level MLI

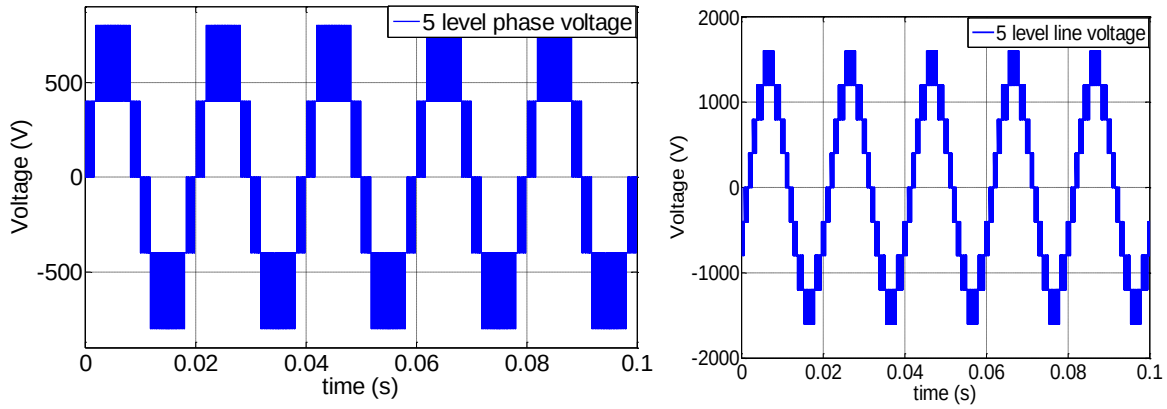
The above figures verify that PD PWM gives the least THD across the MI used for the different level of MLI selected and is used as the PWM switching scheme of choice from this point onwards.

6.2 Output Voltage and Current waveforms from simulations

Real life scenarios often expose power inverters to different non ideal conditions under which they should work. These range from open circuit (no load), load conditions, fault conditions, starting conditions (especially for machines and motors which may require large start up currents) among others. Some of these conditions are briefly described below.

6.2.1 Correct inverter configuration with no load

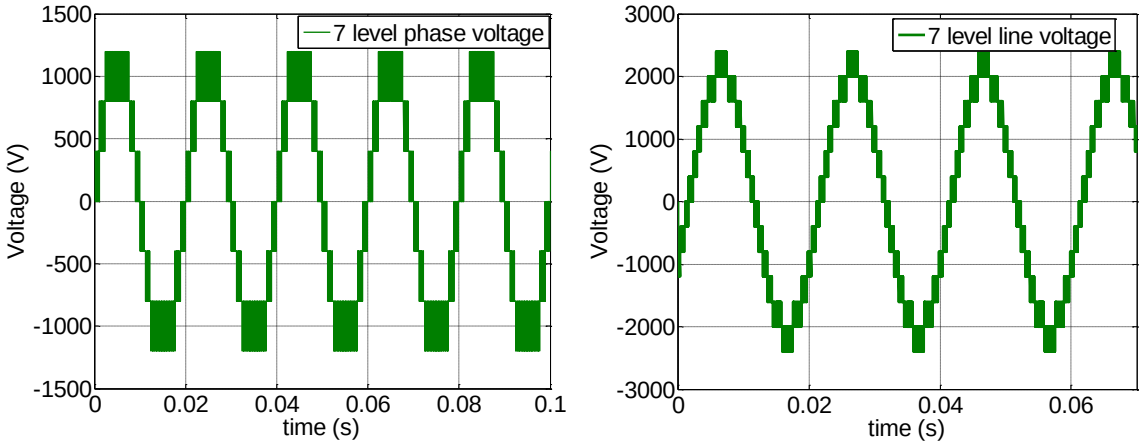
Harmonic signatures for the three basic topologies for MLIs are almost the same as THD is dependent more on the switching scheme used and the MI, with switching frequency held constant. Each topology has its own unique advantages which have been discussed in the early chapters. Shown in figures to follow are the outputs from the CHB-MLI whose outputs are representative of the other basic topologies, except in special cases where it will be mentioned which topology is being referred to.



(a) (b)

Fig. 6-4: (a) 5 level phase voltage MLI output

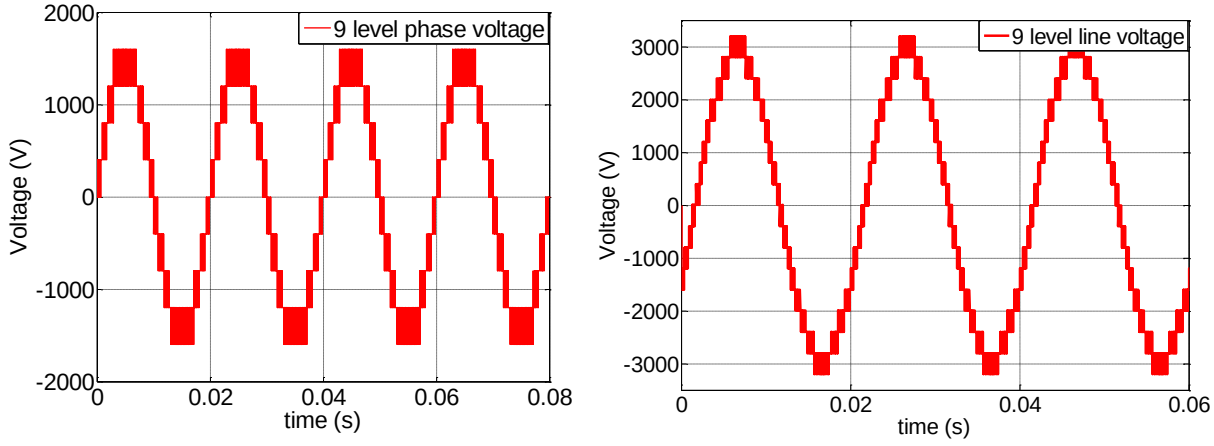
(b) 5 level line voltage MLI output



(a) (b)

Fig. 6-5: (a) 7 level phase voltage MLI output

(b) 7 level line voltage MLI output



(a) (b)

Fig. 6-6: (a) 9 level phase voltage MLI output

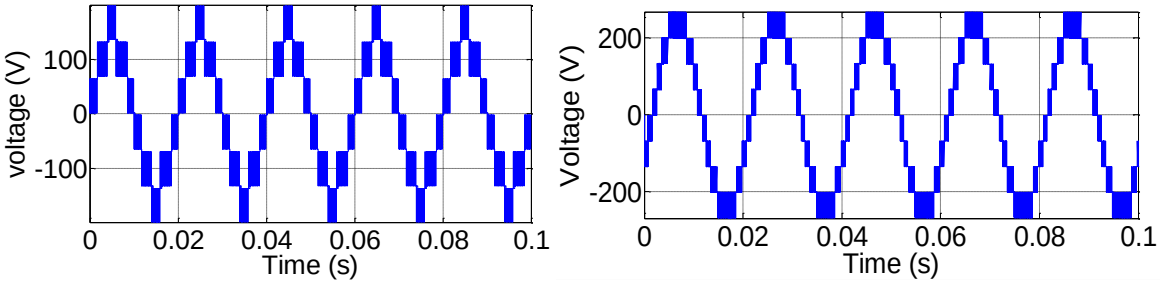
(b) 9 level line voltage MLI output

Five steps (or levels) are expected at the phase output of the five level MLI and 9 steps (2m-1) in the line output of the same MLI. Similarly, 7 steps in phase output and 13 steps in line output are expected for the 7 level MLI whilst 9 steps in phase output and 17 steps in line output are expected. Fig. 6-4, Fig. 6-5, and Fig. 6-6 confirm that the expected outputs are achieved.

6.2.2 Level Utilization outputs

Suppose the MI used is outside the nominal range, the levels or steps deteriorate and eventually are absorbed to produce less steps in the output waveform if the MI is smaller than a certain value. The minimum MI governs the operation of MLIs, with lower MI resulting in loss of intermediate voltage levels in the output waveform. This phenomenon is called Level Utilization. For example, in a seven level diode clamped inverter, the minimum MI allowed without losing any levels is 0,667. The minimum MI using multi-carrier based PWM is [41]

$$mi = \frac{m-3}{m-1} \tag{6.1}$$

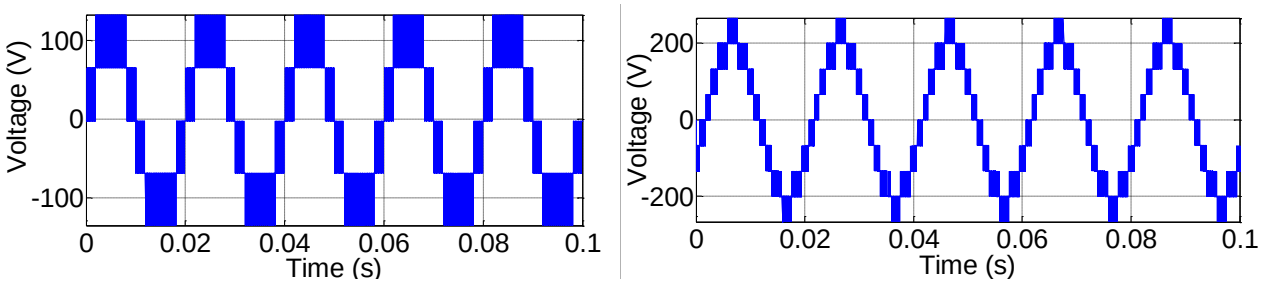


(a) (b)

Fig. 6-7: (a) distorted phase output from 7 level MLI

(b) line output from 7 level MLI with less Level Utilization

As mentioned before, Fig. **6-7** shows the output of the MLI when an MI of 0.7 is used. Notice that although the phase output still has 7 levels, the steps are already showing some deviations from the normal waveforms expected from a 7 level MLI. The topmost and bottommost levels have lost a bit of 'ON' time as they would have been ON for longer than the other switches considering the switching scheme used. It can be seen from the line output that some of the levels in the output have already been lost. Should the MI be reduced to a figure below the minimum MI, then even the phase output will be affected as shown in below.



(a) (b)

Fig. 6-8: (a) phase output from 7 level MLI with less level utilization

(b) line output from 7 level MLI with less level utilization

Fig. 6-8 shows the output shrinking to fewer levels because the MI has been allowed to go below the minimum MI allowable. Both the phase and line outputs have lost some levels and the effect of this is seen as making the output waveforms less sinusoidal-like.

6.2.3 Simulation outputs with load connected

The output waveforms from the MLI simulations are considered. For simplicity, the single phase or leg will be considered so as to match the hardware implementation.

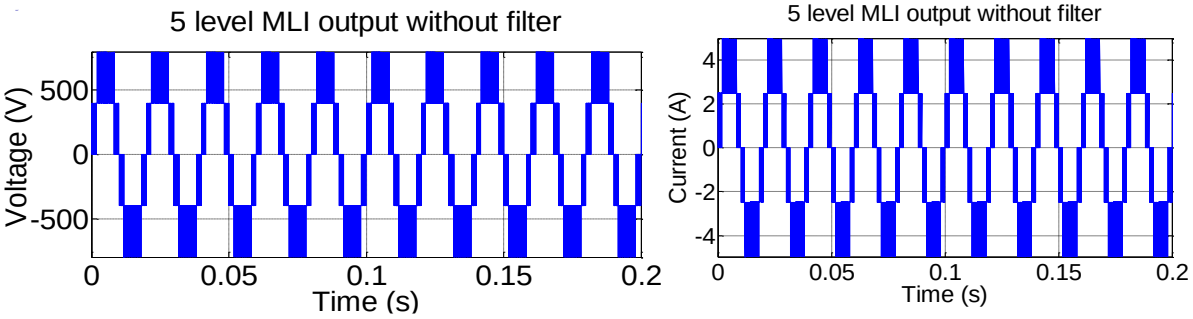


Fig. 6-9: five level MLI unfiltered output waveforms; left) voltage, right) current

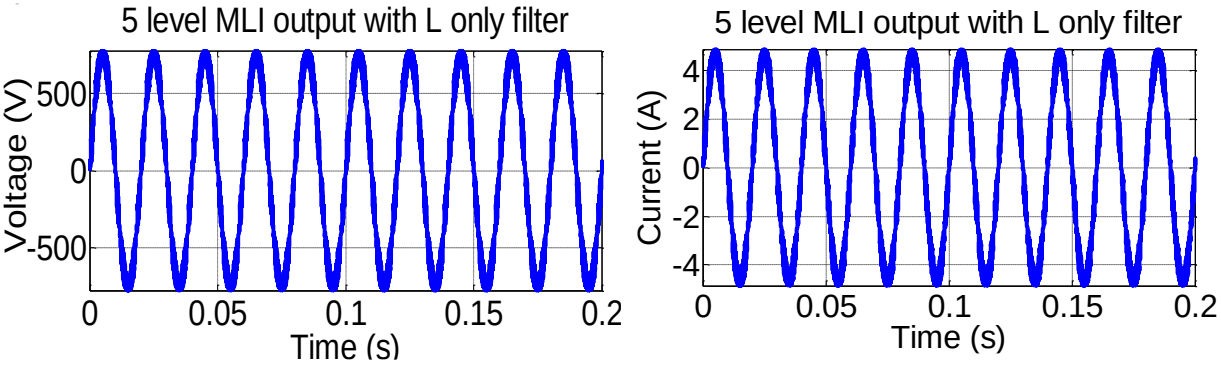


Fig. 6-10: five level MLI output waveforms with L filter; left) voltage, right) current

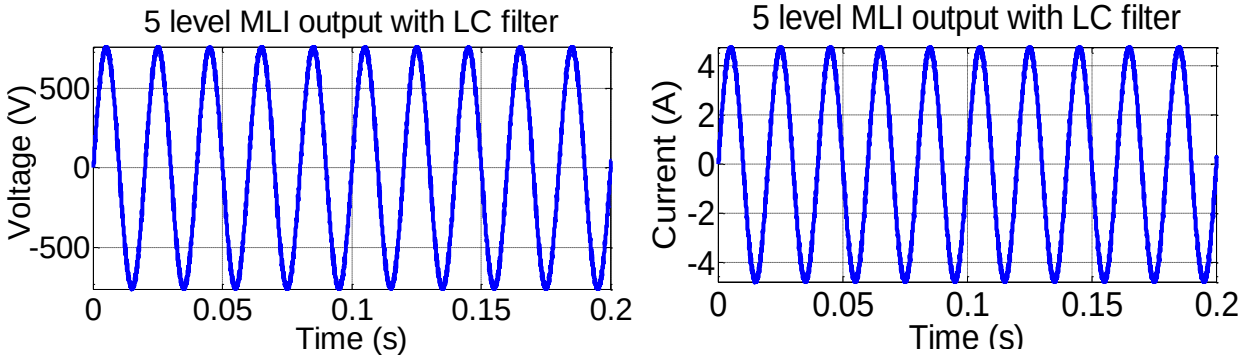


Fig. 6-11: five level MLI output waveforms with LC filter; left) voltage, right) current

Fig. 6-9 up to Fig. 6-11 shows the variation of the output voltage and current when there is no filter, filtering with an L only filter and lastly filtering with an LC filter. These figures shown above are

all for an MI of 0.95 and so the unfiltered phase voltage will show 5 steps for the five level MLI under consideration. The current waveform will follow the voltage in profile since the load is purely resistive. For completeness and to observe the effects of varying MI across the acceptable range in MLI, the results for the three level, seven level and nine level are recorded in the appendix section.
Fig. 11-12 up until Fig. 11-17 all show outputs for the three level inverter; the first figure shows output voltage without a filter connected whilst the second figure shows the output current when no filter is connected to the same 3 level MLI. Third and fourth figures show first the output voltage when an L only filter is connected to the 3 level MLI and secondly the output current when the same L only filter is connected to the three level MLI. Lastly, the last two figures are the voltage output waveform and current output waveform when using an LC filter.
The same format is done for getting the waveforms for the 7 level (Fig. 11-18 up until Fig. 11-23) and 9 level (Fig. 11-24 up until Fig. 11-29) MLI. The three level outputs are plotted in pink, five level in blue, 7 level in green and nine level in brown just to differentiate which set of results are being looked at.
To illustrate the effects of the MI on the filter, the following table is created. It focuses only on just one performance marker of each level of MLI, the filter size in H or F or both. In the creation of the table, only a small range in the values of the MI is used to ensure that there is complete level utilization. However, the simulations were done in the entire applicable MI range for each level with and without an output filter.

Table 6-1:THD variation with MI on different filters

		Without filter			L Only filter				LC Filter				
		THD%	V	A	L (mH)	THD%	V	A	L (mH)	C (μF)	THD%	V	A
3 level	0.8	77.1	636.2	4.0	130	2.6	617.5	3.9	3.3	12.8	2.2	639.5	4.0
	0.85	70.4	677.7	4.2		2.3	657.7	4.1			2.0	681.1	4.3
	0.9	64.6	715	4.5		2.1	693.8	4.3			2.5	718.5	4.5
	0.95	58.3	756	4.7		1.8	731.8	4.6			1.8	759.5	4.7
	1	52.5	794.8	4.9		1.7	771.2	4.8			1.8	798.4	5.0

		Without filter			L Only filter				LC Filter				
		THD%	V	A	L (mH)	THD%	V	A	L (mH)	C (μF)	THD%	V	A
5 level	0.8	38.4	634.9	4.0	60	2.7	631.1	3.9	1.8	7.0	3.0	635.8	4.0
	0.85	36.2	673.4	4.2	60	2.6	669.3	4.2	1.7	6.8	3.1	674.2	4.2
	0.9	33.6	713.3	4.5	50	2.8	710.5	4.4	1.7	6.6	2.8	714.2	4.5
	0.95	30.5	752.8	4.7	50	2.5	749.7	4.7	1.6	6.4	2.8	753.5	4.7
	1	27.1	761.6	4.9	50	2.2	788.3	4.9	1.6	6.3	2.6	792.3	5.0

		Without filter			L Only filter				LC Filter				
		THD%	V	A	L (mH)	THD%	V	A	L (mH)	C (μF)	THD%	V	A
7 level	0.8	24.4	632.1	4.0	40	2.6	630.5	3.9	1.5	5.7	2.8	632.5	4.0
	0.85	23.8	671.5	4.2	40	2.5	669.8	4.2	1.4	5.5	3.2	671.8	4.2
	0.9	22.5	710.2	4.4	40	2.4	708.4	4.4	1.4	5.4	3.0	710.6	4.4
	0.95	20.7	749.4	4.7	30	2.9	748.5	4.7	1.3	5.2	3.2	749.7	4.7

	1	18.3	788.1	4.9	30	2.5	787.1	4.9	1.3	5.1	3.0	788.4	4.9

		Without filter			L Only filter				LC Filter				
		THD%	V	A	L (mH)	THD%	V	A	L (mH)	C (μF)	THD%	V	A
9 level	0.8	17.3	629.4	3.9	30	2.3	628.6	3.9	1.2	4.9	3.2	629.5	3.9
	0.85	17.2	668.1	4.2	30	2.4	667.2	4.2	1.2	4.8	3.3	668.2	4.2
	0.9	16.8	707.2	4.4	30	2.4	706.3	4.4	1.2	4.7	3.3	707.3	4.4
	0.95	15.7	745.6	4.7	30	2.2	744.7	4.7	1.2	4.5	3.3	745.7	4.7
	1	13.8	784.3	4.9	30	1.9	783.3	4.9	1.1	4.4	3.4	784.3	4.9

Table 6-1 above shows the variation of THD and how the filter components changes when MI is varied.

6.3 Hardware output

When the 5 level CHB-MLI was being set up, there were numerous challenges that were experienced such as having to put isolating transformers on the inputs of the DC batteries. This was because at times two halves of the 5 level CHB-MLI would work separately but not when put together. This then is interpreted as either the switching of both CHB cells interfering with each other (which it was at first whilst using bipolar switching technique) or that the independent DC cells may not be properly isolated (which could have been because they were charging from the same controller and one mains supply which may have a common ground). Thus at first only the three level output voltage and current waveforms were realised.

After using isolating transformers on the output of the DC batteries, the CHB cells started working properly; producing 3 levels individually and the required five levels when cascaded. The outputs are shown in figures below.

Fig. 6-12 shows output from one of the two cells that make up the 5 level CHB-MLI. As expected, the waveform has three distinct levels. The outputs from both CHB-MLI cells are shown alongside each other in Fig. 6-13. It should be noted that the components used had some tolerances associated with them and the lengthy wires used introduced interferences and probably also picked up noise from nearby machines. Shortening the connecting wires from the cells, tightening all connections and properly grounding the ground signals of the level shifting circuit through a separate metallic plate ‘cleaned’ the signals and hence the outputs from the two cells to produce a better looking output as shown by Fig. 6-14. Depending on how clean the signals are transmitted, various imperfections could be seen in the output as illustrated by Fig. 6-15.

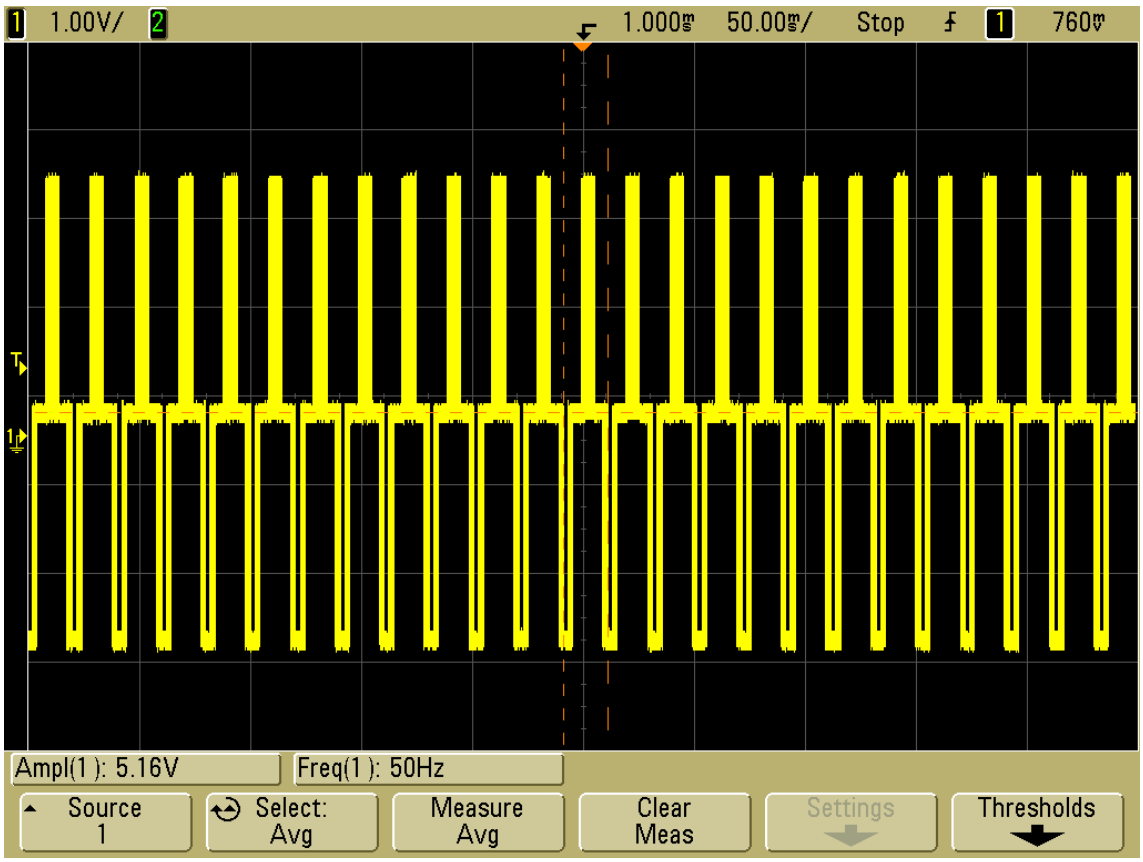


Fig. 6-12: three level output from half of the CHB-MLI

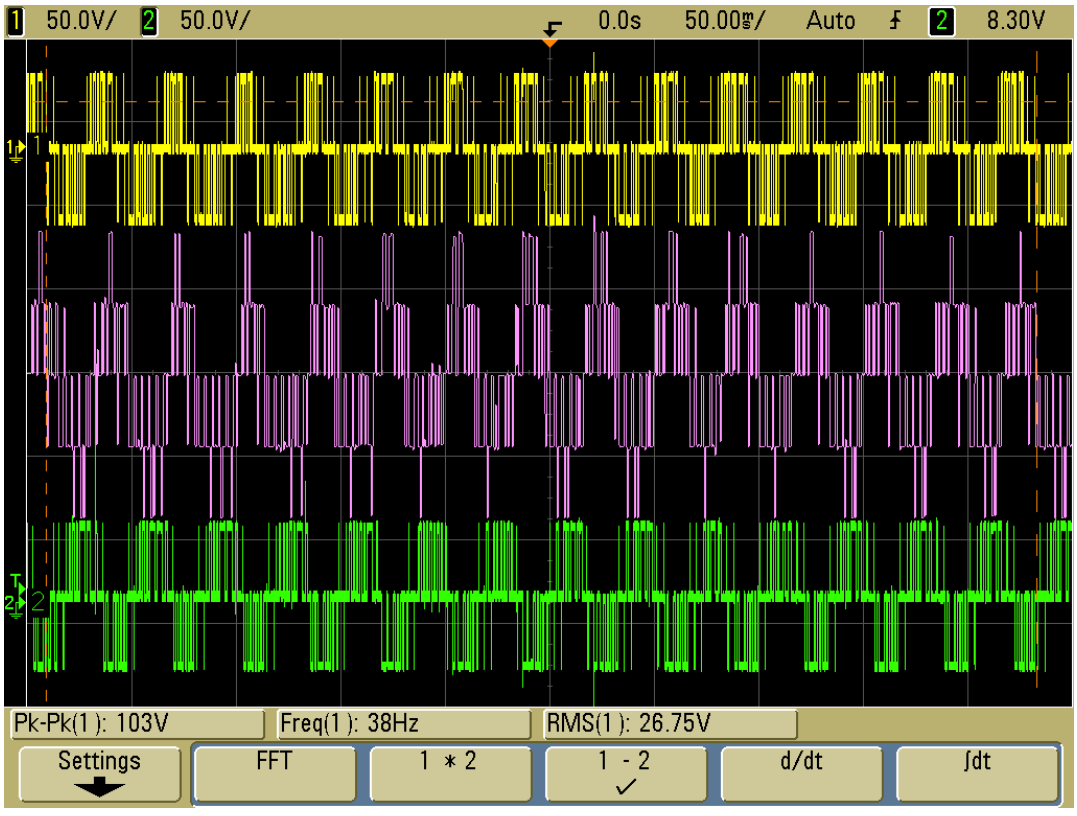


Fig. 6-13: output of two CHB cells cascaded to produce the five level MLI output

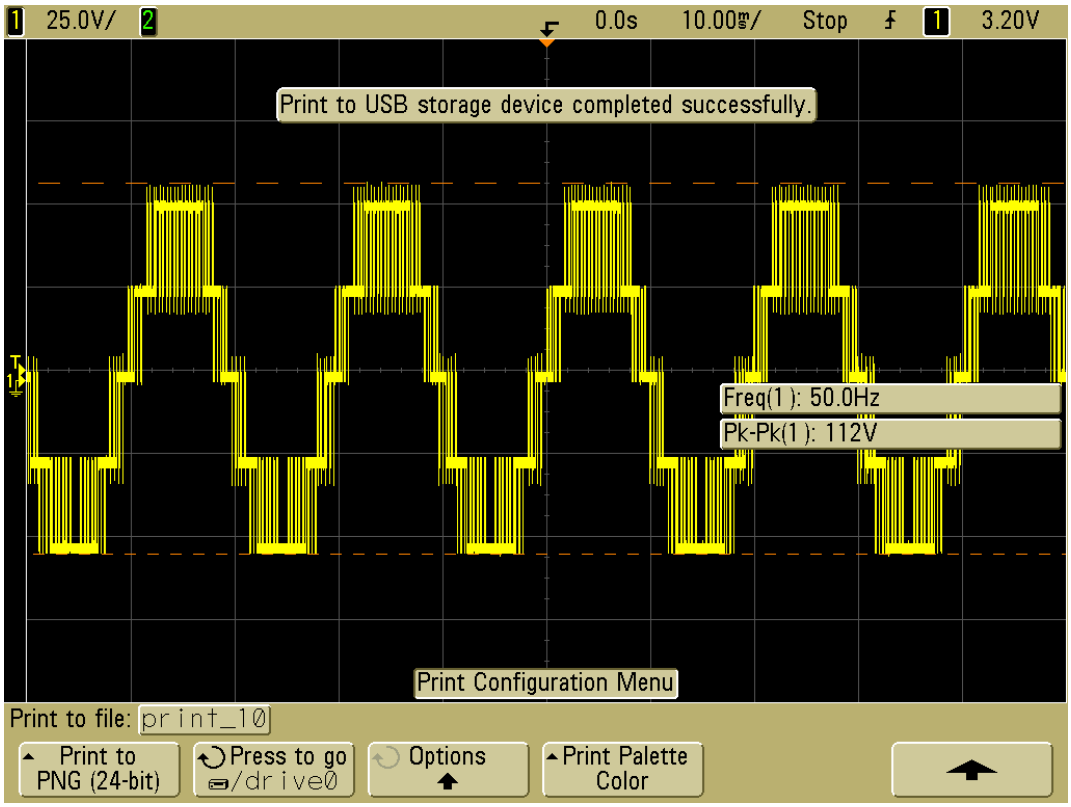


Fig. 6-14: proper unfiltered 5 level output from VSI

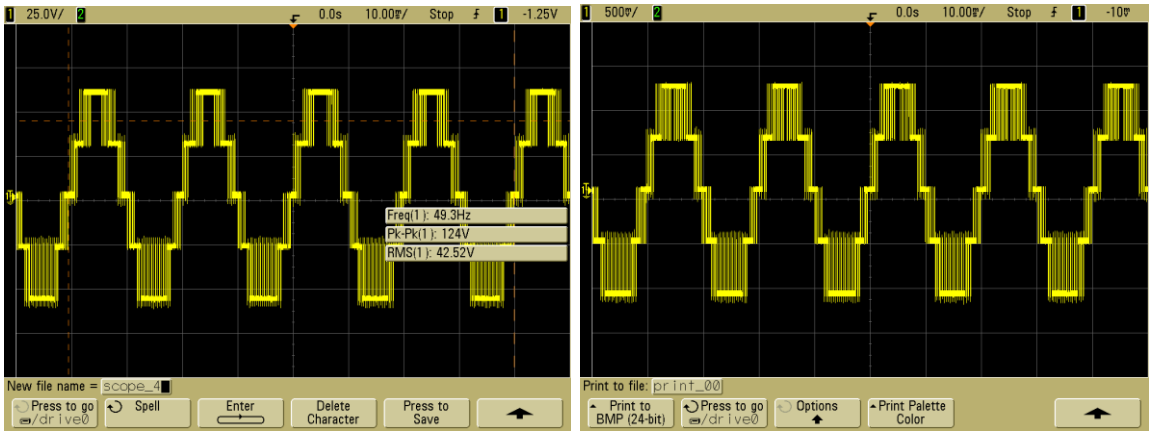


Fig. 6-15: unfiltered 5 level output; left) with interference, right) using cleaner outputs

6.3.1 Calculation of harmonics from VSI hardware

The calculation of harmonics is straightforward when done in software. This is because most software such as Simulink has ways of manipulating the data or extracting it from plots and with just a simple command, they can calculate things like the nth harmonic and THD. However, it becomes complicated to do in hardware as most available oscilloscopes such as the one used in this research does not have the function of doing power analysis at this level. The best way forward will be to save the plots manually as comma separated files (CSV) format which automatically saves the plots of x and y plots time stamped and with a very high resolution. This gives the ability to

calculate manually what the harmonics were and what the THD of the voltage or current waveform is.
With the x and y values extracted from the plots, a simple command line function exists in MATLAB which can be applied here. Here is the 'thd' function for calculating the percentage THD:

>>>//matlab command line// a = thd (y, f_s, n) //end of function

The function takes in the y values from the x-y plots, needs switching frequency f_s and n the number of harmonics needed to be calculated from the x-y plot.
The result given out will be a decibels that is units are dB.
To convert from dB to normal percentage, first convert output to a power ratio x, then afterwards take the root of x to get the amplitude ratio, which will be a decimal or multiply by 100 to convert to percentage.

For example, if dB value is -10, then power ratio x value will be the value of x from the logarithmic equation:

$$10\log x = -10$$
$$10^{\log x} = 10^{-1}$$
$$\log x = -1$$
$$x = 10^{-1}$$

Therefore x=0.1. from this, the amplitude ratio is taken as the root of the power ratio x. so the amplitude will be root of 0.1 which is 0.3162.. or 31.62% as the THD.

6.3.2 Filter results

When a 25.5V DC bus is connected to each H bridge module in a five level VSI, and a load whose resistive value is 160 ohms, a 16.4mH inductor and a 0.64µF capacitor are required for filtering according to (5.3) and (5.4). Doing a Fast Fourier Transform (FFT) on a waveform in Simulink will give the frequency spectrum of the waveform or the amount and location of individual harmonics. The current flowing in the load has the harmonic spectrum shown on left before filtering and on right after filtering in Fig. 6-16.

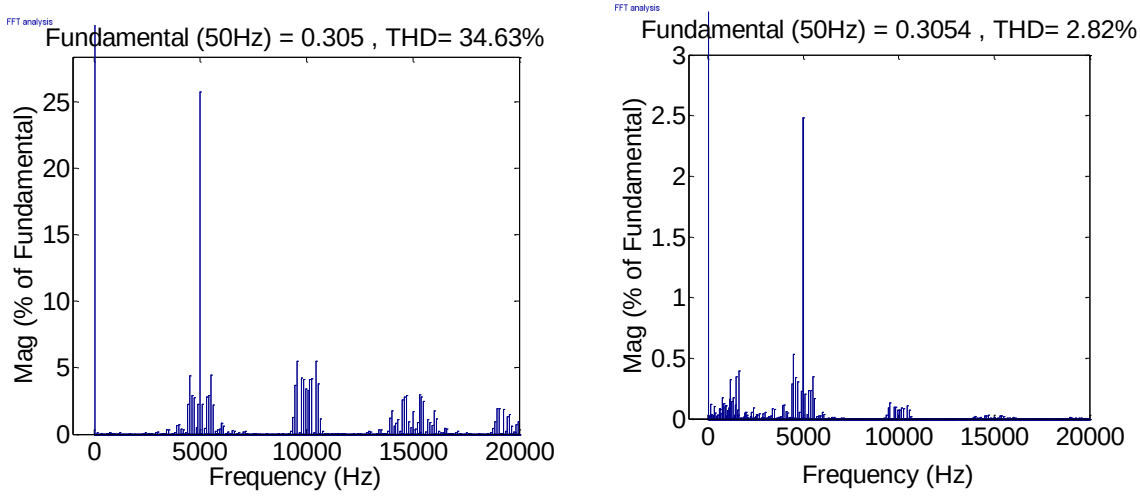


Fig. 6-16: fft of output waveforms; left) unfiltered, right) filtered

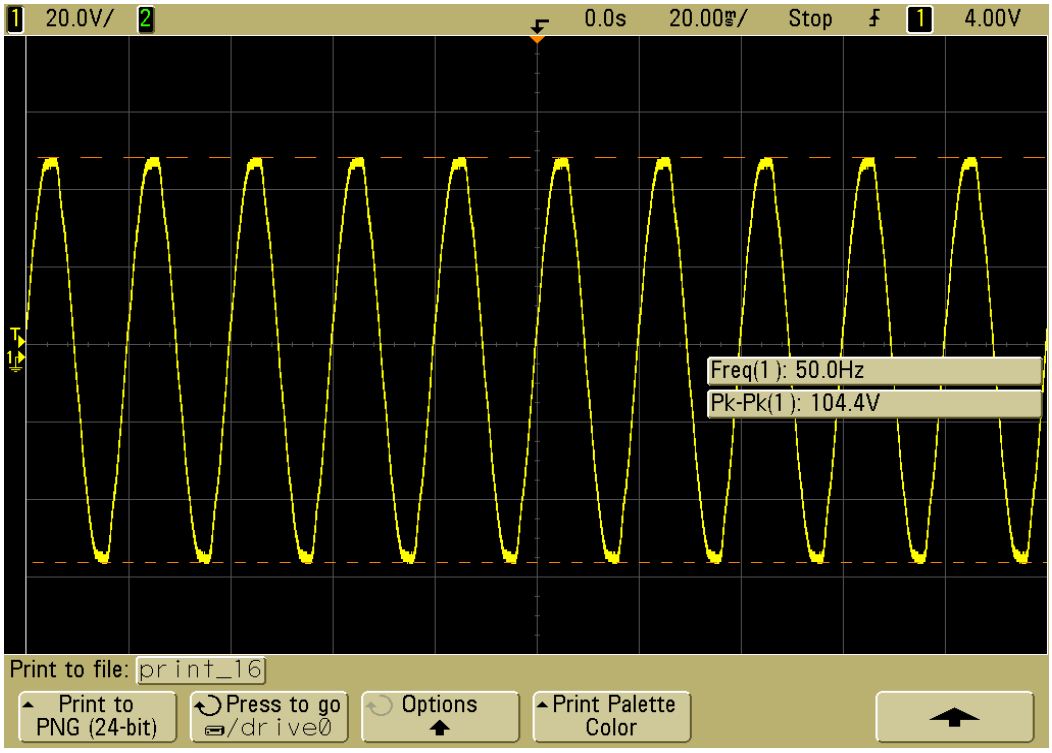


Fig. 6-17: filtered output from 5 level VSI with LC filter

The above figure shows a smooth sinusoidal output from the filtering action of an LC filter on the output of a five level CHB-MLI. The frequency spectrum in Fig. 6-16 shows that the THD is indeed less than 5% but does not show individual harmonics values hence a need arises again to further do another FFT analysis to check them. This is shown in Fig. 6-18 below.

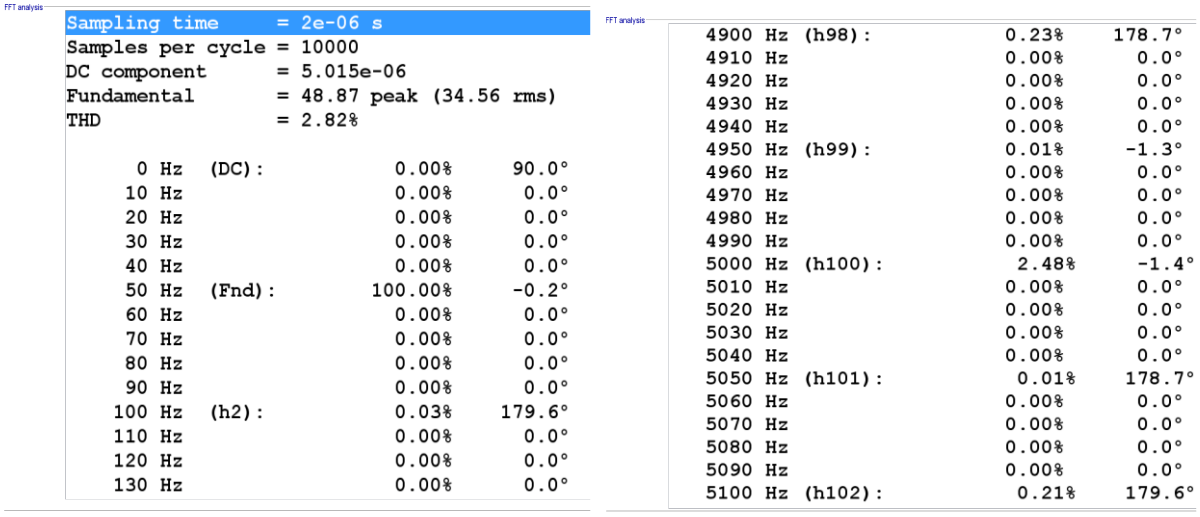


Fig. 6-18: fft analysis of filtered output to show individual harmonics

Fig. 6-18 above shows parts of the harmonics spectra until the 102nd harmonic. It can be seen that none of the individual harmonics are greater than 3% hence the IEEE std 519 rules are not violated.

6.4 Harmonics prediction outputs

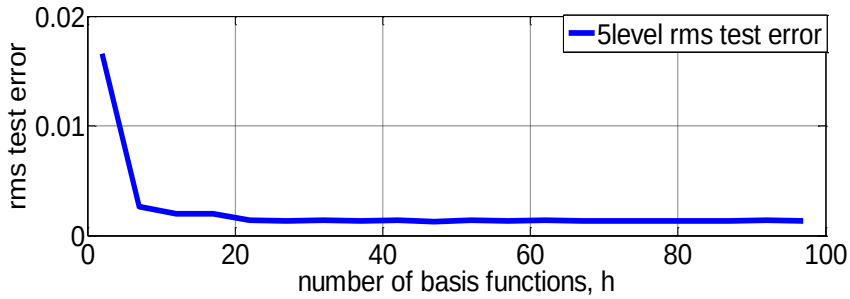


Fig. 6-19: 5 level rms test error for number of basis function selection

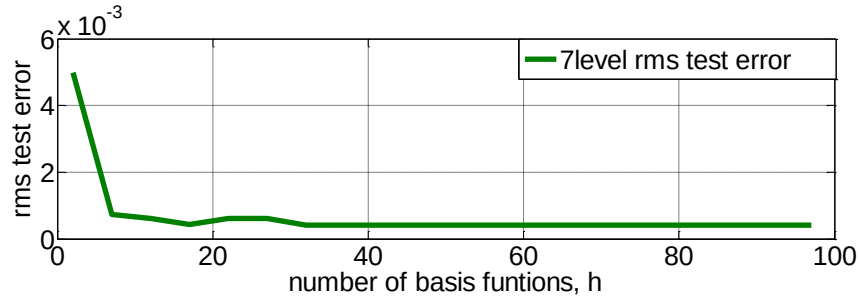


Fig. 6-20: 7 level rms test error for number of basis function selection

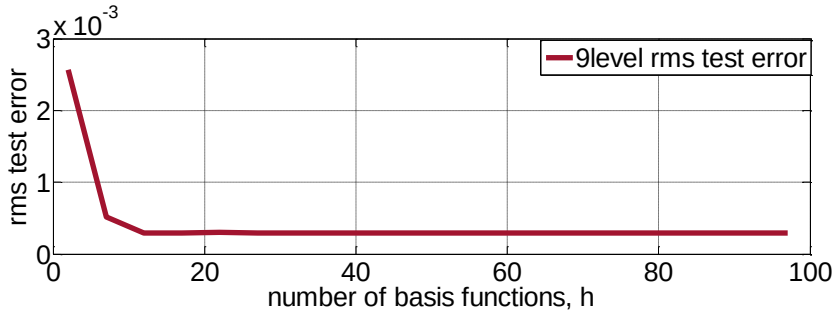


Fig. 6-21: 9 level rms test error for number of basis function selection

The above figures show how many basis functions would be ideal for each of the 5, 7 and 9 level topologies. Since the functions being looked at are not varying too randomly, a small number of basis functions (less than 20) is adequate to use for prediction. In other words, the rms test error shows the variation in accuracy as different number of basis functions are used.

When the number of basis functions is decided using the above reasoning, running the simulations and predicting the THD will result in numbers which closely foretell how much THD is expected with high accuracy. This is illustrated below.

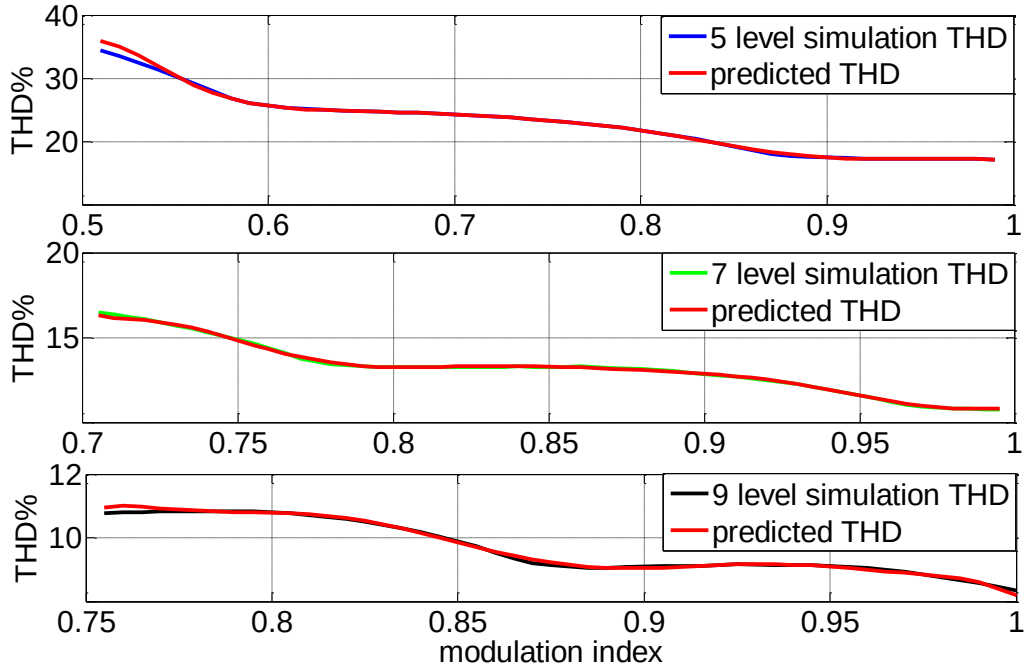


Fig. 6-22: predicted vs simulation results for five, seven and nine level VSIs

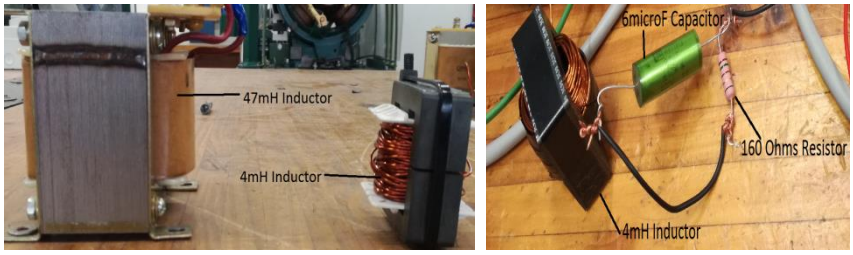


Fig. 6-23: L and LC filter components differences in size

The figure above the simulated vs predicted waveforms for the five, seven and the nine level MLIs. Since the test error was very small and the number of basis functions used more than adequate (an h of 100 was used as the computational resources allowed!) the plots show that the predictions were within very close range to the simulated results. This is when 20% of the data is used for training and the rest used for testing showing marked improvements from the authors which applied similar techniques to their harmonics predictions.

7. Discussion

It has been seen from the results how well the simulations are representing what actually happens in hardware. A look at some of the results already given before but side by side will further strengthen this view. Beginning with the unfiltered five level output, the hardware and software results are compared below.

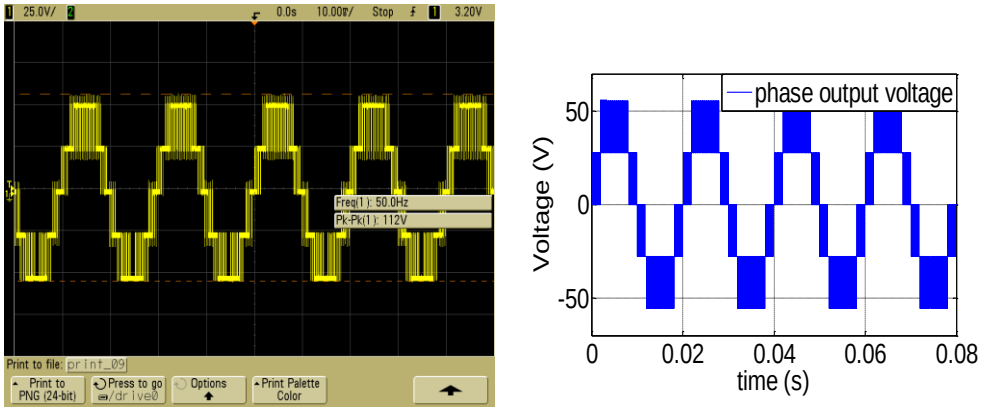


Fig. 7-1: five level VSI vs software unfiltered results

From Fig. 7-1, it can be seen that the hardware results closely resemble the software simulation results. The peak to peak output shown from the VSI is 112V as the oscilloscope measures peak to peak of the signal, not of the fundamental which will be slightly less (sinusoidal component is about 102V peak-peak). Applying the method of filter design from the filtering section, the following outputs are observed.

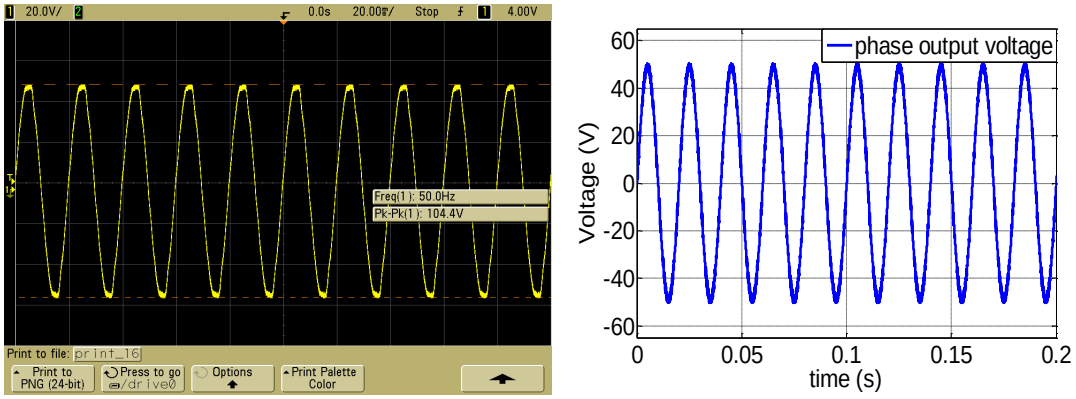


Fig. 7-2: LC filtered output from 5 level VSI and software

The output from the VSI in figure above again is the same as the expected output from simulation and the THD is found to be within the allowed range.

In interpreting results for the unfiltered signals, the fundamental signal of the stepped waveforms is assumed to be an equivalent sinusoidal, hence the peak fundamental recorded on scope and calculated by Simulink will be slightly different.
To compare how simulations relate to practical hardware, a table with measurements of peak values of voltage and current taken from both is shown below.

Table 7-1: hardware and software results comparison for filtered and unfiltered VSI outputs

	Without filter			LC Filter		
	THD%	V_{pk}	A_{pk}	THD%	V_{pk}	A_{pk}
simulink	34.6	48.8	0.3	2.8	48.9	0.3
hardware	35.9	52.2	0.3	3.0	52.2	0.3

Before filtering, the THD differed by 1.3% whilst after filtering the difference dropped to 0.2%. The measured voltage is slightly different (by about 3V) probably due to the tolerances on the measurement device (differential probe) and in the inductor values.
The results section has shown that more levels means less THD and harmonics, and that some switching techniques may be slightly advantageous is certain circumstances, how the CHB-MLI is advantageous when it comes to the output voltage or current values when compared to the other topologies.
The filtering exercise has shown that a good filter can be designed just by following a few basic principles and not designing from scratch when tolerances of the filter values required are not tight.
With regards to prediction, the results achieved by applying the techniques of the harmonics prediction section prove with a good design of the number of basis functions, a very close and accurate prediction of the THD and harmonics in the output waveforms can be made.

8. Conclusions

The aim of this paper was to compare and contrast the basic multilevel inverter topologies. It has illustrated how to implement each topology from gate signal generation to assigning of the signals to the individual gates. A description of how the gates should be controlled has been given, with the DC-MLI and CC-MLI showing similarities in both structure and switching pattern. Only in the switching sequence did the two topologies differ slightly. The CHB-MLI is different in the way it is built and also in the way it is switched. Requiring separate DC sources has been shown to be a disadvantage of the CHB-MLI but the uses in renewable energy sources or when a center tapping transformer is available has shown that the CHB-MLI is the topology of choice in these applications with added advantages such as distributed control, modularity and better voltage output (quantity wise) when compared to the other two topologies. The advantage of distributed control has been illustrated in hardware especially when controlling or balancing individual cells of the CHB-MLI.
Comparison of the PWM schemes confirmed that PD-PWM produces the least THD as expected from theory.
It was confirmed that machine learning can be used to predict harmonics within a system even with very limited data (both for testing and training). By using 20% of the collected simulation data, machine learning algorithm was successfully employed and proved to be able to save time in estimating the variation of THD with MI, as the predictions were very accurate.
In this sense, time is saved if a designer is trying to fine tune the inverter's operating parameters (range of applicable MI, output voltage), or when trying to choose which level of MLIs to use from the infinite number of levels possible.
Lastly it was shown that more levels reduce the size of the filter components and also produces higher output voltage with fewer distortions than a similarly rated inverter with a lower level count.

9. Further work

This paper has shown how MLIs can be used both for reducing harmonics and filter components size and costs. It also provided a walkthrough on how to design an L only filter or LC filter that suites most designs without much hassle. It has been shown that as little as 20% of the data collected in machine learning can be used for training, with the rest being used for testing. Using more training data basically points to a less intelligent predictor as many simulations need to be done to collect the data to train the prediction algorithm.

There is still work that can be done especially in filter designs suitable for both grid connected or off-grid systems. Most authors either look into the physical side of the filter design such as materials, gaps in capacitors, dimensions, heating or cooling properties etc, or look into the frequency response and attenuation of the filter to meet their needs theoretically. However, very few look into both. It may also be recommended to use DC sources which are being charged independently from renewable sources. This project used DC sources which were separate but were charging from the same mains supply. This caused valuable time to be lost that may have been used elsewhere in this project.

The prediction algorithm had to be trained whenever the number of levels are changed, ie, a five level predictor only worked for 5 level predictions. The prediction algorithm trained with five level data would not work properly to predict harmonics from a seven level MLI. A prediction algorithm that can be trained only once to work on all levels would be a wonderful improvement.

10. References

[1] D. Ahmadi *et al*, "A universal selective harmonic elimination method for high-power inverters," *IEEE Transactions on Power Electronics,* vol. 26, *(10),* pp. 2743-2752, 2011.

[2] N. Anani *et al*, "Prediction of line current harmonics in an AC-DC converter using neural networks," in *Industrial Electronics & Applications (ISIEA), 2010 IEEE Symposium on,* 2010, pp. 66-69.

[3] M. F. Arman, *An'Active'Passive-Filter Topology for Low Power DC/AC Inverters,* 2011.

[4] C. R. Balamurugan *et al*, "A Review on Modulation Strategies of Multi Level Inverter," *Indonesian Journal of Electrical Engineering and Computer Science,* vol. 3, *(3),* pp. 681-705, 2016.

[5] J. Balcells *et al*, "Influence of data resolution in nonlinear loads model for harmonics prediction," in *Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE,* 2016, pp. 6560-6565.

[6] H. Belkamel *et al*, "Novel three-phase asymmetrical cascaded multilevel voltage source inverter," *IET Power Electronics,* vol. 6, *(8),* pp. 1696-1706, 2013.

[7] Y. Birbir, H. S. Nogay and S. Taskin, "Prediction of current harmonics in induction motors with artificial neural network," in *Electrical Machines and Power Electronics, 2007. ACEMP'07. International Aegean Conference on,* 2007, pp. 707-711.

[8] D. S. Braga and P. R. Jota, "Prediction of total harmonic distortion based on harmonic modeling of nonlinear loads using measured data for parameter estimation," in *Harmonics and Quality of Power (ICHQP), 2016 17th International Conference on,* 2016, pp. 454-459.

[9] B. Cao, L. Chang and R. Shao, "A simple approach to current THD prediction for small-scale grid-connected inverters," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE,* 2015, pp. 3348-3352.

[10] I. Colak, E. Kabalci and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management,* vol. 52, *(2),* pp. 1114-1128, 2011.

[11] P. J. Crawley and G. W. Roberts, "Predicting harmonic distortion in switched-current memory circuits," *IEEE Trans. Circuits Syst. II Analog Digital Signal Process.,* vol. 41, *(2),* pp. 73-86, 1994.

[12] S. Daher, J. Schmid and F. L. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.,* vol. 55, *(7),* pp. 2703-2712, 2008.

[13] de Almeida Cacau, Ronny Glauber *et al*, "Five-Level T-Type Inverter Based on Multistate Switching Cell," *IEEE Trans. Ind. Appl.,* vol. 50, *(6),* pp. 3857-3866, 2014.

[14] B. L. Dokić and B. Blanuša, *Power Electronics.* Springer, 2015.

[15] E. C. Dos Santos and Cabral da Silva, Edison Roberto, "Three-Phase to Three-Phase and other Back-to-Back Converters," *Advanced Power Electronics Converters: PWM Converters Processing AC Voltages,* pp. 324-346, .

[16] Z. Du *et al*, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Transactions on Power Electronics,* vol. 24, *(1),* pp. 25-33, 2009.

[17] L. G. Franquelo *et al*, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine,* vol. 2, *(2),* 2008.

[18] Y. Guo, J. Zhu and M. R. Islam, *Power Converters for Medium Voltage Networks.* Springer, 2014.

[19] D. Huang *et al*, *Advanced Intelligent Computing Theories and Applications. with Aspects of Artificial Intelligence: Fourth International Conference on Intelligent Computing, ICIC 2008 Shanghai, China, September 15-18, 2008, Proceedings.* Springer, 2008*5227*.

[20] G. Huang, "An insight into extreme learning machines: random neurons, random features and kernels," *Cognitive Computation,* vol. 6, *(3),* pp. 376-390, 2014.

[21] G. Huang, L. Chen and C. K. Siew, "Universal approximation using incremental constructive feedforward networks with random hidden nodes," *IEEE Trans. Neural Networks,* vol. 17, *(4),* pp. 879-892, 2006.
[22] G. Huang, Q. Zhu and C. Siew, "Extreme learning machine: theory and applications," *Neurocomputing,* vol. 70, *(1),* pp. 489-501, 2006.
[23] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on Power Electronics,* vol. 21, *(1),* pp. 140-147, 2006.
[24] P. Kala and S. Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications," *Renewable and Sustainable Energy Reviews,* vol. 76, pp. 905-931, 2017.
[25] N. Karnik, D. Singla and P. Sharma, "Comparative analysis of harmonic reduction in multilevel inverter," in *Power India Conference, 2012 IEEE Fifth,* 2012, pp. 1-5.
[26] V. Karthikeyan, V. Vijayalakshmi and P. Jeyakumar, "Selective Harmonic Elimination (SHE) for 3-Phase Voltage Source Inverter (VSI)," *American Journal of Electrical and Electronic Engineering,* vol. 2, *(1),* pp. 17-20, 2014.
[27] H. Ke and W. Li, "Extreme learning machine-based stable adaptive control for a class of nonlinear system," in *Control and Decision Conference (2014 CCDC), the 26th Chinese,* 2014, pp. 387-391.
[28] M. Lamich *et al*, "Non linear Loads Model for Harmonics Flow Prediction, Using Multivariate Regression," *IEEE Trans. Ind. Electron.,* 2017.
[29] K. Lee and K. E. Willcox, "Structural integrity assessment via structural response predictions using a certified reduced basis model," in *54th AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics, and Materials Conference,* 2013, pp. 1625.
[30] S. Lee, P. Fajri and M. Ferdowsi, "A robust hybrid multilevel rectifier with adjustable output voltage and variable load," in *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on,* 2015, pp. 14-20.
[31] J. Lu *et al*, "Harmonic balance method used for harmonics calculation and prediction in power systems," in *Power Engineering Conference (AUPEC), 2016 Australasian Universities,* 2016, pp. 1-6.
[32] S. Mariéthoz, "Systematic design of high-performance hybrid cascaded multilevel inverters with active voltage balance and minimum switching losses," *IEEE Transactions on Power Electronics,* vol. 28, *(7),* pp. 3100-3113, 2013.
[33] A. Massoud, S. Finney and B. Williams, "High-power, high-voltage IGBT applications: series connection of IGBTs or multilevel converters?" *International Journal of Electronics,* vol. 90, *(11-12),* pp. 763-778, 2003.
[34] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.,* vol. 49, *(4),* pp. 858-867, 2002.
[35] A. Namboodiri and H. S. Wani, "Unipolar and bipolar PWM inverter," *International Journal for Innovative Research in Science & Technology,* vol. 1, *(7),* pp. 237-243, 2014.
[36] Y. Park, J. Yoo and S. Lee, "Practical implementation of PWM synchronization and phase-shift method for cascaded H-bridge multilevel inverters based on a standard serial communication protocol," *IEEE Trans. Ind. Appl.,* vol. 44, *(2),* pp. 634-643, 2008.
[37] M. A. Perez and S. Kouro, "Asymmetric cascaded converter for solar PV applications," in *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on,* 2014, pp. 2484-2489.
[38] A. Prayag and S. Bodkhe, "A comparative analysis of classical three phase multilevel (five level) inverter topologies," in *Power Electronics, Intelligent Control and Energy Systems (ICPEICES), IEEE International Conference on,* 2016, pp. 1-5.
[39] P. Rajeevan *et al*, "A seven-level inverter topology for induction motor drive using two-level inverters and floating capacitor fed H-bridges," *IEEE Transactions on Power Electronics,* vol. 26, *(6),* pp. 1733-1740, 2011.

[40] S. N. Rao, D. A. Kumar and C. S. Babu, "New multilevel inverter topology with reduced number of switches using advanced modulation strategies," in *Power, Energy and Control (ICPEC), 2013 International Conference on,* 2013, pp. 693-699.
[41] M. H. Rashid, Ed., *Power Electronics Handbook: Devices, Circuits and Applications.* (3rd edition ed.) Burlington, United States of America: Elsevier, 2011.
[42] J. Rodriguez *et al*, "Matrix converter controlled with the direct transfer function approach: analysis, modelling and simulation," *International Journal of Electronics,* vol. 92, *(2),* pp. 63-85, 2005.
[43] J. Rodway *et al*, "Prediction of PV power quality: Total harmonic distortion of current," in *Electrical Power & Energy Conference (EPEC), 2013 IEEE,* 2013, pp. 1-4.
[44] Z. Rymarski, "The discrete model of the power stage of the voltage source inverter for UPS," *International Journal of Electronics,* vol. 98, *(10),* pp. 1291-1304, 2011.
[45] Z. Rymarski and K. Bernacki, "Different approaches to modelling single-phase voltage source inverters for uninterruptible power supply systems," *IET Power Electronics,* vol. 9, *(7),* pp. 1513-1520, 2016.
[46] Y. Song, J. Crowcroft and J. Zhang, "Automatic epileptic seizure detection in EEGs based on optimized sample entropy and extreme learning machine," *J. Neurosci. Methods,* vol. 210, *(2),* pp. 132-146, 2012.
[47] J. Steele and G. Vinnicombe, "The ν-gap metric and the generalised stability margin," in *Advanced Techniques for Clearance of Flight Control Laws*Anonymous Springer, 2002, pp. 57-75.
[48] R. P. Vishvakarma, S. Singh and T. Shukla, "Multilevel inverters and its control strategies: A comprehensive review," in *Power, Control and Embedded Systems (ICPCES), 2012 2nd International Conference on,* 2012, pp. 1-9.
[49] L. Wang *et al*, "Ground Leakage Current Analysis a Suppression in a 60-kW 5-Level T-Type Transformerless SiC PV Inverter," *IEEE Transactions on Power Electronics,* vol. 33, *(2),* pp. 1271-1283, 2018.
[50] J. Wu *et al*, "Novel power electronic interface for grid-connected fuel cell power generation system," *Energy Conversion and Management,* vol. 71, pp. 227-234, 2013.
[51] R. Yadav, P. Bansal and A. R. Saxena, "A three-phase 9-level inverter with reduced switching devices for different PWM techniques," in *Power India International Conference (PIICON), 2014 6th IEEE,* 2014, pp. 1-6.
[52] C. Yeu *et al*, "A new machine learning paradigm for terrain reconstruction," *IEEE Geoscience and Remote Sensing Letters,* vol. 3, *(3),* pp. 382-386, 2006.
[53] Blake, Carl & Bull, " IGBT or MOSFET: Choose Wisely. ." *Chris & Rectifier, International.* (2018)

11. Appendices

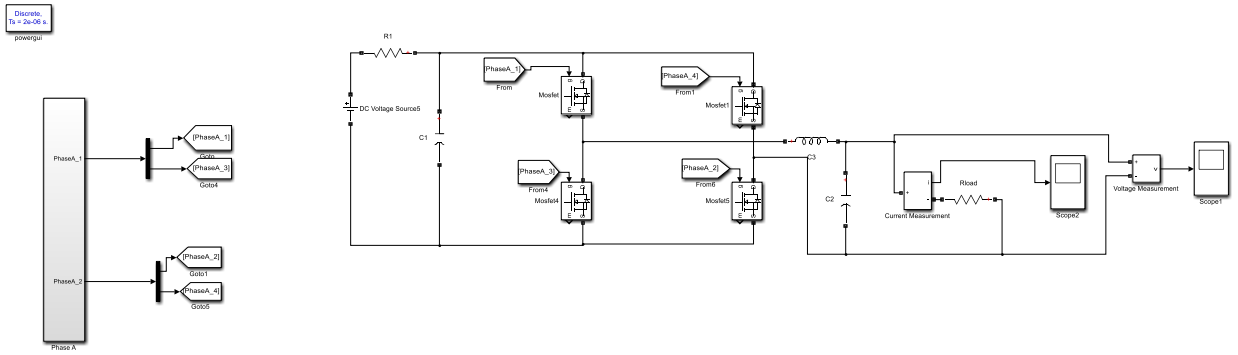


Fig. 11-1: single phase 3 level CHB-MLI.

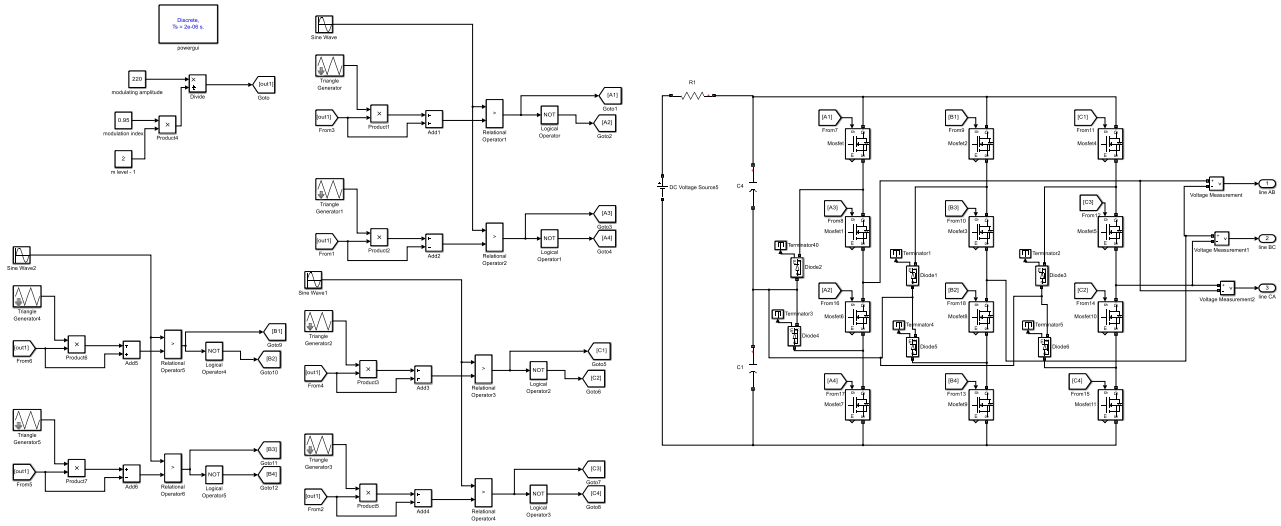


Fig. 11-2: three phase 3 level DC-MLI

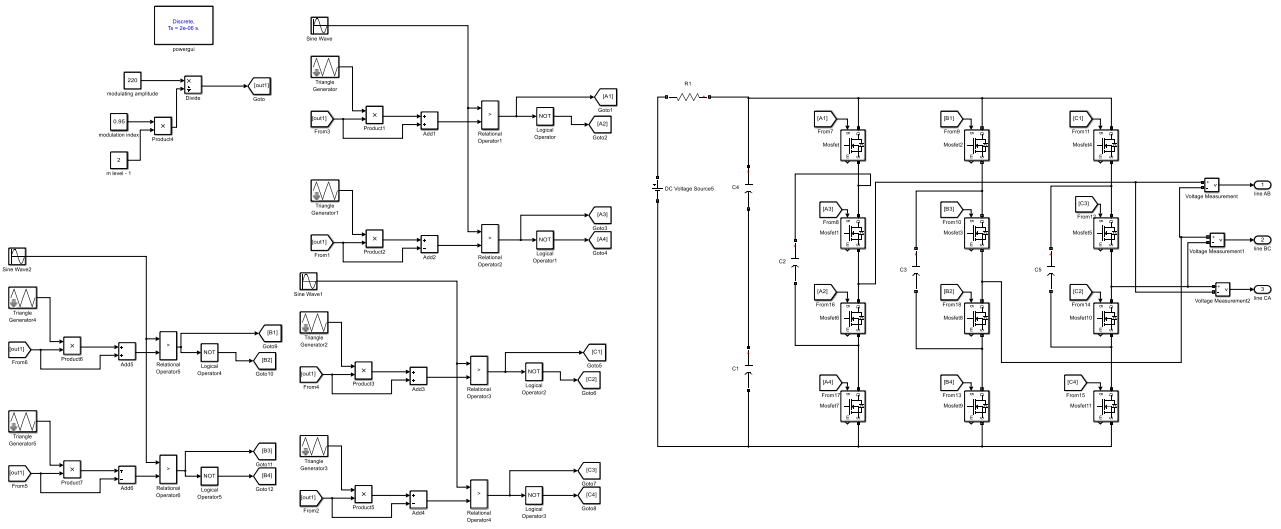


Fig. 11-3: three phase 3 level CC-MLI

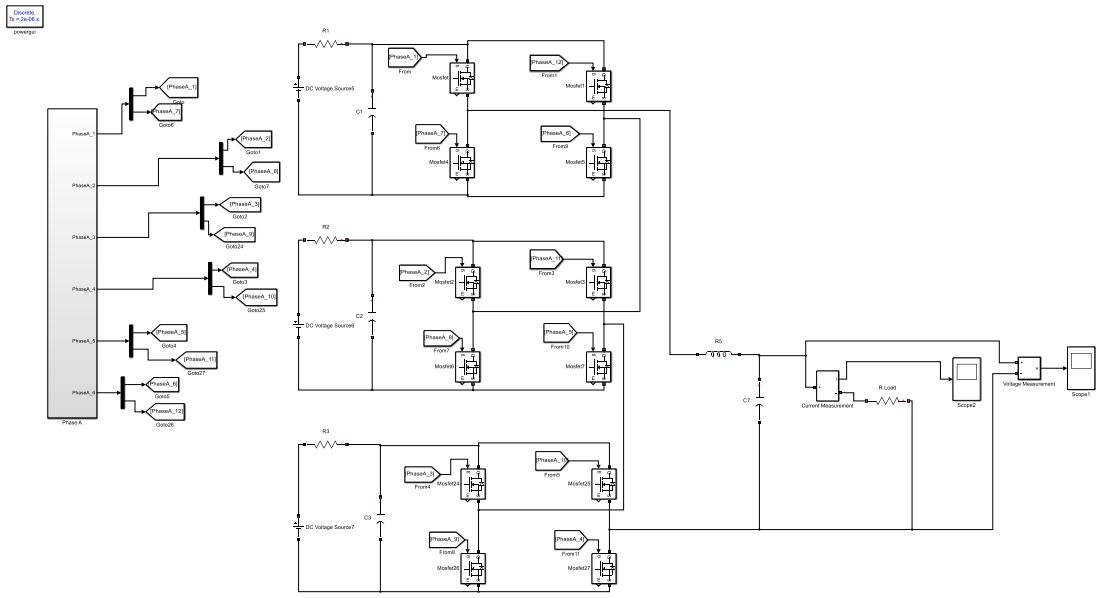


Fig. 11-4: single phase 7 level CHB-MLI

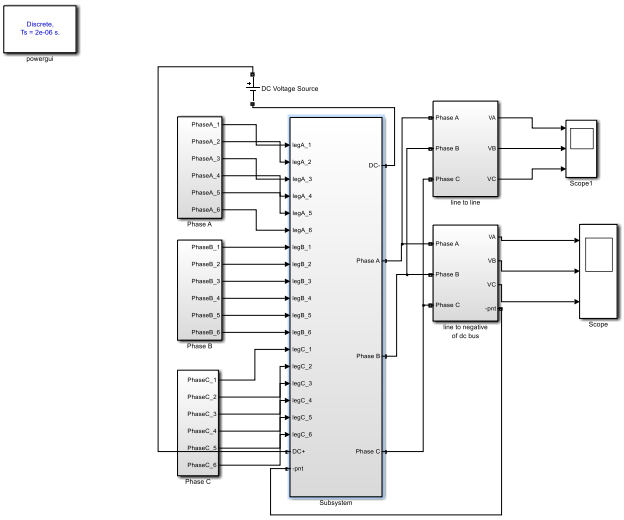


Fig. 11-5: three phase 7 level DC-MLI subsystem blocks

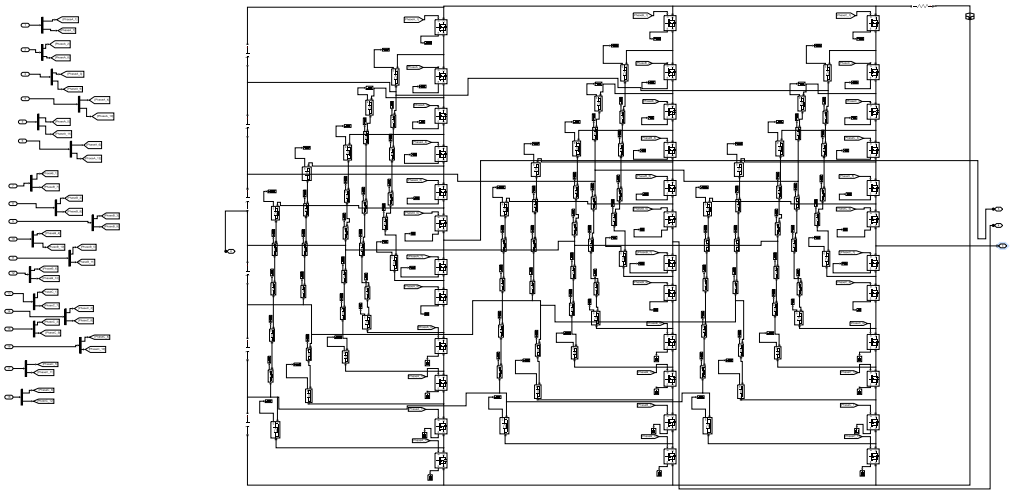


Fig. 11-6: Switches' connections for a three phase 7 level DC-MLI

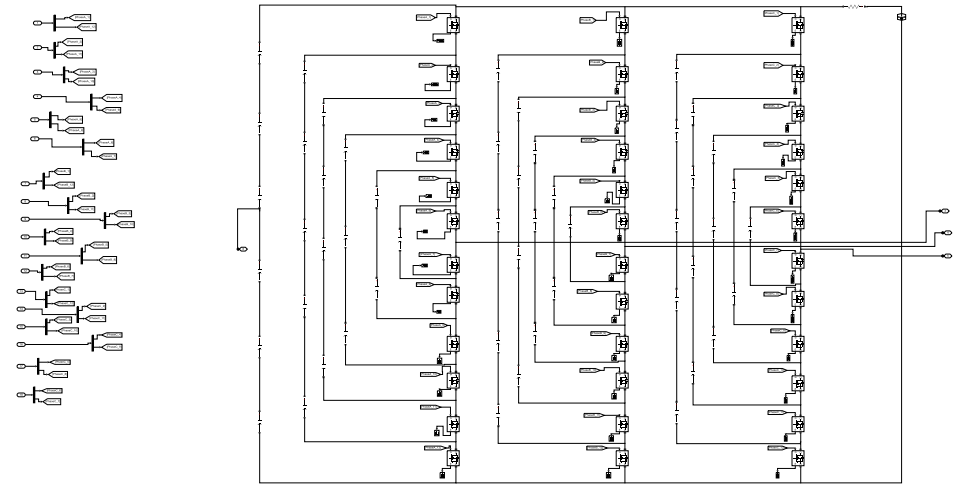


Fig. 11-7: switches' connections for a three phase 7 level CC-MLI

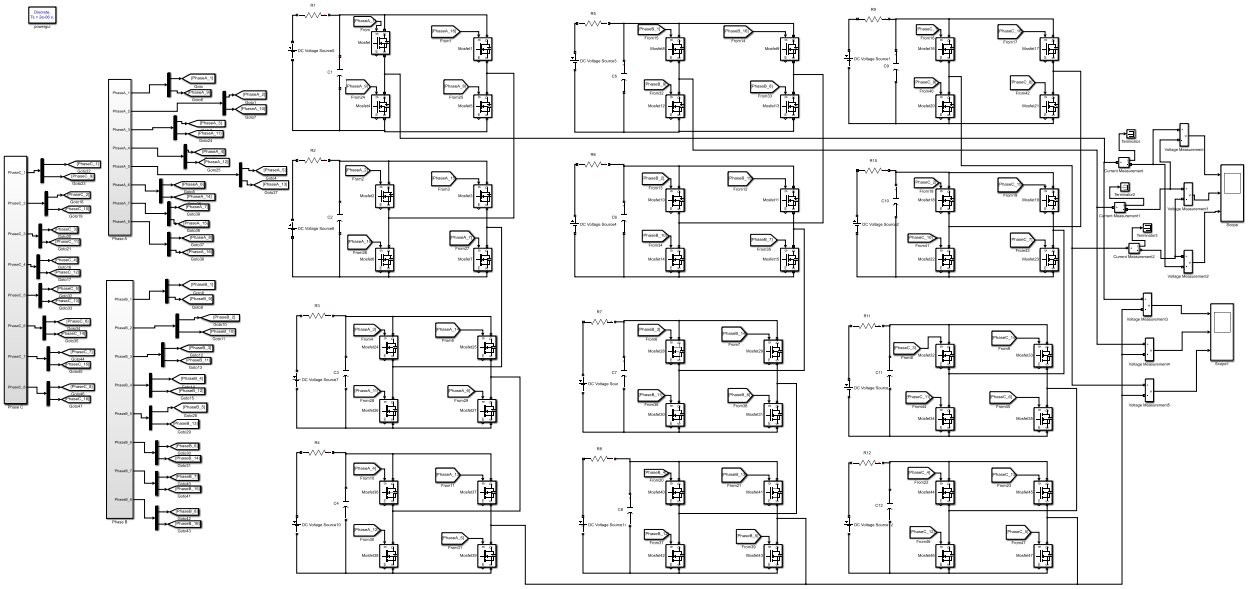


Fig. 11-8: three phase 9 level CHB-MLI

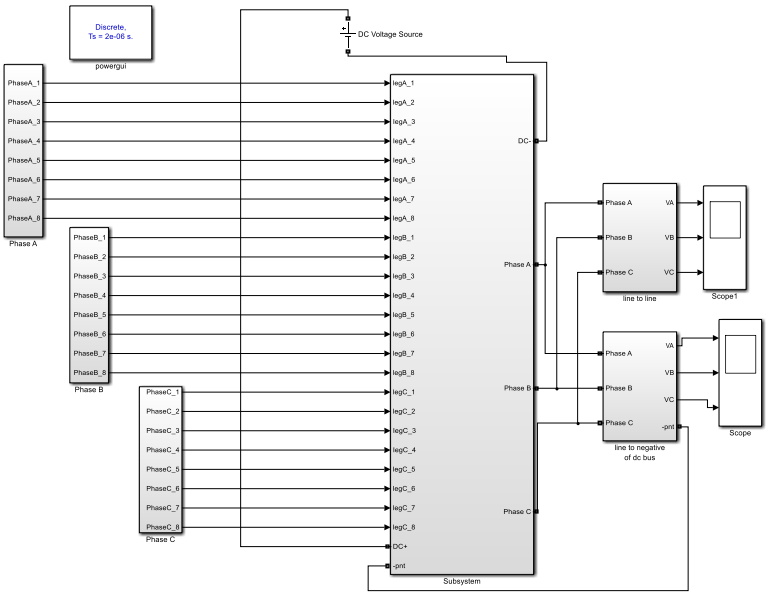


Fig. 11-9: 9 level DC-MLI subsystem blocks

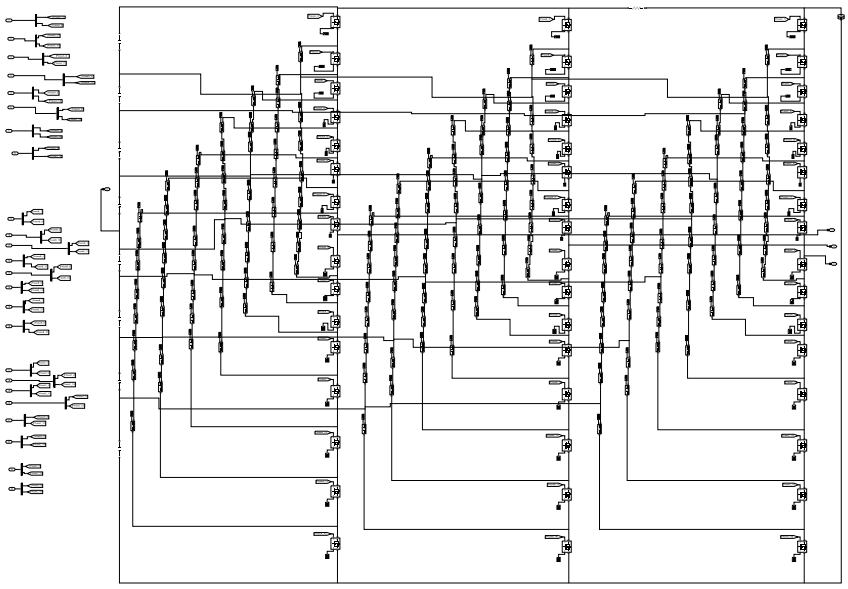


Fig. 11-10: 9 level DC-MLI switches' connections

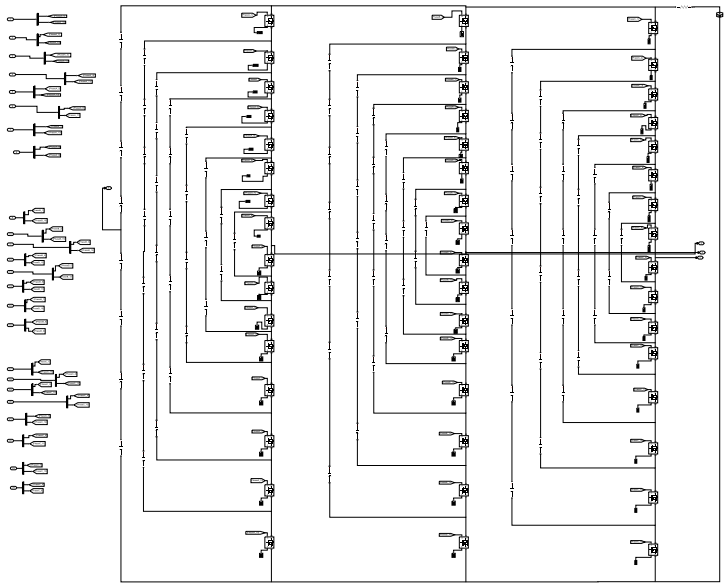


Fig. 11-11: 9 level CC-MLI switches' connections

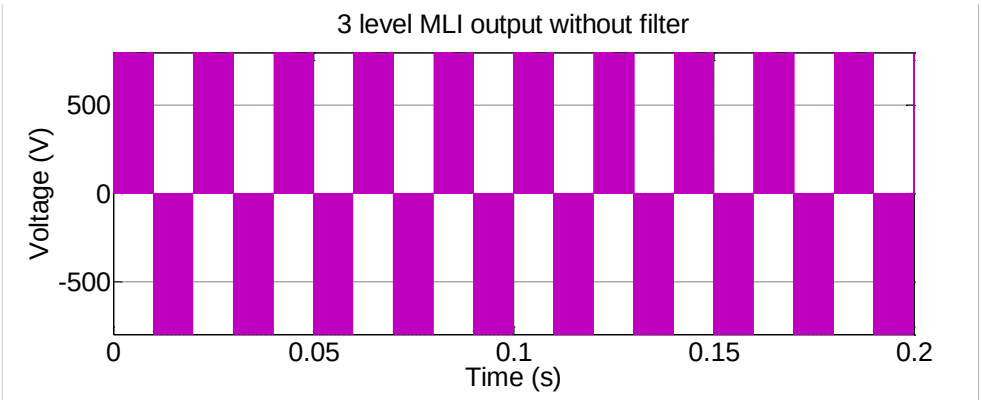


Fig. 11-12: output voltage for a 3 level MLI without filter

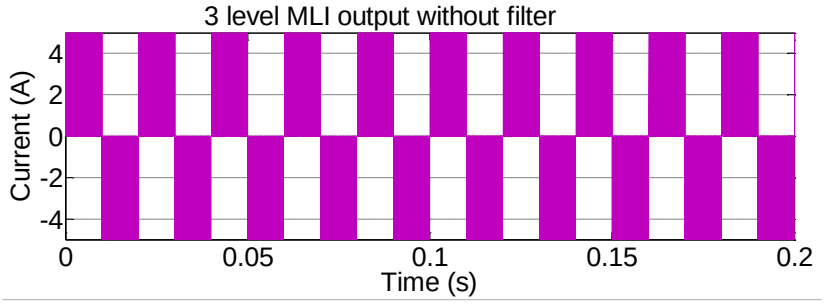


Fig. 11-13: three level MLI output current without filter

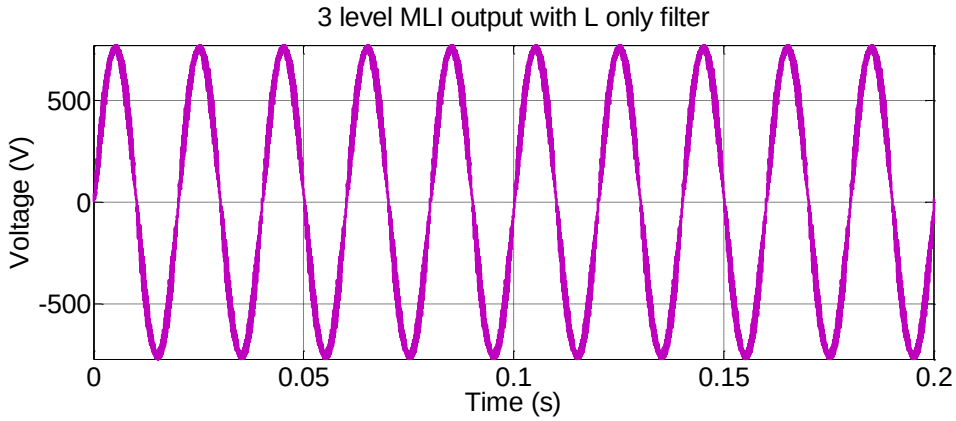


Fig. 11-14: three level MLI output voltage with L filter

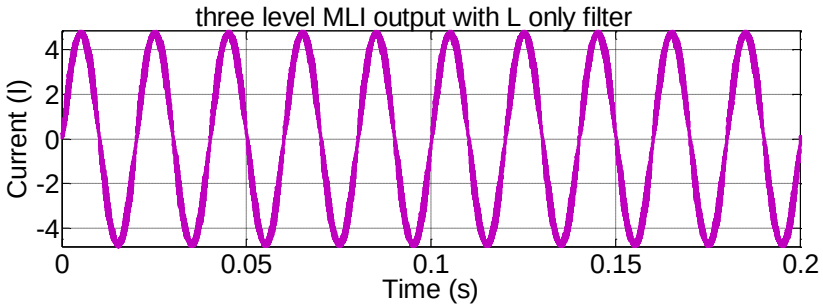


Fig. 11-15: three level MLI output current with L filter

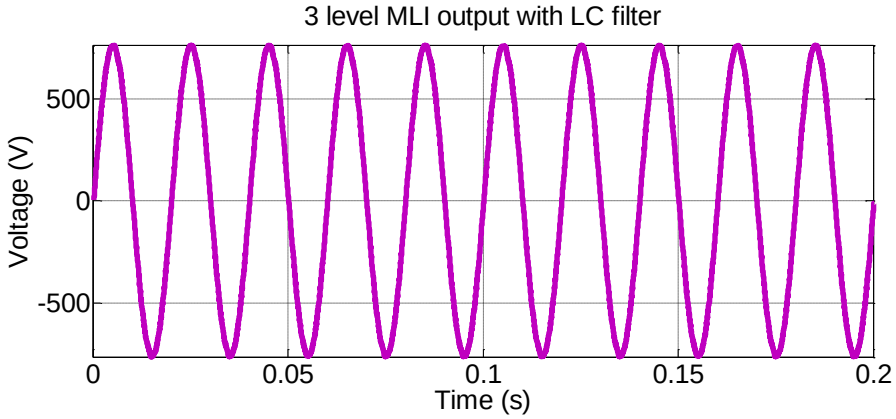


Fig. 11-16: three level MLI output voltage with LC filter

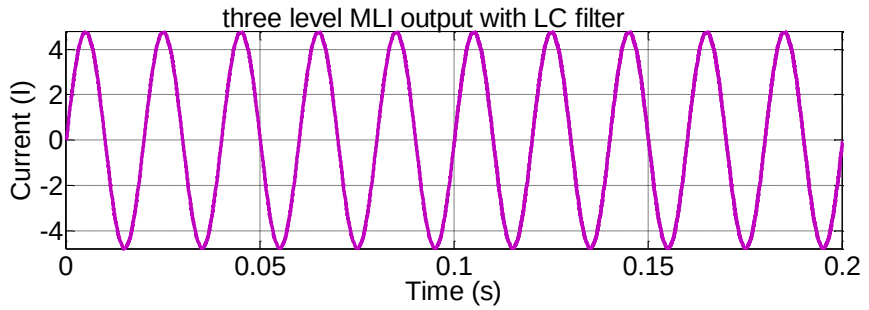


Fig. 11-17: three level MLI with LC filter

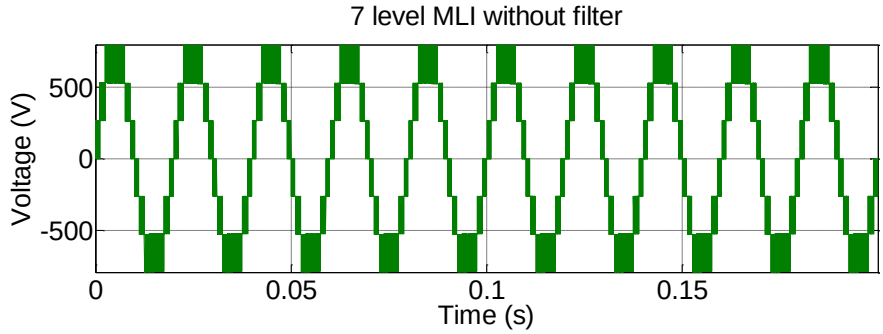


Fig. 11-18: seven level MLI output voltage without filter

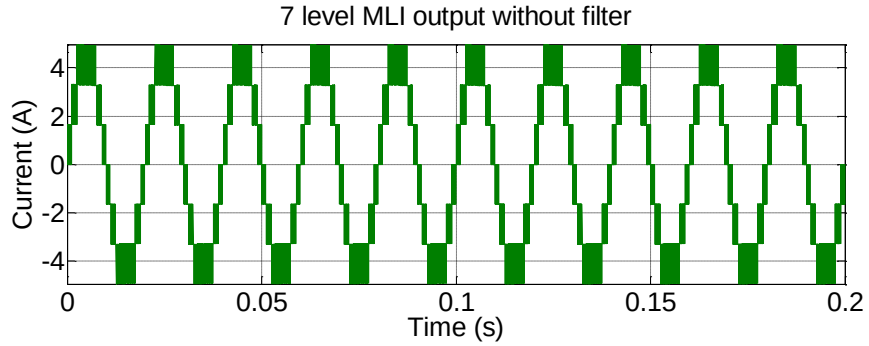


Fig. 11-19: seven level MLI output current without filter

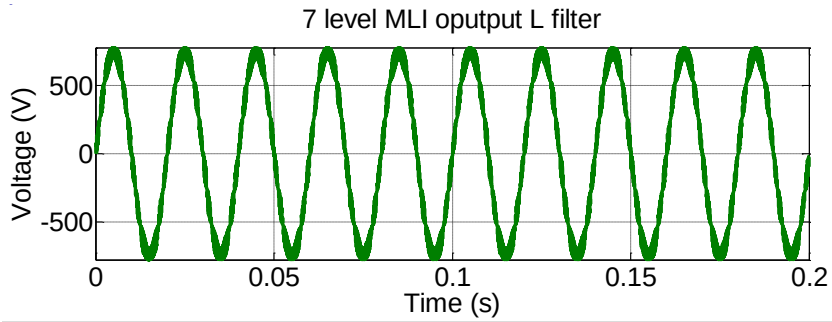


Fig. 11-20: seven level MLI output voltage with L filter

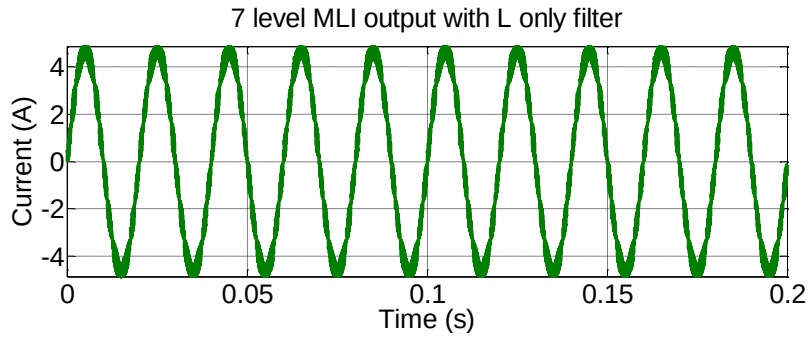


Fig. 11-21: seven level MLI output current with L filter

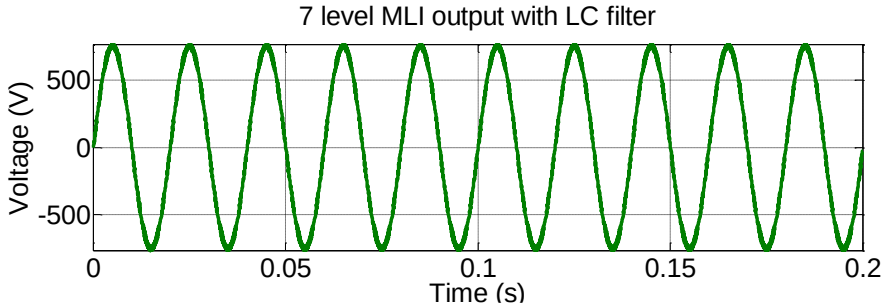


Fig. 11-22: seven level MLI output voltage with LC filter

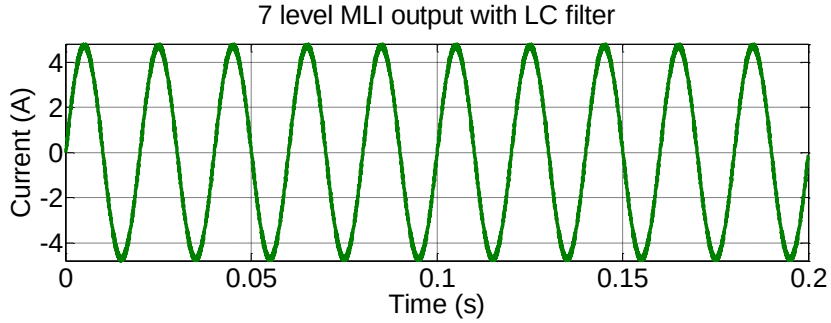


Fig. 11-23: seven level MLI output current with LC filter

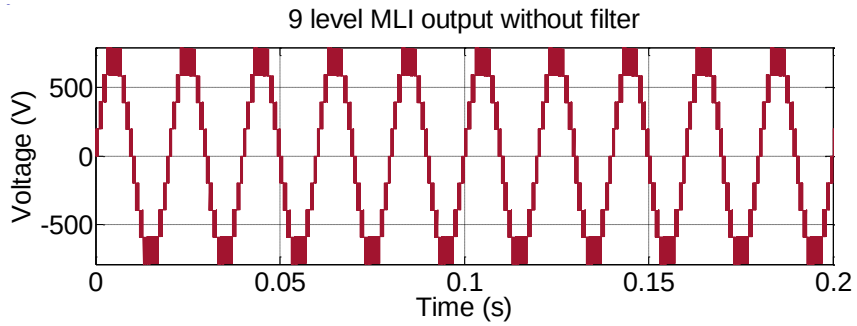


Fig. 11-24: nine level MLI output voltage with no filter

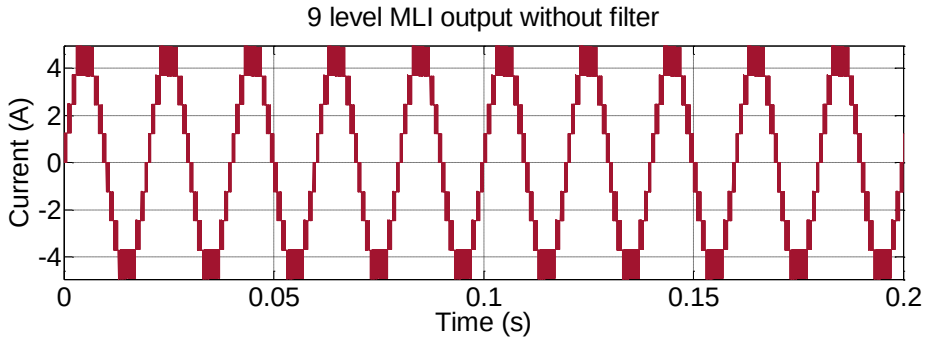


Fig. 11-25: nine level MLI output current with no filter

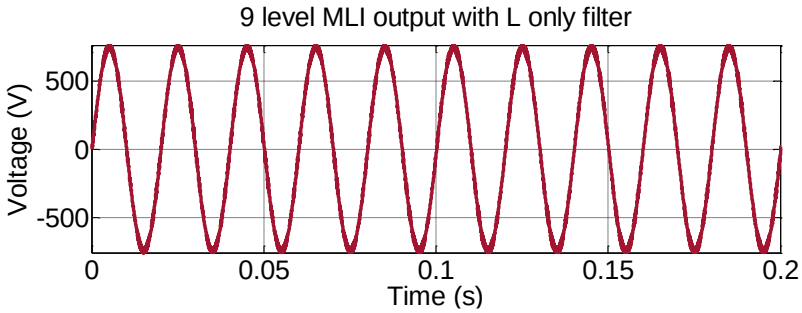


Fig. 11-26: nine level MLI output voltage with L filter

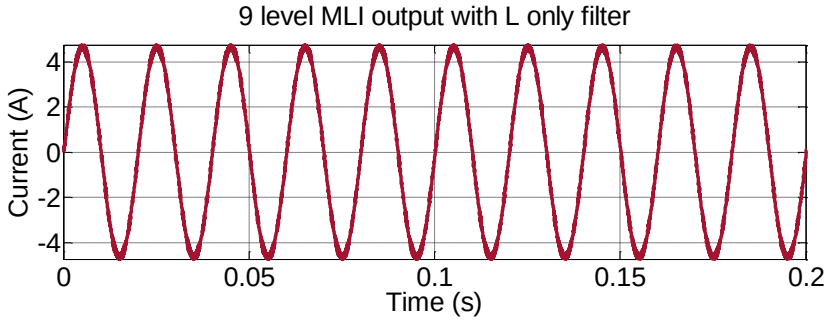


Fig. 11-27: nine level MLI output current with L filter

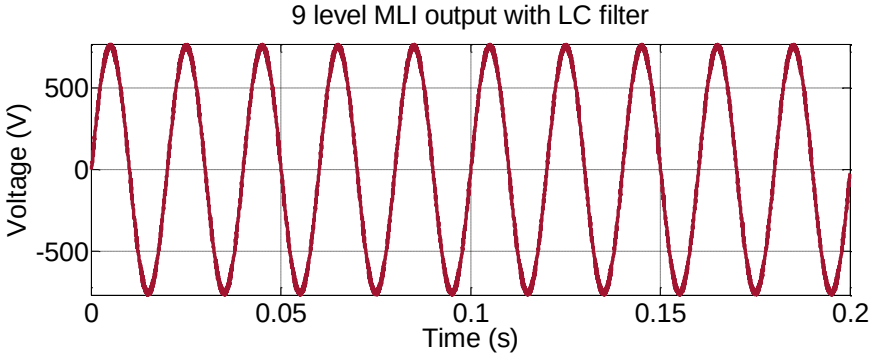


Fig. 11-28: nine level MLI output voltage with LC filter

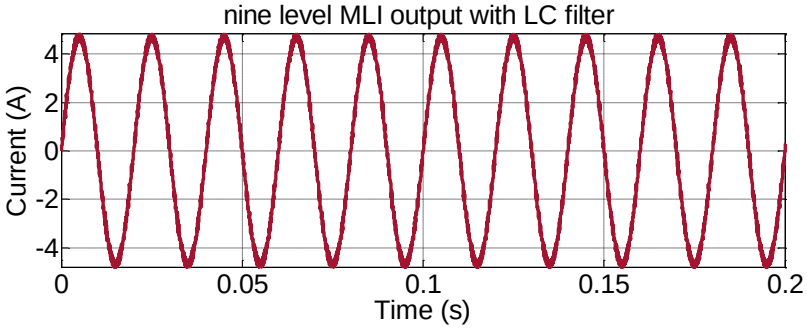
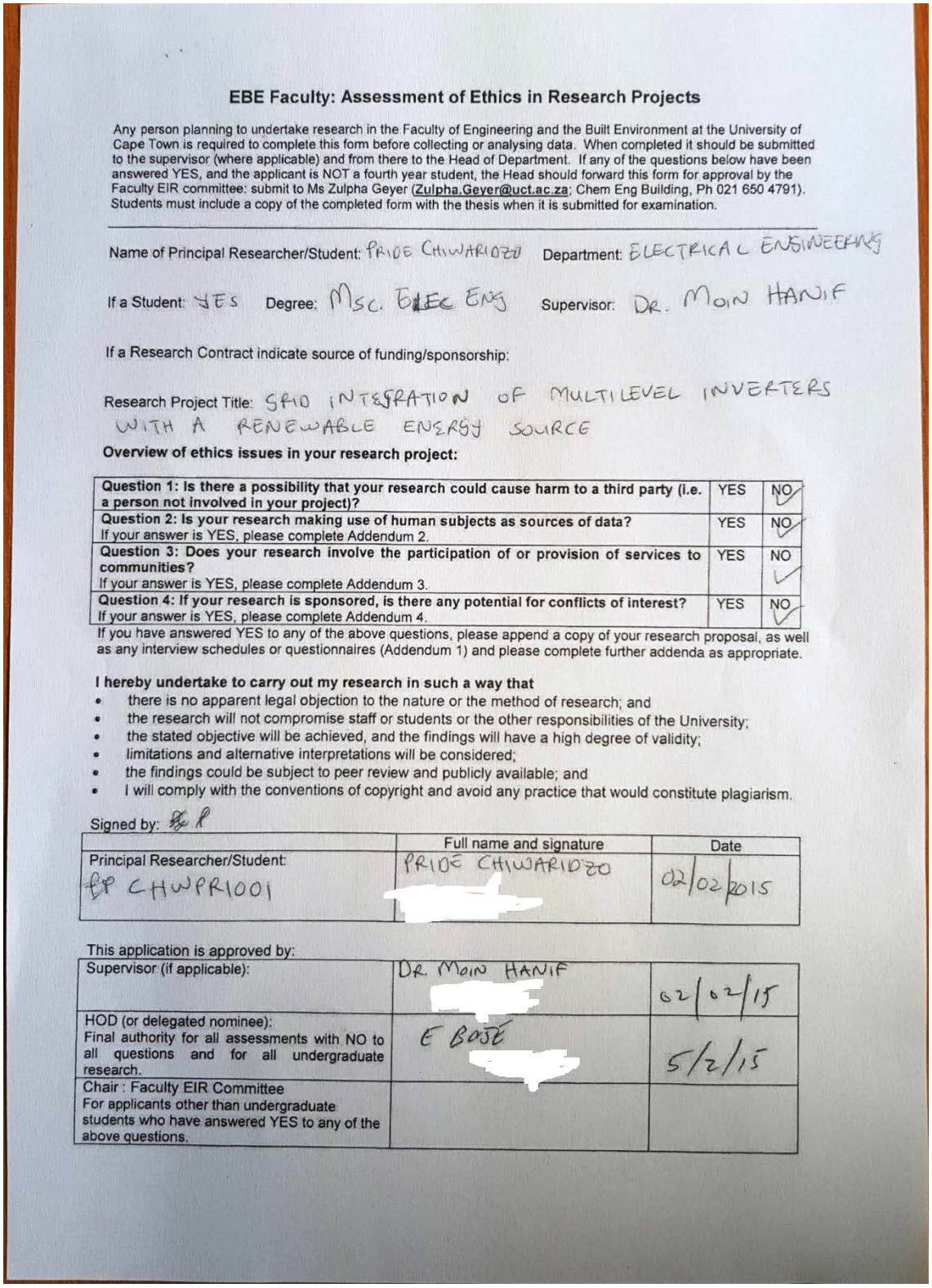


Fig. 11-29: nine level MLI output current with LC filter

Table 11-1: hardware components specifications

Hardware component	Key component specifications
Texas instruments controller F28335	Output voltage: 0 – 3V Frequency: 150 MHz Flash:512kB, Ram: 68kB PWM channels: 12 (+6 high resolution channels) GPIO: 88 Operating temperature: -40 – 125 °C
Desktop computer	Intel core i7, 4GHz 16gB ddr3ram,
600V half bridge driver IC for making the voltage level shifter with interlock	Floating gate driver Operational up to 600V Gate supply 10 – 20V Under voltage lockout for both channels 3.3V, 5V and 15V logic input compatible Programmable deadtime of 5µs to 540ns Low di/dt
LGN series Aluminium electrolytic capacitors for making the H-Bridge cells	Rated voltages up to 600V Temperature range: -25 – 105 °C Rated capacitance changes: 56 - 33000µF Can withstand 2000hrs of rated ripple current application at 105 °C

12. EBE Faculty: Assessment of Ethics in Research Projects



EBE Faculty: Assessment of Ethics in Research Projects

Any person planning to undertake research in the Faculty of Engineering and the Built Environment at the University of Cape Town is required to complete this form before collecting or analysing data. When completed it should be submitted to the supervisor (where applicable) and from there to the Head of Department. If any of the questions below have been answered YES, and the applicant is NOT a fourth year student, the Head should forward this form for approval by the Faculty EIR committee: submit to Ms Zulpha Geyer (Zulpha.Geyer@uct.ac.za; Chem Eng Building, Ph 021 650 4791). Students must include a copy of the completed form with the thesis when it is submitted for examination.

Name of Principal Researcher/Student: PRIDE CHIWARIDZO Department: ELECTRICAL ENGINEERING

If a Student: YES Degree: MSc. ~~Elec~~ Eng Supervisor: DR. MOIN HANIF

If a Research Contract indicate source of funding/sponsorship:

Research Project Title: GRID INTEGRATION OF MULTILEVEL INVERTERS WITH A RENEWABLE ENERGY SOURCE

Overview of ethics issues in your research project:

Question 1: Is there a possibility that your research could cause harm to a third party (i.e. a person not involved in your project)?	YES	NO ✓
Question 2: Is your research making use of human subjects as sources of data? If your answer is YES, please complete Addendum 2.	YES	NO ✓
Question 3: Does your research involve the participation of or provision of services to communities? If your answer is YES, please complete Addendum 3.	YES	NO ✓
Question 4: If your research is sponsored, is there any potential for conflicts of interest? If your answer is YES, please complete Addendum 4.	YES	NO ✓

If you have answered YES to any of the above questions, please append a copy of your research proposal, as well as any interview schedules or questionnaires (Addendum 1) and please complete further addenda as appropriate.

I hereby undertake to carry out my research in such a way that

- there is no apparent legal objection to the nature or the method of research; and
- the research will not compromise staff or students or the other responsibilities of the University;
- the stated objective will be achieved, and the findings will have a high degree of validity;
- limitations and alternative interpretations will be considered;
- the findings could be subject to peer review and publicly available; and
- I will comply with the conventions of copyright and avoid any practice that would constitute plagiarism.

Signed by:

	Full name and signature	Date
Principal Researcher/Student: CHWPRI001	PRIDE CHIWARIDZO	02/02/2015

This application is approved by:

Supervisor (if applicable):	DR. MOIN HANIF	02/02/15
HOD (or delegated nominee): Final authority for all assessments with NO to all questions and for all undergraduate research.	E BOSE	5/2/15
Chair : Faculty EIR Committee For applicants other than undergraduate students who have answered YES to any of the above questions.		

ADDENDUM 1:

Please append a copy of the research proposal here, as well as any interview schedules or questionnaires:

ADDENDUM 2: To be completed if you answered YES to Question 2:

It is assumed that you have read the UCT Code for Research involving Human Subjects (available at http://web.uct.ac.za/depts/educate/download/uctcodeforresearchinvolvinghumansubjects.pdf) in order to be able to answer the questions in this addendum.

2.1 Does the research discriminate against participation by individuals, or differentiate between participants, on the grounds of gender, race or ethnic group, age range, religion, income, handicap, illness or any similar classification?	YES	NO
2.2 Does the research require the participation of socially or physically vulnerable people (children, aged, disabled, etc) or legally restricted groups?	YES	NO
2.3 Will you not be able to secure the informed consent of all participants in the research? (In the case of children, will you not be able to obtain the consent of their guardians or parents?)	YES	NO
2.4 Will any confidential data be collected or will identifiable records of individuals be kept?	YES	NO
2.5 In reporting on this research is there any possibility that you will not be able to keep the identities of the individuals involved anonymous?	YES	NO
2.6 Are there any foreseeable risks of physical, psychological or social harm to participants that might occur in the course of the research?	YES	NO
2.7 Does the research include making payments or giving gifts to any participants?	YES	NO

If you have answered YES to any of these questions, please describe below how you plan to address these issues:

ADDENDUM 3: To be completed if you answered YES to Question 3:

3.1 Is the community expected to make decisions for, during or based on the research?	YES	NO
3.2 At the end of the research will any economic or social process be terminated or left unsupported, or equipment or facilities used in the research be recovered from the participants or community?	YES	NO
3.3 Will any service be provided at a level below the generally accepted standards?	YES	NO

If you have answered YES to any of these questions, please describe below how you plan to address these issues:

ADDENDUM 4: To be completed if you answered YES to Question 4

4.1 Is there any existing or potential conflict of interest between a research sponsor, academic supervisor, other researchers or participants?	YES	NO
4.2 Will information that reveals the identity of participants be supplied to a research sponsor, other than with the permission of the individuals?	YES	NO
4.3 Does the proposed research potentially conflict with the research of any other individual or group within the University?	YES	NO

If you have answered YES to any of these questions, please describe below how you plan to address these issues: