

Development of a Synchronisation and Video Conversion Unit for Denel Overberg Test Range's Tracking Radar

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for the degree of Master of Science in Engineering.

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Declaration

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Abstract

This dissertation discusses the re-development of a subsystem of the tracking radar (TR) at Denel Overberg Test Range (OTR), defined as the Synchronisation and Video Conversion Unit (SVCU). The SVCU performs the task of baseband video processing, generation of all synchronisation triggers, and timing within the TR. The report is based on the Research and Design (R&D) project conducted at Denel OTR and built on the previous study where an SVCU model was designed and tested in SystemVue.

A comprehensive measurement and analysis of all functions was first conducted on all (identical) TRs of Denel OTR to verify against the limited literature that is available relating to the SVCU. Various anomalies were discovered between the design specification documents and measured values. Modifications made to functions in the SVCU as a result of development done on other subunits of the TR and not documented were also discovered. A comprehensively revised design specification and high-level description for the SVCU was then generated.

A new SVCU architecture was specified to improve the current tasks performed by various discrete analogue and digital components, Single-Board Microcontroller and data bus interfaces using commercial off the shelf (COTS) hardware. A prototype was built on the National Instruments (NI) PCI eXtensions for Instrumentation Express (PXIe) platform, utilising high-speed ADCs and Field Programmable Gate Array (FPGA) modules. All functions of the SVCU were modelled and implemented on these modules using LabVIEW and LabVIEW FPGA software.

Fractional Decimators were designed to meet the sample resolution requirement of the range gates (used for range and Doppler measurement). Custom functions were written to integrate samples to increase SNR and apply a correction for errors carried over during the I/Q demodulation. The jitter on the synchronisation pulse responsible for RF energy transmission (TX), the ADC sample clock, and triggers signals that need to travel over excessively long transmission lines used for calibration were found to be the most critical aspects of the SVCU. The root-sum-square of all the jitter on these synchronisation pulses was calculated to ensure that the specified measurement accuracy of the TR is satisfied.

Based on these findings, the PXIe based SVCU is recommended for deployment. Further development of other subunits for the TR receiver on the current platform is recommended, and an outline for future work is provided.

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List of Abbreviations

A/D	Analogue to Digital
A/R	Amplitude / Range
ADC	Analogue to Digital Converter
CC-TWT	Cavity Coupled Travelling Wave Tube
CCA	Central Command Assembly
CFA	Cross Field Amplifiers
CFAR	Constant False Alarm Rate
COTS	Commercial Off-The-Shelf
DC	Direct Current
DDC	Digital Down Converter
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HSDI	High Speed Digital Interface
I/H	Integrate and Hold
IF	Intermediate Frequency
IP	Internet Protocol
IRIG	Inter-Range Instrumentation Group
MCP	Master Computer
NI	National Instruments

OTR	Overberg Test Range.
PCB	Printed Circuit Boards
PPS	Pulse Per Second
PRF	Pulse Repetition Frequency
PRI	Pulse repetition interval
PXIe	PCI eXtensions for Instrumentation Express
R&D	Research and Development
RF	Radio Frequency
RFFE	RF Front End
RFH	RF Head
RHINO	Reconfigurable Hardware Interface for Computation and Radio
RTU	Remote Terminal Unit
SEL	Systems Engineering Laboratories
SP	Signal Processing
SSA	Solid State Amplifier
STCG	Standard Time Code Generator
SVCU	Synchronisation and Video Conversion Unit
TR	Tracking Radar
TRLA	Transmit Receive Limit Attenuator
UCT	University of Cape Town
UDP	User Datagram Protocol
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

This chapter gives background information on the Research & Design project for a Tracking Radar (TR), currently being carried out at Denel Overberg Test Range (OTR), that is the core of this dissertation. The reasons which warranted the re-development of the Synchronisation and Video Conversion Unit (SVCU) project and requirements that needed to be fulfilled is also discussed.

1.1 Background

Radar Systems form a vital role in the instrumentation capabilities offered by Denel OTR. Three coherent Tracking Radars (TR) provide OTR with real-time data of the targets. These are monopulse systems operating in C-band and are known as OTR Tracking Radars. These TRs were acquired in the late 1980's.

The acquired TRs initially transmitted RF energy using a combination of two power amplifiers, namely, Cavity Coupled Travelling Wave Tubes (CC-TWTs), and Cross Field Amplifiers (CFAs). A two-stage heterodyne receiver system consisting of various subsystems was used to convert the reflected signal to baseband level. Signal Processing (SP) and Tracking Algorithms were implemented in a Systems Engineering Laboratories (SEL) series computer, where decisions were made and instructions were created for continuous functioning of the TR.

The operation of a TR requires each subsystem to operate with synchronised timing and in a particular sequence. The received signal also needs to be filtered to improve SNR, digitised, and corrected of any known errors. The SVCU ensures that the synchronisation, filtering and data conversion is correctly implemented for efficient operation of the TR.

The SVCU is a custom built subsystem for the OTR TR. It consists of a single board microprocessor, printed circuit boards (PCBs), and modules designed using discrete components. The technology used is outdated and the components utilised are obsolete. Obsolescence is an existing problem surrounding not only the SVCU but all subsystems of the Tracking Radar. Over the years, various subsystems have been modified and modernised. Some noticeable changes were made to the transmitter to use only the CC-TWT and discard the CFA, due to sustainability and maintenance considerations. The SEL Computer has been replaced with a PC-based framework, and the Central Command Assembly (CCA) has gone through many upgrades to improve the interface between the TR system and operator. Modernisation of the receiver system is now a priority and the SVCU subsystem was identified as a priority.

1.2 Project Description and Requirement

A design specification was documented in the late 1980's for a proposed SVCU. Since the proposal, during the development, concepts and parameters were modified. Unfortunately, no other detailed description and design specification was documented for the SVCU of OTR TR after development.

In 2010, a detailed study of the SVCU was started by J Abraham, a former employee at Denel OTR. The study resulted in understanding the framework of the original SVCU. The theory behind the implementation of different processes and various modes of operation was described. The interfaces between the SVCU and all other subsystems were identified.

His study was concluded in the form of a dissertation titled 'Study of the TR Synchronization and Video Conversion Unit'. The dissertation was submitted in June 2012, after a working model was developed using SystemVue and a Field Programmable Gate Array (FPGA) based technology was recommended for use in the development of the SVCU. The recommendation of the re-development using FPGA's was so that the stringent specifications relating to timing requirements could be met.

The project has moved to the second phase where a working prototype of the SVCU is to be developed. In 2015, a Research and Development (R&D) project was initiated for re-development of the SVCU, taken upon by Kushal Uprety (author), an employee at OTR. The project, in collaboration with the Radar Master's group at the University of Cape Town (UCT), forms part of the dissertation towards the fulfilment of a Master's degree in Electrical Engineering.

The key requirement in this R&D project and dissertation is the re-development and

implementation of a functional SVCU prototype. The prototype will act as a building block to the continuous modernisation and improvements to be made to the TRs. The technology or framework used, and the requirements that need to be fulfilled, forms the critical part of the development. Comprehensive requirements and specifications for the re-development of the SVCU are identified and given as follows:

Identify and source industry standard reconfigurable (FPGA) hardware to fulfil the stringent requirements and provide a platform for continuous improvement on the receiver system of the OTR TR.

Create a platform in the new SVCU framework to re-develop other subsystems that require immediate attention following the re-development of the SVCU.

Make provisions for the replacement of Ambiguous Range Scopes used for operational purposes (Future Project).

Investigate the use of Digital Down Conversion to replace the Quadrature Demodulators in the receiver subsystem that are obsolete.

Replace MUXBUS Interface with an Ethernet UDP interface and evaluate the performance on acquiring configuration from a System Computer.

Conversion of tasks performed using analogue and discrete components to digital domain.

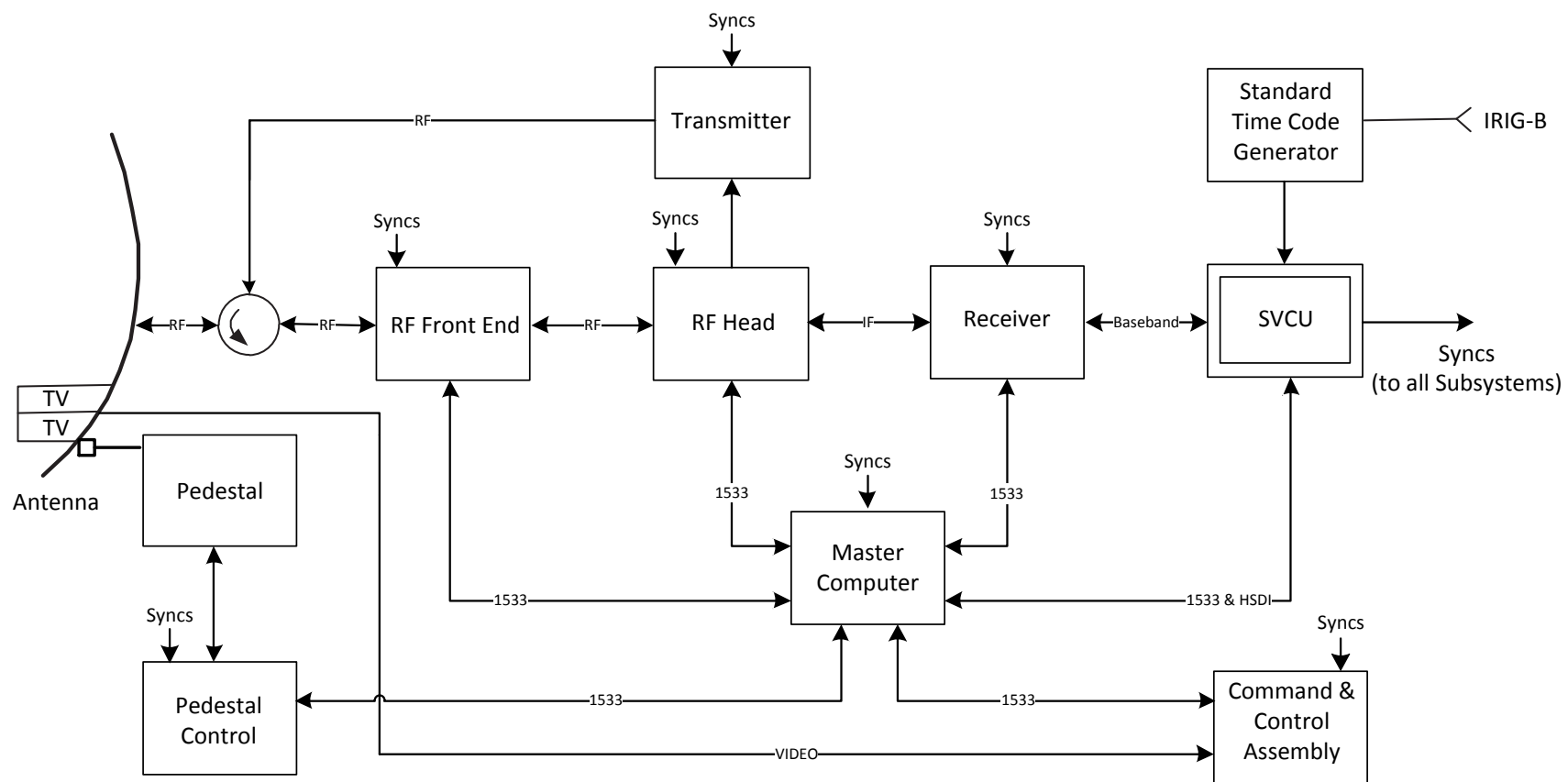
Replacement of High Speed Data Interface (HSDI) with Ethernet and change in format of output data from the SVCU to floating point format.

Test the performance of the re-developed SVCU prototype against stringent timing requirements.

Synchronise the new system with the time generated by the OTR's Standard Time Code Generator (STCG).

1.3 Literature Review

The SVCU is a subsystem built for the OTR's TRs, which is located at the end of the receiving chain, as shown in Figure 1.1. The SVCU is the focus of this dissertation and is discussed in detail in Section 2.3. A general introduction to the TR and its receive chain is also presented Chapter 2, to give a better understanding of the SVCU's role within the radar system.



HSDI – High Speed Data Interface
 1533 – Mil-Std 1553B Serial Databus

Figure 1.1: A general block diagram of the OTR's TR

The SVCU serves as the analogue to digital interface and synchronises the entire TR by providing timing (syncs) to all the TR subunits. Radar systems utilise a synchroniser to generate the Pulse Repetition Frequency and various other timing signals. However, the SVCU performs the functionality of a combination of various other subunits in the radar system. Given the different functions of the SVCU, it is important to establish a connection between the requirements for the new SVCU, advancement in the field of various functional aspects of the SVCU, and the technology currently used. Many techniques and modern methods employed in radar systems around the world are classified. Even though there are many studies done in the theory of operation, few are implemented and in most cases information is not disclosed. This Chapter will discuss various sources of information that are available in the academic and public domain that complements the functionality of the SVCU.

1.3.1 Timing and Framework

In 2012, a study was done by J Abraham on the SVCU of the TR at Denel OTR. In the study the functionality of the SVCU was modelled at a high level using SystemVue. This showed the effect that timing uncertainty, caused by hardware, has on range accuracy [1]. The study also identified that Field Programmable Gate Array (FPGA) technology is able to meet all the timing requirements of the SVCU.

One of the most important facts gathered from the study was that the total jitter (uncertainty) budget on the measurement process within the tracking radar is set at 30 ns. This corresponds to the specified 1.5 m (RMS) accuracy of the TR. The measurement process in the SVCU involves generation of synchronisation and transmit pulses, analogue to digital conversion and range gate triggers used for the integration of sampled data.

The study concluded with the recommendation that the Reconfigurable Hardware Interface for Computation and Radio (RHINO) board from UCT, be used as a prototyping platform for the new SVCU. From the study of Mr. J Abharam's thesis it was evident that a framework used for prototyping the new SVCU should be based on FPGA technology.

In 2011 a study was conducted to create a platform for radio prototyping and signal processing at a reasonable cost. The research done (as a master's project) was to develop a cost-effective platform for software defined radio applications [2]. This aided radar enthusiasts and engineers to perform research and implement certain applications within a constrained budget. The RHINO board would act as back-end to any radar prototyping. Various modular hardware (e.g. transceiver, GPS disciplined timing cards) from different vendors could then be interfaced with the Rhino Board to perform research into different

aspects of a radar system.

1.3.2 Data Processing

The objective of this dissertation is to modernise the SVCU system. It is crucial to ensure that modifications made in the processes of developing a new SVCU system does not warrant a significant adjustment of the Signal Processing and Tracking Algorithm in the Master Computer. Changes to other subunits of the radar system would be beyond the scope of this dissertation. A study was conducted with regards to data processing to investigate an alternative or improved method to digitise and process the baseband video signal in the SVCU.

A journal entry by FH Krantz and WD Murray titled ‘A survey of digital methods for radar data processing’, reviews some declassified techniques used in digital data processing. The paper focuses on signal time-sampling, quantisation, integration methods, and trigger manipulation, amongst other aspects [3]. This supplemented the understanding of processes in the current SVCU and how it can be improved.

From the paper, it was identified that the sliding window integration method is still a preferred way of processing digital data for detection. A sliding window integrator integrates and produces the cumulative sum of input signals over the time of a fixed specified length. The current SVCU system uses this integrator to produce 20 range bin sums for detection. This process is explained in more detail in Chapter 3.

Instead of changing this technique to process data, the focus is put on improving the implementation of the integration function. The existing three range gate (Early, Centre & Late) sum for tracking purposes, uses an analogue integrate and hold circuit. These analogue components will be replaced with a digital integrator. All digital functions performed using discrete components will also be implemented as a function inside the FPGA.

1.3.3 Sample Correction and Compensation

The current SVCU system uses coherent quadrature demodulator modules to down convert signals to baseband. Despite it producing an accurate result in the OTR radar system, it is always sensitive to gain and phase mismatch (errors) when producing In-Phase and Quadrature outputs.

The correction method implemented in the current system is based on the paper titled

‘The correction of I and Q Errors in a Coherent Processor’ by FE Churchill, GW Ogar and BJ Thompson. It describes the method of correcting gain and phase imbalances and the bias errors in the I/Q channels by means of coefficients derived from measurement of a test signal [4].

The method takes into account the contribution of errors specifically in a multiple target indicator canceller, Constant False Alarm Rate (CFAR) detector [4]. The method describes the process of digital filtering being implemented at DC, test signal frequency, image frequency, and producing a phase and gain correction coefficient relating to digital samples of the signal [4]. The bias correction factor is generated by subtracting the average level from the acquired signal.

Other preferred methods do not make use of test signals and use techniques such as blind source separation [5, 6] and interface-canceller (IC) [7, 5] methods. These methods have been proven to operate at low intermediate frequencies.

A novel approach was published in the paper produced by JJ de Witt and GJ van Rooyen titled ‘Novel I/Q imbalance and offset compensation techniques for quadrature mixing radio transceivers’. This method differs from others as it generates correction coefficients based on the imbalance extracted from relative sideband measurements and DC offset extraction from spectral measurements [8].

Improving on the technique used for generating the correction coefficients would be beyond the scope of this project as it is a task performed by the main computer. The correction coefficients are, however, applied in the SVCU. In union with the correction coefficient, a scaling factor is also utilised to compensate for the DC offset created in the process of integrating the sampled data for the detection channel. Bits are shifted due to the restriction of bits in the FIFO that carries the sampled data to the arithmetic and calibration module in the SVCU. The new SVCU system will make provision for this and apply only the mismatch correction.

1.4 Project Outline

This dissertation consists of six chapters and two appendices. An overview and operational capabilities of the Denel Overberg Test Range’s TR is presented in Chapter 2. The chapter proceeds to discuss, the various signal channels that are formed and receiver system which converts the signal reflected from the target from RF (transmitted at a selected frequency between 5.4 and 5.9 GHz) to digital baseband video using the following subsystems:

- RF Front End (RFFE)
- RF Head (RFH)
- The Receiver
- Synchronisation and Video Conversion Unit (SVCU)

Table 1.1: Receiver system parameters

Parameters		Value
Noise figure		5 dB
Dynamic range	Instantaneous	50 dB
	Overall	110 dB
Down conversion	IF1 (bandwidth)	1080 MHz (20 MHz)
	IF2 (bandwidth)	30 MHz (6 MHz)
SVCU clock resolution	Fine (Coarse)	6.25 ns (100 ns)
Clock jitter		1 ns

A detailed description of the subunits of the TR's receiver system with the parameters as listed in Table 1.1 [9] is provided within this chapter. An introduction to the original SVCU is then provided with a brief description of all the PCBs and modules that form part of the SVCU subsystem. The chapter concludes by presenting a comprehensive functional description of the new PXIe based SVCU prototype, where the functions (summarised version) as listed in Table 1.2 are implemented.

Table 1.2: Functions of SVCU

Functions		Description
Video Processing		
	Σ_D	20 Range Bins for detection
	Σ_T	Centre range gate for target tracking
	Σ_T, Δ_{AZ} and Δ_{EL}	Early, centre, and late range gate for target positioning
Timing		
	Sync generation	Timing to all TR subsystems
	Timebase	Initiate process and time stamp events
	Clocks	Reference to TR's subsystems
	Composite Video	Markers for raw video display

The analogue properties of the timing signals (syncs) distributed to all subsystems of the TR is discussed in detail in Chapter 3. A revised list of timing and data processing requirements is also presented due to the inconsistencies found in the design specifications of SVCU which was compiled before the original SVCU was developed.

LabVIEW and LabVIEW FPGA software was used to program the various modules of the National Instruments' PXIe based system as listed in Table 1.3. The SVCU processes that are implemented in the various modules are described in detail in Chapter 4.

Table 1.3: Modules of the new SVCU prototype

Module	Description	Function
PXIe 5170R	250 MS/s, 14-bit, FPGA based Digitiser	Baseband video processing
PXIe 7961 R	Reconfigurable FPGA Module	Timing signal generation
PXI 6683H	Timing and Synchronisation Module	Timebase and timestamp generation
PXIe 6684	High Speed Digital I/O Adapter	Timing signal distribution
PXIe 8840	Intel Core i5 Processor	Communication with the TR's Master Computer
PXIe 1082	PXIe Chassis	Distribution of clocks

The key findings and results are discussed in Chapter 5. The FPGA based system is able to meet all the critical aspects of the timing and video processing tasks of the SVCU. The total jitter (root-sum-square) of the new PXIe based system is calculated and verified to be within the specified jitter budget of the TR (30 ns) to meet the range accuracy of 1.5 m (RMS). The chapter is concluded by discussing some of the user interface diagnostic tools created in LabVIEW.

The dissertation is concluded in Chapter 6 based on the findings and outcome of the development project. The new PXIe based SVCU prototype is motivated for deployment in the TRs. The new SVCU architecture and PXIe platform, are also presented as a good base to implement functionalities of other subsystems of the receiver system. Future works are outlined to be built on the current platform and the FPGA based vector signal transceiver is recommended as a long term strategy for obsolescence management of the receiver systems of the TRs.

Chapter 2

Conceptual Framework

This chapter provides an introduction to Denel OTR and the three identical TRs that are at the facility. A brief description of subsystems of the Transmitter-Receiver Chain is provided leading up to the SVCU. The components and architecture of the current SVCU are discussed. The information presented in this chapter gives the reader a quick background to the system being re-developed and various other subsystems around it. A framework for the new SVCU prototype is then discussed in detail.

2.1 Denel Overberg Test Range

Denel Overberg Test Range (OTR) is a multifunction test facility and a division of Denel SOC Ltd. Situated in the Overberg region of the Western Cape, near the southernmost tip of Africa, the main business activity of OTR involves in-flight testing of advanced guidance and aviation systems for international and local clients. The services offered are [10]:

- Air to air tests
- Air to surface tests
- Surface to surface tests
- Surface to air tests
- Aircraft performance, carriage and release clearance
- Avionics evaluation and certification assistance

The layout of the site at Denel OTR is shown in Figure 2.1 [11] below:

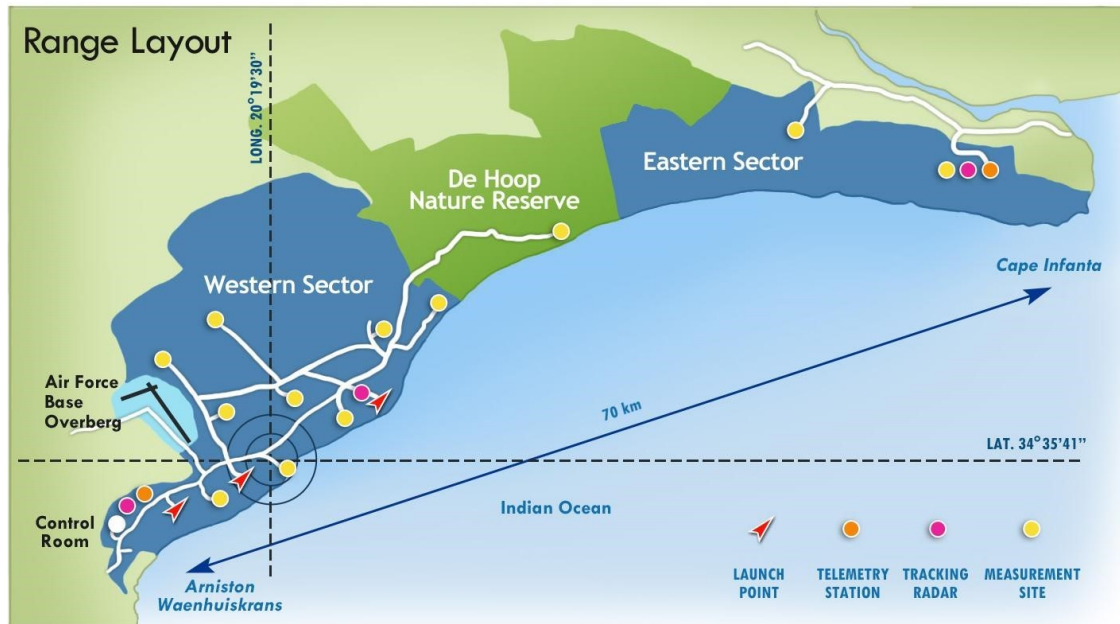


Figure 2.1: Denel OTR layout

2.2 Tracking Radar

Denel OTR has the availability of three Tracking Radars (TR) at the facility. These TRs are pulsed Doppler, coherent, instrumentation radars [9]. The TR system can provide the OTR central computer system with velocity and target position data for real-time or offline analysis. An illustration of a TR is shown below in Figure 2.2.



Figure 2.2: Illustration of Tracking Radar at Denel OTR

The TRs have the ability to track targets in skin (on reflected signal: coherent) and beacon (targets carrying a transponder: non-coherent) mode.

The TR has the following specification and operational capabilities in the measurement of range, azimuth, elevation, and radial velocity as listed in Table 2.1 and Table 2.2 [9]:

Table 2.1: Technical parameters of Denel OTR's Tracking Radar

Technical Parameters	Specification	
Transmit Frequency	5.4-5.9 GHz	
Peak Power	(TWT + CFA)	600 kW
	(TWT only)	50 kW
Pulse width	Single Pulse	0.5, 1 or 2.5 μ s
	Double Pulse (Beacon Mode)	3-12 μ s
PRF	300-3000 Hz	

Table 2.2: Operational parameters

Operational Parameters	Specification	
Range	Min	500 m
	Max	180 km (Skin operation, 1m ² target RCS)
		2800 km (Beacon operation)
Maximum Velocity	Radial	10 km / sec
	Angular	42° / sec
Maximum Acceleration	Radial	300 m / sec ²
	Angular	20° / sec ²

2.2.1 Transmitter

The RF signal in the TR is amplified through a cascade of three amplification stages as listed in Table 2.3 [9]:

Table 2.3: Transmitter amplification stages

Stage	Amplifiers	Output
1	Solid state amplifier (SSA)	1W
2	Travelling Wave Tube (TWT)	60kW-80kW
3	Cross Field Amplifiers (CFA)	600kW

The RF excitation and synchronisation pulse is fed to the transmitter as show in Figure 2.4, which amplifies the RF signal and shapes the pulse to a required pulse width by modulating the amplifying tube [9].

2.2.2 Antenna Feed Assembly (RFFE)

The sub reflector geometry of the parabolic dish antenna, focuses the returned RF signal into the 12 horn feed assembly [12]. The outputs from the horns are passed through a monopulse comparator assembly consisting of a waveguide network, which form the Σ , Δ_{AZ} , and Δ_{EL} channels by summing the outputs from the horn while changing the phase as required [12] as illustrated in Figure 2.3 [1].

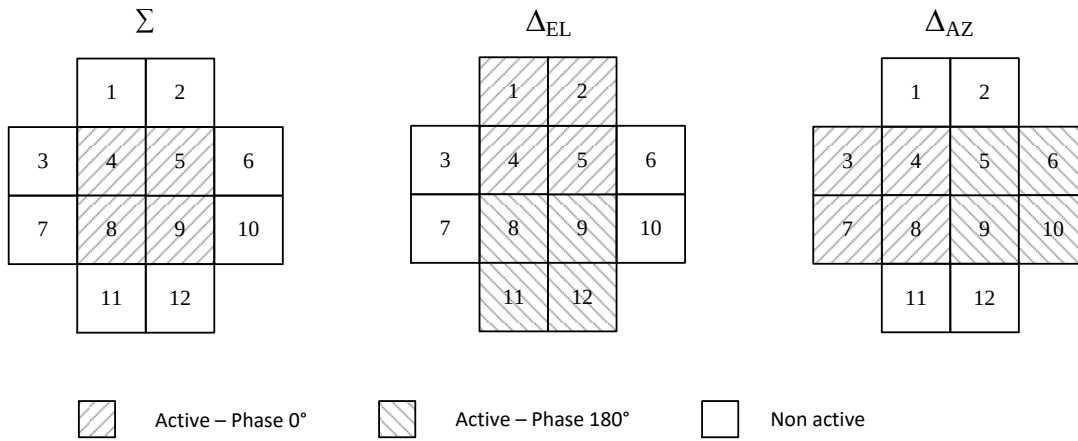


Figure 2.3: Σ and Δ channel formation

2.2.3 RF Front End (RFFE)

The RFFE (Figure 2.4) is the first sub-unit of the receiver system. The signals input to the Front End are the three receiving channels (Σ , Δ_{AZ} , Δ_{EL}) from the monopulse comparator assembly situated in the antenna feed. The RFFE provides the following functionalities [9, 13]:

Protection: The protection of the receiver system is accomplished by the following mechanisms:

- Stage 1: The use of circulators in the RFFE, which allows for the antenna to be switched between transmit and receive modes. This protects the sensitive receiver from high power transmission signals.

- Stage 2: The use of a Transmit Receive Limit Attenuator (TRLA), which protects the receiver from transmitter leakage and attenuates high power signals.

Signal Conditioning: The RFFE performs amplification of weak received signals and suppresses frequencies outside of the 5.4 to 5.9 GHz band using band pass filters.

Test signal injection: Pilot/Built-in Test Equipment (BITE) signal can be injected in this sub-unit to perform diagnostic operations.

2.2.4 RF Head (RFH)

The RFH downconverts signals received from the RFFE to an Intermediate Frequency (IF2). The Σ channel is split in the RFH before down-conversion. Its new branch, Σ_V , is used for display. The conversion is done in a two-stage heterodyning method [9, 13]:

- The first Local Oscillator (LO) converts the signal from the carrier frequency (selected between 5.4 to 5.9 GHz) to an Intermediate Frequency (IF1) of 1080 MHz.
- The second LO converts the 1080 MHz signal to 30 MHz (IF2)

LOs are selected according to the mode of operation: the TR's 120 MHz Temperature Controlled Crystal Oscillator (Master Oscillator) for SKIN mode and an external Voltage Controlled Oscillator (VCO) for BEACON mode. The Master Oscillator is situated within the RFH and provides a reference to various subunits of the TR as follows [9]:

- A 10 MHz signal synthesised from the Master Oscillator as a reference to the SVCU.
- Reference signal for RF excitation in the transmitter and to the calibration system.
- Synthesis of PILOT signals for diagnostic and calibration purposes.

2.2.5 Receiver

Primarily the receiver's function is to convert the IF2 signals received from the RF Head to baseband video. Coherent phase detector modules in the receiver perform Quadrature Demodulation of signals to bipolar In-phase and Quadrature videos. The Σ channel in the receiver is split into two branches to form Σ_T for tracking purposes and Σ_D for detection. Together with these two, the conversion of Σ_V , Δ_{AZ} and Δ_{EL} result in 5 I/Q signal pairs that are sent to the SVCU for digitisation. A block diagram of the receiver subunits preceding the SVCU is shown in Figure 2.4 [13, 1].

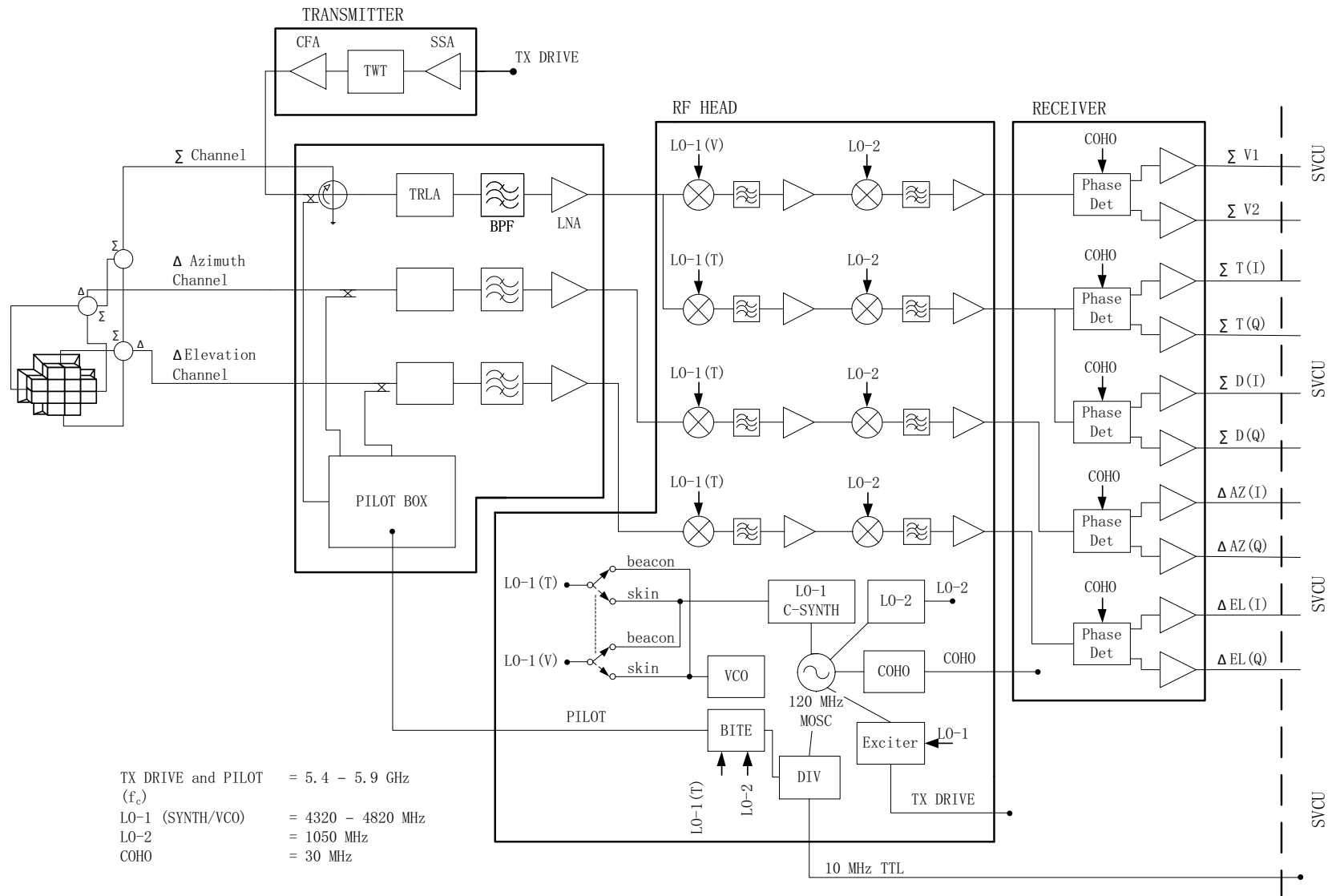


Figure 2.4: Transmit and receive overview

2.3 Synchronisation and Video Conversion Unit

The section describes the original SVCU subsystem of the TR. The functions of the SVCU and its various subunits are discussed in general.

The main function of the SVCU is to serve as an analogue to digital interface and produce complex triggers to synchronise all subsystems of the radar. The digitisation process is dictated by the TR's Master Computer. The digitisation of data is controlled using an ADC module that is triggered for a specific search window where the echo from the target could lie for detection purposes. For target tracking, range gates and Integrate and Hold (I/H) circuits are implemented preceding the digitisation. Together with these, the SVCU performs the following tasks [14, 13, 9]:

- Condition the signal prior to A/D conversion.
- Implement pulse matched filter.
- Apply I/Q mismatch correction coefficients.
- Perform data format transformation.
- Provide raw video to Amplitude/Range (Scope) display.
- Provide clock synchronisation triggers and timing to all subsystems.

The current SVCU contains analogue and digital circuits, including a microprocessor board (based on the standard Intel Single Board Computer 86/12), to achieve this. Lastly, the SVCU also performs specific time-based functions for Test Range analysis [9, 14]:

- Generate timing and frame triggers relative to the time of day received in the Test Range's standard format.
- Time stamping of acquired data.

The SVCU sends the corrected digital samples for signal processing to the Master Computer using the High-Speed Data Interface (HSDI) bus. It receives instructions and gives error status reports to the MCP using the 1553 Interface (a serial 1 MHz avionic data bus).

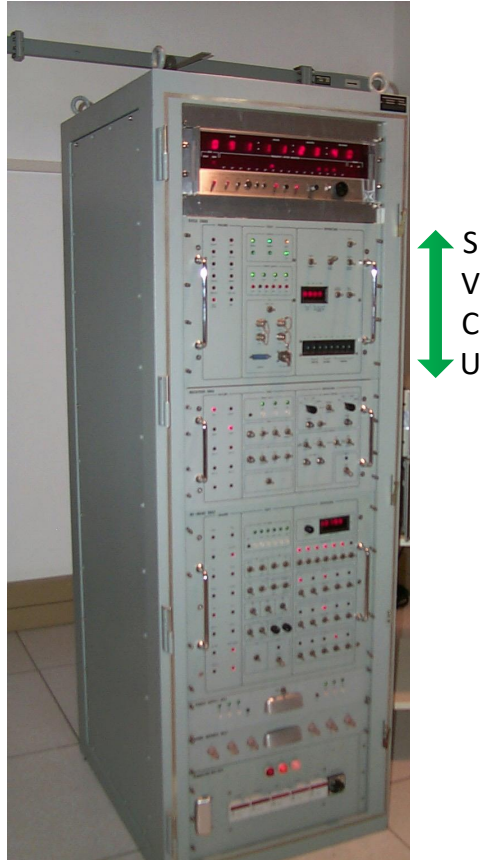


Figure 2.5: SVCU within the receiver rack

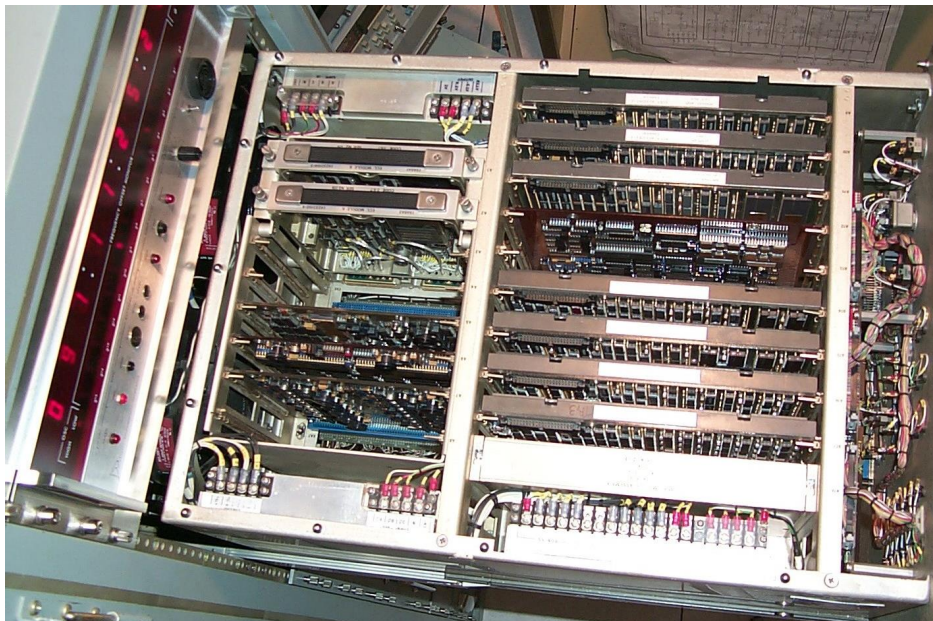


Figure 2.6: SVCU subunits

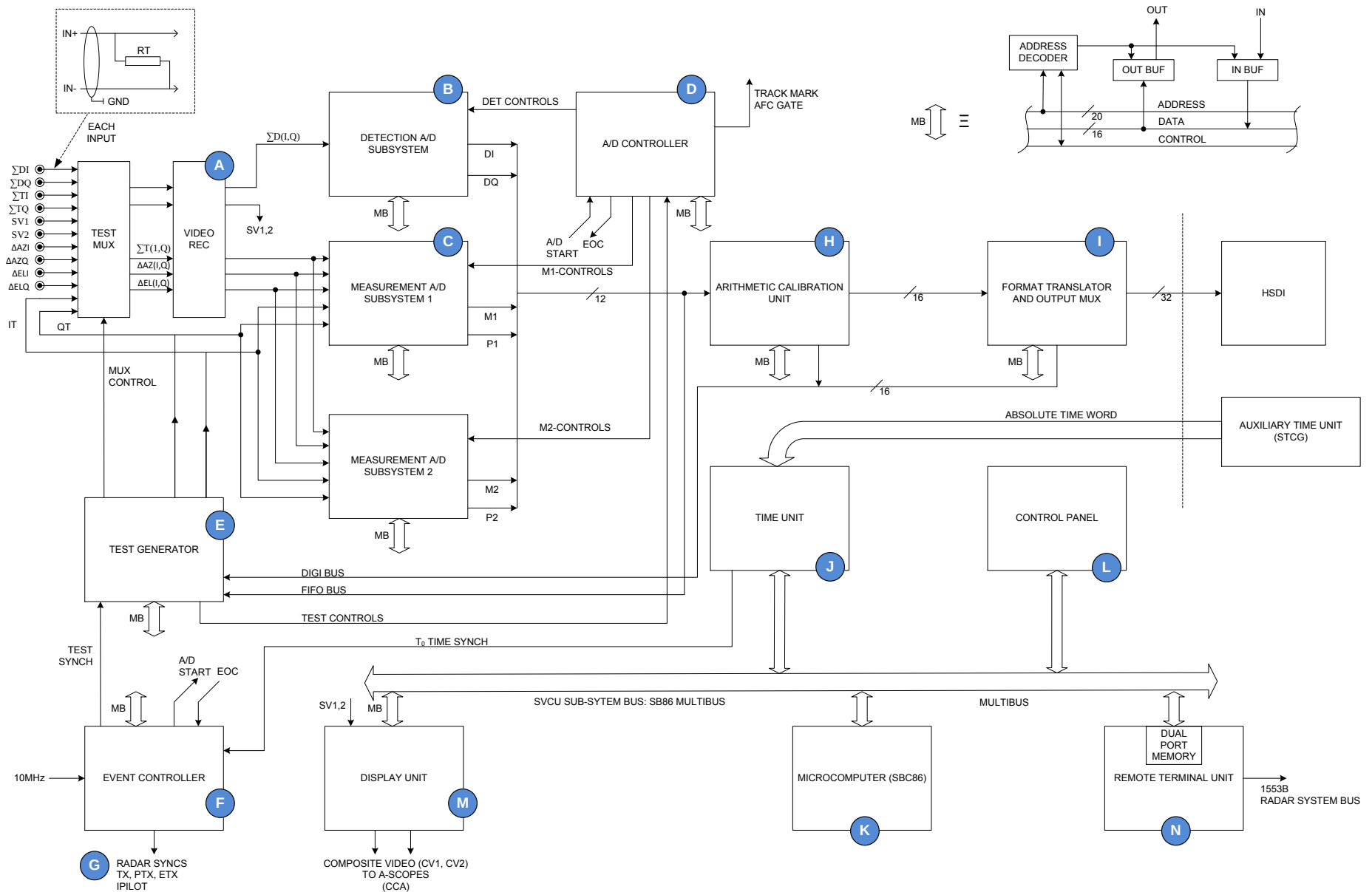


Figure 2.7: Block diagram of previous SVCU subsystem

The design of the SVCU consists of a 19-inch rack with various Printed Circuit Boards (PCBs) or modules stacked horizontally and connected via a wire wrap backplane as shown in Figure 2.5 and Figure 2.6. The subunits of the SVCU and their functions are briefly described below as per the block diagram in Figure 2.7 [14].

A Video Receiver

- Consists of analogue circuitry to condition the signal received from the receiver unit.
- Provides isolation between the SVCU and receiver subsystem.
- Uses a multiplexer to switch between the receiver signals and built-in test signals.

B Detection ADC

- Performs the task of A/D conversion of $\Sigma_D(I, Q)$ signals into digital data for detection purposes.
- Data conversion (digitisation) is done using the 10 MHz clock.
- Digital data are then segmented into 20 overlapping range bins, where each range bin is an integrated sum of samples for the duration of the transmitted pulse width.

C Measurement ADC

- Performs the task of A/D conversion of $\Sigma_T(I, Q)$, $\Delta_{AZ}(I, Q)$, $\Delta_{EL}(I, Q)$ signals for tracking purposes.
- Contains analogue circuitry to integrate and hold returned signal into range gates for the duration of pulse before the A/D conversion.
- The measurement ADC is responsible for tracking a target with a 6.25 ns resolution using ‘range gates’. The ECL module which contains a 160 MHz clock, provides this accuracy.

D A/D Controller PCB

- Operates the Detection and Measurement ADCs.
- Synchronises the data sent to the arithmetic unit from the Detection and Measurement ADCs.
- The event controller operates the A/D controller.



Test Generator PCB

- Performs built in test to analyse and calibrate the analogue channels.
- Can perform tests in following modes:
 - Test Mode: offline testing of A/D, Arithmetic and Format Translation.
 - Normal Mode: real-time testing by injecting one PRI per Radar Frame and recording data.



Event Controller PCB

- Generates events or trigger pulses which:
 - Generate Radar Frames.
 - Control the A/D Controller PCB.
 - Communicates with test generator, time unit, display unit and microprocessor.
- It is activated when T_0 trigger (specific future time, generated by the Master Computer) is received from the time unit.



ECL Modules

Module A

- Contains the following:
 - 10 MHz clock reference.
 - 10 MHz to 160 MHz Phase-Locked Loop (PLL) to create fine time delay to position range gates in measurement A/D to within 6.25 ns.

Module B

- Contains only the clocks used in generating fine time delays.
- Used for positioning the test target pulse where required.

H Arithmetic Calibration PCB

- Performs I/Q Mismatch and DC offset correction by applying:
 - Scaling, gain correction, phase, and DC offset values to the integrated samples.
- Correction Parameters are calculated by analysis of an injection pilot pulse during the receiver's calibration.
- Corrected samples are sent to the format unit and output unit.

I Format and Output PCB

- Translates data into 32-bit floating point format.
- Sends data to the Master Computer via the HSDI.

J Time Unit PCB

- Used to interface the SVCU with External Standard Time Code Generator (STCG).
- Provides the T_0 trigger to the event controller.
- Provides the Single Board Controller with the absolute time of day to within an accuracy of $1\mu\text{s}$.

K Single Board Computer PCB

- It is an adaptation of the standard Intel Single Board Computer 86/12 (iSBC86).
- Receives its commands from the system computer via the Remote Terminal Unit (RTU).
- Decodes the messages into hardware controls and transfers them to the relevant SVCU unit.

L Panel Driver PCB

- Interfaces the front panel of the SVCU to the display unit.

M

Display PCB

- Interface between the radar and the A-scope display.
- Controls the front panel display functions.

N

Remote Terminal Unit (RTU)

- Interfaces the iSBC86 or the SVCU with the 1553 MUX Bus.
- Messages from the system computer are stored in the RTU memory which is read by the iSBC86 for each frame.

2.4 Re-Developed SVCU Architecture

This section discusses the re-development of the SVCU using commercial off-the-shelf (COTS) hardware based on the Field Programmable Gate Arrays (FPGA) and National Instruments' (NI) LabVIEW and LabVIEW FPGA software to meet the following:

- Specifications and requirements of the tasks carried out by the previous system.
- A prototype that fits into the R&D budget and plans of Radar Division at Denel OTR.

The architecture of the re-developed SVCU prototype comprises of the following hardware from National Instruments based on the PXI Express (PXIe) platform as shown in Figure 2.8 and Table 2.4 [15]:



Figure 2.8: Subunits of the new SVCU prototype

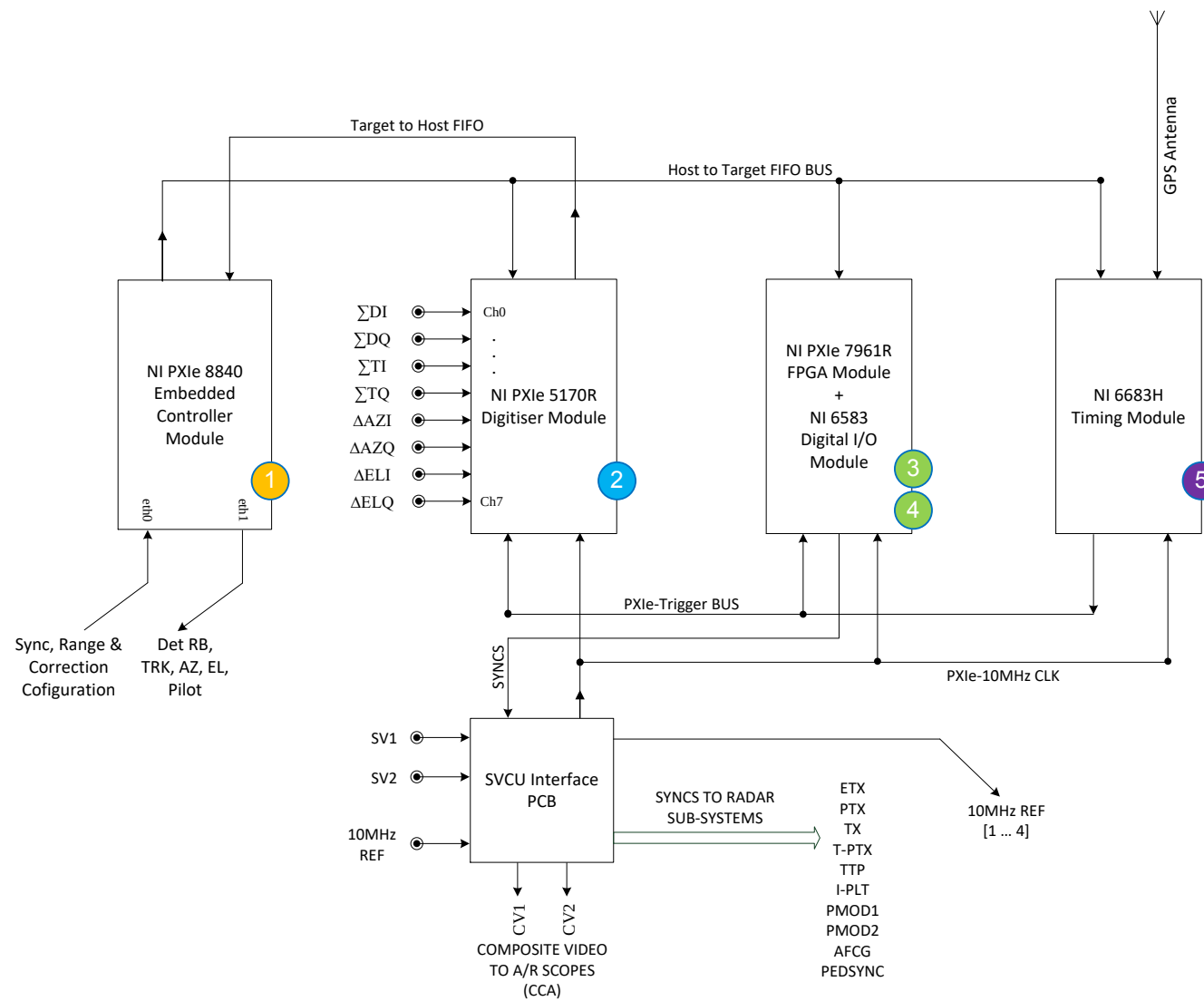


Figure 2.9: New SVCU general block diagram

Table 2.4: Modules of the PXIe based SVCU

	250 MS/s, 14-bit, FPGA based Digitiser Module
 	FPGA Module + High Speed Digital I/O Adapter
	GPS, IRIG-B, 1588 or PPS Timing and Synchronisation Module
 	Intel Core i5 Processor + PXIe Chassis

The subunits of the re-developed SVCU prototype and their functions are described below as per the block diagram in Figure 2.9.

2.4.1 PXIe Embedded Controller

The modules within the PXIe system must be loaded with a set of parameters to perform video signal processing and produce synchronisation triggers. The embedded controller communicates with the Master Computer to receive these parameters before the start of each execution cycle. Communication with the Master Computer is established via Ethernet using a static IP address and port using the UDP protocol. The specifications of the embedded controller are listed in Table 2.5 and all information exchange between the controller and the Master Computer is discussed below.

Table 2.5: Specification for NI-8840 embedded module

Model	NI PXIe - 8840
Maximum Clock	2.7 GHz
Memory	4 GB
Ethernet	2 Gigabit
Other Peripherals	2 $\times$ USB 3.0 ; 4 $\times$ USB 2.0

2.4.1.1 SVCU status to Master Computer

The SVCU status message, transmitted via Ethernet, to the main computer consists of 8 words representing the status of the SVCU and the time of the midpoint of the receiving frame [16, 17]. The message is sent upon start-up, on MCP request and at the end of each frame. The structure of the SVCU status message is shown in Table 2.6.

Table 2.6: SVCU Status to Master Computer

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word 0	ECHOED COMP MSG COUNTER								MESSAGE COUNTER							
Word 1	uSEC FIELD OF MID-RECEIVING TIME															
Word 2	NOT USED						M		NOT USED				MSB uSEC FIELD			
Word 3	SECOND FIELD OF MID-RECEIVING TIME															
Word 4	SVCU STATUS INDICATION															
Word 5	SVCU STATUS INDICATION															
Word 6	ERROR REASON CODE															
Word 7	SPARE															

 Not used in the new SVCU

2.4.1.2 SVCU configuration from Master Computer

This set of messages received from the system computer contains the configuration instructions required by the SVCU. The configuration message contains accurate information about the window where the signal must be digitised, digitised data correction factors and instructions about the syncs that need to be generated within the radar frame. These configuration messages are received as two different UDP packets as follows:

1. Instructions required to control the data acquisition process and events that need generation;
2. Factors used for correcting I/Q imbalance and DC offset within the receiving channels.

The structure of the configuration message is shown in Table 2.7, while its full contents are attached in Appendix A [17].

Configuration messages will reach the SVCU at an interval of 5-10 ms from the start of Signal Processing (SP) CYCLE (N+1)¹. The messages will be relevant for SP CYCLE (N+2). If correction factors are included, it will precede the new set of instructions.

¹For more information on Signal Processing Cycle of Denel OTR TR, please refer to ‘Study of Synchronisation and Video Conversion Unit’, by J Abrahams

Table 2.7: SVCU configuration message and correction parameters

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WORD 0	. MSG. COUNTER									FRAME WIDTH						
WORD 1	NUMBER OF FILLING PRI'S									NUMBER OF RECEIVING PRI'S						
WORD 2	PRI DURATION															
WORD 3	DETECTION FILTER WIDTH					TRACKING FILTER WIDTH			RANGE BIN WIDTH							
WORD 4	NOT USED					XMIT PULSE WIDTH			CODING							
WORD 5	DETECTION WINDOW AMBIGUOUS RANGE															
WORD 6	NOT USED												MSB OF TK.A.R			
WORD 7	TRACKER AMBIGUOUS RANGE (TK.A.R)															
WORD 8	TRACKER RANGE INCREMENT PER PRI															
WORD 9	NOT USED												MSB OF T.T.A.R			
WORD10	TEST TARGET AMBIGUOUS RANGE (T.T.A.R)															
WORD11	TEST TARGET INCREMENT PER PRI															
WORD12	SKIN TO BEACON DELAY															
WORD13	PILOT RANGE															
WORD14	MICROSECONDS FIELD OF ABSOLUTE TIME															
WORD15	NOT USED					M			NOT USED				MSB OF USEC FIELD			
WORD16	SECONDS FIELD OF ABSOLUTE TIME															
WORD17	MID RECEIVING FRAME OFFSET FROM TRIAL PULSE															
WORD18	COMMAND WORD 1															
WORD19	COMMAND WORD 2															

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WORD 1	MESSAGE COUNTER								PW (0-0.5US, 1-1.0US, 2-2.5US, 3-5.0US)							
WORD 2	PARAMETER E OF SUM (D)															
WORD 3	PARAMETER P OF SUM (D)															
WORD 4	PARAMETER A OF SUM (D)															
WORD 5	PARAMETER B OF SUM (D)															
WORD 6	PARAMETER E OF SUM (T)															
WORD 7	PARAMETER P OF SUM (T)															
WORD 8	PARAMETER A OF SUM (T)															
WORD 9	PARAMETER B OF SUM (T)															
WORD10	PARAMETER E OF DELTA (AZ)															
WORD11	PARAMETER P OF DELTA (AZ)															
WORD12	PARAMETER A OF DELTA (AZ)															
WORD13	PARAMETER B OF DELTA (AZ)															
WORD14	PARAMETER E OF DELTA (EL)															
WORD15	PARAMETER P OF DELTA (EL)															
WORD16	PARAMETER A OF DELTA (EL)															
WORD17	PARAMETER B OF DELTA (EL)															

2.4.1.3 SVCU Samples to Master Computer

A set of target data samples is sent to the Master Computer for each PRI within the receiving radar frame. In addition to this the SVCU status message, previously discussed in Section 2.4.1.1, is also forwarded to the MCP after the last PRI of the radar frame. These messages indicate the end of the current frame message and are used for error checking. The structure of data sent per PRI is shown in Table 2.8 [16].

Table 2.8: SVCU samples to Master Computer

32-bit floating point numbers	Number of samples
Detection sample pairs	40 Words
Target samples pairs	10 Words
Detection pilot sample pair	2 Words
Target pilot sample pairs	12 Words

2.4.2 Digitiser Module

The master computer instructs the SVCU to sample the signals in each of the receiver channels using a particular digitisation scheme. Samples acquired from the ADCs of the digitiser module are integrated in the FPGA into range gates equivalent to a filter matched to the transmitted pulse width [14]. The range gates are then corrected to eliminate mismatch between I/Q pairs during quadrature demodulation.

2.4.2.1 Search Window and Range Gates Samples

The I/Q bipolar video in the sum channel Σ_D is digitised into 20 overlapping range bins at the time corresponding to the search window (SMARK) of the TR [18]. The processed range bin size varies according to the transmitted pulse width.

The I/Q bipolar videos in the difference channels Δ_{AZ} and Δ_{EL} are sampled at the centre gate, which is the time corresponding to the estimated target range.

The I/Q bipolar videos in the sum channel Σ_T are sampled and integrated at three instances or range gates: early, late and centre. These range gates are used by the Master Computer to perform slant range tracking of the target. The sampled return signal is monitored by these gates in segments. The relative energy between early and late gates is used to position the target as closely as possible to the centre gate as illustrated in Figure 2.10 [19].

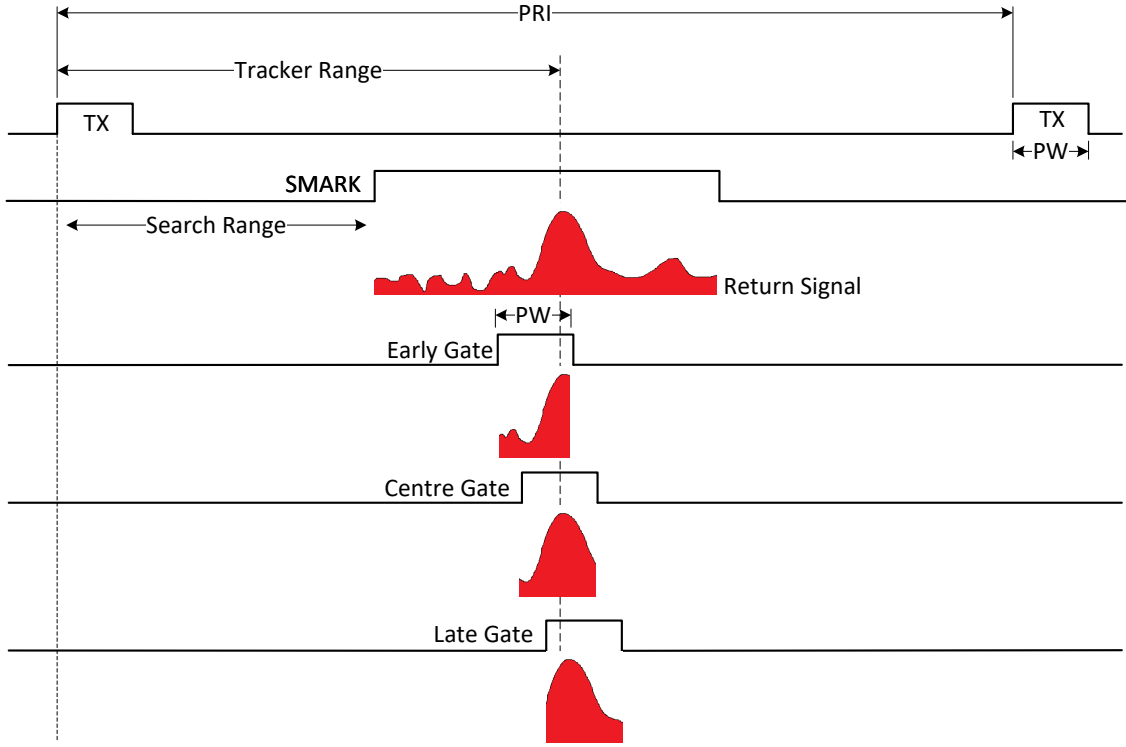


Figure 2.10: Search window and range gates

2.4.2.2 Matched Filtering

Match Filtering is a technique used in pulsed radars to detect a template or pulse of known shape in the presence of noise. It maximises the Signal to Noise Ratio. A matched filter that is matched to a known signal $s[nT_s]$ has the following impulse response:

$$h[nT_s] = s[T_M - nT_s] \quad (2.1)$$

Where, T_s is the sampling time and T_M is the duration of the known pulse template (symbol period). In theory, matched filtering is performed by either correlating a known signal (template) to a measured signal or convolving the received signal with a conjugated time reversed version of the known template. Range bins and gates are formed in the FPGA by summing of the digitised samples for the duration of the pulse width (transmitted pulse).

This integration of digital data over the duration of the pulse width is similar to correlating a received signal with a known waveform or template. This correlation maximises the SNR and is considered as an implementations of the matched filter [20, 9].

2.4.2.3 Data Correction

The correction performed on the samples in the detection and tracking channels are as follows [14, 21]:

$$Re'(t) = (Re(t) + a) \times \left(\frac{E + 1}{2} \right) \quad (2.2)$$

$$Im'(t) = (Re(t) + a) \times P + Im(t) + b \quad (2.3)$$

Where, $Re(t)$ = Real (I sample), $I(t)$ = Imaginary (Q sample).

Parameters a, b, E and P are the correction factors calculated by the system computer and perform the following corrections:

- E is the gain correction factor for the real part. It is sent as $\frac{E + 1}{2}$.
- P is the gain correction factor for the imaginary part.
- a and b are the DC offsets.

2.4.2.4 Sampling Rate and Triggering

The SVCU system has a fine clock or sampling resolution of 6.25 ns (see Section 3.3). This is due to the range where the master computer predicts the target lies and must be sampled using the range gates as specified by the master computer with a fine time resolution of 6.25 ns. To meet this requirement, the measurement PCB in the previous SVCU implemented analogue Integrate and Hold Circuits prior to digitisation. This analogue circuitry has been replaced by an equivalent digital integrator; sample resolution requirements are met by sampling the signals at the rate of 160 MS/s.

The 5170R digitiser module has a selectable input voltage range up to 5 V_{p-p} . The ADCs in the module are configured to run at a constant rate of 250 MS/s due to the dynamic input range. Digital correction is implemented when data is read from the ADCs into the FPGA [22]. Triggering occurs by means of a digital logic after digital correction and a Fractional Decimator is used in the FPGA to re-produce sampled data at the rate of 160 MS/s or sample resolution of 6.25 ns.

A brief functional diagram of the Digitiser Module is illustrated in Figure 2.11.

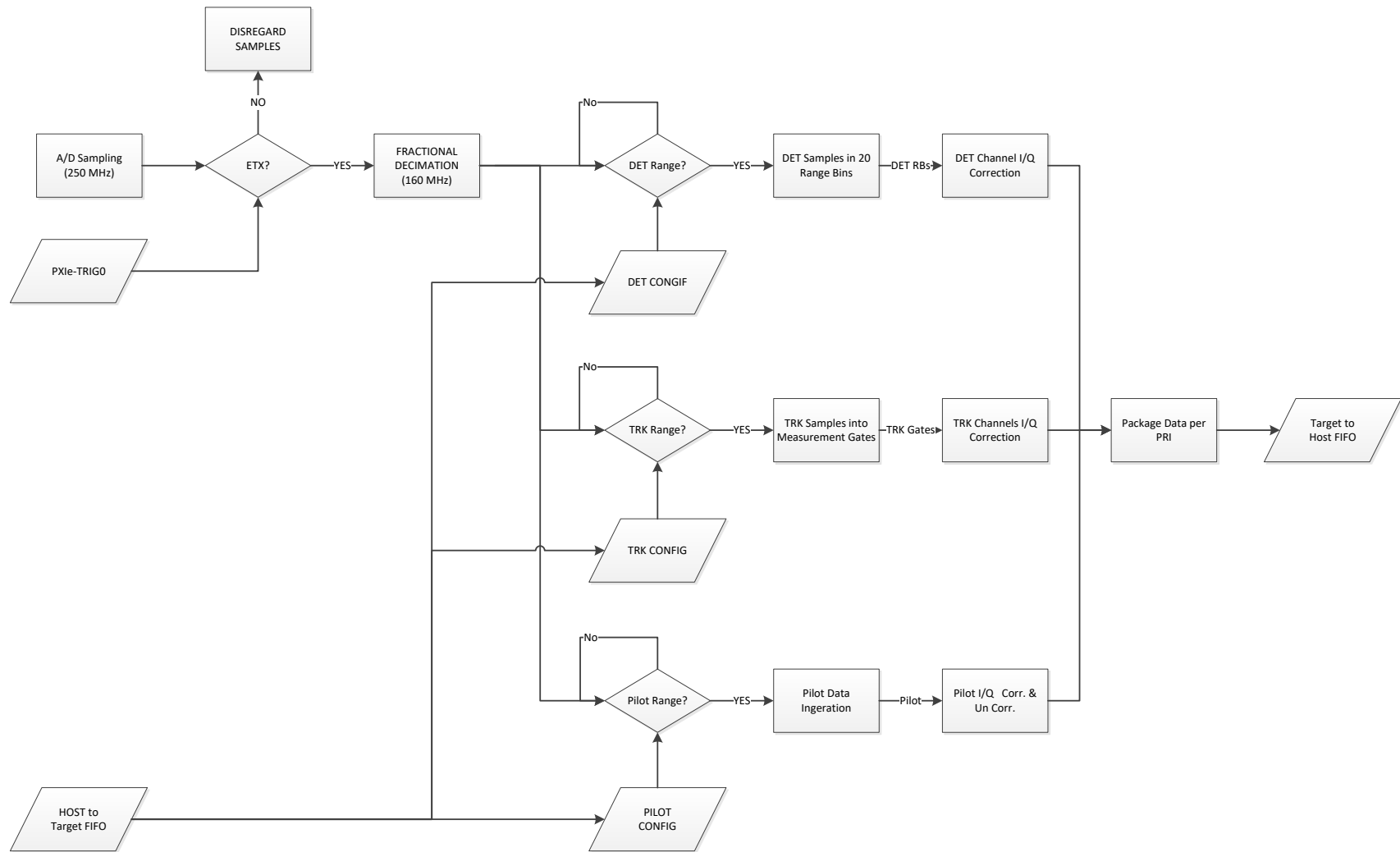


Figure 2.11: Digitiser module process diagram

2.4.3 Reconfigurable FPGA module

The NI FlexRIO 7161R module, referred to as a sync module, is used to generate all timing within the radar frame called syncs. Their purpose is synchronisation to a very high degree of precision. Even though the syncs are digital in nature, the analogue properties of these sync pulses such as absolute position, duration/width, transition times, and jitter are of utmost importance. To meet these requirements, the 6583 High-Speed Digital I/O (HSDIO) adapter module is interfaced with the FlexRIO module as shown in Figure 2.12 [23], which provides us with the required high-performance and custom control of digital I/O lines and ensures accurate generation of digital signals up to 200 MHz.

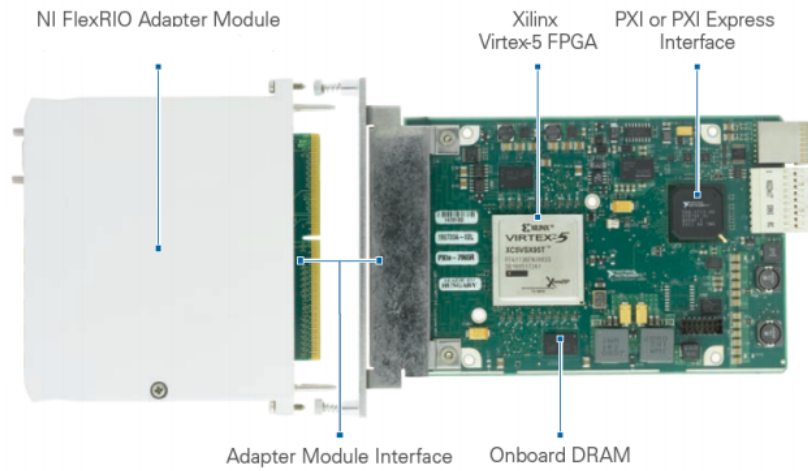


Figure 2.12: NI FlexRIO module

The combination of the FlexRIO module and HSDIO module is used to generate deterministic, multichannel custom triggers for low-latency sequencing of tasks. A functional diagram of the process is shown in Figure 2.14. The signals are distributed within the subunit of the TR as per Figure 2.13 and detailed in the following subsections [16]:

2.4.3.1 Critical signals

Critical signals are associated with signals used for RF energy transmission, as well as references for all other events being generated. These signals have very low transition times, typically less than 10 ns. The interface circuit (Section 2.4.5) needs to meet the jitter requirement of less than 1 ns. These signals need calculation and analysis of the transmission line and delays. The signals are individually analysed and tuned to meet the performance specification.

Transmit Trigger (TX): RF energy transmission occurs in the transmitter on the rising edge of this trigger. All timing within a PRI is referenced to the rising edge of the TX

sync. The time between two consecutive TX rising edges is known as the PRI.

2.4.3.2 Long line signals

These signals are syncs that need to travel over excessively long transmission lines, e.g. Calibration tower signals. The delay in transmission needs to be compensated. These signals are used for synthesising test target pulses with Doppler for calibrations.

Test Target Pulse (TTP): This pulse is used for modulation of a continuous wave radio frequency (CWRf) into a synthesised Pulsed target, including Doppler.

2.4.3.3 Standard signals

These signals are syncs used for synchronisation of various subsystems of the TR, that have a required transition time of less than 100 ns and jitter of less than 50 ns.

EARLY Trigger (ETX): It is used for resetting counters when new instructions are received at the beginning of a new frame.

Temporary Pre-Trigger (T-PTX): The T-PTX is used to initiate a trial PRI. A trial PRI is used to perform automatic gain control (AGC) in the radar receive channels.

Pre-Trigger (PTX): This pulse is an envelope of the transmission synthesiser.

Search Marker (SMARK): The SMARK indicates the start of the search window.

Automatic Frequency Control Gate (AFCG): This is used to track the beacon frequency and monitor the drift on the Voltage Controller Oscillators with respect to the beacon frequency.

Inject Pilot (I-PLT): This pulse is a trigger to inject a pilot signal in the received signal.

Pilot Modulations (MOD): These are used to set the phase of the pilot signal.

Pedestal Sync (PSYNC): The pedestal sync is generated to indicate the middle of the measurement interval and synchronise the pedestal sensors (Azimuth, Elevation).

2.4.3.4 Real Time Clocks

The module produces three real-time synchronised clocks at 5 MHz, 50 Hz, and 1 Hz. The rising edge of these clocks are synchronous and the frequencies of the clocks are synchronised to the absolute time of the day.

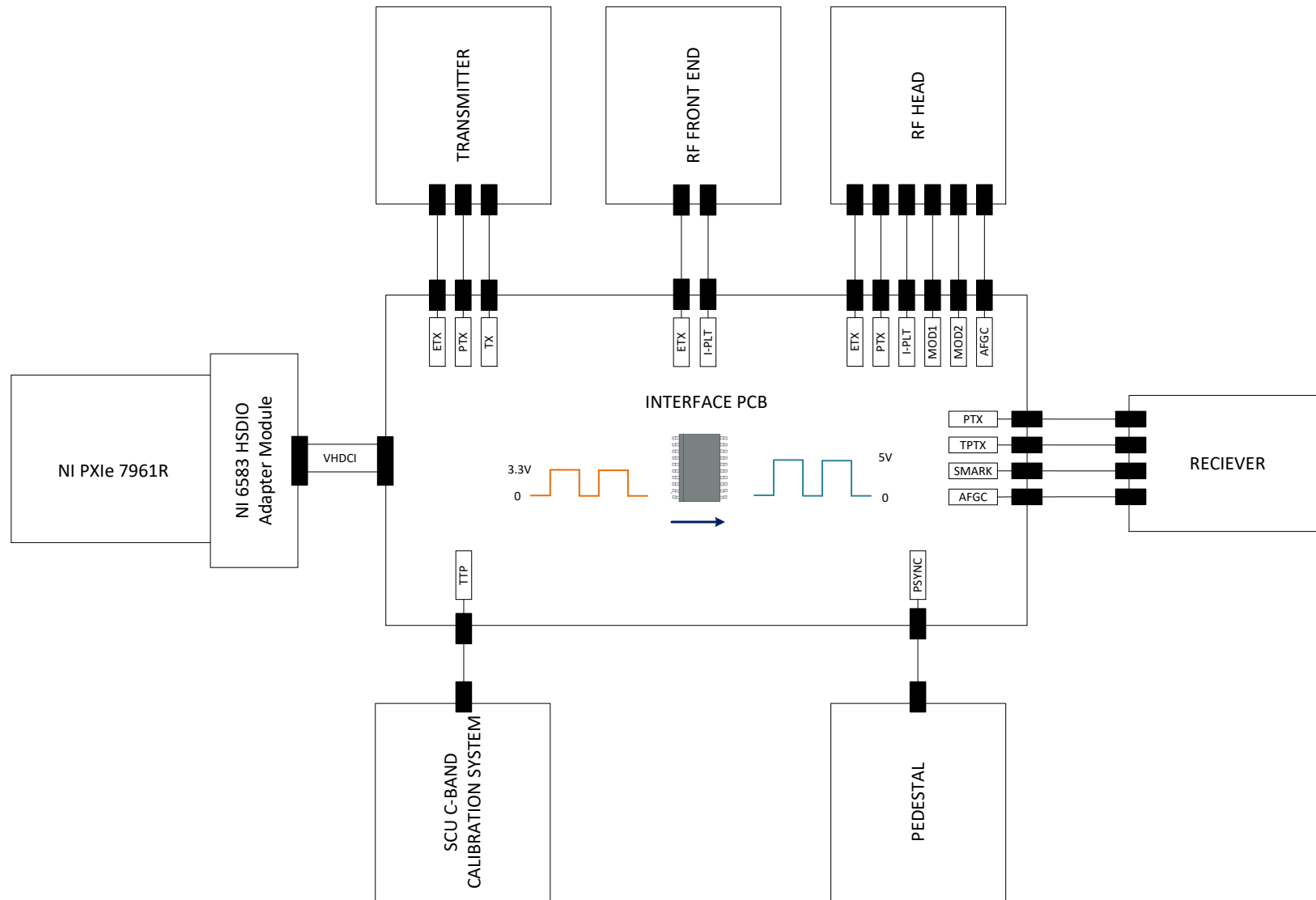


Figure 2.13: Sync distribution: TR subsystems

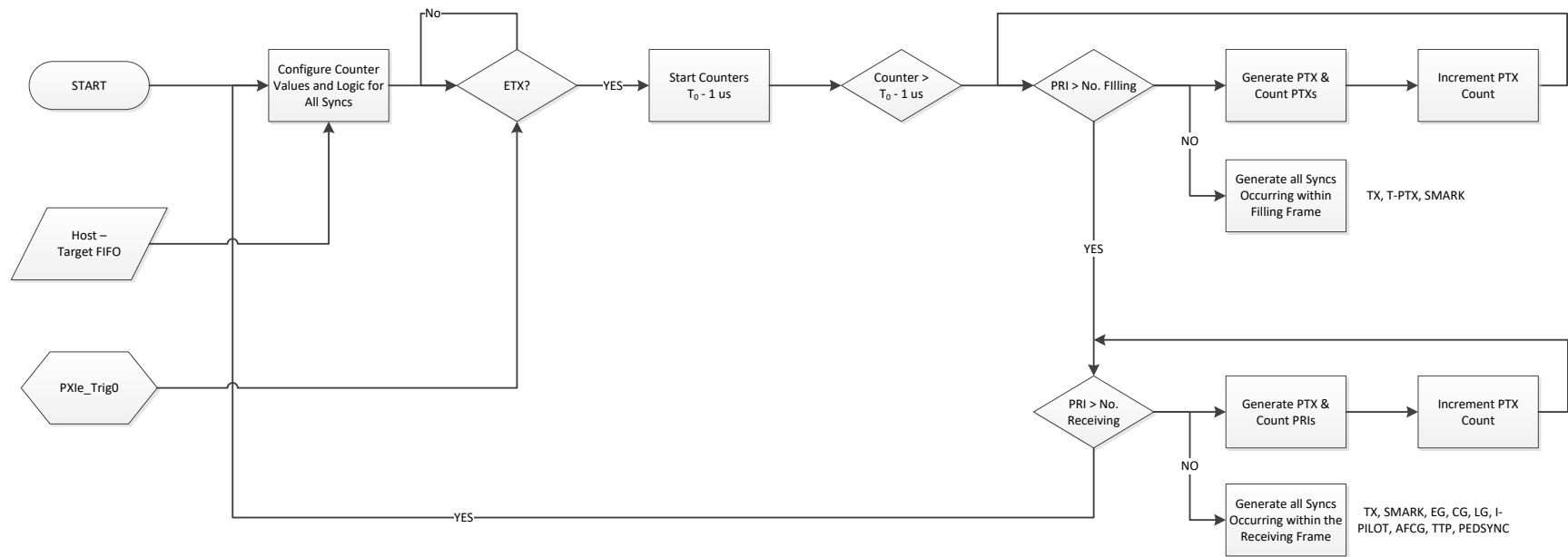


Figure 2.14: SYNC generation process diagram

2.4.4 Timing Module

Upon receiving the parameters from the master computer on how to execute the baseband video signal processing, generate timing signals within the frame, and when exactly to execute these tasks, the SVCU also needs to know what the current time is. The 6683H module receives the current time of day using GPS. The uses of this time within the SVCU is implemented in the 6683H module (Figure 2.15) as follows [24]:

2.4.4.1 Timebase

The PXI-6683H consists of an onboard TCXO that is disciplined to GPS. The module is used to keep a reference timebase to execute all future timing events and provide synchronised clocks to various subunits of the TR.

2.4.4.2 Event Generation

The PXI-6683 with its synchronised timebase is used to generate the T_0 event and clock signals at an arbitrary future time as specified by the master computer. The signals or triggers are then routed through the PXI chassis backplane with minimal skew. This event initiates all video processing and sync generation within the digitiser and sync modules.

2.4.4.3 Time Stamp

The timing module can also be configured to timestamp input events with its synchronised system time. A sync generated in the middle of the measurement interval is routed to the Timing Module which generates a timestamp. This timestamp is sent to the master computer which uses it to synchronise the pedestal sensor (AZ, EL) and read the encoder values.

2.4.4.4 Backplane Trigger Routing

The $1\ \mu\text{s}$ pulse is generated when the current time reaches the T_0 start time, as discussed above. The 6683H module then routes this pulse to the backplane or PXIe_Trig0 in the trigger bus. This PXIe_Trig0 is then accessible to both the FPGA modules used and acts as a reference to start all processes. Additional trigger lines to and from the backplane can be routed to the 6683H module to initiate an isolated event or be used to timestamp random events for diagnostic purposes.

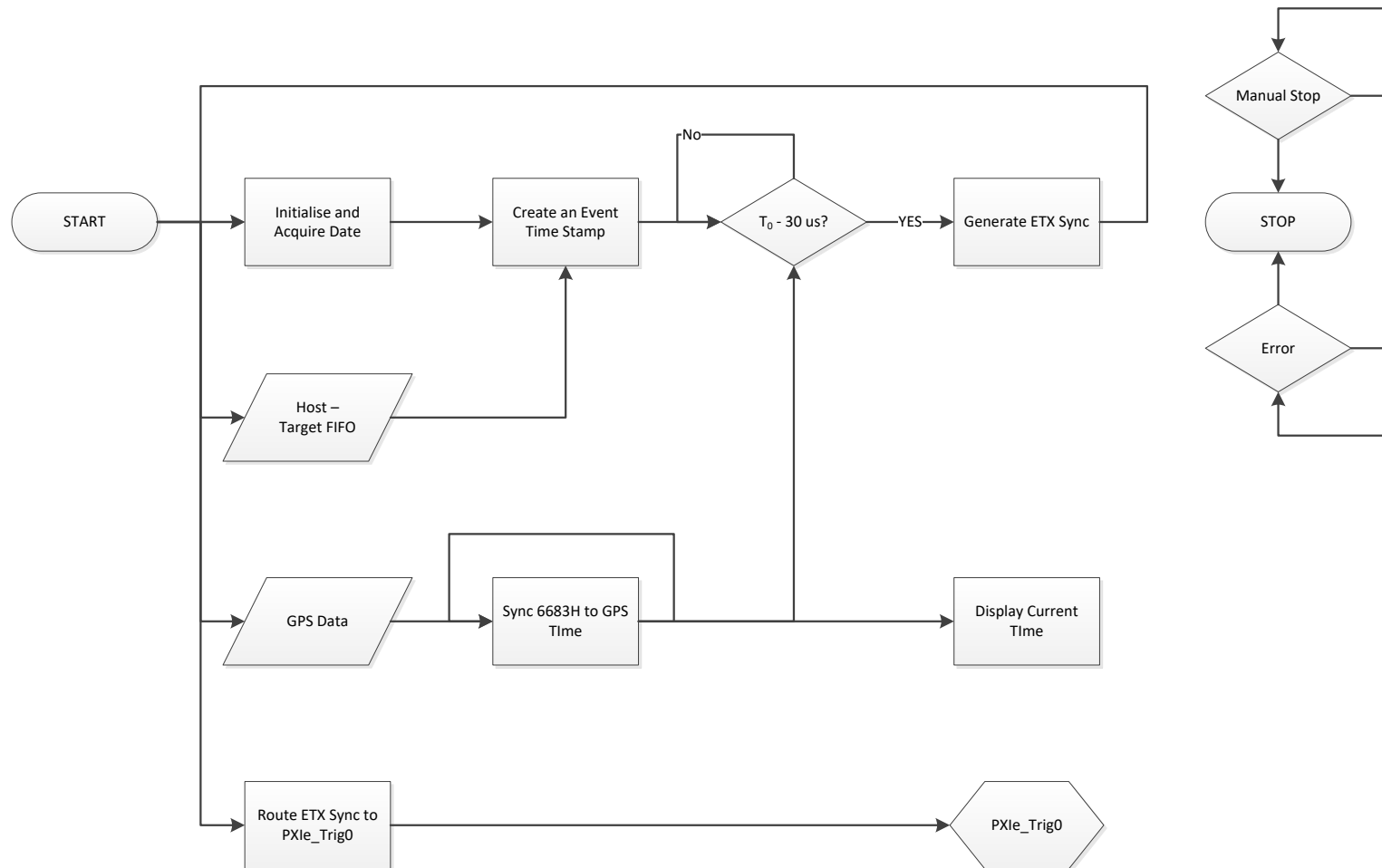


Figure 2.15: Timing module process diagram

2.4.5 Interface PCB

The Interface PCB is created to perform voltage level translation, buffering and signal conditioning of the output signals to meet the requirements of the various receiving sub-units of the TR. An electrical circuit in the crowbar setup is designed to supply power to all discrete components of the PCB to prevent an overvoltage condition of a power supply unit from damaging the circuits attached to the power supply. The PCB was designed using Altium CAD software as shown below in Figure 2.18. The schematic of the PCB can be found in Appendix B.

2.4.5.1 Composite Video

Within the radar Command and Control Assembly (CCA), there exist two analogue A/R scopes. These A/R scopes, whose displays is shown in Figure 2.16 [25], allow the operator of the radar to view the raw video or composite video (skin/beacon) with superimposed trigger and marker pulses. This effectively provides a real-time visual feedback to the operator, and also allows one to lock onto a target by manually positioning the target into the centre gate. The triggers and marker pulses are superimposed on the raw video using a circuit designed in the Interface PCB as shown in Figure 2.17. These circuits are illustrated and described in detail in Section 3.7.

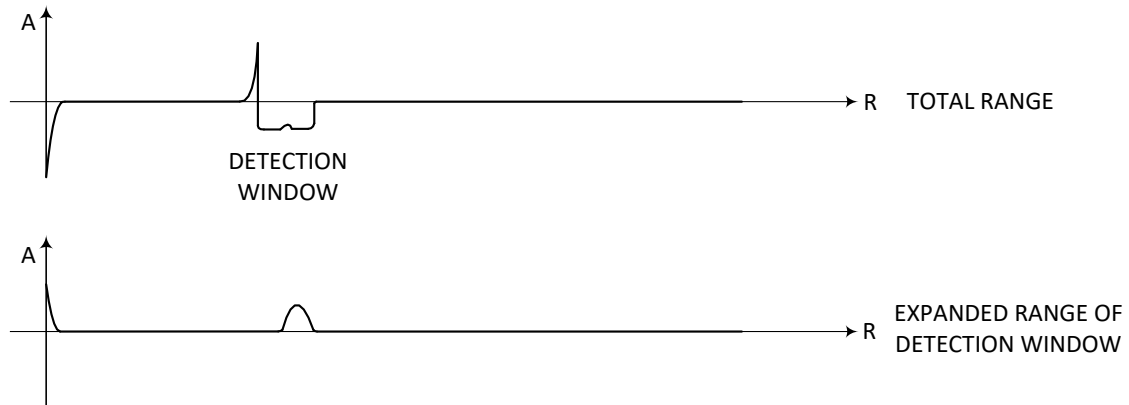


Figure 2.16: A/R display

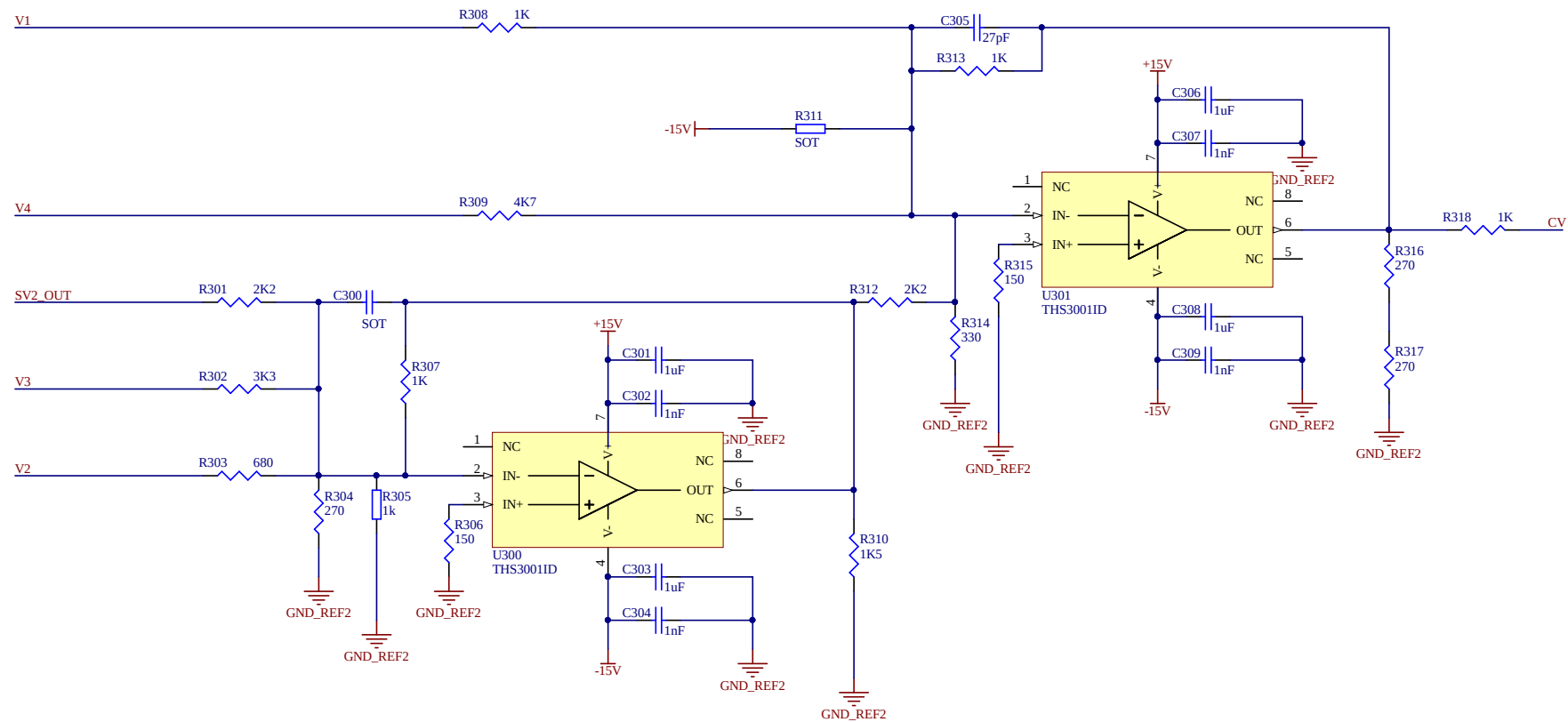


Figure 2.17: Composite video generator

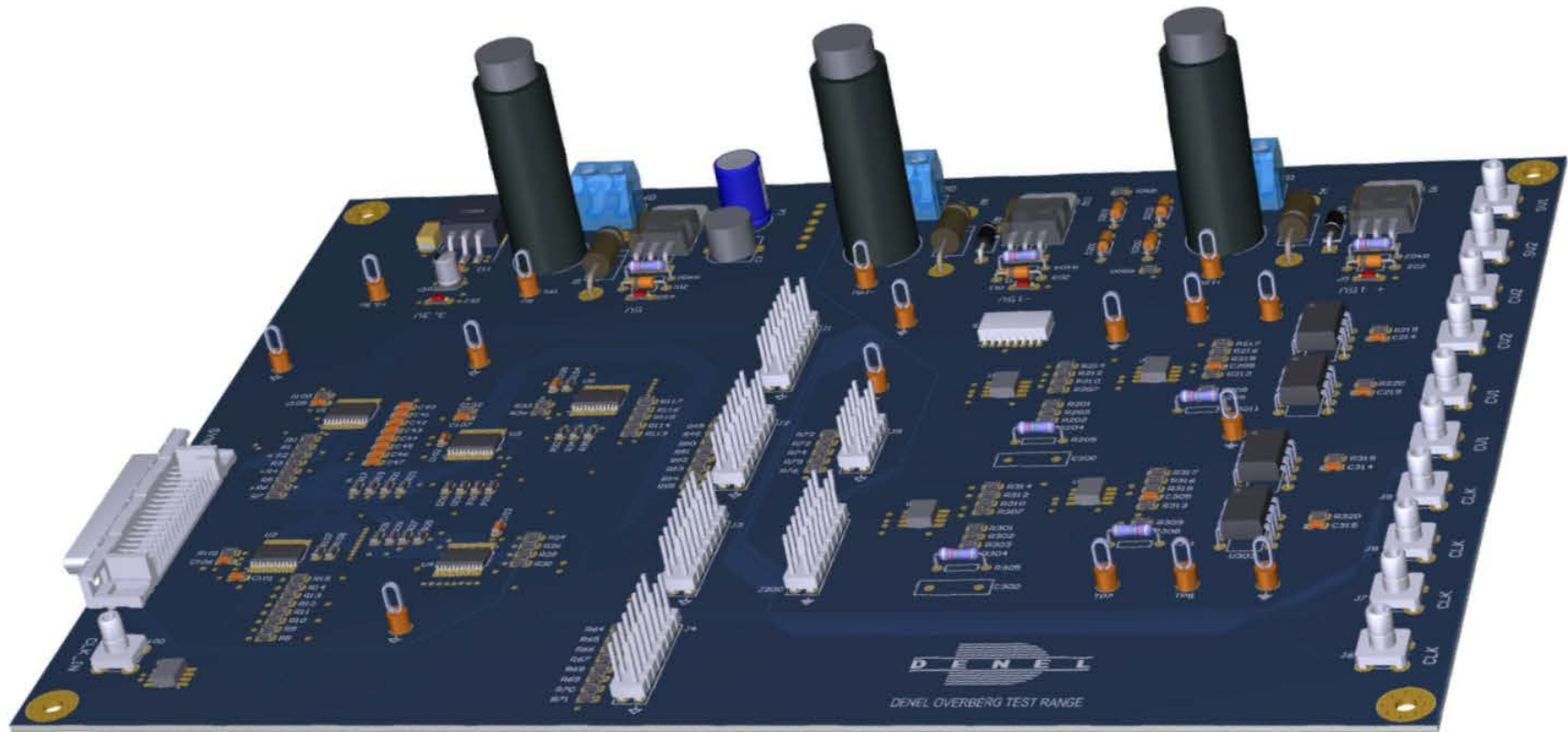


Figure 2.18: Interface PCB

2.4.5.2 Voltage Level Translation

The Digital I/O adapter used on the 7191R Module, which is used for generating syncs and clocks, is able to output signals in two formats: single ended and LVDS via a Very High Density Connector Interface (VHDCI) or Infibus respectively. The receiving subsystems of the tracking radar expects the signal in a 0 to 5V level. Although there are plans to change this interface in the future, it is outside the scope of this project. Therefore all syncs coming out of the digital I/O adapters have been level shifted using ultrafast GTL201PW level translators with propagation delays of less than 250 ps [26].

Level translation circuitry as shown in Figure 2.19 is implemented in the interface PCB (See Appendix B for detailed schematic layout). All individual signals are impedance matched to minimise signal reflection from the various destinations. Provisions have been made to solder select-on-test capacitor to each signal to decouple signals individually if necessary.

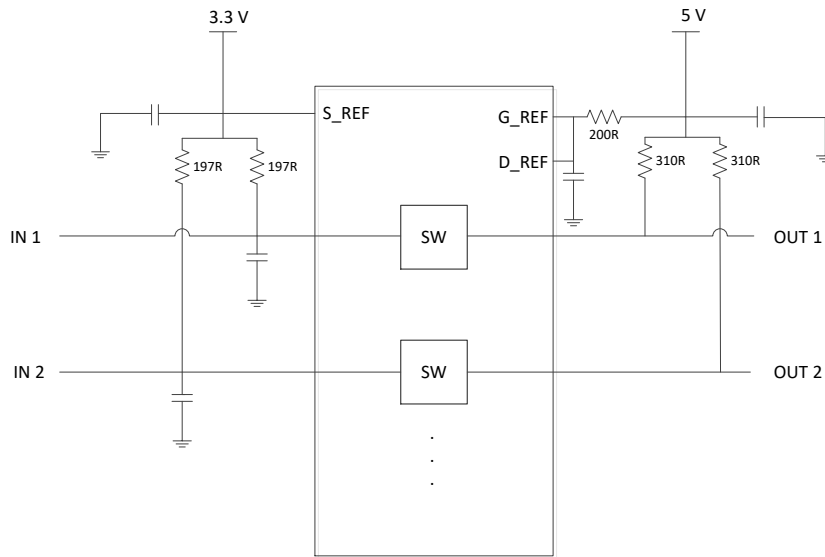


Figure 2.19: Level translator

2.4.5.3 Clock Buffering

The 10 MHz TTL clock, which is a derivative of the 120 MHz master clock, is used as a reference clock to synchronise all modules within the new PXIe SVCU system. This signal is provided by the RF Head and is only available at one output connector. Furthermore, the output has a low fan out, i.e. distributing the signal to various locations effectively

loads the signal. Therefore the clock is buffered using the ON Semiconductor NB3N551 series PLL based zero delay buffer to make it available for multiple distributions. The functions the PCB Interface card performs is summarised into a process diagram below in Figure 2.20.

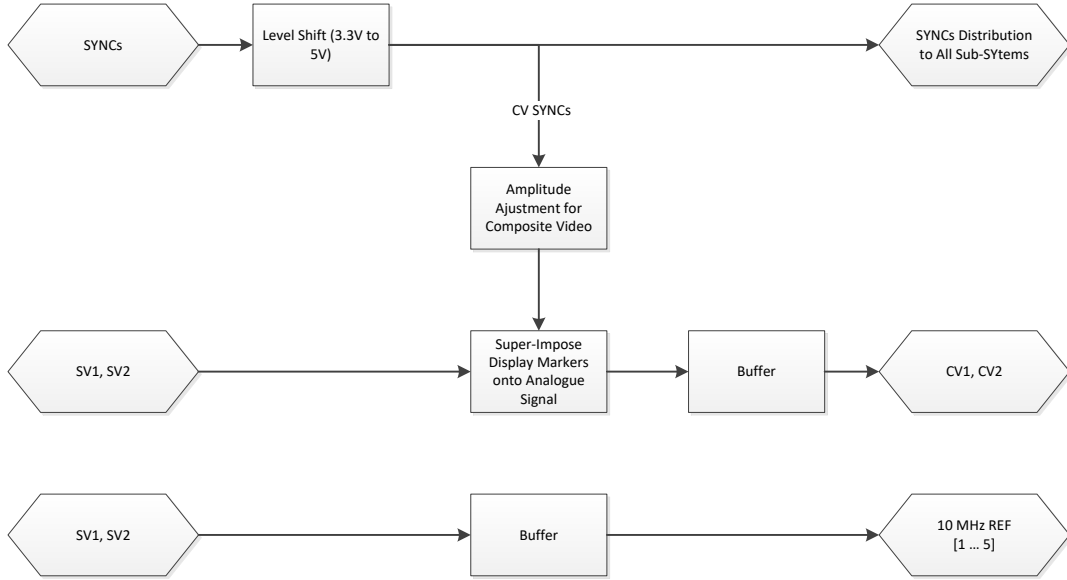


Figure 2.20: Interface PCB process diagram

2.5 Summary

A brief introduction of Denel Overberg Test Range and the Tracking Radars was given. An introduction to the original SVCU and a functional description of the new SVCU prototype was then presented.

An echo signal reflected from the target is fed into the monopulse comparator assembly in the antenna feed consisting of a waveguide network, which form the Σ , Δ_{AZ} , and Δ_{EL} channels. The receiver subsystem architecture of the TR consist of a two stage heterodyne configuration and a quadrature demodulator. The signals are further split into various channels during the down conversion and demodulated into 5 I/Q baseband video pairs. These channels are digitised and processed in the SVCU, into range bins and range gates for detection and tracking purposes. Additional to this, timing signals are generated in the SVCU at a specific future time provided by the Master Computer, to synchronise all subsystems of the TR. The next chapter discusses the video processing scheme in detail and critical aspects of the timing in the SVCU.

Chapter 3

Revised Timing and Data Processing Requirement

As previously discussed, the documents and specifications related to the SVCU are restricted to a general description, concepts and theory. On a system level this may not be a major issue, but on a lower design level, this creates limitations on the re-development process. All the specifications and properties have to be thoroughly verified against the proposed concept document that was created before the initial development of the SVCU. The Tracking Radar has also gone through many re-development and modernisation projects over the years, which has made functions that were crucial once, irrelevant now.

This chapter discusses all the synchronisation pulses and video baseband processing in the SVCU. The synchronisation generated and data processing functions within the existing SVCU were measured and analysed. The results were compared to the values mentioned in the proposed design specifications to find similarities and differences. A comprehensive set of revised specifications was then compiled for the new SVCU prototype.

3.1 Radar Frame

A radar frame can be described as multiple pulses transmitted at a constant frequency in an anticipation to receive feedback and ensure a meaningful response [27]. The TR system can be configured to operate in three different modes with pulse width durations of 0.5, 1.0 or 2.5 μs . The interval between two consecutive pulses is described as the Pulse Repetition Interval (PRI). Thus, The Pulse Repetition Frequency (PRF) can be formulated as:

$$PRF = \frac{1}{PRI} \quad (3.1)$$

In the case of the OTR TR, these frames are further divided into three subsections named pre-frame, transmit and receive frame [18, 17], illustrated below in Figure 3.1:

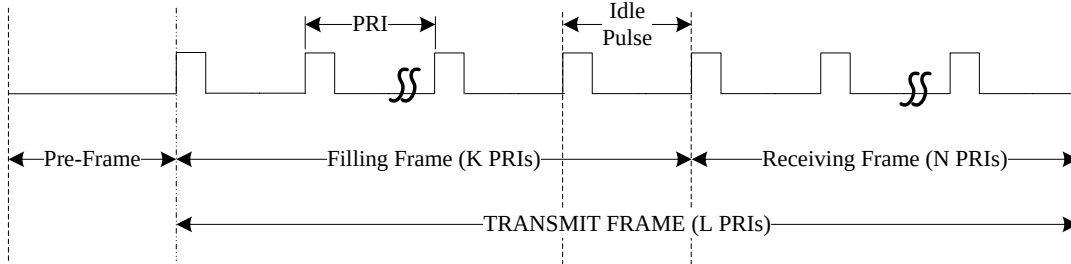


Figure 3.1: Radar frame composition

Pre-Frame

This section contains trigger signals described as pre-frame triggers used to reset counters and initiate updating of parameters in preparation of new timing signals to be generated by the SVCU.

Filling Frame

The filling frame consists of timing signals generated for a group of K Pulses:

$$1 \leq K \leq 32$$

The value for K is set in the MCP1_WORD1 (See Appendix A) of the Configuration Message sent to the SVCU from the Master Computer. The filling pulses ensure the following [1]:

- The transmit frame meets the minimum frame length (in milliseconds)
- Incorporate an idle pulse in the filling frame to measure signal strength and control the attenuators
- All pulses transmitted in the receiving frame returns meaningful echoes from target

Receiving Frame

The receiving frame consist of timing signals generated for a group of N Pulses:

$$1 \leq N \leq 32$$

The value for N is set in the MCP1_WORD2 (See Appendix A) of the Configuration Message, as described under Filling Frame.

Within the PRI and subsequently the radar frame there exists timing signals used for synchronisation of all subsystems of the TR. They are categorised under two main functions [17]:

1. **Operations and Calibration:** Triggers associated with transmitting, synchronisation of all subsystems and Injection of Test Pulses for Calibration and Error Correction. These triggers are defined as syncs external to the SVCU.
2. **Data Processing:** Triggers associated with Sampling for Detection, Tracking and Calibration. These are defined as syncs internal to the SVCU.

Timing parameters of the existing system were verified using a logic analyser against the system documents that were compiled before the original SVCU was developed. The critical signals (e.g. TX Sync) were furthermore observed using an oscilloscope with a high sampling rate to look at the analogue properties of the pulse. The inconsistencies between the specification and measuring were identified in Table 3.1 and categorised as follows:

	Parameters inconsistent with original specification
	Parameters not specified in the System Documents
	Sync not used in the current SVCU

The inconsistencies identified warranted the creation of a new list detailing signal descriptions, critical parameters, and timing diagrams for all the synchronisation pulses that are currently in use by various subsystems of the radar.

Table 3.1: Detailed List of syncs and irregularities

Syncs	Location	Occurrence	Pulse Width	
			Skin	Beacon
ETX	T ₀ + 1 μs	Once Before TX	1 μs	
PTX	T ₀ + 1 μs	For all F + M PRIs (Radar Frame)	5.2 μs	5.2 μs + (Beacon Code - 1) μs
TX	ETX + 30 μs	For all F + M PRIs (Radar Frame)	0.5 μs	500 μs & 2.7 μs
T-PTX	ETX + 30 μs	Last Pulse of Filling Frame (Trial Pulse)	3.7 μs	3.7 μs + (Beacon Code - 1) μs
SMARK (Detect)	MCP1W5	For all F + M PRIs (Radar Frame)	As Specified in MCP1W3B8:15	
ECL GATE (Track)	MCP1W6+7	For all M PRIs (Receiving Frame)	As Specified in MCP1W3B8:15	
PPLT	Not Used			
IPLT	MCPW13	Receiver Frame (Every TX)	5 μs	
PMOD 1		Continuous Pulse Train	Toggle Every Falling Edge of PTX	
PMOD 2		Continuous Pulse Train	Toggle Every 2nd Falling Edge of PTX	
PTTP	Not Used			
TTP	MCP1W9+10	Receive + Filling Frame as specified in MCP1W4B4:7		
AFGC	MCP1W6+7	Centre Gate for M PRIs (Receiving Frame)	0.3 μs	
Pedestal Sync	MCP1W17	Once in the Receiving Frame	5.0 μs	
ETOS SYNC	Not Used			
ETOS ASYNC	Not Used			

3.2 Critical Properties of TR Sync Pulses

All Sync outputs from the SVCU are described as digital pulses. Since these syncs are meant to be of high precision and contribute towards the proper operation of the TR system and accurate measurement, analogue properties have to be considered, such as [18, 16]:

- Amplitude corresponding to high and low logic state.
- Absolute time relative to a reference where the trigger occurs.
- Width of the trigger pulse.
- The time it takes for the state to change from low to high and vice versa.
- Uncertainty in the absolute position of the trigger.

Levels The digital signals are of TTL levels, which range from 0 to 5 V. Where, $V_{\text{on}}(\text{min}) = 2.4 \text{ V}$ and $V_{\text{off}}(\text{max}) = 0.4 \text{ V}$ under load conditions. The properties are illustrated in Figure 3.2 [16] below:

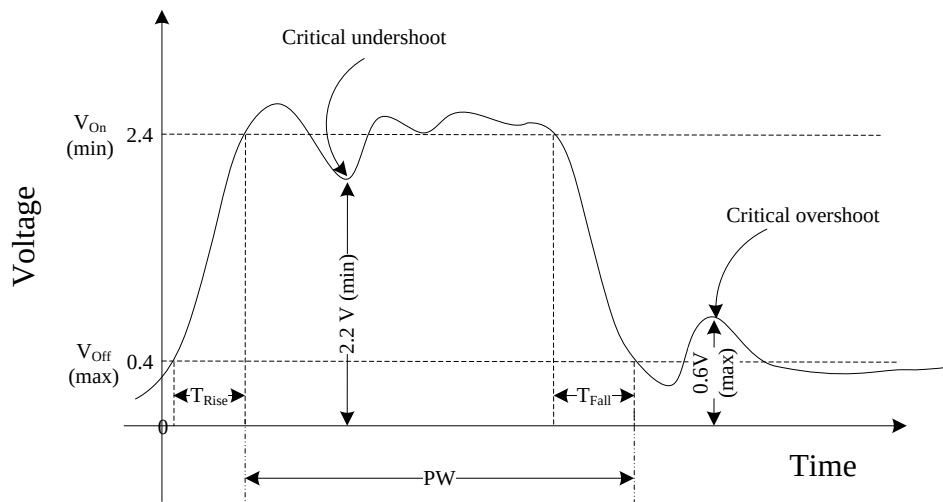


Figure 3.2: Critical properties of a sync pulse

Transition times The T_{Rise} and T_{Fall} times of the sync pulses, measured across the transmission line, is required to be less than 100 ns for standard signals with normal cable lengths up to 15 meters. Long line signals that are sent to the calibration tower need to be compensated through calibration to achieve this standard transition time. Critical pulses have a required transition time of less than 10 ns.

Overshoots and undershoots (amplitude fluctuation) Transmission circuits have been designed with characteristic impedance matching to minimise overshoot or undershoot [28]. However, occurrences due to fast transition must be less than 10 % of the voltage step (2 V). This is illustrated in Figure 3.2 [16].

Uncertainty ‘Uncertainty’ is defined as a random fluctuation in the position of the pulse edge, as shown in Figure 3.3 [16]. The main contributing factor in this jitter is due to the reference clock used to generate all syncs or events. There is a stringent requirement of maximum 1 ns jitter for generation of syncs required for RF Transmission, digitisation, and integration of return signal into range gates for tracking.

Jitter contributed by pulse transmission Transmission circuits designed to distribute syncs to all subsystems of the TR can introduce additional jitter. Total jitter (root-sum-square), contributed by the generation of syncs, transmission circuitry, A/D conversion, and integration into measurement gate must not exceed 30 ns for the TR to operate within the specified accuracy. This is discussed in detail in Section 5.7.

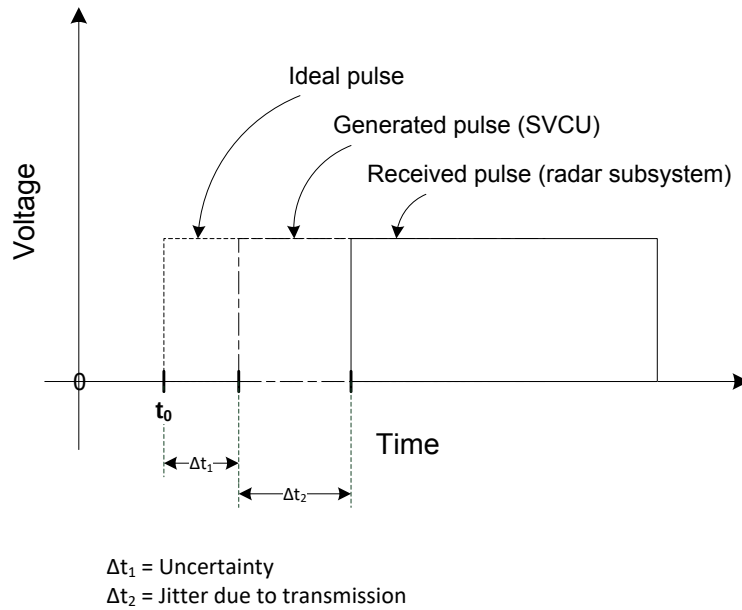


Figure 3.3: Jitter in digital pulses

3.3 Data Acquisition within TX Interval

The synchronisation of data acquisition within the TX interval constitutes the process of digitisation of data, range bin segmentation for detection, and range gate integration for tracking purposes. Samples are gathered at the position detection range, tracking range and pilot range as per Figure 3.4 [1]. The method and requirement for processing the digitised samples into range bins and gates are discussed in detail in Section 3.5 and Section 3.6.

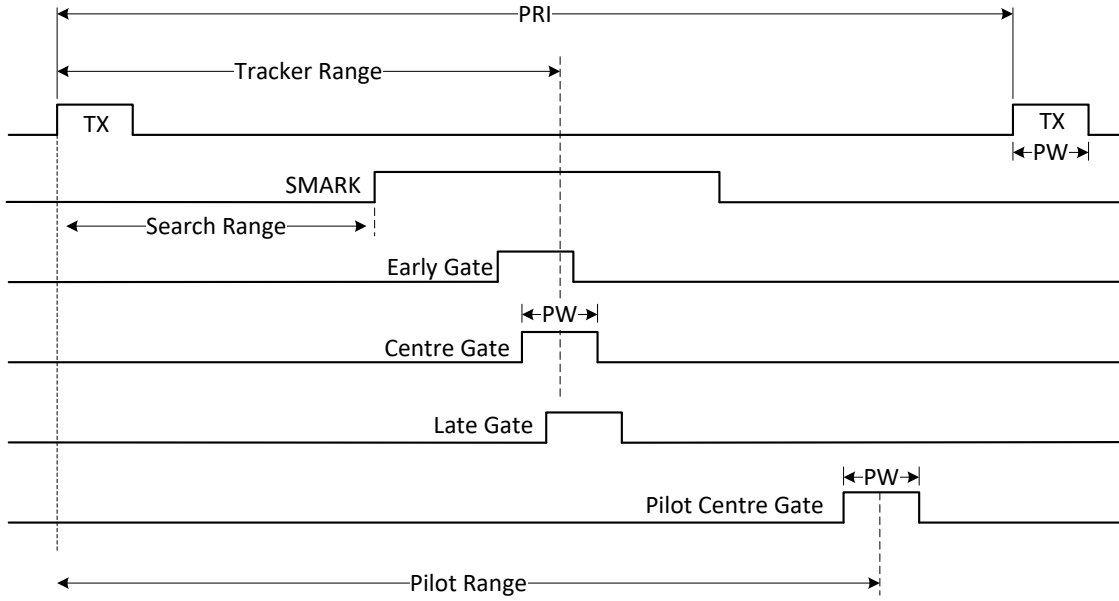


Figure 3.4: Triggers internal to the SVCU

Early, Centre and Late Gates (EGT, CGT, LGT)

Used for digitisation and summation of signals in the tracking channels. The gates are utilised by the master computer to perform slant range tracking [1].

Pilot Center Gate (PCGT)

PCGT operates in a similar fashion to CGT in the tracking channels. It is used for sampling of the injected Pilot signal for I/Q correction.

Search Window (SMARK)

Used for digitisation and processing of samples into 20 range bins. These range bins represent the search window for target detection.

3.4 Description of Syncs external to the SVCU

Early Trigger (ETX)

This is the first trigger signal in the Radar Frame, generated by the SVCU. This signal precedes the start of the Transmit Frame. This trigger is used to reset all counters for the frame, sweep buffers, update parameters and prepare for a new cycle of frame generation. The properties of ETX are listed in Table 3.2.

Table 3.2: ETX properties

Timing		
	Occurrence	The ETX pulse only occurs once per radar frame.
	Position	1 μ s after the T_0 time specified in the configuration message and 30 μ s before the start of the filling frame (first TX).
Properties		
	Transition	Standard.
	Width	1 μ s for all mode of operation
	Jitter	Standard.
Transmission		
	Receiving Unit	Transmitter, RF Front End, RF Head, and the Receiver.

The Radar System computer only generates requests for new frames (former continuous frame mode is no longer used). Therefore, a new requirement for ETX is that it must occur once on every transmit frame generated.

Pre-Trigger (PTX)

This trigger is the envelope of the transmission synthesiser excitation. The leading edge of PTX can be defined as the PRI as it always precedes the TX by 1 μ s. However, all timing within a PRI is relative to the leading edge of the TX trigger.

In 1996, the PTX width was altered due to a modification in the modulator situated in the transmitter. The properties of PTX, as listed in Table 3.3 were derived from this modification.

Table 3.3: PTX properties

Timing		
	Occurrence	PTX is present in every PRI in the radar frame: K PRIs (Filling Frame) set by MCP1W1B0:7 and N PRIs (Receiving Frame) set by MCP1W1B8:15.
	Position	Precedes the TX sync by 1 μ s.
Properties		
	Transition	Standard.
	Width	Skin Mode - 5.2 μ s wide;
		Beacon Mode - 5.2 μ s + (Coding - 1) μ s
	Jitter	Standard.
Transmission		
	Receiving Unit	Transmitter, RF Head, and the Receiver.

Transmit Trigger (TX)

The leading edge of TX results in RF energy transmission. All timing within the PRI is specified with reference to the leading edge of TX.

Table 3.4: TX properties

Timing		
	Occurrence	TX is present for every PTX that is generated for filling and receiving frame.
	Position	Skin Mode: 1 μ s after the PTX;
		Beacon Mode: Second Pulse (1-12) μ s from the leading edge of the TX as specified by MCP1W4B8:15;
Properties		
	Transition	Rise and fall time of 10 ns.
	Width	Skin Mode: 0.5 μ s.
		Beacon Mode: Second Pulse of 2.7 μ s width.
	Jitter	Jitter of less than 1ns.
Transmission		
	Receiving Unit	Transmitter.

The timing properties and functionalities specified in the development specification differed from the measured signal during the operation of the radar. A new set of properties (Table 3.4) generated for the TX Sync is based on the observation and measurement made while operating the TR in various modes.

Temporary Pre-Trigger (T-PTX)

The T-PTX is used to signal a trial PRI, defined as the last PRI in the filling frame. A trial PRI is used to perform automatic gain control (AGC), which is a process where a power measurement is taken and settings for attenuation is configured to prevent saturation conditions. The T-PTX resets the attenuation control and a new measurement of signal strength is taken.

Table 3.5: T-PTX Properties

Timing		
	Occurrence	Once per filling frame.
	Position	Coincides with the leading edge of last PTX of the filling frame also known as Trial PRI.
Properties		
	Transition	Standard.
	Width	Skin Mode : $3.7 \mu\text{s}$;
		Beacon Mode: $3.7 \mu\text{s} + (\text{Coding} - 1) \mu\text{s}$
	Jitter	Standard.
Transmission		
	Receiving Unit	Receiver.

After measurement of T-PTX pulses for all modes of operation, a new specification was identified as per Table 3.5. In skin mode, T-PTX is $3.7 \mu\text{s}$ wide. In beacon mode, T-PTX is $3.7 \mu\text{s} + (\text{Coding} - 1) \mu\text{s}$.

Inject Pilot (I-PLT)

This is the pulse modulated signal to inject the actual pilot signal as specified in Table 3.6.

The specification for the Pre-Pilot (P-PLT) Sync was described as an envelope for the I-PLT Sync in the initial design specification. However, it was identified that the P-PLT was never used when the SVCU was built.

Table 3.6: I-PLT properties

Timing		
	Occurrence	This pulse occurs in all the N PRIs in the receiving frame.
	Position	The centre of the TTP occurs at a pre-programmed time relative to TX set by MCP1W13.
Properties		
	Transition	Standard.
	Width	Always 5.0 μ s wide.
	Jitter	Standard.
Transmission		
	Receiving Unit	RF Front End and the RF Head.

Pilot Modulations MOD1 and MOD2

These signals are of indefinite duration and are used to set the phase of the pilot signal. The properties for the signals are listed in Table 3.7. Using MOD1 ($0^\circ/90^\circ$) and MOD2 ($0^\circ/180^\circ$) the SVCU can create the two phase scenarios:

1. PRF/4, $(0-\pi/2-\pi-3\pi/2-0)$ over 4 PRIs.
2. PRF/2, $(0-\pi-0)$ over 2 PRIs.

Table 3.7: PMOD properties

Timing		
	Occurrence	Continuous Pulse Train occurring throughout the Radar Frame.
	Position	The transition (togglng) of MOD1 is initiated at every falling edge on PTX and every second falling edge of PTX for MOD2
Properties		
	Transition	Standard.
	Width	Length of PRI.
	Jitter	Standard.
Transmission		
	Receiving Unit	RF Head.

Test Target Pulse (TTP)

This pulse is used for modulating a continuous wave radio frequency (CWRF) to synthesise a target including Doppler for test and calibration of the receiver subsystem.

Table 3.8: TTP properties

Timing		
	Occurrence	If simulate target function is set by MCP1W18B11. TTP is synthesised in every PRI in the receiving frame.
	Position	The centre of the TTP occurs at a pre-programmed time relative to TX set by MCP1W9-10. The TTP position can increment or decrement, at a rate set by MCP1W11, per PRI.
Properties		
	Transition	Rise and fall time of 10ns.
	Width	The width of this pulse simulates the standard transmitted pulse-width as in MCP1W4B5:7.
	Jitter	Jitter of less than 1ns.
Transmission		
	Receiving Unit	SCU C-Band Calibration System.

The specification for the Pre-TTP (PTTP) Sync was described as an envelope TTP in the initial design specification. The PTTP is not used in the current SVCU system. The Receiving Unit for the TTP was initially specified as the Calibration Tower. In the present system it is being sent to the C-Band Calibration system (Table 3.8) as a balanced line, which then converts and forwards it as a TTL Sync to the Calibration Tower.

Pedestal Sync (PSYNC)

The Pedestal Sync (Table 3.9) is generated to indicate the middle of the measurement interval. The measurement interval is defined as the time between the first and the last centre measurement gate in a frame. The mid-point of this interval represents the time and range centroid of the measured target as directed by the range tracker. The leading edge of this signal is used to synchronise the pedestal sensor (AZ, EL) readings at this point. The sync pulse is also used by the SVCU to read the mid-frame time from the time unit.

Table 3.9: PSYNC properties

Timing		
	Occurrence	This pulse occurs once in the receiving frame of the transmit frame.
	Position	The position of the PSYNC pulse is set by MCP1W17.
Properties		
	Transition	Standard.
	Width	5.0 μ s.
	Jitter	Standard.
Transmission		
	Receiving Unit	Pedestal Control.

Automatic Frequency Control Gate (AFCG)

In beacon mode, the RF Head uses a Voltage Controlled Oscillator (VCO) as the first LO. The frequency of this VCO is shifted relative to that of the synthesiser in the RF Head, specified by the shift in the beacon/transponder.

Table 3.10: AFCG properties

Timing		
	Occurrence	AFCG is present in every PRI in the receiving frame (N PRIs see above).
	Position	AFCG is centred as closely possible to the centre of the measured target; this is the centre of the Tracking Gate.
Properties		
	Transition	Rise and fall time of 20 ns.
	Width	Width of 200 ns for all transmitted pulse widths.
	Jitter	Standard.
Transmission		
	Receiving Unit	RF Head and the Receiver.

The AFC is used to track the beacon frequency and minimise the drift between the VCO's and beacon's frequencies. An analogue 'discriminator' is used to sense the difference in

frequencies at the IF2 level using the 30 MHz derived from the System Clock [13]. The discriminator outputs a signal proportional to the drift (1 V/1 MHz). This signal is sampled by an S/H circuit at the tracker position using the AFCG Sync (Table 3.10). The AFCG is also used in S/H circuits for sampling the Σ_T channel for AGC purposes by attenuating strong signals using IF attenuators located within the RFH [16].

Search Marker (SMARK)

The SMARK trigger (Table 3.11) is described as the start of the search span within each PRI. The leading edge of this signal triggers the process to digitise baseband signals and process them in 20 range bins. SMARK is also embedded in the composite videos (CV1 and CV2) used for displaying raw video on the A/R Scopes.

Table 3.11: SMARK properties

Timing		
	Occurrence	SMARK is present within each PRI.
	Position	The leading edge of SMARK occurs at the time referenced to TX specified in MCP1W5. The position of the leading edge of this pulse is constant in the filling frame. In the receive frame, the leading edge position of SMARK may increment, at the same rate as the tracking range MCP1W8, if MCP1W18B8 is set.
Properties		
	Transition	Standard.
	Width	The width of SMARK is the search span; 20 range bins set by MCP1W3B8:15.
	Jitter	Standard.
Transmission		
	Receiving Unit	Receiver.

SMARK present in the filling frame is used for the Composite Video display in the A/R - Scopes. Its negative event output, i.e. falling edge, occurs at the range specified by MCP1W5. At the time MCP1W5 referenced to TX, in the receive frame the digitisation of baseband signals occur.

The synchronisation output to radar subsystems is illustrated in Figure 3.5 and Figure 3.6 [1]. Figure 3.5 shows the output over the course of one PRI, while Figure 3.6 shows the output for an entire frame.

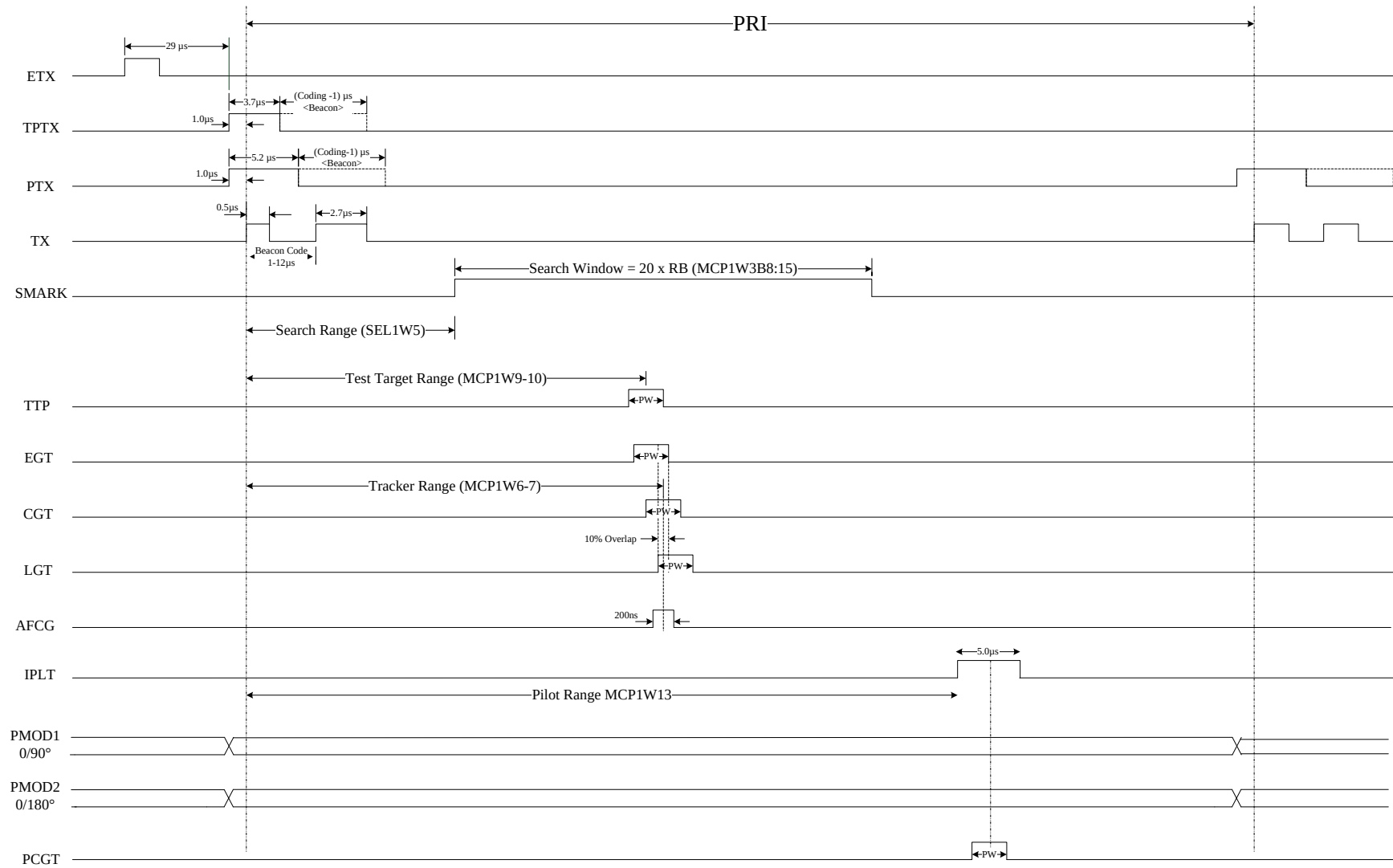


Figure 3.5: Syncs within the PRI

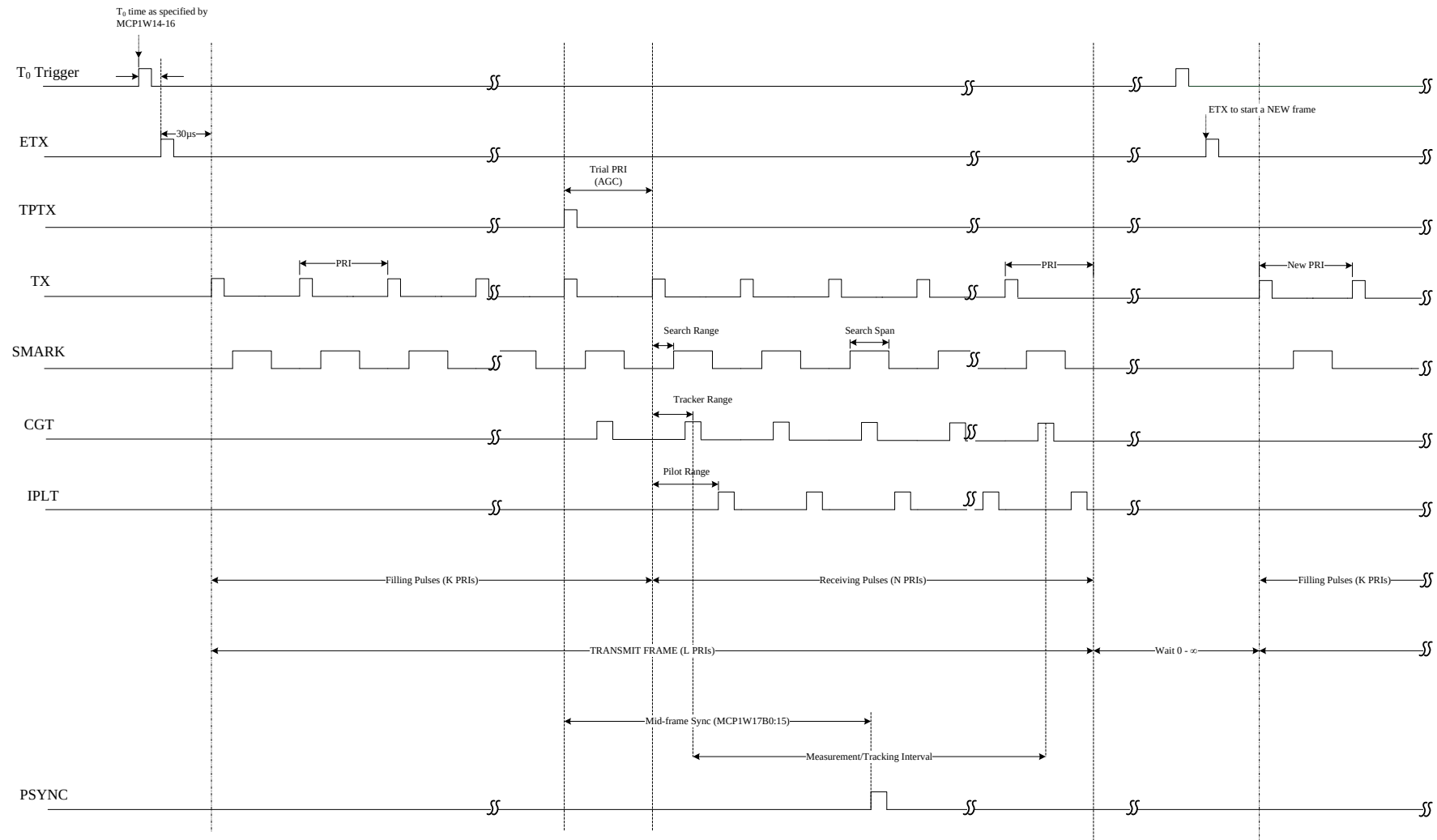


Figure 3.6: Syncs within the radar frame

3.5 Detection Channel Data Processing

Search Range and Range Bins

Digital data representation of the $\Sigma_D(I,Q)$ signal is divided into segments or range bins. The TR uses a ‘range bin’ feature to detect a possible target within a search window. Samples are integrated for the duration of the pulse width to produce 20 successive range bins, which represents the TR’s detection window as per Table 3.12 [9]:

Table 3.12: Detection window

Pulse Width (μs)	Detection Window (metres)
0.5	1200
1.0	2400
2.5	6000
5.0	12000

Threshold

Noise within a signal varies while a return trace of a target will be relatively stable. A reference level can be determined, as noise, when summed up across the range bins, will fluctuate around a reference level. The system keeps tracks of this reference noise level and adjusts the noise threshold accordingly. Most radar systems implement this technique for the Constant False Alarm Rate (CFAR) scheme to detect target presence [19].

Search Span, Sampling and Quantisation

The TR’s Master Computer dictates the precise number of samples and span or window where the sampling takes places for target detection. Sampling and quantisation into range bins for target detection is shown in Figure 3.7 [13, 1]:

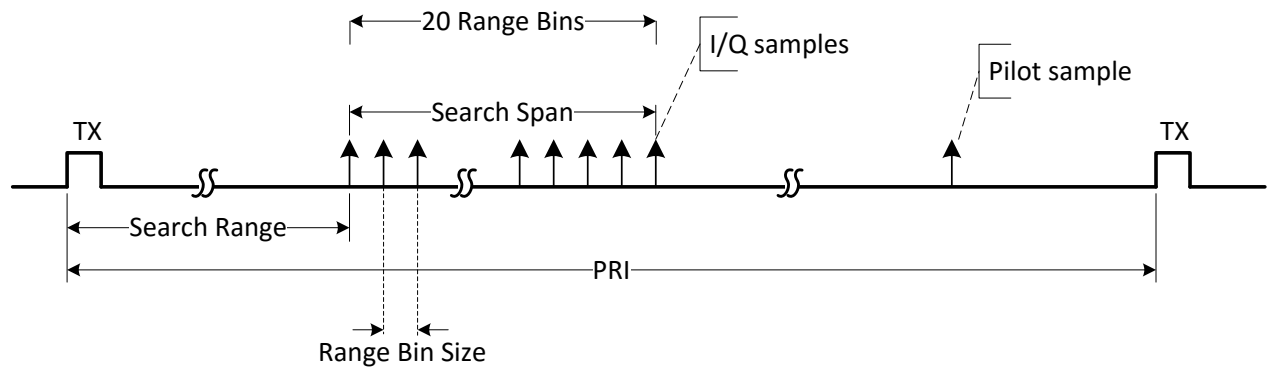


Figure 3.7: Detection channel sampling

The Search Range, Range Bin size and Detection Filter width values are extracted from the instructions received via the Ethernet or Embedded Controller module. Samples are processed into 20 Range Bins depending upon the mode of operation (Pulse Width), which is characterised as follows in Table 3.13:

Table 3.13: Range bin sizes

Pulse Width	Range Bin Size	Sample Array Size for 20 I/Q
0.5 μ s	0.4 μ s	80
1.0 μ s	0.8 μ s	160
2.5 μ s	2.0 μ s	400
5.0 μ s	4.0 μ s	800

There is 20% overlap between consecutive range bins with respect to pulse width, i.e. range bins are of width $RB = 0.8 \times PW$. Sample array size is the number of samples required to create 20 successive range bins. The summation (sample integration) with respect to PW and distribution of data into segments is described in greater detail below.

3.6 Measurement and Pilot Channel Data Processing

The TR uses a ‘range gate’ method to continuously track a desired target. While range bin data from the detection channel is used to identify targets, range gating is used to continuously track it. The range gate is constructed of three sets of gates (Figure 3.8) matched to the pulse width or mode of operation, namely: Early (EGT), Late (LGT) and Centre (CGT) Gate. The return echo is examined under these gates. Depending upon the peak value, and where the echo lies within these segments, the range gate is shifted such that the centre gate is positioned optimally to keep a lock on the target [19].

The range gates have the following specification and timing:

- Pulse widths of 0.5 μ s, 1.0 μ s or 2.5 μ s respectively matched to the transmitted pulse width.
- Overlap of 100 ns, 400 ns or 1.9 μ s respectively between the early and late gate.
- Tracking Range is at midpoint of the centre gate.

Similar to the tracking method, the PCGT is used for sampling of the injected pilot signal.

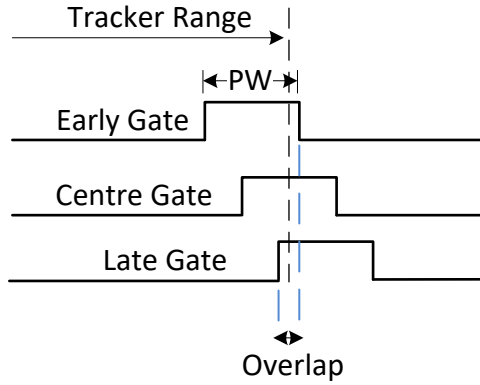


Figure 3.8: ECL range gates

Range Gate Integration

The sampling of Tracking, Azimuth, Elevation and Pilot signals are done using range gates. The Previous SVCU system used the range rate to operate an integrate and hold circuit (I/H) which integrates the signal for the duration of the range gate and holds the value. An A/D conversion of the integrated value is then performed. Using the I/H circuit, A/D conversion for multiple channels was performed using a multiplexer.

The new hardware is capable of sampling multiple channels with very low channel-to-channel skew. Analogue RC integrators used in the previous SVCU are replaced with an equivalent digital integrator, as shown in Figure 3.9, to provide more stability by eliminating discrete components that are susceptible to change due to temperature and limited to tolerance of the components used [29].

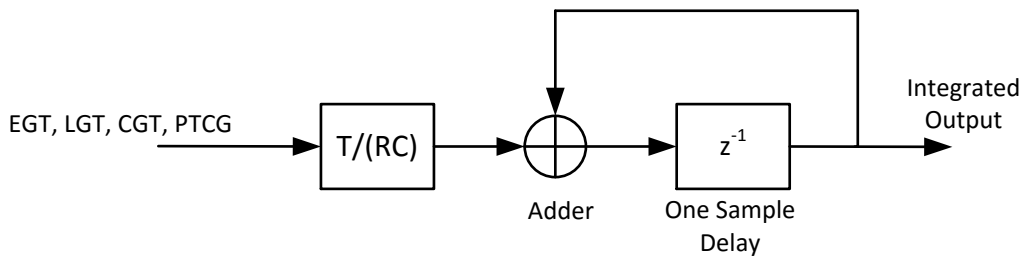


Figure 3.9: Digital integrator

The T/RC equates to the sample delay time. The integrated output of the digital integrator will depend upon this sample delay time. Therefore, the sample delay time of the digital integrator is matched to the RC value of the I/H hold circuit.

3.7 Composite Video for A/R-Scopes

Video signals SV1 and SV2 are superimposed with trigger and marker pulses to yield the composite video signals CV1 and CV2 as shown in Figure 3.10 [1]. Trigger and marker pulses generated are as follows [14]:

- The leading edge of TRIG SYNC coincides with the start of the PRI (PTX).
- The leading edge of SEARCH SYNC coincides with the search range start (SMARK).
- The trailing edge of TRACK SYNC coincides with the measurement centre gate (CGT) trailing edge.
- The trailing edge of PILOT SYNC coincides with the pilot centre gate (PCGT) trailing edge.

All voltage levels are relative to the reference level. The video amplitude is assumed to be $\pm 1V$.

3.8 Summary

The analogue properties of the timing signals (syncs) generated in the SVCU were discussed in detail. The syncs are of logic levels: 0 to 5V. The critical syncs that result in RF energy transmission and target synthesis for calibration have a requirement of transition times of less than 10 ns and jitter of less than 1 ns.

A revised list of timing and data processing requirements was generated due to the inconsistencies found in the design specifications of SVCU that was compiled before the original SVCU was developed. Changes made to the functions of the SVCU, due to the modifications made to other subsystems of the TR, were also taken into consideration.

The next chapter discusses how this revised version of the timing and data processing requirements are implemented in an FPGA based hardware to develop a new SVCU prototype.

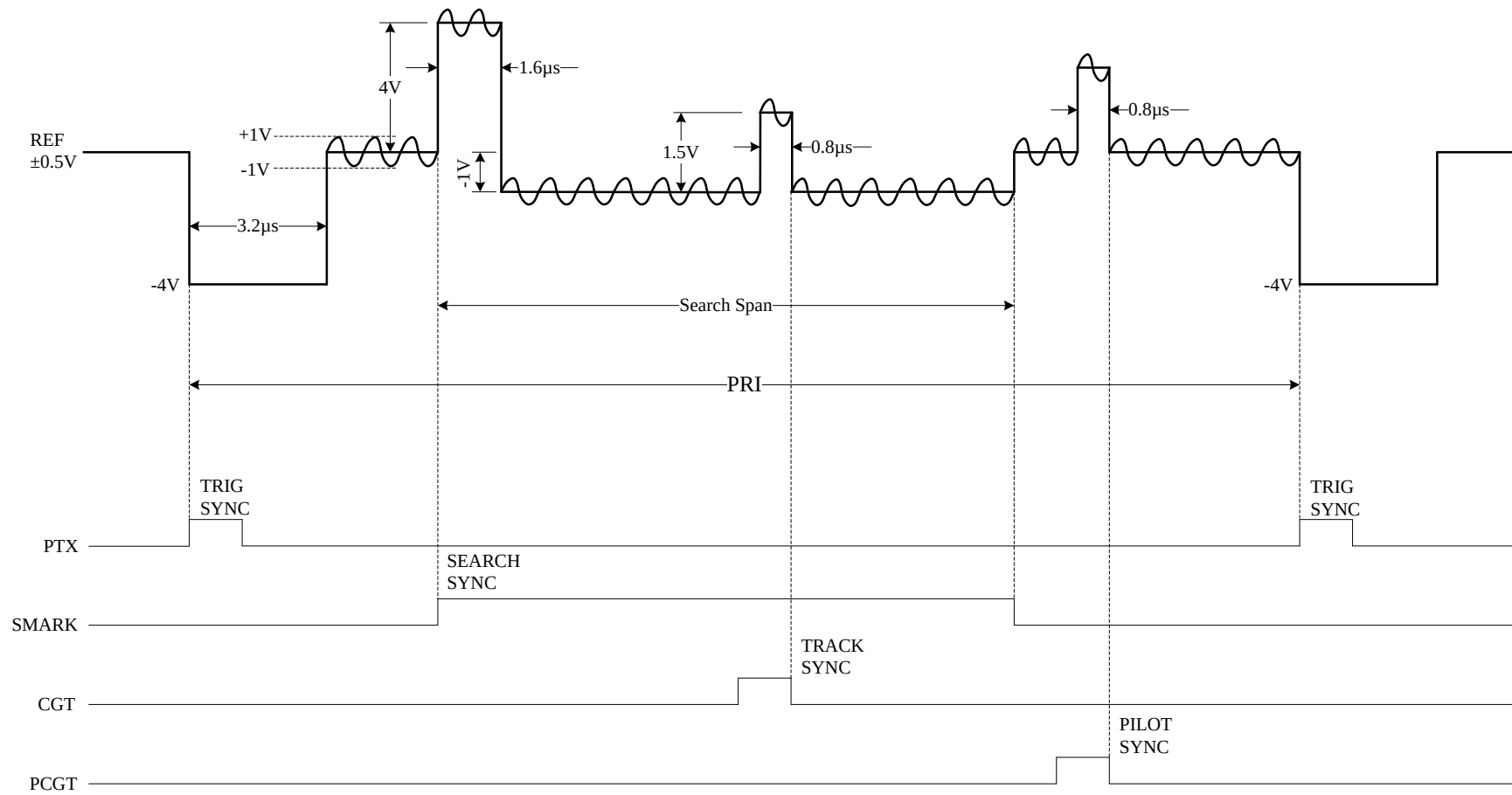


Figure 3.10: Composite video for A-scope

Chapter 4

SVCU Development using LabVIEW and FPGA

This chapter gives a detailed description of the functions created using NI's graphical programming software LabVIEW. The functions detailed in this section meet the practical and operational requirements of the SVCU. The SVCU project in LabVIEW, as shown in Figure 4.1, consists of a HOST SVCU.VI file where the data communication and timebase tasks are configured. The two target FPGA modules are configured to perform video processing and sync generation.

Signals are digitised using the 5170R module and processed in the onboard FPGA. Counters and comparators are implemented in the FPGA of the 7961R Module to generate all timing within the TR frame. These syncs are distributed to all subsystems of the TR using the HSDIO adapter module and a custom interface PCB (Section 2.4.5). The 6683H Timing module is used to keep an internal timebase synchronised to UTC using GPS. LabVIEW codes are implemented in the Embedded Controller to configure the timing module to generate a trigger (a future event) to start all processes of the SVCU. When the Mid Frame sync is generated, it is also timestamped using the timing module.

The Embedded Controller is also used to handle the UDP communication with the MCP to receive and send video processing schemes and frame timing parameters. These parameters are sent to the various FPGA modules using Host to Target FIFOs and upon receiving processed samples, data is sent across UDP to the MCP.

Table 4.1 lists the PCBs or subunits of the SVCU and the high-level LabVIEW functions created in the PXIe modules that perform the tasks of these subunits. The high-level functions in the FPGA are implemented using a timed loop that provides feedback on loop execution and precise timing.

Table 4.1: LabVIEW function representation of discrete components and PCBs

Current Unit	Ref (Figure 2.7)	LabVIEW Functions	PXIe Module / Interface
Detection; Measurement A/D	 	     	FPGA 5170R
A/D Controller		  	FPGA 5170R
Test Generator		Not Used	
Event Generator; ECL Module	 	 	FPGA 7961R + 6583 (HSDIO)
Arithmetic			FPGA 5170R
Time Unit		     	6683H (Timing)
Microcomputer Format and Output RTU	  	  	8840 (Embedded Controller)
Display Unit		Interface PCB	
Video Receiver Control Panel	 	Not Used	

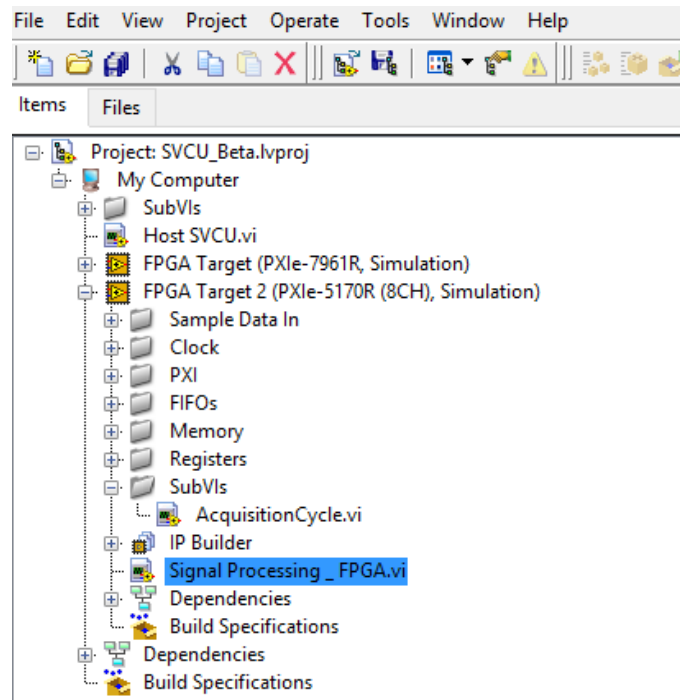


Figure 4.1: SVCU project structure

4.1 System Reference Clock

An independent buffer (having a source impedance matched to the backplane) drives the clocks (PXI.CLK10 PXIe.CLK100 and PXIe_SYNC100) to each peripheral slot [30]. The distribution of clocks within the 1082 Chassis is illustrated below in Figure 4.2 [30].

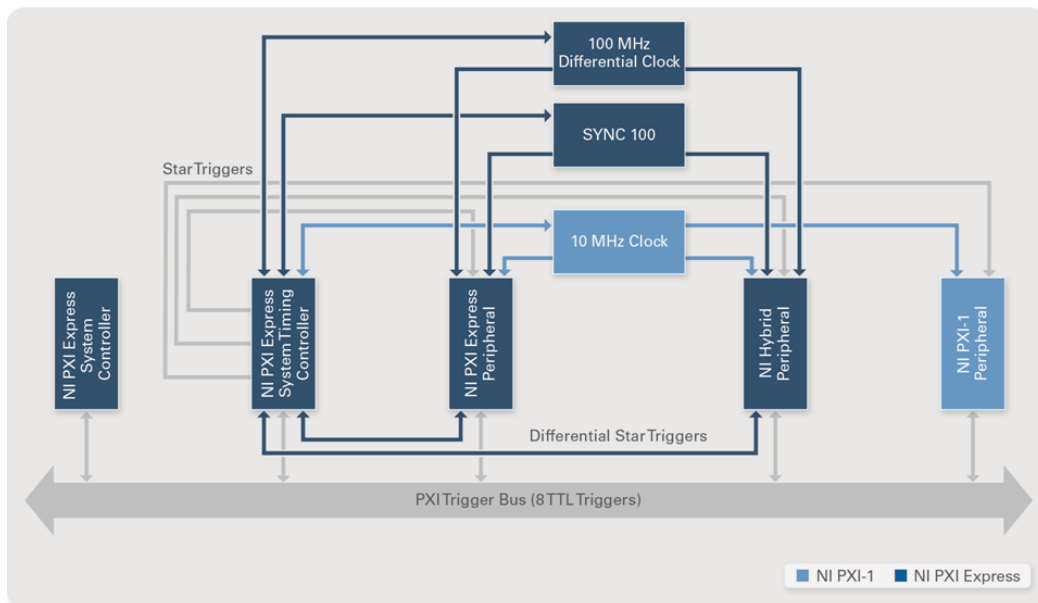


Figure 4.2: PXIe chassis timing and synchronisation features

The 10 MHz clock derived from the TR's Master Clock is connected to the REF IN connector on the rear of the chassis. When this external 10 MHz clock is detected on this connector, the backplane phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 to this external 10 MHz clock, which are then used as reference clocks to synchronise all modules used within the SVCU PXIe Chassis.

4.2 GPS Synchronised Timebase

To initiate the SVCU at a given moment, the SVCU would need knowledge of what the current time is. This current time of day is provided by the NI 6683H Timing Module using GPS. The GPS receiver on the PXI-6683H can power an active GPS antenna, receive, and process the RF signals from the satellites. This generates a very precise PPS signal that the Timing Module uses to achieve sub-microsecond synchronisation. The Timing Module is then able to keep an internal timebase with 10 ns resolution that is synchronised to GPS. The Timing module also allows other methods of synchronised time reference that can be selected such as IRIG-B, IEEE 1588, PPS, or free-running [31].

The synchronised timebase function is configured in the 6683H Timing Module using the following functions:



Initialise the NI-Sync Module driver session.



Use GPS as the preferred source of time reference.



Get the current time.

The module now continuously syncs itself to the external time reference, until it is interrupted.



Close the driver session when stopped or error occurs.

This GPS synchronised timebase is used to schedule triggers to occur at a specified future time T_0 described in Section 4.4. Figure 4.3 shows the implementation of the synchronised timebase using GPS.

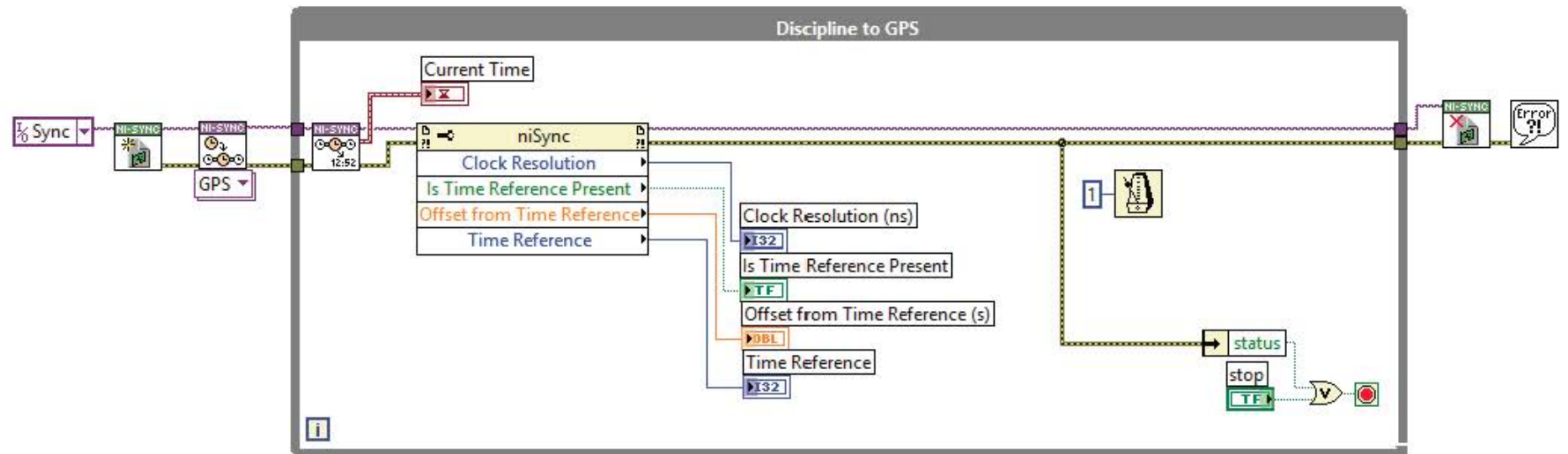


Figure 4.3: Setting up a synchronised timebase

4.3 Message Handling

OTR uses UDP to send and receive short messages over Ethernet to communicate between different systems. Although UDP is not a preferred method for sending critical messages, the network is configured to receive and send data via Ethernet using separate node or IP addresses to maintain good throughput. MCP sends instructions to the SVCU at an interval of 5 to 10 ms. An assumption is made that if data is lost, there would be no time to recover it. The SVCU would simply have to execute the next instructions. The performance of UDP in the PXIe based SVCU has proven to be adequate currently and will continuously be assessed in the future.

The UDP socket is opened and configured on a pre-set port. Data is retrieved from the specified port using a Receive function. Received data is then sent to the T_0 function (Section 4.4) to extract the time that the central computer wants the SVCU to start all processes. The received data is also forwarded to the two FPGA modules to configure the timing to generate syncs and apply the baseband video processing scheme as per the Master Computer's instruction. This process is illustrated in Figure 4.4.

A separate UDP socket is configured to send the processed video samples, status, and midframe time to the Master Computer. The processed data from the digitiser module is fetched from the Embedded Controller using the Fetch Data function (described in Section 4.7). When samples are successfully transferred from the Target (FPGA) to the Host (Embedded Controller) a true logic enables a case structure, which sends the data via the configured UDP socket. This process is illustrated in Figure 4.5.

The UDP receive and write process is implemented in the Embedded Controller using the following LabVIEW functions listed in Table 4.2:

Table 4.2: UDP functions

	UDP Open	Opens UDP socket on the set port
	UDP Read	Read Data being transferred in the configured port
	Case Handler	Ignore timeout and continue to wait for UDP data
	UDP Send	Write to specified port and send data
	UDP Close	Closes UDP socket when error occurs or instructed to stop

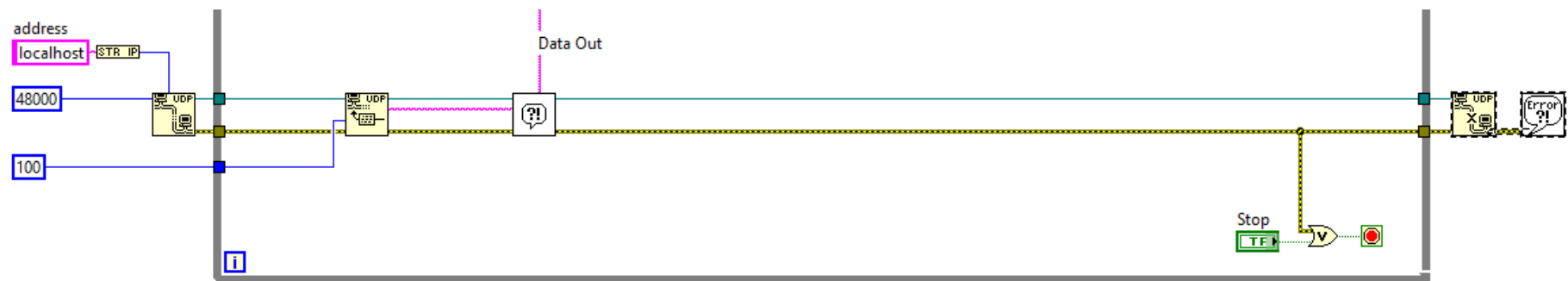


Figure 4.4: UDP receive functions

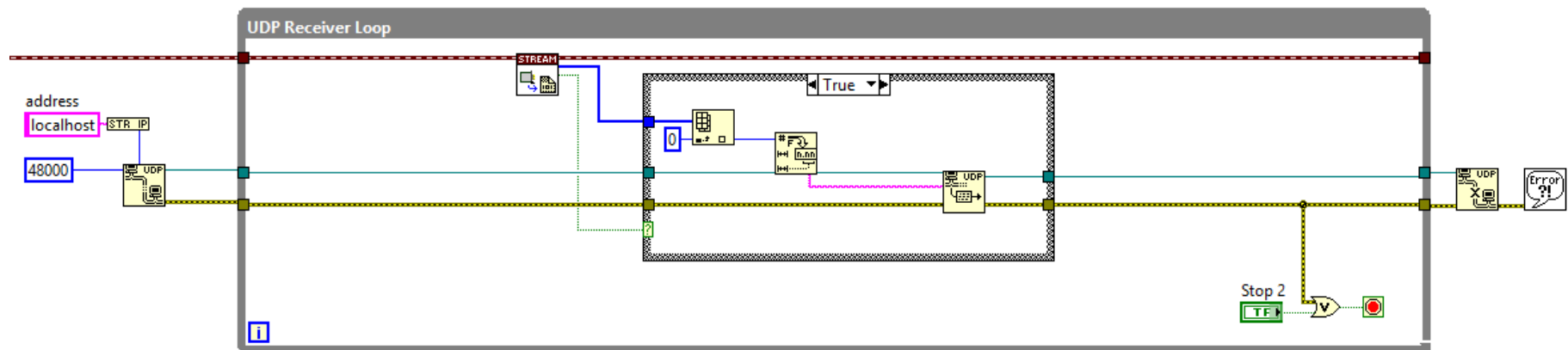


Figure 4.5: UDP send

4.4 T_0 Event Generation

The leading edge of the T_0 trigger starts the SVCU, and hence the generation of the frame triggers, video processing and all timing within the radar. The time at which the T_0 trigger is to occur is programmed, down to $1\mu\text{s}$, by the master computer. This time is extracted from the UDP packet and a future event is created in the FPGA-based Timing Module.

The instruction received from the UDP packet only contains time information relating to seconds and microseconds. An initialisation function outside of the loop is used to extract the date from its internal timebase. A custom timestamp generation function was created to combine this date with the T_0 time received via UDP. The combined event data is then passed on to the Timing Module and a future event is configured. The module generates a $1\mu\text{s}$ pulse on the PXIe_Trig0 line when the time of the day reaches the T_0 time. Figure 4.6 and Figure 4.7 show how this process is configured in the Timing Module. The functions used in the T_0 event generation are the following:



Initialise the NI-Sync Module driver session.



Reset and configure Trig_0 to generate pulse for future events.



Get current time.



Extract T_0 from UDP packet, to generate a future event.



Combine today's date, month and year into required time format.



Set a future time to generate an event on the Sync Module.

When the module reaches the future event time, it generates a pulse on the Trig_0 line in the backplane.



Close the driver session when stopped or error occurs.

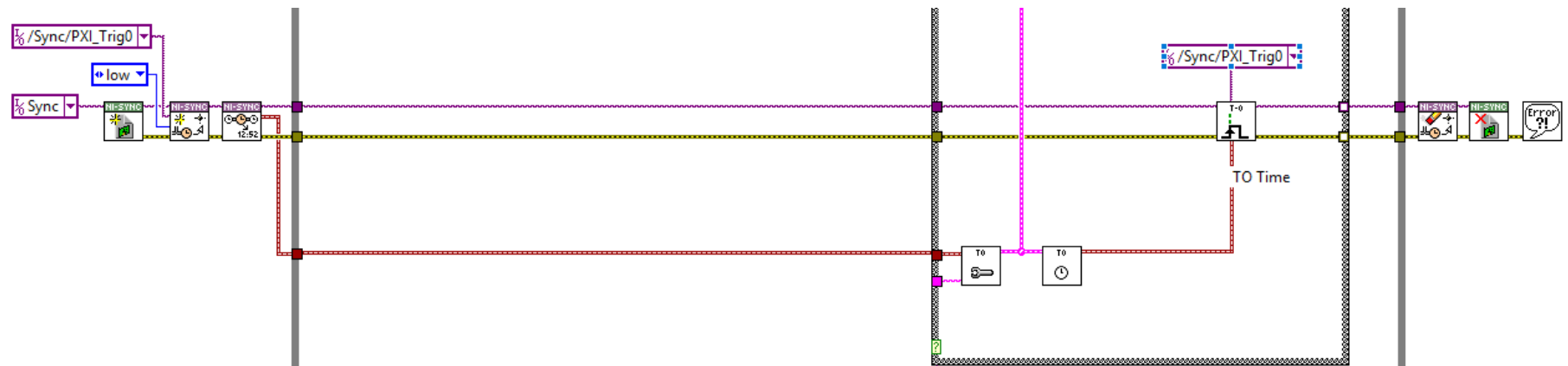
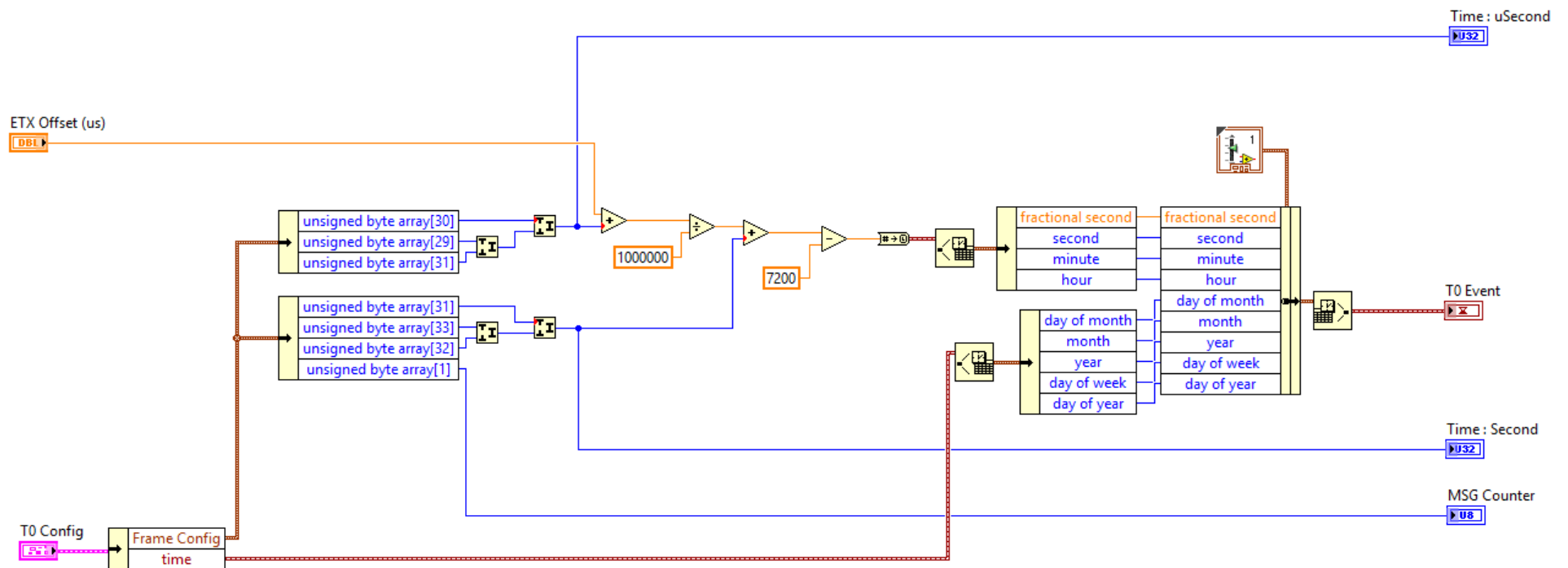
Figure 4.6: T_0 event generation

Figure 4.7: Create T_0 time

4.5 Data Acquisition

The ADCs on the digitiser module are configured with a 250 MHz clock. A set of gain and offset correction values needs to be applied to the digital data depending upon the voltage level it is set to operate at. The samples are fetched from an I/O node in the FPGA at the rate of 125 MHz (half the speed of the ADC's clock rate) using a single timed controlled loop. Every iteration (running at 125 MHz) of the data acquisition loop fetches 2 samples from the ADC and the reduced clock ensures there is enough time to apply corrections and implement DSP functions within one clock cycle. The sampling rate is reduced to 160 MS/s by applying a decimator function within the FPGA. The data acquisition process and its components are discussed in detail in this section.

4.5.1 Single Cycle Timed Loop

A single cycle time loop (SCTL) is a structure or function in LabVIEW which provides advanced timing characteristics such as feedback on loop execution and precise timing. LabVIEW code implemented within the SCTL loop is optimised during the synthesising process to consume fewer resources in the FPGA and ensure the iterations correspond exactly to the clock rate that the loop is configured to run. It differs from the standard While loop as instructions within the while loop can take multiple clock cycles to execute one iteration of the loop. All controlled or critical time processes are implemented in the FPGA using an SCTL. The data acquisition loop is configured in the 5170R module using SCTL as shown in Figure 4.8.

4.5.2 Handshaking

The SCTL loop, implemented in the FPGA, force functions to produce data every loop iteration. However, some functions take more than one clock cycle to process and do not produce valid data every clock cycle. Functions that rely on output from a multi-cycled function need to know which set of data is valid. Therefore a handshaking protocol is used within the SCTL where the functions contain the following terminals [32]:

- Input valid - Identifies that the received data is valid and can be used for processing.
- Output valid - Specified output produced by the function is valid and ready to be utilised by the next function.

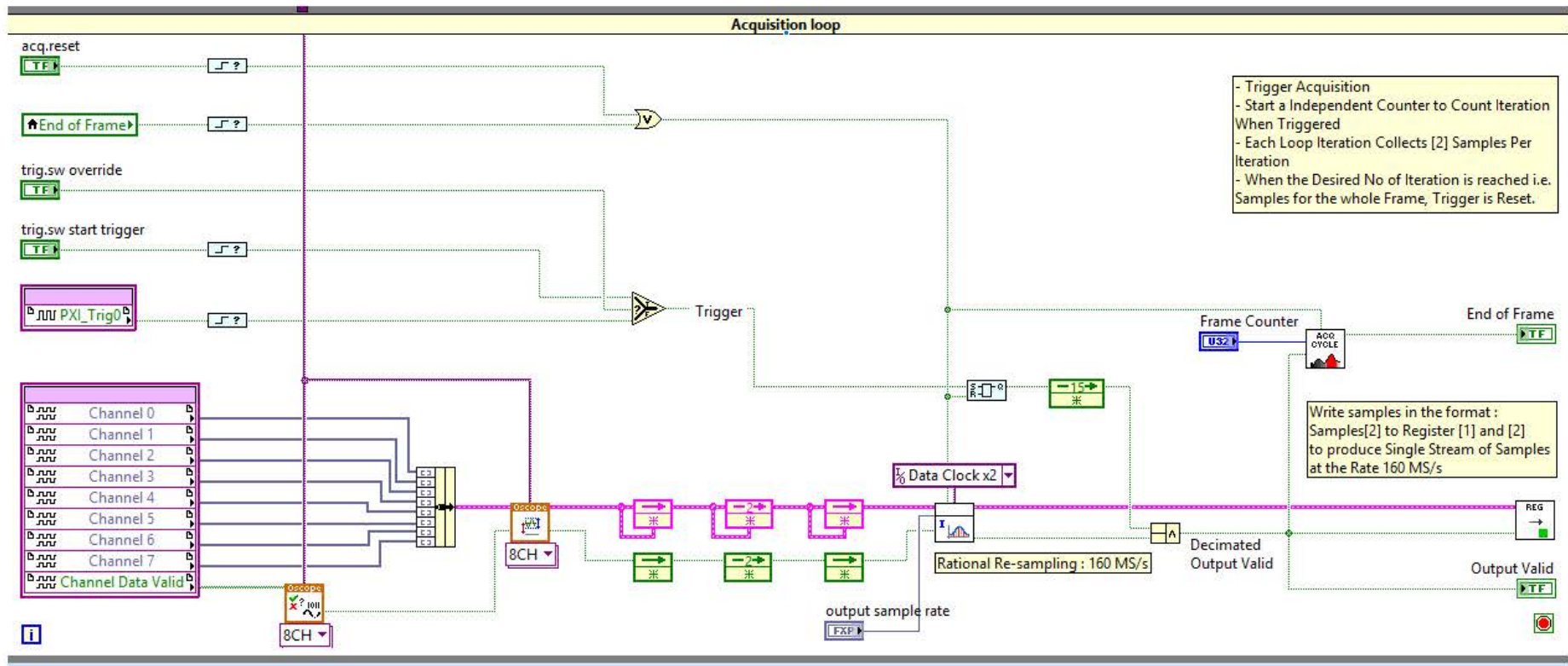
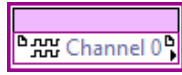


Figure 4.8: Digital data acquisition cycle

4.5.3 Acquisition Cycle

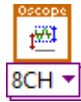
The process of receiving the digital samples within the SCTL is performed by using the following functions:



Receive digital samples from the FPGA I/O Node.



Valid Channel: Enable selected channels and disable the rest.



Apply digital corrections to digital samples.

The triggering is performed using digital logic in the FPGA. Since we are interested in data at a sampling rate of 160 MS/s to process various range gates, the digital logic is implemented as a trigger at the output of the fractional decimator function. There is a group delay of 15 iterations between the input and when the first valid output is generated by the decimator. When a trigger is generated in the PXIe_Trig0 line, a synchronous latch is set and delays are added to compensate for the decimator. When the delayed trigger is true and the output from the decimator is valid, the acquisition data is valid for the radar frame.

Each time there is valid output from the decimator, it is written to a set of registers, to be transferred to a loop running at twice the sampling rate, to convert two samples per acquisition to a single stream of samples. This single stream of samples at 160 MHz can be processed into range gates which has a requirement of 6.25 ns sample resolution. This process is implemented in the Acquisition loop using the following functions:



Decimate samples to 160 MS/s when enabled.



Write samples to a set of registers when output from decimator is valid.



Count Samples; when greater than frame length, reset acquisition latch; regard data from decimator as invalid.

An illustration of the acquisition process is shown in Figure 4.13.

4.5.4 Fractional Decimator

A fractional decimator function was created in LabVIEW FPGA using the Digital Signal Processing (DSP) Toolkit to convert samples acquired from the ADC with a sampling frequency of 250 MS/s to the 160 MS/s. The decimator blocks available in the DSP Toolkit is composed by cascading a L-factor interpolator with a M-factor decimator, to decimate an input with a factor of 16/25 as shown in Figure 4.9. A FIR filter is placed between the interpolator and decimator which acts as an anti-aliasing filter.

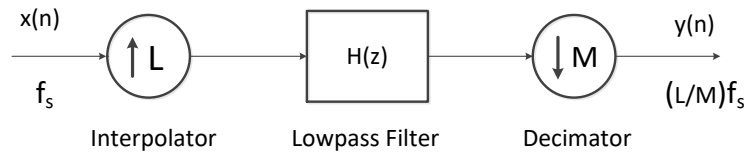


Figure 4.9: Fractional decimation block diagram

The decimator function was created in the FPGA as shown in Figure 4.10.

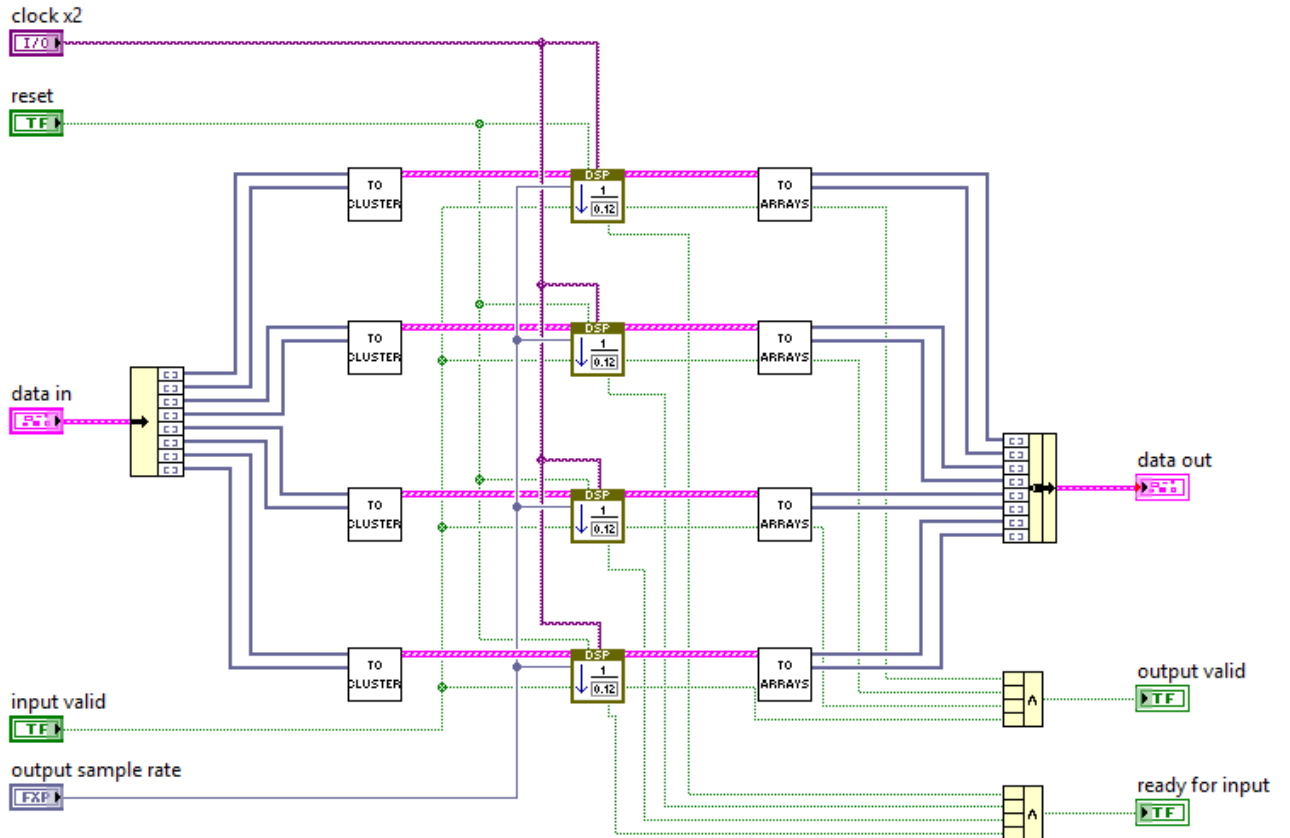


Figure 4.10: Fractional decimator implemented in LabVIEW FPGA

4.5.5 Validate Frame Data

A counter as shown in Figure 4.11 is configured to increment each time acquisition is valid for the radar frame and there is a valid output from the decimator. The counter value is multiplied by a factor of 2 since each valid output from the decimator is a sample pair. When the number of samples are greater than the frame length (received via the Ethernet), end of frame (boolean output) is set high. This resets the acquisition cycle and resets the counter.

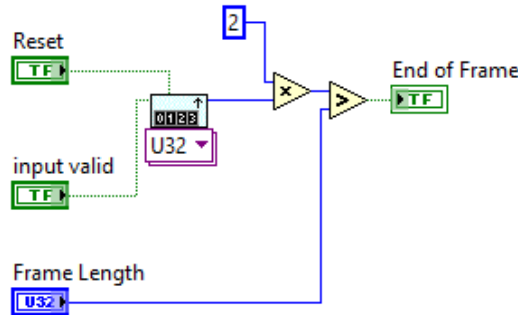


Figure 4.11: Validate frame data

4.5.6 Write to Register

The sample pairs acquired for a valid frame length is written to a set of two registers per channel. A function in the processing loop reads the data in the registers before a new set of values are written. The function created to write values each time input is valid is implemented with a case structure as shown in Figure 4.12.

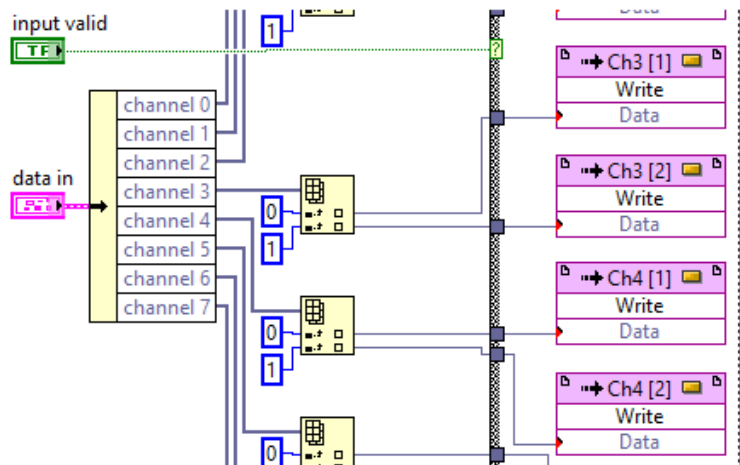


Figure 4.12: Write to register

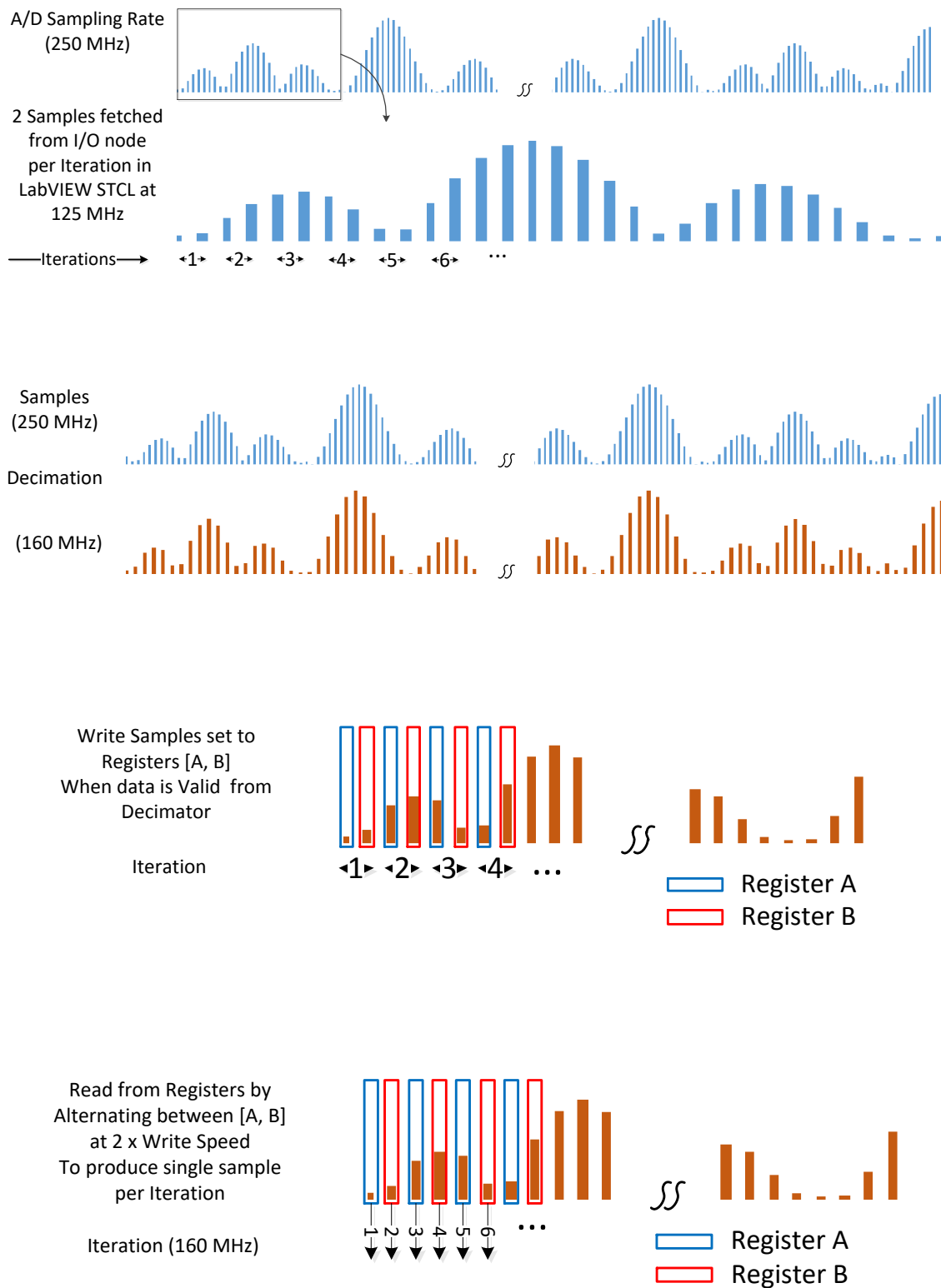


Figure 4.13: Acquisition process

4.6 Baseband Video Processing

This section describes the functions written to be executed within the FPGA to process acquired samples into range bins and tracking gates used by the master computer for target detection, slant range tracking and calibration. The functions are set to execute within SCTL at the rate of 160 MHz. The functions within the processing loop are discussed in this section and listed as follows:



Read received samples from register as a single stream.



Check if the sample count is equal to the search range or tracking range.



Decimate the samples to rate required for range bins integration.



Count the number of samples needed for duration of PW.



Integrate samples to 20 range bins; EGT, CGT, LGT and PGCT.



Perform I/Q mismatch and offset correction.



Store integrated data before transferring it to the Host.

4.6.1 A/R Range

The A/R range function is created to compare the sample count to the search range and tracking range. When the sample count is equal to a respective tracking gate (Search Range, ECT, CGT, LGT or PGCT), it triggers a second stage decimation process to drop the sampling rate required for range bin integration. The function is implemented in the FPGA as shown in Figure 4.14.

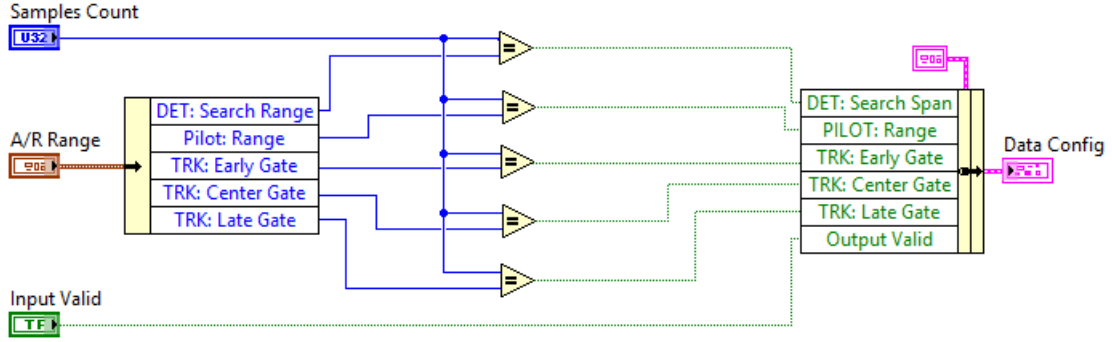


Figure 4.14: Range gate logic

4.6.2 Decimation

The second stage decimator function (Figure 4.15) is created using a counter, which performs decimation by discarding samples. The function is created to match the rate of the range bin integrator with the RC constant of the analogue I/H circuit implemented in the previous SVCU as discussed in Section 3.6.

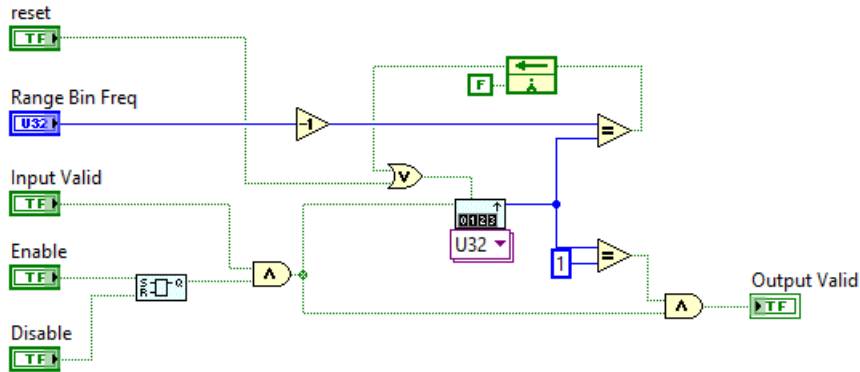


Figure 4.15: Custom decimator

4.6.3 Pulse Duration Counter

This function illustrated in Figure 4.16 is used to count the valid number of samples for the duration of the PW and control the integrator function. When the required number of samples for the size of the range bin or range gate integration is met, this function sends a false condition for data integration and a true logic for Integrated Data Valid. This means it is the end of integration and the sample is ready to be temporarily stored before being sent to the MCP.

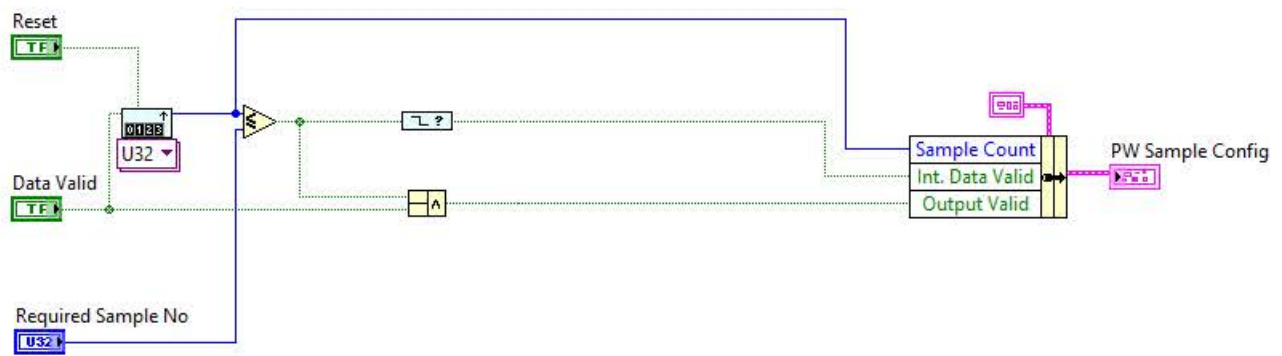


Figure 4.16: Required number of samples

4.6.4 Range Bin Integration

The process begins when the sample count is equal to the Detection Range. At this stage two integrators are used to generate the 20 range bins. These integrators are namely INTA and INTB. The width of INTA/INTB is the pulse integration time which equals the Detection Filter Pulse width as received in the SVCU configuration message. The process is implemented in the Digitiser Module as shown in Figure 4.17. Using these integrators, 20 range bins are generated, where the width of the range bins is $0.8 \times PW$. The process is as follows:

- INTA begins to integrate.
- When INTA reaches $0.8 \times \text{PW}$, INTB begins to integrate.
- When INTA's duration is equal to the PW, INTA stops integrating.
- Correction is applied to this integrated value, upon the instruction from the Master Computer.
- The integrated value is stored in DMA memory and INTA is reset.
- The cycle is repeated for INTB.
- The process is executed for 10 cycles, to produce 20 range bins for a single channel.
- The process is executed for both DET I and Q to produce 20 I/Q Pairs, resulting in 40 samples.

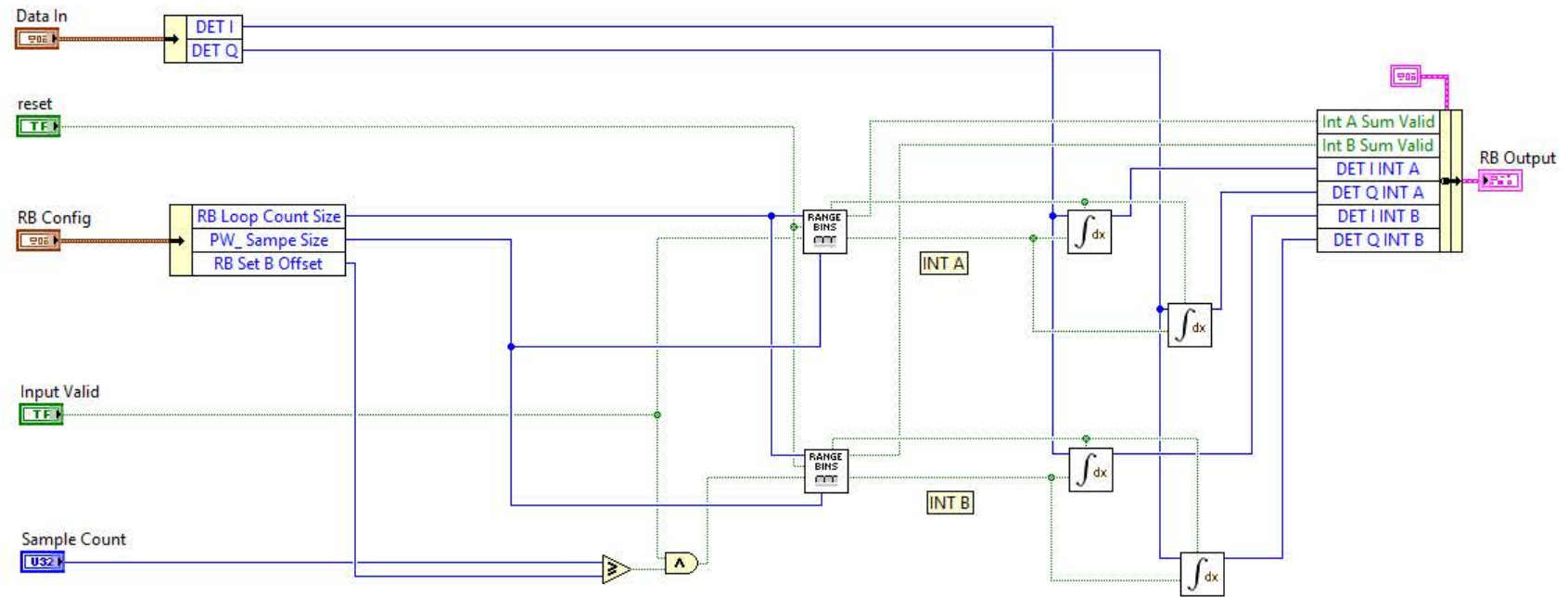


Figure 4.17: Range bins intergration

4.6.5 Range Gate Integration

When the sample count is equal to the EGT, CGT, LGT or PCGT a digital integrator is initiated which accumulates the sum of n samples equivalent to the duration of PW. PCGT is the samples acquired at the range where a pilot signal with known amplitude and phase was injected into the RFFE for calibration. Upon end of integration, the sample is sent to the sample correction function.

Figure 4.18 shows the implementation of the gate integrator function in the FPGA. This function has various instances for integration of range gates, as listed in Table 4.3.

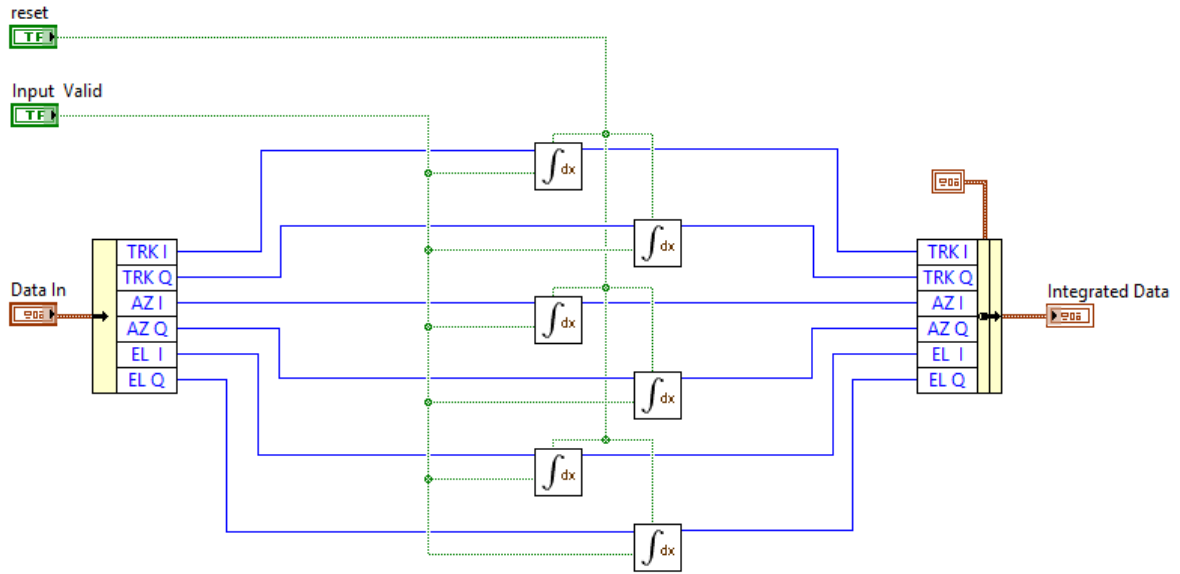


Figure 4.18: Tracking gate integration

Table 4.3: Instances of range gate integrator

Instances	Integration Applied to Channels
	One IQ pair of the Σ_T
	One IQ pair Σ_T , Δ_{AZ} and Δ_{EL}
	One IQ pair of the Σ_T
	One IQ pair of the Σ_D , Σ_T , Δ_{AZ} and Δ_{EL}

An illustration of the range gate integration process is shown in Figure 4.19.

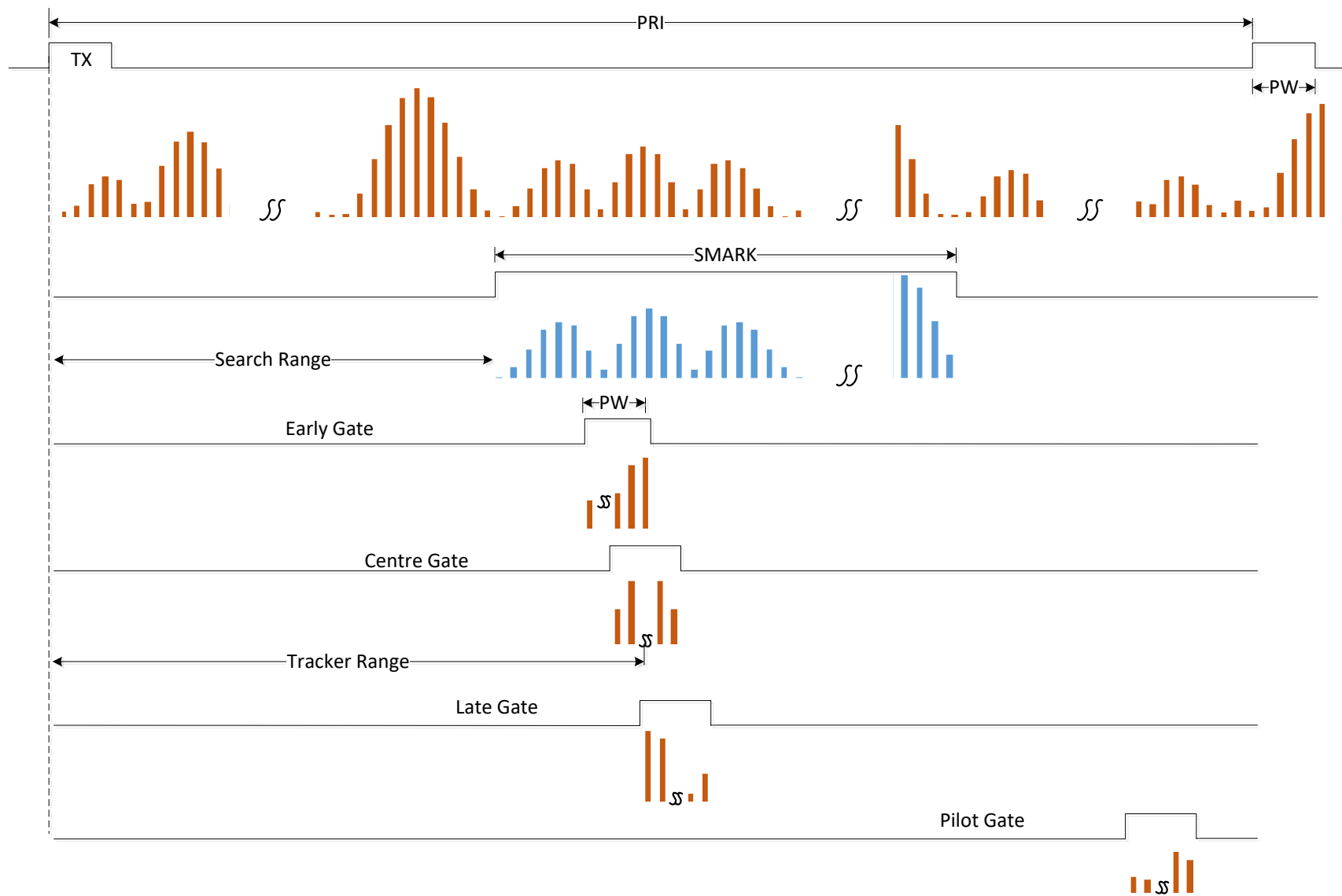


Figure 4.19: Data range gate

4.6.6 Integrator Function

The Integrator function (Figure 4.20) is configured to sum the digitised sample for the duration of the PW. When the input valid condition is true, the input is added to the value in the shift register and the sum is passed to the next iteration to wait for the next valid sample. The number of valid samples needed for the duration of the PW is controlled by the Pulse Duration Counter Function (Section 4.6.3). A reset condition, resets the value in the shift register to zero.

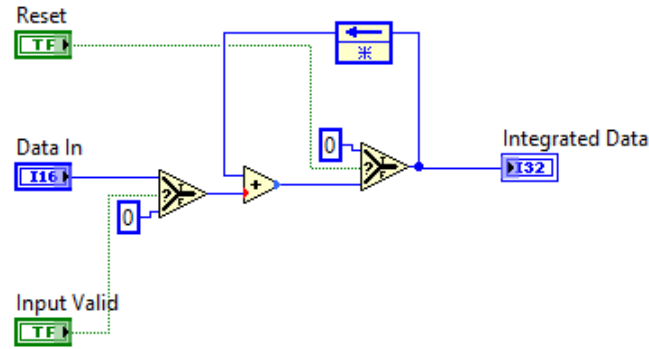


Figure 4.20: Integrator function

4.6.7 Sample Correction

The gain, phase and bias errors between the I and Q subchannels are corrected for each integrated range gate or bin as discussed in Section 2.4.2.3. Figure 4.21 shows the implementation of the range bin correction function in the FPGA.

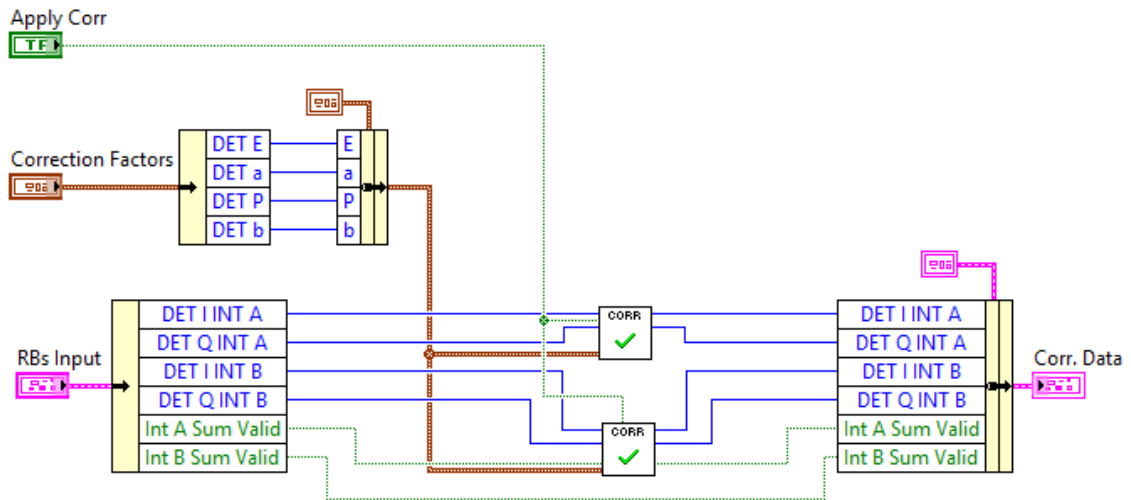


Figure 4.21: Range bin correction

The process of sample integration to range gates and the I/Q mismatch correction applied can be visualised as per Figure 4.22.

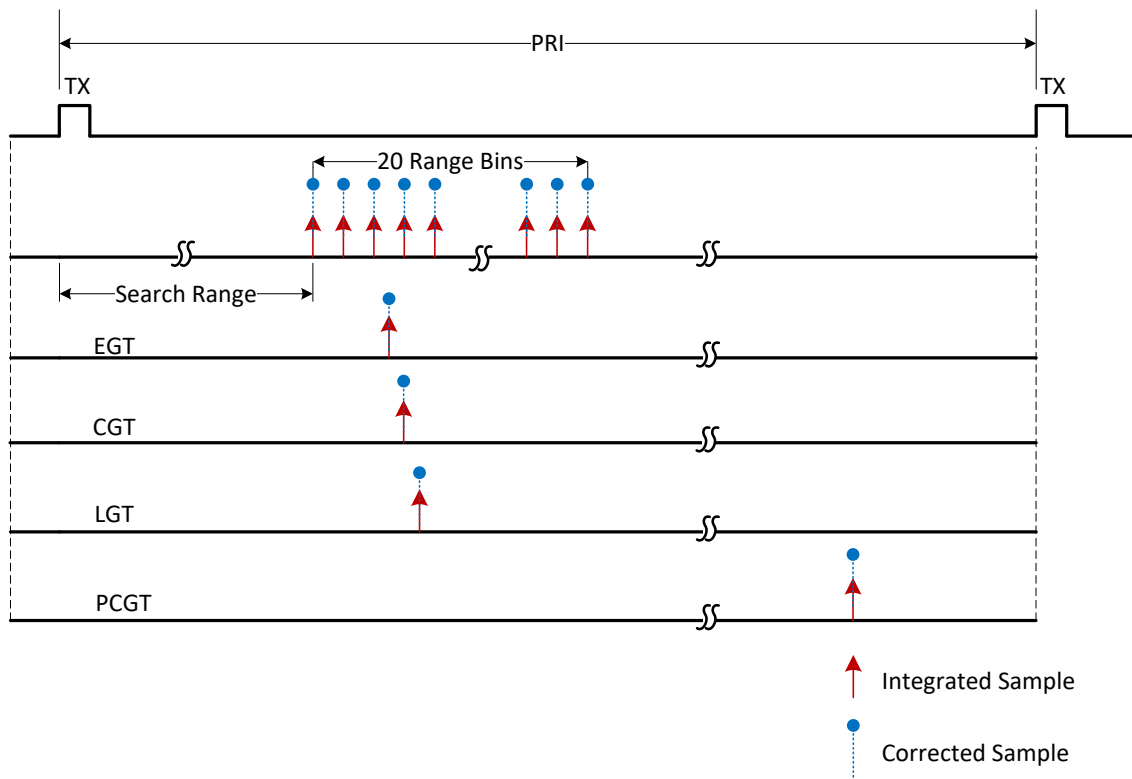


Figure 4.22: Integrated gate data

This function has various instances of its own, which applies corrections to the range gate samples of various channels as listed in Table 4.4:

Table 4.4: Instances of sample correction function

Instances	Integration Applied to Channels
	IQ pair of the Σ_D
	IQ pair of the Σ_T
	IQ pair Σ_T , Δ_{AZ} and Δ_{EL}
	IQ pair of the Σ_T
	IQ pair of the Σ_D , Σ_T , Δ_{AZ} and Δ_{EL}

4.7 Pulse Data

Integration of digitised samples for various range gates occurs at different times. Furthermore, the samples sent to the MCP per PRI also has to be packed into a certain format. A ‘write to memory’ function is created to store the range gate data that has finished integrating temporarily. The data is stored in 64 address memory locations created in the DRAM of the 5170R module. Each range gate is allocated a fixed address (Table 4.5) in the memory and once valid integrated data boolean logic is true, the data is written to the memory address.

Table 4.5: SVCU pulse data memory address list

Sample	Address	Sample	Address	Sample	Address	Sample	Address
Σ_D 00 I	0	Σ_D 08 I	16	Σ_D 16 I	32	Δ_{AZ} Centre I	48
Σ_D 00 Q	1	Σ_D 08 Q	17	Σ_D 16 Q	33	Δ_{AZ} Centre Q	49
Σ_D 01 I	2	Σ_D 09 I	18	Σ_D 17 I	34	Δ_{EL} Centre I	50
Σ_D 01 Q	3	Σ_D 09 Q	19	Σ_D 17 Q	35	Δ_{EL} Centre Q	51
Σ_D 02 I	4	Σ_D 10 I	20	Σ_D 18 I	36	Σ_T Pilot I	52
Σ_D 02 Q	5	Σ_D 10 Q	21	Σ_D 18 Q	37	Σ_T Pilot Q	53
Σ_D 03 I	6	Σ_D 11 I	22	Σ_D 19 I	38	Σ_T Pilot * I	54
Σ_D 03 Q	7	Σ_D 11 Q	23	Σ_D 19 Q	39	Σ_T Pilot * Q	55
Σ_D 04 I	8	Σ_D 12 I	24	Σ_D Pilot I	40	Δ_{AZ} Pilot I	56
Σ_D 04 Q	9	Σ_D 12 Q	25	Σ_D Pilot Q	41	Δ_{AZ} Pilot Q	57
Σ_D 05 I	10	Σ_D 13 I	26	Σ_T Early I	42	Δ_{AZ} Pilot * I	58
Σ_D 05 Q	11	Σ_D 13 Q	27	Σ_T Early Q	43	Δ_{AZ} Pilot * Q	59
Σ_D 06 I	12	Σ_D 14 I	28	Σ_T Centre I	44	Δ_{EL} Pilot I	60
Σ_D 06 Q	13	Σ_D 14 Q	29	Σ_T Centre Q	45	Δ_{EL} Pilot Q	61
Σ_D 07 I	14	Σ_D 15 I	30	Σ_T Late I	46	Δ_{EL} Pilot * I	62
Σ_D 07 Q	15	Σ_D 15 Q	31	Σ_T Late Q	47	Δ_{EL} Pilot * Q	63

* = Uncorrected

A counter is implemented in the ‘Write Range Bins to Memory’ function (Figure 4.24) to sort the 20 I/Q data pairs to the correct memory address. At the end of integration for each range bin, the counter is incremented. The count value is then manipulated by the following factors:

- Counter $\times 2$ - To produce even numbered addresses to store I values
- (Counter $\times 2$) + 1 - To produce odd numbered addresses to store Q values

The writing of Tracking Gate data to memory (Table 4.6) uses fixed numbers for the memory address. The Tracking Gate data to memory function has various instances of its own as listed in Table 4.6, to write range gate data for various channels.

Table 4.6: Instances of data storage function

Instances	Write to Memory
	Σ_T Early Gate
	Σ_T , Δ_{AZ} and Δ_{EL} Centre Gate
	Σ_T Late Gate
	Σ_D , Σ_T , Δ_{AZ} and Δ_{EL} Pilot

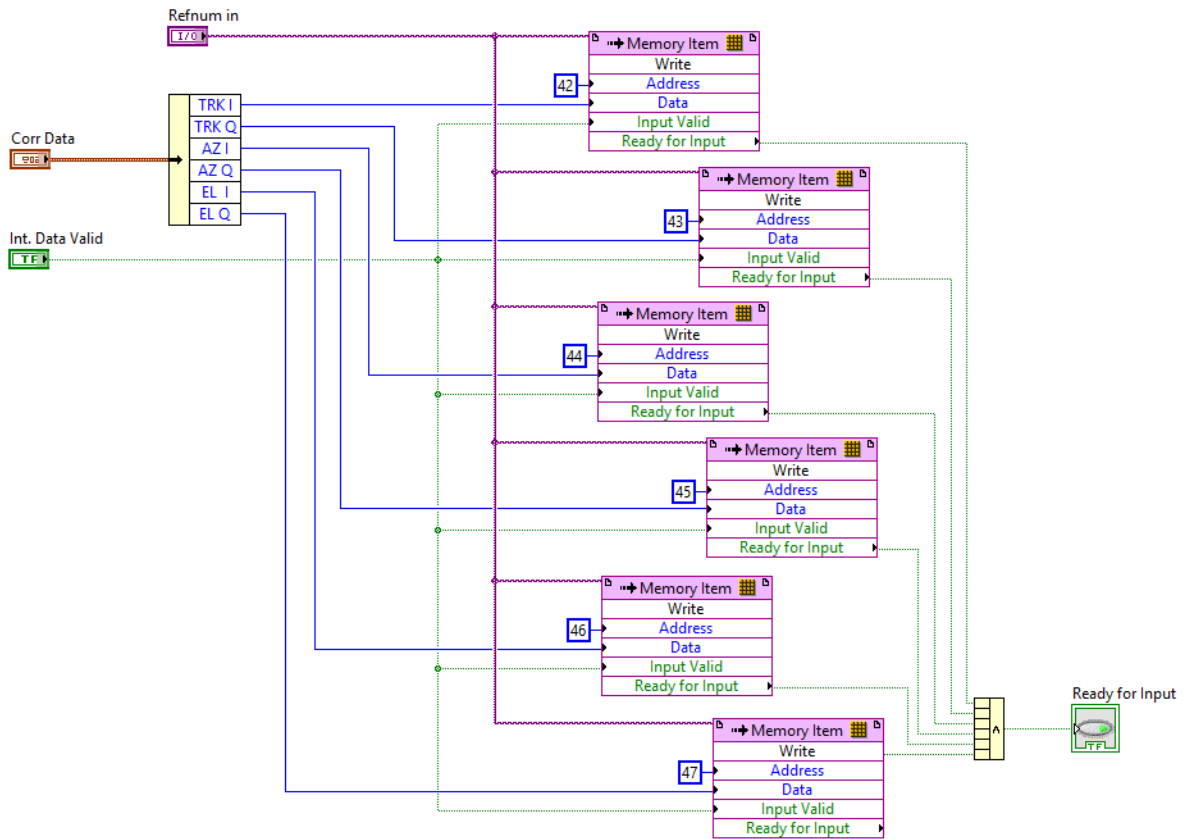


Figure 4.23: Tracking gates to memory

At the end of integration of all range bins and range gates, samples are transferred to the Target to Host FIFO configured in the Data Transfer Loop as per Figure 4.25. Successful writing of all 64 integrated samples generates an interrupt. Upon receiving the interrupt, The Embedded Controller acknowledges the interrupt according to the setup shown in Figure 4.26. The data is fetched from the FIFO and sent to the MCP using the UDP send function as discussed in Section 4.3.

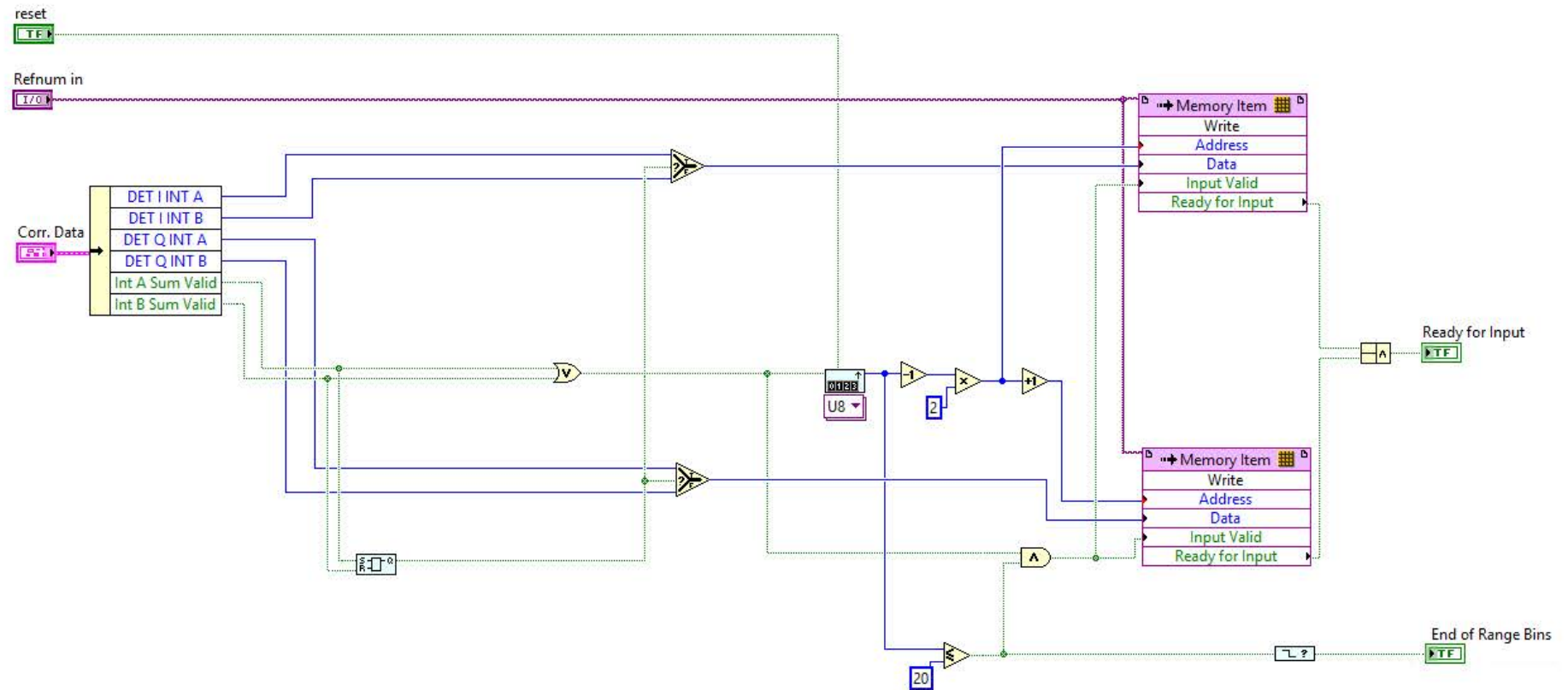


Figure 4.24: Write range bins to memory

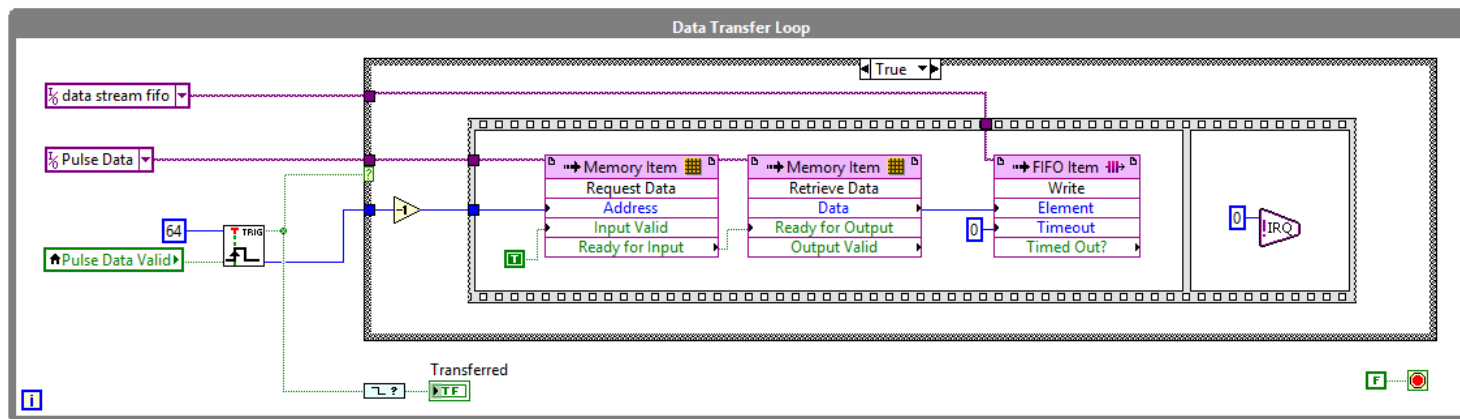


Figure 4.25: Transfer of data using interrupt

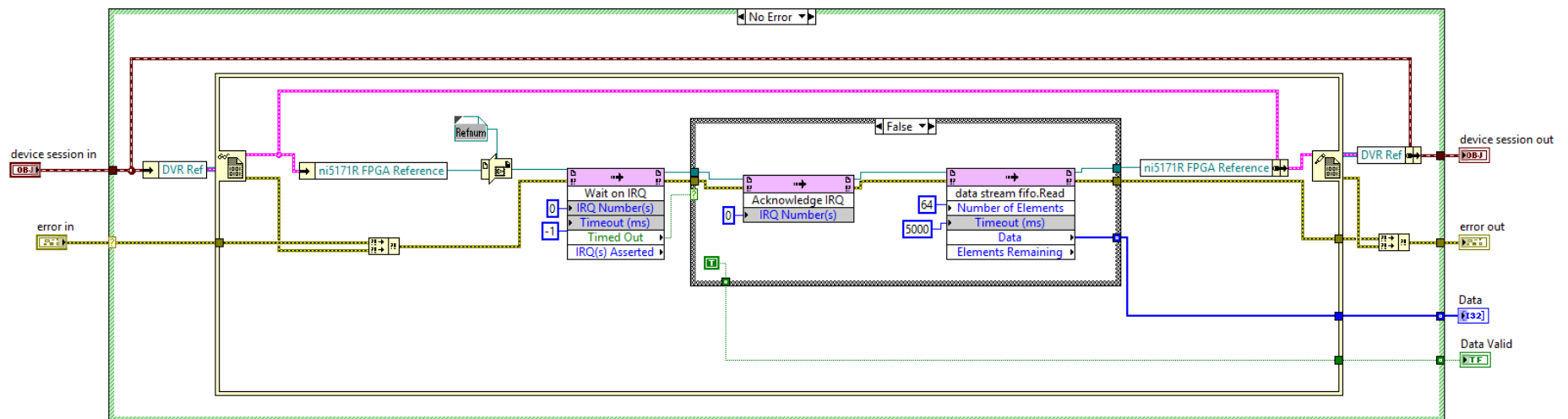


Figure 4.26: Fetching data function in host

4.8 Syncs and Clock Generation

SCTLs, counters, comparators, logic gates, and latches are used to create digital logic circuits in the FPGA to generate all syncs and timing within the radar frame as per Figure 4.32. These digital logic circuits provide precise timing delays for triggering, syncing, delaying and gating events [33]. Counters are used to create multiple, individually delayed outputs. These outputs are configured to drive the various digital I/Os of the FPGA.

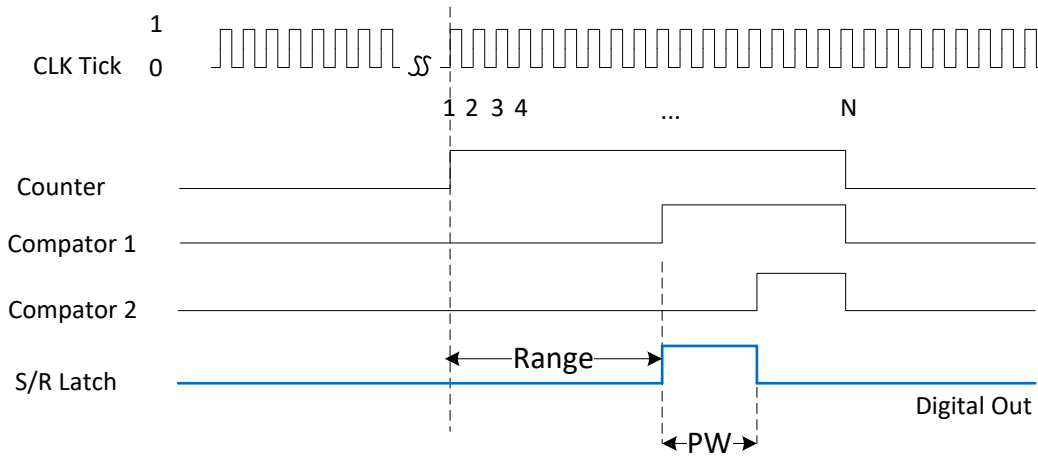


Figure 4.27: Output of digital logic circuits

4.8.1 Counters

The counter function (Figure 4.28) initially waits for an input trigger. Once triggered, as per Figure 4.27, the function starts to count loop iteration or clock ticks where each loop iteration is at a resolution of 6.25 ns. This counter value is then fed to comparators, which generate logical true/false conditions if the clock tick count value overflows a value set in the comparator. A set of two or more comparators is used to produce a digital pulse. The counters then reset to zero when they reach a specified count value. The counters are configured in this method to trigger once to generate the transmit, receive and pre-frame logic and syncs that occur once per radar frame (Figure 4.30). Sub-counters are triggered within these frames in a loop configuration to produce all syncs per PRI as illustrated in Figure 4.31.

4.8.2 Pulse Generation

A set of clock tick values for each sync is sent to the pulse generation function (Figure 4.29). The lower count value is used to set a latch and the higher to reset. The output of the latch is then configured to control the Single Ended Digital Lines in the HSDIO adapter module, or be used as a logic input to another process within the FPGA.

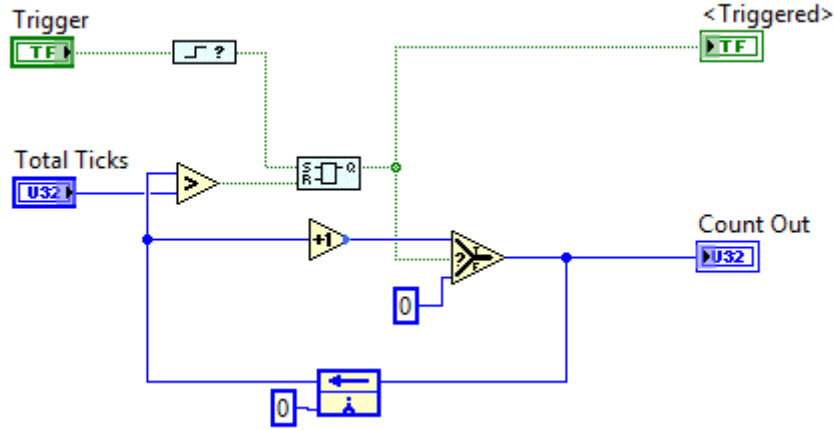


Figure 4.28: Counters

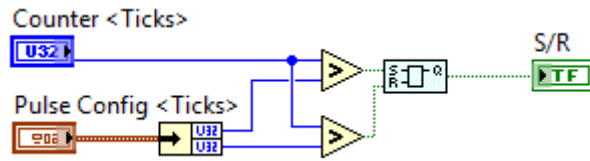


Figure 4.29: Pulse generator

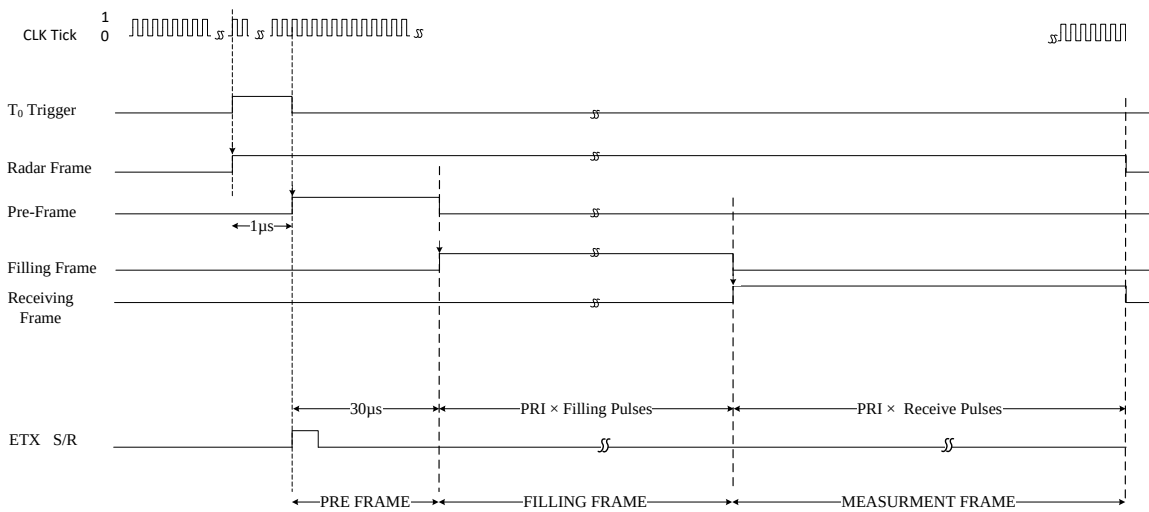


Figure 4.30: Frame counters

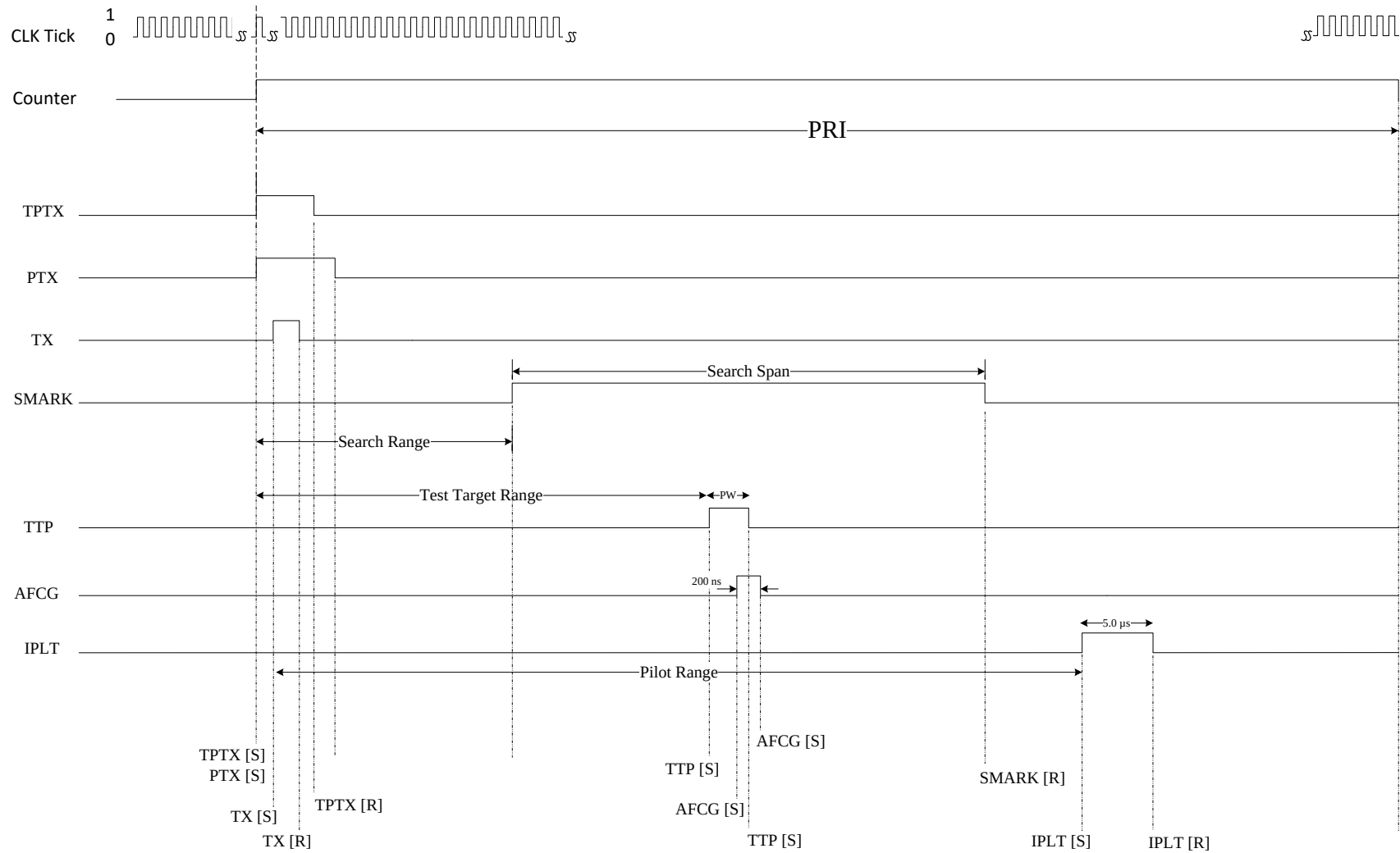


Figure 4.31: Sync generation per PRI using multiple comparators and latches

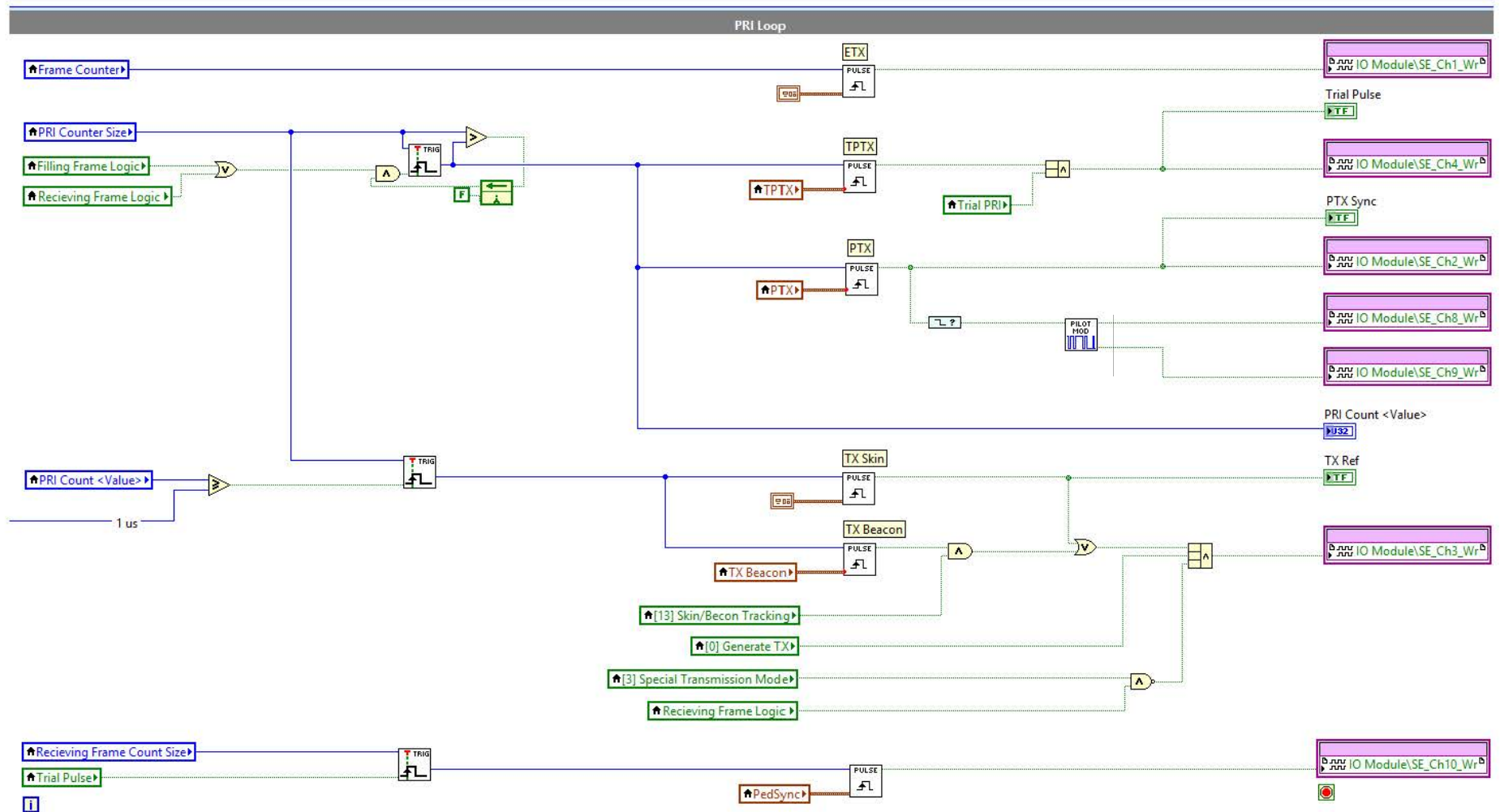


Figure 4.32: Implementation of digital logic to create frame triggers

4.9 Mid-Frame Time

The mid-frame time is defined as the middle of the interval between the first and the last centre measurement gates in a frame. At the mid-frame time, the PSYNC pulse is generated. The leading edge of PSYNC generates a timestamp. This time is then sent, together with the target data, to the Main Computer for signal processing. The functions of the PSYNC pulse is described in detail in Section 3.4. The timestamp loop function in Figure 4.33 implemented to read the sync trigger is as follows:



Initialise the NI-Sync Module driver session.



Enable the time stamping when a rising edge is detected in PXIe-Trig1.



Read the time when the event occurred.



Disable timestamp feature upon stop instruction or if error is detected.



Close the driver session when stopped or error occurs.

4.10 Summary

The implementation of tasks of the SVCU onto the PXIe based system using LabVIEW was discussed in detail. LabVIEW functions were implemented inside a timed loop which provides feedback on loop execution and precise timing. The 6683H module is synchronised using GPS to create an internal timebase for the SVCU which starts the process at a T_0 received from the MCP. PXIe 8840 Embedded Controller module establishes communication with the MCP to receive this time and various parameters. The video baseband processing is performed in the PXIe 5170R digitiser module. A fractional decimator was created to re-produce the digitised data at a resolution of 6.25 ns, to meet the requirement of the Master Computer in order to integrate data into range gates that are defined with the same timing resolution. The timing signals (syncs) are generated in the PXIe 7961R module and output using the HSDIO module.

The next chapter discusses the results and performance of the PXIe based SVCU system.

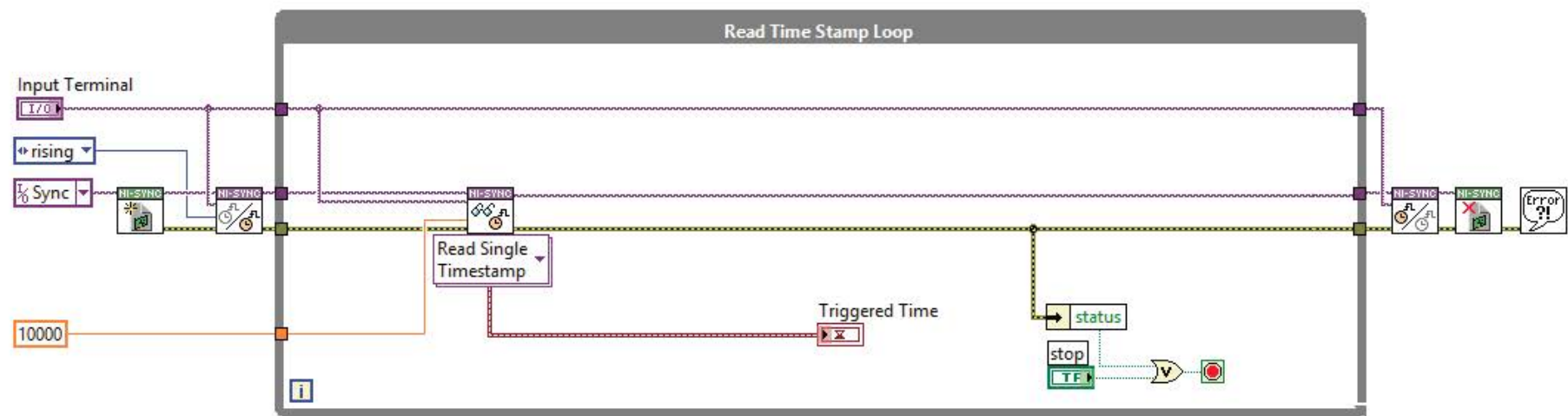


Figure 4.33: Mid frame timestamp

Chapter 5

Discussions and Analysis

This chapter discusses the findings and critical aspects of the development project. The outcome and constraints of implementing the functions of the SVCU into an FPGA and PXIe based system are discussed in this section. The features added and improvements brought about as a result of re-development are described. The chapter also discusses various compensations and modifications added during the design process to optimise performance.

5.1 Dynamic Range

The dynamic range of the ADC is limited due to quantisation error [34]. The dynamic range in a ADC with a certain bit (β) resolution is represented by the ratio of the highest sine-wave (RMS) to noise (RMS) [35]:

$$\text{Dynamic Range}_{ADC} = 20 \times \log_{10}\left(\frac{2^\beta}{1}\right) \text{ dB} \quad (5.1)$$

This can be approximated as:

$$\text{DR}_{ADC} \approx 6.02\beta \text{ dB} \quad (5.2)$$

The NI digitiser module has a 14-bit ADC resolution, which gives us an absolute maximum dynamic range of 84 dB. This is an improvement from the current 12-bit ADCs that are used, which have an dynamic range of 72 dB.

The amplitude of the received signal can vary rapidly. The existing AGC (Section 3.4) module that is in the receiver helps the ADC to best utilise the dynamic range.

5.2 Fractional Decimator and Trigger Alignment

A decimator was implemented in the acquisition loop of the FPGA to reduce the sampling rate of digitised samples. To ensure the FPGA starts the acquisition cycle and captures the samples (through the decimator) at the exact instant that the trigger was received, multiple tests were conducted. This involved sampling a pulse at the same time as we are triggering (using the same pulse).

From the test, it was identified that the valid sample out of the decimator was lagging the trigger due to the delay of the decimator. This caused misalignment between the trigger and the sample set being captured. A delay was added in the FPGA as shown in Figure 5.1 to align the trigger and first sample output from the decimator.

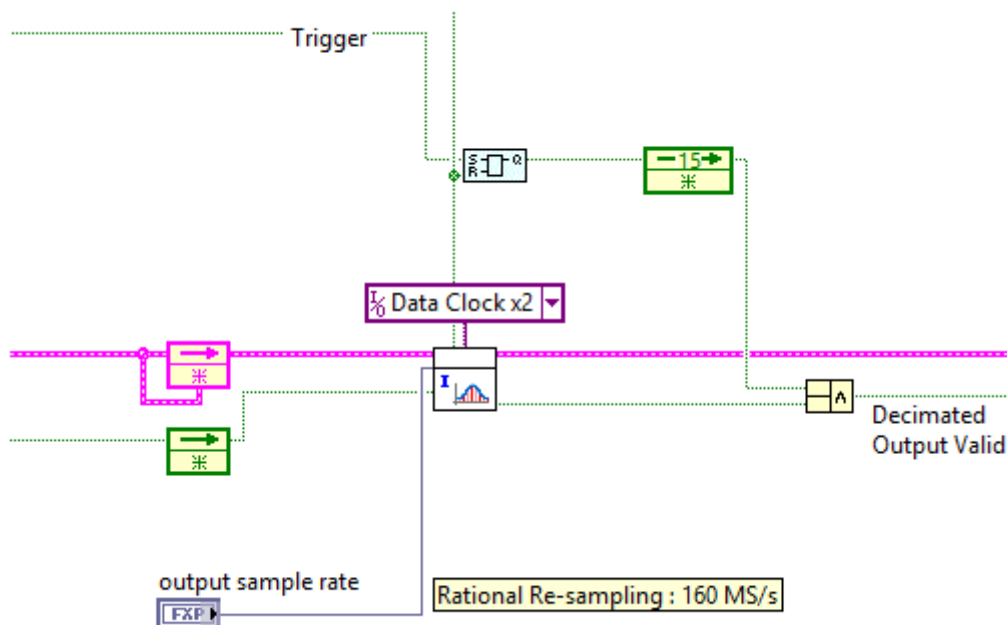


Figure 5.1: FPGA trigger modification

$$t$$

The result is illustrated in Figure 5.2, where the red graph is before adding a delay and blue is after the modification. Adding trigger delays to compensate for the fractional decimator insured the trigger was aligned correctly to the samples being processed at 160 MHz.

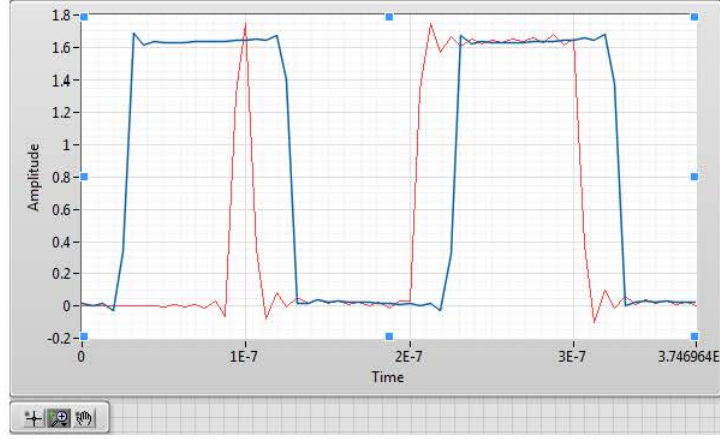


Figure 5.2: Trigger modification

5.3 Radar Frame Data Acquisition

Multiple simulations were conducted to ensure the signal acquisition loop, decimator and the processing functions implemented in the FPGA were operating as desired. Arbitrary signals generated using the 6683H timing module were injected as input to test triggering and to ensure signals were perfectly reconstructed using the digital samples following the output from the fractional decimator.

The test setup was then modified by integrating the PXIe system in parallel to the current SVCU. This allowed the PXIe system to receive instructions and tap into the baseband signal lines without affecting the operation of the TR. The PXIe system was used in parallel to test the functions implemented in the FPGA.

The digitiser module was used to acquire samples during a live flight test involving an aircraft. Digital Samples were continuously captured for each radar frame. Figure 5.3 shows the section of radar frame where the Detection I-sample (Blue) channel was digitised and decimated to a rate of 160 MHz. The PTX sync generated within the SVCU was also digitised by feeding it into the input channel to act as a PRI reference.

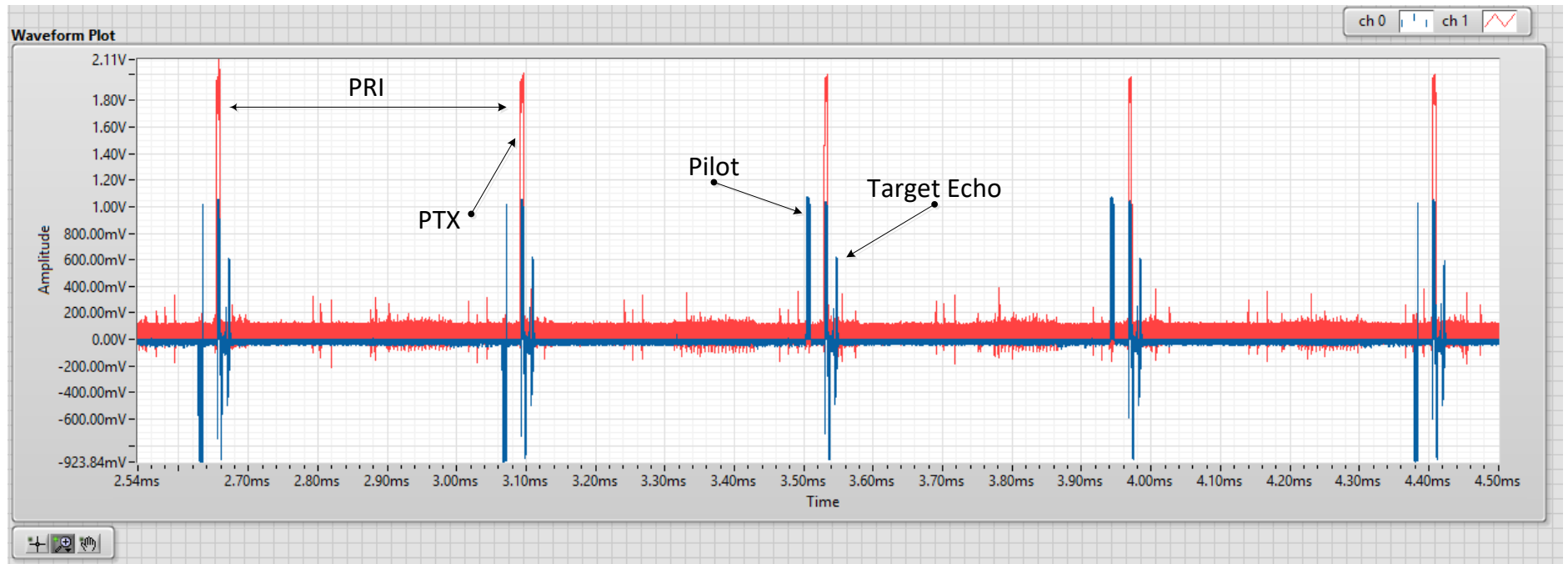


Figure 5.3: Captured frame data

5.4 Sync Analogue Properties

As discussed in Chapter 3, careful measurement and analysis was conducted for all functions generated by the SVCU on all identical TRs. This was due to literature not being readily available at the component level. All syncs generated within the previous system were fed into a Tektronix Logic analyser and each sync was analysed individually regarding position, occurrence, and pulse width.

The syncs were also analysed under different conditions, such as different transmitted pulse widths, single or double pulse (Beacon tracking). Each sync in the TR system was then observed in both mission and calibration mode. This resulted in generating a comprehensive list of syncs and their properties as discussed in Chapter 3.

The behaviour of the syncs observed during various modes of operation identified a number of problem areas that were improved upon in the new PXIe based prototype. The measurements taken by the logic analyser show that at rare instances the syncs were susceptible to longer transition time (low to high) and overshoot before reaching a steady state, causing fluctuation to be seen in the logic levels (as indicated by the arrow in Figure 5.4) of the captured waveform. This observation was also verified using an oscilloscope.

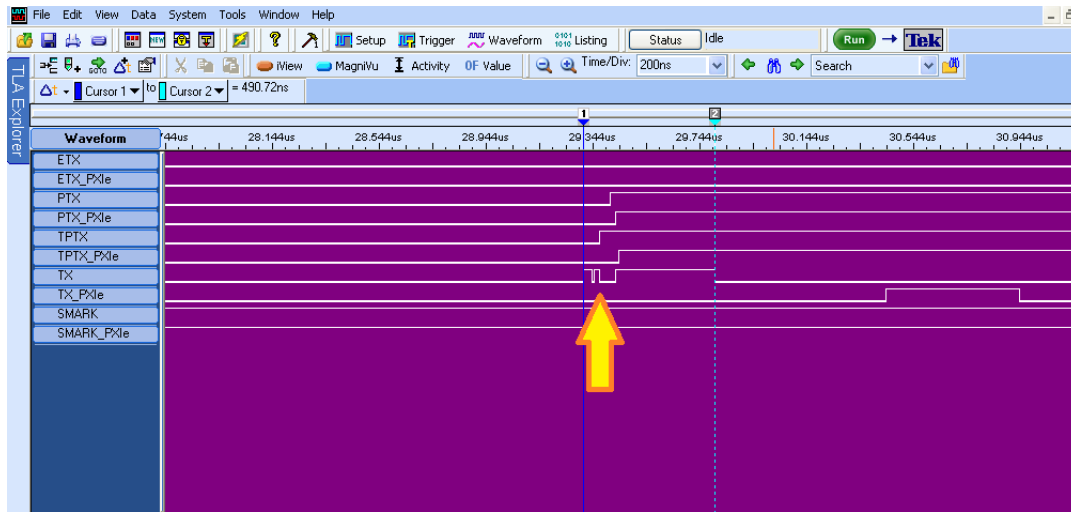


Figure 5.4: Syncs generated in the current SVCU

Furthermore, variations in the position of the syncs was recorded as shown in Figure 5.5. Although in this instance it is within the acceptable range, variations were sometimes observed above the specified requirement. These inconsistencies were mitigated using the HSDIO module and SCTLs in the FPGA which ensures precise generation of syncs with low transition time and fine clock resolution. The result, as shown in Figure 5.6, yielded syncs being generated without any observed or analysed (over the entire radar frame)

variation in position, logic level fluctuation, or pulse width discrepancies in syncs being generated.

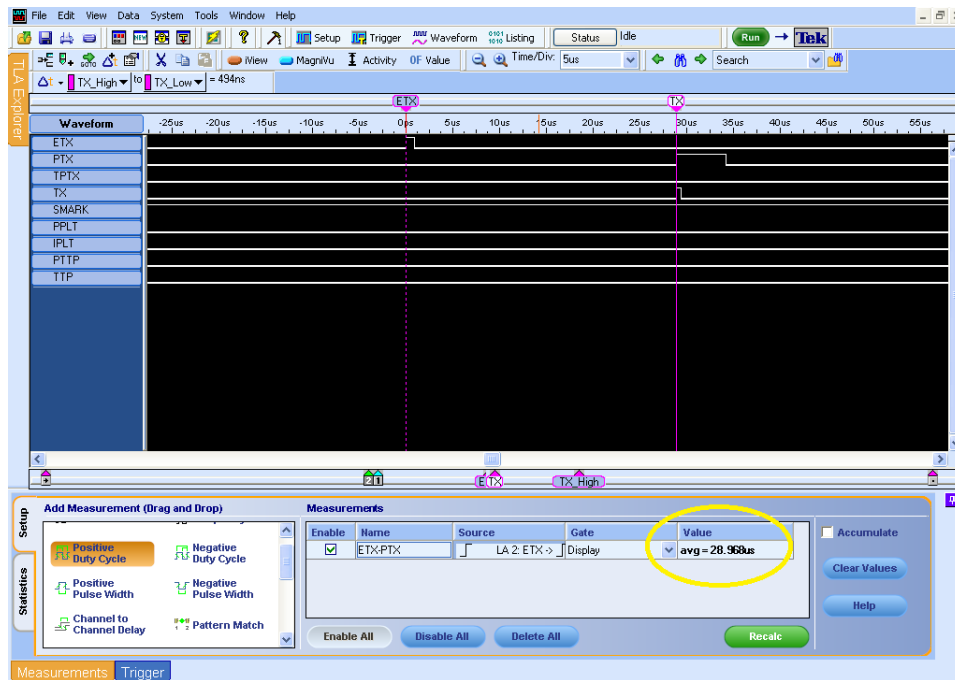


Figure 5.5: Fluctuation in absolute position

The test was concluded by analysing each sync generated using the PXIe prototype and by generating all the required syncs within the radar frame as per Figure 5.7.

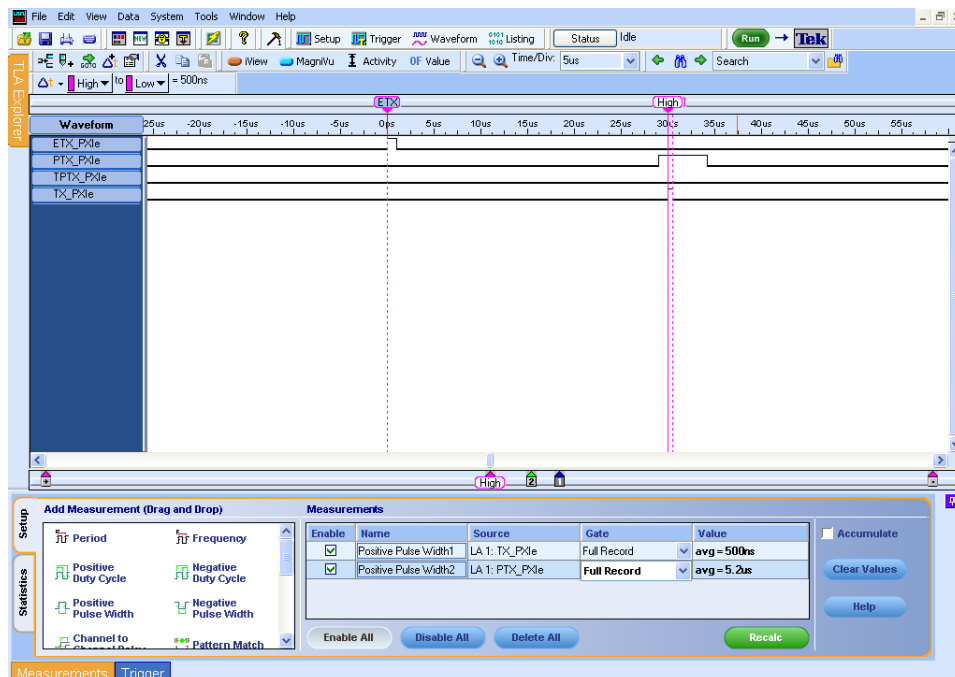


Figure 5.6: Syncs generation in PXIe prototype

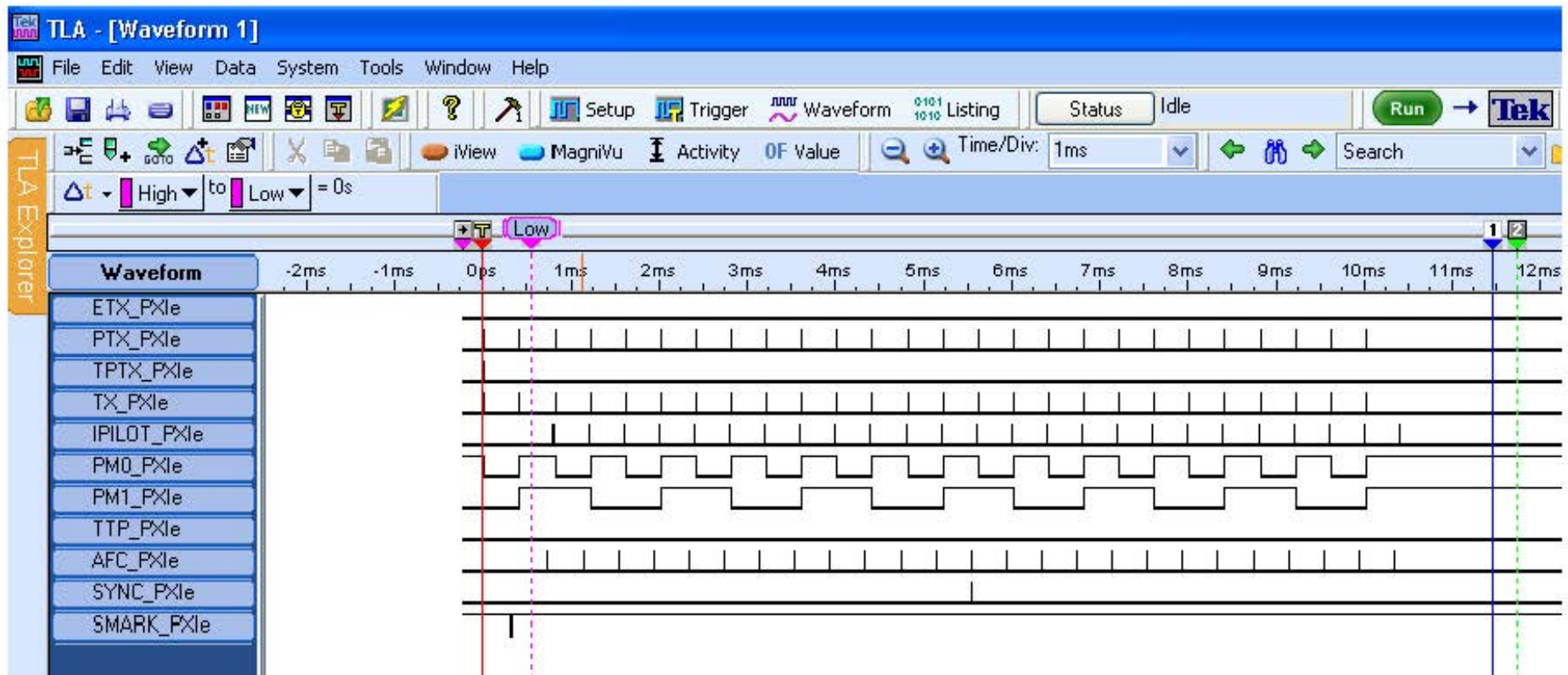


Figure 5.7: All syncs generated using PXIe prototype

5.5 Sync Generation Resolution

Timing resolution of the processes in the PXIe prototype was considered during the design phase. All processes in the FPGA module are running at a rate of 160 MHz (6.25 ns). This is the resolution at which output and syncs are being generated in the PXIe based system. Processing at the rate of 160 MHz means that sequential code in the FPGA has to be kept at a bare minimum, as all code within the SCTL has to be executed within one clock cycle and there is little time to execute code.

Since events in the SVCU have been defined with the finest resolution of 6.25 ns, all other activities defined with a coarse clock resolution of 100 ns has been generated with a 6.25 ns resolution. This greatly simplifies the implementation in the FPGA. Digital logic, counters, and shift registers, implemented in the FPGA to generate syncs and events, are able to be successfully synthesised and executed at 160 MHz as shown in Figure 5.3 and Figure 5.7.

5.6 GPS Time

To test the performance of the GPS, the NI 6683H and another GPS receiver system owned by Denel OTR were independently synchronised to GPS time. Each system was then configured to output a 1 PPS signal. The two 1 PPS signals were then captured throughout the day to analyse the drift between them.

The GPS satellites are only guaranteed to be within 100 ns of UTC [24]. The synchronisation offset or drift between the 6683H and Denel OTR GPS receiver system was assumed to be as high as 200 ns plus the synchronisation offset of each device to the GPS.

Capturing the two 1 PPS signal throughout the day resulted in a drift of less than 80 ns. The result illustrated in Figure 5.8 shows the synchronisation of the 6683H module to GPS is within the specified value of 100 ns of UTC. This was found satisfactory to be used as a reference time base to generate events for the PXIe based SVCU.

5.7 Jitter Analysis

In the previous study done by J Abraham, it was concluded that the root-sum-square of the jitter on the transmit-receive cycle (jitter budget) must not exceed 30 nanoseconds for the TR specified range error of 1.5 m. Jitter on the TX Sync, the ADC sampling clock



Figure 5.8: GPS test

and tracking gates were considered the most critical aspects contributing to the specified measurement accuracy of the TR as shown in (5.3). Jitter introduced when sending the TX Sync from the SVCU to the transmitter was also specified to be kept under 1 ns.

$$\text{Total}_{jit} = \sqrt{\text{TX}_{jit}^2 + \text{Sample}_{jit}^2 + \text{Gate}_{jit}^2} \leq 30\text{ns} \quad (5.3)$$

5.7.1 Signal Generation Clock Jitter

The accuracy and jitter in the clock, used in the generation of the critical TX, needs to be considered. The clock used by the 7961R module has a specified accuracy of 100 ppm and the maximum peak-to-peak jitter of the Virtex 5 FPGA based clock is listed in the Specifications Manual as 250 ps when configured using the PXIe_CLK_100.

5.7.2 Measurement Gate Jitter

The measurement gate jitter is identified as being the result of using a digital clock source to control early, late, and centre gate Integrate-and-Hold (I/H) circuits at a resolution of 6.25 ns. However, in the new SVCU design, digitisation is performed for the entire duration of the Radar Frame. From this sample set, digitised samples corresponding to the target range are identified and integrated. This eliminates any jitter introduced relating to the generation of range gate triggers.

5.7.3 Sample Clock Jitter

The ADCs on the 5170R module have a specified sample clock jitter of 400 fs RMS. This includes the effects of the converter aperture uncertainty and the clock circuitry jitter [36]. Using the Gaussian distribution of $\mu \pm 3\sigma$, the peak-to-peak value can be estimated as an $N\sigma$ factor such that [37, 38, 39]:

$$\begin{aligned} \text{Peak to Peak}_{jit} &= 6 \times \text{RMS ps} \\ \text{ADC}_{jit} &= 6 \times 0.4 \text{ ps} \end{aligned} \tag{5.4}$$

5.7.4 Jitter Budget

The total critical jitter contributing to the measurement can be defined as a root-sum-square:

$$\begin{aligned} \text{SVCU_PXIe}_{jit} &= \sqrt{\text{HSDIO}_{jit}^2 + \text{Sampling}_{jit}^2} \\ &= \sqrt{(250^2 + \text{Int_buffer}_{jit}^2) + 2.4^2} \text{ ps} \\ \text{SVCU_PXIe}_{jit} &= \sqrt{\text{Int_buffer}_{jit}^2 + 62505.76} \text{ ps} \end{aligned} \tag{5.5}$$

Using a jitter budget of 30 ns previously specified for 1.5 range error (RMS):

$$\begin{aligned} \text{SVCU_PXIe}_{jit} &= \sqrt{\text{Int_buffer}_{jit}^2 + 62505.76} \leq 30 \text{ ns} \\ \text{Int_buffer}_{jit} &\leq 29.99 \text{ ns} \end{aligned} \tag{5.6}$$

There is a 29.99 ns jitter buffer for any unidentified jitter contribution caused by the interface circuit. Fine-tuning the process has minimised all known or deterministic uncertainty.

5.8 PCB Impedance Matching

The fast transitions of the syncs in the SVCU meant when designing the interface PCB for distribution of syncs, a good PCB layout and design principals were adhered to. This entailed laying out the circuit design as an impedance controlled board whereby traces were routed with defined impedance. The main factors that influence the impedance are the trace's width, substrate thickness and properties of the material used to fabricate the PCB [40]. These factors are limited to what manufacturers can provide. For the designed Interface PCB, the combination of trace width, layer stack up and material available that provided impedance matching close to the desired value was used for fabrication as per Figure 5.9.

5.9 Ground Plane

Another factor taken into consideration while designing the PCB was separation of ground planes to reduce any interference caused by noisy components on the sensitive ones. The components used in the power supply, voltage regulators and amplifiers use an analogue ground. Components used for level shifting and clock generation use the digital ground. Implementation of this is illustrated in Figure 5.10. The two grounds are then tied together at one place in the PCB using vias as shown in Figure 5.11.

Components in the PCB have also been grouped together to separate the analogue components from the sensitive digital ones. Simple as it is, this is regarded as good practice for noise reduction. It also brings about an organisation to the layout of components and makes routing simpler. Provision has been made on the digital lines of the level shifters, by adding a footprint, to add select-on-test capacitors in the case where additional tuning is required.

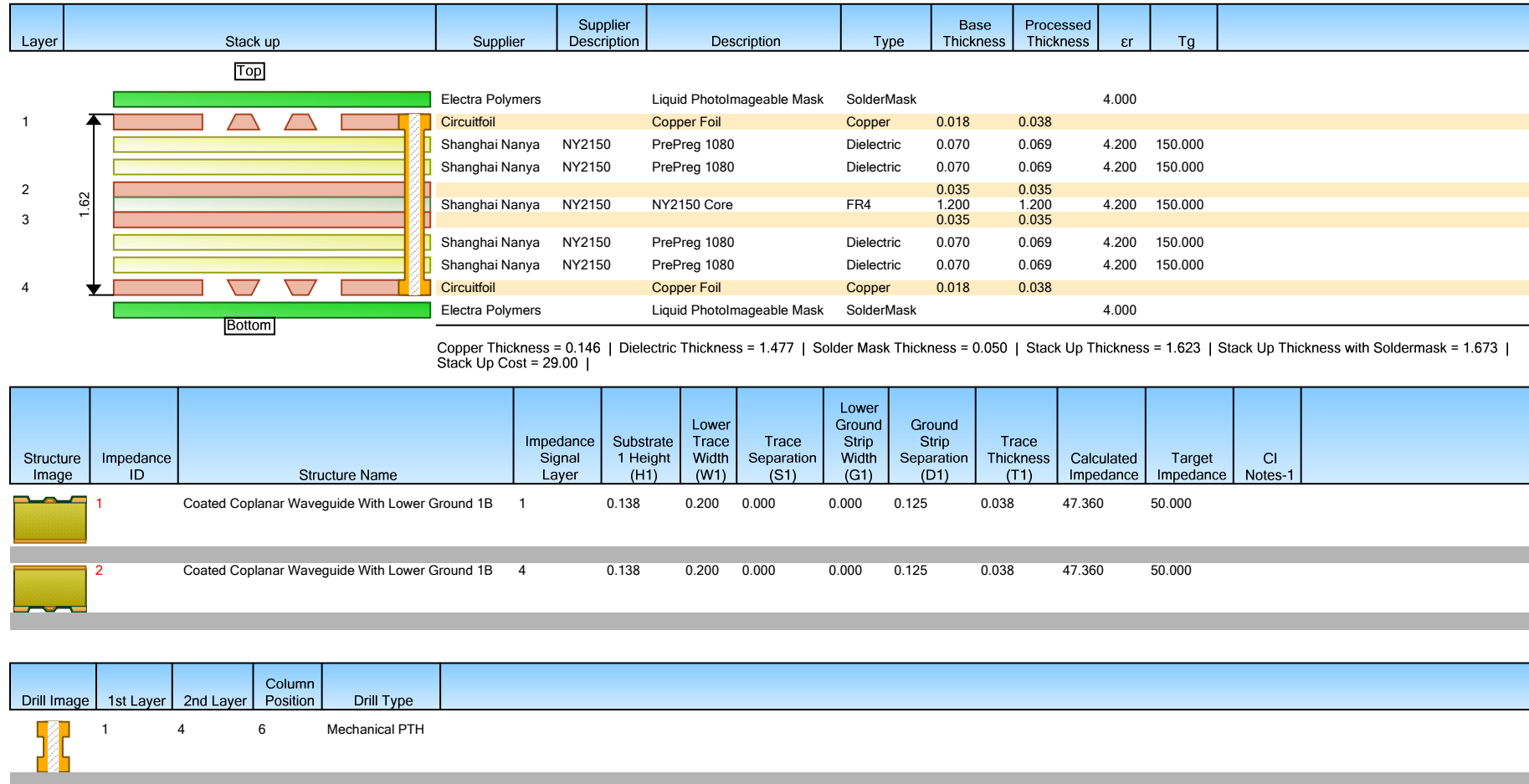


Figure 5.9: Custom stack PCB fabrication

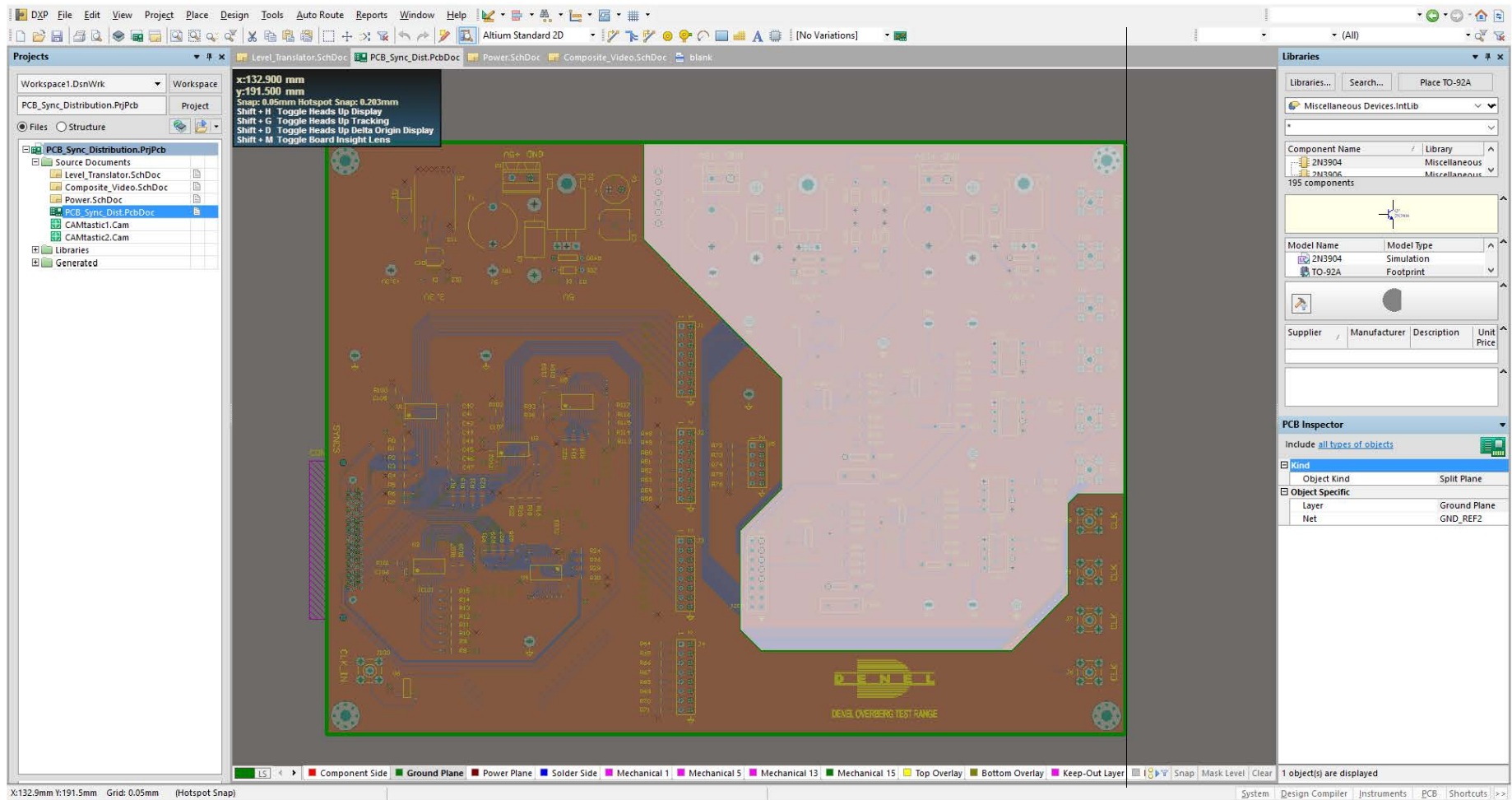


Figure 5.10: Split ground reference

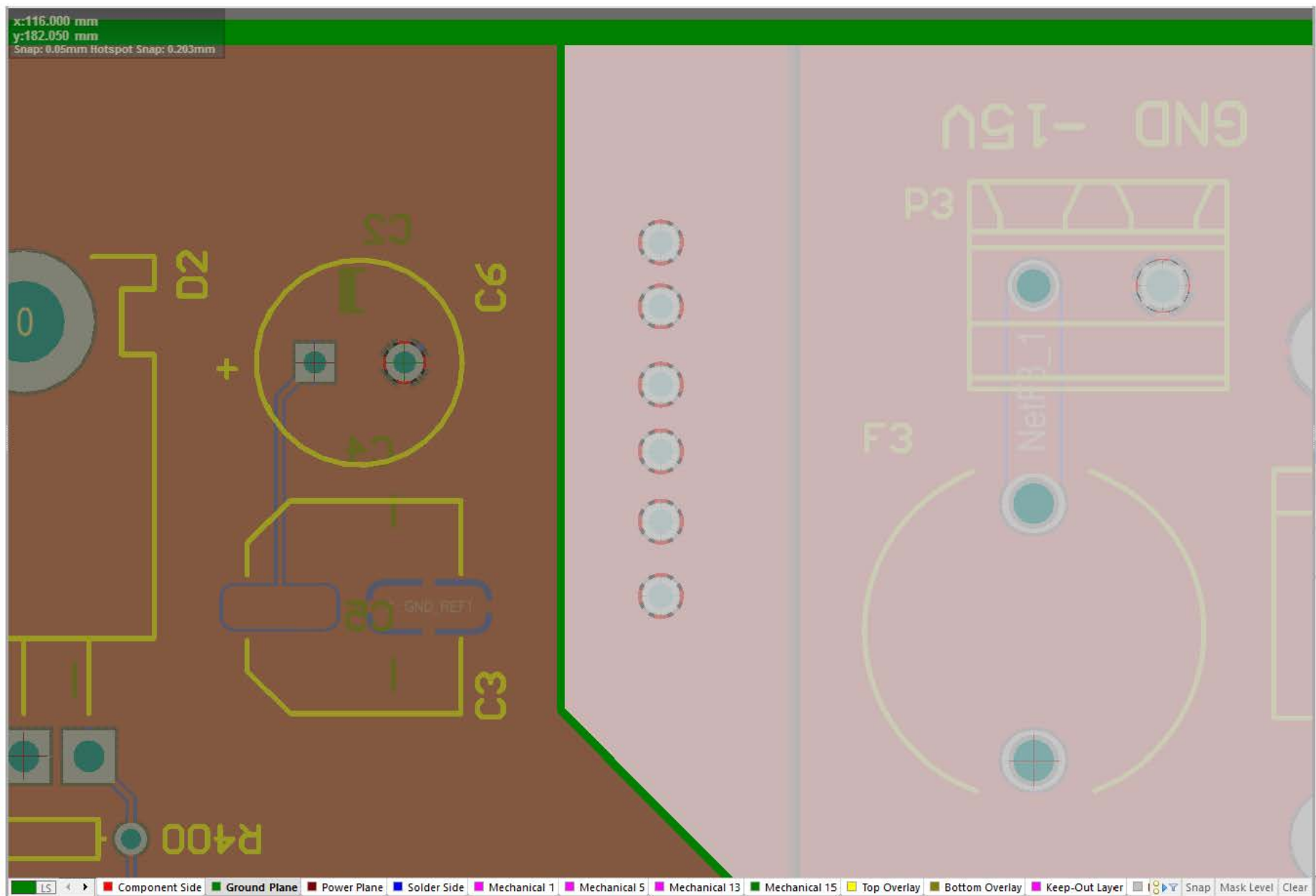


Figure 5.11: Ground plane via Stitching

5.10 Embedded Controller

The process within the SVCU is considered crucial for the operation of the TR. Once configured, FPGA modules of the PXIe work indefinitely and various operations are executed in parallel. This makes the process deterministic. However, the Embedded Controller Module is based on the Intel i5 Processor where tasks are being performed sequentially. Although it is capable of handling a large amount of processes, the number of tasks it needs to perform is kept at a bare minimum. Its primary task currently is to communicate with the master computer and FPGA modules to constantly engage in reading and sending data.

Optional tools are incorporated in the functions carried out by the embedded controller. The Instrument Design Library for the 5170R makes provision for the embedded controller to read some system monitoring parameters of the FPGA module such as temperature and power consumption as shown in Figure 5.12. A UDP message decoding function was also created as a diagnostic tool. This decoding function converts and displays (Figure 5.13) parameters received via UDP into values that can be easily understood: units of time, functions selected and mode of operation. Since the TRs are frequently operational for long periods, these tools become valuable for providing the status of the hardware and parameters received without the system being interrupted.

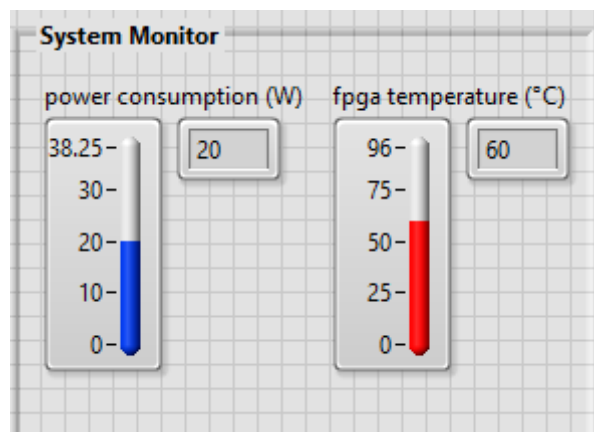


Figure 5.12: System monitoring tools

A multi record or data streaming example project is readily available for the 5170R module. It is an example program that lets the 5170R module operate as an oscilloscope. Digitised samples from the FPGA are transferred to the embedded controller and plotted into a graph in the LabVIEW front panel. This example project was modified by adding the fractional decimator to produce digital data at a sampling rate of 160 MHz and plot a waveform graph. This modified project can be run separately (when SVCU tasks are not running) to view the digitised sample as an additional form of diagnosis tool.

SVCU Instructions		Correction Parameters	
Message Counter 0 /255		Frame Width 0 ms	
No: Filling PRIs 0		No: Recieving PRIs 0	
		PRI Duration 0 ns	
Time : Second 0		Time : uSecond 0	
Mid Recieving Frame Offset 0			
Detection Filter Width 0.5 us		Tracking Filter Width 0.5 us	
TX Pulse Width 0.5 us		Coding 0 ns	
Detection Window Amb Range 0 ns		Tracker Amb Range 0 ns	
Test Target Amb Range 0 ns		Tracker Range Increment / PRI 0 usec/PRI	
Skin to Beacon Delay 0 ns		Test Target Increment / PRI 0 ns /PRI	
		Pilot Range 0 ns	
I/Q Correction Do not Apply Correction		Detection Window Fixed	
Skin / Beacon Tracking Skin		Pilot Modulation OFF - Fixed	
		Frequencv PRF/4	
Next Frame Continuation		Test Target Simulate	
Request for NOP None		Special Transmission Mode Normal Ambiguity	
Auto Callibration Disable ADC Controller Calibration		Range Calibration No Range Calibration Frame	
MSG Source System Computer			
NOP Resume No Change			
Generate TX Signal 4 Before Detection Window			

Figure 5.13: UDP message diagnostic window

5.11 Summary

In this chapter the key findings of the development project were discussed.

The dynamic range of the ADCs in the 5170R module was calculated and established that it was an improvement on the previous system. Tests were conducted to verify the output of the fractional decimator. A delay was added in the FPGA of the digitiser module to align the trigger with the first sample output from the decimator. The tests were concluded by capturing digital samples continuously for each radar frame during a live flight test involving an aircraft.

The analogue properties of the syncs generated in the new SVCU was discussed in detail. The problem areas of the syncs identified in the original SVCU system such as longer transition time, overshoot, fluctuation in logic levels and variation in position was eliminated in the syncs generated in the 7961R module. This was possible by using logics running at high clock resolution and HSDIO adapter module which has a specified minimum transition time of 5 ns.

The total jitter budget (RMS) of the TR was calculated. This included any known jitter from the time the RF energy is transmitted to the return echo is integrated into range gates for tracking and measurement. The new FPGA based SVCU is able to meet the specified jitter budget of 30 ns (RMS). Special attention was given when designing the Interface PCB. Impedance matching, power planes setup, and layout techniques were also discussed in this chapter.

The new SVCU's timebase was also tested against another GPS based timebase system. The 1 PPS reference signal generated by both systems showed that the 6683H was able to synchronise to another timebase with an 80 ns drift between them, when tested for an entire day. The value extracted, from the data sheet, also specifies that the 6683H module is always able to be within the 100 ns of UTC.

A LabVIEW user interfaces was created as a diagnostic tool for the SVCU system. The instruction messages received from the MCP via UDP can be decoded into values that can be easily understood: such as units of time, functions selected, and mode of operation. Some system monitoring parameters of the FPGA based digitiser module such as temperature and power consumption are also shown in the LabVIEW interface.

The next chapter concludes the dissertation by making recommendation and outlining future work based on the findings discussed in this chapter.

Chapter 6

Conclusion and Future Work

This chapter discusses the outcome of the SVCU re-development project. Based on results achieved during measurement of the previous system and development of a prototype, appropriate conclusions are drawn. The primary objectives set out at the beginning of this report were fulfilled. A full analysis of the most critical requirements of the SVCU was performed. A prototype based on the NI PXIe platform was built according to the requirements and with the possibility to implement the functions of other subunits of the TR in the available FPGA resources in the future.

6.1 Baseline Requirement

A revised set of baseline requirements has been generated for functions within the SVCU as set out in Chapter 3 of this report. This was deemed necessary as various technology changes have been implemented on the SVCU and other subunits of the TR over the years. Information on some of the functions or subunits of the previous SVCU is not available. A comprehensive list of syncs and their properties currently implemented in the TR has been documented and critical aspects of baseband video processing have been noted. Synchronisation and timebase requirements have been outlined. Overall functions and use of resources in the PXIe based SVCU have been optimised.

6.2 Deployment of the SVCU

Integrating the SVCU into the current system means making a permanent change to the interfaces within the TR. As the TRs are used for testing of advanced guidance and

avionics systems, errors that result in loss of target will have an impact on the quality of service of Denel OTR. The system is currently being observed and tested in parallel. The prototype SVCU is planned for an Acceptance Test in the second half of 2017. The system will be integrated to one of the TRs upon acceptance and deployment to the remaining two TRs will be planned.

6.3 PXIe System as a Digital Back End

The prototype development also acted as an evaluation of the PXIe system to be used as a digital back end of the TR. Its backplane and clock reference are adequate to run the necessary FPGA modules to perform the most stringent synchronisation and A/D processes. Its modular setup means additional modules can be added to the current system without affecting any process. The NI PXIe system brings an advantage whereby all hardware and software used are from a single supplier. All functions in the previous SVCU system have been converted to functions or VIs in LabVIEW and LabVIEW FPGA as previously discussed and set out in Table 4.1. These functions can be easily and individually modified without affecting other functions (as long as the general operation structure of the SVCU is kept). In conclusion, the advantages and improvements brought by the PXIe and the FPGA-based SVCU system is as follows:

Deterministic Hardware

- All time critical and real-time processes are being run on hardware.
- Independent and parallel execution of processes.

Form Factor

- Modular design.
- Ability to add modules to perform the tasks of another subsystem of the TR.
- Space efficient.
- Visual feedback (graphs and indicators).

Resource Management

- Time spent on building the prototype is immensely reduced by using LabVIEW and its tools.

- Budgets optimised by making provision to modernise other subsystems of the TR using the existing hardware platform.

Stability

- Easy to understand graphical programming (similar to block diagram) for diagnostics and easily re-configurable.
- Low maintenance.

6.4 Future Work and Recommendations

6.4.1 Digital A/R Scopes

The A/R Scopes used in the TR have become obsolete. A project has been initiated to replace them with an improvement in the 2017/18 financial year. After initial investigation and research, the TPC-2230 Touch Panel Computers (TPC) from National Instruments were recommended to be used with the current PXIe solution to the SVCU. The Touch-panel computers shown in Figure 6.1 [15] have been procured to develop a prototype to produce the digital representation of the current A/R Scopes. The TPCs have an embedded processor and 2 Gigabit Ethernet ports amongst other common peripherals.

The samples digitised within the acquisition cycle will be sent via Ethernet to the TPCs. The Embedded Controller of the TPCs will receive these digitised samples and convert them into graphical displays. The TRIG SYNC, SEARCH SYNC, TRACK SYNC and PILOT SYNC will then be superimposed on the graphical display to produce the digital equivalent of CV1 and CV2 being displayed on the current analogue A/R scopes.



Figure 6.1: TPC-2230 Touch Panel Computer

The TPCs will have to handle requests from the user to only show composite video

for selected sum or difference channels. By receiving a continuous stream of data and processing them on the TPCs, the PXIe based SVCU will be allowed to perform its critical tasks without any interruptions.

6.4.2 Digital Down Conversion

The high sampling rate of PXIe 5170R makes it possible to digitise signals at the IF2 (30 MHz) stage. The samples can be brought down to baseband level by implementing Digital Down Converters (DDCs) in the FPGA. Figure 6.2 is a DDC model designed in LabVIEW FPGA based on the example provided by NI, using Xilinx IP CORES [41]. Xilinx offers a CORE Generator configuration utility to implement optimised FIR and numerically controlled oscillator/digital sinusoid synthesis IP in the FPGA.

The DDC model performs the task of the Quadrature Demodulator Modules that are situated in the receiver subsystem of the TR. Due to obsolescence, a project to modernise the receiver sub-unit of the TR is also planned in the future. The FPGA-based DDC function is recommended to be implemented in the current 5170R module. This allows the functions of receiver subunits of the TR to be combined with the SVCU without having to procure additional hardware. This will require extensive investigation of other functions of the receiver subsystems before being ported into the 5170R module.

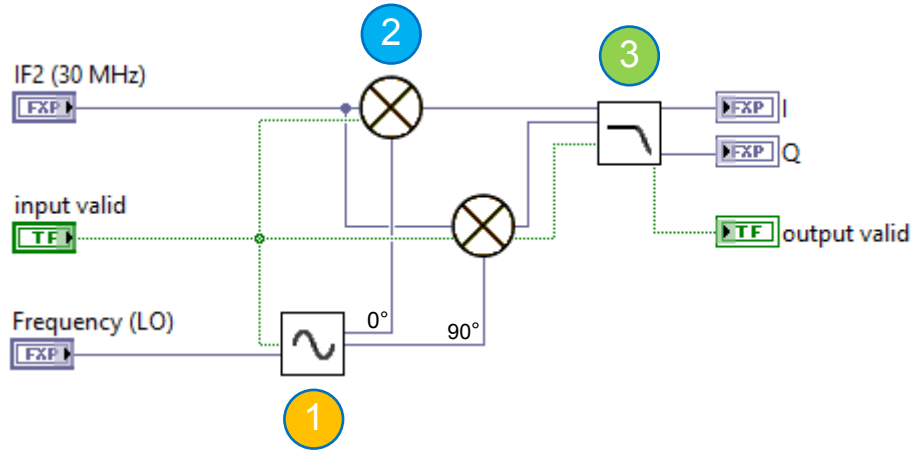


Figure 6.2: DDC in NI FPGA

The DDC technique will bring the following improvement in the TR receiver subsystem [42]:

Digital stability: The system will work indefinitely, no fine-tuning and calibration will

Table 6.1: Components of FPGA-based DDC

		DDS Compiler
		High Throughput Multiplication
		FIR filter

be required. The tolerances of the discrete components will not be a factor and the system will not be affected due to abrupt temperature change or manufacturing processes.

Controllability: DDCs can be implemented in the existing 5170R FPGA-based hardware and re-configured to produce the desired output.

Form Factor: Sampling at a higher frequency or IF-level and reducing the current number of channels where A/D conversion is being performed. The output from a single ADC can be configured to work with multiple parallel processes and implementing a DDC in the 5170R module will only consume a fraction of the FPGA's resources.

6.4.3 Software Defined Receiver

Component obsolescence is a factor that affects the majority of the subsystems of the TR. This brings challenges such as maintenance, continuity, quality, cost management and support relating to the current system. Recent years have brought many improvements to the transmitter and master computer. A requirement to have the receiver system of the TR modernised has been generated and planned in the near future. In addition to this intended maintenance and continuous improvement, a request for new features has surfaced such as the ability to simulate a moving target for subsystem diagnostics.

Procurement of a Vector Signal Transceivers (VST) from NI (Figure 6.3) [15] has been proposed for evaluation as a potential replacement of the total TR receiving system by incorporating it within the current SVCU PXIe prototype.

The NI VST combines the functionality of a vector signal generator, vector signal analyser, and high-speed serial interface with FPGA-based real-time signal processing and control [43]. Baseband video processing functions written in the 5170R module can be implemented in the VSTs without any major changes. The VSTs will also give the ability to emulate various subsystems of the TR on a digital platform. IF or RF signals can be generated and injected within the transceiver module to model scenarios, moving targets



Figure 6.3: Vector Signal Transceiver

and perform calibrations. Functions of subunits of the receiving systems can be ported to the VST in segments, resulting in a Software Defined Receiver for the TR. VST is recommended as a long term solution for obsolescence management of components of the TR.

Appendix A

System Message from Master Computer

This section contains a detailed description of the format of the message sent from the Master Computer to the SVCU. Commands and Status information were derived from the specification of the Mil-Std-1553B Serial Databus, known as the MUXBUS used in the OTR TR System [17].

SVCU SYSTEM STATUS MESSAGE SPECIFICATIONS & REQUIREMENT:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WORD 0	ECHOED COMP. MSG. COUNTER								MESSAGE COUNTER							
WORD 1	MICROSECONDS FIELD OF MID-RECEIVING TIME															
WORD 2	NOT USED								M	NOT USED				MSB - USEC FLD		
WORD 3	SECONDS FIELD OF MID-RECEIVING TIME															
WORD 4	SVCU STATUS INDICATION															
WORD 5	SVCU STATUS INDICATION															
WORD 6	ERROR REASON CODE															
WORD 7	SPARE															

WORD 0 - MESSAGE COUNTER

BITS 8-15	MESSAGE COUNTER A NUMBER MODULE 256 TO CERTIFY SYNCHRONIZATION BETWEEN SVCU CONTROLLER AND SYSTEM COMPUTER.
BITS 0-7	NOT USED

WORDS 1-3: MID RECEIVING FRAME ABSOLUTE TIME

WORD 1 - MICROSECONDS FIELD

BITS 0-15	THE LSB'S OF MICROSECONDS FIELD IN MID-RECEIVING ABSOLUTE TIME. THE FIELD CONSISTS OF 20 BITS. THEY ARE DIVIDED INTO TWO WORDS - THE 4 MSB'S ARE WRITTEN IN WORD 2 AND THE 16 LSB'S ARE WRITTEN IN THIS WORD.
DESCRIPTION:	LSB OF DWORD
RESOLUTION:	LSB = 1 USEC
RANGE:	0 TO 1048575 USEC (OF THE TOTAL FIELD)
POSSIBLE VALUES:	0 TO 999999 USEC

WORD 2 - MSB OF THE SEC & USEC FIELDS

BIT 15-12	THE MSB'S OF THE MICROSECONDS FIELD IN THE MID RECEIVING ABSOLUTE TIME - SEE WORD 1.
	DESCRIPTION: FIELD IN MSW OF DWORD
	RESOLUTION: LSB = 65536 USEC
BITS 11-8	NOT USED
BIT 7	THE MSB OF THE SECONDS FIELD IN THE MID RECEIVING ABSOLUTE TIME - SEE WORD 3.
	DESCRIPTION: FIELD IN MSW OF DWORD
	RESOLUTION: LSB = 65536 SEC
BITS 0-6	NOT USED

WORD 3 - SECONDS FIELD

BITS 0-15 THE SECONDS FIELD IN THE MID-RECEIVING ABSOLUTE TIME.
ACTUALLY 17 BITS REPRESENT THE SECONDS FIELD. THEY ARE
DIVIDED INTO TWO WORDS - THE MSB IS WRITTEN IN WORD 2 (BIT 7)
AND THE OTHER BITS ARE WRITTEN IN THIS WORD.

DESCRIPTION: LSB OF DWORD
RESOLUTION: LSB = 1 SEC
RANGE: 0 TO 131071 SEC (OF THE TOTAL FIELD)
POSSIBLE VALUES: 0 TO 86399 SECONDS (ONE DAY)

WORD 4-7: SVCU Status Indication

NOT USED – STATUS MESSAGES WHICH CONSISTED STATUS OF EACH SVCU SUB_UNIT HAS
BEEN OVERHAULED

SVCU - SYSTEM DATA-TO-SVCU MESSAGE SPECIFICATION & REQUIREMENT:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WORD 0	. MSG. COUNTER								FRAME WIDTH							
WORD 1	NUMBER OF FILLING PRI'S								NUMBER OF RECEIVING PRI'S							
WORD 2	PRI DURATION															
WORD 3	DETECTION FILTER WIDTH					TRACKING FILTER WIDTH			RANGE BIN WIDTH							
WORD 4	NOT USED					XMIT PULSE WIDTH			CODING							
WORD 5	DETECTION WINDOW AMBIGUOUS RANGE															
WORD 6	NOT USED												MSB OF TK.A.R			
WORD 7	TRACKER AMBIGUOUS RANGE (TK.A.R)															
WORD 8	TRACKER RANGE INCREMENT PER PRI															
WORD 9	NOT USED												MSB OF T.T.A.R			
WORD10	TEST TARGET AMBIGUOUS RANGE (T.T.A.R)															
WORD11	TEST TARGET INCREMENT PER PRI															
WORD12	SKIN TO BEACON DELAY															
WORD13	PILOT RANGE															
WORD14	MICROSECONDS FIELD OF ABSOLUTE TIME															
WORD15	NOT USED				M				NOT USED				MSB OF USEC FIELD			
WORD16	SECONDS FIELD OF ABSOLUTE TIME															
WORD17	MID RECEIVING FRAME OFFSET FROM TRIAL PULSE															
WORD18	COMMAND WORD 1															
WORD19	COMMAND WORD 2															

WORD 0 - MESSAGE COUNTER & FRAME WIDTH

BITS 8-15	FRAME WIDTH - FRAME DURATION TRUNCATED TO MILLISECONDS
	DESCRIPTION: UNSIGNED INTEGER
	RESOLUTION: LSB = 1 MILLISECOND
	RANGE: 0 TO 255 MILLISECONDS
	POSSIBLE VALUES: 15 TO 127 MILLISECONDS
BITS 0-7	MESSAGE COUNTER - A NUMBER MODULE 256 TO CERTIFY SYNCHRONIZATION BETWEEN SVCU CONTROLLER AND SYSTEM COMPUTER.

WORD 1 - NUMBER OF PRI'S

BITS 8-15	NUMBER OF RECEIVING PRI'S - THE NUMBER OF PRI'S IN THE RECEIVING FRAME OF THE TRANSMITTING FRAME.
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	DESCRIPTION:	UNSIGNED INTEGER
	RANGE:	0 TO 255
	POSSIBLE VALUES:	0 TO 32
BITS 0-7	NUMBER OF FILLING PRI'S - THE NUMBER OF PRI'S IN THE FILLING FRAME OF THE TRANSMITTING FRAME. THIS NUMBER INCLUDES THE TRIAL PRI.	
	DESCRIPTION:	UNSIGNED INTEGER
	RANGE:	0 TO 255
	POSSIBLE VALUES:	1 TO (MAXIMUM_NUMBER)

WORD 2 - PRI DURATION

BITS 0-15	PRI DURATION - REPRESENTS THE PRI DURATION IN THE FILLING FRAME AND THE RECEIVING FRAME (THE FIGURE IS DERIVED FROM THE PRODUCT OF M*N).	
	DESCRIPTION:	UNSIGNED INTEGER
	RESOLUTION:	LSB = 100 NSEC
	RANGE:	0 TO 6.5535 MSEC
	POSSIBLE VALUES:	333.33 USEC TO 6.5535 MSEC

WORD 3 - RANGE BINS, FILTER WIDTHS

BITS 8-15	RANGE BIN WIDTH - THE FIELD REPRESENTS THE INTERVAL BETWEEN THE 20 SUCCESSIVE SAMPLES IN THE DETECTION ADC UNIT.	
	DESCRIPTION:	UNSIGNED INTEGER
	RESOLUTION:	LSB = 100 NSEC
	RANGE:	0 TO 25.5 USEC
	POSSIBLE VALUES:	300, 400, 700, 800, 1800, 2000, 3500 NSEC
BITS 4-7	TRACKING FILTER WIDTH - THIS FIELD REPRESENTS THE REQUIRED INTEGRATE & HOLD TIME FOR THE MEASUREMENT ADC UNIT.	
	DESCRIPTION:	UNSIGNED INTEGER
	RANGE:	0 TO 15
	POSSIBLE VALUES:	0 0.5 USEC 1 1.0 USEC 2 2.5 USEC 3 2.5 USEC 4-15 NOT USED
BITS 0-4	DETECTION FILTER WIDTH - THIS FIELD REPRESENTS THE REQUIRED LOW PASS FILTER FOR THE DETECTION ADC UNIT.	
	DESCRIPTION:	UNSIGNED INTEGER
	RANGE:	0 TO 15
	POSSIBLE VALUES:	0 0.5 USEC 1 1.0 USEC 2 2.5 USEC 3 2.5 USEC 4-15 NOT USED

WORD 4 - PULSE WIDTH & CODING

BITS 8-15 CODING - THE GAP REQUIRED BETWEEN THE TWO TRANSMIT TRIGGERS (TX) PULSES TRANSMITTED IN BEACON MODE.

DESCRIPTION: UNSIGNED INTEGER
RESOLUTION: LSB = 100 NSEC
RANGE: 0 TO 25.5 USEC
POSSIBLE VALUES: 0 TO 12.7 USEC

BITS 4-7 XMIT PULSE WIDTH - THE TRANSMISSION PULSE WIDTH

DESCRIPTION: UNSIGNED INTEGER
RANGE: 0 TO 15
POSSIBLE VALUES: 0 0.5 USEC
 1 1.0 USEC
 2 2.5 USEC
 3 2.5 USEC
 4-15 NOT USED

BITS 0-3 NOT USED

WORD 5 - DETECTION WINDOW RANGE

BITS 0-15 DETECTION WINDOW RANGE - AMBIGUOUS RANGE OF THE FIRST RANGE BIN IN THE DETECTION WINDOW. THE VALUE IS TRUE FOR THE FIRST VALID PRI OF THE RECEIVING FRAME.

DESCRIPTION: UNSIGNED INTEGER
RESOLUTION: LSB = 100 NSEC
RANGE: 0 TO 6.5535 MSEC
POSSIBLE VALUES: (MINIMUM_RANGE) TO (MAXIMAL_RANGE)

WORD 6 - MSB'S OF TRACKER AMBIGUOUS RANGE

BITS 12-15 MSB'S OF THE TRACKER AMBIGUOUS RANGE - SEE WORD 7

RESOLUTION: LSB = 409.6 USEC

BITS 0-11 NOT USED

WORD 7 - LSB'S OF TRACKER AMBIGUOUS RANGE

BITS 0-15 LSB'S OF TRACKER AMBIGUOUS RANGE – AMBIGUOUS RANGE OF THE MEASUREMENT (NO. 1) PULSE GATE. THE FIGURE CONSISTS OF 20 BITS. THEY ARE DEVIDED INTO TWO WORDS - THE 4 MSB'S ARE WRITTEN IN WORD 6 AND THE 16 LSB'S ARE WRITTEN IN THIS WORD.

DISCRIPTION: UNSIGNED INTEGER
RESOLUTION: LSB = 6.25 NSEC
RANGE: 0 TO 6.5534 MSEC (OF THE TOTAL FIGURE)
POSSIBLE VALUES: MINIMUM_RANGE TO 6.5534 MSEC

WORD 8 - TRACKER RANGE INCREMENT PER PRI

BITS 0-15 TRACKER RANGE INCREMENT PER PRI - THE INCREMENT OF THE MEASUREMENT (NO. 1) PULSE BETWEEN TWO ADJACENT PRI'S IN THE RECEIVING FRAME.

DESCRIPTION: TWO'S COMPLEMENT INTEGER
 RESOLUTION: LSB = 6.25 NSEC/PRI
 RANGE: -204.8 TO +204.79375 USEC/PRI
 POSSIBLE VALUES: -(MAXIMUM_VELOCITY)
 TO+(MAXIMUM_VELOCITY)

WORD 9 - MSB'S OF TEST TARGET AMBIGUOUS RANGE

BITS 12-15 MSB'S OF THE TEST TARGET AMBIGUOUS RANGE - SEE WORD 10.
 LSB = 409.6 USEC

BITS 0-11 NOT USED.

WORD 10 - LSB'S OF TEST TARGET AMBIGUOUS RANGE

BITS 0-15 LSB'S OF TEST TARGET AMBIGUOUS RANGE - THE FIELD REPRESENTS THE AMBIGUOUS RANGE OF THE TEST TARGET (OR AS AN OPTION - THE AMBIGUOUS RANGE OF THE MEASUREMENT (NO. 2) PULSE GATE). THE FIGURE CONSISTS OF 20 BITS. THEY ARE DIVIDED INTO TWO WORDS - THE 4 MSB'S ARE WRITTEN IN WORD 9 AND THE 16 LSB'S ARE WRITTEN IN THIS WORD.

DESCRIPTION: UNSIGNED INTEGER
 RESOLUTION: LSB = 6.25 NSEC
 RANGE: 0 TO 6.5534 MSEC
 POSSIBLE VALUES: (MINIMUM_RANGE) TO (MAXIMAL_RANGE)

WORD 11 - TEST TARGET INCREMENT PER PRI

BITS 0-15 TEST TARGET INCREMENT PER PRI - THE INCREMENT OF THE TEST TARGET (OR AS AN OPTION - THE INCREMENT OF THE MEASUREMENT (NO. 2) PULSE GATE) BETWEEN TWO ADJACENT PRI'S IN THE RECEIVING FRAME.

DESCRIPTION: TWO'S COMPLEMENT INTEGER
 RESOLUTION: LSB = 6.25 NSEC
 RANGE: -204.8 TO +204.79375 USEC/PRI
 POSSIBLE VALUES: -(MAXIMUM_VELOCITY) TO
 +(MAXIMUM_VELOCITY)

WORD 12 - SKIN TO BEACON DELAY

BITS 0-15 SKIN TO BEACON DELAY - COMPENSATION FOR A-SCOPE VIDEO BEACON MARKER.

DESCRIPTION: SIGNED INTEGER
 RESOLUTION: LSB = 100 NSEC
 RANGE: -3.2768 TO +3.2768 MSEC
 POSSIBLE VALUES: 0 TO 50 USEC

WORD 13 - PILOT RANGE

BITS 0-15 PILOT RANGE - THE RANGE OF THE PILOT SIGNAL IN THE RECEIVING FRAME.

DESCRIPTION: UNSIGNED INTEGER
 RESOLUTION: LSB = 100 NSEC
 RANGE: 0 TO 6.5535 MSEC

WORDS 14-16 - TRANSMISSION ABSOLUTE TIME - THE ABSOLUTE TIME TO APPLICABLE ONLY FOR A NEW FRAME. SINCE THE 1ST TIMING SIGNAL IN THE NEW FRAME IS THE ETX, THIS TIME SHOULD BE 30 MICROSECONDS BEFORE THE TRANSMISSION OF THE 1ST PULSE.

WORD 14 - MICROSECONDS FIELD

BITS 0-15 THE LSB'S OF MICROSECONDS FIELD IN TRANSMISSION ABSOLUTE TIME. THE FIELD CONSISTS OF 20 BITS. THEY ARE DIVIDED INTO TWO WORDS - 4 MSB'S ARE WRITTEN IN WORD 15 AND THE 16 LSB'S ARE WRITTEN IN THIS WORD.

DESCRIPTION: LSB OF DWORD
 RESOLUTION: LSB = 1 USEC
 RANGE: 0 TO 1048575 USEC (OF THE TOTAL FIELD)
 POSSIBLE VALUES: 0 TO 999999 USEC

WORD 15 - MSB OF THE SEC & USEC FIELDS

BIT 15-12 THE MSB'S OF THE MICROSECONDS FIELD IN THE TRANSMISSION ABSOLUTE TIME - SEE WORD 14.

DESCRIPTION: FIELD IN MSW OF DWORD
 RESOLUTION: LSB = 65536 USEC

BITS 11-8 NOT USED

BIT 7 THE MSB OF THE SECONDS FIELD IN THE TRANSMISSION ABSOLUTE TIME - SEE WORD 16.

DESCRIPTION: FIELD IN MSW OF DWORD
 RESOLUTION: LSB = 65536 SEC

BITS 0-6 NOT USED

WORD 16 - SECONDS FIELD

BITS 0-15 THE SECONDS FIELD IN THE TRANSMISSION ABSOLUTE TIME. ACTUALLY 17 BITS REPRESENT THE SECONDS FIELD. THEY ARE DIVIDED INTO TWO WORDS - THE MSB IS WRITTEN IN WORD 15 (BIT 7) AND THE OTHER BITS ARE WRITTEN IN THIS WORD.

DESCRIPTION: LSB OF DWORD
 RESOLUTION: LSB = 1 SEC
 RANGE: 0 TO 131071 SEC (OF THE TOTAL FIELD)
 POSSIBLE VALUES: 0 TO 86399 SECONDS (ONE DAY)

WORD 17 - MID RECEIVING FRAME OFFSET FROM TRIAL PULSE

BITS 0-15 MID RECEIVING FRAME OFFSET FROM START OF THE TRIAL PRI , PLUS 1 MICROSECOND.

DESCRIPTION: WORD
 RESOLUTION: LSB = 812 NSEC
 RANGE: 0 TO 53.21442 MSEC

WORD 18 - COMMAND WORD 1 TO SVCU

BIT 15 TRANSMISSION - REQUIRES THE SVCU TO GENERATE THE TRANSMISSION TIMING SIGNALS.

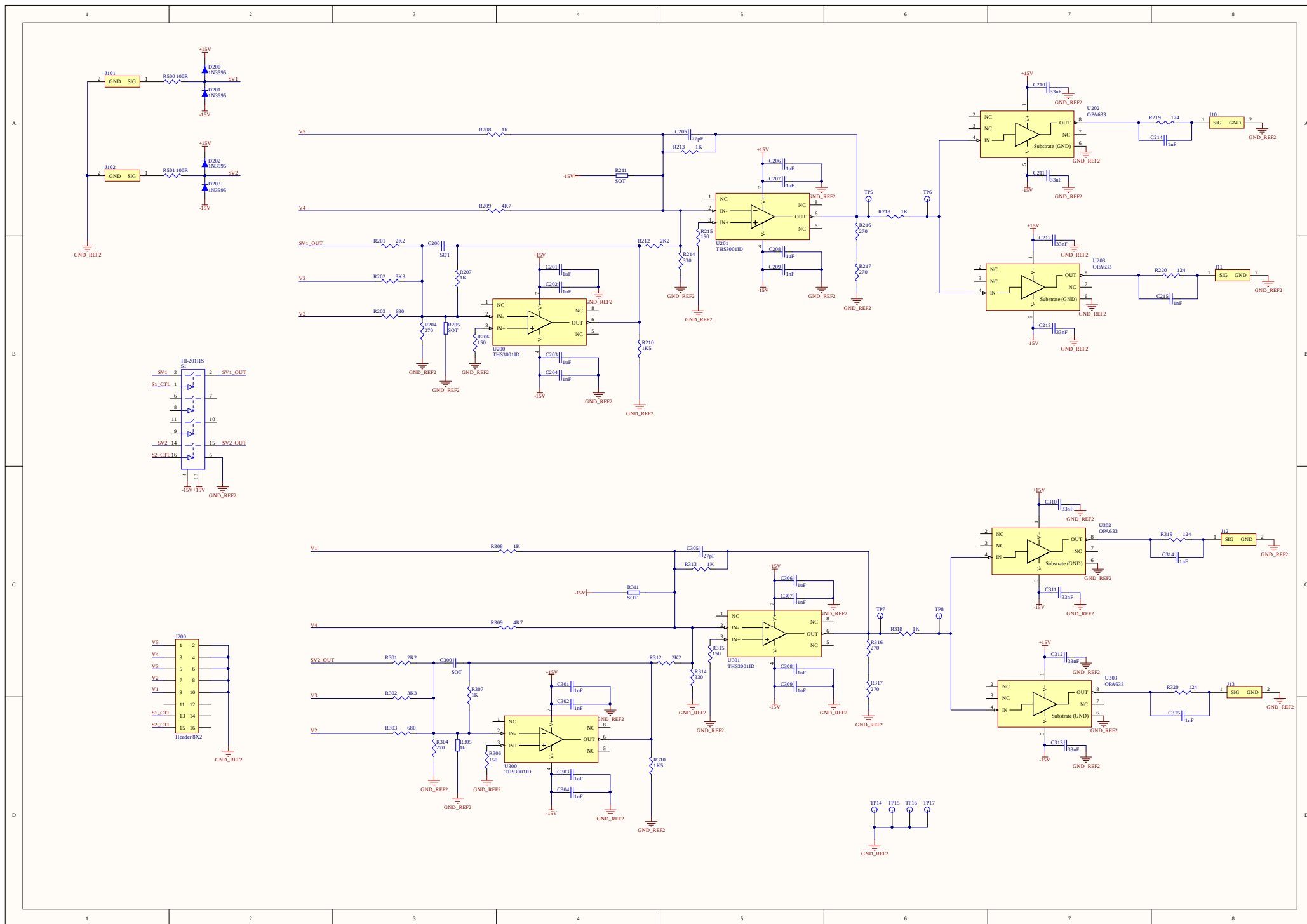
	'0'	NO TRANSMISSION - THE SVCU WILL NOT GENERATE THE TRANSMIT TRIGGER (TX) SIGNAL
	'1'	TRANSMISSION - ALL THE TIMING SIGNALS RELATED TO THE TRANSMISSION WILL BE GENERATED.
BIT 14		RECEIVE AND PROCESS - REQUIRES THE SVCU TO PROCESS AND SEND DATA TO THE SYSTEM COMPUTER THROUGH THE H.S.D.
	'0'	NO PROCESSING - THE SVCU WILL NOT PROCESS AND SEND THE VIDEO SAMPLES TO THE H.S.D.
	'1'	PROCESSING - THE SVCU WILL PROCESS AND SEND THE VIDEO SAMPLES TO THE H.S.D.
BIT 13		RANGE CALIBRATION - REQUIRES THE SVCU TO PERFORM A RANGE CALIBRATION FRAME.
	'0'	NO RANGE CALIBRATION FRAME
	'1'	PERFORM RANGE CALIBRATION FRAME
BIT 12		SPECIAL TRANSMISSION MODE - REQUIRES THE SVCU NOT TO GENERATE THE TRANSMISSION TIMING SIGNAL DURING THE RECEIVING FRAME.
	'0'	NORMAL AMBIGUITY MODE - THE SVCU WILL GENERATE ALL THE TIMING SIGNAL RELATED TO THE TRANSMISSION, DURING THE RECEIVING FRAME.
	'1'	SPECIAL AMBIGUITY MODE - THE SVCU WILL NOT GENERATE THE TRANSMIT TRIGGER (TX) SIGNAL, DURING THE RECEIVING FRAME.
BIT 11		SIMULATE TARGET - REQUIRES TARGET SIMULATION
	'0'	NO SIMULATION OF A TARGET
	'1'	SIMULATE A TARGET ACCORDING TO THE DATA IN WORDS 9-11
BIT 10		PILOT MODULATION FREQUENCY - DEFINES THE FREQUENCY AND THE TYPE OF THE PILOT PHASE MODULATION.
	'0'	PRF/4 - THE PILOT CYCLE IS 4 PRI'S WIDE, AND THE PHASE MODULATION IS AS FOLLOWS:
		1ST PRI - 0 DEGREES
		2ND PRI - 90 DEGREES
		3RD PRI - 180 DEGREES
		4TH PRI - 270 DEGREES
	'1'	PRF/2 - THE PILOT CYCLE IS 2 PRI'S WIDE, AND THE PHASE MODULATION IS AS FOLLOWS:
		1ST PRI - 0 DEGREES
		2ND PRI - 180 DEGREES
BIT 9		PILOT MODULATION ENABLE - DEFINES THE MODE OF THE PHASE PILOT MODULATION. IT CAN BE CONSTANT (0 DEGREES) OR A VARIABLE PHASE MODULATION.
	'0'	CONSTANT PHASE MODULATION
	'1'	VARIABLE PHASE MODULATION ACCORDING TO BIT 10
BIT 8		DETECTION WINDOW MOVING OR FIXED - DEFINES IF THE RANGE OF THE DETECTION WINDOW REMAINS CONSTANT DURING THE RECEIVING FRAME OR IT INCREMENTS AT THE SAME RATE OF THE TRACKER.
	'0'	FIXED RANGE OF THE DETECTION WINDOW
	'1'	MOVING RANGE OF THE DETECTION WINDOW

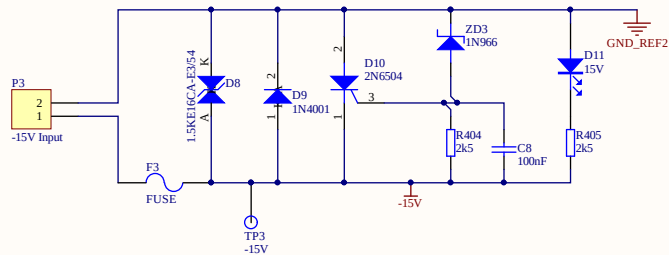
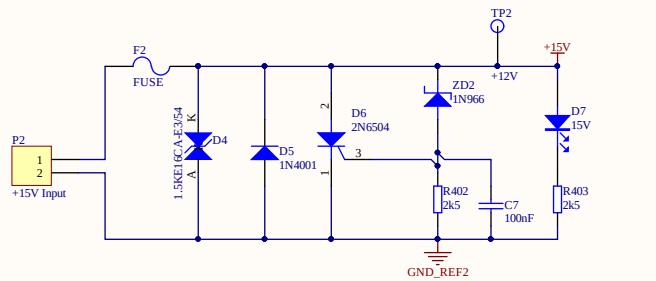
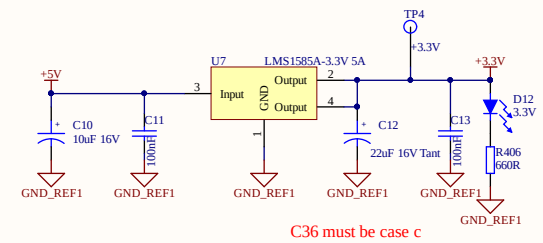
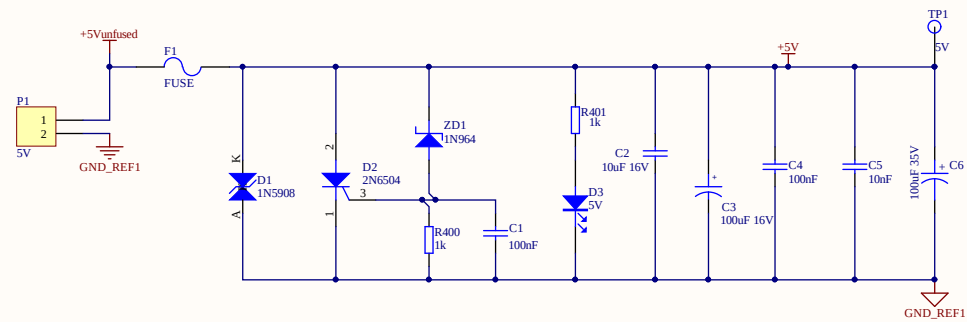
BIT 7	PILOT MEASUREMENT - DEFINES WHICH MEASUREMENT ADC UNIT WILL PERFORM THE PILOT MEASUREMENTS. '0' MEASUREMENT ADC UNIT (NO. 1) '1' MEASUREMENT ADC UNIT (NO. 2)
BIT 6	'0' ALL THE SUB-PULSES IN THE CYCLE WILL BE TRANSMITTED. '1' ONLY EFFECTIVE SUB-PULSES WILL BE TRANSMITTED.
BIT 5	AUTO CALIBRATION - ENABLES THE SVCU CONTROLLER TO APPLY THE A/D CONTROLLER CORRECTIONS. '0' DISABLE THE SVCU CONTROLLER TO APPLY THE A/D CONTROLLER CORRECTIONS. '1' ENABLES THE SVCU CONTROLLER TO APPLY THE A/D CONTROLLER CORRECTIONS.
BIT 4	REQUEST FOR NOP. '1' REQUEST BY THE COMPUTER FOR THE SVCU TO ENTER 'NOP' MODE.
BIT 3	NEW / CONTINUATION FRAME - DEFINES THE TYPE OF THE NEXT FRAME. '0' THE NEXT FRAME IS A CONTINUATION FRAME '1' THE NEXT FRAME IS A NEW FRAME.
BIT 2	SKIN / BEACON TRACK - DEFINES THE SELECTED TRACK VIDEO DURING THE NEXT FRAME. '0' TRACKING ON SKIN VIDEO '1' TRACKING ON BEACON VIDEO
BIT 1	I/Q CORRECTION - REQUIRES THE SVCU CONTROLLER TO APPLY THE I/Q CORRECTIONS. '0' NO I/Q CORRECTIONS TO BE APPLIED. '1' I/Q CORRECTIONS TO BE APPLIED.
BIT 0	SPARE.

Appendix B

Altium Schematics

This section contains the schematic diagrams of Interface PCB discussed in Section 2.4.5.





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