DESIGN AND ANALYSIS OF HIGH-SPEED ELECTRONICS FOR ELECTRO OPTICAL PAYLOAD OF SMALL SATELLITES

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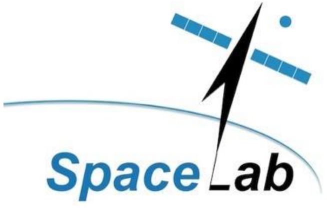

This dissertation is submitted in partial fulfilment of the requirements for the degree of Master of Philosophy in Space Studies

June 2022

SL20-08M

University of Cape Town

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ABSTRACT

With the increase in the resolution of the Earth observation satellites, the cameras on these satellites require more detectors to fulfil the swath need and also the image sensors have to operate at a very high-speed with the sensor electronics requiring faster clock rates and larger bandwidth. The sensor data handler has to transfer a large amount of data to the spacecraft in real time incorporating the outcomes of the signal integrity and power integrity analysis in the design. High-speed analysis is an important consideration for high resolution cameras and is often performed on the satellites.

This research work aims towards presenting the design and analysis of high-speed electronics for small Earth observation satellites. A methodology will be defined for the designing of high-speed electronics that will involve both the pre-layout and post-layout designs for signal and power integrity analysis. The proposed research work also provides the pre-layout and post-layout signal integrity analysis of the high-speed electronics and interfaces and it will also validate the signal integrity performance of the module by comparing it with standard performance parameters. Similarly, we will perform a pre-layout and post-layout power integrity analysis of the high-speed electronics and interfaces and its effects on the power lines and power planes.

ACKNOWLEDGEMENT

First of all, it is to thank Allah for providing me the skills for the completion of this dissertation. Secondly it is to acknowledge the guidance, efforts, and cooperation of all UCT staff and the guest speakers especially the supervision of Professor Peter Martinez that were found beneficial in this dissertation.

Special thanks to my family and friends especially my parents, brother and sisters for their sincere support and love.

Mohammad Naveed (NVDMOH001)

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LIST OF ACRONYMS

AC	Alternating Current
ADC	Analog-to-Digital Convertor
CAD	Computer Aided Design
CCD	Charge-Coupled Devices
CCLK	Configuration Clock
CDC	Camera Data and Control Unit
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DD	Displacement Damage
DDR	Dual Data Rate
DSP	Digital Signal Processor
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FDIR	Fault Detection, Isolation and Recovery
FPGA	Field Programmable Gate Array
GND	Ground
GP I/O	General Purpose Input/output
GSD	Ground Sampling Distance
IBIS	Input/output Buffer Information Specification
IBIS-AMI	Input/output Buffer Information Specification-Algorithm Modelling Interface
IC	Integrated Circuit
IDU	Image Detector Unit
IR	Ohmic Potential
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signal
MTF	Modular Transfer Function
NMOS	N-type Metal Oxide Semiconductor
OBD	On Board Data Unit
OC	Over-Current

PCB	Printed Circuit Board
PDN	Power Delivery Network
PI	Power Integrity
PMOS	P-type Metal Oxide Semiconductor
PRBS	Pseudorandom Binary Sequence
PROM	Programmable Read Only Memory
PSP	Plane Signal Plane
PSSP	Plane Signal Signal Plane
PWR	Power
PWU	Power Unit
RMS	Root Mean Square
SEE	Single Event Effect
SI	Signal Integrity
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SPICE	Simulation Program with Integrated Circuit
SSN	Simultaneous Switching Noise
TDI	Time Delay Integration
TID	Total Ionization Dose
TMTC	Telemetry and Telecommand
VHDL	Very High-speed Integrated Circuit Description Language
VRM	Voltage Regulator Module
VCC	Supply Voltage

1 INTRODUCTION

1.1 Background

Most of the remote sensing satellites have an electro-optical payload to examine, survey and investigate Earth resources like agriculture, weather, forestry, biodiversity and many other applications. The payload of a remote sensing satellite mainly comprises a telescope (mirrors, lenses, structure, opto-mechanics and thermal), focal plane (detectors, electronics, prism, glass, structure, thermal, harnesses), data handlers (electronics, structure, thermal, harnesses) as shown in Figure 1.1. The power to the payload is coming from the power units. To meet the system requirements for each type of detector electronics is optimally designed. The main functions of the electronics are to generate control and timing signals, drive the detector, process the data signals coming from the detector and quantize image information.

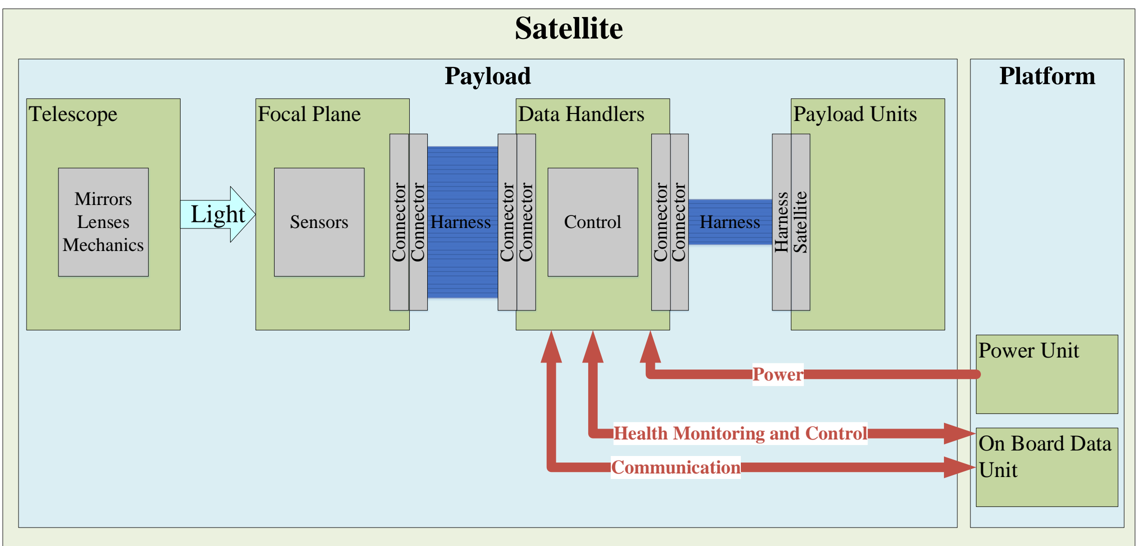


Figure 1.1: Satellite having payload and platform. The electro-optical payload cameras are mainly consisting of detectors, optics and electronics.

In very high-resolution imaging satellites, due to high ground sampling rate, the detector (CCD / CMOS) must be operated at a very high-speed. Time delay & integration (TDI) techniques for ongoing imaging is preferred to get better SNR & dynamic range at elevated resolution. [1] A large number of clocks and bias lines are required by the detector. [1] With the increase in the swath width and resolution the remote sensing satellites require more than one detector in a focal plane, which imposes the requirements of video ports from the sensor. The data coming from each detector is processed in such a way that it yields a 10/12-bit [2] (depending on the type of detector) digitized image. Table 1.1 shows some of the requirements of the Resourcesat-2 operating in-orbit with some future missions. [2]

Table 1.1: Requirements of the Resourcesat-2 and Future Missions. [2]

Payload	No. of Ports/Outputs	Readout Rate	Digitization	Data Rate	Total Data Lines
Resourcesat-2	40	312.5 kHz – 1.75 MHz	10 bit-12 bit	480 Mbps	>416
Future Missions	>60	>3 MHz	>11 bit	>1.9 Gbps	>700

This data is sent to the electronics for processing, formatting and transmission to the ground station. In earlier remote sensing satellite payloads parallel data transfer methods were used for the data transmission and reception.

Data rate can be calculated using equation 1.1 if all the parameters are known [2].

$$\begin{aligned} &\boldsymbol{Data\ Rate} \\ &= \boldsymbol{No.\,of\ Outputs}\ \textbf{OR}\ \boldsymbol{Ports\ X\ \ Digitization\ X\ Readout\ Rate} \end{aligned} \tag{1.1}$$

The parallel data has large number of data lines that requires multiple cables, leading to volume and weight issues for space missions. The high-speed data bring issues linked to crosstalk and data skew. One of the solutions for those multiple cables is to use serial communication. With serial communication the number of cables is decreased thus reducing the volume and weight issues. Even with serial communication the issues associated with high data rates are present. These issues can be sorted in the design using signal integrity and power integrity techniques.

1.2 Electronics in the space environment: Temperature, Vacuum and Radiation

The space environment is a very harsh environment that leaves a satellite and everything inside or outside it, especially electronics, exposed to more radiation. These radiations include solar energetic particles, solar wind, galactic cosmic rays and coronal mass ejections. The effects of the space environment can be found in a more detail in the article *"What could go wrong? The effects of ionizing radiation on space electronics"* [3]. In this article the radiation effects on electronics used in space is divided into three categories:

1.2.1 Total Ionization Dose (TID)

The total ionization dose is the integrated radiation dose over a given time period that a satellite acquires. These high energy ions can rearrange atomic bonds and break down the material properties. Over a period, the electronics are exposed to total ionization dose the insulation materials can become degraded decreasing the insulation capacity and conductive materials like resistors changing their overall characteristics. The biggest effect of the TID is on the PMOS and NMOS transistors. These transistors are mostly used as a switching element to propagate logic states throughout the circuit. [3]

The gate is ionized when it is exposed to radiations by the dose it absorbs, the electrons are moveable, but the “holes” are not. Over the time these holes are accumulated in the gate oxide and trapped as shown in Figure 1.2. The positive charge that builds up due to the holes trapped in the gate oxide has a similar effect as if a voltage is supplied on the gate of the PMOS and NMOS. This trapped positive charge in the gate oxide results in a permanently ON state in the NMOS and permanently OFF state in the PMOS. The gate of the transistors is becoming naturally radiation resistant as technology is advancing continuously and scaling down the sizes which in result causing the gate oxide to be thinner and less of a charge carrier. [3]

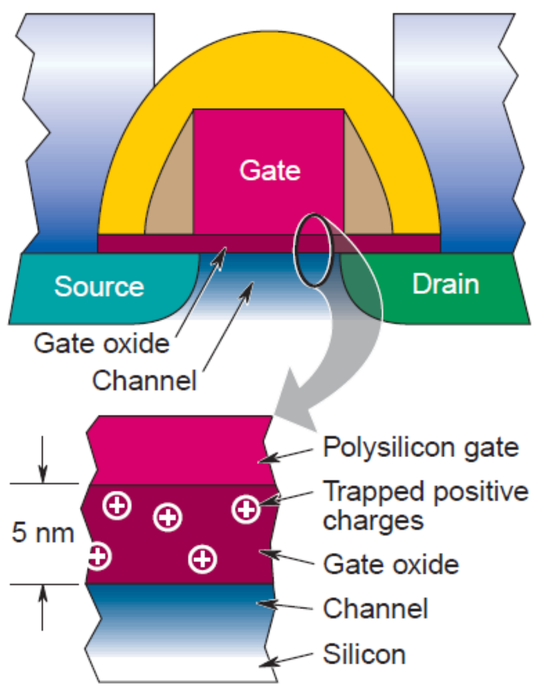


Figure 1.2: The cross section views of the NMOS transistor showing that in between drain and source there is a conducting channel and gate. The voltages that are trapped are responsible for voltage shift. [3]

1.2.2 Single Event Effects (SEE)

Single particles coming from the cosmic rays can pass in a straight line through a space craft and its inner elements. It is highly impractical to shield a satellite from these kinds of particles. When an energetic ion passes through a semiconductor, it leaves a column of ionized material. The column has an equal number of holes and electrons making it electrically neutral and creating a temporary “conducting wire”, as shown in Figure 1.3.

This disturbs current paths and electrical areas that are "normal." As the ion "track" dissipates by recombination, the outcome may be critical current flow or temporary "shorts" which can result in single event burnouts, upsets, latch-up, bit flips or other undesirable effects. As in TID the scaling affects the radiation resistance, but in SEE the scaling has a negative outcome as particles with less energy can induce single event effects on the electronics. [3]

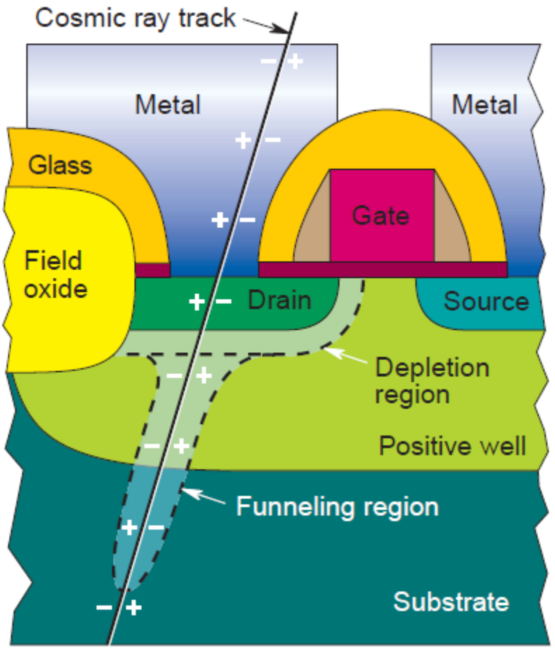


Figure 1.3: A cosmic ray's path through a NMOS transistor's drain. The charge released in the aftermath of the ion is gathered by the funnelling mechanism. A short between the substrate and the drain terminal is currently being developed. [3]

1.2.3 Displacement Damage (DD)

Displacement damage is mostly referred to as proton and neutron damage. When a highly energetic proton or neutron enters the crystal lattice of a semiconductor (silicon), those atoms are displaced in many ways. The disturbing neutron or proton transfers some

of its energy to the nucleus of silicon. If the transferred energy is enough it can knock the nucleus out from its position in the lattice. In elastic scattering, silicon atom released may lose energy by ionizing or displacing other atoms. In inelastic scattering, the nucleus struck absorbs the neutron or proton and then releases it at a lower energy level with a gamma ray. In both inelastic and elastic scattering there is displacement of silicon in the crystal lattice. Due to these displacements the crystal lattice has voids and clusters which can cause interference in the charge transfer mechanism of the crystals as shown in Figure 1.4. [3]

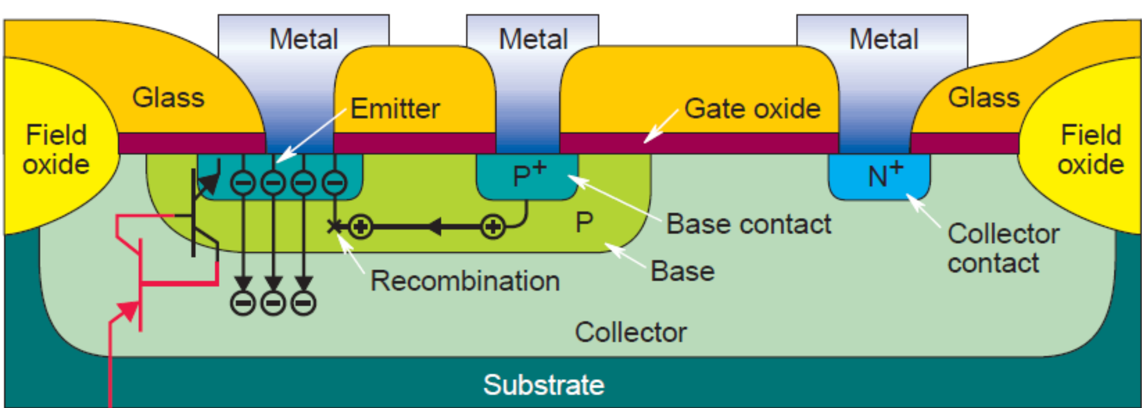


Figure 1.4: Bipolar junction transistor operation. At one end, electrons are emitted, diffused through the centre material (base), and finally gathered. If the transistor were ideal, all the electrons emitted would be gathered; however, some would be lost by recombining with the base holes. [3]

1.2.4 Fault Detection, Isolation and Recovery (FDIR)

When satellites are not directly communicating with a ground station, they require some autonomous operation to perform tasks. This requires a dependable design that can handle faults. The dependable system can be achieved as described in: [4]

- Fault tolerance is to provide the given service by redundancy despite any faults.
- Fault avoidance is to avoid the occurrence of a fault by design.
- Fault removal is to eliminate the existence of design flaws.
- Fault forecasting is to assess the existence, development and implications of mistakes by assessment.
- Faults due to errors: Errors can lead to mistakes.

1.3 Problem Statement

In remote sensing payloads the multiple image sensors with different spectral, spatial and radiometric resolutions collect a large amount of image data that has to be sent to the satellite in real time through a Camera Data and Control (CDC) Unit. These image sensors have multiple data ports and all these ports are processed simultaneously. In earlier mission a large number of cables and interface devices were required for the conventional parallel transmission, resulting in large weight, large volume and signal integrity issues. Therefore, data needs to be converted (serialized) and transmitted with minimal interfaces in order to reduce weight and volume. Although serialized data reduce the weight and cost in terms of launch load, the data rates are increased and the signal integrity, power integrity issues like crosstalk noise, reflection noise, power ground noise etc. are still in the system. Signal integrity and power integrity preservation methods and guidelines are used to overcome the aforementioned challenges of data transmission.

1.4 Objective

The primary objective of this thesis is to achieve a design in which the processing of the high-speed image data is not affected by the different types of noises.

The secondary objective is to learn some of the basic, methods, designing and analysis techniques for ensuring signal and power integrity and to apply them on the design under consideration.

1.5 Scope

The aim of this dissertation lies around the designing and analysis of high-speed electronics to process image data that are coming from the Image Detector Unit (IDU) to the Camera Data and Control (CDC) Unit and from the Camera Data and Control Unit to the satellite. The image data transmitted by the CDC Unit have to pass multiple units and each unit even, if it’s a single connector, affects this image data. The image data generated by the sensor in the IDU is provided to the IDU harness connector through a IDU printed circuit board (PCB) connector. The image data then has to reach the CDC harness connector through image sensor harness. The image data are then fed to the CDC input connector through the CDC harness connector, where they are fed to the FPGA.

Inside the FPGA the data is fed to the serializer block, where the number of data lines are reduced that helps in a lightweight harness with a smaller number of signals. These serialized signals are provided to the satellite through CDC output Connector, CDC harness connector and sensor control harness. The processing, controlling and handling of data is also performed inside FPGA.

The focus of the whole dissertation is around the most critical section in the whole chain which is the high-speed image data lines in parallel configuration received by the CDC from IDU and serialized high-speed image data lines transferred to the satellite also highlighted in the Figure 1.5. This dissertation focuses on the following sections of the design:

- Schematic, PCB design, signal integrity (SI) analysis and power integrity (PI) analysis from “CDC input connector to the FPGA”.
- Schematic, PCB design, signal integrity (SI) analysis and power integrity (PI) analysis from “FPGA to the CDC output connector”.

The other sections of the chain are not included in the scope of this thesis.

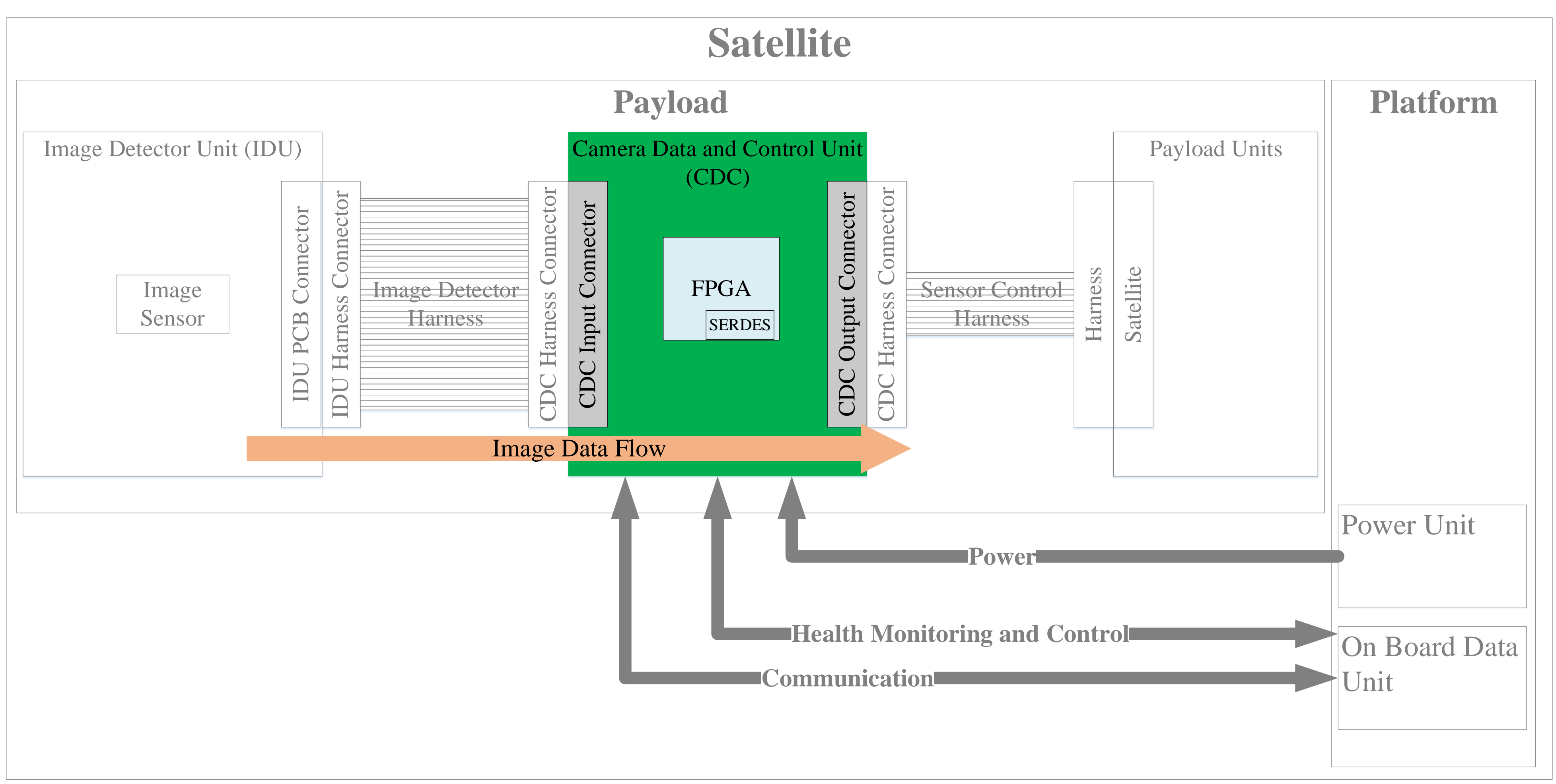


Figure 1.5: Different sections in the chain showing the path of Image Data Flow from IDU to Satellite.

1.6 Dissertation Outline

The 2nd chapter of the thesis deals with the review of the published designs for high-speed electronics for satellite imaging payloads. It also introduces the signal interface network, power delivery networks and some of the basics of transmission line theory.

The 3rd chapter describes the basic hardware requirements on which the whole design will be based. It also covers some of the budgets related to power and data.

The hardware architecture of the IDU design will be elaborated in the 4th chapter.

In chapter 5 the pre-layout design and analysis involving layer stackup and impedance planning pre-layout signal integrity analysis and pre-layout power integrity analysis is explained.

In chapter 6 the post-layout design and analysis involving board layout and planes post-layout signal integrity and post-layout power integrity is explained.

The last chapter will conclude the thesis with some recommendations for future work.

2 LITERATURE REVIEW

2.1 Introduction to Transmission Line Theory

A physical structure that can guide an electromagnetic signal from one place to another is called a "Transmission Line". [5] For a high-speed signal PCB traces are considered as transmission lines. In digital communication especially over long distance the popular configurations are twisted pair cables and coaxial cables with and without shielding. Most of the PCBs nowadays often use either stripline or microstrip traces. These are two parallel conductors with cross-sectional dimensions much smaller than their lengths. Some of the possible transmission structures are discussed below. Any structure can be used for high-speed signals if it is properly terminated. [5]

2.1.1 Trace

Traces are those conductors that are designed for low-frequency, traces can be either the external surface of a board or internal to the board, as shown in Figure 2.1. [6]

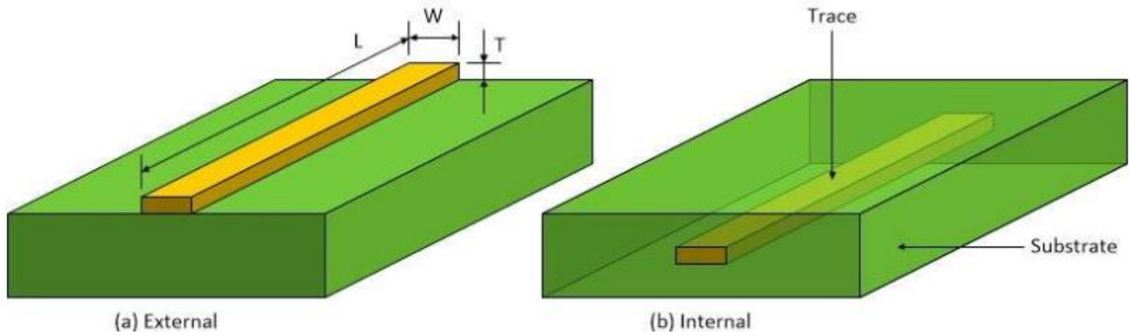


Figure 2.1: The trace is on the external side of the board. (b) The trace is inside the board. [6]

2.1.2 Microstrips

A microstrip is a type of trace created to enable it to behave like a transmission line. The microstrip structure has a trace, a ground plane and a dielectric layer, which separates the conductor from ground, as shown in Figure 2.2. [6]

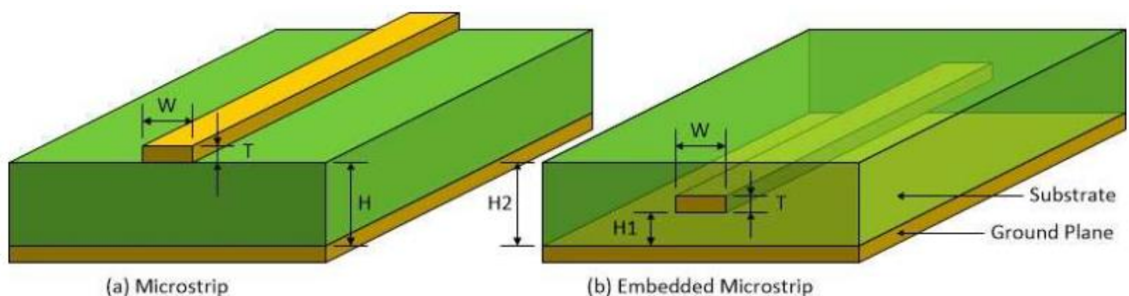


Figure 2.2: (a) The trace is on the external side of the board with ground plane and dielectric is separating them apart. (b) The trace is inside of the board. [6]

2.1.3 Striplines

The stripline has two ground planes and the trace is embedded in the dielectric surrounded by these two ground planes, as shown in Figure 2.3. [6]

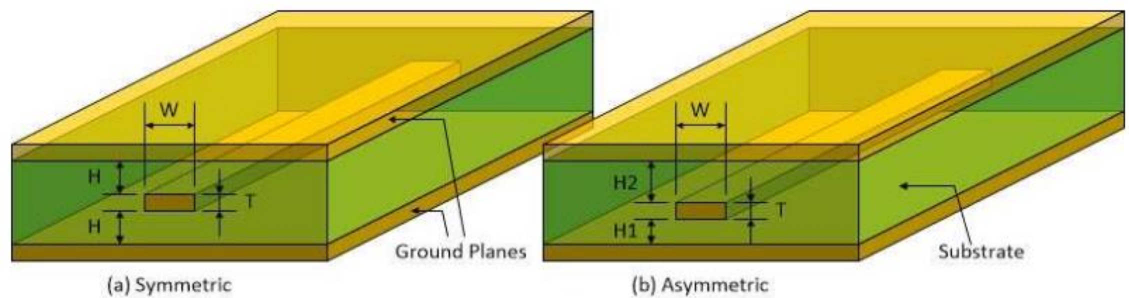


Figure 2.3: (a) The distance of the trace from both ground plane is equal. (b) The distance of the trace from both ground plane is not equal. [6]

2.1.4 Twisted Pair Cable

The twisted pair cable consists of two insulated wires, these wires are twisted around each other, as shown in Figure 2.4. The number of insulated pairs can be more than one. Twisted pair cables come in a shielded and unshielded variety. [7]

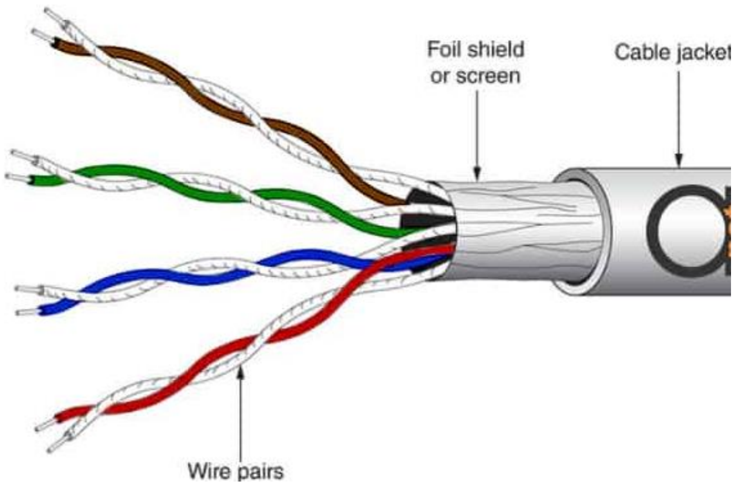


Figure 2.4: Twisted Pair Cable Composition. [8]

2.1.5 Coaxial Cable

Coaxial cables contain a single copper wire surrounded by a wire mesh or foil channel. The outer wire mesh or foil channel serves as a ground, as shown in Figure 2.5. Coaxial cable come in two types which are Thinnet and Thicknet. [7]

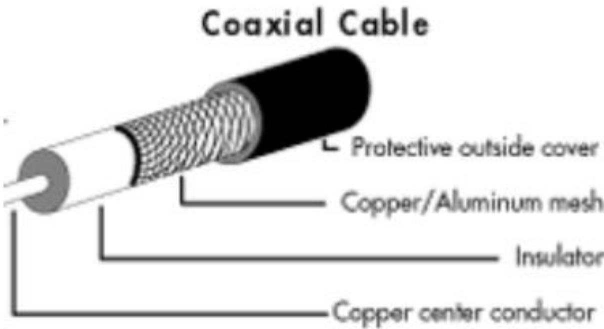


Figure 2.5: Coaxial Cable Composition. [7]

2.1.6 Telegrapher's Equation

The telegrapher's equations were developed in the 19th century to describe the performance of high-speed signals in long telegraph lines. If there is a uniform path for the signal and return flow and the signals are placed closely in contrast to the wavelength conveyed, then all the transmission structures discussed below have the same telegrapher's equations. The telegrapher's equation perfectly models the propagation of the voltages and currents of these structures. The telegrapher's equation can be applied to any transmission media that have following characteristics: [9]

- Minimum two conductors insulated from each other.
- For the full length the cross section of the structure is uniform.

- The wavelength of the signals transported is greater than the cross sectional of the structure.
- The length should be long comparing to the distance between the two conductors.

The transmission line is generally considered as either lossless or lossy.

- In a lossless transmission line, the effect of resistance “R” and shunt conductance “G” is neglected, and the transmission line is considered as an ideal lossless line. [9]

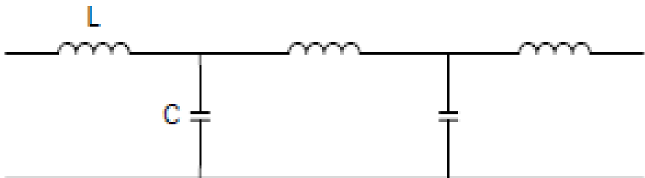


Figure 2.6: The absence of R and G shows and ideal lossless transmission line.

The telegrapher’s basic equations for lossless transmission are:

$$\frac{\partial V}{\partial x} = -L\frac{\partial I}{\partial t} \quad 2.1\ [9]$$

$$\frac{\partial I}{\partial x} = -C\frac{\partial V}{\partial t} \quad 2.2\ [9]$$

where

I is current

V is voltage

C is capacitance

Lis inductance

- In a lossy transmission line, the effect of resistance “R” and shunt conductance “G” is not negligible, [9]

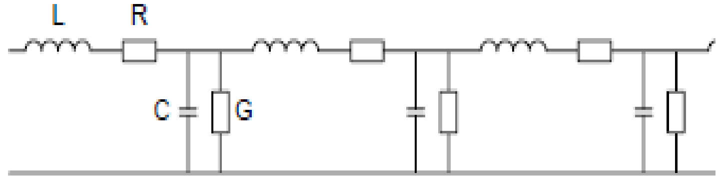


Figure 2.7: The presence of R and G showing the lossy transmission line.

The telegrapher's basic equation for lossy transmission are:

$$\frac{\partial}{\partial x}V(x,t) = -L\frac{\partial}{\partial t}I(x,t) - RI(x,t) \quad 2.3\ [9]$$

$$\frac{\partial}{\partial x}I(x,t) = -C\frac{\partial}{\partial t}V(x,t) - GV(x,t) \quad 2.4\ [9]$$

where

I is current

V is voltage

C is capacitance

Lis inductance

R is resistance

G is conductance

The complete derivation of the telegrapher's equation is given in section 2.2 of [9].

2.1.6.1 Skin effect

The flow of current through a conductor at high-speed is not uniform over the whole cross section. The current starts to flow over the surface. This phenomenon is called the skin effect. When the current flows on the surface of the conductor, the conductor's parasitic resistance is increasing. Due to the high-frequency, the currents flow on the outer layers and the conductor seems to be hollow. [9]

2.1.6.2 DC Resistance

Due to series resistance in a transmission line a some of the signal power is dissipated, causing distortion and attenuation in the signals. [9] The DC resistance is given by:

$$R_{DC} = \frac{k_a \rho}{a} \qquad 2.5\ [9]$$

where

R_{DC} is DC Resistance

k_a is correction factor for the return path DC resistance

a is conductor cross sectional area

ρ is conductor resistivity

2.1.6.3 DC Conductance

Humid or wet conditions or incorrect insulation in between the conductors in long cables creates a shunt conductance "G" per-unit-length of the conductor. Similar to the DC resistance, the DC conductance causes the problem of power dissipation, distortion and attenuation. [9]

In high-frequency the current in a round conductor mostly flows in a nonuniform way on the surface of the wire. Due to this nonuniformity the magnetic field in the conductor and its associated return path distribute in a slightly nonuniform way that in return increases the apparent resistance of the conductors. In parallel conductors this apparent increase in the resistance is called the proximity effect. [9]

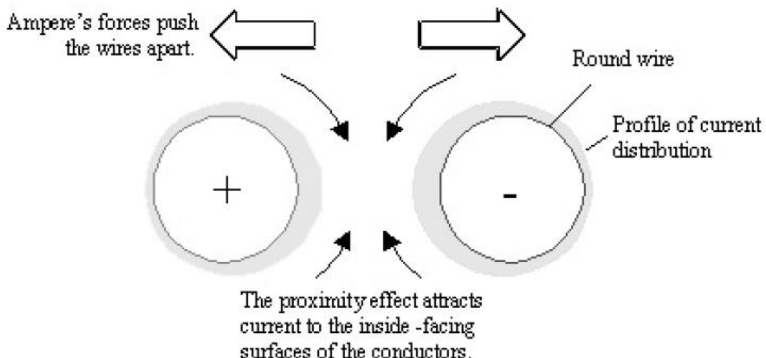
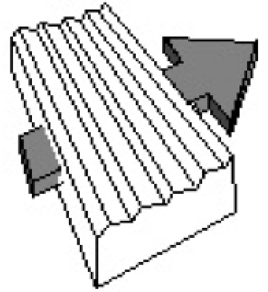


Figure 2.8: Redistribution of the current around the surface of conductor due to Proximity effect. [9]

2.1.6.4 Surface Roughness

Not all surfaces appear completely smooth on a microscopic scale. There are ground irregularities and bumps in all products. The root mean square (RMS) height h_{RMS} is the measure of surface roughness. At low frequencies the penetration depth of current

surpasses h_{RMS}. Therefore, the current flows under the surface bumps and is unaffected by the roughness. [9] At high-frequency the current remains at the surface all the times. As the frequencies are further increased, the skin depths shrink to less than the h_{RMS} and as the current flows in the conductor it follows the contours of the surface. At these frequencies the apparent resistance increases and affects the current passing through the contours of the conductor, as shown in Figure 2.9. [9]



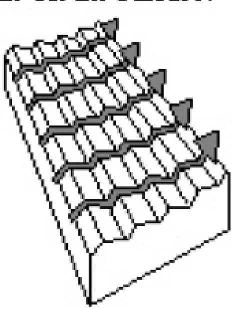


Figure 2.9: The apparent resistance increases with the surface roughness. [9]

2.1.6.5 Dielectric Effect

The amount of electromagnetic incident power converted into heat by a dielectric material is called the dielectric loss. Using insulating material as part of a transmission line causes attenuation of a signal due to dielectric loss. The higher the dielectric loss, the higher the loss in the signals. [9]

2.1.6.6 Characteristic Impedance

As the frequency increases the flow of energy is blocked by the reactance of parasitic inductance. Similarly, with increase in frequency the flow of energy is shunted in the return plane by the reactance of parasitic capacitance. Due to these elements on all frequencies of an electromagnetic field a constant impedance is seen. [9]

$$\boldsymbol{Z_0} = \frac{\boldsymbol{R_0} + \mathbf{j\Omega}\, \boldsymbol{L_0}}{\boldsymbol{G_0} + \mathbf{j\Omega}\, \boldsymbol{C_0}} \qquad 2.6\ [9]$$

where

Z_0 is impedance

L_0 is parasitic inductance

C_0 is parasitic capacitance

R_0 is parasitic resistance

G_0 is trans-conductance

The impedance of a transmission line is not a function of its length if the cross section remains same. The impedance is constant if the dielectric constant is fixed with the frequency.

2.2 Introduction to Signal Integrity

Signal integrity is the study of analogue effects in digital systems. Signal integrity problems occur when the interconnects in an electronic system are no longer electrically transparent. SI has two components that are interlinked; voltage accuracy of the waveform and timing of arrival of switching edges at the input.

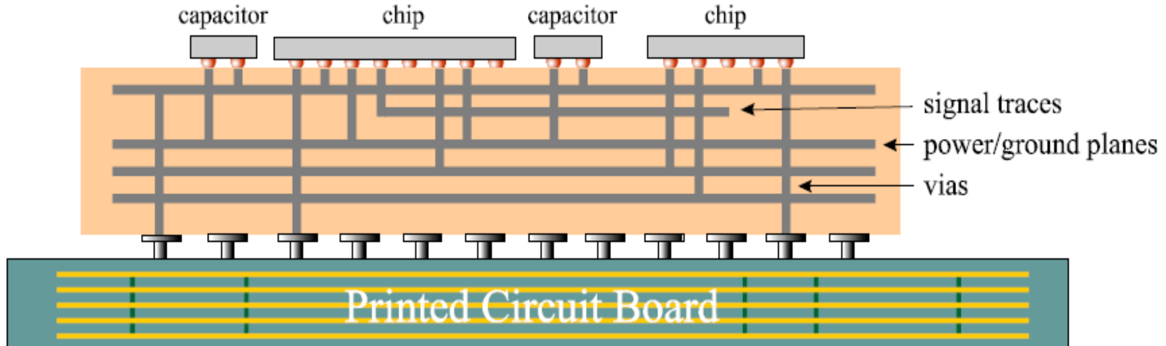


Figure 2.10: Signal integrity challenges in PCB and components. [10]

The waveform voltage accuracy is to maintain the timing and quality of the signal. The waveform voltage accuracy is affected by:

- Impedance matching
- Ground bounce
- Coupling

The timing of the arrival of switching edges is to ensure reliable high-speed data transmission. The timing is affected by

- Propagation delay variations in components
- Travel time on wires

- Variation in edge rates of components

2.2.1 Signal Interface Network

In a high-speed system the signal timing plays a major role, the timing depends on two main elements, i.e. delay due to the physical distance that signal propagates and the shape of the signal when the threshold is reached. The distortion in the signal can be caused by different mechanisms such as:

- Reflections
- Crosstalk
- Power/Ground Noise

2.2.1.1 Reflections

A high-speed signal propagates with little or no loss along the uniform cross section of the transmission line. The change in the impedance of the transmission line causes some of the electromagnetic field to be reflected back toward the source. The electromagnetic field that continues is moderated by the quantity of the energy reflected. Reflection mostly occurs due to impedance mismatching between the transmitter and receiver of the transmission line. [10]

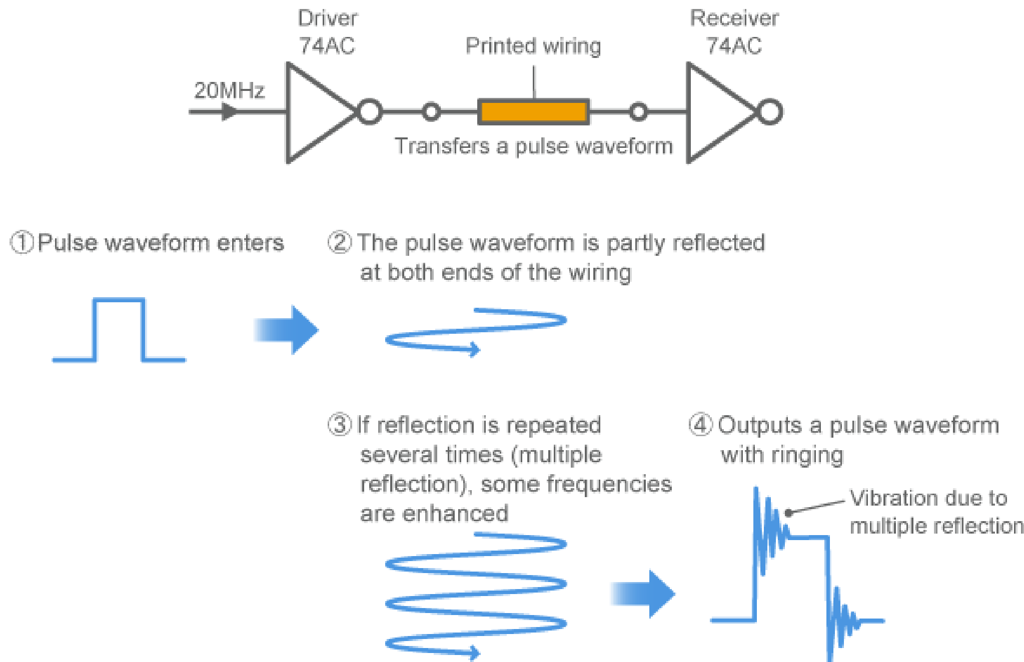


Figure 2.11: In top section of figure a driver and receiver with a wire connected them together is shown, if a pulse is applied to the driver due to impedance mismatching or impurities in wire the pulse is reflected back causing reflection or ringing in the line. [11]

If a transmission line has multiple reflections than this problem is said to be ringing. Overshoots are reflections added to the incident voltage. Undershoots are reflections subtracted from the incident voltage. Reflections can be prevented in the following ways: [10]

- Elimination of Stubs
- Controlling trace impedance
- Selection of a proper termination scheme
- Use of a metal plane for the return path

2.2.1.2 Crosstalk Noise

Crosstalk is an electromagnetic field's unwanted interaction of a line with an adjoining transmission line. The adjoining transmission line may be in the same layer or in different layer. This undesirable connection takes a form of energy dissipated into the adjacent line as a disruptive signal of noise. [5]

Electromagnetic fields have two types of energy components, magnetic and electric. When the stray capacitance between two conductors is greater than the stray inductance between these two transmission lines then the electric field is dominating. When the stray inductance between two conductors is greater than the stray capacitance between these two transmission lines then the magnetic field is dominating. In the electric field the traces run over the top of each other in the neighbouring PCB layers, while in the magnetic field the traces run side by side in the same PCB layer as shown in Figure 2.12. [12]

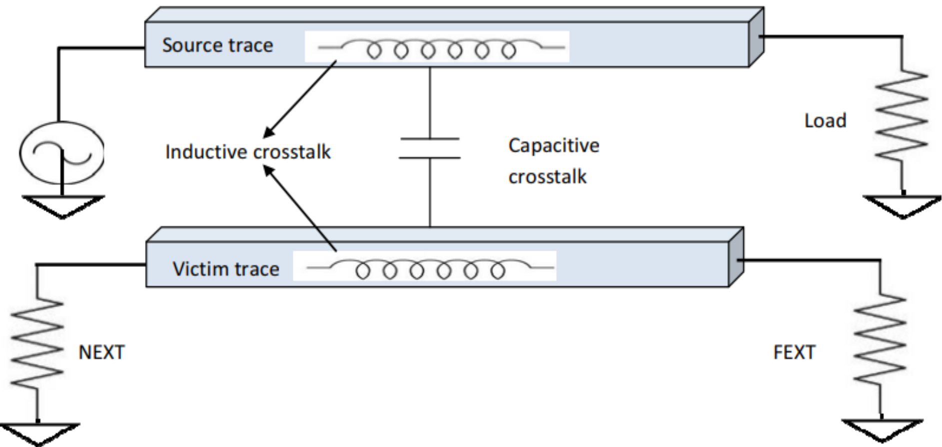


Figure 2.12: Both the inductive crosstalk and capacitive crosstalk between source and victim. [12]

2.2.1.3 Power/G Ground Noise

In today's high-speed systems, the power/ground noise contributes more than 30% of the noise budget. The simultaneous switching noise (SSN) is caused by transient currents drawn by simultaneous switching of ICs and the voltage variation between power and ground lines. The SSN can reduce the speed of the signals and cause logic errors due to imperfect return path.

2.3 Introduction to Power Integrity

Analysis of Power Integrity (PI) is a key component of contemporary electronic design. In relation to drastic rises in power consumption, the ever-increasing amount of voltages used by ICs makes power distribution an extremely challenging task. These problems are amplified by decreased layer counts, lower noise margins and increased operating frequencies. Insufficient power the design can lead to errors in signal integrity, and these errors can cause the logic failure. [13]

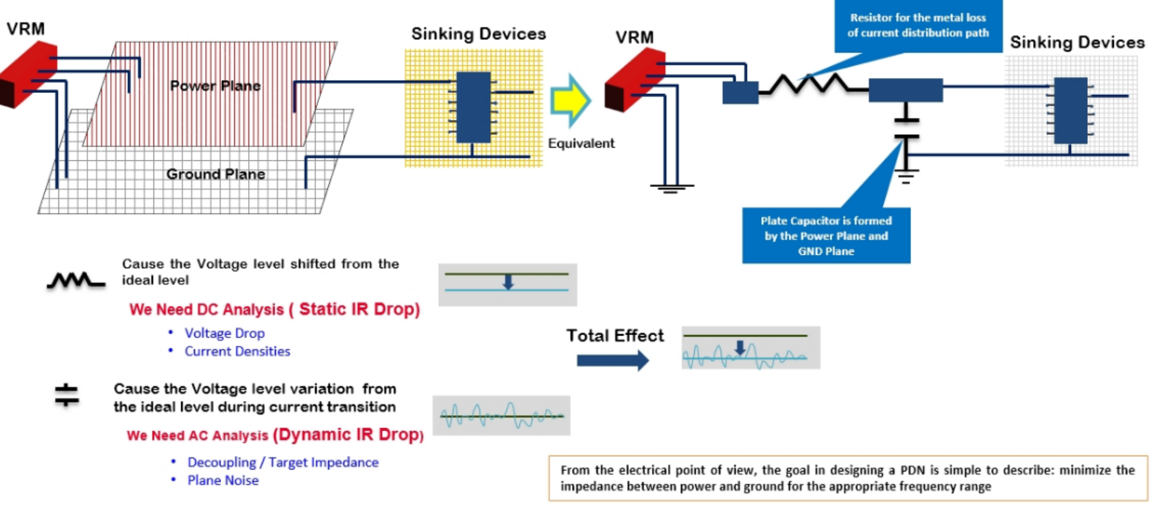


Figure 2.13: The top part of is showing the equivalent network of a PDN having VRM, Power and Ground Plane and Sinking devices. The bottom section shows the effect of DC, AC analysis. [13]

2.3.1 Power Delivery Network

The primary objective of power integrity analysis is to work out the power delivery network (PDN) impedance of a complete system, voltage variations and current waveform of the rails. A full power integrity analysis must consider that the energy is distributed over all the planes, which is difficult to analyse. [14]

2.3.1.1 AC Simulation (Decoupling Analysis)

In decoupling analysis, the impedance response of the PDN is analyzed and improved. In a PCB the target impedances of all the power planes are calculated considering the plane current and plane voltage requirement. [14]

2.3.1.2 DC Simulation (DC-Drop Analysis)

The main objective of DC drop analysis is to compute the IR drop (voltage drop), current and power loss density in power lines. The DC drop analysis identifies the current drawn by an IC, IC pins, connector pins, vias in DC operating conditions. A power drop below the threshold limits of ICs causes malfunctions. Excessive current density passing through vias and planes generates excessive heat. [14]

2.4 Literature Review of Published Designs for High-Speed Electronics for Small Satellite Payloads

2.4.1 High-speed Camera Electronics for Microsatellites [1]

In very high-resolution imaging satellites, due to the high ground sampling rate, the imaging sensor (CCD / CMOS) must be operated at a very high-speed. Time delay & integration (TDI) is preferred for ongoing imaging to get better SNR & dynamic variety at high resolution. TDI operation is a method to increase the effective integration time to collect more incident light by accumulating multiple exposures of the synchronized (moving) object.

Many bias lines and clocks are required by the detector. Due to large swath requirements, the number of output video ports is also large. The main role of camera electronics is to produce stimulus such as clocks and bias to process sensor output information into digital format for the detector. Camera electronics involve faster clock rates and larger bandwidth due to high-speed operation of the detector. Inter-clock stage relationships are very essential with the necessary rise / fall time of these clocks. Some clocks involve a rise/fall time of < 7 ns with a duty cycle of approximately 20%. Therefore, the primary challenge is to preserve signal integrity of video signals and clocks signal with reduced noise. [1]

This leads to the need to place camera electronics close the focal plane detector to provide adequate noise-free bias, receive settled video and detector control signals. Due

to space constraints on the focal plane the electronics in the focal plane need to be miniaturized so that it dissipates less power and does not impose any strict requirement in maintaining the ambient temperature for better performance of detector. [1]

2.4.2 High-speed Electronics Design for TDI Detector [15]

At high spatial frequencies in high-resolution imaging the MTF performance is low. The radiometric efficiency must therefore be sufficiently large for object identification and recognition. Signal energy gathered by the sensor and multiple types of noise dominate the radiometric output. Improving the radiometry is improved with methods such as time delay and integration (TDI) and step and stare. Previous Indian high-resolution missions such as Cartosat-2 used a linear CCD sensor and step and stare methods to improve SNR. The step and stare technique is used to build a high-resolution image of large area from smaller images (mosaic) taken from different locations and orientations . [15]

The design of these sensors is different from a linear CCD sensor. A TDI sensor has a greater number of bias and clock lines and a high-speed of synchronization and operation. [15]

2.4.3 Implementation of a FPGA-based Interface to a High-Speed Image Sensor [16]

Grob [16] describes a FPGA interface to a LUPA-3000 imaging sensor. The FPGA receives the LVDS data signals and synchronizes them for further processing. The data signals designed is discussed and its functionality is explained. A VHDL design is also developed for a LVDS transmitter and it transfers the data to a receiver which interconnects with FPGA IOs. A SystemC test bench was created to assess the hardware design linked to the image sensor, which contains the LUPA-3000 image sensor software system to check the general layout features. [16]

3 Basic Hardware Requirements

3.1 Design Requirements

In this Chapter, the top-level requirements for high-speed design of the Camera Data and Control (CDC) Unit are defined. These requirements provide guidance for the designs to be further developed in Chapter 4 and serve as a check list for design.

3.2 Preliminary Requirement definitions

The top-level requirements define the set of essential characteristics that the design of the CDC Unit must have to fulfil the subsystem level requirements. The top-level design requirements for CDC that are derived from the subsystem requirements are:

1. The CDC controller shall receive image data at approximately 250MHz, nominally, employing DDR, per LVDS pair.
2. The CDC controller shall receive 16 LVDS data pairs, consecutively, at the specified rate.
3. The payload data interface shall use low-voltage differential signals (LVDS) compliant to the EIA-644 standard.
4. The Payload Data Interface (PDI) shall pass the data and clock signals from the CDC Unit to other payload units.
5. The CDC controller shall transmit image data at 1GHz, nominally, employing DDR, per LVDS pair.
6. The CDC controller shall be capable of handling a 0.55meter GSD data.

These requirements provide the design envelope for the electronics hardware design of the CDC controller and the design level specifications are presented in the next section.

3.3 Design Requirements Specifications

Focusing on to the scope of the work, from the requirements stated above the essential set of CDC controller specifications are derived as presented below. High data rates (input and output) combined with performance and physical size constraints makes the design of the CDC Unit more complex. To address these requirements and to maintain the signal and power integrity of the design, the following specifications will be used throughout the design process.

1. The CDC Unit PCB shall have an impedance of 50Ω per single ended line and 100Ω per LVDS pair, as per EIA-644 standard.
2. The CDC Unit shall have a maximum power consumption of 6W.
3. All the high-speed digital traces shall be coupled tightly to a contiguous reference plane with a minimum loop inductance current path.
4. The design shall be optimized with the power distribution network.
5. The voltages supplied by each power supply shall not vary by more than 5% of the nominal specified supply voltage, under load conditions.
6. The design shall meet the timing requirements for all the signals.
7. The design shall eliminate the crosstalk for trace-to-trace and on the same layer or broadside coupled by traces on the adjacent layers.
8. The post-layout analysis of the design shall provide the design validation and verification to ensure that all the constraints are met.

To achieve a design that fulfils the above-mentioned requirements requires adhering to a high-speed PCB design approach. This is based on the development of a design hierarchy that illustrates to the most critical considerations of the design to identify the potential areas of the design where signal integrity or power integrity problems can occur. With good design choices and approach, knowledge of the subject and using the simulation results, a practical design can be achieved that fulfils the design requirements. [16]

4 DESIGN DESCRIPTION

4.1 Camera Data and Control (CDC) Unit Hardware Architecture

The Camera Data and Control Unit performs the operation of the image sensor control and image data handling. The CDC Unit receives the image data from the sensor and sends it to the satellite after performing processing and control operations. The CDC Unit receives the data from a single sensor in the current configuration. The CDC Unit performs power regulation, controlling, monitoring and communication with the IDU. The CDC Unit also monitors the device's health and executes housekeeping tasks. The CDC controller communicates with the other payload units on a communication interface. The CDC Unit converts the primary power coming from the power unit into secondary power that is further down converted and supplied to the IDU and CDC FPGA and supporting circuits. The top-level hardware architecture of the CDC Unit is shown in Figure 4.1. The details of these blocks and their functions are described in the later sections of this chapter.

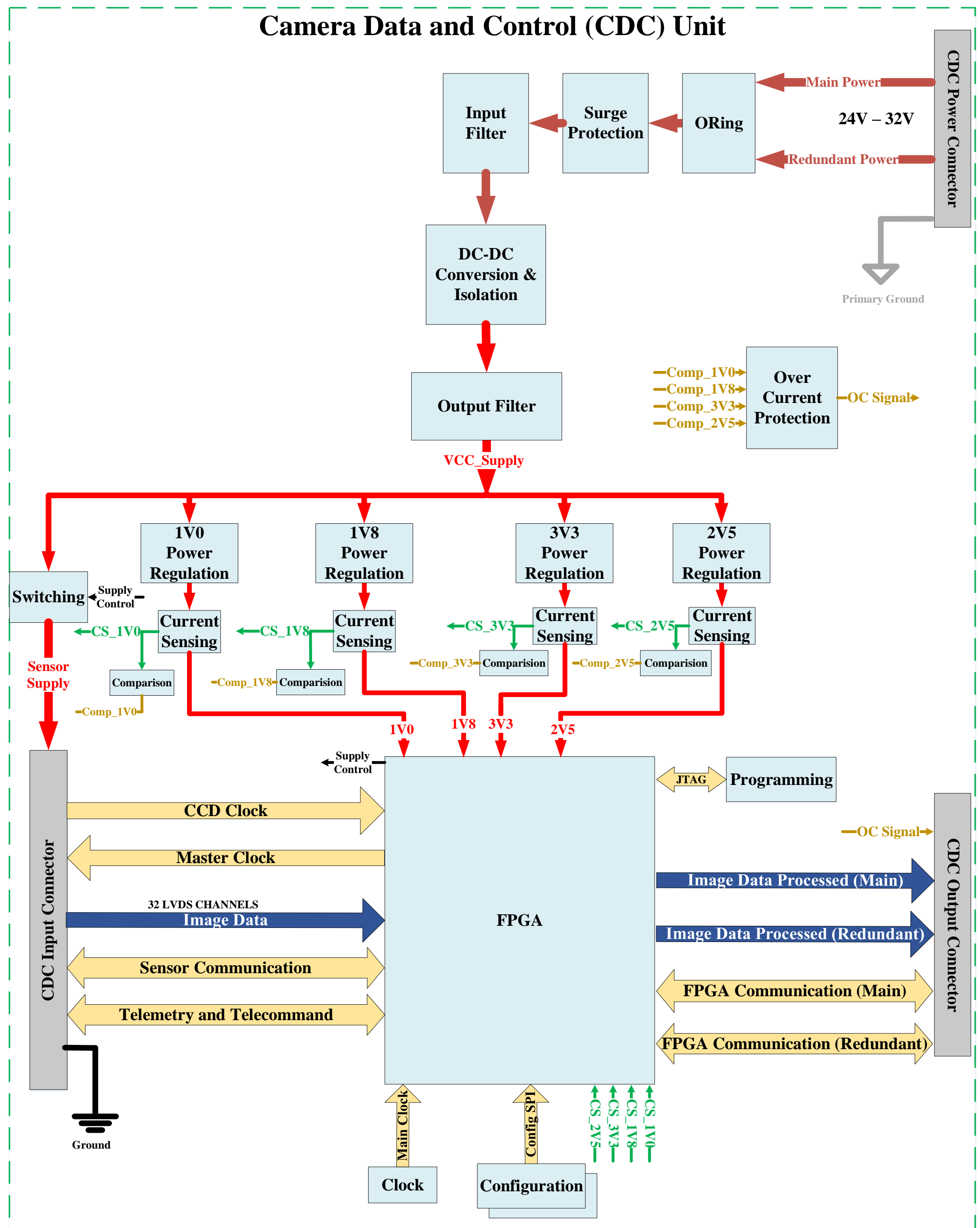


Figure 4.1: Hardware Architecture of Camera Data and Control (CDC) Unit.

4.1.1 Main and Redundant Power Line

The CDC Unit receives an unregulated voltage line ranging from 24Volt to 32Volt from the satellite main power units through the CDC Unit power interface. The CDC Unit receives two power lines, one main and one redundant. The purpose of these two power lines is to avoid single point failure so that in case if one line fails it should not affect

the operation of the CDC Unit. The selection between the main and redundant power lines is done through an OR function. The power line is supplied with a primary ground. The primary power is converted into a down converted secondary power through DC-DC converters. DC-DC converters isolate the secondary power line from the primary power lines as shown in Figure 4.2.

Input surge protection is employed prior to the input filter at the main line. The first function of the input surge protector is to ensure that the CDC Unit starts up without excessive instantaneous inrush current requirements. The second function of the input surge protector is a hold-off, to ensure that the DC-DC conversion is disabled until the input power supply has reached within the threshold level before further down conversion. After surge protection there are choke and EMI filters at the input of the DC-DC converters and their main functions are to reduce the AC ripples and the effect of high-frequency electrical noises respectively. Similarly, at the output of the DC-DC converter there are decoupling capacitors and their main function is to shunt the noise caused by the other circuit elements.

The secondary down converted power line is provided to the CDC Unit and IDU, the power provided to the IDU is controlled by the CDC Unit through switches.

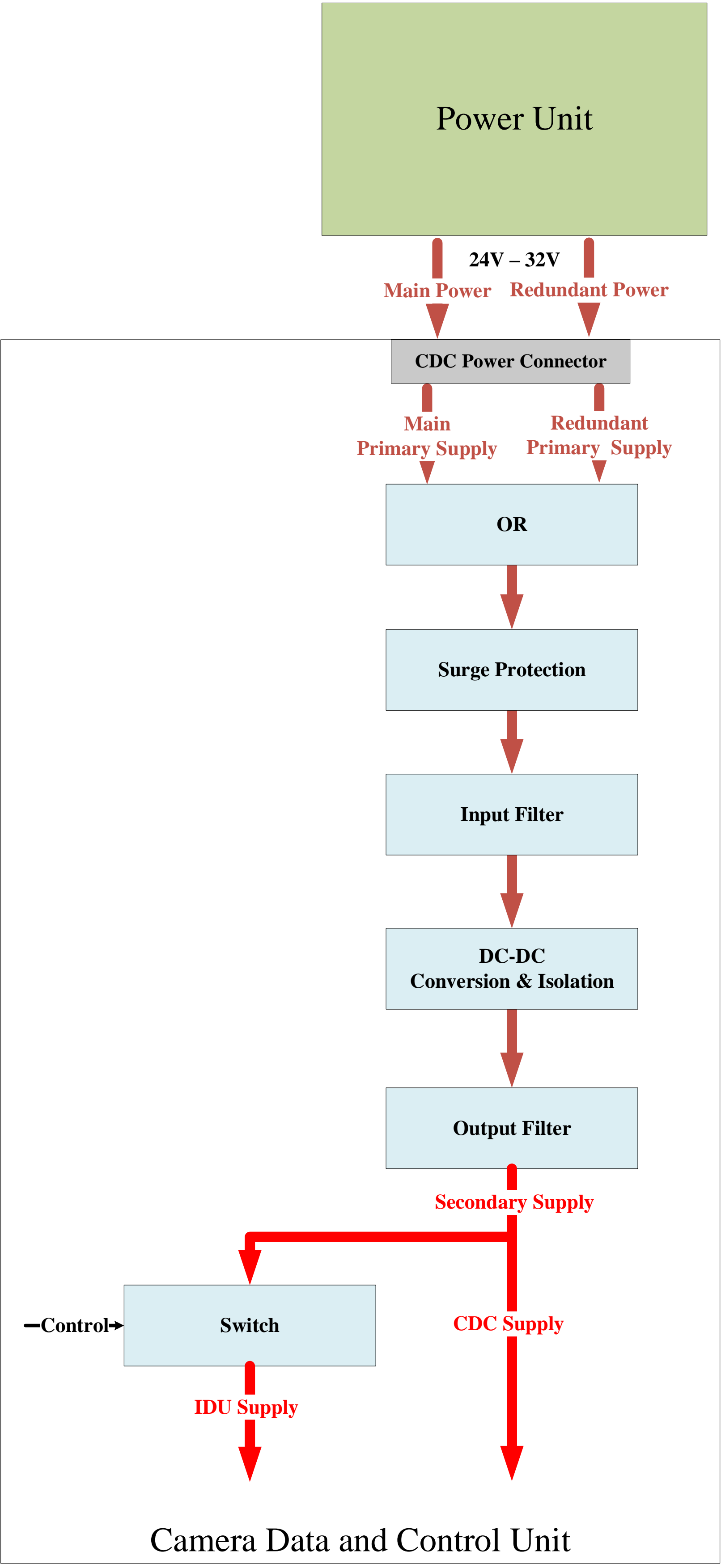


Figure 4.2: Power Flow from the Power Unit to CDC Unit, the power flow is shown from the power conversion of primary to secondary till output filter.

4.1.2 CDC Unit Power Sequencing

The secondary supply is converted into four different voltages through power regulation supplies. The power regulation supplies are used to power the FPGA, LVDS buffers, current sensors, comparators, configuration flashes, over current protection and all the supporting electronics required by CDC.

For the correct start-up of the FPGA banks, to achieve minimum current draw and ensure the input output signals are 3-stated during power ON, the power lines are supplied in a sequenced manner as shown in Figure 4.2. The power regulation lines are gradually started to avoid the excessive surge currents.

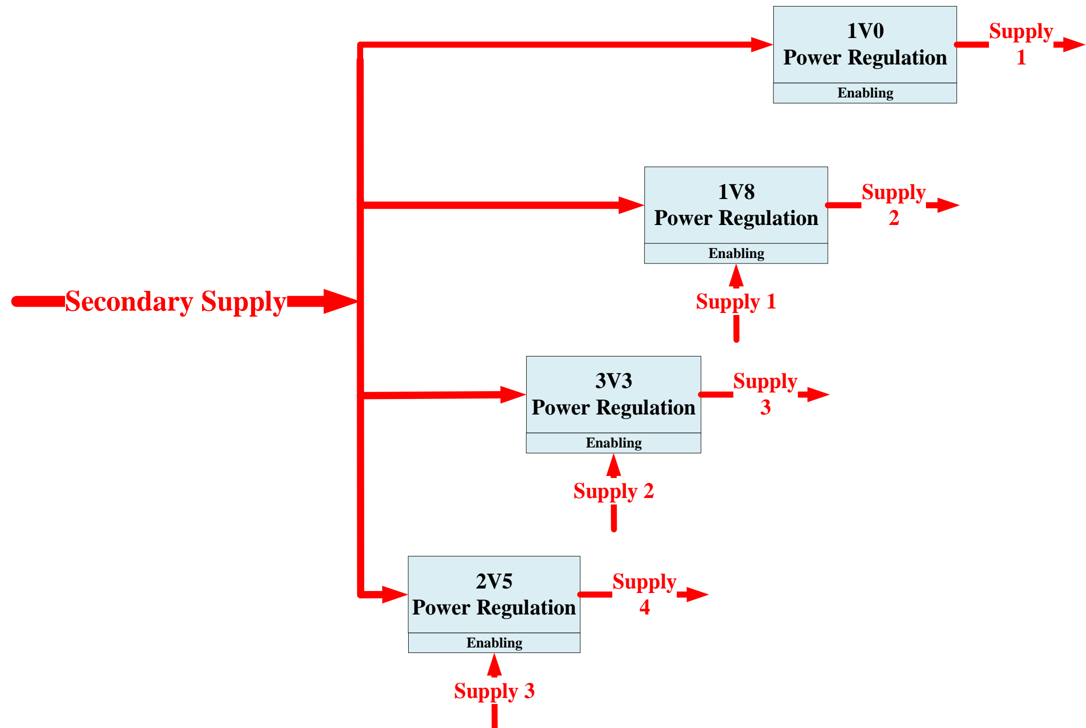


Figure 4.3: Power Sequencing of Supplies for CDC.

For power sequencing the secondary supply is supplied to the first power regulation circuit where the power regulation generates the 1V0 (Supply 1).

The 1V0 controls the enable the line of the second power regulation and forces it to remain disable until the 1V0 has reached the threshold value. At that moment when the 1V0 is within range then the second power regulation is enabled, and it converts the secondary supply into 1V8 (Supply 2).

The 1V8 controls the enable line of the third power regulation and forces it to remain disabled until the 1V8 has reached the threshold value. At that moment when the 1V8 is

within range then the third power regulation is enabled, and it converts the secondary supply into 3V3 (Supply 3).

The 3V3 controls the enable line of the fourth power regulation and forces it to remain disabled until the 3V3 has reached the threshold value. At that moment when the 3V3 is within range then the fourth power regulation is enabled, and it converts the secondary supply into 2V5 (Supply 4) as shown in Table 4.1.

The 2V5 controls the initialization signal of the FPGA and forces it to remain disabled until the 2V5 has reached the threshold value. Once the power sequencing is performed and all the voltages are within range then the FPGA is initialized, and it start working.

Table 4.1: Power ON Sequence Symbols and Details. [17]

Power ON Sequence	**Supply**	**Symbol**	**Detail**
1	1V0	VCCINT	Internal Supply Voltage
2	1V8	VCCAUX	Auxiliary Supply Voltage
3	3V3	GP I/O Banks Supply	General Purpose I/O Banks Supply Voltage
4	2V5	LVDS Banks Supply	LVDS Banks Supply Voltage

The power OFF sequence of FPGA is the reverse of the power ON sequence as shown in Table 4.2. [17]

Table 4.2: Power OFF Sequence Symbols and Details. [17]

Power OFF Sequence	**Supply**	**Symbol**	**Detail**
1	2V5	LVDS Banks Supply	LVDS Banks Supply Voltage
2	3V3	GP I/O Banks Supply	General Purpose I/O Banks Supply Voltage
3	1V8	VCCAUX	Auxiliary Supply Voltage
4	1V0	VCCINT	Internal Supply Voltage
To maintain the device reliability levels the voltage difference between GP I/O banks supply and VCCAUX must not exceed 2.625V. [17]			

4.1.3 CDC Configuration and Clock

The CDC configuration is stored in the Programmable Read Only Memory (PROM). When the FPGA is initialized it starts the routine and a communication link is established between the PROM and the FPGA, and the FPGA is then configured. There are two PROMs the in CDC Unit working as main and redundant. They can be switched using a switching signal coming from the payload units in case one fails as is shown in Figure 4.4.

An external oscillator provides the main clock to the FGPA. The clock provides an operating frequency to different modules.

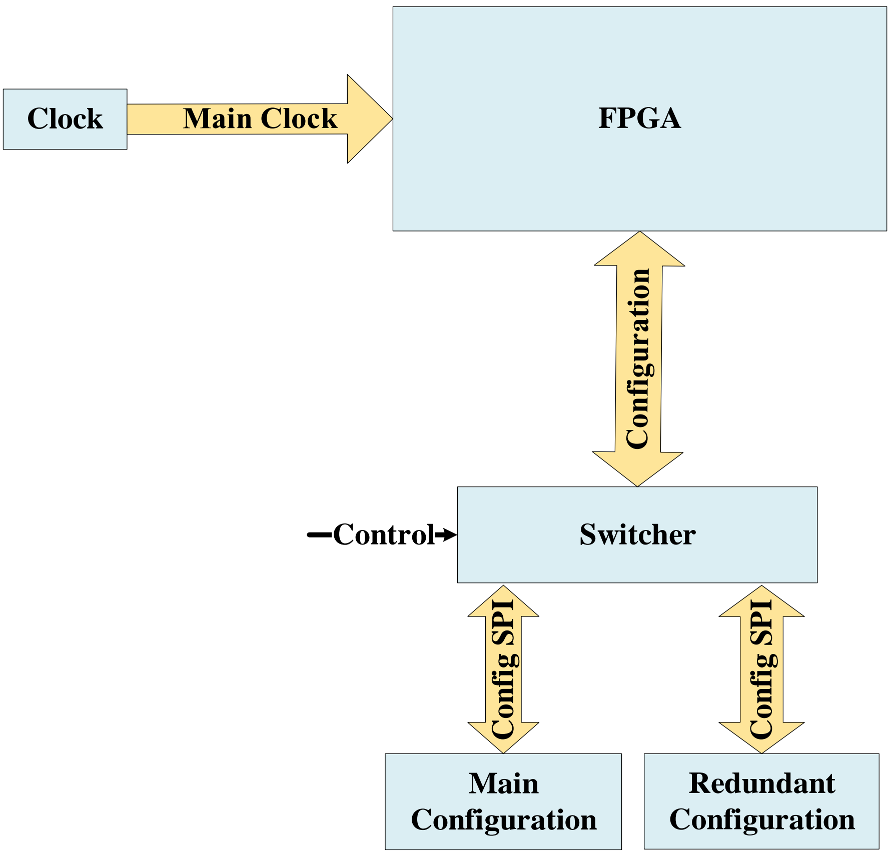


Figure 4.4: Selection between Main and Redundant FPGA Configuration.

4.1.4 Health Monitoring and Over-Current Protection

In the CDC two methodologies are used for health monitoring. These are periodic voltage and current monitoring of the power supply lines and detecting any over-current events of the power lines. The current of each power supply line is monitored through current sensors in the series of the power supply output lines. The current sensor converts the input signal into a readable output voltage which is provided to the analogue-to-

digital convertor (ADC). The ADC reads each telemetry. The periodic voltage monitoring is achieved by feeding the voltage of a power line directly to the ADC.

The over-current detection is achieved by comparing the current measurement of a power supply line with a predefined reference value that is within allowable limits. Similarly, for all the power lines the current measurement is provided to the respective comparators. The outputs of all the comparators are ANDED through an over-current protection circuit. In case of error in any of the power lines an OC signal is generated and provided to the Power Unit (PWU) and On Board Data Unit (OBD), as shown in Figure 4.5. In case of a false signal generated the OC can be overridden by the OBD.

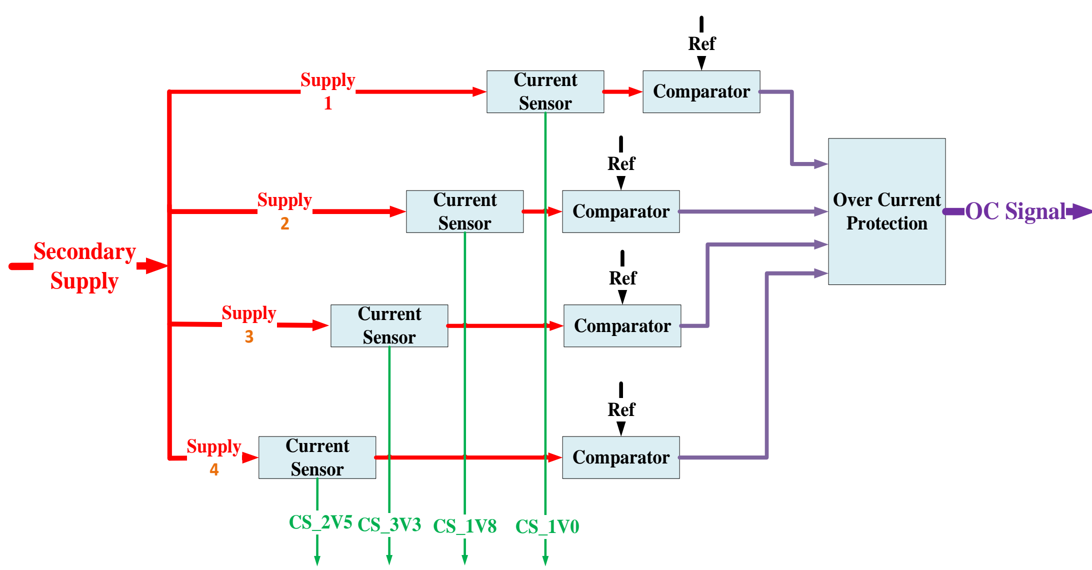


Figure 4.5: Telemetry of each power lines and over current protection signal for the instantaneous reaction in case if there is a problem in the power line current.

4.1.5 IDU Sensor

The image sensor sends 16 LVDS pairs data with clock to the CDC FPGA. The purpose of the clock is to shift charge inside the sensor. A master clock is supplied to the sensor from the FPGA which is required by the senor for its operation. The image sensor has a communication interface with the CDC for the configuration of the sensor. The IDU has a telemetry and telecommand (TMTC) interface with the CDC Unit. On TMTC interface the IDU provide its telemetries for health keeping and provide telecommands to the sensor and its supporting electronics. The characteristics of the IDU sensor are shown in the Table 4.3.

Table 4.3: Characteristics of IDU Sensor.

Characteristics	**Value**
Pixel Pitch	6.4 µm
Active Pixels	5120 x 3840
Frame Rate	30 frames/sec
ADC	12 bits
Output Data Channel (LVDS)	16
LVDS Output Data Rate	480 Mbit/s
Full Well Charge	15 Ke-
Power consumption	1100 mW
Communication Interface	SPI
Master Clock (CLK_IN)	40 MHz
Sensor Type	Area Scan Sensor

The rate at which the data is transferred to the CDC Unit using a single sensor with 5 bands is mentioned in the Table 4.4. All the parameters mentioned in the table are used in the data rate calculation. The data for each differential pair is approximately 250Mbps.

Table 4.4: Data Rate Calculation for the Image Data Supplied to the CDC from IDU.

Number of Sensor	1
Spectral Bands	5
Number of Pixels/Row	5120
ADC Output (bits)	12
Ground Track Velocity (m/sec)	6,908
GSD (m)	0.55
Integration Time (sec)	7.96E-05
Total Data/Integration Time	61440
Number of Output Channel	16
Total Data Rate (Gbps)	3.86
Data Rate/Channel (Mbps)	242 (approximately 250Mbps)

4.1.6 FPGA to Payload Interface

The main function of the CDC FPGA is to provide control and data handling of the image sensor data. The FPGA performs multiple subfunctions like reordering, binning and tagging on the image data. An internal serializer is used to reduce the number of lines. The image data is then transmitted to the Payload Unit through the main and redundant interfaces. The CDC Unit has a main and redundant communication interface with the OBC which is used to transfer telemetry and receive telecommands, sensor configuration parameters transmission and reception of time signals for synchronization. The parameters for calculating the data rate at which the data is transferred to the Payload Unit are listed in Table 4.5.

Table 4.5: Data Rate Calculation for the Image Data Supplied to the Payload Unit from CDC.

Number of Sensor	1
Spectral Bands	5
Number of Pixels/Row	5120
ADC Output (bits)	12
Ground Track Velocity (m/sec)	6,908
GSD (m)	0.55
Integration Time (sec)	7.96E-05
Total Data/Integration Time	61440
Number of Output Channel	4
Total Data Rate (Gbps)	3.86
Data Rate/Channel (Mbps)	965 (approximately 1Gbps)

4.1.7 FPGA Resource Utilization (Estimate)

The FPGA selection is based on resource utilization. An initial estimate can be driven based on all the functions performed by the FPGA. The FPGA resource utilization is shown in Table 4.6.

Table 4.6: FPGA Resource Utilization (Estimate).

Function Name	Resource					
	LUTs	Registers	F7 Mux	F8 Mux	BRAM	DSP
Sensor Configuration	500	500	30	0	0	1
Image Data Reception	1000	1000	50	30	3	0
Image Data Reordering	2500	3000	250	150	70	0
Image Data Binning and Tagging	1300	1100	0	0	6	0
Image data transmission	500	600	10	0	4	0
Payload Unit Communication	2000	1000	50	5	5	0
ADC Control	1500	4000	500	0	0	0
Total	9300	11200	890	185	88	1

5 PRE-LAYOUT DESIGN AND ANALYSIS

5.1 Printed Circuit Boards Modelling

Directly or indirectly all PCB simulation tools are based on the solution of Maxwell's Equations over various PCB geometries. These four equations as shown below describe how dielectrics and conductors interact with magnetic and electric fields. After all, signals are nothing more than propagating electric and magnetic fields. When the magnetic and electric fields are simulated, the interconnects and all passive components must be translated into conductors and dielectrics, with their related geometries and material properties. [18]

Maxwell's equations for time domain are:

$$\nabla \cdot \epsilon \boldsymbol{E} = \frac{\boldsymbol{\rho}}{\boldsymbol{\epsilon_0}} \qquad 5.1\ [18]$$

$$\nabla \cdot \boldsymbol{B} = \boldsymbol{0} \qquad 5.2\ [18]$$

$$\nabla \times \boldsymbol{E} + \frac{\partial \boldsymbol{B}}{\partial \boldsymbol{t}} = \boldsymbol{0} \qquad 5.3\ [18]$$

$$\nabla \times \boldsymbol{B} - \frac{\mu\epsilon}{\boldsymbol{C}^2} \frac{\partial \boldsymbol{E}}{\partial \boldsymbol{t}} = \mu_{\boldsymbol{0}} \qquad 5.4\ [18]$$

where

B is magnetic field

$\boldsymbol{E}$ is electric field

$\boldsymbol{C}$ is speed of light

ρ is total electric charge density

$\nabla \mathbf{x}$ is nabla curl operator

$\nabla\ \cdot$ is nabla divergence operator

$\boldsymbol{\epsilon_0}$is permittivity of free space

$\mu_0$is permeability of free space

$\boldsymbol{t}$ is time

Maxwell's equations for frequency domain are:

$$\nabla \cdot \epsilon \boldsymbol{E} = \frac{\boldsymbol{\rho}}{\boldsymbol{\epsilon_0}} \quad 5.5\ [18]$$

$$\nabla \cdot \mu \boldsymbol{H} = \mathbf{0} \quad 5.6\ [18]$$

$$\nabla \, \mathrm{x} \, \boldsymbol{E} + \boldsymbol{j} \, \boldsymbol{\omega} \, \mu \, \boldsymbol{H} = \mathbf{0} \quad 5.7\ [18]$$

$$\nabla \, \mathrm{x} \, \boldsymbol{H} - \boldsymbol{j} \, \boldsymbol{\omega} \, \epsilon \boldsymbol{E} = \mathbf{J} \quad 5.8\ [18]$$

where

$\boldsymbol{H}$ is magnetic field

$\boldsymbol{E}$ is electric field

$\boldsymbol{C}$ is speed of light

$\boldsymbol{\rho}$ is total electric charge density

$\nabla \mathbf{x}$ is nabla curl operator

$\nabla\ \cdot$ is nabla divergence operator

$\boldsymbol{\epsilon_0}$is permittivity of free space

$\mu_0$is permeability of free space

$\boldsymbol{J}$ is current density

ω is frequency

5.2 Simulators

The three types of electrical simulation tools that model the analog effects of the interconnects on signal behavior are discussed below.

5.2.1 Electromagnetic (EM) Simulators

Electromagnetic simulators solve the Maxwell's Equations and simulate the magnetic and electric field at various points in the frequency or time domains. [18]

5.2.2 Circuit Simulators

Circuit simulators solve the differential equations that correspond to the numerous circuit elements and include Kirchhoff's voltage and current relationships to predict the voltages and currents at various circuit nodes, in the frequency or time domain. [18]

5.2.3 Behavioral Simulators

Behavioural simulators use models that are based on the transmission lines and passive-element models based on transfer functions that quickly predict the currents and voltages at various nodes. [18]

5.2.4 Component Modeling

Component modelling refers to creating an electrical representation of a device or component that a simulator can interpret and use to predict voltage and current waveforms. The models for active devices, such as transistors and output drivers, are radically different from the models of passive devices, such as all interconnects and discrete components. For active devices, a model is typically either a SPICE compatible model (see below) or an input/output buffer information specification (IBIS) compatible model.

5.2.4.1 SPICE models

A SPICE model of an active device will use either combinations of ideal sources and passive elements or specialized transistor models based on the geometry of the transistors. This allows easy scaling of the transistor’s behaviour if the process technology changes. A SPICE model contains information about the specific features and process technology of a driver. For this reason, most vendors are reluctant to give out SPICE models of their chips since they contain such valuable information. [18] [19]

5.2.4.2 IBIS Models

IBIS is a format that specifies the V-I (Voltage-Current) and V-t (Voltage-Time) characteristics of the input or output drivers. A behavioral simulator will take the Voltage-Current and voltage-time curves of devices and simulate how these curves might change. These curves are affected by the transmission lines, lumped inductor (L), capacitor (C) and resistor (R) elements. The advantage of an IBIS model is that an integrated circuit (IC) manufacturer can provide an IBIS model of its active device drivers without disclosing any confidential information regarding transistor geometry. [18] [19]

5.2.5 Transmission Line Simulators with Example

5.2.5.1 RLGC Model

A 3D electromagnetic (EM) simulation model can be formed to analyse the signal distortion that a physical body induces. The 3D model describes the electrical properties like phase shift and attenuation of a physical body. Using s-parameters RLGC model can be formed. These RLGC models are circuits that can be used in SPICE. [20] The RLGC model in Figure 5.1 has N rows of transmission lines and each of these transmission lines has M sections. Each of the M sections contains a series R+L and G+C to ground and models the electrical performance of single line as a transmission line. [20]

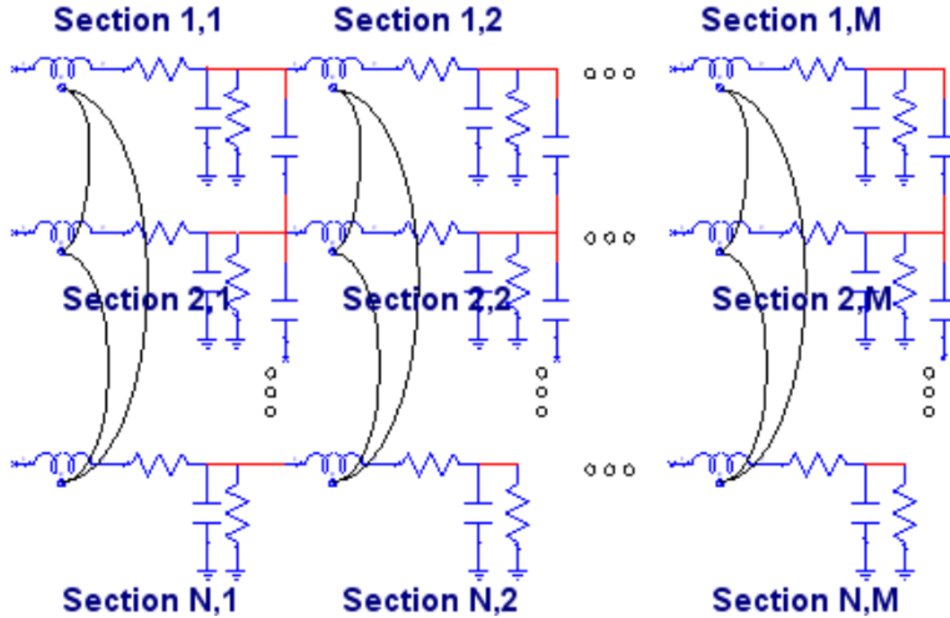


Figure 5.1: Distributed RLGC equivalent model with N number of rows of transmission lines and each of these transmission lines has M number of sections. [20]

Due to partially joined magnetic fields there is coupling between the lines, which is modelled by the coupling of the L in a certain section with the L's in the same section of another line. The charge in these coupled lines affects the charge in another line. As this effect is less noticeable it is generally sufficient to model it by a coupling capacitor between a given line and the neighbouring line.

As the number of sections increases a better time delay model of the physical line is achieved. For lines up to half a wavelength 1 to 4 sections are often enough to have a sufficiently accurate model.

5.3 Simulation Tools for Signal Integrity/Power Integrity and EMC

For high-speed simulation tools, the high-speed designers rely on the venerable IPC-Association Connecting Electronics Industries standard called IPC-D-317 “Design Guide for Electronic Packaging Utilizing High-Speed Techniques”. Table 5.1 lists most of the IPC recognized programs. [21]

Table 5.1: IPC Recognized Tools [21]

Company	Software	Program Category (Impedance Calculator OR SI Tool)	Calculation Method (Field Solver FEA, Field Solver BEM, Simple Equation, Complex Equation)	Website
Avant Corporation Fremont, California	Hspice	Signal Integrity	Field Solver - FEA	https://www.synopsys.com/
Agilent Technologies West Lake Village, California	Advance Design System	Signal Integrity	Complex Equation	https://www.agilent.com/
	HFSS Designer		3D Field Solver FEA	
Allegro Sigrity Santa Clara, California	Allegro Sigrity SI Base Allegro Sigrity PI Base	Signal, Power and Ground Integrity Tool	2D/3D Field Solver	https://www.cadence.com/en_US/home/tools/ic-package-design-and-analysis/si-pi-analysis-integrated-solution/allegro-sigrity-si.html

Company	**Software**	**Program Category (Impedance Calculator OR SI Tool)**	**Calculation Method (Field Solver FEA, Field Solver BEM, Simple Equation, Complex Equation)**	**Website**
Applied Simulation Technology San Jose, California	ApsimSI	Signal Integrity	Field Solver + 2D Complex Equation	http://www.apsimtech.com/
	RADIA	EMI Analysis	Field Solver +2D Complex Equation	
	DELTAI	Signal Integrity	3D Static Solver	
	RPATH	EMI Analysis	3D Static Solver	
	IBIS Tools	Signal Integrity	IBIS Modelling	
Cadence Design Systems San Jose, California	SPECCTRAQuest	Signal Integrity	Field Solver – FEA	https://www.cadence.com/en_US/home.html
	VoltageStorm	Signal Integrity	Complex Equation	
	ClockStorm	Signal Integrity	Complex Equation	
	ElectronStorm	Signal Integrity	Complex Equation	

Company	Software	Program Category (Impedance Calculator OR SI Tool)	Calculation Method (Field Solver FEA, Field Solver BEM, Simple Equation, Complex Equation)	Website
	SI Report	Signal Integrity	Complex Equation	
	Fire & Ice QX	Signal Integrity	3D Field Solver	
Hewlett-Packard Company Palo Alto, CA	MDS Nonlinear Simulator	Signal Integrity	Complex Equation	https://www8.hp.com/us/en/home.html
Mentor Graphics Hyperlynx Redmond, WA	LineSim-PreLayout	Signal Integrity	Complex Equation	https://www.mentor.com/pcb/hyperlynx/signal-integrity/
	BoardSim-PostLayout	Signal Integrity	Complex Equation	
OptEM Eng Calgary, Canada	EMC Workbench	Signal Integrity	2D Field Solver	http://www.optem.com/
	OptEM ID	Signal Integrity	2D/3D Field Solver	
OrCad Beaverton, Oregon	Pspice, Pspice A/D	Signal Integrity	2D+ Field Solver	https://www.orcad.com/

Company	**Software**	**Program Category (Impedance Calculator OR SI Tool)**	**Calculation Method (Field Solver FEA, Field Solver BEM, Simple Equation, Complex Equation)**	**Website**
Polar Instruments Beaverton, Oregon	Si8000m-Impedance calculator Speedstack PCB-Stackup Impedance calculator Si9000e-Signal Integrity Speedstack Si-Stackup Insertion loss solver	Impedance Calculator	2D Field Solver BEM	https://www.polarinstruments.com/
Rogers Corporation Chandler, Arizona	Impedance Calculation Program	Impedance Calculator	Complex Equation	https://www.rogerscorp.com/
Simberian Incorporation	Simbeor	Signal Integrity Tool	Decompositional EM Analysis,	https://www.simberian.com/

Company	Software	Program Category (Impedance Calculator OR SI Tool)	Calculation Method (Field Solver FEA, Field Solver BEM, Simple Equation, Complex Equation)	Website
Las Vegas, Nevada			2D/3D Field Solver	
Zuken USA Inc. Milpitas, California	CR-8000 Design Force	Signal Integrity	Complex Equation 2D Field Solver	https://www.zuken.com/en/

In this work, two tools Hyperlynx LineSim pre-layout and BoardSim post-layout are used for both Signal and Power Integrity Analysis. The latest edition of Hyperlynx is a hybrid type which can provide various levels of simulation and modelling capabilities based on the complexity of problem. It supports all circuit models and behavioral models e.g. HSPICE, IBIS-AMI, ELDO, AMS, IBIS models and S-parameters. For complex geometries such as Vias it provides Integrated 2D/2.5D/3D electromagnetic solvers. The software works with all major PCB layout systems for example Orcad Cadence, Altium, Eagle, Xpedition etc. As shown in Figure 5.2 Hyperlynx SI supports pre-layout and post-layout signal integrity, crosstalk, timing and power-aware simulation. Automated workflows support complete interface-level DDRx verification and compliance analysis of standards-based SerDes channel designs. [22]

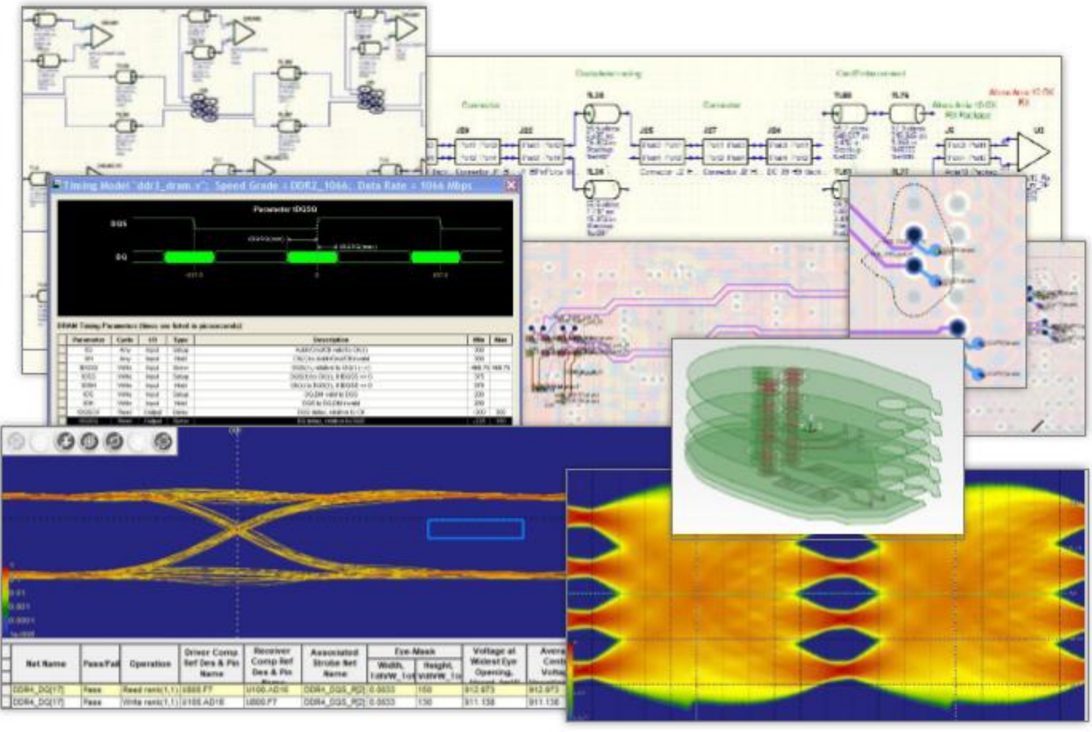


Figure 5.2: Depiction of Mentor Graphics Hyperlynx Simulation Tool. [22]

5.4 Pre-Layout SI/PI Analysis

In pre-layout and post-layout SI/PI analysis for simulation the physical parameters are translated into mathematical models and circuit elements. For pre-layout SI/PI analysis a schematic is built that includes all the functionalities and elements of the simulation. For the purpose of signal integrity these schematics should include IC package models, buffer models, Vias, trace models, discrete components, connectors and cables. In terms of power integrity analysis these models should include plane, plane shapes, power sources, loads, stitching Vias and discrete components.

The main difference between pre-layout analysis and post-layout analysis is that in pre-layout analysis the simulation is performed on the schematics before completing the PCB layout. The post-layout analysis is performed on the completed PCB layout. For example, in post-layout signal integrity analysis exact length of the traces are used in the simulation.

5.4.1 Identification of Critical Interface of CDC Design

The very first step in the analysis flow is to identify which interfaces need to be modelled and analysed. Usually the interfaces switching at high-speed are prone signal and power integrity problems. In CDC Unit design, there are couple of interfaces running at high-speed. For example, the CDC board acquires image data at 250 Mbits/channel. Similarly, it transfers the processed data stream to bus at 1Gbits/s per channel. From the imaging unit to the receiving FPGA, the high-speed LVDS signal has to pass through following critical path that must be modelled and analysed. The hierarchal depiction of critical interfaces is shown in Figure 5.3.

- IDU Image Sensor TO IDU Output Connector
- IDU PCB Connector TO IDU Harness
- IDU Harness TO CDC Input Connector
- CDC Input Connector TO CDC FPGA
- CDC FPGA TO CDC Output Connector
- CDC Output Connector TO CDC Harness
- CDC Harness TO Payload Unit

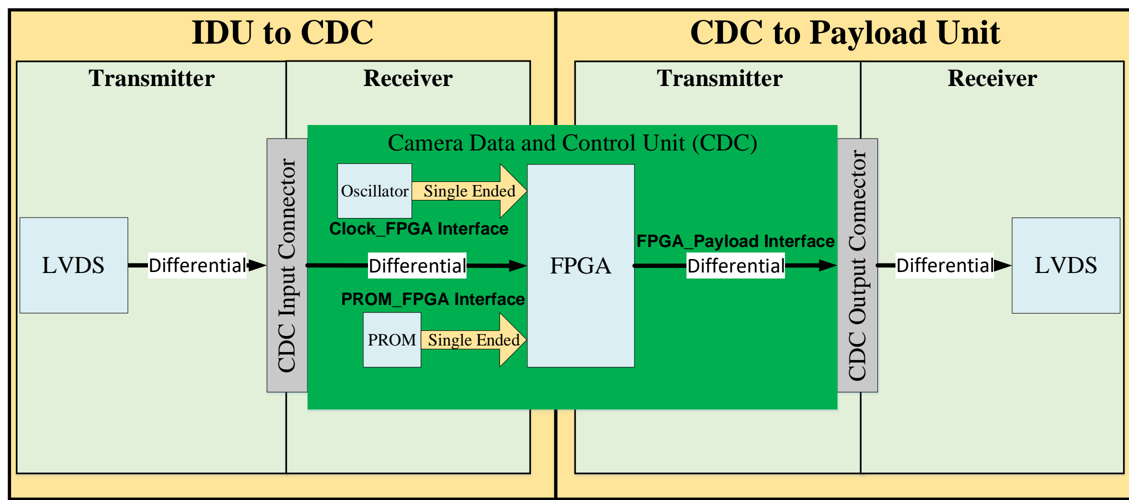


Figure 5.3: Camera Data and Control Unit with all the critical interfaces coming in from the sensor and going out to the Payload Units.

These interfaces include both the input and output interfaces with respect to the FPGA. The critical interfaces from the IDU to the CDC Unit are shown in the Figure 5.4; these interfaces are input to the FPGA.

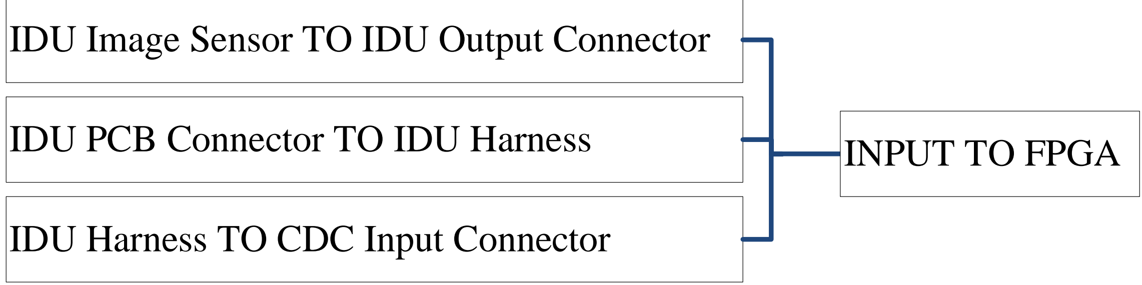


Figure 5.4: Critical Interfaces going into the FPGA.

The critical interfaces from the CDC Unit to the Payload Units are shown Figure 5.5; these interfaces are output from the FPGA.

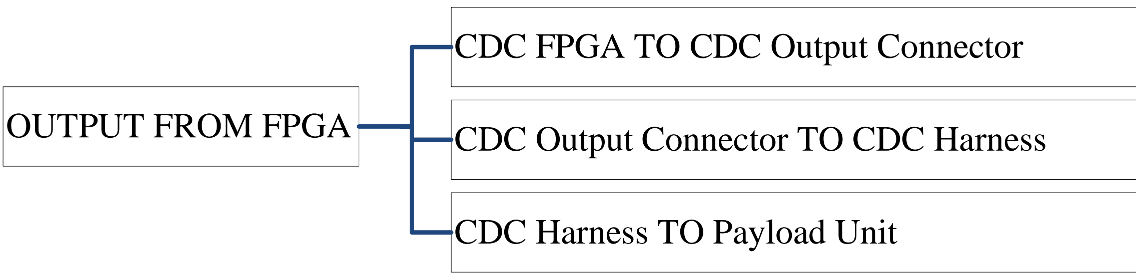


Figure 5.5: Critical Interfaces going out of the FPGA.

5.4.2 Layer Stackup and Impedance Planning

Planning and designing a good layer stackup is an important to assess the performance of an electronic product. A well-planned PCB stackup can reduce impedance mismatches, reflections and crosstalk effects. [23] The layer stackup of the CDC board is shown in Table 5.2. The total number of layers in CDC board is 8; 4 of these layers are signal layers and the other 4 are plane layers.

Table 5.2: Camera Data and Control Unit Layer Stackup detail.

Layer No.	Thickness (oz/mils)	Layers	Dielectric Constant	Single Ended			Differential		
				Trace Impedance (Ω)	Trace Width (mils)	Spacing (mils)	Trace Impedance (Ω)	Trace Width (mils)	Spacing (mils)
1	0.5	TOP		50	6	10	100	4.5	8
	4	PRE-PREG	4						
2	1	GND1							
	6	CORE1	4						
3	0.5	INNER SIGNAL 1		50	6	10	100	4.5	8
	6	PRE-PREG	4.3						
4	1	VCC1							
	6	CORE2	4						
5	1	VCC2							
	6	PRE-PREG	4						
6	0.5	INNER SIGNAL 2		50	6	10	100	4.5	8
	6	CORE3	4						
7	1	GND2							
	6	PRE-PREG	4						
8	0.5	BOTTOM		50	6	10	100	4.5	8

The CDC board has a total thickness of 1.43mm (56.1mils). The CDC board has an unbalanced core of 6mils thickness that have been used in the design with copper thickness of 0.5 oz on one side and 1 oz on the other side. The signal layers used in the board have a copper thickness of 0.5 oz while the plane layers have a copper thickness of 1 oz, the thickness of plane layers is greater than the thickness of signal layers because it has to cater for the power integrity requirements. A detailed layer stackup of the CDC Unit is shown in Figure 5.6.

	Visible	Color	Pour Draw Style	Layer Name	Type	Usage	Thickness mils, oz	Er	Test Width mils	Z0 ohm	Thermal Conductivity Btu/hrftF
1					Dielectric	Solder Mask	0.5	3.9			0.173
2	☑		Solid	TOP	Metal	Signal	0.5	<Auto>	6	54.5	227.476
3					Dielectric	Substrate	4	4			0.173
4	☑		Solid	GND1	Metal	Plane	1	<Auto>	6	65.5	227.476
5					Dielectric	Substrate	6	4			0.173
6	☑		Solid	InnerSignal1	Metal	Signal	0.5	<Auto>	4.5	52.8	227.476
7					Dielectric	Substrate	6	4			0.173
8	☑		Solid	VCC1	Metal	Plane	1	<Auto>	6	58.8	227.476
9					Dielectric	Substrate	15	4			0.173
10	☑		None	VCC2	Metal	Plane	1	<Auto>	6	58.8	227.476
11					Dielectric	Substrate	6	4			0.173
12	☑		None	InnerSignal2	Metal	Signal	0.5	<Auto>	4.5	52.8	227.476
13					Dielectric	Substrate	6	4			0.173
14	☑		None	GND2	Metal	Plane	1	<Auto>	6	65.5	227.476
15					Dielectric	Substrate	4	4			0.173
16	☑		Solid	BOTTOM	Metal	Signal	0.5	<Auto>	6	54.4	227.476
17					Dielectric	Solder Mask	0.5	4			0.173

Figure 5.6: Detailed Layer Stackup of CDC.

In the layer stackup the signal layers are arranged in such a way that they have either a power plane or ground plane as a return path. Two types of layer arrangements Plane Signal Plane (PSP) and Plane Signal Signal Plane (PSSP) are used in the design. All the critical signals (e.g. LVDS) are routed on the PSP layers. In the PSSP layers one signal layer has high-speed signals while the other signal layer has the low-speed signals. The PSSP arrangement is used to reduce the crosstalk effects.

On each signal layer the controlled impedance of 50 ohm and 100 ohms is achieved for single-ended signals and differential signals, respectively, through setting the copper thickness and dielectric thickness.

The layer stackup diagram shown in Figure 5.7 provides an overview of how a PCB layer stackup will look. The layer stackup shows the trace width and separations.

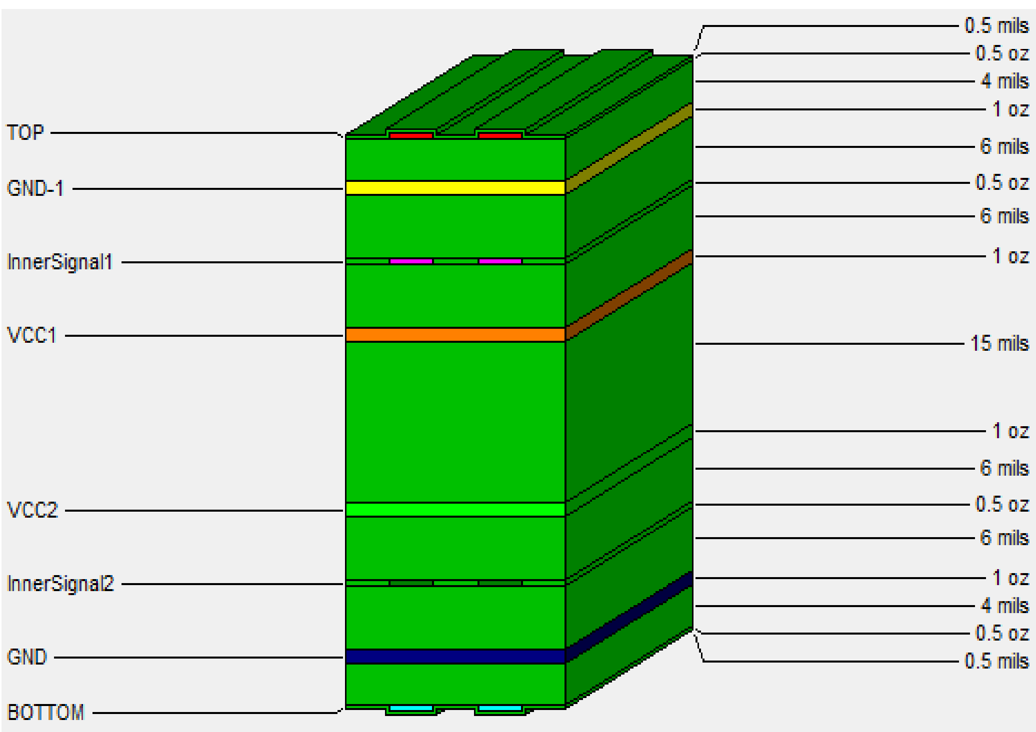


Figure 5.7: Layer Stackup of CDC showing different layers the pre-peg and core between them and their thicknesses.

5.4.3 Pre-Layout Signal Integrity Analysis

The objective is to perform simulation-based pre-layout Signal integrity (SI) analysis of the CDC Schematic. The CDC schematic consists of several critical high-frequency interfaces, one of which is the sensor data interface that has 16 differential LVDs channels. The CDC FPGA receives the LVDS signals at a rate of 250 Mbps per channel from the image sensor and transfers it to payload units at a rate of 1Gbps. For SI analysis the IBIS model of the FPGA [24], the IBIS model of LVDS transceivers [25] and S-parameters for connectors [26] are used.

5.4.3.1 IDU to CDC Data Flow

The differential LVDS Buffer is used as a driver (Image Sensor) and a Kintex 7 FPGA as a receiver. Both are interconnected through a differential transmission line of approximately 100ohm differential impedance, with the interface operating at 250MHz. The component placement is done on both the top layer and bottom layer of the PCB, due to which a small portion of data is routed either on top layer or bottom layer and then the routing layer is also changed to an inner layer through Vias. These inner signals are adjacent to solid plane also shown in layer stackup to cater for crosstalk effects. The

trace width for these data lines is 4.5mils and trace separation is 8mils. Figure 5.8 shows the following elements involved in the transmitter and receiver path of the LVDS data coming from the IDU to CDC:

- Image Detector Unit Transmitter
- Image Detector Unit Connector
- Image Detector Harness
- Camera Data and Control Unit Input Connector
- Camera Data and Control Unit PCB Trace
- Camera Data and Control Unit PCB VIAs
- Camera Data and Control Unit FPGA

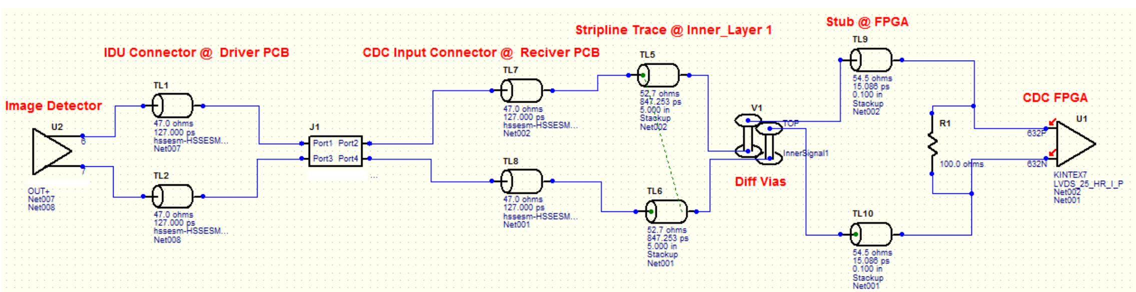


Figure 5.8: LineSim Schematic of Data coming from IDU to CDC.

The resultant waveforms at receiver for offset voltage, output voltages high and low, rise time, fall time, eye height and width are shown in Table 5.3. The minimum, nominal, maximum and observed voltages and timing specifications of the waveforms and their comparison with LVDS standard are also specified. The result also shows the minimum effects of ringing. The waveforms received at the FPGA input are shown in Figure 5.9 and the corresponding Eye Diagram is shown in Figure 5.10.

Table 5.3: Minimum, Nominal, Maximum and observed Voltages and Timing Specifications of Resultant 250MHz Waveform at FPGA.

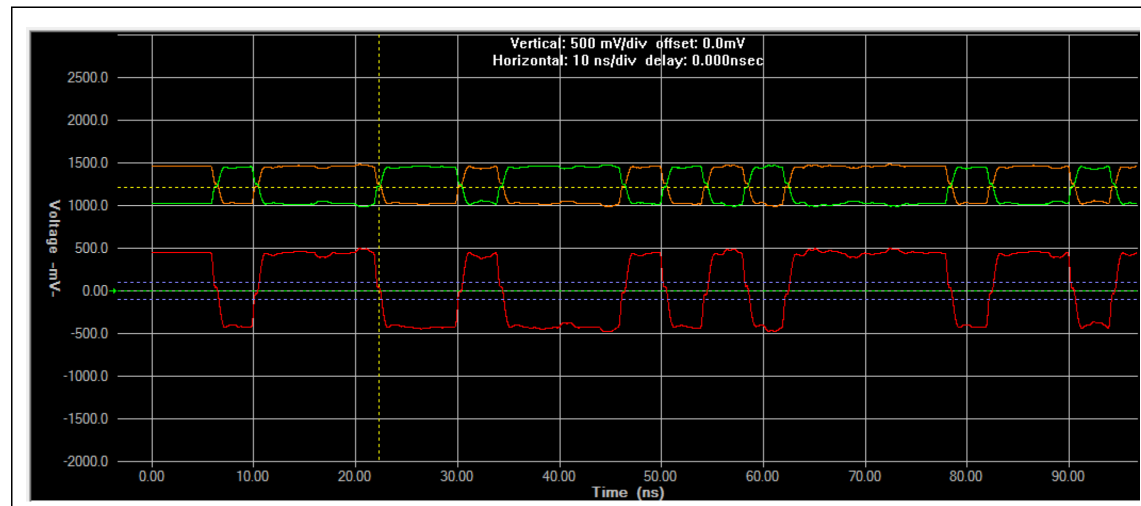


Figure 5.9: Waveforms Received at FPGA Input.

Symbol	Parameter	Minimum	Nominal	Maximum	Observed
VOS	Offset voltage	1.080V [27]	1.2V [27]	1.375V [27]	1.24V
VOH	Output logic high	-	1.4V [28]	1.6V	1.41V
VOL	Output Logic Low	-	1.0V [28]	-	0.982V
Tr	Rise Time	200ps [27]	-	800ps (1/5th of 250MHz) [18]	749ps
Tf	Fall Time	200ps [27]	-	800ps (1/5th of 250MHz) [18]	751ps
Eye Diagram	Eye Width	2.66ns [18]	-	-	3.6ns
	Eye Height	±100mV (200mV P-P)	-	-	732mV P-P
	Figure 5.10: Eye Diagram at FPGA.				

5.4.3.2 CDC to Payload Units Data Flow

The differential LVDS Buffer is used as a receiver (Payload Units) and Kintex 7 FPGA as a transmitter. Both are interconnected through a differential transmission line of approximately 100ohm differential impedance, with the interface operating at 1 GHz. The component placement is done on both top layer and bottom layer of the PCB, due to which a small portion of data is routed either on top layer or bottom layer and then the routing layer is also changed to an inner layer through Vias. These inner signals are adjacent to solid plane also shown in layer stackup to cater for crosstalk effects. The trace width for these data lines is 4.5mils and trace separation is 8mils. Figure 5.11 shows the following elements involved in the transmitter and receiver path of the LVDS data coming from the CDC to Payload Units:

- Camera Data and Control Unit FPGA Transmitter
- Camera Data and Control Unit PCB VIAs
- Camera Data and Control Unit PCB Trace
- Camera Data and Control Unit Output Connector
- Camera Data and Control Unit Harness
- Payload Unit Receiver

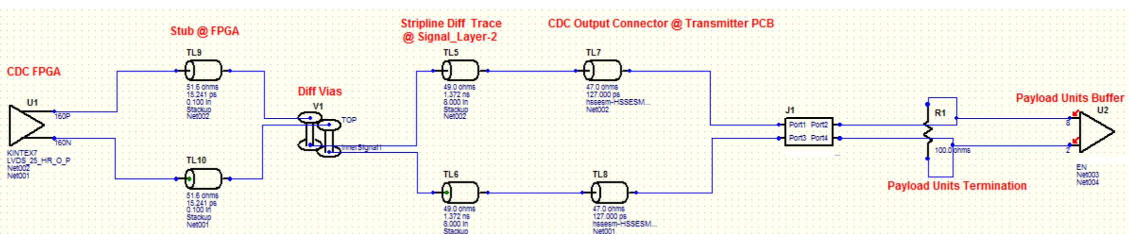


Figure 5.11: LineSim Schematic of Data going from CDC to Payload Units.

The resultant waveforms at the receiver for offset voltage, output voltages high and low, rise time, fall time, eye height and width are shown in Table 5.4. The minimum, nominal, maximum and observed voltages and timing specifications of waveforms and their comparison with LVDS standard are also specified. Figure 5.12 shows the waveforms received at the payload unit and Figure 5.13 shows the Eye Diagram at the payload unit.

Table 5.4: Minimum, Nominal, Maximum and observed Voltages and Timing Specifications of Resultant 1GHz Waveform at Payload Unit.

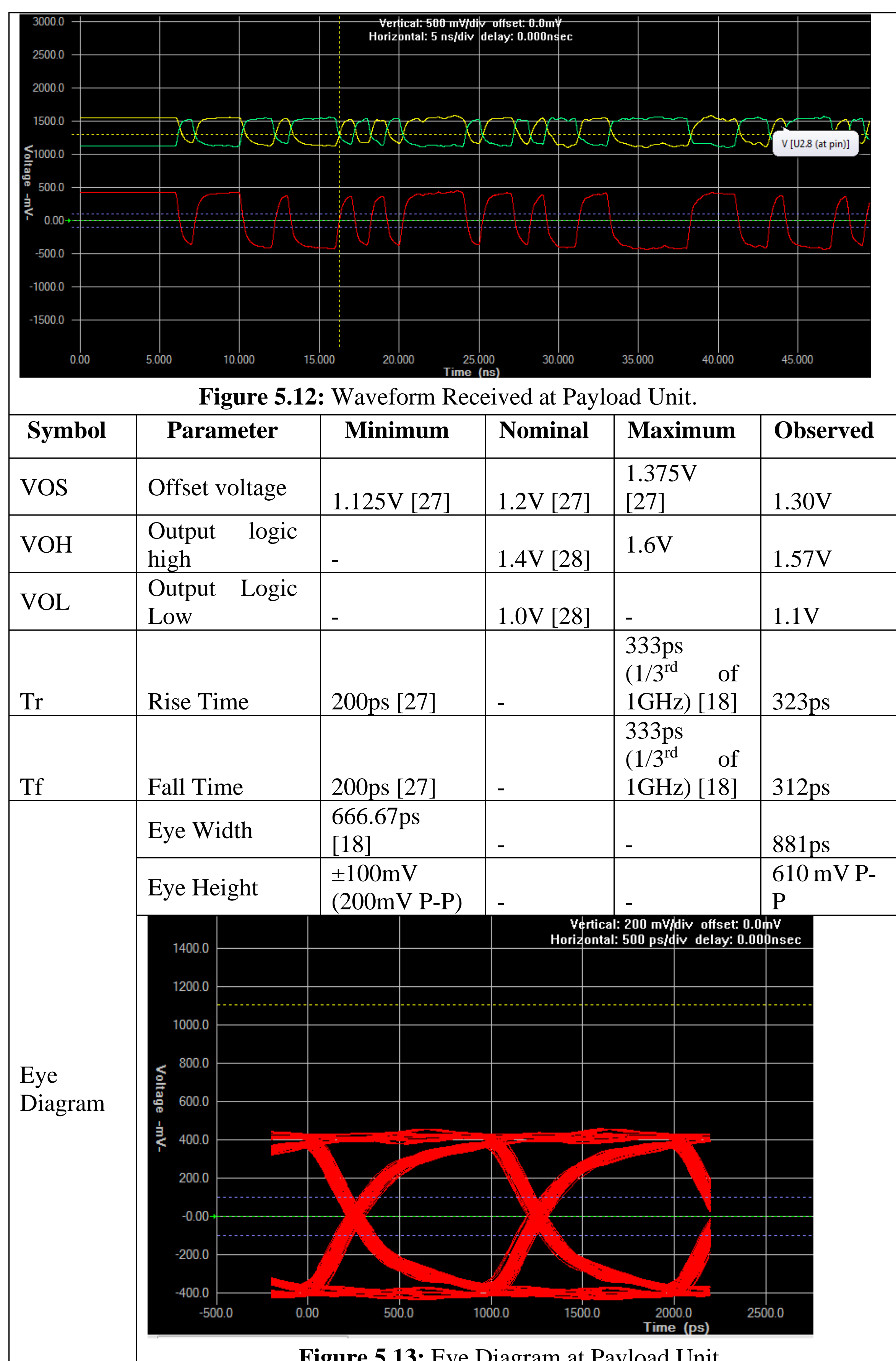


Figure 5.12: Waveform Received at Payload Unit.

Symbol	Parameter	Minimum	Nominal	Maximum	Observed
VOS	Offset voltage	1.125V [27]	1.2V [27]	1.375V [27]	1.30V
VOH	Output logic high	-	1.4V [28]	1.6V	1.57V
VOL	Output Logic Low	-	1.0V [28]	-	1.1V
Tr	Rise Time	200ps [27]	-	333ps (1/3rd of 1GHz) [18]	323ps
Tf	Fall Time	200ps [27]	-	333ps (1/3rd of 1GHz) [18]	312ps
Eye Diagram	Eye Width	666.67ps [18]	-	-	881ps
	Eye Height	±100mV (200mV P-P)	-	-	610 mV P-P

Figure 5.13: Eye Diagram at Payload Unit.

5.4.3.3 CDC Crosstalk Analysis

The aggressor line is an LVDS data channel that transfers the data from the IDU sensor to the CDC FPGA. The agressor line runs at nominal rate of 250 Mbps and causes crosstalk effects in nearby coupled transmission lines. Figure 5.14 below shows the setup for simulating the crosstalk. The effect of the aggressor line's crosstalk is simulated with the adjacent data channel. Both the aggressor line and victim line are coupled. The coupling region is set to more than an inch. Only the aggressor line driver is in data transfer mode the victim line driver is stacked low and generating no ouptut signal at load.

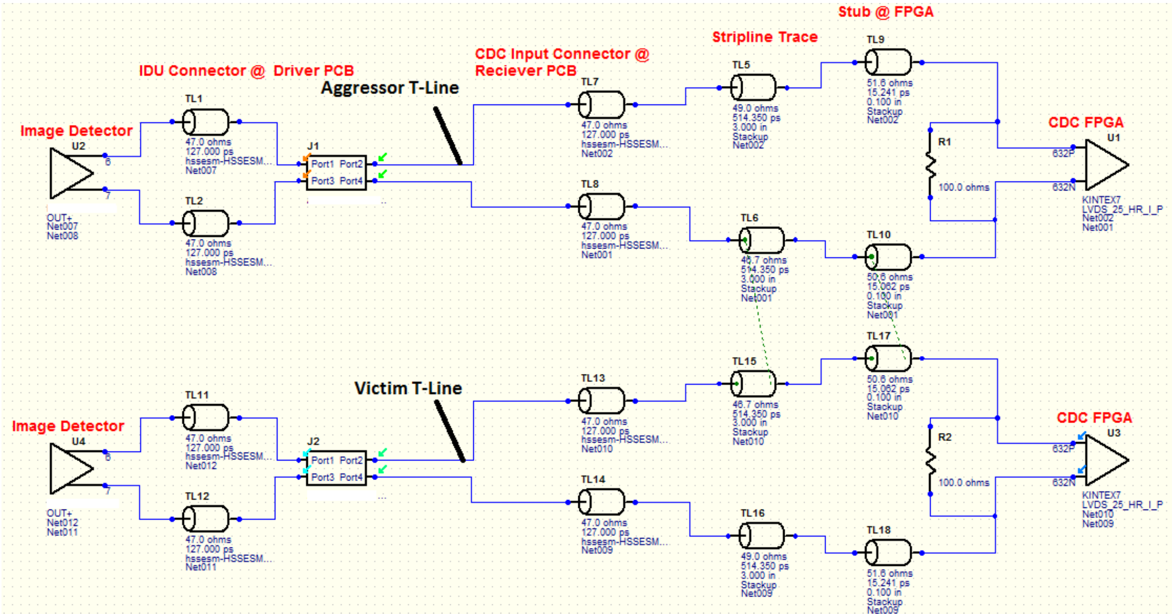


Figure 5.14: Line-Sim Schematic for the Crosstalk Analysis with the Aggressor and the Victim transmission line.

The peak-to-peak voltage observed at the receiver of the victim transmission line for coupling distances of 4 mils and 8 mils is shown in Table 5.5.

Table 5.5: Coupling distance VS Vpp effect on Crosstalk.

Coupling Distance	**Vpp (Peak to Peak Voltage)**
4 mils	42.11 mV
8 mils	17.3 mV

Figure 5.15: Crosstalk Values at Victim Transmission Line Receiver.

For 4 mil or less coupling distance, the aggressor line induces an unwanted signal of 40mV in the victim line receiver, which is stacked low. The crosstalk is reduced to approximately 17mV when the coupling distance is increased to 8mil. Therefore, it is required to keep the aggressor line more than 8mil apart from a victim line while routing on same layer; this will reduce crosstalk to a negligible level.

5.4.4 Pre-Layout Power Integrity Analysis

Before performing the power integrity analysis, the power requirements of each IC used in the design, and hence power requirement of each power line, must be known. This leads to the determination of the impedance profile of each power plane with respect to the switching frequencies of the ICs. Table 5.6 shows the power requirements for power integrity analysis of CDC.

Table 5.6: Power Plane Requirements of CDC.

Supply Name	Plane Voltage (V)	Power (W)	Peak Transient Current (A)	Allowable Voltage Ripple	Ripple (%)	Target Plane Impedance (mΩ)	Reference Plane	Decoupling/Bulk Capacitors [29]
VCC1V0	1	1.5	1.8	+/- 0.03	+/- 3	97	GND	4.7µF x 5 330µF x 3 100µF x 2
VCC1V8	1.8	1.8	1.2	+/-0.09	+/- 5	427	GND	47µF x 3 100µF x 1
VCC3V3	3.3	2.49	0.902	+/-0.165	+/- 5	1042	GND	47µF x 1 100µF x 1
VCC2V5	2.5	0.25	0.12	+/-0.125	+/- 5	5937	GND	100µF x 2

The power integrity pre-layout analysis is basically performed to validate the power delivery network using initial board constraints; pre-layout analysis is performed during schematic design process, before routing the board. With a known PCB stackup and board size and power regulation and power dissipation network, many power integrity issues can be analysed and optimized before routing the PCB. A common power delivery network (PDN) consists of the following

- ICs
- Decoupling Capacitors
- Power Buses (Power/Ground)
- Voltage Regulation

5.4.4.1 Pre-Layout Decoupling Analysis

The decoupling analysis is analysed using Power Delivery Network (PDN) tool. [30] The PDN tool analyses the plane impedance of each power plane referenced to ground and illustrates the behaviour of decoupling capacitors at different frequencies. The formula for calculating target impedance is:

$$\boldsymbol{Z_t = \frac{V_p * V_r}{It_{max}}} \quad 5.9\ [30]$$

where

Z_t is Target Impedance

V_p is Plane Voltage

V_r is Maximum Allowable Ripple Voltage

It_{max} is Maximum transient current that can be drawn from power plane.

The main objective of the decoupling analysis is to analyze and improve the impedance response of the power delivery network; the first step is to calculate the target impedance of power plane in PCB keeping in view the plane voltage ripple factor and plane current requirement. Table 5.7 shows the target impedance requirement of all power planes of the CDC Unit.

Table 5.7: Shows the effective impedance on VCC1V0 supply with both recommended capacitors and additional bulk/decoupling capacitors.

Supply Name	Plane Voltage (V)	Power (W)	Peak Transient Current (A)	Allowable Voltage Ripple	Ripple (%)	Target Plane Impedance (mΩ)	Reference Plane
VCC 1V0	1	1.5	1.8	+/- 0.03	+/- 3	97	GND
Recommended Decoupling/Bulk Capacitors 4.7µF x 5 330µF x 3 100µF x 2					Additional Decoupling/Bypass Capacitors 4.7µF x 5 330µF x 3 100µF x 2 1µF x 4		
Figure 5.16: The plot shows the effective impedance of 1V0 line with recommended capacitors.					**Figure 5.17:** The plot shows the effective impedance of 1V0 line with additional decoupling/bypass capacitors.		

As shown in Figure 5.16 that the impedance profile of the 1V plane is quite stable. The impedance profile is said to be stable if it is lower than the threshold target impedance up to at least 100 MHz of bandwidth. The capacitors having higher values, for example 100µf, 330µf, etc., have also bulkier packages. Therefore, due to higher parasitic impedance these cover lower frequency range in stabilizing impedance of power delivery network. As the impedance plot is already lower than the corresponding target

impedance (blue line), there is no need to add any bulk capacitors, though a few high-frequency and smaller package capacitor for example 1µf have been added to shift the plot a bit nearer to the 100 MHz line. The profile after addition of capacitors is shown in Figure 5.17. [18]

Table 5.8: Shows the effective impedance on VCC1V8 supply with both recommended capacitors and additional bulk/decoupling capacitors.

<table>
<tr><th>Supply Name</th><th>Plane Voltage (V)</th><th>Power (W)</th><th>Peak Transient Current (A)</th><th>Allowable Voltage Ripple</th><th>Ripple (%)</th><th>Target Plane Impedance (mΩ)</th><th>Reference Plane</th></tr>
<tr><td>VCC 1V8</td><td>1.8</td><td>1.8</td><td>1.2</td><td>+/- 0.09</td><td>+/- 5</td><td>427</td><td>GND</td></tr>
<tr><td colspan="5">Recommended Decoupling/Bulk Capacitors
47µF x3
100µF x1</td><td colspan="3">Additional Decoupling/Bypass Capacitors
47µF x3
100µF x1
680µF x2
1µf x3
0.47µF x2</td></tr>
<tr><td colspan="5">Figure 5.18: The plot shows the effective impedance of 1V8 line with recommended capacitors.</td><td colspan="3">Figure 5.19: The plot shows the effective impedance of 1V8 line with additional decoupling/bypass capacitors.</td></tr>
</table>

Similarly, to the 1V0 plane a few more capacitors are added in 1.8V plane, 3.3V plane and 2.5V plane to improve the bandwidth of impedance profile.

The original and improved profiles are shown in Table 5.8, Table 5.9 and Table 5.10.

Table 5.9: Shows the effective impedance on VCC3V3 supply with both recommended capacitors and additional bulk/decoupling capacitors.

<table>
<tr><th>Supply Name</th><th>Plane Voltage (V)</th><th>Power (W)</th><th>Peak Transient Current (A)</th><th>Allowable Voltage Ripple</th><th>Ripple (%)</th><th>Target Plane Impedance (mΩ)</th><th>Reference Plane</th></tr>
<tr><td>VCC 3V3</td><td>3.3</td><td>2.49</td><td>0.902</td><td>+/- 0.165</td><td>+/- 5</td><td>1042</td><td>GND</td></tr>
<tr><td colspan="5">Recommended Decoupling/Bulk Capacitors
47µF x1
100µF x1</td><td colspan="3">Additional Decoupling/Bypass Capacitors
47µF x1
100µF x1
680µF x3
100µF x3</td></tr>
<tr><td colspan="5">Figure 5.20: The plot shows the effective impedance of 3V3 line with recommended capacitors.</td><td colspan="3">Figure 5.21: The plot shows the effective impedance of 3V3 line with additional decoupling/bypass capacitors.</td></tr>
</table>

Table 5.10: Shows the effective impedance on VCC2V5 supply with both recommended capacitors and additional bulk/decoupling capacitors

Supply Name	**Plane Voltage (V)**	**Power (W)**	**Peak Transient Current (A)**	**Allowable Voltage Ripple**	**Ripple (%)**	**Target Plane Impedance (mΩ)**	**Reference Plane**
VCC 2V5	2.5	0.25	0.12	+/- 0.125	+/- 5	5937	GND

Recommended Decoupling/Bulk Capacitors	Additional Decoupling/Bypass Capacitors
100µF x2	100µF x2 680µF x2 100µF x3
Figure 5.22: The plot shows the effective impedance of 2V5 line with recommended capacitors.	**Figure 5.23:** The plot shows the effective impedance of 2V5 line with additional decoupling/bypass capacitors.

6 POST-LAYOUT DESIGN AND ANALYSIS

6.1 Board Layout and Planes

In post-layout signal integrity analysis, each of the critical high-speed interfaces is analysed by importing the actual routed board into a SI simulator. The CDC routed board for the post-layout analysis is shown in Figure 6.1. The CDC Unit receives data from the IDU through connector J3 processes it and then transfers the data to payload units through connector J1. During board layout, certain design rules have been taken into consideration. These include the general guidelines for high-speed boards, specific design considerations mentioned by IC manufacturers and the design rules generated by pre-layout SI/PI analysis.

As determined in pre-layout analysis, the trace width and heights are configured in layout software to achieve the required impedance profile of each of layer as targeted. The CDC board has 8 layers in total. Four layers have been used to accommodate the routing budget of the board. These four layers include Top/Bottom and two of them are inner signal layers. The top and bottom layers provide the space for component placement and low-speed small routes and stubs have been routed on these layers. The inner signal layers are specially planned for distribution of high-speed routing.

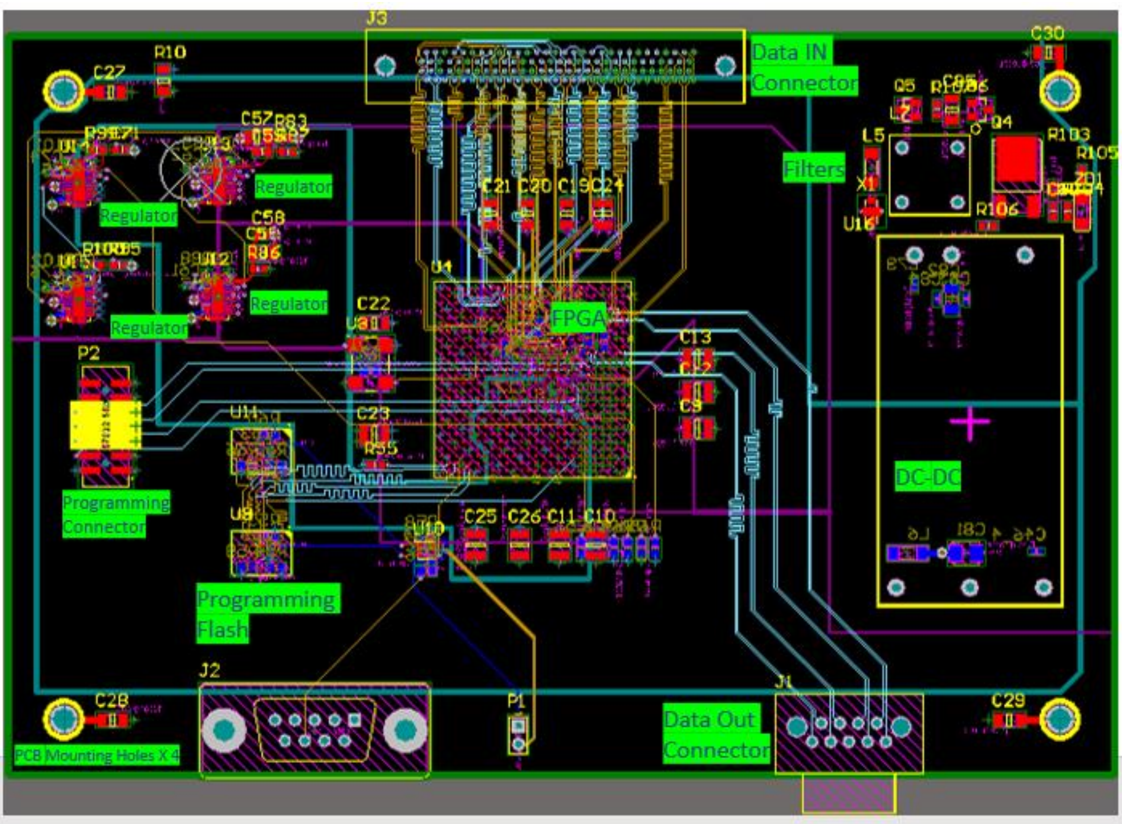


Figure 6.1: PCB Layout of the CDC.

As for as the power plane are concerned, layer stackup is designed to be symmetric from the point of a vertical bisector. This balance of copper distribution on both halves of the stackup is usually recommended for post-fabrication performance of stackup, which prevents rupture and curving in PCBs over a long time of operation. Four power/ground planes have been reserved for the power delivery network of all power supplies. Two layers are used for power and remaining two for ground. The ground layers are simply assigned to the upper and lower half of stackup each to provide return path symmetry in both halves. While power planes are assigned to each of the power supplies with different weights, priority is given to supplies having more load current. For example, the FPGA core voltage, has more load points on the board for the 3.3V line, which is spread geometrically over the large number of points over the board.

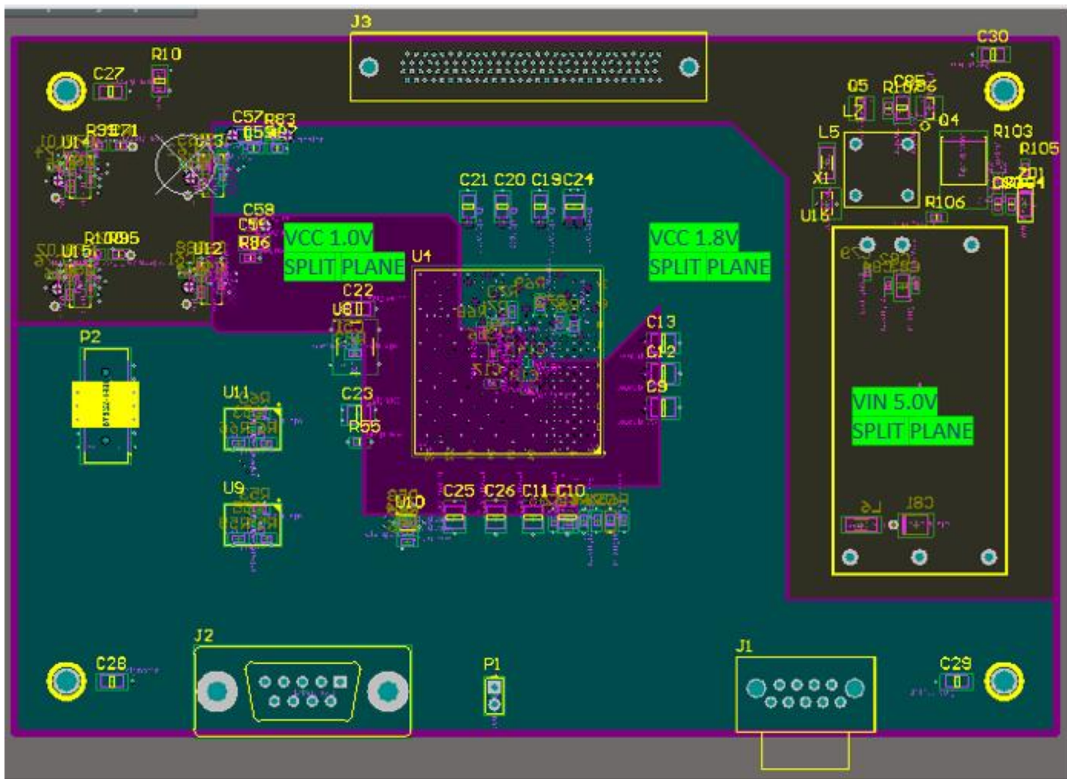


Figure 6.2: CDC PCB VCC1 Plane, the VCC1 plane has split planes for 5V0, 1V8 and 1V0 supplies.

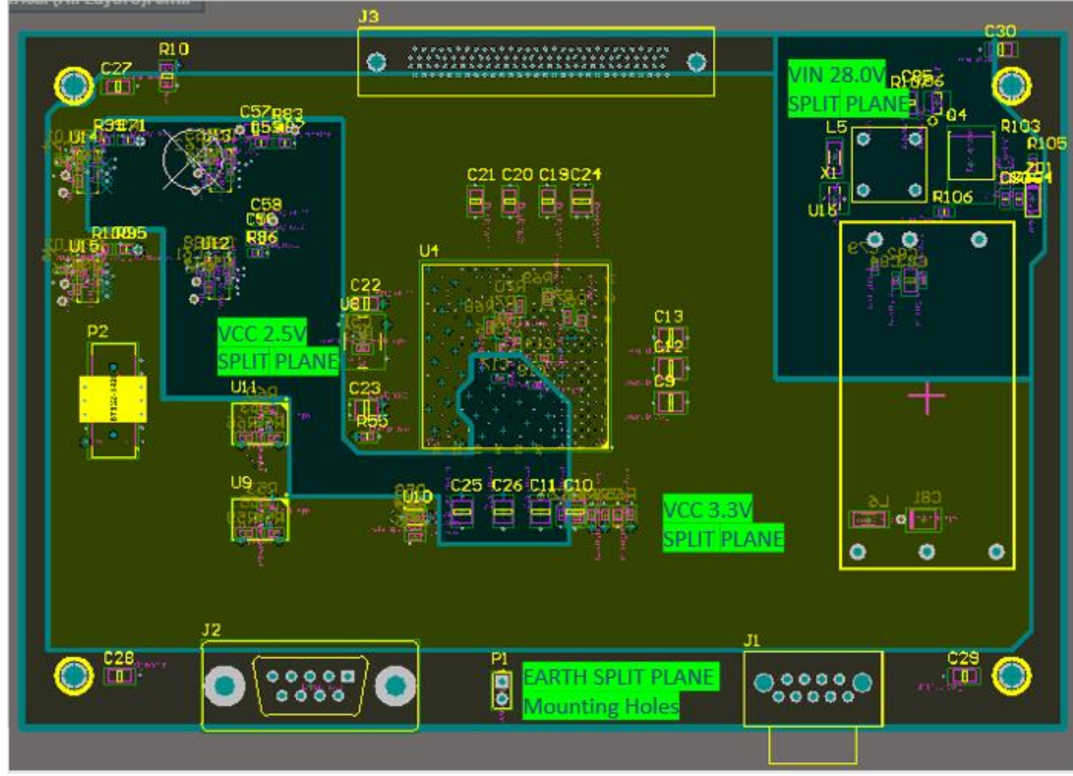


Figure 6.3: CDC PCB VCC2 Plane, the VCC2 plane has split planes for 28V0, 3V3, and 2V5 supplies. VCC2 layer also has Chassis Guard Ring.

6.2 Post Layout Signal Integrity Analysis

At pre-layout level the signal integrity behaviour is analysed with comparatively lesser design information than in the post-layout analysis. At post-layout level, the SI simulations are performed by importing complete CAD geometries, including routes, Vias, stackup and PWR/GND planes; that is why post-layout analysis is a more accurate approximation. Post-layout simulations not only validate the pre-layout results, but also provide of any design change in case of any anomaly observed. This reduces the chances of deviation of post-fabrication performance from expected performance. As shown in Figure 6.4, all of the above mentioned sensitive high-speed interface has been imported along with complete CAD information of the board, including board stackup, packages routed traces, Vias, PWR/GND planes, etc.

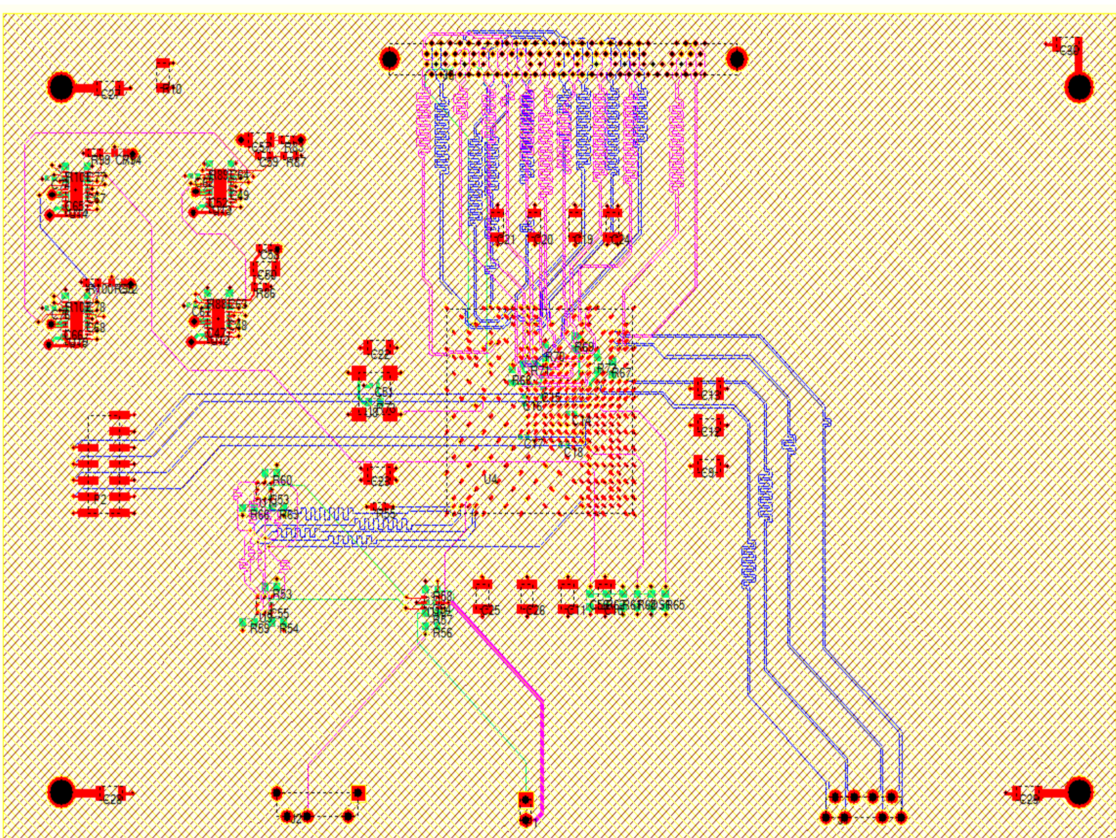


Figure 6.4: Depiction of CDC Board geometries imported in Hyperlynx BoardSim.

6.2.1 Post-Layout Simulations of Critical Interfaces

In the previous chapter the critical interfaces prone to signal integrity problems were identified and analysed with pre-layout level simulation results. In this section the behaviour of these interfaces is analysed at post-layout level. The critical components on the board are assigned the corresponding IBIS model provided by the manufacturer.

Further, the board is configured with PWR/GND nets of corresponding stimulus for each of interface.

6.2.1.1 CDC Input Connector to CDC FPGA (Image Data Reception from IDU)

Input interface routing is shown in Figure 6.5 and Figure 6.6 below. To avoid crosstalk input channels are accommodated in different inner layers. Every routing layer has a corresponding solid plane beneath it to achieve strong coupling between signal routes and return path. The reason for this design practice is to avoid unnecessary EM radiation at board level of high-speed signals causing EMC issues at system level.

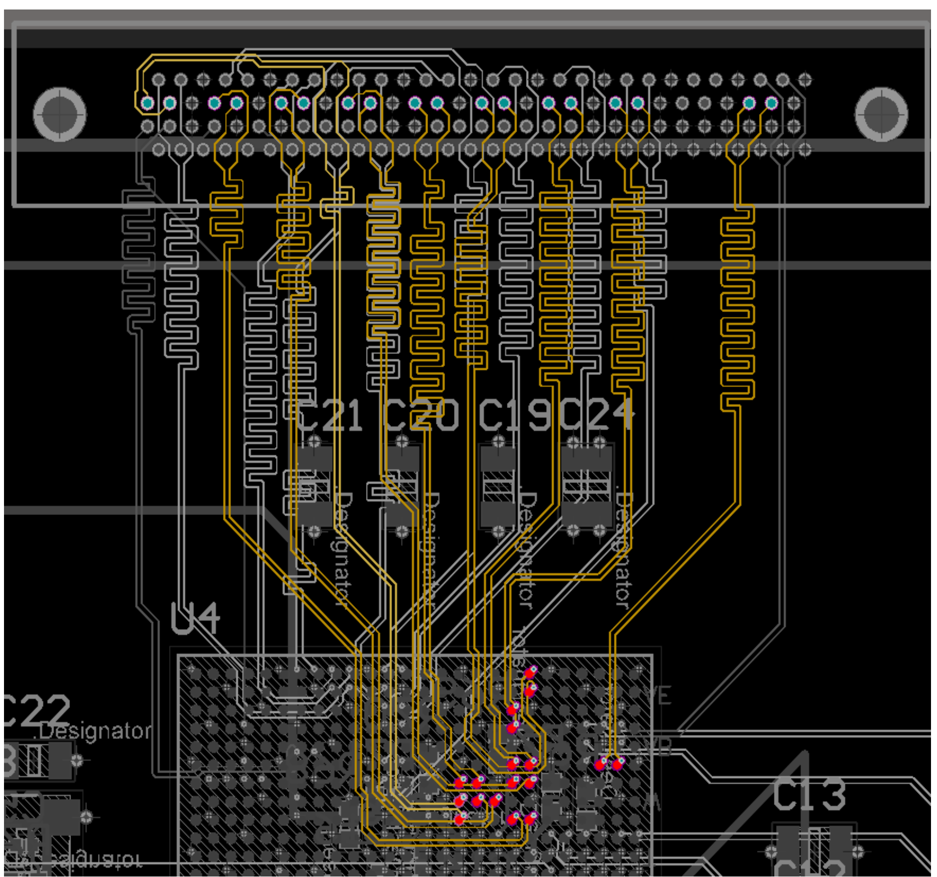


Figure 6.5: Inner Signal 1 showing Input Data Channels coming from IDU.

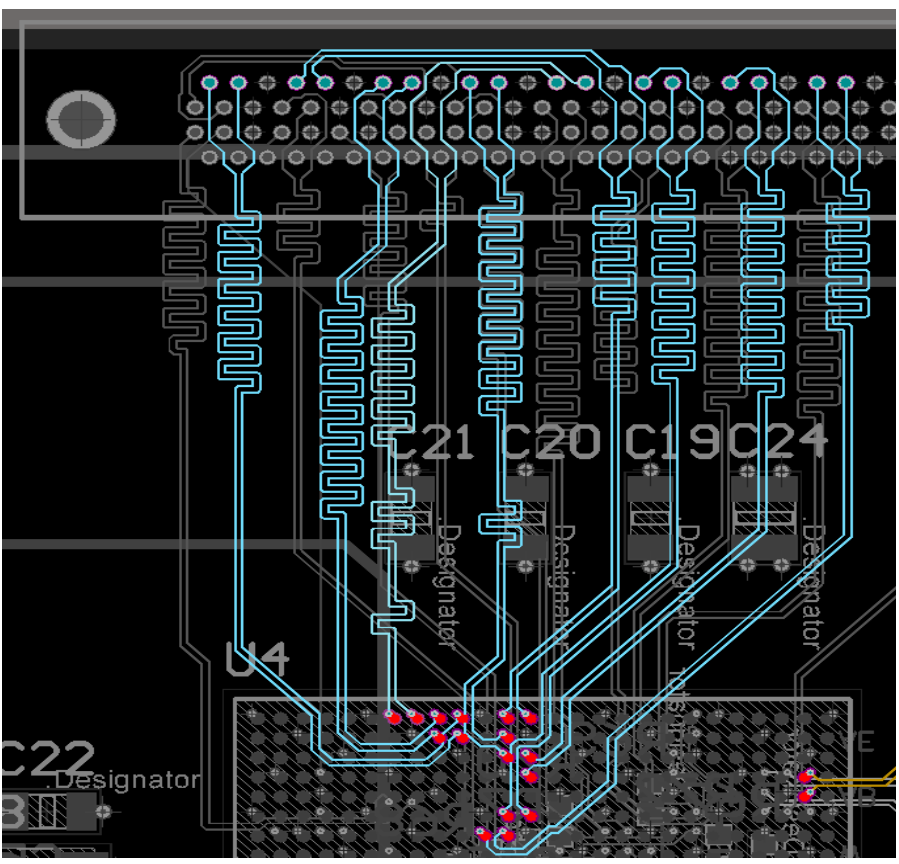


Figure 6.6: Inner Signal 2 showing Input Data Channels coming from IDU.

All these signals have been simulated by injecting a pseudo-random bit steam (PRBS) having a data rate of 250Mbits/s. Gaussian noise of 5% has also been injected to observe worst case response of the input channels at given data rate.

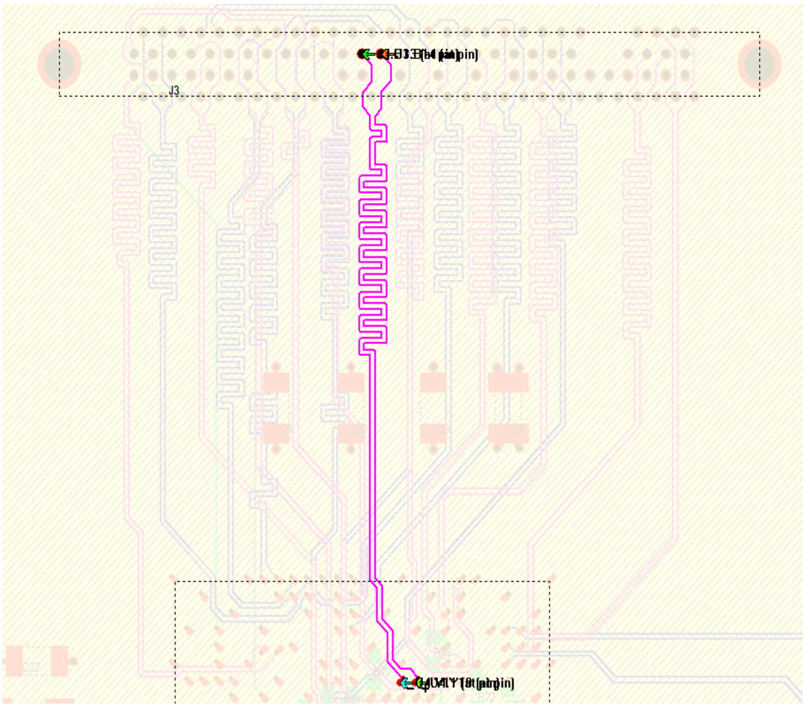
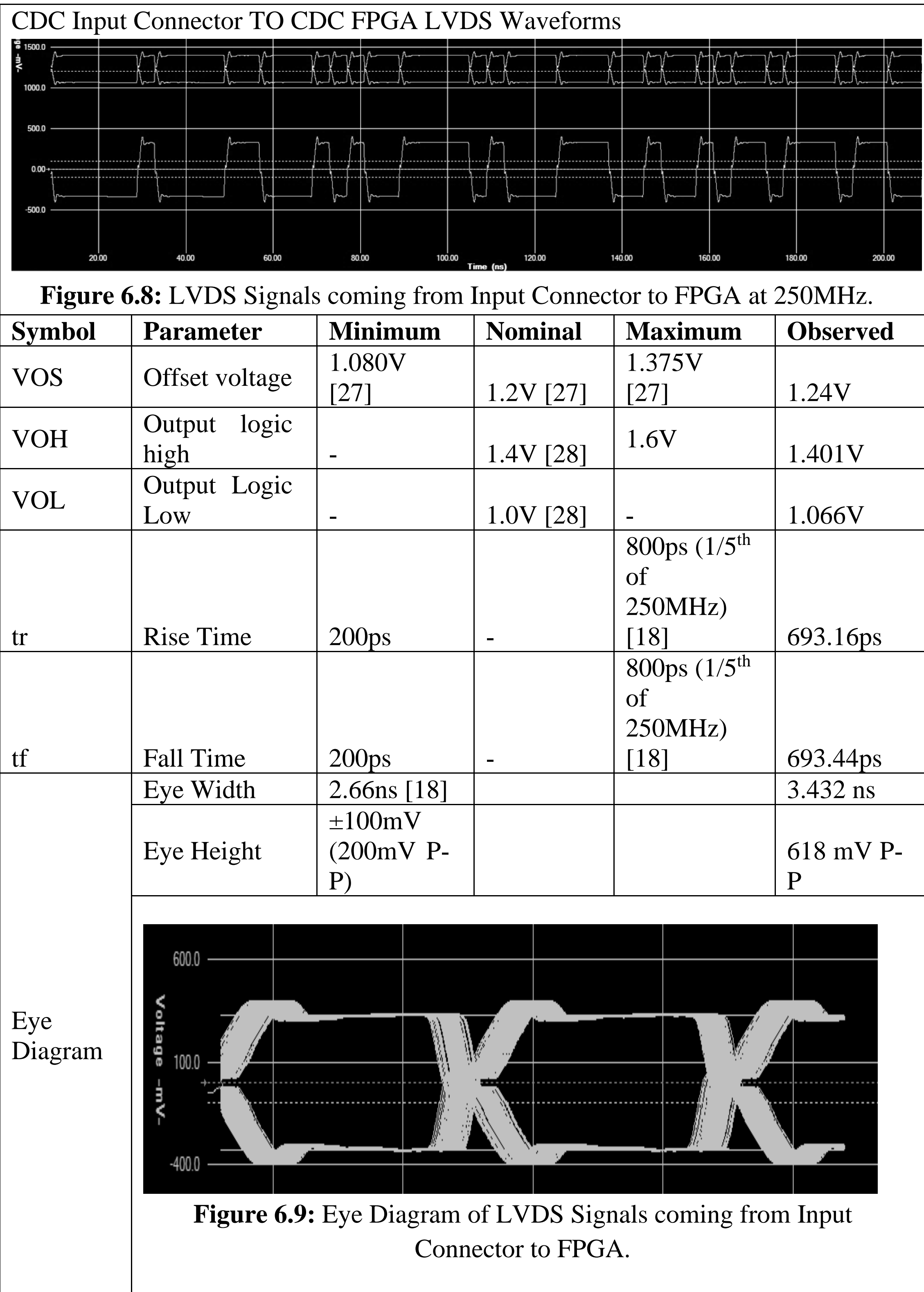


Figure 6.7: Typical Input Signal Simulation.

The Table 6.1 shows the observed parameters of the LVDS waveform and the eye diagram of the signal coming to the CDC FPGA routed through the input connector.

Table 6.1: Simulation results of received waveform at input interface.



CDC Input Connector TO CDC FPGA LVDS Waveforms

Figure 6.8: LVDS Signals coming from Input Connector to FPGA at 250MHz.

Symbol	Parameter	Minimum	Nominal	Maximum	Observed
VOS	Offset voltage	1.080V [27]	1.2V [27]	1.375V [27]	1.24V
VOH	Output logic high	-	1.4V [28]	1.6V	1.401V
VOL	Output Logic Low	-	1.0V [28]	-	1.066V
tr	Rise Time	200ps	-	800ps (1/5th of 250MHz) [18]	693.16ps
tf	Fall Time	200ps	-	800ps (1/5th of 250MHz) [18]	693.44ps
Eye Diagram	Eye Width	2.66ns [18]			3.432 ns
	Eye Height	±100mV (200mV P-P)			618 mV P-P

Figure 6.9: Eye Diagram of LVDS Signals coming from Input Connector to FPGA.

6.2.1.2 CDC FPGA to CDC Output Connector

The Figure 6.10 below shows the on board output data interface from the FPGA device to output connector of board. All these channels are stripline transmission lines, i.e. these are routed to internal routing layers of the PCB stackup to avoid any kind of EMI/EMC issues. For simulation purposes the output is connected with a 100 ohm differential load. A PRBS waveform is generated at the FPGA output and signal integrity of received waveform is analysed at 100ohm termination. All the four channels are simulated to assure the SI stability at the receiver.

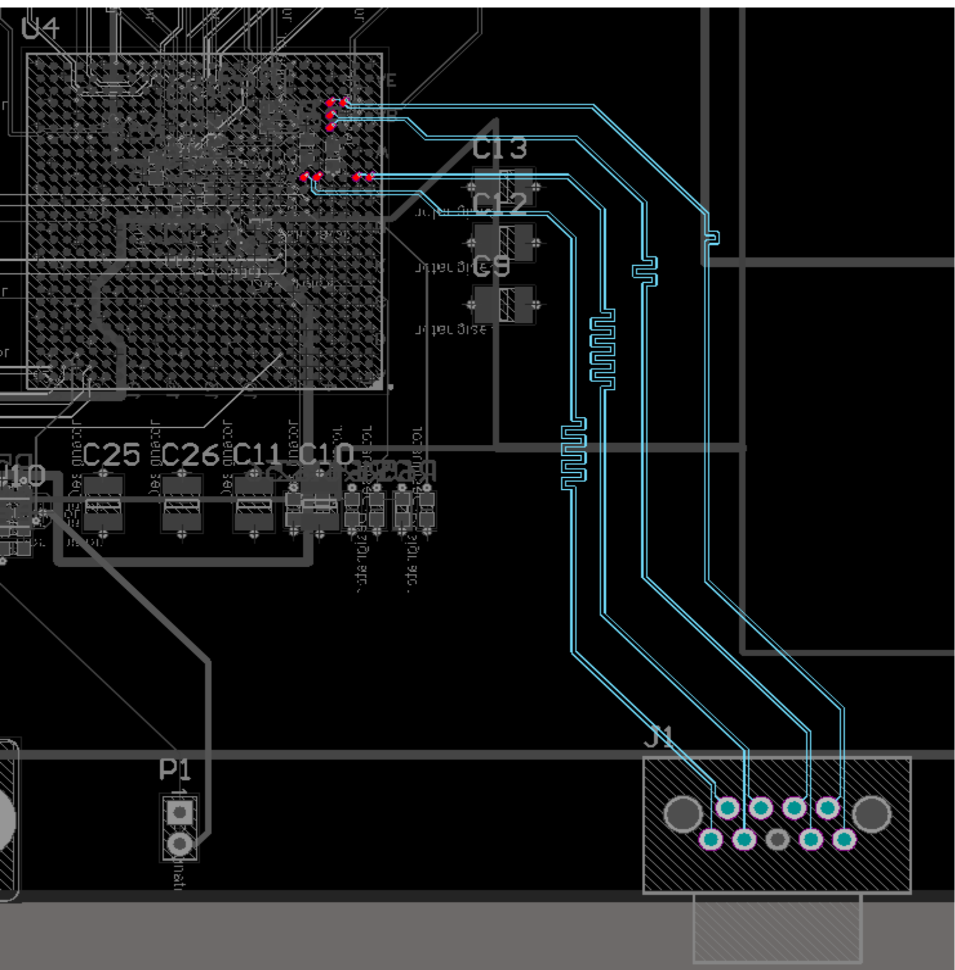


Figure 6.10: Inner Signal 2 showing Output Data Channels going from FPGA to output connector.

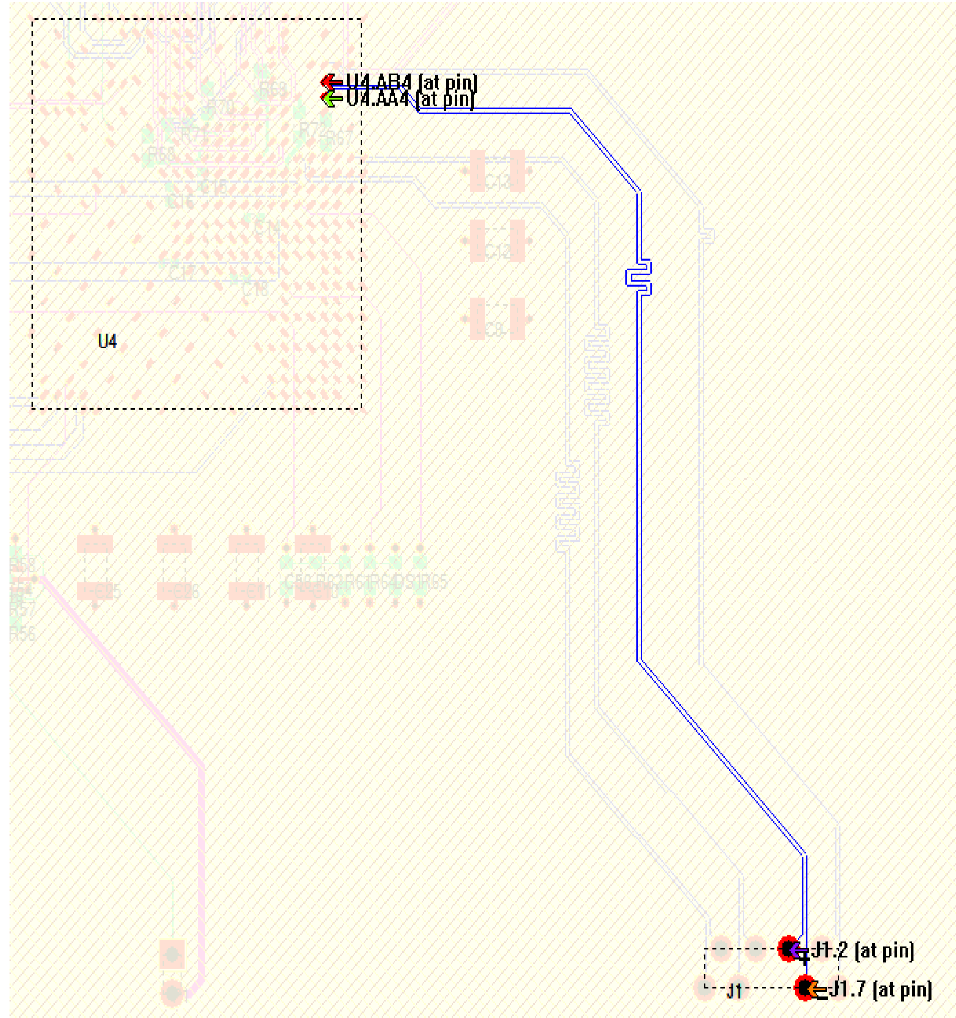


Figure 6.11: FPGA Output Signal Simulation.

Table 6.2 shows the waveform quality and timing results; the eye diagram is also included to analyse the channel performance over a large number of waveforms.

Table 6.2: Simulation results of received waveform at output interface.

CDC FPGA TO CDC Output Connector Waveforms

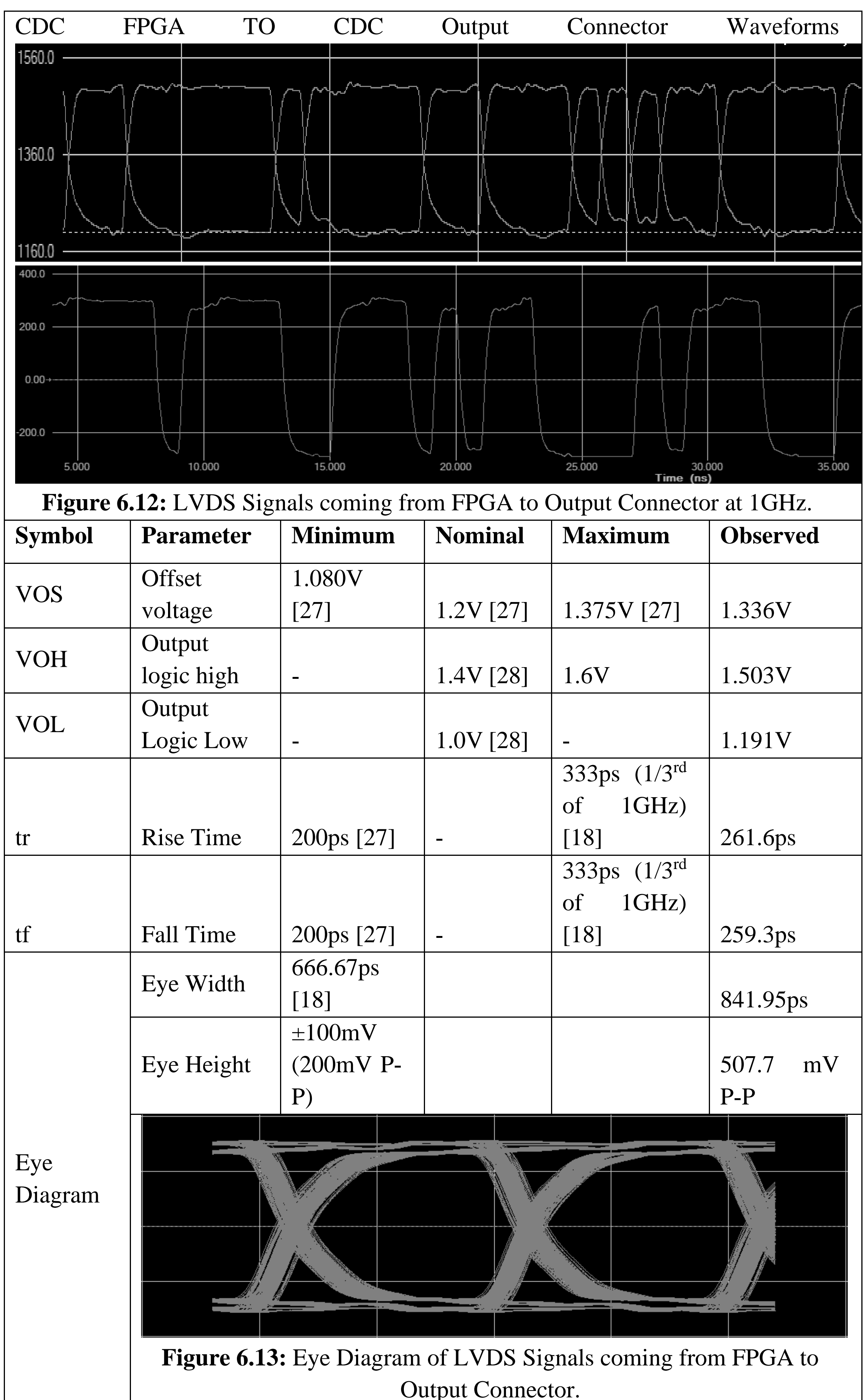


Figure 6.12: LVDS Signals coming from FPGA to Output Connector at 1GHz.

Symbol	Parameter	Minimum	Nominal	Maximum	Observed
VOS	Offset voltage	1.080V [27]	1.2V [27]	1.375V [27]	1.336V
VOH	Output logic high	-	1.4V [28]	1.6V	1.503V
VOL	Output Logic Low	-	1.0V [28]	-	1.191V
tr	Rise Time	200ps [27]	-	333ps (1/3rd of 1GHz) [18]	261.6ps
tf	Fall Time	200ps [27]	-	333ps (1/3rd of 1GHz) [18]	259.3ps
Eye Diagram	Eye Width	666.67ps [18]			841.95ps
	Eye Height	±100mV (200mV P-P)			507.7 mV P-P

Figure 6.13: Eye Diagram of LVDS Signals coming from FPGA to Output Connector.

6.2.1.3 FPGA-PROM Configuration Interface

The Kintex-7 FPGA configuration interface uses the LVCMOS fast slew rate 12 mA standard. This LVCMOS standard has faster edge rates due to which it can support configuration at high frequencies. Due to the faster edge rates it requires more attention to proper termination and PCB trace routing. The configuration clock (CCLK) output should be free from all types of reflections to avoid double-clocking and hence must be routed with the correct routing topology. The interface transmission lines are shown in Figure 6.14 while one each is simulated at a clock rate of 50Mhz. The lines are bidirectional making PROM drivers and FPGA receiver assess how much stripline transmission line distorts the received waveform at either end.

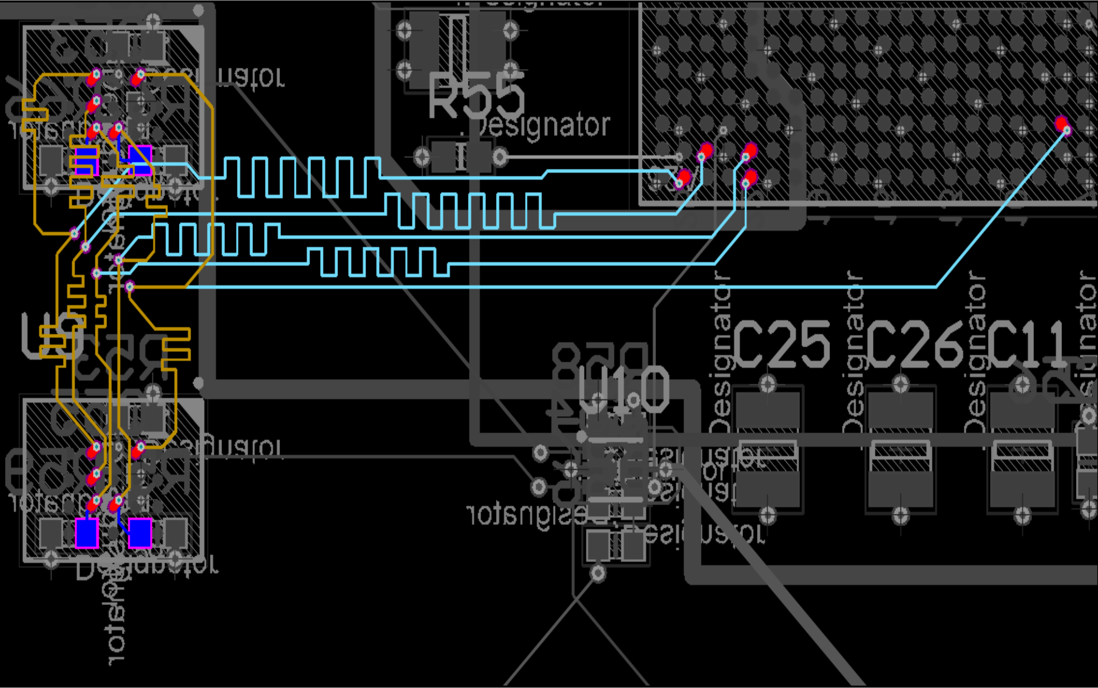


Figure 6.14: Inner Signal 2 showing FPGA Configuration Interface.

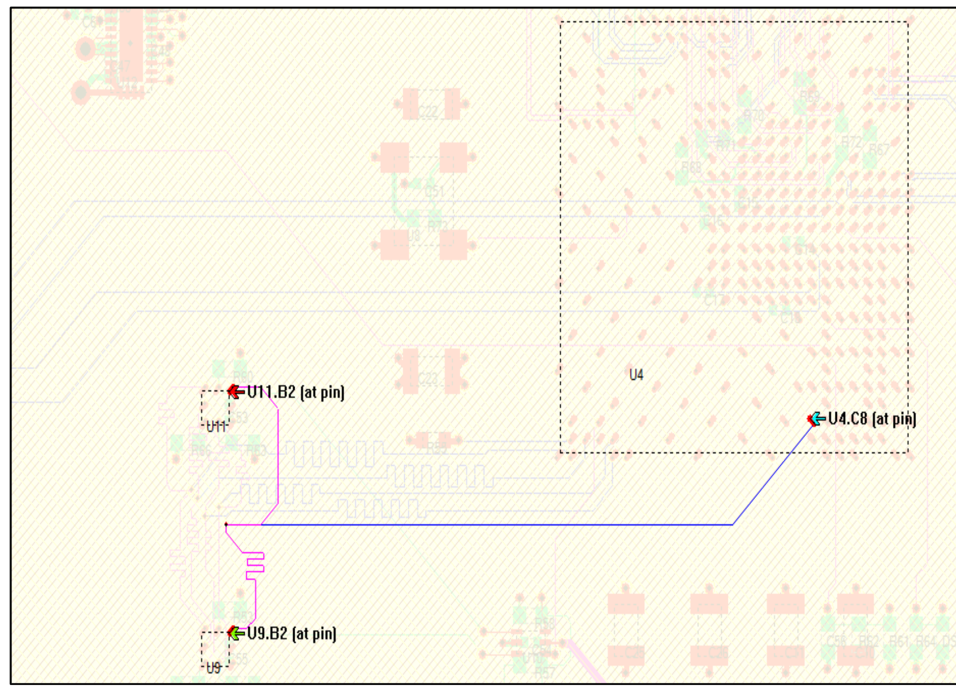


Figure 6.15: FPGA Configuration Interface Simulation.

The typical setup simulation is shown in Figure 6.15. A random waveform is generated from the FPGA end and the received waveforms are observed at both PROM devices. It is worth noting that to achieve integrity of synchronous read and write operations, all the lines are length matched with each other and to the clock line. The simulation results of the configuration interface are tabulated in Table 6.3. All the parameters, including voltage levels, overshoot/undershoot, are under the stipulated limits of the running LVCMOS logic levels.

Table 6.3: FPGA PROM (Configuration) Interface.

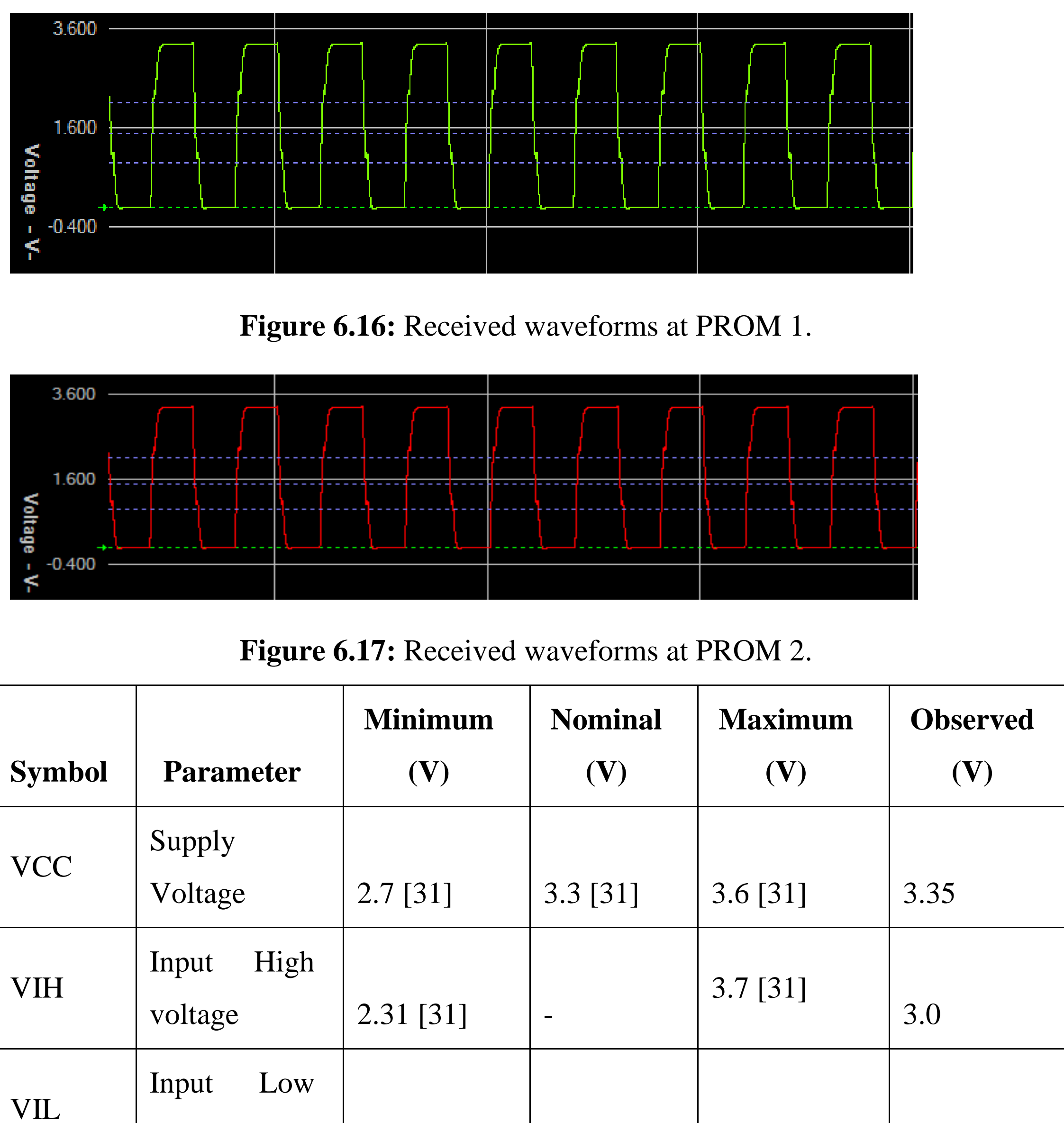


Figure 6.16: Received waveforms at PROM 1.

Figure 6.17: Received waveforms at PROM 2.

Symbol	**Parameter**	**Minimum (V)**	**Nominal (V)**	**Maximum (V)**	**Observed (V)**
VCC	Supply Voltage	2.7 [31]	3.3 [31]	3.6 [31]	3.35
VIH	Input High voltage	2.31 [31]	-	3.7 [31]	3.0
VIL	Input Low Voltage	-0.5 [31]	-	0.99 [31]	0.15

6.2.1.4 Crosstalk analysis

Crosstalk is unwanted interference between the traces switching at high-speed. It occurs when the electromagnetic field lines surrounding a trace influences the other nearby lines in its vicinity. Consequently, this field generates an induced voltage in the victim line. This induced voltage usually degrades the performance of the victim line. The simplest way to avoid crosstalk is to maintain sufficient distance between high-speed traces. [18]

The crosstalk simulation was performed as part of the pre-layout analysis. In light of analysis results it was concluded that trace to trace clearance should be maintained to be

greater than 8 mils because lines with clearance greater than this threshold do not have a noticeable crosstalk effect.

At post-layout level only one case was detected to be having around 20mV of crosstalk. That was due to the several routes accommodated beneath a connector as shown in Figure 6.18. In this case a differential line running at 250mbit/s acts like an aggressor for the passive (stacked low) net and the distance of 8 mils and coupling length of more than 100mil near connector. The simulation is performed to observe the signal at the victim net due to far end crosstalk.

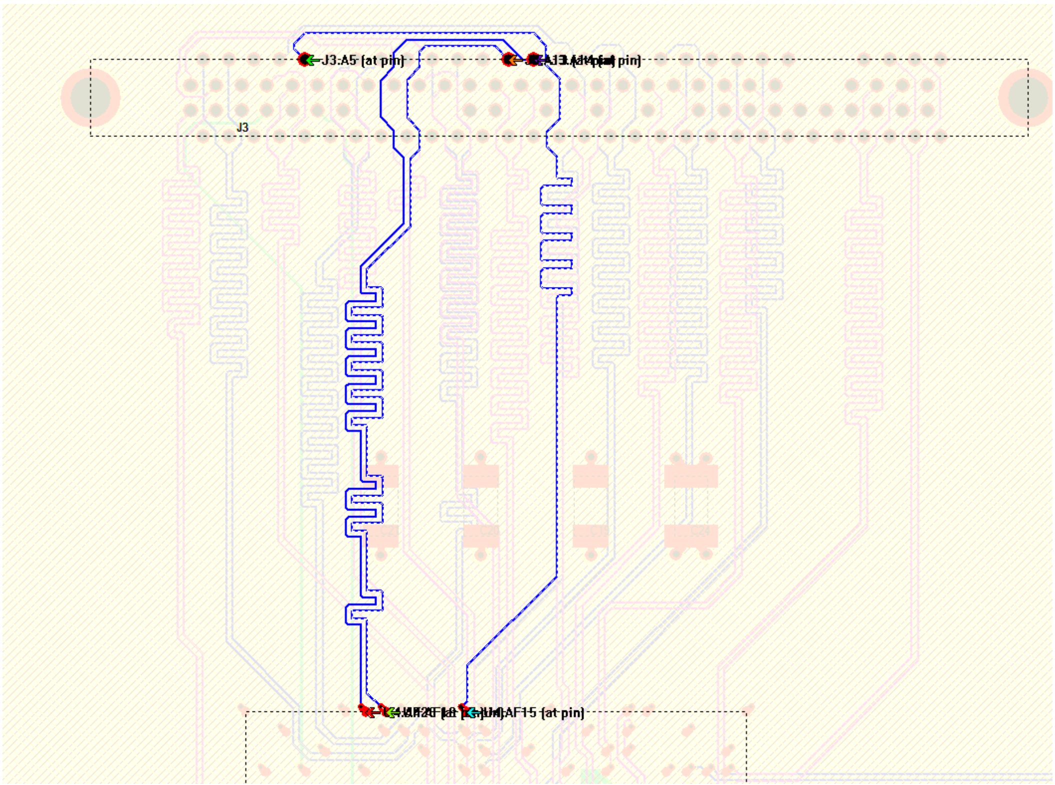


Figure 6.18: Crosstalk Analysis Setup for typical differential interface.

To reduce the crosstalk the clearance is increased to 10 mils. It is observed from analysis results as shown in Figure 6.19 that a very low signal (<10mv) is received at the receiver of the passive line (victim net). This is a negligible value; usually the threshold considered to be unsafe exceed above 50mV.

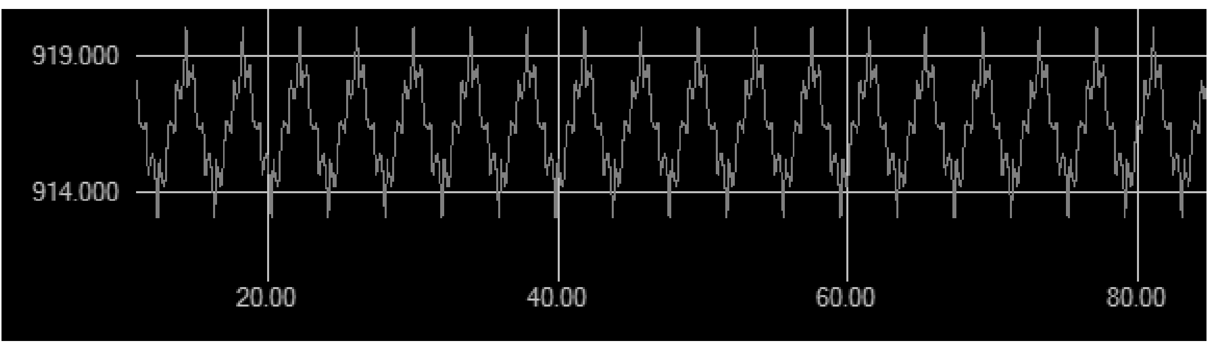


Figure 6.19: Crosstalk results shows a very low signal (<10mV) at 10mil clearance.

6.3 Post Layout Power Integrity Analysis.

The power integrity analysis at pre-layout level was performed to estimate the PWR/GND decoupling analysis. With given parameters including voltage level, worst case load current and allowable ripple factor, the impedance profile was estimated over the stipulated bandwidth. All the capacitors finalized at schematic level were also considered. But a more accurate approximation of the power delivery network is observed after placement and layout. In this case the Hyperlynx post-layout PI not only imports the decoupling capacitors but also the exact geometries of their placement. Similarly, it also picks up the voltage regulator and various sinks with exact placement and models to estimate more accurate model compared to the pre-layout analysis.

6.3.1 Post layout Decoupling Analysis

Decoupling analysis is perfomed to assure the impedence of the power delivery network does not detriorate with increasing freqeuncies. At prelayout level decoupling analysis was performed by taking into account the availible design information at that level. For example all the power supplies have been analyzed for an impedance profile over 100Mhz range with known PWR/GND planes geomatries and decoupling capacitors. The lower threshold was set using load current and ripple percentage. [18]

Post-layout analysis have been performed by importing the finished board with final PWR/GND palne geomatries, VRM and decouping capacitors placement. All these PDN components have been modeled as per parasitics metioned in the manufacturer datasheet. After inclusion of decoupling capacitors in the schematic, the obtained impedance response is shown in Figure 6.20. It can be observed that the plot crosses the target impedance threshold at around 50MHz. It needs to pushed to near 100Mhz for better power delivelry netowork performace.

Therefore a simulation was performed itteratively by adding high-frequency ceramic capacitors to the board near the FPGA pins. After inclusion of couple of 1μf and 100nf capacitors, the plot pushed to 100MHz over the stipulated range of bandwidth to be no more than target impedance. The improved impedance response is shown Figure 6.21.

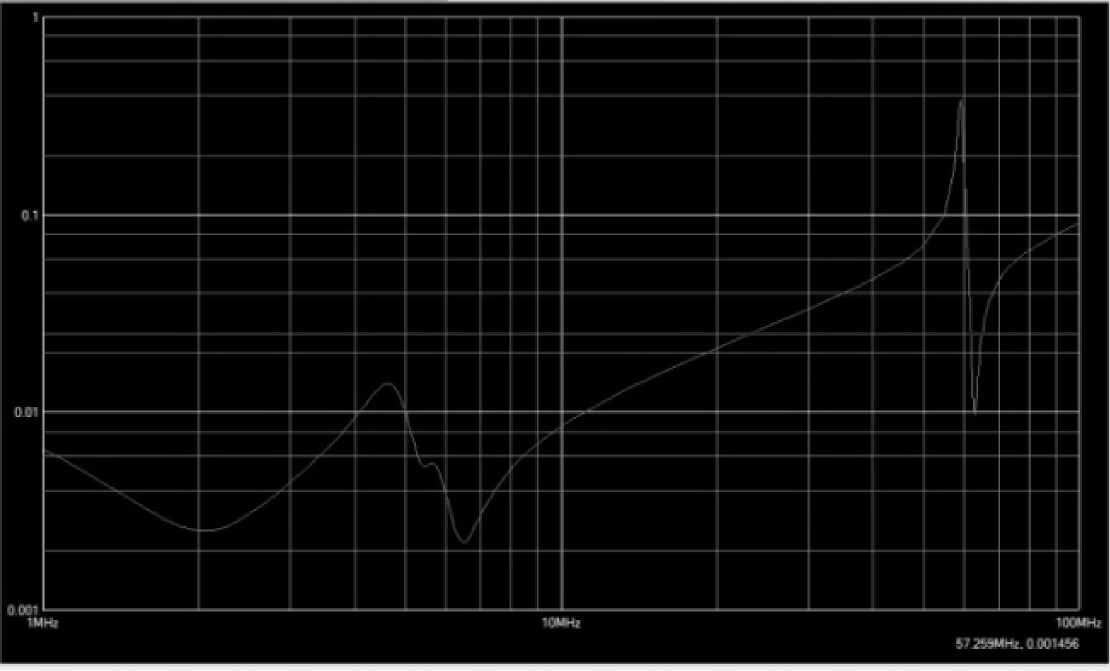


Figure 6.20: Decoupling Analysis of 1V0 FPGA Core Voltage PWR/GND Plane at 50MHz.

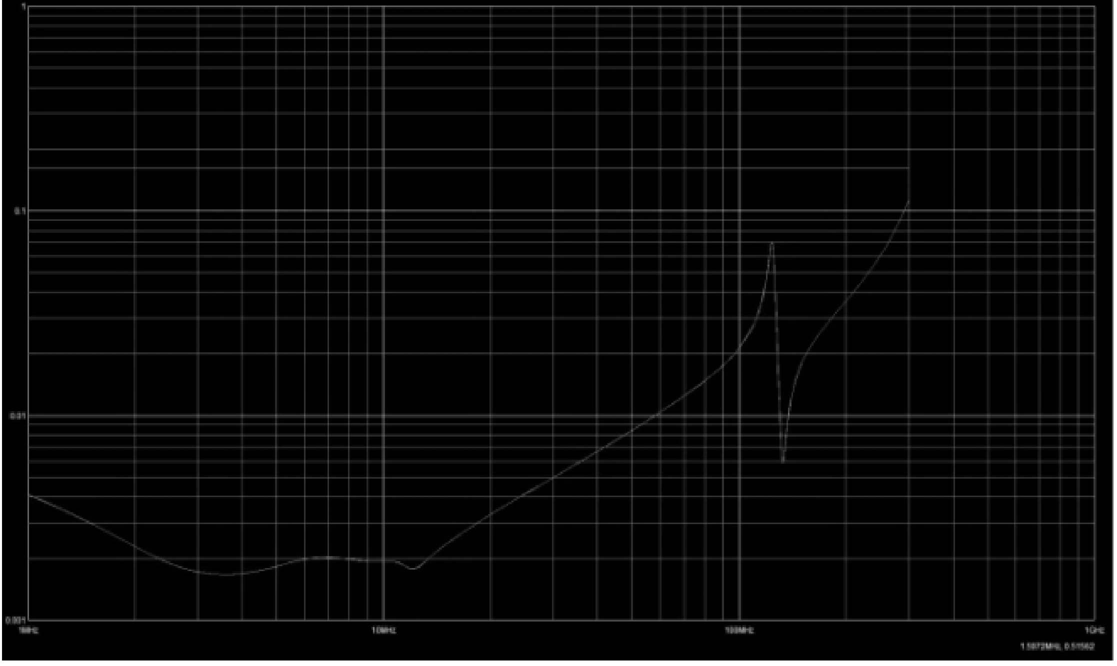


Figure 6.21: Decoupling Analysis of 1V0 FPGA Core Voltage PWR/GND Plane at 100MHz after adding 1μf and 100nF capacitors.

Similarly, for the 1.8V PWR/GND plane it is observed that impedacne plot crosses the threshold at around 70MHz. It clearly meant that existing decaps are able to push it above the threshold over 100MHz bandwidth. By iterative simuation it was observed that by adding couple of 1µf, 2.2µf 100nf and capacitors, the response improved. The improved response is shown in Figure 6.23.

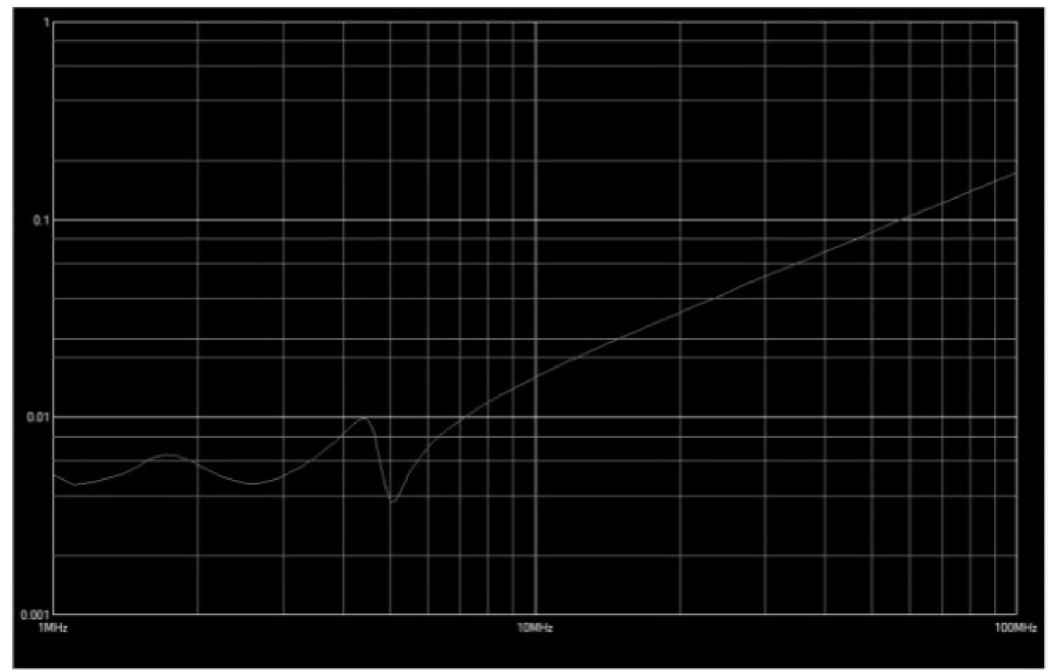


Figure 6.22: Decoupling Analysis of 1V8 FPGA Voltage PWR/GND Plane at 70MHz.

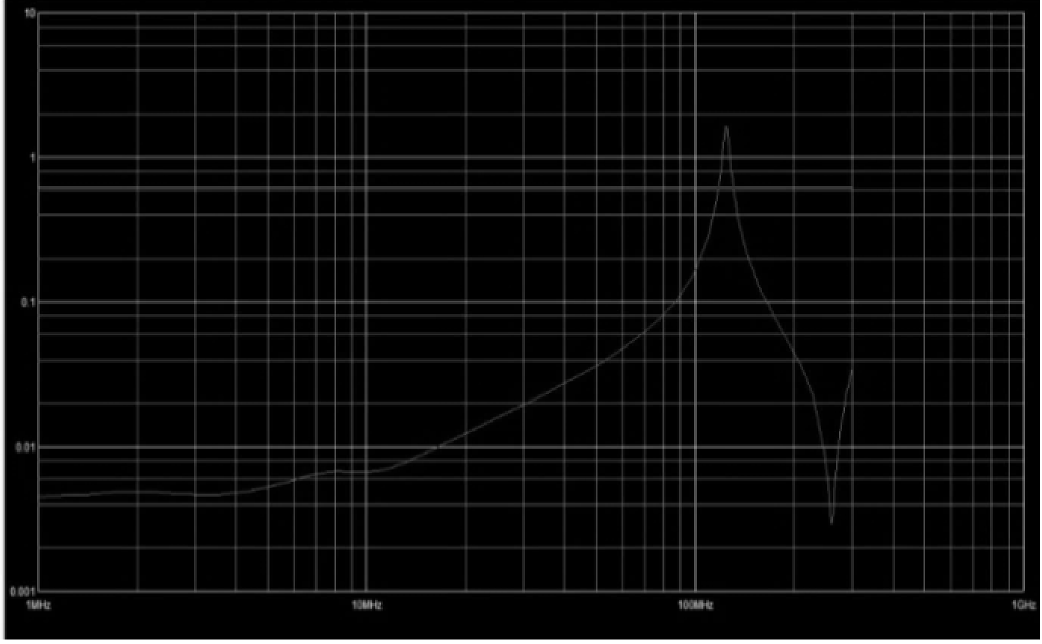


Figure 6.23: Decoupling Analysis of 1V8 FPGA Voltage PWR/GND Plane at 100MHz after adding 1µf, 2.2µf and 100nf capacitors.

6.3.2 DC Drop Analysis

The DC drop analysis is also known as the IR Drop (voltage drop) analysis. The DC drop is a power integrity analysis that includes static power analysis with VRM as a current and voltage sink for each IC. The IR-Drop simulation can be performed using various signal integrity software tools available in market The power integrity DC drop analysis computes the voltage drop, power loss density and current in the power nets. At DC operating conditions, using DC drop analysis can identify how much current is required by the FPGA, ICs, connector pins and Vias (stitching). Because of the excessive voltage drop, the power of the FPGA and ICs may fall below the recommended threshold values. It can also malfunction the FPGA and ICs. Due to excessive current density in the punctured power supply rails these power rails can generate excessive heat, which may lead to board failure due to fusing or delamination. This excessive power can also damage stiching Vias that may lead to connection failures.

Figure 6.24 shows the DC Drop of the 1V power plane. This is core voltage of the main FPGA. The analysis shows that worst case DC drop will be no more than 50mV. The bluish peak in Figure 6.24 shows the peak voltage generated at the output pin of the regulator while reddish area shows this value reduced to 965mV when reaching the pins of the FPGA depicted as the downward dip in Figure 6.24. This is minumum voltage with worst case drop, which is around 940mv, greater then required voltage, i.e. 900mV.

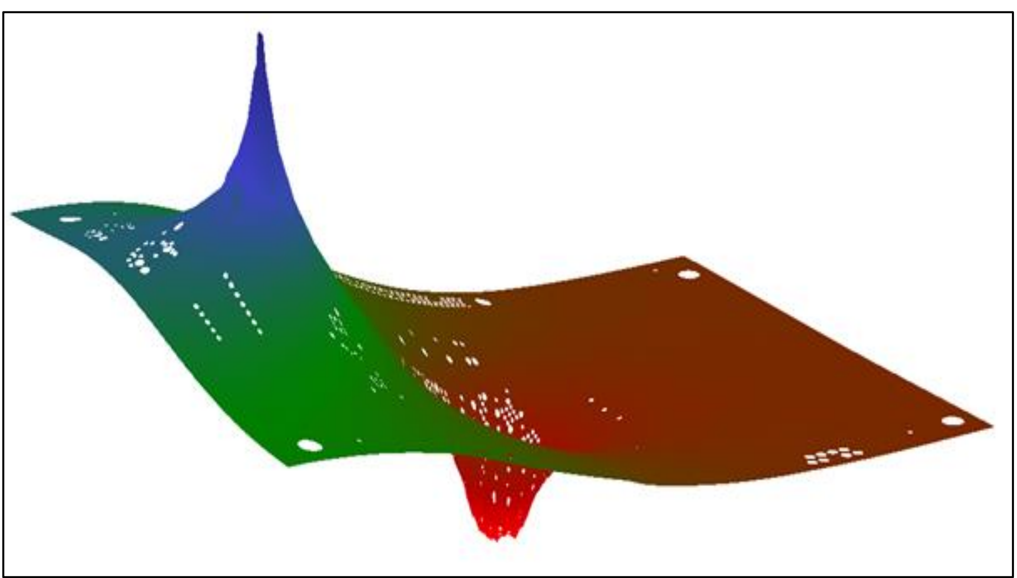


Figure 6.24: DC Drop Analysis of 1V0 Supply.

Similarly the DC drop of the 3.3V power plane is shown in Figure 6.25, though this plane is sourcing some other ICs along with FPGA but, maximum load is sinked by FPGA (more than 2A) for running 3.3V I/O Banks. The minumum point of voltage value in this line is at the FPGA pins where it is around 3208mV greater than the threshold (3100mV).

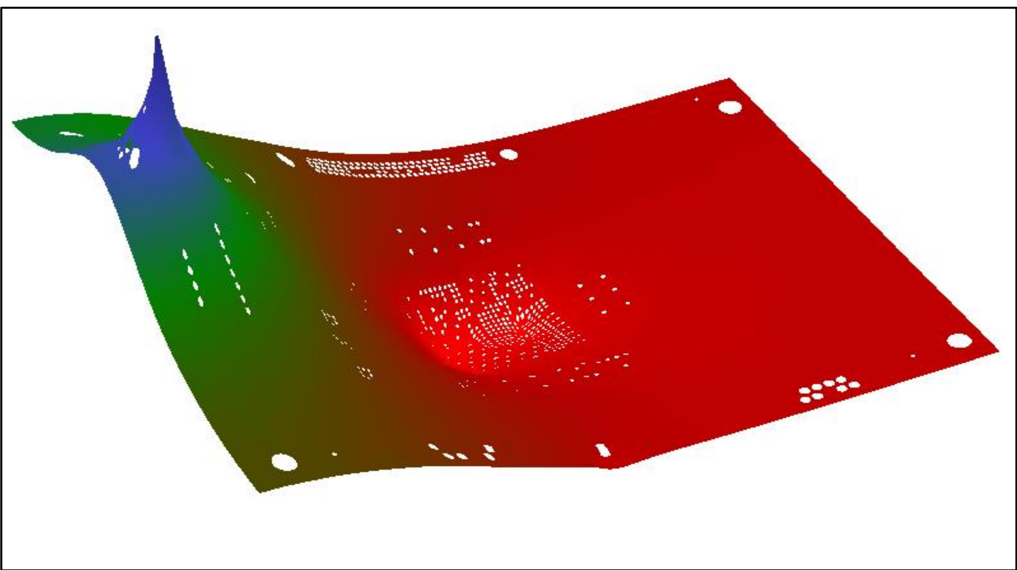


Figure 6.25: DC Drop Analysis of 3V3 Supply.

7 Comparison, Conclusion and Recommendations

7.1 Pre-Layout & Post Layout SI/PI Analysis Comparison

The observations at post-layout are comparable to pre-layout except for some minor differences. For example, the eye width is degraded a bit more as compared to pre-layout, similarly eye height is also degraded from 732mV and the data output interface is observed to be at 618mV but at post-layout it is observed to be 507mV. Similarly, pre-layout crosstalk results have been validated and improved at post-layout level. Altogether the analysis results are nominal and fall within the stipulated range of signalling standards. Simlarly pre-layout power integrity decoupilng results were apparently promising, but when exact geometries of power planes, components and decaps are included in the post-layout level, it is observed that the resonance point of the impedance curve shifted to a lower value than was observed in pre-layout. Therefore, to mitigate this, some high-frequency capacitors are added to get at least 100Mhz bandwidth, which is lower than the target impedance.

7.2 Conclusion

The work being presented covered the design and analysis of a complete on-board FPGA-based system design to cater for the data processing requirements of high throughput satellites. Due to the high throughput requirement of payload input and output interfaces, each interface is analysed to have a stable signal and power integrity performance. All the high-speed interfaces have been designed to have minimum crosstalk so that functionality of any other traces or packages may not be affected by nearby lines switching at high-speed. Crosstalk assurance essentially provides the board-level EMC compliance. The design and analysis flow presented is cost effective because it predicts the board level performance using available simulation tools. This essentially avoids iterative hardware prototyping, thereby reducing cost and development time.

7.3 Recommendations for Future Work

Space borne satellite application are continuously demanding higher bandwidth to cater for ultra-high-speed data acquisition, processing and transmission. The inherent electromagnetic effects due to such high edge rates become more challenging for hardware designers. In this work board level SIPI issues are identified and mitigated. In future work the SIPI analysis shall be performed in conjunction with the board level and system level the conducted emissions and radiated emissions analysis will also be performed, which will not only enable a better SIPI analysis but will also accurately predict the system level EMI/EMC compliance at an early design stage. This will again reduce the number of tedious hardware prototyping and testing levels. Consequently, significant development cost and time would be saved in overall system development.

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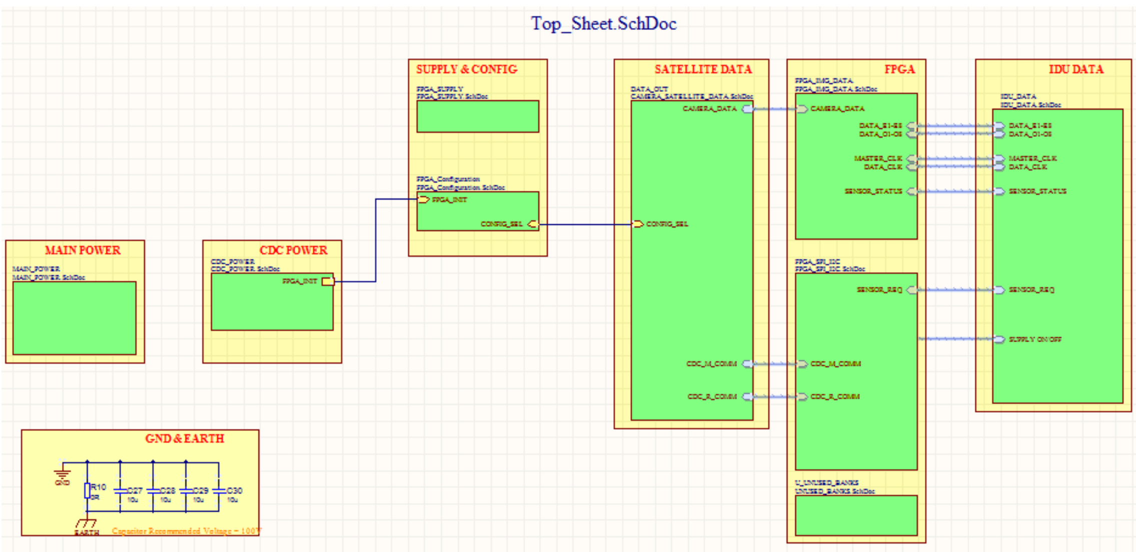
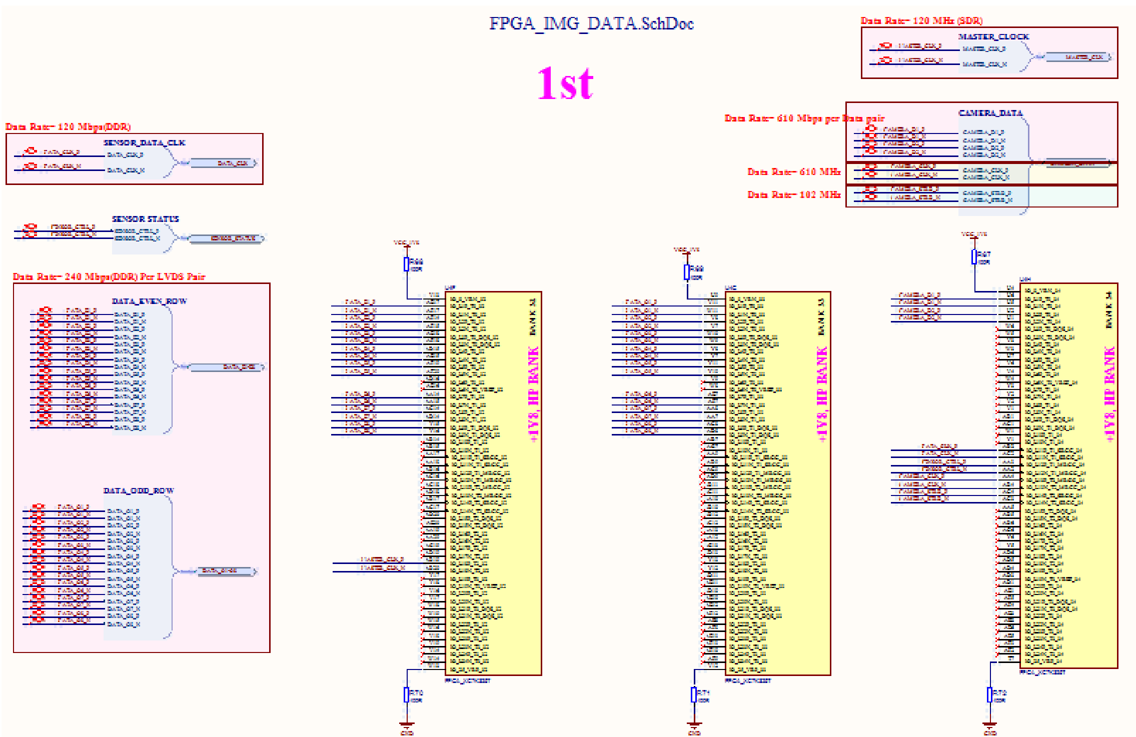
APPENDICES

APPENDIX 1: CDC SCHEMATICS

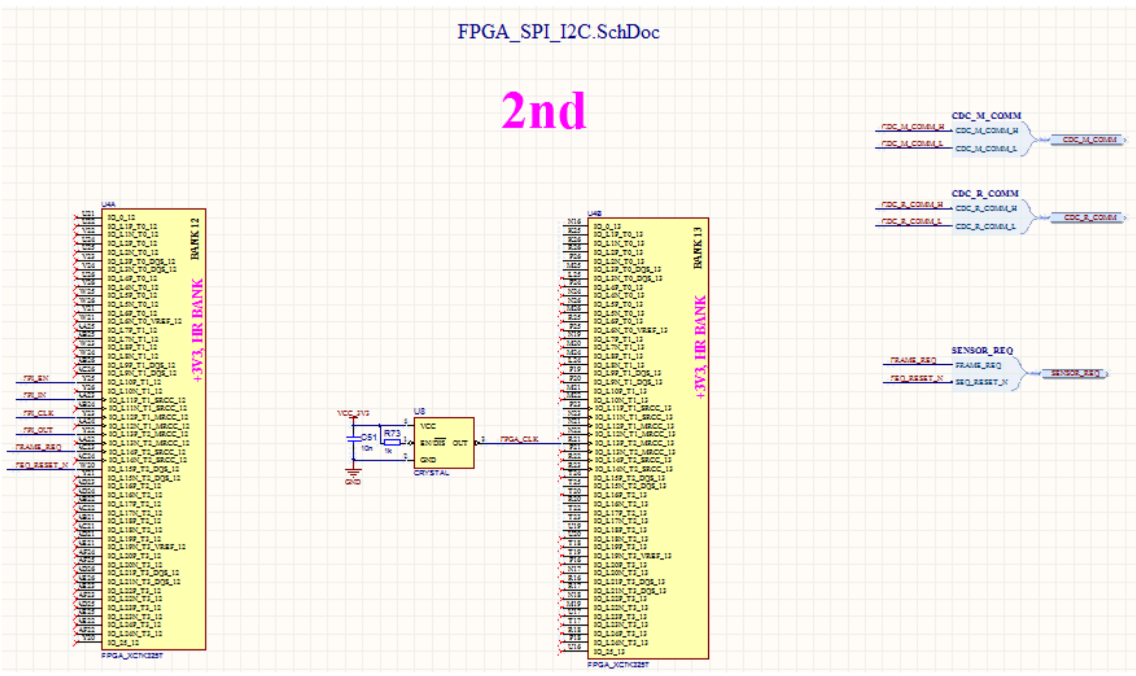
TOP SHEET



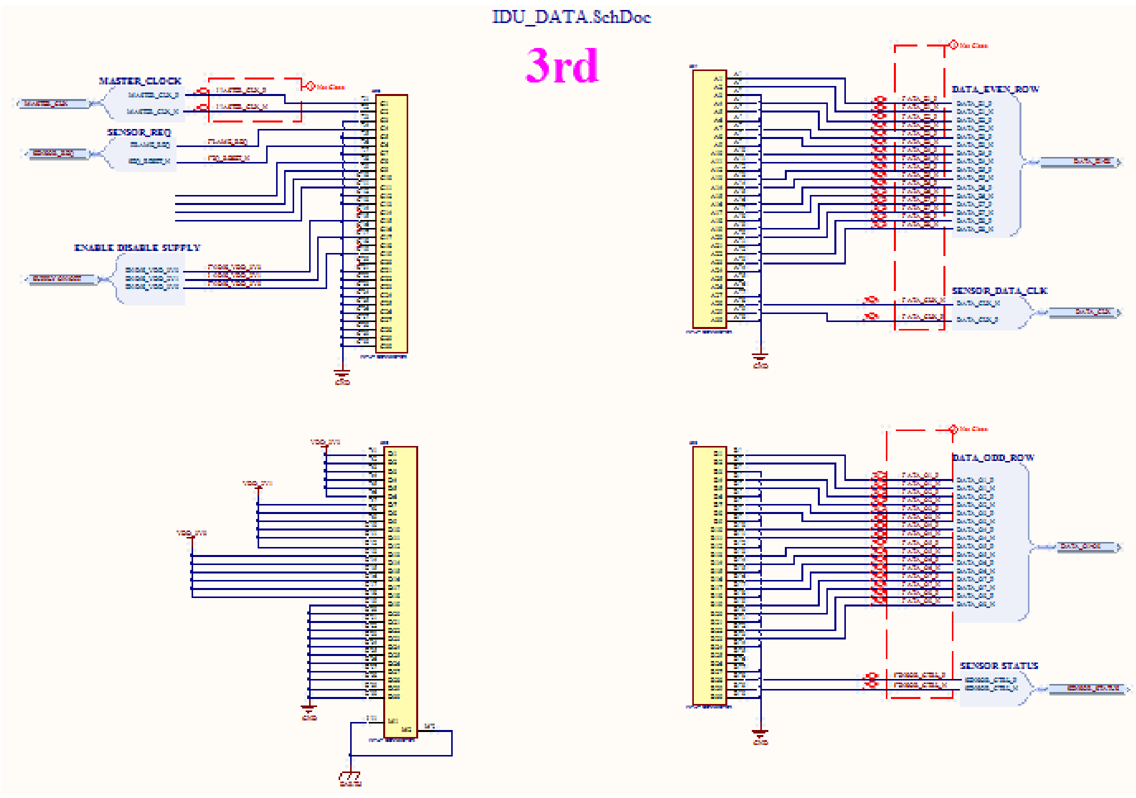
FPGA IMAGE DATA



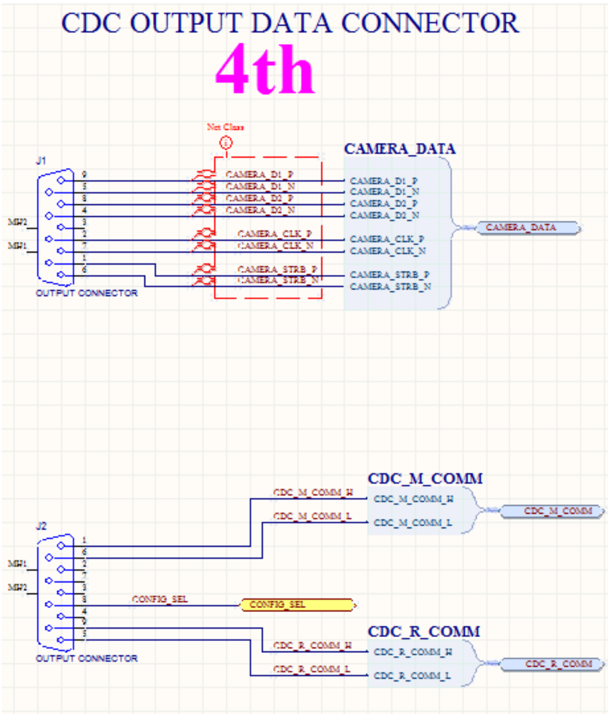
FPGA SPI I2C COMMUNICATION



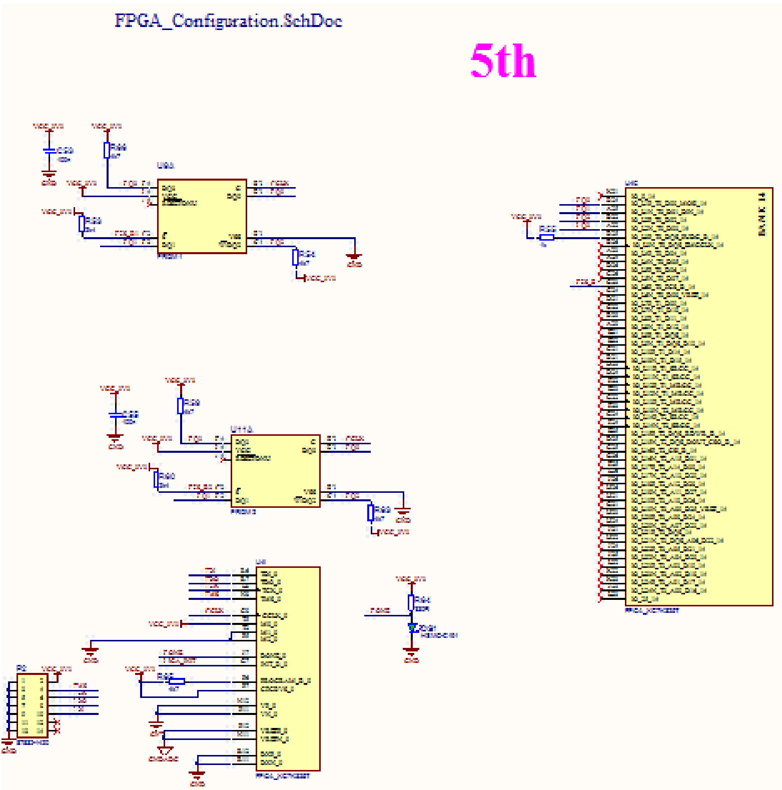
IDU DATA CONNECTOR



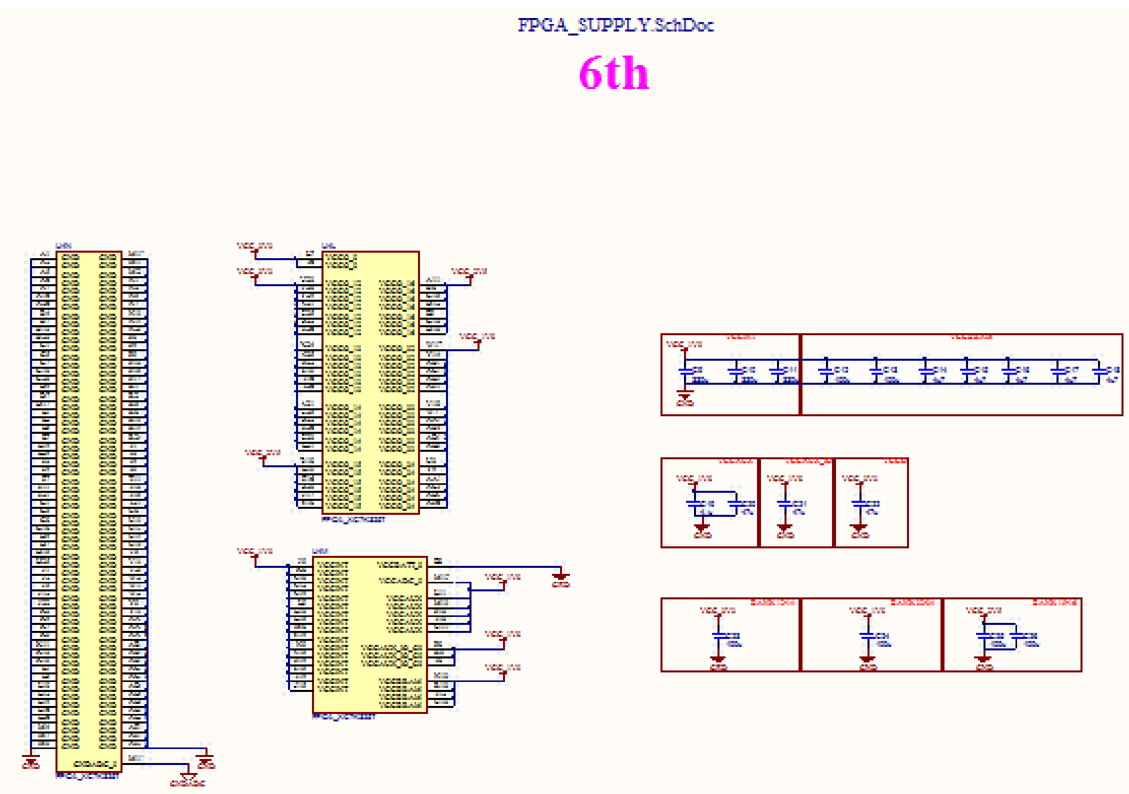
CDC OUTPUT DATA CONNECTOR



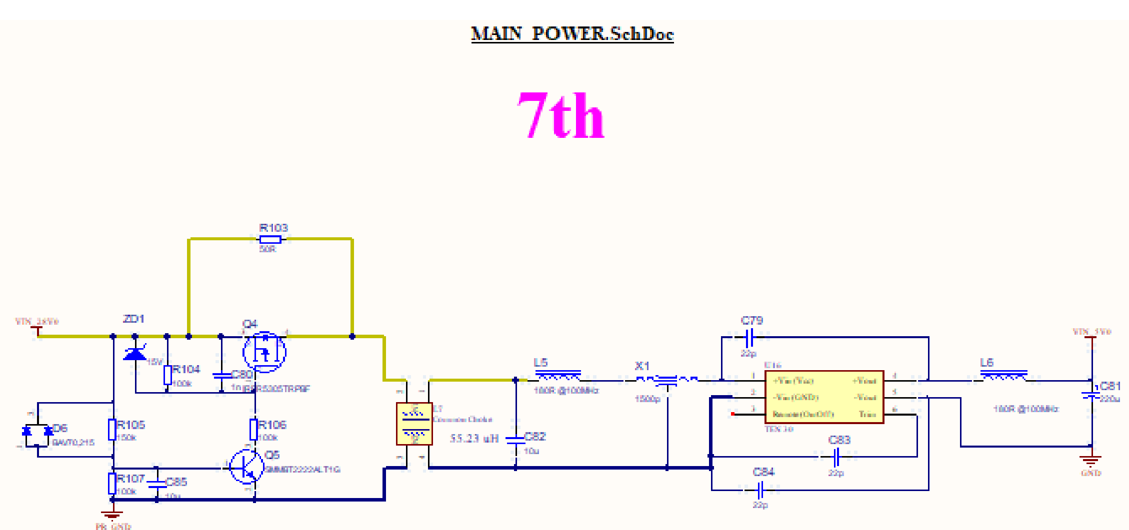
FPGA CONFIGURATION



FPGA SUPPLY

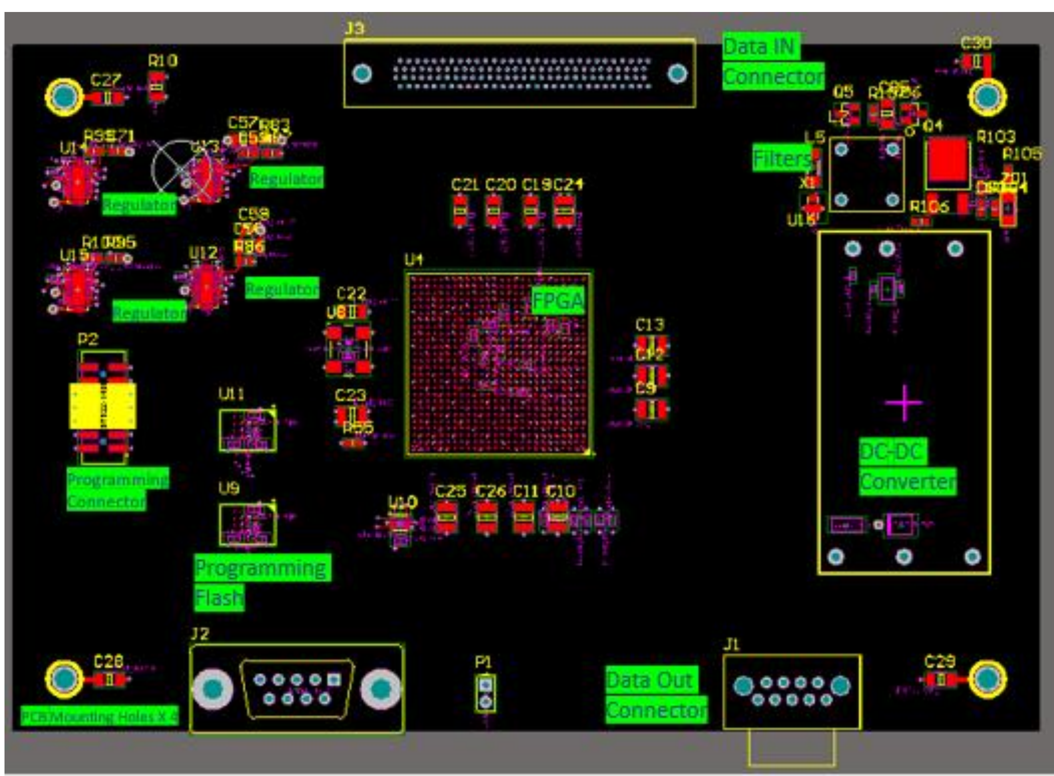


MAIN POWER SUPPLY

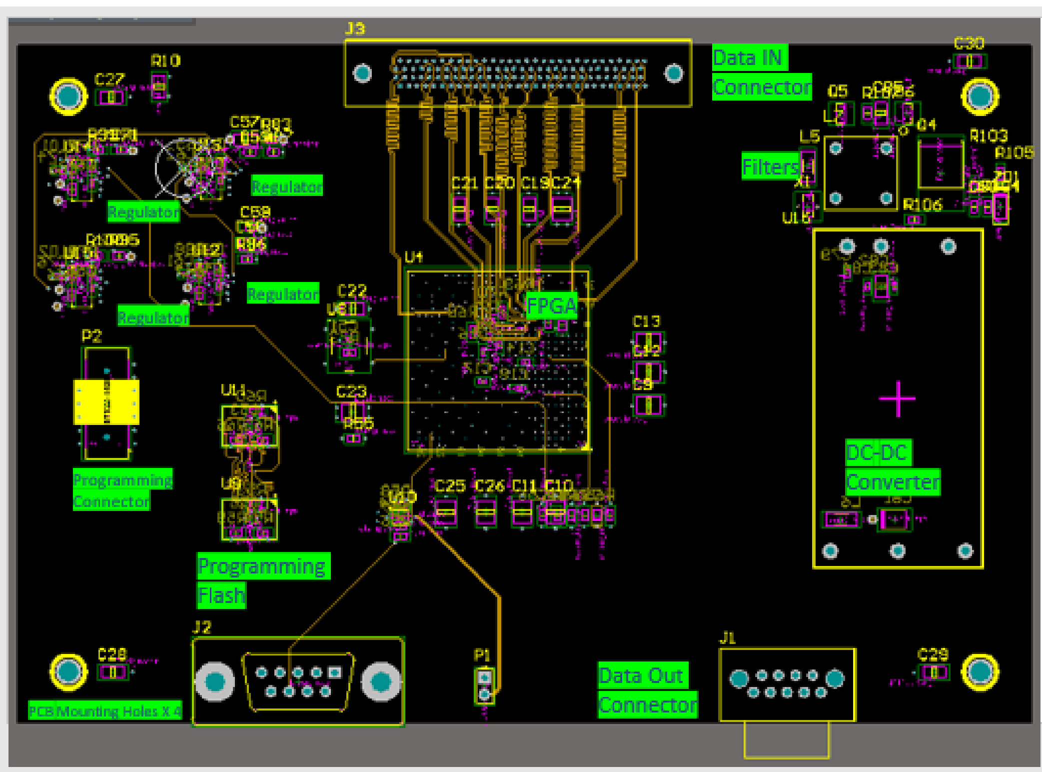


APPENDIX 2: CDC PCB

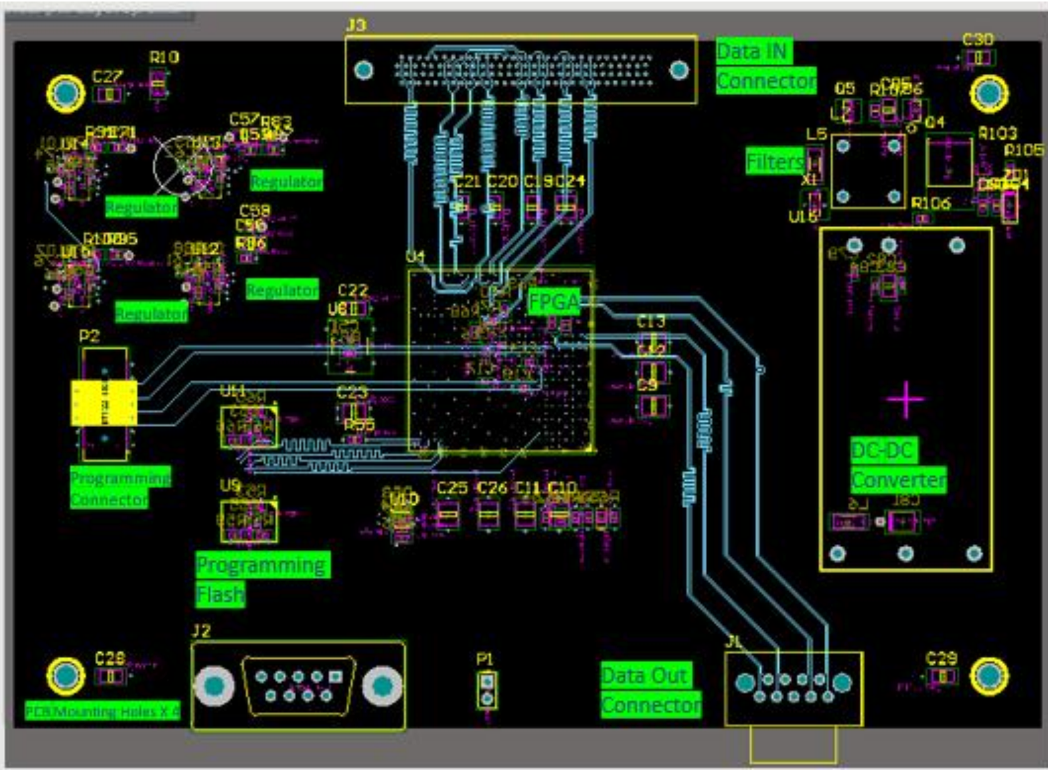
TOP LAYER



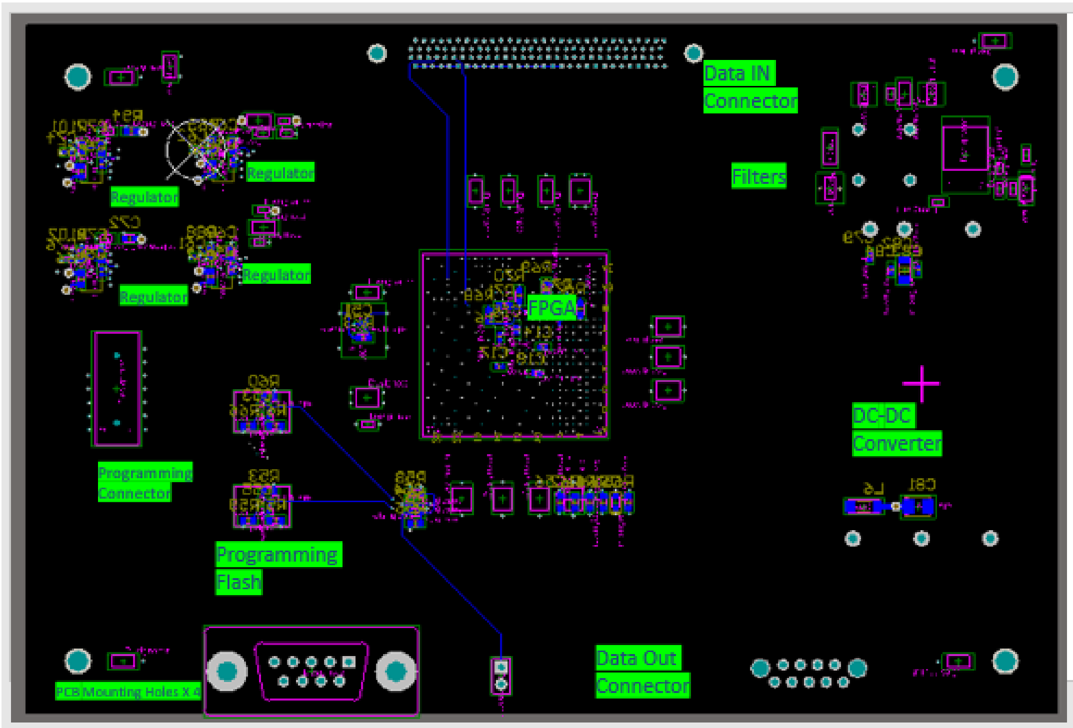
INNER SIGNAL 1



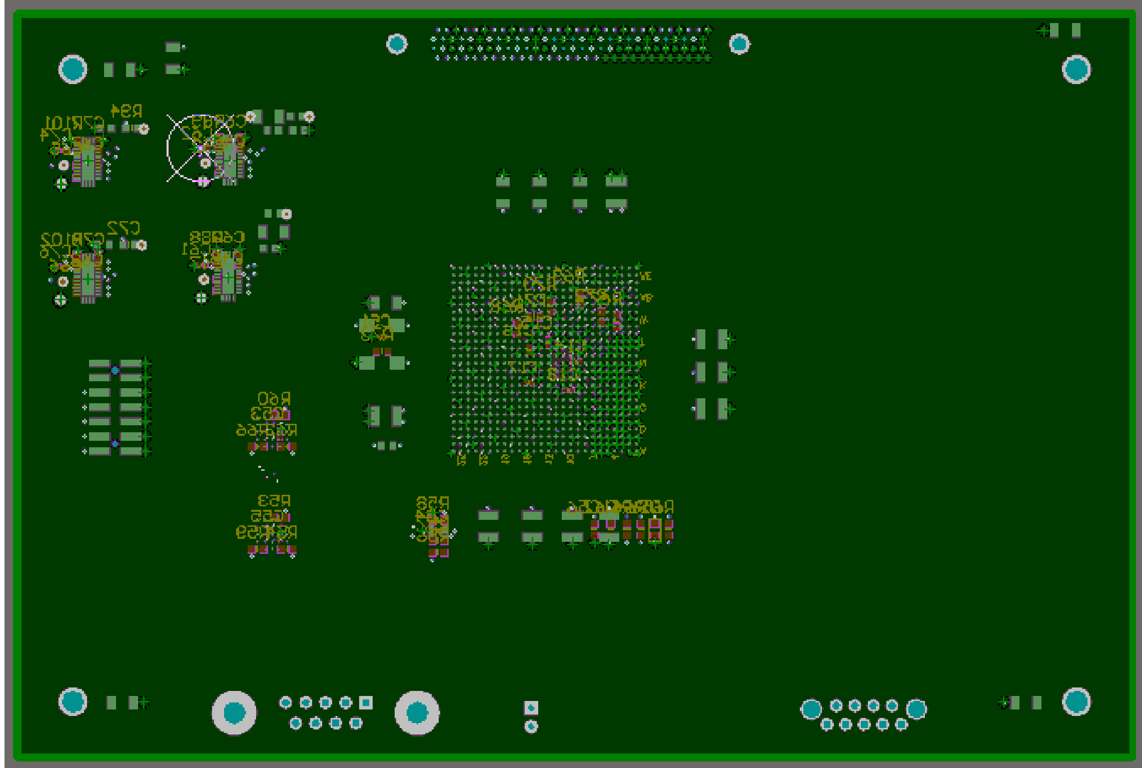
INNER SIGNAL 2



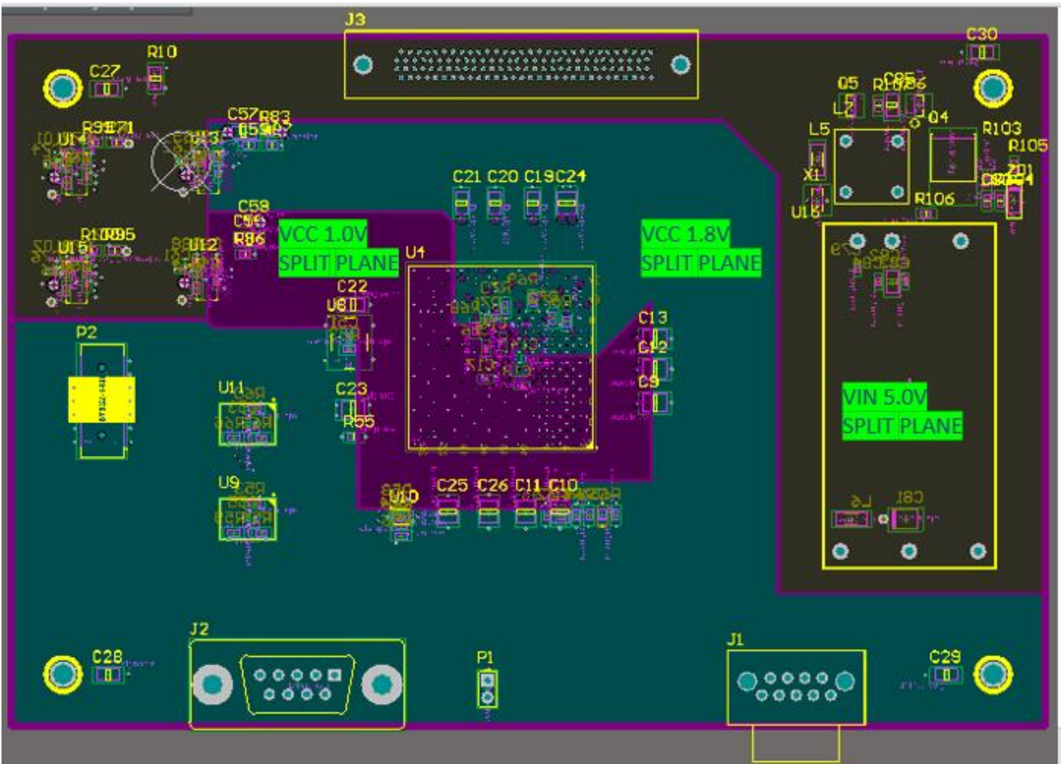
BOTTOM LAYER



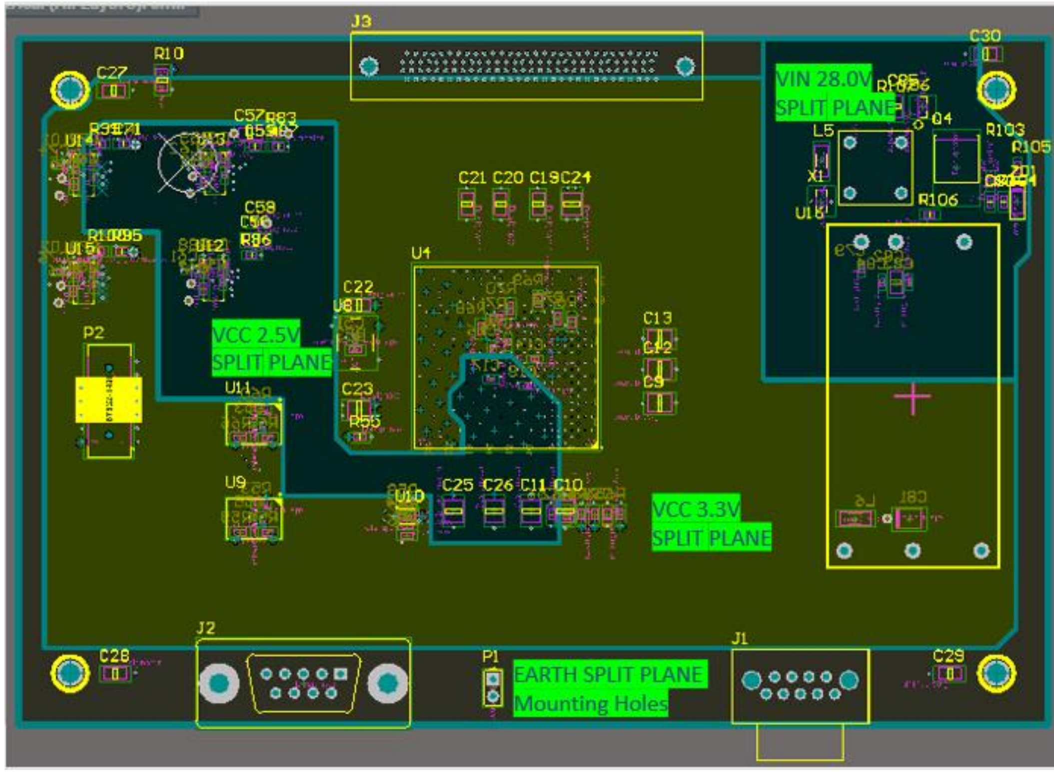
GROUND 1



SPLIT PLANE 1



SPLIT PLANE 2



GROUND 2