THE DESIGN AND IMPLEMENTATION OF A WIDEBAND DIGITAL RADIO RECEIVER

Dissertation for the Degree of Master of Science
in Engineering

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Declaration

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering at the University of Cape Town. It has not been submitted before for any degree or examination at any other university.

Signed by candidate

Signature of Author .....

Cape Town
28 March 2002

Abstract

Historically radio has been implemented using largely analogue circuitry. Improvements in mixed signal and digital signal processing technology are rapidly leading towards a largely digital approach, with down-conversion and filtering moving to the digital signal processing domain. Advantages of this technology include increased performance and functionality, as well as reduced cost.

Wideband receivers place the heaviest demands on both mixed signal and digital signal processing technology, requiring high spurious free dynamic range (SFDR) and signal processing bandwidths. This dissertation investigates the extent to which current digital technology is able to meet these demands and compete with the proven architectures of analogue receivers. A scalable generalised digital radio receiver capable of operating in the HF and VHF bands was designed, implemented and tested, yielding instantaneous bandwidths in excess of 10 MHz with a spurious-free dynamic range exceeding 80 decibels below carrier (dBc).

The results achieved reflect favourably on the digital receiver architecture. While the necessity for minimal analogue circuitry will possibly always exist, digital radio architectures are currently able to compete with analogue counterparts. The digital receiver is simple to manufacture, based on the use of largely commercial off-the-shelf (COTS) components, and exhibits extreme flexibility and high performance when compared with comparably priced analogue receivers.

Acknowledgements

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List of Abbreviations

ADC— Analogue-to-digital converter

AGC— Automatic gain control

ASIC— Application-specific integrated circuit

cf— Characteristic function

CIC— Cascaded integrator-comb

COTS— Commercial off-the-shelf

CPLD— Complex programmable logic device

DAC— Digital-to-analogue converter

dBc— Decibels relative to carrier

dBFS— Decibels relative to full-scale

DDC— Digital down-converter

DDS— Digital signal synthesis

DF— Direction finding

DFT— Discrete Fourier Transform

DMA— Direct memory access

DNL— Differential non-linearity

DUT— Device under test

FFT— Fast Fourier Transform

FIR— Finite impulse response

FPGA— Field-programmable gate array

FSR— Full-scale range

IF— Intermediate frequency

IM3— Third-order intermodulation products

INL— Integral non-linearity

IP3— Third-order intercept point

ISA— Industrial Standard Architecture

LO— Local oscillator

LSB— Least significant bit

MDS— Minimum discernable signal

MGC— Manual gain control

MSB— Most significant bit

NCO— Numerically controlled oscillator

NSD— Non-subtractive dither

pdf— Probability density function

RPDF— Rectangular probability density function

SBC— Single board computer

SD— Subtractive dither

SDR— Software defined radio

SIMD— Single instruction multiple data

SINAD— Signal-to-noise-and-distortion

SFDR— Spurious-free dynamic range

SNR— Signal-to-noise ratio

SSB— Single side band

TDOA— Time difference of arrival

Nomenclature

Band Occupancy— The band occupancy is usually expressed as a percentage and is defined as the ratio of the number of signals present within a particular band-of-interest to the number of available channels allocated to the band.

Noise Factor— The noise factor (NF) provides a measure of the contribution of inherent (internal) device noise on total system noise. It is defined as the ratio of the signal-to-noise ratio (SNR) measured at the device output and the SNR ratio measured at the device input under normal operating conditions. By convention, it is expressed in a dB scale.

Selectivity—The property of a receiver that allows it to distinguish between signals at different frequencies.

Sensitivity—For sufficiently high levels of receiver gain, the weakest signal power that may be acceptably processed is limited by noise. This signal level is referred to as the sensitivity of the system and varies with external noise level.

Spurious Free Dynamic Range (SFDR)—The ratio of the peak RMS signal amplitude to the RMS value of the peak spurious spectral component. This may or may not be a harmonic. It is usually expressed in decibels relative to carrier (*dBc*) or decibels relative to full scale (*dBFS*), and it is therefore important to pay attention to the units of measurement.

Chapter 1

Introduction

Digital radio implementations are increasingly being adopted. Analogue circuitry is rapidly being replaced by digital signal processing (DSP), analogue-to-digital (A-D) and digital-to-analogue (D-A) conversion. Advantages of this technology include increased performance and functionality, and reduced cost. Dedicated analogue circuitry may be replaced by flexible, robust DSP application-specific integrated circuits (ASICs) and software.

Analogue-to-digital conversion technology currently limits the instantaneous energy that may be received, as a result of limited A-D converter dynamic range. If the received energy is widely distributed over the received spectrum (usually a valid assumption given the typical energy spread in the bands of interest), the bandwidth that may be received at any given level of available dynamic range is limited. Continuous technological advances move closer to the ideal of connecting an A-D converter (ADC) directly to a bandwidth-limited antenna, and directly sampling wide RF spectra with sufficient dynamic range to permit the demodulation of narrowband channels using digital signal processing hardware and software. Digitisation of the entire HF spectrum (2-30 MHz) has recently become feasible, with state-of-the-art A-D converters currently capable of sampling rates of up to 105 MSPS at 14 bit resolution. Digital signal processing hardware and algorithm speeds, once considered an impediment to the digitisation of wideband data, continue to advance and are currently capable of performing advanced signal processing tasks, such as adaptive equalisation, which are difficult or impossible to implement in the analogue domain.

This dissertation explores the digitisation and frontend digital signal processing of the HF and VHF spectra for the purposes of wideband radio reception.

1.1 Background

A well-documented history of communications receivers can be found in Rohde *et al.* [23]. The development of the superheterodyne-type receivers revolutionised receiver design, relegating previous receiver architectures to occasional, special-purpose use. The superheterodyne architecture is not without problems, however. The use of mixers to perform frequency translation introduces the associated problems of image frequency rejection, IF leak-through and high order non-linearities. Local oscillator (LO) noise sidebands may be translated to the IF by a strong out-of-band signal (usually a strong adjacent channel), a process termed *reciprocal mixing*[23]. Phase imbalance between in-phase and quadrature channels significantly limits performance in analogue quadrature channel conversion[27].

The advantages of a digital receiver solution are significant, and include reduced system cost, increased temperature stability, finer tuning resolution, faster tuning speed, excellent quadrature channel phase balance, increased filter selectivity, robustness in terms of both hardware and software signal processing algorithms, reconfigurability, advanced signal processing techniques and the ability to store signals for subsequent off-line processing.

These benefits have resulted in the digitisation process moving closer to the RF frontend, with the ultimate goal of directly digitising the antenna output. The "Software Defined Radio" (SDR) has recently been realised, allowing reconfiguration of signal processing functions through software, and resulting in reconfigurable radios capable of operating over multiple air interfaces.

Figure 1.1 illustrates the progression of receivers in recent years. Initially, the limited sample rates of A-D converters and limited digital signal processing power precluded the use of digital hardware beyond baseband signals. With recent improvements in A-D conversion and digital signal processing hardware, sampling and processing of wideband IF signals has become a reality. Digital down-conversion has facilitated the elimination of analogue down-conversion and quadrature conversion stages. It is likely that future digital and mixed signal technology will soon supersede the superheterodyne architecture completely, directly sampling bandlimited RF signals.

1.2 Scope

This dissertation is an investigation and evaluation of state-of-the-art wideband digital radio receiver hardware through the design, implementation and qualification of a scalable multi-channel IF-input wideband digital radio receiver. A survey of digital

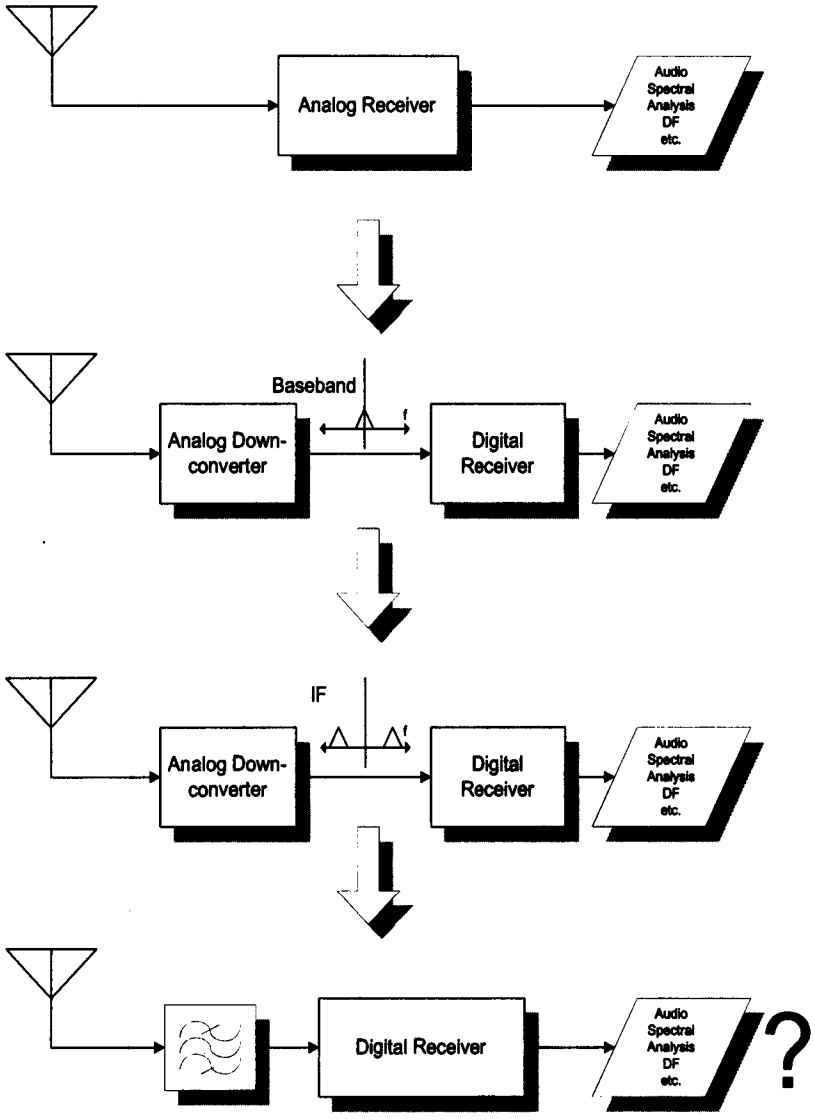

Figure 1.1: The progression of receivers from analogue to digital

radio receiver architectures and relevant theory is conducted. Simulations and empirical investigations are performed. A general-purpose wideband digital receiver capable of operating in the HF and VHF bands is proposed and implemented. The receiver is quantitatively evaluated, after which conclusions on receiver performance and future trends in wideband digital radio architectures are drawn.

The design, implementation and qualification of the general-purpose receiver spans a two-year period during which the author was solely responsible for the design, testing and integration of digital receiver hardware and driver-level software in numerous systems.

1.3 System Specification

The design goal for the system is to realise a highly reconfigurable digital receiver using commercial-off-the-shelf (COTS) components where possible.

- The receiver should be capable of functioning as a backend to wideband and narrowband analogue down-converters.
- It should be capable of digitising the intermediate frequency (IF) output of analogue down-converters with output bandwidths of up to 10 MHz, at IF's in the HF and VHF bands.
- The receiver should accept full scale single-ended analogue input signal levels of ca. 0 dBm, with allowance for fixed amplification of 20 dB. It is presumed that any dynamic analogue receiver gain (manual or automatic gain control) that may exist is included in the analogue down-converter.
- The receiver is required to support wideband down-conversion, baseband filtering and rate reduction in hardware.
- It should further support the extraction of narrowband signals from the wideband input for the purpose of real-time demodulation.
- The system should be scalable, supporting multiple receiver channels.
- It should contain flexible sampling and synchronisation circuitry to support phase-synchronous data acquisition on multiple channels, a prerequisite in applications such as wideband direction finding (DF) and beamforming.

The required modes of operation are presented in table 1.1.

Sampling Frequency	IF	Input Bandwidth	Output Bandwidth	SFDR	Maximum Channel Count
51.2 MSPS	5.0 MHz	800 kHz	800 kHz	80 dBc	5 (synch)
51.2 MSPS	12.8 MHz	10 MHz	10 MHz	75 dBc	6 (synch)
51.2 MSPS	5.0 MHz	500 kHz	11 kHz	80 dBc	12 (asynch)

Table 1.1: Wideband receiver operating mode requirements

1.4 System Architecture

The receiver implementation consists of one (single antenna) or more (multiple antenna) wideband receiver channels implemented on full-length PC ISA adapter cards and mezzanine modules and mounted in a ruggedised industrial computing rack. A commercially available industrial Single Board Computer (SBC) housing single or dual Intel Pentium processors with 100 Mbit ethernet support forms the main system controller and high-performance back-end processor for the system. It further allows the system to act as a networked data server sub-system on larger systems, supporting system growth. The implemented hardware facilitates multi-channel phase-synchronous data acquisition.

Each wideband receiver (ISA adapter card and mezzanine boards) contains minimal analogue signal conditioning circuitry, a wideband 14 bit 65/80 MSPS A-D converter, dedicated digital down-conversion (DDC) signal processing hardware, extensive FIFO buffering and an Analog Devices ADSP-21160 Super Harvard Architecture floating-point digital signal processor (DSP). The SBC communicates directly with the DSP via the DSP's host processor interface which is accessible to the SBC on the ISA bus. Sample timing and synchronisation circuitry may be implemented on-board (asynchronous/stand-alone receivers) or generated externally (synchronous multi-channel receivers).

An important design decision is the approach taken to realise wide instantaneous bandwidths necessary for fast scanning receivers and wideband DF applications. A wide instantaneous bandwidth is formed from multiple digital down-conversion channels tuned to adjacent bands. This approach provides a scalable solution to achieving both narrow and wide output bandwidths while maintaining efficient down-conversion structures and increased signal processing gain. A limitation of this approach is that the wideband data is channelised, making subsequent narrowband time domain processing of the wideband data difficult.

Each digital receiver board may form the back-end to a wideband analogue receiver or may be configured to sample a bandwidth-limited antenna input directly. The re-

ceiver's analogue input bandwidth may extend to 250 MHz (sub-Nyquist sampling), allowing the receiver to operate in the HF and VHF bands, while supporting instantaneous output bandwidths in excess of 10 MHz.

Much consideration was given to the qualification of receiver boards during system design. Test modes were incorporated into the hardware design, such that the receiver performance could be fully evaluated.

Firmware was written in VHDL and was compiled using Altera Max+Plus II software. Test software operating on the ADSP-21160 DSP was developed using the Analog Devices Inc. VisualDSP++ C/C++ V1.0 compiler and development suite. Host CPU software was developed using the Microsoft Visual C++ 6.0 compiler and development platform. WinDK DDK Development Library V2.7 was used in conjunction with the Windows Platform SDK and Windows NT4.0 DDK in the development of device driver software for communicating with the ISA adapter cards. Simulations were performed under MATLAB 5.2.

1.5 Related Work

Current research efforts focus on improving both converter speed and linearity.

Velazquez[29] decribes a technique that may improve the speed of conversion of high-speed, high resolution analog-to-digital converters in RF receiver applications by up to six times the state-of-the-art using a filter bank architecture.

Sigma-delta techniques promise to provide high-resolution A-D converters capable of sampling narrowband signals at a sampling frequency range that extends to gigahertz[14].

Post-digitisation error correction schemes aim to reduce the non-linearities in the digitisation process by modelling the error mechanisms inherent in A-D conversion. A-D conversion error has been shown to be related to analogue input frequency, and static error correction is giving way to dynamic correction schemes such as phase-plane compensation[9], sinewave histogram compensation [15] and adaptive compensation [18]. A-D converter non-linearities have been reduced by as much as 10 to 20 dB using these techniques.

1.6 Document Overview

Chapter 1 provides an overview of this dissertation, motivating the digitisation of wideband spectra and describing the aim of the dissertation. The layout of the dissertation is also described.

Chapter 2 explores the digitisation of wide spectral bandwidths at RF frequencies. An *ad hoc* estimation of the requirements necessary for the digitisation of wide bandwidths is performed. A-D converter architectures are discussed in light of the requirements for wideband digitisation of RF signals. Dynamic range requirements lay the foundation for a discussion of noise and distortion introduced in the digitisation process. It is shown that sampling aperture jitter may be a significant contributor to noise introduced in the digitisation process, leading to stringent requirements on sampling oscillator jitter performance. Distortion mechanisms are analysed, and methods of distortion reduction are reviewed. Dithering is introduced as an efficient method of improving average A-D converter linearity by reducing input dependent errors. The optimal interfacing of an analogue receiver frontend and an A-D converter is discussed.

Chapter 3 investigates digital signal processing algorithms that may be used to perform down-conversion, rate reduction, bandwidth limiting and spectral estimation. Efficient down-conversion, filtering and rate reduction hardware architectures are examined. The FFT is introduced as an efficient method of spectral analysis. The signal-to-noise ratio improvements inherent to decimation filtering and FFT averaging are explored.

Chapter 4 presents the architecture of the generalised wideband digital receiver. The theory presented in chapters 2 and 3 is applied to the design and specification of the digital receiver. The channelised filter bank approach used to realise wide output bandwidths is described and justified.

Chapter 5 discusses parts of the implementation of the digital receiver in further detail. The problems encountered in the receiver design are described.

Chapter 6 characterises the performance of the digital receiver. Signal-to-noise ratio and receiver linearity measurements are performed. The effect of adding band-limited dither noise is quantified.

Chapter 7 concludes that the requirement of designing a wideband digital receiver that satisfies the requirements stipulated in section 1.3 was satisfied. The resulting receiver is shown to be flexible and scalable, using predominantly COTS components and standard assembly methods. The use of dither to improve receiver dynamic range is found to be justified, both theoretically and empirically. Suggestions on possible improvements to the receiver are discussed.

Chapter 2

Wideband Signal Digitisation

Two requirements are paramount in the digitisation of wideband signals, namely high sampling rates and high instantaneous dynamic range. Bandpass sampling theory places a restriction on the minimum sampling rate that may be used to unambiguously represent a band-limited signal using discrete samples. This in turn places strict demands on A-D converters in terms of sampling rates. A high instantaneous dynamic range is required to reliably receive a weak signal in the presence of larger signals.

2.1 Dynamic Range Restrictions in Wideband Digitisation

The maximum signal that may be presented to the input of an A-D converter may be considered to be a sinusoidal waveform with a peak-to-peak amplitude that maps to the full range of A-D output codes. A larger amplitude would result in output waveform clipping, while a smaller amplitude does not take full advantage of the resolution available in the converter. This waveform is therefore used to set an upper limit on dynamic range. Assuming no noise is present, the minimum signal is one which would result in a change of the least significant bit (LSB) of the converter. Subject to these criteria, the dynamic range of an ideal A-D converter may be defined

as the logarithmic ratio of the powers of these signals [27]:

$$\begin{aligned} DR_{ADC} &= 10 \cdot log_{10}\left(\frac{P_{max}}{P_{min}}\right) \\ &= 10 \cdot log_{10}\left(\frac{\frac{2^{2b}Q^2}{8}}{\frac{Q^2}{8}}\right) \\ &= 20 \cdot b \cdot log_{10}(2) \\ &\approx 6 \cdot b \end{aligned} \tag{2.1}$$

where b refers to the number of bits and Q refers to the voltage per quantisation level. Equation 2.1 is the basis on which the familiar rule-of-thumb that the dynamic range of an A-D converter is "6 dB per bit" is formed. It will later be demonstrated that this measure of dynamic range is not applicable to dithered quantisation schemes, but it provides a useful approximation for the discussion to follow [1]:

If the full-scale sinusoid waveform mentioned above were replaced by two equal amplitude sinusoidal waveforms of uncorrelated phase and frequency, the maximum amplitude of each waveform would have to be halved in order to prevent constructive interference of the signals from overloading the A-D converter. In general, for every doubling of the number of equal-amplitude sinusoids, their amplitudes should be reduced by a factor of 2. This may be viewed as the dynamic range available to each of the sinusoidal signals in the presence of the other signals, and may be expressed in logarithmic form as:

$$DR_{avail} = 20 \cdot b \cdot log_{10}(2) - 6 \cdot log_2(N)[dB] \tag{2.2}$$

where b refers to the number of bits in the A-D converter and N refers to the number of channels. The number of channels, N, may be expressed as:

$$N = \frac{B \cdot O_b}{S_{ch}} \tag{2.3}$$

where B refers to the bandwidth [Hz], O_b the band occupancy and S_{ch} the channel separation [Hz].

Equations 2.2 and 2.3 are combined to formulate an expression for B, the maximum bandwidth that may be sampled:

$$B = \frac{2^{\frac{20 \cdot b \cdot log_{10}(2) - DR_{avail}}{6}} \cdot S_{ch}}{O_b} \tag{2.4}$$

[1] This discussion should be viewed as an *ad hoc* estimation of the dynamic range required of a converter in order to digitise a given bandwidth. It aims to give the reader an impression of the impact of converter resolution on maximum sampled bandwidth, as well as a method of broadly measuring the usability of a wideband receiver in a given environment.

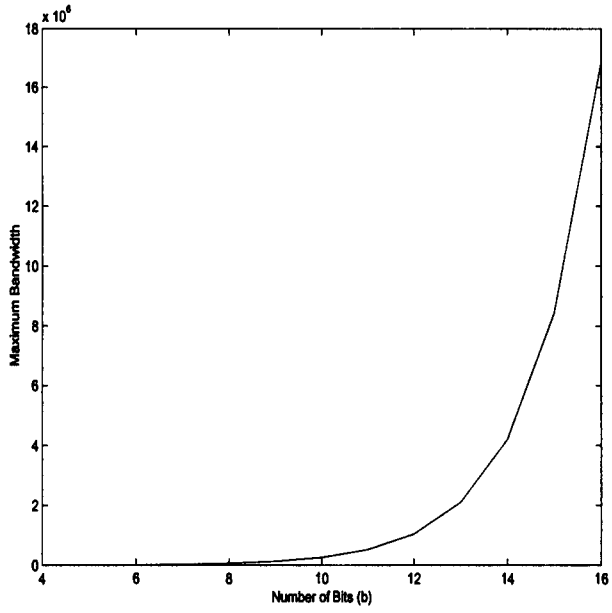

Figure 2.1: An example plot of maximum bandwidth versus number of bits.

By way of example, the assumptions listed in table 2.1 are made.

Parameter	Value
b	4 to 16 bits
DR_{avail}	50 dB
S_ch	8 kHz
O_b	0.1

Table 2.1: Parameters used in the calculation of maximum sampled bandwidth

It is further noted that the above discussion is only a rough approximation, since it was based on equal-amplitude sinusoidal signals as opposed to modulated signals.

The values stated in table 2.1 are substituted into equation 2.4 and plotted in figure 2.1. From this plot it is evident that converter resolution plays a dominant role in determining a maximum bandwidth that may be sampled for any level of desired usable dynamic range.

It should be noted that the probability of all N signals constructively interfering to a given level in a given timespan decreases as N increases, assuming each signal has random phase and frequency. With this in mind, the above may be considered an analysis of the worst-case.

2.2 Bandpass Sampling Theory

This section reviews the theory related to the sampling of wideband signals. For practical purposes, the sampling discussion is restricted to uniform sampling intervals (periodic sampling). The fundamental sampling criterion, credited to Harry Nyquist, forms the basis for the discussion on bandpass sampling theory.

2.2.1 Nyquist's Criterion

Nyquist's criterion stipulates the requirements for perfect reconstruction of a uniformly sampled bandlimited signal [25]:

$$T < \frac{1}{2B} \tag{2.5}$$

where B refers to the upper frequency limit on the spectral components present in the signal and T refers to the uniform sampling interval. Restated in terms of sampling frequency F_s, this can be expressed as:

$$F_s > 2B \tag{2.6}$$

Equations 2.5 and 2.6 can be understood as a necessary condition to prevent overlap of spectral replications, periodically spaced by F_s, that are inherent to the periodic sampling process [17]. This overlap causes ambiguity in signal reconstruction, and is commonly referred to as aliasing. In practice, some level of aliasing does occur, and it is the function of an analogue anti-aliasing filter to reduce the aliasing to acceptable levels. Due to the finite transition band slope that may be realised in practical analogue filtering, it is conventional to restrict the anti-aliasing filter passband to slightly less than that given by equation 2.5. This topic is covered in more detail in sections 2.2.2 and 2.4.

It is conventional to assume that analogue filtering is low-pass, sufficiently attenuating signals above $\frac{F_s}{2}$ to prevent unacceptable aliasing.

2.2.2 Bandpass Sampling

For a variety of applications, including digital receivers, bandpass sampling techniques may be preferable. Bandpass sampling reduces the speed requirement of A-D converters below that necessary with traditional low-pass sampling. The reduced

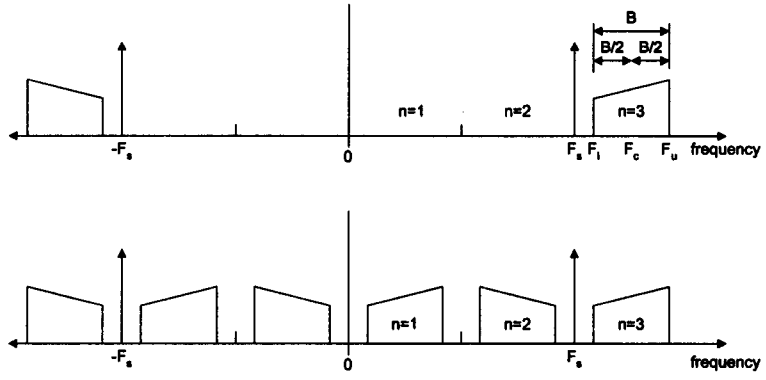

Figure 2.2: A typical bandpass sampling scheme

bandwidth of the converter output reduces the memory required to store the signal in a digital form and reduces the demand placed on subsequent processing.

Figure 2.2 demonstrates the technique of bandpass sampling, also referred to as IF sampling, harmonic sampling, sub-Nyquist sampling and undersampling. The sampling rate is expressed as F_s, and the sampled band, of bandwidth B, is located at (F_l, F_u). The sampling process results in the periodic replication of signals within the sampled spectrum, with period F_s. The spectral replication is used to advantage in bandpass sampling, where it may be viewed as a sampling process with inherent frequency translation into the region $\left(-\frac{F_s}{2}, \frac{F_s}{2}\right)$, commonly referred to as sampling translation[17].

2.2.2.1 Precluding Ambiguities in Bandpass Sampling

A bandpass signal may be sampled at an arbitrary frequency F_s without introducing aliasing ambiguities, provided that the following criteria are met:

- The Nyquist criterion, as expressed in equation 2.5 is met. The definition of B should be redefined as the sampled bandwidth in the bandpass sampling case.
- The passband does not cross an $\frac{NF_s}{2}$ boundary, where N is integer-valued.

These requirements have been stated mathematically as [28]:

$$\frac{2F_u}{n} \leq F_s \leq \frac{2F_l}{n-1} \tag{2.7}$$

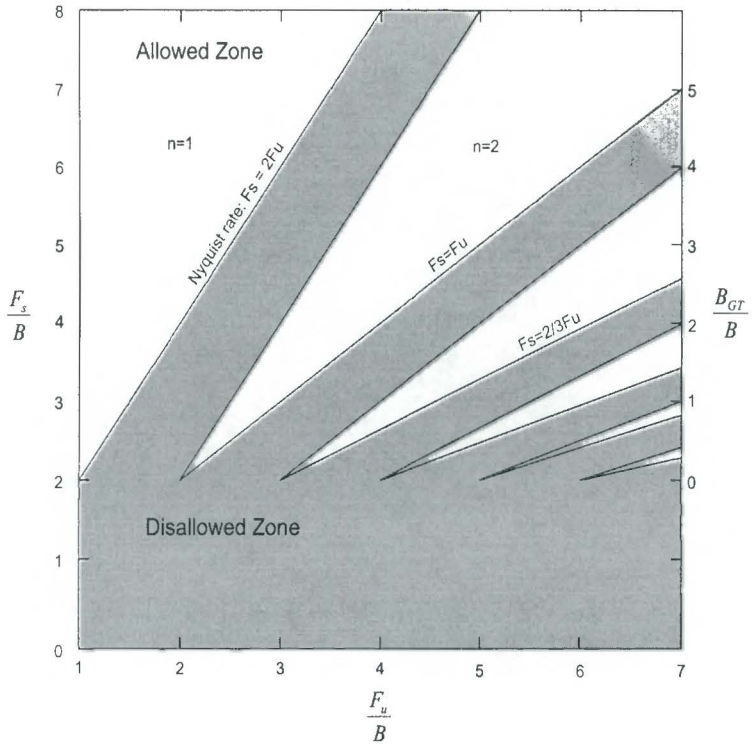

Figure 2.3: The allowed regions for bandpass sampling

where n is an integer given by

$$1 \leq n \leq I_g\left[\frac{F_u}{B}\right] \tag{2.8}$$

and $I_g[x]$ denotes the largest integer within x. Equations 2.7 is depicted graphically in figure 2.3 [28]. With reference to figure 2.3, the abscissa represents the band position F_u, while the ordinate contains the sampling frequency F_s. Both quantities are normalised by B. The band is located at (F_l, F_u). The areas within the wedges are the allowed zones for sampling without aliasing, while the shaded area represents those areas in which aliasing will occur. The lowpass case $F_s \geq 2F_u$, resulting from $n = 1$, corresponds to the large wedge to the left in figure 2.3. Each adjacent wedge corresponds to a successive value of n, and may be referred to as n_{th} zone Nyquist sampling. Vaughan *et al.* [28] propose the inclusion of "guard-bands" in practical bandpass sampling schemes. These assist in eliminating the pathological cases where the edge of the band lies infinitesimally close to an $\frac{F_s}{2}$ boundary (depicted as the wedge borders in figure 2.3). In such pathological cases, minimal deviations in sampling frequency and non-ideal filtering give rise to aliasing. The total guard band, given by $B_{GT} = F_s - 2B$,

is expressed on the right-hand ordinate in figure 2.3.

2.2.2.2 Sampling Frequency Precision

Vaughan *et al.*[28] demonstrates that, to prevent aliasing, the relative precision required of the sampling frequency F_s may be expressed as

$$\begin{aligned} \frac{\Delta F_s}{2B} &= \frac{1}{n(n-1)}\left(\frac{F_u}{B} - n\right) \\ &\approx O\left(\frac{1}{n^2}\right) \end{aligned} \tag{2.9}$$

Equation 2.9 demonstrates that the relative precision required of the sampling frequency F_s increases with separation from the origin, and is approximately related to the inverse square of the separation of the band from the origin. This further demonstrates the necessity for adequate guard-bands as the bandwidth of interest moves up in frequency relative to the sampling frequency.

2.2.3 Spectral Inversion in Bandpass Sampling

Spectral inversion in the baseband alias of the band-of-interest occurs when n is even-valued [28]. This may be seen by examining the aliasing pattern in figure 2.2 When the positive spectral bandpass components are symmetrical about F_c, spectral inversion presents no problem. Spectral inversion should be avoided when signals are asymmetrical with respect to F_c, as is the case in single sideband (SSB) signals. This can be achieved by restricting n to being odd-valued.

It is possible to reverse the spectral inversion with minimal signal processing overhead, so as to avoid this restriction on n. This is achieved by modulating the sample sequence with the sequence $1, -1, 1, -1, \ldots$ or $(-1)^n$ [17]. This effectively translates the sampled spectrum by $\frac{F_s}{2}$. It should further be noted that the DC component will be translated to both $\frac{+F_s}{2}$ and $\frac{-F_s}{2}$.

2.2.4 Applying Bandpass Sampling to Wideband Reception

Bandpass sampling techniques may be used to advantage in wideband digital radio. As mentioned previously, A-D converter output rates may be lowered, reducing the burden on subsequent processing stages.

Furthermore, when undersampling is employed, the signals of interest are aliased into the region $(\frac{-F_s}{2}, \frac{F_s}{2})$. Restated, this inherent down-conversion may be used to translate bandwidths at higher IFs into the aforementioned region. The resulting spectrum, located in the first Nyquist zone, may be translated down to baseband through a variety of digital down-conversion schemes, as detailed in chapter 3. The use of either or both of these techniques may result in a reduction in the number of analogue down-conversion stages and the associated analogue circuitry (LO, mixer etc.).

2.2.5 Quadrature Sampling and Complex Signal Representation

It is common for digital signal processing applications to use a complex data representation with real ("in-phase" or "I") and imaginary ("quadrature-phase" or "Q") parts. A quadrature sampling scheme, as depicted in figure 2.4, may be used to achieve complex or quadrature signal representation at baseband.

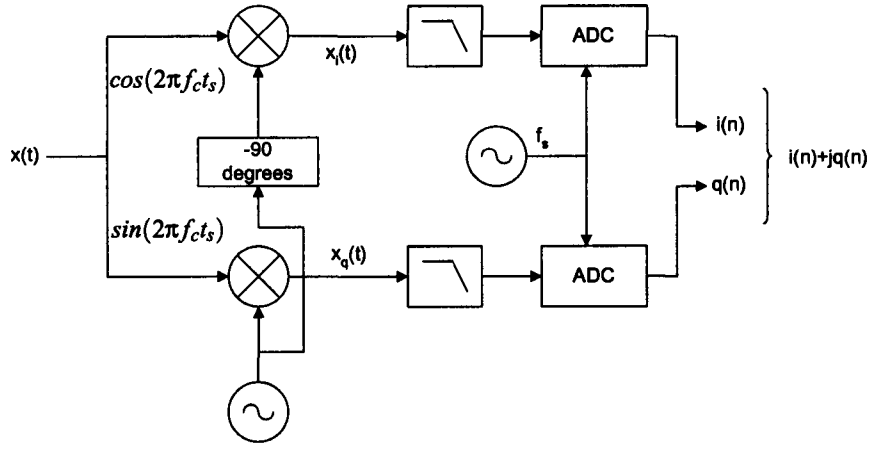

Figure 2.4: Illustration of quadrature sampling scheme.

It may be shown that the multiplication of a signal with a complex exponential $e^{j2\pi f_c t}$ results in a translation or shift of the spectral content of the signal by f_c Hz. The quadrature sampling scheme implements this frequency translation through Euler's identity:

$$e^{\pm j\theta} = cos(\theta) \pm j\, sin(\theta) \tag{2.10}$$

The analogue input signal is mixed by means of analogue mixers with the constituent sinusoidal components of the complex exponential $e^{j2\pi f_c t}$, resulting in a complex-valued representation of the input signal that is translated in frequency by f_c Hz and is

separated into its in-phase (real) and quadrature-phase (imaginary) components. The value of f_c is conventionally chosen such that the input signal is translated to DC ("baseband"). A detailed mathematical account may be found in [16] or [17]. The complex data format is useful in many applications for the following reasons:

1. Each A-D converter may sample at half the rate of conventional sampling, while achieving the same output bandwidth. Restated, the digitised bandwidth may be extended from the theoretical $\frac{f_s}{2}$ imposed by Nyquist's criterion to f_s, the sampling rate of the A-D converter.
2. Quadrature sequences are easily described and manipulated mathematically.
3. Quadrature sequences make Fast Fourier Transform (FFT) processing efficient, covering a wider frequency range than a conventional real FFT. Methods for increasing real FFT efficiency are known, but the complex FFT is usually simpler to use.
4. Phase and amplitude information is easily extracted from the complex representation, facilitating efficient algorithms for demodulating amplitude or frequency modulated signals.

The phase preservation characteristic is particularly useful, and it is for this reason that complex signal representation has been widely adopted in high data rate digital communications systems, radar systems, time difference of arrival (TDOA) processing in radio direction-finding schemes, coherent pulse measurement systems, antenna beamforming applications and single-sideband (SSB) modulators.

Despite the usefulness of quadrature sampling, imbalance in the I and Q channels resulting from amplitude or phase mismatch, mixer DC offsets and $\frac{1}{f}$ noise introduced by active components often limits the dynamic range of a receiver [17] [27]. Complex calibration may be used to improve the dynamic range, but this is undesirable due to increased system cost and complexity. Methods of realising complex basebanded signals which do not suffer from these problems will be presented in chapter 3.

2.3 Sources of Error in Wideband Digitisation

It is conventional in receiver design to characterise the receiver performance in terms of noise and distortion measures. These performance measures dictate the ability of a receiver to detect small signals in the presence of larger signals, and place a limit on the minimum discernable signal (MDS)[23].

In this section, the sources of error in A-D conversion are identified and analysed. It will be shown that many of the errors result in noise or distortion of the digitised signal, which impact negatively on the sensitivity of a digital receiver.

2.3.1 Quantisation Error

The quantisation of a signal into one of l discrete levels, uniformly spaced with spacing q, results in a quantisation error ε, the difference between the signal level and the nearest quantisation level.

Under the assumption that all values of ε in the range $\frac{-q}{2} \leq \varepsilon < \frac{q}{2}$ are equally probable, it may be shown that the quantisation error manifests itself as wideband noise, uniformly distributed within the Nyquist band $\left(\frac{-F_s}{2}, \frac{F_s}{2}\right)$. The mean-square quantisation noise power of an ideal n bit uniform quantiser may then be expressed as [25]:

$$\overline{\varepsilon^2} = \frac{q^2}{12} \tag{2.11}$$

The quantisation of a full scale sinusoid then results in a signal-to-noise ratio of [27]:

$$\left(\frac{S}{N}\right)_{dB} = 1.76 + 6.02n \tag{2.12}$$

The assumption that quantisation error is uniformly distributed within a quantum is generally only true for complex (non-trivial) signals that are large in comparison to the quantisation level [30], and uncorrelated to the sampling frequency [27]. When this assumption fails, error manifests itself as spurious signals within the A-D converter output bandwidth, which may limit the spurious-free dynamic range of a digital receiver. The spurious level may be reduced by sufficiently decorrelating the signal from the sampling frequency. This topic will be explored further in section 2.5.

2.3.2 Static Errors in the A-D Transfer Function

The transfer function of a practical A-D converter differs from the ideal n bit uniform quantiser. The significant errors include gain error, offset error and integral and differential non-linearity. The definitions of the errors, as well as their manifestations, may be briefly summarised as follows:

2.3.2.1 Gain and Offset Error

Gain error refers to an error in the slope of the A-D transfer function, after offset errors have been eliminated. It is defined as [24]:

$$E_{gain} = (V_{FS} - 2 \cdot LSB) - (V_{11} - V_{sz}) \tag{2.13}$$

where V_{11} is the last transition voltage (most positive signal), V_{sz} is the first transition voltage (most negative signal) and $(V_{FS} - 2LSB)$ is the full-scale range minus 2 ideal LSBs. It is expressed as a percentage of full scale range (% FSR) or in least-significant-bits (LSBs).

Offset error may be defined as a common deviation in transition voltage from the ideal transition voltage. It is conventionally measured as the deviation of the first transition from the ideal, after any gain or linearity error has been subtracted, and it is conventionally expressed in mV.

Gain and offset errors manifest themselves as DC offsets in the digitised output, a (minimal) reduction to converter dynamic range (increased noise floor) and a frequency-independent gain error in the digitised signal.

DC offsets are not of severe consequence in IF sampling converters, since the band of interest is located at an IF, and DC offsets are typically filtered out in subsequent digital signal processing stages. Gain errors in the digitised signal may be calibrated out by multiplying each sample with the inverse of the gain error. Gain correction usually does not place increased demand on digital signal processing, since it may be factored into subsequent digital filtering or gain stages. The reduction in A-D converter dynamic range as a result of gain or offset error is small. Gain and offset errors are therefore of minimal impact on the performance of a wideband digital receiver employing an IF sampling architecture.

2.3.2.2 Differential and Integral Non-Linearity

The differential non-linearity (DNL) of an A-D converter may be defined as the difference between an actual code width and the ideal value of one LSB. If the DNL exceeds 1 LSB, the resulting transfer function may become non-monotonic, or missing codes may result.

Differential non-linearity typically manifests itself as higher order non-linearity in the transfer function of an A-D converter [10]. This results in higher order harmonics and mixed products being present in the digital spectrum, which may fall in-band due to aliasing, limiting the spurious-free dynamic range of a digital receiver. The location

and nature of higher-order harmonics are difficult to predict, and it is therefore not possible to place them out-of-band.

The effects of differential non-linearity may be partially eliminated through dithering, as discussed in section 2.5.

Integral non-linearity (INL) may be defined as the deviation of the A-D transfer function from an ideal straight line. End-point INL is specified in terms of the deviation from a straight line between the end-points of the transfer function, in terms of either the transition points or ideal code midpoints. *Best-straight-line* INL is defined as the deviation of a code from a line calculated to minimize the worst-case INL in a mean-squared sense.

INL results in low-order non-linearity in the A-D transfer function. Lower order harmonics and mixed products may result from signals placed at the A-D input, resulting in reduced spurious-free dynamic range. The nature of the non-linearities may vary with differing input power levels, as the integral non-linearities are exercised to different extents.

The effects of integral non-linearity may be reduced through dithering, as discussed in section 2.5.

Although DNL and INL contribute substantially to the degree of linearity of a converter, these measures are generally not sufficient to categorise an A-D converter for communications applications [7], since the position of these errors in the transfer function of the A-D converter may lead to them rarely being exercised. An example of this may be a large DNL error at close to full-scale range. It is unlikely that this would substantially degrade the linearity, since it would rarely be exercised. It is therefore often more beneficial to consider dynamic error measurements, such as spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion (SINAD).

2.3.3 Sampling Jitter

The process of sampling an analogue signal at a given instant in time occurs as follows [24]:

1. An input buffer amplifier tracks the analogue signal. The amplifier output is used to place charge on an energy storage device, and requires a *settling time* in order to track the signal to within a specified accuracy.

2. The output of the amplifier is rapidly disconnected from the energy storage device in response to an encode command (sampling clock transition). The time

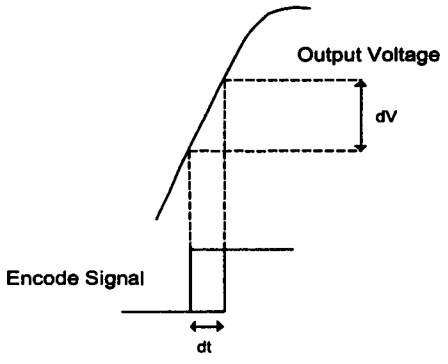

Figure 2.5: The voltage error resulting from encode signal jitter

taken to disconnect is referred to as the *aperture time* and is critical to sampling accuracy.

3. The charge held on the energy storage device is measured and used to determine the quantised output code.

Noise in the A-D converter encode circuitry results in a variance in the exact instant at which the aperture occurs. This time variance is referred to as *aperture uncertainty* or *aperture jitter*, and is usually expressed in seconds RMS. Jitter on the sampling clock adds further variance to the aperture delay. The complete jitter contribution may be found by taking the square root of the sum of the squares of the individual contributions:

$$T_{jitter} = \sqrt{T_a^2 + T_{clk}^2} \tag{2.14}$$

where T_a refers to the aperture uncertainty and T_{clk} refers to the encode clock jitter. The error in sampling time results in a voltage error that is proportional to the slope (slew rate) of the signal at the sampling instant. This is illustrated in figure 2.5. The error contribution for a sinusoidal input may be shown to result in a signal-to-noise ratio of[2]:

$$\left(\frac{S}{N}\right)_{dB} = 20 \cdot log_{10}\left(\frac{1}{2\pi f_a T_{jitter}}\right) \tag{2.15}$$

where f_a refers to the frequency, in Hz, of the input sinusoid and T_{jitter} refers to the total jitter in the encode process, in seconds RMS.

[2]A complete derivation of equation 2.15 may be found in appendix A

2.3.3.1 The Relationship between Oscillator Phase Noise and Jitter

The time-domain jitter content in an oscillator can be related to its frequency-domain characteristic of phase noise. The relationship is explored in [22], a valuable reference on oscillator phase noise. This relationship may be useful, since many oscillator manufacturers do not measure the oscillator jitter[3] , but instead specify their oscillators according to phase noise requirements. It is possible to estimate the time-domain jitter in an oscillator source through its reciprocal relationship to phase noise, as demonstrated by [2]. It should be noted that this estimate is usually an under-estimate, unless oscillator harmonics and sub-harmonics are included in the estimate.

2.3.3.2 Thermal Noise

Noise is generated in the analogue input circuitry of an A-D converter, resulting in an increase in the total receiver noise, and a subsequent reduction in the signal-to-noise ratio. The noise generated in analogue input circuitry (sample-and-hold and amplifiers) can be translated into an equivalent noise temperature, referred to the analogue input. This provides a means by which A-D thermal noise can be factored into total analogue receiver noise.

2.3.4 Relative Noise Contributions in Wideband Digitisation

Wideband noise has been shown to be introduced into the digitisation process in the form of quantisation noise, thermal noise and noise as a result of encode clock jitter. The relative contributions of each of these terms may be found by summing the mean-squared contributions of each of the terms. The following formula, given in [5], provides a reasonable indication of the full-scale (maximum) signal-to-noise ratio that may be expected in a wideband A-D converter:

$$SNR_{dB} = -20 \cdot log_{10} \left[\sqrt{(2\pi f_a t_j)^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{V_n}{2^N}\right)^2} \right] \qquad (2.16)$$

where f_a is the analogue input frequency, t_j the RMS encode jitter, ε the average differential non-linearity normalised to 1 LSB, V_n the rms thermal noise normalised to 1 LSB and N the number of bits. The contributions from encode jitter, static transfer function errors (quantisation noise and differential non-linearity) and thermal noise

[3]The specification of time-domain jitter is becoming more popular, as it is becoming increasingly important in high-frequency applications.

in the A-D analogue input circuitry may be seen as each of the three terms within the square root respectively. Figure 2.6 plots the predicted signal-to-noise ratio versus the analogue input frequency for the AD6644 65 MSPS 14-bit A-D converter, for 1 pica-second RMS oscillator jitter. From this figure, it may be seen that oscillator

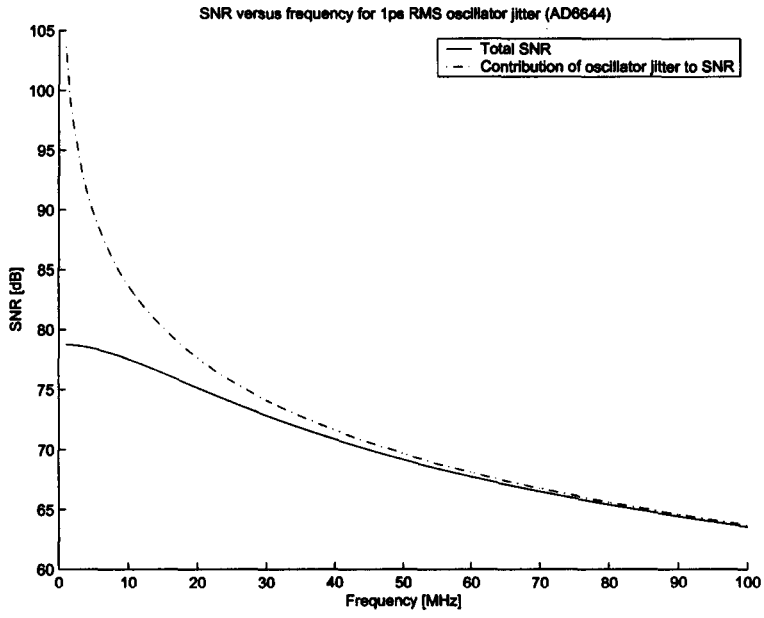

Figure 2.6: Signal-to-noise ratio versus analogue input frequency for the AD6644.

jitter dominates the SNR at high frequencies, for very small levels of oscillator jitter. Since the jitter contribution to SNR is related to the analogue input frequency, undersampling applications impose strict demands on oscillator jitter performance.

2.4 Oversampling

Oversampling is the term used to describe sampling schemes where the Nyquist frequency is greater than the signal bandwidth:

$$\frac{F_s}{2} > B \tag{2.17}$$

The ratio $K = \frac{F_s}{2B}$ is commonly referred to as the *oversampling ratio*. Oversampling may be used to relax the requirements on anti-aliasing filters, as well as to improve the signal-to-noise ratio of a sampled signal. Harmonic spurious may be placed out-of

band through oversampling and appropriate placement of the IF. Oversampling may be used in conjunction with bandpass sampling, realising the benefits of both techniques simultaneously.

2.4.1 Relaxation of Anti-aliasing Filter Requirements

Since analogue filters with infinitely narrow transition regions are not realisable in practice, some degree of oversampling is necessary. By increasing the oversampling ratio, the width of the transition region may be increased, reducing the order of filtering required to meet aliasing requirements. This is illustrated in figure 2.7.

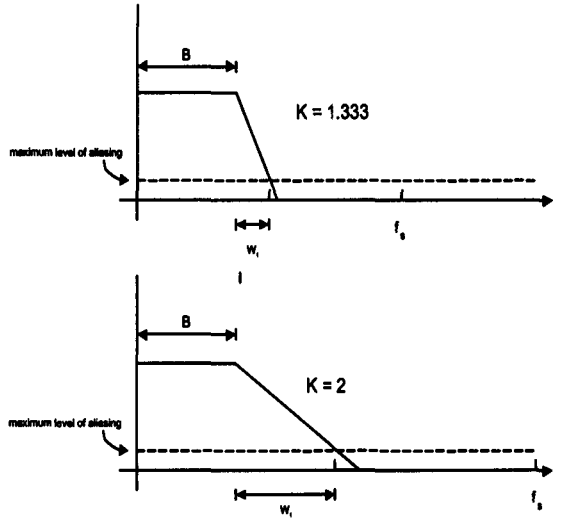

Figure 2.7: Anti-aliasing filter transition width requirements for oversampling ratios of 1.333 and 2 respectively.

2.4.2 Signal-to-Noise Ratio Improvement Through Oversampling

For a given bandwidth B, increasing the oversampling ratio results in a uniform spreading of the quantisation noise power over the wider Nyquist bandwidth $(0, \frac{F_{s\,new}}{2})$. Digital filtering may be employed subsequent to digitisation to filter out noise that falls outside of the bandwidth B, thereby reducing the quantisation noise power, and any other noise falling outside of the bandwidth B, resulting in an improved signal-to-noise ratio. The signal-to-noise ratio improvement due to quantisation noise spreading and

subsequent filtering may be computed using equation 2.18

$$\Delta SNR = 10 \cdot log_{10}(K) \tag{2.18}$$

where K refers to the oversampling ratio. It is noted that the signal-to-noise ratio improvement is limited by the resolution at which the digital filtering is performed. For a reduction in quantisation noise, the digital filtering resolution should exceed the resolution of the A-D converter.

2.4.3 Spurious Harmonic Placement

Lower order harmonics often impose a restriction on the spurious-free dynamic range due to lower order non-linearity within both the analogue receiver sections and the A-D converter. Through correct placement of the band-of-interest B relative to the sampling frequency, lower order harmonics may be constrained to fall outside of the bandwidth-of-interest. Figure 2.8 illustrates a placement of a band-of-interest in the second nyquist zone, such that the second and third harmonics do not fall in-band after digitisation.

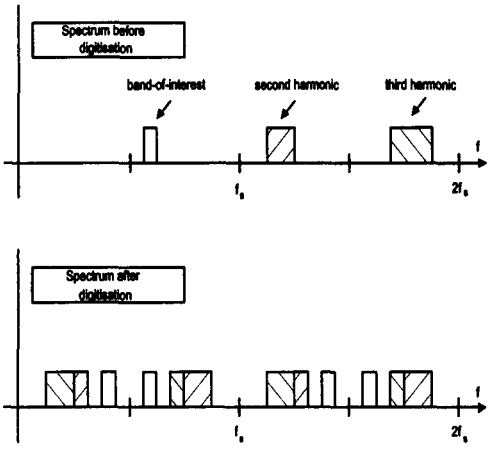

Figure 2.8: Band placement such that harmonics do not fall in-band after digitisation.

2.5 Signal Dithering

Signal dithering is a technique that may be used to improve the dynamic range of an A-D converter. Dithering achieves this by controlling the statistical properties of the

errors introduced in the quantisation process [30]. The input signal is summed with an uncorrelated dither signal which has suitable statistical properties prior to A-D conversion, such that the resulting conversion error is uniformly distributed.

A common misconception is that the level of a sampled signal that may be detected is limited by the converter resolution. In dithered architectures, it is usually possible to extract signals well below the level of a quantum [10]. This is achieved by dithering the signal prior to sampling (which ensures that quantisation noise is sufficiently decorrelated), and using post-conversion digital filtering to reduce the level of quantisation noise. Dithering ensures that the noise is randomly spread across the A-D converter output bandwidth. By sufficiently reducing the A-D output bandwidth through digital filtering, large signal-to-noise ratio improvements may be achieved. This is analogous to analogue receiver band limiting, where received noise is proportional to the receiver bandwidth. The digital filtering should be performed at a higher resolution than the converter resolution, such that quantisation noise may be reduced below the LSB of the converter through band limiting.

2.5.1 Subtractive and Non-subtractive Dithering Techniques

Dithering may be classified as subtractive dither (SD) or non-subtractive dither (NSD). The two techniques are detailed in figure 2.9.

In SD, the dither signal is added prior to quantisation, and subtracted prior to the output. The dither noise does not reduce the signal-to-noise ratio on the output, since it is subtracted. In NSD, the dither signal is not subtracted, and therefore results in an undesirable reduction of the output signal-to-noise ratio.

2.5.1.1 Subtractive Dithering

The characteristic function (*cf*) of a random variable is defined as[30]:

$$\begin{aligned} P_x(u) &= E[e^{-j2\pi ux}] \\ &= \int_{-\infty}^{\infty} F(x) e^{-j2\pi ux}\, dx \end{aligned} \tag{2.19}$$

In SD of an ideal converter, the total error can be rendered uniformly distributed and statistically independent of the system input by choosing a dither such that the *cf* of the dither satisfies the condition [30]:

$$P_v\left(\frac{k}{\Delta}\right) = 0 \quad \forall\, k \in \mathbb{Z}_0 \tag{2.20}$$

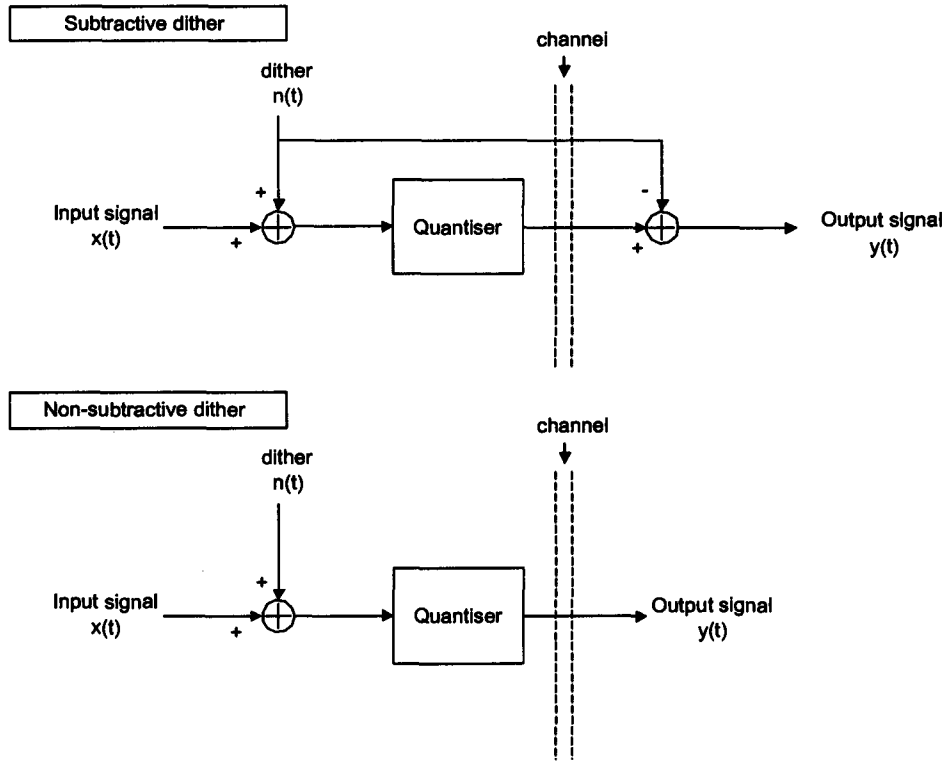

Figure 2.9: Subtractive and non-subtractive dithering schemes

where Δ is the quantisation level and $\mathbb{Z}_0$ is defined as the set of all integers excluding 0. A function that satisfies this condition is a function with a probability density function or *pdf* of the form:

$$p(x) = \Pi_\Delta(x) \tag{2.21}$$

where the rectangular window function of width Γ, Π_Γ, is defined as

$$\Pi_\Gamma(x) = \begin{cases} \frac{1}{\Gamma}, & |x| < \frac{\Gamma}{2}, \\ \frac{1}{2\Gamma}, & |x| = \frac{\Gamma}{2}, \\ 0, & \text{otherwise.} \end{cases} \tag{2.22}$$

The *cf* of this *pdf* may be expressed as

$$P_x(u) = \frac{sin(\pi\Delta u)}{\pi\Delta u} \tag{2.23}$$

This results in the nulls in the *cf* that satisfy the requirements of equation 2.20.

Wannamaker [30] refers to this uniformly distributed dither of peak-to-peak amplitude Δ as rectangular *pdf* dither or *RPDF* dither. He further defines the summation of n such dithers as rectangular *pdf* dither of order n or *nRPDF* dither. The *pdf* of the sum of n random variables may be found by convolving the n individual *pdfs*, while the *cf* is found by multiplying the n *cfs*. Thus, the *pdf* of *2RPDF* dither is triangular, of peak-to-peak amplitude 2Δ.

Furthermore, the values of total error separated in time can be rendered statistically independent of one another by ensuring that the dither values are statistically independent of one another.

2.5.1.2 Non-subtractive Dithering

While subtractive dither may be considered an optimal dither, due to its statistical properties, its implementation may be prohibitively expensive (since the analogue dither needs to be digitally subtracted after digitisation). Non-subtractive dither is therefore given consideration, due to its ease of implementation:

Wannamaker demonstrates that in a non-subtractive dither quantising system it is not possible to render the total error statistically independent of the system input or uniformly distributed for system inputs of arbitrary distribution. An *nRPDF* dither does, however, render the first n moments of the total error process independent of the distribution of the system input, and results in a total error variance of $\frac{(n+1)\Delta^2}{12}$. Higher moments of the error signal will, however, remain input dependent. He further proves that the choice of zero-mean non-subtractive dither *pdf* which renders the first and second moments of the total error independent of the input, such that the first moment is zero and the second moment (the variance) is minimized, is unique and is 2RPDF (triangular) dither.

Non-subtractive dithering cannot render total error values separated in time statistically independent of each other, but it can regulate the joint moments of such errors. Importantly, it can therefore render the power spectrum of the total error white [30].

2.5.2 Small- and Large-scale Dithering

Dither may be categorised as either small-scale (of the order of a quantisation level in amplitude) or large-scale (in the order of full scale in amplitude)[10]. The discussion on dither will be broken down according to these categories, demonstrating the usefulness of each of them.

2.5.2.1 Small-scale Dithering

The aim in small-scale dither (the dithers described above fall into this category) is to reduce the level of fixed-frequency spurious content that is introduced to a signal in the A-D conversion process through quantisation error.

Small-scale dithers aim to ensure that the quantisation error in an otherwise ideal quantisation process results in white noise spread across the sampled spectrum, rather than concentrated at specific frequencies.

2.5.2.2 Large-scale Dithering

The aim of large-scale dither is to average the high-order integral non-linearities in an A-D transfer function, through the addition of large-scale (usually no more than half of full-scale amplitude) noise followed by averaging. This imposes restrictions on the usable dynamic range of the A-D converter [7], but may substantially improve the average linearity of the converter [10]. A subtractive dither scheme is used to eliminate the high degradation in signal-to-noise ratio that results from the addition of high levels of noise prior to sampling.

2.5.2.3 Mid-scale Dithering in Multi-Stage Converters

Practical converter non-linearities, such as DNL and INL discussed above will occur to various extents in regions of the transfer function. This is especially true of multi-stage A-D converters, as is described below.

The total error resulting from DNL may be found by integrating the product of the *pdf* of the input signal and the DNL errors over the input signal range. The amount of non-linearity introduced by the conversion is therefore dependant on the likelihood of samples occurring in code regions with poor differential or integral non-linearity.

In multi-stage sub-ranging converters, the conversion is subdivided into successive conversion stages. A two-stage sub-ranging converter, for example, uses two A-D converter stages. The first A-D converter performs a course conversion. The resulting digitised sample is converted back to an analogue voltage and subtracted from the original signal. The difference signal is scaled and fed into the second A-D converter which performs a finer-resolution conversion. The two A-D conversions are combined to form the total output resolution of the A-D converter. Since the range of the second A-D converter is used many times in the overall range of the A-D converter, any DNL errors in the transfer function of the second A-D converter repeat at intervals of 2^N,

where N is the number of bits in the first-stage A-D converter. Since these errors are repetitive, their likelihood of occurrence is increased, resulting in a drastic decrease the average linearity of the device[7].

Adding dither noise of sufficient amplitude (of the order of the period of the repetitive DNL errors in the transfer function) results in the error being sufficiently decorrelated from the input signal. The reduction in correlation between the input signal and the DNL errors results in a reduction of the spurious harmonics of signals present at the converter input.

2.6 A-D Converter Input Level Matching

In wideband digital receivers it is necessary to precede the A-D converter with analogue signal conditioning.

Analogue filtering is necessary to limit the input bandwidth and reduce aliasing to acceptable levels. Only energy within the input bandwidth is passed to the A-D converter, reducing the input noise power and more importantly the signal energy at the A-D converter input. In section 2.1 the relationship of signal energy to instantaneous dynamic range was demonstrated.

Analogue signal conditioning must also ensure that the received signal level is optimally matched to the A-D converter input voltage range. An optimal match is defined as a match that achieves an optimal combination of desired sensitivity and dynamic range, within the limits of analogue signal conditioning and A-D converter performance. This section discusses the optimal matching of the analogue signal conditioning (in the form of an analogue wideband receiver) and A-D converter interface. The discussion is based on a similar discussion presented in [27].

The following section presents basic analogue receiver design theory which will be required for the discussion that follows.

2.6.1 Characteristics of an Analogue Receiver Chain

For the purposes of gain, noise and distortion analysis, a cascaded chain of analogue components may be modelled as a single component, where:

The overall gain of the cascaded chain is defined as[27]:

$$G = G_1 G_2 \ldots G_n \tag{2.24}$$

or

$$G = G_1 + G_2 + \ldots + G_n[dB] \tag{2.25}$$

where G_1, G_2, ... are the gains of the individual cascaded components.

The overall noise figure F of the cascaded chain is defined as[27]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_2 G_2 \ldots G_{n-1}} \tag{2.26}$$

where F_1, F_2, ... are the noise figures of the individual cascaded components.

The overall output third-order intercept point of the cascade chain is defined as[27]:

$$Q_3 = \frac{G}{\frac{G_1}{Q_{3,1}} + \frac{G_1 G_2}{Q_{3,2}} + \ldots + \frac{G_1 G_2 \ldots G_n}{Q_{3,n}}} \tag{2.27}$$

where $Q_{3,1}$, $Q_{3,2}$, ... are the output third-order intercept points of each individual component.

The intercept point may be used to determine the amplitude of the two-tone third-order intermodulation products by means of the following equation[27]:

$$P_3 = 3\left(P_o - \frac{2}{3}Q_3\right)[dB] \tag{2.28}$$

where P_o refers to the output power of the two signals.

The third-order intercept point may also be related to the two-tone dynamic range by means of the following equation[13]:

$$Q_3 = P_o + \frac{R_d}{2} \tag{2.29}$$

where P_o refers to the output power of the two signals and R_d refers to the dynamic range or difference in level between the test tones and the intermodulation products.

In general, an analysis of the above equations leads to the following guidelines which may be followed in receiver design, in order to achieve either high sensitivity or high linearity:

- Placing lossy elements at the front of an analogue chain reduces the sensitivity of the receiver. A low noise figure amplifier may be placed in the front of the chain to reduce the contribution of successive components to the overall noise figure of the chain.
- Placing lossy elements at the end of the chain increases the third-order non-linearity of the cascaded chain. A high gain amplifier placed at the end of the chain may be used to reduce the contribution of preceding elements within the chain on the overall third-order intercept point.

2.6.2 Combined Analogue and A-D Converter Noise Figure

Under the assumption that the analogue input circuitry may be modelled as a single component as per the above discussion, Tsui[27] demonstrates that the noise figure of the combined analogue circuitry and A-D converter may be written as:

$$F_s = F + M' - M[dB] \tag{2.30}$$

where F refers to the overall noise figure of the analogue signal conditioning circuitry and M and M' are defined as follows:

$$M = 10log_{10}\left(\frac{N_o}{N_c}\right) \tag{2.31}$$

and

$$M' = 10log_{10}(M+1) \tag{2.32}$$

where N_o refers to the output noise power of the analogue circuitry and N_c refers to the noise power of the A-D converter. In an ideal A-D converter, N_c is the quantisation noise power as defined in equation 2.11. M is thus the ratio of the analogue output noise power to the A-D converter noise power.

2.6.3 Optimal Analogue and A-D Converter Interfacing

Tsui[27] proposes to match the analogue input circuitry to the A-D converter, where matching is defined as follows:

- At a certain input level, the level of third-order intermodulation products equals the output noise level.
- The analogue circuitry amplifies this input signal to the maximum allowable input signal level of the A-D converter.

From the above conditions, the required gain and third-order intercept point of the analogue input circuitry can be obtained in the following manner:

The input power is chosen to be a particular level which will be referred to as P_I. The third-order intercept point may then be calculated as[27]:

$$Q_3 = \frac{3P_I - N_1 + 2G - F - B_v - M' + M}{2} \tag{2.33}$$

where Q_3 is the required overall third-order intercept point of the analogue circuitry with input P_I which produces the third-order intermodulation level which matches the noise in a bandwidth B_v. N_1 refers to the noise level present at the amplifier input at room temperature (ca. -174 dBm) with unity bandwidth. B_v is conventionally defined as the processing bandwidth of an N-point FFT where

$$B_v = \frac{F_s}{N} \tag{2.34}$$

and F_s refers to the sample rate of the A-D converter.

The chosen input power P_I is related to the maximum A-D converter input power by[27]:

$$PI + 6 + G = P_{sn}[dBm] \tag{2.35}$$

where

$$P_{sn} = \frac{2^{(b-1)}Q}{2R} \tag{2.36}$$

and b, Q and R refer to the number of bits, the quantisation level in volts and the input impedance of the A-D converter respectively. Noise present at the A-D converter input may require that the maximum input power P_{sn} be marginally reduced. The required gain can thus be determined for the chosen input power P_I.

The dynamic range can be found by[27]:

$$DR = P_I + G - P_3 \tag{2.37}$$

where the third order intermodulation product P_3 equals the noise floor. P_3 may be computed as[27]:

$$P_3 = N_1 + G + F + B_v + M' - M[dBm] \tag{2.38}$$

Tsui demonstrates how the above equations may be used to tabulate G, Q_3, P_3, F_3 and DR for various values of M, such that a designer may optimally choose a desired combination of noise figure and dynamic range to meet the requirements of a particular application.

2.7 Selection of a Wideband A-D Converter

Much of chapter 2 has been devoted to identifying the characteristics of an A-D converter that are important to the wideband digitisation of RF signals. This section considers the selection of an A-D converter that meets these characteristics.

2.7.1 A-D Converter Architectures

A-D converters are largely based on one of five fundamental architectures: successive approximation(SAR), sigma-delta, flash, subranging (pipelined), and bit-per-stage (ripple). A useful description of the architectures and features of each converter type may be found in [1]. In general, the following is noted:

- SAR A-D converters are limited in terms of both sampling rate and dynamic range, and are primarily used in multiplexed data acquisition systems.
- Sigma-delta converters offer excellent dynamic range, but are limited in terms of bandwidth due to high oversampling ratios. Oversampling relaxes the requirements on the analogue anti-aliasing filter, however. Quantisation noise shaping is used to improve signal-to-noise ratio. Bandpass sigma-delta techniques may be used to sample IF (bandpass) signals. The A-D architecture must be designed for the specific frequencies required by the system application, limiting the flexibility of this approach.
- Flash converters provide extremely high sampling rates, but are limited in terms of resolution, due to their hardware-intensive parallel architectures.
- Subranging or pipelined A-D converters achieve sample rates close to those of flash converters, while maintaining high resolution. A Gray-coded output bit-per-stage, proposed by F.D. Waldhauer has been successfully used in high speed ADC architectures [1]. In a pipelined architecture, the conversion is performed by multiple pipelined high-speed, low resolution converters (flash or Gray-coded bit-per-stage converters) which are partially overlapped to form a high-resolution, high speed architecture. Current state-of-the-art allows sampling rates of up to 105 MSPS at 14-bit resolution. It should be noted that many subranging A-D converters are well-suited to bandpass sampling, with analogue input bandwidths in excess of 250 MHz.

2.7.2 Survey of Commercially Available Wideband A-D Converters

The previous section identified pipelined architectures as being the architecture of choice for wideband applications. A brief comparison of commercially available architectures now follows.

The aim was to identify converters which could meet the system requirements as expressed in table 1.1, as well as sampling the HF spectrum (2-30 MHz) and bandwidths

at higher IF's (70 MHz), if these were available. It is noted that in order to sample the HF spectrum, a converter would require a sample rate greater than 60 MSPS in order to meet the Nyquist criterion. Cost was not a primary consideration in the choice of converter.

- Analog Devices Inc. offer a range of 12- and 14-bit pipelined converters, with sampling frequencies which extend to greater than 100 MSPS (in the case of the 12-bit converters). The AD6644 was singled out as the converter of choice, offering 14-bit resolution at a maximum sampling rate of 65 MSPS[4]. The device was offered in sample quantities at the time that the choice was made.
- Intersil offers the HI5905, a 14-bit converter with a 5 MSPS sampling frequency.
- Burr Brown/Texas Instruments offer the ADS850 14-bit, 10 MSPS converter, as well as the 12-bit, 80 MSPS ADS809. Preliminary data sheets were released for the ADS852, a 14-bit, 65 MSPS device presumably in direct competition with the AD6644. At time of publishing, the device is commercially unavailable.
- National semiconductor offer the CLC5958 14-bit, 52 MSPS A-D converter.

Various other manufacturers were considered, but their products were limited in terms of either resolution or sampling frequency.

This concludes the survey of high-speed, high dynamic range A-D converters. It is evident that the Analog Devices AD6644 and the National Semiconductor CLC5958 converters both satisfy the bandwidth requirements at 14-bit resolution.

2.7.3 Comparison of AD6644 and CLC5958

It is necessary to perform a careful comparison of A-D converters, since manufacturers may specify converters in different ways. An example of this is that spurious levels may be defined relative to full scale (dBFS) or relative to the carrier (dBc). When considering spurious levels, careful attention should be given to the analogue input levels and frequencies at which tests are performed, as performance is generally not consistent over the entire Nyquist band, and analogue input levels contribute directly to spurious level. In general, harmonic spurious performance may be seen to degrade with increased frequency and increased signal amplitude. The spurious performance of a pipelined A-D converter may not be a monotonic function of input amplitude, however, due to the repetitive nature of its DNL errors, as described in section 2.5.2.1.

[4]The range has since been extended to 80 MSPS and 105 MSPS devices.

Table 2.2 provides a comparison of the performance of the AD6644 and the CLC5958 A-D converters. Many of the comparative measurements were performed at different analogue input frequencies. Where the input frequencies differed, the device with the lower performance was tested at lower frequencies than the device with the higher performance. Since performance may be seen to degrade with frequency, the comparison favours the lower performing device and therefore may be considered fair.

The AD6644 has a higher analogue bandwidth than the CLC5958. It supports higher sampling rates.

The AD6644 has a 3 dB better SNR and a 5 dB better SINAD. The noise levels are significantly greater than the distortion levels, and it is therefore expected that the SINAD measure is dominated by noise as opposed to distortion. The aperture jitter of the AD6644 is lower than that of the CLC5958. These measures indicate that the noise introduced by the AD6644 is lower than that of the CLC5958 over the entire range of input frequencies, with the noise performance of the AD6644 increasing relative to the CLC5958 as the frequency of signals present at the analogue input increases, due to the lower aperture jitter of the AD6644.

The figures also indicate that the harmonic distortion is lower in the AD6644 device. This is further confirmed by the dynamic performance plots supplied in the data sheets of the respective devices, as well as the static INL and DNL measures.

The gain and offset error performance measures favour the CLC5958 device. These measures do not, however, impact significantly on the performance in an IF sampling architecture, as detailed in section 2.3.2.1.

The AD6644 device was therefore selected as the A-D converter for the implemented system.

	AD6644	CLC5958	
Maximum sampling rate	65	52	*MSPS*
Number of bits	14	14	*bits*
Analogue input bandwidth	250	210	*MHz*
Signal-to-noise ratio[5]	74.0	71.0	*dBFS*
SINAD[5]	74	69	dB
Worst Harmonic Distortion[5] (2_{nd} or 3_{rd})	-90	-89	dBc
Worst Harmonic Distortion[5] (Other)	-92	-91	dBc
Two-tone IM Distortion[7]	-100	-100	dBFS
Offset Error (Typical)	3	2	mV
Gain Error (Typical)	-6	2	%FS
DNL	0.25	0.3	LSBs
INL	0.5	1.5	LSBs
Aperture Jitter	0.2	0.5	ps RMS

[5]Measured with a single tone at -1 dBFS of frequency 15 MHz (AD6644) and 5 MHz (CLC5958) applied to the analogue input

[6]Measured with signal A at 12 MHz (AD6644) and 15 MHz (CLC5958) respectively, and signal B at 15 MHz (AD6644) and 15.5 MHz (CLC5958)respectively.

Table 2.2: A comparison of the AD6644 and CLC5958 A-D converters

Chapter 3

Digital Down-conversion and Multirate Signal Processing

Chapter 2 described the wideband digitisation of IF-sampled signals. After the received spectrum has been sampled, it is necessary for the signal to undergo further processing in order to achieve the desired receiver output. The digitised IF signal is typically translated to baseband after which demodulation or spectral analysis is performed.

The high sample rates required to digitise wide bandwidths at high IFs generally make it either infeasible or not economically viable to perform all of the subsequent signal processing at the full sample rate. The sample rate must be reduced early on in the digital signal processing to the minimum rate at which the required output bandwidth can be unambiguously represented. The process of sample rate reduction, referred to as *decimation*, results in a reduction in the subsequent processing requirements. Digital filtering is required prior to sample rate reduction in order to prevent aliasing ambiguities. It also serves to reduce quantisation noise, if additional resolution is available in the processing stages.

This chapter focuses on the techniques and efficient architectures used to perform spectral translation to baseband, digital filtering and sample rate reduction, which are commonly referred to as digital down-conversion. The discussion is focussed around efficient hardware implementations, since software solutions are currently infeasible at high sampling rates.

3.1 A Generalised IF Sampling Receiver Architecture

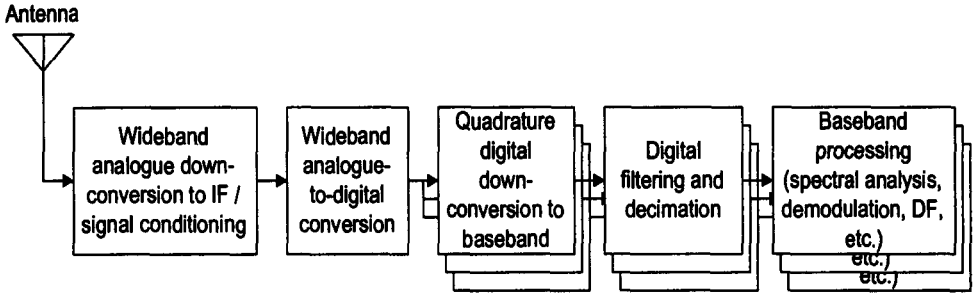

Figure 3.1: A generalised IF-sampling digital receiver.

Figure 3.1 shows a generalised architecture of an IF-sampling wideband digital receiver. While variations on the architecture exist, the functions of frequency translation, filtering and decimation are common to most architectures. The architecture can be seen to have evolved from the conventional analogue super-heterodyne architecture. The input signal received by the antenna undergoes analogue signal processing in order to reduce received bandwidth (reducing received energy and noise), regulate the received signal level using manual gain control (MGC) or automatic gain control (AGC), and translate the wideband spectrum to a suitable IF for A-D conversion, if necessary. The sampled IF signal is translated in frequency to baseband, conventionally by means of multiplying the signal with a local quadrature digital oscillator. Filtering is then employed in order to reduce or reject out-of-band signals, such that they will not alias into the band-of-interest or negatively affect subsequent signal processing. Decimation is used to reduce the signal rate in order to ease the burden on subsequent signal processing. The following sections examine the digital signal processing path in more detail.

3.2 Spectral Translation of IFs to Baseband

Spectral translation is necessary in order to translate the bandwidth of interest to baseband (DC) or a lower IF frequency. It is common to perform the digital frequency translation in hardware, which is often required to operate at the full sampling rate of the A-D converter.

3.2.1 Spectral translation through quadrature digital mixing

The conventional and most flexible approach to digital spectral translation is to multiply the digitised samples by the complex vector $e^{j2\pi f_c n t_s + \theta}$, where f_c is the desired spectral shift, n is a sample indexing variable, t_s is the sampling period and θ is a constant expressing the phase offset.

This is achieved by means of Euler's identity, which is used to separate the complex exponential into real or "in-phase" and imaginary or "quadrature phase" sinusoidal constituents. The sampled signal is separately multiplied by the in-phase and quadrature-phase sinusoids, as depicted in figure 3.2. Digital sinusoidal signal sources

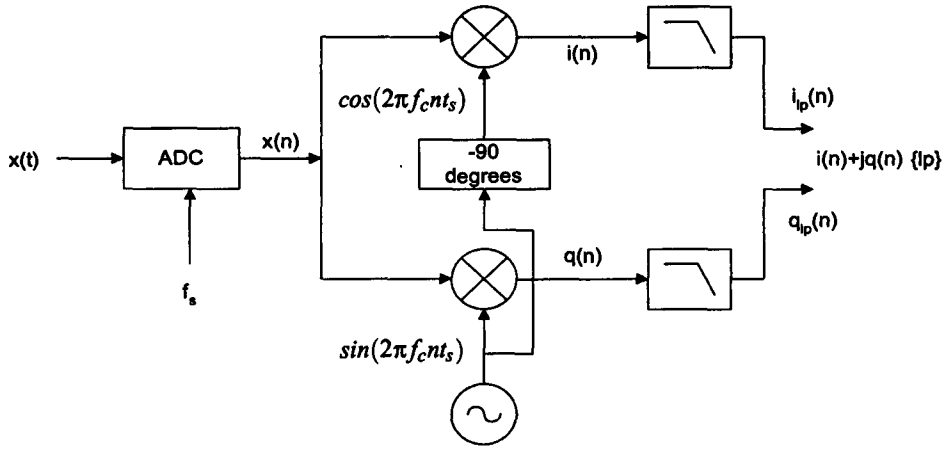

Figure 3.2: The quadrature digital mixing process.

of programmable frequency and phase, commonly referred to as a digital signal synthesisers (DSS) or numerically controlled oscillators (NCOs) are commonly used to create the quadrature signals. The resulting output signal is a spectrally translated complex signal that is separated into in-phase and quadrature-phase components. NCOs are typically implemented using programmable phase accumulators followed by sinewave look-up tables, as described in [4]. NCO-related quantisation errors as a result of low phase or amplitude resolution in the NCO circuitry may manifest themselves as spurious signals. [4] provides a quantitative analysis of the errors involved in digital signal synthesis.

3.2.2 Hardware-Efficient Frequency Translation

If the sampling frequency is related to the centre frequency of the spectrum by $f_s = 4f_c$ then the hardware required to perform quadrature down-conversion can be substantially reduced [17]. Down-conversion of bands at $\frac{f_s}{4}$, with $\theta = 0$ require that the NCO generate samples

$$\begin{aligned} s(n) &= i(n) + jq(n) \\ &= cos\left(\frac{n\pi}{2}\right) + jsin\left(\frac{n\pi}{2}\right) \end{aligned} \tag{3.1}$$

which may be reduced to the repetitive sequences

$$\begin{aligned} i(0) &= 1 \\ i(1) &= 0 \\ i(2) &= -1 \\ i(3) &= 0 \\ i(n+4) &= i(n) \end{aligned} \tag{3.2}$$

and

$$\begin{aligned} q(0) &= 0 \\ q(1) &= 1 \\ q(2) &= 0 \\ q(3) &= -1 \\ q(n+4) &= q(n) \end{aligned} \tag{3.3}$$

The multiplication of a discrete signal by the above sequence can be implemented by hardware efficient circuitry which implements sign changes and zeroing of appropriate samples in the discrete input sequence, as opposed to hardware multipliers which have comparatively higher hardware complexity and therefore reduced speed of operation. A memory-intensive sinusoidal waveform look-up table is also eliminated in this scheme.

3.2.3 Performance Advantages of Digital Spectral Translation

At this stage it is important to note one of the key advantages of digital frequency translation over analogue mixing: Analogue mixers are non-linear devices that rely on the second order (square) term to achieve frequency translation[27]. The output current of an analogue mixer may be related to the input voltage by:

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + \ldots \tag{3.4}$$

where V represents the sum of the input voltage and the local oscillator, a_x the coefficient of the term of order x and I the output current. It is common for mixers to exhibit

significant non-second order output. Both second order and non-second order terms result in mixed products at frequencies other than $f_c + f_{lo}$ and $f_c - f_{lo}$, where f_c refers to the centre frequency of the signal passband and f_{lo} is the frequency of the local oscillator. This is in contrast to a digital multiplier, since the multiplication operator results in only the translated bands centred at $f_c - f_{lo}$ and $f_c + f_{lo}$ being present in the output. In the case of digital frequency translation, non-linearity is introduced through quantisation errors, but these may be reliably limited through appropriate choice of processing resolution.

3.3 Digital Resampling and Multirate Signal Processing

Digital resampling may be used to reduce the sample rate to the minimum rate required to represent the information content of a signal, prior to performing processing on it. Digital resampling is used to convert the sampling rate of a discrete signal from a given rate $F = \frac{1}{T}$ to a different rate $F' = \frac{1}{T'}$ after the signal has been sampled. When the new sampling rate F' is higher than the original sampling rate the process is referred to as *interpolation*, while a reduction in the sampling rate is referred to as *decimation*. If the ratio of the original and new sample rates is restricted such that

$$\frac{T'}{T} = \frac{M}{L} \tag{3.5}$$

where M and L are integers, computational, storage and control efficiencies may be realised [8]. A thorough coverage of multirate signal processing may be found in Crochiere et al.[8]. The processes of integer decimation, integer interpolation and decimation by non-integer factors is briefly summarised below.

3.3.1 Decimation by Integer Factors

Decimation by an integer factor M involves reducing the sampling rate of a signal, such that

$$\frac{T'}{T} = \frac{M}{1} \tag{3.6}$$

The resultant sampling rate may be expressed as

$$F' = \frac{F}{M} \tag{3.7}$$

The sample rate reduction is achieved by retaining every Mth sample of the input signal $x(n)$ to form the sequence $y(m)$. Lowpass digital filtering is conventionally performed at the original sample rate prior to sample rate reduction in order to limit the aliasing at the lower sampling rate. For unity gain through the decimator, the lowpass filter should approximate the ideal characteristic

$$H(e^{j\omega}) = \begin{cases} 1, & |\omega| \leq \frac{2\pi F'T}{2} = \frac{\pi}{M} \\ 0, & \text{otherwise} \end{cases} \tag{3.8}$$

Figure 3.3 illustrates the process of decimation by an integer factor M.

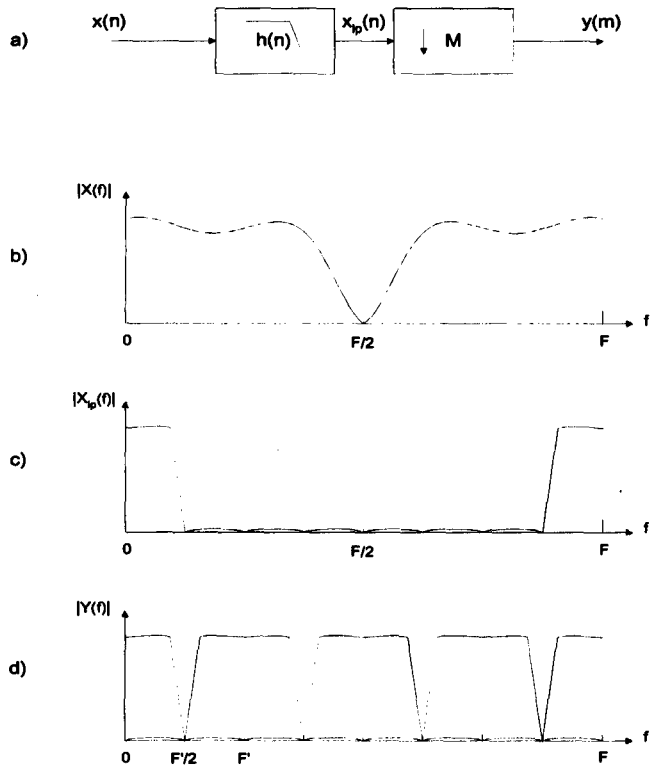

Figure 3.3: Decimation by an integer factor M=4.

3.3.2 Interpolation by Integer Factors

For a sampling rate increase by a factor L, such that

$$\frac{T'}{T} = \frac{1}{L} \tag{3.9}$$

the resulting sampling rate may be expressed as

$$F' = LF \tag{3.10}$$

Increasing the sampling rate by a factor L requires the insertion of $L-1$ zero-valued samples between each pair of adjacent samples in the original sequence $x(n)$, forming the intermediate signal

$$w(m) = \begin{cases} x\left(\frac{m}{L}\right), & m = 0, \pm L, \pm 2L, \ldots \\ 0, & \text{otherwise} \end{cases} \tag{3.11}$$

The spectrum of $w(m)$ contains images of the baseband spectrum centred at harmonics of the original sampling frequency, as illustrated in figure 3.4 (c). To recover the baseband signal of interest and reject the unwanted image components, it is necessary to filter the signal $w(m)$ with a digital lowpass filter which approximates the ideal characteristic

$$H(e^{j\omega}) = \begin{cases} L, & |\omega| \leq \frac{2\pi FT'}{2} = \frac{\pi}{L} \\ 0, & \text{otherwise} \end{cases} \tag{3.12}$$

A gain factor L has been included in the filter, in order to compensate for the loss resulting from the insertion of the zero-valued samples. The process of integer interpolation is depicted in figure 3.4.

3.3.3 Resampling by Non-Integer Factors

Decimation or interpolation by non-integer factors can be achieved by cascading the processes of integer interpolation and integer decimation. This results in resampling by rational factors that adhere to the restrictions expressed in equation 3.5, which favour a reduced complexity of implementation. The rate conversion is achieved by first increasing the sampling rate by an integer factor L, and then decreasing it by the integer factor M. It is imperative that the interpolation precedes the decimation to prevent loss of information [8].

In the aforementioned structure, the digital filters required for the integer interpolation and decimation processes both run at the interpolated sample rate, and may be combined into a single filter. Since the filter must serve the purposes of both the interpolation and the decimation filtering, it should be designed to approximate the ideal lowpass filter characteristic:

$$H(e^{j\omega}) = \begin{cases} L, & |\omega''| \leq min|\frac{\pi}{L}, \frac{\pi}{M}| \\ 0, & otherwise \end{cases} \tag{3.13}$$

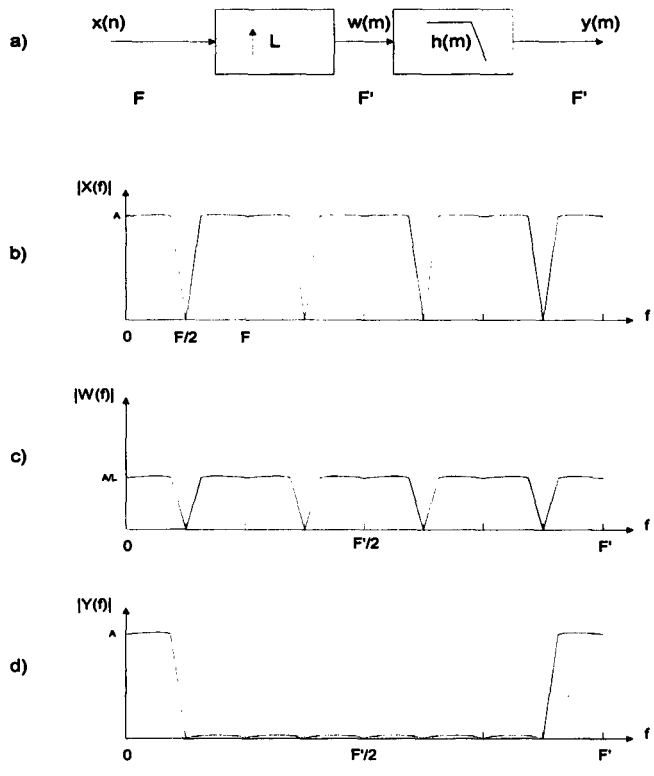

Figure 3.4: Interpolation by an integer factor M=4.

where

$$w'' = 2\pi f \frac{T}{L} \tag{3.14}$$

Figure 3.5 serves as a block diagram of the rational resampling scheme. The individual processes of integer interpolation and decimation are shown in (a), while the efficient combined-filter implementation is shown in (b).

3.3.4 Efficient Architectures for Integer Decimation

The high sampling rates at which decimation filtering may be required to operate has created a need for hardware-efficient decimation filtering. Two methods of combined digital filtering and decimation have gained recognition due to their memory efficiencies and ability to operate at high speeds, namely half-band Finite Impulse Response (FIR) filtering and cascaded integrator-comb (CIC) filters. An explanation of both schemes follows, motivating the usefulness of each in decimating applications.

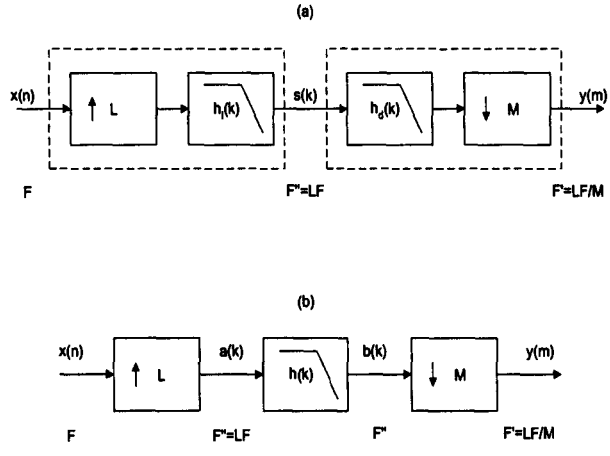

Figure 3.5: Resampling by a rational factor $\frac{L}{M}$.

3.3.4.1 Half-band FIR Decimation Filters

The half-band FIR filter may be considered as a special case of FIR filtering, where the filter characteristics are constrained as follows [8]:

$$\begin{aligned} \delta_s &= \delta_p = \delta \\ \omega_s &= \pi - \omega_p \end{aligned} \tag{3.15}$$

where δ_s and δ_p refer to the ripple in the stopband and passband respectively, as depicted in figure 3.6, and ω_s and ω_p refer to the stopband and passband cut-off frequencies respectively.

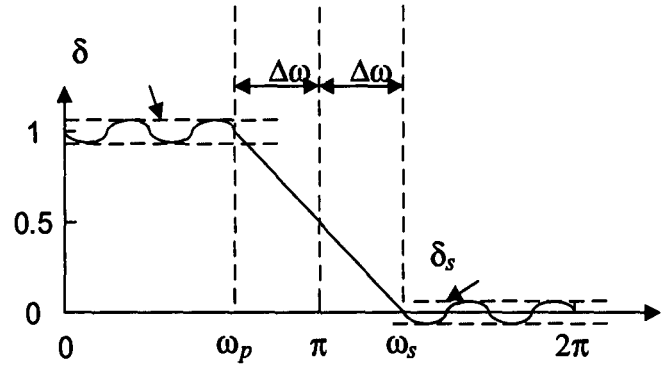

Figure 3.6: Halfband filter frequency response.

The resulting equiripple optimal solution has the frequency domain characteristic that

$$H(e^{j\omega}) = 1 - H(e^{j(\pi-\omega)}) \tag{3.16}$$

The frequency response is thus symmetric about $\omega = \frac{\pi}{2}$. Furthermore, the filter coefficients have the property that

$$h(k) = \begin{cases} 1, & k = 0 \\ 0, & k = \pm 2, \pm 4, \ldots \end{cases} \tag{3.17}$$

This time-domain property results in a substantial reduction in the number of multiplications required per output sample. For the general case of a T-tap half-band filter, $\frac{T+1}{2} + 1$ multiplications are required per output sample. The half-band filters frequency and time domain properties result in useful filter structures for performing efficient decimation by a factor of two[1].

3.3.4.2 Cascaded Integrator-Comb Filters

Hogenauer [12] proposed the structure for a multiplierless, minimal storage decimating filter that is well-suited to economical hardware implementations. The cascaded integrator-comb (CIC) filter consists of an integrator section which operates at the higher sampling rate and a comb section operating at the low sampling rate, as depicted in figure 3.7. The integrator section consists of N ideal digital integrator stages

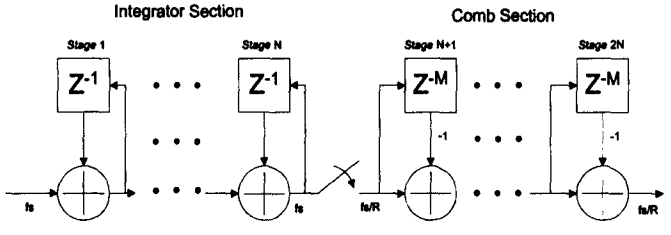

Figure 3.7: Structure of a CIC decimating filter.

operating at the higher sample rate f_s. The comb section operates at the lower sampling rate $\frac{f_s}{R}$, where R is the integer decimation factor and is composed of N comb stages with a differential delay of M samples per stage. The transfer function of the

[1]The restriction that $\delta_p = \delta_s$ may result in increased filter lengths, since for most practical systems $\delta_s << \delta_p$, but this is usually outweighed by the twofold increase which results from the half-band filter structure.

CIC filter, referenced to the high sampling rate, f_s, may be expressed as [12]:

$$H(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \tag{3.18}$$

$$= \left[\sum_{k=0}^{RM-1} z^{-k}\right]^N \tag{3.19}$$

The frequency response is lowpass, with nulls located at multiples of $f = \frac{1}{M}$ relative to the output sample rate. The region around every Mth null is folded into the passband resulting in aliasing errors. The maximum aliasing usually occurs at a frequency of

$$f_a = 1 - f_c \tag{3.20}$$

relative to the output sample rate, where f_c refers to the lowpass output passband. The passband must therefore be chosen such that levels of aliasing are acceptable. The amount of passband aliasing can also be brought within prescribed bounds by increasing the number of stages in the filter. Figure 3.8 illustrates a typical CIC fil-

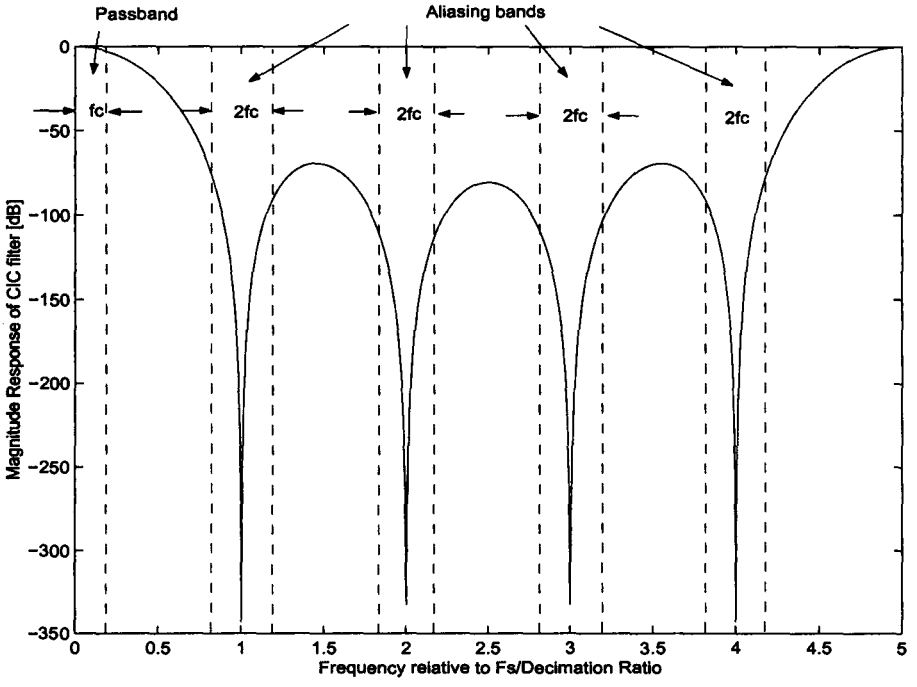

Figure 3.8: Structure of a CIC decimating filter.

ter response, identifying the bands that alias into the passband. Conventional filters

following the CIC filters may be used to flatten the response in the passband, which suffers from drooping, and to limit the transition band width and improve stopband attenuation.

CIC filters are well-suited to applications where high sample rates make multipliers an uneconomical choice or where large rate change factors would require large amounts of coefficient storage or fast impulse response generation. The frequency characteristics of the filter are severely limited. This is typically overcome by using CIC filters to perform decimation, usually by large factors, followed by conventional filters operating at the lower sampling rate to shape the frequency response.

3.3.5 Enhanced Signal-to-Noise Ratio through Decimation Filtering

It has been shown that filtering is required prior to decimation in order to prevent undesired aliasing. While the suppression of aliasing is the primary goal of decimation filtering, the filtering has the added benefit of reducing the received bandwidth, thereby reducing the received noise. The signal-to-noise ratio is improved by:

$$\Delta SNR = 10 \cdot log_{10}\left(\frac{B_n}{B_d}\right) \tag{3.21}$$

where B_n refers to the noise bandwidth (the noise is assumed to be uniformly distributed within this band) and B_d refers to the bandwidth of the decimation filter. For decimation filtering which approaches the ideal characteristic of equation 3.8, under the assumption that noise present in the sampled signal is evenly distributed over the sampled bandwidth[2], the signal-to-noise ratio improvement may be reduced to:

$$\Delta SNR \approx 10 \cdot log_{10}(D) \tag{3.22}$$

Decimation may therefore be viewed as a method of improving signal-to-noise ratio at the cost of reduced output bandwidth.

3.4 Enhanced Signal-to-Noise Ratio using the Discrete Fourier Transform

The Discrete Fourier Transform (DFT) is commonly used to perform spectral analysis. In 1965 Cooley and Tukey re-introduced the Fast Fourier Transform[3] (FFT) as

[2]This is true for uniformly distributed quantisation noise.

[3]Previously known to Gauss

a computationally efficient implementation of the DFT. A complete coverage of the DFT and FFT may be found in many DSP texts, including [20] or [21], and it is assumed that the reader is familiar with the frequency domain decomposition which an appropriately windowed DFT will produce.

In wideband scanning receivers, it is common to use the FFT to perform spectral power estimation. The inherent time averaging of the DFT computation results in a signal-to-noise ratio improvement in the observed output spectrum of a signal. For real-valued signals, the processing gain results in a SNR improvement of approximately

$$\begin{aligned} \Delta SNR &= 20 \cdot log_{10}\left(\sqrt{(N)}\right)\ dB && (3.23) \\ &= 10 \cdot log_{10}(2) \cdot log_2(N)\ dB && (3.24) \\ &\approx 3 \cdot log_2(N)\ dB && (3.25) \end{aligned}$$

where N refers to the number of points in the DFT. The exact processing gain is affected by factors such as the choice of windowing function used. Equation 3.23 serves as a useful approximation, however.

Chapter 4

Wideband Digital Receiver Architecture and Design

This chapter details the implementation of digital receiver hardware capable of realising the specifications listed in table 1.1. The system architecture and requirements are briefly described, with the intention of providing the reader with a background understanding of the digital receiver application within a receiver system.

4.1 Overview of System Architecture

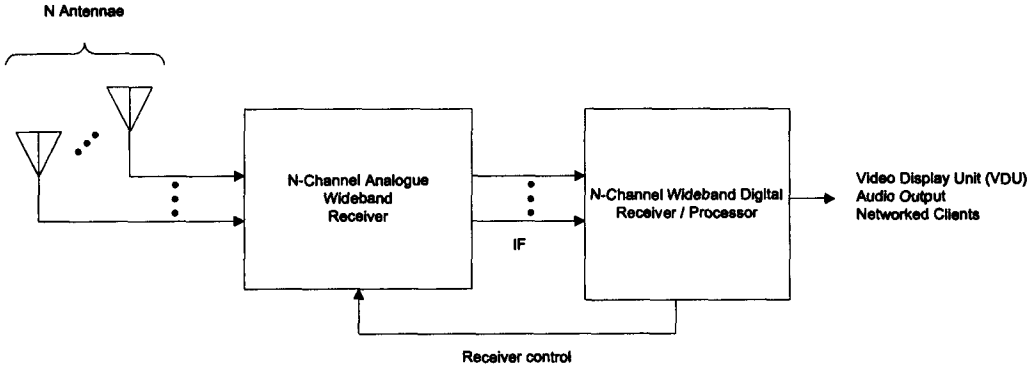

Figure 4.1: Typical wideband surveillance receiver system configuration.

Figure 4.1 demonstrates a typical wideband surveillance receiver system configuration. The system consists of N antennae which are fed into N wideband analogue

receiver channels. The wideband analogue receivers limit the received bandwidth, allow for dynamic receiver gain and are responsible for translating a wideband received spectrum to an output IF within the input frequency range of the A-D converter. In a scanning mode, the wideband analogue receiver sequentially translates successive bands within the analogue receiver input range to the output IF, under the control of the digital receiver. The bands are merged to provide an output display that may be several gigahertz wide. Multiple antennae are necessary in wideband direction finding or beamforming applications, where the relative phases of signals impinging on the antennae is of primary importance. The output signal-to-noise ratio may also be enhanced through appropriate combination of outputs from multiple receiver channels observing the same signal.

Figure D.2 in appendix D provides an example of a typical digital receiver configuration. The digital receiver implementation consists of one (in the case of a single antenna system) or more (in the case of a multi-antenna system) wideband digital receivers implemented on full length ISA adapter cards and accompanying mezzanine modules. The system is housed in a nineteen inch, 4U, rack-mountable ruggedised industrial computing chassis. A commercially available single board computer (SBC) featuring single or dual Intel Pentium processors and 100 Mbit ethernet forms the main system controller and high performance back-end processor for the digital receiver design. The SBC communicates with the adapter cards via a passive backplane. The SBC runs the Microsoft Windows NT operating system.

The rack may function as either a stand-alone receiver or a networked data server subsystem within a larger system, facilitating system expansion. The system is capable of phase-synchronous data acquisition on multiple adapter cards, a prerequisite in direction finding (DF) and beamforming applications.

The following sections focus on the implementation of the ISA adapter card based digital receiver, which is responsible for wideband digitisation, digital down-conversion and baseband processing of HF and VHF signals.

4.2 Digital Receiver Channel Architecture

This section reviews the digital receiver requirements, before presenting a scalable solution based on commercial off-the-shelf (COTS) components. The digital receiver channel design is then described. Detailed design decisions which are worthy of special attention are explored in chapter 5.

4.2.1 A Review of the Digital Receiver Requirements

The digital receiver was required to be implemented on a full length ISA-based adapter card and mezzanine modules. The adapter card was required to function as a general-purpose digital signal processing board, with application-specific hardware residing on mezzanine modules. The wideband digitisation and digital down-conversion circuitry was required to reside on a 110 mm by 170 mm mezzanine board, which will be referred to as the ADC-DDC module from this point onwards.

The digitised, basebanded output from the ADC-DDC mezzanine module was required to interface to a high performance general purpose digital signal processor on the ISA adapter card, which would perform further signal processing such as spectral estimation and demodulation.

The digital receiver design was required to operate in two modes:

- A wideband surveillance receiver mode, in which the Discrete Fourier Transform (DFT) was to be used to perform spectral analysis.
- A narrowband signal extraction and demodulation mode.

In the extreme case, the wideband surveillance receiver application required the digitisation of a 10 MHz input bandwidth centred at an IF of 12.8 MHz, with an instantaneous output bandwidth of 10 MHz at 12.5 kHz frequency resolution. Provision was required for octave reductions in the output bandwidth, down to one eighth of the original bandwidth, with an appropriate output sample rate reduction. The narrowband requirements were to sample input bandwidths up to 800 kHz, and produce a basebanded output of approximately 5 kHz bandwidth, with minimal output rates to ease the burden on subsequent demodulation processing.

These two operating modes generally result in conflicting digital down-conversion hardware implementations:

The former may be realised by a quadrature NCO and multipliers operating at the sampling rate, followed by FIR filtering and appropriate decimation by small integer factors. The FIR filtering is required to operate at the full sampling rate. It is clear that the processing power required to perform filtering at high sampling rates is difficult to achieve using digital signal processors. By way of example, a 63-tap FIR filter running at a sampling rate of 50 MSPS would be required to perform 3.15×10^9 multiply-accumulates (MACs) per second. Decimation by non-integer factors through a combination of integer interpolation and decimation is difficult to achieve at high sample rates, since the image reject/anti-aliasing filter is then required to operate at

the interpolated rate which is even higher than the original sampling frequency. Decimation is therefore usually limited to integer values.

The latter is efficiently achieved by translating the signal to baseband by means of a quadrature NCO and multipliers operating at the full sample rate, followed by a large sample rate reduction by means of CIC decimation filters. FIR filtering operating at the decimated rate may be used to shape the output spectrum, as described in section 3.3.4 on page 46.

4.2.2 Commercially Available Digital Down-conversion Hardware

A survey of commercially available components for digital down-conversion was performed. High-end general purpose digital signal processors, FPGA-based solutions and commercially available ASICs were explored.

The Analog Devices ADSP-21160 general purpose floating-point DSP was considered as a software configurable solution. The ADSP-21160's SIMD architecture, capable of performing 6 floating-point operations per clock cycle at a core clock rate of 80 MHz (480 MFLOPS) could not realise the solution in a single processor. A multi-processor solution was rejected due to cost, complexity and space constraints.

FPGA-based solutions offer the advantages of reconfigurability and parallel architectures. Preliminary experimentation with the Altera Max+plus II FPGA compiler and FIR filter design plug-in[1] demonstrated that an FPGA-based solution would require many devices due to limited memory capacity, and would require much optimisation to perform signal processing at sufficiently high rates with sufficient resolution. The cost of an FPGA-based solution was found to be prohibitively expensive. The FPGA-based solution was therefore rejected.

A survey of commercially-available ASICs identified the components listed in table 4.1.

The GC1012A wideband digital down-converter was rejected due to its 12-bit resolution, which was insufficient to take full advantage of the AD6644's 14-bit resolution.

The Intersil HSP45116 NCO and modulator is an ASIC solution for performing quadrature down-conversion. The HSP43220 is a 4th order CIC programmable decimation filter followed by a decimating FIR filter. By placing the HSP45116 ahead of the HSP43220 (separate HSP43220s are required for the I and Q data paths, quadrature down-conversion may be performed from any IF, and the output may be filtered and

[1] Downloaded from the following URL: `http://www.altera.com/`

Part Number	Manufacturer	Maximum Sample Rate	Resolution	Description
GC1012A	Graychip	80 MSPS	12-bit	Wideband digital down-converter.
GC4016	Graychip	100 MSPS	16-bit	4-Channel narrowband digital down-converter.
HSP45116	Intersil	52 MSPS	16-bit	NCO/Modulator
HSP43216	Intersil	52 MSPS	16-bit	Halfband filter
HSP43220	Intersil	33 MSPS	16-bit	CIC/FIR Filter
HSP50214	Intersil	65 MSPS	14-bit	Narrowband digital down-converter.
HSP50216	Intersil	70 MSPS	16-bit	4-Channel narrowband digital down-converter.
AD6624	Analog Devices	80 MSPS	14-bit	4-Channel narrowband digital down-converter.

Table 4.1: Commercially available ASICs for digital down-conversion

decimated by large factors. This solution is capable of achieving 96 dB SFDR for narrowband outputs. For small decimation factors, the FIR filter length is limited, resulting in poor stopband attenuation and subsequently poor SFDR. The sample rate is limited to 33 MHz. Both of these factors exclude this architecture from achieving the 10 MHz bandwidth at an IF of 12.8 MHz.

The HSP43220 halfband decimate by 2 filter offers 90 dB of stopband attenuation. The device supports $\frac{f_s}{4}$ down-conversion, as described in section 3.2.2. By combining three of these devices in a two-tiered structure, one may perform wideband down-conversion on a signal that is centred at 12.8 MHz with a bandwidth of 10 MHz and a complex output rate of 12.8 MSPS. This architecture is restricted in terms of both bandwidth and input IFs. By preceding the devices with an HSP45116, the restriction on the IF is lifted. The architecture does not allow for decimation by large factors, since each halfband filter may only decimate by a factor of two. Operating speed limitations further limited the use of this architecture.

Narrowband digital down-converters, such as the GC4016, HSP50214, HSP50216 and AD6624 incorporate many of the building blocks required to perform narrowband digital down-conversion in a single package. The devices include a complex NCO and multipliers, programmable CIC decimation and FIR filtering. The devices support decimation by non-integer factors through integer interpolation and decimation. The devices further support AGC (excluding the AD6624), either through internal digital AGC or receive signal strength indication (RSSI) which may be placed in a feedback

loop with analogue gain stages. Rectangular-to-polar conversion and frequency discrimination circuitry is provided in the Intersil devices. The GC4016, AD6624 and HSP50216 provide 4 independent down-conversion channels. The GC4016 offers the widest output bandwidth when operating at any particular input sample rate, subject to the constraint of meeting 90 dB SFDR requirements.

4.2.3 A Scalable Digital Receiver based on COTS components

ASIC solutions for performing digital down-conversion are well suited to either wideband or narrowband outputs. A solution was not available which could cater for both extremes. This section details the implementation of an ASIC-based architecture capable of realising both wideband and narrowband outputs, using the GC4016 narrowband digital down-converter. The GC4016 was selected based on its high output bandwidth per channel, while meeting the system SFDR requirements. It also features a parallel output bus, which facilitates high speed transfer of data to a DSP, as well as operation up to 100 MSPS. Figure 4.2, extracted from the GC4016 datasheet [26], shows a block diagram of the internal architecture of the GC4016. An in-depth discussion of the GC4016 functionality can be found in the GC4016 data sheet[26].

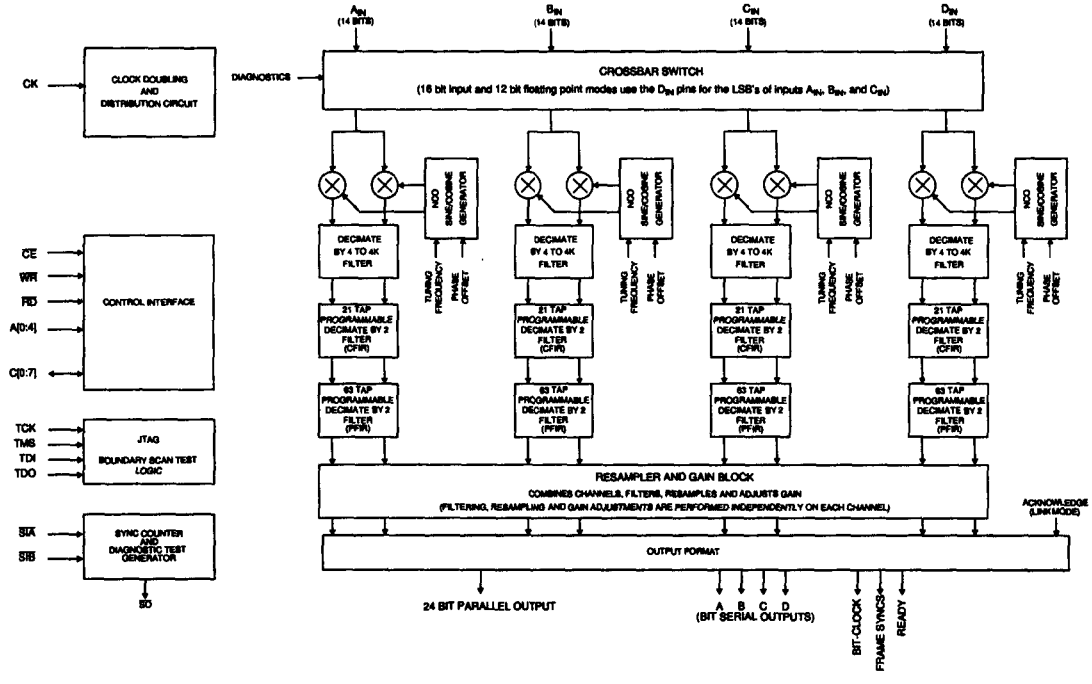

Figure 4.2: Block diagram of the GC4016 quad digital down-converter

The narrowband requirements stipulated in table 1.1 are easily achieved using a narrowband digital down-converter, such as the GC4016. A single A-D converter is used to sample a wide input bandwidth. The sampled spectrum is fed into each of the down-conversion channels. Each channel may be independently programmed to perform complex down-conversion, filtering and rate reduction of a narrowband signal contained within the sampled wideband spectrum. The basebanded outputs are fed to a DSP for baseband processing. Multiple GC4016 devices may be used to implement more than 4 narrowband channels, by feeding the outputs of the wideband A-D converter into each of their channel inputs.

The proposed architecture implementation realises a wideband receiver by processing 8 adjacent narrowband channels individually, using GC4016 narrowband down-converters. The digital down-converters are programmed to translate adjacent channelised bandwidths within the sampled wideband spectrum to baseband. FFT-based spectral analysis is performed individually on each of the narrowband basebanded outputs using a DSP. The resulting frequency-domain spectra are concatenated to form the final output bandwidth.

This method of generating wide bandwidth outputs by means of concatenating narrower bands may be inappropriate if subsequent narrowband time-domain processing (such as demodulation) is required to be performed on the wideband output. The reason for this is that narrowband signals may lie across two adjacent wideband output channels, making time-domain processing impossible. This could be overcome by sufficiently overlapping the output channels, at the expense of increased storage and processing requirements. In the wideband applications for which this receiver was targetted, much of the processing was performed in the frequency domain, and this limitation was not a concern.

While this method has the short-coming described above, it also introduces a number of advantages in spectral analysis applications:

- To analyse a particular bandwidth B at a sample rate F_s and a particular resolution R, an FFT of length N where

$$N \geq \frac{F_s}{R} \tag{4.1}$$

$$N \in \mathbb{Z} \tag{4.2}$$

  is required. The FFT is performed, and P points in the centre of the FFT contain the frequency content in the bandwidth B, where P may be found from:

$$P = \frac{B \cdot N}{F_s} \tag{4.3}$$

$$P \in \mathbb{Z} \tag{4.4}$$

By dividing the received bandwidth into S subbands, the analysis is performed using S FFTs of reduced length $\frac{N}{S}$. This results in a marginally increased computational speed, since the FFT algorithm is of order $N \cdot log_2(N)$. Windowing functions used to reduce FFT leakage are reduced in length by a factor of S, reducing the required storage capacity within the DSP by the same factor. This is of particular advantage in applications where longer polyphase windowing is used.

- The highly parallel architecture allows the output bandwidth to be increased up to the Nyquist bandwidth by increasing the number of narrowband channels. The solution is thus extremely scalable.

- The reduced processing gain which arises from a reduced FFT length is negated by the higher decimation, so the overall SNR improvement achieved through processing gain is preserved.

- The narrowband channels are perfectly matched in amplitude and phase, due to the repeatability of digital filtering. The channels use the same clock, and do not drift in frequency with respect to one another. An analogue wideband receiver implemented similarly would suffer from mismatch in adjacent channels and possible frequency drift.

The narrowband band merging technique for producing wide bandwidths is further described through the following example, which demonstrates the realisation of a 10 MHz output bandwidth at an IF of 12.8 MHz:

The discussion proceeds by determining the maximum output bandwidth which the GC4016 may achieve, for a given input sample rate. The GC4016 can operate at a minimum decimation of 32. The GC4016s FIR filter coefficients were optimised to achieve the widest bandwidth possible while maintaining a passband ripple of less than 0.5 dB and a stopband attenuation and SFDR of greater than 90 dB through the down-converter. A maximum output bandwidth of 79.5 percent of the output sample rate was achieved.

A sampling rate of 51.2 MSPS was chosen to sample the 10 MHz bandwidth at an IF of 12.8 MHz. This sampling rate is slightly reduced from the 65 MSPS that the AD6644 was designed to operate at, so similar performance is expected. The exact sampling frequency was chosen based on the shape factor of the digital filters within the GC4016 with minimal decimation and a stopband attenuation of 90 dB, as well as the number of narrowband channels used. The 12.5 kHz frequency resolution required for the wideband spectral analysis of the 10 MHz band dictates the length of complex FFT, according to equations 4.1 and 4.3. For an output bandwidth of 10 MHz and a

12.5 kHz resolution, 800 points are required in the passband. Assuming a maximum output bandwidth of 79.5 percent of the sample rate, a minimum FFT of length 1006 corresponding to an output sample rate of 12.57 MSPS would be required. This number is rounded to the next power of 2 to maintain an efficient length of 1024 for the FFT. The corresponding sample rate required is:

$$F_s = \frac{1024}{800} \cdot 10\,\text{MHz} \tag{4.5}$$

$$= 12.8\,\text{MSPS} \tag{4.6}$$

Two GC4016 devices (8 narrowband channels) are used to implement the wideband output. The 10 MHz output bandwidth is broken into 8 narrowband bandwidths of 1.25 MHz, each with a sample rate of 1.6 MSPS. Since the minimum decimation is fixed at 32, the sampling rate of the A-D converter should be 51.2 MSPS. 128 point FFTs must be performed on each basebanded output, with the middle 100 points of each FFT being concatenated to form the 10 MHz band. The centre frequencies of the S adjacent channels may be computed as follows:

$$f_c(n) = F_{IF} - \frac{B}{2} + (n + \frac{1}{2}) \cdot \frac{B}{S} \tag{4.7}$$

where

$$n \in [0, S-1] \tag{4.8}$$

$$n \in \mathbb{Z} \tag{4.9}$$

and F_{IF} and B refer to the IF centre frequency and IF bandwidth respectively.

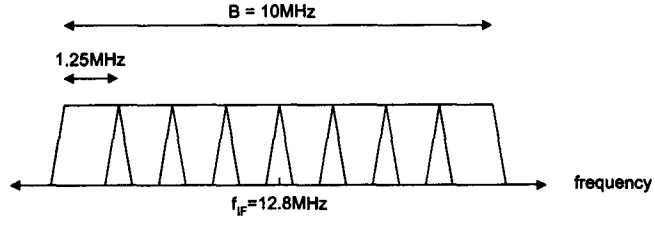

Figure 4.3: Adjacent narrowband channels used to form a wideband output.

Figure 4.3 demonstrates the method by which the wideband sampled spectrum is divided into 8 adjacent narrowband spectra.

4.2.4 A Description of the ADC-DDC Board Architecture

The ADC-DDC mezzanine module design was separated into two boards (figure D.4 in appendix D should be consulted for the physical layout of the boards). The A-D converter and analogue circuitry was placed on a separate circuit board to the digital down-converter (DDC) circuitry. The reasoning behind this was twofold:

- The DDC board is capable of accepting 16-bit inputs, while the AD6644 A-D converter has 14-bit resolution. By separating the two boards, the A-D converter could be upgraded without affecting the DDC circuitry. Essentially, the design is modular, allowing individual modules to be upgraded.
- Physical isolation of the digital and analogue circuitry is possible. This was considered to be useful in tracing the source of poor analogue performance in the form of spurious signals, should they arise. Possible sources of spurious, such as ground-loops, power supply ripple and digital interference could be identified.

A description of the A-D converter and digital down-converter boards follows:

4.2.4.1 A-D Converter Board Description

A block diagram of the A-D converter board is shown in figure 4.4. The analogue input signal enters the board through the IF input, which matches the source impedance with a 50 Ω input impedance for optimal power transfer and minimal noise. An optional mezzanine filter module which may be mounted on the ADC board may be used to provide analogue signal conditioning in the form of bandpass filtering or fixed gain between the analogue receiver and the AD6644. Matching of the analogue input signal level to the A-D converter is further described in section 5.1. The signal is then passed through a final anti-aliasing filter and resistive matching pad, before being combined with a dither signal. The dither signal level may be dynamically adjusted via an I^2C serial interface to a digital-to-analogue converter (DAC) controlling the gain of a programmable gain amplifier. Section 5.2 provides further details of the dither circuit implementation. The combiner output is routed to an RF transformer with a 1 : 16 impedance ratio, before being passed into the AD6644 differential input. The RF transformer accomplishes the following:

- It converts the single-ended signal into a differential signal that is required by the AD6644.

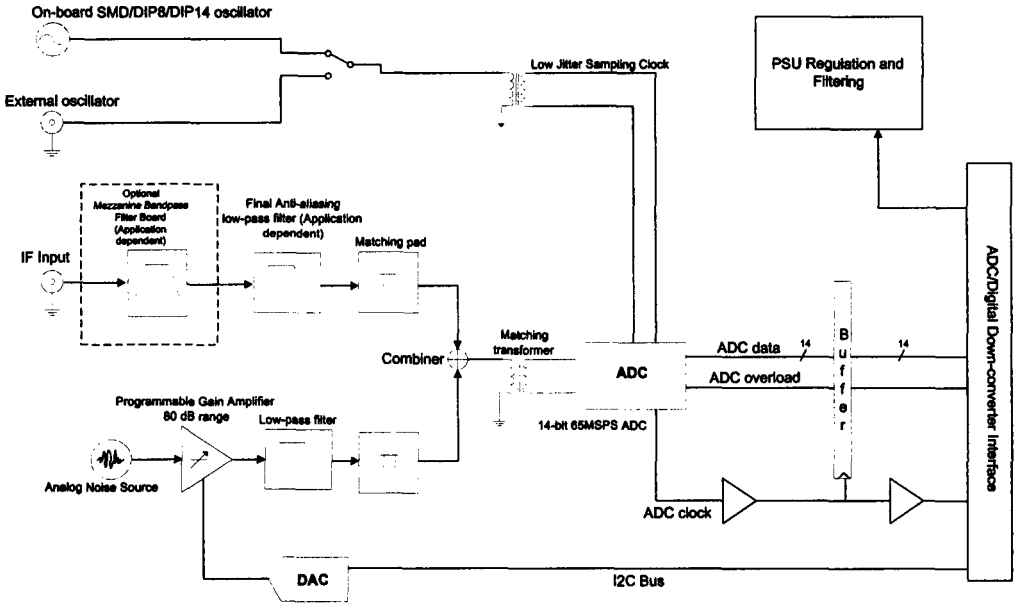

Figure 4.4: Block diagram of the A-D Converter board.

- It matches the 50 Ω output of the combiner to the high impedance (ca. 1kΩ) input of the AD6644. The transformer impedance ratio is 1 : 16, and therefore expects an 800 Ω load on the secondary side. The input impedance of the AD6644 is reduced to 800 Ω through appropriately chosen resistors placed across the differential input.
- It assists in biasing the differential A-D converter analogue input around 2.4 V.

The A-D converter may receive its sampling clock from either an external source or an on-board low jitter oscillator. A common external source is required when synchronous sampling on multiple boards is required. Further detail of oscillator selection is discussed in section 5.3. The two's complement 14-bit digitised samples are buffered before being passed to the DDC board, along with an A-D converter overload detect signal and A-D converter output clock.

4.2.4.2 Digital Down-converter Board Description

Figure 4.5 illustrates the architecture of the digital down-converter board by means of a block diagram. The A-D converter data bus enters the board via the ADC/DDC interface, and is aligned with the upper 14 bits of the 16-bit input bus. The remaining

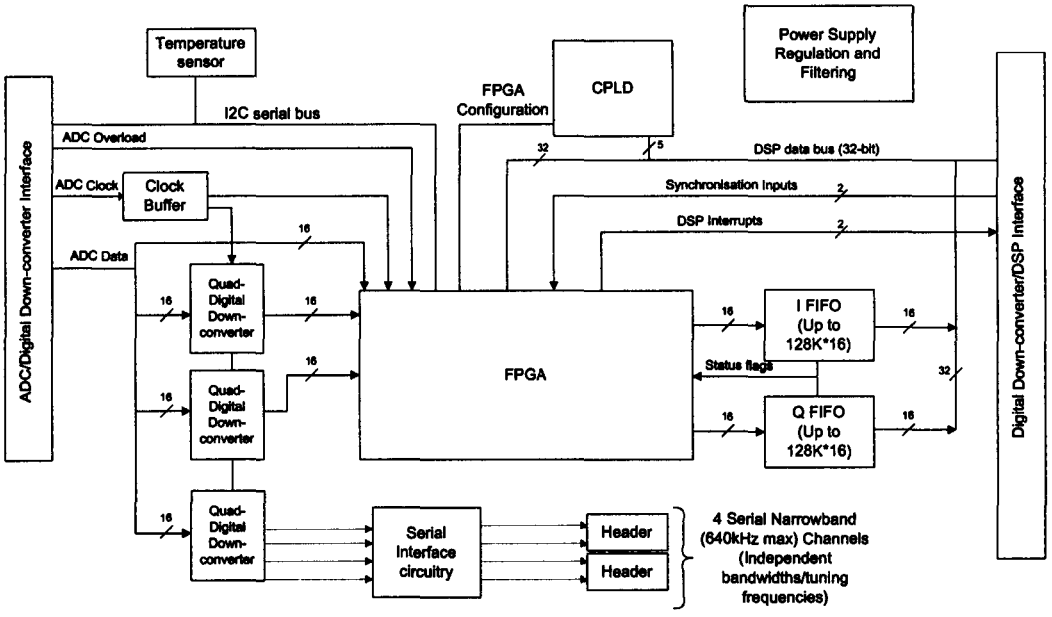

Figure 4.5: Block diagram of the digital down-converter board.

two least-significant bits are grounded on the ADC board[2].

The 16 bit input bus is routed to three GC4016 four-channel digital down-converters. The GC4016s are used to perform complex down-conversion, decimation by factors of 32 to 16384, FIR filtering and optional spectral inversion. Two of the GC4016 devices are configured to output the complex samples from all four internal down-conversion channels on a parallel 16-bit bus, using time division multiplexing. The parallel output facilitates high speed transfer of the samples to the DSP on the ISA baseboard. The remaining GC4016 is configured to output each channel on a separate serial output, with a maximum bandwidth of 640 kHz per channel. The serial output is compatible with the ADSP-21160 DSP's serial port, and the serial channels may run at different output rates.

The A-D converter's wideband output may thus be used for wideband spectral analysis (up to 10 MHz), using the two parallel output GC4016 devices. The third GC4016 may simultaneously extract narrowband signals from the wideband sampled output, and pass them on to digital signal processors for subsequent demodulation at baseband. Alternatively, all twelve channel may be used for narrowband extraction of signals

[2]While it is permissible to increase signal path resolution by grounding the least significant bits on the wider bus, decreasing signal path resolution by means of truncation results in signal distortion, and a rounding algorithm is necessary.

sampled by the A-D converter.

The digital down-converters are highly programmable, requiring that over 1000 registers are appropriately configured. Configuration is performed through a control bus (not illustrated) that is memory mapped on the DSP's external bus. The DSP is thus able to reconfigure the digital down-converters on demand.

The parallel outputs of the digital down-converters are routed into an FPGA, where the samples are sorted into I and Q streams. This allows for efficient processing in the DSP, by taking advantage of its single instruction multiple data (SIMD) mode. The sorted 16-bit I and Q samples are written to separate 16-bit first-in-first-out (FIFO) memories, which vary in depth from 8 to 128 kWords. The FIFO memory facilitates the rate change between the GC4016 output rate and the DSP external bus and allows the DSP to efficiently process blocks of data at a time. In a single-channel wideband receiver, the FIFO status flags are routed to the DSP interrupts to signal that sufficient samples are available to perform block processing of data. The FIFO status flags may be programmed to any required level, allowing for flexibility in the block processing size.

The 16-bit I and Q FIFO outputs are aligned to the upper and lower 16 bits of the 32-bit ADSP-21160 processor's external bus respectively. The DSP's external bus is routed onto the digital down-converter board via the digital down-converter/DSP mezzanine interface. The FIFOs are memory mapped on the DSP's external port. The DSP may thus read an I-Q pair out of the FIFO with each 32-bit access to the FIFO address. The DSP's DMA controller allows the samples to be efficiently read into the DSP's internal SRAM memory while processing continues on a previous block of data. The entire sample capture and processing operation may thus be pipelined.

A non-volatile CPLD is used to assist the DSP in configuring the on-board FPGA, and provides high speed combinational logic where necessary (such as high speed address decoding for the high speed FIFO accesses).

The following logic was implemented in the volatile FPGA:

- Sorting of the GC4016 TDM outputs into I and Q data streams. This was achieved with a two clock cycle pipeline delay from input to output.
- Synchronisation of the I-Q sample streams, to ensure that they are written into the FIFO memory in such a manner that they can be read out predictably. Although the I and Q samples from each of the eight channels follow a predictable sequence, no tagging or labelling is used to distinguish between the samples as they are written into the FIFOs. It is therefore imperative that the first sample written into the FIFO after it is reset or cleared is always the same sample from

the same channel.

- Selection of FIFO data source via a memory-mapped register on the DSP's external bus. The A-D converter output data bus is routed into the FPGA. This allows the A-D samples to be written directly into the FIFO buffers, bypassing the digital down-converters. This is useful for evaluating A-D converter performance, as well as providing a method of diagnosing board faults. A register is used to specify whether the FIFOs receive samples from the A-D converter, the digital down-converters, a FIFO flag programming register (used to configure the partially empty and partially full flags) or a constant valued source (useful for diagnosing board faults).

- Decoding of external synchronisation pulses. In a multi-channel receiver, A-D converter sampling clocks and digital receiver synchronisation pulses are generated on a single timing distribution board. The sampling clock and synchronisation signals are distributed to each of the digital receiver boards. Various pulse types are transmitted through the same synchronisation line, and must be decoded separately. The decoded pulses are used to synchronise the GC4016 down-converter channels and FIFOs on multiple boards, providing support for phase-synchronous data acquisition.

- Selection and enabling or disabling of a DSP interrupt source via a memory mapped register on the DSP's external bus. The DSP may be interrupted by a decoded synchronisation pulse (multi-channel receiver) or one of the FIFO status flags, to indicate that data is ready for processing.

- An I^2C bus controller (master) interface. This allows access to I^2C devices, in particular the DAC used to set the dither level, and an on-board temperature sensor. The I^2C bus controller control registers are memory-mapped on the DSP's external port.

- Address decoding for the internal and external memory-mapped registers.

Two switched-mode DC-DC converters were designed to generate the 5 V and 3.3 V power supplies for the analogue[3] and digital circuitry respectively. These were preferred over linear regulators due to their high efficiency, and therefore lower power dissipation. Power dissipation was of particular concern, since the digital receiver boards are enclosed in shielding to reduce electromagnetic interference (EMI). This reduces the effectiveness of the forced air cooling that is provided in the enclosure.

[3]The AD6644 is considered an analogue component, despite the fact that it produces a digital output.

4.2.5 A Description of the ISA DSP Board Architecture

In the digital receiver context, the processor on the ISA DSP board is responsible for processing the digitised, basebanded received signal.

Figure 4.6 is a block diagram of the ISA adapter board.

The Analog Devices ADSP-21160 was selected as the general-purpose signal processor which would reside on the ISA adapter board. The ADSP-21160 is a 32-bit floating point DSP which operates at an internal clock rate of 80 MHz and an external bus clock rate of 40 MHz. The DSP contains two parallel processing elements, which allows it to execute up to three instructions on two separate data streams in parallel, when configured to operate in single instruction multiple data or SIMD mode. The processor features 4 Mbits of internal SRAM, 6 link ports for dedicated high-speed inter-processor communication and two full-duplex serial ports. The processor supports emulation via a JTAG-compliant interface.

The DSP's external bus is routed to mezzanine board sites, marked M0, M1 and M2 in figure 4.6. The mezzanine board sites allow for application-specific hardware to be interfaced to the processor's external port. The ADC-DDC module is interfaced to the processor via the M2 site. M0 and M1 are typically used to interface to external SRAM and SDRAM memories or application specific peripherals.

Code is typically downloaded to the DSP from the host processor via the ISA bus, which is interfaced to the DSP's host port interface. The ISA bus is interfaced to the board via a CPLD, which is used to perform signal buffering and board address decoding. It further aids in the initialisation of the on-board FPGA.

The ISA adapter board's on-board FPGA acts as a general controller for the board. It is responsible for performing the following functions:

- Address decoding.
- Interfacing of the ISA bus and the DSP's external port.
- Mapping of module site interrupts to the DSP external interrupts.
- Routing of external synchronisation to mezzanine module sites. (This is used to provide the ADC-DDC module with external synchronisation.
- Interfacing the ISA bus to an I^2C serial bus to support I^2C devices, specifically a temperature sensor and serial flash device used to store board configuration details.

- Doorbell registers which, when written to, allow the host processor to interrupt the DSP or the DSP to interrupt the host processor.

The DSP is able to communicate with analogue receivers via two serial interfaces that are RS232 and SSI (serial synchronous interface) compliant respectively.

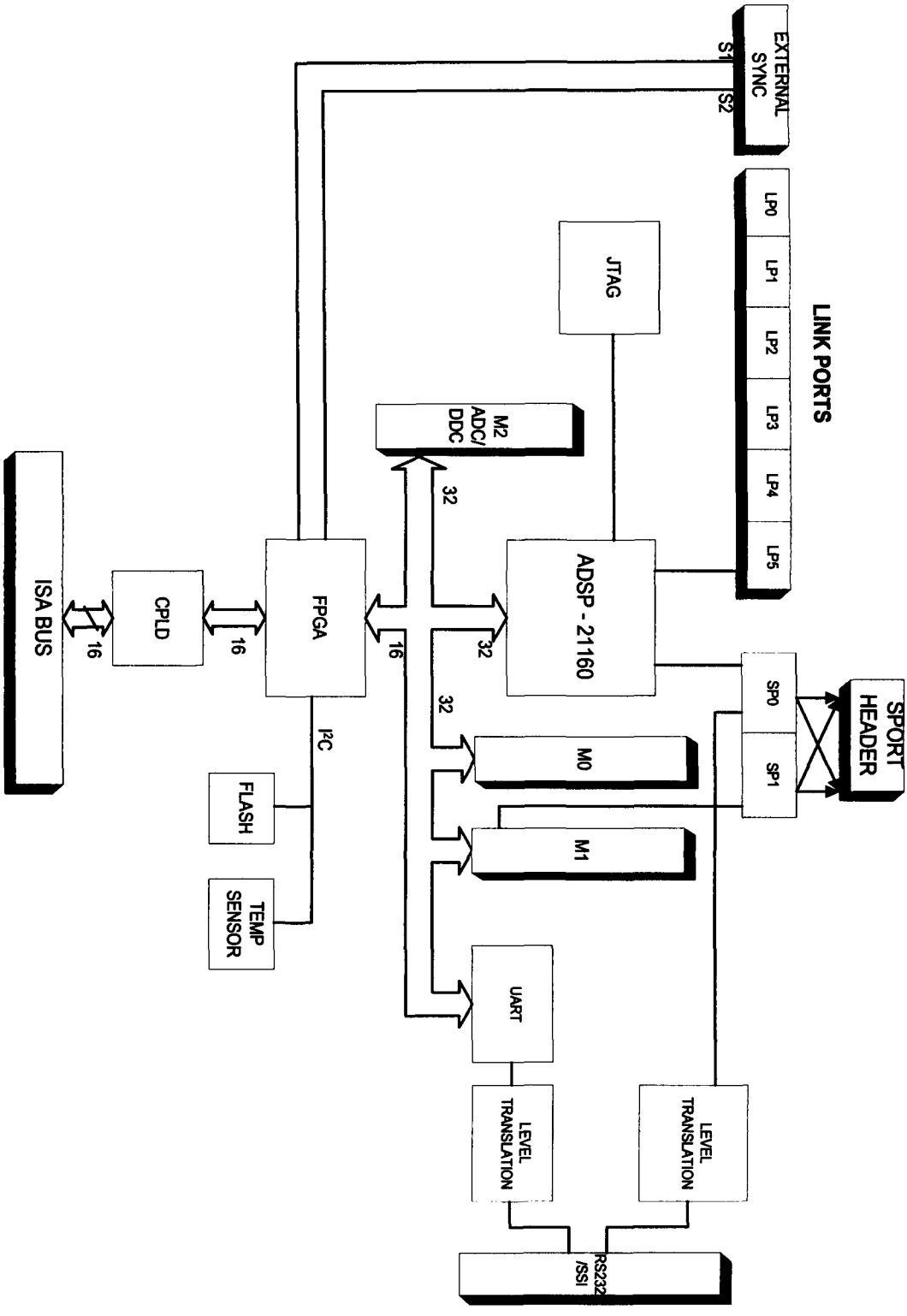

Figure 4.6: Block diagram of the general purpose ISA-based DSP card.

Chapter 5

Digital Receiver Implementation

This chapter describes some of the issues that were taken into consideration in the design of the wideband digital radio receiver. The chapter is not intended to be a complete account of the receiver design, but serves to highlight some of the key issues and problems encountered.

5.1 A-D Converter Input Level Matching

In section 2.6 it was demonstrated that in order to design for an optimal combination of receiver dynamic range and noise figure, the designer should treat the A-D converter as part of the analogue receiver chain. The optimal combination of sensitivity and dynamic range for a particular application may then be used to specify the required performance of the analogue receiver chain.

The specifications of this project, in contrast, required that the digital receiver should be interfaced to existing analogue receivers. The interface between the analogue receiver and the A-D converter could therefore not be optimally designed. The minimum linearity required of the analogue receiver, however, was estimated as follows:

The AD6644 requires a full scale input power of 2.2 V peak-to-peak across an 800 Ω input resistance. This translates to a power requirement of -1.63 dBm. After accounting for the losses incurred through the RF transformer, combiner, anti-aliasing filter and matching pad, the maximum input power presented to the digital receiver was found to be +3.37 dBm.

For two-tone third order intermodulation (IM3) measurement, the test tones are re-

quired to be at -7 dBFS to prevent saturation of A-D converter. This translates to a power level of -3.63 dBm at the input. Equation 2.29 is then used to determine the third order intercept required of the analogue receiver, such that a particular level of SFDR is met. By way of example, an 80 dB dynamic range at an output power of -3.63 dBm requires an output IP3 of +36.37 dBm from the analogue receiver.

The IP3 of one of the analogue receivers did not meet the required intermodulation performance. A matching module was developed, which consisted of a high linearity amplifier ($IP3 \geq 45$ dBm) with sufficient gain (20 dB) to minimise the contributions of the preceding analogue circuitry to the overall third-order intercept point of the analogue receiver, as discussed in section 2.6.1. The module was successful in improving the overall analogue receiver IP3 such that the required specification of 80 dB two-tone SFDR was met.

5.2 A-D Converter Input Signal Dithering

Dithering is implemented prior to A-D conversion. The AD6644 A-D converter has a three stage pipelined architecture, with converter stage resolutions of 5, 5 and 6 bits respectively. Poor linearity is therefore expected at levels of $-20 \cdot log_{10}\left(2^5\right) = -30.1$ dBFS, according to the discussion in section 2.5.2.3, when a single tone is applied to the A-D converter input. This is confirmed by consulting figures 15 and 21 in [3]. According to figure 21, a region of poor linearity exists for single tone analogue inputs with a level of -20 dBFS to -30 dBFS. It is therefore expected that dithering at a level of -20 dBFS will improve the average linearity of the A-D converter.

The dither circuit was implemented using an NC202 wideband noise diode, capable of generating wideband white gaussian noise at a level of 0.1 $\mu V/\sqrt{Hz}$. The dither noise was amplified by means of a programmable gain amplifier to a maximum level of -20 dBFS. An amplifier capable of meeting the 50 dB required amplification was selected. A lowpass elliptic filter was designed in order to limit the noise bandwidth to 500 kHz. The noise was thus placed outside of the IF input frequency range. As a result, the dither noise is subsequently filtered by the digital filtering stages in the digital down-conversion process, and therefore has a negligible effect on the receiver signal-to-noise ratio. The dither noise is effectively subtracted (*cf.* subtractive dither) through the digital filtering.

The added noise reduces the receiver's dynamic range, and dynamic dither level control (by means of PGA output level adjustment) may be used to reduce the dither level when appropriate.

5.3 Selection of a Sampling Oscillator

Sampling oscillator performance is a critical factor in ensuring that high-speed, high dynamic range A-D converters perform well. Section 2.3.3 demonstrated the impact of oscillator time domain jitter (or the related frequency measure of phase noise) on the SNR of the A-D converter.

At this point it should be noted that jitter may be classified as *random* jitter, or *pattern-dependent* jitter (also referred to as *flanging*)[2]. The equations mentioned in section 2.3.3 apply to random jitter. The former usually results from random noise internal to the oscillator, while the latter usually results from oscillator sub-harmonics. Oscillators that exhibit sub-harmonics should be avoided, since the non-stochastic nature of the sampling timing error may result in spurious content in the sampled signals.

In a wideband scanning receiver, the processing gains achieved through decimation filtering and FFT result in an increase in the SNR. This may be understood in terms of noise bandwidth as follows: The received bandwidth is effectively reduced to the bin resolution of the FFT (the decimation must be taken into account when evaluating the FFT frequency resolution). The bandwidth reduction (through the filtering actions of the decimation and FFT) reduces the noise bandwidth, which results in a reduction in noise power. This is analogous to analogue receivers, where channelisation filtering reduces the noise bandwidth.

The 10 MHz bandwidth receiver is used by way of example: A decimation factor of 32 in each channel was used to achieve the 10 MHz bandwidth. This translates to a processing gain (SNR improvement) of approximately 15.05 dBm, according to equation 3.22. The full processing gain may only be achieved if the reduced noise is greater than the quantisation noise in the decimated channel. The 128-point complex FFT performed on each channel achieves a processing gain of 21.07 dB. The total processing gain is thus 36.12 dB. Under the assumption that the receiver noise is dominated by noise generated in the A-D converter, the maximum A-D converter noise that will ensure an 87 dBFS dynamic range (80 dB dynamic range under two-tone intermodulation test conditions, which requires that each tone has a maximum amplitude of -7 dBFS) is therefore $36.12 - 87 = -50.88$ dBFS. The maximum signal frequency which may appear in the 10 MHz band centered at 12.8 MHz is $12.8 + (10/2) = 17.8$ MHz. Equations 2.16 and 2.14 may then be used to find the corresponding jitter, using the parameters listed in table 5.1. The parameters used in table 5.1, obtained from the AD6644 data sheet[3] and the above reasoning, result in an encode clock jitter value of 25.5 ps. This is thus the upper limit on oscillator jitter that should be specified. It is further noted that this is a rather relaxed speci-

SNR_{dB}	50.88 dB
f_a	17.8 MHz
ε	0.75 LSB
N	14
V_n	2.5 LSBs
T_a	0.2 ps

Table 5.1: Parameters used in the calculation of oscillator jitter.

fication for clock jitter[1], and it is therefore likely that many commercially available oscillators would meet this specification. It was not possible to obtain an oscillator characterised with adequate jitter specifications due to poor availability in small quantities. Empirical testing was therefore used to verify that oscillators that were more readily available, but were uncharacterised for jitter, would meet or exceed this (relaxed) jitter requirement. The empirically tested oscillators were found to meet the jitter requirements at these analogue input frequencies, as will be shown in chapter 6.

As a further note, the spurious and SNR performance of the AD6644 is related to sampling clock output power, as may be seen in figure 22 in the AD6644 datasheet[3]. An oscillator that could supply 5 dBm was therefore used to optimise the A-D converter performance.

In synchronous multichannel system design, care should be taken in the design of a sampling oscillator distributed to multiple A-D converters, since buffers placed after the oscillator result in increased jitter at the A-D encode input.

5.4 Analogue Power Supply Filtering

As mentioned previously, a DC-DC converter was used to provide the analogue voltages for the A-D converter and analogue circuitry, in order to improve power efficiency and reduce power dissipation that could result in overheating. Switching regulators introduce switching ripple into the power supply, and care must be taken to ensure that the ripple noise generated by the system ATX power supply and the switching regulator does not negatively impact on the A-D converter performance. Since the switching ripple is periodic, it may introduce spurious signals in the A-D converter output. The buck mode switching regulator was selected to operate at a high switching frequency (500 kHz), generating a peak switching ripple of 65 mV. A high switching frequency was deliberately chosen to reduce the physical size of components required to filter

[1]Low jitter oscillators under consideration boasted jitter specifications of 5 ps or less.

the regulator output. The AD6644's power supply rejection ratio (60 dB) was used as a basis to design a low-pass power supply filter which could provide sufficient attenuation such that switching ripple voltages of 100 mV peak-to-peak were attenuated to levels smaller than -120 dBFS (2.2 μV) at frequencies greater than 100 kHz.

5.5 Grounding

Due to the separation of the A-D converter and digital down-converter circuitry onto two separate PC boards, the analogue and digital circuitry was located on two separate ground planes. Careful consideration was given to the physical layout of the board in order to minimise the coupling of the sampling clock and digital signals to the analogue input signal, which may introduce fixed-frequency spurious signals that limit the receiver SFDR. This was achieved by:

- Physical separation to improve isolation between sensitive signal traces and signals traces that were considered aggressors.
- Use of a ground plane as isolation between sensitive traces and aggressor traces.
- Where possible, ground return current loops were physically separated between sensitive and aggressor traces.
- The high-speed digital interface (A-D converter output bus) between the A-D converter and digital down-converter boards contained sufficient low impedance ground connections to ensure that return currents flowed through the connector rather than through other ground return paths which may have resulted in ground loops.

5.6 EMI Shielding

The digital receiver circuitry resides in the non-ideal environment, in terms of electromagnetic radiation, of the 19 inch, 4U enclosure. Switching power supplies and processors running at high frequency exhibit high levels of electromagnetic radiation, as was observed with a close-field probe connected to a spectrum analyser. Electromagnetic shielding, in the form of metal shielding covers, was therefore used to reduce the susceptibility of the analogue circuitry to electromagnetic interference (EMI).

Due to the fairly high power dissipation of the AD6644 and GC4016 devices, it was decided that it was necessary for the shielding cover to contain holes in order to improve the air circulation over the digital receiver circuitry. The aperture of the holes was designed to be less than $\frac{\lambda}{20}$ of the highest frequency that should be prevented from passing through the shielding, where λ refers to the wavelength corresponding to that frequency. The highest frequency was chosen to be 1.5 GHz, substantially higher than the AD6644's analogue input bandwidth of 250 MHz [3].

5.7 GC4016 Decimating Filter Coefficients

Each GC4016 digital down-converter consists of a quadrature NCO followed by a 5th order CIC filter which may be programmed to decimate by factors of 8 to 4096, and two subsequent stages of programmable FIR filtering with 21 and 63 filter taps respectively. Each filter stage decimates the complex signal by a further factor of two. The coefficients for the first FIR filter (CFIR) stage were chosen to compensate for the droop in the CIC filter's passband.

In order to achieve a 90 dB SFDR, the digital down-conversion was required to ensure that out-of-band signals would not alias into the passband of a particular down-converter channel at levels greater than -90 dBFS. The second FIR filter (PFIR) stage coefficients were designed to achieve the widest passband possible, while ensuring that the filter attenuated all out-of-band signals and aliasing by greater than 90 dB. Aliasing results from the CIC and FIR decimation, as described in chapter 3. An optimiser was developed under the MATLAB environment which achieved a maximum output bandwidth of 79.5% of the final output rate, while meeting the attenuation and passband ripple requirements. The motivation for optimising the filter coefficients was the realisation that the 14-bit filter coefficients were not of sufficient resolution to design a filter of desired output bandwidth using standard filter design techniques. Preliminary filter designs which used the Parks-McClellan optimal equiripple FIR filter design methodology resulted in inadequate performance when the filter coefficients were rounded to 14 bits.

Appendix B contains plots of the magnitude and phase response of the CIC and FIR filters for each channel, for the 10 MHz wideband (decimate by 32) case with a sampling frequency of 51.2 MHz.

The magnitude and phase response of the CIC filter is shown in figure B.1. Aliasing occurs around each of the nulls, as described in section 3.3.4.2.

Figure B.2 shows the magnitude and frequency response of the CFIR filter, interpo-

lated to the sampling rate. Careful examination of the filter passband shows that the passband edge is emphasised. This emphasis compensates for the droop in the CIC filter's passband. Figure B.3 shows the combined response of the CIC and CFIR filter. The effect of the compensation may be seen in the filter passband, which is flat.

Figure B.4 shows the magnitude and phase response of the PFIR filter, interpolated to the sampling rate. The 63-tap filter achieves a worst-case stopband attenuation of 88 dB. Figure B.5 shows the combined response of the CFIR and PFIR filters, interpolated to the sampling rate.

Figure B.6 finally shows the combined response of the CIC, CFIR and PFIR filters, interpolated to the sampling frequency. The combined response of the three filters may be seen to have suppressed all out-of-band signals by more than 90 dB.

5.8 Problems Encountered during Receiver Design

This section briefly lists the problems encountered in the design of the digital radio receiver.

5.8.1 Insufficient EMI Suppression

Careful consideration was given to eliminating sources of electromagnetic interference by means of metal shielding covers, as described in section 5.6. Despite efforts in this regard, EMI was found to be a problem on boards placed in the slot adjacent to the SBC. A close-field probe was used to identify the source of the electromagnetic radiation: extremely high levels of radiation emerging from the SBC's on-board switch-mode power supply and Pentium processor. Both sources were in close proximity to the analogue section of the digital receiver and produced radiation of correct frequency content to result in in-band spurious.

An immediate solution to the problem was to introduce further isolation by physical separation of the SBC from the digital receiver boards. The slot adjacent to the SBC was therefore left vacant, and the problem was sufficiently reduced. It was noted that if this slot were to be required in future systems, the EMI shielding would need to be improved.

5.8.2 Problems due to Faulty Silicon

The design began at a time when some of the key devices were still in pre-release stages. The AD6644, GC4016 and ADSP-21160 in particular were pre-production silicon. As a result, the silicon contained more than 40 anomalies, some of which had not been identified by the manufacturers when the receiver design commenced. In particular, the following silicon bugs were found to be most problematic:

- The ADSP-21160 clock PLL is not guaranteed to reset correctly, leading to unpredictable device behaviour. A workaround was provided by the manufacturer, which required an awkward stopping and starting of the clock with timing constraints while holding the device in reset.
- The ADSP-21160 asynchronous host writes fail if the rising edge of the write strobe is relatively coincident with the rising edge of the internal core clock. The data is written to the wrong address, which results in the DSP hanging. The result was that the DSP could not be booted through its host interface. The manufacturer was assisted to reproduce and characterise this problem and design workarounds were developed.
- Numerous problems were encountered when running the ADSP-21160 link ports at full speed due to silicon bugs. The link ports thus had to be operated at half speed to ensure reliable data transfer.
- The GC4016 silicon had a bug in the NCO circuitry that resulted in poor SFDR (less than 60 dBFS) when down-conversion was performed at any frequency other than $\frac{f_s}{4}$. As a result, all testing was performed at 12.8 MHz until updated silicon became available.
- The output synchronisation circuitry on the GC4016 did not function according to the documentation. As a result, the start of frame strobe did not correctly identify the start of a frame of 4 complex sample pairs on the GC4016 parallel output. External logic was required in order to generate a valid start of frame pulse. The manufacturer subsequently updated the documentation to more accurately reflect the actual device functionality.

Chapter 6

Performance Measurements

This chapter describes the methods and results of empirical testing performed on the digital receiver. The performance of the A-D converter and analogue circuitry was initially tested in isolation by by-passing the digital down-converter circuitry. Subsequent testing was performed through the digital down-converters, showing performance in the 5 MHz IF (800 kHz bandwidth) and 12.8 MHz IF (10 MHz bandwidth) modes respectively.

6.1 Empirical Testing of A-D Converter and Analogue Front-End Circuitry

This section describes the testing of the AD6644 A-D converter and analogue input circuitry in isolation. The tests were performed by placing the digital receiver in a mode which by-passed the digital down-converters. The AD6644 output samples were routed directly into the 32k FIFO memories. The FIFOs were allowed to fill with 16k of data points, before the data was read out by the DSP. The data was then relayed to the host SBC for subsequent analysis through a Blackman-windowed FFT.

6.1.1 Non-harmonic Spurious Free Dynamic Range

Testing was performed on the digital receiver with the analogue input terminated in 50 Ω (matched to input impedance). The test aimed to determine the presence of any fixed-frequency spurious signals generated on the board, and the extent to which they limited the spurious-free dynamic range of the digital receiver. Potential sources of

conducted and radiated spurious signals include the sampling clock oscillator, digital signals, power supply switching noise and ground loops.

Figure C.1 shows the output of the A-D converter from DC to Nyquist. Averaging was performed on the 16k FFT output in order to reduce the noise variance, such that fixed frequency spurious was emphasised. Band-limited dither noise can be identified in the band from DC to 500 kHz. The remainder of the noise floor may be seen to lie at approximately -113 dBFS. This agrees closely to the -74 dBFS noise level quoted in the AD6644 data sheet, when the 42 dB of processing gain introduced by the 16k FFT is taken into account, indicating that the on-board noise is dominated by the AD6644 noise.

Fixed frequency spurious signals may be identified above the noise floor. The peak spurious is lower than -100 dBFS over the entire Nyquist band, and therefore meets the design requirements for all the intended receiver modes. The noise generated internally in the AD6644 (as well as by the dither circuit, when active) is sufficient to act as small-scale dither, allowing the converter to see well below the 84 dB dynamic range that the AD6644's 14 bits provides, when averaging in the form of decimation or FFT processing follows the digitisation. Since the noise is not regulated to be 1RPDF dither, the quantisation error is not guaranteed to be uniformly distributed and independent of the input signal, although in practice the noise is seen to be uniformly distributed, and is uncorrelated with the input signal.

6.1.2 Harmonic Spurious Free Dynamic Range

Figure 6.1 shows the test setup used to determine the spurious-free dynamic range of the AD6644 as limited by spurious signals that are harmonically related to the frequency of a signal at the analogue input. A signal generator is used to inject a single tone into the receiver's analogue input. A filter with a stopband attenuation of greater than 90 dB is positioned between the signal generator and the device under test (DUT), in this case the digital receiver, such that harmonics arising from the signal generator are sufficiently filtered out. Any harmonics exceeding -90 dBc are therefore related to non-linearities on the board (A-D converter or analogue input circuitry), rather than the test equipment.

It is common practice to test single tone converter performance at -1 dBFS at the converter input[3]. The results of placing a signal of -1 dBFS amplitude at a frequency of 7.6 MHz are shown in figure C.2. A lowpass filter with a 10 MHz cut-off was placed between the signal generator and the receiver input. It is noted that for this particular plot, spurious signals did not exceed -90 dBFS. Tests were not performed over the full Nyquist range of the converter, due to a lack of availability of filters with adequate

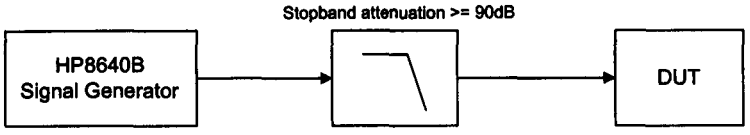

Figure 6.1: Test setup for harmonic spurious performance measurement.

stopband suppression.

More comprehensive testing was performed in each of the receiver operating bands, and is presented in sections 6.2 and 6.3 respectively.

6.1.3 Effect of Band-limited Dither Noise on A-D Converter Linearity

This section aims to measure the effect of the dither noise circuitry on the A-D converter linearity. The test setup used in section 6.1.2 was used to place a test signal of amplitude -30 dBFS at an arbitrarily chosen frequency of 7.6 MHz. The -30 dBFS amplitude was specifically chosen to exercise the region of poor linearity in the AD6644's transfer function resulting from its multi-stage architecture.

Figure C.3 shows the resulting spectrum when dither noise is disabled. Spurious signals are visible throughout the Nyquist band, with peak levels recorded at -85 dBFS. Figure C.4 shows the effect of adding band-limited dither noise to the A-D converter's analogue input. The spurious signals resulting from poor converter linearity are dramatically reduced, with the peak spurious level recorded at -97 dBFS. A comparison with figure C.1 shows that many of the remaining spurs are not harmonically related to the input signal, but result from spurious generated on the board.

6.2 Empirical Testing of the Digital Receiver at 5 MHz IF

This section presents the results of tests performed on the digital receiver while operating in the 5 MHz IF, 800 kHz wideband receiver mode, with a resolution bandwidth (FFT frequency resolution) of 1 kHz. The 800 kHz bandwidth was realised by concatenating eight 100 kHz bands. Each of the GC4016 channels was configured to

decimate by a factor of 400, resulting in an output sample rate and output bandwidth of 128 kSPS and 100 kHz per channel respectively. Band-limited dither noise at approximately -20 dBFS was present during all testing of this receiver mode.

6.2.1 Non-harmonic Spurious-free Dynamic Range

Testing was performed on the digital receiver with the analogue input terminated in 50 Ω. Decimation by a factor of 400 resulted in a processing gain of approximately 26 dB, which was sufficient to reduce the level of the noise floor to -100 dBFS. The reduced noise level was too small to be represented in the 96 dB resolution available at the 16-bit GC4016 outputs. As a result, the FFT output was zero-valued, and is therefore not plotted. This peculiarity is further illustrated in section 6.2.2.

6.2.2 Harmonic Spurious-free Dynamic Range

The test setup shown in figure 6.1 was used to evaluate the single-tone SFDR of the digital receiver. A lowpass filter with a 6 MHz cut-off was used between the signal generator and the receiver input. A signal corresponding to a level of -1 dBFS at the A-D converter input at a frequency of 5.15 MHz was placed on the digital receiver input.

The resulting spectrum is shown in figures C.5 and C.6, which shows the average and peak spectral power estimations respectively. The lack of noise floor described in section 6.2.1 may be seen in the seven down-converter channels that contain no signal. A noise floor is present in the channel that contains the signal. This is expected, since the output of this channel is sufficiently large to be represented by the 96 dB dynamic range, and therefore contains quantisation noise.

6.2.3 Two-tone Third-order Intermodulation Distortion Measurement

Intermodulation distortion products arise as a result of the mixing of two or more input signals of different frequencies within a device. The mixing results from non-linearity in the device's transfer function. For signals with fundamental frequencies f_1 and f_2 presented to the input of a device with a degree of non-linearity in its transfer function, intermodulation products will arise at frequencies of [13] $nf_1 + mf_2$ where $n, m = 0, \pm1, \pm2, \pm3...$ and the order of the resultant intermodulation products is defined as

[13] $i = |n| + |m|$. Third-order intermodulation distortion is of particular concern, since the distortion products fall at frequencies of $2f_1 - f_2$ and $2f_2 - f_1$. For closely spaced signals within the bandwidth of a wideband receiver, the intermodulation products often fall in-band, reducing the receiver's SFDR.

In analogue components, the level of third-order intermodulation distortion may usually be reliably predicted for any output power using equation 2.28, once the third order intercept point (a measure of third order non-linearity) has been determined. This is usually not true for sub-ranging A-D converters, where regions of poor linearity may be localised to a particular input power range (such as the -20 dBFS to -30 dBFS range discussed in 5.2).

The two-tone third-order intermodulation test requires that two equal-amplitude signals are placed at the input of the device under test (DUT). When testing A-D converters, it is conventional to set the amplitude of each signal to a level of -7 dBFS at the A-D converter input[3]. Figure 6.2 shows the test setup that was used to perform two-tone third-order intermodulation testing.

The test setup consists of two signal generators which are used to generate the two input tones. Amplifiers follow the signal generators to provide isolation between the signal sources, since inadequate isolation may result in inaccurate measurements [19]. Filters with a stopband attenuation of 90 dB follow the amplifiers. The cut-off frequency of the filters was chosen to attenuate second-order and higher-order harmonics generated by the signal generators and amplifiers, which may negatively affect the results of the intermodulation test. The filtered signals are combined, before being amplified by 30 dB using highly linear amplifiers and placed on the input of the DUT. The linearity of the output amplifiers is of particular importance, due to the high output power (-7 dBFS at the A-D converter input or -3.63 dBm at the digital receiver input) required.

The output IP3 of the test setup was calculated at +42 dBm, according to equation 2.27. Equation 2.29 was used to calculate the two-tone dynamic range of the test setup, which was found to be -87.63 dBc at the -3.63 dBm output level. The test setup performance was verified by replacing the digital receiver with a spectrum analyser, and measuring the two-tone dynamic range. The two-tone dynamic range of the test setup was measured as -85 dBc. The test setup thus limits the measurement of two-tone dynamic range to no better than -85 dBc.

The intermodulation distortion for the 5.1 MHz IF mode was measured by placing two signals at frequencies of 4.9 MHz and 5.1 MHz respectively. Third-order intermodulation products were therefore expected at frequencies of 4.7 MHz and 5.3 MHz on the wideband output. Figures C.7 and C.8 show the average and peak power outputs of the receiver respectively. The averaged two-tone dynamic range, measured on

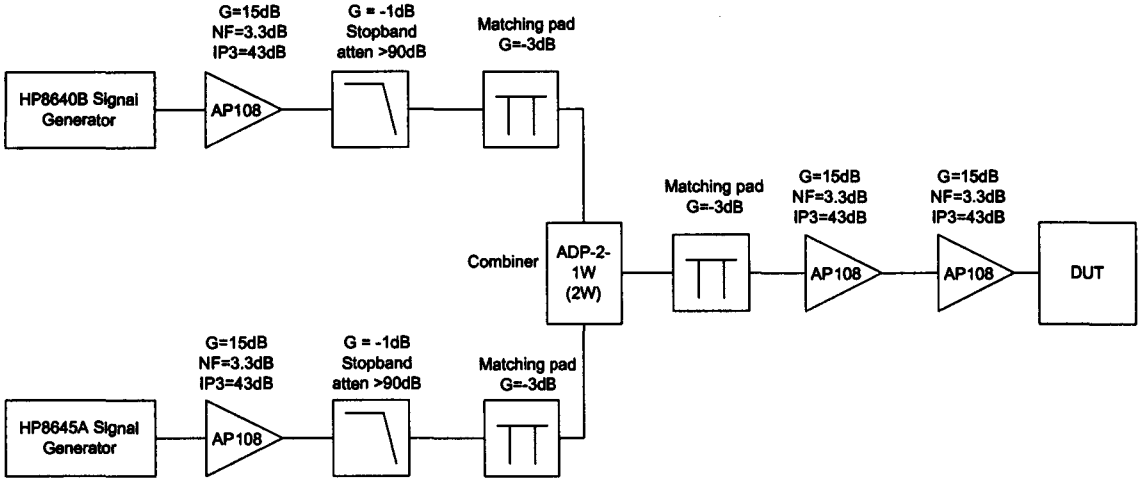

Figure 6.2: Intermodulation distortion test setup.

figure C.7, was -85 dBc, while the worst-case two-tone dynamic range was found to be -81 dBc. The large discrepancy between the averaged and worst-case performance may be attributed to the fact that the average linearity of the A-D converter exceeds its worst-case linearity. The measurement of average two-tone dynamic range is limited by the test equipment, which was measured at -85 dBc.

6.3 Empirical Testing of the Digital Receiver at 12.8 MHz IF

This section presents the results of tests performed on the digital receiver while operating in the 12.8 MHz IF, 10 MHz wideband receiver mode, with a resolution bandwidth (FFT frequency resolution) of 12.5 kHz. Band-limited dither noise at approximately -20 dBFS was present during all testing of this receiver mode, unless otherwise noted.

6.3.1 Non-Harmonic Spurious-free Dynamic Range

Testing was performed on the digital receiver in a 10 MHz bandwidth configuration with the analogue input terminated in 50 Ω. The resulting output spectrum is shown in figures C.9 and C.10, illustrating the averaged and worst-case (peak hold) spurious respectively. The worst-case non-harmonic spurious-free dynamic range was found to be noise-limited, at a level of -93 dBFS.

6.3.2 Harmonic Spurious-free Dynamic Range

The test setup shown in figure 6.1 was used to evaluate the single-tone SFDR of the digital receiver. A lowpass filter with a 12.8 MHz cut-off was used between the signal generator and the receiver input. A signal corresponding to a level of -1 dBFS at the A-D converter input at a frequency of 12.64 MHz was placed on the digital receiver input. The frequency was deliberately chosen to be close to 12.8 MHz (one quarter of the sampling rate), such that the odd-ordered harmonics generated in the A-D converter would fold back close to the input frequency, falling within the 10 MHz band. Figures C.11 and C.12 plot the averaged and worst case (peak hold) output respectively. The worst-case spurious was found to be caused by the third harmonic at a level of -88 dBFS.

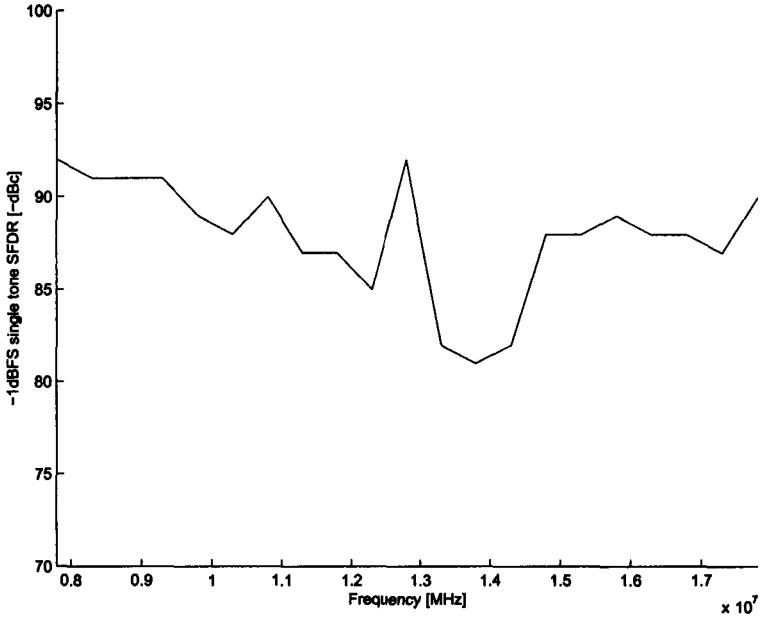

Figure 6.3: Single-tone harmonic spurious-free dynamic range versus frequency.

Figure 6.3 shows the results of sweeping a -1 dBFS signal across the 10 MHz bandwidth, and recording the spurious-free dynamic range at 0.5 MHz increments. The results at 12.8 MHz are misleading, since at this frequency all of the even-ordered harmonics fall out-of-band, and the odd-ordered harmonics alias back onto 12.8 MHz. The region around 12.8 MHz shows a poor SFDR, which results from the third harmonic folding back in-band. The amplitude of the third harmonic was found to increase as the input frequency was increased.

Figure 6.4 plots the single-tone spurious-free dynamic range versus input amplitude,

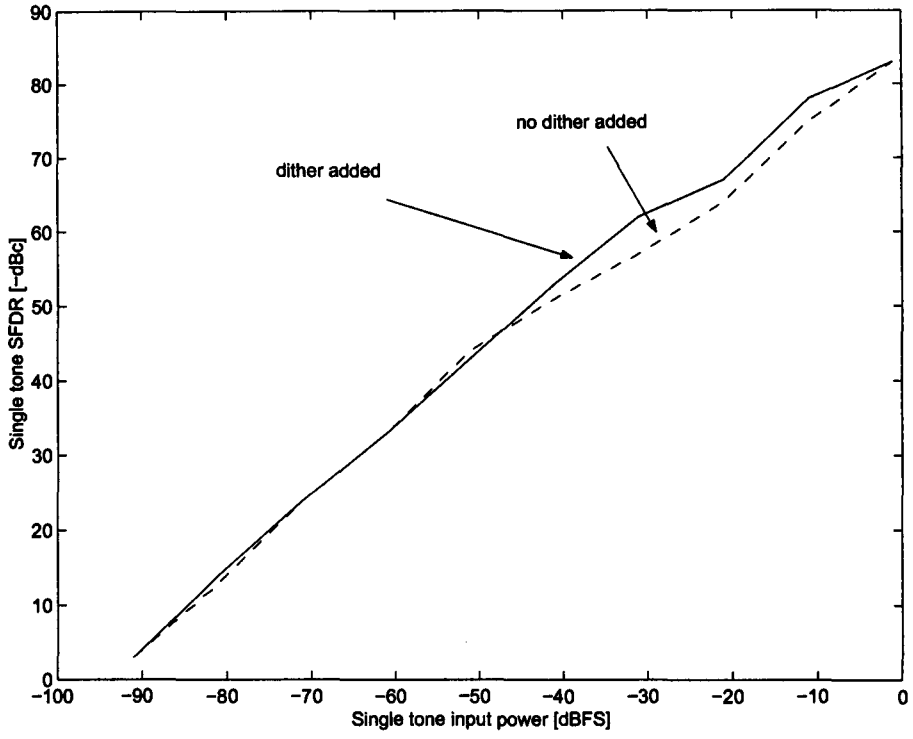

Figure 6.4: Single-tone harmonic spurious-free dynamic range versus input amplitude.

for an input signal at a fixed frequency of 12.64 MHz. The plot compares the results with no dither noise added to those with a dither noise level of approximately -20 dBFS. The region of poor linearity around -20 to -30 dBFS is clearly visible in the case where no dither was added. The additional dither noise can be seen to improve the single tone SFDR at these input power levels by 5 dB.

6.3.3 Two-tone Third-order Intermodulation Distortion Measurement

The two-tone third-order intermodulation tests were performed using the test setup discussed in section 6.2.3. The filters used in the test setup were designed with a cut-off frequency of 13 MHz and a stopband attenuation greater than 90 dB.

The intermodulation distortion for the 12.8 MHz IF mode was measured by placing two signals at frequencies of 12.7 MHz and 12.9 MHz respectively, each at a level of -7 dBFS. Initial tests showed that the noise generated in the IMD test setup resulted

in the receiver noise floor being higher than the level of third-order intermodulation distortion products. It was therefore necessary to reduce the noise level, such that the intermodulation distortion products could be measured. The noise level reduction was achieved by decimating the signal by a further factor of eight in each channel (equivalent to the eight times zoom mode discussed in chapter 4). The noise floor was reduced by 9 dB through the resulting processing gain, which was sufficient to allow the intermodulation products to be measured.

Figures C.13 and C.14 show the averaged and worst-case receiver outputs for the 12.8 MHz IMD tests respectively. The intermodulation products are visible above the noise floor at frequencies of 12.5 MHz and 13.1 MHz. The averaged two-tone dynamic range, measured on figure C.13, was -85 dBc, while the worst-case two-tone dynamic range, measured on figure C.14, was found to be -79 dBc. The large discrepancy between the averaged and worst-case performance may be attributed to the fact that the average linearity of the A-D converter exceeds its worst-case linearity. The worst-case linearity measurement may be attributed to the A-D converter, when a large percentage of the samples fall into non-linear regions of its transfer function. The measurement of average two-tone dynamic range is limited by the test equipment. The average was measured at -85 dBc.

Chapter 7

Conclusion

The aim of this dissertation was to investigate and evaluate state-of-the-art wideband digital radio receiver hardware through the design and implementation of a high-performance digital receiver capable of functioning in both wideband and narrowband modes, that would satisfy the requirements described in section 1.3. The system that was implemented is successful in achieving these aims:

- The designed system was shown to be highly flexible, supporting output bandwidths from 2.5 kHz to 1.25 MHz in each down-converter channel by altering the decimation factor.

  In a narrowband output mode, the receiver is capable of simultaneously providing 12 basebanded output channels. This mode has been successfully used in the implementation of a 12-channel narrowband demodulator, using a single ISA adapter board and mezzanine modules. Each down-converter channel may be independently programmed to down-convert any signal within the wideband input range of the digital receiver.

  Operating in a wideband mode, the receiver is capable of supporting bandwidths of up to 10 MHz at a 12.5 kHz frequency resolution, with zoom modes being supported through decimation factor adjustment.

- The design approach taken to form wide output bandwidths (up to 10 MHz) through the concatenation of narrower bandwidths was shown to be a highly scalable solution, capable of achieving output bandwidths that may be scaled up to near to the Nyquist bandwidth of the A-D converter, through the use of a sufficient number of down-converter channels. The solution was shown to reduce processing time and window coefficient storage requirements. A limitation of the approach is that the channelised wideband output may not be suitable for

subsequent narrowband time-domain processing such as demodulation, since the narrowband signals may fall over two wideband output channels.

- The spurious-free dynamic range realised by the receiver was found to be limited by harmonic spurious, rather than noise. Although the SNR quoted by the AD6644 datasheet[3] is worse than its harmonic distortion, the processing gains achieved through decimation filtering and the use of the FFT result in the noise bandwidth being sufficiently reduced, such that noise is not the limiting factor in the receiver's spurious-free dynamic range.

- The addition of appropriate levels of band-limited dither noise to the input of a multi-stage pipelined A-D converter was shown to increase the average linearity of the converter (SFDR increases of up to 5 dB) in the regions of poor linearity in its transfer function.

- The noise internal to the AD6644 was of sufficient level to exercise the LSBs and act as small-scale dither noise, enabling the receiver to observe signals that are well below the 84 dB of dynamic range which an undithered 14-bit A-D converter can provide, when averaging in the form of decimation or FFT processing is used.

- The receiver was shown to meet and exceed its performance specifications in all receiver modes, achieving a SFDR of better than -80 dB in all modes.

- The receiver was shown to be capable of phase-synchronous data acquisition across multiple boards. This mode has been successfully used in the implementation of a 6-channel wideband DF system (shown in figures D.1 and D.2).

- The receiver was shown to use predominantly COTS components and standard assembly methods.

The following improvements to the receiver design are suggested:

- The interfacing of the analogue receiver circuitry to the A-D converter should be optimised according to the discussion in section 2.6. The A-D converter performance should therefore be taken into account when designing the analogue receiver, rather than being treated as a separate entity.

- Consideration should be given to moving the IF to a higher frequency (70 MHz), in a sub-sampling architecture. This is seen as advantageous in that it removes the necessity for a second analogue mixer in the analogue receiver (which is currently responsible for limiting the analogue receiver dynamic range), and

facilitates the use of COTS SAW filters at the IF. System cost is therefore reduced, and performance is improved. Based on the findings of this dissertation, the noise resulting from the sampling clock jitter is likely to be a limiting factor in receiver SFDR at these analogue input frequencies, and a careful selection of sampling clock and related circuitry will be required.

- The dither circuitry should be moved closer to the receiver frontend. The inclusion of dither circuitry incurs losses at the end of the analogue receiver chain (the combiner results in a minimum of 3 dB loss). The losses increase the intermodulation distortion for any particular output level. This can be improved by moving the lossy components closer to the analogue receiver frontend.

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Appendix A

Derivations

A.1 Signal-to-Noise Ratio resulting from Encode Jitter

In this section the author derives equation 2.15. This derivation is based on the discussion in [5], which is further ellucidated:

We begin by considering a sinusoid with zero phase offset. The sinusoid may be expressed as:

$$V(t) = Asin(2\pi f_a t) \tag{A.1}$$

where A refers to the amplitude of the sinusoid, and f_a its frequency in Hertz.

From figure 2.5, it is noted that an error in the sampling time results in an error voltage that is proportional to the instantaneous slew rate (slope) of the signal:

$$\Delta V = slew\ rate * \Delta t \tag{A.2}$$

The slew rate of the signal is defined as the signals first derivative. We proceed to find the derivative of equation A.1:

$$\frac{d}{dt}V(t) = A2\pi f_a cos(2\pi f_a t) \tag{A.3}$$

We may express the rms error voltage as (cf. equation A.2):

$$\begin{aligned} (\Delta V)_{rms} &= \left(\tfrac{d}{dt}V(t)\right)_{rms} \cdot (\Delta t)_{rms} \\ &= \tfrac{A2\pi f_a t_{jitter}}{\sqrt{2}} \end{aligned} \tag{A.4}$$

The rms signal value is:

$$\begin{aligned}(V(t))_{rms} &= (A \cdot sin(2\pi f_a t))_{rms} \\ &= \frac{A}{\sqrt{2}}\end{aligned} \tag{A.5}$$

The rms signal-to-noise ratio may now be expressed as the logarithmic ratio of powers:

$$\begin{aligned}\left(\frac{S}{N}\right)_{rms} &= 10 \cdot log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) \\ &= 10 \cdot log_{10}\left(\frac{\left(\frac{A}{\sqrt{2}}\right)^2}{\left(\frac{A2\pi f_a t_{jitter}}{\sqrt{2}}\right)^2}\right) \\ &= 10 \cdot log_{10}\left(\frac{1}{2\pi f_a t_{jitter}}\right)^2 \\ &= 20 \cdot log_{10}\left(\frac{1}{2\pi f_a t_{jitter}}\right)\end{aligned} \tag{A.6}$$

Appendix B

GC4016 Wideband Decimation Filtering Frequency Response

This appendix shows the magnitude and phase response of the decimation filtering employed in the GC4016, in order to achieve an overall bandwidth of 10 MHz (1.25 MHz per channel), with a sampling frequency of 25.6 MHz.

The GC4016 decimation filtering consists of a 5th order CIC filter with programmable decimation in the range 8 to 4096, followed by two stages of FIR filtering with programmable 14-bit coefficients. Each FIR filter performs a further decimation by a factor of two.

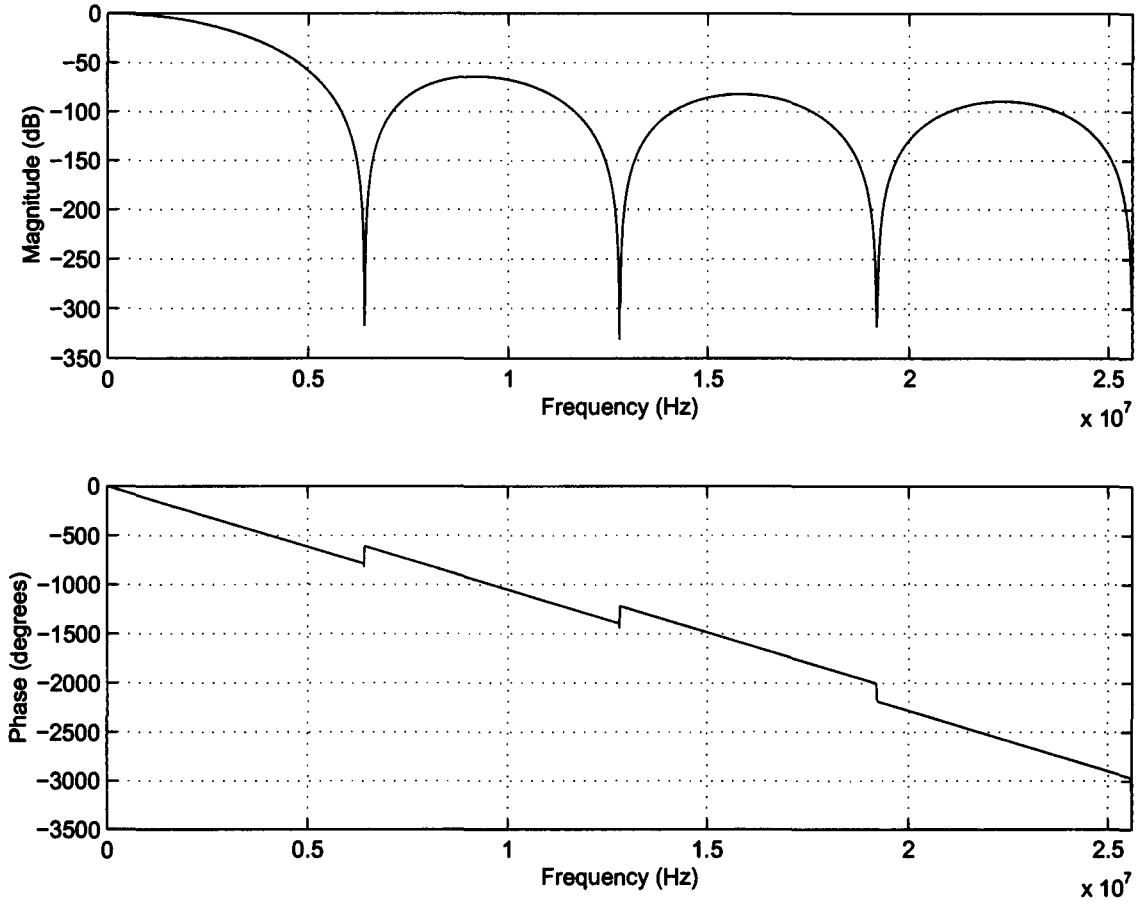

Figure B.1: Magnitude and phase response of 5th order CIC decimation filter (decimate by 8).

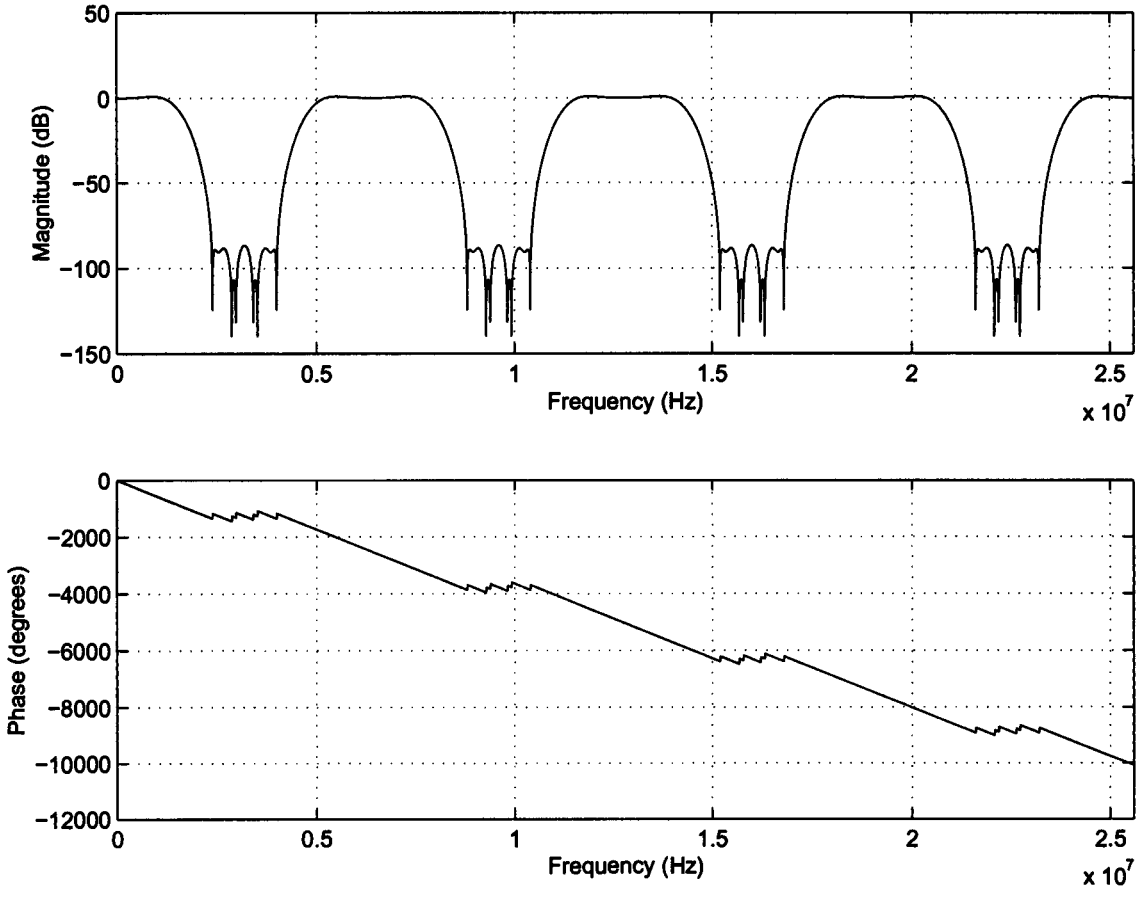

Figure B.2: Magnitude and phase response of 21-tap CFIR FIR filter.

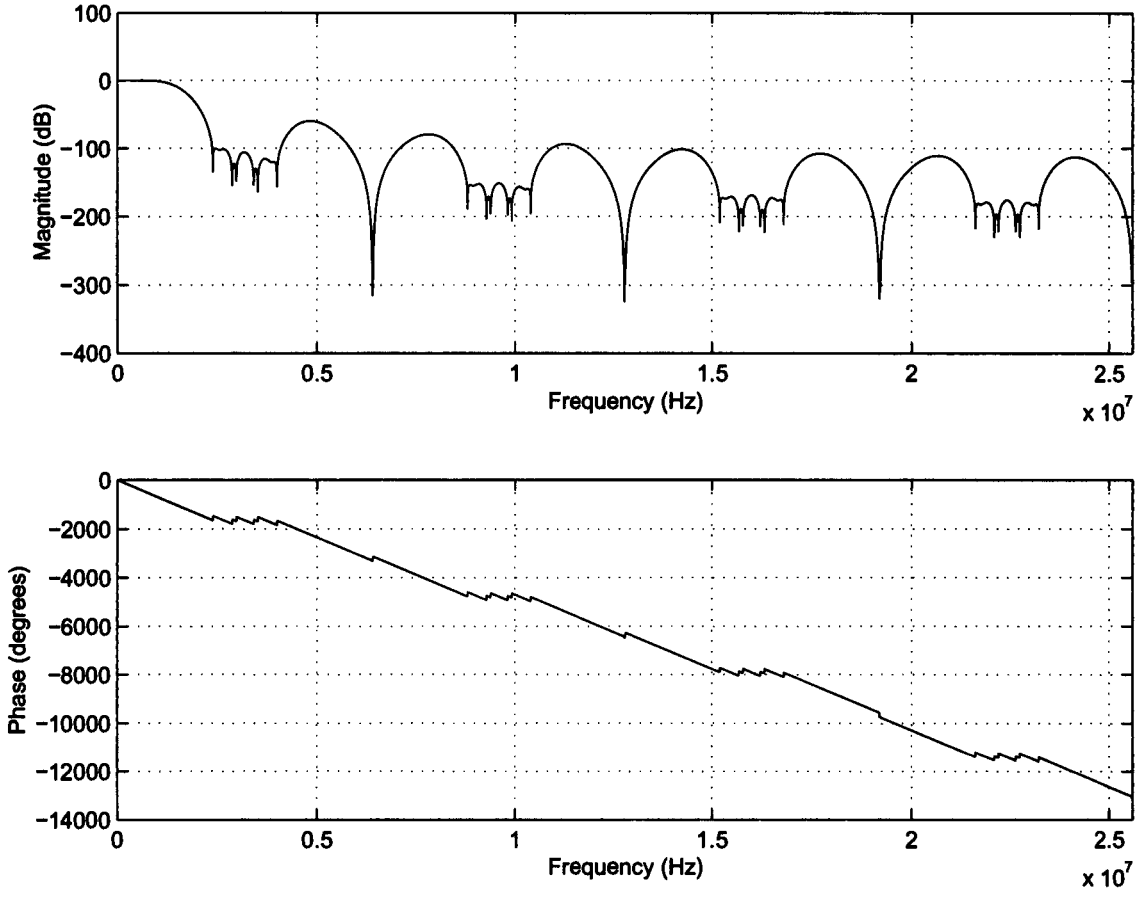

Figure B.3: Combined magnitude and phase response of CIC and CFIR.

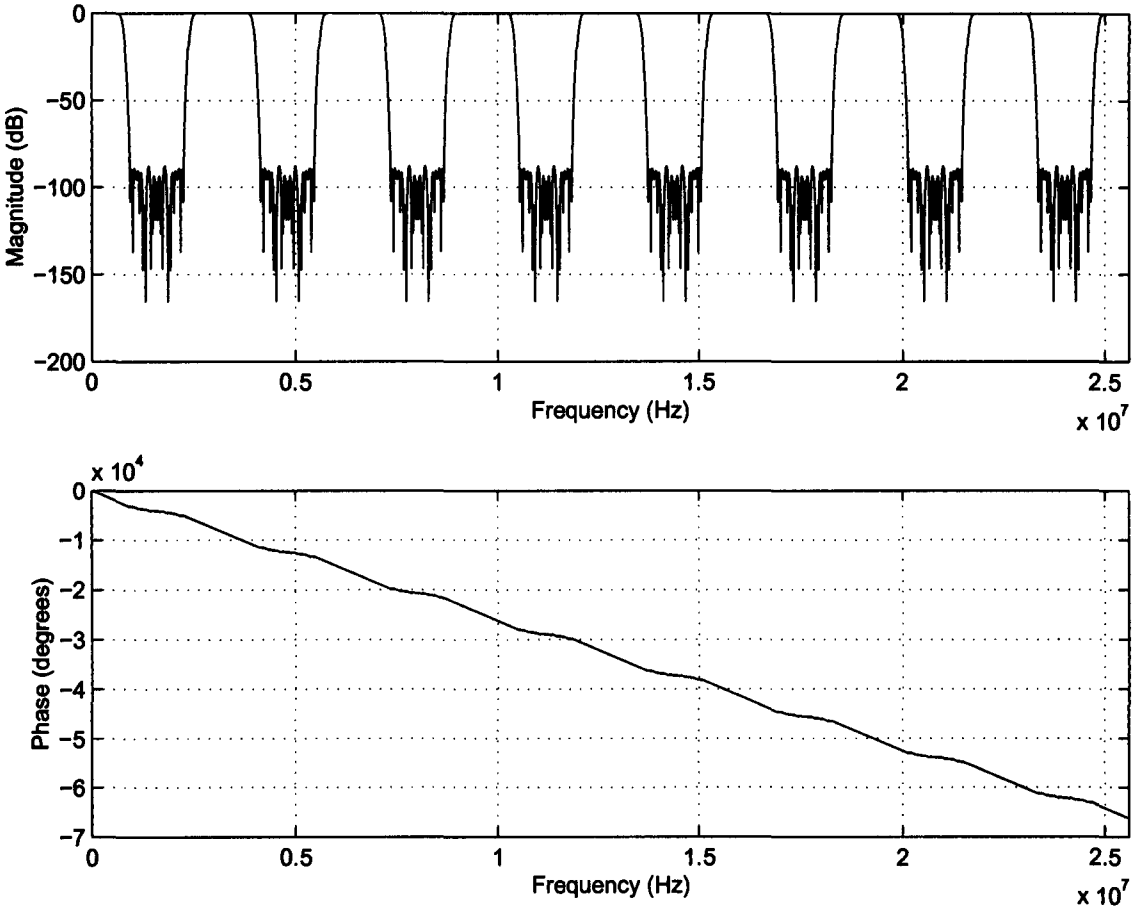

Figure B.4: Magnitude and phase response of 63-tap PFIR FIR filter.

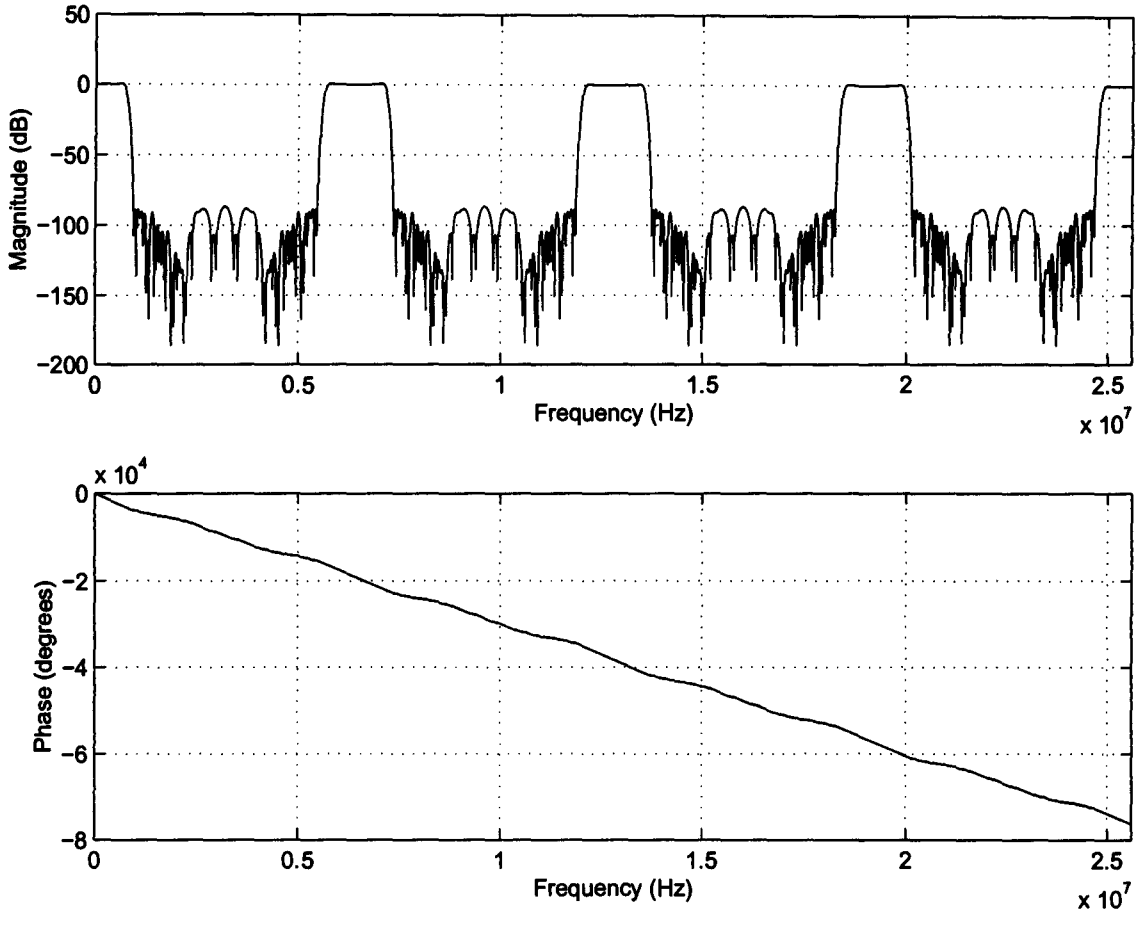

Figure B.5: Combined magnitude and phase response of CFIR and PFIR filters.

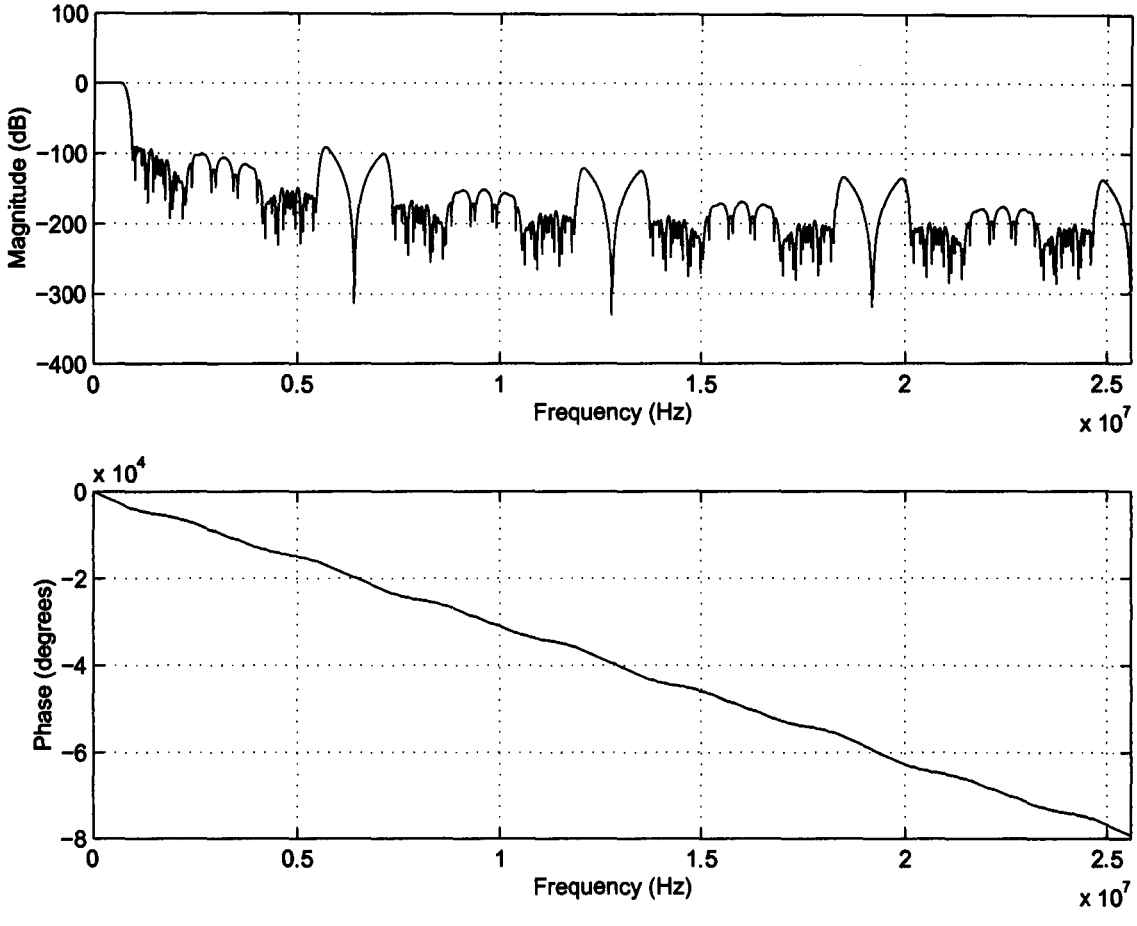

Figure B.6: Combined magnitude and phase response of CIC, CFIR and PFIR filters.

Appendix C

Digital Receiver Performance Plots

This appendix contains plots depicting the typical performance of the digital receiver.

C.1 AD6644 A-D Converter Output Plots

Plots C.1, C.2, C.3 and C.4 show the averaged output from DC to Nyquist (25.6 MHz) of a 16k FFT performed on the AD6644 output samples with various signals placed at the digital receiver's analogue input. A discussion of the plots is contained in section 6.1.

C.2 Wideband 5 MHz IF 800 kHz Bandwidth Receiver Output Plots

Plots C.5, C.6, C.7 and C.8 demonstrate the functionality of the digital receiver in the 5 MHz, 800 kHz mode of operation, with a resolution bandwidth (FFT frequency resolution) of 1 kHz. A discussion of the plots may be found in section 6.2.

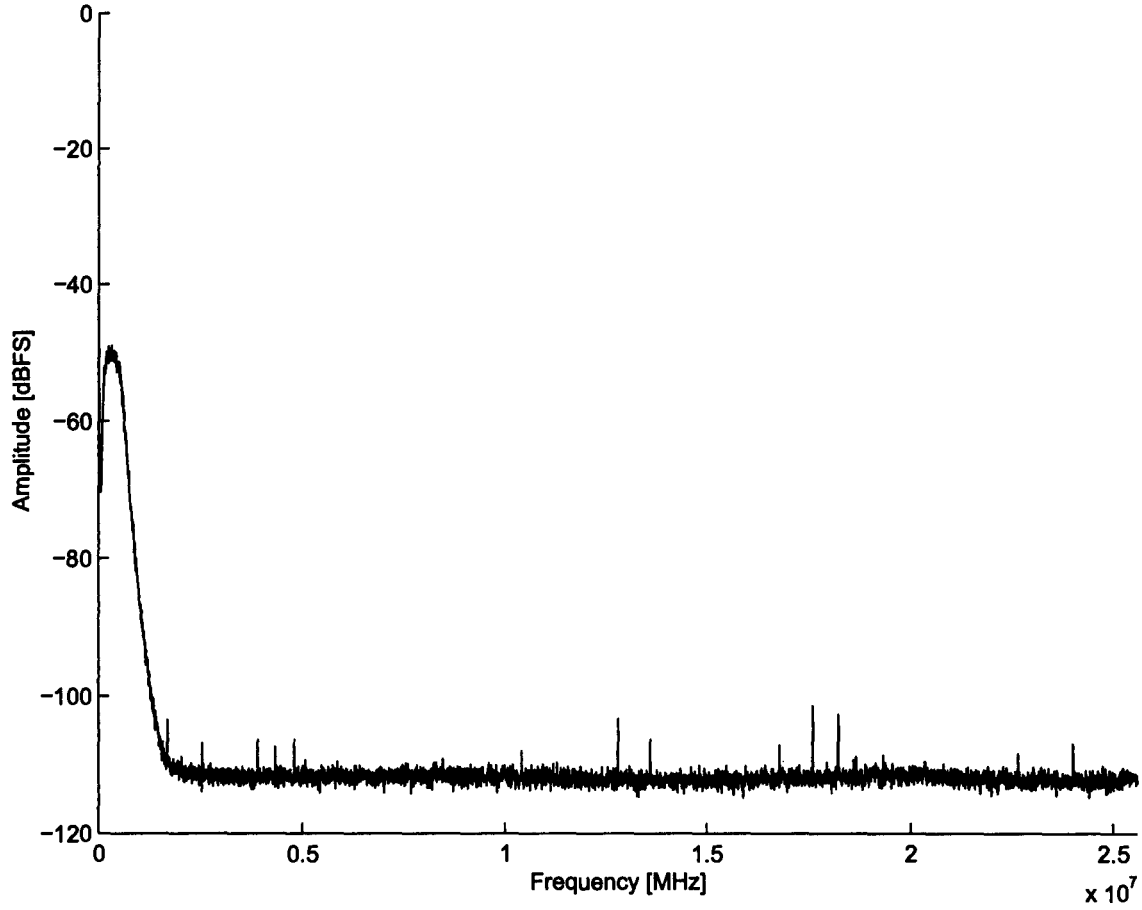

Figure C.1: Receiver analogue input terminated in 50 Ω.

C.3 Wideband 12.8 MHz IF 10 MHz Bandwidth Receiver Output Plots

Plots C.9, C.10, C.11, C.12, C.13 and C.14 show the output of the digital receiver configured in a 10 MHz bandwidth output. The 10 MHz bandwidth is formed by concatenating eight 1.25 MHz bands tuned to adjacent frequencies. The resolution bandwidth (FFT frequency resolution) of all plots corresponds to the 12.5 kHz used in the 10 MHz system configuration described in chapter 4, with the exception of the intermodulation tests. A further decimation by eight (corresponding to the eight times zoom mode with an eight times increase in frequency resolution) was necessary to reduce the high noise levels generated by the IMD test setup, such that the intermodulation products could be reliably measured.

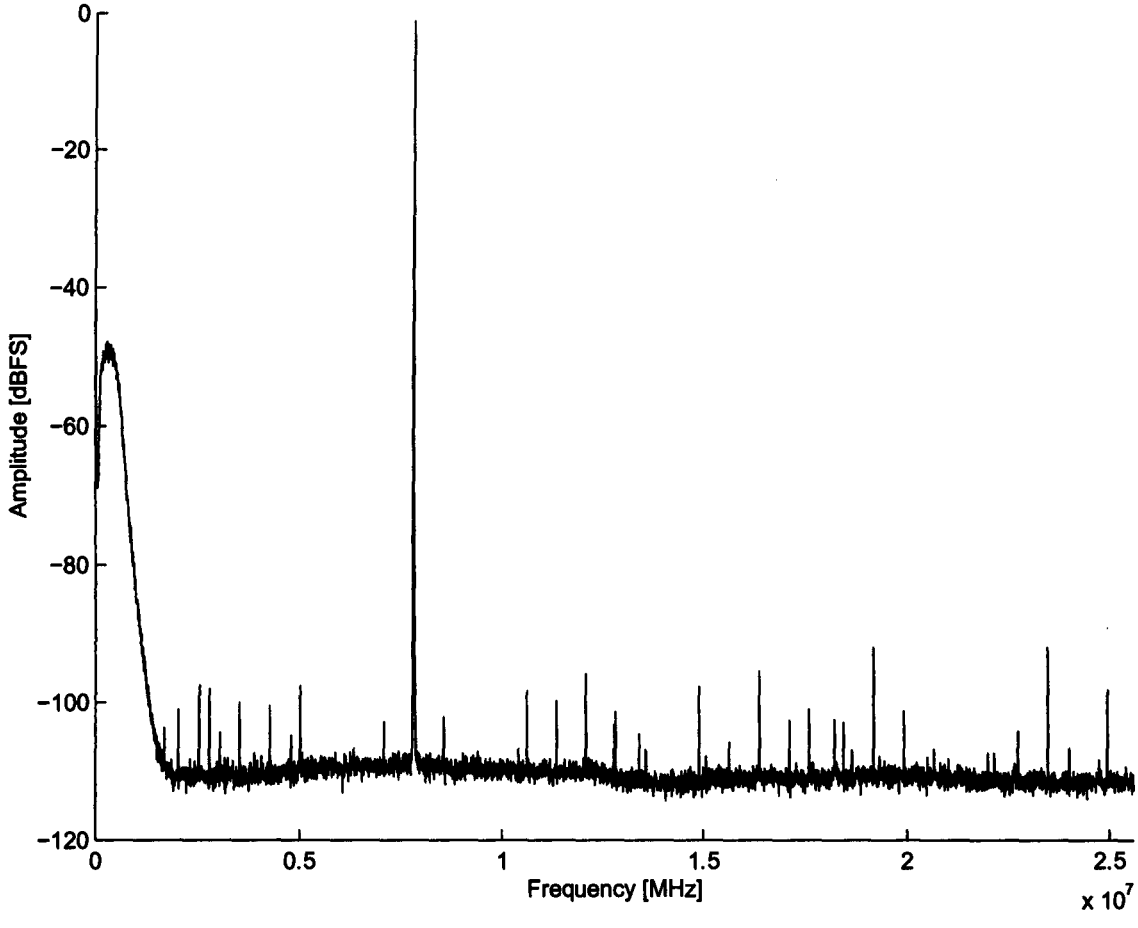

Figure C.2: 7.6 MHz, -1 dBFS tone at receiver analogue input.

A discussion of the plots may be found in section 6.3.

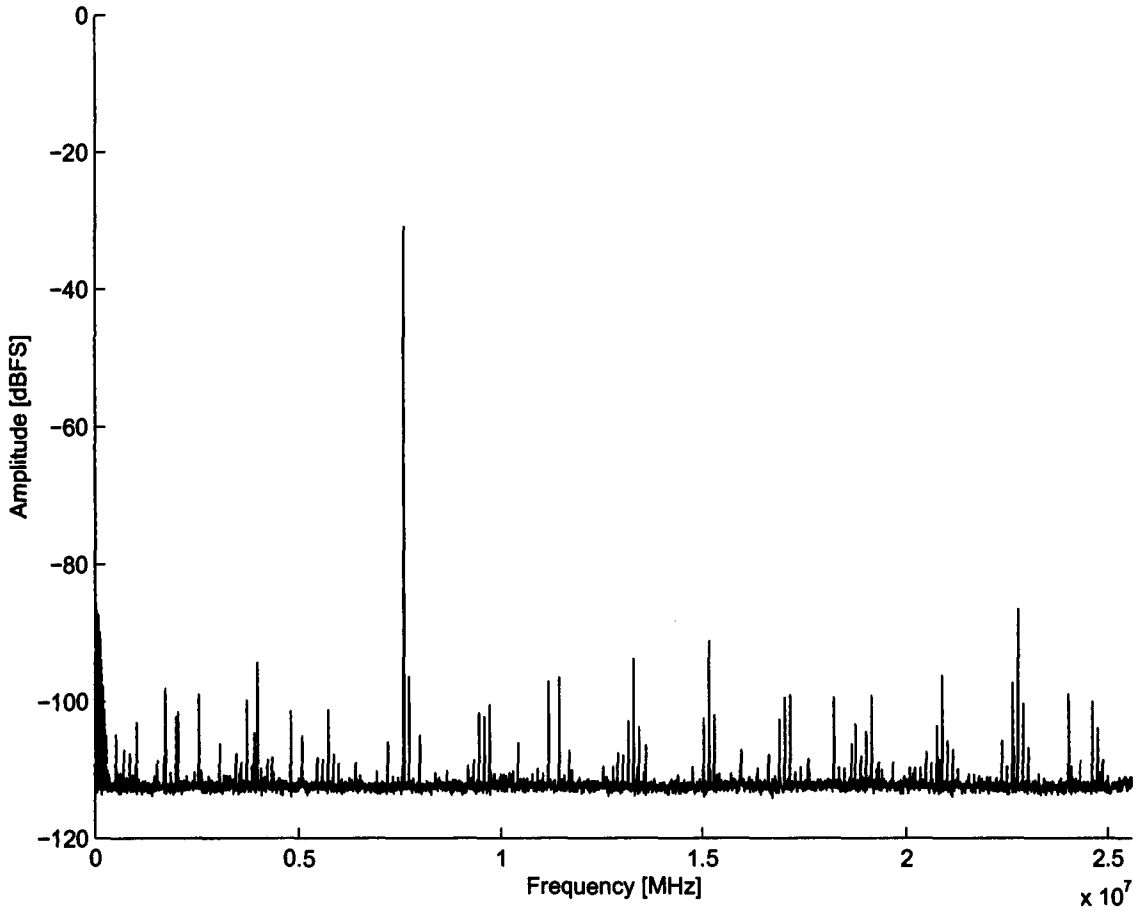

Figure C.3: 7.6 MHz, -30 dBFS tone at receiver analogue input with no dither.

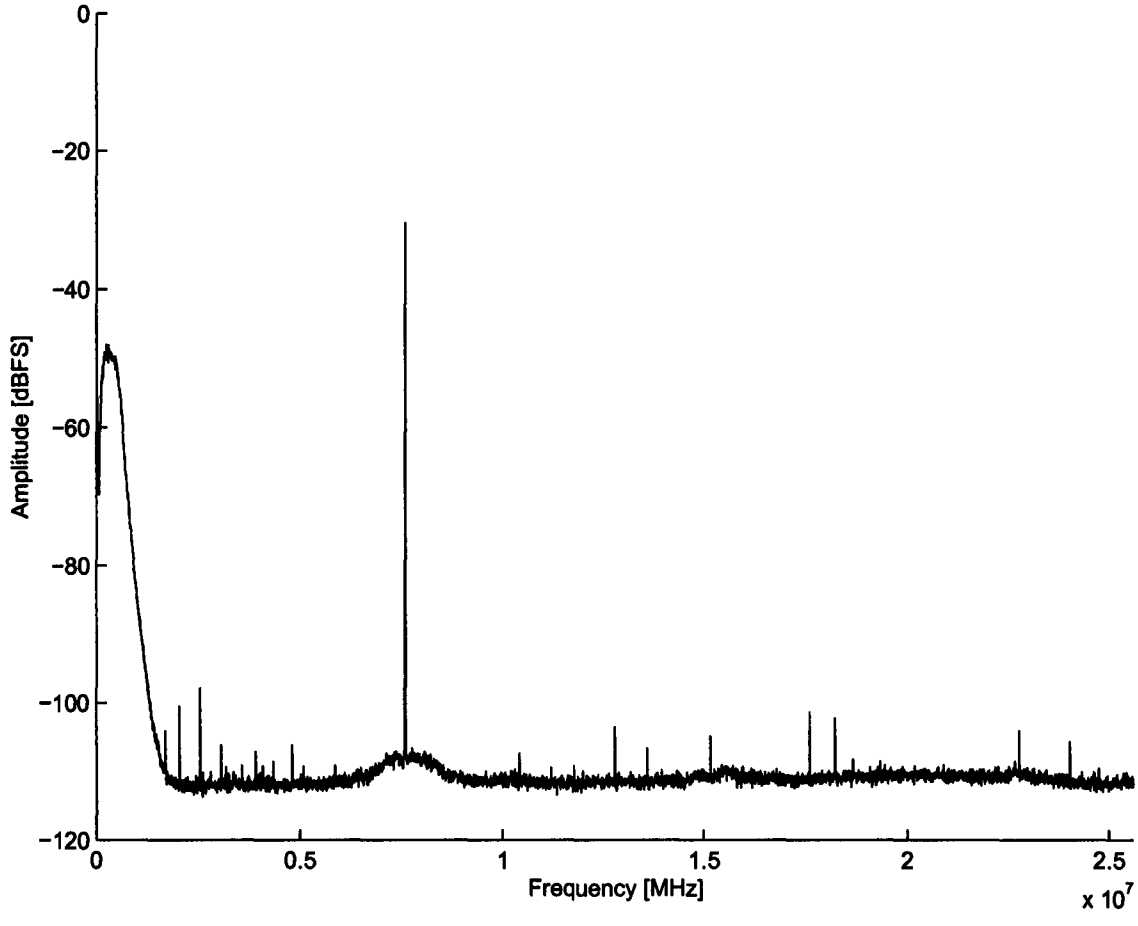

Figure C.4: 7.6 MHz, -30 dBFS tone at receiver analogue input with dither.

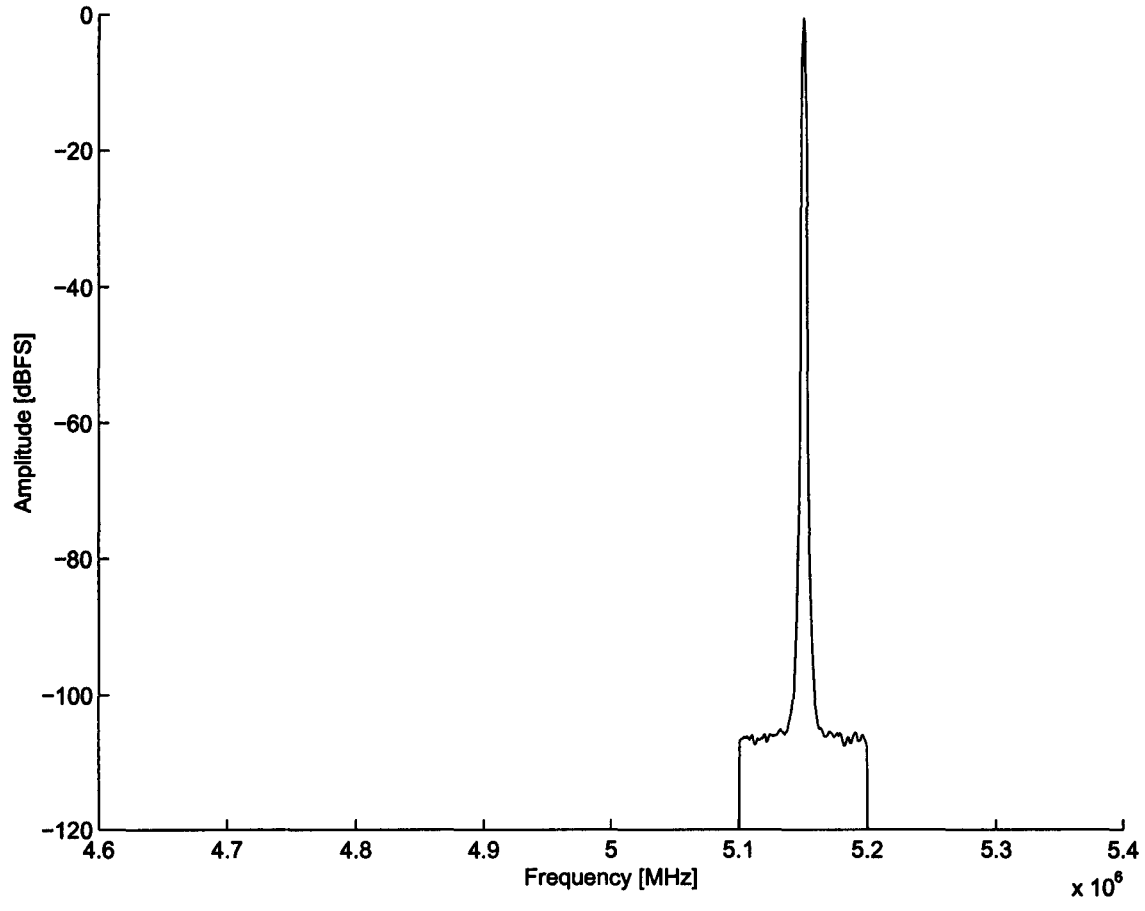

Figure C.5: Single tone at 5.15 MHz of amplitude -1 dBFS (averaged).

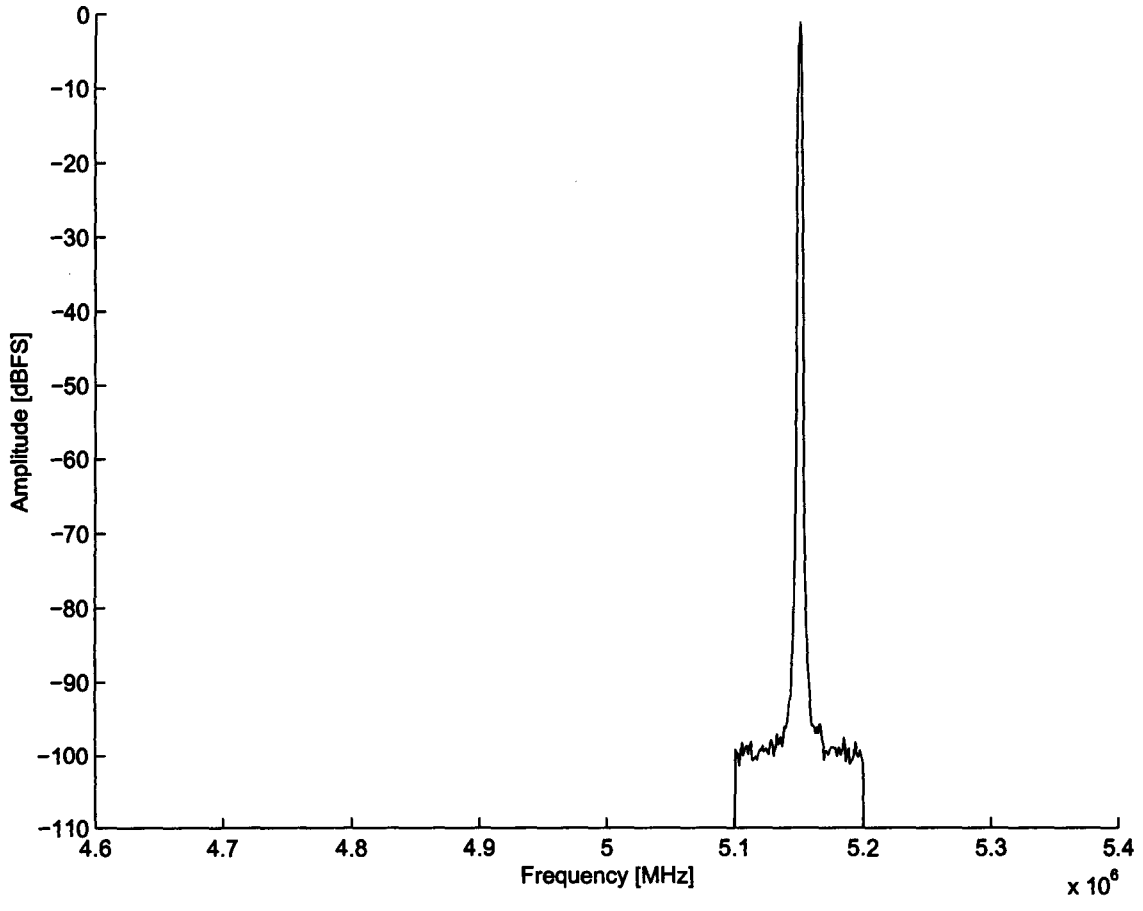

Figure C.6: Single tone at 5.15 MHz of amplitude -1 dBFS (peak hold).

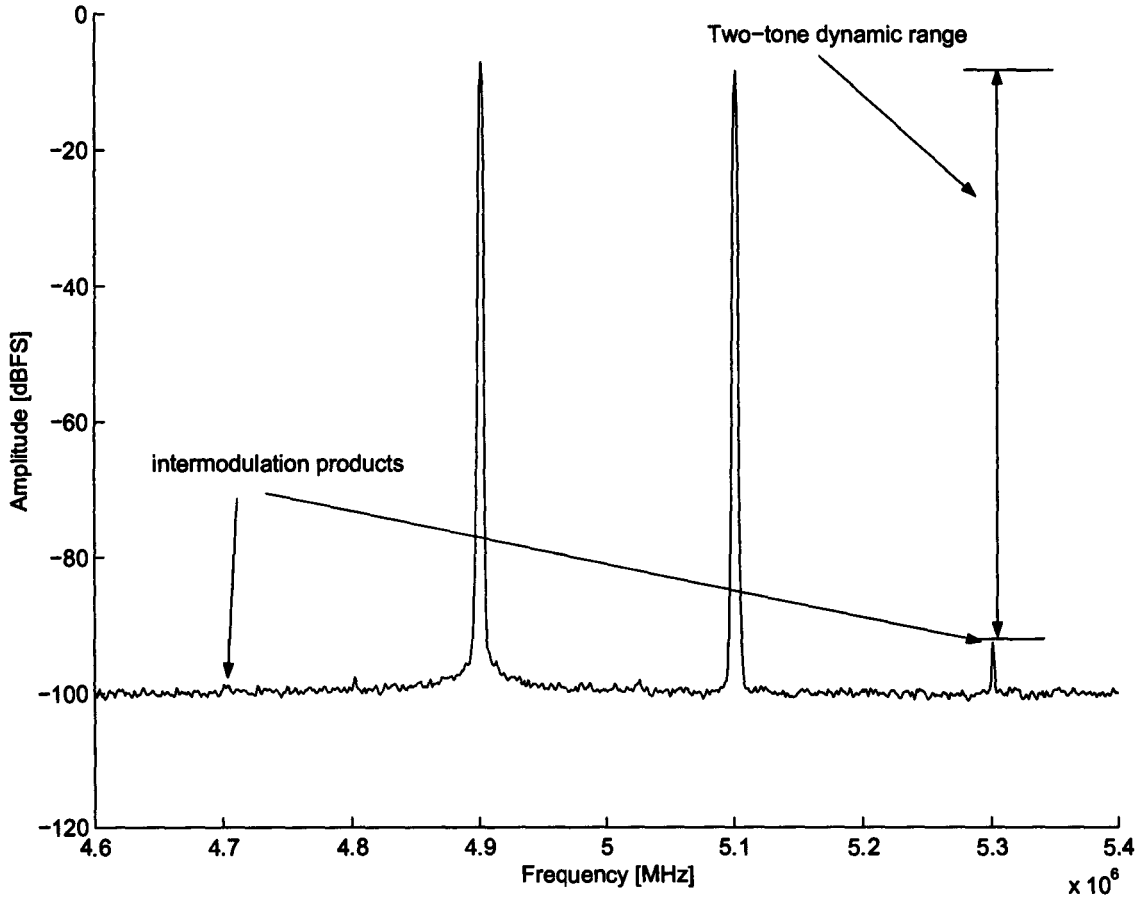

Figure C.7: Two-tone intermodulation test results at 5 MHz IF (averaged).

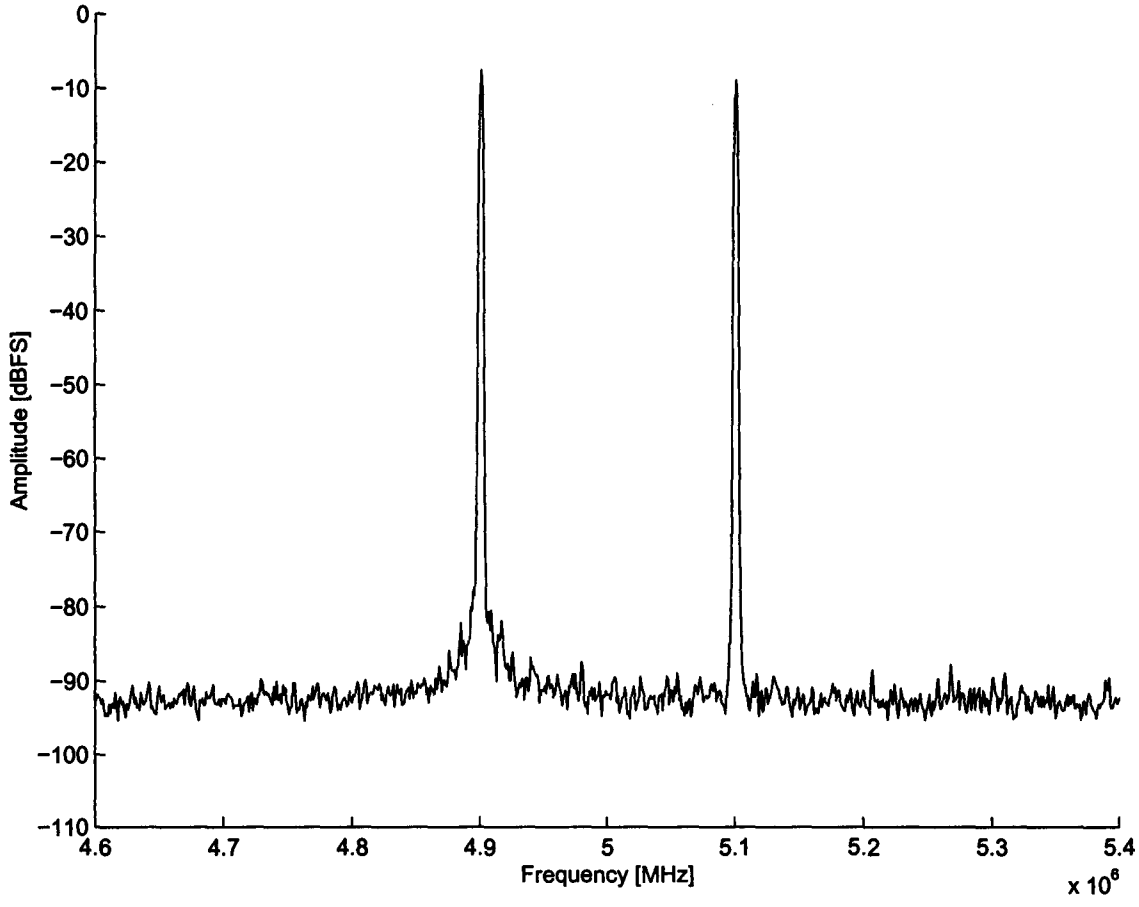

Figure C.8: Two-tone intermodulation test results at 5 MHz IF(peak hold)

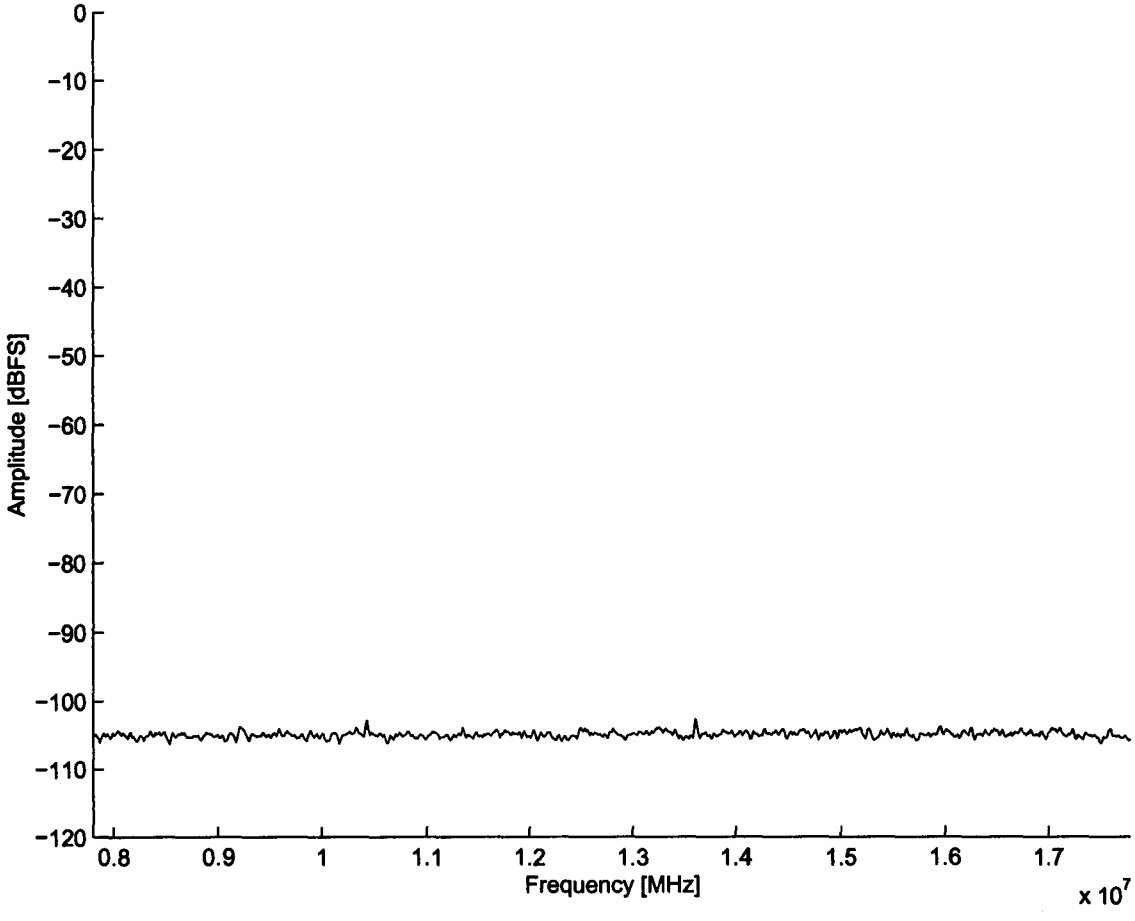

Figure C.9: Receiver input terminated in 50 Ω (averaged).

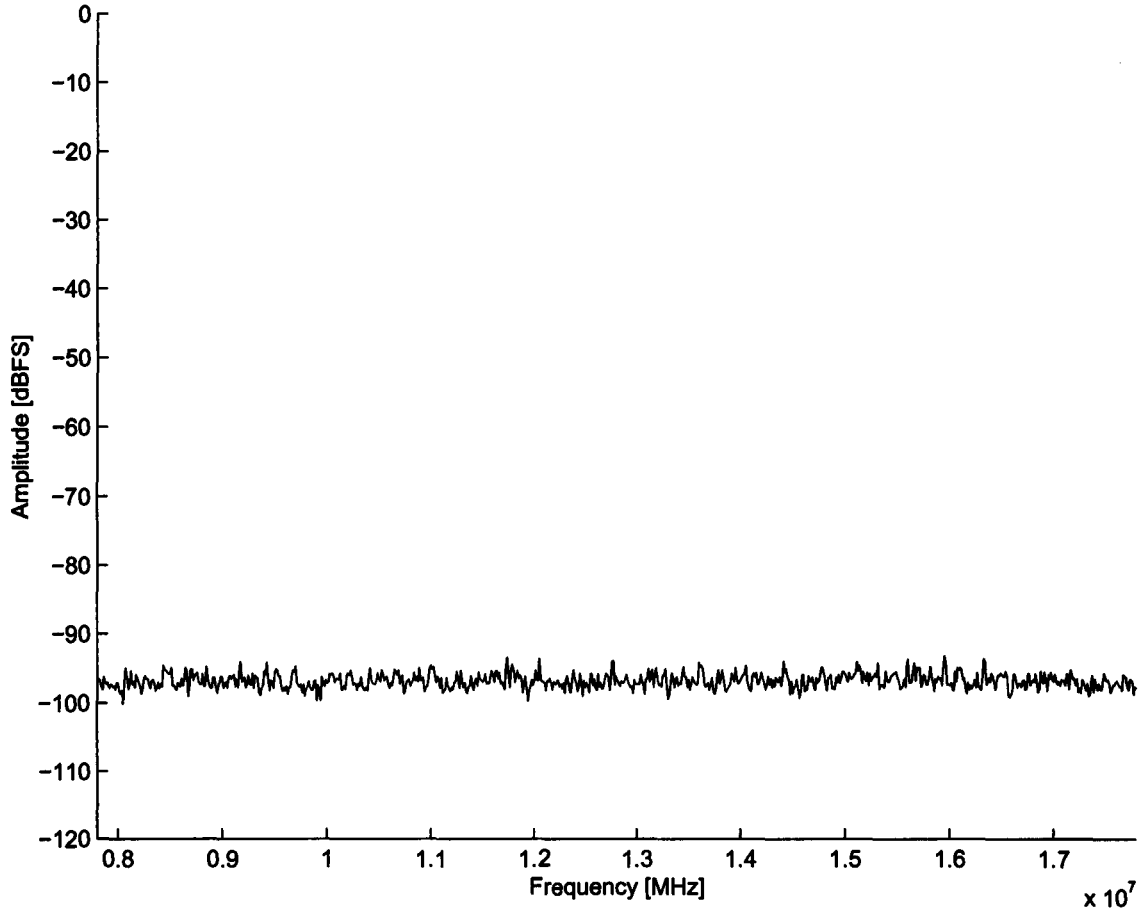

Figure C.10: Receiver input terminated in 50 Ω (peak hold).

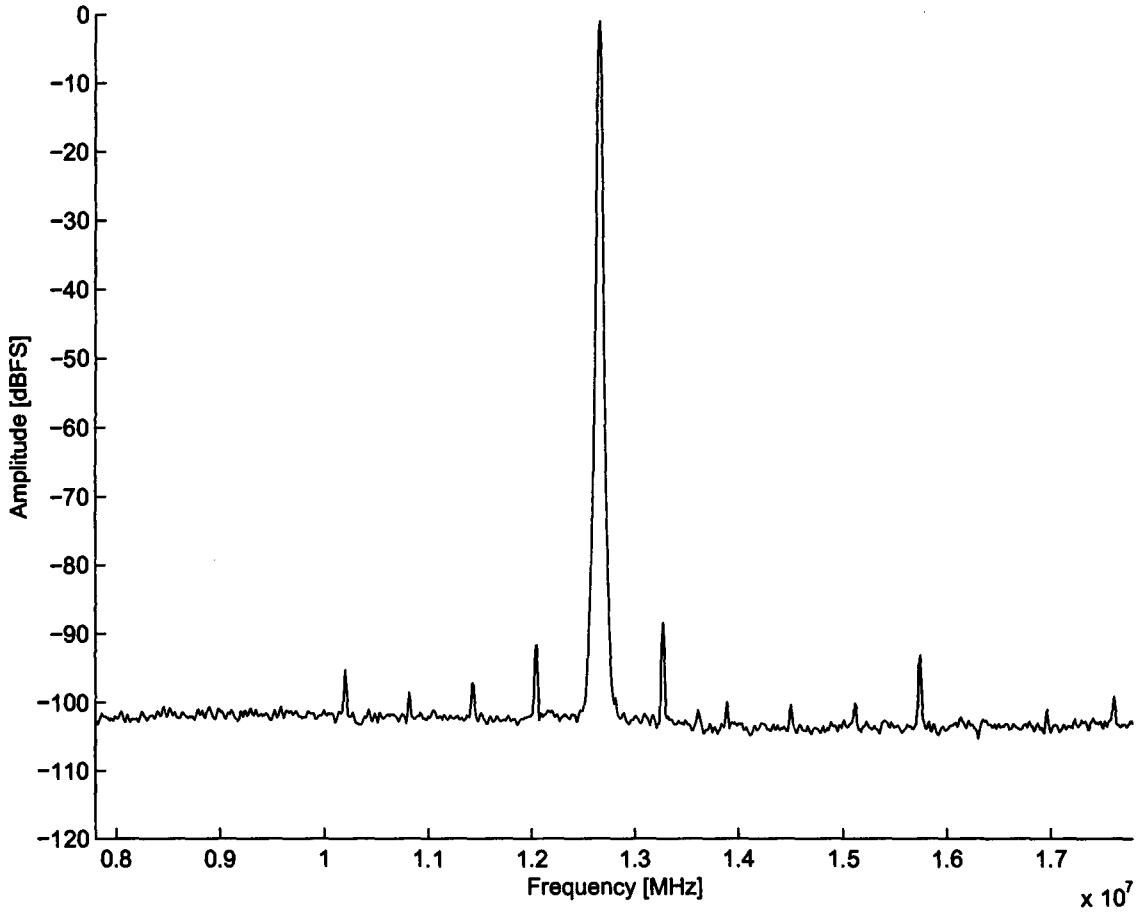

Figure C.11: Single tone at 12.64 MHz, -1 dBFS (averaged).

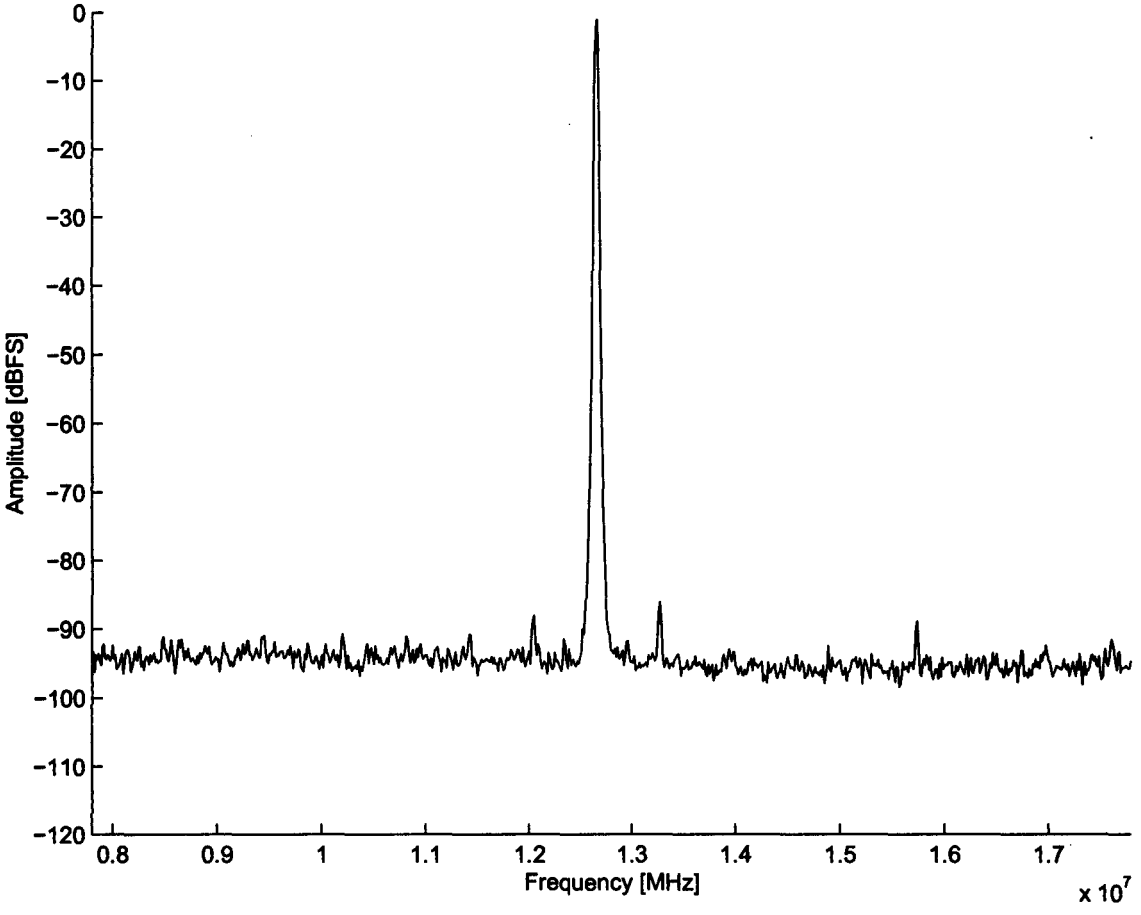

Figure C.12: Single tone at 12.64 MHz, -1 dBFS (peak hold).

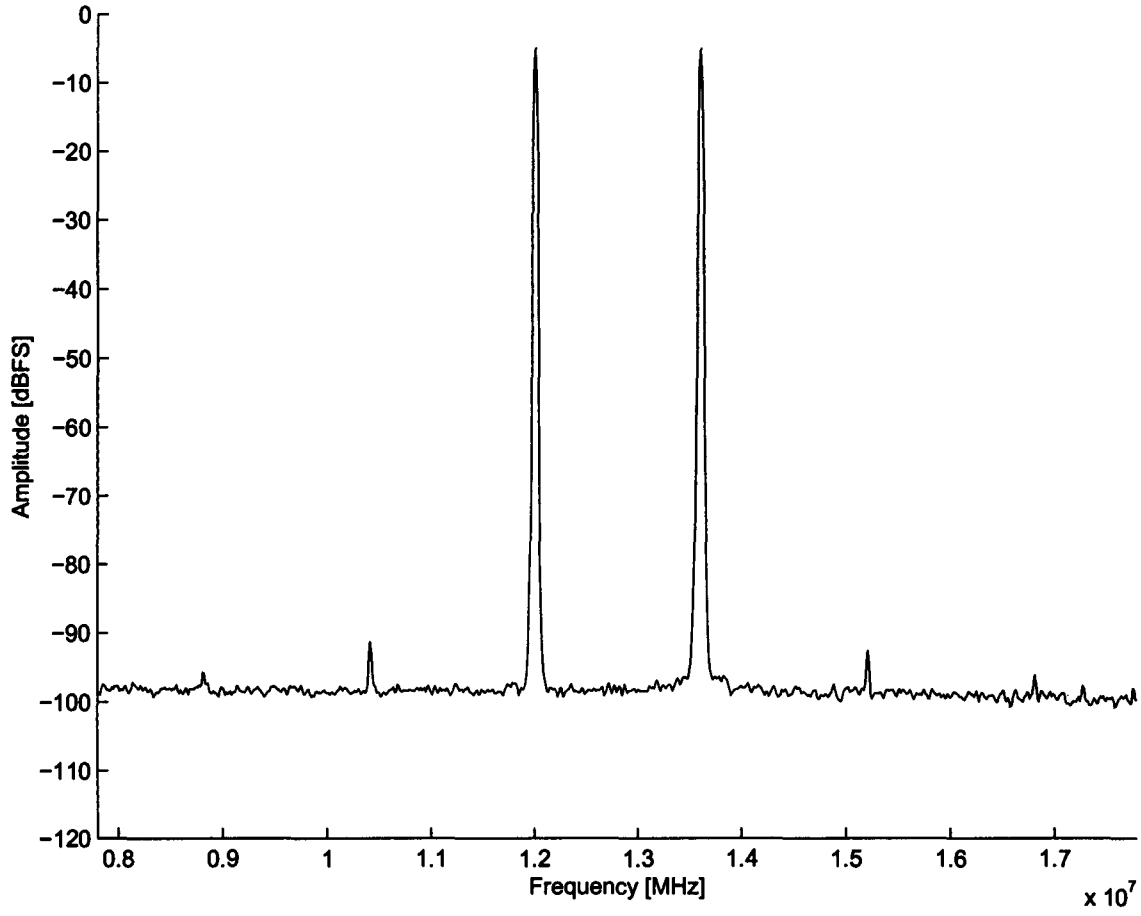

Figure C.13: Two-tone intermodulation test results at 12.8 MHz IF (averaged).

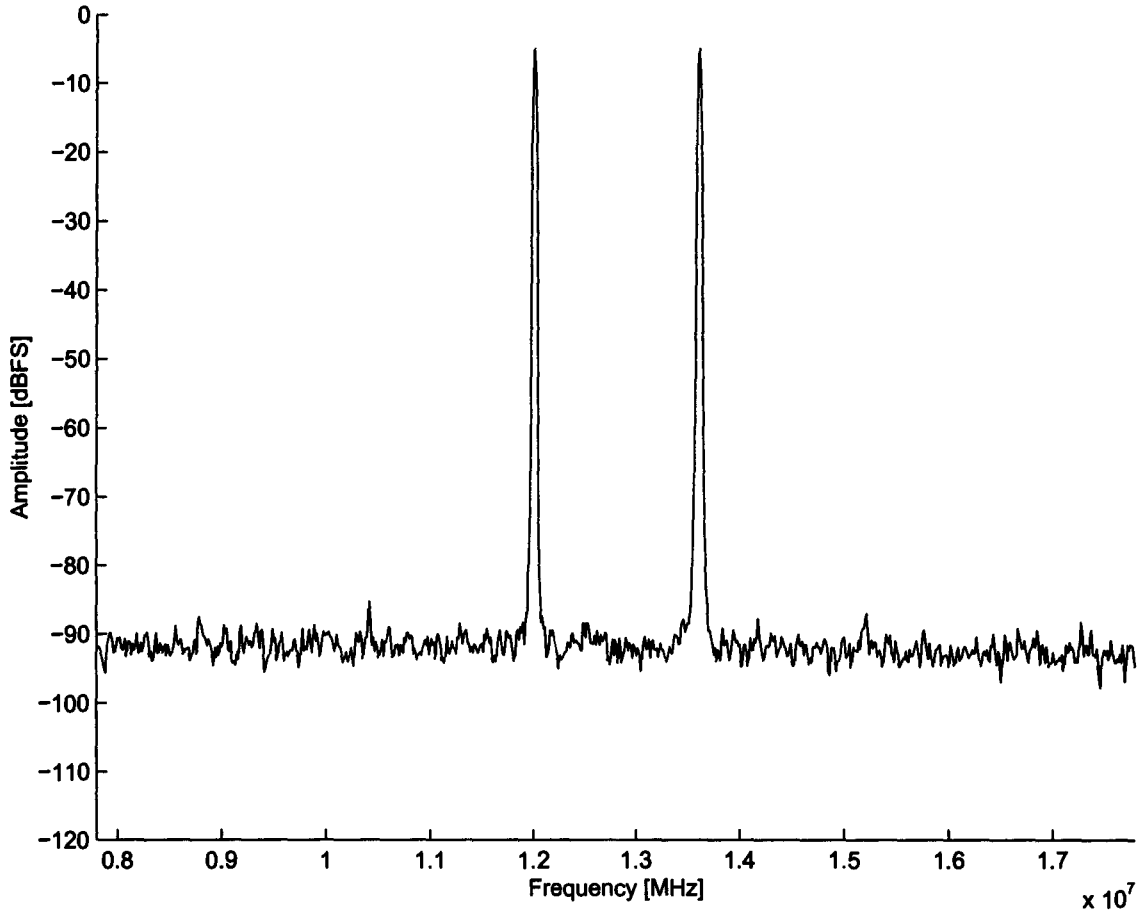

Figure C.14: Two-tone intermodulation test results at 12.8 MHz IF (peak hold).

Appendix D

System and Board Physical Construction and Layout

This appendix demonstrates the physical layout and construction of a typical system and digital receiver boards through a series of photographic images. Labels have been included where appropriate.

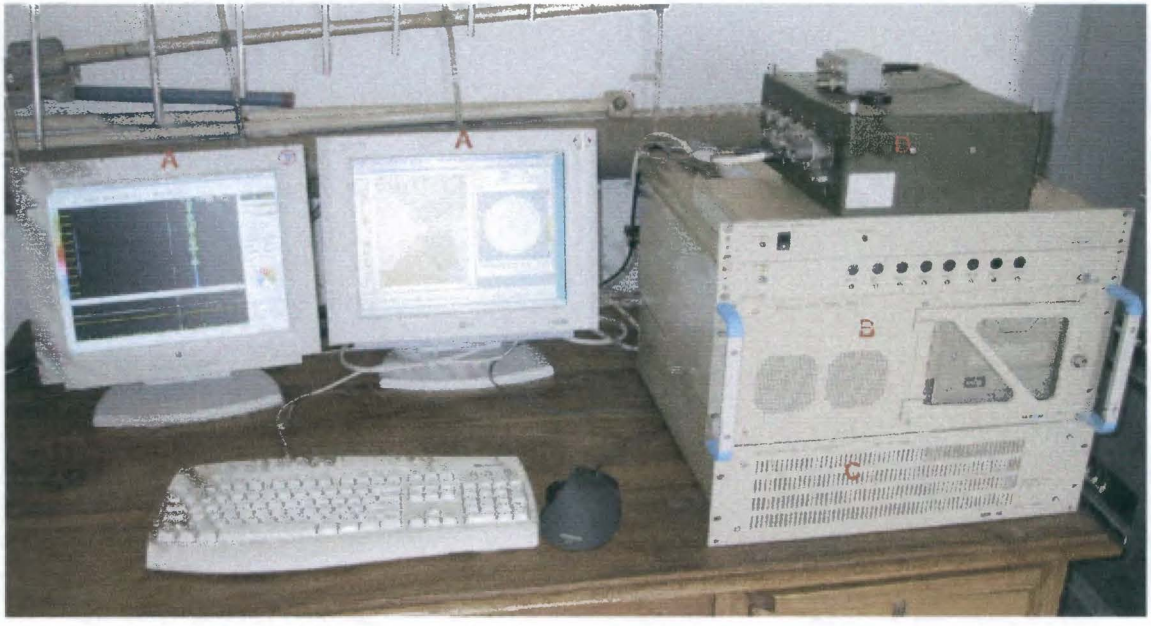

Figure D.1: 6-Antenna wideband receiver incorporating the digital receiver.

Key	Description
A	Video Display
B	Digital Receiver
C	Analogue Receiver
D	Antenna Selector

Table D.1: Key for figure D.1

Key	Description
A	Sampling clock and synchronisation board
B	Digital receiver adapter cards
C	Single board computer (SBC)
D	DSP processing boards
E	ATX Power supply
F	4U, 19 inch rack-mountable enclosure

Table D.2: Key for figure D.2

Key	Description
A	ADC and DDC mezzanine modules.
B	ADC and DDC shielding cover.
C	Mezzanine site on ISA base board.
D	ADSP-21160 digital signal processor.
E	External multichannel synchronisation input (PECL levels).
F	IF input connector (rigid co-axial cable runs along back of ISA board to top left of ADC module

Table D.3: Key for figure D.3

Figure D.2: 6-Channel wideband digital receiver.

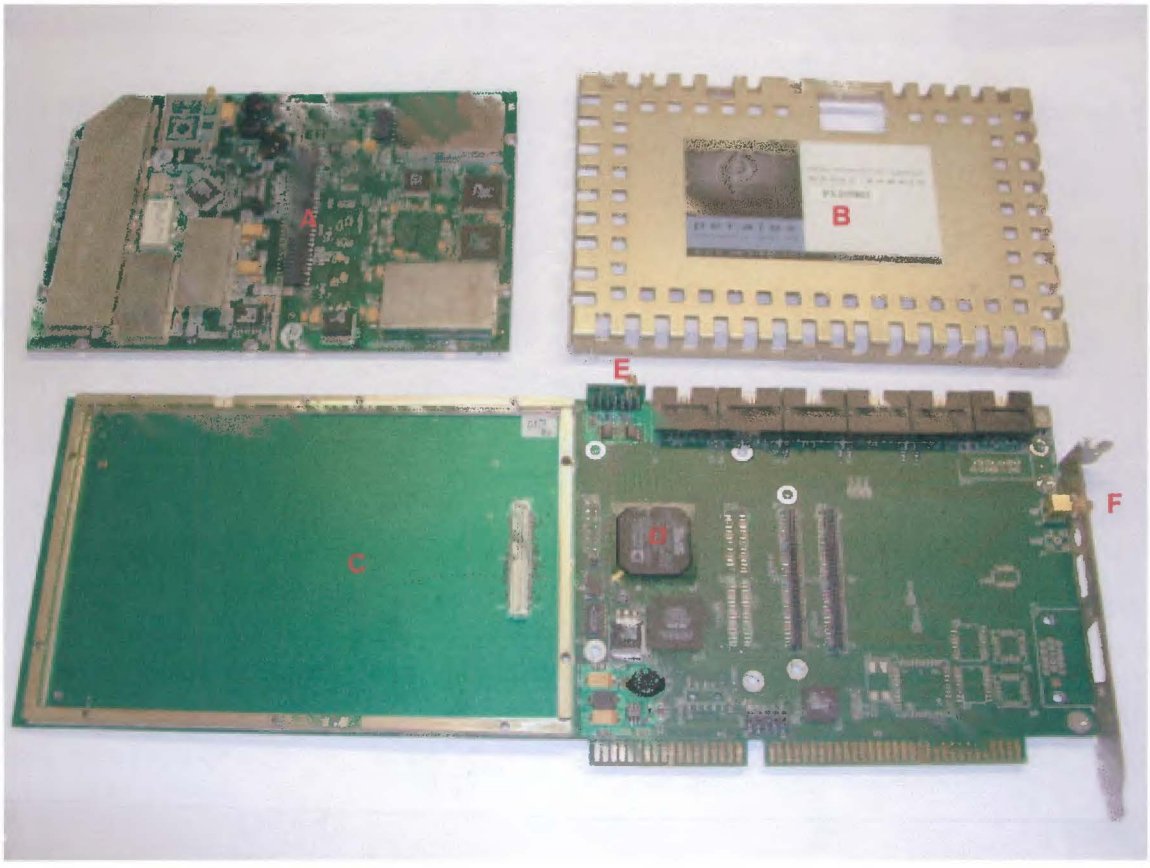

Figure D.3: Physical layout of the digital receiver adapter card and mezzanine module.

Key	Description
A	EMI shielding for sensitive circuitry.
B	Level matching and filter board (unpopulated).
C	Final anti-aliasing filter.
D	Dither circuitry.
E	AD6644 A-D converter.
F	External clock input.
G	GC4016 DDC's (BGA on bottom side of board).
H	Altera FPGA (BGA on bottom side of board).
I	+5.1V Analog DC-DC converter.
J	+3.3V Digital DC-DC converter.
K	FIFO memories.
L	Altera CPLD.

Table D.4: Key for figure D.4

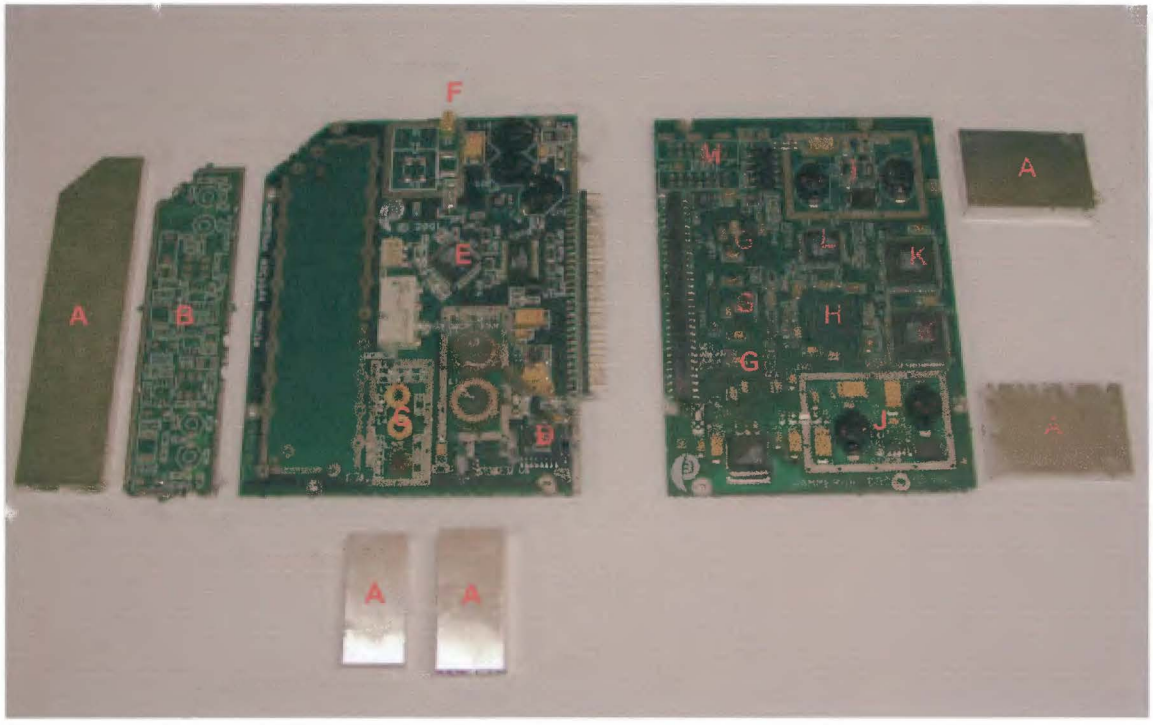

Figure D.4: Physical layout of the ADC and DDC boards.

Figure D.5: Assembled digital receiver card (no shielding cover).