Improvement in Control and Gain Aspects of Impedance Source Inverters and Converters

By: Zeeshan Aleem

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Supervisor: Dr. Simon Winberg

Co-Supervisor: Dr. Moin Hanif

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Declaration

This thesis was submitted to the Department of Electrical Engineering, University of Cape Town, in complete fulfilment of the requirements for the degree of Doctor of Philosophy. It has not been submitted before for any degree or examination at this or any other university. The author confirms that this thesis is based on his own work, save for which is duly referenced. Portions of this work have been published in peer reviewed journals and at refereed international conferences.

Signed by candidate

Zeeshan Aleem

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Abstract

Power electronics have revolutionized the concept of power control for power conversion and for control of electrical motor drives. Power electronics has been extensively used in industrial applications since it was first discovered in 1902. Power conversion is one of the most important and prominent applications of power electronics. Impedance source networks cover the entire spectrum of electric power conversions from DC-AC (e.g. inverters), to phase and frequency conversion (AC-AC) in a wide range of applications. A wide variety of topologies and control methods using different impedance-source networks have been presented in the literature to overcome the limitations and problems of traditional voltage source and current source as well as various classical buck–boost, unidirectional, and bidirectional converter topologies. Proper implementation of the impedance-source network with appropriate switching configurations and topologies reduces the number of power conversion stages in the system power chain, which may improve the reliability and performance of the power system.

The main focus of this thesis is to study and analyze different impedance source inverters and their control methods, and the development of improved impedance source power systems that will comprise advanced circuitry and provide higher voltage gains needing less complex systems that together provide more cost-efficient solutions. The systems under considerations would have high frequency electrical isolation and voltage clamping across the DC-link inverter bridge that would resulting in better protection, lower overall system losses, and increased efficiencies. Then parallel techniques will be discussed, analyzed and implemented for the class of impedance source inverters. This parallel operation of ZSIs leads to reduced components stress across the inverter bridges by sharing the currents, interleaving, ease of maintenance, modularity, higher reliability, and (N+1) redundancy.

The scope of impedance source networks is not limited to inverters (i.e., DC-AC power conversion), but covers a wide range of electric power conversion applications including (DC-DC and AC-AC converters). Thus, the last part of this research project will include the development of a new class of transformer based impedance source AC-AC

converters with novel control strategies to increase the input to output gains and to improve the conglomerate characteristics of the AC-AC converters.

Validation of the proposed structures will be done virtually using the Saber, PSIM simulations, and physically using experimental hardware prototypes. Several KW power systems will be fabricated and implemented using a DSP-kit based on the TMS320f28335 processor. Modified modulation schemes will be applied to control the switching of active devices. Furthermore, clamping techniques by minimizing the high frequency loop via clamping diode will be applied to the proposed inverters to limit the voltage overshoots caused by the leakage inductance energy.

The better performance of improved impedance source network (with added benefits of HF isolation and parallelization) to design more resilient and efficient converter topology for various applications such as adjustable speed drives, distributed generation systems, super-capacitor energy storage systems, uninterruptable power supply, dc circuit breakers, electric vehicles, avionics, and electronic loads will attract researchers and professional engineers to explore it in depth.

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Nomenclature

VSI	Voltage Source Inverter
CSI	Current Source Inverter
PVs	Photo-voltaic System
HEVs	Hybrid Electrical Vehicles
EMI	Electro-magnetic Interference
ZSI	Z-Source Inverter
qZSI	Quasi-Z-Source Inverter
M	Modulation Index
STDC	Shoot-through Duty Cycle
THD	Total Harmonic Distortion
B	Boost Factor
G	Voltage Gain
PWM	Pulse Width Modulation
SL-ZSI	Switched Inductor Z-source Inverter
SL-qZSI	Switched Inductor Quasi-Z-source Inverter
CA-EBZSI	Capacitor Assisted Extended Boost Z-Source Inverter
DA-EBZSI	Diode Assisted Extended Boost Z-Source Inverter
LCCT	Inductor Capacitor Capacitor Transformer
DSP	Digital Signal Processor
HFT	High Frequency Transformer
LC	Inductor Capacitor
KVL	Kirchhoff's Voltage Law
Volt-sec	Voltage Second
IGBT	Insulated Gate Bipolar Transistor
MC	Magnetically Coupled
ZSAC	Z-Source AC-AC Converter
DVR	Dynamic Voltage Restorer

List of Symbols

V_{in}	Input voltage
v_o	Output voltage
v_{pn}	DC-link voltage
$\widehat{v_{ph}}$	Output peak phase voltage
V_{sw}	Switch voltage stress
V_{RMS}	Root mean square voltage
v_a	Reference signal of phase A
v_b	Reference signal of phase B
v_c	Reference signal of phase C
V_p	Upper envelop signal
V_n	Lower envelop signal
V_c	Voltage across capacitor
n	Turns ratio of the transformer (coupled inductor)
Γ	Gamma
T_1	Transformer 1
T_2	Transformer 2
N	Number of inverters
kW	Kilo watt
v_L	Voltage across inductor
$v_{L_{sh}}$	Voltage across inductor in shoot-through state
$v_{L_{non}}$	Voltage across inductor in non-shoot-through state
D	Duty cycle
V_D	Voltage across diode
f_{sw}	Switching frequency
L_o	Output inductor
C_o	Output capacitor

L_p	Primary inductance
L_s	Secondary inductance
L_{lkp}	Primary side leakage inductance
L_{lks}	Secondary side leakage inductance
v_{ab}	Line-Line output voltage
i_o	Output current
P_{fe}	Core loss
P_{L_cu}	Inductor copper loss
P_{T_cu}	Transformer copper loss
K_{fe}	Proportionality constant
ΔB	Flux density
A_c	Cross sectional area
l_m	Mean core length
ρ	Resistivity
I	RMS winding current
K_u	Winding fill factor
W_A	Core window area
C_p	DC-blocking capacitor
C_s	Level shift capacitor
S	Switches
v_{rec}	Rectified voltage
v_{tri}	Triangular (carrier) wave
Σ	Sigma
i_{a1}	Inductor current of inverter 1
i_{a2}	Inductor current of inverter 2
V_{saw}	Saw-tooth wave
V_{ref}	Reference wave

1. Chapter 1
Introduction

1.1 Background

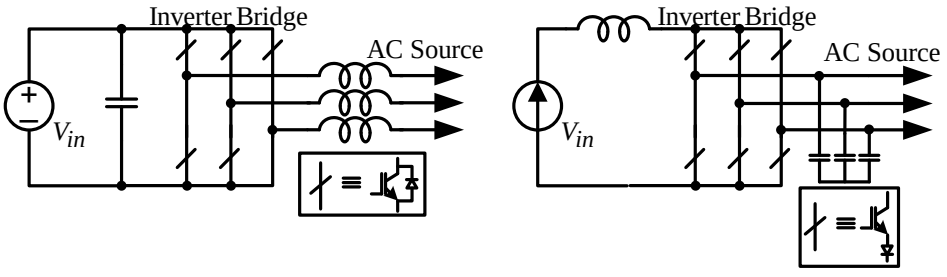
Traditionally there exist two types of power inverters for DC-AC conversion: voltage-source (VSI) and current-source (CSI) [1] as shown respectively in Fig. 1.1(a) and (b). Despite their huge demand in industrial applications, such as power distribution systems, photovoltaic (PV) systems and hybrid electric vehicles (HEVs), they suffer from some severe limitations [2-4] which makes them less preferable – some of the significant reasons for this, in terms of the using VSIs, are as follows:

- The obtainable output voltage is limited and cannot exceed the input DC voltage. Therefore, VSI is a step-down (buck) inverter and requires an additional boost DC-DC converter where over-drive (high o/p voltage) is required.
- Another major concern with the traditional VSIs is the requirement of dead time between the switching components of the same leg of an inverter-bridge. The switches cannot be turned on concurrently either by purpose or electromagnetic interference (EMI). Otherwise it will short-circuit the input capacitor and high current spikes will cause severe damage to the switches

Similarly, in terms of using CSIs:

- The obtainable output voltage is always higher than the supplied input DC voltage. Therefore, CSI is a step-up (boost) inverter and requires an additional buck dc-dc converter where reduced o/p voltage is required.
- CSIs requires an overlap between the switching components of the same leg of an inverter-bridge. The switches cannot be turned off concurrently either by purpose or electromagnetic interference (EMI). Otherwise it will open-circuit the input inductor

and high voltage spikes will cause severe damage to the switches. Therefore, an overlap time is always required for the safe commutation of inductor current.



(a) (b)

Fig. 1.1 (a) Voltage source inverter (b) Current source inverter.

In addition both VSIs and CSIs have the common drawbacks such as they are either a buck or a boost power converter and thus requires additional dc-dc converter for a wide range of output voltage. This results in two stage power conversion and brings about additional switching losses and costs of the overall power system. Moreover, both have low reliability and are vulnerable to EMI noises resulting in poor output waveform qualities.

In order to address these issues, an impedance source inverter (ZSI) was proposed in 2002 [4] as shown in Fig 1.2. It efficiently utilizes the shorting (shoot-through) of the phase legs to boost the output voltage; it therefore provides single stage power conversion and has a better output waveform quality due to the elimination of dead time.

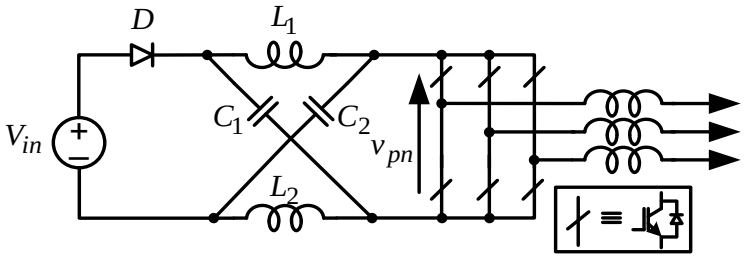
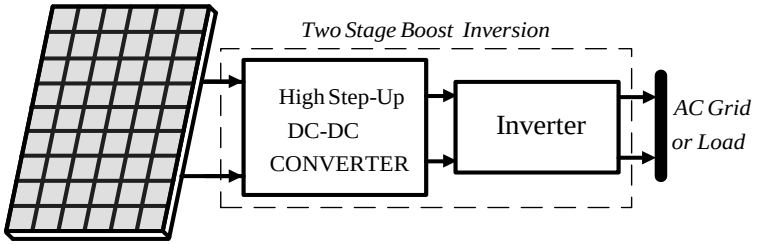


Fig. 1.2. Z-Source inverter

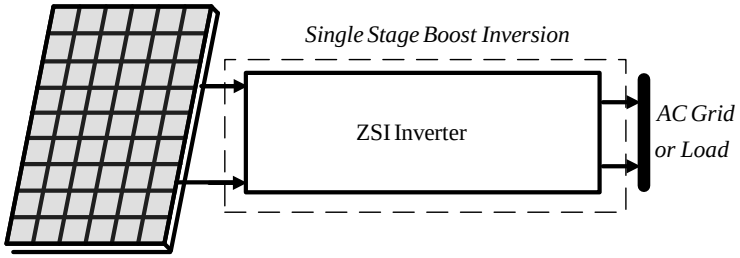
Nowadays ZSIs are widely employed in many applications, catering for all types of electric power conversion (AC-AC, AC-DC, DC-AC, DC-DC). However, these ZSIs have severe short comings that are discussed in the next section.

1.2 Problem Statement

In PV generation systems, the voltage produced by a solar cell is very low (a single solar cell usually generates .5 volt). One way to increase the input voltage is the series connection of PV panels. However, this is not recommended practice because of the substandard power conversion efficiency and will reduce the lifetime of the PV panels [5]. To overcome this problem, modular systems have been proposed, such as the example shown in Fig 1.3(a) [6].



(a)



(b)

Fig. 1.3. PV systems (a) Two-stage power conversion (b) Single-stage power conversion

In these systems, an independent high step converter followed by conventional VSI was applied to the PV panel to increase the output voltage. However, due to the utilization of more switching devices and two stage power conversion, the cost and complexity of such a system increases. In order to replace these two stage power conversion systems with single stage power conversion, ZS inverters are utilized, as shown in Fig. 1.3(b). But the boost factor of these ZSIs needs to be enhanced in order to meet the desired output voltage while keeping in view the limitations of the components as well

Since the first publication of ZSI, many researchers have focused on developing new Z-source topologies with improved modulation schemes, boost capabilities, dynamics and control methods, and have introduced them in many diverse studies [7-45]. In [7] a family of quasi-Z-source inverters (qZSIs) were introduced, which have benefits over the ZSIs, such as sharing of common ground, improved input profiles and lower component voltage stresses. Despite these significant benefits and theoretical infinite voltage gains, all of these qZSIs suffer from one serious drawback: their practical boost abilities (*B*) are restricted due to higher component stresses and low output power quality, which is caused by the tradeoff between the modulation index (*M*) and the shoot-through duty cycle (*D*).

$$B = \frac{v_{pn}}{V_{in}} = \frac{1}{1 - 2D} \tag{1.1}$$

$$M = 1 - D \tag{1.2}$$

Equation (1) shows the relationship between the boost factor and the shoot-through duty cycle of the ZSI for a given value of input voltage. From (2), it can be inferred that the duty cycle and modulation index are interdependent, i.e. to achieve a higher boost factor, shoot-through duty cycle has to be increased which in turns consequently decreases the modulation index. Reduced modulation index results in lowering the quality of the output power, reduced power factor as it gives significant rise to total harmonic distortion (THD) while decreasing the AC output voltage fundamental component [8]. Furthermore, with the utilization of higher *D* and lower *M*, leads to higher voltage stresses across the passive (inductors, capacitors, diodes etc) and switching devices due to poor usage of dc-link voltage.

Therefore, transformer based ZSIs were proposed [9-17]. They employs a transformer (coupled inductor) in the impedance network and utilizes its turns ratio to increase the boost factor while keeping the duty cycle lower. However, with the use of higher secondary windings isolation between the windings is increased which causes the leakage inductance to increase manifolds. Huge voltage spikes occurs across the switching devices and switching losses becomes more prominent, therefore addition of extra clamping circuits are required. Moreover, with higher turns ratio and increased secondary windings

the size of the magnetic component becomes significantly higher resulting in bulky and oversized power system.

Another major concern among ZSIs is that the typical existing circuits do not use any electrical isolation. Therefore, when these ZSIs are used in photo-voltaic modules as grid inverters, a DC current is injected in the grid which may cause saturation of the distribution transformer [46, 47] as well as poor power quality, higher loss, and overheating of the power system. According to IEEE Standard 1547-2003, the level of DC component injected into grid should be less than 0.5% of the rated output current [48-50]. In order to avoid this injection of DC current into the grid, and to fulfil safety standards, the conventional approach is to incorporate a line frequency transformer between the inverter and the grid. However, this low frequency transformer is bulky, heavy, expensive, and decreases the efficiency and power density of the system. Many other methods have also been developed to minimize the injection of DC currents into the grid within transformer-less inverters (e.g. existing ZSIs). Most of these methods for blocking DC currents include a DC capacitor [50], voltage and current detection-based techniques. However, they either use bulky and expensive capacitors, or voltage and current sensing circuitry, yet may not guarantee the safety standards are met.

These are the challenges needed to be addressed and overcome in developing a reliable, and minimal loss power converter system that will have an overall improved spectral performance compared to existing ZSI circuits.

1.3 Aim and Sub-objectives

The overarching aim of this thesis is the improvement in variety of aspects of impedance source inverters and converters. This includes the output gain of the inverter, total cost of the system, complexity of the system, dynamic response of the inverter. Additionally, modulation strategies will be modified to effectively control the proposed inverter system. From this aim, the following research objectives were established for this work:

1. Develop understanding about the operating principles and features of impedance source inverters and converters.
2. Advancement in the circuitry of impedance source inverters (DC-AC) which results in improved voltage gains, less complexity and cost-efficient systems.
3. Implementation of high frequency electrical isolations resulting in protection, safety and avoids the injection of circulating currents into the grid with the utilization of higher modulation index.
4. Modifications in the modulation strategies for the advanced impedance source inverters resulting in simpler control.
5. Implementation of parallelising multiple inverters to the class of impedance source inverters which in turns results in increased output voltage, reduced component stress by sharing the currents, ease of maintenance, modularity facilitating plug and play, higher reliability, and (N+1) redundancy. Moreover, by parallel operation of inverters, output ripples can be reduced by utilizing interleaving mechanism, which will reduce the requirements for output filters.
6. Development of new class of transformer based impedance source AC-AC converters with novel control strategies to increase the voltage gains and to improve conglomerate characteristics of the converters.
7. Design and development of hardware laboratory prototypes of proposed structures to validate their advantages and benefits over existing topologies and improve their overall efficiencies.

All of the proposed structures will be comprehensively discussed with brief analysis and theoretical derivations will be done that would be the major focal point of this thesis. Saber models will be presented and simulations will be performed to verify their working principles. Comparisons with existing topologies will be made to show efficiency improvements of the proposed power converters. At the end, hardware prototypes are built to validate their advantages that is the second major task of the thesis project.

1.4 Research Questions

The main idea of the proposed Z-source inverters is to overcome the drawbacks faced with the existing topologies such as leakage inductance problem, complex structure, low gain, low modulation index value, and high stress issue. Thus, to confirm the benefits claimed, efficiency plots are highly important.

The research questions to be answered in this thesis are:

1. How should the power losses and efficiencies be calculated?
2. What methods to applied for improving the voltage gain of the proposed inverters?
3. How will the voltage clamping technique be applied to the proposed inverters?
4. How should the dc circulating current be controlled in isolated impedance source inverters?
5. What control methods are applicable for the proposed isolated structures?
6. How to implement the interleaving mechanism in the existing modulation strategies of parallel operated impedance source inverters?

A more detailed description of these research questions are discussed in the proposed design plan and the procedures that are taken into account to achieve the required results.

1.5 Methodology

The methodology focuses on planning the research steps followed for the modelling and design of an improved impedance source inverters and the implementation of electrical isolations and parallelization of ZSIs. It will also consider the measurement methods which are to be used for the analysis and process results with simulation modellings and the design of the experimental setup that is required for the physical testing.

1.5.1 Literature Review

The literature review will focus on studying impedance source inverters and their control techniques. This part of the project is discussed in much detail in Chapter 2 and it will investigate the operating principles and their working in a very comprehensive

manner and identify their significant features and contributions to the field of power electronics with their pros and cons and the motivation behind the thesis project.

1.5.2 Research Plan

This research project is designed around the sequence of multiple steps as illustrated in Fig. 1.4 below. The figure provides detail of the research process in the form of a flow chart which will be carried out to achieve the research goals as described in Section 1.3. The flow chart shows the step by step approach to achieve the final goal of this thesis and the major phases of the project. It includes the measurement methods and techniques that will be used for the complete analysis and verifications of the impedance source inverters.

The major part of research plan consists of four significant contributions of the project. Initially, the research plan is to survey in detail the main Z-source topology, its features, applications and modulation (control) strategies followed up by comprehensive study of DC-AC, AC-AC Z-source power circuits. Afterwards, step by step approach for the derivation of improved ΓZSI with clamping diode, implementation of HFT, parallelization of ΓZSI and other ZSIs, and transformer based AC-AC ZSIs with brief analysis including detail testing will be carried out.

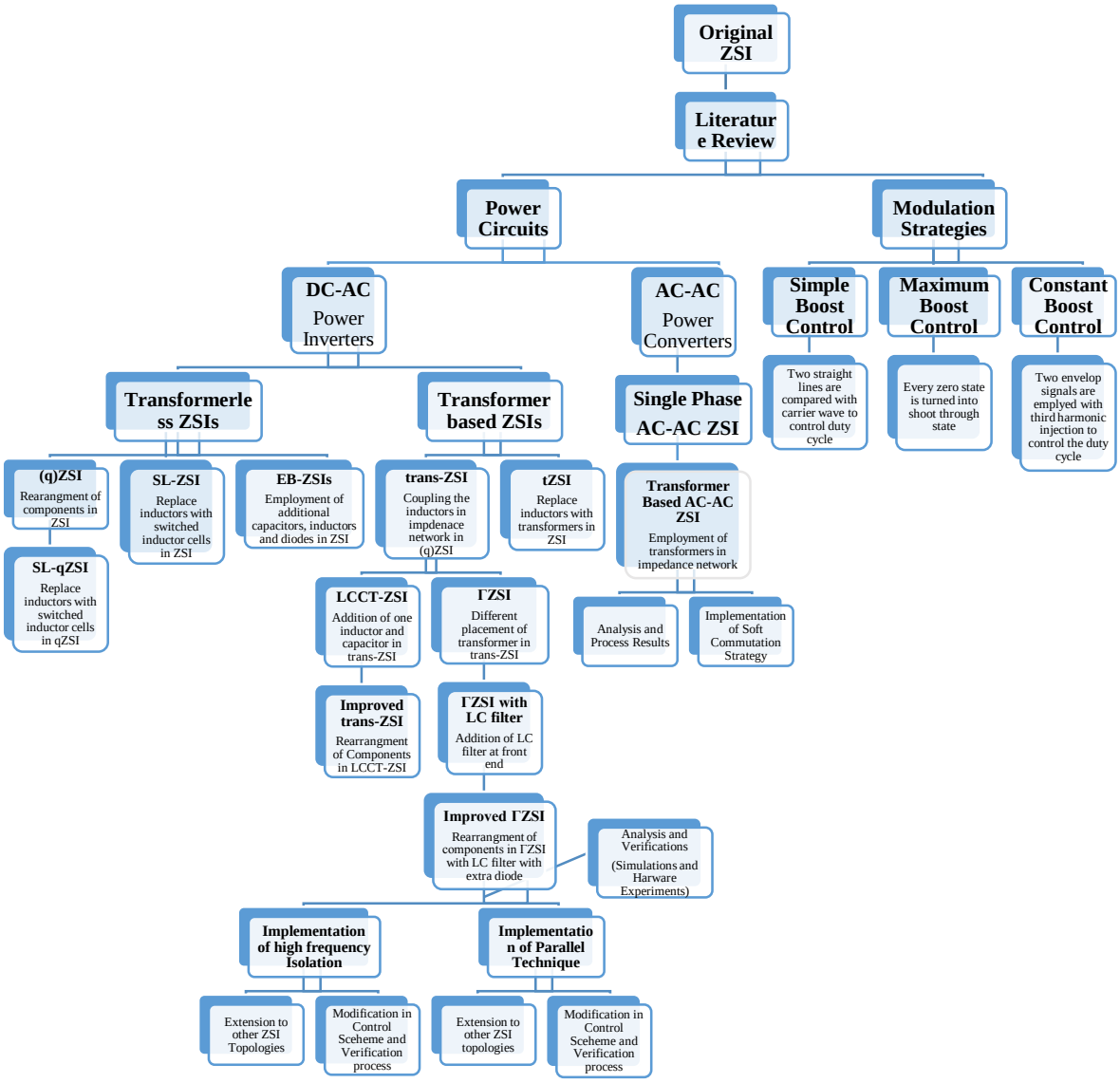


Fig. 1.4. Flow Chart of the Planned Research Process

1.6 Research Outputs

This section lists the articles have been published from this thesis project, including those which are in press and anticipated to be published shortly. Refereed conference are

indicated by the "(C)" numbers, and peer-reviewed journal are indicated by the "(J)" numbers. The outputs are as follows:

C1. Z. Aleem, and M. Hanif, "Improved Γ-Z-Source Inverter," in *IEEE Energy Conversion Congress and Exposition*, Sep. 2016, pp. 1-5.

C2. Z. Aleem, and M. Hanif, "A Class of Parallel Operated Impedance Source Inverters," in *IEEE Annual Southern Power Electronics Conference*, Dec. 2016, pp. 1-6.

C3. Z. Aleem, and M. Hanif, "Single-Phase Transformers Based Z-Source AC-AC Converters," in *IEEE Annual Southern Power Electronics Conference*, Dec. 2016, pp. 1-6. (Received Paper Award).

C4. Z. Aleem, S. Winberg, A. Iqbal and M. Al-Hitmi, "High Frequency Transformer Based Improved Gamma ZSI with Lossless Snubber," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Washington, DC, 2018, pp. 3731-3736.

C5. Z. Aleem, and M. Hanif, "Current-Fed Converters with Switching Cells," in *IEEE Energy Conversion Congress and Exposition*, Sep. 2016, pp. 1-7.

J1. Z. Aleem and M. Hanif, "Operational Analysis of Improved Γ-Z-Source Inverter With Clamping Diode and Its Comparative Evaluation," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9191-9200, Dec. 2017.

J2. Z. Aleem, S. Winberg, A. Iqbal, M. A. Al-Hitmi and M. Hanif, "Single-Phase Transformer based HF-Isolated Z- Source Inverters with Voltage Clamping Techniques for Solar PV Applications," in *IEEE Transactions on Industrial Electronics*. doi: 10.1109/TIE.2018.2889615

J3. Z. Aleem, S. Winberg, and H. F. Ahmad "A Class of Single-Phase Z-Source AC-AC Converters Based on Transformers with Safe-Commutation Strategy", (Submitted in IEEE transactions on Industrial Informatics).

1.7 Organisation and Scientific Contributions of the Thesis

This research project contributed an overall approach to the modelling and development of advanced impedance source inverters with high frequency isolation technique and parallel connected inverter operations. Accordingly, this approach has involved tasks of reviewing relevant studies from the literatures, surveying industry standards, trends and practical implementation of these topologies in a specific and controllable manner. The chapters in this thesis are arranged according to the modelling techniques and methods used to propose and analyse designs, rather than following the historical progression of how this investigation proceeded.

Chapter 2 presents the literature overview of the Z-source power control topologies and their modulation strategies are discussed. The merits and demerits of these topologies are identified. It concludes by justifying the proposition of improved ZSIs with HFTs and parallel connection of ZSIs in this thesis.

In Chapter 3, the improved ΓZSI with voltage clamping technique is proposed and detailed analysis is presented. Its comparative evaluations with the existing topologies are also discussed and verified its advantages over existing inverters through simulations. Efficiency plots are also given and in the end a hardware prototype is fabricated and experimental studies are investigated.

Chapter 4 the use of high frequency transformer is discussed and implemented. Its advantages in terms of protection and safety are elaborated. Then this HFT technique is applied to all existing ZSI topologies and their theoretical and virtual analysis are shown. New modulation method for the control of HFT-ZSIs is also proposed and voltage clamping diodes are implemented. In the end of this chapter an experimental setup of HFT-improved ΓZSI is prepared and experiments are performed.

Parallel operation of improved ZSI with magnetic coupling is proposed and presented in Chapter 5 to increase the power of the system up to several KWs. This concept is extended to other ZSI topologies and extensive simulations are performed. Interleaving mechanism is used to lower the output filter requirements. A hardware prototype is fabricated based on DSP Kit TMS320f28335 for the control of switching devices. The

interleaving method is implemented through DSP programming by phase shifting the switches of inverter bridge 2 by 180°.

Chapter 6 focuses on the development of new class of transformer-based impedance source AC-AC converters. The proposed converters provides a wide range of step up and step down functions with maintaining or reversing the phase angle. It can produce a higher boost factor than existing Z-source AC-AC converters with continuous input currents and improved input profiles. A soft commutation strategy is also discussed. The operation of the proposed converters is validated mathematically, virtually through simulations and through experimental hardware prototypes and results.

Finally, Chapter 7 concludes this thesis by summarizing the main findings and presenting significant observations. The last section provides recommendations for future research.

2. Chapter 2

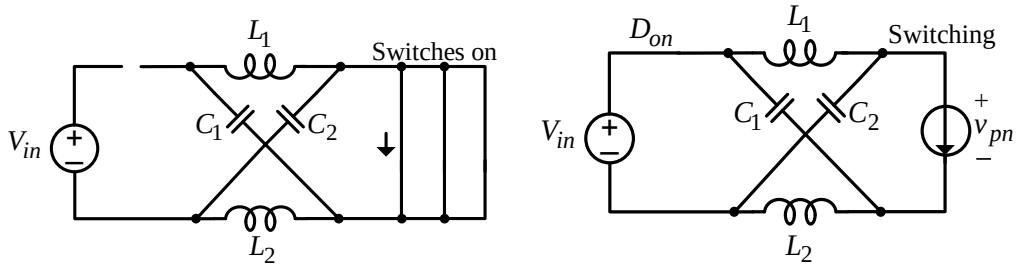
Review of the Z-Source Converter Topologies and their Modulation Strategies

Various converter topologies have been developed, according to recent literature, to overcome the limitations and problems of the traditional voltage source, classical buck/boost, unidirectional, and bidirectional converter topologies [51-55]. Proper implementation of the impedance-source network (ZSI) with appropriate switching configurations and topologies reduces the number of power conversion stages in the system power chain, which may improve the reliability and performance of the power system.

2.1 Z-Source Inverter (ZSI)

The basic impedance-source network can be generalized as a two-port network with a combination of two basic linear energy storage elements, i.e., *L* and *C* (dissipative components (*R*) are generally omitted). However, different configurations of the network are possible to improve the performance of the circuit by adding different nonlinear elements into the impedance network, e.g., diodes, switches, and/or a combination of both.

A three-phase voltage-fed ZSI, as shown in Fig. 2.1, is used as an example to briefly illustrate the operating principle as described previously. The three-phase ZSI bridge has nine permissible switching states (six active states, two zero states, and one shoot-through state) shown in Fig. 2.1 unlike the traditional three-phase VSI which has eight (six active states, two zero states) [1].



(a) (b)

Fig. 2.1. Operation modes (a) Shoot-through state (b) Non-shoot-through state

During zero states, the upper three or lower three switches of the inverter bridge are turned on simultaneously, thus shorting the output terminals of the inverter and producing zero voltage across the load. During one of the six active states, the DC voltage is impressed across the load, positively or negatively. However, during shoot-through states, the load terminals are shorted through both the upper and lower devices of any one-phase leg, any two phase legs, and all three-phase legs producing zero voltage across the load. This shoot-through state has the same effect, i.e., producing zero voltage across the load as the traditional zero states; however, these shoot-through states can boost the output voltage. The shoot-through state is forbidden in the traditional VSI, because it would cause a short circuit across the dc link and damage the inverter. The *Z*-source network and the shoot-through zero state provide a unique buck–boost capability for the inverter by varying the shoot-through time period and modulation index *M* of the inverter. Theoretically, the output voltage of the inverter ($\widehat{v_{ph}} = MB/2 = M[1 - 2D_{sh}]^{-1}V_{in}/2$) can be set to any value between 0 and ∞ . However, some practical aspects and performance of the converter need to be considered for large voltage buck or boost operation, (as discussed in section 1) e.g., to avoid exceeding device limitations.

2.2 Pulse Width Modulation Strategies for Z-Source Inverters

Many PWM methods have been developed for the control of three phase voltage-source inverters. Traditionally voltage-source inverters have eight switching states, six active states in which energy is transferred to load, and two zero states in which either the

upper switches or lower switches of all the legs are switched off and thus the output voltage to the load is zero.

The ZSI has an additional zero state, which is forbidden in the voltage-source inverters. Insertion of this zero-state became the focal point of these control schemes. Three different PWM schemes are proposed in [21-24] are discussed in the next section.

2.2.1 Simple Boost Control

As in (2.1) the gain of the Z-source inverter is expressed as

$$B = \frac{1}{1 - 2D} \tag{2.1}$$

$$\widehat{v_{ph}} = MB\, {V_{in}}/{2} \tag{2.2}$$

Where, D is the shoot-through duty of the switches, which is defined in (1.2) as $M = 1 - D$. It can be seen that the modulation index and shoot-through duty are interdependent. Fig. 2.2 illustrates the simple boost control scheme for Z-source inverter [4, 24]. It employs a straight line equal to or greater than the peak value of three phase references to control the duty ratio. In simple boost control, the modulation index decreases significantly with the increase in shoot-through duty. In order to have a large boost gain, a smaller modulation index has to be used which results in high voltage stress on the inverter bridge. For any desired voltage gain the maximum modulation index can be achieved is

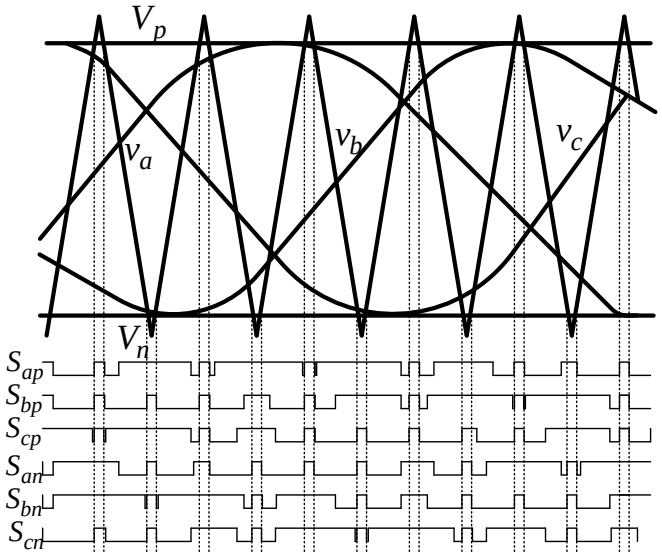


Fig. 2.2 Simple boost control

$$M = \frac{G}{2G - 1} \tag{2.3}$$

Whereas G is the gain of the inverter. Fig 2.3 shows the plot curve of modulation index versus the voltage gain of the inverter with simple boost control. The voltage stress V_s across the switches are as follows

$$V_{sw} = BV_o(2G - 1)V_o \tag{2.4}$$

From this equation, it can be inferred that in simple boost control the voltage stress across the switches is quite high which will restrict the voltage gain because of the limitation of device voltage rating. The curve of switches voltage stress versus the voltage gain is plotted in Fig. 2.4.

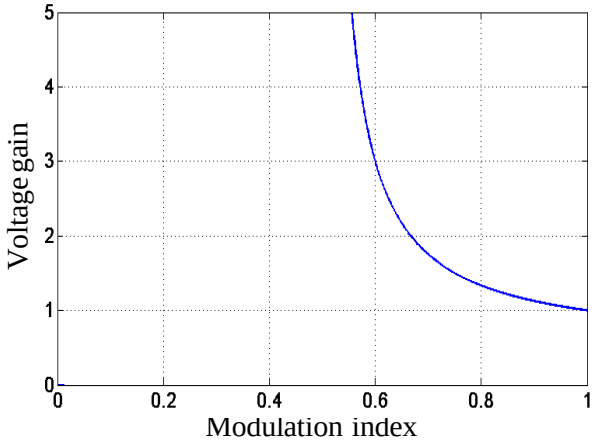


Figure 2.3 Voltage gain of the simple boost control

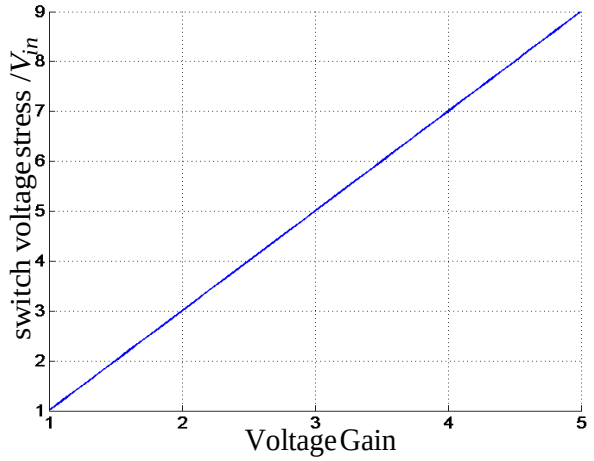


Figure 2.4 Switch voltage stress versus the voltage gain

2.2.2 Maximum Boost Control

In simple boost control, the obtainable shoot-through duty decreases with the increase in modulation index as given by (1.2). Moreover, from Fig. 2.4 it can be inferred that switch voltage stress is quite high which restricts the achievable voltage gain of the inverter due to the limitation of the device voltage rating.

Reducing the voltage stress while keeping gain higher becomes important for the control of Z-source inverter. To attain this objective, the shoot-through duty should be as large as possible with enough modulation index to minimize the voltage stress across the switches. Fig. 2.5 shows the strategy of maximum boost control [21].

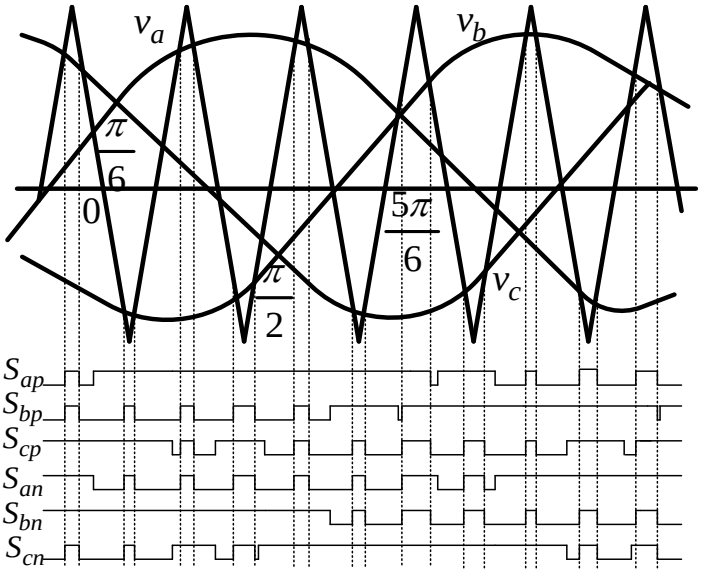


Fig. 2.5 Maximum boost control

It is similar to the traditional carrier-based PWM scheme. It maintains all the active states unchanged and turn all the zero states into shoot-through states, thus maximum boost factor is achieved for any given modulation index. From Fig. 2.5, the circuit is in shoot-through state whenever the triangular carrier wave is either greater than or lower than the reference sinusoidal waveforms. The shoot-through duty in maximum boost control varies each cycle and this zero state repeats periodically every $\frac{\pi}{3}$. Thus the voltage gain can be expressed as:

$$G = MB = \frac{\pi M}{3\sqrt{3}M - \pi} \tag{2.5}$$

The curve of voltage gain versus modulation index is shown in Fig. 2.6. As can be seen output voltage increases when *M* decreases and reaches to infinity when *M* approaches to $\frac{\pi}{3\sqrt{3}}$. On the other hand a higher modulation index for any voltage gain results in lower voltage stress. Thus the voltage stress is given by

$$V_{sw} = BV_{in} = \frac{3\sqrt{3}G - \pi}{\pi} V_{in} \tag{2.6}$$

The voltage stress versus the voltage gain curve is shown in Fig 2.7. Compared to simple boost control the voltage stress across the switches in maximum boost control is much lower. With maximum boost PWM scheme the inverter can be operated to achieve a higher voltage gain for given active devices.

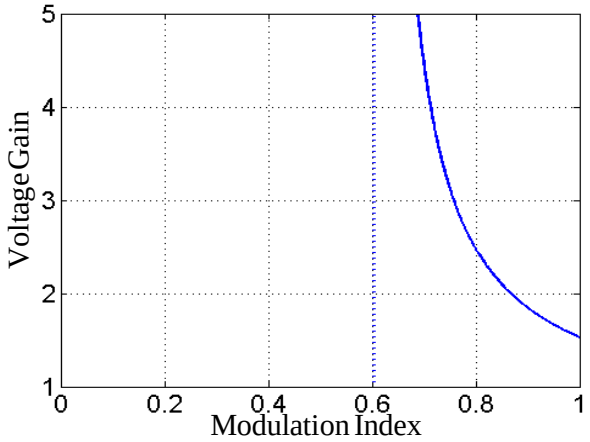


Fig. 2.6 Voltage gain of the maximum boost control

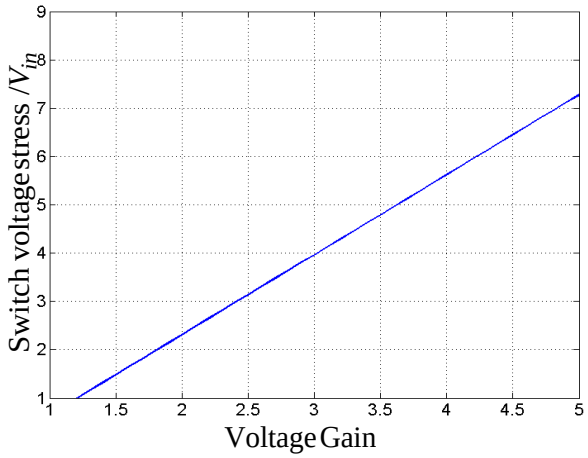


Fig. 2.7. Switch voltage stress versus the voltage gain

2.2.3 Maximum Constant Boost Control

As compared to simple boost control the voltage stress across the switches in maximum boost control is much lower as it turns all the zero states into shoot-through states. However, this control scheme has a serious drawback, the shoot-through duty cycle is not constant in this method which introduces a low-frequency current ripple that is associated with the output frequency of the inductor current and capacitor voltage. This

ripple increases the requirements of passive components when the output frequency is very low which in turns effects the overall efficiency of the system in terms of cost and size. In order to address this problem, constant shoot-through duty is needed to eliminate this low output frequency ripple. Consequently, a greater modulation index with high enough duty cycle is required to achieve both lower voltage stress and high gain of the inverter. In 2006 [22], maximum constant boost control scheme was proposed. Fig. 2.8 shows the sketch map of this control scheme.

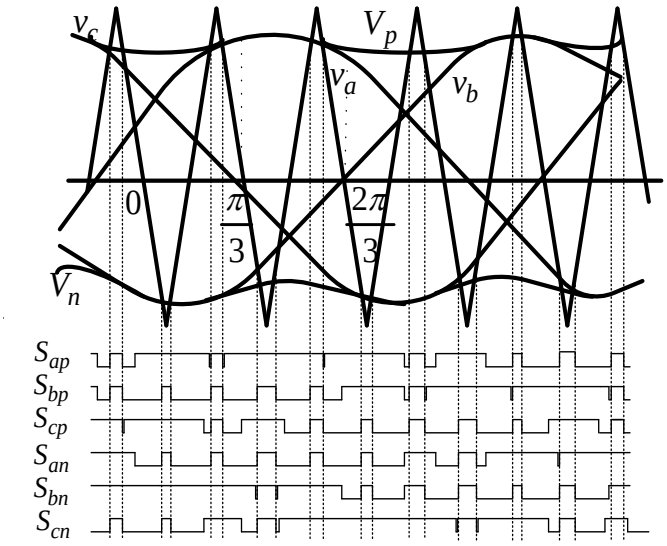


Fig. 2.8 Maximum constant boost control

As can be seen from the Fig, there are five modulation curves in this scheme, three reference signals v_a, v_b, and v_c, and two shoot-through envelop signals V_p, and V_n. When the carrier wave is greater than or lower than these envelop signals the inverter is turned into shoot-through states. The shoot-through duty must be kept same from switching cycle to switching cycle to have a constant boost. The voltage gain is expressed as follows

$$G = MB = \frac{M}{\sqrt{3}M - 1} \tag{2.7}$$

Fig. 2.9 shows the curve of voltage gain versus modulation index, as it is shown voltage gain approaches to infinity when *M* decreases to $\frac{\sqrt{3}}{3}$.

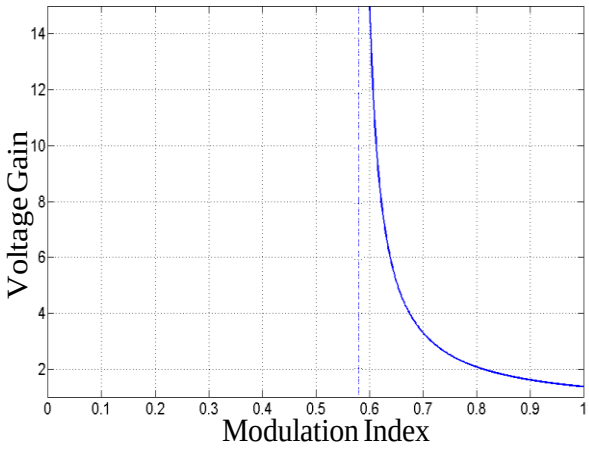


Fig. 2.9 Voltage gain of the constant boost control

Similarly, all the PWM schemes can be implemented using third harmonic injection. Third harmonic injection is usually used in three phase inverter systems to increase the modulation index range. It can be utilized here to increase the modulation index range which would result in increased voltage gain range.

2.2.4 Summary

Three control methods: Simple boost control, maximum boost control and constant boost control were presented in this chapter. The ratios of the voltage stress to the equivalent input DC voltage of simple, maximum and constant boost control are summarized as:

$$\frac{V_s}{GV_{in}} = 2 - \frac{1}{G} \quad \text{for simple control} \tag{2.8}$$

$$\frac{V_s}{GV_{in}} = \frac{3\sqrt{3}G - \pi}{\pi} \quad \text{for maximum control} \tag{2.9}$$

$$\frac{V_s}{GV_{in}} = \sqrt{3} - \frac{1}{G} \quad \text{for constant control} \tag{2.10}$$

Fig. 2.10 shows the voltage stress ratios of the three modulation schemes. From Fig. it can be inferred that the constant boost control has a much lower voltage stress across the switches than simple boost control but have a slightly higher stress than maximum boost control.

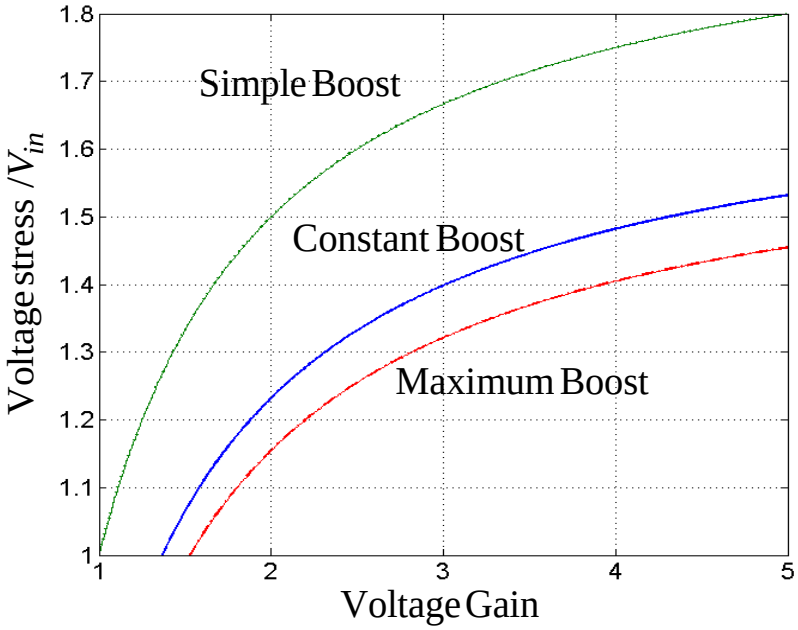


Fig. 2.10 Voltage stress comparison

2.3 Transformer-less ZSIs

This section will provide a brief overview of the existing ZSIs, reviewing in particular the following approaches: the quasi(q)-ZSI [7], extended boost ZSIs [20] (capacitor assisted, diode assisted), switched inductor(SL)-ZSI [8], SL-qZSI [28], trans-ZSI [9], LCCT-ZSI [10], improved trans-ZSI [11], TZSI [12], and gamma(Γ)-ZSI [14] together with a discussion of their pros and cons.

2.3.1 Quasi-ZSI (qZSI)

QZSI is derived by rearranging the components in original ZSI circuit. Fig. 2.11 shows the basic structure of how qZSI is implemented [7]. As can be seen from the Fig. 1.2, the capacitor C_2 and input voltage share the common ground. Therefore, C2 can be moved to top side and then the voltage across C_2 is reduced from V_{c2} to $(V_{c2} - V_{in})$ in the new configuration. Once this alteration is made, L_1 is connected in series with V_{in}. Rearranging the circuit leads to the qZSI shown in Fig. 2.11.

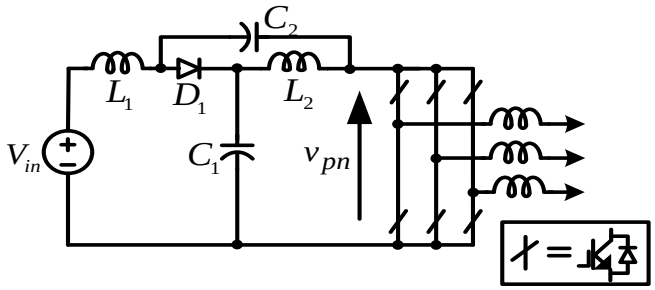


Fig. 2.11. Quasi-Z-source inverter

2.3.2 Diode-Assisted Extended-Boost ZSI (DA-EBZSI)

To overcome the gain limitation as discussed earlier without further reducing the modulation index extended boost ZSIs were proposed [20]. Fig. 2.12 shows the basic topology of extended boost diode-assisted ZSI. This topology adds additional two diodes, one inductor, and one capacitor in the Z-source topology to have higher gain than original ZSI.

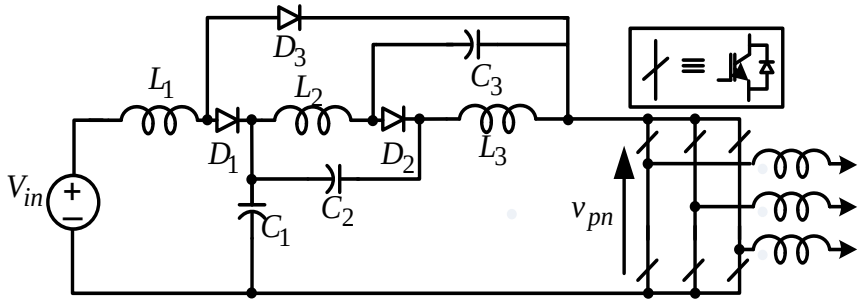


Fig. 2.12. DA-EBZSI

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{(1-D)(1-2D)} \tag{2.11}$$

Equation (2.11) shows the boost factor of the extended boost diode assisted ZSI which is higher than the original ZSI at the expense of more diodes, inductors and capacitors which increases the cost and complexity of the overall system.

2.3.3 Capacitor-Assisted Extended-Boost ZSI (CA-EBZSI)

Fig. 2.13 shows the basic topology of extended boost capacitor assisted ZSI. As compared to the previous topology this structure adds additional two capacitors, one

inductor, and one diode (as the name suggests) in the Z-source topology to have slightly higher gain than DA-EBZSI.

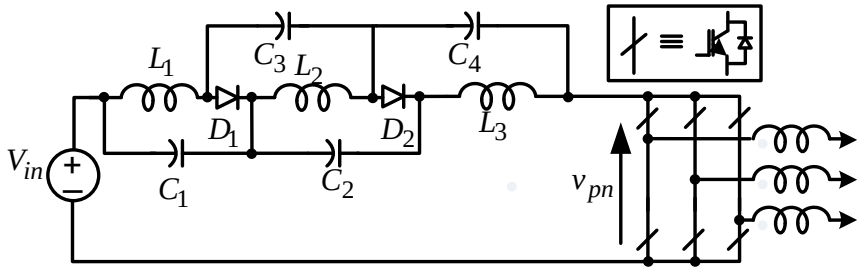


Fig. 2.13. CA-EBZSI

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{1-3D} \tag{2.12}$$

Similarly, CA-EBZSI have more capacitors instead of diodes in the impedance network compared to DA-EBZSI. But both of these circuits have large no. of components only to increase the boost factor of the inverter circuit.

2.3.4 Switched Inductor ZSI (SL-ZSI)

The SL-ZSI is shown in Fig. 2.14, which is obtained by replacing the two inductors L_1 and L_2 in the classical ZSI with SLs [8], each of which consists of two inductors and three diodes. By adding six additional diodes and two inductors, it obtains a boost factor of (1+D) / (1-3D), which is much larger than that of the classical (q)ZSIs.

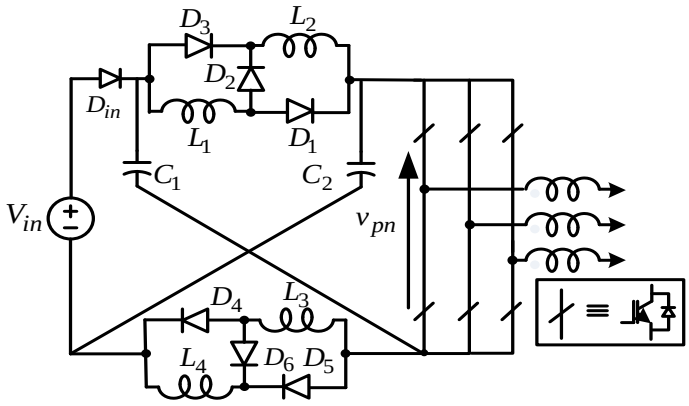


Fig. 2.14. SL-ZSI

2.3.5 Switched Inductor qZSI (SL-qZSI)

Due to the drawbacks faced by SL-ZSI, such as huge inrush current, discontinuous input current, absence of common ground between input voltage and inverter bridge and large number of components, switched inductor quasi Z-source inverter was proposed [28] shown in Fig. 2.15.

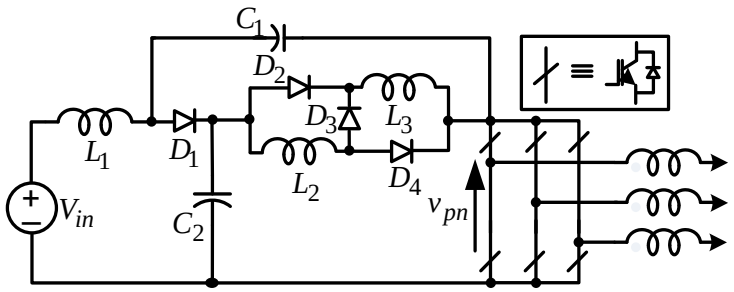


Fig. 2.15. SL-qZSI

The SL-qZSI inverter is obtained by replacing inductor L_2 in the classical qZSI with the same SL as that used in the SL-ZSI. Compared to the SL-ZSI, it has continuous input current, common ground between the dc-voltage source and the inverter-bridge, and has no startup inrush current. Nevertheless, its boost ability is $(1 - D)/(1 - 2D - D^2)$, which is significantly lower than that of the SL-ZSI, and, hence, dilutes its other advantages over SL-ZSI.

2.4 Transformer Based ZSIs

Despite having higher gains, the boost capability remains limited, and its further enhancement requires the use of multiple extensions of the same components, which increases the volume and cost of the inverters and effects of the parasitic components become more severe. To overcome these issues, transformer based impedance source inverters are proposed [9-17] to achieve high voltage gains by keeping the component count as low as possible. These inverters induce a coupled inductor in the Z-source network and utilize the turns ratio of the magnetic component to increase the voltage gain of the inverters. This section reviews the different transformer based ZSI topologies presented in literature.

2.4.1 Trans-ZSIs

The trans-Z-source [9] inverter induces a coupled inductor in the impedance network and the voltage of inductor L_1 is reflected to inductor L_2 through magnetic coupling, therefore capacitor C_2 can be removed from the impedance network. The boost factor B (ratio of dc-link v_{pn} to input voltage) of the trans-Z-source inverter is defined as

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{1-(1+n)D} \tag{2.13}$$

where, n is the turns ratio of the coupled inductor and can be adjusted according to the desired output value. Fig. 2.16 shows the basic structure of trans-ZSI.

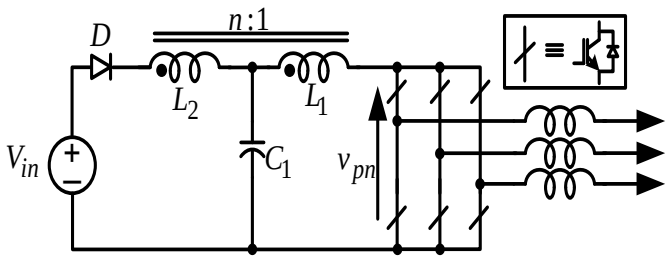


Fig. 2.16. Trans-ZSI

2.4.2 LCCT-ZSI

Fig. 2.17 shows an inductor-capacitor-capacitor transformer (LCCT) ZSI [10] which adds one additional inductor and capacitor to offer some benefits over the trans-Z-source inverter such as continuous input profiles and reduced inrush current at startup. However, these benefits are attained at the expense of more components while retaining the same voltage gain and other features of trans-ZSI.

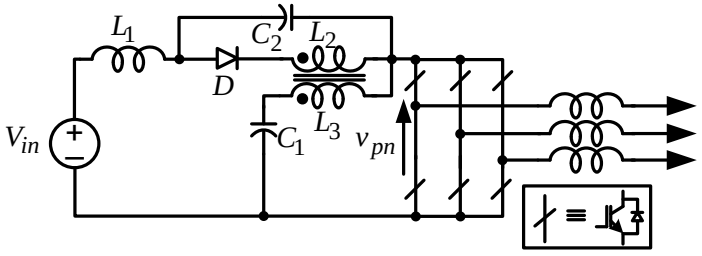


Fig. 2.17. LCCT-ZSI

2.4.3 Improved trans-ZSI

In, [11], improved trans-ZSI was proposed as shown in Fig. 2.18. The improved trans-ZSI overcomes the issues of trans-ZSI which are discontinuous input current, inrush current at startup and unlike LCCT-ZSI, the improved trans-ZSI also provides higher voltage gain compared to LCCT and trans-ZSI. The boost factor is as follows

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{1-(2+n)D} \tag{2.14}$$

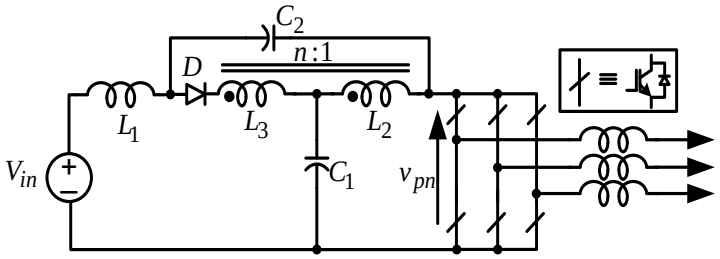


Fig. 2.18. Improved trans-ZSI

2.4.4 TZSIs

Similarly, in 2013 a new family of TZ-source inverters was proposed [12] as shown in Fig. 2.19. These inverters replace the inductors with the transformers (T_1 and T_2) to achieve a higher gain than conventional trans-Z-source and improved trans-Z-source inverters. The boost ability of the TZSI is expressed as

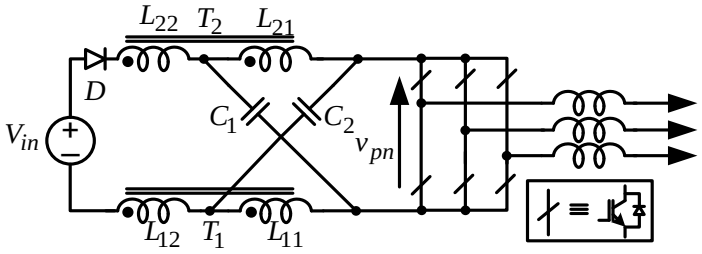


Fig. 2.19. TZSI

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{1-(2+n_1+n_2)D} \tag{2.15}$$

where, n_1 is the turns ratio of T_1 and n_2 is the turns ratio of T_2. The voltage gain of the inverter is adjusted by varying the turns ratio of the transformers. Even with a turns ratio of 1 ($n_1 = n_2 = 1$) the TZSIs produces higher gain than the trans-ZSIs.

2.4.5 Γ-Z-Source Inverter (ΓZSI)

The ΓZSI shown in Fig. 2.20 boosts the output voltage by lowering the turns ratio of the transformer rather than increasing it. As compared to other transformer based impedance source topologies, the ΓZSI [14] uses the same or less number of components for producing higher voltage gain while utilizing a higher modulation index and consequently a lower shoot-through duty ratio. Moreover, the output voltage of the ΓZSI is adjusted by varying the turns ratio of the magnetic component within a narrow range of $1 < n \leq 2$. This leads to lesser winding turns and confined transformer size to achieve higher gain which makes it more preferable in the industrial applications. The boost ability of the inverter is expressed as:

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{1 - \left(1 + {}^{1}/_{n-1}\right)D} \tag{2.16}$$

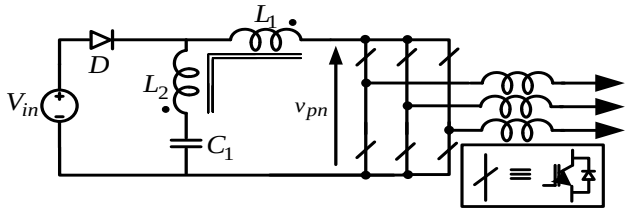


Fig. 2.20. ΓZSI

Although the inverters discussed earlier are attractive and have several significant features, the transformer turns ratio might become too high for obtaining high voltage gain which leads to oversized and bulky transformers. Additionally, there are several short comings associated with these inverters, e.g. discontinuous input currents, huge inrush current at startup in the case of trans-ZSI, TZSI, and ΓZSI thus requiring additional LC filter at the front end [33], absent common ground b/w input and inverter bridge in TZSI, addition of more components in TZSI, improved trans-ZSI, LCCT ZSI resulting in increased cost of the overall system. In all other transformer based Z-source topologies, to get higher boost larger turns ratios are needed, which requires more isolation between

the windings, which will in turn cause the leakage inductance to increase manifolds. This leakage inductance is directly in series with inverter-bridge without any snubber circuit in between and, therefore, large *di* / *dt* caused by the switching of the windings currents results in large switch-voltage spikes. In this thesis, new structures for the ZSIs are discussed to improve several features of the impedance source topology including voltage gains and then voltage clamping technique is implemented to overcome the voltage overshoots. These proposed structures of ZSIs can utilize higher modulation index and thus have improved output power quality and efficiencies. High frequency electrical isolations and parallel operating methods are also implemented which can provide more safety and protection in terms of meeting IEEE safety standards by providing galvanic isolation, redundancy and modularity.

Table 2.1 summarizes the features of different transformer based ZSIs discussed earlier.

TABLE 2.1

	Trans-ZSI	LCCT-ZSI	Improved trans-ZSI	TZSI	ΓZSI	ΓZSI with LC
Boost Factor	$\frac{1}{1-(1+n)D}$	$\frac{1}{1-(1+n)D}$	$\frac{1}{1-(2+n)D}$	$\frac{1}{1-(2+n_1+n_2)D}$	$\frac{1}{1-(1+{}^{1}/_{n-1})D}$	$\frac{1}{1-(1+{}^{1}/_{n-1})D}$
Components in impedance network	3	5	5	5	3	5
Gain	Higher than ZSI with increase in turns ratio	Same as trans-ZSI	Higher than trans-ZSI with same turns ratio	Higher than improved trans-ZSI with same turns ratio	Gain is increased by decreasing the turn ratio	Same as ΓZSI
Input current	Discontinuous	Continuous	Continuous	Discontinuous	Discontinuous	Continuous
Inrush current	High	Low	Low	High	High	Low
Share ground	Yes	Yes	Yes	No	Yes	Yes
Leakage inductance problem	Yes	Yes	Yes	Yes	Yes	Yes

3. Chapter 3
Improved ΓZSI with Clamping Diode

3.1 Introduction

The Γ-Z-source inverter shown earlier in Fig. 2.20 boosts the output voltage by lowering the turns ratio of the transformer rather than increasing it resulting in small transformer size and lower cost making it more preferable as compared to other transformer based ZSI topologies. However, despite having these features, the Γ-Z-source inverter suffers from several serious drawbacks:

1. The input current is discontinuous, thus requiring an additional *LC* filter at the front end of the Γ-Z-source inverter as shown in Fig 3.1 [33], to eliminate the discontinuity of the input current and protect the energy source.
2. There is huge inrush current at startup and the resulting voltage and current spikes can damage the devices. It appears due to large resonant current flowing in to the input diode, transformer windings, capacitor, and body diodes of the IGBTs.
3. The Γ-Z-source inverter uses the same number of components as of trans-ZSI but with a different transformer placement. This difference in dot polarities of the magnetic component causes the capacitor C1 current to bypass, which is very high. This leads in the increment of current ratings and cost of the switching devices.
4. The leakage inductance of the transformer is utilized to minimize the current of capacitor C1, however the leakage inductance is in series with the inverter bridge without any snubber circuit causing large voltage spikes due to the switching of the winding currents.

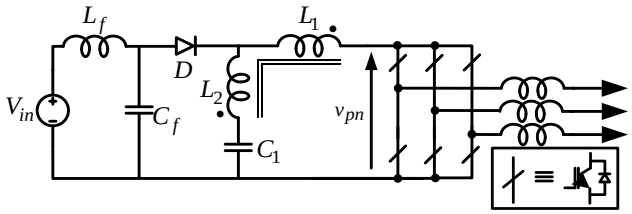


Fig. 3.1. ΓZSI with LC filter

To resolve these severe shortcomings and improving the reliability of the power system, this chapter proposes and analyses the improved Γ-Z-source inverter that enhances upon the conventional Γ-Z-source inverter to overcome the aforementioned drawbacks of existing topologies. Fig. 3.2 shows the basic structure of the improved Γ-Z-source inverter with clamping diode D_2.

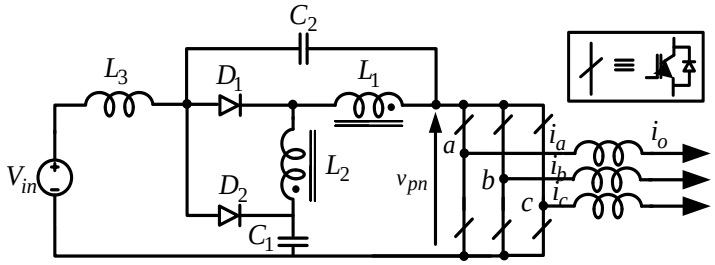


Fig. 3.2. Improved ΓZSI with clamping diode

This chapter shows the step by step derivation of improved ΓZSI with clamping diode from the conventional ZSI using a flow chart, and presents the detailed analysis of the proposed inverter. Then it discusses the benefits of the proposed inverter over existing transformer based ZSI topologies and shows its comparative evaluations through Matlab plots. Finally, experimental hardware of the proposed inverter is shown with validated results and efficiency plot.

3.2 Advantages of Improved ΓZSI with Clamping Diode

This section reports the main advantages of the proposed improved ΓZSI with clamping diode as compared to existing ZSI circuits as discussed in Sections 2.3 and 2.4. It also shows the derivation of improved ΓZSI with clamping diode from the original Z-

source inverter. Fig. 3.3 shows the flow diagram of improved ΓZSI with clamping diode derived from original ZSI.

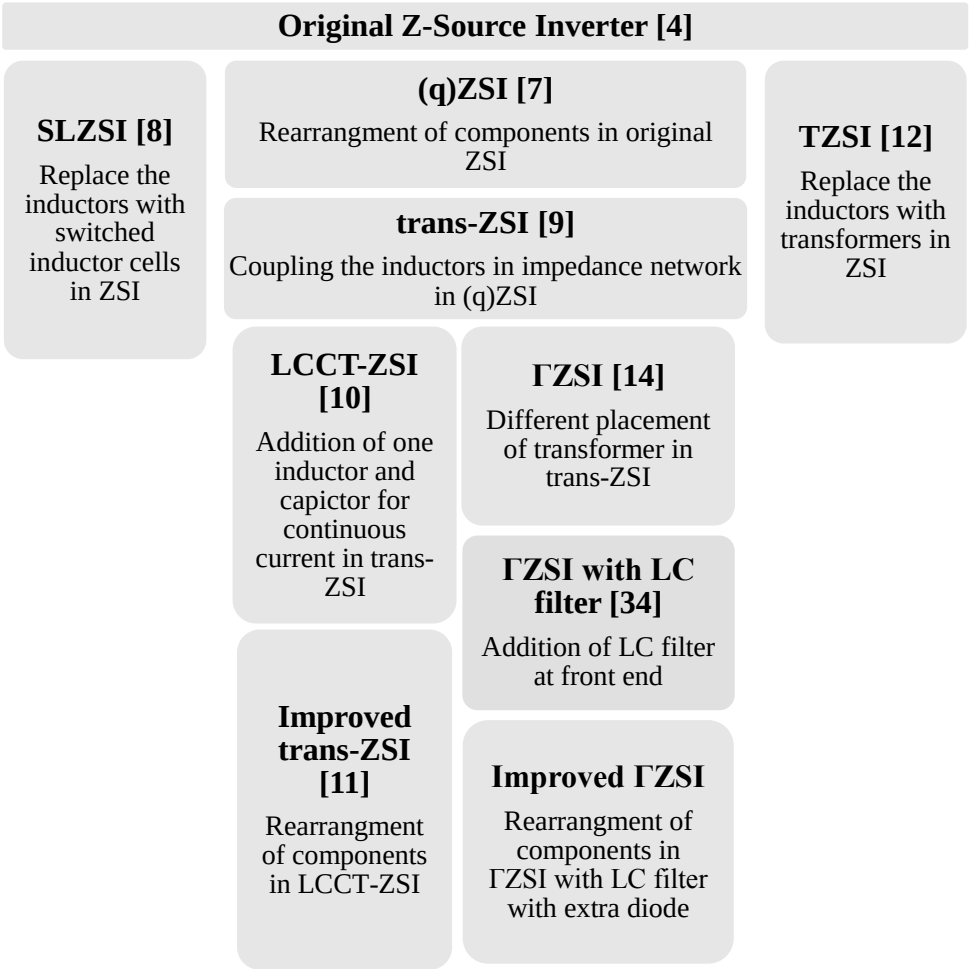


Fig. 3.3 Derivation of proposed improved ΓZSI with clamping diode

The main characteristics of the proposed ΓZSI with clamping diode can be summarized as follows and will be discussed in detail in the later section:

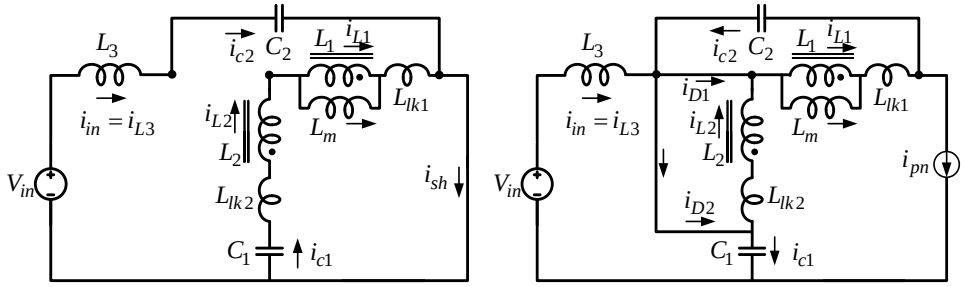
1) The input current is continuous and no additional filter is required.
2) It provides start-up inrush current suppression, unlike the trans-ZSI, tZSI and ΓZSI, because no current flows into the main circuit at start-up.
3) In other transformer based Z-source topologies, the energy stored in the leakage inductance of the transformer produces voltage spikes across the inverter bridge, while in the improved ΓZSI inverter, the clamping diode forms a new high frequency

loop comprising of C_2-D_2-C_1. As a result, the dc-link voltage is clamped to (V_{c1}+ V_{c2}), thus eliminating the voltage spikes across the inverter bridge.

4) The improved ΓZSI with clamping diode has higher voltage gain than the original ΓZSI and above discussed topologies such that with same input/output conditions and same transformer turns ratio, the improved ΓZSI uses a lower shoot through duty cycle and consequently a higher modulation index as compared to original ΓZSI, which results in lower component voltage stress and better output power quality.

3.3 Working Principle of the Improved ΓZSI with Clamping Diode

Like all the other existing impedance source inverters, the improved ΓZSI inverter with clamping diode have one extra shoot-through state besides the two traditional zero states and six active states. For analytical purposes, the operating states are simplified as shoot-through state (state 1) and non-shoot-through state (state 2). The equivalent circuits of the improved ΓZSI inverter during these operating states are shown in Fig. 3.4 (a) and (b).



(a) (b)

Fig. 3.4. Operating modes of the proposed inverter (a) State 1: Shoot-through mode (b) State 2: Non-shoot-through mode

State 1: In the shoot-through state, all the switches of the same legs are turned on and the circuit is equivalent to a short circuit. During this shoot-through state both the diodes are 'off' and the windings 1 and 2 are charged by the capacitor current C_1.

State 2: The non-shoot-through state consists of two zero states and six active states, in this mode both the diodes are 'on' and stored energy in the windings are released to the circuit and the load, thus the capacitors C_1 and C_2 are charged by it. During this state, the energy stored in the leakage inductances is absorbed by C_1 and C_2 through diode D_2 and it is, therefore, recycled without creating voltage spikes.

3.4 Boost Factor of Improved ΓZSI with Clamping Diode

The boost factor of the inverter is the ratio of dc-link voltage of the inverter bridge to the input dc voltage. The boost factor can be determined by analysing the shoot-through and non-shoot-through states and by applying the Kirchhoff's voltage law across the circuits in both states. Fig. 3.5 (a) and (b) shows the simplified equivalent circuits of the improved ΓZSI inverter with clamping diode during the shoot-through and non-shoot-through states.

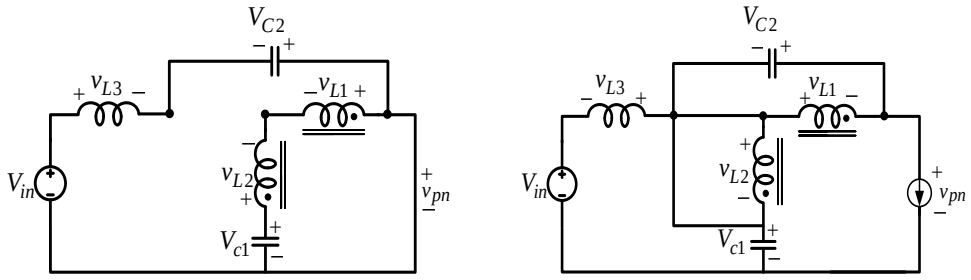


Fig. 3.5. Simplified circuits (a) Shoot-through state (b) Non-shoot-through state

By applying KVL to the circuit in Fig. 3.5(a) in shoot through state, we obtain:

$$\begin{cases} -V_{c1} + v_{L2_{sh}} - v_{L1_{sh}} = 0 \\ v_{L1_{sh}} = v_{L2_{sh}} - V_{c1} - - - -(\text{i}) \\ n = {}^{v_{L1}}/_{v_{L2}} \\ -V_{in} + v_{L3_{sh}} - V_{c2} = 0 \\ v_{L3_{sh}} = V_{in} + V_{c2} - - - -(\text{ii}) \end{cases} \tag{3.1}$$

Similarly, by applying KVL to the circuit in fig. 3.5(b), we get:

$$\begin{cases} -V_{c1} - v_{L2_{non}} + v_{L1_{non}} + v_{pn} = 0 \\ -V_{in} - v_{L3_{non}} + v_{L2_{non}} + V_{c1} = 0 \\ v_{L3_{non}} = -V_{in} + v_{L2_{non}} + V_{c1} \\ v_{L3\_sh} = V_{in} + V_{c2} V_{c1} - - - -(\text{iii}) \\ v_{L1_{non}} = -V_{c2} \\ n v_{L2_{non}} = -V_{c2} \end{cases} \tag{3.2}$$

By applying the flux balance condition across L_1, and L_2, we have:

$$\begin{cases} v_{L2_{sh}} D = v_{L2_{non}} (1 - D) \\ v_{L2_{sh}} = -V_{c2} (1 - D)/_{nD} \\ v_{L1_{sh}} D = v_{L1_{non}} (1 - D) \\ -V_{in} + v_{L3_{sh}} - V_{c2} \\ v_{L1_{sh}} = -V_{c2} (1 - D)/_{D} - - - -(\text{iv}) \end{cases} \tag{3.3}$$

By substituting (iv) in (i), we have:

$$\begin{cases} v_{L1_{sh}} = v_{L2_{sh}} - V_{c1} \\ -V_{c2} (1 - D)/_{D} = -V_{c2} (1 - D)/_{nD} - V_{c1} \\ V_{c1} = V_{c2} (n - 1)(1 - D)/_{nD} - - - -(\text{v}) \end{cases} \tag{3.4}$$

By applying voltage second condition across L_3, yields:

$$\begin{cases} (V_{in} + V_{c2}) D = (v_{L2_{non}} - V_{in} + V_{c1})(1 - D) \\ V_{c2} = V_{in} (nD)/_{n(1 - 2D) - 1 + D} - - - -(\text{vi}) \end{cases} \tag{3.5}$$

By substituting (vi) in (v), we have:

$$V_{c1} = \frac{V_{in}(1 - D)(n - 1)}{n(1 - 2D) - 1 + D} \tag{3.6}$$

where, n is the turns ratio of the transformer, V_{in} is the input voltage and D is the shoot through duty of the improved ΓZSI with clamping diode. By (ii) and (iii), we can find the dc-link voltage, v_{pn} of the improved ΓZSI with clamping diode, which is expressed as:

$$\begin{cases} (V_{in} + V_{c2}) D = (v_{pn} - V_{in} - V_{c2})(1 - D) \\ v_{pn} = \frac{V_{in}(n - 1)}{n(1 - 2D) - 1 + D} \end{cases} \tag{3.7}$$

Therefore, the boost factor *B* of the improved ΓZSI with clamping diode is given by:

$$B = \frac{(n-1)}{n(1-2D)-1+D} \tag{3.8}$$

3.5 Comparisons with the Previous Works

To validate the benefits of the improved Γ-Z-source inverter with clamping diode, comparisons with the previously proposed topologies have been made in this section. The plot of boost factor *B* vs duty cycle *D* for the improved ΓZSI, TZSI, ΓZSI, trans-ZSI and improved trans-ZSI has been shown in Fig. 3.6. The turns ratio of the transformers has been set to 1.24 for each of inverter topologies for the sake of comparisons. From the plot, it can be inferred that the boosting capacity of the improved ΓZSI with clamping diode is significantly greater than that of other topologies with same number of turns.

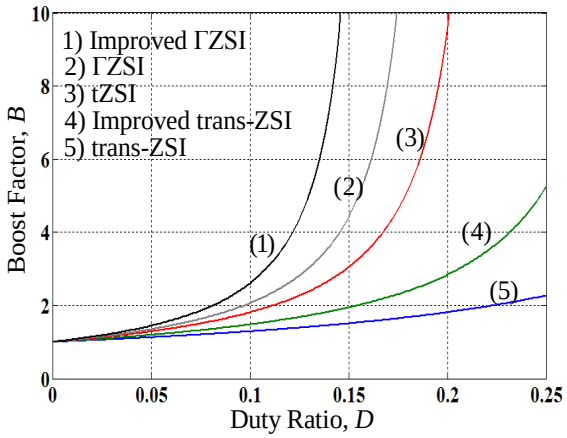


Fig. 3.6. Plot of boost factor versus duty cycle with n=1.24

All of the pulse width modulation schemes (PWM) developed for the impedance source inverters which are simple boost control, maximum boost control, and constant boost control [24] are applicable to the improved Γ-Z-source inverter with clamping diode as well. The simple boost control scheme has been applied in this study. The relation between the modulation index and the duty ratio in simple boost scheme is expressed as in (1.2)

$$M = (1-D) \tag{1.2}$$

The output phase peak voltage v_{ph} of the ZSIs is defined in (2.2) as

$$\widehat{v_{ph}} = MB\,{}^{V_{in}}/_{2} \tag{2.2}$$

Therefore, from (1.2) and (2.2), the voltage gain G can be expressed in terms of modulation index as

$$G(MB) = \frac{\widehat{v_{ph}}}{V_{in}/2} = \frac{M(n-1)}{M(2n-1)-n} \tag{3.9}$$

Fig. 3.7 shows the voltage gain versus modulation index graph for the improved ΓZSI, tZSI, ΓZSI, trans-ZSI and improved trans-ZSI. From Fig. 3.7, it can be observed that with the decrement in modulation index the voltage gain rises. Thus for the same voltage gain compared with other impedance source topologies the improved ΓZSI utilizes higher modulation index and consequently a lower shoot-through duty ratio, which results in lower stress across the inverter bridge, better output quality and overall better spectral performance.

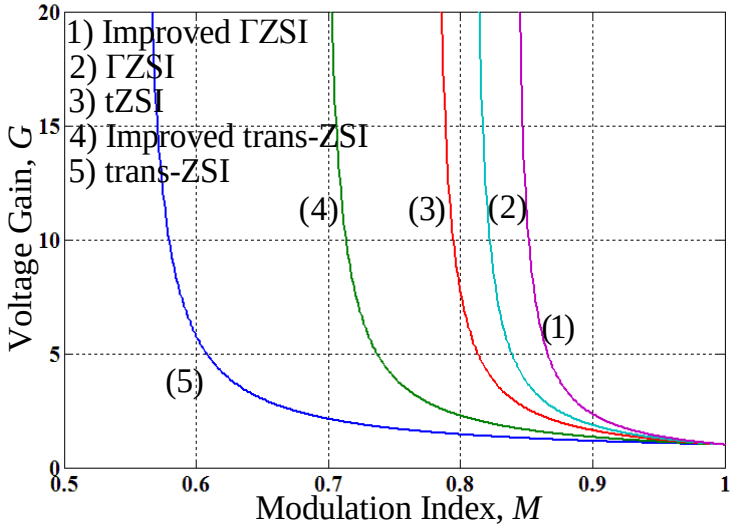


Fig. 3.7. Voltage gain against modulation index plot with n=1.24.

Another main concern associated with the impedance source inverters is the voltage stress across the switching devices. The voltage stress across the inverter bridge is same as the dc-link voltage for every impedance source inverter which is expressed as:

$$V_{sw} = v_{pn} = BV_{in} \tag{3.10}$$

By using the relation in (3.10) and (3.8), the voltage stress of the improved ΓZSI with clamping diode in terms of voltage gain can be obtained as

$$\frac{V_{sw}}{V_{in}} = \frac{G(2n-1)+1-n}{n} \tag{3.11}$$

The plot of switch voltage stress versus the voltage gain is shown in Fig 3.8. As discussed earlier, for obtaining the same voltage gain the improved Γ-Z-source inverter with clamping diode utilizes a higher modulation index with lower shoot through duty cycle resulting in lower voltage stresses across the switching devices. Thus, it is clearly shown in the Fig. 3.8 that for the same gain, the voltage stress of the improved ΓZSI is the lowest among the other mentioned impedance source topologies. This makes improved Γ-Z-source inverter with clamping diode a good practical candidate for the industrial applications that requires higher boost abilities with cost efficient demands.

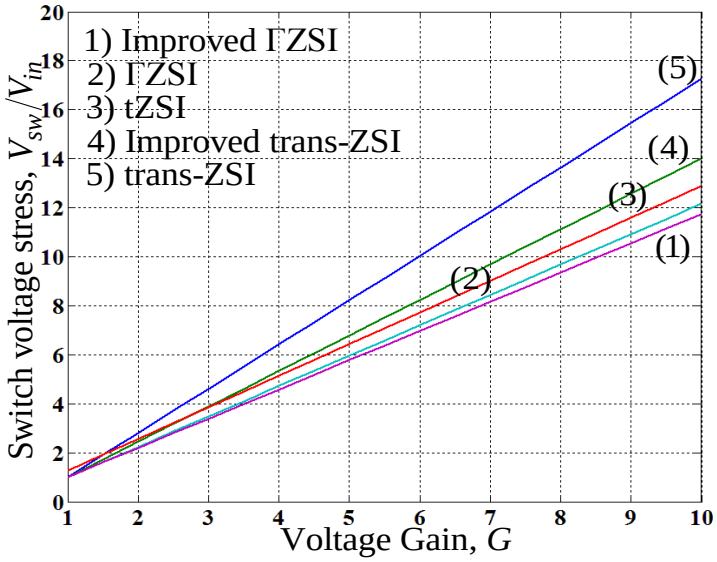


Fig. 3.8. Plot of voltage stress versus voltage gain with n=1.24.

Table 3.1 compares the governing equations for improved ΓZSI with clamping diode, ΓZSI, TZSI, trans-ZSI and improved trans-ZSI. It summarizes all the voltage stresses under the conditions of same input voltage and same shoot-through duty cycle. In Table 3.1, S_D represents the shoot-through switching function, which is defined as '1' when the

inverters are in shoot-through states and as '0' when the inverters are in non-shoot-through states. In Table 3.1, v_{pn} is dc-link voltage of the inverter, V_c is the voltage across the capacitor, V_D is the voltage of the input diode, *D* is the shoot-through duty cycle and *n* is the turns ratio of the transformer.

TABLE 3.1

Summary of Voltage Stresses

	Trans-ZSI Fig. 2.16	Improved trans-ZSI Fig. 2.18	TZSI Fig. 2.19	ΓZSI Fig. 2.20	Improved ΓZSI with clamping diode Fig. 2.1
v_{pn} V_{sw}	$\overline{S_D}.\left[\frac{V_{in}}{1-(1+n)D}\right]$	$\overline{S_D}.\left[\frac{V_{in}}{1-(2+n)D}\right]$	$\overline{S_D}.\left[\frac{V_{in}}{1-(2+n_1+n_2)D}\right]$	$\overline{S_D}.\left[\frac{V_{in}}{1-\left(1+\frac{1}{n-1}\right)D}\right]$	$\overline{S_D}.\left[\frac{(n-1)V_{in}}{n(1-2D)-1+D}\right]$
V_c	$V_{c1}=\frac{(1-D)V_{in}}{1-(1+n)D}$ $V_{c2}=NA$	$V_{c1}=\frac{(1-D)V_{in}}{1-(2+n)D}$ $V_{c2}=\frac{(1+n)V_{in}}{1-(2+n)D}$	$V_c=\frac{(1+n_1+n_2)DV_{in}}{1-(2+n_1+n_2)D}$ $V_c=V_{c1}=V_{c2}$	$V_{c1}=\frac{(1-D)V_{in}}{1-\left(1+\frac{1}{n-1}\right)D}$ $V_{c2}=NA$	$V_{c1}=\frac{(n-1)(1-D)V_{in}}{(n(1-2D)-1+D}$ $V_{c2}=\frac{(nD)V_{in}}{(n(1-2D)-1+D}$
V_D	$S_D.\left[\frac{nV_{in}}{1-(1+n)D}\right]$	$S_D.\left[\frac{(1-n)V_{in}}{1-(2+n)D}\right]$	$S_D.\left[\frac{(1+n_1+n_2)DV_{in}}{1-(2+n_1+n_2)D}\right]$	$S_D.\left[\frac{V_{in}}{n-1-nD}\right]$	$V_{D1}=S_D.\left[\frac{nV_{in}}{n(1-2D)-1+D}\right]$ $V_{D2}=S_D.\left[\frac{(n-1+D)V_{in}}{n(1-2D)-1+D}\right]$
G MB	$\frac{M}{1-(1-M)(1+n)}$	$\frac{M}{1-(1-M)(2+n)}$	$\frac{M}{1-(1-M)(2+n_1+n_2)}$	$\frac{M}{1-\left(1+\frac{1}{n-1}\right)(1-M)}$	$\frac{(n-1)M}{n(2M-1)-M}$

3.6 Simulation Results

Saber simulations are performed to validate the operation of the improved ΓZSI with clamping diode. Simulations are performed for the improved ΓZSI with clamping diode and the conventional ΓZSI to validate the advantages of the former inverter. Simple boost modulation scheme is applied. Control scheme in Saber simulations are performed using comparators and logic gate blocks as shown in Fig. 3.9 in which the reference waveforms are compared with carrier waveforms to generate the gating signals. The carrier waveform is compared with straight line envelops to generate shoot through states as explained in section 2.2.1.

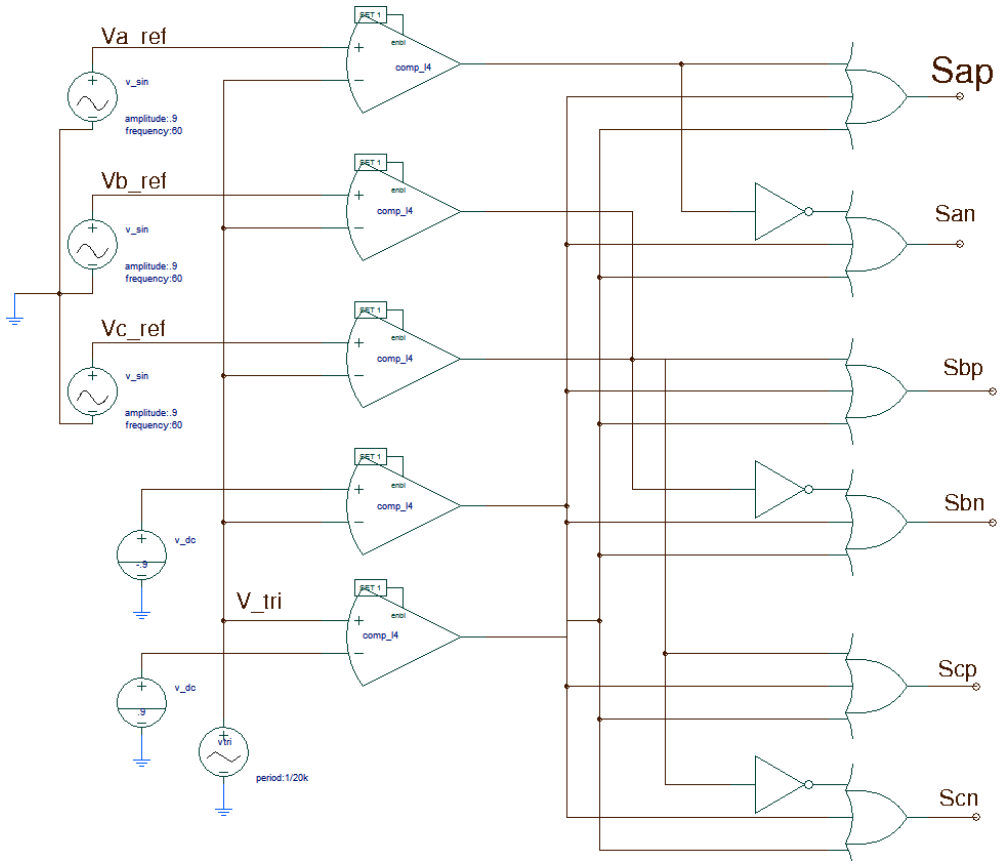
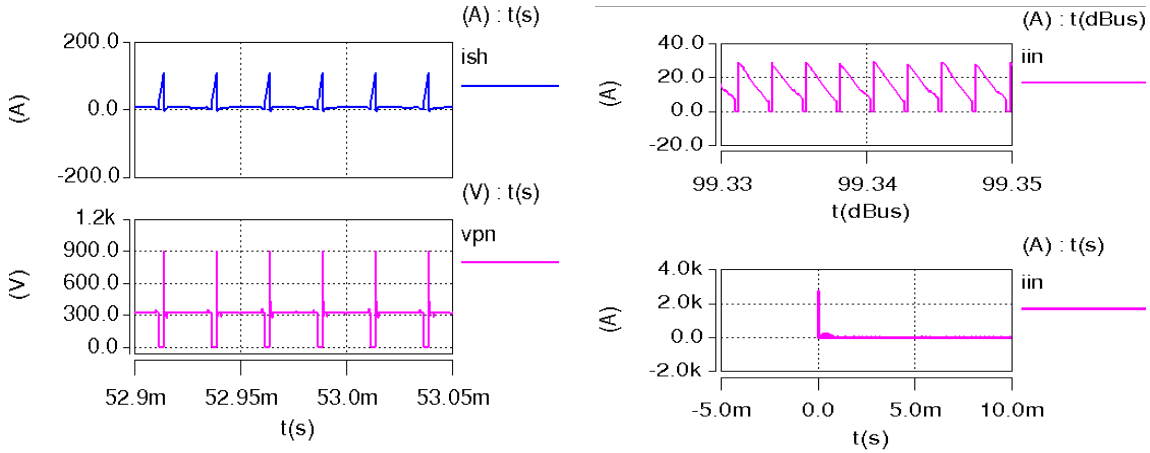


Fig. 3.9. Block diagram of simple boost control in saber simulation

Below are the detailed electrical specifications for testing of the proposed inverter:

- Input voltage: $V_{in} = 152\ V$
- Output voltage: 220 V_{rms}
- Coupled Inductor: L_1= 200 µH, L_2= 130 µH
- Inductor: L_3= 500 µH
- Z-source Capacitors: $C_1 = C_2 = 100$ µF
- Modulation index: M = 0.9
- Switching frequency: $f_{sw} = 20$ kHz
- Output AC filter inductors: L_o= 850 µH
- Output AC filter Capacitors: C_o= 100 µF
- Resistive load: R = 20Ω/phase

For the sake of comparisons and explaining the issues faced with conventional ΓZSI, simulations are done for conventional ΓZSI and improved ΓZSI with clamping diode. Fig. 3.10 shows the waveforms of the conventional ΓZSI with STDC 0.1 and modulation index 0.9, the dc-link voltage is boosted to 314 V. Fig. 3.10(a) shows the waveforms of dc link voltage with $L_{lkp} = L_{lks} = 300\ nH$ and shoot-through current. Fig. 3.10 (b) shows the large inrush current at startup and the expanded waveforms of discontinuous input current.



(a) (b)

Fig. 3.10. Simulation results of the conventional Γ-ZSI (a) shoot-through current and dc-link voltage (b) input current

Fig. 3.11 shows the simulation power stage prototype of the proposed improved ΓZSI with testing points and Fig. 3.12 shows the simulation results of improved ΓZSI with clamping diode. Fig. 3.12(a) shows the waveforms of the improved ΓZSI inverter dc-link voltage, and shoot through current. From the results, it can be realized that the voltage spikes caused by the leakage inductances are minimized with the addition of the extra diode. Additionally, with the same electrical parameters the dc-link voltage of the improved ΓZSI is boosted to 400 V which is higher than the original ΓZSI. Fig. 3.12 (b) shows the suppressed inrush current and expanded input current waveform. As it can be seen from the waveform, the input current is continuous, thus no additional filter is required at the front end. Fig. 3.12 (c) shows the capacitor voltage waveforms $V_{c1} \approx 356\ V,\ V_{c2} \approx 204\ V$ and comply with the derived theoretical equations (3.5) and (3.6).

Fig. 3.12 (d) shows the output filter inductor current waveforms. Fig. 3.12(e) shows the waveforms of line-to- line output voltage, output current and input voltage.

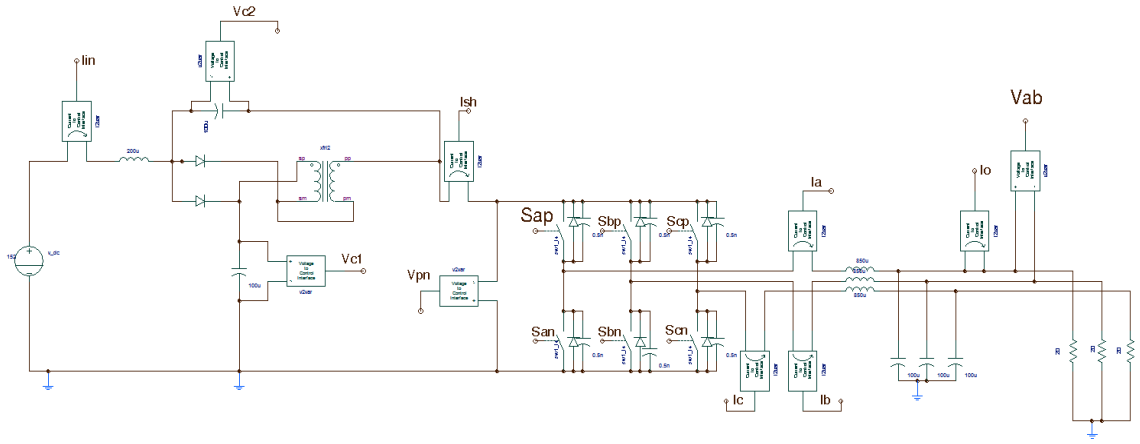
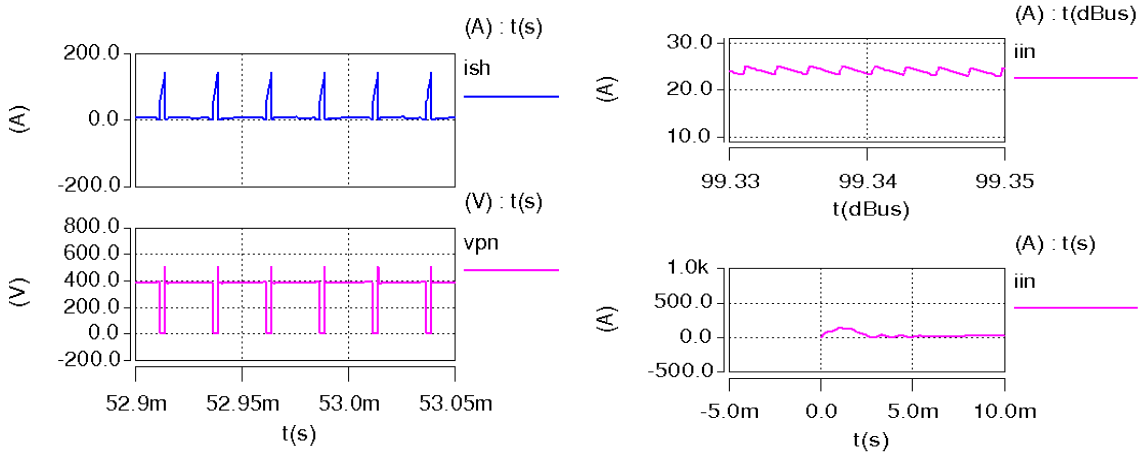
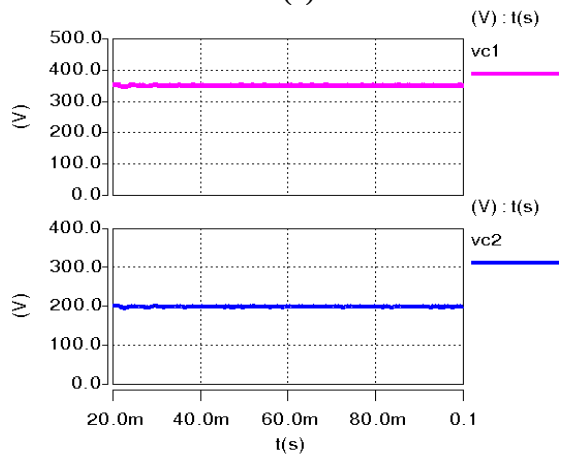


Fig. 3.11. Block diagram of proposed inverter in saber simulation

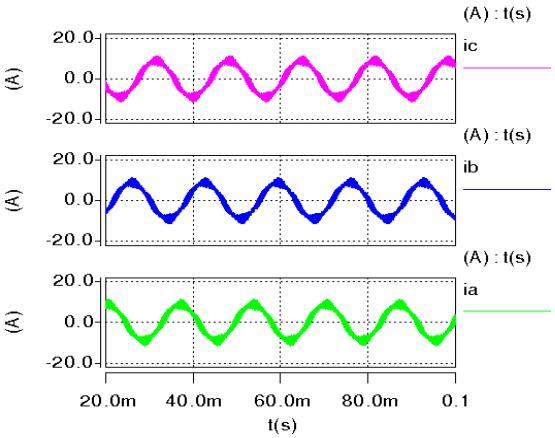


(a)

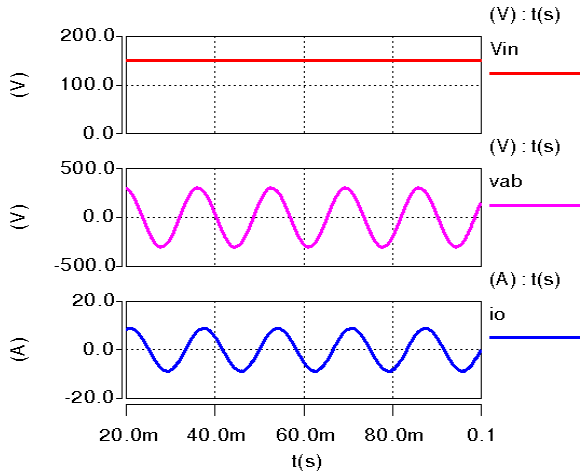
(b)



(c)



(d)



(e)

Fig. 3.12. Simulation results of improved Γ-ZSI with clamping diode. (a) shoot-through current and dc-link voltage (b) input currents (c) capacitor voltages (d) output filter inductor currents (e) input voltage, line-line output voltage and output current

3.7 Prototyped System Results

A hardware prototype of improved ΓZSI with clamping diode was fabricated and experiments are performed to validate its advantages.

3.7.1 Platform Selection

In the literature, most of the work that has been done in the area of power electronics utilize two most common platforms for the implementation of the circuit designs [4-30].

1. dSPACE Ace kit [1]
2. DSP kits based on TMS320f28335[2]

In the thesis, DSP kit based on TMS320f28335 is utilized. The merits of the specified DSP kit were already tested in the power electronics laboratory of UCT and have been used in numerous projects. dSPACE kit was also given consideration for the development of the proposed system but DSP kit was preferred due to strong expertise of myself and other lab members. Simple boost control scheme is applied for the control of inverter

[1] https://www.dspace.com/en/pub/home/products/hw/singbord/ds1104.cfm
[2] http://www.ti.com/tool/TMDSDOCK28335

bridge switches due to its simple coding protocols and it can give a better understanding of the proposed inverter system due to its less complex algorithms.

3.7.2 Parameter Design of Proposed Inverter components

The design parameters of the components in the proposed improved ΓZSI are given in this section. The parameters are determined based on maximum allowable voltage and current stresses.

During shoot-through state *DT*, the voltage across inductors L_1, L_2 and L_m of transformer are $V_{c2} + V_{in}$, V_{c1}, and V_{cp} respectively. Therefore, we get:

$$\begin{cases} L_m = \dfrac{V_{c1}}{\Delta i_{Lm}} DT \\ L_3 = \dfrac{V_{c2} + V_{in}}{\Delta i_{L3}} DT \end{cases} \tag{3.12}$$

The values of V_{c1} and V_{c2} are given by (3.5) and (3.6). By assuming the maximum allowable current ripple for the inductors L_m and L_3 are $\Delta i_{Lm} \leq x\% I_{in}$, $\Delta i_{L3} \leq x\% I_{in}$, and $\Delta i_{Lm} \leq x\% I_o$ respectively, and further solving (3.12), we get:

$$\begin{cases} L_m = \dfrac{V_{in}^2 (1-D)(n-1)}{(n(1-2D)-1+D) x\% P_o} DT \\ L_3 = \dfrac{V_{in}^2 (n(1-D)-1+D)}{(n(1-2D)-1+D) x\% P_o} DT \end{cases} \tag{3.13}$$

where I_{in}, V_{in} are the average values of the input current and voltage, respectively, while P_o is the rms value of the output power, respectively.

During shoot-through state *DT*, the current flowing through C_1 and C_2 are I_{Lm} and I_{L3}, respectively, where I_{Lm} and I_{L3} are same as I_{in}. Therefore, we get

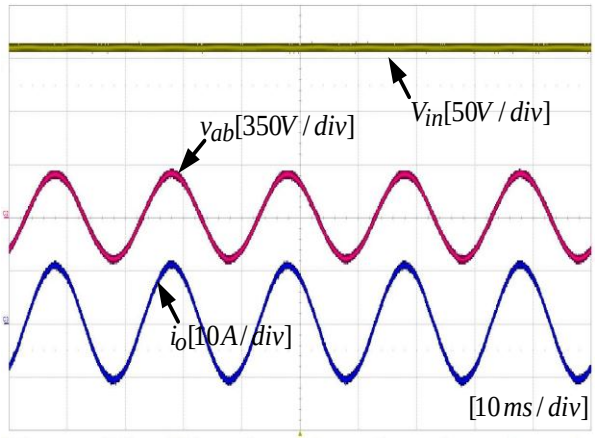
$$\begin{cases} C_1 = \dfrac{I_{Lm}}{\Delta v_{c1}} DT \\ C_2 = \dfrac{I_{L3}}{\Delta v_{c2}} DT \end{cases} \tag{3.14}$$

By assuming the maximum allowable voltage ripple for the capacitors C_1 and C_2 are $\Delta v_{c1} \leq y\%V_{c1}$, and $\Delta v_{c2} \leq y\%V_{c2}$ respectively, and by solving (3.14), the value of capacitors can be given as:

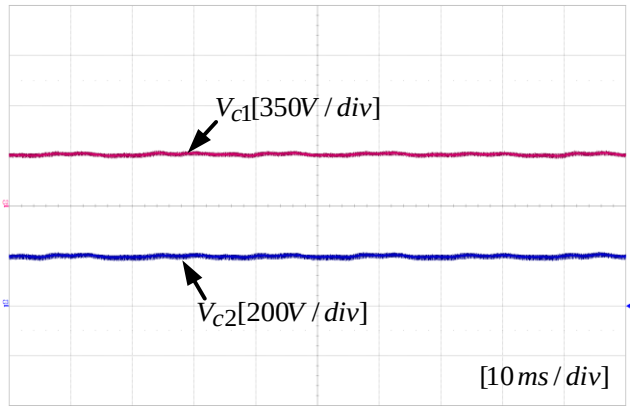
$$\begin{cases} C_1 = \dfrac{P_o(n(1-2D)-1+D)}{(1-D)(n-1)\%yV_{in}^2}DT \\ C_2 = \dfrac{P_o(n(1-2D)-1+D)}{\%yV_{in}^2 nD}DT \end{cases} \tag{3.15}$$

3.7.3 Experimental Results

Simple boost control signals are generated using a DSP-kit based on TMS320f28335. Details of the assembly of hardware prototype with coding protocols to this thesis are given in Appendix A and B. All the parameters in experiments are kept same as in simulations. Fig. 3.13(a) shows the experimental waveforms of input voltage V_{in}, line-to-line output voltage v_{ab}, and output current i_o. Fig. 3.13(b) shows the waveforms across the Z-source network capacitors C_1 and C_2. Fig. 3.14(a) and (b) shows the waveforms of input current and dc-link voltage v_{pn} of the improved ΓZSI, i.e. with D_2 in Fig. 3.14(a) and without D_2 in Fig. 3.14(b). It clearly shows the added benefit of clamping diode which eliminates the voltage spikes caused by leakage inductances of the transformer. Fig. 3.15 shows the experimental waveforms of output inductor currents. Fig. 3.16 shows the picture of improved ΓZSI with clamping diode experimental setup.

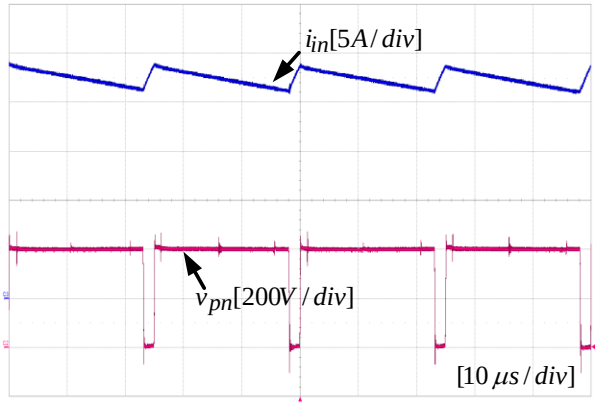


(a)

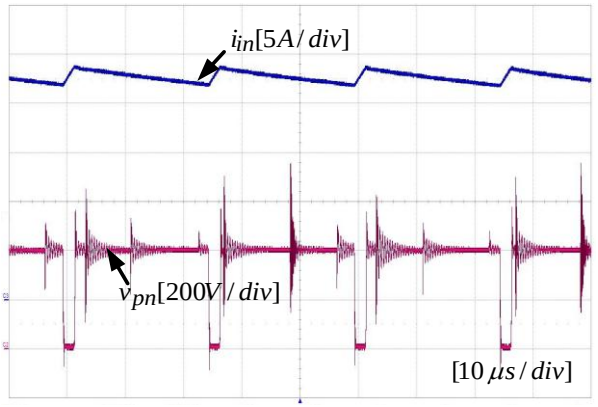


(b)

Fig. 3.13. Experimental waveforms of improved ΓZSI with clamping diode. (a) Input voltage, line-to-line output voltage, and output current. (b) Capacitor voltages



(a)



(b)

Fig. 3.14. Experimental waveforms of dc-link voltage and input current. (a) with clamping diode D_2. (b) without clamping diode D_2.

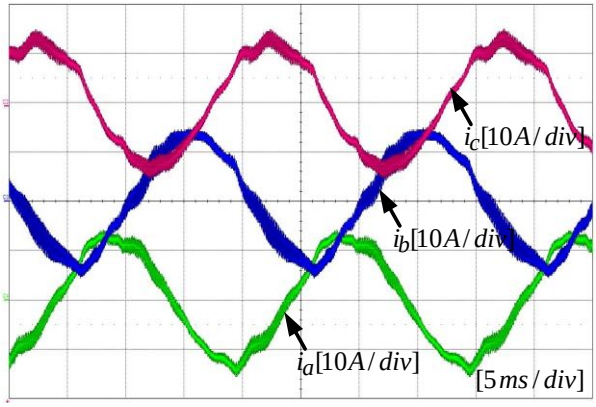


Fig. 3.15. Experimental waveforms of output inductor currents

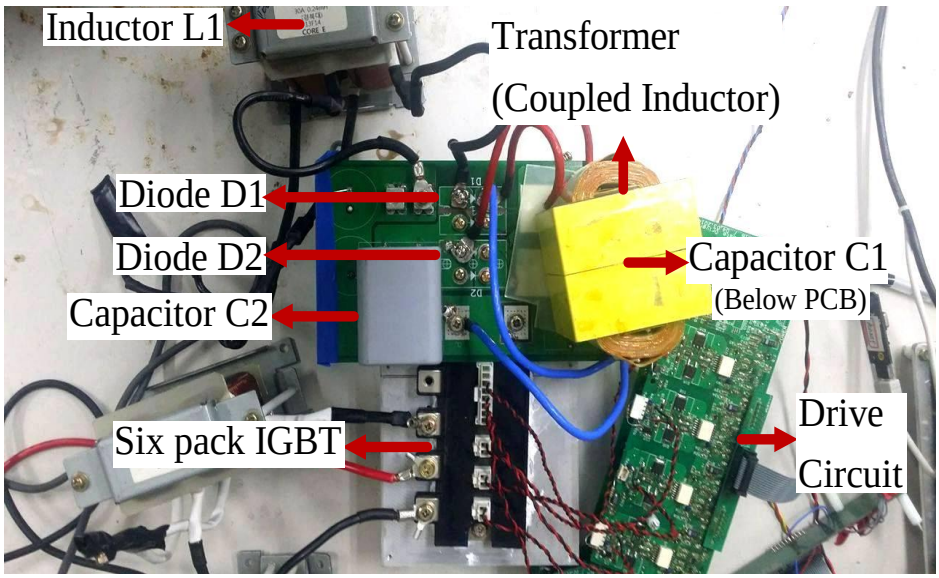


Fig. 3.16. Hardware prototype of improved ΓZSI with clamping diode

3.8 Efficiency Calculation

In this section, the efficiencies of improved ΓZSI-clamped, conventional ΓZSI, and ΓZSI with LC filter are compared. The method used by [11, 12] for efficiency calculation is adopted here and PSIM simulations are performed considering some loss related parameters which are listed in table 3.2.

TABLE 3.2

Efficiency Parameters

IGBT (six pack)	CM100TU-12H
Diode	STTH60L06C
Core	EE 110/114/36
Capacitor ESR	2.5 mΩ (100 μF)
Copper wire resistivity (ρ)	1.724 μ Ω-cm

The main power losses within an inverter are semiconductor switching and conduction losses, inductor and transformer core losses and its winding resistance and losses in the esr of the capacitors. Among them, the semiconductor losses are the most prominent and biggest. The semiconductor losses are calculated using a thermal module in PSIM simulations. Moreover, as it can be seen from the experiment and simulation results, the improved ΓZSI with clamping diode clearly reduces the voltage overshoots as the leakage inductance energy is recycled through the additional diode without creating voltage spikes, unlike the other inverters in which the leakage inductance energy creates high voltage spikes across the switching devices. Thus, it can use 600-V IGBT module having almost four times smaller switching and conduction losses [56] compared to 1200-V IGBT module which has to be used for conventional ΓZSI, and ΓZSI with LC filter. The power losses in the magnetic components consists of its core loss and copper loss and the equations for calculating the power loss are given in [51]. The core loss is calculated by:

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c l_m \tag{3.15}$$

The inductor and transformer copper losses can be calculated by:

$$P_{L\_cu} = \frac{\rho N^2 MLT I^2}{K_u W_A} \tag{3.16}$$

$$P_{T\_cu} = \frac{(N_1 I_1 + N_2 I_2)^2 \rho MLT}{K_u W_A} \tag{3.17}$$

where, K_{fe} is the proportionality constant, ΔB is the flux density variation, β is determined by the core manufacturers sheet, A_c is the cross-sectional area, l_m is the mean core length, ρ is the resistivity, N is the winding turns, I is the rms winding current, (MLT) is the winding mean length per turn, K_u is the winding fill factor, and W_A is the core window area. Additionally, the improved ΓZSI gain is higher than conventional ΓZSI, thus it requires small inductance as compared to conventional ΓZSI which results in lower winding resistance and losses. Under these conditions, the efficiencies of the three inverters are plotted and shown in Fig. 3.17.

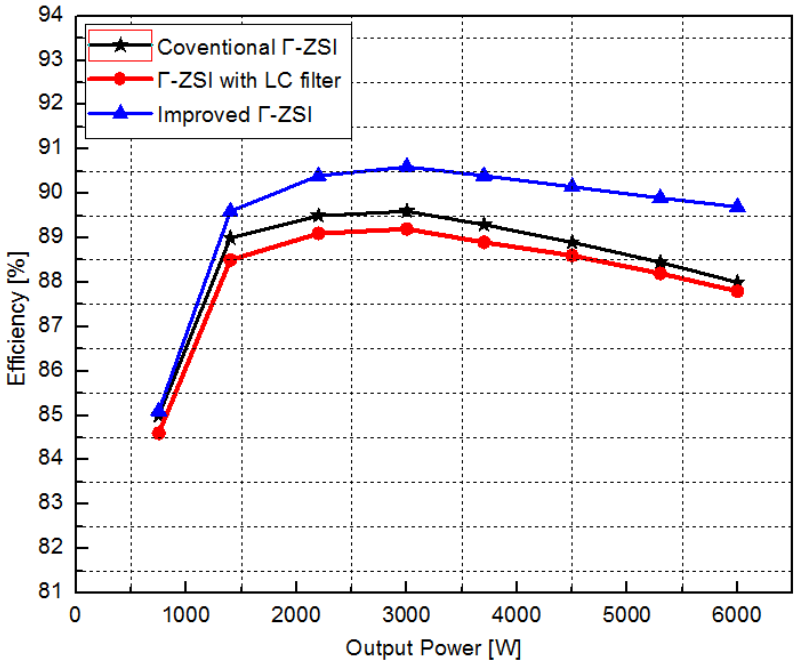


Fig. 3.17. Efficiency comparison.

From the plot, it can be seen that despite having more components than conventional ΓZSI, the improved ΓZSI has higher efficiency because of much smaller switching losses and winding losses due to the utilization of higher modulation index (small shoot-through interval) and clamping diode.

3.9 Conclusions

In this chapter, an improved ΓZSI with clamping diode is proposed and explained in detail. Compared to the conventional ΓZSI and other ZSI topologies, improved inverter inherits the main advantages which are:

1. Continuous input current and improved input profile.
2. Minimization of the voltage spikes caused by the leakage inductance of the transformer.
3. Higher voltage gain is obtained.
4. For the same input and output voltage conditions, higher modulation index with lower shoot-through duty can be used thus resulting in lower component voltage stresses, better output power quality and increased efficiency.

The improved inverter is best suited for applications that require a single step high voltage conversion with low input dc voltage such as fuel cells and PV cells. A 7 kW hardware prototype is constructed and experiments are performed to validate its working operation and benefits. Next chapter of the thesis project will discuss the implementation of high frequency transformer to the improved ΓZSI-clamped and the advantages of employing high frequency isolation. Extension of the HFT technique to other transformer based ZSIs will also be discussed in detail.

4. Chapter 4
Single-Phase Transformer based HF-Isolated Impedance Source Inverters with Voltage Clamping Techniques

4.1 Introduction

This chapter reports on the design and implementation of a new class of ZSIs. It employs high frequency electrical isolation between the inverter bridge switches and the load along with voltage clamping across the DC-link voltage. One of the major concerns among ZSIs is that the existing impedance source circuits do not have electrical isolation. Therefore, when these ZSIs are used in photo-voltaic modules as grid inverters, a DC current is injected in the grid which may cause saturation of the distribution transformer [46, 47] as well as poor power quality, higher loss, and overheating of the power system. According to IEEE Standard 1547-2003, the level of DC component injected into grid should be less than 0.5% of the rated output current [48-50]. In order to avoid this injection of DC current into the grid, and to fulfil the safety standards, the conventional approach is to incorporate a line frequency transformer between the inverter and the grid. However, this low frequency transformer is bulky, heavy, expensive, and decreases the efficiency and power density of the system. Many other methods have also been developed to minimize the injection of DC currents into the grid within transformer-less inverters (e.g. existing ZSIs). Most of these methods for blocking DC currents include a DC capacitor [50], voltage and current detection based techniques. However, they either use bulky and

expensive capacitors, or voltage and current sensing circuitry, yet may not guarantee the safety standards are met.

In order to resolve this, this chapter focuses on developing a new class of impedance source inverters topology based on high frequency link. High frequency isolation has many advantages in terms of immunity and reliability [57-60]; when applied with impedance source inverters this makes ZSIs a preferable choice for industrial applications. In PV systems, the addition of the high frequency transformer provides safety by avoiding the injection of DC circulating current into the grid, without the need of an external bulky line frequency transformer. The gain of the proposed inverter design can be accurately selected by choosing the turns ratio of the HFT or by adjusting the shoot-through duty cycle (STDC) to the inverter. This allows for greater freedom especially when utilizing a higher modulation index, with the STDC allowing dynamic gain adjusts to be done speedily during operation of the inverter. Additionally, a DC-rail voltage clamping technique for the proposed class of isolated ZSIs is also discussed. This technique provides benefits not only in improving the output voltage quality, but also in reducing voltage stress of the active and passive components by minimizing the voltage spikes across the switching devices. In this chapter, several high frequency isolated ZSIs are presented, and an example isolated improved ΓZSI design is shown and discussed in detail. Simulations are provided for the proposed class of isolated inverters to verify their working. Further experimental investigation has been done for which results for the isolated improved ΓZSI are reported. These empirical results have largely confirmed the expected benefits that were determined through simulation and accurate model-based testing.

4.2 Proposed Isolated Impedance Source Inverter

The general structure of the proposed isolated high frequency impedance source inverter is shown in Fig. 4.1. The proposed inverter maintains all the features of existing non-isolated ZSIs, which can be realized as having a single stage buck/boost power conversion capability with high reliability owing to their immunity from short circuit and open circuit problems. The proposed structure (Fig. 4.1) offers high frequency isolation

provided by the HF transformer. The high frequency isolation has advantages in terms of protection and durability [38]. Moreover, it avoids the injection of DC circulating current into the grid. Therefore, it provides electrical isolation and safety without the utilization of a bulky line frequency transformer. The small DC-blocking capacitor added in series with the high frequency transformer avoids saturation of the transformer core. Additionally, the gain of the proposed isolated impedance source inverter can also be regulated by tuning the turns ratio of the transformer. Thus, it provides added flexibility in choosing the shoot-through duty cycle and modulation index of the inverter. Even at maximum value of modulation index, this design provides step up and step down functions, obtained only by adjusting the turns ratio resulting in better output quality. Furthermore, by adding one additional diode, a new high frequency loop, consisting of impedance network capacitors C_1, C_2 and extra diode D_c, is formed. Thus, it bypasses the leakage inductance loop thereby minimizing the voltage spikes across the switches. Therefore, it reduces the overall cost of the system by reducing the switch power ratings.

The proposed isolated improved ΓZSI with additional diode is considered in detail and Fig. 4.2 shows its basic structure. From Fig. 4.2 it can be clearly seen that the proposed inverter retains the original impedance network configuration of their non-isolated counter parts on the primary side with extra diode. Additionally, it contains one high frequency transformer and a small DC-blocking capacitor C_p on the primary side. While on secondary side, the level shift capacitor C_s and bidirectional switch pair S_5, S_6 are used to restore the DC component of the voltage.

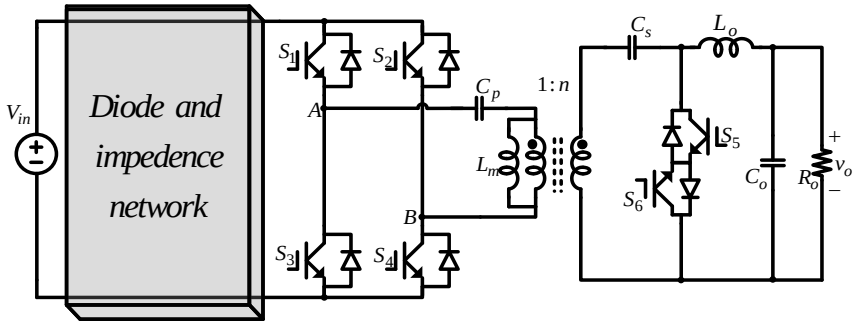


Fig. 4.1. Proposed isolated impedance source structure

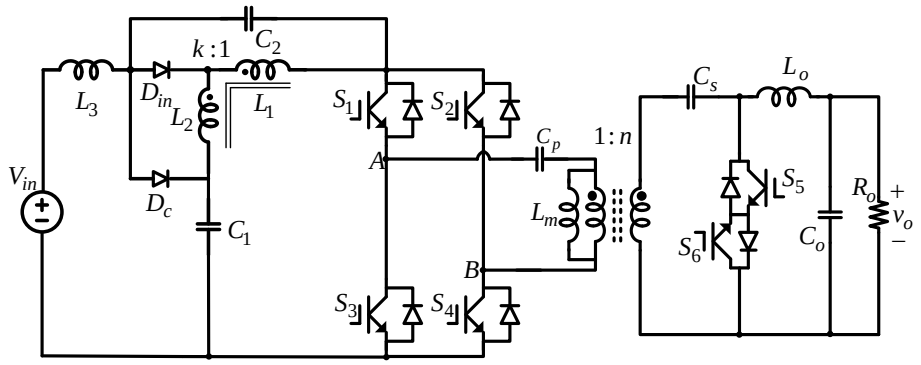
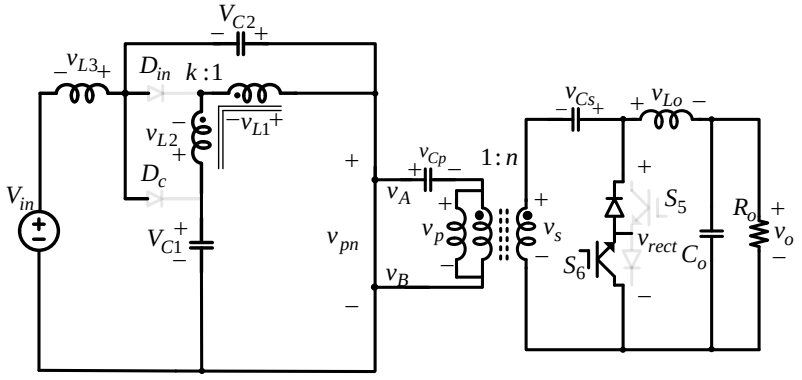


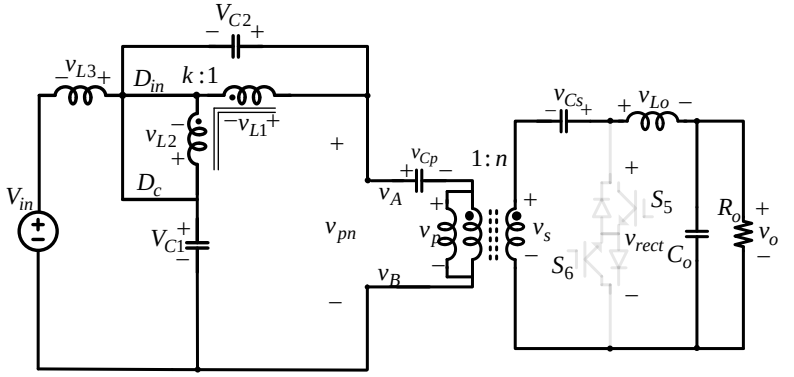
Fig. 4.2. Proposed isolated improved ΓZSI with extra diode.

4.2.1 Working Principle of the Improved ΓZSI with Extra Diode and its Circuit Analysis

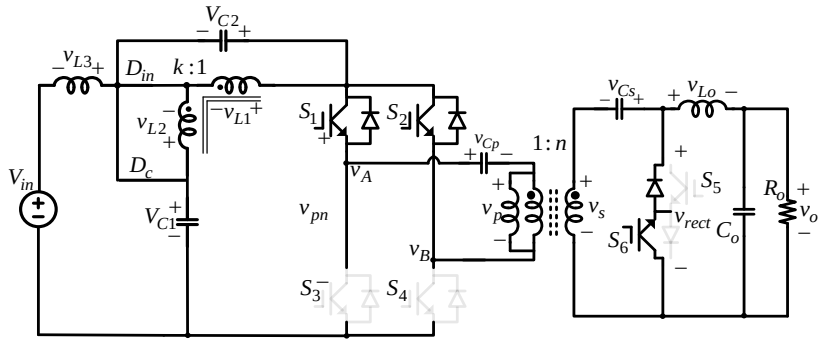
The operation of the proposed isolated improved ΓZSI (Fig. 4.2) is similar to the existing non-isolated ZSIs, having one shoot-through state, two zero states, and two active states as shown in Fig. 4.3.



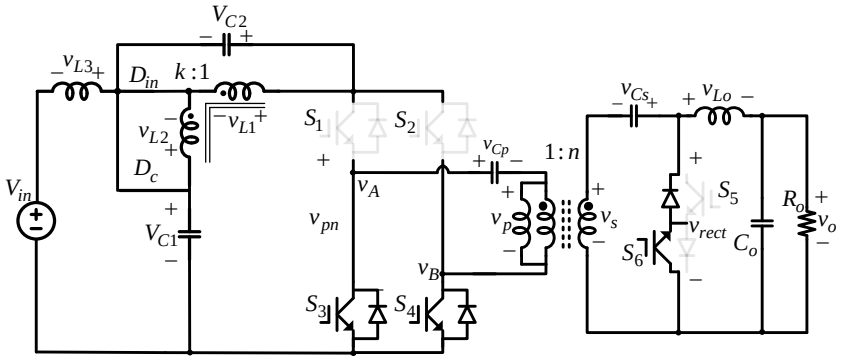
(a)



(b)



(c)



(d)

Fig. 4.3. Equivalent circuits of the proposed isolated ΓZSI with additional diode, (a) Shoot-through state, (b) Active state, (c) and, (d) Zero states

During the shoot-through interval, the inverter is equivalent to a short circuit, and the diodes are reverse biased as shown in Fig. 4.3(a). The reserved energy in the capacitors C_1, C_2 is released to the inductor L_3, and coupled inductor windings L_1 and L_2. The primary winding of the HF transformer is charged by the stored energy in the capacitor C_p while the capacitor C_s is charged through secondary winding of the HF transformer. The stored energy in output inductor is transferred to the load. Thus, we get:

$$\begin{cases} -V_{c1} + v_{L2_{sh}} - v_{L1_{sh}} = 0 \\ v_{L1_{sh}} = v_{L2_{sh}} - V_{c1} - - - -(\text{i}) \\ k = {}^{v_{L1}}/_{v_{L2}} \\ -V_{in} + v_{L3_{sh}} - V_{c2} \\ v_{L3_{sh}} = V_{in} + V_{c2} - - - -(\text{ii}) \end{cases} \tag{4.1}$$

During the active states, as shown in Fig. 4.3(b), the diodes are 'on', and the bidirectional switch is turned 'off', The inductor L_3 windings of the coupled inductor L_1, L_2 and primary winding of the transformer charges the capacitors C_1, C_2 and C_p, while, output inductor is charged through secondary winding of the transformer and capacitor C_s. During this state, the reserved energy in the leakage inductances is consumed by C_1 and C_2 through diode D_c and it is, therefore, recycled without creating voltage spikes. Thus, by another application of KVL, we get:

$$\begin{cases} -V_{c1} - v_{L2_{non}} + v_{L1_{non}} + v_{pn} = 0 \\ -V_{in} - v_{L3_{non}} + v_{L2_{non}} + V_{c1} = 0 \\ v_{L3_{non}} = -V_{in} + v_{L2_{non}} + V_{c1} \\ v_{L3\_sh} = V_{in} + V_{c2} V_{c1} - - - -(\text{iii}) \\ v_{L1_{non}} = -V_{c2} \\ k v_{L2_{non}} = -V_{c2} \end{cases} \tag{4.2}$$

During the zero states, as shown in Fig. 3.3(c) and Fig. 3.3(d), either the upper two switches or the lower two switches are turned 'off'. In this mode, the capacitor C_p discharges and primary winding is charged by it, while the capacitor C_s is charged by the secondary winding of the transformer. Applying the flux-balance condition across L_1, and L_2 gives:

$$\begin{cases} v_{L2_{sh}} D = v_{L2_{non}} (1 - D) \\ v_{L2_{sh}} = -V_{c2} {(1 - D)}/{nD} \\ v_{L1_{sh}} D = v_{L1_{non}} (1 - D) \\ -V_{in} + v_{L3_{sh}} - V_{c2} = 0 \\ v_{L1_{sh}} = -V_{c2} {(1 - D)}/{D} - - - -(\text{iv}) \end{cases} \tag{4.3}$$

Substituting equation (iv) into (i) produces:

$$\begin{cases} v_{L1_{sh}} = v_{L2_{sh}} - V_{c1} \\ -V_{c2} {(1 - D)}/{D} = -V_{c2} {(1 - D)}/{kD} - V_{c1} \\ V_{c1} = V_{c2} {(k - 1)(1 - D)}/{kD} - - - -(\text{v}) \end{cases} \tag{4.4}$$

and applying flux balance condition across L_3, gives:

$$\begin{cases} (V_{in} + V_{c2})D = (v_{L2_{non}} - V_{in} + V_{c1})(1 - D) \\ V_{c2} = V_{in}\,{(kD)}\big/{k(1 - 2D) - 1 + D} \end{cases} \quad ----\text{(vi)} \tag{4.5}$$

Substituting eq. (vi) in (v) results in:

$$V_{c1} = \frac{V_{in}(1 - D)(k - 1)}{k(1 - 2D) - 1 + D} \tag{4.6}$$

where, *k* is the turns ratio of the coupled inductor in impedance network. Substituting the values of V_{c1} and V_{c2} in (4.2), yields:

$$v_{pn} = \frac{V_{in}(k - 1)}{k(1 - 2D) - 1 + D} \tag{4.7}$$

The voltages across capacitor C_p is the same as peak phase voltage, and it is given as:

$$v_{Cp} = Mv_{pn} = \frac{(1 - D)V_{in}(k - 1)}{k(1 - 2D) - 1 + D} \tag{4.8}$$

$$v_{Cs} = nv_{Cp} \tag{4.9}$$

As the average voltage across the secondary winding of HF transformer and L_o is zero, we have:

$$v_o = nMv_{pn} = n\frac{(1 - D)V_{in}(k - 1)}{k(1 - 2D) - 1 + D} \tag{4.10}$$

It should be noted that, '*k*' is the turns ratio of the coupled inductor in the impedance network while '*n*' is the turn ratio of the high frequency transformer (HFT). Since, $((k - 1)/k(1 - 2D) - 1 + D)$ is the boosting ability (*B*) of improved ΓZSI, the gain of the proposed isolated improved ΓZSI can be defined as:

$$G = \frac{v_o}{V_{in}} = nMB \tag{4.11}$$

From (4.11), it can be inferred that the voltage gain of the proposed isolated improved ΓZSI not only depends on the modulation index and the boost factor, but also relies on the turns ratio of HFT. Therefore, the voltage gain of the proposed isolated inverter can be increased utilizing higher turns ratio of the HFT, without further increasing the shoot-

through duty; consequently higher M is available for use. The voltage gain in terms of modulation index can be written as:

$$G(MB) = n\frac{M(k-1)}{M(2k-1)-k} \tag{4.12}$$

Fig. 4.4 shows the voltage gain vs. modulation index plot with k=1.75. The plot clearly shows the behaviour of the proposed isolated inverter with different values of n. As the turns ratio goes beyond 1, the gain begins to increase even with maximum value of modulation index – this is currently not possible with any other impedance source topology.

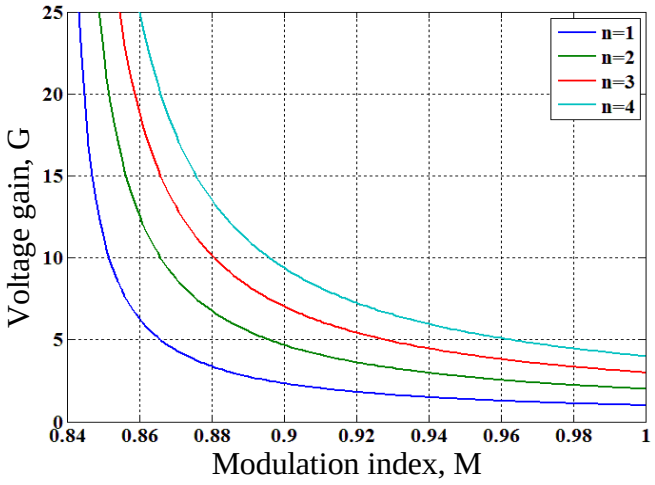


Fig. 4.4. Voltage gain versus modulation index plot for different values of n.

The increment in turns ratio of the high frequency transformer not only improves the power quality by keeping M higher, but it also reduces the voltage stresses across the components. By increasing turns ratio, the voltage stress across the switches can also be decreased compared to that in its non-isolated counter parts, which is a major concern in industrial applications. The maximum voltage stress across switches S_1, S_2, S_3, S_4 in the inverter bridge in Fig. 4.2 is equal to v_{pn}. In terms of voltage gain, it can be defined as:

$$v_{pn} = \frac{G(2k-1)+n(1-k)}{nk} \tag{4.13}$$

Fig. 4.5 shows the plot of voltage stress (normalized with input voltage) against the voltage gain. It can be seen from the figure that at n=1 the stress across the switches (inverter bridge) is the same as that of improved ΓZSI without isolation. With the increase in the turns ratio, the voltage stress across the switches reduces for the same voltage gain as seen in the plot. The voltage stress across switches S_5 and S_6 is same as v_{rec} (in Fig. 4.3), and is given as:

$$v_{rec} = \frac{G(2k-1) + n(1-k)}{nk} \tag{4.14}$$

Similarly, the voltage stress across the switches S_5, S_6 also decreases with the higher value of n for the same voltage gain.

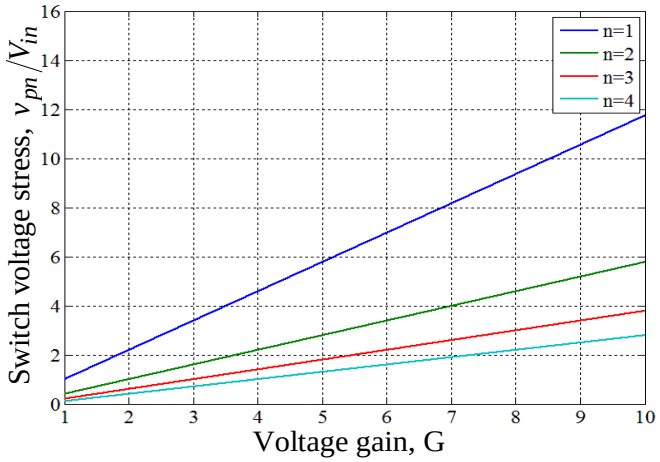


Fig. 4.5. Plot of inverter bridge switch stress against voltage gain for different values of *n*.

4.3 Pulse Width Modulation Strategy

The proposed class of isolated ZSIs can be controlled using the same modulation strategies proposed for single phase H-bridge ZSI [23]. The simple boost control scheme is applied to the proposed isolated inverter in this study. Fig. 4.6 illustrates the control scheme for the proposed inverters. It can be seen from Fig. 4.6 that all the switches of the inverter bridge have the same switching pattern, as in the case of existing ZSIs for simple boost control. However, the switches S_5 and S_6 at the secondary side of the transformer are turned on when the triangular (carrier) waveform v_{tri} is either higher or lower than

the phase references v_a and v_b. In other words, whenever the proposed isolated inverter operates in zero state, the switches S_5 and S_6 are turned 'on'.

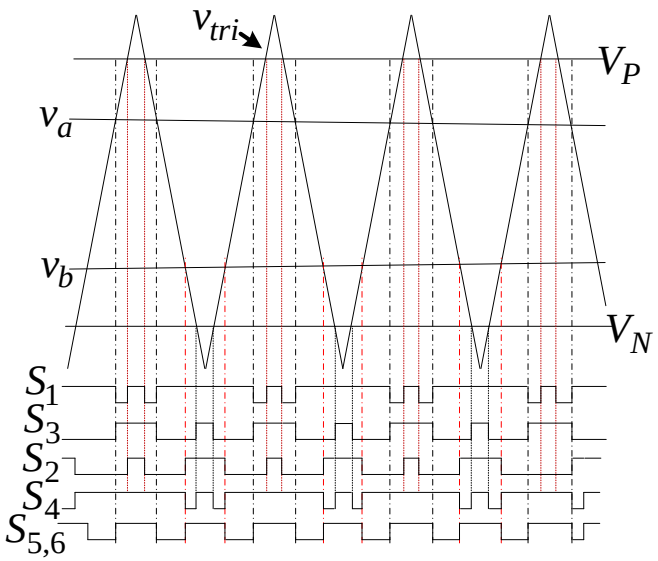


Fig. 4.6. PWM switching pattern for the simple boost control.

4.4 Simulation Results of the Proposed Isolated Improved ΓZSI with additional diode

To check the working of the proposed circuits, Saber simulations are performed. The circuit parameters are selected as: 1) Input voltage: $V_{in} = 43\ V$ 2) Output voltage: $v_o = 110\ V_{rms}$ 3) Switching frequency: 20 *k*Hz. 4) High frequency transformer: L_m= 1 *m*H, *n*=1.5. 5) Coupled inductor turns ratio $k = k_1 = k_2 = 1.75$. 6) All inductors: 850 µH. 7) All capacitors: 6.8 µF. 8) Shoot-through duty cycle: 0.2.

The control strategy as depicted in 4.6 in saber simulations are implemented using logic gates and comparators. Only two reference waveform generators are used for v_a and v_b reference waveforms. Switches S5 and S6 are turned on whenever the inverter operates in zero states. Fig. 4.7 shows the control scheme block diagram in saber.

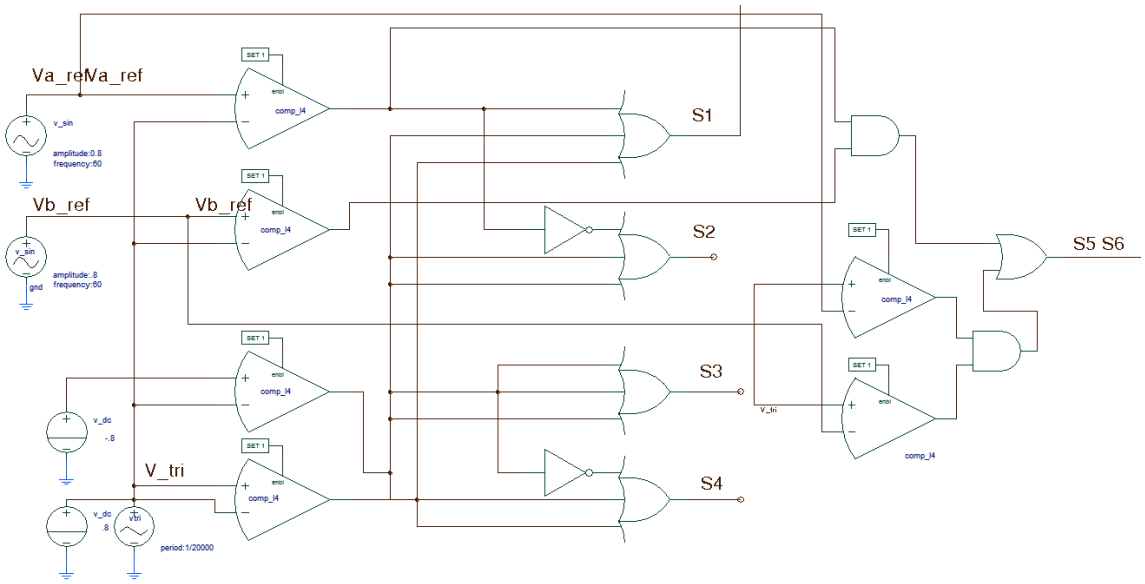
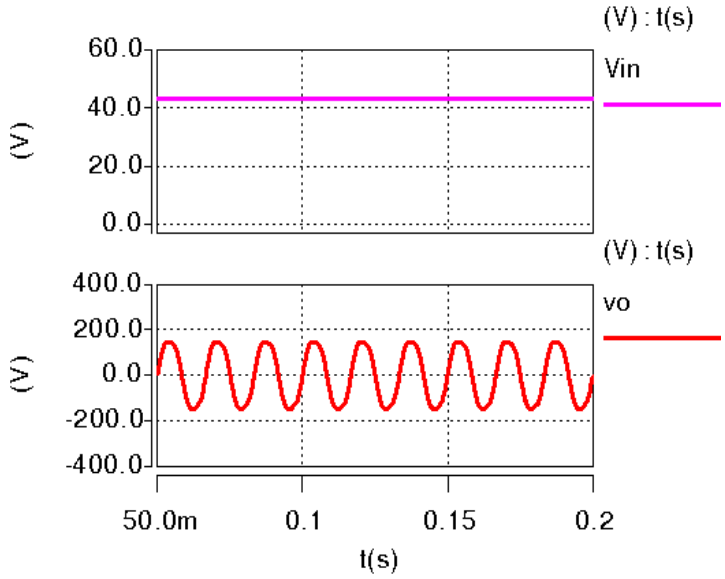
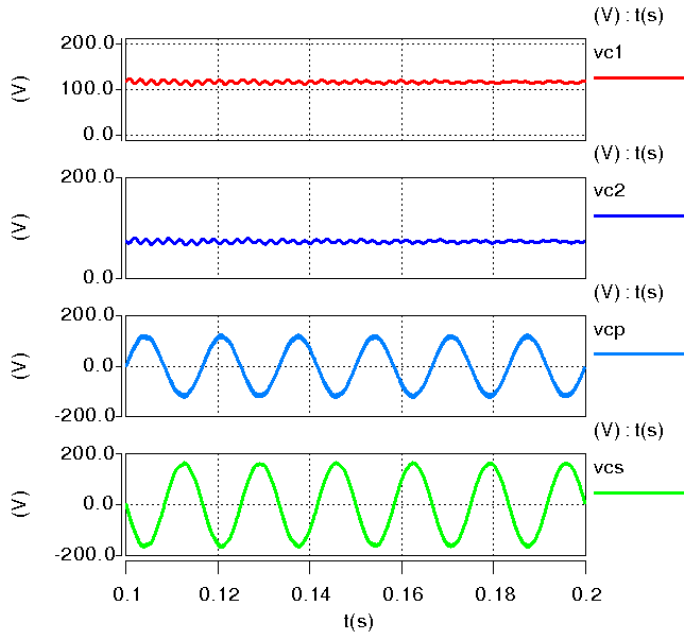


Fig. 4.7 Block diagram of control strategy for the proposed class of HFT isolated ZSIs.

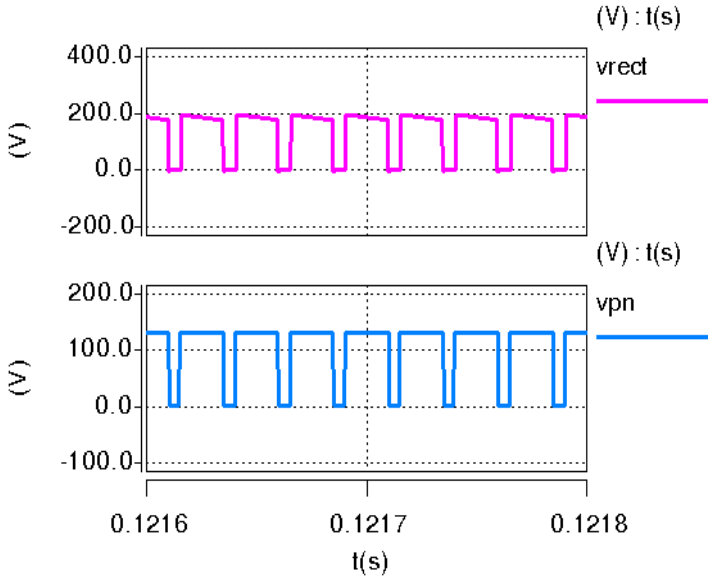
Fig. 4.8 (a) shows the input voltage and output voltage waveforms .Fig. 4.8 (b) shows the capacitor waveforms $C_1, C_2, C_p,$ and C_s. Fig. 4.8 (c) shows the v_{rect} and v_{pn} voltage waveforms.



(a)



(b)



(c)

Fig. 4.8 Simulation results of the proposed isolated improved ΓZSI (a) Input voltage and output voltage (b) voltages across the capacitors V_{c1}, V_{c2}, v_{cp} and v_{cs} (c) voltage across v_{pn} and v_{rect}

4.5 Prototype Type based Validation

A hardware prototype of the high frequency transformer-isolated ΓZSI proposed in Section 4.2 was fabricated in the laboratory to validate the physical implementation of the design. Same platform is used for the experimental validation as discussed in Section 3.7.1. A DSP-kit, based on TMS320f28335 and shown in Fig. 4.9, was utilized to implement the control strategy elaborated in Section 4.3 for the proposed isolated ΓZSI inverter.

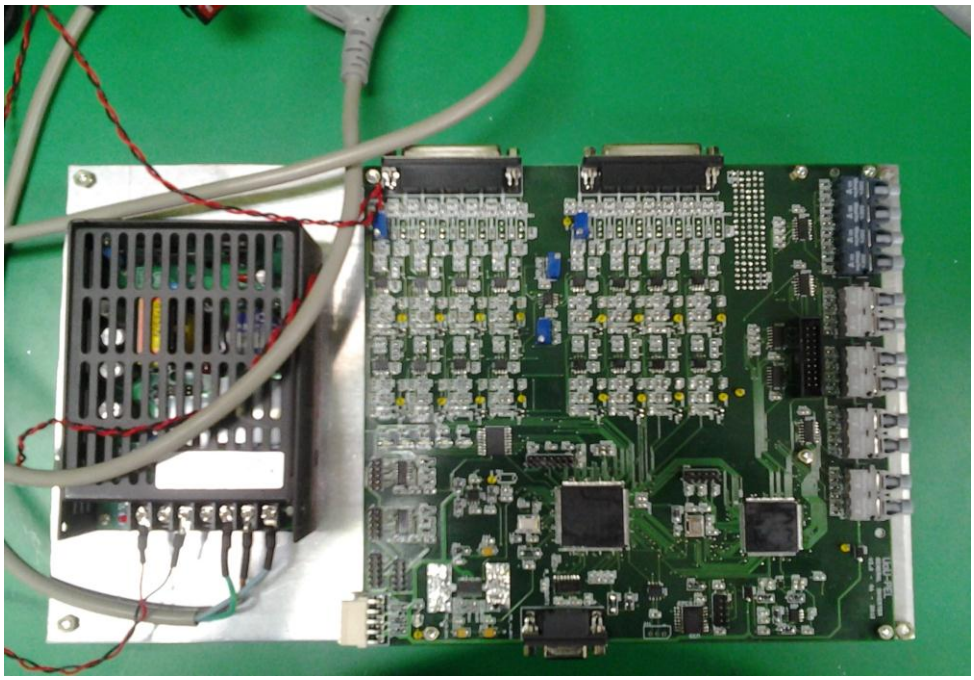


Fig. 4.9 DSP Kit based on TMS320f28335

4.5.1 Parameter Design of High Frequency Transformer

The HFT design of the proposed isolated improved ΓZSI is discussed in this section. The parameters are determined based on maximum allowable voltage and current stresses.

During shoot-through state *DT*, the voltage across inductors L_1, L_2 and L_m of transformer are $V_{c2} + V_{in}$, V_{c1}, and V_{cp} respectively. Therefore, we get:

$$L_m = \frac{v_{cp}}{\Delta i_{Lm}} DT \tag{4.15}$$

The value of v_{cp} changes sinusoidally and its maximum value is given by (4.8). By assuming the maximum allowable current ripple for L_m is $\Delta i_{Lm} \leq x\% I_o$ respectively, and further solving (4.15), we get:

$$L_m = \frac{nV_{in}^2(1-D)^2(k-1)^2}{\sqrt{2}(k(1-2D)-1+D)^2 x\% P_o} \tag{4.16}$$

Where, I_o, and P_o are the rms values of output current and power respectively.

4.5.2 Experimental Results

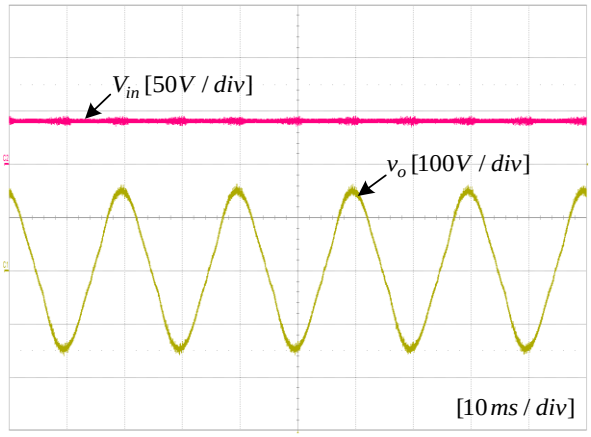
The detailed electrical specifications of the prototype isolated inverter are given in Table 4.1, which were the same as those used for the simulations. Details relating to the PCB design of the hardware is given in Appendix C.

TABLE 4.1

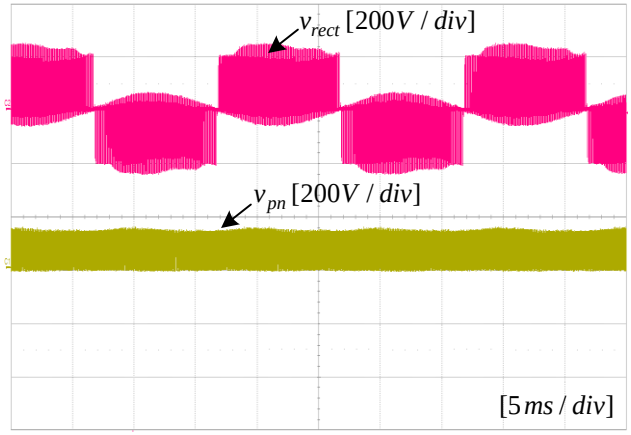
Electrical Specifications for HFT Isolated Improved ΓZSI

Input voltage	43 V
Output voltage	110 VRMS/ 60 Hz
Switching frequency	20 kHz
Transformer	$L_m = 1.5\ mH, n = 1.5$
Coupled Inductor	$k = 1.75$
Capacitors $(C_1, C_2, C_p, C_s, C_o)$	6.8 μF
Inductors (L_3, L_o)	850 μH

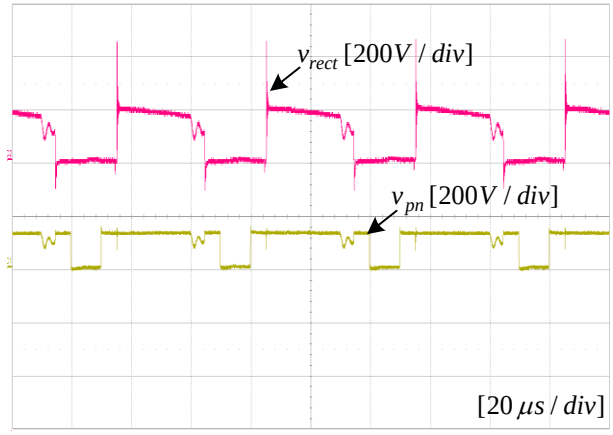
Fig. 4.10 (a) shows the experimental waveforms of input and output voltage. Fig. 4.10 (b) shows the waveforms of v_{pn} and v_{rec} and Fig. 4.10 (c) shows its expanded waveforms. Fig. 4.10 (d) shows the waveforms of the voltage across capacitors C_1, C_2, C_p and C_s. All of the given experimental results comply with the aforementioned analysis and thus, verify the practical working and benefits of the proposed isolated improved ΓZSI


V_{in} [50V / div]
v_o [100V / div]
[10 ms / div]

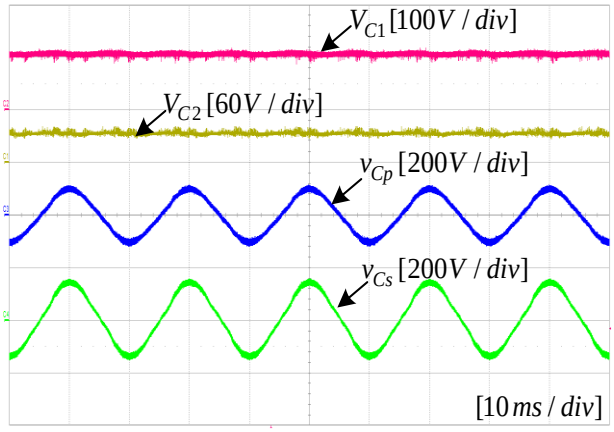
(a)


v_{rect} [200V / div]
v_{pn} [200V / div]
[5 ms / div]

(b)


v_{rect} [200V / div]
v_{pn} [200V / div]
[20 μs / div]

(c)



(d)

Fig. 4.10. Experimental waveforms of proposed isolated improved ΓZSI. (a) Input and output voltages. (b) v_{pn} and v_{rect} waveforms: Zoom out mode. (d) Capacitor voltages.

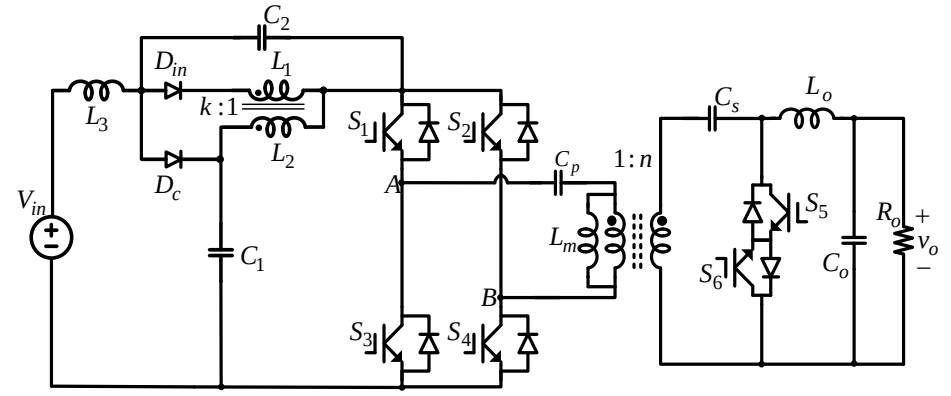
4.6 Extension of the Proposed Technique to Magnetically Coupled ZSIs

The main concept of high frequency isolation can be applied to all the existing transformer (coupled inductor) based impedance source inverters and similar analysis can be performed as discussed briefly in the previous section. Fig. 4.11 shows the structures of several high frequency isolated ZSIs which are derived from their classical non-isolated versions. As it can be seen from the Fig. 4.11, all the proposed isolated inverters retain their existing impedance network and benefits. In addition to these, they contain high frequency transformer and a small dc blocking capacitor on the primary side. While, capacitor C_s and bidirectional switch are on the secondary side to restore the dc component of the voltage. Moreover additional diode helps in recycling the leakage inductance energy of the magnetic components resulting in reduced voltage spikes across the inverter bridge. The description and the main features of the impedance source networks of the proposed isolated inverters are explained below:

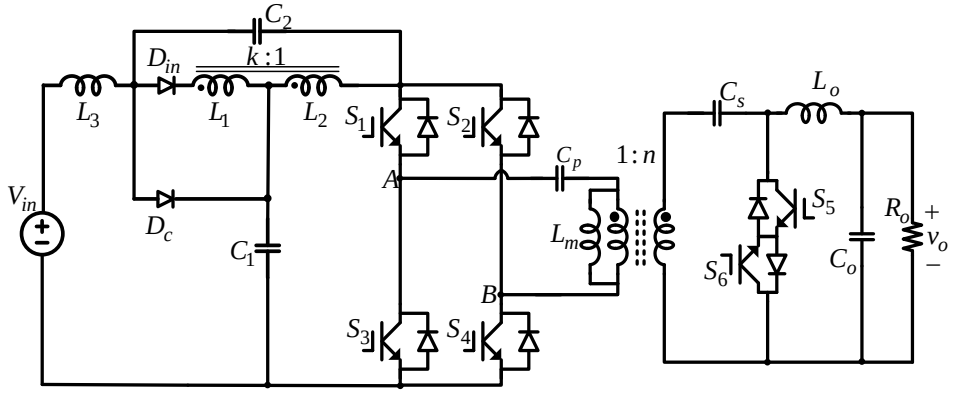
- Fig. 4.11 (a) shows the proposed HF isolated LCCT-ZSI based on LCCT-ZSI [10] which consists of one coupled inductor with windings L_1 and L_2, one inductor L_3

and two capacitors C_1, C_2. It has improved input profiles and reduced inrush current.

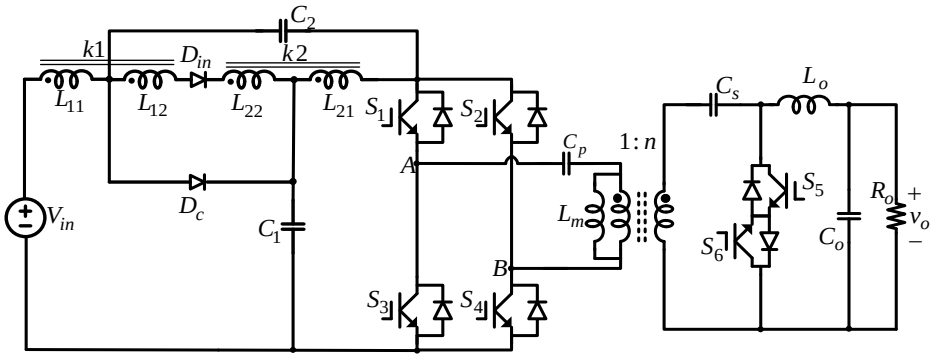
- Fig. 4.11 (b) shows the proposed HF isolated improved trans-ZSI based on improved trans-ZSI [11]. It has the same number of components as of isolated LCCT-ZSI, and isolated improved ΓZSI but with a slightly different coupled inductor placement. In this structure, turns ratio (*k*) of the coupled inductor can also be increased to achieve a higher voltage gain.
- Fig. 4.11 (c) shows the proposed HF isolated quasi-tZSI based on tZSI [12]. This inverter replaces the two inductors in the qZSI with two coupled inductors.
- Fig. 4.11 (d) shows the proposed HF isolated ΣZSI based on ΣZSI [16]. Unlike tZSI, the turns ratio of the coupled inductors are lowered to achieve a higher gain.



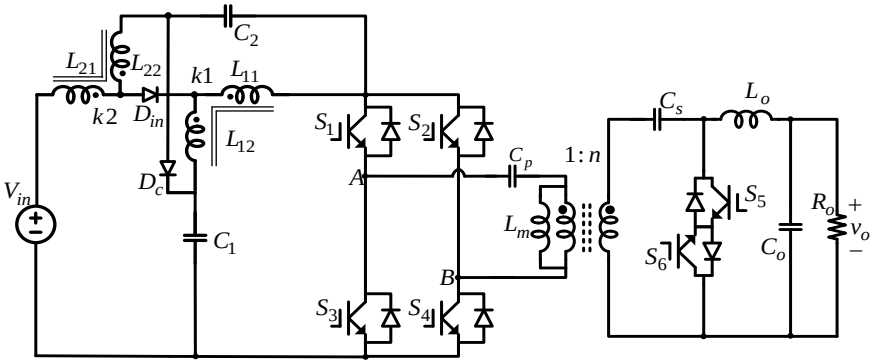
(a)



(b)



(c)



(d)

Fig. 4.11. Proposed isolated impedance source inverters. (a) Isolated LCCT-ZSI. (b) Isolated improved trans-ZSI. (c) Isolated quasi-tZSI. (d) Isolated ΣZSI.

Table 4.2 summarizes all the voltage stresses of the components in the proposed high frequency isolated impedance source inverters and their voltage gains. In Table 4.2, n is the turns ratio of the high frequency transformer and k (k_1, k_2) are the turns ratio of the coupled inductors in the impedance network. The Table 4.2 is a guideline for practical engineers to design and implement the proposed circuits in industrial applications. The equations in table shows the power rating of each circuit which can be directly used to select the components according to the requirements and eliminates the need for theoretically deriving each and every circuit which is a major time saver.

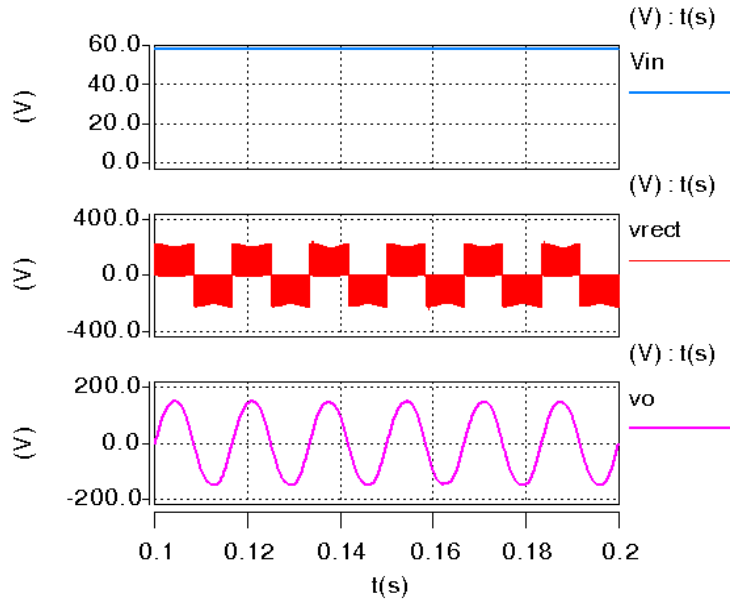
TABLE 4.2

Summary of Magnetically Coupled HF Isolated ZSIs Voltage Stresses

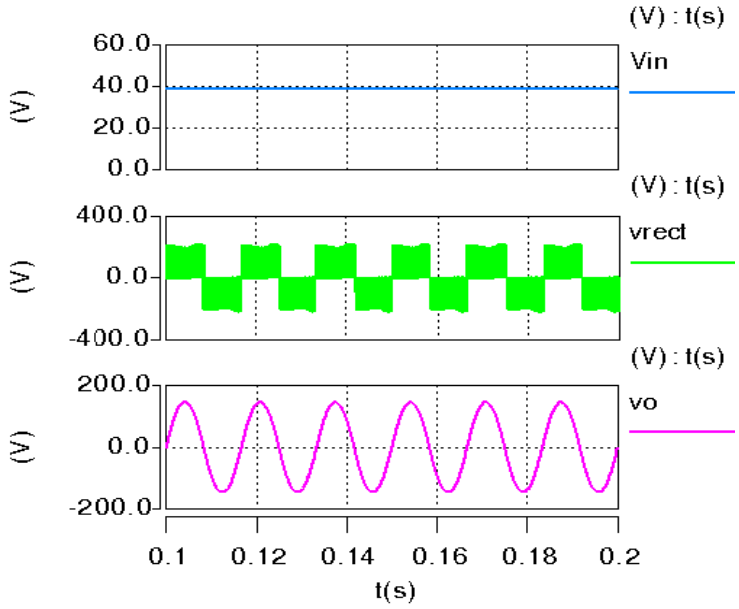
	Fig. 4.11 (a)	Fig. 4.11 (b)	Fig. 4.11 (c)	Fig. 4.11 (d)
V_{c1}	$\frac{(1-D)V_{in}}{1-(1+k)D}$	$\frac{(1-D)V_{in}}{1-(2+k)D}$	$\frac{(1-D)V_{in}}{1-(2+k_1+k_2)D}$	$\frac{(1-D)V_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
V_{c2}	$\frac{(D)V_{in}}{1-(1+k)D}$	$\frac{(1+k)V_{in}}{1-(2+k)D}$	$\frac{(1+k_1+k_2)DV_{in}}{1-(2+k_1+k_2)D}$	$\frac{\frac{(k_1k_2-1)(D)V_{in}}{(k_1-1)(k_2-1)}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
v_{pn}	$\frac{V_{in}}{1-(1+k)D}$	$\frac{V_{in}}{1-(2+k)D}$	$\frac{V_{in}}{1-(2+k_1+k_2)D}$	$\frac{V_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
v_{cp}	$\frac{(1-D)V_{in}}{1-(1+k)D}$	$\frac{(1-D)V_{in}}{1-(2+k)D}$	$\frac{(1-D)V_{in}}{1-(2+k_1+k_2)D}$	$\frac{(1-D)V_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
v_{cs}	$\frac{(1-D)nV_{in}}{1-(1+k)D}$	$\frac{(1-D)nV_{in}}{1-(2+k)D}$	$\frac{(1-D)nV_{in}}{1-(2+k_1+k_2)D}$	$\frac{(1-D)nV_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
v_{rec}	$\frac{nV_{in}}{1-(1+k)D}$	$\frac{nV_{in}}{1-(2+k)D}$	$\frac{nV_{in}}{1-(2+k_1+k_2)D}$	$\frac{nV_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$
v_o	$\frac{(1-D)nV_{in}}{1-(1+k)D}$	$\frac{(1-D)nV_{in}}{1-(2+k)D}$	$\frac{(1-D)nV_{in}}{1-(2+k_1+k_2)D}$	$\frac{(1-D)nV_{in}}{1-\left(2+(\frac{1}{k_1-1})+(\frac{1}{k_2-1})\right)D}$

4.6.1 Simulation Results of the Proposed Isolated Inverters

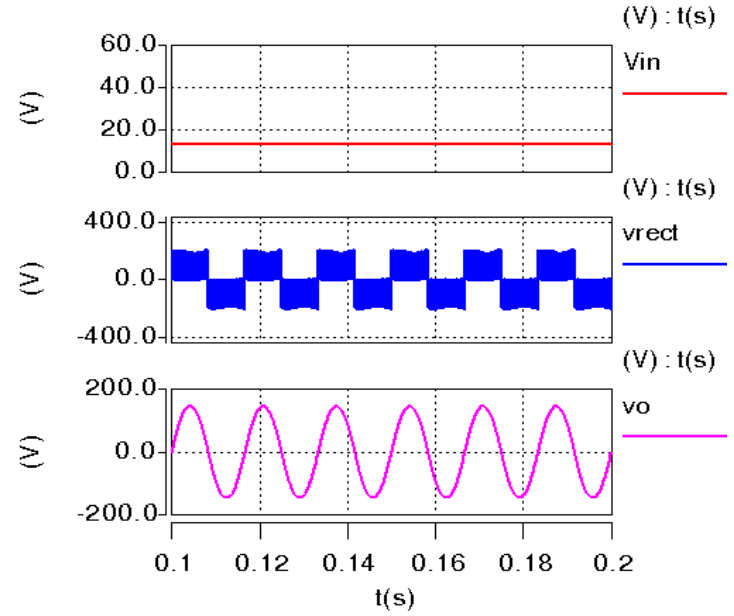
In order to validate the working of the isolated inverter circuits proposed above, Saber simulations were performed. The input voltage was varied for each of the proposed inverter circuits due to their different voltage gain properties, as to achieve the desired fixed output voltage of 110 V_{rms}/60 Hz. Fig. 4.12(a) shows the simulations of isolated LCCT-ZSI and Fig. 4.12(b) shows the waveforms of isolated improved trans-ZSI. Fig. 3.9(c) shows the simulation results of isolated quasi-TZSI. Fig. 4.12(d) shows the results of proposed isolated ΣZSI. All the simulation results shown agreement with the derived equations in Table 4.2.


(V) : t(s)
Vin
60.0
40.0
20.0
0.0
(V)
(V) : t(s)
vrect
400.0
0.0
-400.0
(V)
(V) : t(s)
vo
200.0
0.0
-200.0
(V)
0.1
0.12
0.14
0.16
0.18
0.2
t(s)

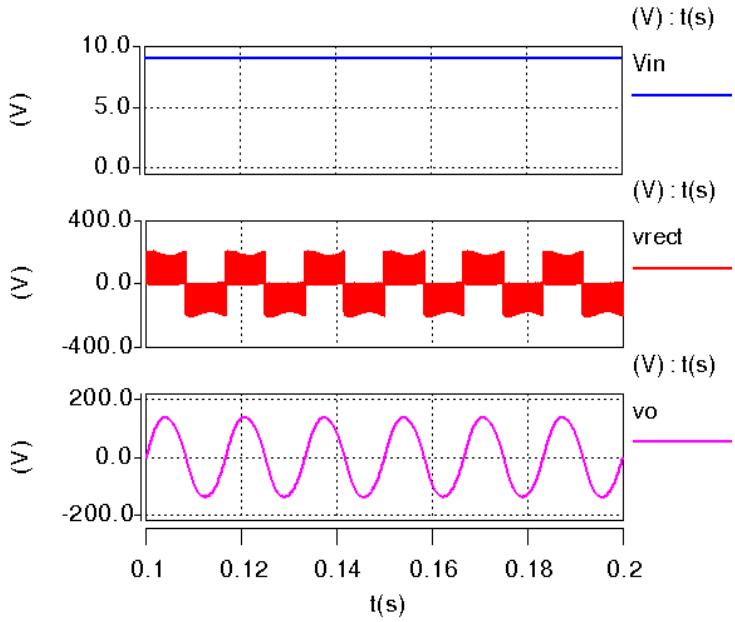
(a)


(V) : t(s)
Vin
60.0
40.0
20.0
0.0
(V)
(V) : t(s)
vrect
400.0
0.0
-400.0
(V)
(V) : t(s)
vo
200.0
0.0
-200.0
(V)
0.1
0.12
0.14
0.16
0.18
0.2
t(s)

(b)



(c)



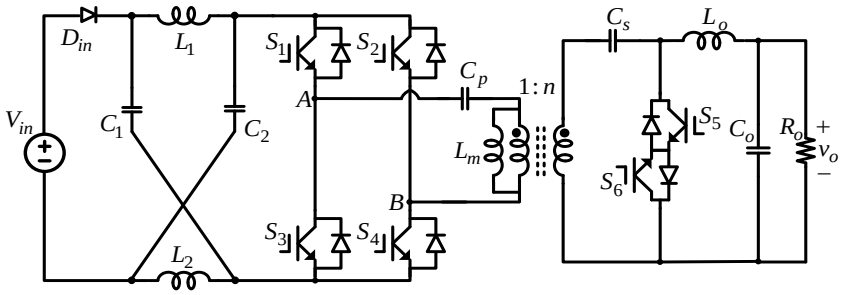
(d)

Fig. 4.12. Simulations of proposed isolated magnetically coupled impedance source inverters. (a) Isolated LCCT-ZSI with V_{in}= 58V. (a) Isolated improved trans-ZSI with $V_{in} = 38V$. (c) Isolated QTZSI with V_{in} = 13V. (d) Isolated ΣZSI with V_{in} = 9V.

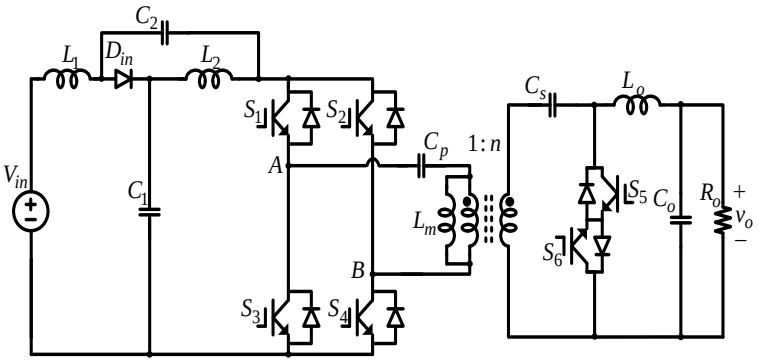
4.7 Extension of the Proposed HF Isolation to Transformerless ZSIs

The concept of high frequency isolation can be applied to existing transformerless ZSIs in a similar way to how it is used for transformer based ZSIs to attain the additional benefits of electrical isolation in terms of protection and to meet the safety standards. All of the ZSIs will retain the benefits of their non-isolated counter parts with the additional benefits of HFT. Additionally, in the case of transformerless ZSIs, the absence of coupled inductors in the impedance network automatically eliminates the leakage inductance problem caused by imperfect coupling. Thus, it minimizes the voltage spikes across the inverter bridge without the need of an additional clamping diode or clamp circuit. Moreover, the stray inductance of the impedance network can be reduced by minimizing the high frequency loop between the inverter bridge and the DC-source. Fig. 4.13 shows the circuits of several isolated ZSIs derived from their original impedance networks. The description and the main features of the impedance source networks of the proposed isolated inverters are explained below:

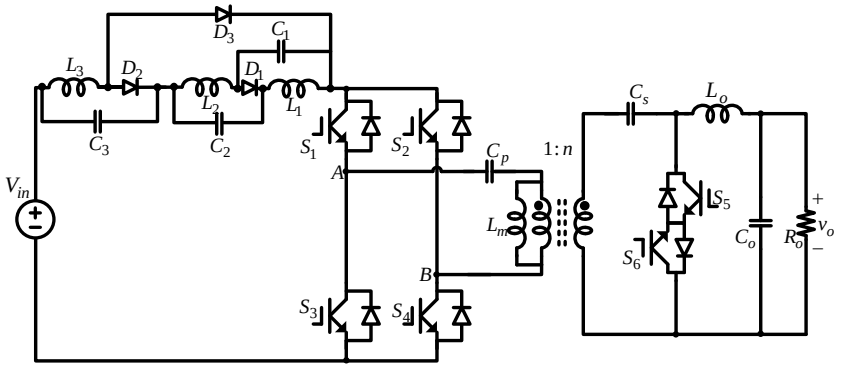
- Fig. 4.13(a) shows the conventional ZSI with high frequency isolation.
- Fig. 4.13 (b) shows the isolated qZSI structure.
- Fig. 4.13 (c) and (d) shows the isolated versions of the diode assisted and capacitor assisted extended boost ZSIs, in which multiple diodes and capacitors are added in the Z-source network.
- Fig. 4.13 (e) shows the isolated version of ZSI based on switched inductor (SL) network. It is obtained by replacing the two inductors L_1 and L_2 with two SL cells. Each SL cell consist of three diodes (D_1-D_6) and two inductors (L_1-L_4). It has discontinuous input current and unshared ground between input and inverter bridge.
- In fig. 4.13 (f), high frequency isolated SL-qZSI. It overcomes the drawbacks faced with SL-ZSI. It is obtained by replacing inductor L_2 in qZSI with the SL cell.
- Fig. 4.13 (g) shows the isolated L-ZSI based on L-ZS structure. This unique L-ZSI consists of only inductors (L_1, L_2) and diodes (D_1,D_2,D_3) in the Z-source network.


D_{in}
L_1
S_1
S_2
C_p
$1:n$
C_s
L_o
V_{in}
C_1
C_2
A
L_m
S_5
C_o
R_o
+
v_o
−
S_6
B
S_3
S_4
L_2

(a)


C_2
L_1
D_{in}
L_2
S_1
S_2
C_p
$1:n$
C_s
L_o
V_{in}
C_1
A
L_m
S_5
C_o
R_o
+
v_o
−
S_6
B
S_3
S_4

(b)


D_3
C_1
L_3
D_2
D_1
L_2
L_1
C_3
C_2
S_1
S_2
C_p
$1:n$
C_s
L_o
V_{in}
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L_m
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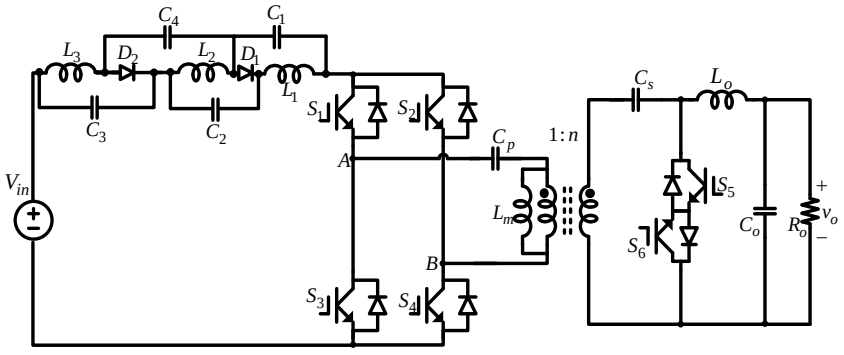
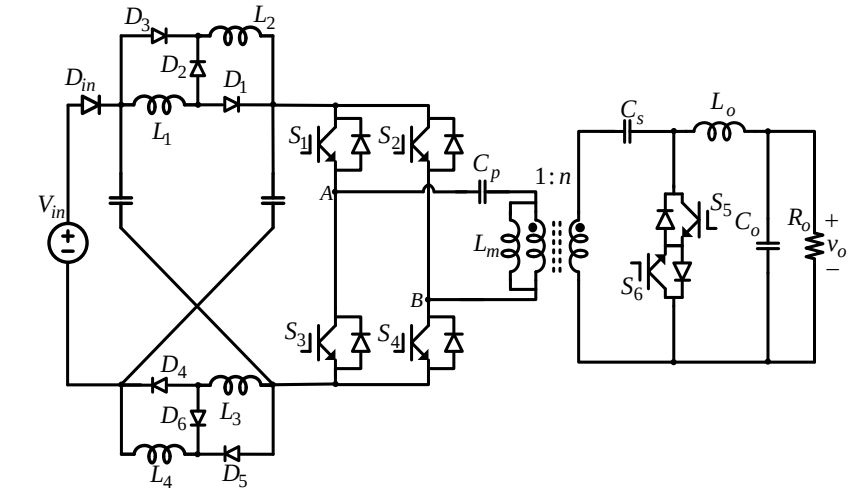
C_o
R_o
+
v_o
−
S_6
B
S_3
S_4

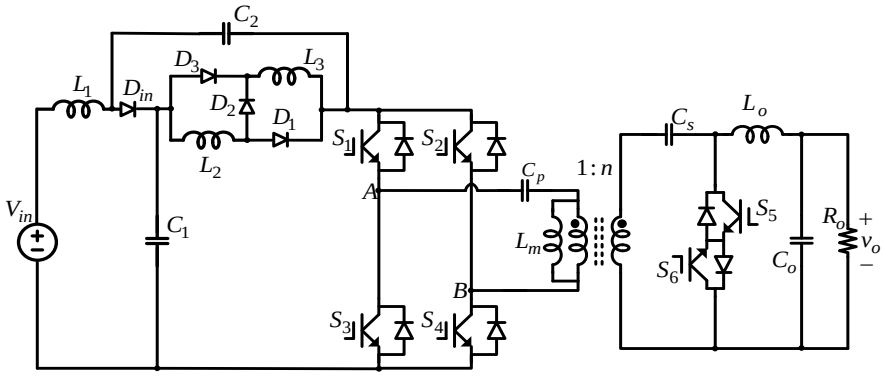
(c)


C_4
C_1
L_3
D_2
L_2
D_1
L_1
C_3
C_2
S_1
S_2
C_p
$1:n$
C_s
L_o
V_{in}
A
L_m
S_5
C_o
R_o
+
v_o
−
S_6
B
S_3
S_4

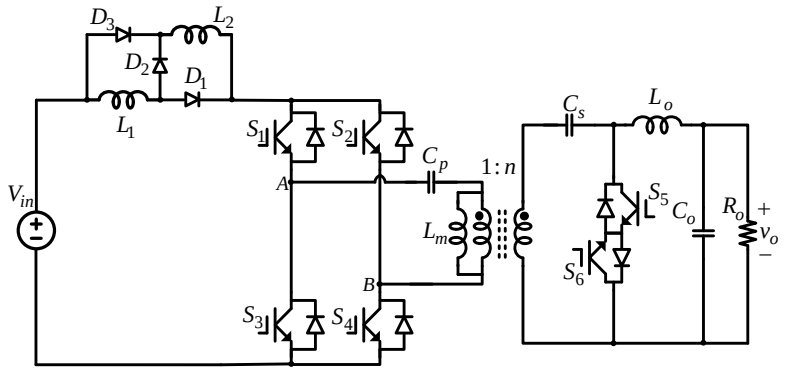
(d)



(e)



(f)



(g)

Fig. 4.13. Proposed isolated impedance source inverters. (a) Conventional isolated ZSI. (b) Isolated qZSI. (c) Isolated diode-assisted extended-boost ZSI. (d) Isolated capacitor-assisted extended-boost ZSI. (e) Isolated SL-ZSI. (f) Isolated SL-(q)ZSI. (g) Isolated L-ZSI.

Table 4.3 summarizes all the voltage stresses of the components in the proposed high frequency isolated impedance source inverters and their voltage gains.

TABLE 4.3

Summary of Transformerless High Frequency Isolated ZSIs Voltage Stresses

	Fig. 4.13 (a)	Fig. 4.13 (b)	Fig. 4.13 (c)	Fig. 4.13 (d)	Fig. 4.13 (e)	Fig. 4.13 (f)	Fig. 4.13 (g)
V_{c1}	$\frac{(1-D)V_{in}}{1-2D}$	$\frac{(1-D)V_{in}}{1-2D}$	$\frac{(D)V_{in}}{(1-2D)(1-D)}$	$\frac{(D)V_{in}}{1-3D}$	$\frac{(1+D)(1-D)V_{in}}{1-3D}$	$\frac{(1-D)V_{in}}{1-2D-D^2}$	N/A
V_{c2}	$\frac{(1-D)V_{in}}{1-2D}$	$\frac{(D)V_{in}}{1-2D}$	$\frac{(D)V_{in}}{(1-2D)(1-D)}$	$\frac{(D)V_{in}}{1-3D}$	$\frac{(1+D)(1-D)V_{in}}{1-3D}$	$\frac{(2D)V_{in}}{1-2D-D^2}$	N/A
v_{pn}	$\frac{V_{in}}{1-2D}$	$\frac{V_{in}}{1-2D}$	$\frac{V_{in}}{(1-2D)(1-D)}$	$\frac{V_{in}}{1-3D}$	$\frac{(1+D)V_{in}}{1-3D}$	$\frac{(1+D)V_{in}}{1-2D-D^2}$	$\frac{(1+D)V_{in}}{1-D}$
v_{cp}	$\frac{(1-D)V_{in}}{1-2D}$	$\frac{(1-D)V_{in}}{1-2D}$	$\frac{(1-D)V_{in}}{(1-2D)(1-D)}$	$\frac{(1-D)V_{in}}{1-3D}$	$\frac{(1+D)(1-D)V_{in}}{1-3D}$	$\frac{(1-D)(1+D)V_{in}}{1-2D-D^2}$	$\frac{(1+D)(1-D)V_{in}}{1-D}$
v_{cs}	$\frac{(1-D)nV_{in}}{1-2D}$	$\frac{(1-D)nV_{in}}{1-2D}$	$\frac{(1-D)nV_{in}}{(1-2D)(1-D)}$	$\frac{(1-D)nV_{in}}{1-3D}$	$\frac{(1+D)(1-D)nV_{in}}{1-3D}$	$\frac{(1-D)(1+D)nV_{in}}{1-2D-D^2}$	$\frac{(1+D)(1-D)nV_{in}}{1-D}$
v_{rec}	$\frac{nV_{in}}{1-2D}$	$\frac{nV_{in}}{1-2D}$	$\frac{(n)V_{in}}{(1-2D)(1-D)}$	$\frac{nV_{in}}{1-3D}$	$\frac{(1+D)nV_{in}}{1-3D}$	$\frac{(1+D)nV_{in}}{1-2D-D^2}$	$\frac{(1+D)nV_{in}}{1-D}$
v_o	$\frac{(1-D)nV_{in}}{1-2D}$	$\frac{(1-D)nV_{in}}{1-2D}$	$\frac{(1-D)nV_{in}}{(1-2D)(1-D)}$	$\frac{(1-D)nV_{in}}{1-3D}$	$\frac{(1+D)(1-D)nV_{in}}{1-3D}$	$\frac{(1-D)(1+D)nV_{in}}{1-2D-D^2}$	$\frac{(1+D)(1-D)nV_{in}}{1-D}$

The proposed isolated structures can be simulated using the same simulation modelling approach discussed in Section 4.4 and Section 4.6.1. The only difference is the absence of clamping diode and magnetically coupled element from the impedance network which will not effect the working principle of the proposed concept.

4.8 Conclusions

In this chapter, a new and improved class of Z-source inverters is proposed that utilizes a high frequency transformer. As explained in Section 4.2, the proposed inverters retained

all the existing benefits of their non-isolated counterparts, namely they supported 1) single stage buck-boost power conversion, 2) immunity from short-circuit of voltage source or open circuit of inductor, and 3) improved reliability.

In addition to these advantages, use of the high frequency transformer provides electrical isolation and improved safety by avoiding the injection of DC current into the grid when used in grid-tied photo-voltaic systems. The proposed design also eliminates the need for heavy and bulky line transformers. Moreover, the proposed family of inverters have more freedom in adjusting the voltage gain. They can perform step-up operation by increasing the turns ratio of the HF transformer without further increasing the duty ratio. Hence, a higher modulation index is available for use which results in reduced voltage stress and improved output quality.

Several isolated impedance source inverters are proposed in this paper and their simulations verifications are shown. An example of isolated improved ΓZSI is presented in brief to explain their operations and benefits. A hardware prototype of the isolated improved ΓZSI was fabricated; experiments using this prototype were conducted and which validated the simulation results. Further work on this topic concerns additional physical experimentation using the other types of transformer-based and transformerless Z-source topologies that were presented earlier in this chapter.

5. Chapter 5
Parallel Operation of Improved Z-Source Inverter based on Magnetic Coupling

5.1 Introduction

Due to the substantial shortage of conventional energy sources, utilization of renewable energy is gaining attention [61-63]. Therefore, high power inverters for photo-voltaic (PV) and wind power generation systems are in huge demand. Parallel connected inverters for high power conversion systems are more desirable because of the limitations faced by switching devices in terms of its voltage and current ratings. Modular configured converters are imminent in high power industrial applications due to their numerous benefits over singular high capacity converter or inverter. They can be realized with reduced component stress by sharing the currents, ease of maintenance, modularity facilitating plug and play, higher reliability, and (N+1) redundancy.

Modular inverters [25, 26, 64-69] are widespread in power conversion systems due to their dominant features: System wise benefits comprise the easing of thermal management, reducing the component stress, reduction in the manufacturing cost by standardization of system components, increasing the reliability through structural redundancy, and improved modularity. In terms of performance wise benefits, parallel connected inverters allows for the reduction of the output ripples by using interleaving pattern which results in lowering the requirements for input and output filters. .

Fig. 5.1 shows the general circuit configuration of parallel connected inverters. These inverters can be voltage source inverter or current source inverter depending upon the conditions. In Fig. 5.1, the switching devices of the inverter 1 and inverter 2 are phase

shifted by 180° to achieve the interleaving effect which can greatly reduce the filter requirements.

This technique can be applied to ZSIs which will result in improved performance of the overall power system while retaining the benefits of ZSI topologies with enhanced boosting abilities.

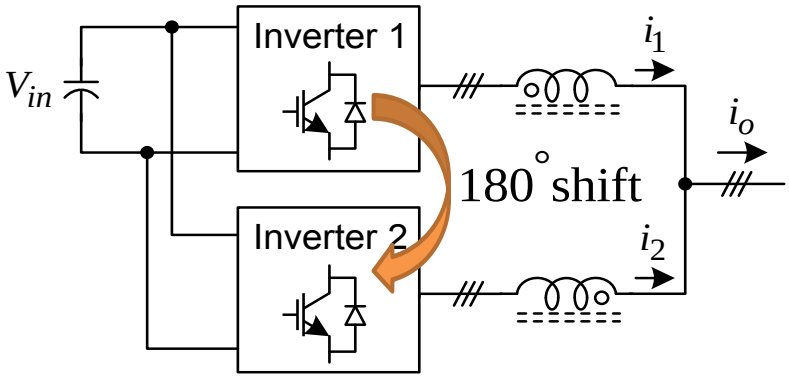


Fig. 5.1. Parallel operation of the inverters

5.2 Proposed Parallel Operated Improved Z-Source Inverter Using Magnetic Coupling

Since the power ratings of the active switches are limited due to technical considerations [70-71], utilization of parallel connections have been preferred in high power industrial applications owing to its significant benefits as discussed earlier in section 5.1. In this chapter, an improved parallel connected ZSI with magnetic coupling is proposed, analysed in detail and verified through simulations and experiments. Fig. 5.2 shows the basic circuit of the proposed converter topology. One of the main advantages of proposed structure is its expandability, that many identical inverters can be easily paralleled to obtain both high voltage gain and increased power ratings while retaining all the benefits of Z-source inverters.

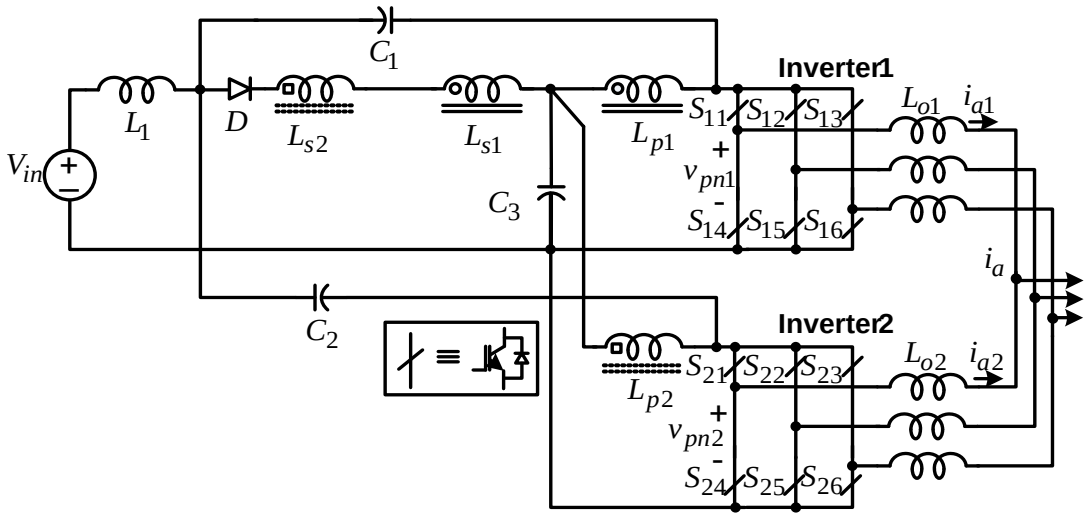
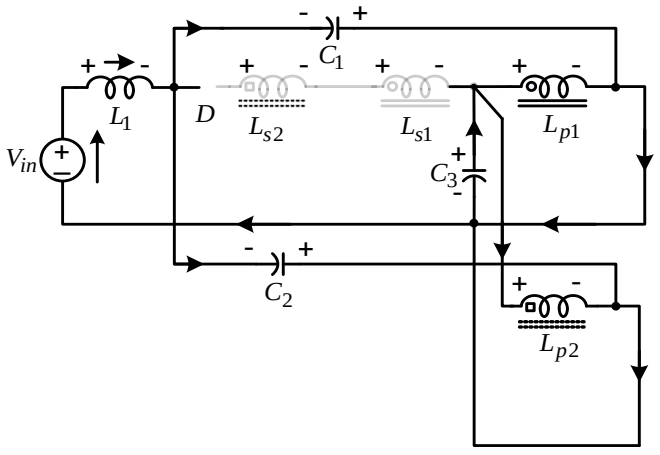


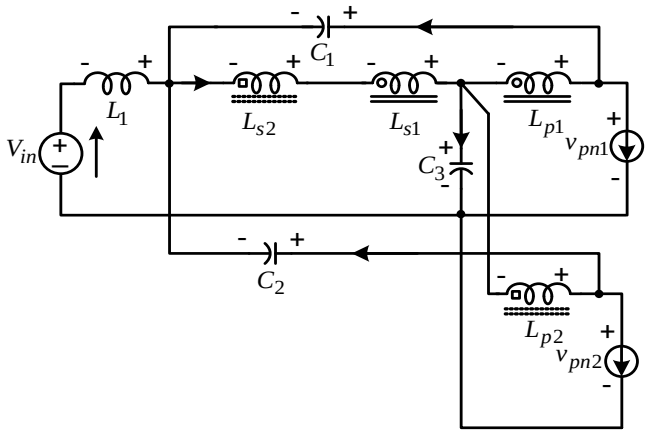
Fig. 5.2. Proposed parallel connected improved-ZSI based on magnetic coupling.

5.2.1 Working Principle of the Proposed Inverter and its Circuit Analysis

Fig. 5.3 elaborates the operating modes of the proposed inverter. Similar to existing Z-source inverters, the proposed inverter also consists of six active states, two zero states, and one shoot-through state. The equivalent circuits of these shoot-through and non-shoot-through states are shown in fig. 5.3(a) and (b). In Fig. 5.3, (L_{p1},L_{s1}) and (L_{p2},L_{s2}) represents the primary and secondary windings of each coupled inductor or transformer.



(a) State 1: shoot-through state



(b) State 2: non shoot-through state

Fig. 5.3. Operation states of the proposed inverter.

Fig. 5.3(a) shows the shoot-through state in which the circuit is equivalent to a short circuit. Analysing this state yields:

$$\begin{cases} -V_{in} + v_{L1} - V_{C1} = 0 \\ -V_{in} + v_{L1} - V_{C2} = 0 \\ -V_{c3} + v_{Lp1} = 0 \\ -V_{c3} + v_{Lp2} = 0 \\ v_{Ls} = n v_{Lp} \end{cases} \tag{5.1}$$

Similarly, by applying KVL in the non-shoot-through state (active state) in fig. 5.3(b), yields:

$$\begin{cases} -V_{in} - v_{L1} - V_{C1} + v_{pn1} = 0 \\ -V_{in} - v_{L1} - V_{C2} + v_{pn2} = 0 \\ -v_{pn1} + V_{c3} + v_{Lp1} = 0 \\ -v_{pn2} + V_{c3} + v_{Lp2} = 0 \\ -V_{in} - v_{L1} - v_{Ls2} - v_{Ls1} + V_{c3} = 0 \end{cases} \tag{5.2}$$

By applying voltage second condition across L_2, L_{p1}, and L_{p2}, we obtain:

$$\begin{cases} (-V_{in} - V_{c1})D = (-V_{in} - V_{c1} + v_{pn1})(1 - D) \\ (-V_{in} - V_{c2})D = (-V_{in} - V_{c2} + v_{pn2})(1 - D) \\ -V_{c3}D = (V_{c3} - v_{pn1})(1 - D) \\ -V_{c3}D = (V_{c3} - v_{pn2})(1 - D) \end{cases} \tag{5.3}$$

By solving (5.3) for V_{c1}, V_{c3}, V_{c3}, and v_{pn}, we obtain:

$$\begin{cases} V_{c1} = V_{c2} = \dfrac{(1+2n)D}{1-(2+2n)D} V_{in} \\ V_{c3} = \dfrac{1-D}{1-(2+2n)D} V_{in} \\ v_{pn1} = v_{pn2} = \dfrac{1}{1-(2+2n)D} V_{in} \end{cases} \tag{5.4}$$

whereas, *n* is the turns ratio of the transformer which can also be utilized to obtain a higher voltage gain by increasing its turn ratio. Therefore, the output phase peak voltage $\widehat{v_{ph}}$ of the proposed inverter can be expressed as:

$$\widehat{v_{ph}} = \frac{M v_{pn}}{2} = M \frac{V_{in}}{1-(2+2n)D} \tag{5.5}$$

5.3 Interleaved Modulation Scheme for the Proposed Parallel Connected Inverter

One of the main benefits of paralleling inverters is interleaved switching. Interleaving of two inverters is achieved by employing a 180° phase shift between the two inverter bridges of the proposed circuit. The proposed inverter can be controlled using the same modulation schemes invented for original ZSI i.e. simple boost control, maximum boost control and constant boost control. However, a phase shift of 180° is employed between the triangular (carrier) waveforms V_{tri} of the two inverters as shown in Fig. 5.4. Simple boost control is applied to the proposed inverter. V_p and V_n are the two straight lines (envelops) that are used to define the shoot through state of the inverter, while v_a, v_b and v_c are the reference waveforms. V_{tri1} is the triangular (carrier) waveform of inverter 1. V_{tri2} is the carrier waveform of Inverter 2 which is phase shifted by 180 degrees with regards to Inverter 1.

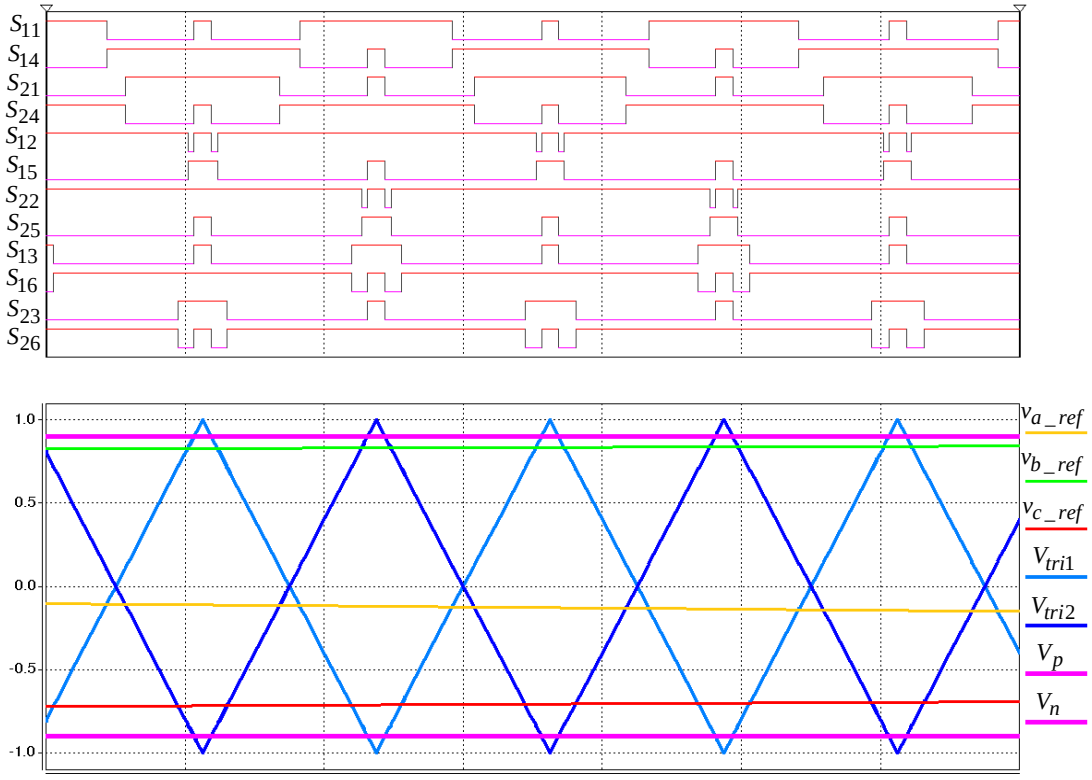


Fig. 5.4. Interleaved simple boost control of the proposed inverter

5.4 Extension of the Proposed Concept to N-parallel Connected Inverters

The proposed concept of paralleling two inverters can be extended to N-parallel connected improved ZSIs with magnetic coupling to increase the output voltage and voltage gains. It also improves the power rating of the whole system by sharing the stresses. Fig. 5.5 shows the basic structure of proposed N-parallel connected inverters.

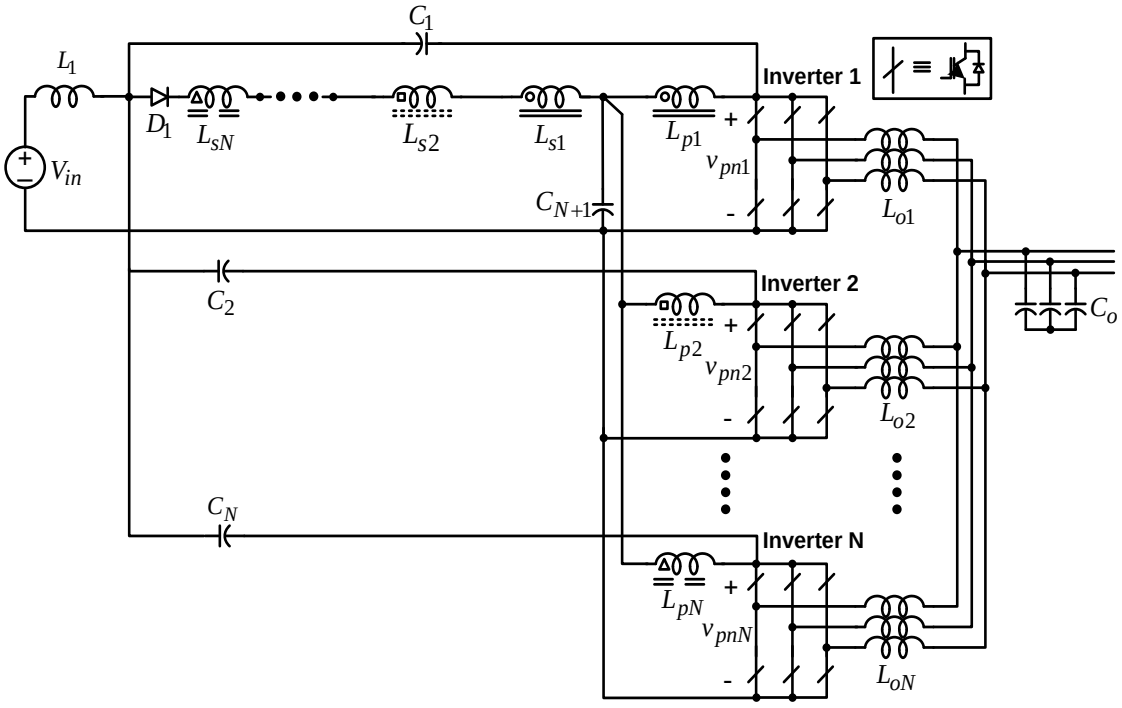


Fig. 5.5. Proposed N-parallel connected inverter

Similarly, the corresponding voltages across the capacitors and dc-link can be expressed as

$$\begin{cases} V_{cN} = \dfrac{(1+Nn)D}{1-(2+Nn)D} V_{in} \\ V_{cN+1} = \dfrac{1-D}{1-(2+Nn)D} V_{in} \\ v_{pnN} = \dfrac{1}{1-(2+Nn)D} V_{in} \end{cases} \tag{5.6}$$

In (5.6), the number of paralleled inverters is denoted by 'N', where 'n' is the turns ratio of the coupled inductor or transformer. Therefore, from equation (5.6) it can be seen that higher voltage gain be achieved by either increasing the turns ratio of the magnetic coupled component or by increasing the number of inverters paralleled. The gain of the proposed inverter can be expressed as:

$$G = MB = \frac{M}{1-(2+Nn)(1-M)} \tag{5.7}$$

Fig. 5.6 shows the plot of voltage gain vs. modulation index for different values of N. It clearly shows with the increment of no. of inverters paralleled a high voltage gain can be obtained while keeping modulation index higher resulting in improved power quality.

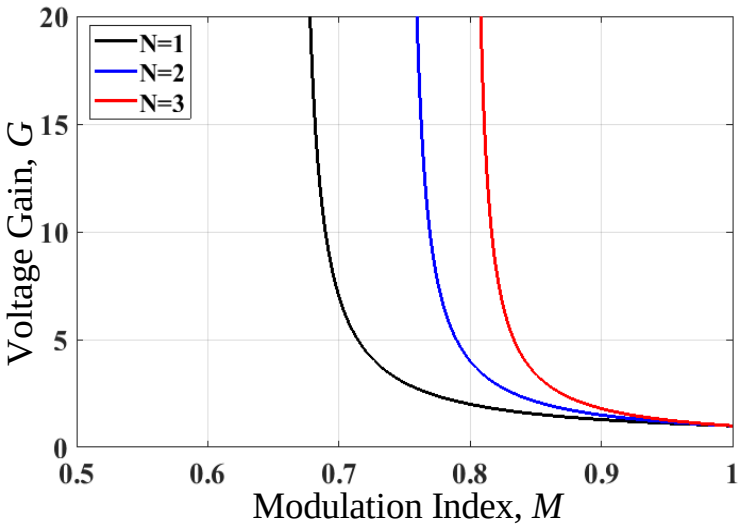


Fig. 5.6 Voltage gain vs. modulation index plot

Utilizing higher modulation index will also results in reduced switch stress across the inverter bridge thus improving the dynamic performance of the whole system. By reducing the ratings of the switching components will reduce the losses related to higher rating components. The switch voltage stress V_{sw} of the proposed inverter can be written as:

$$V_{sw} = \frac{G(2+Nn)-1}{Nn+1} V_{in} \tag{5.7}$$

Fig. 5.7 shows the voltage stress against voltage gain plot for the different values of *N*. It is noted that higher the number of inverters paralleled, lower the switch voltage stress across the inverter bridge.

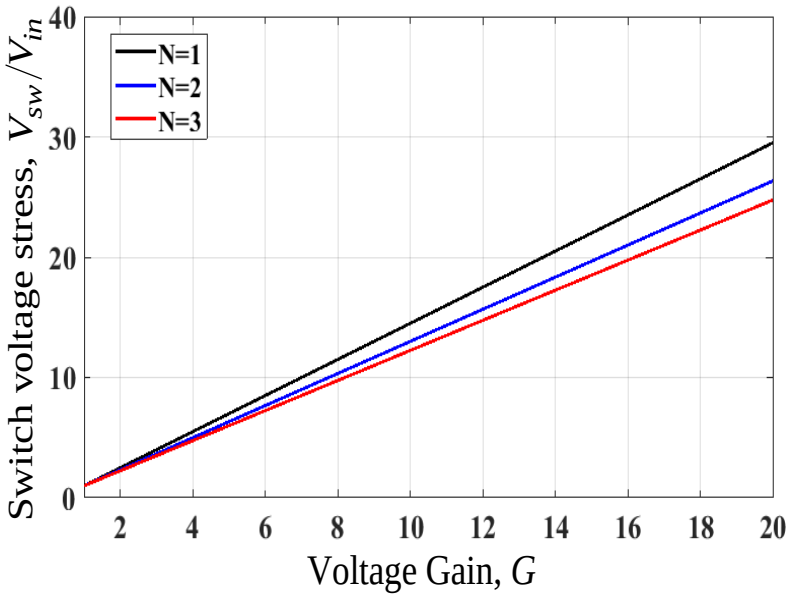


Fig. 5.7. Plot of voltage stress (normalized with input voltage) vs. voltage gain

These plots validate the numerous benefits (mentioned earlier) of paralleling impedance source inverters for improving the overall spectral performance of the power system.

5.5 Simulation Results

Detailed simulations are performed for the proposed parallel inverter to verify the aforementioned theoretical analysis and confirm the advantages. As explained in Section 5.3 the proposed inverter is controlled using simple boost scheme with phase shift of 180° for interleaved switching. The parameters for the simulations are as follows:

- Input voltage: $V_{in} = 240\ V$
- Output voltage: 220 V_{rms}
- Transformer (coupled inductor) turns ratio: $n_1 = n_2 = 1$
- Inductor: $L_1 = 500$ µH
- Z-source Capacitors: $C_1 = C_2 = C_3 = 100$ µF
- Modulation index: M = 0.9
- Switching frequency: $f_{sw} = 20$ kHz

Fig. 5.8 shows the simulation waveforms of proposed inverter output line to line voltage and input voltage. Fig. 5.9 (a) shows the dc-link voltages of the two inverter bridges connected in parallel. These are phase shifted by 180° to achieve the interleaving effect. Fig. 5.9(b) shows the capacitor voltages of the Z-source network that comply with the equations derived in (5.4). Fig. 5.10 shows the output filter inductor currents. With interleaving effect the ripple of the currents is reduced significantly.

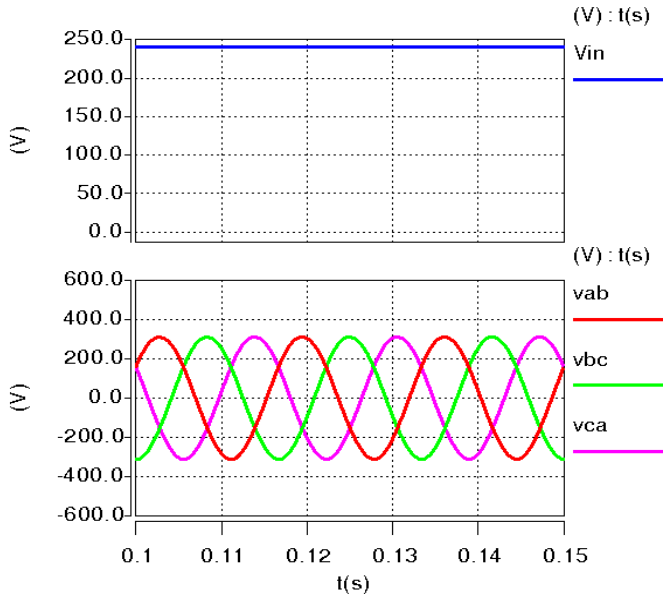
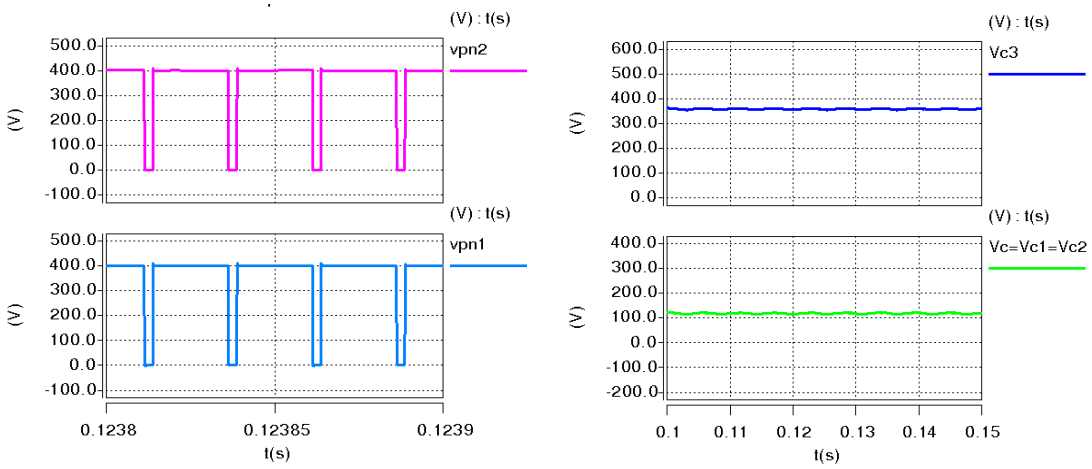


Fig. 5.8. Simulations results of the proposed parallel inverter output line-line voltage and input voltage



(a) (b)

Fig. 5.9. Simulation results (a) dc-link voltage (b) capacitor voltages

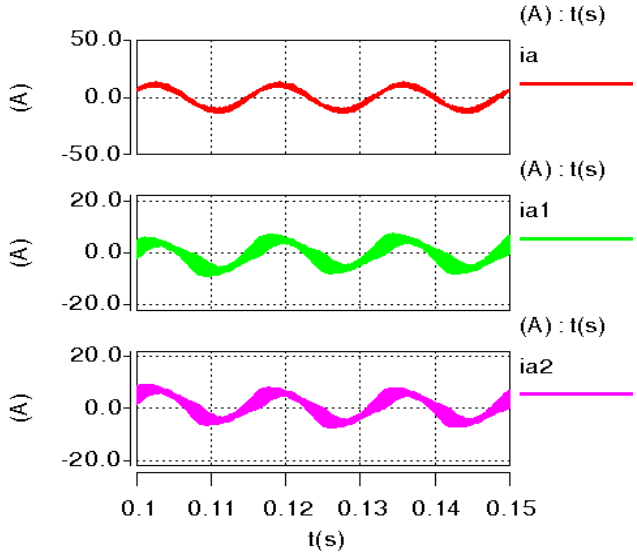


Fig. 5.10 Output filter inductor current simulation results

5.6 Prototyped Based Verification

A hardware prototype matching the circuit configuration ratings shown in Fig. 5.2 was built based on DSP kit TMS320528335 shown in Fig. 4.8. Table 5.1 shows the detailed specifications of the proposed inverter. The proposed inverter is controlled using the simple boost control scheme.

TABLE 5.1

Electrical Specifications

Output Power	7.2 kW
Input voltage	240 V
Output voltage	220 Vrms (line-line)
Switching frequency	20 kHz
Modulation index	0.9
Transformer (coupled inductor)	$L_{p1}, L_{s1}, L_{p2}, L_{s2} = 200\ \mu H$ $n = 1$
Capacitors (C_1, C_2, C_3)	100 μF
Output Inductors (L_o)	850 μH
Resistive load	20 Ω/phase

Interleaved switching mechanism is employed in the simple boost control as shown in Section 5.3. Fig. 5.11 shows the experimental waveforms of output line-line voltage and input voltage of the proposed inverter. Fig. 5.12 shows the waveforms of dc-link voltages of the inverter bridges and voltages across the capacitors. Fig. 5.13 shows the zoom in and out waveforms of output filter inductor currents with interleaving effect. Fig. 5.14 shows the hardware setup of the proposed two-paralleled improved magnetic coupled (MC) ZSI.

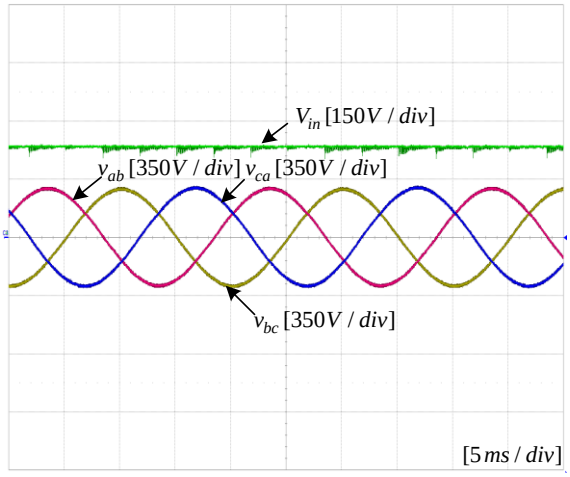
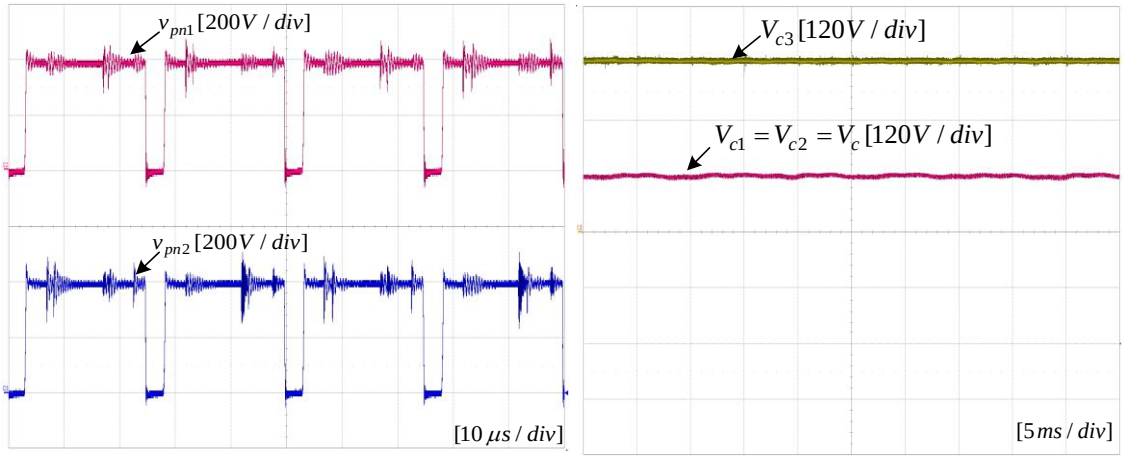
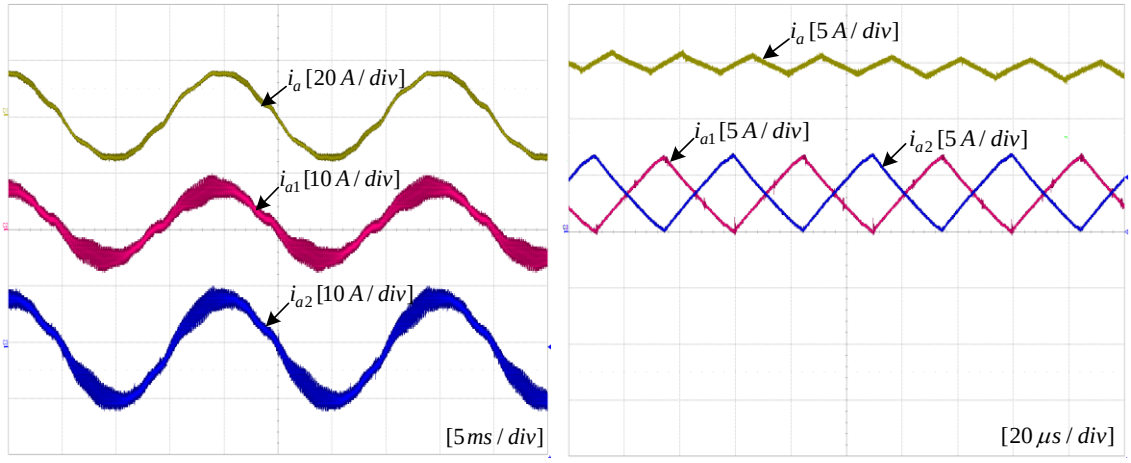


Fig. 5.11. Experiments of the proposed parallel inverter output line-line voltage $v_{LL\,peak} = 311\,V$, and input voltage $V_{in} = 240\,V$



(a) (b)

Fig. 5.12. Experimental results. (a) Dc-link voltage $v_{pn} = 400\,V$. (b) Capacitor voltages $V_{c1} = V_{c2} = V_c = 120\,V$, $V_{c3} = 360\,V$.



(a) (b)

Fig. 5.13 Output filter inductor current experiments. (a) Zoom-out mode (b) Zoom-in mode

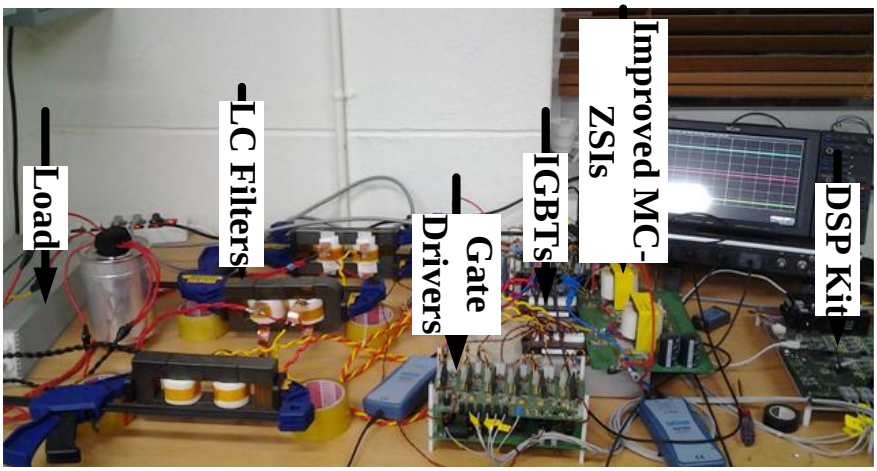
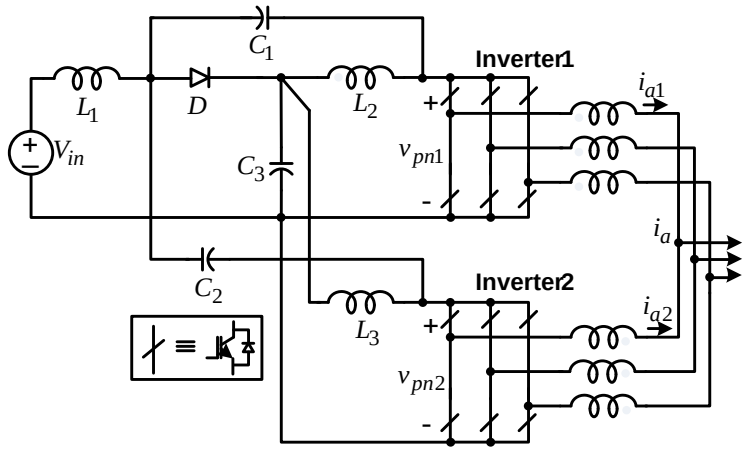


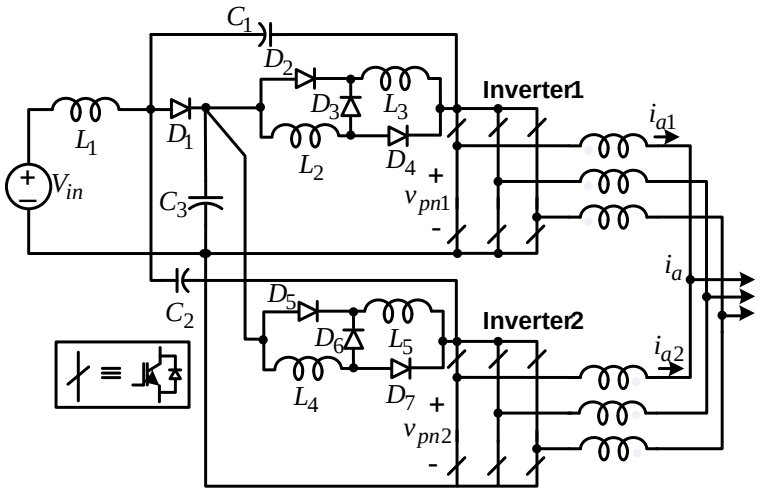
Fig. 5.14 Hardware prototype of parallel connected improved MC-ZSI

5.7 Extension of Paralleling Inverters Concept to Existing ZSIs

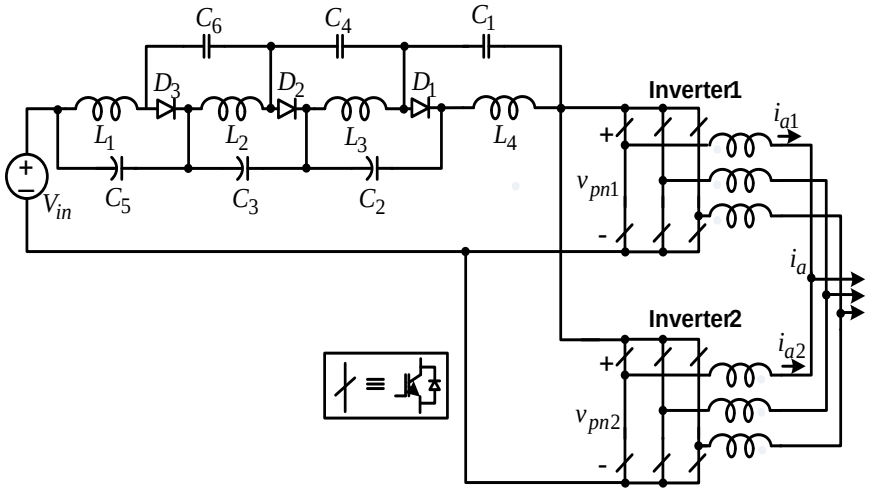
The main concept of parallel operation can be applied to other existing ZSIs to achieve the benefits of paralleling inverters as well as the advantages of Z-source structures. Fig. 5.15 (a) shows the parallel qZSI inverter derived from quasi-Z-source structure. Fig. 5.15(b) shows the paralleled version of switched inductor (SL) qZSI. Fig. 5.16 (c) and (d) shows the parallel connected capacitor assisted and diode assisted ZSIs. Fig. 5.16 (e) shows the parallel gamma ZSI derived from ΓZSI.


C1
L1
D
L2
Inverter1
ia1
Vin
C3
vpn1
ia
C2
Inverter2
ia2
L3
vpn2

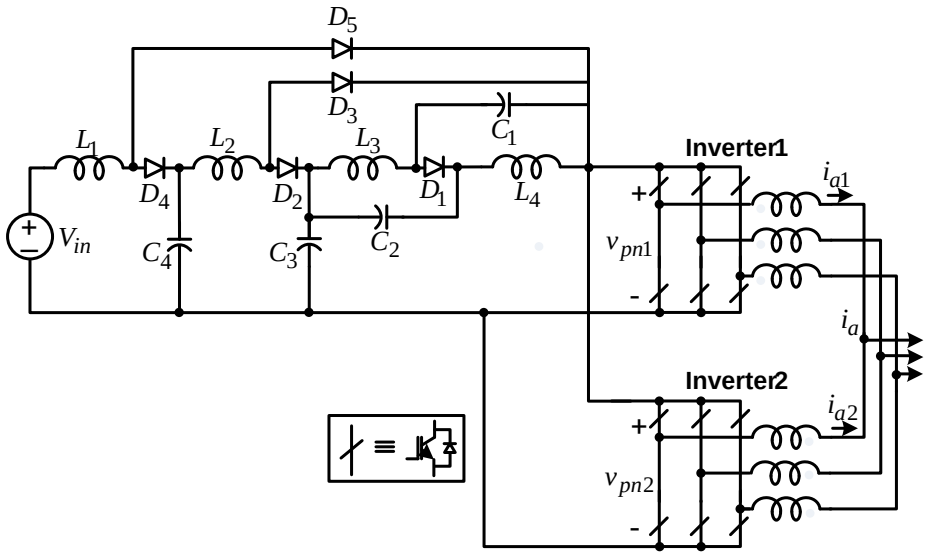
(a)


C1
D2
D3
L3
Inverter1
ia1
L1
D1
Vin
L2
D4
vpn1
C3
ia
D5
C2
Inverter2
D6
L5
ia2
L4
D7
vpn2

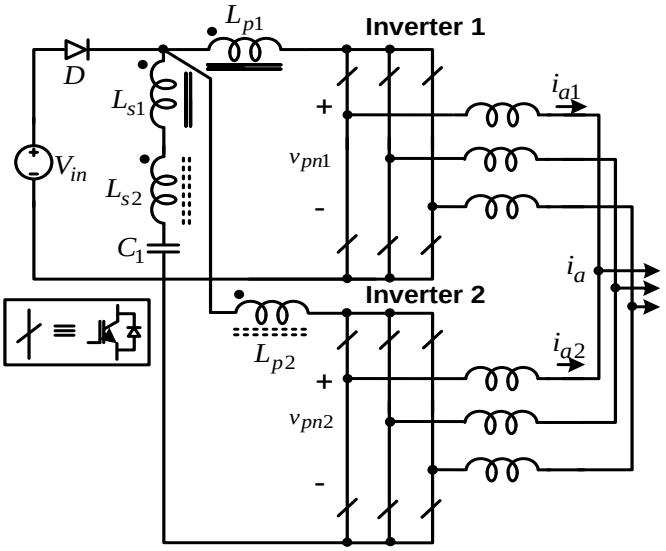
(b)


C6
C4
C1
D3
D2
D1
Inverter1
ia1
L1
L2
L3
L4
Vin
C5
C3
C2
vpn1
ia
Inverter2
ia2
vpn2

(c)



(d)



(e)

Fig. 5.15 Proposed parallel inverters. (a) qZS (b) SL-qZS (c) Capacitor assisted (d) Diode assisted (e) ΓZS version.

5.8 Conclusions

In this chapter the design for the parallel connected improved ZSI with magnetic coupling is proposed and analysed in detail. The main features of the proposed inverter can be summarized as:

- The proposed inverter can achieve a high voltage gain either by increasing the number of inverters paralleled or by increasing the turns ratio of the transformer (coupled inductor).
- The proposed inverter retains all the existing characteristics of Z-source inverters such as immunity to open and short circuits, resilient to EMI noise and increased reliability.
- The proposed inverter has all the benefits of modular inverters that can be realized as ease of maintenance, thermal relieving, (N+1) redundancy, shared stress and modularity.
- The interleaving effect reduces the current ripples reducing the output filter requirements.

A high power 2 parallel connected inverter is built and tested successfully. The proposed concept can be applied to MW power systems such as distributed generation systems (fuel cells, wind, etc.), or to a power station with multi-generator units by increasing the number of inverters in parallel with low input dc voltage to achieve very high power with improved modularity.

6. Chapter 6
Single-Phase Z-Source AC-AC Converters Based on Transformers

6.1 Introduction

In industrial applications, the classical approach for AC-AC power conversions is to utilize AC thyristor power controllers which implements the phase angle or integral cycle control on input ac voltage to meet the output demands [72-73]. However, due to severe shortcomings associated with these AC thyristor controllers which are low power factor, high total harmonic distortion (THD) in the source current and low efficiency, are reinstated by pulse width modulation (PWM) AC controllers [74-75]. These controllers have features like better power factor and good efficiency with relatively smaller input-output filter requirements. However, for industrial applications where only voltage regulation is desired, the direct PWM AC-AC converters are utilized due to the following features; low harmonic current in line, single-stage conversion, smaller size, lower cost, and realization of better power factor and efficiency. These direct PWM AC-AC converters are derived from DC-DC topologies in which the unidirectional switches are replaced with the bidirectional switches [76-79]. The AC-AC converters can also achieve conditioning, isolating and filtering of the inflowing power in addition to the voltage regulation.

A family of single-phase direct PWM AC-AC converters is presented in [81]. These include simple topologies like buck, boost, buck-boost, and cuk converters. However, each of these simple topologies have its own imperfections and limitations such as the AC output voltage is limited below and cannot exceed the input voltage in buck converter

while boost converter cannot step down the input voltage. Whereas, buck-boost and cuk converters can provide both step up/down functions with reversible phase angle at the expense of higher switch voltage stresses and there are discontinuous input and output currents for the former converter. The multi-cell/level step-down converters [82] can subdue the switch voltage stress and improve the output voltage quality. However, they need additional balancing circuits like RLC boosters are required and to be connected in parallel with load to reduce the voltage imbalance problem of the flying capacitors.

Recently, the Z-source network applied to DC-AC power conversion has also been applied to AC-AC converters. The work on AC-AC converters utilizing Z-source structures has been focused on single phase and three phase topologies [32-38, 83-85]. Single phase Z-source AC-AC converter (ZSAC) can perform buck-boost operations with reversing and maintaining phase angle. The basic structure of single phase ZSAC is shown in Fig. 6.1.

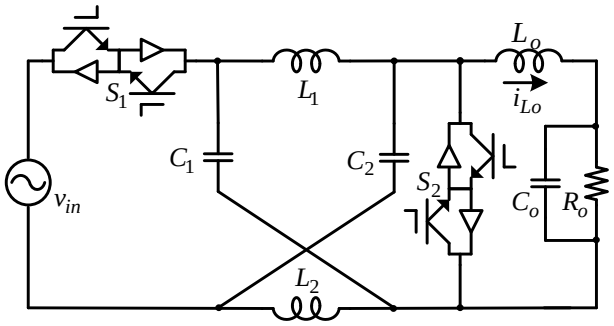


Fig. 6.1. Single-phase Z-source AC-AC converter.

The boost factor of ZSAC is expressed as:

$$B = \frac{1 - D}{1 - 2D} \tag{6.1}$$

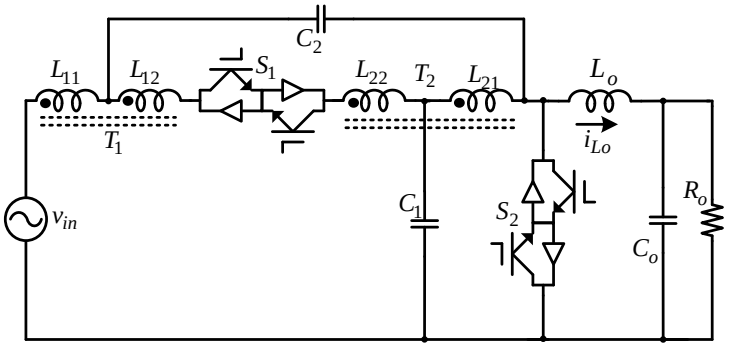
However, it has some significant drawbacks such as input and output do not share the common ground, so the feature of output maintaining or reversing the phase angle with input is not supported well, the input current is operated in the discontinuous current mode, and a small snubber circuit is required to limit the voltage spikes and to provide commutation paths during the dead times. This results in unreliability and poor efficiency.

Therefore, this chapter proposes a new class of Z-source AC-AC converters based on transformers with different configurations. The proposed converters replaces the inductors in the Z-source network with transformers and it obtains higher boost factor by tuning the turns ratio (n) of transformers compared to conventional ZSAC. The commutation strategy for the proposed converters is also presented to achieve soft commutation and eliminates the voltage and current spikes caused by short/open circuits during overlap and dead times.

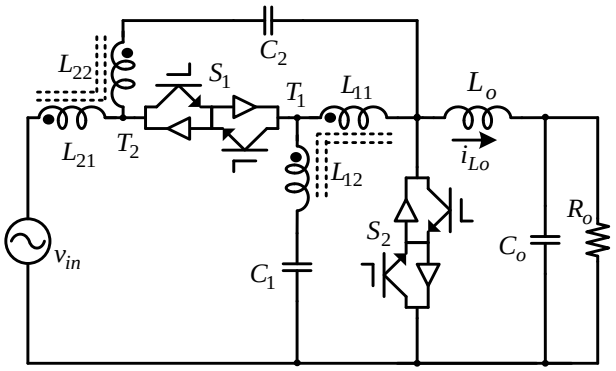
6.2 Proposed Transformer based Z-Source Converters

Fig. 6.2(a) and (b) shows the basic configurations of the proposed converters with different transformer placements resulting in different outcomes. In common, they replaces the two inductors in the conventional Z-source ac-ac converter with two transformers. The main characteristics of the proposed converters are as follows:

1) It retains all the features of conventional ZSAC.
2) It provides a large range of output voltage with buck-boost function.
3) The voltage gain can be adjusted by tuning (either increasing or decreasing depending on the configuration) the turns ratio of the transformer thus giving more freedom in adjusting the gain in terms of n and D.
4) It has continuous input current, improved input profiles and reduces the input current THD.
5) It has shared common ground thus the feature of maintaining and reversing the phase angle is supported well. 6) It has improved reliability and better power factor.



(a)



(b)

Fig. 6.2. ZS AC-AC converters based on transformers (a) configuration 1 (b) configuration 2

Fig. 6.3 shows the basic control strategy of the switches without considering the commutation problem. In general, a saw-tooth V_{saw} waveform is compared with the reference waveform V_{ref} to generate the PWM signals, whenever the saw-tooth waveform exceeds the reference line the converter goes into shoot-through state i.e. switch S_2 is turned on to allow buck-boost function of the converter.

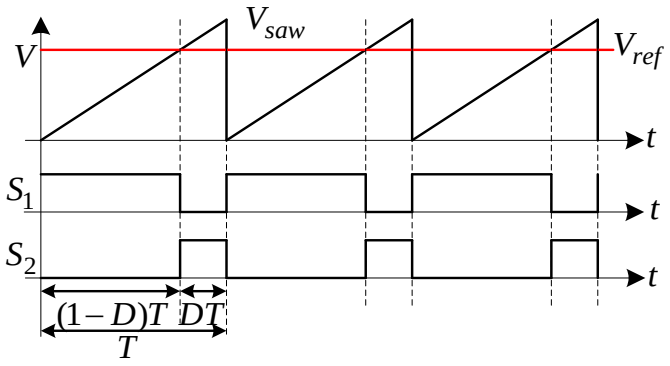


Fig. 6.3. Ideal PWM switching signals of the proposed converters.

6.2.1 Circuit Analysis of Configuration 1

Fig. 6.2 (a) shows the proposed Z-source AC-AC converter based on transformers with configuration 1. In this configuration, the capacitors C_1 and C_2 are connected between the primary and secondary windings of transformers t_1 and t_2 forming two T structures mirroring each other. With this configuration, an increase in the turns ratio of the transformers results in higher voltage gain. The following assumption is assumed for the

circuit analysis of the proposed converter that all the capacitors and switches are ideal and lossless. Like the conventional ZSAC converter the proposed converter has two operational states generally named as shoot-through and non-shoot-through states as shown in Fig. 6.4.

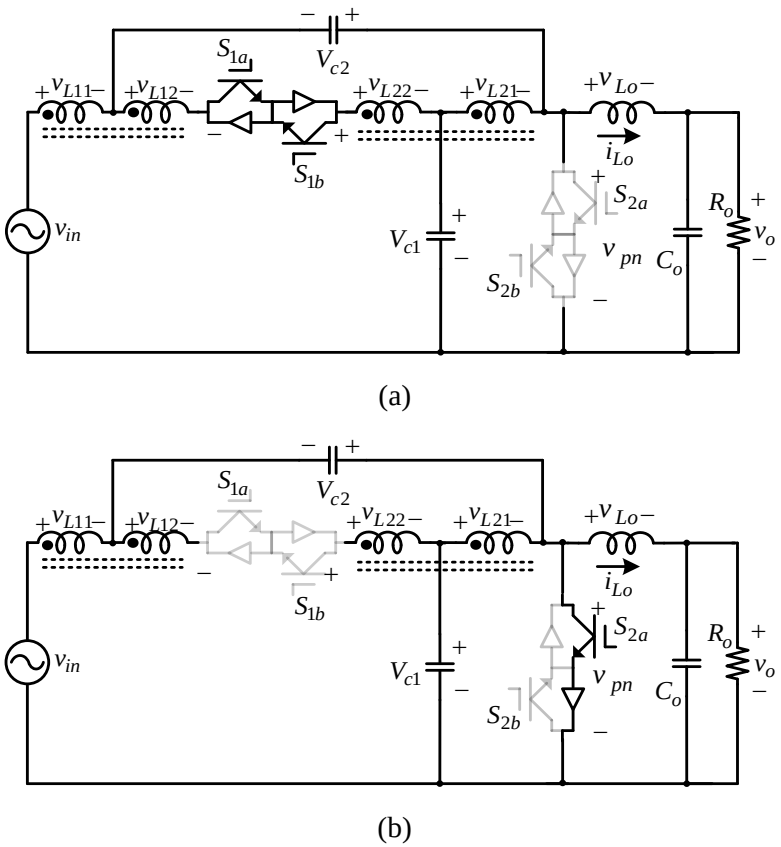


Fig. 6.4. Equivalent circuits (a) Non-shoot-through state (b) Shoot-through state

During the non-shoot-through interval as shown in fig. 6.4(a) the switch S_1 is turned on and switch S_2 is turned off and the energy stored in the windings is transferred to the load. The corresponding voltages across the transformers primary and secondary windings are named as $v_{L11_{non}}, v_{L12_{non}}, v_{L21_{non}}$, and $v_{L22_{non}}$. Thus by application of Kirchhoff's voltage law we obtain:

$$\begin{cases} v_{L11_{non}} = v_{in} - v_{L12_{non}} - v_{L22_{non}} - V_{c1} \\ v_{L21_{non}} = -v_{L22_{non}} - v_{12_{non}} - V_{c2} \\ -V_{c1} + v_{L21_{non}} + v_{pn} = 0 \\ v_{Lo_{non}} = v_{pn} - v_o \end{cases} \tag{6.2}$$

Similarly, during the shoot-through interval the switch S_1 is turned off and switch S_2 is tuned on as shown in fig. 6.4(b) and therefore the voltage v_{pn} is zero in this mode. Thus by applying KVL across the equivalent circuit in the fig. 6.4(b) yields:

$$\begin{cases} v_{L11_{sh}} = v_{in} + V_{c2} \\ v_{L12_{sh}} = n_1 v_{L11_{sh}} \\ V_{c1} = v_{L21_{sh}} \\ v_{L22_{sh}} = n_2 v_{L21_{sh}} \\ v_{Lo} = -v_o \end{cases} \tag{6.3}$$

Whereas, n_1 is the turns ratio of transformer T_1 and n_2 is the turns ratio of transformer T_2. By applying flux balance condition across the transformers primary and secondary windings we get:

$$\begin{cases} v_{L11_{non}} = \dfrac{-D}{1-D}(v_{in} + V_{c2}) \\ v_{L12_{non}} = \dfrac{-n_1 D}{1-D}(v_{in} + V_{c2}) \\ v_{L21_{non}} = \dfrac{-D}{1-D}(V_{c1}) \\ v_{L22_{non}} = \dfrac{-n_2 D}{1-D}(V_{c1}) \end{cases} \tag{6.4}$$

Substituting (6.4) into (6.2) reveals:

$$\begin{cases} V_{c1} = \dfrac{1-D}{1-(2+n_1+n_2)D}(v_{in}) \\ V_{c2} = \dfrac{(1+n_1+n_2)D}{1-(2+n_1+n_2)D}(v_{in}) \\ v_{pn} = \dfrac{1}{1-(2+n_1+n_2)D}(v_{in}) \end{cases} \tag{6.5}$$

By applying volt-sec balance condition across the L_o, the voltage gain of the proposed converter is defined as

$$v_o = \frac{1-D}{1-(2+n_1+n_2)D}(v_{in}) \tag{6.6}$$

Fig. 6.5 shows the voltage gain $G(v_o/v_{in})$ versus duty cycle graph for the proposed converter. From the plot it can be inferred that when $n_1 + n_2 = 0$ the transformers

secondary windings are eliminated then the proposed converter behaves like a classical ZSAC [73]. When $n_1 + n_2 > 1$ the proposed converter produces a very high gain compared to conventional ZSAC. This feature allows the proposed converter to has wide range of gain control due to the use of transformers.

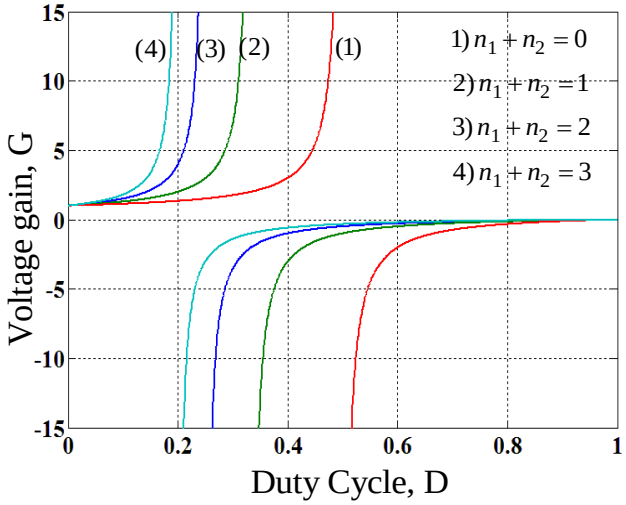


Fig. 6.5. Plot of voltage gain versus duty cycle of the proposed configuration 1 converter with variable turns ratio.

6.2.2 Circuit Analysis of Configuration 2

The second configuration proposed Z-source AC-AC converter based on transformers is shown in fig. 6.2(b), whose capacitors and transformers form two mirrored Γ shapes. As compared to the previous circuit, with this configuration the proposed converter has its voltage gain raised by lowering the turns ratio of the transformers with the same number of components. The desired output voltage can be tuned by varying the turns ratio of transformers with in the narrow range of $1 < n \leq 2$. Like the previous circuit, this converter also has two operating modes shown in fig. 6.6(a) and (b).

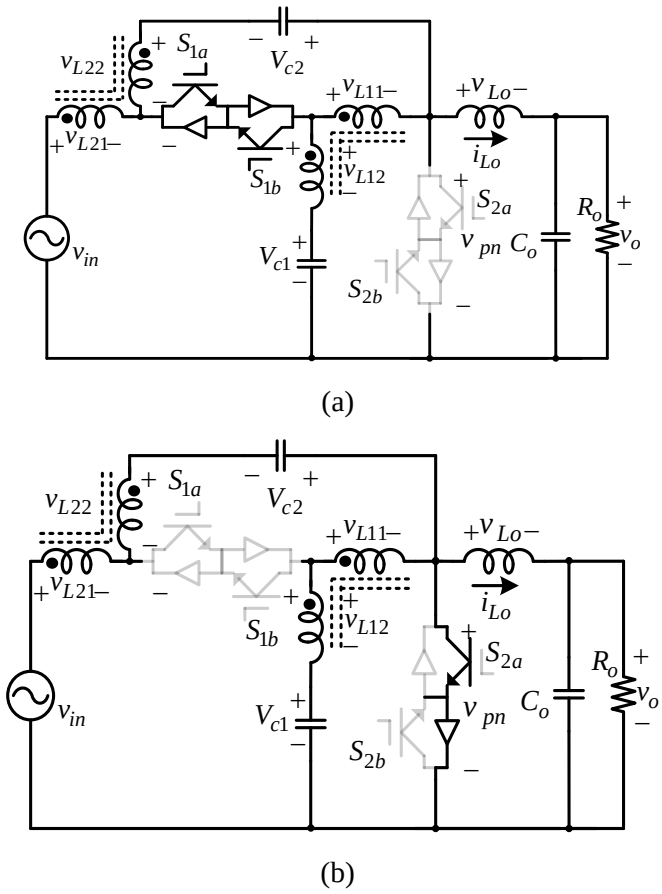


Fig. 6.6. Equivalent circuits (a) Non-shoot-through state (b) Shoot-through state

The operating mode during the non-shoot-through interval is shown in fig. 6.6(a) in which the switch S_1 is turned on and S_2 is turned off. The corresponding voltages across the transformers primary and secondary windings are named as $v_{L11_{non}}, v_{L12_{non}}, v_{L21_{non}}$, and $v_{L22_{non}}$. Thus, KVL yields:

$$\begin{cases} v_{L11_{non}} = -v_{L22_{non}} - V_{c2} \\ v_{L21_{non}} = v_{in} - v_{L12_{non}} - V_{c1} \\ -v_{in} + v_{L21_{non}} - V_{c2} - v_{L2_{non}} + v_{pn} = 0 \\ v_{Lo_{non}} = v_{pn} - v_o \end{cases} \tag{6.7}$$

Similarly, by applying KVL during the shoot-through interval shown in fig. 6.6(b) reveals:

$$\begin{cases} v_{L11_{sh}} = V_{c1} + v_{L21_{sh}} \\ v_{L11_{sh}} = n_1 v_{L12_{sh}} \\ v_{L21_{sh}} = v_{in} + v_{L22_{sh}} + V_{c2} \\ v_{L21_{sh}} = n_2 v_{L22_{sh}} \\ v_{Lo} = -v_o \end{cases} \tag{6.8}$$

Whereas, n_1 and n_2 are the turns ratio of transformer T_1 and transformer T_2. By applying volt-sec balance condition across the transformers we get:

$$\begin{cases} v_{L11_{non}} = \dfrac{-n_1 D V_{c1}}{(1-D)(n_1-1)} \\ v_{L12_{non}} = \dfrac{-D V_{c1}}{(1-D)(n_1-1)} \\ v_{L21_{non}} = \dfrac{-n_2 D (v_{in} + V_{c2})}{(1-D)(n_2-1)} \\ v_{L22_{non}} = \dfrac{-D (v_{in} + V_{c2})}{(1-D)(n_2-1)} \end{cases} \tag{6.9}$$

Substituting (6.9) into (6.7) and by solving we get:

$$\begin{cases} V_{c1} = \dfrac{1-D}{1-(2+(1/n_1-1)+(1/n_2-1))D}(v_{in}) \\ V_{c2} = \dfrac{(n_1 n_2 - 1)(D v_{in})/(n_1-1)(n_2-1)}{1-(2+(1/n_1-1)+(1/n_2-1))D} \\ v_{pn} = \dfrac{v_{in}}{1-\left(2+\left(1/n_1-1\right)+\left(1/n_2-1\right)\right)D} \end{cases} \tag{6.10}$$

Thus, the voltage gain of the 2nd proposed converter can be found by applying the flux balance condition across the output inductor L_o as:

$$v_o = \frac{1-D}{1-(2+(1/n_1-1)+(1/n_2-1))D}(v_{in}) \tag{6.11}$$

The plot of voltage gain $G(v_o/v_{in})$ versus duty cycle graph for the proposed 2nd configuration converter is shown in fig 6.7. Fig. 6.7 clearly shows that with the decrement in the turns ratio of the transformers, the voltage gain starts increasing.

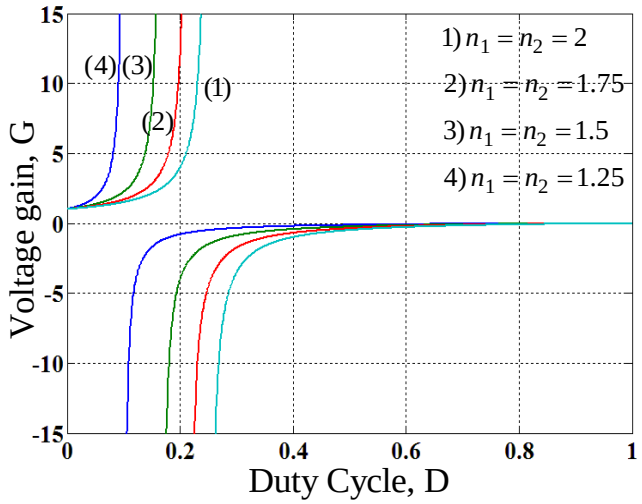


Fig. 6.7. Plot of voltage gain versus duty cycle of the proposed configuration 2 converter with variable turns ratio.

6.3 Commutation Study

Both of the proposed converters discussed in Sections 6.2.1 & 6.2.2 contains two bidirectional switches S_1 and S_2, which are realized by connecting two IGBTs with anti-parallel diodes in back- to-back common emitter configuration. Generally, the switches S_1 and S_2 are complementary to each other as shown in Fig. 6.3. In ideal case they are turned on and off without any dead or overlap time. However, practically due to time delays and limited speed of switches there exists a short overlap or dead time between the switching devices. Therefore, sudden changes occurs in capacitor voltages and inductor currents during these overlap and dead times resulting in current and voltage spikes. Traditionally, to prevent the voltage and current spikes dead time is induced in the switching with extra snubber circuits across the IGBTs to avoid the voltage overshoots [84]. These additional snubbers increase complexity, hardware cost and reduce the efficiency of the power converters. Hence, in order to eliminate these lossy and bulky snubbers, a soft commutation strategy is utilized for the proposed converters which provides path for the inductor currents during dead times to remove the voltage spikes across the switching devices [86].

Fig. 6.8 illustrates the soft commutation PWM switching strategy for the proposed family of converters for both in-phase and out-of-phase modes. For every half cycle of input voltage, one switch from each bidirectional switch pair is modulated at high frequency while the rest of the switches are completely turned on for the commutation purposes. For explanatory purposes boost in-phase mode is considered and proposed converter with 2nd configuration is used as an example, when $v_{in} > 0$ switches S_{1b} and S_{2a} are modulated complementary at high frequency with small dead time to prevent the short circuit problem. Switches S_{1a} and S_{2b} are completely turned on to avoid the commutation problem and provide continuous current path during the dead times.

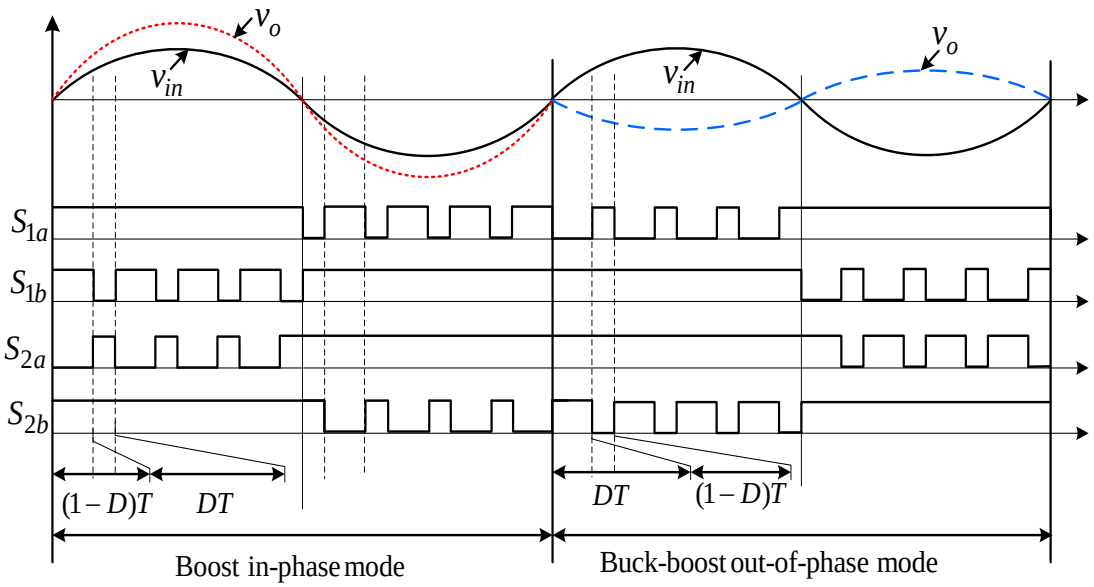


Fig. 6.8. Switching pattern with soft-commutation strategy for the proposed family of converters.

Fig. 6.9 shows the operating states in the in-phase mode when $v_{in} > 0$. During the non-shoot-through state as shown in fig. 6.9(a) switch S_{1a} is on and conducts positive input current, while switch S_{1b} conducts if the current flows from load to source. Switch S_{2b} is turned only for commutation purposes whereas it does not conduct current.

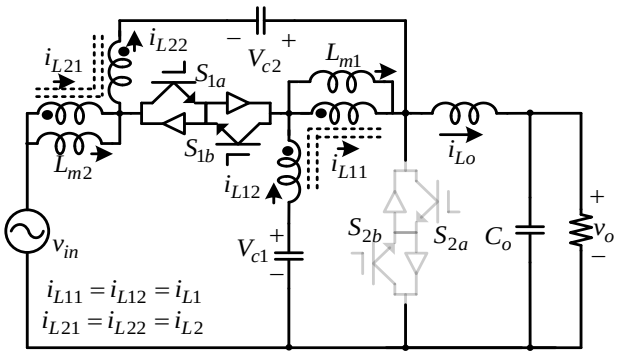
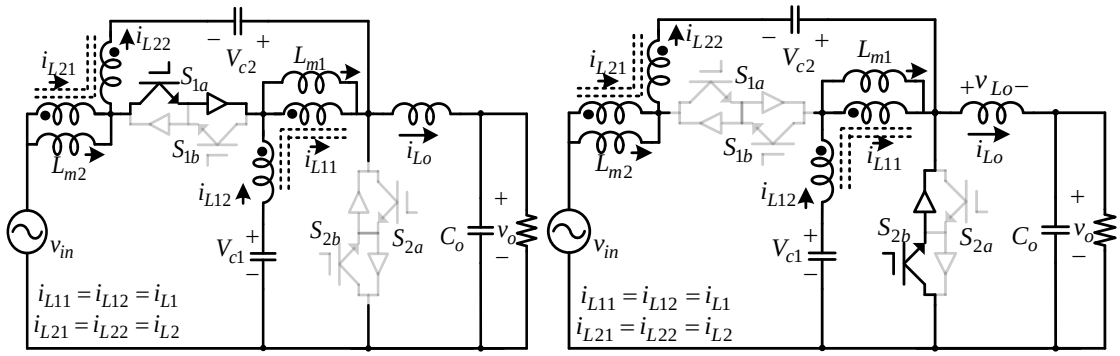


Fig. 6.9. Operation state of the proposed converter in boost in-phase mode when $v_{in} > 0$. (a) Non-shoot-through state.

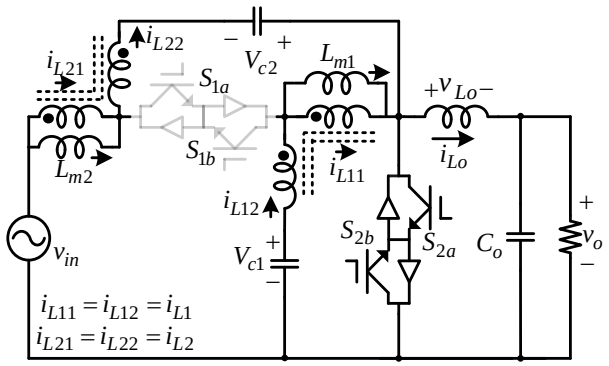
At the end of the non-shoot-through state, switch S_{1b} is turned off while switch S_{2a} has not yet turned on due to the presence of dead time, there exists two commutation states. State 1 as shown in fig. 6.9(b): when $i_{L1} + i_{L2} > i_{Lo}$ the current flows along switch S_{1a} while switch S_{2b} do not conduct current. State 2 as shown in fig. 6.9(c): when $i_{L1} + i_{L2} < i_{Lo}$ the current flows through switch S_{2b} whereas switch S_{1a} do not conduct current.



(b) (c)

Fig. 6.9. Operation states of the proposed converter in boost in-phase mode when $v_{in} > 0$. (b) Commutation state when $i_{L1} + i_{L2} > i_{Lo}$. (c) Commutation state when $i_{L1} + i_{L2} < i_{Lo}$.

After dead time, shoot-through state occurs as shown in fig. 6.9(d). In this state, S_{1a} do not conducts current and is turned on only for commutation purposes, while switch S_{2a} conducts current from source towards load and switch S_{2b} conducts only if the current flows from load towards source (negative direction). In this way the current is always continuous regardless of the current direction, thus eliminating the switch voltage spikes. Similarly, with $v_{in} < 0$ same analysis can be performed.



(d)

Fig. 6.9. Operation state of the proposed converter in boost in-phase mode when $v_{in} > 0$. (d) Shoot-through state.

The switching pattern for the buck and boost out-of-phase mode is shown in fig. 6.8. In out-of-phase mode with $v_{in} > 0$ the switches S_{1a} and S_{2b} are complementary modulated at high frequency while switches S_{1b} and S_{2a} are completely tuned on to provide commutation paths. Likewise, when $v_{in} < 0$ switches S_{1a} and S_{2b} are fully turned on for commutation basis while switches S_{1b} and S_{2a} are complementary modulated at high frequency with a small dead time.

Table 6.1 summarizes all the switching states with soft-commutation for the proposed converters. Table 6.2 provides the summary of the voltage stresses for the proposed family of ZSAC based on transformers.

TABLE 6.1

Switching Sequences

Mode	v_{in}	Switch "on" states			
		Non-shoot-through		Shoot-through	
		Active	Commutation	Active	Commutation
Boost in-phase	>0	S_{1a}, S_{1b}	S_{2b}	S_{2a}, S_{2b}	S_{1a}
	<0	S_{1a}, S_{1b}	S_{2a}	S_{2a}, S_{2b}	S_{1b}
Buck-boost out-of-phase	>0	S_{1a}, S_{1b}	S_{2a}	S_{2a}, S_{2b}	S_{1b}
	<0	S_{1a}, S_{1b}	S_{2b}	S_{2a}, S_{2b}	S_{1a}

TABLE 6.2

Summary of Voltage Stresses

	Configuration 1, Fig. 6.2(a)	Configuration 2, Fig. 6.2(b)
V_{c1}	$\frac{(1-D)v_{in}}{1-(2+n_1+n_2)D}$	$\frac{(1-D)v_{in}}{1-\left(2+(\frac{1}{n_1-1})+(\frac{1}{n_2-1})\right)D}$
V_{c2}	$\frac{(1+n_1+n_2)Dv_{in}}{1-(2+n_1+n_2)D}$	$\frac{\frac{(n_1n_2-1)(D)v_{in}}{(n_1-1)(n_2-1)}}{1-\left(2+(\frac{1}{n_1-1})+(\frac{1}{n_2-1})\right)D}$
v_{pn}	$\frac{v_{in}}{1-(2+n_1+n_2)D}$	$\frac{v_{in}}{1-\left(2+(\frac{1}{n_1-1})+(\frac{1}{n_2-1})\right)D}$
v_o	$\frac{(1-D)v_{in}}{1-(2+n_1+n_2)D}$	$\frac{(1-D)v_{in}}{1-\left(2+(\frac{1}{n_1-1})+(\frac{1}{n_2-1})\right)D}$

6.4 Simulation Results

Saber simulations are performed for the proposed class of Z-source AC-AC converters based on transformers to validate the aforementioned theoretical analysis. Circuit configuration 1 and circuit configuration 2 will be validated through simulations in Sections 6.4.1 & 6.4.2 followed up with experiments of circuit configuration 2 in Section 6.5 to confirm the working principle and benefits mentioned in earlier sections. Simulation models of circuit configurations 1 & 2 with testing points are shown in Appendix D.

6.4.1 Simulation Results of Circuit Configuration 1

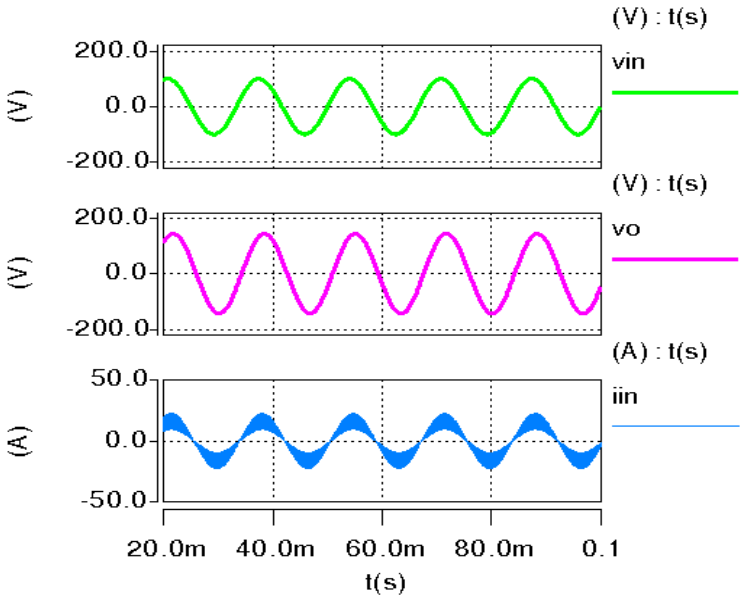
The main parameters selected for the simulations of the proposed 1st configuration circuit are shown in Table 6.3.

TABLE 6.3

Electrical Specifications

Output voltage	110 Vrms
Input voltage (boost mode)	100 V, 70 V
Input voltage (buck mode)	200 V
Switching frequency	25 kHz
Shoot-through duty cycle	0.1, 0.43
Transformer (coupled inductor)	$n_1 = 1, 2$ $n_2 = 1, 2$
Capacitors (C_1, C_2)	6.8 μF
Output inductor (L_o)	800 μH
Output capacitor (C_o)	4.5 μH

Fig. 6.10 shows the simulations of input voltage, input current and output voltage for the proposed configuration circuit 1 in buck/boost out-of-phase and in-phase modes. Fig. 6.10 (a) shows the waveforms of input voltage, output voltage and input current with transformer turns ratio $n_1 = n_2 = 1$ in boost mode. Fig. 6.10 (b) shows the capacitor voltage and v_{pn} voltage waveforms. Fig. 6.10 (c) shows the waveforms of output current, input voltage and output voltage with turns ratio $n_1 = n_2 = 2$. Fig. 6.10 (c) clearly shows the increment of output voltage with increased turns ratio while keeping the same duty ratio. Fig 6.10 (d) shows the voltage waveforms of v_{pn} and capacitors C_1 and C_2 with turns ratio $n_1 = n_2 = 2$. Fig. 6.11 shows the waveforms of proposed configuration circuit 1 in buck out-of-phase mode with transformer turns ratio $n_1 = n_2 = 1$. Fig. 6.11 (a) shows the input voltage, current and output voltage while Fig. 6.11 (b) shows the waveforms of capacitor C_1, C_2 voltages and v_{pn}.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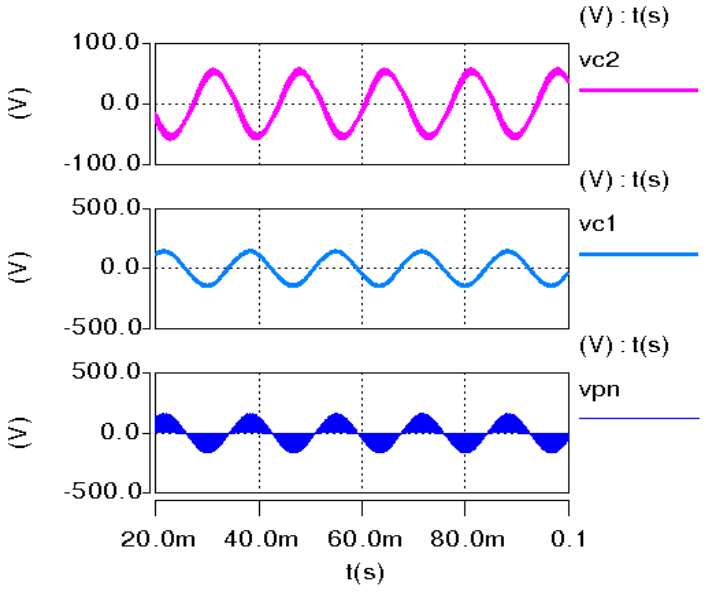
vin
200.0
0.0
-200.0
(V)
(V) : t(s)
vo
200.0
0.0
-200.0
(V)
(A) : t(s)
iin
50.0
0.0
-50.0
(A)
20.0m
40.0m
60.0m
80.0m
0.1
t(s)

(a)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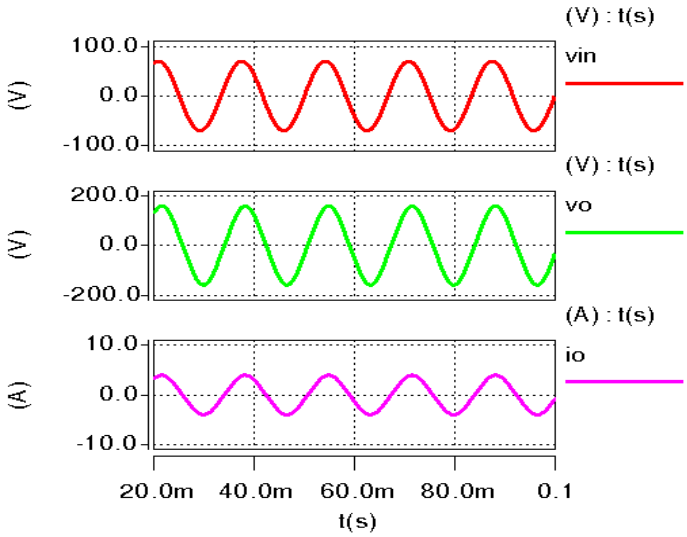
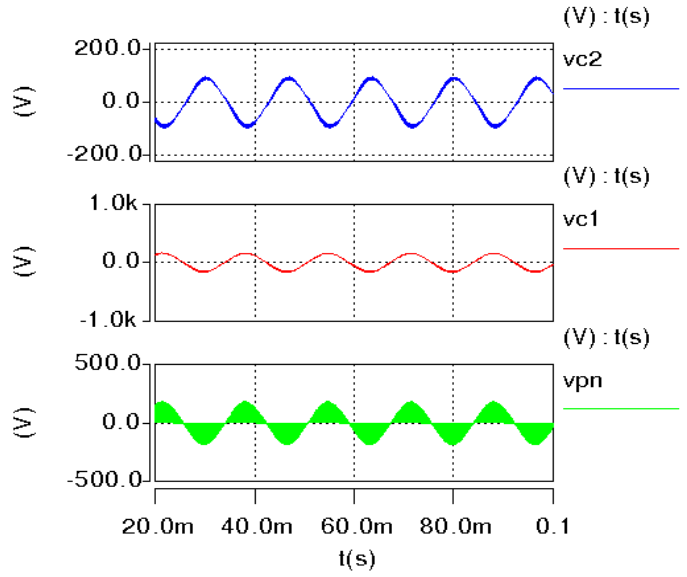
0.0
-100.0
(V)
(V) : t(s)
vc1
500.0
0.0
-500.0
(V)
(V) : t(s)
vpn
500.0
0.0
-500.0
(V)
20.0m
40.0m
60.0m
80.0m
0.1
t(s)

(b)

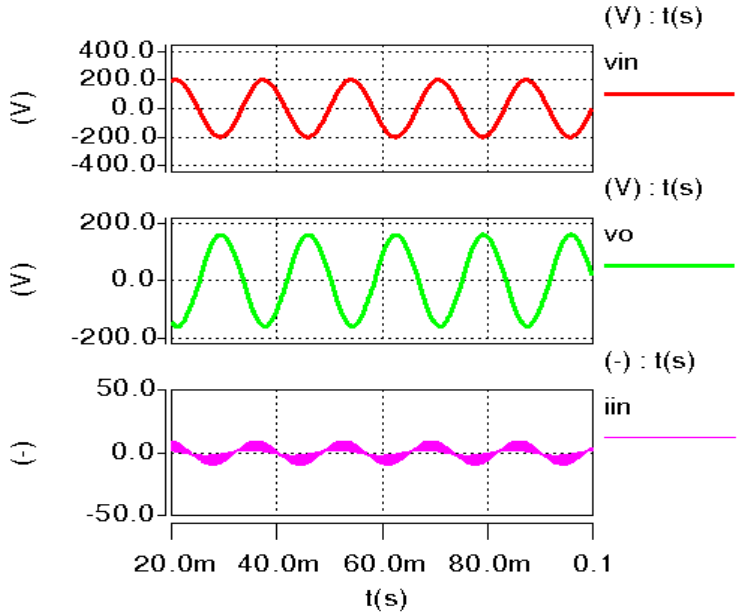


(c)

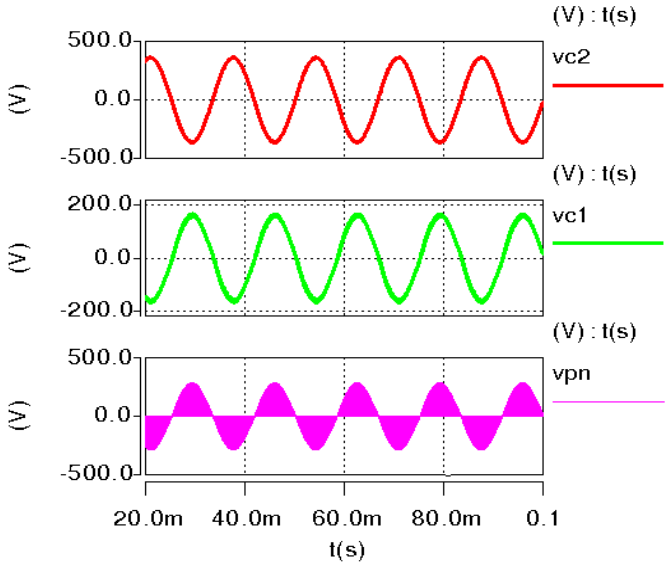


(d)

Fig. 6.10. Simulation results in boost mode. (a) $n_1 = n_2 = 1$, $v_{in} = 100\,V$ (b) $v_{c1} \approx 155\,V$, $v_{c2} \approx 50\,V$, $v_{pn} \approx 166.6\,V$ (c) $n_1 = n_2 = 2$, $v_{in} = 70\,V$. (d) $v_{c1} \approx 155\,V$, $v_{c2} \approx 125\,V$,$v_{pn} \approx 175\,V$.



(a)



(b)

Fig. 6.11. Simulation results in buck mode. (a) $n_1 = n_2 = 1$, $v_{in} = 200\,V$ (b) $v_{c1} \approx 155\,V$, $v_{c2} \approx 358\,V$, $v_{pn} \approx 278\,V$

6.4.2 Simulation Results of Circuit Configuration 2

The main parameters selected for the simulations of proposed 2nd configuration circuit are shown in Table 6.4. Almost all the parameters selected are same with 1st configuration

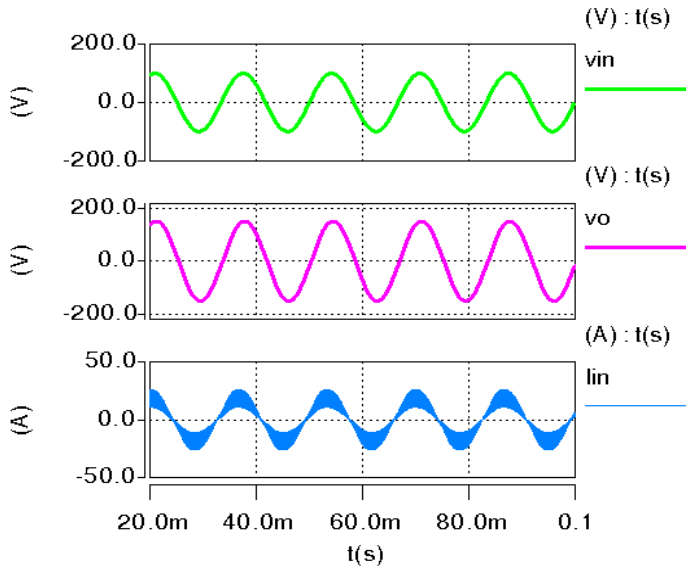
circuit except for turns ratio of the transformer and input voltage due to different gain properties.

TABLE 6.4

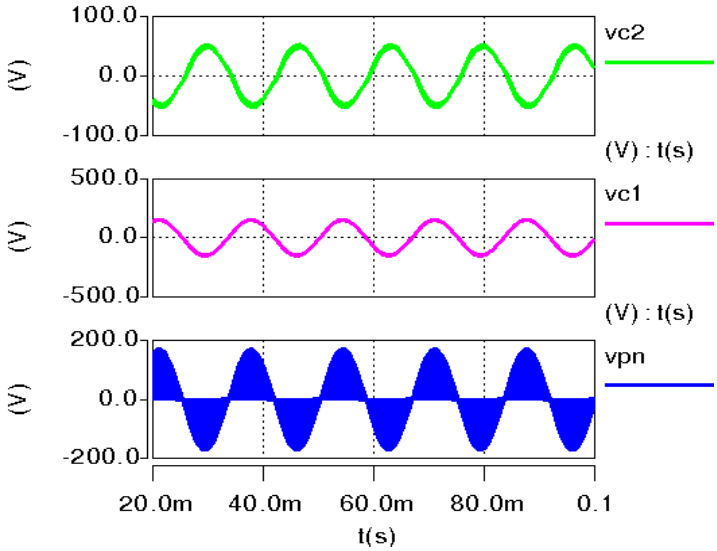
Electrical Specifications

Output voltage	110 Vrms
Input voltage (boost mode)	100 V, 50 V
Input voltage (buck mode)	200 V
Switching frequency	25 kHz
Shoot-through duty cycle	0.1, 0.43
Transformer (coupled inductor)	$n_1 = 2, 1.41$ $n_2 = 2, 1.41$
Capacitors (C_1, C_2)	6.8 μF
Output inductor (L_o)	800 μH
Output capacitor (C_o)	4.5 μH

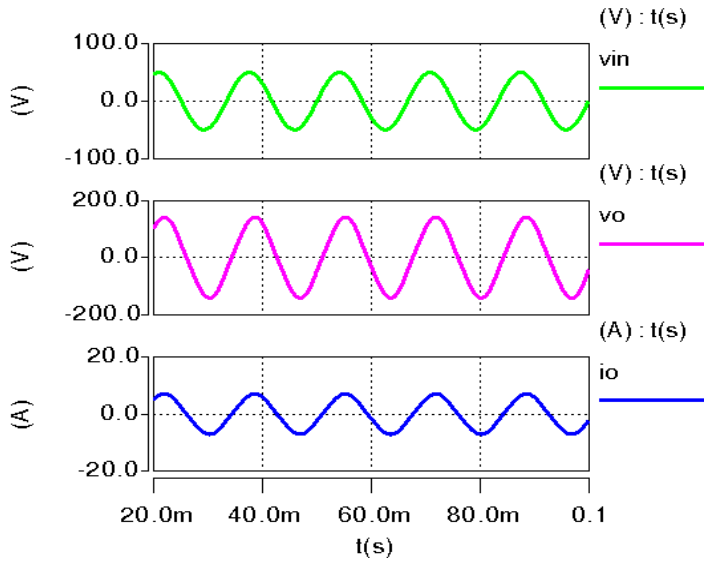
Fig. 6.12 shows the simulations of input voltage, input current and output voltage for the proposed configuration circuit 2 in buck/boost out-of-phase and in-phase modes. This configured circuit can increase voltage gain by decreasing the turns ratio rather than increasing it. Fig. 6.12(a) shows the waveforms of input voltage, output voltage and input current with transformer turns ratio $n_1 = n_2 = 2$ in boost mode. Fig. 6.12(b) shows the waveforms of the voltage across the capacitors and v_{pn}. Fig. 6.12(c) shows the waveforms of output current, voltage and output voltage with turns ratio $n_1 = n_2 = 1.41$. Fig. 6.12(c) clearly shows the increment of output voltage with decreased turns ratio with the same duty ratio. Fig. 6.12(d) shows the waveform of v_{pn}. Fig. 6.13 shows the waveforms of proposed configuration circuit 2 in buck out-of-phase mode with transformer turns ratio $n_1 = n_2 = 2$. Fig. 6.13(a) shows the input voltage, current and output voltage while Fig. 6.13(b) shows the waveforms of capacitor C_1, C_2 voltages and v_{pn}.


(V) : t(s)
vin
200.0
0.0
-200.0
(V)
(V) : t(s)
vo
200.0
0.0
-200.0
(V)
(A) : t(s)
lin
50.0
0.0
-50.0
(A)
20.0m
40.0m
60.0m
80.0m
0.1
t(s)

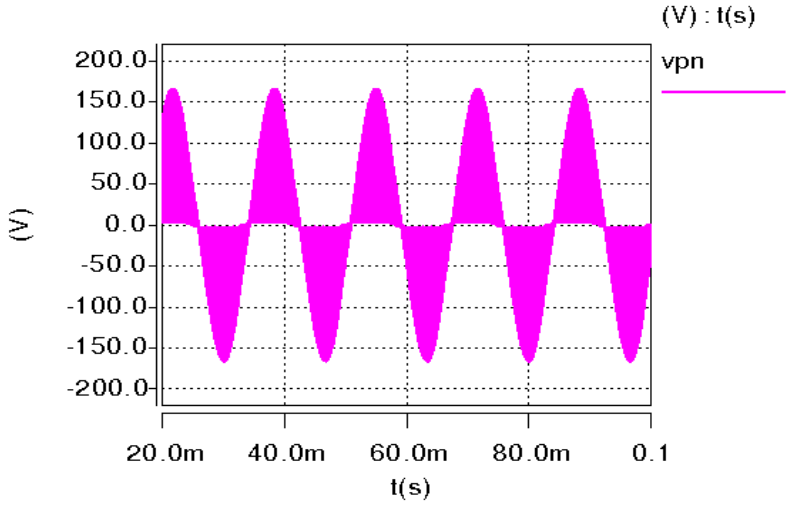
(a)


vc2
100.0
0.0
-100.0
(V)
(V) : t(s)
vc1
500.0
0.0
-500.0
(V)
(V) : t(s)
vpn
200.0
0.0
-200.0
(V)
20.0m
40.0m
60.0m
80.0m
0.1
t(s)

(b)

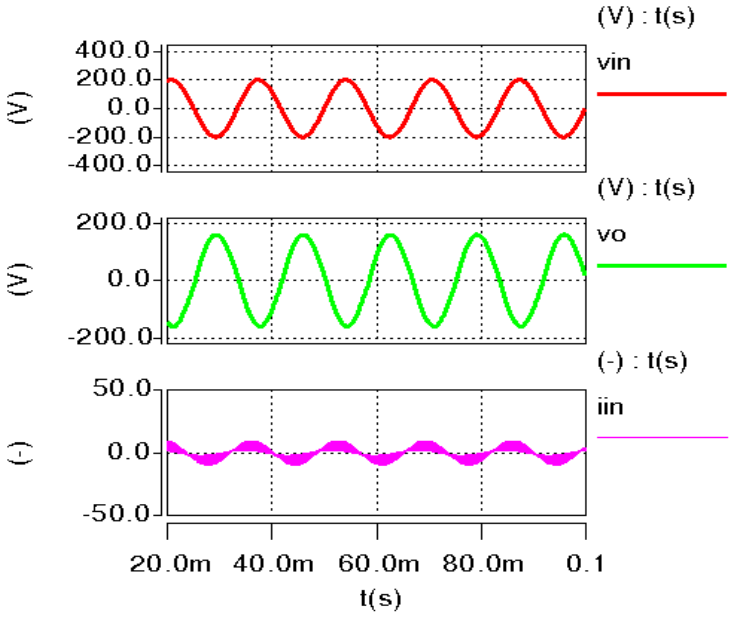


(c)

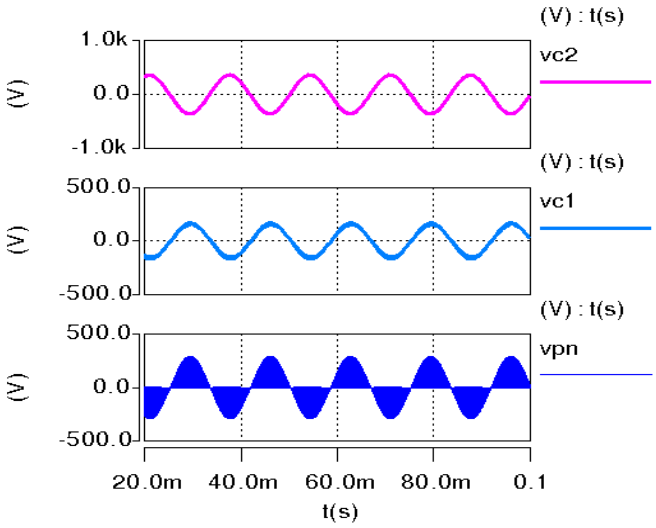


(d)

Fig. 6.12. Simulation results in boost mode. (a) $n_1 = n_2 = 2,\ v_{in} = 100\,V$ (b) $v_{c1} \approx 155\,V$, $v_{c2} \approx 50\,V$, $v_{pn} \approx 165\,V$ (c) $n_1 = n_2 = 1.41$, $v_{in} = 54\,V$. (d) $v_{pn} \approx 165\,V$.



(a)



(b)

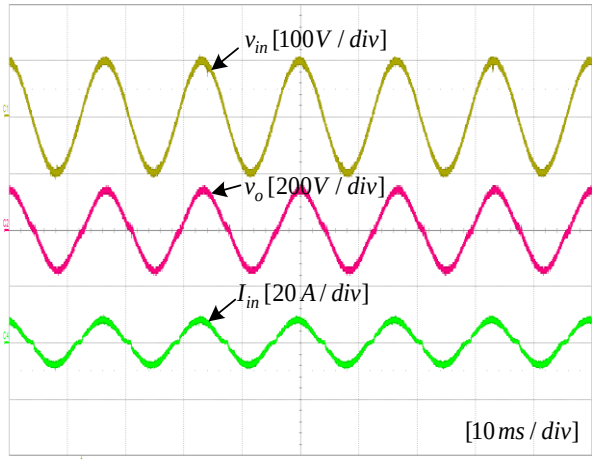
Fig. 6.13. Simulation results in buck mode. (a) $n_1 = n_2 = 2$, $v_{in} = 200\,V$ (b) $v_{c1} \approx 155\,V$, $v_{c2} \approx 358\,V$, $v_{pn} \approx 278\,V$

Therefore, from the above simulation results, all the values comply with the theoretical derivations mentioned in Table 6.2.

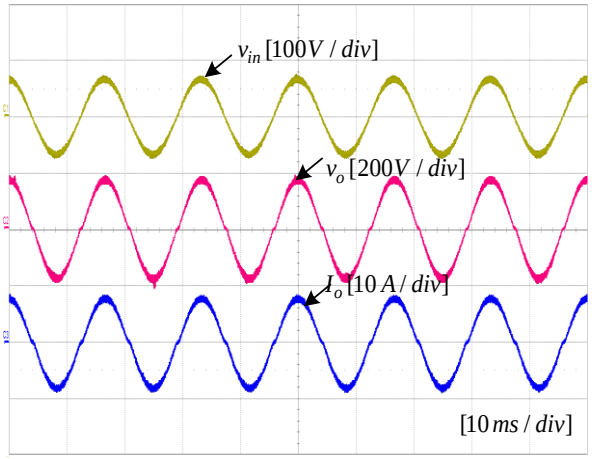
6.5 Experimental Verifications

To experimentally verify the working of the proposed class of Z-source AC-AC converters a laboratory prototype of the 2nd configuration was fabricated and tested. The electrical specifications are kept same as in simulations. Commutation strategy is employed using a voltage transducer LEM LV 25-P and DSP kit based on TMS320f28335.

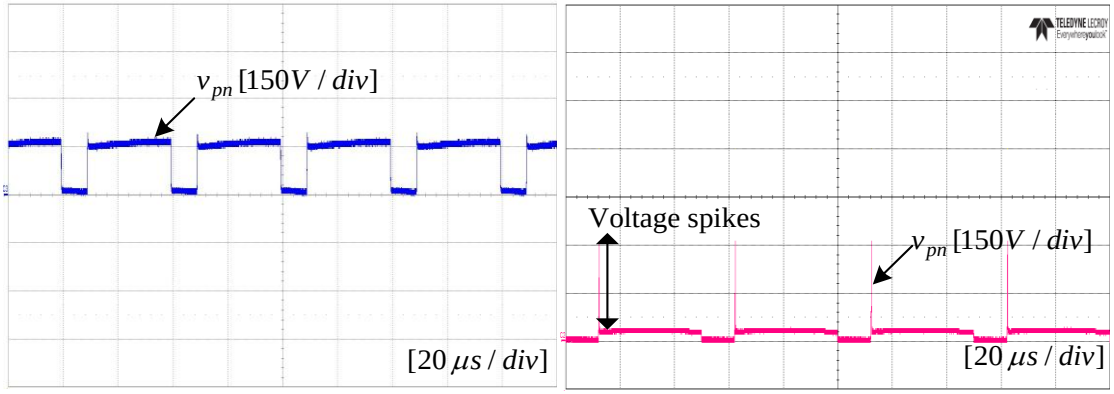
Fig. 6.14 shows the experimental results of the 2nd configuration in boost mode. Fig. 6.14 (a) shows the output voltage, input voltage and input current waveforms with turns ratio $n_1 = n_2 = 2$. Fig. 6.14 (b) shows the output voltage, input voltage and output current waveforms with turns ratio $n_1 = n_2 = 1.41$. Fig. 6.14 (c) and (d) shows the expanded waveforms of v_{pn} with and without commutation strategy which clearly shows the benefits of proposed commutation strategy that are reduced voltage spikes without the need of extra clamp circuits. Fig. 6.15 shows the experimental waveforms of the proposed 2nd configuration circuit in buck out of phase mode.



(a)



(b)



(c) (d)

Fig. 6.14. Experimental results in boost mode. (a) $n_1 = n_2 = 2$, $v_{in} = 100\ V$ (b) $n_1 = n_2 = 1.41$, $v_{in} = 50\ V$. (d) $v_{pn} \approx 165\ V$.

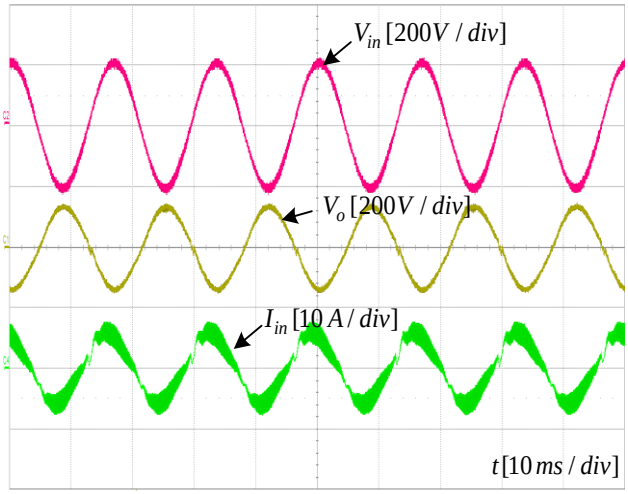


Fig. 6.15. Experimental results in buck mode.

6.6 Conclusions

In this chapter a new family of single phase, transformer-based AC-AC Z-source converters is proposed. The proposed converters inherit all the benefits of existing ZSAC converters which are buck-boost, maintaining, or reversing the phase angle, and improved reliability. Additionally, both the proposed converters have different transformers placement configurations that leads to achieving different characteristics as follows:

- Transformer with configuration 1 obtains a high voltage gain by increasing the number of turns. So in order to achieve a high gain larger turns ratio is required or alternatively a high duty cycle can be used.
- Transformer with configuration 2 obtains a high gain by decreasing the turns ratio of the magnetic component rather than increasing it. It can achieve a very high gain by a minimal difference between the primary and secondary windings. Therefore, careful consideration is required while selecting the number of turns of the transformer

Moreover, both the converters have some similar features as follows:

- The proposed converter(s) have shared grounds.
- The proposed converter(s) have improved input profiles.
- They have reduced inrush current, thus eliminates the need for additional LC filter at the input side.
- The proposed converter(s) regulates the output voltage by either adjusting the turns ratio of the transformers or by adjusting duty cycle which gives more freedom in modifying the gain in terms of D and n.

These aforementioned features of the proposed converters makes it a good choice in solid state transformer and DVR applications. It can be used to compensate voltage sags and swells in ac-ac line conditioning.

Experimental results show the working and merits of the proposed configurations. It shows the reduction of voltage spikes that can greatly increase the reliability of the switches.

7. Chapter 7 Conclusions and Recommendations

7.1 Overview of the Thesis

Impedance source network became a research hotspot and have been widely used in power conversion applications due to its numerous features. Despite its huge demand, the shortcomings associated with conventional ZSI approaches cannot be ignored. These shortcomings greatly limit its applications and lower the efficiency of the power system. Therefore, a deep study of ZSIs with strong and reliable modifications have to be made to improve the overall effectiveness of the power system for industrial, commercial and domestic use. The main objective was to propose an advanced impedance source topology which can cater the drawbacks face with conventional ZSI approach and provide a valuable solution for these limitations as discussed in Chapter 1 and 2.

The findings from this thesis provide valuable insight into impedance source power systems. The contributions made are presented in each chapter of the thesis. Specific attention was given to the development of improved ΓZSI with clamping diode and the employment of high frequency isolation and parallel techniques by overcoming challenges in the conventional Z-source power inverters. This was achieved by conducting detailed analysis of the previous topologies in Chapter 1 and Chapter 2. To aid in the analysis of the proposed inverter circuits experimentation were developed in Sections 3.7, 4.5, 5.6 and 6.5. The models were tailored to accommodate healthy and faulted conditions while minimizing complexity and error. Implementation of advanced and new modulation techniques with soft commutation strategies were also implemented and tested in Sections 4.3, 5.3 and 6.3. In the end, new transformer-based Z-source AC-AC converters are also proposed and verified through simulations and experiments in Chapter 6.

A summary of the significant issues explored and findings in the thesis are given below:

- In chapter 1, discussed brief background of original ZSI is discussed. Problem statement is identified and the road map of research plan with aims and objectives to carry out the thesis are elaborated.
- In chapter 2, a comprehensive review of ZSIs is presented and its modulation strategies are elaborated. The main pros and cons of existing ZSIs are discussed in detail.
- In chapter 3, a new and improved ΓZSI with clamping diode is proposed and analyzed in detail. It has improved voltage gains, lower voltage stresses, and improved output quality as compared to existing topologies.
- Chapter 4 proposed a new class of high frequency isolated ZSIs. It employs a high frequency transformer between the inverter bridge and the output side. It eliminates the need for bulky line transformer and reduces the overall size of the system. It also avoids the injection of dc circulating current into the grid thus fulfilling the safety standards of the power system.
- In chapter 5, parallel connected ZSIs are proposed and magnetically coupled ZSI is considered in detail. Paralleling of inverters have many benefits including (N+1) redundancy, ease of maintenance, thermal management, lower stress, with the added benefits of increased voltage gain, expandability and interleaving. By increasing the number of inverters paralleled much higher output power can be achieved without overloading single inverters.
- Chapter 6 investigates a new class of Z-source AC-AC converters based on transformers with soft commutation strategy. These converters gives more freedom in adjusting the voltage gain in terms of duty cycle and turns ratio. Additionally, soft commutation strategy removes the need for extra clamp circuits resulting in reduced overall size and cost of the power converter system.

All of the inverters proposed and discussed in this thesis are validated through experimental hardware prototypes and simulation models at the end. Moreover, comparisons involving simulations and experimental studies have been made to confirm the merits and demerits of each proposed topology over existing ones.

7.2 Important Findings

This section lists the main findings and deals with the research queries that are reported in Section 1.4. It summarizes the significant contributions made in the thesis in the form of specific questions.

1. How the power losses and efficiencies will be calculated?

Section 3.8 shows the method adopted to calculate the efficiency and power losses of the proposed improved ΓZSI. The proposed improved ΓZSI can achieve upto 91% efficiency at high power. The proposed improved ΓZSI have higher efficiency than existing topologies due to utilization of high modulation index and low rated switching devices resulting in fast dynamics and lower cost.

2. What methods are applied to improve the voltage gain of the proposed inverters?

In ZSIs, many researcher have focused on developing new modulation schemes and Z-source structures to improve the voltage gain of the inverters which would rather increase the complexity of the system or increase the size due to addition of several components in the system as discussed in chapter 2 in detail. The proposed improved ΓZSI only adds one inductor and capacitor to obtain high gain compared to existing topologies with same modulation index, shoot-through duty cycle, turn ratio and input voltage.

3. How will the voltage clamping technique be applied to the proposed inverters?

In other transformer-based Z-source topologies, the energy stored in the leakage inductance of the transformer produces voltage spikes across the inverter bridge. These voltage spikes leads to the utilization of high voltage rating switching devices resulting in high cost and more switching and conduction losses. Thus the efficiency of the inverter is greatly reduced.

However, the proposed improved ΓZSI inverter employs a clamping diode in the circuit which forms a new high frequency loop comprising of C_2-D_2-C_1. As a result, the dc-link voltage is clamped to (V_{c1}+ V_{c2}), thus eliminating the voltage spikes across the inverter bridge. Thus, it can utilize a low rated switching device which can have almost

three to four times lower switching and conduction losses and can achieve a significantly high efficiency as discussed in section 3.8.

4. How should the dc circulating current be controlled in isolated impedance source inverters?

One of the major concerns in existing ZSIs is that when they are used as grid-tied inverters in PV systems, a DC current is injected in the grid which may cause saturation of the distribution transformer as well as poor power quality, higher loss, and overheating of the power system. The proposed high frequency transformer with small DC blocking capacitor avoids the injection of DC circulating current and meets the safety standards of IEEE. Moreover, it provides galvanic isolation and eliminates the need for bulky line transformer resulting in lower cost and size of the whole power system as discussed in chapter 4 in detail.

5. What control methods are applicable for the proposed isolated structures?

All of the existing modulation and control schemes proposed for the single-phase H-bridge ZSIs can be applied to the proposed high frequency isolated inverter with slight modification to control the bidirectional switch at the output side. In the thesis, simple boost control is applied to validate the working of the proposed isolated systems as shown in section 4.3.

6. How the interleaving mechanism is implemented in the existing modulation strategies of parallel operated impedance source inverters?

One of the main benefits of parallel operated inverter is interleaved switching leading to lower output filter requirements which results in reduced size and cost of the overall system. In this thesis, the interleaving mechanism is implemented in simple boost control scheme by employing a phase shift of 180° between the two inverter bridges of the parallel operated proposed inverter as shown in section 5.3 in detail.

7.3 Recommendations and Future Work

The original impedance source network has added a new trend in the field of power electronics and provides a unique solution to overcome the barriers and limitations faced by traditional voltage source and current source inverters. The concept of impedance network can be applied to entire spectrum of power electronic conversion (AC-AC, DC-DC, DC-AC, and AC-DC). The exemplary performance of impedance network attracts researchers and engineers from both academia and industry to explore its depth for various applications including renewable energy systems and power distribution systems. This thesis has proposed and analyzed an improved structure of ΓZSI that enhances upon the conventional ZSI design in many aspects and eliminates the shortcomings faced with traditional inverters and basic ZSI as well as other impedance source topologies that are reported in the literature. The system designed in the thesis is focused towards renewable energy systems specifically for PV systems as explained in Chapter 1 section 1.2. The scope of this thesis can be extended to other renewable energy systems, uninterruptable power supply applications and distributed generation systems. Moreover, the platform used in the thesis as mentioned in Section 3.7.1 is based on DSP kit TMS320F28335 and the modulation strategy implemented is simple boost control. This leaves an area to be explored in terms of different platform selections such as dSPACE Ace kit and employment of different control & modulation strategies i.e. maximum boost control, constant boost control, maximum constant boost control with third harmonic injection that can report some interesting results and findings.

Additionally, in terms of thesis work, the HFT isolated ZSIs experimental work conducted in this thesis was done on only improved Γ-Z-Source inverter. Not all the inverters proposed in chapter 4 are verified experimentally. It is possible to further the research by designing other isolated ZSIs and perform testing. Moreover, some further work is also recommended for the increment in number of parallel connected inverters to increase the output power up to MW. The circuits reported in Section 5.7 can also be analyzed and experimented on to report their important features and characteristics in detail. Furthermore, the configuration circuit 1 in chapter 6 can also be deigned with same

electrical parameters as of configuration 2 circuit to compare the dynamic properties of both circuits.

Bibliography

[1] M. H. Rashid, *Power Electronics*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1993.

[2] R. R. Errabelli, and P. Mutschler, "Fault- tolerant voltage source inverter for permanent magnet drives," *IEEE Trans. Power Electron.,* vol. 27, no. 2, pp. 500-508, Feb. 2012.
DOI: 10.1109/TPEL.2011.2135866

[3] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1453–1463, Jul. 2007.
DOI: 10.1109/TPEL.2007.900505

[4] F. Z. Peng, "Z-source inverter," IEEE Trans. Ind. Appl., vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.
DOI: 10.1109/TIA.2003.808920

[5] Z. J. Zhou, X. Zhang, P. Xu, and W. X. Shen, "Single-phase uninterruptible power supply based on Z-source inverter," IEEE Trans. Ind. Electron., vol. 55, no. 8, pp. 2997–3004, Aug. 2008.
DOI: 10.1109/TIE.2008.924202

[6] L. Zhang, K. Sun, Y. Xing, L. Feng, and H. Ge, "A modular grid-connected photovoltaic generation system based on dc bus," IEEE Trans. Power Electron., vol. 2, no. 26, pp. 523–531, Feb. 2011.
DOI: 10.1109/TPEL.2010.2064337

[7] J. Anderson, and F. Z. Peng, "Four quasi-Z-source inverters," in Proc. IEEE PESC'08, Jun. 2008, pp.2743-2749.
DOI: 10.1109/PESC.2008.4592360

[8] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2150–2158, Aug. 2010.
DOI: 10.1109/TPEL.2010.2046676

[9] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3453–3463, Dec. 2011.
DOI: 10.1109/TPEL.2011.2122309

[10] M. Adamowicz, R. Strzelecki, F. Z. Peng, J. Guzinski, and H. A. Rub, "New type LCCT-Z-source inverters," in Proc. Eur. Conf. Power Electron. Appl., 2011, pp. 1-10.
DOI: 10.1109/EEEIC.2011.5874799

[11] M.-K. Nguyen, Y.-C. Lim, and S.-J. Park "Improved trans-Z-source inverter with continuous input current and boost inversion capability," IEEE Trans. Power Electron., vol. 28, no. 10, pp. 4500–4600, Oct. 2013.
DOI: 10.1109/TPEL.2012.2233758

[12] M. K. Nguyen, Y. C. Lim, and Y. Kim, “TZ-source inverters,” IEEE Trans. Ind. Electron., vol. 12, no. 60, pp. 5686–5695, Dec. 2013
DOI: 10.1109/TIE.2012.2229678

[13] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, “New Magnetically Coupled Impedance (Z-) Source Networks,”, IEEE Trans. Power Electron., IEEE Trans. Power Electron., vol. 31, no. 11, pp. 7419-7435, Nov. 2016.
DOI: 10.1109/TPEL.2015.2459233

[14] P. C. Loh, D. Li, and F. Blaabjerg, “Γ-Z-Source Inverters,” IEEE transactions on Power Electronics, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.
DOI: 10.1109/TPEL.2013.2243755

[15] Z. Aleem, and M. Hanif, "Operational Analysis of Improved Γ-Z-Source Inverter with Clamping Diode and its Comparative Evaluation," in *IEEE Trans. on Ind. Electronics* , vol. 64, no. 12, pp.9191-9200, Dec. 2017.
DOI: 10.1109/TIE.2017.2708358

[16] S. J. Jun, and L. Kay-Soon, “Sigma-Z-source inverters,” *IET Power Electron.*, vol. 60, no. 12, pp. 5686–5695, 2015.
DOI: 10.1049/iet-pel.2014.0274

[17] W. Mo, P. C. Loh, and F. Blaabjerg, “Asymmetrical Γ-source inverters,” IEEE Trans. Ind. Electron., vol. 61, no. 2, pp. 637–647, Feb. 2014.
DOI: 10.1109/TIE.2013.2253066

[18] D. Vinnikov, and I. Roasto, “Quasi-Z-source-based isolated dc/dc converters for distributed power generation,” IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 192–201, Jan. 2011.
DOI: 10.1109/TIE.2009.2039460

[19] Y. P. Siwakoti, P. Fang Zheng, F. Blaabjerg, L. Poh Chiang, and G. E. Town, “Impedance-source networks for electric power conversion part I: A topological review,” IEEE Trans. Power Electron., vol. 30, no. 2, pp. 699–716, Feb. 2015.
DOI: 10.1109/TPEL.2014.2313746

[20] C. J. Gajanayake, F. L. Luo, H. B. Gooi, and L. k. Siow “Extended-boost Z-source inverters,” IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2642–2652, Oct. 2010.
DOI: 10.1109/ECCE.2009.5315977

[21] F. Z. Peng, M. Shen, and Z. Qian, “Maximum boost control of the Z-source inverter,” IEEE Trans. Power Electron., vol. 20, no. 4, pp. 833–838, Jul. 2005.
DOI: 10.1109/TPEL.2005.850927

[22] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, “Constant boost control of the Z-source inverter to minimize current ripple and voltage stress,” IEEE Trans. Ind. Appl., vol. 42, no. 3, pp. 770–778, May/Jun . 2006.

DOI: 10.1109/TIA.2006.872927

[23] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua, and Y.W. Li, "Pulse width modulation of Z-source inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1346–1355, Nov. 2005.
DOI: 10.1109/TPEL.2005.857543

[24] Y. P. Siwakoti, P. Fang Zheng, F. Blaabjerg, L. Poh Chiang, G. E. Town, and Y. Shuitao, "Impedance-source networks for electric power conversion part II: Review of control and modulation techniques," IEEE Trans. Power Electron., vol. 30, no. 4, pp. 1887–1906, Apr. 2015.
DOI: 10.1109/TPEL.2014.2329859

[25] Z. Aleem, D. Shin, H. Cha, J. P. Lee, D. W. Yoo, and F. Z. Peng, "Parallel Operation of Inverter Using Trans-Z-Source Network," IET Power Electronics, vol. 8, no. 11, pp. 2176-2183, 2015.
DOI: 10.1049/iet-pel.2014.0841

[26] Z. Aleem and M. Hanif, "A class of parallel operated impedance source inverters," *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Auckland, 2016, pp. 1-6.
DOI: 10.1109/SPEC.2016.7846026

[27] D. Xinping, and Z. Chenghui, "Switched coupled-inductor Z-source inverters with large conversion ratio and soft-switching condition," in IEEE Energy Conversion Congress and Exposition (ECCE 2014), pp. 5052-5058, 2014.
DOI: 10.1109/ECCE.2014.6954094

[28] M.-K. Nguyen, Y.-C. Lim, and G.-B. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183–3191, Nov. 2011.
DOI: 10.1109/TPEL.2011.2141153

[29] H. F. Ahmed, H. Cha, S.-H. Kim, H.-G. Kim, "Switched-coupled-inductor quasi-Z-source inverter", *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241-1254, Feb. 2016.
DOI: 10.1109/TPEL.2015.2414971

[30] Z. Aleem, and M. Hanif, "Improved Γ-Z-Source Inverter," in *IEEE Energy Conversion Congress and Exposition*, Sep. 2016, pp. 1-5.
DOI: 10.1109/ECCE.2016.7855192

[31] L. Pan, "L-Z-source inverter", *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6534-6543, Dec. 2014.
DOI: 10.1109/TPEL.2014.2303978

[32] S. Liu, B. Ge, X. Jiang, H. Abu-Rub, F. Z. Peng, "Comparative Evaluation of Three Z-Source/Quasi-Z-Source Indirect Matrix Converters", IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp.692-701, Feb. 2015.
DOI: 10.1109/TIE.2014.2349877

[33] L. He, S. Duan, and F. Z. Peng, "Safe-commutation Strategy for The Novel Family of Quasi-Z-source AC/AC Converter", IEEE Transactions on Industrial Informatics, vol. 9, no. 3, pp.1538-1547.
DOI: 10.1109/TII.2013.2245333

[34] M. R. Banaei, R. Alizadeh, N. Jahanyari, and E. S. Najmi, “An ac Z-source converter based on gamma structure with safe-commutation strategy,” IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1255–1262, Feb. 2016.
DOI: 10.1109/TPEL.2015.2415735

[35] B. Ge, Q. Lei, W. Qian, and F. Z. Peng, “A family of Z-source matrix converters,” IEEE Trans. Ind. Electron, vol. 59, no. 1, pp. 35–46, Jan. 2012.
DOI: 10.1109/TIE.2011.2160512

[36] Z. Aleem and M. Hanif, "Single-phase transformer based Z-source AC-AC converters," *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Auckland, 2016, pp. 1-6.
DOI: 10.1109/SPEC.2016.7846040

[37] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, “Single-phase ac–ac converter based on quasi-Z-source topology,” IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2200–2210, Aug. 2010.
DOI: 10.1109/TPEL.2010.2042618

[38] H. F. Ahmed, H. Cha, A. A. Khan and H. G. Kim, "A Family of High-Frequency Isolated Single-Phase Z-Source AC–AC Converters With Safe-Commutation Strategy," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7522-7533, Nov. 2016.
DOI: 10.1109/TPEL.2016.2539216

[39] S. Rajakaruna and L. Jayawickrama, “Steady-state analysis and designing impedance network of Z-source inverters,” IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2483–2491, Jul. 2010.
DOI: 10.1109/TIE.2010.2047990

[40] C. J. Gajanayake, D. M. Vilathgamuwa, and P. C. Loh, “Development of a comprehensive model and a multiloop controller for Z-source inverter DG systems,” IEEE Trans. Ind. Electron., vol. 54, no. 4, pp. 2352–2359,Aug. 2007.
DOI: 10.1109/TIE.2007.894772

[41] M. Shen and F. Z. Peng, “Operation Modes and Characteristics of the Z-Source Inverter With Small Inductance or Low Power Factor,” IEEE Trans. on Industrial Electronics, vol. 55, no. 1, pp. 89-96, Jan. 2008.
DOI: 10.1109/TIE.2007.909063

[42] Q. Tran, T. Chun, J. Ahn, and H. Lee, “Algorithms for controlling both the DC boost and AC output voltage of Z-source inverter,” IEEE Trans. Ind. Electron., vol. 54, no. 5, pp. 2745–2750, Oct. 2007.
DOI: 10.1109/TIE.2007.895146

[43] B. Zhao, Q. Yu, Z. Leng, and X. Chen, “Switched Z-source isolated bidirectional dc-dc converter and its phase-shifting shoot-through bivariate coordinated control strategy,” IEEE Trans. Ind. Electron., vol. 59, no. 12, pp. 4657–4670, Dec. 2012.
DOI: 10.1109/TIE.2011.2181136

[44] Z. Aleem. H. F. Ahmed, H. Cha, and H.-G. Kim, "Single-phase isolated impedance-source inverters," in Proc. Int. Conf. Power Electron., June. 2015, pp. 2359-2364.
DOI: 10.1109/ICPE.2015.7167776

[45] H. Cha, Y. Li, and F. Z. Peng, "Practical Layouts and DC-Rail Voltage Clamping Techniques of Z-Source Inverters," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7471-7479, Nov. 2016.
DOI: 10.1109/TPEL.2016.2518807

[46] D. G. Infield, P. Onions, A. D. Simmons, and G. A. Smith, "Power quality from multiple grid-connected single-phase inverters," IEEE Trans. Power Del., vol. 19, no. 4, pp. 1983–1989, Oct. 2004.
DOI: 10.1109/TPWRD.2004.829950

[47] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep. 2005.
DOI: 10.1109/TIA.2005.853371

[48] W. M. Blewitt, D. J. Atkinson, J. Kelly, and R. A. Lakin, "Approach to low-cost prevention of DC injection in transformer less grid connected inverters," IET Power Electron., vol. 3, no. 1, pp. 111–119, Jan. 2010.
DOI: 10.1049/iet-pel.2008.0319

[49] B. Wang, X. Guo, H. Wu, Q. Mei, and W. Wu, "Real-time DC injection measurement technique for transformerless PV systems," in Proc. IEEE 2nd Int. Symp. Power Electron. Distrib. Generation Syst., Hefei, China, Jun. 2010, pp. 980–983.
DOI: 10.1109/PEDG.2010.5545854

[50] X. Guo, W. Wu, W. Herong, and G. San, "DC injection control for grid connected inverters based on virtual capacitor concept," in Proc. IEEE Elect. Mach. Syst. Conf., Wuhan, China, Oct. 17–20, 2008, pp. 2327–2330.

[51] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics. Norwell, MA: Kluwer (Academic), ch. 15, 2001.

[52] K. Thorborg, Power Electronics. London, U.K.: Prentice-Hall International (U.K.) Ltd., 1988.

[53] N. Mohan, W. P. Robbin, and T. Undeland, Power Electronics: Converters, Applications, and Design, 2nd Ed. New York: Wiley, 1995.

[54] A. M. Trzynadlowski, Introduction to Modern Power Electronics. New York: Wiley, 1998.

[55] P. T. Krein, Elements of Power Electronics. London, U.K.: Oxford Univ. Press, 1998.

[56] P. J. Grbovic, P. Delaure, and P. L. Moigne, "A novel three-phase diode boost rectifier using hybrid half-dc-bus-voltage rated boost converter," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1316–1329, Apr. 2011.
DOI: 10.1109/TIE.2010.2050757

[57] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, “Comprehensive study of single-phase AC-DC power factor corrected converters With high-frequency isolation,” IEEE Transactions on Industrial Informatics, vol. 7, no. 4, pp.540-556, Nov. 2011.
DOI: 10.1109/TII.2011.2166798

[58] M.A. Sayed, K. Suzuki, T. Takeshita, W. Kitagawa, "PWM Switching Technique for Three-phase Bidirectional Grid-Tie DC-AC-AC Converter with High-Frequency Isolation", *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 845-858, Jan. 2018.
DOI: 10.1109/TPEL.2017.2668441

[59] G. Xu, D. Sha, X. Liao, "Input-series and output-parallel connected single stage buck type modular AC–DC converters with high-frequency isolation", *IET Power Electron.*, vol. 8, no. 7, pp. 1295-1304, Jul. 2015.
DOI: 10.1049/iet-pel.2014.0518

[60] W. Sulistyono, P. Enjeti, "A series resonant ac-to-dc rectifier with high frequency isolation", *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 784-790, Nov. 1995.
DOI: 10.1109/63.471299

[61] M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galván, R. C. P. Guisado, M. Á. M. Prats, J. I. León, and N. M. Alfonso, "Power electronic systems for the grid integration of renewable energy sources: A survey," IEEE Trans. Ind. Electron., vol. 53, no. 4, pp. 1002-1016, Aug. 2006.
DOI: 10.1109/TIE.2006.878356

[62] M. Singh, V. Khadkikar, A. Chandra, R. K. Varma, "Grid Interconnection of Renewable Energy Sources at the Distribution level with Power Quality Improvement Features," IEEE Transaction on Power Delivery, Vol. 26, No. 1, pp. 307-315, Jan. 2011.
DOI: 10.1109/TPWRD.2010.2081384

[63] O. Ellabban, H. Abu-Rub, F. Blaabjerg, "Renewable energy resources: Current status future prospects and their enabling technology", *Renew. Sustain. Energy Rev.*, vol. 39, pp. 748-764, 2014.
DOI: 10.1016/j.rser.2014.07.113

[64] T. Kawabata and S. Higashino, “Parallel operation of voltage source inverters,” *IEEE Trans. Ind. Applicat.*, vol. IA-24, pp. 281–287, Mar./Apr. 1988.
DOI: 10.1109/28.2868

[65] H. Cai, R. Zhao, and H. Yang, “Study on ideal operation status of parallel inverters,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2964-2969, Nov. 2008.
DOI: 10.1109/TPEL.2008.2003358

[66] B. Shi and G. Venkataramanan, “Parallel operation of voltage source inverters with minimal intermodule reactors,” in *Proc. 2004 IEEE Ind. Appl. Conf.*, pp. 156–162.
DOI: 10.1109/IAS.2004.1348402

[67] H. Behjati, A. Davoudi, and F. Lewis, "Modular DC-DC Converters on Graphs: Cooperative Control," in IEEE Transactions on Power Electronics, 2014, pp. 6725-6741.
DOI: 10.1109/TPEL.2014.2303192

[68] J. W. Kim, J. S. Yon, B. H. Cho, "Modelling control and design of input-series-output-parallel-connected converter for high-speed-train power system", *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 536-544, Jun. 2001.
DOI: 10.1109/41.925580

[69] Linbing Wang, and Xiangning He, "Input-Series and Output-Parallel Connection Modular DC-DC Converters with Interleaved Constant Duty Cycle Control Strategy," in IECON 2007-33rd Annual Conference of the IEEE Industrial Electronics Society: IEEE, 2007, pp. 1901-1906.
DOI: 10.1109/IECON.2007.4460355

[70] E. A. Jones, F. F. Wang, D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges", *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707-719, Sep. 2016.
DOI: 10.1109/JESTPE.2016.2582685

[71] D. Y. Chen, "Power semiconductors: Fast tough and compact", *IEEE Spectrum*, vol. 24, no. 9 pp. 30-35, Sept. 1987.
DOI: 10.1109/MSPEC.1987.6448932

[72] F. L. Luo and H. Ye, "Research on dc-modulated power factor correction ac/ac converters," in Proc. IEEE IECON, 2007, pp. 1478–1483.
DOI: 10.1109/IECON.2007.4460078

[73] "IEEE Standard Definitions and Requirements for Thyristor AC Power Controllers", in IEEE Std. 428-1981, pp. 1-28, 1981.
DOI: 10.1109/IEEESTD.1981.81455

[74] N. A. Ahmed, K. Amei, and M. Sakui, "A new configuration of single phase symmetrical PWM ac chopper voltage controller," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 942–952, Oct. 1999.
DOI: 10.1109/41.793343

[75] X. P. Fang, Z. M. Qian, and F. Z. Peng, "Single phase Z-source PWM ac-ac converters," IEEE Power Electron. Lett., vol. 3, no. 4, pp. 121–124, Dec. 2005.
DOI: 10.1109/LPEL.2005.860453

[76] M. Kazerani, "A direct AC AC converter based on current-source converter modules," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1168–1175, Sep. 2003.
DOI: 10.1109/TPEL.2003.816184

[77] B. Metidji, N. Taib, L. Baghli, T. Rekioua, and S. Bacha, "Review of three-phase PWM ac-ac converter topologies," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 4088– 5006, Nov. 2011.
DOI: 10.1109/TIE.2011.2159353

[78] J. Espina, J. Balcells, A. Arias, and C. Ortega, "Common mode EMI model for a direct matrix converter," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5049– 5056, Nov. 2011.
DOI: 10.1109/TIE.2011.2158774

[79] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, "Voltage swell/sag compensation with single-phase Z-source AC/AC converter," in *Proc. EPE'09,* pp. P.1-P.8, 2009.

[80] D. H. Jang and G. H. Choe, "Step-up/down ac voltage regulator using transformer with tap changer and PWM ac chopper," IEEE Trans. Ind. Electron., vol. 45, no. 6, pp. 905–911, Dec. 1998.
DOI: 10.1109/41.735334

[81] F. Z. Peng, L. Chen, and F. Zhang, "Simple topologies of PWM ac-ac converters," IEEE Power Electron. Letters, vol. 1, no. 1, pp. 10– 13, Mar. 2003.
DOI: 10.1109/LPEL.2003.814961

[82] R. Stala, S. Pirog, A. Mondzik, M. Baszynski, A. Penczek, J. Czekonski, and S. Gasiorek, "Results of investigation of multicell converters with balancing circuit. Part II," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2620–2628, Jul. 2009.
DOI: 10.1109/TIE.2009.2022562

[83] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, "Single-phase Z-source ac–ac converter with wide range output voltage operation," J. Power Electron.,vol. 9, no. 5, pp. 736–747, Sep. 2009.

[84] M. K. Nguyen, Y. C. Lim, and Y. J. Kim, "A modified single-phase quasi-Z-source ac-ac converter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 201–210, Jan. 2012.
DOI: 10.1109/TPEL.2011.2157362

[85] H. F. Ahmed, Z. Aleem, H. Cha, and H.-G. Kim, "A high frequency isolated single-phase impedance-source ac-ac converter," in Proc. Int. Conf. Power Electron., June. 2015, pp. 2359-2364.
DOI: 10.1109/ICPE.2015.7168099

[86] M. K. Nguyen, Y. G. Jung, H. Y. Yang, and Y. C. Lim, "Single-phase Z-source cyclo-converter with safe-commutation strategy," IET Power Electron., vol. 3, no. 2, pp. 232–242, Mar. 2010.
DOI: 10.1049/iet-pel.2008.0131

Appendix A

Assembly of the Hardware Prototype of Improved ΓZSI with clamping diode

The experimental rig consists of three major parts:

1. DSP Kit

2. Gate Drive Circuit

3. Power Stage circuit

DSP kit based on TMS320f28335 shown in Fig. 4.9 is used for the programming. The code composer software is used to generate the gating signals of the inverter bridge. The main coding protocols are shown in Appendix B. The fiber optics cables are used to connect the DSP kit with gate drive circuit. The voltages generated by DSP kit are below 5 Volts.

The gate drive circuit shown in Fig. A.1 works like a boost circuit for the switching signals generated by DSP Kit. The threshold voltage for IGBTs is 15V for switching 'on' and 'off'. The gate drive circuits boost the DSP signals (3V approx.) to meet the desired 15 V for the accurate working of the inverter bridge.

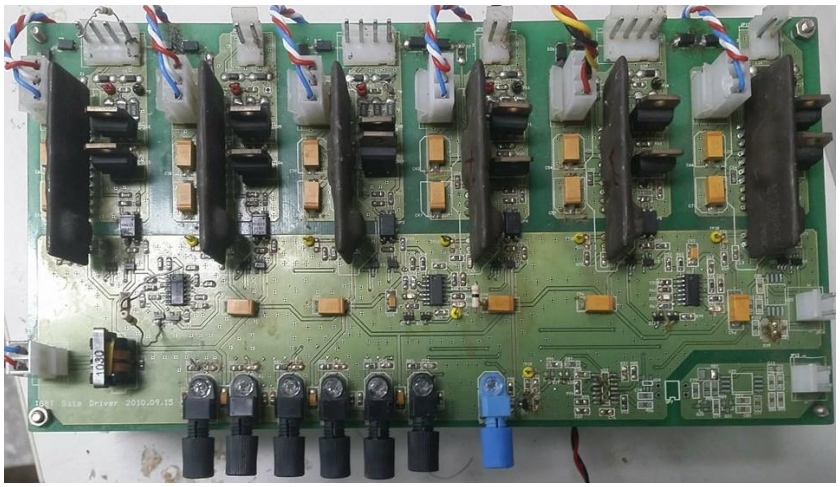


Fig. A.1 Gate drive circuit

Third part is the most important stage of the experimental rig that connects the power system with the load. It consists of inductors, film and filter capacitors, IGBTs, diodes and resistive load. The components selected to carry out experiments are shown in table A.1.

TABLE A.1

Electrical and Magnetic Components

Inductor and Transformer Core	EE 110/114/36
IGBT Six pack	CM100TU-12H
Diodes	IXYS DSEI 2 × 61-12B
Capacitors	MKP B32774 (EPCOS)

Appendix B

Coding Protocols

1. Header Files and Functions

```
#define      SYSCLK              150000000    /* Hz */
#define      ADC_SOC_FREQ        100000       /* Hz */
#define      PWM_CARRIER_FREQ    20000        /* Hz */
#define      Period              20000/* Hz */
#define      SINE_FREQ           50           /* Hz */

#define      PI                  3.1415927
#define      BUFFSIZE            400
#define MI_1                     0.9
#define MI_2                     0.9
#define SHOOT_THROUGH            0.1
#define SHOOT_THROUGH_INVERSE    0.1
#define dead_time1               100 //Z-source 100, non_Z-source 340
#define dead_time2               100 //Z-source 100, non_Z-source 340

/* Prototype statements for functions found within this file */
interrupt void MainISR(void);
void InitEPWMModules(Uint16 Period);
void InitECAPModules(Uint16 Period);

/* Global variables used in this file */

float32      Radian;
float32      RadianMax;
float32      RadianStep;
float32      SineOut1,SineOut2,SineOut3,SineOut4,SineOut5,SineOut6;

Uint16 PWMPeriod;
Uint16 PwmDuty1_H, PwmDuty1_L, PwmDuty2_H, PwmDuty2_L, PwmDuty3_H, PwmDuty3_L,
PwmDuty4_H, PwmDuty4_L, PwmDuty5_H, PwmDuty5_L, PwmDuty6_H,PwmDuty6_L;
Uint16 ShootDuty;
Uint16 ShootShift1,ShootShift2;

Uint16  ShootThough;
```

2. Sine Modulated PWM

```
SineOut1 = (1+MI_1*sin(Radian))/2;
       SineOut2 = (1+MI_1*sin(Radian-(RadianMax/3)))/2;
       SineOut3 = (1+MI_1*sin(Radian-(RadianMax/3*2)))/2;

       SineOut4 = (1+MI_2*sin(Radian))/2; // (Sine 4-6 to be used in case of
parallel inverters)
```

```
        SineOut5 = (1+MI_2*sin(Radian-(RadianMax/3)))/2;
        SineOut6 = (1+MI_2*sin(Radian-(RadianMax/3*2)))/2;

        Radian += RadianStep;

        if(Radian > RadianMax)
        {
                    Radian = 0.0;
        }

        PwmDuty1_H = PWMPeriod * SineOut1 - dead_time1/2;
        PwmDuty1_L = PWMPeriod * SineOut1 + dead_time2/2;

        PwmDuty2_H = PWMPeriod * SineOut2 - dead_time1/2;
        PwmDuty2_L = PWMPeriod * SineOut2 + dead_time2/2;

        PwmDuty3_H = PWMPeriod * SineOut3 - dead_time1/2;
        PwmDuty3_L = PWMPeriod * SineOut3 + dead_time2/2;

           // PwmDuty1_H = PWMPeriod * SHOOT_THROUGH;
               //PwmDuty1_L = PWMPeriod * SHOOT_THROUGH;

               //PwmDuty2_H = PWMPeriod * SHOOT_THROUGH_INVERSE ;
               //PwmDuty2_L = PWMPeriod * SHOOT_THROUGH_INVERSE ;

               //PwmDuty3_H = PWMPeriod * SHOOT_THROUGH;
               //PwmDuty3_L = PWMPeriod * SHOOT_THROUGH;

        /* Update EPWM's CMPA registers */
        EPwm1Regs.CMPA.half.CMPA = PwmDuty1_H;              /* Set Compare A
value */
        EPwm1Regs.CMPB = PwmDuty1_L;

        EPwm2Regs.CMPA.half.CMPA = PwmDuty2_H;              /* Set Compare A
value */
        EPwm2Regs.CMPB = PwmDuty2_L;

        EPwm3Regs.CMPA.half.CMPA = PwmDuty3_H;              /* Set Compare A
value */
        EPwm3Regs.CMPB = PwmDuty3_L;
```

3. EPWM Module Configuration

```
EPwm1Regs.TBPRD = Period;                           /* Set timer period */
        EPwm1Regs.TBCTR = 0;                        /* Clear counter */

        /* Setup counter mode */
        EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;            /* Count
up/down (Symmetric) */
        EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
        EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;                    /* Shadow
Mode */
```

```
	EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;         /* TB_CTR_ZERO */
	EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
	EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;                    /* TBCLK =
SYSCLKOUT / (HSPCLKDIV * CLKDIV) */

	/* Set Compare values */
	EPwm1Regs.CMPA.half.CMPA = 0;                /* Set Compare A value */
	EPwm1Regs.CMPB = 0;
	/* Set Compare B value */

	/* Setup shadowing */
	EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;       /* Load on
CNTR=Zero */
	EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
	EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;   /* Enable Shadowing */
	EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

	/* Set actions */
	EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
	EPwm1Regs.AQCTLA.bit.CBD = AQ_CLEAR;

	/* Set Dead time */
	EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
	EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
	EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
	EPwm1Regs.DBFED = dead_time1;
	EPwm1Regs.DBRED = dead_time2;
```

4. ECAP Modules (Shoot-through)

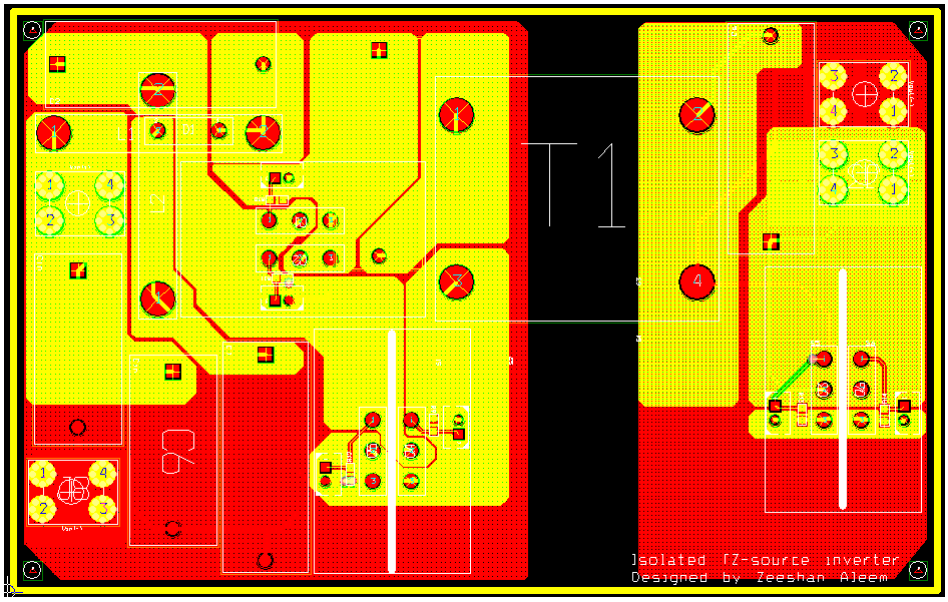
```
ShootShift1 = Period/2-Period*(1-(SHOOT_THROUGH/2+0.5))/2;
	ShootShift2 = ShootShift1+Period/2;

	// ECAP module 1 config
	ECap1Regs.CAP1 = Period; // Set period value
	ECap1Regs.CTRPHS = ShootShift1; // make eCAP1 reference phase = zero
	ECap1Regs.ECCTL2.bit.CAP_APWM = 1;
	ECap1Regs.ECCTL2.bit.APWMPOL = 1;
	ECap1Regs.ECCTL2.bit.SYNCI_EN = 1;
	ECap1Regs.ECCTL2.bit.SYNCO_SEL = 0;
	ECap1Regs.ECCTL2.bit.TSCTRSTOP = 1;

	// ECAP module 2 config
	ECap2Regs.CAP1 = Period; // Set period value
	ECap2Regs.CTRPHS = ShootShift2; // Phase offset = 1200-400 = 120 deg
	ECap2Regs.ECCTL2.bit.CAP_APWM = 1;
	ECap2Regs.ECCTL2.bit.APWMPOL = 1;
	ECap2Regs.ECCTL2.bit.SYNCI_EN = 1;
	ECap2Regs.ECCTL2.bit.SYNCO_SEL = 0;
	ECap2Regs.ECCTL2.bit.TSCTRSTOP = 1;

	ShootDuty =  Period*(SHOOT_THROUGH/2+0.5);
```

```
//ECap1Regs.CAP2 = ShootDuty; // Set duty
//ECap2Regs.CAP2 = ShootDuty; // Set duty
ECap1Regs.CAP2 = 2000; // Set duty
ECap2Regs.CAP2 = 2000; // Set duty
```

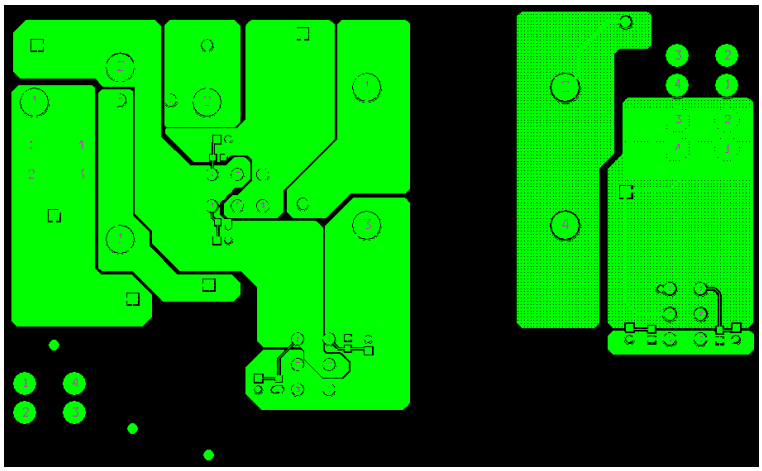
Appendix C

PCB Design of the Isolated Improved ΓZSI

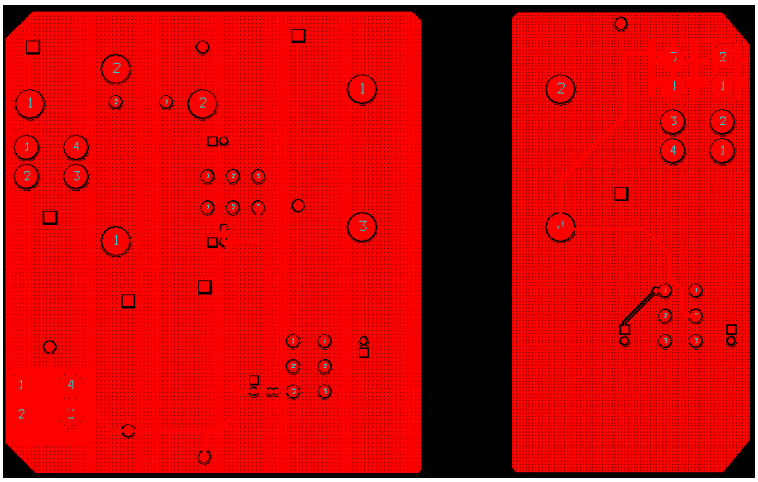
Orcad software version 10.5 is used to design the PCBs of the inverters and converters discussed in the thesis. The PCB design of the proposed high frequency isolated inverter is shown in Fig. C.1 as an example. Fig. C.1 (a) shows the full design the PCB, while Fig. C.1 (b) and (c) shows the top and bottom side of the PCB design.



(a)



(b)



(c)

Fig. C.1 PCB layout for the proposed isolated inverter

Appendix D

Simulation Model of Circuit Configuration 1

The saber simulation model of circuit configuration 1 with control blocks and testing points is shown in Fig. D.1. The values of components selected are shown in the saber simulation model and given in table 6.2.

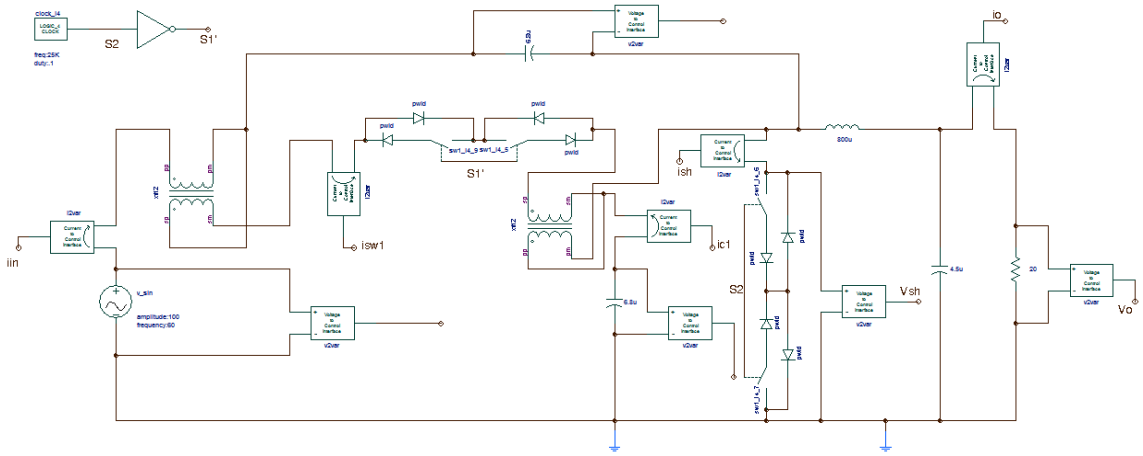


Fig. D.1. Saber simulation model of circuit configuration 1

Simulation Model of Circuit Configuration 2

The configuration 2 prototype model in saber simulation is shown in Fig. D.2. Current probes and voltage probes are connected at proper testing points to measure the voltage and current waveforms shown in Section 6.4.

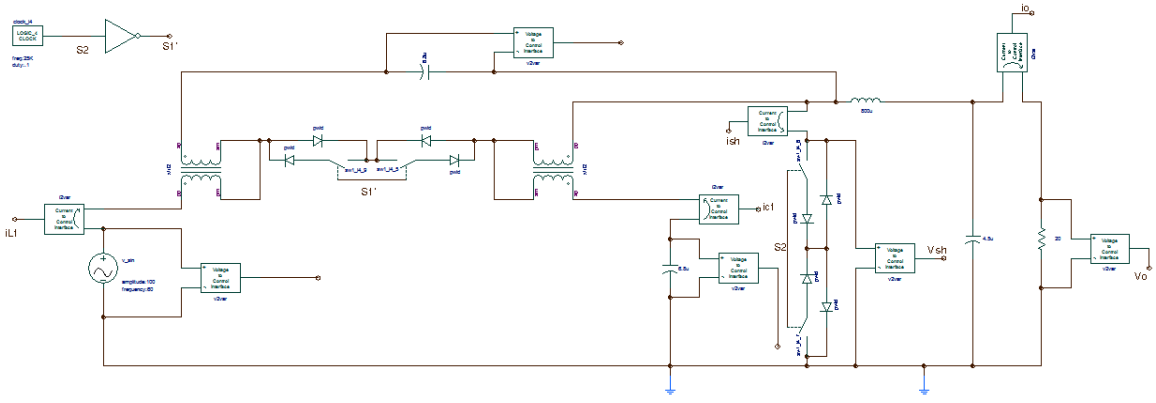


Fig. D.2. Saber simulation model of circuit configuration 2