An Electrical Power System for CubeSats

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Declaration

I know the meaning of plagiarism and declare that all work in this document, save for that which is properly acknowledged, is my own.

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Abstract

The advent of CubeSats has provided a platform for relatively low-budget programmes to realise space missions. In South Africa, Stellenbosch University and the Cape Peninsula University of Technology have impressive space programmes and have been involved in numerous successful satellite launches. A number of CubeSat projects are currently in progress and commercial-grade Attitude Determination and Control Systems (ADCS), and communications modules, are being developed by the respective universities. The development of a CubeSat-compatible Electrical Power System remains absent, and would be beneficial to future satellite activity here in South Africa.

In this thesis, some fundamental aspects of electronic design for space applications is looked at, including but not limited to radiation effects on MOSFET devices; this poses one of the greatest challenges to space-based power systems. To this extent, the different radiation-induced effects and their implications are looked at, and mitigation strategies are discussed.

A review of current commercial modules is performed and their design and performance evaluated. A few shortcomings of current systems are noted and corresponding design changes are suggested; in some instances these changes add complexity, but they are shown to introduce appreciable system reliability.

A single Li-Ion cell configuration is proposed that uses a 3.7 V nominal bus voltage. Individual battery charge regulation introduces minor inefficiencies, but allows isolation of cells from the pack in the case of cell failure or degradation. A further advantage is the possibility for multiple energy storage media on the same power bus, allowing for EPS-related technology demonstrations, with an assurance of minimum system capabilities.

The design of each subsystem is discussed and its respective failure modes identified. A limited number of single points of failure are noted and the mitigation strategies taken are discussed. An initial hardware prototype is developed that is used to test and characterise system performance. Although a few minor modifications are needed, the overall system is shown to function as designed and the concepts used are proven.

Overall system design is concluded to be reliable and efficient, with a few hardware-based recommendations made to bring its power capabilities in line with current offerings and, indeed, the initial specifications. Active Maximum Power Point Tracking (MPPT) functionality is tested under a variety of irradiance and temperature conditions and although performance is not yet optimal, control stability and the possibility for high conversion efficiency is demonstrated.

Additional software development is still required to fully optimise the system. Nevertheless, after further testing, performance characterisation and full environmental qualification, it is anticipated that the goal of producing a realistic alternative to commercial-grade EPS modules will be met.

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Acronyms

ADC Analogue-to-Digital Converter.

ADCS Attitude Determination and Control System.

BCR Battery Charge Regulator.

BOL Beginning-of-Life.

CAN Controller Area Network.

CC Constant Current.

COTS Commercial off-the-Shelf.

CPUT Cape Peninsula University of Technology.

CRC Cyclic Redundancy Check.

CV Constant Voltage.

DMA Direct Access Memory.

DOD Depth of Discharge.

ECC Error Correcting Code.

EDAC Error Correction and Detection.

EM Electro-magnetic.

EPS Electrical Power System.

ESR Equivalent Series Resistance.

F'SATI French South African Institute of Technology.

IR Infrared.

LCL Latching Current Limiter.

LEO Low Earth Orbit.

MPPT Maximum Power Point Tracking.

MTBF Mean Time Between Failures.

RBF Remove Before Flight.

RTG Radioisotope Thermoelectric Generator.

SAA South Atlantic Anomaly.

SCR Silicon Controlled Rectifier.

SEB Single Event Burnout.

SEC-DED Single Error Correction, Double Error Detection.

SEE Single Event Effect.

SEL Single Event Latchup.

SEU Single Event Upset.

SOC State of Charge.

SUN Stellenbosch University.

TID Total Ionising Dose.

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Chapter 1

Introduction

The field of electronics is ever-evolving; new applications require new technology, and innovative ways are found to use this technology. While the application of electronics to space exploration is inherent and has existed for over fifty years, opportunity for innovative and/or new electronic space systems was limited, given that space missions were, for a long time, associated with high budgets and long timeframes.

It was the advent of the nanosatellite category and the subsequent CubeSat concept that, in 1999, opened up the field of space technology to universities and similar institutions. Very quickly, it became possible for low-budget missions to realise a launch, at low cost, within a reasonable timeframe.

In South Africa, an increasing level of satellite work is being seen: both the Cape Peninsula University of Technology (CPUT) and Stellenbosch University (SUN) have been involved with successful nano- and micro-satellite launches, and have active space-based research programmes. Impressive work is being done on Attitude Determination and Control Systems, as well as communications systems, with these modules seeing international commercial availability.

The development of a CubeSat-compatible Electrical Power System (EPS) module serves two purposes: it initiates the University of Cape Town's contribution to the field of space technology, and also makes available a local EPS module for use on future CubeSat missions; no such module is currently available.

1.1 Objectives

The objectives of this work are thus to design a CubeSat-compatible EPS that is a realistic alternative to the commercial modules currently used for local satellite projects. Although the scope will show that having a flight-ready module as the initial aim is impractical for a variety of reasons, this remains the ultimate goal; thus, this work serves to produce such a system that, after some further development and testing, can achieve this end goal.

In light of this, the objectives are thus to design a system that takes into account the reliability, efficiency and functionality needed, in such an application, at each fundamental design step. Functionality and performance should match or exceed that of comparable modules which necessitates a review of such modules.

Sufficient testing of the system must be done to quantify its suitability to meeting the end goal.

1.2 Scope and Limitations

Work is initiated with the intention to develop a fully-functional EPS module that has the potential to be used on CubeSat missions. However, the long time frames that are associated with full qualification and testing, make the production of a flight-ready module impractical, and thus it is not the immediate goal.

Having the system evolve into one that is flight-ready, nevertheless, remains the ultimate purpose of this work; thus, sufficient scope is given to produce a system, ready for initial (ground-based) field testing, and to validate its suitability to CubeSat missions. Full consideration for this end goal should be given, at each step of the design process, to prevent fundamental compromises being made.

1.3 Outline of the Report

This report begins with a review of relevant background theory, literature and aspects of electronic design, in the context of space-based applications. Particular focus is placed upon different energy storage technologies, the harvesting of solar power and the effects of radiation on electronics.

A brief but detailed review is then done of existing EPS modules that have seen popularity amongst international, but more importantly local, CubeSat missions. The functionality and performance of these modules is used initially as a guideline for the EPS design, and later as a benchmark for performance analysis.

The work then shifts to the preliminary specifications and high-level design of the module. Few assumptions are started with and each subsystem is carefully specified and its implementation discussed. Where relevant, consideration is given to maintaining compatibility with current designs. By the end of System Design, a high-level design is presented that has each subsystem well defined and specified.

Chapter 5 presents the schematic design of each subsystem: component choice is argued, the low-level operation is discussed where relevant, and a detailed analysis is performed that identifies points of failure.

The design of the application software is then discussed, with a high-level approach taken to present the flow of operation. A number of key software features are discussed, as well as an overview of the high-level tasks that are performed.

Results and accompanying analyses follow, with emphasis placed upon the capabilities and efficiencies of the system. Certain aspects of the system are discussed with respect to improvements that are needed.

The work concludes with conclusions and recommendations, before a series of appendices provide summaries of system functions, along with additional work that was performed.

Chapter 2

Designing for Space & Other Background Theory

Compared to other nanosatellite subsystems, the EPS appears to have very little research devoted to it. This may be because the design of scientific payloads, advanced communications systems and the like, is far more appealing than that of the underlying power system. Moreover, its critical role may also be a deterring factor: with mission designers unwilling to risk new power systems over those with flight heritage, there is little opportunity for new research to be put into practice.

EPS-based innovation, at least for CubeSats and nanosatellites, appears to be limited to university designs for student CubeSat projects. It has been noted that such EPS designs are often overly complex, due to a need and/or desire for innovation [1], which may be the reason for the suggestion of the power system being the leading cause of CubeSat failure [2, p. 807]. Thus, something could be said for innovation being an improvement upon the fundamental reliability of the system.

Given this, and an aim to produce a system that is a realistic alternative to commercially-available, flight-proven systems, this chapter will focus on some fundamentals to allow a truly reliable and flexible end product be designed.

2.1 CubeSats

Nanosatellites are a category of small satellites typically weighing between 1 and 10 kg. CubeSats, a subset of nanosatellites, are characterised by complying with a specific set of design rules and constraints. This standardisation is what drives down their cost and development time, and allows the possibility for "plug-and-play" modules. This section looks at said standardisation, as well as past, present and future CubeSat activity in South Africa.

2.1.1 Specifications

CubeSats take their name from, and indeed are characterised by, the ten centimetre cubes that make up their structure. These cubes are referred to as "units", with a basic one-unit structure known as a "1U CubeSat". Usually only expandable along one axis — in multiples of these cubes and limited to a total of three such cubes — variations on this, such as 0.5U and 6U, have been seen. The limitation comes from the fact that multiple CubeSats are deployed using a standard deployment mechanism; as a result, they must conform to very specific sizing constraints.

With the CubeSat design philosophy suggesting low cost, electronic components are usually limited to Commercial off-the-Shelf (COTS) devices that are far cheaper, and more widely available, than their radiation-hardened counterparts. To make operation with such components more reliable, CubeSats are generally limited to Low Earth Orbit (LEO) with altitudes ranging from around 100–600 km. At these low altitudes, the spacecraft is still under appreciable protection from the Earth's magnetosphere, making exposure to ionising radiation tolerable [3].

Nevertheless, the lifespan of CubeSats is typically limited to 24 months. Besides radiation-induced electronic degradation, the multiple daily eclipse periods — a result of being in Low Earth Orbit (LEO) — means that on-board batteries suffer thousands of cycles over any extended period. The Colorado Student Space Weather Experiment (CSSWE) CubeSat is one such example where severe battery degradation, after 24 months, meant there was no longer sufficient power for the transmitter to function [4].

2.1.2 The Electrical Power System

The primary function of the EPS is to deliver electrical power to other subsystems, with power generation the first step of this process. While solar energy is most frequently used — it is reliable, cheap, safe and predictable — satellites with higher power requirements, as well as spacecraft heading to the outer solar system, may rely on other methods such as a Radioisotope Thermoelectric Generator (RTG). An RTG generates heat from the slow decay of a radioactive element and is a very effective method for large spacecraft — *Voyager 1* for instance, launched in 1977 and currently passing through the outer threshold of our solar system and into interstellar space, has RTGs that still generate a constant 225 W of power, down from 470 W at launch [5].

In order to effectively distribute power, the generated power needs to be stored as well as regulated. An on-board processor will typically perform some power management, including but not limited to overcurrent protection, turning subsystems on and off and providing housekeeping data to the communications bus.

A detailed power budget would be drawn up by the mission designer. From this, a set of power requirements can be determined in order to specify the size of solar panels and energy storage. These power requirements need to take into account the anticipated orbital parameters as these influence the number and length of eclipse periods. The tight sizing constraints also mean that solar panels are usually limited to being mounted on the body, although a driving need for more power has seen an increase in the use of deployable panels [2, pp. 807-808].

2.1.3 The CubeSat Kit Standard

The popularity of CubeSats and their use for fast turnaround missions has led to a number of commercially-available EPS modules. *GomSpace* and *Clyde Space* both provide a good range of products that are widely used, and Chapter 3 looks at their range of EPS modules in detail.

As a result of said popularity a form of standard has evolved, known as CubeSat Kit. While essentially a prototyping platform, allowing the development of mission-specific modules including both software and hardware, it also defines a structure

and set of requirements to allow different modules to connect to one another and interact through a defined bus system [6].

Modules that comply to CubeSat Kit are based on a PC/104 mechanical design. The characteristic stack-through connector and physical size makes it well-suited to CubeSats, with the connector allowing a "bus" structure that has pin functionality fairly well defined.

Inter-subsystem communications are typically carried out over an I^2C bus available on the header, although with no specification as to data packets or how subsystems should communicate. A central processor, usually apart of a "motherboard", manages communications and acts as the bus master — it will run mission-specific software that issues commands to and requests data from subsystems, which it then prepares for downlink via the communications system.

2.1.4 Launch Requirements

The standardisation of the CubeSat deployment process means that a few launch requirements exist [7]. At a minimum, a CubeSat is required to have one 'kill switch' that disables the CubeSat during launch. A separation switch will usually be positioned on the top plate of the CubeSat and use the deployment rails to keep it depressed. As the CubeSat is automatically released, this switch is activated and can allow the satellite to turn on. Depending on implementation, this separation switch may be the kill switch, or, rather, be used to trigger a separate kill switch.

In addition, the CubeSat requires a Remove Before Flight (RBF) pin that keeps the satellite deactivated during shipping and launch preparation. This pin usually functions such as to prevent the separation switch from triggering a separate kill switch.

2.1.5 South African CubeSat Work

CubeSats are relatively new to the South African scene with the first locally-built CubeSat launched in 2013. Named *ZACube-1*, the 1U CubeSat was built through a collaboration by the French South African Institute of Technology (F'SATI) based

at the CPUT, SUN and the South African National Space Agency (SANSA) [8].

ZACube-1's Attitude Determination and Control System (ADCS) and RF communications system were developed by CPUT. The on-board computer (OBC) module and EPS were both purchased from Pumpkin Inc. and Clyde Space respectively [9].

Although ZACube-1 is experiencing problems with its primary payload, it is still responsive and transmitting. Meanwhile, work is underway on ZACube-2, a 3U CubeSat that will serve as a technology demonstrator for a Software Defined Radio (SDR) platform. ZACube-2 will feature an ADCS developed by SUN, an RF communications module developed by CPUT, and a Clyde Space EPS [10].

ZA-AeroSat is a 2U CubeSat under development by SUN as apart of QB50, an initiative by the Von Karman Institute in Belgium that aims to simultaneously launch 50 CubeSats in early 2016 [11]. This CubeSat will use an innovative passive aerodynamic attitude control system, developed by the university.

Apart from these projects, SUN and CPUT are continuing development and research on their respective ADCS and RF communications modules and related work. It seems work on an EPS remains absent, and that such a module would help contribute to a future CubeSat that is entirely South African-developed.

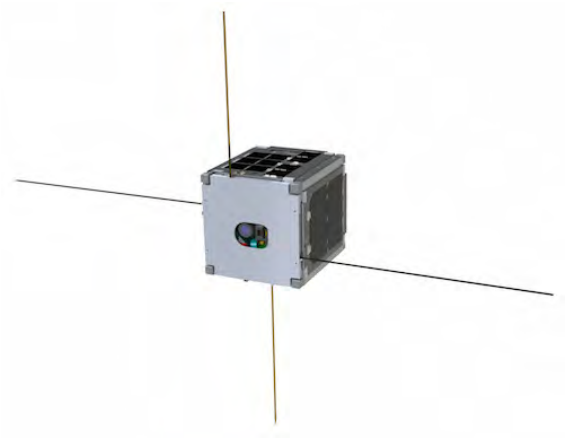


Figure 2.1: Computer render of ZACube-1. Image Credit: F'SATI.

2.2 The Space Environment

One of the most significant differences between systems designed for terrestrial use versus space is their operating environment. Radiation is probably the greatest threat to electronics, with further stress coming from large temperature variations and being in a near-vacuum. In addition, an EPS needs to take into account solar availability and strength, and implications the orbital path has on this.

2.2.1 Radiation

The harsh radiation environment in space presents a significant challenge to the design of space-destined electronics. Trapped protons and electrons within the Van Allen belts, heavy ions trapped within the magnetosphere, cosmic ray protons and heavy ions, and protons and heavy ions from solar flares are all sources of radiation, and are the predominant sources of energetic particles within the space environment [12]. While the specifics of each of these sources is not of immediate interest, what should be noted is that the amount of radiation experienced by a satellite will vary depending on numerous factors, including coinciding solar activity and the satellite's specific orbital path.

For low-altitude satellites, the dominant radiation source will be the Van Allen belts. Orbital inclinations of $0^o < i < 30^o$ give rise to the greatest variation in particle fluxes along the orbital path, while inclinations greater than 60^o see an almost constant level of radiation. Variations with altitude are most pronounced within the LEO range, and the greatest threat within this range is the South Atlantic Anomaly (SAA) [12, pp. 2-3].

The specific effects that radiation has on electronic devices will be discussed in later sections, with particular emphasis on power MOSFETs due to their likelihood of being a single point of failure within the system.

2.2.2 Temperature Variations

The absence, or at least near-absence, of gasses within the space environment causes objects to experience extreme temperature fluctuations; when exposed to the sun, the object's temperature will rise rapidly and, when in shadow, will radiate its heat back into space. Larger satellites will generally have advanced active thermal control systems, including heaters and radiators, to precisely regulate spacecraft temperature. In contrast however, CubeSats will typically rely on innovative thermal design using insulation and other techniques that keep the internal components within a range of -30–+30^{o}C [2, pp. 685-690] [2, pp. 809-810] [13]. Thermal design is separate from the design of the EPS and other payloads however and its presence, and thus a suitable thermal environment, will be assumed.

Solar panels will almost always cover the outer surface of the six CubeSat facets and thus form the thermal boundary between the satellite and the environment [2, pp. 805-807] [14]. Although reports differ slightly on the temperatures seen by body-mounted solar panels, the fluctuations are in the range of -80–+100^{o}C, with the extremes seen at the end and beginning of the eclipse period respectively [2, p. 645] [14]. The effect of these fluctuations, and implications for the EPS, will be discussed in subsequent sections.

2.2.3 Solar Strength

The solar constant is a level of solar irradiance (power per unit area, denoted E_e) equal to 1368 W/m^2; this is the amount of incident solar power received by a surface, perpendicular to the *sun line*[1], at the top of Earth's atmosphere [2]. Solar radiation power decreases with the inverse-square law, and is the reason why spacecraft heading towards the outer solar system typically do not rely on solar energy to power their systems.

In terms of solar panels and a fixed solar irradiance, the effective panel area is reduced by the angle that it makes with the sun line. This relationship closely

[1]The *Sun line* is an imaginary line from the object of interest to the Sun.

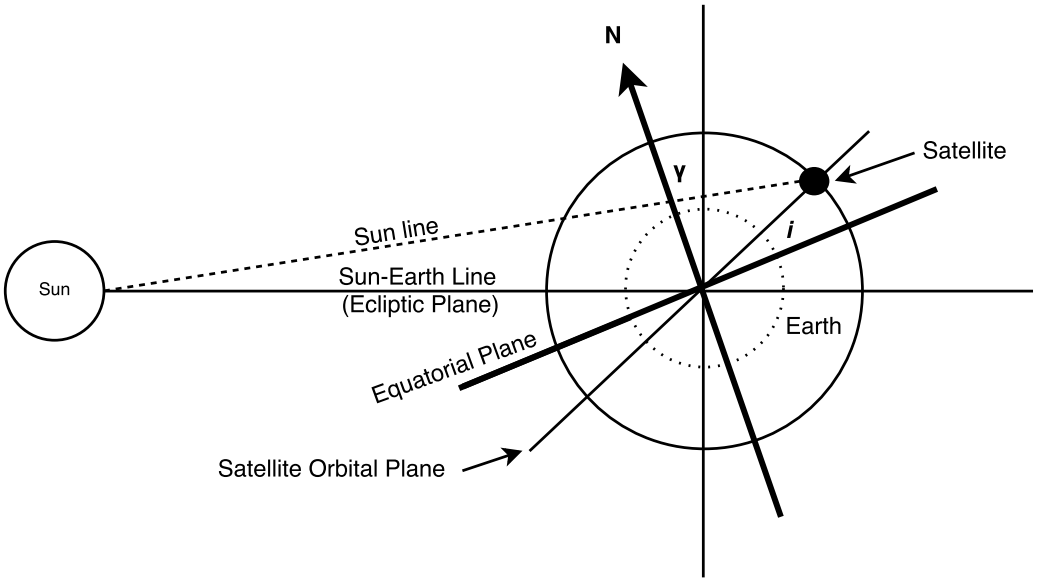


Figure 2.2: Diagram depicting the geometry of the Sun-Earth-satellite system. Adapted from [15, p. 17].

follows the cosine law [15, p. 22], giving

$$E_{effective} \approx E_e \cos\theta \tag{2.1}$$

For $\theta > 80^o$ however, the panel should not be expected to generate any usable power [15, p. 112].

2.2.4 Orbital Implications

The specific orbital path that a spacecraft takes through the atmosphere affects not only the radiation environment it will experience, but also the availability of sunlight. While the angle θ in (2.1) refers to the angle between a given surface (ie. a solar panel) and the sun line, a further angle exists — the beta angle — that describes the angle that the Sun-Earth line makes with the orbital plane [15, p. 19]. This angle varies seasonally in a range given by $\beta = \pm(i + \gamma)$, where i is the orbit inclination and γ the angle between the sunline and ecliptic plane (23.45^o). These angles are shown in Fig. 2.2. Given a beta angle, the percentage of the eclipse period of the entire orbital period (for a circular orbit) can be determined by [16]

$$f_e = \frac{1}{\pi} \arccos \left\{ \frac{\sqrt{h^2 + 2R_E h}}{(R_E + h)\cos\beta} \right\} \tag{2.2}$$

where h is the orbit altitude and R_E the radius of the Earth. Fig. 2.3 shows the variation in percentage with the beta angle. Note that this is for an altitude of 400 km; it is not representative of any particular mission, but it can be seen that the eclipse period can vary from 0% to around 40% of the orbital period.

The orbital inclination will affect the average eclipse time, and thus the anticipated orbit is a crucial consideration when designing a spacecraft's power system. Although such design is performed only when sizing the solar panels and energy storage in order to fulfil a particular mission's power requirements, this emphasises the need for flexibility in terms of power capabilities.

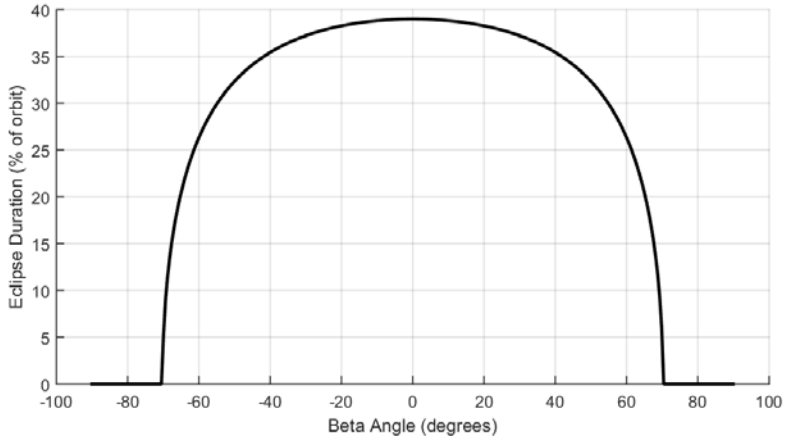


Figure 2.3: Variation in a spacecraft's eclipse period with beta angle at a 400 km altitude.

2.3 Photovoltaic Cells

Photovoltaic cells, or solar cells, generate the power for the vast majority of satellites. Their simplicity, reliability and relative low cost make them ideal for a wide range of spacecraft. While much of this section will be of more concern to a mission designer — they choose the types of panels to be used — the data will be important when simulating the EPS's performance in a typical environment and understanding the inputs that the EPS can expect.

2.3.1 Solar Cell Fundamentals

Cells are named and categorised according to the semiconductor material used, with materials differing in the portion of the Electro-magnetic (EM) spectrum that they absorb. In order to convert as much solar radiation as possible, the material should realistically absorb the entire visible, and part of the Infrared (IR), range. By combining two or more semiconductor material layers within a cell, the cell's EM absorption range can be increased; these are known as *multi-junction* cells, due to the multiple P-N junctions now present within the cell [17]. The inherent added complexity in manufacturing multi-junction cells makes them significantly more expensive than their single-junction counterparts; however, they have found wide use in space applications where a high performance-to-cost ratio is justified through a superior power-to-weight ratio [2]. Degradation of cells from the radiation they are exposed to is also of concern, especially in the space environment.

The efficiency of a cell is an important metric that relates to the percentage of the incident solar energy it can convert into electrical energy. Specifically, it refers to the cell's output power when exposed to 1368 W/m^2 (the solar constant). In practice however, a cell is not exposed to these conditions and will rather receive a fraction of this: *irradiance* is a measure of actual solar energy striking a given area per unit time. The amount of power generated by the cell will increase as irradiance increases [18].

Each cell develops a potential of between 0.5–1 V under open-circuit (V_{oc}) conditions, and can output in the order of tens of milliamps when short-circuited (I_{sc}). While the amount of current is useful, the voltage may be inadequate for the major-

Table 2.1: Beginning-of-Life (BOL) specifications for the Clyde Space 1U solar panel. Data from [23].

Parameter	**Temperature** (^{o}C)	**1U Module**
V_{oc}	-40	6.13 V
V_{mpp}	-40	5.58 V
V_{mpp}	+80	4.02 V
V_{mpp}	+28	4.70 V
P_{mpp}	-40	2.46 W
P_{mpp}	+80	1.79 W
P_{mpp}	+28	2.08 W

ity of applications. Thus, it is common for cells to be connected in series, known as *strings*, which can then be paralleled together to form a *module* [19, 2]. It is common amongst the literature to see nanosatellite applications using module configurations with $V_{oc} = 5$ V and $I_{sc} \approx 500$ mA.

2.3.2 Use On Satellites

Solar cells have been employed to provide power to satellites since the fourth successful satellite ever launched. While the first three, *Sputnik 1 and 2*, and the USA's *Explorer 1* relied on chemical batteries that ran flat after a few months, the USA's *Vanguard 1 (TV4)* contained a solar-powered transmitter that allowed transmissions to continue for a further six years [20, pg. 9] [21].

With the aforementioned importance placed on the power-to-weight ratio (cost a relatively insignificant factor), along with the need to have good endurance in space's radiation environment, Gallium Arsenide (GaAs)-based cells have found themselves the standard amongst the majority of space applications [2, pp. 643-644] [22].

Triple-junction GaAs cells, consisting of wafers of Indium gallium phosphide (InGaP), Indium gallium arsenide (InGaAs) and Germanium (Ge), have efficiencies approaching 30% [2, p. 645] [19]. Radiation exposure in the upper atmosphere causes a 15% reduction in output power over a span of up to 33 years, with other commercially-available cells seeing the same degradation over a period of approximately ten years [2, p. 645].

The Beginning-of-Life (BOL) properties for Clyde Space solar modules are listed in Table 2.1. These modules are commonly used on CubeSats, and in particular for local CubeSat missions.

2.3.3 I-V Curve

A solar cell can be approximated by a current source in parallel with a diode, along with a couple of parasitic elements. Fig. 2.4 gives the equivalent circuit of a solar cell. The model contains an ideal current source producing the *photocurrent* (I_L), a parallel diode, a parallel shunt resistance R_{sh} and a series resistance R_s [24].

The diode is characteristic of the P-N structure of the cell, while the series resistance models losses from the transfer of current from the cell material to the electrical contacts. The series resistance also includes resistive losses through the contacts themselves, and the shunt resistance models the leakage current within the cell. Variations in these parameters give rise to the current-vs-voltage curves in Fig. 2.5 [19]. The magnitude of the photocurrent is proportional to irradiance.

It is clear from the shape of the I-V curve in Fig. 2.5 that the power extracted from the cell will vary depending on the load voltage, V, and the corresponding current, I, drawn. The combination of V and I is known as the *operating point* of the cell/module, with maximum power available when the operating point is such that $V \times I$ is maximal. This point is known as the *global maximum*, and will be discussed further in Sec. 2.3.5.

Partial shading of panels can cause multiple *local maxima* that makes finding the global maximum more complex. In the context of a CubeSat, such partial shading

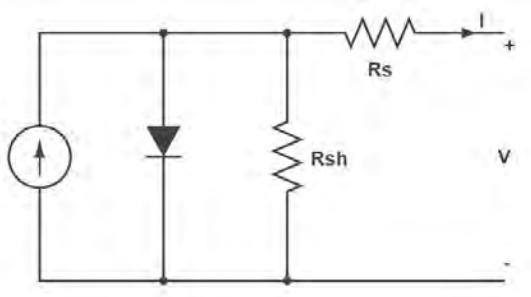


Figure 2.4: Equivalent circuit of a solar cell.

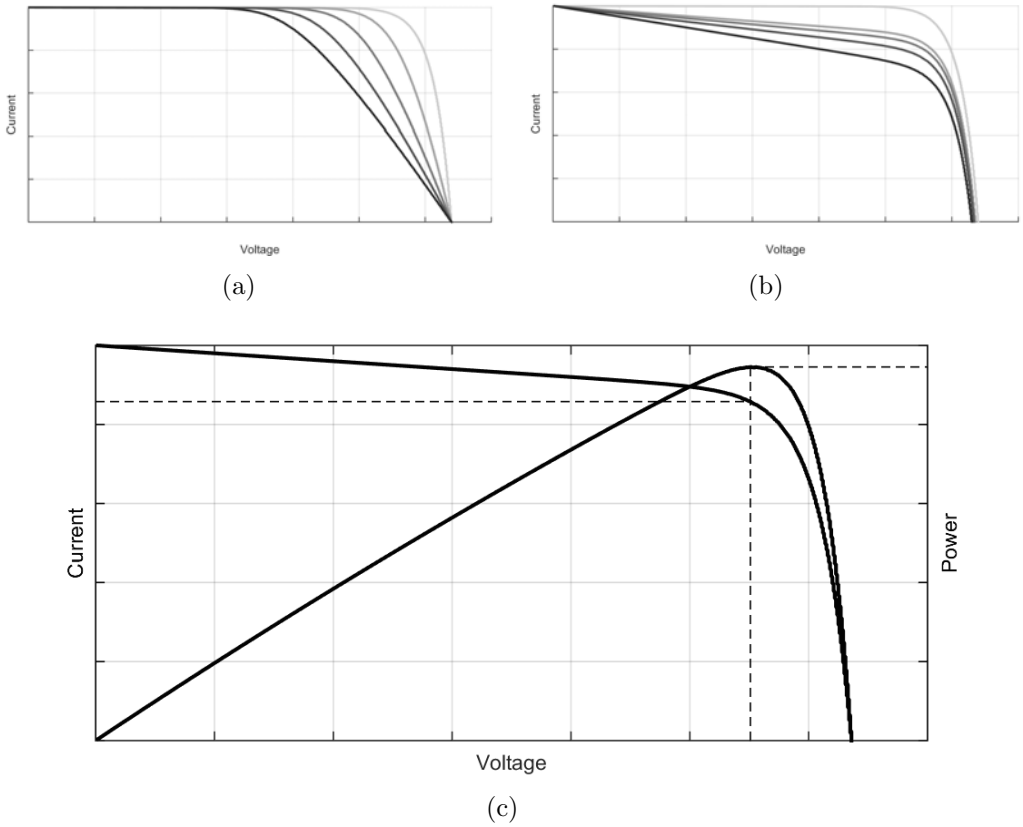


Figure 2.5: Plots showing the variations in a solar cell's I-V curve with varying cell parameters. (a) Lines darken with increasing R_s ($R_{sh} \to \infty$), (b) lines darken with decreasing R_{sh} ($R_s = 0$), and (c) a typical cell's I-V and corresponding P-V curve at a specified irradiance.

may be caused by deployable panels, antennae and/or external sensors for scientific experiments, that cast shadows on the body of the satellite.

2.3.4 Temperature Variation

Irradiance is not the only factor influencing the photocurrent generated by a cell, with environmental conditions also having a significant effect. A change in temperature of the cell or panel can have three effects on the I-V curve, namely [2]:

- A scaling of the curve along the current axis;
- A translation of the curve along the voltage axis; and
- A change in the roundness of the knee region.

The extent to which these affect the output depend upon a cell's *temperature coefficient* which is characteristic of the type of cell and the array configuration; however, an increase in temperature will always reduce cell performance [2, p. 645] [24].

2.3.5 Maximum Power Point Tracking

The non-linear I-V curve seen in Fig. 2.5 describes a power curve that will have a "peak" that corresponds to the knee of the I-V curve. Fig. 2.5c shows the power curve overlaid over a typical I-V curve; such a characteristic has the implication that, in order to extract the maximum possible power from a panel, the operating point needs to be set to the appropriate voltage, V_{mpp}, and corresponding current, I_{mpp}.

For an unobstructed panel, the position of the global maximum (V_{mpp}) stays roughly proportional to V_{oc} with changes in irradiance. The introduction of environment effects however, such as variations in temperature and non-uniform irradiance, causes the V_{mpp}/V_{oc} relationship to deviate from proportionality [18, 25]. Thus, while simple enough under constant operating conditions, in practice, this task of choosing and/or finding the optimal operating point becomes more complex. A Maximum Power Point Tracking (MPPT) technique is typically employed, the aim of which is maintaining a panel voltage that gives maximum power output.

When used in conjunction with batteries however, a simpler technique is connecting the panel directly to a regulated (or battery) bus, known as *direct energy transfer*. This technique minimises losses by avoiding an intermediate DC-DC converter (inherent to MPPT implementations), but the panel will almost always be operating sub-optimally if environmental conditions are constantly changing. Because the panels will either be operating at the battery voltage (battery bus topology) or a predetermined bus voltage (regulated bus topology), the panels will need to be sized to output this voltage at minimum power output.

To maintain this bus voltage, power will need to be shunted off at all other times. While both methods are ineffective in LEO with large and regular temperature swings, these topologies remain popular in systems designed for geosynchronous orbits where panels can be sized for a fairly-constant equilibrium temperature [26].

Given this inefficiency, the need for active MPPT presents itself. There exist a number of different methods and/or techniques; some of these are in widespread use, but each are suited to different applications and the relevant ones will be briefly discussed below. In addition to these 'standard' techniques, many authors have proposed variations on these with some of particular interest.

Constant Voltage

Simplest of the MPPT methods is the Constant Voltage (CV) method, which maintains a fixed panel voltage — usually some constant factor of the open-circuit voltage — such that:

$$V_{mmp} = kV_{oc} \tag{2.3}$$

By briefly interrupting the load V_{oc} can be measured, with the load then reconnected at the calculated V_{mpp}. While being very fast and simple to implement, the calculated operating point is approximate and does not factor in environmental conditions as previously discussed [18]. Constant Current (CC) is a similar method, although based on the relationship between I_{mpp} and I_{oc}.

Both of these methods suffer from the same disadvantage in that the load is periodically interrupted while V_{oc} is taken. If batteries are present this is usually not a problem but, if not, and including when the batteries have reached their End-of-Life (EOL) and can no longer hold charge, this would cause subsystems to continuously reset.

Perturb and Observe

A more robust technique calculates the panel's output power and then adjusts, or steps, the panel's operating voltage. The direction of the step is based upon the calculated power before the previous step — if output power is increasing, the direction remains unchanged; if power is decreasing, the direction is reversed. Known as the *perturb and observe* (P&O) method, its popularity has been attributed to its ease of implementation and relative low cost [27]. Similar to P&O is the *hill*

climbing method that, instead of adjusting the panel's operating voltage, adjusts the duty cycle of a DC-DC converter, thereby perturbing the current drawn from the array [28].

A fundamental drawback of this technique is the inherent oscillations around the peak power point [28]. To counter this, a variable-size step can be used that reduces the perturbations around the peak; such a method is proposed by [27]. Rapidly-changing levels of irradiance in certain applications will also pose a limitation, as discussed by [27], who goes on to reference proposed counter-measures including an optimised (or simply high) sampling rate, with a weighted comparison between multiple power readings. In its basic form, the technique can also suffer from becoming stuck on a local power maxima.

Incremental Conductance

The *incremental conductance* (IncCond) method exploits the shape of the V-P curve and the fact that the slope is positive for $V < V_{mpp}$, negative for $V > V_{mpp}$ and zero for $V = V_{mpp}$. Given the instantaneous panel parameters I and V, along with their time-derivatives ΔI and ΔV, the derivative of interest ${}^{dP}/_{dV}$ can be re-written in terms of said parameters and subsequently interpreted as [28]:

$$\begin{cases} \Delta I/\Delta V = -I/V & \text{at MPP} \\ \Delta I/\Delta V > -I/V & \text{left of MPP} \\ \Delta I/\Delta V < -I/V & \text{right of MPP} \end{cases} \tag{2.4}$$

For sufficiently-small increments, the inherent oscillations of the P&O method can be avoided by maintaining the operating point when $\Delta I = 0$. However, small increments subject the method to similar performance limitations in rapidly-changing conditions as was described for P&O. Esram [28] notes proposed implementations using a CV method to initially approximate the operating point that largely avoid these limitations.

Other Methods

Fuzzy logic-based and neural network controllers have also been seen in implementations; however, these controllers require complex design with parameters that are closely linked to the system configuration [28]. With a flexible and adaptive system the goal of this thesis, these methods will not be considered.

2.3.6 MPPT Implementations

With active MPPT, the operating voltage of the panels and of the system will differ, and thus a DC-DC converter is needed. This gives rise to two control loops, one controlling the operating point of the converter that maintains a fixed output current or voltage, and another loop controlling the operating point of the panel. Seeing that the converter is adjusting its duty cycle in order to maintain the desired output, it is fundamentally varying the current drawn from the input.

The voltage-current curve seen in Fig. 2.5 shows a steep drop in voltage as current increases past the knee. This suggests that unless fine control is available, the input voltage to the converter may suddenly and/or unexpectedly drop below its minimum operating voltage. In this case, the system may become unstable: as the converter shuts off, input voltage will increase, allowing the converter to function once again, but then repeating the cycle. This would result is oscillations around this point that may or may not reach some sort of equilibrium. For this reason, care should be taken to avoid such a situation.

2.4 Energy Storage

The *specific energy* of an energy storage medium refers to its energy per unit mass; this is an important metric in satellite applications where mass is a critical consideration. Energy density — the energy per unit volume — should also be considered, as space is also a crucial constraint.

The energy storage capacity of a given medium will inevitably diminish over time, with capacity degradation exacerbated through varying factors that depend upon the medium. *Cycle life* is a characteristic that is thus also important, and refers to the number of charge/discharge cycles the medium can sustain with a capacity that is useful to the system [29].

2.4.1 Battery Storage

Batteries are characterised by the electrochemical process that takes place during the storage and release of electrical energy. They are a combination of one or more (fundamental) *cells* — each cell consisting of two electrodes surrounded by an electrolyte — and can have varying terminal voltages or capacities by connecting cells together in series or parallel respectively [29].

Various different combinations of chemicals can be employed, and the specific combination of these chemicals is known as the cell or battery's *chemistry*. In terms of rechargeable batteries, lead-acid, nickel-based and lithium-based chemistries are currently prevalent with each suited to different applications. Lead-acid, nickel-based and lithium-based cells have specific energies around 30 Wh/kg, 50–80 Wh/kg and 100–150 Wh/kg respectively; from this metric, it is obvious why lithium-based batteries, or more specifically lithium-ion batteries, seem to have dominated rechargeable applications in recent times. While lead-acid batteries have a good cycle life (1200–1800 cycles is typical [29]), their low energy density does not make them feasible for space- or weight-constrained applications.

Before the advancements in Li-Ion batteries in the late 1990s, Nickel-Cadmium (NiCd) (pre-1980s) and Nickel Hydrogen (NiH_2) (1980s–1990s) were the predominant battery types used on satellites due to their comparatively-long cycle life

(> 1000 cycles), good performance at low temperatures and general ruggedness [2, pp. 650-651]. However, once Li-Ion batteries became more widespread and reliable, their far-superior energy density quickly made them an attractive replacement. Indeed, almost all the literature points to the use of Li-Ion batteries, with [2] describing them in 2011 as likely to become the preferred rechargeable battery for all spacecraft missions.

Li-Ion batteries have a subset type known as Lithium-Ion-Polymer, often abbreviated to Lithium-Polymer and LiPo. These employ a variation on the electrolyte used and the construction of the battery. From the clear advantages of lithium batteries over other types, only Li-Ion and LiPo batteries will be considered.

Lithium-Ion

Li-Ion batteries have a nominal terminal voltage of 3.7 V and can typically be charged to a maximum of 4.2 V. Over-charging them, allowing them to discharge too deeply or operation at high temperatures severely affects their ageing process. However, these limitations are overshadowed by their high energy density and a lifetime upwards of 1500 cycles should conservative operating conditions be maintained [2, 29]. Furthermore, a protection circuit is often built into the battery pack to ensure safe operating conditions [29].

In terms of charging, a CC/CV profile is required that sees the charging current taper off at a pre-determined float voltage. There are many ICs available from manufacturers such as Texas Instruments and Linear Technology that safely manage the charging of this chemistry. Note that Li-Ion is used here as an umbrella term for various differing Li-Ion technologies such as Lithium Manganese Oxide ($LiMn_2O_4$) and Lithium Iron Phosphate ($LiFePO_4$).

Lithium-Polymer

While there are chemical differences between LiPo and Li-Ion cells, one of the major and relevant differentiating factors between the two is in the battery's construction: very thin cells, a result of the polymer technology, allow for thin, flat batteries, as well as a battery moulded to a very specific shape. While this can be a major

advantage in certain applications, the chemical differences result in a cycle life, energy density and operating-conditions range that is slightly lower than that of Li-Ion batteries [29]. Furthermore, test results of a typical CubeSat LiPo battery that are included in [30] show them to have a significantly higher Equivalent Series Resistance (ESR) than that of a tested Li-Ion cell. This will have an impact upon the cell's ability to deliver high-current pulses.

That being said, *Clyde Space* seem to have found success in LiPo batteries with LiPo the only energy storage medium used across their various product offerings [1]. The popularity of Clyde Space's EPSs is evident amongst the reviewed CubeSat missions, although there is little independent data available on their success and/or performance over the full length of successful missions.

Cell Combinations & Charge Equalisation

To increase the storage capacity of a battery system, multiple batteries can be combined in series and/or parallel. However, variations within each battery mean that some form of charging regulator should be present to ensure each battery is charged correctly: Li-Ion batteries in particular are highly sensitive to over- and under-discharge which can lead to catastrophic failure [31].

In both series and parallel combinations, individual cells can have unequal terminal voltages as a result of variations in internal resistances and State of Charges (SOCs), as well as differences in the ambient temperature gradient during charge/dischange and natural age-induced degradation [31].

In a series combination, unequal terminal voltages can cause a cell to be overcharged if it tapers off at a voltage lower than the other(s). A cell could also be over-discharged if it was initially charged to a lower SOC than the other(s) [31]. To avoid damage to cells in this configuration, cell balancing circuitry (or a cell balancer IC) is usually used that ensures charge is equally distributed amongst mismatched cells.

Although careful matching of cells — in terms of SOC and other characteristics — can mostly avoid these complications, it does not mitigate the effect of variations in natural ageing, and slight temperature variations over thousands of cycles. Proper balancing of cells also contributes to improving their useful life [31].

2.4.2 Supercapacitors

Supercapacitors can be thought of as occupying the space between capacitors and rechargeable batteries; with energy densities in the range of 0.5–15 Wh/kg, they can be charged and discharged at extremely high rates while being able to withstand $\gg$ 100 000 charge cycles [29, 32]. Characterised by capacitances in the order of 1000 F, supercapacitors are however limited to terminal voltages of around one to three volts. Placed in series though, a more useful terminal voltage can be achieved and, as opposed to batteries, supercapacitors can be cycled through a 100% Depth of Discharge (DOD).

The need for the rapid charge and discharge of energy in hybrid vehicles has seen much development of supercapacitor technology in recent years, as evidenced by the abundant literature on the topic. They have also found use in space applications with the European Space Agency and NASA both investigating their applicability to space EPSs over the past decade [33, 34]. Barde [34] suggests that supercapacitors are however more suited to spacecraft pyrotechnics (burning of deployables' fuses), and assisting in power averaging for payloads that have large differences between their peak and average power requirements (e.g. radar and telecommunications payloads).

Flight Heritage

There appears to be little data on the actual performance of supercapacitors in space applications, with most of the available literature addressing their *potential* use in satellite EPSs. *TurkSat-3USat* was a 3U CubeSat built by the Istanbul Technical University that incorporated both a COTS EPS from Clyde Space and an EPS with supercapacitors as the storage medium, developed in-house, serving as a backup [35]. Unfortunately, reports suggest that the satellite went silent after one day of successful operation with no indication as to the cause of the failure [36].

A hybrid Li-ion and supercapacitor system for small satellites is also proposed by [30] as part of an investigation into its feasibility for deep-space CubeSat missions. After ground-based testing, they conclude that although no significant performance gains in energy storage are achieved over a standalone Li-ion battery system, there is a substantial peak current capability. This increase is attributed to the lower

impedance of the hybrid system, a result of supercapacitors having a much lower ESR than Li-Ion batteries; their included test data shows, at a temperature of -40^{o}C, ESRs of 10 mΩ, 100 mΩ and 1000 mΩ for their supercapacitor assembly, a standalone Li-Ion, and a standalone LiPo battery respectively.

2.5 Electronic Design and Failure Analysis

The EPS is known to be one of the leading causes of spacecraft failures: while Wertz [2, p. 807] suggests that the EPS is the most common system in a CubeSat to fail, Tafazoli [37], in a study of in-orbit spacecraft failures, concludes that the power system accounts for 27% of all spacecraft failures[2]. This is behind a 32% failure rate of the Attitude and Orbital Control System (AOCS). However, seeing that a spacecraft may well continue to operate with the loss of the AOCS albeit with reduced capabilities, a loss of the EPS would most certainly result in loss of the mission, and could thus indeed be argued to be the leading cause of satellite failure.

Tafazoli's study reviews data from 156 in-orbit spacecraft failures (i.e. discounting launch failures) that occurred between 1980 and 2005, and includes a few interesting statistics on EPS-related failures: In addition to a 27% failure rate of power systems, 45% of all failures are electronic-related, with a less significant 6% related to software errors. Software errors include erroneous commands sent to the spacecraft, along with programming errors within on-board software. Another significant statistic is that 48% of failures occur within the first year of operation which he postulates to be a result of inadequate ground testing. Finally, failure of the solar array is attributed to 49% of power system failures, and 22% a result of battery failure. Noted however is that solar array failure is predominantly due to failed deployment of external panels (arguably a mechanical fault rather than electrical), thus making the expected failure rate for body-mounted panels far lower.

These statistics highlight the importance of careful electronic design and perhaps a greater emphasis on reliability and redundancy than is currently practised.

[2]It should be noted that CubeSats started to appear only towards the end of this study (1980–2005).

2.5.1 Electronics Failures in Spacecraft

Failure of actual electronic components is a subset of electrical failures described above and deserves a closer analysis. In terms of the actual failure rate of individual parts, Sarsfield [38] states, in 1998, that component quality issues account for 11% of spacecraft failures. While outdated, what is notable is his assessment of the decline of this figure, down from 26%, over the period from the 1970s to the 1990s. Of more interest, however, is that the failure rate of standard commercial components/parts has reduced so dramatically, that it appears to be on-par with so-called 'space-rated' components [38, pp. 135-141]. Note that this is not referring to radiation-hardened versus unhardened parts, but rather the grade and screening of standard parts.

Nevertheless, it is evident that the selection of high-quality parts is paramount to improving the survivability of systems: even if standard-grade parts have a comparable overall failure rate to those that are mil-spec or even space-grade, the "time to first failure" is far more important than the Mean Time Between Failures (MTBF) [38, pp. 135-141].

The popularity of using COTS components in harsh operating environments with a high degree of risk could be linked to the creation, in 2005, of the Aerospace Qualified Electronic Component Standard (ANSI/GEIA STD-0002-1); this standard qualifies components to meet minimum requirements for use in aerospace and other rugged operating environments. Although adoption of the standard appears limited, Texas Instruments offers a so-called "Enhanced Products" range that qualifies components to meet this standard [39].

2.5.2 Radiation Effects

There are two separate radiation-induced phenomena that are spoken of, those being the prolonged effect of an electronic device within a radiation environment, and the direct effect that a single, highly-energetic particle can have on a device. The former is known as the Total Ionising Dose (TID), while the latter is referred to as a Single Event Effect (SEE) [12, 40].

Single event effects or phenomena manifest themselves primarily as Single Event Upsets (SEUs), Single Event Latchup (SEL) and Single Event Burnout (SEB) [2,

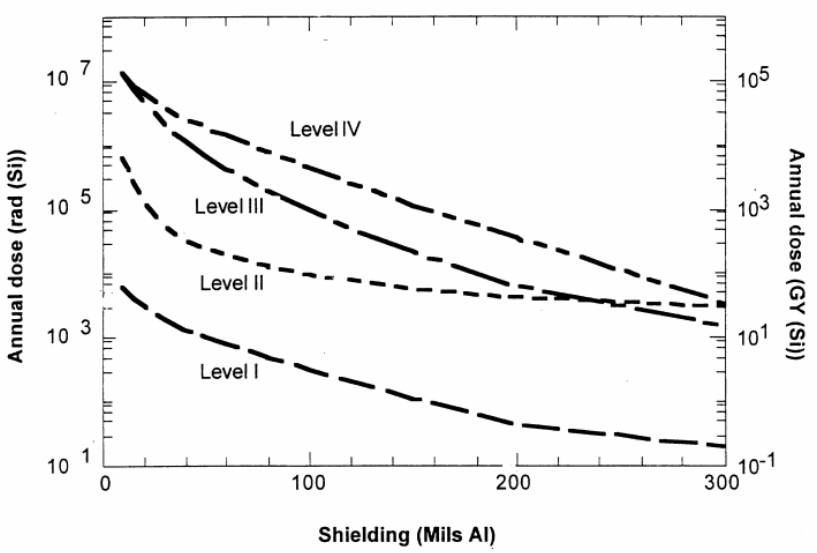


Figure 2.6: Annual total dose versus shielding for different qualification levels. Taken from [41].

p. 137]. SEUs are discussed within this section in relation to digital memory, while SELs and SEBs are discussed later on in their effect on MOSFET devices.

Survivability

An electronic device's survivability in a radiation environment is dictated by its radiation hardness, quantified by a total dose rating (typically measured in the non-SI unit *rad(x)* or *krad(x)*, where x is the material of interest, usually Silicon (Si)).

Although outdated, the IEEE Standard for Spaceborne Computer Modules [41] provides useful data on anticipated total dose levels as a function of shielding, expressed as an effective thickness of aluminium in the units mil. Avery *et. al.* [42] assume an effective shielding of 10 mil for a CubeSat with a weight-optimised structure that offers little shielding. Fig. 2.6 shows this graph of annual dose vs. shielding thickness for various qualification levels, with level I corresponding to a satellite in LEO at an altitude of < 500 km. The annual dose is stated to include contributions from all sources[3], made conservative through adding two times the standard deviation in the data and a safety margin of two.

[3]See Sec. 2.2.1

From Fig. 2.6, a total dose of 4 krad(Si)/yr should be allowed for, giving 10 krad(Si) as a good target for a typical CubeSat mission. This data also shows the exponential effect that shielding has on minimising the total dose requirements; however, excessive shielding is usually not feasible on a CubeSat with strict weight requirements. Furthermore, shielding is ineffective at blocking the very-high energy particles that cause SEEs [43] and thus the effects of radiation can never be entirely negated.

Single Event Upsets

SEUs correspond to a change in memory state in logic devices, also known as a "bit-flip". This phenomenon is most commonly associated with RAM (both DRAM and SRAM), but is also seen in non-volatile technologies such as flash and EEPROM [2, p. 608] [44]. SEUs are "soft errors" and do not result in permanent damage; however, the detection of errors is important to prevent runaway code and/or invalid control outputs.

The use of Error Correction and Detection (EDAC) is a common practice for mitigating the effects of SEUs. In microcontrollers, an EDAC implementation commonly relies upon Error Correcting Code (ECC), stored alongside blocks of data, that enable the detection and, potentially, correction of bit errors. The length of the ECC determines how many bit errors can be reliably detected, but one fewer error can ever be corrected than detected: eg., commonly seen is Single Error Correction, Double Error Detection (SEC-DED).

When a hardware EDAC is not available, there exist techniques to implement an EDAC in software (see eg. [45]). Hardware implementations are by far preferable however for reasons of complexity and efficiency [2, p. 609]. Furthermore, software EDACs will usually be unable to function on flash memories: seeing that microcontrollers would typically run the EDAC code out of flash, the architecture would need to allow for concurrent flash read and writes, or read-while-writes (RWW).

2.5.3 Points of Failure

Analysing the reliability of a system typically involves identifying single points of failure; although any component or aspect of a system *can* fail, it may not necessarily cause entire system failure. These failure points usually find themselves on single-string elements, those being components or subsystems that are relied upon for useful operation of the system. The concept of redundant strings then emerges, in which elements are placed in parallel (not necessarily in the electrical sense) to ensure backup functionality exists. Consideration does, however, have to be given to ensure failed redundant strings cannot have adverse effects on the remaining strings, thereby negating their purpose.

In addition to complete failure of a system element, partial failures may also occur. These might not cause direct failure of the system, but the combination of multiple partial failures, occurring over time, may indeed reduce system capabilities to the extent that it can no longer operate usefully.

2.6 MOSFETs in a Radiation Environment

Metal Oxide Field-Effect Transistors (MOSFETs) are universally used in power electronics and other switching applications; their high voltage and current-carrying abilities combined with very low 'on' resistance makes them close to ideal switches. Their use is further inherent to all CMOS ICs, encompassing practically every electronic device. However, their inherent semiconductor structure — that of layers of n- and p-type substrates — lends itself to radiation-induced effects: ionised particles, entering the device structure, mobilise electrons and create so-called 'holes' that can not only cause unintended operation, but also permanent damage [46].

The TID effects and SEEs cause different failure modes; while the full physics behind the interaction of ionised particles with the internal semiconductors is outside the scope of this work, a sufficient overview of the aforementioned failure modes, in order to make suitable design choices and predict system failures, is presented here.

2.6.1 Structure Types

The first MOSFETs were very low current devices, running in the order of tens of milliamps. It was only in the late 1970s that an introduction of a different internal structure allowed for MOSFETs with high current and voltage ratings, dubbed "power MOSFETs" [47].

A vertical structure characterised the first power MOSFETs (known as VDMOS or simply DMOS), which was a change from the lateral structure of the low-power MOSFETs. Different structure designs have subsequently evolved, with the most common being trench MOSFETs (UMOS or TMOS) and HEXFETs [47, p.159].

Galloway [48], in his review of radiation-induced degradation on UMOS transistors, notes similar failures to those of VMOS devices. He does however caution that enough is not yet known and further experimentation should be done. While this topic is not investigated here, this remains an interesting section to be explored in order to maximise reliability from non-hardened devices through choice of device structure[4].

2.6.2 Single Event Effects

MOSFET-related SEEs are almost always destructive events, occurring at any time within a system [43]. Of interest to a power subsystem are SEL, SEB and Single Event Gate Rupture (SEGR) effects; while SEL affects CMOS devices, SEB affects n-channel power MOSFETs (biased off) and SEGR affects both n- and p-channel power MOSFETs [43, 49, 50]. The inevitable use of these devices motivates a brief look at these effects and corresponding mitigation strategies.

Single Event Burnout

SEB is a catastrophic failure mode that sees a permanent short circuit forming between the drain and source. A heavy ion entering the device through the source (drain) of an n-channel (p-channel) MOSFET generates a transient current that

[4]This is further corroborated by [49] who states that failure mechanisms in MOSFETs may indeed be affected by different design, process and operating parameters.

triggers the parasitic BJT within; when the device is biased off, and thus blocking a high drain-source voltage, regenerative feedback causes the BJT's collector currents to increase to the point where secondary breakdown occurs, resulting in the drain-source short circuit [50].

Although done in 1996, [50]'s review of the literature at the time indicates that there are no reports of SEB occurring in p-channel MOSFET's, under normal operating conditions, with others making the same conclusion [43, 51]. [50] does however suggest that SEB *may* occur in p-channel devices, although far less probable than that for n-channel devices. This paper can be referred to for the specifics behind the reasoning.

Because the breakdown is a direct result of the available energy from the blocked drain-source voltage, it follows that low-voltage operation is not, or at least far less, susceptible to this failure mode. [51] notes a 28 V system voltage as the threshold for sufficient energy to be available for this failure to occur.

Single Event Gate Rupture

SEGR can also cause irreversible damage to MOSFET devices. As opposed to SEB that affects the drain-source path, SEGR is characterised by a localised breakdown in the gate oxide dielectric that results in a permanent short circuit between the gate and drain. The cause is heavy ions generating an accumulation of charge at the silicon interface at the gate-drain overlap region, that forms a high electric field across the gate oxide [50]. For short breakdown times the device may recover, albeit with degraded performance. An event of this nature is known as Single Event Gate Damage (SEGD) [51].

A summary of mitigation strategies is provided by [51], who states that this failure mode is influenced by both drain-to-source voltage and gate-to-source voltage. Low voltage systems are said to be practically immune to this as well as SEB, provided that appropriately-rated parts are used. It is suggested that in terms of biasing, the gate voltage should ideally be limited to the voltages used by manufacturers to specify turn-on and turn-off times.

Single Event Latchup

SEL is a well-known failure mechanism that is prevalent in CMOS devices: resulting in either so-called soft errors or — more seriously — device destruction, latchup is characterised by a sudden increase in current through the inadvertent triggering of parasitic BJTs inherent to the CMOS structure. These BJTs form an *n*-*p*-*n*-*p* structure that can be modelled as a Silicon Controlled Rectifier (SCR); once triggered, current will continue to flow until the device's supply is removed (or dropped below the holding voltage V_H) and, unless this current is limited, the device may quickly burn out [43, 52, 53].

The mechanisms that cause latchup are of interest. Even in terrestrial applications latchup is a well-known issue; terminal over-voltage and improper grounding, resulting in input pins being driven below the device's ground, are key causes [54]. However, the risk of the condition occurring is minimised not only through proper PCB layout, but also through internal IC design techniques; the preventative measures taken are outlined in detail in application notes from many manufacturers (see eg. [54, 55]).

Of particular concern to space applications is the risk of ionising particles triggering the intrinsic SCR. While the best approach to avoiding latchup in such environments is to use radiation-hardened parts that are not prone to latchup, [53] notes that this is often not possible due to a lack of such parts that meet the performance requirements of the system. Furthermore, even hardened parts are not fully immune.

Making use of techniques that remove power from a latched-up device can avoid catastrophic damage, although [53] does caution that latent damage to internal device traces can occur, and indeed has been observed through studies. Such damage is said to reduce the lifespan of the affected device.

One strategy, to avoid catastrophic damage, is to use a series resistor in the V_{cc} line that limits the current through the device should a latch up condition occur. With a large increase in current, the corresponding drop in voltage will often allow the latch up condition to clear when the supply voltage drops below the holding voltage. This approach does, however, have limited use for large-scale integration as a useful operating current must be maintained; device supply current is inherently restricted by the addition of such a resistor.

2.6.3 Total Dose Effects

TID effects have a different failure mechanism to SEEs; while SEEs can occur at any time and are largely unavoidable, TID effects only occur after prolonged exposure to ionising radiation. These effects will thus only present themselves after a period of time within the radiation environment and, as such, TID effects can, to an extent, be designed for and anticipated.

The primary and most widely-documented total dose effect, related to power MOSFETs, is that of the shift in the threshold voltage. Other significant effects are an impact on the breakdown voltage and a reduction in maximum device current.

In short, these effects are all thought to be a result of positive charge developing in the gate oxide, along with the formation of interface traps[5] [56, 57]. In n-channel devices, these traps contribute negative charge at the oxide-silicon interface, exacerbating the effect over comparable p-channel devices [56].

Threshold Voltage Shift

Ma [46, pp. 37-38] provides a detailed explanation on the formation of the aforementioned interface traps, how they contribute to accumulation of charge and how they influence device operation. Important to note is that for n-channel devices, the gate threshold voltage ($V_{g_{th}}$) is lowered and thus a smaller voltage is needed to turn the transistor on. Similar but opposite, the effect is not as severe for p-channel devices.

From Fig. 2.7 it can be seen that for total doses in the order of 10 krad, the shift for n-channel devices is far more pronounced than for p-channel devices; these see a negligible shift.

If radiation exposure is ceased a process of annealing takes place, during which the threshold will usually recover to the pre-irradiance level and, in some cases, surpass it [56]. Schrimpf [56] notes that, for very low dose rates, the annealing process can, in fact, take place concurrently. This has the potential to result in a net increase in

[5] Interface traps are electrically active defects located at the interface between oxide and semiconductor. They are capable of trapping and de-trapping charge carriers, having an adverse effect on device performance.

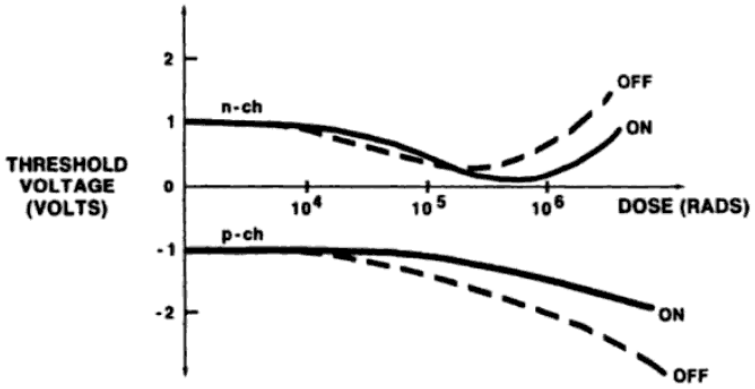


Figure 2.7: Plot showing the threshold voltage of n- and p-channel MOSFETs as a function of radiation dose, for devices biased 'on' and 'off' during irradiation. Taken from [46, pp. 39].

the voltage threshold. Their results point to this effect only observed in radiation-hardened devices, a phenomenon they attribute to a thicker gate oxide typical of such devices. For unhardened parts, their results suggest a negative shift for all dose rates.

Other Effects

The drain-source breakdown voltage (BV_{DS}) is another parameter that is affected by TID and is thought to have the same cause as the threshold voltage shift [57]. Blackburn [57] shows this effect to be highly dependant on V_{DS} with a decrease in the order of 5 V for a total dose up to 10 krad(Si) at $V_{DS} < 20$ V.

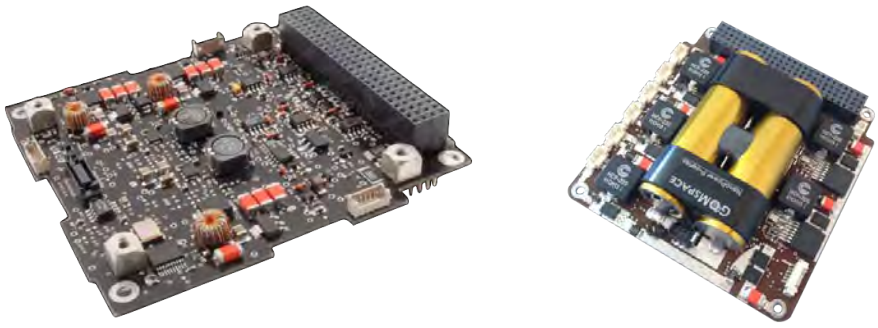
With particular reference to space-based switching power supplies, Wahle [58] concludes that threshold voltage shift and reduction in channel mobility (a function of interface traps) are the dominant factors to consider when designing such a system: both effects lower drive capability and operational speed and thus must be taken into account when selecting power MOSFETs.

Chapter 3

Existing Systems

The following chapter looks at the features and design of commercial EPS modules from two major manufacturers, Clyde Space and GomSpace. Together they have significant flight heritage and great commercial popularity — in fact, as was seen in the previous review of South African CubeSat work, the Clyde Space modules are currently the preferred modules for local satellite development.

A close look at their design, scalability and configuration options will give insight into current design techniques and industry expectations.



(a) (b)

Figure 3.1: CubeSat EPS modules available from (a) Clyde Space and (b) GomSpace.

3.1 Clyde Space

Clyde Space offer a wide range of CubeSat-specific modules, from EPSs to de-orbit devices. Their modules are all "plug-and-play", are compatible with CubeSat Kit, and have a certain level of customisation that is done before leaving the factory. At the time of writing a new generation of their EPSs has been released, but little data on them is currently available. However, it appears that changes are limited to small design improvements with a few noticeable capabilities added. While this section's discussion is aimed at their previous generation modules, these new capabilities will be noted later on.

The company states that they have sold over 400 CubeSat EPS modules to date, and further claim that their product is used in over 50% of all CubeSat missions. This is a significant statistic and thus a close examination of their specifications, capabilities and compatibility would be hugely beneficial.

3.1.1 EPS Modules

Clyde Space's EPS range includes modules suitable for 1U, 1.5U, 2U, 3U, 6U and 12U CubeSats with the major differences being the number and power ratings of the input stages. The modules all retain the same basic design and block diagram elements.

The 1U, 1.5U and 2U modules allow for up to two integrated LiPo battery packs to be connected via daughter boards that provide 10 Wh or 20 Wh of capacity (one or two battery packs respectively). The 3U module offers higher output current capabilities along with input stages optimised for larger, and possibly deployed, panels.

Although similar to the 3U module, the 6U and 12U-suitable modules come as one flexible module but with even higher power capabilities and the option for a further three input stages through a daughterboard. An external battery module is required for the 3U+ modules, that is interfaced to via the CubeSat Kit header.

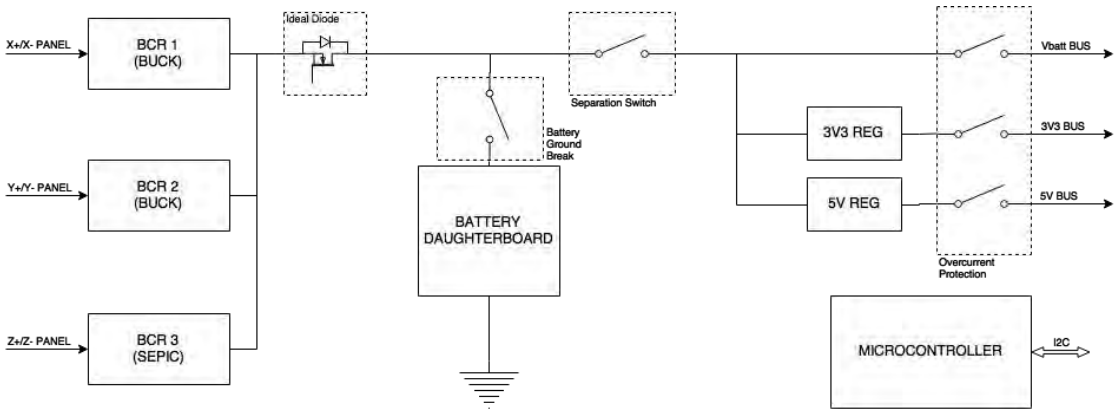


Figure 3.2: Block diagram of the Clyde Space 1U CubeSat EPS. Adapted from [59].

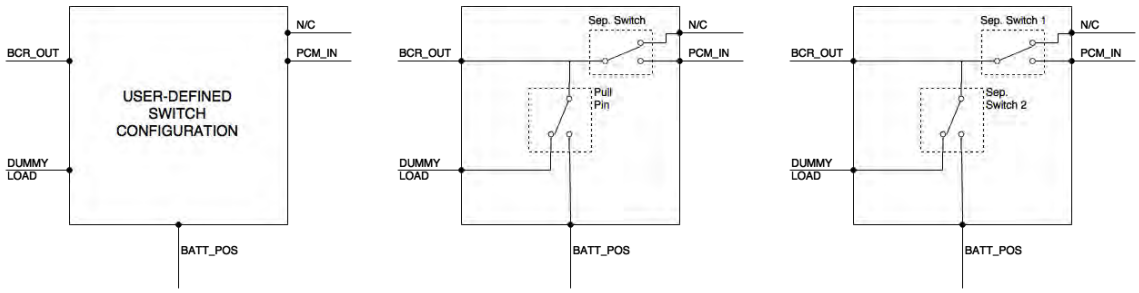
3.1.2 System Design

The system block diagram in Fig. 3.2 is specific to the 1U module but is representative of their entire range. As noted, the 3U+ modules do not allow for the battery daughterboard and instead rely upon an additional module. Their 6U+ flexible module uses a daughterboard to add three further input stages.

At a high level, they use a battery bus topology with MPPT. The battery bus has direct connection to one or more dual-LiPo cell series strings, with buck and SEPIC regulators used to perform MPPT on each of the panel inputs. Direct connection to a two-cell series LiPo string means that the bus voltage varies between 6.2 V and 8.26 V. The battery bus also provides power to the power conditioning module (PCM), used to generate 3.3 V and 5 V system voltages. Some of the modules have an additional 12 V regulator.

Input Stage

Depending on the number of series solar cells expected, the input stages use either a buck- or SEPIC-based battery charge regulator (BCR), with an appropriate power rating for the size of CubeSat. The BCR performs the maximum power point tracking with no microcontroller intervention. The input stages' outputs are directly combined to form the battery bus. At this point a configuration option exists, as seen in Fig. 3.3.



(a) (b) (c)

Figure 3.3: Switch configuration options for Clyde Space's EPS modules. (a) External interface connections, (b) configuration option 1, and (c) configuration option 2. Adapted from [59].

The Battery Bus

The implementation of switches between the battery bus input (BCR_OUT), the battery positive terminal ($BATT\_POS$) and the input to the PCM (PCM_IN), is left to the user, with these pins brought out on the CubeSat Kit header. A separation switch is always required at the input to the PCM to ensure that the CubeSat remains completely powered off during launch.

They do however suggest two options for the connection of the battery to the battery bus: either a Remove Before Flight (RBF) pull-pin or, if two separation switches are available, connection to this second switch. Whether the battery remains disconnected only while on the ground or up until the point of deployment is the only difference between these options.

Power Conditioning and Distribution

Two buck regulators are used to generate 3.3 V and 5 V buses with varying output current capabilities (see Table 3.1); they both operate at 500 kHz with a stated efficiency of 95%. Each regulated bus, along with the battery bus, has overcurrent protection: in the event of an overcurrent condition, the line is switched off for around 500 ms before resetting. It is unclear whether this is implemented purely in hardware or requires software control.

The modules thus have three current-limited outputs; these can be connected di-

rectly to subsystems or used by a separate power distribution module to provide individually-switched outputs to subsystems.

The latest version of their EPS includes ten integrated output channels that can be assigned to different subsystems. Each output incorporates a 1 A Latching Current Limiter (LCL) that turns the output off if the current draw exceeds 1 A for a preset time (1–20 ms). It appears that the microcontroller is used to trigger a reconnect attempt.

Telemetry

The on-board microcontroller is configured as a simple I^2C node that responds to some pre-defined commands. Besides providing some basic status information, the node can also respond with ADC channel readings that include:

- Array voltages and currents;
- Battery full voltages, currents, cell temperatures and charging/discharging state; and
- Regulated bus currents.

The microcontroller, an analogue multiplexer and an I^2C buffer, are said to be the only significant components that are not a part of the power path, drawing a quiescent power of 100 mW.

3.1.3 Discussion

The buck and SEPIC input stages (depending on solar array configuration) introduce the main inefficiencies in the power path: with maximum efficiencies of 92% and 80% respectively, these figures are, however, typical of the respective switching topology. In addition, these regulators have in-built maximum power point tracking using a constant-current method. An external comparator circuit switches the regulators to a constant voltage output once the present battery float voltage is

Table 3.1: Specifications for the Clyde Space range of EPS modules.

Model	**Input Stages**	**Integrated Batt.**	**Buses**	**Outputs**	**Cost (USD)**
CS-1UEPS2-XX [1]	3 x 3 W SEPIC	10 Wh or 20 Wh optional [2]	3V3 @ 1.2 A 5 V @ 1.5 A V_{batt} @ 4 A	None [3]	3 650
CS-1.5UEPS2-XX [1]	3 x 4.5 W SEPIC	10 Wh or 20 Wh optional [2]	3V3 @ 3 A 5 V @ 3 A V_{batt} @ 6 A	None [3]	4 150
CS-3UEPS2-NB	2 x 8 W buck 1 x 3 W SEPIC	None [4]	3V3 @ 4 A 5 V @ 4 A V_{batt} @ 6 A	None [3]	4 900
CS-3UEPS3-NB	2 x 12 W buck 1 x 3 W SEPIC	None [4]	3V3 @ 4.5 A 5 V @ 4.5 A 12 V @ 1.5 A V_{batt} @ 4.5 A	10 @ 1 A with LCL	6 700

[1] XX is NB, 10 or 20 for no battery, 10 Wh int. battery and 20 Wh respectively.
[2] Each 10 Wh of capacity adds USD 1000 to the cost.
[3] A 24-channel Power Distribution Module can be added to the stack for an additional USD 8450.
[4] External 10 Wh, 20 Wh or 30 Wh battery modules can be added for USD 1800, USD 2850 and USD 3850 respectively.
[4] External 10 Wh, 20 Wh or 30 Wh battery modules can be added for USD 1800, USD 2850 and USD 3850 respectively.

Data obtained from [23].

reached. There do not appear to be diodes after each input stage but rather one ideal diode; this prevents current leaking into the input stages during eclipse.

Reliance upon external implementation of a separation switch allows for added flexibility, although does come with a few disadvantages:

- If a purely mechanical switch is used, there exists the possibility for mechanical failure;
- If a (latching) solid-state switch is designed by the end user, reliability of the entire system is affected through this single-string element that may not be optimally designed; and
- Power losses and single points of failure are introduced through external routing of the main power flow.

Strings of two LiPo cells (in the form of daughterboards and external modules) are used in a direct parallel configuration. There is no mention of cell balancing and all strings are charged using the same CC/CV output from the combined BCRs used in the input stages. Each battery does, however, have a current limiter (in

the form of a resettable fuse) and a current sensor that provides telemetry to the motherboard. In addition, each battery has a heater and thermostat that can maintain cell temperature above 0^oC.

This approach also has both advantages and disadvantages: while losses are avoided (through minimal components) between each battery and the battery bus, degradation or the failure of any single cell will induce a drain upon the remaining functional cells. Furthermore, with only a combined battery bus voltage reading available, it is difficult, if not impossible, to estimate the state of capacity and/or health of individual cells and strings. They state that if all battery strings fail, the system will continue to operate intermittently with a regular 2.5 s interruption of the power buses due to the MPPT implementation.

The latest version of their module has the noticeable addition of ten current-limited outputs. An overcurrent condition on any given output, that exceeds a preset time threshold, causes the output to latch off. Available data shows that the microcontroller is used to attempt to reconnect the output: while allowing flexibility with the timing elements of the latching and reconnecting process, any failure of the microcontroller could result in a subsystem being permanently and unnecessarily turned off.

3.2 GomSpace

GomSpace, a Danish company specialising in CubeSat subsystems, offers a comparable, albeit more limited, range of EPS modules. In terms of functionality they appear very similar to those of Clyde Space, although there are a few noticeable differences.

Mention of their modules amongst published papers is far less frequent than that of Clyde Space; however, their position as the only other major player in the commercial EPS market, justifies a discussion of their systems.

3.2.1 EPS Modules

In contrast to the wide variety of Clyde Space modules, Gomspace offers only two modules with the differentiating factor being the battery bus voltage: the P31u has a two series cell configuration, while the P31us uses four series cells for nominal battery bus voltages of 7.4 V and 14.8 V respectively. Additional battery modules are available; the higher-power P31us relies upon these external modules, but the P31u includes two Li-Ion cells integrated onto the module.

3.2.2 System Design

The system has almost identical design elements to the Clydespace system, as can be seen in the system block diagram in Fig. 3.4.

Input Stage

The input stage consists of three boost regulators, accepting solar inputs in the range of 4.2–8.5 V. The onboard microcontroller is used to set the regulators at a constant-voltage operating point, or to implement active power point tracking.

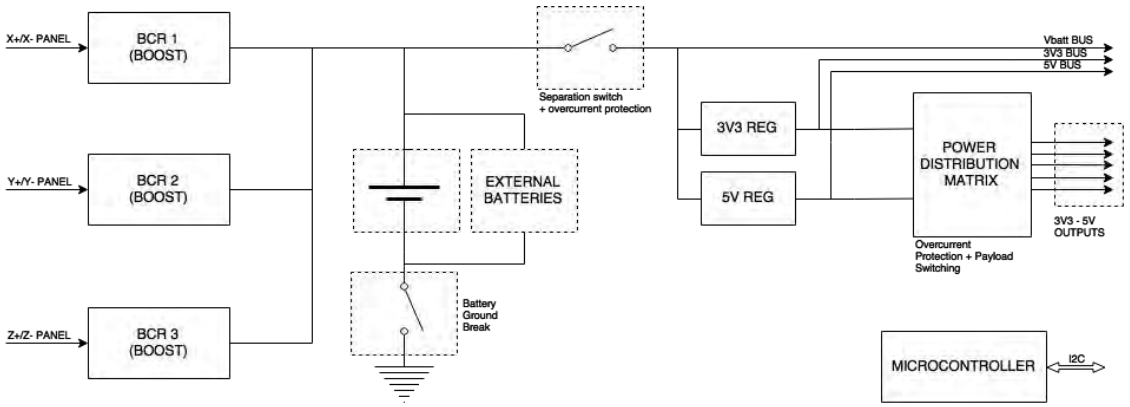


Figure 3.4: Block diagram of the Gomspace CubeSat EPS. Adapted from [60].

The Battery Bus

Once combined, the output of the regulators form the battery bus that has direct connection to the Li-Ion strings. The separation switch takes the form of a solid-state latching circuit that requires a brief pulse to switch and remain on. Overcurrent protection for the bus is implemented through microcontroller monitoring of the bus current; if the threshold is met, the bus is turned off for 100 ms. The low-level implementation of this is unclear.

Power Conditioning & Distribution

The battery bus and regulated 3.3 V and 5 V buses are brought out on the CubeSat Kit header as "always on" outputs. In addition, both the GomSpace modules include six outputs with latching current limiters. These limiters operate such that an overcurrent condition (0.5–3 A) will cause the output to be cycled for a brief period (< 28 ms); if the condition persists, the output is cycled for progressively longer periods. Each output can be configured to default on or off.

Telemetry

An onboard microcontroller gathers telemetry and performs housekeeping, while also controlling the input regulators and output switches. A fairly elaborate command system, via the I^2C interface, allows for retrieval of housekeeping data and configuration of various options.

Table 3.2: Specifications for the Gomspace range of EPS modules.

Model	Input Stages	Integrated Batt.	Buses	Outputs	Cost (EUR)
P31u	3 x 8 W boost	19.2 Wh [1]	3V3 @ 5 A 5 V @ 4 A V_{batt} @ 12 A	6 @ 3 A with LCL	3 800
P31us	3 x 17 W boost	None [1]	3V3 @ 5 A 5 V @ 4 A V_{batt} @ 12 A	6 @ 3 A with LCL	5 550

[1] Additional 38.4 Wh battery module available @ EUR 2450.
Data taken from [60].

3.2.3 Discussion

Similar in design to the Clyde Space EPS, the Gomspace EPS enjoys many of the same advantages, but also suffers from the disadvantages.

The boost input regulators are able to achieve efficiencies up to 95% and have three power point tracking options: a hardware-set default operating point, a software-set constant-voltage operating point, or microcontroller-controlled active maximum power point tracking.

Implementation of battery charging is almost identical to that of Clyde Space, with two- or four-cell Li-Ion strings that are charged directly from the battery bus. Battery heaters also allow battery temperature to be maintained above a preset temperature.

An onboard latching kill switch is a noticeable difference: a brief trigger, requiring that only a small current is sent through the separation switch(es), will cause it to latch on. This implementation increases both reliability and efficiency. For handling and testing purposes, a reset input is available to release the latch.

Bus overcurrent detection relies upon constant monitoring of bus current by the microcontroller; an overcurrent condition will see the kill switch turned off for 100 ms which effectively shuts down the entire satellite. A drawback to this is a dependency on a working microcontroller.

The latching current limiters on each of the six outputs also suffer from the microcontroller being a single point of failure: subsystems may be left switched off, should it not operate correctly.

Chapter 4

System Design

The previous two chapters outlined a few important aspects that need to be taken into account when designing this EPS. In summary, these are:

- Being a leading cause of satellite failure, the system will need to be designed with reliability being a key factor;
- The popularity of existing commercial systems means that the system will need to offer compatibility and comparable features and functionality; and
- The module must be flexible enough to suit a variety of different mission needs.

With past and future CubeSat projects from Stellenbosch University and the Cape Peninsula University of Technology ranging from 1U to 3U in size, flexibility should allow for a corresponding range of power requirements.

This chapter aims to establish a set of specifications, along with a complete high-level block diagram, to allow schematic-level design. Individual components will not be identified although a microcontroller will be chosen, given the very specific requirements and its associated implications.

4.1 Specifications

These specifications and features are preliminary; additional features may be added as the design process evolves, and specifications may change somewhat as practicalities are taken into account. A final set of specifications and features can only be established once testing is complete.

4.1.1 Energy Storage

In order to match the offerings of the integrated modules from both Clyde Space and GomSpace, the EPS should have the ability to include up to 20 Wh of on-board storage capacity. In addition, particularly in the case of batteries, it should be possible to completely isolate the battery to avoid self-discharge during the characteristically-long storage and transportation periods that CubeSat missions endure.

It should also be possible to expand the storage capacity through additional modules. This allows for great flexibility and would be in line with current offerings.

4.1.2 Separation Switch and Bus Protection

The inclusion of an integrated latching separation switch should ensure that the EPS, and by extension the entire CubeSat, remains off during launch as per launch operator requirements. A brief pulse from an external separation switch, triggered by the release from the deployment mechanism, should turn this switch on. There should be no expectation that this mechanical switch will remain closed; the only reliance should be upon a brief, one-off pulse.

In addition, a Remove Before Flight (RBF) pin, implementing a normally-open switch (with normal considered to be the pin removed), should prevent the switch from latching for handling purposes; the pin is expected to be removed only after the CubeSat has been securely placed in the deployment mechanism. A normally-open switch ensures that a mechanical connection is only needed when on the ground.

The main power bus should further be current-limited with an overcurrent condition causing the bus to cycle off, to allow the fault time to clear. This 'off' period would need to be hardware-set and should be around 500 ms. The ability for the microcontroller to trigger such a reset would be beneficial.

4.1.3 Power Capabilities

The power handling capabilities affect not only component ratings and specifications, but also the physical PCB trace requirements. Calculation of the power budget is not required, and it can be assumed that solar panels will be appropriately sized for the orbital parameters and satellite requirements.

Input Stage

A typical Gallium Arsenide (GaAs) triple-junction solar module, physically sized for a 1U face, is rated for 2.4 W maximum power output in LEO [61]. It is assumed that there will exist a maximum of three such modules per array, corresponding to a 3U CubeSat face, although the actual configuration of the array is not specified. It is also assumed that there will be no deployable panels and that all panels are fixed to the CubeSat faces. The final design may, however, allow for deployable panels, depending on achievable power capabilities.

Output Stage

5 V and 3.3 V regulated buses should be able to provide peak currents of 5 A, with average currents expected to be much lower. Six outputs should be integrated into the module; each output should have a selectable output voltage and a latching current limiter (LCL).

The LCL should be implemented in hardware and function such that overcurrent conditions cause the output to be switched off, with automatic reconnection after 500 ms. A microcontroller could provide additional functionality, such as an adjustable off-period. This implementation would allow fully-autonomous operation

that does not rely upon host software, but rather uses software control to provide optimisations.

4.1.4 Interfaces

Besides needing an interface through which the module can be programmed and debugged during development, the module needs to be able to communicate with other subsystems. However, an important design goal is to ensure the EPS is not dependant upon successful communication once in operation: any node connected to the bus has the potential to break communications and would otherwise become a point of failure for the EPS.

Inter-subsystem Communication

An inter-integrated circuit (I^2C) bus is currently the CubeSat Kit standard for inter-subsystem communication. A master node on the bus would request telemetry from the EPS for downlink, and may command it to perform certain functions. There is no prescribed functionality or telemetry that the EPS must provide; however, system currents and voltages should be provided at a minimum, along with the ability to turn subsystems on and off.

A standard for the format of data packets and commands also appears to be absent. It is left to custom mission software, usually running on a processor on a dedicated "motherboard" module, to request and interpret such data packets to prepare and queue for downlink. This processor would also then issue commands on an ad hoc basis.

Available commands and housekeeping data can thus be defined once hardware design is complete, although it will be important to properly document all functionality.

Controller Area Network

Controller Area Network (CAN) is a communications bus that has been popularised through its use in automotive applications. Designed specifically for multi-nodal networks, CAN uses a message-based protocol with an arbitration field that allows both prioritisation and identification of messages. A differential pair at the physical layer, along with Cyclic Redundancy Check (CRC) built into the standard, makes it particularly suitable for noisy environments and high-reliability applications. CAN is seeing increasing use in spacecraft [62] [63], and it is likely that it is these attributes driving it.

The true bus topology that alleviates the need for a master node and allows subsystems to seamlessly communicate with one another, reduces the probability of a single point of failure. Although the bus is not yet supported by most COTS modules, it would be beneficial to include the capability, to allow for development and future compatibility.

Programming & Debugging

The programming interface will depend on the chosen microcontroller. In addition to this though, there should be a way for the mission design team to perform high-level debugging, testing and configuration. Such an interface could be a simple serial port, but should have additional functionality to allow for the triggering and resetting of the separation switch, as well as the charging of batteries.

4.2 Energy Storage Design

The method of energy storage is a relatively fundamental design feature: it will dictate system bus voltages and thus the types of regulators needed, as well as influencing other design elements.

Secondary batteries and supercapacitors, charged via solar arrays, were outlined as being the only energy storage methods feasible for CubeSats in LEO. In terms of secondary batteries, only Lithium Ion and Lithium Ion Polymer batteries will be considered for their many advantages over Nickel-based batteries.

4.2.1 Supercapacitors vs. Lithium-based Batteries

Supercapacitors are relatively new to satellite applications and have little flight heritage; in fact, there does not appear to be any in-orbit data for them, and it is unclear whether there exist any successful satellites powered purely off a supercapacitor array. In designing a high-reliability system that should inherently use flight-proven technology, this is already a major drawback. However, there exist a few more fundamental issues that will be shown here.

The typical capacity for a space-qualified Li-Ion 18650 cell — measuring 65 mm in length and diameter 18.5 mm — is 2600 mAh [64]. With an average terminal voltage of 3.7 V, this gives a total energy capacity of:

$$E = 2600 \times 3.7 = 9620\,\mathrm{mW\,h} \tag{4.1}$$

Weighing approximately 45 g, this gives an effective specific energy and energy density of 214 Wh/kg and 551 Wh/L respectively. Larger batteries (ie. not in the 18650 form factor) may well achieve better specific energy and energy density figures; however, such a cell is a likely candidate for a CubeSat due to their convenient size and the relative ease of sourcing space-qualified versions.

These are best case figures that assume full discharge (100% DOD) and a BOL capacity. Over a typical two-year lifespan of a CubeSat however, experiencing 16 orbits per day or 5 840 total charge/discharge cycles, the effects of cycle life need to be taken into account.

Table 4.1: Specifications for the BCAP1500 Maxwell supercapacitor.

Capacitance	1500 F
Initial Maximum ESR_{DC}	0.47 mΩ
Rated Voltage	2.7 V
Absolute Maximum Current	1150 A
Operating Temperature	-40– +65^{o}C
Weight	280 g
Length	85 mm
Diameter	60.7 mm

Data taken from [65].

Data given in [64] suggest that reducing the end of charge voltage (EOCV) to 4.1 V and restricting the DOD to 15%, will see capacity drop by 65% after 4 200 cycles. A very conservative DOD of 10% would thus provide a more realistic specific energy and energy density; such a DOD effectively reduces the available capacity to 260 mAh, giving 21 Wh/kg and 55 Wh/L respectively.

Being able to withstand many thousands of charge/discharge cycles, cycling at 100% DOD whilst seeing a negligible drop in capacity, is one of the main advantages of supercapacitors that negates the need for such dramatic capacity derating. However, their characteristic low terminal voltage influences the actual energy that can be stored.

A search of online component distributors shows a very limited range of supercapacitors suitable to the size constraints of a CubeSat. Nevertheless, it will be assumed that the following parameters used, taken from the datasheet for the Maxwell BCAP1500 and shown in Table 4.1, are representative of what could be expected from a potential device with a suitable form factor.

Given a maximum terminal voltage of 2.7 V and making the unrealistic assumption that a boost regulator could extract all the stored energy (operate down to an input voltage of 0 V), the total stored energy is given as:

$$\begin{aligned} E_{stored} &= \frac{{}^1\!/_2 CV^2}{3600} \\ &= 1519\,\mathrm{mW\,h} \end{aligned} \tag{4.2}$$

This equates to a respective specific energy and energy density of 12.4 Wh/L and 5.4 Wh/kg. The minimum operating voltage for a suitably-sized boost regulator would need to be taken into account, and would result in some loss of available energy storage. While using series combinations would allow for a more usable terminal voltage range, the energy density can never improve.

Where supercapacitors trump any available battery is in their power density — a high maximum current rating combined with an extremely low ESR, allows them to output considerable power in the order of kW/kg. For payloads with brief but high power demands, this is a significant advantage.

Conclusion

Lithium-based batteries are by far the most widely-used storage medium in nanosatellite power systems; it is a flight-proven technology with multiple vendors of space-qualified products. The fact that the maximum lifespan of a typical CubeSat is two years — a result of radiation-induced degradation of electronics and natural orbital decay — means that their decreasing capacity can be adequately designed for through appropriate derating. As shown, conservative derating still results in a energy density close to five times that of supercapacitors. In a CubeSat with such stringent mass and space constraints, these densities become deciding factors.

The effectively limitless lifespan that supercapacitors enjoy should not be overlooked, but this is perhaps more advantageous in a satellite power system designed for a lifespan of five or more years. Such a satellite would undoubtedly be much larger than a CubeSat, have more relaxed space constraints, and thus be able to accommodate sizeable capacitor banks. A communications satellite, typically designed for a long lifespan, would likely also take advantage of their high power density for short, high-current power draws.

For CubeSats with minimal power requirements — such as one drawing an average power of $\ll 1$ W — a single supercapacitor may well provide sufficient and reliable energy storage; however, it is suggested that before designing such a system, more data on the performance and reliability of supercapacitors in space be established. A hybrid system, where batteries either co-provide power or simply act as a backup, would be beneficial in this regard. Using supercapacitors as the primary energy

storage medium in higher-power CubeSats remains impractical though, and are thus not compatible with the design goals.

When choosing between Li-Ion and LiPo batteries, the choice seems open: GomSpace use Li-Ion cells for their modules, and Clyde Space use LiPo cells but also offer Li-Ion cells. Both variations thus have flight heritage and have been proven to be reliable in space applications. However, Li-Ion offer a few advantages including lower internal resistance and a marginally-improved cycle life. Although LiPo cells have more flexible form factors including incredibly thin profiles, this is not seen to be a crucial advantage unless marginal space constraints become a deciding factor.

For these reasons, Li-Ion cells will initially be used. Indeed, their identical charging profiles and similar characteristics means they could be interchanged at a later stage, should it become necessary. Depending on the battery bus configuration, it may even be possible to use a combination of the two.

4.2.2 Battery Configuration

The common topology seen on commercial EPSs is to place two cells in series for a 7.4 V nominal battery bus. Total capacity is increased through the addition of these two-cell strings, directly in parallel, with no separate charge management per string. There also appears to be an absence of cell balancing circuitry, but it is claimed that cells are carefully matched through a variety of screening tests [66]. Charge management is performed at the bus level via the battery charge regulators used for each solar input (see Figs. 3.2, 3.4).

Such a design has a few advantages: Firstly, power transfer efficiency between the bus and the batteries is maximised. Secondly, having only passive components between the batteries and bus, ensures that this connection is immune to radiation effects. The final advantage is the simplification of battery management: the BCRs limit current and restrict the maximum bus voltage (and thus maximum terminal voltage), and no further interaction is required by the host.

There are some significant disadvantages though, that relate to the failure of one or more cells. Battery failures were already stated to account for an estimated 22% of EPS failures; that is, one in five power system failures are attributed to the battery.

Consequently, their failure modes should be carefully scrutinised.

If one cell in a two-cell string degrades faster than the other, it will become stressed through overcharging and may fail catastrophically. Furthermore, if parallel strings exist, this weaker string will be a drain upon the functional string(s). Finally, if a cell fails as a short circuit, there is no way to isolate it from the pack and it will thus likely prevent the system from operating.

Many of these problems can be avoided through careful matching of cell internal resistances and capacities, and ensuring that they are at an equal SOC before connecting. However, such stringent matching criteria can only add significantly to their cost, and there is no guarantee that a screened cell won't exhibit irregularities after some time in operation.

A Single-Cell String Configuration

While the above described configuration clearly has some advantages and has found its way into commercial systems, it is hard to justify it over a simpler single-cell configuration. In addition to avoiding the need for cell balancing, a single-cell configuration also allows any number of cells — not necessarily a multiple of two — to be used. A more subtle advantage that comes with a lower bus voltage is some gain in regulator efficiency, through the unregulated bus voltage being similar to those of the 3.3 V and 5 V regulated buses, particularly at light loads. However, this may be somewhat negated by the increased I^2R losses along the bus path.

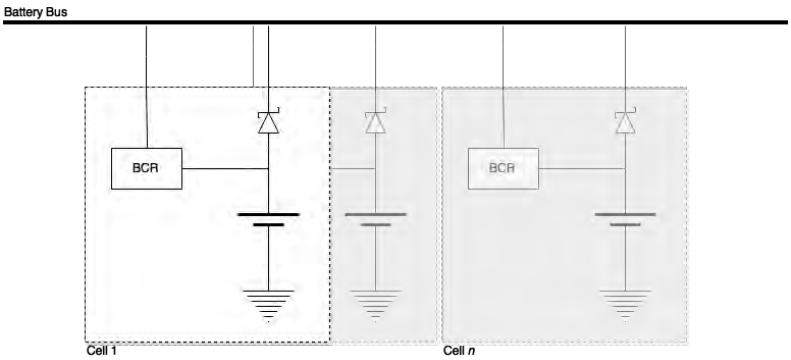


Figure 4.1: High level block diagram for a single-cell battery configuration with independent charging.

The second design decision relates to whether the cells should be placed directly in parallel, as opposed to each having the ability to be isolated from the bus. For isolation to be possible, a battery charge regulator would be needed for each cell, along with a diode for current to be fed to the bus. Such a method is depicted in Fig. 4.1. The most significant advantages include the potential for isolation of degraded or faulty cells, as well avoiding the possibility of overcharging and stressing any one cell. However, there are a few disadvantages:

- Inefficiencies are introduced through the BCR and diode paths;
- Points of failure are added at these two devices; and
- The additional control required to take advantage of this functionality, adds complexity.

The inefficiency that the BCR introduces is inherent, although minimal for a switch-mode device. Nevertheless, it would be swiftly offset through the ability to isolate a degraded or faulty cell. A regulator does, however, remain a point of failure in two senses: not only would its loss mean the cell can no longer be charged, thus rendering a functional cell useless, but a latchup event would result in a direct drain on the bus. With the exception of such a latchup event, the fact that multiple independent cell subcircuits exist ensures there is redundancy; the system can continue to operate unaffected, albeit with reduced capacity.

The diode necessary to allow discharge introduces further losses: while a Schottky diode would provide a reliable path with reasonable losses, an ideal diode would ostensibly negate losses but be prone to radiation effects through the use of semiconductor components.

The advantages of a configuration such as that shown in Fig. 4.1 are seen to balance the associated disadvantages: Where efficiency is lost through additional components, it is also gained through the isolation ability, should it become necessary. The increased risk of the loss of a cell is weighed against the new element of redundancy that prevents failed cells from negatively affecting the system. A remaining concern is a latchup event in the charge regulator; this will be addressed at a later stage.

A final advantage is the capability for a future supercapacitor-based energy storage module operating in parallel with the battery module. The topology lends itself to different energy storage elements, operating at different voltages and states of charge, each contributing safely to the bus, whilst having the ability to be either temporarily or permanently isolated. This would allow for an EPS-based technology demonstration, with the assurance that should the new technology fail to operate as expected, the system will default to standard functionality. For these reasons, such a configuration will be used.

4.2.3 Battery Bus

For the purposes of battery charging, the battery bus in this configuration will not require regulation — charge management is implemented at the individual cell level. However, the bus voltage will never drop below the highest cell voltage: with the assumption that cells will be prevented from discharging below 3.5 V, this will be the lower bus voltage limit.

The dropout voltage of the chosen regulator will need to be taken into account, but an upper bus limit of 4.8 V is a safe assumption.

State-of-Charge Monitoring

The extent to which each cell draws and contributes from the bus would be useful data, and indeed current monitoring is included on each battery string on the referenced COTS modules. However, the non-linear and plateau-like voltage vs. SOC curve, characteristic of lithium ion cells, makes it very difficult to estimate the SOC from the voltage alone, and tracking the net current flow in host software is an intensive, if not impractical, task. Although knowing the exact SOC might seem superfluous, it could provide vital statistics when comparing the performance of different cell chemistry variations, something that this particular battery configuration allows for.

Seeing that the power consumption of a dedicated gas gauge sensor, compared to that of a simple current shunt monitor, is comparable if not better[1], including such

[1]See eg. the BQ27411 and INA199Ax from Texas Instruments: The BQ27411 Fuel Gauge uses

a device would come at no cost to power, and would allow for state of charge monitoring and state of health estimation. It appears that all gas gauge sensors use an I^2C interface with one fixed address; thus, an I^2C multiplexer would be necessary to interface to multiple devices on the same bus.

4.3 Solar Input Design

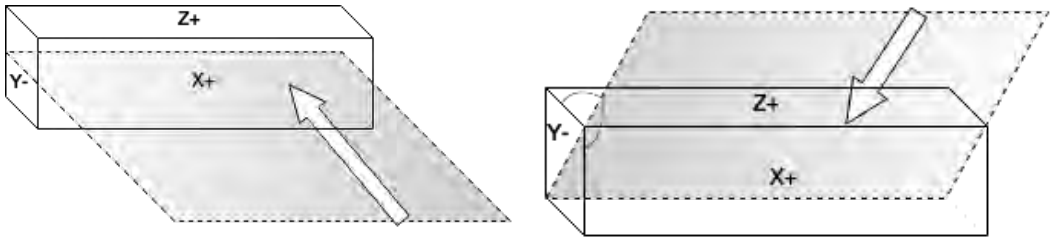
Being a CubeSat with six faces, there will be three sets of opposing panels, thus requiring three separate input channels. Opposing panels will never both be in sunlight at the same time (with the exception of some albedo light from the Earth's reflection), so with appropriate blocking diodes, one panel per set will always be dominant. It is also expected that configurations of triple-junction Galium Arsinide (GaAs) solar panel modules will be used: with typical modules outputting 5 V @ 500 mA under full illumination and at the maximum power point, a rating of at least 15 V @ 1 A will allow for up to two parallel or three series panels.

4.3.1 Expected Input Power

Assuming an input configuration in which opposing faces' panels are grouped to the same input stage, each input can be expected to see a maximum of 7.5 W for a 3U face. Important to note is that this is under optimal conditions, including beginning-of-life operation, maximum irradiance and low temperature, and thus is not representative of typical operation.

When calculating the maximum combined input power, the cosine law for solar irradiance takes effect. The form of (2.1) suggests that maximum effective irradiance will occur when the X+ and Z+ faces are both at 45^o to the sun line, as depicted in Fig. 4.2b. An alignment of the X+ (or Z+) face normal to the sunline, will mean that the other faces receive no direct irradiance. However, as the satellite rolls around the y-axis and the Z+ (or X+) face becomes illuminated, its power output increases, while that of the other decreases. When both faces are at 45^o,

a 10 mΩ shunt resistance, has an operating current of 93 µA, a sleep current of 21 µA and draws only 0.6 µA in shutdown mode. The INA199Ax current monitor has maximum and typical quiescent currents of 100 µA and 65 µA respectively.



(a) (b)

Figure 4.2: Diagrams depicting different cases of irradiance angles. (a) The X+ face is normal to the sun line, and (b) The X+ and Z+ faces are both at 45^o to the sunline.

total effective power output becomes:

$$\begin{aligned} E_{effective} &= E_e \cos\theta_{X+} + E_e \cos\theta_{Z+} \\ &= E_e \cos 45^o + E_e \cos 45^o \\ &= \sqrt{2} E_e \end{aligned} \tag{4.3}$$

Yaw around the z-axis can only reduce total available power, as the loss of power from the 3U face will be greater than the gain in power from the 1U face. Given the 7.5 W figure previously stated, total available solar power will thus never exceed $7.5\sqrt{2} = 10.6$ W.

4.3.2 DC-DC Converter

Solar array configurations consisting of a single panel (or more, but in parallel), at high temperature, may well have V_{mpp} below the maximum 4.8 V battery bus voltage. For this reason, a SEPIC regulator at the input stages will be necessary. Not only will a SEPIC regulator allow for maximum flexibility with regards to compatible panels and configurations, but it will also avoid the discontinuity, or possible instability, of a buck-boost topology operating at the crossover point. Furthermore, the topology has no reverse DC path, preventing discharge under dark conditions.

A disadvantage of a SEPIC regulator is their inherently-higher inefficiency over a buck regulator; for larger CubeSats with higher-voltage arrays, a buck regulator may be suitable. However, a 1U CubeSat, with very little external surface area, would almost certainly be limited to low voltage arrays.

4.3.3 Power Ratings

While each input stage is technically rated for 15 W, it was shown that the input power will never exceed 7.5 W. Furthermore, incidence angles limit the combined maximum power to 10.6 W on a 3U CubeSat with body-mounted panels. With a maximum input stage efficiency of 80% predicted, this figure is further reduced to 8.5 W by the time it is available on the bus.

4.3.4 Maximum Power Point Tracking

The environmental conditions in LEO, in particular both large temperature and irradiance fluctuations, means that a form of MPPT will be needed that is more sophisticated than a simple constant-voltage or constant-current technique. In addition, a spinning satellite could result in un-trackable conditions. While a regulator with integrated MPPT offers simplification, as well as an MPPT algorithm designed through many highly-experienced engineering hours, there are some disadvantages:

- The selection of regulators with integrated MPPT is limited, as opposed to those without;
- The inherently-higher transistor count on the regulator die, needed to implement the algorithm, *may* make it more susceptible to radiation-induced effects, including but not limited to bit flips that could result in indeterminable and undetectable behaviour; and
- The integrated MPPT algorithms will likely not be suited to potential fast-changing conditions that a spinning satellite may cause.

For the above reasons, the microcontroller should implement the power point tracking. In addition to radiation-induced bit flips being detected though an EDAC method, the EPS can intelligently switch between MPPT algorithms, depending on the current environmental and system conditions. For example: during periods of spinning, a CV or CC method can be used, while a true MPPT algorithm is used during nominal sunlit flight. During periods of critical power, the regulators can be left to a fixed operating point to allow the microcontroller to be put into a full shut-down state.

4.4 Microcontroller Selection

The need for telemetry and intelligent control of the EPS requires the use of a microcontroller. The following section details the requirements and selection of a suitable device.

4.4.1 Specifications

The following specifications take into account the system requirements above, as well as anticipated needs. Unless noted, the specifications are not considered crucial, as other methods to enable the functionality are available.

Communication Interfaces

Two I^2C interfaces — one configured as a master to communicate with external ICs, and one as a slave to communicate with the CubeSat bus — would be optimal. Although external I^2C interfaces are available, having them integrated may reduce power consumption through deep integration with the microcontroller's interrupt controller. If one or no I^2C peripherals are available, another interface, such as SPI, would be needed.

A CAN interface would also be beneficial; although external controllers also exist, CAN's complex message-based structure would be simplified though an integrated controller and the resulting direct access to registers.

UART interfaces are usually always available, and would be useful for debugging purposes.

Error Detection and Correction

Hardware-based EDAC is usually far more efficient than a software-based implementation, and undoubtedly less complex. Nevertheless, as long as EDAC is available on the flash memory, the option for software-based EDAC on RAM remains.

It is unlikely that the microcontroller will be able to correct flash errors due to architecture-based limitations.

The EDAC implementation will need to be looked at for the chosen device: If memory reads perform only detection, and not automatic correction, careful interrupt handling will need to ensure the error is corrected before execution continues. Furthermore, if detection (and correction) of errors only takes place during requested read and/or write accesses, periodic memory "flushes" will need to take place, to prevent the accumulation of errors.

Another consideration will need to be the case of uncorrectable errors occurring (such as two simultaneous bit errors in a word, detected in a SEC-DED implementation). In such a scenario, one strategy could be to change the reset vector (or have a bootloader) to point to an identical flash image in a different memory location. This, however, assumes sufficient flash memory is available; for this reason, a minimum of 64 KB is a requirement, although 128 KB would allow better margin for expansion.

Pin Functionality

In order to monitor the voltages and currents of the three solar inputs, along with the bus voltage, current before and after the battery sub-circuits, and the six outputs' currents, at least 15 Analogue-to-Digital Converter (ADC) channels will be necessary. An analogue multiplexer or an entire external ADC could ease this requirement.

Taking into account pins needed for communication interfaces, GPIO-pins for control lines, pins for device programming (ie. JTAG or similar) and power supply pins, a 100-pin package should be sufficient. If an external ADC is used, a 64-pin package may also be sufficient. Larger packages would unnecessarily take up valuable board space.

4.4.2 Selection

Table 4.2 lists the features of a few potential microcontrollers. Identification was made through a comprehensive online search, using the above fixed requirements as criteria, and excludes variations on those listed. With at least some form of EDAC a fixed requirement, choice is constrained.

The SPC560B50L3 from STMicroelectronics' (STM) SPC5 Automotive Range is a 32-bit microcontroller based on Freescale's e200z0h CPU. In fact, Freescale offers a comparable line of MCUs, based on the same core, with the MPC5604B a functionally-identical device. Distributor availability is the only reason it is not included here, although it offers no advantages. The CPU is based on the less-common Power Architecture, but because the fact that no assembly-level programming or complex mathematical operations are anticipated, this is considered irrelevant.

A multitude of power domains, along with SEC-DED on the flash, RAM and data flash interfaces makes it particularly suitable. Although it only has one I^2C interface, numerous other communications interfaces allow for an external I^2C controller bridge.

STM's STM32L051R8 microcontroller is from their ultra-low power range of ARM Cortex devices. Its low power consumption is a significant advantage, although limited volatile and non-volatile memory is a drawback. The lack of ECC on the RAM is a major disadvantage however; RAM is the most prone to SEUs and unless a software-based EDAC method is implemented, errors may go unnoticed.

Texas Instruments has a wide selection of Automotive-range microcontrollers, all designed for safety and reliability and thus implementing ECCs on all memory interfaces. The RM42L432PZ was found to best fit the requirements. A dual-CPU system, running in lockstep, along with a mirrored flash image in memory, ensures maximum immunity to SEUs, although such a powerful device is considered excessive. The lack of an I^2C interface is also a drawback.

Finally, Microchip offers the dsPIC33EV256GM106, the most suitable device from their dsPIC33EV range of high-performance 16-bit MCUs. This is their only line to include some form of EDAC controller. RAM is slightly limited and it does not include an EEPROM interface; furthermore, and similar to the STM32L051R8, it

Table 4.2: Specifications for a variety of suitable microcontrollers.

Model	**Architecture**	**Flash**	**RAM**	**EEPROM**	**Interfaces**[2]	**ADC**	**Power**[1]	**EDAC Solution**
SPC560B50L3	32 bit (Power)	512 KB	32 KB	64 KB [3]	1 x I^2C 3 x CAN 3 x SPI	28 channels (10bit)	60 mW (3V3)	Flash, RAM and Data Flash all have hardware SEC-DED
STM32L051R8	32 bit (ARM)	64 KB	8 KB	2 KB	2 x I^2C 2 x SPI	16 channels (12bit)	8 mW (3V3)	Single error detection and correction on Flash and EEPROM interfaces only.
RM42L432PZ	32 bit (ARM)	384 KB	32 KB	16 KB [3]	2 x CAN 2 x SPI	16 channels (12bit)	75 mW (1V2)[4]	Flash, RAM and Data Flash all have hardware SEC-DED; Dual-CPUs running in lockstep.
dsPIC33EV256GM106	16 bit	256 KB	16 KB	none	1 x I^2C 1 x CAN 2 x SPI	36 channels (12bit)	75 mW (5 V)	SEC-DED ECC integrated into Flash memory controller.

[1] Power consumption is calculated from available data and assumes:

- 16 MHz system clock
- Run/Operating mode with no peripherals enabled
- Core supply voltage as specified

[2] All devices have at least two UART or flexible serial communication interfaces.
[3] EEPROM is emulated in separate Flash.
[4] Power consumption is for the 1V2 core and excludes the 3V3 I/O supply.
Additional Notes:

- All packages are LQFP type or similar; the SPC560B50L3 and RM42L432PZ are 100-pin, and the STM32L051R8 and dsPIC33EV256GM106 are 64-pin.

only has EDAC on the flash memory. Its final drawback is that with 5 V operation and thus logic levels, all ICs will likely need to run off the same voltage which can result in slightly increased power consumption.

Given the above, the most suitable MCU is STM's SPC560B50L3; it offers the best features-versus-power consumption, has the necessary peripherals, and has EDAC on all memory interfaces. Although its power consumption is greater than would be liked, its low-power standby modes can be exploited to reduce overall consumption. An interrupt-driven software design would also contribute to lowering power consumption.

4.5 High-level Design

The high-level block diagram, shown in Fig. 4.3, takes into account the decisions made and the choice of microcontroller. Each SEPIC input stage will need a method for digitally varying the panels' operating points so that a software-based MPPT can be implemented.

The combined power entering the battery bus will need to be monitored for housekeeping purposes, as well as the power leaving the bus. This will allow for calculation of net battery power (the difference of the two), and can be implemented through current sensors before and after the branches to the battery subsystems, along with monitoring the bus voltage.

While the bus input current monitor can be a simple high-side current shunt monitor, the bus output current monitor needs to include a form of comparator in order to cycle system power — for a predetermined time — should an overcurrent condition occur. The microcontroller should also have the ability to trigger such a reset as a 'last-resort' tactic to clear unidentified faults.

The separation switch is as previously described and should allow an external trigger to latch it on. Even the removal of system power should not reset the latch; the only method of resetting should be a separate external signal that is only connected to the EPS during testing and flight preparation.

The fact that multiple I^2C devices with the same address will likely exist across each

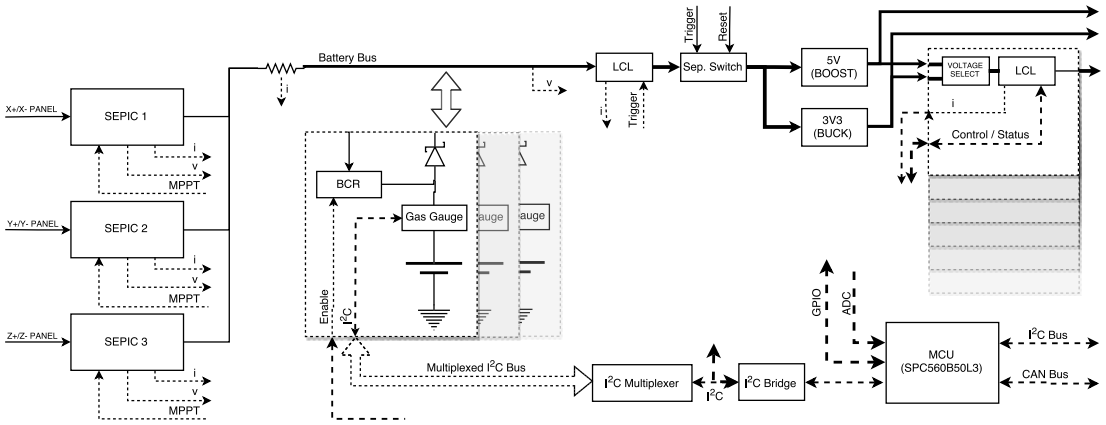


Figure 4.3: High-level block diagram for the full EPS.

battery subsystem means that each subsystem's I^2C bus will need to be multiplexed. Although adding to the bill of materials and power consumption, a multiplexer will allow for scaling of the number of such subsystems, without being limited by available MCU pins.

Because only one I^2C interface exists on the SPC560B50L3, an I^2C bridge will be necessary if the CubeSat has I^2C as its communications bus. If CAN is used, the I^2C bridge can be left unpopulated along with appropriate jumpers. If unused however, the CAN transceiver can be left unpopulated.

Chapter 5

Hardware Design

The following chapter brings together the specifications given previously, along with the background theory of Chapter 2, to develop schematic-level design of the various subsystems. Together, the subsystems should implement a system capable of adequate output capabilities with no software control needed. Although performance will be limited, this is considered an important design goal.

While previous chapters used the word 'subsystem' to refer to different satellite subsystems, this and future chapters will use subsystem to refer to subsystems within the EPS. External satellite subsystems will in turn be referred to as 'payloads'. Each subsystem will be looked at separately with its design, as well as its modes of failure, discussed.

In terms of component choices, all components will need to be rated for at least the industrial range (-40– +85^{o}C), with the extended range preferred. Where reasonable, negligible price differences between 'standard value' components and components that give maximum performance/resolution will not be taken into account. This is justified through this module being a specialised device, and thus not destined for mass production.

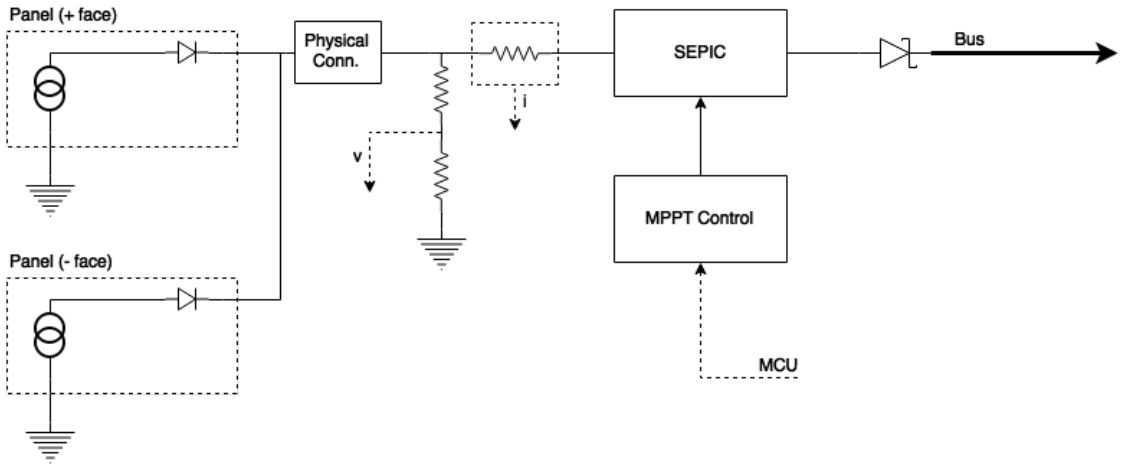


Figure 5.1: Block diagram for the input stage.

5.1 Input Stages

Each SEPIC input stage needs to regulate solar input power in a way that can track a settable panel operating point and provide an output to a common bus. This OR-ing (in a power sense) of the input stages suggests a constant current output with diodes used to allow unidirectional flow onto the bus.

The (as yet undefined) MPPT algorithm will need to know the panels' current and voltage outputs, and thus these readings will need to be taken from a point before each converter. With the microcontroller controlling the power point tracking, the setpoint will need to be digitally adjustable.

5.1.1 Subsystem Functionality

The block diagram in Fig. 5.1 shows the various components needed to implement the input stage. Note that the output diode will be inherent to the SEPIC topology, and that depending on the exact device chosen, the external MPPT control block may not be needed.

As specified, each input can expect to be connected to two sets of parallel arrays with only one ever in sunlight. External blocking diodes will be necessary to prevent power from the sunlit panel being radiated out as heat by the dark panel, and a reliable physical connector will need to be used to interface each panel to the PCB.

With input voltages specified to be up to 15 V, a voltage divider will be needed to allow interfacing to the microcontroller's 3.3 V ADC. A simple high-side current shunt monitor will allow measuring of input current. Some COTS modules have separate current monitoring for each opposing pair, allowing the system to explicitly tell which of the two connected panels is currently dominant. This is considered unnecessary as such knowledge will not and should not be necessary for the MPPT algorithm. It would also require additional hardware that increases both power consumption and physical area, while also adding potential failure points. If, for failure analysis, such information is needed, the ADCS should be able to provide attitude data from which the sunline, and thus the dominant panels, can be established by ground crew.

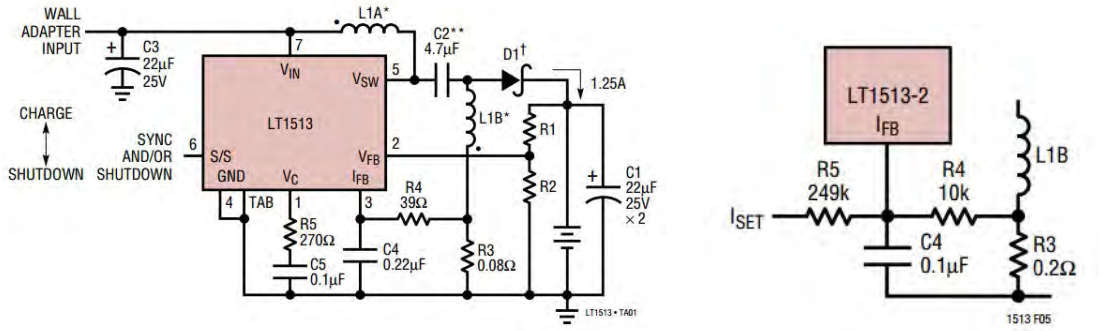
The SEPIC converter will need to have both CC and CV operating modes. The CC mode will allow OR-ing of power from the three input stages, while the CV mode will limit the bus voltage when demand is low. This will in turn adjust the operating point of the panels, leaving excess power on the panels as heat.

Depending on the capabilities and built-in functionality of the chosen converter, additional hardware to implement control of its setpoint may be necessary. In either case, a digital interface to perform this control is needed.

5.1.2 Components

The INA199 range of high or low-side current shunt monitors, from Texas Instruments, was chosen to implement current sensing. They offer a -0.3–26 V common-mode range with an offset voltage that allows full-scale shunt drops of just 10 mV. With a 1 A maximum input current specified, this allows a 10 mΩ shunt resistance that will minimise losses. 10 mΩ is also considered the smallest practical shunt. The current sense resistor will need to be carefully specified for the power requirements and temperature environment — 5 ppm/^{o}C should be targeted in order to maintain full-range accuracy.

Choice of appropriate SEPIC converters is limited and the most suitable device was chosen to be the LT1513-2 from Linear Technology. The device is designed as a BCR for lithium-based batteries, providing an automatic CC/CV output. Fig. 5.2a shows a typical configuration that gives this functionality: the CV output



(a) (b)

Figure 5.2: Datasheet-suggested schematic design for the LT1513. (a) Typical design for a CC/CV Li-Ion battery charger, and (b) modifications for programmable charge current.

is regulated though a resistor-divider feedback network on the output, while the R3/R4 network limits inductor current and by extension output current. Note that this is using the LT1513; the LT1513-2 has internal modifications that regulate the I_{FB} pin at 0 mV to allow a programmable charge current, as depicted in Fig. 5.2b. Under anticipated conditions an 80% efficiency can be achieved.

The device, although in a bulky 7-pin TO-263 package, requires few external components: it has an integrated MOSFET and the CC/CV control is further integrated. A simple DAC could provide the I_{SET} voltage shown in Fig. 5.2b. The datasheet notes that instability can occur when the battery is replaced with a resistive load, as will be our case, or if large resistances are used at the current set input. It will thus be important to accurately calculate the values for the compensation network components (R5 & C5) and not simply use the suggested values.

To provide the current-setting voltage, the DAC081C085 DAC from Texas Instruments was chosen. It has very low power consumption (156 µA max @ 3.3 V) and a simple I^2C interface. An 8-bit resolution should provide reasonable control with a rail-to-rail output over its 2.7–5.5 V supply range.

Two tri-state address inputs allow up to nine devices on the same I^2C bus, with a bus-wide broadcast address also available. The DAC081C085 requires a 2-byte data word that sets the output voltage as well as an output impedance-settable power-down mode. A read request returns the contents of this register which can be used to verify the DAC has been correctly set.

Two separate connectors are needed per input that need to be reliable and capable of carrying up to 1 A of current. The Molex Picoblade series of connectors was chosen for this: it is used on the majority of COTS modules, thus providing compatibility as well as assurance that they are reliable within the vibration environment. The connector features a thin profile with blade-like pins, as well as a slight mechanical latch. A four-pin connector will be used per input, doubling up the ground and positive connections for the purposes of reliability and current handling.

5.1.3 Schematic Design

Unless otherwise noted, for this and all other subsystem schematics, V_{CC} refers to the EPS-specific 3.3 V supply that is shared amongst all EPS subsystems. Port elements are used to indicate inputs and outputs to/from other subsystems, and net names are used to show electrical connections between nets within the same subsystem. Net names are formatted in **boldface**.

Input Current and Voltage Sensing

Fig. 5.3 shows the schematic of the input connectors and the current and voltage sensing. The LT1513-2 can operate with inputs from 2.7–25 V. To allow some margin on both this lower limit and the upper limit (15 V) previously specified, a final specification will be 3–18 V. Maximum input current was specified to be 1 A.

Given this, along with a 10 mΩ shunt resistance, the maximum drop over the shunt will be 10 mV. With a 3.3 V supply voltage, maximum sensor gain is 330; to provide some margin the INA199A3, with a gain of 200, is used. The datasheet-suggested R13/R14/C8 filter network will allow some smoothing from the regulator's switching. The current sense resistor should have at least a 100 mW power rating.

The resistor-divider of R17 and R19 is used to accommodate the microcontroller's 3.3 V ADC.

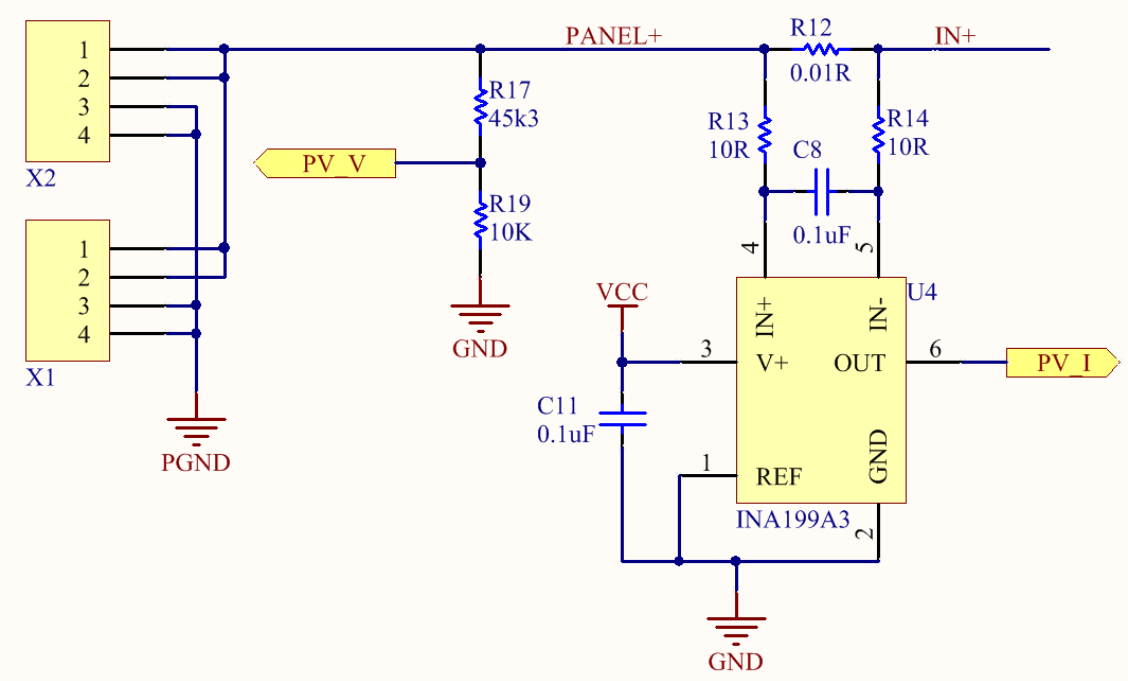


Figure 5.3: Schematic of the input connectors and current and voltage sensing.

LT1513-2 Regulator

The schematic of the LT1513-2 regulator is shown in Fig. 5.4. Input capacitor C6 is ceramic, but the output capacitors are tantalum — to provide a good safety margin over the 4.8 V maximum bus voltage, they should be rated for at least 25 V.

It was specified that the maximum input power per stage is limited to 7.5 W and is only available with highly-optimal conditions. The 80% efficiency means that only 6 W will be available at the output. Taking the minimum bus voltage of 3.5 V, maximum output current is thus 1.7 A.

Although there is an option to use two separate inductors, the SEPIC topology allows for a coupled inductor that reduces the required land area. The choice of coupled inductors is, however, more limited than standard inductors. The DRQ125-100-R is a coupled inductor rated for $I_{rms} = 2.67$ A, although is fairly large at 13 mm x 13 mm. Seeing that available physical area is at this point unknown, the lower-rated DRQ74-100-R is chosen; this would initially suit 2U CubeSats and, at only 7.6 mm x 7.6 mm, will require appreciably less area. It is rated for $I_{rms} = 1.2$ A and $I_{sat} = 1.6$ A and thus is only intended for the initial revision.

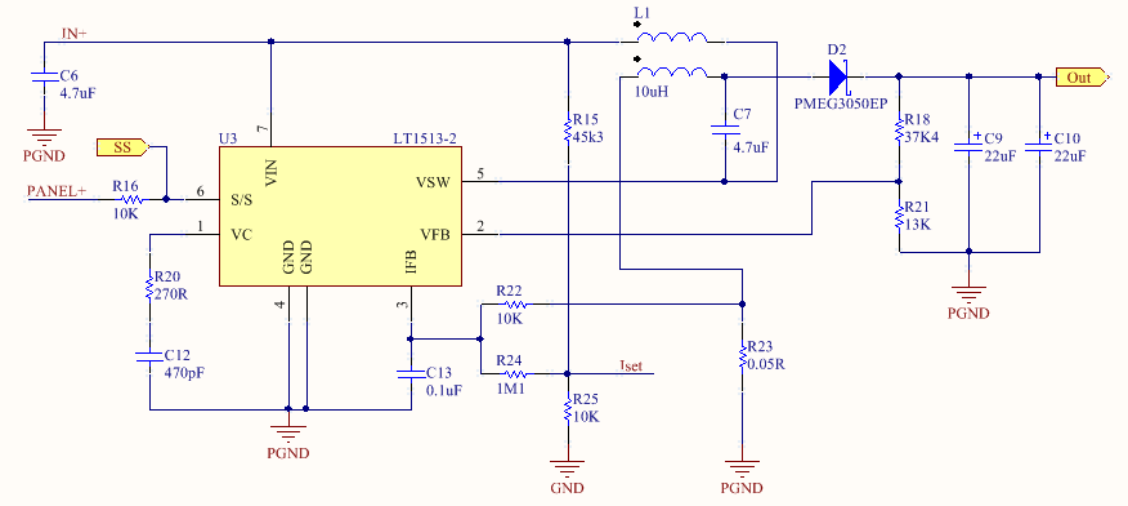


Figure 5.4: Schematic of the input stage LT1513-2 regulator.

The S/S pin allows regulator synchronisation and/or shutdown. Only the shutdown functionality is required (although it will likely remain enabled) and can be controlled by a microcontroller pin. The only reason the pin is pulled up to the point before the current sense resistor (**PANEL+**) is for layout simplification that becomes apparent during PCB design.

Diode D2 was chosen to be Schottky type with as small a forward voltage as possible (360 mV) and has a good reverse current characteristic under intended operation.

R18 and R21 form the regulator's CV feedback and set the output limit to 4.84 V. The CC feedback network consisting of R15, R25, R22, R24 and R23 is however more intricate: Firstly, the sense resistor R23, although suggested to be 80 mΩ, is reduced to 50 mΩ to improve efficiency. Then, R15 and R25 serve to set a default operating point should the DAC not be operational. They form a voltage divider that is specifically taken from the unregulated input to ensure that, should the satellite be coming out of eclipse with failed batteries, the regulator can start up. The rest of the network provides the desired range of current control.

The full output current (I_L) will flow up through R23 and thus a voltage drop $V_{R23} = R_{23}I_L$ will develop. Pin I_{FB} is regulated to 0 mV[1], and thus the divider R22/R24 can be used to programme the output current. **Iset** is the output of the DAC but, as will be seen, this passes through a Schottky diode to prevent DAC failure tying this point to 0 V. With a 3.3 V supply, the DAC output range is thus effectively reduced to 0–2.93 V. Disregarding the R15/R25 divider and balancing the currents through R22 and R24 (assuming negligible input current into I_{FB}), we get:

$$\frac{V_{I_{set}} - 0}{R_{24}} = \frac{0 - R_{23}I_L}{R_{22}} \tag{5.1}$$

R22 is arbitrarily set to 10 kΩ, which leaves R24 to set the maximum output current when the DAC outputs its maximum output voltage. This resistor could thus be left to configuration-specific customisation to maximise control resolution, and can be calculated from:

$$R_{23} = \frac{(10\ K)(2.93)}{(50\,\mathrm{m\Omega})(I_L)} \tag{5.2}$$

With single-module arrays anticipated during testing, the maximum output current will not exceed 500 mA and thus R24 is initially specified as 1.1 MΩ.

The datasheet provides the equation for calculating the compensation network of R20 and C12. While the filter resistor R20 is suggested to remain at 270 Ω, the value of C12 has no inherent limitation, and was calculated to be 470 pF — this takes into account the previously-calculated feedback resistances and, seeing that the network provides stability in the CC mode, an output voltage of 4.5 V.

Digital-Analogue Converter

The DAC and accompanying circuitry is shown in the schematic of Fig. 5.5. C14 and C15 are manufacturer-specified decoupling capacitors, and R26 and R28 allow for differentiating the devices' I^2C addresses. ADR0 and ADR1 are tri-state inputs,

[1]This pin is also specified to have an offset voltage of $-7.5\,\mathrm{mV} < I_{FBVOS} < 12.5\,\mathrm{mV}$ — this will cause some (quantifiable) error in the current setpoint.

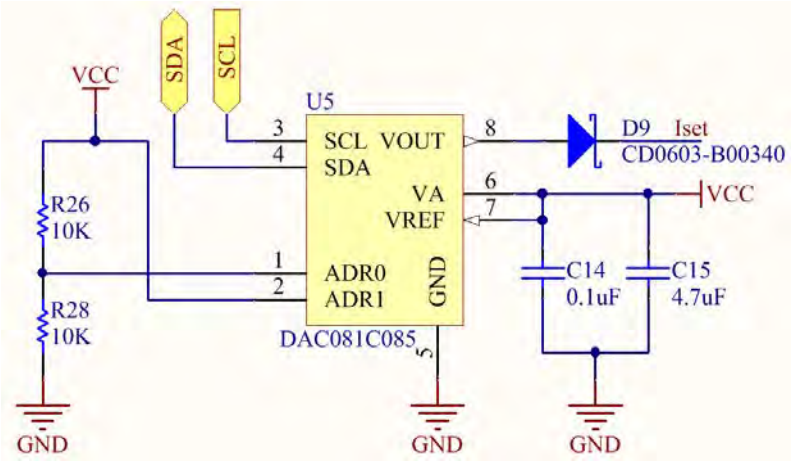


Figure 5.5: Schematic of the input stage DAC.

and thus one stage will have R26 unpopulated, the second R28 unpopulated and the third both unpopulated.

In order to prevent the DAC becoming a point of failure for the input, a diode is used to prevent the DAC output tying **Iset** to 0 V. An alternative to this would be replacing the diode with a resistor, however this would mean **Iset** would be dependent not only on the DAC's output voltage, but also variations in the input voltage as a result of the R15/R25 divider[2].

The disadvantage of the diode is the inherent voltage drop and resulting reduction in output voltage range. This is however easily quantified and control can be designed around it. Important to note is that for DAC output voltages below the voltage created by divider R15/R25, the DAC will no longer control the current setpoint and will instead be set by that voltage created by the divider. It thus follows that R15/R25 should be specified to set a desired minimum current setpoint:

At the end of the orbit's sunlit period when the panels are at their highest temperature and minimum power output, an assumption of 1.8 W output power will be made (see Table 2.1). Then, assuming a worst case incidence angle of $\theta = 60^o$, the panel output power will further be reduced by half (from (2.1)). Calculating this for the true worst case would mean that should this default configuration be in effect (the DAC has failed), the system will be limited to this minimum when, during the

[2]It can be shown that setting a desired panel operating point becomes dependant on the input voltage, the DAC output voltage, as well as the bus voltage. Using a diode, a constant operating point can be set simply through a DAC output voltage that is slightly adjusted for the bus voltage.

majority of the time, it could be drawing much more. This design element could potentially be optimised after testing and/or in-flight data.

Under these conditions — assuming a panel voltage of 4 V and 0.9 W of output power — a current of 225 mA can be expected . From conservation of power and (5.2), we get:

$$\begin{aligned} \eta V_{in} I_{in} &= V_{bus} I_L \\ &= V_{bus} \left[\frac{R_{22} V_{I_{set}}}{R_{23} R_{24}} \right] \\ &= V_{bus} \left[\frac{R_{22} (\lambda V_{in})}{R_{23} R_{24}} \right] \end{aligned} \tag{5.3}$$

where $V_{I_{set}} = \lambda V_{in}$ is created by the R15/R25 divider and η is the converter efficiency. It is immediately clear that the functionality we want is independent of V_{in}, thus allowing us establish a minimum default panel operating point from only an assumption of V_{bus}. Seeing that the minimum assumed panel current occurs at the end of the sunlit period, the batteries will likely be fully charged. This means that the bus should be at its maximum of 4.8 V.

(5.3) can be rearranged and, given this reasoning and the previously-calculated component values, simplified to give:

$$\begin{aligned} \lambda &= \frac{\eta I_{in} R_{23} R_{24}}{V_{bus} R_{22}} \\ &= \frac{(0.8)(0.225)(55)}{(4.8)(10)} \\ &\approx 0.21 \end{aligned} \tag{5.4}$$

The R15/R25 divider is thus set to create this fraction of the input voltage. The above calculations have shown that this design should maintain this default operating point, irrespective of the number of series modules in the solar array.

5.1.4 Failure Analysis

The fact that three separate input stages exist that are not directly coupled (the diode ensures power can only be transferred onto the bus, assuming diode breakdown has not occurred) means that there is inherent redundancy — if one input stage fails, the rest of the system can continue to operate unaffected. However, analysing the failure modes of this stage along with discussing their implications and the preventative measures taken will be useful to future development.

For each input stage, the regulator itself is a point of failure: if switching stops, the loss of coupling between the input and output means that the connected panels can no longer contribute to the system. However, this can have no further system effects seeing that it is powered directly off its input. If the microcontroller fails, the S/S input should remain pulled high and thus the regulator enabled, unless a direct short circuit within the MCU or a software anomaly pulls the relevant pin low.

A failure of the current sensor should not cause any direct effect on the system, unless an internal latch-up event draws excessive current through the V_{cc} pin. Nevertheless, because the sensor is powered off the EPS power supply, power can be cycled and thus the latch-up likely released.

A latch-up event in the DAC can be resolved for the same reason. And, as mentioned, an internal direct short circuit of its output is protected against through the external diode.

It thus follows that this subsystem has no highly-probable single points of failure. Redundancy should ensure backup power is always available, although the loss of one or more input stages may mean power scheduling of external payloads, should it be severe.

5.2 The Bus

The bus is a critical subsystem, central to the entire system and the main and only power path. It serves as the interface between the solar inputs, the batteries and the main regulators that provide power to the external subsystems. With the entire satellite thus dependant on it functioning correctly, it is likely to contain single points of failure and will be looked at in close detail.

The 'kill switch', although technically part of the bus, will be looked at in its own section due to the specific functionality it needs to implement.

5.2.1 Subsystem Functionality

Fig. 5.6 shows the block diagram for this subsystem. For naming purposes, the bus before the input current monitor will be referred to as the *raw bus*, the section between this and the output current monitor the *battery bus* and the section after this the *main bus*.

Two current sensors are needed to be able to calculate power flow through the three branches seen in Fig. 5.6 — the net power in the third will be the difference of the two. The bus voltage reading can be determined from a simple resistor-divider whose output feeds into an ADC input.

The overcurrent protector for this main bus is specified to limit current to a hardware-

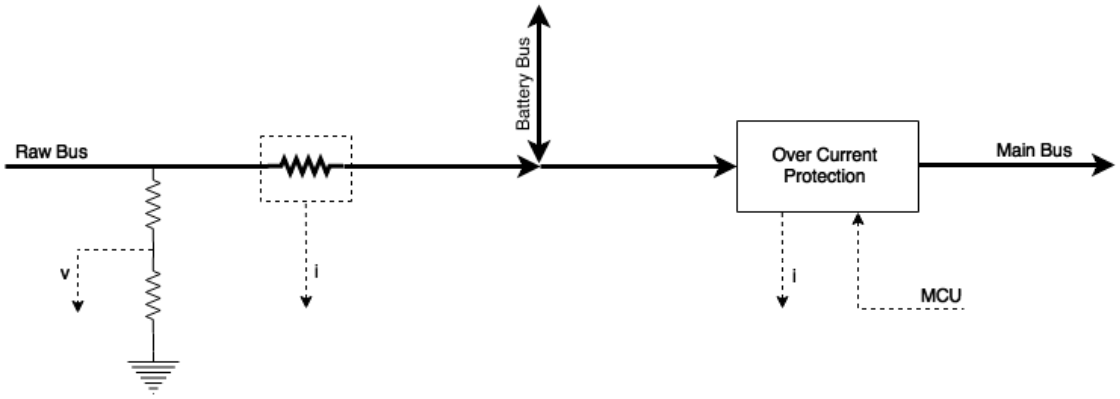


Figure 5.6: Block diagram for bus monitoring and overcurrent protection subsystem.

defined value and cycle the bus, for a pre-determined time, should an overcurrent condition occur. The reason for this being implemented purely in hardware is that the entire satellite, including the EPS, will be turned off as a result of said cycling. It was specified that the microcontroller should be able to trigger such a cycle should an unidentified or uncorrectable fault occur.

5.2.2 Components

For the same reasons that were given, the INA199 range of current monitors was chosen for the input sensor. The output sensor requires additional functionality however, in the form of a comparator that can trigger the cycle when a threshold is met. Texas Instruments' INA20x range of current shunt monitors, with integrated comparators, provides the needed functionality; a similar range, the MAX437x, is made by Maxim Integrated. Both devices have similar and sufficient common mode and accuracy parameters and gain ranges, and use an external resistor-divider to set the current limit. Both devices also provide a latched open-drain output that is controlled by the comparator. A reset input releases the latch and returns the open-drain output to its default state.

The choice between the two is made simple through their quiescent currents — the INA20x draws a typical 1.3 mA, while the MAX437x draws just 50 µA.

A p-channel MOSFET is the obvious choice for the switching element, and the AON7407 from Alpha & Omega Semiconductor was selected. It has a small physical size, is rated for a 40 A drain current, with V_{DS} = -20 V, and $R_{DS\ (on)} < 10$ mΩ at an expected V_{GS} = -4.5 V .

5.2.3 Schematic Design

Fig. 5.7 shows the schematic that implements the required functionality.

The voltage range for the bus varies from 3.5–4.8 V during nominal operation. However, when the EPS is being charged externally during testing and flight preparation, this may rise up to 5 V. The R6/R8 divider is chosen accordingly to give maximum ADC resolution.

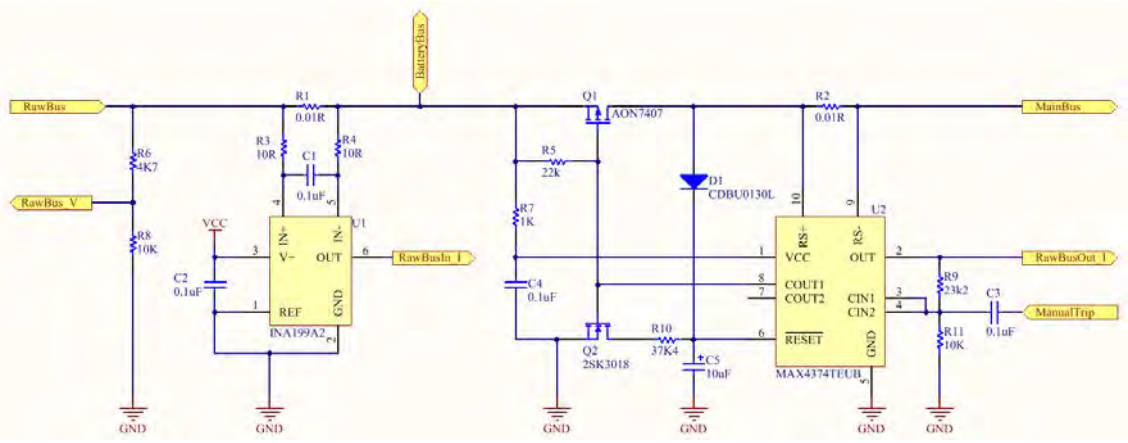


Figure 5.7: Schematic of the bus current monitoring and overcurrent protection subsystem.

Total combined input power was shown to be 8.2 W. At the minimum bus voltage of 3.5 V, this equates to 2.34 A. Sense resistor R1 should thus be rated for at least 200 mW.

Between the two current sensors is the battery bus, and is the point where cell subcircuits will connect to. During charging, power will be drawn from here and, during discharge, power will be contributed. Each of the 5 V and 3.3 V regulated buses are to be rated for 5 A (peak); although the bus at this point should technically be rated for 10 A[3], this is impractical for a few reasons: Firstly, PCB trace widths become unreasonably large. Secondly, with the amount of available power, the system cannot sustain such large continuous power draws. It is expected that 5 A will be the maximum current drawn for any appreciable length of time (ie. neglecting inrush current spikes).

In terms of accurately sensing the current at this point, the sensor gain will be set for 6 A: with a 10 mΩ sense resistor, maximum gain is 55 and the MAX4375FEUB with a gain of 50 is chosen. Any current greater than this will be a spike or a defective payload: in the latter case, the payload should be power cycled. The current sense resistor should have a 1 W rating.

CIN1 and CIN2 are the inputs for the two internal comparators: the first has a latching open-drain output that is active during normal operation, and the second is non-latching with an active output when triggered. Both comparators have the

[3]Approximate, due to voltage differences between the bus and regulated buses.

same internal 600 mV bandgap reference voltage.

R9 and R11 are initially set to trigger on a current of 10 A. This will avoid false triggering on inrush current spikes, but can likely be reduced once the system is characterised during testing. A future revision could also create an RC time constant at the input to alleviate this potential problem. A microcontroller GPIO pin is coupled to the comparator inputs through C3: a transition from a low to high output will cause a spike at the inputs which will trigger the reset cycle.

The microcontroller's datasheet specifies a minimum pin transition time of 100 ns for a highly-capacitive load with a 'slow' slew rate configuration. Given a capacitor's current-voltage relation,

$$I(t) = C\frac{dV(t)}{dt}, \tag{5.5}$$

a maximum pin current of around 4 mA is expected. This is well below the pin's maximum and should thus be safe. Testing will have to ensure that the pulse width generated (the sum of the transition time and the resulting RC constant that is created, when the pin is held high and the capacitor discharges through R11) is sufficient to trigger the comparator.

During nominal operation, the gate of Q1 is pulled to ground by COUT1 and biased on while Q2 is biased off. The RESET input is subsequently pulled high with capacitor C5 simultaneously charged. An overcurrent condition is triggered when the CIN1 input exceeds 600 mV. At this point, the COUT1 open-drain output is latched open and remains in that state until RESET is brought below 800 mV. As Q1 turns off, D1 is no longer forward biased and capacitor C5 starts discharging through R10 and Q2.

R10 and C5 are thus chosen to provide the 500 ms bus cycle time. D1 was chosen to have good forward voltage and reverse current characteristics — at anticipated temperature conditions, these are around 200 mV and 1 µA respectively.

Rearranging (5.5) and integrating over t gives us

$$t = -RC\ln\left(\frac{V(t)}{V_0}\right). \tag{5.6}$$

The voltage drop across D1 means that at a minimum and when charged, the voltage across C5 will be 3.3 V. For the voltage to drop to 800 mV over 500 ms, (5.6) can be used to give a resistance of approximately 35 kΩ when a 10 µF capacitor is used. To account for the diode's reverse current and to provide a margin, this is rounded up.

With such a low quiescent current, a series resistor in the V_{cc} line can be used as latch-up protection. When drawing its maximum rated 100 µA, a 1 kΩ resistor drops just 100 mV, while dropping the full supply as soon as just a few milliamps are drawn. During normal operation, just 10 µW is dissipated by this resistor.

5.2.4 Failure Analysis

The only single point of failure in this subsystem is the MOSFET: it has two different modes of failure, each with several causes:

Internal failure of the device is the first, and the inability for it to conduct would mean the loss of the system. Such a failure is highly unlikely, but could arise from radiation-induced gate rupture that would see a (partial) short circuit forming between the gate and drain. Although partial failure (SEGD) would rather result in increased gate leakage current and likely wouldn't cause the device to stop functioning, a full short circuit would in all likelihood mean it can no longer be biased on.

Nevertheless, the risk of SEGR is known to be largely alleviated through appropriate derating and low voltage operation. The AON7407 has a drain-source breakdown voltage of -20 V and rated current of 40 A. It will only ever block the 4.8 V bus voltage, and nominal current draw should never exceed a few amps. Turn-on and turn-off times are tested at $V_{gs} = -4.5\,\mathrm{V}$ — 4.5 V is indeed the nominal bus voltage, and will never exceed 4.8 V[4].

A more realistic failure mode however is if an *external failure* results in the gate no longer being pulled to ground. This could arise as a result of the failure of the MAX4374, and has a few possible causes:

[4]Section 2.6.2 explained that aiming for a V_{gs} that matches that of manufacturer-tested turn-on/off times is a good SEGR risk-mitigation strategy.

Firstly, if the device experiences latch-up, operation would be unpredictable and, if excessive current flows, the device would likely be destroyed. However, the addition of the series resistor in the V_{cc} line prevents this, and should ensure clearing of the latch-up event. It is possible that a state of equilibrium will be reached as the supply voltage lowers. But, the fact that current is limited to just 3.3 mA means that this should be below the parasitic thyristor's holding current. If it becomes possible to perform radiation testing and the latch-up condition proves to not reliably clear, the value of the series resistor could be raised at the expense of a further (but still slight and indeed acceptable) decrease in supply voltage and a slight increase in power consumption.

Secondly, if the device does not reset after being triggered, COUT1 will not resume its active state. This could only occur if RESET is not pulled low after said trigger. There is however no scenario in which this could happen: even if Q2 fails, C5 will still have a discharge path through D1 as well as the RESET pin.

With such low-power operation, Q2 is not realistically prone to radiation-induced SEEs. A threshold voltage shift would mean it may be biased on at lower gate voltages; even if Q2 remains permanently on, subsystem operation is unaffected. In fact, testing may show Q2 to be unnecessary — the power loss through R10 would be small.

The capacitive coupling to the microcontroller means that a static software and/or hardware anomaly cannot influence the subsystem's operation; it is practically impossible for the pin to get into an unintended fast switching state. Even so, if an anomaly does occur, the resulting power cycle will see the microcontroller perform a hard reset, and should hence resume normal operation.

This subsystem is thus reliable and high-unlikely to have failure modes that affect system operation in any severe manner.

5.3 Kill Switch

The kill switch subsystem is required to ensure the satellite remains powered off during launch. It thus needs the critical functionality of remaining off until a trigger signal is received from the separation switch, after which reliably turning and remaining on indefinitely. There should, however, be a method for resetting the switch, to enable ground testing, as well as an input for a Remove Before Flight (RBF) pin; this ensures the switch cannot be falsely triggered during transportation and loading.

A straightforward design decision is to keep the actual implementation of the kill switch separate to the mechanical separation switch for previously-given reasons. This subsystem however, like the previous, is a single string element and its failure would break the power path.

5.3.1 Subsystem Functionality

Fig. 5.8 shows the block diagram for this subsystem. A physical connector is needed to interface to the separation switch, as well as to the RBF pin.

The separation switch will close upon deployment, and having it pull to ground means that no other signals are routed away from the system. As specified, there should be no reliance on the separation switch remaining closed due to possible

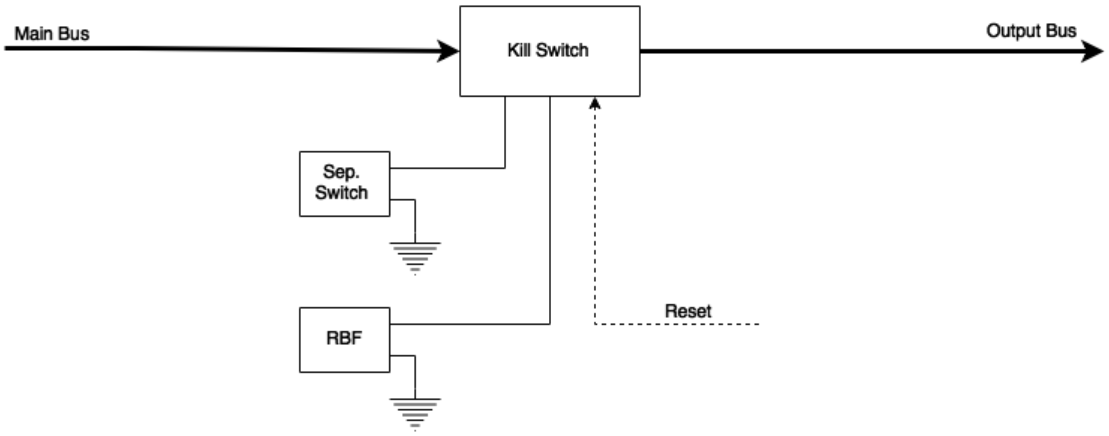


Figure 5.8: Block diagram for the kill switch subsystem.

environmentally-induced effects. A difficulty thus presents itself when considering that, in the case of failed cells, all power could be removed from the system during eclipse periods.

In terms of implementing the required latching functionality, there are a few options:

- A thyristor would allow a small current to trigger it, and would remain on, so long that system current remains above the holding current. It would, however, need a method to keep it triggered if power is lost, or there is an interruption to system current.
- A flip-flop-based approach would allow similar functionality, but would also need a method to remain latched if system power is lost.
- A MOSFET using a feedback system to keep it triggered would also provide the needed functionality, but keeping it triggered during system power loss remains a problem.

A thyristor has an inherent voltage drop that would result in relatively high inefficiencies in this particular low-voltage application; for this reason, it is not considered a viable option. The second and third options are similar, although the third avoids the use of a CMOS flip-flop (although it could be implemented in discrete components), and is thus thought to be the best choice for this design element.

5.3.2 Schematic Design

Fig. 5.9 shows the schematic design that implements the required functionality. The same p-channel MOSFET, as used previously, was selected for similar reasons.

After power-up, Q4 is biased off and will remain in that state until its gate is pulled low. Q8 is normally on, and thus closing the separation switch will cause Q4 to turn on. However, the RBF pin input has the ability to turn Q8 off, thereby breaking the separation switch path[5]. The Trigger input allows this functionality to be bypassed, to enable final testing when the RBF pin is inserted and/or the separation switches are inaccessible.

[5]If it is found that the mechanical switch connects to an external ground (and/or cannot use the intended return path), the position of Q8 can be moved with some added circuitry required.

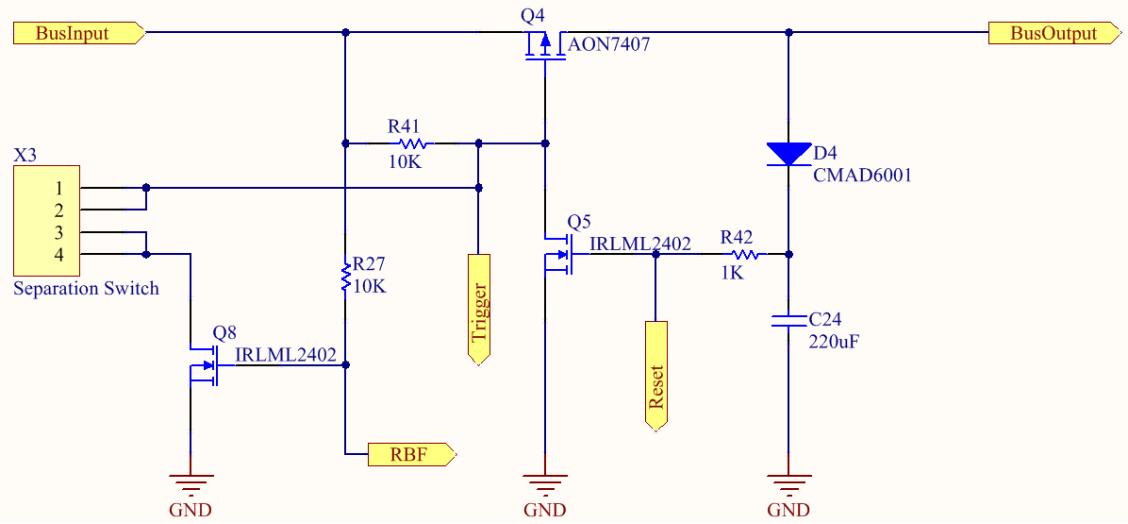


Figure 5.9: Schematic of the kill switch subsystem.

Once the separation switch is triggered, Q5 is turned on through the feedback path and thus keeps the switch latched, regardless of the state of the separation switch. If all power is lost, diode D4 allows Q5 to remain biased on while C24 still has sufficient charge. This is a finite period of time, and is limited by the discharge paths through D4 (reverse current) and Q5 (gate leakage current (I_{gss})). This length of time must be greater than the longest eclipse period: Fig. 2.3 showed a maximum eclipse lasting around 40% of the orbital period; for an average 90 min orbit, this time constant should thus be at least 36 min.

D4 was selected to have as low a reverse current as possible — at 0.5 nA typical, this is negligible. It does however have a forward voltage of 1.1 V. Finding a MOSFET with a comparable gate leakage current is far more difficult and the IRLM2402 is rated for 100 nA maximum at $V_{gs} = 12$ V. Choice of capacitor is further limited to those of ceramic type in order to keep leakage currents negligible, which in turn limits capacitance to the 100–330 µF range for a suitable voltage rating.

The chosen capacitor[6] is a 6.3 V, 220 µF multilayer ceramic capacitor that has a leakage current of $\ll 1$ nA. At a minimum DC bias voltage (corresponding to a minimum bus voltage) and taking into account its X5R rating and ±20% tolerance, a minimum capacitance of 110 µF can be expected. A maximum bus voltage and thus maximum DC bias further reduces capacitance to 82 µF.

[6]Part number JMK325ABJ227MM-T.

Taking into account the diode voltage drop and gate threshold voltage, C24 can drop 1.7 V and 3 V at minimum and maximum bus voltages respectively. Given the two corresponding capacitances and a desired 40 min minimum time constant, maximum total leakage current is limited to 78 nA, which is below the 100 nA maximum gate leakage current of Q5. However, data given in [67] suggests an exponential relationship between I_{gss} and V_{gs} which would achieve the $I_{gss} < 78$ nA requirement. This design element requires further verification but capacitance can nevertheless be increased at the cost of physical area.

Although such verification should ensure the minimum time constant holds under worst case conditions, it should be noted that the assumptions made are conservative for the following reasons:

- By the time all cells might have failed, the TID-induced threshold voltage shift of Q5 should see a lower threshold voltage;
- If cells have failed and are not charging, the bus voltage should be at its maximum, or at least higher than the worst case 3.5 V; and
- As the capacitor discharges, the DC bias has a corresponding decrease; the voltage over the capacitor thus has a non-linear decrease, even if leakage current remains constant over V_{gs}.

These reasons would result in an extended latching period.

The Reset function will release the latch provided that it is not simultaneously triggered, and should be available through a connector that is completely removed before launch to ensure the subsystem cannot be falsely reset during flight.

5.3.3 Failure Analysis

Similarly to the previous subsystem, the MOSFET in the power path is the only direct point of failure, with an external failure once again the only realistic cause. However, there is an element of redundancy in that if the feedback system fails, the mechanical switch could be relied upon to keep Q4 turned on. Furthermore, if the latching period is not long enough to see the system through an eclipse period

with no system power, another brief trigger signal from the separation switch will re-latch the switch. Threshold voltage shift of Q5 and/or Q8 can only improve the specific functionality they provide.

If follows that the only scenarios in which this subsystem can fail are:

- The mechanical switch fails entirely, all cells fail, and the latching period is not long enough to keep the switch latched through an eclipse period;
- Q4 fails in a catastrophic manner, such that it can no longer be turned on.

Q4 thus remains the only single point of failure but, as argued previously, careful MOSFET choice has ensured this to be a very remote possibility.

5.4 Regulators

Two switch-mode regulators are used to provide the main 5 V and 3.3 V buses. Although no special functionality is required, a brief discussion of component choice and failure modes will be looked at in this section.

Fig. 5.10 shows the block diagram for this subsystem. The absence of redundant regulators was a design decision based predominantly on a concern for available physical area, but also the fact that high reliability parts are available. An enable line for the 3.3 V regulator is futile seeing that the microcontroller is powered off its output. A recommendation will be made to consider a separate LDO regulator to power the EPS, so that the 3.3 V regulator can be enabled and disabled. Further advantages would be complete shut down of both power buses[7] in times of critical power while keeping the EPS operational, as well as being able to monitor the *power good* output in a useful manner. However, the increased inefficiency and new failure modes would have to be looked at carefully.

5.4.1 Schematic Design

The schematic for the regulator subsystem is shown in Fig. 5.11. Two Texas Instruments regulators were chosen from their line of Enhanced Products (EP) and Automotive-grade products. As discussed, the EP qualification implies that the device complies with the (desired) minimum standards for space-destined COTS components. Although neither ratings imply immunity to radiation effects, an

[7]Note that an 'off' buck converter completely disables its output, but a non-synchronous boost converter, in its 'off' state, still has a current path through the topology's inductor and diode.

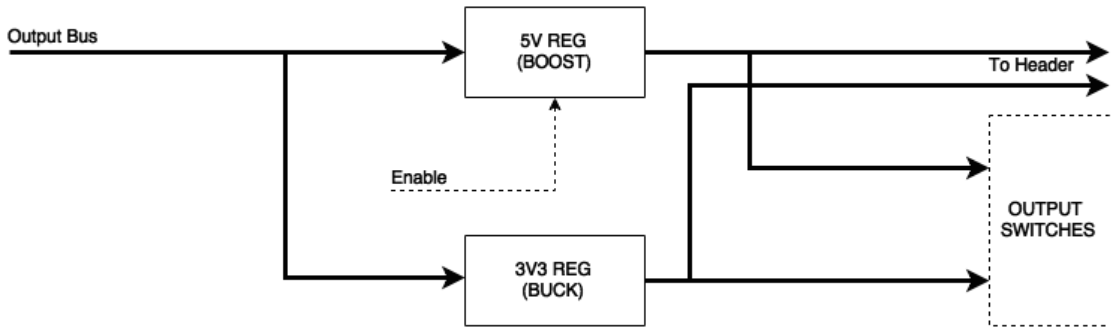


Figure 5.10: Block diagram for the switch-mode regulators.

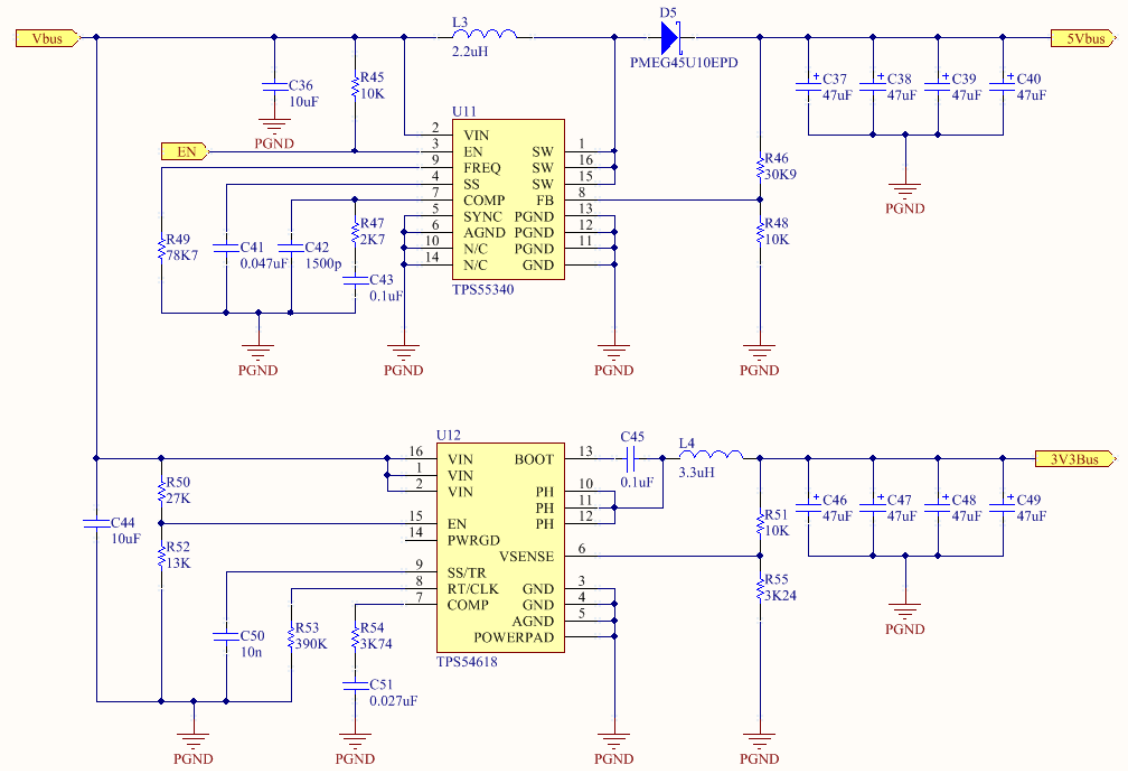


Figure 5.11: Schematic of the switch-mode regulators.

assurance is made that the components are of very high quality.

Boost Converter

The TPS55240 is a 5 A boost regulator that is rated over the extended temperature range, has very small physical size, and has an internal MOSFET with extremely low on resistance that allows efficiencies up to 96%. At a 600 kHz switching frequency, its minimum duty cycle is low enough to allow a 5 V output from the maximum 4.8 V bus voltage. Built-in overcurrent protection sees the output voltage dropping at an output current of approximately 5.25 A.

Calculation of component values was done through a Texas Instruments-provided calculator spreadsheet, and is designed for a 1 A load transient with a maximum 200 mV voltage transient. A minimum of 140 µF output capacitance is needed at a maximum ESR of 27 mΩ. In order to achieve this, four 47 µF tantalum capacitors are used in parallel, each with a maximum ESR of 100 mΩ, resulting in an effective ESR of 25 mΩ. The chosen capacitors are rated for 20 V.

Diode D5 is chosen to have very fast recovery time and small forward voltage. It is rated for a 10 A average forward current (double the absolute maximum current expected) and a 45 V reverse voltage gives a sufficient margin for transient spikes.

The inductor chosen has a ferrite core, a 14 A maximum current rating and a 5.3 mΩ DC resistance. At the maximum 5 A output current (25 W), copper losses amount to just 135 mW. Although its saturation current is 12.5 A, at an rms current of 5 A there is a negligible drop in inductance. Its 8.4 x 7.9 mm footprint is also manageable.

Although a converter with synchronous rectification would provide improved efficiencies and load-disconnect functionality, the addition of (typically) another n-channel power MOSFET suggests a slightly higher risk of radiation-induced failure. This decision remains open for possible change in future.

Buck Converter

The TPS54618 has the same small footprint as the boost regulator, along with an extended temperature range rating and high efficiency using two integrated MOSFETs for synchronous rectification. Its ability to operate up to 100% duty cycle means that it is well capable of a 3.3 V output from a minimum 3.5 V bus voltage. Its low maximum input voltage of 6 V is not problematic.

Seeing that the microcontroller cannot control the operation of this regulator, the R50/R52 divider sets an undervoltage lockout. The divider is set to cut out the regulator when the supply voltage drops below 3.4 V, and only start up again once the supply voltage exceeds 3.7 V. With a nominal 3.5 V minimum, this ensures that the EPS can remain on for even critical supply voltages, while cutting off the external payloads to conserve power. If capacity drops even further, the EPS will also be shut off. If this occurs, the system will be left to build capacity before any payloads are turned on.

A similar output capacitance to the boost regulator is needed, and exactly the same combination of parallel capacitors is used. Similar voltage/current transient requirements are designed for.

The chosen inductor is from the same range as that of the boost regulator and has

the same footprint. Its 7.5 mΩ DC resistance contributes just 190 mW of losses at the maximum 5 A output current, and its ferrite core should also aid in minimising electromagnetic interference. Although rated for 14 A, its saturation current is lower at just 8.5 A. However, at a 5 A rms output current, there is once again a negligible drop in inductance with a temperature rise of just a few degrees.

5.4.2 Failure Analysis

Being single string elements between the main bus and the regulated buses, the two regulators are also single points of failure for their respective buses. Although not points of failure for the entire system, a critical payload that relies on a single supply might nevertheless cause satellite failure should its power supply be lost.

As the system ages, TID effects will cause degradation of the internal MOSFETs that was said to result in reduced switching speeds, increased losses and reduced output capabilities. None of these symptoms are however catastrophic, and operation can continue. The 5 A rating is well above any expected continuous load and thus provides a good safety margin. Switching frequencies for both regulators are still relatively low at around 500 kHz[8], and thus reduced switching capabilities should also not affect performance.

While the boost regulator is available with an Enhanced Products qualification, the buck regulator has an Automotive grade qualification. They can thus be reasonably relied upon to perform under expected conditions. However, the fact that the two regulated buses are provided to the CubeSat header means that an external permanent short circuit that forms on either bus would result in the loss of the bus, and possibly the entire system. It will be recommended that these 'free buses' are not used, but, in addition, a future revision could implement overcurrent protection on each of these bus outputs.

Although the synchronous buck regulator has two n-channel MOSFETs, the fact that the regulator is rated for a maximum 6 V input voltage implies that the drain-source ratings of these transistors is corresponding low. The device should thus not be prone to the risk of SEB.

[8]The regulators are able to operate up to 1.2 MHz and thus it is assumed that they are matched to at least such a frequency.

5.5 Payload Switches

The payload switches serve to provide switch-able and protected outputs to the different payloads. Each is specified to have its output selectable between the 3.3 V and 5 V regulated buses. In addition to including hardware overcurrent protection, there should also be the ability for the microcontroller to trigger a reset as well as control the length of the power cycle.

5.5.1 Subsystem Functionality

The block diagram that implements each payload switch is shown in Fig. 5.12. A hardware-configurable jumper can allow the user to select between a 3.3 V or 5 V output, with the switched output taken out to the CubeSat Kit header.

The switches should operate similarly to the bus control subsystem, in that they default on, and rely on hardware to trigger overcurrent resets. Microcontroller triggers should function over and above this, and thus not be relied upon for proper operation.

Although not included here, a method for permanently disabling a channel will be recommended for future versions. The fact that COTS modules have listed as a feature the ability to set channels to default on or off, along with discrete control of their on/off state, is seen as a potential failure point: a software anomaly, communications breakdown or hardware failure could see a payload permanently switched off. For this reason, an alternative design is preferred whereby active control is needed, through similar capacitive coupling as was used in the bus control subsystem, to set a payload's on/off state. This comes at the cost of increased

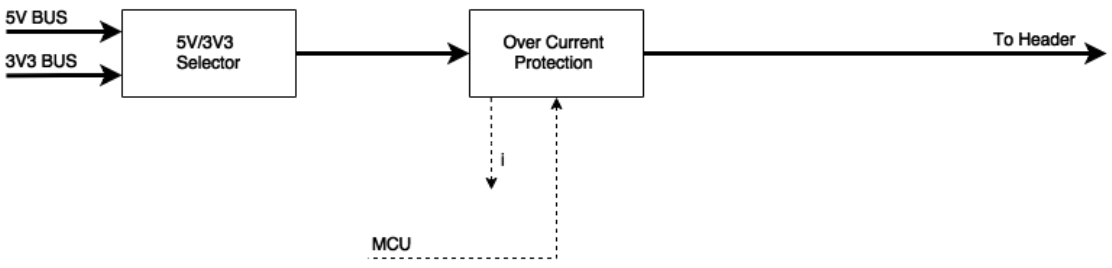


Figure 5.12: Block diagram for the payload switch subsystem.

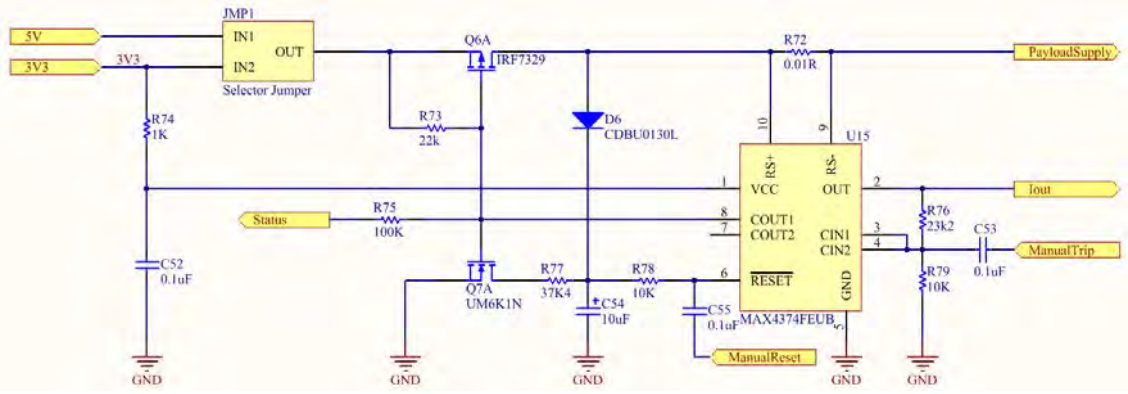


Figure 5.13: Schematic of the payload switch subsystem.

software complexity and marginally-increased power consumption, but the failure modes this avoids is seen to outweigh the disadvantages. The method for permanently disabling a channel would allow complete isolation of a payload should the need arise.

5.5.2 Schematic Design

The bulk of this subsystem follows the same design as the bus control subsystem and will not be repeated here. Each payload switch was specified to be rated for 4.5 A, and the R76/R79 divider is set accordingly. Current-sense resistor R72 should have a 1 W power rating.

In order to conserve physical area, MOSFETs Q6 and Q7 were chosen to be dual-channel packages, with the UM6K1N (Q7) consisting of two 2SK3018 MOSFETs[9]. The IRF7329 is two *p*-channel MOSFETs that are similarly-rated to the AON7407: they have an 'on' resistance of around 20 mΩ at the expected gate bias voltage, a drain-source breakdown voltage of -12 V, and a continuous current rating of 9 A.

The time constant of the reset circuit is set for the same 500 ms cycle of the bus subsystem, although this will be slightly longer for 5 V operation and slightly shorter for 3.3 V operation. Resistor R75 allows an interrupt-enabled microcontroller pin to catch hardware-triggered overcurrent conditions. The Manual Reset input allows premature resetting of the latch circuitry, which enables power cycles shorter than

[9]This is the same device that was used for the bus control subsystem and thus has the same specifications per channel.

the hardware-defined 500 ms. A minimum 4 µs pulse is needed by the RESET input, which is easily achieved through the inherent time constant of R78 and C55.

A problem remains in achieving power cycles longer than 500 ms — in order to trigger another reset cycle, Q6 needs to be switched on long enough for C54 to charge. This pulse should last microseconds, but does mean that a payload that is required to remain off is briefly powered. Although payload capacitance, in combination with parasitic resistance through the CubeSat stack connector, should mean that the supply voltage seen by the payload never rises very high, C55 can always be replaced with a resistor: if the RESET pin is held high, the latch will remain asserted and thus Q6 off.

It was previously calculated that microcontroller pin current, as a result of the fast transition of the capacitive load, is just a few milliamps. However, if multiple pins are being toggled simultaneously, it may be necessary to consider maximum combined current for pins that are on the same supply segment within the microcontroller. Appropriate staggering would negate this potential issue.

5.5.3 Failure Analysis

The failure modes of this subsystem largely mirror those of the bus control subsystem: the most realistic way for the power path to be inadvertently broken is if U15 is unable to pull the gate of Q6 low. Inclusion of the resistor R74 largely avoids the risk of latch-up-induced failure, and capacitive coupling once again provides a high degree of certainly that software and/or hardware anomalies will not affect operation of the subsystem.

Permanent short circuits that arise on external payloads could cause problems through the aforementioned inability to permanently shut off channels. However, a 4 µs typical propagation delay ensures that even if it is left to hardware overcurrent-limiting to continuously trigger power cycles, the effective duty cycle of high current draw is extremely small: this 4 µs period would only occur every 500 ms.

Nevertheless, if a method of permanent isolation is included in future, this issue is alleviated.

5.6 Lithium-Ion Cells

As discussed in detail in Section 4.2, it was decided that energy storage will take the form of a variable number of Lithium Ion (Li-Ion) cells, in independent subcircuits, each interfacing separately to the battery bus. The reasons for such a design included redundancy and avoiding the need for cell balancing.

5.6.1 Subsystem Functionality

Fig. 5.14 shows the block diagram that depicts the individual cell subcircuits, the interface between the battery bus and these subcircuits, as well as the interface to possible external battery modules. When surplus power is available (ie. the satellite is in its sunlit period and generating more power than is needed by the system), the Battery Charge Regulators (BCRs) charge the cells and, when additional power is needed on the bus, power is discharged via the diode element.

The gas gauge sensor monitors cell voltage and current and is interfaced to via an I^2C bus. It was mentioned that available gas gauge sensors do not have enough hardware-configurable bus addresses, and thus an I^2C multiplexer is needed. The multiplexer will be considered in the next section along with additional supporting circuity.

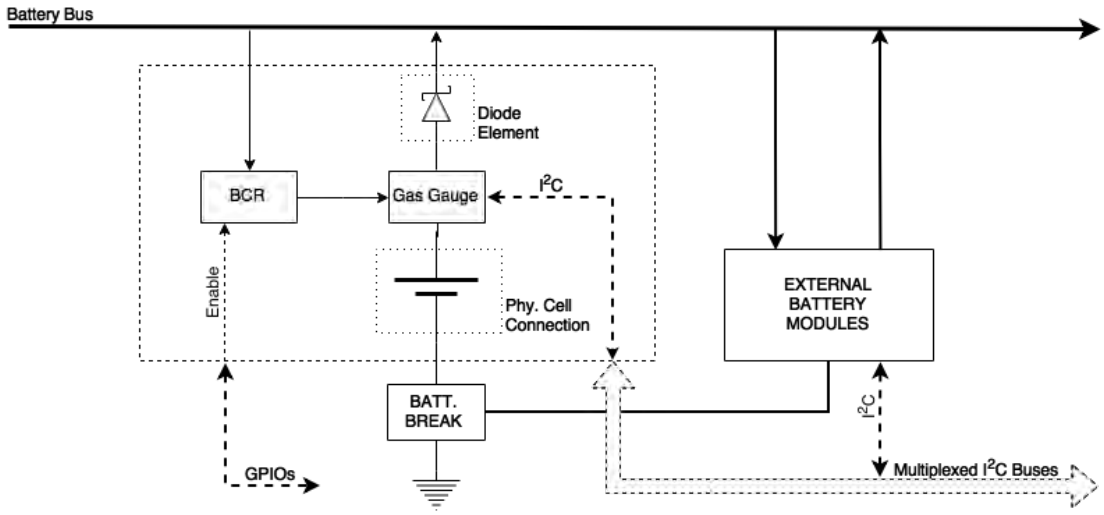


Figure 5.14: Block diagram for the integrated cell subsystems, including the interface to external cell modules.

The battery break connector serves to completely isolate the cells during storage and transportation to prevent discharge. This is implemented as an eight pin header that allows quadrupling of pins. Standard 18650 cell holders will be used initially, but a more robust method, such as welded tabs, will be needed for a flight-ready module.

5.6.2 Components

The choice of the three main components will be looked at in some detail, due to their importance to efficiencies and system capabilities.

Battery Charge Regulator

The BCR needs to allow charging of a single Li-Ion cell from a 3.5–4.8 V supply voltage. A wide selection of such regulators is available, that manage a safe charge current, while tapering off at a fixed float voltage. During selection, the critical criteria were considered to be hardware-settable parameters (ie. not reliant upon a digital interface), switch-mode regulation, the ability for charging to be disabled, and small physical size.

A large number of devices was looked at from manufacturers Linear Technology, Texas Instruments, Maxim Integrated and Analog Devices. The above criteria limited choice significantly and, from the potential candidates, differences in specifications were mostly negligible.

The LTC4001 from Linear Technology was chosen for its suitability, the additional functionality it provides, as well as its tiny 4 x 4 mm QFN package. With a 1.5 MHz switching frequency, the external inductor can be very small. A useful feature it offers is programmable charge current, allowing for more efficient regulation of bus power as well as flexibility for future software-based improvements. While the LTC4001 has a fixed 4.2 V float voltage, a drop-in replacement, the LTC4001-1, is available that has a 4.1 V float voltage. For missions with a long design life, this would likely be a desired feature to prolong battery life as far as possible. The device also allows charging from any supply voltage, greater than its 2.75 V undervoltage lockout, so long that it is 250 mV above the cell's terminal voltage.

Charge current is set according to a multiple of the current delivered by a specific pin (the PROG pin) — with the pin regulated to a fixed voltage, charge current can thus be dynamically programmed via either a digital potentiometer (DP), or a current-output DAC. However, availability of such DACs with the required ouput range is extremely limited and, for this reason, a digital potentiometer was decided upon.

The AD5246 128-position digital potentiometer from Analog Devices was selected for its simple operation, tiny physical size and < 1 µA supply current over the 3.5–4.8 V bus voltage. It also does not implement unnecessary I^2C address inputs (the subcircuits have their I^2C buses multiplexed) nor an unnecessary third wiper terminal. A 10 kΩ wiper resistance allows for the required range of current settings. Resistance is set through a one-byte data word that is written to a volatile register. This register can also be read back through a read request.

Gas Gauge Sensor

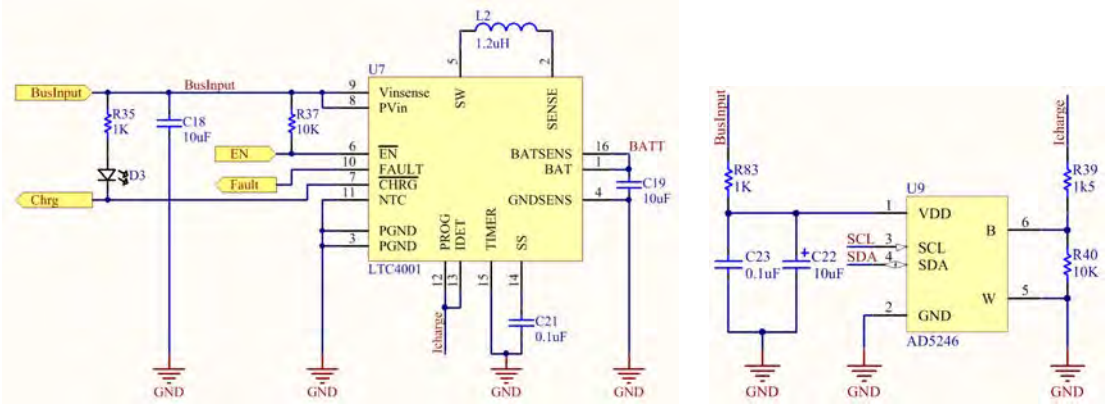
A wide range of gas gauge sensors was looked at, with the fixed criteria being designed for a single cell, low-power operation, high efficiency (in terms of current monitoring) and an I^2C interface[10]. Although some suitable sensors are available from Linear Technology, the BQ27411 from Texas Instruments was chosen. Similarly to selection of BCRs, functionality and specification differences between different devices are generally negligible. The BQ27411, however, offers an extremely low-power sleep mode, as well as a wide range of monitoring capabilities.

Ideal Diode

An ideal diode was chosen to implement the diode element for the near-100% efficiency it offers. Although there is an added risk of failure, redundancy in this subsystem makes this acceptable. Furthermore, the inherent MOSFET has its internal body diode to serve as a backup for certain failure modes.

The ideal diode controller was chosen to be the LTC4412 from Linear Technology.

[10] Alternative interfaces are typically UART (requiring separate UART interfaces for each device) or propriety standards such as a one-wire serial interface (thus also requiring multiplexing or separate interfaces).



(a) (b)

Figure 5.15: Schematic of the cell subsystem's (a) battery charge regulator and (b) the charge current-setting digital potentiometer.

Once again, a number of choices were available but with marginal differences. The LTC4412 drives an external *p*-channel MOSFET and is rated for the necessary voltage range. The previously-used AON7407 MOSFET was chosen for its suitability and the fact that it is already on the bill of materials. With the AON7407's 'on' resistance and the LTC4412's 11 µA quiescent current, the device allows diode-like functionality at 98%+ efficiency.

5.6.3 Schematic Design

The schematic components will be discussed separately. Each combination of BCR, gas gauge, ideal diode and digital potentiometer will form one of multiple independent cell subsystems. Also discussed is the interface for the connection of external battery modules, further consisting of multiple cell subsystems.

Battery Charge Regular and Digital Potentiometer

Fig. 5.15 shows the schematic design of the BCR and accompanying digital potentiometer. A design decision for a maximum charge current of 1.2 A is made, seeing that with multiple cells being charged simultaneously, along with system power demands, it is unlikely this will ever be insufficient to make use of all available solar power.

In terms of charge termination, the LTC4001 allows the option for an externally-set maximum charge time, or for a trickle-current threshold to be set, also via an external pin. It is thought that the inherent regular charge cycles, that the orbital path effects, negates the need for time-based termination, and thus the TIMER pin is pulled to ground to disable the functionality.

The PROG pin programmes the high-rate charge current, while the IDET pin programmes the charge termination current threshold. Internal implementation is such that the these currents are multiples of the currents drawn from the respective pins. In order to have control over both currents without using two DPs, both pins are tied together, with operation as follows: During full-rate charging, the charge current is set by the DP. As the battery charges, it will reach a point where charge current naturally falls below the minimum-settable current. At this point, the DP can be set such as to programme the current through the IDET pin, thus setting the termination threshold.

Inductor L2 is specified to be 1.2 µH. The datasheet provides the necessary equations to calculate the peak inductor current, which, accounting for a 4.8 V maximum input voltage and 1.2 A maximum charge current, is 1.62 A. A Wurth Electronics moulded inductor was chosen. With a DC resistance of 106 mΩ, more efficient inductors are available although at the cost of physical size. Depending on available area, a different choice could be made for a future revision, and at the least should be made for an external battery module.

LED D3 provides a visual indication of charging, and is included for testing purposes. A flight-ready module should leave this unpopulated. The FAULT pin provides a digital indication of a detected battery fault, while the EN pin allows charging to be disabled. The thermistor NTC input is left unused initially, but could be incorporated in future.

Resistors R39 and R40 serve to provide a suitable range of charge currents for a failed DP. The DP has three possible failure modes: the B pin may be inadvertently tied to ground, there may be a break in the dynamic wiper path, or the device may be left uninitialised — due to a loss of communications — and thus at its 5 kΩ default resistance.

Fig. 5.16 shows the variation in programmed charge current over the full 10 kΩ wiper

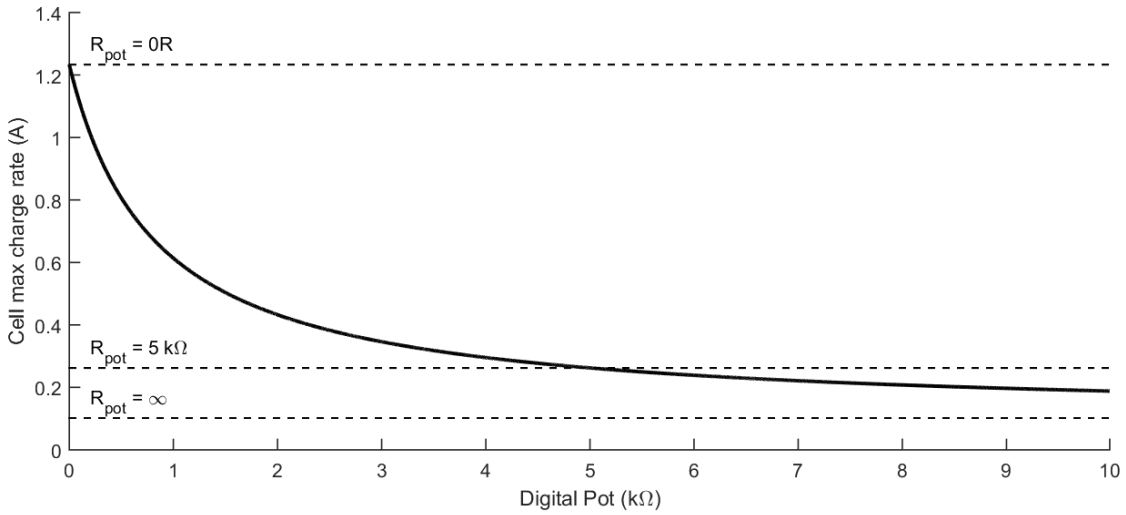


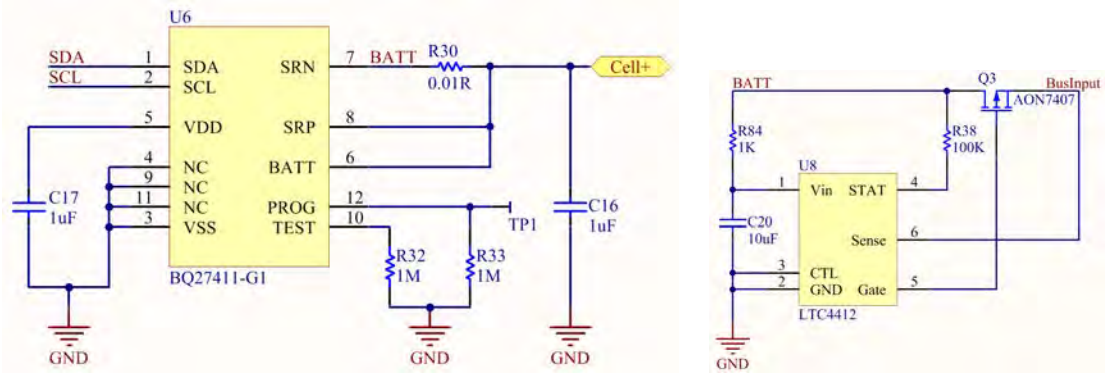
Figure 5.16: Variations in cell charge current over the digital potentiometer range.

range. The horizontal lines show charge currents for the above mentioned failure modes; R39 and R40 thus provide workable defaults, whilst adding an acceptable degree of non-linearity.

Gas Gauge and Ideal Diode

The schematic design of the gas gauge sensor and ideal diode is shown in Fig. 5.17. Sense resistor R30 will conduct the full cell current and thus should have a 1 W power rating. A 7.4 V voltage applied to the PROG pin enables writing of one-time programmable (OTP) memory that allows configuration settings be permanently saved. With a large number of internal configuration registers, making use of this functionality would be beneficial.

The **BATT** net sees current flow into the cell during charging and out the cell during discharge. This current flow is monitored by the gas gauge, and discharge is done via the ideal diode. The STAT pin allows external monitoring of diode status, but this can easily be determined by the sign of the average current reading, as determined by the gas gauge. The controller can also be forced to turn the MOSFET off through the CTL input, although the inherent body diode of the AON7407 makes this futile.



(a) (b)

Figure 5.17: Schematic of the cell subsystem's (a) gas gauge and (b) ideal diode controller.

External Module Interface

Specifications suggested that in addition to two integrated cells, there should be the capability to link external battery modules for missions with greater power requirements. It was decided that this should take the form of a physical header that links the external board to the EPS module. From the block diagram in Fig. 5.14, it is clear that four connections are needed: the battery bus, the battery ground connection, and an I^2C bus. It may prove better to rather have two separate battery break connectors — one on the EPS module and one on the external module — so that the external batteries' ground can be directly interfaced to the CubeSat header to improve performance.

The fact that GPIO pins are needed to monitor and control the LTC4001 means that an I^2C-based GPIO expander will be required on the external module. This is considered preferable to the large number of digital lines that would otherwise need to be routed to the external board. In order to accommodate the multiple cell subcircuits on the external module, an additional external I^2C multiplexer will be needed. This is also considered preferable to multiple I^2C buses routed to the external board.

5.6.4 Failure Analysis

The failure modes of this subsystem will be considered in two sets: failure modes that affect only the subcircuit, and those that affect the external system. Redundancy ensures that the former set are not single points of failure, but nevertheless will affect system performance through the loss of storage capacity.

Internal Subcircuit Failures

The BCR is a single point of failure in the context of the subcircuit, in that its failure would mean the cell can no longer be charged, and would thus be lost. Such a failure could manifest itself in two ways: firstly, an internal failure that disables switching, or secondly an external failure that results in the EN pin never pulled to ground (and thus never enabling charging). Although the first failure is unavoidable, the internal block diagram suggests that a trickle charge *may* continue to flow into the battery. However, to prevent the second it might be better to rather pull the EN pin to ground by default, and use the microcontoller to override this if charging needs to be disabled. It is suggested that, in such a design, a system of permanently disabling charging is incorporated, to ensure failed cells are never an unnecessary drain.

As was shown previously, failure of the DP simply results in fixed maximum charge currents. A latch-up event is protected against through the inclusion of R83, although it needs to be tested that the time constant, created with the suggested 10 µF decoupling capacitor, does not impact the device's power-up cycle.

Failure of the ideal diode controller could result in the MOSFET either switched permanently on or off. The body diode ($V_f = 520$ mV typical) ensures that being permanently off simply adds some loss in efficiency, and being permanently on means the cell will be directly charged from the bus. This could have consequences if the micrcontroller is unable to limit the bus voltage to 4.2 V. However, a specification for cells with integrated over-voltage protection would provide a backup against this failure mode[11]. Similarly to the DP, a latch-up event is protected against and will likely clear itself.

[11]This protection circuit would, in turn, also become a point of failure, and would need to be chosen carefully.

Loss of the gas gauge would simply mean loss of cell information, and is not a critical failure. The fact that it has no direct connections to the bus means that it cannot impact the external system. A latch-up protection resistor is, however, not possible on this device, seeing that the BATT input is used for both the internal regulator supply and battery voltage monitoring: at its maximum 100 µA supply current, the voltage drop would produce unacceptable errors. An option exists of using a positive temperature coefficient (PTC) thermistor and should be investigated further.

External Failures

The only two components with direct influence on the bus are the BCR and ideal diode. Failure modes of the ideal diode controller were considered and unless an internal short circuit forms within the cell, they have no critical consequences for the external system. Nevertheless, such a catastrophic failure is not protected against in other known systems and is thus not an additional failure mode in this EPS. In fact, the inclusion of dedicated charge regulation per cell should improve the reliability of cells.

As discussed, a failure of the BCR results in the loss of system storage capacity. However, an internal latch-up event within the BCR would cause a direct drain on the bus and, with no method of power cycling the battery bus, it is possible this will not clear. Although recommendations will be made to better address this, the fact that this is not a single string element means that it is unlikely it will cause system failure.

5.7 Supporting Circuitry

The following sections look at the selection and operation of the remaining supporting circuity. Schematic design of the microcontroller itself is not looked at here and can be found in Appendix D — its selection has already been discussed and few modifications are made from manufacturer-recommended design that consists simply of passive decoupling, a 16 MHz resonator and a 32.684 kHz crystal as an input for its Real Time Clock (RTC) module.

5.7.1 CAN Transceiver

CAN transceivers all provide similar functionality, and allow interfacing between the differential bus and logic-level transmit and receive outputs/inputs. The Texas Instruments SN65HVD233 was selected for its availability in their Enhanced Products range. Its schematic can be found in Appendix D.

5.7.2 I^2C Interfaces

It was noted that if the satellite uses an I^2C communications bus, an external I^2C bridge will be needed: the microcontroller needs one interface operating in master mode, and one in slave mode. If a CAN bus is used, the internal I^2C interface can be used as the master while the external interface is left unpopulated.

Two options are available, that of having the external module implement a bus master or a bus slave. The former option means the external module would be used to interface to the EPS's I^2C nodes, while the second would mean it would listen for commands on the satellite bus.

Choice of I^2C interfaces is very limited, with the only two viable options the SC18IS602 (I^2C slave to SPI master) and the SC18IS600 (SPI slave to I^2C master), both from NXP Semiconductors. This design decision is made simple through an efficiency consideration: The SC18IS602 has no power-down mode and thus its 3.3 mA idle supply current will be a constant power drain. However, the SC18IS600 has a low-power mode, triggered by a GPIO pin, that sees supply current drop to

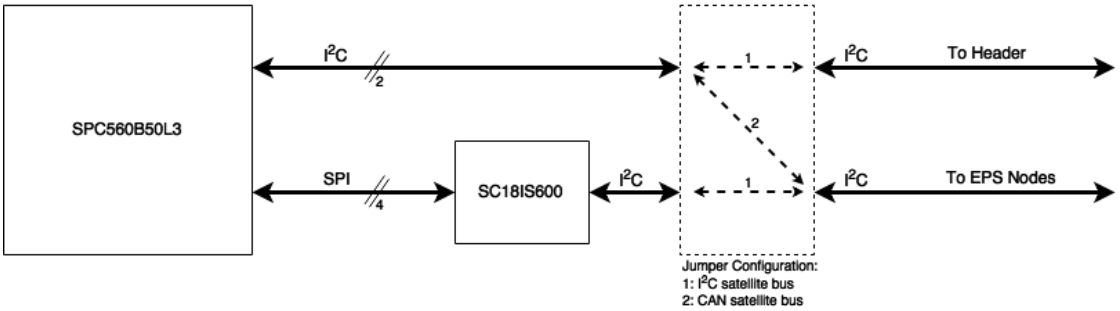


Figure 5.18: Block diagram for I^2C bus configurations.

$\ll 1$ µA. Being the I^2C master, this mode can be entered into whenever communication with EPS nodes is not needed.

Fig. 5.18 shows the block diagram depicting the different I^2C bus configurations, and the schematic can be found in Appendix D. The jumper is implemented through four zero-ohm resistors: for the first configuration, where an I^2C satellite bus is used, R57 and R67 should be placed with R69 and R70 left unpopulated; for the second, R69 and R70 should be placed with R57 and R67 left unpopulated. In this second configuration, the SC18IS600 (U14) can also be left unpopulated, although if it is present, software can simply keep it in its low-power sleep mode.

Multiplexer

The four-channel PCA9546A I^2C multiplexer from Texas Instruments was chosen. A one-byte data word selects one or more downstream pairs (SDA and SCL), and a reset input can put the device into a low-power mode in which it consumes $\ll 1$ µA. This multiplexer will allow the system to communicate with either of the onboard cell subcircuits, or with an external battery module.

As discussed, an external battery module would need a further multiplexer to select between its cell subcircuits. The PCA9546A also allows for a range of hardware-selectable bus addresses, meaning that this same device can be used across multiple external modules. Once again, the schematic can be found in Appendix D.

5.7.3 External Interfaces

The module will have two external interfaces — one intended for development, and the second for pre-flight configuration, testing and charging.

JTAG / Debug Port

An 11-pin low-profile connector is used to connect to the SPC56B-Discovery development board. This connection allows programming of the microcontroller via its JTAG interface, connection to the development board's integrated serial transceiver, as well as a battery bus connection for external powering and/or charging. The modifications needed to the development board along with the required pin mapping is detailed in Appendix E.

Flight Preparation Port

A second 7-pin low-profile connector is intended to serve as an umbilical cord for the EPS, allowing triggering and resetting of the separation switch (for testing purposes), and connection to the same serial interface as the debug port for configuration and pre-flight diagnostics. A connector pin also serves the Remove Before Flight pin, and another allows external power input for cell charging.

The design and functioning of a separate board, that incorporates appropriate connectors and switches, as well as a USB-serial transceiver, is documented in Appendix B.

5.8 PCB Design

The previous schematics were designed in Altium Designer, with a corresponding printed circuit board laid out. All design files can be found in the supporting material. To minimise costs during the development phase, a two-layer board was designed. Although a two-layer board is sufficient for the level of component complexity and given the absence of high-speed digital interfaces, a four-layer board, with internal ground planes, may be necessary to improve efficiency through greater available copper area as well as noise performance, both radiated and received.

As far as possible, all passive components were chosen to have an 0603 footprint to minimise their required area. Ceramic capacitors were also ensured to have an X7R temperature coefficient or better. Assembly was done by hand and photographs of the assembled board can be seen in Appendix A, along with further descriptions of component placements and layout considerations.

Initial layout considerations were based on the fixed PC/104 mechanical outline, including the positioning of the CubeSat header and the mounting holes. It was also necessary to place the Li-Ion cells on the top and centre of the board for optimal mass distribution. Furthermore, the CubeSat Kit specifications allow for a maximum component height of 4 mm on the underside of modules: this means that all inductors and physical connectors need to be placed on the top side.

The selection between 3.3 V and 5 V for each payload switch is done via a solder jumper, with Fig. 5.19 showing the copper design. While minimising space, care will have to be taken that short circuits between buses cannot form, and for this reason it is suggested that these jumpers are covered with an insulating epoxy or resin before flight.

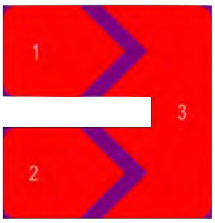


Figure 5.19: Copper layer of the solder jumper design: voltage selection is made by bridging terminals 1 and 3, or 2 and 3.

Chapter 6

Software Design

The following chapter outlines the software designed to run on the microcontroller that manages the EPS, its housekeeping, power point tracking, and additional functionality. Full code and project files can be found in the accompanying material, with additional descriptions and information in Appendix E.

Although the device uses Freescale's e200z0h Power Architecture core, this is largely abstracted away through all code being written in C. Some assembly code was however written to implement the software-based core interrupt handler that performs the handshaking between the external interrupt controller and processor.

An important consideration in the software design is that the interrupt controller provides priority-based, pre-emptive scheduling of interrupt requests; it must be ensured that interrupts that use shared resources, such as the I^2C module, cannot pre-empt each other.

Software design has been broken into a set of low-level drivers that are built directly on the integrated modules and peripherals, a set of higher-level abstraction functions that implement external interaction, and finally a set of functions that implement system monitoring, housekeeping and power point tracking.

Before these sets of functions are outlined, some of the important features and peripherals will be briefly described and discussed first. Information on microcontroller features within this section is a consolidation of datasheets, reference manuals and application notes — in particular, [68], [69] and [70].

6.1 Microcontroller Features and Peripherals

The following features and peripherals are considered central to the software design and/or differing slightly from common implementations. Not mentioned are the more standard features such as the software watchdog timer, real time clock or communications interfaces — these are briefly described in the section that follows.

6.1.1 Power Management

A complex power-management module is available that is not fully taken advantage of in the current software revision. A set of 'RUN' modes are available — including RESET mode, SAFE mode, DRUN mode, and modes RUN0..3 — with each mode capable of configuring pad control, the main voltage regulator, the power status of the flash modules and the system clock source. Low-power modes HALT, STOP and STANDBY have similar control but, depending on the mode, configuration is limited to just the clock source. An external 16 MHz resonator has been included, but fast and slow internal RC oscillators exist.

A set of eight 'run mode' and eight 'low-power' *peripheral groups* then exist, with each group selecting one or more run modes, and one or more low-power modes, that it is active in respectively. Each peripheral then selects *a* run-mode group and *a* low-power group that it belongs to.

It is difficult to design these different configurations until the entire software system has been developed, tested and its performance characterised. The time necessary to exit a low-power mode and resume operation will need to be considered carefully, along with the increased power consumption during mode switching. Standby mode, which has the lowest power consumption, shuts down power to most of the device including all peripherals; a time-based interrupt from the RTC module is needed to generate a wakeup request.

6.1.2 Memory Interfaces

Three memory interfaces are present on the device — 512 KB of program/code flash, 32 KB of SRAM, and 64 KB of data flash. All memory has hardware-implemented Error Detection and Correction (EDAC) that uses an Error-Correcting Code (ECC) technique to protect data integrity.

A conventional single-error-correcting-double-error-detection (SEC-DEC) Hamming algorithm, requiring 7 check bits per 32-bit word or 8 check bits per 64-bit double word, is used by the ECC block present on each memory interface. Although the RAM's ECC block protects data on 32-bit word boundaries, both flash interfaces protect data on 64-bit double-word boundaries. Single bit errors are automatically corrected by the hardware, are flagged in a status register for the respective module, and can generate a standard interrupt. Non-correctable errors however are handled differently for each memory interface and are discussed below for each.

All bit errors are further reported by the separate Error Correction Status Module (ECSM), consolidating various error information and providing the last affected address as well as the corrected data associated with single-bit errors: although this corrected data is returned to the core on the internal data bus during the transaction, the actual memory bits are left unchanged. It is up to application software to write the corrected data to the appropriate address, by using the data provided by this module.

Furthermore, ECC checks are only performed during read operations[1]; thus, the application needs to periodically read the contents of memory and, where necessary, correct single-bit errors. This prevents the accumulation of errors and should usually avoid non-correctable errors occurring. If available, it is suggested that the Direct Access Memory (DMA) module be made use of to remove this task from the processor.

[1]For RAM, write operations on 8- and 16-bit boundaries have an inherent read in order to generate the new ECC for the full 32-bit word.

Code Flash Module

The 512-KB flash array used for code storage is implemented as a single array consisting of eight sectors. Read-while-write (RWW) operations are not supported and thus software to correct single-bit errors would need to run out of either RAM or data flash. The large size does, however, provide the possibility of storing separate application images as contingency for non-correctable flash errors: a small application, dynamically placed in RAM or simply placed in data flash, could be used to update the reset vector.

In fact, each of the eight sectors within code flash have an 8-byte boot sector that, if programmed correctly, defines the sector as bootable — the first valid boot sector is used for application entry. Thus, the non-correctable error handling software could simply corrupt the boot sector of the affected flash sector[2].

On detection of single bit errors a similar small application, running on a different memory interface, will need to use the data provided by the ECSM module to write the corrected data to the appropriate address. However, a complication arises in that bits in flash memory can only be programmed from a '1' to a '0'; thus, a bit flip from '1' to '0' cannot be re-programmed back to a '1' without erasing the entire sector. The aforementioned duplicate flash images would need to be made use of, to copy back the entire sector.

Non-correctable errors are not only signalled by the ECSM module, but also result in a core-level interrupt, due to the inherent error on the data bus. Different core interrupts occur for data-fetch and instruction-fetch errors, with the latter being the more serious. If a further error occurs while trying to recover in such an interrupt, the microcontroller is automatically forced into a state that generates a reset.

SRAM Interface

As mentioned, the SRAM's ECC mechanism uses a 7-bit ECC to protect each 32-bit word. Thus, 39-bits are stored for every 32-bits of data: this has consequences

[2]The corruption would need to ensure that the ECC is not interfered with as this may cause reliability issues during microcontroller boot. There exist different sequences of bits that result in the same ECC [70].

for 8- or 16-bit data accesses where the entire register needs to be read for calculation of the new ECC. Depending on the previous instruction, this can cause a few wait states to be asserted. Although the application is not expected to need such performance optimisation, it could be kept in mind for future performance enhancements.

Handling of single-bit errors is similar to that in flash memory: errors are flagged and can generate an interrupt, but the corrected data needs to be written to the affected address. Where handling of non-correctable errors differs is that for RAM, these are not considered critical by the core and the application can decide whether to terminate the system or simply write over the affected memory address. Because a new ECC now needs to be generated, the entire 32-bit word containing the affected address needs to be written.

Upon reset, RAM may contain unknown data and thus, for ECC purposes, the entire RAM block needs to be initialised. This is done during the boot process, and requires that 32-bit words are written to all RAM locations.

Data Flash Interface

Data flash has a very similar implementation to code flash: it is a single 64 KB array consisting of four sectors that are individually-erasable. RWW operations are also not possible and an entire sector needs to be erased in order to overwrite previously-written data. Because ECCs are calculated for double words, data needs to be written on 64-bit boundaries regardless of the length of data being written. Furthermore, because the ECC is calculated and set on the first write, even if only part of the 64-bit block is initially written, subsequent writes to the same block will likely result in an ECC error.

When a data-fetch generates a core-level interrupt, the handler can decide to continue from a known point; this could be the next instruction, or a specific external handler that deals with a data error. This is accomplished in the interrupt handler by modifying a register that contains the program counter before the interrupt handler was entered into.

6.1.3 Analogue-to-Digital Converter

The Analogue-to-Digital Converter (ADC) module is a single 10-bit converter that interfaces to 28 analogue input channels. Three different types of conversions are available and used by the application: *normal* conversions, *injected* conversions and *Cross-Triggering-Unit (CTU)-triggered* conversions. Normal conversions consist of a chain of selected channels, generating an interrupt once all conversions have been completed. While these conversions are ongoing, an injected chain can be started that temporarily pauses the normal conversions. On top of this, a specific channel can be triggered for a conversion via the CTU; these conversions have highest priority that pause the normal conversion chain and in fact abort an injected chain.

The CTU is a separate module that can trigger specific ADC conversions upon events within the Timer module, the benefit of this being that no processor intervention is needed; the application can simply be reliant upon the respective interrupt being called once the conversion has completed.

Analogue Watchdog

A useful feature of the ADC module is four analogue watchdog channels: four separate ADC channels can be configured to generate an interrupt when their converted value falls outside a set range. With appropriate interaction between the Timer module, CTU and ADC, a specific ADC channel can be periodically sampled, only requiring processor interaction once a threshold has been crossed.

6.1.4 CAN Module

With an automotive-focused design, the integrated CAN module, named *FlexCAN*, is highly capable and has substantial functionality. Proper use of CAN requires definition of CAN messages and corresponding message identifiers that define the message's priority; seeing that there is currently no definition of either, development of CAN communications has been neglected in the current software version.

A useful feature to take note of is the *CAN Sampler* module that has the ability to sample the first two incoming CAN frames while in standby mode (and thus the

FlexCAN module disabled). Upon wakeup, these frames can be analysed by the application to determine if it was requested to interact with an external system.

6.2 Functions

6.2.1 Low-level Functions and Drivers

The following groups of functions allow abstraction from the integrated modules and were developed through consultation with the microcontroller's reference manual and some very limited, manufacturer-provided, driver libraries. Unless they perform special functionality, initialisation functions, including other simpler functions, are not listed.

System

`SYSTEMInit(void)` Performs basic system initialisation, including the vector table and ensuring the device is in the correct RUN mode. The system settings structure is also copied out of flash and into RAM with its validity checked. Finally, the error logging mechanism is initialised, along with the real time clock in order for error logs to have a valid timestamp.

`SYSTEMStoreSystemSettings(void)` Stores the system settings structure from RAM into flash — this involves erasing the relevant flash sector.

`SYSTEMLogError(ErrorCode code, char param)` Logs a system error (or status message) to flash. Different errors are given a code and can have an associated parameter that provides more information about the error. String descriptions of the different errors are also stored in flash and, if the system settings' debug flag is set, this function will also print out the error to the serial interface. Error codes also have an associated priority which can be used to filter error messages.

`SYSTEMGetErrorLog(ushort index, SYSTEMErrorLog *log)` Fetches the error log with the given index. This can be used by ground crew to request different status logs.

SPI Interface

`SPIExecuteTransaction(SPITransaction * txn)` Takes an SPI transaction structure and synchronously performs the requested transaction. A status byte within the structure is set that indicates whether it was successful or, if not, provides a reason for the error. Future optimisations could make this an asynchronous operation although, with minimal SPI transactions needed, it is unlikely the added complexity will justify the performance gain.

Internal I^{2}C Interface

`I2CExecuteInternalTransaction(I2CTransaction * txn)` Similar to SPI, it performs a synchronous I^{2}C transaction in Master mode using the internal module.

Analogue-to-Digital Converter

A number of functions are available to set and unset specific channels for different conversion types, and to enable and disable various interrupt types for the watchdog channels. Some interrupt handlers provide abstraction from determining the exact cause of the interrupt and, in turn, call event-specific handlers. These event handlers are weakly defined and can be overridden by other modules.

`ADCSetupWatchdog(ADCWatchdogChannel ch, uchar adc_ch,`
`ushort u_thres, ushort l_thres)` Enables an ADC watchdog channel with given upper and lower threshold values.

UART Interface

The UART interface is only initialised when in flight preparation mode and is used to provide command-line-type functionality to test and debug the system. Received data is added to a buffer and, when a newline character is received, a flag is raised that indicates a command to be parsed. Command parsing is taken outside the handler and into the main loop to ensure it does not interfere with more important software routines.

Timers

Although 28 independent timer channels exist, only 12 of these can be used to generate timeout events. Similarly to the ADC, a number of interrupt handlers provide abstraction from determining the channel and type of interrupt, and call channel-specific handlers that can be implemented by other modules.

`TIMERSSetupTimeoutChannel(TimerTimeoutChannel ch)` Sets up a given channel for timeout-based operation.

`TIMERSStartTimeout(TimerTimeoutChannel ch, uint match_value)` Starts the timer to generate a timeout at the given match value. The `TIMER_MILLISECONDS(ms)` macro converts a milliseconds value to the corresponding match value.

Data Flash

The DFLASH functions allow abstraction from the specific sequences of events involved with writing to the flash array. This involves locking and unlocking sectors, and ensuring that data is written on the correct boundaries for ECC purposes.

`DFLASHSectorErase(DFLASHSector sector)` Erases a given DFLASH sector. The function waits until the sector has been erased which takes in the order of milliseconds — this should be considered if erase operations need to take place during critical software routines.

`DFLASHWrite(DFLASHSector sector, uint offset, uchar len, uint *buffer)` Writes a given length of data (in bytes) from a buffer array, starting at the given offset within the sector. The function ensures that the offset falls on the correct boundary and that the sector is not overrun.

Software Watchdog Timer

A standard software watchdog timer module allows the generation of an interrupt on an initial timeout, and a reset on a second consecutive timeout. The module is configured during system initialisation and the initial interrupt functionality is

used to log a system error before forcing a system reset. A future hardware revision should consider the addition of an external hardware-based watchdog timer for increased system reliability.

Real Time Clock

The real time clock is configured to use the external 32.768 kHz crystal as this can be specified for the anticipated temperature environment. A simple 32-bit counter, set to zero on reset, implements the clock and is set for a 500 ms resolution. If the EPS receives a UTC timestamp from an external payload, it could update this timestamp to reflect an absolute time.

`RTCGetTimestamp(RTCTimestamp * timestamp)` Sets the given timestamp structure. This structure has a flag bit that indicates whether the timestamp is relative to the last reset, or whether a UTC timestamp has been received and now indicates an absolute time.

All system error/status logs include a timestamp and all reset events, as well as transitions from relative to absolute time and timer roll-over events, are logged. Thus, an analysis of system logs should be able to construct a fairly accurate timeline, should critical failures need to be diagnosed.

6.2.2 Abstraction Functions

The following set of functions provide interaction with the external devices and make use of the low-level drivers.

External I²C Bridge

The SC18IS600 SPI–I²C bridge's module has a number of functions for initialising the device, writing to and reading from internal registers, powering-down the device and waking it up. These functions make use of `SPITransaction`[3] objects and provide the application with abstraction from the SPI-I²C conversion process.

`SC18IS600ExecuteI2CTransaction(I2CTransaction * txn)` Executes an I²C transaction via the bridge. To the application, it provides identical functionality to `I2CExecuteInternalTransaction`.

`I2CExecuteEPSTransaction(I2CTransaction * txn)` Although part of the I²C module, this function provides abstraction from determining which interface needs to be used for communication with EPS nodes. It automatically delegates the transaction to the bridge or the internal module, depending on system configuration.

Multiplexer

I²C multiplexing takes place via the PCA9546A — depending on hardware jumper configuration, it uses either the SC18IS600's bus or the microcontroller's bus that it switches to the different cell subcircuits, as well as the bus for external battery modules.

`PCA9546ASelectChannel(PCA9546AChannel channel)` Selects a given channel, and logs an error if it was unsuccessful. When additional multiplexers are used on external battery modules, this function will also provide abstraction from the multi-stage multiplexing sequence.

[3] As a note for future development, the SC18IS600 appears highly sensitive to the delay between the clock line going high to the MOSI line going high. The internal SPI module allows for some control over this period, and is set up during SPI initialisation.

`I2CExecuteCellTransaction(Cell cell, I2CTransaction * txn)` Also part of the I^2C module, this function provides further abstraction from the multiplexing process and allows the application to communicate with a desired cell regardless of whether it is on an external module or not, or if the internal I^2C module should be used or the external bridge.

BQ7411

Interaction with the gas gauge sensors takes place through the BQ7411 module, which provides functions for performing read and write commands, reading and writing to internal registers, and setting default values to volatile registers. The functions used during nominal application flow are as follows:

`BQ27411Init(void)` Ensures the device is responding correctly by testing the values returned from one-time programmable registers and, if necessary, sets register defaults.

`BQ27411ReadCommand(uchar command, ushort subcommand, uchar bytes)` Returns the result of a read command, typically used for fetching cell voltage, average current and (estimated) state of charge.

Input Stages

The input stages are interfaced to via the PV module, which includes enabling and disabling the SEPIC regulators and setting the DACs.

`PVChannelSet(PVChannel ch, uchar value)` Ensures the respective channel's regulator is enabled and sets the DAC with the given value. Because the series diode in the hardware implementation means that DAC ouput voltages below the diode's forward voltage serve no purpose, a value of zero will result in the software configuring the DAC for its lower power mode. The calling function should use a zero value when it does not intend control.

6.2.3 System-level Functions

This final level of abstraction includes a set of functions that implement intelligent control of the system, making use of both sets of previously-defined functions. These functions will only be briefly described here, but their internal flow and operation, within the context of the overall software flow, will be described in their own sections that follow.

Maximum Power Point Tracking

Each input channel has a structure placed in flash and another in RAM. The flash structure stores channels' port control indices, ADC channel indices and some further static channel-specific data. This allows the MPPT functions to operate on a given input channel by referencing the appropriate offset of the array of said structures. This avoids many 'if-else' statements that would otherwise be needed to determine which channels and pins to operate on.

The RAM structures are implemented for a similar reason, and contain a multitude of flags, variables and settings that are used and dynamically set by the algorithm.

`MPPTInit(void)` Initialises the MPPT channels. An analogue watchdog is assigned to each array voltage input — when an upper threshold is crossed, the algorithm is initiated; when the lower threshold is crossed, the algorithm is aborted. A Timer timeout channel is also assigned to each input that allows a variable step size be used per channel.

`MPPTEnable(PVChannel ch)` This function is called automatically by the appropriate threshold violation on the analogue watchdog channel and initiates the MPPT algorithm. Various flags and variables used by the algorithm are initialised and the watchdog is configured to detect low-voltage inputs.

`MPPTDisable(PVChannel ch)` Similar to the enable function, this function is also called automatically on a threshold crossing on the analogue channel and ends the MPPT algorithm. The watchdog is once again re-configured.

`MPPTTriggerConversion(PVChannel ch)` The MPPT module uses injected conversion chains within the ADC module — these have a higher priority over the normal conversion chain used by the housekeeping module and the interrupt handler can be optimised to find which input channel has caused the conversion. This function appends the input channels' ADC channels to the conversion chain and triggers a conversion. The function does, however, first check whether the main bus is at its maximum voltage; if it is, this signifies that demand is currently low and there is thus no need to step the algorithm. In this case a conversion is not requested, but rather a timer set to re-call this function after a set period.

`MPPTStep(PVChannel ch)` This function implements the MPPT algorithm, and is called automatically by the ADC injected chain interrupt handler upon completion of a conversion chain. The algorithm determines the step size and sets its timer appropriately.

`MPPTInitialiseChannel(PVChannel ch)` Because the series diode on the DAC's output limits the lower output voltage that provides control, this function is initially called to find the minimum setpoint that provides software control of the operating point. This is typically only ever called once but, if an anomaly is detected by the algorithm, this function could be re-called.

Payload Monitoring

The payload-monitoring module provides functionality to monitor the six payload output channels and turn the various channels on and off. Similarly to the MPPT module, each channel has both a flash-based structure and a RAM-based structure; this once again allows the monitoring functions to work with a channel index that is simply used to reference the two arrays.

Channel control software is initially designed for the capacitive coupling to the payload switches (as defined in Section 5.5.2). The results of this control is discussed in detail in a later section, and software modifications to revert to simpler control are minor.

`PAYLOADMONITORInit(void)` Sets up the various ports used to control the channels, as well as the timers assigned to each.

`PAYLOADMONITORTripChannel(PayloadChannel ch, ushort duration)` Triggers the overcurrent protection on the appropriate channel by generating a capacitive spike on the current monitor's comparator input. A duration, in milliseconds, can be set to keep the channel off. If the duration is non-zero, the channel's timer is set to restore the channel after the set time.

`PAYLOADMONITORRestoreChannel(PayloadChannel ch)` Restores a tripped channel by triggering a briefly low spike on the current monitor's reset input. If the channel is being held off, the function immediately trips the channel again. If not, it is assumed that the channel is recovering from an overcurrent condition: a timer is set to measure channel current after a brief settling period at which point the next function is called. Because overcurrent conditions are considered critical, this timer uses a CTU-triggered ADC conversion — these have the highest priority within the ADC and will interrupt any other active conversion chain.

`PAYLOADMONITORCheckPayloadRecovered(void)` This function ensures that a recently turned-on channel is not still drawing excessive current. It first finds the affected channel by scanning the ADC registers to find which channel was set for conversion, after which it determines whether the channel is still exhibiting an overcurrent condition. If it is, the action taken is dependant on how long the previous trip period was.

`PAYLOADMONITORTurnChannelOff(PayloadChannel ch)` Turns a channel off. This involves tripping the channel, as well as configuring interrupts to detect the channel turning on again.

`PAYLOADMONITORTurnChannelOn(PayloadChannel ch)` Turns a channel on. Hardware causes channels to naturally turn on, so this function simply sets flags to prevent the system keeping the channel off.

`PAYLOADMONITORCheckInterruptReason(PayloadChannel ch)` This function is called by the External Interrupt Request (EIRQ) handler and can detect whether a hardware overcurrent has occurred or not.

System Monitoring

The system monitoring module is intended to perform system-level management, including managing the ECC mechanism on each memory interface. It is also responsible for setting the last analogue watchdog channel to monitor the system current flow on the main power bus. Overcurrent conditions are first logged before triggering a bus power cycle.

Housekeeping

The periodic logging of system status information, updating of the current log of system currents and voltages, and managing of system transitions from eclipse to sunlit periods, is performed by the housekeeping module. Two different types of housekeeping logs exist, these being logs of readings (all the various current and voltage readings) and of cell status information. Each log is saved along with a timestamp from the RTC module and can be requested to be retrieved for downlink. The following are the major functions that make up this module:

`HOUSEKEEPINGInit(void)` Initialises the housekeeping tasks, including bus monitoring, enabling the relevant ADC channels, initialising cell modules, and initialising the status-logging mechanism.

`HOUSEKEEPINGConvertSystemSettingsLimits(void)` For efficiency purposes, voltage and current readings are stored as raw ADC values. System settings, however, are (initially) stored as milliamps and millivolts and thus the different current-monitoring functions need to convert either set of values for comparison purposes. This function converts the system settings limits to raw ADC values, as this need only be done once. Conversion factors are automatically calculated by macros that use resistor values and gain factors, set in the `boardconfig.h` header file.

`HOUSEKEEPINGSaveCurrentReadingsToLog(void)` Saves the current (global) set of readings to data flash, along with a timestamp.

`HOUSEKEEPINGSaveCellStatusToLog(Cell cell)` Fetches the cell status log for the given cell and saves it to data flash.

`HOUSEKEEPINGEnterEclipse(void)` Performs a set of tasks needed to optimise the system for the eclipse period.

`HOUSEKEEPINGExitEclipse(void)` Performs a set of tasks to optimise the system for the sunlit period. This function is called by the automatic `MPPTEnable` function if the `IN_ECLIPSE` system settings flag is set.

`HOUSEKEEPINGManageBus(void)` Periodically manages power flow in the bus to optimise cell charging and bus stability. This function automatically calls the `HOUSEKEEPINGEnterEclipse` function when it notices that there is no bus input current for a preset length of time.

`HOUSEKEEPINGGetReadingsLog(ushort ind, HOUSEKEEPINGReadings *log)` Fetches a readings log from flash with the given index.

`HOUSEKEEPINGGetCellStatusLog(ushort ind, HOUSEKEEPINGCellStatus *log)` Fetches a cell status log from flash with the given index.

`HOUSEKEEPINGUpdateCurrentReadings(void)` Updates the global current readings structure. This function is called automatically upon completion of ADC normal conversion chains.

`HOUSEKEEPINGConvertReadingsLog(HOUSEKEEPINGReadings *log)` Converts the current readings structure/log to millivolts and milliamps. This is used for standardisation purposes before logs are returned via external requests.

Preparation Mode

The preparation mode module contains functions for parsing and subsequently interpreting text-based commands received via the serial interface. The serial interface is only initialised when the system settings `PREP_MODE` flag is set. A further 'preparation mode key' exists in the system settings to provide a second check to ensure preparation mode is not inadvertently entered into. A specific sequence of data needs to be received by the communications interface before preparation mode is entered into. Preparation mode is exited by a similar command, although this is done via the text-based command line, running on a terminal-emulator (or similar) on a launch-site computer.

6.3 Maximum Power Point Tracking

The MPPT algorithm developed is a variation on the hill climbing method, whereby the operating point adjustment is based on the difference between the current panel power output, and that measured during the previous perturbation. The variation arises as a result of the hardware control method that makes operating on the left-hand side of the power curve exceptionally difficult, if not impossible. This phenomenon is described in the first section, after which the developed algorithm is discussed.

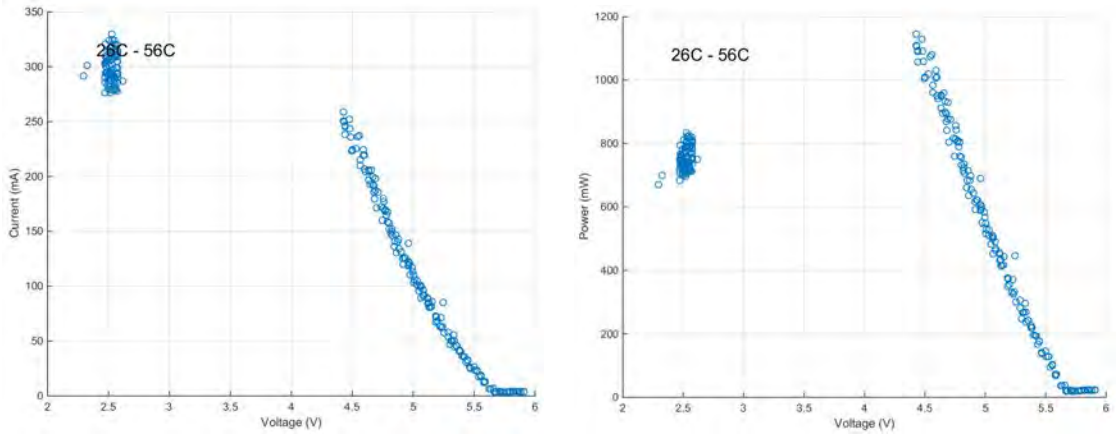
6.3.1 Hardware Characterisation

Initial characterisation of the hardware control method to adjust a panel's operating point was performed using the light box (described in Appendix C) under constant irradiance. The plots showing the results of this control over the full DAC output range are shown in the current-voltage (I-V) and power-voltage (P-V) curves in Fig. 6.1. Note the relatively large variation in temperature inherent to the test environment. This is, however, typical of the intended operating environment and thus is not considered a weakness of the testing method.

It is immediately apparent that maintaining an operating point on the left-hand side of the curve is not possible with the hardware. This is easily explained however through the theory presented previously, and was specifically referred to in Section 2.3.6: The typical shape of an I-V curve (seen in Fig. 2.5) shows a relatively constant current output once the MPP has been crossed (moving from right to left) — as the converter tries to draw more input current, input voltage drops steeply and falls below its drop-out voltage. The regulator is then held in a form of equilibrium until it is either turned off or the setpoint significantly reduced.

6.3.2 Algorithm Overview

It was previously argued that 'static' methods of control, such a Constant Voltage and Constant Current, are not suitable to the very-limited availability of power. An Incremental Conductance (IncCond) algorithm is also impractical, seeing that



(a) (b)

Figure 6.1: Characterisation of operating point control showing different DAC set-points on (a) an I-V curve and (b) a P-V curve.

it relies on smooth control of the operating-point to determine certain voltage-current derivatives. With inherent noise in sensor readings and a limited 10-bit ADC[4], the ratio of two time-based sensor reading derivatives ($\Delta i/\Delta v$) will produce an unreliable result: although time-based derivatives have time being a well-defined and stable parameter, having two within the same factor will likely produce large fluctuations. Furthermore, IncCond algorithms have as fundamental their ability to predict the direction to the MPP; it is clear that reliable operation to the left of the MPP is not possible.

That being said, similar limitations are found in a hill climbing method in that 'there is a cliff at the top of the hill'. For this reason, the base hill-climbing algorithm is adapted to first find, and later dynamically predict, the MPP in an attempt not to cross it. Although the approach has limitations in quickly 'moving' this point if irradiance levels suddenly increase, this shortfall is addressed by the algorithm.

Avoidance of the 'equilibrium' state is guaranteed by an analogue watchdog on each input channel — if this voltage drop is detected, the regulator is immediately switched off. The subsequent increase in voltage causes the same watchdog to re-initiate the algorithm.

[4]Some improvement could be found in significant time-averaging of sensor readings; however, this impacts the ability to maintain optimal control in rapidly-changing environmental conditions.

6.3.3 Algorithm Inputs

The following inputs and dynamically-calculated parameters are used by the algorithm:

Input Voltage and Current Performed during an ADC injected-chain conversion and retrieved during each algorithm step. For efficiency, raw ADC values are used by the algorithm. Sudden and significant increases in input voltage are used to flag an increase in irradiance.

Input Power and ΔP Simply the product of input voltage and current, but divided down to reduce the size of the variable needed. The factor is kept at 16 to allow an efficient bit shift perform the division and to allow the product of the two 10-bit numbers be stored in a short integer. The change in input power, ΔP, is calculated with each algorithm step.

Maximum Power Indicative of the maximum input power found. It is, however, dynamically lowered to account for increasing panel temperature and changes in irradiance. This maximum predicted power is used, in conjunction with the current input power, to predict the proximity to the maximum setpoint and thus how far to step the operating point. The calculated proximity is further used to set the variable step size; the algorithm operates quickly when it predicts that it is far from the MPP and reduces the step size when it is near. If a sudden increase in irradiance is detected, this is reset in order to rapidly find the new maximum.

Setpoints A minimum, current and maximum setpoint is stored: the minimum setpoint reflects the lowest DAC output that provides control of the operating point, and the maximum setpoint is a dynamically-adjusted variable that limits the current setpoint. This maximum is lowered when the regulator shuts off from attempting a too-high a setpoint and increased when a set number of periods have successfully been spent at the estimated MPP.

Further Flags and Variables Two flags — `direction` and `change_detected` — are used to determine a positive or negative step in the setpoint. A decrease in input power implies direction should be changed, but this is only effected once the decrease is seen on a consecutive step of the algorithm. A number of other variables are used to avoid oscillations when control cannot be maintained; in these cases, the regulator is left to operate at the hardware-defined default setpoint. Control is re-attempted after a dynamically-determined length of time. Variables and flags also exist to determine whether the moving average filter has had sufficient time to settle, thus producing a valid output.

Moving Average Algorithm

To improve algorithm performance in the context of relatively low sensor resolution combined with small changes in measured parameters, a modest moving average filter is applied to voltage and current readings. A similar filter is used to slowly lower the maximum-predicted input power when the operating point is near or at the MPP, but output power is lower than the current maximum.

The computationally-efficient algorithm used is

$$MA_n = MA_{n-1} + \frac{x}{m} - \frac{MA_{n-1}}{m} \tag{6.1}$$

where n is the MPPT step, m the number of data points and MA the current moving average of the input x. By keeping m a power of two, an efficient bit-shift operation can be used to perform the division.

Future work may want to investigate possible performance gains using a weighted-average approach, although at the cost of computational efficiency.

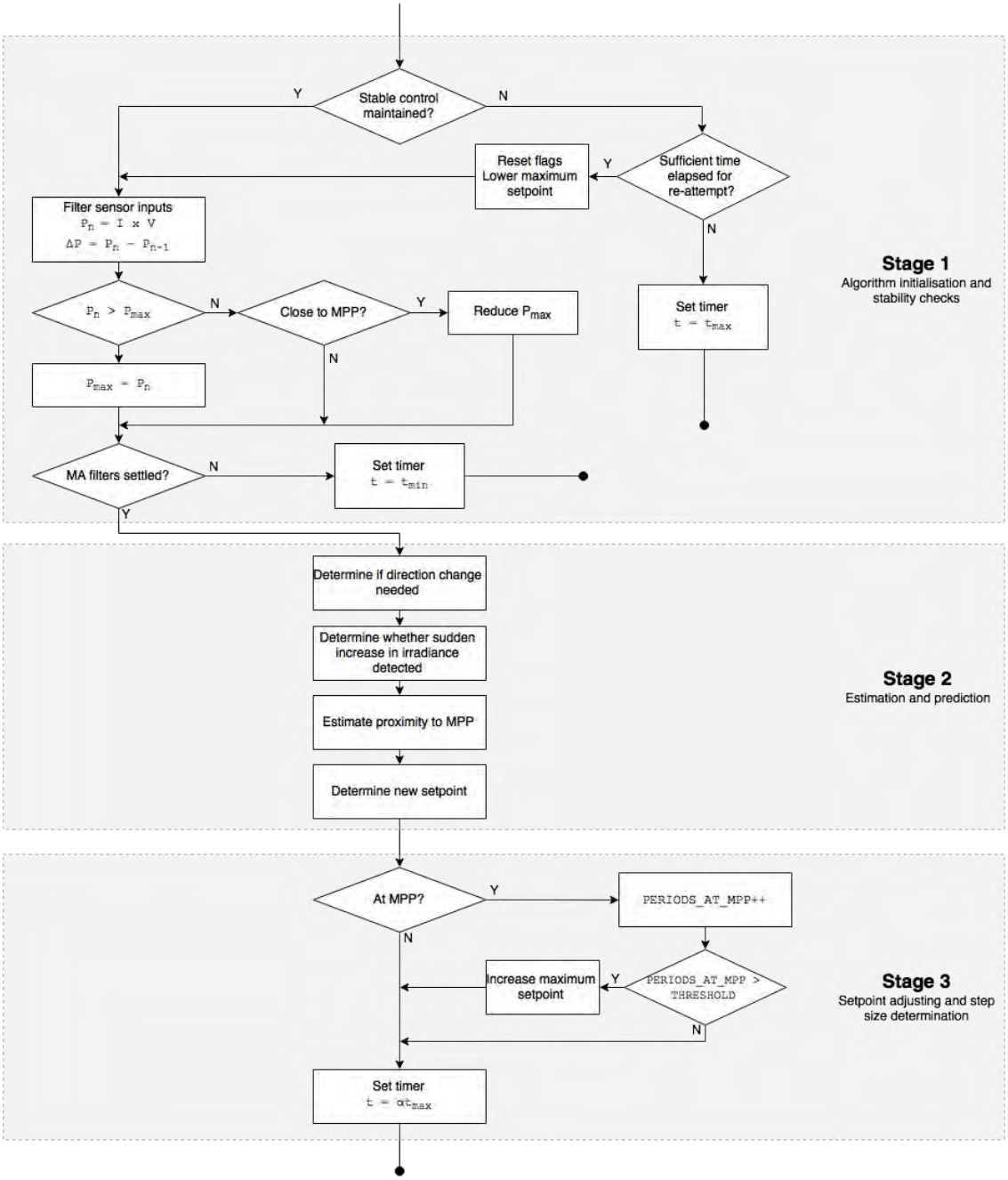


Figure 6.2: Depiction of the MPPT algorithm. Note that the blocks in stage two implement a number of checks that are described further in the text.

6.3.4 Algorithm Design

The MPPT algorithm is initiated with a crossing of the voltage threshold, and each step ends, or is aborted, with a timer set to initiate the next step; a crossing of the lower voltage threshold is the only input that can break the autonomy. As seen in Fig. 6.2, the step has been divided into three stages to simplify explanations:

Stage One

In stage one, an initial check is done to limit the number of control attempts over a short period of time — with each start of the algorithm, the number of attempts is incremented; after a certain number of valid control steps, this counter is reset. When control cannot be sustained, the regulator is configured to operate at the hardware-defined minimum operating point. A re-attempt is made after a preset time, and the maximum setpoint is reduced in a bid to prevent a recurrence.

The moving average filter is applied to the voltage and current inputs, and input power is calculated. Maximum power is updated if this value exceeds the previous; if not, the maximum power is adjusted down if the panels are thought to be operating near their MPP — this accounts for the increase in temperature, and thus reduction in output power, over the orbit's sunlit period. This proximity to the MPP is determined by the current setpoint being near to the maximum, as determined by previous algorithm steps.

If the filters have not yet settled, the step is aborted. This settling process happens rapidly however during the initialisation process in which the minimum setpoint is determined.

Stage Two

Various predictions and estimations are made in stage two using a number of parameters, available for adjustment in the `mppt.h` header file. The first decision is determining whether a change of direction is needed, depending on the sign of ΔP. The first negative change in power is rather flagged however, with a second consecutive decrease effecting the change.

A sudden increase in measured input voltage is used to predict a sudden increase in irradiance, and results in the maximum power being reset; this forces the algorithm to quickly re-scan the power curve to find the new maximum.

The proximity to the MPP is then estimated using the relationship between the current setpoint and maximum setpoint, as well as the current input power in relation to the maximum estimated input power. If one or more necessary inputs are unavailable (indeterminable or uninitialised), some assumptions are made to optimise performance in the majority of such cases.

Stage Three

Stage three performs some final adjustments to the maximum setpoint, depending on how many steps have been spent at the MPP. This ensures that the algorithm continuously but cautiously searches for more available power. The algorithm step ends with the setting of a new step size, dependant on the previously-estimated proximity.

Overall design and interaction between stages has ensured that, once the system has sufficient knowledge of the power curve, the MPP can be rapidly re-found. As the algorithm settles, step sizes increase proportionally which reduces the necessary computational input, as well as reducing the risk of losing control.

6.3.5 Performance

Although a number of parameters are needed to 'tune' the algorithm, these are not considered limiting as they do not assume a specific panel configuration. Fast and stable performance has been found, and further results are documented in a later section.

6.4 Payload Monitoring

The payload monitoring system serves to monitor the six output channels (of which the EPS is one) and trigger a recovery process if an overcurrent condition is detected. Although overcurrent conditions are logged by the system, it is left to the housekeeping module to periodically store current readings of the six outputs.

6.4.1 Channel Settings

The system settings structure allows for individual settings per channel, with these settings outlined in Table 6.1. As previously described, these settings can be configured during flight preparation and it is anticipated that the EPS's command system will allow for in-flight adjustment of these settings; such functionality is currently absent from the software.

6.4.2 Watchdog Functionality

Each channel can enable a watchdog feature that sees the respective output power-cycled, should it not receive communications from the payload within the set time-out period. This functionality is implemented using the real time clock module given the relatively long time periods.

Table 6.1: Payload channel settings available within the system settings.

Setting	Values	Units	Description
`ENABLED`	0–1	T/F	Whether the channel is enabled (ie. in use by the satellite). Separate to the channel being on/off.
`WARNING_ENABLED`	0–1	T/F	Whether current warnings should be issued.
`WATCHDOG_ENABLED`	0–1	T/F	Whether the watchdog functionality should be enabled.
`CURRENT_LIMIT`	0–4095	mA	Current that will trigger a channel power cycle.
`WARNING_THRESHOLD`	0–4095	mA	Current that will trigger a warning, if enabled.
`WATCHDOG_TIMEOUT`	0–31	s	Time within which a message from the payload needs to be received to prevent a power cycle.

6.4.3 Overcurrent Handling

Overcurrent monitoring and the subsequent recovery process for violating channels is done autonomously with a few 'fail safe' checks to ensure an interrupted sequence (in the sense of a software anomaly) is swiftly corrected. The frequency at which checks are performed is set by a compiler constant in the `payload_monitoring.h` header file. Although absent from the current software revision, a future version should include intelligent variation of this rate.

The flow structure of the overcurrent checks, as well as the various different entry points into the structure, is shown in Fig. 6.3. The periodic overcurrent-checking process is initiated during the module's initialisation function, after which it recursively re-calls itself. Actual sampling of the channel current is achieved using the ADC's normal conversion chain, as this forms the lowest priority and can be automatically paused by time-critical conversion requests.

Upon entry into the monitoring process, a fail safe mechanism is implemented to ensure an 'off' channel is indeed off — if not, it enforces the usual turning-off sequence. An overcurrent condition initiates the 'payload recovery' process whereby the channel is power cycled for a short initial period. Counters that keep track of this period are initialised to allow subsequent resets be extended.

The channel trip function performs the requested trip and can set a timer to enable premature resetting of a tripped channel. Some additional logic, not shown in Fig. 6.3, allows power cycle durations longer than the hardware-defined maximum, by re-tripping the channel should it still be requested to be off. A duration value of zero is used to indicate the channel should be left to an automatic hardware reset.

The channel restoration function resets the respective channel before determining whether the channel should remain off; this functionality is used to implement power cycles longer than the hardware maximum. If not, a timer is set to cause a CTU-triggered ADC conversion (highest priority within the module) after a short time that allows the channel to settle.

Once this conversion has completed, the channel is tested for a further overcurrent condition; if the condition still exists, the recovery process if repeated until such time that the maximum cycle time has been exceeded.

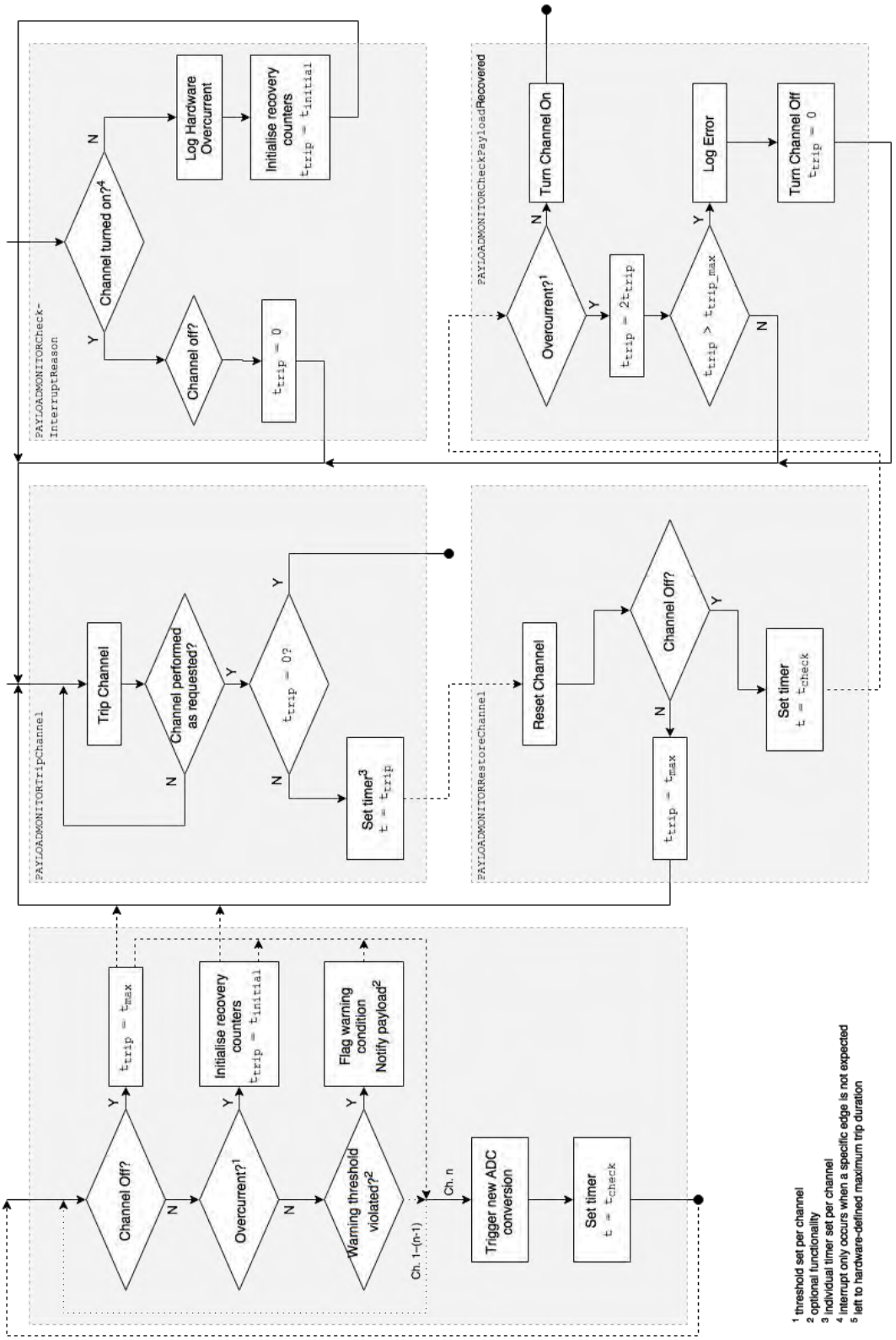


Figure 6.3: Depiction of the payload monitoring system. For simplicity, dotted lines indicate loop structures, and dashed lines indicate timed sequences and/or asynchronous sequences.

The on/off status of each channel is further monitored by an external interrupt pin that is used to detect unexpected transitions. This can be used to keep a channel turned off (the channel turned on when it was supposed to have been off) or detect a hardware-enforced overcurrent power cycle (the channel turned off when it was supposed to have been on).

6.5 System Monitoring

The system monitoring module acts in a more global role, that includes monitoring the system input current for overcurrent conditions and performing ECC-related tasks.

6.5.1 Bus Current Monitoring

The analogue input channel for the system current sensor is linked to another analogue watchdog channel, that triggers a bus power cycle when a set threshold is crossed. This limit can be dynamically adjusted: during periods of critical power, it can be lowered to below the lowest channel current limit, meaning that individual channel monitoring can be eased until bus current increases.

Before the bus is power cycled, a system error is logged: error logs are scanned upon reset and a previous bus power cycle can initiate a 'safe' mode whereby the cause of said power cycle can be determined.

6.5.2 ECC Management

ECC-related error handlers are also contained in the module, consisting of functions that correct single-bit errors and manage non-correctable double-bit errors. All errors are saved in the error log, and single-bit RAM errors are corrected in the application background. RAM non-correctable errors result in a forced reset, but non-correctable program-flash errors result in the device entering standby mode. Periodic reading of RAM locations is performed which automatically triggers the ECC handlers.

6.6 Housekeeping

The housekeeping module is responsible for maintaining the system-wide structure of current and voltage readings and providing facilities for converting between raw ADC values and the scaled mV/mA equivalents.

Functionality is also provided to store and retrieve housekeeping logs from data flash and preparing them for transmission to an external device. Logs are saved periodically as well as upon ad hoc requests.

Power flow on the main bus is also managed in an effort to improve system performance, efficiency and stability. Cell charge rates are varied to account for differences in their states of charge as well as available input power. Cells are never allowed to charge each other to maximise efficiency and their cycle life. The amount of power flow into the bus is also used to determine when an eclipse period has been entered into.

Upon eclipse detection, functionality is provided to transition the system into a low(er)-power mode. A similar process is performed when the MPPT module triggers the start of a sunlit period when power generation resumes; bus control is not needed during eclipse seeing that power flow can only be out of the cells.

A number of other miscellaneous functions are provided for other modules to determine system power levels.

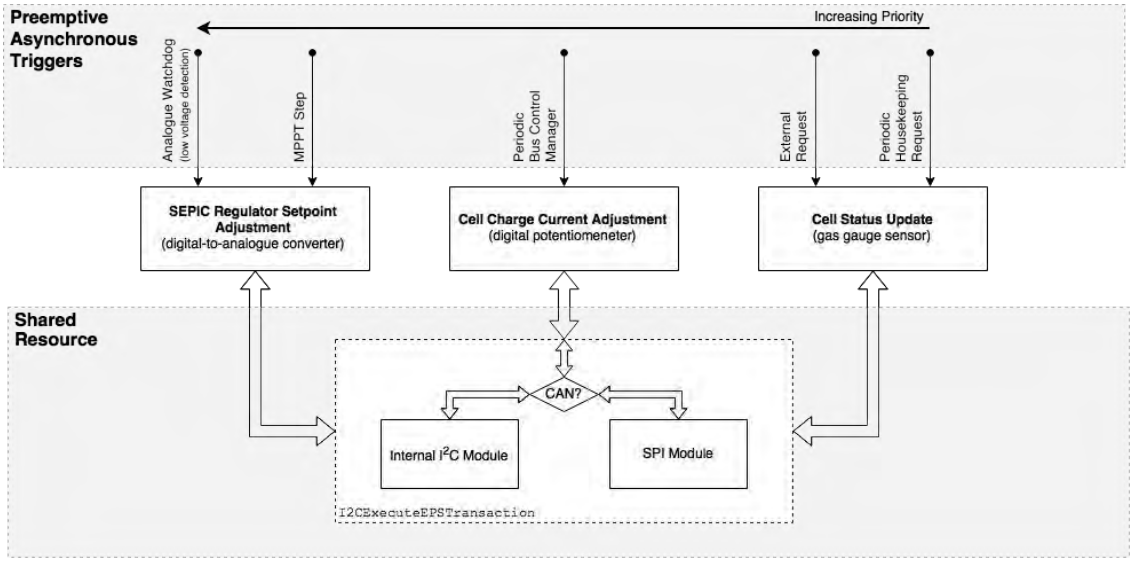


Figure 6.4: Sources and priorities of triggers to the I^{2}C module.

6.7 Pre-emption and Priority Management

As described in the introduction to this chapter, the microcontroller features a preemptive interrupt controller with assignable-priorities for each of its 142 interrupt requests. This means that unless proper management of interrupt priority is done, concurrency issues could lead to system reliability issues. The following sections briefly describe preventative measures taken to ensure reliability with the two most-commonly shared resources: the ADC module and the I^{2}C module.

6.7.1 I^{2}C Module

The I^{2}C module is used to control the SEPIC regultors' setpoints, cell charge rates and retrieve data from the cells' gas gauge sensors. Each of these functions have asynchronous triggers, that come predominantly from the Timer module, in which multiple interrupt requests are used for different timer channels, each with (potentially) differing priorities. Fig. 6.4 depicts these triggers and their associated priorities, as defined by the application.

It was mentioned that both internal and external interface drivers are synchronous, waiting until the bus transaction has completed before releasing the module and returning the transaction data to the calling function. To ensure the I^{2}C driver

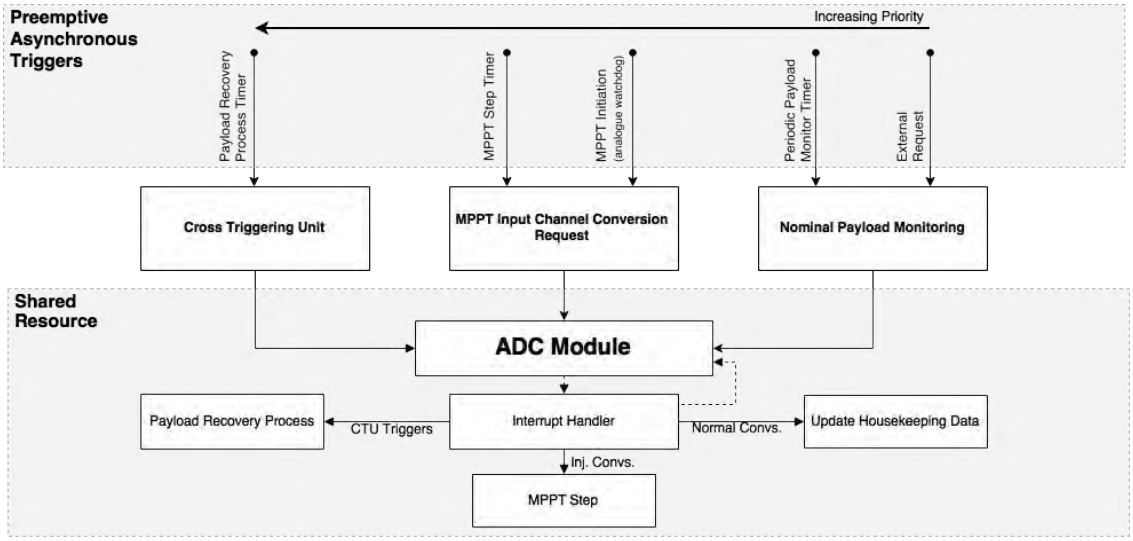


Figure 6.5: Sources and priorities of triggers to the ADC module.

cannot be called while in use, it makes use of the interrupt controller module's ability to temporarily raise the interrupt ceiling: this ensures that the transaction cannot be interrupted until it completes. While not the most efficient approach, it ensures reliability so long that software timeouts are built into the driver.

6.7.2 ADC Module

Although simultaneous ADC triggers are handled within the module and thus pre-emption cannot affect the reliability of the application, Fig. 6.5 shows the priority structure and functionality of the shared ADC module. CTU-triggered conversions have the ability to abort injected chain conversions, and thus it is important to re-trigger such conversions within the handler if necessary.

The global housekeeping data is updated whenever new data is available and thus, because these updates happen asynchronously, flags are used to indicate to modules whether or not valid data is available.

Chapter 7

Results & Analysis

This chapter focuses on the results of four main aspects of the system: its power capabilities, the efficiencies of the different subsystems, the functionality of said subsystems and the performance of the maximum power point tracking (MPPT) algorithm.

Initial work consisted of developing sufficient software to test the full functionality of each subsystem; these were found to function as designed and all concepts were proven. A few minor shortcomings were however evident, and are noted in their respective sections within these results. These shortcomings are predominantly related to physical layout and can be remedied in a future hardware revision. It was not found necessary to realise this revision during the course of this work as further testing and development should first be done; this is discussed within this work's recommendations.

7.1 Maximum Power Point Tracking

The MPPT algorithm, discussed in Section 6.3, was tested in an artificial environment to have better control over test parameters and to ensure uniformity amongst test results. This environment is discussed further in Appendix C which includes characterisation of the panels used for testing.

7.1.1 Test Setup

Testing was performed using the EPS hardware that was developed, with the algorithm running on the target microcontroller. The data points in the plots that follow are representative of actual algorithm variables, whose values are transmitted via serial link, in real-time, with each step of the algorithm. *Available power* is calculated for each set of data points in post-processing; this takes into account irradiance and panel temperature, and is an estimation that is described in Appendix C.

The MPPT efficiency is calculated based on the ratio between the input power and the (estimated) available power. It is thought that this gives a fairly accurate estimation of MPPT performance that can be used as a reliable metric to compare variations of the algorithm.

It was ensured that there was sufficient system load to make use of the full input power and that all tests begun at similar panel temperature. The inherent and fast temperature rise is accounted for within the available power calculation, although this rise is faster than could be expected in the end application.

7.1.2 Performance

The following plots show the algorithm's performance under different irradiance conditions.

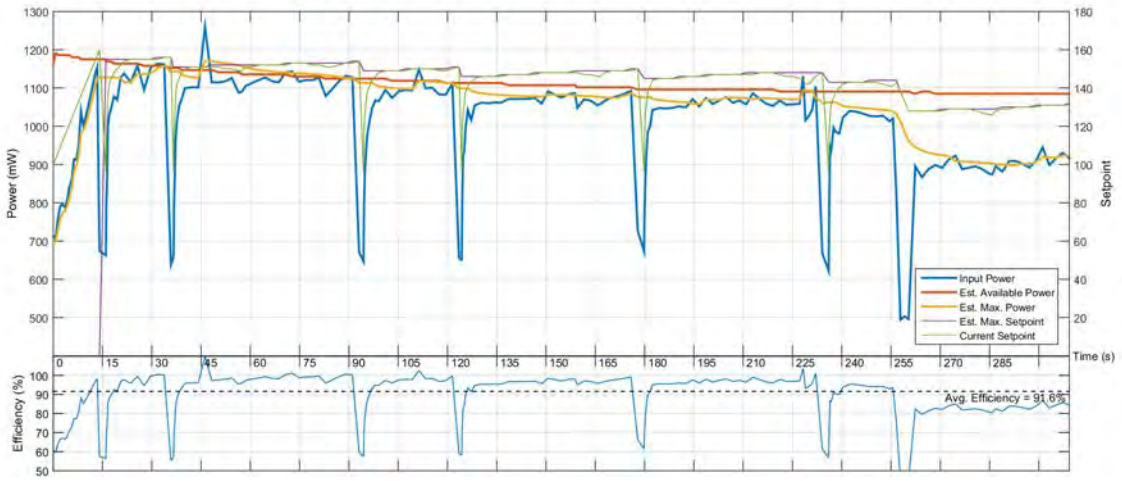


Figure 7.1: MPPT algorithm performance plot for a fixed irradiance.

Constant Irradiance

Fig. 7.1 shows algorithm performance under a five-minute constant-irradiance test. For the period up to $t = 15$ s, the algorithm initialises itself: the setpoint is increased at a moderate rate while maximum estimated power is simultaneously updated with each increase in input power. Once the operating point passes the MPP, input power falls dramatically; the algorithm responds by initialising the maximum setpoint to avoid crossing this operating point during the next curve traversal. The operating point is then initially brought up rapidly, before tapering off as this maximum approaches.

The decrease in available power (owing to the increase in temperature) means that the MPP is again crossed, but the operating point is once more quickly restored. A few more such crossings occur as temperature increases further. Note that this increase, as mentioned, is faster than the environment would exhibit and it is thus expected that performance would be more stable under true constant irradiance and temperature.

Around $t = 260$ s, the maximum setpoint is lowered to account for an initial decrease in input power, but is lowered on further consecutive steps when low input power continues to be seen. The raw data indicates a brief loss of DAC setpoint control, the reason for which is unclear and needs to be further investigated. Although this is unintended operation, the data does show the algorithm to remain stable and to slowly increase the maximum setpoint as it returns to the MPP.

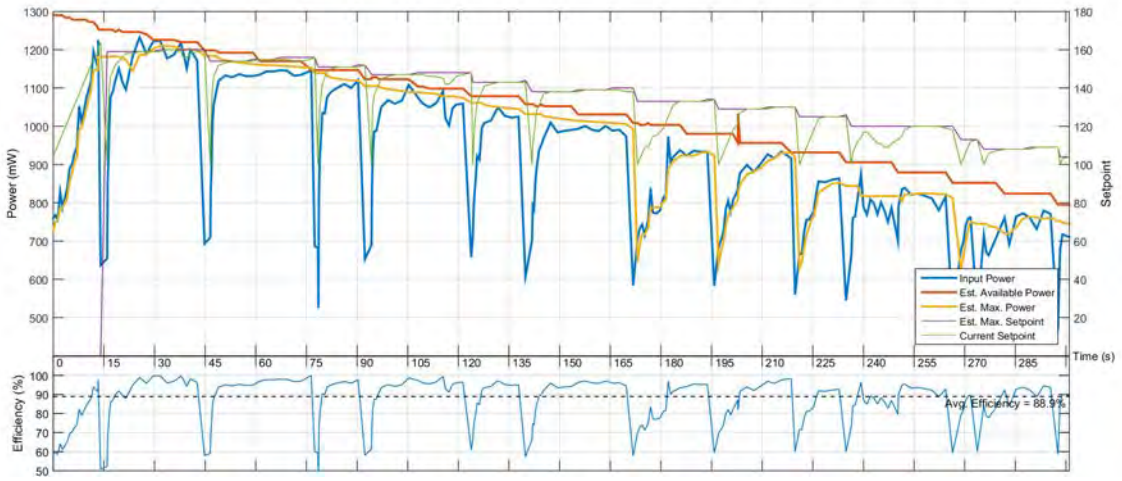


Figure 7.2: MPPT algorithm performance plot for periodic step decreases in irradiance.

An overall efficiency of 92% for the period is estimated, with the period after $t = 260$ s contributing to a substantial lowering of this average.

Decreasing Irradiance

Periodic step decreases in irradiance were tested and the performance result is shown in Fig. 7.2. Control stabilises within approximately 20 s, after which the estimated maximum power is able to accurately follow the actual available power until $t = 170$ s. At this point, the estimated maximum power is reset with each substantial drop in input power. This slows the algorithm's ability to re-find the MPP. It is likely that some adjustment to algorithm parameters could avoid this.

Nevertheless, an overall efficiency of 89% is obtained and performance remains stable. The maximum setpoint, which limits the current setpoint when maximum estimated power is undefined (it has the same value[1] as the current input power), remains well-defined and is appropriately reduced with each loss in input power.

[1]Maximum estimated power is based on the filtered moving-average input power, whereas these plots show instantaneous input power.

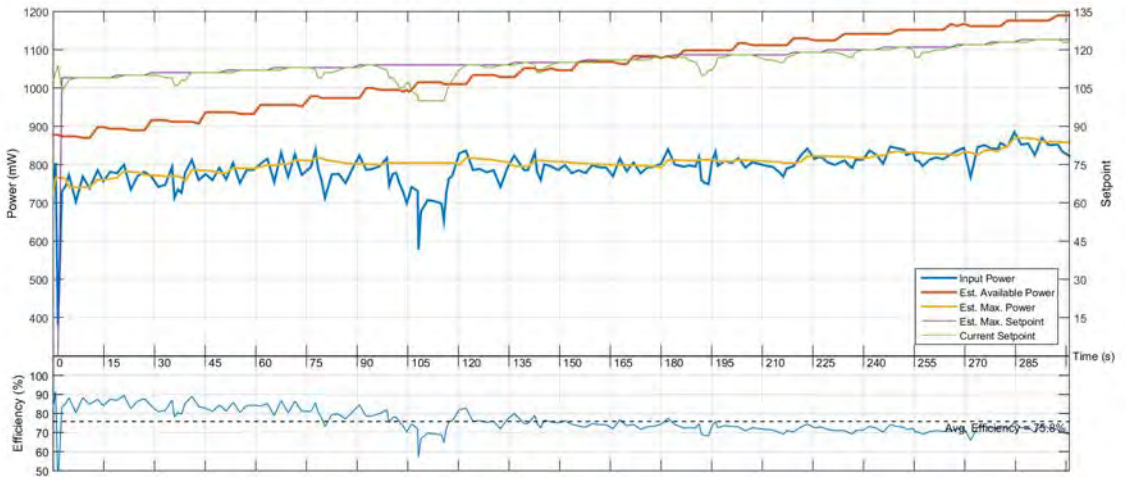


Figure 7.3: MPPT algorithm performance plot for periodic step increases in irradiance.

Increasing Irradiance

Fig. 7.3 shows periodic step increases in irradiance. The algorithm is slow to adjust to such increases in available power, and substantial efficiency is correspondingly lost. This difficultly arises from the (intended) conservative search for more power once an initial setpoint is found: it can be seen that the maximum estimated setpoint, once established, steadily rises, but at a rate lower than the increase in available power.

It is expected that the rate of increase used in this test is faster than could be expected under nominal conditions in the end application. Such a rate is used, however, to show the current limitations of the algorithm.

The average 76% efficiency is poor; however, it is also likely that further adjustment to algorithm parameters could increase this. For example, the successful consecutive increases in setpoint could trigger a new search for the MPP: this would quickly regain the true MPP. Such an approach would have relatively large time constants which would in turn limit its usefulness for fast-changing irradiance levels.

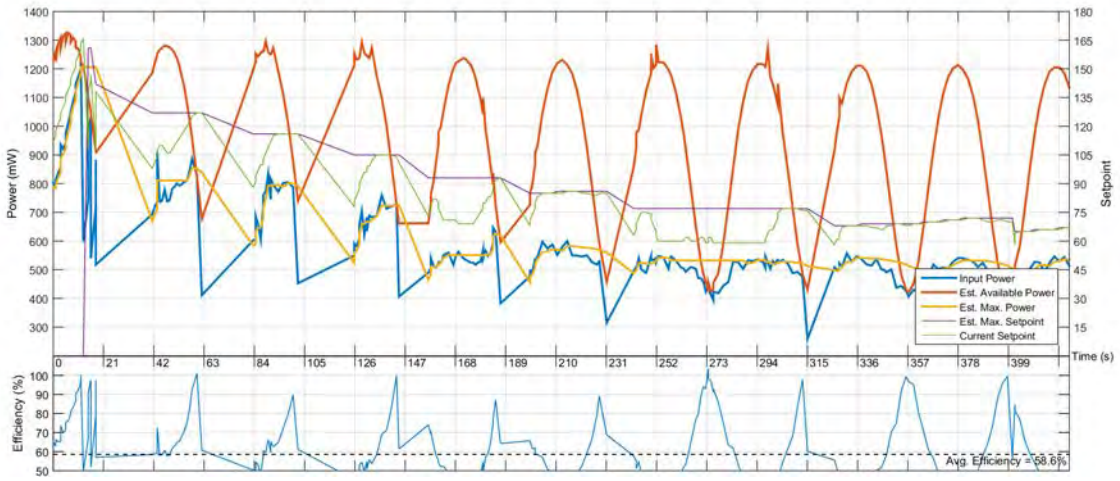


Figure 7.4: MPPT algorithm performance plot for a spinning satellite.

Spinning Satellite

The final test is one in which a spinning satellite is simulated by exposing the panels to sinusoidally-varying irradiance levels. A period of 42 s corresponds to a yaw/pitch/roll of 0.15 rad/s, characteristic of the initial tumbling phase a satellite may experience after deployment.

The algorithm is unable to track the MPP at this rate and an efficiency of 59% is achieved. Although these are not expected to be nominal conditions, it is desired to improve performance to account for spin-stabilised satellites[2] as well as to improve overall algorithm robustness.

It is once again likely that certain modifications and improvements to the algorithm could allow it to better track such variations. MPPT algorithms can achieve significant tracking speeds[3] and active control should be capable of tracking the conditions seen in this test. Indeed, the initial stabilisation period shows the ability to rapidly move along the curve.

Allowance for shorter step sizes and better characterisation of hardware performance are thought to be the predominant aspects for improvement.

[2]Spin-stabilised satellites maintain a slow rotation around their principle axis to achieve single-axis stability through the inherent gyroscopic stiffness of fixed body.

[3]See eg. [27], although this uses fuzzy-based control which was previously argued against.

7.1.3 Discussion

The difficultly in operating on the left-hand side of the P-V curve makes control non-trivial and the cautious approach needed to avoid oscillations and instability slows performance. Although this was shown to only have consequences for increasing and sinusoidal (or fast-changing) irradiance levels, these are scenarios where high efficiency is needed: As the satellite enters the sunlit period of its orbit, irradiance will likely exhibit similar rates of increase. Furthermore, if periods of spinning are encountered, the relatively power-hungry Attitude Determination and Control System may have appreciable power requirements.

It is clear nevertheless that control remains stable in all cases and that the structure of the algorithm is suited to the available hardware. Furthermore, the regulated 3.3 V and 5 V buses remained stable throughout these tests, indicating stability of the battery bus and seamless transitions between battery charging and discharging.

It was expected, and indeed observed, that the large variation in panel temperature, inherent to the test environment and characteristic of the intended operating environment, causes great variation in the position of the MPP: passive tracking methods, such as Constant Voltage or Constant Current, would thus achieve far inferior efficiencies to even those observed in the cases of increasing and sinusoidally-fluctuating irradiance levels.

The default operating point of the converters, discussed during hardware design, was proven to function as designed and remain stable.

7.1.4 Algorithm Constants and Potential Improvements

The algorithm makes use of a number of fixed constants and logic-based decisions for determining various estimations. These are briefly discussed in relation to the effect they were observed to have; they are considered likely areas for future development that have the potential to significantly improve performance.

Detecting Increases in Irradiance

Sudden increases in irradiance are important to detect as this inherently signifies additional power being available. In different hardware implementations, the ability to move the operating point around the curve means that the system can more easily detect the direction to the MPP and not be limited to maintaining an operating point on the right-hand side of the power curve.

Currently, the software tests for a minimum positive increase in both instantaneous panel voltage and power. Although this was seen to be effective for large and sudden increases, smaller increases go unnoticed. Furthermore, this test results in false positives for a number of insignificant input conditions. It was not investigated in detail, but it appears there may be a more complex relationship between the input and dynamic parameters that could reliably predict such increases.

Detecting Drops in Irradiance

Sudden decreases in irradiance are simpler to detect than increases in that typically, if the drop is significant enough, the constant-current control results in an immediate drop in input voltage. Section C.2 reasons that the MPP is likely to coincide with the greatest regulator setpoint and thus, if the regulator is operating, a decrease in irradiance is unlikely to reduce the MPPT efficiency. This drop is very quickly detected and a lower operating point can be rapidly reinstated.

Nevertheless, these drops could be better characterised in order to improve the system's response to such events.

Searching for Available Power

To ensure that the slow increases in available power do not go unnoticed, further liberty needs to be given to the algorithm to increase the maximum setpoint: this maximum setpoint is one of the parameters that limit input power to prevent instability. An improved set of logic and memory flags could be used to better control this setpoint.

7.1.5 Software Implementation

The MPPT software module has been written in such a way that it can operate independently on each of the three input channels. Each channel is further monitored by a robust analogue watchdog that reliably initiates and ends tracking operation. This is further used by the housekeeping module to appropriately begin and end its eclipse-entering and -exiting programmes.

The built-in safety measure, that ensures instability does not occur, was found to successfully end control after a set number of short-lived control attempts. Control is re-attempted after a further set period of time with the regulator operating reliably at its hardware-set default operating point in the interim period. Such measures appear necessary when available power drops particularly low, and the required setpoint is close to, or at, the minimum setpoint (that provides software control).

7.1.6 Testing Platform

A set of software tools have been developed to allow improvement of the algorithm. The plots seen in the previous sections can be automatically and immediately generated after a test period, and thus the results of modifications quickly and easily observed. Integration with the testing environment means that panel temperatures can be recorded alongside algorithm steps, as well as allowing automatic simulation of different irradiance scenarios.

7.2 Performance and Efficiencies

The following section discusses the efficiencies and performance results of power flow within the main power bus, as well as the power requirements of the EPS. Various other EPS subsystems are also discussed with respect to their performance.

7.2.1 Power Bus

The different states of power requirements are depicted in Fig. 7.5 which further indicates where power flow is measured. The so-called 'battery efficiency' that will be referred to is representative of the power flow measured by the gas gauge sensors in relation to the net bus power: During discharge, this is the ratio of power leaving the two cells to the power entering the system, and is depicted by the blue arrow. If sufficient solar power is available to meet system requirements (with corresponding power flow indicated by green arrows), this efficiency is representative of the battery charge regulators' losses. Red arrows indicate a further case whereby the batteries are used to supplement input power.

Input stage efficiency refers to the difference in combined solar input power to the bus input power. This is representative of the efficiency of the SEPIC regulators.

In the following results, negative cell power indicates discharging and positive cell power indicates charging. Cell 1 was charged to a marginally higher terminal voltage than that of the second cell, resulting in increased current output during discharge. The second cell also had charging disabled while the first was set for maximum charge rate. Test data was obtained in real-time using the EPS hardware and software systems.

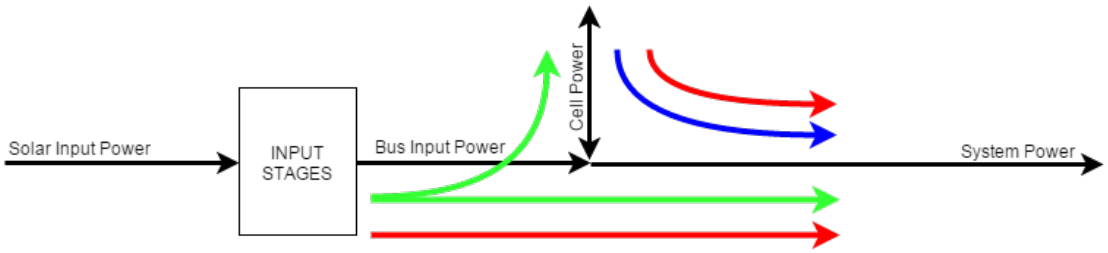


Figure 7.5: Bus power flow cases.

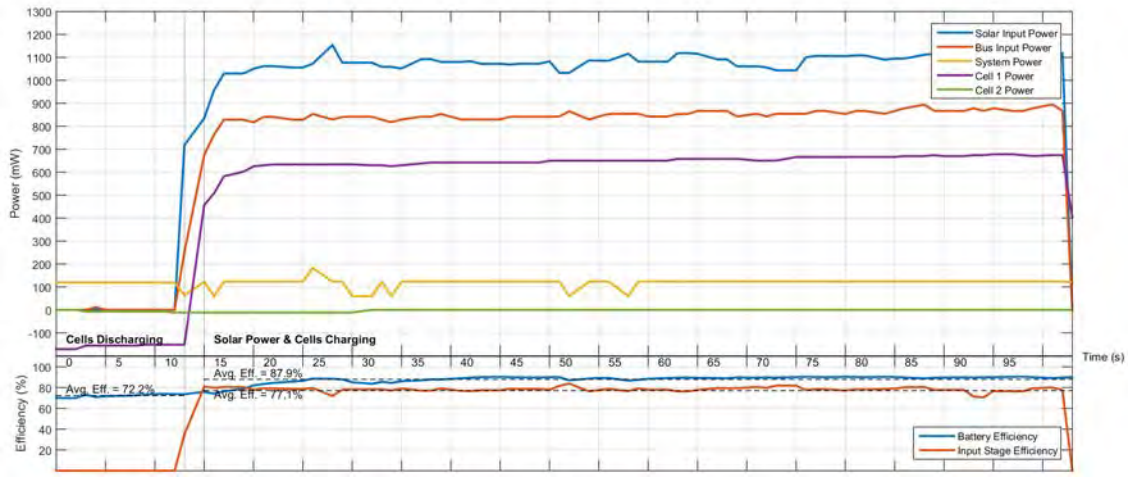


Figure 7.6: Power flow through the different bus branches showing input and cell charging efficiencies.

Low System Load

Fig. 7.6 shows the different power levels measured by the system with the EPS the only downstream load on the system.

The low battery discharge efficiency seen in the first stage can be attributed to low bus sensor resolution at low currents, as well as further calibration that is needed by the gas gauge sensors; during discharge, current has a low-loss path through the ideal diode directly onto the bus. Although it was mentioned that reverse current through the input-stage Schottky diodes may present losses, this was tested to account for $\ll 1$ mA of leakage.

Solar input power is introduced at $t = 12$ s, at which point a brief transition period takes place where the cells continue to contribute power to the bus. Once input power increases beyond system requirements, cell 1 is able to begin charging. This charging is shown to attain an efficiency approaching 90%. A different choice of inductor may be able to provide a slight efficiency gain.

During this stage, an input efficiency of just under 80% is achieved. This is as expected and is a figure that was consistently observed.

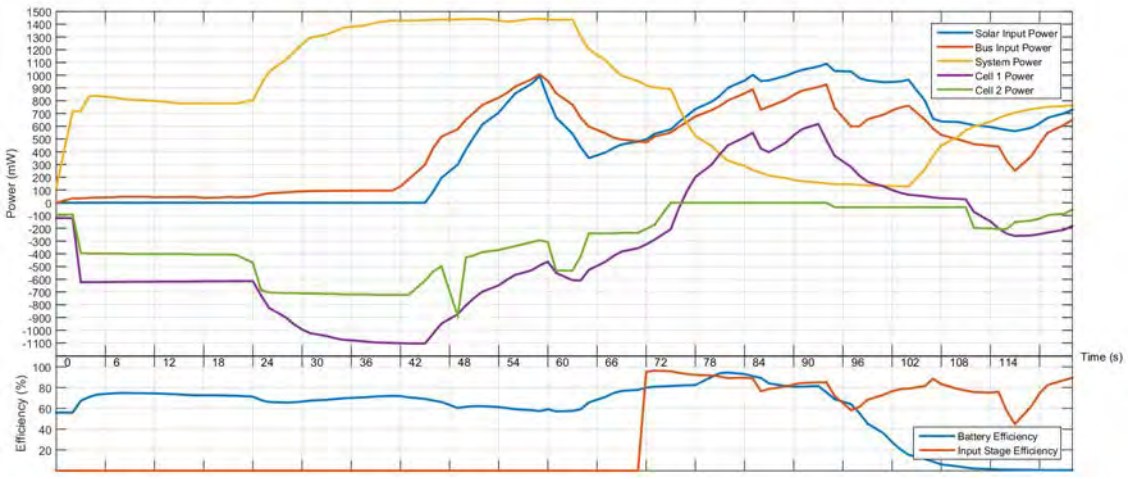


Figure 7.7: Power flow through the different bus branches for varying load cases.

Varying System Load

Fig. 7.7 shows the same set of system parameters but for a varying system load. As will be explained, this data does not show useful efficiency estimations but rather an issue with physical PCB layout:

A system load of 800 mW is initially introduced with an absence of solar input power. It is immediately observed that bus input power is indicated when this is indeed not possible: bus input power should never be expected to exceed 80% of input power. This phenomenon is attributed to parasitic PCB trace resistance between the ADC ground and the ground used by the current sensor[4]: as system current increases, the resulting voltage drop over the ground plane, that the returning current effects, causes the sensor to use a higher reference voltage to that of the ADC. Indeed, the data appears to become more accurate once system load is later decreased.

The data does however show that relatively smooth, and indeed stable, transitions between different power flow cases (as per Fig. 7.5) are achieved. Note that the low efficiencies that are suggested, in particular towards the end of the capture period, are not representative of actual performance due to the aforementioned sensing errors.

[4]The different current paths through the ground plane make it difficult to verify and/or quantify this resistance, but it is calculated that an effective 50 mΩ would produce the discrepancy seen. This is thought to be feasible given the multiple interrupts to the ground plane needed to keep layer count to two.

7.2.2 EPS Efficiency

The EPS itself was characterised in terms of its power consumption: it was found that during microcontroller *run mode*, with all peripherals and external devices out of standby mode, the system consumes 130 mW. This is a significant amount of power but is the maximum power the system could draw (neglecting brief and irregular flash write and erase operations).

However, in microcontroller *standby mode*, total system consumption is reduced to 24 mW. The biggest single user of this power is the CAN transceiver that draws an average of 6 mA when active[5]. A design decision to not make use of the transceiver's standby functionality was made for two reasons: Firstly, if CAN is *not* used on the module, the device can be left unpopulated. Secondly, if CAN *is* used on the module, the device should always be listening on the bus. An exception to this is during periods of critical power when all output channels may in fact be turned off; this is considered an oversight and standby functionality can be easily added in the next hardware revision, with the addition of a single control line.

It is expected that once refined overall software design is complete and time-based interrupts are used to trigger EPS tasks that bring the device out of standby mode, the system could achieve an average consumption below 50 mW.

Furthermore, the current 32 MHz system clock could likely be halved to 16 MHz, given the relatively low processor load, or at least be dynamically adjusted depending on system requirements, with clock-based timer functions adjusted accordingly. The datasheet suggests a 30 mW power saving at this lower system clock which would substantially improve efficiency. In addition, the (less temperature-stable) internal fast RC oscillator could be switched to that lowers consumption even further.

[5]The device is not transmitting or receiving, but is functioning as an active node on the bus.

7.2.3 Regulators

The buck and boost converters were found to perform to their stated efficiencies of approximately 95%. However, while the buck regulator performs well under both light and heavy load conditions, the boost regulator has a 'noisy' output — attributed to physical layout and positioning of output capacitors — that could be greatly improved in a future hardware revision.

Furthermore, this positioning of output capacitors also contributes to poor transient performance. The brief but high current demand needed to fulfil these transients effects a significant voltage drop over the power bus; this is a demand that should be fulfilled by the output capacitors and the resulting voltage drop is significant enough to cause a power cycle of the 3.3 V bus.

Nevertheless, this is also an issue that can be corrected with a hardware revision.

7.2.4 Separation Switch

The functionality of both nominal operation of the separation switch and the additional functionality that the flight preparation interface provides[6] was tested and found to perform as designed. A momentary trigger is able to latch the switch with its state remembered when all system power is removed; this memory ability was tested to hold for periods of over twelve hours under standard conditions.

It was mentioned that proper verification is needed to ensure the assumptions made during the design of this subsystem hold under worst case conditions; in this regard, further testing with regards to temperature performance is needed, as well as a close analysis of part-to-part parameter variations.

When inserted, the the remove-before-flight pin able to prevent triggering; the reset input on the controller board is able to return the switch to its off state.

[6] See Appendix B.

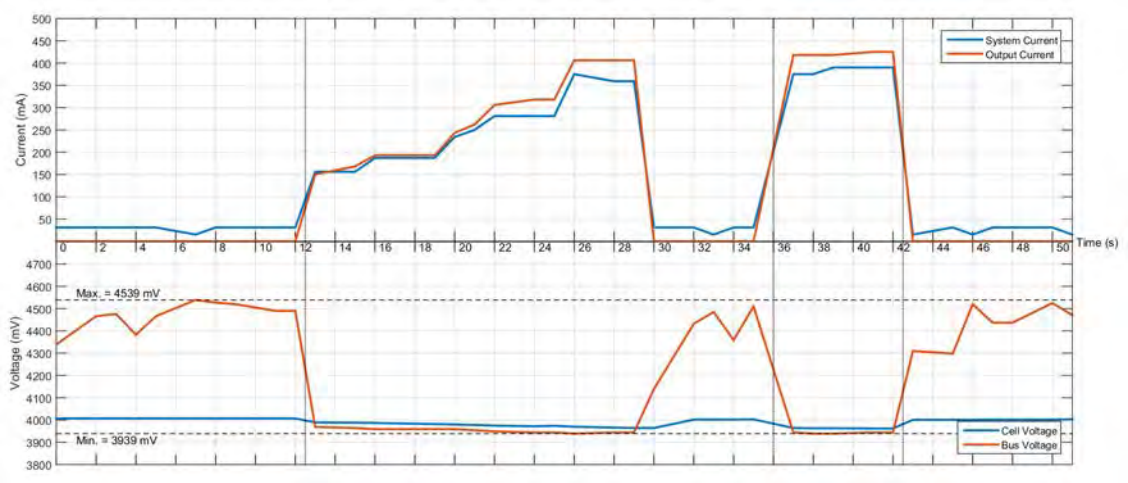


Figure 7.8: Power bus response to small system loads.

7.3 Output Capabilities

The output channels were tested in terms of their power capabilities as well as their hardware- and software-based overcurrent protection mechanisms. Although these mechanisms proved to function as designed, it was found that under high load, the voltage drop along the power bus is significant enough to drop below the buck regulator's dropout voltage. This is particularly evident when the cells are at lower states of charge and thus exhibiting low terminal voltages.

7.3.1 Transient Response

Fig. 7.8 shows the power bus' response to small (400 mA) system loads: a resistive load was connected to a channel configured for 3.3 V output with the load initially increased slowly before it was removed and subsequently re-applied at $t = 35$ s. The system and output voltage were found to remain stable under this load transient.

Before the initial load is added, it can be seen that the bus voltage reaches its maximum of 4.5 V as solar input power allows charging of the cell with a 4 V terminal voltage. When the load is introduced, this bus voltage immediately drops as the cells are required to contribute to system power requirements. It can be seen here that the small difference between cell and bus voltage implies a high ideal diode efficiency ($> 99\%$ likely, allowing for sensor errors).

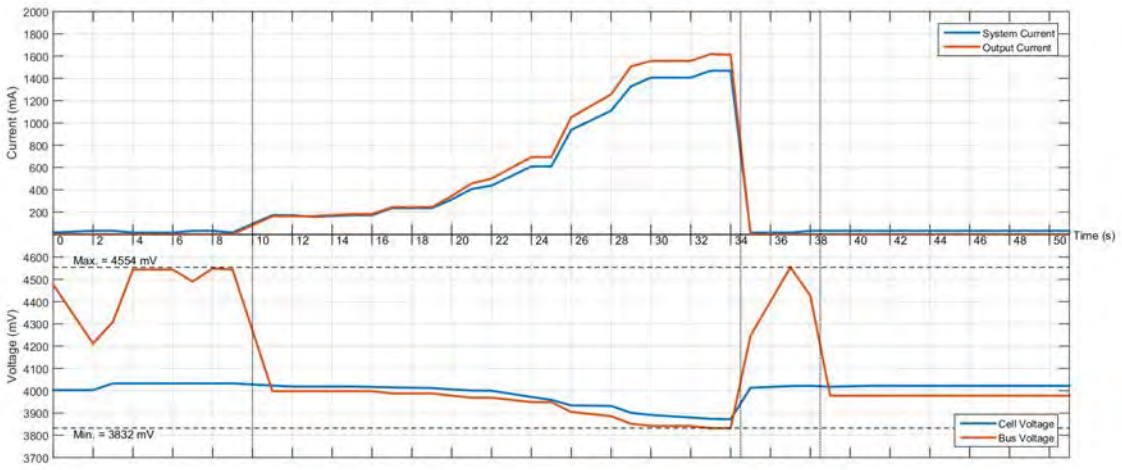


Figure 7.9: Power bus response to large system loads.

Large Transients

In Fig. 7.9 a similar test is done, although increasing output load to 1.5 A. Note that similar ground reference issues cause slight errors in sensor readings; output current should be marginally below that of the system current to account for the EPS's load.

The initial gradual increase in load is sustained by the system. However, when the full load is reconnected at $t = 38$ s, the transient results in a brief dip in the 3.3 V regulated bus that causes the microcontroller to reset: although the system manages to register the drop in bus voltage, the increase in output current is not and the last known values are plotted.

It was found that the regulator is able to serve transients up to 1 A whilst maintaining a stable output voltage; this is in line with what was designed for.

Although the application of large load transients currently results in an initial microcontroller reset, the regulator's soft-start circuitry allows for normal system operation to resume[7]. Such large transients are not expected in the application; nevertheless, this capability could be improved through the addition of greater output capacitance.

[7]This is not shown in the results due to the connection loss that the reset effects.

7.3.2 Output Control

The payload-monitoring software subsystem, described in Section 6.4, was tested with respect to its overcurrent limiting and subsequent payload recovery functionality, including its ability to disable and enable output channels.

Software-configurable channel overcurrent limits were found to be reliably detected. The subsequent process whereby the output is power-cycled for increasingly-longer periods — until the overcurrent condition clears itself — functioned as designed; cycle periods that exceed a software-configurable limit result in the logging of an error condition and the channel is subsequently disabled.

Discrete Output Control

The capacitive coupling that isolates the microcontroller from the payload switches, used as mitigation against static (DC) control errors affecting the output, was extensively tested. With reference to the schematic of Fig. 5.13, it was found that semi-discrete control is possible: software is able to keep the output off but with a ±200 µs 'on' period needed every ±500 ms to charge C54. This is the capacitor that controls the reset functionality and that needs to be charged before the following reset cycle. For a typical load, it was found that this pulse is still long enough to charge the bulk and decoupling capacitors; although the load would likely not function, this is undesirable and it is suggested that modifications be made.

The suggested modification is that the subsystem be subtly re-designed to allow an active high control signal to maintain a high input on the RESET pin. This would keep the internal comparator's latch enabled and thus temporarily disable the automatic reset functionality. An active low signal should have no effect, however, as this would increase the likelihood of a hardware- or software-based error disabling the hardware overcurrent protection.

Permanent Output Isolation

In order to provide the ability to permanently isolate a faulty payload, it is suggested that a fuse be used that, when blown, ensures the output can no longer be a load

on the system. One possible position for such a fuse could be on the output with a MOSFET used to cause a brief short circuit at the point beyond the fuse. However, this approach has a few drawbacks:

- The hardware overcurrent protection would need to be temporarily disabled;
- It may be possible that a recoverable short circuit on the output results in this fuse being inadvertently blown; and
- In order to blow a fuse as fast as possible, a much greater current is needed than that for which it is rated, and the system may not be able to reliably provide this; this is considered the most fundamental drawback.

A preferred position for a fuse would be between the gate of the switch's power MOSFET and the open-drain comparator output. A 100 mA fuse could rapidly be blown with a 1 A current that a system of MOSFET switches could provide. Using multiple control lines would ensure that this is only done on intention.

7.3.3 Feedback Phenomenon

As a result of the feedback used to implement the reset functionality, a phenomenon exists whereby if a sufficient downstream voltage is applied, a form of equilibrium can occur where the payload switch is off but unable to automatically reset. This can be observed when debugging the system via the JTAG interface: the push-pull outputs of the host processor can provide enough current to bias the microcontroller's internal ESD protection diodes, and thus provide a small voltage to the EPS's V_{cc} net. ADC input pins connected to bus-side subsystems can induce the same effect, as can an external serial interface with a push-pull transmit output and/or a pull-up resistor on the receive input.

This is only an issue for the EPS payload switch as a functional system has the ability to manually reset other output channels. Preventative measures have been taken for the EPS, including high-impedance and open-drain inputs and outputs on the Flight Preparation Controller's serial interface.

Chapter 8

Conclusions

This work set out to develop a fully-functional, CubeSat-compatible, Electrical Power System module for use on future CubeSat projects. The lack of previous work on such a module (in a local capacity) meant that a bottom-up design approach was used: background and some fundamental theory was considered and existing flight-proven systems were analysed and discussed.

Each subsystem within the EPS was carefully designed and its failure modes and implications considered. Initial testing and results have shown that each subsystem functions as designed, and that the overall design implements a fully-functional system.

Although it was ensured that all components are specified for the operating environment and that all calculations (where applicable) take worst case conditions into account, full environmental testing and qualification is still needed. Recommendations are made in this regard.

The following conclusions cover the four fundamental aspects of the design: reliability, power capabilities, functionality and efficiency. Although not central to the design of the system, the supporting software is also covered.

8.1 Reliability

Reliability is a difficult metric to gauge without significant and lengthy testing and, in the case of such a module, flight heritage. Neither was possible over the available time-frame, but initial testing has been positive. The failure modes and mechanisms of each subsystem were discussed and analysed in depth: a few single points of failure were identified along the power bus, and careful electronic design and component choice was used to mitigate against such failures occurring.

The single points of failure are limited to radiation-induced single-event effects, with total-ionising dose effects causing degradation of system performance. It is likely that the eventual failure of the system will result from the combination of various smaller failures, occurring over an extended period of time, rather than a particular design weak point.

A degree of redundancy is present for a number of subsystems, including true redundancy for individual battery/cell failure and failure of one or two of the input stages. These failure modes do, however, result in a loss of system performance capabilities, but intelligent power management can ensure satellite operation continues.

A key design element was using the microcontroller to perform system optimisations rather than rely upon it for system operation. This goal was achieved and although system capabilities are reduced, operation can continue. Nevertheless, a high degree of microcontroller reliability has been introduced through the selection of a device with hardware EDAC implementations on all memory interfaces.

8.2 Functionality

The subsystems were all carefully specified to provide functionality equal or exceeding that of existing modules. All subsystems were comprehensively tested and found to function as designed.

Additional software needs to be written to implement full system functionality, including the external communications module. Frameworks have been set up within the application and thus the implementation of said full functionality is a rela-

tively minor task. Effective device power management is also needed in order to reduce EPS power consumption to the 50 mW target; it was shown that this is an achievable target.

The design of an external battery module has not been completed, although such a module will simply consist of multiple replications of the current cell subcircuit. An interface in the form of a physical connector, along with appropriate functional descriptions, has been provided for future design of this module.

8.3 Power Capabilities

Optimistic power-related specifications were made and were not fully achieved. However, these shortcomings were attributed to physical board layout rather than a flawed system design.

The cause of these issues arises from the single-cell battery string configuration, and the corresponding lower bus voltage, that introduces a significant design change from that of existing modules. This lower voltage makes parasitic trace resistance a far more crucial consideration: firstly, a greatly increased current is carried by the bus; secondly, and as a result of this increased current, a greater voltage drop is experienced that results in a small window in which the buck regulator can reliably operate. Nevertheless, it is not desired to change this design: its advantages are still present and it is anticipated that a revised layout will address the issues. Power capabilities can correspondingly be raised to the initial specifications.

Solar input stages were found to operate as expected and at the specified power levels.

8.4 Efficiency

Efficiency was made a key design goal, although it was argued that reliability cannot be ignored when they are placed against each other. The majority of subsystem efficiencies are nevertheless in line with existing modules: each SEPIC input stage has an 80% DC-DC conversion efficiency and regulators operate at nominal efficien-

cies of 95%. An inefficiency was introduced with individual cell charging circuitry which is around 90%; discharge via the ideal diode has negligible losses. These losses were argued to be justified through the ability to isolate one or more cells.

Full optimisation of the maximum power point tracking (MPPT) algorithm was not performed, but it was demonstrated that efficiencies, in terms of operating at the maximum power point, approach 90%+. Additional work is needed to achieve similar efficiencies for fast-changing irradiance conditions. In addition, it is expected that an 100% efficiency can be approached under optimal conditions.

8.5 Supporting Software

An initial set of supporting software has been developed, including an interface GUI for module configuration and MATLAB classes for abstracting away from the command line system. In addition, further MATLAB classes have been developed to aid in MPPT algorithm optimisation, as well as characterisation of bus power flow to determine system efficiencies and capabilities.

The interface GUI needs additional work to allow full module configuration, and a suite of ground-station software needs to be developed.

8.6 Cost

Although cost is not a critical factor in such specialised applications, it is worth noting that the cost to populate the module, including all components and the physical circuit board, is in the order of R4000. With minimum order quantities and price breaks, the production of multiple modules would see a far-reduced cost-per-module.

Chapter 9

Recommendations

Given the aim of producing a system that is a realistic alternative to commercially available and flight-proven systems, it is believed that such a goal can be met with a few modifications and further testing of the work that has been presented here.

To this extent, the following recommendations are made:

9.1 Hardware Revision

A hardware revision is needed to implement the suggested changes and improve performance. These improvements will allow the module to meet the full specifications that were set.

Although the current module can and should initially be used to test its compatibility with actual CubeSat subsystems, this revised hardware will be needed before full performance data can be gathered.

9.1.1 LDO Regulator for EPS

A linear low drop-out regulator should be included in the design to serve the EPS's power needs. This would provide a number of advantages:

- An additional output channel will become available for use by an external payload;
- The EPS will have the ability to completely disable both regulated buses to conserve power should it become necessary; and
- Large transients (or short circuits) on the 3.3 V bus will not affect operation of the EPS which, in turn, can concentrate on isolating the problem.

The failure modes of this additional component would need to be looked at carefully to ensure this has no adverse effects on the system.

9.1.2 Output Isolation

As discussed in Section 7.3.2, a method for permanently isolating output channels should be considered. Various implementations were discussed in the aforementioned section and additional options may exist. This would increase the module's ability to cope after the failure of a payload, should such a failure be severe.

9.1.3 Physical Layout

The PCB should be redesigned on a four-layer board to improve grounding and power handling abilities, amongst other benefits. In particular, this will allow more copper area to increase the widths of high-current traces. Some noise and voltage ripple was present on the regulated buses; while a redesigned layout should offer some improvements, it is also suggested that output capacitance be better implemented.

The routing of the power bus needs to be redesigned in order for it to take the shortest possible path from the input stages to the regulator payload switches and, ultimately, the header. This should be a sufficient improvement for the module to meet the specified power capabilities.

9.2 Software Refinement

A number of software additions and improvements are needed to fully optimise the system. In addition to the work listed below, development should continue on the supporting software; this is not however crucial work until such a time that a flight-ready module has evolved.

9.2.1 Error Handling

The ECC error-handling ability of the application should be further tested and refined. The use of multiple application images in flash should be implemented and thoroughly tested to ensure that it is a reliable method of handling non-correctable flash errors.

The microcontroller's Error Correction Status Module's ability to simulate bit errors should be extensively used, to fully characterise the response of the application to different types, and frequencies, of bit errors.

9.2.2 Power Management

The flexible power management features of the microcontroller should be exploited to reduce power consumption as far as possible. It was stated that a lower system clock frequency and proper use of the standby mode should be able to reduce average power consumption considerably.

9.2.3 MPPT Algorithm

As discussed, the maximum power point tracking algorithm needs refinement to cope with fast-changing irradiance conditions, or at least improve performance in more constant conditions. The software tools and testing environment developed for this purpose can be used. Increased control resolution and/or the introduction of a feedback path, to adjust the setpoint based to the input voltage, could be considered to improve control over the operating point.

9.3 Further Testing

Once the hardware revision has been completed, the module should be subjected to radiation testing, vibration testing, vacuum cycling and operation in temperature extremes.

The radiation testing in particular should be used to confirm the theory used throughout the design stages. The two different p-channel power MOSFETs used - the AON7407 and IRF7329 - should be further characterised with respect to SEE and TID effects. If useful and positive data is obtained, it would be beneficial to make this data public to allow the devices be used in other space-based applications.

It should be attempted to induce latch-up events in the relevant devices to confirm the operation of the protection mechanisms used. Such events must reliably clear themselves; if not, alternative designs for this protection should be investigated.

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Appendix A

The EPS Module

This appendix describes the operation and specifications for the current revision of the EPS module. Maximum input and output ratings are listed in Section A.3 and photographs can be found in Section A.4.

A.1 External Connections

Fig. A.1 shows the physical placement of the module's connectors. The Debug and Flight Preparation ports are contained on the underside of the module and are not pictured.

A.1.1 Solar Inputs

Solar panels are connected via four-pin Molex Picoblade connectors, with two connectors available for each input channel. The positions of these connectors is shown in Fig. A.1. With respect to the pin numbering in Fig. A.2a, pins are assigned as follows:

Pin No.	Function
1, 2	$V+$
3, 4	Ground

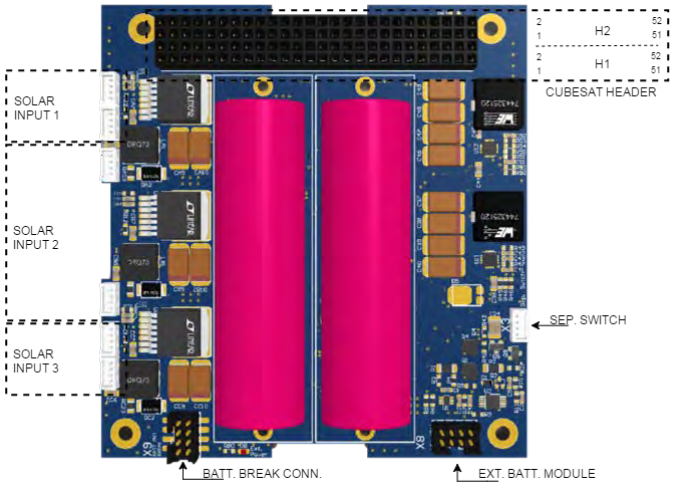


Figure A.1: Position of physical connectors on the topside of the module.

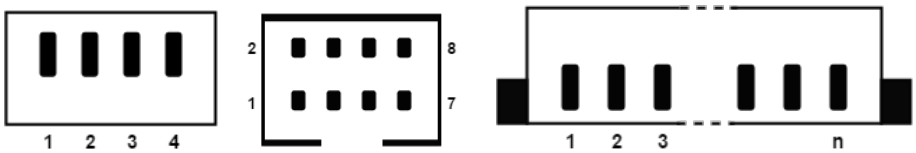


Figure A.2: Pin numbering of the (a) four-pin Molex Picoblade connectors, (b) the eight-pin FCI connectors and (c) the n-pin right-angle Picoblade connectors.

Each input per channel should have an external blocking diode if they are to be positioned such that each is not on the same satellite face.

A.1.2 Battery Break Connector

The battery break connector (X9) allows the ground terminal connection of both cells to be disconnected from the module's ground, and thus the cells completely isolated. The ground connector from the external module interface is also routed through this connector.

With respect to the pin numbering in Fig. A.2b, pins are assigned as follows:

Pin No.	**Function**
1, 3, 5, 7	Module Ground
2, 4, 6, 8	Battery Ground

A.1.3 External Battery Module Connector

The external battery module connector (X8) can be used to interface further cell subcircuits to the system. This connection is done via an eight-pin connector; pin functionality, with respect to Fig. A.2b, is as follows:

Pin No.	Function
1, 2, 3	Battery Ground
4, 5, 6	Battery Bus
7	SDA (Ext. module I^2C bus)
8	SCL (Ext. module I^2C bus)

The I^2C bus on this connector is a multiplexed bus and not linked to the satellite bus.

A.1.4 Separation Switch

The position of the separation switch (X3) input is indicated in Fig. A.1 and uses the same four-pin Picoblade connector. Pin definitions are as follows:

Pin No.	Function
1, 2	Trigger
3, 4	Ground

To latch the separation switch, pins one and/or two should be momentarily bridged to pins three and/or four. Note that the ground connection on this connector is routed through an additional switch that implements the Remove Before Flight (RBF) pin functionality; although the trigger input can be bridged to a permanent ground, this will negate the RBF switch.

A.1.5 JTAG / Debug Port

The JTAG / Debug port is implemented on connector X7 and is further described in Appendix E. Its pin numbering is as seen in Fig. A.2c.

A.1.6 Flight Preparation Port

The Flight Preparation port is implemented on connector X6 and its functionality is described in Appendix B with pin definitions listed in Table B.1. Its pin numbering is as seen in Fig. A.2c.

A.1.7 CubeSat Kit Header

The pin numbering of the CubeSat Kit Header is shown in Fig. A.3 with its orientation explicitly shown in Fig. A.1.

Pin functionality is as follows:

Pin No.	**Function**	**Pin No.**	**Function**
H1.41	I^2C SDA	H2.25, H2.26	5 V Bus
H1.43	I^2C SCL	H2.27, H2.28	3.3 V Bus
H1.47	Output Channel 6	H2.29, H2.30, H2.31, H2.32	Ground
H1.49	Output Channel 5	H2.45, H2.46	Battery Bus
H1.50	Output Channel 4	H2.51	CAN H
H1.51	Output Channel 3	H2.52	CAN L
H1.52	Output Channel 2		

If CAN is used and the EPS is the end-of-bus node, termination resistor R82 can be placed and should typically have a resistance of 120 Ω.

H2.2	H2.4	H2.6	H2.8	H2.10	H2.12	H2.14	H2.16	H2.18	H2.20	H2.22	H2.24	H2.26	H2.28	H2.30	H2.32	H2.34	H2.36	H2.38	H2.40	H2.42	H2.44	H2.46	H2.48	H2.50	H2.52
H2.1	H2.3	H2.5	H2.7	H2.9	H2.11	H2.13	H2.15	H2.17	H2.19	H2.21	H2.23	H2.25	H2.27	H2.29	H2.31	H2.33	H2.35	H2.37	H2.39	H2.41	H2.43	H2.45	H2.47	H2.49	H2.51
H1.2	H1.4	H1.6	H1.8	H1.10	H1.12	H1.14	H1.16	H1.18	H1.20	H1.22	H1.24	H1.26	H1.28	H1.30	H1.32	H1.34	H1.36	H1.38	H1.40	H1.42	H1.44	H1.46	H1.48	H1.50	H1.52
H1.1	H1.3	H1.5	H1.7	H1.9	H1.11	H1.13	H1.15	H1.17	H1.19	H1.21	H1.23	H1.25	H1.27	H1.29	H1.31	H1.33	H1.35	H1.37	H1.39	H1.41	H1.43	H1.45	H1.47	H1.49	H1.51

Figure A.3: Pin numbering of the CubeSat Kit Header connector.

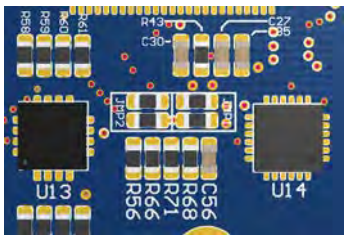


Figure A.4: Position of the communications-bus jumpers on the PCB.

A.2 Communications Configuration

In addition to needing selection via software, the use of CAN or I^2C as the main communications bus needs some hardware configuration. With respect to the designators in the Top Level schematic (see Appendix D), the following configuration is needed:

	Jumper 1		Jumper 2		I^2C -SPI Bridge	CAN Transceiver
Configuration	**R69**	**R70**	**R57**	**R67**	**U14**	**U16**
I^2C	DNP	DNP	0 R	0 R	Place	DNP[1]
CAN	0 R	0 R	DNP	DNP	DNP[1]	Place

DNP = do not place.

[1] DNP optional, but will result in increased power consumption if not.

The physical location of the zero-ohm jumpers are indicated in Fig. A.4.

A.3 Specifications

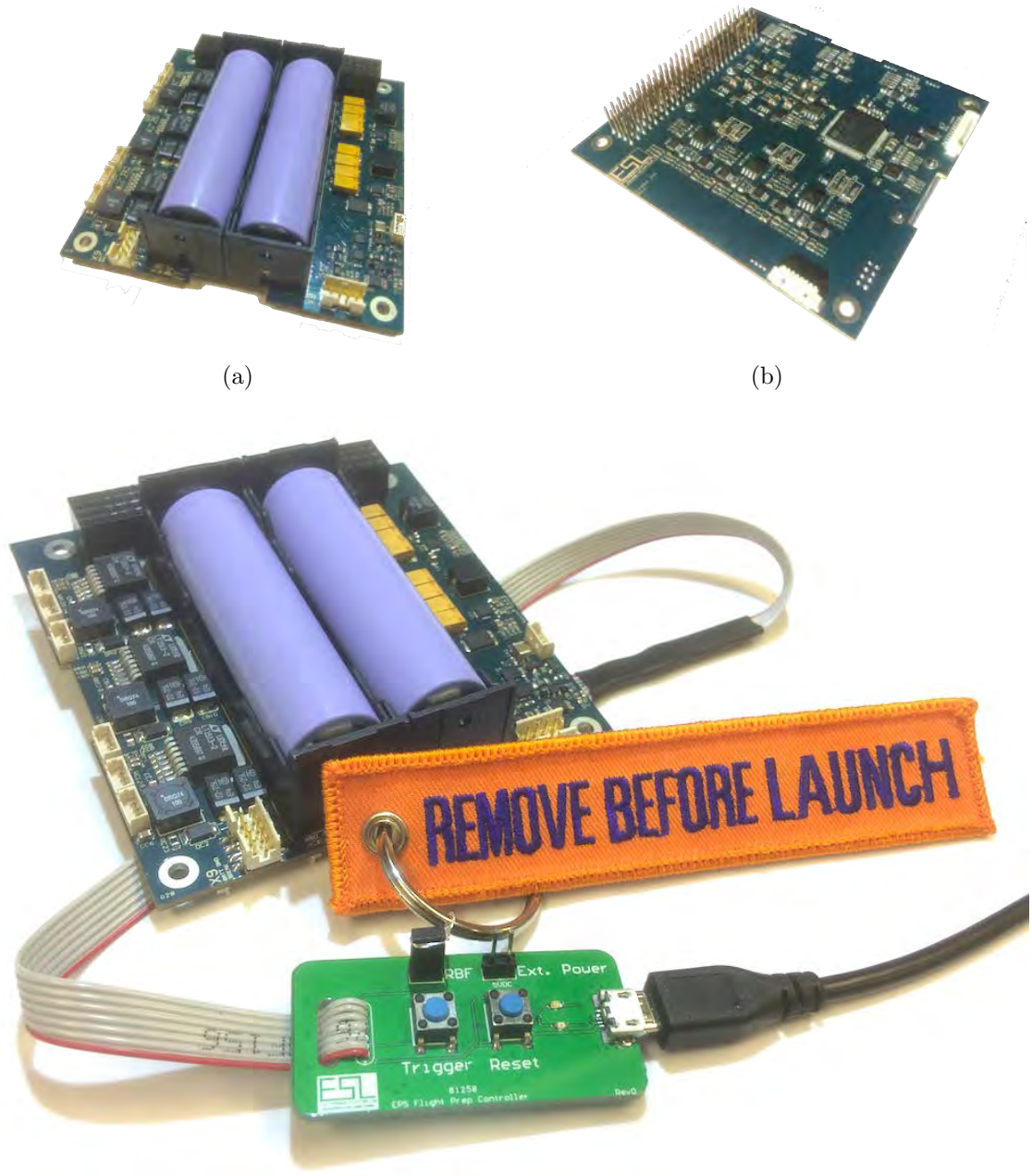
The specifications for the current hardware revision are listed in Table A.1. Note that where indicated, specifications are subject to improvement in a future hardware revision.

A.4 Photographs

Photographs of the module are shown in Fig. A.5.

Table A.1: EPS specifications for the current hardware revision.

	Min.	Typ.	Max.	Units	Notes
Solar Inputs					
Input Voltage	3		18	V	Limited by max. input power
Input Current			1	A	
Input Power			4.2	W	Limited by combined input power
Default Operating Point		200		mA	Hardware-configurable
MPPT Efficiency		86	92	%	Constant irradiance
Combined Input Power			8.2	W	
Converter Efficiency			80	%	
Battery					
Float Voltage	4.15	4.20	4.24	V	4.1 V typical possible with IC substitute
Charging Efficiency		90	92	%	
Discharge Efficiency		99		%	
On-board Capacity		18		Wh	
Bus					
Nominal Voltage	3.5	4.5	4.84	V	
External Charging Voltage	4.4		5	V	
Current Limit (Hardware)		6		A	
Current Limit (Software)			6000	mA	
Power Cycle Length	400		500	ms	
Separation Switch					
Trigger Pulse Current			$\ll 1$	mA	
Latching Memory			$\gg 120$	min	Subject to additional verification
Regulated Buses					
5 V Bus Current			3	A	To be increased with layout changes
3.3 V Bus Current			3	A	To be increased with layout changes
Efficiency		95		%	
Output Switches					
Current Limit (hardware)		2.5		A	To be increased with layout changes
Current Limit (software)			4095	mA	
Power Cycle Length (hardware)	400		500	ms	
Power Cycle Length (software)	50		30000	ms	
Load Transient			1	A	
Electrical Power System					
Supply Voltage		3.3		V	
Average Supply Current		15*	40	mA	* To be confirmed with a software update
Shutdown Current		1	7	mA	
I^2C Clock Frequency			400	kHz	
Serial Baud Rate		9600		baud	



(a) (b)

(c)

Figure A.5: Photographs of the prototype module. (a) Top view, (b) bottom view, and (c) the module with flight controller interface attached.

Appendix B

Flight Preparation

To enable pre-flight configuration, testing and high-level debugging by the mission design team, a flight preparation system has been included in the design. The physical interface allows connection to the inputs for the additional separation switch functionality, the battery bus for charging, and the micrcontroller's serial interface for preparation mode configuration and testing.

B.1 The Physical Interface

The controller interface is pictured in Fig. B.1 and includes a USB-serial transceiver, push buttons for triggering and resetting the separation switch, and headers for a remove-before-flight (RBF) pin and external power input. Although the USB connection can be used to charge the batteries, the external power pins could be used if limited USB power is available. The trigger input on this controller is not affected by the state of the RBF pin.

In order to prevent the phenomenon described in Section 7.3.3 whereby power can be inadvertently transferred to an 'off' system via the serial lines, circuitry is included on the interface to implement an open-drain transmit output and a high-impedance receive input. The open-drain output requires that an internal pull up resistor be enabled on the microcontroller.

Table B.1: Pin definitions for the Flight Preparation Controller interface.

Pin Number	Name	Description
1	Reset	Short to ground to reset the separation switch
2	Trigger	Short to ground to trigger the separation switch[1]
3	RBF	Short to ground to implement the Remove Before Flight pin functionality
4	TX	Serial transmit line (open-drain output)[2]
5	RX	Serial receive line (high-impedance)[2]
6	Battery Bus	4.4–5 VDC input to allow battery charging and/or system operation
7	Ground	Board ground connection

[1] Trigger functionality is independent of the state of the RBF input.
[2] Default baud rate is 9600.

B.1.1 Pin Definitions

Connection to the EPS module is accomplished via a seven-way ribbon cable that connects to physical connector X6 on the underside of the board. Pin definitions are as indicated in Table B.1, and the schematics of the board can be found in Appendix D.

B.1.2 USB Connection

The USB transceiver is an FTDI interface that does not require special drivers. The device should appear as a standard COM port on the host.

Figure B.1: Photograph of the Flight Preparation Controller interface.

B.2 The Software Interface

Communication with the board is done via the serial interface. Both a text-based command line and an interactive graphical user interface (GUI) are available, and are briefly described in the following sections.

Serial communication is only available when the module is in its 'preparation mode' — this mode is intended for configuration and testing only, and should be exited before flight. It can be exited from either the command line or GUI, and can be re-enabled via a specific sequence of commands using the satellite's communication bus (CAN or I^2C).

B.2.1 Command Line

A text-based command line is available to test and configure the module. Commands are sent and received over the serial link and are only available when the module is in preparation mode. The list of available commands is documented in Table B.2.

A command takes the form of a descriptive ASCII string, followed by one or more numeric parameters, separated by single white-space characters. A single new-line character is used to signify the end of the command.

B.2.2 Graphical User Interface

A GUI has been developed to provide a visual overview of the system and allow abstraction from the command line. The command line is, however, used to access the module and thus no additional functionality is available.

A screenshot of the interface is shown in Fig. B.2.

Table B.2: Commands available in preparation mode.

Command & Parameters	**Description**
`reset`	Perform a software reset
`standby`	Enter standby mode
`textenab`[1,2]	Enable/disable text responses
`settings`	Display system settings
`settingsdefault`	Restore default system settings
`settingssave`	Save current system settings
`cellenab [cell_number]`[1]	Enable/disable cell charging
`cellset [cell_number] [value]`	Set cell charge rate (0–127)
`pvenab [input_channel]`[1]	Enable/disable an input channel
`pvset [input_channel] [value]`	Set input operating point (0–255)
`mpptenab`[1]	Temporarily enable/disable power point tracking
`bustrip`	Perform a bus trip
`trip [channel_number]`	Perform a channel trip
`chon [channel_number]`	Turn an output channel on
`choff [channel_number]`	Turn an output channel off
`cellsave [cell_number]`	Save a cell's status to the log
`readingssave`	Save the current housekeeping readings to the log
`measure`	Get a cell's current status
`cellstatus [cell_number]`	Display the current housekeeping readings
`errorlog [log_index]`[3]	Get a saved error log
`celllog [log_index]`[3]	Get a saved cell status log
`readingslog [log_index]`[3]	Get a saved readings log

[1] Substitute `disab` for `enab` for opposite functionality.
[2] Non-text responses are used by the GUI to receive structure-based data responses.
[3] Log indices range from zero to the number of available logs, as indicated in the system settings.

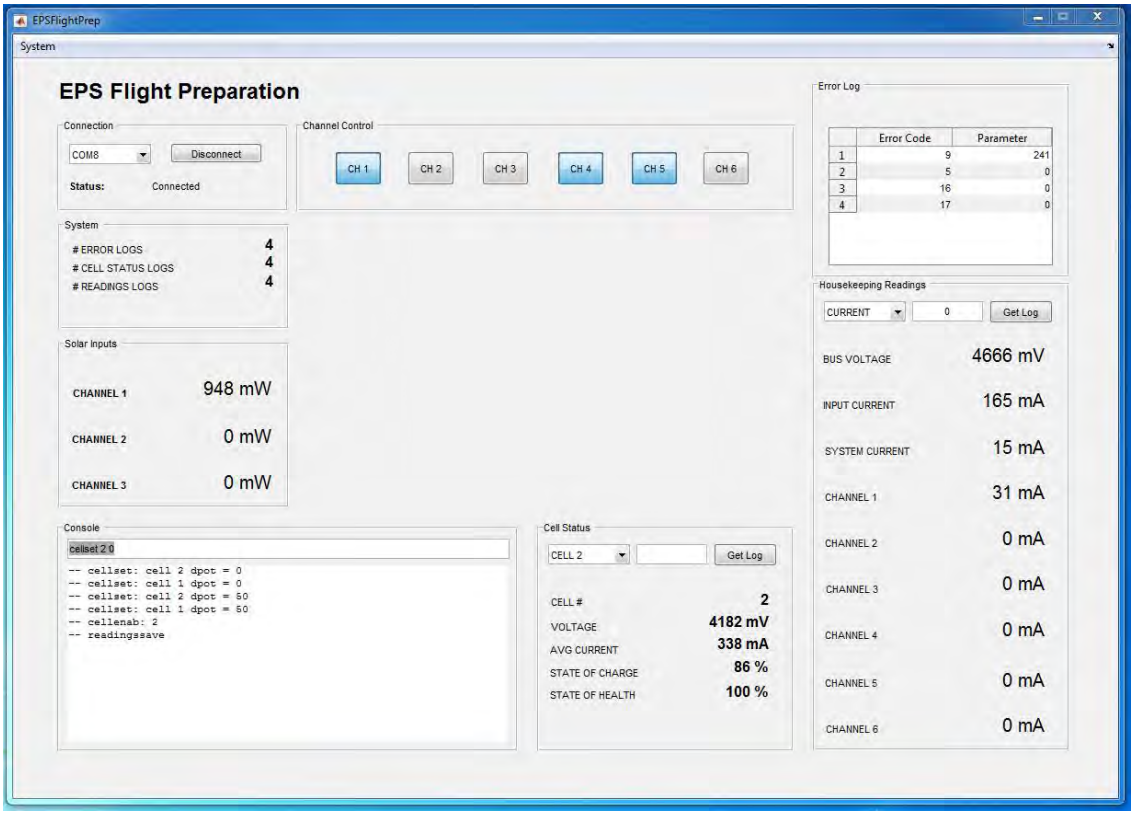


Figure B.2: Screenshot of the Flight Preparation GUI.

B.2.3 Preparation Mode

Preparation mode is fundamentally a state that the module initialises into, whereby the serial interface is enabled, with the system continuously checking whether commands are available to be parsed. The system is also prevented from entering standby when in this mode.

Preparation mode is exited by the `prepexit` command, followed by two keys as parameters. These keys are '1234' and '2580' respectively. Once executed, the system resets and begins nominal operation. With the exception of the system prevented from entering standby, all other system functionality is available in this mode.

To return to preparation mode, the module needs to be commanded via the chosen communications interface (CAN or I^2C). The `prepenter` command should be issued, followed by the same two keys. Exact implementation depends on the interface and thus formatting is to be confirmed upon finalisation of the communications system.

Appendix C

Solar Simulation & Panel Characterisation

The environment experienced by solar panels in space, particularly those on satellites in Low Earth Orbit, is significantly different from the environment experienced on Earth. In particular the vast temperature swings, and potential fast-changing irradiance conditions, cause frequent and large changes in the current-voltage characteristic of the panels. In order to better simulate such conditions, a testing environment was developed that uses infra-red (IR) bulbs in an enclosed box. The panels used for testing were also characterised within this environment to provide a benchmark to which power point tracking algorithms can be compared against.

C.1 Simulator Design

The testing environment is one or more fully-enclosed boxes — used to represent different faces of a satellite — each with two 175 W IR bulbs used to simulate sunlight. Different configurations of panels can be placed in the box and the power to each set of bulbs can be independently varied. An AC dimmer controller was developed to control the irradiance within each box; with a serial interface, a simulation can be set up that requires no user input. The schematic design of this controller can be found in Appendix D.

Table C.1: Commands available for the solar-simulation controller.

Command & Parameters	**Description**
`[channel] [value]`	Sets a channel (1–4) to the specified value (0–255)
`[channel]`	Returns the current channel value
`T [1,2]`	Returns the temperature (in ^{o}C) of one of the two sensors on the controller
`T 3`	If implemented, returns the temperature (in ^{o}C) of the external temperature sensor

Fans are used to cool the panels due to the intense heat that the IR bulbs radiate, and a temperature sensor is placed amongst the panels, to both record panel temperature and to allow the controller to automatically turn off the outputs should the temperature rise too high.

The controller uses a lookup table to accurately switch the AC waveform to a desired percentage power output (assuming a purely resistive load). Irradiance percentages given in this chapter refer to this percentage power output.

C.1.1 Serial Interface

For reference purposes, the available controller commands are listed in Table C.1. The serial connection uses a default 9600 baud rate and commands should be terminated with a single new-line character.

C.2 Solar Panel Characterisation

The EPS module's solar inputs were tested using an array of two parallel PET-laminated panels. Each panel is rated for 1.3 W output, with $V_{oc} = 6$ V and $I_{sc} =$ 260 mA. Using a varying resistive load, the plots of Fig. C.1 were obtained, at an average temperature of approximately 35^{o}C, and at maximum simulator irradiance.

It can be seen that a very 'flat' I-V characteristic on the left of the maximum power point (MPP, indicated by dotted lines) results in a small difference in output current for $0 < V < V_{mpp}$. This has implications for current-based operating point control:

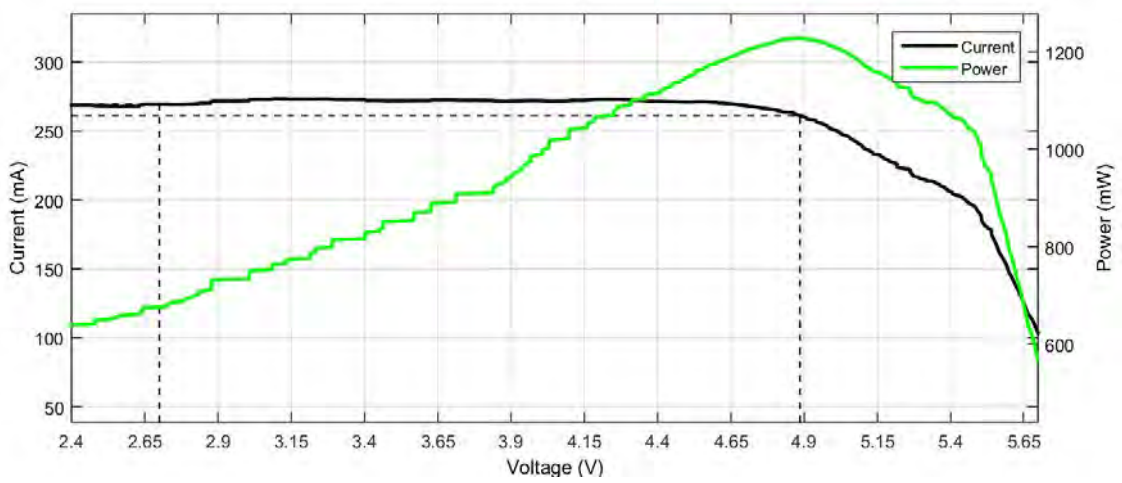


Figure C.1: I-V and P-V curves of the solar panels used during testing.

a small increase in operating point can take a DC-DC regulator from operating at V_{mpp} to a voltage below its minimum. It thus follows that such a regulator is unlikely to be able to reliably maintain an operating point to the left of the MPP.

C.2.1 Temperature & Irradiance Variation

Fig. C.2 shows the maximum power output for different irradiance levels and at different temperatures. The plots are, in fact, a linear best-fit of the data points, which appears to accurately characterise the temperature variation within this 35–60^{o}C range.

For a maximum temperature of 35^{o}C over the brief test period, the plots of Fig. C.3 were obtained. These plots are second-degree polynomial best-fits of the data, and show the scaling and slight shifting of the MPP for different irradiance levels.

C.2.2 Estimation of Available Power

The plot in Fig. C.2 can be used to determine an estimation of available power given a panel temperature and level of irradiance. This is a useful benchmark to determine the efficiency of a maximum power point tracking algorithm.

Exploiting the linear relationship between power and temperature and the near-

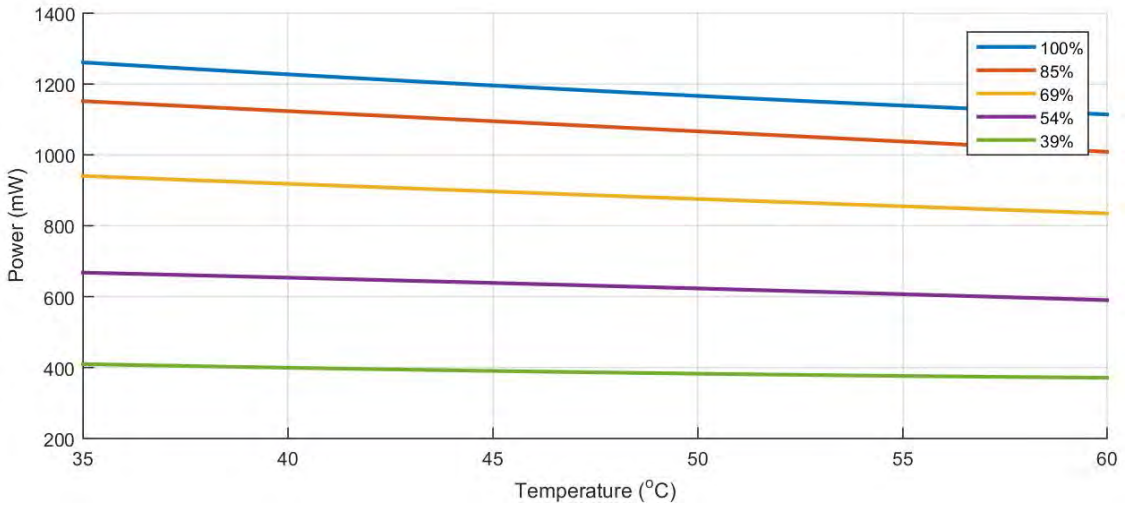


Figure C.2: Variation in maximum panel output power with temperature for different irradiance levels.

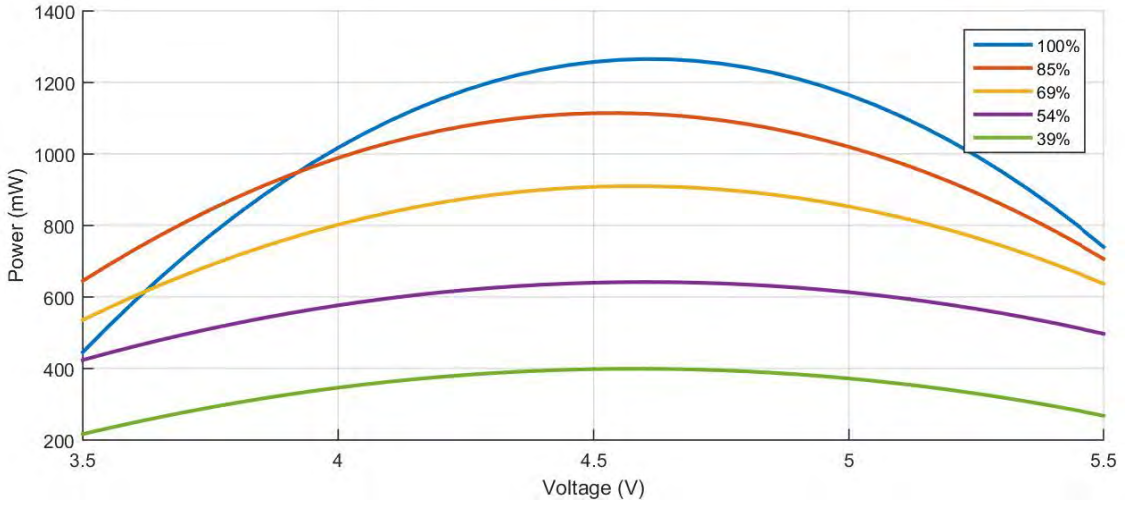


Figure C.3: Variation in the panel's P-V curve with different irradiance levels at 35^{o}C.

second-degree relationship between power and irradiance, an expression of the form

$$P_{max}(C,T) = \left(a_2C^2 + a_1C + a_0\right) + \left(b_2C^2 + b_1C + b_0\right)T. \tag{C.1}$$

can be obtained where C is the level of irradiance and T the panel temperature. MATLAB code is included in the supporting material that calculates the coefficients from a set of input data.

Appendix D

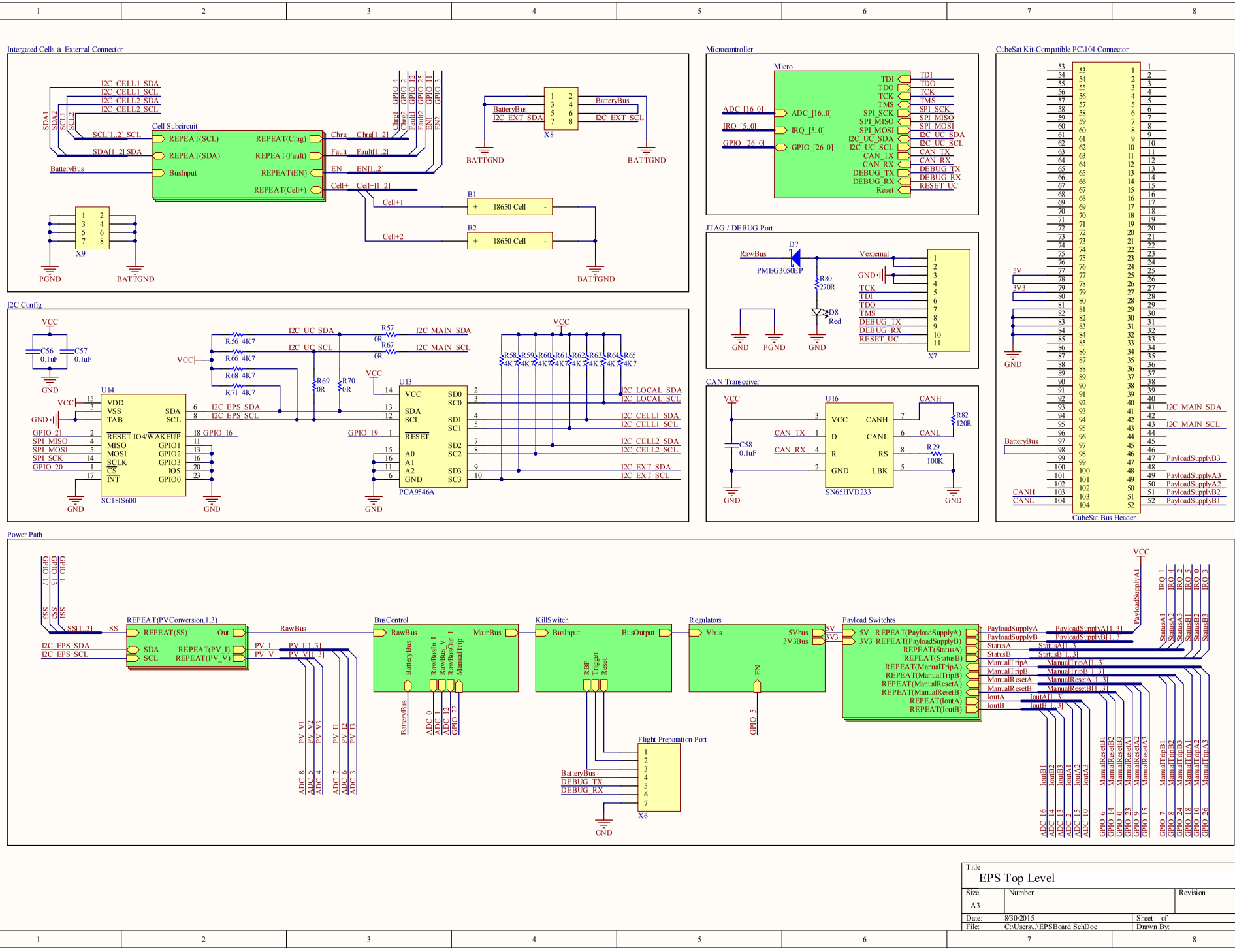
Schematics

D.1 Electrical Power System

The following schematics are of the first iteration of the full Electrical Power System module. The first schematic is a top-level schematic that links subsystems together and contains supporting circuitry.

Design files can be found in the supporting material under the `PCBs/EPSRev0` folder.

During initial development stages, two additional EPS-related PCBs were constructed to test solar panel operating point control and the cell subcircuit design. Design of the final hardware did not vary significantly from these initial revisions and thus these have not been discussed in the text. Nevertheless, the design files can also be found in the supporting material under the `PCBs/PVConversionRev0` and `PCBs/BatteryBoardRev0` folders.


Intergated Cells a External Connector
Cell Subcircuit
REPEAT(SCL)
REPEAT(SDA)
BusInput
REPEAT(Chrg)
REPEAT(Fault)
REPEAT(EN)
REPEAT(Cell+)
I2C_CELL1_SDA
I2C_CELL1_SCL
I2C_CELL2_SDA
I2C_CELL2_SCL
BatteryBus
B1
B2
18650 Cell
X8
X9
BATTGND
PGND
Microcontroller
Micro
ADC_[16..0]
IRQ_[5..0]
GPIO_[26..0]
TDI
TDO
TCK
TMS
SPI_SCK
SPI_MISO
SPI_MOSI
I2C_UC_SDA
I2C_UC_SCL
CAN_TX
CAN_RX
DEBUG_TX
DEBUG_RX
RESET_UC
Reset
CubeSat Kit-Compatible PC\104 Connector
CubeSat Bus Header
JTAG / DEBUG Port
RawBus
D7
PMEG3050EP
R80
270R
D8
Red
Vextemal
X7
I2C Config
U14
SC18IS600
U13
PCA9546A
VCC
GND
I2C_UC_SDA
I2C_UC_SCL
I2C_MAIN_SDA
I2C_MAIN_SCL
I2C_EPS_SDA
I2C_EPS_SCL
I2C_LOCAL_SDA
I2C_LOCAL_SCL
I2C_CELL1_SDA
I2C_CELL1_SCL
I2C_CELL2_SDA
I2C_CELL2_SCL
I2C_EXT_SDA
I2C_EXT_SCL
CAN Transceiver
U16
SN65HVD233
CANH
CANL
CAN_TX
CAN_RX
Power Path
REPEAT(PVConversion,1,3)
BusControl
KillSwitch
Regulators
Payload Switches
Flight Preparation Port
X6
RawBus
MainBus
BusInput
BusOutput
Vbus
5Vbus
3V3Bus
5V
3V3
PayloadSupplyA
PayloadSupplyB
StatusA
StatusB
ManualTripA
ManualTripB
ManualResetA
ManualResetB
IoutA
IoutB
Title
EPS Top Level
Size
A3
Number
Revision
Date:
8/30/2015
File:
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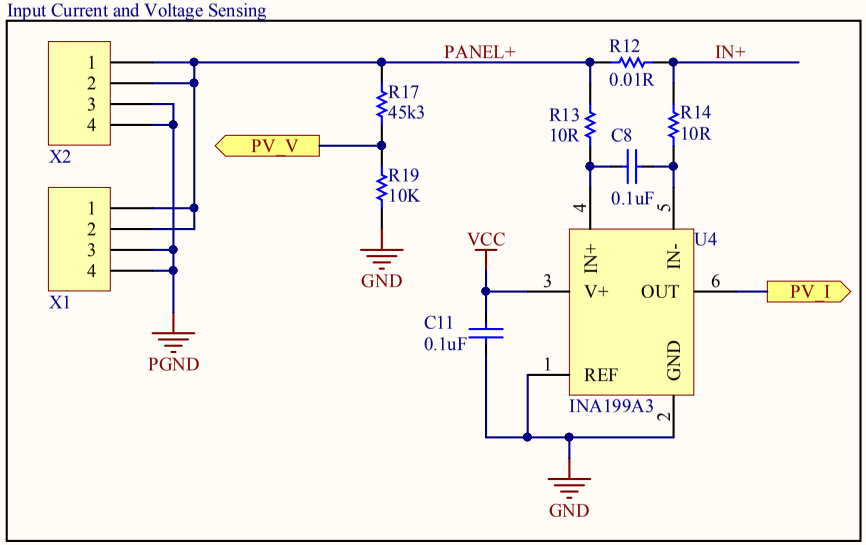
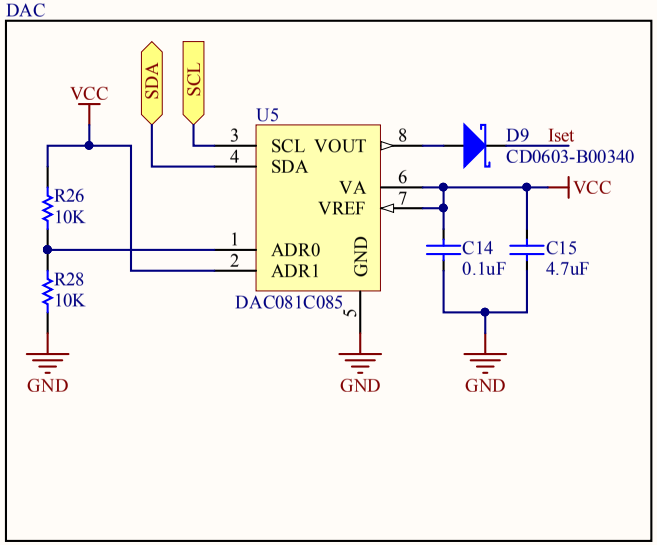
Drawn By:

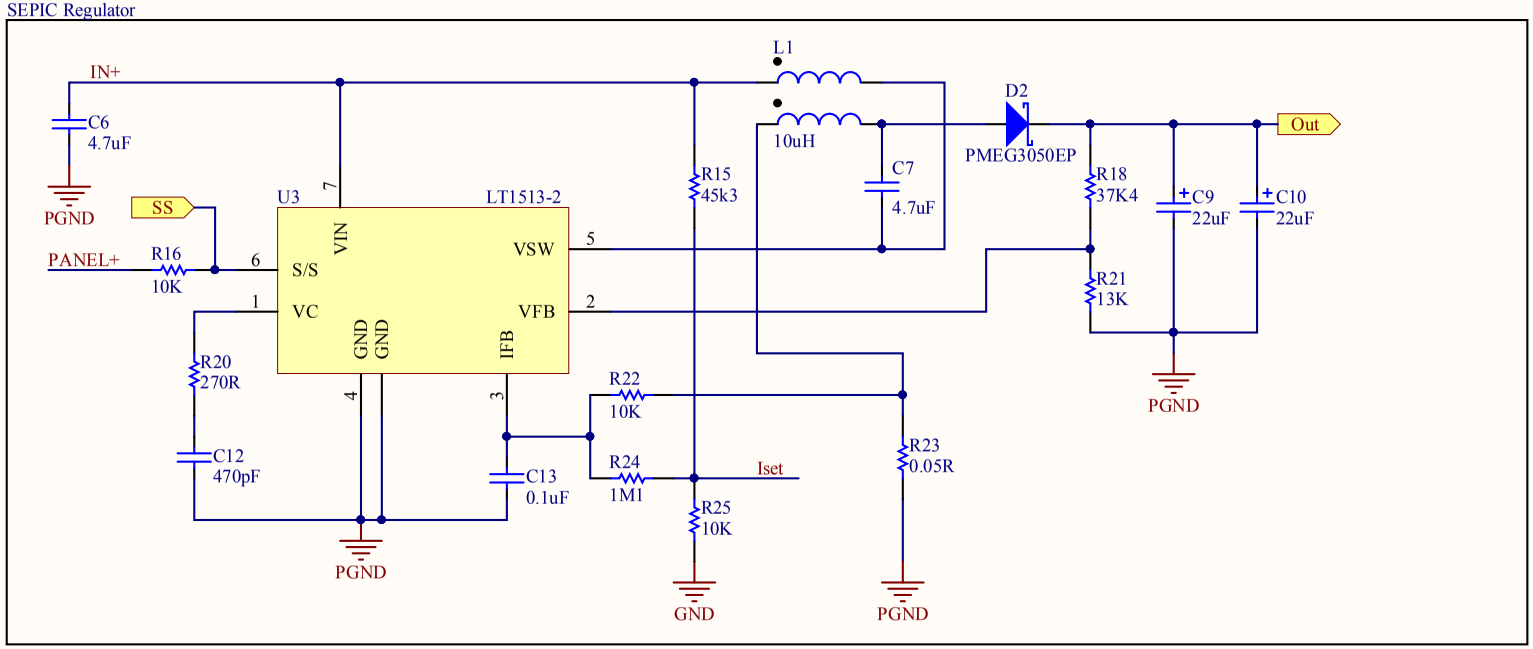
Input Current and Voltage Sensing



DAC



SEPIC Regulator



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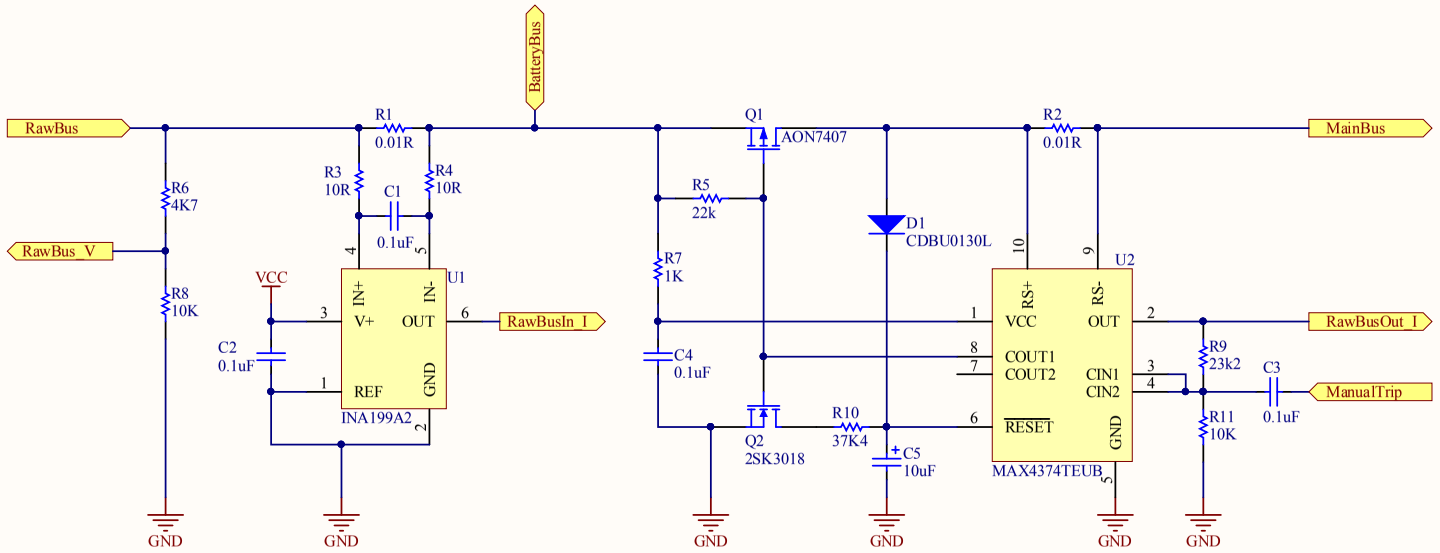

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EPS Bus Current Monitor a Protection		
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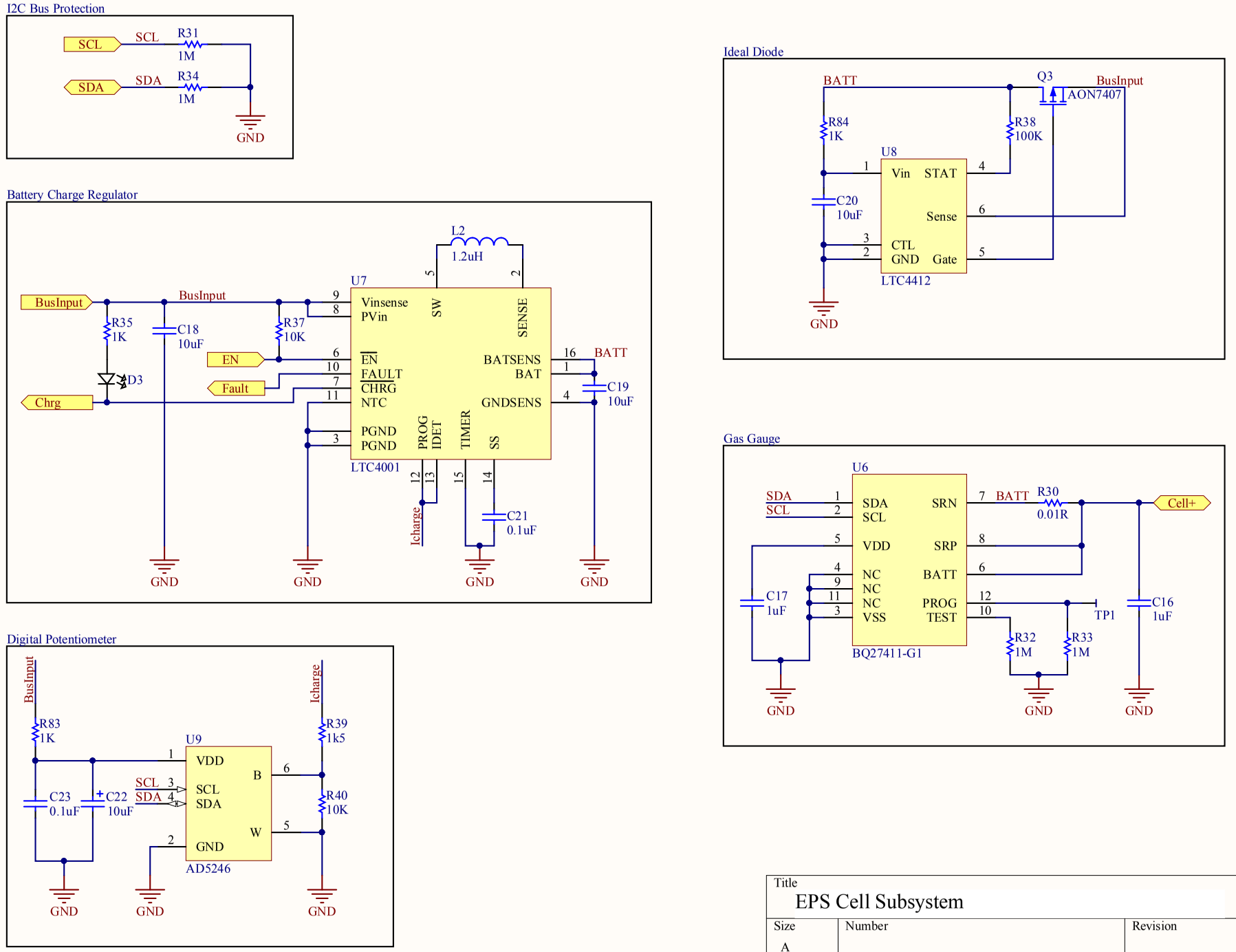
I2C Bus Protection
SCL
SDA
R31
1M
R34
1M
GND
Battery Charge Regulator
L2
1.2uH
U7
BusInput
R35
1K
C18
10uF
R37
10K
EN
Fault
Chrg
D3
Vinsense
PVin
SW
SENSE
EN
FAULT
CHRG
NTC
BATSENS
BAT
GNDSENS
PGND
PGND
PROG
IDET
TIMER
SS
LTC4001
BATT
C19
10uF
C21
0.1uF
Icharge
Digital Potentiometer
R83
1K
U9
VDD
SCL
SDA
GND
B
W
AD5246
C23
0.1uF
C22
10uF
R39
1k5
R40
10K
Ideal Diode
BATT
Q3
AON7407
BusInput
R84
1K
R38
100K
U8
Vin
STAT
Sense
CTL
GND
Gate
LTC4412
C20
10uF
Gas Gauge
U6
SDA
SCL
VDD
NC
NC
NC
VSS
SRN
SRP
BATT
PROG
TEST
BQ27411-G1
R30
0.01R
Cell+
C17
1uF
C16
1uF
TP1
R32
1M
R33
1M
Title
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A
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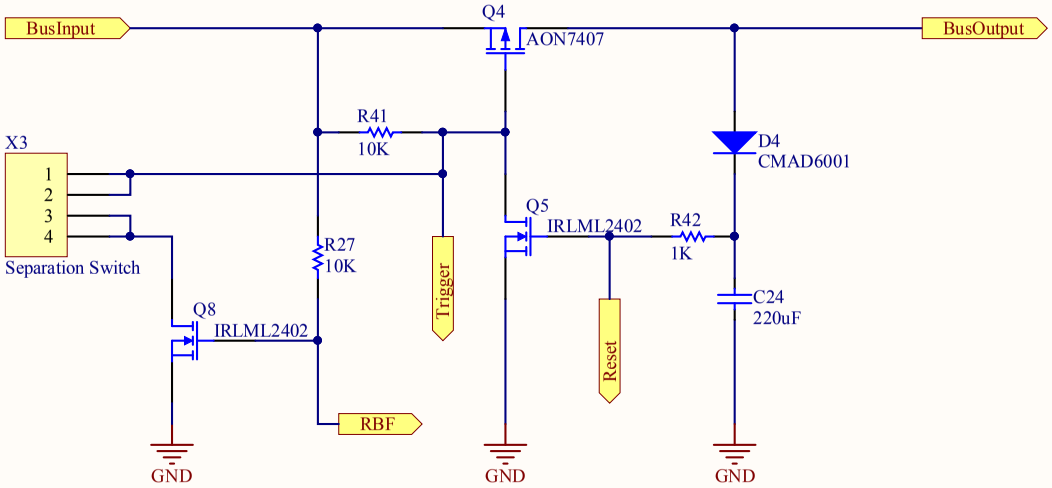

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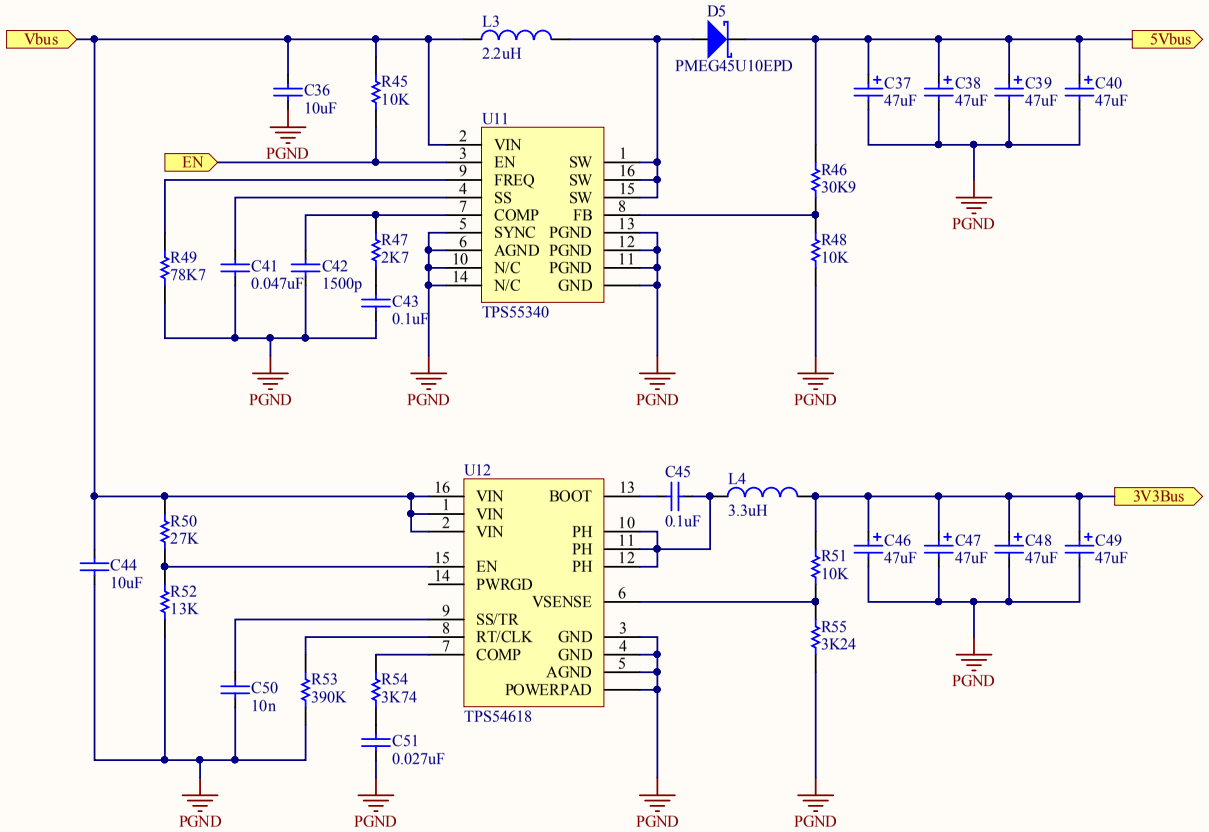

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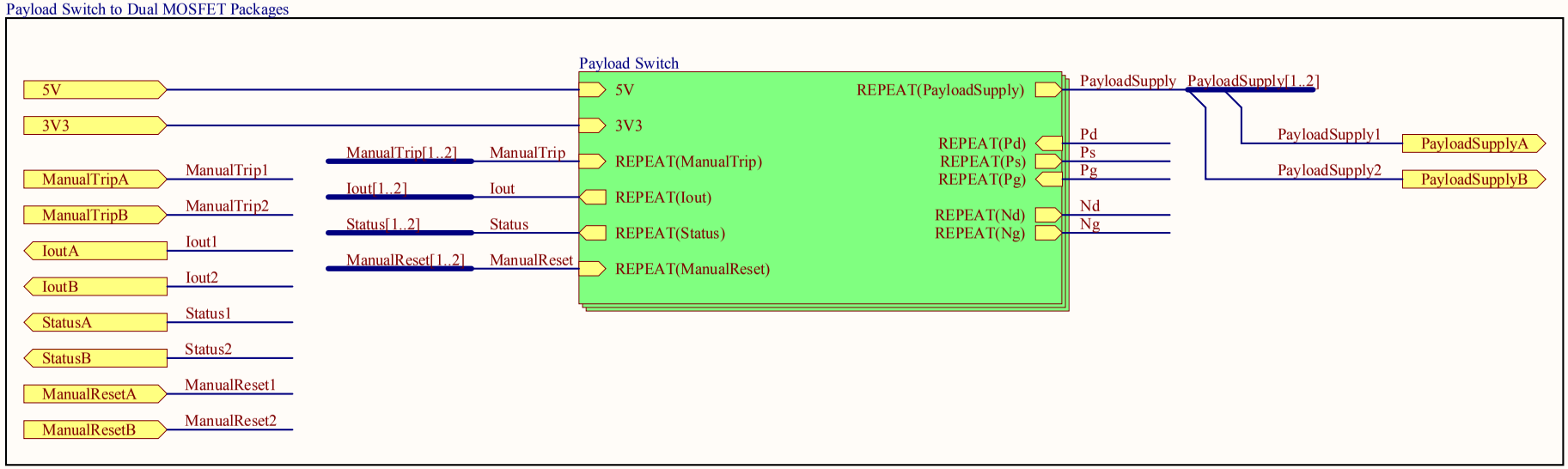
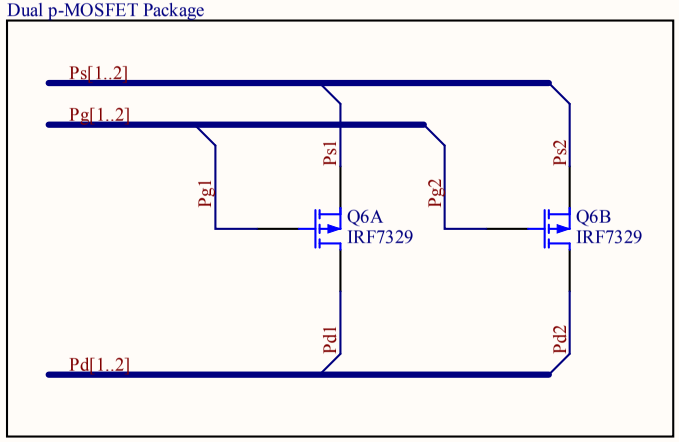
File: C:\Users\..\Regulators.SchDoc		Drawn By:

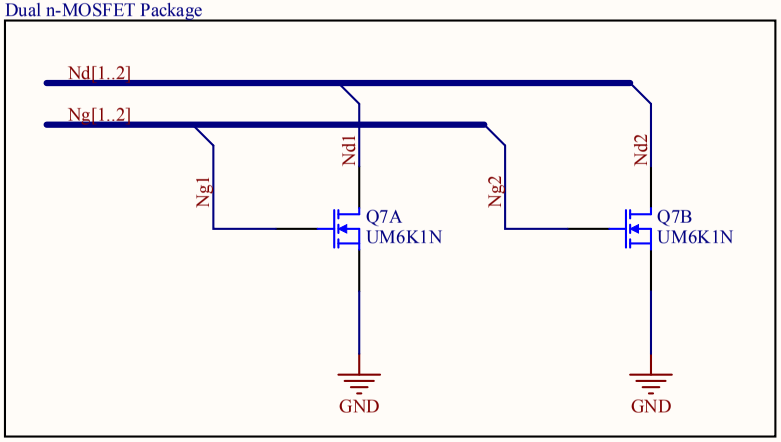
Payload Switch to Dual MOSFET Packages



Dual p-MOSFET Package

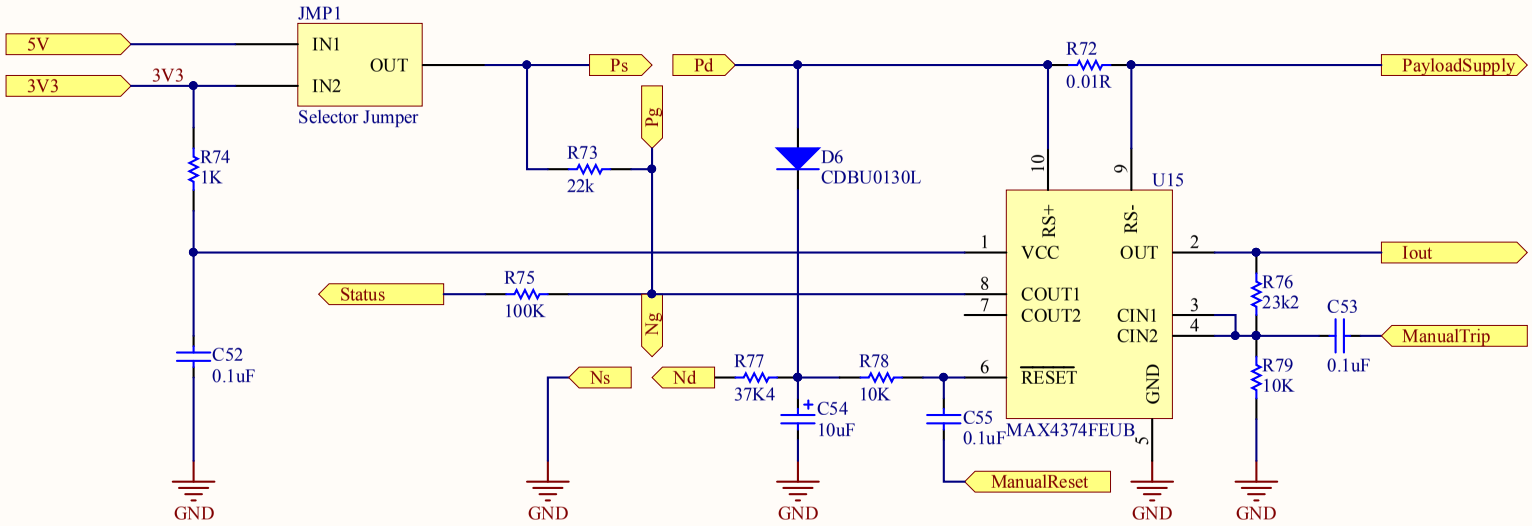


Dual n-MOSFET Package

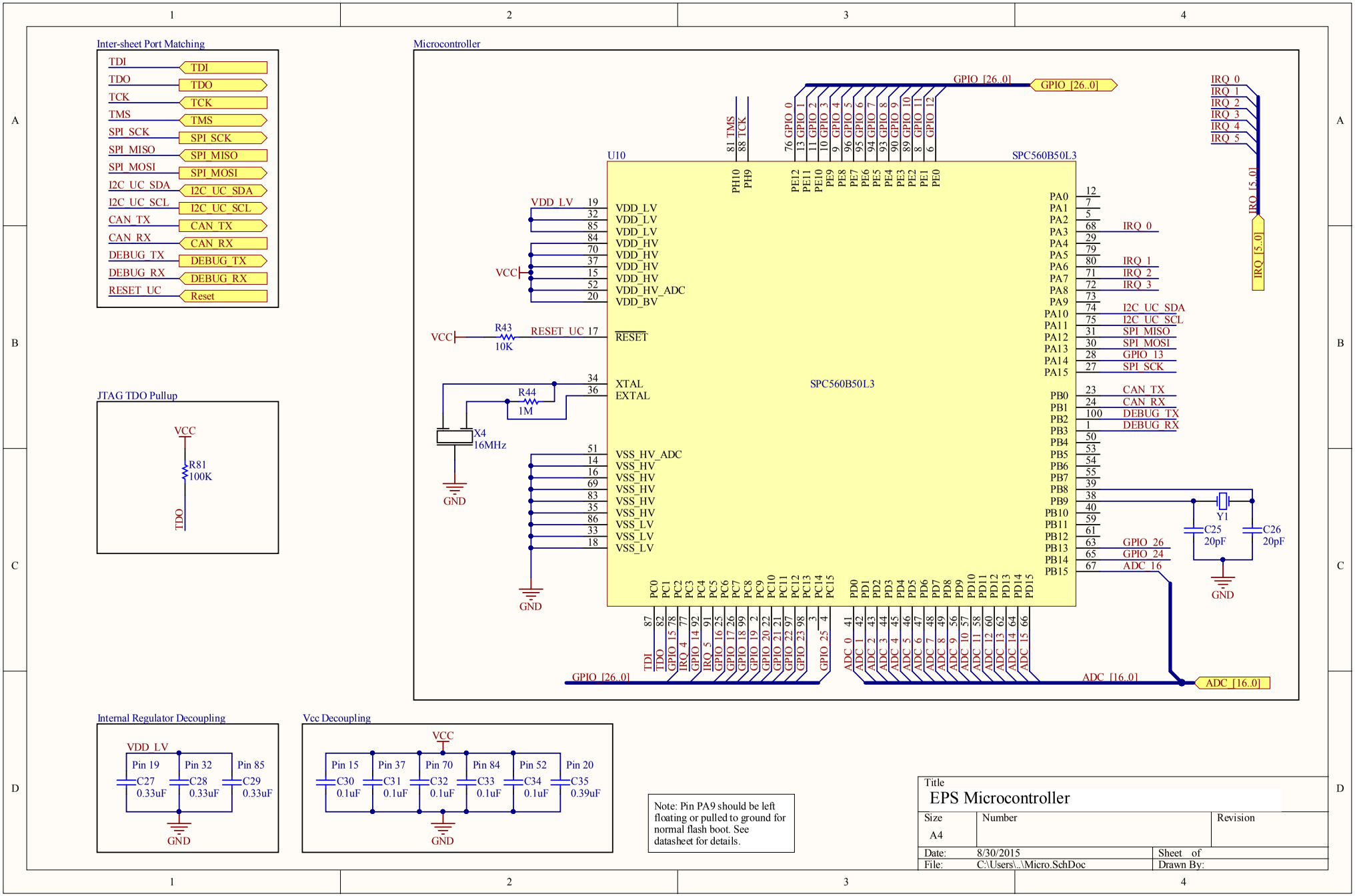


This schematic serves to link two payload switches to the dual-channel MOSFET packages.

Title: EPS Dual Switch Linking		
Size: A	Number	Revision
Date: 8/30/2015		Sheet of
File: C:\Users\..\DualPayloadControl.SchDoc		Drawn By:



Title: EPS Payload Switch		
Size: A	Number:	Revision:
Date: 8/30/2015		Sheet of
File: C:\Users\..\PayloadControl.SchDoc		Drawn By:

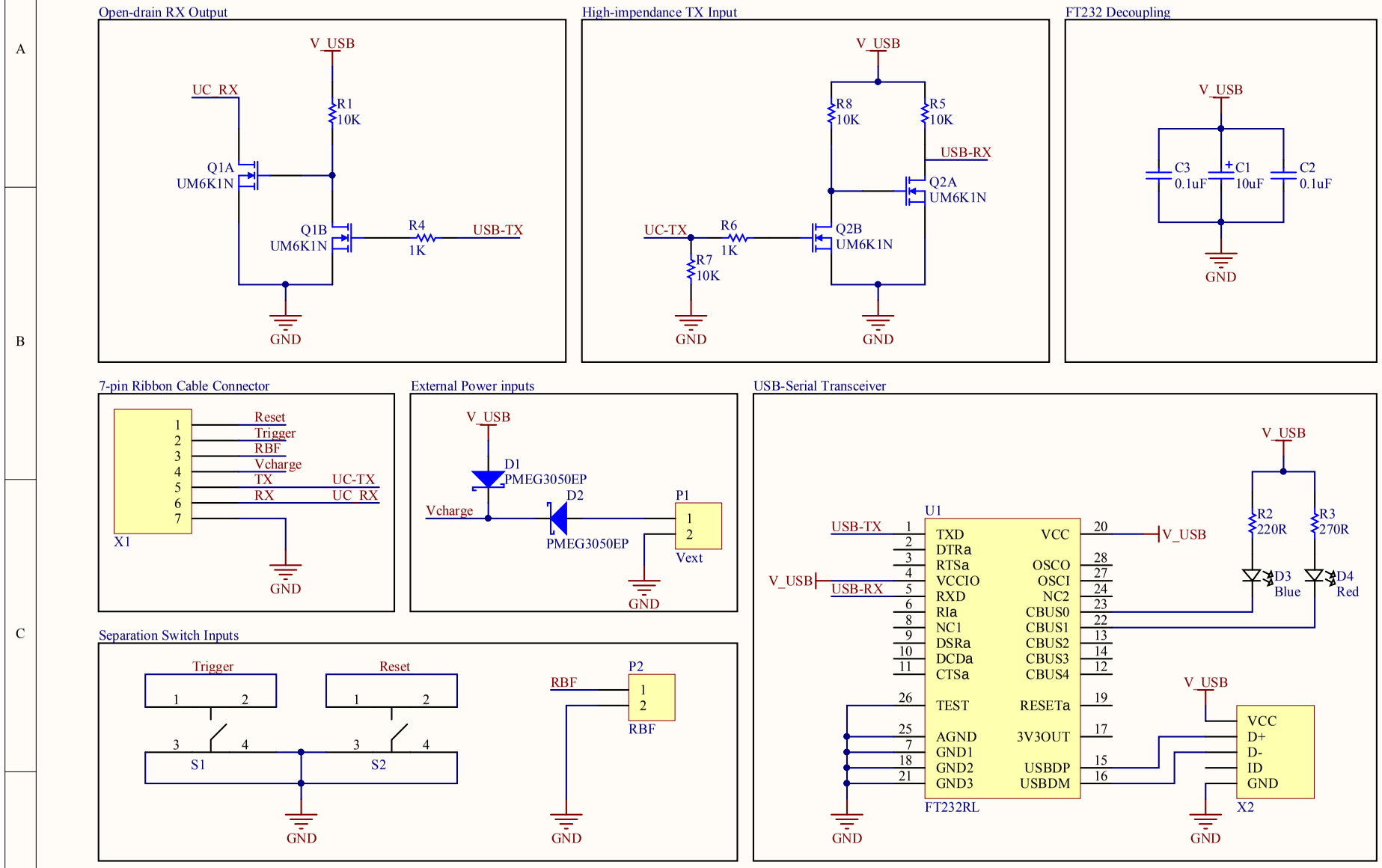

Inter-sheet Port Matching
TDI
TDO
TCK
TMS
SPI_SCK
SPI_MISO
SPI_MOSI
I2C_UC_SDA
I2C_UC_SCL
CAN_TX
CAN_RX
DEBUG_TX
DEBUG_RX
RESET_UC
Reset
JTAG TDO Pullup
VCC
R81
100K
TDO
Microcontroller
U10
SPC560B50L3
GPIO_[26..0]
IRQ_0
IRQ_1
IRQ_2
IRQ_3
IRQ_4
IRQ_5
IRQ_[5..0]
VDD_LV
VDD_HV
VDD_HV_ADC
VDD_BV
VCC
R43
10K
RESET_UC
RESET
R44
1M
X4
16MHz
XTAL
EXTAL
VSS_HV_ADC
VSS_HV
VSS_LV
GND
I2C_UC_SDA
I2C_UC_SCL
SPI_MISO
SPI_MOSI
GPIO_13
SPI_SCK
CAN_TX
CAN_RX
DEBUG_TX
DEBUG_RX
GPIO_26
GPIO_24
ADC_16
Y1
C25
20pF
C26
20pF
ADC_[16..0]
Internal Regulator Decoupling
VDD_LV
Pin 19
Pin 32
Pin 85
C27
0.33uF
C28
0.33uF
C29
0.33uF
Vcc Decoupling
Pin 15
Pin 37
Pin 70
Pin 84
Pin 52
Pin 20
C30
0.1uF
C31
0.1uF
C32
0.1uF
C33
0.1uF
C34
0.1uF
C35
0.39uF
Note: Pin PA9 should be left floating or pulled to ground for normal flash boot. See datasheet for details.
Title
EPS Microcontroller
Size
A4
Number
Revision
Date:
8/30/2015
Sheet of
File:
C:\Users\..\Micro.SchDoc
Drawn By:

D.2 Flight Preparation Controller

The following schematic is of the first iteration of the Flight Preparation Controller. Its schematic design has not been referred to in the text as it implements a simple USB-serial transceiver with a few physical switches and headers for separation switch functionality.

It makes use of two non-inverting MOSFET input and output drivers to ensure power cannot be transferred to the target module when connected.

Design files can be found in the supporting material under the `PCBs/FlightPrepRev0` folder.



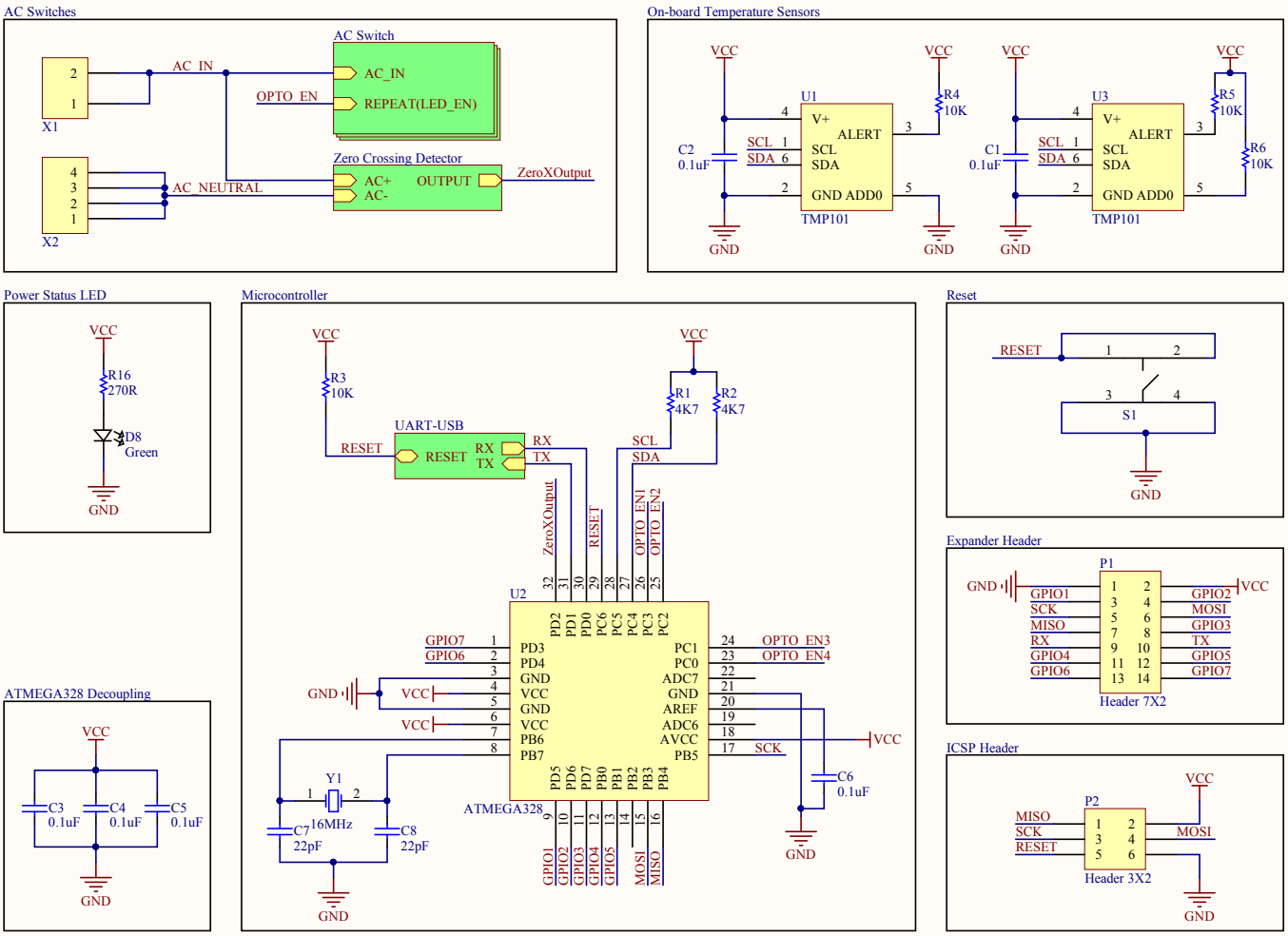
Title	EPS Flight Prep. Controller	
Size: A	Number:	Revision:
Date: 8/24/2015		Sheet of
File: C:\Users\..\FlightPrep.SchDoc		Drawn By:

D.3 AC Dimmer Board

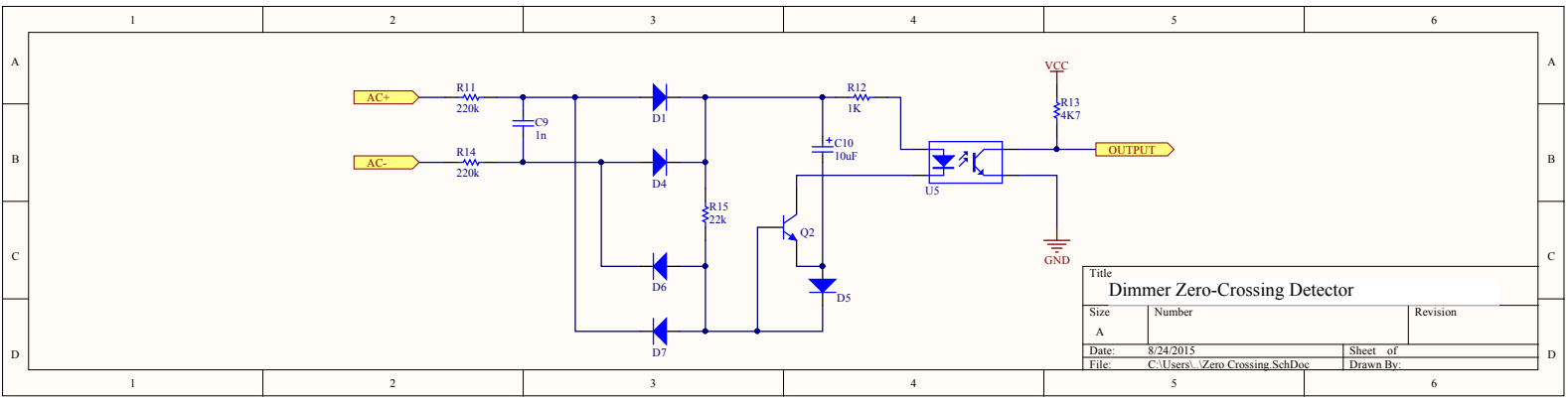
As described in Appendix C, an AC dimmer board was designed to allow automatic control of irradiance conditions within the light box. Its schematic design has not been discussed as it is not central to this work, but is included here for reference.

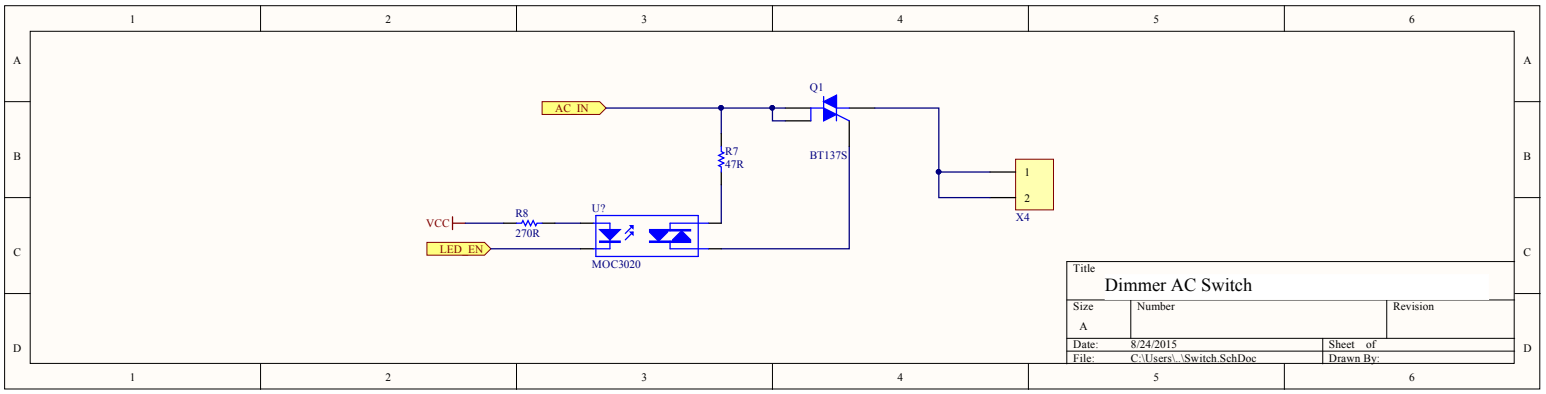
The board makes use of four TRIAC switches that are interfaced to the microcontroller via optocouplers. A zero-crossing detector allows the microcontroller software to accurately switch the AC waveform to a set percentage-power output.

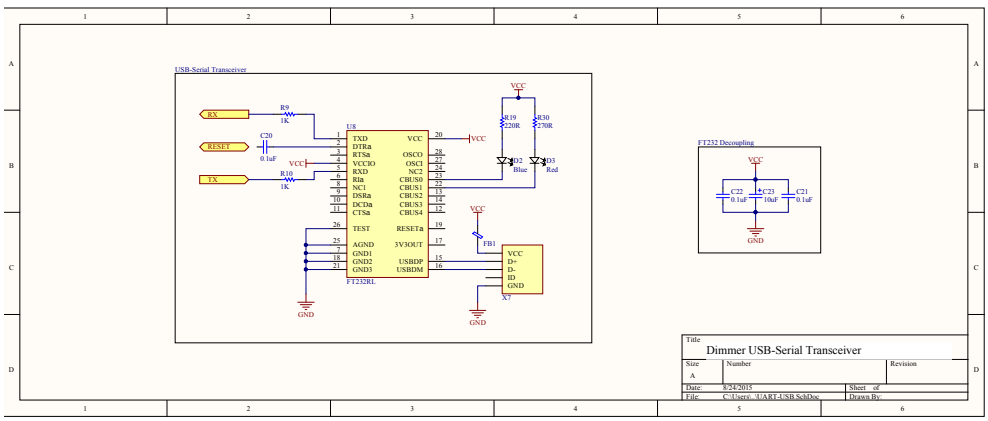
Design files can be found in the supporting material under the `PCBs/Dimmer` folder.



Title	Dimmer Top Level	
Size: A	Number:	Revision:
Date: 8/24/2015		Sheet of
File: C:\Users\..\Dimmer.SchDoc		Drawn By:


AC+
AC-
R11
220k
R14
220k
C9
1n
D1
D4
D6
D7
R12
1K
C10
10uF
R15
22k
Q2
D5
VCC
R13
4K7
U5
OUTPUT
GND
Title
Dimmer Zero-Crossing Detector
Size
A
Number
Revision
Date: 8/24/2015
Sheet of
File: C:\Users\..\Zero Crossing.SchDoc
Drawn By:


AC_IN
Q1
BT137S
R7
47R
1
2
X4
VCC
R8
270R
U?
LED_EN
MOC3020
Title
Dimmer AC Switch
Size
A
Number
Revision
Date: 8/24/2015
Sheet of
File: C:\Users\..\Switch.SchDoc
Drawn By:


USB-Serial Transceiver
RX
TX
RESET
R9
1K
R10
1K
C20
0.1uF
U8
TXD
DTRa
RTSa
VCCIO
RXD
RIa
NC1
DSRa
DCDa
CTSa
TEST
AGND
GND1
GND2
GND3
VCC
OSCO
OSCI
NC2
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
RESETa
3V3OUT
USBDP
USBDM
FT232RL
R19
220R
R30
270R
D2
Blue
D3
Red
FB1
X7
GND
FT232 Decoupling
C22
0.1uF
C23
10uF
C21
0.1uF
Title
Dimmer USB-Serial Transceiver
Size
A
Number
Revision
Date: 8/24/2015
Sheet of
File: C:\Users\...\UART-USB.SchDoc
Drawn By:

Appendix E

Development Toolchain

The following appendix briefly describes the use of the development board for programming and debugging, as well as the software toolchain used during development.

E.1 Development Board

The SPC560B50L3 microcontroller is programmed and debugged using a JTAG interface that is accessed via the 11-pin JTAG / Debug connector. A ribbon cable is currently used to link this connector to the JTAG port on the SPC560B-DIS development board that further provides a USB-serial interface.

3.3 V operation must be configured to ensure no damage is done to the target, and can be accomplished by removing jumper switches S1 and S2, and bridging solder jumpers J19 and J20. Furthermore, inductor L103 should be removed.

To access the serial interface on the JTAG header, physical wires need to be used to link pin 5 of U111 to R112 (with the resistor removed and connection made to the pad with the electrical connection to the header), and a similar wire used to link pin 4 of U110 to R111.

Pin-to-pin connections between the EPS's JTAG / Debug port and the development board's JTAG header are as follows:

EPS Port	Function	Dev. Board Header
1	$V_{external}$	11
2	$V_{external}$	11
3	GND	2, 4, 6, 12
4	GND	2, 4, 6, 12
5	TCK	5
6	TDI	1
7	TDO	3
8	TMS	10
9	TX	7
10	RX	8
11	RESET	9

E.2 Toolchain

The Eclipse-based SPC5Studio was used to develop the application software, with PLS's Universal Debug Engine Visual Platform used to upload the application to the target.

A PLS JTAG programmer is included on the development board with the jumper configurations, described previously, allowing this programmer to communicate with external targets. It should be noted that without a full license, this programmer has a 128-KB code size limit. The current software application has an upload size of approximately 35 KB.

Appendix F

Ethics Form

The following page contains the EBE Faculty 'Assessment of Ethics in Research Projects' form.

EBE Faculty: Assessment of Ethics in Research Projects

Any person planning to undertake research in the Faculty of Engineering and the Built Environment at the University of Cape Town is required to complete this form before collecting or analysing data. When completed it should be submitted to the supervisor (where applicable) and from there to the Head of Department. If any of the questions below have been answered YES, and the applicant is NOT a fourth year student, the Head should forward this form for approval by the Faculty EIR committee: submit to Ms Zakiya Chikte (**Zakiya.chikte@uct.ac.za)**; New EBE Building, Ph 021 650 5739). Students must include a copy of the completed form with the dissertation/thesis when it is submitted for examination.

Name of Principal Researcher/Student: **Ben Sheard** Department: **Electrical Engineering**

If a Student: Degree: **MSc (Electrical Engineering)** Supervisor: **Samuel Ginsberg**

If a Research Contract indicate source of funding/sponsorship: **n/a**

Research Project Title: **An Electrical Power System for CubeSats**

Overview of ethics issues in your research project:

Question 1: Is there a possibility that your research could cause harm to a third party (i.e. a person not involved in your project)?	YES	NO X
Question 2: Is your research making use of human subjects as sources of data? If your answer is YES, please complete Addendum 2.	YES	NO X
Question 3: Does your research involve the participation of or provision of services to communities? If your answer is YES, please complete Addendum 3.	YES	NO X
Question 4: If your research is sponsored, is there any potential for conflicts of interest? If your answer is YES, please complete Addendum 4.	YES	NO X

If you have answered YES to any of the above questions, please append a copy of your research proposal, as well as any interview schedules or questionnaires (Addendum 1) and please complete further addenda as appropriate.

I hereby undertake to carry out my research in such a way that

- there is no apparent legal objection to the nature or the method of research; and
- the research will not compromise staff or students or the other responsibilities of the University;
- the stated objective will be achieved, and the findings will have a high degree of validity;
- limitations and alternative interpretations will be considered;
- the findings could be subject to peer review and publicly available; and
- I will comply with the conventions of copyright and avoid any practice that would constitute plagiarism.

Signed by:

	Full name and signature	Date
Principal Researcher/Student:	**Benjamin Sheard**	

This application is approved by:

Supervisor (if applicable):	**Samuel Ginsberg**	
HOD (or delegated nominee): Final authority for all assessments with NO to all questions and for all undergraduate research.		
Chair : Faculty EIR Committee For applicants other than undergraduate students who have answered YES to any of the above questions.		