University of Cape Town

Doctoral Thesis

Fully printed transistors employing silicon nanoparticles

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Abstract

A new device, which utilises a previously unknown two-way mode of current switching, has been developed. This is the current switching transistor, a three-terminal electronic device which exhibits a transfer resistance, in which the application of a potential or injection of charge to one terminal controls the current at either of the two remaining terminals. The development of the current switching transistor arose from a more general project focussed on printed electronics using nanoparticulate silicon, with the aim of producing fully printed transistors. All of the printed transistors produced to date have been field-effect transistors (FETs), due to the fact that printing processes are easily applicable to the planar FET architectures. The majority of the work in the area of printed FETs has so far been focussed on the use of organic semiconducting polymers to produce organic field-effect transistors (OFETs). However, research has also been undertaken regarding the use of inorganic semiconductors, including for example, transparent metal oxides, compound semiconductors and silicon. Of the active devices, the key element is the transistor. It is essential, especially for its function as an electronic switch, in enabling a wide variety of technologies. Of particular interest are its applications in digital electronics, including logic gates, memory and comparators. The ultimate goal of printed electronics is to replace conventional electronic components with their printed equivalents, which requires the use of functional inks to deliver the desired electronic properties. Printed electronic components have potential advantages over conventional discrete and integrated circuits, especially in applications in which the printed electronics form factor is more important than the absolute technical performance of the system. Furthermore, the processes of fabrication of printed devices are far simpler and more cost efficient than those of conventional devices. This is particularly true for the current switching transistor, which can be realised by a simple two layer print.

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Chapter 1

Introduction

Printed electronics is concerned with the creation of electrical and electronic devices by the application of conventional printing techniques. This has received much interest in the past few decades, owing to its promise to enable the production of large-area, flexible and conformable electronics at low cost [1, 2]. Printed electronic components have potential advantages over conventional discrete and integrated circuits, especially in applications in which the printed electronics form factor is more important than the absolute technical performance of the system [3]. Furthermore, the processes of fabrication of printed devices are far simpler and more cost efficient than those of conventional devices.

The ultimate goal of printed electronics is to replace conventional electronic components with their printed equivalents, which requires the use of functional inks to deliver the desired electronic properties. The essential characteristics of a functional ink are that it be compatible with the printing process, that the resulting printed layer have the required electrical characteristics and, equally important, that the printed layer be compatible with the other materials forming the device or circuit which may also be printed. The balancing of these requirements has been the main challenge in the development of printed electronics. There is already a long history of functional inks for printing passive devices, beginning with conducting inks, such as those based on silver [4] or graphene [5], as well as in-

sulators and resistive inks, usually based on carbon [6]. Further developments of printed components have included the printing of reactive devices, such as inductors [7] in which conducting inks are printed in a particular pattern to optimise the inductance, as well as capacitors [8], in which conducting and dielectric inks are combined to form a multilayer functional printed device. This work has been crucial in the advancement of printed electronics. However, a full realisation of the potential of this emerging field will require the further development of printed *active* devices.

Of the active devices, the key element is the transistor. It is essential, especially for its function as an electronic switch, in enabling a wide variety of technologies. Of particular interest are its applications in digital electronics, including logic gates [9], memory [10] and comparators [11]. All of the printed transistors produced to date have been field-effect transistors (FETs) [12], due to the fact that printing processes are easily applicable to the planar FET architectures. Conversely, the production of a junction transistor [13], such as a bipolar junction transistor (BJT), requires the formation of a p-n junction, in which semiconducting regions of p- and n-type conductivity are in near-atomic contact. This is currently not achievable by printing, but rather it requires the use of other methods such as junction growth, alloying or diffusion [14]. The majority of the work in the area of printed FETs has so far been focussed on the use of organic semiconducting polymers to produce organic field-effect transistors (OFETs) [15]. However, research has also been undertaken regarding the use of inorganic semiconductors, including for example, transparent metal oxides [16], compound semiconductors and silicon [17].

Silicon is the ubiquitous semiconductor in modern electronics, and consequently it has the most well understood electronic system. As an indirect band gap material, it is far better suited to electronic applications than optical ones. However, it is still the most common semiconductor used in photovoltaics [18]. Finally, as the second most abundant element on Earth, it remains relatively inexpensive. Therefore, the focus of the research presented in this thesis has been on the application of silicon, and in particular, nanoparticulate silicon, to the fabrication of fully

printed transistors. In the course of this work, printed silicon-based insulated-gate field-effect transistors (IGFETs) were produced. An analysis of the performance characteristics of the IGFETs indicated the presence of a previously unknown switching behaviour. Further investigation led to the development of a new class of transistor, herein named the current switching transistor (CST). The CST differs fundamentally from traditional transistors, in terms of both functionality and the physical principles of their operation. Traditional transistor functionality includes one-way switching as well as amplification, in which the current between two terminals may be controlled by charge injection or application of a potential to a third terminal. This relies on the influence of induced internal electric fields to modulate the current in a semiconducting channel. The CST, in contrast, functions as an electrically controlled two-way switch, analogous to an electromechanical single pole double throw (SPDT) switch. This two-way mode of current switching enables the direction of current through the device to be changed, from between one pair of terminals to between another pair of terminals, by modifying the potential at, or current through, the common terminal of the two pairs. This functionality depends on activated charge transport within the semiconductor, which results in a nonlinear dependence of the current between two terminals on the difference in their electric potentials. Although it was research focussed on printed electronics which resulted in the development of the CST, it will be shown that this switching behaviour may also be realised in non-printed devices, provided the required nonlinearity of the current-voltage characteristics of the conduction paths between the terminals is present.

Chapter 2 will include relevant background information on conventional transistors and printed electronics, with a particular focus on printed silicon. The experimental methods employed in this work, as well as preliminary results related to the characterisation of printed layers, will be discussed in chapter 3. The designs of the printed transistors developed in this work will be presented in chapter 4. The results of the electrical characterisation of the printed transistors are presented in chapter 5. Chapter 6 includes a detailed analysis of the results of the electrical characterisation as well as the proposal and testing of a theoretical model for

the switching behaviour exhibited by the CST. Finally, conclusions are drawn in chapter 7.

Chapter 2

Background

The research presented in this thesis is focussed on the development of printed silicon transistors. The purpose of this chapter is to set the work into context by providing pertinent background information. Here, the transistor will be introduced and the mechanisms responsible for its operation explained, after which conventional methods of transistor fabrication will be described. The final section will introduce the field of printed electronics with a particular focus on its application to the fabrication of transistors.

2.1 The transistor

The advent of the transistor revolutionised industrial and consumer electronics in the 20$^{\text{th}}$ century [19]. Although Lilienfeld invented the concept of the field-effect transistor in 1925 and patented it in 1927 [20], it was not until 1948 that Bardeen, Brattain and Shockley produced the first practical transistors at Bell Labs [21,22], for which they were jointly awarded the 1956 Nobel Prize in Physics [23–25]. Originally developed as signal amplifiers to replace the thermionic triode vacuum tube [26], transistors began to be used as electrically driven switches in digital computers by the mid 1950s [27,28]. Switching remains their main use today, with

applications in computer logic [19] and driving displays [29], among others. The remainder of this section will be devoted to a description of transistors, in terms of the physical principles governing their operation, as well as their methods of production.

2.1.1 Transistor functionality

In general terms, a transistor is a three-terminal electronic device which exhibits a transfer resistance. There are to date two classes of transistors used in applications: junction transistors [22] and field-effect transistors [12].

Junction transistors

A bipolar junction transistor (BJT), named for the fact that its operation relies on both majority and minority charge carriers, consists of two coupled p-n junctions, constructed from three semiconducting layers of alternating type. There are two types of BJT. These are the PNP, in which a common n-type region is sandwiched between two p-type regions, and the NPN, in which two n-type regions surround a common p-type region. It is sufficient to consider only one of these types to develop an understanding of the BJT and therefore, the following explanation will be confined to the PNP type.

To begin the construction of an idealised model PNP, consider a forward-biased p^+-n junction, where + signifies that the p-type region is much more highly doped than the n-type region. A reverse-biased p-n junction, which has similar doping levels in its two regions, is coupled to the p^+-n junction, such that they share a common n-type region. Figure 2.1 shows the structure of the PNP BJT, including the externally applied biases. The p-type region of the forward-biased junction is named the emitter, while the n-type region and p-type region of the reverse-biased junction are the base and collector respectively.

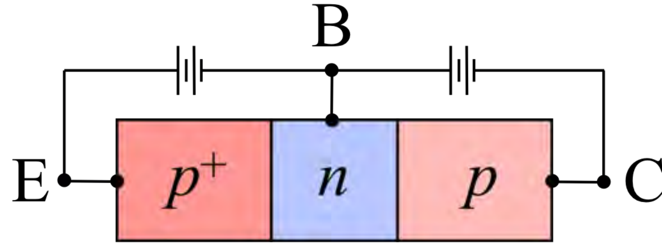


Figure 2.1: *Schematic of PNP type BJT. The electrical contacts to the emitter, base and collector regions are labeled E, B and C respectively.*

In the vicinity of a p-n junction, a *depletion region* is formed which is devoid of free charge carriers. The formation of the depletion region occurs by diffusion of electrons from the n-region to the p-region and of holes from the p-region to the n-region, as illustrated in Figure 2.2a, followed by the recombination of diffused electrons with holes in the p-region and likewise for diffused holes in the n-region. The recombination process leaves behind fixed charged ion cores which cause an electric field directed from the n-region into the p-region, as shown in Figure 2.2b. A forward-biased junction, with p biased positive and n biased negative, will have a narrower depletion region and a reduced electric field, while the opposite is true for a reverse-biased junction with p biased negative and n biased positive.

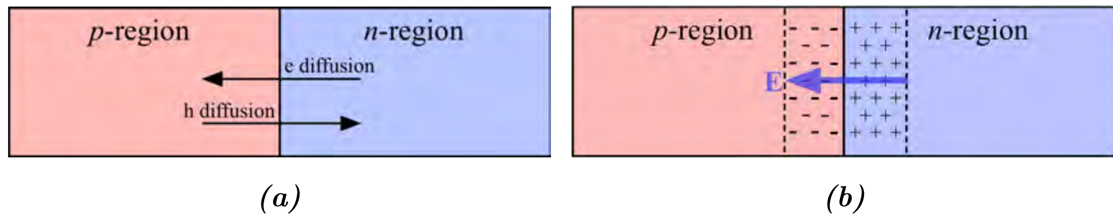


Figure 2.2: *Formation of a depletion region. (a) Electrons and holes diffuse from regions of high concentration to regions of low concentration. (b) Diffused carriers recombine with carriers of opposite charge, resulting in fixed charged ions and an electric field pointing from the n-region to the p-region.*

In the BJT, the applied bias voltage influences the energy barriers to charge transport within the transistor. This is illustrated in Figure 2.3, which shows the band

structure of the PNP for the (a) unbiased and (b) biased cases. The valence band is shaded in grey in each figure, with the conduction band represented by the upper solid line. The emitter, base and collector regions of the transistor are labelled E, B and C respectively, with the doping types indicated above the diagram. The forward bias applied to the emitter-base junction reduces the energy barrier to holes, which increases the rate of injection of minority holes into the base region. On the other hand, the reverse bias applied to the collector-base junction increases the energy barrier to holes diffusing into the base.

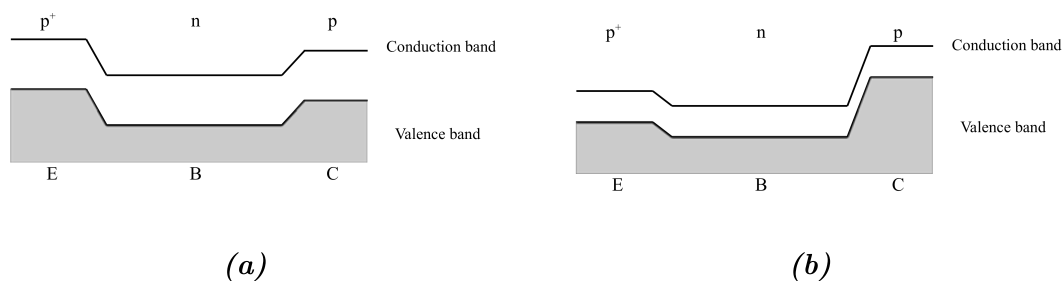


Figure 2.3: *Effect of bias voltages on a PNP transistor band diagram: (a) No bias voltages applied. (b) Emitter-base junction forward-biased and collector-base junction reverse-biased [30].*

To explain how the BJT functions as a current amplifier the charge flow within the transistor will now be examined. Figure 2.4a illustrates the individual carrier flows in the BJT, which may be grouped into the hole flows, shown in red, and the electron flows, shown in blue. Flow a represents holes injected into the base by the emitter. Flow b is due to those injected holes diffusing across the base region. Flow c represents holes moving from the base to the collector under the influence of the electric field within the depletion region of the collector-base junction. Flow d is due to injected holes recombining with majority electrons within the base. Flow e represents electrons moving from the external circuit into the base, which replace those electrons lost to recombination with the holes of flow d. Electrons injected from the base into the emitter, as well as their replacements from the external circuit, constitute flow f.

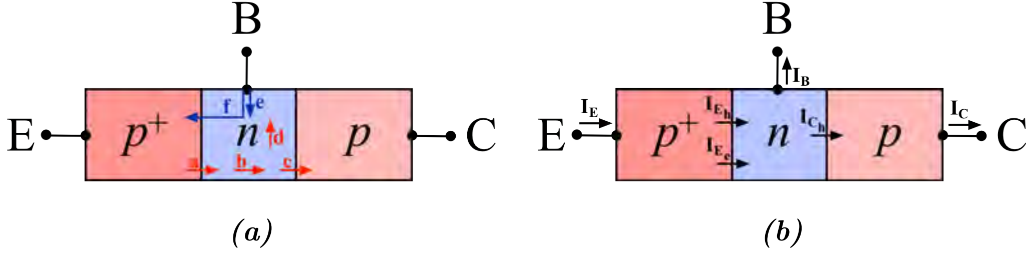


Figure 2.4: *(a) Carrier flows within the BJT. Hole flows are shown in red while electron flows are shown in blue. (b) Currents in the BJT (after [30]).*

Figure 2.4b illustrates the internal and external electrical currents in the BJT. By convention, the currents associated with the particle flows are in the flow direction for holes, opposite to the flow direction for electrons. Therefore, the emitter hole current I_{E_h} associated with flow a is in the same direction as the emitter electron current I_{E_e} associated with flow f, from the emitter to the base. Together, these two internal currents constitute the external emitter current, $I_E = I_{E_h} + I_{E_e}$. The external base current I_B is in the opposite direction of the electron flows e and f and the external collector current is equal to the collector hole current, $I_C = I_{C_h}$. The reverse collector current has been ignored in this description, which is justifiable by its small magnitude, compared to the forward collector hole current I_{C_h}, due to the forward bias applied to the collector-base junction.

The BJT functions as a current-controlled amplifier, in which the output current (at the collector) can be controlled by the input current (at the base). The collector current, which is a flow of holes across the base, is related to the base current, a flow of electrons into the base, because the base region is electrically neutral. An increase in the flow of electrons into the base will cause more holes to be injected from the emitter, maintaining base neutrality, which will then flow to the collector. Similarly, a decrease in the base current will cause a decrease in the emitter hole current and hence the collector current. In this way, the base current modulates the collector current. Furthermore, this relationship between the base and collector currents enables the switching functionality of the BJT. The emitter-

collector current may be switched on or off by sufficiently increasing or decreasing the base current.

Field-effect transistors

Whereas the junction transistor functions as a current-controlled device, the field-effect transistor is voltage-controlled. That is, the current between two terminals may be controlled by varying the voltage applied to a third terminal. There are several types of field-effect transistor, the simplest of which is the junction field-effect transistor (JFET). This device will be taken as the first example to explain the principle of FET operation, after which a second example, the insulated-gate field-effect transistor, will be discussed.

The structure of a JFET consists of two semiconducting regions of opposite doping type, in contact with one another such that the interface between them forms a p-n junction. One of these regions is lightly doped and connected to two terminals, called the source and drain. The other region is highly doped and connected to the third terminal, called the gate. All three contacts to the terminals are ohmic.

There are two types of JFET. These are the p-channel JFET, in which the source and drain are connected to the p-type region while the gate is connected to the n-type region, and the n-channel JFET, in which the source and drain are connected to the n-type region while the gate is connected to the p-type region. Once again, it is sufficient to consider only one of these and this explanation will be focussed on the n-channel JFET. Figure 2.5 shows schematically the structure of an n-channel JFET. The source and drain electrodes, labelled S and D respectively, are connected to the lightly doped n-type channel, which is shaded blue. The gate electrode, labelled G, is connected to the highly doped p^+-region, which is shaded red. There is formed a depletion region near the p^+-n junction, shaded grey in the figure. Due to the fact that the p^+-region is much more highly doped than the n-region, a smaller volume on the p^+ side of the junction will be equal but

opposite in charge to a larger volume on the n side and thus the depletion region of the the junction will be almost entirely on the n side.

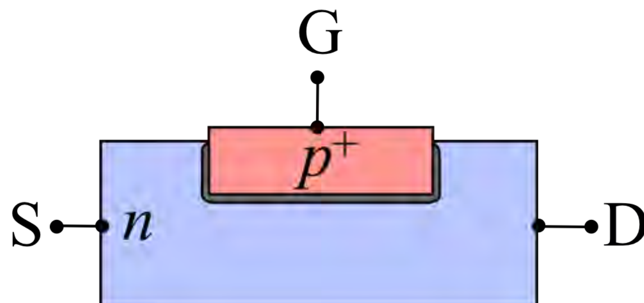


Figure 2.5: *Schematic representation of an unbiased n-channel JFET. The source, drain and gate are labeled S, D, G respectively. The depletion region is shaded grey.*

Figure 2.6a illustrates the effect of applying a potential difference, V_{DS}, to the drain relative to the source. If the value of V_{DS} is positive, so that the drain is at a higher potential than the source, then an electron current, I_{DS}, is caused in the channel from the drain to the source. The electric potential is not constant throughout the channel. Rather, it decreases continuously from the drain to the source, such that any point closer to the drain is at higher a potential than any point closer the source. As a result the reverse bias applied to the junction is larger near the drain and therefore the depletion region penetrates further into the channel at these locations, as shown in the figure. The wider depletion region effectively narrows the channel, which increases its electrical resistance, given by

$$R = \mathrm{d}V_{DS}/\mathrm{d}I_{DS}. \tag{2.1}$$

Figure 2.6b shows the drain-source current-voltage characteristic, I_{DS} vs V_{DS}, of the JFET for the case with zero potential difference, V_{GS}, applied to the gate relative to the source. For low values of V_{DS}, the widening depletion region has relatively little impact on the channel resistance, and therefore the gradient,

$$\mathrm{d}I_{DS}/\mathrm{d}V_{DS} = 1/R, \tag{2.2}$$

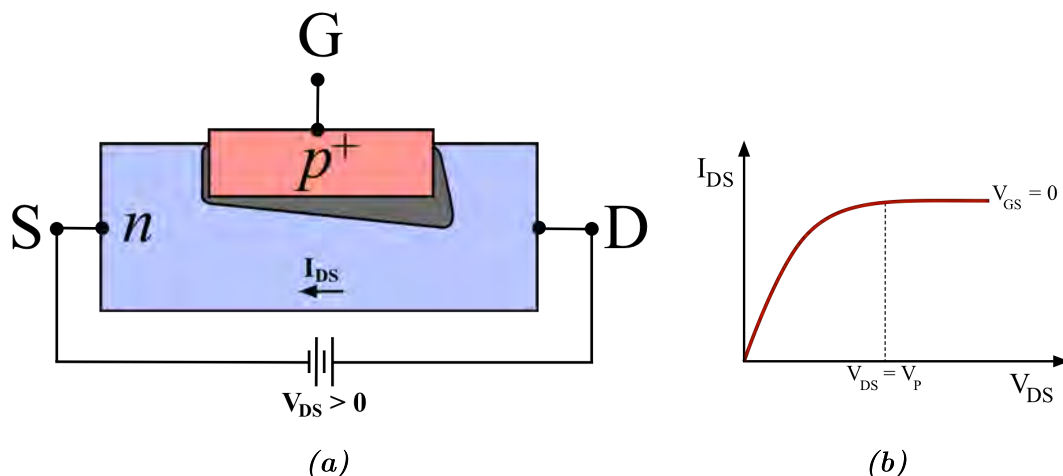


Figure 2.6: *Effect of a potential difference applied to the drain relative to the source. (a) A positive drain-source potential V_{DS} causes the depletion region to penetrate further into the channel near the drain; a current I_{DS} exists in the channel. (b) Drain-source current-voltage characteristic, I_{DS} vs V_{DS} for zero gate-source potential V_{GS}. Pinch-off occurs at $V_{DS} = V_P$ (after [30]).*

decreases slowly with increasing V_{DS}. As V_{DS} is further increased, the depletion region continues to widen until a state of quasi-equilibrium is established between the tendency of the increasing potential to enhance the current and that of the narrowing channel to reduce it. This event is known as *pinch-off*, because of the constriction of the channel, and it occurs at a drain-source potential $V_{DS} = V_P$. The drain-source current effectively saturates and additional increases in the drain-source potential have little to no effect on the current. The transistor is then said to be in saturation mode.

Figure 2.7a illustrates the effect of applying a reverse bias to the gate relative to the source. $V_{GS} < 0$, so that the gate is at a lower potential than the source. The asymmetry of the depletion layer, which results from the varying electric potential over the length of the channel, is still present. However, the reverse gate-source bias widens the entire depletion region, which reduces the current in the channel. Figure 2.7b shows typical JFET drain-source current-voltage characteristics for

increasing magnitudes of the reverse gate-source potential. Note that the values of V_{GS} are related by

$$0 > -V_1 > -V_2 > -V3. \tag{2.3}$$

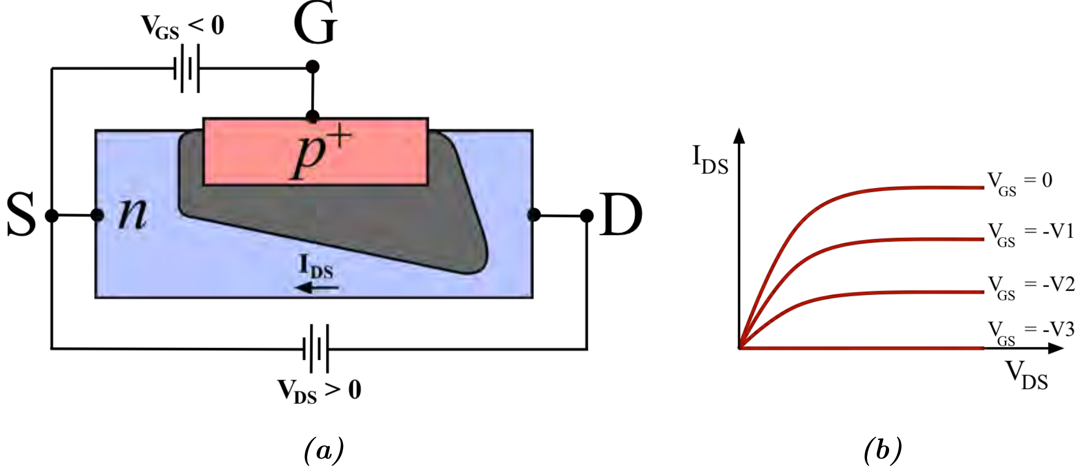


Figure 2.7: *Effect of a reverse bias applied to the gate relative to the source. (a) The depletion layer widens, reducing the current in the channel. (b) Drain-source current-voltage characteristic, I_{DS} vs V_{DS} for different values of the gate-source potential V_{GS} (after [30]).*

For any given value of the drain-source potential, V_{DS}, the current may be controlled by adjusting the value of the gate-source potential, V_{GS}. Decreasing the magnitude of V_{GS} increases the current and conversely, increasing the magnitude of V_{GS} reduces the current. If V_{GS} is made sufficiently negative, $V_{GS} = -V_3$, the conducting channel is completely constricted and the current is zero. In this way, the JFET functions as a voltage controlled amplifier and as a switch, whereby the drain-source current may be increased, decreased or switched off by adjusting the gate-source potential. The FET is a unipolar device because, unlike the BJT, it relies solely on majority carriers for conduction.

In the following section, the conventional methods of transistor fabrication will be discussed. However, it is first necessary to briefly highlight one important variant of the field-effect transistor, namely the insulated-gate field-effect transis-

tor (IGFET), which is important for two reasons. Firstly, it is by far the most commercially important transistor, in the form of the metal-oxide-semiconductor field-effect transistor (MOSFET) which is ubiquitous in modern electronics [31]. In the MOSFET structure an insulating oxide, typically silicon dioxide, is used as the gate insulator. Secondly, the present research has been partially focussed on the development of printed IGFETs. Figure 2.8 shows the structure of a typ-

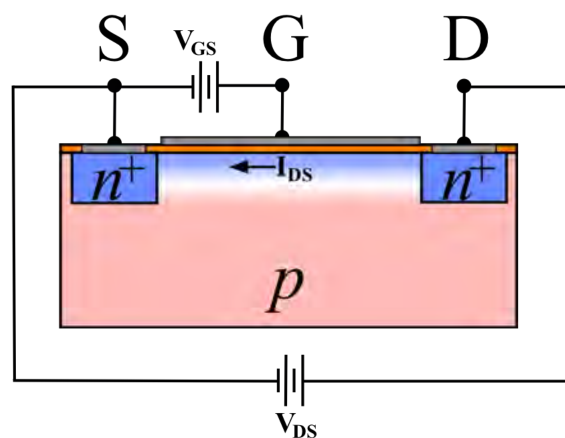


Figure 2.8: *Schematic representation of an IGFET and formation of the inversion layer. Source, drain and gate are labelled S, D and G respectively. Colour shading within the substrate indicates the carrier density: blue for electrons, pink for holes. The gate insulator is shaded orange and the metal contacts are grey.*

ical IGFET, consisting of a p-type semiconducting substrate, two highly doped n-type regions connected to the source and drain electrodes and a gate electrode which is electrically insulated from the substrate. By applying a positive potential to the gate relative to the source, holes within the substrate are repelled from the insulator-substrate interface and electrons are attracted to the interface. This creates an *inversion layer* below the interface, so named because it contains an excess of the opposite charge carriers with respect to the majority carriers in the substrate. In the figure, colour shading within the substrate represents the charge carrier density: pink for holes and blue for electrons. The white area between the inversion layer and the rest of the substrate is devoid of free carriers. The inversion layer is a conducting channel between the source and drain, and its conductance

can be controlled by the gate-source potential. Increasing V_{GS} attracts more electrons to the inversion layer, which allows more current between the source and drain for a given source-drain potential.

Both the JFET and the IGFET are essentially voltage-driven devices. However, within the JFET there is a small gate current, while in the IGFET there is ideally no gate current because of the gate insulator. In both devices, the conductance of a semiconducting channel is modulated, via the field effect, by the application of a gate potential. The main difference is that in the JFET the electric field is built-in to the depletion region associated with the *p*-*n* junction, whereas in the IGFET the electric fields are induced within the gate insulator as well as within the semiconductor, below the inversion layer.

2.1.2 Conventional transistor fabrication and architecture

Currently, billions of discrete transistors are produced each year for a variety of applications, but this pales in comparison to the production of transistors in integrated circuits (ICs). An IC is a set of circuit elements produced on a single piece of semiconducting material, typically a wafer of monocrystalline silicon. The advancement of semiconductor fabrication technology has enabled the production of progressively smaller devices and more highly integrated circuits, to the extent that modern ICs, such as microprocessors, commonly contain billions of individual transistors.

The fabrication of an integrated circuit on a silicon wafer is a complex, multi-step production process. The most prevalent semiconductor technology is complimentary metal-oxide-semiconductor (CMOS), in which the transistors are MOSFETs. Figure 2.9 shows the structure of a typical MOSFET. First, an epitaxial layer of silicon is grown on the wafer. For integrated circuits in which the half-pitch (half the distance between adjacent identical elements) is less than 250 nm, shallow trench isolation (STI) is used to prevent leakage current between devices [32]. The current standard technology has a half-pitch of 22 nm and that of the next technol-

ogy node will be 14 nm [33], therefore STI is typically required and will continue to increase in importance. Once the substrate is prepared, a gate dielectric, typically silicon dioxide is grown on the wafer by thermal oxidation. The device features are patterned subtractively by a combination of photolithography and chemical or plasma etching to form the required elements. Ion implantation followed by thermal processes such as rapid thermal annealing are used to adjust the doping of the source and drain regions.

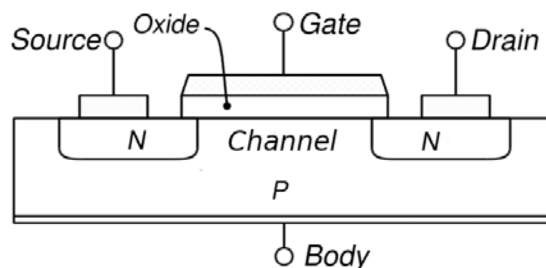


Figure 2.9: *Schematic representation showing the structure of a P-channel MOSFET (http://volga.yale.edu).*

2.2 Thin film transistors

Thin film transistors (TFTs) are a class of field-effect transistors in which the materials forming the electrodes, gate insulator and semiconducting layer are deposited on an insulating substrate. Traditionally the substrate is glass, but increasingly polymer film substrates are being used. The deposition process is typically chemical vapour deposition (CVD), so in principle there is no restriction on the substrate size. With the current generation 10 display technology the substrate size is 2.85 m $\times$ 3.05 m [34]. TFTs are therefore commonly used as pixel switches in video displays, a function enhanced by the use of transparent materials in their fabrication. These include transparent conductors such as indium tin oxide (ITO) and transparent semiconductors such as zinc oxide. Figure 2.10 illustrates the

structure of a typical TFT [35], shown here with microcrystalline silicon (μc-Si) as the semiconductor. After deposition of the layers, similar pattering techniques are required as for the MOSFET. The fundamental difference between the two is that in the MOSFET, the substrate forms part of the device, while in the TFT it does not.

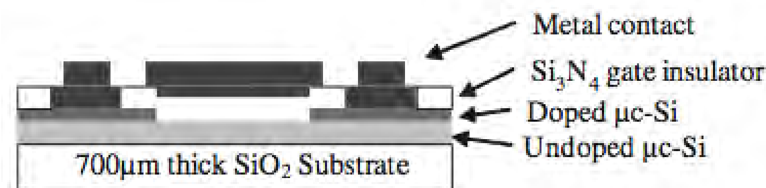


Figure 2.10: *Schematic representation of a μc-Si TFT [35].*

2.3 Printed electronics and printed transistors

Printed electronics refers to the application of conventional printing technologies to the production of electronic components and circuitry. This field has received much interest of late, which has been driven by the anticipation that it will enable high volume, low cost production of electronics, including flexible, conformable and large area devices [36]. The central concept of printed electronics is that conventional graphic inks are replaced by functional inks with specific electronic properties, which are deposited on substrates to form circuits using standard printing techniques.

A great variety of printing methods are applicable to the fabrication of electronic circuits [37], including rotogravure [38, 39], flexography [39] and offset lithography [40], as well as single substrate processes such as ink-jet [39,41] and screen printing [42]. The latter two processes have been adapted to roll-to-roll printing for high-volume production, but these adaptations are not their principal modes of use. The transistors produced in the course of carrying out the present research were printed using a standard single substrate screen printing method.

The production of electronic devices in this way is a fully additive process, which involves the printing of different layers of electronic materials in a specific order and layout to form the circuit elements. Development of functional inks began with materials for passive components. Inks containing, for example, silver [4] or copper [43], are used to print conducting traces. Resistive elements are typically printed with carbon inks. Dielectric, or insulating inks are used as protective encapsulants to isolate the printed devices electrically, mechanically and environmentally, and also to fabricate capacitors, in which a dielectric layer is printed between two conducting layers. Printed sensors currently represent a significant area of active research, with applications in sensing such diverse physical quantities as force [44], strain [45], humidity [46] and temperature [47], as well as chemically sensing the concentration of various gases [48].

However, the real potential of printed electronics lies in the possibility to print active components, and more specifically, transistors, the realisation of which requires the continuing development of printable semiconductors. The bulk of the prior work relating to printed semiconductors has been focussed on organic semiconducting polymers [43], which may be doped to the desired conductivity and applied, for example, to the fabrication of organic field-effect transistors (OFETs). Examples of organic polymers commonly used in OFETs include poly(3-hexylthiophene) (P3HT) [49] as well as polyacetylene, the discoverers of which were awarded the 2000 Nobel prize for Chemistry [50].

OFETs were initially fabricated using a coplanar structure [51], in which the gate was deposited on a substrate, followed by a thin layer of gate insulator and the source and drain electrodes. The three electrodes were thus in a co-planar arrangement, onto which the organic semiconductor would be deposited, typically by drop-casting or spin-coating. This was a convenient configuration for test structures, but as the OFETs developed they have moved to a higher performance opposed-gate structure [39], as illustrated in Figure 2.11, which is more similar to the conventional TFT architecture.

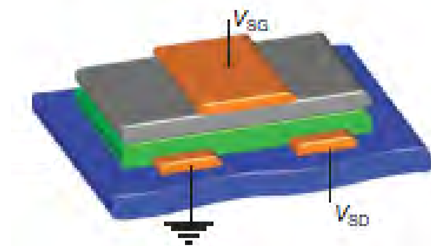


Figure 2.11: *Schematic representation of an OFET structure [39].*

In addition, several promising inorganic semiconductors have been used to fabricate FETs. These materials, in contrast with the liquid phase organic polymers, typically contain nano-scale solid constituents. Transparent metal oxides such as vanadium oxide and zinc oxide have been deposited by spin coating [52] and later by printing [53] to form FET structures. The use of silicon-based semiconducting inks in printed electronics has heretofore been less common than organic semiconductors. The use of silicon nanoparticles in printed electronics was demonstrated in 2006 [17], which has subsequently led to the development of printed negative temperature coefficient thermistors [47] as well as the printed silicon transistors presented here [54, 55]. Other applications for printed silicon have also emerged in recent years, such as the use of silicon nanoparticle inks in dopants for selective emitter fabrication in photovoltaics [56]. For transistor applications, another method is the liquid-phase processing of polycrystalline silicon [57], which employs hydrogenated cyclic silane precursors.

Chapter 3

Experimental methods and preliminary results

The focus of this work has been on the design, production and testing of novel printed electronic devices, with a particular emphasis on transistors. Achieving this has required the use of a variety of experimental techniques, related to the production and characterisation of nanoparticles as well as to device fabrication. Silicon nanoparticles have been produced and used to formulate semiconducting functional inks. These inks, along with commercially available inks, have been deposited in specially designed patterns on flexible substrates by screen printing to produce multi-layer electronic devices. The nanoparticles and printed layers were characterised by electron microscopy and optical profilometry, and the device performance was evaluated using a range of electronic measurement techniques. This chapter comprises descriptions of the experimental methods employed throughout this work as well as presentations of preliminary results as they relate to the characterisation of nanoparticles and printed layers.

3.1 Nanoparticle production

The various methods and processes of nanoparticle production may be categorised into two basic types: bottom-up or top-down. In the bottom-up approach, nanoparticles are assembled from smaller components. This may be achieved by direct physical manipulation, such as in "dip-pen" nanolithography (DPN) [58], or more commonly, by chemical synthesis. Chemical methods may be classified as either liquid phase, including precipitation [59] and sol-gel processes [60], or gas phase, such as in chemical vapour deposition (CVD) [61]. CVD processes are now among the most common for industrial-scale production of nanoparticles, and more particularly, have been well applied to the production of microcrystalline silicon (μc-Si) [62–64] as well as silicon nanoparticles [65, 66].

The top-down approach applies an opposite strategy. In these processes, nanomaterials are produced by reducing the size of larger structures. This may be accomplished in a variety of ways, such as by chemical etching [67], electrolysis [68] or laser ablation [69, 70]. One of the dominant modes of top-down nanoparticle production, and that which has been employed in the present work, is mechanical size reduction through milling. Milling is the physical breakdown of solids into smaller particles without changing their state of aggregation [71]. The original use of milling for nanomaterial synthesis in a technical application was in the field of metallurgy, specifically aimed at the preparation of oxide dispersion strengthened solids [72]. Subsequently, it has found such diverse applications as the production of rare–earth magnetic nanoparticles [73] and nanocrystalline materials [74]. Milling processes, and high energy milling in particular, have been used to produce luminescent silicon nanoparticles [75]. Nanoparticles which exhibit luminescence tend to have capping oxide shells and are therefore not useful in applications which require electronic charge transport.

3.1.1 Milling apparatus and procedure

Nanoparticles were produced by milling bulk silicon using a Siebtechnik 800 W vibratory disc mill. This machine is capable of accepting a variety of vessel configurations, including the four pot station shown in Figure 3.1a. This station was chosen for silicon nanoparticle production due to its ability to accommodate more feedstock, as well as its relative insusceptibility to heat build-up compared to a single pot configuration.

Each milling vessel is a cylindrical pot with a cavity of diameter 8 cm and height 3.7 cm, and contains a cylindrical pestle of diameter 5.5 cm and height 3.3 cm. The lids are equipped with rubber o-rings to seal the vessels. The mill imparts linear vibrational motion to the pots in two directions as indicated by the arrows in Figure 3.1a. This results in circular and linear motion of the pestles, relative to their respective pots, whereby the feed stock is broken down by comminution, undergoing a combination of impact forces, compression and shear forces to produce progressively smaller particles [76, 77].

Figure 3.1: *(a) Four pot milling station. Pots containing pestles are sealed with lids equipped with rubber o-rings. The arrows indicate the directions of vibrational motion imparted by the mill. (b) 2503 grade silicon feed stock.*

The following milling protocol was followed throughout this project. In preparation for milling, a thorough cleaning process was carried out, whereby the pots, lids

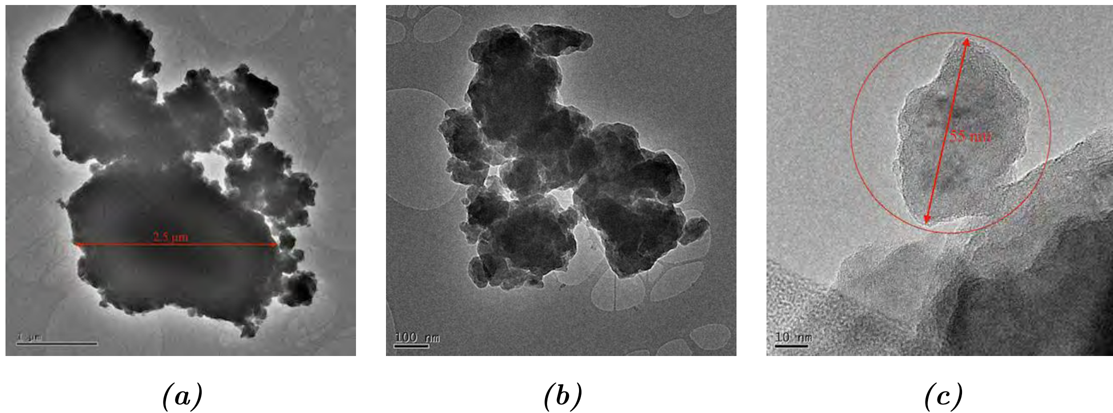
and pestles were wiped twice each with acetone and ethanol and the rubber o-rings were wiped separately with ethanol only. The pots were each loaded with 27 g of silicon feedstock. The vessels were clamped into the disc mill and the material was milled for a cumulative total of five hours. Every fifteen minutes, the milling process was briefly interrupted in order to redistribute the compacted powder in the pots.

This milling process was used to produce nanoparticles from three classes of bulk silicon. The first two classes were electronic grade single crystalline Czochralski-grown wafers, highly doped with either boron (p-type) or arsenic (n-type) and provided by Siltronix, St Louis, USA. Both types of wafer had initial resistivity $\rho < 0.005\ \Omega$cm prior to milling. The third class, shown in Figure 3.1b, was 99.9% purity 2503 grade silicon provided by Silicon Smelters, Polokwane, South Africa.

3.1.2 Nanoparticle morphology

The morphology of the nanoparticles has been investigated by transmission electron microscopy (TEM) and scanning electron microscopy (SEM). TEM was performed using a JEOL-Jem 2100 transmission electron microscope. The samples were prepared by sonicating the milled powder in methanol for 10 s and allowing the powder to settle before transferring a drop from the top of the liquid onto a holey carbon grid. Since the aim was to image single particles and small clusters of particles, a relatively long settling time of 30 s was chosen. The nanoparticle morphology was found to be characterised by clustering of smaller particles into aggregate groupings around larger particles or structures. Figure 3.2 shows TEM images of 2503 grade silicon milled for five hours, at three levels of magnification. Figure 3.2a shows a structure with a long axis 2.5 μm surrounded by clusters of smaller particles. While the large structure may appear at first to be a single particle, the gradient in its opacity or apparent density suggests that it is composed of smaller particles. Figure 3.2b shows clusters of particles ranging in size from under 100 nm to several hundred nm. Here it is clearly visible that

the clusters contain an internal structure. At higher magnification, Figure 3.2c shows a single nanoparticle of length 55 nm, circled in red. On closer inspection of this figure, it can be seen that the particle is composed of individual crystal grains. It has been determined that the silicon nanoparticle surfaces are terminated by less than a monolayer of oxygen [17, 47]. This is sufficient to chemically passivate the particles while still allowing electronic charge transport, as will be shown later, in contrast with the more common luminescent milled silicon particles [78]. Similar morphologies were observed for the nanoparticles produced from p-type wafers, n-type wafers and 2503 grade silicon [79]. It is important to note that the particle sizes obtained from these TEM studies should not be taken as generally representative of the silicon nanoparticles. This is because the sample preparation, specifically the long settling time and removal of the drop from the top of the methanol, tends to disproportionately select smaller particles.



(a) *(b)* *(c)*

Figure 3.2: *Transmission electron micrographs of 2503 grade silicon milled for five hours, shown in increasing levels of magnification. (a) at low magnification, clusters of smaller particles are visible, formed around large structures, (b) medium magnification, also showing clusters of nanoparticles, (c) high magnification: the red circle surrounds a single nanoparticle.*

The size distribution of the silicon nanoparticles was investigated by performing line-scan analyses on SEM images, captured with a LEICA/LEO Stereoscan S440 scanning electron microscope, of pellets of the milled powder. For all three classes

of five hour milled silicon, p-type, n-type and 2503 grade silicon, the distribution was found to be log-normal, with mean size of 80 nm [80].

3.2 Formulation of electronic inks

There is a long history, at least 4500 years, of using inks to form images [81]. Ink formulations vary with application and may be complex, but the two fundamental components of an ink are the colourant and the vehicle. Colourants are either pigments, which are solid particles suspended in the ink, or dyes dissolved in the liquid phase. A vehicle, consisting of a binder and a solvent, carries the colourant and binds the ink to the substrate.

In printed electronics, the goal is to print electronic components by traditional printing methods. To accomplish this, electronic inks are required, in which the colourants used in traditional inks are replaced by active materials which deliver the desired functionality. The field of printed electronics has existed for several decades and there is already a long tradition of conducting inks, such as those based on copper [43] and on silver [82], and resistive inks, usually based on carbon [83]. There has recently been much interest in the development of semiconducting inks, particularly organic polymers [49,84] and inorganic particulate inks. The inorganic inks include those containing metal oxides such as vanadium oxide [85] and zinc oxide [57], as well as silicon. Silicon inks have been used in selective emitter solar cells [56] and liquid-phase processing of polycrystalline silicon has been achieved using hydrogenated cyclic silanes such as cyclopentasilane [86] and cyclohexasilane [87]. The silicon ink which is produced in this work is unique among the available printable semiconductors, in that it is based on nanoparticulate silicon produced by a top-down method, and it does not require post-printing heat treatment to function as a semiconductor [17].

An ink must possess certain properties in order for it to be printable. Of particular relevance to printability are the rheological properties of the ink, which determine how it flows and deforms under mechanical load [88, 89]. The rheological require-

ments depend on the method of printing and it is therefore necessary to take the printing process into consideration when formulating an ink [90].

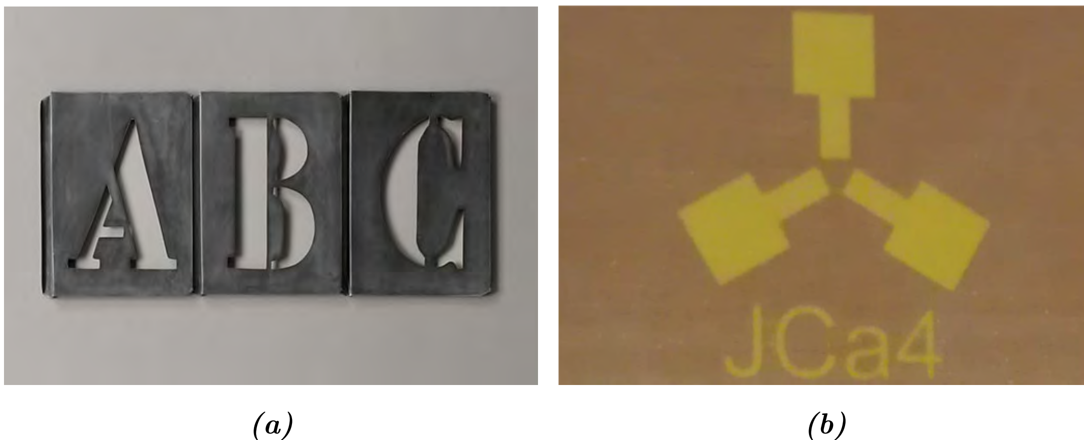
In general, to perform well in screen printing, the rheology of an ink should satisfy two requirements. The first is that it should be *thixotropic*. A material which exhibits thixotropy has the property that when it has been left to stand for a sufficiently long time, a gel structure builds up within the material, which increases its apparent viscosity. By applying a shear stress, both by mixing and through the action of the squeegee during printing, the gel structure is broken down and the material becomes less viscous [81]. This process is entirely reversible and the material will stiffen again on standing, even after undergoing shear stress. Therefore it is necessary to thoroughly mix thixotropic inks prior to printing. The second rheological requirement for a screen printing ink is that it should be *visco-elastic*. Such a material is neither purely viscous nor purely elastic but exhibits the characteristics both of a viscous liquid and of an elastic solid. Viscous liquids move under the application of a stress and retain any resulting deformation after removal of the stress, whereas elastic solids recover their form immediately on removal of the stress [81, 91].

Inks were produced by successive addition of the different silicon nanoparticles, p-type, n-type or 2503 grade silicon, to a water-based acrylic emulsion binder, provided by Marchem, South Africa. The final mass ratio of silicon to binder was 80:20 [54]. The (electrically required) high particle loading of 80% notwithstanding, the inks were screen printable. After the silicon nanoparticles had been fully mixed into the acrylic binder the consistency of the ink was adjusted by addition of a thinner, 99% pure propylene glycol, to achieve the aforementioned general rheological requirements of thixotropy and visco-elasticity as well as more specific requirements as determined by a previous study [92].

3.3 Printing the transistors

3.3.1 Screen printing electronics

Screen printing is an adaptation of the much older stencil process, in which the stencil is supported by a woven mesh. Traditional stencil printing has the disadvantage that the stencil must be one continuous piece. Isolated areas of the negative space, also known as islands, such as the interiors of the letters *A* and *B* shown in Figure 3.3a must be connected to the main image. This is a serious limitation on the possible designs which may be printed with traditional stencils. Screen printing solves this problem by applying the stencil to a mesh [93]. Figure 3.3b shows a screen stencil used for printing the electrodes of the device which will be discussed in section 4.2. The yellow area is open mesh, through which ink may pass during printing,while the brown area is blocked. Using such a stencil, it is possible to print designs which include isolated areas of negative space, such as the interiors of the letter *a* and the number 4 in the figure.



(a) *(b)*

Figure 3.3: *Stencils: traditional and screen printing. (a) Traditional stencil letters. Isolated areas of the design, such as the interiors of the letters A and B, must be connected to the main stencil by ties (image source:* `http://www.restorationhardware.com/`*). (b) Screen printing stencil. The yellow area is an open mesh through which ink may pass and the brown area is blocked.*

The devices produced in this work were printed using an Atma 60PD semi-automatic screen printer, similar to that shown in Figure 3.4. There are four basic elements which are essential in order to screen print. These are the ink, a screen which defines the design, a substrate onto which to print and a squeegee to force the ink through the screen [94]. Figure 3.5 illustrates the basic screen printing process,

Figure 3.4: *Atma 60PD semi-automatic screen printer.*

with the elements shown in cross-section. The screen consists of a woven mesh stretched over a frame. Originally, screens were made of woven silk, hence the term silk screen printing. More recently, however, screens tend to be either of synthetic fibers, such as nylon or polyester, or metal fabric. The screens used in this study were woven monofilament polyester stretched over aluminium frames. A stencil has been produced on the underside of the mesh by applying a light-sensitive emulsion and using photolithography to expose the image. The stencil pattern leaves open areas in the mesh, through which ink may pass. The screen is

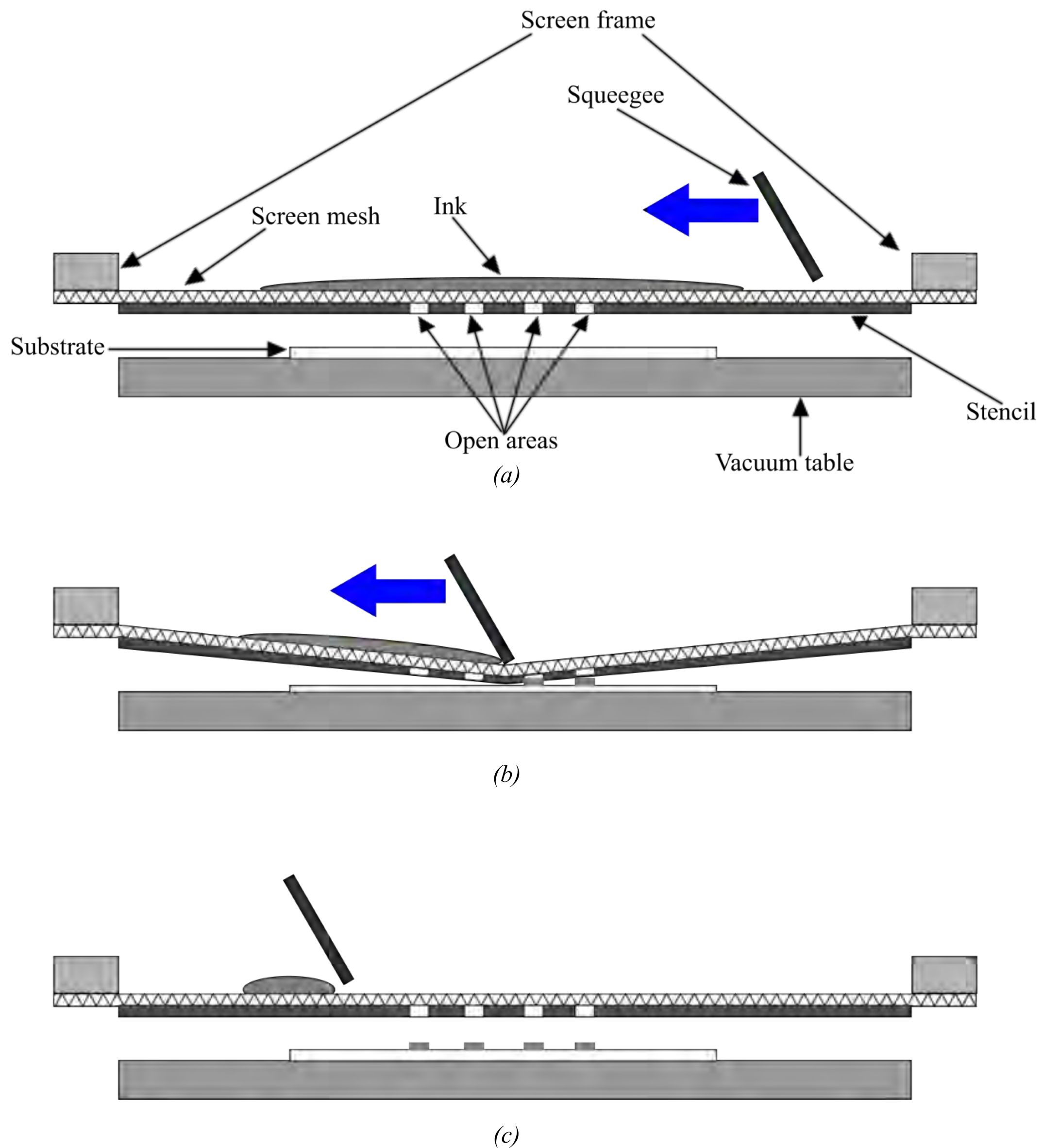


Figure 3.5: *The screen printing process. (a) The screen consists of photolithographic stencil supported by a stretched woven mesh which is mounted on a frame. Ink is applied to the upper side of the screen. The substrate is mounted on a vacuum bed located below the screen. (b) The squeegee moves down, forcing the screen into contact with the substrate and then moves to the left. Ink is forced by the squeegee through the open areas of the mesh, from where it is transferred to the substrate by capillary action. (c) As the squeegee passes, the screen snaps off the substrate, leaving behind the printed image.*

positioned in close proximity to a substrate, which is held in place by a vacuum bed during the printing process. Ink is placed on the screen. To print, the sharp-edged rubber squeegee is lowered, forcing the mesh into a line of contact with the substrate. The squeegee is then moved across the screen, in the direction indicated by the blue arrow. The ink is pushed along the screen and forced into the open areas of the mesh, from where it is transferred to the substrate by capillary action. As the squeegee passes a given open area, that part of the screen snaps off the substrate, leaving behind the printed image.

Finally, the printed layer must be cured. Curing methods vary with substrate, ink type and application. Certain inks are designed to be curable by exposure to ultraviolet radiation or laser light [95] and high temperature curing is ubiquitous in printed electronics [96]. However, it has been found that printed layers consisting of the materials used in this study are curable simply by exposure to ambient conditions for 24 hours [97]. Therefore, ambient curing has been used throughout this work.

Printing electronic devices involves the deposition of different functional inks, in specific orders and patterns, onto substrates. The devices produced in this work required, in addition to the semiconducting silicon inks which have already been discussed, conducting ink to form the electrodes as well as, in the case of the insulated-gate field-effect transistors to be described in section 4.1, an insulating ink to isolate the gate from the semiconducting region. The specific material combinations used for each type of device will be discussed in detail in the next chapter. However, it is appropriate at this point to include some general comments regarding the printing of these materials. The electrodes were printed with a commercially available silver ink, DuPont LuxPrint 5000 silver conductor, with the exception of a few test structures for which an indium tin oxide (ITO)-based transparent conducting oxide (TCO) was used. The insulating layers, where required, were printed with DuPont 8153 high-k dielectric. A double stroke printing mode was employed for each of these materials, which improved the ink coverage. The print speed, that is, the speed with which the squeegee moves along the

screen, was 250 mm/s for the silver ink and 200 mm/s for both the silicon ink and the insulating ink. The print speed was varied because it affects the printed layer thickness: faster printing results in a thinner layer, and these parameter values were found to yield the best results. The samples were allowed to cure under ambient conditions for 24 hours between printing successive layers.

3.3.2 Characterisation of the printed layers

The printed layers have been studied using optical profilometry and scanning electron microscopy, in order to determine certain characteristics which could influence their electrical performance, such as layer thickness, layer uniformity and surface roughness.

The profilometry studies were carried out using a Wyko NT9100 Optical Profiler supplied by Veeco, in Vertical Step Interferometry (VSI) mode. With this technique, height profiles of printed layers with resolution below 100 nm were obtained. Prior to profiling, the samples were coated with an evaporated layer of gold-palladium (AuPd), the purpose of which was to eliminate the differences in reflectivity of the silver, silicon and substrate, allowing them to be imaged simultaneously.

Figure 3.6 shows the profilometry results for a sample consisting of a silver layer screen printed on paper. A colour height map is plotted in Figure 3.6a, with the height scale graded in μm. The regions of silver and substrate are indicated. The red and blue lines indicate the locations over which line-scan height profiles were taken, which are plotted in Figure 3.6b and Figure 3.6c. The contour plot indicates that height variation of the silver layer is approximately ± 2 μm, while the line-scan height profiles show that the average thickness of the silver layer is $4.5 - 5.0$ μm.

In order to compare the uniformity of the different printed layers, it is useful to calculate certain parameters pertaining to surface roughness. There exist several surface roughness parameters [98], two of the most common being the average

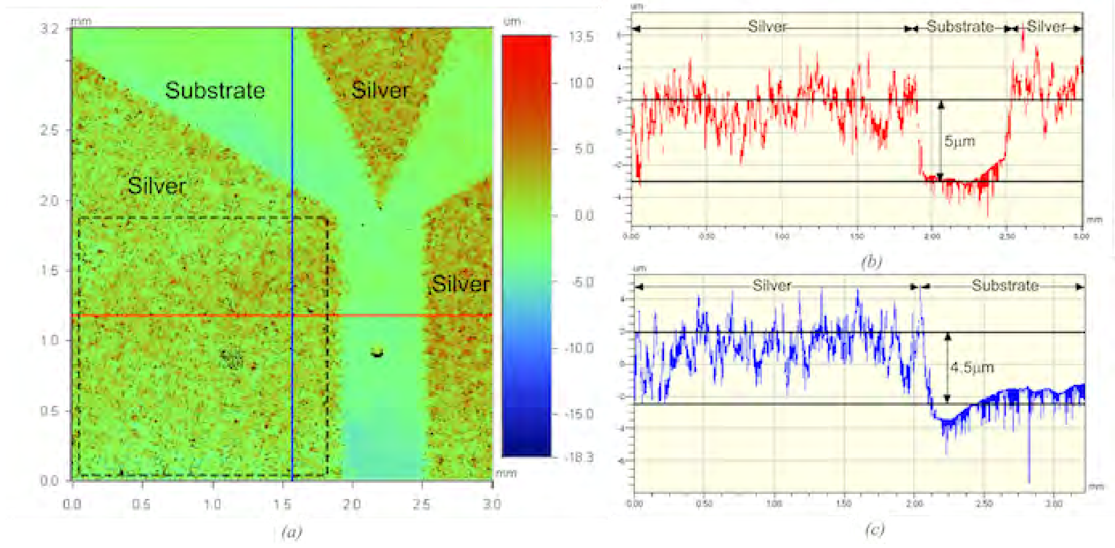


Figure 3.6: *(a) Optical profile of silver electrodes printed on paper. The colour map indicates height, graded in µm by the scale on the right. The regions of silver and substrate are indicated. The dashed black square indicates the area over which the surface roughness has been calculated. The red and blue lines indicate the locations of the line-scan height profiles. (b) Height profile along the red line. (c) Height profile along the blue line.*

roughness, R_a, and root-mean-squared roughness, R_q. R_a is the mean deviation in height of each measurement point from the mean height of all the points, while R_q is the root-mean-square deviation in height of all the points from the mean height. These parameters are defined as

$$R_a = \frac{1}{n}\sum_{i=1}^{n}\left|Z_i - \bar{Z}\right| \text{ and } \tag{3.1}$$

$$R_q = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(Z_i - \bar{Z}\right)^2}, \tag{3.2}$$

where n is the number of height measurement points, Z_i are the individual height measurements and $\bar{Z}$ is the mean height. For each of these parameters, the larger its value, the more rough the surface. For the printed silver layer shown

in Figure 3.6a, the surface roughness parameters have been calculated over an area of (1.76 mm $\times$ 1.81 mm), indicated by the dashed black square, yielding $R_a = 1.05$ μm and $R_q = 1.34$ μm.

Figure 3.7 shows the profilometry results for a printed structure consisting of three silver electrodes printed on paper, with an elliptical layer of silicon nanoparticle ink printed on top. The silicon layer of this sample was displaced to the left during

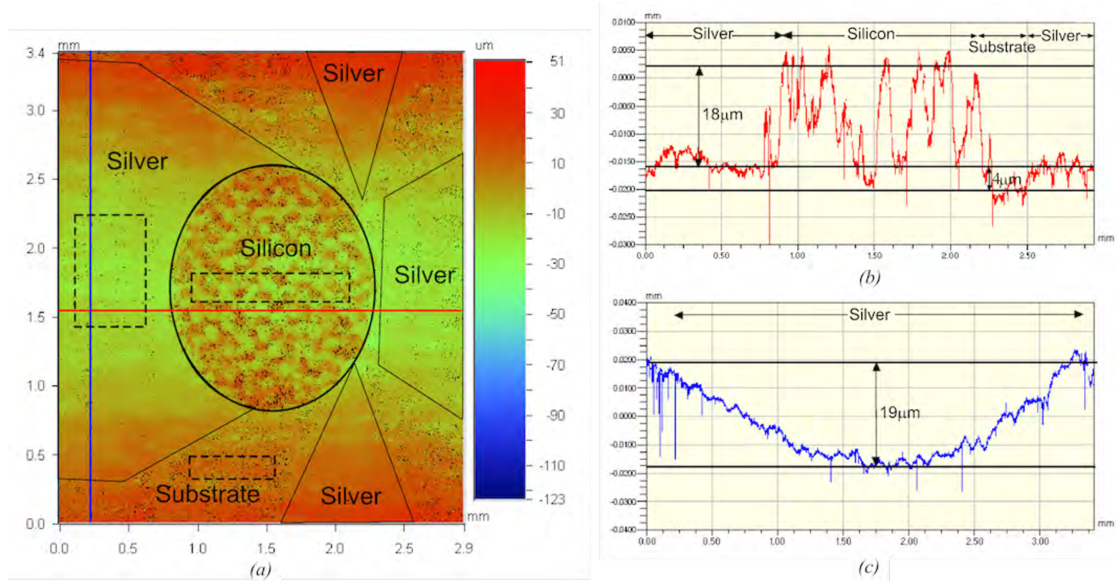


Figure 3.7: *(a) Optical profile of silicon nanoparticle ink and silver printed on paper. The colour map indicates height, graded in μm by the scale on the right. The regions of silicon, silver and substrate are indicated, with the boundaries between these demarcated by solid black lines. Dashed black rectangles indicate areas over which surface roughness has been calculated. The red and blue lines indicate the locations of the line-scan height profiles. (b) Height profile along the red line. (c) Height profile along the blue line.*

the printing process, relative the to corresponding device design to be presented in section 4.2, to be positioned on top of the relatively flat silver electrode, in order that the silicon surface profile could be measured with minimal influence from the opening between the silver electrodes. As with the previous sample, this figure includes a colour height map and two line-scan height profiles. In Figure 3.7a the regions of silicon, silver and substrate are indicated and demarcated by

solid black lines, while the dashed black rectangles indicate the areas over which the surface roughness has been calculated. The red and blue lines indicate the scan lines which were used for the height profiles shown in Figure 3.7b and Figure 3.7c. The red line scan in Figure 3.7b shows that the silicon layer has a maximum thickness of approximately 18 μm, and that its height is much less uniform than the adjacent silver layers. This indicates that the silicon has significant roughness, which is also illustrated by the puckered effect in the colour map, whereby regions of orange and yellow are closely interspersed within the silicon ellipse. This is in stark contrast to the silver layers, which in the colour map exhibit locally smooth variation. Additionally, the red line scan was used to measure the height of the right-hand silver electrode, yielding a value of 4 μm. This is in general agreement with the silver height values obtained for the previous sample.

There is a general trend in the vertical direction on the colour map, in which the top and bottom are red-orange while the centre is yellow-green. This is not due to the intrinsic properties of the printed layers, but rather it is an artefact arising from a slight curvature of the sample, and is well illustrated by the vertical direction line scan height profile, shown in Figure 3.7c. There appears to be a quasi-parabolic trend to the sample height in the vertical direction, with the top and bottom being approximately 19 μm higher than the centre.

The surface roughness properties have been calculated for the substrate, silver and silicon, using areas of (0.63 mm $\times$ 0.18 mm), (0.51 mm $\times$ 0.81 mm) and (1.15 mm $\times$ 0.28 mm) respectively. These are indicated by the dashed black rectangles in Figure 3.7a. The results of the calculations are shown in Table 3.1. The average roughness of the silver layer was found to be approximately 1.92 μm, which is significantly higher than that of the previous sample (1.05 μm). However, this is not expected to influence the device performance, because the area under consideration is on the surface of an electrode, and not the interface between the silver and silicon. The average roughness of the silicon layer was found to be approximately 5.09 μm. It is unsurprising that the silicon layers had a higher

average roughness than the silver, given that when the silver ink is wet, it tends to pool and forms a smoother surface upon curing.

Generally, silver is the smoothest surface, while the paper is slightly more rough and the printed silicon has the highest roughness. The average roughness of the silver showed significant variation across the print runs. However, the silver layer thickness exhibited uniformity across the print runs, which suggests that printed layer thickness in general may remain relatively constant across multiple print runs, provided the printing parameters are held constant.

Table 3.1: *Surface roughness parameters for the structure shown in Figure 3.7a, comprising silicon and silver printed on paper.*

Surface	R_a (μm)	R_q (μm)
Paper	2.27	3.16
Silver	1.92	2.37
Silicon	5.09	6.15

Scanning electron microscopy (SEM) was used to study printed layers in cross-section. Sample cross-sections were prepared by casting printed layers in resin, cutting the casts into slices with a diamond-coated saw and polishing the resulting slices with a paste containing aluminium oxide. The studies were carried out on a LEICA/LEO Stereoscan S440 SEM. The insulated-gate field-effect transistor (IGFET), the design of which will be presented in the next chapter, was chosen for cross-sectional imaging due to its relatively complex layer structure, which consists of a bottom gate electrode printed on paper with DuPont LuxPrint 5000 silver, followed by an insulating layer of DuPont 8153 high-k dielectric, a layer of silicon nanoparticle ink and finally a top layer of DuPont LuxPrint 5000 silver forming the source and drain electrodes. Figure 3.8 is a low magnification SEM micrograph showing a cross-sectional view of a printed structure designed to be an IGFET. The inset figure shows a photograph of the printed device, with the dashed blue line indicating the location of the cross-section. From left to right in the micrograph, the paper substrate, the silver layer forming the gate contact,

the dielectric and the silicon layer are indicated. It is clear that the interfaces between the printed layers are not flat, but rather follow the contours of the paper substrate. From the scale bar, the silicon layer has a thickness of $15 - 20$ μm, in general agreement with the profilometry results. There are also two visible areas where the silicon and dielectric layers have delaminated, which could have resulted from the cross-section sample preparation.

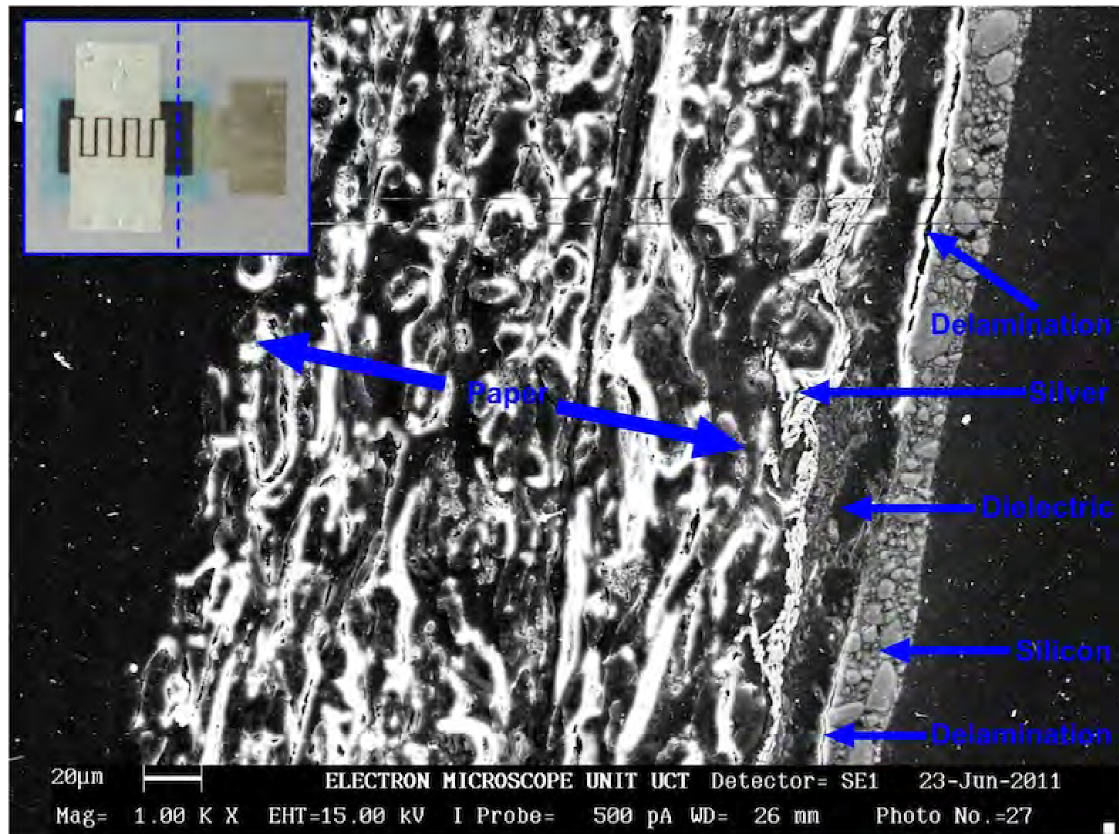


Figure 3.8: *SEM micrograph: cross-section view of a printed structure designed to be an IGFET, showing p-type silicon, DuPont high-k dielectric and DuPont silver on paper. There are two visible areas of delamination between the silicon and dielectric layers. Inset: photograph of the printed structure. The dashed line indicates the position where the cross-section image was taken.*

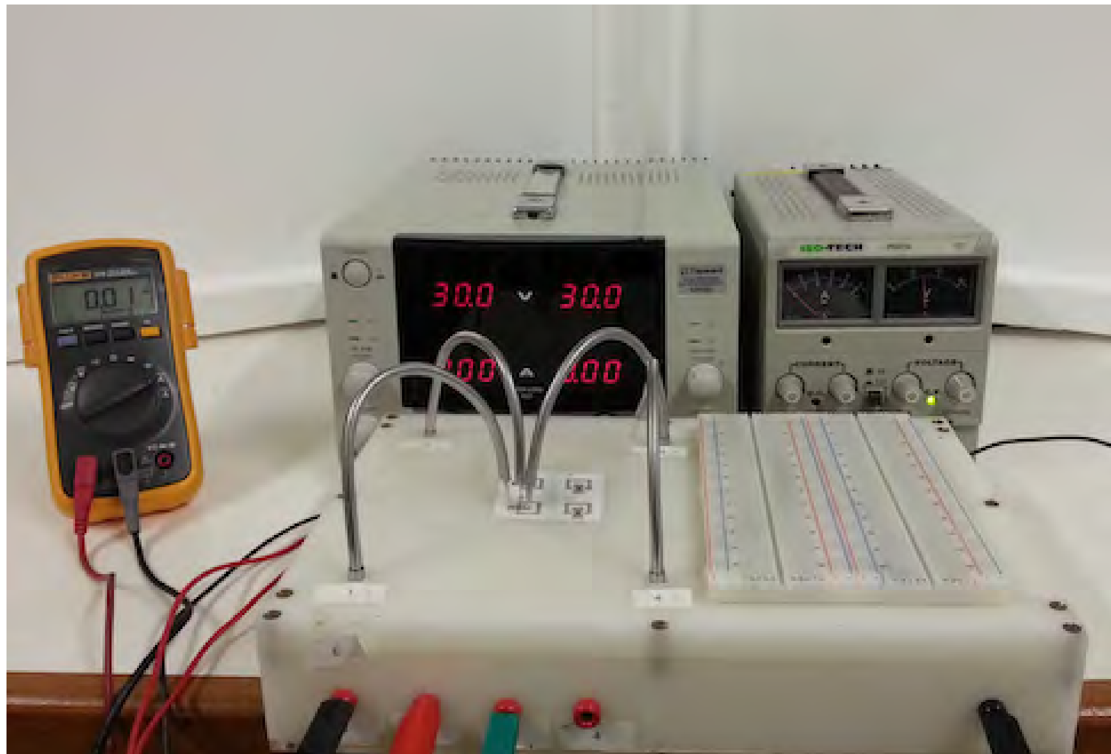
3.4 Electrical characterisation of the printed devices

In carrying out this study, the most important experimental work has been the electrical characterisation of the transistors under development. Two classes of electrical tests were carried out, the first of these being rudimentary bench tests, followed by more advanced testing using an industry standard semiconductor characterisation system. In this section the experimental setup for both classes of tests will be described.

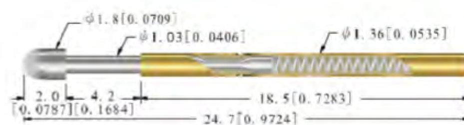
3.4.1 Bench tests

The purpose of the bench tests was to evaluate the DC performance of the printed transistors. The measurement setup is shown in Figure 3.9a. To facilitate the connection of the transistors to the measurement circuit a customised testing station, shown in the foreground, was designed and fabricated. The station comprises a box made of 18 mm thick vinyl, which provides good electrical insulation. It features four spring-loaded test probes (see schematic shown in Figure 3.9b) mounted in adjustable gooseneck cables. The probes are made from Au plated brass barrels and Rh plated BeCu plungers, both of which exhibit excellent electrical conductivity. Round probe tips were chosen to avoid damaging the printed devices. Each probe is wired to a 4 mm banana socket on the left of the front panel. In order to provide shielding, the gooseneck cables are connected to a common terminal on the right of the front panel, which was grounded during testing. A solderless breadboard mounted on the top panel of the testing station allows connection to external components if desired.

Printed transistors were connected to the testing station by placing them on the top panel and positioning the test probes in contact with the printed electrodes, as shown in Figure 3.9a. Two Topward 6303D 30 V DC power supplies together with an ISO-TECH IPS601A 60 V DC power supply were used in different combinations



(a)



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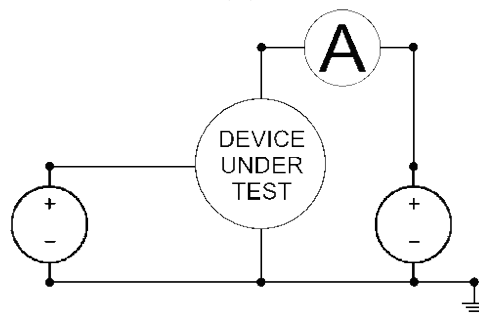


(c)

Figure 3.9: *(a) Bench test setup for electrical characterisation. Custom built testing station (foreground) is used to connect a printed transistor to DC voltage sources (background). (b) Spring-loaded test probe schematic with dimensions shown in millimetres. (Figure from* `http://www.electrocomponents.com`*). (c) Bench test circuit diagram.*

to provide a constant bias potential across the collector-emitter while varying the potential difference applied across the base-emitter. Throughout the tests, a FLUKE 111 digital multimeter was used to monitor the current at the collector terminal and the measurement was repeated for several different values of the collector-emitter potential. Figure 3.9c shows a circuit diagram representing the setup. The bench power supplies limited the possible combinations of the base potential and the collector potential which could be simultaneously applied, as illustrated by the chart in Figure 3.10. To supply a maximum potential of 90 V either to the base or the collector, the other potential is limited to 30 V. In a balanced configuration, both potentials are limited to 60 V.

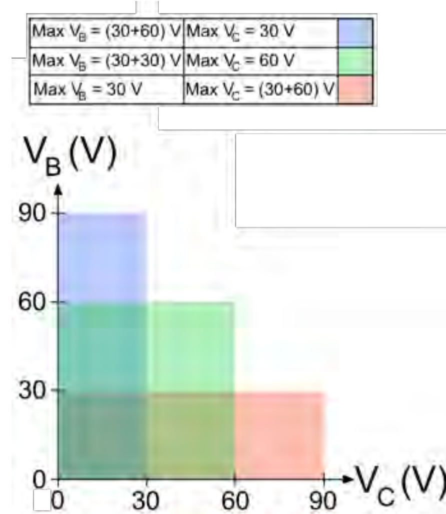


Figure 3.10: *Bench power supply limitations.*

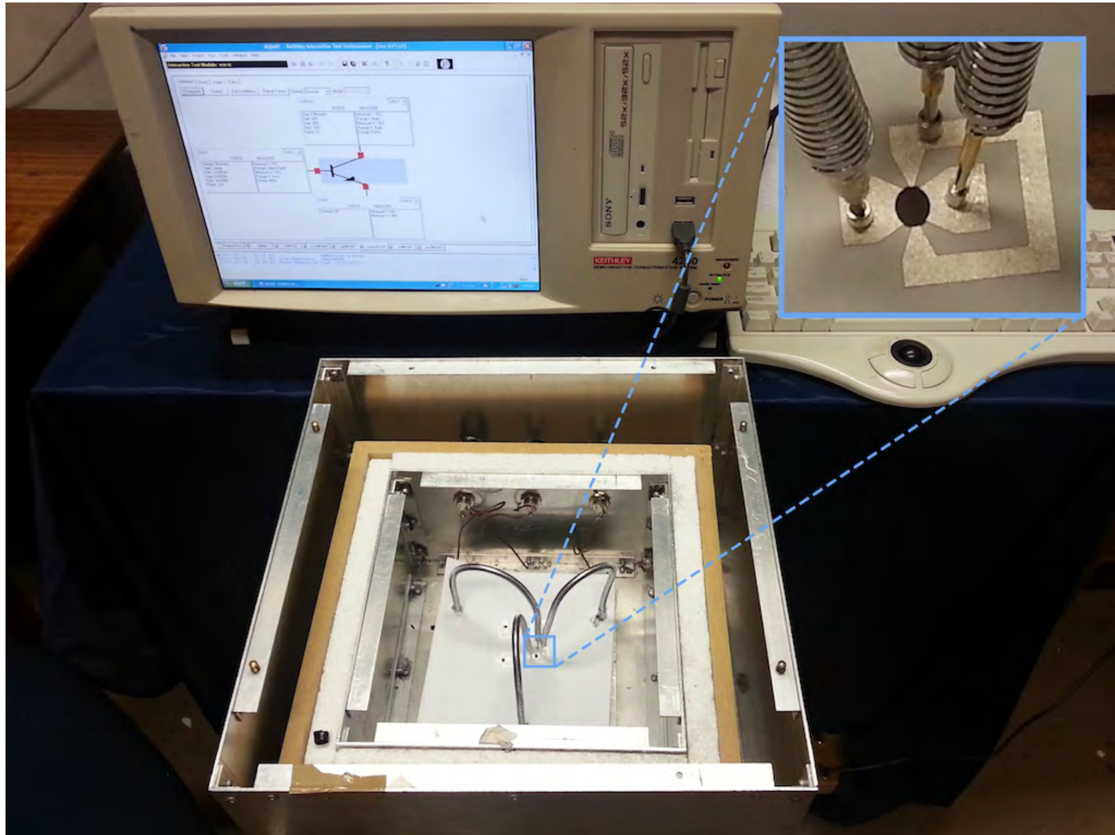
3.4.2 Keithley 4200 SCS tests

The electrical performance of the transistors developed in this study was investigated using an industry standard Keithley 4200 Semiconductor Characterisation System equipped with two Source Measurement Units (SMUs) (see Figure 3.11). These enable the independent supply of DC voltage signals up to 200 V or DC

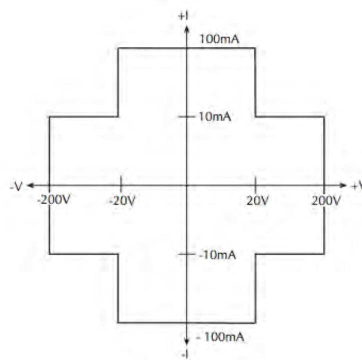
currents up to 100 mA, while simultaneously measuring these signals with millivolt and microampere resolution. Figure 3.11b illustrates the operating boundaries of the SMUs. When acting as a voltage source, the SMU operates in one of two ranges with maximum voltages of 20 V and 200 V. In the 20 V source range, the measured current is limited to 100 mA, while in the 200 V source range, the measured current is limited to 10 mA. Similarly, when acting as a current source the SMU operates either in a 10 mA source range or a 100 mA source range, with measured voltages limited to 200 V and 20 V respectively. In each case, the power delivered to the device under test is limited to 2 W [99].

Figure 3.11a shows the experimental setup. The SMUs and the ground unit were connected by triaxial cables to three spring-loaded probes of the type described in section 3.4.1. In order to shield the measurement circuit from electromagnetic interference, the adjustable gooseneck cables supporting the probes were mounted inside a double Faraday cage. The central lines of the triaxial cables were connected to the test probes by single core copper wires. The inner shielding lines of the triaxial cables as well as the goosenecks were electrically common with the inner Faraday cage, which was grounded. The inset figure shows a magnified view of a fully printed transistor connected to the measurement circuit via the test probes.

The printed current switching transistors were subjected to a standard test, which consisted of sweeping the base current from -0.1 mA to $+0.1$ mA while measuring the collector current and the base potential, to determine two characteristics: the output characteristic and the current-voltage transfer characteristic. The output characteristic is the current-voltage relationship at the collector terminal: it is the collector current as a function of the collector-emitter potential, measured for various values of the base-emitter potential. The transfer characteristic is an indication of the device's output at the collector, given a certain input at the base. It is the collector current as a function of the base-emitter potential, measured for various values of the collector-emitter potential. An alternative transfer function,



(a)



(b)

Figure 3.11: *(a) Keithley 4200 SCS (background) connected to a double Faraday cage testing box (foreground). Inset: magnified view of a fully printed transistor connected to the measurement system via spring-loaded probes which are mounted on adjustable goosenecks. (b) Keithley 4200 SCS SMU operating boundaries. This chart maps the current and voltage limits of the Source Measurement Units. (Image from Keithley 4200 reference manual.)*

the current-current transfer characteristic, was also measured. This is the collector current as a function of the base current.

Throughout this research, several thousand CSTs have been printed and characterised. Table 3.2 is a directory of those asymmetric CSTs whose characteristics will be presented, along with their material constituents as well as figure references to locate the corresponding data plots. The electrodes were typically printed with DuPont LuxPrint 5000 silver conductor, but in a few cases these were printed with an ITO-based TCO. The semiconducting layers were printed with n-type, p-type or grade 2503 silicon nanoparticles, as well as TCO in certain test structures. Similarly, Table 3.3 lists the symmetric and interdigitated CSTs which will be presented. For the sake of brevity, the characteristics of a representative set of devices, comprising one sample for each material combination, are presented in chapter 5. The data associated with the remaining devices are included in appendix A.

Table 3.2: *A list of the asymmetric CST samples to be presented. The electrodes have been printed with silver or TCO, with active layers being n-type Si, p-type Si, 2503 grade Si or TCO.*

Sample ID	Electrodes	Active Layer	Figure
N-02-J03	Silver	n-type Si	5.6
N-02-J05	Silver	n-type Si	A.1
N-15-J03	Silver	n-type Si	A.2
N-15-J05	Silver	n-type Si	A.3
N-15-J09	Silver	n-type Si	A.4
N-15-J10	Silver	n-type Si	A.5
N-15-J19	Silver	n-type Si	A.6
N-22-J04	Silver	n-type Si	A.7
N-22-J11	Silver	n-type Si	A.8
N-22-J12	Silver	n-type Si	A.9
P-03-J06	Silver	p-type Si	5.7
P-03-J10	Silver	p-type Si	A.10
P-03-J20	Silver	p-type Si	A.11
P-05-J12	Silver	p-type Si	A.12
P-08-J03	Silver	p-type Si	A.13
P-08-J04	Silver	p-type Si	A.14
P-08-J05	Silver	p-type Si	A.15
P-08-J11	Silver	p-type Si	A.16
P-08-J14	Silver	p-type Si	A.17
P-10-J11	Silver	p-type Si	A.18
M-07-J19	Silver	grade 2503 Si	5.8
M-01-J13	Silver	grade 2503 Si	A.19
M-15-J13	Silver	grade 2503 Si	A.20
TCO-P-04-J12	TCO	p-type Si	5.9
TCO-P-04-J13	TCO	p-type Si	A.21
TCO-02-J03	Silver	TCO	5.10

Table 3.3: *A list of the symmetric and interdigitated CST samples to be presented.*

Design	Sample ID	Active Layer	Figure
Symmetric	JTA3-P-02	p-type Si	5.11
Symmetric	JTB1-P-09	p-type Si	A.22
Interdigitated	Inter-P-2-8	p-type Si	5.12
Interdigitated	Inter-P-2-9	p-type Si	A.23

Chapter 4

Transistor designs

In this chapter the designs of the transistors developed in this study are presented. Initially, in order to demonstrate that printed silicon may be used in a functional transistor, a fully printed insulated-gate field-effect transistor (IGFET) was produced [100]. Finally, a novel type of device was developed, which represents the bulk of the research undertaken in the present work, and which is the main focus of this thesis. The behaviour of this device has been found to be unlike that of any known transistors. Based on an analysis of its performance, to be discussed in the following chapters, this device has been named a current switching transistor (CST) [54, 55].

4.1 Insulated-gate field-effect transistor

The architecture of the printed IGFETs presented here has more in common with those used in the fabrication of amorphous silicon thin film transistors (a-Si TFTs) [101] than with the classical planar architecture of traditional silicon devices [102]. The IGFET design consists of four layers, which are shown in Figure 4.1a. These are the gate electrode, an insulating layer, a semiconducting layer and co-planar, interdigitated source and drain electrodes. In the bottom-gate config-

uration, the layers are printed in the aforementioned sequence, resulting in the structure schematically shown in Figure 4.1b. Top-gate devices are produced by printing in the reverse order, starting with the source and drain electrodes. Figure 4.1c shows a photograph of a fully printed bottom gate IGFET, consisting of silver electrodes printed on paper with p-type silicon and DuPont 8153 high-k dielectric. The interdigitation of the source and drain results in higher conductances of the semiconducting region between these electrodes, owing to the increased channel width as compared to non-interdigitated designs. The source-drain channel of the present design has width 14.4 mm and length 200 μm, giving a width to length ratio of 72.

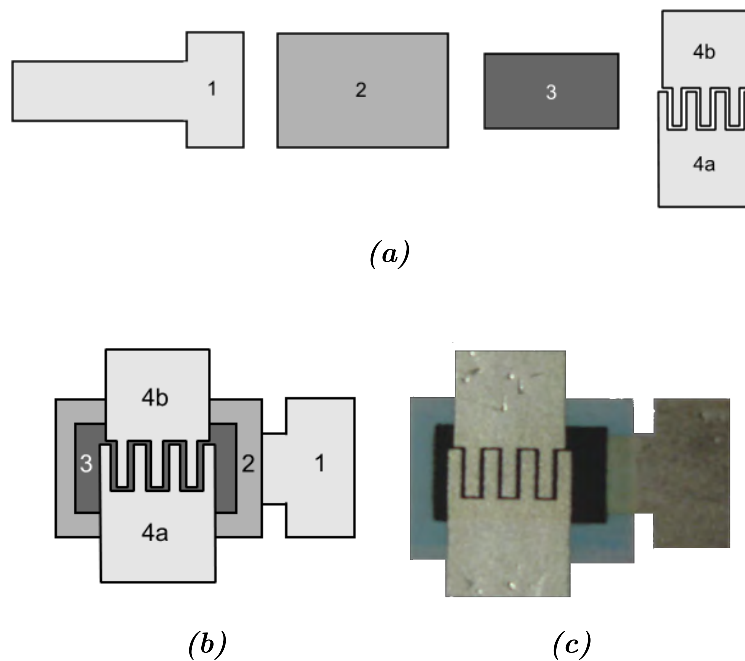


Figure 4.1: *Design of the fully printed insulated-gate field-effect transistor: (a) IGFET layers shown individually: (1) gate, (2) insulator, (3) semiconducting layer, (4a) source and (4b) drain. (b) Staggering sequence of printed layers, shown for the bottom gate configuration. (c) Photograph of a fully printed IGFET: silver electrodes with a printed p-type silicon semiconducting layer and DuPont 8153 high-k dielectric as a gate insulator, printed on paper.*

The IGFETs were screen printed on a variety of flexible substrates, most commonly 80 g m^{-2} uncoated bond paper of nominal thickness 100 μm. The electrodes were printed with DuPont LuxPrint 5000 silver conductor and the gate insulators were printed with DuPont 8153 high-k dielectric. The semiconducting layers were printed with inks containing nanoparticles produced from electronic grade n-type and p-type silicon, doped with arsenic and boron respectively, as well as 2503 grade silicon.

4.2 Current switching transistor

The designs of a novel device produced in this study, the current switching transistor, will be presented here. Figure 4.2 shows photographs of three variations of fully printed current switching transistors: (a) the asymmetric CST, (b) the symmetric CST and (c) the interdigitated CST. Although it was later found to behave entirely differently, the CST was intended to function in a similar manner to the point contact transistor. The electrodes have therefore by analogy been named collector, emitter and base. These contacts were printed with DuPont LuxPrint 5000 silver ink and are indicated by C, E and B respectively, in Figure 4.2. The semiconducting layers, indicated by S, were printed with either boron-doped p-type (pictured), arsenic-doped n-type, or 2503 grade silicon nanoparticles which were produced as described in section 3.1 and mixed into inks as discussed in section 3.2. The doped silicon had an initial resistivity of $\rho < 0.005$ Ωcm prior to milling. Scale bars at the top of each photograph, ruled in mm, give an indication of device size.

The substrate material was 160 g/m^2 uncoated bond paper of nominal thickness 200 μm, supplied by Sappi, South Africa. Uncoated paper is hygroscopic, which presents the risk that the electrical performance of the printed devices could be influenced by relative humidity, through the addition of a shunt resistance. However, the electrical measurements were performed at approximately standard conditions, in which humidity is not a significant factor. Furthermore, the electrical resistance

of the silicon devices is low compared to that of the substrate, and therefore shunt resistances through the substrate are not a concern.

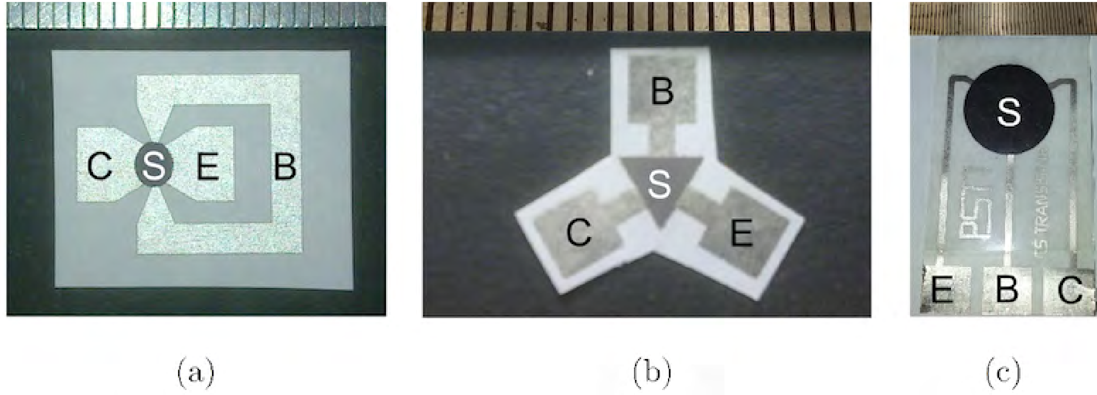


Figure 4.2: *Photographs of three fully printed current switching transistors on paper substrates: (a) Asymmetric CST. (b) Symmetric CST. (c) Interdigitated CST. C, E, B and S indicate the collector, emitter, base and semiconducting layer respectively. The electrodes were printed with DuPont LuxPrint 5000 silver ink. Semiconducting layers were printed with ink containing boron-doped p-type silicon nanoparticles. Top rules indicate the scale and are graded in mm.*

The three CST variants are functionally similar, differing only in their electrode configurations. Before discussing the intricacies of each design, the common elements will be introduced. The CST consists of three electrodes, printed on a substrate in a co-planar configuration and connected by a semiconducting material.

A detailed illustration of the asymmetric CST configuration is shown in Figure 4.3. The dashed ellipse in Figure 4.3a represents the boundary of the semiconducting layer, while the solid lines denote the shape of the electrodes. Figure 4.3b shows a magnified view of the electrode layout beneath the semiconductor. The base electrode (B) is in contact with the semiconductor in two regions, near both ends of the major axis of the ellipse. The collector (C) and emitter (E) electrodes are reflections of one another about the major axis of the ellipse, and make contact with the semiconductor layer on its left and right side respectively. The electrode dimensions are a = 2.5 mm, b = 5.1 mm, c = 11.1 mm, d = 12.1 mm and

$e = 0.2$ mm. The collector and emitter are separated by a distance of $f = 0.4$ mm and the shortest distance between the base electrode and either the collector or emitter is $g = 0.2$ mm.

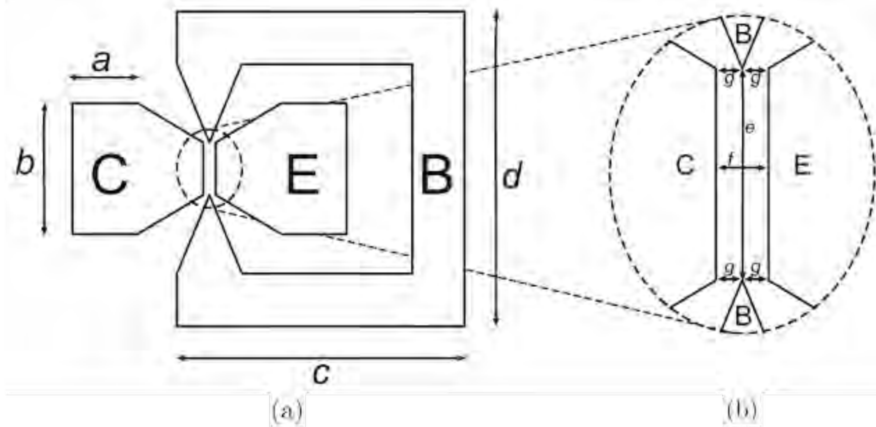


Figure 4.3: *(a) Asymmetric CST design. Collector, emitter and base electrodes are labelled C, E and B respectively. The dashed ellipse represents the boundary of the semiconducting layer. (b) Magnified view of the electrode layout beneath the semiconductor.*

The second design, the symmetric CST, is shown in Figure 4.4. This device is named for the third order rotational symmetry it exhibits about its geometric centre. As with the asymmetric design, the semiconductor is represented by the dashed shape, in this case an equilateral triangle. Figure 4.4b shows a magnified view of the electrode layout beneath the semiconductor. The electrode dimensions are $h = 3.2$ mm, $i = 2.2$ mm and $j = 1.2$ mm. The shortest distance between the contacts is $k = 0.2$ mm.

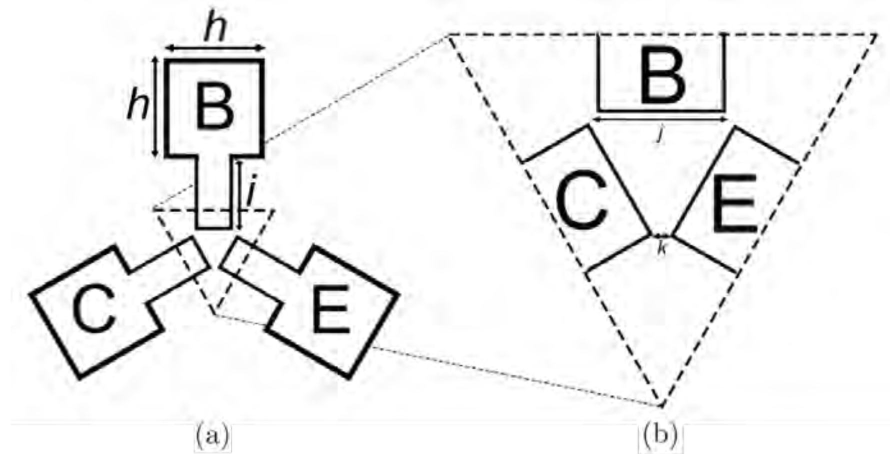


Figure 4.4: (a) Symmetric CST design. Collector, emitter and base electrodes are labelled C, E and B respectively. The dashed triangle represents the boundary of the semiconducting layer. (b) Magnified view of the electrode layout beneath the semiconductor.

The third and final CST design, shown in Figure 4.5, is the interdigitated CST. For this design, the electrodes are interdigitated in order to reduce the resistance of the semiconducting region between the contacts. This device is thus designed to operate at higher currents than the asymmetric and symmetric configurations. The dashed circle represents the semiconducting layer and the electrode layout is magnified in Figure 4.5b. Considering only the areas of the electrodes which are beneath the semiconductor, this device exhibits third order rotational symmetry similar to the symmetric CST. The electrodes consist of circular arcs of various radii, connected to a radial branch. The fingers are separated by a distance $n = 0.4$ mm and there is a circular gap at the centre of the device of diameter $m = 2.8$ mm.

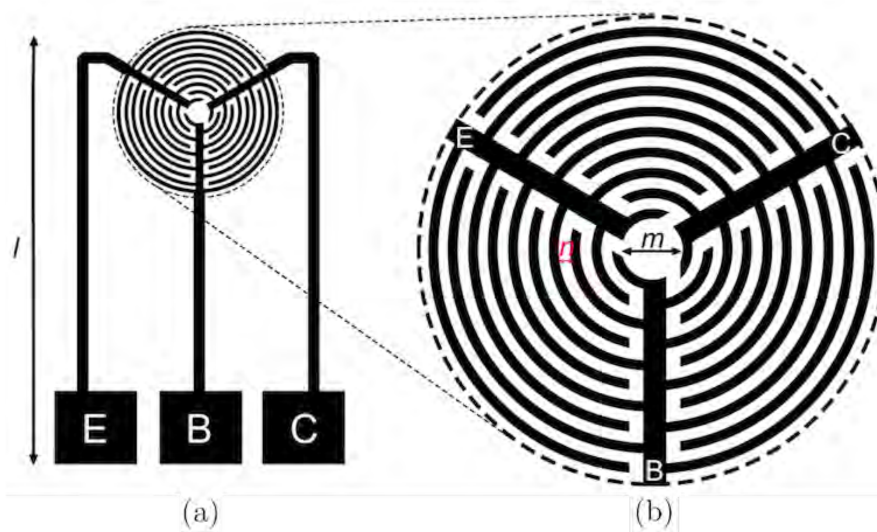


Figure 4.5: *(a) Interdigitated CST design. Collector, emitter and base electrodes are labelled C, E and B respectively. The dashed circle represents the boundary of the semiconducting layer. (b) Magnified view of the electrode layout beneath the semiconductor.*

Chapter 5

Results

In this chapter the results of the electrical characterisation of both the insulated-gate field-effect transistors and the current switching transistors will be presented. The devices were characterised as described in section 3.4.2.

5.1 Electrical properties of the printed silicon

The electrical properties of the printed silicon layers have been studied by measuring their current-voltage characteristics using a Keithley 4200 semiconductor characterisation system. Printed layers of 2503 grade, n-type and p-type silicon on silver contacts were investigated. Figure 5.1 shows a representative current-voltage characteristic curve measured at 300 K for an ink containing 2503 grade silicon nanoparticles in a ratio of 80:20 by mass with an acrylic binder. The IV curve shows that at low applied voltage, the differential conductance $\mathrm{d}I/\mathrm{d}V$ is small, implying a large resistance. As the applied voltage increases, there is a nonlinear increase in conductance, or a decrease in resistance. The IV characteristic is symmetrical, with equal conductances for voltages of equal magnitude but opposite sign. The symmetry of the IV curve, together with the nonlinear dependence of current on voltage, are indicative of a symmetric diode arrangement, typical of a

varistor. Similar behaviour was observed for all three types of silicon. In chapter 6, these electrical characteristics will be examined in more detail, and will be shown to be a crucial element in explaining the principles of operation of the current switching transistor (CST) developed in this study.

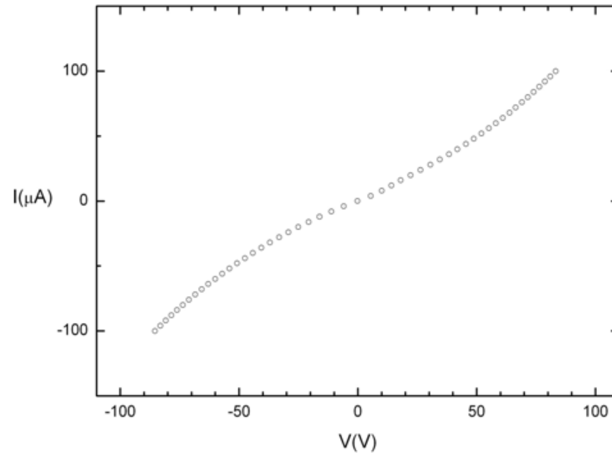


Figure 5.1: *Typical current-voltage characteristics of a layer of 2503 grade silicon nanoparticles, printed on paper and measured at a temperature of 300 K.*

5.2 Insulated-gate field-effect transistor results

Although many fully printed insulated-gate field-effect transistors, which exhibit similar behaviour, have been printed in the course of this research, the characteristics of a representative set of two devices will be presented here. The material configurations of these devices are shown in Table 5.1, with the semiconducting layers printed using highly doped silicon nanoparticles, either p-type or n-type. IGFETs with both bottom-gate and top-gate architectures have been printed. However, the top-gate structure was found to exhibit poorer characteristics [100], especially when DuPont 8153 high-k dielectric was used as the gate insulator. This is possibly due to the fact that, in the top-gate structure, the dielectric is printed

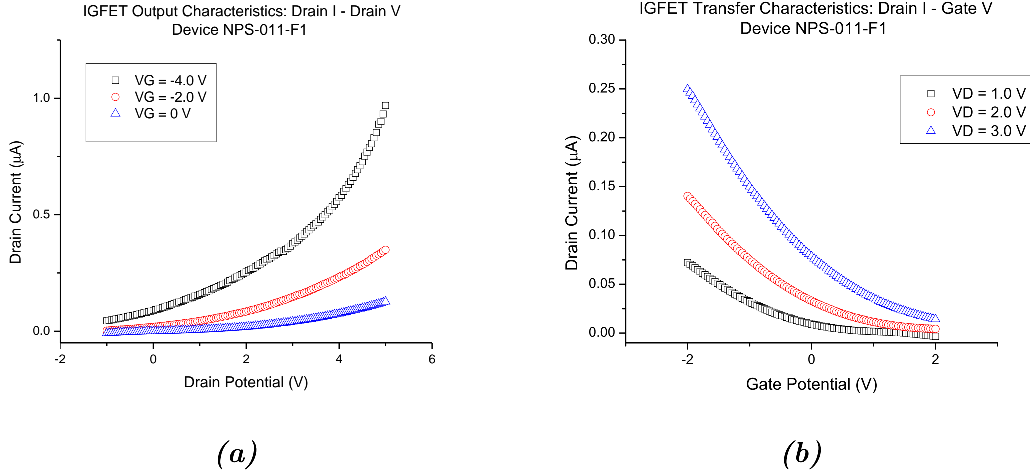
on top of the silicon. Since the printed silicon layers are relatively rough, as shown in section 3.3.2, printing in this order may adversely affect the final integrity of the insulating layer. Conversely, with the bottom-gate structure, the dielectric is printed on top of the relatively smooth silver gate layer and allowed to cure before the silicon is printed. For these reasons, the production of IGFETs was mainly focussed on the bottom-gate devices, from which the results to be presented here will be drawn.

Table 5.1: *Material configurations of IGFET devices presented in this chapter. DuPont 5000 is a silver ink used for the electrodes. DuPont 8153 is a high-k dielectric used for the gate insulator.*

Sample ID	Electrode ink	Active layer ink	Insulator ink
NPS-011-F1	DuPont 5000	n-type Si	DuPont 8153
PNS-009-F1	DuPont 5000	p-type Si	DuPont 8153

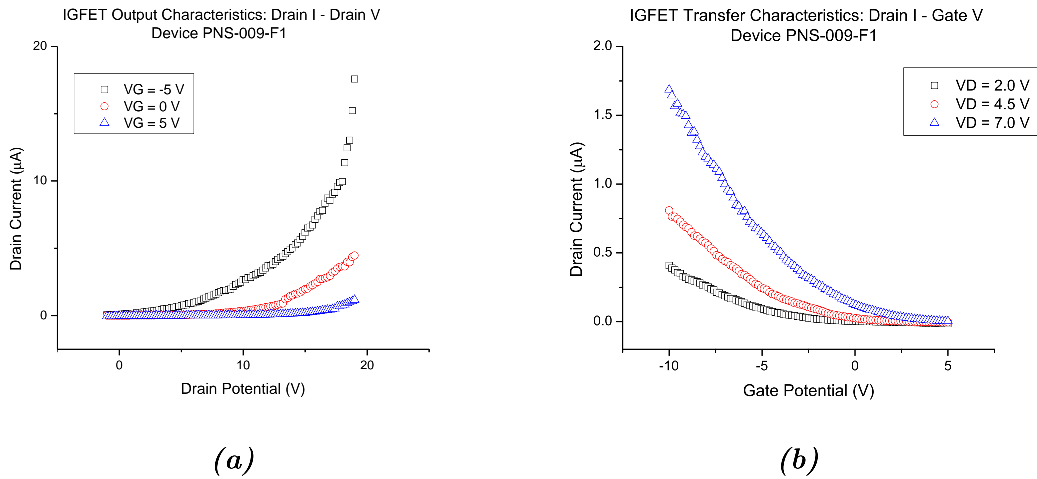
Figures 5.2 shows the output and current-voltage transfer characteristics of device NPS-011-F1, a bottom-gate IGFET printed with highly doped n-type silicon. For potentials (both drain and gate) of the order of a few volts, the device operates with drain currents in the microampere range. The output characteristics show that for low applied drain potential, the drain current is small. Increasing the applied drain potential results in an increase in the differential conductance $\mathrm{d}I_D/\mathrm{d}V_D$ as well as an exponential increase in the drain current. The application of a negative gate potential enhances the drain current. This IGFET does not go into saturation within the examined regimes of potential. The output and current-voltage transfer characteristics of device PNS-009-F1, a bottom-gate IGFET printed with highly doped p-type silicon, are shown in Figure 5.3. This device was tested over a higher range of potentials, as compared with the n-type IGFET, which resulted in higher drain currents. However, the behaviour of the two devices is qualitatively very similar. This can be easily seen by comparing the relative shapes of the two sets of corresponding characteristic curves. The curves are similar, although the current and potential levels are different. Interestingly, the doping type of the silicon

feedstock appears to have no effect on the electrical behaviour: devices printed with n-type and p-type silicon behave similarly.



(a) ***(b)***

Figure 5.2: *Characteristics of device NPS-011-F1, a fully printed bottom-gate IGFET fabricated with n-type silicon. (a) Output characteristics for gate potentials from -4 V to 0 V. (b) Current-voltage transfer characteristics for drain potentials from 1 V to 3 V.*



(a) ***(b)***

Figure 5.3: *Characteristics of device PNS-009-F1, a fully printed bottom-gate IGFET fabricated with p-type silicon. (a) Output characteristics for gate potentials from -5 V to +5 V. (b) Current-voltage transfer characteristics for drain potentials from 2 V to 7 V.*

An important figure of merit of an insulated-gate field-effect transistor is the gate leakage current, which should ideally be low. In order to evaluate the gate leakage in the printed IGFETs, an additional characteristic, beyond the output and current-voltage characteristic, has been measured. This is the current-current transfer characteristic, which is given by the drain current as a function of the gate current. Figure 5.4 shows the results of this measurement for the p-type IGFET (device PNS-009-F1) for drain potentials 2.0 V, 4.5 V and 7.0 V. When the gate current is negative, there is a nonlinear drain current response, which increases with increasing drain potential. The drain current appears to saturate at roughly 0.5 μA for drain potential 2.0 V. When the drain potential is increased to 4.5 V, the drain current response increases, which suggests there is increased leakage current passing through the dielectric. This effect is even stronger for drain potential 7.0 V, where the drain current response retains a slight concave-down curvature, but is nearly linear with unit gain, suggesting that the dielectric is conducting and that the device is in breakdown.

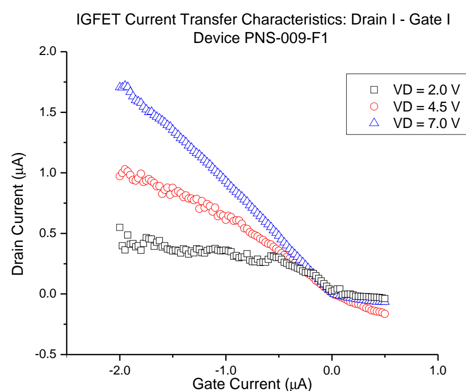


Figure 5.4: *Current-current transfer characteristics of device PNS-009-F1, a fully printed bottom-gate IGFET fabricated with p-type silicon, for drain potentials from 2 V to 7 V.*

The current-current transfer characteristics exhibit an unusual property. For all values of the drain potential, there is a discontinuous shift in the gradient of the transfer curve when the direction of the gate current changes. In particular, when

the gate current changes from negative to positive, the gradient $\mathrm{d}I_D/\mathrm{d}I_G$ and the drain current response both decrease. It appears as though the device preferentially conducts current in the drain, depending on the direction of the current in the gate. The effect is most noticeable with $V_D = 7.0$ V, for which the device also showed the highest gate leakage current through the dielectric.

There are indications from the results that these devices function as FETs, which implies, in agreement with earlier findings [100], that the nanoparticulate silicon has the potential to enable printed transistors. However, the IGFETs exhibit significant gate leakage currents, particularly at higher drain potentials. This suggests that the gate insulator is not performing well. Furthermore, the current-current transfer characteristics yielded the unexpected result that there is a strong asymmetry in the drain current response, with respect to the direction of the gate current. To further study this effect, a device structure with no gate insulator has been investigated. The results of the characterisation of this device, the current switching transistor, will be presented in the next section.

5.3 Current switching transistor results

The electrical characterisation of the current switching transistors (CSTs) consisted of preliminary bench tests followed by more detailed studies using the Keithley 4200 SCS. The results of these tests, for the three CST design variants, are presented here.

5.3.1 Asymmetric CST

The first version of the CST to be produced and tested was the asymmetric CST, the design of which is shown in Figure 4.3. The DC current-voltage characteristics of these devices were measured as described in section 3.4.1. Figure 5.5 shows a set of current-voltage transfer characteristics measured for device P-08-J14, which was printed with highly doped p-type silicon and which is representative of the

asymmetric CSTs. The current-voltage transfer curves, collector current versus base potential, are plotted for a range of different collector potentials. Generally, the collector current increases nonlinearly with increasing negative base potential. For a fixed base potential, the collector current is enhanced by an increase in the

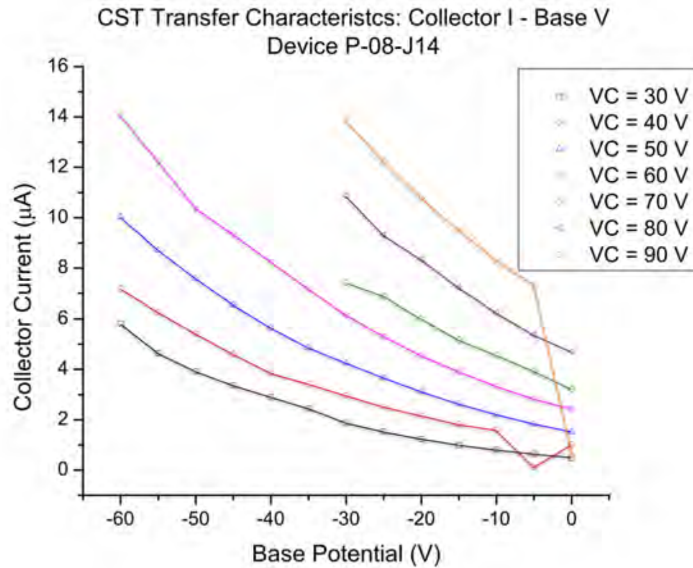


Figure 5.5: *Bench test results show the transfer characteristics of an asymmetric CST printed with silver electrodes and highly doped p-type silicon, device P-08-J14.*

positive collector potential. The collector current is lower than would be expected from the trends at two points: when the collector potential is 40 V and the base potential is -5 V, as well as when the collector potential is 90 V and the base is unbiased. Apart from these anomalies, the trends are qualitatively similar to the behaviour observed for the current-voltage transfer characteristics of the IGFETs. The two device types differ quantitatively, in that for the IGFETs, applied potentials of a few volts resulted in currents in the microampere range. However, for the asymmetric CST, microampere range currents require the application of potentials in the range of several tens of volts. This suggests that the semiconducting region of the asymmetric CST is significantly more resistive than that of the IGFET. The ranges of base potential and collector potential which were available in the bench tests were limited, as illustrated in Figure 3.10. This is the reason, for ex-

ample, that the magnitude of the base potential was limited to 30 V for collector potentials greater than 60 V.

To more fully investigate the CSTs, it was necessary to make use of the higher voltages and more accurate measurements made available by the Keithley 4200 SCS. This was used to measure the current-current and current-voltage transfer characteristics, I_C vs I_B and I_C vs V_B, of the CSTs as described in section 3.4.2. The present experiments employed higher potential differences than those of the initial bench tests, such that typical voltage bias levels applied to the collector, relative to the emitter, were in the range 80 V - 120 V. Maximum base potentials were limited to ±200 V by the apparatus. Table 3.2 lists the devices which will be presented.

Figure 5.6a shows the current-current transfer characteristics of an asymmetric CST printed with highly doped n-type silicon on silver electrodes (device N-02-J03).

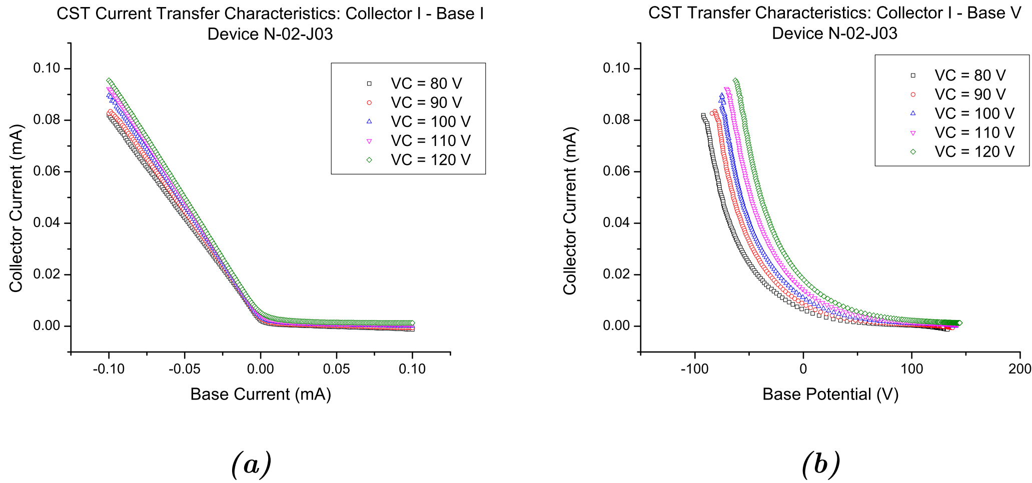
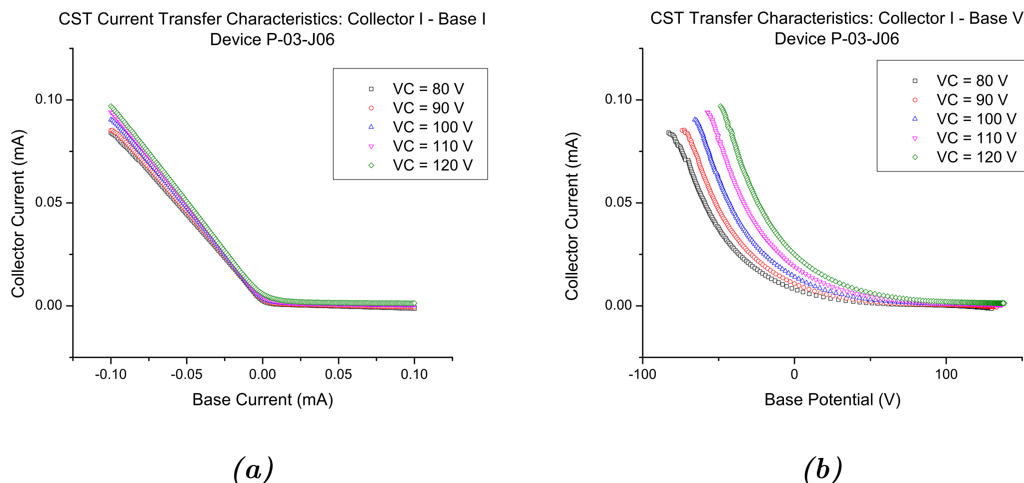


Figure 5.6: *Transfer characteristics of an asymmetric CST printed with silver electrodes and highly doped n-type silicon, device N-02-J03: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

The results reveal that the collector current response has two distinct characters, depending on the direction of the base current. These are visible in the graph as two regions where the gradients are approximately linear, with a transition between them at zero base current. If the current injected at the base terminal is negative, i.e. if $I_B < 0$, a comparable positive current is measured at the collector, resulting in a current-current transfer gradient of $I_C/I_B \approx -1$. However, if the direction of the injected base current is reversed, such that $I_B > 0$, the current measured at the collector is comparatively small, resulting in a gradient of $I_C/I_B \approx 0$.

The observed response of the collector current as a function of the base current represents a type of switching effect, whereby the collector current can be switched on or off by selecting the direction of the base current. It is precisely this behaviour for which the new device has been named the current switching transistor. To illustrate the strength of this switching effect, Figure 5.6a shows that a base current of $I_B = -50$ μA results in a collector current of $I_C \approx 50$ μA, while for a base current of $I_B = 50$ μA the collector current is $I_C \approx 1$ μA. The current measured at the collector has been reduced by a factor of 50 with the change in direction of the base current. It is useful here to consider the base and collector currents respectively as input and output. For positive input, the output is low and the device can be said to be in the *off* state, while for negative input, the output is high and it is in the *on* state.

The current-voltage transfer characteristics, shown in Figure 5.6b, illustrate the switching behaviour from an alternative viewpoint. Rather than being concerned with the current injected at the base, this characteristic indicates the effect on the output current of varying the potential applied to the base terminal. The results show that for base potentials $V_B \approx 100$ V, the collector current is small, and the device is in the off state. Reducing the base potential results in a nonlinear increase in the collector current, which appears to be exponential in character. Additionally, the collector current is enhanced by increasing the collector potential, which was also observed in the behaviour of the IGFETs. The precise nature of the $I_C - V_B$ relationship in the CST will be examined in the next chapter.

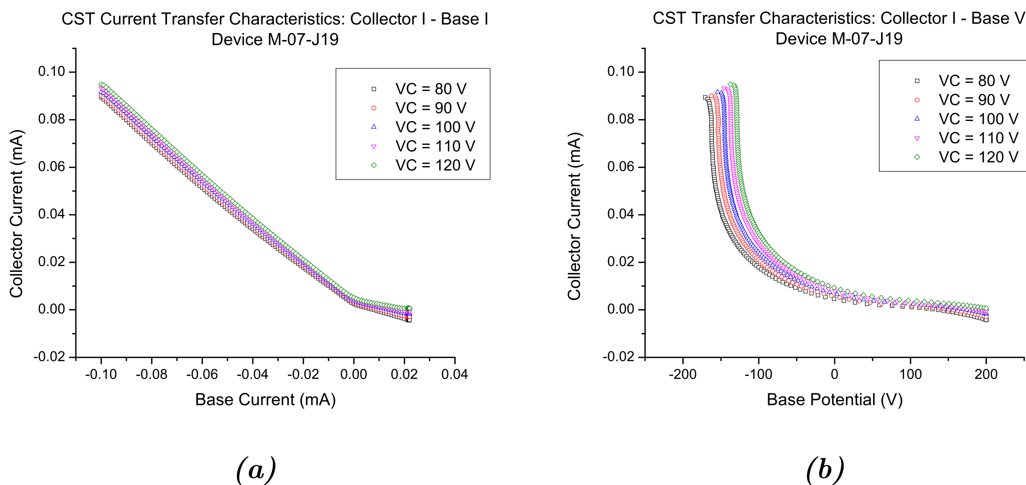


(a) ***(b)***

Figure 5.7: *Transfer characteristics of an asymmetric CST printed with silver electrodes and highly doped p-type silicon, device P-03-J06: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

Figure 5.7 shows the transfer characteristics of an asymmetric CST printed with highly doped p-type silicon (device P-03-J06). The switching effect is apparent here and the behaviour is very similar, both qualitatively and quantitatively, to that of the n-type device discussed above. The most significant difference between these results is that in the case of device N-02-J03, the current-voltage transfer curves for the different collector potentials are more tightly grouped, with higher maximum gradients, while for device P-03-J06 they are more spread out, with lower maximum gradients.

Figure 5.8 shows the transfer characteristics of an asymmetric CST printed with 2503 grade silicon (device M-07-J19). The switching effect is visible in the current-current transfer function in Figure 5.8a, but there are significant differences between this behaviour and that exhibited by the highly doped n- and p-type devices in Figures 5.6a and 5.7a. For the 2503 grade silicon device, the collector current response has a gradient of approximately -1 in *on* mode (where the base current is negative), as expected. However, for positive base currents, the gradient of the collector current does not reduce by as large a factor as was observed for the n- and p-type devices. That is, for the 2503 grade silicon, the device does not switch



(a) ***(b)***

Figure 5.8: *Transfer characteristics of an asymmetric CST printed with silver electrodes and 2503 grade silicon, device M-07-J19: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

off as strongly. A further significant difference is related to the range of current injected into the base. Recall from section 3.4.2 that the CSTs were tested over a programmed range of base currents from -0.1 mA to + 0.1 mA. Now, it can be seen in Figure 5.8a that the maximum base current during the measurement was approximately 0.02 mA. The current-voltage transfer characteristic in Figure 5.8b shows that the corresponding base voltage was 200 V. At this point, the Keithley 4200 entered compliance mode, limiting the base potential to its pre-set maximum of 200 V, as was illustrated in Figure 3.11b. This result shows that the semiconducting channel in the 2503 grade silicon device is significantly more resistive than those in the n- and p-type devices, which are similar to each other.

Figure 5.9 shows the transfer characteristics of an asymmetric CST printed with TCO electrodes and highly doped p-type silicon, device TCO-P-04-J12. This device, like those which have previously been discussed, switches collector current with sign change of the base current. Its performance characteristics may be described as being in between those of the highly doped silicon-on-silver and the 2503 grade silicon-on-silver devices. Similarly to the former, this highly doped p-type silicon-on-TCO device shows a large change in the current-current gradient

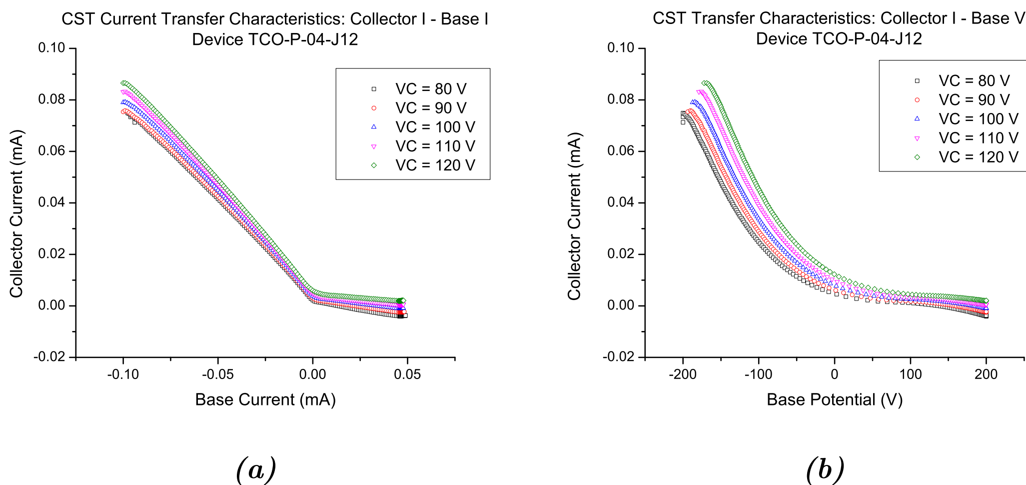
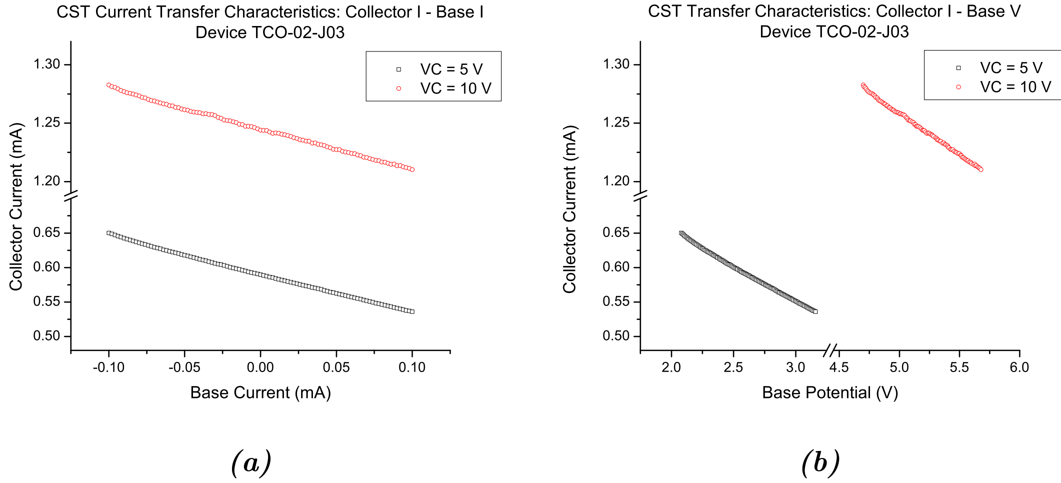


Figure 5.9: *Transfer characteristics of an asymmetric CST printed with TCO electrodes and highly doped p-type silicon, device TCO-P-04-J12: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

at approximately zero base current. However, the off-currents are not quite as low as for the p-type silicon with silver. This is particularly true for the lower collector potentials. For higher collector potentials, such as $V_C = 120$ V, the switching effect strengthens, as signified by the very low gradient of the collector current response. This is highly reminiscent of the IGFET current-current transfer shown in Figure 5.4, in which a similar behaviour to the present switching emerged for higher drain potentials. On the other hand, as with the 2503 grade silicon-on-silver device, the Keithley SCS enters voltage compliance mode before the base current reaches 0.1 mA. This is likely to be due to the high resistance of the TCO electrodes compared with the silver electrodes.

Finally, Figure 5.10 shows the transfer characteristics of an asymmetric CST printed with silver electrodes and TCO as the active layer (device TCO-02-J03). This device does not exhibit the switching behaviour seen previously. The lack of switching is characterised by uniform gradients in both the current-current and current-voltage transfer functions. In particular, there is no perceptible shift in the collector current response when the base current changes direction.



(a) *(b)*

Figure 5.10: *Transfer characteristics of an asymmetric CST printed with silver electrodes and a TCO active layer, device TCO-02-J03: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

The switching behaviour of the asymmetric CST appears to be independent of the doping type of the semiconducting body. This is an indication that the mechanisms by which the switching occurs are distinct from those involved in the operation of conventional transistors. The resistivity of the semiconducting channel has a qualitative effect on the nature of the switching, and on the degree to which the device switches off the collector current for positive base currents. Furthermore, the switching behaviour persists when the devices are printed with TCO electrodes. However, the switching does not occur when the active channel is printed with another semiconductor, TCO. These observations imply that the processes governing this current switching behaviour are related to the nature of the silicon nanoparticle network. In the following section, the performance of the two CST design variants will be presented.

5.3.2 CST design variants: symmetric and interdigitated

Two CST variants, the symmetric CST and the interdigitated CST, were characterised in the same manner as the asymmetric CST, as described in section 3.4.2. However, the test parameters were adjusted to suit expected operating conditions of the different devices. Table 3.3 lists the devices which will be presented. Figure 5.11 shows the transfer characteristics of a symmetric CST printed with highly doped p-type silicon (device JTA3-P-02). This device exhibits a sharp switching behaviour, characterised by rapid change in the gradient of the current-current transfer function, as well as low collector currents for positive base current. The sharpness of the switching manifests itself in the current-voltage transfer characteristic as large gradients in the on mode.

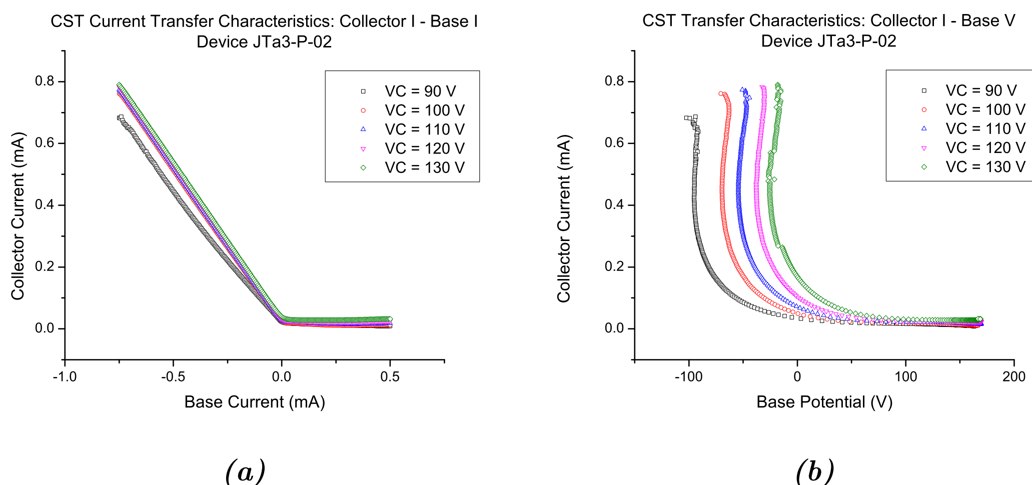


Figure 5.11: Transfer characteristics of a symmetric CST, printed with silver electrodes and highly doped p-type silicon, device JTA3-P-02: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.

Figure 5.12 shows the transfer characteristics of an interdigitated CST, printed with highly doped p-type silicon (device Inter-P-2-8). The switching behaviour is present, as shown by the change in gradient of the current-current transfer at zero base current. However, the switching is more poorly defined, to the extent

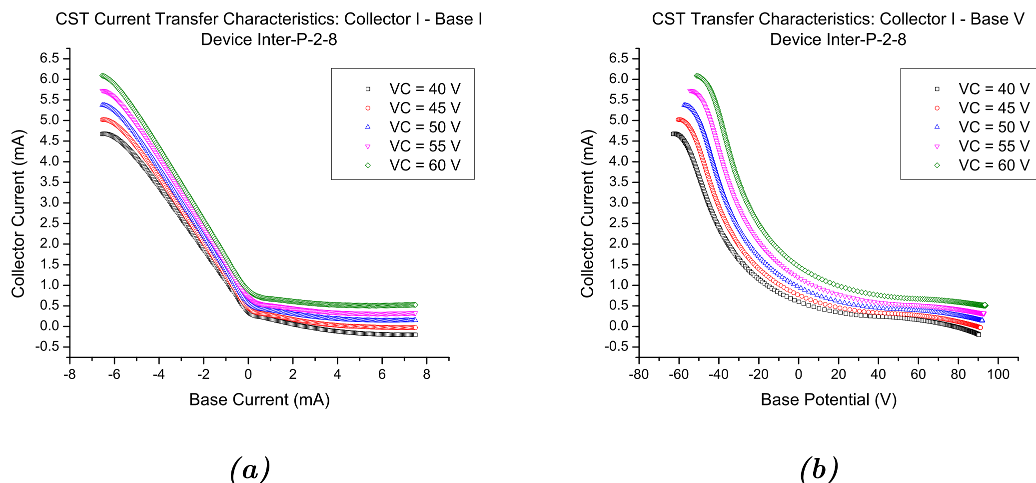


Figure 5.12: *Transfer characteristics of an interdigitated CST, printed with silver electrodes and highly doped p-type silicon, device Inter-P-2-8: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

that the collector currents in the off-mode are significant. Furthermore, there is strong variation of collector current response with changing collector voltage. As was observed for the asymmetric CST with TCO contacts, and for the IGFET before that, an increase in the collector potential enhances the collector current, as well as strengthening the switching behaviour. The last point is reinforced by noting that in the off-mode, the current-current gradient is smallest for the highest collector potential.

It has been shown that the three varieties of CST exhibit strong behavioural similarity, although in certain cases this is only qualitative. The principal distinguishing factor is that the three device types operate in different current ranges. In the case of the asymmetric CST, it was observed that applied base potentials of 200 V resulted in base currents of the order of 0.1 mA. The currents observed in the symmetric CST are higher, at the level of 0.5 mA, and higher still in the interdigitated CST, at approximately 7 mA. These differences may be explained in terms of the electrode designs. An examination of the contacts in Figures 4.3, 4.4 and 4.5 reveals that the electrodes in the symmetric design are closer to each other than in the asymmetric design. Other factors, such as semiconductor material, be-

ing equal, this difference in electrode spacing results in lower channel resistances in the symmetric design. The interdigitated electrodes of the third design result in dramatically wider channels between the contacts and again, even lower resistances. It is not surprising, therefore, that higher currents were observed for these designs.

The insulated-gate field-effect transistors were shown to have limited FET functionality, though they suffer from considerable gate leakage currents. An unexpected behaviour emerged in the IGFETs, whereby it was observed that the drain current was reduced by changing the gate current from negative to positive. This effect gained in strength for increased drain potentials, which was linked to an insulation failure of the dielectric layer. Following these results, the devices which would later be named current switching transistors, having no dielectric layers, were investigated and found to exhibit an even stronger switching behaviour, whereby the collector current may be switched on or off by setting the direction of the base current. This switching effect occurs in silicon nanoparticle devices, independent of the doping type, but in a way that seems to be related to the open-circuit resistance of the semiconductor. In the next chapter, a detailed analysis and discussion of these results will be presented.

Chapter 6

Analysis and discussion

In this chapter, the electrical characteristics of the current switching transistor will be more closely examined, with a view toward explaining the observed switching behaviour in terms of the underlying physical processes. To accomplish this, charge transport within the printed silicon will be considered, which will lead to the proposal and testing of a model and an equivalent circuit for the device.

6.1 Electrical behaviour of the printed silicon

The electrical behaviour of silicon nanoparticle networks has been investigated by measuring the current-voltage characteristics of samples comprising two silver electrodes printed on paper and bridged by a printed layer of silicon. The results of such a test, carried out at a temperature of 300 K on a sample which was printed with 2503 grade silicon, were presented in section 5.1. Recall that the IV characteristic of the printed silicon is nonlinear and symmetrical, as was shown in Figure 5.1. The nonlinearity of the current-voltage response, together with its symmetry, suggest that the electrical behaviour of the printed silicon network could be modelled as an equivalent circuit consisting a pair of anti-parallel diodes, such as those shown in Figure 6.1. The initial motivation for this model was phenomenological:

the nonlinearity suggests a diode-like behaviour, while the inclusion of a second diode, anti-parallel to the first, satisfies the symmetry. Subsequent work has shown that this is a good model for the printed nanoparticulate silicon. Charge transport within the printed network has been shown to be dominated by inter-particle hopping, with depletion layers forming at the particle-particle interfaces. These junctions between the particles give rise to the diode-like behaviour [103].

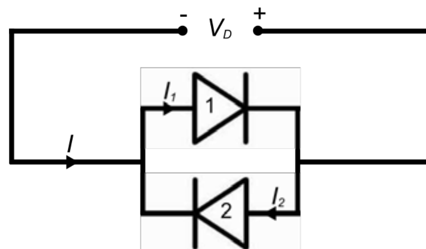


Figure 6.1: *A model circuit for a printed silicon layer consists of two diodes connected in anti-parallel. The applied voltage is V_D and the main current in the circuit is I. The currents in the circuit are I, I_1 and I_2.*

If the anti-parallel arrangement of diodes is biased by a voltage V_D, as shown in Figure 6.1, then diode 1 will be forward-biased and diode 2 will be reverse-biased. In order for this model to be consistent with the observed electrical behaviour of the printed silicon and in particular, for the current in the model circuit not to go into saturation, the applied voltage should be sufficiently high for the reverse-biased diode to be in reverse breakdown condition.

The current I through a diode biased by a voltage V_D is given by the Shockley diode equation:

$$I = I_S \left(\mathrm{e}^{eV_D/nkT} - 1 \right), \tag{6.1}$$

where I_S is the reverse bias saturation current, e is the electronic charge, k is the Boltzmann constant, T is the absolute temperature, and n is the ideality or quality factor. This equation can be used to express the currents I_1 and I_2 through diodes 1 and 2 respectively as

$$I_1 = I_S \left(\mathrm{e}^{eV_D/nkT} - 1 \right), \tag{6.2}$$

$$\text{and} \quad I_2 = -I_S \left(\mathrm{e}^{-eV_D/nkT} - 1 \right), \tag{6.3}$$

where it has been assumed that the the reverse saturation currents I_S are the same for both diodes, since the currents flow through the same material. The difference in sign signifies that I_1 and I_2 are in opposite directions.

The current I through the circuit is given by the sum of the two anti-parallel currents:

$$I = I_1 + I_2 \tag{6.4}$$

$$\Rightarrow I = I_S\left(\mathrm{e}^{eV_D/nkT} - 1\right) - I_S\left(\mathrm{e}^{-eV_D/nkT} - 1\right) \tag{6.5}$$

$$\Rightarrow I = I_S\left(\mathrm{e}^{eV_D/nkT} - \mathrm{e}^{-eV_D/nkT}\right). \tag{6.6}$$

Equation (6.6) represents the current through the anti-parallel combination of diodes as a function of the applied voltage. To assess the applicability of the diode model to the printed silicon system, a least-squares fit of this function to the IV curve in Figure 5.1, which was measured at 300 K as described in section 5.1, has been performed. The fit, shown in Figure 6.2, resulted in a reduced χ^2 value of 2.25×10^{-12} and an adjusted R^2 value of 0.99936, both of which indicate that the model is, to a first approximation, a reasonable representation of the material system.

The parameter values extracted from the fit were a reverse saturation current of $I_S = 24.34 \pm 0.86$ μA and an ideality factor of $n = 2216 \pm 54$. The latter value seems surprisingly large when thought of in the context of typical diodes, for which the ideality factors tend to be in the range $n = 1 - 2$. However, conduction paths through the printed silicon consist of a large number of particle-particle interfaces, which present potential barriers to charge transport. If a voltage V_D is applied across a conduction path containing n barriers, then the potential energy drop across each barrier will be proportional to $\mathrm{e}^{eV_D/nkT}$. In this way the large ideality factor obtained from the fits may be interpreted as a scaling down of the applied potential, due to the many interfaces, as compared with a single ideal diode [54, 103].

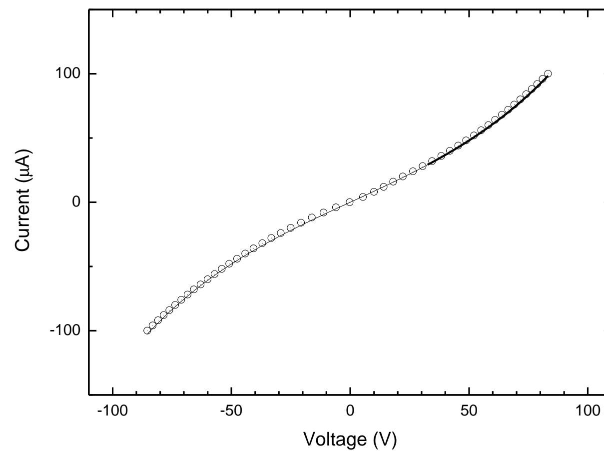


Figure 6.2: *Current-voltage characteristics of a layer of 2503 grade silicon nanoparticles at 300 K. The solid line is a least-squares fit to the function of equation 6.6, representing anti-parallel diodes.*

6.2 Modelling the current switching transistor

In this section the anti-parallel diode model of the printed silicon material system shall be used to construct a model circuit for the current switching transistor. As discussed before, the CST consists of three electrodes connected by printed silicon. Therefore, in applying the model of the printed silicon system, the device will be considered to have three terminals, with each pair of contacts connected by two anti-parallel diodes, as illustrated in Figure 6.3. In this way, the silicon channels between each pair of contacts are treated as being distinct from one another, each having similar electrical characteristics to those discussed in the previous section.

To explore the predicted behaviour of this model circuit, it is necessary to set it into an appropriate electrical context. In measuring the CST transfer characteristics presented in the previous chapter, the emitter terminal was grounded, with the collector held at at fixed positive potential while varying the base potential. In Figure 6.3 the CST model circuit is connected in an equivalent manner to that

used in the measurements of the printed devices. The emitter (E) is connected to ground, while the base (B) and collector (C) are at potentials V_B and V_C respectively. When a potential difference is applied across any pair of terminals, then there is a current between them. These internal currents, indexed by the terminals between which they flow, are I_{CB}, I_{CE} and I_{EB}. The external currents measured at the base and collector terminals are I_B and I_C respectively.

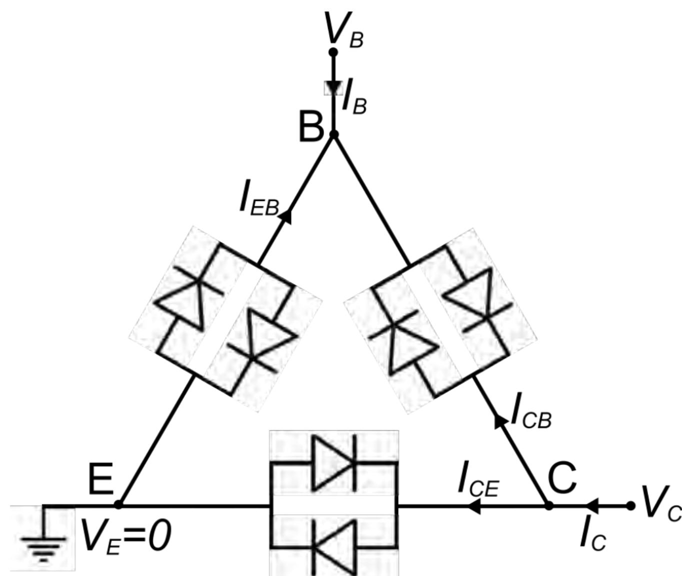


Figure 6.3: *Model circuit of the CST, consisting of three electrodes, with each pair of these connected by an anti-parallel pair of diodes, shown here connected to an external circuit. In this arrangement the emitter (E) is grounded while the base (B) and collector (C) are at potentials V_B and V_C respectively. I_B and I_C are the external currents, while I_{CB}, I_{CE} and I_{EB} are the internal currents.*

In order to test the model, a function is required to fit to the data. Using simple circuit analysis and the known behaviour of the anti-parallel diodes, the current-voltage transfer function $I_C(V_B)$ of the model circuit can be obtained. The collector current I_C is given by Kirchhoff's junction rule as being equal to the sum of the two internal currents I_{CB} and I_{CE}:

$$I_C = I_{CB} + I_{CE}. \tag{6.7}$$

Now, each of these internal currents flows through a pair of anti-parallel diodes and, from the discussion in the previous section, the current through anti-parallel diodes is a function of the voltage applied across them, given by equation (6.6). Substituting the internal currents and the potential differences applied across the relevant electrode pairs into this equation, the following equations for the internal currents I_{CE} and I_{CB} are obtained:

$$I_{CB} = I_{CB_S}\left(\mathrm{e}^{e(V_C-V_B)/nkT} - \mathrm{e}^{-e(V_C-V_B)/nkT}\right), \tag{6.8}$$

$$I_{CE} = I_{CE_S}\left(\mathrm{e}^{e(V_C-V_E)/nkT} - \mathrm{e}^{-e(V_C-V_E)/nkT}\right), \tag{6.9}$$

where I_{CB_S} and I_{CE_S} are reverse saturation currents. Finally substituting equations (6.8) and (6.9) into equation (6.7) gives the collector current I_C as a function of the voltage-dependent currents through the collector-emitter and collector-base channels, which is the current-voltage transfer function of the model circuit:

$$\begin{aligned} I_C &= I_{CB_S}\left(\mathrm{e}^{e(V_C-V_B)/nkT} - \mathrm{e}^{-e(V_C-V_B)/nkT}\right) \\ &+ I_{CE_S}\left(\mathrm{e}^{e(V_C-V_E)/nkT} - \mathrm{e}^{-e(V_C-V_E)/nkT}\right). \end{aligned} \tag{6.10}$$

Equation (6.10) has been used as a fitting function to the measured CST current-voltage transfer data. The results of these fits shall be discussed in the next section.

6.3 Fitting the CST model

A symplectic least-squares procedure has been used to fit the model current-voltage transfer function to the measured transfer characteristics. It should be noted that although the model function, shown in equation (6.10), includes several elements, the sole independent variable is the collector potential V_B. Since the emitter is always grounded during the measurements, the emitter potential V_E is identically zero, while the collector potential V_C is varied between measurements, but remains constant for the duration of a given test. The Boltzmann constant k and electronic charge e are fundamental constants, and the temperature T remains constant

throughout a measurement. The internal reverse saturation currents I_{CB_S} and I_{CE_S} as well as the ideality factor n are fitting parameters.

The fitting results for an asymmetric CST printed with p-type silicon are shown in Figure 6.4. In order to ensure that the model function fits are clearly visible, 80% of the original data points for each collector potential curve have been omitted. From the plots it appears that the model fits the device behaviour reasonably well, particularly for the higher collector potentials. Table 6.1 shows the extracted parameter values as well as the goodness of fit metrics, χ^2 and R^2, which indicate that the fit consistently improves with increasing collector potential. The reverse saturation currents I_{CB_S} and I_{CE_S} range from approximately 900 nA and 130 nA at V_C = 80V to approximately 690 nA and 44 nA, respectively, at V_C = 120 V. The mean ideality factor was 1349 with a standard deviation of 26.

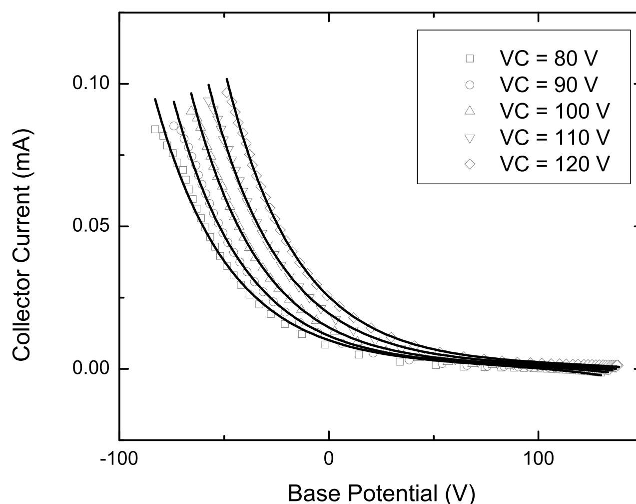


Figure 6.4: *Current-voltage transfer characteristics of an asymmetric CST, printed with highly doped p-type silicon (device P-03-J06). The solid lines are least squares fits of the model transfer function.*

The compatibility of the model with the observed switching behaviour is perhaps better demonstrated by plotting the fitted collector current values as a function of the base current along with the original data, as shown in Figure 6.5. Again,

Table 6.1: *Results of fitting model current-voltage transfer function to characteristics of an asymmetric CST (device P-03-J06): extracted fit parameters I_{CB_S}, I_{CE_S} and n and goodness of fit metrics χ^2 and R^2.*

V_C (V)	I_{CB_S} (nA)	I_{CE_S} (nA)	n	χ^2	R^2
80	913 ± 39	133 ± 16	1394 ± 14	3.18816E-12	0.99598
90	733 ± 21	84.9 ± 6.9	1342 ± 9	1.23654E-12	0.9985
100	669 ± 15	62.5 ± 3.7	1323 ± 6	6.72231E-13	0.99925
110	712 ± 16	52.9 ± 2.9	1345 ± 6	6.72773E-13	0.99929
120	693 ± 13	44.0 ± 1.8	1343 ± 5	4.79487E-13	0.99951

80% of the original data points have been omitted for clarity. While there is some noticeable deviation from the data for a highly negative base current, the model agrees well with the data and tracks it smoothly through the transition region of low base current.

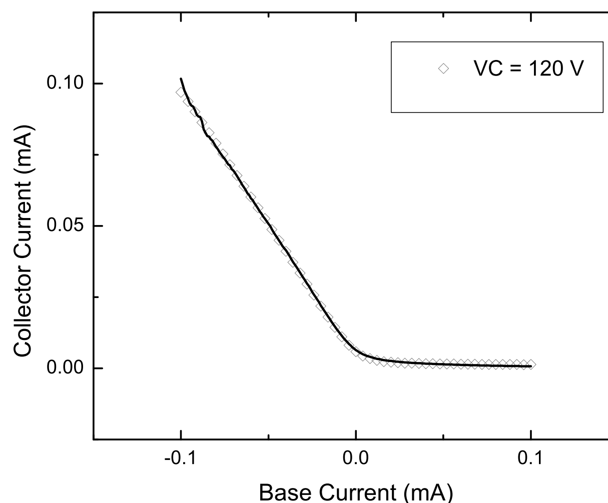


Figure 6.5: *Current-current transfer characteristics of an asymmetric CST (device P-03-J06) for a collector potential of 120 V. The solid line represents the collector current values obtained from the current-voltage fit, plotted against base current.*

Similar results were obtained by fitting the model to the characteristics of asymmetric CST devices printed with n-type silicon. Typical fitted curves are plotted in Figures 6.6 and 6.7, with the corresponding extracted fitting parameters presented in Table 6.2. Broadly, these show the same type of behaviour, with two notable differences being that the n-type devices exhibit lower reverse saturation currents and lower ideality factors, the latter of which had a mean value of 1130 with a standard deviation of 28.

These results indicate both that the anti-parallel diode model is a good description of the behaviour of the printed silicon nanoparticle network and that it is the non-linear current-voltage response which leads to the switching behaviour of the CSTs.

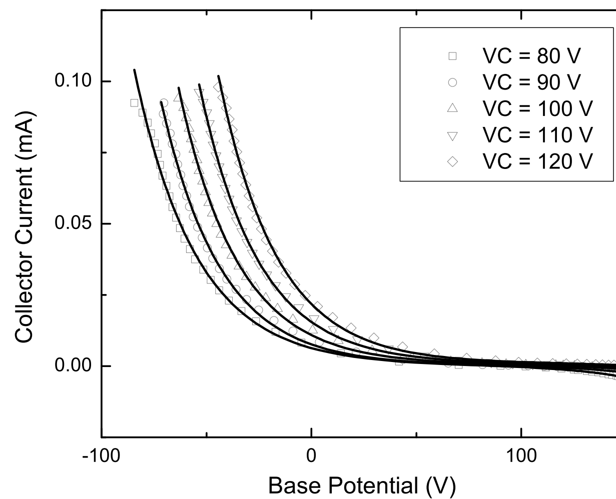


Figure 6.6: *Current-voltage transfer characteristics of an asymmetric CST, printed with highly-doped n-type silicon (device N-15-J05). The solid lines are least squares fits of the model transfer function.*

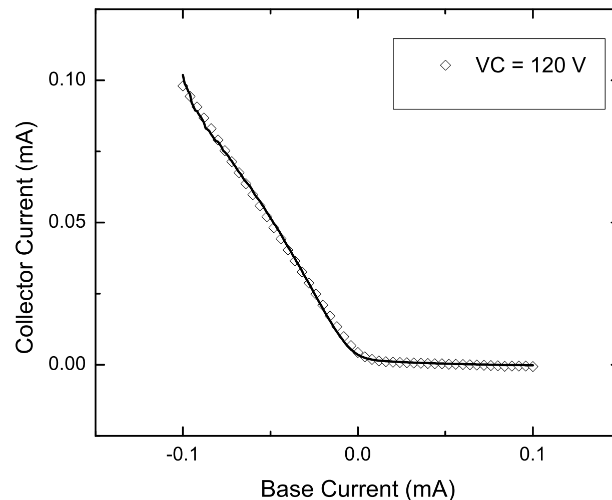


Figure 6.7: *Current-current transfer characteristics of an asymmetric CST (device N-15-J05) for a collector potential of 120 V. The solid line represents the collector current values obtained from the current-voltage fit, plotted against base current.*

Table 6.2: *Results of fitting model current-voltage transfer function to characteristics of an asymmetric CST (device N-15-J05): extracted fit parameters* I_{CB_S}, I_{CE_S} *and* n *and goodness of fit metrics* χ^2 *and* R^2.

V_C (V)	I_{CB_S} (nA)	I_{CE_S} (nA)	n	χ^2	R^2
80	415 ± 15	18.5 ± 8.4	1179 ± 9	1.99621E-12	0.99796
90	310 ± 10	10.0 ± 3.9	1123 ± 7	1.16819E-12	0.99877
100	304 ± 9	15.2 ± 2.4	1121 ± 6	8.91387E-13	0.99908
110	299 ± 9	16.0 ± 1.8	1117 ± 6	9.50699E-13	0.99905
120	288 ± 9	13.9 ± 1.2	1111 ± 6	9.20443E-13	0.9991

6.4 Modifying the CST model

The current switching transistor has heretofore been modelled as a triangular network of anti-parallel diode pairs, which has been shown to fit the observed behaviour reasonably well. However, in such a physical system there will be elements which contribute to the electrical resistance. These include the silicon itself and the metal-semiconductor junctions, as well as components of the measurement system, such as the connecting leads. The model may therefore be improved upon by taking into account the these resistances present in the system. Figure 6.8 shows an extended model circuit which combines the triangular anti-parallel diode network with resistances R_B, R_C and R_E in series with the base, collector and emitter contacts respectively. These represent the combined series resistances due to the factors mentioned above.

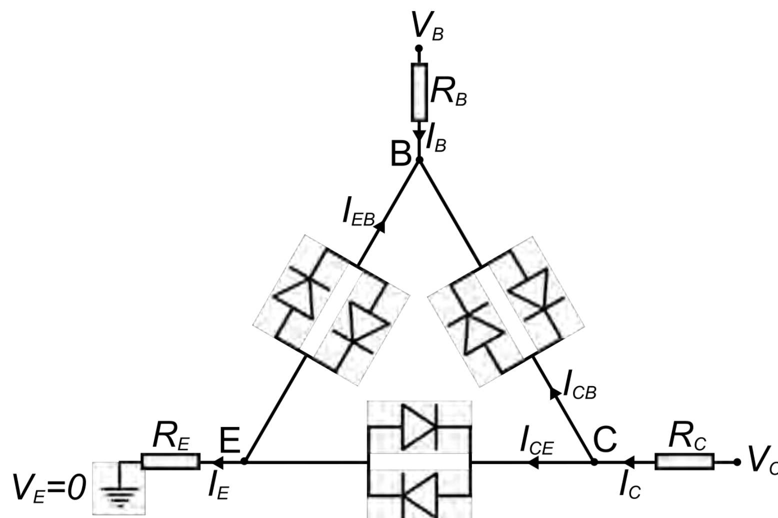


Figure 6.8: *CST model circuit, extended to include series resistances R_B, R_C and R_E.*

In the original model, the voltage applied across an anti-parallel diode pair is simply the difference between the potentials of the relevant terminals. For example, $\Delta V_{D_{CB}} = V_C - V_B$. In the new model, introduction of the resistances results in the reduction of the applied potential differences by amounts equivalent to the drops

in voltage across each resistor, as follows:

$$\Delta V_{D_{CB}} = V_C - V_B - I_C R_C - I_B R_B, \tag{6.11}$$

$$\Delta V_{D_{CE}} = V_C - V_E - I_C R_C - I_E R_E. \tag{6.12}$$

The new model transfer function is obtained by substituting these diode voltages into equation (6.10), yielding:

$$\begin{aligned} I_C &= I_{CB_S}\left(\mathrm{e}^{e(V_C - V_B - I_C R_C - I_B R_B)/nkT} - \mathrm{e}^{-e(V_C - V_B - I_C R_C - I_B R_B)/nkT}\right) \\ &+ I_{CE_S}\left(\mathrm{e}^{e(V_C - V_E - I_C R_C - I_E R_E)/nkT} - \mathrm{e}^{-e(V_C - V_E - I_C R_C - I_E R_E)/nkT}\right). \end{aligned} \tag{6.13}$$

Equation (6.13) is not directly usable as a fitting function, since it depends explicitly on the emitter current, I_E, which was not measured due to this terminal being grounded. However, this may be overcome by noting that there is no current source or sink within the triangular network and therefore the emitter current is given by the sum of the base and collector currents:

$$I_E = I_C + I_B. \tag{6.14}$$

Substituting equation (6.14) into equation (6.13) yields a usable fitting function:

$$\begin{aligned} I_C &= I_{CB_S}\left(\mathrm{e}^{e(V_C - V_B - I_C R_C - I_B R_B)/nkT} - \mathrm{e}^{-e(V_C - V_B - I_C R_C - I_B R_B)/nkT}\right) \\ &+ I_{CE_S}\left(\mathrm{e}^{e(V_C - V_E - I_C R_C - (I_C + I_B) R_E)/nkT} - \mathrm{e}^{-e(V_C - V_E - I_C R_C - (I_C + I_B) R_E)/nkT}\right). \end{aligned} \tag{6.15}$$

Figures 6.9 and 6.10 show the resistance-inclusive model function fitted to the current-voltage and current-current characteristics of CST device P-03-J06 and the extracted fit parameters are shown in Table 6.3. The results indicate that for collector potentials of 80-90 V, the effective series resistances are in the range 1-2 MΩ, decreasing to 500-600 kΩ as the collector potentials increase. By way of comparison with the original model, it is noted that both sets of results indicate significantly higher reverse saturation currents in the collector-base channel than in the collector-emitter channel. Furthermore, in the range of collector potentials $V_C \geq 100$ V, the ideality factors agree reasonably well. It is perhaps unsurprising

that the ideality factors obtained from the two models disagree most strongly for the lower collector potentials, the regime in which their distinguishing factors, the series resistances, were largest.

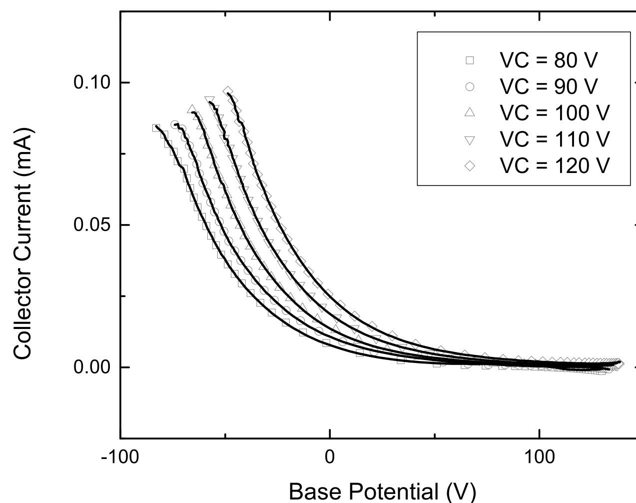


Figure 6.9: *Current-voltage transfer characteristics of an asymmetric CST (device P-03-J06). The solid lines are least squares fits of the model transfer function, taking into account the series resistances.*

Table 6.3: *Results of fitting model current-voltage transfer function to characteristics of an asymmetric CST (device P-03-J06): extracted fit parameters I_{CB_S}, I_{CE_S}, R_C, R_B, R_E and n.*

V_C (V)	I_{CB_S} (nA)	I_{CE_S} (nA)	R_C (kΩ)	R_B (kΩ)	R_E (kΩ)	n
80	397 ± 15	27.9 ± 1.8	2677 ± 30	2105 ± 33	2467 ± 35	987.9 ± 12.4
90	955 ± 10	31.6 ± 1.2	1468 ± 17	1151 ± 13	1164 ± 14	1475 ± 6
100	629 ± 54	15.6 ± 11.0	614.6 ± 48.1	560.5 ± 53.3	584.1 ± 1017.0	1282 ± 28
110	708 ± 66	10.3 ± 11.1	613.2 ± 39.7	572.8 ± 47.4	594.3 ± 1325.0	1322 ± 31
120	649 ± 59	19.0 ± 6.9	568.1 ± 30.5	557.2 ± 39.2	601.9 ± 423.2	1300 ± 29

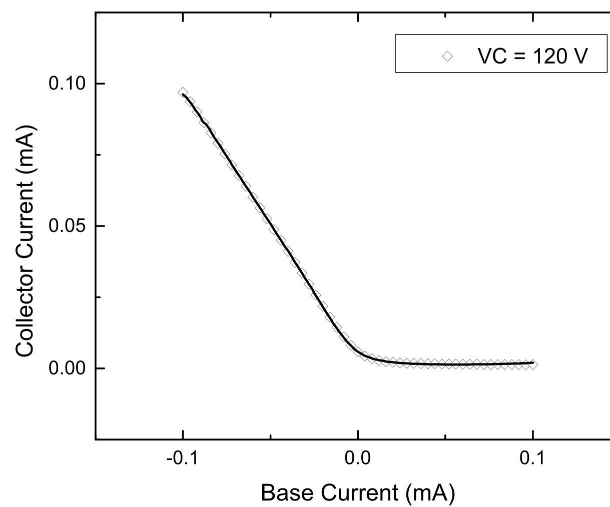


Figure 6.10: *Current-current transfer characteristics of an asymmetric CST (device P-03-J06) for a collector potential of 120 V. The solid line represents the collector current values obtained from the resistance-inclusive current-voltage fit, plotted against base current.*

6.5 CST switching mechanism

It has been shown that by modelling the CST device as a triangular network of anti-parallel diode pairs, it is possible to reproduce the observed electrical characteristics, which implies that the switching behaviour arises from the non-linear or *diode-like* characteristics of the material. The switching mechanism shall now be examined, with the aim of understanding it in terms of these current-voltage characteristics.

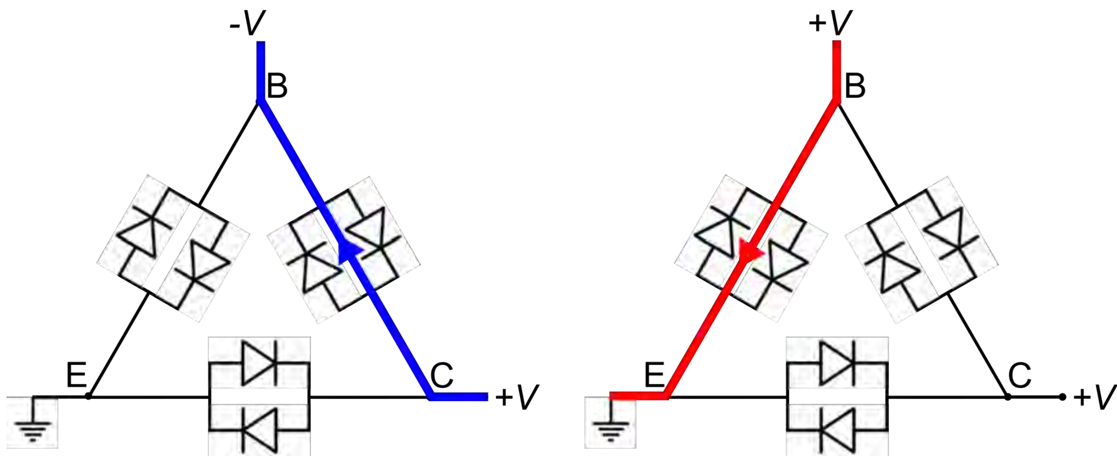


Figure 6.11: *Switching mechanism of the CST. The collector and emitter are held at fixed potentials. The base potential is used to switch the conduction path. A negative base potential results in conduction in the base-collector channel (left), whereas a positive base potential results in conduction in the base-emitter channel (right).*

The main observation from the CST characterisations was that by controlling the base signal, the collector current may be switched on or off. Figure 6.11 illustrates the electrical situation for the two states. The emitter and collector potentials are maintained at ground and $+V$ respectively. In the first state, shown on the left, a large negative potential is applied to the base. Now, the potential difference across the collector-base channel is larger than that across any other pair of terminals. Therefore, because of the non-liner IV characteristics of the material, significantly more current will flow in this channel than any other. In the second state, shown on the right, the base potential is switched to $+V$. The base and collector terminals

are now at the same potential, resulting in no current flow in this channel, whereas the potential difference across the base-emitter channel is large, making this the principal conduction path.

It is now clear that the principle of operation of the current switching transistor is distinct from that of both field effect and junction transistors, in that when there is a current through the base, there is a negligible current between the emitter and collector and in that the electric current is either between the base and collector or between the emitter and base, depending on the direction of the current through the base. For ease of comparison, an illustration of the mechanical switch analogues of the two principles of operation is shown in Figure 6.12.

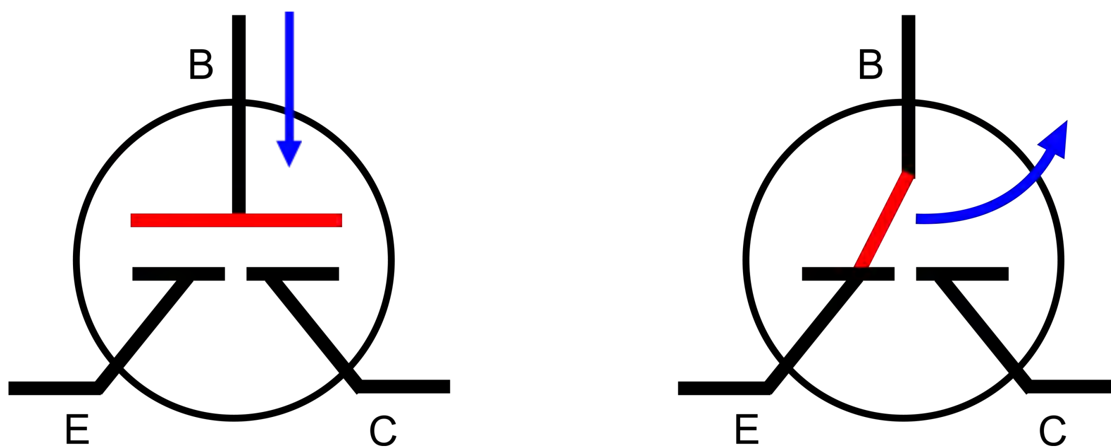


Figure 6.12: *Mechanical analogues of conventional transistor (left) and the CST (right). In contrast with the conventional device, the CST functions as a two-way switch.*

Mechanical switch analogues of transistor operation are shown schematically for a bipolar junction transistor (BJT) and a CST in Figures 6.12a and 6.12b, respectively. In Figure 6.12a application of a signal to the base is equivalent to a linear motion of the plunger in the direction indicated by the blue arrow such that a connection between the emitter and collector is made or broken. In Figure 6.12b a current through the base is equivalent to a rotation of the lever in the direction indicated by the blue arrow such that a connection is made between either the base and collector or the emitter and base.

6.6 Modelling the CST with discrete components

The current switching transistor demonstrates a novel mode of current switching in which three terminals are connected by a material with non-linear current-voltage characteristics, such as a printed network of silicon nanoparticles, wherein the conduction path may be switched from one pair of terminals to another. The implication is that this type of switch could be constructed by bridging three terminals with any material which possesses similar non-linear current-voltage characteristics. To test this idea, a model circuit consisting of three 75 V metal oxide varistors connected in a triangular arrangement was constructed. The current-voltage characteristics of one such varistor are shown in Figure 6.13, where it can be seen that the varistor exhibits highly non-linear behaviour.

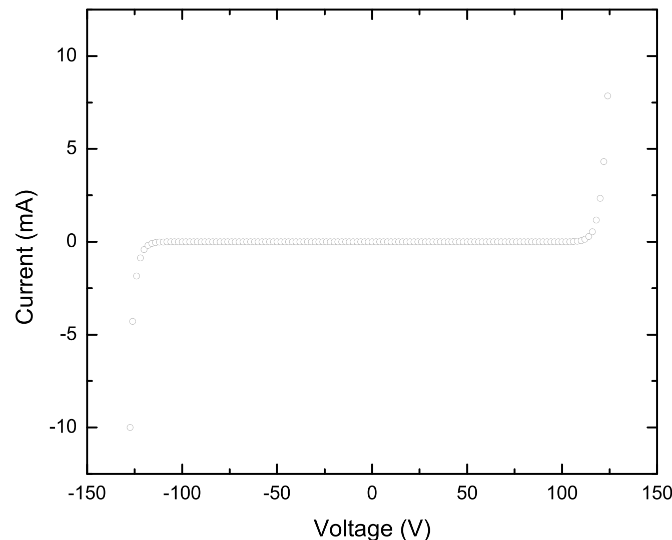
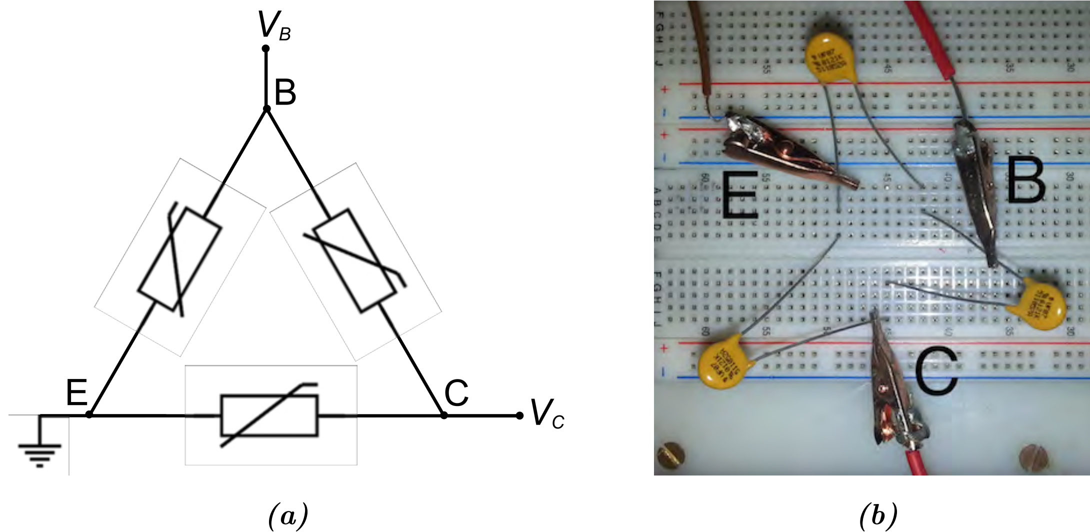


Figure 6.13: *Current-voltage characteristics of a 75 V metal oxide varistor.*

Figure 6.14 shows a circuit diagram and a photograph of the model circuit. Figures 6.15a and 6.15b show the current-current and current-voltage characteristics of the varistor model circuit. The results indicate that the switching behaviour



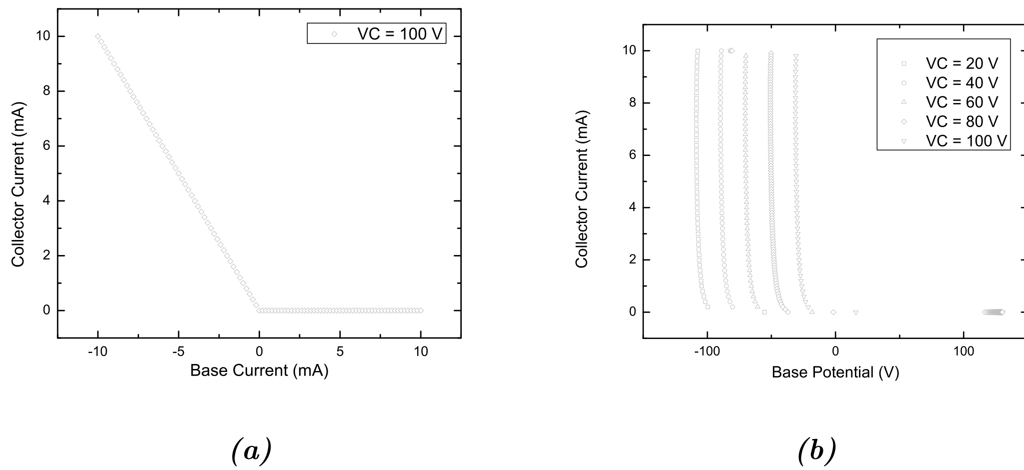
(a) *(b)*

Figure 6.14: *(a) Varistor model circuit diagram. (b) Photograph of varistor model circuit.*

of this model is even more pronounced than that observed in the printed devices. For negative base currents, the collector current response is linear with a slope slightly less than unity and for positive base currents the off-current in the collector terminal is small. The current-voltage transfer curves show that the device has well-defined switching voltages, which are dependent on the collector potential. These results imply that the model circuit is an idealised form of the CST, exhibiting the same mode of switching.

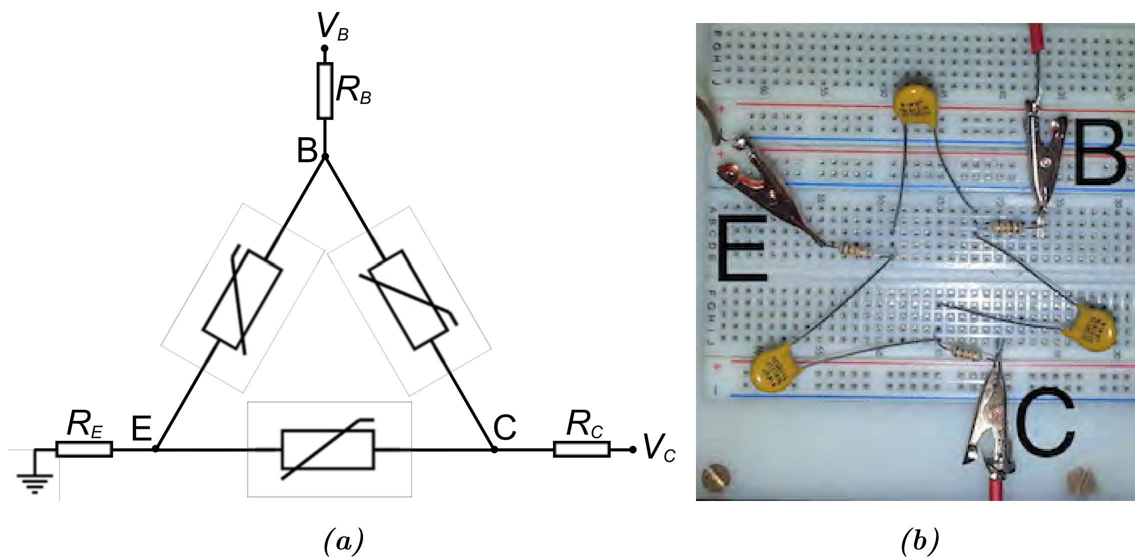
In an attempt to more accurately model the observed switching behaviour of the printed CST devices, the discrete circuit has been extended to include the series resistances which were introduced in section 6.4. Figure 6.16 shows a circuit diagram and photograph of the extended model circuit.

The current-current and current-voltage transfer characteristics of this model, using 10 kΩ series resistances, are shown in Figures 6.17a and 6.17b. The effect of the series resistance is a departure from the sharp switching which was observed for the initial, resistance-exclusive, model circuit. For negative base current, the current-current gradients ($\mathrm{d}I_C/\mathrm{d}I_B$) are lower in the series resistance model. For



(a) ***(b)***

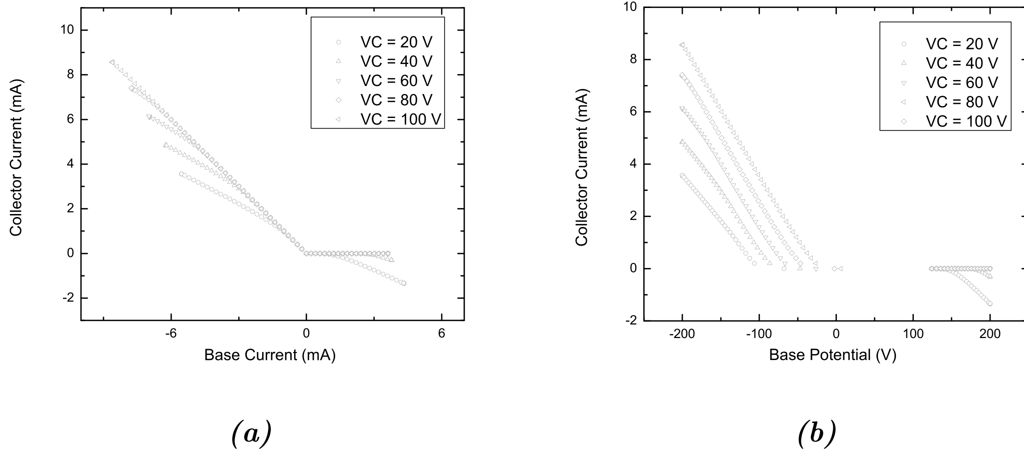
Figure 6.15: *(a) Current-current transfer characteristics of varistor model circuit for collector potential 100 V. (b) Current-voltage transfer characteristics of varistor model circuit, for collector potentials from 20 V to 100 V.*



(a) ***(b)***

Figure 6.16: *(a) Varistor model circuit diagram, including series resistances R_E, R_B and R_C. (b) Photograph of varistor model circuit with 10 kΩ series resistances.*

positive base current, the collector current tends to be larger and negative. That is, the off currents are larger. The current-voltage transfer characteristics exhibit comparatively poorly defined switching voltages, characterised by lower current-



(a) *(b)*

Figure 6.17: *(a) Current-current transfer characteristics of series resistance inclusive varistor model circuit for collector potential 100 V. (b) Current-voltage transfer characteristics of series resistance inclusive varistor model circuit, for collector potentials from 20 V to 100 V.*

voltage gradients ($\mathrm{d}I_C/\mathrm{d}V_B$). Generally, these differences in behaviour are more pronounced for lower collector potentials, and the switching approaches the ideal behaviour with increasing V_C.

6.7 CST mode of operation

The preceding analysis of the electrical behaviour of the current switching transistor has revealed that its mode of operation is distinct from that of previously known transistors. It functions as an electrically controlled two-way switch, in which modifying the signal applied to the base switches the conduction path from between the collector and base to between the base and emitter. Furthermore, the proposed theoretical models and subsequently tested model circuits have been used to demonstrate that the two-way switching is a result of the nonlinear current-voltage characteristics of the conduction paths between any pair of terminals. The current switching transistor does not function as an amplifier, because injected cur-

rent is simply directed through the device by controlling the terminal potentials. This is in stark contrast to the operation of conventional transistors, in which the application of potential or the injection of charge induces internal electric fields or modulates potential barriers in order to control the output current.

Chapter 7

Conclusion

A new device, which utilises a previously unknown two-way mode of current switching, has been developed. This is the current switching transistor (CST), a three-terminal electronic device which exhibits a transfer resistance, in which the application of a potential or injection of charge to one terminal controls the current at either of the two remaining terminals. These are the essential characteristics of a transistor, and hence its classification as such.

The development of the CST arose from a more general project aimed at producing fully printed transistors based on nanoparticulate silicon. The first result of these efforts was the creation of insulated-gate field-effect transistors (IGFETs), which showed mixed results. While they function as FETs and have characteristics comparable to amorphous silicon thin film transistors (a-Si TFTs), they also exhibit significant leakage current. This challenge may be overcome by addressing material incompatibilities within the device structure, especially pertaining to the dielectric and semiconducting layers. The IGFETs demonstrated that silicon nanoparticles represent a viable option for producing printed transistors, and more generally, printed active devices. However, the most important result obtained from the IGFETs was the discovery of an asymmetry of the drain current with respect to the direction of the gate current, which was more pronounced at higher drain potentials. Since this effect coincided most strongly with those regimes of potential

in which the gate leakage current was highest, silicon devices without an insulating layer were investigated.

The CST and previously known transistors differ from each other in two respects. First, the mode of operation of the CST is as an electrically controlled two-way current switch, in which the direction of current can be switched from "collector to base" to "base to emitter" by controlling the potential at, or current through, the base. This is in contrast with conventional transistors, in which the current between two terminals (the emitter and collector or the source and drain) is modulated by applied potential or injected charge at the third terminal (the base or gate). The conventional transistor is therefore a simple one-way switch, in which signal amplification is also possible. The second difference is between the mechanisms governing their operation. In a conventional transistor, internal electric fields are induced by controlling the base (or gate) signal, which cause a change in the conductivity of the semiconducting channel between the other two terminals, thereby controlling the current in the channel. However, in the CST the electrical resistance of the conduction paths between each pair of terminals is modulated by controlling the potentials applied to the base, with the other two terminals held at fixed potentials. The switching behaviour exhibited by the CST is therefore a result of the nonlinear current-voltage characteristics of the semiconducting material, which depends upon activated charge transport.

In the case of the CST devices presented here, the nonlinearity was an intrinsic property of the printed nanoparticulate silicon with which they were produced. However, it is important to note that similar two-way switching behaviour could be achieved by employing any other material combination with a nonlinear current-voltage response, including the use of discrete components. In addition to the printing methods used here, other processes such as thin film techniques may be applied to the production of these devices. While the simplicity of using an intrinsically nonlinear material such as printed silicon is seen as an advantage, similar properties could be realised in a device containing Schottky junctions at all three contacts. The principles of conventional semiconductor fabrication could

then be applied to the production of devices, using monocrystalline silicon, thereby leveraging the development of that industry.

In terms of the possible applications of the current switching transistor, there are a number of opportunities. Most obviously, a two-way switch can always perform the same function as a simple switch, and therefore the CST may be used as an alternative to insulated-gate FETs in flexible electronics. The greatest suitability of the CST to such applications will be to those in which the simplicity of not requiring a compatible gate insulator is sufficiently advantageous as to outweigh a potentially significant base current. Examples of such applications include pixel switches for current driven displays such as electroluminescent elements, or in addressing memory. However, it is envisioned that the most interesting applications will ultimately be those which fully take advantage of the two-way mode of switching, for example to simplify the construction of logic gates.

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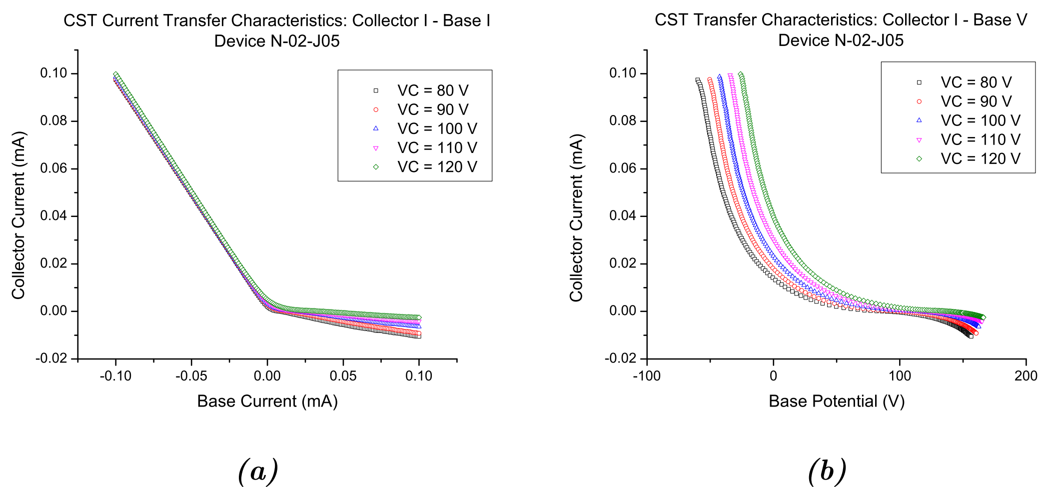
Appendix A

Current switching transistor transfer characteristics

Asymmetric CSTs with n-type silicon



(a) ***(b)***

Figure A.1: *Test results for asymmetric CST device N-02-J05: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

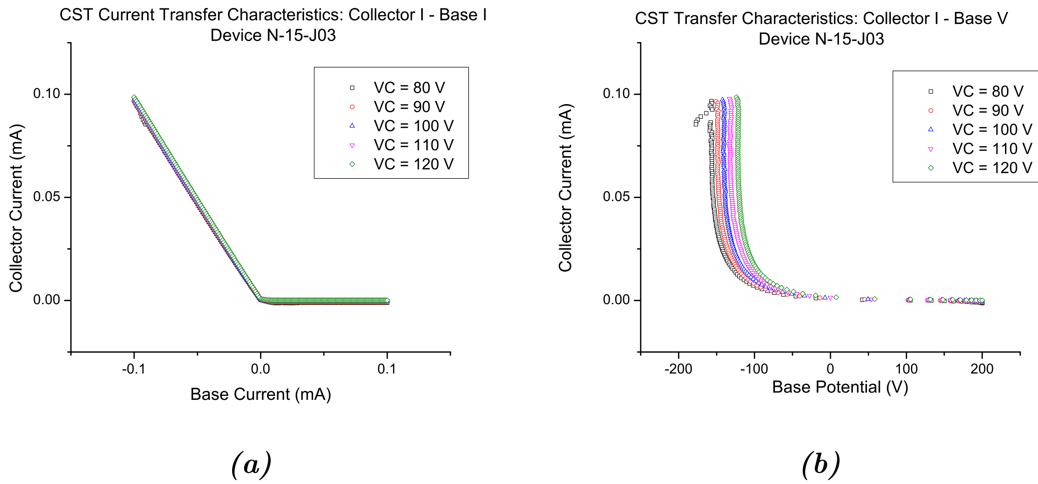


Figure A.2: *Test results for asymmetric CST device N-15-J03: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

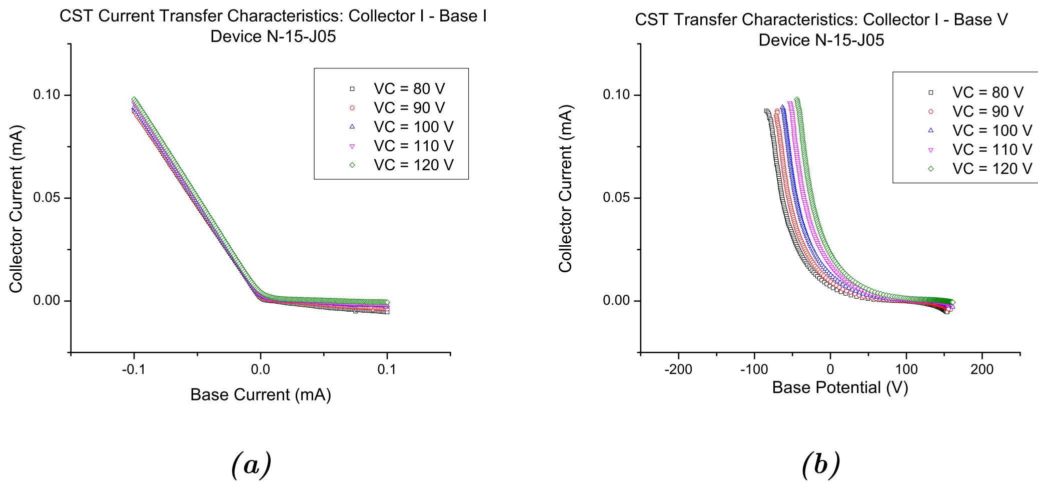
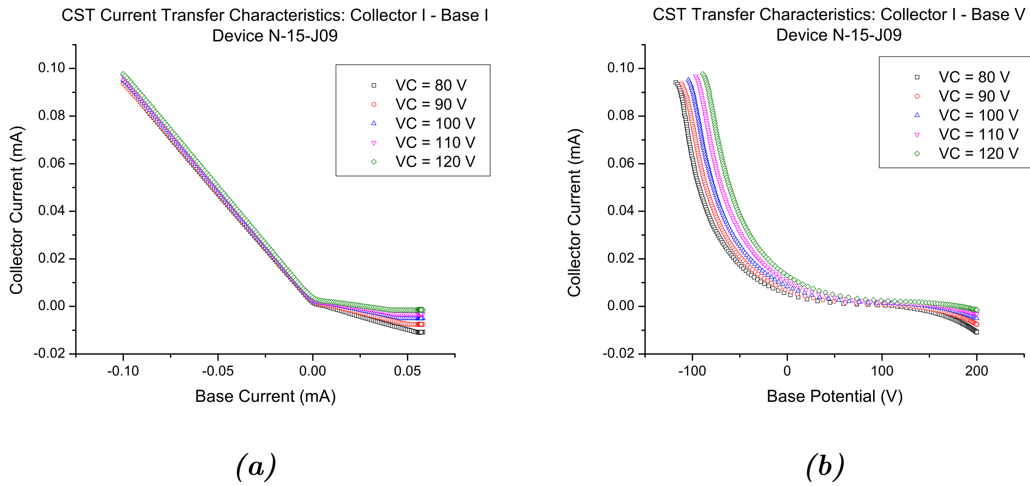
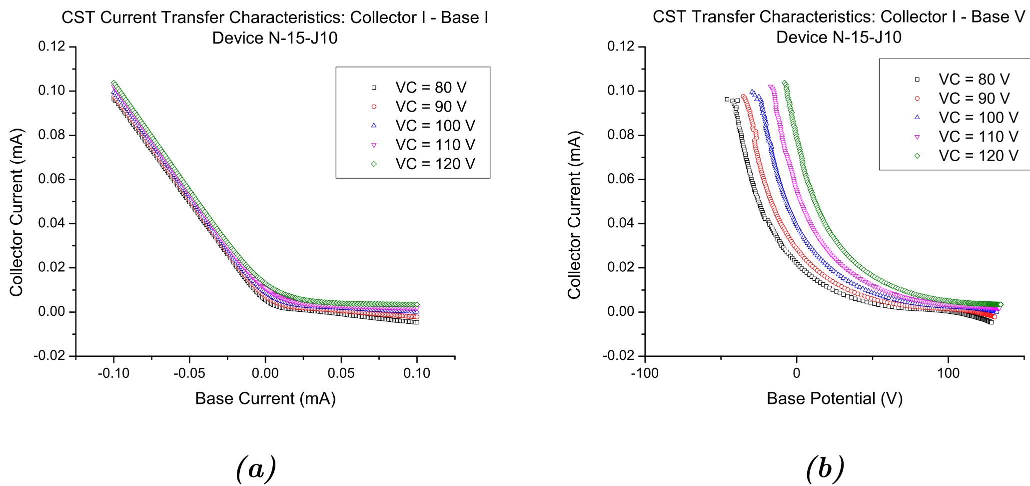


Figure A.3: *Test results for asymmetric CST device N-15-J05: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



(a) *(b)*

Figure A.4: *Test results for asymmetric CST device N-15-J09: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



(a) *(b)*

Figure A.5: *Test results for asymmetric CST device N-15-J10: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

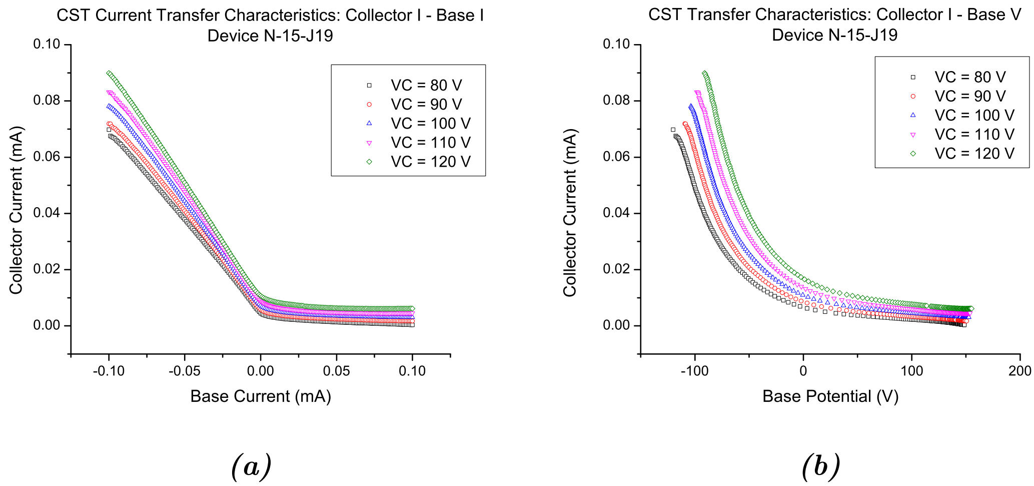


Figure A.6: *Test results for asymmetric CST device N-15-J19: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

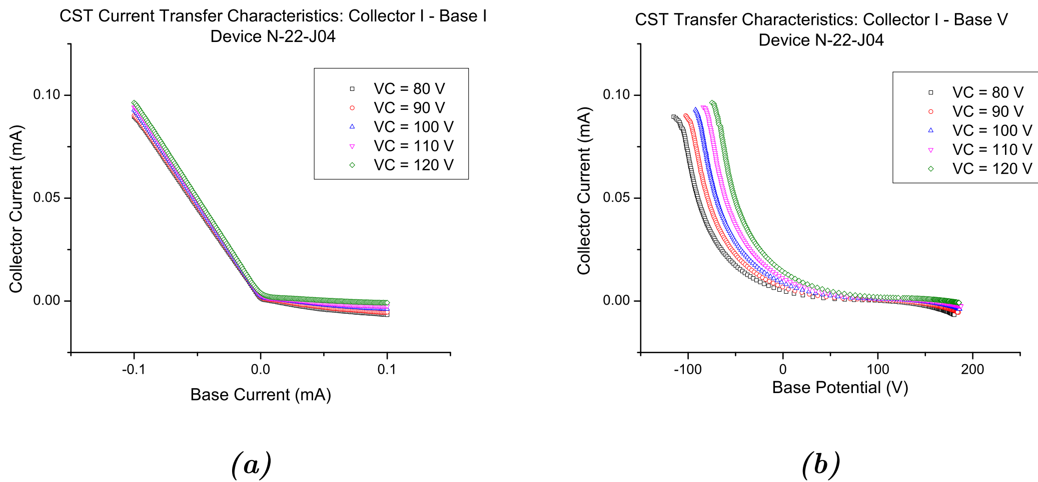


Figure A.7: *Test results for asymmetric CST device N-22-J04: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

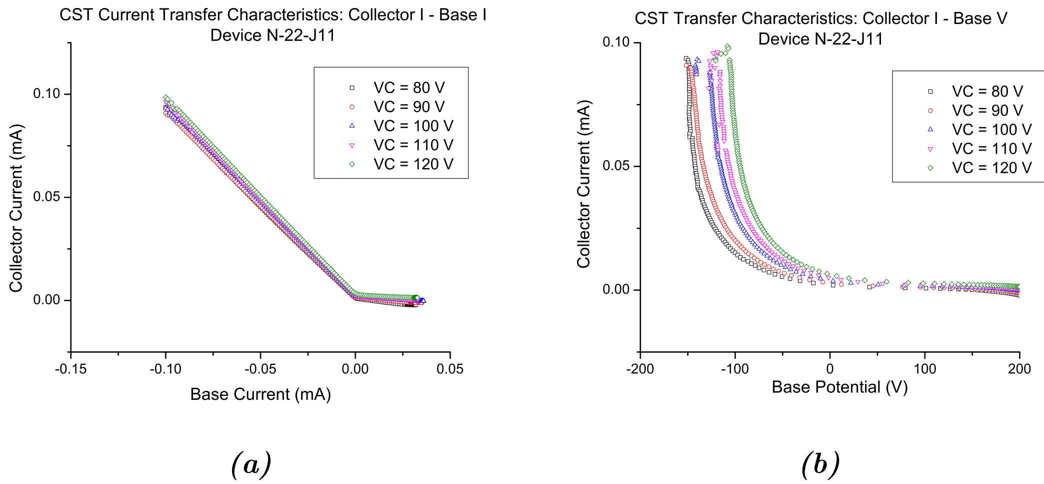


Figure A.8: *Test results for asymmetric CST device N-22-J11: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

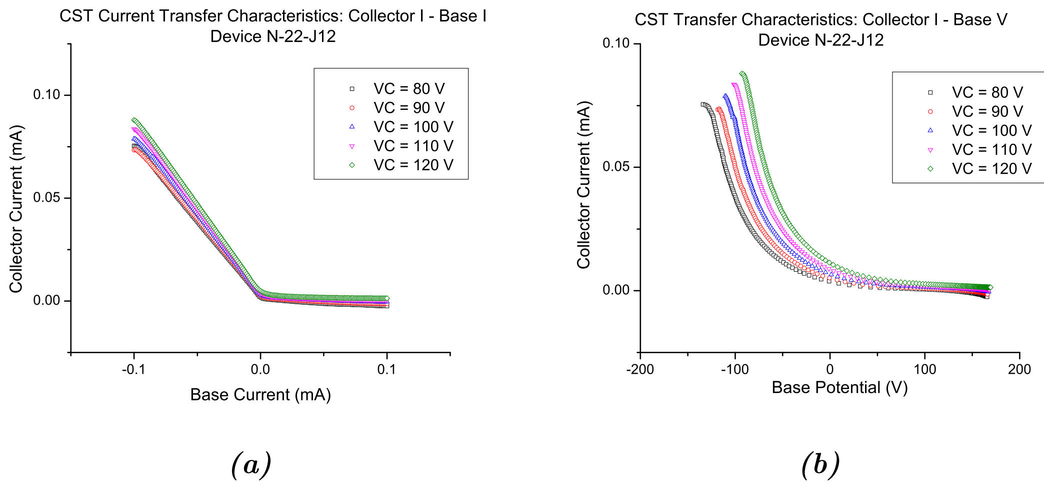
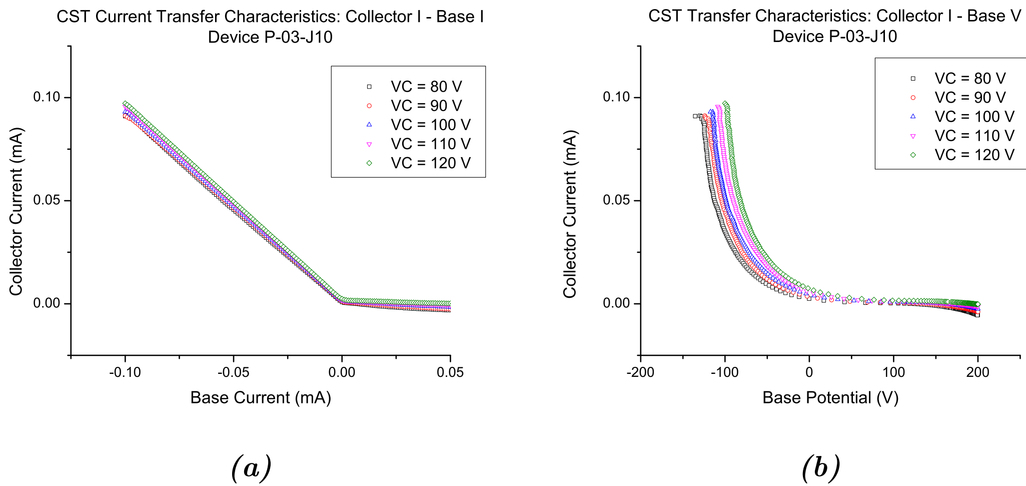


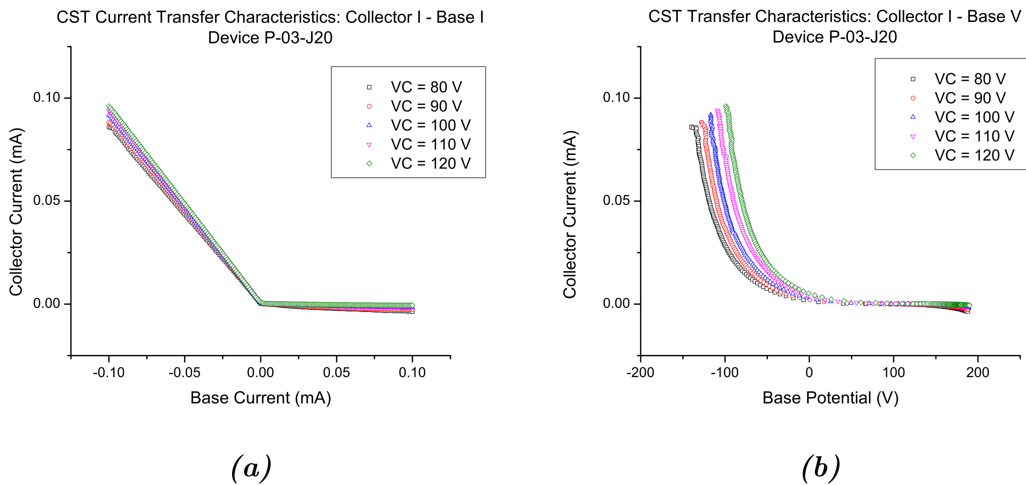
Figure A.9: *Test results for asymmetric CST device N-22-J12: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

Asymmetric CSTs with *p*-type silicon



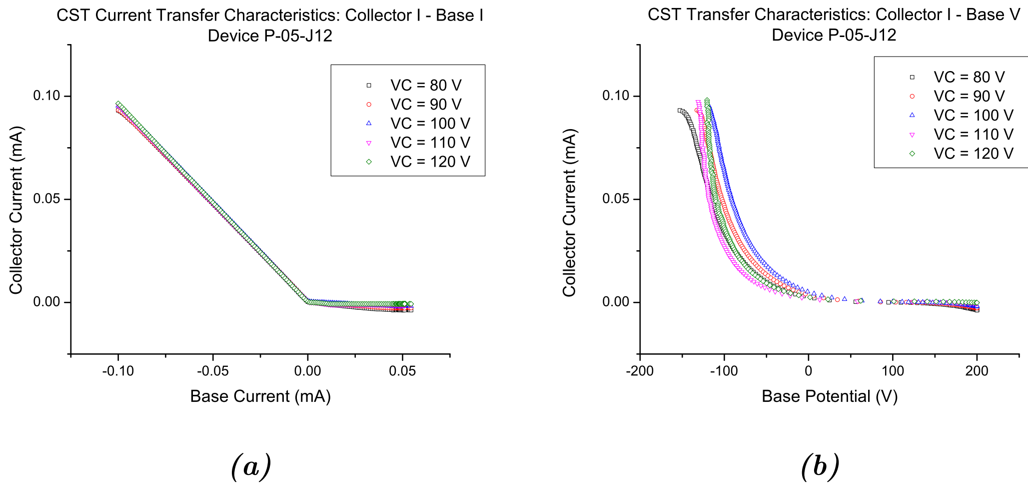
(a) *(b)*

Figure A.10: *Test results for asymmetric CST device P-03-J10: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



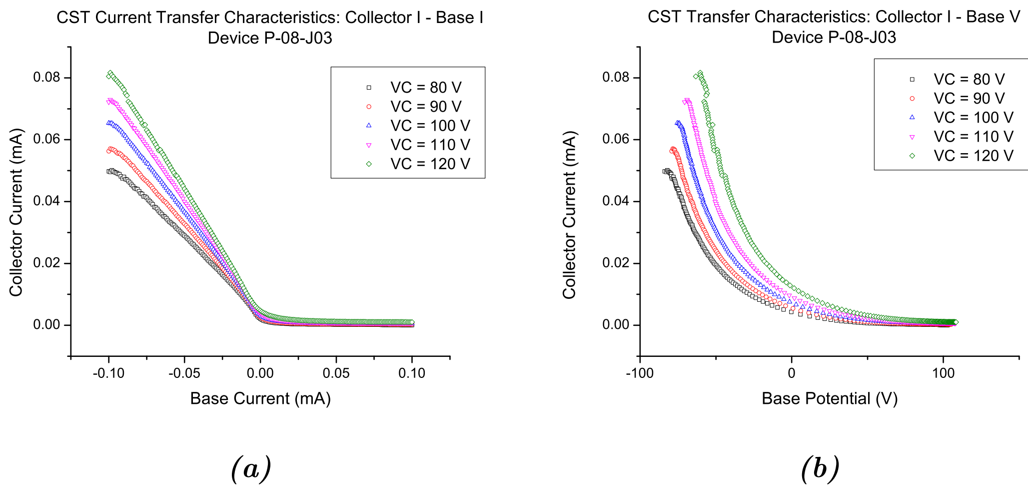
(a) *(b)*

Figure A.11: *Test results for asymmetric CST device P-03-J20: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



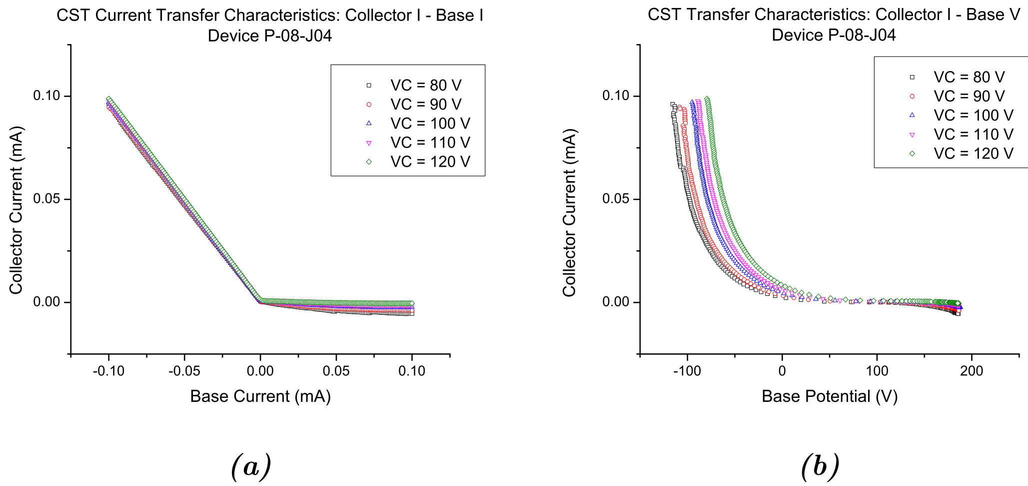
(a) *(b)*

Figure A.12: *Test results for asymmetric CST device P-05-J12: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



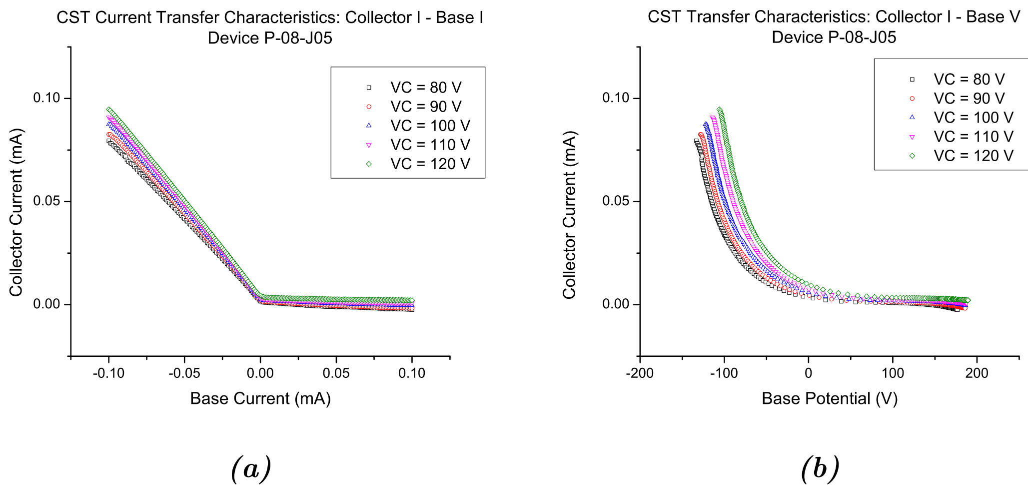
(a) *(b)*

Figure A.13: *Test results for asymmetric CST device P-08-J03: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



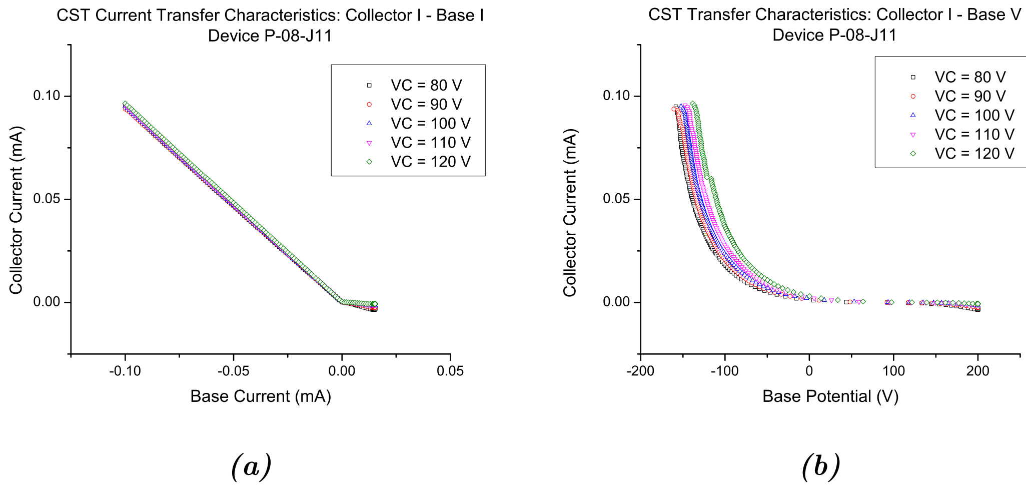
(a) *(b)*

Figure A.14: *Test results for asymmetric CST device P-08-J04: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



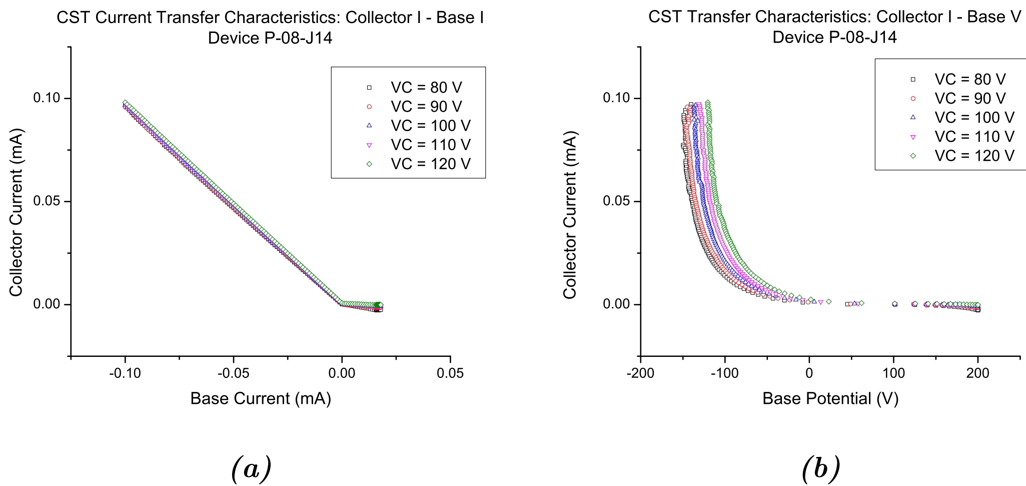
(a) *(b)*

Figure A.15: *Test results for asymmetric CST device P-08-J05: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



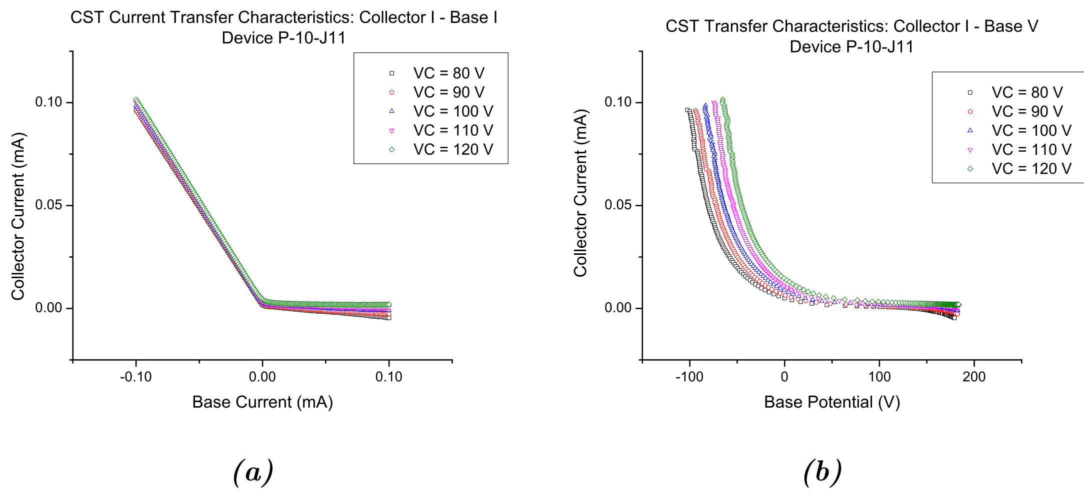
(a) *(b)*

Figure A.16: *Test results for asymmetric CST device P-08-J11: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



(a) *(b)*

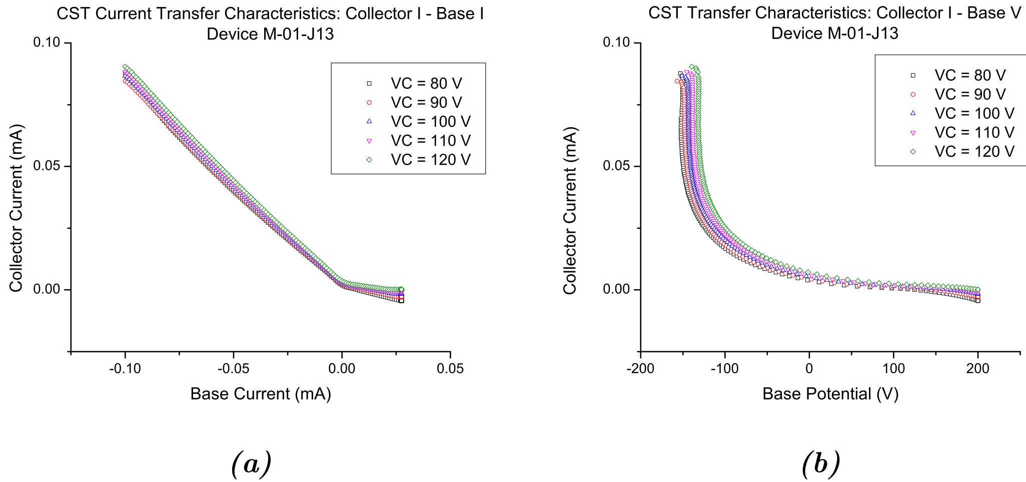
Figure A.17: *Test results for asymmetric CST device P-08-J14: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



(a) *(b)*

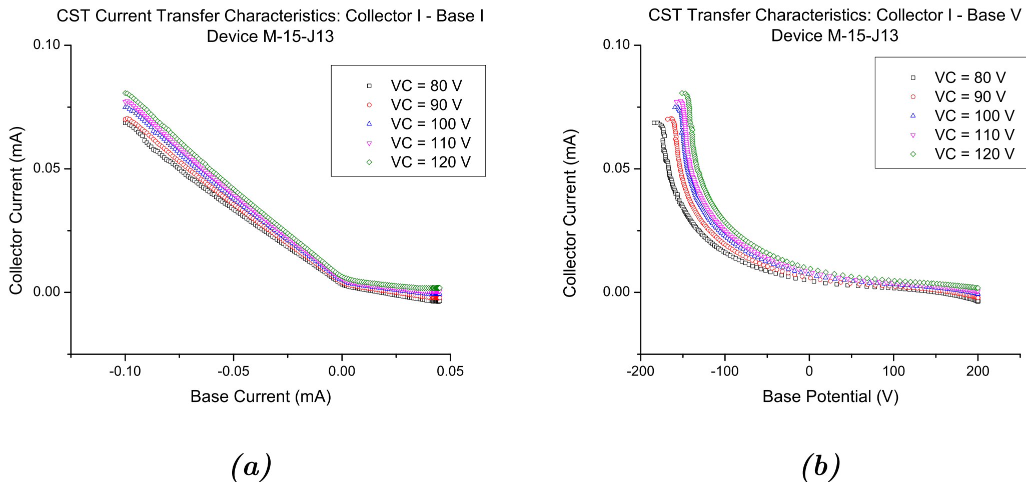
Figure A.18: *Test results for asymmetric CST device P-10-J11: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

Asymmetric CSTs with 2503 grade silicon



(a) *(b)*

Figure A.19: *Test results for asymmetric CST device M-01-J13: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*



(a) *(b)*

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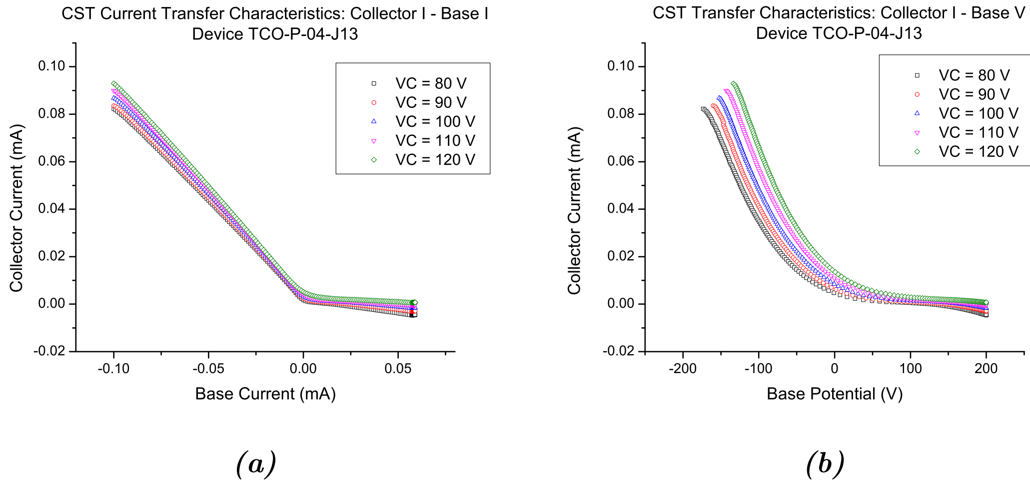
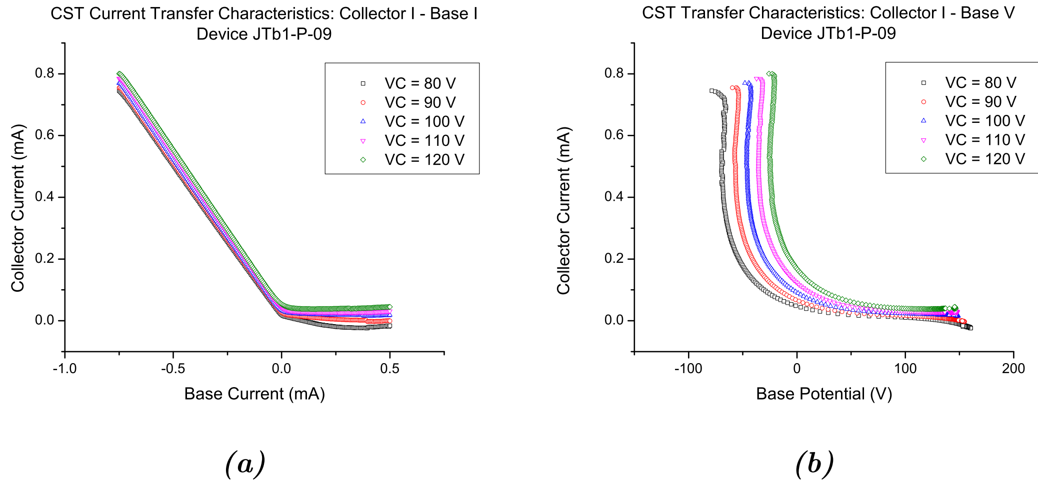
Asymmetric CSTs with TCO electrodes



(a) ***(b)***

Figure A.21: *Test results for asymmetric CST device TCO-P-04-J13: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

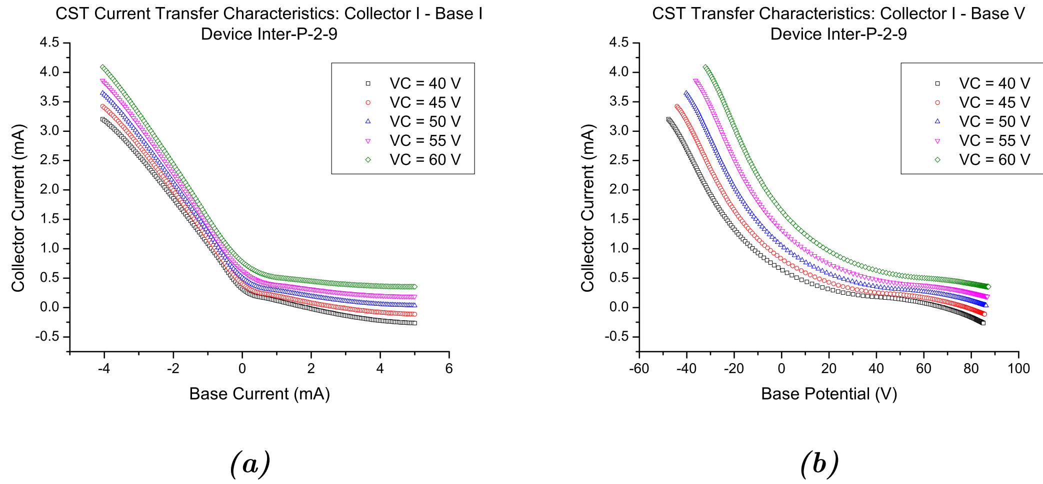
Symmetric CSTs with p-type silicon



(a) ***(b)***

Figure A.22: *Test results for symmetric CST device JTB1-P-09: (a) current-current transfer characteristics and (b) current-voltage transfer characteristics.*

Interdigitated CSTs with p-type silicon



(a) *(b)*

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