A DIRECT A.C. TO A.C. REGENERATIVE FREQUENCY AND VOLTAGE CONVERTER

BY

Michael James Case

Submitted to

THE UNIVERSITY OF CAPE TOWN

in fulfilment of the

requirements for the

degree of

DOCTOR OF PHILOSOPHY

July 1980

ACKNOWLEDGEMENTS

The author wishes to thank -

Professor N.C. de V. Enslin for his help and encouragement during the course of this thesis ,

Professor L.J.L.N. Besseling for his pithy and timely words of advice ,

Messrs. M. Attfield and M.N.B. Stephens for building a large amount of the experimental equipment ,

The University of Cape Town for providing the facilities to make this research possible ,

Assoc. Professor S.G. MacLaren for his comments on the final production of this thesis ,

My wife , Glynne , for bearing with me during the writing of this thesis .

ABSTRACT

The reliable variable speed operation of an a.c. machine over a wide speed range is a problem that has received attention for some time. In this thesis a system to permit such operation from a fixed frequency fixed voltage supply is proposed, under the name of the asynchronous modulation converter. This converter is of the cycloconverter family, but is force-commutated and is not synchronised with the supply frequency. The power switching element comprises a power transistor in a diode bridge, coupled to the control circuitry by opto-isolators.

The output of the a-mod converter is produced by a "chopper" modulation process and this results in the harmonics present being at frequencies well removed from the fundamental.

A feedback system to ensure smooth commutation of the output current from the power switches is described. This feedback system operates by sensing the rate of rise of the inductive voltage surge on the load when a switch is opened to operate a freewheel path switch.

CONTENTS

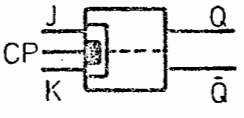
Appendix 8 : DESIGN DETAILS OF COMPLETE SYSTEM 142

NOTES ON DRAWINGS

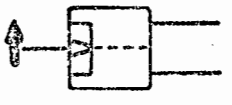
1) Resistor values are in ohms and capacitor values are in microfarads
2) Logic symbols are in accordance with DIN practice , as follows :

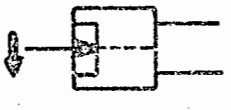
NAND Gate :

J-K Flip-flop

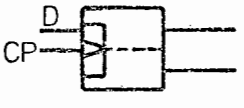


Monostable





D Flip-flop



NOMENCLATURE

C_L = Load stray capacitance

C_t = Transistor bypass or "snubber" capacitance

C_{sup} = Supply bypass capacitance

f_c = Switching rate

f_{hI} = Input current harmonic frequency

f_{hO} = Output voltage harmonic frequency

f_i = Supply frequency

f_o = Output frequency

f_t = Transistor transition frequency

h_{FE} = Transistor forward current transfer ratio

I_1 = Input current fundamental component

I_B = Base current

I_C = Collector current

I_f = Fundamental current

I_h = Harmonic current

I_o = Peak output current

i_o = Instantaneous output current

i_{ph} = Current in one supply phase

$I_{s/b}$ = Second breakdown collector current

j = Any integer 1 , 2 , or 3

k = Boltzmann's constant

L_L = Load inductance , R-L load

L_o = Load inductance , L load

L_s = Supply circuit inductance

E_s = Supply voltage

m = Any integer 1 , 2 , 3 , etc.

n = " " " " " "

p = Pulse number

q = Charge on an electron

R_L = Load resistance

R_S = Supply circuit resistance

R_{sup} = Supply bypass resistance

S_n = Switching function

T = Control pulse frame duration , or transistor turn-off time ; clear from context

t = Time in general , or in eqn. 3.15 , abs. temp.

V_{CE} = Collector - emitter voltage

$V_{CEO(SUS)}$ = Maximum collector-emitter voltage, base open circuit

V_{CEX} = Maximum collector-emitter voltage, base reverse-biassed

V_{av} = Mean output voltage

V_i = Peak input voltage

v_i = Instantaneous input voltage

v_o = Instantaneous output voltage

ω_i = Supply angular velocity

ω_m = Modulating angular velocity

ω_o = Output angular velocity

μ = Input current distortion factor

τ = Time duration of switch conduction

ϕ_i = Input current phase angle

CHAPTER 1

INTRODUCTION

1.1 A HISTORICAL PERSPECTIVE:

"Now that electric power is so widely distributed on the three-phase system, there is a distinct advantage in being able to use an induction motor directly connected to the mains, instead of a motor that requires the conversion of the power into direct current ...

The recent advances that have been made in the economical control of the speed of induction motors have opened up to the manufacturer and other power users the possibility of employing this type of motor in cases where its so-called constant-speed characteristic would have banned it as unsuitable only a few years ago."

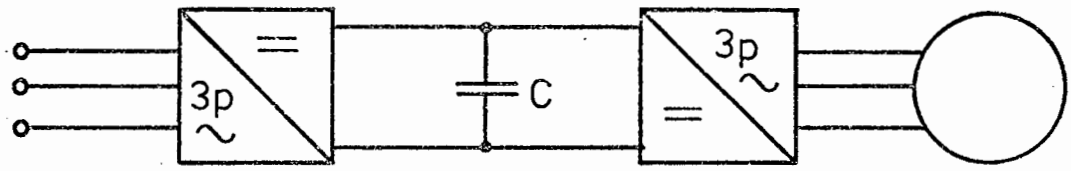
These prophetic words introduce Miles Walker's book of 1924, "The control of the speed and power factor of induction motors"(1). It is noteworthy that the first part of the prediction has indeed come true, as the induction motor today drives a myriad of rotating devices at ratings from a fraction of a kilowatt to tens of megawatts. The latter part of the prediction has, however, been somewhat tardy in its fulfilment, as the variable-speed induction motor drive still has a multitude of effective competitors (2) (4) (10) (13).

The relative lack of acceptance by users of rotating machinery of the variable-speed induction motor in comparison to the widespread use of variable-speed d.c. machines may be

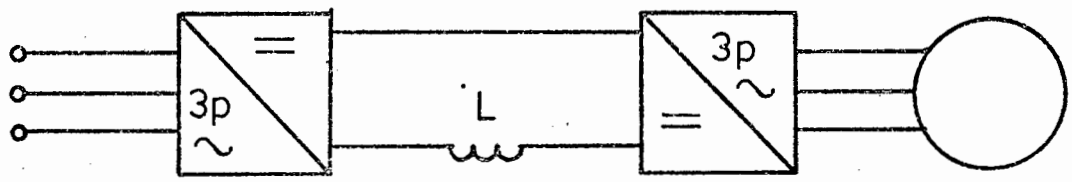
ascribed to various factors. Many of what may be termed the non-electronic solutions have suffered from a limited speed range, poor starting torque (in comparison to the d.c. motor), low efficiency and high cost(1). Very often the machine is purpose-built, like the Boucherot machine, and is thus only applicable where a special motor would have to be used in any case, like the U.S. Navy battleships of the pre-war era(1). On the other hand, the electronic frequency converter has been, before the advent of the solid-state device, an unreliable, costly and cumbersome affair(8). The mercury-arc rectifier, while being an efficient device, certainly is not compact, and large-scale use of these for, say, cycloconversion would only be justified when the need to avoid a d.c. machine (in say, a Ward-Leonard configuration) was created by environmental or similar factors(4).

The tremendous amount of significant research carried out during the 1920's and 1930's laid the theoretical foundation which is seeing practical fulfilment during the present era of the solid-state device. The d.c. drive has also benefited from modern advances, and, in comparison with its a.c. counterpart, offers the advantage of simplicity and hence reliability. The inherent simplicity of the induction motor, coupled to the increasing reliability and decreasing (relative) cost of electronic systems, make the advantages of the d.c. drive of lesser significance in many applications. The commutator of the d.c. motor is particularly suspect, from both a maintenance and environmental hazard point of view.

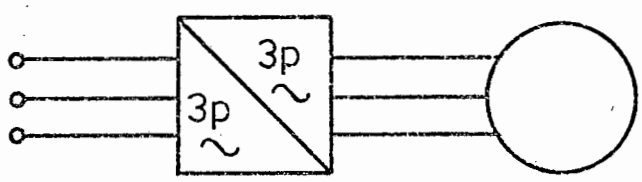
Thus it is proposed to confine this work to the variable-speed induction motor drive, and in particular to an electronic converter capable of altering constant-voltage constant-frequency a.c. into variable-frequency variable-voltage a.c.



Voltage-fed inverter



Current-fed inverter



Direct converter

Fig. 1.1. Induction motor speed control by electronic stator frequency variation .

suitable for powering an induction motor.

The methods for achieving this conversion are, broadly speaking, the d.c. link inverter and the direct converter. The d.c. link inverter comprises a rectifier, which may or may not be phase-controlled, with constant voltage or constant current output, driving a polyphase inverter. The direct converter, which could be a cycloconverter, in one of many configurations (8) (9) (12) (13), or the asynchronous modulation converter which forms the subject of this work, directly modulates the supply to produce the desired output. These possibilities are shown diagramatically in Fig. 1.1.

1.2 VARIABLE-SPEED INDUCTION MOTOR DRIVES - GENERAL:

The fundamental principles governing the variable-speed operation of an induction motor are summed up in the equations

$$n_s = \frac{2f}{\text{no. poles}} \qquad (1.1)$$

and

$$n_r = n_s (1 - S) \qquad (1.2)$$

From these equations (ref. 5) it can be seen that the speed of an induction motor may be varied by varying

* Stator frequency
* Number of poles
* Slip

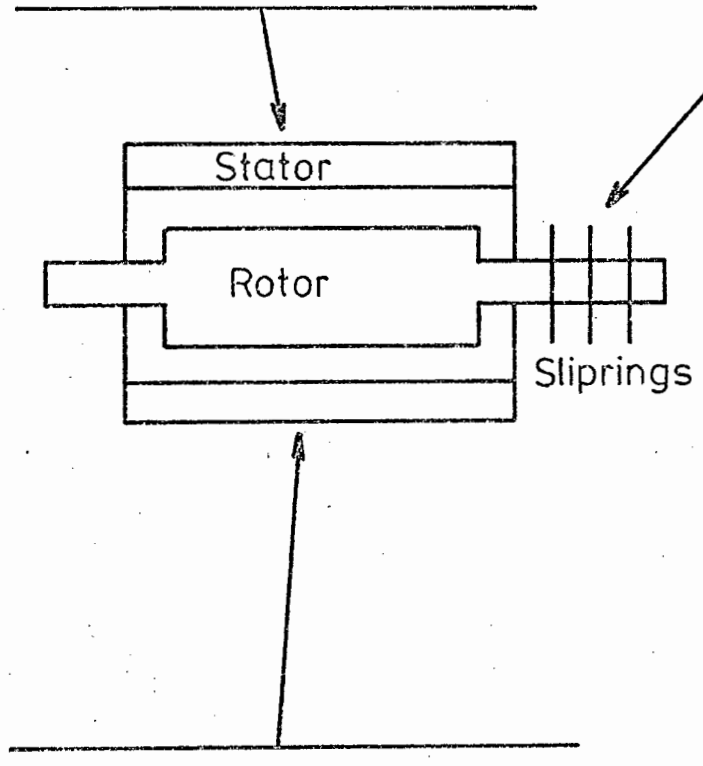
The ingenuity of many designers has been applied to various schemes to control these parameters, and Fig. 1.2 indicates diagramatically, but not exhaustively, some of the possibilities. It is, however, true to say that the advent of the solid-state power device (diode, thyristor, transistor) has

STATOR FREQUENCY :

Voltage-fed inverter (10)(13)
Cycloconverter (10)(9)(12)
Current-fed inverter (10)
A-mod coverter (14)(12)(15)

SLIP CONTROL :

Rotor rheostat (1)
Boucherot motor (1)
Motors in cascade (1)
Slip energy recovery (1)
Leblanc phase advancer (1)
Commutator motors
- N-S
- Schrage (3)(4)



POLE CHANGING :

Discrete number pole changes (1)(4)(5) (2:1 , 3:1 etc.)
Pole amplitude modulation (5)
Pole stretching (5)
Log motor (5)
Cylindrical rotor (5)

Fig. 1.2. Induction motor speed control possibilities .

tended to put most of these ingenious schemes in the shade and modern development has tended to focus attention on the possibilities of supplying a variable-frequency a.c. supply to the variable-speed induction motor drive.

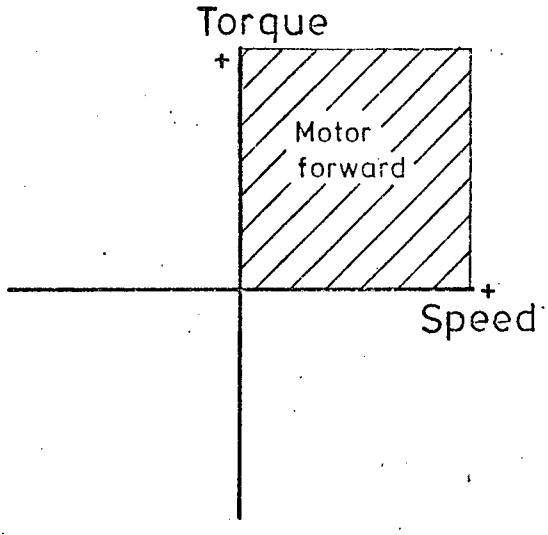
It is also, however, a requirement of a variable-frequency system to maintain constant flux in the machine(7) (5). This is from the property of an inductance,

$$e = N\frac{d\phi}{dt} \qquad (1.3)$$

Thus any variable-frequency scheme must also be capable of varying the voltage at the terminals of the motor.

The operation of a drive may be considered from the point of view of its speed-torque capabilities. This is usually illustrated diagramatically on 4 quadrants of operation as in Fig. 1.3(9). One-quadrant operation is the simplest to arrange, be it by means of voltage-fed or current-fed inverter. Two-quadrant operation implies the ability of inversion, i.e. current direction unchanged but energy return to mains via reversed potential. Four-quadrant operation means that the machine may motor or regenerate in either direction. D.c. link inverters may operate in any mode, the only determining factor being the preparedness of the user to pay for additional facilities. Four-quadrant operation of the voltage-source d.c. link inverter does mean that the rectifier portion of the system must be a dual converter; a conscious decision must be made to switch between thyristor banks, in order to supply a reversed-potential reversed-current output.

The cycloconverter, which comprises a modulated dual converter, is inherently a 4-quadrant device, but the bank-selection problem remains a determining factor in design (8) (9) (10) (12) (13).

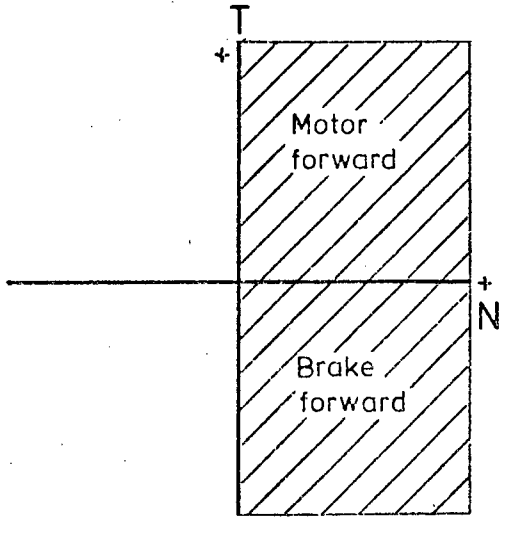


ONE QUADRANT

OPERATION :

Unidirectional rotation ;

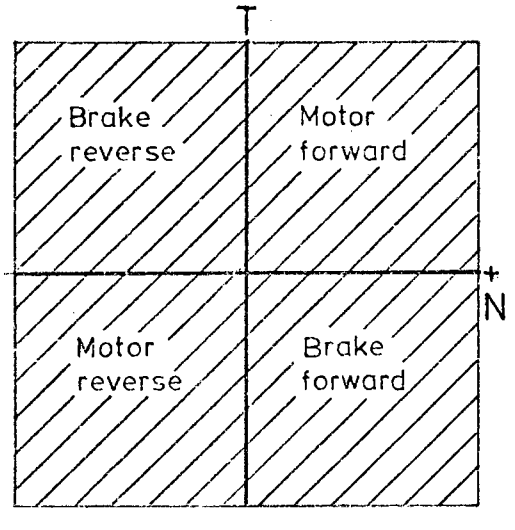
no braking .



TWO QUADRANT OPERATION :

Unidirectional rotation ;

braking .



FOUR QUADRANT OPERATION :

Bidirectional rotation ;

braking .

Fig. 1.3. Modes of drive operation .

The asynchronous modulation converter, which could be classed with the cycloconverter family, avoids the bank selection problem by force-commutating the switching elements; use of force-commutation in the normal cycloconverter would also solve this problem(12) (14) (15).

1.3 THE D.C. LINK INVERTER:

The d.c. link inverter, as previously mentioned, comprises a rectifier coupled to a d.c. to a.c. converter. The two main types are the voltage-source(27) inverter and current-source converter(25) (26). Briefly, the voltage-source inverter produces a constant d.c. voltage from a (usually) phase-controlled rectifier. If the inverter is to operate in 4 quadrants then the rectifier comprises two back-to-back thyristor banks to enable regeneration to take place. Thyristors are used on equipments of larger sizes and these have to be fast-turn-off "inverter grade" devices.

The output waveform of the voltage-source inverter is not a pure sinusoid and various attempts have been made to reduce the distortion(28). Triple-n harmonics are eliminated by the 3-phase connection, and reduction of 5th and 7th harmonics is quite feasible. It is thus possible to operate an induction motor over a wide speed range; even down to standstill.

The disadvantages of the voltage-source inverter are serious. These are

High speed thyristors must be used.

Complex circuitry required for regeneration.

Forced commutation of inverter thyristors is prone to failure. This leads to unkind remarks like "An equipment only microseconds from failure"!(26)

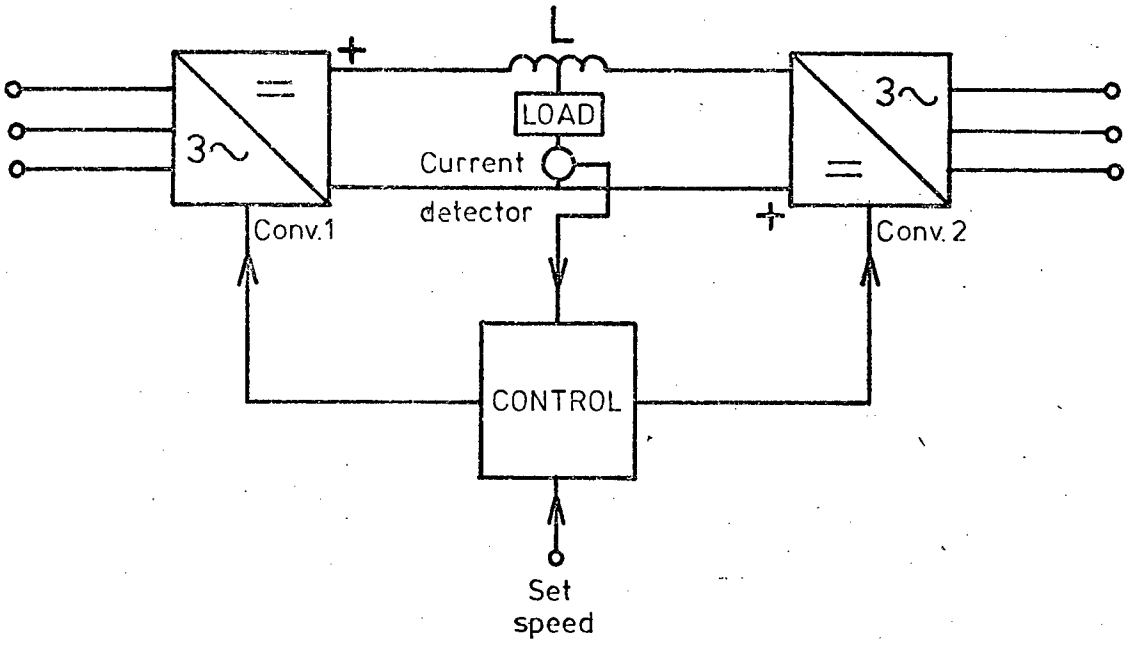
The current-source inverter, on the other hand, comprises a phase-controlled (full bridge) rectifier supplying a constant current (via a large inductance) to a force-commutated thyristor inverter(25) (26). The commutation circuitry is considerably simpler and "rectifier grade" thyristors may be used. Since the current flow is undirectional, regeneration is obtained when the rectifier goes into the inversion mode of operation, avoiding the bank selection problem.

The main disadvantage of the current-source is the erratic behaviour of the motor at low speeds, due to the current waveform that must perforce be impressed on the machine(29).

The disadvantages listed for both classes of inverter, while not being entirely inhibitory to the use of these systems, are sufficient to hamper the fulfilment of Miles Walker's prophecy. The d.c. drive suffers from few similar disadvantages, on the other hand, and would account for the continued "popularity" of it.

1.4 THE CYCLOCONVERTER:

The cycloconverter performs a direct a.c. to a.c. frequency conversion - that is, there is no d.c. link in the circuit. Fig. 1.4 shows how two converters (rectifiers) may be connected to provide a single-phase output. These two converters connected in parallel comprise a dual converter. The control signal controls the firing angle of each converter in order to produce half-sine outputs which are summed to produce a sinusoidal output. The usual electronic control devices used in the dual converter are thyristors(9); since there is



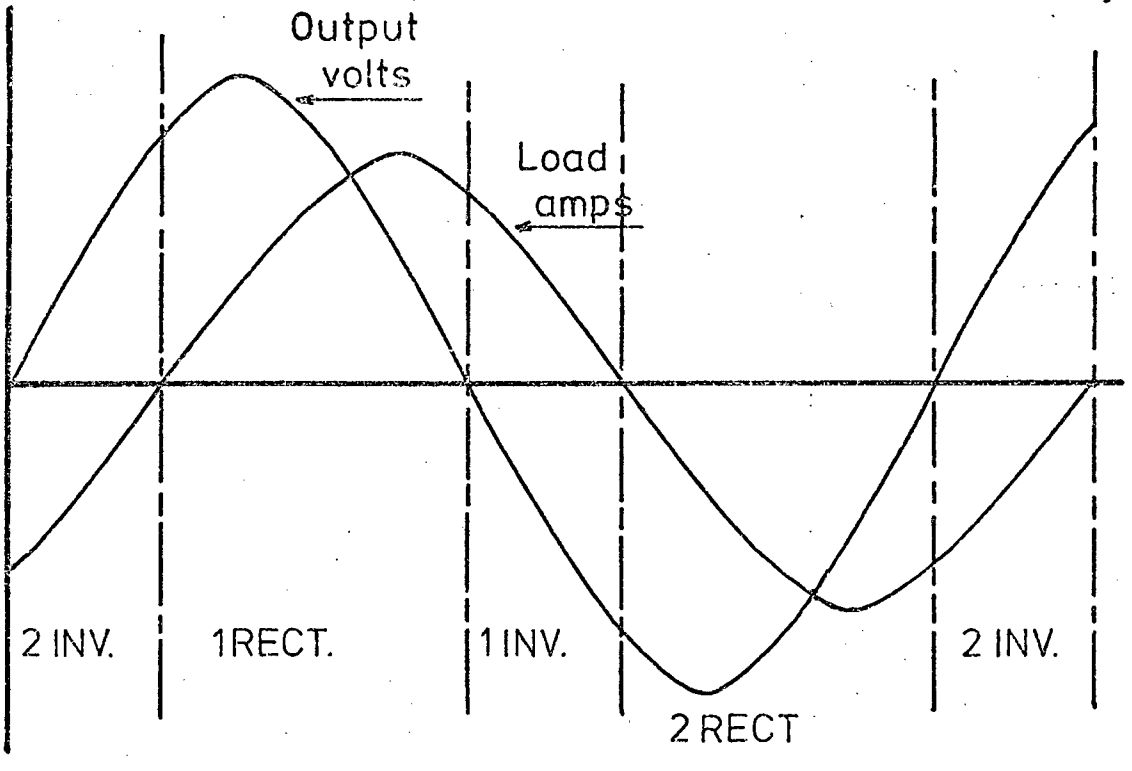


Fig. 1.4. Basic cycloconverter operation . Bank selection by current detection or circulating current limited by L .

no intrinsic turn-off capability care must be taken to avoid a short-circuit between converters (or thyristor "banks"). Fig. 1.4 indicates some possibilities. If the tapped inductor L is used for current-limiting then both converters may conduct simultaneously and the cycloconverter operates in the "circulating current" mode(9). If the current-zero detector is used then bank selection may take place under its direction; various control strategies may be adopted, such as "first current zero" or "fundamental current zero"(9) (12) (13).

Since the control signal continuously varies the firing angle, the output voltage and input current harmonics are not simple functions of output frequency and voltage separately, but functions of both(9) (12) (30). Especially troublesome are subharmonics in the supply line current.

The commutation problem poses difficulties for high frequency operation of the cycloconverter and generally the use of these systems is confined to low-frequency systems operating below 1/3 of supply frequency. The large number of components is also considered a disadvantage, but this disappears at high power drives(31).

If the use of a force-commutated switching element is postulated, then the classical cycloconverter acquires a new appearance. It is then possible to operate with unity or controllable input displacement factor, minimum output voltage distortion or unrestricted input-to-output frequency ratio. These possibilities are dealt with in refs. (12) and (13). The unrestricted frequency changer (U.F.C.) in particular is very interesting as this system overcomes some of the objections to the cycloconverter.

The asynchronous modulation converter which forms the subject of this work is an extension of the cycloconverter

concept; in particular of the U.F.C. By using a switch with intrinsic turn-off capability and by operating with a higher modulation frequency it is possible to overcome most of the problems associated with cycloconverter operation, in particular the bank selection, input current harmonic and output voltage distortion problems.

CHAPTER 2

THE ASYNCHRONOUS MODULATION CONVERTER

2.1 BASIC PRINCIPLES AND CIRCUIT CONFIGURATION:

The basic principle of the a - mod converter is shown in fig 2.1, which depicts a rotary switch coupling a load successively to the supply phases.

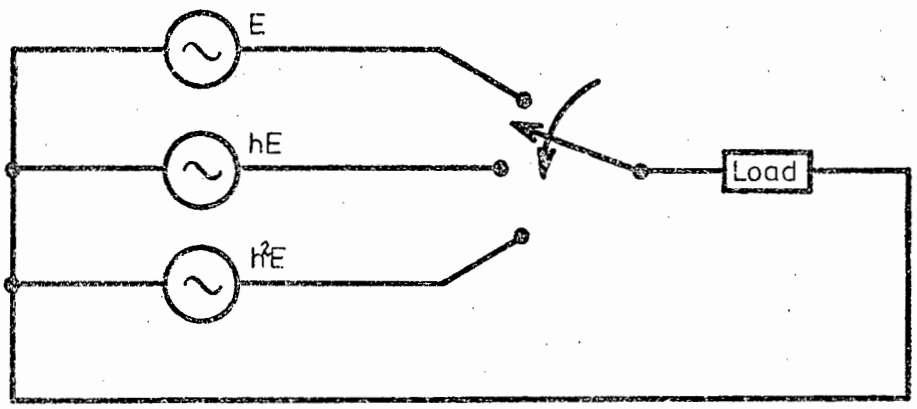


Fig.2.1 . Basic a-mod converter

The switch wiper would rotate at a steady speed, applying the load to each supply phase for an equal length of time. The waveform which would be produced by this arrangement is shown in fig. 2.2.

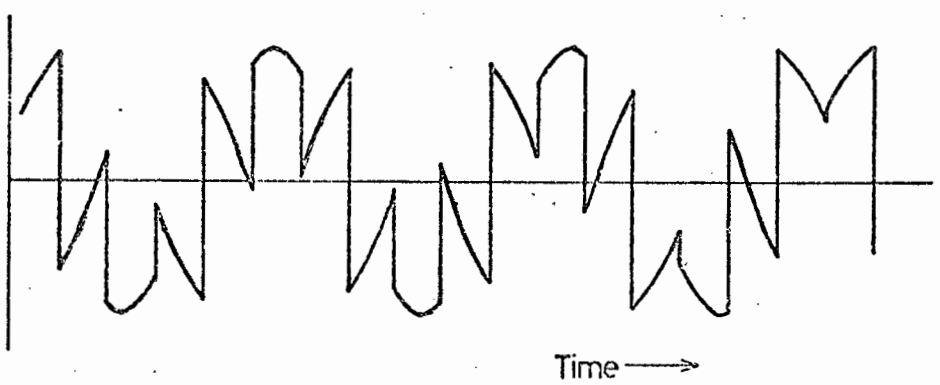


Fig. 2.2. Waveform produced by basic converter

This arrangement only provides for frequency control, with a fundamental output frequency of (Appendix 1)

$$f_o = f_i \pm \frac{f_c}{p} \qquad (2.1)$$

The $\pm$ signs indicate a frequency increase or decrease depending on whether the direction of rotation of the switch is the same as the phase rotation of the supply, or opposing it.

The arrangement shown above thus produces an output voltage wave by successively switching the input waves. A more realistic approach would be to replace the "rotary switch" with a number of bidirectional electronic switches, one to each supply phase. The output wave then would consist of segments of the input waves, with the length (in time) of each segment depending on the duration of the closure of the relevant switch. If we refer to the duration of a pulse sequence of S pulses (that is, one pulse to each of S switches) as a control pulse frame of time T, then the duration of each input wave segment may be varied by varying the duration of each control pulse during the relevant $\frac{1}{S}$ time slot of time τ . The mean value of the output voltage is then:

$$V_{av} = \frac{1}{T} \int_0^{\tau} v_o dt = \frac{\tau}{T} v_o \qquad (2.2)$$

The average value of the output wave voltage may thus be varied by this process, used in the control of

D.C drives and known as pulse width modulation.(2,3,10,13) The relevant pulses are shown in fig. 2.3, and the circuit configuration for a 3 pulse system supplying a single-phase load is shown in fig. 2.4. The usually-accepted symbol for a triac is used here to denote a bidirectional switch with intrinsic turn-off capability.

Note that in this thesis the pulse number of a system is defined as "the number of discrete phase - related A.C. sources available for the fabrication of the output wave", in place of the usually accepted definition which is "the number of discrete segments of the output wave which are fabricated during each cycle of the A.C. input wave". Since it is proposed ultimately to fabricate an output wave from many segments the classical definition is not entirely relevant, since it is really meant to apply to naturally-commutated systems. (8)

2.2 THE FUNDAMENTAL THEORY OF THE A-MOD CONVERTER.

The fundamental theory of the a-mod converter is obtained by using a similar process to that used to derive the basic expressions describing the operation of the cycloconverter. This consists of multiplying the input wave by a switching function which describes the operation of the switches. This process is shown schematically in fig. 2.5.

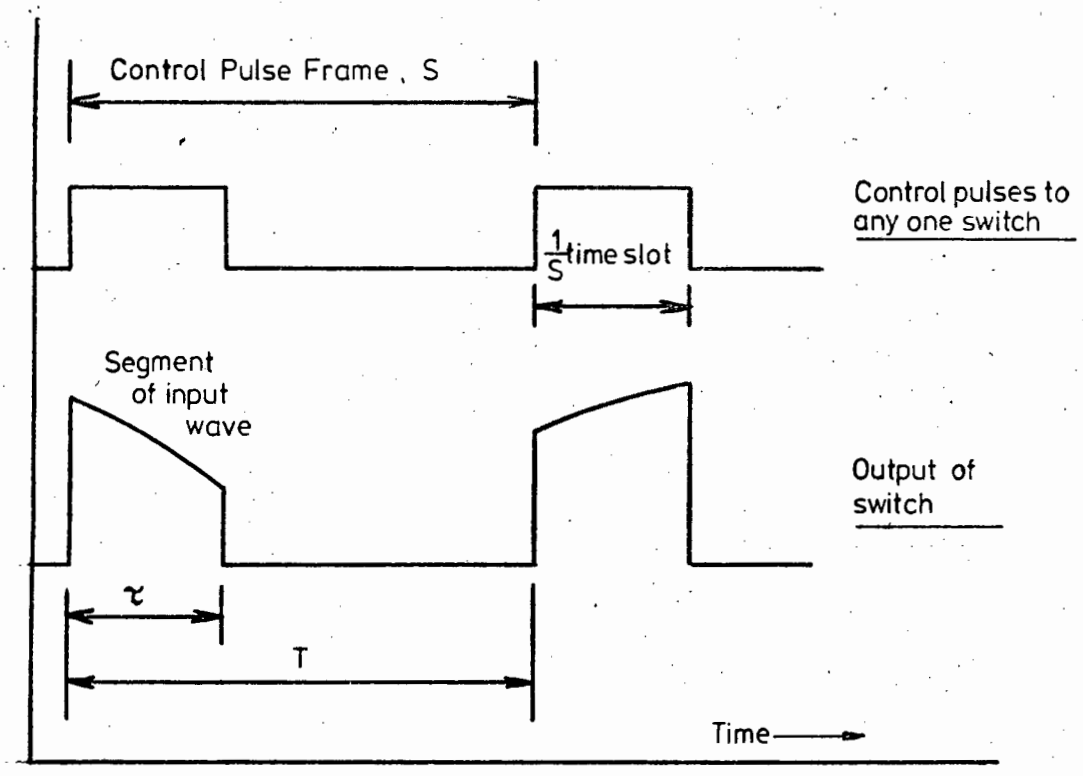


Fig. 2.3. Control pulses for pulse width modulation

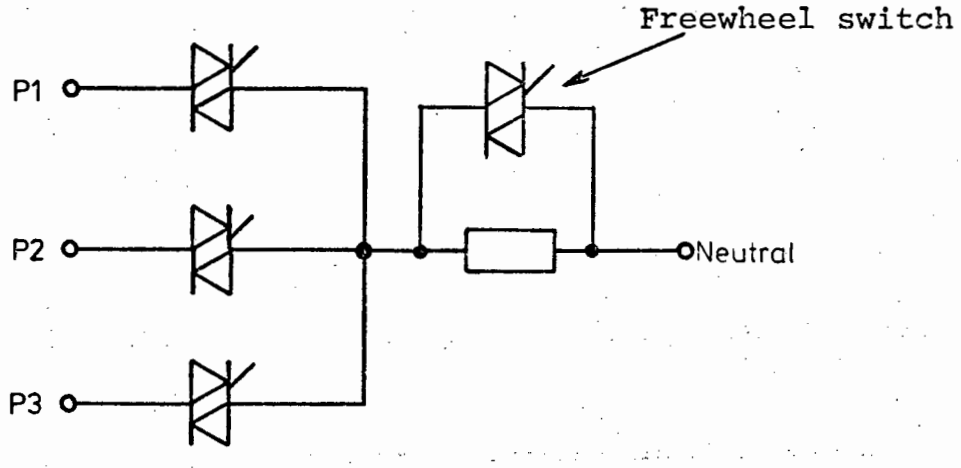


Fig. 2.4. 3-Pulse circuit configuration

The freewheel or shunt switch provides current continuity during the supply off time . An open circuit , in the case of an inductive load , would produce destructive voltage surges .

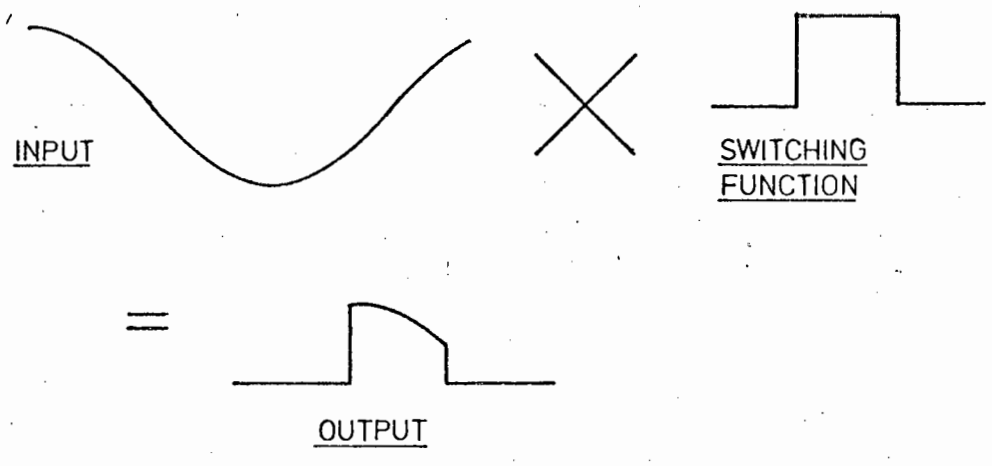


Fig. 2.5. Deriving the output expression

The following assumptions are made, which are usual for converter and cycloconverter analysis, and are valid in the case of the a-mod converter: (8,9,10,12)

i) The supply wave is a pure sinusoid from a zero impedance source. The assumption is made for the basic derivations, but it will be shown further on that source impedance has an important effect on the commutation process in the switches.

ii) The output current is a pure sinusoid at the desired output frequency f_o.
This assumption is justified if the load comprises some device which only permits current to flow at fundamental output frequency. Since the demand for power frequency conversion is mainly in the field of motor speed control the inductive nature of the usual loads postulated prevents

significant harmonic current from flowing. It will be shown that the output voltage harmonics are at frequencies very much higher than fundamental output frequency.

2.2.1 SINGLE PHASE OUTPUT VOLTAGE (Appendix A1)

The control pulses, which form a 3-phase switching function may be expanded by the usual Fourier series to yield the following expression: (16)

$$S_n(\omega_i t, \omega_o t) = \frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin\left(\frac{n\pi\tau}{T}\right) \cdot \cos\{n(\omega_i t + \omega_o t - \ldots\ldots \ldots -(j-1)\frac{2\pi}{3})\} \quad (2.3)$$

The ouput voltage is the product of the control pulse and the input wave, by analogy to the familiar "chopper" amplitude modulation process.

Now

$$v_i = V_i \cos\{\omega_i t - (j-1)\frac{2\Pi}{3}\} \quad (2.4)$$

Thus

$$v_o = S_n(\omega_i t, \omega_o t) \times v_i \quad (2.5)$$

And

$$v_o = \frac{3V_i}{\Pi} \sum_{m=o}^{m\to\infty} \frac{\sin(3m \pm 1)\frac{\Pi\tau}{T}}{(3m \pm 1)} \{\cos\{3m\omega_i t + (3m \pm 1)\omega_o t\}\} \quad (2.6)$$

Note that the $\pm$ signs indicate that the summation must be repeated for + and - signs.

For a 3-pulse system, referred to the supply neutral, which corresponds to the midpoint rectifier system, the fundamental output voltage is:

$$v_{ol} = \frac{3V_i}{\Pi} \sin\frac{\Pi\tau}{T} \cdot \cos\omega_o t \quad (2.7)$$

The maximum value of this expression occurs when:

$$\tau = \frac{1}{p} \times T$$

Or

$$\tau = \frac{1}{3}T$$

Thus

$$v_{olmax} = \frac{3\sqrt{3}V_i}{2\Pi} \cos \omega_o t \qquad (2.8)$$

Or

$$v_{olmax} = 0,827V_i \cos \omega_o t \qquad (2.9)$$

The pulse number may be extended to higher multiples of 3, in which case a transformer is needed, and then:

$$v_o = \frac{2pV_i}{\Pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\Pi\tau}{T}}{(mp \pm 1)} \{ \cos \{mp\omega_i t + (mp \pm 1)\omega_o t \} \} \qquad (2.10)$$

As is apparent from equations 2.5 and 2.9, the output voltage is a function of the ratio of the conduction period τ to the control pulse frame time T. At maximum output voltage, $\frac{p\tau}{T}$ is unity. That is, the conduction period fills the entire slot allocated to it. This quantity $\frac{p\tau}{T}$ is referred to as the "control ratio". Using this definition means that the maximum output is obtained at a control ratio of unity, and zero output when it (the control ratio) is zero. The midpoint converter has the disadvantage that a component of the output current flows in the input. This is overcome by the bridge converter shown in fig. 2.6, in single phase form. (See para. 2.2.4 p. 27) .

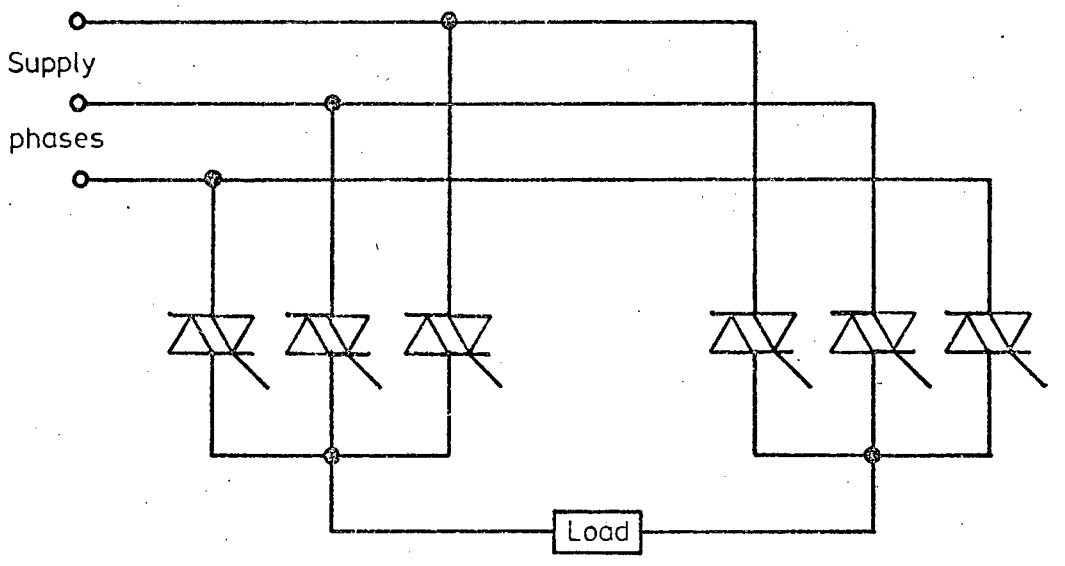


Fig. 2.6. Single phase bridge configuration

The output voltage is then:

$$v_o = \frac{2pV_i}{\Pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\Pi\tau}{T}}{(mp \pm 1)} \{ \cos \{mp\omega_i t + (mp + 1)\omega_o t \}\} \qquad (2.11)$$

The laboratory-tested model was a 6-pulse bridge converter, which yields a fundamental output voltage:

$$v_{ol} = \frac{6V_i}{\Pi} \sin \frac{\Pi\tau}{T} \cos \omega_o t \qquad (2.12)$$

And

$$v_{olmax} = \frac{3V_i}{\Pi} \cos \omega_o t = 0{,}955V_i \cos \omega_o t \qquad (2.13)$$

And if we extend the system to say 12 pulses, using a transformer,

$$v_{olmax} = \frac{1.2V_i}{\Pi} \sin \frac{\Pi}{12} \cos \omega_o t \qquad (2.14)$$

$$= 0{,}989V_i \cos \omega_o t \qquad (2.15)$$

Note that the fundamental frequency occurs when m is zero.

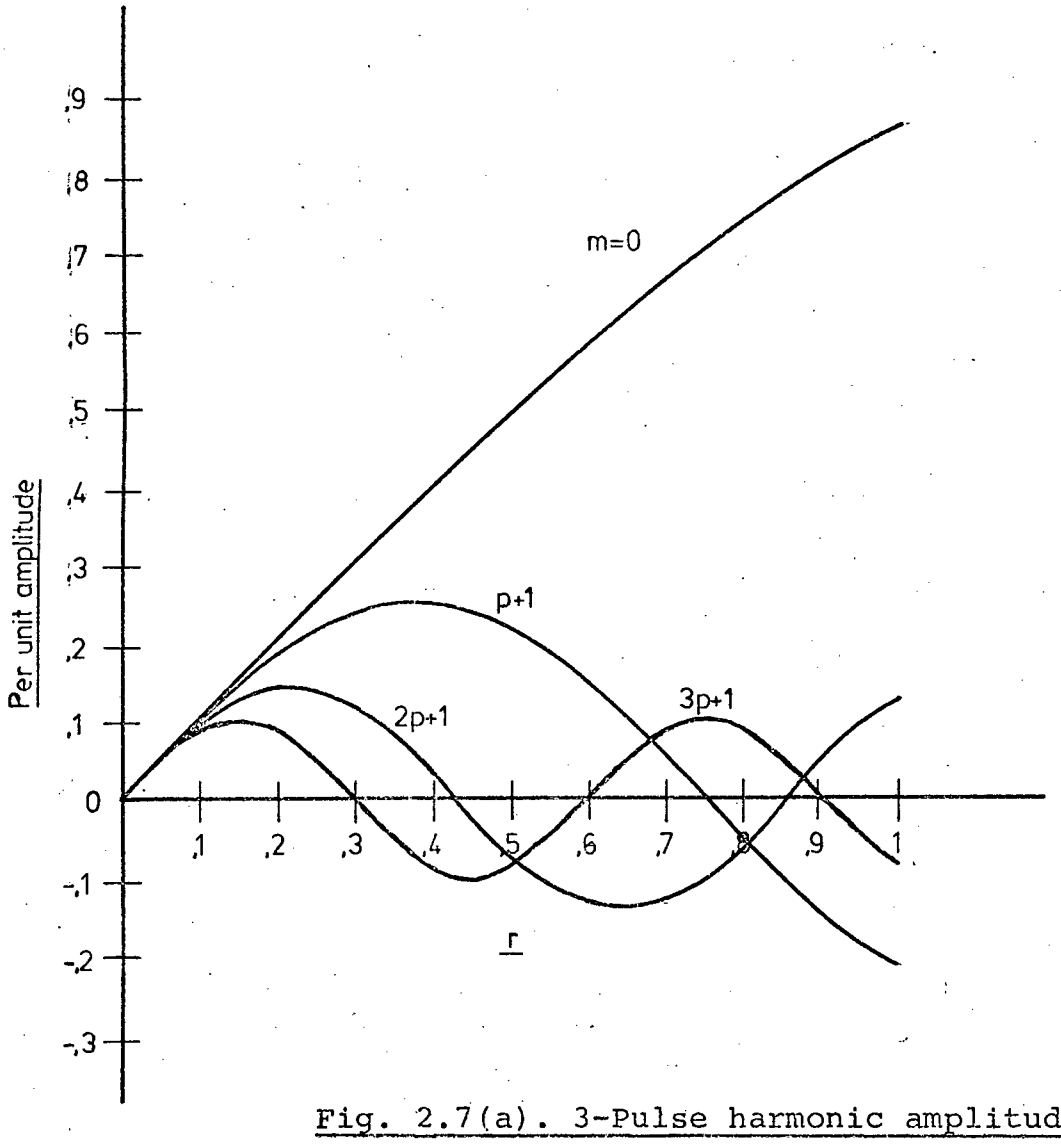


Fig. 2.7(a). 3-Pulse harmonic amplitudes

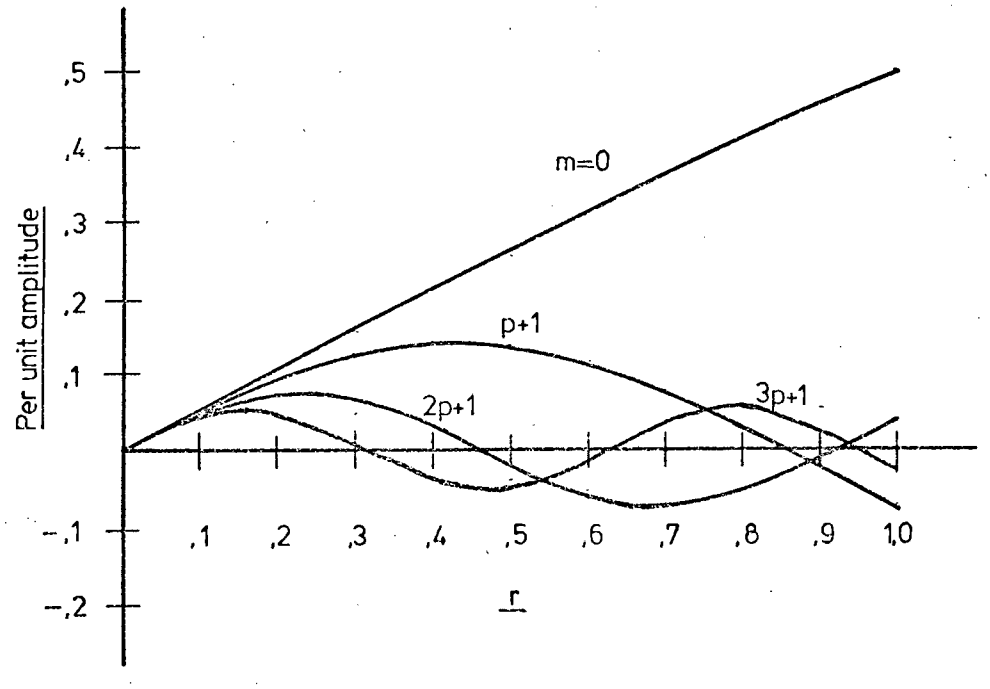


Fig. 2.7(b). 6-Pulse harmonic amplitudes

2.2.2 OUTPUT VOLTAGE HARMONICS:

Unlike the naturally commutated cycloconverter, the harmonics present in the output voltage of the a-mod converter obey a simple relationship as shown in equation (2.5). That is, the relative amplitude of a given harmonic is a function of the pulse ratio $\frac{\tau}{T}$ only, and not of output frequency. Also the frequency of a given harmonic is a function only of input and output frequencies. Note that the word 'harmonic' is used rather loosely here, since the usual meaning of the word applies to simple multiples of some fundamental frequency, whereas in this text the "harmonics" have a frequency (from eqn. 2.5) of:

$$f_m = mpf_i + (mp \pm 1)\, f_o \qquad (2.16)$$

Since however it is customary in current literature to term the higher multiple frequencies of converter-like devices "harmonics", the use of the term is considered justified in this instance.(8,9,10,11,12,13) The relationship between voltage reduction ratio, harmonic amplitude and harmonic frequency is illustrated graphically in figs. 2.7 (a) and 2.7 (b), for the 3 pulse and 6 pulse cases respectively.
The harmonics are of relatively high frequency, the lowest possible being from a 3 pulse converter with D.C. output when the first harmonic to appear occurs at 150 Hz.

These are thus easily filtered, or in the case of an induction motor output, have little effect on motor performance. (7)

However, at small voltage reduction ratios i.e. low output voltages, it is observed that the amplitude of the harmonics is nearly the same as the fundamental frequency. This naturally sets a limit to any filter design, but, as noted above, the wide frequency separation eases the requirements of such a filter. In the case of an inductive load or induction motor load, the harmonic currents are reduced in the ratio:

$$\frac{I_h}{I_f} = \frac{\omega_o}{mp\omega_i + (mp \pm 1)\omega_o} \qquad (2.17)$$

This usually represents a considerable reduction.

2.2.3 OUTPUT VOLTAGE DISTORTION: (Appendix A2)

Since the output voltage contains unwanted frequency components, distortion is present and a means of evaluating this distortion is the distortion factor, defined as: (9)

$$\text{Voltage distortion factor} = \frac{\text{R.M.S. fundamental output voltage}}{\text{R.M.S. total output voltage}}$$

For a 6 pulse bridge configuration, the maximum value of voltage distortion factor is 0,955, and for a 3 pulse midpoint system the corresponding value is 0,826.

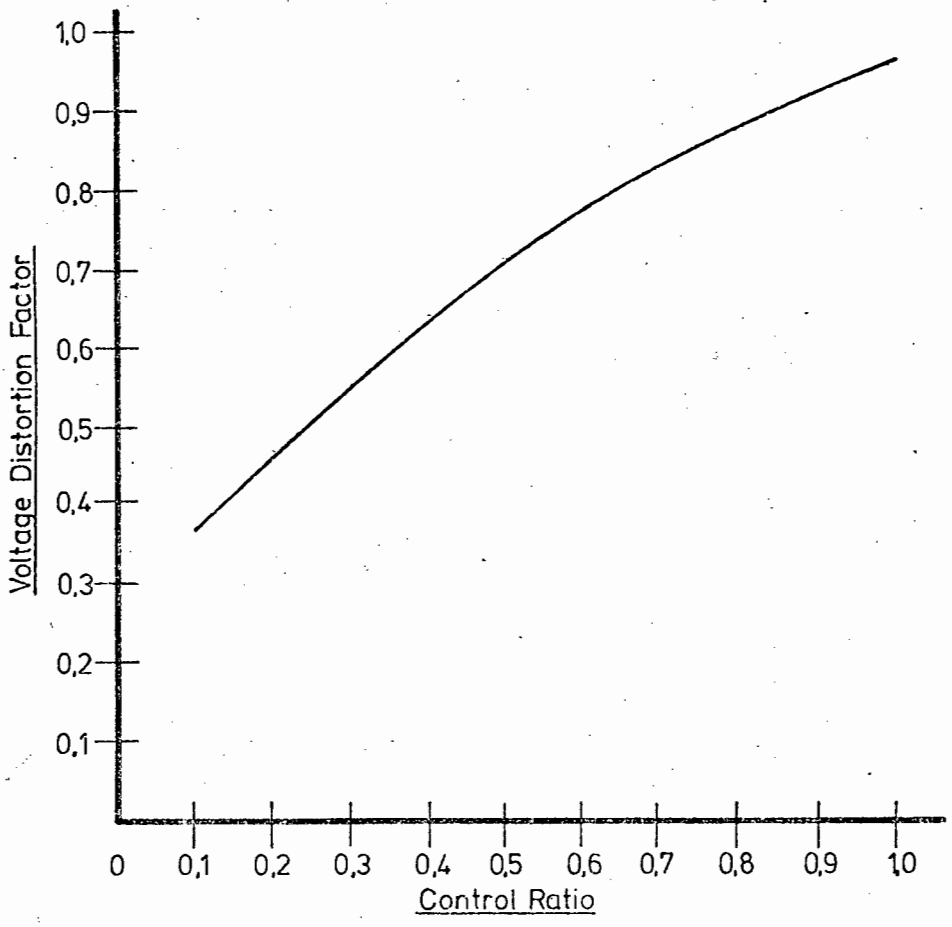


Fig. 2.8(a). 6-Pulse bridge distortion factor

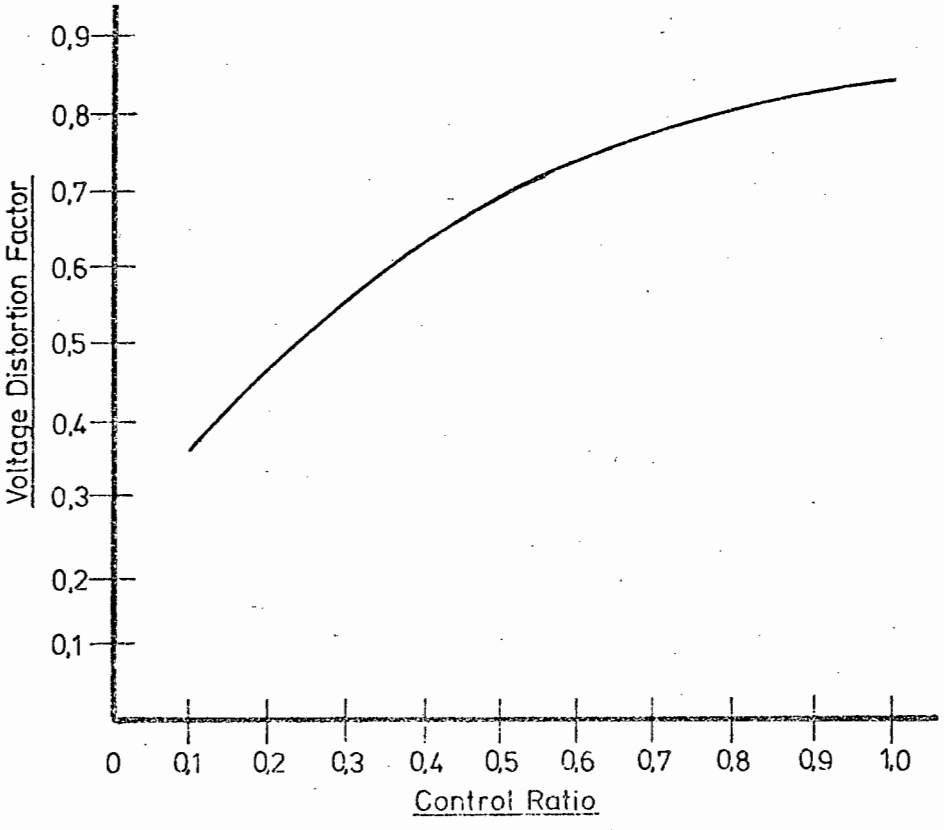


Fig. 2.8(b). 3-Pulse midpoint distortion factor

The maximum values are reached at maximum control pulse duration, and fig. 2.8 (a) and 2.8 (b) show the variation of voltage distortion factor for 6 pulse and 3 pulse systems, respectively.

2.2.4 INPUT CURRENT PER SUPPLY PHASE, SINGLE PHASE OUTPUT: (Appendix A3)

The current which is supplied to the system may be regarded as the (sinusoidal) output current "chopped" by the control pulses. For the 3 pulse midpoint system, this process is illustrated graphically in fig. 2.9.

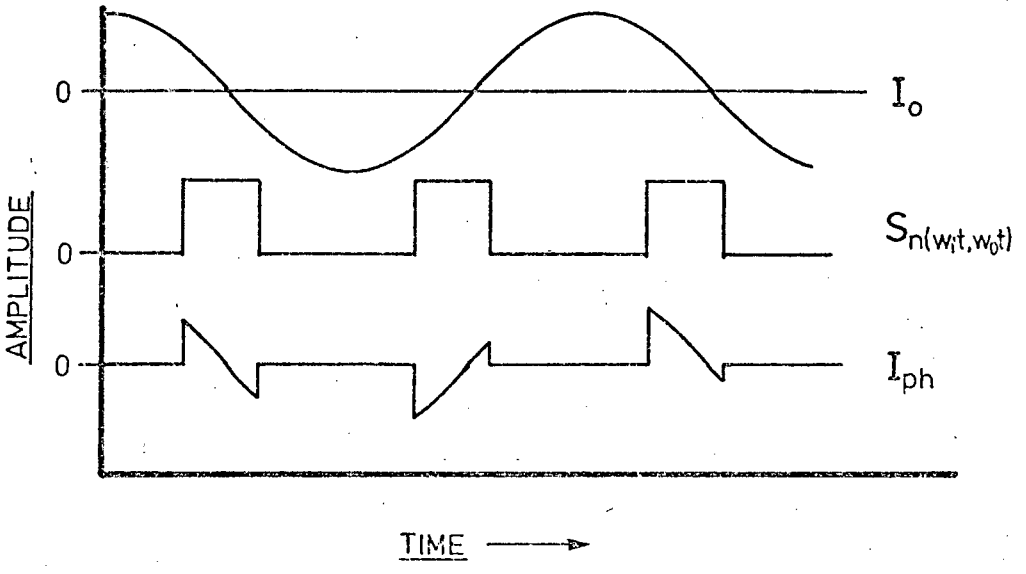


Fig. 2.9. Deriving the input current expression

Using the expression 2.3 for $S_{n(\omega_o t, \omega_i t)}$ and writing

$$i_o = I_o \cos \omega_o t \qquad (2.18)$$

we have:

$$i_{ph} = \frac{\tau}{T} I_o \cos\omega_o t + \frac{2I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\tau}{T}}{(mp \pm 1)} \{\cos\{(mp \pm 1)\omega_i t + mp\omega_o t\}\} \quad (2.19)$$

For the 6 pulse bridge system, the control pulses are effectively modified by the circuit configuration in the manner shown in fig. 2.10:

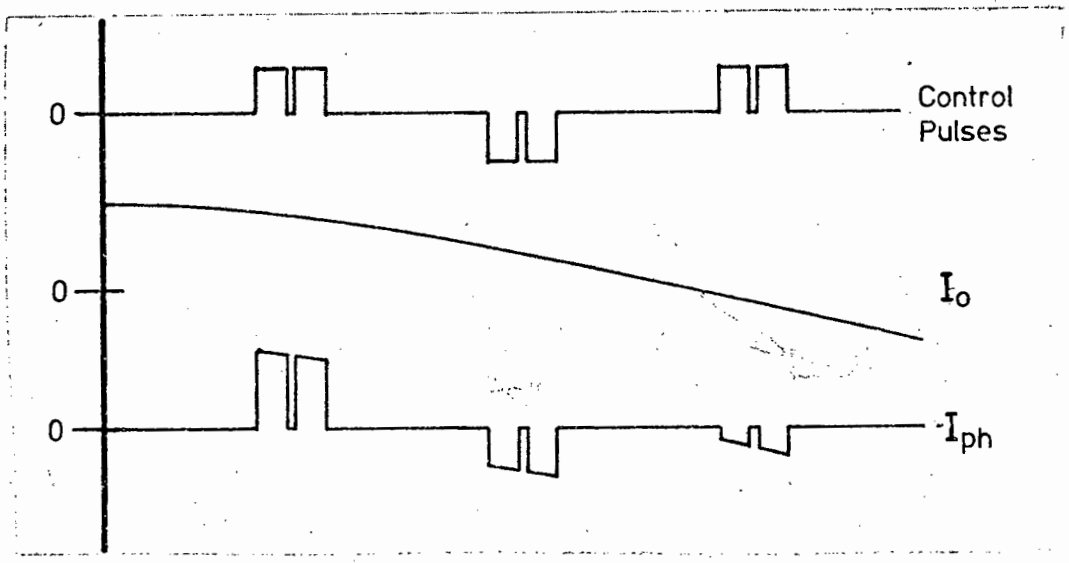


Fig. 2.10. Effective 6-pulse bridge control pulses

This process is like that occuring in the standard bridge converter and cycloconverter systems.
The switching function then becomes:

$$S_{n(\omega_i t, \omega_o t)} = \frac{4\sqrt{3}}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos(mp \pm 1)\{\omega_i t + \omega_o t + \frac{\pi}{6}\}\} \quad (2.20)$$

Using the previous expression for output current, the input current per supply phase is:

$$i_{ph} = \frac{2\sqrt{3}I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{(mp \pm 1)\omega_i t + mp\omega_o t + \frac{(mp \pm 1)\pi}{6}\}\} \quad (2.21)$$

The following are to be noted concerning the input current:

1) The midpoint converter has a component of current at output frequency, which does not occur in the bridge configuration. This process occurs in other converters, and is an advantage of the bridge configuration.
2) The harmonics are never integral multiples of the pulse number and supply frequency, and the amplitude of an harmonic is only a function of harmonic number.
3) The phase angle $\frac{(mp \pm 1)\pi}{6}$ occurs because of the delta connection of the system, while the control pulses and supply voltages are referred to the supply neutral, as in a star connection.
4) The current harmonics are never at the same frequency at the (output) voltage harmonics, having a frequency

$$f_{hI} = (mp \pm 1)f_i + mpf_o \qquad (2.22)$$

whereas the voltage harmonics occur at a frequency

$$f_{ho} = mpf_i + (mp \pm 1)f_o \qquad (2.23)$$

5) The pulse numper p becomes unity when considering a single supply phase, with the proviso that the

quantity mp is never an odd multiple of three. This has the result that an harmonic of large amplitude may be expected at a frequency $(\omega_i + \omega_o)$ when m is unity.

2.2.5 INPUT CURRENT PER SUPPLY PHASE, 3 PHASE OUTPUT:

Three single phase converters may be combined into a three-phase output device as shown in fig. 2.11.

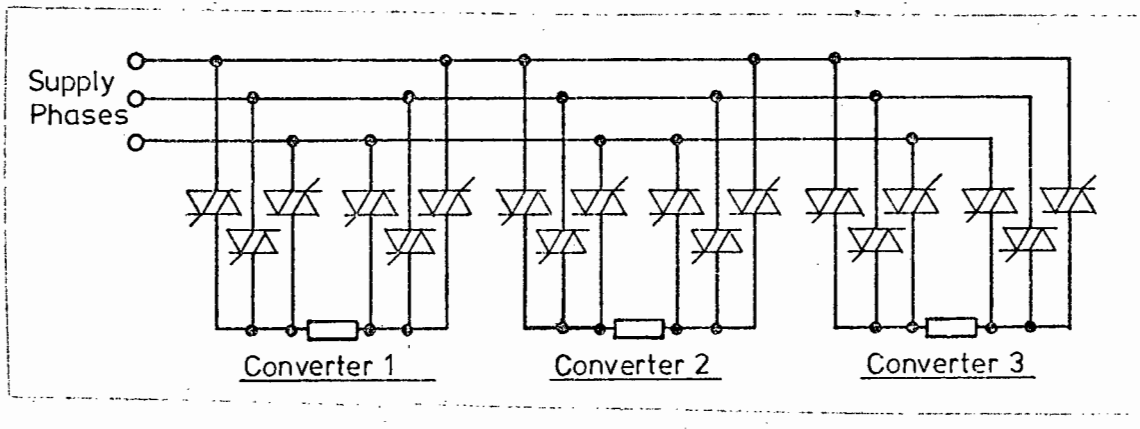


Fig. 2.11. Three-phase bridge converter

Each converter operates independantly and their outputs are combined within the load, usually a 3 phase A.C. motor.

The current per supply phase is then

$$i_{ph} = \frac{6\sqrt{3}I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \left\{\cos\left\{(mp \pm 1)\omega_i t + mp\omega_o t + \frac{(mp \pm 1)\pi}{6}\right\}\right\} \quad (2.24)$$

The pulse number now becomes three, and the harmonic at $(\omega_i + \omega_o)$, associated with the single bridge converter, disappears.

2.2.6 INPUT CURRENT DISTORTION FACTOR (Appendix A4)

The distortion factor of the input current waveform is given by

$$\mu = \frac{\text{R.M.S. fundamental input current}}{\text{R.M.S. total input current}} = \frac{I_1}{I_{r.m.s.}} \qquad (2.25)$$

The 3-pulse midpoint converter with single phase output has a maximum value (of current distortion factor)

$$\mu = 0,68$$

The variation in current distortion factor for the 3 pulse midpoint converter with control pulse duration is shown graphically in fig. 2.12.

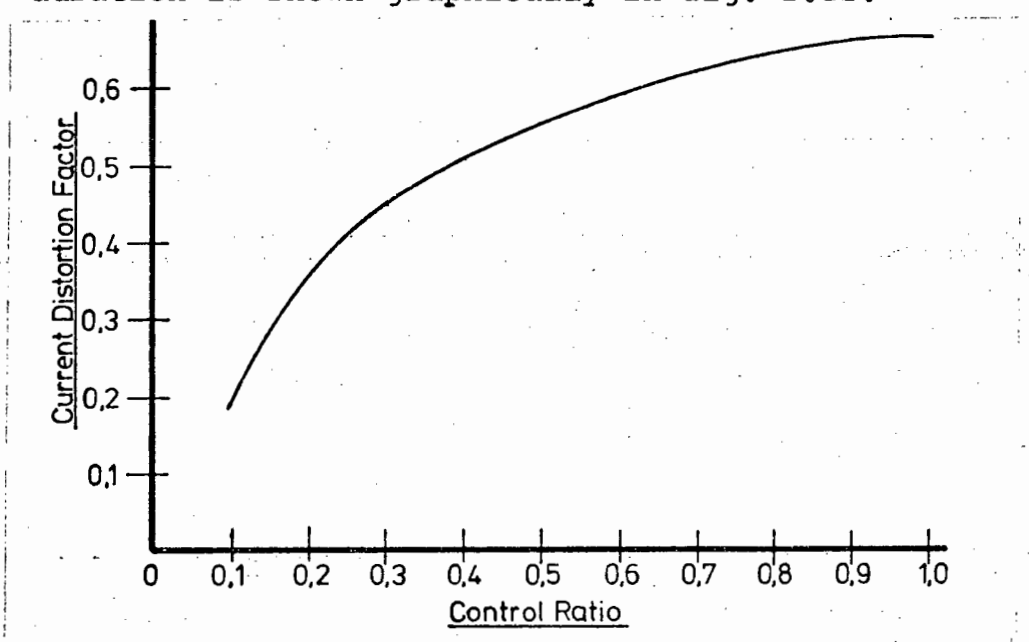


Fig. 2.12. 3-Pulse current distortion factor

The 6 pulse bridge converter, with single phase output, has a maximum current distortion factor of

$$\mu = 0.95$$

The variation in current distortion factor, for the 6 pulse bridge converter, with control pulse duration, is shown graphically in fig. 2.13

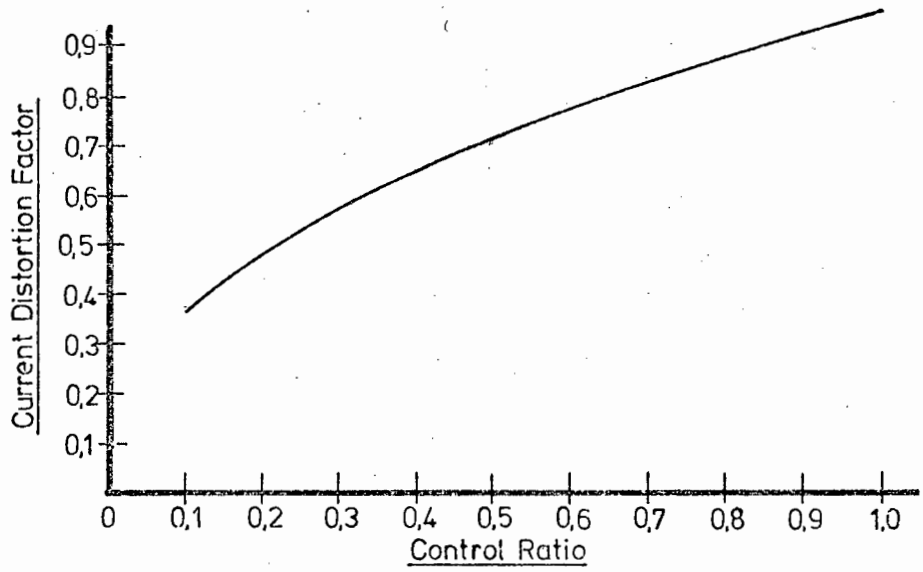


Fig. 2.13. 6-Pulse bridge current distortion factor

For 3 phase output systems, only the 6 pulse bridge converter will be considered as this is the only system likely to be of use in the operation of say a 3 phase induction motor. Fig.2.14 shows how the three converter supply currents are added.

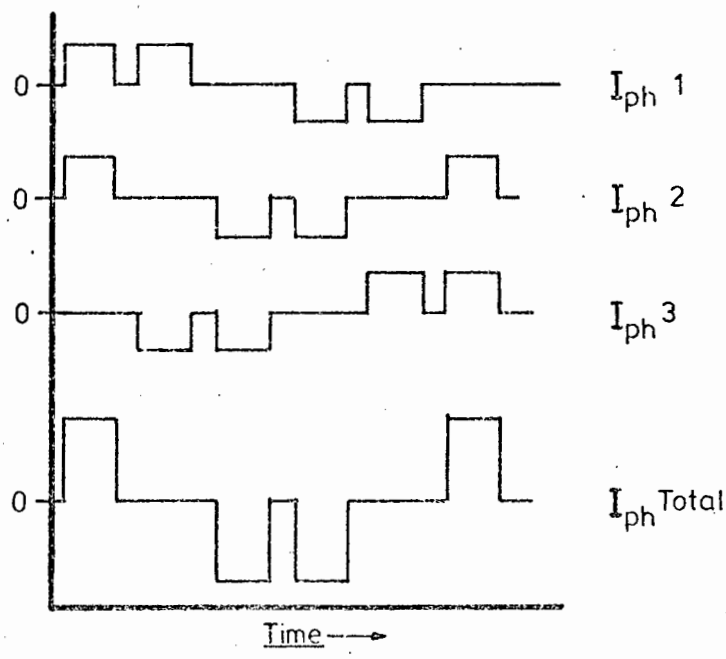


Fig. 2.14. 6-Pulse bridge input currents

The distortion factor is clearly then the same as for the single phase converter, that is:

$$\mu = 0.95 \text{ maximum.}$$

2.2.7 DISPLACEMENT FACTOR AND POWER FACTOR (9,12)

The waveform of the supply current is not as observed in para. 2.2.4, a pure sinusoid. It comprises a fundamental component at supply frequency, and various harmonics. In the case of the midpoint converter, a subharmonic also exists at output frequency.
The angular displacement between the fundamental current component phasor, and the line to neutral voltage phasor is defined as the input displacement angle, denoted by ϕ_i . (9)
The input power factor is defined as the ratio of total mean input power to total mean input volt - amperes. Thus

$$\text{Power factor } \lambda = \frac{P_i}{V_n \times \text{total R.M.S. current}}$$

$$= \frac{P_i}{V_n \times \sqrt{\left(I_1^2 + \sum_{m=0,2,3\ldots}^{m\to\infty} I_m^2\right)}} \qquad (2.26)$$

Now , as shown previously , the input current distortion factor is :

$$\mu = \frac{I_1}{\text{Total R.M.S. input current}} .$$

$$= \frac{I_1}{\sqrt{(I_1^2 + \sum_{m=0,2,3,\ldots}^{m\to\infty} I_m^2)}} \qquad (2.27)$$

From 2.26 and 2.27 ,

$$\lambda = \mu \times \frac{P_i}{V_n I_1}$$

$$= \mu \cos \phi_i \qquad (2.28)$$

The input displacement angle is a function of the load which is presented to the output of the converter, and this has not been considered up to this point in the text.

Noting that the switching function which produces the output voltage is the same as the switching function responsible for the nature of the input current, and that the output voltage is assumed to be in phase with the supply phase which is under consideration for the purposes of power factor etc. evaluation, it follows that any displacement between output current and voltage is reflected to the input such that

$$I_{ph} = \frac{2\sqrt{3}I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp\pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{(mp\pm 1)\omega_i t + mp\omega_o t + \frac{(mp\pm 1)\pi}{6} \ldots$$

$$\ldots + \phi_i\}\} \qquad (2.29)$$

for the 6-pulse bridge converter.

The fundamental component of input current then becomes

$$I_1 = \frac{2\sqrt{3}}{\pi} \sin\frac{\pi\tau}{T} \cos(\omega_i t + \frac{\pi}{6} + \phi_i) \qquad (2.30)$$

which yields a maximum value

$$I_{1max} = 0{,}55 \cos(\omega_i t + \frac{\pi}{6} + \phi_i) \qquad (2.31)$$

Thus the input power factor for the 6-pulse bridge converter with single phase output is limited to a maximum value of 0,827.

Now if the switching sequence of the converter is such that

$$\omega_m = \omega_o + \omega_i \qquad \text{and} \qquad \omega_o < \omega_i$$

then the phase rotation of the output is opposite to that of the supply, and thus

$$I_{ph} = \frac{2\sqrt{3}I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp\pm1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{ - \{(mp\pm1)\omega_i t + mp\omega_o t\} + \ldots$$

$$\ldots\ldots + \frac{(mp \pm 1)\pi}{6} + \phi_i\}\} \qquad (2.32)$$

This yields a fundamental current

$$I_1 = \frac{2\sqrt{3}}{\pi} \sin\frac{\pi\tau}{T} \cos(-\omega_i t + \frac{\pi}{6} + \phi_i)$$

The ruggedness of the thyristor and triac make these very attractive, but the turn-off problem poses many difficulties. These could be overcome with further work, and the recently-available gate turn-off thyristor appears to be a strong contender in the future.

The power transistor with its fully controlled transfer characteristic has been found the most easily employed device for implementing the switch. Transistors with VCEX ratings of 800 V and maximum collector current of 15 amps are now readily available in quantity, and accordingly it is on this device that attention will be focussed.

Another likely device which shows great promise is the V-MOS field-effect transistor. It has the speed, current and voltage ratings to be very effective, and does not need an elaborate drive circuit like the bipolar transistor. This device was, however, not readily available when this work was carried out, but is the device most likely to be used for future investigations.

3.5.1 THE POWER TRANSISTOR:

The transistor operating as a switch, that is, in the large-signal mode, has been well-described in much literature over the past years, thus it is proposed to deal only briefly with the salient points of transistor theory relevant to the development of the switch. Attention will be focussed in particular on the type BUY69B which has sufficient voltage and current

or

$$I_1 = \frac{2\sqrt{3}}{\pi} \sin\frac{\pi\tau}{T} \cos(\omega_i t - \frac{\pi}{6} - \phi_i)$$

This yields the interesting result that the phase angle ϕ_i is changed from a positive value to a negative value. Which means that a load with lagging power factor is converted to a leading power factor and vice versa. If, however, the switching sequence is such that

$$\omega_m = \omega_i - \omega_o$$

then the phase rotations of the output and the supply are identical. The power factor inversion does then not occur.

This phenomenom of power factor inversion is also noted by Schauder (ref.7) , apparently as an empirically observed event .

CHAPTER 3

THE ELECTRONIC SWITCH

3.1 INTRODUCTION:

The frequency conversion process outlined in Chapter 2 of this work has depended on the existence of some switching device capable of successively connecting a load to one of several supply phases. It is now proposed to examine this switch in detail.

The operation of the switch proposed in this chapter depends on the load having an inductive characteristic, and this is thus the basic assumption. Since the usual load demanding frequency conversion is some form of induction motor, this assumption is valid. However, if the inductance of the load is negligible, the effect on the switch is not disastrous.

3.2 COMMUTATION: (17)

The operation of disconnecting a load from one supply and reconnecting it to another is known as commutation, which finds its most familiar application in the commutator of the D.C. machine. The proposed switch thus is a commutator, from the definition of a commutator: "A contrivance for altering the course of electric current". This is from the Latin 'commutare'. (O.E.D.)

To be successful, a commutator must perform the disconnection and reconnection without causing either a discontinuity in the load current or a short circuit of the supply. As there could be a voltage difference

between supply phases at the instant of commutation, the commutator must supply any e.m.f. required to maintain the integrity of Kirchoff's Loop Law. The time required for commutation is also important in view of the limits imposed on conduction times by the 50 Hz (or 60 Hz) supply frequency.

3.3 FUNDAMENTAL PRINCIPLES OF COMMUTATION IN THE A-MOD CONVERTER: (24)

The basic circuit shown in fig. 3.1 represents the current elements involved in the commutation process.

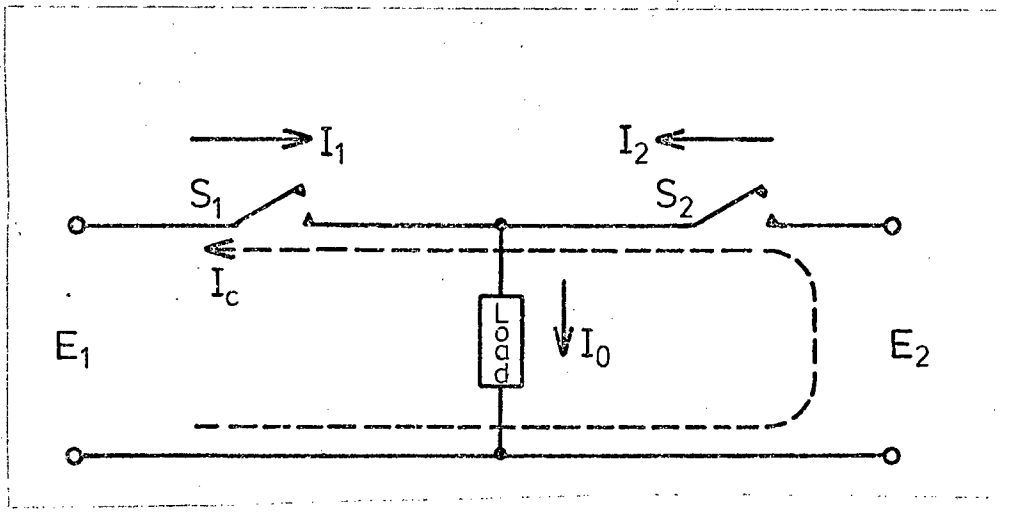


Fig. 3.1. The commutation process

The load is transferred from supply 1 at voltage E_1 to supply 2 at voltage E_2 during a time T_c, while maintaining load current I_o constant. The transition will take place if at all times

$$I_1 + I_2 = I_o \qquad (3.1)$$

and $$I_1 - I_2 < I_o \qquad (3.2)$$

and $$I_1 - I_2 > -I_o \qquad (3.3)$$

finally $I_1 = 0$ and $I_2 = I_o$ at the end of the commutating period T_c.

The equation (3.1) indicates the condition of constant voltage across the (inductive) load, thus avoiding sudden excessive voltage excursions. The equation (3.2) sets limits to the currents and indicates the avoidance of supply short circuits.

The commutation process may be regarded as the superposition of a commutating current I_c on the currents I_1 and I_2. Ideally,

$$I_c = I_o \frac{t}{T} \qquad (3.4)$$

The time t is measured from the commencement of the commutation process.

The commutation time is short, of the order of 50 μsecs., (which will be shown later) which indicates that the loop (fig. 3.1) $E_1 - S_1 - S_2 - E_2$ should have low inductance. Conversely, the stray inductance of this loop sets some of the limits to the commutation. If all the stray loop and supply inductances are lumped together as L_s, then

$$E_c = L_s \frac{dI_c}{dt} = L_s \frac{I_o}{T_c} \qquad (3.5)$$

where E_c is an additional commutating voltage. That is, when the supply current is interrupted an additional voltage appears in series with the supply. The switch has to withstand this and so the various circuit parameters must be adjusted to maintain the increase within permissible bounds.

The commutating process from E_1 to E_2 requires that the impedances of S_1 and S_2 go from zero to infinity and vice versa respectively. (Assuming pure resistance, T_c

must be short to avoid excessive losses.) The circuit equations must then be:

$$E_1 - L_o \frac{dI_o}{dt} = E_2 + L_o \frac{dI_o}{dt}$$

$$\text{Thus} \longrightarrow \quad \frac{dI_o}{dt} = \frac{E_1 - E_2}{2L_o} \qquad (3.6)$$

$\frac{E_1 - E_2}{2}$ represents the e.m.f. appearing in the circuit to make the commutation process possible. If the commutation time is short, then this e.m.f. is small and the load current is virtually constant. Linear commutation takes place, that is, the currents I_1 and I_2 vary as linear functions of time during the period T_c.

The switches S_1 and S_2 may be represented as variable resistors R_1 and R_2 respectively, and then

$$R_1 = \frac{E_2 - E_1}{I_o} \cdot \frac{T_c}{T_c - t} \qquad (3.7)$$

$$R_2 = \frac{E_2 - E_1}{Io} \cdot \frac{T_c}{t} \qquad (3.8)$$

The voltage across the load V_o is maintained constant at

$$V_o = \frac{E_1 + E_2}{2} \qquad (3.9)$$

In the motor speed control system outlined here, the load is commutated between a supply voltage E_s and a short circuit (zero voltage condition), when it is desired to control the average voltage across the load by "chopper" control. The second switch then forms a freewheel path for the load current which is maintained through it.

3.4 DIFFICULTIES IN THE COMMUTATION PROCESS AND THEIR SOLUTION:

There are two problems occurring during the commutation process.

Firstly, when the load possesses back-e.m.f., as in an induction motor, there is a clear dichotomy between

motoring and regeneration. That is, during motoring, the E_1 to E_2 transition is only possible when E_2 is greater than E_1. During regeneration, E_1 must be greater than E_2. These are normal limitations occurring with rectifier and inverter systems where similar commutation processes take place.

In the second case it has been found virtually impossible to generate the functions described by equations (3.7) and (3.8) with the required degree of accuracy. Small errors result in excessive voltages or currents appearing in the circuit. Since the switching operation was finally executed by means of transistors, the limited overload capability of the transistor made it imperative to ensure that commutation was controlled within strict bounds.

The method of ensuring correct commutation is to turn off say S_1 in some manner which is non-critical provided the operation is completed well within the commutation period. This operation would produce a high value of $\frac{d I_o}{dt}$, which is then used to turn S_2 on. That is, the voltage across the device produced by the switch going off is used to assist the turn-on operation of the switch going on. The large value of $\frac{d I_1}{dt}$ is balanced by $\frac{d I_2}{dt}$ so that

$$\frac{dI_1}{dt} - \frac{dI_2}{dt} = \frac{dI_o}{dt} \qquad (3.10)$$

In this situation a commutation voltage is available which is

$$E_c = \frac{dI_o}{dt} L_L - E_L - I_o R_L + E_2 \qquad (3.11)$$

in the case of a load with a back-e.m.f.

The commutation voltage is coupled to the control

terminal of the switch by some appropriate means, and this drives the switch to the desired conduction state. The switch is kept in conduction by the application of a further signal.

This addition to the commutator circuit is shown in fig. 3.2.

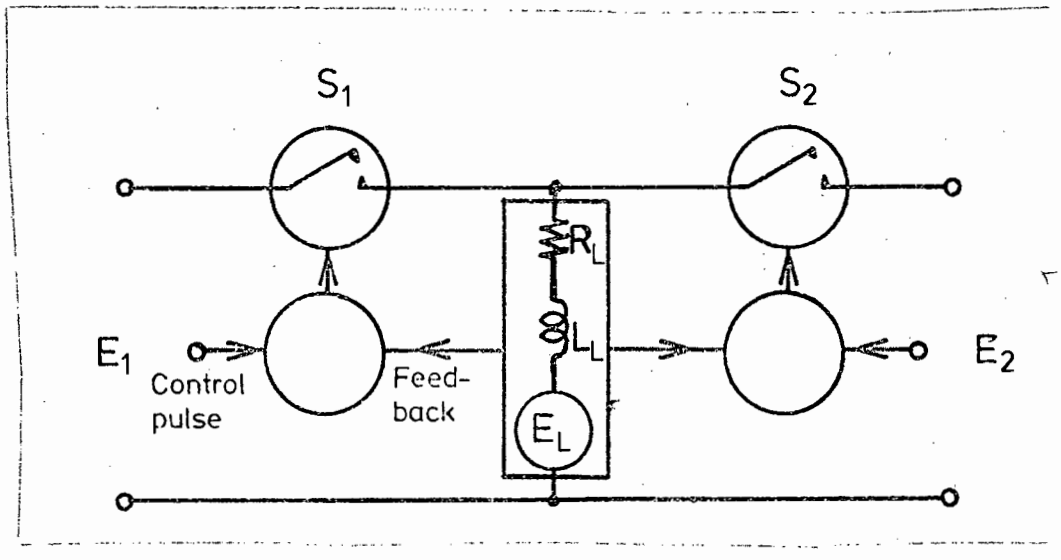


Fig. 3.2. Commutation circuit with feedback

Another approach to the problem is to use a current overlap system. Here the switch S_2 (in the $E_1 \rightarrow E_2$ transition) is turned on in a non-critical manner. This would produce an excessive short-circuit current, but this is prevented by some current sensor turning switch S_1 off, such that at all times equation (3.1) is maintained. This scheme is shown in fig. 3.3. In practice this arrangement has proved difficult to implement owing to the high speed, sensitivity and linearity demanded of the current transducers, although it remains a possibility for further investigation.

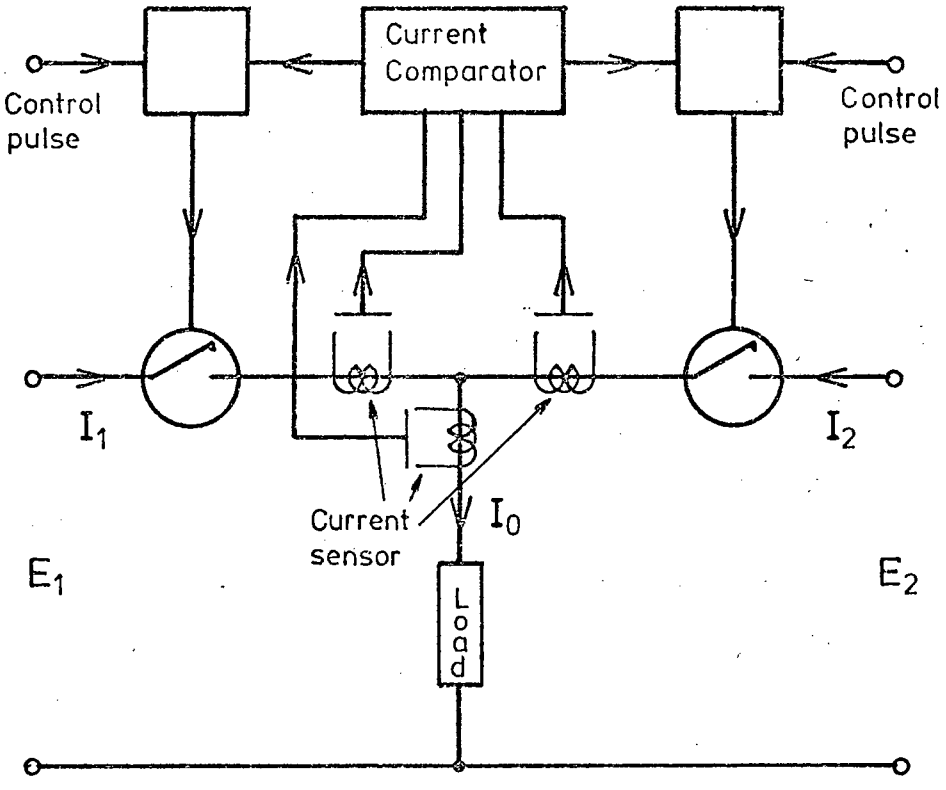


Fig. 3.3. Current sensor feedback

3.5 IMPLEMENTATION OF THE SWITCH:

The individual switches of the commutator are identical, thus the practical implementation of only one switch will be considered.

Although bidirectional current flow is required, and most available electronic devices only permit unidirectional current flow, this problem is easily overcome by using a diode bridge circuit as in fig. 3.4.

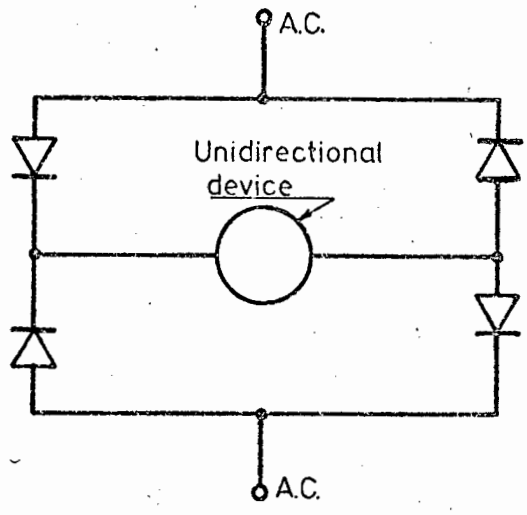


Fig. 3.4. Diode bridge for bidirectional current flow

The available devices are listed below with their advantages and disadvantages.(2, 3, 8, 9, 10, 11, 13, 18, 19, 21, 22, 23.)

DEVICE	ADVANTAGES	DISADVANTAGES
Relay	High current capability. High withstand voltage capability. Low "on" resistance. Very high "off" resistance. Economical.	Slow speed. Uncontrolled transition from "off" to "on". Prone to contact bounce.
Electron Tube	High speed. High withstand voltage. High "off" resistance.	Low current. High "on" voltage. Costly. Needs filament supply.

DEVICE	ADVANTAGES	DISADVANTAGES
Thyristor (Silicon controlled rectifier)	High current overload capability. Sufficiently fast. High withstand voltage. Easy to trigger to conducting state. No continuous control current needed to maintain conduction.	No intrinsic turn-off capability. No control over "off" to "on" transition.
Triac	As for thyristor with additional advantage of bi-directional current flow.	As for thyristor with limited speed.
Bipolar Transistor	Fast. Fully controllable under all conditions.	Very limited overload capabilities of both current and voltage. Requires continuous drive current to maintain conduction. Limited choice of available devices with ratings suitable for proposed application. Prone to second breakdown.

Two devices from the above list may be eliminated. These are the relay and electron tube (valve). The relay is slow and does not have the smooth resistance variation demanded by equations (3.7) and (3.8). The electron tube, now virtually obsolete, is difficult to obtain in the current ratings required for motor control. (That is, a current capability of some 10 amps as a minimum.) The sheer size of a tube of this rating would make the system unattractive, as well as the present-day cost of such devices being prohibitive.

The ruggedness of the thyristor and triac make these very attractive, but the turn-off problem poses many difficulties. These could be overcome with further work, and the recently-available gate turn-off thyristor appears to be a strong contender in the future.

The power transistor with its fully controlled transfer characteristic has been found the most easily employed device for implementing the switch. Transistors with VCEX ratings of 800 V and maximum collector current of 15 amps are now readily available in quantity, and accordingly it is on this device that attention will be focussed.

Another likely device which shows great promise is the V-MOS field-effect transistor. It has the speed, current and voltage ratings to be very effective, and does not need an elaborate drive circuit like the bipolar transistor. This device was, however, not readily available when this work was carried out, but is the device most likely to be used for future investigations.

3.5.1 THE POWER TRANSISTOR:

The transistor operating as a switch, that is, in the large-signal mode, has been well-described in much literature over the past years, thus it is proposed to deal only briefly with the salient points of transistor theory relevant to the development of the switch. Attention will be focussed in particular on the type BUY69B which has sufficient voltage and current

capability to make the experimental realisation of the circuit possible. Manufacturers' specifications are reproduced in Appendix 5.

The device will be examined with regard to the base drive circuitry, the maximum ratings and the collector circuit.

3.5.2 THE TRANSISTOR BASE DRIVE CIRCUIT: (19, 20, 21, 22)
The circuit supplying current to the base of the power transistor must be able to switch the transistor on under the control of the feedback circuit and turn the transistor off under the control of the system control circuit.

The transistor exhibits certain inherent qualities which affect the turn-on process. These are

* Turn-on delay
* Turn-on rise-time.

The turn-on delay represents the time required to supply charge to the collector-base and emitter-base junction depletion layer capacitances. The data sheet of the BUY69B transistor (Appendix 5) shows that this represents a time of 0,08 μsec, independent of collector current or base current.

The turn-on rise time represents the time required for the base circuit to supply charge to do the following

* Change the collector current to a new value
* Change the collector voltage
* Allow for recombination of charge carriers (recombination current).

The rise time is thus a function of collector and base currents, but a quantitative evaluation is laborious and not relevant in this context, since the rise of the collector current depends on the load impedance, and the recombination current is the ratio of collector current to D.C. current gain. However, curves of rise time, as a function of collector current with collector current to base current ratio as parameter, are provided (Appendix 5). From this it can be seen that the family of curves tends asymptotically to a rise time of 2 μsecs at a collector current of 10 A.

Thus, the delay inherent in the device, depending on the spread of characteristics among various samples, could be of the order of 3 μsecs. As a design limit it is proposed to use a figure of 5 μsecs. This means that any feedback system would be ineffective during this period.

Forward-bias second breakdown is a phenomenon which imposes a limitation on the operation of a transistor at high power levels.(21) It is caused by the focussing of the charge carriers around the outer perimeter of the emitter by the transverse electric field of the base region. This causes localised heating or "hot spots" and ultimate failure of the device. The severity of the hot spots is inversely proportional to the width of the transistor base (hence the frequency capability) and the applied collector to emitter voltage. The following empirical relations hold:

$$Is/b = \frac{K_1}{f_t} \qquad (3.12)$$

and

$$Is/b = \frac{K_2}{V_{CE}^n} \qquad (3.13)$$

The value of the constant n ranges from 1,5 to 4, depending on the transistor construction.

Forward-bias second breakdown is not as severe as reverse-bias second breakdown, which occurs on turn-off, but is a factor which must be taken into account by avoiding a condition of simultaneous high voltage and high current.

Once the transistor has passed the turn-on transient stage, a steady current is required into the base to maintain the collector current. The usual relationship is

$$I_C = h_{FE} I_B \qquad (3.14)$$

However, at high collector currents the current gain h_{FE} no longer remains constant. This fall off in gain is due to the transverse volt drop across the active part of the base caused by the intrinsic resistance of the base material. Basic transistor theory predicts that the collector current is an exponential function of base-emitter voltage, i.e.

$$I_C = f\ (\exp \frac{qV_{eb}}{kt}) \qquad (3.15)$$

This relationship no longer holds at high current, as fig. 7 of Appendix 5 indicates. Noting further that the maximum base current is given as 3,0 A, a base current of 1,5 A is accordingly selected which would result typically in a collector current of maximum 7,5 A, depending on load impedance and supply voltage. This is considered sufficient for an experimental model.

The turn-off process requires that the charge imparted to the transistor by the base and collector currents be removed, and that the base-emitter voltage

be reduced to the point where the base-emitter current ceases. Turn-off falls into two regions. These are

* Storage time
* Fall time.

Storage time results from a transistor being driven into saturation by a base current such that

$$I_B > \frac{I_C}{h_{FE}} \qquad (3.16)$$

When a transistor is in saturation the collector-base junction is forward-biased and the collector injects charge carriers into the base. As a result, excess charge accumulates in the base, and this charge has to be removed for the transistor to be turned off. Since it is proposed to maintain a constant base current of some 1,5 A, whereas the collector current may vary over the range 0 → 7,5 A, it would be desirable to keep the transistor out of saturation to avoid unpredictable storage times. The Baker clamp (19) is one such circuit which does provide a means of avoiding this problem.

Fall time occurs while the transistor is in the active region, and is the time required to remove the charge after the storage time, reducing the collector current to zero. Recombination aids this process, and fall times of the order of 1 μsec apply to the BUY69B transistor selected for this application; see Appendix 5, fig. 9.

The removal of charge from the base may be regarded as the effective reversal of the base current during turn-off, and thus this process is expedited by applying a negative voltage to the base-emitter junction. The amount of negative bias is limited by the

emitter-base reverse breakdown voltage, which is of the order of -8 volts for the BUY69B transistor. To avoid this extreme a negative bias of -2 volts is proposed. It should be noted that in this application, the negative feedback system makes the turn-off process non-critical, and any limitation is due to second breakdown and power dissipation considerations.

Reverse-bias second breakdown occurs during turn-off, and occurs when the reverse base current causes the emitter current to be focussed near the centre of the emitter. The current is crowded into a smaller area than is the case with forward-bias second breakdown and thus reverse-bias second breakdown occurs at lower energy levels. (It is usual to refer to second breakdown energy levels since voltage, current and time are involved.)

The transverse base field which causes this phenomenon is a function of turn-off base current and voltage. This means that a compromise must be reached between rapid turn-off and second breakdown. Since no data is available on the transistor selected, the value of reverse base-emitter voltage appears to be a fair compromise, confirmed by successful experimental operation.

3.5.3 TRANSISTOR OPERATING LIMITS: (22)

Any component will continue to operate satisfactorily only as long as the maximum operating conditions, which are set by the physical properties of the device, are not exceeded. In the case of the power transistor these

are

* Collector current
* Collector-emitter voltage
* Second breakdown
* Maximum dissipated power.

As has been indicated in section 3.5.1, the collector current reaches a limit when the base circuit is no longer able to inject more charge into the transistor. Any attempt to increase the collector current by variations in the load impedance or supply voltage only result in an increase in collector-emitter voltage which causes overheating of the device and eventual thermal destruction. The BUY69B (which is the transistor proposed for this model) has a continuous collector current rating of 10 A and a peak pulse rating, for pulses less than 500 μ sec duration, of 15 A. The previously proposed limit, arrived at from base current considerations, of 7,5 A, offers then a reasonable safety margin.

The maximum collector-emitter voltage depends on several factors. These are current level, base-emitter bias and mode of variation of current level. Two values are usually quoted. These are $VCEO_{(SUS)}$ and VCEX. The former applies when the base is open-circuited (or driven from a high-impedance source) and the latter applies to the condition when a reverse bias is applied to the base-emitter junction. The value of $VCEO_{(SUS)}$ depends on whether it is measured under conditions of reducing or increasing current; the former giving a lower value than the latter. These quantities and their

relationship to other transistor parameters are shown in figs. 3.5(a) and (b).

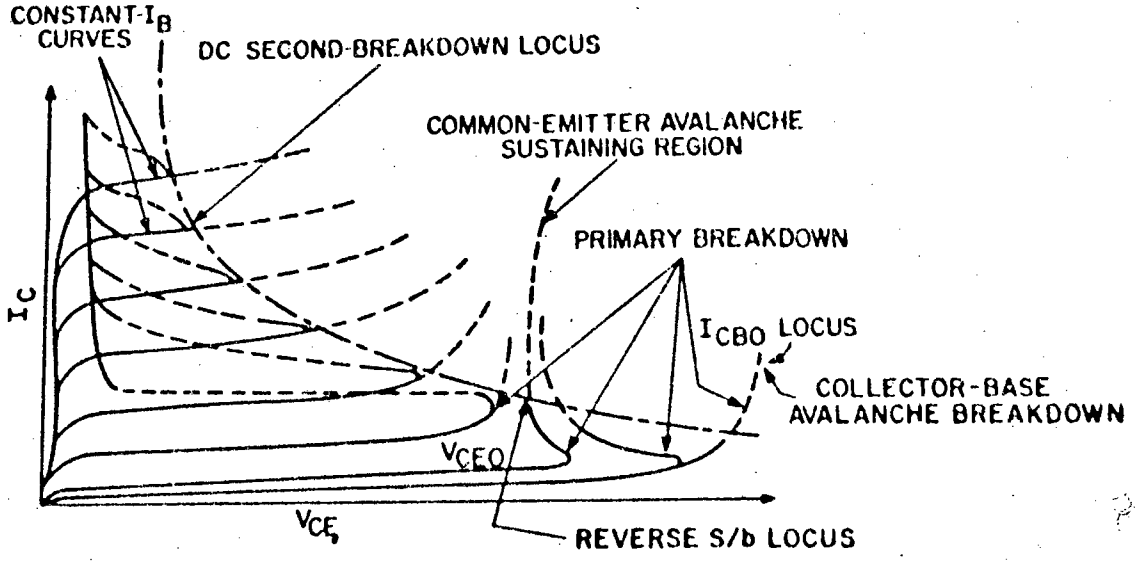


Fig. 3.5(a). Transistor parameters

Maximum dissipated power may be regarded in three stages:

* Switching losses
* "Off" condition losses
* "On" condition losses.

If one assumes linear commutation, which is dependent on the feedback system operating correctly, then the collector current and voltage would ideally be represented by fig. 3.6, and switching times would be equal.

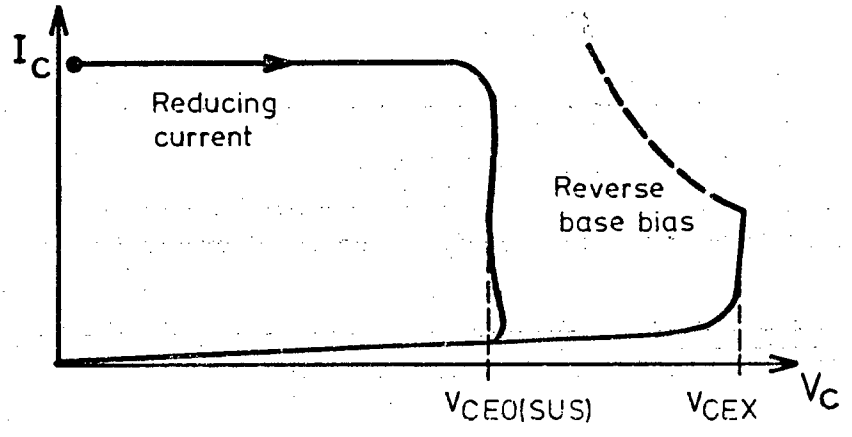


Fig. 3.5(b). Effect of current on collector voltage

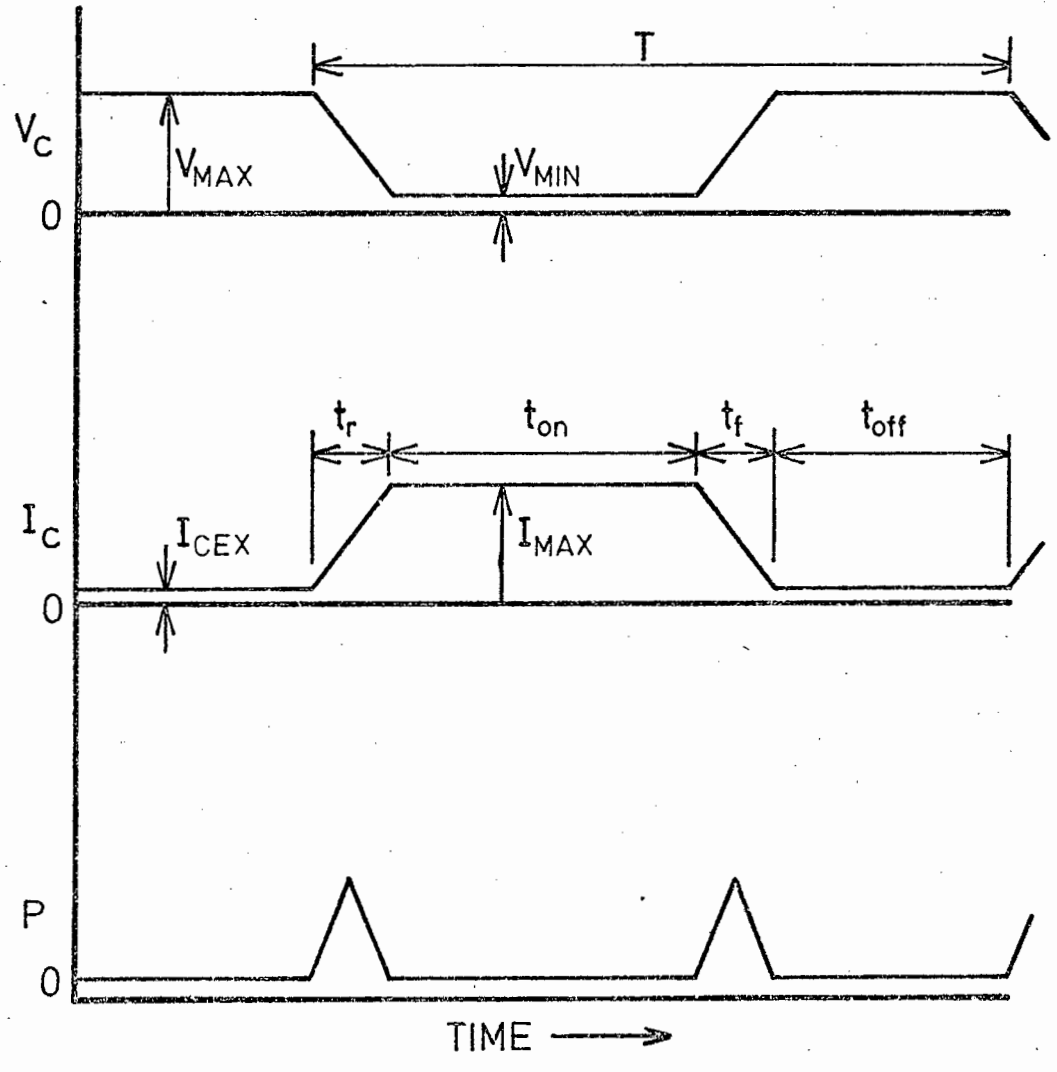


Fig. 3.6. Transistor switching times and other parameters

The switching losses are then represented by (19)

$$P = \underbrace{\frac{1}{T}\int_0^{t_r}\left\{V_{max} - \frac{(V_{max} - V_{min})t}{t_r}\right\}\left\{\frac{I_{max}\,t}{t_r}\right\}dt}_{\text{Turn-on loss}} + \underbrace{\frac{1}{T}\int_0^{t_f}\left\{V_{min} + \frac{(V_{max} - V_{min})t}{t_r}\right\}\left\{I_{max} - \frac{I_{max}\,t}{t_r}\right\}dt}_{\text{Turn-off loss}} \qquad (3.17)$$

It is assumed that the transistor leakage current ICEX is negligible during the switching interval; since

ICEX = 1,0 mA typically for the BUY69B, this assumption is valid.

Furthermore, if it is assumed that the minimum voltage across the transistor may also be ignored, and that rise and fall times are equal, where $t_r = t_f = t_s$

$$P = \frac{2V_{max}I_{max}}{T} \int_o^{t_s} \left(1 - \frac{t}{t_s}\right)\left(\frac{t}{t_s}\right)dt = \frac{V_{max}I_{max}t_s}{3T} \quad (3.18)$$

The "on" condition losses are given by

$$P = \frac{1}{T} \int_o^{t_{on}} I_{max}V_{min}dt = \frac{V_{min}I_{max}t_{on}}{T} \quad (3.19)$$

Finally the "off" losses are given by

$$P = \frac{1}{T} \int_o^{t_{off}} V_{max}I_{min}dt = \frac{V_{max}I_{min}t_{off}}{T} \quad (3.19)$$

The total losses then are given by

$$P = \frac{V_{max}I_{max}t_s + 3V_{min}I_{max}t_{on} + 3V_{max}I_{min}t_{off}}{3T} \quad (3.20)$$

The effect of second breakdown has been discussed in section 3.5.1, and the limiting effect of this phenomenon is expressed in the safe-area rating of the transistor. This comprises a log-log plot of collector current vs. collector-emitter voltage, and is stated for reverse-bias and forward-bias conditions. The forward-bias safe area rating indicates both thermal and second breakdown limits, and fig. 2 of Appendix 5 shows this rating for the BUY69B family of transistors. The switching circuit must ensure that, depending on the pulse duration, the locus of collector current and collector-emitter voltage must remain within the boundaries of the safe area of operation.

The reverse-bias safe area of operation is not available for the BUY69B family, but should quote

figures of minimum second breakdown energy as a function of base-emitter resistance and base-emitter voltage for constant values of collector load series inductance.

All safe area of operation ratings have junction temperature as parameter; those quoted for the BUY69B family are at 200°C.

3.5.4 THE COLLECTOR CIRCUIT AND THE INFLUENCE OF THE LOAD THEREON:

The operation of the transistor switch as a device exercising control over the typical type of load postulated in Chapter 2, i.e. the winding of an a.c. motor, assumes two distinct phases. These are turn-on and turn-off, and accordingly the description of the circuit operation will follow this dichotomy.

3.5.4.1 CIRCUIT BEHAVIOUR AT TURN-ON: (22, 24)

The complete circuit at turn-on may be represented as in fig. 3.7. The load comprises a series-parallel circuit

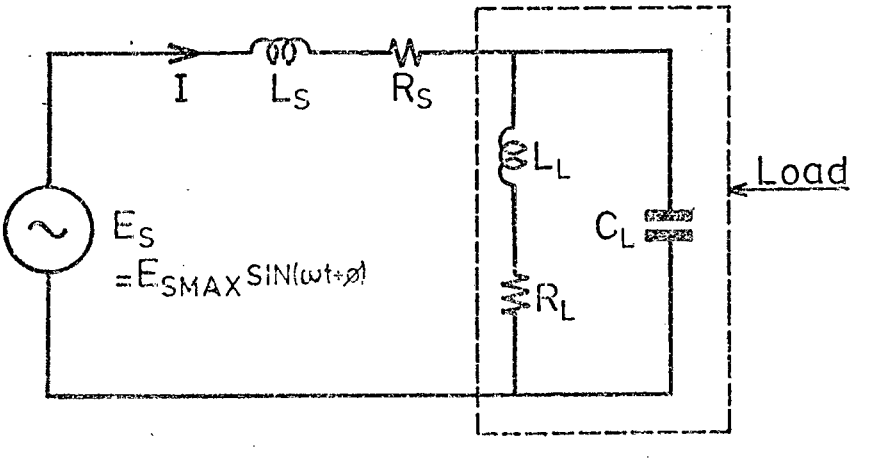


Fig. 3.7. Effective circuit at turn-on

R_L, L_L, C_L and the supply is represented by a voltage source E_s with internal impedance comprising L_s and R_s. The phase angle ϕ represents the point on the voltage wave where the switch operates.

The analysis of this circuit is facilitated by regarding it as the combination of two circuits. These are a first-order system of E_s, L_s, R_s, L_L and R_L, and a second-order system of E_s, L_s, R_s and C_L. Fig. 3.8 shows this schematically. The current flowing in the complete circuit is the sum of the currents in each sub-circuit.

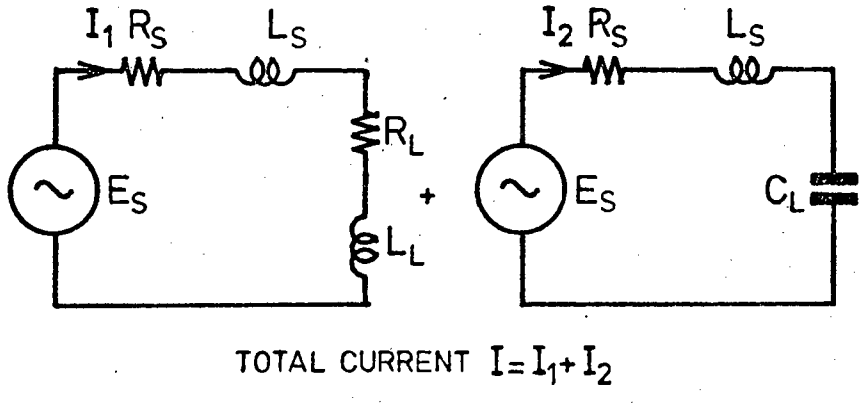


Fig. 3.8. Separating circuit into simpler elements

(Note that this process is only approximately valid when C_L is of such an order of magnitude to make $I_2 \ll I_1$. See App. 6)

The current in the first-order system, i_1, is given by (Appendix 6)

$$i_1 = \exp\left(\frac{R_L}{L_L}t\right)\left\{\frac{-E_{smax}}{\sqrt{(R_L^2 + \omega^2 L_L^2)}}\sin\left(\phi - \tan^{-1}\frac{\omega L_L}{R_L}\right)\right\} + \ldots\ldots$$

$$\ldots\ldots + \frac{E_{smax}}{\sqrt{(R_L^2 + \omega^2 L_L^2)}}\sin\left(\omega t + \phi - \tan^{-1}\frac{\omega L_L}{R_L}\right)\right\} \qquad (3.21)$$

$$L^1 = L_L + L_s \quad \text{and} \quad R^1 = R_L + R_s$$

For the second order system it is assumed that the system is underdamped, that is

$$\left\{\frac{R_s}{2L_s}\right\}^2 < \frac{1}{L_s C_L} \tag{3.22}$$

The solution then is (Appendix 6)

$$i_2 = \left(\frac{E_s \sin\phi}{\theta L_s}\right)(\exp -\alpha t . \sin\theta t) + \frac{E_{smax}}{\sqrt{\{R_s^2 + (\frac{1}{\omega C_L} - \omega L_s)^2\}}} \sin(\omega t + \phi + \tan^{-1}(\ldots$$

$$\ldots \left\{\frac{\frac{1}{\omega C_L} - \omega L_s}{R_s}\right\}$$

where $\theta = \sqrt{\{\frac{1}{L_s C_L} - \frac{R_s^2}{4L_s^2}\}}$ (3.23)

and $\alpha = \frac{R_s}{2L_s}$

The total current that flows at turn-on is then given by

$$i = i_1 + i_2$$

Generally speaking, it may be assumed that the capacity of a typical machine winding is low enough to make the second order system current of such a short duration and low amplitude as to make it of negligible importance during turn-on.

3.5.4.2 CIRCUIT BEHAVIOUR AT TURN-OFF: (22, 24)

The turn-off process occurs over three separate stages. These are

* The initial stage when the transistor current is reduced to zero; the feedback system has not yet operated.
* The stage when the transistor has turned off but the freewheel path has not yet operated. Current flows in whatever circuit element may by-pass the collector-emitter circuit.
* The final stage when the freewheel switch operates.

The feedback system, and thus the freewheel path, cannot operate instantaneously owing to the delays in the turn-on process of the freewheel transistor, which can be as long as 5 μsec. It is also important that the feedback system only operates when the "turning-off" transistor is indeed off; this avoids the condition of a short-circuit across the supply terminals.

The final stage of operation allows whatever energy is stored in the supply load inductance and stray capacitance to be dissipated.

Fig. 3.9 indicates schematically the initial stage of the operation; the diode bridge is omitted

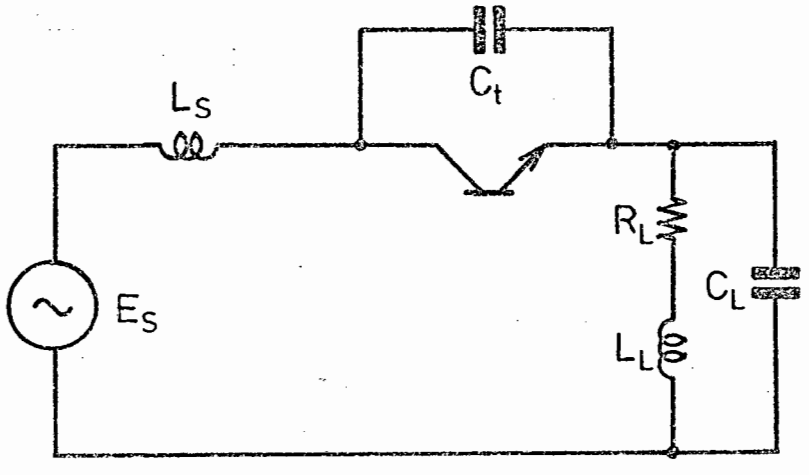


Fig. 3.9. Circuit conditions at commencement of turn-off.

for clarity. The load current is assumed constant; thus only the voltage across the transistor changes as the bypass capacitor C_t is charged. Note that if some form of bypass is not provided then the stray collector-emitter capacity serves in that stead. As is indicated in Appendix 7, the voltage across the transistor during

turn-off is

$$V_{c(t)} = \frac{It^2}{2C_t T} \qquad (3.24)$$

and reaches a maximum

$$V_{cmax} = \frac{IT}{2C_t} \qquad (3.25)$$

at the end of the turn-off period T.

The current into the capacitor then continues constant and the voltage across the transistor rises as a linear function of time,

$$V_c = \frac{It}{C_t} \qquad (3.26)$$

At some point the freewheel switch operates and the circuit is then reduced to that shown in fig. 3.10.

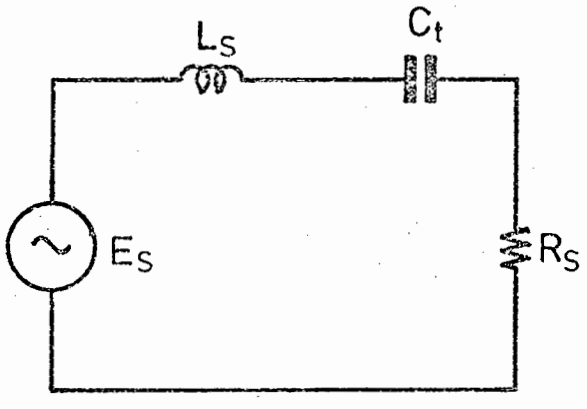


Fig. 3.10. Supply and transistor bypass capacitor at instant of freewheel switch operating

The voltage across the transistor continues to rise;

$$\Delta V_c = I\sqrt{\{\frac{L_s}{C_t}\}} \qquad (3.27)$$

Thereafter the current decays as a typical second-order system. Since R_s is usually very small, the condition for underdamping (equation 3.22) is most likely to prevail, thus the current is given by

$$i_t = \frac{I}{\sin\phi} \exp{-\alpha t}.\sin(\theta t + \phi) \qquad (3.28)$$

where $\alpha = \frac{R_s}{2L_s}$; $\theta = \sqrt{\{\frac{1}{L_s C_t} - \frac{R_s}{4L_s^2}\}}$

and $\tan \phi = \frac{\theta L_s}{V_c + \frac{3IR_s}{2}}$

It is obviously undesirable to turn on the power transistor while the bypass capacitor is fully charged since there is nothing to limit the rise of current. This problem is overcome by including a small value resistor in series with the capacitor with a fast diode in parallel. During turn-off the diode effectively removes the resistor from the circuit, but brings it into operation during turn-on. Maximum current at turn-on is then

$$I_{max} = \frac{V_c}{R_t} + I_L \qquad (3.29)$$

The maximum voltage Vc is that of the supply; that is, E_{smax}.

Instead of the capacitor in parallel with power transistor, it is possible to replace it with a zener diode acting as an energy dissipator. Fig. 3.11

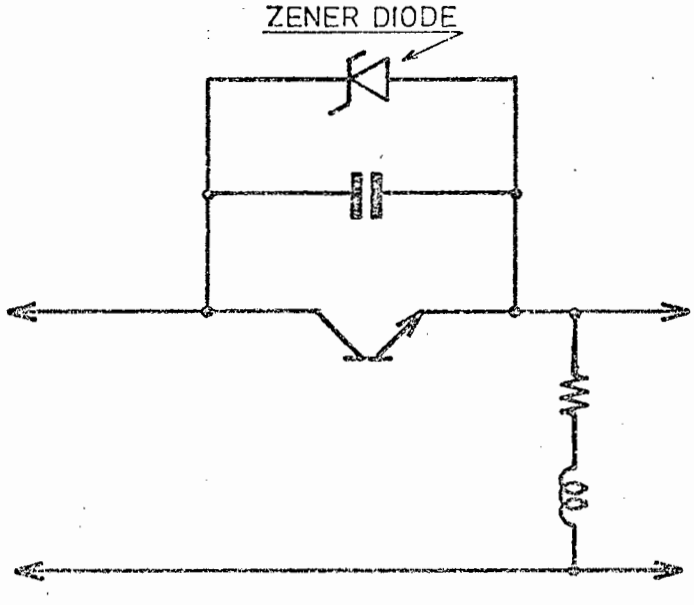


Fig. 3.11. Zener diode snubber

illustrates the arrangement. When the transistor is turned off the current is diverted into the stray capacity; the voltage rise is very fast; the zener diode breaks over and conducts. The voltage across the transistor is then held constant until the free-wheel path comes into operation.

The advantage of the zener diode over the capacitor as a bypass element is that excessive collector-emitter voltages are avoided if the feed-back system should by any chance be delayed in its operation. Equation 3.27 indicates that the voltage across the capacitor rises as a linear function of time, which could rapidly reach an excessive level. The zener voltage remains constant and the only require-ment is that the diode be capable of dissipating the excess energy.

The disadvantage of the zener diode system is that, since the voltage is constant, the danger of second breakdown is enhanced. Fig. 3.12 illustrates the turn-off loci of the two systems. The capacitor bypass has a turn-off locus which can keep well clear of the safe operating limits regardless of switching speed, while the zener diode system pushes to the limits of safe operation.

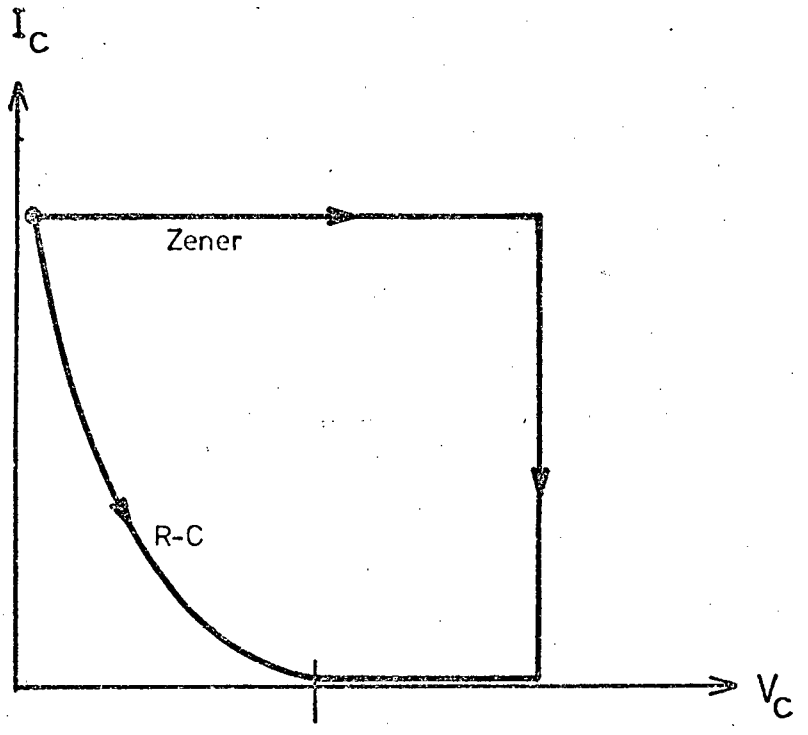


Fig. 3.12. Zener diode vs. R-C turn-off loci

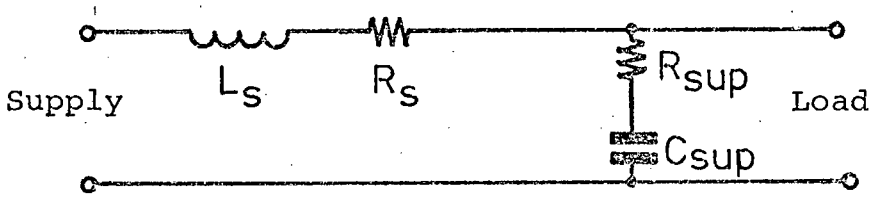


Fig. 3.13. Bypassing the supply

Excessive voltage excursions may occur in the final stages of the switch-off process if the supply inductance is overly large. This may occur when the system is operated from a variable transformer, say for experimental purposes. If the supply is bypassed by a series resistance-capacitance network, as in fig. 3.13, and the values are arranged such that

$$\frac{R^2}{4L_s^2} > \frac{1}{L_s C_{sup}} \qquad (3.30)$$

where $R = R_s + R_{SUP}$

then the system is overdamped and no voltage excursions can occur.

3.6 FEEDBACK CIRCUIT BEHAVIOUR:(24)

The voltage across the load comprises a forced component,

$$V_{Lforced} = I_o Z_L \qquad (3.31)$$

and a natural component during the transient period,

$$V_{Lnat} = -V_c \qquad (3.32)$$

Vc is the voltage appearing across the bypass capacitor.

If one considers the voltage appearing across the freewheel transistor, then the diode bridge ensures a uniform polarity irrespective of the behaviour of the voltage across the load. Thus the requirement of the feedback network is to discriminate between the transient voltage, appearing at commutation, and the "off" condition collector-emitter voltage VCE. The maximum collector-emitter voltage is the peak value of the supply voltage. (In the "off" state).

Noting that the rate of rise of the transient voltage is several orders magnitude larger than that of the supply, two possibilities present themselves. These are

* Absolute value detection by comparing the transient voltage to a preset value which is higher than the peak supply voltage.
* Rate of rise measurement by means of a differentiator circuit, and again comparing this to some preset value.

These possibilities are illustrated in figs. 3.14(a) and (b).

Further feedback circuit operation security is provided by the overall system control which inhibits

feedback operation except during a set "window" during the commutation period.

Note that the time rate of rise of voltage across the transistor depends on the bypass capacitor C_t. Thus

$$\frac{dV_c}{dt} = \frac{It}{C_t T} \qquad (3.33)$$

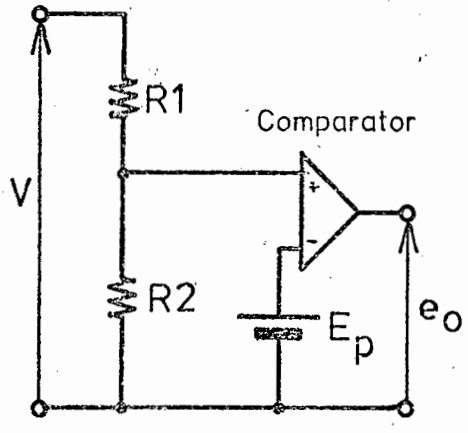


Fig. 3.14.(a) Feedback by absolute value detection

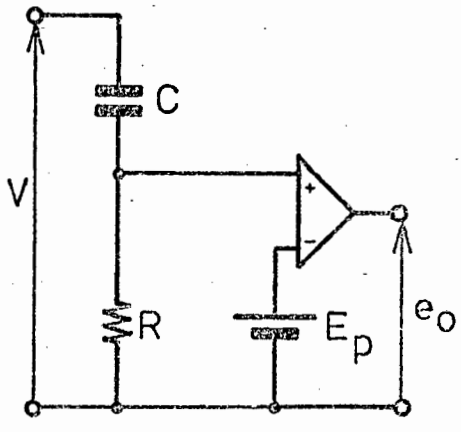


Fig. 3.14.(b) Feedback by rate-of-rise detection

CHAPTER 4

EXPERIMENTAL REALISATION OF THE A-MOD CONVERTER

4.1 INTRODUCTION:

The practical realisation of the converter system outlined in the previous chapters involves two basic elements. These are the power switch and the control circuit. A prototype of the complete system has been constructed with a 6-pulse bridge configuration. Any examination of the 3-pulse mid-point configuration may be obtained by simply using one half of the 6-pulse bridge circuit.

Fig. 4.1 gives a block diagram of the system, for a 3-phase input and single phase bridge output. Since this represents the basic minimum converter the description that follows centres on this system. Three-phase output systems involve the interconnection of a number of single-phase systems.

The block entitled "switch" comprises the power transistor, the diode bridge (to provide bidirectional conduction), the base drive circuit, coupling isolators and a power supply. The "control pulse generator" contains all the logic circuits to operate the switches in the correct sequence at variable frequency, vary the series/shunt conduction ratio and control the feedback circuits.

The protection system provides a means of limiting the current and voltage applied to the power transistors. Since the transistor has no reserve of short-term

NOTE :

The shunt switch performs the function of maintaining load current continuity during the supply "off" period . That is , when one of the series switches is opened , the shunt switch operates , under control of the feedback system , to keep the (inductive) load current constant . When it is neccessary to recouple the load to the supply , the shunt switch opens and the feedback system operates the appropiate series switch .

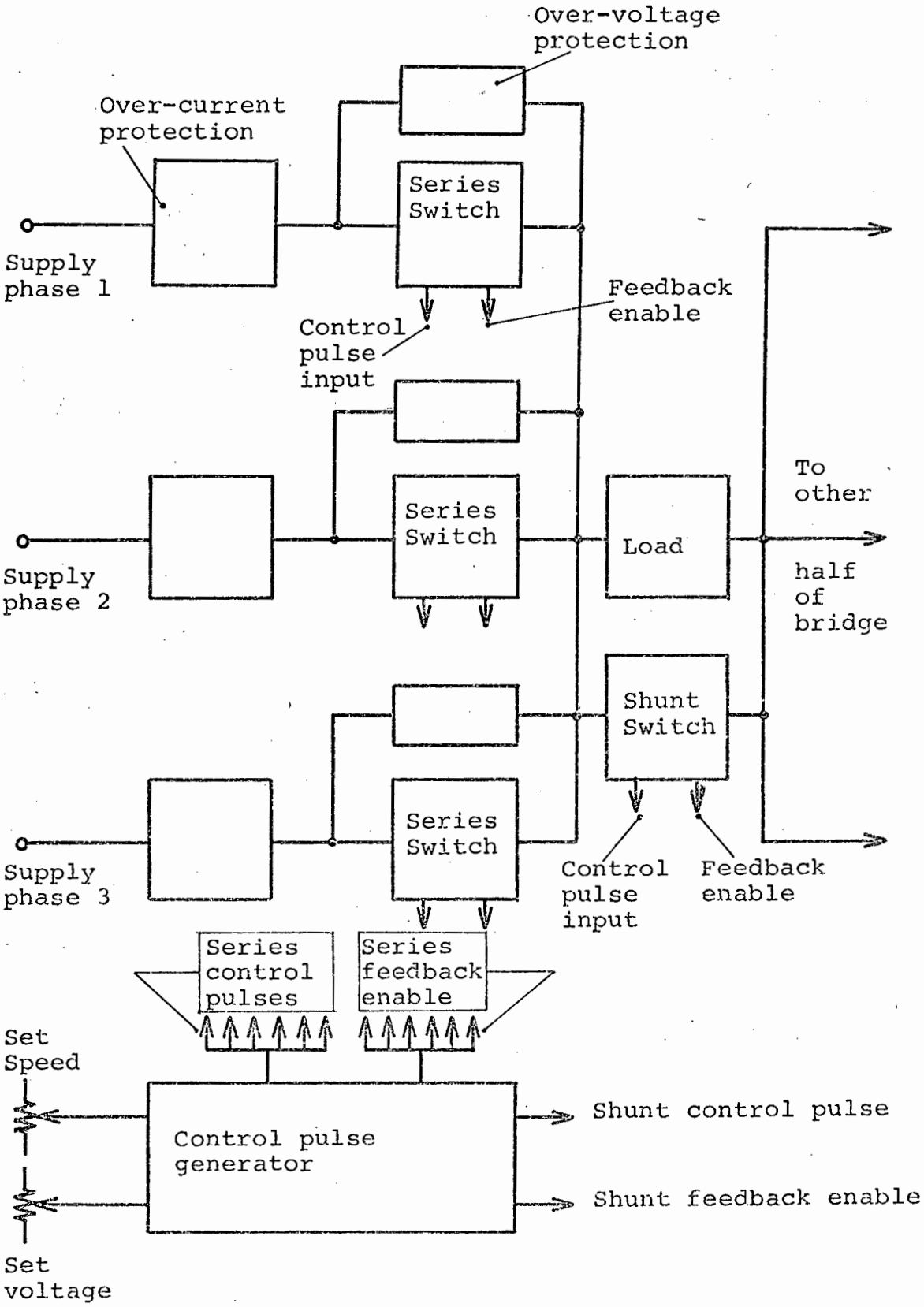


Fig. 4.1. Block diagram of 6-pulse bridge configuration

overload current capacity, and similarly has no self-protect capability on overvoltage, external means are provided to protect the device. These comprise a fast-operating "crowbar" fuse for current limiting, and high-power surge suppressors for voltage protection. The "crowbar" circuit is detailed in Appendix 8.

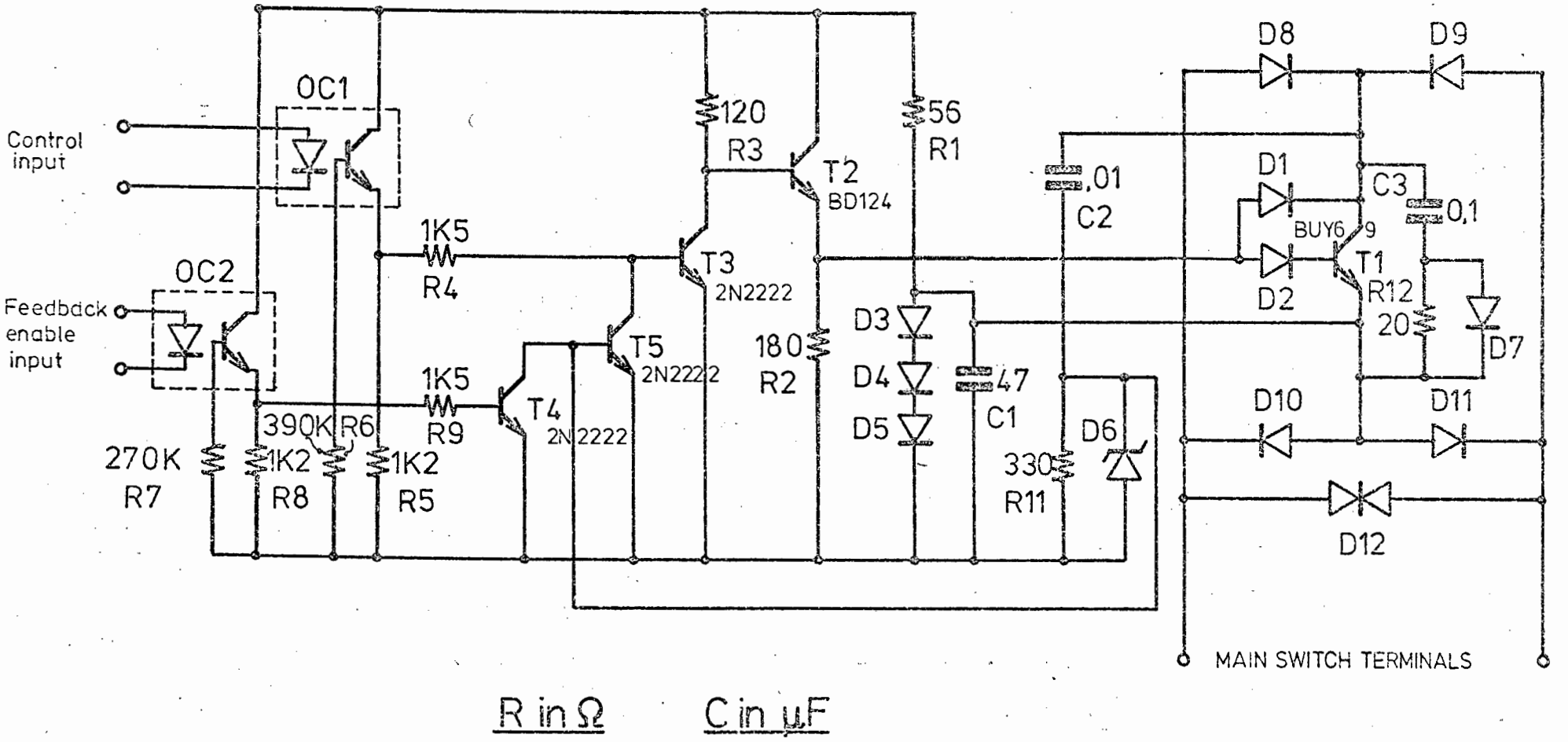
4.2 DESIGN OF THE COMPLETE TRANSISTOR SWITCH:

The circuit associated with the power transistor must meet the following objectives:

* Provide sufficient base current to turn the transistor on, with a fast enough rise time to avoid extending the 3 μsec delay inherent in the power transistor at turn-on.
* Prevent the power transistor from going into saturation.
* Provide a reverse-bias on the base of the power transistor during the "off" period.
* The circuit must be able to operate while floating at supply live-to-neutral potential, i.e. some isolated interface must be provided to the control pulse generator.
* Provide a circuit for the feedback system to operate over.

The complete switch circuit is shown in fig. 4.2, and a detailed component function description is given in Appendix 8, since it is only proposed to outline here the salient features which give effect to the

Fig. 4.2. Circuit of complete power switch



R in Ω C in µF

requirements listed above.

The protection or "snubber" circuit for the power transistor is provided by C3, R12 and D6. The values selected result in the feedback circuit, which depends on time rate of rise of voltage across the power transistor, being operative for load currents greater than 0,3 A. The voltage rise produced by currents below 0,3 A is negligible. Maximum voltage is limited to 300 V by the protection diode which dissipates 30 m Joule on each turn-off operation.

Base drive to power transistor T1 is provided by transistor T2 which is connected in an emitter-follower configuration. The switching times of T2, a type BD124, are an order of magnitude faster than T1, a BUY69B. The diodes D1 and D2 are a Baker clamp anti-saturation circuit which ensure that the base-collector voltage can never be less than the base-emitter voltage.

The reverse bias to the base is provided by means of R1 and diodes D3, D4 and D5, which make a 2,1 volt positive bias to the emitter which is in effect a reverse bias on the base.

Opto-couplers OC1 and OC2 isolate the switch circuit from the system control logic. The main control is through OC1 while OC2 controls the feedback circuit. Both of these devices are of the photo-transistor-light emitting diode type, which are much slower than the photodiode type. However, the output of the phototransistor optocoupler is much greater, and thus the loss of speed was felt to be more than offset by the simplification of the subsequent circuit.

Typical rise (and fall) times are 2 μsec, which when added to the 3 μsec delay of the power transistor, makes an overall system turn-on delay of 5 μsecs, mentioned earlier. Full specifications of this device are in Appendix 5 .

The feedback circuit, which in this instance is of the type which detects the rate of rise of voltage across the switch, is made up of capacitor C2 and resistor R11, operating into transistor T5. Transistor T4 inhibits feedback action when it is not required.

Bidirectional conduction is provided by diodes D7, D8, D9 and D10. These are 600 V 12 A (av.) devices with a 200 nsec turn-off, thus having a marginal effect on the overall performance of the switch. Heatsinking is provided by means of 50 mm of the same extrusion used for the power transistor and designed by the same approach.

4.3 THE CONTROL PULSE GENERATOR:

The control pulse generator is required to fulfill the following functions:

* Operate the transistor switches in an ordered sequence as in fig. 2.3.
* Ensure that the feedback circuit comes into operation at the correct point in the operating cycle.
* Provide a means, if necessary, to make closed loop speed control of the load motor possible.
* Vary the duration of the control pulses in

order to provide voltage variation, as set out in section 2.1.

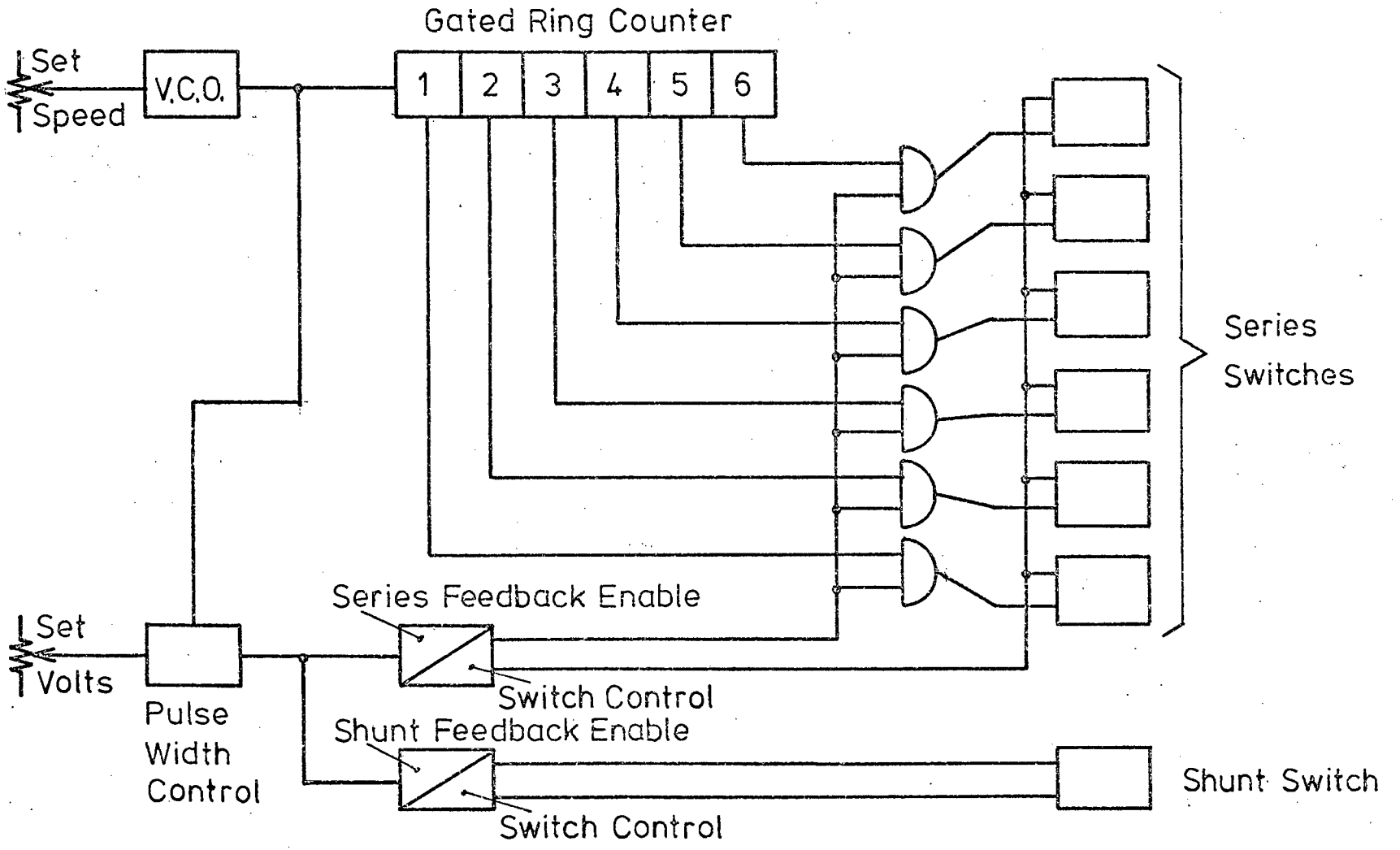
A functional block diagram, using positive AND-OR logic, is shown in fig. 4.3. Power switches for only one phase are shown.

The implementation of this simple sequence, shown in fig. 4.3, requires that a voltage-controlled oscillator (V.C.O.) drives a 6-stage ring counter, with outputs gated to provide 120° phase displaced signals. The output of the V.C.O. also drives the pulse width controller which varies the control ratio (section 2.2.1) under the control of an external voltage. Design details of these units are to be found in Appendix 8, while all the relevant waveforms are shown in fig. 4.4.

The feedback enable circuits, which comprise a composite unit for both shunt and series control, are critical to the operation of the switching system, and are unique to it. Accordingly a more detailed examination is presented here. Fig. 4.5 shows the waveforms produced by this unit in relation to the V.C.O., and fig. 4.6 gives a complete circuit diagram.

The truth table for the feedback enable circuits is as follows:

Fig. 4.3. Block diagram of control pulse generator



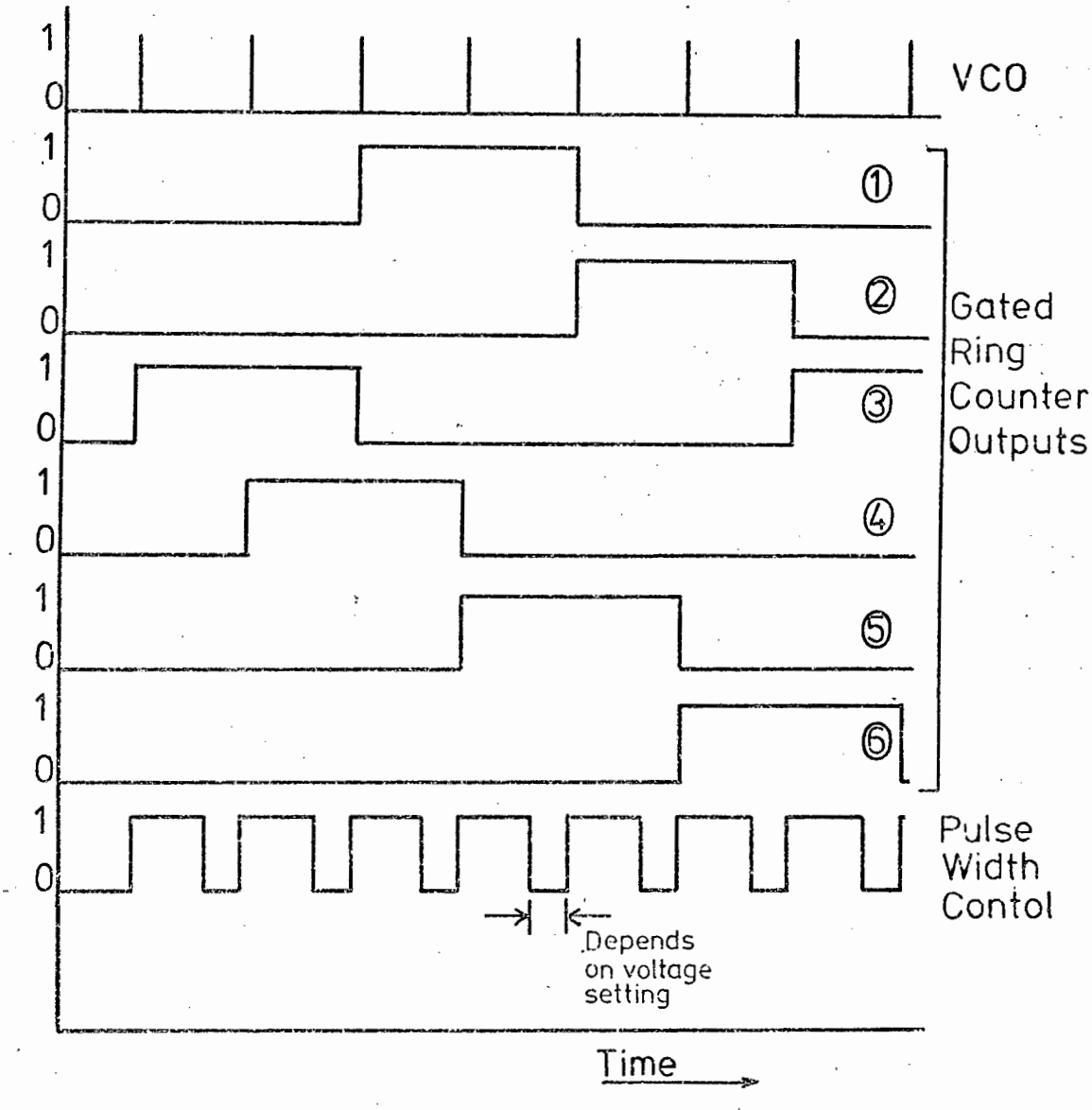


Fig. 4.4. Control pulse generator waveforms

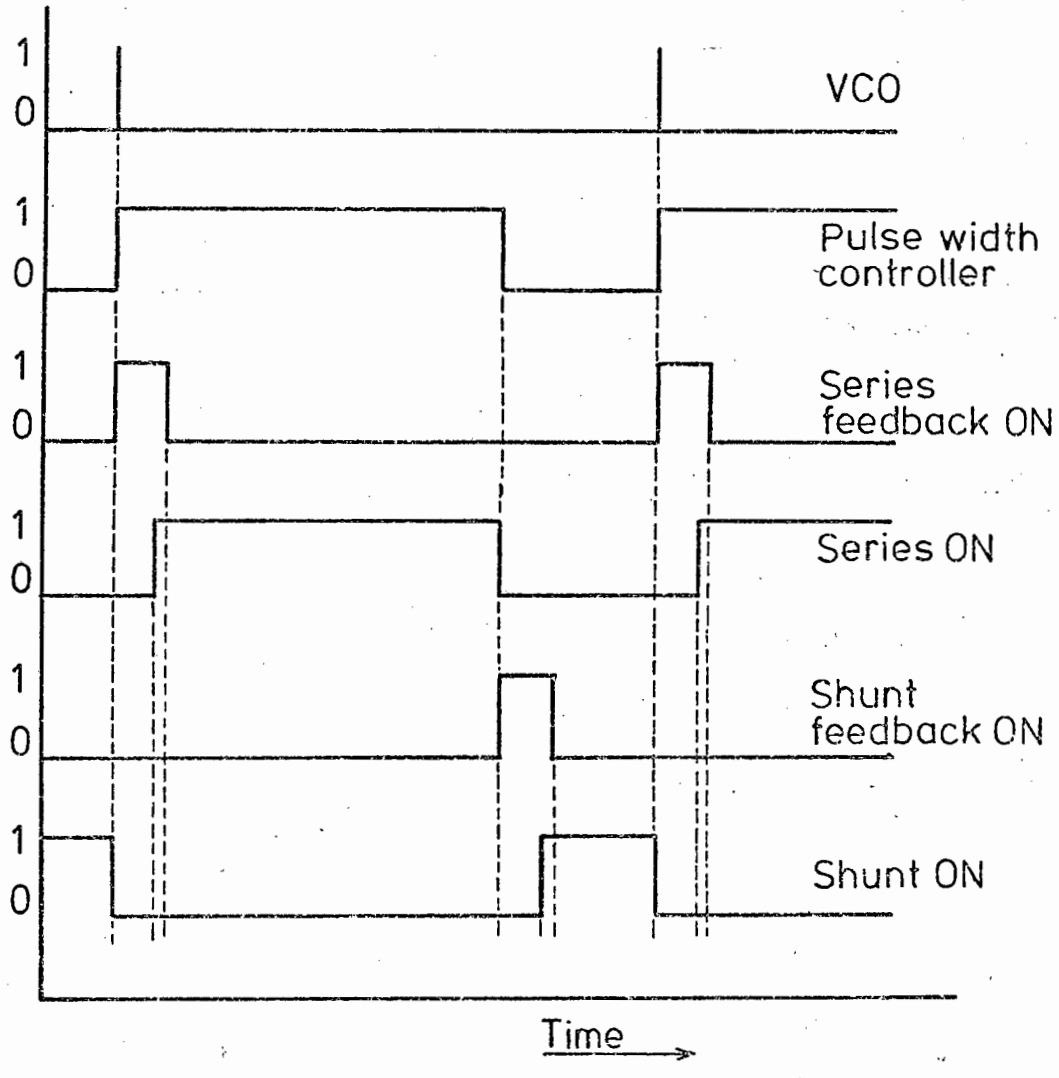


Fig. 4.5. Feedback enable waveforms

Unit / Time	Gated Ring Counter	Pulse width controller	Series switch control	Shunt feedback enable	Shunt switch control	Series feedback enable	Series switch	Shunt switch
t_o	1	1	0	0	0	1	1	0
t_1	1	1	1	0	0	0	1	0
t_2	1	0	0	1	0	0	0	1
t_3	1	0	0	0	1	0	0	1

t_o : Start of sequence; series feedback operates

t_1 : End of series feedback period; series switch control operates

t_2 : Series switch off; shunt feedback on (Voltage control mode)

t_3 : Shunt feedback off; shunt switch control on.

The above process is repeated, t_o through to t_3, when 6-pulse bridge operation is required.

Referring to fig. 4.6, positive-going pulses from the pulse width controller trigger monostable multivibrator MS1. The $\bar{Q}$ output of MS1 is applied to 2-input NAND gate N1 together with the $\bar{Q}$ output of MS2. The output of N1 then goes low, and this activates the series switch feedback circuits through inverter-drivers D1 to D6. The high pulse from the PWC is also applied to the D input of bistable DF1, and, through inverter I, to the D input of DF2. DF1 remains unchanged as the clock input is still low, while the $\bar{Q}$ output of DF2 goes high, which switches off the shunt switch through inverter-driver D8 . Monostable MS1 remains high for a period of 50 μsec maximum, which is the commutation period. When MS1 goes low, the $\bar{Q}$ output triggers MS2 which extends the duration of the feedback circuit operation for a further 10 μsec maximum, in order to allow for the turn-on delay in the power switch. The bistable DF1 clock input goes high when MS1 goes low, through NAND gate N2, and the high pulse from the PWC is then entered into DF1 which enables the gated ring counter outputs to operate the appropriate series switch. The $\bar{Q}$ output of MS2 is also applied to NAND gate N4, preventing any operation of the shunt switch during this period.

When the PWC signal goes low, monostable MS2 is triggered, the D input of DF1 is removed and a high is applied to the D input of DF2. A similar process to that described previously is then followed, with MS4 providing the additional pulse to compensate for turn-on delay.

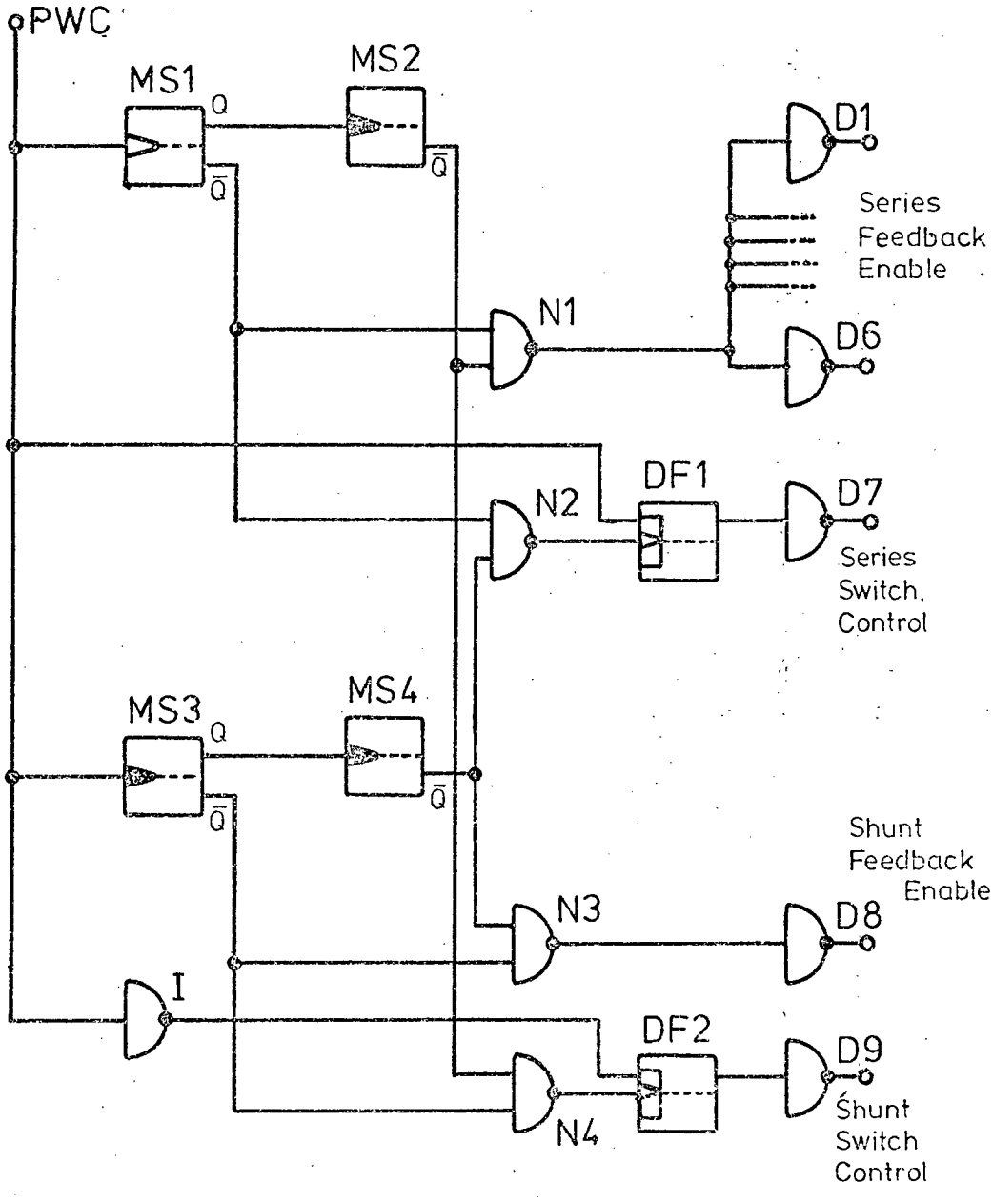


Fig. 4.6. Feedback enable unit ; circuit diagram

The sum of the commutation and turn-on times means that there is always a gap between steps of the series switches. That is, if one refers to fig. 2.1, the wiper of the switch goes into a dead time between contacts. The monostable multivibrators MS1 and MS3 were set to a pulse duration of 25 μsecs and MS2 and MS4 were set to 5 μsecs, which gave a total duration of 30 μsecs. Since the changeover from one series switch to another involves turning off the first switch, with attendant 30 μsecs delay, and then turning on the next, which also produces a 30 μsecs delay, the total gap between switches is then 60 μsecs. This imposes a maximum limit to the on-off ratio, i.e. a "full-on" condition cannot be achieved. The maximum on-off ratio at 50 Hz output, was set at 4,5 : 1.

The frequency range of the voltage-controlled oscillator is in fact wide enough to investigate the possibilities of "slow" sampling or sampling at a rate $(w_i - w_o)$. (See Appendix 1.)

CHAPTER 5

RESULTS OBTAINED FROM THE EXPERIMENTAL MODEL

5.1 Test methods and equipment:

Test results were obtained using standard laboratory test instruments, as indicated in Fig. 5.1, which shows a typical configuration for measuring the output waveform, both for waveshape and spectral content. Current waveforms were evaluated using Hall-effect transducers to provide isolation.

5.2 Test results; waveforms:

Figures 5.2 to 5.13 illustrate typical waveforms obtained from the transient recorder. Comment follows in numerical sequence:

Fig. 5.2: Output waveform from a 3-pulse system with V.C.O. set at 600 Hz and pulse width varied. The zero line is added in.

Fig. 5.3: Output waveform from a 3-pulse system with V.C.O. at 480 Hz and pulse width varied.

Fig. 5.4: Output waveform from a 3-pulse system with V.C.O. at 360 Hz and pulse width varied.

These three figures illustrate the fabrication of the output voltage waveform from the 3 supply phases and how the mean output voltage is varied by pulse width control.

Fig. 5.5: Figs. 5.5(a) and 5.5(b) show, on an expanded scale, the output voltage with the V.C.O. at 600 Hz and 480 Hz respectively and pulse width ratio of 0,8. The voltage spikes required by

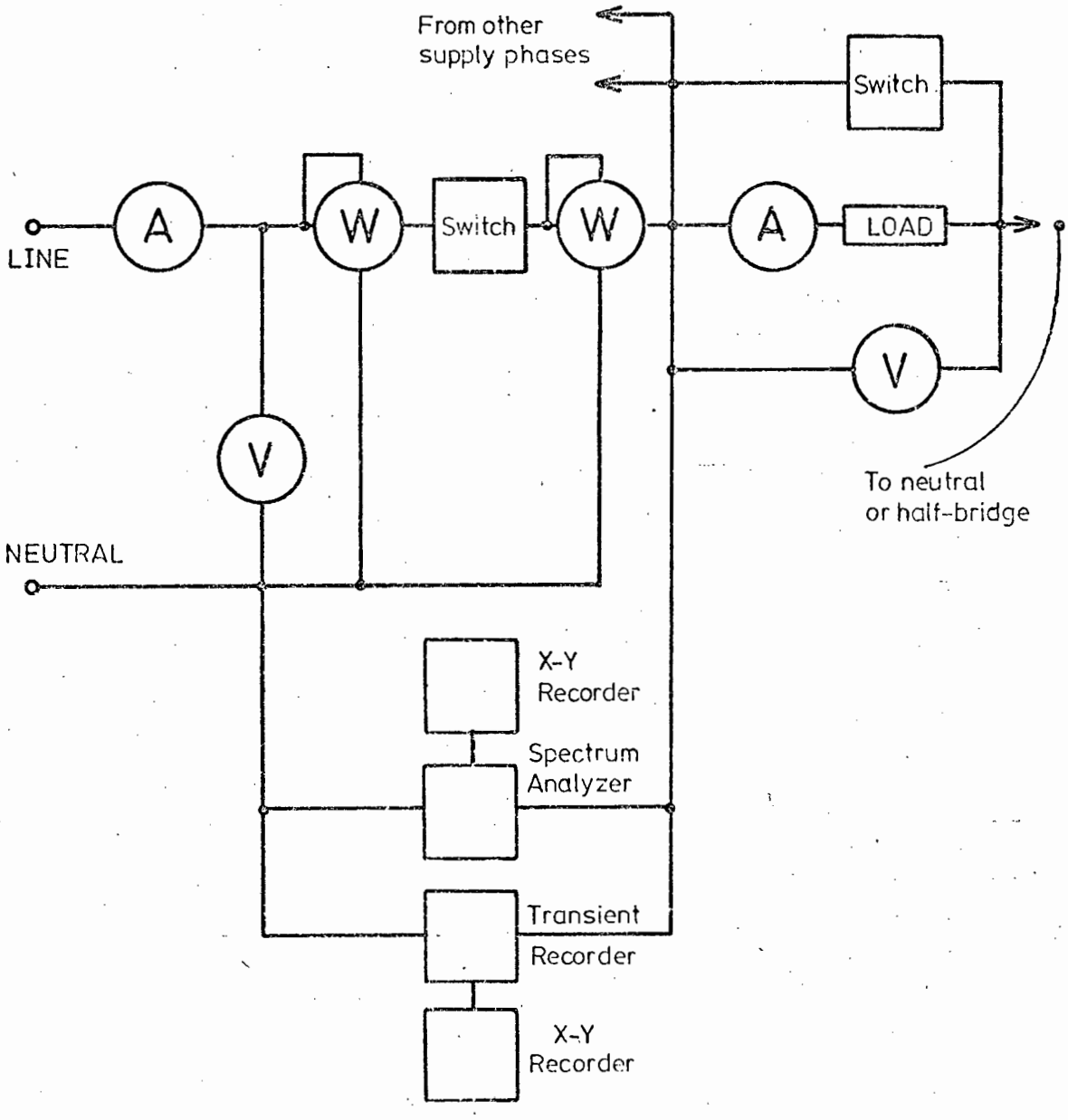


Fig. 5.1. Testing the system. The ammeter and wattmeter elements were replaced with Hall-effect transducers in order to obtain permanent records via the transient recorder - X-Y recorder .

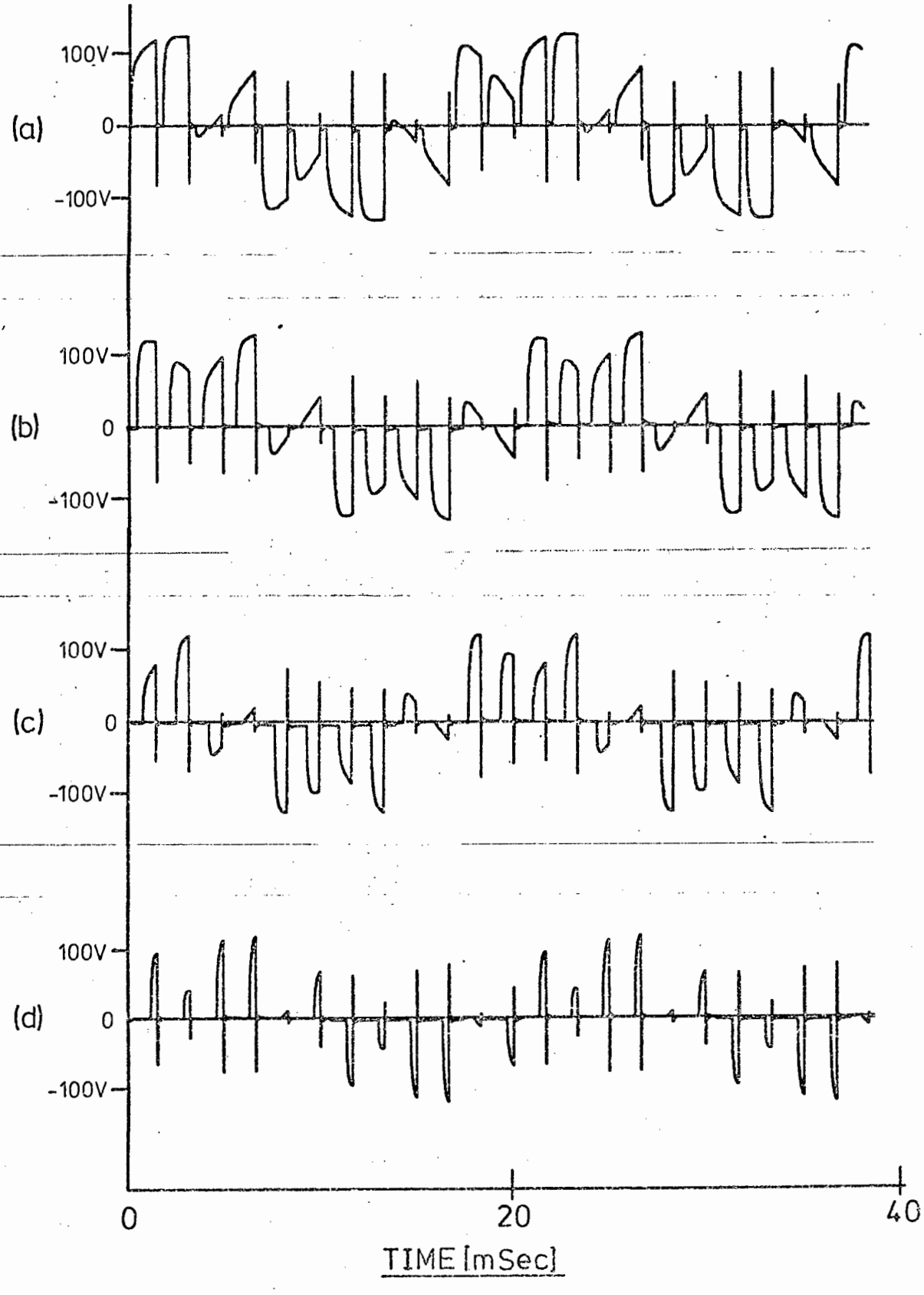


Fig. 5.2. Output waveform ; f_o = 50 Hz. (a) : r=0,8 (c) : r=0,4
(b) : r=0,6 (d) : r=0,2

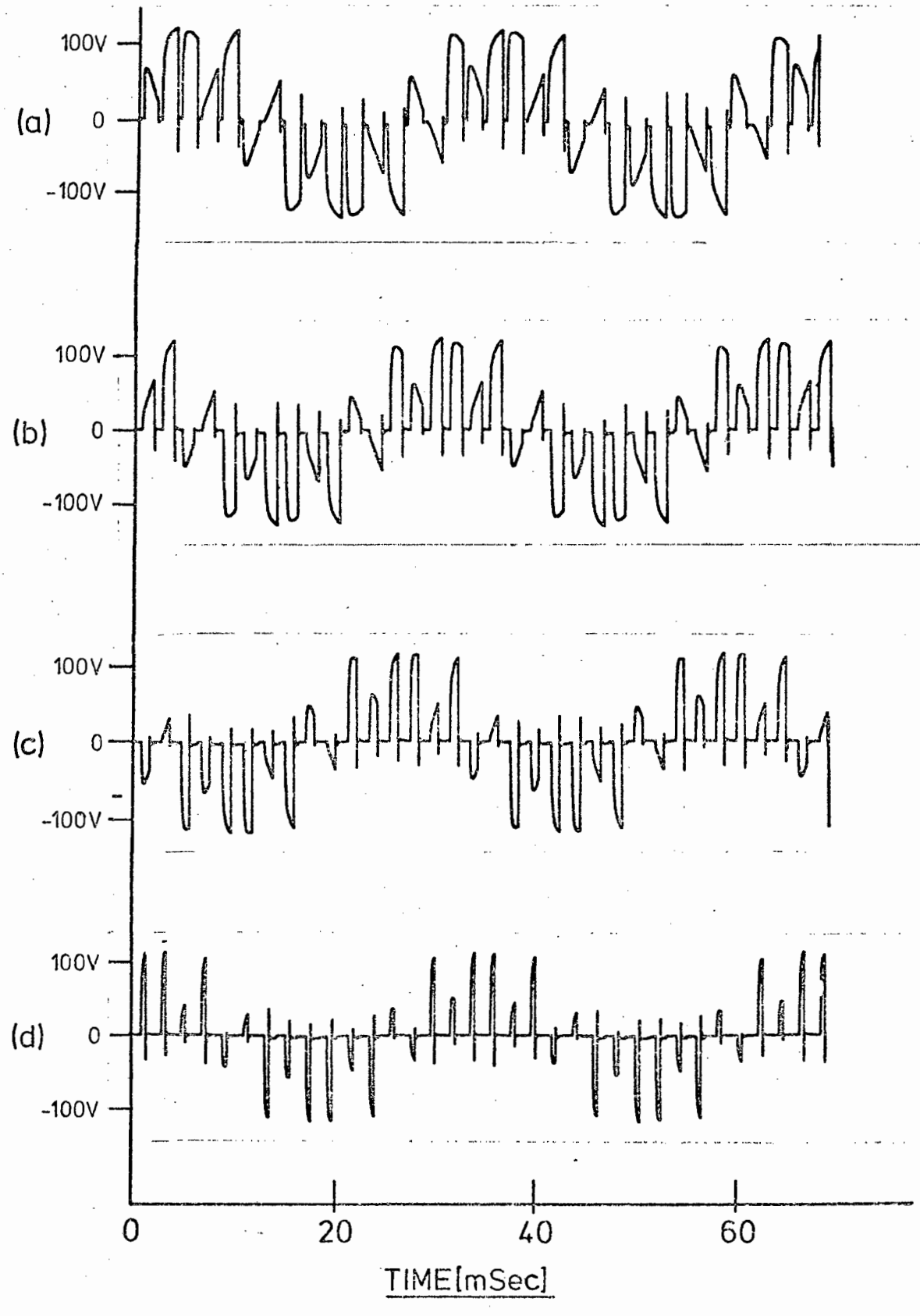


Fig. 5.3. Output waveform ; f_o= 30 Hz . (a) : r=0,8 , (b):r=0,6
(c) : r=0,4 , (d):r=0,2

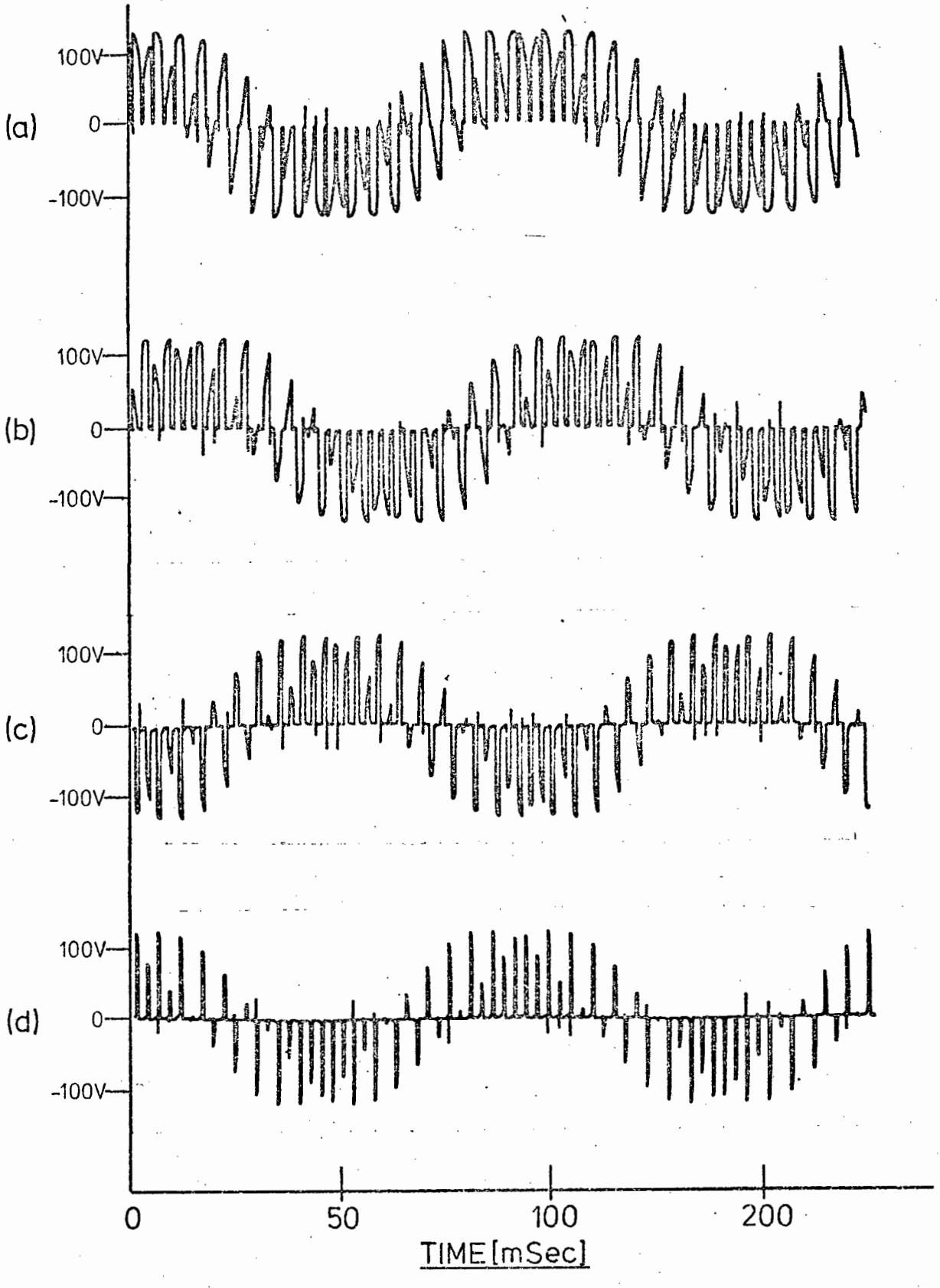


Fig. 5.4. Output waveform ; f_o = 10 Hz .(a):r=0,8 (b):r=0,6 (c):r=0,4 (d);r=0,2

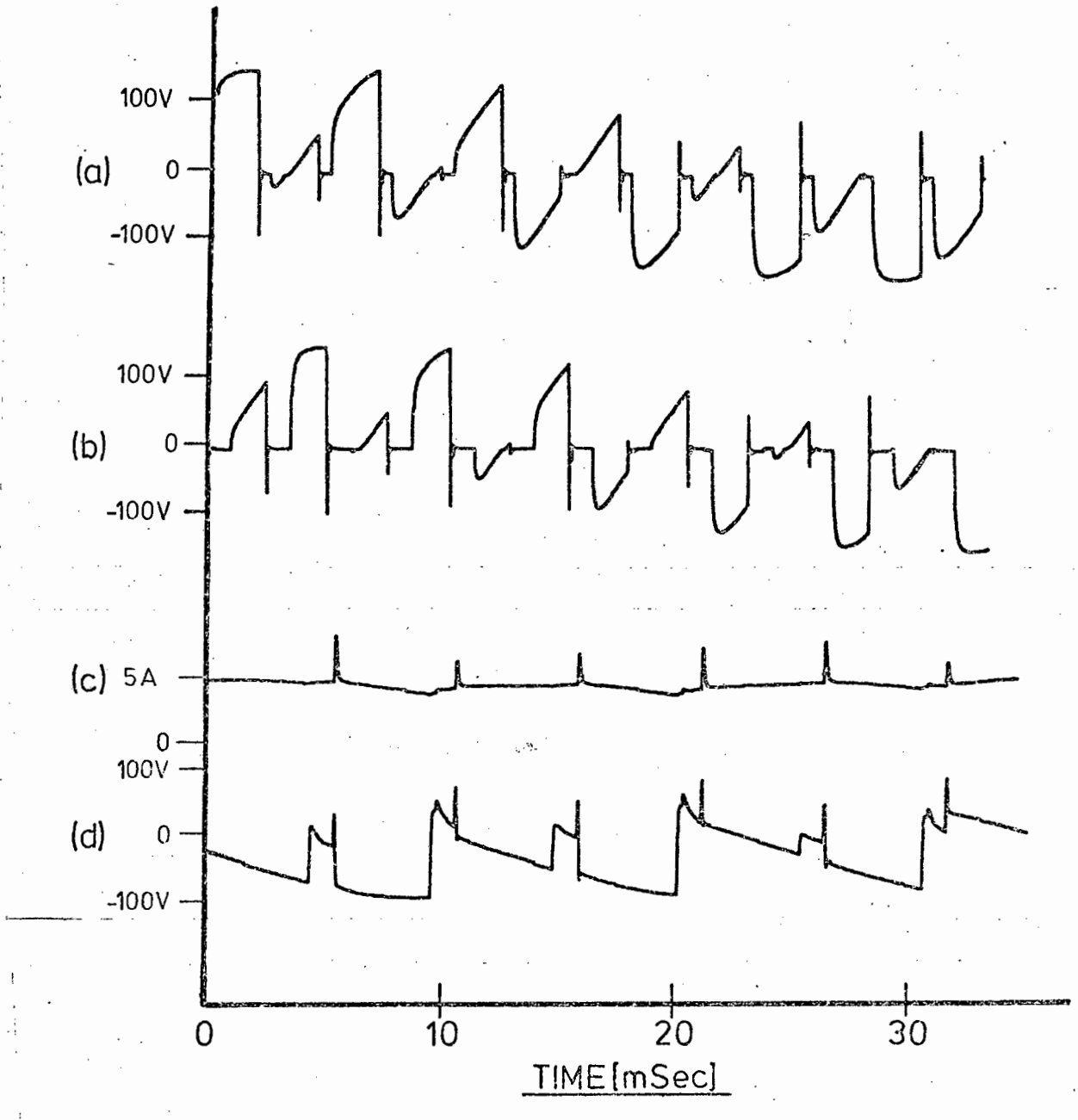


Fig. 5.5. Output waveform ; (a): Voltage , expanded time scale , f_o=50Hz , r=0,8

(b): Voltage , expanded time scale , f_o=30Hz , r=0,8

(c): Load current , inductive load

(d): Output voltage , inductive load

the feedback commutation system appear clearly at turn-off points. Figs. 5.5(c) and (d) show load current and output voltage respectively for a 3-pulse system into an inductive ($\frac{L}{R}$ = 0,014) load and here the output voltage waveform illustrates the commutation problem mentioned in para. 3.4, where the load possesses a "back-e.m.f.".

Fig. 5.6: Figs. 5.6(a), 5.6(b) and 5.6(c) show output voltage, current at the junction of the 3 switches and load current, respectively, for a 3-pulse system operating into an inductive load and illustrate the correctness of the assumption that the load current is sinusoidal.

Fig. 5.7: Figs. 5.7(a) and 5.7(b) show, respectively, output voltage and input power, the latter obtained by means of a Hall-effect transducer in one input supply phase. The V.C.O. was set at 600 Hz, that is, an output frequency of 50 Hz, which enabled a transformer supplying a 50 Hz signal to be connected in series with the load. This results in an output as in Fig. 5.7(c) and an input power in one supply phase as per Fig. 5.7(d). The regeneration capability of the system is clearly illustrated here.

Fig. 5.8: The output voltage was separated into positive and negative banks by means of diodes in the supply phases, to produce the waveforms of Fig. 5.8(b) and (c), while Fig. 5.8(a) shows the total output. This is to illustrate the avoidance of the bank selection problem which

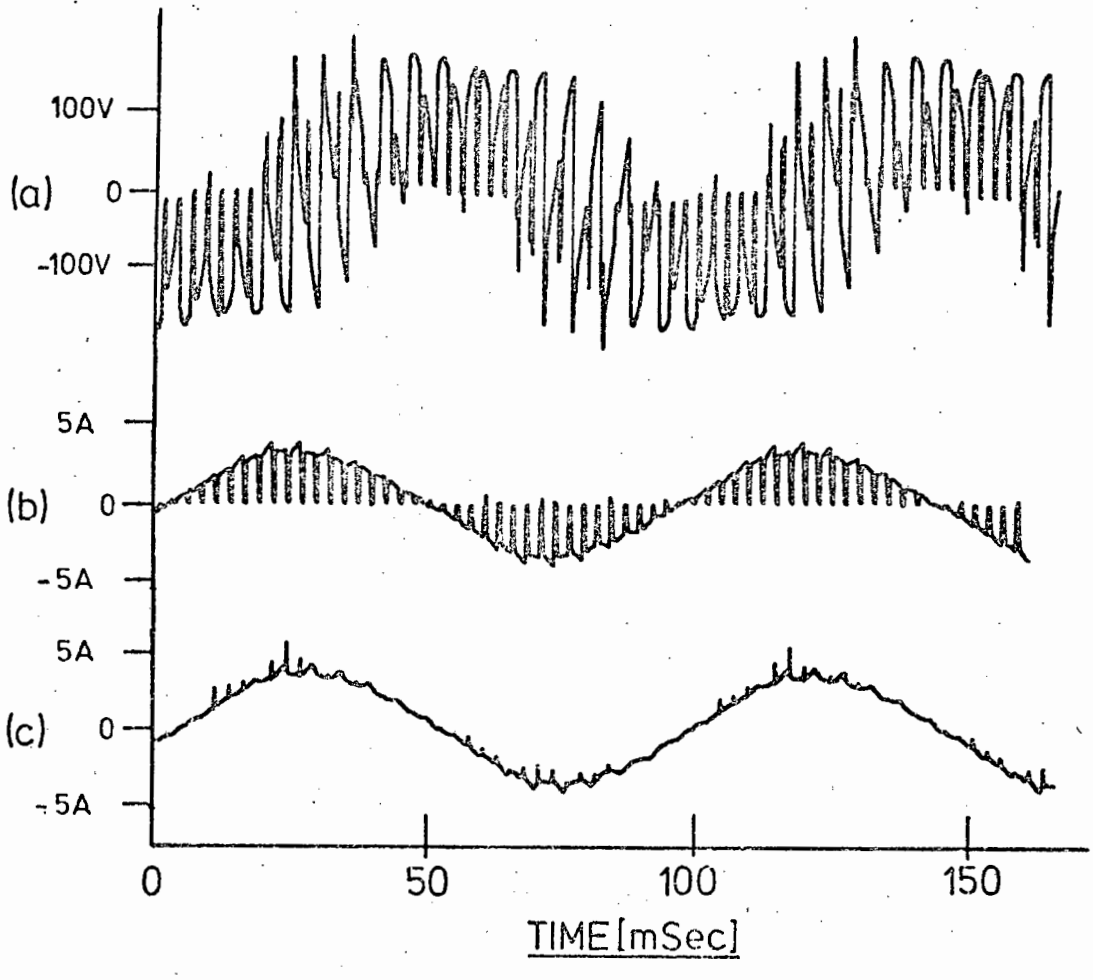


Fig. 5.6. (a) Output voltage , inductive load
(b) Switch current , " "
(c) Load current , " "

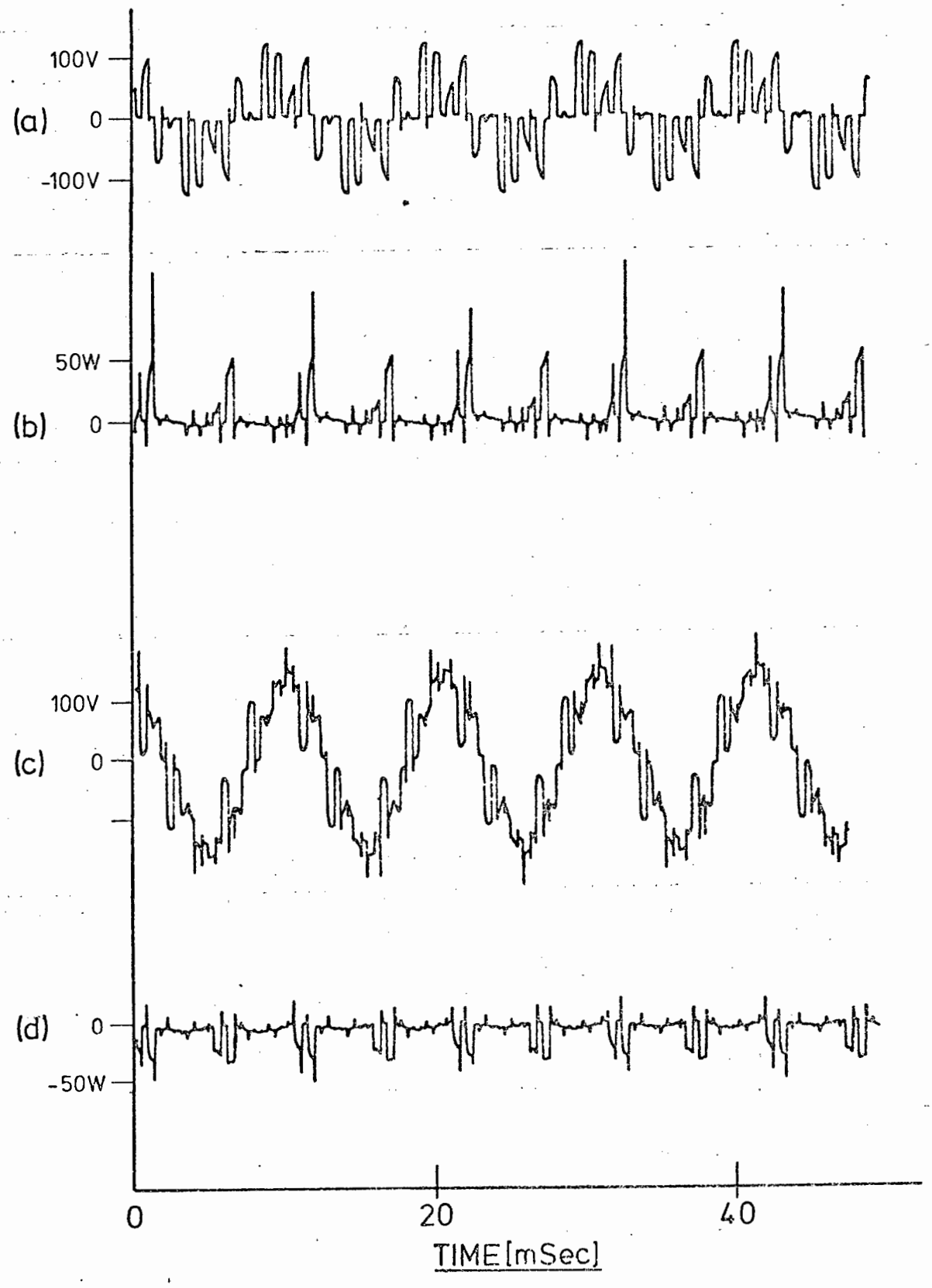


Fig. 5.7. Power in the system

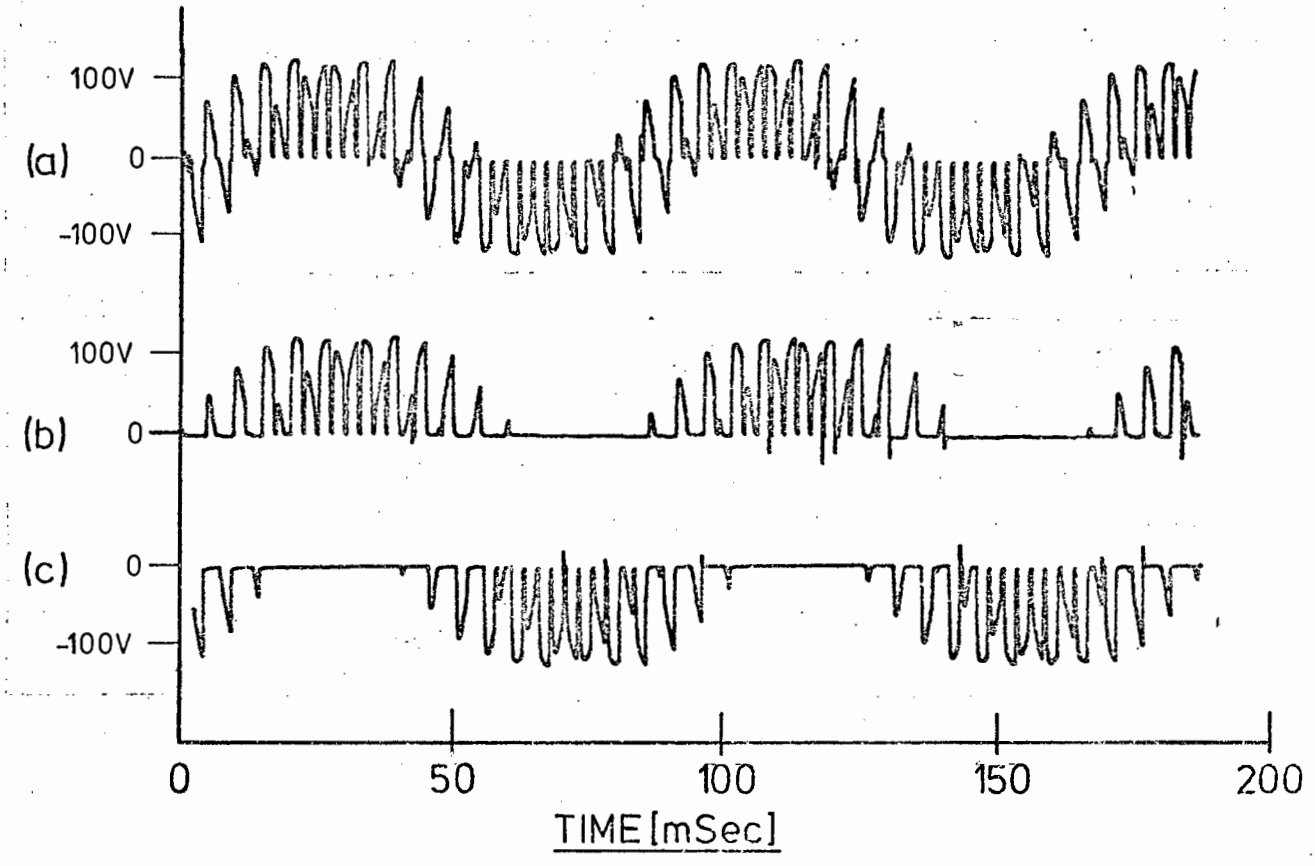


Fig. 5.8. Solving the bank selection problem

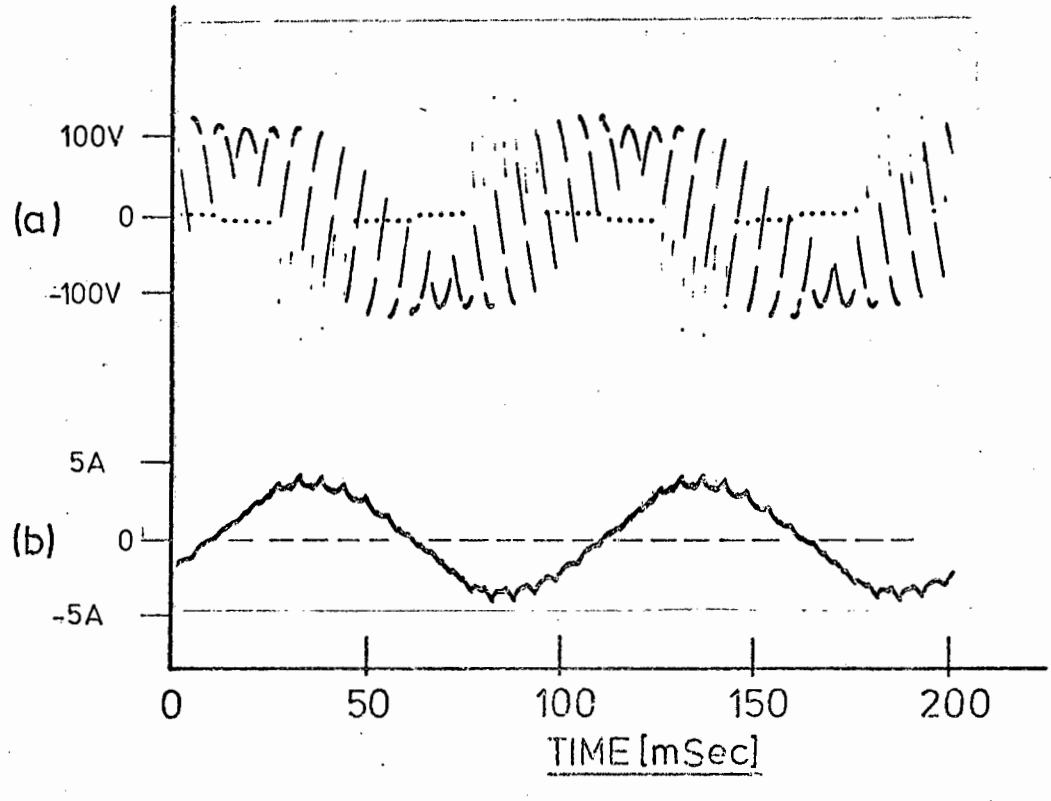


Fig. 5.9. Photographic record ; (a) : Output voltage
(b) : Load current

bedevils the naturally-commutated cycloconverter.

Fig. 5.9: These two waveforms of output voltage and current were obtained by means of a camera and an oscilloscope and are included merely for completeness.

Fig. 5.10: Figs. 5.10(a) and 5.10(b) show, respectively, input current in one supply phase and supply phase-to-neutral voltage for a 6-pulse system, and illustrate graphically the elimination of the fundamental component of output current in the input current.

Figs. 5.11 and 5.12: These two should be considered together, being input current in one supply phase and input voltage for resistive and inductive loads respectively. Note the phase advance of the current discernable in Fig. 5.12. This was confirmed by a standard power factor meter indicating a leading power factor (on an inductive load).

Fig. 5.13: Figs. 5.13(a), (b), (c) and (d) are, respectively, output voltage, and load current for resistive-inductive and inductive loads, driven by a 6-pulse system with V.C.O. at 480 Hz and pulse width ratio of 0,9. These illustrate again the sinusoidal form of the output current.

5.3 Test results; spectographs:

Figures 5.14 to 5.17 illustrate typical results obtained from the spectrograph. Comment follows in numerical sequence:

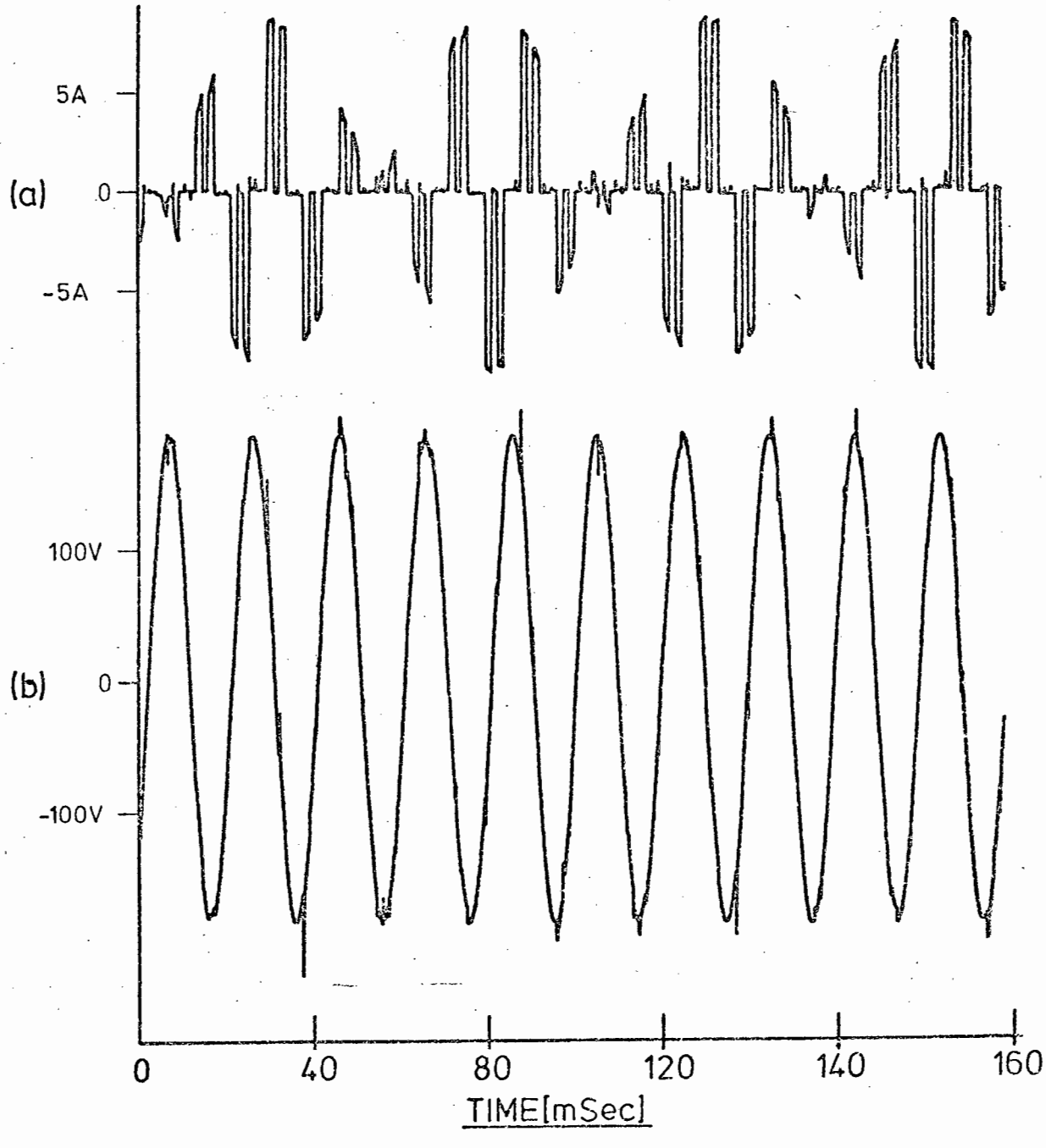


Fig. 5.10. 6-Pulse system ; (a) : Input current
(b) : Load current

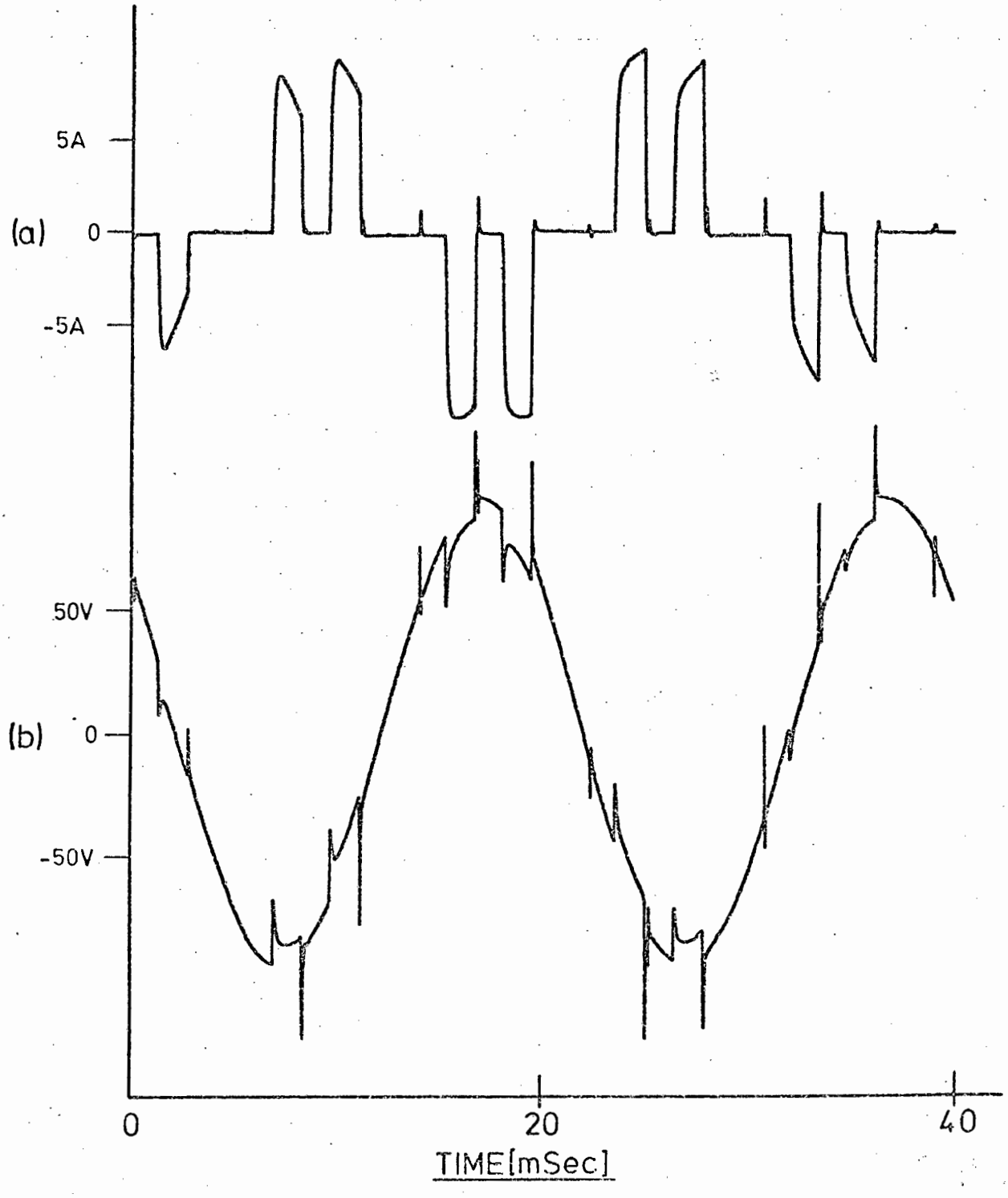


Fig. 5.11. Resistive load ; (a) Input current
(b) Supply voltage

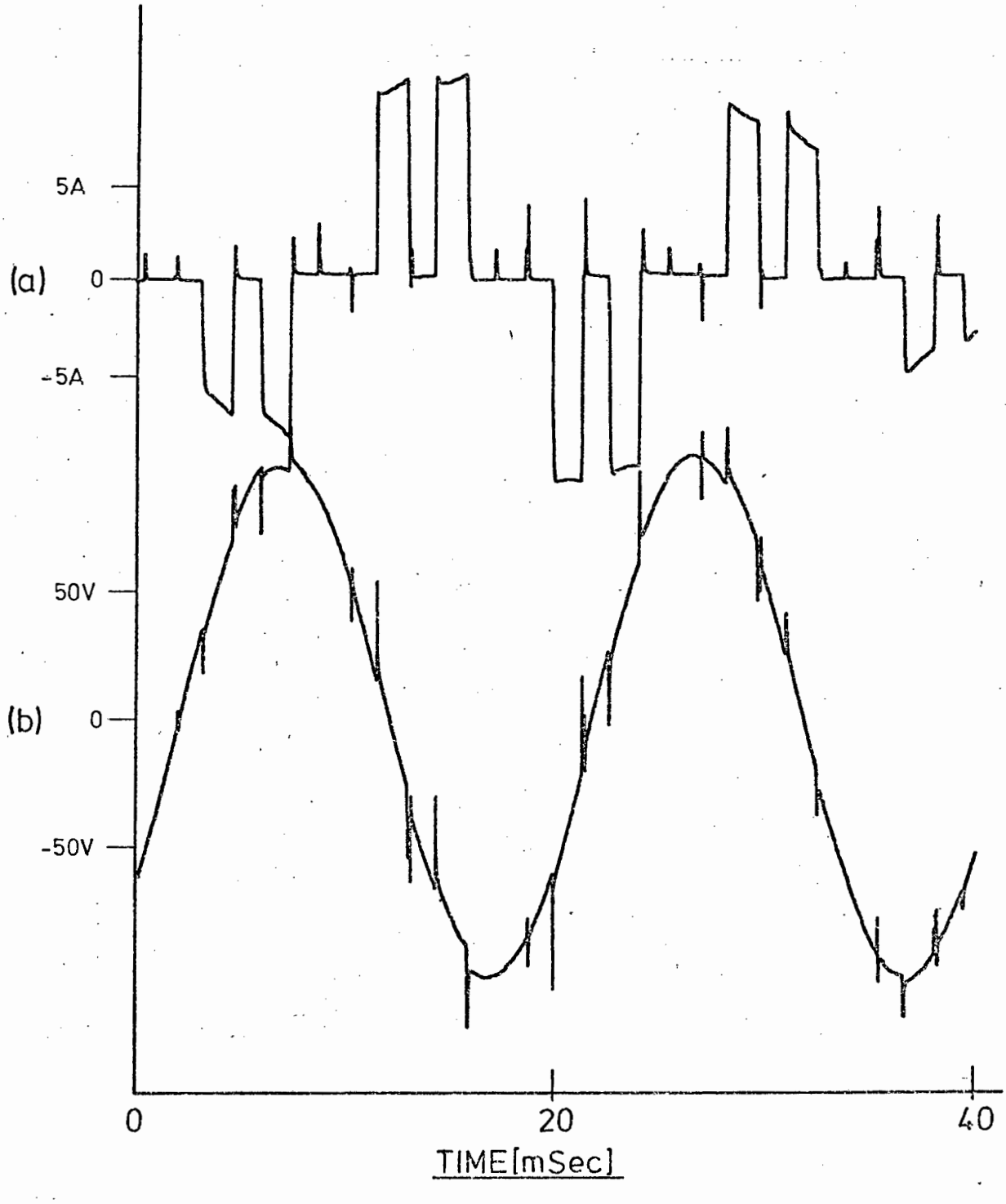


Fig. 5.12. Inductive load ; (a) Input current
(b) Supply voltage

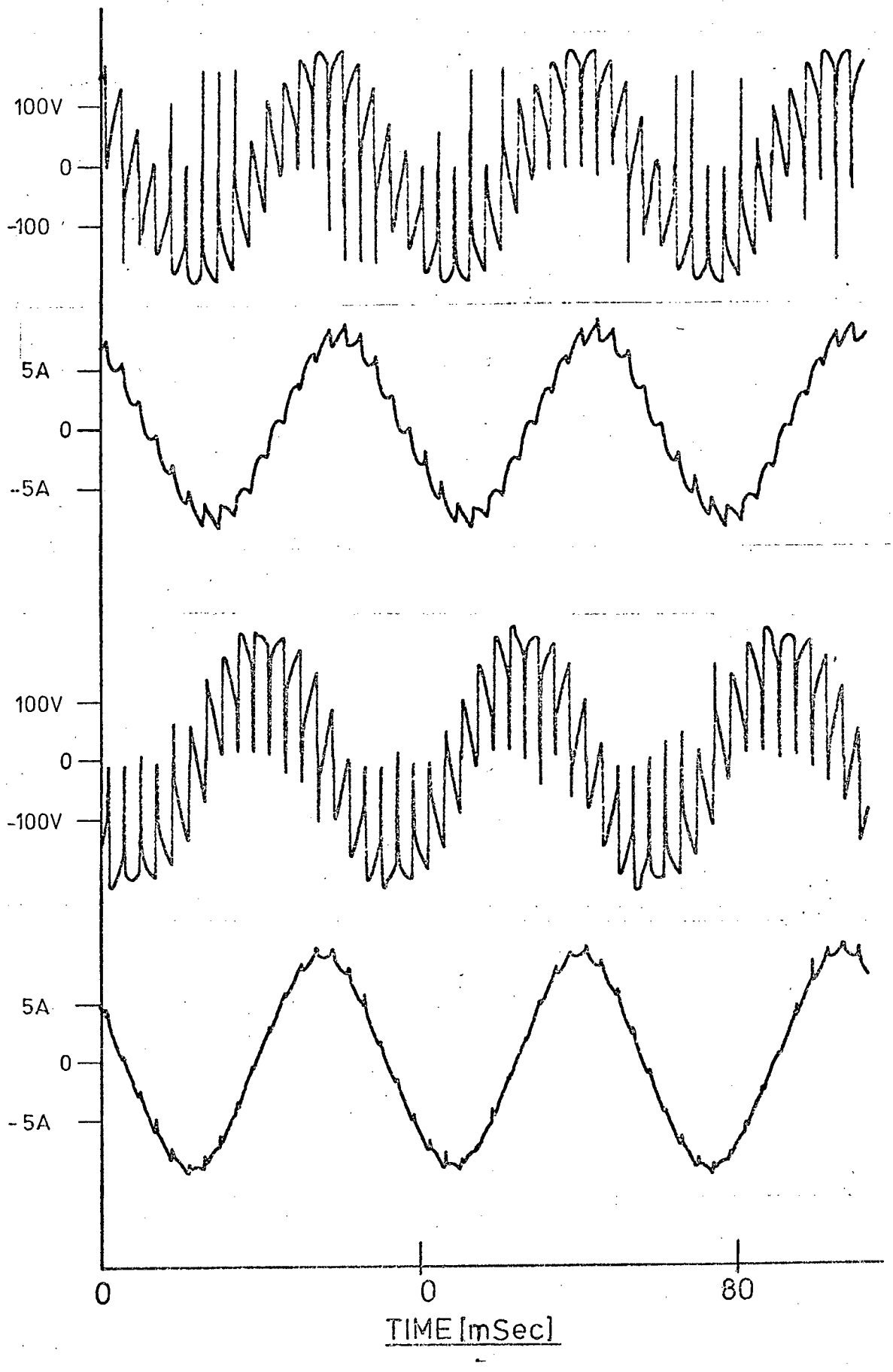


Fig. 5.13. 6-Pulse system ; f_o = 30 ; r = 0,9

Fig. 5.14: Spectra of output voltage of 3-pulse system for V.C.O. frequency of 600 Hz and voltage control ratio of 0,8 for Fig. 5.14(a); voltage control ratio of 0,2 for Fig. 5.14(b). Note that, unlike the naturally-commutated cycloconverter, the frequency of the harmonics does not change with output voltage.

Fig. 5.15: Spectra of output voltage of 6-pulse system. The V.C.O. frequency for Fig. 5.15(a) and Fig. 5.15(b) is 600 Hz and 360 Hz for Figs. 5.15(c) and 5.15(d). The voltage control ratios are 0,8 for Fig. 5.15(a) and Fig. 5.15(c), and 0,2 for Figs. 5.15(b) and (d).

Fig. 5.16: Spectra of input current per phase with single phase output, inductive load, with voltage control ratio of 0,8 for Fig. 5.16(a) and 0,2 for Fig. 5.16(b). Note the preponderance of harmonics at low voltage control ratios.

Fig. 5.17: Spectra of input current, V.C.O. frequency 600 Hz and voltage control ratios of 0,8 and 0,2 for Figs. 5.17(a) and 5.17(b) respectively, with resistive load. This represents an unusual case of non-sinusoidal output current, but is included to show the generation of harmonic pairs as predicted in Chapter 2.

5.4 Test results; general:

Figure 5.18 shows the relative amplitude of the harmonics present in the output of a 6-pulse system driving an inductive load; this should be compared with Fig. 2.7(b) which gives results calculated from the analytical expression

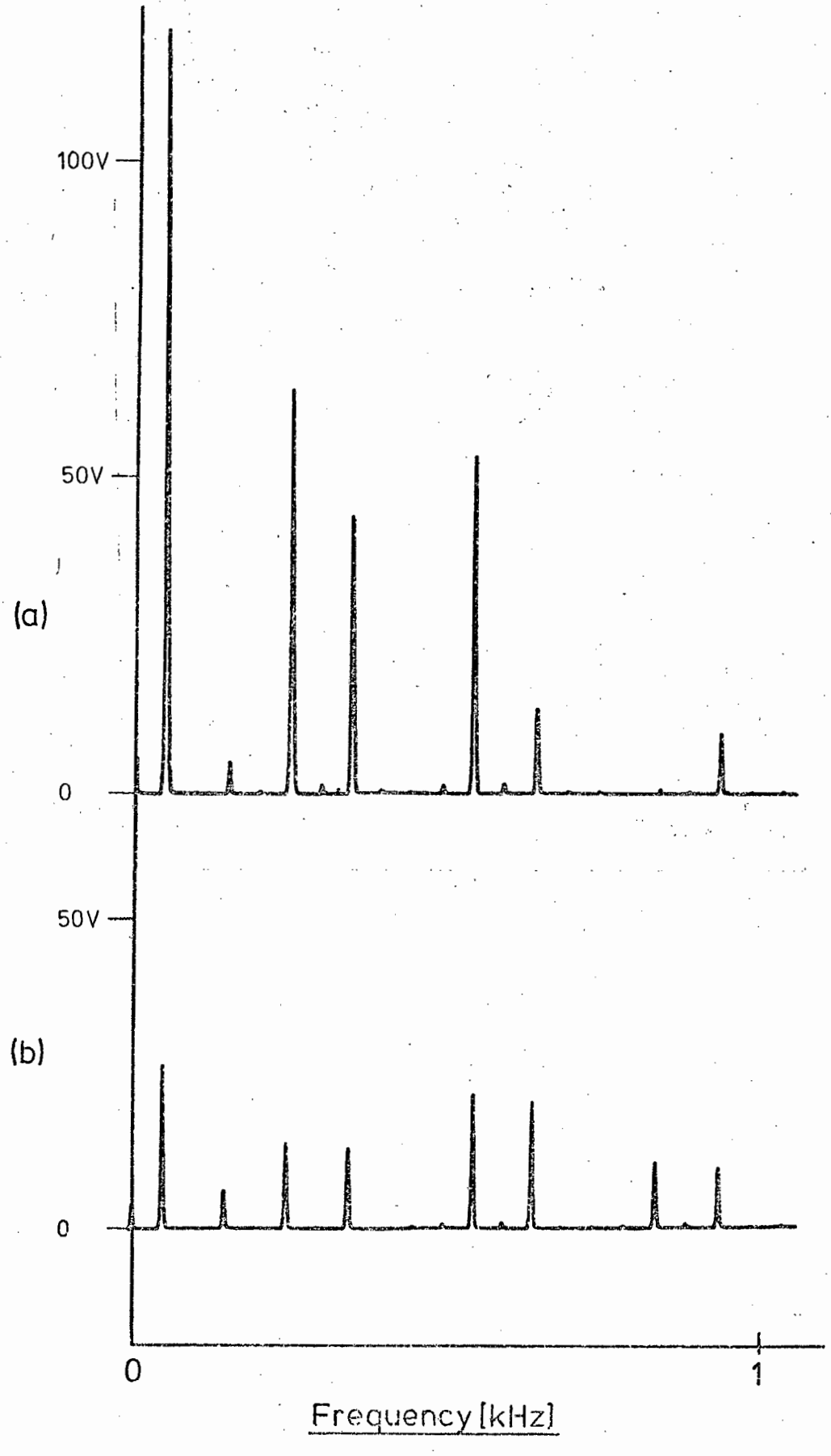
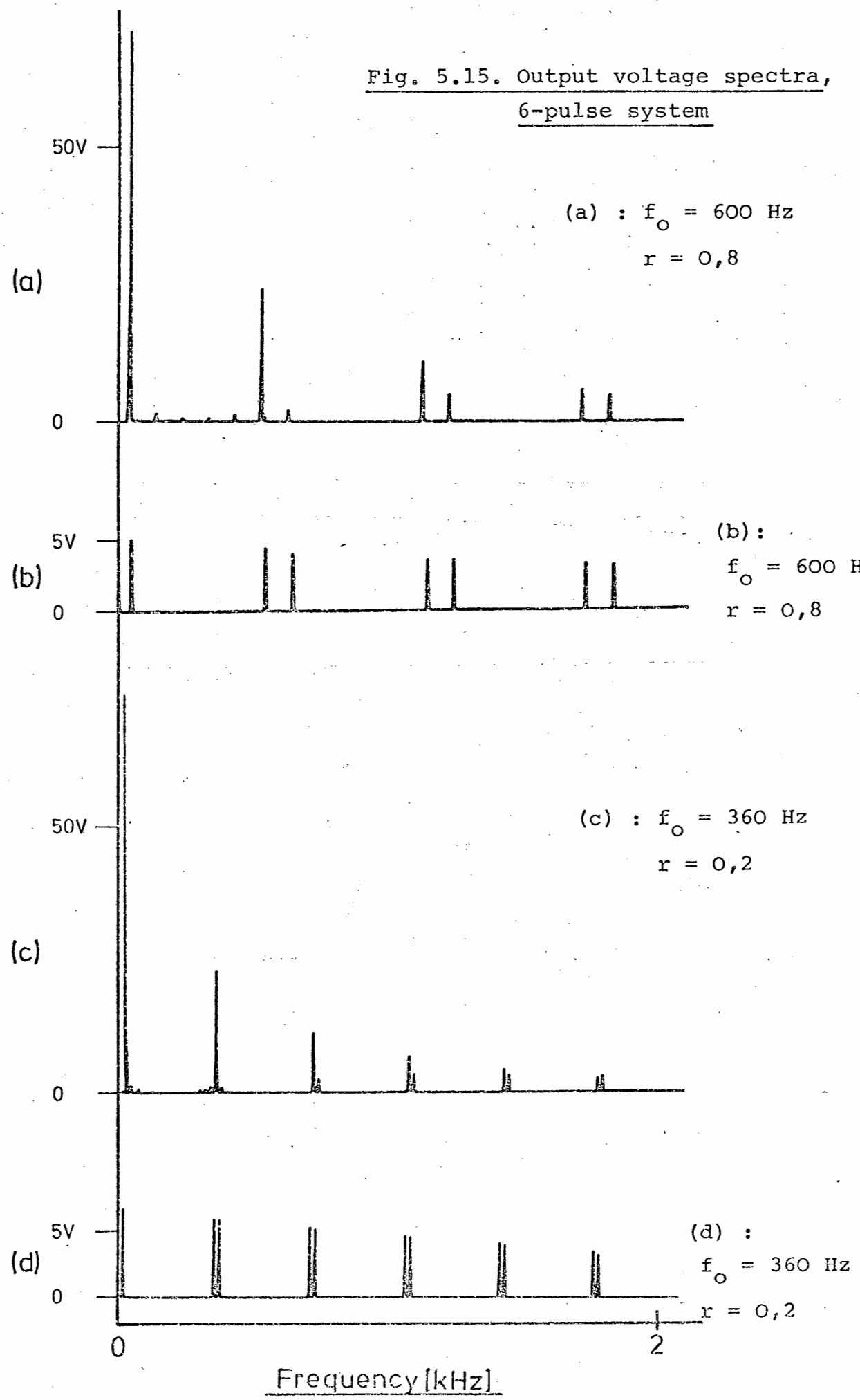


Fig. 5.14. Output voltage spectrum , 3-pulse system
f_o = 50 Hz , (a) r= 0,8 , (b) r= 0,2

Fig. 5.15. Output voltage spectra, 6-pulse system



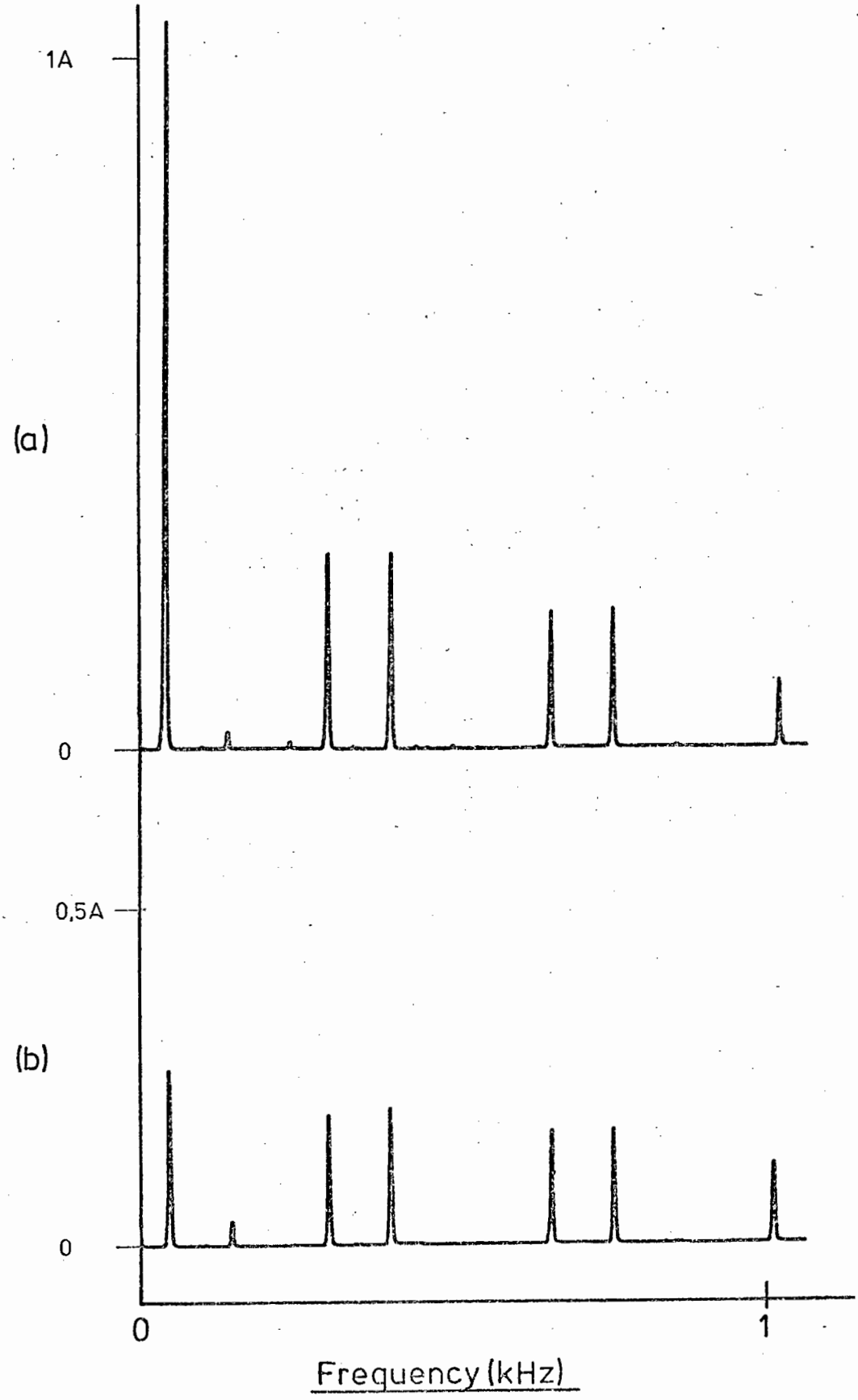


Fig. 5.16. Input current spectra , single phase inductive load , f_o= 50 Hz , (a) r= 0,8 (b) r= 0,2

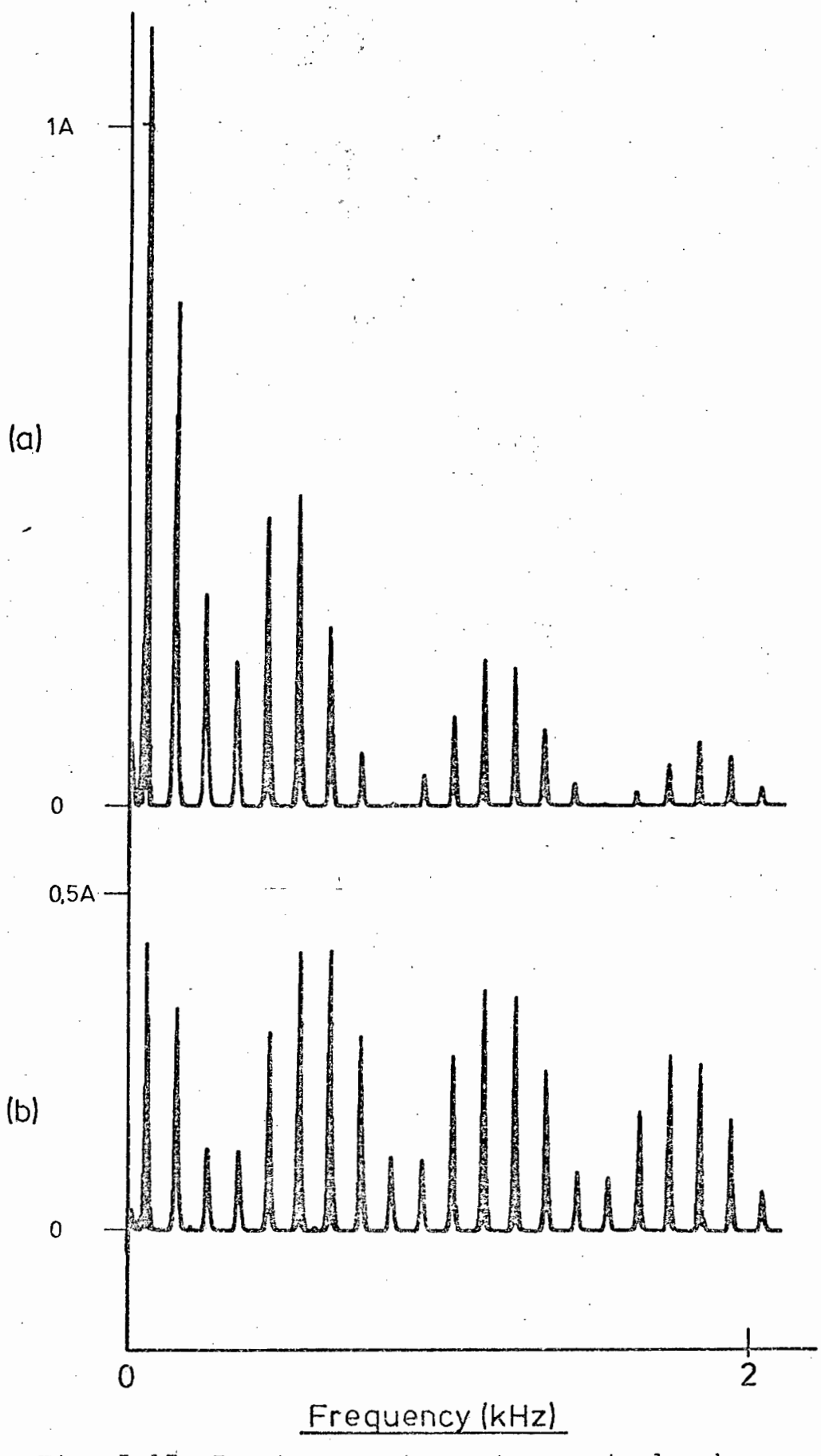


Fig. 5.17. Input current spectra , single phase resistive load , f_o= 50 Hz , (a) r= 0,8 (b) r= 0,2

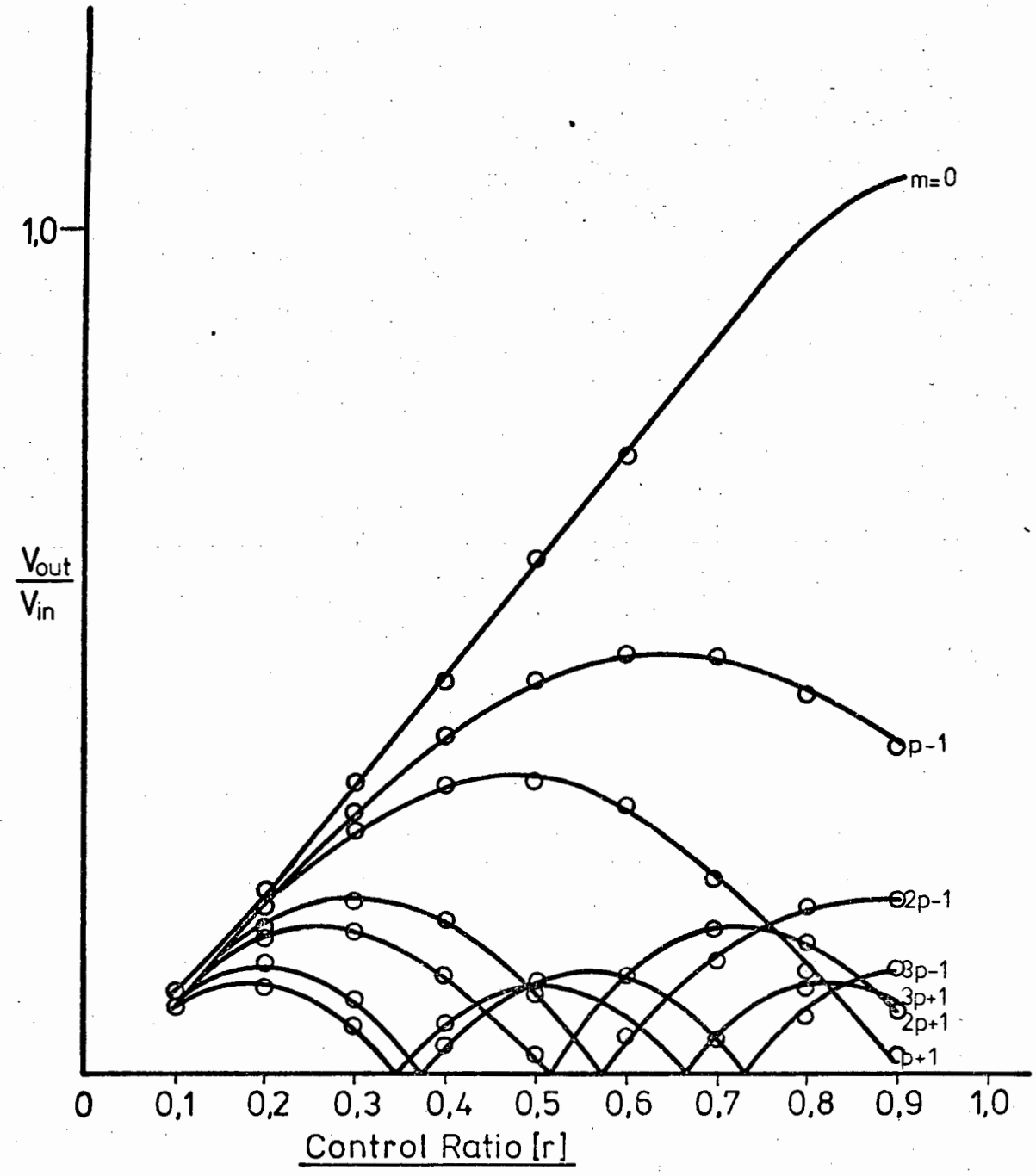


Fig. 5.18 Relative harmonic amplitudes , 6-pulse system

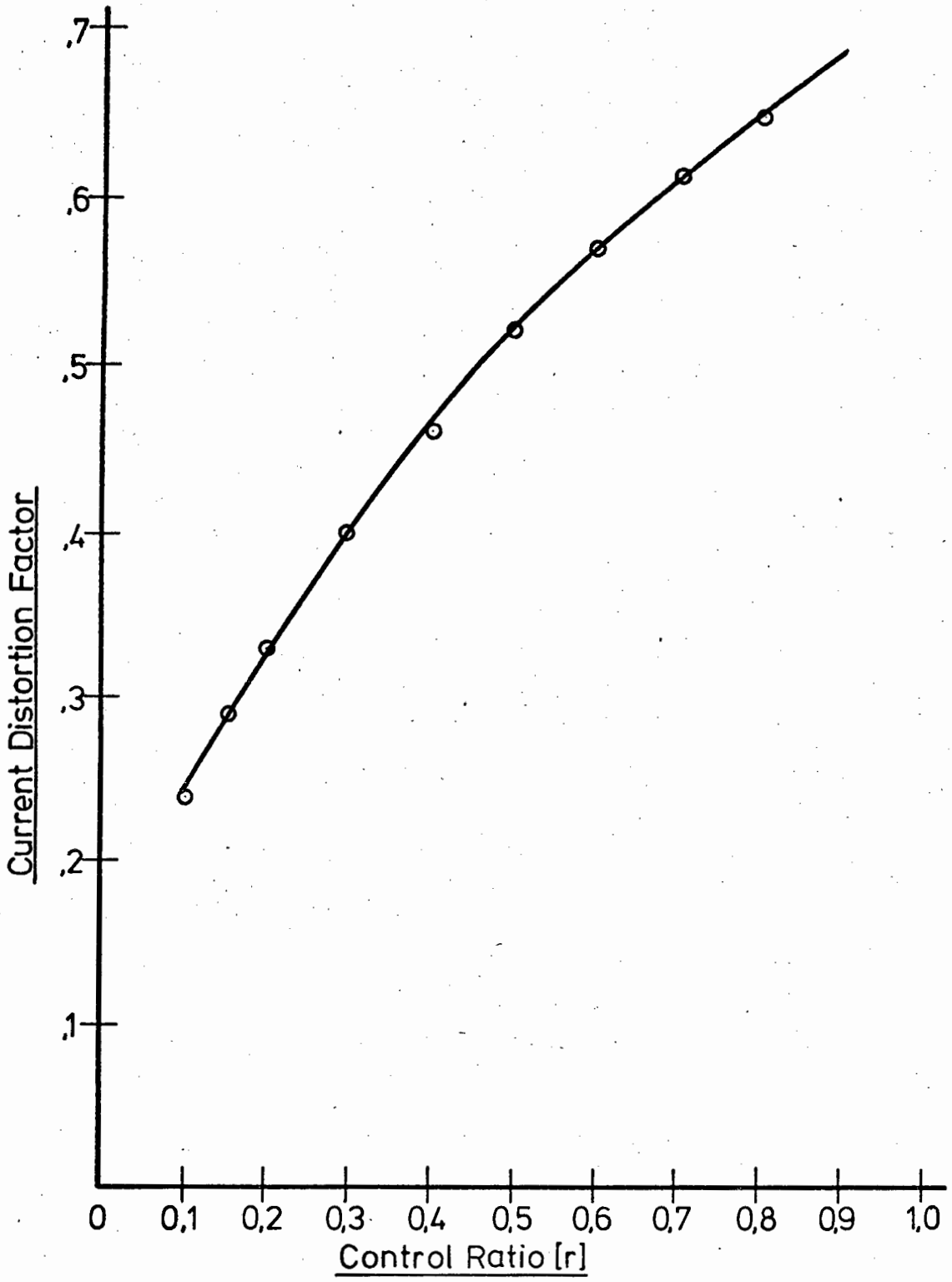


Fig. 5.19. Input current distortion factor

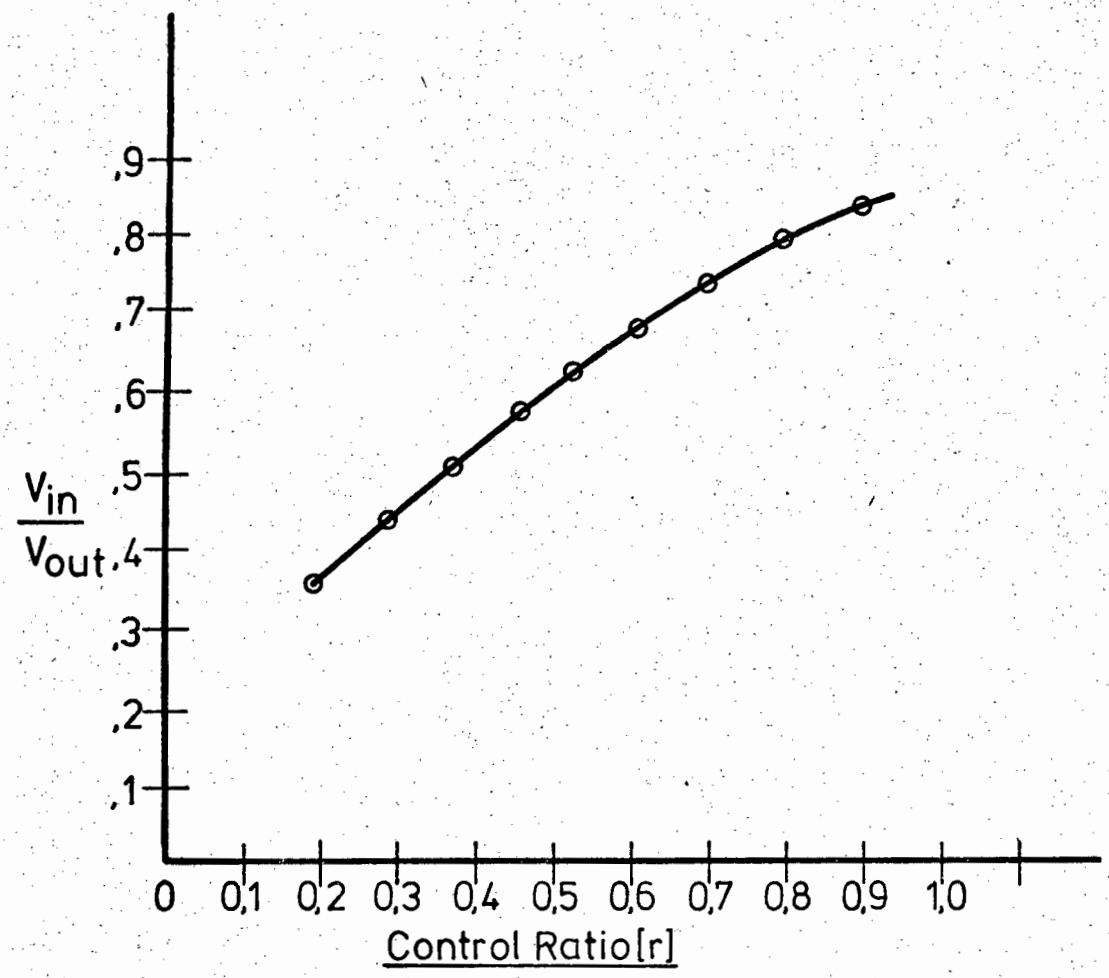


Fig. 5.20. Voltage control action

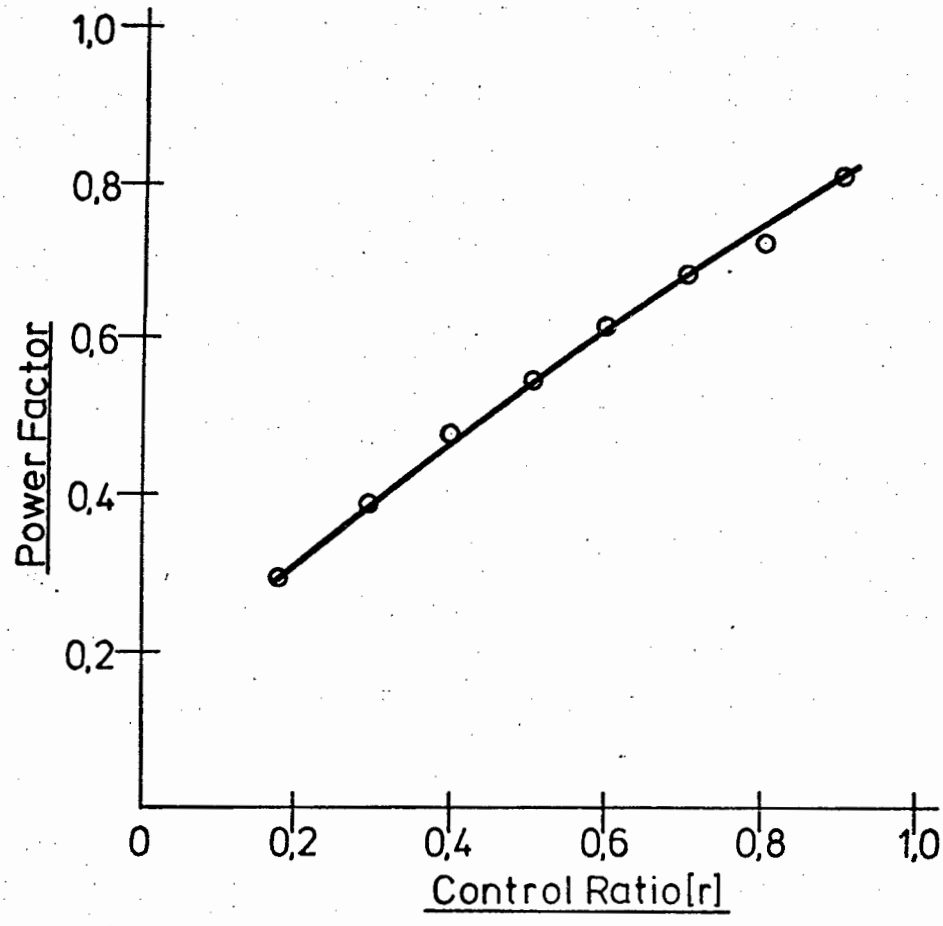


Fig. 5.21. Input power factor , resistive load

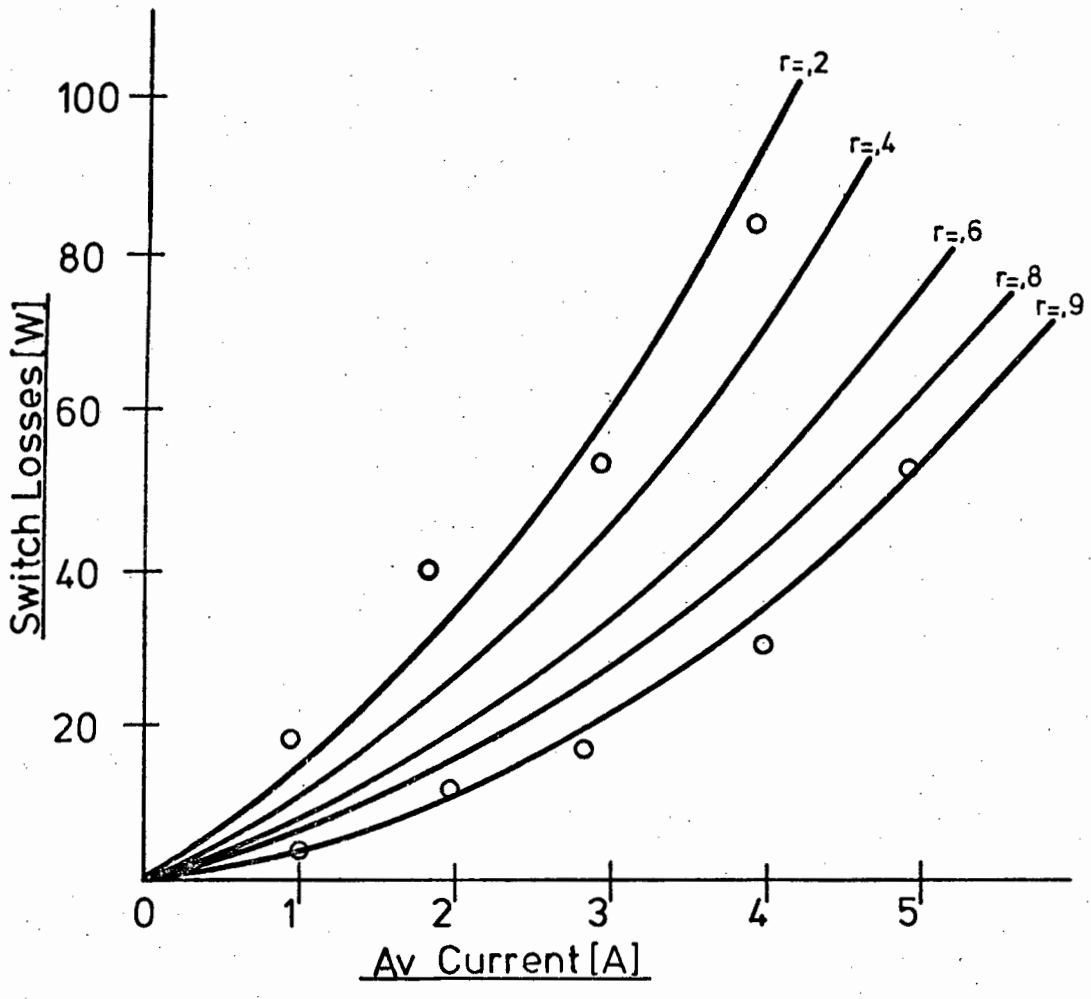


Fig. 5.22. Switch losses

for output voltage. Note that Fig. 5.18 does not indicate the negative-going part of the curves since the wave analyser used to obtain these data is not phase-sensitive.

The input current distortion factor, shown in Fig. 5.19 and obtained by means of a wave analyser examination of input current, should be compared with the calculated values shown in Fig. 2.12.

The voltage control capabilities of the converter are shown in Fig. 5.20. The test result agrees well with the result predicted in Chapter 2. Note that the output voltage in this case is the effective value which includes harmonics. This curve should be compared with Fig. 5.18 ($m = 0$) as an indication of voltage control operation.

Switch losses as a function of current for one unit with control ratio as parameter and unity power factor load are shown in Fig. 5.22 while input power factor, for the same load, as a function of control ratio is shown in Fig. 5.21.

The results shown graphically in Figs. 5.20 to 5.22 were obtained from readings of standard moving iron voltmeters and ammeters and electrodynamic wattmeters. Thus there is bound to be some error as the response to the complex waveforms produced by the converter is not known accurately. However, there is a broad agreement which gives one confidence both in the test results and the derived expressions.

Figs. 5.23 and 5.24 are the waveforms obtained from one switch driving an inductive load from a D.C. source. These illustrate normal commutation (Fig. 5.23) and the fault condition of simultaneous switch operation (Fig. 5.24). Referring to Fig. 5.23, the shunt switch opens at

A. The bypass capacitor, which in this case had a 1 ohm resistor in series, charges from A to B. Note that the current continues unchanged. At B the series switch is fully operated and the current changeover takes place. The ringing at C represents the discharge of the R-L-C second order load circuit, as indicated in para. 3.5.2.2.

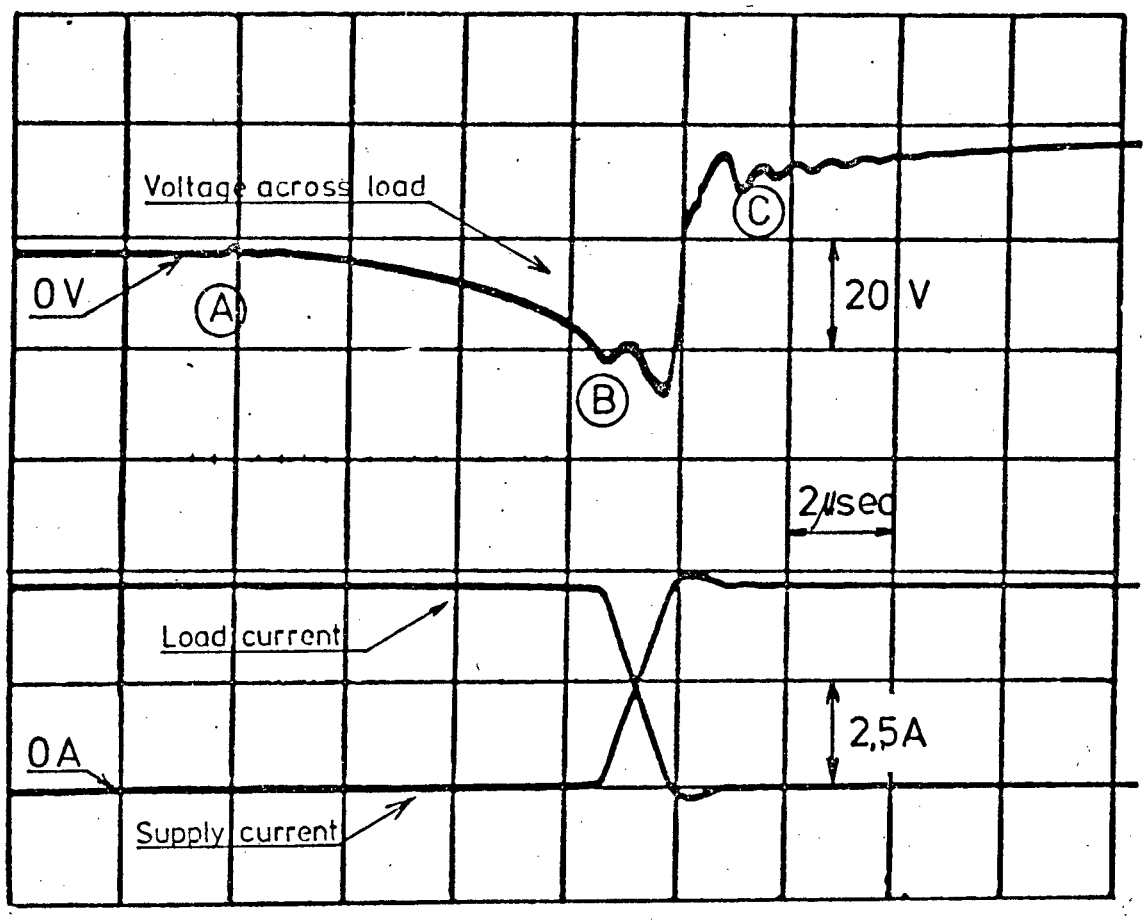
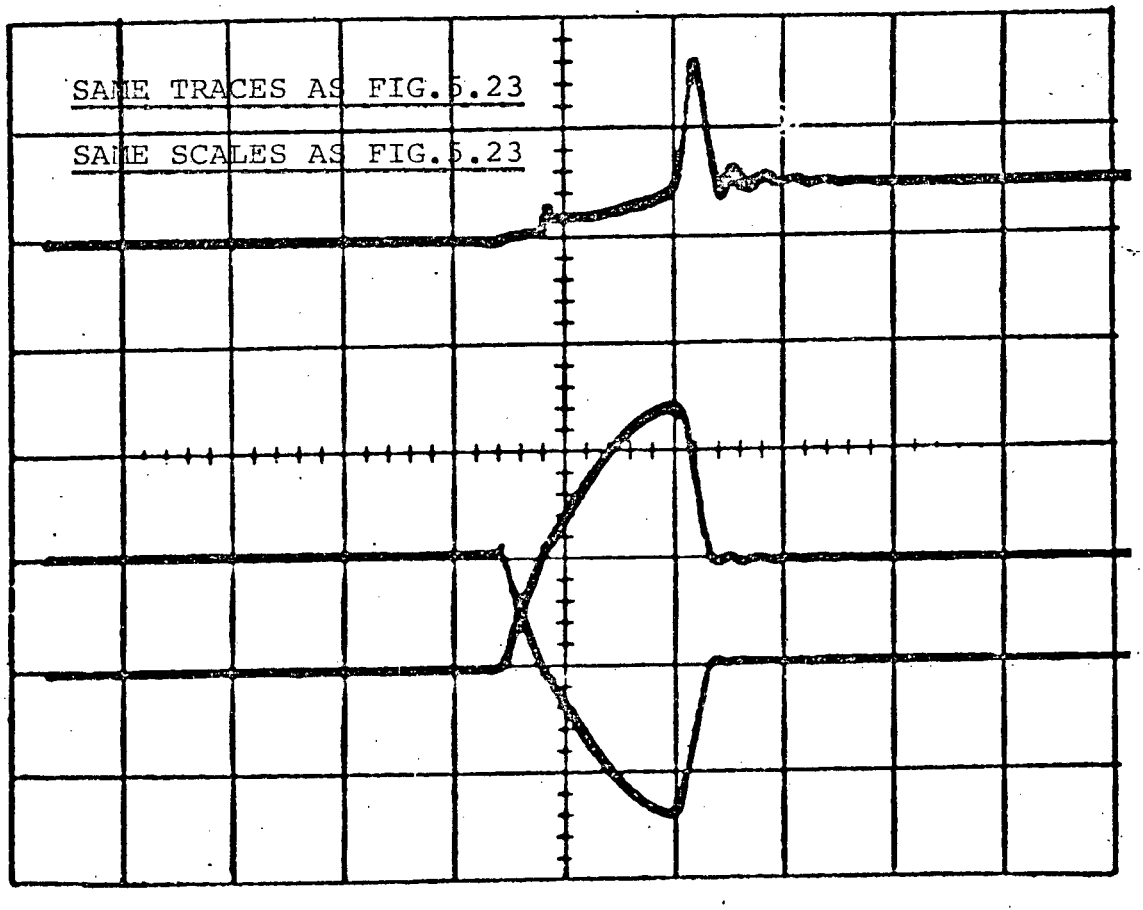


Fig. 5.23. Switch commutation , correct operation

Fig. 5.24. Switch commutation , current overlap



CHAPTER 6

A REVIEW AND SOME OBSERVATIONS:

6.1 GENERAL COMMENTS - THE ADVANTAGE OF THE SYSTEM

The system described in this work fulfills the requirements expressed in Chapter 1 for controlling the speed of an induction motor. That is, the a-mod converter enables a fixed-voltage fixed-frequency supply to be converted to a variable-frequency variable-voltage source. This has been accomplished using an electronic switch comprising a power transistor, fast-switching diodes and associated drive circuitry. This places a power-handling limitation on the experimental model, but as higher-powered transistors become available this will vanish. The question may well arise at this stage as to whether a force-commutated thyristor would not be more suitable, owing to its inherently greater robustness. There are two major problems with this approach.

The slowness of operation of even the fastest thyristor would place a severe limitation on the higher frequencies of operation of the system, when the output frequency approaches 50 HZ. It is possible to postulate that the system should operate in what has been termed the "slow-stepping" mode (14) but this introduces unacceptably low frequency supply current harmonics. Naturally this speed limitation would prevent operation above 50 HZ - a limitation which appeared even with the transistor switch employed.

The force-commutation would require an external energy source, as the periodic nature of the a.c. supply make a self energised system a hazardous proposition. This then would involve a considerable multiplication of the complexity of the system, and the commutation system would also demand an additional time penalty as energy storage elements require charging time.

The advantages of the system - that is, features advantageous in themselves, and not in comparison to any "competitors" may be stated as follows:

* Inherently fully regenerative without any power-flow sensing elements needed for control.

* Harmonics not likely to produce excessive unwanted torque components in the output of a machine coupled to the converter, even at standstill. In the event, filtering would be simple to arrange. (7)

* Reasonably low distortion factor in input current and output voltage. Again, if filtering is required, the demands placed on such a filter would not be excessive.

* The control circuitry is not complicated to the point where reliability would be impaired, being comparable to most variable-speed drive systems. (13) It would, however, be wrong to assume increased simplicity as a particular virtue. (14)

* The output frequency is unlimited, with the only restriction being the operating speed of the switching elements. In particular, the control is "smooth" around zero frequency output and may reverse the direction of rotation of an induction motor without any need for reconnecting any windings. This may well be an advantage in the "inching" operations.

The work of Schauder (ref. 7) in this regard provides

ample confirmation of the virtues of the a-mod converter as a supply to a variable-speed induction motor.This has been confirmed by a limited test (speed-torque) on a 4-pole 50 volt machine .

6.2 LIMITATIONS OF THE SYSTEM:

The use of current state-of-the-art high voltage power transistors has still shown a serious limitation to the maximum power available from the converter. Even with the BUY69A transistor it is still not feasible to operate a 380 volt machine from the experimental model. Higher voltage transistors, usually developed for T.V. work, are of a lower current rating and would have to be paralleled to supply a sufficient current to make possible reliable operation of even a 5 kW motor. (It is considered here that a large field of application lies open for drives in this class.)

When transistors with higher ratings become available then the situation will change except for the problem of base drive current. While it is possible to supply any base current demanded, the problem of providing this economically is a large one. The Darlington configuration transistor (or a Darlington circuit built up of individual transistors) is a likelihood but this usually drives the driver stage into saturation and leaves a higher voltage drop across the power transistor.

However, it should not be considered that the power transistor inherently represents a block to any further development.

The opto-coupler used is a compromise between gain and speed. An earlier experimental model was attempted using diode couplers. The high transfer loss of the device placed an undue emphasis on the subsequent stages and this approach was abandoned when it became clear that the speed loss was

more than offset by the lower transfer losses of the transistor coupler. However, the relatively low current of the experimental model meant that the snubber circuit was able to allow for the circuit delays. If a very much higher current is allowed then the use of the snubber network for this purpose might no longer be permissible and high-speed opto-coupler, of low loss, would have to be found.

Protection of the power transistor does represent a problem. The "crowbar" system adopted has the virtue of effectiveness, but it would be much simpler to use fuse protection on its own. Since this matter is a peripheral detail it does not inhibit the overall system operation, and, like larger transistors, will no doubt be solved as faster fuses appear.

A serious impediment to the use of power transistors is, however, the apparent deterioration of these devices when switching inductive loads. Gaur and Lowe have reported (23) that defects appeared in the structure of a power transistor chip after some 1000 hours of on-off switching, without any variation of electrical parameters being apparent. This would no doubt lead to what have been regarded as inexplicable failures in the past. No indication was given in this paper of the ratings of the device or of the voltage and current levels, except that second breakdown was avoided. It could well be that a generous rating system would minimise this cause of failure.

A final limitation, inherent in the system, is the power factor inversion phenomena. Strictly speaking, it could be argued that if a load demands lagging volt-amperes reactive, then the supply must supply a lagging p.f. and nothing else. However, it should be borne in mind that in

the a-mod converter, a three-phase supply is switched to a single-phase load, and thus a conventional power factor meter would not necessarily reflect the true position. It is the power factor meter that gives the supply authority his indication, and so the a-mod converter does represent a problem. A simplistic approach to this occurrence is not sufficient to explain the complex modulation process which occurs, but until a different approach to power factor prevails, any supply authority is bound to frown on a device drawing leading volt-amperes, even if only apparently.

In summing up, it may be said that the a-mod converter has few inherent limitations, and most of the present limitations are those imposed by current technology on the switching device.

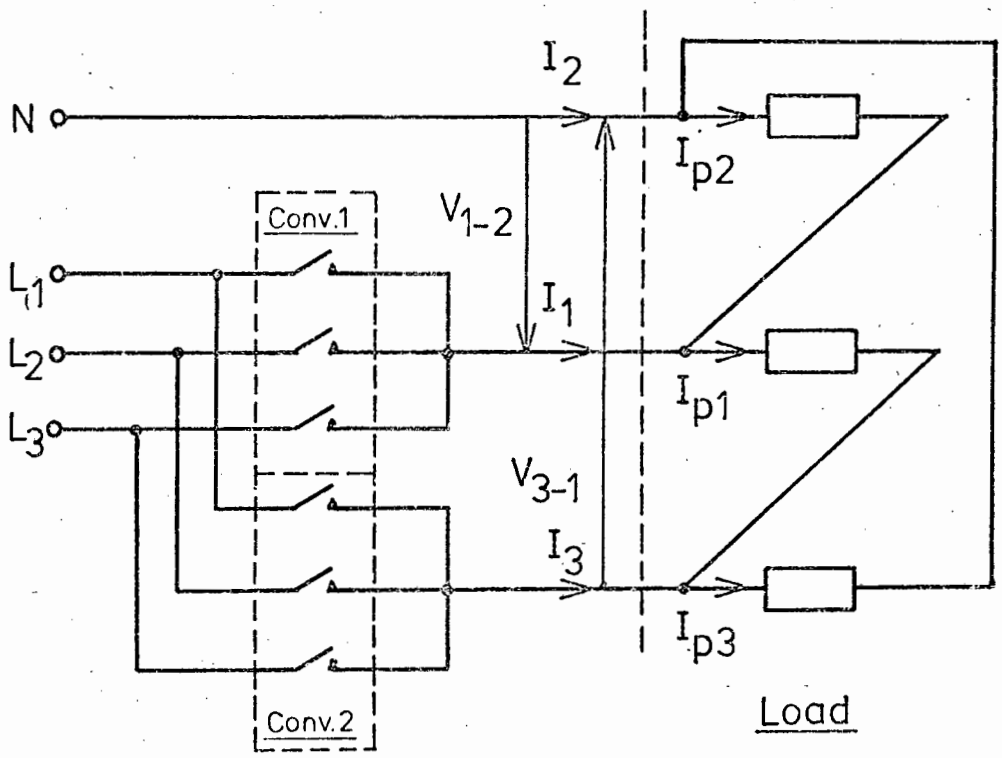
6.3 SOME FURTHER POSSIBILITIES:

As with the classical cycloconverter (9) it is possible to modify the circuit configuration in order to obtain enhancement (or suppression) of certain features of the a-mod converter.

If a lower distortion factor is aimed at, then the pulse number may be increased by using a polyphase transformer to increase the number of supply phases. The additional cost of a transformer would have to be borne as a penalty, as well as the increase in the number of power switches and control circuitry.

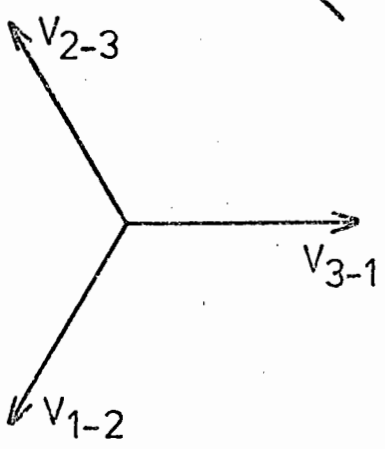
A reduction in the amount of converter "hardware" may be achieved by means of the "open-delta" connection. In this system only two (single phase output) converters are used to generate a three-phase output. This is possible, since, for a balanced three-phase system of voltages, any

Fig. 6.1. The Open-delta connection

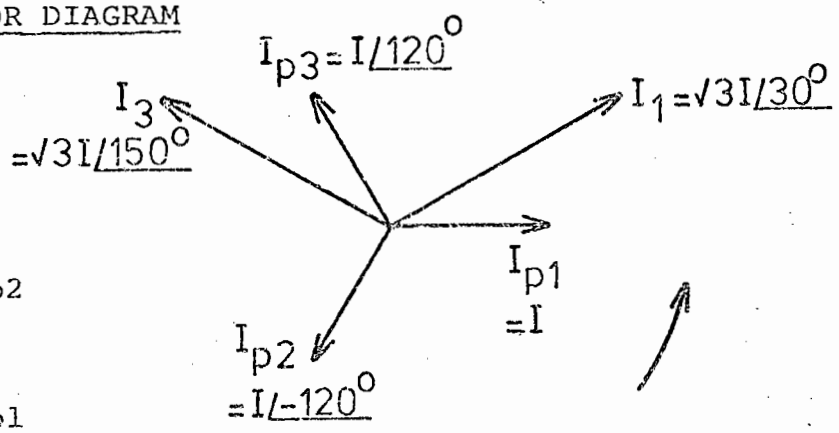


VOLTAGE PHASOR DIAGRAM

$$V_{2-3} = V_{3-1} - V_{1-2}$$



CURRENT PHASOR DIAGRAM



$$I_1 = I_{p1} - I_{p2}$$

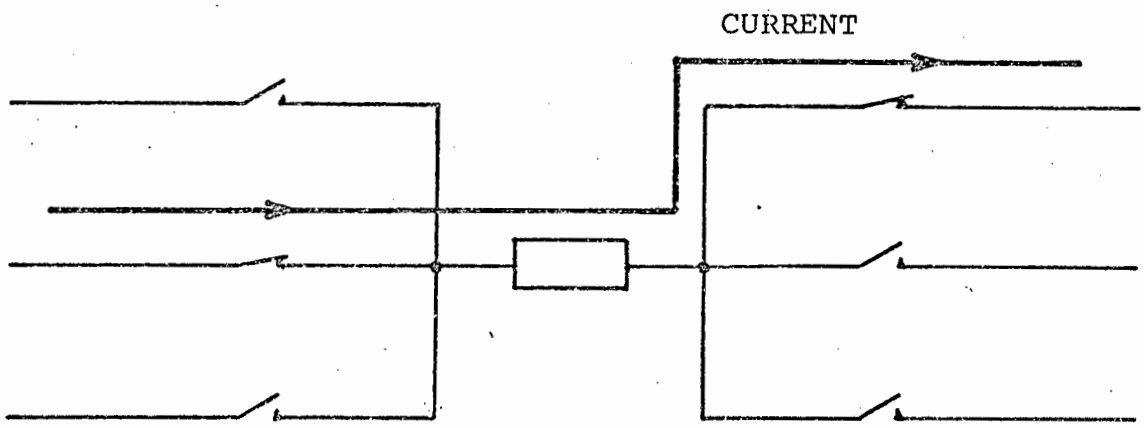
$$= \sqrt{3}I/30^{\circ}$$

$$I_3 = I_{p3} - I_{p1}$$

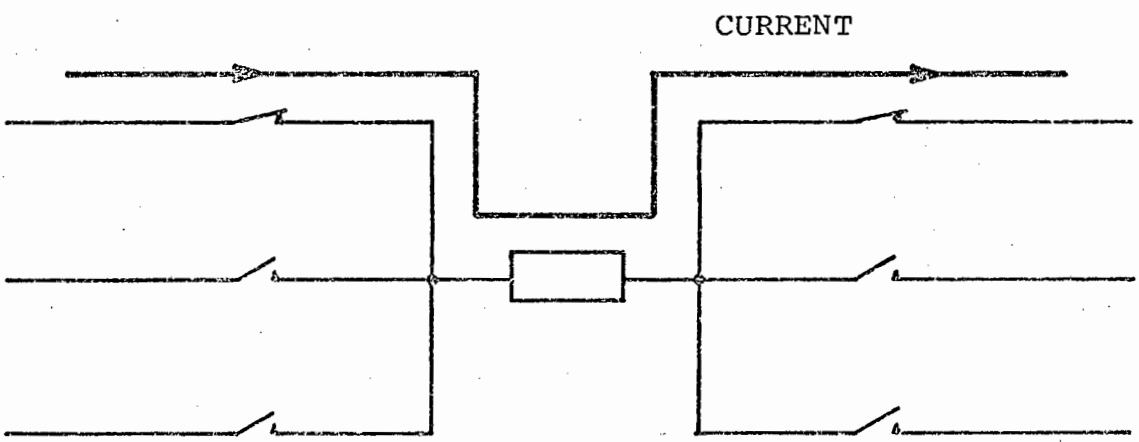
one phasor can be generated from the summation of the other two. Fig. 6.1 shows a schematic illustration of the arrangement. The disadvantage of this system is the inherently lagging displacement factor of the system. A unity displacement factor load appears as a 30^{o} lagging load, as shown on the current phasor diagram in Fig. 6.1. (Although midpoint converters are shown in Fig. 6.1, obviously bridge converters may also be used.) In addition to the displacement factor problem, care would have to be exercised in ensuring proper synchronisation between converters. On balance, the economic advantages of the open delta may well outweigh the disadvantages.

The freewheel switches of the bridge-connected converter may be eliminated by a process known as "backstepping". That is, when it is desired to turn off the supply current, both ends of the load are connected to the same supply phase for the duration of the freewheel period. The only penalty incurred is a slight increase in the complexity of the control circuitry and also this only applies to the bridge connection. Fig. 6.2 illustrates the operation. This system is decidedly the approach to adopt in any commercial application in the lower power range where the cost of the electronic equipment is a deciding factor.

The experimental converter described operated only in the open-loop mode, but there is no limitation on using, say, a tachometer feedback system to control the system. This could also be coupled with current transformers in the supply lines to exercise control over the current. These are standard control strategies for inverter-fed induction motors and their application is covered in refs. (4), (13), (25) and (32).



SUPPLY CONDUCTION



FREEWHEEL CONDUCTION

Fig.6.2. Backstepping mode

The question of operation at higher voltages and currents, with particular reference to the feedback system, deserves some further attention. It has been pointed out that, in the experimental model, there is a finite delay in the operation of the feedback system. This is unavoidable in any configuration, and the possibility arises that at high currents, say hundreds of amperes, the voltage rise across the "turning-off" transistor might reach catastrophically high levels. Assuming that turn-on delays do not increase, and there is no reason to believe that they should, then a ten-fold increase in current produces (for constant inductance) an equal voltage rise. An examination of equations 3.27 and 3.28 shows that the voltage rise is also a linear function of bypass (or snubber) capacity, and thus one can easily postulate a considerable increase in the value of this capacitor and still remain within the bounds of reasonableness. Thus, the feedback system is well able to function at considerably increased power levels, and must play an important part in making the reliable operation of the a-mod converter possible.

6.4 AN ECONOMIC COMPARISON WITH OTHER DRIVE SYSTEMS:

The survey by Ludbrook (31) provides an excellent base for discussion. Firstly, it should be noted that the non-regenerative d.c. drive remains the cheapest, but is not necessarily the best for all applications.

Any comparison with the a-mod converter should be made on equal terms. That is, any comparitive system should be regenerative and able to operate a standard machine. Thus, the comparison will be made with the following:

TABLE 1

Type of System	Comments	Rating (kW)	Transformer	Power Electronics	Control Electronics	Forced Commutation	Total
D.c. regenerative	Poor power factor at low speeds.	10	1,5	2,0	1,0	-	4,5
		100	7,5	20,0	1,3	-	28.8
Voltage-fed inverter	Requires "inverter grade" thyristors. Assume these cost 2 times standard thyristors.	10	1,5	3,7	1,0	1,0	7,2
		100	7,5	3,7	1,3	10,0	55,8
Current-fed inverter	Operates with standard thyristors. Cost of commutating components same as v-fed inverter.	10	1,5	2,3	1,0	1,0	5,8
		100	7,5	23,0	1,3	10,0	41,8
Cycloconverter (Non-circulating current)	Limited speed range. Lower utilisation factor of power components.	10	2,0	6,0	3,0	-	11,0
		100	10,0	60,0	3,9	-	73.9
A-mod converter	Since there is no natural commutation, no transformer needed.	10	-	7,0	3,0	-	10,0
		100	-	70,0	3,9	-	73,9

* D.C. Regenerative drive (D.C. motor fed from dual converter)
* Voltage-fed inverter to induction motor, regenerative
* Current-fed inverter to induction motor
* Cycloconverter

The following assumptions are made about costs:

* Cost of transformers proportional to 1,5 X $(\text{rating})^{0,7}$. It is assumed desirable to operate all drives from a transformer intended to supply commutation leakage reactance. The a-mod converter does not need this transformer.
* Cost of thyristors and transistors proportional to rating.
* Cost of electronic control circuitry, and auxiliary controls such as interlocks, proportional to $(\text{rating})^{0,1}$. This includes thyristor firing circuits and transistor base drives.
* Cycloconverter and a-mod converter power devices yield only half the power of d.c. bridges because of duty cycle considerations.
* Cost of a power diode is one third that of a power transistor or thyristor.
* Cost of commutating components proportional to rating. (Inductors and capacitors.)

The relative costs are tabulated in Table 1. Although it might be possible to dispute the basis for the cost comparison on an absolute basis, this table shows that the a-mod converter is cost-comparable with the cycloconverter. In every case it might be argued that the competing system has a glaring defect which makes it unsuitable for some or other application, e.g.

Drive System	Defect
D.c. regenerative drive	Uses d.c. motor with attendant commutator problem
Voltage-fed inverter	Commutation problems
Current-fed inverter	Uneven rotation at low speeds
Cycloconverter	Limited speed range

Thus taken all around, the a-mod offers a premium performance at a cost comparable to its competitors.

6.5 FINAL CONCLUSION:

This thesis has examined in detail a direct a.c. to a.c. frequency converter. A member of the cycloconverter family, it has been given the name of asynchronous modulation converter to distinguish it from the other converters which need to be synchronised to the supply frequency. Expressions have been derived for the input current and output voltage and these have been verified experimentally.

The experimental model, using power transistors as switches, demanded that a feedback system be developed to make their (the transistors') utilisation possible. The operation of this feedback system has been examined and described in detail. From the experimental model, design criteria were established for the system, making further development possible.

Plate 1 shows one of the switch units of the experimental model . Clearly to be seen are the snubber network , diode bridge , and the driver stage .

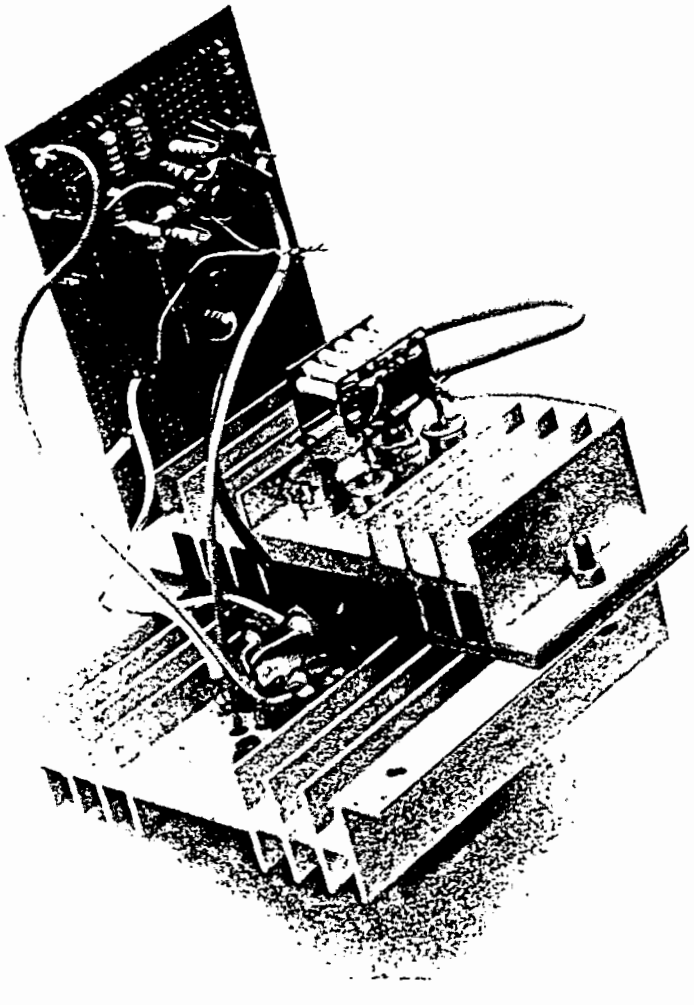


Plate 1 . The complete switch.

REFERENCES

1. Walker, M. "The control of the speed and power factor of induction motors". Ernest Benn Ltd., London (1924).

2. Van Wyk, J.D. "Power - and machine - electronics 1914 - 1966". S.A.I.E.E., Johannesburg (1967).

3. Kemp, P. "Alternating current electrical engineering". MacMillan, London (1963).

4. Pike, C.H. "Automatic control of industrial drives". Newnes-Butterworths, London (1971).

5. Jayawant, B.V. "Induction machines". McGraw-Hill, London (1968).

6. Fitzgerald, A.E. and Kingsley, Charles "Electric Machinery". 2nd ed., McGraw-Hill, New York (1961).

7. Schauder, C.D. "Induction motors with modulated terminal voltage". Ph.D. thesis, U.C.T., (1978).

8. Rissik, H. "The fundamental theory of arc convertors". Chapman and Hall, London (1939).

9. Pelly, B.R. "Thyristor phase-controlled converters and cycloconverters". Wily-Interscience, New York (1971).

10. Mazda, F.F. "Thyristor Control". Newnes-Butterworths, London (1973).

11. Rice, L.R. (ed.) "Silicon controlled rectifier designer's handbook". Westinghouse, Youngwood, Penna. (1970).

12. Gyngyi, L. and Pelly, B.R. "Static power frequency changers". John Wiley and Sons, New York (1976).

13. Fink, D.G. (ed.) "Electronic Engineers Handbook". McGraw-Hill, New York (1975).

14. Hurley, N.V., "A static frequency changer for the speed control of induction motors". M.Sc. thesis, U.C.T. (1974).

15. Case, M.J. and Enslin, N.C. "A direct a.c. to a.c. frequency converter suitable for variable speed induction motors". Trans. S.A.I.E.E. Vol. 68 part 9, Sept. 1977.

16. Brown, J. and Glazier, E.V.D. "Telecommunications", Science Paperbacks, London (1964).

17. Case, M.J. and Enslin, N.C. "A high speed transistorized commutating circuit". Conf. Rec. S.A.I.E.E. Conference on "Electronic Control of Rotating Electric Machines" pp. 130-137.

18. Bowler, P. "Power Transistors in Variable Speed Drives". Electronics and Power, October 1978.

19. Greenberg, Ralph (ed.) "Motorola Power Transistor Handbook". Motorola, Phoenix Arizona (1961).

20. Roehr, W.D. (ed.) "Switching Transistor Handbook". Motorola, Phoenix Arizona (1963).

21. "R.C.A. Silicon Power Circuits Manual", Radio Corporation of America, Harrison (1967). (No author stated.)

22. Various authors, "Power transistors in the switching mode". Sescosem, Aix en Provence, 1974.

23. Gaur, S.P. and Lowe, G. "Power Transistor Crystal Damage in Inductive Load Switching". Solid-State Electronics, 1977 Vol. 20.

24. Van Valkenburg, M.E. "Network Analysis". 3 ed., Prentice-Hall, Englewood Cliffs, New Jersey, 1974.

25. Phillips, K.P. "Current-source converter for a.c. motor drives". I.E.E.E. Transactions Vol. IA - 8, No. 6, 1972.

26. Farrer, W. "Quasi-sine-wave fully regenerated invertor". I.E.E. Proceedings, Vol. 120 No. 9 1973.

27. Heumann, K. "Pulse control of d.c. and a.c. motors by silicon controlled rectifiers". I.E.E.E. Trans. 1964 CE-73, Vol. 83.

28. Turnbull, F.G. "Selected harmonic reduction in static d.c. - a.c. inverters". I.E.E.E. Trans. C.E.-73, Vol. 83.

29. Lienau, W. and Müller-Hellmann, A. "Möglichkeiten zum Betrieb von stromeinprägenden Wechselrichtern ohne niederfrequente Oberschwingungen". et z-a Bd. 97 (1976) H. 11.

30. Kloss, A. "Netzstromoberschwingungen bei Direktumrichtern". Bull. SEV/VSE 69 (1978) 24.

31. Ludbrook, A. "Basic economics of thyristor adjustable speed drive systems". Power Semiconductor Applications, J.D. Harnden ed., I.E.E.E., New York (1972).

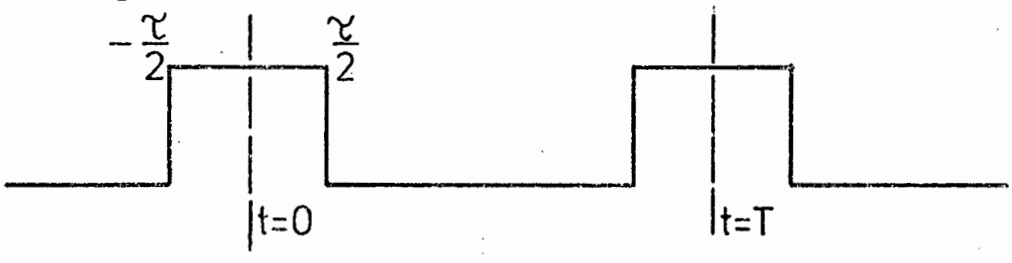
32. Miller, D.W. and Lawrence, R.G. "Variable frequency inverter and its application to motor drives". Electronics and Power, Vol. 22 No. 10, Oct. 1976 pp. 675-678.

33. Daniels, A.R. and Slattery, D.T. "Applications of power transistors to polyphase regenerative power converters". Proc. I.E.E. Vol. 125 No. 7 , July 1978 , pp. 643 - 647 .

APPENDIX 1 OUTPUT VOLTAGE EXPRESSION

A1.1 THE SWITCHING FUNCTION:

The 3-phase supply is sampled by a 3-phase switching function S_n of period T , where one phase would have a waveshape :



Using the Fourier series to analyze this function , we have :

$$a_o = \frac{1}{T} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} dt = \frac{1}{T} (\tau) = \frac{\tau}{T}$$

$$a_n = \frac{2}{T} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} \cos n\omega t \, dt$$

$$= \frac{2}{n\omega T} (\sin n\omega\frac{\tau}{2} + \sin n\omega\frac{\tau}{2})$$

$$= \frac{2}{n\pi} \sin n\pi\frac{\tau}{T}$$

$$b_n = \frac{2}{T} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} \sin n\omega t \, dt$$

$$= 0$$

Thus :

$$S_{n(\omega_i t)} = \frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos \{n(\omega_i t - (j-1)\frac{2\pi}{3})\}$$

where j = 1 , 2 or 3

For some output frequency ω_o , the sampling rate is changed to $(\omega_i + \omega_o)$ or $(\omega_i - \omega_o)$, depending on the direction of phase rotation . It is more convenient to sample at $(\omega_i + \omega_o)$, since this produces higher frequency harmonics which are more easily filtered .

Then ,

$$S_{n(\omega_i t, \omega_o t)} = \frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos \{ n(\omega_i t + \omega_o t - (j-1)\frac{2\pi}{3}) \}$$

A1.2 THE OUTPUT VOLTAGE

The 3-phase supply to the converter may be described by

$$v_i = V_i \cos (\omega_i t - (j-1)\frac{2\pi}{3})$$

where j = 1 , 2, or 3

The output of the converter is then :

$$v_o = v_i \times S_{n(\omega_i t, \omega_o t)}$$

Or

$$v_o = \{V_i \cos(\omega_i t - (j-1)\frac{2\pi}{3})\}\{\frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos\{.....$$

$$....\{n(\omega_i t + \omega_o t - (j-1)\frac{2\pi}{3}\}\}$$

$$= \frac{\tau}{T} V_i \cos(\omega_i t - (j-1)\frac{2\pi}{3}) + ...$$

$$... + \frac{2V_i}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T} \cos\{n(\omega_i t + \omega_o t - (j-1)\frac{2\pi}{3}\}\cos...$$

$$... \cos\{\omega_i t - (j-1)\frac{2\pi}{3}\}$$

Since the supply is balanced 3-phase , the first term of the above expression is zero . Thus :

$$v_o = \frac{2V_i}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T} \cos\{n(\omega_i t + \omega_o t - (j-1)\frac{2\pi}{3}\} \cos....$$

$$...\cos\{\omega_i t - (j-1)\frac{2\pi}{3}\}$$

$$= \frac{3V_i}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T} \{\cos\{(n-1)\omega_i t + n\omega_o t\} +.....$$

$$..+ \cos\{(n+1)\omega_i t + n\omega_o t\}\}$$

Noting that all harmonics of ω_i must be multiples of mp , where p = pulse number and m = any integer , which means that mp is a multiple of 3 for 3-phase systems , then

$mp = n + 1$ and $mp = n-1$

or $n = mp - 1$ and $n = mp + 1$

Thus

$$v_o = \frac{3V_i}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp + 1)\frac{\pi\tau}{T}}{mp + 1} \{\cos\{mp\omega_i t + (mp + 1)\omega_o t\}\} + ...$$

$$...+ \frac{3V_i}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp + 1)\frac{\pi\tau}{T}}{mp + 1} \{\cos\{mp\omega_i t + (mp - 1)\omega_o t\}\}$$

or

$$v_o = \frac{3V_i}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{mp\omega_i t + (mp \pm 1)\omega_o t\}\}$$

APPENDIX 2 VOLTAGE DISTORTION FACTOR

The maximum values of the voltage distortion factor are obtained as follows :

V.D.F. (At maximum conduction)

$$= \frac{\text{R.M.S. fundamental output volts}}{\text{Total R.M.S. output volts}}$$

For a 6-pulse bridge ,

$$V_{olr.m.s.} = \frac{6V_i}{\pi\sqrt{2}} \times \frac{1}{2} = \frac{3V_i}{\pi\sqrt{2}}$$

and $$V_{or.m.s.} = \frac{3V_i}{\pi\sqrt{2}} \sqrt{\left(1 + \frac{1}{5^2} + \frac{1}{7^2} + \frac{1}{11^2} + \frac{1}{13^2} + \ldots\right)}$$

$$= \frac{3V_i}{\pi\sqrt{2}} \sqrt{\left(\frac{\pi^2}{9}\right)}$$

$$= \frac{V_i}{\sqrt{2}}$$

Thus V.D.F. $= \frac{3V_i}{\pi\sqrt{2}} \div \frac{V_i}{\sqrt{2}} = \frac{3}{\pi} = 0,95$

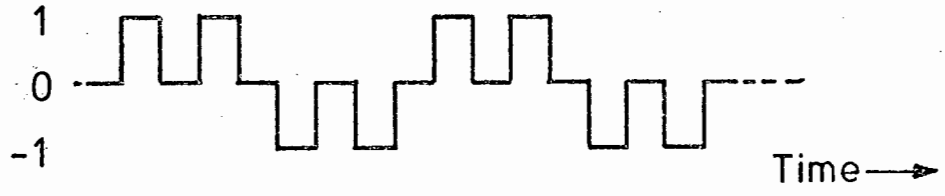
For a 3-pulse midpoint system ,

$$V_{olr.m.s.} = \frac{3\sqrt{3}V_i}{2\sqrt{2}\pi} \quad \text{and} \quad V_{olr.m.s.} = \frac{3V_i}{\pi\sqrt{2}}$$

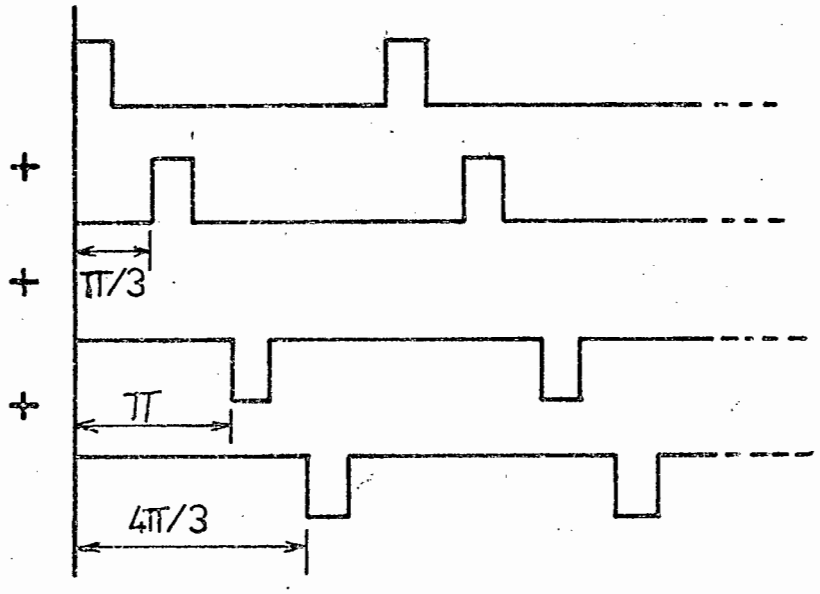
Thus V.D.F. $= \frac{3\sqrt{3}}{2\pi} = 0,826$

APPENDIX 3 INPUT CURRENT , SINGLE PHASE BRIDGE OUTPUT

The control pulse train is as follows :



This is equivalent to :



Thus $S_{n(\omega_i t)} = \frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos n\omega_i t + ...$

$$...+ \frac{\tau}{T} + \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos(n\omega_i t + \frac{n\pi}{3}) -....$$

$$...- \frac{\tau}{T} - \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos(n\omega_i t + n\pi) -....$$

$$...- \frac{\tau}{T} - \frac{2}{n\pi} \sum_{n=o}^{n\to\infty} \sin \frac{n\pi\tau}{T} \cos(n\omega_i t + \frac{4n\pi}{3})$$

This reduces to :

$$S_{n(\omega_i t)\,(\omega_o t)} = \frac{4}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T} \{ \cos n\omega_i t + \cos(n\omega_i t + \frac{n\pi}{3}) \}$$

where $n = (mp \pm 1)$ since $n \neq mp$ for input current (ref. 8)

If the pulse train is modulated , then

$$S_{n(\omega_i t)\,(\omega_o t)} = \frac{4}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T}\{\cos n(\omega_i t + \omega_o t) + \cos n(\omega_i t + \omega_o t + \frac{\pi}{3})\}$$

Note : n is odd ; not a multiple of 3

The input current per phase is thus :

$$i_{ph} = i_o \times S_n$$

$$= I_o \cos \omega_o t \times S_{n(\omega_i t, \omega_o t)}$$

$$= \frac{2I_o}{n\pi} \sum_{n=o}^{n\to\infty} \sin\frac{n\pi\tau}{T}\{\cos(n\omega_i t + n\omega_o t + \omega_o t) + \cos(n\omega_o t + n\omega_i t - \omega_o t)$$

$$\ldots\ldots + \cos(n\omega_i t + n\omega_o t + \omega_o t + \frac{n\pi}{3}) + \ldots\ldots$$

$$\ldots\ldots + \cos(n\omega_i t + n\omega_o t - \omega_o t + \frac{n\pi}{3})\}$$

This expression only exists when $n = (mp \pm 1)$

i.e. $\neq$ odd multiple of 3

Thus

$$i_{ph} = \frac{2I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{(mp \pm 1)\omega_i t + mp\omega_o t + \frac{(mp \pm 1)\pi}{6}\}\}$$

In the case of the 3-pulse midpoint system ,

$$i_{ph} = \frac{\tau}{T} I_o \cos\omega_o t + \frac{2I_o}{\pi} \sum_{m=o}^{m\to\infty} \frac{\sin(mp \pm 1)\frac{\pi\tau}{T}}{(mp \pm 1)} \{\cos\{(mp \pm 1)\omega_i t + mp\omega_o t\}\}$$

For the 6-pulse bridge system, the input current fundamental is :

$$I_1 = \frac{2\sqrt{3}I_o}{\pi} \sin\frac{\pi\tau}{T} \cos(\omega_i t + \frac{\pi}{6})$$

which occurs when m = O

APPENDIX 4 INPUT CURRENT DISTORTION FACTOR

By definition (ref. 9)

$$\text{Current distortion factor} = \frac{I_{il}}{I_{irms}} = \mu$$

$$= \frac{\text{R.M.S. fundamental input current}}{\text{R.M.S. total input current}}$$

at maximum conduction period.

For a 6-pulse bridge , $\mu = 0,95$

(This result is identical to the V.D.F. since the constants involved are the same).

For a 3-pulse midpoint converter ,

$$I_{r.m.s.total} = \sqrt{(\tfrac{1}{3}I_o^2) + \{\frac{2I_o}{\pi\sqrt{2}} \times \frac{\sqrt{3}}{2} \times 1,17\}^2}$$

$$= 0,5649I_o$$

$$I_{r.m.s.fund.} = \frac{2\sqrt{3}}{2\pi\sqrt{2}} I_o$$

$$= 0,3898I_o$$

Thus $\mu = 0,68$

APPENDIX 5 CHARACTERISTICS OF THE POWER TRANSISTOR AND OPTO-ISOLATOR EMPLOYED

NPN SILICON POWER TRANSISTOR

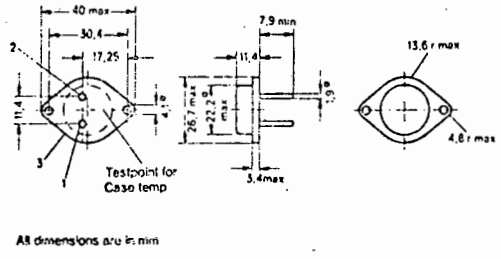
873

BUY69 SERIES TRANSISTORS ARE DESIGNED FOR USE IN

- Switching Mode Power Supplies
- Inverters
- C.R.T. Scanning Systems

They Feature High Voltage and Peak Current Capability
Together with Fast Switching and a High Degree of Robustness

mechanical specification



All dimensions are in mm

TO-3

absolute maximum ratings (at 25 °C case temperature)

	BUY69A	BUY69B	BUY69C
Collector-Base Voltage (I_E = 0)	1000 V	800 V	500 V
Collector-Emitter Voltage (I_B = 0)	400 V	325 V	200 V
Emitter-Base Voltage	←	8 V	→
Continuous Collector Current Peak (see Note 1)	←	15 A	→
Continuous Collector Current Continuous	←	10 A	→
Continuous Base Current	←	3 A	→
Continuous Dissipation (V_{CE} = 17 V) See Note 2	←	100 W	→
Operating Temperature Range	←	−65 °C to +200 °C	→

NOTES: 1. Pulse Width ≤ 500 μSec. Duty Cycle ≤ 25 %.
2. Refer to Safe Operating and Dissipation Derating Curves.

NPN SILICON POWER TRANSISTOR

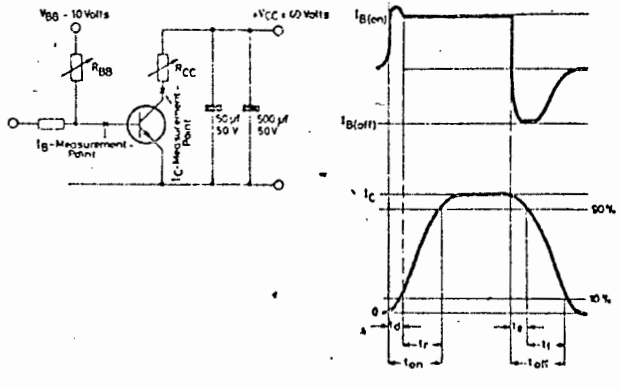
electrical characteristics at 25 °C case temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		TYPE	MIN	TYP	MAX	UNIT
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 1 mA, See Note 1	I_E = 0	BUY69A	1000			V
				BUY69B	800			V
				BUY69C	500			V
LV_{CEO}	Collector-Emitter Latching Voltage	I_C = 50 mA,	I_B = 0	BUY69A	400			V
				BUY69B	325			V
				BUY69C	200			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_B = 10 mA		BUY 69A	8			V
				BUY69B	8			V
				BUY69C	8			V
I_{CEX}	Collector-Emitter Leakage Current	V_{CE} = 1000 V		BUY69A			1.0	mA
		V_{CE} = 800 V	V_{BE} = −2 V	BUY69B			1.0	mA
		V_{CE} = 500 V		BUY69C			1.0	mA
h_{FE}	DC Current Gain	I_C = 2.5 A, See Note 3	V_{CE} = 10 V	BUY69A	15			
				BUY69B	15			
				BUY69C	15			
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 8.0 A,	I_B = 2.5 A	BUY69A			2.2	V
				BUY69B			2.2	V
				BUY69C			2.2	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 8.0 A,	I_B = 2.5 A	BUY69A			3.3	V
				BUY69B			3.3	V
				BUY69C			3.3	V
t_f	Collector-Current Fall Time	I_C = 8.0 A, $I_{B(on)}$ = 2.5 A,	V_{CE} = 40 V $I_{B(off)}$ = 2.5 A	BUY69A			1.0	μs
				BUY69B			1.0	μs
				BUY69C			1.0	μs
f_t	Transition Frequency	V_{CE} = 10 V,	I_C = 0.5 A	BUY69A	6			MHz
				BUY69B	6			MHz
				BUY69C	6			MHz
C_{obo}	Output Capacitance	V_{CB} = 20 V,	I_C = 0	BUY69A			150	pF
				BUY69B			150	pF
				BUY69C			150	pF

NOTES: 1. Pulse Width ≤ 500 μS, Duty Cycle ≤ 25 %.
3. Pulsed Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2 %.

DETAILS FOR THE MEASUREMENT OF SWITCHING PARAMETERS

R_{CC} Adjustable to give Collector Current
R_{BB} Adjustable to give Base Current
V_{CC} Constant at 40 Volts
Pulse Width 10 μs
Pulse Repetition Rate = 200 P.P.S.
All resistances are non-inductive types
Recommended Pulse generator Velonex type 380 using type V1265 plug in.
Recommended current probe Tektronix type P6019, P6020, or P6042.
Oscilloscope to have rise time better than 20 ns
R_{BB} R_{CC} and V_{BB} may be varied to obtain the correct test condition required.



FORWARD BIASED SAFE AREA OF OPERATION
(NON REPETITIVE OPERATION) $T_{j\,max}$ = 200 °C

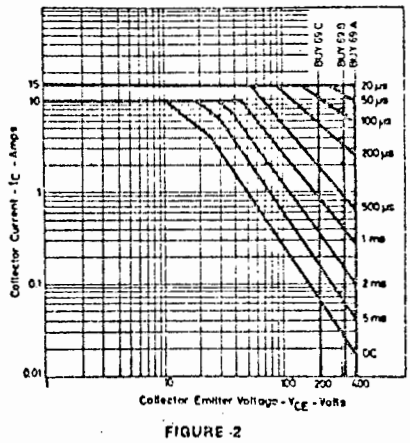


FIGURE 2

The graph of Forward biased Safe Area of operation is for single non-repetitive rectangular power pulses, with a case temperature held at 25 °C. For operation at case temperature above 25 °C derate the value of current indicated in Figure by the power derating factor, determined from the derating curve.
For repetitive pulse operation the following procedure should be followed. Work out the energy of the power pulse by graphical integration and determine the equivalent rectangular power pulse, using the pulse duration and the peak voltage applied. Ensure that the equivalent power pulse, as determined, is within the safe operating area, applying a derating factor for the case temperature as indicated from the derating curve.
Also calculate the average power dissipation and ensure that it falls within the steady state (DC) condition for the peak voltage applied, having first derated the steady state condition for the effect of case temperature.

TYPICAL VARIATION OF TRANSITION FREQUENCY
WITH COLLECTOR CURRENT

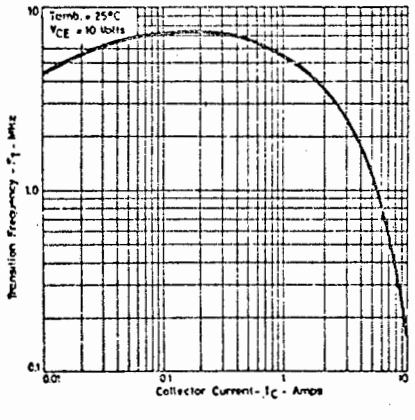


FIGURE 3

DISSIPATION DERATING CURVE

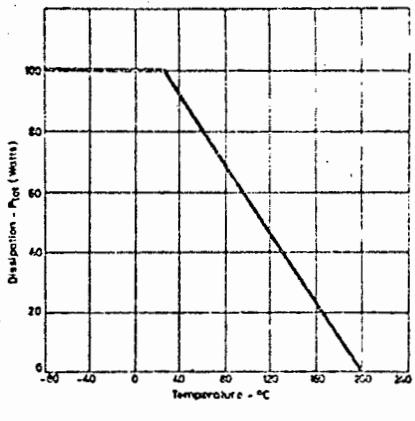


FIGURE 4

BUY69
NPN SILICON POWER TRANSISTOR

TYPICAL AND MAXIMUM VARIATION OF I_{CBO} WITH TEMPERATURE

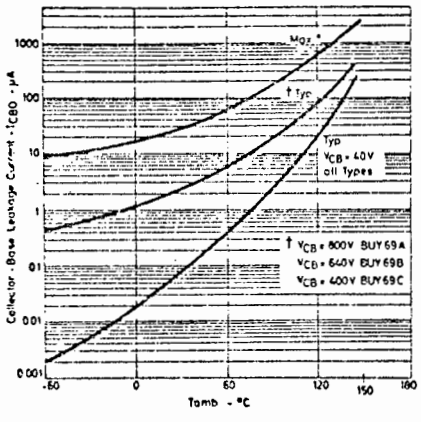


FIGURE 5

TYPICAL VARIATIONS OF BASE-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT

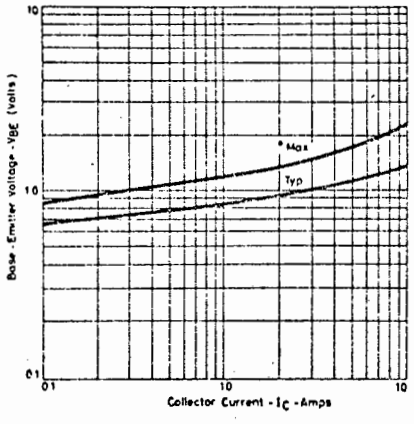


FIGURE 6

TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIOS WITH COLLECTOR CURRENT

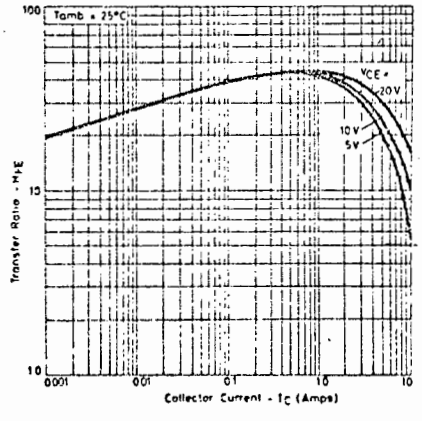


FIGURE 7

TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT

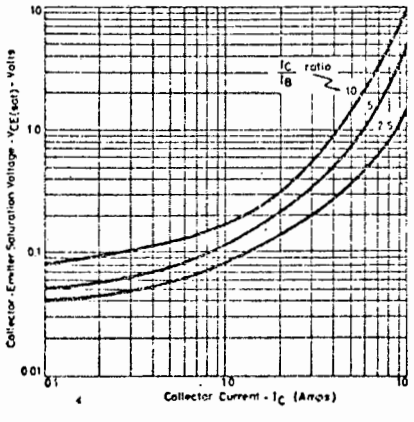


FIGURE 8

BUY69
NPN SILICON POWER TRANSISTOR

TYPICAL VARIATION OF STORAGE AND FALL TIMES WITH COLLECTOR CURRENT

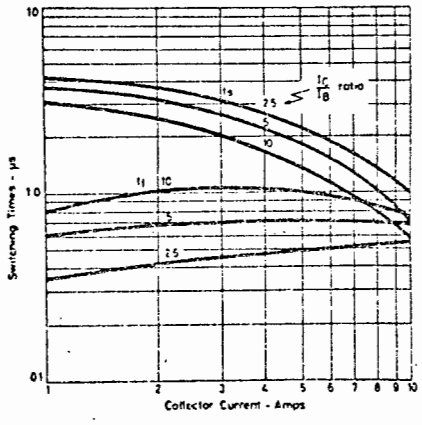


FIGURE 9

TYPICAL VARIATION OF DELAY AND RISE TIMES WITH COLLECTOR CURRENT

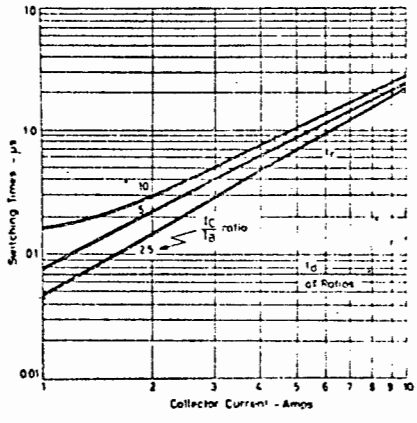


FIGURE 10

Monsanto

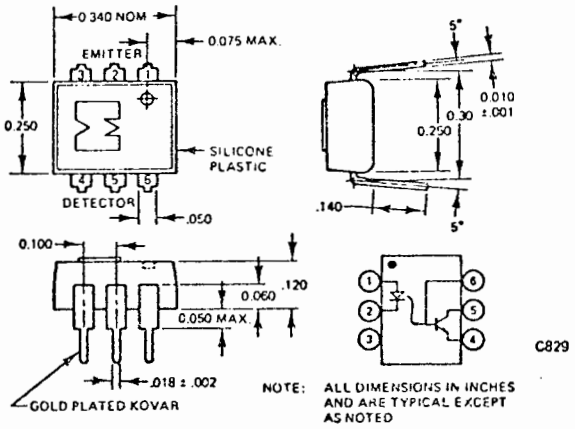
PHOTOTRANSISTOR OPTO-ISOLATOR

MCT26

PRODUCT DESCRIPTION

The MCT26 is a NPN silicon planar phototransistor coupled to a gallium arsenide diode. It is mounted in a six lead plastic DIP.

PACKAGE DIMENSIONS



NOTE: ALL DIMENSIONS IN INCHES AND ARE TYPICAL EXCEPT AS NOTED

APPLICATIONS

- AC line/digital logic isolator
- Digital logic/digital logic isolator
- Telephone/telegraph line receiver
- Twisted pair line receiver
- High frequency power supply feedback control
- Relay contact monitor
- Power supply monitor

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -55°C to 150°C
Operating temperature -55°C to 100°C
Lead temperature (Soldering, 10 sec) 260°C

Input Diode
- Forward DC current . . . . . 60 mA
- Reverse current . . . . . 10 μA
- Peak forward current (1 μs pulse, 300 pps) . . . . . 3.0 A
- Power dissipation at 25°C ambient . . . . 200 mW
- Derate linearly from 25°C . . . . . 2.6 mW/°C

Output Transistor
- Power Dissipation at 25°C ambient . . . . 200 mW
- Derate linearly from 25°C . . . . . 2.6 mW/°C

Input to output voltage . . . . . 1500 volts

Total package power dissipation at 25°C ambient (LED plus detector) . . . . 250 mW

Derate linearly from 25°C . . . . . 3.3 mW/°C

ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Emitter					
Forward voltage		1.25	1.5	V	I_F = 20 mA
Reverse current		.15	10	μA	V_R = 3.0 V
Capacitance		100		pF	V = 0
		300		pF	V = 1 V
Detector					
h_{FE}	100	150			V_{CE} = 5 V, I_C = 100 μA
BV_{CEO}	30	75		V	I_C = 1.0 mA, I_F = 0
BV_{ECO}	7	12		V	I_C = 100 μA, I_F = 0
I_{CEO}		5	100	nA	V_{CE} = 5 V, I_F = 0
Capacitance Collector-emitter		8		pF	V_{CE} = 0
BV_{CBO}	30	100		V	I_C = 10 μA
I_{CBO} (dark)		1	100	nA	V_{CB} = 5 V, I_F = 0
Coupled					
DC current transfer ratio	6	14		%	V_{CE} = 10 V, note 1
Breakdown voltage	1500	2500		VDC	
	300				VAC, RMS @ f = 60 Hz
Resistance emitter detector	10^{11}	10^{12}		Ω	V_{E-D} = 500 V
V_{CE} (sat)		0.2	0.3	V	I_C = 250 μA, I_F = 20 mA
		0.2	0.5	V	I_C = 1.6 mA, I_F = 60 mA
Capacitance LED to detector		1.0	2.0	pF	
Bandwidth (see figure 5)		300		kHz	I_C = 2 mA, note 2
Rise time and fall time (see operating characteristics)		2		μs	I_C = 2 mA, V_{CE} = 10 V, note 3

MCT26

TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES
(25°C Free Air Temperature Unless Otherwise Specified)

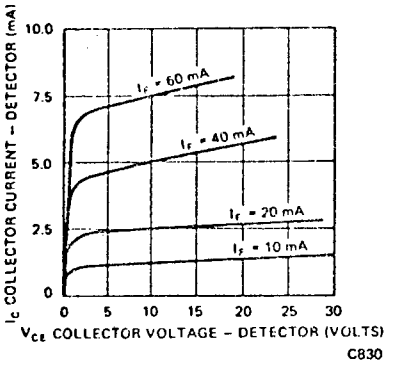


Fig. 1 Detector Output Characteristics

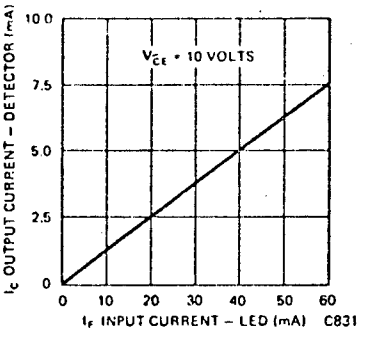


Fig. 2 Input Current vs. Output Current

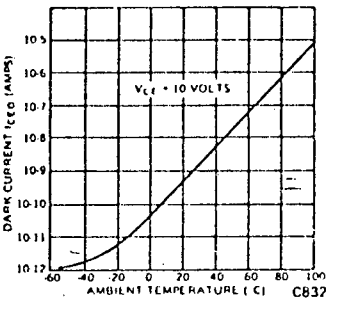


Fig. 3 Dark Current vs. Temperature (°C)

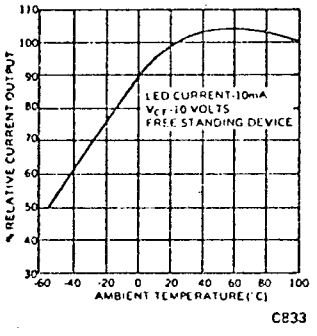


Fig. 4 Current Output vs. Temperature

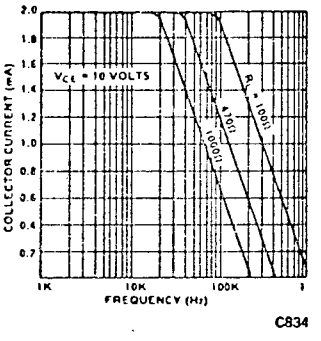


Fig. 5 Output vs. Frequency

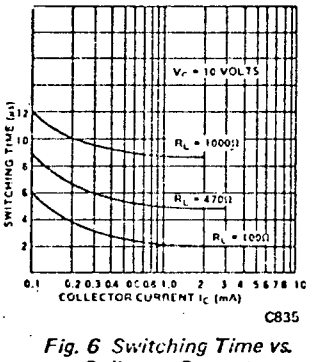


Fig. 6 Switching Time vs. Collector Current

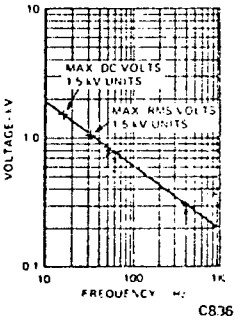
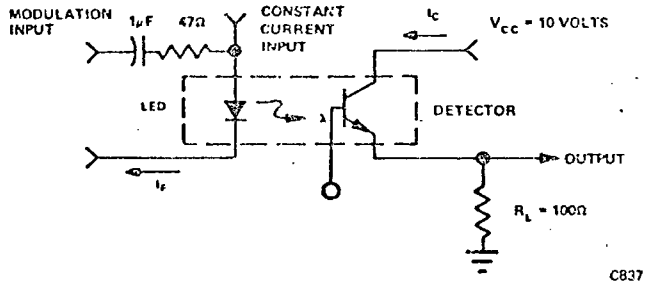


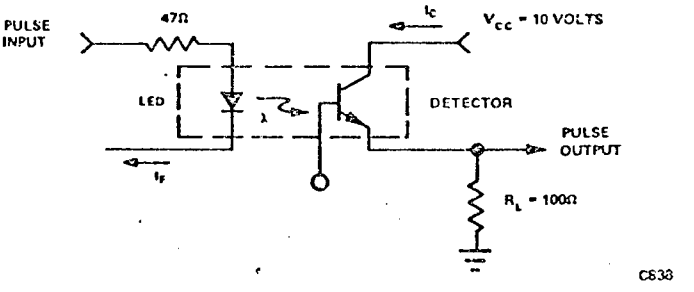
Fig. 7 Steady-State AC Voltage Limit of Isolation Dielectric

For additional characteristic curves, see figures 2, 3, 5, 6, 8, 11, 12, & 13 on MCT2.

OPERATING SCHEMATICS



Modulation Circuit Used to Obtain Output vs. Frequency Plot



Circuit Used to Obtain Switching Time vs. Collector Current Plot

NOTES

1. *The current transfer ratio (I_C/I_F) is the ratio of the detector collector current to the LED input current with V_{CE} at 10 volts.*
2. *The frequency at which i_c is 3 dB down from the 1 kHz value.*
3. *Rise time (t_r) is the time required for the collector current to increase from 10% of its final value to 90%. Fall time (t_f) is the time required for the collector current to decrease from 90% of its initial value to 10%.*

APPENDIX 6 THE BEHAVIOUR OF THE COMPLETE CIRCUIT AT TURN-ON

The complete response of any system may be resolved into the natural and forced responses . For a first-order L-R circuit :

$$L\frac{di}{dt} + iR = E_s \sin (\omega t + \phi)$$

The impedance functions are : $Z(s) = R + sL$

and : $Z(j\omega) = R + j\omega L$

The forced response is :

$$i_f = \frac{E_s}{Z(j\omega)} = \frac{E_s}{R + j\omega L}$$

$$= \frac{E_{smax}}{\sqrt{(R^2 + \omega^2 L^2)}} . \sin(\omega t + \phi - \tan^{-1} \frac{\omega L}{R})$$

The natural response is obtained by setting $Z(s) = 0$

Thus $s = - \frac{R}{L}$

Assuming an exponential form of solution ,

$$i_n = Ae^{-\frac{R}{L}t}$$

Taking the complete response as $i = i_f + i_n$,

at time $t = 0^+$, $i = 0$

Thus ,

$$0 = A(1) + \frac{E_{smax}}{\sqrt{(R^2 + L^2\omega^2)}} . \sin(\phi - \tan^{-1} \frac{\omega L}{R})$$

$$\text{Thus , } A = \frac{-E_{smax}}{\sqrt{(R^2 + \omega^2 L^2)}} . \sin(\phi - \tan^{-1} \frac{\omega L}{R})$$

Substituting this value yields equation 3.23

For the second-order R-L-C system ,

$$Z(s) = R + Ls + \frac{1}{sC}$$

The natural response has a solution of the form ,

$$s = Ae^{-\alpha t}\sin(\theta t + \beta)$$

where $\alpha = \frac{R}{2L}$ and $\theta = \sqrt{\left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)}$

The applied voltage at the instant of closing (t = O) is :

$$e = E_s\sin\phi$$

At time t = O , the current i_n = O , and at $t = O^+$, i_n = O , since there must be continuity of current , thus the voltage across the , V_c = O

Thus

$$L\frac{di}{dt} = E_s\sin\phi$$

or

$$\frac{di}{dt} = \frac{E_s\sin\phi}{L}$$

and

$$A\sin(\omega t + \beta) = O$$

A is finite ; thus β = O

$$\frac{di}{dt} = A\theta e^{-\alpha t}\cos\theta t - A\alpha e^{-\alpha t}\sin\theta t$$

Thus

$$\frac{E_s\sin\omega t}{L} = A\theta\cos(O) - A\alpha\sin(O)$$

and

$$A = \frac{E_s\sin\phi}{\theta L}$$

then

$$i_n = \frac{E_s\sin\phi}{\theta L} \cdot e^{-\alpha t}\sin\theta t$$

The forced response yields :

$$Z(j\omega) = R + \omega L + \frac{1}{\omega C}$$

and from this

$$i_f = \frac{E_s}{\sqrt{(R^2 + \{\frac{1}{\omega C} - \omega L\}^2)}} \cdot \sin(\omega t + \phi + \tan^{-1} \frac{\{\frac{1}{\omega C} - \omega L\}}{R})$$

Adding i_f and i_n above yields equation 3.25 .

Using the current notation of chapter 3 , the rigorous solution is :

$$(i_1 + i_2)R_s + sL_s(i_1 + i_2) + \frac{1}{sC}i_2 = E \qquad (1)$$

and $(i_1 + i_2)R_s + sL_s(i_1 + i_2) + R_L i_1 + sL_L i_1 = E \qquad (2)$

(1) - (2) :

$$\frac{1}{sC}i_2 - (R_L i_1 + sL_L i_1) = 0$$

or $i_2 = i_1 sC(R_L + sL_L)$

Subst. in (1) :

$$R_s(i_1 + i_1 sC(R_L + sL_L)) + (i_1 + i_1 sC(R_L + sL_L)sL_s + ...$$

$$..... + i_1(R_L + sL_L) = E$$

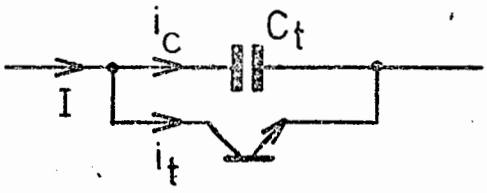
Setting Z(s) to zero ;

$$s^3 C_L L_L L_s + s^2 C_L L_s R_L + s^2 C_L L_L R_L + sC_L R_s R_L + sL_L + R_s + R_L = 0$$

Similarly a solution may be found around the i_2 loop .

APPENDIX 7 THE COMPLETE CIRCUIT BEHAVIOUR AT TURN-OFF

Stage 1 : Transistor turn-off :



I is constant . Thus

$$I = i_c + i_t$$

Voltage across capacitor $V_c = \frac{1}{C_t} \int_o^t i_c dt$

Capacitor current $i_c = I \frac{t}{T}$

where T = transistor turn-off time .

Thus :

$$V_c = \frac{I}{C_t T} \int t dt$$

$$= \frac{It^2}{2C_t T}$$

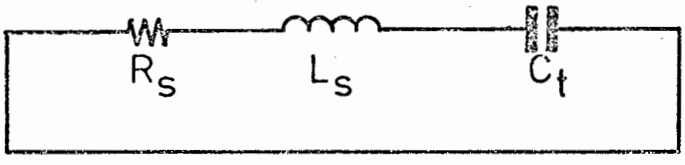
which reaches a maximum value $V_{cmax} = \frac{IT}{2C_t}$

when t = T

Stage 2 : t = T

Stage 3 : Final energy clearance :

The circuit is reduced to the following :



The solution for the current as a function of time is :

$$i(t) = Ae^{-\alpha t}\sin(\theta t + \phi)$$

and

$$\frac{di}{dt} = Ae^{-\alpha t}\theta\cos(\theta t + \phi) - Ae^{-\alpha t}\alpha\sin(\theta t + \phi)$$

At time $t = O^+$, i = I , the load current .

Thus $I = A\sin\phi$

and $L_s \frac{di}{dt} = V_c + IR_s$

thus : $\frac{di}{dt} = \frac{1}{L_s}(V_c + IR_s) = A\theta\cos\phi - A\alpha\sin\phi$

$= A\theta\cos\phi - I\alpha$

so that $A\cos\phi = \frac{1}{L_s\theta}(V_c + IR_s + L_s I\alpha)$

But $\alpha = \frac{R_s}{2L_s}$

Thus $A\cos\phi = \frac{1}{L_s\theta}(V_c + IR_s + \frac{IR_sL_s}{2L_s})$

$= \frac{1}{L_s\theta}(V_c + \frac{3IR_s}{2})$

and $\tan\phi = \frac{L_s\theta}{V_c + \frac{3IR_s}{2}}$

and $A = \frac{I}{\sin\phi} = \frac{I}{\sin\{\tan^{-1}\frac{\omega L}{V_c + \frac{3IR_s}{2}}\}}$

Equation 3.29 follows from the substitution of the above expressions .

APPENDIX 8 DESIGN DETAILS OF COMPLETE SYSTEM

A8.1 THE POWER TRANSISTOR SWITCH:

The circuit may be broken into 3 separate units. These are: The power transistor and its associated driver, the feedback circuit and the interface to the control pulse generator. Fig. 4.2 is reproduced here, with these elements identified.

The "snubber" circuit comprises C3, R12 and D6. Assuming a maximum load current of 10 A, a turn-off time of the power transistor of 3 μsecs and a maximum voltage rise of 150, we have

$$C_t = \frac{IT}{2V_{cmax}} = \frac{10 \times 3 \times 10^{-6}}{2 \times 150} = 0{,}1\ \mu F$$

During the turn-on time of the freewheel switch, 5 μsecs, the further voltage rise is

$$\Delta V = \frac{It}{C_t} = \frac{10 \times 5 \times 10^{-6}}{0{,}1 \times 10^{-6}} = 500\ V$$

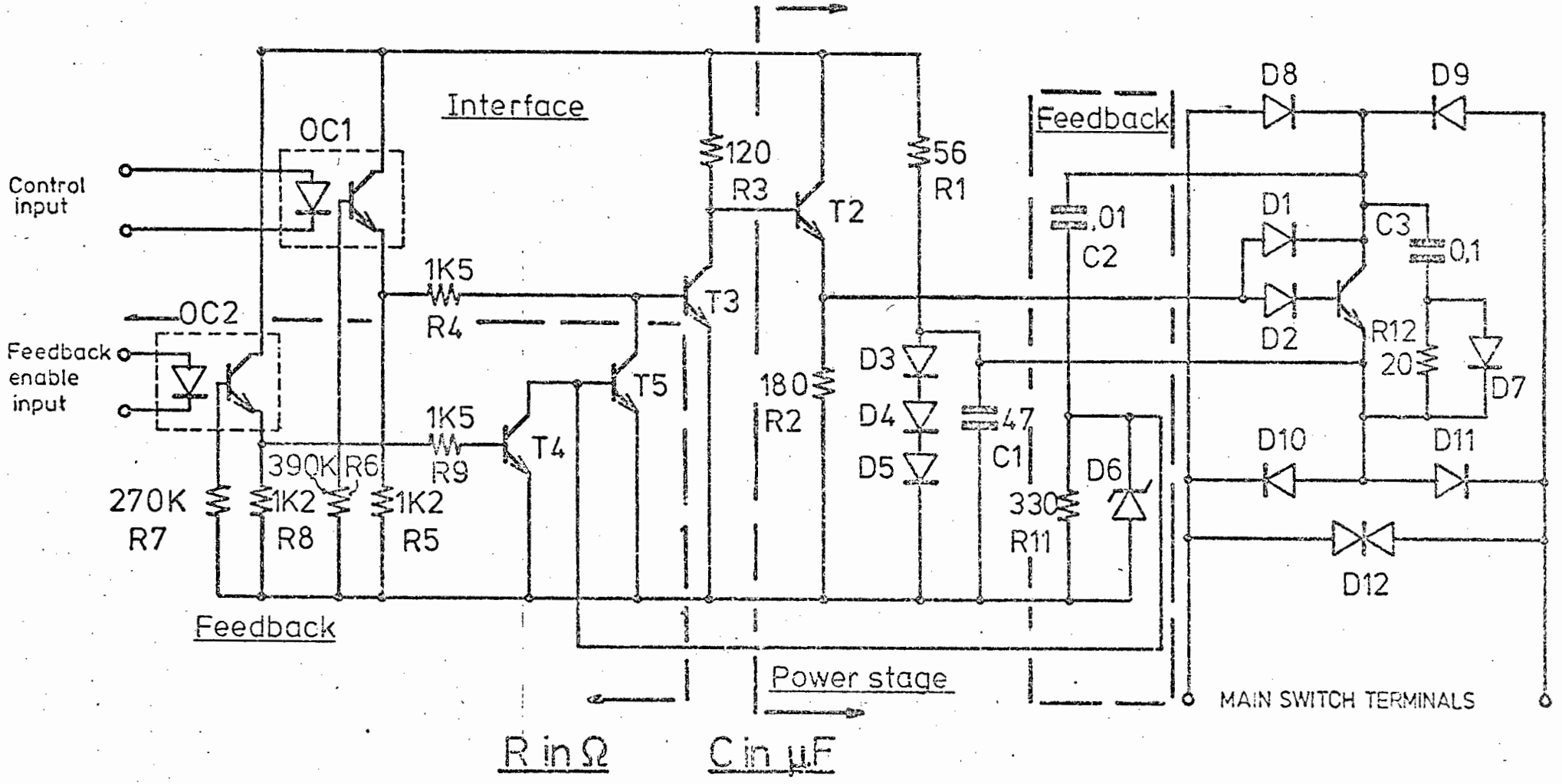
This is clamped at 300 V by the zener diode D5, which means that current flows in this diode for 3,5 μsecs (i.e. rate of rise of 100 V/μsec). This results in 30 m Joules being dissipated in the diode on each turn-off.

Assuming that the maximum voltage across the capacitor during the "off" period is 200, and that the surge current at turn-on is not allowed to exceed 10 A, then

$$R_{12} = \frac{V_{cmax}}{I} = 20\ \text{ohms}$$

If the load current normally does not exceed 5 A, then the maximum current through the power transistor would be

Fig. 4.2. Circuit of complete power switch



blowing the fuse. The operate time of the fuse is immaterial, since the rise time of the current in the thyristors is limited by lead inductance and must be kept below 50 A/μsec for the devices employed. If necessary, additional inductance is included in series with the thyristors to achieve this. Turn-on delay for the whole unit is 2μsecs. The use of a standard shunt, with its stray inductance, tends to assist the operation of the "crowbar" in the "fail-safe" direction, since the voltage surges produced by the shunt speed up the comparator operation.

Fig. A8.6 shows the circuit diagram of the comparator trigger unit. A 711 dual comparator is connected as a double limit comparator, with the trip level (usually 100 mV) provided by zener diode Z1 and potentiometer P1. The 741 operational amplifier serves to invert the voltage from P1, providing thus both comparator voltages. The output of the comparator gates the unijunction transistor T3 which is coupled through transistor T2 to a pulse transformer. The pulse transformer in turn triggers the thyristors. The capacitor C of the U.J.T. circuit is fully charged when the comparator trips, thus providing an immediate pulse at the detection of a fault.

The performance of the unit is shown in the oscillographs A8.7 and A8.8 . The former shows the load current with the "trip" point set at 5 amperes , while the latter shows supply current . The successful diversion of the current away from the load is very clear .

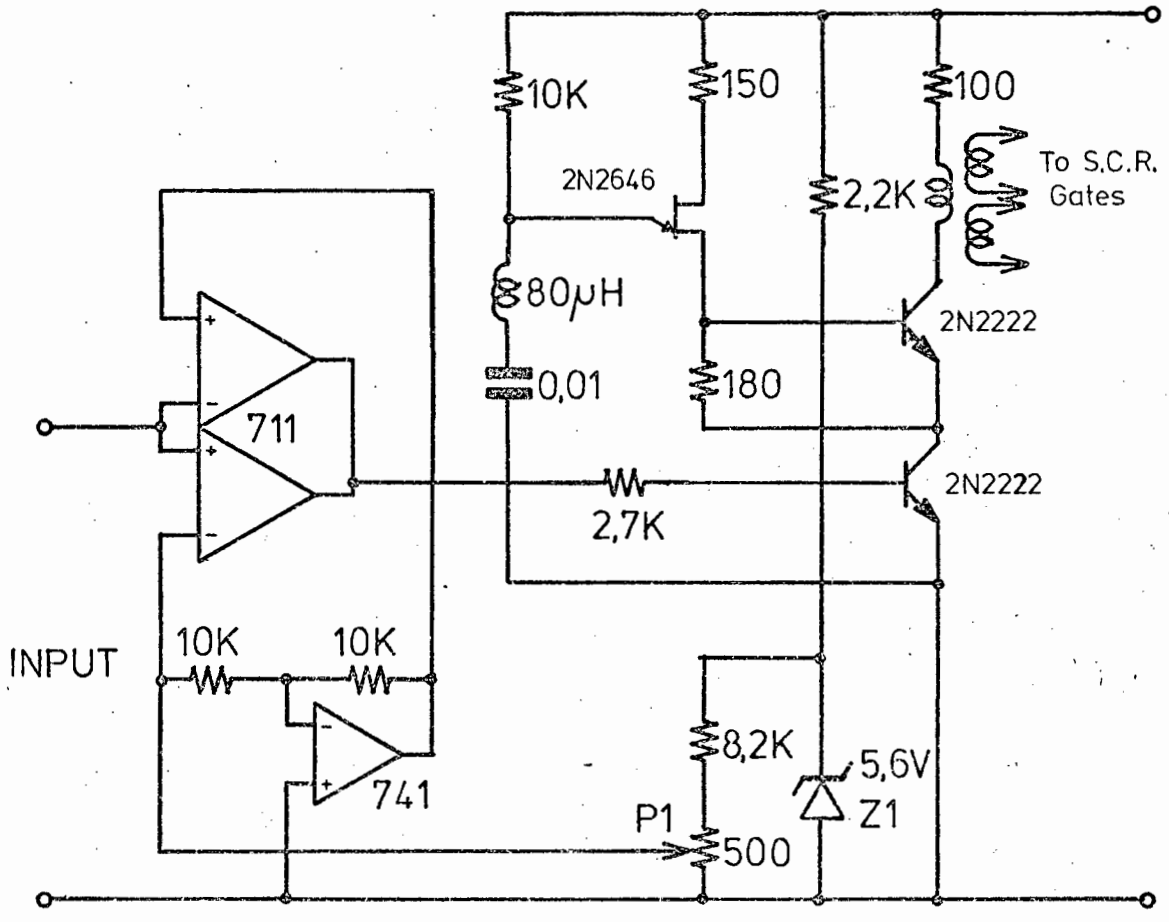


Fig. A8.6. Crowbar ; circuit diagram

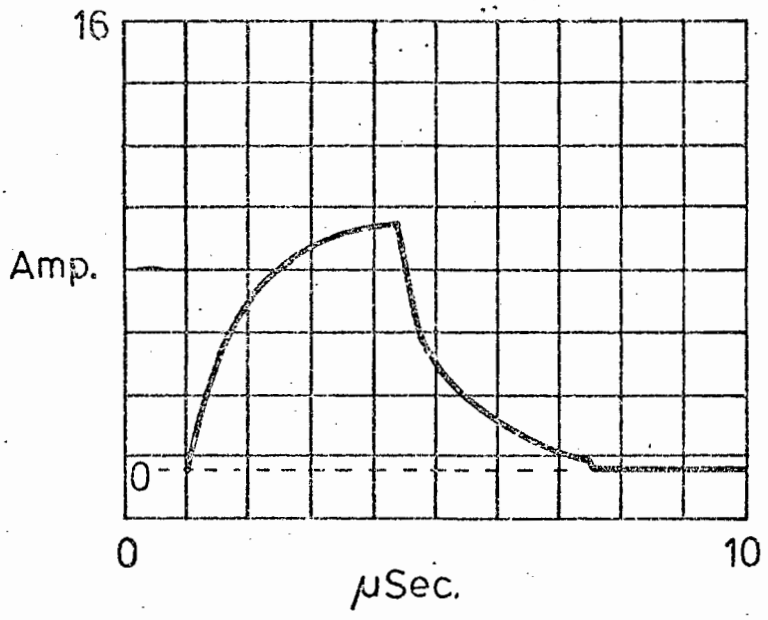


Fig. A8.7. Crowbar action ; load current . The trip point is 5 A

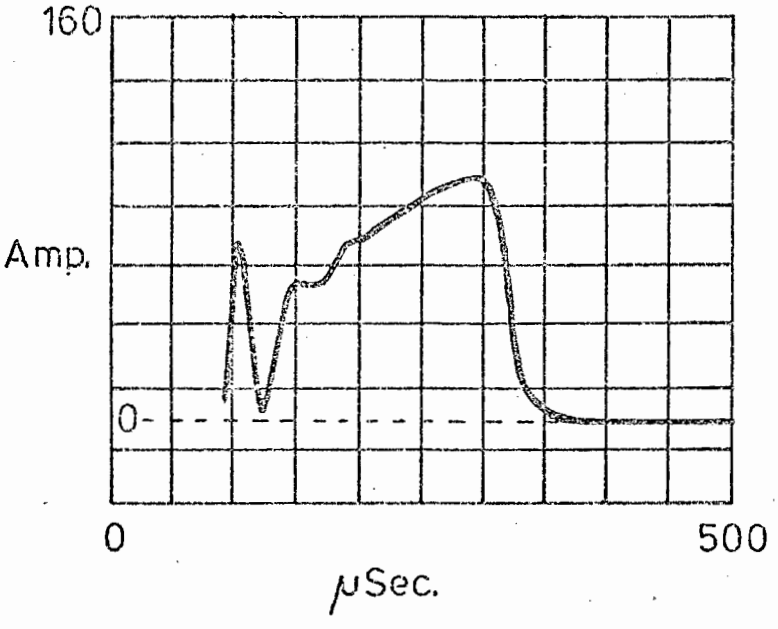


Fig. A8.8. Crowbar action ; supply current

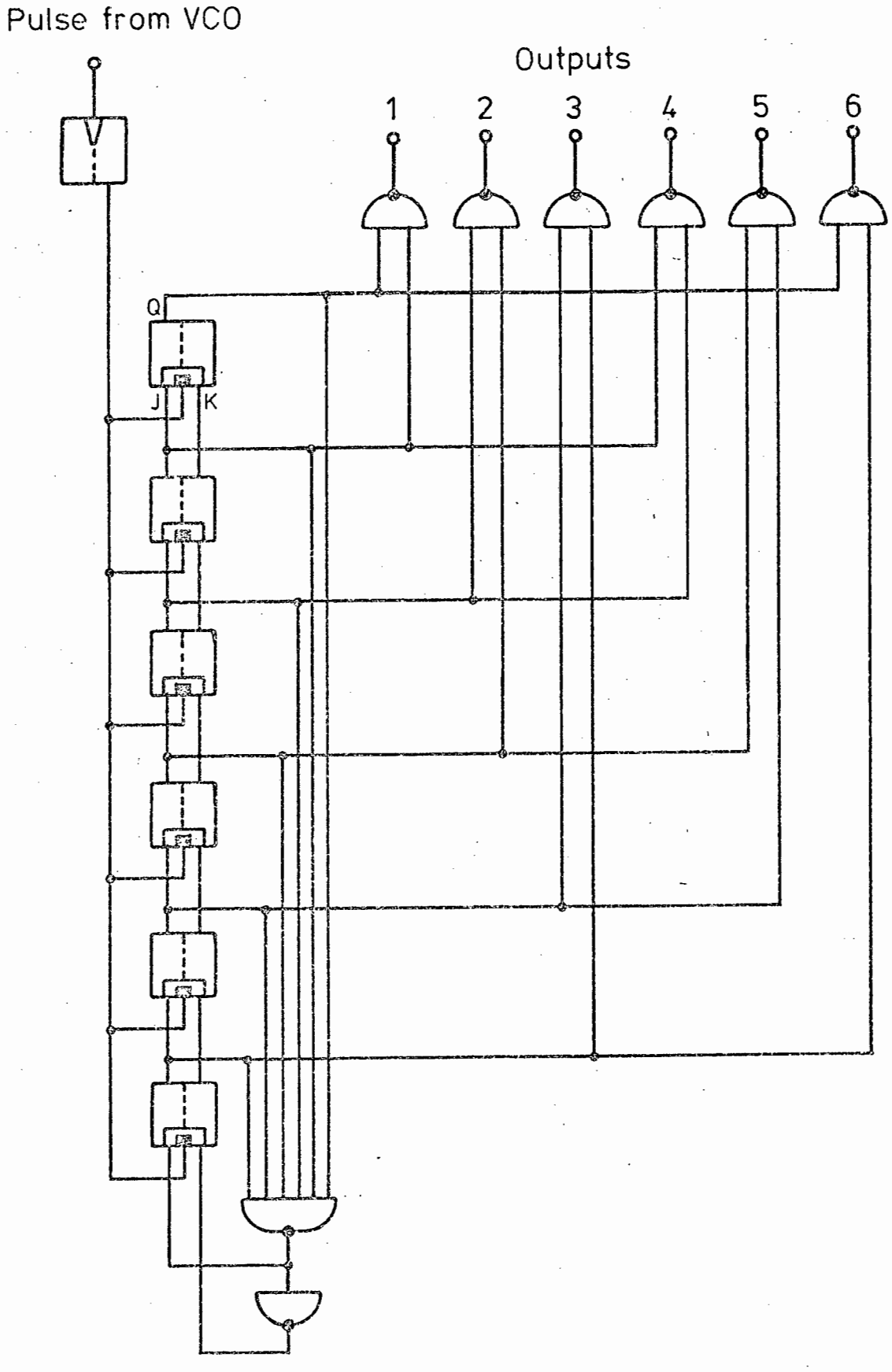


Fig. A8.3. Logic diagram ; gated ring counter

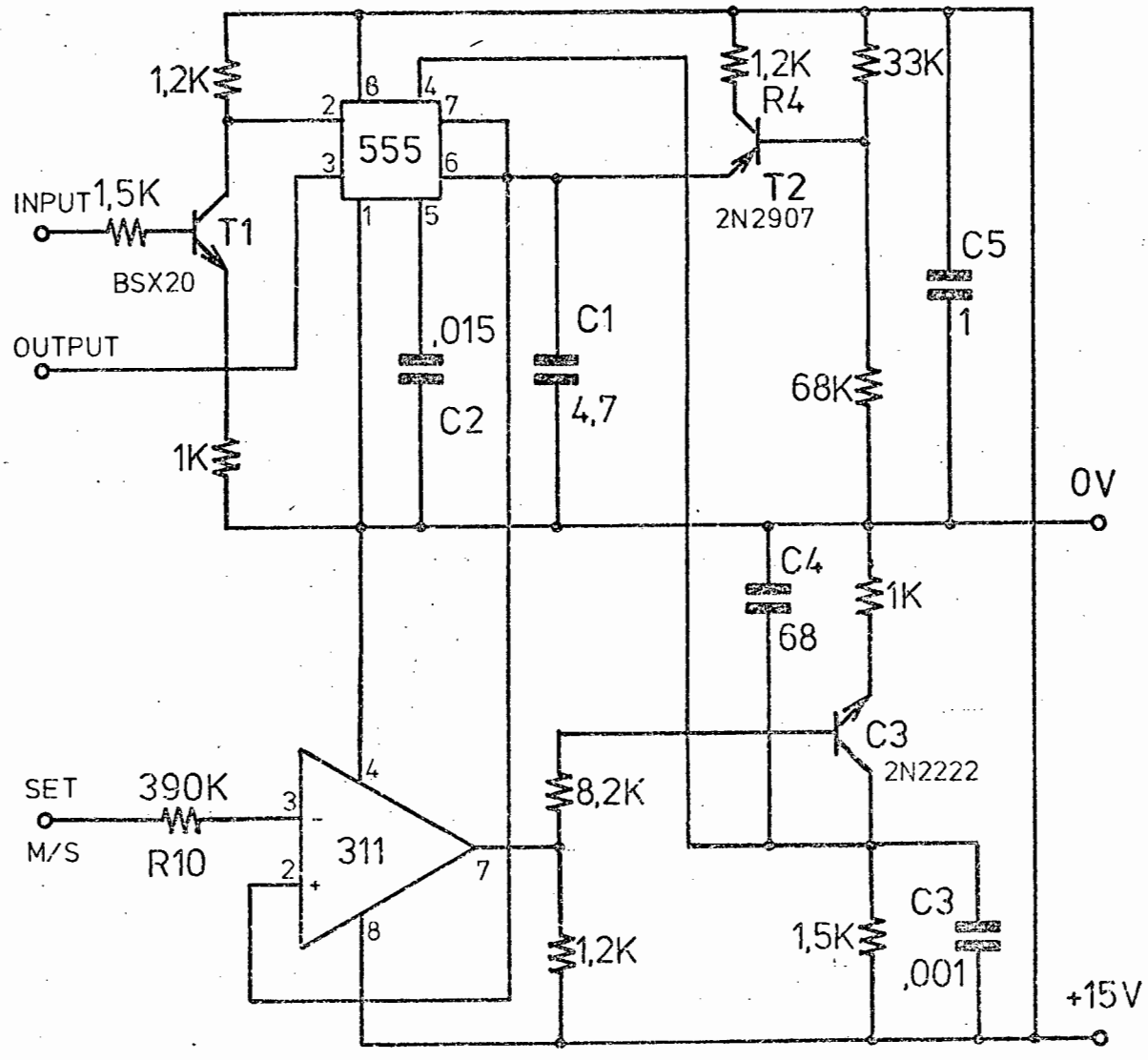


Fig. A8.4. Pulse width controller ; circuit diagram

across R4 and thus a constant current in T2.

T2 Base voltage $V_B = R_5V_{cc}/(R_5 + R_6) = 1,7$ Volts

T2 Emitter voltage $V_E = 1,7 - B_{be} = 1,0$ Volts

T2 Emitter current $= V_E / R_4 = 1,0 / 1200 = 0,8$ mA

The voltage across C1 then rises as a linear ramp, appearing at pins 6 and 7 of the 555 timer. This voltage is also applied to the positive input of the 311 comparator.

The pulse width control voltage is applied to the negative input of the comparator through isolating resistor R10. When the voltage across C1 exceeds the control voltage, the comparator trips. The output of the comparator is level-shifted by transistor T3 and applied to the "reset" terminal of the timer. Capacitor C is then discharged and the process starts again.

Capacitors C3 and C4 bypass the reset line, to avoid spurious oscillations of the comparator, while capacitor C5 decouples the power supply for the same reason.

A simple solution to varying the duty cycle is to apply the control voltage direct to pin 5 of the 555 timer. This permits control over a limited range, insufficient for the wide range of variation considered necessary in the prototype.

A8.5 THE CURRENT PROTECTION ("CROWBAR") UNIT:

The basic system is shown in fig. A8.5. When the voltage drop across the shunt (a standard 100 mV instrument unit) exceeds the trip level of the comparator, both thyristors are triggered and the current is diverted to neutral,

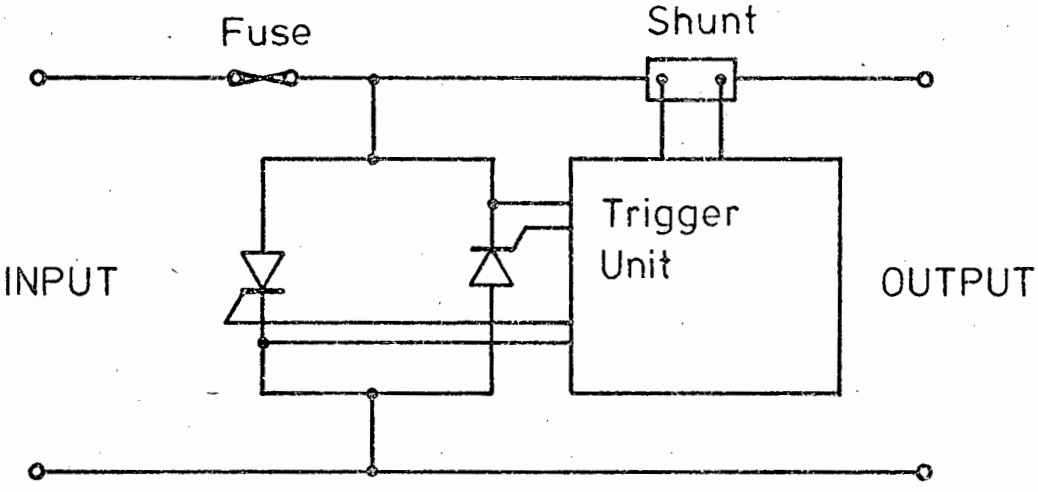


Fig.A8.5. Crowbar ; block diagram

15 A, which is within the maximum rated pulse current. Duration of this current is the time constant of $R_{12}C_3$, of 2 μ secs.

The power transistor T1 is driven by emitter-follower transistor T2, with diodes D1 and D2 providing a Baker clamp anti-saturation circuit. The diode D1 must have a reverse voltage rating at least equal to the maximum forward blocking voltage which T1 has to withstand. The maximum reverse voltage applied to D2 is the reverse base-emitter bias of T1, some 1,5 volts. The current ratings of both diodes should equal the maximum base current. The diodes selected were type MR826, being of 600 V, 6 A rating. The turn-off time of these diodes is 0,2μsec, which is short enough not to add materially to the turn-off time of T1. The reverse bias to the base during turn-off is provided by resistor R1 and diodes D3 - D5. Resistor R2 provides the return path for this potential. The diodes D3 - D5 are type IN4001 operating with a steady current of 230 mA supplied by R1. Capacitor C1 acts as a charge store.

Transistor T2, a type BD124, acts as an emitter-follower driver for T1. From available data, the current gain of 3 A is typically 40. Taking the voltage drop along the path base-emitter T2 - D2, base-emitter T1 - D3 - D4 - D5 as 4,7 volts (values of base-emitter drops from Appendix 5), we have

Base current of T2 = = 75 mA

Thus R3 = = 150,6 ohms

A preferred value resistor of 120 ohms was used to overcome any spread in transistor characteristics.

The feedback circuit is coupled to the power circuit via capacitor C2 which, with resistor R11 and transistor T5, together form the type of configuration shown in fig. 13.14(b). The base-emitter voltage of T5 functions as a crude comparator. The zener diode D5 serves to limit the maximum voltage available and R10 limits the base current. Transistor T4 is the feedback enable element. When T4 is hard on, T5 is inhibited and no feedback signal is able to activate the switch.

The maximum rate of rise of voltage across the power transistor is determined by C3, the "snubber" capacitor, and is, if the load current reaches a maximum of 10 A, 50 V/μsec (from equation 3.27). The feedback voltage is

$$e_{fb} = R_{11}C_2\frac{dv}{dt}$$

and $R_{11}C_2$ should be tailored to obtain a feedback voltage of say 5 volts at the lowest rate of rise of voltage. If it is assumed that a voltage rise of 5 during the turn-off period, followed by a further rise of 18 volts during the freewheel turn-on, is not likely to cause any damage, then

$$I_{min} = \frac{2C_tV_{cmax}}{T} = 0,3 \text{ A}$$

Thus the feedback circuit is not expected to operate at load currents below 0,3 A. The rate of rise of voltage is 1,6 V/μsec.

Thus

If $C_2 = 0,01$ μF

Then $R_{11} = 310\ \Omega$ or nearest preferred value 330 .

The maximum feedback voltage, at say 10 A load current, is

$$e_{fb} = 330 \times 0,01 \times 50 \times 10^{-6} \times 10^{6} = 165 \text{ Volts}$$

which is clamped by D5.

Isolation for the driver stage is provided by opto-coupler OC1, a type MCT26, connected as an emitter-follower with R5 as load and R6 providing a return path to ground for the base current. The photo-transistor does not go into saturation in this connection and then operates with a fall time of 2,6 sec. (See data, Appendix 5.) The transistor T3, a 2N2219, controls the base of T2. (The nett result of this amplifier chain is the control signals are inverted. That is, an input to OC1 turns T1 off and vice versa.) Resistor R4 limits the base current supplied to R3.

Base drive voltage = R5 X I_{oc1} and

R5 = 1,2 KΩ ; I_{oc1} = 2 mA

Base drive voltage = 2,4 volts

$$R4 = \frac{2,4 - V_{be}}{I_b} = \frac{1,7}{I_b} \text{ Ohms}$$

If the base current of T3 is limited to 1 mA, then

R4 = 1700 ohms.

The preferred value of 1500 ohms was chosen.

The feedback circuit is enabled through opto-coupler OC2. R7, R8 and R9 are derived from similar considerations as R4, R5 and R6. Transistor T5, under control of T4 and the feedback signal, diverts base current from T3 to turn it off and hence turn T1 on.

A simple power supply rated at 15 volts and 5 amps drives the circuit.

The heat-sinking arrangements for the power transistor are based on equation 3.28. The various parameters are at worst-case values:

V_{MAX} = 400 Volts

V_{MIN} = 3,3 Volts

I_{MAX} = 5,0 Amperes

I_{MIN} = 1,0 mA

t_s = 25 secs

T = 1 millisec (That is, an operating frequency of 1 FHz, maximum.)

t_{on} = 0,8 millisec (At 1 6Hz)

t_{off} = 0,2 millisec (At 1 6Hz)

Then $$P = \frac{(400X5X25X10^{-6}) + (3X3,3X5XO,8X10^{-3}) + (3X400X1X10^{-3}X..}{(3X1X10^{-3})} \quad \frac{..XO,2X10^{-3})}{}$$

= 29.9 Watts.

Which is well within the maximum allowable dissipation of the transistor (100 W).

The transistor operates in a pulsed mode, but since the duty cycle range is likely to be very large, a worst-case is postulated where the maximum duty cycle is 80%, and no allowance is made for the fact that this may very often be lower for most of the transistor operating cycle.

The thermal resistance from junction to case is not stated in the manufacturer's specifications for the BUY69, but since this device is contained in a TO3 package, it may be assumed that this is 3 ^{o}C/W. The maximum temperature rise of the junction above that of the case is then

T_{jc} = 3,0 X 29,9 ≒ 90 ^{o}C

The insulator between heat sink and transistor is mica; using a silicon heat sink grease the thermal resistance from heat sink to transistor is then 0,40 ^{o}C/W.

The total thermal resistance from junction to heat sink is then

$$\theta_{js} = 3,0 + 0,40 = 3,4 \ ^{o}C/W$$

The temperature rise of the junction above the heat sink is then

$$T_{js} = 3,4 \times 29,9 \div 102 \ ^{o}C$$

If the maximum temperature of the junction is set at 180°C, the maximum temperature rise of the heat sink above ambient is then

$$T_{sa} = 180 - 102 = 78 \ ^{o}C$$

This means that the thermal resistance of the heat sink to air must be:

$$\theta_{s} = \frac{78,0}{29,9} = 2,6 \ ^{o}C/W$$

From the available data, this is provided by 100 mm of the aluminium extrusion available.

A maximum case temperature rise of 78°C results in a dissipation derating to 70 watts; this leaves a comfortable margin over the 30 watts needed to be dissipated. (Fig. 4 of Appendix 5.)

No allowance is made for the fact that the thermal capacity of the heatsink allows for transient overloads; the transistor does not permit such overloads.

A8.2 VOLTAGE-CONTROLLED OSCILLATOR:

The voltage-controlled oscillator is in essence a unijunction transistor relaxation oscillator with voltage-controlled current supply to the capacitor. Fig. A8.1 shows a block diagram of the system. Referring to this diagram for the nomenclature, we have that the capacitor C is charged during the time T to reach the stand-off voltage V_s of the U.J.T. which triggers and discharges C.

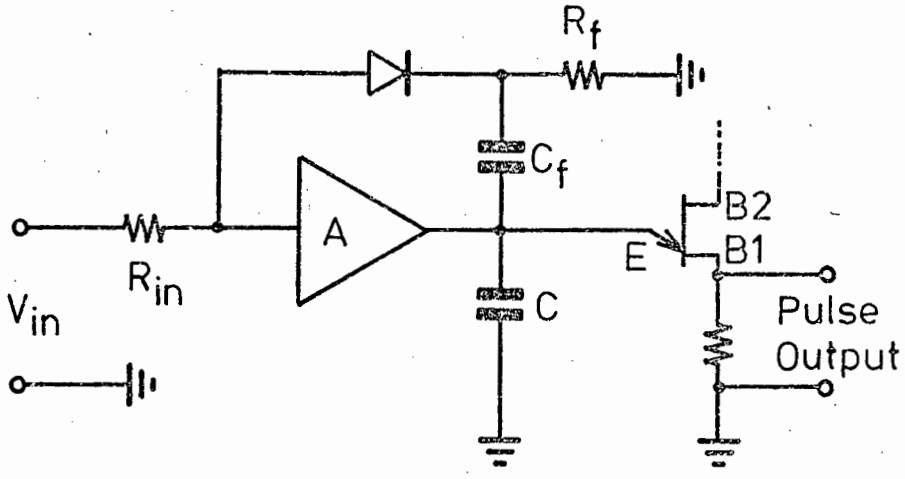


Fig. A8.1. Block diagram of V.C.O.

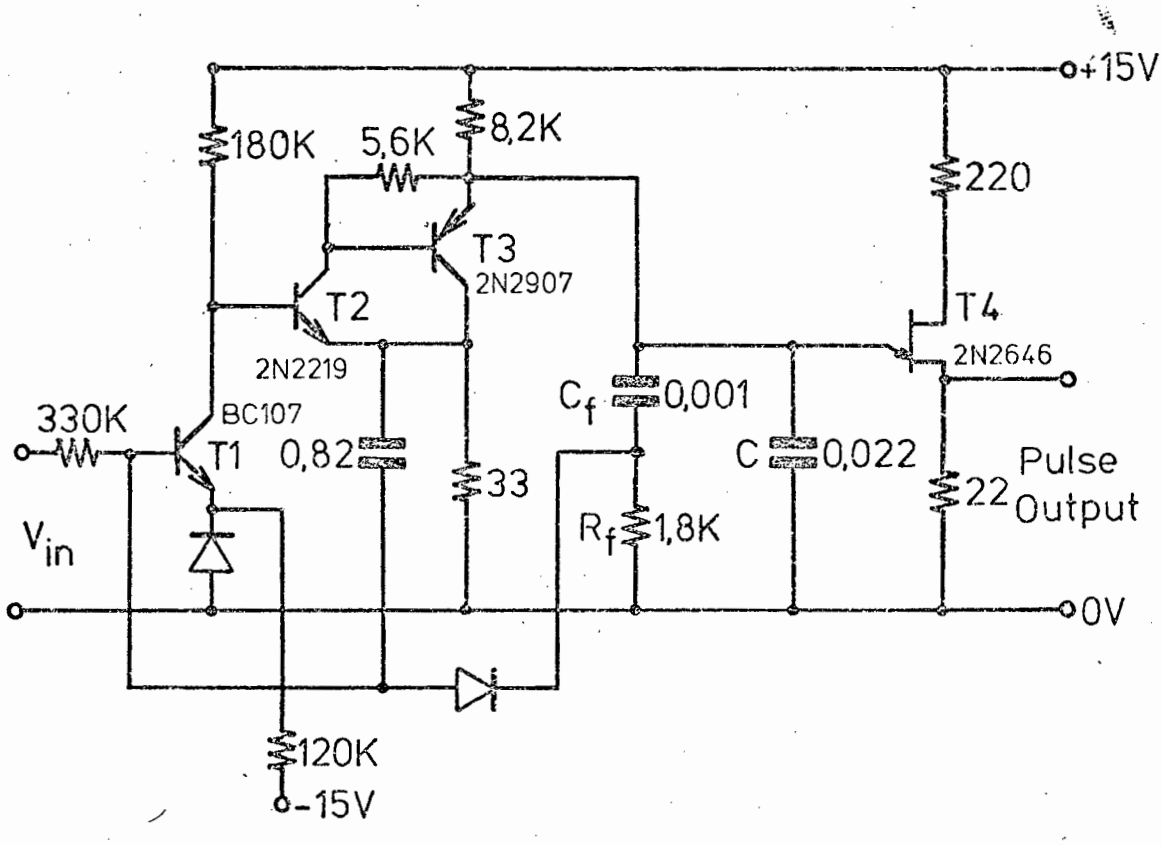


Fig. A8.2. Complete circuit diagram of V.C.O.

The voltage developed across the B1 resistance is the pulse output. Then:

$$e_{fb} = R_f C_f \frac{d}{dt} e_{out}$$

but $$e_{out} = \frac{1}{C} \int_0^T I_{out}\, dt$$

or $$\frac{d}{dt} e_{out} = \frac{I_{out}}{C}$$

$$= \frac{V_s}{T}$$

thus $$e_{fb} = R_f C_f \frac{V_s}{T}$$

If A is very large,

$$I_{in} = I_f = \frac{e_{fb}}{R_f}$$

$$= \frac{V_{in}}{R_{in}}$$

Thus

$$\frac{R_f C_f V_f}{T \cdot R_f} = \frac{V_{in}}{R_{in}}$$

or $$T = \frac{R_{in} C_f V_s}{V_{in}}$$

or Pulse repetition frequency $$= \frac{1}{T} = \frac{V_{in}}{R_{in} C_f V_s}$$

i.e. a linear function of frequency.

The unijunction transistor chosen is a type 2N2646 with an intrinsic stand-off voltage of 7; with the values of R_{IN} and C_f chosen for the final circuit, shown in fig. A8.2, an input voltage range of 0,7 to 1,4 gives a frequency range of 300 Hz to 600 Hz.

The amplifier portion comprises transistors T1, T2 and T3. The only noteworthy part of this circuit is the use of the IN914 diode and 120 KΩ resistor connected to a -15 volt supply, which balances out the base-emitter voltage drop of T1. This enables the input voltage to go to zero if necessary.

It might be added that voltage-controlled oscillators are available at present in integrated circuit form; when the work commenced on the prototype these were excessively

expensive and thus the design and construction of the unit mentioned above was embarked upon.

A8.3 GATED RING COUNTER:

The gated ring counter, fig. A8.3, comprises a synchronous counter using J-K bistables which is reset on the sixth count through a 6-input NAND gate. The outputs are decoded through 2-input NAND gates to give the waveforms of fig. 4.4. A monostable multivibrator triggered by the V.C.O. provides the clock pulses for the counter.

Although the number of components could have been reduced by using either a ripple-through binary counter or a shift register with decoding, both of these configurations introduce the possibility of a spurious pulse entering the count. An additional pulse in the sequence would have disastrous consequences for the system, causing a short-circuit between supply phases.

A8.4 PULSE WIDTH CONTROLLER:

The pulse width controller varies the ratio between the shunt and series switch conduction times, independently of the frequency. The circuit diagram is shown in fig. A8.4.

The 555 timer is triggered from the V.C.O. through the pulse amplifier BSX20 transistor T1. This stage is required to provide the pulse polarity inversion required to trigger the 555.

Transistor T2, a 2N2907, provides a constant current to the 4,7 F capacitor C1. The base of T2 is kept at a constant voltage, thus maintaining a constant voltage