UNIVERSITY OF CAPE TOWN

Design and Implementation of a Single Phase Active Power Filter

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Terms of Reference

This thesis was commissioned and supervised by Dr. Michel Malengret of the Electrical Engineering Department at the University of Cape Town. This document is an outline of the design and implementation of a single phase shunt active power filter (APF). Dr. Malengret's requirements were:

- Research into existing APF topologies and different theories used in their design and implementation.
- Design and build an APF which is based on injecting compensation current using a power electronics inverter.
- Build and test a laboratory prototype.
- Finally, to draw conclusions and make recommendations for future developments.

Declaration

This section gives a breakdown of the work that has been done in the respective chapters of this document. It serves to give a brief description of what each section consists of:

Chapter 1 gives an introduction and overview to the subject of APFs and their control. It also gives the objectives, scope, APF topology, the limitations of this project and the plan of development.

Chapter 2 gives a literature review on APFs, instantaneous power theory and ends with a review on control strategies used in APFs.

Chapter 3 gives the theoretical aspects of the selected shunt APF topology and also gives the mathematical expressions used to derive the compensation current and the control algorithms.

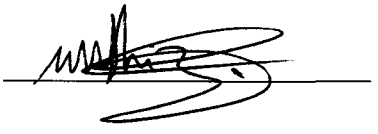
Chapter 4 outlines the simulations done. The designs were done using PSpice Schematics, version 9.2 by Cadence Design Systems, Inc. Other simulations were also done using Matlab, Simulink package from Mathworks. Matlab simulations were done to verify the validity of the simulations in Spice. Therefore they are not discussed at length in this chapter but can be found in appendix D for reference.

Chapter 5 describes how the simulations are implemented in hardware. The equipment used to implement the hardware and software to build the laboratory prototype is described.

Chapter 6 presents the results obtained in simulation as well a from the laboratory experiment. A case study is conducted where the experimental results are compared to the simulation results. The simulations results form the benchmark of the discussion.

Finally, chapter 7 succinctly draws conclusions based on the results obtained in chapter 6 and recommendations are also drawn from the conclusions.

I know the meaning of plagiarism and declare that all the work in the document, save for that which is properly acknowledged, is my own.

Signature:  **Date:** 1 September 2010

Abstract

Various active filter solutions have been proposed in recent years [1], [2], and are still being widely investigated today. This thesis discusses the design and implementation of the shunt APF topology. The thesis starts with a general literature review of various APFs which includes voltage control and current control topologies for single phase and three phase configurations. In particular, the single phase shunt APF was focused on.

Secondly, the theoretical aspects of the shunt APF topology are discussed. The methodology of the APF consists of measuring the load current and extracting the harmonic components using the sine-multiplication theorem. Then the extracted current is used as the reference current to be injected by the single phase full-bridge static converter. The control method used is based on a predictive control approach.

Thirdly, the APF theory is verified by simulation and through construction of a laboratory prototype. A case study was conducted in which the simulation results are compared with the laboratory prototype results. The experimental results show that the active filter, together with feed-forward control technique can effectively reduce harmonics. The application of the APF resulted in the source current harmonics being reduced from 42% total harmonic distortion (THD) to a desired allowable level of less than 5% THD in simulation. The practical results obtained were 8.5% but could however be improved with further work in order to meet the IEEE 519-1992 standard.

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Glossary

ABM: Analogue behavioural model

APF: Active Power Filter

AC: Alternating Current

ADC: Analogue-to-digital converter

APF: Active Power Filter

CPU: Central Processing Unit

DAC: Digital to Analogue Converter

DC: Direct Current

DSP: Digital Signal Processor

FFT: Fast Fourier Transform

GTO: Gate-turn-off Thyristor

HVDC: High Voltage Direct Current

IGBT: Insulated Gate Bipolar Transistor

kW: Kilo Watts

LEM: Transducers modules

LPF: Low Pass Filter

MW: Mega Watts

MVA: Mega Vars

PCC: Point of Common Connection

PI: Proportional Integral Controller

PLL: Phase Locked Loop

S/H: Sample and Hold

PWM: Pulse Width Modulation

RMS: Root Mean Square

STATCOM: Static Synchronous Compensator

UPS: Uninterruptible Power Supply

HVDC: High Voltage Direct Current

HVAC: High Voltage Alternating Current

1. Introduction

1.1 Background

There has been a significant increase in the use of power electronics in industry and in consumer applications in recent years. This has consequently lead to increased effort from the utilities to meet the quality of supply required. The problem is exacerbated by the increased use of so-called non-linear loads – most of which are power electronics devices. The following problems can result from increased use of such loads:

- Harmonic overloads.
- Untimely tripping of protection devices (which contribute to down-time).
- Considerable levels of high voltage and current distortion.
- Temperature rise in conductors, generators, transformers and motors.

All of these factors result in the reduction of AC mains power quality. Recent studies have shown that the use of non-linear loads will increase significantly in the future [3]. This will consequently increase the need for effective mitigation of harmonics. The conventional application of tuned passive filters can create system resonances which are dependent on specific system conditions. In addition to that, passive filters often need to be significantly overrated to account for possible harmonic absorption from the power system [4].

Passive filter ratings must take into account reactive power requirements of the loads and this makes it more difficult to design the filters to avoid leading power factor operation for some load conditions. APFs have the advantage of being able to compensate for harmonics without fundamental frequency reactive power concerns,

which means that the rating of the active power can be less than a comparable passive filter for the same non-linear load. Furthermore, the active filter will not introduce system resonances that can move a harmonic problem from one frequency to another [4]. Generally, shunt APFs works as a current source connected in parallel with the non-linear load and generating the harmonics that the load requires.

The APF consists of power electronic components which consist of capacitors, inductances and semiconductor switches that introduce current or voltage components, which cancel the harmonic components caused by nonlinear loads. Many different active power filter topologies have been introduced and already commercially available. APFs are very effective not only for harmonic compensation but can also have other benefits and applications – all in one unit. With an appropriate control strategy, it is possible to correct power factor, correct unbalanced loads and compensate for reactive power [5]. Much work has been done in the development of theory for determining compensation currents. However, there has not been a significant focus on their control [6-9]. Today, the wide-spread use of IGBTs and the implementation on digital signal processors (DSPs) has paved the way for the future success of APFs.

1.2 Problem description

To design an active filter that will attenuate harmonics to an acceptable level so as to comply with international standards such as the IEEE 519 and CEI 1000 standards. The subsystems of the filter must be designed, built and tested. These subsystems include an inverter, voltage and current transducers and laboratory set-up of the system.

1.3 Thesis Objectives

The objective of this thesis is to design, build and test a single phase shunt APF. In order to do so, the following tasks need to be completed:

1. Study the literature on APFs, their topologies and their implementation.
2. Study literature on various control theories and strategies and compare their various merits.
3. Design, build and test the subsystems forming the APF which can compensate a 3kW load with a maximum of 45% THD.
4. Draw conclusions and make recommendations for future work.

1.4 Shunt Current Controlled APF topology

The schematic diagram of the APF topology is shown in figure 1-2. The filter consists of three major parts; the compensator which computes compensation currents to be injected, a controller which is implemented on DSP to produce PWM and the full-bridge inverter. The validity of this topology is demonstrated by means of simulations and experimental results as shown in chapters 4 and chapter 6 respectively.

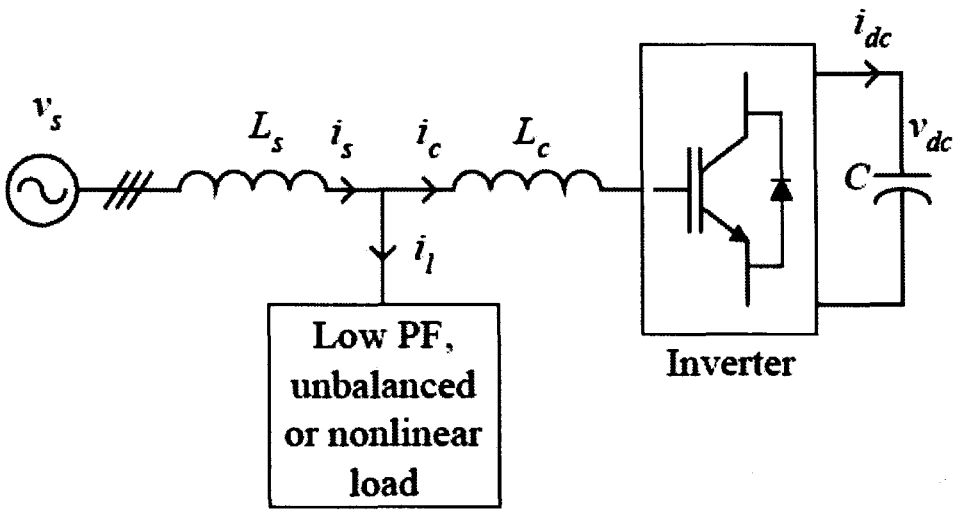

Figure 1-2 Schematic diagram of the single phase shunt APF topology [51]

2. Literature Review

2.1 Review of existing filter topologies

2.1.1 Introduction

The development of active filters began in the 1970s [10]. The APF has been developing technically over the years in order to meet larger power demands with increasing efficiencies. Initially, APFs were used to reduce irregularities in AC utilities in small capacities [11]. Nowadays, APFs can reach powers around mega watts, allowing them to be used in power distribution systems and in power transmission lines. In [10], Akagi affirms that in 1995 more than 300 shunt APFs with PWM control were in operation in Japan. These APFs used IGBTs and GTOs and had ratings ranging from 50 KVA to 50 MVA.

Active filters are designed to meet a number of compensation objectives. These objectives are typically unbalance, "flicker", reactive power compensation and harmonic compensation. The combination of all these compensation schemes in one compensator is often called a "universal power compensator," [11].

2.2 Harmonic mitigation approaches

Harmonic distortion in power systems can be suppressed through three basic approaches:

- Passive filtering.
- Active filtering and,
- Hybrid active power filters.

The following sections discuss general properties of the various approaches. Furthermore, the advantages, disadvantages and limitations of these approaches are discussed.

2.2.1 Traditional passive filters overview

Passive filters consisting of a bank of tuned LC filters such as high pass filters are widely used to suppress harmonics. They are the conventional solution to harmonic distortion problems. Passive filters use reactive storage components, namely capacitors and inductors. The more commonly used passive filters configurations are the shunt-tuned LC filters, the shunt low pass LC filter and the single-tuned "notch" filter which is the most common and economical type of passive filter which is used today [13], [14], [15]. The notch filter is usually connected in parallel with the power distribution system and is series-tuned to present a low impedance path to a particular harmonic current component. Some of the other more commonly used passive filter configurations are shown in figure 2-1.

2.2.1.1 Advantages and disadvantages of Passive Filters

Amongst other advantages, passive filters are simpler to implement, reliable, efficient and less costly [16]. However, while passive filters are widely used, there are some disadvantages associated with their use. The disadvantages are the resonances introduced into the AC supply, low filter effectiveness and the tuning issues [17]. Most of these disadvantages can be surmounted with the use of active power filters.

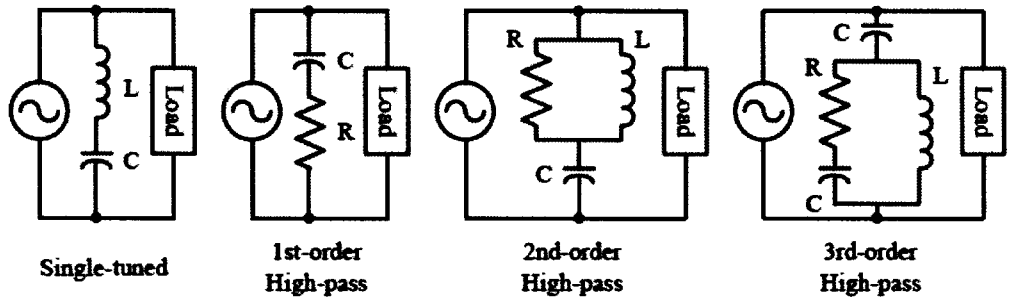

Figure 2-1 Commonly used passive filter configurations [43]

2.3 Active filter overview

Due to the shortcomings of shunt passive filters [18], APFs have been studied and developed in recent years [19], [20]. Most active power filter topologies use voltage source inverters. This topology converts a DC voltage into an AC voltage by appropriately gating the power semiconductor switches. A typical DC to AC converter is shown in figure 2-2. It consists of a DC source which is represented by a large capacitor; and six IGBT switches.

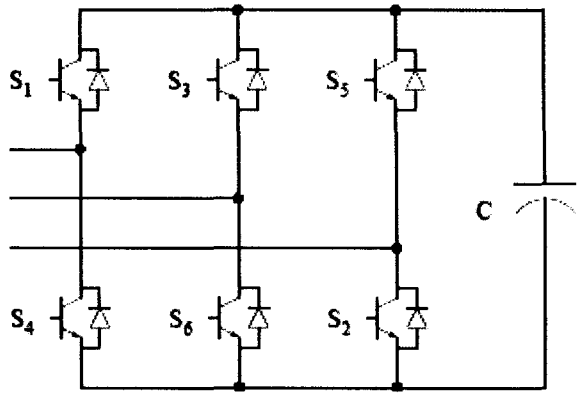

Figure 2-2 Three phase voltage source inverter

Although a single pulse for each half cycle can be applied to synthesize an AC voltage; for most applications requiring dynamic performance, pulse width modulation (PWM) is most commonly employed to control the inverter [16]. There are a large number of PWM techniques available to synthesize sinusoidal patterns, or any arbitrary pattern [12]. A simple PWM technique which compares a triangular

waveform carrier, (which defines the switching frequency); with the appropriate signal is shown in figure 2-3. The signal is compared with a high frequency triangular waveform to produce PWM pulses used to switch the semi-conductor switches of the converter.

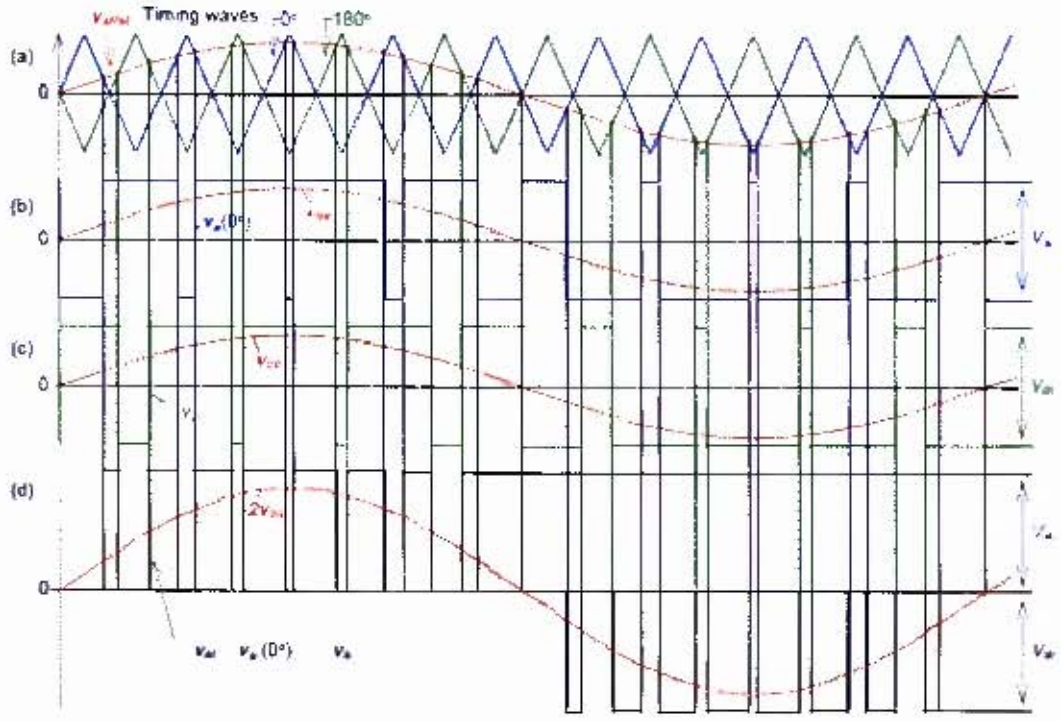

Figure 2-3 Synthesis of output voltage using triangular carrier [49]

With PWM, the AC output of the converter can be controlled as a current or voltage source device. The resulting output voltages consist of a sinusoidal fundamental at 50 Hz and some unwanted harmonic components due to high frequency switching. The unwanted components can be removed by using a low pass filter (LPF) at the output of the inverter. This is easily accomplished since high switching frequencies are typically used - ranging from 5-20 kHz. The maximum switching frequency does however depend on the maximum switching frequency of the semiconductors used [16], i.e., (IGBTs, GTOs or IGCTs).

The idea of APFs or harmonic conditioners is relatively old. It is however believed that the slow development of the APF was due to the lack of effective implementation

techniques at a competitive cost. Nowadays, with the wide spread use of IGBTs, and the availability of DSP technology; APFs have evolved rapidly and paved a path for their future success [3]. Converter based solutions to power quality problems surely seem to be the way of the future. In 1996, more than 100 converter based shunt harmonic compensators were operating in Japan [19]. However, even with the availability of IGBTs and DSPs, the cost of APFs is still relatively high [5], and they are difficult to implement in large scale.

One way of improving their practical utilization is to design the filter for only a fraction of the total load power. This can be done by designing a combined system of shunt passive filters and series APFs. This has an effect of largely reducing cost and results in increased overall system efficiency [22]. Combined systems of power APFs and shunt passive filters to reduce initial costs and improve efficiency are currently under investigation. The greatest advantage of implementing this synergy is the decrease in the required power rating of the converter and this is what primarily brings down initial costs [17].

Depending on the particular application or load to be compensated, APFs can be implemented as shunt type, series type or a combination of shunt and series APF. These filters can also be combined with passive filters to form hybrid power filters. The above-mentioned topologies will now be discussed in detail in the following sections.

2.3.1 Shunt Active power filters

The shunt active power filter permits to compensate for harmonics and asymmetries of the mains currents caused by nonlinear loads [23]. The shunt connected APF has a topology that is similar to that of a static var compensator (STATCOM) used for reactive power compensation in power transmission systems [16]. Shunt APFs compensate load current harmonics by injecting equal but opposite harmonic currents at the point of common connection (PCC) with the power distribution system. Thus, the shunt APF acts as a current source injecting the harmonic components required by the load but phase shifted by 180°. The result is that the source only has to supply the fundamental current required by the load. The concept of a shunt APF is shown more clearly in figure 2-4 below.

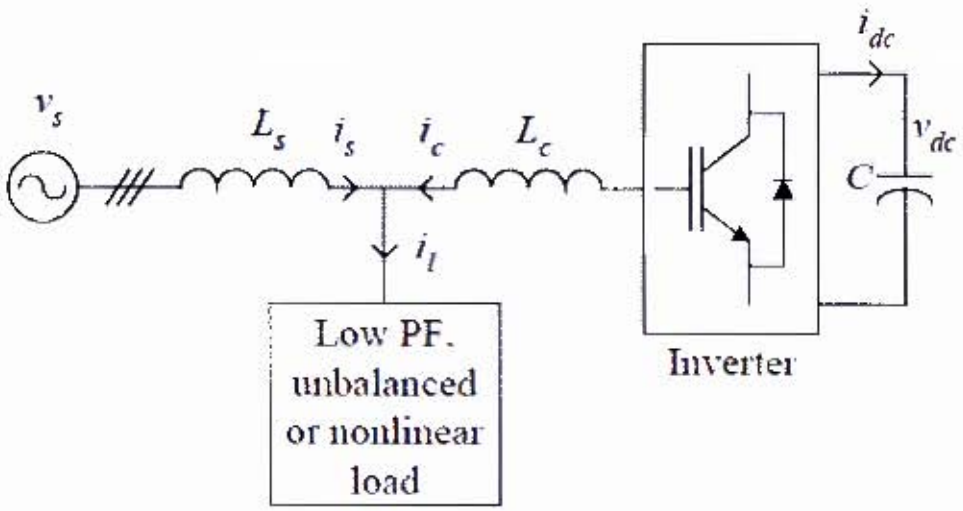

Figure 2-4 APF power circuit [51]

From the diagram above if the FFT of the load i_l is taken, it can be the deduced that:

$$i_l = I_{Fundamental} + I_{harmonics} \quad (2.6)$$

But: $i_C = i_{harmonics}$; and $i_S = i_{Fundamental}$, (2.7)

Therefore: $i_l = i_S + i_C$ (2.8)

Thus, from Kirchhoff's current law, it can be easily deduced that the two currents add up at the PCC to make up the total load current. Then the shunt APF must supply the rest of the harmonic current components required by the non-linear load.

Currently existing shunt APFs have the ability to compensate for the entire low frequency harmonic spectrum up to the 50th harmonic or more. They are also rated in such a way that if the harmonic currents drawn by the load are greater than the rating of the active filter, the filter automatically limits its output current to its maximum rating thus avoiding an over-load situation [3]. A typical shunt active power filter from Group Schneider named ACCuSine™ is shown in figure 2-5 [4] and has the following characteristics:

Figure 2-5 Group Schneider active filter product [4]

- Active harmonic filtration.
- Filters up to the 50th harmonic.
- Power factor correction.
- Dynamic VAR compensation.

- Filters entire network or specific loads depending on installation point.
- Response to load fluctuations begins in 40 micro seconds with 8 Milliseconds for full response to step load changes.
- IGBT based power electronic technology.

Figure 2-6 to figure 2-8 shows the results of ACCUSINE as recorded at Group Schneider laboratory, (taken from a presentation by Group Schneider at ***Driving performance in 2008*** power quality conference). Figure 2-6 is the load current that is drawn by a non-linear load (AC-DC converter), without ACCUSINE compensation. Figure 2-7 shows the current waveform injected by ACCUSINE. Figure 2-8 shows the corrected current waveform supplied by the source to the non-linear load.

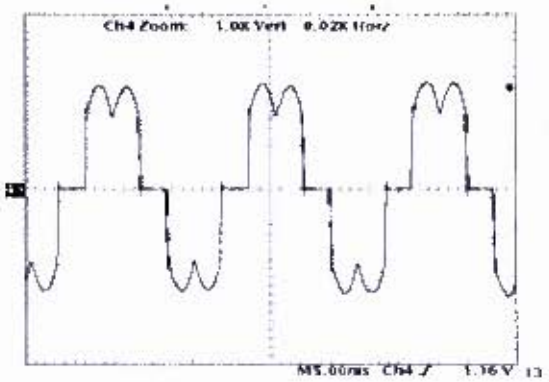

Figure 2-6 Load current [4]

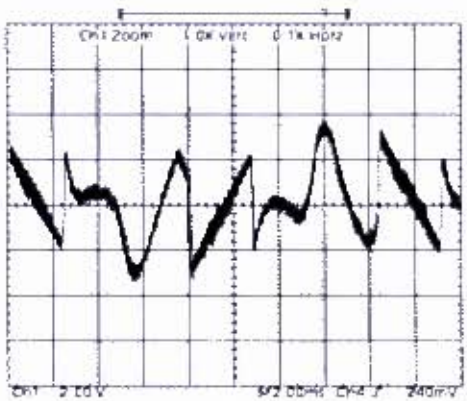

Figure 2-7 Current injected by Accusine™ [4]

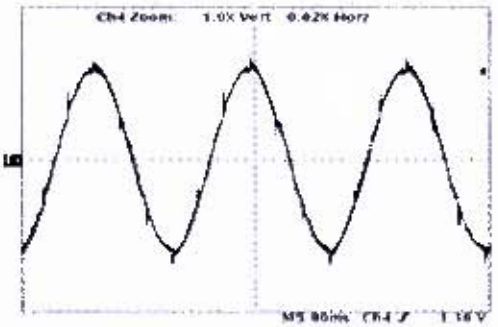

Figure 2-8 Source current after injection [4]

The performance of the filter is depicted in table 2.1 below in terms of the improvement in total harmonic distortion (THD) of the source current.

Table 2.1: Performance of ACCUSINE APF

Perfomance of Accusine		
	APF Off	APF On
Harmonic Order	% Ifund	% Ifund
1	100	100
3	0.038	0.478
5	31.660	0.674
7	11.480	0.679
9	0.435	0.297
11	7.068	0.710
13	4.267	0.521
15	0.367	0.052
17	3.438	0.464
19	2.904	0.639
21	0.284	0.263
23	2.042	0.409
25	2.177	0.489
27	0.293	0.170
29	1.238	0.397
31	1.740	0.243
33	0.261	0.325
35	0.800	0.279
37	1.420	0.815
39	0.282	0.240
41	0.588	0.120
43	1.281	0.337
45	0.259	0.347
47	0.427	0.769
49	1.348	0.590
% THD	35.280	2.670

The active filter topology presented above will be used as a benchmark against which the performance of the APF developed in this thesis will be measured.

2.3.2 Series APFs

Series active power filters were introduced towards the end of the 1980s [16]. They normally operate as voltage regulators and as harmonic isolators between the non-linear load and the utility system instead of generators of harmonics as is the case in shunt APF. This topology is especially recommended for compensation of voltage unbalances, voltage sags and for low power applications [8]. The topology also presents an economically attractive alternative to UPS since it can be designed to perform UPS functionality and harmonics isolation in a single unit [16]. In this approach, the evaluation of reference voltages as opposed to reference currents is required. Therefore, the control strategy used also differs. This is often very complicated since control has to be achieved through a precise measurement of line currents and voltage waveforms [5]. A series active filter configuration is shown figure 2-9.

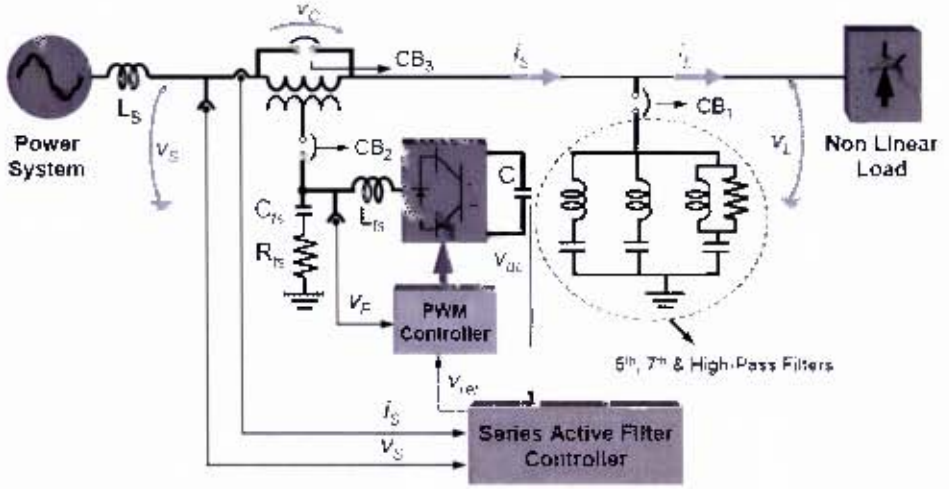

Figure 2-9 Series Active Filter [8]

In many cases, series active filters work as hybrid topologies with shunt passive filters networks. The shunt passive filter is connected in parallel with the load and tuned to eliminate odd harmonics to presents a low impedance path for the rest of the load current harmonics [22]. The passive LC filters may also be connected as in figure 2-9 when the series active filter operates as a harmonic isolator. The filter forces the

load harmonics to circulate mainly through the passive filter rather than the power distribution system [16]. The main advantages of this scheme are that the rated power of the series APF is a small fraction of the total load's kVA rating, typically 5%. However, the power rating of the series active filter may increase significantly in the case where the filter acts as a voltage compensator [16].

2.3.3 Series-shunt APFs

As the name suggests, series-shunt APFs consist of a combination of a series APF and the shunt APF components. The shunt APF is usually located at the load side and can be used to compensate for load harmonics. The series APF is then located at the source side and blocks harmonics from the load; compensates for supply voltage harmonics and voltage unbalances and damps power system oscillations. This topology is often called the Unified Power Flow Conditioner (UPFC) [55]. A schematic of the conditioner is shown in figure 2-10.

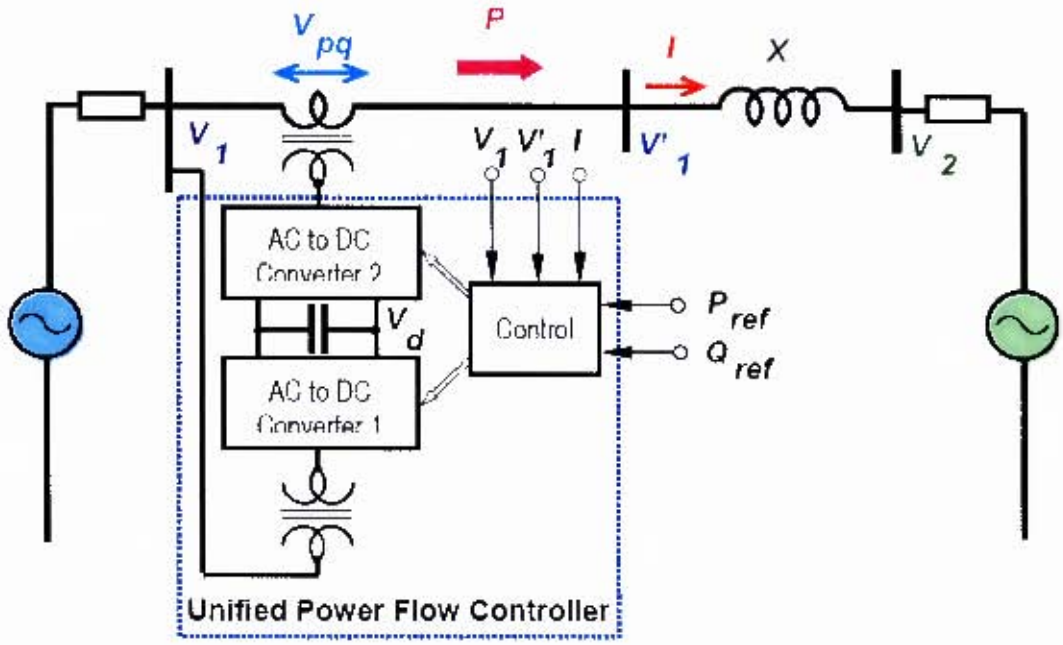

Figure 2-10 Unified Power Flow Conditioner [49]

The UPFC, by its multifunctional capacity can with adequate rating; directly force the line current to assume an angle and magnitude with respect to a given bus voltage to deliver the desired active power and simultaneously minimize the reactive power flow in the line. In other words, the UPFC has the functional capability of directly and independently controlling the active and reactive power flow in a power distribution line [49].

2.3.4 Summary of APF topologies

A summary of active filter topologies is shown in Table 2.2. Table 2.2 tabulates the advantages and disadvantages of using each type of topology discussed above. As can be seen from the table, it is clear that the shunt active filter does not introduce additional problems when connected to the AC grid; such as voltage sag/swell, voltage unbalance, voltage distortion, voltage interruption, voltage flicker and voltage notching as is the case with the series active filter and the shunt-series active filters.

Table 2.2: Summary of APF topologies [25]

ActiveFilter Connection	**Load Effect on AC Supply (Advantages)**	**Effect of Filter on the power-distribution System (Disadvantages)**
Shunt:	▪ Current Harmonic Filtering ▪ Reactive Current Compensation ▪ Current unbalance ▪ Voltage Flicker	
Series:	▪ Current Harmonic Filtering ▪ Reactive Current Compensation ▪ Current Unbalance ▪ Voltage Flicker ▪ Voltage Unbalance	▪ Voltage sag/swell ▪ Voltage Unbalance ▪ Voltage Distortion ▪ Voltage Interruption ▪ Voltage Flicker ▪ Voltage Notching
Series-Shunt	▪ Current Harmonic Filtering ▪ Reactive Current Compensation ▪ Current Unbalance ▪ Voltage Flicker ▪ Voltage Unbalance	▪ Voltage sag/swell ▪ Voltage Unbalance ▪ Voltage Distortion ▪ Voltage Interruption ▪ Voltage Flicker ▪ Voltage Notching

2.4 Reference signal estimation techniques

A number of methods can be applied to extract harmonic components to be used as reference signals for the active filter [24], [25], [26–29]. The reference signal estimation is initiated through the detection of essential voltage and or current signals in order to gather accurate system variable information. Typically, the voltage variables to be detected are the AC source voltage and the DC-bus voltage of the APF inverter. Typical current variables are load current, AC source current and the actual compensation current flowing across link inductor of APF. Based on these system variable feedbacks, reference current/voltage estimation is executed either in time or frequency domain. Figure 2-11 shows some of the reference signal estimation techniques which are widely used in literature.

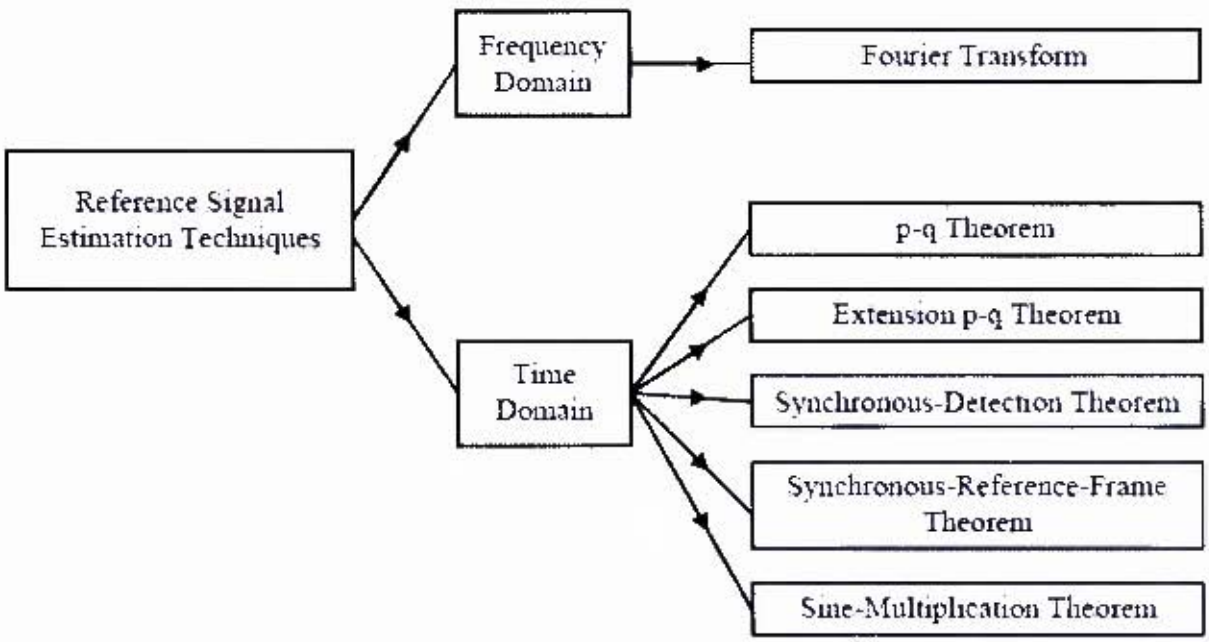

Figure 2-11 Reference signal estimation techniques [43]

2.4.1 Frequency domain approaches

Reference signal estimation in the frequency domain is suitable for both single and three phase systems. This method is fundamentally derived from the principle of Fourier analysis as follows:

2.4.1.1 Fourier analysis technique

The frequency-domain approach implies the use of the Fourier transform and its analysis which leads to complex mathematical calculations thereby making the control method non-ideal. Fourier transform, (either conventional or Fast Fourier Transform (FFT)), is applied to the captured voltage or current signal. Typically, the fundamental component of the load current is eliminated - thus separating the harmonic components form the fundamental as shown in figure 2-12. Inverse Fourier transform is then applied to estimate the compensation reference signal in the time domain [24], [25], [30], [26-29].

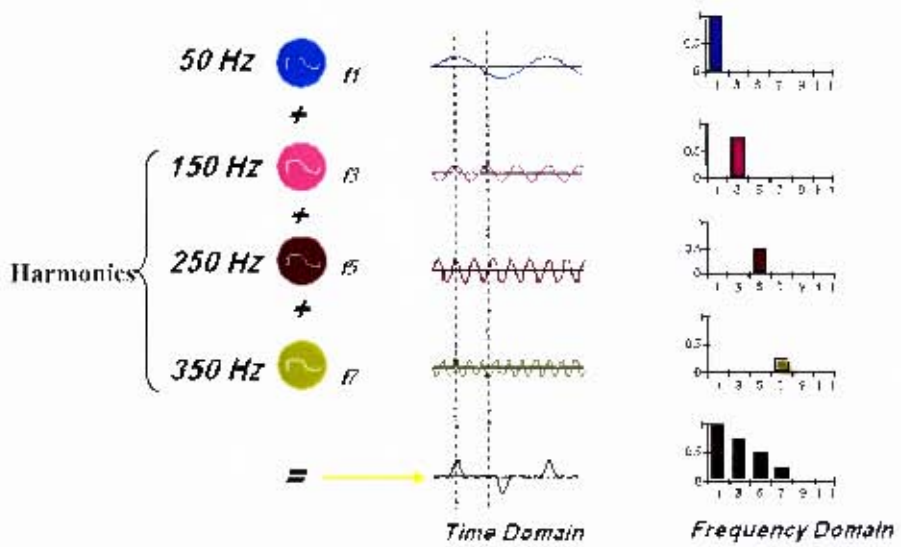

Figure 2-12 Source current transformed from time to frequency domain

The main drawback of this technique is the associated time delay in system variable sampling and computation of Fourier coefficients. This makes it impractical for real-time application with dynamic loads. This method is therefore only suitable for slow

varying load conditions. In order to make the computational process faster, some modifications were proposed and implemented in [64]. In this modified Fourier-series scheme, only the fundamental component of current/voltage is calculated and this is used to separate the total harmonic signal from the sampled waveform.

2.5 Time domain approaches

Time-domain approaches involve the use of algebraic transformations associated with changes of reference frames. This significantly reduces the control task. Time-domain approaches are based on instantaneous estimation of reference signal in the form of either voltage or current, derived from measured, distorted waveforms. These approaches are equally applicable for both single-phase and three-phase systems except for the synchronous detection theorem [32], [33] and synchronous reference frame theorem [34-36], which can only be used in three-phase systems.

2.5.1 Instantaneous reactive-power theorem

One of the instantaneous reactive-power theorems known as the (p-q) theorem was proposed by Akagi et al. [37] for three phase systems. This theory is based on the Clarke transform which transforms three-phase voltages and currents into the α 0 stationery reference frame [38], [39], and [40]. From these transformed quantities, the instantaneous active and reactive power of the non-linear load is calculated, which consists of AC and DC components. The AC component is extracted using a high pass filter (HPF) and taking the inverse transformation results in the attainment of the reference signals in terms of either current or voltage. Calculations are made using instantaneous values of the measured variable. The controller model executes the p-q theory calculations according to equations (2.9)-(2.16):

$$\begin{bmatrix} e\alpha \\ e\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix} \begin{bmatrix} ea \\ eb \\ ec \end{bmatrix} \tag{2.9}$$

$$\begin{bmatrix} i\alpha \\ i\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix} \begin{bmatrix} ia \\ ib \\ ic \end{bmatrix} \tag{2.10}$$

In equation (2.11) and (2.12), alpha and beta are the orthogonal coordinates; eα and iα are on the α axis and e and i on the axis. In three phases, conventional instantaneous power is calculated as follows:

$$P = e\alpha.\, i\alpha + e\ .\ I \qquad (2.11)$$

In fact, in the abc coordinate active power; (P) is given by the following equation:

$$P = ea.ia + eb.ib + ec.ic \qquad (2.12)$$

Instantaneous real and reactive power represented by p and q can respectively be calculated as shown in equation 2.13.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} e\alpha & e\beta \\ -e\beta & e\alpha \end{bmatrix} \begin{bmatrix} i\alpha \\ i\beta \end{bmatrix} \qquad (2.13)$$

In equation 2.13, eαiα and e .I represent instantaneous power ***p*** since these equations are products of instantaneous currents and voltages on the same axis. However, in contrast, eαi and e .iα are not instantaneous powers since these are products of instantaneous currents and voltages on orthogonal axes. Therefore ***q*** is not a conventional electric unit like the Watt or Var, ***q***; is instantaneous imaginary power or "non-real" power. In order to derive the reference currents, equation 2.13 is now re-written as 2.14:

$$\begin{bmatrix} i\alpha \\ i\beta \end{bmatrix} = \begin{bmatrix} e\alpha & e\beta \\ -e\beta & e\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix} \qquad (2.14)$$

Therefore, from equation 2.14, the instantaneous compensating currents on the ,α coordinates can be expressed as:

$$\begin{bmatrix} ic\,\alpha \\ ic\,\beta \end{bmatrix} = \begin{bmatrix} e\alpha & e\beta \\ -e\beta & e\alpha \end{bmatrix}^{-1} \begin{bmatrix} \tilde{p} \\ -q \end{bmatrix} \qquad (2.15)$$

It should be noted that $p = \tilde{p} + \bar{p}$ where $\tilde{p}$ is the AC component of p and $\bar{p}$ is the DC component. Therefore, $\tilde{p}$ can be extracted by passing $\boldsymbol{p}$ through a low pass filter and subtracting the result from $\boldsymbol{p}$ to obtain $\tilde{p}$ as expressed in equation 2.16.

$$\tilde{p} = p - \bar{p} \qquad (2.16)$$

2.5.2 Synchronous-detection theorem

Synchronous detection theorem [32], [33] is very similar to the p-q theorem. However, this technique is only suitable for three-phase application. The application of this theorem relies on the assumption that the three-phase currents are balanced. It is based on the idea that the APF forces the source current to be sinusoidal and in phase with the AC source voltage despite any variations in the load. The average power is calculated and divided equally between the three phases. The reference signal is then synchronised relative to the source voltage for each phase respectively. Even though this technique is relatively less difficult to implement; it does however suffer from the fact that it depends to a large extent on the harmonics in the source voltage [24].

2.5.3 Synchronous reference frame theorem

This theorem relies on the Park transformation which transforms the three phase system voltage and current variables into a synchronous rotating reference frame [34], [35]. The active and "non real" components of the three-phase system are represented by the direct and quadrature components respectively. In the theorem, the fundamental components are transformed into DC quantities which can be separated

easily through low pass filtering. This theorem is applicable only to three phase systems. The notable advantage associated with this method is that the system is very stable since the controller deals mainly with DC quantities. The computation is almost instantaneous except for time delays due to filtering DC quantities [28].

2.5.4 Sine multiplication theorem

This method is based on the process of multiplying the non-linear load current by a sine wave of fundamental frequency and integrating the result to calculate the real fundamental component of the nonlinear load current [41], [42] and [48]. The method is applicable for both single and three phase systems. Taking the difference between the fundamental component of the load current and the total instantaneous load current results in the derivation of the reference current for the APF. Although this technique eliminates the time delay due to low/high pass filtering experienced in instantaneous reactive power theorems, its performance is still slow (for more than one complete mains cycle), due to integration and sampling [28]. This technique is similar to the Fourier technique; however, it is implemented differently.

2.6 Review of control strategies

The purpose of APF controller is to generate appropriate gating signals for switching the inverter based on the estimated compensation reference signals [43]. Therefore, its inputs are the computed reference signals which are computed using one of the methods above, and the output is the gating pulses to be fed to the inverter switching devices.

The performance of the APF is greatly affected by the choice of control technique utilized [45]. Thus the choice and implementation of the control technique is very important for the achievement of a satisfactory APF performance [43]. A variety of control techniques, such as linear control [30], [34], [41], [42], [[44], digital dead-beat control [35], [38], and hysteresis control [17], [46], [47], have been implemented for APF application. A number of publications [17], [26], [28], [46-47] comprehensively report on the theories related to the APF. This section briefly discusses some of the techniques and their basic features.

2.6.1 Linear control technique

Linear control of an APF can be accomplished by using a negative-feedback system like the one shown in figure 2-13 [12]. In this control scheme, the compensation current i_f or voltage V_F signal is compared with the computed reference signals i_{fref} or V_{fref}. These signals are compared through the compensated error amplifier in order to produce the control signal. The resultant control signal is then compared with a saw-tooth through PWM in order to generate the appropriate gating signals for the switching transistors [30], [34], [41],[42],[45]. The frequency of the repetitive saw-tooth signal establishes the switching frequency [43]. This frequency is kept constant in the linear control technique [43]. Figure 2-14 shows how when the control signal

has a higher numerical value, the gating signal is set high, and when it has a lower value the gating signal is set low.

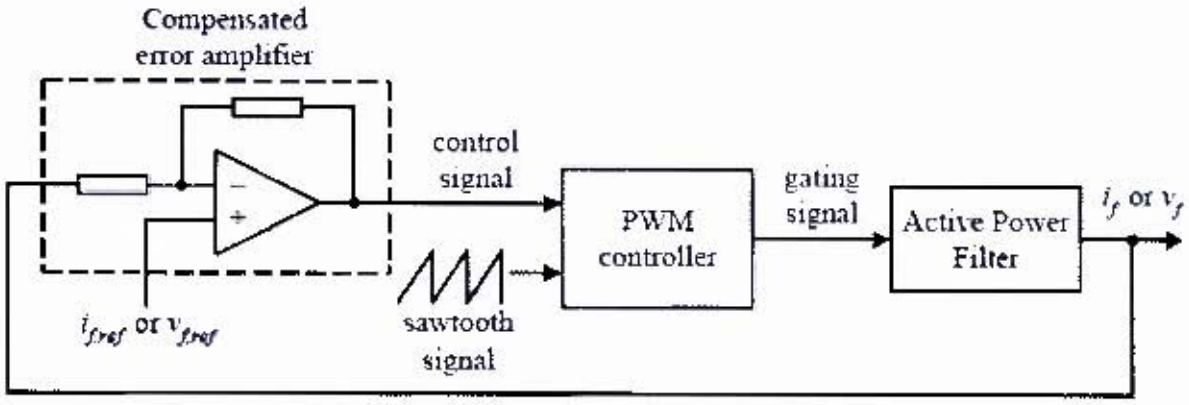

Figure 2-13 Linear control technique [43]

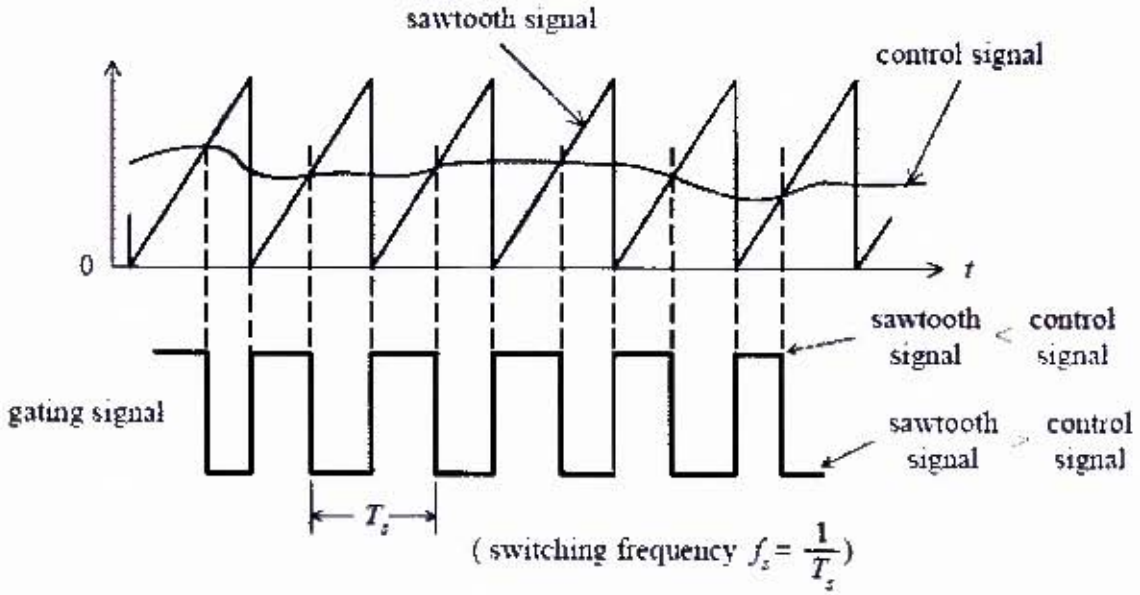

Figure 2-14 Gating signal generation by linear controller [43]

Generally, Bode plots and the Nyquist stability criterion is used to establish the appropriate compensation in the feedback loop for the desired transient and steady state responses.

Linear control techniques like the one described above, often result in an unsatisfactory harmonic compensation performance. This is mainly due to the

limitation of achievable bandwidth of the compensated error amplifier [26], [44]. (The argument in the rest of this section is extracted from [48]).

When this scheme is applied to an APF, the filter inductor current I_f (or feed-back current) is sensed and compared directly with the reference current as calculated by the harmonic calculator. This error is amplified and used as the modulating signal in the unipolar PWM which controls the gating of the switches. This scheme, however when used as it is suffers from a number of disadvantages. Firstly, the current sensed will have switching ripple in it and will have to be filtered before being fed into the high gain error amplifier. This pertinent filter would introduce a time delay. The system is already a second order due to the high frequency LPF. This second order dynamic has a sharp phase angle variation near its resonant frequency due to its under-damped nature. In addition, the phase angle delay contributed by the filter depends largely on the operating conditions.

Therefore, if a high gain stage with a first order filter is put in the feedback path, the system easily becomes unstable. Even if the system is stable, its transient performance would not be satisfactory. Hence this would call for the reduction of gain in the error amplifier which will affect the ability of the APF to track the reference current adversely. If a high gain is mandatory, then a high switching frequency has to be used. However, the current that is being sensed will be corrupted by the inevitable high frequency switching noise. The control loop usually gets upset with this noisy feedback. The limitations of the feedback control scheme as discussed above are overcome with the use of a feed-forward control scheme. Feed-forward control is implemented in the single phase shunt APF topology and will be discussed in detail in the following chapter.

2.6.2 Hysteresis Control

This type of control imposes a bang-bang type of instantaneous control that forces the APF compensation current to follow the estimated reference signal within a certain tolerance band [36], [37], [46-47]. The control scheme is shown in block diagram in figure 2-15. In this control scheme, a signal deviation **H** is defined and imposed on ***iref*** to form the upper and lower limit of the hysteresis band. The inverter output current ***if***, is then measured and compared with ***iref***. The resultant error is subjected to a hysteresis controller to determine the gating signals determined by the upper or lower limits set by H/2 and –H/2. As long as the error is within the defined hysteresis band, no switching action is takes place. Switching occurs whenever the error exceeds the value of the upper or lower band limits. The APF is therefore switched in such a way that the peak-to-peak compensation current is limited to a specified band determined by **H** as illustrated in figure 2-16.

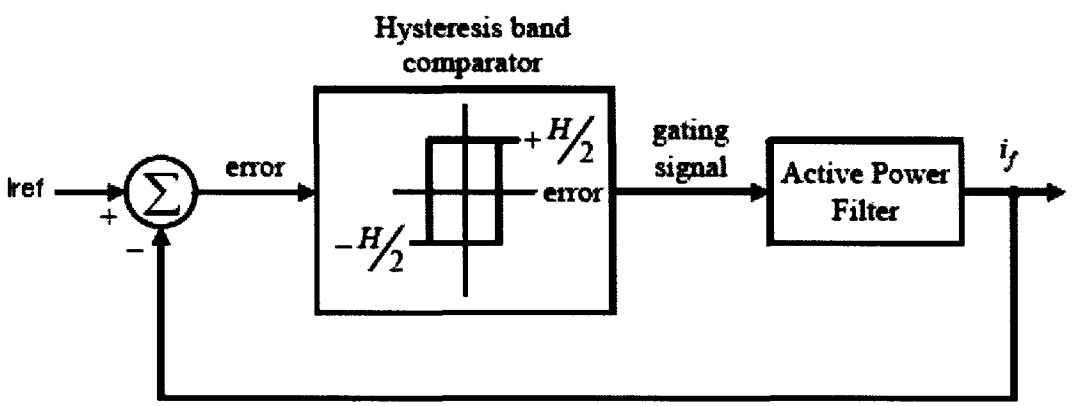

Figure 2-15 Hysteresis current controller [43]

To obtain a compensation current, ***if*** with switching ripples as small as possible, the value of **H** can be reduced. However, doing so results in higher switching frequency thus resulting in increased losses in the switching transistors.

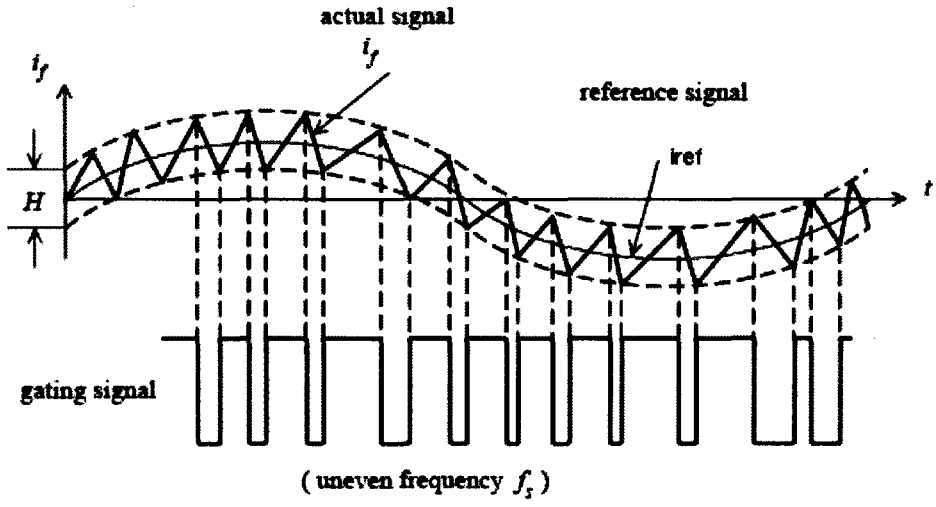

Figure 2-16 Gating signal generation by hysteresis controller [43]

It should however be noted that hysteresis current control is indeed suitable for APF application if only low order harmonics like (3^{rd}, 5^{th}, 7^{th}....25^{th}) need to be compensated. However, if harmonics up to the 50^{th} need to be compensated, hysteresis control will require excessively high switching frequency. In addition to that, the variation in switching frequency - which is inherent in hysteresis control - makes it difficult to choose the LPF components. However, for practical application, hysteresis control remains the preferred method for implementing effective current control of inverter in APF applications.

3. Theoretical concepts of the Single Phase Shunt APF topology

3.1 Operating principles of the selected APF topology

The operating principle of the single phase shunt APF topology is illustrated in figure 3-1. In the entire design the subscripts *s*, *L* and *f* respectively represent source, *L* stands for load and *f* stands for shunt APF. The shunt APF generates compensation current i_f which consists of equal but opposite load harmonic components. It does so by producing a voltage V_{out} in the inverter's output terminals that will result in the compensation current i_{fref} flowing to the grid at the point of common coupling (PCC). The real and imaginary current components add up at the PCC to produce i_o, the load current. To explain this concept in another way, it can be said that the source current contributes the real power consumed by the load, whereas the APF supplies the imaginary power. The source current i_s is desired to be sinusoidal and in phase with the source voltage v_s, in order to yield maximum power factor.

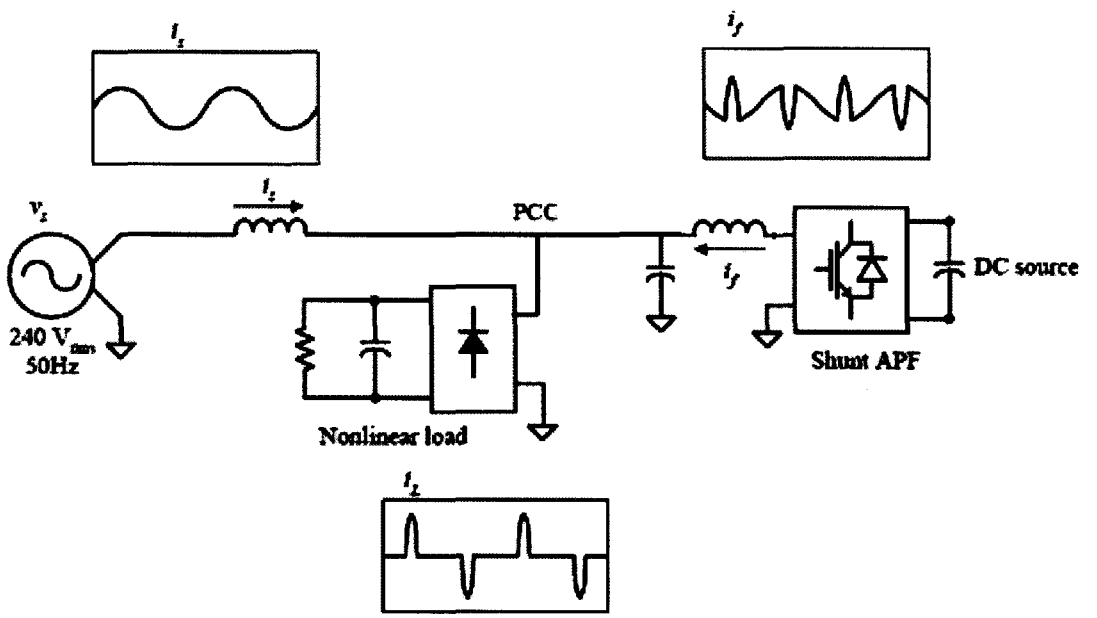

Figure 3-1 Desired operation of the APF

Figure 3-1 above depicts the required operation of the single phase shunt APF, (figure 3-1 is constructed using information from [43]). Thus, the basic operating principle of the shunt APF topology is that it must compute a current that is equal but opposite in polarity to the harmonic current components drawn by the load, inject this current at PCC thus forcing the source current to become sinusoidal.

3.2 System configuration

In this section the configuration of the single-phase APF topology is presented. The overall power circuit, the APF inverter and the control system will be discussed.

3.2.1 Overall system

Figure 3-2 depicts the overall system configuration for the single phase shunt APF topology. The APF is connected in parallel with the full bridge 500VA converter which represents the non-linear load. The system consists of a single phase shunt APF which is constructed using a full-bridge voltage source inverter (VSI) and a DC source. The APF is connected to the distribution system at the PCC through the interfacing inductor L_f. The interfacing inductor provides isolation against transients in the distribution line and variations in the load. Furthermore, the driving voltage across the interfacing inductor determines the optimal dynamic response that can be achieved by the APF. The LC filter which consists of L_f and C_f provides low pass filtering which eliminates high frequency switching noise due to IGBT switching action.

The VSI utilizes a DC bus capacitor as the DC supply and it switches at the frequency of 10kHZ in order generate a compensation current that follows the estimated current reference, i_{fref}. Therefore, the voltage across the DC bus capacitor V_{cf} must be controlled in such a way that it remains at a value that is higher than the peak of the source voltage i.e, $(> \sqrt{2} \cdot Vs)$ in order to force the current in the direction of the load.

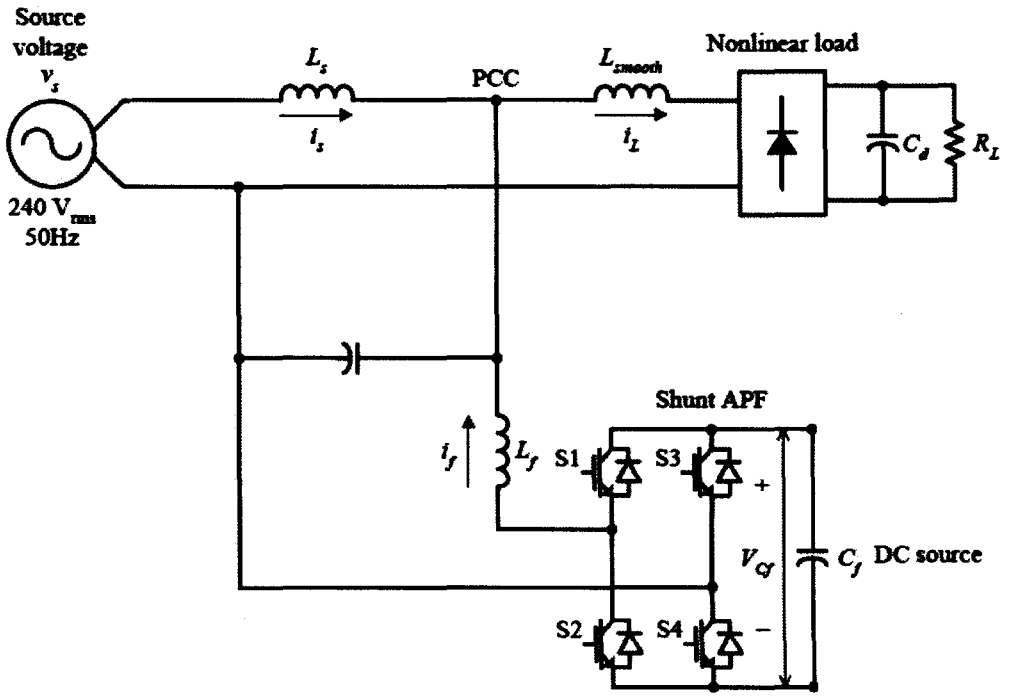

Figure 3-2 Configuration of the single phase shunt APF [43]

The desired waveform i_f, as shown in figure 3-1 is achieved by accurately switching the gates (S1, S2, S3, S4) of the IGBTs of the inverter. The exact control of the output current wave shape is limited by the switching frequency of the inverter in terms of frequency and by the available RMS voltage across the interface inductor in terms of amplitude.

3.3 APF control system

Figure 3-3 depicts the details of the overall control system. It consists of the harmonic current calculator, the DC link voltage regulator and the feed-forward controller.

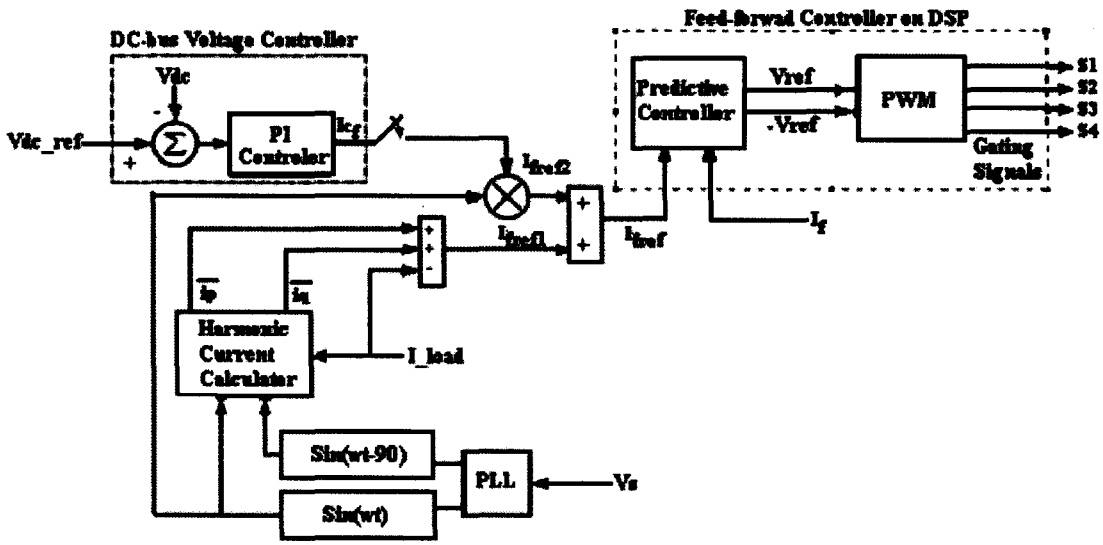

Figure 3-3 Overall APF control scheme

The harmonic current calculator accepts the load current i_o; it also accepts a sine and cosine wave templates to extract the harmonics from the load current in real time. The DC link voltage regulator senses the DC voltage across the capacitor and compares it with a fixed reference voltage, V_{dc_ref}. The error is processed in the PI controller. The reference currents from the harmonic calculator and from the PI controller are then added in a summer to give i_{fref}. The reference i_{fref}, is fed to the predictive controller as shown in figure 3-3. The feed-forward controller uses the reference current input and the feedback current i_f, to work out the reference output voltage, V_{ref}. The feed-forward controller, therefore, ensures that the inverter output current i_f follows i_{fref}. The following sections discuss the major subsystems of the control scheme i.e.; the harmonic current calculator, the DC-bus PI controller and the predictive controller in detail.

3.3.1 Harmonics Calculator

The sine multiplication theorem [41] discussed briefly in the previous chapter is used to extract the harmonics contained in the load current, i_o. The harmonic calculator accepts the load current i_o, and orthogonal sinusoidal templates from the PLL and returns the harmonic content of the load current. The method of extracting the "non real" fundamental components contained in the load current is based on extracting orthogonal fundamental frequency components from the waveform. This is achieved as shown in figure 3-4. The load current ***io***, is multiplied by the unit sine wave and unit cosine templates produced by PLL. The products are integrated every half cycle i.e., (10mS); of the 50Hz AC cycle. The values of the integrated outputs are sampled and held at the end of the half cycle period. After sampling, the integrators are reset briefly to start the next integration cycle [48].

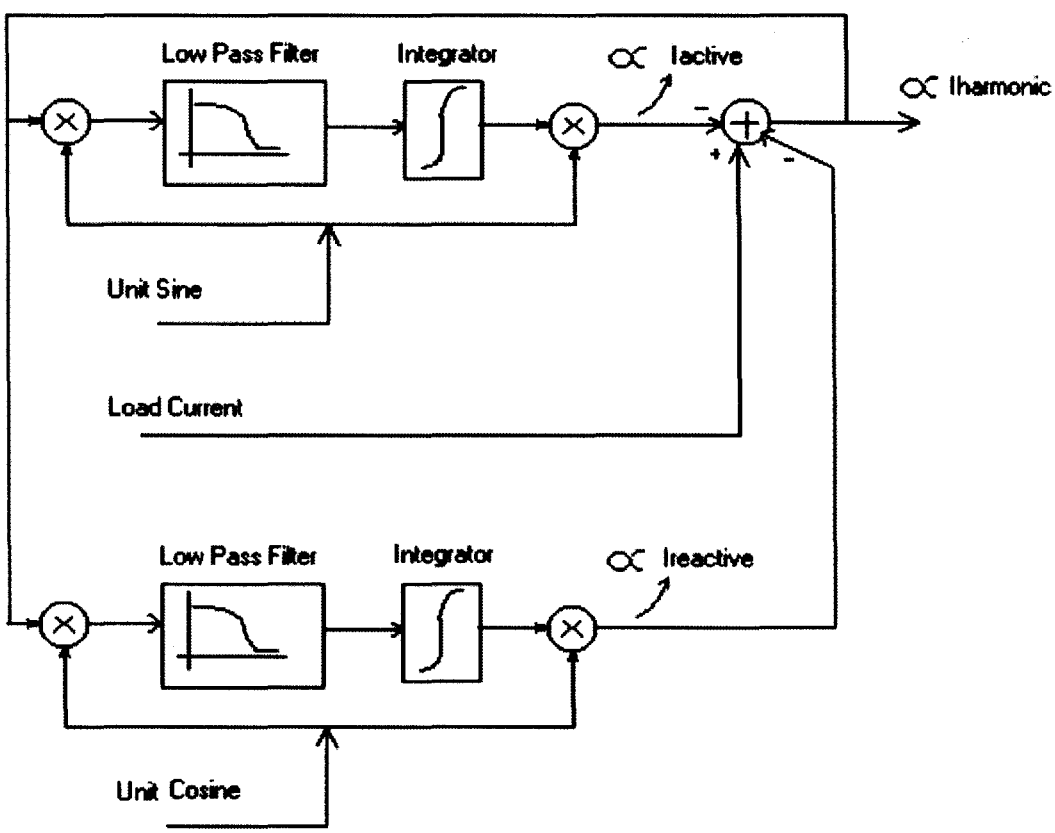

Figure 3-4 harmonic extraction using sine multiplication theorem [48]

The sampled outputs are the amplitudes of the DC components of active and reactive components of the load current respectively. These components are then re-multiplied by the unit sine and cosine templates in order to re-create the active and reactive fundamental components. The fundamental components are then added together and their sum is subtracted from the total load current to yield the harmonics or "non-real" current components. The active and reactive current components can be thought of as the current components that contribute to active and non-real power required by the load. Therefore if $\boldsymbol{p}$ represents the total real power consumed by the load and $\boldsymbol{q}$ represents the non-real power consumed by the load. The following formulas clarify the statements made above and are taken from Akagi's theorem [5]:

Given that the load current is: $io(t) = \sum_{n=1}^{\infty} \sqrt{2} Lo, n \sin(n\omega t + \theta n)$ (3.4)

Where θn is the phase angle of the nth load current component. Under normal circumstances, the source voltage can be assumed to be sinusoidal, i.e,

$$Vs(t) = \sqrt{2} Vs \sin(wt + \phi) \tag{3.5}$$

where ϕ is the phase angle of the source voltage.

Therefore, the instantaneous active load power is derived as:

$$Po(t) = Vs(t) \cdot io(t) \tag{3.6}$$

$$= \bar{Po} + \tilde{Po}$$

The instantaneous imaginary load power can be derived as:

$$qo(t) = V's(t) \cdot io(t) \tag{3.7}$$

$$= \bar{qo} + \tilde{qo}$$

Where $\bar{P}o, \bar{q}o$ represent the DC components and $\tilde{P}o, \tilde{q}o$ denote the AC components and Vs'(t) denotes the source voltage delayed by 90°. Thus Akigi's theorem given above makes it easy to deduce that by extracting the DC components through LPF, the reference current i_{fref} is obtained by subtracting the fundamental components from the total load current as shown in equation 3.8.

$$i_{fref} = i_{0(t)} - \bar{i}_{0p(t)} - \bar{i}_{oq(t)} \qquad (3.8)$$

Where io(t) is the total load current, $\bar{io}\,p(t)$ is the fundamental components of the load current that contribute real power and $\bar{io}\,q(t)$ is the fundamental components that contribute non-real power.

3.3.2 Control Strategy

The control problem of the APF is to regulate the DC-link voltage and to inject the reference current i_{fref}, obtained using the method above. The first controller regulates the current ***Ic***, drawn from the grid in order to charge the DC link capacitor to a set voltage, ***Vdc_ref***. The second controller controls the current that is injected by the VSI at the PCC. The two control schemes are discussed below.

3.3.2.1 Design of PI controller to control DC capacitor voltage

The DC voltage across the DC bus capacitor is detected and compared with the reference voltage ***Vdc_ref***. The error is processed in a PI controller. The output of the PI controller is the DC-bus capacitor charging current, ***Ic***. The charging current is multiplied by the unit reference sine wave sin (wt), obtained by phase-locked-loop (PLL) to ensure that only real in-phase current is drawn from the grid to charge up the capacitor. The charging current ***Ic***, will continue to charge the capacitor until the capacitor voltage has reached the set reference voltage, ***Vdc_ref***. The PI controller used to control the DC-bus voltage is shown in Figure 3-5. Its transfer function can be represented as shown in equation 3.9.

$$H(s) = Kp + \frac{Ki}{s} \tag{3.9}$$

Where, ***Kp*** is the proportional constant that determines the dynamic response of the DC-bus voltage control and ***Ki*** is the integration constant that determines the settling time,T.

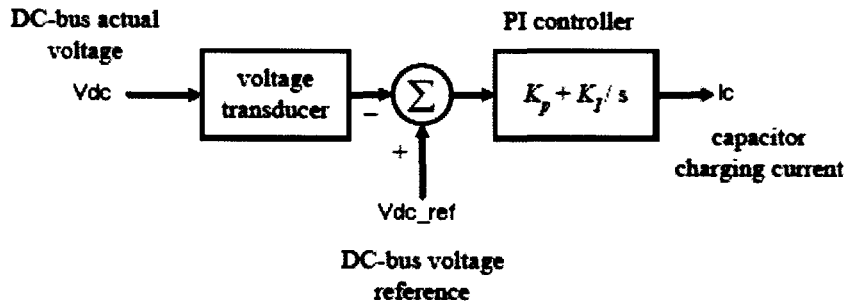

Figure 3-5 PI Controller for DC link voltage control [43]

Kp and ***Ki*** constants must be chosen in such a way that the correct control performance is met. If ***Kp*** and ***Ki*** are too large, the DC voltage regulation will be dominant, and the steady-state DC-bus voltage error is low. If, on the other hand, ***Kp*** and ***Ki*** are small, the DC voltage regulation will have little effect on the transient performance of the APF. As described in [43], ***Kp*** can be calculated using the energy-balance principle. After ***Kp*** is calculated, ***Ki*** can be determined empirically; also see [22] for the derivation of ***Ki*** and ***Kp*** constants. Thus the total reference current that is fed to the feed-forward current controller is obtained by adding the capacitor charging current, ***Ic*** from the DC-bus PI controller to the reference current obtained from the harmonics calculator as shown in equation 3.10.

$$i_{fref} = io(t) - \bar{io}, p(t) - \bar{io}, q(t) + Ic \qquad (3.10)$$

The reference current i_{fref} is now fed to the main current controller which is described below.

3.3.3 Feed-forward current control scheme

The feed forward control scheme was introduced in chapter 2. In chapter 2 it was discussed that predictive control has an advantage over conventional closed loop control due to the advantage of large bandwidth available in the loop resulting in faster response time which is highly desired in APF. This control scheme is now

explained further and it will be shown how it can be implemented in the shunt APF topology:

Assuming that the control is successful, the current that will flow through the inverter's inductor L_f is known beforehand, i.e.; equal to the known reference current i_{fref}. Thus, if ($i_f = i_{fref}$) is known beforehand, then the voltage that the inverter should generate in order to realise this current flow can be calculated before-hand using equation 3.15 [48], refer also to figure 3-6.

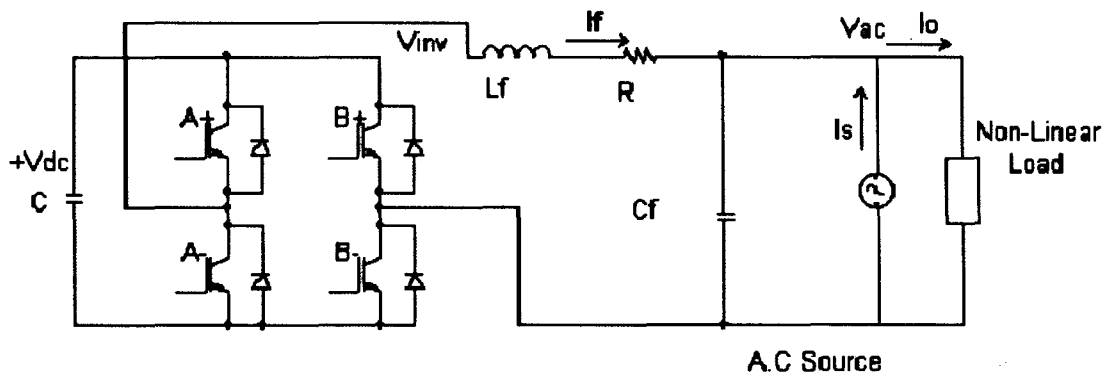

Figure 3-6 equivalent single phase circuit of APF and source voltage [48]

$$Vinv = Vac + Ri_{fref} + Lf(\frac{\partial i_{fref}}{\partial t}) \qquad (3.15)$$

Where: i_{fref} is the reference current calculated by harmonic calculator and DC bus PI controller.

R is the equivalent loss resistance (which includes winding resistance of L_f, switch power loss etc),

L_f is the output filter inductance and,

Vac is the source voltage.

Figure 3-7 shows the practical application of the feed-forward control scheme in block diagram form. It requires precise knowledge of the values of R and L_f. The

value of ***R,*** however, is operating point dependant (due to switch power losses) and cannot be known exactly [48]. Nevertheless, if these values can be approximated then the goal of achieving current control that is "free of dynamics" can be attained. However, there are inaccuracies in the estimation of the parameters and inaccuracies in the measurement of the grid voltage, ***Vac***. Furthermore, the differentiator operation has to be band limited in practice due to the sensitivity of the differentiator circuit to noise and high frequency signals. Thus in practice a small amount of actual current feedback will be needed, along with other components in order to correct minor deviations. Nevertheless, in this case the role of current feedback is merely to correct second order effects thus enabling the feedback loop to be of low gain. Moreover, since the gain is low no filtering is needed in the feedback loop in this case.

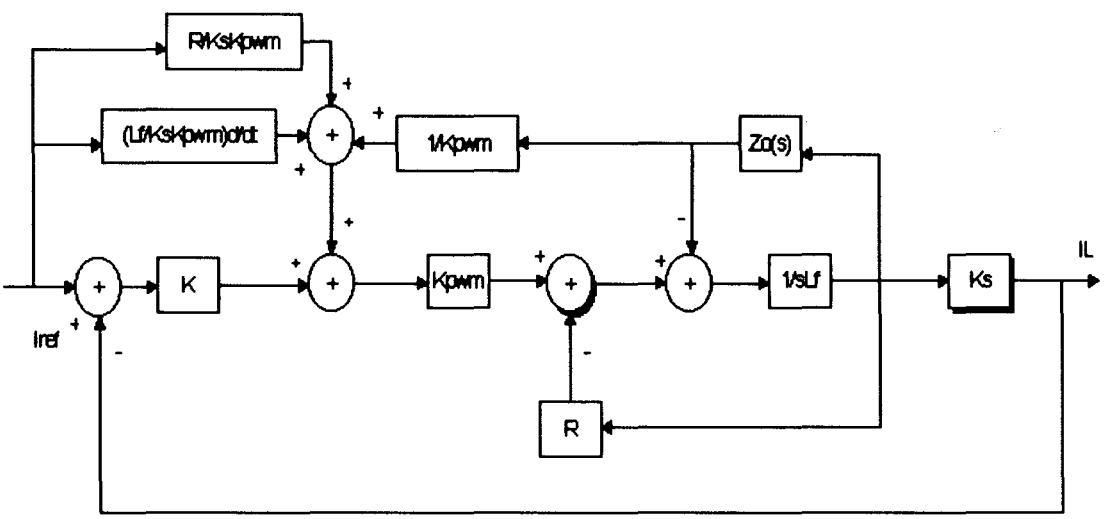

Figure 3-7 Feed-forward control scheme [48]

With the feedback loop added, the control voltage worked out according to equation 3.15 is modified as show in equation 3.16 [48].

$$Vinv = Vac + Ri_{fref} + Lf(\frac{di_{fref}}{dt}) + K(i_{fref} - If) \qquad (3.16)$$

Where K is the feedback gain and is very small. This scheme is capable of a rise time of 50mS to 250mS which yields a high bandwidth current control loop that is desirable in APF since it is expected to track up to the 25^{th} harmonic and more. In figure 3-7, K is the feedback gain, $Kpwm$ is the gain of the inverter and Zo is the equivalent load impedance connected at the AC source point. Note that the sum total of the inverter output voltage, V_{inv}, is the total voltage drops across the output link inductance, inductor resistance and the grid voltage, Vac. Thus the output inverter voltage must be larger than the grid voltage after the inverter is synchronised to the grid. This requires that the grid voltage be kept low in practice in order not to exceed the VA rating of the inverter. However, according to equation 3.16, the output of the inverter depends on the value of the supply voltage Vac. Practically this posses a catch 22 situation. In order to overcome this, a potentiometer is used in the DSP which multiplies the inverter output voltage by a factor by varying the modulation index, ma, in PWM. Once the inverter has been configured correctly, the next important component to consider in the design is the interface inductor L_f, and the output LC filter to prevent switching noise passing to the grid.

3.4 Design of link inductor and DC-Bus capacitor

The link inductor is a relatively important component since it determines the overall frequency response of the system and the time constant needed in order to cancel out high order harmonic components [53]. A large inductor is better for isolation from the power system and from protection against transient disturbances. However, too large an inductor will limit the ability of the APF to cancel higher order harmonics. Therefore, there is a trade-off involved in sizing the interface inductor.

3.4.1 Design of link inductor

The design starts with some known parameters such as the DC-link design voltage, the effective switching frequency f_s, and the acceptable current ripple ΔI, in the inverter output current. The forth factor to consider is the RMS value of the highest frequency current component that the APF must output. The latter enables to design for the worst case scenario, i.e., the inductor to be chosen must be able to track up to and including the 25th harmonic at the desired RMS value with the available DC link voltage. Equation 3.11 [53] relates the DC link voltage and the inductor value to the highest frequency current component, I_h:

$$I_h = \frac{\frac{U_{dc}}{\sqrt{2}} - V_s}{n\omega L_h} \qquad (3.11)$$

I_h is the RMS value of the harmonic current of order n. v_s is the rms line voltage, Udc is the available DC link voltage, L_h is the main inductance and is the fundamental frequency. It should be apparent from equation 3.11 that the link inductance L_h, and the DC link voltage U_{dc} predominantly determine the value of I_h. The inductor value can therefore be obtained by manipulating equation 3.11 as 3.12:

$$L_h = \frac{\frac{U_{dc}}{\sqrt{2}} - V_s}{I_h n\omega} \qquad (3.12)$$

Once a satisfactory inductance value has been determined, it is necessary to determine what the resulting current ripple will be at the desired inverter switching frequency, f_s. Equation 3.13 [53] gives the peak-to-peak ripple of the output current i_f, of the inverter given the inductor value obtained using equation 3.12.

$$\Delta I = \frac{U_{dc}}{4 \cdot f_{PWM} \cdot L_h} \qquad (3.13)$$

If the current ripple is too large i.e., > 1Ap-p, the ripple can be cured by incorporating an LC filter between the output of the inverter and the grid. The filter can be a damped second order system R-Lf-Cf. The equivalent filter circuit is shown in figure 3-9. The purpose of the filter is to provide good suppression of switching noise and other unwanted harmonics of the PWM switching frequency.

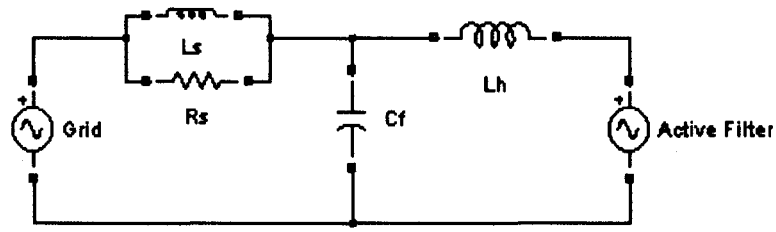

Figure 3-9 Equivalent circuit of Grid-APF interface [53]

The overall transfer function from the grid voltage, e and the active filter voltage u, to the line current i; flowing through the filter is given by:

$$i = \frac{[u - e \cdot (1 + s^2 L_h C_f)](1 + s\frac{L_f}{R})}{s \cdot (L_f + L_h) \cdot [1 + s\frac{(\frac{L_f L_h}{L_f + L_h})}{R} + s^2 (\frac{L_f L_h}{L_f + L_h}) C_f} \qquad (3.14)$$

Equation 3.14 is used in Matlab Simulink to design the filter shown in figure 3-9 to test its response.

3.4.2 Design of DC-Bus capacitor

A small capacitor is ideal for yielding fast response to follow the rapidly varying compensation current. However, a larger capacitor results in slower response time thus delaying the PI control action. Therefore, a balance has to be striked between adequate capacitor size versus good dynamic performance. The DC bus capacitor value can be estimated using equation 3.15, according to [16]. The value of the DC bus capacitor is dependant on the magnitude and frequency of the source voltage, the set DC-bus voltage and the desired minimum ripple in the DC-bus, thus:

$$Cdc \geq \frac{\sqrt{2}Vs \cdot \Delta IL \cdot \frac{T}{2}}{|(\Delta VCdc)^2 - (VCdcref)^2|} \qquad (3.15)$$

Where: v_s, is the RMS value of the source voltage.

ΔIL, is the peak RMS value of the harmonic load current.

T, is the period of the source voltage and,

ΔVdc, is the minimum and maximum DC-bus voltage respectively.

4. Simulation of the shunt APF

4.1 Introduction

Due to the complexity of modern power electronics systems, computer simulations is an indispensable tool to analyse circuits which are otherwise too complex to do with hand calculations. This chapter is dedicated to the Orcad Pspice™ verification of the single phase shunt APF topology. To begin with, Orcad Pspice™ simulations of subsystems and then of the overall system is developed. The simulation mainly focuses on the time-domain response analysis. The simulation models are discussed part by part starting with the modelling of the entire circuit followed by a detailed discussion of all the subsystems.

Simulation was used extensively in the development of the single phase shunt APF. Firstly, the model was built on simulation using the available components from PSpice library. However, when the project evolved to building stage, it was discovered that while the prototype worked well in simulation, most of the parts were not practically available. Thus the simulation was changed several times in order to ensure that optimal performance is reached whilst ensuring that the components used in the design are available on the market. Thus a compromise between performance, cost and availability of components was borne in mind in order to produce the final completed simulations described below.

4.2 System modelling in Orcad PSpice

The complete simulation of the single-phase 240V RMS, 50Hz, 500VA active filter of current injection type is depicted in figure 4-1. It consists of the power distribution system, non-linear load, shunt APF and its overall control system. The simulation fixed-step size was chosen to be one micro-second. Generally, the smaller the simulation step size, the more accurate the simulation results will be. However, this also results in longer simulation time.

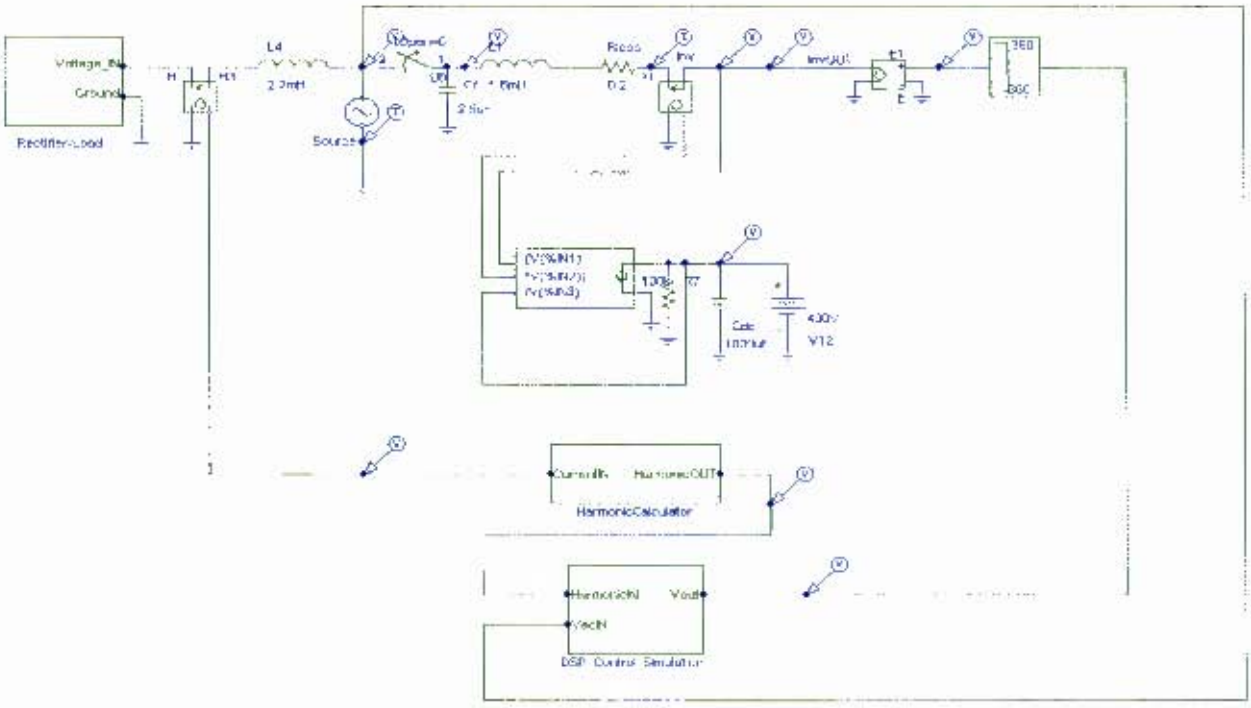

Figure 4-1 Complete simulation model of APF

The main blocks which will be discussed in detail are the power distribution system and the APF. The distribution system consists of the source and the non-linear load. An inductance of 2.2mH is deliberately placed between the source and the load in order to increase the source impedance in order to suppress high frequency harmonics. The APF consists of the 'Harmonic Calculator', the controller which implements feed-forward control and the inverter. The blocks are now discussed in detail below.

4.2.1 Distribution System

The power distribution system consists of the source voltage, the reactive elements and the non-linear load. The source considered in the simulation is a 240Vrms, 50 Hz sinusoidal single phase AC voltage source. The distribution voltage v_s, is generated by the Orcad PSpice 'sources' library. The utility supply voltage is modelled as a sinusoidal voltage source in series with an inductance which simulates the source internal impedance. The purpose of the inductor is also to increase the source impedance to suppress flow of high frequency harmonics.

The values that were selected to simulate the series inductance that is present between the source and the load was chosen to be:

$$Ls = 2.2mH$$

$$Rs = 0.2\ \Omega \qquad (4.1)$$

4.2.2 Non-linear load rectifier

Figure 4-2 shows the detail of the non-linear load block which is represented by a single phase full bridge converter. The converter was constructed using MR860 high power diodes from Motorola obtained from PSpice Orcad 'semiconductors' library, (see data sheet in appendix A). The AC-DC rectifier is driving an 118W resistive load, R_L. A DC smoothing capacitor, C_d is installed to reduce the ripple on the DC side of the rectifier. The passive component values selected for the simulation model are given by:

$$C_d = 470uF$$

$$R_L = 250\ \Omega \qquad (4.2)$$

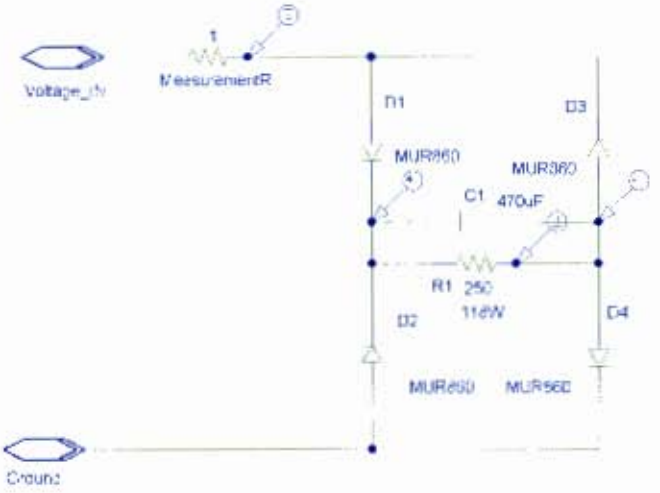

Figure 4-2 Details of non-linear load block

The resistance of 250 Ohms was chosen to ensure that the converter draws a minimal current of 8A to ensure that the APF is not burdened to supply a large compensation current. This also ensures that the inverter output voltage does not have to be too large.

4.3 Shunt Active Filter (APF)

The APF consists of the 'Harmonic Calculator', The 'DC bus regulator' and the 'inverter control voltage block' which implements feed-forward control. Each of these blocks has been discussed in detail in the previous chapter. However, the components that make up the blocks will be discussed below.

4.3.1 Details of Harmonic Calculator Block

The harmonic calculator block implements the sine multiplication theorem discussed previously. The details of the "Harmonic Calculator" block are shown in figure 4-3. It consists of two low pass filters (LPF) which are tuned at 50Hz. The outputs of the LPFs are then fed to the integrators made up using the "LF411" op-amps. The LF411 op-amp was chosen because of its ideal high speed performance and large bandwidth, (see datasheet in appendix A). The LF411has a large gain bandwidth of 3 MHz which produces a fast slew rate of 10V/ s.

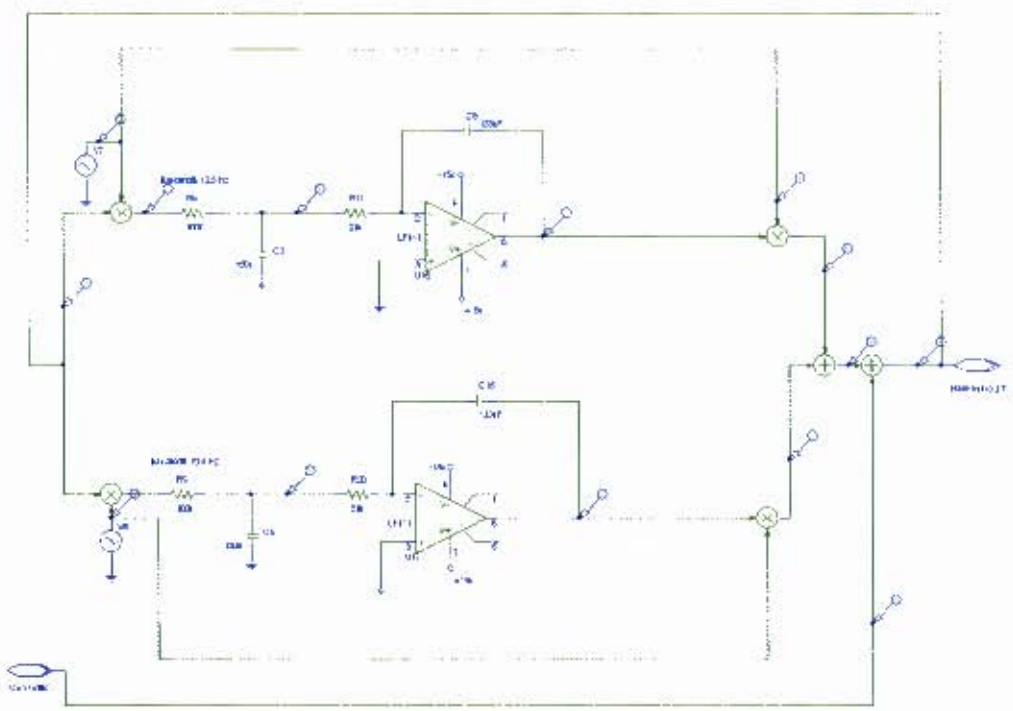

Figure4-3 Detail of harmonic calculator

The cheaper LM741 op-amp was tried in the place of the LF411 in an attempt to alleviate cost. However, its performance yielded a highly distorted output. The output of the integrator is fed into an analogue multiplier and then multiplied with the unit sine-wave in order to reconstruct the fundamental active and "non real" components of the input current. The result of the integrators is then subtracted from to the original input current which leaves only the harmonic components of the load current.

4.3.2 Details of DC bus regulator block

The inverter's DC bus controller shown in figure 4-4 is an analogue proportional integral (PI) controller. Its purpose is to maintain a steady capacitor DC voltage. The DC value is set to $\sqrt{2} * Vac$ which is approximately 360 VDC. The actual voltage across the capacitor is measured and reduced to a suitably low voltage and fed to the PI controller. The PI controller proportional and integral gain values were chosen to be:

$$P = 2.2; \qquad I = 10 \qquad (4.3)$$

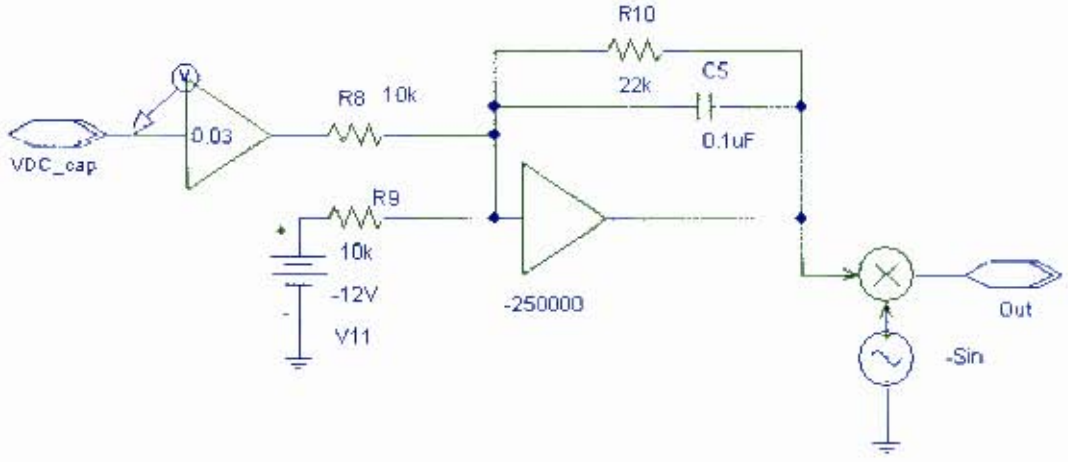

Figure 4-4 Analogue DC-Bus PI controller

The output of the PI controller is the capacitor charge current Ic. The output is multiplied by an in-phase unit reference sine wave, sin (wt), obtained by PLL. The sine wave is in phase with the source voltage to ensure that real power is drawn from the grid in order to charge the capacitor. This block ensures that the capacitor remains charged at approximately 360V DC - slightly higher than the source voltage. This is to ensure that compensation current flows from the inverter to the source.

4.3.3 Details of Voltage Source Inverter

In the simulation of figure 4-1, the VSI is modelled as a voltage controlled voltage source with saturation behaviour. The input side i.e., the DC capacitor side is modelled by implementing power balance using the PSpice ABM block, (see glossary). The ABM block senses the inverter output current, multiplies it by the inverter's output voltage and divides the product by the DC side capacitor voltage. Using the power balance principle, it is evident that the result of this calculation will be the DC link capacitor current. The ABM block outputs this current and feeds it to the capacitor node as shown in figure 4-5.

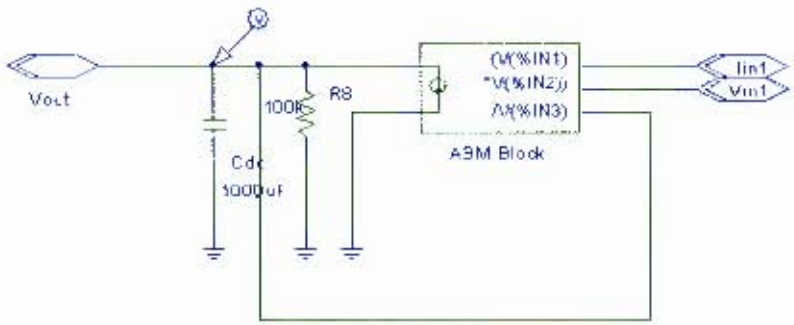

Figure 4-5 Detail of VSI model

The design of the DC-bus capacitor was covered in the previous chapter. Here, a DC capacitor value was calculated based on equation 3.14. The actual value of the DC-bus capacitor, Cdc was calculated to be 1000uF.

4.3.4 Output low pass filter inductive and capacitive components

The selection of the AC link inductance and the capacitor values directly affects the performance of the active power filter performance. The method of selecting the components of the output filter components i.e., L-C is obtained by utilising the theory outlined in section 3.5.1 above. The linear electrical circuit of the L-C components is modelled is simulated in Matlab in order to analyse its steady-state operation and to analyse the actual frequency response of the output filter in relation to the grid and the inverter. The inverter is modelled by a controlled current source producing a noise at 10 kHz which represents the inverter switching frequency.

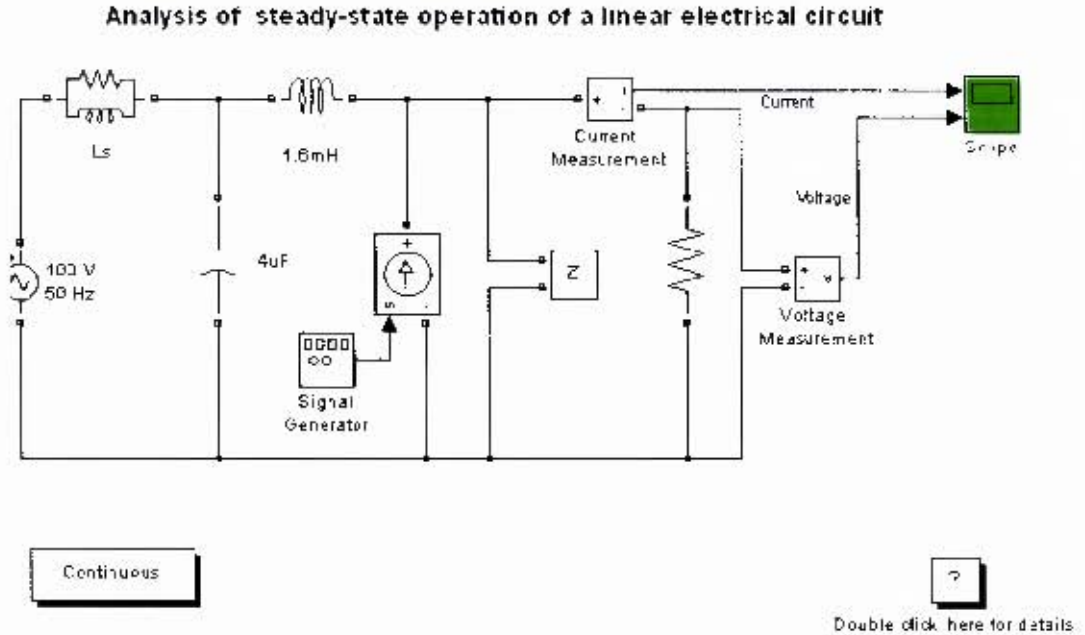

Figure 4-6 Analysis of LC filter network

Utilizing equation 3.11-3.13, the inductor value is 1.6mH, and 2kHz is selected as the natural frequency ω_n of the filter. This allows the active filter to compensate currents up to the 25th harmonic, while providing good attenuation of the PWM frequency at 10kHz. Thus, the following values were obtained:

$$Lf = 1.6mH$$

$$Cf = 4uF \qquad (4.8)$$

Figure 4-7 illustrates the effect of the output filter. The curve represents the current through the main inductance L_h, at the switching frequency of 10kHz. Thus as shown in figure 4-7, the switching frequency harmonics are well suppressed without visibly affecting the desired bandwidth.

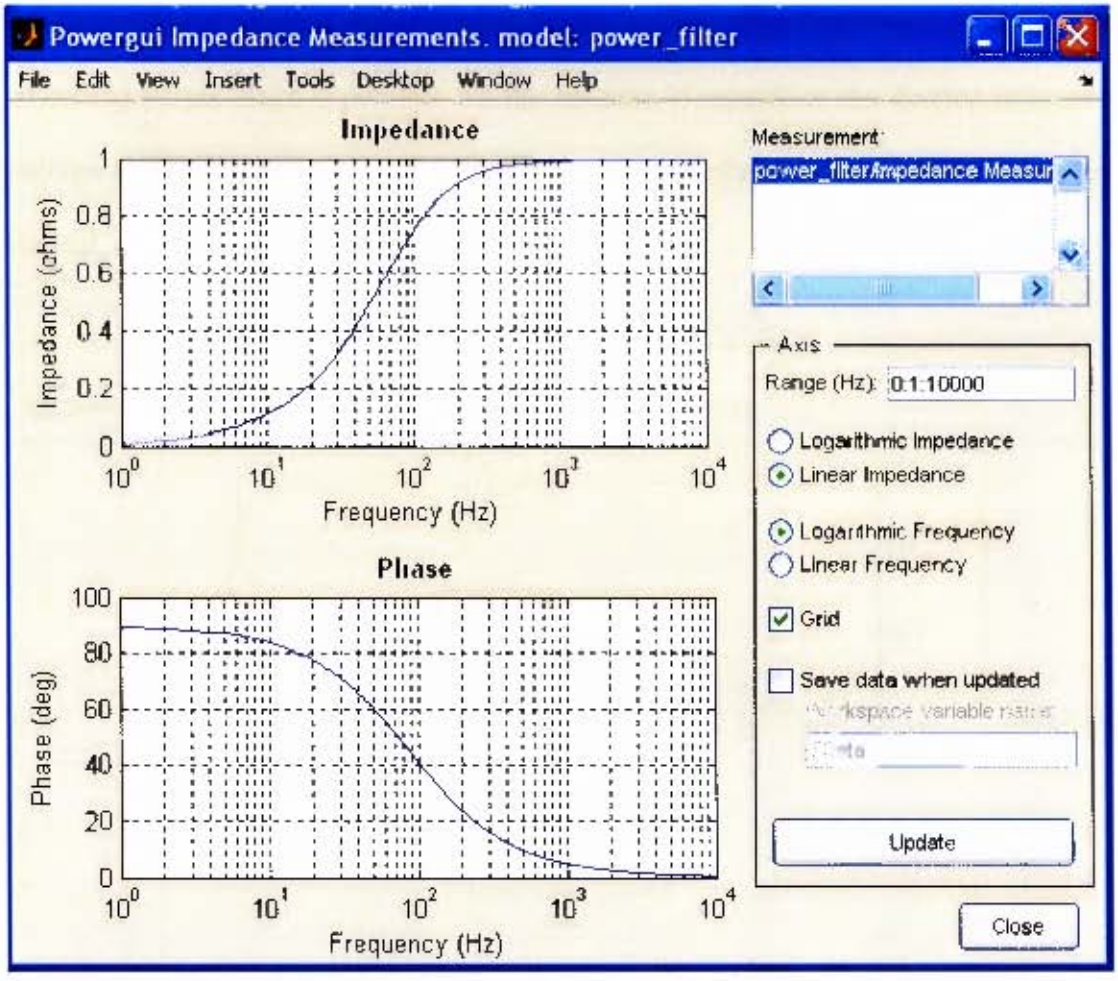

Figure 4-7 Frequency response of output filter

4.3.5 Inverter control voltage block (feed-forward control)

The inverter control voltage block implements feed-forward control which was discussed in the previous chapter. It accepts the output of the harmonic calculator, I_{ref} and outputs the inverter reference voltage, V_{ref}. The output voltage is calculated by implementing equation 3.12, (without the feedback gain). This voltage is sent to the PWM module to produce the switching pulses for switching the inverter IGBTs. The switching pulses make it possible for the inverter to reproduce the desired reference voltage V_{ref}, at the inverter output terminals which results in the flow of the reference current, i_{ref} through the link inductor.

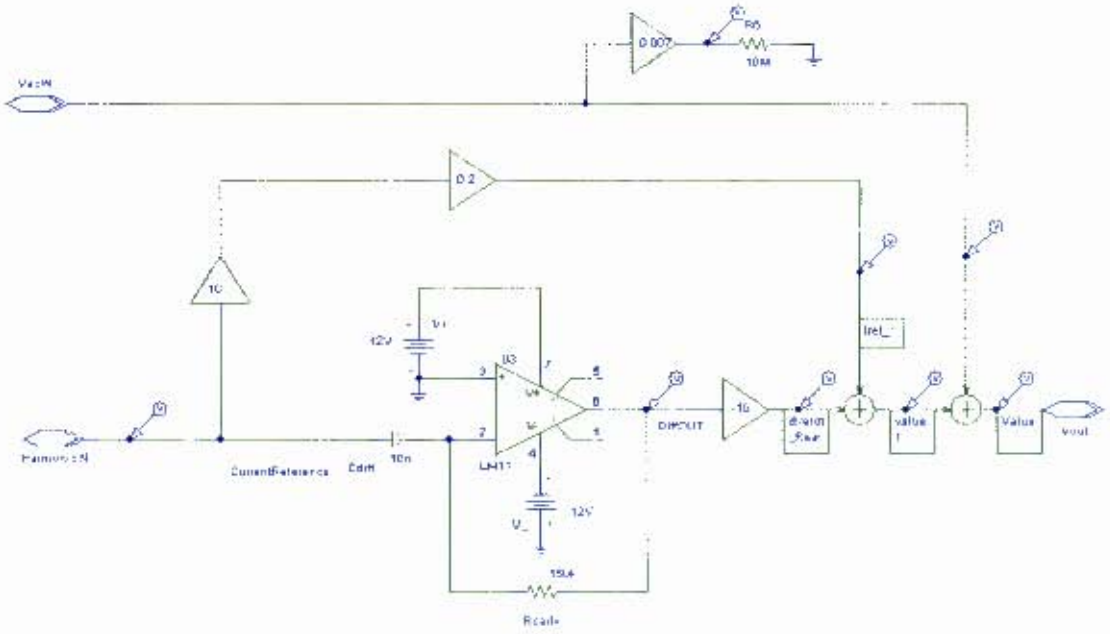

Figure 4-8 Inverter control voltage block

The circuit in figure 4-8 implements equation 3.12 using analogue components. As can be seen in figure 4-8, the physical differentiator simulates the voltage drop across the inductor. The differentiator is implemented using the LF411 IC. The differentiator has a gain equal to the value of the link inductor **L**r. The gain of 0.2 represents the voltage drop across the inductor resistance; **R**. Vac is added to the output representing the voltage drop across the source voltage, v_s. The circuit in figure 4-8 is however

implemented in the TMS320LF2407 digital signal processor in the laboratory set-up which is discussed in the next chapter.

5. Hardware Description

5.1 Introduction

In this chapter the hardware implementation of the 500 VA experimental prototype of the single phase shunt APF is presented. The system parameters used in hardware are kept very much the same as the parameters used in simulation. Firstly, the general laboratory set-up of the prototype will be discussed. This will be followed by the description of each building block of the prototype. Finally, the control system, which involves the use of a TMS320LF2407 digital signal processor (DSP) from Texas Instruments, will be discussed.

5.2 General description of experimental set-up

An overall diagram of the experimental set-up is shown in figure 5-1. Figure 5-2 shows the actual photo of the experiment in UCT's machines laboratory. The experimental prototype is supplied from a 240Vrms, 50 Hz distribution source coupled through an isolation transformer with ratio of 1:1. The full bridge diode rectifier is constructed using MUR860 diodes from MOTOROLLA and a DC smoothing capacitor.

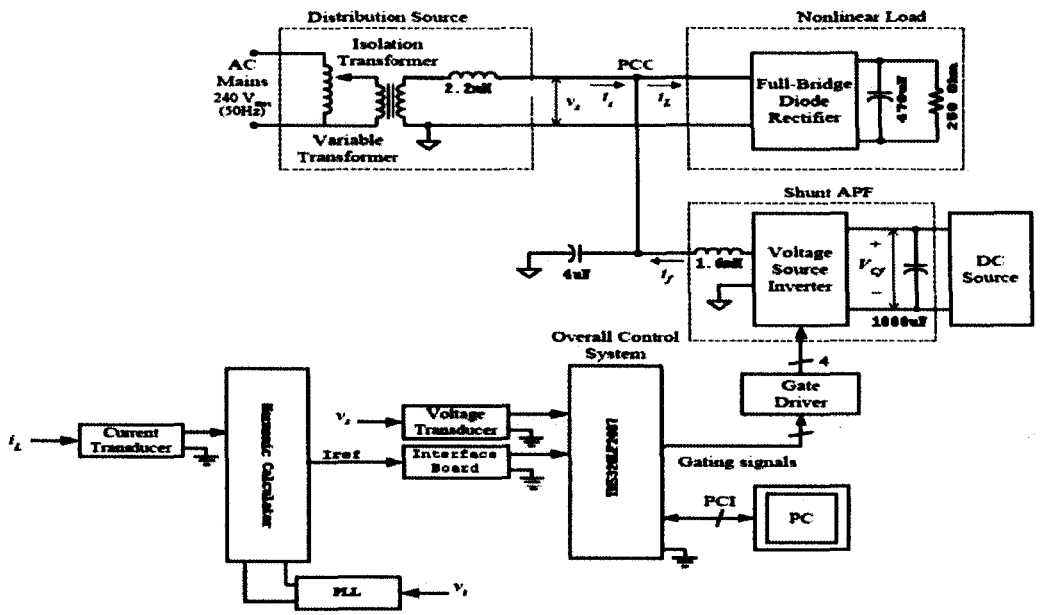

Figure 5-1 Block diagram of practical APF

The non-linear load is supplied by the source in order to generate non-linear current to be compensated by the APF. The diode rectifier load used is a purely resistive bank made from heater elements.

The APF is constructed using a full-bridge voltage source inverter (VSI), and a DC bus capacitor. The APF is connected in parallel with the non-linear load being compensated. One of the major components to be constructed in the practical APF is the inverter output low pass filter which is formed by the link inductor and the capacitor as shown in figure 5-1. The purpose of the filter is to remove the high

switching frequency of up to 10 kHz generated by inverter switching action. The values of the inductor and capacitor (LC) of the low pass filter were chosen in such a way that the cut-off frequency is 2.5 kHz. This will ensure that the switching noise is filtered out without filtering out vital harmonic components to be injected by the APF. This means that the APF can compensate for load harmonics up to the 25^{th} harmonic. (Note that all the other components used in the construction of the prototype are the same as those used in the simulation and the reason for choosing their values were discussed in the previous chapter).

To prove the effectiveness of the APF, the experimental results were taken without the capacitor's DC bus voltage PI controller; instead an AC supply ranging from 0 to 360 VAC is supplied via a variable transformer. The AC supply is connected through the AC-DC rectifier and supplied to the inverter.

The heart of the overall control system is the TMS320LF2407a DSP board which implements feed-forward control and PWM. The DSP is programmed to realize the switching signals of the VSI. It implements feed-forward control by accepting the reference current rich in harmonics which is calculated by the external analogue circuit. It also accepts the AC voltage measurement from the voltage transducer and computes the inverter's reference voltage. The voltage will ensure that the reference current is flowing through the link inductor, Lf. Finally, the DSP implements PWM in order to produce gating signals for inverter switching. The DSP is programmed in C++ code which can be found in appendix B. The DSP is linked to a laptop through an RS232 interface. Programming in C++ code is done using the dedicated MLT Drives DSP interface program version 2.07 compiler and linker. The executable object files and libraries are generated and loaded into the DSP's on-board memory

for real time execution. The signals fed into the DSP are sampled by the on-board analogue-to-digital converter (ADC), and passed onto the DSP for further processing.

5.3 Experimental Prototype construction

This section explains the construction of the experimental prototype in steps describing each circuit used. Figure 5-2 shows the actual experimental set-up of the prototype. The prototype consists of the VSI with DC bus made up from an AC to DC rectifier supplied through an isolation transformer and variac to vary the DC bus voltage between 0 to 360V DC. The DC-bus capacitor, rectifier load, TMS320LF2407 DSP, current and voltage transducers and the passive LPF. The power distribution system is represented by a full-bridge rectifier supplying a bank of resistors connected in parallel adding up to 250 ohms and supplied from a normal wall plug. The prototype parameters are tabulated in Table 5.1 below. The values and parameters of the experimental prototype are similar to those designed and simulated in Chapter 4.

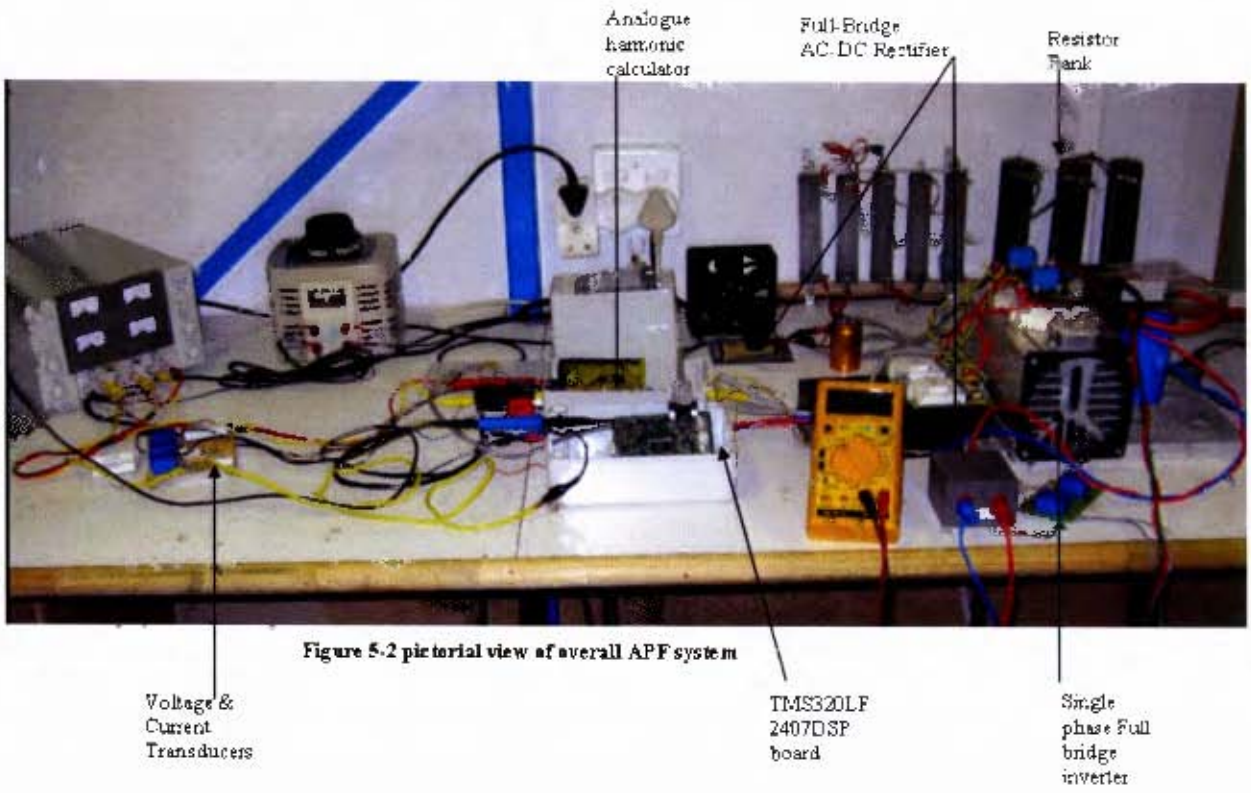

Figure 5-2 pictorial view of overall APF system

Figure 5-2 Pictorial view of overall APF system

Table 5.1 experimental prototype parameters

Parameters	Symbol	Value
Source Voltage	V_s	240 Vrms (50 Hz)
Rectifier Load Nominal Complex Power	S_R	500 VA
Rectifier DC smoothing capacitor	C_1	470uF, 400VDC
Load Resistor	R_L	250 ohm
Interfacing inductor	L_f	1.6mH
DC Bus Capacitor	C_f	1000uF
DC Bus voltage	VDC	230 VDC
LPF Capacitor	C_{LPF}	4uF, 400VAC
LPF inductance	L_{LPF}	1.6 mH

5.3.1 Non-linear load

The non-linear load is used in the experimental prototype is a single-phase full bridge diode rectifier. The type of diode used in the construction of the rectifier is the MUR860 diode from Motorola, which is capable of handling 60A at 800 Vrms (see datasheet in appendix A). The DC smoothing capacitor is a high performance, electrolytic long life capacitor. The capacitor has low equivalent resistance (ESR) and low equivalent series inductance (ESL). The rectifier is built on veri-board as shown in figure 5-3. No heat-sinks were used as only a small amount of heat (2kW) is dissipated.

Figure 5-3 Single phase converter circuit

5.3.2 Shunt active power filter

The shunt APF consists of the analogue harmonic calculator, the voltage source inverter (VSI), an interfacing LPF and control system. This subsection briefly describes the construction of sub-systems of the shunt APF.

5.3.2.1 Harmonic Calculator

The analogue harmonic calculator was built on a printed circuit board (PCB) and on perforated veri-board. The PCB was designed on TraxMaker™ which is a track design package in a simulation package called Circuit Maker. The track design is shown in appendix C. The actual completed circuits were housed in a non-conductive box as depicted in figure 5-4. All the components used are the same as the ones used in the simulation and the circuit diagrams can be found in appendix C. The only additional circuits that had to be constructed were the multipliers which were implemented using the AD633 integrated circuits (see datasheet in appendix A). The PLL to produce the sine and cosine templates were constructed from the sine template obtained from the source voltage measurement transducer. The sine template was then differentiated with an analogue integrator in order to produce the cosine template. Summers were also constructed using normal 741 operational amplifiers.

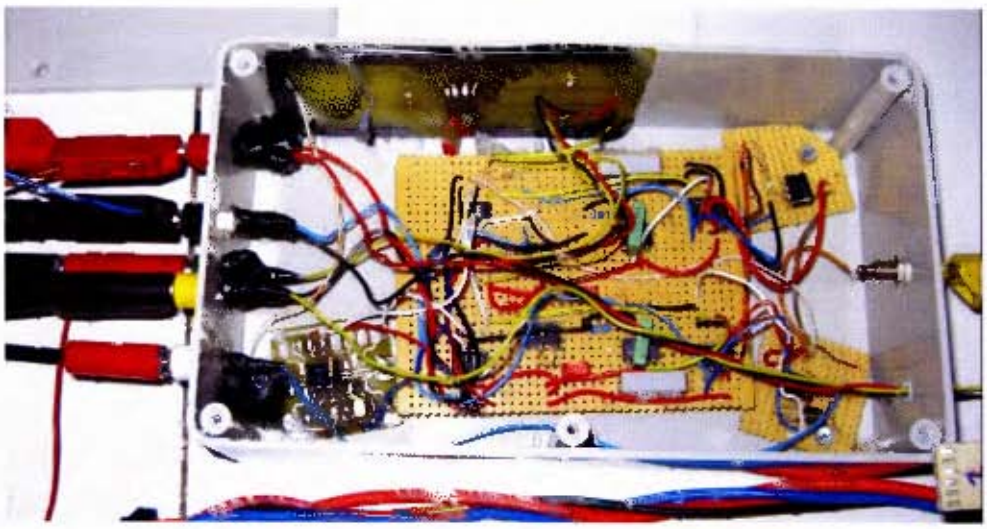

Figure 5-4 Harmonic calculator on PCBs and veri-board

5.3.2.2 Voltage Source Inverter (VSI)

Recall that the voltage source inverter is a power electronics device that converts DC voltage into AC voltage. The picture of the actual inverter used in the lab is shown in figure 5-5. Its output frequency and voltage can be varied by varying the gating pulses of the IGBTs. The PWM technique is used to produce the firing pulses for the IGBT switches. This technique was explained in detail in chapter 2. The peak value of the output voltage at the fundamental frequency of 50Hz from the inverter is given by the following formula [12].

$$Vinv = maVd \qquad (5.1)$$

where: $$Vd < Vinv < \frac{4}{\pi} Vd \qquad (5.2)$$

Ma is the modulation index which can be varied between 0 to 1 using a potentiometer. The potentiometer is connected via an ADC into the DSP in order to vary the amplitude of the output inverter voltage as shown in equation 5.1. An inverter comprises of two main parts, which are:

- The switching devices (Internal Gate Bipolar Transistors) and,
- the driver modules.

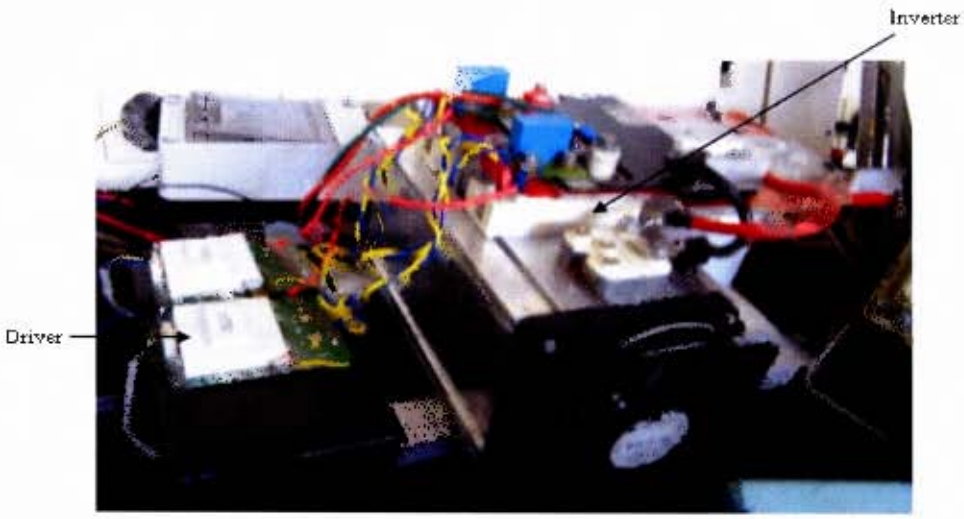

Figure 5-5 Semikron inverter and driver modules

IGBTs are good for DC voltages greater than 100V DC but suffer from low efficiency due to high volt drop (e.g.2-3 V), for voltages greater than 100V DC. The IGBTs used in the inverter depicted above are the SKM50GB063D from Semikron. The SKM50GB063D IGBT package contains two IGBTs forming one leg of the inverter. The driver modules are also from Semikron drivers. They are a special type of driver package called SKHI22B to run the dual IGBT package. These drivers have numerous protection schemes to protect both the IGBTs and the preceding control circuit. Data sheets for Semikron IGBT packages and drivers can be found in appendix A.

5.3.2.3 Link inductor

The link inductor which also forms part of the inverter output LPF is an important component in the APF construction. The value of the inductor used is 1.6mH. This device provides isolation between the output of the voltage source inverter and the power system where the APF is connected. The inductance allows the output of the active filter to look like a current source to the power system.

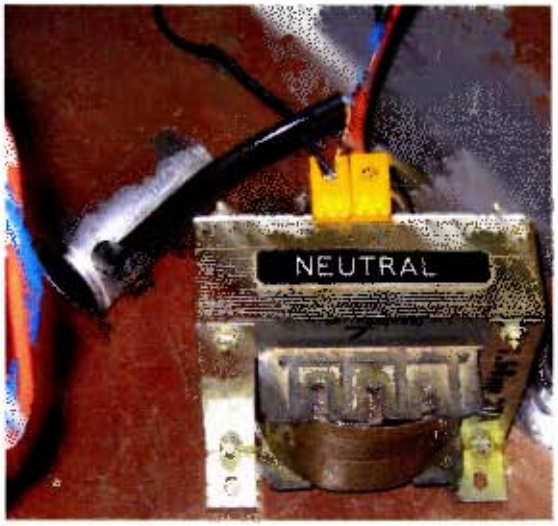

Figure 5-7 1.6mH link inductor

The value of 1.6mH was chosen in order to:

- Ensure that a maximum di/dt can be achieved by the filter and,
- to ensure adequate isolation from the power system and protection from transient disturbances.

(Please also refer to the previous chapter, section 4.3.4 to see how the value of inductance and filter capacitor was chosen).

5.4 Hall-Effect transducers

For power voltage and current measurements, a simple voltage divider could be used in order to obtain a scaled down version of say, a 240 VAC high voltage supply for micro-processing. Although this method is simple, there are two potential drawbacks. The measurement of high voltage causes the wire-wound resistors to heat-up causing it to deviate from its nominal value. The second important drawback is that there is no electrical isolation between the high voltage ground and the electronics circuitry. Thus, occurrence of transients on the high voltage side; such as spikes, noise etc., will be directly transmitted to the sensitive low-power circuits. The practical solution was to implement Hall-Effect LEM voltage and current transducers. The practical construction of the transducer circuits is shown in figure 5-8. For LEM data-sheets please refer to appendix A.

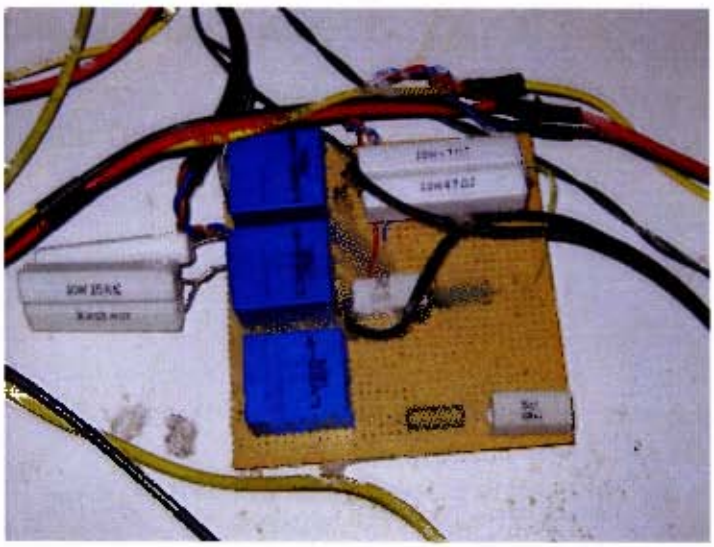

Figure 5-8 LEM transducers built on veri-board

5.5 TMS320LF2407 DSP board

The DSP board is used in this work to implement control action and to produce the pulses required to control the VSI using PWM. All control actions and calculations are performed in it in real time. The DSP used is part of the TMS320LF2407 family from Texas Instruments and is shown pictorially in figure 5-9 below. The board can be programmed in both assembly language or in C++. For this project it was programmed in C++. In comparison to hardwired component circuits, using a DSP has the following advantages:

- Fast response, resulting in higher performance.
- Increased reliability.
- Flexibility of control i.e., to upgrade or modify control algorithms.
- Costs less to implement.

See appendix B for the DSP data sheet and the interface card.

Figure 5-9 TMS320LF2407 DSP board with interface board

5.5.1 Features of TMS320LF2407 DSP

- 16-bit fixed point DSP running at 20MHZ.
- 32-bit registers to store real time data.
- Two hardware shifters to scale numbers independently of the CPU.
- Operates at only 3.3V, therefore low power consumption.
- Able to perform 20 million instructions per second (50 ns per instruction).
- Equipped with a 10-bit ADC and an 8-bit DAC.

5.6 Software development of the TMS320LF2407 DSP

This section describes the programme that implements the control algorithm executed by the DSP. The full code can be found in appendix B. The DSP is equipped with an analogue to digital converter (ADC). The ADC is used to instantaneously measure three input signals – two voltage signals and one current signal from the voltage and current transducers respectively. The DSP uses these measurements to calculate four PWM pulses after implementing feed-forward control. The second analogue voltage signal is a 0 to 2.8V DC signal which is adjusted by a potentiometer in order to vary the modulation index. This is used to vary the amplitude of the AC sine wave of the inverter output to ensure that the inverter output is kept slightly higher than the grid voltage.

5.6.1 Programme structure

The programme structure is based on the sampling cycle of the general purpose timer (GPT1) of the DSP. The timer provides the time base required for PWM generation, ADC sampling and coordinates all other control loops. In this programme, the frequency of Timer 1 is set to 10 kHz which gives a period of 100 micro-seconds. The timer operates in continuous up/down counting mode. Interrupt mask registers IMR and EVIMRA are configured to allow Timer 1 to generate an interrupt on underflow, i.e., when Timer 1 value is zero.

5.6.1.1 Main program chart

The flow chart of the main program is shown in figure 5-6. The task of the program is to initialize all variables, to enable desirable registers and interrupts and to mask unused interrupts. When this has been done, timer 1 is then enabled. This program is a background routine that ensures that the main program has defined bounds.

5.6.1.2 Interrupts

Two interrupts named INT2 and INT6 which occur on different interrupt levels have been defined. When the CPU is interrupted, the background operation of the main program is stopped and the interrupt level is determined. A context save of important registers is carried out before branching to the respective interrupt service routines.

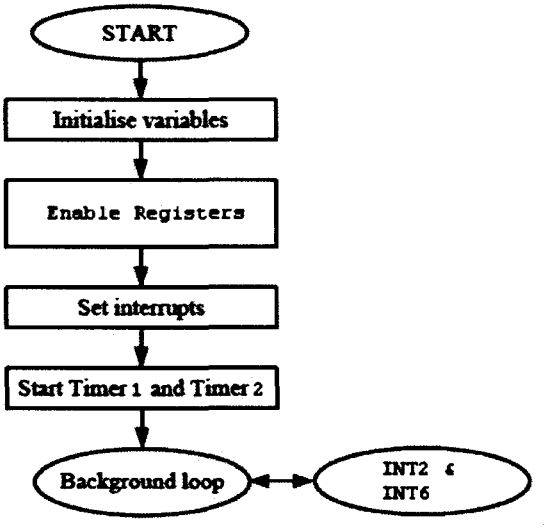

Figure 5-10 Initialisation routine flow-chart

5.6.1.3 INT2 Interrupt service routine

INT2 is the program that reads all the ADCs and carries out all control loops. The source of this interrupt is Timer 1 underflow. This program is listed in appendix B. The code begins by the ADC reading the current values from the analogue harmonics calculator and the source voltage. The source voltage is also sampled and read by the ADC. It then calculates the real values of these signals. The sampled signals are then reverse calculated to produce their real values (i.e., before passing through the voltage/current transducers and the DSP's interface board). The algorithm for implementing feed-forward control is then executed which results in the reference voltage, Vref. The flow chart of this routine is illustrated in figure 5-11 below. The reference voltage is then passed onto PWM registers to produce switching pulses for

the inverter. The pulses produced by the DSP have peak amplitude of 5V. However, the IGBT drivers can only accept voltage between 15V and 30V. Therefore, a level shifter is installed between the DSP and the driver which shifts the DSP output voltage from 5V to 15V.

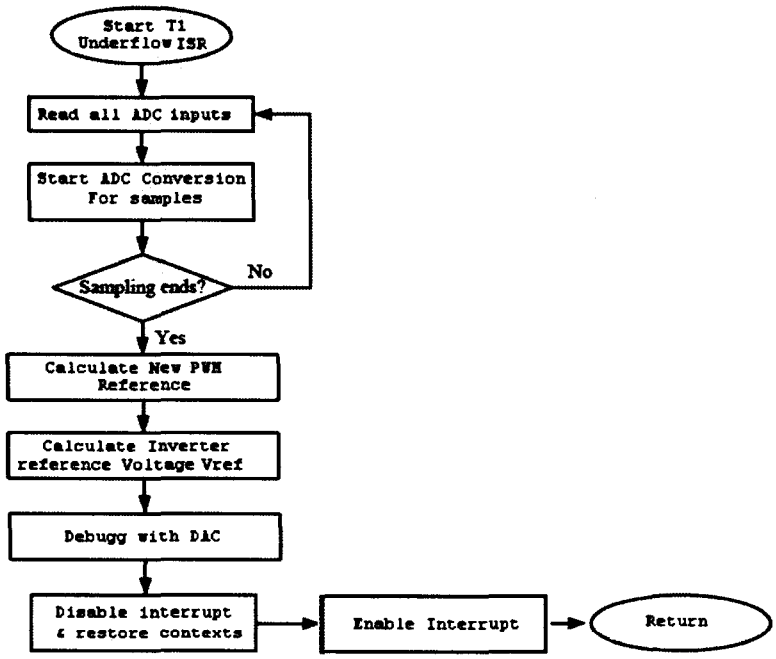

Figure 5-11 Flow diagram of INT2 service

It should be noted that some of the results that will be shown in the next chapter were obtained from the 8-bit DAC which is also used for debugging the code. The actual program is detailed in appendix B.

6. Simulation and Hardware Results and Analysis

6.1 Introduction

In chapter 4, the Orcad Pspice simulation of the APF was discussed. This was followed by the description of the hardware for the prototype construction. In this chapter, the experimental results will be presented and analysed with reference to the simulation, in other words; the results of the laboratory prototype will be assessed using the simulation results as the benchmark. The practical experiment measurements were taken using the oscilloscope from Agilent Technologies. It also became necessary to make use of the QualiStar power quality analyser from Chauvin Amoux to perform power quality analysis.

To begin with, the results of the system will be shown before compensation. This will be followed by the depiction of results after the active filter is connected to the distribution system via an isolation breaker. The overall effect on the power distribution system, (also referred to as the grid), under the compensation of the shunt APF will be shown. Special emphasis is placed on the discrepancies between the simulation results and the experimental results. Finally, analysis of the total harmonic distortion (THD) before and after compensation will be carried out.

6.2 Results before compensation

Figure 6-1 shows the resultant waveforms when a single-phase 500VA full-bridge diode rectifier with a 250 ohm resistive load is applied to the distribution system. The waveforms come from the simulation circuit in figure 4-1 without compensation. As shown, the resulting source current is distorted resulting in poor power factor. The total harmonic distortion of the source current is 42%.

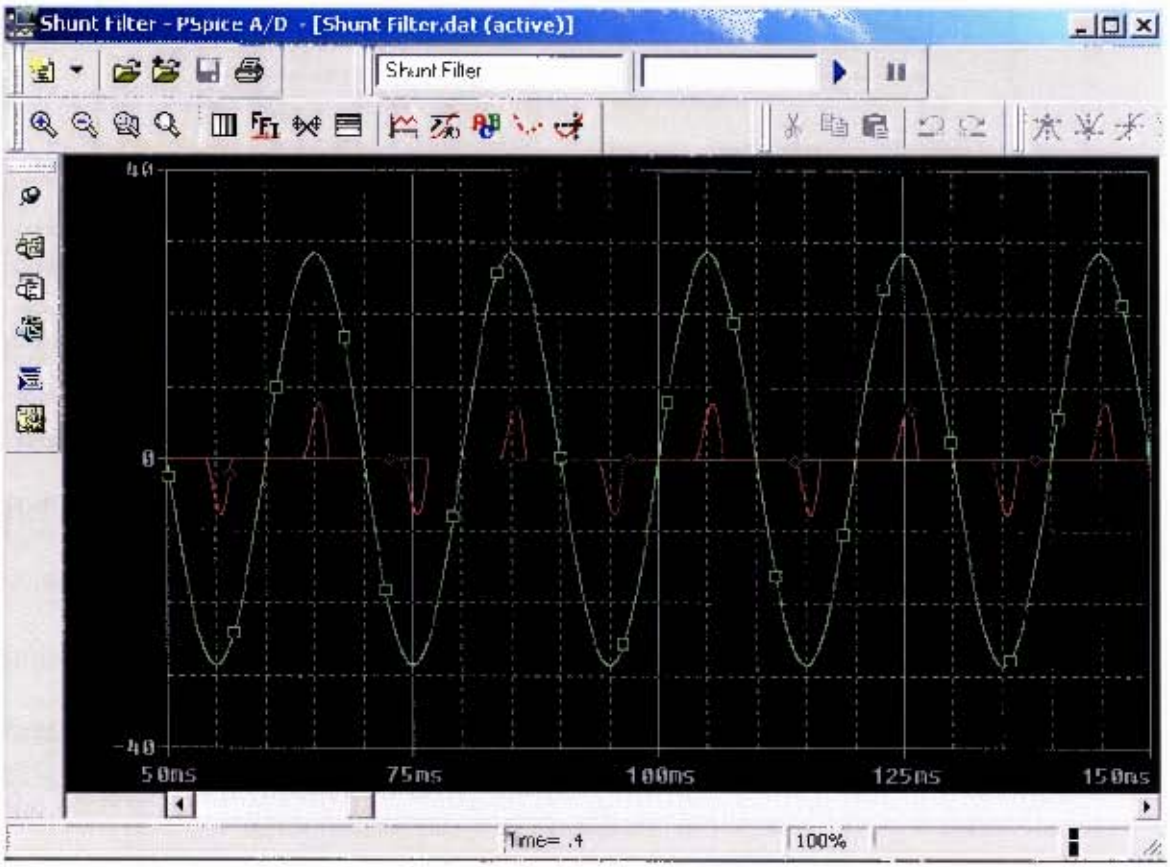

Figure 6-1 Simulation - source voltage and source current waveforms without compensation

The practical experiment source voltage and source current waveforms with similar operating conditions are shown in figure 6-2. It can be seen that the experimental results are in close agreement with the simulation results shown in figure 6-1. These waveforms were obtained using the power quality analyser.

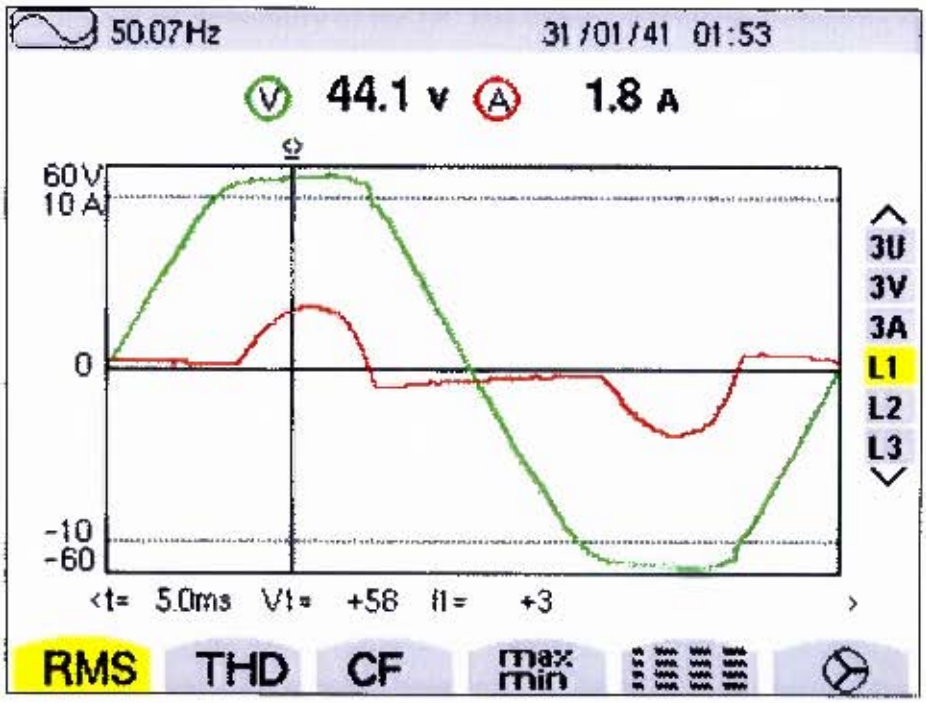

Figure 6-2 Practical - source voltage and source current waveforms without compensation

6.2.1 Synchronising APF to power distribution system

After the APF circuit was set up, the next step is to connect the inverter to the grid. Before the inverter can be connected to the power distribution system it has to be synchronised, i.e., the phase, frequency and amplitude of the inverter output voltage must match with that of the grid voltage. This is accomplished by using an isolation breaker between the inverter output and the grid. The two voltages on either side of the breaker are measured and displayed on the oscilloscope as shown in figure 6-3. The grid voltage is adjusted by means of a variac up to about 90V RMS. Then the DC bus voltage is adjusted until the inverter output voltage is of same amplitude as the grid voltage. The inverter isolation breaker is then closed enabling the inverter to be connected to the grid. It should be noted that the load angle between the inverter output voltage and the grid i.e.,σ was kept constant to prevent real power flow. This could be done since the losses incurred in the inverter are compensated by the DC source.

Therefore there is no possibility of the DC bus capacitor voltage decreasing suddenly. (Note that a PI regulator is not employed in order to vary the load angle between the inverter output voltage and grid voltage to send or receive power for the purpose of keeping the voltage across the capacitor constant. In this case, constant DC source is applied across the DC capacitor).

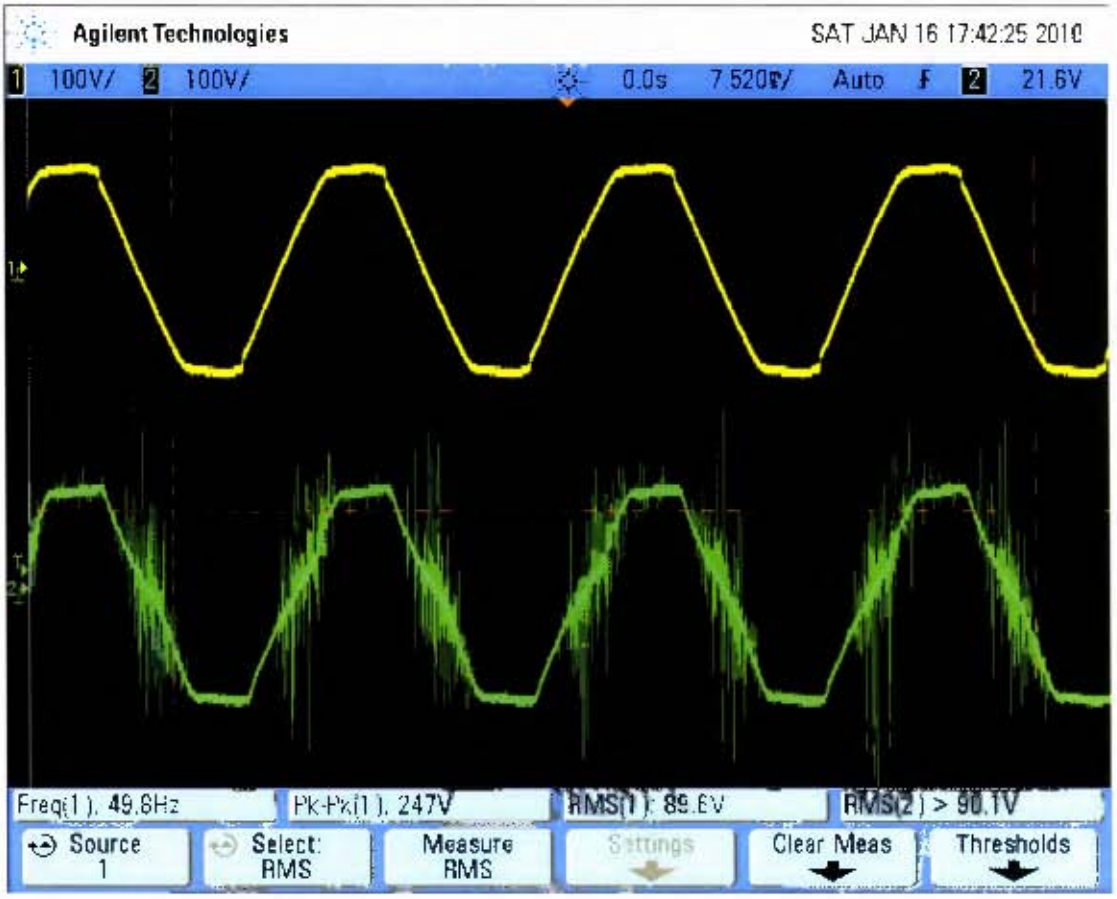

Figure 6-3 Practical - synchronisation of inverter to grid

Figure 6-4 depicts the source voltage and inverter output voltage after synchronisation. The latter is read from the DSP's 8-bit DAC. As shown in figure 6-4; the inverter output voltage carries the compensation current I_f which is rich in harmonics. Thus the inverter voltage waveform is distorted compared to the source voltage.

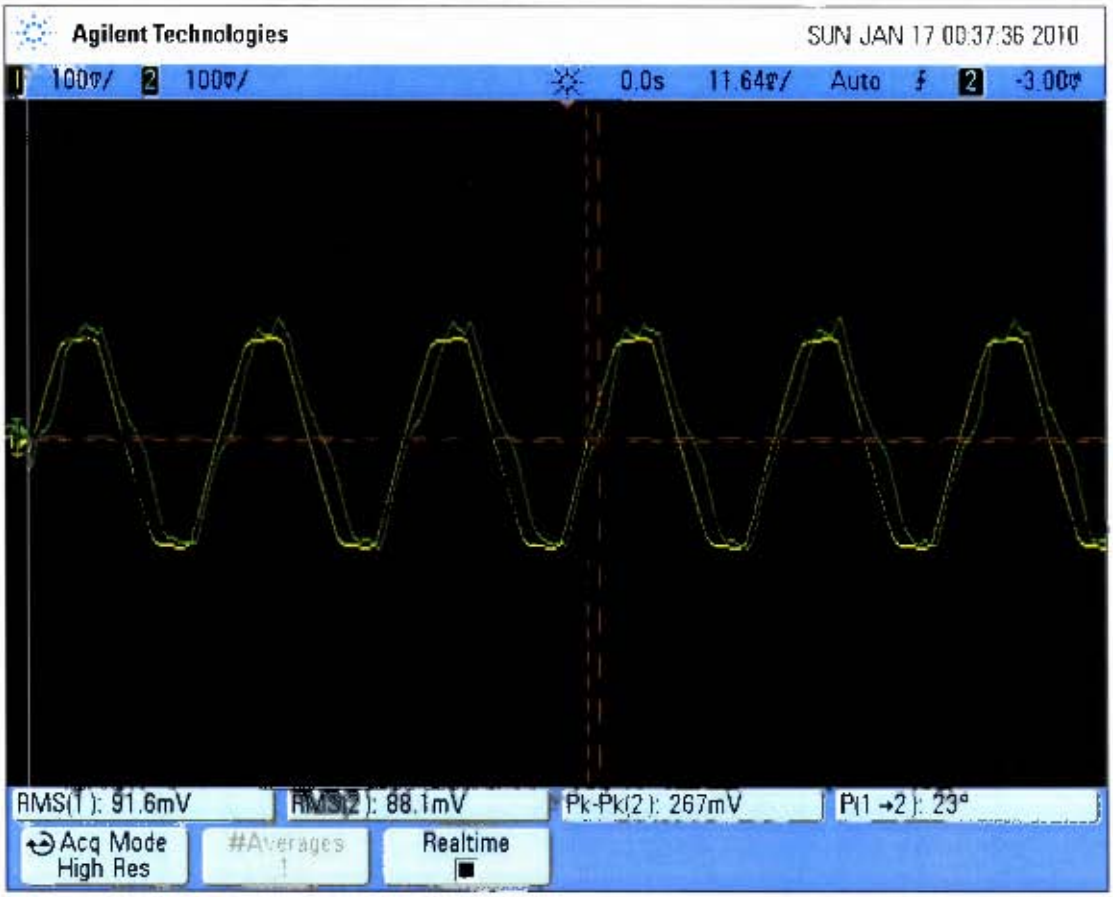

Figure 6-4 Practical - inverter and grid voltage after synchronisation

6.3 Sine-Cosine generation (PLL) for control circuit

Figure 6-5 shows the simulated source voltage and phase-lock loop (PLL) generated reference sine waves, (sin (wt) and sin (wt-90°)). Recall that PLL is used to generate the reference compensation current i_{ref}. The waveforms produced must be one unity sine-wave synchronised to the source voltage and a 90° phase shifted sine-wave, (sin (wt - 90°)). The cosine is obtained by delaying sin (wt) by 90° using an analogue integrator.

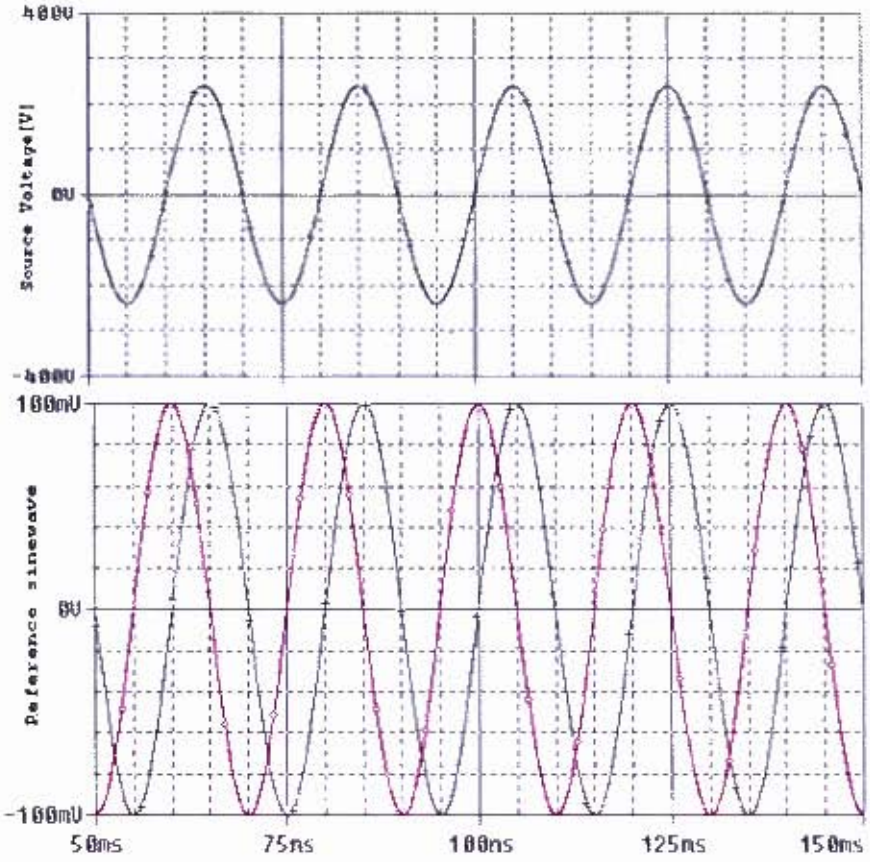

Figure 6-5 Simulation - PLL generated reference sine waves and source voltage

The PLL reference waves, (sin (wt) and sin (wt-90°)) generated by the practical PLL is depicted in figure 6-6. The practical PLL was generated by shifting a sample of the source voltage to create the cosine waveform.

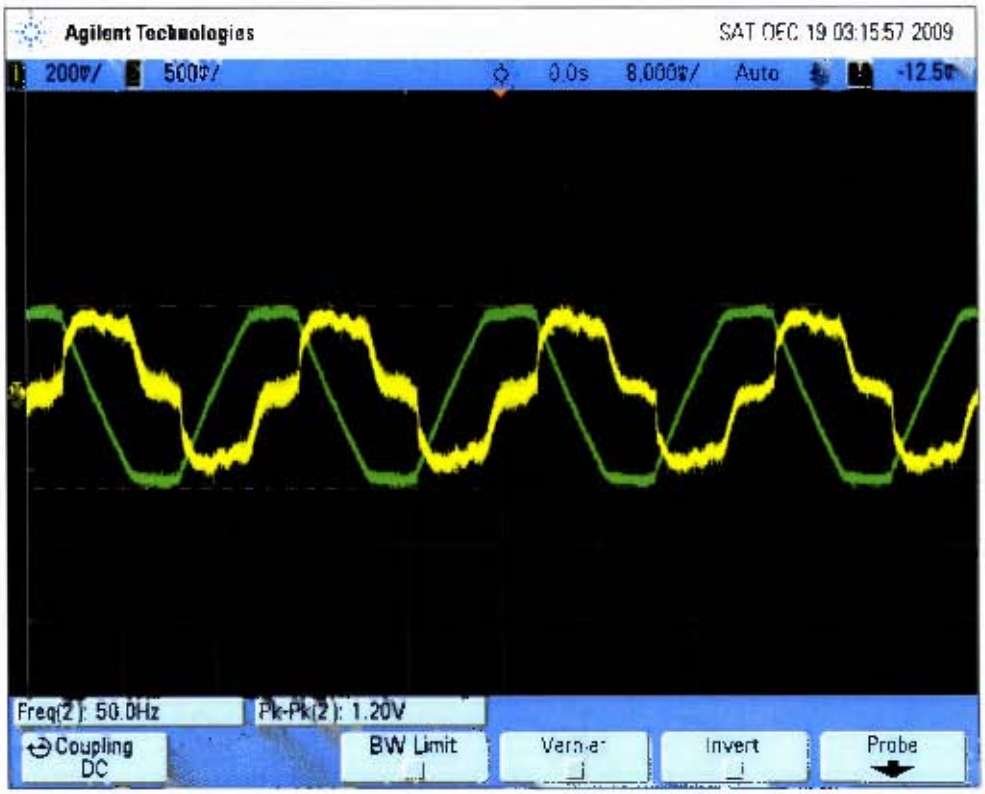

Figure 6-6 Practical - PLL generated reference sine waves

6.4 Compensation current reference estimation

In this section, the results for the estimation of compensation reference current are shown. The reference compensation current is generated by the circuit of figure 4-3 in the simulation and figure 5-4 in the practical. Figure 6-7 shows the simulated results of the APF's harmonic calculator using the sine multiplication theorem. The compensation current reference can be decomposed into active current, reactive current and harmonic current or non-active current as shown in figure 6-7.

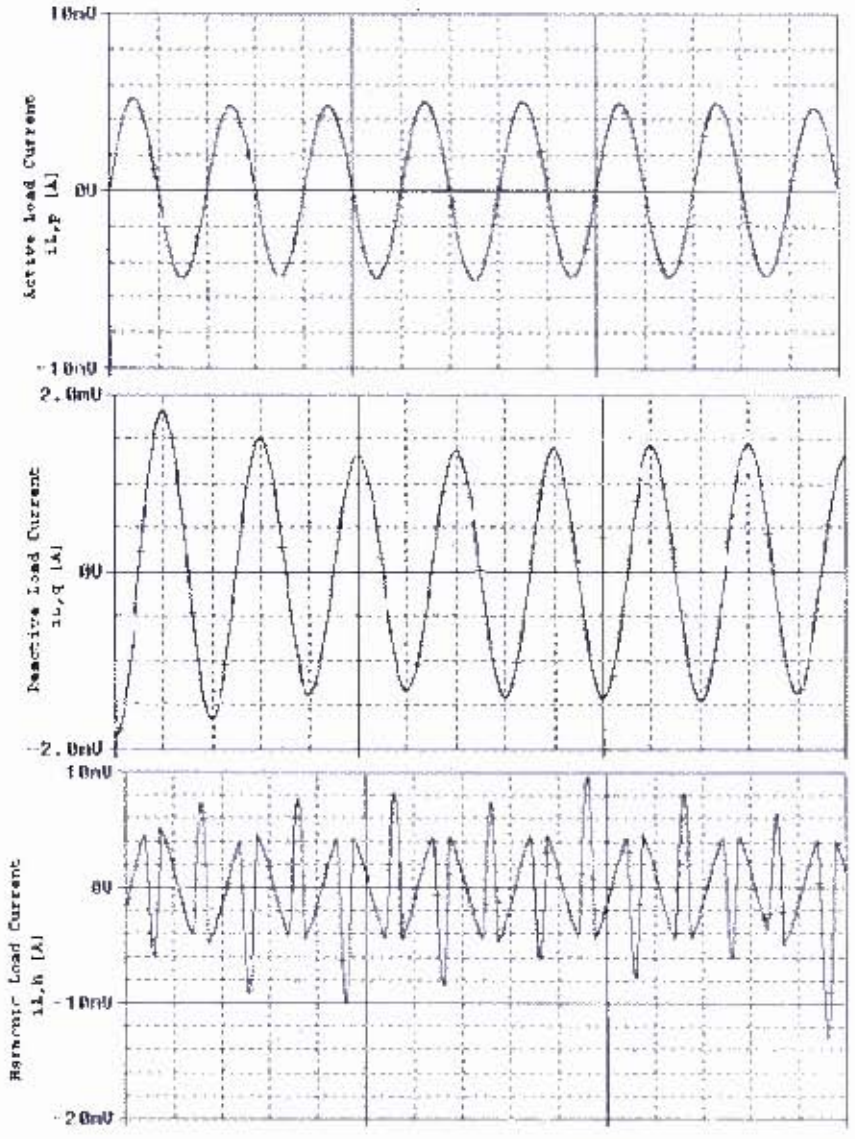

Figure 6-7 Simulation - active, reactive and harmonic load components

As can be seen in figure 6-7, the active load current $i_{L,p}$ is in phase with the source voltage v_s, while the "non real" load current component $i_{L,q}$ lags $i_{L,p}$ by 90°. Recall that the harmonic load current is obtained by simply subtracting the fundamental active and reactive current components from the total load current as was shown in equation 3.8. The experimental results of the reference compensation current i_{fref} and the load current i_n, are shown in figure 6-8. As can be seen, the experimental results match very well with the simulation results. The practical results in this case are measured from the output of the 8-bit DAC of the TMSLF240A DSP.

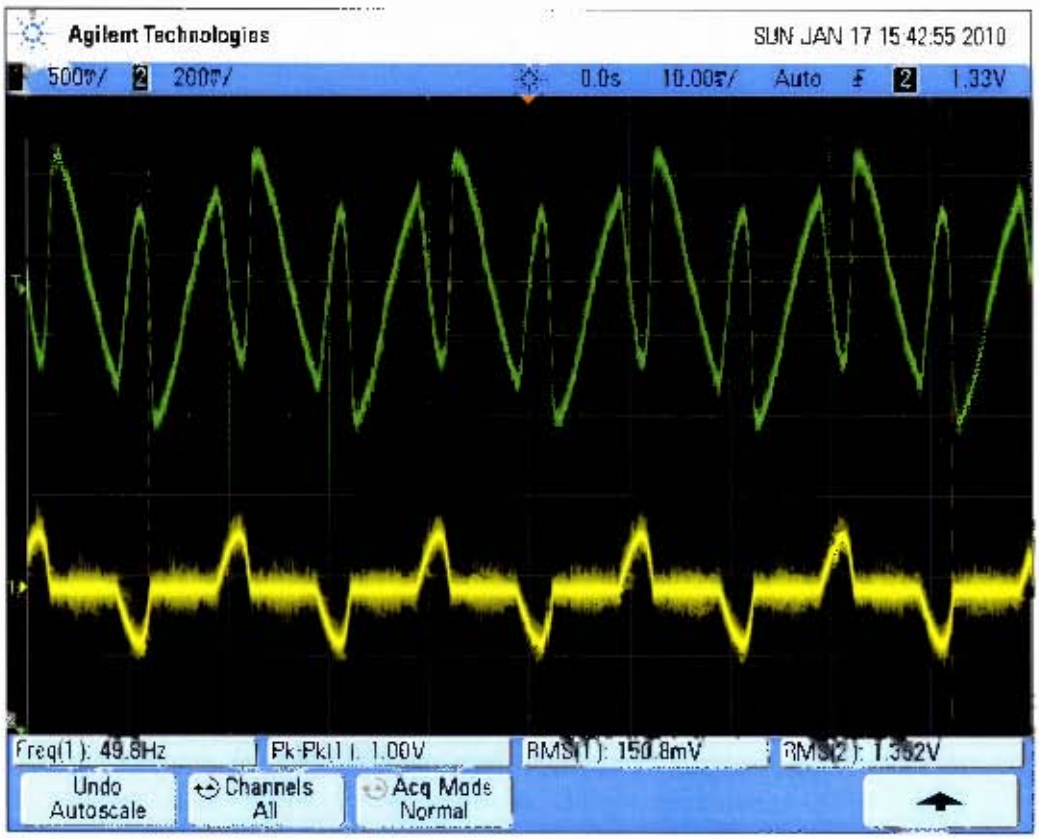

Figure 6-8 Practical - compensation current (top) and source current (bottom)

Recall that the theory of feed-forward control assumes that the generated reference current produced in the previous sampling period was successfully tracked by the controller. Therefore, the compensation current to be produced in the next cycle is known prior. Therefore, a corresponding reference voltage is produced which will result in the reference current i_{fref} flowing in the output of the inverter as i_f. The

reference voltage is produced using equation 3.15. Figure 6-9 depicts the reference voltage that is worked out from the reference current which is then added to the sample of the source voltage, v_s to produce the inverter's reference voltage which will result in the compensation current, i_f flowing at the PCC. The waveform of figure 6-9 is read from the output of the 8-bit DAC of the TMSLF240A DSP.

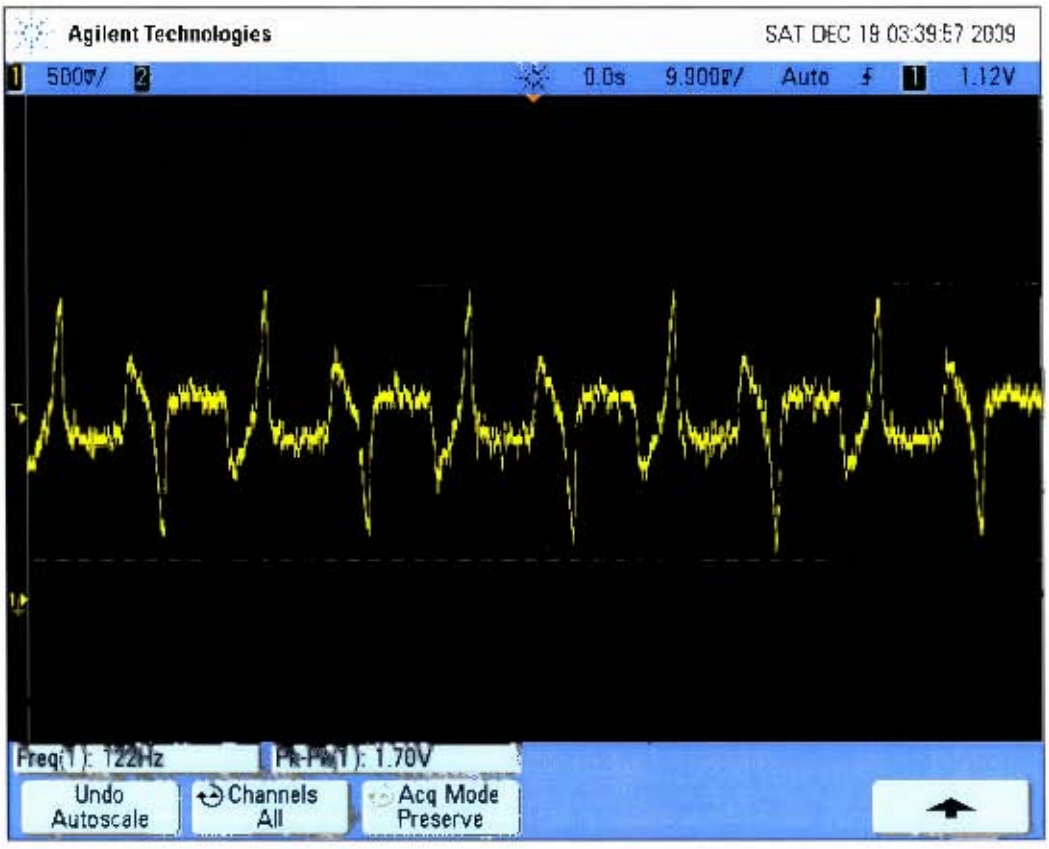

Figure 6-9 practical - reference voltage waveform before adding to VAC (see eq. 3.15)

The output current, i_f of the inverter was measured together with the inverter output voltage, V_{inv} depicted in figure 6-10. This is after the APF is connected to the grid through the link inductor. As can be seen from figure 6-10, the output current of the inverter, i_f resembles the reference current i_{fref}. The compensation current waveform was measured from the current LEM transducer.

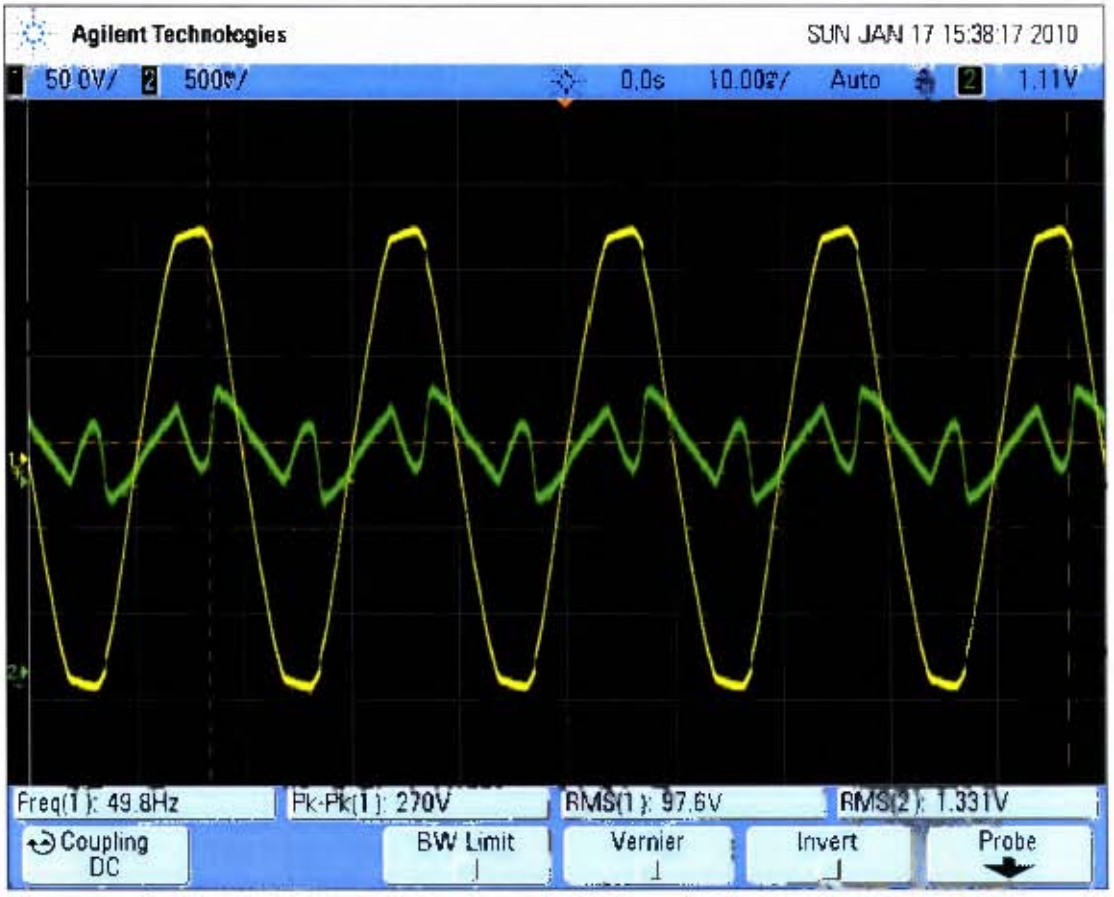

Figure 6-10 Practical - inverter output voltage, V_{inv} and compensation current, i_f flowing through the link inductance, L_f

6.5 Results – control scheme

In the previous section, the current components of the compensation current reference i_{fref}, were obtained. This section illusrates the effectiveness of the feed-forward controller to track the reference current. The control objective is to ensure that the compensation current i_f follows the estimated current reference i_{fref}.

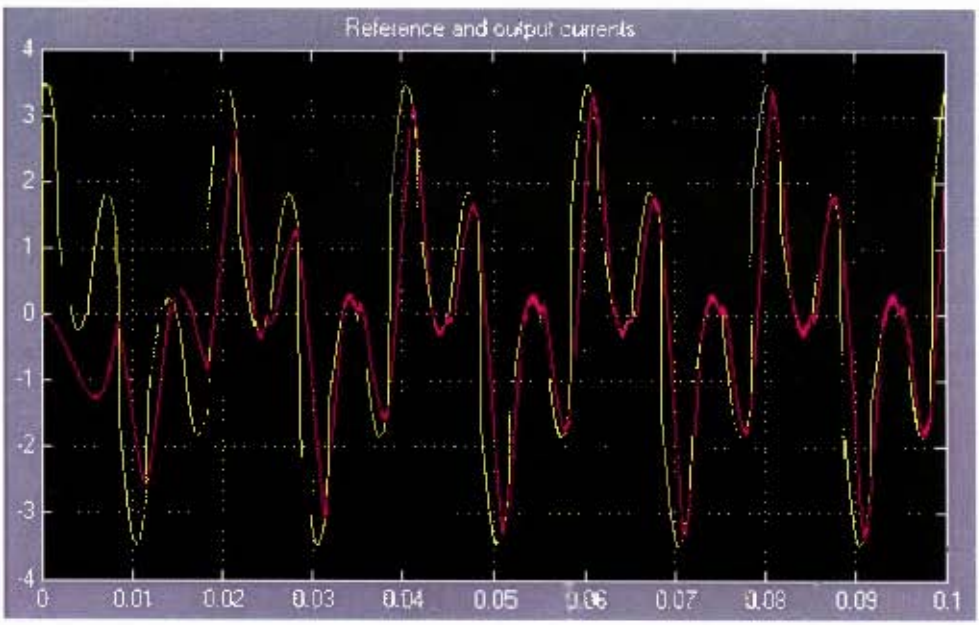

Figure 6-11 Simulation - reference and APF compensation current

As shown in figure 6-11, the controller reaches steady state at 2mS. After 2mS the inverter output current, i_f (shown in purple in figure 6-11) is following i_{fref} very well.

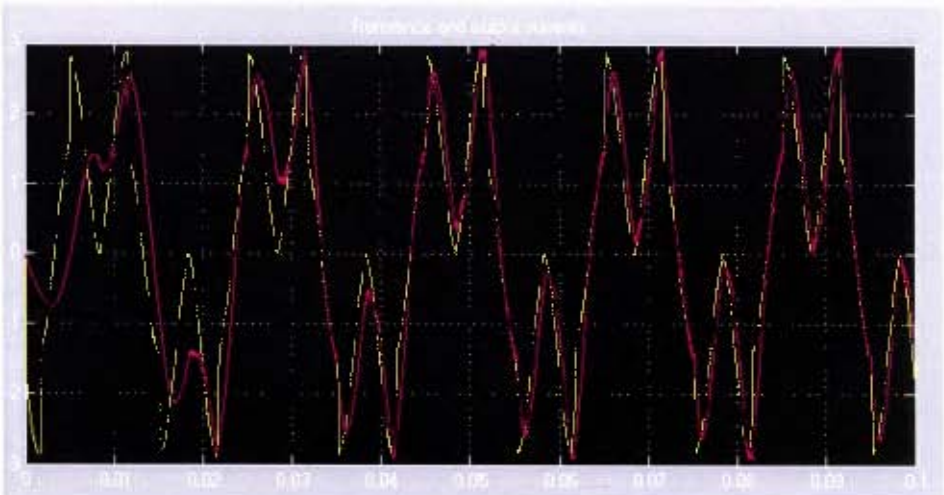

Figure 6-12 Simulation - distorted reference and APF compensation current

To further demonstrate the effectiveness of the controller, the waveform shown in figure 6-12 was put as a reference into the controller (reference is shown in yellow in figure 6-12). The inverter output current, i_f (shown in purple in figure 6-12), still followed i_{fref} very well which proves the effectiveness of the control scheme. Note that the controller reaches steady-state after about 2mS mainly due to the large DC link capacitor initially having to charge up to capacity.

6.6 Results of APF shunt compensator

Figure 6-13 shows the source voltage v_s, and source current i_s, waveforms before and after compensation. The shunt APF is introduced at the PCC via the isolation circuit breaker. The injected compensation current i_f forces the source current i_s to become sinusoidal. Figure 6-13 shows the case where the shunt APF is switched on at PCC after 300 milliseconds (to ensure that the APF is operating at steady state). When the current is injected; the source voltage v_s, remains invariant. However, the source current waveform becomes sinusoidal. This shows that the source is no longer supplying current harmonics to the load but that nearly 100% of the harmonics are supplied by the APF.

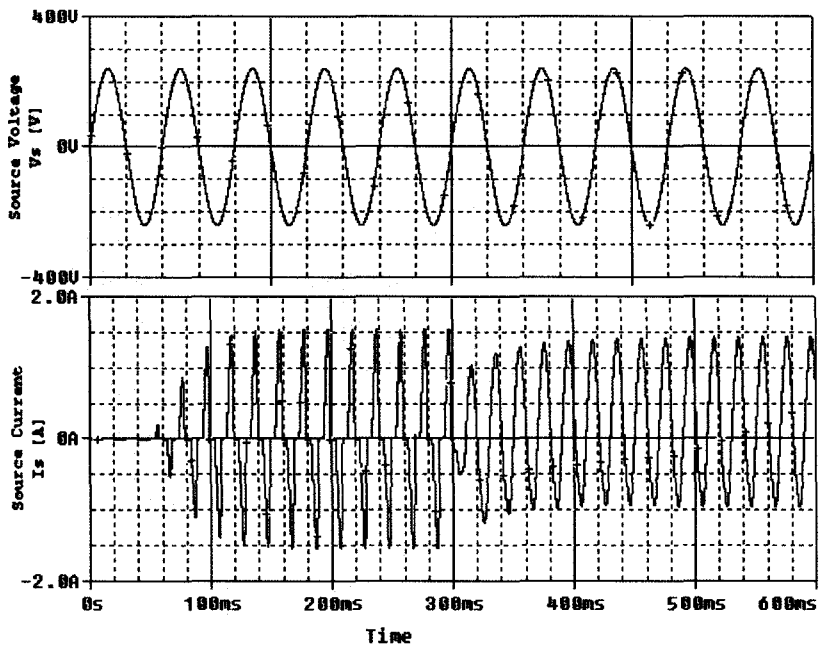

Figure 6-13 Simulation - APF switched on at 300mS

Figure 6-14 further validates the effectiveness of the APF by demonstrating that the load current also remains invariant proving that the load still operates normally while the compensation current is injected, (compare these results with the ACCUSINE APF from Schneider in section 2.3.1). The source current is sinusoidal due to the fact

that there is virtually zero harmonics required from the source. The waveforms in figure 6-14 were recorded from 100mS to 300mS.

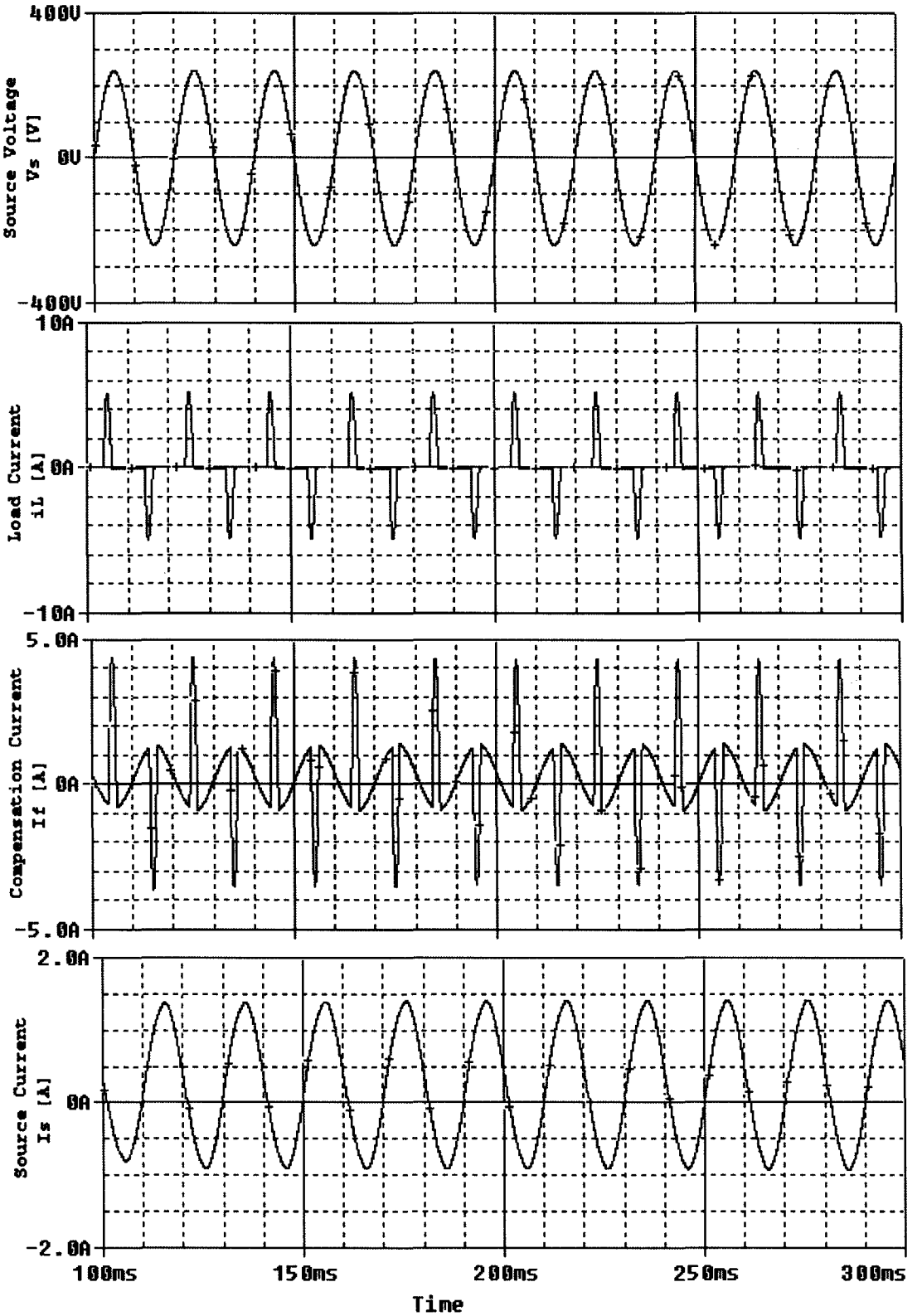

Figure 6-14 Simulation - basic shunt APF compensation showing main waveforms

The experimental result of the basic shunt APF compensation scheme is shown in figure 6-15. The APF isolation breaker was closed after a few seconds to allow the DC-bus capacitor to charge up fully and stabilize. Figure 6-15 indicates that the resulting source current is sinusoidal and in phase with the source voltage. The THD of the source voltage changed from 5% to 6.6%. This is due to the leakage of harmonic currents through the source impedance. However, on the other hand; the THD of the source current has improved from 42% to 8.5% as can be seen in the results obtained using the power quality analyser in figure 6-16.

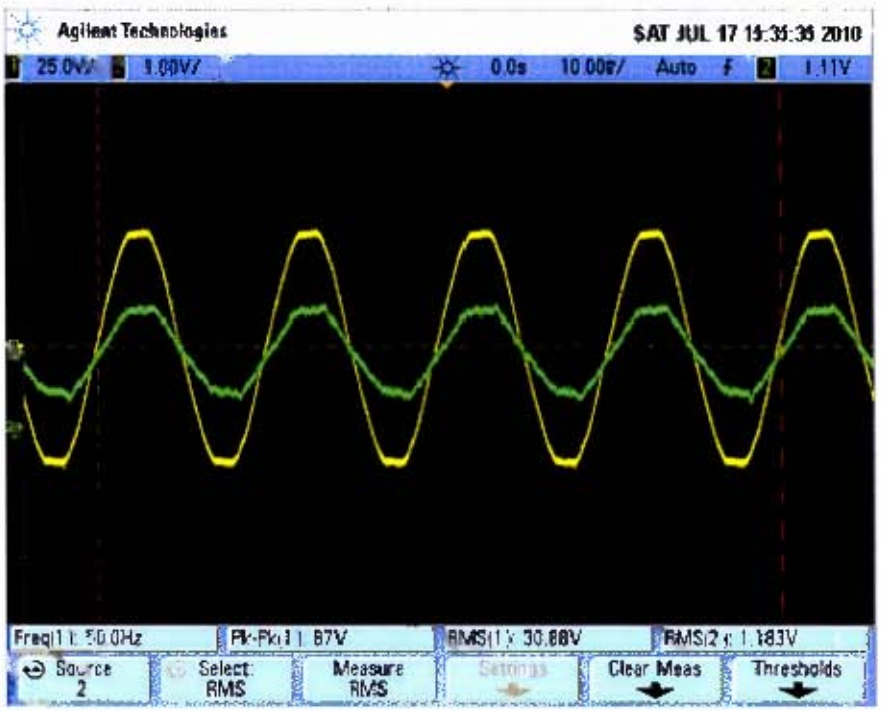

Figure 6-15 Practical - source current and source voltage after compensation

As can be seen in figure 6-16 the voltage (green) and current (red) waveforms are in phase. This implies that the power factor has improved to nearly unity and the harmonics have been virtually eliminated. As it was explained above, due to the absence of the PI regulator in the DC link, the DC-bus voltage has to be increased manually in order to increase the amplitude of the compensation current - thus improving the performance of the APF. However, for practical reasons the DC-bus voltage was kept minimal at 180V DC.

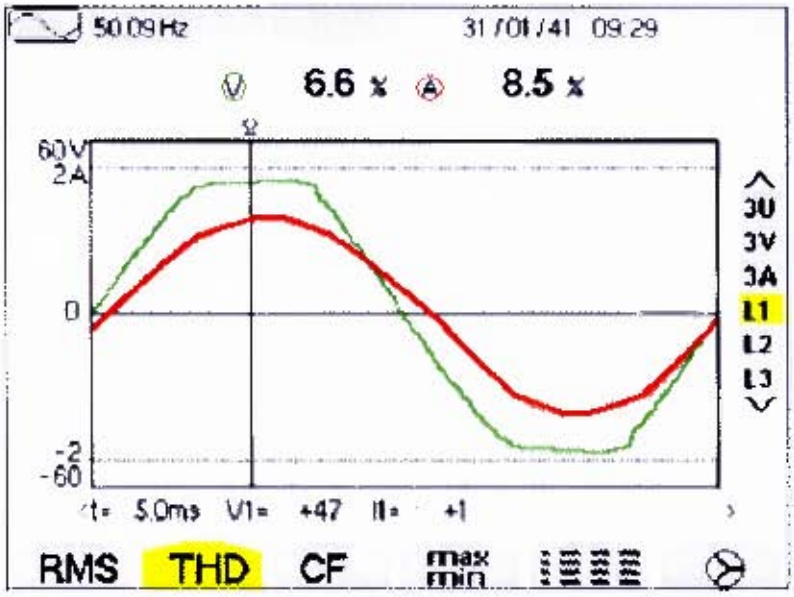

Figure 6-16 Practical - source voltage and current after compensation

6.7 Harmonic Distortion Analysis

The total harmonic distortion (THD) is the most expedient indicator of the quality of AC waveforms. In this section, the Fast Fourier Transform (FFT) is used to analyse the harmonic spectrum of the source current under different compensation conditions. Thereafter, the THD of both the simulation results and experimental results is carried out.

The spectrum of the source current without compensation is shown in figure 6-17. From the spectral plot, it can be seen that the source current contains large amounts of harmonic current components of frequencies up to 1kHz. However, the current component with the highest amplitude is the 3rd harmonic (150 Hz).

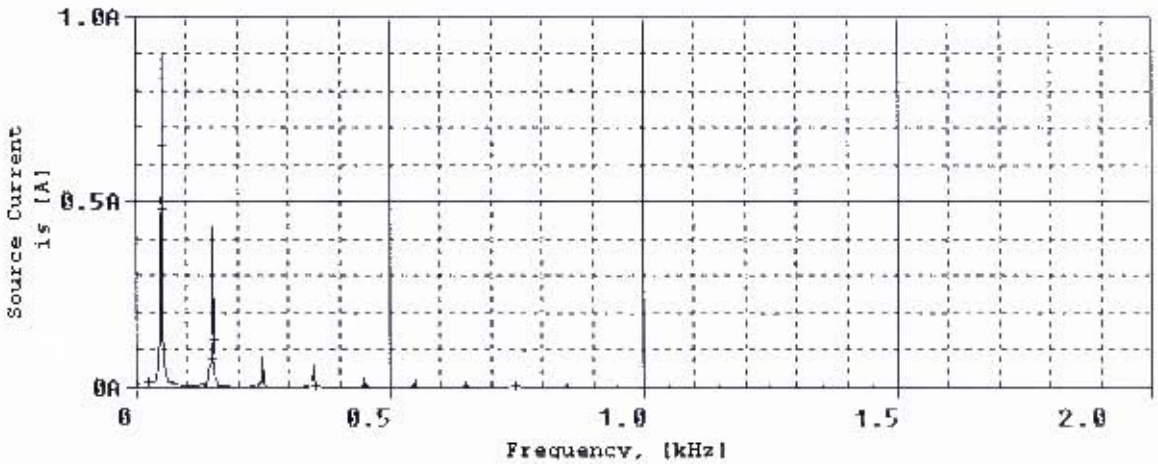

Figure 6-17 Simulation - frequency spectrum of source current without compensation

Figure 6-18 shows the experimental results of the source current and voltage before compensation. The voltage waveform has a moderate THD of 5.2% whereas the current waveform has a high THD of 42%. Figure 6-19 shows the FFT of the source current frequency spectrum. It can be noted that the odd harmonics (i.e. 150 Hz, 250 Hz, 350 Hz... 1kHz) of the experimental source current spectrum has larger amplitude compared to those of the simulation. This can be attributed to the deviation

of component parameters between the simulation model and the experimental prototype. However, as can be noted, the trend is consistent.

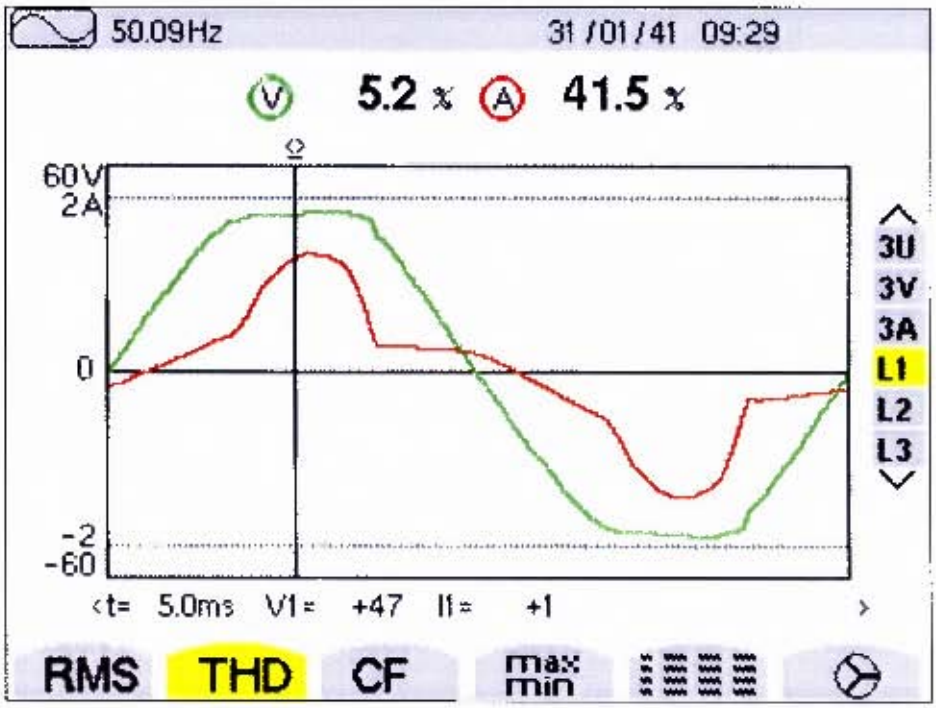

Figure 6-18 Practical - source voltage and current before compensation

Figure 6-20 shows the frequency spectrum of the source current under ideal compensation conditions.

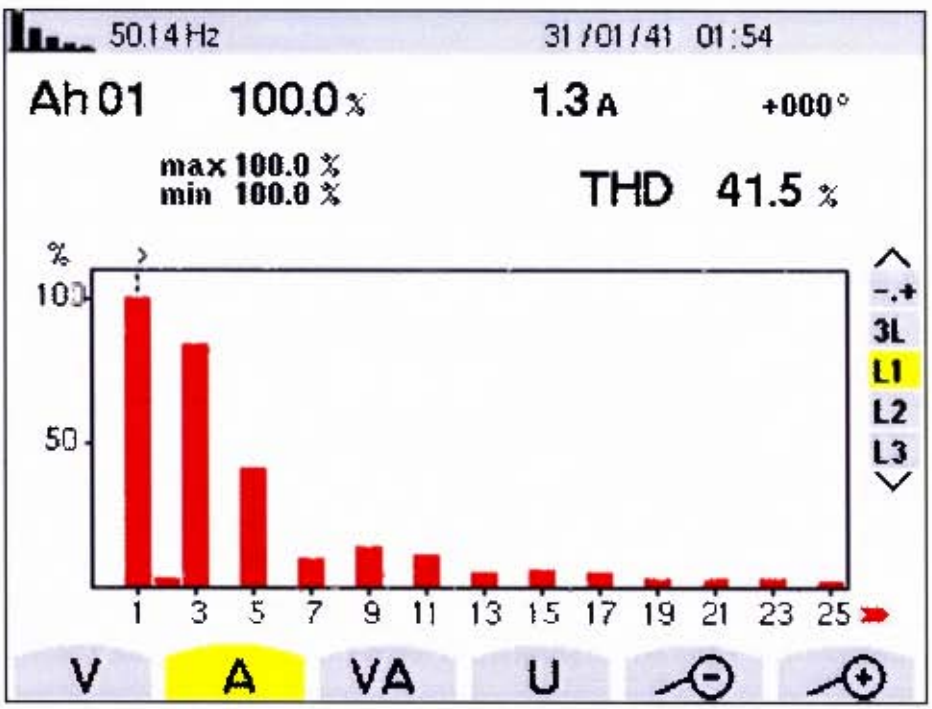

Figure 6-19 Practical - frequency spectrum of source current after compensation

When comparing the frequency spectrum of the source current in figure 6-17 with that of figure 6-20, it is evident that the source current is effectively free of harmonics. This clearly indicates that the proposed compensation scheme works well without the influence of external disturbances and noise.

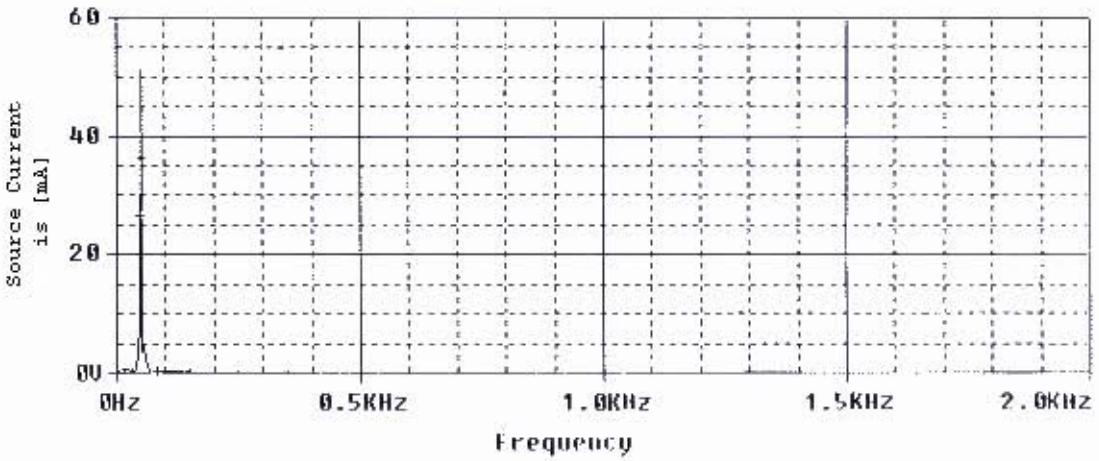

Figure 6-20 Spectrum of source current under ideal compensation conditions

The spectrum of the source current under non-ideal conditions is shown in figure 6-21 for the simulation results and in figure 6-22 for the experimental results. It is clearly evident that the shunt APF successfully filters the harmonic current components proliferated by the non-linear load under simulation and in the practical laboratory prototype.

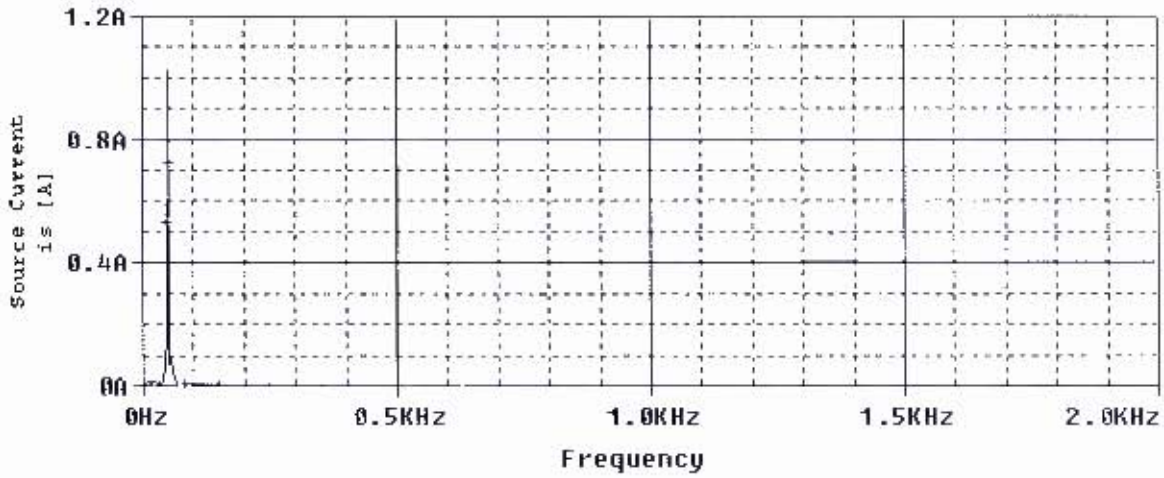

Figure 6-21 Simulation of source current frequency spectrum under APF compensation

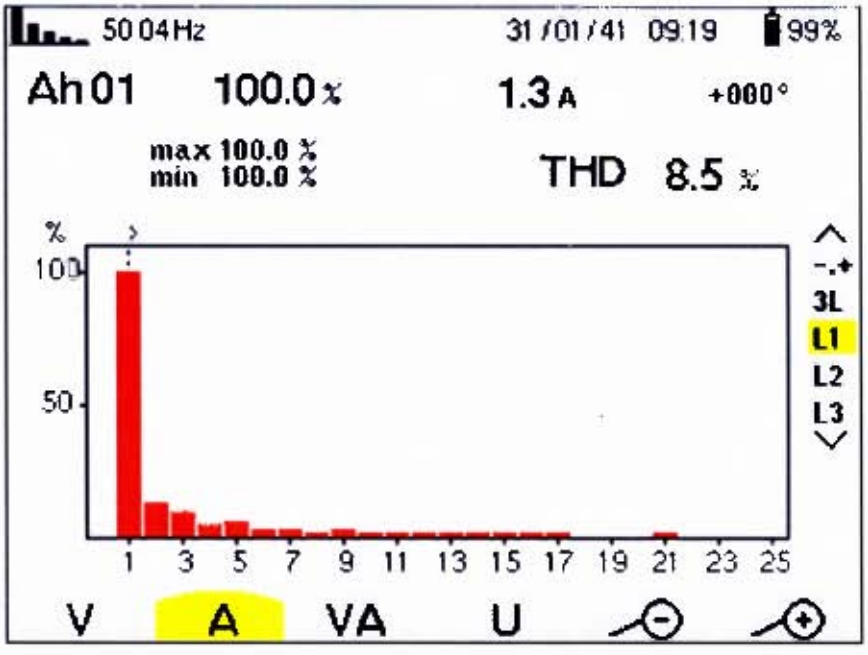

Figure 6-22 Practical - source current frequency spectrum under APF compensation

The THD calculated up to the 25th harmonic for the source current shown in figure 6-17 to 6-22 are tabulated in table 6.1. When comparing the two columns of the results, it can be seen from the table that the THD obtained from the experimental results is in close correlation with the simulation results.

Table 6.1 Computed THD for the source current

Type of Compensation	Simulation results THD [%]	Experimental results THD [%]
Without compensation	42.5	41.5
Ideal compensation	2.5	N/A
Shunt APF compensation	**3.5**	**8.5**

The source current THD is reduced from 42.5% to less than 5% in the simulation and from 41.5% to 8.5% in the practical. The THD of 3.5% is an acceptable distortion level by all known energy regulatory standards in the world such as the IEEE Standard 519 [50]. The compliance of the experimental results in relation to the

recommended harmonics limit imposed by IEEE Standard 519 [50] is not scrutinised further in this work but will however be discussed in the conclusions and recommendations presented in the next chapter.

7. Conclusions and Recommendations

7.1 Conclusions

This thesis has presented the development of an APF topology and its subsystems. This work began with the review of the previous research work and related literature in order to understand the background of the research area. Secondly, the theoretical analysis and design of the single phase shunt APF is outlined to give a theoretical background of the specific topology chosen. The theory governing the shunt APF topology is discussed with special emphasis given to the design of the sine-multiplication theorem for calculating compensation current and feed-forward control for the control of compensation current.

Computer aided simulations were carried out using both PSpice and Matlab/Simulink simulation packages. A 500VA laboratory prototype was then constructed and tested to prove the validity of the theory and the accuracy of the simulations. Lastly, in the previous chapter, the results obtained from the simulation and experimental prototype were compared and analysed with reference to the theory. The harmonic filtering performance of the APF topology is authenticated by a detailed THD analysis using the FFT.

Therefore from the results obtained above the following can be concluded:

- The practical did not perform in such a way as to cancel the harmonics to the satisfaction of the IEEE 519 standard. This is contrary to the simulation results which yielded an above-average THD of 3.5%. If the practical is compared to the simulation, the part that is missing in the practical is the PI controller in the DC-link. This shows that the greatest short-coming of the practical APF is

related to the absence of this component which was omitted due to time constraints. The consequential effect of the absence of the DC-link controller is that the DC-link voltage had to be controlled manually which yielded sub-standard performance. The inverter output voltage has to be kept at least $\sqrt{2}$ times higher than the source voltage for effective compensation. At the same time; to obtain a descent RMS value of compensation current, a high DC-link voltage is required.

- When tested at low power, the APF performed reasonably well with the overall THD of 8.5%. This demonstrates that this topology has the potential to perform well with further turning and revision of components.

- Feed-forward control is a relatively easy control strategy to implement on an APF. However, the major draw back is in implementing it successfully in practice. Furthermore, the requirement to estimate parameters in the control loop and the necessity to output a high voltage at the inverter output terminals- to obtain descent performance – are major drawbacks of this scheme.

- Overall, it can be said that this topology has the capability to compensate up to the 25^{th} harmonic or 1.2 kHz due to the constraints of the LPF at the output. However, more improvement is required if performance comparable to the Group Schneider ACCUSINE APF is desired i.e., achieving compensation up to the 50^{th} harmonic and achieve THD of less than 3%.

7.2 Recommendations

Therefore, from the conclusions presented above the following is recommended:

1. Implement entire APF in DSP.

- For practical implementation of the APF, the harmonic calculator implemented using the sine-multiplication theorem must be implemented in the DSP together with the controller. This will ensure that the APF is compact and easily assembled and installed. It will also remove the need for multiple analogue-to-digital conversions which results in loss of information.

2. Replacement of current controller.

- Although feed-forward control is a practical and simple approach for injecting current via an inverter, it has proven to be the major cause for sub-standard performance especially in the practical. Therefore, it may be fine for compensating low order harmonics i.e., up to 1 kHz. However, for commercial implementation where in some cases it can be necessary to compensate up to the 50th harmonic, or more; it is recommended to incorporate a more suitable control strategy such as hysteresis band current regulators or PI control.

3. Implementation of DC Bus voltage controller.

- Lastly, due to time constraint, the DC bus voltage controller was not implemented in this work. The capacitor voltage in the DC bus was supplied by a DC source instead of the DC bus capacitor. However, this approach will not be valid if the amplitude of the source voltage is

increased. Therefore, the DC bus voltage controller is needed to avoid additional use of DC source, as it was shown in the simulation.

- Future research will focus on the improvement of the current controller, possibly leading to an implementation using hysteresis band current regulators such as the one described in [52].

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Appendix A

(Technical Datasheets)

National Semiconductor

August 2000

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

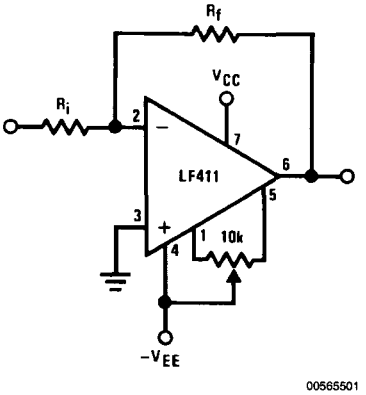
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage:	0.5 mV(max)
■ Input offset voltage drift:	10 µV/°C(max)
■ Low input bias current:	50 pA
■ Low input noise current:	0.01 pA/√Hz
■ Wide gain bandwidth:	3 MHz(min)
■ High slew rate:	10V/µs(min)
■ Low supply current:	1.8 mA
■ High input impedance:	$10^{12}\Omega$
■ Low total harmonic distortion:	≤0.02%
■ Low 1/f noise corner:	50 Hz
■ Fast settling time to 0.01%:	2 µs

Typical Connection



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Ordering Information

LF411XYZ

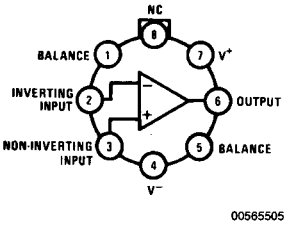
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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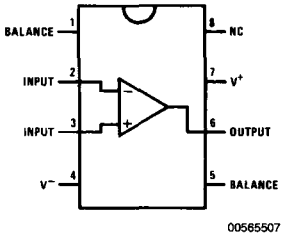
Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 11)
See NS Package Number H08A

Dual-In-Line Package



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Top View
Order Number LF411ACN, LF411CN
See NS Package Number N08E

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 2)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 3, 10)	670 mW	670 mW

	H Package	N Package
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined.	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 6)			7	10		7	20 (Note 6)	µV/°C
I_{OS}	Input Offset Current	V_S=±15V (Notes 5, 7)	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 5, 7)	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristic (Note 5)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25°C, f=1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

AC Electrical Characteristic (Note 5) (Continued)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02		%

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_j A$.

Note 4: These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF411A and for V_S=±15V for the LF411. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 6: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

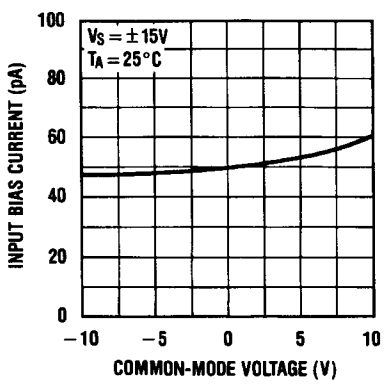
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

Note 9: RETS 411X for LF411MH and LF411MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

Input Bias Current



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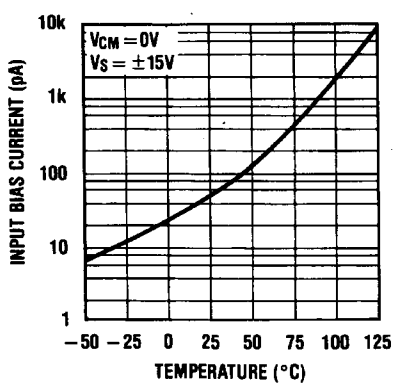
Input Bias Current



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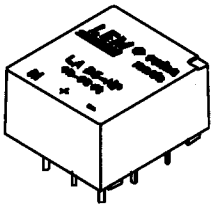
Current Transducer LA 25-NP

I_{PN} = 5-6-8-12-25 A

For the electronic measurement of currents : DC, AC, pulsed, mixed, with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		25		At
I_P	Primary current, measuring range		0 .. ± 36		At
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 15 V	@ ± 25 At_{max}	100	320	Ω
		@ ± 36 At_{max}	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		1-2-3-4-5 : 1000		
V_C	Supply voltage (± 5 %)		± 15		V
I_C	Current consumption		10 + I_S		mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn		2.5		kV
V_b	R.m.s. rated voltage [1],	safe separation	600		V
		basic isolation	1700		V

Accuracy - Dynamic performance data

X	Typical accuracy @ I_{PN}, T_A = 25°C		± 0.5		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current [2] @ I_P = 0, T_A = 25°C		± 0.05	± 0.15	mA
I_{OM}	Residual current [3] @ I_P = 0, after an overload of 3 x I_{PN}		± 0.05	± 0.15	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [4] @ 90 % of I_{PN}		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
f	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary resistance per turn @ T_A = 25°C		< 1.25	mΩ
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
R_{IS}	Isolation resistance @ 500 V, T_A = 25°C		> 1500	MΩ
m	Mass		22	g
	Standards [5]		EN 50178(97.10.01)	

Features

- Closed loop (compensated) multi-range current transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Notes : [1] Pollution class 2
[2] Measurement carried out after 15 mn functioning
[3] The result of the coercive field of the magnetic circuit
[4] With a di/dt of 100 A/µs
[5] A list of corresponding tests is available.

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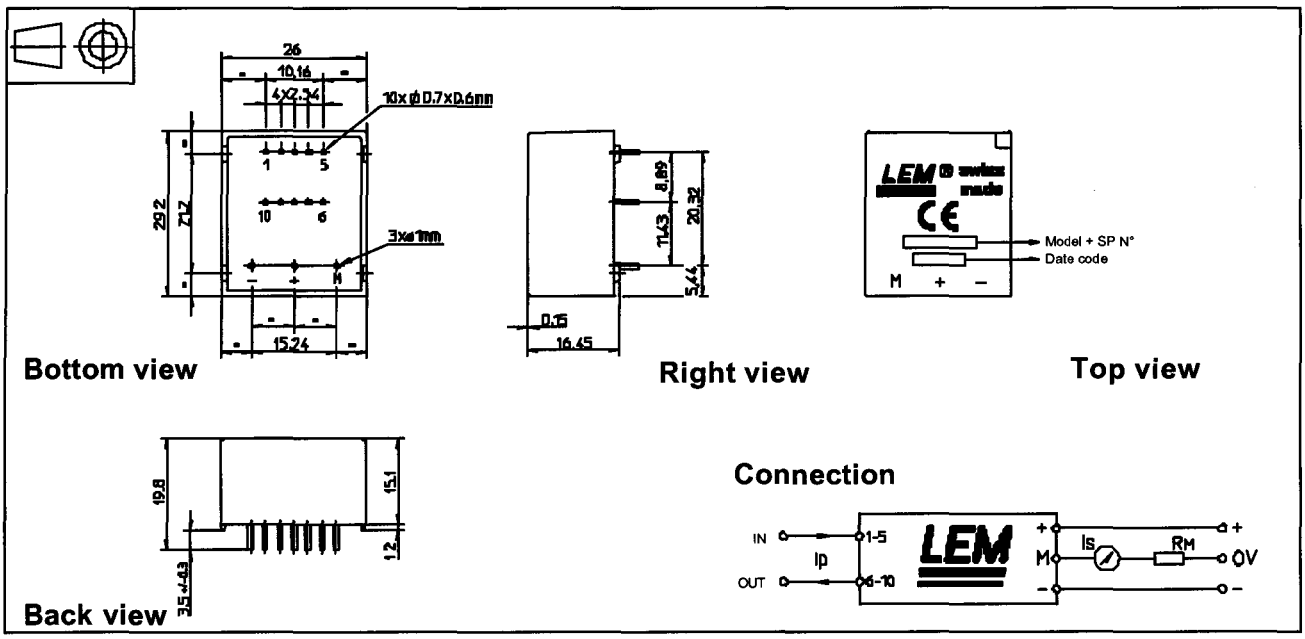
Dimensions LA 25-NP (in mm. 1 mm = 0.0394 inch)



Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended connections
1	25	36	25	1/1000	0.3	0.023	5 4 3 2 1 IN / OUT 6 7 8 9 10
2	12	18	24	2/1000	1.1	0.09	5 4 3 2 1 IN / OUT 6 7 8 9 10
3	8	12	24	3/1000	2.5	0.21	5 4 3 2 1 IN / OUT 6 7 8 9 10
4	6	9	24	4/1000	4.4	0.37	5 4 3 2 1 IN / OUT 6 7 8 9 10
5	5	7	25	5/1000	6.3	0.58	5 4 3 2 1 IN / OUT 6 7 8 9 10

Mechanical characteristics

- General tolerance ± 0.2 mm
- Fastening & connection of primary 10 pins 0.7 x 0.6 mm
- Fastening & connection of secondary 3 pins ∅ 1 mm
- Recommended PCB hole 1.2 mm

Remarks

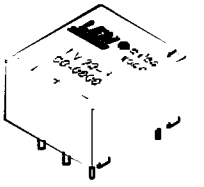
- I_S is positive when I_P flows from terminals 1, 2, 3, 4, 5 to terminals 10, 9, 8, 7, 6
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Voltage Transducer LV 20-P

I_{PN} = 10 mA

V_{PN} = 10 .. 500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		10		mA
I_P	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA $_{max}$	30	190	Ω
		@ ± 14 mA $_{max}$	30	100	Ω
	with ± 15 V	@ ± 10 mA $_{max}$	100	350	Ω
		@ ± 14 mA $_{max}$	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@±15V)+I_S		mA
V_d	R.m.s. voltage for AC isolation test[1], 50 Hz, 1 mn		2.5		kV

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 1.1		%
		@ ± 15 V (± 5 %)	± 1.0		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.20	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.10	± 0.30	mA
		+ 25°C .. + 70°C	± 0.14	± 0.40	mA
t_r	Response time[2] @ 90 % of $V_{P\,max}$		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C		250	Ω
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
m	Mass		22	g
	Standards [3]		EN 50178	

Notes : [1] Between primary and secondary

[2] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit)

[3] A list of corresponding tests is available

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0
- Optimized.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

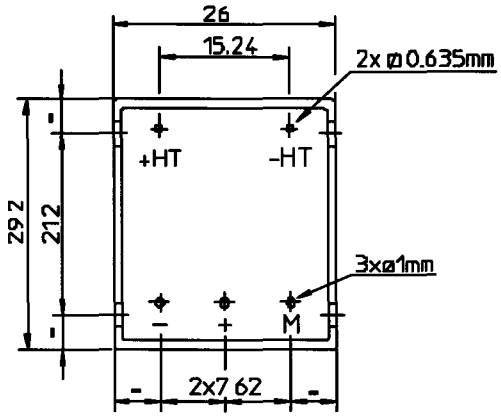
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

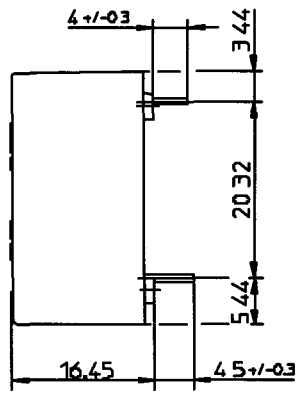
010802/0

Dimensions LV 20-P (in mm. 1 mm = 0.0394 inch)

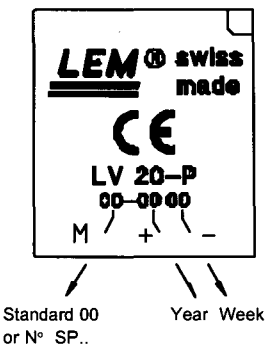
Bottom view



Right view

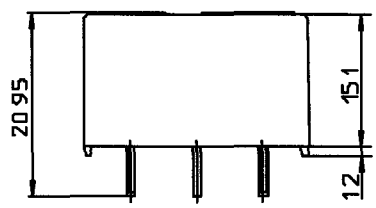


Top view



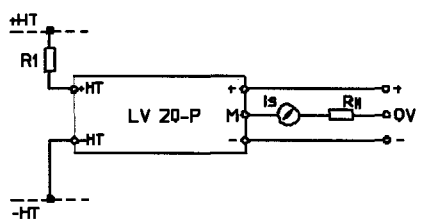
Secondary terminals

Terminal + : supply voltage + 12 .. 15 V
Terminal M : measure
Terminal - : supply voltage - 12 .. 15 V



Back view

Connection



Mechanical characteristics

• General tolerance	± 0.2 mm
• Fastening & connection of primary	2 pins 0.635 x 0.635 mm
• Fastening & connection of secondary	3 pins ∅ 1 mm
• Recommended PCB hole	1.2 mm

Remarks

- I_S is positive when V_P is applied on terminal +HT.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Instructions for use of the voltage transducer model LV 20-P

Primary resistor R_1 : the transducer's optimum accuracy is obtained at the nominal primary current. As much as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Example: Voltage to be measured V_{PN} = 250 V
a) R_1 = 25 kΩ / 2.5 W, I_P = 10 mA Accuracy = ± 1 % of V_{PN} (@ T_A = +25°C)
b) R_1 = 50 kΩ / 1.25 W, I_P = 5 mA Accuracy = ± 2 % of V_{PN} (@ T_A = +25°C)

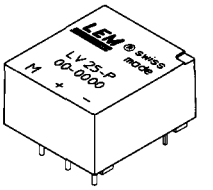
Operating range (recommended) : taking into account the resistance of the primary windings (which must remain low compared to R_1 in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

Voltage Transducer LV 25-P

I_{PN} = 10 mA

V_{PN} = 10 .. 500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		10		mA
I_P	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA $_{max}$	30	190	Ω
		@ ± 14 mA $_{max}$	30	100	Ω
	with ± 15 V	@ ± 10 mA $_{max}$	100	350	Ω
		@ ± 14 mA $_{max}$	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@±15 V) + I_S		mA
V_d	R.m.s. voltage for AC isolation test [1], 50 Hz, 1 mn		2.5		kV

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [2] @ 90 % of $V_{P\,max}$		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C		250	Ω
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
m	Mass		22	g
	Standards [3]		EN 50178	

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

Notes : [1] Between primary and secondary

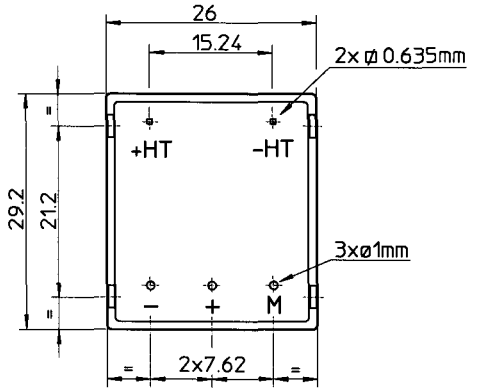
[2] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit)

[3] A list of corresponding tests is available

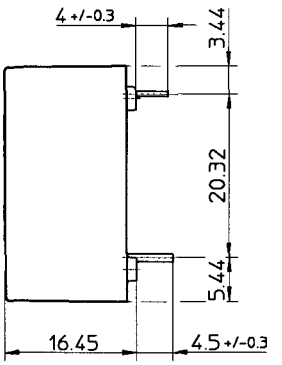
981125/14

Dimensions LV 25-P (in mm. 1 mm = 0.0394 inch)

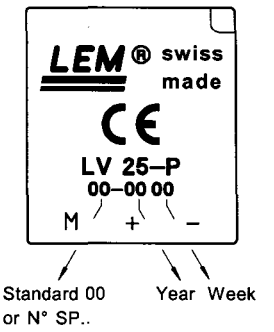
Bottom view

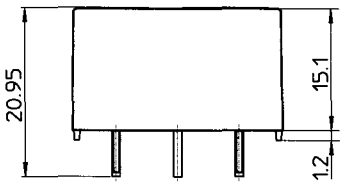


Right view



Top view

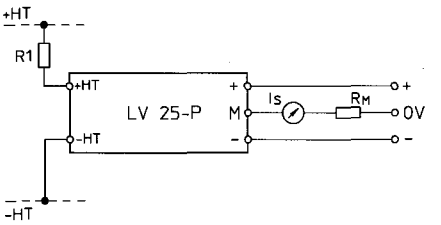




Secondary terminals

Terminal + : supply voltage + 12 .. 15 V
Terminal M : measure
Terminal - : supply voltage - 12 .. 15 V

Connection



Back view

Mechanical characteristics

• General tolerance	± 0.2 mm
• Fastening & connection of primary	2 pins 0.635 x 0.635 mm
• Fastening & connection of secondary	3 pins ∅ 1 mm
• Recommended PCB hole	1.2 mm

Remarks

- I_S is positive when V_P is applied on terminal +HT.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

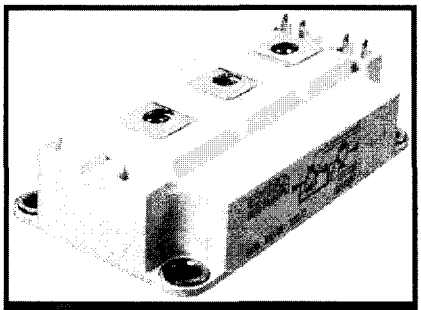
Instructions for use of the voltage transducer model LV 25-P

Primary resistor R_1 : the transducer's optimum accuracy is obtained at the nominal primary current. As far as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Example: Voltage to be measured V_{PN} = 250 V
a) R_1 = 25 kΩ / 2.5 W, I_P = 10 mA Accuracy = ± 0.8 % of V_{PN} (@ T_A = +25°C)
b) R_1 = 50 kΩ / 1.25 W, I_P = 5 mA Accuracy = ± 1.6 % of V_{PN} (@ T_A = +25°C)

Operating range (recommended) : taking into account the resistance of the primary windings (which must remain low compared to R_1, in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

SKM 200GB123D



SEMITRANS® 3

Trench IGBT Modules

SKM 200GB123D
SKM 200GAL123D
SKM 200GAR123D

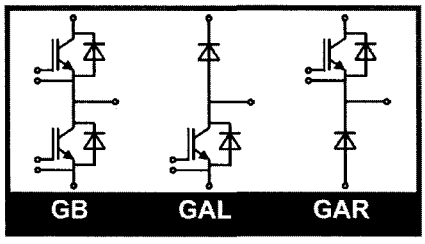
Z_{th} Symbol	Conditions	Values	Units
$Z_{th(j-c)I}$			
R_i	i = 1	59	mk/W
R_i	i = 2	23	mk/W
R_i	i = 3	6,8	mk/W
R_i	i = 4	1,2	mk/W
tau_i	i = 1	0,03	s
tau_i	i = 2	0,0087	s
tau_i	i = 3	0,002	s
tau_i	i = 4	0,0002	s
$Z_{th(j-c)D}$			
R_i	i = 1	170	mk/W
R_i	i = 2	66	mk/W
R_i	i = 3	12	mk/W
R_i	i = 4	2	mk/W
tau_i	i = 1	0,0348	s
tau_i	i = 2	0,0072	s
tau_i	i = 3	0,077	s
tau_i	i = 4	0,0002	s

Features

- MOS input (voltage controlled)
- N channel, homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 x I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (13 mm) and creepage distances (20 mm)

Typical Applications

- AC inverter drives
- UPS



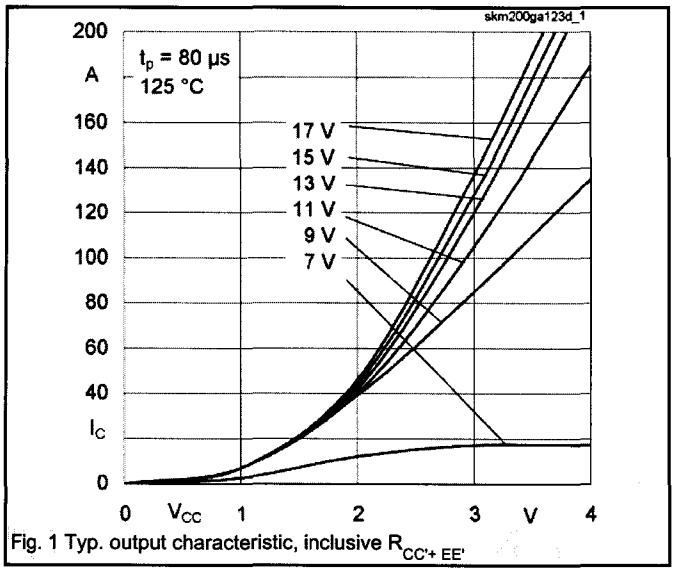


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

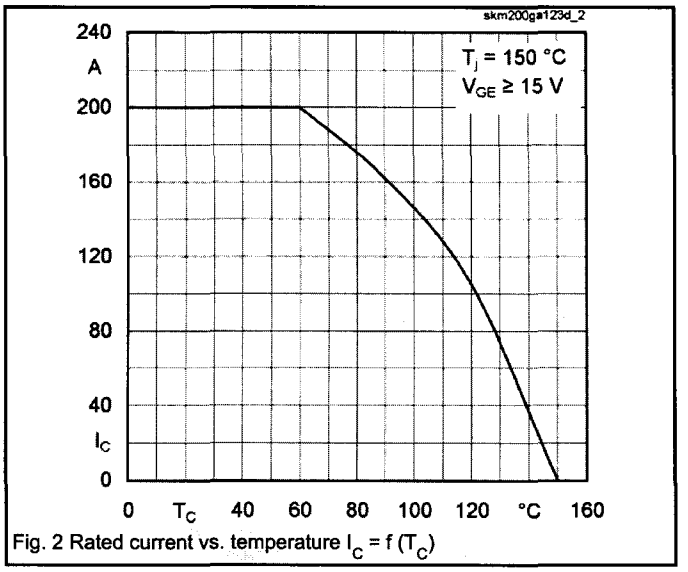


Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

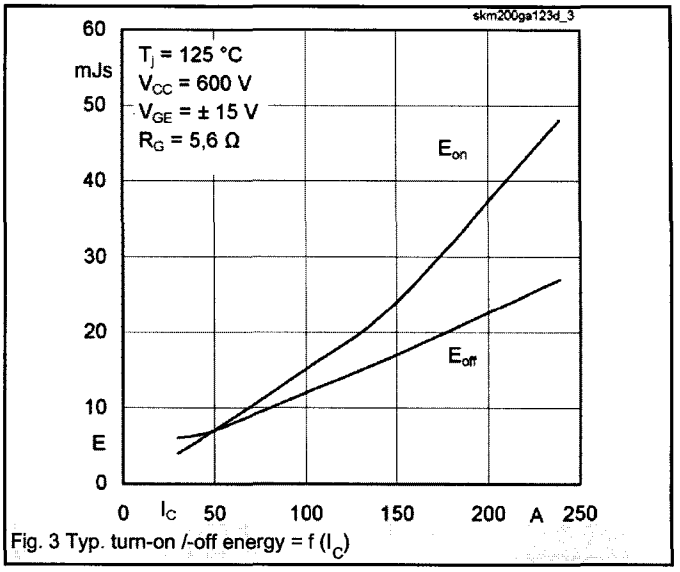


Fig. 3 Typ. turn-on /-off energy = f (I_C)

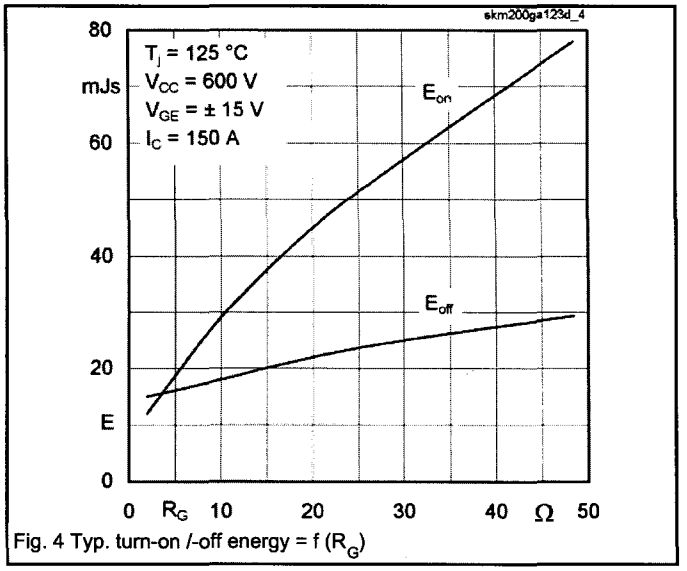


Fig. 4 Typ. turn-on /-off energy = f (R_G)

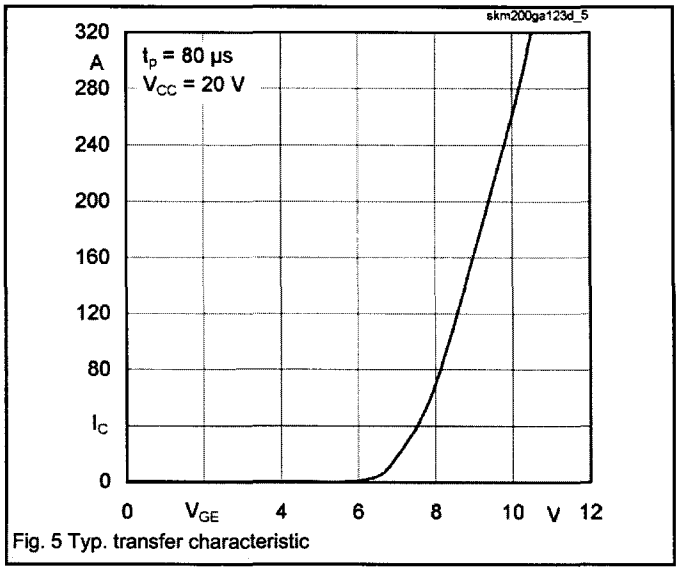


Fig. 5 Typ. transfer characteristic

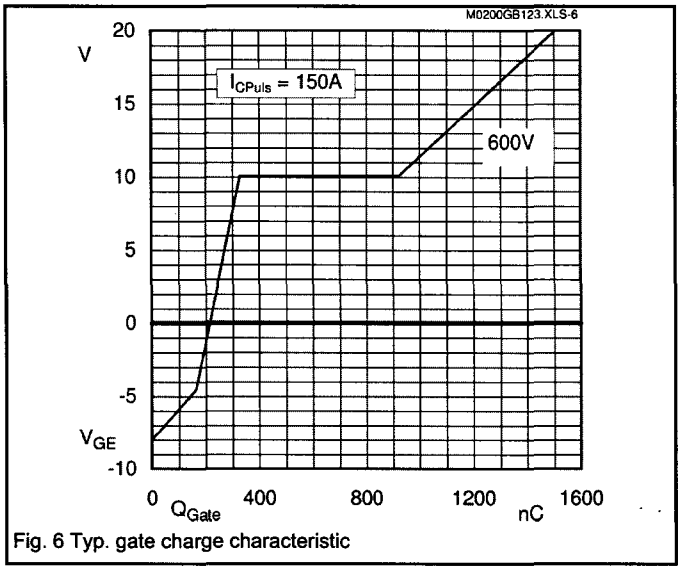
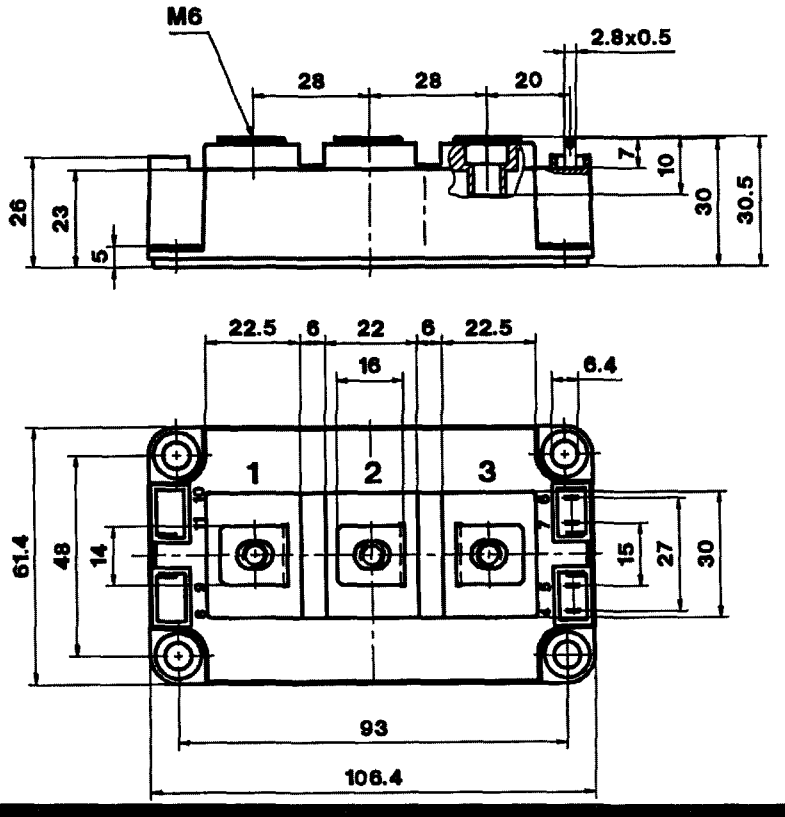


Fig. 6 Typ. gate charge characteristic

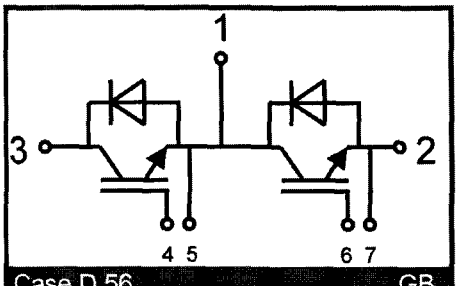
UL Recognized
File no. E 63 532

Dimensions in mm

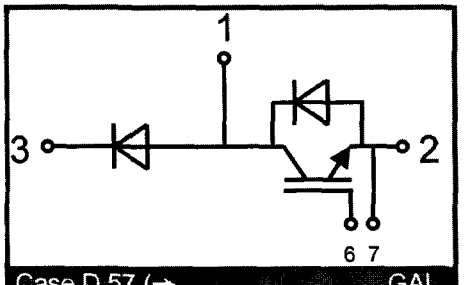
CASED56



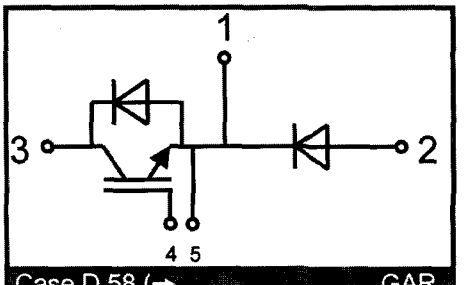
Case D 56



Case D 56 GB



Case D 57 (→ 56) GAL



Case D 58 (→ 56) GAR

T-03-19

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MR860 MR861 MR862 MR864 MR866

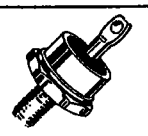
Designers Data Sheet

STUD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference, sonar power supplies and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 150 nanoseconds providing high efficiency at frequencies to 250 kHz.

FAST RECOVERY POWER RECTIFIERS

50-600 VOLTS
40 AMPERES



Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

MAXIMUM RATINGS

Rating	Symbol	MR860	MR861	MR862	MR864	MR866	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	75	150	250	450	650	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	Volts
Average Rectified Forward Current (Single phase, resistive load, T_C = 100°C)	I_O	40					Amps
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	350					Amps
Operating Junction Temperature Range	T_J	-65 to +160					°C
Storage Temperature Range	T_{stg}	-65 to +175					°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.85	°C/W

ELECTRICAL CHARACTERISTICS

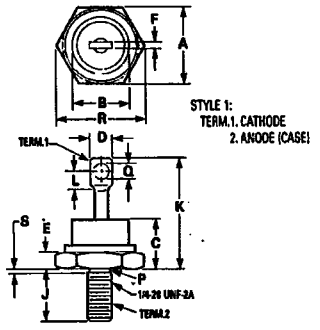
Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (i_F = 125 Amp, T_J = 150°C)	v_F	–	1.3	1.6	Volts
Forward Voltage (I_F = 40 Amp, T_C = 25°C)	V_F	–	1.0	1.4	Volts
Reverse Current (rated dc voltage) T_C = 25°C T_C = 100°C	I_R	– –	25 1.0	50 2.0	μA mA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 16) (I_{FM} = 36 Amp, di/dt = 25 A/μs, Figure 17)	t_{rr}	– –	150 200	200 400	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 16)	$I_{RM(REC)}$	–	2.0	3.0	Amp

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed
FINISH: All external surfaces corrosion resistant and readily solderable
POLARITY: Cathode to Case
WEIGHT: 17 Grams (Approximately)
STUD TORQUE: 25 in. lbs.



NOTES:
1. DIM "P" IS DIA.
2. CHAMFER OR UNDERCUT ON ONE OR BOTH ENDS OF HEXAGONAL BASE IS OPTIONAL.
3. ANGULAR ORIENTATION AND CONTOUR OF TERMINAL ONE IS OPTIONAL.
4. THREADS ARE PLATED.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.94	17.45	0.599	0.687
B	—	16.94	—	0.667
C	—	11.43	—	0.450
D	—	9.53	—	0.375
E	2.92	5.08	0.115	0.200
F	—	2.03	—	0.080
J	10.72	11.51	0.422	0.453
K	—	25.40	—	1.000
L	3.86	—	0.156	—
P	5.59	6.32	0.220	0.249
Q	3.56	4.45	0.140	0.175
R	—	20.16	—	0.794
S	—	2.26	—	0.089

CASE 257-01
DO-203AB
METAL

MR860, MR861, MR862, MR864, MR866

FIGURE 1 – FORWARD VOLTAGE

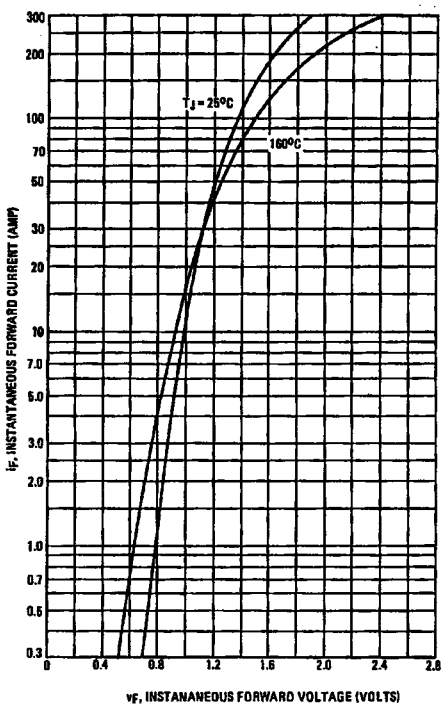
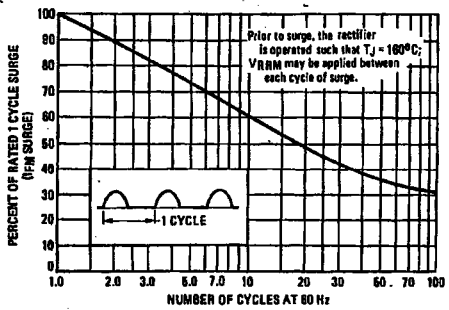
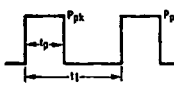


FIGURE 2 – MAXIMUM SURGE CAPABILITY



NOTE 1



DUTY CYCLE: D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see Note 3). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

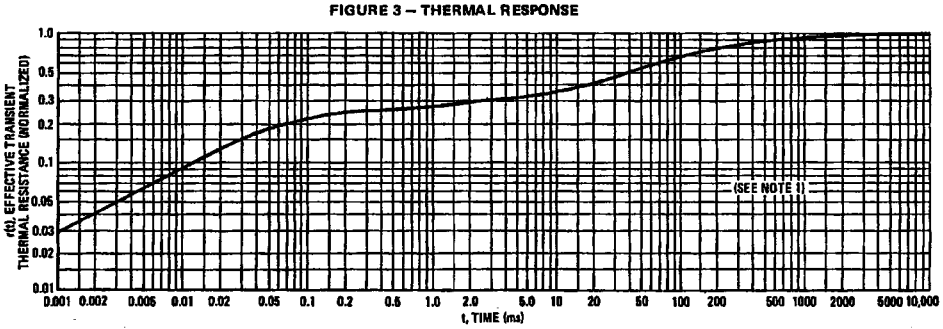
$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 3, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

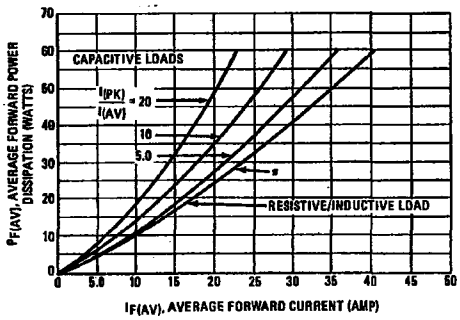
FIGURE 3 – THERMAL RESPONSE



MR860, MR861, MR862, MR864, MR866

SINE WAVE INPUT

FIGURE 4 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 5 – FORWARD POWER DISSIPATION

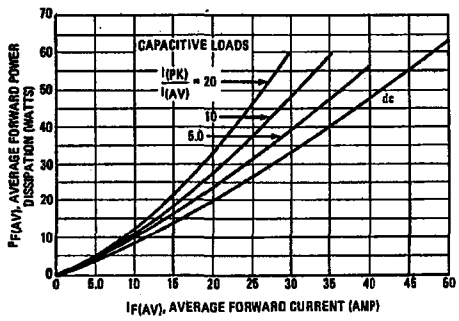


FIGURE 6 – CURRENT DERATING

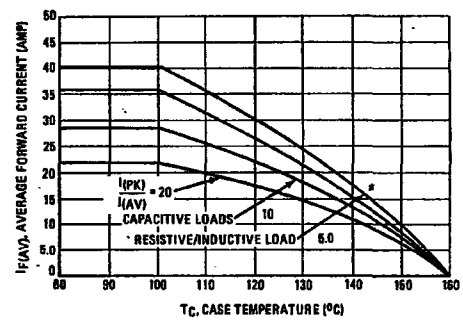


FIGURE 7 – CURRENT DERATING

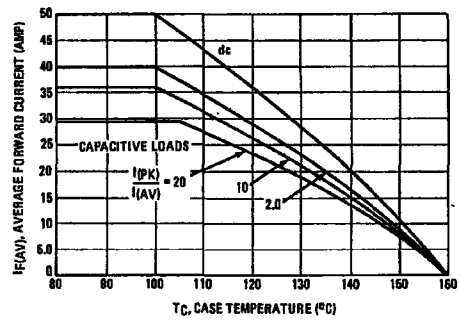


FIGURE 8 – TYPICAL REVERSE CURRENT

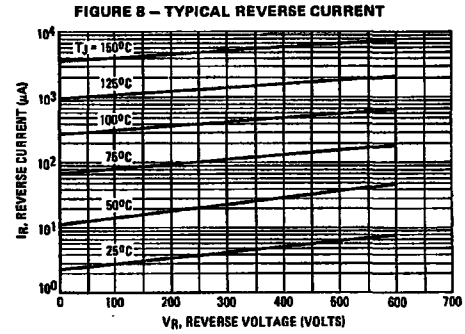
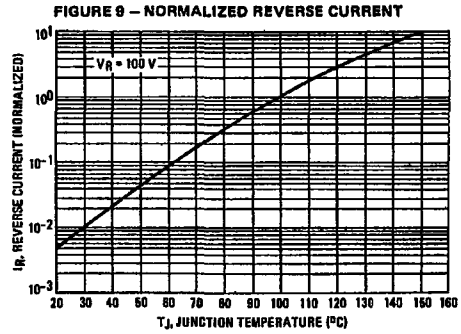


FIGURE 9 – NORMALIZED REVERSE CURRENT



Appendix B

(C++ Code and Datasheet for TMS320LF2407 DSP)

```
/*****************************************************************************
*/
/* written by: Michael Mkhize                                                */

/* Date: Aug 2009                                                            */
                                                                             */
/* Title:  Feedforward/predictive control of single phase APF                */
/*                                                                           */
                    */
/* Comments:                                                                 */          */
/*         This code implements feed-forward control                         */
/*         for a single-phase inverter.                                      */          */
/*         the function of the controller is to produce          */
/*         the switching pulses to control a full-bridge               */
/*         single phase inverter in order to implement               */
/*         shunt Active filter.                                  */
/*****************************************************************************
*/

/*Initialising pointers*/

volatile unsigned int *COMCONA = (volatile unsigned int *) 0x7411;
volatile unsigned int *GPTCONA = (volatile unsigned int *) 0x7400;
volatile unsigned int *ACTRA = (volatile unsigned int *) 0x7413;
volatile unsigned int *DBTCONA = (volatile unsigned int *) 0x7415;

volatile unsigned int *CMPR1 = (volatile unsigned int *) 0x7417;
volatile unsigned int *CMPR2 = (volatile unsigned int *) 0x7418;
volatile unsigned int *CMPR3 = (volatile unsigned int *) 0x7419;

volatile unsigned int *T1CON = (volatile unsigned int *) 0x7404;
volatile unsigned int *T2CON = (volatile unsigned int *) 0x7408;
volatile unsigned int *T1PR = (volatile unsigned int *) 0x7403;
volatile unsigned int *T1CNT = (volatile unsigned int *) 0x7401;
volatile unsigned int *T2PR = (volatile unsigned int *) 0x7407;
volatile unsigned int *T2CNT = (volatile unsigned int *) 0x7405;

volatile unsigned int *MCRA = (volatile unsigned int *) 0x7090;
volatile unsigned int *MCRB = (volatile unsigned int *) 0x7092;
volatile unsigned int *MCRC = (volatile unsigned int *) 0x7094;
volatile unsigned int *PADATDIR = (volatile unsigned int *) 0x7098;
volatile unsigned int *PBDATDIR = (volatile unsigned int *) 0x709A;
volatile unsigned int *PCDATDIR = (volatile unsigned int *) 0x709C;
volatile unsigned int *PFDATDIR = (volatile unsigned int *) 0x7096;

volatile unsigned int *EVAIMRA = (volatile unsigned int *) 0x742C;
```

```
volatile unsigned int *IMR = (volatile unsigned int *) 0x0004;
volatile unsigned int *IFR = (volatile unsigned int *) 0x0006;
volatile unsigned int *EVAIFRA = (volatile unsigned int *) 0x742F;

volatile unsigned int *SPICCR = (volatile unsigned int *) 0x7040;
volatile unsigned int *SPICTL = (volatile unsigned int *) 0x7041;
volatile unsigned int *SPISTS = (volatile unsigned int *) 0x7042;
volatile unsigned int *SPIBRR = (volatile unsigned int *) 0x7044;
volatile unsigned int *SPIRXEMU = (volatile unsigned int *) 0x7046;
volatile unsigned int *SPIRXBUF = (volatile unsigned int *) 0x7047;
volatile unsigned int *SPITXBUF = (volatile unsigned int *) 0x7048;
volatile unsigned int *SPIDAT = (volatile unsigned int *) 0x7049;
volatile unsigned int *SPIPRI = (volatile unsigned int *) 0x704F;

volatile unsigned int *SCSR1 = (volatile unsigned int *) 0x7018;

volatile unsigned int *ADCTRL1 = (volatile unsigned int *) 0x70A0;
volatile unsigned int *ADCTRL2 = (volatile unsigned int *) 0x70A1;
volatile unsigned int *MAXCONV = (volatile unsigned int *) 0x70A2;
volatile unsigned int *CHSELSEQ1 = (volatile unsigned int *) 0x70A3;
volatile unsigned int *CHSELSEQ2 = (volatile unsigned int *) 0x70A4;
volatile unsigned int *CHSELSEQ3 = (volatile unsigned int *) 0x70A5;
volatile unsigned int *CHSELSEQ4 = (volatile unsigned int *) 0x70A6;
volatile unsigned int *AUTO_SEQ_SR = (volatile unsigned int *) 0x70A7;
volatile unsigned int *RESULT0 = (volatile unsigned int *) 0x70A8;
volatile unsigned int *RESULT1 = (volatile unsigned int *) 0x70A9;
volatile unsigned int *RESULT2 = (volatile unsigned int *) 0x70AA;
volatile unsigned int *RESULT3 = (volatile unsigned int *) 0x70AB;
volatile unsigned int *RESULT4 = (volatile unsigned int *) 0x70AC;
volatile unsigned int *RESULT5 = (volatile unsigned int *) 0x70AD;
volatile unsigned int *RESULT6 = (volatile unsigned int *) 0x70AE;
volatile unsigned int *RESULT7 = (volatile unsigned int *) 0x70AF;
volatile unsigned int *RESULT8 = (volatile unsigned int *) 0x70B0;
volatile unsigned int *RESULT9 = (volatile unsigned int *) 0x70B1;
volatile unsigned int *RESULT10 = (volatile unsigned int *) 0x70B2;
volatile unsigned int *RESULT11 = (volatile unsigned int *) 0x70B3;
volatile unsigned int *RESULT12 = (volatile unsigned int *) 0x70B4;
volatile unsigned int *RESULT13 = (volatile unsigned int *) 0x70B5;
volatile unsigned int *RESULT14 = (volatile unsigned int *) 0x70B6;
volatile unsigned int *RESULT15 = (volatile unsigned int *) 0x70B7;
volatile unsigned int *CALIBRATION = (volatile unsigned int *) 0x70B8;


/*initializing variables*/
```

```
/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
        Initialization of integers for DAC
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

int i,j,angle,DAC1,DAC2,DAC3,DAC4,DAC5,DAC6,DAC7,DAC8;

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
        Initialization of integers for input values
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

int Vac,Iref,VacShift,output_shift,pot1,Irefshift;
int VsArr[100],index,VsReal,VsImag,VsPhase,pot2,power_angle;
long int InputSample,VacReal,VacScaled,IrefReal,value1,value;

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
-----------------------------------------------
        Initialization of float values for implementing derivative function and control
equation
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

float stDeriv,dIref_dt,dIref_dt_scaled,Iref_r,dIref_dtReal;
float PrevIref;
float PrevPrevIref=0;
float SampleRate=10000;        /*Sampling at 10kHz */
float L=52/32768;              /* Representing a 1.6mH inductor   */
float r=65540/32768;           /* representing equivalent inductor resistance */

/* Calling up external functions */

extern int sine();
extern int atan();

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
```

```
        starting point for the interrupters
-------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------
------*/

interrupt void Test1(void)
{
}

/*-------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------
--------
        main interrupter "GPT1_underflow"
-------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------
------*/

interrupt void GPT1_underflow(void)
{
        *PFDATDIR &= 0xFFFB;

        *CHSELSEQ1 = 0x0B20;
/*      *CHSELSEQ2 = 0x1010; */
        *ADCTRL2 |= 0x2000;
         while(ADCTRL2 && 0x0200 == 0x0000) {};
        *ADCTRL2 |= 0x0200;

/*-------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------
--------
        reading Analogue values through 10-bit ADC
-------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------
------*/

   Vac = *RESULT0;
        Vac = Vac>>6;
        Vac &= 0x03FF;

        Iref = *RESULT1;
        Iref = Iref>>6;
        Iref &= 0x03FF;

        pot1 = *RESULT1;
        pot1 = pot1>>6;
        pot1 &= 0x03FF;
```

```
/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
     Udjusting phase angle and amplitude with a pot to tie inverter to grid
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

    output_shift=pot1;              /*Adjusting inverter output amplitude*/

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
         scaling down to zero reference  to remove 1.6V offset & working out real values
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

   VacShift=Vac-512;
         VacReal=((long int)VacShift*3620)/1024;    /* Analogue input value of 1.5VAC
peak-to-peak is conveted to Real digital value of 640V peak-to-peak */
   VacScaled=((long int)VacReal*1024)/595;

         Irefshift=Iref-512;
         IrefReal=(Irefshift*266)/51200;          /* Converting load current to real value */

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
--------
         Power angle control subroutine: Adjusting power angle
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/
/*       VsReal=Vs;
         VsImag=VsArr[index];
         VsPhase=arctan(VsReal/2,VsImag/2);
    anglea=VsPhase+power_angle;
    if(anglea > 200) anglea = 200;
         if(anglea < -200) anglea = -200;   */
    /*VacReal=sine(anglea)/2;

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
-----------------------------------------------------------------------
```

```
        Working out derivative of input harmonic current in order to calculate
approximate inductor voltage drop at the output
------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
------*/

   stDeriv=(Irefshift-PrevPrevIref)/(2*(1/SampleRate));    /* Output of 1stDeriv is equal
to frequncy*2*pi*(original amplitude)  */
        PrevPrevIref=PrevIref;
   PrevIref=Irefshift;
   dIref_dt=stDeriv;
   dIref_dtReal=((float)dIref_dt*4)/20480;          /* Scaling down derivative output to a
suitable amplitude */

/*--------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
---------
        Implementing feed-forward control
------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
------*/

   Iref_r=IrefReal*r;                    /* Calculating approx voltage drop on inductor
equivalent resistance */
   value1=dIref_dtReal+Iref_r;              /*Summing up voltage drop across the
inductor */
        value=value1+VacScaled;                 /* Value is the total voltage drop
required across the loop */

/*--------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
---------
        generating switch signal
------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
------*/

        *CMPR1=value*pot1+1024;
        *CMPR2=-value*pot1+1024;

/*--------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
---------
        Sending data to 8-bit DAC for debugging purposes
```

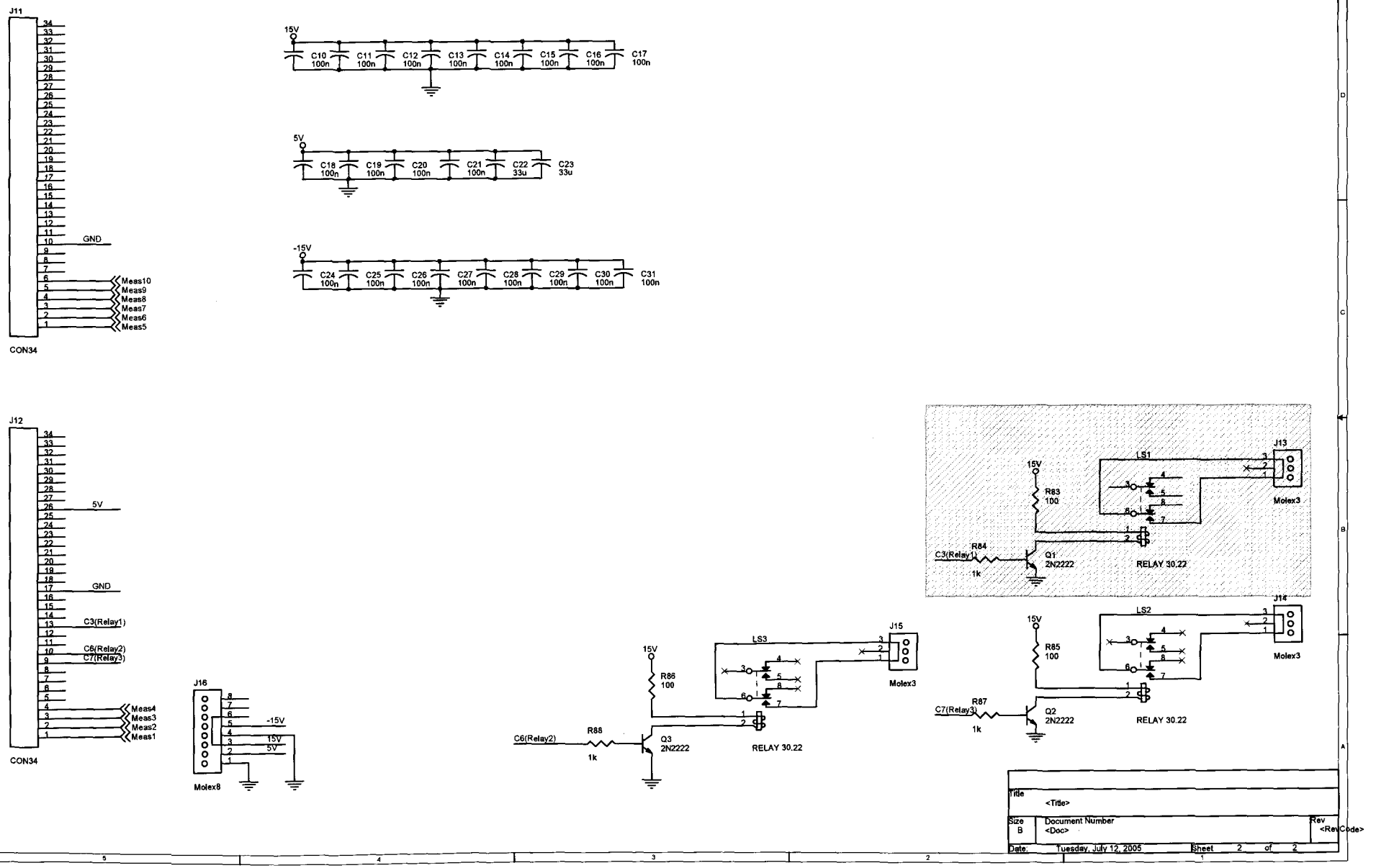
```
------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------
------*/

/*  VsArr[index]=Vs;        /* Updating phase shifting array */

        DAC1 = (dIref_dt/1000+128);
        DAC1 = DAC1<<4;
        DAC1 &= 0x0FFF;
        DAC1 |= 0x0000;
        *SPITXBUF = DAC1;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC2 = VacReal/8+128;
        DAC2 = DAC2<<4;
        DAC2 &=0x0FFF;
        DAC2|=0x2000;
        *SPITXBUF = DAC2;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC3 = value1+128;
        DAC3 = DAC3<<4;
        DAC3 &= 0x0FFF;
        DAC3 |= 0x4000;
        *SPITXBUF = DAC3;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC4 = Irefshift+128;
        DAC4 = DAC4<<4;
        DAC4 &= 0x0FFF;
        DAC4 |= 0x6000;
        *SPITXBUF = DAC4;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC5 = dIref_dtReal+128;
        DAC5 = DAC5<<4;
        DAC5 &= 0x0FFF;
        DAC5 |= 0x8000;
```

```
        *SPITXBUF = DAC5;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC6 = (value/8)+128;
        DAC6 = DAC6<<4;
        DAC6 &= 0x0FFF;
        DAC6 |= 0xA000;
        *SPITXBUF = DAC6;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

/*      DAC7 = (comp1in)/4;
        DAC7 = DAC7<<4;
        DAC7 &= 0x0FFF;
        DAC7 |= 0xC000;
        *SPITXBUF = DAC7;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;

        DAC8 = (comp2in)/4;
        DAC8 = DAC8<<4;
        DAC8 &= 0x0FFF;
        DAC8 |= 0xE000;
        *SPITXBUF = DAC8;
        for (i=0; i<4; i++) {}
        *PCDATDIR &= 0x0FFDF;
        *PCDATDIR |= 0x0020;      */

        *EVAIFRA |= 0x0200;

   *PFDATDIR |= 0x0004;

}

interrupt void Test3(void)
{
}

interrupt void Test4(void)
{
}
```

```
interrupt void Test5(void)
{
}

interrupt void XINT2(void)  /*   ADCInterrupt, external interrupt pin in high-priority
mode */
{
}


/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
---------
        starting of main program
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

void main(void)
{

        *SCSR1 = 0x00AC;

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
---------
        Interrupt set-up
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

        *IMR = 0x0022;
        *IFR = 0xFFFF;
        *EVAIMRA = 0x0200;
        asm("   clrc INTM");

/*-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
---------
        SPI port set-up for DAC coms
-------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------
------*/

        *SPICCR &= 0x0FF7F;
        *MCRB |= 0x001C;
```

```
        *SPICCR |= 0x000B;
        *SPICTL = 0x0006;
        *SPIBRR |= 0x0003;
        *SPICCR |= 0x0080;

        *PCDATDIR |= 0x2020;


/*-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
---------
        Registers for IOPF2 code-timer
-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
------*/

        *MCRC &= 0xFDFF;
        *PFDATDIR |= 0x0404;

/*-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
---------
        Registers for ADC
-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
------*/

        *ADCTRL1 = 0x0840;
        *ADCTRL2 = 0x0000;
        *MAXCONV = 0x0002;
/*      *CHSELSEQ1 = 0x0001; */

/*-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
---------
        Registers for PWM generation
-----------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------
------*/

        *MCRA |= 0x0FC0;
        *ACTRA = 0x0999;
/*      *DBTCON = 0x0AE0;  */
        *DBTCONA = 0;

        *CMPR1 = 0;
```

```
        *CMPR2 = 0;

        *COMCONA = 0x0307;
        *COMCONA = 0x8307;

        *T1PR = 2048;                          /* Period = 2048*25nsec*2 = 100usec
: freq approx 10kHz */
        *T1CNT = 0x0;
        *T1CON = 0xA802;                        /* up/down continuous mode */

        *T2PR = 6138;                          /* Period = 6138*25nsec*128 approx =
20msec or 50Hz */
        *T2CNT = 0x0;
        *T2CON = 0x9702;                        /* set in cont up, and set clock
prescaler to 128 */

        *T1CON = 0xA842;                        /* start the clock */
        *T2CON = 0x9742;                        /* start the clock */


        /*Initialising variables */

        index = 1;
        power_angle=0;
        j = 1;
        /*PrevPrevIref=0;   */

        for (;;)
        {
        }

}
```


J11
GND
Meas10
Meas9
Meas8
Meas7
Meas6
Meas5
CON34
15V
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
5V
C18 100n
C19 100n
C20 100n
C21 100n
C22 33u
C23 33u
-15V
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
C29 100n
C30 100n
C31 100n
J12
5V
GND
C3(Relay1)
C6(Relay2)
C7(Relay3)
Meas4
Meas3
Meas2
Meas1
CON34
J16
-15V
15V
5V
Molex8
LS1
J13
R83 100
C3(Relay1)
R84 1k
Q1 2N2222
RELAY 30.22
Molex3
LS3
J15
R86 100
C6(Relay2)
R88 1k
Q3 2N2222
RELAY 30.22
Molex3
LS2
J14
R85 100
C7(Relay3)
R87 1k
Q2 2N2222
RELAY 30.22
Molex3
Title
<Title>
Size B
Document Number
<Doc>
Rev
<RevCode>
Date: Tuesday, July 12, 2005
Sheet 2 of 2

TYPICAL CHARACTERISTICS

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

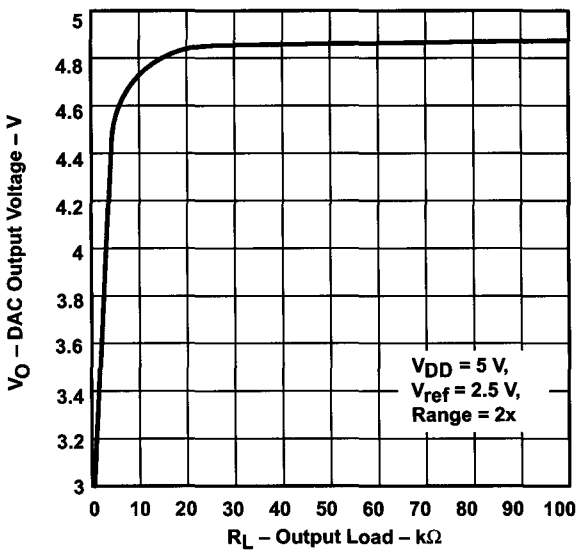


Figure 9

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

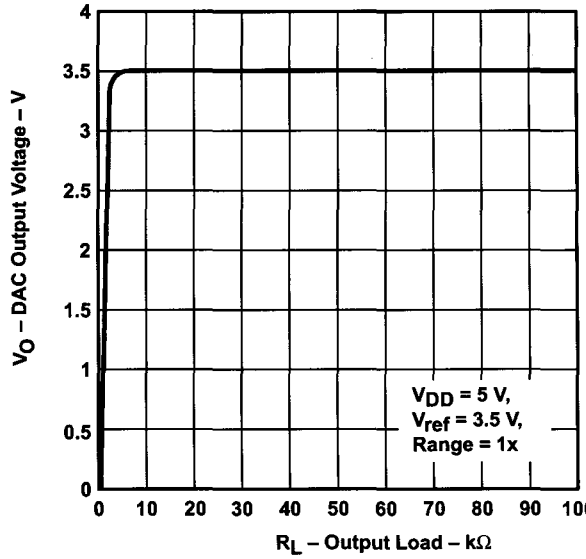


Figure 10

OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE

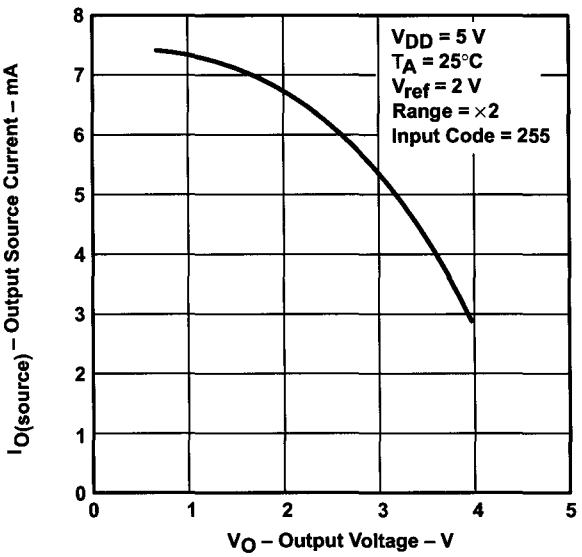


Figure 11

SUPPLY CURRENT
vs
TEMPERATURE

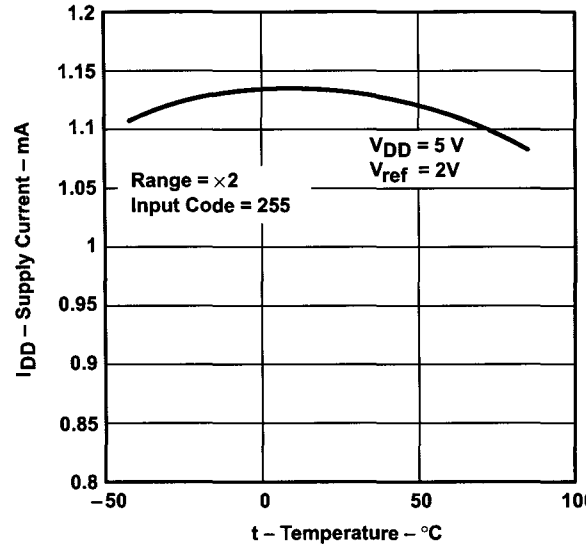


Figure 12

TYPICAL CHARACTERISTICS

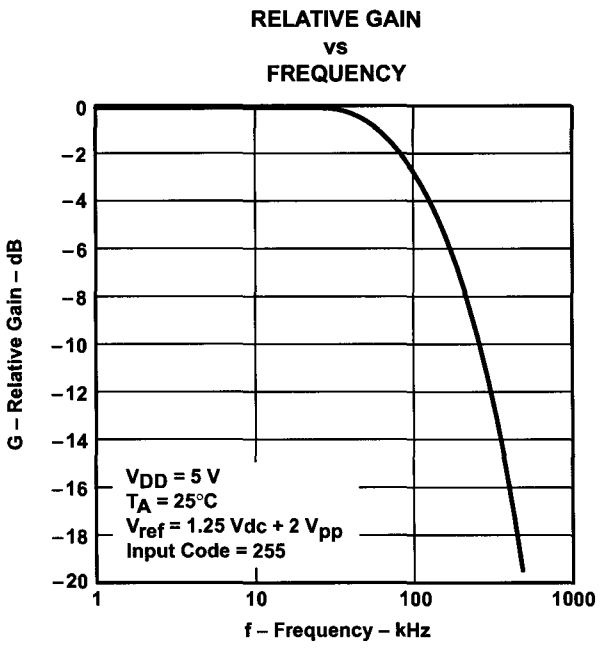


Figure 13

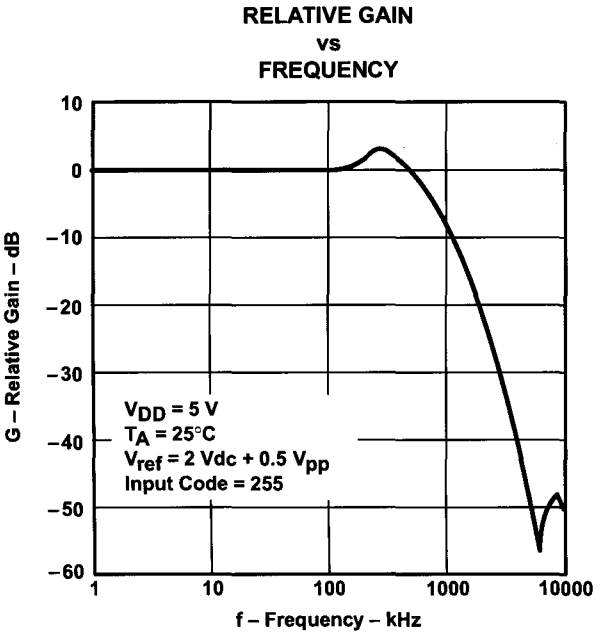
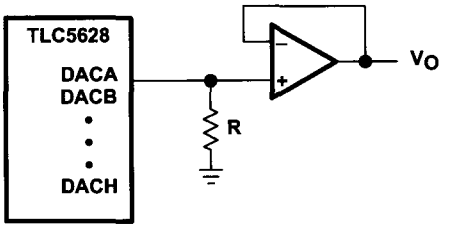


Figure 14

APPLICATION INFORMATION



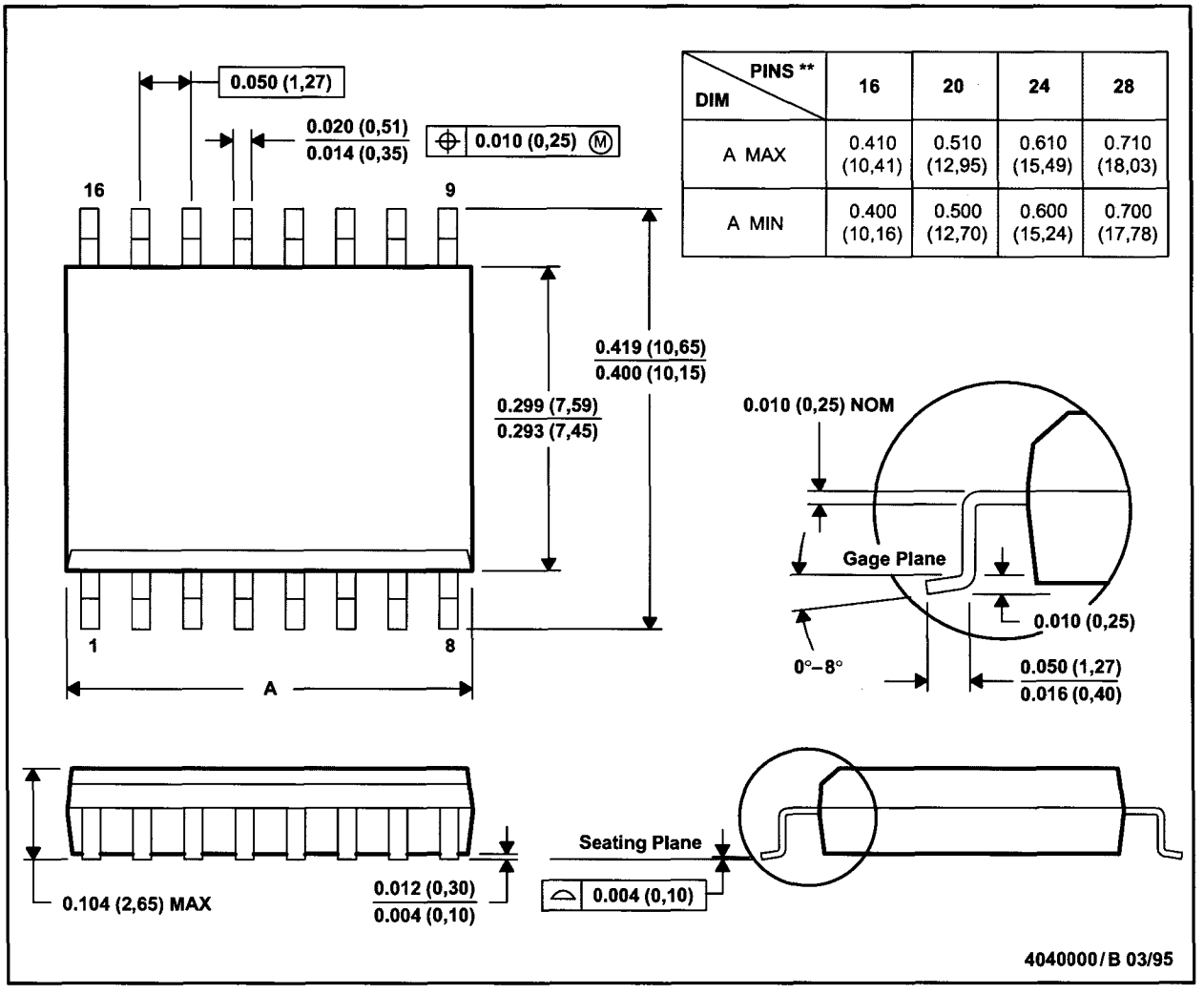
NOTE A: Resistor R ≥ 10 kΩ

Figure 15. Output Buffering Scheme

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



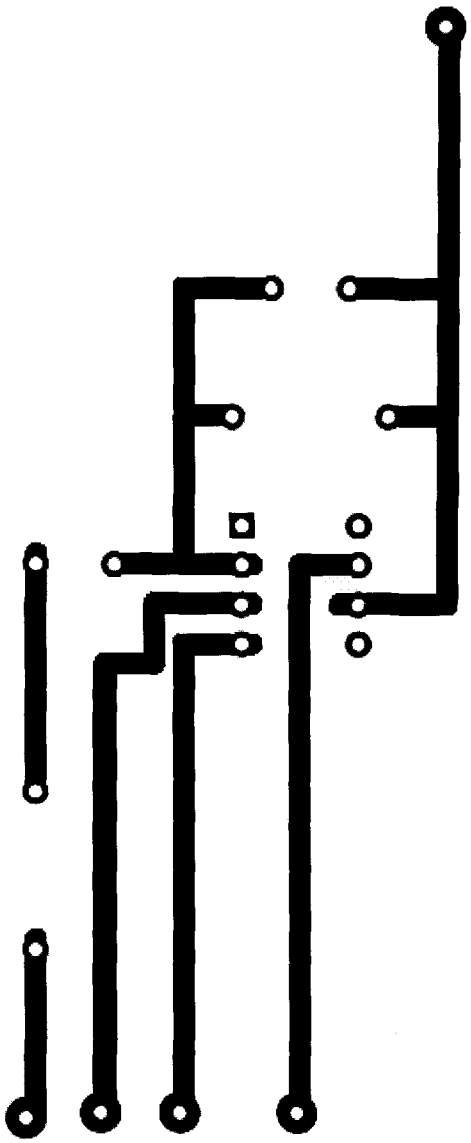
DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

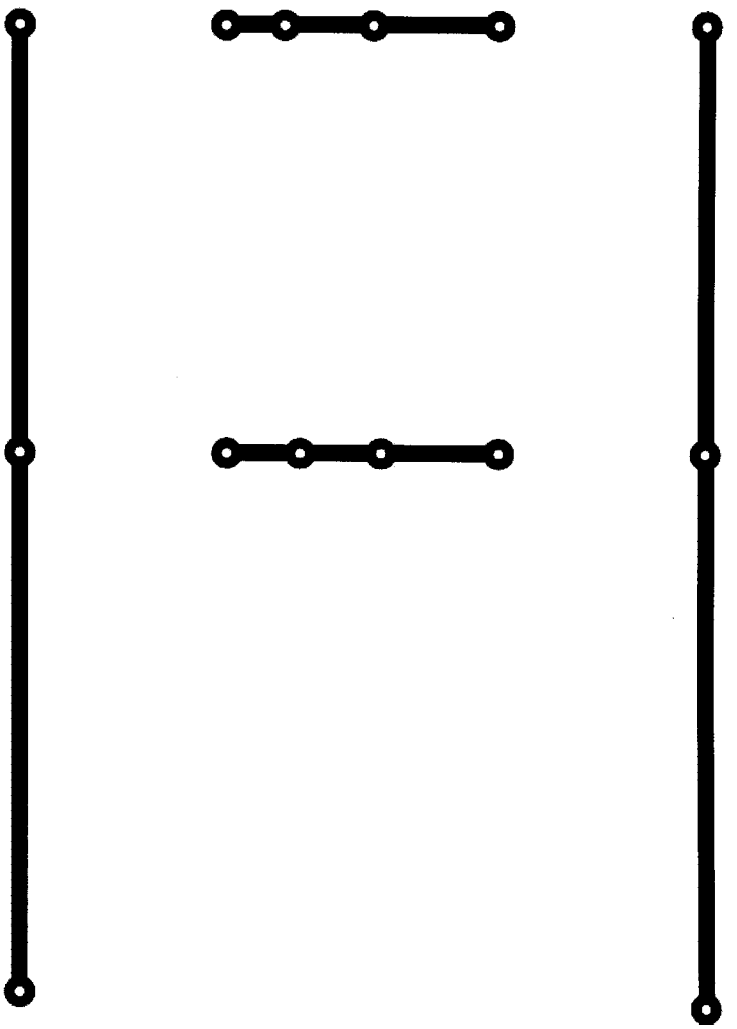
Appendix C

(TraxMaker™ PCB Designs and Circuits)

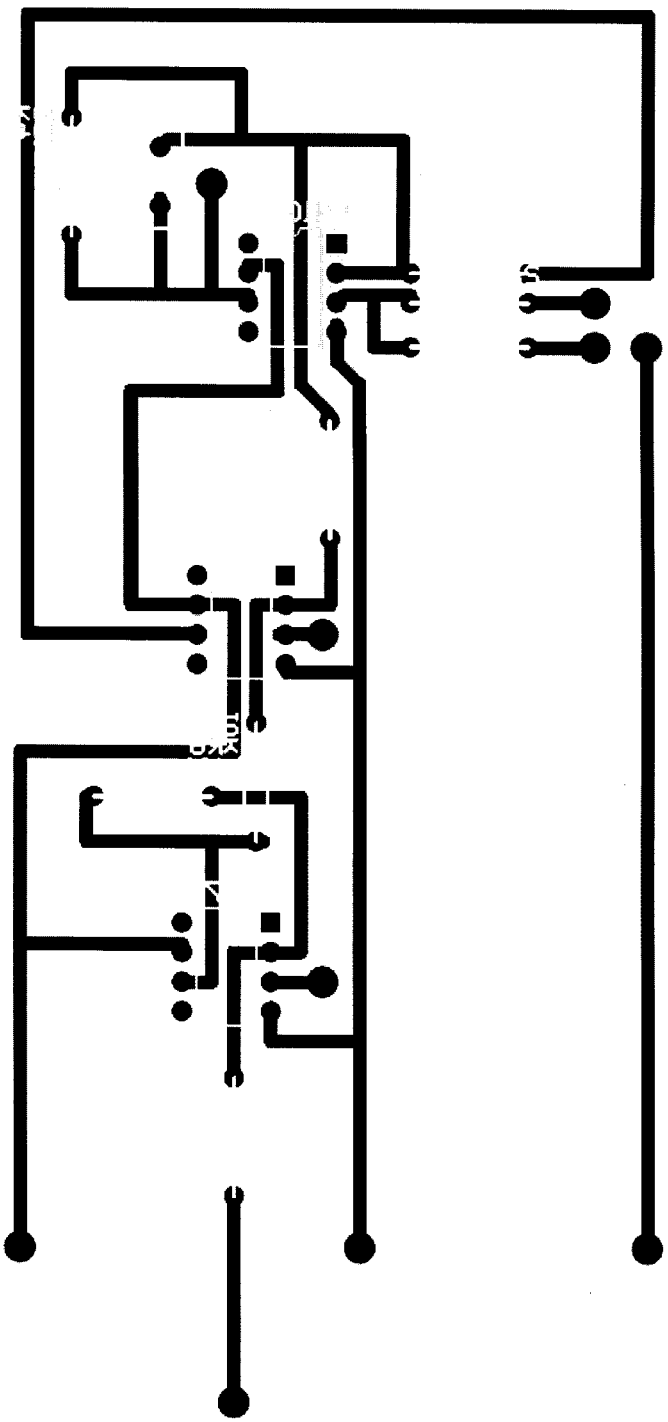
PCB Design of Analogue Sine_Cos generator



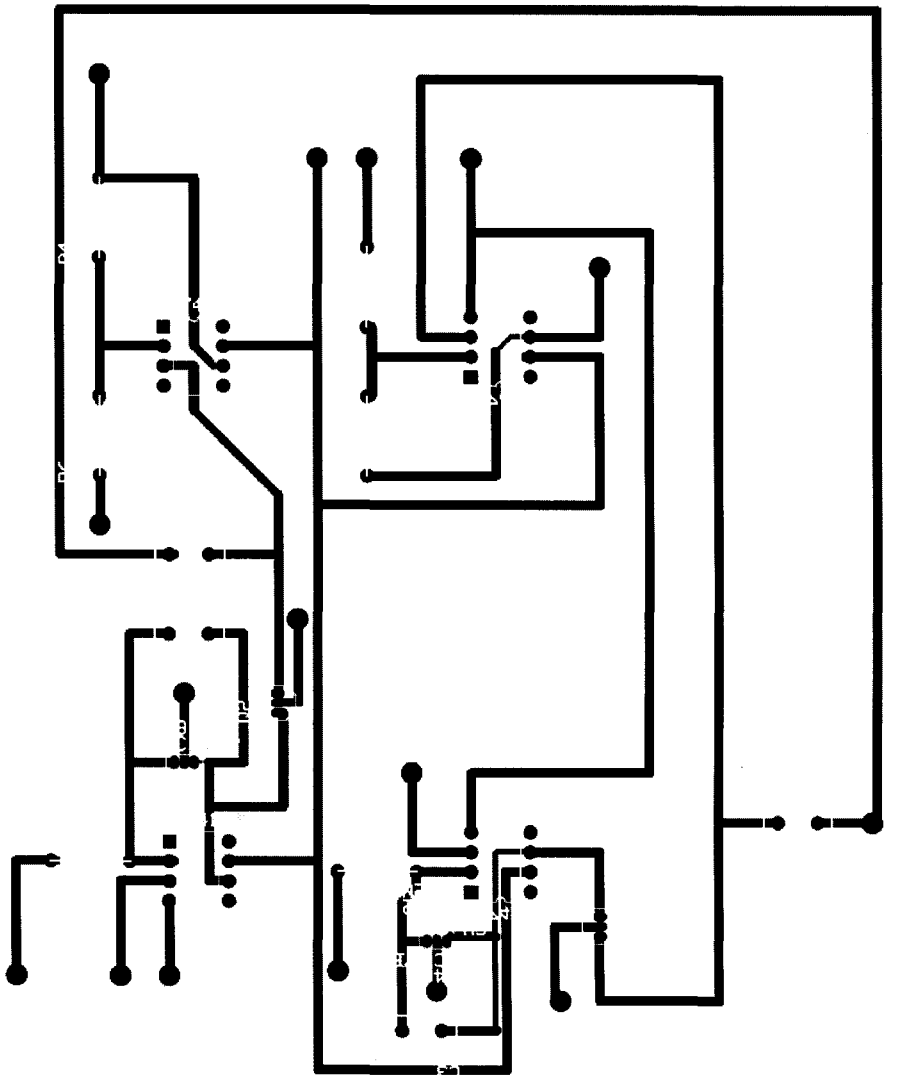
PCB Design of AC-DC Converter



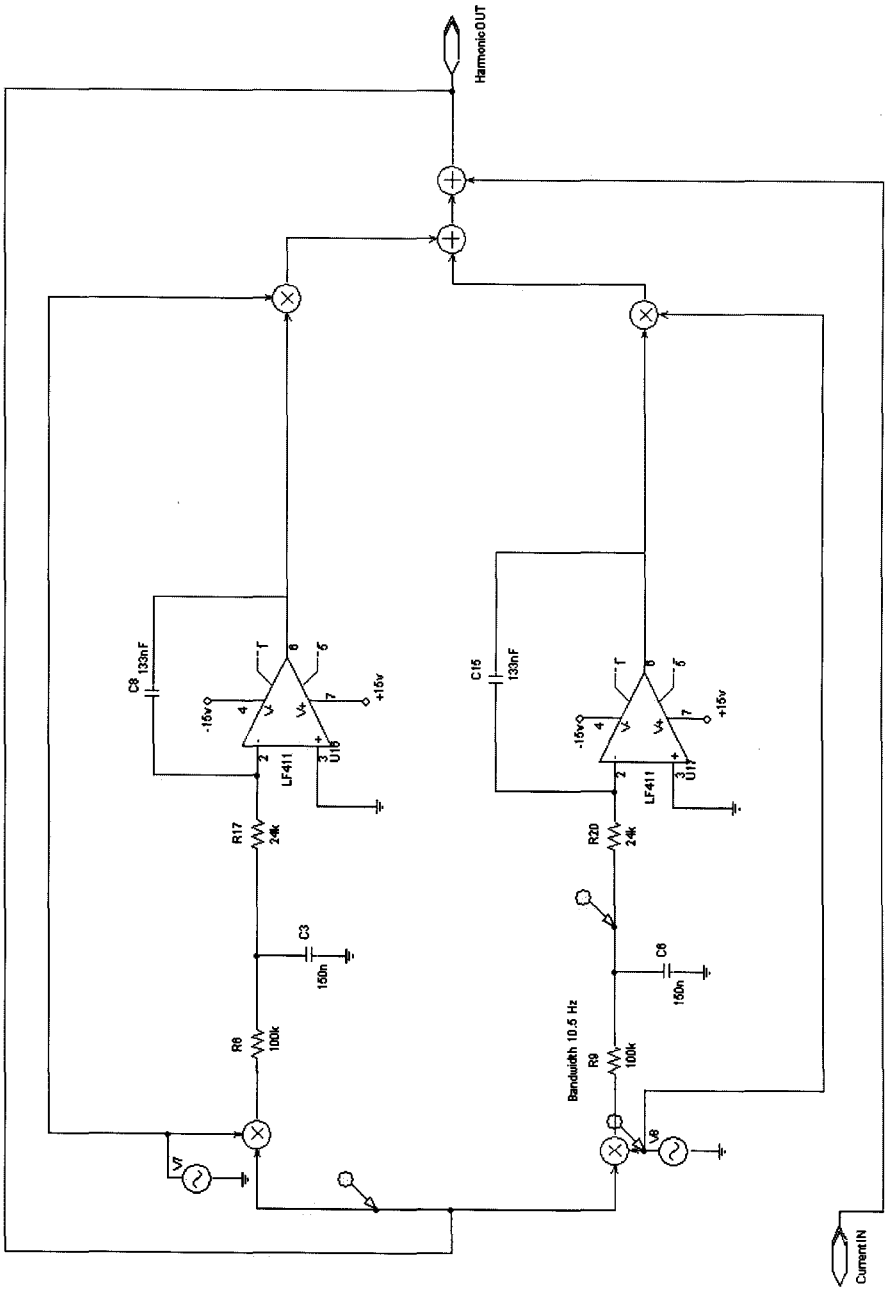
PCB Design of Capacitor DC Bus PI Controller

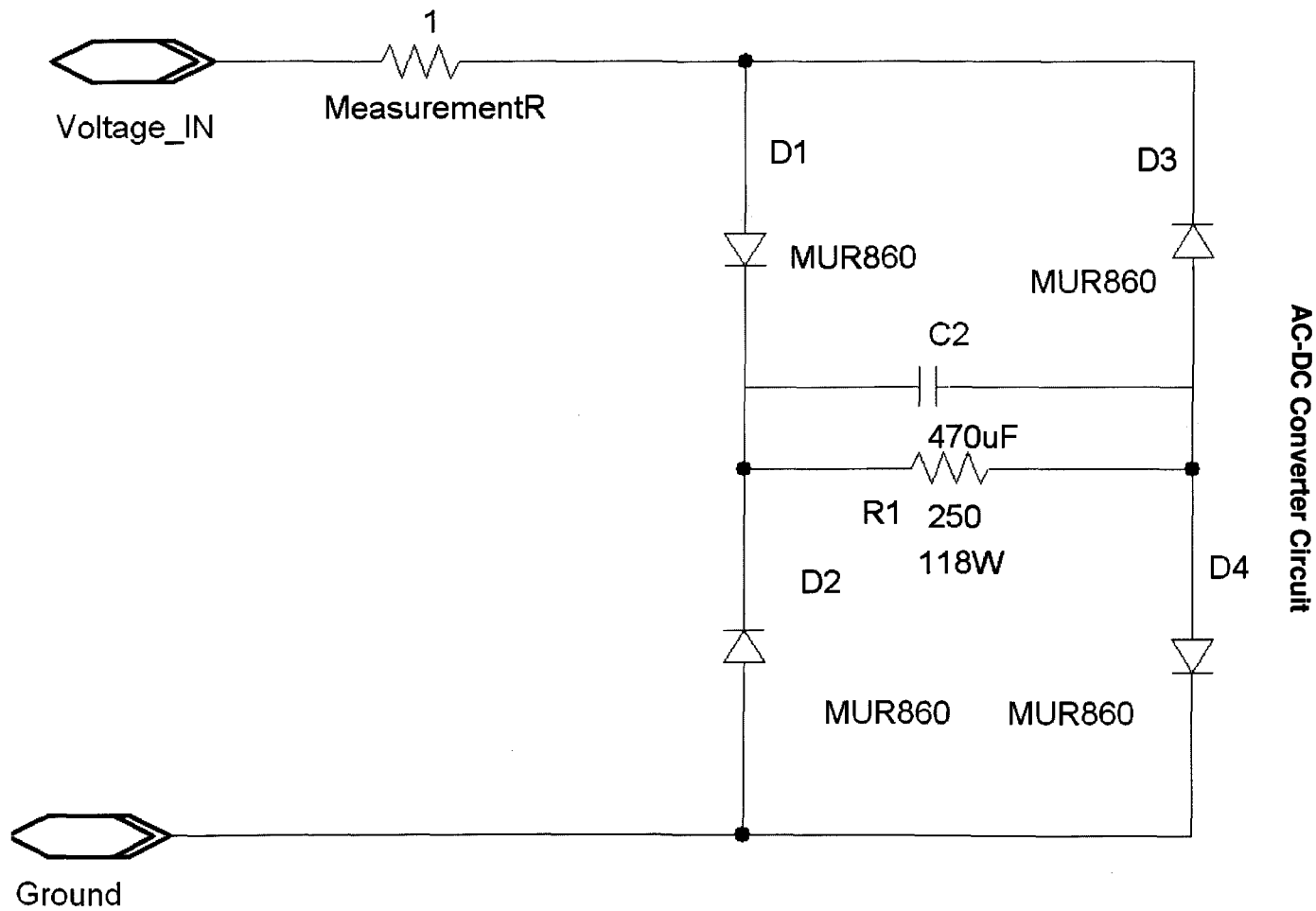


PCB Design of Harmonic Calculator

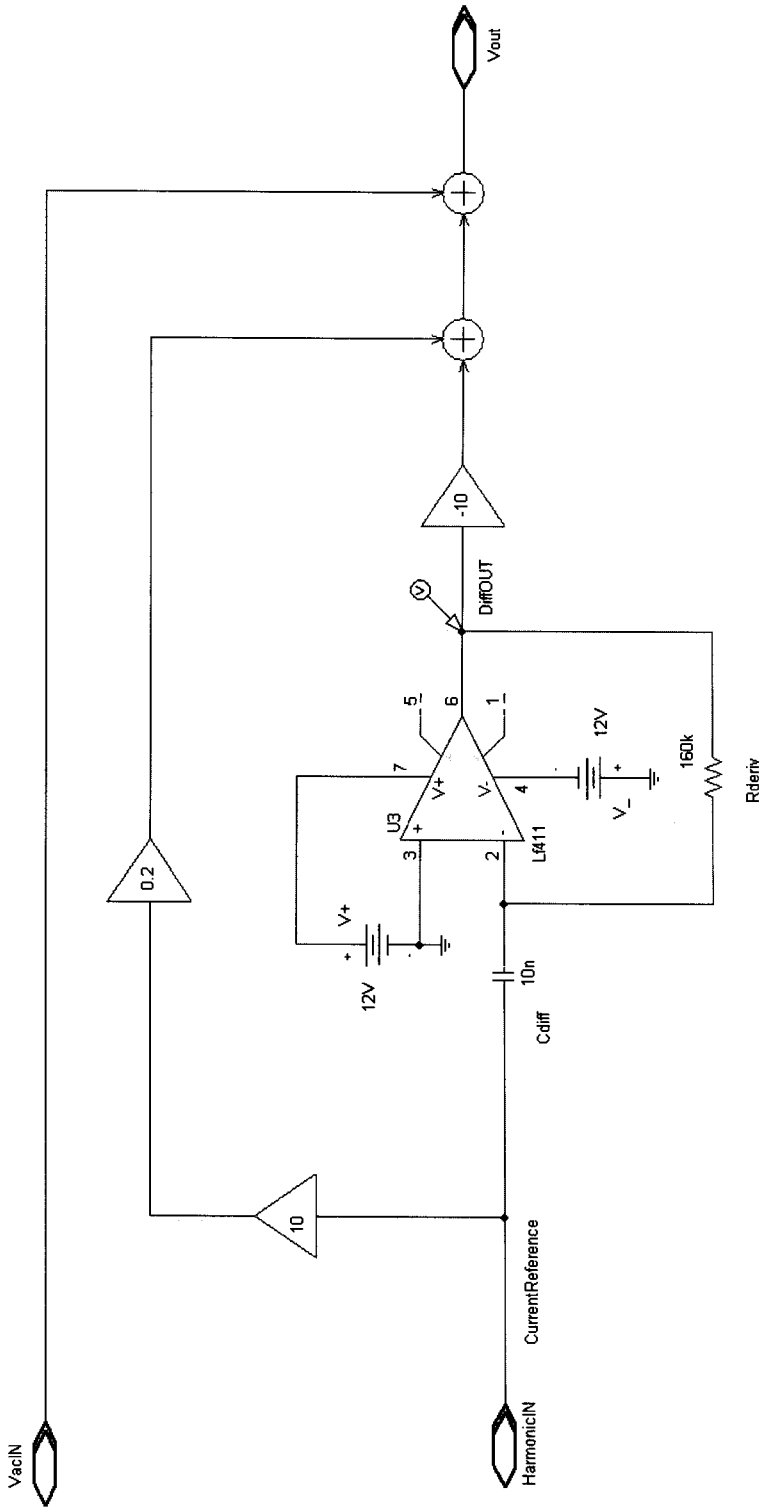


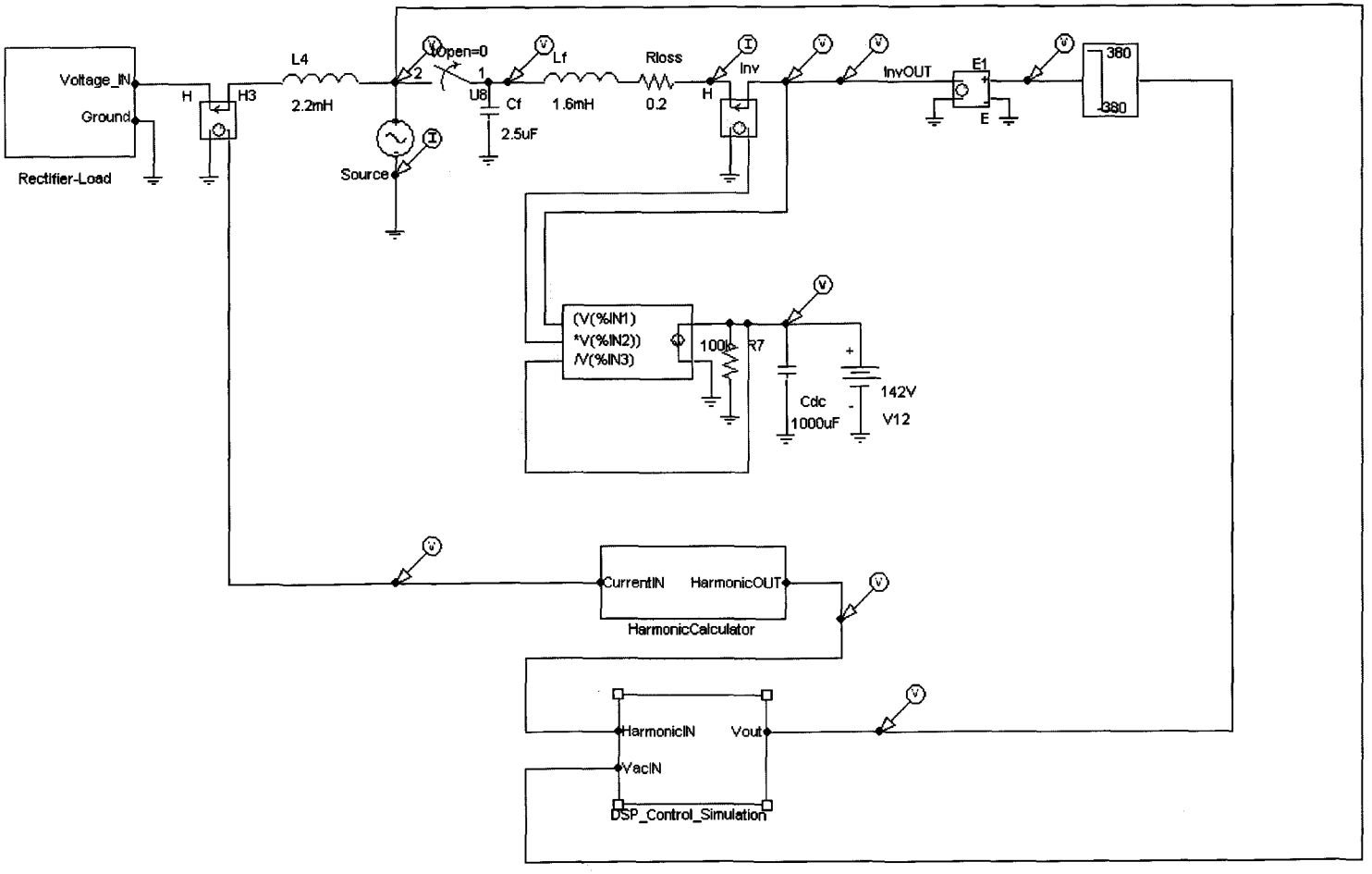
Harmonic Calculator Circuit



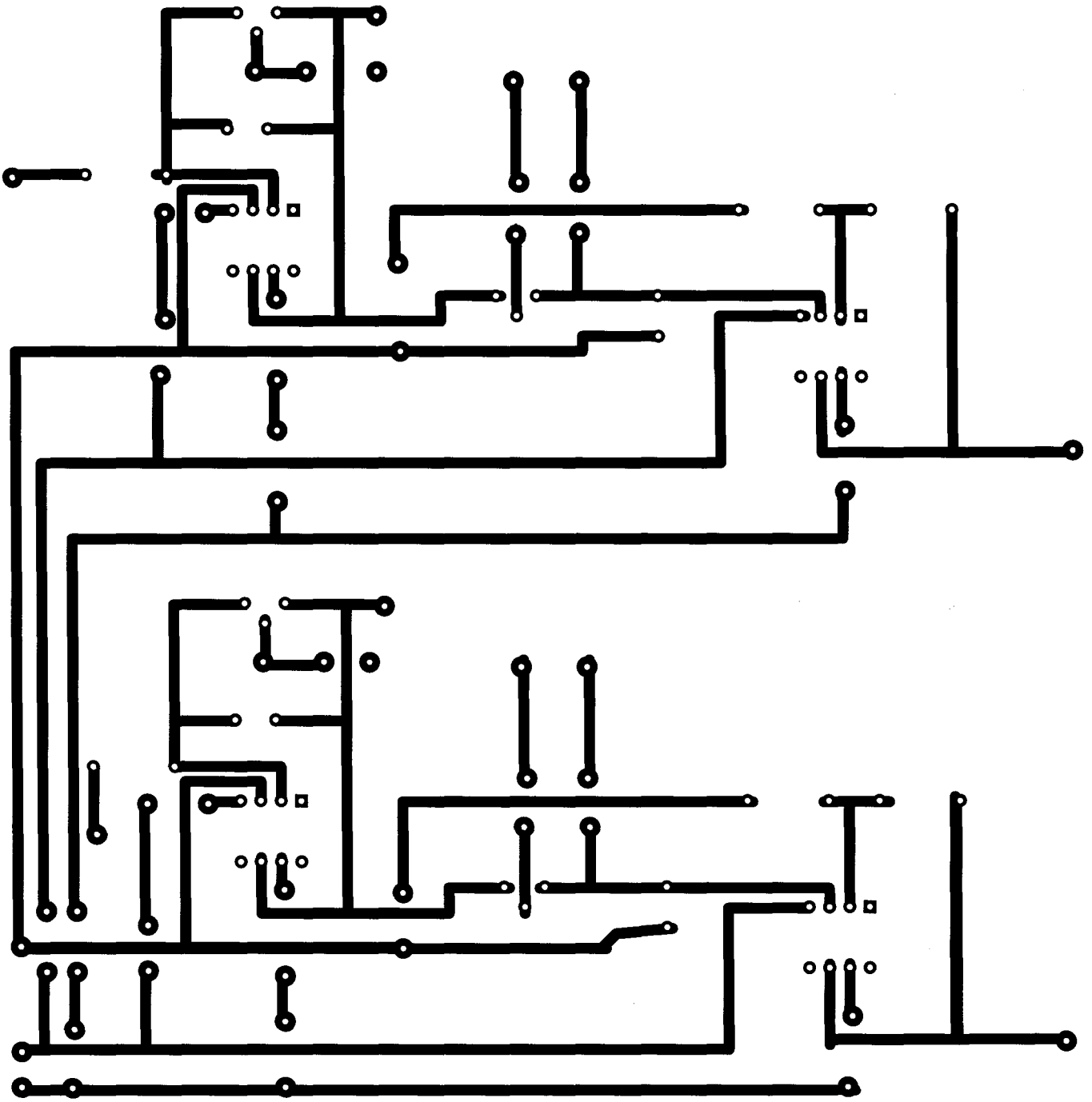

1
Voltage_IN
MeasurementR
D1
MUR860
D3
MUR860
C2
470uF
R1 250
118W
D2
MUR860
D4
MUR860
Ground
AC-DC Converter Circuit

Simulation Control Circuit



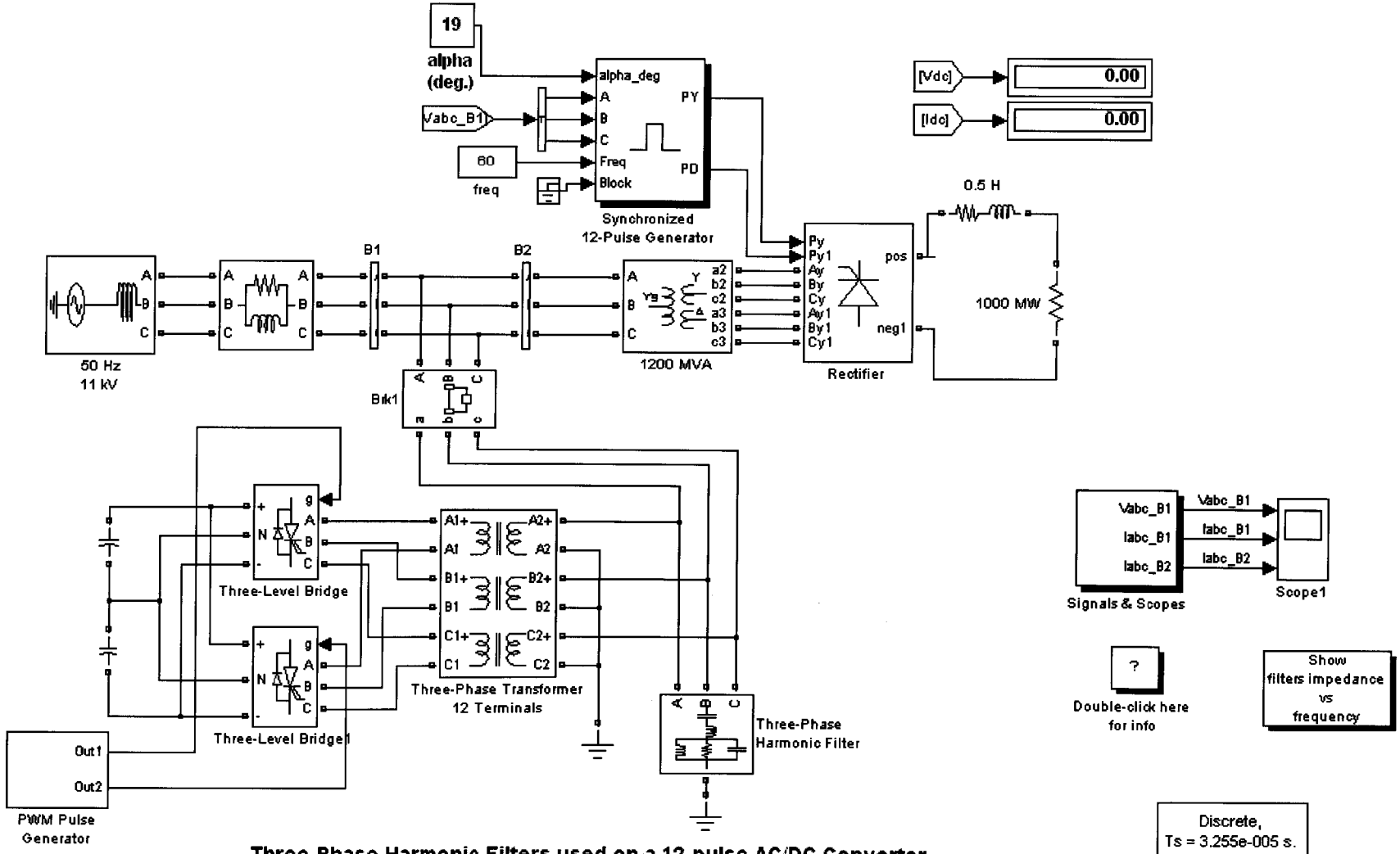


APF Complete Circuit

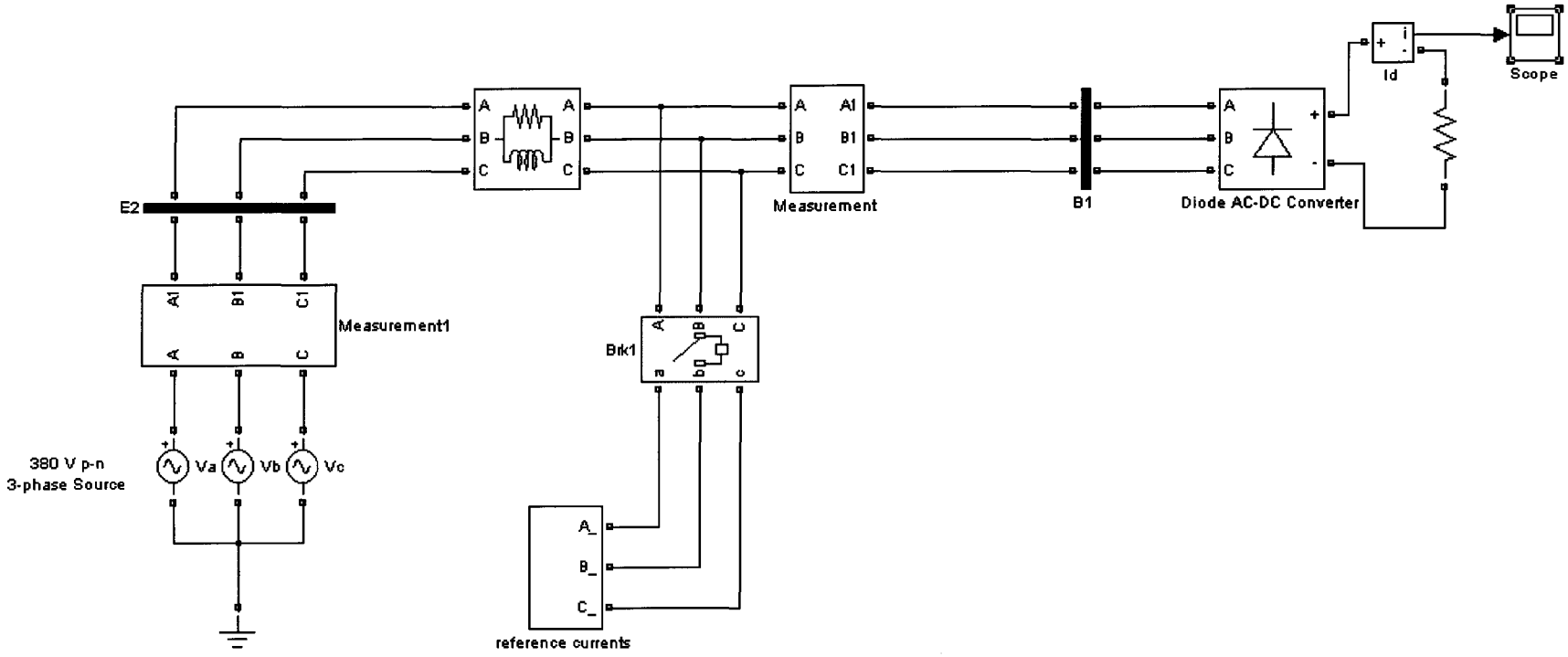


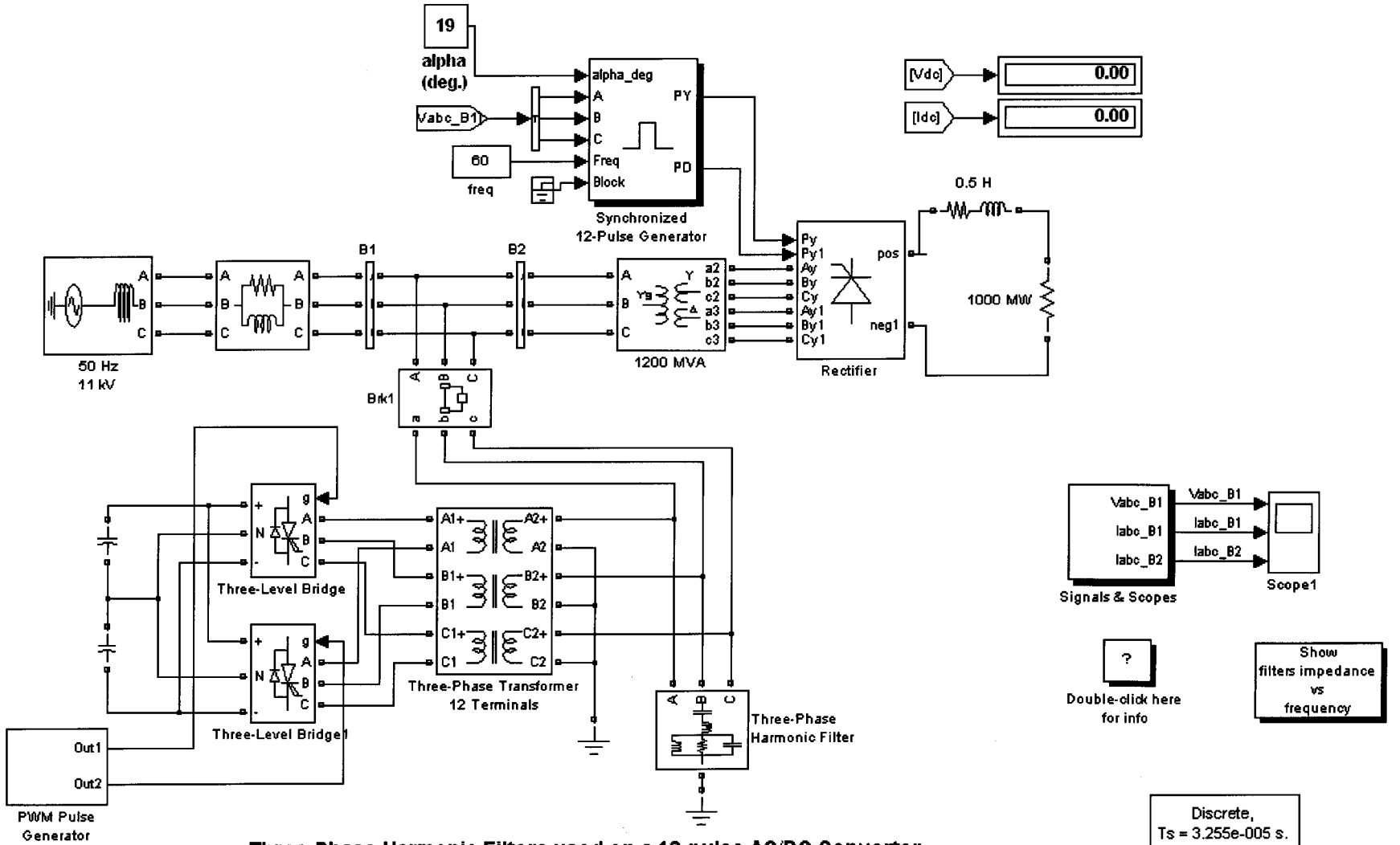
Appendix D

(Matlab Simulations)

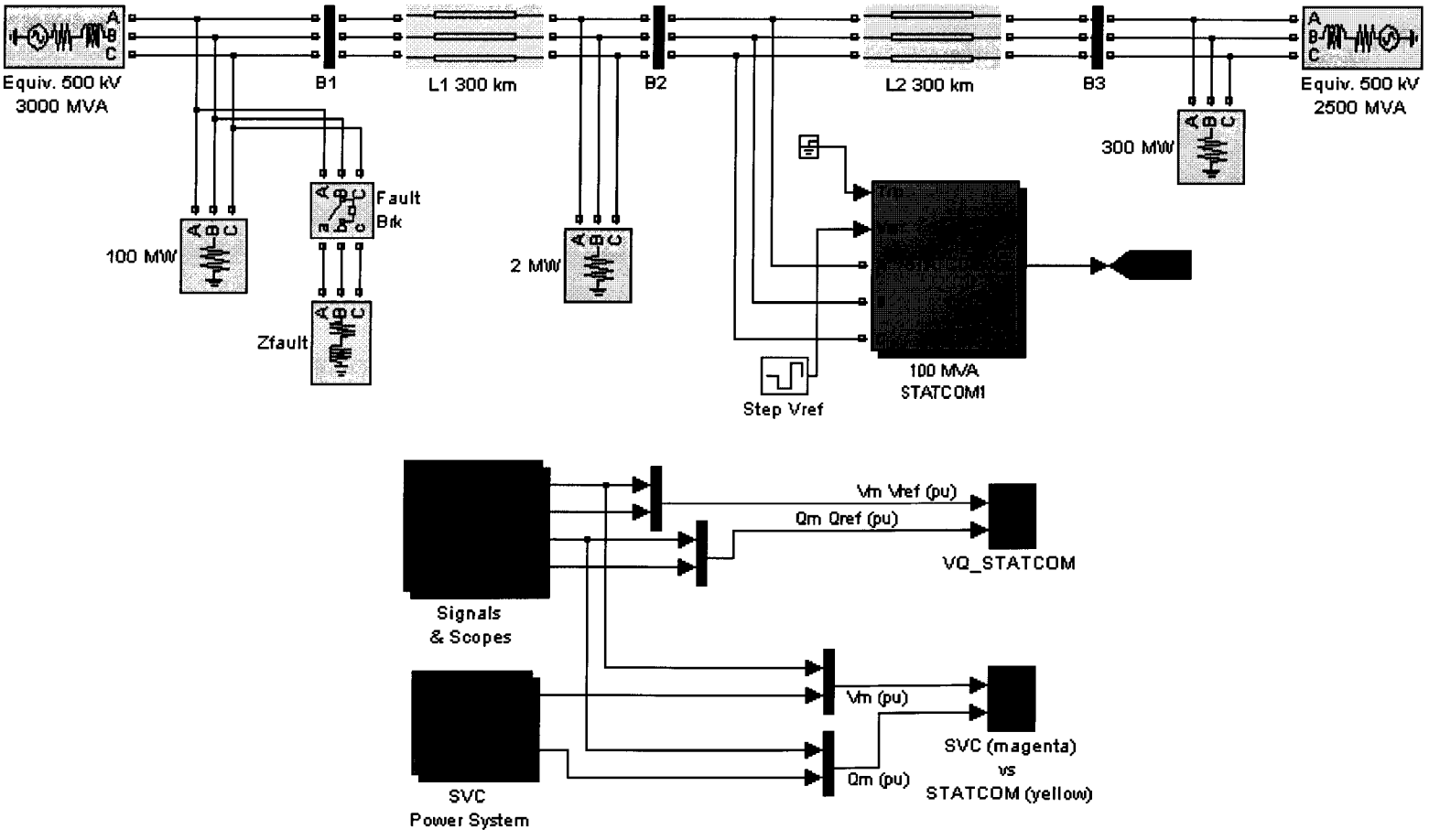


Three-Phase Harmonic Filters used on a 12-pulse AC/DC Converter

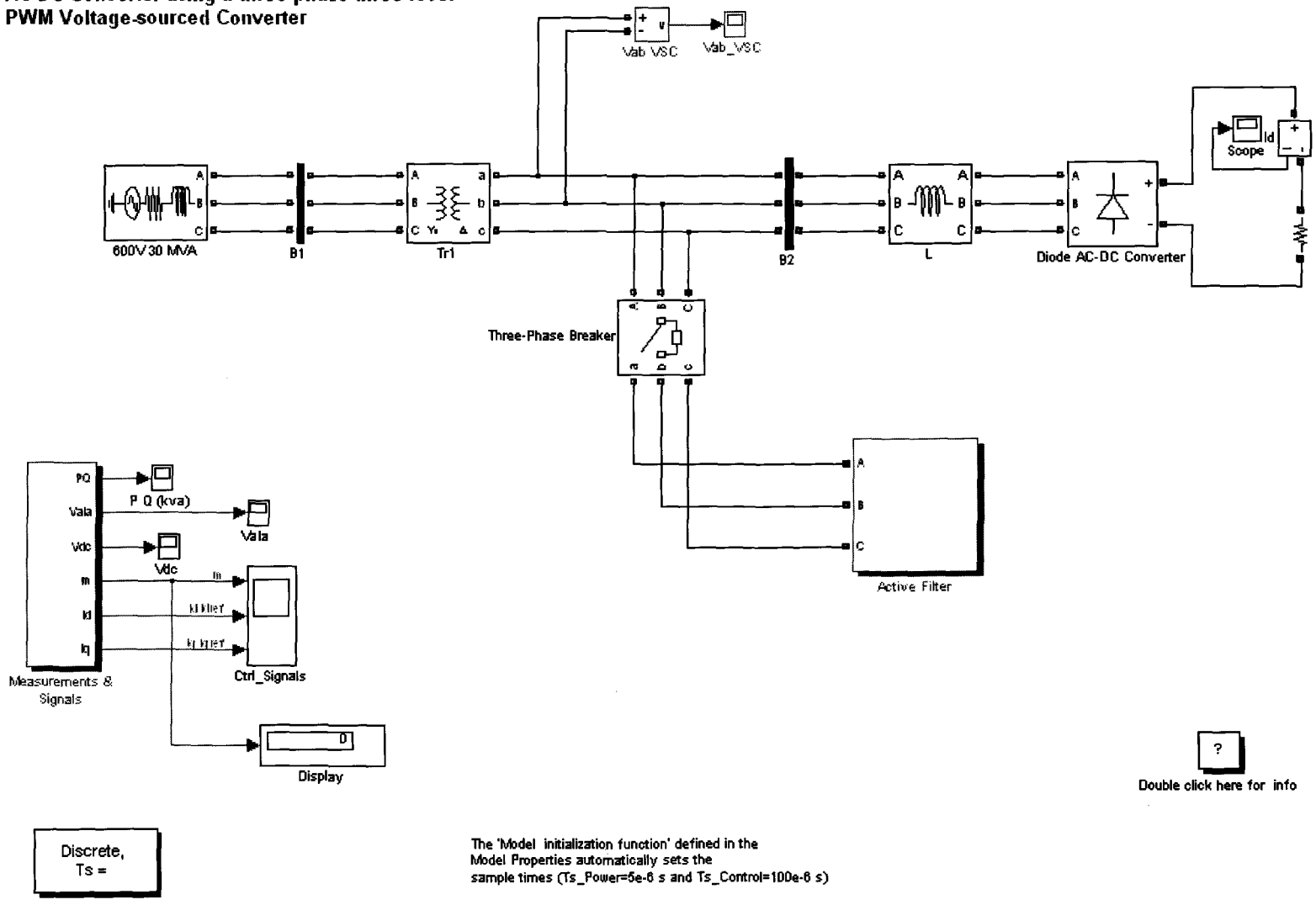

E2
A1
B1
C1
A
B
C
Measurement1
380 V p-n
3-phase Source
Va
Vb
Vc
Brk1
a
b
c
A_
B_
C_
reference currents
Measurement
B1
Diode AC-DC Converter
Id
Scope

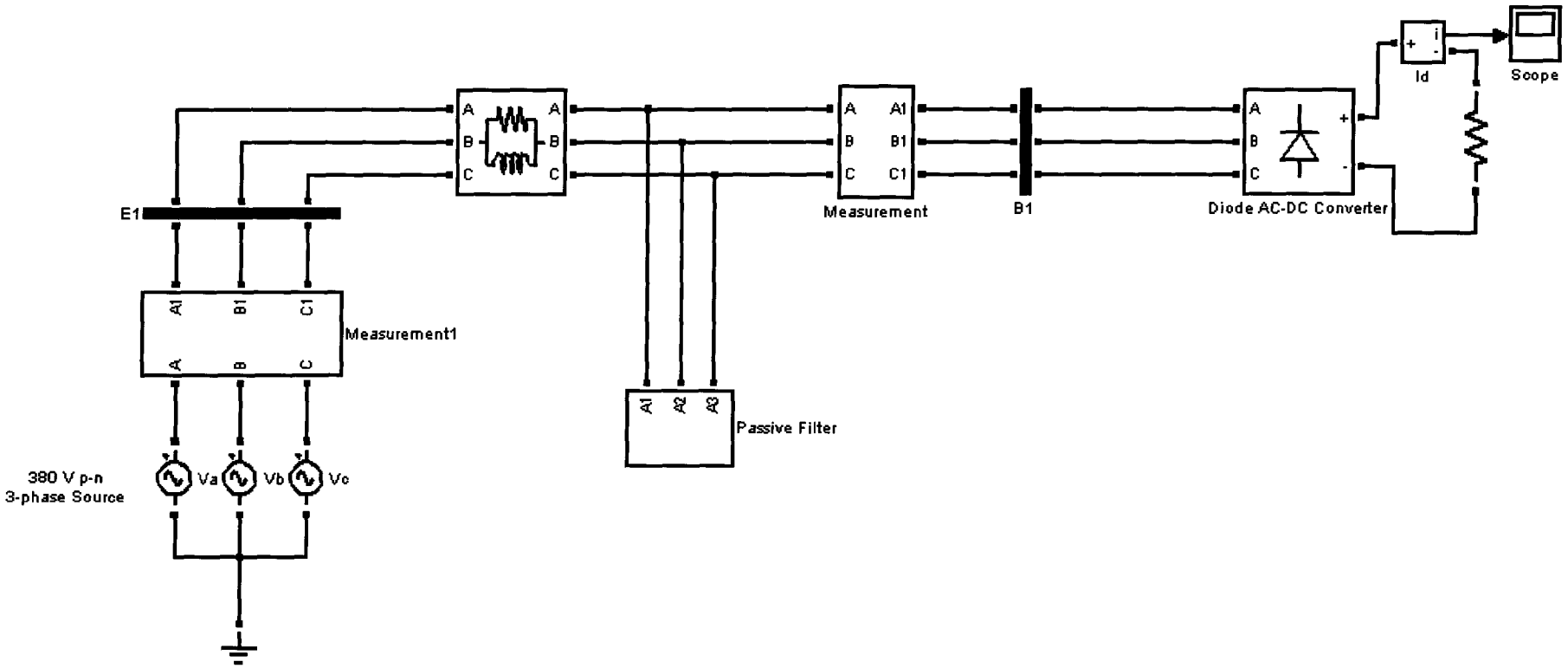


Three-Phase Harmonic Filters used on a 12-pulse AC/DC Converter


Equiv. 500 kV
3000 MVA
B1
L1 300 km
B2
L2 300 km
B3
Equiv. 500 kV
2500 MVA
300 MW
100 MW
Fault
Brk
Zfault
2 MW
100 MVA
STATCOM1
Step Vref
Signals
& Scopes
Vm Vref (pu)
Qm Qref (pu)
VQ_STATCOM
Vm (pu)
Qm (pu)
SVC (magenta)
vs
STATCOM (yellow)
SVC
Power System
Phasors
powergui
Reactive shunt compensation using a STATCOM
?
info

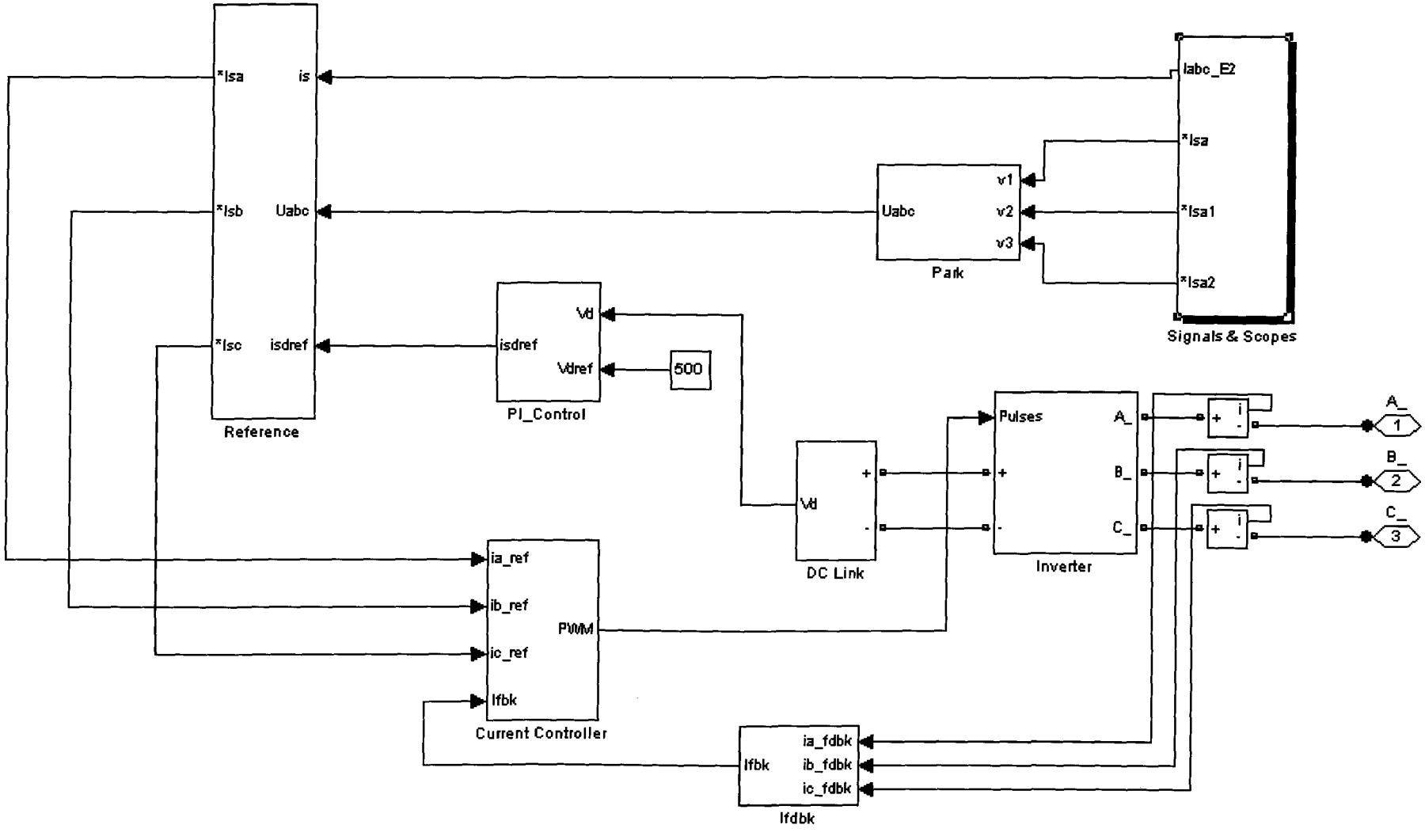
AC-DC Converter using a three-phase three-level PWM Voltage-sourced Converter

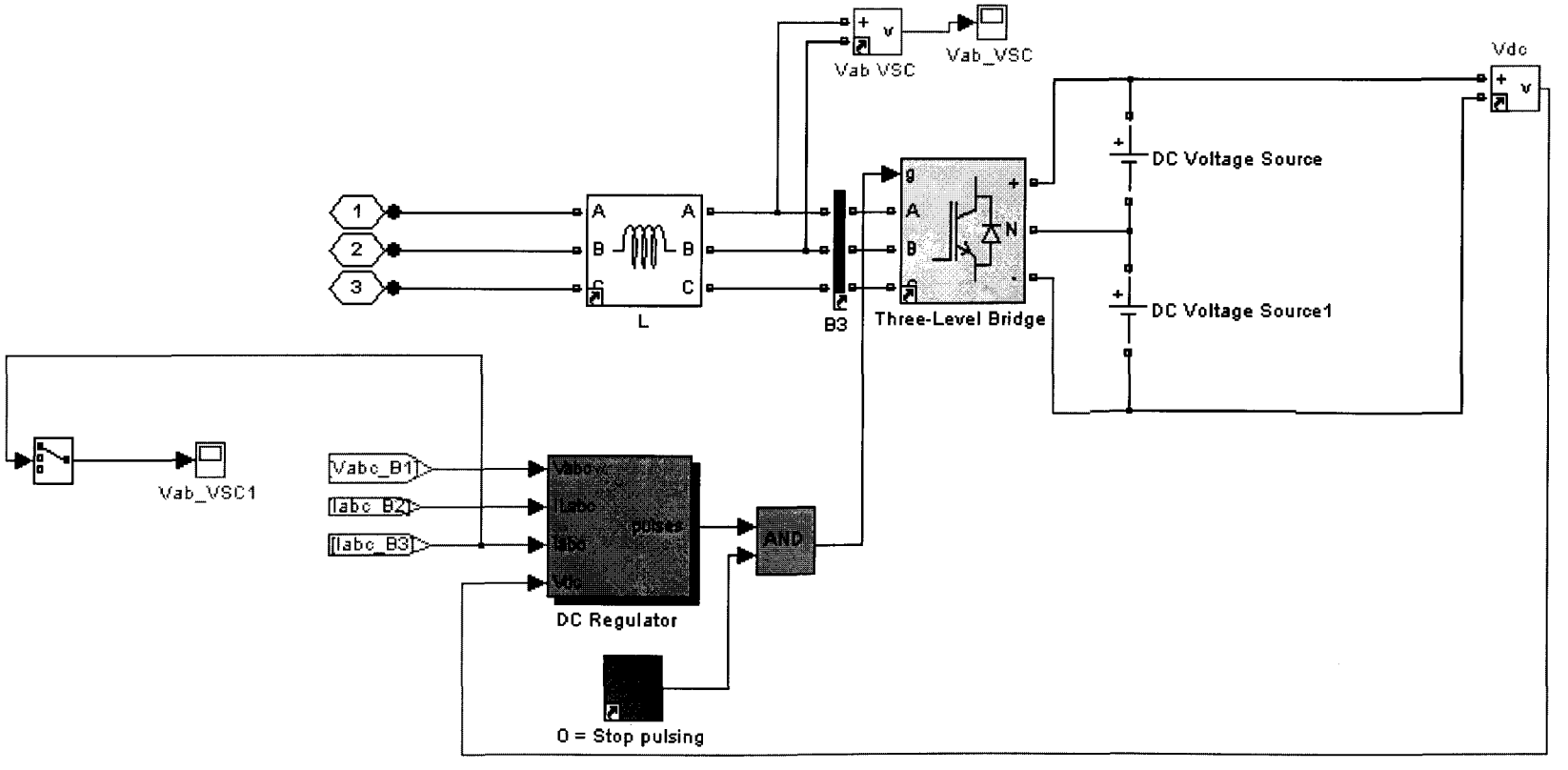




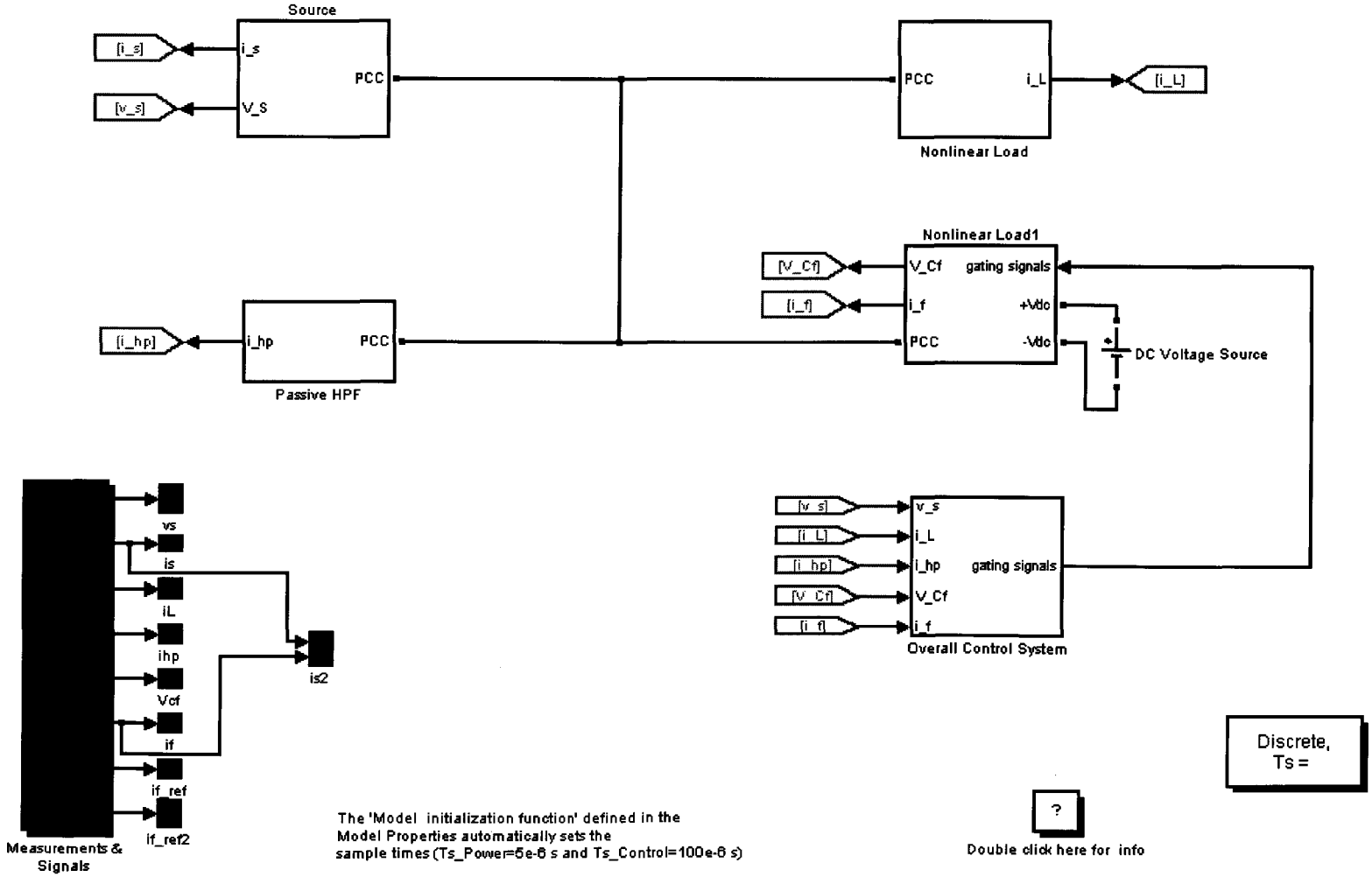
Continuous

Use the Powergui FFT tool to display the spectrum of Scope signals stored in the 'psbconverter_str' structure.


*Isa
is
*Isb
Uabc
*Isc
isdref
Reference
Iabc_E2
*Isa
*Isa1
*Isa2
Signals & Scopes
Uabc
v1
v2
v3
Park
isdref
Vd
Vdref
500
PI_Control
Vd
+
-
DC Link
Pulses
+
-
A_
B_
C_
Inverter
A_
B_
C_
1
2
3
ia_ref
ib_ref
ic_ref
Ifbk
PWM
Current Controller
Ifbk
ia_fdbk
ib_fdbk
ic_fdbk
Ifdbk


Vab VSC
Vab_VSC
Vdc
DC Voltage Source
DC Voltage Source1
1
2
3
A
B
C
L
B3
Three-Level Bridge
Vab_VSC1
Vabc_B1
Iabc_B2
Iabc_B3
Vdc
pulses
DC Regulator
AND
0 = Stop pulsing

Power Active Filter using a three-phase three-level PWM Voltage-sourced Inverter



The 'Model initialization function' defined in the Model Properties automatically sets the sample times (Ts_Power=5e-6 s and Ts_Control=100e-6 s)